LOW-VOLTAGE HIGH-EFFICIENCY ANALOG-TO-DIGITAL CONVERTER FOR BIOMEDICAL SENSOR INTERFACE

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DECLARATION

I hereby declare that this thesis is my original work and it has been written by me in its entirety.

I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Wen-Sin Liew

ACKNOWLEDGMENT

I want to express my deepest gratitude toward my project supervisor Professor Lian Yong. I sincerely thank him for the valuable guidance, continuous encouragement, financial support, and freedom he gave me throughout my research work. The sharing of his profound knowledge and abundant experience has been of great value for me. I owe my success to him.

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Wen-Sin Liew

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ABSTRACT

Many recent works focus on single-chip integration solution in order to transform the conventional bulky and stationary biomedical instrumentation device into a portable or implantable device which will be powered through inductive link or battery with very limited power capacity. This calls for the development of low-power sensor circuits which include low-noise front-end amplifier, analog-to-digital converter (ADC), and radio transceiver. Among different blocks, this work focuses on the design of low-power high-efficiency ADC dedicated for biomedical sensor interface.

Firstly, an energy-efficient dual-capacitive-array architecture for successive approximation (SA) ADC is proposed. Unlike conventional topologies, the proposed architecture utilizes two capacitive arrays for quantization to reduce the switching energy in capacitive array. Additionally, the proposed design is a low-voltage rail-to-rail ADC without the need of rail-to-rail comparator. The ADC is fully dynamic and is optimized for low power dissipation while maintaining its accuracy. A 10-bit 10-kS/s ADC prototype fabricated in a standard 0.35-μm CMOS technology achieves an ENOB of 9.07 bits at rail-to-rail input swing while dissipating 170 nW from a 0.8-V supply. The ADC attains a figure-of-merit (FOM) of 32 fJ/conversion-step.

Secondly, digital multiplexing scheme is introduced for the ADC design in multi-channel biomedical recording interface. An 8-channel SA ADC based on digital multiplexing is presented to facilitate multiplexing among channels and thus eliminates the need for analog multiplexer and associated power-consuming buffers. The prototype 8-channel ADC was fabricated in a standard 0.13-μm CMOS technology with an active area of 0.15 mm^2. It consumes 1.23 μW from a 0.6-V

supply. At 30-kS/s-per-channel sampling rate, the proposed design achieves a mean ENOB of 7.59 bits, which can be translated into a FOM of 26.6 fJ/conversion-step.

Lastly, both of the proposed designs were integrated into practical biomedical sensor interface and verified through actual clinical trial and *in-vivo* test. All results show good recording quality.

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LIST OF ABBREVIATIONS

AD	Analog-to-Digital
ADC	Analog-to-Digital Converter
CMRR	Common Mode Rejection Ratio
DAC	Digital-to-Analog Converter
DNL	Differential Nonlinearity
ECG	Electrocardiograph
EEG	Electroencephalograph
ENOB	Effective Number of Bits
FOM	Figure of Merit
FS	Full Scale
INL	Integral Nonlinearity
LSB	Least Significant Bit
MUX	Multiplexer
MSB	Most Significant Bit
PSD	Power Spectral Density
SA	Successive Approximation
SAR	Successive Approximation Register
SFDR	Spurious-Free Dynamic Range
SNDR	Signal to Noise and Distortion Ratio
S/H	Sample-and-Hold
S/s	Sample-per-Second

CHAPTER 1

INTRODUCTION

1.1 Research Background

Bioinstrumentation is a very effective diagnostic and health monitoring tool [1]. For example, the monitoring of heart diseases can be done with the help of electrocardiograph (ECG); while electroencephalograph (EEG) is commonly used in the diagnosis of epilepsy, coma, and brain death. On the other hand, research in brain-machine interfaces has shown success in decoding electronic signals from the motor cortex of the brain to control artificial limbs in both primates and humans, providing hope for patients with spinal cord injuries, Parkinson's disease, and other debilitating neurological conditions [2]. However, commercially-available bioinstrumentation system is wired, stationary, and bulky. This calls for the development of miniature wireless sensor interface which is portable or implantable.

Recent works focus on single-chip solution in order to minimize the device size [3-13]. Fig. 1.1 shows a typical wireless sensor interface chip. It integrates the recording front-end, data processing unit, radio transceiver, clock generation, and power supply unit on the same silicon die. To enable portability and implantability, this miniature device is to be powered through wireless inductive link [3, 5, 8], energy harvesting [14, 15], miniature battery [16], or bio-fuel cell [17, 18] with very limited power capacity. Consequently, low-power operation and energy-efficiency are among the major challenges in designing the miniature wireless sensor interface in order to maximize the signal recording duration.

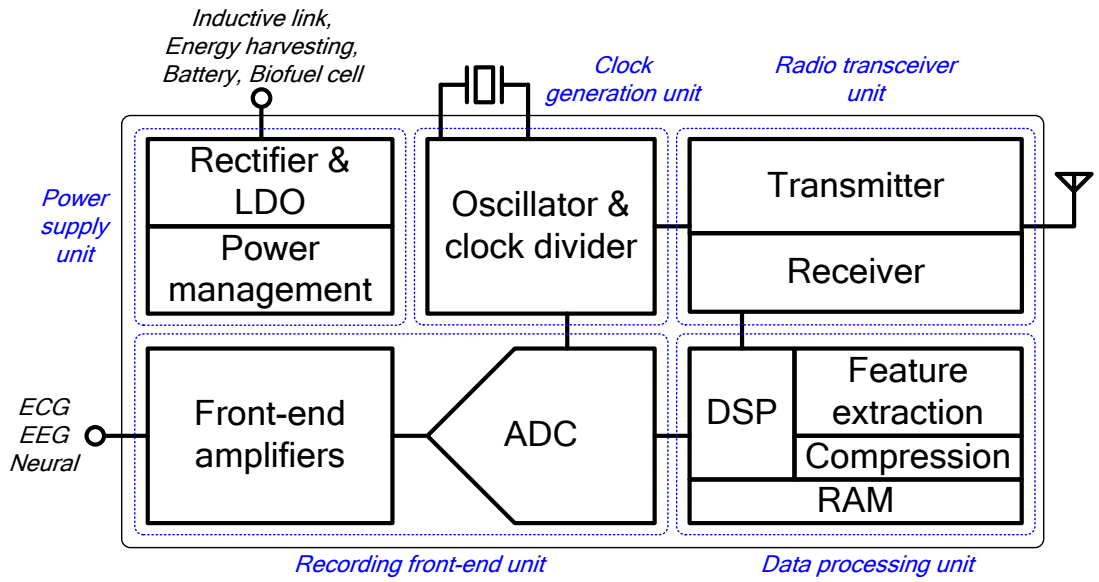

Fig. 1.1. Typical wireless sensor interface chip.

Both system-level and circuit-level optimizations are necessary to achieve low-power operation and high energy efficiency for the interface chip shown in Fig. 1.1. At system level, customized digital signal processing (e.g. feature extraction, data compression, etc.) and on-chip data buffering using random access memory (RAM) are needed to duty-cycled the radio transceiver unit which typically dissipates highest instantaneous power. Additionally, power management unit is used to power-gate the inactive modules and put them into sleep. On the other hand, much effort is required to design and optimize individual module at circuit level, especially for recording front-end unit which has to stay active throughout the entire signal acquisition period.

A recording front-end unit generally consists of low-noise front-end amplifiers and analog-to-digital converter (ADC). The low-noise front-end amplifiers are used for signal conditioning and amplification while the ADC digitizes the signal for further processing. Both of the low-noise amplifiers and ADC must dissipate as little power as possible without sacrificing any recording performance to maximize the overall

energy efficiency. The designs of low-power front-end amplifier were discussed by my main project partner Dr. Xiaodan Zou in her work [19] and many other publications [20-25]. Therefore, my work focuses on the design of energy efficient ADC.

1.2 Research Objectives

The main objective of my work is to develop an energy-efficient ADC with best figure of merit (FOM). The commonly used FOM for ADC is the amount of energy required to complete one conversion step. The lower this FOM, the better is the ADC performance in terms of energy efficiency.

Furthermore, the ADC should also operate from a supply as low as possible to facilitate its integration with low-voltage digital circuitry. In fact, low-voltage operation not only relaxes the design specifications on power link and supply regulator but is also effective in reducing dynamic power dissipation. However, low-voltage supply also demands rail-to-rail input range to boost the ADC dynamic range.

Moreover, it is preferable that the ADC readily supports multiple channels because almost all of the biomedical sensor applications need more than one channel to effectively record all of the relevant signals. For example, a 12-lead ECG requires at least 8 recording channels, typical EEG monitoring demands more than 32 channels, neural recording may need as many as 100 channels or more, and so on.

Additionally, the ADC, which mainly aims for the use in bioinstrumentation, is designed with medium resolution (8-12 bits) and relatively low sampling rate (<10 kS/s).

Last but not least, the ADC must be system-compatible and thus the overheads of integrating the ADC into a sensor system have to be minimized. For instance, ADC input loading has to be small so that it will not load the preceding stage; ADC input clock has to be as slow as possible to avoid the use of high-speed clock source.

1.3 Research Contributions

The main contributions of my research works are in the design of low-voltage high-efficiency ADC dedicated for biomedical sensor interface and the practical applications based on the proposed ADC design.

A dual-capacitive-array ADC architecture is proposed for ECG and EEG sensor application. This architecture aims for low-voltage low-power operation. The chip prototype based on the proposed ADC architecture achieves a FOM of 32 fJ/conversion-step under a 0.8-V supply, comparing favorably to other low-power ADC designs for biomedical application. Furthermore, a low-power EEG sensor interface incorporating the proposed ADC design confirms its performance in practical biomedical sensor implementation.

In the design of multi-channel biomedical signal recording interface, for instance a neural recording interface, the power and area consumption of each individual channel is crucial to minimize the total power and area of the overall system. A multi-

channel ADC based on digital multiplexing scheme is proposed, which eliminates the need of analog multiplexer and power-consuming driving buffer. The ADC alone achieves a 26.6-fJ/conversion-step FOM, which is comparable to other state-of-the-art designs. Moreover, this design is the first to demonstrate a low-voltage multi-channel ADC. A neural recording interface was built using this proposed ADC. The recording interface was verified through *in-vivo* neural recording and neural spikes were clearly recorded.

1.4 List of Publications and Achievements

Listed below are publications and achievements generated from my research works (in chronological order):

[1] W.-S. Liew, L. Yao, and Y. Lian, "A moving binary search SAR-ADC for low power biomedical data acquisition system," in *Proc. of the IEEE Asia Pacific Conf. on Circuits and Systems (APCCAS)*, Macao, 2008, pp. 646-649.

[2] W.-S. Liew and Y. Lian, "A 1-V 60-μW 16-channel interface chip for multimodality neurophysiological signals," presented at *IEEE Int. Solid-State Circuits Conf. (ISSCC) Student Forum*, San Francisco, 2009.

[3] W.-S. Liew, X. Zou, L. Yao, and Y. Lian, "A 1-V 60-μW 16-channel interface chip for implantable neural recording," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, San Jose, 2009, pp. 507-510.

[4] X. Zou, W.-S. Liew, L. Yao, and Y. Lian, "A 1V 22μW 32-channel implantable EEG recording IC," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, 2010, pp. 126-127.

[5] W.-S. Liew, L. Yao, and Y. Lian, Winner of *47th DAC/ISSCC Student Design Contest* on "A 0.8-V 32-fJ/conversion-step dual-capacitive-array successive approximation analog-to-digital converter," 2010.

[6] W.-S. Liew, X. Zou, and Y. Lian, "A 0.5-V 1.13-μW/channel neural recording interface with digital multiplexing scheme," in *Proc. European Solid-State Circuits Conf. (ESSCIRC)*, Helsinki, 2011, pp. 219-222.

[7] M. Khayatzadeh, X. Zhang, J. Tan, W.-S. Liew, and Y. Lian, "A 0.7-V 17.4-μW 3-lead wireless ECG SoC," in *Proc. of the IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Hsinchu, 2012.

[8] J. Tan, W.-S. Liew, C.-H. Heng, and Y. Lian, "A 2.4GHz ULP reconfigurable asymmetry transceiver for single-chip wireless neural recording IC," submitted for journal publication.

[9] W.-S. Liew and Y. Lian, "A 0.6-V 8-bit 8-channel rail-to-rail SA ADC with dual-capacitive-array for multi-channel biomedical sensor interface," submitted for journal publication.

1.5 Organization of the Thesis

This thesis is organized as follows:

CHAPTER 2 reviews the conventional ADC design for biomedical recording interface. State-of-the-art ADC designs are included and investigated. Various techniques to improve the ADC energy efficiency are discussed in this chapter.

CHAPTER 3 presents the proposed dual-capacitive-array ADC architecture, including the detailed description and circuit implementation for each of the functional blocks. The functioning and advantages of the proposed dual-capacitive-array architecture will be explained. In addition, chip verification, measurement results, and example on practical EEG sensor application will also be presented.

CHAPTER 4 proposes multi-channel ADC with digital multiplexing scheme dedicated for multi-channel biomedical sensor interface. Chip verification and measurement results are presented. Example on practical neural recording application will also be provided.

CHAPTER 5 summarizes and concludes my research works.

CHAPTER 2

SUCCESSIVE APPROXIMATION ADC

2.1 ADC Architecture for Low-Power Biomedical Sensor Interface

There are many different ADC architectures. For example, flash, folding, pipelined, sigma-delta (ΣΔ), successive approximation (SA or commonly known as SAR), and so on [26-28]. In order to select the most suitable architecture to implement the ADC in a low-power biomedical sensor interface, we need to consider the respective ADC sampling rate, resolution, and energy efficiency.

Fig. 2.1 and Fig. 2.2 show some of the most popular ADC architectures in terms of resolution and FOM. Both figures are based on the data adopted from [29], which includes state-of-the-art designs published in recent International Solid-State Circuits Conference (ISSCC) and Symposium on VLSI Circuits.

Fig. 2.1 shows the achieved ADC resolution versus Nyquist sampling rate for different architectures. It is obvious that flash, folding, and pipelined are aiming for high-speed system (>10 MS/s). In contrast, both sigma-delta and SA are suitable for biomedical sensor application because a biomedical sensor interface usually does not require high sampling rate. Although sigma-delta provides higher resolution (10-18 bits), it also dissipates more power and it is less energy efficient as compared to SA with a typical resolution of 8-12 bits.

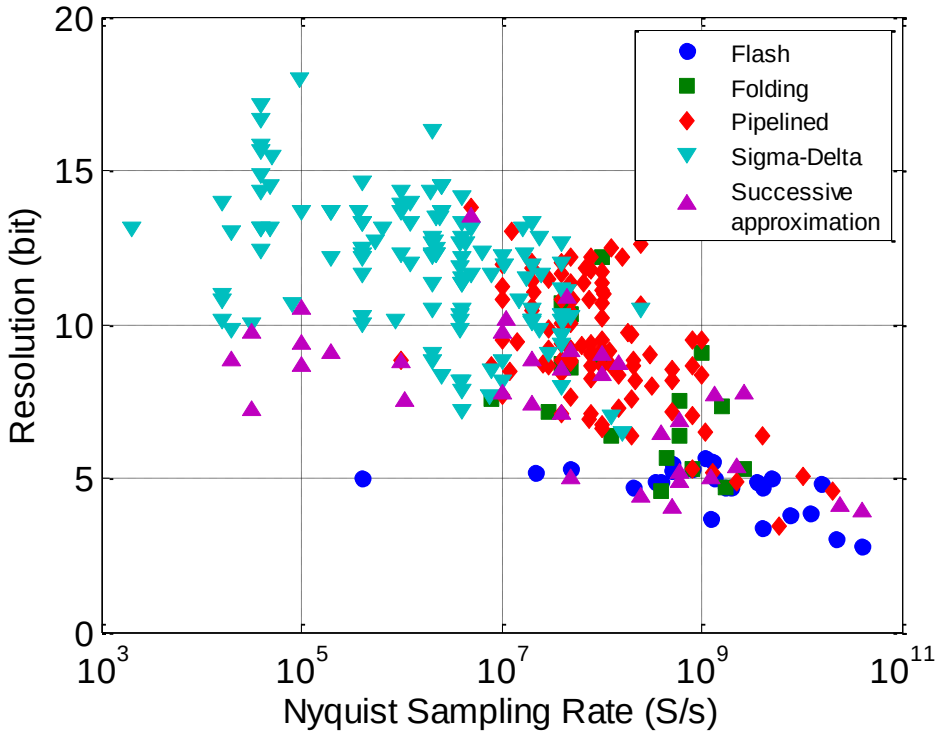

Fig. 2.1. Resolution versus Nyquist sampling rate for state-of-the-art ADC.

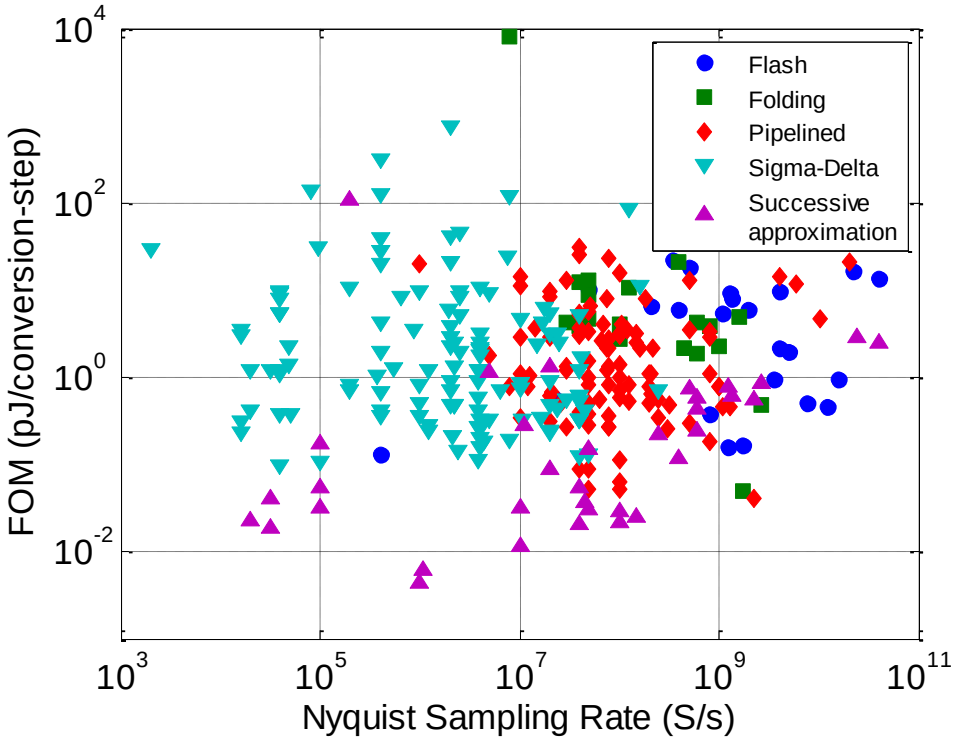

Fig. 2.2. FOM versus Nyquist sampling rate for state-of-the-art ADC.

Fig. 2.2 compares the energy efficiency of different ADC architectures using FOM. As shown in Fig. 2.2, SA in general achieves better FOM than all other architectures and thus it is the most energy-efficient ADC architecture. In fact, the FOM achieved by SA ADC in the publications are well below 100 fJ/conversion-step for low sampling rate (<10 MS/s) designs.

Therefore, it is clear that SA architecture is the most suitable candidate for implementing the ADC in a low-power wireless biomedical sensor interface due to its excellent energy efficient and moderate resolution and low sampling rate. Consequently, my research work will focus on the ADC design based on SA architecture.

2.2 Successive Approximation ADC

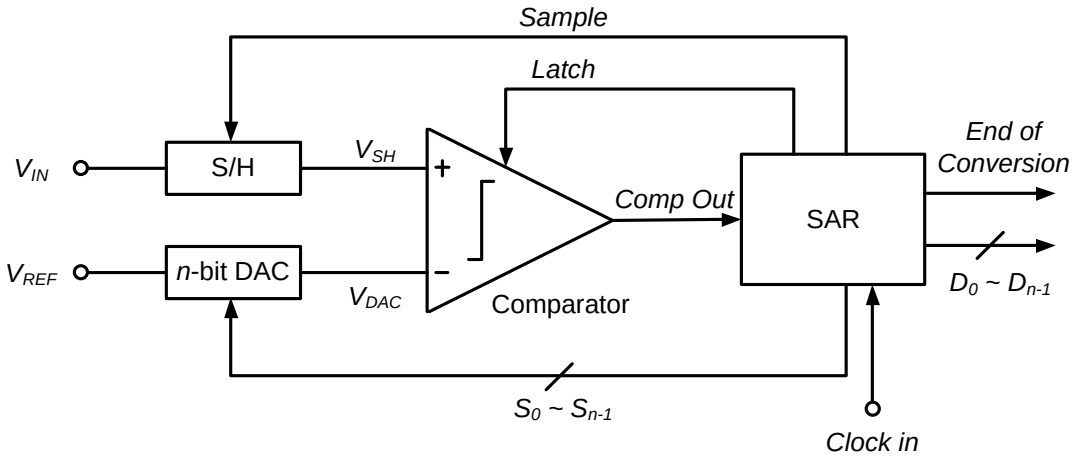

Fig. 2.3. Block diagram of a typical SA ADC.

A SA ADC performs binary search through possible quantization levels before converging to the final digital answer [30]. It demands only relatively simpler

circuitry as compared to other architectures. As shown in Fig. 2.3, a typical *n*-bit SA ADC has a successive approximation register (SAR), a comparator, a sample-and-hold (S/H), and an *n*-bit digital-to-analog converter (DAC).

The SAR generally consists of sequencer and code register [31]. It is purely digital and made of flip-flops and combinational circuits. The sequencer controls the timing of the conversion, while a code register stores and generates the conversion result.

A SA ADC requires only one comparator. The fundamental role of this comparator is to amplify the analog difference between its inputs and convert it into digital signal. Since SA ADC relies on the comparator decision to perform binary search, comparison accuracy and speed are the main design specifications for comparator.

The DAC is the most crucial building block of a SA ADC. An *n*-bit SA ADC always requires an *n*-bit DAC array to cater for all of the quantization levels. The DAC linearity and accuracy directly determine the overall ADC resolution because binary search is based on the comparison between the sampled input and DAC output. There are different approaches in implementing the DAC, e.g. current steering, resistor ladder, capacitive array, etc. Among all these approaches, capacitive array is preferred because its charge redistributive operation leads to lower power dissipation as compared to other approaches. Furthermore, capacitor matching in currently available CMOS process, which directly affects the DAC linearity, is more than adequate to realize a medium resolution ADC design.

Fig. 2.4 illustrates the SA ADC operation. At the beginning of the conversion, input signal, V_{IN}, is first sampled onto the S/H. Then, it is compared to the output of the DAC, V_{DAC}. The comparator result not only decides the direction of the binary search

but it is also the digital code corresponding to the analog input. The AD conversion is performed from most significant bit (MSB) down to least significant bit (LSB) through successive addition and subtraction on DAC value. Owing to the nature of binary search, a typical *n*-bit SA ADC requires at least *n* clock cycles to complete the entire AD conversion.

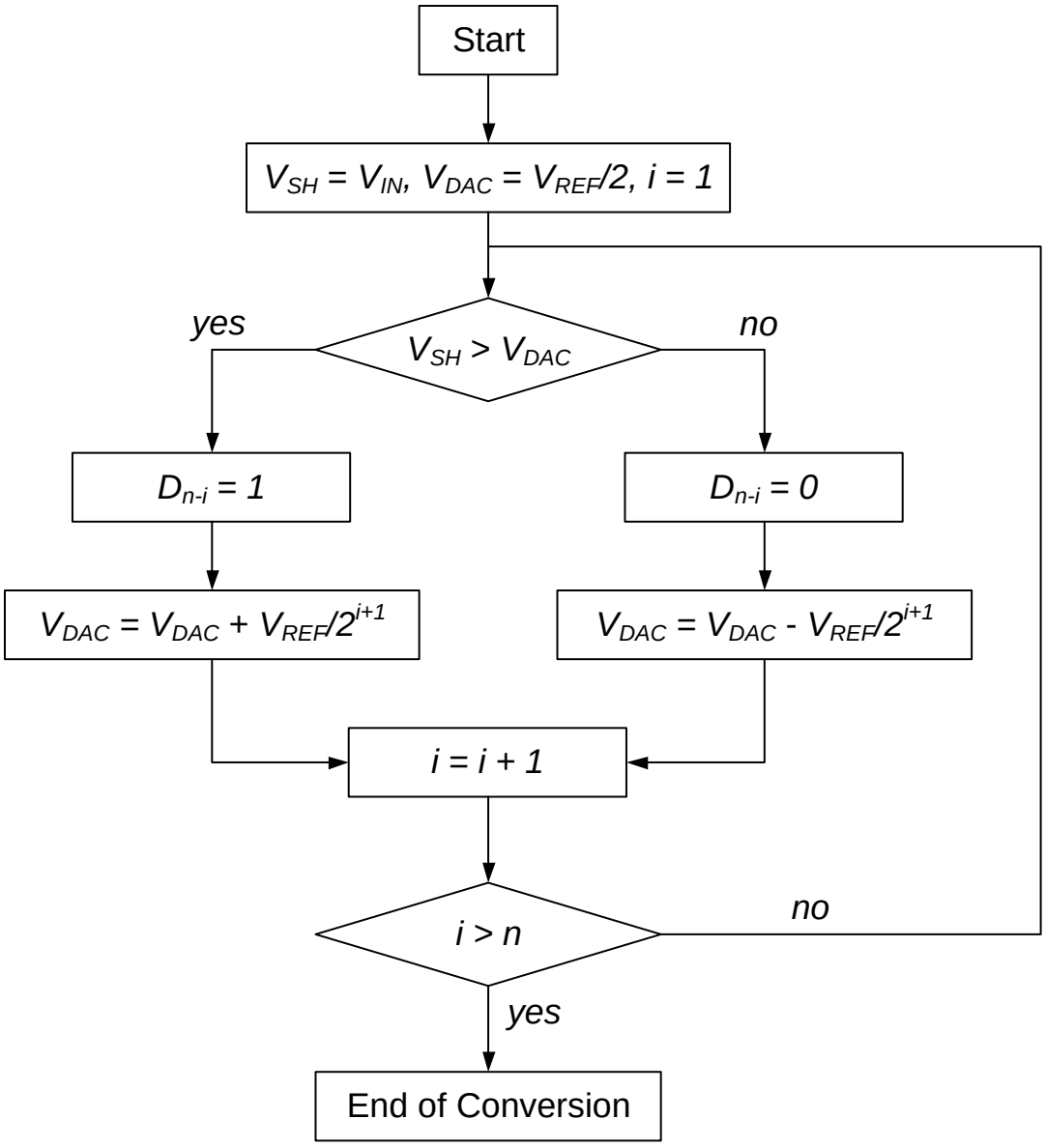

Fig. 2.4. Flowchart for the ADC operation.

2.3 Conventional SA ADC with Capacitive DAC

This section discusses the conventional works on SA ADC design based on capacitive DAC array. Three general structures will be investigated in order to better understand the differences as well as the advantages and disadvantages among these structures.

2.3.1 Single-Ended Structure (sampling using DAC array)

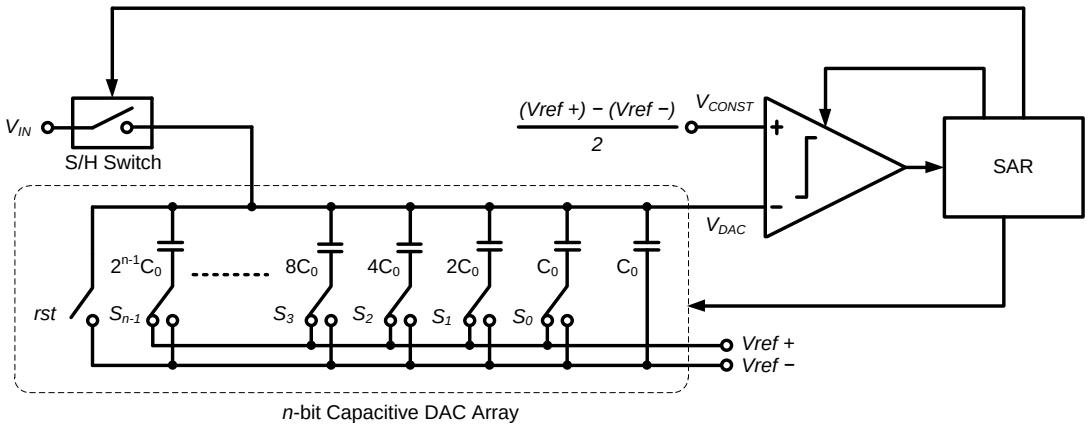

Fig. 2.5. Implementation example based on [32].

SA ADC with capacitive DAC array was first introduced in [32]. Fig. 2.5 illustrates an *n*-bit SA ADC implementation based on this classical structure. It uses a binary-weighted capacitor array to form the DAC. In this design, input signal is sampled using the capacitive DAC array while AD conversion is performed by comparing the DAC output, V_{DAC}, to a constant reference voltage, V_{CONST}, which is set at half of ADC full scale (FS). The size of DAC array is exponentially proportional to the ADC resolution. Its total capacitance is given by

$$C_{total,DAC} = 2^n \cdot C_0 \tag{2.1}$$

where C_0 is the unit capacitor. With a C_0 value of 50 fF, the total capacitance of a 10-bit DAC array can be as large as 51.2 pF. As a result, sampling using the DAC array requires a large buffer at the ADC input in order to address the driving issue and to minimize the sampling error.

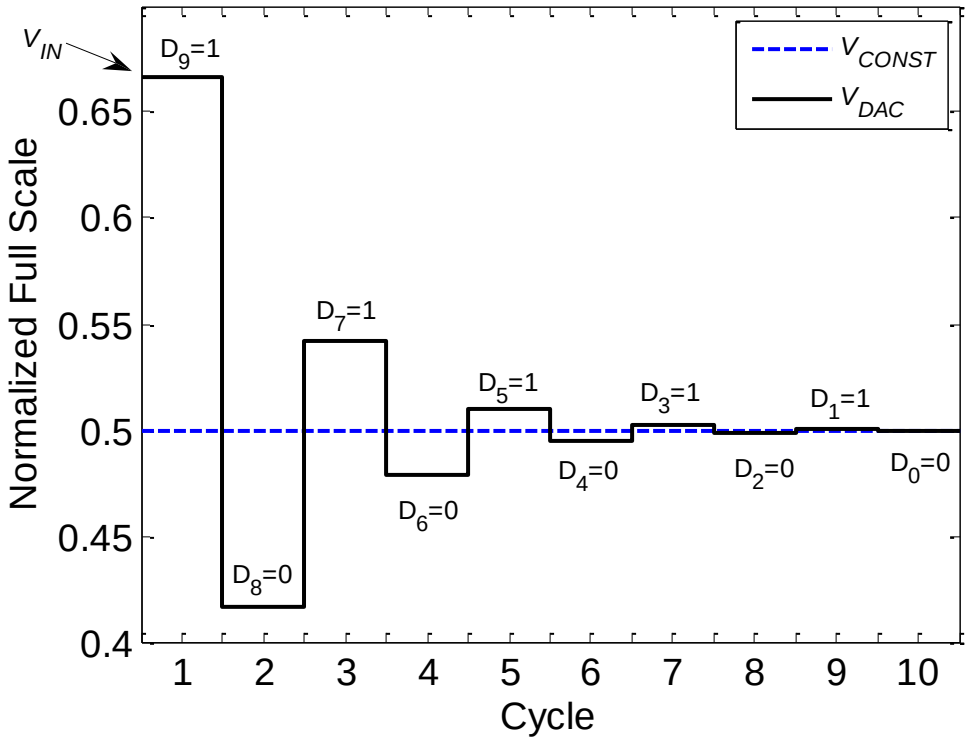

Fig. 2.6. Conversion example for ADC using DAC array for sampling.

Fig. 2.6 shows a 10-bit conversion example for ADC using DAC array for sampling. Signals at the comparator inputs are plotted. In this example, V_{IN} is two third of FS which corresponds to a digital output of 1010101010. The digital code is generated based on comparator output, from MSB to LSB. Successive subtraction and addition are made onto the sampled signal through charge redistribution and V_{DAC} eventually

converges to the V_{CONST} at the end of AD conversion. This means that the common-mode voltage of comparator input, V_{CM}, is constant, i.e.

$$V_{CM,Comparator} = V_{CONST}. \tag{2.2}$$

Consequently, this architecture does not require a rail-to-rail comparator to achieve a rail-to-rail ADC FS input range.

2.3.2 Single-Ended Structure (sampling using dedicated C_S)

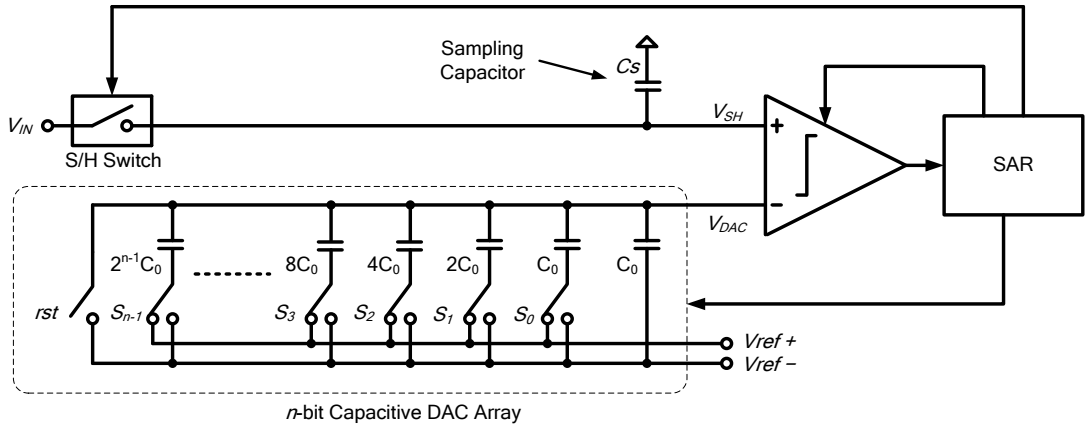

Fig. 2.7. ADC with dedicated sampling capacitor based on [33].

On the other hand, [33] presented an alternative implementation for the SA ADC. As shown in Fig. 2.7, the ADC still has an *n*-bit binary-weighted capacitor array to for AD conversion but it incorporates a dedicated sampling capacitor, C_S, for signal sampling. The size of C_S is typically chosen to be a few pF after considering the *kT/C* noise and compensation requirement. As compared to previous design which performs sampling using the DAC array, this structure does not require a large

preceding buffer because C_S is now significantly smaller than the total capacitance of the DAC array.

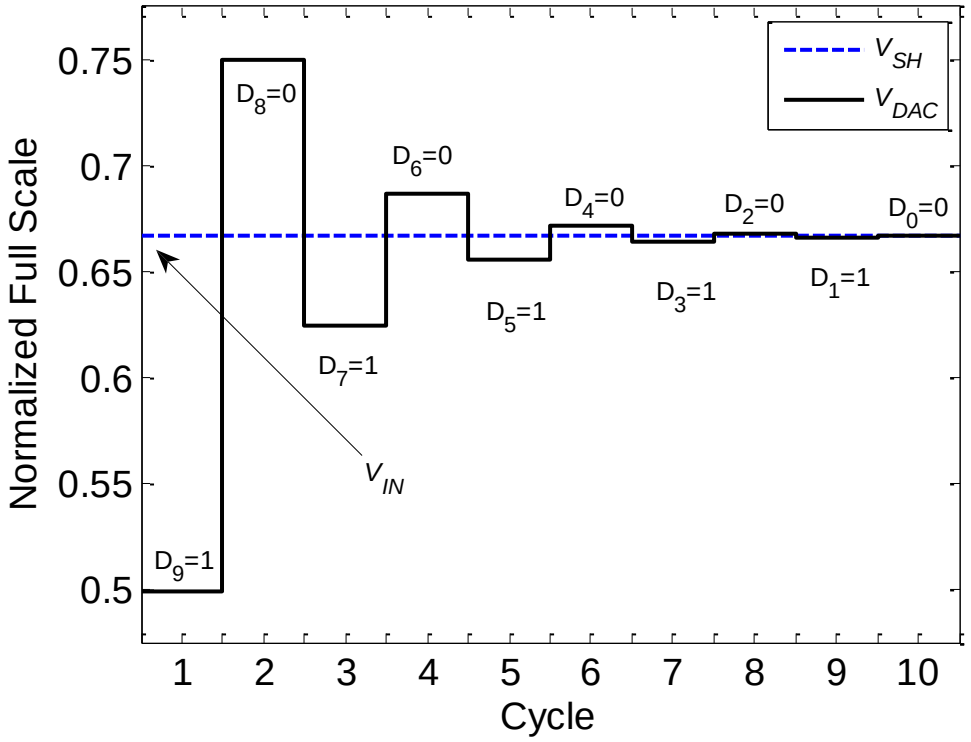

Fig. 2.8. Conversion example on ADC using dedicated C_S for sampling.

Fig. 2.8 shows a 10-bit conversion example for ADC using dedicated C_S for sampling. Signals at the comparator inputs are plotted, namely S/H output, V_{SH}, and DAC output, V_{DAC}. Same as the previous example, V_{IN} is two third of FS which corresponds to a digital output of 1010101010. However, the digital code is now produced by comparing V_{SH} to V_{DAC} based on successive approximation. As a result, V_{DAC} always converges to V_{SH} (which is the sampled V_{IN}) at the end of AD conversion and the comparator input common-mode can be proved to be

$$V_{CM,comparator} = V_{SH} = V_{IN} . \tag{2.3}$$

From Eq. (2.3), we know that the comparator common-mode is dependent on ADC input FS. Therefore, SA ADC using dedicated C_S for sampling requires a rail-to-rail comparator in order to realize a rail-to-rail ADC, as discussed in [34].

2.3.3 Fully-Differential Structure

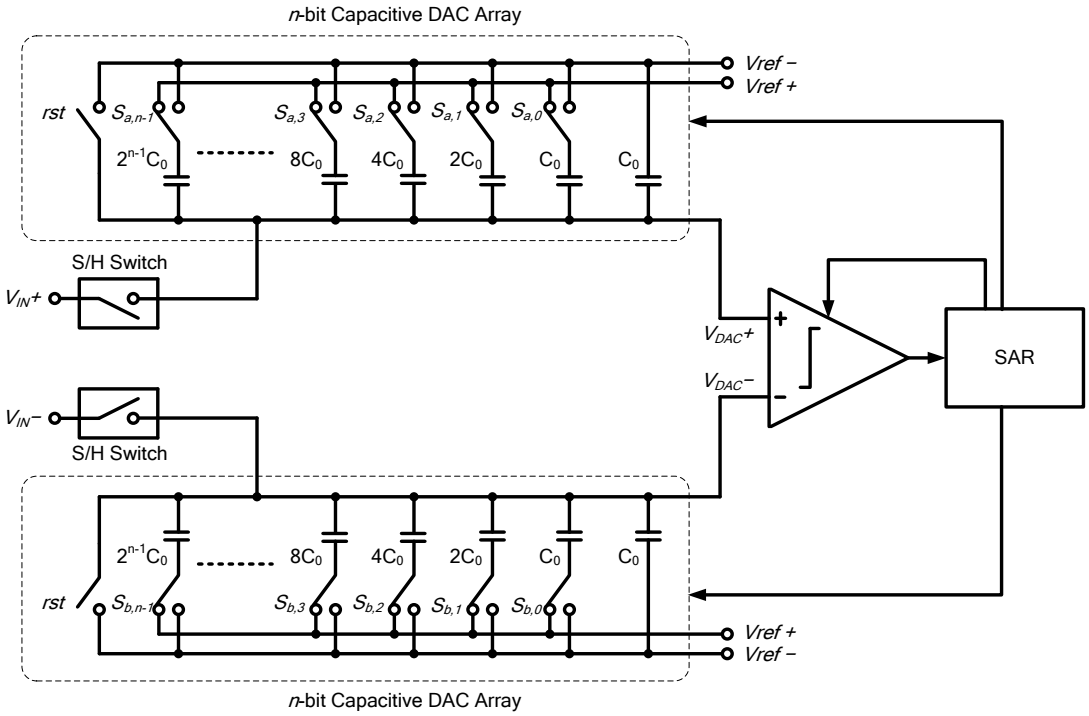

Fig. 2.9. Fully-differential structure based on [35].

In contrast to single-ended structure, there is also fully-differential structure. For instance, [35] presented a fully-differential SA ADC. Fig. 2.9 shows an example based on the presented design. This fully differential structure provides improved common-mode noise performance and it can achieve maximum input range that is two times larger as compared to single-ended structure. However, it demands twice of the area to implement the complimentary DAC array and sampling switch.

Furthermore, its power dissipation is also doubled due the duplicated DAC array and switches. Besides of that, this fully differential structure also demands two large driving buffers since it uses the differential DAC arrays for signal sampling.

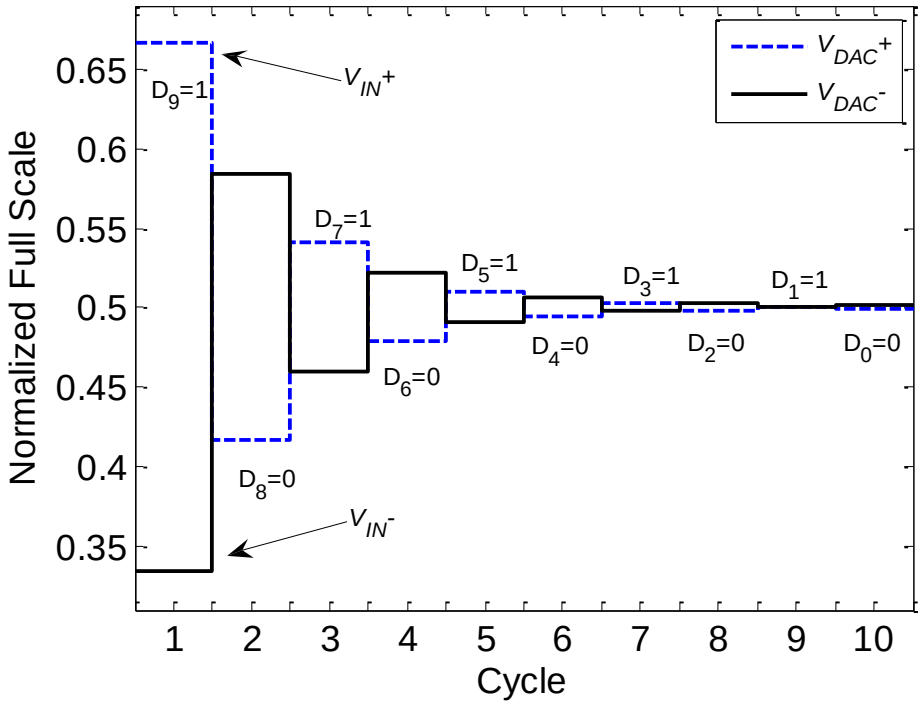

Fig. 2.10. Conversion example on fully-differential ADC.

Fig. 2.10 shows a 10-bit conversion example for the fully differential SA ADC. Differential signals at the comparator inputs, $V_{DAC}+$ and $V_{DAC}-$, are plotted. This example illustrates the AD conversion with differential input at two third of FS and one third of FS, which gives an output code of 1010101010. As shown in Fig. 2.10, both $V_{DAC}+$ and $V_{DAC}-$ converge to the predefined input common-mode, which is typically set at half of FS for a maximum signal swing. Thus, the comparator common-mode is given as

$$V_{CM,comparator} = V_{CM,input} = \frac{1}{2} FS \,. \tag{2.4}$$

From Eq. (2.4), this fully differential structure has a predefined constant common-mode and it does not require a rail-to-rail comparator.

2.3.4 Summary on Conventional Structures

Table 2.1 Advantages and disadvantages of conventional SA ADC structures.

ADC Structure	Advantages	Disadvantages
Single-Ended (Sampling using DAC array)	✓ Does not require rail-to-rail comparator	× Large driving buffer
Single-Ended (sampling using dedicated C_S)	✓ Small driving buffer	× Rail-to-rail comparator
Fully-Differential	✓ Does not require rail-to-rail comparator ✓ Improved CMRR ✓ 2 × input range	× Large driving buffers × Double area and power

Table 2.1 lists and compares the conventional SA ADC structures. In summary, sampling using DAC array does not need a rail-to-rail comparator to achieve rail-to-rail FS range but always requires large driving buffer to address the sampling error. On the other hand, sampling using dedicated C_S requires only a small driving buffer but it needs a rail-to-rail comparator to achieve rail-to-rail FS range. Lastly, fully-differential design provides improved CMRR and twice of input range but at a price of double area and power dissipation as compared to single-ended designs.

2.4 Techniques to Improve Energy Efficiency

We need to first investigate the power profile of a SA ADC based on capacitive array in order to reduce the power dissipation and improve its energy efficiency through optimization and circuit design technique. In general, the power dissipation is mainly attributed to three blocks, i.e. SAR, comparator, and capacitive array.

Among the blocks, SAR is purely-digital and consumes only dynamic, leakage, and short-circuits power. It can be easily optimized using electronic design automation (EDA) tools like SYNOPSYS Design Compiler and Power Compiler.

On the other hand, comparator is conventionally formed by analog pre-amplifier and clocked decision circuit with positive feedback (or a latch) [27, 36]. In order to eliminate the DC current consumption by analog pre-amplifier, clocked or dynamic comparator is more commonly used in low-power design for sensor application [37-39].

Lastly, switching power dissipated by capacitive array is usually dominant in a SA ADC design. Therefore, reducing the switching power in capacitive array has been a main focus in improving the SA ADC efficiency. It is well-known that the switching power in capacitive array is dynamic and is proportional to the sampling rate, f_S, unit capacitor, C_0, and ADC reference voltage (*VDD* for a rail-to-rail ADC). It can be written as

$$P_{switching} = a \cdot f_S \cdot C_0 \cdot VDD^2 \tag{2.5}$$

where *a* is a variable dependent on the capacitive array design and switching activities.

From Eq. (2.5), the value for f_S is defined by the sensor application, while *VDD* can be chosen so that the circuit is operating in sub-threshold region which yields highest g_m/I_d ratio and thus optimal power-delay product [9]. Ideally, it is preferred to have a very small C_0 to minimize the switching power. However, this is either limited by the process matching or the compensation requirement. In the later case, C_0 has to be large enough to compensate for the non-linear parasitic capacitance associated with the comparator input and the S/H switch. As presented in [39], a C_0 as small as about 0.5 fF could be used to achieve significantly low power dissipation and excellent FOM but it is extremely sensitive to non-linearity caused by parasitic. Consequently, various DAC array structures have been proposed to alter the variable*a* in Eq. (2.5).

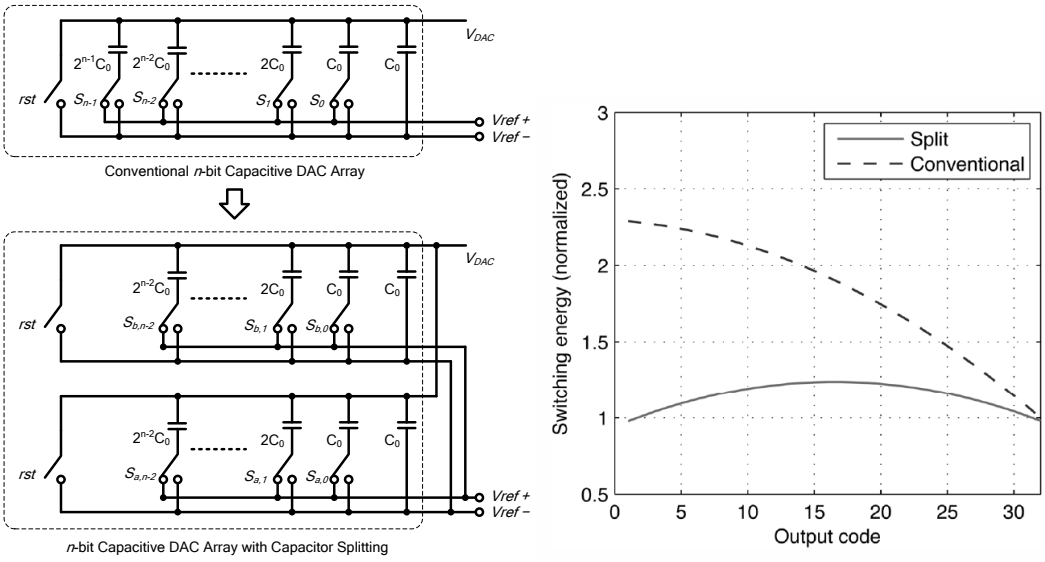

Fig. 2.11. Capacitor splitting and switching energy [40, 41].

[40, 41] propose capacitor splitting technique which splits the MSB capacitor into smaller sub-arrays as shown in Fig. 2.11. Instead of switching the entire MSB capacitor, only a smaller portion of the sub-array is switched during conversion. Consequently, this technique avoids throwing away charges in capacitive array during AD conversion. This technique is expected to have 37% lower switching power as

compared to conventional capacitive array. But the drawback of this technique is more complicated switching network for the DAC array.

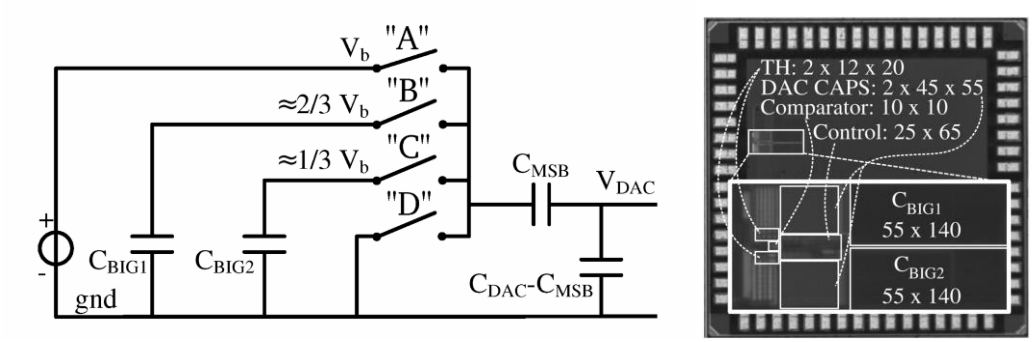

Fig. 2.12. Step-wise charging technique and the die photo of chip prototype [39].

In addition, [39] proposes the use of step-wise charging technique to increase the ADC efficiency. As shown in Fig. 2.12, step-wise charging technique introduces additional capacitors (C_{BIG1} and C_{BIG2}) onto the conventional DAC array to store and reuse the charge throughout the conversion. However, the trade-off of this technique is that the additional charge-recycling capacitors have to be at least a few times larger than the entire DAC array in order to effectively recycle the charges. This means a huge increment in core area, as shown in the die photo (see Fig. 2.12).

Besides of new DAC array structures, it is also possible to reduce the power by minimizing the switching activities in DAC array. This can be done through the use of adaptive AD conversion [42]. Considering a typical biomedical signal, such as ECG, most of its main components are located at very low frequencies while leaving few components with small amplitude at higher frequencies. This slow-varying characteristic is very common among biomedical signals. As a result, the difference between two consecutive sampled inputs is limited to a small range as compared to the ADC FS. Therefore, it is possible start the AD conversion from last sample value

and to perform successive approximation for the LSB portion only. This technique effectively reduces the switching activities in DAC array and thus reduces its power dissipation. However, this technique requires signal-specific customization and it may not be suitable for general purpose biomedical application.

To conclude, all of the above-mentioned techniques help to reduce the ADC power dissipation and to achieve better efficiency. However, none of them address the driving buffer and/or rail-to-rail comparator issue. This calls for the research of an alternate SA ADC architecture.

CHAPTER 3

DUAL-CAPACITIVE-ARRAY SA ADC

3.1 Overview

In this chapter, a dual-capacitive-array architecture and the design of a 0.8-V 10-kS/s 10-bit SA ADC with a 32-fJ/conversion-step figure of merit (FOM) are presented. This ADC design aims for the use in low-cost biomedical sensor interface, especially ECG and EEG with signal bandwidth less than 150 Hz.

3.2 Dual-Capacitive-Array Architecture

Knowing that dynamic power dissipation is dominant in a capacitive SA ADC, reducing supply voltage is very effective in reducing the power dissipation. However, low supply voltage will limit the maximum ADC input dynamic range. Although a fully-differential structure provides larger input swing and improved common-mode rejection ratio (CMRR), it is less favorable in a low-power moderate-resolution ADC design as compared to single-ended structure due to its power- and area- demanding nature. In fact, a fully differential structure requires at least twice the power and area, as discussed in Section 2.3. Therefore, the use of rail-to-rail single-ended SA ADC is adopted in my work. Rail-to-rail input range not only improves the ADC input dynamic range but also boosts the peak signal-to-noise-and-distortion ratio (SNDR). In addition, a rail-to-rail SA ADC utilizes only one single supply voltage, i.e. *VDD*,

and does not require additional reference voltage generator. This simplifies the system integration of a sensor interface.

Rail-to-rail input range can be achieved by either performing signal sampling using the capacitive DAC array [32] or incorporating a dedicated sampling capacitor together with a rail-to-rail input common-mode comparator [34]. On one hand, sampling using the huge DAC array limits the input bandwidth and requires a large driving buffer because the size of the DAC array is exponentially proportional to the ADC resolution. Although the driving buffer is not part of the ADC and a power-consuming buffer never affects the ADC individual FOM, it is most undesirable from a sensor-system perspective. On the other hand, designing a rail-to-rail comparator is never a trivial task especially under low supply voltage. Furthermore, the offset of a rail-to-rail comparator is dependent on input common-mode and a rail-to-rail variation in input common-mode will result in undesirable signal distortion.

Therefore, a dual-capacitive-array structure is proposed, as shown in Fig. 3.1. Instead of having only the *n*-bit DAC array as in the conventional designs, an additional but smaller *k*-bit S/H array is introduced for both signal sampling and quantization, in which $0 < k < n$. The AD conversion of the proposed structure resembles the conventional SA ADC operation, except that the successive approximation is now performed on two arrays. Considering the proposed architecture in Fig. 3.1, the ADC without the DAC array is actually a coarse ADC analogous to the single-ended design using capacitive array for signal sampling in [32] while the ADC without the S/H array is in fact a fine ADC analogous to the design using dedicated C_S for signal sampling in [34]. Therefore, the dual-capacitive-array structure can be seen as a hybrid between the two conventional single-ended designs.

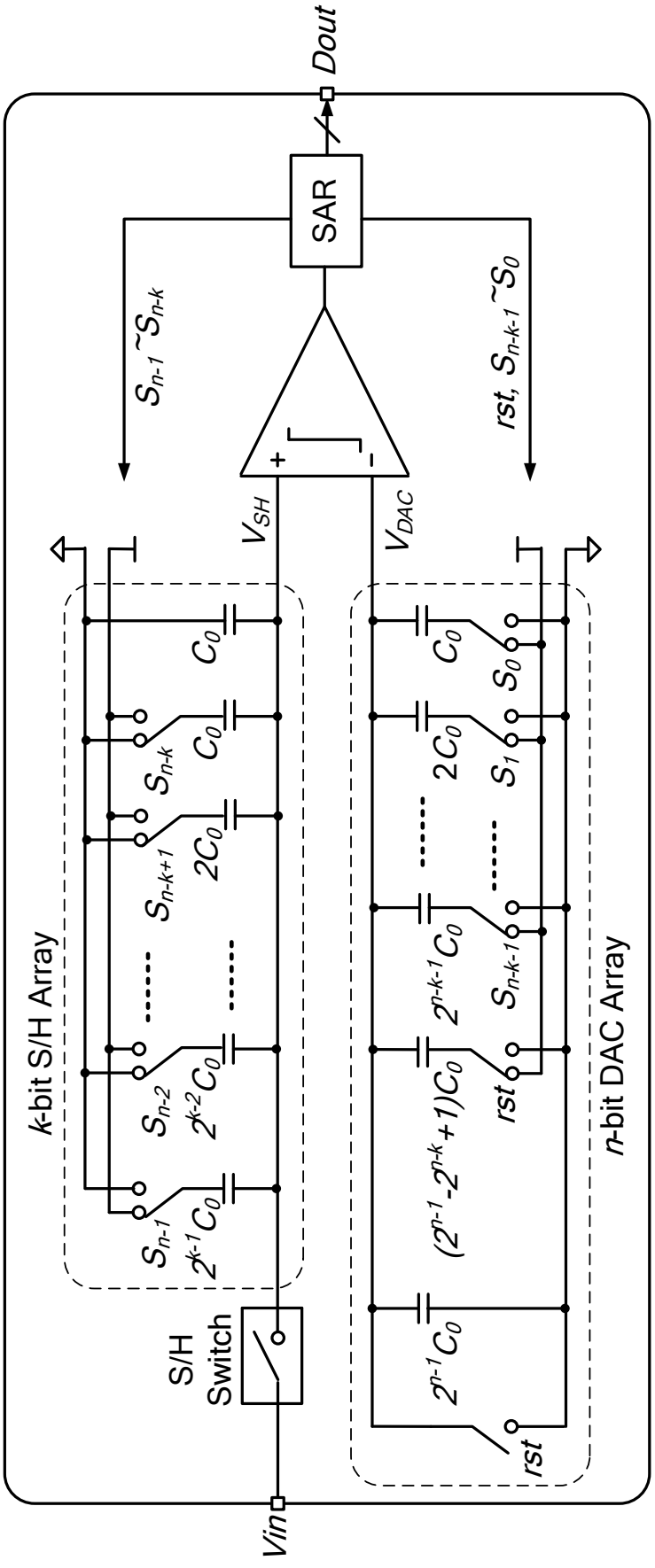

Fig. 3.1. Schematic of the proposed dual-capacitive-array SA ADC.

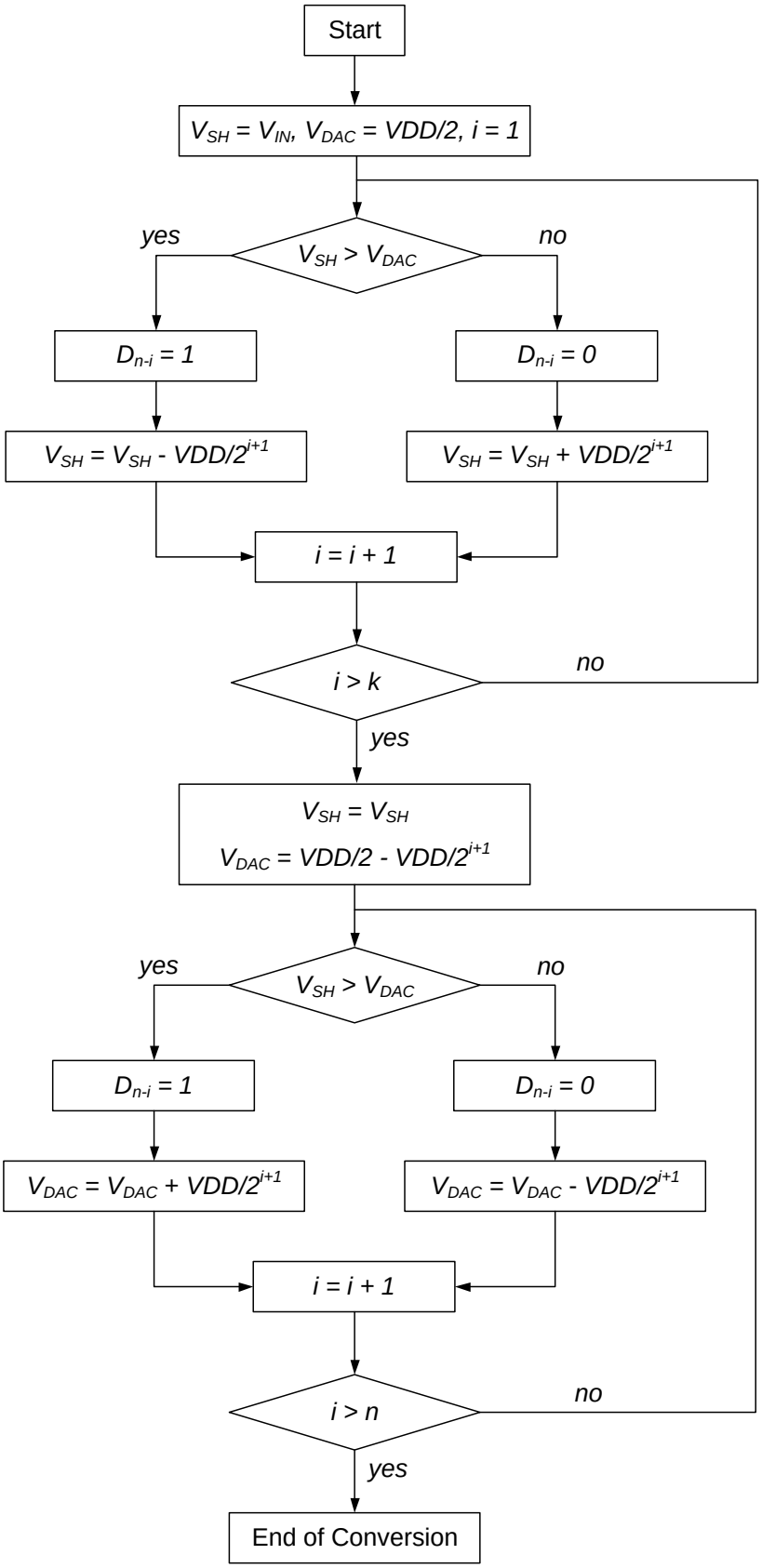

Fig. 3.2. Flowchart of the proposed dual-capacitive-array SA ADC.

Fig. 3.2 illustrates the operation of the proposed ADC. At the beginning of the conversion, input signal, V_{IN}, is first sampled onto the S/H array. Then, it is compared to the output of the DAC array, V_{DAC}. The AD conversion is performed from most significant bit (MSB) down to least significant bit (LSB). The comparator result decides the direction of the binary search and also provides the digital code corresponding to the analog input. For the first *k* bits, successive approximation is performed using S/H array and V_{DAC} is set at half of ADC full scale (FS). A comparator output of '1' results in subtraction on sampled input while a '0' results in addition. For the remaining *n*-*k* bits, S/H array will be hold at its last value and successive approximation is continued using DAC array. In contrast to the previous case, a '1' now results in addition on DAC output while a '0' results in subtraction. Same as the conventional counterpart, the proposed *n*-bit ADC requires at least *n* clock cycles to complete the entire AD conversion.

In the following sections, the detailed operation and circuit implementation of the proposed architecture will be explained through the design of a 10-bit SA ADC.

3.2.1 S/H Array Sizing

The additional S/H array is binary-weighted and can be of any size from 1 bit to *n*-1 bits for an *n*-bit SA ADC design while the trade-off is additional area to build the S/H array. Therefore, we need to consider the resulting switching energy and required area versus S/H array sizing in order to select the optimal solution. Switching energies for various S/H array sizing are obtained through circuit simulation. On the other hand,

the required area in term of unit capacitor, C_0, is simply 2^k since the array size is exponentially proportional to the number of bits.

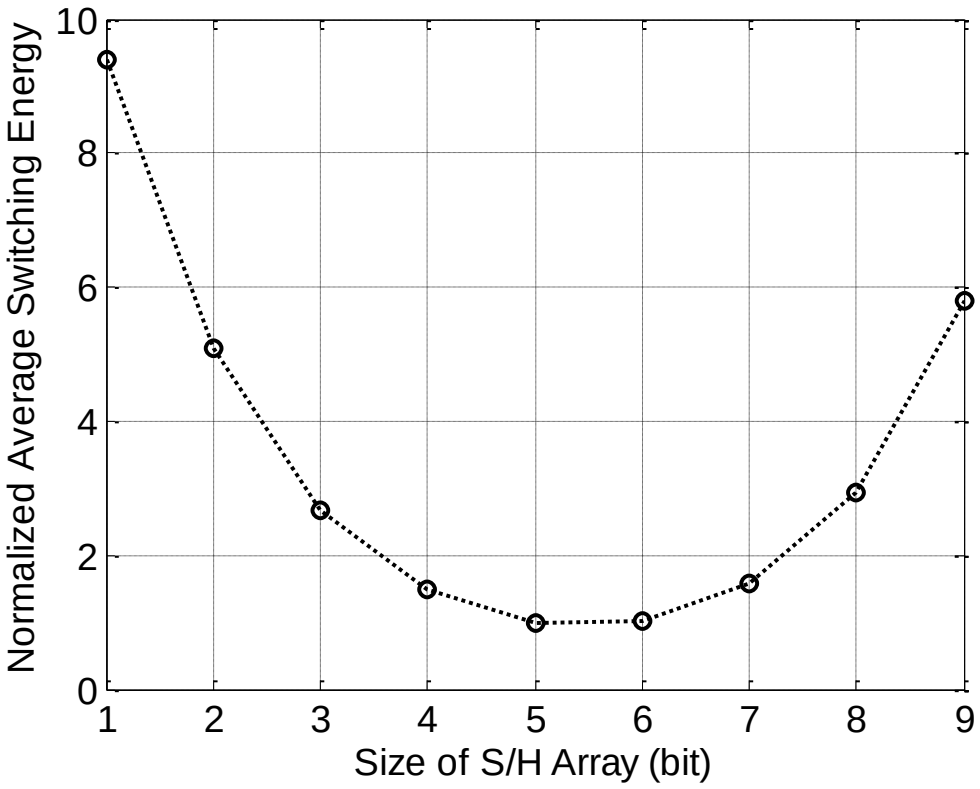

Fig. 3.3. Normalized average switching energy in capacitive arrays versus size of S/H array.

In the case of a 10-bit design, the normalized average switching energy in capacitive arrays for different S/H array sizing is as depicted in Fig. 3.3. Fig. 3.3 reveals that both 5-bit and 6-bit S/H array can be used on the top of the 10-bit DAC array in order to achieve the lowest switching energy. However, with unit capacitor of same size, a 6-bit array requires twice the area as compared to a 5-bit array. Therefore, a 5-bit additional S/H array is chosen. As a rule of thumb, it is suggested to use a *k*-bit S/H array (where $k = n/2$) for an *n*-bit ADC design with the trade-off in additional area of $2^{-(n-k)}$ times of that for an *n*-bit DAC array.

3.2.2 Dual-Capacitive-Array SA ADC

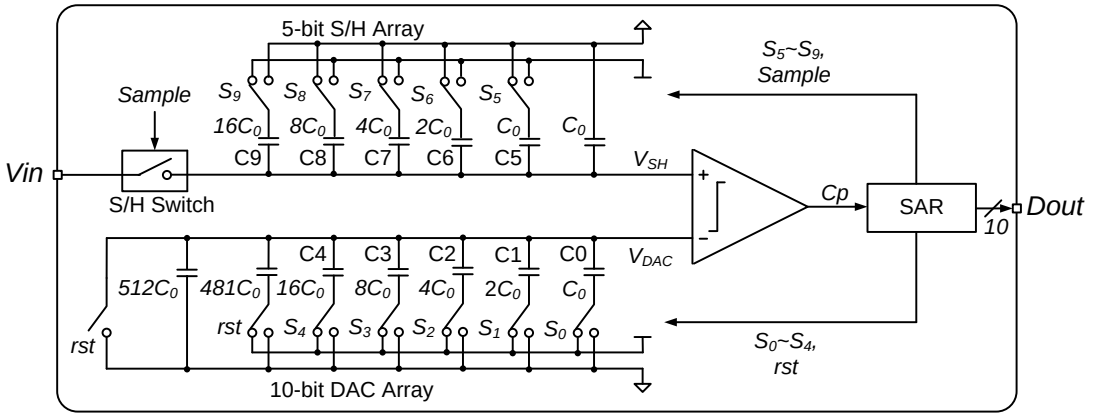

Fig. 3.4. Schematic of the 10-bit SA ADC based on dual-capacitive-array.

Fig. 3.4 illustrates the schematic of a 10-bit ADC design. A 5-bit additional S/H array is used in this design. Both of the capacitive arrays are binary-weighted and connected to the comparator. SAR latches the comparison result, *Cp*, to form the digital output and generates the control signals for both arrays. The switching of DAC array and S/H array are based on S_0 to S_4 and S_5 to S_9, respectively.

The detailed state transition for the ADC is shown in Table 3.1. The AD conversion of the proposed architecture resembles those in conventional SA ADC operation, except that the successive approximation is performed on both S/H array and DAC array.

AD conversion always starts from Cycle 0 in which signal is being sampled onto the S/H array while DAC array is purged of residue value by shorting both of the top and bottom plates to *GND*. Throughout sampling period, C9 on S/H array is switched to *VDD* through control signal S_9 and sampling is performed using top plate. As compared to bottom-plate sampling, this technique demands only one sampling

Table 3.1 State transition for analog-to-digital conversion.

Cycle	State	*Dout*	Switching on Capacitive Array										
			S/H Array					DAC Array					
			S_9	S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	*rst*
0	Sampling with Purging of DAC	-	0	1	1	1	1	1	1	1	1	1	1
	Sampling without Purging of DAC	-	0	1	1	1	1	0	0	0	0	0	0
1	Successive Approximation	$D_9=Cp_9$	Cp_9	0	1	1	1	0	0	0	0	0	0
2		$D_8=Cp_8$	Cp_9	Cp_8	0	1	1	0	0	0	0	0	0
3		$D_7=Cp_7$	Cp_9	Cp_8	Cp_7	0	1	0	0	0	0	0	0
4		$D_6=Cp_6$	Cp_9	Cp_8	Cp_7	Cp_6	0	0	0	0	0	0	0
5		$D_5=Cp_5$	Cp_9	Cp_8	Cp_7	Cp_6	Cp_5	1	0	0	0	0	0
6		$D_4=Cp_4$	Cp_9	Cp_8	Cp_7	Cp_6	Cp_5	$\overline{Cp_4}$	1	0	0	0	0
7		$D_3=Cp_3$	Cp_9	Cp_8	Cp_7	Cp_6	Cp_5	$\overline{Cp_4}$	$\overline{Cp_3}$	1	0	0	0
8		$D_2=Cp_2$	Cp_9	Cp_8	Cp_7	Cp_6	Cp_5	$\overline{Cp_4}$	$\overline{Cp_3}$	$\overline{Cp_2}$	1	0	0
9		$D_1=Cp_1$	Cp_9	Cp_8	Cp_7	Cp_6	Cp_5	$\overline{Cp_4}$	$\overline{Cp_3}$	$\overline{Cp_2}$	$\overline{Cp_1}$	1	0
10		$D_0=Cp_0$	Cp_9	Cp_8	Cp_7	Cp_6	Cp_5	$\overline{Cp_4}$	$\overline{Cp_3}$	$\overline{Cp_2}$	$\overline{Cp_1}$	$\overline{Cp_0}$	0

Note: $Cp_{0:9}$ are the comparator output.

switch and thus reduces the complexity in circuit implementation.

During successive approximation, bit-cycling is performed on the capacitive arrays, from MSB to LSB, in order to form *Dout*. Successive addition and subtraction on both arrays are performed through charge redistribution. Nonetheless, it is important to note that the control signals for S/H array (S_5 to S_9) and DAC array (S_0 to S_4) are complimentary. This is because the two arrays are connected to the complimentary comparator input and thus an addition on S/H array is equivalent to subtraction on DAC array and vice versa.

At the end of conversion, all C0 to C9 are switched back to their default position and the ADC operation restart at Cycle 0.

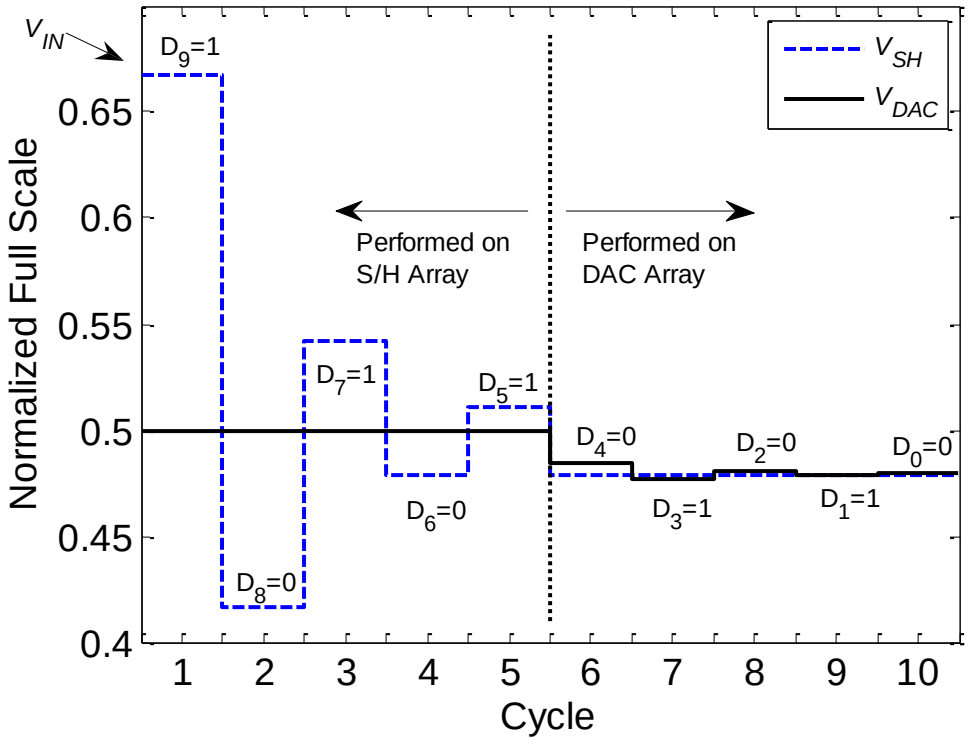

Fig. 3.5. Example on AD conversion.

Fig. 3.5 illustrates an example on signal conversion using dual-capacitive-array structure. The capacitive array outputs, V_{SH} and V_{DAC}, are plotted. Comparison results for each cycle are also annotated. In this example, V_{IN} is two third of FS which corresponds to a digital output of 1010101010. With the proposed dual-capacitive-array, the successive approximation of first five bits are performed using C5 to C9 on the 5-bit S/H array while the remaining five bits using C0 to C4 on the 10-bit DAC array. For Cycle 1 to Cycle 5, V_{DAC} serves as reference at half of *VDD* and the sampled V_{IN} on S/H array converges toward V_{DAC} through successive subtraction or addition. After Cycle 5, V_{SH} is held constant and AD conversion continues using DAC array through Cycle 6 to Cycle 10.

From this example, we can deduce that the common-mode of V_{SH} and V_{DAC} is dependent on V_{IN} but it does not vary from rail-to-rail. Considering the state transition in Table 3.1 and the conversion example in Fig. 3.5, it can be proved that the V_{SH} at the end of conversion is given by

$$V_{SH} = V_{IN} - VDD\left(2^{-1} - 2^{-1}\cdot\overline{D_9} - 2^{-2}\cdot\overline{D_8} - 2^{-3}\cdot\overline{D_7} - 2^{-4}\cdot\overline{D_6} - 2^{-5}\cdot\overline{D_5}\right). \quad (3.1)$$

On the other hand, V_{DAC} is given by

$$V_{DAC} = VDD\left(2^{-1} - 2^{-6}\cdot\overline{D_4} - 2^{-7}\cdot\overline{D_3} - 2^{-8}\cdot\overline{D_2} - 2^{-9}\cdot\overline{D_1} - 2^{-10}\cdot\overline{D_0}\right). \quad (3.2)$$

Taking into account all possible values for V_{SH} and V_{DAC}, it can be shown that the comparator input common-mode, $V_{CM,\,comparator}$, always limited to

$$\frac{VDD}{2} - \frac{2^5\cdot VDD}{2^{10}} \le V_{CM,comparator} \le \frac{VDD}{2}. \quad (3.3)$$

By limiting the common-mode input range of comparator, the proposed dual-capacitive-array architecture can achieve rail-to-rail full scale range without the need of rail-to-rail comparator. Consequently, common-mode dependent offset associated with rail-to-rail comparator which will degrade the ADC resolution can be avoided as well.

3.2.3 Switching Energy in Capacitive Arrays

Conversion example in Fig. 3.5 also reveals that approximation steps with larger changes in voltage level are actually performed using smaller S/H array while approximation steps with lesser changes in voltage level, i.e. finer resolution, are resolved using larger DAC array. Knowing that the switching energy is proportional to total capacitance to be switched and changes in voltage level, switching energy required by each successive approximation step is now considerably smaller as compared to conventional design.

Furthermore, purging of DAC array after every conversion is not necessary. As a result, switching of the S/H array and DAC array back to their default positions after each conversion involve only relatively smaller capacitors, i.e. C5 to C9 on S/H array and C0 to C4 on DAC array (see Fig. 3.4). Comparing to the case in conventional single DAC array structure, in which the whole DAC array has to be reset after each conversion, the dual-capacitive-array structure effectively achieves higher energy efficiency by retaining most of the charge stored in DAC array after each conversion. Moreover, power saving is also achieved in array switches, switch drivers, and bootom-plate parasitic capacitance for not switching a larger part of the DAC array.

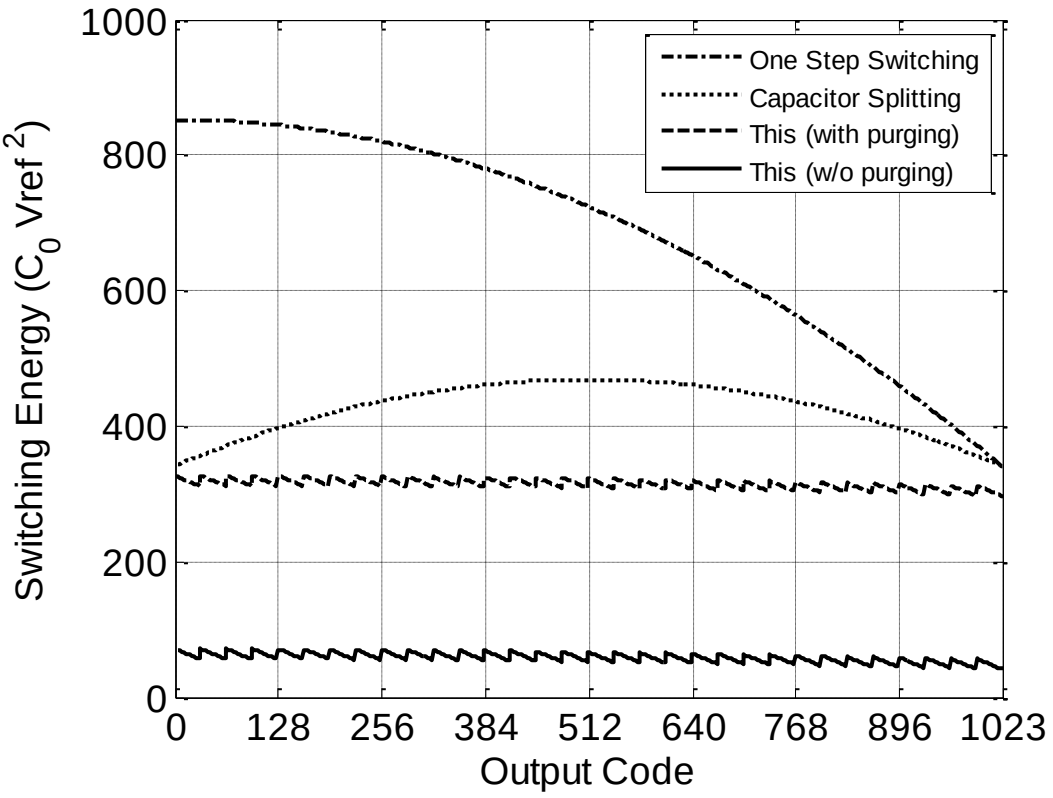

Fig. 3.6. Normalized switching energy for different architectures.

The simulated switching energies in capacitive array with respect to the ADC output code are shown in Fig. 3.6. Energy consumed by bottom-plate parasitic, switches, and drivers are not included for simplification. Nevertheless, the proposed dual-capacitive-array structure consumes significantly less switching energy and it is less dependent on ADC output code. Even if purging of DAC array is performed for each conversion, the proposed structure saves as much as 45% of switching energy as compared to conventional single DAC architecture using one step switching [32, 34] and about 24% as compared to capacitor splitting technique [40]. Moreover, a further saving of 38% can achieved because purging of DAC array after every conversion is not needed. Consequently, the maximum achievable saving is 83% in total.

3.3 Circuit Implementation

Since the target biomedical sensor application does not require high operating speed, a standard 0.35-μm CMOS technology is used to implement the proposed ADC.

3.3.1 Successive Approximation Register (SAR)

The SAR produces the control signals based on the successive approximation algorithm to control the S/H switch, S/H array, DAC array, and comparator. It is synchronized through a reference clock.

In the low-power sensor system design, the use of external clock with excessively high clock rate should be avoided. Therefore, the ADC clock rate, f_{CLK}, is chosen to be as slow as possible. With the use of successive approximation algorithm, at least 1 clock cycle is needed for sampling and each bit requires 1 clock cycle for AD conversion. Thus, the minimum clock rate, $f_{CLK,min}$, is given by

$$f_{CLK,\min} = (n+1) \cdot f_S \tag{3.4}$$

where n is the ADC resolution and f_S is the ADC sampling rate. Consequently, the proposed 10-bit design uses 11 clock cycles, in which 10 cycles are used for successive approximation while 1 cycle is used for signal sampling and data output.

The SAR is built using standard CMOS digital cells. It consists of simple combinational logics and flip-flops that serve as code register and bit-cycling

sequencer. It is generated and optimized for low power dissipation based on state transition given in Table 3.1 using EDA tool.

3.3.2 Sample-and-Hold (S/H) Switch

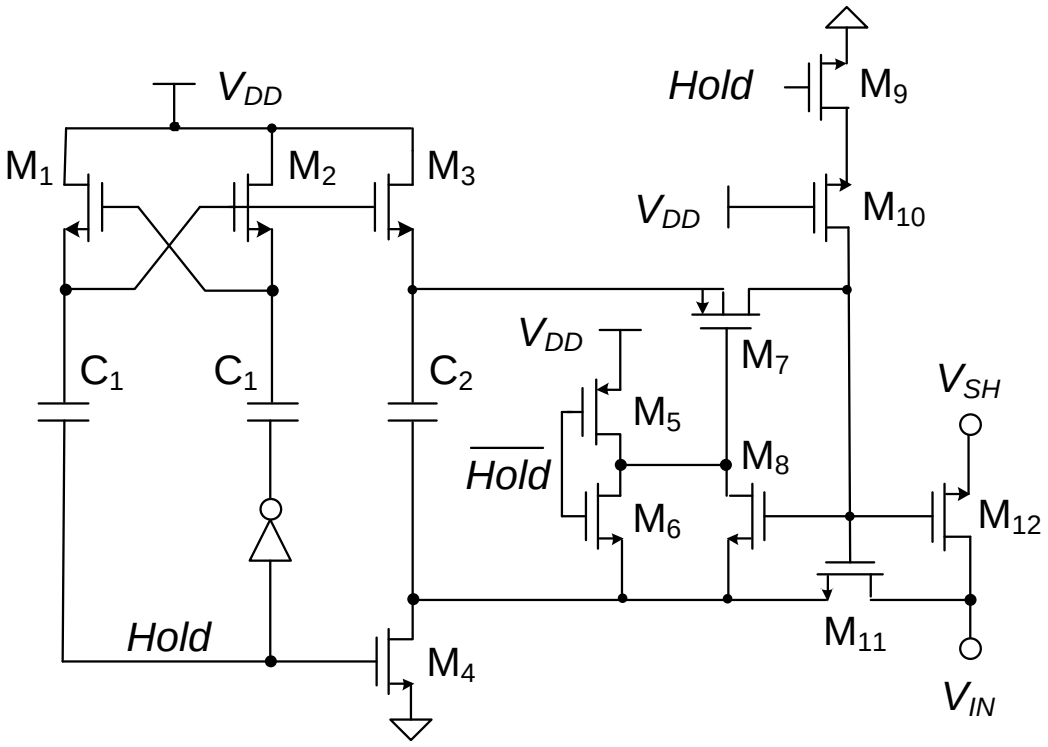

Fig. 3.7. Bootstrapped switch introduced by A. M. Abo [43].

The S/H switch is critical to the ADC. It must have rail-to-rail signal swing and low on-resistance, R_{ON}, so that the voltage drop across the switch during signal sampling does not affect the ADC resolution. However, conventional transmission gate is inadequate to realize a rail-to-rail swing under low voltage supply (sub-1 V) because the typical threshold voltages for NMOS and PMOS are 0.46 V and 0.68 V, respectively, in the target 0.35-μm technology. Furthermore, excessively large device

size will be needed to realize a low R_{ON} and results in large parasitic capacitance which can directly affect the charge redistribution in S/H array.

Therefore, the bootstrapped technique introduced in [43] is adopted. The schematic of the S/H switch is shown in Fig. 3.7. By using the bootstrapped technique, the gate-overdrive voltage, V_{GS}, of the NMOS switch (device M12) is always boosted to *VDD* and it is independent of input signal. This allows the switch to pass rail-to-rail signal and small R_{ON} can be obtained throughout the entire input range.

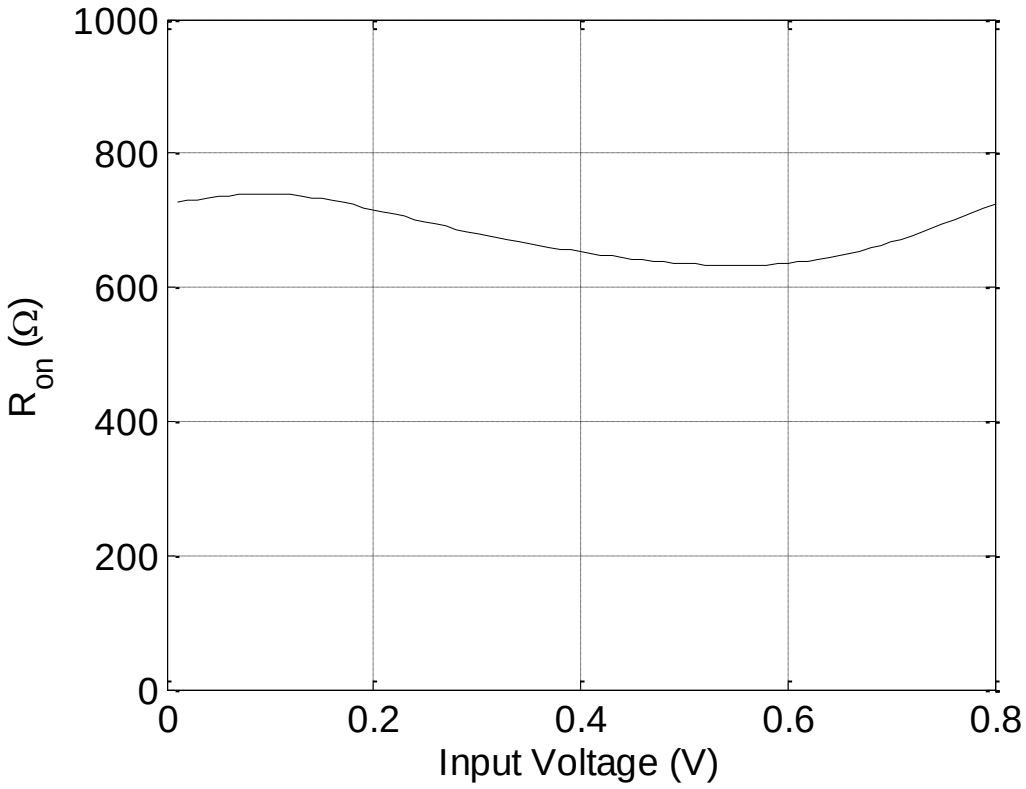

Fig. 3.8. Simulated R_{ON} of the bootstrapped switch versus input voltage.

Fig. 3.8 shows the simulated R_{ON} versus the input signal under a 0.8-V *VDD* supply. With a NMOS switch size of 15μm/0.35μm, the achieved R_{ON} is smaller than 740 Ω and variation is reasonably small across the rail-to-rail input range. Treating the S/H switch and the S/H array (with total capacitance of C_{SH}) as a resistor connected in

series with a capacitor, the input bandwidth of the sampling stage is defined as $1/(2\pi R_{ON} C_{SH})$. With C_{SH} of about 2.4 pF in this design, the input bandwidth is estimated to be larger than 90 MHz which guarantee the signal settling during sampling phase.

3.3.3 Capacitive Arrays

Ideally, the unit capacitance, C_0, should be as small as possible to reduce the power dissipation. In practice, C_0 is decided by considering the kT/C noise, capacitor matching, and error compensation requirement. In my 10-bit design, C_0 is limited by device matching according to the process document. Since the S/H array and DAC array are independent of each other and thus any mismatch between arrays will not affect the ADC linearity. However, the ADC linearity is still constrained by the capacitor matching within each array. Therefore, a $9.2 \times 9.2\ \mu m^2$ poly-insulator-poly (PIP) capacitor is used as the unit capacitor to achieve the required matching. From process document, capacitor mismatch is estimated to be less than 0.05% for adjacent units. The resulting unit capacitance value is 75 fF. Consequently, the total capacitance for S/H array and DAC array are about 2.4 pF and 76.8 pF, respectively.

Fig. 3.9 shows the layout detail of the capacitive array. The capacitive array is formed using carefully drawn unit capacitors to achieve better matching. Since the array size is proportional to the resolution, the common node for each array (i.e. V_{SH} and V_{DAC}) requires the longest connection across the layout and the resulting parasitic capacitor coupled to substrate can significantly affect the accuracy. Therefore, it is routed using Metal 3 which yields the smallest parasitic per unit area. Furthermore, Metal 1 is used

to shield the common node while providing connection to the bottom plate. Lastly, dummy capacitors are added at the edges of the array so that all capacitors see similar surrounding condition.

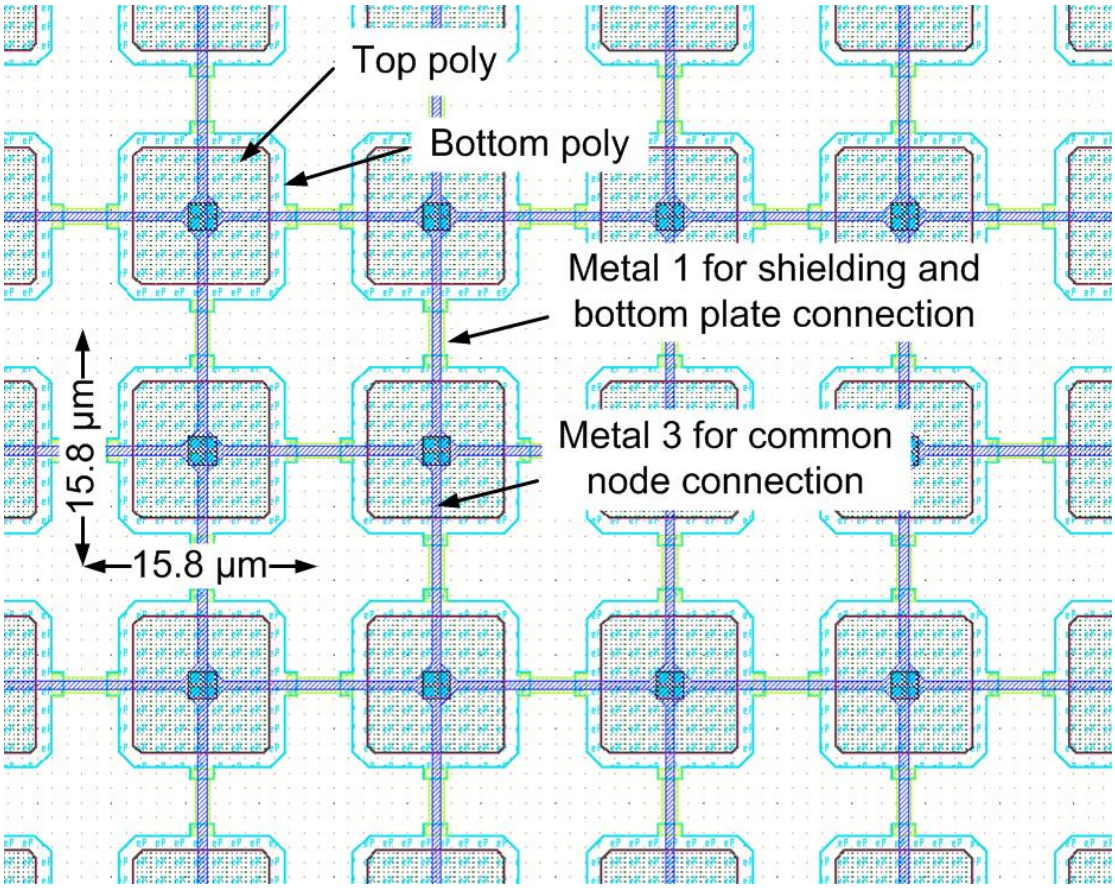

Fig. 3.9. Layout detail of the PIP capacitive array.

On the other hand, the switches of the capacitive arrays are implemented using inverters, as depicted in Fig. 3.10, because they only switch between *VDD* and *GND* for a rail-to-rail ADC. Detail transition is shown in Table 3.1. This greatly reduces the circuit complexity by avoiding the use of additional transmission gate or clock-boosting switch. Moreover, circuit optimization of the switches is now simplified. Each switch can be optimized separately by taking into account the propagation delay of an inverter driving a capacitive load.

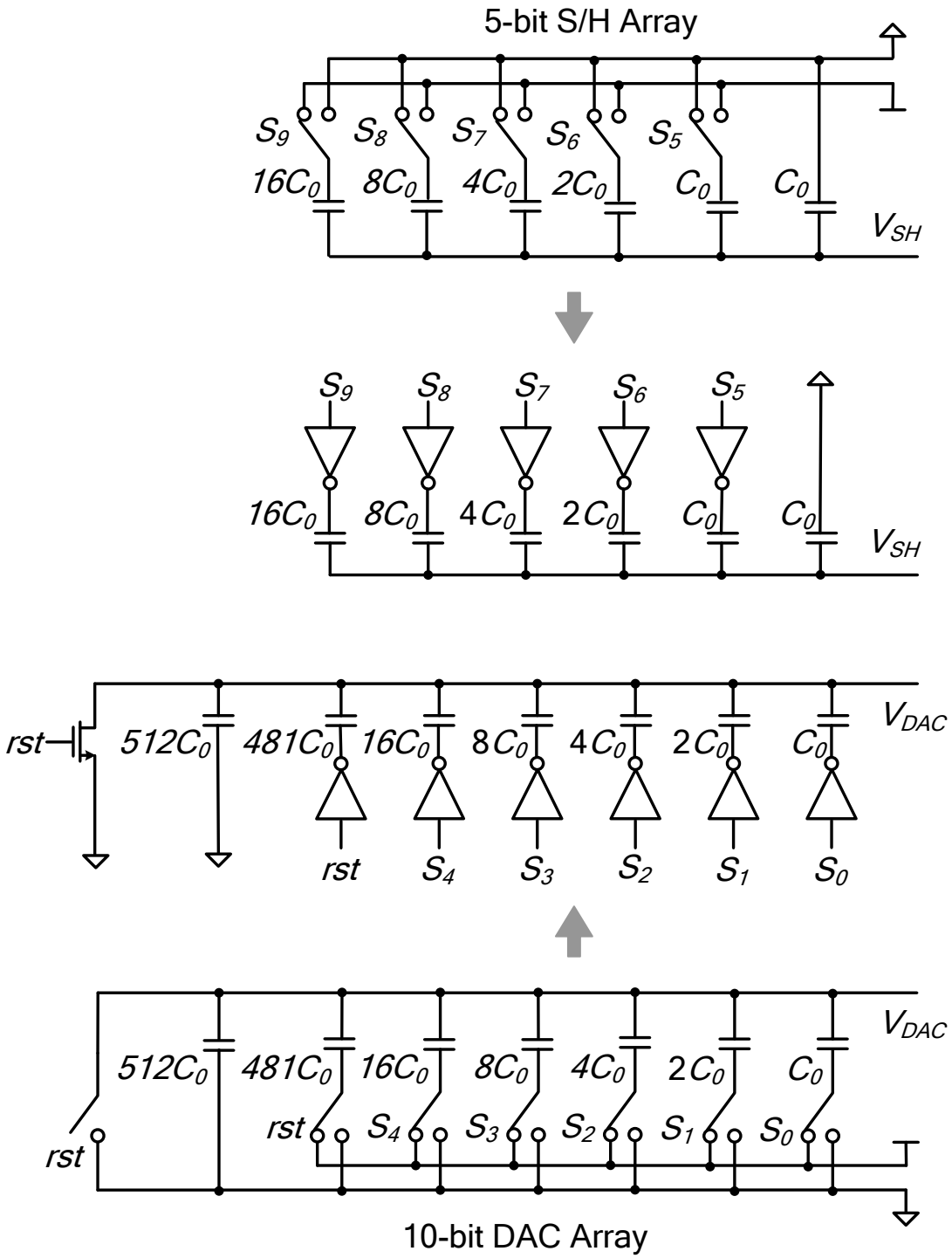

Fig. 3.10. Inverter-based switches for capacitive arrays.

In order to ensure that the settling error is less than 1/2 LSB, the settling time requirement for the capacitive array is set by

$$FS \cdot e^{-\frac{T_{clk}/2}{\tau_{array}}} < \frac{FS}{2^{n+1}} \Rightarrow \tau_{array} < \frac{T_{clk}}{2 \cdot (n+1) \cdot \ln 2}. \quad (3.5)$$

From Eq. (3.4) and (3.5), to achieve a 10-bit resolution and 10-kS/s sampling rate, τ_{array} is set to be less than 596 ns.

3.3.4 Dynamic Comparator

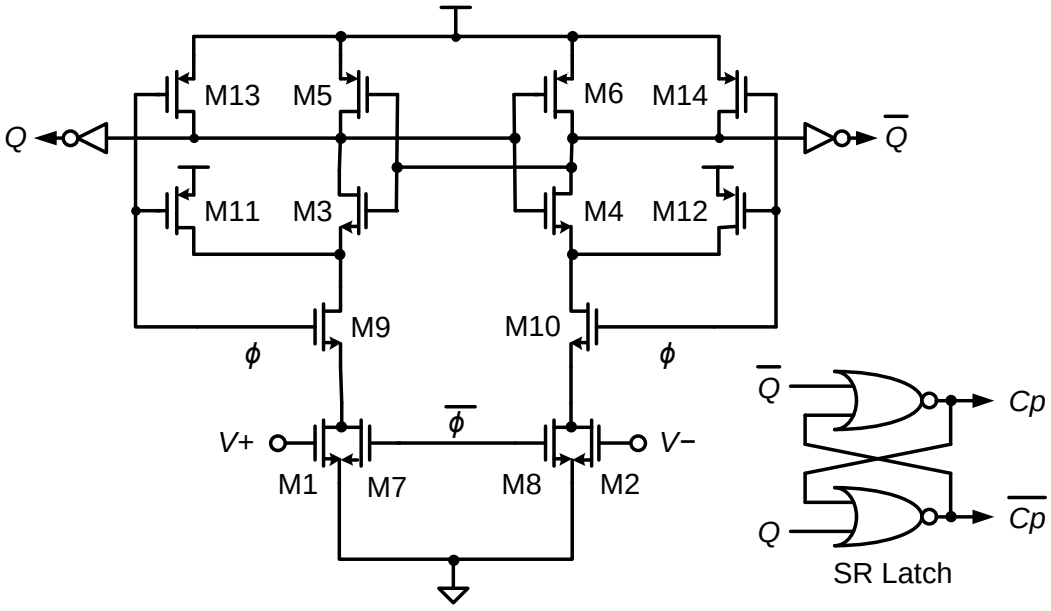

Fig. 3.11. Schematic of the dynamic comparator.

The simplified schematic for the dynamic comparator is shown in Fig. 3.11. It is implemented based on dynamic latch. It has no analog pre-amplifier in order to eliminate static current consumption. M1 and M2 form the comparator input which are connected to S/H array and DAC array. M3 to M6 are the cross-coupled pair providing positive feedback to the comparator. M7 to M14 are clocked switches synchronized with SAR. Minimum size inverters are inserted after the cross-coupled

pair in order to isolate the cross-coupled pair from any possible distortion. The comparator uses a set-reset (SR) latch to hold the comparison result.

According to Eq. (3.3), the required common-mode input range is 0.375 V to 0.4 V for a 0.8-V supply. This is achieved using NMOS input pair. From simulation result, the input pair, M1 and M2, has a common-mode input range of 0.315 V to 0.8 V, satisfying the derived specification.

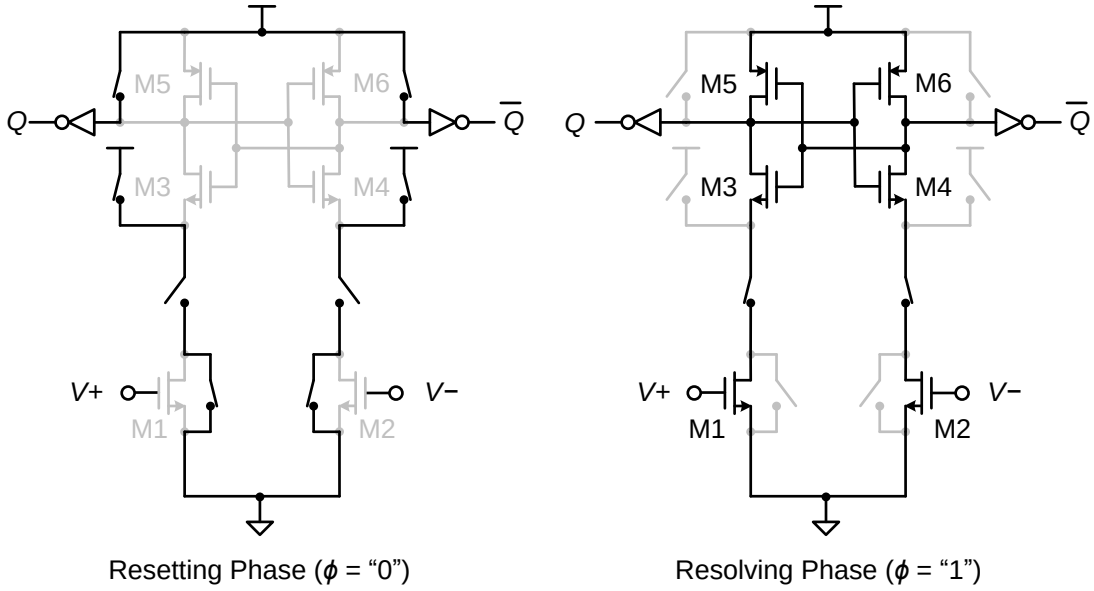

Fig. 3.12. Operations of the dynamic comparator.

Fig. 3.12 illustrates the operation of the dynamic comparator. The comparator operation has two phases, which are the resetting phase (ϕ = "0") and the resolving phase (ϕ = "1"). During resetting phase, all of the critical nodes are reset to minimize the hysteresis effect. On the other hand, the comparator will compare the inputs and produce the corresponding digital output during resolving phase. The pulling currents produced by the input pair will trigger the positive feedback cross-coupled pair and generate the comparison result.

We avoid offset cancellation techniques in order to maintain low power dissipation. As a trade-off, any V_t mismatch in input pair will directly result in ADC DC offset. This DC offset will not affect the ADC linearity and single sample offset calibration can be performed by using external DSP. Furthermore, V_t mismatch is suppressed by careful layout for M1 to M6 in order to limit the DC offset to a few LSBs.

3.4 Chip Verification and Measurement Results

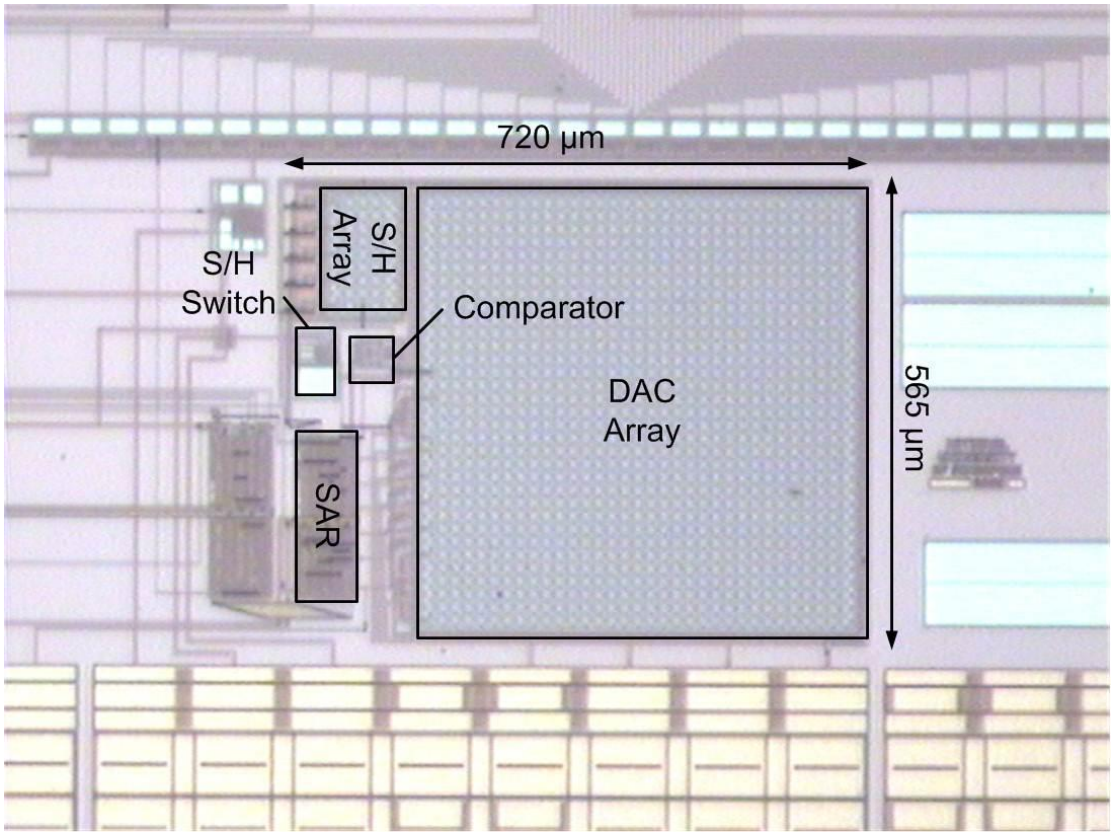

Fig. 3.13. Die photo of the 10-bit ADC prototype.

The chip prototype is fabricated in a standard 4-metal-2-poly (4M2P) 0.35-µm technology and packaged using ceramic quad flat pack (CQFP). The die photo is

shown in Fig. 3.13. The ADC core occupies a 565 × 720 μm² silicon area. The chip prototype was tested under a 0.8-V supply with 10-kS/s output rate. For performance measurement, Agilent 33250A Function/Arbitrary Waveform Generator was used to generate various test signals and 1672G Logic Analyzer was used to collect the ADC output. Since the power dissipation is expected to be very small, Agilent 4156C Precision Semiconductor Parameter Analyzer was used as the power supply and facilitates the power dissipation measurement.

3.4.1 Static Performance

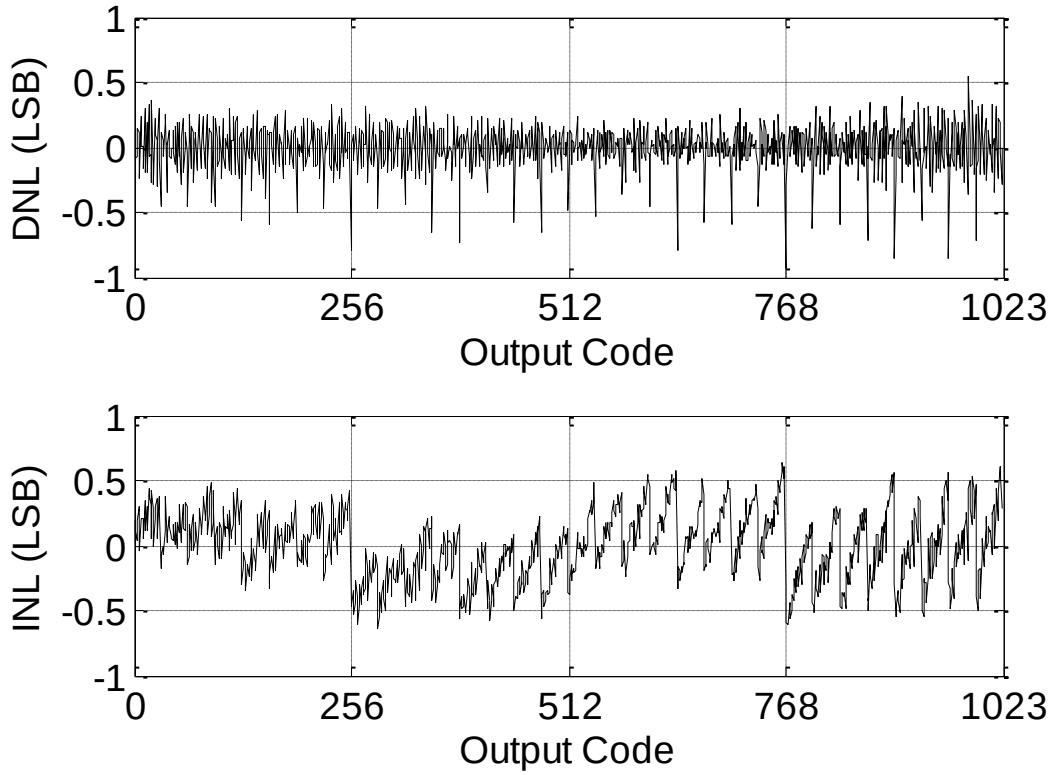

Fig. 3.14. Measured DNL and INL.

Fig. 3.14 shows the static performance for the ADC. Triangular input signal was used as input so that hysteresis effect is also taken into account. An average count of 56 samples per code were collected for result accuracy. The differential nonlinearity (DNL) is in the range of −0.93/+0.55 LSB while the integral nonlinearity (INL) is in the range of −0.64/+0.64 LSB. No significant bending is found in the INL. This proves that the ADC rail-to-rail linearity is unaffected by limiting the comparator input common-mode to a small range.

3.4.2 Dynamic Performance

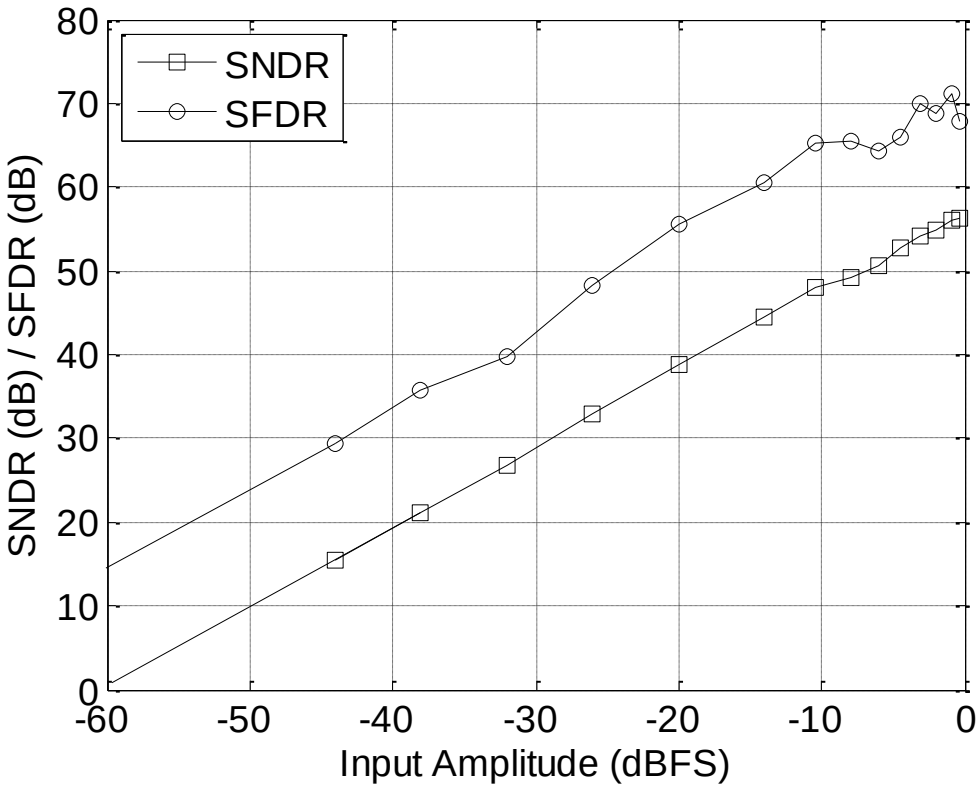

Fig. 3.15. Measured SNDR and SFDR versus input signal amplitude.

Fig. 3.15 plots the measured signal-to-noise-and-distortion ratio (SNDR) and spurious free dynamic range (SFDR) of the ADC with respect to the input stimulus amplitude at 147 Hz. The results prove that the ADC indeed achieves a rail-to-rail input range. Additionally, the ADC achieves a peak SNDR at rail-to-rail input of 56.4 dB while the SFDR is 67.9 dB. The SNDR corresponds to an effective number of bits (ENOB) of 9.07 bits. The ENOB is given by

$$ENOB = \frac{SNDR - 1.76}{6.02}. \tag{3.6}$$

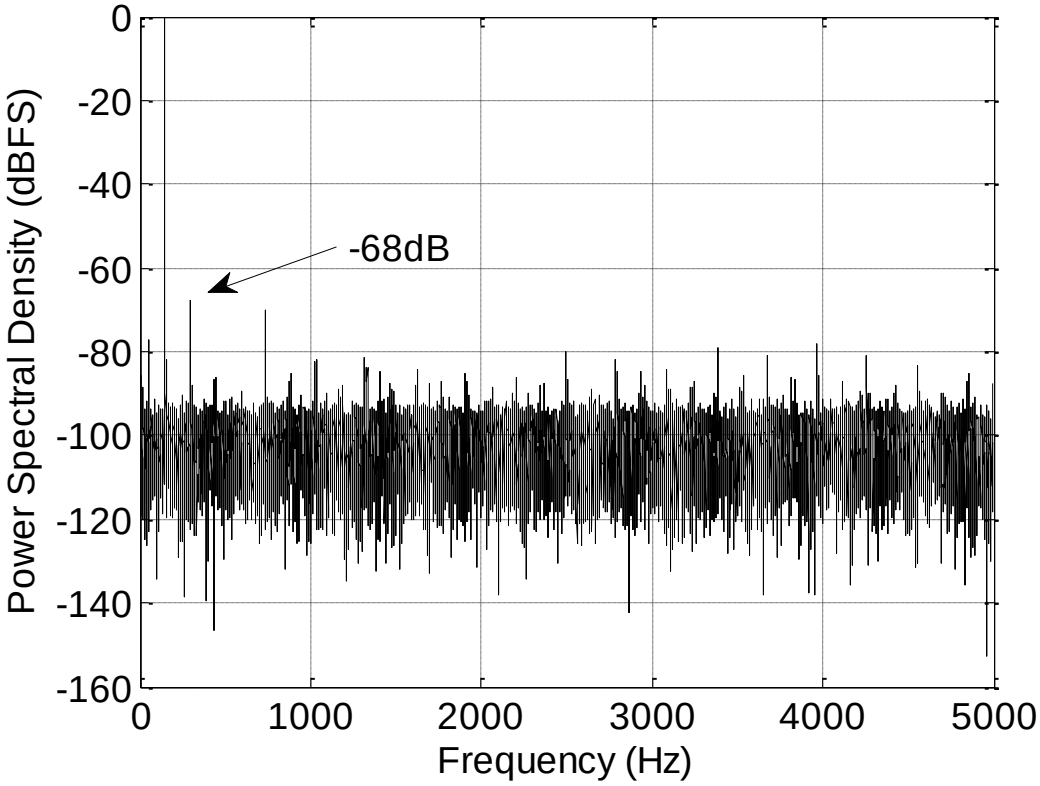

Fig. 3.16. Measured output PSD with 147-Hz rail-to-rail sine input.

Fig. 3.16 shows the measured ADC output spectrum where the ADC achieves its peak SNDR. The input signal was a rail-to-rail sine wave at 147 Hz. A total of 65535 samples were collected to derive the output spectrum. Since the proposed design is a

single-ended ADC, the main spurious tone is the second harmonic. Even so, the spurious is about −68 dBFS and has no significant effect on the SNDR.

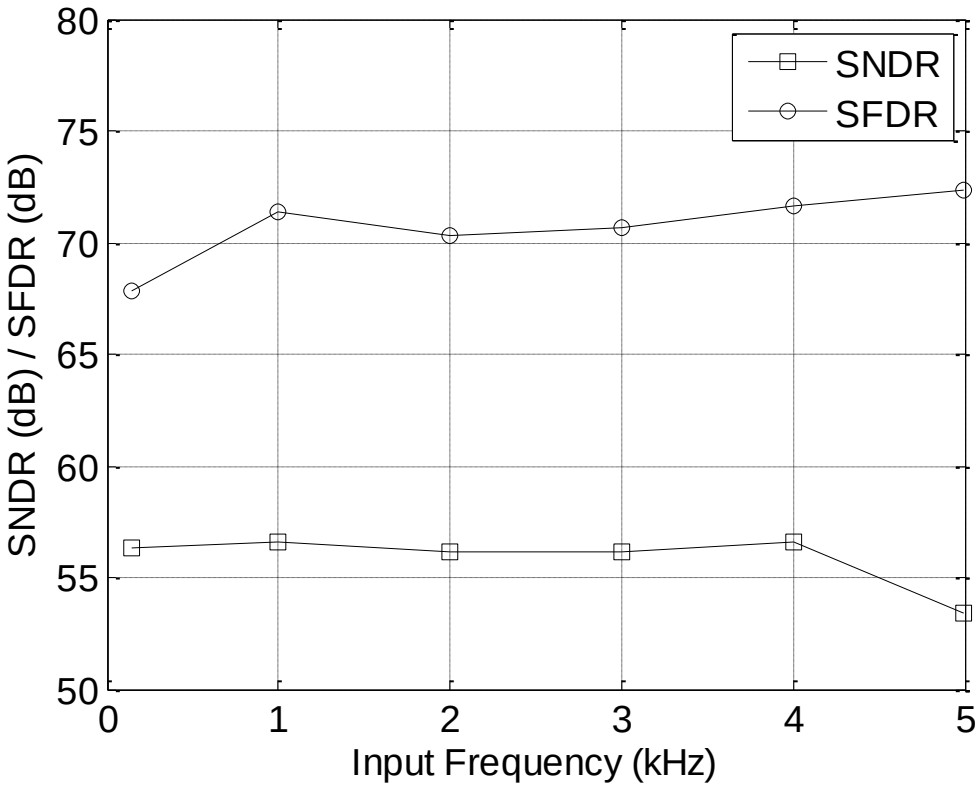

Fig. 3.17. Measured SNDR and SFDR versus input signal frequency.

Fig. 3.17 plots the measured measured SNDR and SFDR versus input signal frequency. The SNDR and SFDR are reasonably constant across the entire ADC Nyquist bandwidth. The mean SNDR and SFDR are 55.9 dB and 70.7 dB, respectively.

3.4.3 Power Dissipation

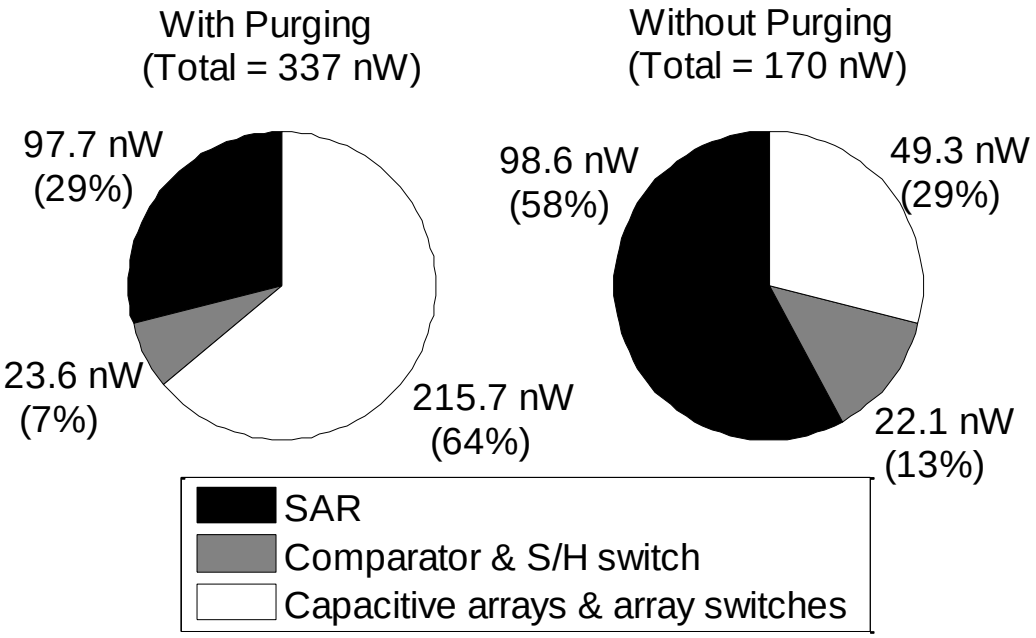

Fig. 3.18. ADC power distribution with purging (left) and without purging (right).

At 0.8-V supply and 10-kS/s output rate, the measured ADC power dissipation and the distribution among the main blocks are shown in Fig. 3.18. Although the ADC has same performance for operation with and without the purging of DAC array after each conversion, the power dissipations for both cases are shown for comparison. If purging is performed for every conversion, the total power is 337 nW and power dissipation in capacitive arrays (including the power consumed by array switches and their drivers) is dominating. On the other hand, without purging of DAC array, the power dissipation of the ADC is reduced to 170 nW. The savings is achieved in capacitive arrays while the power dissipation in SAR, comparator and S/H switch are about the same. From Fig. 3.18, since the power digital SAR is now dominant, it is possible for the proposed design to achieve lower power if the proposed design is scaled down to more advanced technology which favors the digital SAR.

3.4.4 Summary and Comparison

Table 3.2 Summary of measurement result.

Technology	0.35μm CMOS
Supply voltage (V)	0.8
Input swing	Rail-to-rail
Total power dissipation (nW)	170
Sampling rate (Sample/s)	10k
SNDR (dB) / SFDR (dB)	56.4 / 67.9
ENOB (bit)	9.07
DNL (LSB)	−0.93 / +0.55
INL (LSB)	−0.64 / +0.64
Power dissipation (μW)	0.17
FOM (fJ/conversion-step)	32

Table 3.2 summarizes the measured ADC performance. The proposed design operates under a 0.8-V supply and has a rail-to-rail input range. It achieves an ENOB of 9.07 bits at 10-kS/s sampling rate.

Table 3.3 Comparison with state-of-the-art designs.

Design	JSSC'03 [33]		JSSC'07 [35]	JSSC'07 [34]			JSSC'07 [44]	This work
Technology	0.18μm		0.18μm	0.18μm			90nm	0.35μm
Supply voltage (V)	1	0.6	1	1	0.9	0.83	0.5	0.8
Input swing/Supply voltage	0.5	0.5	N/A	1	1	1	2	1
Sampling rate (S/s)	150k	34k	100k	400k	200k	111k	1.5M	10k
ENOB (bit)	8.21	7.43	10.55	7.31	7.58	7.46	5.15	9.07
Power dissipation (μW)	30	3.12	25	6.15	2.47	1.16	7	0.17
FOM (fJ/conversion-step)	674	531	167	97	65	60	140	32

The proposed ADC is compared with other state-of-the-art low-voltage designs at the time of publication in Table 3.3. Figure of merit (FOM) is used to benchmark the energy efficiency of the ADC. The FOM is defined as

$$FOM = \frac{Power}{2^{ENOB} \cdot f_S}. \tag{3.7}$$

The proposed design achieves a FOM of 32 fJ/conversion-step. Despite the technology used, the proposed design achieves the lowest FOM. This means that the proposed ADC structure is more energy-efficient than the existing designs because it spends the least energy for an effective AD conversion step.

3.5 Practical Application – EEG Recording Interface

3.5.1 32-Channel EEG Recording Interface

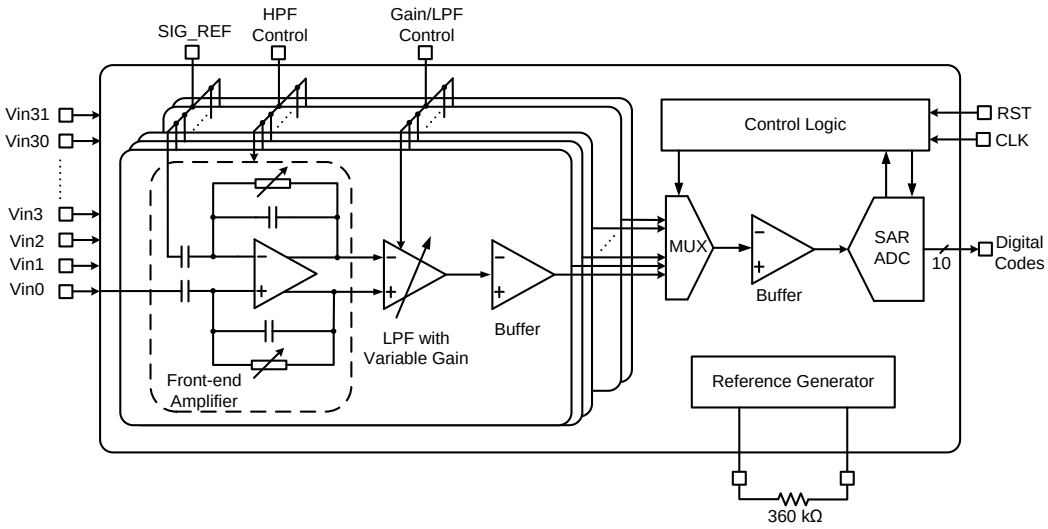

Fig. 3.19. System diagram of the 32-channel EEG recording interface.

The proposed SA ADC was put to test by integrating it into a practical EEG recording interface [12]. Fig. 3.19 depicts the system diagram of the 32-channel EEG recording interface. The recording interface consists of 32 analog front-ends with low-noise

amplifier, filter, and variable gain amplifier (VGA). The detail circuit design for analog front-end is discussed in [12, 19].

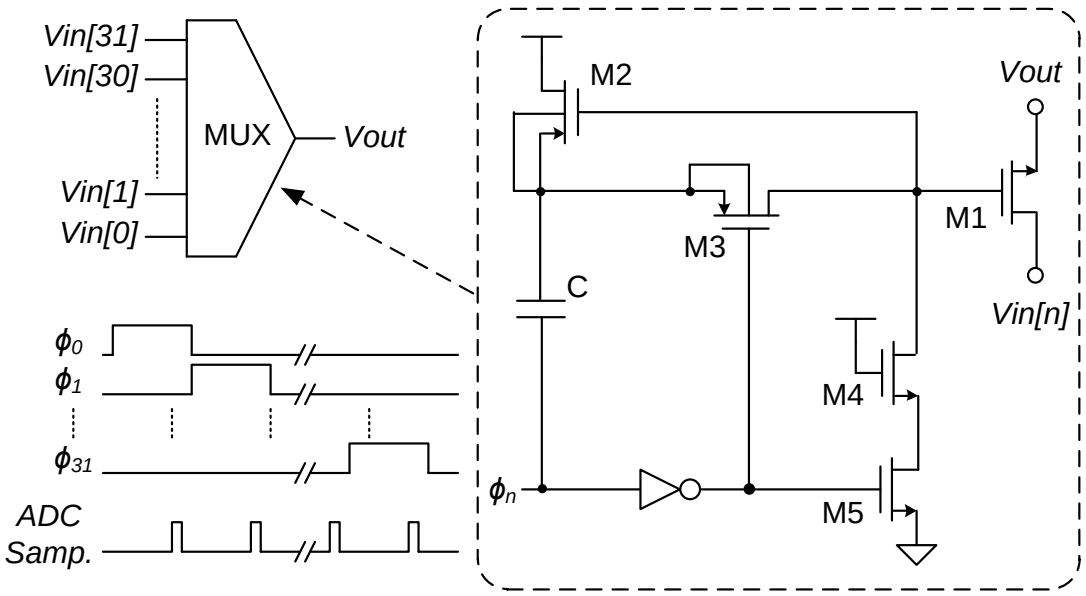

Fig. 3.20. Schematic of 32-to-1 analog multiplexer.

On the other hand, all channels are multiplexed to the ADC for AD conversion using an analog multiplexer. The multiplexer is implemented using bootstrapped switches as shown in Fig. 3.20. Bootstrapped technique allows reduced size NMOS to be used as the switch. Consequently, the associated parasitic capacitance and on-resistance of the switches are smaller as compared to conventional transmission gate. This not only ensures that the system bandwidth is not limited by the multiplexer but also minimizes the signal interference between channels. As shown in the timing diagram, the multiplexer multiplexes 32 inputs to the ADC in sequential order. Its switching is misaligned with ADC sampling and sufficient settling time is assigned before ADC sampling to minimize signal distortion. Buffers are inserted before and after the multiplexer in order to address the driving issue.

The complete die photo of the 32-channel EEG recording interface is shown in Fig. 3.21. It occupies a silicon area of 2.6 × 1.8 mm².

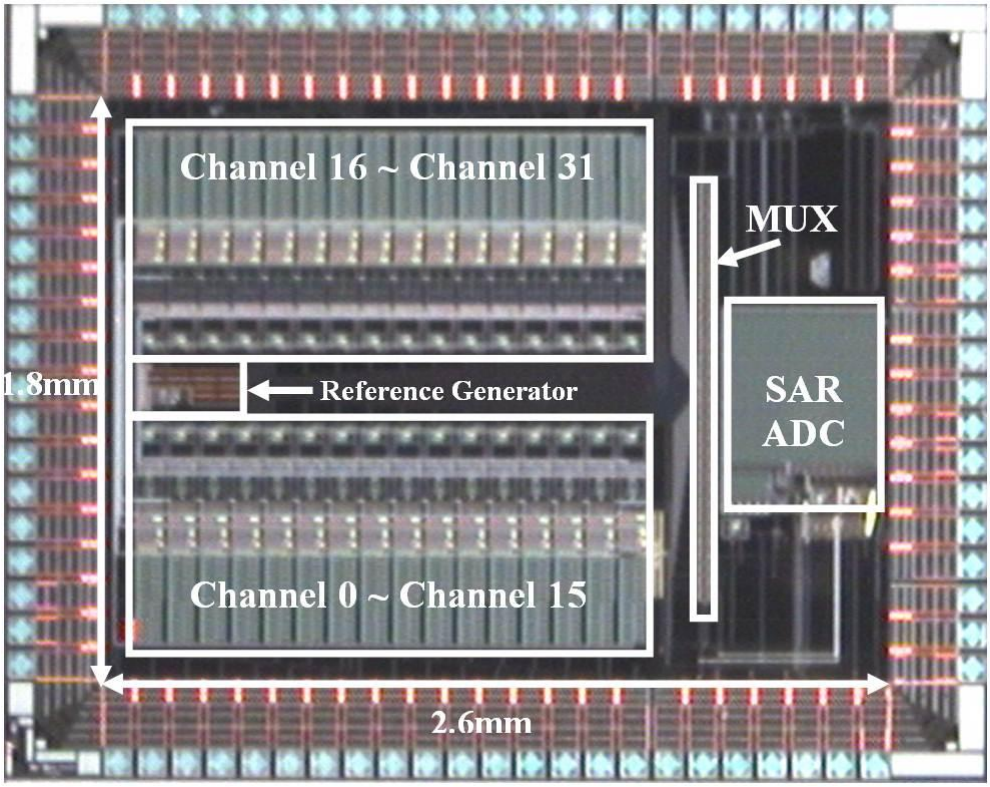

Fig. 3.21. Die photo of the EEG recording interface.

3.5.2 Clinical Trial: EEG Recording

Clinical trial on EEG recording was carried out using the recording interface. Fig. 3.22 shows one of the recordings on two EEG channels, i.e. O_Z and P_Z. Both of the eye open and eye closed periods are recorded for comparison. During eye closed, repetitive Alpha waves[1] are identified. The PSD for both cases are potted in Fig. 3.23.

[1] Alpha waves are neural oscillations in the frequency range of 8–12 Hz arising from synchronous and coherent (in phase/constructive) electrical activity of thalamic pacemaker cells in humans.

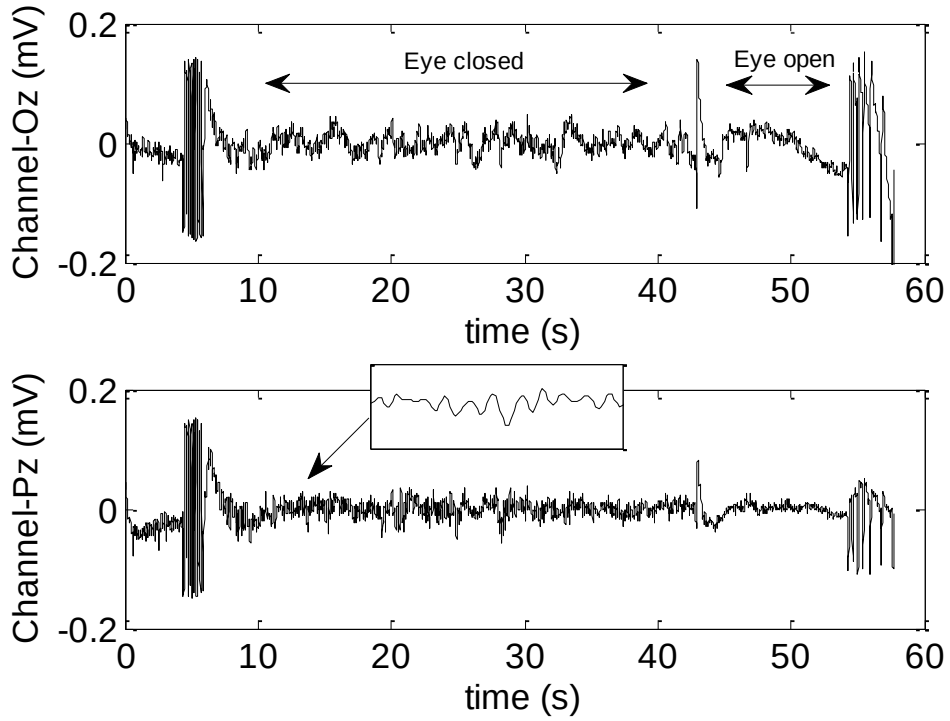

Fig. 3.22. EEG recording on O_Z and P_Z: Alpha wave is identified when eye is closed.

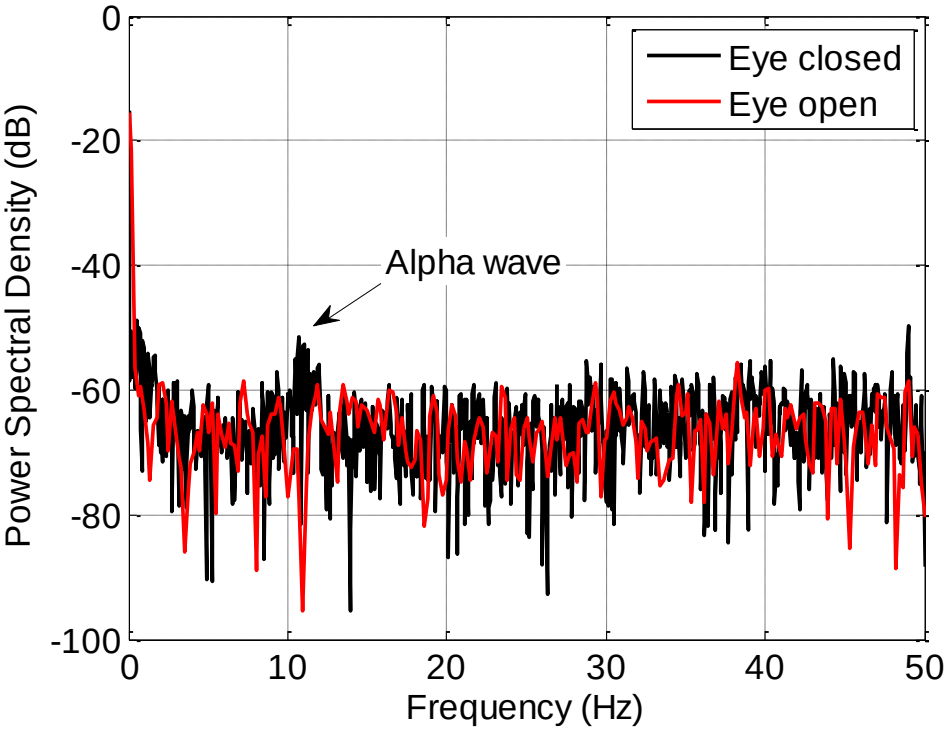

Fig. 3.23. PSD showing Alpha wave (8-12 Hz) during eye closed period.

It is very clear that the eye closed period consists of strong Alpha wave at frequency range around 8-12 Hz, as compared to eye open period which does not contain any Alpha wave.

CHAPTER 4

MULTI-CHANNEL ADC FOR BIOMEDICAL SENSOR APPLICATION

4.1 Overview

In CHAPTER 3, a dual-capacitive-array architecture to implement the SA ADC for biomedical sensor application was presented. The proposed design is a general structure which is suitable for typical biomedical signal acquisition. However, it does not readily support multi-channel application. As shown in Section 3.5, the proposed ADC requires an analog multiplexer if it is used for the AD conversion for several channels. Moreover, additional buffers are needed before and after the multiplexer to address the driving issue. For ECG and EEG sensor application with relatively small signal bandwidth (< 150 Hz), a multi-channel system based on analog multiplexer can be easily accomplished with minimum trade-off in power dissipation because of rather insignificant system bandwidth and slew-rate requirements. However, the power overhead for implementing a multi-channel system based on multiplexer can be very high in sensor application with higher signal bandwidth, for instance neural signal recording with about 10-kHz signal bandwidth.

Therefore, a 0.6-V 8-bit 8-channel ADC is proposed in this chapter. Similar to the previous design, this ADC is designed to be rail-to-rail, so that the ADC operates between *VDD* and *GND* only, and thus eliminate the use of operational amplifier and additional reference generator under low supply voltage. Moreover, the design makes

use of the proposed dual-capacitive-array structure and introduce time-interleaved sample-and-hold (S/H) architecture by integrating the multiplexing function within the converter to provide multi-channel conversion. The proposed 8-channel ADC prototype readily supports eight channels with minimum additional overhead from a system perspective. It achieves a mean effective number of bits (ENOB) of 7.59 bits with 240-kS/s total output rate while dissipates 1.23 μW from a 0.6-V supply. Additionally, measurement results show that the ADC operates robustly, with more than 7-bit ENOB maintained, for 0.5-V to 0.75-V supply and over a temperature range of 25℃ to 70℃. Last but not least, the ADC per-channel sampling rate is scalable from 3 kS/s to 50 kS/s, makes it most suitable for various multi-channel biomedical sensor applications.

4.2 Time-Interleaved S/H Stage for Multi-Channel System

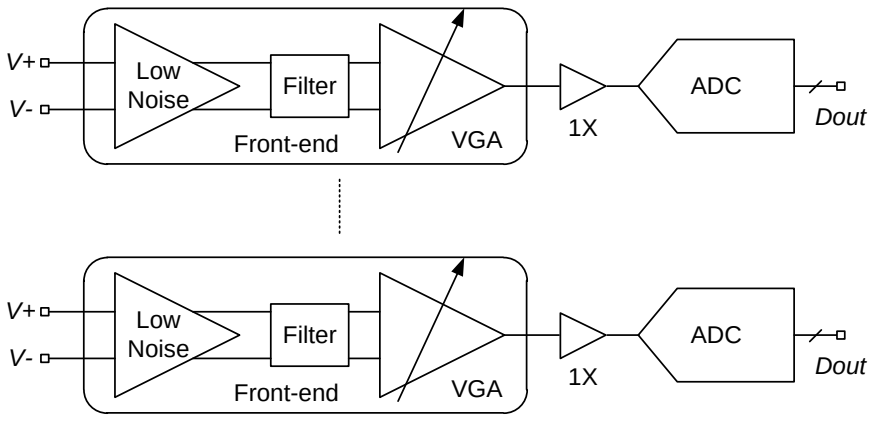

Fig. 4.1. Independent ADC for each channel.

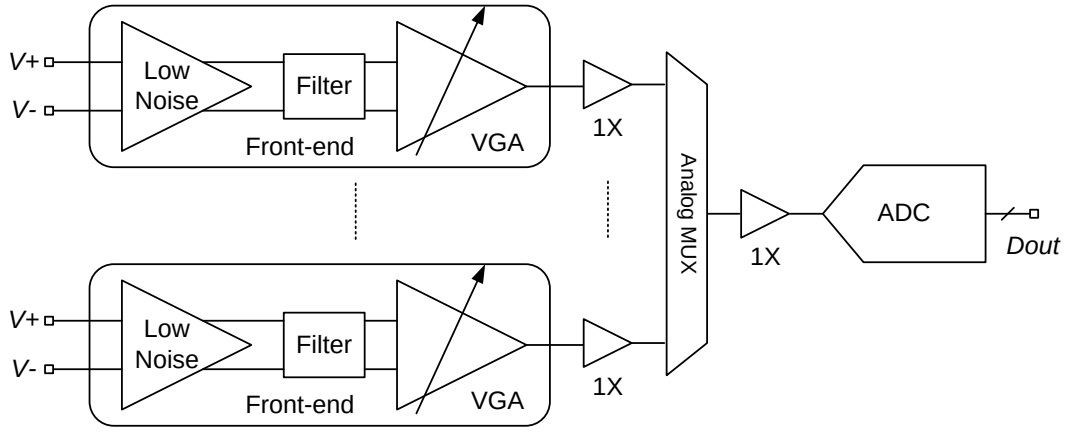

Fig. 4.2. Sharing of ADC through multiplexer.

The most direct method of implementing a multi-channel AD conversion system for biomedical sensor interface is to employ independent ADC for each channel as shown in Fig. 4.1. In this case, all channels are treated as separated channel. However, this requires large silicon area due to the duplicated ADC [45]. A cost effective way is to share one ADC among several channels through analog multiplexer, as illustrated in Fig. 4.2 [4, 12, 46]. In this case, the ADC is to switch among a number of inputs within a limited settling time and demands more stringent dynamic requirement at system level [47].

As a result of time multiplexing, the maximum difference in signal level between two consecutive samples could be as large as ADC input full scale, *FS*, when the consecutive inputs are at maximum amplitude but completely out of phase. Assuming n+1 clock cycle, T_{clk}, is used for an n-bit SA ADC and the ADC is multiplexed to support m input channels with bandwidth of f_{signal}. Taking into account Nyquist-Shannon sampling theorem, the sampling time, t_{s1}, available for each channel is

$$t_{s1} = \frac{1}{(n+1)} \cdot \frac{1}{2 \cdot m \cdot f_{signal}} = T_{clk} . \tag{4.1}$$

While the holding time due to *n*-bit conversion is proved to be

$$t_h = \frac{n}{(n+1)} \cdot \frac{1}{2 \cdot m \cdot f_{signal}} = n \cdot T_{clk} . \tag{4.2}$$

The system bandwidth requirement can be estimated by considering a first-order model during tracking phase. To achieve a tracking error of less than 1/2 LSB, we require that

$$FS \cdot e^{-2 \cdot \pi \cdot f \cdot t_s} < \frac{1}{2} \cdot \frac{FS}{2^n} . \tag{4.3}$$

From Eq. (4.1) and (4.3), the required system bandwidth is approximately

$$f_1 > \frac{m \cdot (n+1)^2 \cdot \ln 2}{\pi} \cdot f_{signal}. \tag{4.4}$$

And the required slew rate is given by

$$SR_1 > \frac{FS}{t_{s1}} = 2 \cdot m \cdot (n+1) \cdot FS \cdot f_{signal}. \tag{4.5}$$

As revealed by Eq. (4.4) and (4.5), the system requires excessively large bandwidth and slew rate comparing to the bandwidth of target signal. Consequently, the ADC must be preceded by a buffer with sufficient bandwidth and slew rate to address the tracking error. This explains the excessive power dissipation for buffers in [4], where the power dissipation for buffer is more than 30 times compared to the low-noise preamplifier. This is inefficient from a system perspective, even if a high efficiency ADC with low figure of merit (FOM) is used in the sensor interface. In addition, the use of analog MUX is the same as inserting additional switches in the critical signal

path that results in undesirable signal distortion [48], especially under low voltage operation with limited voltage headroom.

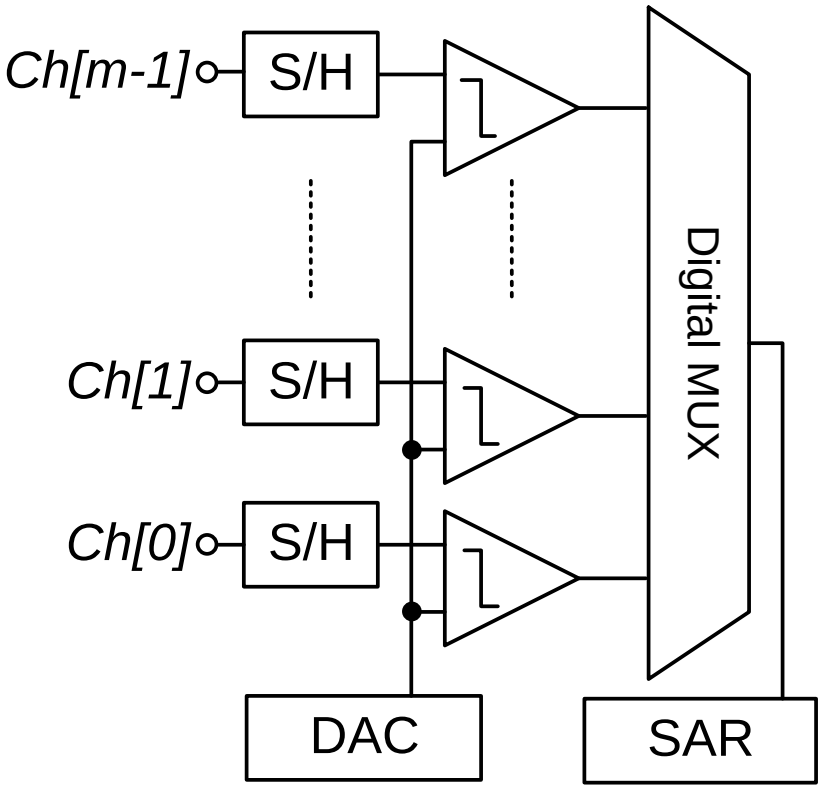

Fig. 4.3. An *m*-channel SA ADC with time-interleaved S/H stages.

Therefore, it is the goal of research to design a multi-channel ADC supporting multiple channels in order to eliminate the use of large bandwidth buffers and analog MUX. Fig. 4.3 illustrates the time-interleaved S/H stage architecture and the resulting multi-channel SA ADC. The multi-channel SA ADC consists of independent S/H stage and comparator for every channel while sharing the large digital-to-analog converter (DAC). Comparison results are being multiplexed to the successive approximation register (SAR) using a digital multiplexer (MUX). As oppose to analog multiplexing, this architecture can be known as digital multiplexing since the signals are being multiplexed only after quantization. The total ADC output rate is the same as in conventional single-channel design, but is evenly distributed among all channels.

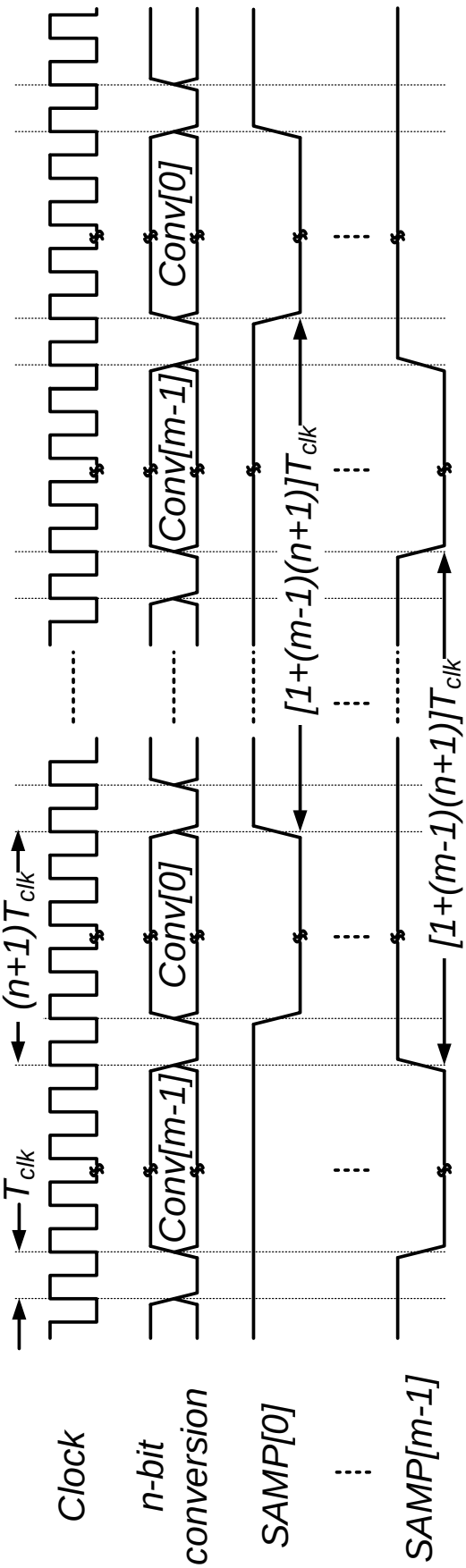

Fig. 4.4. Timing diagram for time-interleaved S/H stages architecture.

As illustrated by the timing diagram in Fig. 4.4, an *n*-bit conversion is performed for each input channel in sequential order. The holding time, t_{h2}, is the same as in conventional case as given by Eq. (4.2). Since only one input channel is active during conversion and each channel has independent S/H stage, the sampling time is much longer as compared to its conventional single-channel ADC. As shown in Fig. 4.4, the available sampling time, t_{s2}, is

$$t_{s2} = \left[1+(m-1)\cdot(n+1)\right]\cdot T_{clk}$$

$$= \left[1+(m-1)\cdot(n+1)\right]\cdot \frac{1}{(n+1)}\cdot \frac{1}{2\cdot m\cdot f_{signal}}$$

$$\approx (m-1)\cdot \frac{1}{2\cdot m\cdot f_{signal}}. \tag{4.6}$$

By lengthening the sampling time, the ADC effectively allows larger window for signal settling. Consider the worst case when the maximum change in input signal is close to rail-to-rail. From Eq. (4.3) and (4.6), the required system bandwidth, f_2, to achieve 1/2 LSB tracking error is approximately

$$f_2 > \frac{\left[m/(m\text{-}1)\right]\cdot(n+1)\cdot \ln 2}{\pi}\cdot f_{signal}. \tag{4.7}$$

And the required slew rate can be found as

$$SR_2 > \frac{FS}{t_{s2}} = \frac{2\cdot m}{(m-1)}\cdot FS\cdot f_{signal}. \tag{4.8}$$

Table 4.1 compares the conventional analog multiplexing with proposed time-interleaved S/H architecture (digital multiplexing) in the case of an 8-bit 8-channel

system. It is proved that the proposed multi-channel ADC based on time-interleaved S/H stage architecture provides sampling time that is 64 times longer comparing to its counterpart in conventional design. Consequently, both of the bandwidth and slew rate requirements are relaxed by about 63 times. From a system perspective, the proposed multi-channel ADC readily supports multiple channels without the need of analog multiplexer and power-consuming buffer.

Table 4.1 System bandwidth and slew-rate requirements for conventional analog multiplexing and proposed time-interleaved S/H architecture.

Architecture	Analog Multiplexing	Time-Interleaved S/H
Sampling time	T_{clk}	64 T_{clk}
Holding time	8 T_{clk}	8 T_{clk}
Required bandwidth	143 f_{signal}	2.27 f_{signal}
Required slew rate	144 $FS{\cdot}f_{signal}$	2.29 $FS{\cdot}f_{signal}$

4.3 Circuit Implementation

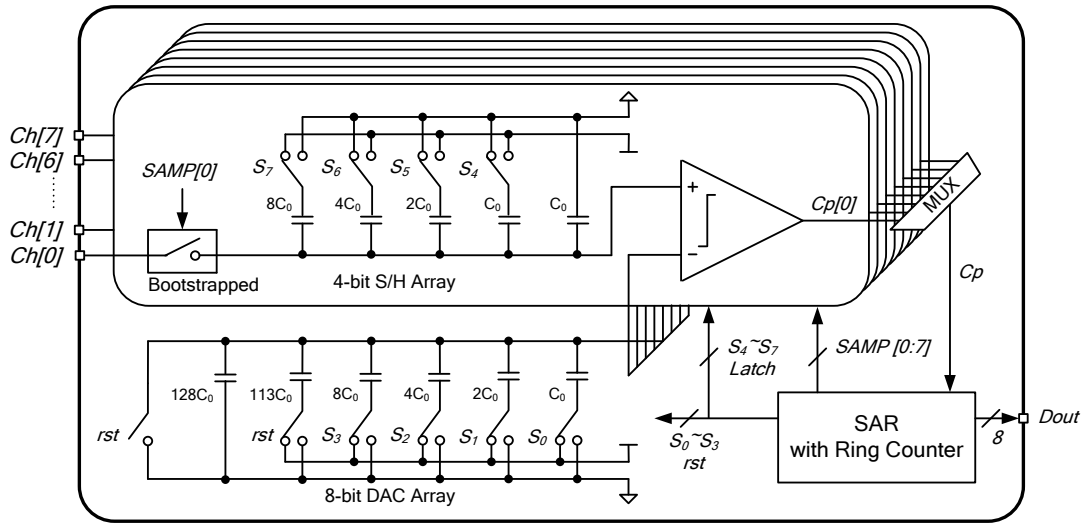

Fig. 4.5. 8-bit 8-channel SA ADC based on dual-capacitive-array.

Table 4.2 State transition for multi-channel analog-to-digital conversion.

Cycle	State	*Dout*	*SAMP[m]*	Switching on Capacitive Array								
				S/H Array				DAC Array				
				S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	*rst*
0~62	Sampling	-	1	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*
63	Sampling with Purging of DAC	-	1	0	1	1	1	1	1	1	1	1
	Sampling without Purging of DAC	-	1	0	1	1	1	0	0	0	0	0
64	Successive Approximation	$D_7=Cp_7$	0	Cp_7	0	1	1	0	0	0	0	0
65		$D_6=Cp_6$	0	Cp_7	Cp_6	0	1	0	0	0	0	0
66		$D_5=Cp_5$	0	Cp_7	Cp_6	Cp_5	0	0	0	0	0	0
67		$D_4=Cp_4$	0	Cp_7	Cp_6	Cp_5	Cp_4	1	0	0	0	0
68		$D_3=Cp_3$	0	Cp_7	Cp_6	Cp_5	Cp_4	$\overline{Cp_3}$	1	0	0	0
69		$D_2=Cp_2$	0	Cp_7	Cp_6	Cp_5	Cp_4	$\overline{Cp_3}$	$\overline{Cp_2}$	1	0	0
70		$D_1=Cp_1$	0	Cp_7	Cp_6	Cp_5	Cp_4	$\overline{Cp_3}$	$\overline{Cp_2}$	$\overline{Cp_1}$	1	0
71		$D_0=Cp_0$	0	Cp_7	Cp_6	Cp_5	Cp_4	$\overline{Cp_3}$	$\overline{Cp_2}$	$\overline{Cp_1}$	$\overline{Cp_0}$	0

Note: $Cp_{0:7}$ are the comparator output; $X \rightarrow$ don't care.

The proposed dual-capacitive-array architecture in CHAPTER 3 enables the circuit implementation of time-interleaved S/H multi-channel ADC. Fig. 4.5 illustrates the schematic of an 8-bit 8-channel SA ADC. Duplicated 4-bit S/H arrays and comparators form the time-interleaved S/H stages while comparator results are multiplexed to SAR using a digital MUX. The larger 8-bit DAC array is connected to all comparators for sharing. Both of the DAC array and SAR are always running but only one specific pair of S/H array and comparator will be active at a time.

Table 4.2 shows the state transition for one of the ADC channels. As oppose to the single-channel design in Table 3.1, signal *SAMP* is added to clock-gate the S/H array or toggle the successive approximation among different channels. For the first 63 cycles (Cycle 0 to Cycle 62), the respective S/H array is in sampling mode while the shared DAC array is performing successive approximation on other channels and any switching on DAC array is irrelevant at this moment. Sampling continues into Cycle 63 and the DAC is reset for successive approximation. In the last 8 cycles, clock-gating is disabled (i.e. *SAMP* = "0") and an 8-bit successive approximation will be carried out for this specific channel in order to produce the corresponding digital output code.

The following sections explain the circuit of each block in detail.

4.3.1 S/H Switch

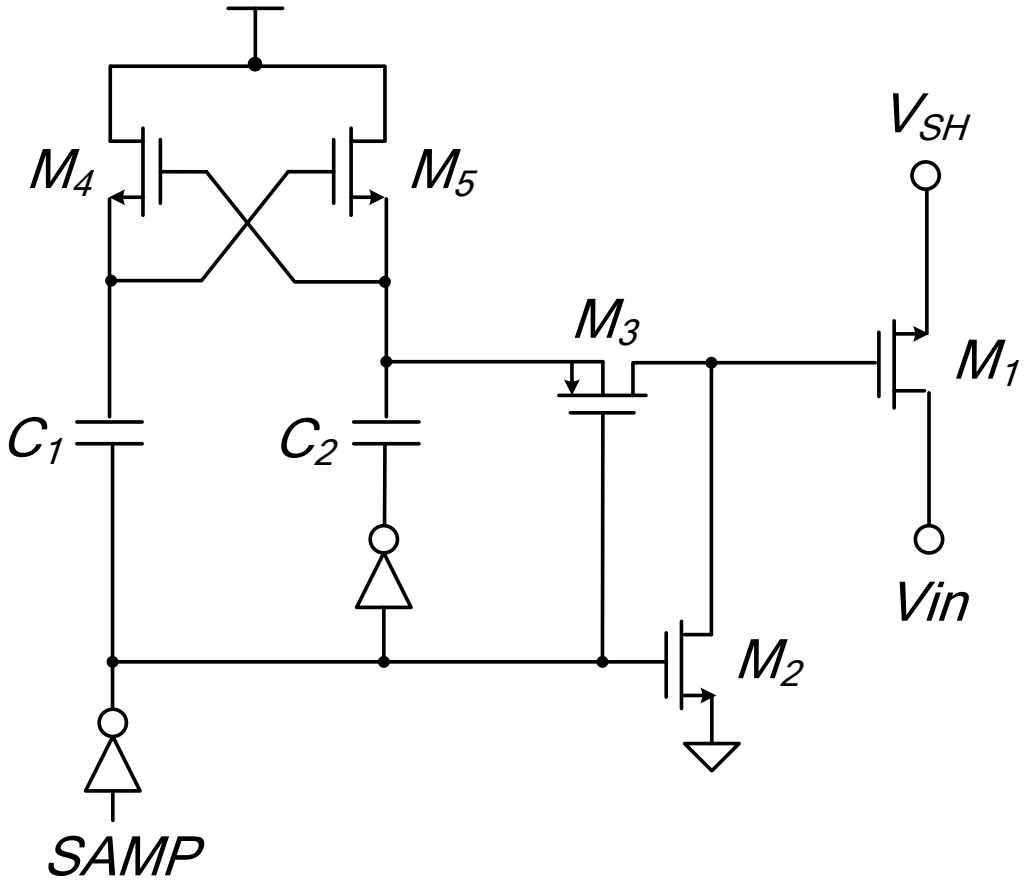

Fig. 4.6. Clock boosting S/H switch.

The clock-boosting S/H switch [34, 44] is used to realize rail-to-rail input range under low supply voltage. As shown in Fig. 4.6, the gate voltage of M1 is boosted to 2 × *VDD* during sampling in order to achieve small R_{on}. Both of the boosting capacitors C1 and C2 are chosen to be 1 pF so that the boosted voltage is unaffected by parasitic capacitance associated with the M1 gate node. According to simulation result, R_{on} with chosen W/L ratio of 30 is less than 0.4 kΩ over the entire input range (see Fig. 4.7). With S/H array total capacitance of 2.5 pF, the bandwidth is estimated to be more than 160 MHz. This guarantees that the sampling accuracy is not restricted by the S/H switch.

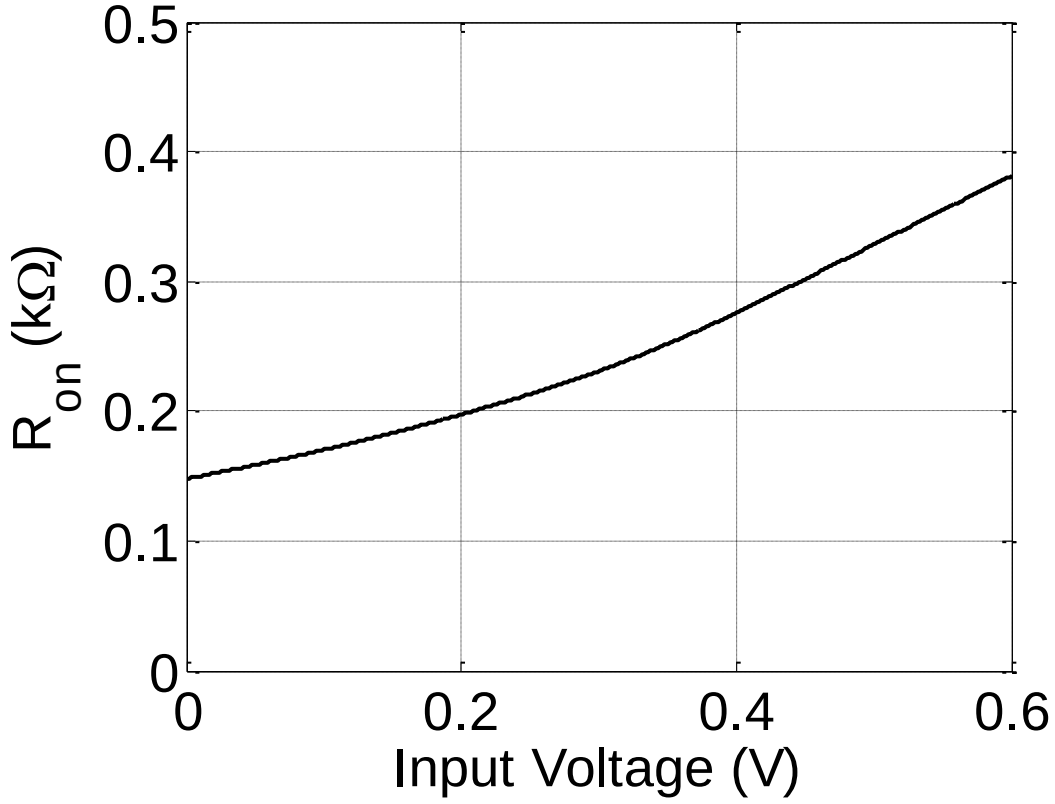

Fig. 4.7. Simulated R_{on} for the clock boosting S/H switch.

4.3.2 Capacitive S/H and DAC Arrays

Since all of the S/H arrays and DAC array are independent of each other and thus any mismatch between arrays will not affect the ADC linearity. However, the ADC linearity is still constrained by the capacitor matching within each array. Therefore, an 8.5 μm × 8.5 μm metal-insulator-metal (MIM) capacitor is used as the unit capacitor and thus the mismatch is limited to 0.5% according to process document. The resulting unit capacitance value is 153 fF. Consequently, the total capacitance for S/H array and DAC array are about 2.5 pF and 40 pF, respectively. Fig. 4.8 shows the

layout detail. The capacitive array is formed using identical unit capacitors with dummy unit at all edges to achieve better matching.

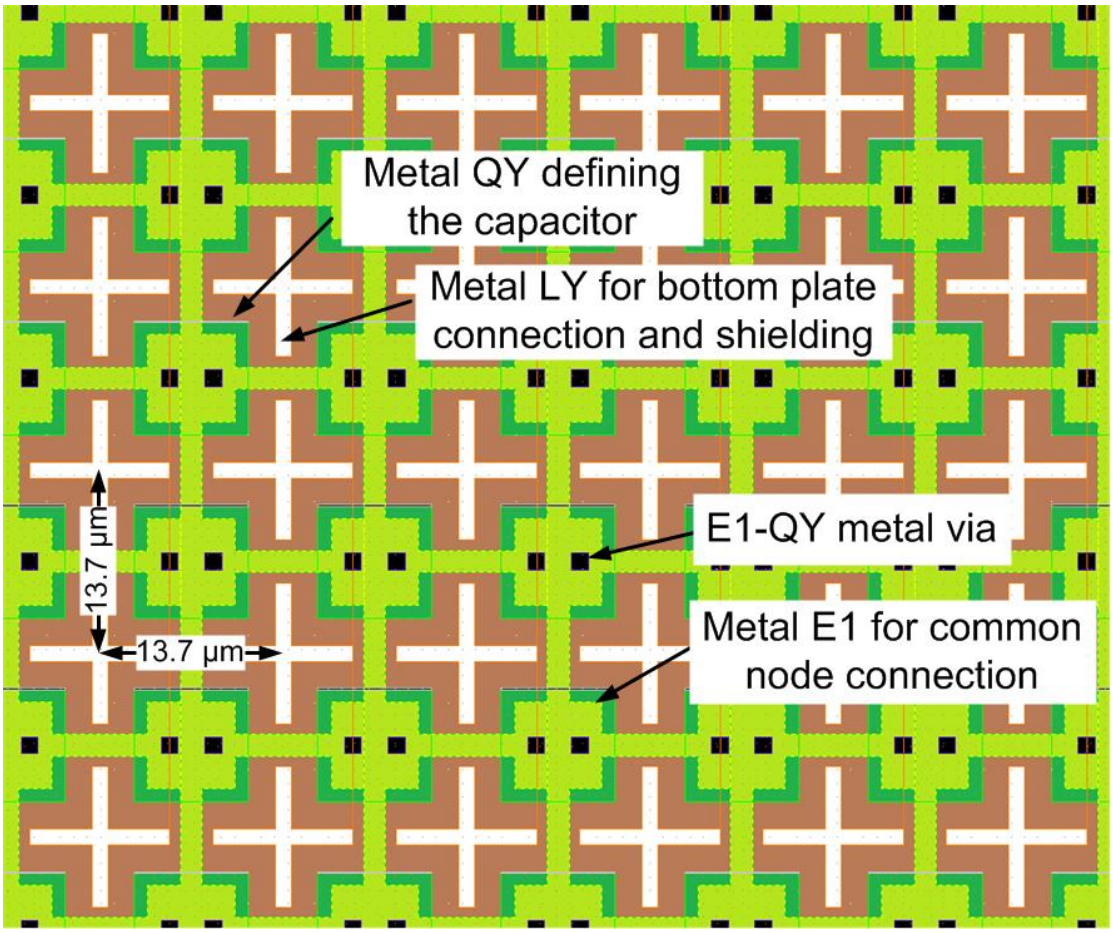

Fig. 4.8. Layout detail of the MIM capacitive array.

Fig. 4.9 shows the DAC array and one of the S/H arrays. As shown in Fig. 4.9, the switches are implemented based on logic gate because the switches only switch between *VDD* and *GND* under rail-to-rail operation. S/H array is gated by clock gating signal *SAMP* to enable or disable its switching. Detail transition is shown in Table 4.2 Both S/H and DAC arrays are designed to settle within half a clock cycle. Based on Eq. (3.5), all the switches are sized by considering the settling time of a logic gate driving a capacitive load. To achieve 8-bit resolution and 240-kS/s total sampling rate for 8 channels, τ_{array} is set to be less than 37 ns.

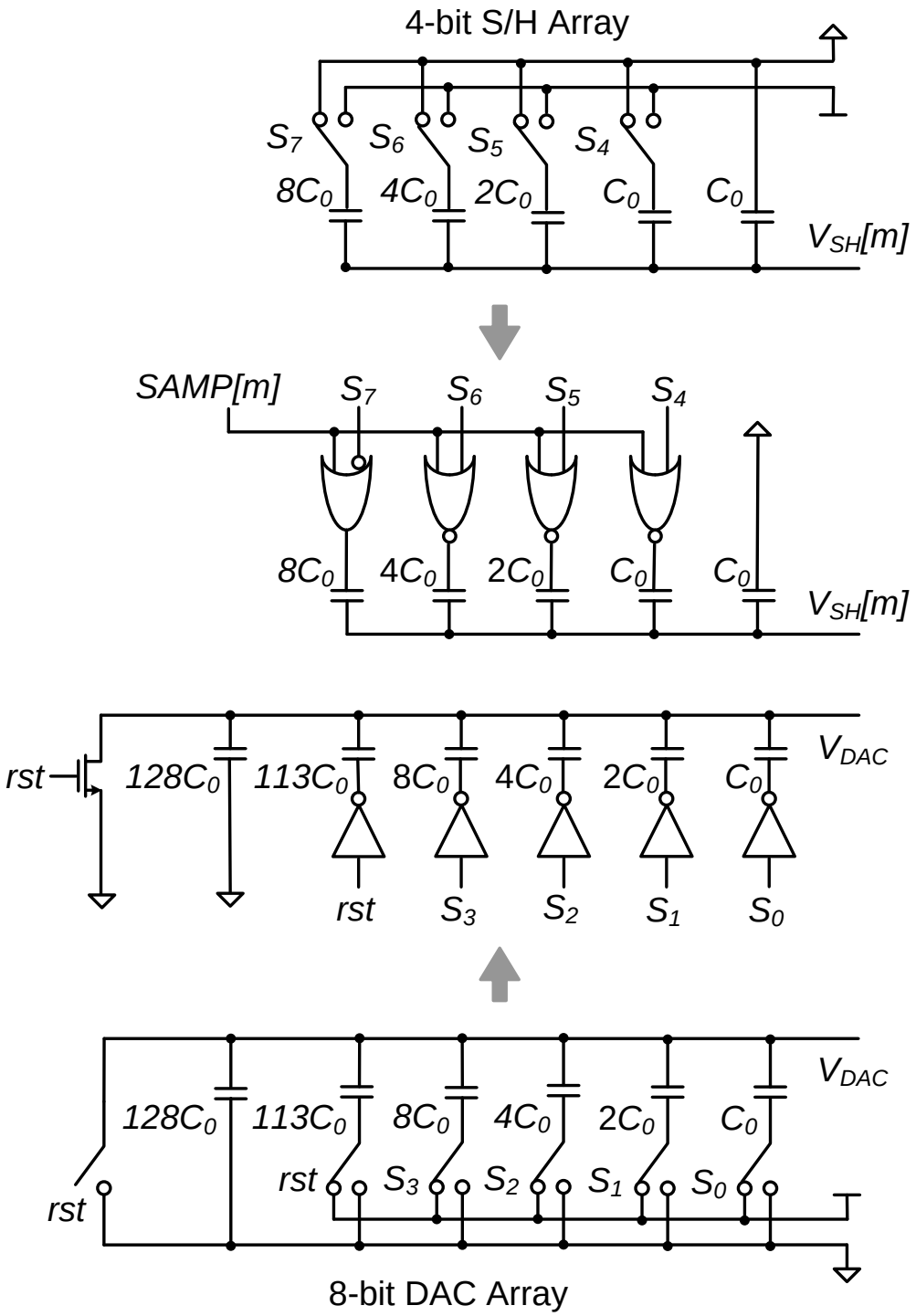

Fig. 4.9. Switches for capacitive arrays with clock-gated S/H array.

4.3.3 Dynamic Latch Comparator

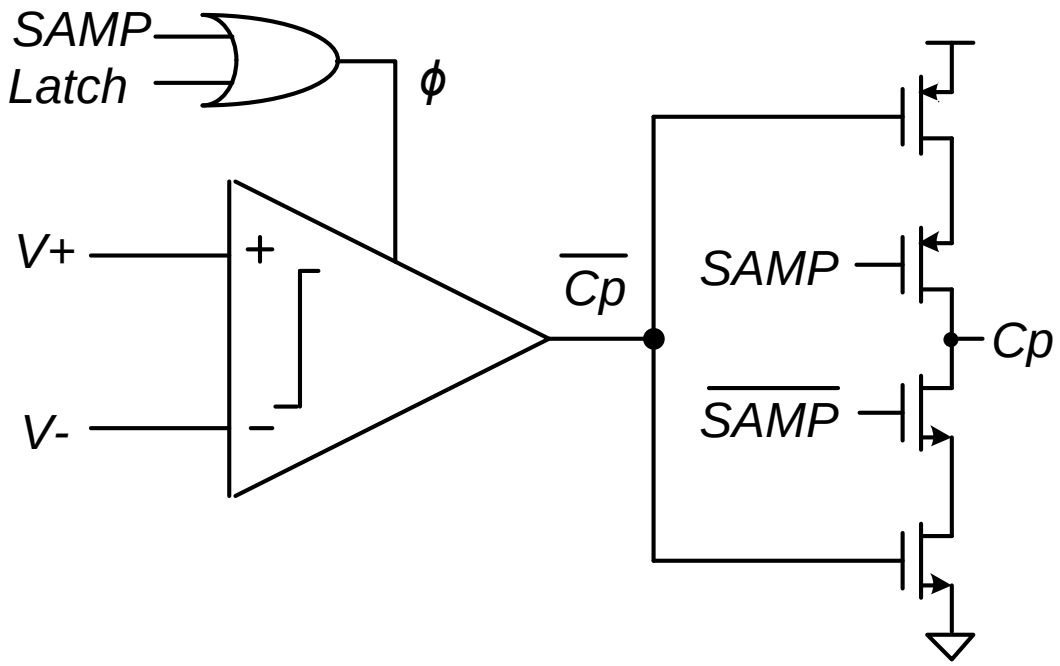

Fig. 4.10. Schematic of the clock-gated dynamic comparator.

The simplified schematic for the dynamic comparator is shown in Fig. 4.10. I use the same implementation for the comparator (see Fig. 3.11) but additional *OR* gate is used to clock-gate the comparator clock. Clocked inverter is introduced at the output to realize the digital multiplexing.

Non-inverting comparator input, *V*+, is connected to the independent S/H array while the inverting input, *V*−, is connected to the shared DAC array. According to Eq. (3.3), the required common-mode input range is 0.26 V to 0.3 V for a 0.6-V supply operation. This is achieved using NMOS input pair. The input pair, M1 and M2, has a common-mode input range of 0.17 V to 0.6 V based on simulation, satisfying the given specification. Additionally, their W/L ratio is designed to be 100 times to obtain

a comparator bandwidth of about 50 MHz so that the ADC conversion rate is not constrained by the speed of the comparator.

4.3.4 Successive Approximation Register (SAR) with Ring Counter

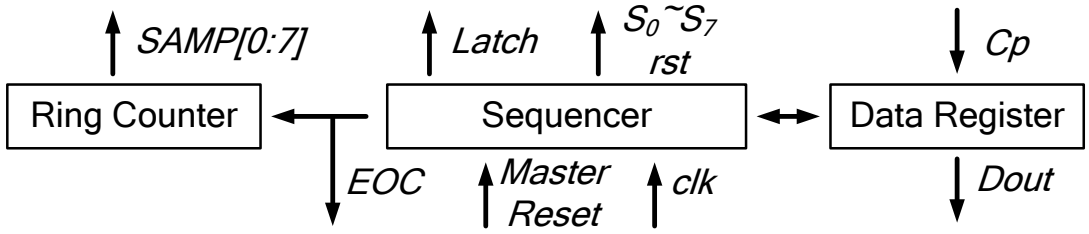

Fig. 4.11. Simplified diagram of the SAR logic with ring counter.

The SAR, as depicted in Fig. 4.11, is a finite state machine that produces the control signals based on successive approximation algorithm to control and synchronize the ADC operation. It was synthesized from a VERILOG description based on the state transition described in Table 4.2. It consists of data register and bit-cycling sequencer which resemble those in conventional design. An additional ring counter is added to toggle AD conversion among the 8 channels. S/H array switching signal, S_4-S_7, and comparator latching signal, *Latch*, generated by sequencer are connected to all S/H arrays and comparators of different channels. However, only one channel is active for conversion based on the clock-gating signal, *SAMP*, generated through ring counter. When *SAMP* = "1", the respective channel is performing sampling. In contrast, the channel is active for conversion if *SAMP* = "0". During successive approximation, the sequencer performs bit-cycling on both S/H array (using S_4-S_7) and DAC array (using S_0-S_3) according to the comparison result from comparator to produce the digital

output code, from MSB to LSB. At the end of each conversion, *EOC* signal is asserted and the conversion continues on subsequent channel.

4.4 Chip Verification and Measurement Results

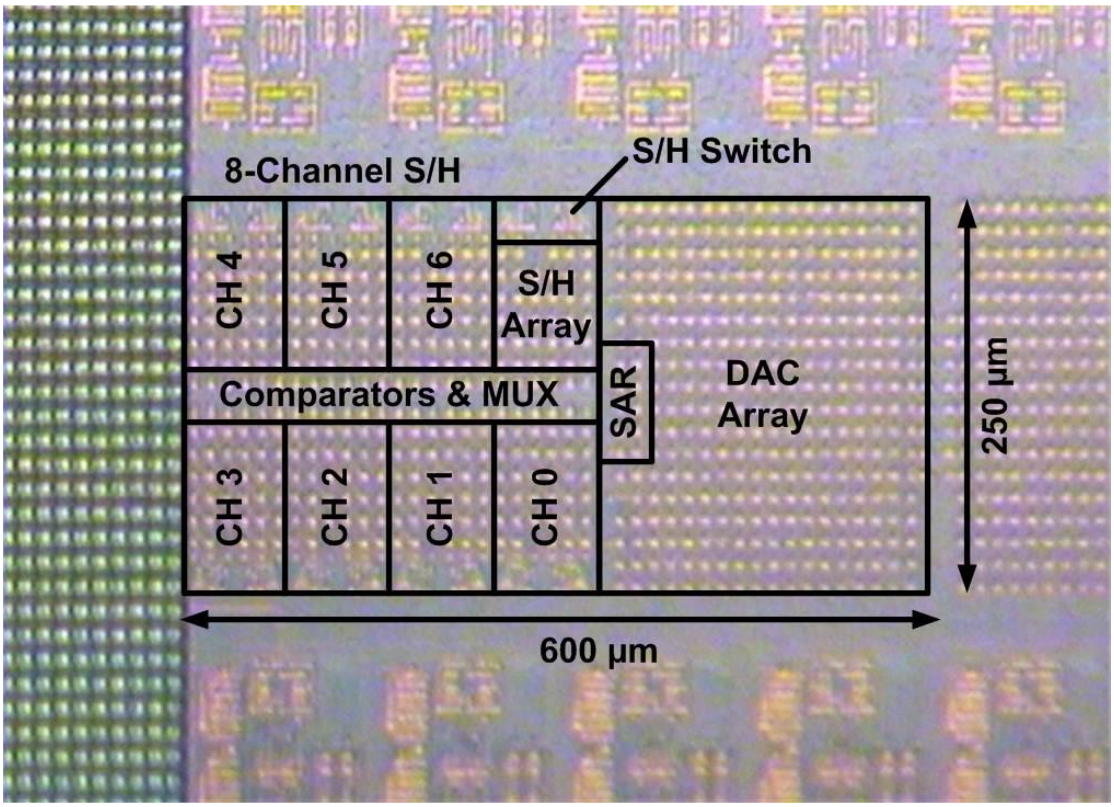

Fig. 4.12. Die photo of the 8-channel ADC.

The 8-bit 8-channel ADC prototype was fabricated in a 0.13-µm single-poly eight-metal (1P8M) CMOS process without using any high-V_t or low-V_t devices. It was packaged as low profile quad flat pack (LQFP). The core occupies a silicon area of 600 µm × 250 µm. Fig. 4.12 shows the die photo of the ADC prototype.

For all measurement, Agilent 33250A Function/Arbitrary Waveform Generator was used to generate various test signals and ADC clock. Agilent 167802A Logic

Analyzer was used to collect the ADC output. Yokogawa 7651 Programmable DC Source was used as the single supply voltage.

At 25 ℃, the 8-channel ADC dissipates 1.23 μW from a 0.6-V supply at 30-kS/s-per-channel sampling rate. The capacitive arrays dissipate 645 nW while the SAR logic, comparators, and S/H switches consume 585 nW. Table 4.3 lists the measured performance for all channels with mean value and standard deviation calculated. Form Table 4.3, all channels actually achieve similar performance. The following sections discuss the measurement results in detail.

Table 4.3 Measured performances for all channels at 0.6-V supply and 30-kS/s-per-channel.

Channel	DNL (LSB)		INL (LSB)		SNDR (dB)	SFDR (dB)	ENOB (bit)	FOM (fJ/Conversion-step)
0	-0.74	0.23	-0.62	0.51	46.77	63.92	7.48	28.79
1	-0.44	0.19	-0.32	0.34	47.91	67.76	7.67	25.24
2	-0.84	0.26	-0.59	0.55	46.92	62.62	7.50	28.27
3	-0.34	0.15	-0.28	0.14	48.01	71.55	7.68	24.95
4	-0.22	0.19	-0.22	0.36	47.99	65.15	7.68	24.99
5	-0.17	0.19	-0.18	0.31	47.87	68.63	7.66	25.34
6	-0.73	0.23	-0.54	0.57	47.39	65.21	7.58	26.80
7	-0.72	0.21	-0.51	0.43	46.77	61.84	7.48	28.78
Mean	-0.52	0.21	-0.41	0.40	47.45	65.83	7.59	26.64
Std.	0.27	0.04	0.18	0.15	0.56	3.27	0.09	1.74

4.4.1 Static Performance

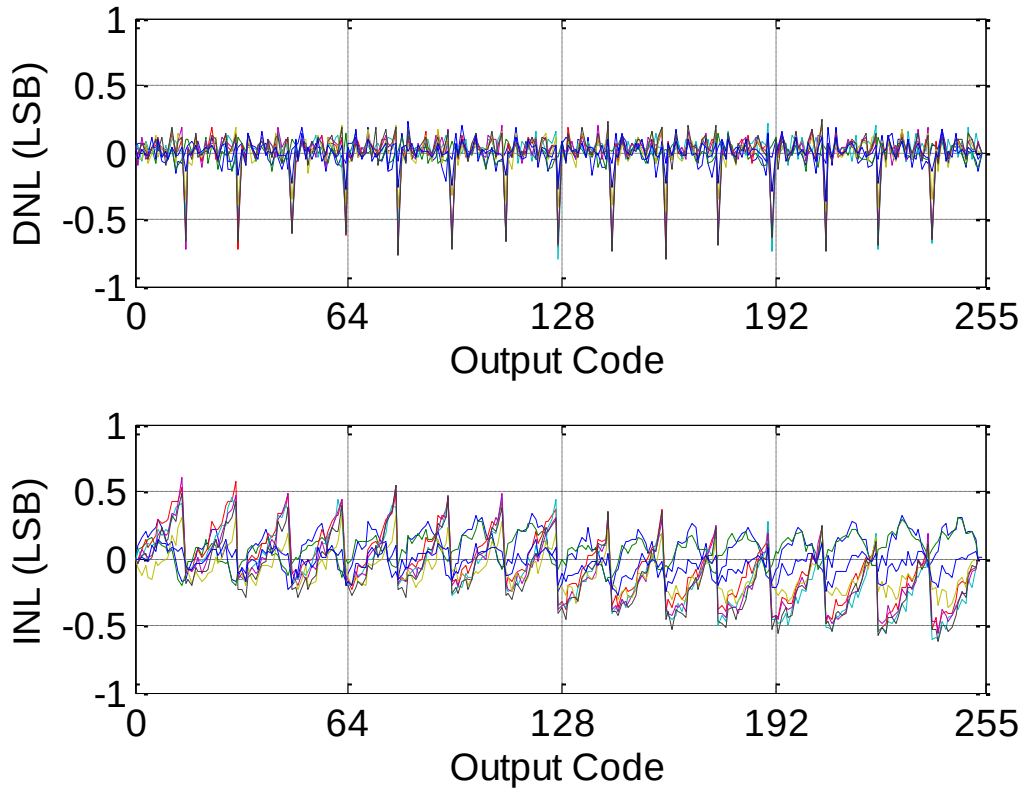

Fig. 4.13. Measured ADC DNL and INL for all channels.

The static linearity test is conducted using a 5 Hz full-swing triangular input. Fig. 4.13 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) for all channels with respect to the output code. The mean DNL is in the range of −0.52/+0.21 LSB, while the mean INL is in the range of −0.41/+0.40 LSB.

4.4.2 Dynamic Performance

Fig. 4.14 depicts one of the measured ADC output spectral density plots with rail-to-rail 1-kHz sine wave input for all channels. Fig. 4.15 plots the measured mean SNDR and SFDR versus input signal frequency. The mean SNDR is relatively constant across the entire ADC Nyquist bandwidth. Fig. 4.16 shows the measured mean SNDR and SFDR versus input stimulus, which proves that the ADC achieves rail-to-rail input range. The peak SNDR and SFDR are 47.45 dB and 65.83 dB, respectively. This translates to an effective number of bits (ENOB) of 7.59 bits and figure of merit (FOM) of 26.6 fJ/conversion-step according to Eq. (3.6) and (3.7).

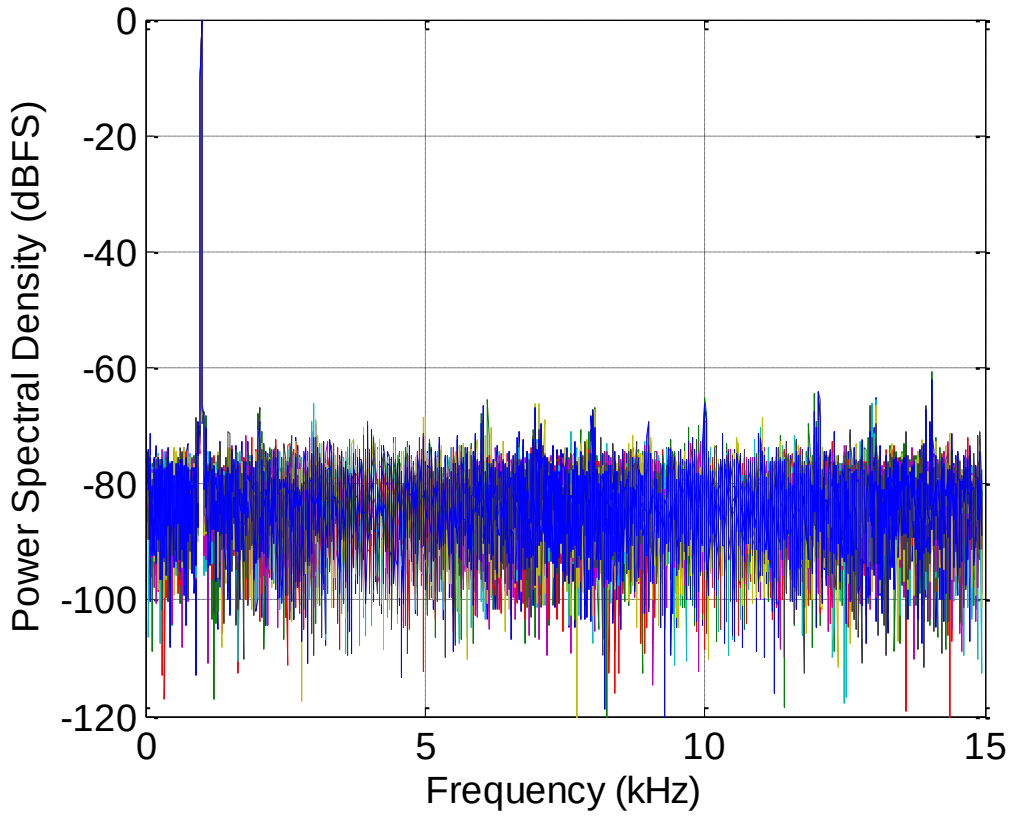

Fig. 4.14. Measured PSD for all channels with 1-kHz rail-to-rail sine wave.

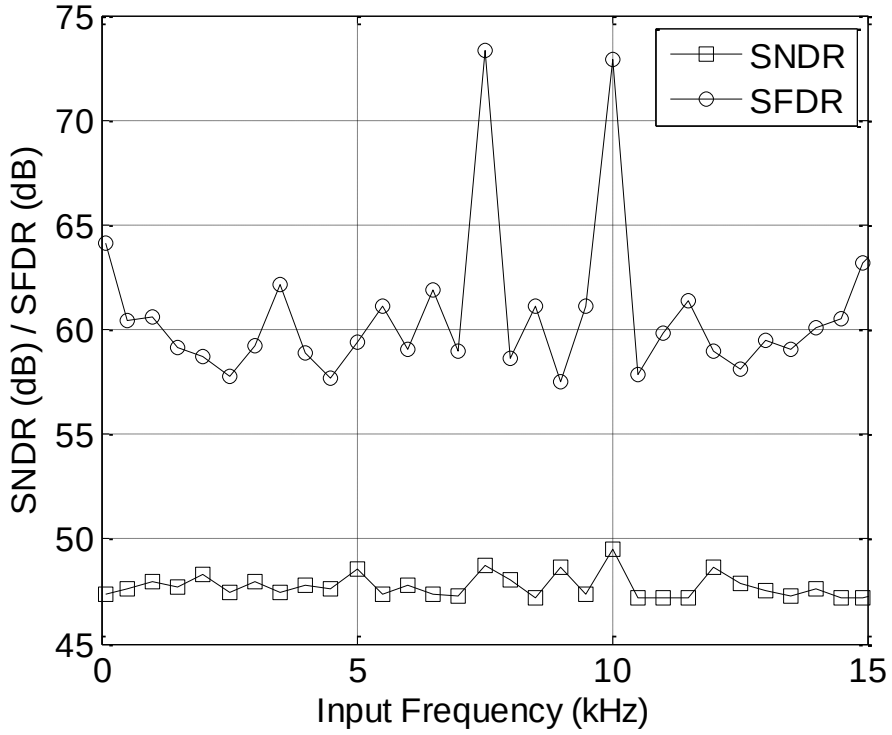

Fig. 4.15. Measured mean SNDR and SFDR versus input signal frequency.

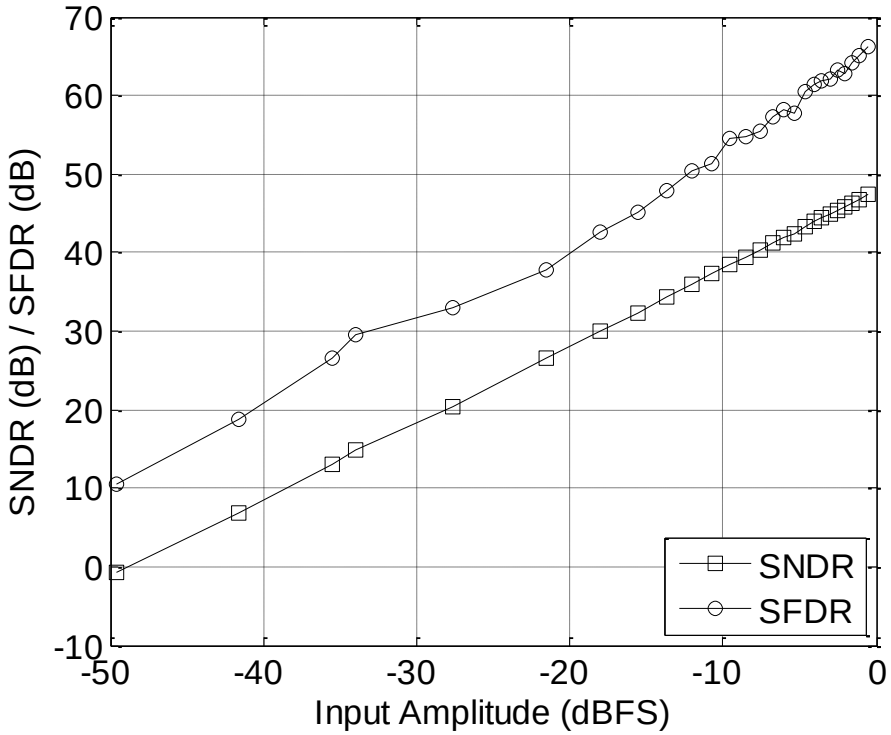

Fig. 4.16. Measured mean SNDR and SFDR versus input signal amplitude.

4.4.3 Sampling Rate Scalability

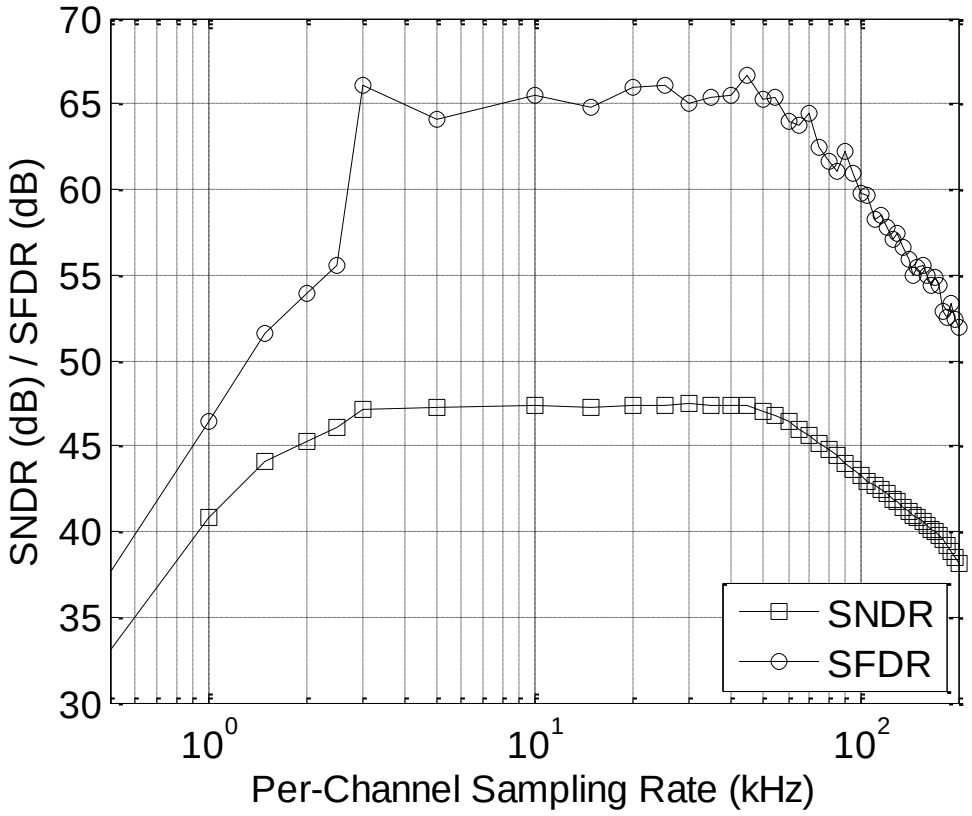

Fig. 4.17. Measured ADC SNDR and SFDR versus per-channel sampling rate.

Fig. 4.17 shows the measured ADC mean SNDR and SFDR versus per-channel sampling rate. The ADC sampling rate was changed by selecting different input clock frequencies. From Fig. 4.17, the ADC maintains its accuracy with scalable sampling rate of 3 kS/s to 50 kS/s, which make the ADC suitable for various biomedical sensor interface applications. With sampling rate below 3 kS/s, leakage current through S/H switch becomes more significant due to lengthen holding phase. This results in degradation in SNDR and SFDR. At sampling rate above 50 kS/s, the ADC performance drops abruptly because of incomplete capacitive array settling.

4.4.4 Supply Voltage Range

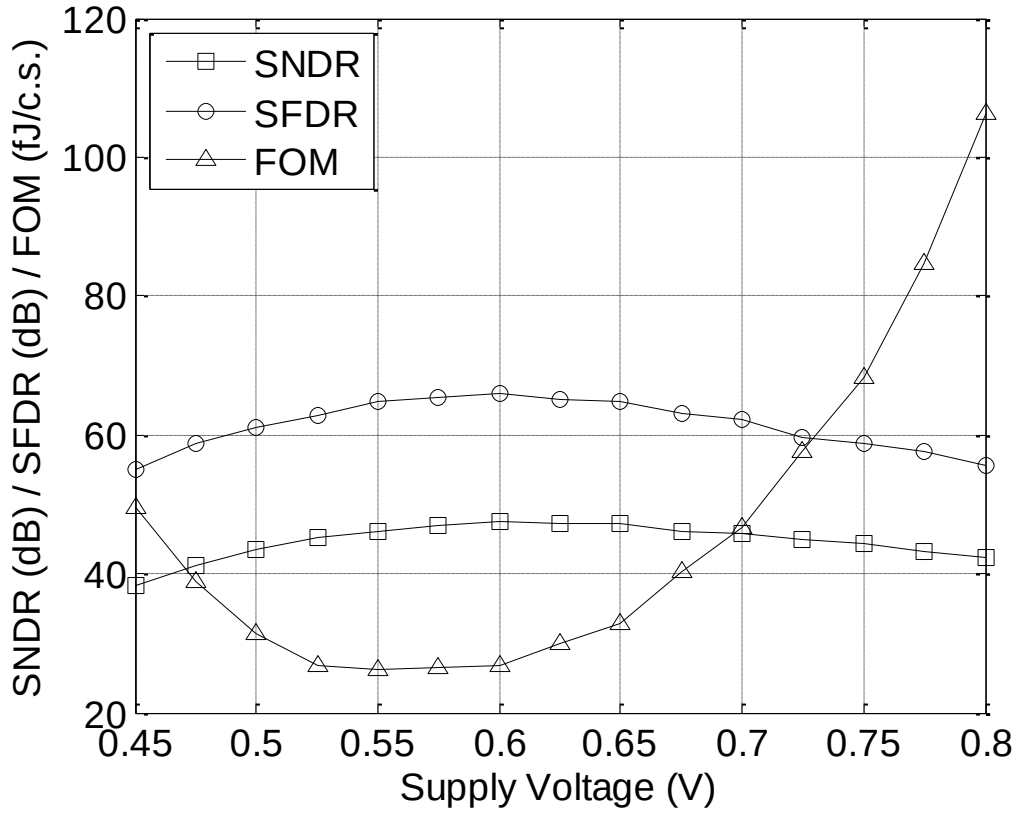

Fig. 4.18. Measured ADC SNDR, SFDR, and FOM versus supply voltage.

At 30 kS/s-per-channel sampling rate, the measured ADC SNDR, SFDR, and FOM versus supply voltage are shown in Fig. 4.18. The ADC operates robustly with ENOB above 7 bits (44-dB SNDR) under 0.5-V to 0.75-V supply. Since the proposed ADC architecture is fully dynamic, it is expected that the power dissipation increases exponentially with respect to supply voltage. This is shown by the exponential increment in FOM for supply voltage higher than 0.6 V. On the other hand, degrading SNDR also contributes to the increment in FOM at both ends. Lastly, FOM below 30 fJ/conversion-step is achieved when the ADC is operating near sub-threshold region with 0.5-V to 0.625-V supply.

4.4.5 Operating Temperature Variation

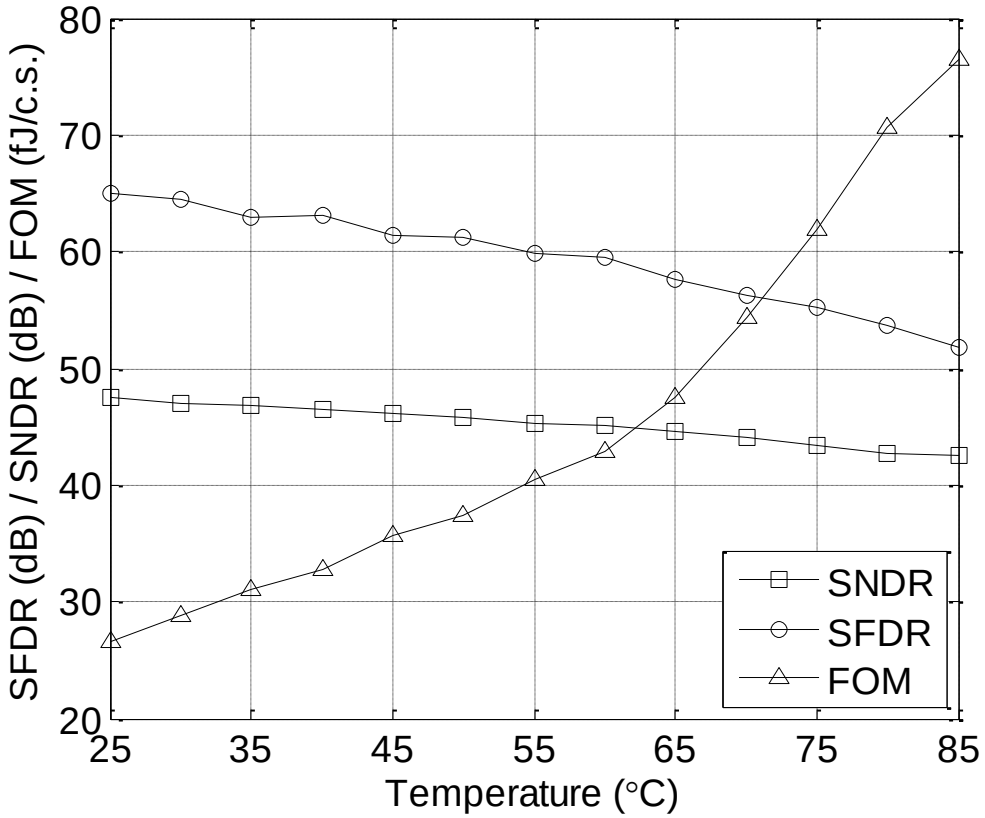

Fig. 4.19. Measured ADC SNDR, SFDR, and FOM versus operating temperature.

The ADC was also tested from 25℃ to 85℃. This is to ensure that the ADC is functioning over a wide temperature range. For example, as an integral part of an implantable device for human the ADC must be operational at 37.5℃, which is the nominal human body temperature. Fig. 4.19 shows the measured SNDR, SFDR, and FOM versus operating temperature. At higher temperature, larger leakage current through S/H switch during conversion affects the ADC accuracy. Both SNDR and SFDR are decreasing when temperature increases. In addition, leakage current from digital circuit starts to dominate at temperature higher than 60℃ and increases accordingly afterward. This causes the FOM to degrade abruptly. Nonetheless, the

ADC attains more than 44 dB SNDR (7-bit ENOB) for operating temperature from 25 ℃ to 70 ℃.

4.4.6 Summary and Comparison

Table 4.4 summarizes the ADC performances. Table 4.5 compares the proposed ADC with other state-of-the-art sub-1V SA ADC designs suitable for different biomedical sensor interface application with sufficient sampling rate and resolution. The proposed ADC achieves comparable performance and FOM among the designs. Nonetheless, the proposed ADC is the first one to demonstrate the implementation of a multi-channel ADC under low-voltage supply.

Table 4.4 Performance summary of the 8-channel ADC.

Technology	0.13 μm CMOS
Core area (mm^2)	0.15
Typical performances	
Supply (V)	0.6
Number of channel	8
Per-channel sampling rate (kS/s)	30
Total sampling rate (kS/s)	240
Input swing	Rail-to-rail
DNL (LSB)	-0.52 / 0.21
INL (LSB)	-0.41 / 0.40
SNDR (dB)	47.45
SFDR (dB)	65.83
ENOB (bit)	7.59
Power dissipation (μW)	1.23
FOM (fJ/conversion-step)	26.64
Additional performances	
Supply range (V)	0.5-0.75
Scalable per-channel sampling rate (kS/s)	3-50
Operating temperature (℃)	25-70

Table 4.5 Comparison with state-of-the-art sub-1 V SA ADC designs.

Ref.	Sauerbrey'03 [33]	Hong'07 [34]	Yip'11 [37]	Lee'11 [49]	Chang'11 [50]	This work
Technology	0.18 µm	0.18 µm	65 nm	0.18 µm	0.25 µm	0.13 µm
Supply (V)	0.6	0.9	0.55	0.6	0.5	0.6
Number of channel	1	1	1	1	1	8
Total sampling rate (kS/s)	34	200	20	100	31.25	240
ENOB (bit)	7.43	7.58	8.84	9.30	7.21	7.59
Power dissipation (µW)	3.12	2.47	0.21	1.3	0.087	1.23
FOM (fJ/conversion-step)	532	65	22.4	21	20	26.64

4.5 Practical Application – Neural Recording Interface

4.5.1 16-Channel Neural Recording Interface

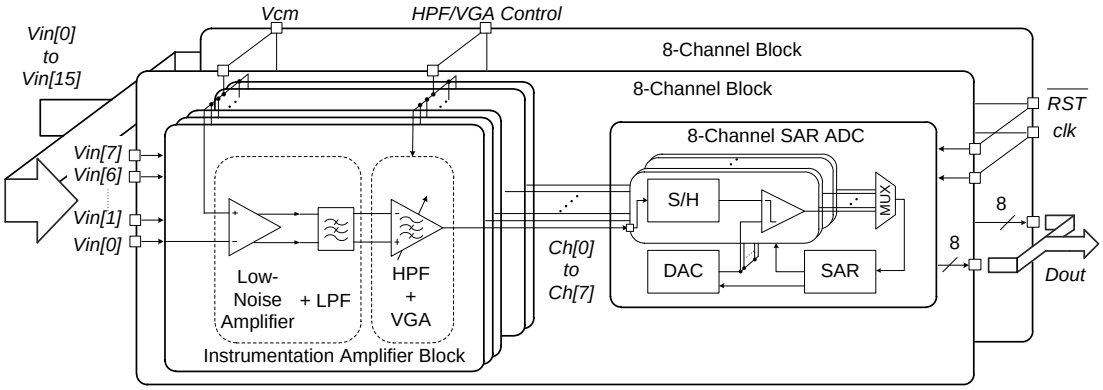

Fig. 4.20. System block diagram of the 16-channel neural recording interface.

The proposed multi-channel SA ADC was used to implement a 16-channel neural recording interface [13]. The system block diagram of the neural recording interface is shown in Fig. 4.20. An 8-channel block is employed as the building block to form a

larger multi-channel recording array. A 16-channel neural recording interface based on two 8-channel blocks is demonstrated. Each 8-channel block consists of eight instrumentation amplifier (IA) and an 8-channel SA ADC. The IA is divided into two cascaded stages. The first stage is a fully differential low-noise amplifier with fixed low-pass filter. The second stage provides programmable high-pass corner frequency, variable gain as well as driving the ADC input. The detailed circuits for the amplifiers are described in [19]. Fig. 4.21 shows the die photo of the 16-channel recording interface.

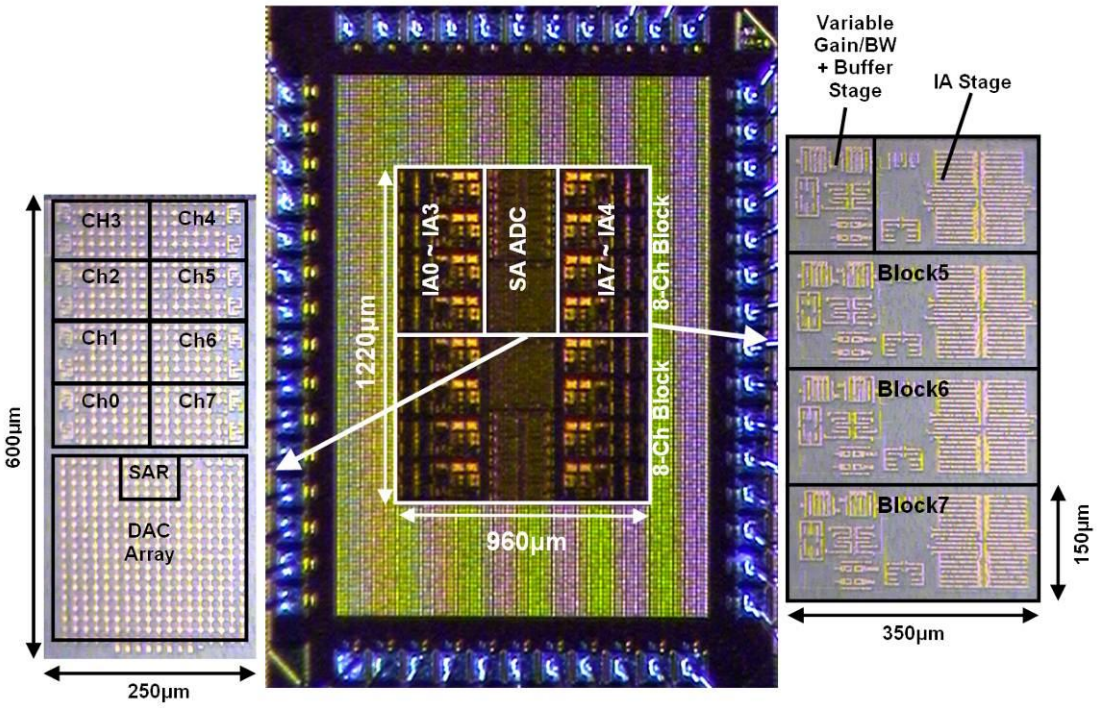

Fig. 4.21. Die photo of the 16-channel recording interface prototype. Insets show the 8-channel SA ADC (left) and the IA block (right).

The recording interface was first tested using arbitrary input signals with different frequency and amplitude, for example sine wave, triangular wave, and cardiac signal generated from signal sources. Fig. 4.22 plots the recorded 8-channel output. The proposed multi-channel design is functioning well.

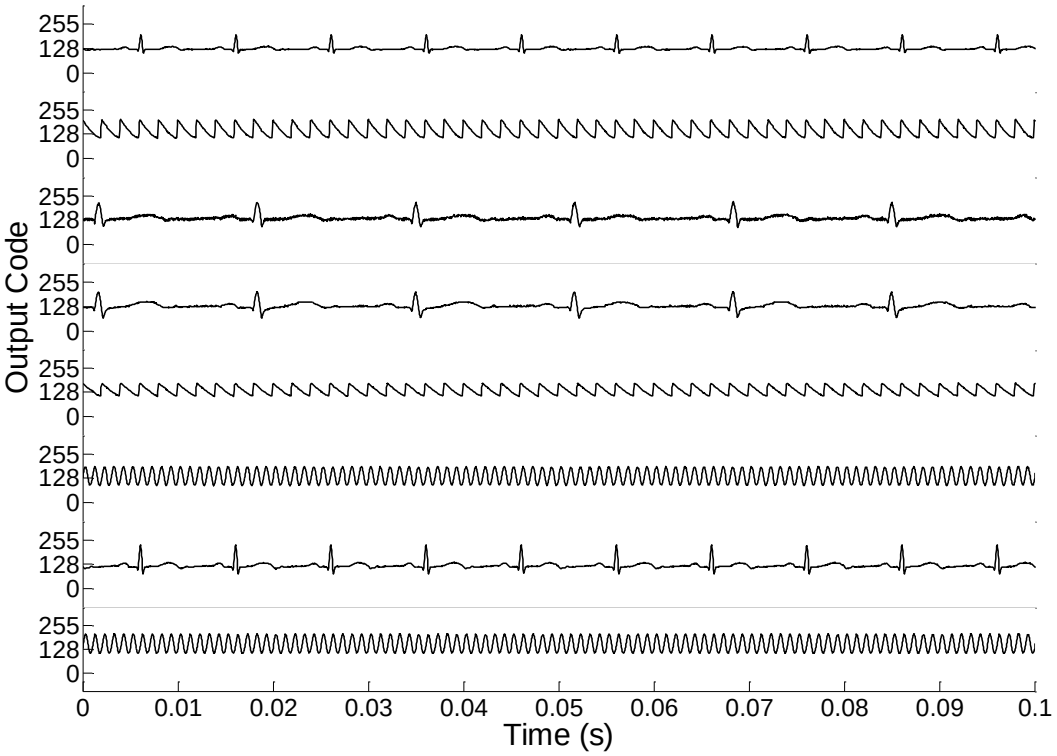

Fig. 4.22. Preliminary test on the recording interface using arbitrary inputs.

4.5.2 In-Vivo Test

In-vivo test on neural recording was carried out using the proposed recording interface[2]. The test was performed at nucleus incertus in the caudal part of an awake and free-moving male Sprague-Dawley rat. Fig. 4.23 shows one of the single-channel recordings. The measurement shows good recording quality in which both single and continuous neural spike firings are clearly recorded. An 8-channel *in-vivo* recording is as depicted in Fig. 4.24, showing neural spike trains across different channels.

[2] The author would like to thank Dr. Gavin Dawe and Dr. Rajkumar Ramamoorthy at Center for Life Sciences for their helps in performing the neural recording.

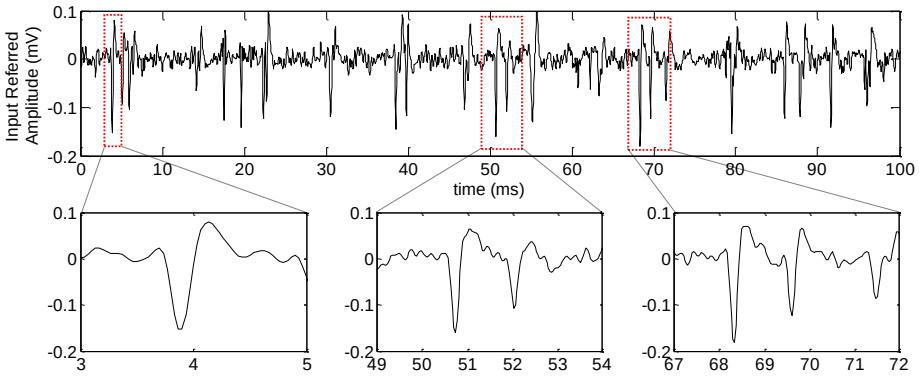

Fig. 4.23. A single-channel *in-vivo* recording: input referred waveform (top), single neural spike (bottom left), and double neural spike (bottom middle and bottom right).

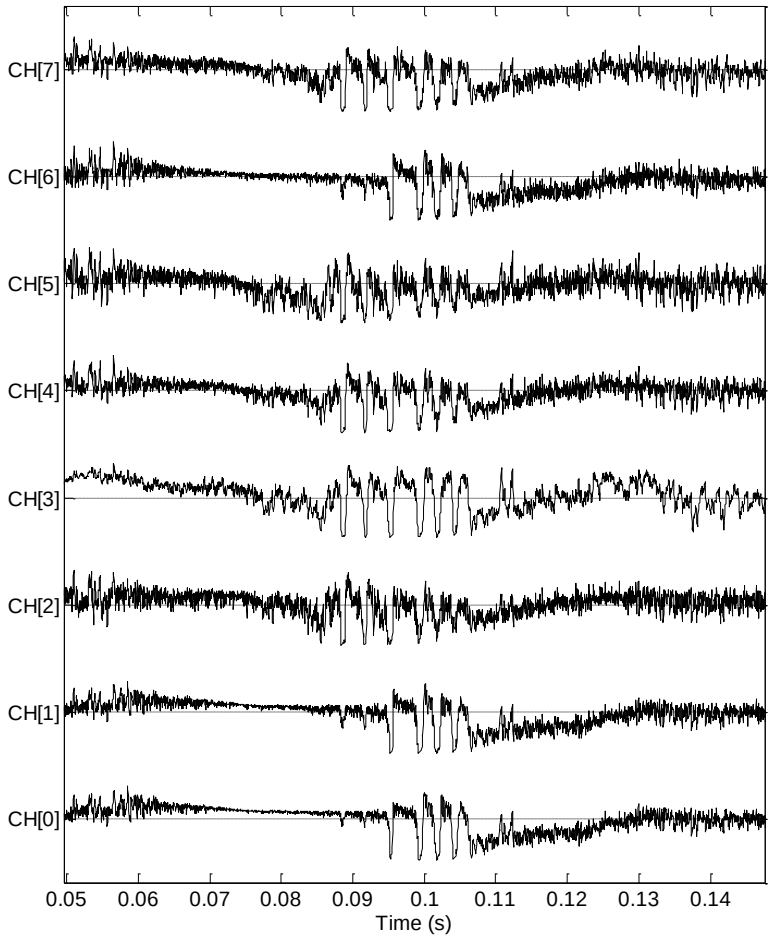

Fig. 4.24. An 8-channel *in-vivo* recording showing multi neural spike train across different channels.

CHAPTER 5

CONCLUSION

The main contributions of this research works are in the design of low-voltage high efficiency ADC dedicated for biomedical sensor interface and the practical application based on the proposed ADC design.

Firstly, the conventional ADC design for biomedical recording interface is reviewed. The state-of-the-art ADC designs are included and several techniques to improve energy efficiency have been investigated.

Secondly, an energy-efficient dual-capacitive-array architecture for SA ADC is proposed. Unlike conventional topologies, the proposed architecture utilizes two capacitive arrays for quantization in order to reduce the switching energy in capacitive array. Additionally, the proposed ADC is a fully dynamic ADC with rail-to-rail input range without the use of a rail-to-rail comparator. The ADC is optimized for low power dissipation while maintaining its accuracy. A 10-bit 10-kS/s ADC prototype fabricated in a standard 0.35-µm CMOS technology achieves an ENOB of 9.07 bits at full input swing while dissipating 170 nW from a 0.8-V supply. This translates to a FOM of 32 fJ/conversion-step.

Thirdly, a digital multiplexing scheme for the design of multi-channel biomedical recording interface using time-interleaved S/H stage is presented. An 8-channel SA ADC based on dual-capacitive-array is introduced to facilitate multiplexing among channels and thus eliminates the need for analog multiplexer and associated buffers. The proposed 8-channel ADC was fabricated in a standard 0.13-µm CMOS

technology with an active area of 0.15 mm^2. It consumes 1.23 µW from a 0.6-V supply. At per-channel sampling rate of 30 kS/s, the proposed design achieves a mean ENOB of 7.59 bits, which can be translated into a FOM of 26.6 fJ/conversion-step.

Lastly, examples on practical implementation for both proposed designs have been provided and discussed. A clinical EEG recording utilizing the proposed dual-capacitive-array SA ADC design shows promising result. On the other hand, a 16-channel neural recording interface based on the proposed multi-channel ADC demonstrates good recording quality on neural spike signal.

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