FABRICATION AND CHARACTERIZATION OF ADVANCED AlGaN/GaN HIGH-ELECTRON-MOBILITY TRANSISTORS

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DECLARATION

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

LIU XINKE

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Abstract

Fabrication and Characterization of Advanced AlGaN/GaN

High-Electron-Mobility Transistors

by

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AlGaN/GaN high electron mobility transistors (HEMT) have become a very promising candidate for the next generation high voltage electronic devices, mainly due to the superior material properties of GaN. Especially, the growth of GaN-on-silicon wafers with large diameters of 6 inches and 8 inches was demonstrated, which can enable the cost-effective fabrication of GaN power devices. This thesis focuses to explore the application of AlGaN/GaN HEMTs for the power devices beyond the silicon-based transistors.

To take full advantage of AlGaN/GaN HEMTs, a gate dielectric process technology that provides good interfacial properties is required. In this thesis, an effective and highly manufacturable passivation technology based on a multi-chamber metal-organic chemical vapor deposition (MOCVD) gate cluster system was demonstrated. The key characteristics of the novel *in situ* passivation using vacuum anneal and silane (SiH_4) treatment were determined and identified. AlGaN/GaN metal-oxide-semiconductor HEMTs (MOS-HEMTs) with *in situ* vacuum anneal and SiH_4 treatment exhibit good electrical characteristics.

Further enhancement of AlGaN/GaN MOS-HEMTs by integration of a highly compressive stress liner was also investigated. This work explored a novel highly compressive diamond-like-carbon (DLC) stress liner to induce non-uniform stress along the channel of the AlGaN/GaN MOS-HEMTs. It was found that the compressive stress was induced by the DLC stress liner in the channel under the gate stack, thus reducing the polarization charge by piezoelectric polarization; a tensile stress was induced in the source/drain access regions between the gate and the source/drain (S/D) contacts, thus leading to an increase of the polarization charge and a reduction of source/drain series resistance.

To enable cost-effective GaN power devices in the silicon complementary metal-oxide-semiconductor (CMOS) foundry, a CMOS compatible gold-free process is essential. Both high breakdown voltage AlGaN/GaN-on-silicon and -on-sapphire MOS-HEMTs were realized using a CMOS compatible gold-free process, where CMOS compatible ohmic contacts and gate stack were adopted. In this work, AlGaN/GaN-on-sapphire MOS-HEMTs achieved the highest breakdown V_{BR} of 1400 V, as compared to other gold-free AlGaN/GaN HEMTs reported to date.

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List of Symbols

Symbol	Description	Unit
E_G	Bandgap	eV
ε_r	Dielectric constant	
ξ_{br}	Breakdown field	MV/cm
v_p	High-field peak electron velocity	cm/s
μ_n	Electron mobility	$cm^2/V{\cdot}s$
K	Thermal conductivity	$WK^{-1}cm^{-1}$
P_{PE}	Piezoelectric polarization charge	C/m^2
P_{SP}	Spontaneous polarization charge	C/m^2
σ	Polarization charge density	C/m^2
$e_{31,}\ e_{33}$	Piezoelectric constant	C/m^2
$C_{13},\ C_{33}$	Elastic constant	GPa
a	Lattice constant	Å
n_s	Density of 2-dimensional electron gas	cm^{-2}
d	Thickness of the AlGaN barrier layer	nm
q	Electronic charge	C
ϕ_b	Schottky barrier height	V
E_F	Fermi level	eV
ΔEc	Conduction band offset	eV
V_{BR}	Breakdown voltage	V
R_{on}	On-state resistance	$\Omega{\cdot}cm^2$
ξ_P	Vertical polarization field	V/cm
$\xi_{br,AlGaN}$	Breakdown field of the AlGaN layer	MV/cm
L_{GD}	Gate-to-drain spacing	μm
J_G	Gate leakage current density	A/cm^2
D_{it}	Interface state density	$cm^{-2}\ eV^{-1}$
V_{th}	Threshold voltage	V
S	Sub-threshold swing	mV/decade
I_G	Gate leakage current	A/mm
ΔV_{FB}	Flatband voltage shift	V
C	Capacitance	F
E_C	Conduction band edge	eV
E_V	Valence band edge	eV
G	Conductance	S

τ_e	Characteristic emission time	s
E_t	Trap energy	eV
k	Boltzmann constant	eVK^{-1}
T	Temperature	K
v_{th}	Thermal velocity	cm/s
N	Density of states in the majority carrier band	cm^{-2}
σ_{cro}	Capture cross section of the trap state	cm^2
f_{res}	Characteristic response frequency	Hz
C_{ox}	Gate oxide capacitance	F
C_d	Depletion capacitance	F
C_{it}	Capacitance of interface states	F
R_{it}	Resistance of interface states	Ω
G_m	Measured conductance	S
C_m	Measured capacitance	F
R_{ser}	Series resistance	Ω
C_{ma}	Measured accumulation capacitance	F
G_{ma}	Measured accumulation conductance	S
G_c	Corrected conductance	S
C_c	Corrected capacitance	F
f	Measurement frequency	Hz
C_p	Parallel capacitance	F
R_p	Parallel resistance	Ω
G_p	Parallel conductance	S
L_{GS}	Gate-to-drain spacing	µm
L_G	Gate length	µm
I_{off}	Off-state current (per unit width)	A/mm
I_{on}	On-state current (per unit width)	A/mm
g_m	transconductance	S
V_D	Drain voltage	V
g_m	Measured extrinsic transconductance	S
$g_{m,i}$	Intrinsic transconductance	S
$g_{m,max}$	Measured extrinsic peak transconductance	S
$g_{m,i,max}$	Intrinsic peak transconductance	S
R_S	Parasitic source resistance	Ω·mm
$R_{S/D}$	Parasitic source/drain series resistance	Ω·mm
$R_{Channel}$	Channel resistance	Ω·mm
σ_{xx}	Lateral stress	GPa

t_1	AlGaN barrier layer thickness	nm
t_2	Gate oxide thickness	nm
d	Contact spacing	μm
R_{sh}	Sheet resistance	Ω/square
ρ_c	Specific contact resistivity	$\Omega \cdot cm^2$

List of Abbreviations

Abbreviation	Description
BFOM	Baliga's figure of merit
2-DEG	Two-dimensional electron gas
HEMTs	High-electron-mobility tansistors
IT	Information technology
PV	Photovoltaic
EV	Electric Vehicles
HEV	Hybrid electric vehicles
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
CMOS	Complementary metal-oxide-semiconductor
MOCVD	Metal-organic chemical vapor deposition
I_{on}/I_{off}	Current on/off ratio
JVD	Jet vapor deposition
BCB	Benzocyclobutene
PDA	Post-deposition anneal
XPS	X-ray photoelectron spectroscopy
TEM	Transmission electron microscopy
C-V	Capacitance-voltage
PM 1	Process module 1
PM 2	Process module 2
PM 3	Process module 3

Chapter 1

Introduction

1.1 Overview of Gallium Nitride

1.1.1 Gallium Nitride Material and Potential Applications

Over the past three decades, enormous progress has been made on the development of gallium nitride (GaN) and its family of alloys (InAlGaN) for both electronic and optoelectronic applications [1]-[3]. GaN possesses a large bandgap of 3.4 eV, a very high breakdown field of 3.3×10^6 V/cm, an extremely high-field peak electron velocity (3×10^7 cm/s) and saturation electron velocity (1.5×10^7 cm/s) [4]. These GaN properties together with the combination of a large conduction band offset and a high electron mobility of the AlGaN/GaN heterostructure, make the GaN-based transistor an excellent candidate for the application in electronic devices operating at high temperature, high power, and high frequency [5]-[6], even in a harsh environment, due to the chemical inertness of GaN [7].

Silicon has long been the dominant semiconductor for power devices. However, the electrical performance of silicon-based devices is approaching the theoretical limit. As a result, wide bandgap materials, such as GaN, have attracted significant attention, because they offer numerous advantages over other materials. To further describe the advantages of GaN in high temperature and high power electronic devices, the material properties of GaN and its competing materials are presented in Table 1.1 [5]. As shown in

Table 1.1. Comparison of material properties of Si, GaAs, 4H-SiC, and GaN at 300 K. BFOM is Baliga's figure of merit for power transistor performance ($\mu_n.\varepsilon_r.E_G^3$), and the benchmark is Si [5].

Material	Si	GaAs	4H-SiC	GaN
Bandgap E_G (eV)	1.12	1.42	3.2	3.4
Dielectric Constant ε_r	11.9	12.5	10	9.5
Breakdown Field ξ_{br} (MV/cm)	0.3	0.4	3.0	3.3
High-field Peak Electron Velocity v_p ($\times 10^7$ cm/s)	1.0	2.0	2.0	3.0
Electron Moblity μ_n ($cm^2/V \cdot s$)	1300	5000	260	1500
Thermal Conductivity K ($WK^{-1}cm^{-1}$)	1.5	0.5	4.9	1.3
BFOM Ratio	1.0	9.6	3.1	24.6

Table 1.1, the value of the Baliga's figure of merit (BFOM) for GaN normalized to that of Si is higher than those of all the other materials. For the high power and high voltage power devices, large bandgap E_G, high breakdown field ξ_{br}, high thermal conductivity K, and high electron mobility μ_n are essential requirements. As compared with other materials, GaN has a larger E_G and a higher $\xi_{br,}$ which means that GaN-based transistors can achieve a higher breakdown voltage for high-voltage switching devices. The high-field peak electron velocity v_p and high electron mobility μ_n of the two-dimensional electron gas (2-DEG) in AlGaN/GaN heterostructures allow the AlGaN/GaN high-electron-mobility transistors (HEMTs) to have a low on-state resistance and to operate at high switching frequencies. The large polarization charge in the GaN-based materials can lead to a high output current for AlGaN/GaN or InAlN/GaN HEMTs, thus making GaN-based HEMTs very promising candidates for high power devices. The large E_G and

thus low intrinsic carrier concentration, together with the intermediate thermal conductivity, all benefit to the high temperature operation of GaN transistors.

Fig. 1.1 illustrates the potential applications of GaN-based power devices. There are three major categories, in which GaN-based devices can compete with the existing or new technologies [6], [8]. In the lower supply voltage range, such as information technology (IT) and consumer electronics, traditional silicon devices currently take almost all the markets due to their low cost and good reliability. GaN market players in the low voltage range, such as International Rectifier and Efficient Power Conversion, are bringing their GaN products into this market (source: http://www.irf.com/ and http://www.epc-co.com/). In the high supply voltage range, such as motor drives and the power inverters for photovoltaic (PV) cell or uninterruptible power supplies (UPS), GaN-based devices can compete with both Si and SiC

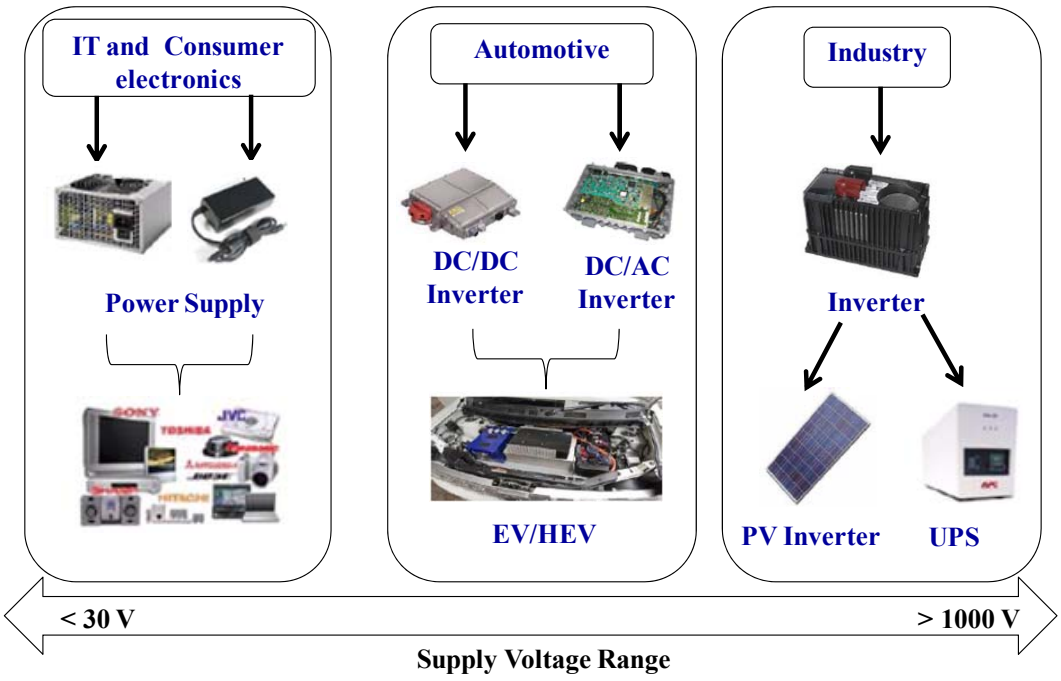


Fig. 1.1. Potential applications for GaN-based power devices. Based on the supply voltage range, the applications are divided into three categories: IT and consumer electronics, automotive, and industry [8].

devices, which have already been commercially adopted. Recently (July 2012), a 600 V GaN power diode was announced by Transphorm Inc. for application in PV panels and electric vehicles (EV) or hybrid electric vehicles (HEV) (source: http://www.transphormusa.com/).

As shown in Fig. 1.2, GaN belongs to a group of nitride materials, such as indium gallium nitride (InGaN) and aluminum gallium nitride (AlGaN), which covers a broad range of the direct bandgap energy from 1.9 to 6.2 eV [2]-[3]. With the development of GaN-based heterostructure growth, the advantages of GaN-based devices are being further exploited. A brief review of the polarization charge in AlGaN/GaN heterostructure is given in Section 1.1.2.

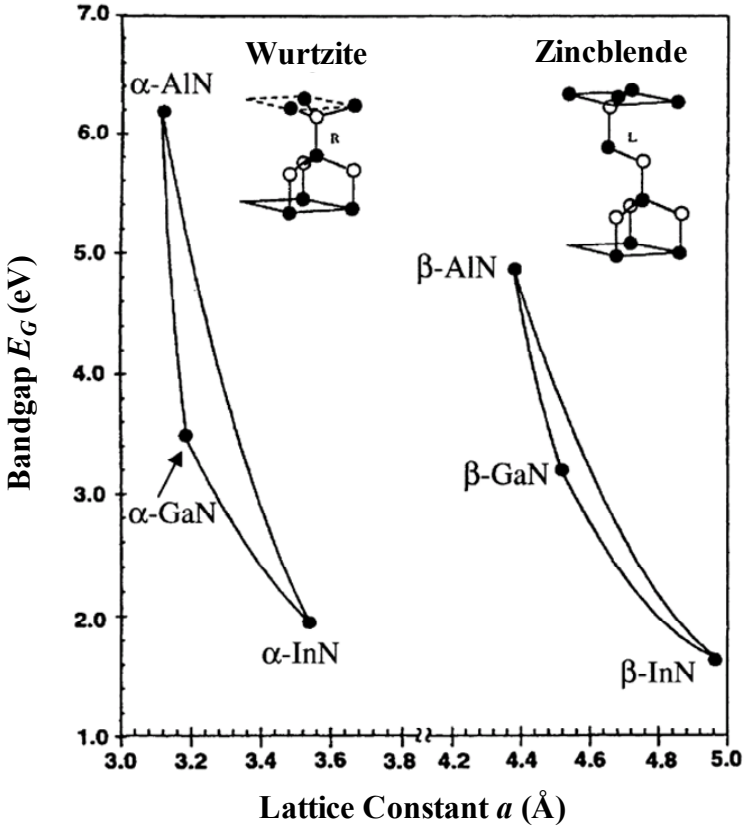
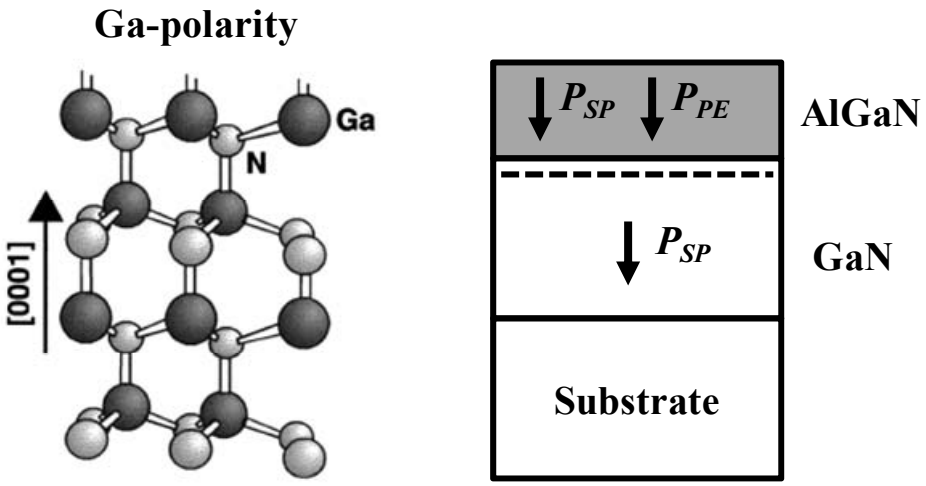


Fig. 1.2. Bandgap E_G of hexagonal (α-phase) and cubic (β-phase) InN, GaN, AlN, and their alloys versus lattice constant a [3].

1.1.2 AlGaN/GaN Heterostructure: Polarization Charge

The AlGaN/GaN heterostructure offers a high density of 2-DEG (~ 1×10^{13} cm^{-2}), due to its large spontaneous and piezoelectric polarization [9]-[10]. In addition, electron mobility of more than 2000 $cm^2/V \cdot s$ in the 2-DEG has been achieved [9]. Typically AlGaN/GaN HEMTs use the Ga-polarity face. Fig. 1.3 (a) shows the crystal structure of wurtzite GaN with the Ga-polarity face. Due to the smaller lattice constant as compared to GaN, the AlGaN barrier layer is under tensile strain if there is no strain relaxation. Usually, the GaN layer under the AlGaN barrier layer is assumed to be relaxed, since the thickness of the GaN layer is usually several micrometers, whereas the thickness of the AlGaN barrier layer is in the order of tens of nanometers. Directions of the spontaneous (P_{SP}) and piezoelectric (P_{PE}) polarization for wurtzite AlGaN/GaN heterostructure with the Ga-polarity face are labeled in Fig. 1.3 (b). Polarization charge density σ for an abrupt pseudomorphic



(a) (b)

Fig. 1.3. (a) Schematic drawing of the crystal structure of wurtzite GaN with the Ga-polarity face. (b) Directions of the spontaneous (P_{SP}) and piezoelectric (P_{PE}) polarization for wurtzite AlGaN/GaN heterostructure with the Ga-polarity face are labeled [9].

AlGaN/GaN heterostructure can be expressed as [10]:

$$\sigma = P(\text{AlGaN}) - P(\text{GaN})$$

$$= \{P_{SP}(\text{AlGaN}) + P_{PE}(\text{AlGaN})\} - \{P_{SP}(\text{GaN})\}. \quad (1.1)$$

To calculate the dependence of polarization charge density σ on the Al content x of the $Al_xGa_{1-x}N$ barrier layer, the equations for P_{SP} and P_{PE} of the $Al_xGa_{1-x}N$ barrier layer are given by [10]:

$$P_{SP}(Al_xGa_{1-x}N) = (-0.052x - 0.029)\ \text{C/m}^2, \quad (1.2)$$

$$P_{PE}(Al_xGa_{1-x}N) = 2\frac{a-a_0}{a_0}(e_{31} - e_{33}\frac{C_{13}}{C_{33}})\ \text{C/m}^2, \quad (1.3)$$

where a is the lattice constant of the $Al_xGa_{1-x}N$ barrier layer, a_0 is the equilibrium value of the lattice constant of GaN, C_{13} and C_{33} are the elastic constants, and e_{31} and e_{33} are piezoelectric constants. With a linear interpolation between the physical properties of GaN and AlN, the lattice constant of the $Al_xGa_{1-x}N$ barrier layer is given by [10]:

$$a\ (x) = (-0.077x + 3.189)10^{-10}\ \text{m}, \quad (1.4)$$

the elastic constants of the $Al_xGa_{1-x}N$ barrier layer are:

$$C_{13}(x) = (5x + 103)\ \text{GPa}, \quad (1.5)$$

$$C_{33}\ (x) = (-32x + 405)\ \text{GPa}, \quad (1.6)$$

the piezoelectric constants of the $Al_xGa_{1-x}N$ barrier layer are:

$$e_{31}(x) = (-0.11x - 0.49)\ \text{C/cm}^2, \quad (1.7)$$

$$e_{33}(x) = (0.73x + 0.73)\ \text{C/cm}^2. \quad (1.8)$$

Based on Equations (1.1)-(1.3), the amount of polarization charge density σ for the $Al_xGa_{1-x}N$/GaN heterostructure can be expressed as [10]:

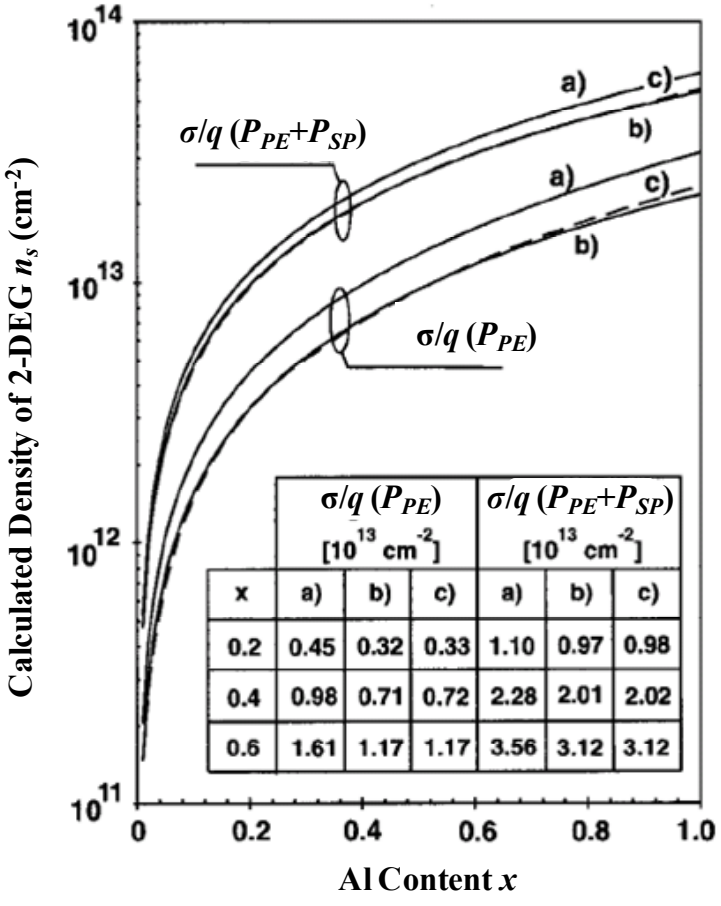
$$|\sigma(x)| = |P_{SP}(Al_xGa_{1-x}N) + P_{PE}(Al_xGa_{1-x}N) - P_{SP}(\text{GaN})|$$

$$= \mid 2\frac{a(0)-a(x)}{a(x)}(e_{31}-e_{33}\frac{C_{13}}{C_{33}})+P_{SP}(x)-\ P_{SP}(x)\ \mid . \quad (1.9)$$

Due to the positive polarization charges at the $Al_xGa_{1-x}N$/GaN interface, the free electrons tend to compensate at the AlGaN/GaN interface, and form 2-DEG. The density of 2-DEG n_s can be estimated using [10]

$$n_s(x)=\frac{+\sigma(x)}{q}-\left(\frac{\varepsilon_0\varepsilon_r(x)}{t_1 q^2}\right)[q\phi_b(x)+E_F(x)-\Delta E_C(x)], \qquad (1.10)$$

where t_1 is thickness of the $Al_xGa_{1-x}N$ barrier layer, ε_r is the dielectric constant of the $Al_xGa_{1-x}N$ barrier layer, q is the electronic charge, ϕ_b is the Schottky-barrier height, E_F is the Fermi level with respect to the GaN



x	$\sigma/q\ (P_{PE})$ [10^{13} cm^{-2}]			$\sigma/q\ (P_{PE}+P_{SP})$ [10^{13} cm^{-2}]		
	a)	b)	c)	a)	b)	c)
0.2	0.45	0.32	0.33	1.10	0.97	0.98
0.4	0.98	0.71	0.72	2.28	2.01	2.02
0.6	1.61	1.17	1.17	3.56	3.12	3.12

Fig. 1.4. The calculated density of 2-DEG n_s of pseudomorphic AlGaN/GaN heterosture as a function of Al content x of the $Al_xGa_{1-x}N$ barrier layer [10].

conduction band edge energy, and ΔE_C is the conduction band offset at the $Al_xGa_{1-x}N$/GaN interface. Fig. 1.4 plots the calculated n_s of pseudomorphic AlGaN/GaN heterostructure as a function of Al content x of the $Al_xGa_{1-x}N$ barrier layer [10].

1.2 Literature Review of High Voltage AlGaN/GaN HEMTs

For the AlGaN/GaN HEMTs in high voltage applications, high breakdown voltage V_{BR} and low on-state resistance R_{on} are two of the most important requirements. For a vertical device with a uniform doping profile, if low on-state resistance R_{on} is desired, the device doping level should be increased. However, breakdown voltage V_{BR} decreases with increasing doping level. For the lateral AlGaN/GaN HEMTs during the off-state, it is assumed that the electric field in the depletion region under the gate is a combination of a vertical polarization field ξ_P and a constant lateral electric field due to the drain bias (assuming the gate-to-drain is fully depleted), the relationship between on-state resistance R_{on} and breakdown voltage V_{BR} can be expressed as [11]:

$$R_{on} = \frac{V_{BR}^2}{q\mu_n n_s \xi_C^2}, \text{ and } \xi_C^2 = \xi_{br,AlGaN}^2 - \xi_P^2 , \qquad (1.11)$$

where q is the electronic charge and $\xi_{br,AlGaN}$ is the breakdown field of the AlGaN barrier layer. Fig. 1.5 shows the theoretical limit of on-state resistance R_{on} as a function of breakdown voltage V_{BR} for GaN, SiC, and Si. With a given breakdown voltage, for example, 1000 V, GaN-based devices can offer an on-state resistance R_{on} of 2 ~ 3 orders of magnitude lower than that of Si.

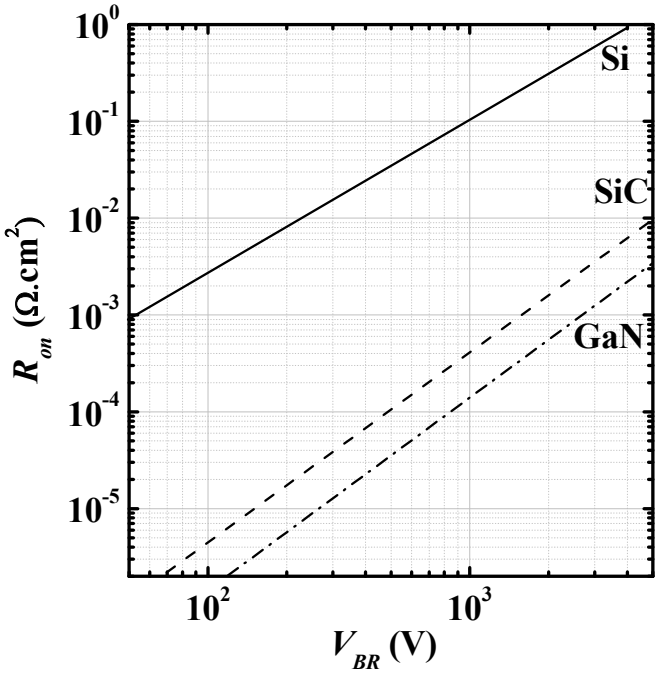


Fig. 1.5. Theoretical limit of the on-state resistance R_{on} as a function of breakdown voltage V_{BR} for GaN, SiC, and Si devices [11].

Since the first demonstration of AlGaN/GaN HEMTs on sapphire substrate by Khan *et al*. [12] in 1993, tremendous progress has been made for AlGaN/GaN HEMTs on sapphire, SiC, or silicon substrates [13]-[14]. Preliminary work on high voltage AlGaN/GaN HEMTs was done by Zhang *et al*. [15]. The breakdown mechanism of AlGaN/GaN HEMTs is due to an avalanche process that usually occurs near the gate edge of the drain side. It is generally accepted that the essence of achieving a high breakdown voltage V_{BR} in AlGaN/GaN HEMTs is to have an increased depletion width from the drain to the gate or to decrease the peak electrical field near the gate edge of the drain side. It is worth noting that a highly resistive buffer is essential to achieve AlGaN/GaN HEMTs with a high breakdown voltage V_{BR}. Technologies of increasing the breakdown voltage V_{BR} of AlGaN/GaN HEMTs can be divided into two categories: (1) GaN buffer growth technology

and (2) device design technology. The purpose of GaN buffer growth technology is to reduce the buffer leakage current and avoid the vertical breakdown by using various methods, such as C-doped [16] or Fe-doped buffer [17], thick GaN buffer [18]-[19], AlN buffer [20], AlGaN-based buffer [21], multi-pairs of alternate AlN/GaN layer buffer [22], etc. Buffer layer growth technologies are mainly developed by the GaN epitaxial growth groups. On the other side, there are many innovative designs from device groups to reduce the peak electrical field near the gate edge of the drain side, such as field plate structure [15], trench gate structure [23], etc.

For the conventional AlGaN/GaN HEMTs with a Schottky gate structure, breakdown voltage V_{BR} of 460 V was achieved by Zhang *et al*. [15] for devices with a gate-to-drain spacing L_{GD} of 20 μm. With an integration of an overlapping gate structure on the AlGaN/GaN HEMTs, the breakdown voltage V_{BR} of devices was increased to 570 V by Zhang *et al*. [15] [Fig. 1.6 (a)]. Enhancement of breakdown voltage V_{BR} was due to the reduction of the peak electrical field near the gate edge of the drain side, since it can locally cause the impact ionization near the drain side of the gate structure and increase the gate leakage current. To further reduce the gate leakage current, AlGaN/GaN HEMTs with an insulated gate structure were demonstrated by Zhang *et al*. [24] using jet vapor deposition (JVD) SiO_2 as the gate dielectric, and achieved a breakdown voltage V_{BR} of 1300 V and an on-state resistance R_{on} of 1.7 mΩ·cm^2 for the devices with a gate-to-drain spacing L_{GD} of 20 μm [Fig. 1.6 (b)]. Later, Xing *et al*. [25] demonstrated the conventional AlGaN/GaN HEMTs with a breakdown voltage V_{BR} up to 900 V using multiple field plates over insulators [Fig. 1.6 (c)]. With a modification of the

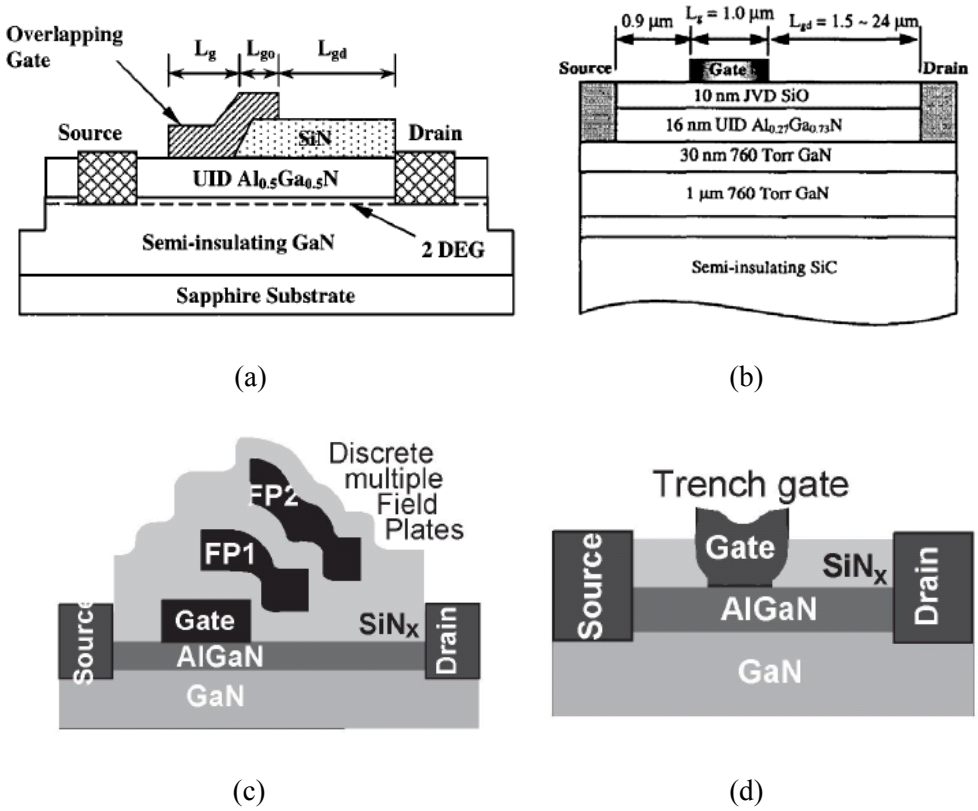


Fig. 1.6. Schematic diagrams of epitaxial layers and cross sections of (a) AlGaN/GaN HEMT with an overlapping gate [15], (b) insulated gate AlGaN/GaN HEMT with JVD deposited SiO_2 gate dielectric [24], (c) AlGaN/GaN HEMT with discrete multiple field plates [25], and (d) AlGaN/GaN HEMT with a trench gate [23].

gate shape for conventional AlGaN/GaN HEMTs, Dora *et al*. [23] achieved a breakdown voltage V_{BR} of 1900 V and an on-state resistance R_{on} of 2 mΩ·cm^2 for the devices with a gate-to-drain spacing L_{GD} of 20 μm by introducing a trench gate structure [Fig. 1.6 (d)].

Most of the early work done on high voltage AlGaN/GaN HEMTs employed sapphire or SiC substrates. Single crystalline GaN was first realized on sapphire using vapor phase deposition by Marusha *et al*. [26] in 1969. Since then, GaN-on-sapphire growth technique has become more mature, due to the demand of GaN-based optical devices [27]. As for the GaN-on-SiC wafers, there are two main advantages. The first is that it is much easier to

grow semi-insulating GaN layers on SiC (3.3 % lattice mismatch) than on sapphire substrate (14 % lattice mismatch), and the other reason is that SiC has a high thermal conductivity K (4.9 $WK^{-1}cm^{-1}$), which is highly desired for high power AlGaN/GaN HEMTs [28]. However, the high cost of SiC substrates makes it difficult for commercial application in the cost sensitive consumer electronics sector. Although there is a large lattice mismatch of 17 % between silicon and GaN, huge progress has been made for GaN grown on silicon substrate in recent years. For example, growth of GaN-on-silicon wafers with diameters of 6 inches [29]-[31] or 8 inches [32] was demonstrated. In addition, device results of AlGaN/GaN HEMTs on 8-inch GaN-on-silicon wafers were

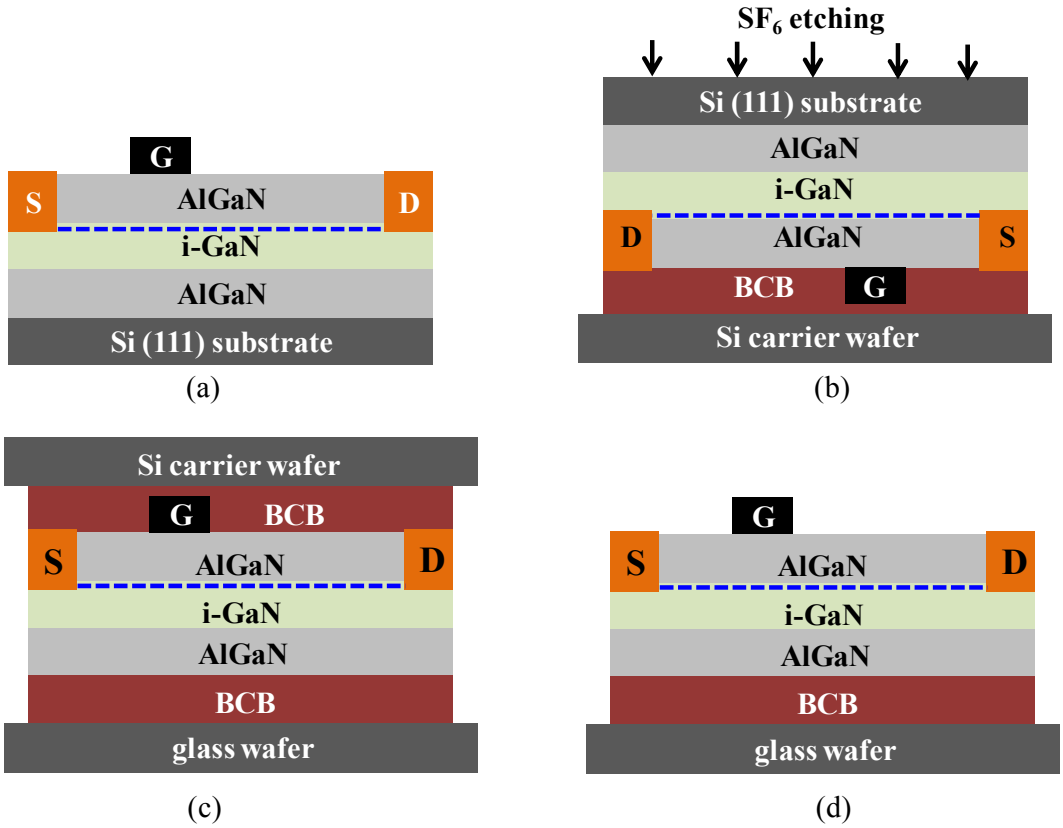


Fig. 1.7. Process flow of the substrate transfer technology [34]. (a) Standard AlGaN/GaN HEMT on Si substrate. (b) Bonding to a Si carrier wafer and Si (111) substrate removal, and BCB stands for benzocyclobutene. (c) GaN/AlGaN buffer bonded to a glass wafer. (d) Final device structure after releasing the carrier wafer. G, S and D stand for gate, source and drain, respectively.

reported by Arulkumaran *et* al. [33]. Due to the low cost of silicon wafers, GaN-on-silicon technology on large diameter wafers (6-inch or 8-inch) is a promising approach for the next-generation power electronic devices.

For GaN-on-silicon power devices, it was suggested that the V_{BR} of the AlGaN/GaN-on-silicon HEMTs is limited by the silicon substrate [34]. By removing the silicon substrate and transferring the AlGaN/GaN HEMTs to a glass substrate, the devices with a gate-to-drain spacing L_{GD} of 20 μm achieved a breakdown voltage V_{BR} of 1900 V and an on-state resistance R_{on} of 2 mΩ·cm^2 (Lu *et al*. [34]). The process flow of silicon substrate transfer technology is shown in Fig. 1.7. Instead of removing the whole silicon wafer,

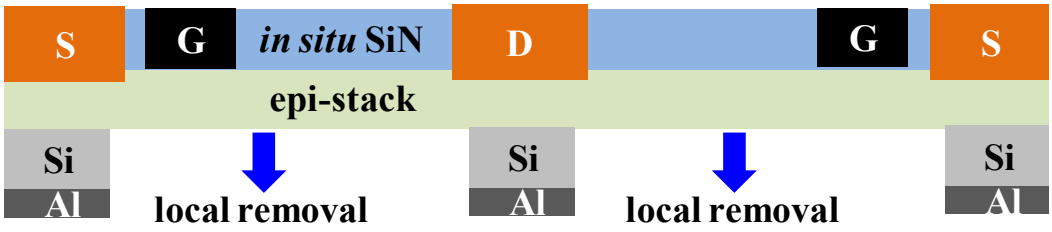


Fig. 1.8. Schematic cross section after the local silicon removal process [35]. G, S and D stand for gate, source and drain, respectively.

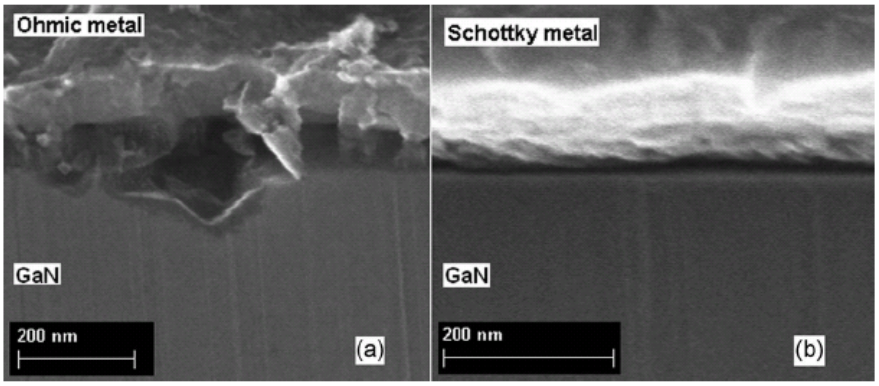


Fig. 1.9. Cross-sectional SEM images of (a) ohmic contact on AlGaN/GaN and (b) Schottky contact on AlGaN/GaN structure grown on Si substrate [36].

a local silicon removal technology for AlGaN/GaN/AlGaN double-heterostructure HEMTs was demonstrated by Srivastava *et al*. [35]. The devices with a gate-to-drain spacing L_{GD} of 20 μm achieved a breakdown voltage V_{BR} of 2200 V. The schematic cross section after the local silicon removal process is shown in Fig. 1.8 [35]. In addition, Schottky drain technology for AlGaN/GaN HEMTs was proposed by Lu *et al*. [36] to improve the device breakdown voltage V_{BR}. A cross-sectional scanning electron microscope (SEM) image of the ohmic contact (Au/Ni/Al/Ti) on AlGaN/GaN is shown in Fig. 1.9 (a). It can be seen that there are "metal spikes" in the GaN underneath the ohmic contacts. However, the surface of AlGaN/GaN with a Schottky contact (Au/Ti) is smooth [Fig. 1.9 (b)]. It was suggested by Lu *et al*. [36] that the "metal spikes" in the GaN created during the ohmic alloying process are responsible for the higher leakage current and lower breakdown voltage V_{BR} of the devices with ohmic source/drain contacts.

Some of major device design technologies to enhance the breakdown voltage V_{BR} of AlGaN/GaN HEMTs were discussed above. Most of the efforts are to reduce the peak electric field near the gate edge of the drain side, or to eliminate the vertical breakdown through the silicon substrate.

1.3 Challenges of AlGaN/GaN High Electron Mobility Transistors

1.3.1 Formation of High Quality Gate Stack

Conventional AlGaN/GaN HEMTs employ a Schottky gate, which typically have the shortcoming of a large gate leakage current density J_G. High J_G not only results in a lower breakdown voltage, but also leads to issues related to noise, power loss, and reliability. High J_G could be reduced by

integrating a metal-oxide-semiconductor (MOS) structure into the AlGaN/GaN HEMTs to form AlGaN/GaN MOS-HEMTs. There has been many work using a MOS gate structure by using various dielectrics, such as HfO_2 [37], Al_2O_3 [38], MgO [39], Sc_2O_3 [40], ZrO_2 [41], Gd_2O_3 [42], SiO_2 [43], SiN_x [43], and TiO_2 [44], to reduce the gate leakage current density J_G of the AlGaN/GaN HEMTs. In addition, treatment on the AlGaN/GaN surface has also been intensively explored in many ways, such as treatment using $(NH_4)_2S_x$ [45], H_2O_2 [46], ultraviolet (UV) illumination [47], and gas plasma (O_2 [48], [49], NH_3 [50], BCl_3 [51], CHF_3 [52], CF_4 [52]-[53], SF_6 [54], or N_2 [55]). Nevertheless, further improvement on the quality of the interface between the dielectric and GaN or AlGaN is still highly desired.

1.3.2 Strain Engineering

Strain engineering for silicon metal-oxide-semiconductor field-effect transistor (MOSFET) has been intensively studied, such as SiGe source/drain stressor for silicon p-MOSFET [56]-[60], silicon-carbon source/drain stressor for silicon n-MOSFET [61]-[65], gate-induced channel stress [66], diamond-like carbon (DLC) stress liner for silicon p-silicon MOSFET [68]-[71], and silicon nitride stress liner for silicon n-MOSFET [67]. Polarization charge density for AlGaN/GaN heterostructure could be locally modulated through piezoelectric polarization of AlGaN/GaN heterostructure, thus further enhancing the carrier mobility by reducing the Coulomb carrier scattering." In the literature, AlGaN/GaN HEMTs with a tensile silicon nitride liner has been studied [72]. In order to further enhance the performance of AlGaN/GaN

HEMTs, strain engineering by a higher stress liner for AlGaN/GaN HEMTs is worthy to be further explored.

1.3.3 Gold-Free CMOS Compatible Process

GaN power devices have been considered as one of the candidates for the next-generation power devices. If GaN devices can be fabricated using the current mature silicon complementary metal-oxide-semiconductor (CMOS) technologies, the fabrication cost can be lowered down. The use of gold is typically avoided in the silicon CMOS fabrication process, because gold will introduce deep-level traps in silicon transistors. However, in the reported literatures, most of the GaN-based HEMTs were fabricated using a gold-contained process, where gold was used either in the gate or the source/drain contacts [73]-[74]. Therefore, the development of gold-free fabrication process is essential to fabricate the GaN-based HEMTs in silicon CMOS foundries.

1.4 Objective of Research

The objective of the research work in this thesis is to address some of the most challenging issues faced by AlGaN/GaN HEMTs. In order to form a high quality MOS gate stack on GaN or AlGaN, novel *in situ* surface passivation technique, such as *in situ* vacuum anneal and SiH_4 treatment, was proposed. The quality of the interface between the dielectric and GaN was evaluated using a GaN MOS capacitor structure. Effectiveness of this *in situ* surface passivation technique on AlGaN/GaN MOS-HEMTs was also demonstrated. In order to further boost the device performance of

AlGaN/GaN MOS-HEMTs, strain engineering using a DLC stress liner was explored. In order to enable GaN power devices to be fabricated in the silicon foundries, high voltage AlGaN/GaN MOS-HEMTs using a CMOS compatible gold-free process were demonstrated on both AlGaN/GaN-on-silicon and AlGaN/GaN-on-sapphire substrates.

1.5 Thesis Organization

The main work in this thesis is documented in 4 Chapters.

Chapter 2 describes the novel surface passivation technique to realize high quality metal gate/high-permittivity dielectric stacks on GaN surface. This novel *in situ* surface passivation technique comprises vacuum anneal for desorption of contaminants on the GaN surface, followed by a surface treatment in a multi-chamber metal-organic chemical vapor deposition (MOCVD) gate cluster system. A capacitor test structure consisting of a tantalum nitride (TaN)-hafnium aluminum oxide (HfAlO) gate stack on GaN was used. Interface state density D_{it} was measured from midgap to near conduction band edge using the conductance method at a high temperature, and the lowest D_{it} of ~ 1×10^{11} cm^{-2} eV^{-1} between GaN and HfAlO was achieved using *in situ* vacuum anneal and SiH_4 treatment [75]-[77].

Chapter 3 reports the effect of *in situ* vacuum anneal and SiH_4 treatment on the electrical characteristics of AlGaN/GaN MOS-HEMTs. Devices with *in situ* vacuum anneal and SiH_4 treatment show reduced gate leakage current I_G and improved saturation drain current. In addition, devices with *in situ* vacuum anneal and SiH_4 treatment achieved current on/off, I_{on}/I_{off}, ratio of ~ 10^6 and sub-threshold swing S of less than 100 mV/decade [78].

Chapter 4 demonstrates the integration of a highly compressive DLC stress liner on AlGaN/GaN MOS-HEMTs. In this work, a 40 nm thick DLC film with a highly intrinsic compressive stress of up to 6 GPa was integrated on AlGaN/GaN MOS-HEMTs. Up to 32 % enhancement of saturation drain current and 10 % reduction of the source/drain series resistance were observed for the DLC-strained AlGaN/GaN MOS-HEMTs over the control. Also, a positive threshold voltage (V_{th}) shift was observed for the DLC-strained AlGaN/GaN MOS-HEMTs, which thus shows the potential of realizing enhancement mode AlGaN/GaN MOS-HEMTs by strain engineering [79]-[80].

Chapter 5 reports the realization of high voltage AlGaN/GaN MOS-HEMTs using a CMOS compatible gold-free process. AlGaN/GaN-on-silicon MOS-HEMTs with a gate-to-drain spacing L_{GD} of 5 μm achieved a breakdown voltage V_{BR} of 800 V and an on-state resistance R_{on} of 3 mΩ·cm^2. In addition, sub-threshold swing S of ~ 97 mV/decade and current on/off, I_{on}/I_{off}, ratio of ~ 10^6 were obtained. Compared with those of gold-free AlGaN/GaN-on-silicon MOS-HEMTs having a gate-to-drain spacing L_{GD} of less than 10 μm reported in the literature, the breakdown voltage V_{BR} achieved in this work is the highest to date. Also, AlGaN/GaN-on-sapphire MOS-HEMTs with a gate-to-drain spacing L_{GD} of 20 μm achieved a breakdown voltage V_{BR} of 1400 V and an on-state resistance R_{on} of 22 mΩ·cm^2. This is the highest breakdown voltage V_{BR} achieved for gold-free AlGaN/GaN MOS-HEMTs to date. In addition, high I_{on}/I_{off} ratio of ~ 10^9 and low I_G of ~ 10^{-11} A/mm were also obtained [81]-[83].

Finally, the main contributions of this thesis and suggestions for future work are summarized in Chapter 6.

Chapter 2

In Situ Surface Passivation of Gallium Nitride in Advanced Gate Stack Process

2.1 Introduction

Gallium nitride (GaN)-based materials are attractive for high power, high temperature, and high frequency applications [84]-[87], primarily due to their superior properties, such as large breakdown electric field, wide energy bandgap, and high electron mobility. High electron mobility transistors (HEMTs) employing the AlGaN/GaN heterostructure further exploit the high electron mobility in the two-dimensional electron gas (2-DEG) at the AlGaN/GaN interface. However, many GaN-based HEMTs employ a Schottky gate structure, which has the shortcoming of a high gate leakage current density J_G. High J_G could be reduced by using a metal-oxide-semiconductor (MOS) structure [88] and through optimal selection of gate dielectric materials [89]. In addition, AlGaN/GaN HEMTs suffer from current collapse during large signal operation at high frequency, usually referred as "dc-to-radio frequency (RF) dispersion". Slow response of surface traps is believed to be one of the major contributing factors [90].

Employing a MOS gate structure using various dielectrics, such as HfO_2 [37], Al_2O_3 [38], MgO [39], Sc_2O_3 [40], ZrO_2 [41], Gd_2O_3 [42], SiO_2 [43], SiN_x [43], and TiO_2 [44], can significantly reduce J_G for the AlGaN/GaN HEMTs with a Schottky gate structure. As shown in Table 2.1, various

Table 2.1. Various deposition methods to achieve a high quality dielectric/GaN interface [37]-[44]. "–" means "not reported".

Dielectric	**Deposition Method**	**Interface State Density D_{it} ($cm^{-2}eV^{-1}$)**	**Characterization Method**	**Ref.**
HfO_2	Atomic Layer Deposition (ALD)	~ 2×10^{11} at midgap	Terman method	[37]
Al_2O_3	ALD	~ (4-9) $\times 10^{11}$ near the midgap	–	[38]
MgO	Electron-Cyclotron-Resonance Molecular Beam Epitaxy (ECR-MBE)	~ 6×10^{11} at 0.3 eV below E_C	Both Terman and conductance methods at 300 °C	[39]
Sc_2O_3	MBE	–	–	[40]
ZrO_2	Electron Beam Evaporation	–	–	[41]
Gd_2O_3	MBE	~ 4.2×10^{11}	–	[42]
SiO_2	Plasma Enhanced Chemical Vapor Deposition (PECVD)	~ 2.5×10^{11}	Terman method	[43]
SiN_x	PECVD	~ 6.5×10^{11}	Terman method	[43]
TiO_2	Liquid Phase Deposition	~ 7.48×10^{11}	Terman method	[44]

deposition methods were intensively investigated to achieve a high quality dielectric/GaN interface in terms of interface state density (D_{it}).

As illustrated in Fig. 2.1, there are two commonly employed techniques for passivating AlGaN/GaN HEMTs: (1) surface passivation/treatment is to reduce surface traps on the GaN or AlGaN surface by using various treatment methods (e.g. *in situ* VA and SiH_4 passivation), and (2) device passivation is to encapsulate the device by using various insulators or dielectrics (e.g. oxide/nitride passivation). Surface passivation on the GaN or AlGaN surface before the dielectric layer deposition has been intensively explored to further improve the interface quality between dielectric and GaN or AlGaN layer, such as $(NH_4)_2S_x$ treatment [45], H_2O_2 treatment [46], ultraviolet (UV) illumination[47], and various gas plasma treatments,

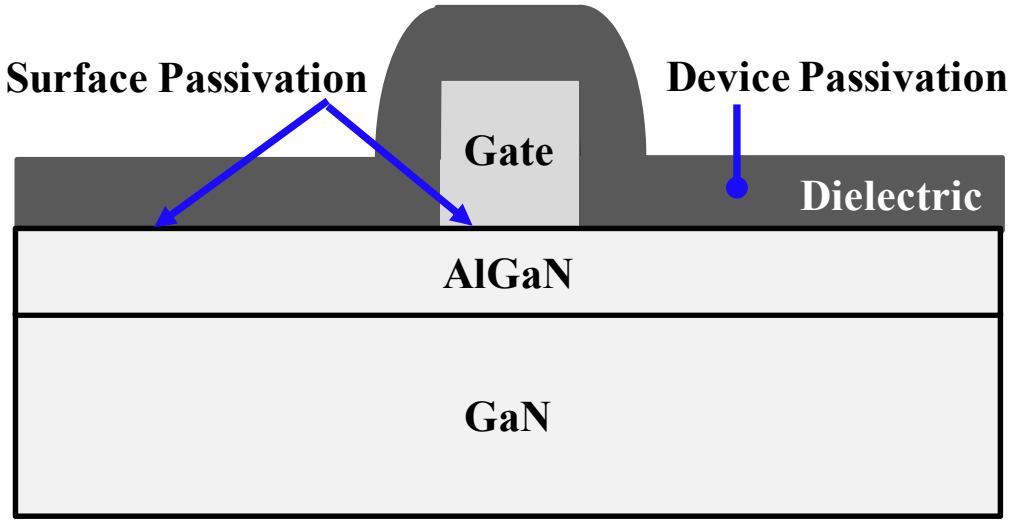


Fig. 2.1. Schematic diagram illustrating two approaches for passivating AlGaN/GaN HEMTs: surface passivation/treatment and device passivation.

including the use of O_2 [48]-[49], NH_3 [50], BCl_3 [51], CHF_3 [52], CF_4 [52]-[53], SF_6 [54], and N_2 [55] plasma. Although plasma-enhanced chemical vapor deposition (PECVD) SiN_x film is the most widely used as the device passivation layer for AlGaN/GaN HEMTs [91], some reports show that it increases the device gate leakage, which is dominated by surface leakage current due to the electron hopping through the gap-states in the SiN_x layer [92]-[93]. Besides, an even more effective device passivation technique was demonstrated by performing *in situ* Si_3N_4 [94] or SiCN cap layer [95] growth, immediately after the AlGaN/GaN layers were grown without breaking the chamber vacuum.

In this Chapter, a novel and effective surface passivation technique for GaN is demonstrated, and it comprises the steps of *in situ* vacuum anneal (VA) and treatment in either silane-ammonia (SiH_4+NH_3) or silane (SiH_4) only, prior to the deposition of hafnium-based high-permittivity dielectric using a metal-organic chemical vapor deposition (MOCVD) system [75]-[77]. The effect of VA temperature and the SiH_4+NH_3 or SiH_4 treatment temperature on

D_{it} and flatband voltage shift ΔV_{FB} was investigated. A capacitor test structure consisting of a tantalum nitride (TaN)-hafnium aluminum oxide (HfAlO) gate stack on GaN was used. D_{it} from near the conduction band edge E_C to the mid-gap of GaN was measured at temperatures of 300 and 460 K using the conductance method with series resistance correction. HfAlO with 10 % Al was chosen as the dielectric for this study due to its higher crystallization temperature (~ 800 ºC) than that of pure HfO_2 (~ 400 ºC) and its higher dielectric constant ($\varepsilon_r \sim 20$) than that of pure Al_2O_3 ($\varepsilon_r \sim 9$) [96]-[97].

2.2 Development of *In Situ* Surface Passivation for Gallium Nitride

2.2.1 Experiment

Si-doped (2×10^{18} cm^{-3}) GaN (0001) epitaxial layer on sapphire substrates were used as the starting materials. The GaN epitaxial layer has a thickness of 2 μm and a root-mean-square surface roughness of less than 0.5 nm. Pre-gate cleaning for all samples comprised a 2-minute acetone and a 3-minute isopropanol degreasing step, a 10-minute dilute HCl (H_2O:HCl=1:1) native oxide removal step, and an *ex situ* surface passivation step in an undiluted $(NH_4)_2S$ solution for 30 minutes.

After pre-gate cleaning, the wafers were quickly loaded into a multi-chamber MOCVD gate cluster system, where VA, SiH_4+NH_3 or SiH_4 treatment, and deposition of HfAlO were performed (Fig. 2.2). In the first chamber of the MOCVD system, the wafers were annealed at various temperatures ranging from 200 to 600 ºC for 1 minute under a pressure of ~ 1×10^{-6} Torr. After VA, the wafers were transferred to the second chamber

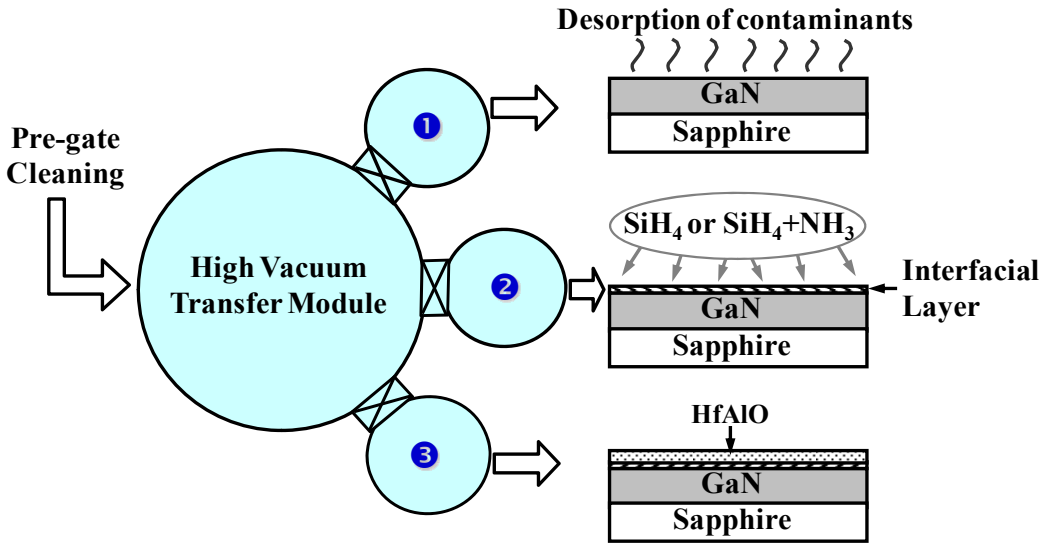


Fig. 2.2. Schematic diagram illustrating the *in situ* passivation and HfAlO deposition processes in a multi-chamber metal-organic chemical vapor deposition (MOCVD) gate cluster system. A high vacuum transfer module is connected to the three process chambers, including the first chamber for VA, the second chamber for surface treatment with SiH_4+NH_3 or SiH_4 only, and the third chamber for HfAlO deposition.

for either SiH_4+NH_3 or SiH_4 treatment at various temperatures ranging from 300 to 500 ºC for 1 minute at a pressure of 5 Torr. For SiH_4+NH_3 treatment, the flow rates of SiH_4 (mole fraction of 49.3 % and partial pressure of 2.46 Torr), NH_3 (mole fraction of 50.5 % and partial pressure of 2.53 Torr), and N_2 were 60, 60, and 250 standard cubic centimeter per minute (sccm), respectively. For the SiH_4 treatment, the flow rates of SiH_4 (mole fraction of 99.6 % and partial pressure of 4.98 Torr) and N_2 were 60 and 250 sccm, respectively. The detailed recipes for the VA, SiH_4+NH_3 or SiH_4 treatment, and HfAlO deposition are documented in Appendix A. Without breaking vacuum, the wafers were transferred to the third chamber for the deposition of HfAlO dielectric layer using liquid $HfAl(MMP)_2(OiPr)_5$ as a precursor [97]. The deposited HfAlO thickness was ~ 20 nm. For the control sample, the VA and SiH_4+NH_3 or SiH_4 treatment steps were skipped [98]-[100].

Post-deposition anneal (PDA) at 500 ºC for 60 s in a N_2 ambient was then performed for all the samples to improve the quality of the as-deposited HfAlO film [Fig. 2.3 (a)]. 100 nm of TaN was then deposited by reactive sputtering. This was followed by gate photolithography and Cl_2-based plasma etching of TaN for the gate electrode formation [Fig. 2.3 (b)-(c)]. Wet etching in dilute HF solution was performed to remove the HfAlO in the source/drain (S/D) contact regions. A contact metal stack (71 nm of Al on 30 nm of Ti) was deposited using an electron beam evaporator and patterned using a lift-off process. A 650 ºC, 30 s alloying process in N_2 ambient was performed to form ohmic contacts on GaN. The fabrication process was completed with a 30-minute forming gas anneal at 420 ºC [Fig. 2.3 (d)]. The fabricated capacitors with a square shape have an area of 40000 μm^2. Fig. 2.3 (e) shows the top-view of an optical image of the fabricated capacitor in this work.

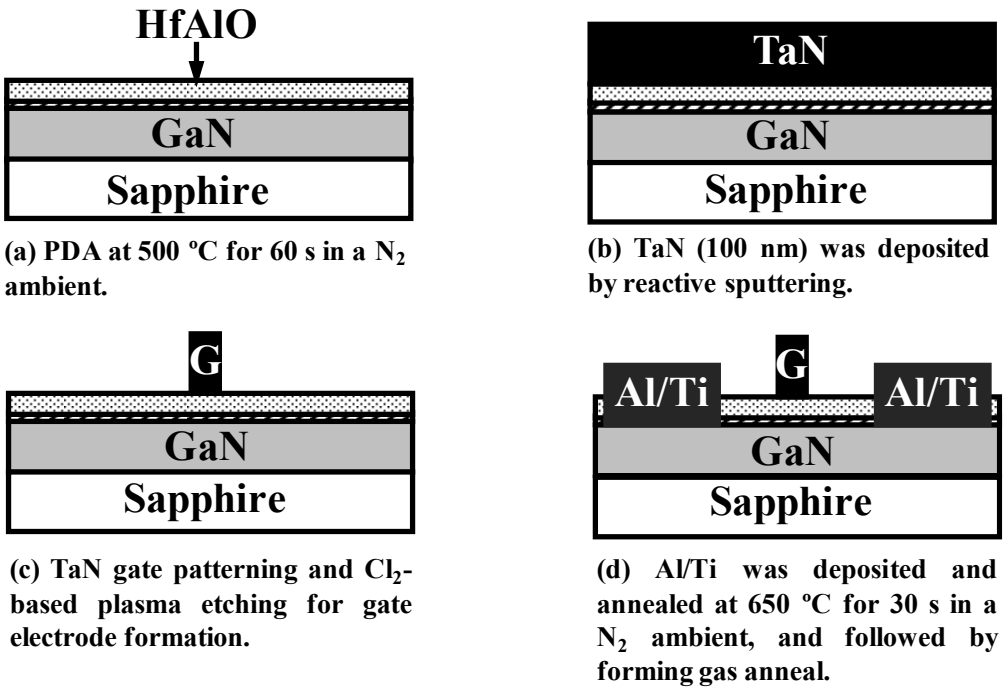
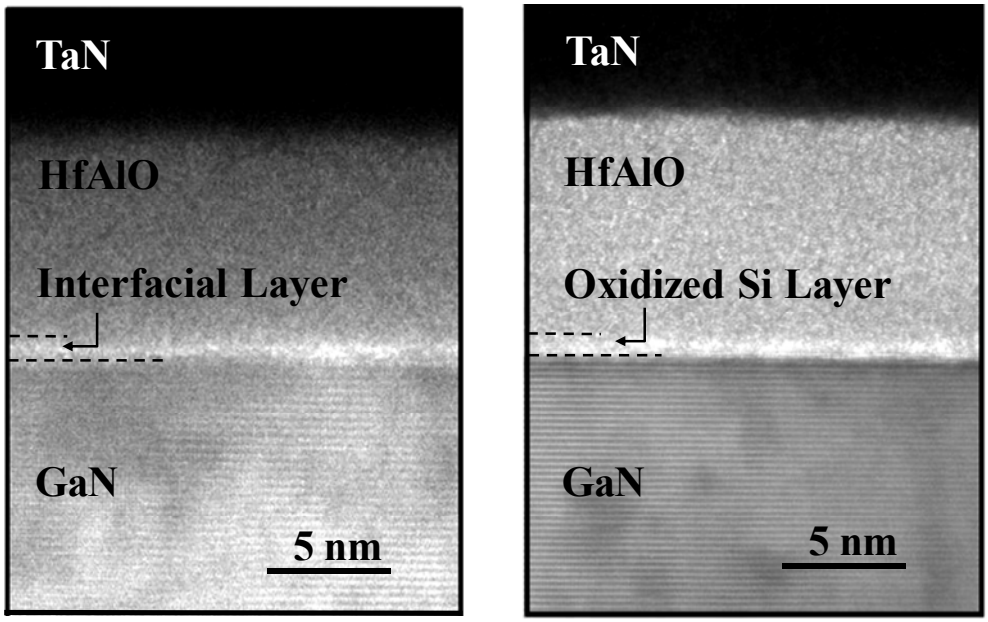


Fig. 2.3. (a) PDA was used to improve the quality of the as-deposited HfAlO film. 100 nm of TaN was deposited (b) and patterned (c) as the gate electrode using Cl_2-based plasma etching. (d) HfAlO was removed in the contact regions. An Al/Ti stack was deposited and annealed at 650 ºC for 30 s in a N_2 ambient to form ohmic contacts. (e) Optical image of the fabricated TaN/HfAlO/GaN capacitor structure.

2.2.2 Effect of Vacuum Anneal on Interface Quality

Fig. 2.4 (a) shows a transmission electron microscopy (TEM) image of a sample which received neither VA nor any gas treatment. An interfacial layer comprising the native oxide of GaN is observed between the gate dielectric and GaN. Fig. 2.4 (b) shows a TEM image of a sample which received 300 °C VA and 400 °C SiH_4 treatment. VA was performed for desorption of contaminants on the GaN surface [99]. The SiH_4 treatment formed a layer of Si which was subsequently oxidized during HfAlO deposition, as confirmed by X-ray photoelectron spectroscopy (XPS) [78]. The oxidized Si layer served as a protective layer to prevent the GaN surface from oxidation during HfAlO deposition.

To further investigate the effect of VA and SiH_4 treatment on the GaN surface, high-resolution XPS study [Fig. 2.5 (a) and (b)] was carried out on two GaN samples coated with a thin HfAlO (~1 nm) film. On a reference sample, VA and SiH_4 treatment were skipped. On the other sample, VA and SiH_4 treatment were performed at 300 and 400 ºC, respectively, prior to HfAlO deposition. In the Ga $3d_{5/2}$ spectrum, the main peak at 19.6 eV is contributed by Ga-N bond. For the reference sample, an additional peak corresponding to Ga-ON bond at 20 eV is detected [Fig. 2.5 (a)], and is attributed to the oxidation of the GaN surface in the initial stage of the dielectric deposition. For the GaN sample with VA and SiH_4 treatment prior to HfAlO deposition, the Ga-ON peak is absent as the GaN surface is protected by several monolayers of Si during the HfAlO deposition. This is similar to the results obtained from *in situ* SiH_4 passivation and HfAlO deposition on indium gallium arsenide [100].



(a) (b)

Fig. 2.4. Cross-sectional TEM images of TaN/HfAlO/GaN gate stacks, including (a) one which received neither VA nor any gas treatment, and (b) one which underwent VA at 300 ºC and SiH_4 treatment at 400 ºC.

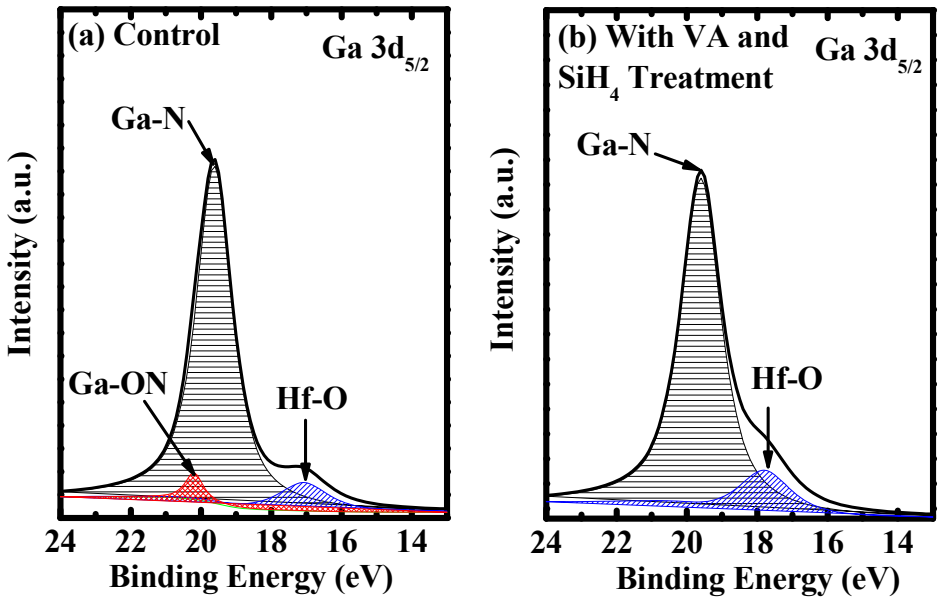


Fig. 2.5. *Ex situ* high-resolution XPS study showing the Ga $3d_{5/2}$ peak from two samples with a thin HfAlO (~ 1 nm) film formed on GaN. The Ga-ON and Ga-N bond energies are located at 20 and 19.6 eV, respectively. (a) Ga-ON peak is observed for the sample without VA and SiH_4 treatment, and (b) is absent for the sample with VA and SiH_4 treatment.

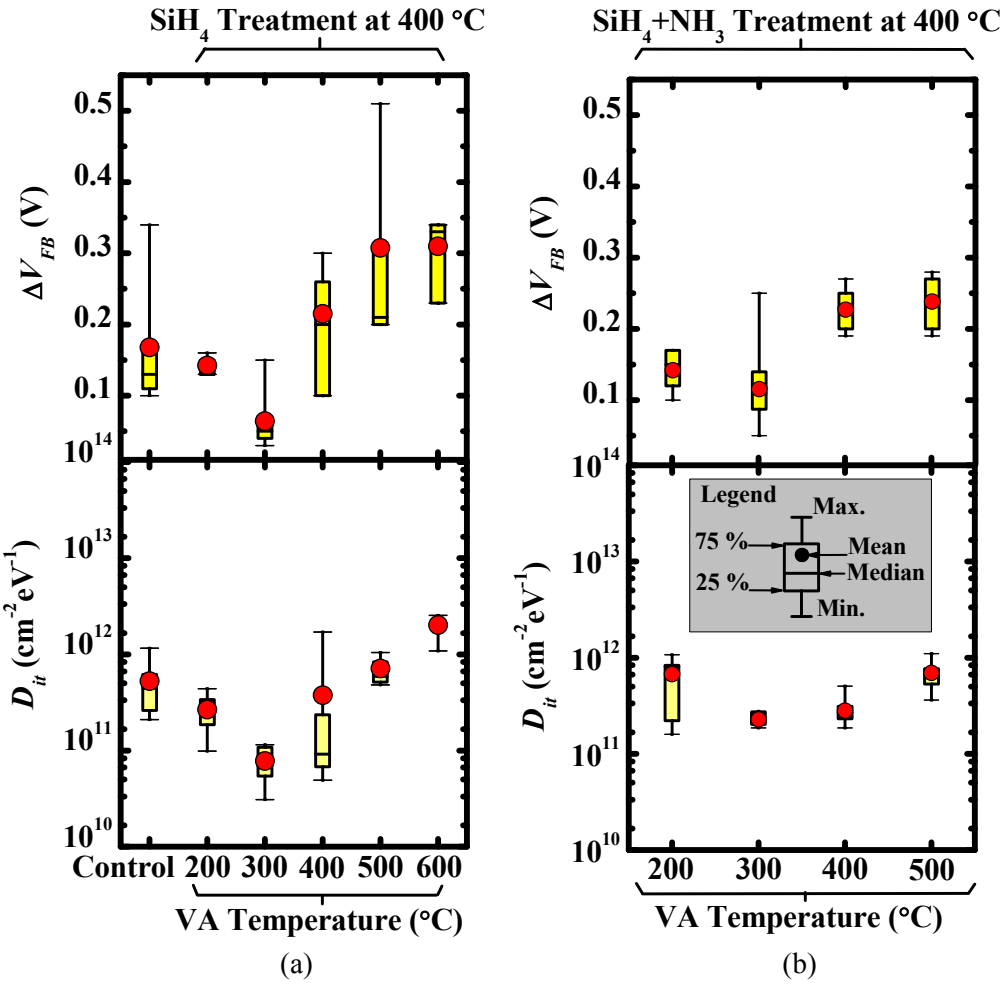


Fig. 2.6. (a) ΔV_{FB} and D_{it} as a function of VA temperature of TaN/HfAlO/GaN capacitors. VA time was fixed at 1 minute and the chamber pressure was 1×10^{-6} Torr. The control sample received neither VA nor any gas treatment. All other samples were subsequently treated with SiH_4 at 400 ºC before HfAlO deposition. (b) ΔV_{FB} and D_{it} as a function of VA temperature for samples which were subsequently treated with SiH_4+NH_3 at 400 ºC. There are ten devices in each experimental split.

The effect of VA temperature on D_{it} and ΔV_{FB} will be examined next. The treatment temperature in either SiH_4+NH_3 or SiH_4 ambient was fixed at 400 °C. ΔV_{FB} is defined as the flat-band voltage shift when the capacitance-voltage (*C-V*) characterization frequency is increased from 10 to 500 kHz, and voltage is swept from –3 to 4 V. D_{it} at 0.4 eV below the conduction band edge E_C of GaN for each TaN/HfAlO/GaN sample was measured using a single frequency *C-V* and conductance-voltage (*G-V*) extraction method at 100 kHz at room temperature [101]. It should be noted that this is a rapid characterization method to aid process development, and a more elaborate D_{it} characterization method will be introduced later. Using this rapid characterization technique, a large number of samples can be measured to obtain the statistical distribution of D_{it} for analysis (Fig. 2.6).

Vacuum anneal at 300 °C gives the lowest mean D_{it} of ~ 7.8×10^{10} cm^{-2} eV^{-1} at 0.4 eV below E_C and the lowest mean ΔV_{FB} of 0.06 V for samples which were subsequently treated with SiH_4 at 400 °C [Fig. 2.6 (a)]. This is significantly smaller than the mean D_{it} of 5.3×10^{11} cm^{-2} eV^{-1} and the mean ΔV_{FB} of 0.17 V for the control sample [leftmost data points in Fig. 2.6 (a)], which was not vacuum-annealed and was not treated with any gas. Moreover, it is also observed that vacuum anneal at temperatures exceeding ~ 500 °C leads to larger D_{it} and ΔV_{FB} as compared to the control. This is due to the fact that the decomposition of GaN takes place at temperatures above 496 °C under a pressure of 1×10^{-6} Torr, leading to surface deterioration [102].

For samples which were annealed in vacuum at various temperatures followed by SiH_4+NH_3 treatment at 400 °C, the lowest mean D_{it} (~ 2.3×10^{11} cm^{-2} eV^{-1} at 0.4 eV below E_C) and ΔV_{FB} (0.11 V) was achieved at 300 °C

vacuum anneal [Fig. 2.6 (b)]. The optimum vacuum anneal temperature is 300 °C. The D_{it} is generally higher for the samples with the addition of NH_3 in the surface treatment, and the possible reason for this will be explained in Section 2.2.3.

2.2.3 Effect of SiH_4 or SiH_4+NH_3 Treatment Temperature on Interface Quality

The vacuum anneal temperature is fixed at 300 °C and the effect of the SiH_4 or SiH_4+NH_3 treatment temperature on D_{it} and ΔV_{FB} will be investigated next. SiH_4 treatment at 400 °C achieved the lowest mean D_{it} and the smallest mean ΔV_{FB}, as seen from Fig. 2.7 (a). The increased mean D_{it} and mean ΔV_{FB} indicate that the HfAlO/GaN interface quality degrades when the SiH_4 treatment temperature is higher, e.g., at 500 °C. For the samples which were treated in SiH_4+NH_3 prior to HfAlO deposition [Fig. 2.7 (b)], the optimized SiH_4+NH_3 treatment temperature is also 400 °C. However, D_{it} at the optimum temperature is higher for the samples with the SiH_4+NH_3 treatment than that with the SiH_4 only treatment.

The higher D_{it} with SiH_4+NH_3 treatment is likely to be related to NH_3 and its dissociation: Partial dissociation of NH_3 into N_2 and H_2 occurs at above 200 °C, and dissociation of NH_3 on a Si surface to produce radicals such as NH, NH_2, and H has been observed at temperatures as low as -173 °C [103]-[104]. H could possibly diffuse into GaN during SiH_4+NH_3 treatment, but released in subsequent annealing steps to result in hydrogen-related defects in the interfacial layer [105]-[106].

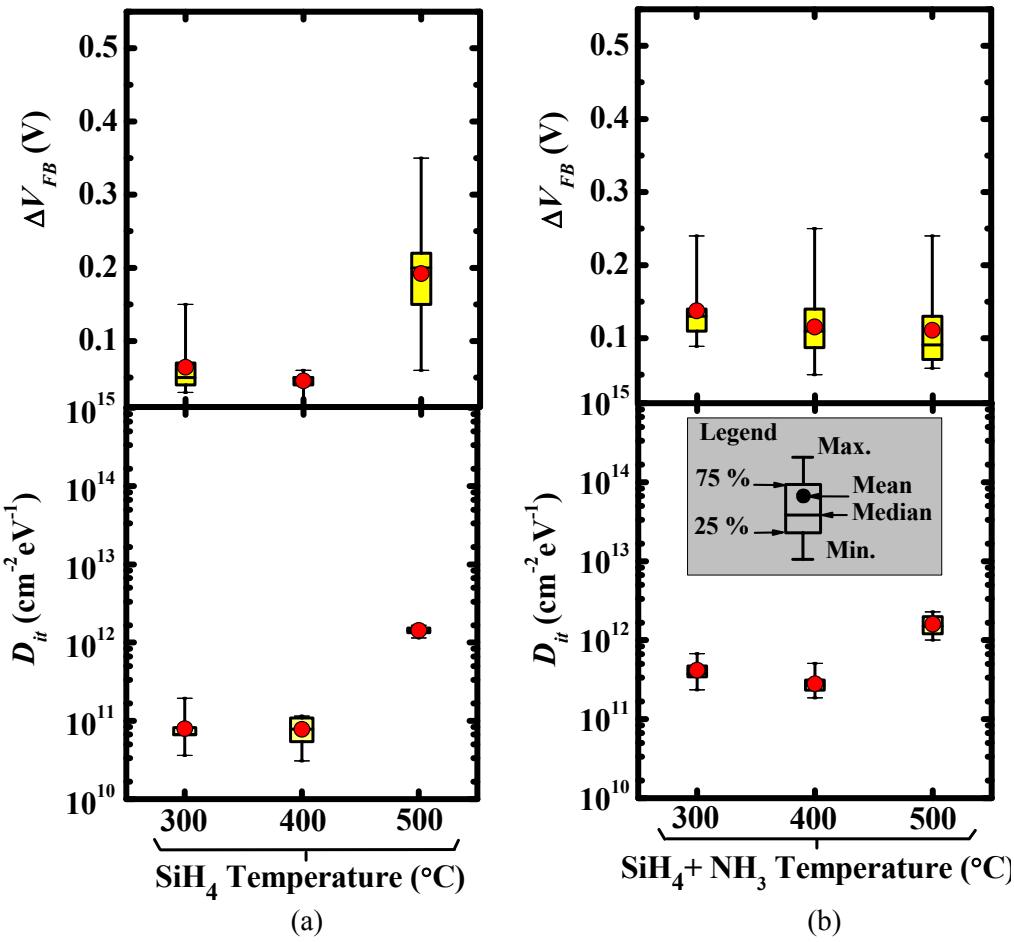


Fig. 2.7. The density of interface states D_{it} and the flat-band voltage shift ΔV_{FB} observed when the characterization frequency was increased from 10 to 500 kHz as functions of the SiH_4 or SiH_4+NH_3 treatment temperature. The vacuum anneal condition was fixed at 300 ºC for 1 minute, and the samples were subsequently treated in (a) SiH_4 or in (b) SiH_4+NH_3 at various temperatures from 300 ºC to 500 ºC. There are ten devices in each experimental split.

2.3 Detailed Characterization of Interface State Density

Room temperature capacitance-voltage (*C-V*) characterization technique used for silicon is inadequate for an elaborate study of the interface between high-*k* dielectric and GaN, such as the extraction of D_{it} over a large range of energy within the bandgap. The large E_G of 3.4 eV for GaN leads to a characteristic response time constant for mid-gap interface traps to be much larger than the usual time constant observed in silicon. Since the characteristic response time constant decreases with increasing temperature, one needs to select a higher characterization temperature to obtain an appropriate response time for GaN case. Therefore, the density of the interface traps located at near mid-gap of GaN can be measurable by a proper choice of the measurement temperature [107].

2.3.1 Need for Electrical Characterization at an Elevated Temperature

The characteristic emission time τ_e with which a trapped charge is emitted from a trap state of energy E_t is given by [107]

$$\tau_e = 1/(\sigma_{cro} v_{th} N) e^{\Delta E / kT}, \qquad (2.1)$$

where ΔE is the energy difference between the majority carrier band edge (conduction or valence band) and E_t, k is the Boltzmann constant, T is the characterization temperature, σ_{cro} is the capture cross section of the trap state, v_{th} is the thermal velocity of the majority charge carriers, and N is the density of states in the majority carrier band. σ_{cro}, v_{th}, and N are all temperature dependent [108].

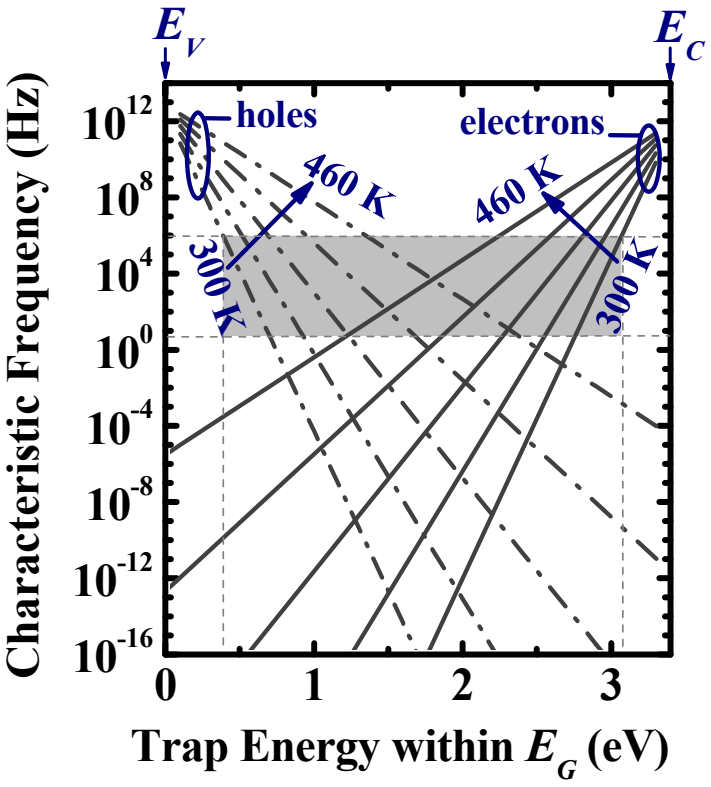


Fig. 2.8. Characteristic response frequencies f_{res} of trapped charge carriers (solid lines for electrons and dash-dot lines for holes) in GaN, at various temperatures from 300 K to 460 K in steps of 40 K, as a function of trap energy E_t with respect to the valence band edge E_V. The position of the conduction band edge E_C is also indicated. The horizontal dashed lines cover the usual frequency range of 3 kHz to 1 MHz commonly available in characterization equipment. The gray region indicates the energy range for which interface state density D_{it} can be measured.

Fig. 2.8 shows the characteristic response frequency $f_{res} = 1/(2\pi\tau_e)$ for electrons (solid line) and holes (dash-dot line) in GaN as a function of E_t taken with respect to the valence band edge E_V at various temperatures. For example, traps located at 0.4 eV below E_C have a characteristic response frequency f_{res} of 100 kHz, and these traps can be probed using a single frequency method for rapid characterization as described in Section 2.2. The horizontal dashed lines enclose the frequency range (3 kHz to 1 MHz) generally available in the instruments for *C-V* measurements, such as Agilent 4284A. Trap states with characteristic response frequencies within this range will contribute to a frequency dependent *C-V* component in the measurement.

Fast trap states with high characteristic frequencies would not produce the frequency-dependent component, and slow trap states with low characteristic frequencies are too sluggish to respond.

At room temperature (300 K), interface trap states lying between 0.44 and 0.62 eV or between 2.90 and 3.10 eV above E_V can be probed using the MOS structure formed on p- or n- type GaN, respectively (Fig. 2.8). Interface trap states near the mid-gap have very low characteristic response frequencies for both electrons and holes at room temperature. Consequently, the mid-gap states lying between 0.62 and 2.9 eV above E_V are not accessible to *C-V* measurement at room temperature. One method to measure the interface trap states near the mid-gap is to thermally activate them using an elevated temperature, so that their characteristic response frequencies f_{res} lie within the accessible frequency range. Fig. 2.8 shows that the interface states near the mid-gap of GaN are accessible to measurements when the measurement temperature is increased to up 460 K.

2.3.2 Method of Extracting Interface State Density [109]

The GaN MOS capacitor can be modeled by the circuit shown in Fig. 2.9 (a), which shows the contribution from the gate oxide capacitance C_{ox}, the capacitance of the depletion region C_d, the capacitance C_{it} and resistance R_{it} of the interface states, as well as the series resistance R_{ser}. C_d in parallel with the series combination of C_{it} and R_{it} can be replaced by the combination of a parallel capacitance C_p and a parallel resistance R_p [Fig. 2.9 (b)]. The interface state density D_{it} can then be calculated from the measurement data obtained using the conductance method. Electrical characterization was

performed on GaN MOS capacitors to obtain the measured capacitance C_m and conductance G_m based on the model in Fig. 2.9 (d). The presence of series resistance R_{ser} in the device structure is then accounted for or extracted. R_{ser} extraction is done using the measured accumulation conductance G_{ma} and the measured accumulation capacitance C_{ma} from a capacitor biased in the accumulation at a measurement frequency f of 1 MHz:

$$R_{ser} = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2}, \tag{2.2}$$

where ω is the angular frequency, and $\omega = 2\pi f$. With the extracted value of R_{ser}, the corrected capacitance C_c and corrected conductance G_c [Fig. 2.9 (c)] can be obtained using [109]

$$C_c = \frac{[G_m^2 + \omega^2 C_m^2]C_m}{a^2 + \omega^2 C_m^2}, \tag{2.3}$$

$$G_c = \frac{[G_m^2 + \omega^2 C_m^2]a}{a^2 + \omega^2 C_m^2}, \text{ and } \quad a = G_m - [G_m^2 + \omega^2 C_m^2]R_{ser}. \tag{2.4}$$

Thus giving the circuit model as shown in Fig. 2.9 (c) for the GaN MOS capacitor.

Next, de-embedding is done to account for the presence of C_{ox}, and the parallel conductance G_p is extracted from C_c and G_c using [Fig. 2.9 (b)]

$$C_{ox} = C_{ma}[1 + (\frac{G_{ma}}{\omega C_{ma}})^2], \tag{2.5}$$

$$G_p = \frac{\omega^2 G_c C_{ox}^2}{G_c^2 + \omega^2 (C_{ox} - C_c)^2}. \tag{2.6}$$

From a series of conductance measurements made at a given temperature over a range of measurement frequencies f, and by using Equations (2.2) to (2.6), a plot of G_p/ω versus angular frequency ω can be generated, from which one

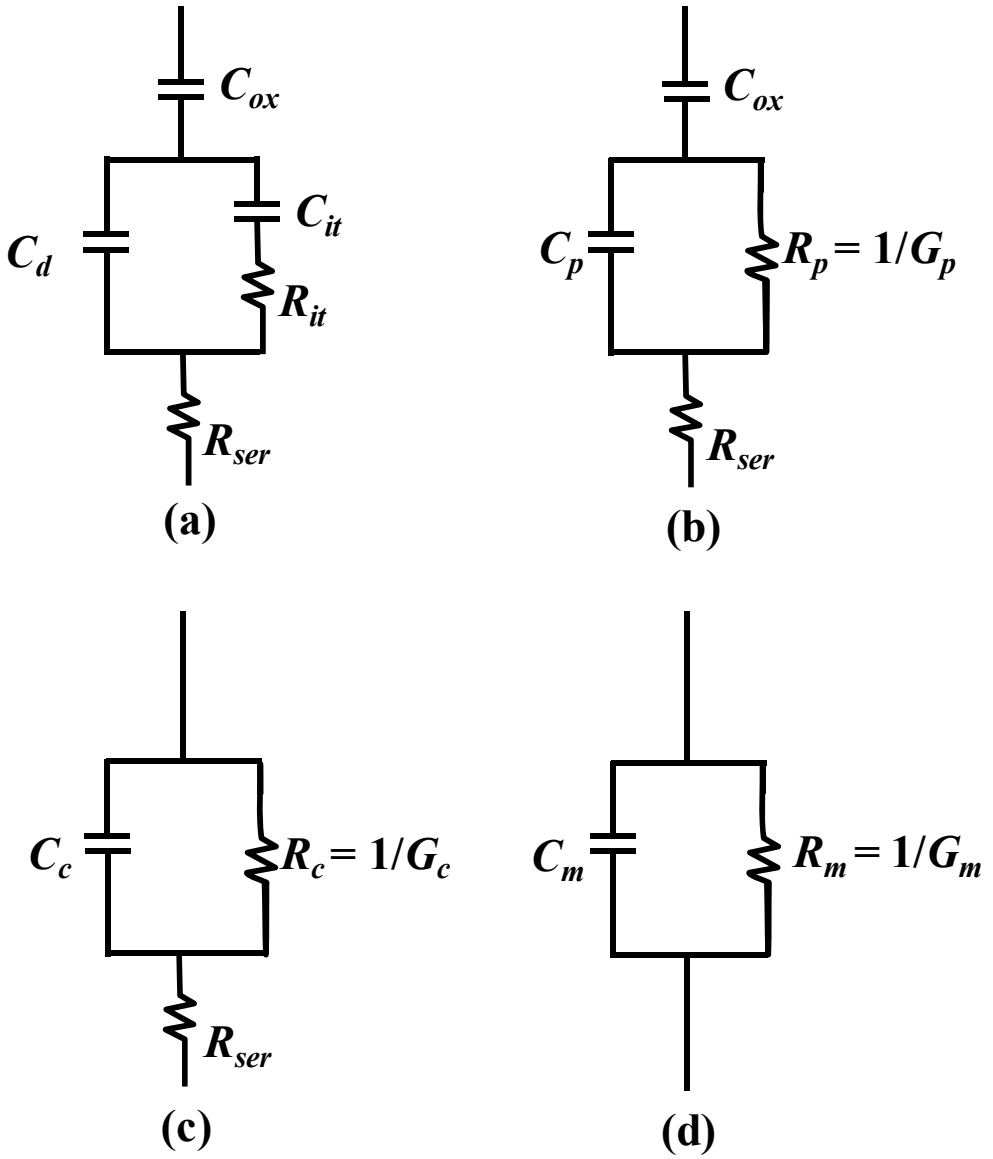


Fig. 2.9. (a) Equivalent circuit of the metal-oxide-semiconductor structure, showing the oxide capacitance C_{ox}, the capacitance of the depletion region C_d, the capacitance C_{it} and resistance R_{it} of the interface states, and the series resistance R_{ser}. (b) A simplified circuit of (a) with C_d, C_{it}, and R_{it} replaced by C_p and R_p. (c) A simplified circuit that is equivalent to (b). (d) An equivalent circuit showing the measured capacitance C_m and measured conductance G_m obtained during *C-V* characterization.

obtains the maximum value of G_p/ω, $(G_p/\omega)_{max.}$ D_{it} is then extracted using [110]

$$D_{it} = \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{\max}, \tag{2.7}$$

where A is the area of the MOS capacitor and q is the electronic charge.

A non-negligible gate leakage current, which was not accounted for in the present model, could be a possible source of error in the D_{it} extraction. For capacitors with a large gate leakage current due to the use of an ultrathin gate dielectric, an improved model that accounts for gate leakage may be used [111]. In this work, a thick gate dielectric was used to avoid the gate leakage issue, and the gate leakage current level is below 5×10^{-8} A/cm^2 at V_{FB} −1 V, where V_{FB} is the flat-band voltage of the capacitor.

2.3.3 Comparison of *In Situ* Passivation Methods

The capacitance C_m and conductance G_m between the gate and the substrate terminals of the TaN/HfAlO/n-GaN capacitors were measured from 3 kHz to 1 MHz at 300 K and 460 K for the control sample, the sample with *in situ* SiH_4+NH_3 passivation (300 °C vacuum anneal, 400 °C SiH_4+NH_3 treatment), and the sample with *in situ* SiH_4 passivation (300 °C vacuum anneal, 400 °C SiH_4 treatment). The results of the measurements are shown in Fig. 2.10 and Fig. 2.11. In each graph of Fig. 2.10 and Fig. 2.11, the data obtained at 300 K is plotted on the left, and the data obtained at 460 K is plotted on the right. After taking R_{ser} into consideration, the corrected capacitance C_c and the corrected conductance G_c were obtained based on C_m and G_m using Equations (2.3)-(2.5), and plotted in Fig. 2.12 and Fig. 2.13,

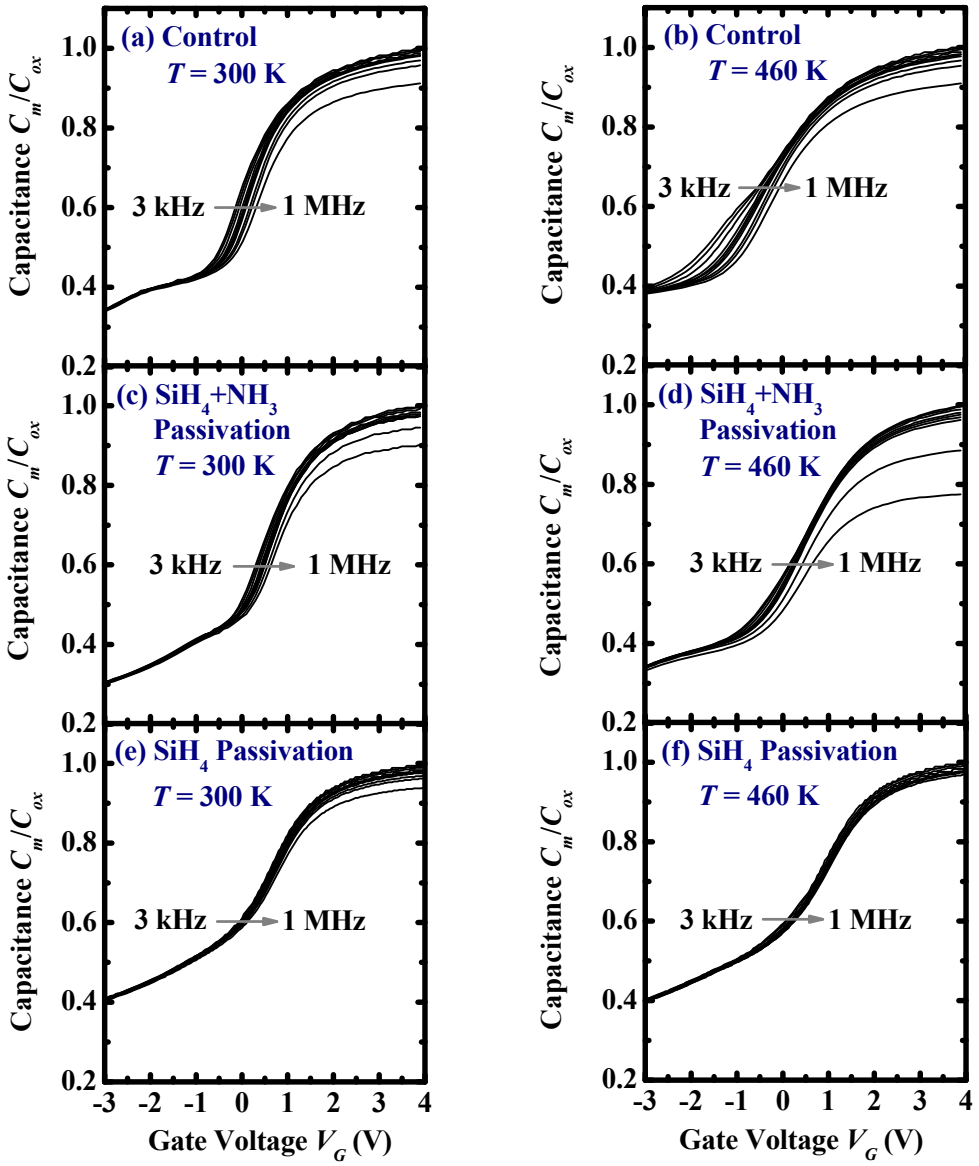


Fig. 2.10. Measured normalized capacitance-gate voltage curves (C_m/C_{ox} versus V_G) of the control sample obtained at characterization temperatures of (a) 300 K and (b) 460 K. The control did not undergo any vacuum anneal or surface treatment. C_m/C_{ox} versus V_G curves of samples which received *in situ* 300 °C vacuum anneal and 400 °C SiH_4+NH_3 treatment, and characterized at (c) 300 K and (d) 460 K. Similar measurements at (e) 300 K and (f) 460 K were performed for samples which received *in situ* 300 °C vacuum anneal and 400 °C SiH_4 treatment. For each plot, ten characterization frequencies (3, 5, 10, 30, 50, 70, 100, 300, 500, and 1000 kHz) were used.

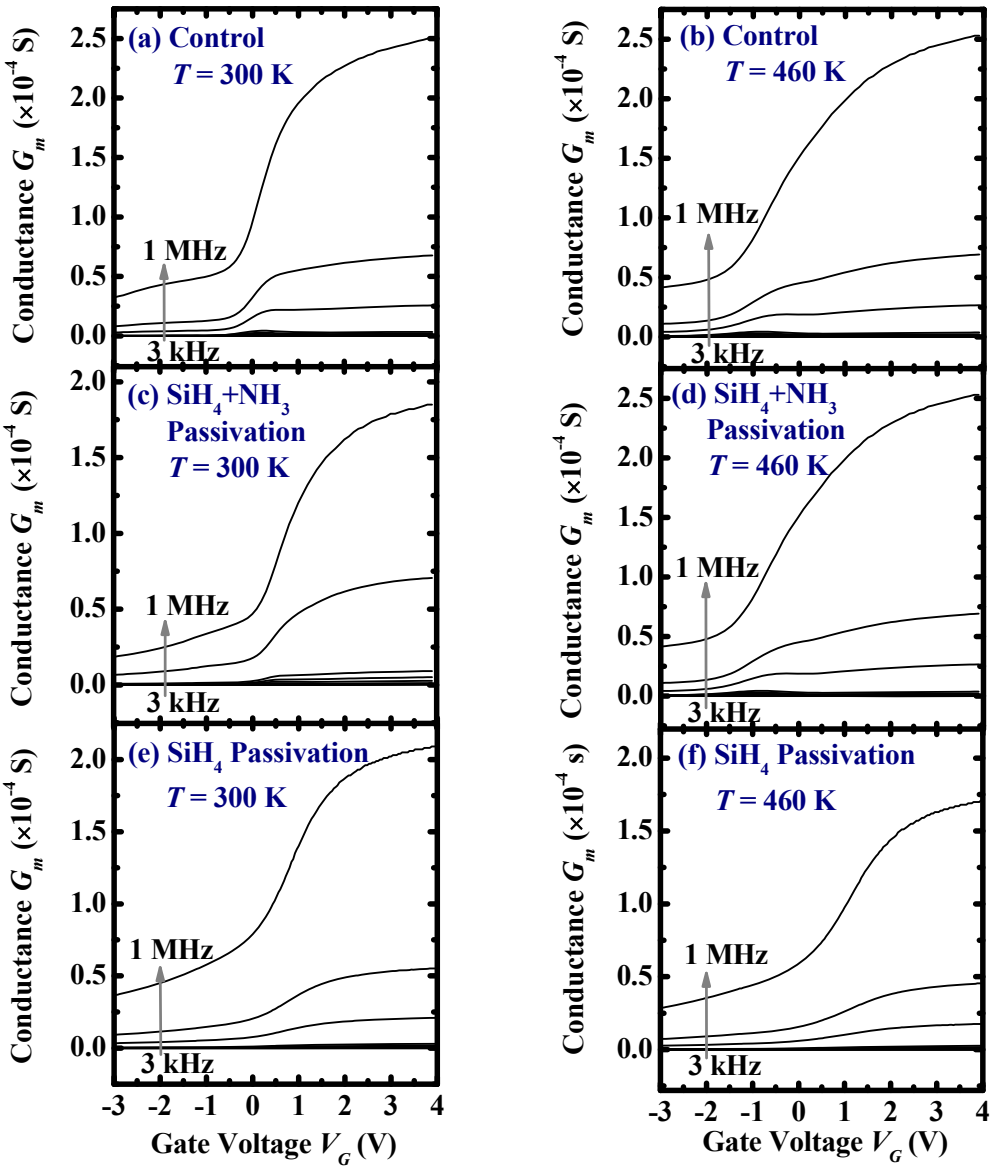


Fig. 2.11. Measured conductance-gate voltage (G_m-V_G) curves of the control sample at characterization temperatures of (a) 300 K and (b) 460 K. G_m-V_G curves of samples which received *in situ* 300 °C vacuum anneal and 400 °C SiH_4+NH_3 treatment, characterized at (c) 300 K and (d) 460 K. Similar measurements at (e) 300 K and (f) 400 K were performed for samples which received *in situ* 300 °C vacuum anneal and 400 °C SiH_4 treatment. For each plot, ten characterization frequencies (3, 5, 10, 30, 50, 70, 100, 300, 500, and 1000 kHz) were used.

respectively, for all the three samples. The frequency dependence of the accumulation capacitance in the C_m-V_G plots, a manifestation of R_{ser}, is negligible in the corrected C_c-V_G plots (Fig. 2.12).

Fig. 2.12 (a) shows the corrected capacitance-voltage (C_c-V_G) plot for the control sample measured at 300 K. The capacitance response observed in the transition region between accumulation and depletion is caused by shallow traps at the HfAlO/GaN interface. With *in situ* SiH_4+NH_3 passivation, as shown in Fig. 2.12 (c), a smaller frequency dispersion in the C_c-V_G plot at 300 K is observed, and there is reduced carrier response in the depletion region. This is due to the reduced density of shallow interface traps, as compared to that of the control sample. The frequency dispersion in the C_c-V_G plot is the smallest for the sample with *in situ* SiH_4 passivation [Fig. 2.12 (e)].

Traps located near the mid-gap can be accessible to the measurement at a higher measurement temperature of 460 K. Compared with Fig. 2.12 (a), the C_c-V_G plot for the control sample at 460 K [Fig. 2.12 (b)] shows an increased capacitance or a bump in the depletion region at low frequencies. This is related to deeper interface states in the bandgap, and illustrates the importance of high temperature characterization for a detailed study of the interface state density at the dielectric-GaN interface.

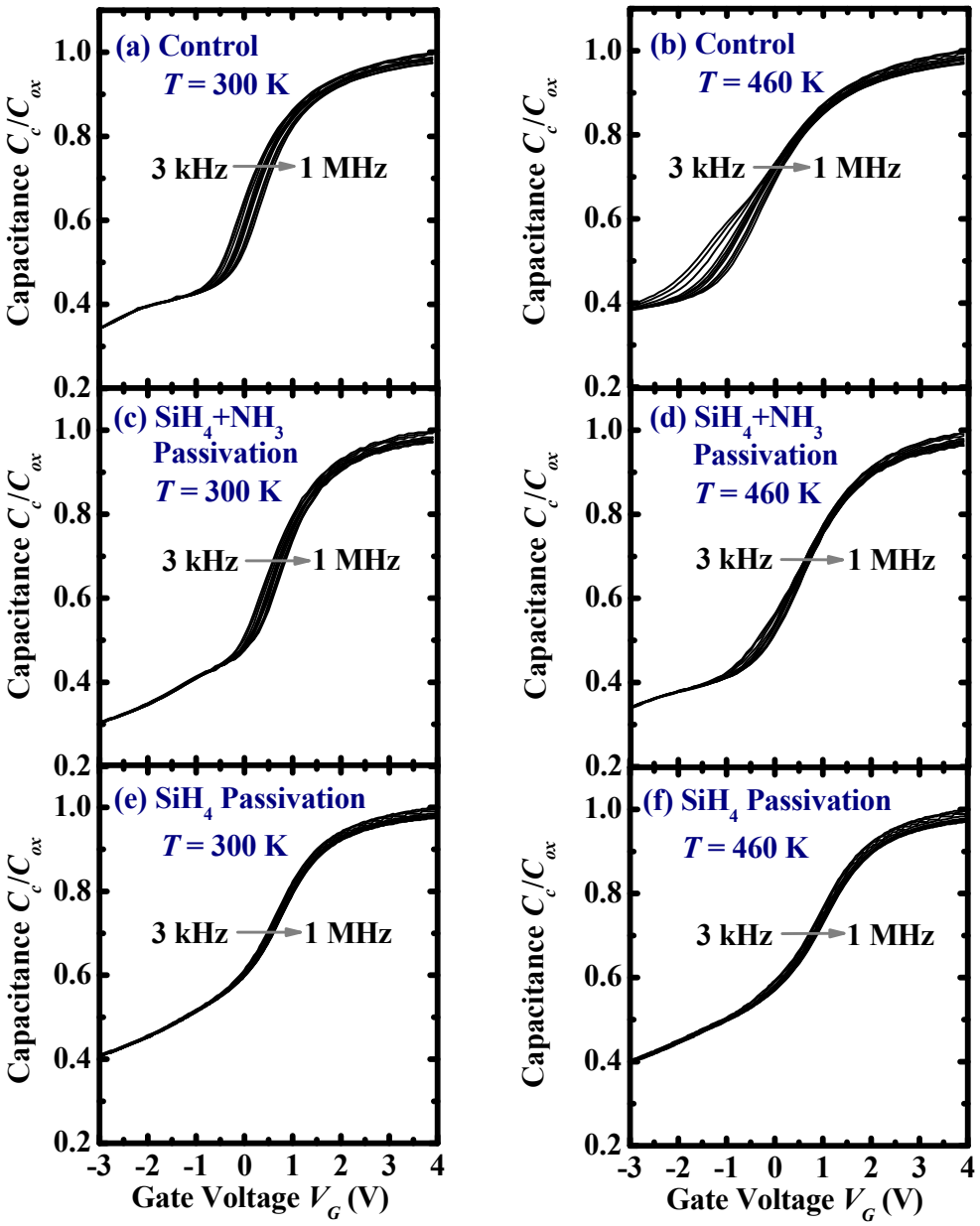


Fig. 2.12. Corrected normalized capacitance-gate voltage curves (C_c/C_{ox}-V_G) of the control sample at characterization temperatures of (a) 300 K and (b) 460 K. C_c/C_{ox}-V_G curves for samples which received *in situ* 300 °C vacuum anneal and 400 °C SiH_4+NH_3 treatment, characterized at (c) 300 K and (d) 460 K. Similarly, C_c/C_{ox}-V_G curves of samples which received *in situ* 300 °C vacuum anneal and 400 °C SiH_4 treatment, characterized at (d) 300 K and (e) 460 K. For each plot, ten characterization frequencies (3, 5, 10, 30, 50, 70, 100, 300, 500, and 1000 kHz) were used.

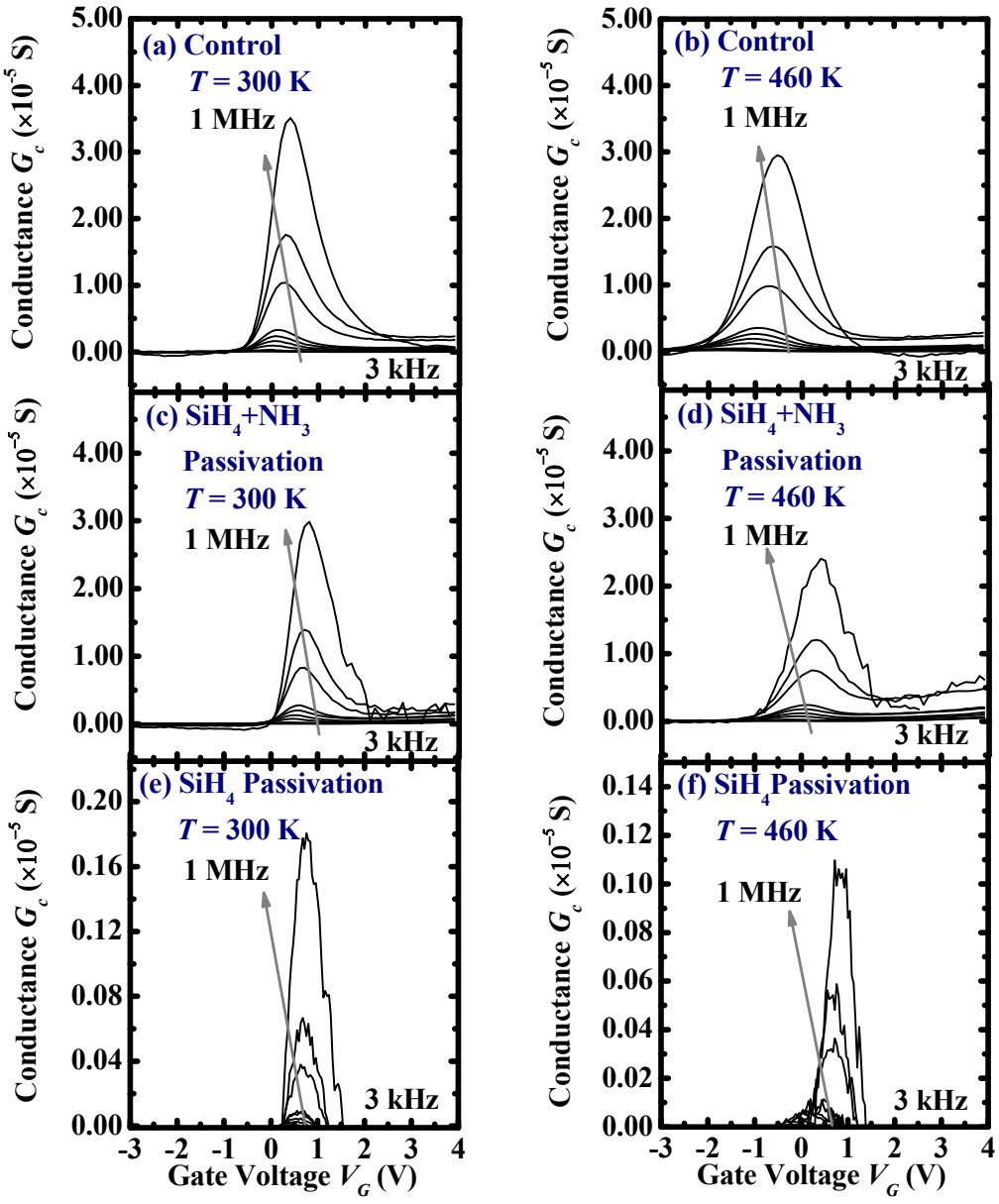


Fig. 2.13. Corrected conductance-gate voltage curves (G_c-V_G) of the control sample at characterization temperatures of (a) 300 K and (b) 460 K. G_c-V_G curves of the samples which received *in situ* 300 °C vacuum anneal and 400 °C SiH_4+NH_3 treatment, characterized at (c) 300 K and (d) 460 K. Similarly, G_c-V_G curves of the samples which received *in situ* 300 °C vacuum anneal and 400 °C SiH_4 treatment, characterized at (d) 300 K and (e) 460 K. For each plot, ten characterization frequencies (3, 5, 10, 30, 50, 70, 100, 300, 500, and 1000 kHz) were used.

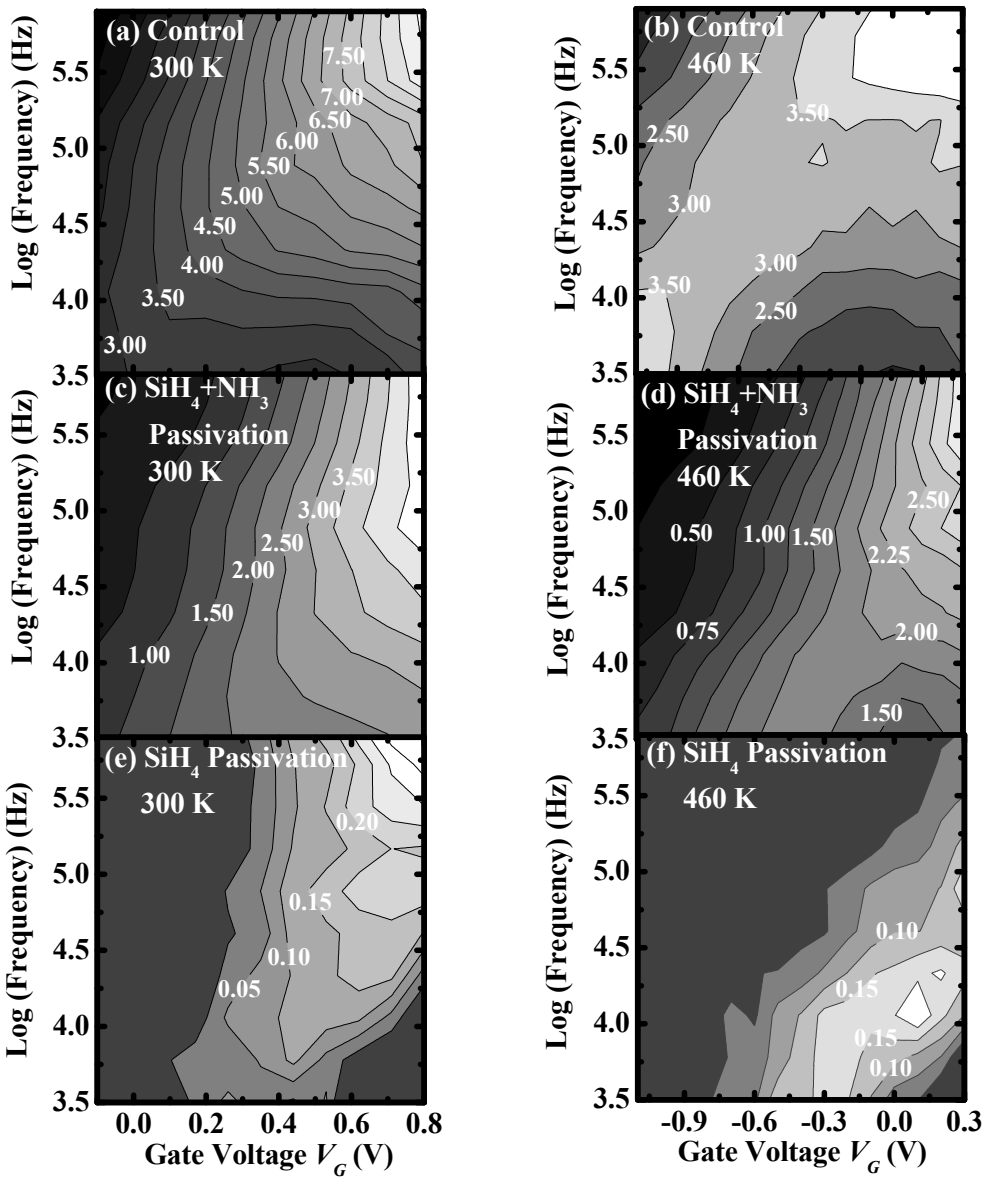


Fig. 2.14. $G_p(\times 10^{-11})/\omega$ contours as a function of frequency (log scale) and gate voltage V_G for the control sample at characterization temperatures of (a) 300 K and (b) 460 K. $G_p(\times 10^{-11})/\omega$ contours as a function of frequency (log scale) and gate voltage V_G for samples which received *in situ* 300 °C vacuum anneal and 400 °C SiH_4+NH_3 treatment at characterization temperatures of (c) 300 K and (d) 460 K. Similarly, $G_p(\times 10^{-11})/\omega$ contours as a function of frequency (log scale) and gate voltage V_G for samples which received *in situ* 300 °C vacuum anneal and 400 °C SiH_4 treatment at characterization temperatures of (e) 300 K and (f) 460 K.

Compared with the data obtained at 300 K in Fig. 2.12 (e), the C_c-V_G curves obtained at 460 K [Fig. 2.12 (f)] for the sample with *in situ* SiH_4 passivation show no observable change in the frequency dispersion, which is consistently low. This indicates better interfacial quality as compared to the control or the sample with *in situ* SiH_4+NH_3 passivation.

To probe further, the oxide capacitance C_{ox} was de-embedded from the C_c data, and the parallel conductance G_p was extracted at each bias using Equation (2.5) and (2.6). The maximum of the G_p/ω versus ω plot at each bias is proportional to the D_{it} at the corresponding energy in the bandgap. In order to have a clear view of G_p/ω as a function of frequency and gate voltage, the G_p/ω contours were plotted for all the three samples, as shown in Fig. 2.14. The G_p/ω peaks at various gate voltages are obtained from these G_p/ω contours, and the corresponding values of D_{it} were then calculated using Equation (2.7). Furthermore, D_{it} as a function of energy in the GaN bandgap was extracted from near E_C to mid-gap for all the three samples, as shown in Fig. 2.15. At 0.4 eV below E_C, the extracted D_{it} in Fig. 2.15 for the sample with *in situ* 300 °C vacuum anneal and 400 °C SiH_4 treatment is ~ 1×10^{11} cm^{-2} eV^{-1}, which is similar to the value obtained from the single frequency method shown in Fig. 2.6 (a). For the sample with *in situ* 300 °C vacuum anneal and 400 °C SiH_4+NH_3 treatment, the D_{it} value at 0.4 eV below E_C in Fig. 2.15 is ~ 6.6×10^{11} cm^{-2} eV^{-1}, which is higher than ~ 2×10^{11} cm^{-2} eV^{-1} obtained using the single frequency method in Fig. 2.6 (b). This could be due to the traps with various characteristic frequency at this specific energy level.

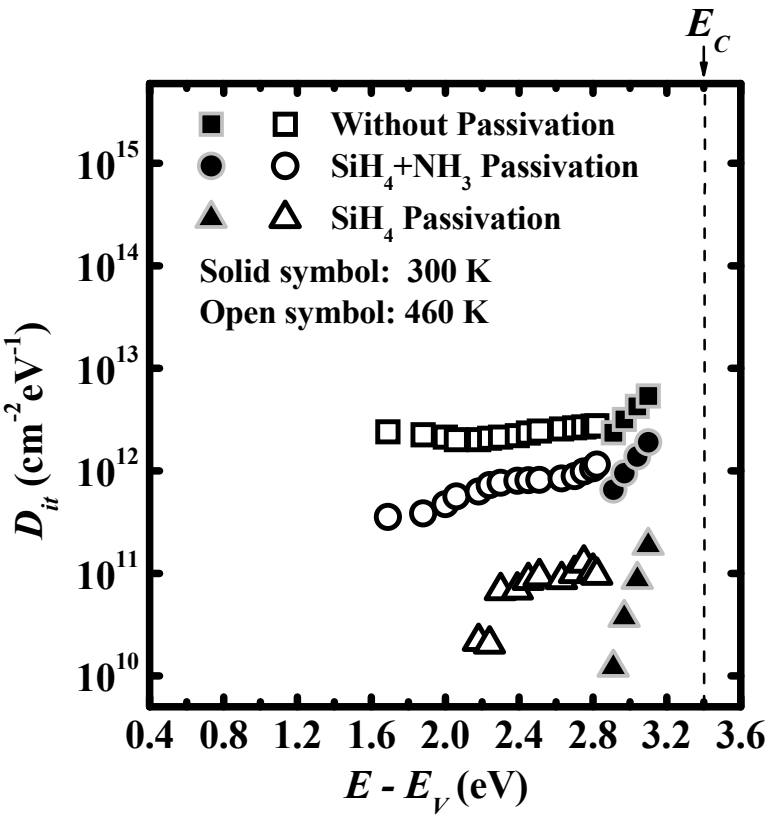


Fig. 2.15. Interface state density D_{it} from near E_C to mid-gap for the control sample, sample with *in situ* 300 ºC vacuum anneal and 400 ºC SiH_4+NH_3 treatment, and sample with *in situ* 300 ºC vacuum anneal and 400 ºC SiH_4 treatment, extracted using the conductance method at 300 K and 460 K with series resistance correction.

As shown in Fig. 2.15, D_{it} of ~ 2.0×10^{12} cm^{-2} eV^{-1} was measured at mid-gap for the control sample. D_{it} for the samples with *in situ* SiH_4+NH_3 passivation and with *in situ* SiH_4 passivation are reduced by 80 % to ~ 4.0×10^{11} cm^{-2} eV^{-1}, and by 2 orders of magnitude to ~ 2.0×10^{10} cm^{-2} eV^{-1} at mid-gap, respectively, as compared with the control sample.

2.4 Summary

In summary, two novel *in situ* surface passivation techniques based on *in situ* vacuum anneal and SiH_4+NH_3 or SiH_4 treatment for GaN in a MOCVD tool were demonstrated using TaN/HfAlO/GaN capacitors. The optimum temperature for vacuum anneal was 300 °C, because this temperature is not only suitable for desorption of contaminants on GaN surface, but also low enough to prevent surface deterioration of GaN. Due to the possible hydrogen-related defects from NH_3 dissociation, GaN surface with SiH_4 treatment only achieves better interface quality, as compared to that of GaN surface with SiH_4+NH_3 treatment. The effects of both vacuum anneal temperature and SiH_4 or SiH_4+NH_3 treatment temperature on the GaN/HfAlO interface quality were studied. In addition, interface state densities of the control sample, the sample with *in situ* 300 °C vacuum anneal and 400 °C SiH_4+NH_3 treatment, and the sample with *in situ* 300 °C vacuum anneal and 400 °C SiH_4 treatment were determined by using the conductance method at 300 and 460 K with series resistance correction. It was found that *in situ* 300 °C vacuum anneal and 400 °C SiH_4 treatment can achieve a better interface quality ($D_{it} \sim 2.0 \times 10^{10}$ cm^{-2} eV^{-1} at mid-gap), as compared with *in situ* 300 °C vacuum anneal and 400 °C SiH_4+NH_3 treatment.

Chapter 3

AlGaN/GaN MOS-HEMTs with *In Situ* Vacuum Anneal and SiH_4 Treatment

3.1 Introduction

As discussed in Chapter 2, owing to the advantages of gallium nitride material properties, AlGaN/GaN high-electron-mobility transistors (HEMTs) are promising for application in high power switching circuits and high frequency monolithic microwave integrated circuits [112]-[116]. Since the first demonstration of AlGaN/GaN HEMTs, rapid progress has been made in the development of AlGaN/GaN HEMTs in both power devices and microwave devices [12]. AlGaN/GaN-on-sapphire HEMTs with a thick poly-AlN passivation layer have realized a high breakdown voltage V_{BR} of 8300 V with an on-state resistance R_{on} of 186 mΩ·cm^2 [117]. AlGaN/GaN-on-silicon MOS-HEMTs recently achieved a breakdown voltage V_{BR} of 800 V with an on-state resistance R_{on} of 3 mΩ·cm^2 using a silicon complementary metal-oxide-semiconductor (CMOS) compatible gold-free process [81]. As for microwave devices, GaN-based HEMTs have demonstrated a current-gain cutoff frequency up to 370 GHz and a maximum oscillation frequency of 400 GHz [118]-[120]. In addition, AlGaN/GaN HEMTs with high current density (> 1 A/mm), due to the large spontaneous and piezoelectric polarizations, have also been reported [85]. However, the conventional Schottky-gate AlGaN/GaN HEMTs typically suffer from a large gate leakage current density,

which may result in issues related to noise, power loss, lower breakdown voltage, and reliability [15], [121].

Insertion of a gate dielectric, such as HfO_2 [37], Al_2O_3 [28], and SiO_2 [43], can significantly reduce the gate leakage current density of AlGaN/GaN HEMTs. In addition, treatment on the AlGaN or GaN surface has also been intensively explored in many ways, such as treatment using $(NH_4)_2S_x$ [45], and gas plasma (O_2 [48], CF_4 [52], and N_2 [55]), to reduce the gate leakage current density. In Chapter 2, an *in situ* passivation technique comprising vacuum anneal (VA) and silane (SiH_4) treatment before the dielectric (HfAlO) deposition was demonstrated to be effective in reducing the density of interface states between HfAlO and GaN by using a TaN/HfAlO/n-GaN MOS capacitor test structure [75]-[77].

In this Chapter, *in situ* VA and SiH_4 treatment was incorporated in the fabrication of AlGaN/GaN metal-oxide-semiconductor HEMTs (MOS-HEMTs) to enhance the device electrical performance. X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM) were employed to study the surface chemistry of the AlGaN surface with and without the *in situ* VA and SiH_4 treatment. Electrical characterization was performed on the AlGaN/GaN MOS-HEMTs with and without *in situ* VA and SiH_4 treatment. As compared to the control devices, the devices with *in situ* VA and SiH_4 treatment showed reduced gate leakage current I_G, increased current on/off, I_{on}/I_{off}, ratio, and improved sub-threshold swing S.

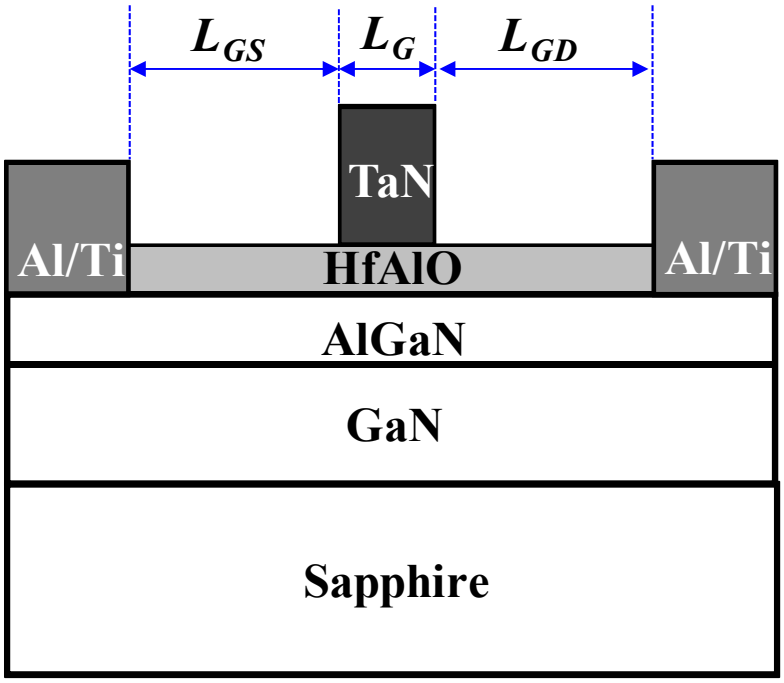
3.2 Device Fabrication

The devices were fabricated on an undoped $Al_{0.25}Ga_{0.75}N$ (20 nm) / GaN (3 μm) heterostructure, which was purchased from Nippon Telegraph and Telephone Advanced Technology (NTT-AT) and grown by metal-organic chemical vapor phase deposition (MOCVD) on a *c*-plane (0001) sapphire substrate with a diameter of 2 inches. From Hall measurement, this heterostructure had an electron mobility of 1800 $cm^2/V{\cdot}s$, and a two-dimensional electron gas (2-DEG) density of ~ 1.0×10^{13} cm^{-2}.

The process flow employed to fabricate the AlGaN/GaN MOS-HEMTs is shown in Fig. 3.1 (a). Mesa isolation was first realized by Cl_2 (10 sccm) / BCl_3 (20 sccm) reactive ion etching (RIE) using an inductive-coupled plasma (ICP) system with a chamber pressure of 5 mTorr at a chuck temperature of 6 ºC. The etched mesa depth was around 45 nm, which is sufficient to ensure device-to-device isolation. Pre-gate cleaning for all the samples comprised a 2-minute acetone and a 3-minute isopropanol degreasing step, followed by surface native oxide removal using dilute HCl ($HCl:H_2O$ = 1:1) for 10 minutes and *ex situ* surface passivation using an undiluted $(NH_4)_2S$ solution for 30 minutes at room temperature [122]. The wafer was then loaded into a multi-chamber MOCVD gate cluster system for *in situ* surface passivation and HfAlO deposition. A photograph of this multi-chamber MOCVD gate cluster system is shown Fig. 3.2. This gate cluster system is equipped with a high vacuum transfer module at a pressure of 1×10^{-6} Torr to prevent wafers from exposure to a low vacuum or the atmosphere. In process module 1, the wafer

- 2 inch AlGaN/GaN epi wafer on sapphire substrate
- Mesa formation using RIE (Cl_2/BCl_3)
- Pre-gate cleaning:
  Acetone, Isopropanol, HCl, $(NH_4)_2S$
- *In situ* passivation:
  Vacuum anneal and SiH_4 treatment
- HfAlO deposition and PDA
- Metal gate deposition and gate patterning
- Contact patterning and Al/Ti deposition by E-beam evaporator
- Lift-off process and ohmic alloying (650°C, 30s)

(a)



(b)

Fig. 3.1. (a) Process flow for the fabrication of the AlGaN/GaN MOS-HEMT with *in situ* VA and SiH_4 treatment. A gate-first fabrication approach was used in this work. (b) Schematic of the AlGaN/GaN MOS-HEMT structure.

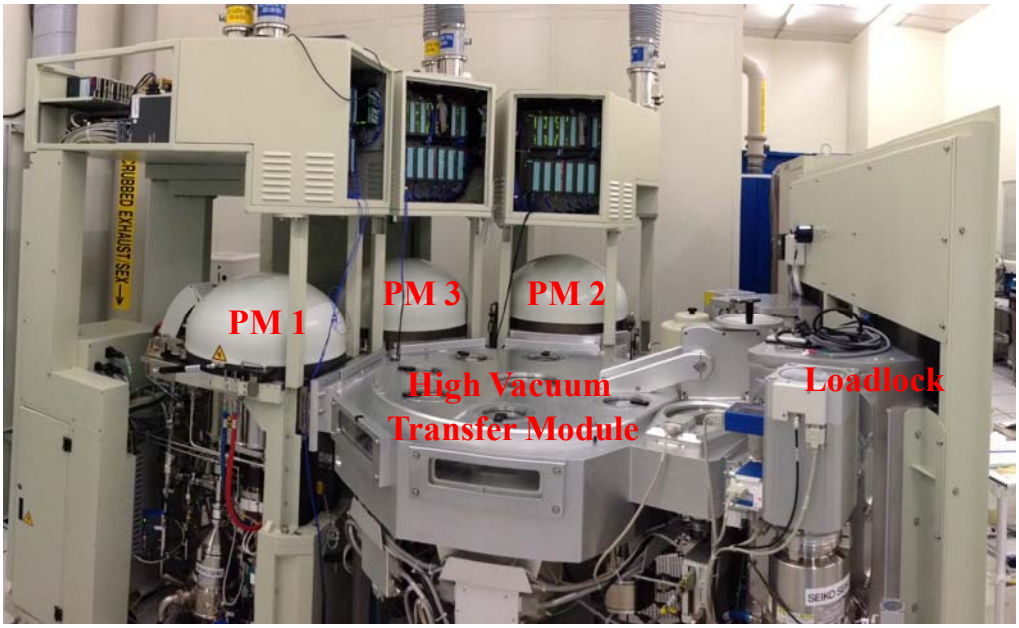


Fig. 3.2. Photograph of a multi-chamber MOCVD gate cluster system: process module 1 (PM 1) for vacuum anneal, process module 2 (PM 2) for SiH_4 treatment, and process module 3 (PM 3) for HfAlO deposition. Wafers can be transferred among these three PM chambers through a transfer module, which was kept at a high vacuum (1×10^{-6} Torr) level. A loadlock was used to load/unload the wafers for this MOCVD system.

was annealed at a temperature of 300 ºC for 60 s at a pressure of 1×10^{-6} Torr. After vacuum anneal (VA), the wafer was transferred to the process module 2 for SiH_4 treatment at a temperature of 400 ºC for 60 s at a pressure of 5 Torr. During the SiH_4 treatment, the flow rate of SiH_4 and N_2 were 60 and 250 sccm, respectively. Without breaking vacuum, the wafer was transferred to the process module 3 for the deposition of HfAlO (7 nm) using a $HfAl(MMP)_2(OiPr)_5$ liquid source. A post-deposition anneal (PDA) in N_2 ambient was then performed at 500 ºC for 60 s to improve the as-deposited HfAlO film quality [123].

TaN (100 nm) was deposited as a gate metal at a pressure of 3 mTorr by using a magnetron sputtering system. The DC power supply for the Ta target was 250 W, and the N_2 flow rate was 3 sccm. This was followed by a

gate photolithography and Cl_2-based plasma etching step of TaN (the flow rate of Cl_2 was 200 sccm, and the chamber pressure was 10 mTorr) for the gate electrode formation. After source/drain (S/D) contact lithography, the HfAlO in the contact regions was removed using dilute HF. A contact metal stack (71 nm of Al on 30 nm of Ti) was deposited using an electron beam (E-Beam) evaporator and patterned using a lift-off process. Finally, an alloying process in N_2 ambient was performed at 650 ºC for 30 s to form ohmic S/D contacts.

A schematic of the fabricated AlGaN/GaN MOS-HEMT in this work is shown in Fig. 3.1 (b). In this work, the gate length L_G of the fabricated AlGaN/GaN MOS-HEMT is 2 μm, and both the gate-to-source spacing, L_{GS}, and gate-to-drain spacing, $L_{GD,}$ are 5 μm. For comparison, control AlGaN/GaN MOS-HEMTs were also fabricated using the same process flow except that the *in situ* VA and SiH_4 treatment steps were skipped. Fig. 3.3 shows a cross-sectional TEM image of the TaN/HfAlO/AlGaN/GaN stack, where the thicknesses of the TaN layer, HfAlO layer, and AlGaN barrier layer are 100 nm, 7 nm, and 20 nm, respectively. As seen from the zoomed-in image of the left side of the gate stack, the sidewall of the TaN gate is normal to the surface of the AlGaN barrier layer, indicating the anisotropy of the gate etch process.

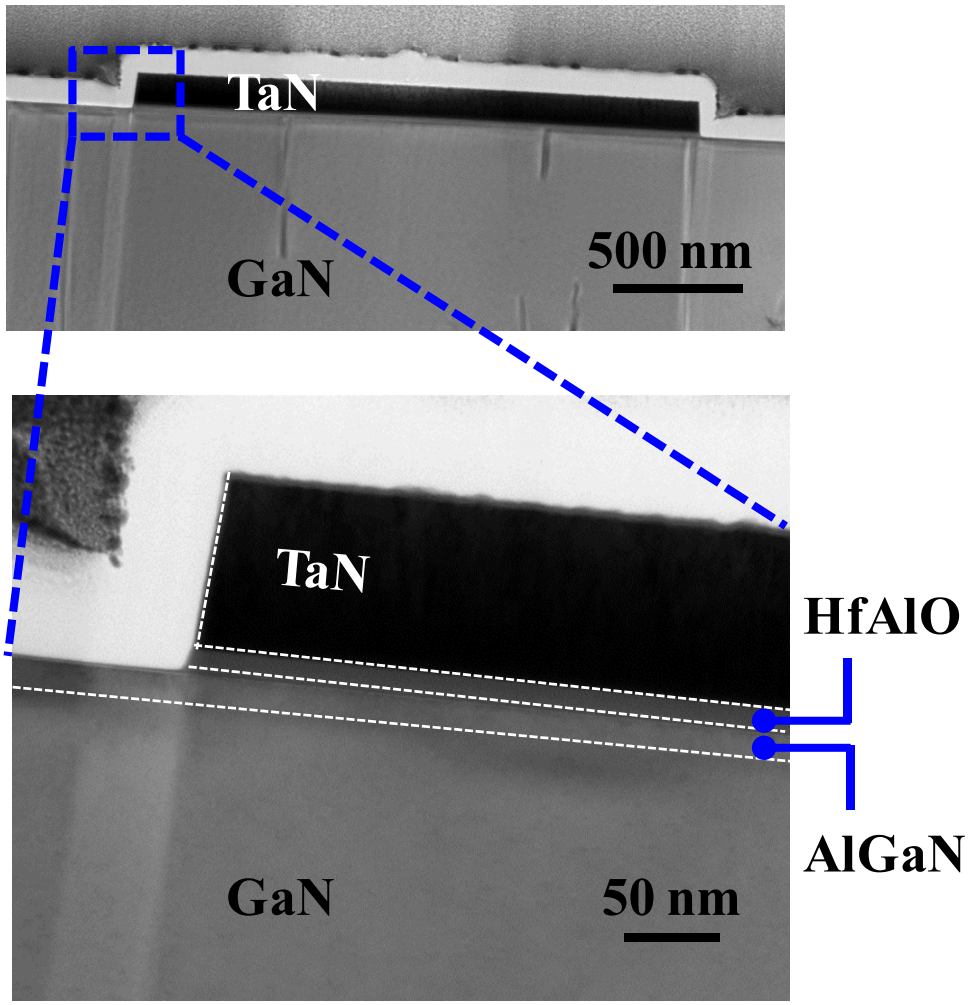


Fig. 3.3. Cross-sectional TEM image of TaN/HfAlO/AlGaN/GaN stack, where the thicknesses of the TaN layer, HfAlO layer, and AlGaN barrier layer are 100 nm, 7 nm, and 20 nm, respectively. As seen from the zoomed-in image of the left side of the gate, the sidewall of TaN gate is normal to the surface of AlGaN barrier layer, indicating the anisotropy of the gate etch process.

3.3 Results and Discussions

3.3.1 Material Characterization: XPS and TEM

To investigate the effect of *in situ* VA and SiH_4 treatment on the AlGaN surface, XPS was performed on two AlGaN/GaN samples deposited with a thin HfAlO (~ 1 nm) film. On the control sample, *in situ* VA and SiH_4 treatment were skipped. On the other sample, *in situ* VA and SiH_4 treatment

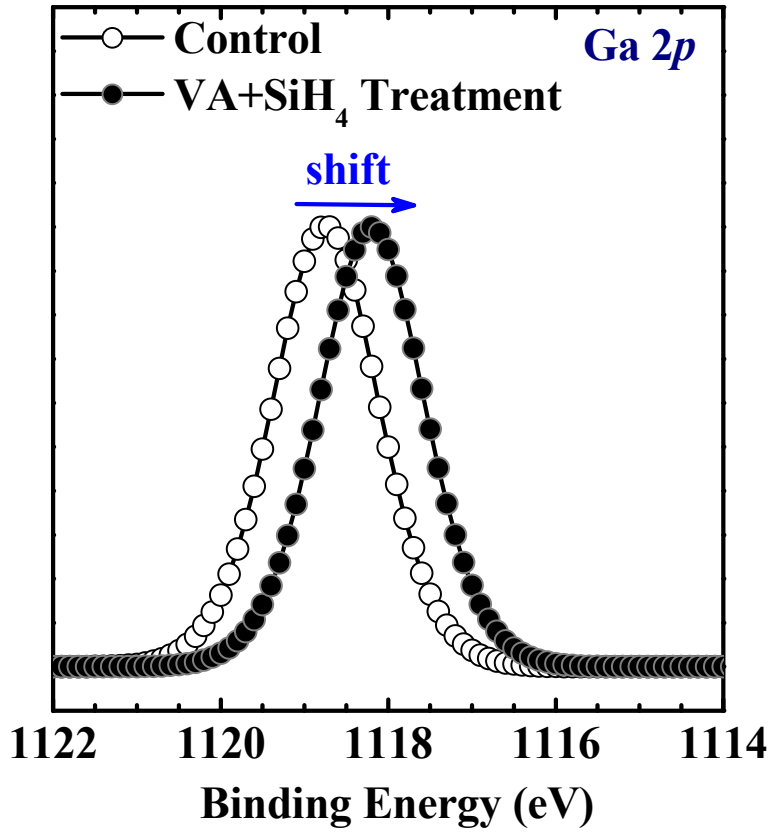


Fig. 3.4. XPS Ga 2*p* spectra of the two AlGaN/GaN samples deposited with a thin HfAlO (~1 nm) film. The values of the binding energy of the Ga 2*p* peak are 1118.2 and 1118.8 eV for the samples with and without *in situ* VA and SiH_4 treatment, respectively.

were performed at 300 ºC for 60 s and 400 ºC for 60 s, respectively, prior to the HfAlO deposition. The XPS Ga 2*p* and Ga 3*p* spectra of the two samples are shown in Fig. 3.4 and Fig. 3.5, respectively. As shown in Fig. 3.4, the binding energy of the Ga 2*p* peak for the sample with *in situ* VA and SiH_4 treatment is 1118.2 eV, which is lower than the binding energy of 1118.8 eV of the Ga 2*p* peak for the control sample. The approximate 0.6 eV reduction

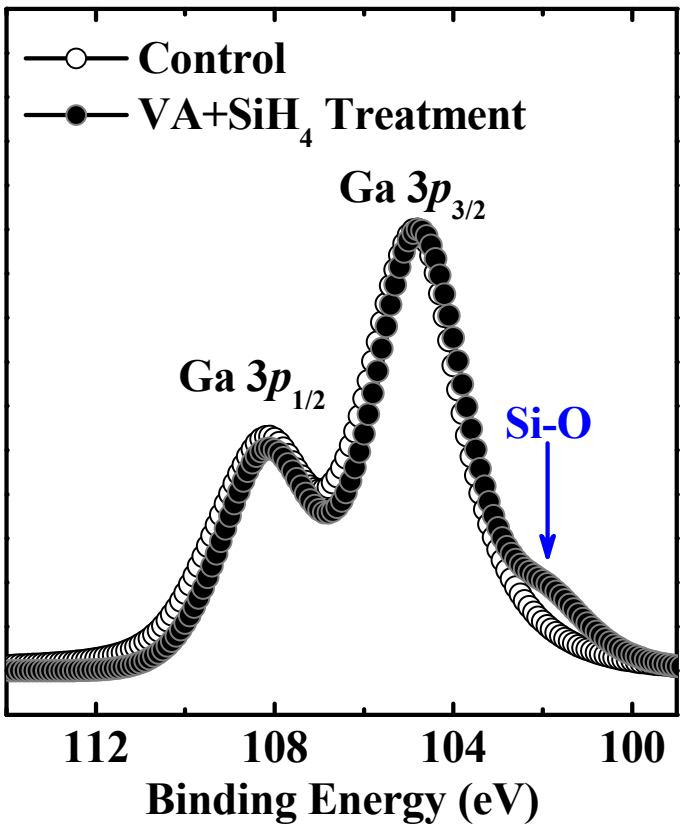


Fig. 3.5. XPS results showing the Ga 3*p* spectra of two AlGaN/GaN samples deposited with a thin HfAlO (~1 nm) film. The left shoulders of the Ga $3p_{3/2}$ and Ga $3p_{1/2}$ of the control sample are slightly broader than those of the sample with *in situ* VA and SiH_4 treatment, which indicates the reduction of Ga-O bond at AlGaN/HfAlO interface with *in situ* VA and SiH_4 treatment. A Si-O peak is detected for the sample with *in situ* VA and SiH_4 treatment.

of the Ga 2*p* binding energy of the sample with *in situ* VA and SiH_4 treatment is due to the reduction of the Ga-O bond at AlGaN/HfAlO interface. As shown in Fig. 3.5, the left shoulders of the Ga $3p_{3/2}$ and Ga $3p_{1/2}$ of the control sample are slightly broader than those of the sample with *in situ* VA and SiH_4 treatment, which indicates the reduction of Ga-O bond at AlGaN/HfAlO interface with *in situ* VA and SiH_4 treatment. In addition, the Si-O peak with a binding energy of 101.8 eV was detected for the sample with *in situ* VA and SiH_4 treatment.

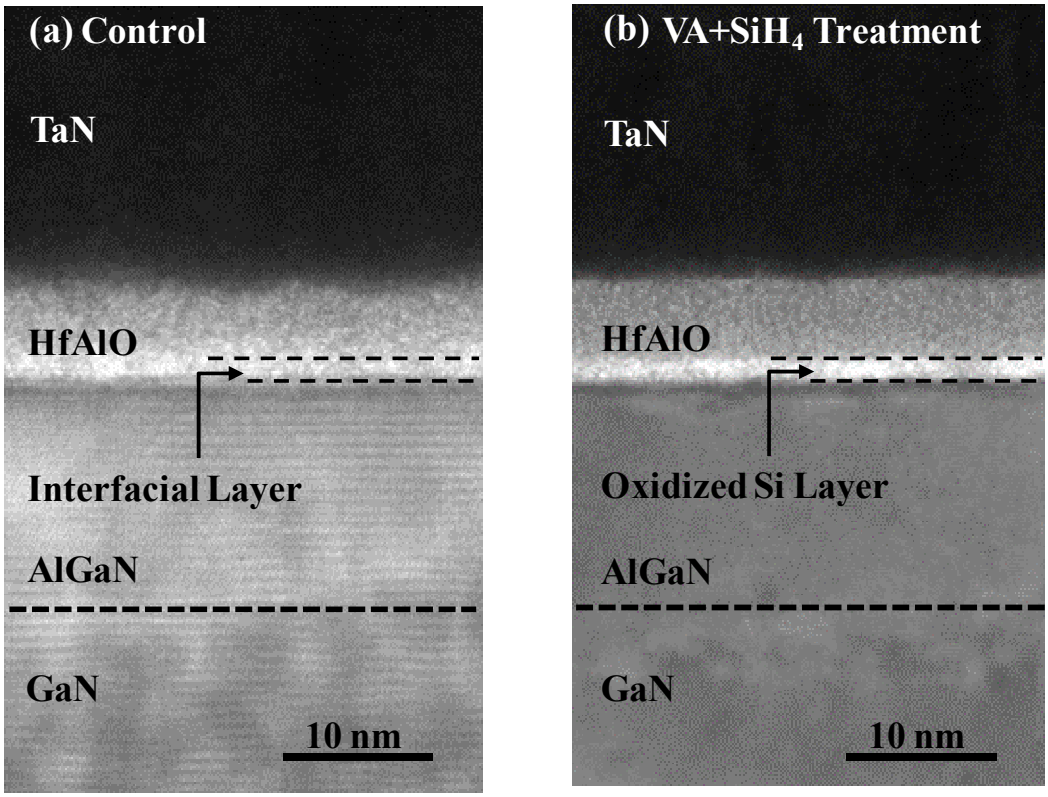


Fig. 3.6. (a) Cross-sectional TEM image of a TaN/HfAlO/AlGaN/GaN stack without *in situ* VA and SiH_4 treatment, showing that a native oxide interfacial layer is formed on the AlGaN surface. (d) Cross-sectional TEM image of a TaN/HfAlO/AlGaN/GaN stack with *in situ* VA and SiH_4 treatment, showing that an oxidized Si layer (1 ~ 2 nm) is formed on the AlGaN surface.

Fig. 3.6 (a) shows a high resolution TEM image of a TaN/HfAlO/AlGaN/GaN stack without *in situ* VA and SiH_4 treatment. An interfacial layer, which could be the native gallium oxide as detected by XPS, is observed between the gate dielectric and AlGaN barrier layer. Fig. 3.6 (b) shows a high resolution TEM image of a TaN/HfAlO/AlGaN/GaN stack with *in situ* VA and SiH_4 treatment. Vacuum anneal was performed for desorption of contaminants on the AlGaN surface. SiH_4 treatment formed a layer of Si, which was subsequently oxidized to form the oxidized Si layer (Si-O) during HfAlO deposition. The presence of the oxidized Si layer was confirmed by XPS, which was discussed in Fig. 3.5. This oxidized Si layer (1 ~ 2 nm)

served as a protective layer to prevent the AlGaN surface from oxidation during the HfAlO deposition.

3.3.2 Electrical Characterization of the AlGaN/GaN MOS-HEMTs with and without *in situ* VA and SiH_4 Treatment

Fig. 3.7 shows the gate leakage current density J_G as a function of gate voltage V_G of the AlGaN/GaN MOS-HEMTs with and without *in situ* VA and SiH_4 treatment. J_G was measured with both source and drain grounded. As compared with the control device, J_G of the device with *in situ* VA and SiH_4 treatment is suppressed by around 3 orders of magnitude at V_G = 4 V, and by around 2 orders of magnitude at V_G = –9 V. The reason for J_G reduction could be the suppression of trap-assisted tunneling current in both positive and negative V_G regimes [124]. Fig. 3.8 shows the capacitance-voltage (C-V) characteristics of the AlGaN/GaN MOS-HEMTs with and without *in situ* VA and SiH_4 treatment. The accumulation capacitance at V_G = 0 V for both cases is around 0.27 μF/cm^2. The left shift of the C-V characteristic of the AlGaN/GaN MOS-HEMT with *in situ* VA and SiH_4 treatment indicates the reduction of negatively charged interface states, as compared with the control device [125], [126].

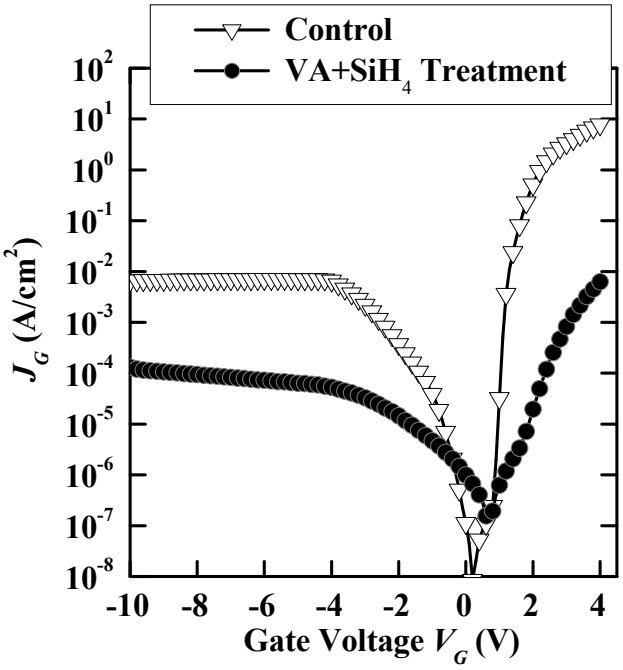


Fig. 3.7. Gate leakage current density J_G as a function of gate voltage V_G of the AlGaN/GaN MOS-HEMTs with and without *in situ* VA and SiH_4 treatment. J_G of the device with *in situ* VA and SiH_4 treatment is suppressed by ~ 3 orders of magnitude at $V_G = 4$ V.

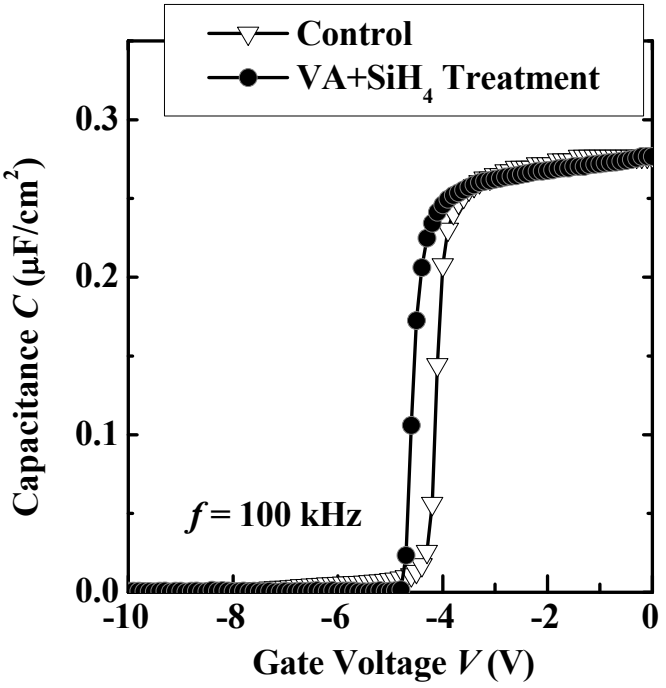


Fig. 3.8. Measured capacitance-voltage (*C-V*) characteristics of the AlGaN/GaN MOS-HEMTs with and without *in situ* VA and SiH_4 treatment.

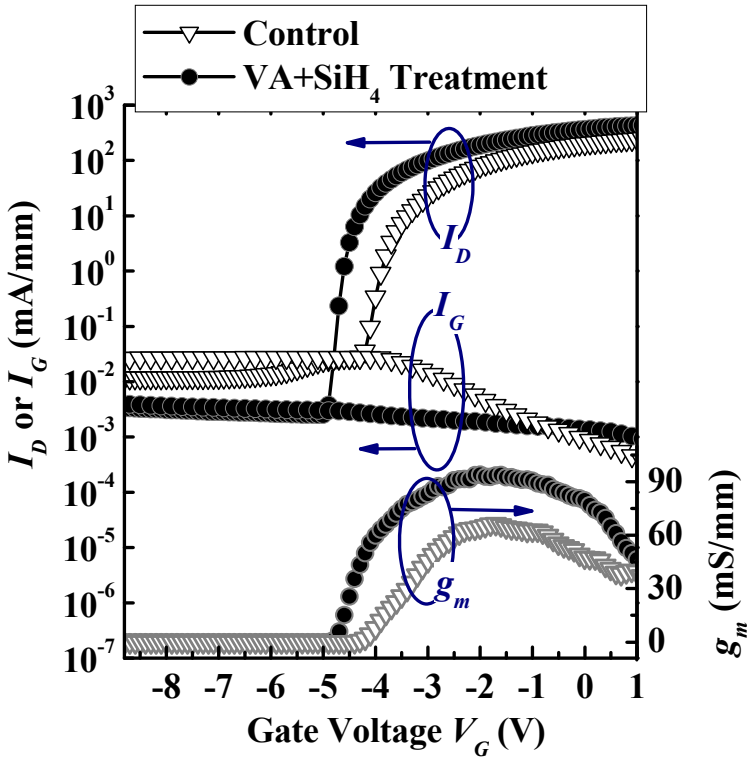


Fig. 3.9. Drain current (I_D-V_G), gate leakage current (I_G-V_G), and extrinsic transconductance (g_m-V_G) as a function of gate voltage V_G of the AlGaN/GaN MOS-HEMTs with and without *in situ* VA and SiH_4 treatment at V_D = 5 V.

Fig. 3.9 shows the drain current versus gate voltage (I_D-V_G) characteristics (at V_D = 5 V) of the AlGaN/GaN MOS-HEMTs with and without *in situ* VA and SiH_4 treatment. The gate leakage current I_G is also plotted as a function of V_G for these two samples. In the off-state, I_D is dominated by the gate leakage current I_G. As compared with the control, off-state I_D is decreased by around one order of magnitude for the device with *in situ* VA and SiH_4 treatment. The reduction of I_G in the off-state for the device with *in situ* VA and SiH_4 treatment is attributed to the suppression of trap-assisted tunneling current from the TaN gate to the channel through the HfAlO/AlGaN stack [124]. As shown in Fig. 3.9, the values of the threshold voltage for the devices with and without *in situ* VA and SiH_4 treatment are

–4.0 and –3.3 V, respectively. As compared with the control device, there is –0.7 V of the threshold voltage shift for the device with *in situ* VA and SiH_4 treatment. Negative threshold voltage shift could be due to the reduction of the negatively charged interface states at the HfAlO/AlGaN interface, and the amount of reduced interface states due to this passivation technique will be discussed later. 2-DEG density could be increased with the reduction of negatively charged interface states, since the negatively charged interface states could partially deplete the electrons in the AlGaN/GaN heterostructure [125]. In the literature, a positive threshold voltage shift was also reported, and was due to the reduction of the positively charged interface states at the dielectric/AlGaN interface [126].

With the aid of Silvaco TCAD, device simulation was carried out to analyze the effect *in situ* VA and SiH_4 passivation on the device characteristics. The AlGaN/GaN heterostructure used in the Silvaco TCAD is same as the one used in the experimental work: $Al_{0.25}Ga_{0.75}N$ (20 nm) / GaN (3 μm) / Sapphire. As for the 3 μm GaN buffer layer, 1 μm GaN layer on the top has donor-like background doping concentration of 1.0×10^{15} cm^{-3} and the 2 μm GaN layer at the bottom has acceptor-like background doping concentration of 3.0×10^{17} cm^{-3}. As shown in Fig. 3.10, the polarization charge used in the simulation at HfAlO/AlGaN, AlGaN/GaN, and GaN/Sapphire interfaces are -2.58×10^{13}, 1.04×10^{13}, and 1.54×10^{13} cm^{-2}, respectively. The polarization charge density was calculated based on the paper by O. Ambacher *et al*. [10], which has been discussed in the Section 1.1.2 of Chapter 1. Device in the simulation has the gate length of 2 μm, gate-to-drain spacing of 5 μm, and gate-to-source spacing

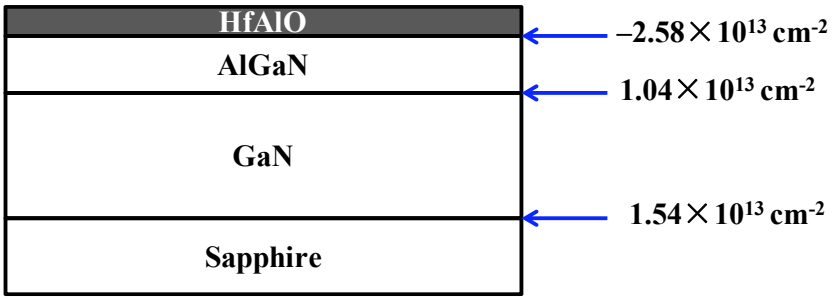


Fig. 3.10: Polarization charge used in the simulation at HfAlO/AlGaN, AlGaN/GaN, and GaN/Sapphire interfaces are -2.58×10^{13}, 1.04×10^{13}, and 1.54×10^{13} cm^{-2}, respectively.

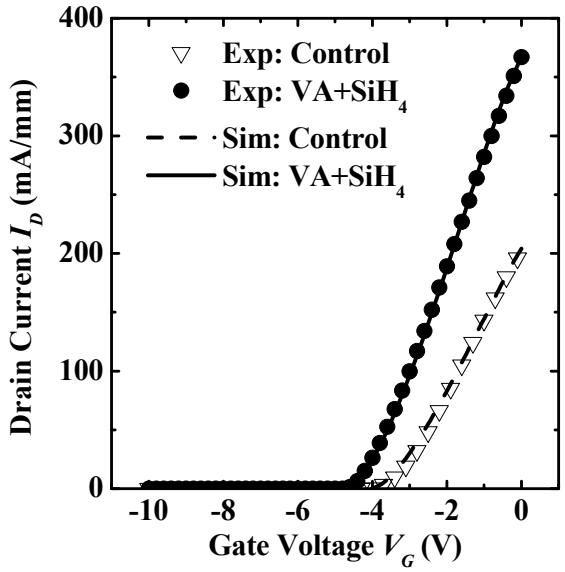


Fig. 3.11: Linear I_D-V_G characteristics (V_D = 5 V) of AlGaN/GaN MOS-HEMTs with and without *in situ* VA and SiH4 treatment were fitted using Silvaco TCAD. (Exp: experimental result; Sim: simulation result)

of 5 μm, which are same as the ones of the fabricated devices. At the HfAlO/AlGaN interface, two types of interface traps are introduced: donor-like traps located at 0.37 eV below the conduction band of AlGaN (E_c–0.37 eV) and acceptor-like traps located at 1 eV above the valence band of AlGaN (E_v+1.0 eV) [127]. Donor-like and acceptor-like traps could be formed by the point defects of nitrogen-vacancies and gallium-vacancies, respectively. In the control device, the density of donor-like and acceptor-like traps are 2.96×10^{13} and 1.2×10^{13} cm^{-2}, respectively. As shown in Fig. 3.11, the linear

I_D-V_G plots shown in Fig. 3.9 were well fitted using Silvaco TCAD. In order to match the experimental data for the device with *in situ* VA and SiH_4 passivation, the acceptor-like traps at the HfAlO/AlGaN interface was reduced by the amount of 6.0×10^{12} cm^{-2}. Through this simulation, it is found that this passivation technique helps to reduce the acceptor-like traps located at 1 eV above the valence band of AlGaN [128]. In addition, the simulation code used in Fig. 3.11 was added as Appendix B.

The extrinsic peak transconductance (V_D = 5 V) for the devices with and without *in situ* VA and SiH_4 treatment are defined to be $g^1_{m,max}$ and $g^0_{m,max}$, respectively. As shown in Fig. 3.9, the values of $g^1_{m,max}$ and $g^0_{m,max}$ are 93 and 66 mS/mm, respectively. The extrinsic transconductance g_m is affected by both carrier mobility μ and parasitic S/D series resistance. Due to the parasitic S/D series resistance, the value of the extrinsic transconductance g_m is smaller than that of the intrinsic transconductance $g_{m,i}$, which is independent of the parasitic S/D series resistance. $g_{m,i}$ of the long channel device can be extracted using [129]

$$g_{m,i} = g_m/(1 - R_S g_m), \tag{3.1}$$

where R_S is the parasitic source resistance. The value of R_S can be estimated as half of the value of the parasitic S/D series resistance $R_{S/D}$, and $R_{S/D}$ is defined as $R_{S/D} = R_{Total} - R_{Channel}$. R_{Total} is the total resistance measured between the source and drain of the device and $R_{Channel}$ is the channel resistance. For a very large gate-overdrive $V_G - V_{\text{th}}$ ($V_G - V_{th} >> V_D$) and a fixed small V_D (1 V), $R_{Channel}$ becomes very small compared to $R_{S/D}$, and then

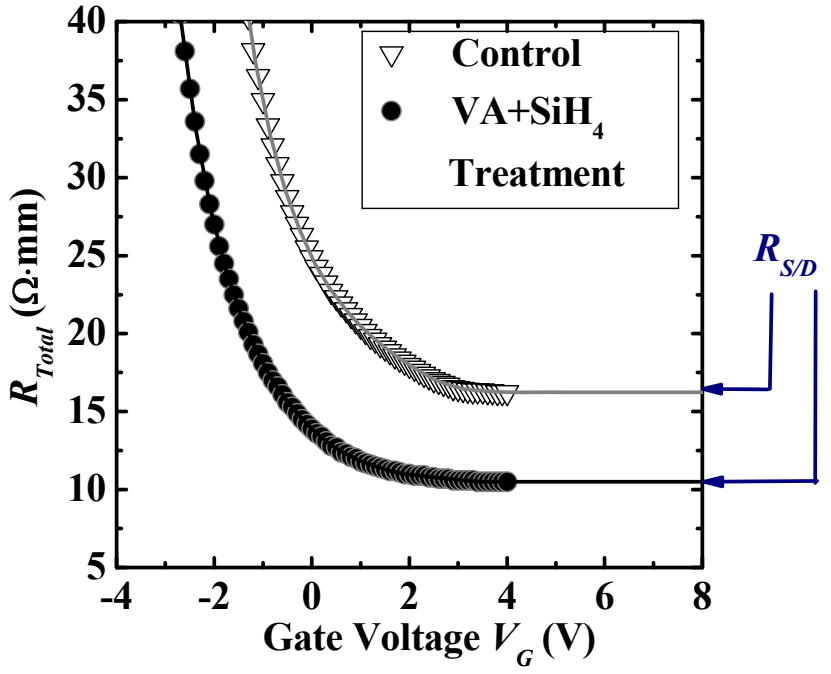


Fig. 3.12. Total resistance R_{Total} as a function of gate voltage V_G when the drain voltage was fixed at 1 V. Parasitic S/D series resistance $R_{S/D}$ for the devices with and without *in situ* VA and SiH_4 treatment shown in Fig. 3.9 is 10.4 and 16.2 Ω·mm, respectively.

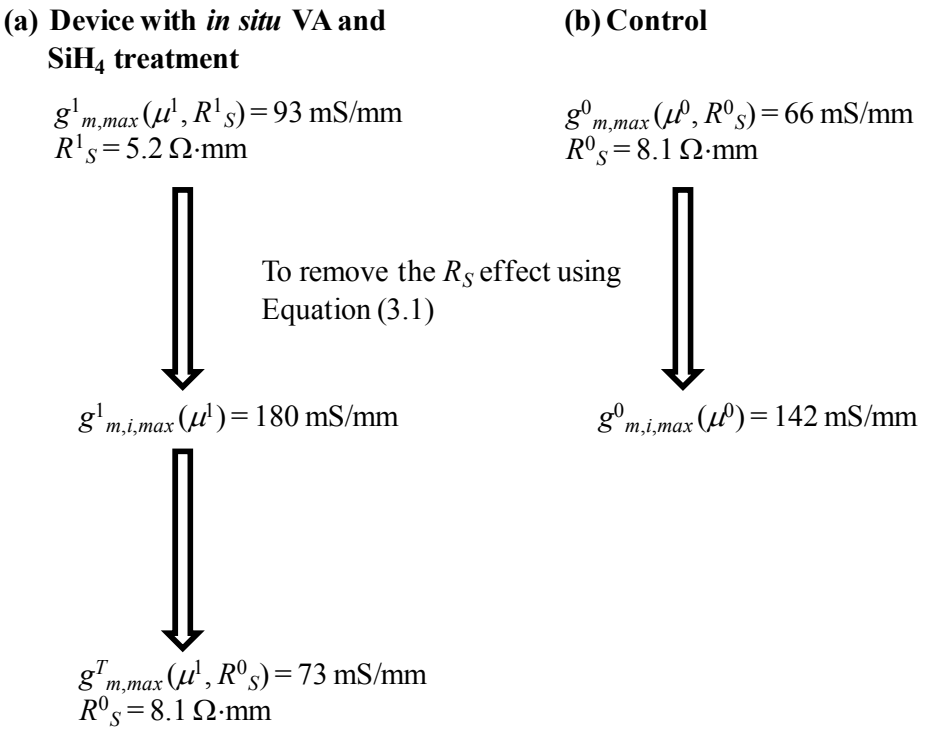
$R_{S/D}$ can be estimated from the R_{Total} versus V_G plot. As shown in Fig. 3.12, the extracted $R_{S/D}$ for the devices with and without *in situ* VA and SiH_4 treatment are 10.4 and 16.2 Ω·mm, respectively. For the device with *in situ* VA and SiH_4 passivation, the acceptor like-traps located in the access regions between gate and source/drain was reduced, thus leading to an increase of 2-DEG density and a reduction of access resistance.

The parasitic source resistance for the devices with and without *in situ* VA and SiH_4 treatment are defined to be R^1_S and R^0_S, respectively. Therefore, the values of R^1_S and R^0_S are extracted to be 5.2 and 8.1 Ω·mm, respectively. The intrinsic peak transconductance for the devices with and without *in situ* VA and SiH_4 treatment are defined to be $g^1_{m,i,max}$ and $g^0_{m,i,max}$, respectively. Using the Equation (3.1), the values of $g^1_{m,i,max}$ and $g^0_{m,i,max}$ are extracted to be

180 and 142 mS/mm, respectively. As compared with the control device, the device with *in situ* VA and SiH_4 treatment shows 27% enhancement of the intrinsic peak transconductance, indicating the carrier mobility μ enhancement for the device with *in situ* VA and SiH_4 treatment. The carrier mobility enhancement for the device with *in situ* VA and SiH_4 treatment could be due to the reduced carrier scattering, such as remote charge scattering [115], [116]. The thicknesses for AlGaN barrier layer in Reference [115] and [116] are 20 and 30 nm, respectively. As compared to that of the control device, the extrinsic peak transconductance for the device with *in situ* VA and SiH_4 treatment is increased from 66 to 93 mS/mm, giving a change in $g_{m,max}$ of 27 mS/mm or 41 % enhancement.

Fig. 3.13 (a) shows the procedure to analyze the contribution from carrier mobility μ enhancement and R_S reduction to the enhancement of the extrinsic peak transconductance for the device with *in situ* VA and SiH_4 treatment. In order to separate carrier mobility μ enhancement and R_S reduction for the enhancement of the extrinsic peak transconductance, an intermediate variable of extrinsic peak transconductance is introduced here. This intermediate extrinsic peak transconductance is defined to $g^T_{m,max}$, which have an intrinsic peak transconductance (180 mS/mm) and a source resistance (8.1 Ω·mm). Using Equation (3.1), $g^T_{m,max}$ is calculated to be 73 mS/mm. As illustrated by Fig. 3.13 (b), the enhancement of the extrinsic peak transconductance due to the carrier mobility μ enhancement can be estimated based on the difference between $g^T_{m,max}$ and $g^0_{m,max}$, as source resistance for $g^T_{m,max}$ and $g^0_{m,max}$ is the same. Similarly, the enhancement of the extrinsic peak transconductance due to R_S reduction can be estimated based on the

difference between $g^{T}_{m,max}$ and $g^{1}_{m,max}$, as carrier mobility for $g^{T}_{m,max}$ and $g^{1}_{m,max}$ is the same. As shown in Fig. 3.13 (b), the percentage contribution to the extrinsic peak transconductance enhancement from carrier mobility μ enhancement and R_S reduction is 26 % and 74 %, respectively.

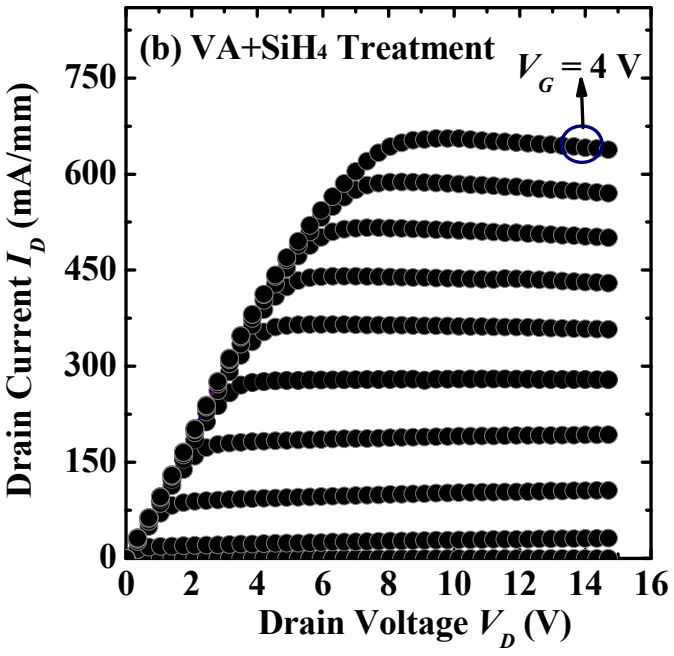


(b)

Difference between		Due to the difference in
$g^{1}_{m,max}(\mu^{1}, R^{1}_{S})$ and $g^{0}_{m,max}(\mu^{0}, R^{0}_{S})$	27 mS/mm	μ and R_S
$g^{T}_{m,max}(\mu^{1}, R^{0}_{S})$ and $g^{0}_{m,max}(\mu^{0}, R^{0}_{S})$	7 mS/mm or 26 % of 27 mS/mm	μ
$g^{T}_{m,max}(\mu^{1}, R^{0}_{S})$ and $g^{1}_{m,max}(\mu^{1}, R^{1}_{S})$	20 mS/mm or 74 % of 27 mS/mm	R_S

Fig. 3.13. (a) Schematic illustrating the extraction of $g^{1}_{m,i,max}$, $g^{0}_{m,i,max}$, and $g^{T}_{m,max}$, to analyze the contribution from carrier mobility and R_S to the total extrinsic peak transconductance enhancement using Equation (3.1). Here, the carrier mobility for devices with and without *in situ* VA and SiH_4 treatment is μ^1 and μ^0, respectively. (b) By comparing among $g^{1}_{m,max}$, $g^{0}_{m,max}$, and $g^{T}_{m,max}$, the percentage contribution to the extrinsic peak transconductance enhancement from carrier mobility enhancement and R_S reduction can be separated.

Fig. 3.14 (a) and (b) show the drain current versus drain voltage (I_D-V_D) characteristics of the AlGaN/GaN MOS-HEMTs with and without *in situ* VA and SiH_4 treatment (Note: Devices shown here are the same pair whose I_D-V_G characteristics are shown in Fig. 3.9). As shown in Fig. 3.9, the values of the threshold voltage for the devices with and without *in situ* VA and SiH_4 treatment are –4.0 and –3.3 V, respectively. At a gate overdrive ($V_G - V_{th}$) of 7 V and a drain voltage V_D of 10 V, the drain current for the device with *in situ* VA and SiH_4 treatment is ~ 575 mA/mm, which is ~ 53 % higher than ~ 375 mA/mm of the control device. The enhancement of saturation drain current is due to both carrier mobility μ enhancement and parasitic S/D series resistance reduction.



(a)

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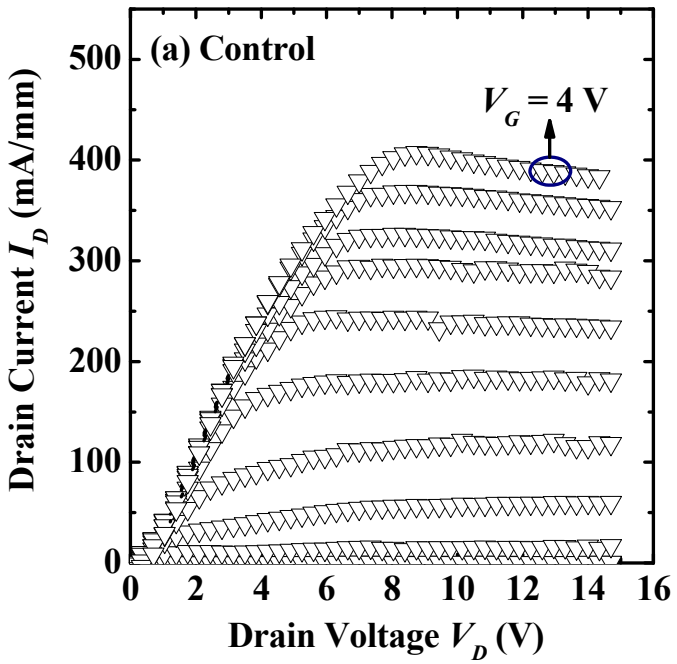


(b)

Fig. 3.14. Output (I_D-V_D) characteristics of the AlGaN/GaN MOS-HEMTs (a) with and (b) without *in situ* VA and SiH_4 treatment, where V_G is varied in steps of 1 V from −5 to 4 V.

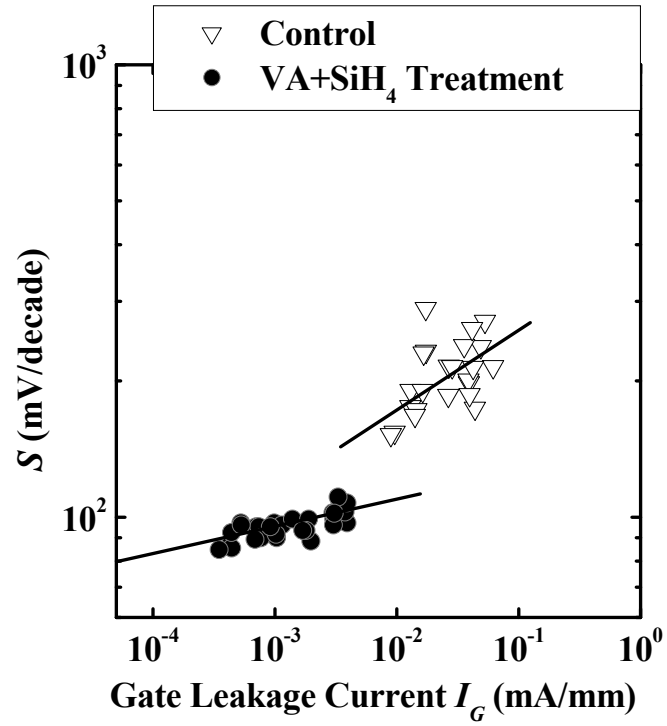


Fig. 3.15. Plot of sub-threshold swing S as a function gate leakage current I_G for the AlGaN/GaN MOS-HEMTs with and without *in situ* VA and SiH_4 treatment. The number of the measured devices with and without *in situ* VA and SiH_4 treatment are 29 and 23, respectively.

Fig. 3.15 shows a plot of sub-threshold swing S as a function of the gate leakage current I_G for the AlGaN/GaN MOS-HEMTs with and without *in situ* VA and SiH_4 treatment. I_G shown in Fig. 3.15 was measured at $V_G = V_{th} - 5$ V and $V_D = 5$ V. For the devices with *in situ* VA and SiH_4 treatment, the median S is well below 100 mV/decade, which is much lower than that of over 150 mV/decade for the control devices. The devices with *in situ* VA and SiH_4 treatment have a lower S and I_G, which is attributed to a lower interface state density at HfAlO/AlGaN interface. Within each set of data, the device-to-device variation in the I_G and S is possibly due to the variation of the interface state density at the HfAlO/AlGaN interface [48].

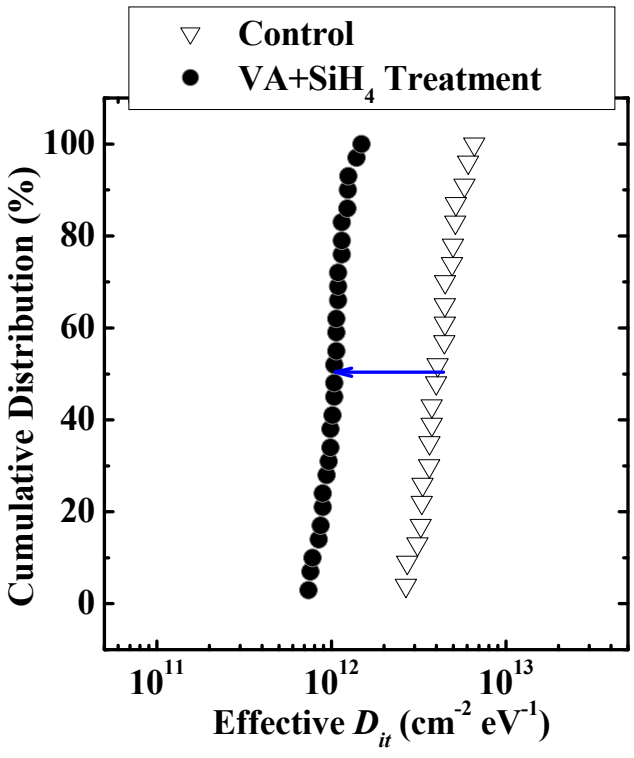


Fig. 3.16. Cumulative distribution plot of effective D_{it} for the AlGaN/GaN MOS-HEMTs with and without *in situ* VA and SiH_4 treatment. The number of the measured devices with and without *in situ* VA and SiH_4 treatment are 29 and 23, respectively. With *in situ* VA and SiH_4 treatment, the median value of effective D_{it} was reduced from 4.2×10^{12} to 1.1×10^{12} cm^{-2} eV^{-1}.

The effective interface state density can be estimated by the equation of sub-threshold *S* swing:

$$S = \frac{kT}{q}\ln(10)\times(1+\frac{C_S + C_{it}}{C_{OX}}), \qquad (3.2)$$

where k is the Boltzmann constant, T is the characterization temperature, q is the electronic charge, C_S is the depletion capacitance of GaN, C_{it} is the HfAlO/AlGaN interface state capacitance, and C_{OX} is the gate capacitance of 0.27 μF/cm^2 (shown in Fig. 3.8). When V_G is near to the threshold voltage, C_{it} is the negligible compared to C_{it}, and the effective interface state density D_{it} at HfAlO/AlGaN interface can be estimated using the following equation [130]:

$$D_{it} = \frac{C_{it}}{q} \approx (\frac{qS}{kT\ln(10)} - 1)\times\frac{C_{OX}}{q}. \qquad (3.3)$$

Effective D_{it} was calculated using Equation (3.3) and shown in Fig. 3.16 for the devices with and without *in situ* VA and SiH_4 treatment. For the control devices, the effective D_{it} is estimated to be ~ 4.2 × 10^{12} cm^{-2} eV^{-1} for a median *S* value of 200 mV/decade. As for the devices with *in situ* VA and SiH_4 treatment, the effective D_{it} is estimated to be ~ 1.1 × 10^{12} cm^{-2} eV^{-1} for a median *S* value of 95 mV/decade. The amount of reduced interface state density, ΔD_{it}, is calculated to be ~ 3.1 × 10^{12} cm^{-2} eV^{-1}, based on the change of the median sub-threshold swing alone. As discussed in Chapter 2, the interface state density at HfAlO/GaN interface of TaN/HfAlO/GaN capacitors with *in situ* VA and SiH_4 treatment was extracted to be ~ 10^{11} cm^{-2} eV^{-1} by using a conductance method. As compared to that at HfAlO/GaN interface of TaN/HfAlO/GaN capacitors with *in situ* VA and SiH_4 treatment, the interface

state density at HfAlO/AlGaN interface of the AlGaN/GaN MOS-HEMTs with *in situ* VA and SiH_4 treatment is about 1 order of magnitude higher. The higher interface state density for the HfAlO/AlGaN interface could be due to more point defects on AlGaN surface, such as cation vacancies, when Al is incorporated in AlGaN [131].

Fig. 3.17 shows the effect of *in situ* VA and SiH_4 treatment on the current on/off, I_{on}/I_{off}, ratio as a function of gate leakage current I_G of the AlGaN/GaN MOS-HEMTs with and without *in situ* VA and SiH_4 treatment. I_{off} and I_{on} are defined to be the values of I_D measured at $V_G = V_{th} - 5$ V and V_{th} + 6 V, respectively, at V_D = 5 V. Here, the gate leakage current I_G was measured at $V_G = V_{th} - 5$ V and $V_D = 5$ V. The I_{on}/I_{off} ratio for the devices with

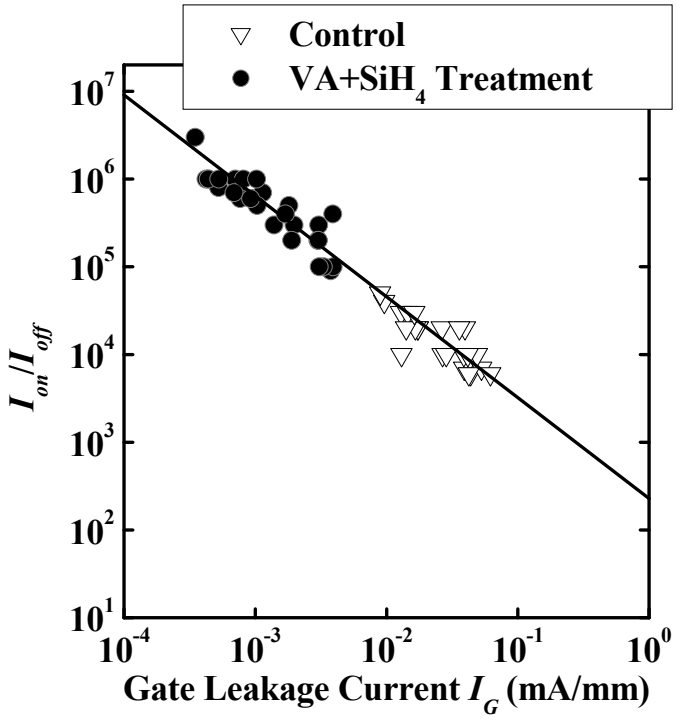


Fig. 3.17. Plot of I_{on}/I_{off} ratio as a function of gate leakage current I_G for the AlGaN/GaN MOS-HEMTs with and without *in situ* VA and SiH_4 treatment. The number of the measured devices with and without *in situ* VA and SiH_4 treatment are 29 and 23, respectively.

in situ VA and SiH_4 treatment is increased up to ~ 10^6. Also, the gate leakage current I_G for the devices with *in situ* VA and SiH_4 treatment is reduced to ~ 10^{-3} mA/mm.

3.4 Summary

The effect of *in situ* VA and SiH_4 treatment on the electrical characteristics of AlGaN/GaN MOS-HEMTs was investigated. The devices with *in situ* VA and SiH_4 treatment showed reduced gate leakage current due to the suppression of trap-assisted tunneling current and improved saturation drain current attributed to both carrier mobility enhancement and parasitic source/drain series resistance reduction. *In situ* VA and SiH_4 treatment of the AlGaN surface prior to HfAlO deposition enables the realization of AlGaN/GaN MOS-HEMTs with sub-threshold swing of less 100 mV/decade, reduced gate leakage down to ~ 10^{-3} mA/mm, and high I_{on}/I_{off} ratio of ~ 10^6.

Chapter 4

Diamond-Like Carbon Liner with Highly Compressive Stress for Performance Enhancement of AlGaN/GaN MOS-HEMTs

4.1 Introduction

Wide bandgap GaN-based heterostructure devices, such as high electron mobility transistors (HEMTs), are promising for application in high power and high frequency electronics [112], [117], [118], [120]. The large polarization charge in AlGaN/GaN heterostructure causes a high 2-dimensional electron gas (2-DEG) density, which inevitably results in normally-on operation featuring a negative threshold voltage V_{th}. However, normally-off, i.e., enhancement mode AlGaN/GaN HEMTs with a positive threshold voltage V_{th}, are desirable for microwave and digital circuits [132].

In the literature, various techniques have been explored to realize enhancement-mode AlGaN/GaN HEMTs, such as the use of a thin AlGaN barrier layer with a low Al mole fraction [133], treatment of the channel region using fluorine-based plasma [134], use of a recessed gate structure [135], use of a metal gate with a high work function [136], use of a gate with selectively grown p-n junction (p-GaN/n-AlGaN/GaN) [137], and use of a gate with p-AlGaN/AlGaN/GaN layer [138]. In addition, a compressively strained InAlN [139] or an InGaN [140] cap layer can be grown on AlGaN/GaN heterostructure for the threshold voltage adjustment. A numerical study of the effect of deivce passivation film induced stress on the

electrical properties of AlGaN/GaN HEMTs was carried out using an edge force model [141]. This study shows that the compressive stress in the AlGaN barrier layer under the gate could result in positive threshold voltage shift for AlGaN/GaN HEMTs. This is due to the raised conduction band minimum in the 2-DEG channel at the AlGaN/GaN interface after applying a compressive passivation film [141]. On the other hand, experiment work has shown that the AlGaN/GaN HEMTs with a tensile silicon nitride encapsulating layer could cause a negative threshold voltage shift [142]. The threshold voltage shift under a compressive or tensile stress is due to the local modulation of the polarization charge of the AlGaN/GaN heterostructure with the Ga-polarity face: tensile stress increases the density of polarization charge and compressive stress decreases the density of polarization charge [9]-[10], [143].

In this Chapter, the effect of a diamond-like carbon (DLC) liner with highly compressive stress (~ 6 GPa) on the electrical characteristics of AlGaN/GaN metal-oxide-semiconductor HEMTs (MOS-HEMTs) was studied. The compressive stress induced by the DLC liner in the channel region under the gate can reduce the tensile stress in the AlGaN barrier layer, thus reducing the polarization charge density through the piezoelectric polarization effect. In the access regions between the gate and the source/drain (S/D) contacts, the polarization charge density is increased by the additional tensile stress induced by the DLC liner, thereby reducing the paracitic S/D series resistance $R_{S/D}$. The overall result is a positive shift of the threshold voltage and an enhancement of the saturation drain current for the devices with the DLC liner, as compared with the control devices. In addition, *in situ* vacuum anneal and

SiH_4 treatment technique, which was discussed in Chapter 3, was also incorporated into the process flow to enhance the device performance.

4.2 Device Concept and Stress Simulation

Fig. 4.1 shows a schematic diagram of the AlGaN/GaN MOS-HEMT encapsulated by a DLC liner. Two-dimensional distribution of the lateral stress σ_{xx} induced by the DLC liner was simulated for an AlGaN/GaN MOS-HEMT with a gate length L_G of 400 nm [Fig. 4.2 (a)]. Horizontal profiles of the simulated lateral stress σ_{xx} at the AlGaN/GaN interface (y = –27 nm,

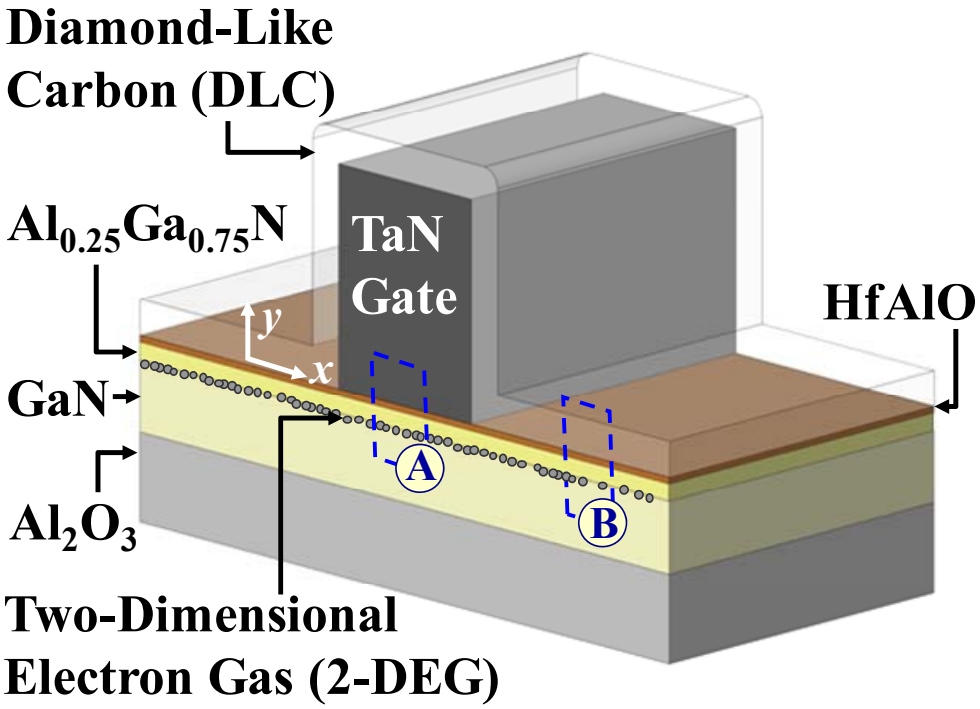


Fig. 4.1. Schematic diagram of the AlGaN/GaN MOS-HEMT encapsulated by a diamond-like carbon (DLC) liner with highly compressive stress. The thicknesses of the DLC Layer, HfAlO layer, and AlGaN barrier layer are 40 nm, 7 nm, and 20 nm, respectively. TEM image were taken in regions of A and B, and shown in Fig. 4.7.

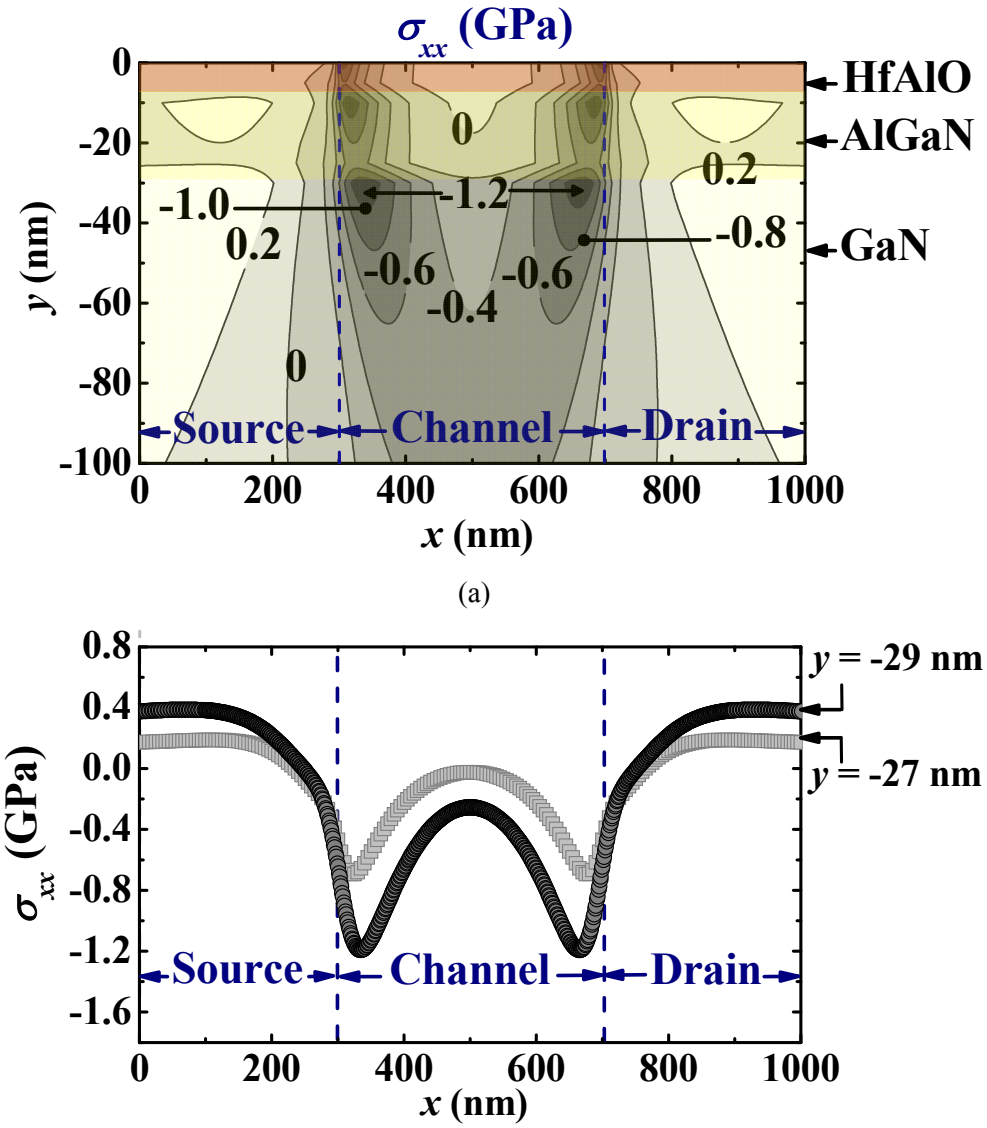


Fig. 4.2. (a) Simulated lateral stress σ_{xx} (in units of GPa) contributed by a 40 nm thick DLC liner with an intrinsic compressive stress of ~ 6 GPa in an AlGaN/GaN MOS-HEMT with a gate length L_G of 400 nm. The stress contours are labeled. The contour interval is 200 MPa. (b) Stress σ_{xx} along horizontal lines at the AlGaN/GaN interface (y = –27 nm, denoted by light gray squares) and 2 nm below AlGaN/GaN interface (y = –29 nm, denoted by dark gray circles). A peak compressive stress of –1.2 GPa is observed near the edges of the gate. The tensile stress contributed by the DLC liner in the access regions between the gate and S/D contacts is ~ 0.3 to 0.4 GPa.

denoted by light gray squares) and 2 nm below AlGaN/GaN interface (y = –29 nm, denoted by dark gray circles) are shown in Fig. 4.2 (b). To simulate the stress in the device, the Taurus Abaqus simulation suite was used. The Abaqus simulation suite is able to simulate the mechanical stress that is experienced in the entire device due to a stress liner being deposited. As the DCL liner was only deposited over the gate region and the access regions between the gate and source/drain, only data from those regions were extracted after the simulation. Lateral stress along the source-to-drain, σ_{xx}, is shown in Fig. 4.2 (a), and is the dominant stress that affects the in-plane piezoelectric polarization in the AlGaN/GaN heterosturcture. In addition, code used for stress simulation was added as Appendix C. The stress near the top of the GaN region under the gate is generally compressive, and a peak compressive stress of –1.2 GPa is located near the edges of the gate. The compressive stress induced by the DLC liner in the region under the gate effectively reduces the tensile stress in the AlGaN barrier layer. This reduces the polarization charge density through the piezoelectric polarization effect, which could in turn lead to a positive V_{th} shift. On the other hand, the tensile stress (~ 0.3 to 0.4 GPa) induced by the DLC liner in the access regions between the gate and the S/D contacts can increase the polarization charge density through the piezoelectric polarization effect, thus reduces the $R_{S/D}$.

The polarization charge density σ at the AlGaN/GaN interface with and without the DLC liner was calculated using Equations (1.1)-(1.9) of Chapter 1 and is shown in Fig. 4.3. Without the DLC liner, the polarization charge density is 1.38×10^{13} cm^{-2}, which is represented by the square symbols in Fig. 4.3. As shown in Fig. 4.3, the non-uniform stress induced by the DLC

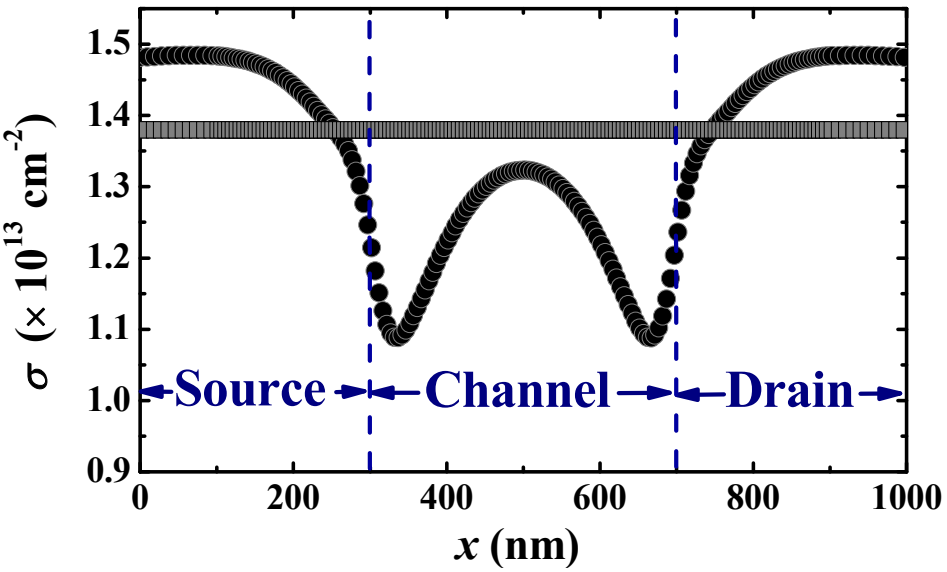


Fig. 4.3. Calculated polarization charge density σ at the AlGaN/GaN interface (at the depths of –27 nm) for an AlGaN/GaN MOS-HEMT (L_G = 400 nm) with and without the DLC liner. It was assumed that there was no strain relaxation due to the external stress. The square symbols represent the polarization charge for the control device, and the circle symbols represent the polarization charge for the device with the DLC liner.

liner leads to a non-uniform polarization charge profile at the AlGaN/GaN interface, which is represented by the circle symbols. The polarization charge density in the access regions between gate and S/D contacts for the DLC-stained device is 1.48 × 10^{13} cm^{-2}, which is ~ 7.2 % higher than 1.38 × 10^{13} cm^{-2} of the control device, leading to a $R_{S/D}$ reduction. The effective polarization charge density σ^{eff} under the gate for the DLC-strained device in Fig. 4.3 is calculated to be 1.22 × 10^{13} cm^{-2} using the equation below:

$$\sigma^{eff} = \frac{\int_{x_1}^{x_2} \sigma \, dx}{L_G}, \; x_1 = 300 \text{ nm and } x_2 = 700 \text{ nm}. \qquad (4.1)$$

As compared with the control device, the DLC-strained device has a lower effective polarization charge density under the gate. The reduction of

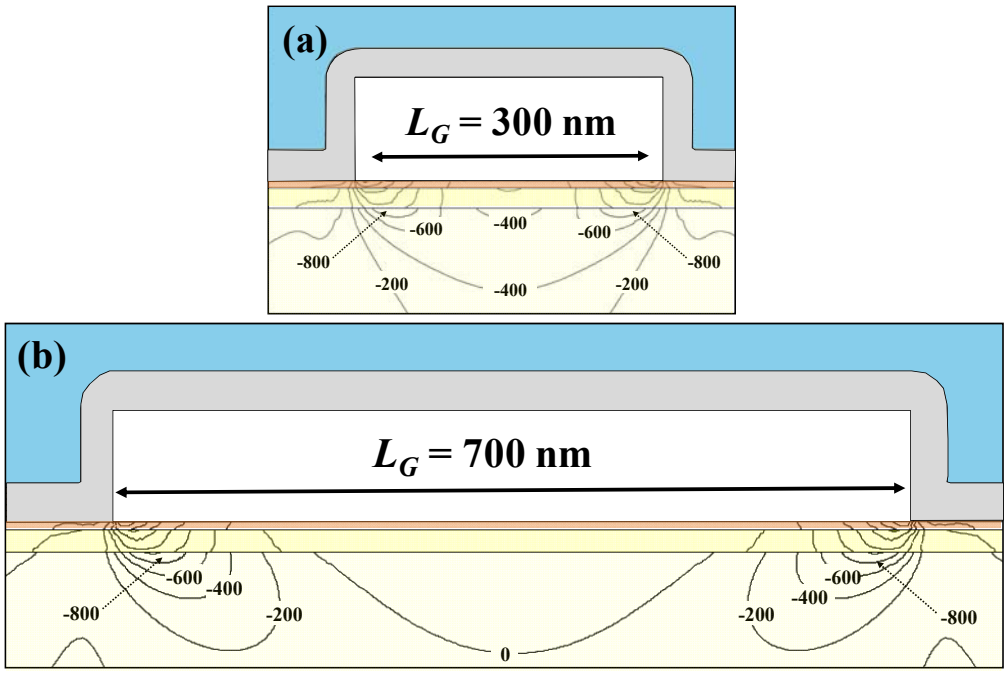


Fig. 4.4. Simulated stress contour (in units of MPa) for the DLC-strained AlGaN/GaN MOS-HEMTs with gate length L_G of (a) 300 nm and (b) 700 nm. The magnitude of stress is higher near the gate edges than that at the center of channel.

polarization charge under the gate could result in a positive threshold voltage shift, which will be discussed in Section 4.4.

The stress induced by the DLC liner in AlGaN/GaN MOS-HEMTs with gate lengths of 300 and 700 nm, was also simulated and shown in Fig. 4.4 (a) and (b), respectively. As shown in Fig. 4.4 (a) and (b), the compressive stress under the gate is non-uniform. The term "average channel stress" is defined as the average value of the stress at the AlGaN/GaN interface, or at depths of –27 nm. The average channel stress in the 2-DEG channel under the gate was calculated for AlGaN/GaN MOS-HEMTs with various gate lengths (300, 400, and 700 nm) and shown in Fig. 4.5. The average channel stress in the 2-DEG channel is higher for a device with a shorter gate length, since scaling down the gate length brings the two gate edges closer.

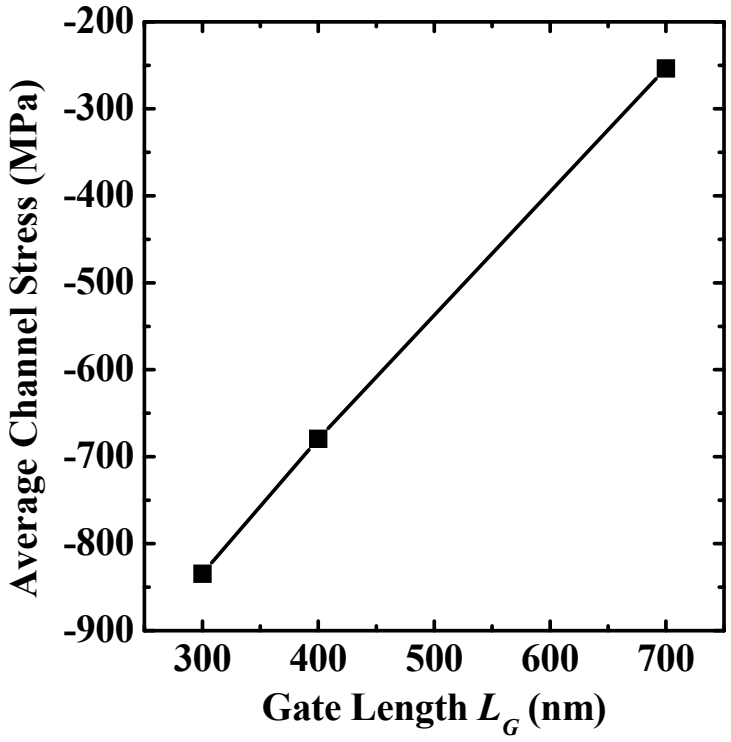


Fig. 4.5. Average channel stress in the 2-DEG due to a 40 nm thick DLC liner was simulated for various gate lengths (300, 400, and 700 nm). Stress magnitude increases with decreasing gate length.

4.3 Integration of Diamond-like Carbon Liner on AlGaN/GaN MOS-HEMTs

Fig. 4.6 shows the process flow for the fabrication of the DLC-strained AlGaN/GaN MOS-HEMTs with a HfAlO gate dielectric and a TaN gate. The epitaxial layer structure used in this study was purchased from Nippon Telegraph and Telephone Advanced Technology (NTT-AT) and grown by metal-organic chemical vapor phase deposition (MOCVD) on *c*-plane (0001) sapphire substrate. The HEMT structure, which comprises an undoped $Al_{0.25}Ga_{0.75}N$ (20 nm) barrier layer formed on an undoped GaN (3 μm)

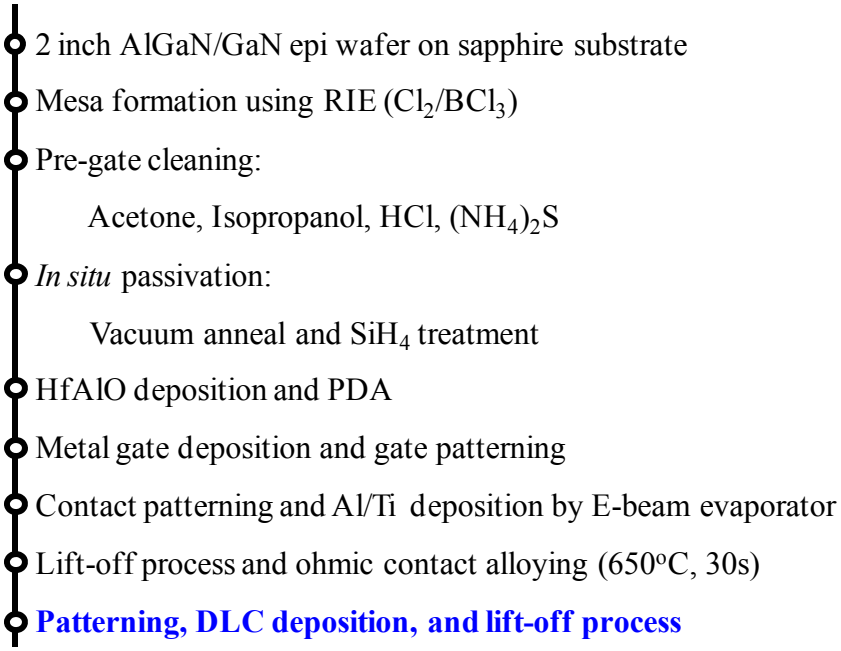


Fig. 4.6. Process flow for the fabrication of the DLC-strained AlGaN/GaN MOS-HEMTs. A novel *in situ* vacuum anneal and SiH_4 treatment technique was used prior to the gate dielectric deposition.

channel layer, has an electron Hall mobility of 1800 $cm^2/V{\cdot}s$ and a 2-DEG density of ~ 1×10^{13} cm^{-2}. Mesa isolation was first realized by Cl_2 (10 sccm) / BCl_3 (20 sccm) reactive ion etching (RIE) using an inductive-coupled plasma (ICP) system with a chamber pressure of 5mTorr and a chuck temperature of 6 ºC. Pre-gate cleaning for all samples comprised a 2-minute acetone and a 3-minute isopropanol degreasing step, followed by surface native oxide removal using dilute HCl ($HCl:H_2O$ = 1:1) for 10 minutes and *ex situ* surface passivation using an undiluted $(NH_4)_2S$ solution for 30 minutes at room temperature. The wafers were then loaded into a multi-chamber MOCVD gate cluster system for *in situ* passivation: vacuum anneal at 300 ºC for 60 s and SiH_4 treatment at 400 ºC for 60 s [75]-[76]. This was followed by HfAlO dielectric (7 nm) deposition. A post-deposition anneal (PDA) was performed

at 500 ºC for 60 s in N_2 ambient to improve the as-deposited HfAlO film quality.

Reactive sputter deposition of metal gate TaN (100 nm), photolithography, and Cl_2-based plasma etch were performed for the gate electrode definition. The gate length for this work is varied from 300 to 1000 nm. After S/D contact lithography and HfAlO removal in the contact regions using dilute HF ($HF:H_2O$ = 1:100), deposition of Ti (30 nm) followed by Al (71 nm) was performed using an electron beam (E-beam) evaporator. The Al-on-Ti stack was patterned by a lift-off process, and an alloying process was performed at 650 ºC for 30 s in N_2 ambient to form ohmic S/D contacts. Both the gate-to-source spacing and gate-to-drain spacing of the devices in this work are 5 μm. A 40 nm thick DLC film was deposited using a filtered cathodic vacuum arc (FCVA) system and patterned using a lift-off process, so that the device was encapsulated by the DLC liner except the pads for the gate and source/drain. In the FCVA system, carbon ions were generated by an arc discharge, and introduced into the process chamber through a magnetic filter duct for the deposition on the sample. The current values for the arc and filter of the FCVA system were 50 and 11 A, respectively [144]. For comparison, the control AlGaN/GaN MOS-HEMTs were also fabricated using the same process flow except that the DLC deposition was skipped.

Cross-sectional transmission electron microscopy (TEM) images of the TaN/HfAlO/AlGaN/GaN stack and the DLC/AlGaN/GaN stack are shown in Fig. 4.7 (a) and (b), respectively. The oxidized Si layer served as a protective layer to prevent the AlGaN surface from oxidation during HfAlO deposition, which has been discussed in Chapter 3. As shown in Fig. 4.7 (b), the highly

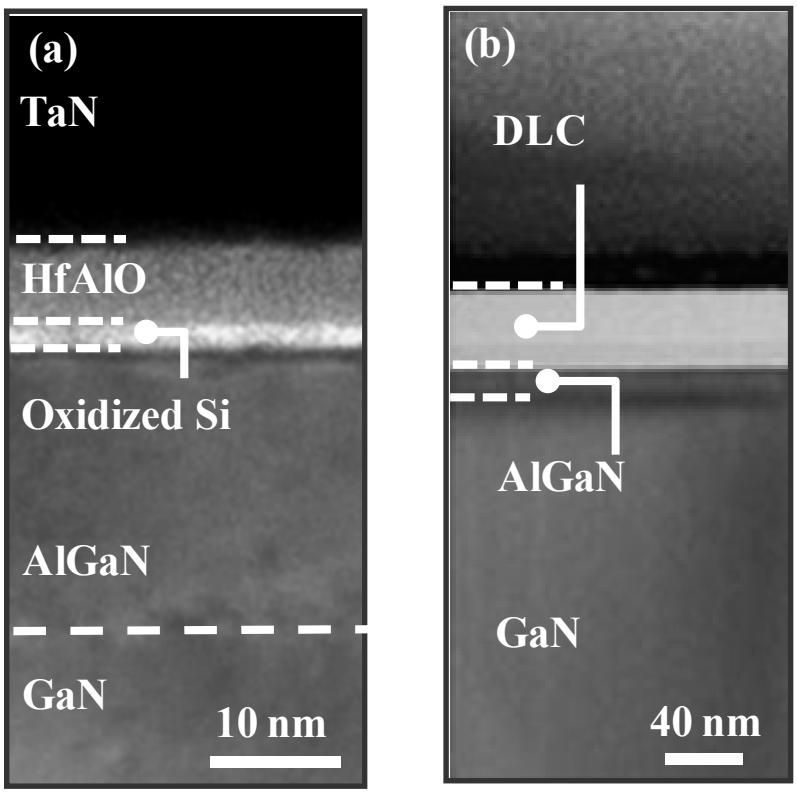


Fig. 4.7. Cross-sectional TEM images of (a) TaN/HfAlO gate stack on AlGaN/GaN (box labeled A in Fig. 4.1) and (b) 40 nm DLC liner on AlGaN/GaN (box labeled B in Fig. 4.1).

compressive stress DLC layer adheres well to the AlGaN surface. This is necessary for the coupling of mechanical stress to the channel region of the MOS-HEMTs. The vertical elemental profiles of C, Al, and Ga, obtained from secondary ion mass spectrometry (SIMS), of the DLC/AlGaN/GaN stack are shown in Fig. 4.8. The region with a high C concentration is the DLC liner.

The DLC liner is a dense film of carbon, and its material properties are strongly affected by the bonding configuration of carbon in the film. Atomic bond of carbon in the DLC liner can be sp^3 and sp^2. A DLC film with high sp^3 content will have properties close to those of diamond, such as extreme hardness and chemical inertness. Conversely, a DLC film having high sp^2 content will have properties close to those of graphite, such as high electrical

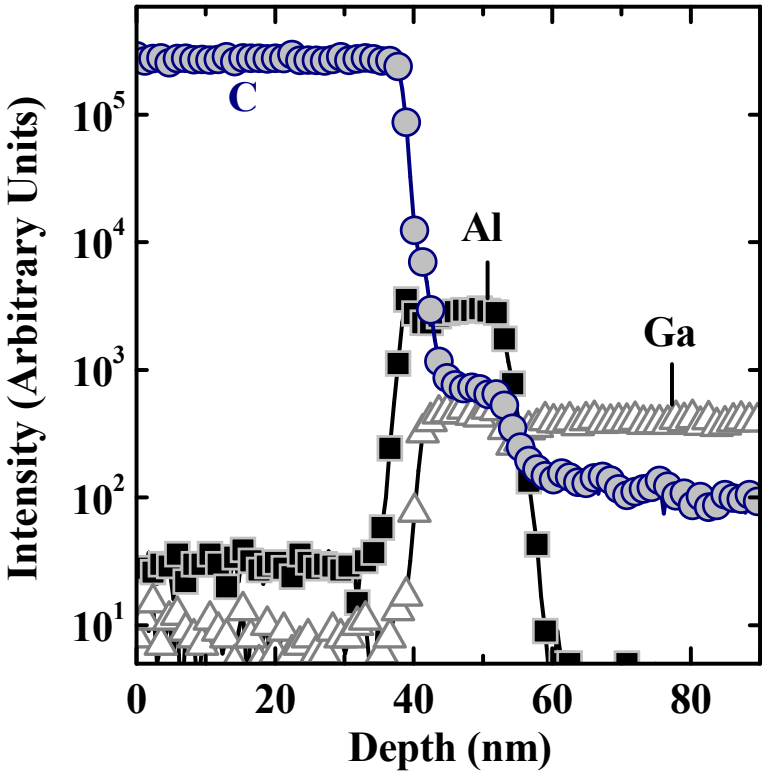


Fig. 4.8. Elemental profiles of C, Al, and Ga in the DLC/AlGaN/GaN stack was obtained using secondary ion mass spectrometry (SIMS). The region with a high C concentration is the DLC liner.

conductivity. For the application of stress liner on AlGaN/GaN MOS-HEMTs, a DLC liner with low sp^2 content is preferred, since the DLC liner with high sp^2 content could result in current leakage, e.g., device-to-device leakage [68]-[69]. On the other hand, the DLC film with high sp^3 content exhibits a large intrinsic stress, which is desirable for the stress liner integration. Fig. 4.9 shows an X-ray photoelectron spectroscopy (XPS) spectrum (C 1*s*) obtained from the DLC liner used in this work, and the spectrum is deconvoluted into three peaks: sp^3, sp^2, and C-O bonds. The DLC liner employed for the integration in AlGaN/GaN MOS-HEMTs has a sp^3 content of ~ 60 %, which was estimated by taking the ratio of the area under the curve due to sp^3 bonds

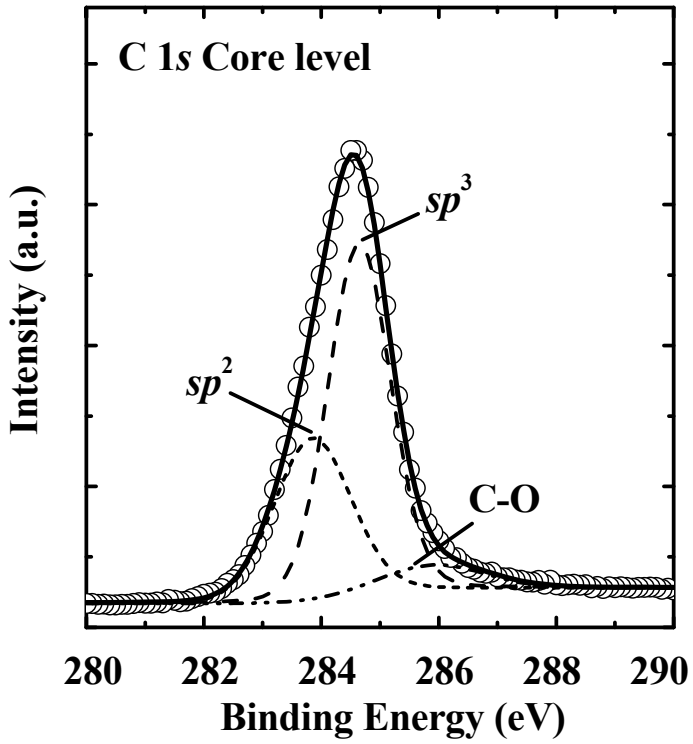


Fig. 4.9. XPS spectrum of the carbon 1*s* core level of the deposited DLC liner, which was fitted by sp^2, sp^3, and C-O bonds.

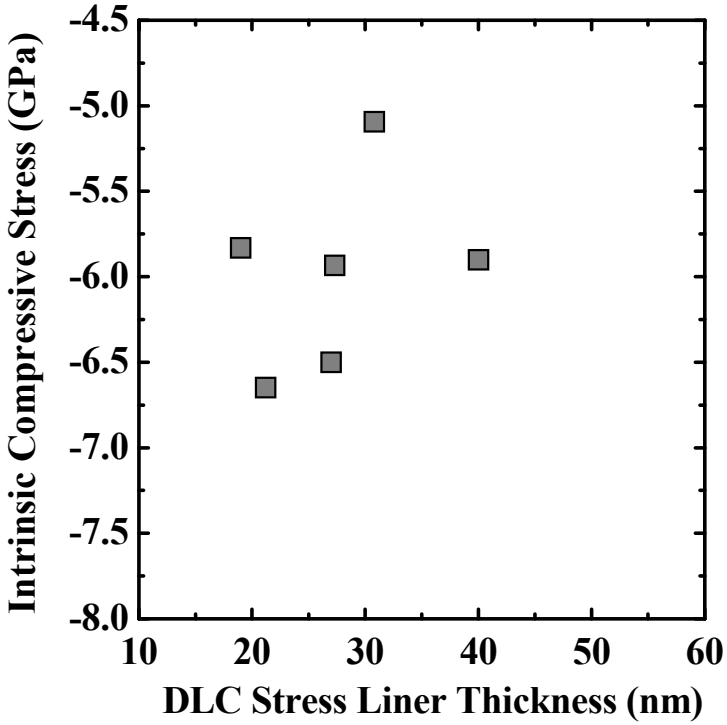


Fig. 4.10. Intrinsic compressive stress of the DLC liner was plotted as a function of the DLC liner thickness [68].

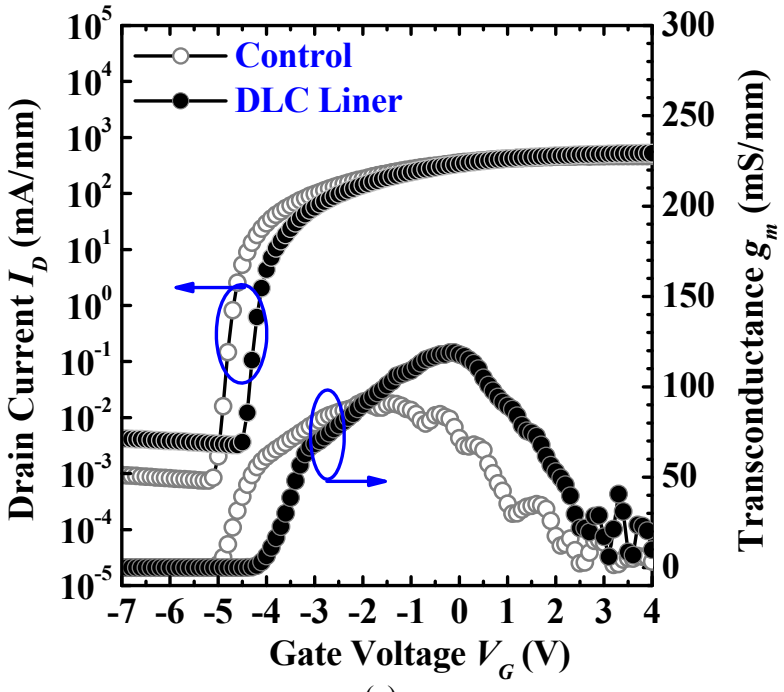
to the total area under the C 1*s* curve. In addition, the intrinsic compressive stress of the DLC liner with various thicknesses was measured using the wafer curvature measurement on the blank silicon wafers and is shown in Fig. 4.10 [68]. In this work, a 40 nm DLC liner with ~ 6 GPa intrinsic compressive stress was employed for the device integration.

4.4 Electrical Characterization of the Devices with and without the Diamond-Like Carbon Liner

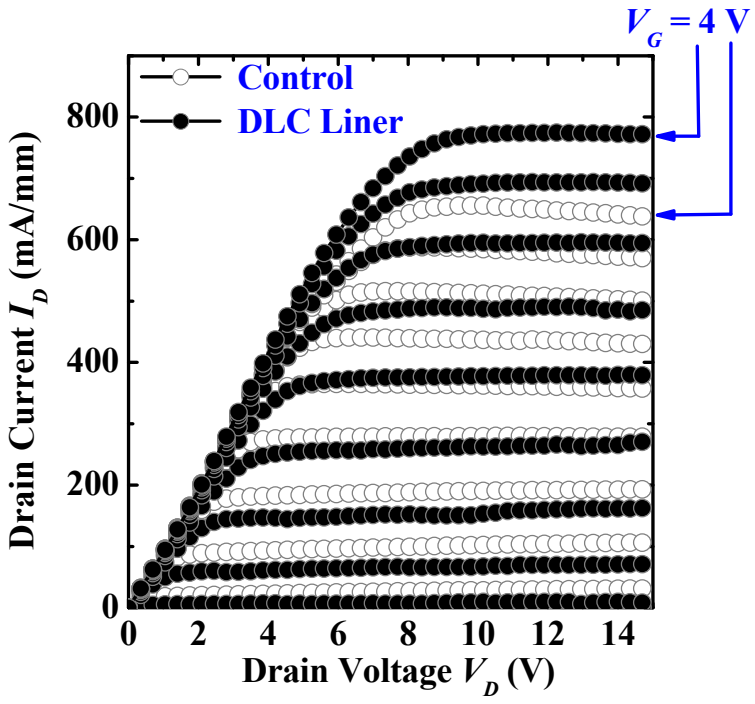
Fig. 4. 11 (a) shows drain current versus gate voltage (I_D-V_G) and extrinsic transconductance versus gate voltage (g_m-V_G) of the AlGaN/GaN MOS-HEMTs (L_G = 400 nm) with and without the DLC liner. Sub-threshold swing for the devices with and without the DLC liner is ~ 110 mV/decade. As shown in Fig. 4.11 (a), the threshold voltage V_{th} for the devices with and without the DLC liner is –3.4 and –4.2 V, respectively. The threshold voltage for a typical AlGaN/GaN MOS-HEMT is expressed as [145]-[148]:

$$V_{th} = \Phi_b - \frac{\Delta E_C}{q} - \frac{qt_1\sigma}{\varepsilon_0\varepsilon_{AlGaN}} - \frac{qt_2\sigma}{\varepsilon_0\varepsilon_{oxide}}, \qquad (4.2)$$

where Φ_b is the Schottky barrier height, ΔE_C is the conduction band offset between AlGaN and GaN, q is the electronic charge, t_1 is the AlGaN barrier layer thickness (20 nm), σ is the polarization charge density, $\varepsilon_0\varepsilon_{AlGaN}$ is the dielectric permittivity of the AlGaN, t_2 is the gate oxide thickness (7 nm), and $\varepsilon_0\varepsilon_{oxide}$ is the dielectric permittivity of the gate oxide. It is assumed that all the terms except the polarization charge density in Equation (4.2) are the same



(a)



(b)

Fig. 4.11. (a) I_D-V_G and g_m-V_G (V_D = 5 V) characteristics of the AlGaN/GaN MOS-HEMTs (L_G = 400 nm) with and without the DLC liner. (b) Output (I_D-V_D) characteristics of the same pair of devices in (a), where V_G is varied in steps of 1 V from –4 to 4 V. 32 % enhancement of saturation current is observed for the device with the DLC liner over the control at $V_G - V_{th}$ of 7 V and V_D of 15 V.

for the devices with and without the DLC liner. Therefore, the change of polarization charge density can be estimated based on the threshold voltage shift ΔV_{th} using the relationship below:

$$\Delta\sigma = \Delta V_{th} / (\frac{qt_1}{\varepsilon_0 \varepsilon_{AlGaN}} + \frac{qt_2}{\varepsilon_0 \varepsilon_{oxide}}) . \quad (4.3)$$

As compared with the control device, there is a 0.8 V threshold voltage shift for the device with the DLC liner. The change of polarization charge density $\Delta\sigma$ is calculated to be 1.80×10^{12} cm^{-2} using Equation (4.3). Based on the polarization charge of 1.38×10^{13} cm^{-2} (Fig. 4.3) under the gate for the control device, the effective polarization charge density under the gate for the device with the DLC liner is calculated to be 1.20×10^{13} cm^{-2}, which is close or consistent to the value of 1.22×10^{13} cm^{-2} obtained from the simulation (Fig. 4.3) and Equation (4.1). As compared to the polarization charge density of 1.38×10^{13} cm^{-2} for the control device, there is ~ 15 % reduction of polarization charge density under the gate for the DLC-strained device.

Based on the calculated polarization charge for AlGaN/GaN MOS-HEMTs with and without the DLC liner shown in Fig. 4.3, Sentaurus TCAD was used to verify the trend of threshold voltage shift. The $Al_{0.25}Ga_{0.75}N$ (20 nm) / GaN (3μm) heterostructure was used in the Sentaurus TCAD. For the control device, the polarization charge used in the simulation at HfAlO/AlGaN and AlGaN/GaN interfaces are -3.14×10^{13} and 1.38×10^{13} cm^{-2}, respectively. For the DCL-stained device, the polarization charge at the AlGaN/GaN interface is non-uniform. In order to introduce non-uniform polarization charge, polarization charge for DLC-strained device shown in Fig. 4.3 was put into the simulation at discreet points in 10 nm intervals at AlGaN/GaAN

interface. For both devices with and without DLC, the donor-like traps of 3.0×10^{13} cm^{-2} located at 0.2 eV above the midgap of AlGaN was introduced at HfAlO/AlGaN interface. Simulated I_D-V_G plots for AlGaN/GaN MOS-HEMTs with and without the DLC liner are shown in Fig. 4.12. As compared to that of control, the threshold voltage for the device with the DLC liner was positively shifted by around 0.8 V. The trend of threshold voltage shift is consistent with the experimental results. As compared with polarization charge of 1.38×10^{13} cm^{-2} at AlGaN/GaN interface for the control, ~0.8 V positive threshold voltage shift was observed for DLC-strained device, which has an effective polarization charge of 1.22×10^{13} cm^{-2} at AlGaN/GaAN interface. It could be implied that every 0.2×10^{13} cm^{-2} polarization charge reduction at AlGaN/GaAN interface could cause about 0.1 V positive threshold voltage shift. In addition, the code used in device simulation was added as Appendix D."

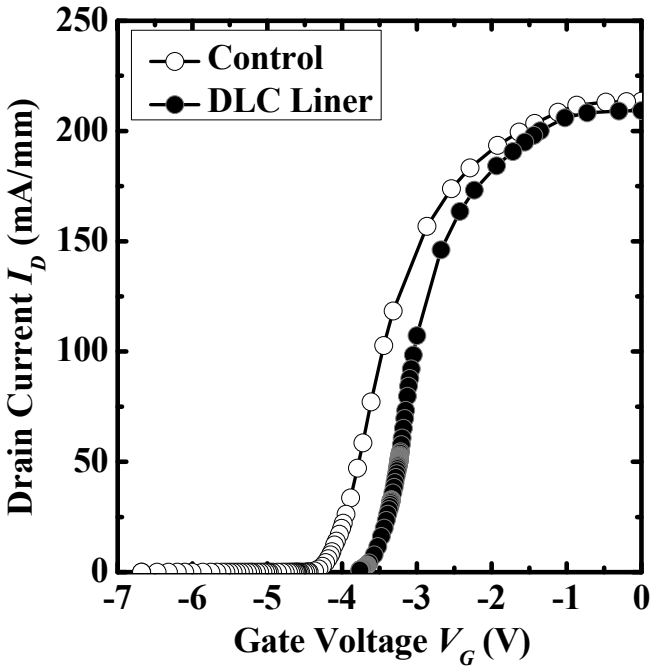


Fig. 4.12. Simulated I_D-V_G plots for AlGaN/GaN MOS-HEMTs with and without the DLC liner. The trend of positive threshold voltage shift is consistent with the experimental results.

Fig. 4.11 (b) shows the drain current versus drain voltage (I_D-V_D) characteristics of the AlGaN/GaN MOS-HEMTs with and without the DLC liner. At a gate overdrive ($V_G - V_{th}$) of 7 V and a drain voltage V_D of 15 V, the drain current for the device with the DLC liner is ~ 735 mA/mm, which is ~32 % higher than ~ 556 mA/mm of the control device. The enhancement of saturation drain current is due to both carrier mobility enhancement and parasitic S/D series resistance reduction, which will be discussed next.

The extrinsic peak transconductance (V_D = 5 V) for the devices with and without the DLC liner are defined to be $g^1_{m,max}$ and $g^0_{m,max}$, respectively. As shown in Fig. 4.11 (a), the values of $g^1_{m,max}$ and $g^0_{m,max}$ are 119 and 92 mS/mm, respectively. The extrinsic transconductance is affected by both carrier mobility μ and parasitic S/D series resistance. Due to the parasitic S/D series resistance, the value of extrinsic transconductance g_m is smaller than that of intrinsic transconductance $g_{m,i}$, which is independent of the parasitic S/D series resistance. $g_{m,i}$ can be extracted using [129]

$$g_{m,i} = g_m / (1 - R_S g_m), \tag{4.4}$$

where R_S is the parasitic source resistance. The value of R_S can be estimated as half of the value of the parasitic S/D series resistance $R_{S/D}$, where $R_{S/D}$ is defined as $R_{S/D} = R_{Total} - R_{Channel}$. R_{Total} is total resistance measured between the source and drain of the device and $R_{Channel}$ is the channel resistance. For a very large gate overdrive $V_G - V_{\text{th}}$ ($V_G - V_{th} >> V_D$) and a fixed small V_D (1 V), $R_{Channel}$ becomes very small compared to $R_{S/D}$, and then $R_{S/D}$ can be estimated from the R_{Total} versus V_G plot. As shown in Fig. 4.13, the calculated $R_{S/D}$ for the devices with and without the DLC liner shown in Fig. 4.11 is 8.8 and 9.8 Ω·mm, respectively. As compare with that of the control, the $R_{S/D}$ for the

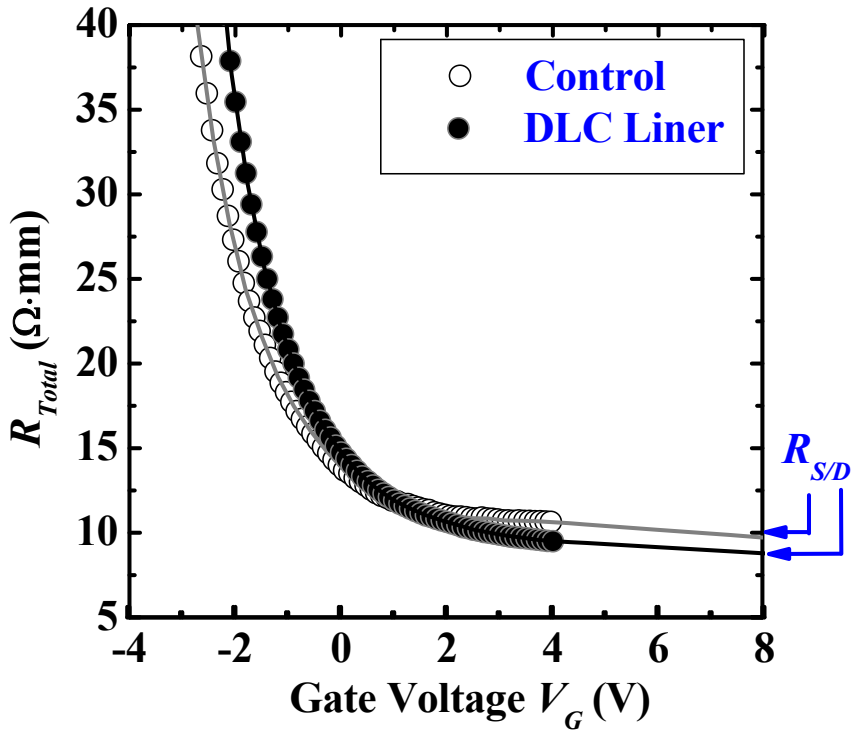


Fig. 4.13. Total resistance R_{Total} as a function of gate voltage V_G when the drain voltage was fixed at 1 V. Parasitic S/D series resistance $R_{S/D}$ for the devices with and without the DLC liner shown in Fig. 4.11 is 8.8 and 9.8 Ω·mm, respectively.

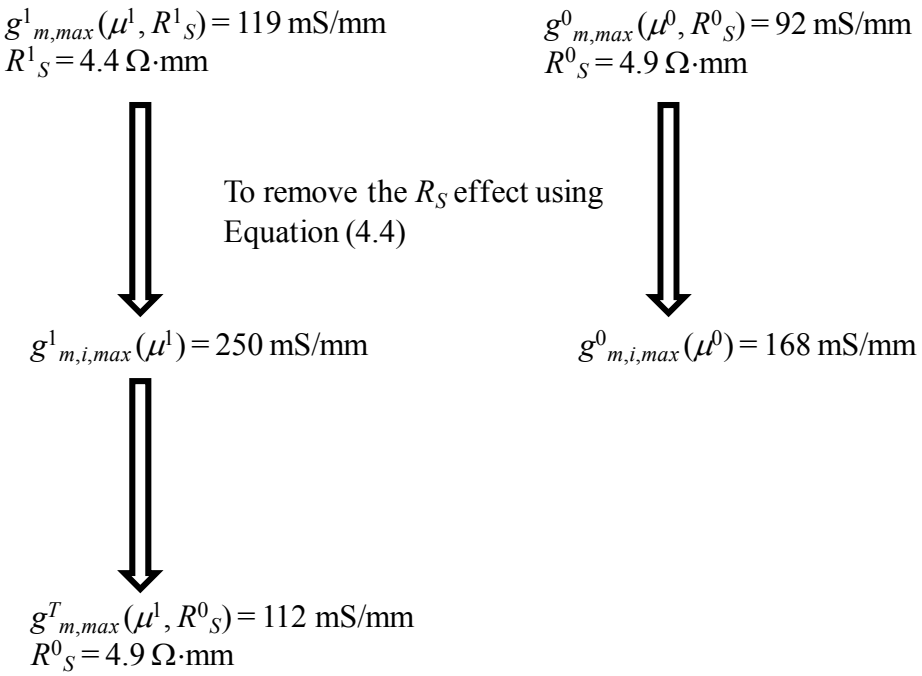
DLC-strained device is reduced by ~ 10 %, and this is due to the increase of polarization charge in the access regions between gate and source/drain pads.

The parasitic source resistance for the devices with and without the DLC liner are defined to be R^1_S and R^0_S, respectively. Therefore, the values of R^1_S and R^0_S are extracted to be 4.4 and 4.9 Ω·mm, respectively. The intrinsic peak transconductance for the devices with and without the DLC liner are defined to be $g^1_{m,i,max}$ and $g^0_{m,i,max}$, respectively. Using the Equation (4.4), the values of $g^1_{m,i,max}$ and $g^0_{m,i,max}$ are extracted to be 250 and 168 mS/mm, respectively. As compared with the control device, the device with the DLC liner shows 49 % enhancement of intrinsic peak transconductance, indicating the carrier mobility μ enhancement for the device with the DLC liner. The carrier mobility μ enhancement for the device with the DLC liner could be due

to the reduced Coulomb carrier scattering, since the polarization charge under the gate is reduced for the DLC-strained device [9]-[10]. As compared to that of the control device, the extrinsic peak transconductance for the device with the DLC liner is increased from 92 from 119 mS/mm, giving a change in $g_{m,max}$ of 27 mS/mm or 29 % enhancement.

Fig. 4.14 (a) shows the procedure to analyze the contribution from carrier mobility μ enhancement and R_S reduction to the enhancement of the extrinsic peak transconductance for the device with the DLC liner. In order to separate carrier mobility μ enhancement and R_S reduction for the enhancement of the extrinsic peak transconductance, an intermediate variable of extrinsic peak transconductance is introduced here. This intermediate extrinsic peak transconductance is defined to $g^T_{m,max}$, which have an intrinsic peak (250 mS/mm) and a source resistance (4.4 Ω·mm). Using Equation (4.4), $g^T_{m,max}$ is calculated to be 112 mS/mm. As illustrated by Fig. 4.14 (b), the enhancement of the extrinsic peak transconductance due to the carrier mobility μ enhancement can be estimated based on the difference between $g^T_{m,max}$ and $g^0_{m,max}$, as source resistance for $g^T_{m,max}$ and $g^0_{m,max}$ is the same. Similarly, the enhancement of the extrinsic peak transconductance due to R_S reduction can be estimated based on the difference between $g^T_{m,max}$ and $g^1_{m,max}$, as carrier mobility for $g^T_{m,max}$ and $g^1_{m,max}$ is the same. As shown in Fig. 4.14 (b), the percentage contribution to the extrinsic peak transconductance enhancement from carrier mobility μ enhancement and R_S reduction is 74 % and 26 %, respectively.

(a) **Device with the DLC stress liner** **Control**



(b)

Difference between		**Due to the difference in**
$g^1_{m,max}(\mu^1, R^1_S)$ and $g^0_{m,max}(\mu^0, R^0_S)$	27 mS/mm	μ and R_S
$g^T_{m,max}(\mu^1, R^0_S)$ and $g^0_{m,max}(\mu^0, R^0_S)$	20 mS/mm or 74 % of 27 mS/mm	μ
$g^T_{m,max}(\mu^1, R^0_S)$ and $g^1_{m,max}(\mu^1, R^1_S)$	7 mS/mm or 26 % of 27 mS/mm	R_S

Fig. 4.14. (a) Schematic illustrating the extraction of $g^1_{m,i,max}$, $g^0_{m,i,max}$, and $g^T_{m,i,max}$, to analyze the contribution from carrier mobility enhancement and R_S reduction to the total extrinsic peak transconductance enhancement using Equation (4.4). Here, the carrier mobility for devices with and without the DLC liner is μ^1 and μ^0, respectively. (b) By comparing among $g^1_{m,max}$, $g^0_{m,max}$, and $g^T_{m,max}$, the contribution from carrier mobility μ enhancement and R_S reduction can be separated.

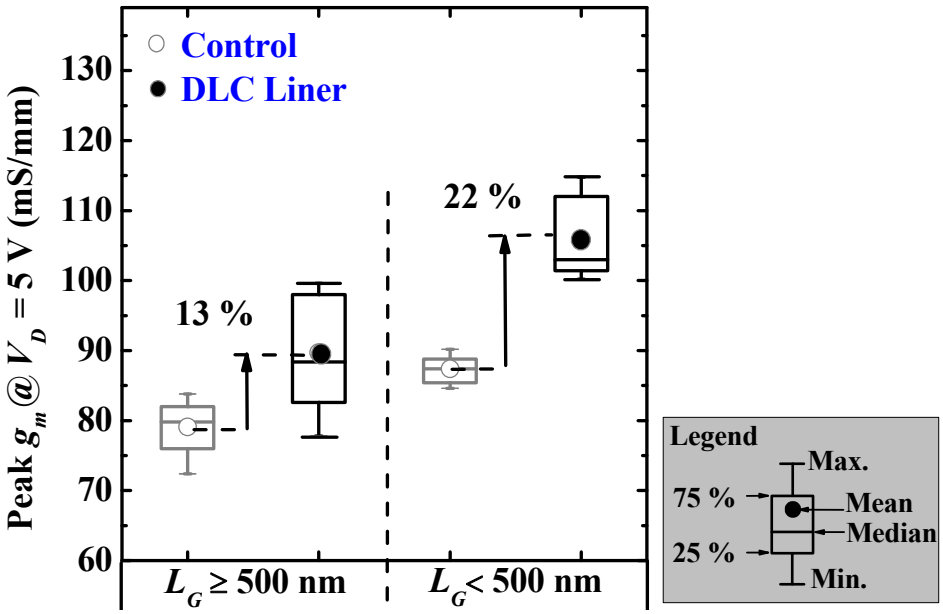


Fig. 4.15. The extrinsic peak transconductance $g_{m,max}$ of the AlGaN/GaN MOS-HEMTs with the DLC liner shows enhancement over the control devices at V_D = 5 V. The extrinsic peak transconductance enhancement is larger for the devices with L_G less than 500 nm than that of the devices with L_G more than 500 nm. The device length here varies from 300 to 1000 nm.

Fig. 4.15 shows the dependence of DLC-induced $g_{m,max}$ enhancement on the gate length L_G of the fabricated devices. As compared with the control devices, DLC-induced $g_{m,max}$ enhancement is 22 % for the DLC-strained devices with L_G less than 500 nm and 13 % for the DLC-strained devices with L_G larger than 500 nm. As L_G is reduced, the $g_{m,max}$ enhancement is increased. As discussed in Fig. 4.5, a 40 nm thick DLC liner induces a higher compressive channel stress for the devices with shorter L_G. This compressive stress reduces the polarization charge under the gate, thus reducing the Coulomb carrier scattering.

4.5 Summary

The effect of a DLC liner on the electrical characteristics of AlGaN/GaN MOS-HEMTs was studied. The compressive stress induced by the DLC liner in the channel under the gate reduces the tensile strain in the AlGaN barrier layer, leading to a reduction in polarization charge density through the piezoelectric polarization effect, and further causes a positive threshold voltage shift for the AlGaN/GaN MOS-HEMTs with the DLC liner. In addition, tensile stress induced by the DLC liner in the regions between gate and source/drain contacts reduces the source/drain series resistance, due to the increase of polarization charge density in the access regions between gate and source/drain contacts.

Chapter 5

High Voltage AlGaN/GaN MOS-HEMTs with a Complementary Metal-Oxide-Semiconductor Compatible Gold-free Process

5.1 Introduction

Owing to GaN's large breakdown electric field and wide energy bandgap, AlGaN/GaN high-electron-mobility transistors (HEMTs) are promising for power electronic applications, such as high voltage and high power switches used in power-factor-correction circuits and uninterruptible power supplies [110]. GaN power devices with outstanding performance that exceeds the limit of silicon devices have been reported [34], [149]-[157]. AlGaN/GaN HEMTs formed on a sapphire substrate have achieved a high breakdown voltage V_{BR} of 10.4 kV and an on-state resistance R_{on} of 186 $m\Omega \cdot cm^2$ [158]. InAlN/GaN metal-oxide-semiconductor HEMTs (MOS-HEMTs) formed on a SiC substrate have also achieved a high breakdown voltage V_{BR} of 3000 V and an on-state resistance R_{on} of 4.25 $m\Omega \cdot cm^2$ [159]. For AlGaN/GaN MOS-HEMTs formed on silicon substrate, breakdown voltage up to 2500 V has also been reported [160]. In addition, voltage boost converters employing AlGaN/GaN HEMTs-on-SiC, -on-sapphire or -on-silicon have achieved high power efficiency at a switching frequency of 1 MHz [161]-[163]. A single chip voltage boost converter using a

monolithically integrated AlGaN/GaN-on-silicon rectifier and a normally-off AlGaN/GaN HEMT has also been demonstrated [164].

The approach of fabricating AlGaN/GaN HEMTs on silicon substrate has attracted increasing attention due to the availability of cheap, high-quality, and large-diameter GaN-on-silicon substrates. Recently, the growth of GaN epitaxial layers on 150 and 200 mm silicon substrate with crack-free and pit-free surfaces has been reported [31]-[32], [165]-[166]. GaN-on-silicon wafers with a large diameter could enable cost-effective fabrication of GaN power devices in silicon foundries. In addition, AlGaN/GaN HEMTs have been heterogeneously integrated with silicon devices on a single wafer by wafer bonding to realize functional diversification in integrated circuits [167]-[168].

Most of the reported GaN devices employed gold-bearing structures, in which gold was used either as the gate or source/drain contacts. However, in silicon complementary metal-oxide-semiconductor (CMOS) foundries, gold is typically not allowed, because gold could introduce deep-level traps in silicon and these gold related traps are the carrier recombination centers which can reduce the carrier lifetime in silicon [169]. Therefore, CMOS compatible gold-free process is essential for GaN devices to be fabricated using the

Table 5.1. Reports of AlGaN/GaN MOS-HEMTs with a CMOS compatible gold-free process [156]-[157], [172] and key device parameters.

Ref.	On-state Resistance R_{on} (mΩ·cm^2)	Breakdown Voltage V_{BR} (V)	Gate-to-drain Spacing L_{GD} (μm)
[156]	2.6	640	7.5
[157]	0.0047	87	1.5
[172]	2.9	770	9.5

facilities in silicon foundries. Table 5.1 summarizes the breakdown voltage V_{BR}, on-state resistance R_{on}, and gate-to-drain spacing L_{GD} of AlGaN/GaN MOS-HEMTs using a CMOS compatible gold-free process reported so far [156], [157], [172], and the highest breakdown voltage of 770 V was achieved by M. V. Hove *et al*. [172].

As discussed in Chapters 2 and 3, AlGaN/GaN HEMTs with a Schottky gate typically suffer from a high gate leakage current, leading to reliability issues and a lower breakdown voltage [121]. An effective way to suppress the gate leakage current is to fabricate AlGaN/GaN MOS-HEMTs by inserting a layer of gate dielectric between the gate electrode and the AlGaN barrier layer [173]-[175]. A preferred gate dielectric should have a high dielectric constant to achieve a high gate-to-channel capacitance and transconductance for a given physical thickness. Furthermore, a large conduction band offset between the gate dielectric and AlGaN/GaN helps to suppress the gate leakage current. Al_2O_3 has a large bandgap E_G (~ 7 eV) [172], a relatively high dielectric constant ε_r (~ 9) [96], [172], and a high breakdown field (~ 10 MV/cm) [172], making it attractive for application in high voltage AlGaN/GaN MOS-HEMTs.

In this Chapter, Al_2O_3 deposited by atomic layer deposition (ALD) was chosen as the gate dielectric for the fabrication of AlGaN/GaN MOS-HEMTs using a CMOS compatible gold-free process. Section 5.2 reports the fabrication and characterization of AlGaN/GaN-on-silicon MOS-HEMTs, which achieve a breakdown voltage V_{BR} of 800 V and an on-state resistance R_{on} of 3 mΩ·cm^2. Section 5.3 reports the demonstration of AlGaN/GaN-on-

sapphire MOS-HEMTs with a breakdown voltage V_{BR} of 1400 V and an on-state resistance R_{on} of 22 mΩ·cm^2.

5.2 High Voltage AlGaN/GaN-on-Silicon MOS-HEMTs

In this Section, the fabrication and characterization of AlGaN/GaN-on-silicon MOS-HEMTs using a CMOS compatible gold-free process will be discussed. Devices with a gate-to-drain spacing L_{GD} of 5 μm achieved a breakdown voltage V_{BR} of 800 V and an on-state resistance R_{on} of 3 mΩ·cm^2. In addition, sub-threshold swing S of ~ 97 mV/decade and current on/off, I_{on}/I_{off}, ratio of ~ 10^6 were obtained.

5.2.1 Fabrication of AlGaN/GaN-on-Silicon MOS-HEMTs using a CMOS Compatible Gold-Free Process

The epitaxial layer structure used in this study was purchased from DOWA and grown metal-organic chemical vapor deposition (MOCVD) on a 4 inch p-type silicon (111) substrate. The AlGaN/GaN HEMT structure consists of a 25 nm thick undoped $Al_{0.25}Ga_{0.75}N$ barrier layer, a 1.5 μm thick undoped GaN layer, and a 3.3 μm thick buffer made of multi-pairs of alternate AlN/GaN layer [18], [19], [22]. A thick buffer layer not only promotes good quality of GaN layer with a smooth surface, but also suppresses the leakage current in both lateral and vertical directions of the devices, thereby enhancing the breakdown voltage [75].

After the active region or mesa was formed by Cl_2-based reactive ion etching (detailed etching conditions have been mentioned in Chapter 3), pre-gate cleaning for all samples was performed. The pre-gate cleaning consisted

of a 2-minute acetone and a 3-minute isopropanol degreasing step, followed by a 10-minute dilute HCl ($HCl:H_2O=1:1$) native oxide removal step and an *ex situ* surface passivation step in an undiluted $(NH_4)_2S$ solution for 30 minutes at room temperature (25 ºC). An Al_2O_3 gate dielectric (10 nm) was then deposited by ALD, and followed by a post deposition annealing (PDA) at 450 ºC for 60 s in N_2 ambient.

Reactive sputter deposition of TaN (100 nm), photolithography, and Cl_2-based plasma etch were performed for the gate electrode definition. A 80 nm thick SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD) to encapsulate the devices, followed by contact hole opening. An Al (71 nm) on Ti (30 nm) stack was deposited by an electron beam (E-Beam) evaporator and patterned in the source/drain contact regions. An alloying process at 650 ºC for 30 s in N_2 ambient was used to form the ohmic contacts. In this work, the devices have a gate length L_G of 2 μm, a gate-to-source spacing L_{GS} of 5 μm, and a gate-to-drain spacing L_{GD} of 5 μm. All processing steps, except the MOCVD growth of nitride materials, were performed by the author.

5.2.2 Device Characterization and Analysis

Fig. 5.1 (a) shows a cross-sectional transmission electron microscopy (TEM) image of a gate stack of the fabricated AlGaN/GaN MOS-HEMT (L_G of 2 μm). Fig. 5.1 (b) shows a zoomed-in image of a $TaN/Al_2O_3/AlGaN$ gate stack, where an atomically sharp interface between Al_2O_3 and AlGaN is

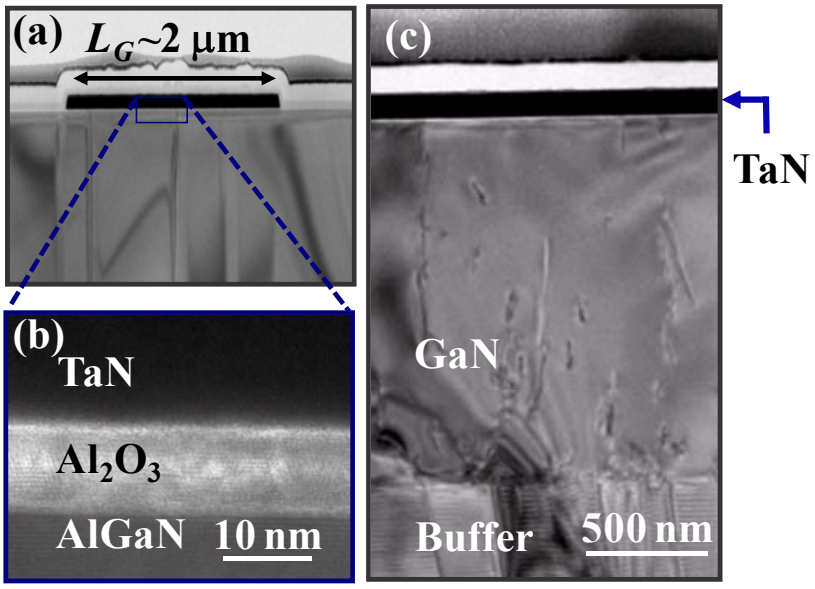
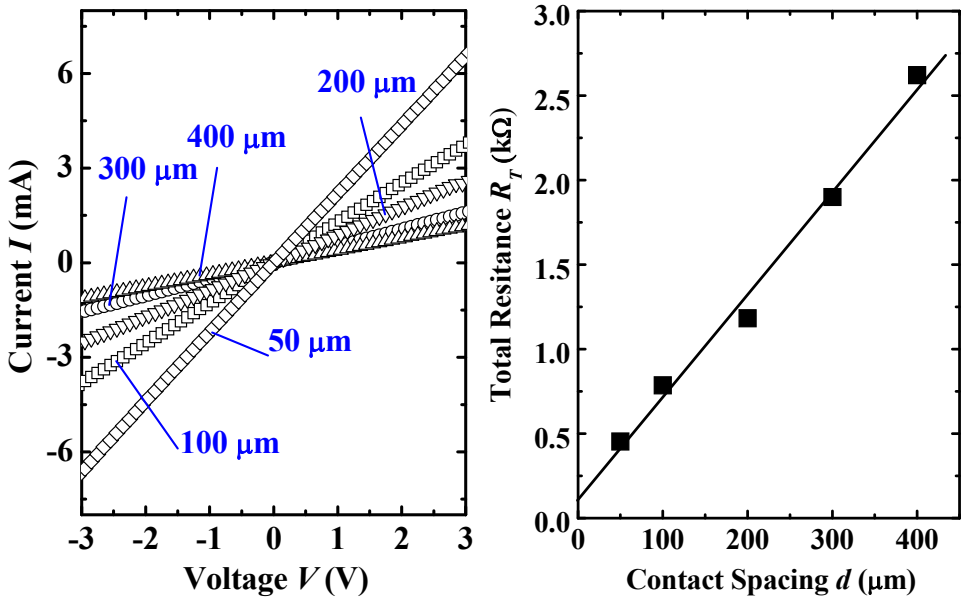


Fig. 5.1. (a) Cross-sectional TEM image of a gate stack of the fabricated AlGaN/GaN MOS-HEMT. (b) Zoomed-in image of a TaN/Al_2O_3/AlGaN stack. (d) Cross-sectional TEM image of the TaN/Al_2O_3/AlGaN/GaN/Buffer.



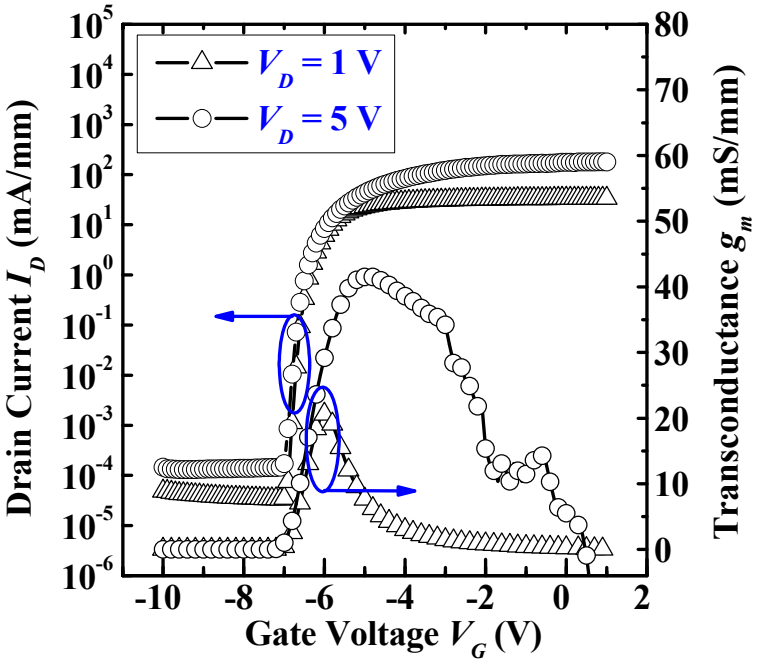
(a) (b)

Fig. 5.2. (a) Current-voltage (I-V) characteristics and (b) total resistance R_T as a function of contact spacing d of the transmission line method (TLM) test structure, fabricated on the same die as the AlGaN/GaN MOS-HEMT in Fig. 5.1, after an annealing step at 650 °C for 30 s in N_2 ambient.

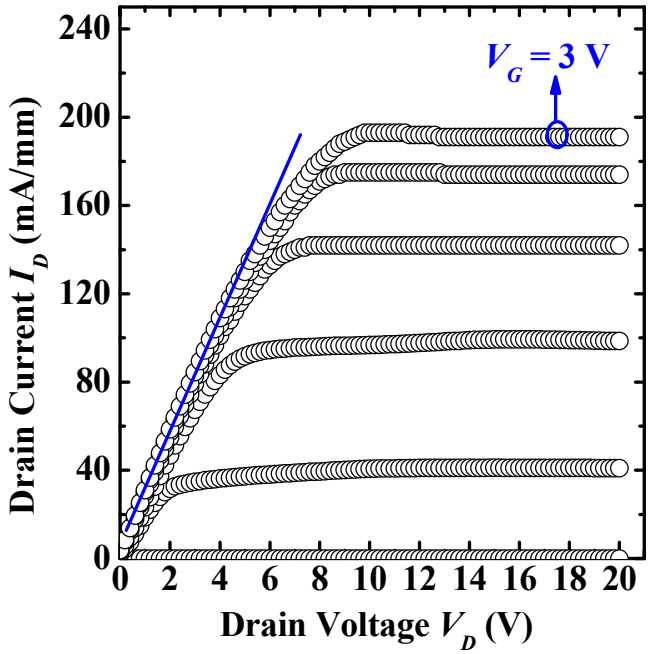
observed. Fig. 5.1 (c) shows a cross-sectional TEM image of a TaN/Al_2O_3/AlGaN/GaN/buffer. As shown in Fig. 5.2, a sheet resistance R_{sh} of 607 Ω/square and a specific contact resistivity ρ_c of 2.1×10^{-3} Ω·cm^2 were obtained from a fabricated transmission line method (TLM) test structure. Lower specific contact resistivity could be obtained by using a higher contact annealing temperature, such as 800 °C [176]. However, as a gate-first process was adopted in this work, a higher contact annealing temperature could degrade the quality of gate stack, leading to a larger sub-threshold swing and a higher off-state current.

Fig. 5.3 (a) shows drain current versus gate voltage (I_D-V_G) and extrinsic transconductance versus gate voltage (g_m-V_G) characteristics of the AlGaN/GaN MOS-HEMTs (L_G = 2 μm). The threshold voltage V_{th} is –6.3 V using the peak g_m (V_D = 1 V) extrapolation method [177]. Sub-threshold swing S and peak g_m (V_D = 5 V) are 90 mV/decade and 41.6 mS/mm, respectively. Fig. 5.3 (b) shows the drain current versus drain voltage (I_D-V_D) characteristics of the same device shown in Fig. 5.3 (a). The gate voltage V_G is varied in steps of 2 V from –7 to 3 V. An on-state resistance R_{on} of 3 mΩ·cm^2 was extracted from the slope of the I_D-V_D plot in the linear region with the consideration of the device active area between the source and drain ohmic contacts.

Fig. 5.4 shows the sub-threshold swing S (left axis) and I_{on}/I_{off} ratio (right axis) as a function of the gate leakage current I_G. I_{on} and I_{off} are defined to be the values of I_D measured at $V_G = V_{th} + 6$ V and $V_{th} - 4$ V, respectively, at V_D = 5 V. I_G was measured at $V_G = V_{th} - 4$ V and V_D = 5 V. The devices



(a)



(b)

Fig. 5.3. (a) I_D-V_G and g_m-V_G characteristics of the fabricated AlGaN/GaN MOS-HEMT (L_G = 2 μm). Sub-threshold swing S is 90 mV/decade, peak g_m is 41.9 mS/mm at V_D = 5 V, and the threshold voltage V_{th} is around −6.3 V. (b) Output (I_D-V_D) characteristics of AlGaN/GaN MOS-HEMTs (L_G = 2 μm), where V_G is varied in steps of −2 V from 3 to −7 V.

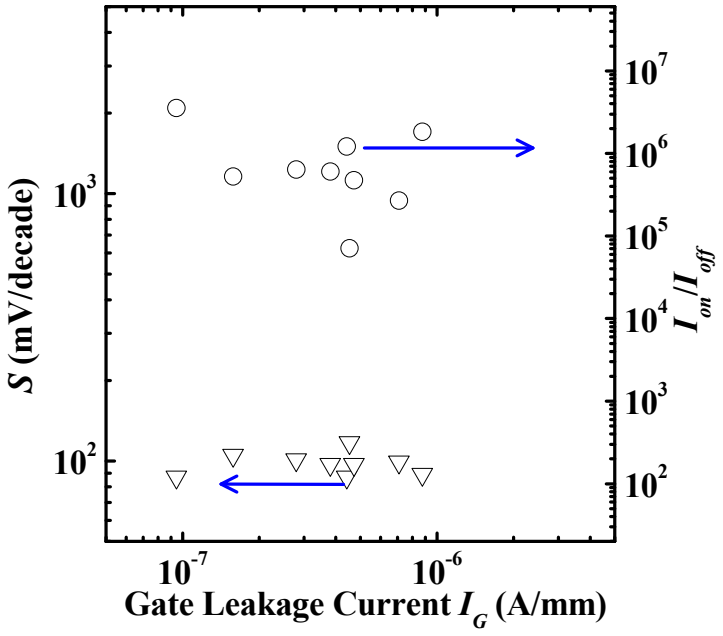


Fig. 5.4. Sub-threshold swing S (left axis) and I_{on}/I_{off} ratio (right axis) as a function of the gate leakage current I_G for the AlGaN/GaN MOS-HEMTs.

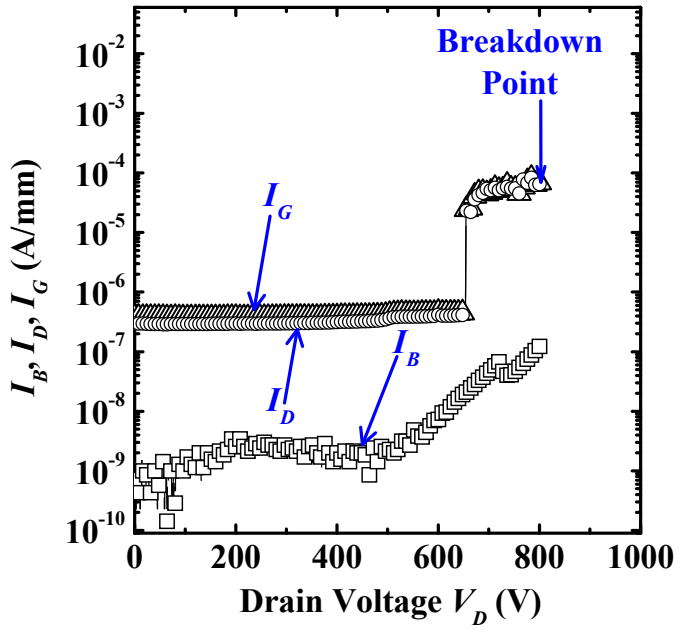
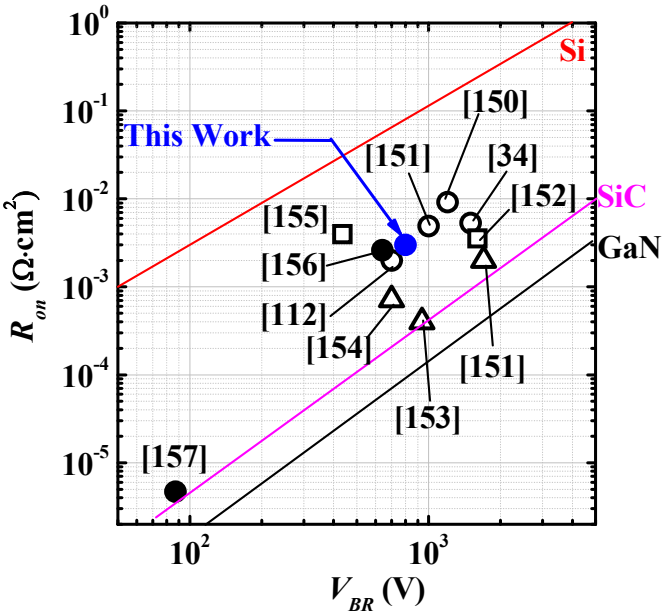


Fig. 5.5. Substrate current I_B, drain current I_D, and gate current I_G of the fabricated AlGaN/GaN MOS-HEMTs as functions of drain voltage V_D for the four-terminal off-state measurement in Fluorinert ambient (L_G = 2 μm, $L_{GS} = L_{GD}$ = 5 μm), where $V_S = V_B$ = 0 V and V_G = –12 V.

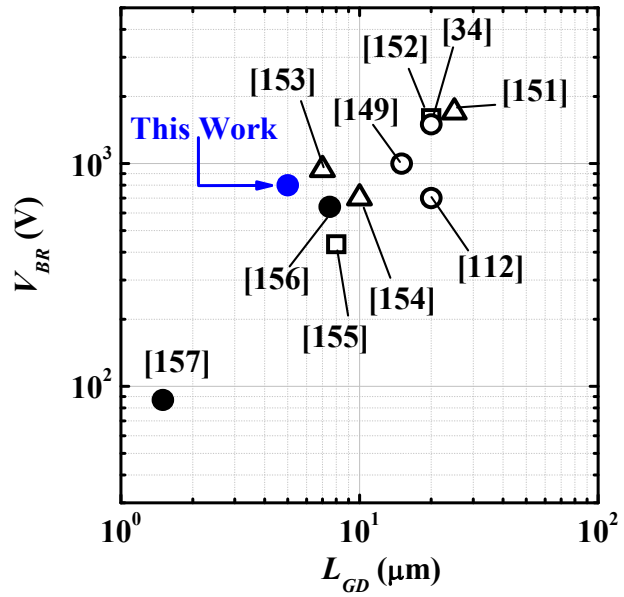
shown in Fig. 5.4 have a mean S of 97.7 mV/decade, a mean I_{on}/I_{off} ratio of 1.0 $\times 10^6$, and a mean I_G of 1.02 $\times 10^{-6}$ A/mm. Device-to-device variation in I_G, I_{on}/I_{off} ratio, and S is possibly due to the variation of the interface trap density at the Al_2O_3/AlGaN interface [48].

A four-terminal off-state breakdown measurement was carried out in Fluorinert ambient to prevent any atmospheric surface flashover in gate-to-drain access regions [150]. During the measurement, the source and silicon substrate were grounded, and the TaN gate was biased at −12 V. The breakdown voltage V_{BR} is defined as the value of drain voltage V_D at which drain current I_D reaches 1 mA/mm with the gate biased below V_{th}. As shown in Fig. 5.5, the substrate current I_B is ~ 1 $\times 10^{-7}$ A/mm at V_D = 800 V, indicating that the vertical breakdown voltage is more than 800 V [22]. The drain current I_D remains ~ 3.8 $\times 10^{-7}$ A/mm until V_D = 650 V and is below 1 mA/mm when V_D = 800 V. The breakdown could be due to the impact ionization at the drain side of the gate edge [178].

Fig. 5.6 (a) shows a comparison of breakdown voltage V_{BR} versus on-state resistance R_{on} between this work and other state-of-the-art AlGaN/GaN MOS-HEMTs. As shown in Fig. 5.6 (a), AlGaN/GaN-on-SiC MOS-HEMTs achieve a lower on-state resistance, as compared with AlGaN/GaN-on-silicon and AlGaN/GaN-on-sapphire MOS-HEMTs. This could be due to the higher quality of epitaxial layer on SiC wafers. Fig. 5.6 (b) shows a comparison of breakdown voltage V_{BR} versus gate-to-drain spacing L_{GD} between this work and other state-of-the-art AlGaN/GaN MOS-HEMTs. This work achieved a breakdown voltage V_{BR} of 800 V. Compared with those of gold-free AlGaN/GaN-on-silicon MOS-HEMTs having a gate-to-drain spacing L_{GD}



(a)



(b)

Fig. 5.6. (Open symbol: AlGaN/GaN MOS-HEMTs with gold; Solid symbol: AlGaN/GaN MOS-HEMTs without gold; Square: AlGaN/GaN-on-sapphire; Triangle: AlGaN/GaN-on-SiC; Circle: AlGaN/GaN-on-silicon) (a) Breakdown voltage V_{BR} versus on-state resistance R_{on} of the fabricated AlGaN/GaN MOS-HEMTs, as compared with those of state-of-the-art AlGaN/GaN MOS-HEMTs. (b) Breakdown voltage V_{BR} versus gate-to-drain spacing L_{GD} of the fabricated AlGaN/GaN MOS-HEMTs, as compared with those of state-of-the-art AlGaN/GaN MOS-HEMTs. On-state resistance was extracted using the device active area between the ohmic contacts, and large electrode pads were not included here.

of less than 10 μm, the breakdown voltage V_{BR} achieved in this work is the highest reported to date [156], [157], [172]. In addition, high voltage measurement was carried out on the devices with various gate-to-drain spacing L_{GD}, where the gate length L_G and gate-to-source spacing L_{GS} were fixed at 2 and 5 μm, respectively. As shown in Fig. 5.7, the breakdown voltage was almost constant with respect to the gate-to-drain spacing, this could be due to the vertical breakdown [179].

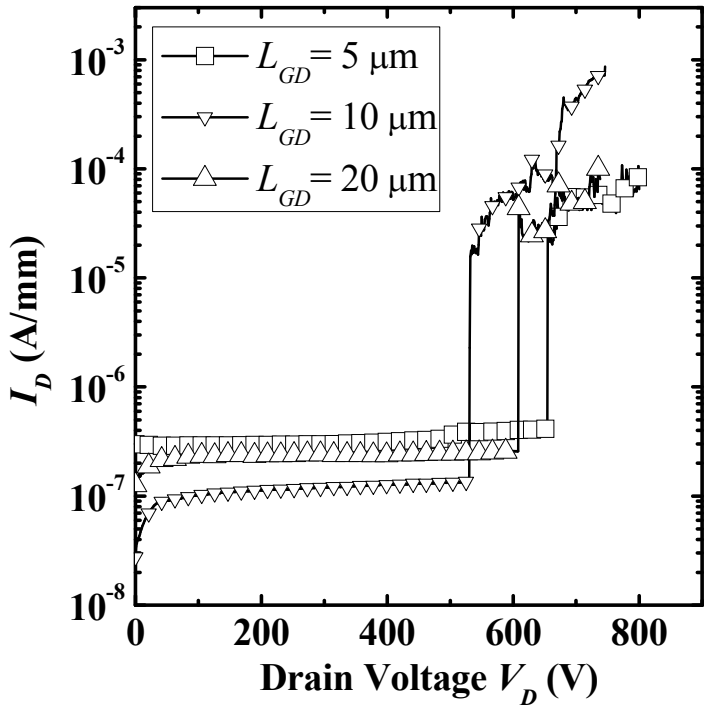


Fig. 5.7 Drain current I_D was plotted as a function of drain voltage V_D during the four-terminal off-state measurement in the Fluorinert ambient, where $V_S = V_B = 0$ V and $V_G = -12$ V. Devices have a gate length L_G of 2 μm, L_{GS} of 5 μm, and various L_{GD}.

5.3 High Voltage AlGaN/GaN-on-Sapphire MOS-HEMTs

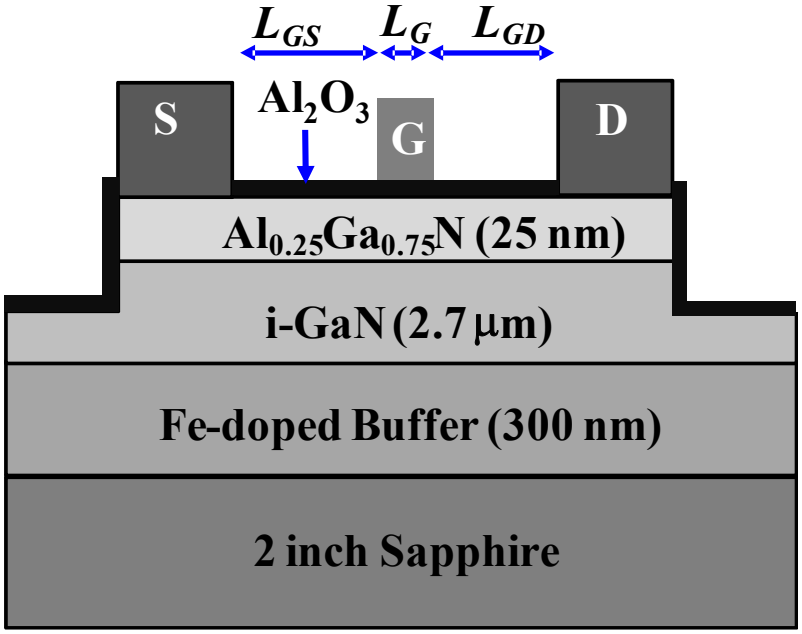
In the previous Section 5.2, high voltage AlGaN/GaN-on-silicon MOS-HEMTs were discussed. In this section, the fabrication and characterization of AlGaN/GaN-on-sapphire MOS-HEMTs using a CMOS compatible gold-free process will be discussed. Devices with a gate-to-drain spacing L_{GD} of 20 μm achieved a breakdown voltage V_{BR} of 1400 V and an on-state resistance R_{on} of 22 mΩ·cm^2. In addition, high current on/off, I_{on}/I_{off}, ratio of ~ 10^9 and low gate leakage current I_G of ~ 10^{-11} A/mm were obtained.

5.3.1 Fabrication of AlGaN/GaN-on-Sapphire MOS-HEMTs using a CMOS Compatible Gold-Free Process

The AlGaN/GaN structure used in this study was purchased from Nippon Telegraph and Telephone Advanced Technology (NTT-AT) and grown by MOCVD on a 2 inch sapphire substrate. The epi-layers consist of a 25 nm thick undoped $Al_{0.25}Ga_{0.75}N$ barrier layer, a 2.7 μm thick undoped GaN layer, and a 300 nm thick Fe-doped GaN buffer with a doping concentration of 4×10^{17} cm^{-3}. Fe-doped GaN buffer not only can reduce the dislocation density of GaN layer, but also compensate the background doping, thereby making the GaN layer highly resistive and increase the vertical breakdown voltage of the devices [17]. Fig. 5.8 (a) illustrates the gold-free process flow employed in the fabrication of AlGaN/GaN-on-sapphire MOS-HEMTs. Mesa isolation was first realized by Cl_2 (10 sccm) / BCl_3 (20 sccm) reactive ion etching (RIE) using an ICP system at a chamber pressure of 5 mTorr and a

- 2 inch AlGaN/GaN epi wafer on Al_2O_3
- Active region formation using RIE
- Gate stack formation:
  - Pre-gate cleaning: Acetone, IPA, HCl, $(NH_4)_2S$
  - Al_2O_3 deposition and PDA
  - Metal gate deposition and gate patterning
- Contact patterning and Pt/Ti/Al/Ti deposition
- Ohmic contact alloying (650 °C, 30 s)

(a)



(b)

Fig. 5.8. (a) Process flow employed in the fabrication of gold-free AlGaN/GaN-on-sapphire MOS-HEMTs. (b) Schematic of an AlGaN/GaN-on-sapphire MOS-HEMT, where the gate electrode is TaN, and the source/drain electrodes are Pt/Ti/Al/Ti (from top layer to bottom layer).

chuck temperature of 6 ºC. Pre-gate cleaning for all samples comprised a 2-minute acetone and a 3-minute isopropanol degreasing step, followed by a 10-minute dilute HCl ($HCl:H_2O$ = 1:1) native oxide removal step and an *ex situ* surface passivation step in an undiluted $(NH_4)_2S$ solution for 30 minutes at room temperature. An Al_2O_3 gate dielectric (15 nm) was deposited by ALD at a temperature of 250 ºC and a chamber pressure of 25 mTorr using trimethylaluminum as a precursor. The deposition rate of Al_2O_3 was 0.12 nm/cycle. PDA at 450 ºC for 60 s in N_2 ambient was then performed.

Immediately after the PDA, TaN (100 nm) was deposited as the gate metal at a pressure of 3 mTorr by a magnetron sputtering system. The process was carried out at a DC power of 250 W for the Ta target and a N_2 flow rate of 5 sccm. This was followed by photo-lithography and Cl_2-based plasma etching of TaN (the flow rate of Cl_2 was 200 sccm and the chamber pressure was 10 mTorr) for the gate electrode definition. After the source/drain (S/D) contact patterning, a metal stack consisting of Pt (100 nm) / Ti (20 nm) / Al (120 nm) / Ti (10 nm) (from top layer to bottom layer) was deposited as the source/drain contacts using an E-Beam evaporator at a pressure of 1×10^{-6} Torr, followed by a lift-off process. Finally, an alloying process was performed at 650 ºC for 30 s in N_2 ambient to form the S/D ohmic contacts. A schematic of an AlGaN/GaN-on-sapphire MOS-HEMT is shown in Fig. 5.8 (b), where the gate length, gate-to-source spacing, and gate-to-drain spacing of AlGaN/GaN MOS-HEMTs are defined as L_G, L_{GS}, and L_{GD}, respectively.

5.3.2 Device Characterization and Analysis

Fig. 5.9 (a) shows the current-voltage (*I-V*) characteristics of the TLM test structure fabricated on the same die as the AlGaN/GaN-on-sapphire MOS-HEMTs. Fig. 5.9 (b) shows the total resistance R_T as a function of contact spacing d (50, 100, 200, 300, and 400 μm) for the TLM structure. A sheet resistance R_{sh} of 527 Ω/square and a specific contact resistivity ρ_c of 4.5×10^{-3} Ω·cm^2 were obtained from a fabricated TLM structure. Lower contact resistivity can be obtained by using a higher contact annealing temperature [177]. However, as a gate-first process was adopted, a higher contact annealing temperature could degrade the quality of TaN/Al_2O_3/AlGaN/GaN gate stack, leading to a larger sub-threshold swing and a higher off-state

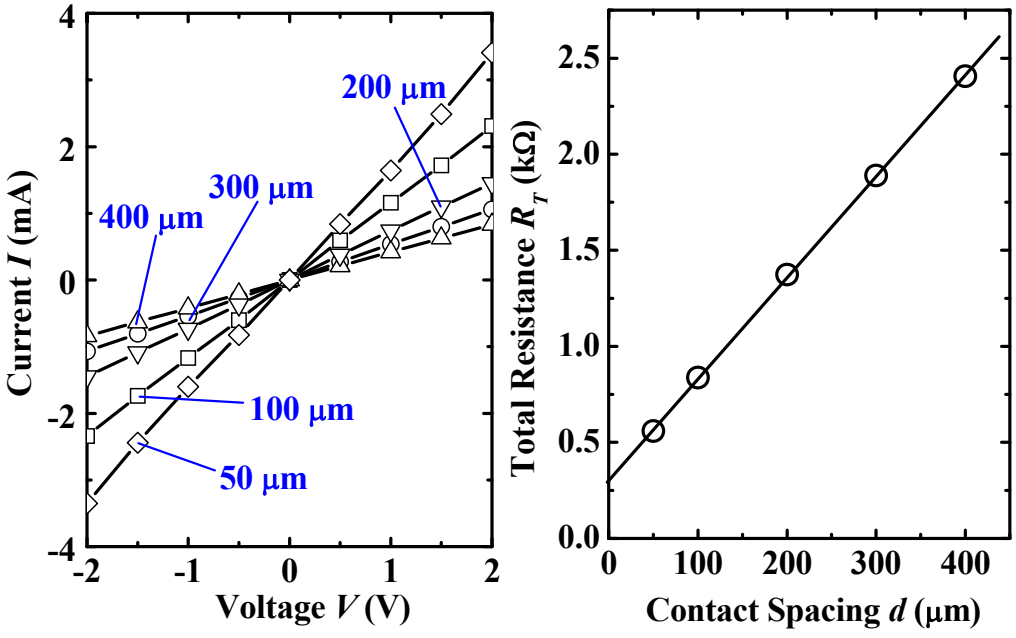


Fig. 5.9. (a) Current-voltage (*I-V*) characteristics and (b) total resistance R_T as a function of contact spacing d for the TLM test structure, fabricated on the same die as the AlGaN/GaN-on-sapphire MOS-HEMTs, after an annealing step at 650 °C for 30 s in N_2 ambient.

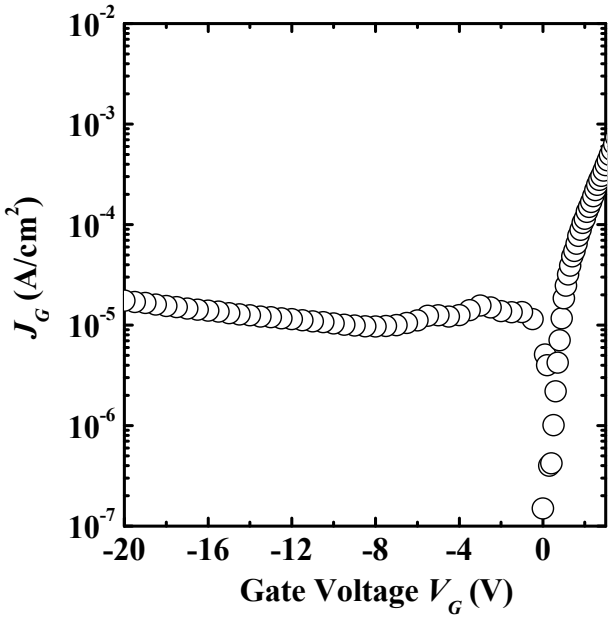
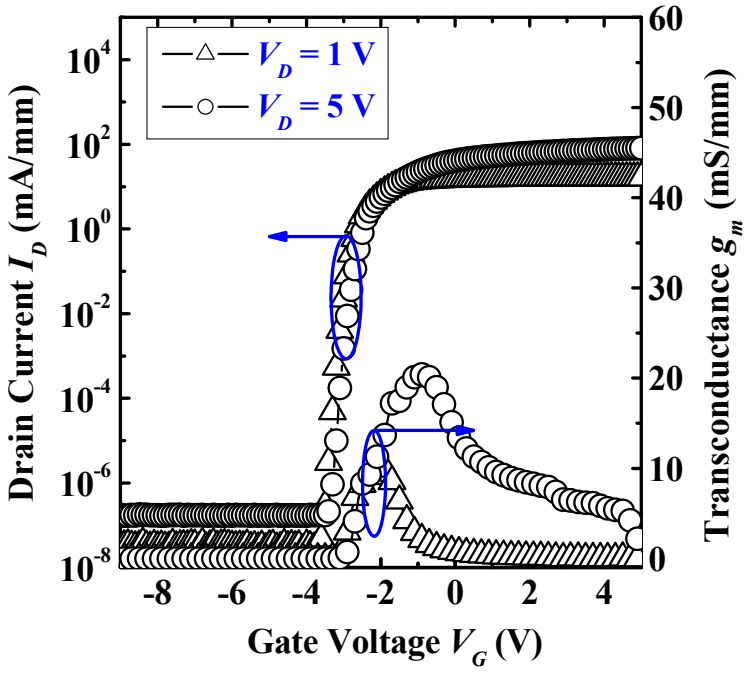
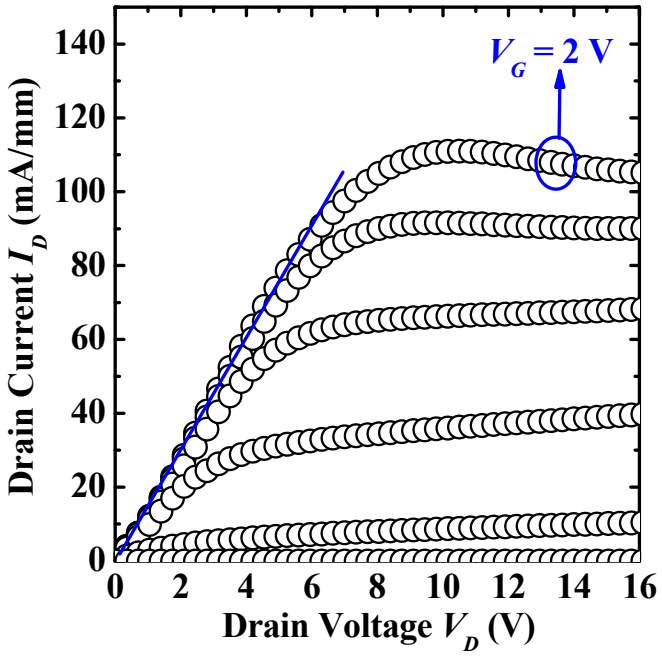


Fig. 5.10. Gate leakage current density J_G as a function of gate voltage V_G of the fabricated AlGaN/GaN MOS-HEMTs, when both source and drain were grounded. In the negative gate voltage regime, J_G is below ~ 2×10^{-5} A/cm^2 for V_G as negative as –20 V.

current. Fig. 5.10 shows the gate leakage current density J_G as a function of gate voltage V_G of AlGaN/GaN MOS-HEMTs, when both source and drain electrodes were grounded during the measurement. As shown in Fig. 5.10, J_G remains below ~ 2×10^{-5} A/cm^2 for V_G as negative as –20 V. For the positive V_G bias of 0 to 2 V, J_G rises as V_G increases. Mechanism of gate leakage current in the low positive V_G could be due to the trap-assisted tunneling from the 2-DEG channel to the gate, which is related to the traps within AlGaN barrier layer and Al_2O_3 layer [124].



(a)



(b)

Fig. 5.11. (a) I_D-V_G and g_m-V_G characteristics of the AlGaN/GaN-on-sapphire MOS-HEMT (L_G = 2 μm and L_{GS} = L_{GD} = 5 μm). (b) Output (I_D-V_D) characteristics of the AlGaN/GaN-on-sapphire MOS-HEMT, where V_G is varied in steps of 1 V from –3 to 2 V.

Fig. 5.11 (a) shows shows drain current versus gate voltage (I_D-V_G) and extrinsic transconductance versus gate voltage (g_m-V_G) characteristics of the AlGaN/GaN MOS-HEMT with L_G = 2 μm and L_{GS} = L_{GD} = 5 μm. A threshold voltage V_{th} of –2.6 V was extracted using the linear-extrapolation method, which extrapolates the I_D-V_G characteristic measured at V_D = 1 V from the point of maximum slope to the intercept with the gate voltage axis. The sub-threshold swing S and peak transconductance $g_{m,max}$ (V_D = 5 V) are 89 mV/decade and 20.4 mS/mm, respectively. The relatively low $g_{m,max}$ is due to the large gate-to-channel distance (40 nm) and a relatively high parasitic source/drain (S/D) series resistance. The extrinsic transconductance g_m is smaller than the intrinsic transconductance $g_{m,i}$ due to the parasitic S/D series resistance. $g_{m,i}$ can be extracted using

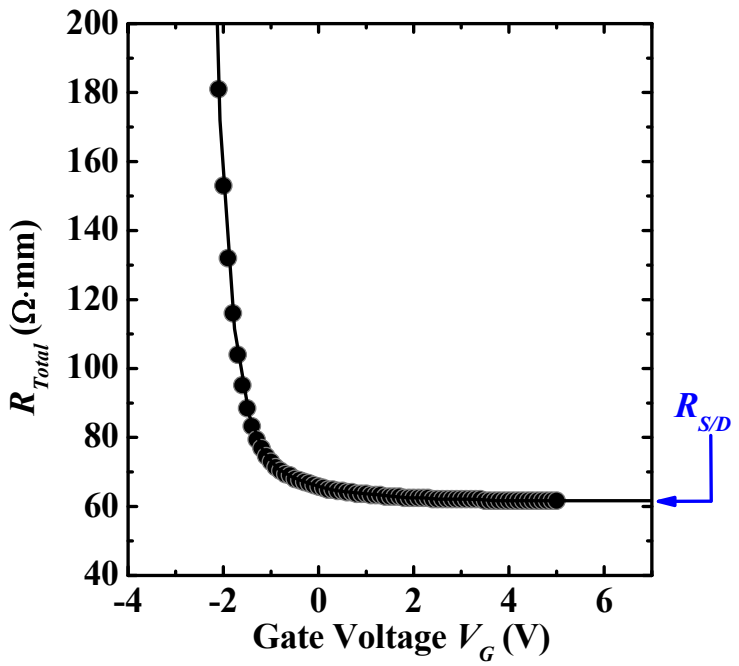


Fig. 5.12. Total resistance R_{Total} as a function of gate voltage V_G when the drain voltage was fixed at 1 V. Parasitic S/D series resistance $R_{S/D}$ for the device in Fig. 5.10 is 62 Ω·mm.

$$g_{m,i} = g_m / (1 - R_S g_m), \quad (5.1)$$

where R_S is the parasitic source resistance [180]. The value of R_S can be estimated as half of the value of the parasitic S/D series resistance $R_{S/D}$, where $R_{S/D}$ is defined as $R_{S/D} = R_{Total} - R_{Channel}$. R_{Total} is the total resistance measured between the source and drain of the device, and $R_{Channel}$ is the channel resistance. For a very large gate overdrive $V_G - V_{\text{th}}$ ($V_G - V_{th} >> V_D$) and a fixed small V_D (1 V), $R_{Channel}$ becomes very small compared to $R_{S/D}$, and $R_{S/D}$ can be estimated from the R_{Total} versus V_G plot. As shown in the Fig. 5.12, the extracted $R_{S/D}$ for the device in Fig. 5.11 is 62 Ω·mm. For $g_{m,max}$ of 20.4 mS/mm and R_S of 31 Ω·mm, the peak intrinsic transconductance $g_{m,i,max}$ is calculated to be 55.5 mS/mm using Equation (5.1).

The output (I_D-V_D) characteristics of the same device in Fig. 5.11 (a) are shown in Fig. 5.11 (b), where good saturation and pinch-off characteristics are observed. The gate voltage V_G was varied in steps of 1 V from –3 to 2 V. An on-state resistance R_{on} of 9 mΩ·cm^2 was calculated from the slope of the I_D-V_D plot in the linear region with the consideration of the device active area between source and drain ohmic contacts.

Fig. 5.13 shows the sub-threshold swing S (left axis) and I_{on}/I_{off} ratio (right axis) as a function of the gate leakage current I_G for the AlGaN/GaN MOS-HEMTs (L_G = 2 μm and $L_{GS} = L_{GD}$ = 5 μm). I_{on} and I_{off} are defined to be the values of I_D measured at $V_G = V_{th}$ + 4 V and V_{th} – 7 V, respectively, at V_D = 5 V. I_G was measured at $V_G = V_{th}$ – 7 V and V_D = 5 V. The devices shown in

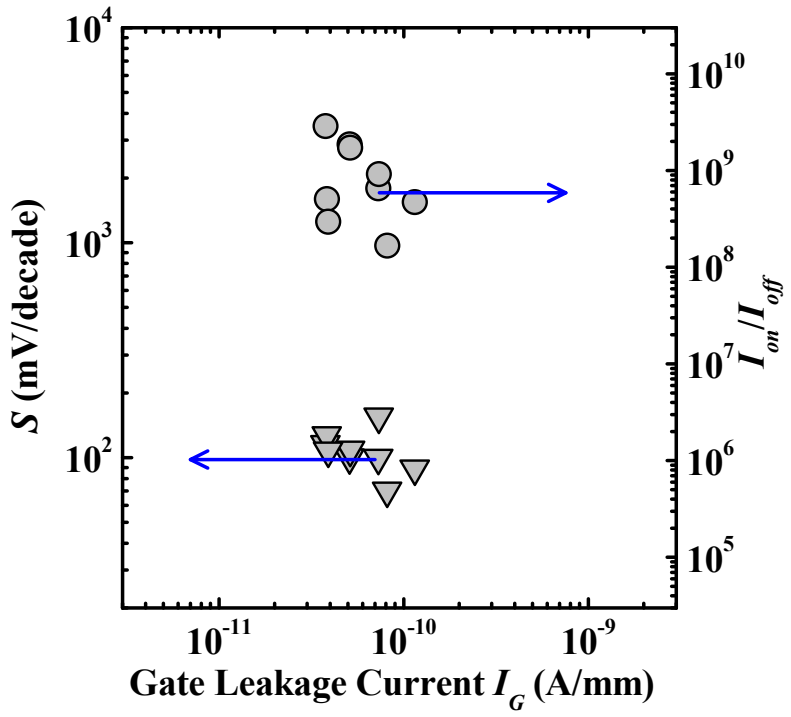


Fig. 5.13. Sub-threshold swing S (left axis) and I_{on}/I_{off} ratio (right axis) as a function of gate leakage current I_G for the AlGaN/GaN MOS-HEMTs (L_G = 2 μm and $L_{GS} = L_{GD}$ = 5 μm).

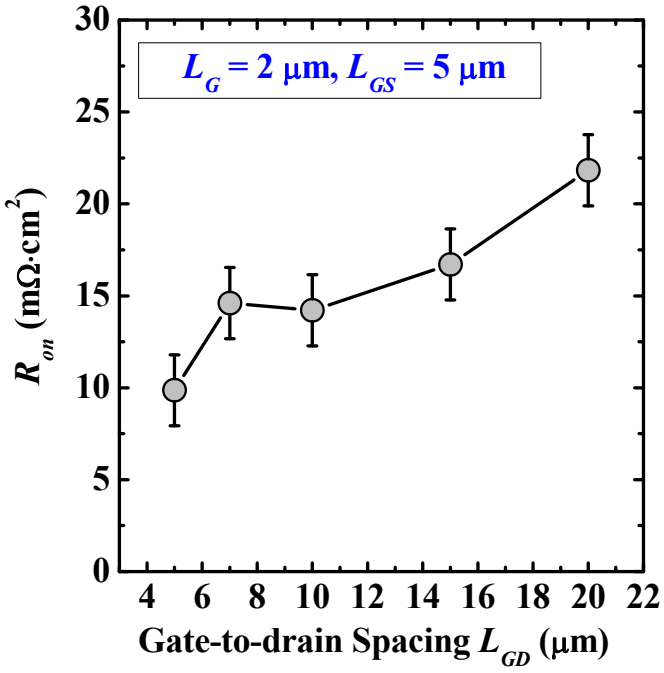


Fig. 5.14. On-state resistance R_{on} of the AlGaN/GaN MOS-HEMTs (L_G = 2 μm and L_{GS} = 5 μm) as a function of the gate-to-drain spacing L_{GD}.

Fig. 5.13 have a mean S of 108.2 mV/decade, a mean I_{on}/I_{off} ratio of 1.1×10^{9}, and a mean I_G of 6.2×10^{-11} A/mm. The device-to-device variation in the I_G, I_{on}/I_{off} ratio, and S is possibly due to the variation in the interface trap density at the Al_2O_3-AlGaN interface [48].

In order to increase the breakdown voltage, devices with a larger value of the gate-to-drain spacing L_{GD} were fabricated. Fig. 5.14 shows the dependence of on-state resistance R_{on} on the gate-to-drain spacing L_{GD}. The gate length L_G of 2 μm and the gate-to-source spacing L_{GS} of 5 μm are fixed, while the gate-to-drain spacing L_{GD} is varied to be 5, 7, 10, 15, and 20 μm. On-state resistance R_{on} increases as the gate-to-drain spacing L_{GD} increases, as a result of the increase in parasitic source/drain series resistance.

A three-terminal off-state breakdown measurement was carried out with Agilent 1505A seminconductor analyzer in Fluorinert ambient to prevent early surface or air breakdown due to the surface flashover. Usually, the surface or air breakdown due to surface flashover is ~ 325 V [114]. During the measurement, the source was grounded with a floating substrate, and the TaN gate was biased at −10 V. A schematic drawing of measurement setup is shown in Fig. 5.15. The source, gate, and drain were connected to ground unit (GNDU), high power (HP) SMU, and high voltage SMU (HVSMU), respectively. Fig. 5.16 shows source current I_S, gate current I_G, and drain current I_D as a function of the drain voltage V_D for a device with L_G = 2 μm, L_{GS} = 5 μm, and L_{GD} = 20 μm. Below V_D = 900 V, the value of gate current I_G is around 1 to 2 orders of magnitude lower than those of drain current I_D and source current I_S. Above V_D = 900 V, gate current I_G reaches almost the same value as drain current I_D, while source current I_S still remains constant.

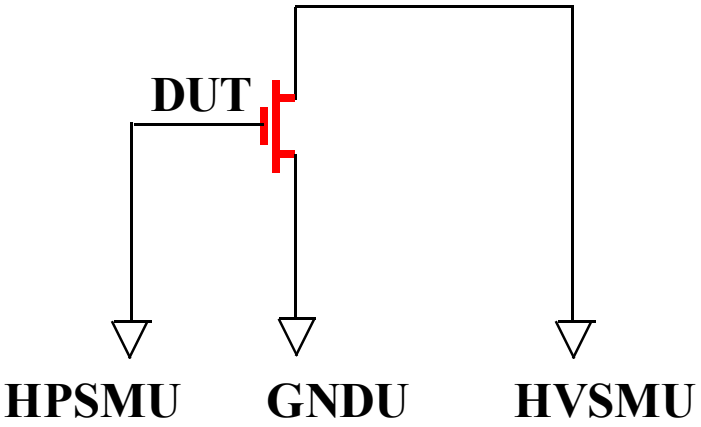


Fig. 5.15 During the high voltage measurement with Agilent B1505A, the gate of the device under test (DUT) was biased below threshold voltage using high power (HP) SMU, source was connected to the ground unit (GNDU), and drain was connect to the high voltage (HV) SMU. The device is kept in the Fluorinert ambient.

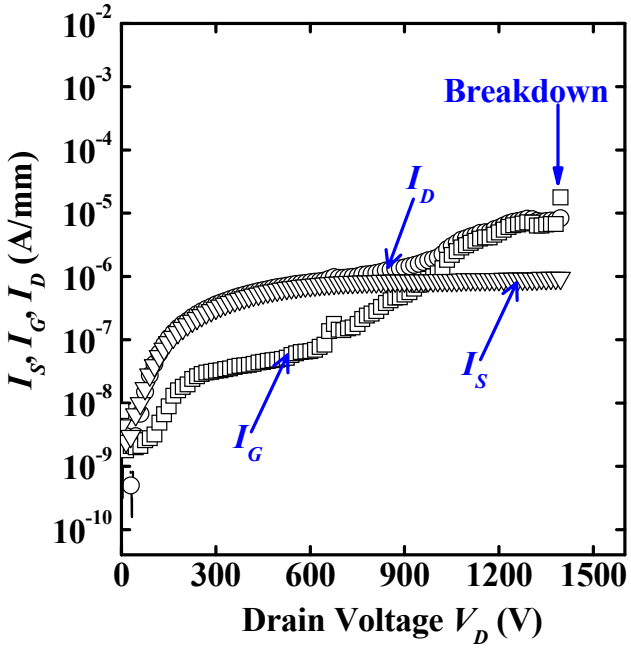


Fig. 5.16. Source current I_S, gate current I_G, and drain current I_D as a function of drain voltage V_D for the high voltage off-state measurement in a Fluorinert ambient of the AlGaN/GaN MOS-HEMT (L_G = 2 μm, L_{GS} = 5 μm, and L_{GD} = 20 μm), where V_S = 0 V and V_G = –10 V. The drain current I_D is below 1 mA/mm when V_D = 1400 V.

Above V_D = 900 V, drain current I_D is dominated by gate current I_G, which indicates that the gate dielectric and the AlGaN barrier layer do not effectively limit the electron transport from the gate to the channel. Drain current I_D remains at ~ 8×10^{-6} A/mm when drain voltage V_D is increased up to 1400 V.

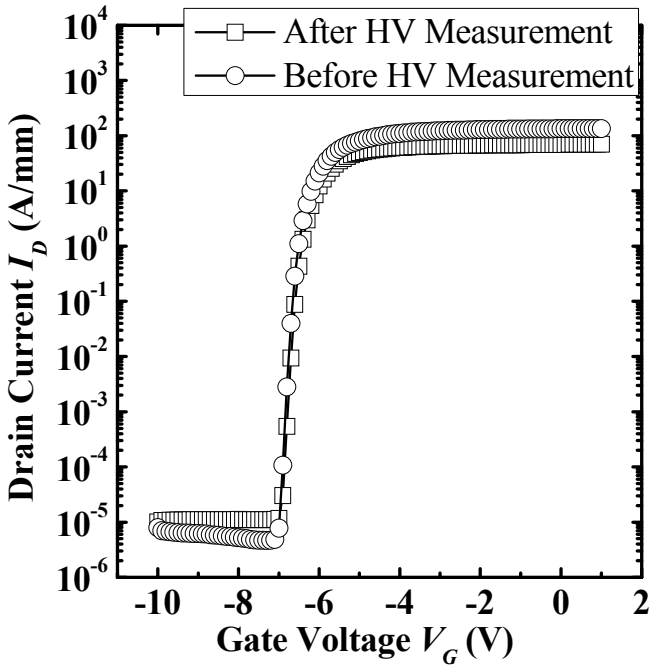
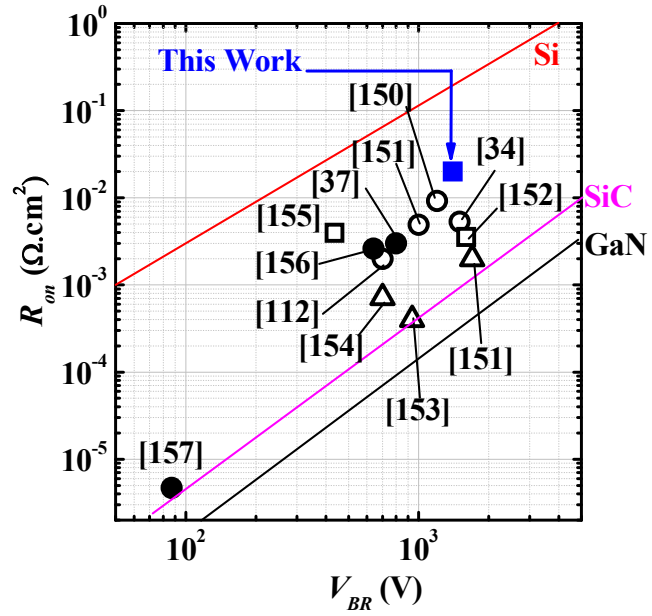


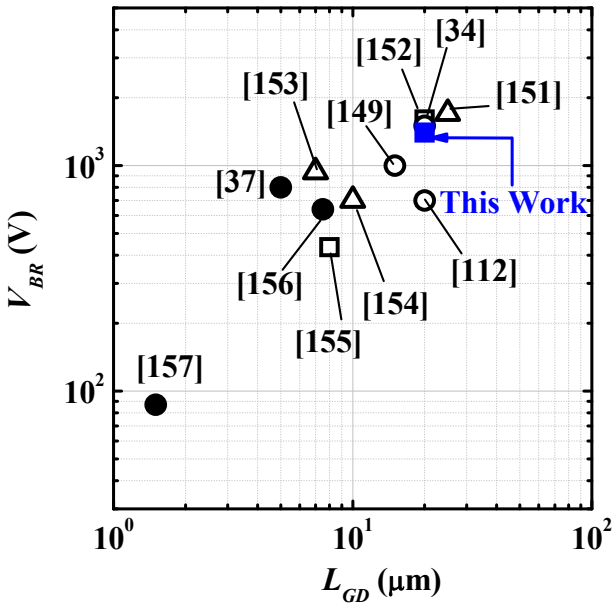
Fig. 5.17 I_D-V_G at V_D = 1 Vcharacteristics of the fabricated AlGaN/GaN MOS-HEMT (L_G = 2 μm, L_{GS} = *5* μm, and L_{GD} = 20 μm) before and after the high voltage (HV) measurement.

The breakdown could be due to the impact ionization at the drain side of the gate edge [181]- [183]. After receiving the wafer from Hong Kong University of Science and Technology, I_D-V_G measurement was done on the device with high voltage (HV) measurement. As shown in Fig. 5.17, the device after high voltage measurement does not show degradation in both off-state and on-state, as compared to that before high voltage measurement."

Fig. 5.18 (a) shows a comparison of breakdown voltage V_{BR} versus on-state resistance R_{on} between this work and other state-of-the-art AlGaN/GaN MOS-HEMTs. Fig. 5.18 (b) shows a comparison of breakdown voltage V_{BR} versus gate-to-drain spacing L_{GD} between this work and other state-of-the-art AlGaN/GaN MOS-HEMTs. A breakdown voltage V_{BR} of 1400 V achieved in this work, to our knowledge, is the highest to date, for AlGaN/GaN MOS-HEMTs fabricated using a gold-free process.



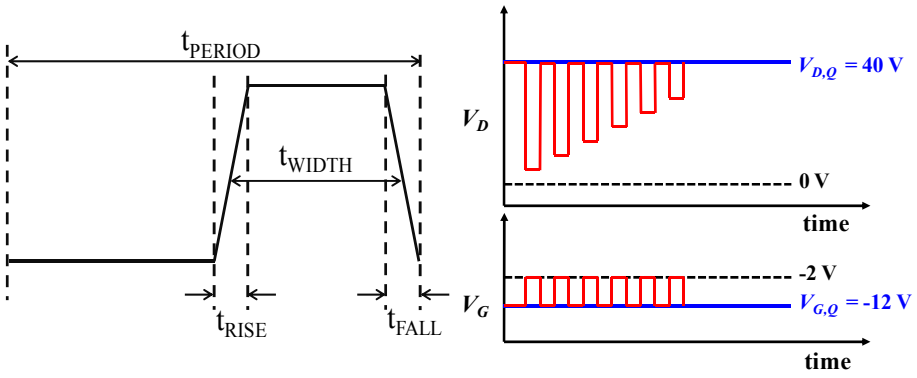
(a)



(b)

Fig. 5.18. (Open symbol: AlGaN/GaN MOS-HEMTs with gold; Solid symbol: AlGaN/GaN MOS-HEMTs without gold; Square: AlGaN/GaN-on-sapphire; Triangle: AlGaN/GaN-on-SiC; Circle: AlGaN/GaN-on-silicon) (a) Breakdown voltage V_{BR} versus on-state resistance R_{on} of the fabricated AlGaN/GaN MOS-HEMTs, as compared with those of state-of-the-art AlGaN/GaN MOS-HEMTs. (b) Breakdown voltage V_{BR} versus gate-to-drain spacing L_{GD} of the fabricated AlGaN/GaN MOS-HEMTs, as compared with those of state-of-the-art AlGaN/GaN MOS-HEMTs. On-state resistance was extracted using the device active area between the ohmic contacts, and large electrode pads were not included here.

High voltage AlGaN/GaN MOS-HEMTs are attractive for high voltage switching devices. The pulse current-voltage (*I*-*V*) measurement was used to evaluate the switching behavior. The pulse used here has a width of 600 ns and a period of 1 ms, where both the rise and fall time is 100 ns. A schematic drawing of the pulse waveform is shown in Fig.5.19 (a). As shown in Fig. 5. 19 (b), the conditions for pulse quiescent bias ($V_{G,Q}$, $V_{D,Q}$) = (–12 V, 40 V), are illustrated when the gate voltage is chosen at –2 V. There is no drain current flow under quiescent bias ($V_{G,Q}$, $V_{D,Q}$) = (–12 V, 40 V), since the channel under the gate was depleted. When the gate was turned off at –12 V under the quiescent bias, the drain was biased at 40 V (the highest voltage that could be applied in our lab). Under this quiescent bias, electrons could be trapped in the buffer or barrier layer. Especially, the trapped electrons with long emission time constant could be trapped for a long time, and would deplete electrons in the channel when the device is turned on, which further increase the channel resistance.



(a) (b)

Fig. 5.19 (a) Schematic drawing of the pulse waveform used in the study. The pulse used here has a width (t_{WIDTH}) of 600 ns and a period (t_{PERIOD}) of 1 ms, where both the rise (t_{RISE}) and fall (t_{FALL}) time is 100 ns. (b) Illustration of pulse quiescent bias ($V_{G,Q}$, $V_{D,Q}$) = (–12 V, 40 V), when the gate voltage was chosen at –2 V (Not-drawn-to-scale here).

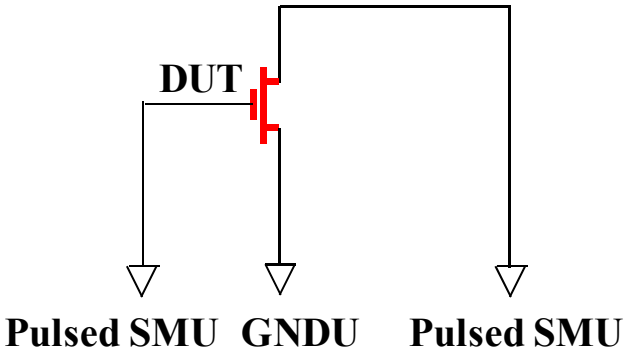


Fig. 5. 20. During the pulse measurement, both gate and drain of the device under test (DUT) were connected to pulsed SMU units, and source was connected to ground unit (GNDU).

As shown in Fig. 5. 20, during the pulse measurement,gate and drain were connected to two separate pulsed SMU units, and source was connected to ground unit (GNDU). The schematic drawing of gate and drain voltage waveform is shown in Fig. 5.19 (b). In Fig. 5.21, two different quiescent bias conditions were used to characterize the device under dynamic current-voltage conditions: ($V_{G,Q}$, $V_{D,Q}$) = (–12 V, 40 V) and ($V_{G,Q}$, $V_{D,Q}$) = (0 V, 0 V). Under

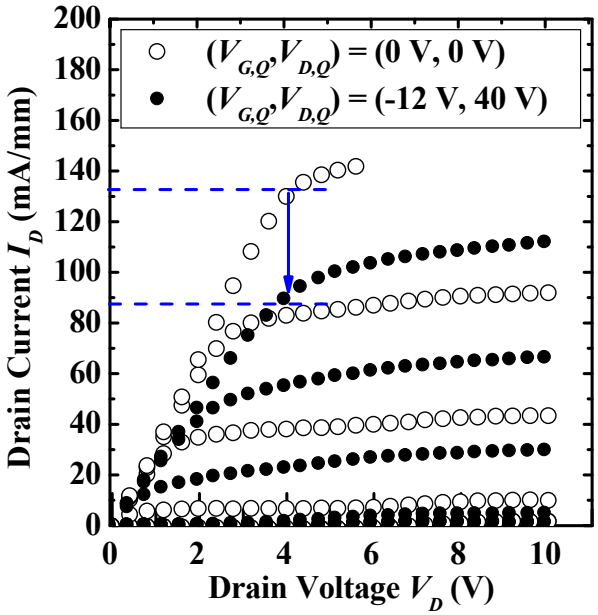


Fig. 5.21 Pulse I-V characteristics of AlGaN/GaN MOS-HEMTs (L_G = 2 μm, L_{GS} = 5 μm, and L_{GD} = 20 μm) under two pulse quiescent bias conditions ($V_{G,Q}$, $V_{D,Q}$) = (0 V, 0 V) and (–12 V, 40 V), where the V_G is varied in steps of 1 V from –2 to –6 V.

quiescent bias ($V_{G,Q}$, $V_{D,Q}$) = (0 V, 0 V), there is no electron trapping, since both gate and drain was biased at 0 V (source was grounded during the measurement). As shown in Fig. 5.21, at V_G = –2 V and V_D = 4 V, the drain current under a quiescent bias ($V_{G,Q}$, $V_{D,Q}$) = (–12 V, 40 V) drops ~ 30 %, as compared to that under a quiescent bias ($V_{G,Q}$, $V_{D,Q}$) = (0 V, 0 V). The reduction of the drain current under quiescent bias ($V_{G,Q}$, $V_{D,Q}$) = (–12 V, 40 V) could be due to trapping of carriers in the barrier or buffer layers [184].

5.4 Summary

In this Chapter, both high voltage AlGaN/GaN-on-silicon and AlGaN/GaN-on-sapphire MOS-HEMTs were realized using a CMOS compatible gold-free process. CMOS compatible ohmic contacts and gate stack were adopted. For AlGaN/GaN-on-silicon MOS-HEMTs, the highest breakdown voltage V_{BR} of 800 V was achieved, as compared with those of gold-free AlGaN/GaN-on-silicon MOS-HEMTs having a gate-to-drain spacing L_{GD} of less than 10 μm reported to date. For AlGaN/GaN-on-sapphire MOSHEMTs, the highest breakdown voltage V_{BR} of 1400 V was obtained, as compared to other gold-free AlGaN/GaN MOS-HEMTs reported to date.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

Over the past three decades, AlGaN/GaN high electron mobility transistor (HEMT) has become a very promising candidate for the next generation high voltage and high power electronic devices, mainly due to the superior material properties of GaN. In particular, growth of GaN-on-silicon wafers with large diameters of 6 inches and 8 inches was demonstrated [29]-[32]. This thesis has sought to explore the application of AlGaN/GaN HEMTs for power devices beyond the silicon-based transistors. Challenges faced by the AlGaN/GaN HEMTs were addressed, and various technology options have been proposed and experimentally realized. To harness the full potential of the AlGaN/GaN HEMTs for power device application, different directions for improving the performance of AlGaN/GaN HEMTs have been explored, such as the surface passivation on GaN or AlGaN surface, strain engineering using a high stress liner, and complementary metal-oxide-semiconductor (CMOS) compatible gold-free fabrication process. The key contributions of this thesis are listed in the next section.

6.2 Contributions of This Thesis

6.2.1 *In Situ* Surface Passivation for High Quality Metal Gate/High-Permittivity Dielectric Stack

Concept and demonstration of *in situ* surface passivation techniques was explored to realize high quality metal gate/high-permittivity dielectric stacks on GaN surface in Chapter 2 [75]-[77]. This passivation technique is highly compatible with a mature high-permittivity dielectric deposition process, and comprises vacuum anneal and surface treatment in a multi-chamber metal-organic chemical vapor deposition (MOCVD) gate cluster system.

6.2.2 *In Situ* Vacuum Anneal and SiH_4 Treatment on AlGaN/GaN MOS-HEMTs

The effect of *in situ* vacuum anneal and SiH_4 treatment on the electrical characteristics of AlGaN/GaN metal-oxide-semiconductor HEMTs (MOS-HEMTs) was investigated in Chpater 3. Devices with *in situ* vacuum anneal and SiH_4 treatment showed reduced gate leakage current and improved saturation drain current. *In situ* vacuum anneal and SiH_4 treatment of the AlGaN surface prior to high-permittivity dielectric deposition enables the realization of AlGaN/GaN MOS-HEMTs with high current on/off, I_{on}/I_{off}, ratio of ~ 10^6, and sub-threshold swing of less 100 mV/decade [78], [185].

6.2.3 Strain Engineering for Performance Enhancement of AlGaN/GaN MOS-HEMTs

In this technology demonstration, a highly compressive diamond-like-carbon (DLC) stress liner was integrated on the AlGaN/GaN MOS-HEMTs for performance enhancement in Chapter 4 [79]-[80]. The DLC high stress liner induced a non-uniform stress along the channel of the AlGaN/GaN MOS-HEMTs. It was found that a compressive stress was induced by the DLC liner in the channel under the gate, thus reducing the polarization charge density and leading to a positive threshold voltage shift, and a tensile stress was induced in the access regions between the gate and the source/drain contacts, thus leading to an increase of the polarization charge density and a reduction of the parasitic source/drain series resistance.

6.2.4 High Voltage AlGaN/GaN MOS-HEMTs with CMOS Compatible Gold-Free Process

Both high voltage AlGaN/GaN-on-silicon and -on-sapphire MOS-HEMTs were realized using a CMOS compatible gold-free process, where CMOS compatible ohmic contacts and gate stack were adopted in Chapter 5 [81]-[83], [183]. CMOS compatible gold-free process is essential for fabricating GaN-based power devices in silicon CMOS foundries without the risk of gold contamination, thus enabling the cost effective fabrication of GaN-based power devices.

6.3 Future Directions

In summary, this thesis conceptualized and realized several exploratory technology options to address several technical challenges of AlGaN/GaN HEMTs, such as novel surface passivation, strain engineering, and development of CMOS compatible gold-free process. Preliminary assessment was performed and the technology options appear to be promising for possible application in GaN-based devices. Several issues related to this work may deserve further investigation. Some of the suggestions for future directions in the field of GaN-based devices are highlighted below.

6.3.1 Other Silicon Passivation Technique

In Chapters 2 and 3, *in situ* surface passivation technique comprising vacuum anneal and SiH_4 treatment in a multi-chamber MOCVD gate cluster system was demonstrated to realize high quality gate stacks on GaN or AlGaN layer. The SiH_4 treatment introduced a layer of silicon, which was subsequently oxidized during the dielectric deposition, and the oxidized silicon layer can serve as a protective layer to prevent the GaN or AlGaN surface from oxidation during the HfAlO deposition. In term of silicon passivation technique, there are other ways of depositing silicon layer on the GaN or AlGaN surface, such as Si_2H_6 surface treatment using a CVD process, which may be further investigated [186]-[187].

6.3.2 Surface Passivation Technique on Other Nitride Material System

AlGaN/GaN heterostructure was used in this thesis work. Materials with even higher polarization charge than that of the AlGaN/GaN

heterostructure, such as InAlN/GaN heterostructure, are very attractive for high power device applications. InAlN/GaN heterostructure has two main advantages over AlGaN/GaN heterostructure: (1) the charge induced by the spontaneous polarization is almost three times higher than that of the AlGaN/GaN heterostructure; (2) $In_{0.17}Al_{0.83}N$ and GaN are lattice matched, so that there is no mechanical constraint in the epitaxial structure. Further work can focus on the development of InAlN/GaN HEMTs [188]-[191].

6.3.3 Strain Engineering Technique

DLC stress liner was explored in Chapter 4 of this thesis for the performance enhancement of AlGaN/GaN MOS-HEMTs, such as threshold voltage adjustment and parasitic source/drain series resistance reduction. However, the thermal stability of the DLC liner may be a concern for the high temperature power devices [192]. The reliability aspects of DLC liner may be investigated. Further work can focus on developing other stress liners with a high thermal stability, such as compressive silicon nitride liner.

6.3.4 Source/Drain Series Resistance Reduction

Although GaN power devices, such as AlGaN/GaN HEMTs, have achieved a lower on-state resistance than that of silicon devices for a given breakdown voltage, they have yet to achieve an on-state resistance value close to the theoretical limit of GaN. The reasons for this could be the high contact resistance and relatively high sheet resistance in the source/drain access regions. Further reduction of parasitic source/drain series resistance is

desirable through source/drain engineering, such as re-growth GaN source/drain [193]-[195].

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Appendix A

Process Flow for Fabricating AlGaN/GaN MOS-HEMTs in This Work

Step	Process	Process Specifications	Equipment
1	**AlGaN/GaN on Al_2O_3 or Si wafer**	2", 3", or 4" wafer provided by NTT-AT.	
2	**Alignment mark definition**		
2.1	PR Patterning		Mask Aligner
2.2	Cl_2-based gas etching	5 sccm He, 20 sccm BCl_3 10 sccm Cl_2, 5 mTorr, 6 ºC, RIE = 200 W, ICP = 500 W, 3 mins.	ICP
2.3	PR Removal	O_2 Gas (30 sccm), 250 W, 170 ºC, 10 mins.	Asher
3	**Mesa definition**		
3.1	PR Patterning		Mask Aligner
3.2	Cl_2-based gas etching	5 sccm He, 20 sccm BCl_3 10 sccm Cl_2, 5 mTorr, 6 ºC, RIE = 200 W, ICP = 500 W, 30 s, depth of 45 nm.	ICP
3.3	PR Removal	30 sccm O_2, 170 ºC, RF = 250 W, 10 mins.	Asher
4	**Pre-gate cleaning**		
4.1	Acetone	2 mins.	Ultrasonic
4.2	Isopropanol	3 mins.	Ultrasonic
4.3	Dilute HCL	$HCl:H_2O$ = 1:1, 10 mins.	Beaker, Wet Bench
4.4	$(NH_4)_2S$ solution	30 mins.	Beaker, Wet Bench
5	***In situ* passivation and HfAlO gate dielectric deposition**		
5.1	Vacuum Anneal	1 minute, 300 ºC, 1×10^{-6} Torr.	MOCVD

5.2	SiH_4 Treatment	60 sccm SiH_4, 250 sccm N_2, 60 s, 400 ºC, 5 Torr.	MOCVD
5.3	High-κ HfAlO Deposition	40 mg/min $HfAl(MMP)_2(OiPr)_5$, 170 sccm Ar, 450 ºC, 400 mTorr.	MOCVD
or 5	**Al_2O_3 gate dielectric deposition**		
5.1	Al_2O_3 Deposition	250 ºC, 25 mTorr, 0.12 nm/cycle.	ALD
6	**Post-Deposition Anneal**		
6.1	Rapid thermal anneal	500 ºC, 30 s.	Rapid Thermal Anneal
7	**TaN Gate deposition**		
7.1	TaN sputtering	DC = 450 W, 3 mTorr, 5 sccm N_2.	Sputter
8	**Gate definition**		
8.1	PR Patterning		Mask Aligner
8.2	TaN etching	200 sccm Cl_2, 10 Torr.	Lam Etcher
8.3	PR Removal	30 sccm O_2, 170 ºC, RF = 250 W, 10 mins.	Asher
9	**PECVD SiO_2 Encapsulation layer**		
9.1	PECVD SiO_2 deposition	30 sccm SiH_4, 400 sccm N_2O, 280 ºC.	PECVD
10	**Ohmic contact hole opening**		
10.1	PR Patterning		Mask Aligner
10.2	DHF wet etching	HF:H_2O=1:100.	Beaker, Wet Bench
11	**Contact patterning and Al/Ti deposition**		
11.1	PR Patterning		Mask Aligner
11.2	DHF wet etching	HF:H_2O=1:100.	Beaker, Wet Bench
11.3	Al/Ti deposition	Al (71 nm) / Ti (30 nm), 1×10^{-6} Torr.	E-beam Evaporator
11.4	Lift-off process	Acetone	Beaker, Wet Bench
12	**Contact formation anneal**		
12.1	Rapid thermal anneal	1500 sccm N_2, 30 s, 650 ºC.	Rapid Thermal Anneal

Appendix B

Silvaco TCAD Code Used for AlGaN/GaN MOS-HEMTs with *in situ* VA and SiH_4 Passivation

```
GO atlas simflag="-V 5.16.3.R"
MESH auto width=1000
set thickness=0.007
# x plane meshing
x.m l=0    s=0.2
x.m l=0.5  s=0.1
x.m l=1    s=0.1
x.m l=13.  s=0.1
x.m l=14   s=0.2
# y plane meshing
y.m l=-0.02   s=0.05
y.m l=-0.0075 s=0.005
y.m l=-0.007  s=0.00025
y.m l=-0.0035 s=0.002
y.m l=0.0     s=0.00025
y.m l=0.0125  s=0.005
y.m l=0.02    s=0.0001
y.m l=0.0275  s=0.001
y.m l=0.03    s=0.001
y.m l=0.05    s=0.01
y.m l=0.1     s=0.1
y.m l=0.2     s=0.2
y.m l=0.5     s=0.5
y.m l=1       s=0.2
y.m l=2       s=0.2
y.m l=2.9995  s=0.2
y.m l=3       s=0.00025
y.m l=3.0005  s=1
y.m l=4       s=1
ELIMINATE columns x.min=0 x.max=14 y.min=0.1
#########################################################################
# R e g i o n  D e f i n i t i o n s
#########################################################################
REGION num=1 x.min=0 x.max=14 y.min=0 y.max=0.02 mat=AlGaN x.comp=0.25
donor=1e15
REGION num=2 x.min=0 x.max=14 y.min=-0.02 y.max=0 mat=SiO2 insulator
REGION num=3 x.min=0 x.max=14 y.min=-$thickness y.max=0 material=HfO2
REGION num=4 x.min=0 x.max=14 y.min=0.02 y.max=1 mat=GaN donors=1e15
REGION num=5 x.min=0 x.max=14 y.min=1 y.max=3 mat=GaN acceptor=3E17
REGION num=6 x.min=0 x.max=14 y.min=3 y.max=4 mat=sapphire insulator
ELEC num=1 name=source x.min=0 x.max=1 y.min=-0.02 y.max=0.03
ELEC num=2 name=drain x.min=13 x.max=14 y.min=-0.02 y.max=0.03
ELEC num=3 name=gate x.min=6 x.max=8 y.min=-0.02 y.max=-$thickness
ELEC num=4 substrate
#########################################################################
# P o l a r i z a t i o n  C h a r g e s  D e f i n i t i o n
#########################################################################
INTERFACE charge=1.04008E13 y.min=0.02 y.max=0.0205 s.s
```

```
INTERFACE charge=-2.57861E13 y.min=0 y.max=0.0005 s.i
INTERFACE charge=1.53853E13 y.min=2.9995 y.max=3 s.i
#########################################################################
# T r a p  C h a r g e s  D e f i n i t i o n
#########################################################################
intTRAP donor e.level=3.54 density=2.96e13 degen=1 sign=1e-15 sigp=1e-15
y.min=-0.0005 y.max=0.01 s.i
#intTRAP acceptor e.level=2.91 density=6e12 degen=1 sign=1e-15 sigp=1e-15
y.min=-0.0005 y.max=0.01 s.i
#########################################################################
# O u t p u t  a n d  O t h e r  P a r a m e t e r s
#########################################################################
MATERIAL mat=AlGaN align=0.75 Eg300=3.91
#MATERIAL mat=GaN VSATN=4E8 BETAN=1
#MATERIAL mat=AlGaN VSATN=2E7 BETAN=2
MATERIAL mat=SiO2 affinity=1.0
MATERIAL mat=HfO2 Eg300=6.4 Permittivity=19 affinity=2.1
#user.group=insulator user.default=oxide Eg300=6.4 Permittivity=19 affinity=2
MODELS PRPMOB albrct fermi print srh hei fnord fnholes nearflg joule.heat
TRAP.TUNNEL f.ae=1e-7 f.be=1.78e7
MOBILITY albrct.n an.albrct=3e-3 bn.albrct=3e-4 cn.albrct=1.95e-2 vsatn=3e7
CONTACT name=gate workfunction=4.8
OUTPUT con.band val.band charge band.par qss e.mobility
METHOD trap autonr newton maxtrap=100 tol.relax=100
MOBILITY GANSAT.N
#########################################################################
# O u t p u t  S t r u c t u r e
#########################################################################
SOLVE
SAVE outf=IS_85Pol_Pass_mob.str
#TONYPLOT IS.str
quit
#########################################################################
#######
# G a t e  L A G  S i m u l a t i o n
#########################################################################
#######
solve init
solve vgate=0
solve vdrain=0
Log outfile=Ramp_Vd.log
solve vdrain=0 vfinal=5 vstep=0.05 name=drain
log off
Log outfile=Ramp_Vg.log
solve vgate=0 vfinal=0 vstep=0.05 name=gate
log off
tonyplot Ramp_Vd.log Ramp_Vg.log
LOG outf=IdVg_Vd5_85Pol_Pass3.log
solve vgate=0 vfinal=-10 vstep=-0.05 name=gate
SAVE outf=IdVg_Vd5_85Pol_Pass3.str
log off
tonyplot IdVg_Vd5_85Pol_Pass3.log
quit
```

Appendix C

Taurus Abaqus Code Used for Stress Simulation

```
TaurusProcess
# 1/2 gate length
Define (Lg = 400nm)
Define (sp = 500nm)
# Define the initial simulation domain and the initial grid. Also
DefineDevice
(
        xSize = expr(($Lg)+ $sp)
        ySize = 0.5um
        #zSize = 0.5um
        AmbientHeight = 1um
        RefinementsFile = refinements_data
)
# Add a set of regrid parameters to the current list of refinements.
Physics(
        Material=diamond
        YoungsModulus=760e+9
        PoissonRatio=0.20
)
#Change Property of Si to GaN
Physics(
Material=Silicon
C11= 3.9e+11
C12= 1.45e+11
C44= 1.05e+11
)
#Change Property of Ge to AlGaN
Physics(
Material=Germanium
YoungsModulus=3.97e11
)
Refinements(
        Regrid(
                MeshSpacing = 0.3um
                MergeRegionsOfMaterial = oxide
                MergeRegionsOfMaterial = diamond
                CriticalFeatureSize = 0.1nm
                ThinLayer = 1nm
                Criterion(
                AllInterfaces
                MeshSpacing = 5nm
                )
        )
        Regrid(
        MeshSpacing = 0.003um
        MinX = expr(($sp)-0.1) MaxX = expr(($Lg)+ ($sp))
        MinY = 0um MaxY = 0.01um
        )
        Regrid(
```

```
        MeshSpacing = 0.005um
        MinX = 0.2 MaxX = expr(($Lg)+ ($sp))
        MinY = 0um MaxY = 0.2um
        )
)
# Enable automatic stress history simulation during process flow.
Physics(
        KeepStressHistory
        Material = silicon
        Anisotropic = true
        Bandgap (StressInducedBGNActive = true)
)
Physics
(
        Material=Silicon
        Equation=Germanium
        Diffusion(
                StrainFactor(
                StrainDependency = true
                StrainCoefficient = 40.0)
                )
        Equation=Boron
        Diffusion(
                StrainFactor(
                StrainDependency=true
                StrainCoefficient= -17.0)
                )
)
# Modify the linear solver and associated solution parameters.
Numerics(
        Linearsolver = direct
        NewtonResid = 1e-10
)
Numerics (ImbalanceLimit = 10.0)
Numerics(
Iterations=20
maxDivergenceCount=10
)
Deposit(
        Material = Germanium
        Thickness = 0.02um
)
Deposit(
        Material = oxide
        Thickness = 0.01um
)
Deposit(
        Material = nitride
        Thickness = 0.1um
)
Etch
(
        Thickness = 0.5um
        EtchType = dry
        MaskPolygon
```

```
        (
        Point(x=0.2um z=-0.3um)
        Point(x=expr(($Lg)+ ($sp)) z=-0.3um)
        Point(x=expr(($Lg)+ ($sp)) z= 0.3um)
        Point(x=0.2um z= 0.3um)
        )
)
Deposit
(
Layer(
        Material = oxide
        thickness = 5nm
        Onto(Material = silicon)
)
)
#Save(MeshFile = SiGe_50nm_01.tdf)
Deposit
(
        Material = teos
        SurfacePosition = -0.02um
)
Etch
(
        Material = nitride
        EtchType = all
)
#Save(MeshFile = SiGe_50nm_02.tdf)
Etch
(
        Material = oxide
        Thickness = 150A
        EtchType = dry
)
Save(MeshFile = SiGe_50nm_03.tdf)
# Create the gate oxide and the gate layer.
Deposit
(
        Material = hafniumoxide
        thickness = 7nm
)
Deposit
(
        Material = Tantalum
        Thickness = 0.1um
)
#Save(MeshFile = SiGe_50nm_04.tdf)
# Define the gate.
Etch
(
        Material = Tantalum
        EtchType = dry
        MaskPolygon
        (
                Point(z=-1um x=expr($sp))
                Point(z=-1um x=expr(($Lg)+ ($sp)))
```

```
                Point(z= 1um x=expr(($Lg)+ ($sp)))
                Point(z= 1um x=expr((($sp))))
        )
)
#deposit DLC
define(a=0)
while ($a<8)
{
define(a=expr($a+1))
Deposit (
        AllowMerge = false
#       Region = stressor
        Material=nitride
        Thickness=5nm
        IntrinsicStress = -5900.0MPa
        )
}
ReflectMesh(
Right
)
Save (MeshFile="SiGe_50nm_11_400nm.tdf")
Save (MeshFile="SiGe_50nm_11_400nm.tree")
Extract(

        only(

                Name = stressXX
        )
        ExtractFile = gan400.dat
)

        Sample = values
)
#Save (MeshFile="SiGe_50nm_10.tdf")
#Save (TreeFile="SiGe_50nm_10.tree")
Stop()
```

Appendix D

Sentaurus TCAD Code Used for DLC-Strained AlGaN/GaN MOS-HEMTs

```
;-----------------------------------------------------------------------;
; vertical dimensions
(define hAlN      0.100)
(define hGaN      2.000)
(define hAlGaN    0.020)
(define hPass     0.050)
(define hDielectric         0.007)

; horizontal dimensions
(define Xmin     -5.650)
(define SrcLngth  5.000)
(define DrnLngth  5.000)
(define GtLngth   0.300)
(define SrcSep    0.500)
(define DrnSep    0.500)
; Ohmic contact definitions
(define Sep       0.00)
(define Dpng      1E20)
; Molefraction definition
(define x_AlGaN  0.25)
;-----------------------------------------------------------------------;
; Derived quantities
;-----------------------------------------------------------------------;
(define Xmax    (+ Xmin SrcLngth SrcSep GtLngth DrnSep DrnLngth))
(define Ymax    (+ hGaN))
(define Ymin    (- 0 hAlGaN hPass))
(define Ysrfc   (- 0 hAlGaN))
(define Yjnctn  (- 0 Sep))

(define Xsrc    (+ Xmin SrcLngth))
(define XgtLft  (+ Xsrc SrcSep))
(define XgtRght (+ XgtLft GtLngth))
(define Xdrn    (+ XgtRght DrnSep))
;-----------------------------------------------------------------------;
; Create structure
;-----------------------------------------------------------------------;
(sdegeo:create-rectangle (position Xsrc Ymin 0)  (position XgtLft (- Ysrfc hDielectric)
0) "Nitride" "LeftPassivation" )
(sdegeo:create-rectangle (position Xsrc (- Ysrfc hDielectric) 0)  (position Xdrn Ysrfc
0) "Al2O3" "Dielectric")
(sdegeo:create-rectangle (position XgtRght Ymin 0)  (position Xdrn (- Ysrfc
hDielectric) 0) "Nitride" "RightPassivation" )
(sdegeo:create-rectangle (position Xmin Ysrfc 0)  (position Xmax 0 0) "AlGaN"
"AlGaN_barrier" )
(sdegeo:create-rectangle (position Xmin 0 0)  (position Xmax Ymax 0) "GaN"
"GaN_bulk" )
; -------------------------------------------------------------------------
; Place AlGaN mole fraction
; -------------------------------------------------------------------------
```

```
(sdedr:define-constant-profile "CP.xMole" "xMoleFraction" x_AlGaN)
(sdedr:define-constant-profile-material "CP.xMole" "CP.xMole" "AlGaN" 0
"Replace")
; ---------------------------------------------------------------------------
; Place doping profiles to emulate metal spikes
; ---------------------------------------------------------------------------
(sdedr:define-refinement-window "Pl.Source" "Rectangle" (position Xmin Ysrfc 0)
(position Xsrc Yjnctn 0))
(sdedr:define-constant-profile "P.source" "PhosphorusActiveConcentration" Dpng)
(sdedr:define-constant-profile-placement "P.source" "P.source" "Pl.Source")

(sdedr:define-refinement-window "Pl.Drain" "Rectangle" (position Xdrn Ysrfc 0)
(position Xmax Yjnctn 0))
(sdedr:define-constant-profile "P.drain" "PhosphorusActiveConcentration" Dpng)
(sdedr:define-constant-profile-placement "P.drain" "P.drain" "Pl.Drain")

; ---------------------------------------------------------------------------
; Create and place all electrodes
; ---------------------------------------------------------------------------
(sdegeo:define-contact-set "source")
(sdegeo:set-current-contact-set "source")
(sdegeo:set-contact-edges (find-edge-id (position (+ Xmin 0.001) Ysrfc 0)))

(sdegeo:define-contact-set "gate")
(sdegeo:set-current-contact-set "gate")
(sdegeo:set-contact-edges (find-edge-id (position (+ XgtLft 0.001) (- Ysrfc
hDielectric) 0)))
(sdegeo:set-contact-edges (find-edge-id (position (* 0.5 (+ XgtLft XgtRght)) (- Ysrfc
hDielectric) 0)))
(sdegeo:set-contact-edges (find-edge-id (position (- XgtRght 0.001) (- Ysrfc
hDielectric) 0)))

(sdegeo:define-contact-set "drain")
(sdegeo:set-current-contact-set "drain")
(sdegeo:set-contact-edges (find-edge-id (position (+ Xdrn 0.001) Ysrfc 0)))

;---------------------------------------------------------------------------
; Grid refinement definitions
; ---------------------------------------------------------------------------
(sdedr:define-refinement-window "Pl.Default" "Rectangle" (position Xmin Ymin 0)
(position Xmax Ymax 0))
(sdedr:define-refinement-size "Ref.Default" 0.4 0.2 99 0.01 0.005 66 )
(sdedr:define-refinement-placement "Ref.Default" "Ref.Default" "Pl.Default" )
(sdedr:define-refinement-function "Ref.Default" "DopingConcentration"
"MaxTransDiff" 1)

(sdedr:define-refinement-window "Pl.eDensity" "Rectangle"
  (position (- XgtRght 0.05) Ymin 0)
  (position (+ XgtRght 0.3)   0.1 0))
(sdedr:define-refinement-size "Ref.eDensity" 0.005 99 99 0.005 66 66 )
(sdedr:define-refinement-placement "Ref.eDensity" "Ref.eDensity" "Pl.eDensity" )

(sdedr:define-refinement-window "Pl.channel_h" "Rectangle"
  (position (- XgtLft 0.1) Ymin 0)
  (position (+ XgtRght 1)   0.1 0))
```

```
(sdedr:define-refinement-size "Ref.channel_h" 0.1 99 99 0.001 66 66 )
(sdedr:define-refinement-placement "Ref.channel_h" "Ref.channel_h"
"Pl.channel_h" )

(sdedr:define-refinement-window "Pl.drain_c" "Rectangle"
  (position (- XgtRght 0.2) Ymin 0)
  (position (+ XgtRght 0.7)   0  0))
(sdedr:define-refinement-size "Ref.drain_c" 0.04 99 99 0.005 66 66 )
(sdedr:define-refinement-placement "Ref.drain_c" "Ref.drain_c" "Pl.drain_c" )

(sdedr:define-refinement-window "Pl.contact_r" "Rectangle"
  (position (- XgtRght 0.005) Ymin 0)
  (position (+ XgtRght 0.05)   0.1 0))
(sdedr:define-refinement-size "Ref.contact_r" 0.005 99 99 0.001 66 66 )
(sdedr:define-refinement-placement "Ref.contact_r" "Ref.contact_r" "Pl.contact_r" )

(sdedr:define-refinement-window "Pl.contact_l" "Rectangle"
   (position (- XgtLft 0.005) Ymin 0)
   (position (+ XgtLft 0.005) 0.1  0))
(sdedr:define-refinement-size "Ref.contact_l" 0.005 99 99 0.001 66 66 )
(sdedr:define-refinement-placement "Ref.contact_l" "Ref.contact_l" "Pl.contact_l" )

(sdedr:define-refinement-window "Pl.surface" "Rectangle"
  (position Xmin Ysrfc 0)
  (position Xmax 0 0))
(sdedr:define-multibox-size "MB.surface" 99 0.05 99 66 0.001 66 1 2 1 )
(sdedr:define-multibox-placement "MB.surface" "MB.surface" "Pl.surface" )

(sdedr:define-multibox-size "MB.barrier" 99 0.05 99 66 0.0004 66 1 -2 1 )
(sdedr:define-multibox-placement "MB.barrier" "MB.barrier" "Pl.surface" )

(sdedr:define-refinement-window "Pl.surface_Pol" "Rectangle"  (position Xmin Ysrfc
0) (position Xmax (+ Ysrfc 0.0001) 0))
(sdedr:define-multibox-size "MB.surface_Pol" 99 0.05 99 66 0.0002 66 1 4 1 )
(sdedr:define-multibox-placement "MB.surface_Pol" "MB.surface_Pol"
"Pl.surface_Pol" )

(sdedr:define-refinement-window "Pl.channel" "Rectangle"
  (position Xmin    0 0)
  (position Xmax hGaN 0))
(sdedr:define-multibox-size "MB.channel" 99 0.1 99 66 0.0004 66 1 1.5 1 )
(sdedr:define-multibox-placement "MB.channel" "MB.channel" "Pl.channel" )

(sdeaxisaligned:set-parameters "yCuts"
   (list -0.025 -0.0249 -5e-5 0 5e-5)
)
;--- Generate and save the mesh using Mesh
(sde:build-mesh "snmesh" "" "n2_dielec")
Electrode {
          { Name="gate"   Voltage= 0 Workfunction = 4.4 }
          { Name="source" Voltage= 0 Resist = 100 }
          { Name="drain"  Voltage= 0 Resist = 100 }
}
File {
          * Input files
```

```
        Grid= "n2_dielec_msh.tdr"
        Parameter= "pp4_des.par"
        * Output filesDLC_IdVd
        Current= "n4_des.plt"
        Plot= "n4_des.tdr"
        Output= "n4_des.log"
}
Physics {
        Mobility(
                Enormal(Lombardi)
                DopingDependence
                eHighfieldsaturation
        )
        EffectiveIntrinsicDensity (Nobandgapnarrowing)
        Fermi
        Recombination(SRH)
        RecGenHeat
        Aniso(Poisson)
        Thermionic
}
Physics (Material="GaN") {
        Traps (
                (Acceptor Level Conc= 5e17 EnergyMid= 1.0 EnergySig= 0
FromMidBandGap
                 eXSection= 1e-15 hXSection= 1e-15)
        )
}
Physics (Material="AlGaN") {
        Traps (
                (Acceptor Level Conc= 5e17 EnergyMid= 1.0 EnergySig= 0
FromMidBandGap
                 eXSection= 1e-15 hXSection= 1e-15)
        )
}
Physics (MaterialInterface="AlGaN/GaN") {
        Charge(
                (Uniform Conc=1.38211e13)
Physics (MaterialInterface="AlGaN/Hf2O3") {
        Charge((Uniform Conc=-3.13841e13)
           )
Traps (
                (Donor Level Conc= 3.0e13 EnergyMid= 0.2 FromMidBandGap)
        )}
Plot {
        Potential Electricfield/Vector
        eDensity hDensity
        eCurrent/Vector hCurrent/Vector
        TotalCurrent/Vector
        SRH Auger Avalanche
        eMobility hMobility
        eQuasiFermi hQuasiFermi
        eGradQuasiFermi hGradQuasiFermi
        eEparallel hEparallel
        eMobility hMobility
        eVelocity hVelocity
```

```
        DonorConcentration Acceptorconcentration
        Doping SpaceCharge
        ConductionBand ValenceBand
        BandGap Affinity
        xMoleFraction
        eTemperature hTemperature
        eTrappedCharge hTrappedCharge
        eInterfaceTrappedCharge hInterfaceTrappedCharge
        }
Math {
        Extrapolate
        Iterations= 16
        Digits= 6
        ErrRef(electron) = 1E5
        ErrRef(hole) = 1E3
        RHSmin= 1e-10
        RHSmax= 1e30
        CDensityMin= 1e-20
        DirectCurrentComputation
        RelTermMinDensity= 1e5
        eMobilityAveraging= ElementEdge
}
Solve {
Coupled (Iterations= 100000 LinesearchDamping= 0.001) {Poisson}
Coupled (Iterations= 100) {Poisson Electron Hole}
*****************************************************************
* Zero bias plot
*****************************************************************
Plot(FilePrefix="300nm_NS_n4_Zero_Bias")
*****************************************************************
* IdVd curve with Vg=0 V
*****************************************************************
NewCurrentFile="300nm_NS_IdVd_Vg0_"
Quasistationary (
InitialStep= 5e-3 Minstep= 1e-7 MaxStep= 0.05 Increment= 1.55
Goal {Name="drain" Voltage= 10}
) {
Coupled {Poisson Electron Hole}
}
Plot(FilePrefix="300nm_NS_Vg0_Vd10")
*****************************************************************
* IdVg curve with Vd=0.5 V
*****************************************************************
*NewCurrentFile="NS_IdVg_Vd10_"
*Quasistationary (
* InitialStep= 0.025 Minstep= 1e-7 MaxStep= 0.05 Increment= 1.5
* Goal {Name="gate" Voltage= -5}
*) {
* Coupled {Poisson Electron Hole}
*}
*
*Plot(FilePrefix="NS_Vg-5_Vd10")
}
```

Appendix E

First Author Publications Arising from This Thesis Research

[1] **X. Liu**, H.-C. Chin, L. S. Tan, and Y.-C. Yeo, "High-permittivity dielectric stack on gallium nitride formed by silane surface passivation and metal-organic chemical vapor deposition," *IEEE Electron Device Lett*., vol. 31, no. 1, pp. 8-10, 2010.

[2] **X. Liu**, H.-C. Chin, L. S. Tan, and Y.-C. Yeo, "*In situ* surface passivation of gallium nitride for metal-organic chemical vapor deposition of high-permittivity gate dielectric," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 95-102, 2011.

[3] **X. Liu**, B. Liu, E. K. F. Low, W. Liu, M. Yang, L. S. Tan, K. L. Teo, and Y.-C. Yeo, "Local stress induced by diamond-like carbon liner in AlGaN/GaN MOS-HEMTs and impact on electrical characteristics," *Appl*. *Phys*. *Lett*., vol. 98, 183502, 2011.

[4] **X. Liu**, E. K. F. Low, J.-S. Pan, W. Liu, K. L. Teo, L. S. Tan, and Y.-C. Yeo, "Impact of *in situ* vacuum anneal and SiH_4 treatment on electrical characteristics of AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors," *Appl*. *Phys*. *Lett*., vol. 99, 093504, 2011.

[5] **X. Liu**, C. Zhan, K. W. Chan, W. Liu, L. S. Tan, K. J. Chen, and Y.-C. Yeo, "AlGaN/GaN-on-silicon MOS-HEMTs with breakdown voltage of 800 V and on-state resistance of 3 $m\Omega \cdot cm^2$ using a CMOS-compatible gold-free process," *Appl*. *Phys*. *Express*, vol. 5, 066501, 2012.

[6] **X. Liu**, C. Zhan, K. W. Chan, M. H. S. Owen, W. Liu, D. Z. Chi, L. S. Tan, K. J. Chen, and Y.-C. Yeo, "AlGaN/GaN metal-oxide-

semiconductor high-electron-mobility transistors with a high breakdown voltage of 1400 V and a CMOS-compatible gold-free process," *Jpn. J. Appl. Phys.*, vol. 52, no. 4, 04CF06, 2013.

[7] **X. Liu**, H.-C. Chin, L. S. Tan, and Y.-C. Yeo, "Metal-gate/high-permittivity dielectric stack on gallium nitride formed by silane surface passivation and metal-organic chemical vapor deposition," *Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials*, Sendai, Japan, pp. 1214-1215, 2009.

[8] **X. Liu**, H.-C. Chin, E. K. F. Low, W. Liu, L. S. Tan, and Y.-C. Yeo, "*In situ* silane surface passivation for gate-first undoped AlGaN/GaN HEMTs with minimum current collapse and high-permittivity dielectric," *Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials*, Tokyo, Japan, pp. 141-142, 2010.

[9] **X. Liu**, B. Liu, E. K. F. Low, H.-C. Chin, W. Liu, M. Yang, L. S. Tan, and Y.-C. Yeo, "Diamond-like carbon (DLC) liner with high compressive stress formed on AlGaN/GaN MOS-HEMTs with in situ silane surface passivation for performance enhancement," in *IEDM Tech. Dig.*, San Francisco CA, pp. 261-264. 2010.

[10] **X. Liu**, C. Zhan, K. W. Chan, W. Liu, L. S. Tan, K. L. Teo, K. J. Chen, and Y.-C. Yeo, "AlGaN/GaN-on-silicon MOS-HEMTs with breakdown voltage of 800 V and on-state resistance of 3 $m\Omega \cdot cm^2$ using a CMOS-compatible gold-free process," *International Symposium on VLSI Technology, Systems and Applications* (*VLSI-TSA*), Hsinchu, Taiwan, 2012.

[11] **X. Liu**, C. Zhan, K. W. Chan, W. Liu, D. Z. Chi, L. S. Tan, K. J. Chen, and Y.-C. Yeo, "AlGaN/GaN-on-sapphire MOS-HEMTs with breakdown voltage of 1400 V and on-state resistance of 22 $m\Omega \cdot cm^2$ using a CMOS-compatible gold-free process," *International Conference on Solid-State Devices and Materials*, Kyoto, Japan, pp. 879-880, 2012.

Other Publications

[12] H.-C. Chin, M. Zhu, **X. Liu**, H.-K. Lee, L. Shi, L. S. Tan, and Y.-C. Yeo, "Silane-ammonia surface passivation for gallium arsenide surface-channel n-MOSFETs," *IEEE Electron Device Lett*., vol. 30, no. 2, pp. 110-112, 2009.

[13] H.-C. Chin, X. Gong, **X. Liu**, and Y.-C. Yeo, "Lattice mismatched $In_{0.4}Ga_{0.6}As$ source/drain stressors with *in situ* doping for strained $In_{0.53}Ga_{0.47}As$ channel n-MOSFETs," *IEEE Electron Device Lett*., vol. 30, no. 8, pp. 805-807, 2009.

[14] H.-C. Chin, **X. Liu**, X. Gong, and Y.-C. Yeo, "Silane and ammonia surface passivation technology for high mobility $In_{0.53}Ga_{0.47}As$ MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 5, pp. 973-979, 2010.

[15] H.-C. Chin, M. Zhu, Z.-C. Lee, **X. Liu**, K.-M. Tan, H. K. Lee, L. Shi, L.-J. Tang, C.-H. Tung, L. S. Tan, and Y.-C. Yeo, "A new silane-ammonia surface passivation technology for realizing inversion-type surface-channel GaAs n-MOSFET with 160 nm gate length and high-

quality metal-gate/high-*k* dielectric stack," in *IEDM Tech*. *Dig*., San Francisco CA, pp. 383-386, 2008.

[16] H.-C. Chin, Z. Lin, **X. Liu**, L. S. Tan, and Y.-C. Yeo, "Inversion-type surface channel $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistors with metal-gate/high-*k* dielectric stack and CMOS-compatible PdGe contacts," *International Symposium on VLSI Technology, Systems and Applications* (*VLSI-TSA*), Hsinchu, Taiwan, pp. 143-144, 2009.

[17] H.-C. Chin, X. Gong, **X. Liu**, Z. Lin, and Y.-C. Yeo, "Strained $In_{0.53}Ga_{0.47}As$ n-MOSFETs: Performance boost with in-situ doped lattice-mismatched source/drain stressors and interface engineering," *Symp. on VLSI Tech. 2009*, Kyoto, Japan, pp. 244-245, 2009.

[18] S. S. Pannirselvam, **X. Liu**, Y.-C. Yeo, and L. S. Tan, "Effects of *in situ* surface passivation of AlGaN/GaN MOS-HEMT: A simulation study," *International Conference on Solid-State Devices and Materials*, Kyoto, Japan, 2012.