SEMICONDUCTOR NANOWIRES FOR THERMOELECTRIC APPLICATIONS

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Declaration

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Li Yida

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Summary

This thesis aims to develop a complete semiconductor nanowire (NW) based thermoelectric device (TED), and to benchmark it with current bulk materials-based TEDs. First of all, by using finite element analysis (FEA) simulation, the effects of key material parameters – NW's length, thermal conductivity, electrical contact resistance, and filler material, on the thermoelectric cooling (TEC) performance were elucidated. Accordingly, a design guideline was proposed for the implementation of a complete silicon (Si) NW-based TEC.

Following, by using complementary-metal-oxide-semiconductor (CMOS) process which is prevalent in the semiconductor industry, SiNW and silicon-germanium (SiGe) NW were successfully integrated into a complete TED. Two filler materials – Si dioxide (SiO_2) and polyimide for the NW array were explored during the TED's fabrication. The SiO_2 filled TED generated a maximum thermoelectric power of 1.5nW with open circuit voltage (V_{oc}) of 1.5V under 70K across experimental setup. This represented the first complete SiNW-based TED to be demonstrated, from fabrication to characterization. Characterizing the polyimide filled TED, it was found that its incorporation enhanced the maximum thermoelectric power output > 2 orders to 1.3μW with V_{oc} of 17.9mV at the same testing condition as the SiO_2 filled TED. With various process optimizations, our

polyimide filled TED achieved a power output density (17kW/m^3) compared to a bismuth-based TED (18.1kW/m^3). As a TEC, the maximum temperature depression was measured to be 0.1K due to the existence of large electrical contact resistance between the SiNW and aluminum metallization. Concurrently, individual SiNW was extracted from the fabricated TED, and characterized for its thermal conductivity using a micro-electrothermal system (METS) device. The results exhibited a commendable SiNW thermal conductivity value (4.1W/mK) comparable to that reported in notable literature.

In a NW-based TED, the formation of good ohmic contacts from the top metal traces to the NW array is a key to device performance. For free standing-SiGe NWs, it was found that attempts at silicidation with nickel (Ni) metallization gave rise to voids. Hence, the growth mechanism of Ni-germanosilicide in SiGe NW was thoroughly investigated using real time transmission electron microscope with *in-situ* annealing. Annealing at temperatures 200^{o}C and 400^{o}C, the growth of Ni-germanosilicide was minimal. On the other hand, during annealing at 600^{o}C, loss of material with time in the SiGe NW was observed. However, it was found that by incorporating a compressive stress (constraining the boundary of the SiGe NW with a SiO_2 shell), the loss of material and void can be effectively suppressed.

Hence, in this thesis, we successfully demonstrated the integration of Si/SiGe NW in a complete TED using CMOS process, and characterized its thermoelectric performance. With proper filler material and contact process optimizations, the thermoelectric performance of the SiNW-based TED improved

significantly. In SiGe NW, we discovered a way to suppress the void formation which is critical to improve the electrical performance of the TED. Our fabrication and characterization methodologies provide a platform in which future works of a NW-based TED can be built on.

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List of Symbols

1-D	One-dimensional
BARC	Bottom anti reflection coating
BOX	Bottom oxide
CLT	Central limit theorem
CMOS	Complementary metal oxide semiconductor
COP	Coefficient of performance
CVD	Chemical vapor deposition
DOS	Density of states
DRIE	Dry reactive ion etching
DUV	Deep ultraviolet
EBL	Electron beam lithography
EDX	Energy dispersive x-ray spectroscopy
FEA	Finite element analysis
IMD	Implantable medical device
IR	Infra-red
LPCVD	Low pressure chemical vapor deposition

MC	Monte carlo
MD	Molecular dynamics
METS	Micro-electrothermal system
PCB	Printed circuit board
PID	Proportional-integral-derivative
RTD	Resistance temperature detector
SiNW	Silicon nanowire
SiGe NW	Silicon-germanium nanowire
SEM	Scanning electron microscope
SOI	Silicon-on-insulator
TCR	Temperature coefficient of resistance
TED	Thermoelectric device
TEC	Thermoelectric cooler
TEG	Thermoelectric power generator
TEM	Transmission electron microscope
TIM	Thermal interface material
VLS	Vapor liquid solid

Chapter 1: Introduction

The thermoelectric phenomenon has been an active area of research since the discovery of the Seebeck and Peltier effects in the 1800s. This phenomenon was first explained by Seebeck where an electrical voltage is generated in a conducting material that is subjected to a temperature gradient. 12 years later, Peltier discovered that a temperature change occurs at the vicinity of a junction between dissimilar conductors when a current is passed. Subsequently, from the development of thermodynamics, Lord Kelvin established a relationship between both effects and predicted a third thermoelectric effect known as the Thomson effect [1.1]. This effect relates to the heating/cooling in a homogeneous conductor when a current is passed in the presence of a temperature gradient.

A thermoelectric material is characterized by a figure of merit $ZT = \frac{S^2\sigma}{\kappa}T$, where S, σ, and κ represent the Seebeck coefficient, electrical conductivity, and thermal conductivity respectively. A good thermoelectric material should possess a high Seebeck coefficient and electrical conductivity to reduce ohmic losses while having a low thermal conductivity to prevent unwanted heat flow between the two junctions. In the early days, researchers focused on metal/metal alloys and found that most of them possess a Seebeck coefficient less than 10μV/K. This resulted in an efficiency of a fraction of 1%. It was only in the 1930s when semiconductors were found to be much better thermoelectric materials with Seebeck coefficients >100μV/K. In addition, the electrical conductivity can be

controlled with doping which results in a much larger *ZT* value, and hence the focus shifted to semiconductors thereafter.

A modern TED design is made up of alternating n- and p- type semiconductors which are connected electrically in series and thermally in parallel as shown in Figure 1.1. Such a design improves the thermoelectric effect greatly as opposed to using solely n- or p- type thermoelectric legs [1.2].

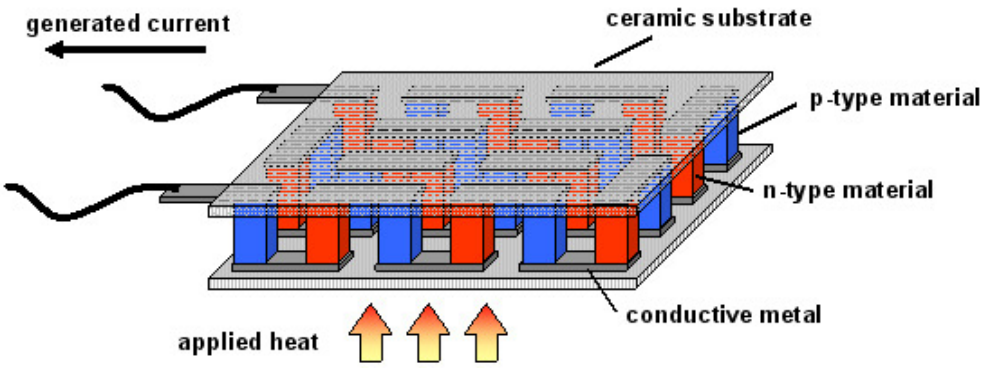

Figure 1.1: Alternating n- and p- type thermoelectric legs in a device (HIS GlobalSpec CR4, 2013)

Established thermoelectric materials used in a TED are generally grouped into three categories depending upon their operating range of temperature. They are namely Bismuth telluride and its alloys, lead telluride and its alloy, and silicon germanium alloy. Bismuth telluride alloys are extensively used in refrigeration with a maximum operating temperature of ~450K while Lead telluride and silicon germanium are commonly used for power generation with an operating temperature >1000K. A comparison of the thermoelectric efficiencies as a function of *ZT* and operating temperature are compared to several heat engines in Figure 1.2.

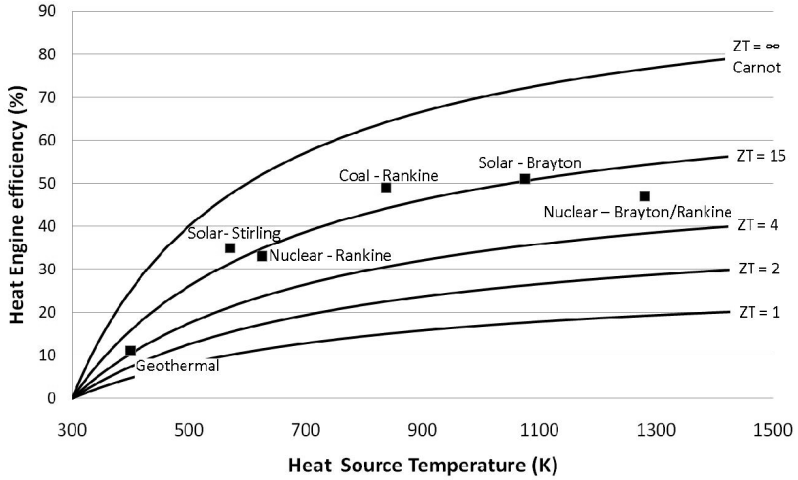

Figure 1.2: Relation of *ZT* with the efficiency of heat engine [1.3]

It can be seen that in order for TED to contend with large scale power production technology, a *ZT* in excess of 4 is needed. However, commercial bismuth telluride and its alloys based TED have a *ZT* of ~1. Hence, more efficient materials are needed before a TED it can compete at the same level [1.3].

In the early 1990s, low dimensional (D) materials – 2-D quantum well, 1-D quantum wire/nanowire (NW), and 0-D quantum dot were theoretically predicted to have enhanced *ZT* as compared to their bulk counterpart due to the quantum confinement effect [1.4-1.5]. However, experimental work on such systems was limited by technology at that time. The availability of new methods for nanostructure synthesis, complemented with the use of powerful analysis tools such as scanning electron microscope (SEM) and transmission electron microscope, resulted in a spate of studies involving such class of nanostructures [1.6-1.8].

1-D nanoscale NW with its unusual mechanical, optical, electrical, and thermal properties holds potential in the area of thermoelectrics. Depending on its size at the nanoscale, the thermal conductivity of NW is modified greatly from its bulk counterpart [1.8]. The thermal conductance suppression is primarily due to two reasons. Firstly, there is increased phonon boundary scattering as the diameter reduces to the order of the phonon mean free path in the bulk material (tens to hundreds of nm) [1.7]. Secondly, the size confinement of a NW modifies the phonon frequency *versus* wave-vector dispersion relation from that of the bulk material [1.9]. This will lead to the discovery of much more efficient thermoelectric materials. Complementary-metal-oxide-semiconductor (CMOS) compatible semiconductor NW such as silicon (Si), silicon-germanium (SiGe) alloy, germanium (Ge) etc., are particularly attractive due to the availability of established processing technology for large scale fabrication. This is supplemented by two highly interesting works on SiNW which reported tremendous improvement in the *ZT* value of two orders of magnitude as compared to bulk Si [1.10-1.11].

The promise of NW as an efficient thermoelectric material makes it a potential replacement for commercially used bismuth telluride and its alloys. Two interesting areas of implementations are on-chip cooling or miniaturize power source. Due to aggressive transistor scaling, the emergence of hot spots (typical size – 400μm x 400μm) on a microprocessor chip becomes prevalent, and brings about the need to dissipate it so as to retain performance [1.2]. SiNW being able

to scale to appropriate size and target hot spots directly is much more efficient compared to conventional fan cooling [1.12].

Furthermore, a NW-based TED can be possibly used to provide a continuous and uninterrupted source of power for miniaturized devices, for example, as a wearable electronics such as watches, and implantable medical devices (IMDs). Low powered wearable watch and IMD such as a cardiac pacemaker typically requires a power supply in the region of tens to hundreds of μW [1.13-1.14]. It was experimentally measured that power harvested from body heat can exceed 80μW/cm^2 [1.13]. Hence, a SiNW-based TED which is efficient enough to harvest sufficient power (tens of μW) from body heat could be a potential candidate for low powered devices.

The potentials of Si/SiGe NW as a thermoelectric material, and how it can be applied in real applications deserve further investigation. Hence, this thesis aims to develop a fabrication method to assemble Si/SiGe NW into a complete TED, as well as to evaluate the suitability of the Si/SiGe NW-based TED in practical power generation and cooling applications. This thesis is organized as follows. In Chapter 2, the concepts of thermoelectricity are introduced, focusing on the underlying physics of 1-D NW. In addition, the development of micro scale TEDs is presented. In Chapter 3, we present the potential of SiNW as a TEC through finite element analysis (FEA) simulation. The impact of key material parameters in the performance was investigated, followed by a design guideline for a complete SiNW-based TEC. In Chapter 4, we fully describe the fabrication steps of a Si/SiGe NW-based TED using CMOS process; this includes the

problems encountered and the mitigating solutions. Following, Chapter 5 discusses the characterization methodology of the fabricated SiNW-based TED. This includes the thermal measurement of individual SiNW using a home-made micro-electrothermal system (METS) device, as well as power generation/cooling measurements at the device level. Chapter 6 on the other hand, focuses on the characterization of a SiGe NW-based TED, and the investigation of the growth mechanism of nickel-germanosilicide in SiGe NW. Finally in Chapter 7, the thesis will be concluded with proposed future works that can be carried out to further understand and optimize the Si/SiGe NW-based TED's performance for future implementation.

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Chapter 2: Concepts and Development of Thermoelectricity in One-Dimensional Nanowire

In this chapter, the concepts of thermoelectricity and its relevance in one-dimensional (1-D) nanostructures, in particular, silicon (Si), silicon-germanium (Ge), and germanium (Ge) nanowire (NW) will be presented. The thermoelectric parameters that characterize a thermoelectric device (TED) will first be discussed, followed by the thermoelectric transport (electronic and thermal), and engineering efforts of a thermoelectric material. In addition, the developments of Si/SiGe/Ge NW in reported theoretical and experimental works will be reviewed. The discussion on theoretical efforts includes the prediction and optimization of the thermoelectric properties via modeling and simulations. On the other hand, the discussion on experimental works will focus on the methods of synthesizing Si/SiGe/Ge NW, the measurement technique, and the results. Lastly, the development of micro/nano scale TED will be touched on.

2.1 Thermoelectric efficiency

The performance of a thermoelectric material is universally recognized to be dependent on a special parameter known as the figure of merit Z given in Equation 2.1 [2.1].

$$Z = \frac{S^2\sigma}{\kappa} \quad \text{--- (2.1)}$$

where S, σ, and κ refer to the Seebeck coefficient, electrical conductivity, and thermal conductivity, respectively. A thermoelectric material has the ability to transport heat (refrigeration), or to generate a potential difference across its two ends (power generation), depending on the type of input energy supplied (thermal or electrical). In refrigeration mode, the coefficient of performance (COP) is the characterizing parameter while in power generation mode, the conversion efficiency (η) is of interest; both the COP and η and are related to Z. The following discussion on the COP and η will be made on a thermocouple – two alternately doped n- and p- type thermoelectric legs connected electrically in series and thermally in parallel (Figure 2.1). It is worth pointing out that the number of thermoelectric legs will not affect the overall efficiency of the device; it only affects the amount of useful work output. In the following analysis, temperature independent thermoelectric parameters are used.

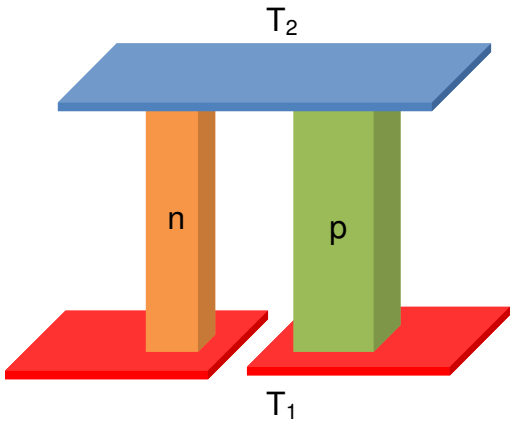

Figure 2.1: A thermocouple with n- and p- type thermoelectric legs connected in series

2.1.1 Coefficient of Performance (COP)

COP determines the cooling efficiency of conventional refrigeration as well as a thermoelectric cooler (TEC) [2.2-2.6]. The COP of a refrigerator is defined as the ratio of the maximum heat (Q) that can be removed and the input power (W) supplied to the device as:

$$COP = \frac{Q}{W} \text{ --- (2.2)}$$

A simple illustration of the COP: if 1 W of power is required to be removed by a TEC with a COP of 0.5, 2 W of input power is needed; this translates to a total of 3 W of heat to be removed. From a mathematical perspective, considering the thermocouple illustrated in Figure 2.1, the total amount of power W supplied to the n- and p- type thermoelectric legs with input current I is given by:

$$W_{total} = W_n + W_p = \left(S_p - S_n\right)I(T_2 - T_1) + I^2R \text{--- (2.3)}$$

where the subscript refers to the doping type and R refers to the total electrical resistance of the thermocouple. Given the amount of heat that can be removed from the cold side:

$$Q = \left(S_p - S_n\right)IT_1 - \frac{1}{2}I^2R - K(T_2 - T_1) \text{ --- (2.4)}$$

the COP as a function of Z is derived as:

$$COP = \frac{Q}{W} = \frac{(S_p - S_n)IT_1 - \frac{1}{2}I^2R - K(T_2 - T_1)}{(S_p - S_n)I(T_2 - T_1) + I^2R} \text{ --- (2.5)}$$

by taking the derivative of COP with respect to I and setting it to zero, the maximum COP can be expressed as a function of Z:

$$COP_{max} = \frac{T_1\left[(1+ZT_m)^{1/2} - T_2/T_1\right]}{(T_2 - T_1)\left[(1+ZT_m)^{1/2} + 1\right]} \text{ --- (2.6)}$$

where $T_m = (T_1 + T_2)/2$ is the mean temperature of the two ends. It can be seen that apart from the temperature difference at the two ends, the Z value is a main determinant of the COP.

2.1.2 Thermoelectric conversion efficiency (η)

The thermoelectric conversion efficiency η of a material is related to the product of the Carnot efficiency and Z [2.7]. Mathematically, η is defined as:

$$\eta = \frac{\text{Useful work done}}{\text{Total input energy}} \text{ --- (2.7)}$$

To further illustrate, let us consider a load of resistance R_L connected across the thermocouple in Figure 2.1. In the presence of a temperature gradient ($\Delta T = T_2 - T_1$), a potential difference is generated by the thermocouple and results in a total useful work W generated across R_L:

$$W = \left[\frac{(S_p - S_n)(T_2 - T_1)}{(R_L + R)}\right]^2 R_L \text{--- (2.8)}$$

In supplying heat by the source, most of the heat is conducted to the sink through the thermocouple and some is used to balance the Peltier effect associated with the flow of current. According to Peltier's equation, half of the Joule heat from the thermoelectric legs will travel all the way to the source. With the inclusion of all the mentioned terms, q is expressed as:

$$q = K(T_2 - T_1) + \left(S_p - S_n\right)IT_2 - \frac{I^2R}{2} \text{ --- (2.9)}$$

where q is the heat removed and $I = \frac{(S_p - S_n)(T_2 - T_1)}{(R_L + R)}$. The maximum η is obtained when $R_L = R$ (matched load condition). However, even with the condition of R_L satisfied, the maximum η achievable will never exceed 50% of the ideal thermodynamic efficiency $\eta_{max} = \frac{(T_2 - T_1)}{T_2}$ [2.1]. As analyzed by Ioffe [2.1], the ratio of R_L and R (represented by M) as a function of Z, has an optimum value given by:

$$M = \frac{R_L}{R}(optimum) = (1 + ZT_M)^{1/2} \text{ --- (2.10)}$$

$$\eta = \frac{(T_2 - T_1)}{T_2} \cdot \frac{M - 1}{M + \frac{T_2}{T_1}} \text{ --- (2.11)}$$

It can be seen from Equation 2.11 that the ideal thermodynamic efficiency is degraded by the second term. When $ZT << 1$, Equation 2.11 reduces to

$$\eta \rightarrow \frac{(T_2 - T_1)}{T_2} \cdot \frac{ZT_M}{2(1 + \frac{T_2}{T_1})}$$

where the ideal thermodynamic efficiency is multiplied by a value that is much less than unity. On the other hand when $ZT >> 1$,

$$\eta \rightarrow \frac{(T_2 - T_1)}{T_2}$$

where the ideal thermodynamic efficiency is achieved. It can be thus seen that apart from the hot and cold side temperature, Z is again the crucial parameter for thermoelectric power generation. Common thermoelectric materials bismuth telluride (BiTe) yields a best ZT value of ~1 which translates to a η of ~20% (Equation 2.11). The analysis of the thermoelectric refrigeration and generation shows the significance of the parameter Z on the performance of a TED. As Z is a function of the material's electrical and thermal properties, the understanding of the carriers transport process is useful for further work.

2.2 Thermoelectric transport in one-dimensional nanostructures

A good thermoelectric material is effectively a phonon glass and an electron crystal [2.8]. It means that it should possess a thermal conductivity as low as possible while maintaining good electronic properties. This is to achieve a high Seebeck coefficient and electrical conductivity. The choice of thermoelectric materials in the early days was metals and metal alloys, and the thermoelectric properties of such materials are limited by the Widemann-Franz-Lorenz law where κ/σ is a constant. Hence, semiconductor as thermoelectric materials is a much preferred choice where κ and σ can be decoupled through engineering [2.1].

In the early 1990s, the theoretical work on 1-D nanostructures for thermoelectrics by Hicks and Dresselhaus brought about renewed research interest [2.9]. In their work, the *ZT* enhancement is attributed to the quantum confinement of electrons and phonons (carriers of charge and thermal energy respectively) in their transport mechanisms. In addition, when the size of a material becomes comparable to the mean free path of the carriers, classical interface scattering effects will emerge and greatly modify the thermal transport properties.

2.2.1 Electronics properties

In a solid-state TED, the Boltzmann equation is a popular method to express the electronic properties considering the carrier transport process occurring much slower than that of the relaxation process. The derivation of the *S* and σ is not straightforward, but can be expressed with a modification to the Boltzmann equation in the form of integrals over the electron energy in Equations 2.12 to 2.14 [2.10]:

$$\sigma \equiv \int \sigma(E) \left(\frac{\partial f_{eq}}{\partial E}\right) dE \text{ --- (2.12)}$$

$$\sigma(E) \equiv q^2 \tau(E) \iint {v_x}^2 \left(E, k_y, k_z\right) dk_y dk_z \cong q^2 \tau(E) \bar{v}_x{}^2 (E) D(E) \text{ --- (2.13)}$$

$$S = \lim_{E \to E_f} \frac{\pi^2}{3} \frac{{k_b}^2 T}{q} \frac{d \ln[\sigma(E)]}{dE} \propto \left(E - E_f\right) \text{ --- (2.14)}$$

where the variables used are $E_f(r)$ – Fermi energy, $v(k)$ – carrier velocity, $\tau(k)$ – the momentum-dependent relaxation time, k_b – Boltzmann constant (1.38×10^{-23} m^2 kg $s^{-2}K^{-1}$), $D(E)$ – density of states at energy E, and $\sigma(E)$ –contribution of electrons with energy E to the total conductivity

In the simplified expression, there is an assumption that the local deviation from the equilibrium is small. In order to achieve the best thermoelectric properties, $\sigma(E)$ near the Fermi window should be as large as possible to enhance σ, and as asymmetric as possible with respect to the Fermi energy to enhance the S as illustrated in Figure 2.2 [2.10].

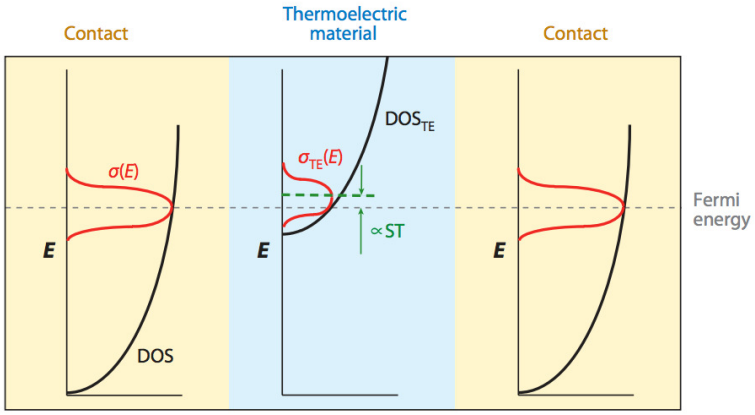

Figure 2.2: Density of states (DOS) and differential conductivity $\sigma(E)$ *versus* electron energy (E) for a thermoelectric material and the contact layers. [2.10]

A high S and σ values are always desired, but there is always a trade off in the course of maximizing these two values as explained using the concept of differential conductivity as presented by Shakouri [2.10]. When the Fermi energy is close to the band edge, the DOS is asymmetric with respect to the Fermi level. In an n- type material, more states are available for transport above the Fermi energy. If the doping concentration of the material increases, the Fermi energy will start to move deeper in the band and the differential conductivity will become more symmetric to the Fermi energy. Hence, the increased of σ value will result in a reduction in the S value of the material. Shakouri further explained the trade-off between S and σ using fundamental relations between the electronic DOS and the

electron group velocity in crystals; a crystal with high electron effective mass and multiple valleys have a large DOS but lower mobility. The shape of the DOS dominates the overall performance, and thus materials with a heavy electron effective mass and multiple valleys have the potential as a good thermoelectric material.

The nature of the DOS holds the key to improving the Seebeck coefficient and in 1-D NW, the shape of the DOS is different from a 3-D bulk material [2.10]. For a particle travelling in a 1-D direction, the DOS as a function of energy $D(\varepsilon)$ is expressed in equation 2.15

$$D(\varepsilon) = \frac{2n_{1D}(k)}{\frac{dE}{dk}} = \frac{\frac{(2)(2)L}{2\pi}}{\left(\frac{\hbar^2 k}{m}\right)} = \frac{1}{\pi\hbar}\sqrt{\frac{2m}{\varepsilon}} \text{ --- (2.15)}$$

and the general form of a 1-D NW DOS is just a summation of Equation 2.15 as

$$D(\varepsilon) = \sum_j D_j(\varepsilon) \text{ --- (2.16)}$$

$$D_j(\varepsilon) = \frac{dN_j}{dk}\frac{dk}{d\varepsilon} = (2)(2)\frac{L}{2\pi}\left[\frac{m}{2\hbar^2(\varepsilon-\varepsilon_j)}\right]^{1/2} \text{ --- (2.17)}$$

where ε_j refers to the energy at different states. The DOS of a 1-D system and 3-D system is shown in Figure 2.3 for comparison.

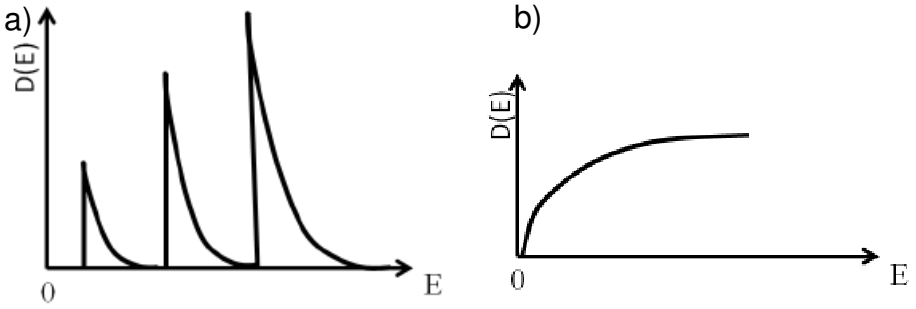

Figure 2.3: DOS of a) 1-D system, and b) 3-D system

We can easily note sharp features present in the electronic DOS at all ε_j due to the square root dependency. This effectively improves the *S* of 1-D materials as compared to its 3-D counterpart. In a 1-D material, *S* can be enhanced by tuning the Fermi level of the material to be near the bottom of a subband where the DOS is high [2.9] and thus is a theoretically more superior thermoelectric material compared to its 3-D counterpart.

2.2.2 Thermal properties

The heat conduction property of a material depends on both the electrons and phonons, with the latter known as the lattice contribution. In metals and degenerately doped small band-gap semiconductors, the dominant thermal carriers are the electrons while for lightly to heavily doped semiconductor and insulators, phonons are the main contributor. According to the theory of thermal transport, phonon is the quantum unit of energy of a lattice vibration, which is analogous to the photon of an electromagnetic wave [2.11]. In a lattice crystal,

although phonon itself is not a physical entity, the general idea of its transport is the same as that of charge carrying electrons and holes.

The thermal conductivity of a solid is defined by the expression $j_v = -K\frac{dT}{dx}$, where j_v is the flux of energy transmitted across unit area per unit time [11]. The presence of the differential form of temperature gradient per unit length rather than just the temperature difference ΔT between two ends of a solid reveals that the energy transfer is a random process via scattering mechanism [2.11]. Charles gave a very good description in the derivation of thermal conductivity of a crystal using elementary kinetic theory which will be briefly presented [2.11]. The derivation begins with the flux of particles *f* in the *x* direction as

$$f = \frac{1}{2}n\langle|v_x|\rangle \text{ --- (2.18)}$$

where n is the concentration of particles and $\langle|v_x|\rangle$ the average velocity of the particles. As a particle travel between two locations having a temperature difference of ΔT, a finite amount of energy $c\Delta T$ is given up, where c is the heat capacity of the particle. The temperature difference ΔT can be expressed in the form

$$\Delta T = \frac{dT}{dx}l_x = \frac{dT}{dx}v_x\tau \text{ --- (2.19)}$$

where τ is the mean free time between collisions of the particles. The corresponding net flux of energy is then expressed as

$$j_v = -n\langle {v_x}^2\rangle c\tau \frac{dT}{dx} = -\frac{1}{3}n\langle v^2\rangle c\tau \frac{dT}{dx} \text{ --- (2.20)}$$

where $\frac{1}{3}$ is to account the movement of the particle in one direction only. Assuming that the particle's velocity is constant, Equation 2.20 can be written as

$$j_v = -\frac{1}{3}n\langle v^2\rangle c\tau \frac{dT}{dx} = -\frac{1}{3}Cvl\frac{dT}{dx} \text{ --- (2.21)}$$

where $l=v\tau$ is the mean free path of the phonons and $C=nc$ is the specific heat capacity of the crystal lattice. Finally, the thermal conductivity is extracted as

$$K = \frac{1}{3}Cvl \text{ --- (2.22)}$$

The key parameter *C* in Equation 2.22 is defined as the change in internal energy with respect to temperature $\frac{\partial U}{\partial T}$. The contribution of the phonons to the heat capacity of a crystal is known as the lattice heat capacity and their total energy *U* is the sum of the energies over all phonon modes as a function of the wave vectors and polarization index. Using the Planck distribution, the total energy *U* in Equation 2.23 is differentiated w.r.t to obtain the lattice heat capacity in Equation 2.24:

$$U = \sum_p \int d\omega D_p(\omega) \frac{\hbar\omega}{\exp\left(\frac{\hbar\omega}{\tau}\right)-1} \text{ --- (2.23)}$$

$$C = k_B \sum_p \int d\omega D_p(\omega) \frac{x^2 \exp x}{(\exp x - 1)^2} \text{ --- (2.24)}$$

In order to evaluate C, the DOS, or the number of modes per unit frequency is needed. The DOS can be evaluated analytically or obtained experimentally from the measurements of the phonons dispersion curve (with wavevector) in a desired direction using inelastic neutron scattering followed by analytical fitting. Analytically, such an evaluation is non-trivial but there are two popular models, namely the Debye model and the Einstein model.

In the Debye model, the velocity of sound is approximated to be constant for each polarization type and the famous Debye heat capacity C_D is given as

$$C_D = \frac{3V\hbar^2}{2\pi^2 v^3 k_B T^2} \int_0^{\omega_D} d\omega \frac{\omega^4 e^{\hbar\omega/\tau}}{\left(e^{\hbar\omega/\tau} - 1\right)^2} \text{ --- (2.25)}$$

where ω_D is the Debye cut off frequency. The Debye temperature T_D as a function of ω_D is given by

$$T_D = \frac{\hbar v}{k_B} \cdot \left(\frac{6\pi^2 N}{V}\right)^{1/3} \text{ --- (2.26)}$$

where N is the number of primitive cells in the crystal. As the temperature becomes much larger than T_D, the heat capacity will approach the classical value of $3Nk_B$. A plot of the Debye heat capacity with respect to the Debye temperature is as shown in Figure 2.4.

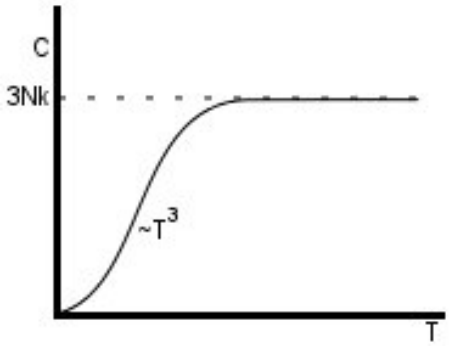

Figure 2.4: Debye's model of heat capacity C_D plotted with respect to temperature [2.11]

The Debye model of the heat capacity is a good approximation for low and high temperature. At reasonably low temperature of ~T_D/50, C_D is approximately linearly related to T^3 [2.11].

In the Einstein model, a crystal is assumed to have N oscillators of the same frequency ω_0 without coupling to each other. The Einstein DOS is

$$D(\omega) = N\delta(\omega - \omega_0) \text{ --- (2.27)}$$

and the heat capacity C_E

$$C_E = \frac{dU}{dT} = Nk_B\left(\frac{\hbar\omega}{\tau}\right)^2 \frac{e^{\hbar\omega/\tau}}{(e^{\hbar\omega/\tau} - 1)^2}$$

The approximation is simple but it only fits well with experimental results at high temperature. In practice, the low temperature heat capacity is often treated using the Debye T^3 law while the Einstein model is used to approximate the phonon part of the phonon spectrum.

2.2.3 Reducing thermal conductivity through engineering

Most of the bulk material engineering efforts in achieving an efficient thermoelectric material have focused on the reduction of the thermal conductivity. There are a number of ways in which this can be done but the basis is built on engineering defect to scatter phonons while not affecting the charge carriers, for example, alloy disorder, resonance scattering process, charge carriers (electrons), grain boundaries and with other phonons [2.1, 2.12-2.15]. The scattering process introduces some form of resistance to heat transport and reduces the thermal conductivity of a material. In a crystalline semiconductor, a spectrum of phonons with widely varying wavelengths and mean free paths ranging from 1nm to 10μm exists [2.10]. There is a need to introduce scattering agents over the full spectrum of phonon wavelengths while not affecting the electrons transport. In this section, a variety of engineering efforts will be presented on how the thermal conductivity of a thermoelectric material can be reduced.

The effect of introducing point defects scattering through alloying is the most straightforward way to reduce the thermal conductivity. For example, a thermoelectric alloy system which is widely used for high temperature applications is SiGe alloy [2.1, 2.16]. However, the trade-off in this method is the reduction of electron transport at the same time. Hence, the key here is to achieve an optimum amount of point defect such that the ratio of κ and σ value reduction is maximized. For example, it was computationally shown that in a SiGe alloy NW, the peak Z value is obtained at a 50% Ge concentration [2.17]. Another method which is used to reduce the thermal conductivity is resonance scattering

[2.12]. It is a process where phonons combine to excite a localized mode in the crystal. There are certain impurities in particular host lattices that give rise to a scattering which results in small dips or undulations in the thermal conductivity curves. This kind of process can also be understood in terms of inelastic scattering of phonons at the impurity modes [2.18-2.19]. In addition, scattering of phonons by charge carriers can be achieved by heavily doping a semiconductor. The dopants itself fulfill two functions, firstly, acting as scattering centers for phonons and restricting heat flow, and secondly, aids the transport of heat via the introduction of additional charge carriers (electrons/holes). However, such a method of increasing the ratio of σ and κ value differs between materials system. In n- type InSb for example, the thermal conductivity is higher than that of undoped InSb while p- type InSb exhibits the opposite trend [2.20]. Last but not least, the introduction of grain boundaries in a material such as a poly-Si can be used to selectively scatter long wavelength phonons, thus improving the σ and κ value ratio [2.21].

2.3 Semiconductor nanowire for thermoelectric applications

The thermal properties of crystal are an important area for study, with the first work pioneered by Callaway in 1959 [2.21]. Thermal properties of 1-D semiconductor NW is of interest in this thesis. The more widely studied thermoelectric nanostructures in the literature include BiTe NW and Si/SiGe/Ge based NW. The availability of theoretical works today on the thermoelectric

properties of Si/SiGe/Ge based NW initiated more experimental works to verify and better understand the potential and limitations for real-life applications [2.9, 2.22-2.26]. However, it is worth pointing out that in existing works and this thesis, the electrical properties of the NWs studied behave more like a "bulk" 3-D NW then to exhibit the quantum confinement effect. This is due to the NWs which we are dealing with having a much larger length scale.

2.3.1 Fabrication Methods

There are two main approaches to obtain semiconductor NW namely, bottom-up and top-down. In the following, we will describe synthesis methods for SiNWs; the concepts of synthesizing other conventional semiconductor materials system such as Ge or SiGe alloy are the same.

VLS (Vapor-Liquid–Solid) growth is a bottom-up method that typically takes place in a Chemical Vapor Deposition chamber [2.27]. In this technique, a catalyst (commonly gold (Au)) liquid alloy phase is introduced to rapidly absorb a vapor such that the vapor reaches super-saturation levels, and from which crystal growth can subsequently occur from nucleated seeds at the liquid-solid interface. During growth of SiNW, a silicon based source gas such as $SiCl_4$:H_2 mixture is fed into the chamber. Au-Si droplets will absorb Si from the vapor until reaching a super-saturated state of Si in Au, and thereafter Si atoms precipitate out of the super-saturated liquid-alloy droplet at the droplet/substrate interface as shown in

Figure 2.5. As more Si atoms precipitate out to the substrate, the droplet rises and the precipitation reaction continues.

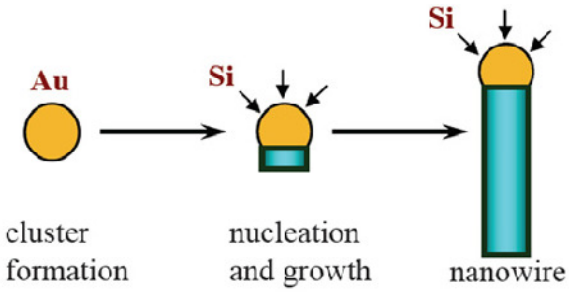

Figure 2.5: Schematic illustration of Si NW growth using VLS method. This reaction is catalyzed by gold-silicon droplet deposited on the wafer surface prior to whisker growth.

In this method, theoretically, the orientation of the SiNW grown will be dependent on the substrate as the growth is epitaxial. This is beneficial as the desired orientation for use in device fabrication can then be predetermined. However, there are several issues from synthesizing SiNWs from this method which can be attributed to the size variations of the Au catalysts to obtain SiNW with uniform diameters (Figure 2.6).

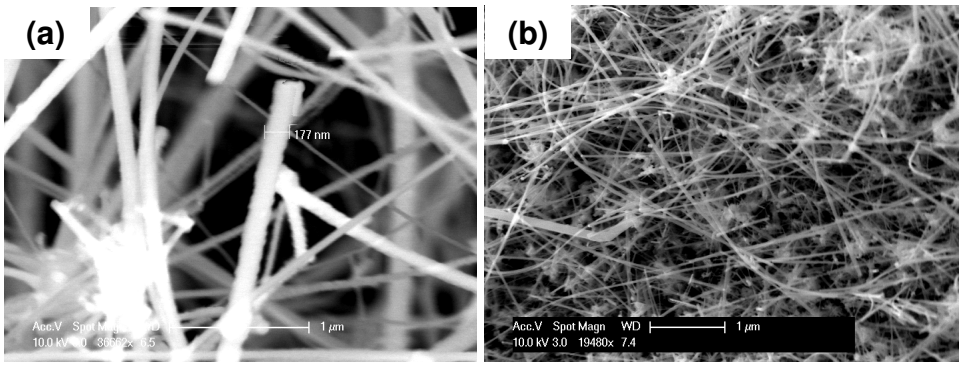

Figure 2.6: SiNW grown from VLS method. (a) The non-uniformity in size of the SiNW and (b) random orientation of the growth SiNW are clearly seen.

These are the limiting factors of using VLS grown SiNW for industrial scale applications, where control is of utmost importance. Nevertheless, the bottom-up method allows for a simple and straightforward synthesis of large amount of SiNW and is especially popular among researchers for study of the properties of individual NWs [2.22, 2.24-2.26].

In the top-down method, SiNW are usually fabricated with the aid of conventional optical lithography [2.28-2.30]. The SiNW are then defined using an etching process. Figure 2.7(a) and (b) show examples of lateral and vertical SiNWs, respectively, that can be synthesized using the top-down approach.

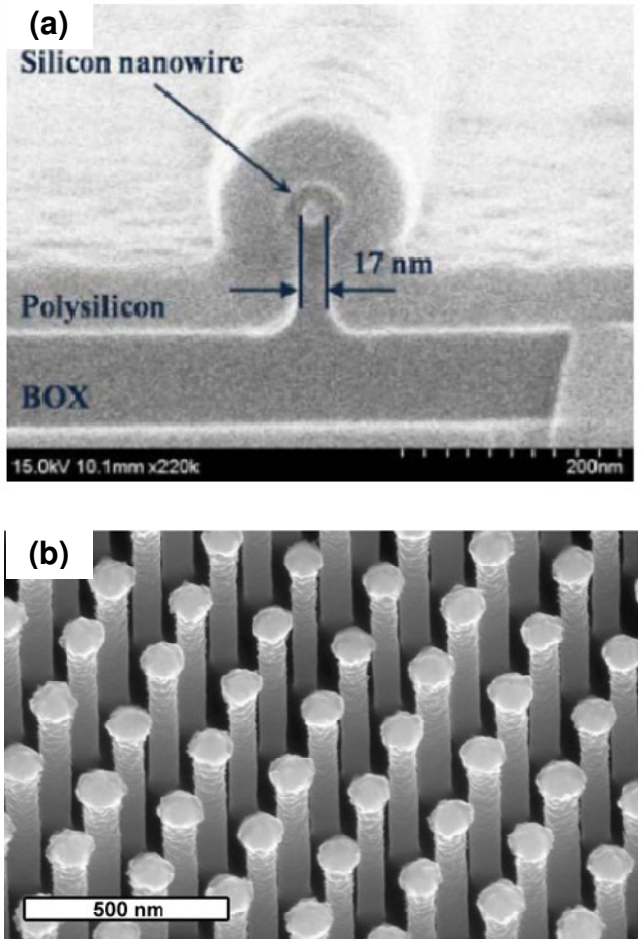

Figure 2.7: SEM images of (a) lateral SiNW [2.30], and (b) vertical SiNW array synthesized using the top down approach [2.31]

The disadvantages associated with using the top-down method includes- (but are not limited to) the density being limited by the lithography technology and the cost involved as compared to the bottom-up method. The main advantages of using the top down method on the other hand are the control over the size and locations of placing the SiNW structures, and the process compatibility with current industry standard. This implies easy implementation of this method into

today's industry process flow. In this thesis, the top-down method is the preferred method in obtaining Si/SiGe/Ge based NWs.

2.3.2 Development of silicon/silicon-germanium/germanium nanowire for thermoelectrics

The great interest in Si/SiGe/Ge NWs is due to the materials being the core of the modern electronics industry. In just a short period of less than two decades, a number of theoretical and experimental works have been carried out. There is significant reduction of thermal conductivity in NWs as compared to their bulk counterparts [2.22-2.26] mainly due to enhanced boundary scattering at the nano length scale. Theoretically, Mingo *et al* [2.32] predicted the thermal conductivity of Si/Ge NW by using "real dispersions" and considering interatomic potentials. It was found that the thermal conductivity calculations for Ge are ~2x lower than that of SiNW. However, the results could only serve as a reference to future work due to the lack experimental works for Ge NW currently. In 2008, the study of Trinh *et al* [2.33] of SiNW using Boltzmann transport equation and *ab initio* electronic structure calculations found that the growth direction and the tuning of surface structure can be used to improve the *ZT* value. The largest *ZT* was calculated for the [001] orientation followed by [011] and [111]. It was suggested that further improvement is achievable by alloying SiNW with Ge, thus highlighting the benefits of Ge alloying. In order to enhance phonon boundary scattering, Liu *et al* [2.34] investigated the reduction of SiNW thermal conductivity through induced surface roughness. It was found that the thermal

conductivity of SiNW can be reduced significantly by altering the surface roughness wavelength and amplitude. Besides modeling, simulation approaches such as Monte Carlo (MC) and Molecular Dynamics (MD) also offer a valuable avenue to further analyze and predict the thermoelectric properties of NWs [2.35-2.38]. However, with all the theoretical works reported, the NW in study is often of computationally manageable dimensions, i.e., in the order of a few nm at most. Such sizes are currently rare in experimental works.

In the experimental works reported, the majority of the reports discuss the thermoelectric properties of individual NWs; the integration of NW into a complete TED only started to appear lately. In the reports on individual NWs, the thermal transport attracted more attention as compared to the electronic properties. Most of the measurements for studying the thermal transport were made using a suspended device consists of micro heaters/temperature detectors and electrodes. This device (Figure 2.8) and the methods used are similar to that reported by Li *et al* [2.39], and provided a good platform for thermoelectric properties measurements.

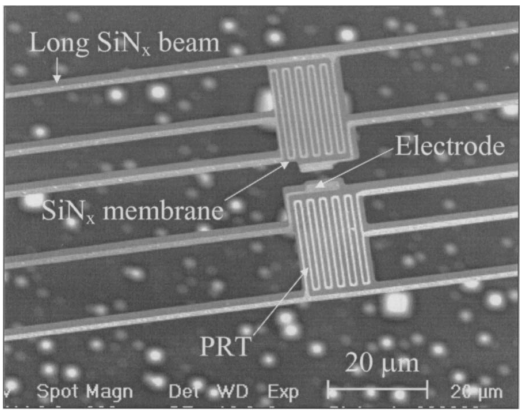

Figure 2.8: SEM image of a microfabricated device used to measure nanostructures thermal properties [2.39]

In addition, other existing thermal measurements methods include the thermoreflectance techniques [2.40] and the 3ω method [2.41]. However, measurements using the suspended device method proved to be the most popular one due to its simplicity and accuracy.

In 2003, Li *et al.* reported on the thermal conductivity of SiNW with diameters ranging from 22 nm to 115 nm. This work was one of the first which discussed the thermal properties of SiNWs. The measurements show that the thermal conductivity of the SiNW reduces as the diameter decreases. It was a good indication that enhanced phonon scattering at the SiNW boundary occur as the SiNW's diameter scales down.

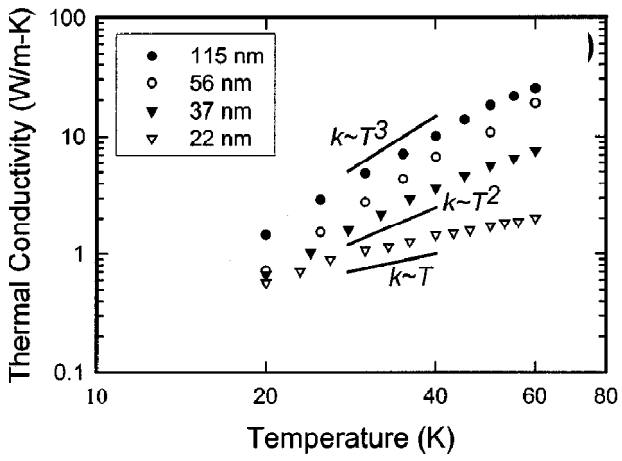

Figure 2.9: Thermal conductivity results extracted from 20 K to 60 K and plot in logarithmic scale [2.26]

An interesting observation was that when the results from 20 K to 60 K are plotted on a logarithmic scale (Figure 2.9), the thin SiNWs (diameter 37 nm and 22 nm) start to deviate from the Debye T^3 law. Specifically, the exponential power is reduced from 3 to 1 from the SiNW of 115 nm diameter to SiNW of 22 nm diameter. When the diameter of the SiNW is large, phonon boundary scattering is the dominant phonon scattering mechanism, and the thermal conductivity follows the temperature dependence of specific heat. However, as the SiNW diameter decreases, the violation of the Debye T^3 law could suggests strongly that the confinement effects has started to appear, and led to reduced phonon group velocities. The interesting observation of the Debye T^3 law violation of thin SiNW at low temperature prompted Chen *et al* [2.25] to further investigate the low temperature dependence thermal conductivity of SiNW with small diameters < 30 nm. The thermal conductance measurements of the SiNW at low temperature (20 K to 100 K) in Figure 2.10 is consistent with that of Li *et*

al.'s (Figure 2.8); the Debye T^3 law is indeed violated and the thermal conductance has a linear relationship with temperature.

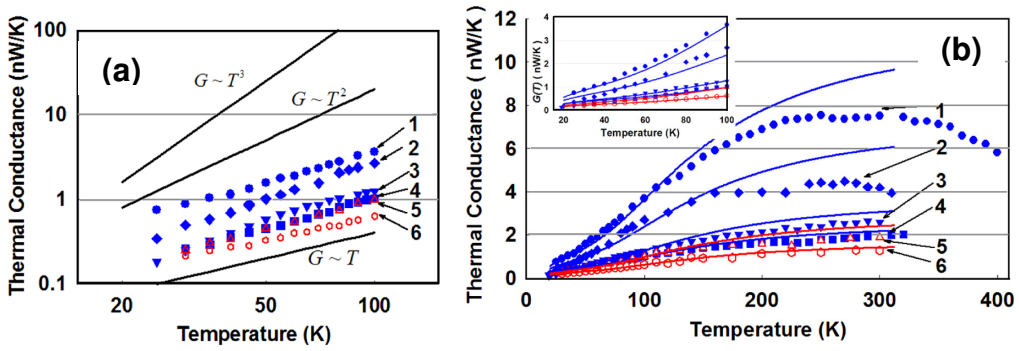

Figure 2.10: (a) Thermal conductance of thin SiNW measured from 20 K to 100 K and (b) thermal conductance of thin SiNW over a temperature range of 20 K to 400 K. The theoretical model (solid line) is fit to the experimental model (dotted line) [2.25].

In order to explain the observations, the Landauer expression of the thermal conductance of a cylinder with boundary scattering was derived. Without going into the rigorous mathematical derivation of the theoretical model, the explanation is such that at low temperature the unusual linear behavior of the thermal conductance is a result of the competition between the two phonon transmission regimes: the specularly scattered modes in thin SiNW, and the other phonon modes in bulk materials. Surprisingly, the curve plotted from the proposed model is in excellent agreement with measured results at low temperature (Figure 2.9(b)) It was then claimed that for thin SiNW, the contribution from the specularly scattered mode should be taken into account in the theoretical model. It seems to suggest the model is a plausible explanation for Li *et al.*'s reported work [2.26].

As compared to SiNW, there are far fewer reports on SiGe alloys. Although SiNW is a potential thermoelectric material, alloys of SiGe can prove to

be much more superior. In a separate experiment, Li *et al*. measured the thermal conductivity of Si/SiGe superlattice NW [2.24]. As compared to SiNW of similar diameters, the Si/SiGe NW exhibited ~5x lower thermal conductivity, which was attributed to the alloy scattering effect. Further analysis of a homogeneous SiGe NW will be helpful in understanding more of the phonon scattering mechanisms in such a material.

It is seen that prior works on the Si and Ge based NW focus solely on the thermal conductivity measurements. It was only recently that a more complete thermoelectric properties study on SiNW was reported. In 2009, two prominent articles by Hochbaum et *al*. (Berkeley) [2.22], and Boukai *et al*. (Caltech) [2.23], reported significant enhancement of the thermoelectric properties of SiNW. It is interesting to note that the reported works appeared within a short time period and were carried out independently of each other. In the Berkeley's group, rough SiNWs were obtained using electroless etching. It was found that the thermal conductivity of the SiNW is dependent on the surface roughness. However, as the induced surface roughness arose from a random process, it was not possible to find a direct relation between it and the thermal conductivity measured. Surprising thermoelectric parameters of a 50 nm diameter rough SiNW, doped to a concentration of ~10^{19}cm^{-3} at room temperature were measured: S = 240μV/K, σ = 5.88 x 10^{-4}S, and κ = 1.6W/mK, translating to a ZT value of 0.6. At Caltech, similar work was performed on SiNWs. The difference was that the study was not on the effect of surface roughness but rather on the size effect. SiNW down to a dimension of 10nm x 20nm exhibited huge reduction in thermal conductivity

compared to bulk Si, up to ~200x lower for the 10 nm SiNW at 200K. Consequently, the *ZT* value of 1 peaked at 200K for the 20nm wide SiNW. The ZT measurement results of both groups are as shown in Figure 2.11.

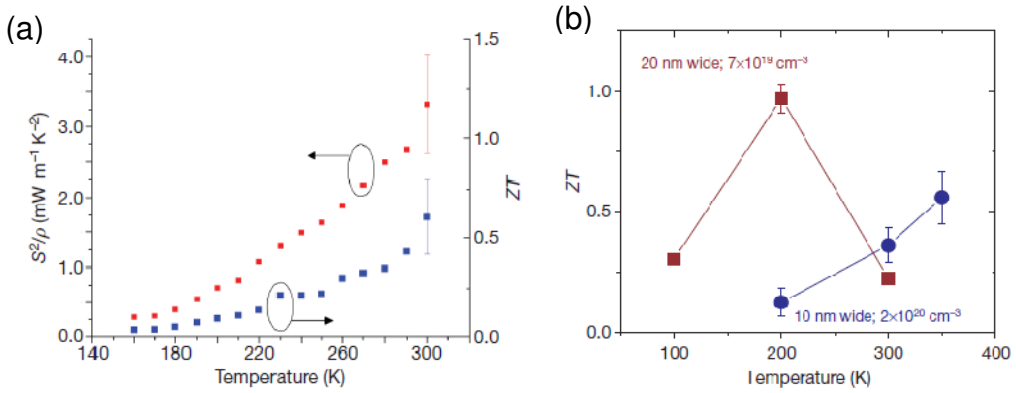

Figure 2.11: Thermoelectric properties measurements of a) rough SiNW by Berkeley group [2.22], (b) Ultra thin SiNW by Caltech group [2.23]

It is worth noting that both claims of the *ZT* enhancement are attributed mainly to the significant thermal conductivity reduction. In the Berkeley's group, the mechanism in place is argued to be phonon boundary scattering, and this effect is further enhanced via roughness in the SiNW surface. The Caltech group's argument on the other hand, was the effect of both phonon boundary scattering and phonon drag in the SiNW [2.22-2.23]. Regardless, these two reports appear to be intriguing as currently, there is no theoretical prediction that the enhancement can be of this order at diameters > 10 nm.

2.3.3 Development of micro thermoelectric device for power generation/cooling applications

There are two areas of applications for thermoelectric which are attracting lots of interest, namely, on-chip waste heat harvesting and chip cooling. The use of micro/nano-scaled materials-based TED has potential in on-chip applications due to the existent of hot spots (~300 W/m^2) that are predominantly present in today's microprocessor [2.5, 2.42-2.43]. Of the functional TEDs reported, the use of Bi/Sb, poly-Si, and SiGe based materials are popular due to the merits of its bulk counterparts.

In 2007, researchers from the Research Triangle Institute (RTI) presented a thermoelectric power generator (TEG) using Bi_2Te_3 based superlattice materials [2.44]. The TEG was fabricated using MOCVD and assembled using standard semiconductor manufacturing tools. The limitation of this fabrication approach is the size of the TEG obtainable. To further scale down the size, a complete CMOS process can be used. A poly-Si thin film based TEG for MEMS applications reported was fabricated entirely using CMOS compatible process [2.45-2.48]. It consists of horizontally placed thin film with top and bottom cavity to maximize the temperature gradient (Figure 2.12).

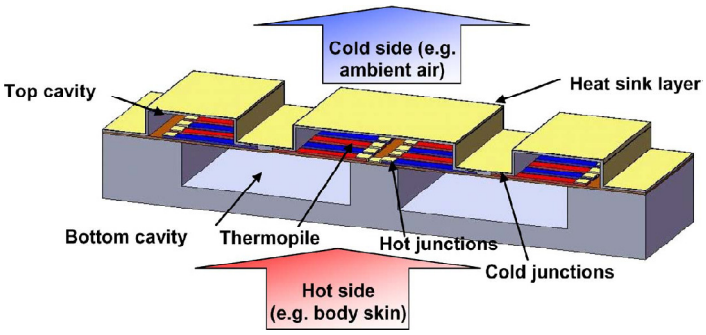

Figure 2.12: Schematic of a polysilicon thin film TEG fabricated using CMOS process [2.46]

The Seebeck coefficients of the n- and p- type poly Si are measured to be -132 μV/K and 147 μV/K, respectively; the values are of the same order as bulk Bi/Sb. With proper design to capture large temperature gradient, Si can prove to be a strong contender. Nevertheless, it is worth pointing out that the presence of a large electrical contact resistance limits the performance of the reported TEG [2.48]. The effect of electrical contact resistance is undesirable will be further amplified in nanostructures contacts [2.49]. Such an issue is still dominant and warrants further study and optimization.

The thermal management of a microprocessor usually involves the use of a conventional heat sink and fan. However, such an approach fails to address localize heating issues. Novel cooling solutions such as using micro-fluidic channel and embedded thermoelectric cooler [2.42] exist but the use of embedded thermoelectric cooler seems to be more attractive due to “on-demand cooling”, and has been actively studied by Nextreme and Intel [2.5, 2.43, 2.50]. One of the notable reports in 2009 was that of Intel demonstrating hot spot cooling using a

Bi_2Te_3 based superlattice based thin film thermoelectric cooler [2.5]. A total cooling capability of 15°C (passive and active) was achieved (Figure 2.13).

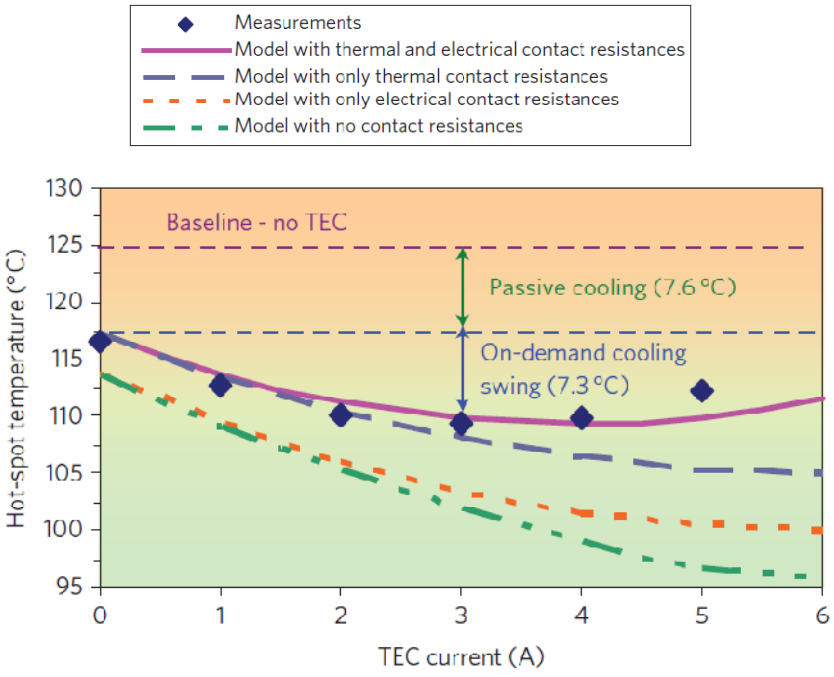

Figure 2.13: Performance of a BiTe based superlattice thermoelectric cooler cooling a hotspot [2.5]

This marked a significant progress of the potential in using nanoscaled thermoelectric cooler for targeted on-chip hot spot cooling [2.26-2.28]. Apart from Bi/SbTe based material, Fan *et al* demonstrated cooling performance of a one thermoelectric element SiGeC/Si superlattice cooler which should be further developed for on-chip application due to its CMOS compatibility nature [2.51].

There are proposals in the literature on fabricating a NW-based TED, for example, using alumina template assisted eletrodeposition (BiTe NW) and

catalyst grown (SiNW) methods [2.52-2.54]. In all, the key structure of a NW-based TED consists of a NW array composite layer to support the high aspect ratio NW. From the reports of the partial NW-based TED, the repeatability of the thermoelectric legs fabrication is poor due to the random growth process of the NW; hence the CMOS method is a good solution. In 2011 and 2012, the work of this thesis reported the first SiNW-based TED fabricated entirely using CMOS compatible process [2.56-2.57].

2.4 Chapter summary

In this chapter, we have presented an overview of thermoelectricity concepts, relevance to 1-D nanostructures, and the current developments of thermoelectric materials and devices. In the discussion, we focused on Si/Ge based NW which is of interest in this thesis. Most reported works on Si/Ge based NW are currently focused on the study of individual NW's thermoelectric properties Nevertheless, great effort has been made in moving towards a nanostructured TED, which provides a good platform for the development of Si/SiGe NW-based TED in this thesis.

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Chapter 3: Design of a Silicon Nanowire based Thermoelectric Cooler using Numerical Simulations

In this chapter, the thermoelectric performance of a silicon nanowire (SiNW) based thermoelectric cooler (TEC) will be explored using finite element analysis (FEA) simulation. Most of the works thus far on SiNW as thermoelectric material have focused on the thermoelectric properties [3.1-3.8] and have provided limited insight into using such material in a complete device. Although a thermoelectric device (TED) can operate in both cooling and power generation modes, analysis of the latter is much more straightforward with the Seebeck relation $S = \frac{dV}{dT}$, where the power output is dependent on the potential difference (dV) generated with a temperature difference (dT). Hence, this chapter aims to better understand the potential of using SiNW in a TEC [3.9-3.11]. Based on a systematic study using FEA on the key material parameters, a design guideline for a SiNW-based TEC for on-chip cooling application is then proposed [3.12].

3.1 Modeling of a single nanowire thermoelectric cooler

In this section, the FEA software COMSOL Multiphysics [3.13] was employed to study the performance of a SiNW-based TEC. In the FEA, classical heat and electrical transport models will be used to describe the SiNW-based TEC

performance. This approach is reasonable because when considering the length of the SiNW at micrometer scale, it has been shown that the accuracy is not compromised [3.14-3.16]. In 2010, two papers by Zhang *et al*. presented single-SiNW-based TEC FEA studies for both transient and steady-state modes using thermoelectric parameters obtained from the literature [3.17-3.18].

3.1.1 Thermoelectric field equations

In analytical form, the 1-D thermoelectric equation which stipulates the rate of absorption of heat from the cold side is given by [3.19]:

$$Q = ST_cI - \frac{1}{2}I^2R - \kappa\frac{A}{L}(T_h - T_c) \text{ --- (3.1)}$$

where the total heat absorbed (Q) is the net difference of the competition between the Peltier effect, Joule heating, and the heat reversal (hot to cold end) through conduction. In FEA, the thermoelectric equations are described by coupling the heat equation and Poisson's equation, and solving them simultaneously. Equations 3.2 and 3.3 describe the heat equation and Poisson's equation respectively.

$$-\vec{\nabla}\left((\sigma S^2T + \kappa)\vec{\nabla}T\right) - \vec{\nabla}\left(\sigma ST\vec{\nabla}V\right) = \sigma((\vec{\nabla}V)^2 + S\vec{\nabla}T\vec{\nabla}V) \text{ --- (3.2)}$$

$$\vec{\nabla}\left(\sigma S\vec{\nabla}T\right) + \vec{\nabla}\left(S\vec{\nabla}V\right) = 0 \text{ --- (3.3)}$$

where S, σ, and κ represent the Seebeck coefficient, electrical conductivity and thermal conductivity respectively. It is worth noting that equation 3.2 is a direct consequence of equation 3.1, and accounts for the 3-D form. Isotropic temperature-independent material properties will be used in order to reduce considerably the iteration time in the simulation. Specifically, equations 3.2 and 3.3 will be implemented using the "Coefficient Form" of the partial differential equation (PDE) of COMSOL Multiphysics [3.20]. The following PDE equations defined are used to describe the thermoelectric field equations:

$$e_a \frac{\partial^2 u}{\partial^2 t} + d_a \frac{\partial u}{\partial t} + \nabla \cdot (-c\nabla u - \alpha u + \gamma) + \beta \cdot \nabla u + au = f \text{ --- (3.4)}$$

$$n \cdot (c\nabla u + \alpha u - \gamma) + qu = g - h^T \mu \text{ --- (3.5)}$$

$$hu = r \text{ --- (3.6)}$$

In equation 3.4, e_a and d_a are zero for steady-state calculation. Equation 3.5 is a generalized Neumann boundary condition (or natural boundary condition), and equation 3.6 is a Dirichlet boundary condition (or boundary constraints condition). The thermoelectric equations in 3.2 and 3.3 are modeled in the "Coefficient Form" PDE equations with the field variable

$$\vec{u} = \begin{pmatrix} T \\ V \end{pmatrix} \text{---(3.7)}$$

and coefficients c and f in equation 3.4 are given as

$$c = \begin{pmatrix} \lambda + \sigma S^2 T & \sigma S T \\ \sigma S & \sigma \end{pmatrix} \text{--- (3.8)}$$

$$f = \begin{pmatrix} \sigma((\vec{V})^2 + S\vec{\nabla}T\vec{\nabla}V \\ 0 \end{pmatrix} \text{--- (3.9)}$$

3.1.2 Silicon nanowire model

The baseline model which was used for the simulation is depicted in Figure 3.1, which shows a single SiNW being contacted at both ends by aluminum (Al) electrodes. The geometry of the SiNW was modeled as a long rectangular cuboid with varying length x μm, in which the length of each side of the cross-section is equal to the diameter.

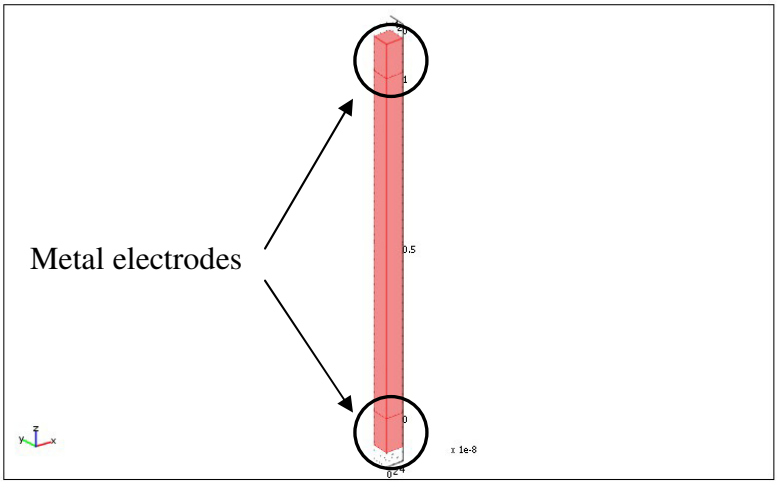

Figure 3.1: Model of the single SiNW contacted at both ends by metal electrodes (Al)

Leveraging on the many reports of the thermoelectric properties of SiNW, reported values of S, λ, σ will be used in the simulation [3.1]. In the following sections 3.2 and 3.3, the cooling performance of a single SiNW with varying parameters, namely thermal conductivity, length of the SiNW, surrounding material of the SiNW, and the electrical contact resistance of a SiNW-Metal system will be systematically studied.

3.2 Effect of thermal conductivity, length and filler material on a silicon nanowire-based thermoelectric cooler

3.2.1 Effect of thermal conductivity

In a TEC, the thermal conductivity plays an important role in determining how efficient it can be operated. Analytically, the thermal conductivity determines how rapidly heat can be transported between the hot and cold side of the device. To illustrate further, a TEC works by removing the heat from the cold side to the hot side electrically. Hence, a low thermal conductivity of the thermoelectric material is desired so as to reduce the reversal heat flow (hot side to cold side) from happening. SiNW has a lower thermal conductivity than its bulk counterpart, but depends on several parameters such as its diameter, concentration of point defects, and surface roughness [3.1-3.4].

We will first discuss the effect of thermal conductivity on the cooling performance of a single SiNW of length 1 μm without any applied heat load. The

SiNW cooling performance is simulated based on reported parameters of SiNWs [3.1-3.2]. The difference in the SiNWs' parameters reported is the thermal conductivity due to differences in surface roughness. However, there is minimal variation in S and σ as compared to bulk Si [3.1]. Table 3.1 shows the different parameters used in this simulation.

Table 3.1: Material parameters used in the simulation. The different kinds of SiNW used (electroless etch *versus* VLS) are indicated in the parentheses where r – rough, s – smooth. [3.1]

Cross sectional dimension	***κ (W/mK)***	***S (μV/K)***	***σ (S)***
50nm x 50nm (r)	1.6	245	5.88×10^4
50nm x 50nm (s)	25		
98nm x 98nm (r)	5		
115nm x 115nm (r)	8		
115nm x 115nm (s)	40		

Varying current is passed through the SiNW while maintaining the hot side at 300K. The temperature difference (dT) is observed. Subsequently, dT for the different SiNWs listed in Table 3.1 were calculated. The results of the dT obtained for different current are plotted and shown in Figure 3.2(a). The comparison of both the 50nm x 50nm SiNW is shown separately (Figure 3.2 (b)).

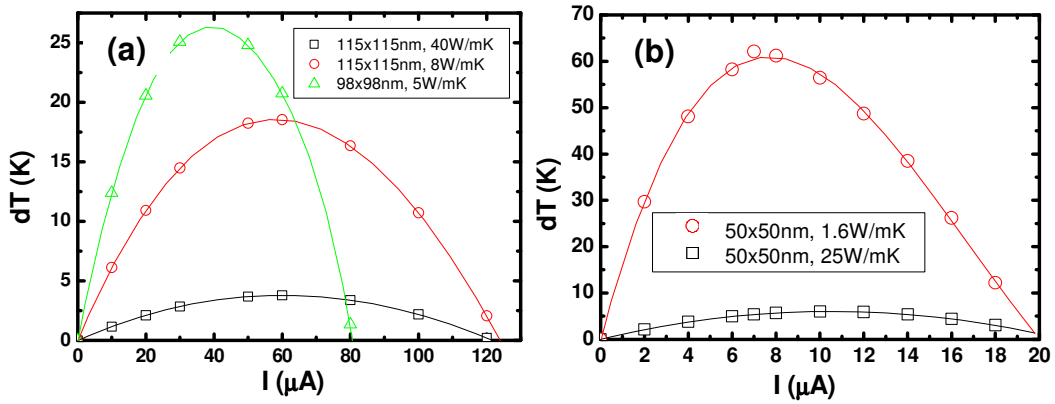

Figure 3.2: Dependence of cooling temperature on thermal conductivity and applied current of SiNWs that are 1μm long. The symbols are simulated results while the line is drawn for clarity. a) 115nm, 98nm SiNWs, b) 50nm SiNWs. Geometry of the SiNWs with different thermal conductivity used are indicated in the legend.

In both figures, the solid line represents a polynomial fit to the data points obtained. From Figure 3.2(a) and (b), it can be observed that the cooling performance improves as the diameter of the SiNW scales down due to the reduction of the thermal conductivity. A maximum *dT* of ~60K was obtained from the SiNW of size 50nm x 50nm and a thermal conductivity of 1.6W/mK, which is the same as that reported by Zhang *et al*. [3.18]. The *dT* obtained by an equivalent size SiNW with a higher thermal conductivity of 25W/mK is ~5 K, which is significantly lower. For comparison purpose, the rated *dT* of a state-of-the-art TEC made from bulk Bi_2Te_3 based material is in the region of 60K [3.21]. A large lowering of temperature is clearly an important parameter for defining performance in commercial TEC.

3.2.2 Effect of silicon nanowire length

Using the same model, we next investigate the effect of applying various heat loads at the cold side of the SiNW. This is especially useful in the design of a TEC for specific applications where the heat load to be removed is known. Using the properties of the SiNW with size 50nm x 50nm and thermal conductivity of 1.6W/mK, varying heat loads (0W, 0.2μW, 0.4μW and 0.6μW) were applied to the hot side of the SiNW. We obtained the cold side temperature under different current flow through the SiNW, and in total, results for SiNW of length 1μm and 2μm were plotted in Figure 3.3(a) and (b), respectively.

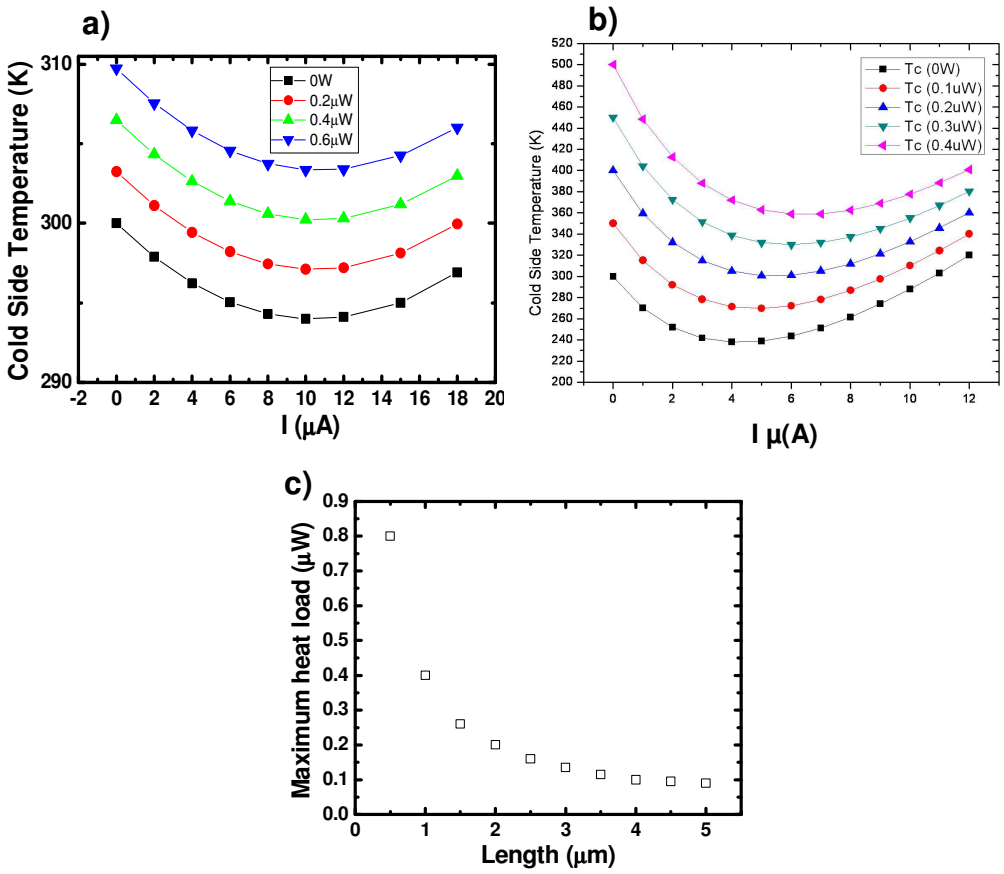

Figure 3.3: Temperature at hot side of SiNW with varying heat loads and applied current. a) SiNW of length 1μm, b) SiNW of length 2μm, c) dependence of SiNW length on the maximum heat load pumped

There are a few observations; firstly, the lowering of the cold side temperature can be achieved in the presence of any heat load. The maximum amount of heat load removable is defined as the heat load applied for which, at optimum current (for maximum depression), the temperatures of the hot end and cold end are equal (300 K in this case). From the results, we see that a shorter SiNW favors a much larger target heat load, i.e. 0.4μW and 0.2μW for the 1μm and 2μm SiNW, respectively. Extending the model to several lengths from 0.5μm to 5μm, the results are plotted in Figure 3.3 (c). It is seen that as the length of the SiNW is decreased, the heat load removable increases. Quantitatively, the simulated cooling performance of SiNW (assuming zero parasitic resistances) is compared with state of art thermoelectric material shown in Table 3.2.

Table 3.2: Performance of simulated SiNW cooling performance with literatures

	***dT* (max) at 0 W heat load**	**Heat flux (max)**
SiNW (simulation – 2μm, $(50nm)^2$, zero parasitic)	62K at 300K	8000 W/cm^2 at 300K
Bi_2Te_3/Sb_2Te_3 bulk device [3.22]	83K – 92K at 353K	92-132 W/cm^2 at 353K
Nanostructured SiGe thin film (<10μm) [3.23]	7K at 373K	1000 W/cm^2 at 373K
Nanostructured Bi_2Te_3 thin film (<10μm) [3.24]	55K at 300K	715 W/cm^2 at 300K

From the comparison Table 3.2, it can be observed that the temperature depression of SiNW at the ideal case is respectable, and is slightly worse off than

that of the state-of-art TEC. However, it is commendable that the heat load removal capacity surpasses that of the state-of-the-art material TEC. Nevertheless, non-idealities in the design, which will be discussed in the following sections, should be taken into consideration as well.

3.2.3 Effect of filler material

The above analysis dealt with the electrical and thermal properties of the SiNW and would have been sufficient if the use of SiNW in a thermoelectric is as straightforward as the baseline model. However, in the case of NWs, this is hardly the case; there have been quite a number of reports to date which describe experimentally the fabrication of a SiNW array based thermoelectric leg [3.25-3.26]. In all, the structure of the TEC included some kind of a filler material in between the SiNWs. The composite layers (SiNW with a filler material) include, but are not limited to SiO_2, polymers such as parylene and polyimide, and alumina template. In this set of simulations, we termed the filler material as the surrounding material of the SiNW. Using the same model, we modeled 50nm of surrounding material around the SiNW. We varied the thermal conductivity of the surrounding material and obtained the maximum dT which can be obtained under optimum current through the SiNW. The results of the dT as a function of surrounding material thermal conductivity is plotted in Figure 3.4.

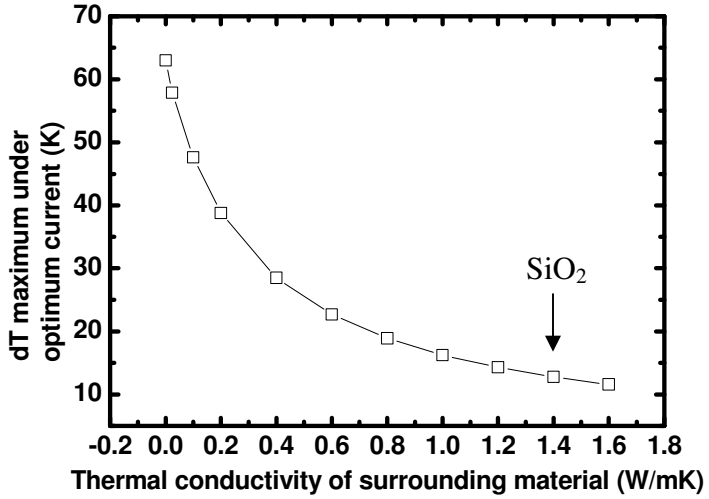

Figure 3.4: Dependence on the maximum cooling temperature with surrounding material of different thermal conductivity

In Figure 3.4, it can be seen that although SiO_2 has a relatively low thermal conductivity of ~1.4 W/mK, the maximum *dT* can still be degraded greatly, i.e., a reduction of maximum *dT* from ~60K to ~13K. Air is the best material with a thermal conductivity of 0.024W/mK but does not provide any form of reliable mechanical support. Alternatively, polymers like parylene or polyimide (κ ~0.14W/mK) are some of the better materials for consideration in place of SiO_2. The effect of the filler material on the maximum thermoelectric power output will be explored in Chapter 5.

3.3 Effects of electrical contact resistance on a silicon nanowire-based thermoelectric cooler

In the previous section, we have presented the SiNW TEC performance dependent parameters such as thermal conductivity, length, and the choice of

filler material. However, the results discussed and in other reported works of a similar nature were based on zero electrical contact resistance; hence, it does not fully represent the real-world scenario. While the electrical contact resistance is less of a concern for TEC using bulk material (mm^2 sized contact per thermoelectric leg [3.10]), its impact in nanostructures cannot be underestimated. In this section, we are going to extend the simulation effort in the previous section and address the effect of the electrical contact resistance on the performance of a SiNW TEC system. This will be done using a combination of experimental effort to extract the electrical contact resistance of metal to SiNW, and the simulation methodology presented earlier.

3.3.1 Experimental details

In any nanostructured device, the electrical contact resistance is critical [3.27]. In order to achieve a good contact with the nanostructure, complementary metal oxide semiconductor (CMOS) process is preferred due to the widely developed infrastructure and the stringent processing conditions. To better understand the magnitude of electrical contact resistance obtainable via CMOS process, we first experimentally extract the electrical resistivity values of a SiNW-metal system, where the choice of metal is aluminum (Al). On an 8" Si wafer, SiNWs of diameter 100 nm and pitch 400nm were first formed via nano-dot lithography and dry reactive ion etching (DRIE) method using SF_6 and CF_4 gas chemistries. In order to extract the SiNW resistivity, two sets of test structures

with SiNW length of 0.6µm and 1.1µm were fabricated. The idea was that by subtracting the resistance values of the two sets of SiNWs measured independently later, 0.5µm of SiNWs (without contact resistance) can be obtained. Following, the SiNWs were doped n- type to a concentration of ~10^{19} cm^{-3} using Phosphorus ion implantation which was verified with process simulation (Synopsys Tsuprem4). Thereafter, a filler material oxide (SiO_2) was deposited between the gaps between the SiNW, and etched back to expose the SiNW tips (100nm); the filler material acts as support for the final metallization. Finally, the exposed tips were contacted with Al metallization for electrical measurements. The SEM images of the different lengths of SiNW etched (0.6µm and 1.1µm), the exposed SiNW tips (100 nm) and the schematic of the completed test structure are shown in Figure 3.5(a) to (d), respectively.

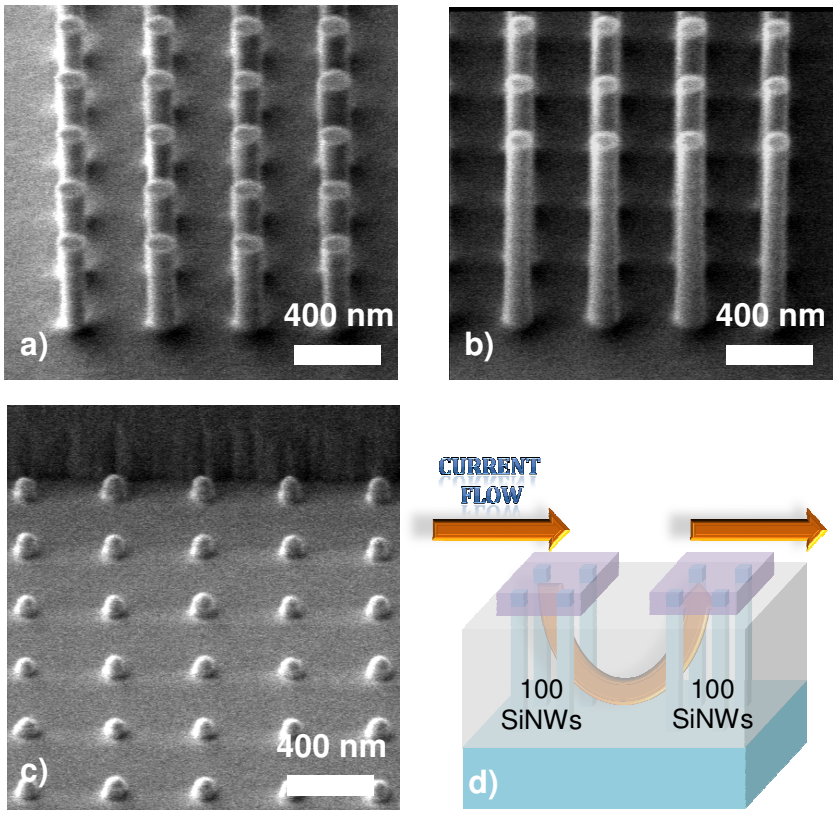

Figure 3.5: a) SEM image of the SiNW with length 1.1µm, b) SEM image of the SiNW with length 0.6µm, c) SEM image of SiNW tips (100 nm) exposed after SiO_2 etchback, and d) Schematic of the fabricated test structure. The two groups of SiNW (100 SiNW each) are electrically connected in series through the silicon substrate at the bottom, and through Al on the top, hence, the current flow direction as indicated by the arrow.

In the completed test structure, two groups of SiNWs (100 SiNWs each) are electrically connected in series through the silicon substrate at the bottom, and through Al on the top (Refer to Figure 3.5(d)). Details on the fabrication process of a SiNW-based TED will be presented in Chapter 4.

3.3.2 Electrical contact resistance of a silicon nanowire-aluminum system

Following, the electrical resistivity (ρ) of the SiNW and electrical contact resistivity (ρ_{con}) between SiNW and Al were extracted. In the measurement and extraction process, we assumed that the contacts on both sets of SiNW (Figure 3.5(a) and (b)) were identical due to similar geometry and process conditions. Hence, it was deduced that the difference in the resistance values will provide the resistance of 200 SiNWs (100 SiNWs x 2) of length 0.5µm without the effect of contact resistance. The measurements of the test structures show that the contacts of the SiNW-Al system are ohmic as shown in Figure 3.6(a). In Figure 3.6(b), the distributions of the electrical resistance of the two sets of SiNW over 30 dies at different locations on the wafer are plotted in the form of box plots. From the measurements, a mean value of ρ was obtained as 4.7 x $10^{-3}\Omega$cm, which agrees very well with reported values of bulk silicon at similar doping concentration [3.28]. At the dimensions of the fabricated SiNW (in this work), the electrical properties are not affected much as compared to the thermal conductivity [3.1].

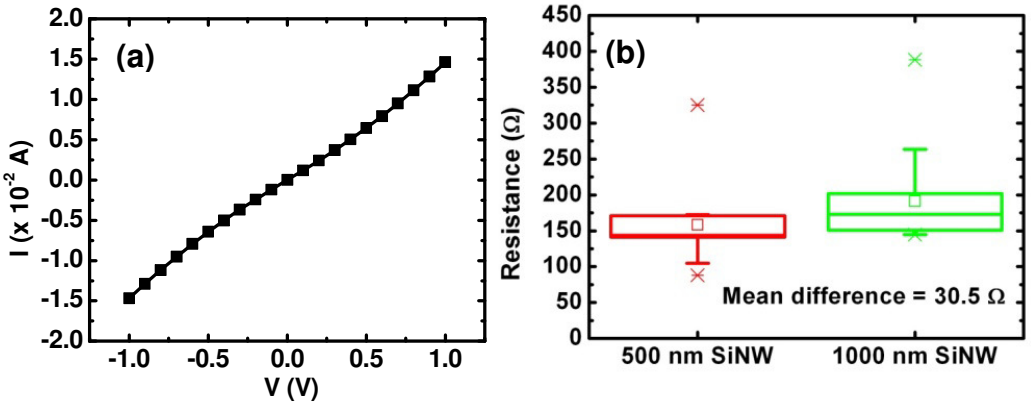

Figure 3.6: (a) I-V measurements of a 0.5µm tall SiNW test structure indicating ohmic contact, and (b) box plot of the resistances obtained for the SiNW test structures of two different effective lengths – 0.5µm and 1µm, measured over 30 dies.

To extract the ρ_{con} of the SiNW-Al system, test structures without the SiNW on the same wafer were measured; this is to find out the substrate contribution to the total resistance of the SiNW test structures (Figure 3.5(d)). It was found that the substrate contribution to the total resistance presented in Figure 3.6(b) is less than 3%. This indicates that the dominant resistance comes from the SiNW and its contact to Al. Hence, a mean value of ρ_{con} – 6.1 x 10^{-2}µΩcm^2 was extracted. In our fabrication process, the SiNW were doped to a high level of 10^{19}cm^{-3} to achieve good contacts, which is close to the degenerate level of bulk Si. The extracted ρ_{con} from our measurements is significantly lower than VLS grown SiNW as reported in the literature, i.e., 1.3 x 10^{-1}µΩcm^2 to 5 x 10^{2}µΩcm^2 [3.27, 3.29]. The results obtained indicated the advantages of using CMOS process; the doping level was precise, as well as the prevention of surface states formation in the contacts. Nevertheless, it should be noted that the doping level in this work was not optimized.

3.3.3 Modeling of a silicon nanowire-based thermoelectric cooler with electrical contact resistance

Using the same model shown in Figure 3.1, an interface material of negligible thermal resistance was introduced to represent ρ_{con}. Apart from the values of ρ and ρ_{con} which were taken from our experimental results, the same S and κ from the previous section were used for a new FEA simulation (with contact resistance factored in). In the first set of simulations, we varied ρ_{con} (Min – 1.8 x 10^{-2}μΩcm^2, Mean – 6.1 x 10^{-2}μΩcm^2, Max – 1.9 x 10^{-1}μΩcm^2) while maintaining a fixed SiNW length of 1μm. In the second set of simulations, we varied the SiNW length (1μm, 2μm, 3μm), while maintaining a fixed mean ρ_{con} of 6.1 x 10^{-2}μΩcm^2. The results of *dT versus* the operating voltage ($V_{operating}$) are plotted in Figure 3.7(a) and (b). It should be noted that the use of the operating voltage rather than the operating current differs only by a factor equal to the resistance value of the SiNW. From Figure 3.7(a), it can be seen that an increase in ρ_{con} from zero (ideal case) to 1.9 x 10^{-1}μΩcm^2 (maximum measured value) reduces the maximum dT by 35%. On the other hand, maximum dT is found to increase with SiNW length (Figure 3.7(b)) and thus can be used to partially mitigate the impact of high contact resistance. Furthermore, regardless of ρ_{con} or SiNW length, the optimum $V_{operating}$ for maximum dT remains the same, which in this case is 0.07V. We modeled the simulated results by incorporating the contact resistance term at the cold side in the thermoelectric equation 3.1 and making $dT = T_h - T_c$ the subject. The modified analytical equation with electrical contact resistance can thus be written as

$$dT = \frac{ST_hI - \frac{1}{2}I^2R_{leg} - I^2R_{con}}{SI + \kappa\frac{A}{l}} \text{ --- (3.10)}$$

where R_{con} is the contact resistance at the cold side, R_{leg} is the resistance of the thermoelectric leg and T_h is the hot side temperature. The term I^2R_{con} is the result of localized Joule heating caused by the non-zero electrical contact resistance. Equation 3.10 matches very well with the FEA simulation results as indicated by the dotted lines in both Figure 3.7(a) and (b). Shown in Figure 3.8(a) and (b) is the cooling per SiNW – *dT* created by the single SiNW TEC *versus* varying heat load. Both graphs were plotted with varying ρ_{con} and length as indicated in the legend, while the optimum $V_{operating}$ applied across the SiNW was fixed at 0.07V.

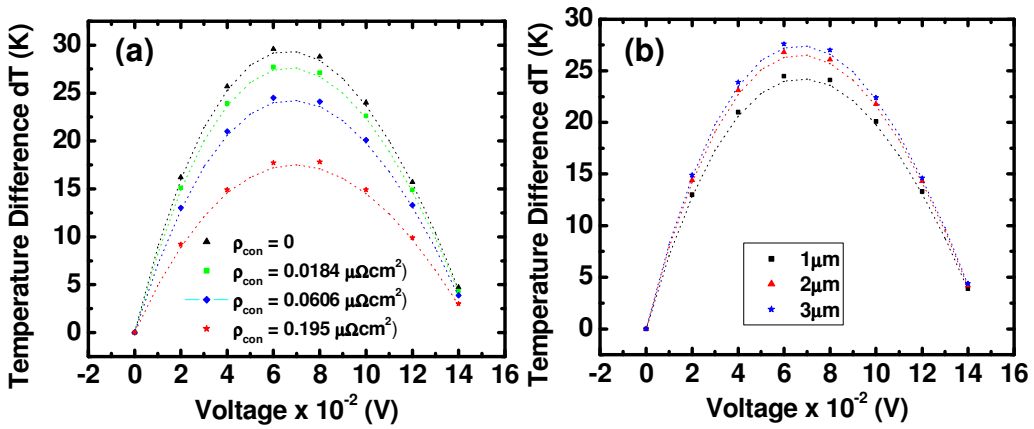

Figure 3.7: Steady state thermoelectric performance simulation: dT across SiNW *versus* $V_{operating}$. (a) Varying ρ_{con} with a fixed length of 1 μm and (b) varying lengths as indicated in the legends with a fixed mean contact resistivity of 6.1 $x10^{-2}$μΩcm^2. In both cases, the optimum $V_{operating}$ to provide maximum achievable *dT* is 0.07V. Symbols represent simulated data while dotted line the analytical model

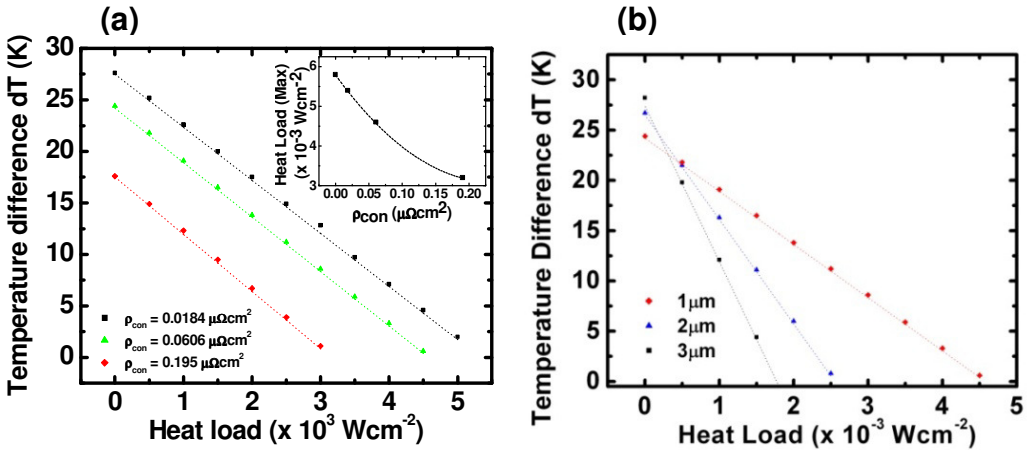

Figure 3.8: *dT* across the SiNW *versus* heat load applied to the cold junction of the SiNW while operating at 0.07V (optimum $V_{operating}$); (a) varying ρ_{con} as indicated in the legend with a fixed length of 1μm, and (b) varying length as indicated in the legend with a fixed mean contact resistivity of 6.1 x 10^{-2} μΩcm^2. Inset of both graphs shows the corresponding maximum removable heat load (heat load which reduces the maximum *dT* to 0K). Symbols represent simulated data while dotted line the analytical model.

The inset of the graphs shows the maximum removable heat load with respective variations (ρ_{con} and length). It can be seen that apart from the length of the SiNW, the heat load removal capability is a strong function of ρ_{con} as well. The ρ_{con} contributes towards unwanted Joule heating and reduces the amount of external heat that can be removed to the hot side. In the presence of the ρ_{con}, the benefits of using a short SiNW for heat load removal becomes apparent. Equation 3.11 provides the analytical model for heat removal capability with the inclusion of the electrical contact resistance which agrees well with the simulations.

$$dT = \frac{-Q}{SI+\kappa\frac{A}{l}} + \frac{ST_hI-\frac{1}{2}I^2R_{leg}-I^2R_{con}}{SI+\kappa\frac{A}{l}} \quad \text{--- (3.11)}$$

where Q is the external heat load applied to the cold side. It should be noted that both equations 3.10 and 3.11 offer an estimation of the performance of a SiNW TEC with the inclusion of electrical contact resistance. However, the simulation approach is recommended to obtain more accurate performance parameters for different and/or more complicated SiNW systems.

3.4 Proposal of a SiNW-based TEC design guideline for on-chip cooling application

In this section, the analysis based on the FEA results in section 3.3 will be incorporated into a design methodology for a SiNW based TEC. In the design, there are several parameters that can be designed as follows: heat load to be removed (Q), number of thermoelectric legs, fill factor – Pitch (P) and number of SiNW (N), and hot spot size. It is well worth noting that the SiNW thermoelectric material properties (S, κ, ρ) are determined through the fabrication technology used. The inclusion of ρ_{con} in our design methodology is critical. However, the real question is the magnitude of ρ_{con} that a SiNW based TEC should be designed for. Practically, the magnitude of ρ_{con} has an extremely wide range depending on how good the contact is in the SiNW-metal system; this is especially so with the large number of contacts made in a SiNW array. Hence, the maximum ρ_{con} values achievable in the fabrication process should be used. However, considering the large statistical variation in Figure 3.6(b), a statistical approach to this problem would be reasonable. We propose using the central limit theorem (CLT) and

select appropriate ρ_{con} value to achieve certain success probability. For a given probability, the suitable ρ_{con} value can be calculated using equation 3.12.

$$\rho_{con}(to\ be\ used) = z \times \sigma_{\rho_{con}}(measured) + \overline{\rho_{con}}(measured) \text{--- (3.12)}$$

where the z value is related to the z-distribution statistics and can be obtained from a Z-table [3.30]. By obtaining at least 30 different data points, the statistical parameters can be calculated easily [3.31]. In our experiments, $\overline{\rho_{con}}$ is 6.1 x 10^{-2}μΩcm^2 while standard deviation '$\sigma_{\rho_{con}}$' is 7.7 x 10^{-3}μΩcm^2. In order to design the appropriate ρ_{con} to be used, it basically comes down to the confidence level in the performance which we able to accept, in another words, it can be interpreted as the yield of the TEC which meets the prescribed requirements. With ρ_{con} decided, the corresponding maximum heat load removable per SiNW (SiNW Q_{max}) can be obtained from a heat load-ρ_{con} graph as in Figure 3.8(a). There have been many proposals of an embedded TEC to address the local heating (hot spot) issues on a microchip [3.9-3.10]. Three critical SiNW TEC parameters are to be designed as follows: optimum number of thermoelectric leg ($No.\ legs_{optimum}$), optimum number of SiNW ($N_{optimum}$), and optimum pitch of SiNW array ($P_{optimum}$). The parameters are obtained with the following equations 3.13 to 3.15.

$$No.legs_{optimum} = \frac{V_{operating}}{V_{optimum}} \text{--- (3.13)}$$

$$N_{optimum} = \frac{Q(W)}{SiNW\ Q_{max}\ (\rho,\rho_{con})(Wcm^{-2})\times Area_{SiNW}(cm^2)} \text{ --- (3.14)}$$

$$P_{optimum}(m) =$$

$$Hotspot\ length\ (m)/\ (\sqrt{\frac{Q(W)}{SiNW\ Q_{max}\ (\rho,\rho_{con})(Wcm^{-2})\times Area_{SiNW}(cm^2)} - 1}) \text{ --- (3.15)}$$

In order to better explain the design methodology, let us consider an embedded TEC operating at 5V (chip operating voltage), and cooling a typical 300Wcm^{-2} hot spot of size 400 x 400µm [3.9]. Using equations 3.13 to 3.15, the design parameters of a SiNW based TEC are calculated and presented in Table 3.3 by considering a 50nm wide, 1µm long SiNW. The design is demonstrated with the selection of three different probabilities corresponding to three different heat flux specifications (Q) that could be generated by hot spots on a microprocessor chip. In all the cases, the number of optimum thermoelectric legs is 72 (not shown explicitly in Table 3.3). As with any engineering design, a general rule of thumb is to over-engineer a device to meet the specifications set; in the case of designing a TEC, the specified heat load Q will always be designed higher than the actual Q handled for real applications.

Table 3.3: Parameters calculation using design methodology described. A chip $V_{operating}$ of 5 V and hot spot size of 400 x 400µm were considered. In all cases, number of thermoelectric leg is fixed at 72 and thus not shown.

Selected Probability	**ρ_{con}-value (µΩcm^2) [Eq. (3.12)]**	**SiNW Q_{max} (Wcm^{-2}) [Fig 3.8]**	**Q (Wcm^{-2}) [as design]**	**$N_{optimum}$ [Eq. (3.14)]**	**$P_{optimum}$ (nm) [Eq. (3.15)]**
0.99	7.86×10^{-2}	4.15×10^{3}	1×10^{2}	1.54×10^{6}	321
			2×10^{2}	3.08×10^{6}	228
			3×10^{2}	4.63×10^{6}	186
0.95	7.32×10^{-2}	4.25×10^{3}	1×10^{2}	1.51×10^{6}	326
			2×10^{2}	3.01×10^{6}	230
			3×10^{2}	4.52×10^{6}	188
0.90	7.05×10^{-2}	4.40×10^{3}	1×10^{2}	1.45×10^{6}	331
			2×10^{2}	2.91×10^{6}	234
			3×10^{2}	4.36×10^{6}	192

3.5 Chapter summary

In this chapter, the performance analysis of a SiNW-based TEC is carried out using FEA software COMSOL Multiphysics. The parameters which impact the TEC performance -- thermal conductivity, length, filling material, and contact resistance -- are systematically studied. The effect of contact resistance on the performance of a SiNW-based TEC is complemented with experimentally extracted values from a SiNW-Al system fabricated using CMOS process. The use of a top-down approach in device fabrication allows for precise control over the SiNW geometry for specific applications. With the study of the different parameters that influence a TEC's performance, a design guideline for a complete SiNW-based TEC for on-chip cooling application is proposed. The issue of hot-spot removal on microchips can definitely be addressed more appropriately with further verification.

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Chapter 4: Development and Fabrication of a Silicon Nanowire Based Thermoelectric Device using CMOS Process

There have been a number of reports praising the merits of individual silicon nanowire (SiNW) as a potential thermoelectric material [4.1-4.2]. At a device level, attempts in fabricating a NW based thermoelectric device (TED) have been reported, but they are limited to single thermoelectric leg form, or incomplete ones using the vapor-liquid-solid (VLS) methods [4.3-4.4]. In this chapter, the development of a fabrication scheme for a complete SiNW-based thermoelectric device (TED) using complementary-metal-oxide-semiconductor (CMOS) compatible process is presented. This includes practical design considerations and the detailed fabrication steps taken. Finally, the problems and issues of the fabrication scheme will be discussed, and the mitigating solutions presented.

4.1 Design considerations of a silicon nanowire based thermoelectric device

Schematically, a SiNW-based TED is as illustrated in Figure 4.1.

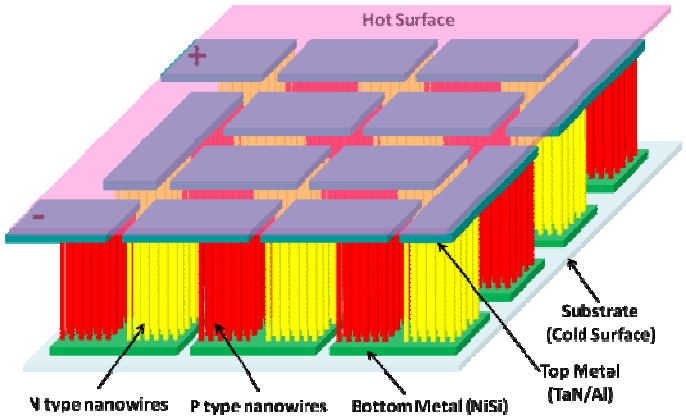


Figure 4.1: Schematic of a SiNW-based TED. The layer responsible for power generation is a composite layer consisting of alternating doped n- and p- type groups of SiNW (active), and a filler material (not visible for clarity) for mechanical support.

From a design perspective, a SiNW-based TED should not differ from that of a conventional one, where alternating n- and p- type thermoelectric legs connected electrically in series is standard [4.5]. However, in place of the usual alternating n- and p- type thermoelectric legs using bulk materials, it comprises of bundles of n- and p- type SiNWs embedded in an electrically non-conducting filler material (not shown in Figure 4.1 for clarity), connected in series in a serpentine fashion through the metal lines. In a SiNW-based TED, a filler material between the SiNW air gaps in the array is essential to support the high aspect ratio structure from a mechanical point of view. The choice of filler material will affect the performance of the final device. As the heat flux needs to be channelled preferentially through the SiNW over the filler material, a filler material of low thermal conductivity, ideally zero as in a vacuum, is desired. The presence of the filler material introduces a parallel heat path which degrades the performance. In the fabrication of a SiNW-based TED using a complete CMOS process, the use of silicon-on-insulator (SOI) as the starting substrate is required as it provides for the

isolation of individual thermocouples which cannot be easily achieved using normal Si wafers. However, it is worth noting that the bottom oxide acts as a parasitic to reduce the temperature gradient that can be applied across the SiNW layer, and will be addressed in Chapter 5. In addition, there are other essential process considerations which will be further discussed in the later sections.

4.2 Fabrication process of a complete silicon nanowire based thermoelectric device

In this section, the fabrication steps of a complete SiNW-based TED using a top down CMOS compatible process will be presented. The integration scheme developed in this work represented the first reported attempt in fabricating a complete and functional SiNW-based TED [4.6-4.7]. Figure 4.2 illustrates the entire process flow of fabricating a SiNW-based TED, as well as accompanying schematic where necessary to represent the outcome at that point. It should be noted that in the schematic, the individual "legs" presented represents bundles of SiNWs. The details of the individual process steps are described in the following sections.

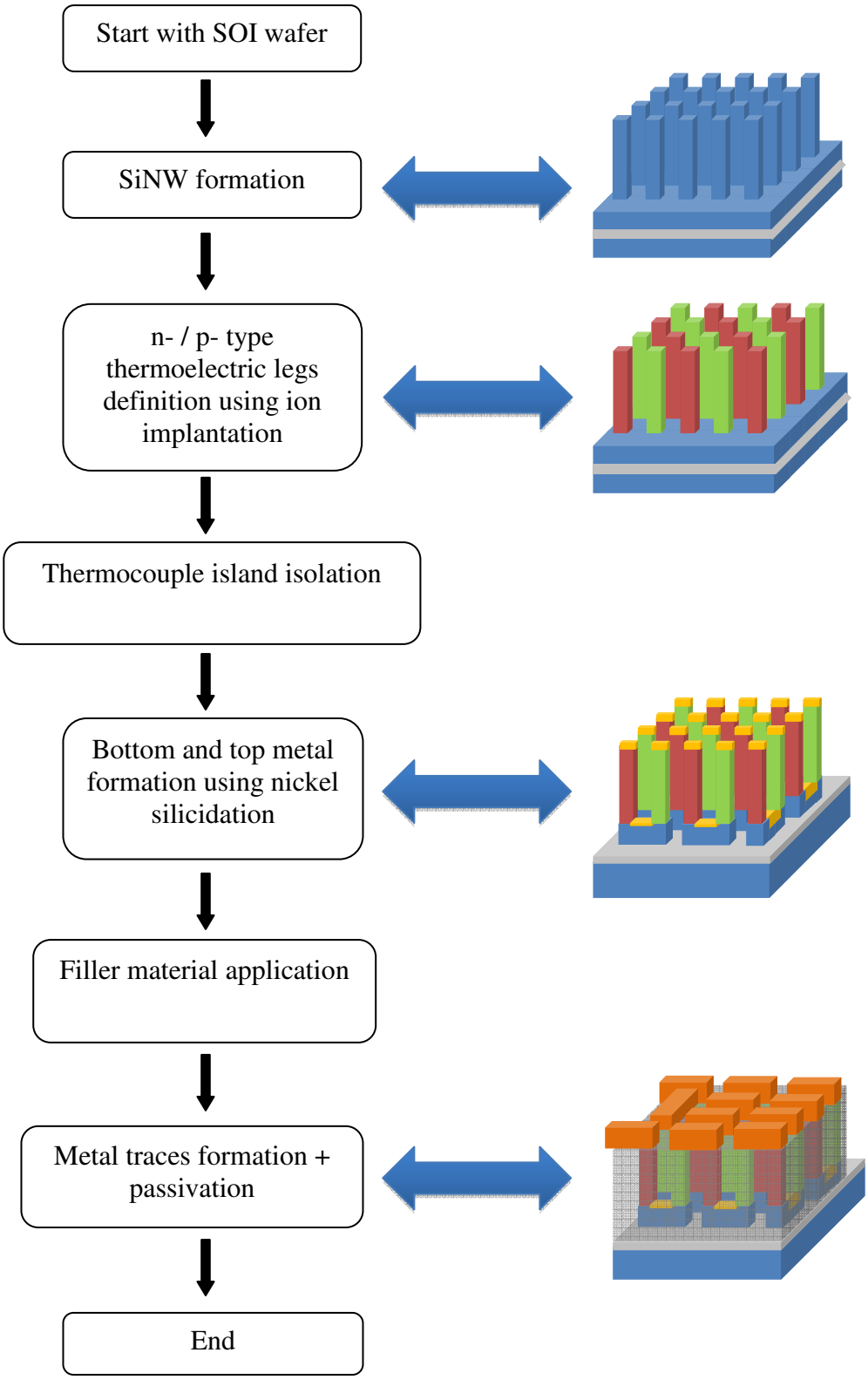


Figure 4.2: Schematic illustrating the entire process flow of fabricating a SiNW based TED

4.2.1 Formation of silicon nanowire array

The fabrication process started with an 8" SOI wafer (p- type, top Si thickness of 2µm and bottom oxide (BOX) of 1µm) as the starting substrate. In the formation of the SiNW array, a top down CMOS method using dry etching, as opposed to the common vapor-liquid-solid (VLS) method [4.8] for SiNW synthesis, was used. The use of this method to obtain lateral or vertical SiNWs has been widely reported for fabricating SiNW transistors, and offers great control in the size and position of the SiNW [4.9-4.10]. To form the SiNW, a deep ultraviolet (DUV) lithography process was first used to pattern an array of nano-dot on designed locations on the SOI wafer surface. The limitations of the DUV lithography technology allowed for a minimum pitch size of 400nm of the nano-dot array. Due to the small pitch, a bottom anti reflection coating (BARC) layer was applied before the coating of a positive photoresist prior to exposure. Figure 4.3(a) and (b) shows top-view scanning electron microscope (SEM) images of the patterned nano-dot array of pitch 400 nm at different magnifications while (c) shows an SEM image of the nano-dot at 45^{o} tilt angle

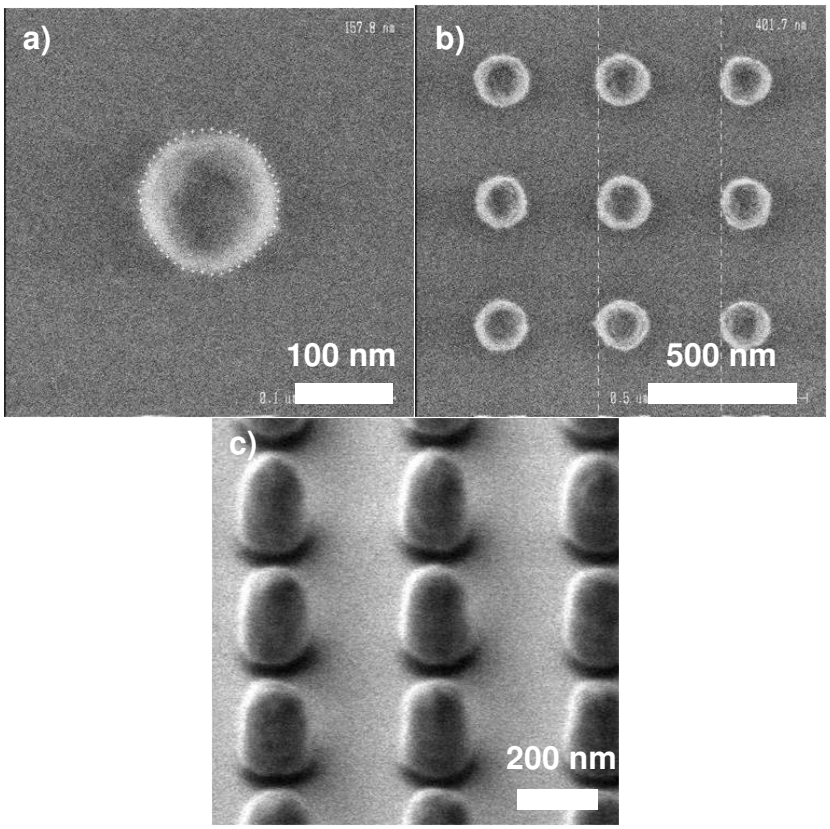


Figure 4.3: (a) and (b) shows the top view SEM images of the patterned nano-dot array of pitch 400 nm at different magnifications while (c) shows the SEM image of the nano-dot tilted at 45^{o}.

From the SEM images, the diameters of the nano-dot were measured to be ~150 nm and will be further trimmed (to 80nm) in subsequent process. It should be noted that the limitations of the DUV lithography is on the pitch of the nano-dot array and not on the individual nano-dot size. The size of the nano-dot affects the final SiNW size and can be controlled in 2 ways: (i) by varying the exposure dose during lithography, (ii) using a photoresist trimming process after lithography. The photoresist trimming method is preferred due to the more precise control it has on the final nano-dot diameter. The photoresist trimming process is critical in ensuring there is minimum photoresist loss vertically as this will impact the length

of the final SiNW attainable. As the SiNW was formed with the photoresist acting as a hardmask, the smaller the photoresist thickness, the shorter the final length of the SiNW that can be obtained. The photoresist trimming process was done using a timed etch using oxygen (O_2) plasma. It was crucial that the etch rate of the photoresist be kept low ~1nm/s in order to precisely control the diameter of the final nano-dot. Figure 4.4 shows the SEM images of the nano-dot after the trimming process. It can be observed that the diameter of the nano-dot has been reduced from ~150 nm to ~80 nm.

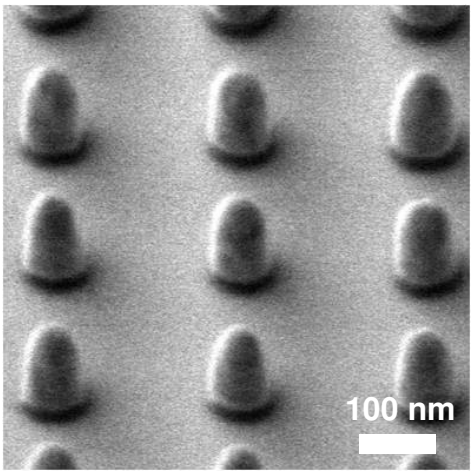


Figure 4.4: SEM images of the nano-dot after photoresist trimming process. The diameter of the nano-dot has been reduced from 150nm to 80nm

After the trimming process, a dry etching process was carried out to form the SiNW array. Etching of Si can be done conventionally using purely SF_6 as the etchant gas. However, for etching of high aspect ratio Si structure such as SiNW, this will result in sidewall tapering. Hence, an etching process modified from the well-known Bosch process for etching high aspect ratio structures is used to form

the SiNW [4.11]. In this etching process, two etchant gases, SF_6 and CF_4 were introduced at alternate intervals to the chamber. The role of SF_6 is mainly used for etching while CF_4 is used for sidewall passivation. During the passivation process, a layer of fluorocarbon compound is introduced to the side wall of the SiNW to protect it against further etching at the next etching cycle. Schematically, this etching method is illustrated in Figure 4.5.

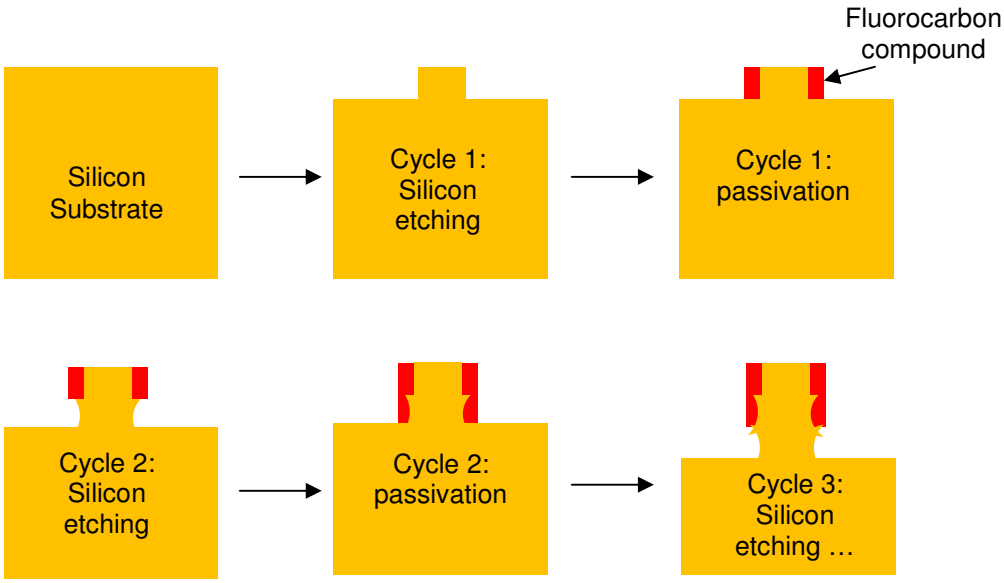


Figure 4.5: Schematic illustrating the etching process used to form the SiNW array. The etching process of the different cycles are indicated.

Since the nano-dot photoresist is used as a hard mask, the final length of the SiNW is dependent on the initial thickness of the photoresist, and the selectivity ratio of photoresist to Si. With a nano-dot photoresist thickness of ~2300Å, a maximum SiNW length of ~1.5µm can be obtained. Figure 4.6(a) to (c) show the SEM images of the SiNW etched to different lengths to illustrate the modified Bosch process, as well as the photoresist/Si selectivity ratio. It can be observed

that the etching process was effective in forming SiNW with a straight profile, with a maximum length of ~1.5 µm achievable (photoresist was almost depleted). The magnification of the images is presented such that the whole length of the SiNW can be clearly seen. Corresponding Figure 4.6(d) to (f) show the SEM images of the SiNW array after stripping off the photoresist after etching.

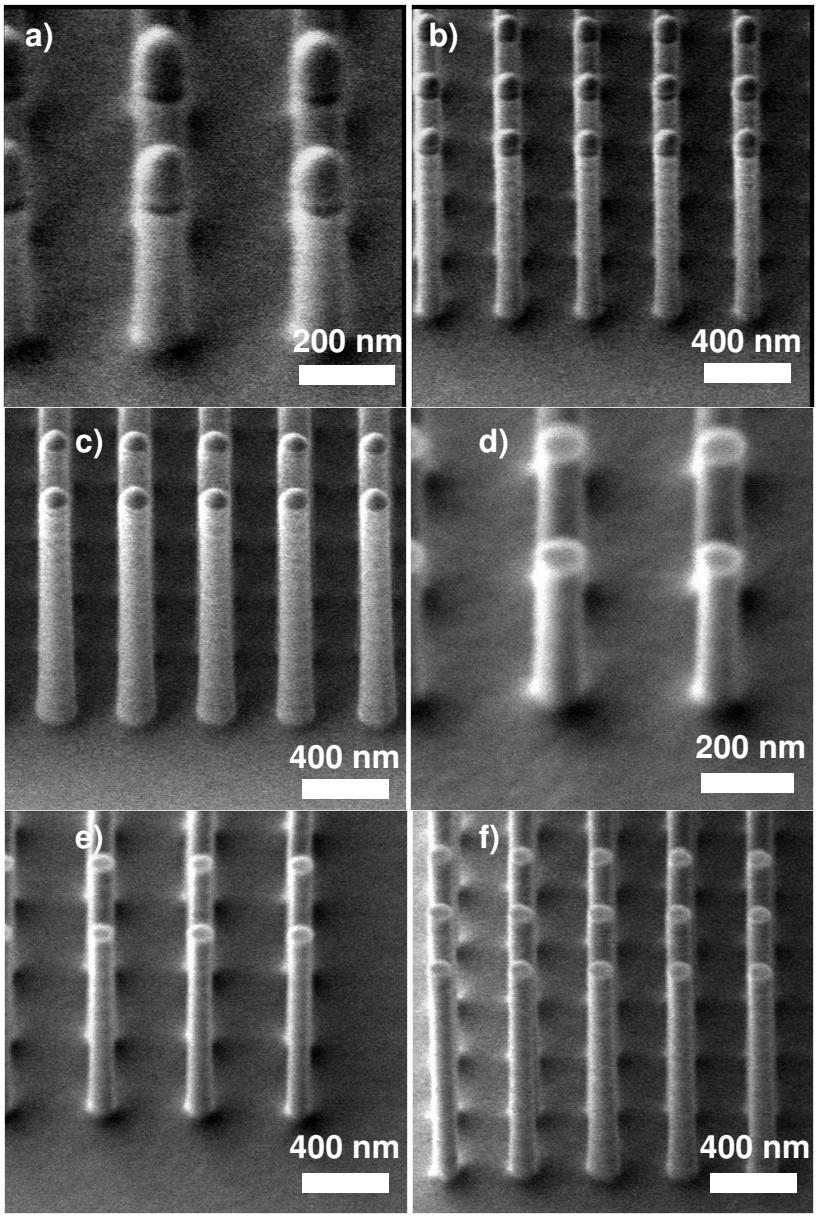


Figure 4.6: (a) to (c) show the SEM images of the SiNW etched with different lengths. It can be seen that at the maximum length achievable of ~1.5µm, the photoresist at the tip of the SiNW is almost depleted. (d) to (f) shows the corresponding SEM images of the SiNW array after stripping of the photoresist after etching. The magnification of the images is presented such that the whole length of the SiNW can be clearly seen.

It is worth pointing out that further reduction to the SiNW diameter after the etching process can be accomplished using a combination of thermal oxidation process followed by a isotropic oxide etch using hydrofluoric acid (HF).

4.2.2 Defining n- and p- type thermoelectric legs of a thermoelectric device

A complete TED consists of alternating n- and p- type thermoelectric legs. In a SiNW-based TED, each n- and p- type thermoelectric leg is made up of bundles of SiNWs. With the CMOS process used in the fabrication, the doping of specific groups of SiNW can be achieved easily by using a combination of lithography prior to a doping process. In the doping process, ion implantation is the preferred method as it provided good control in the resulting doping level in other SiNW-based devices [4.9]. The doping process is as follows: in order to define the n- type thermoelectric legs, the locations of all the p- type thermoelectric legs were masked off using photoresist while the locations to be implanted n- type were exposed; similarly, the process was repeated to define the p- type thermoelectric legs. Figure 4.7 shows the schematic and a optical micrograph where the n- type thermoelectric legs are covered in photoresist, leaving the areas to the implanted p- type exposed.

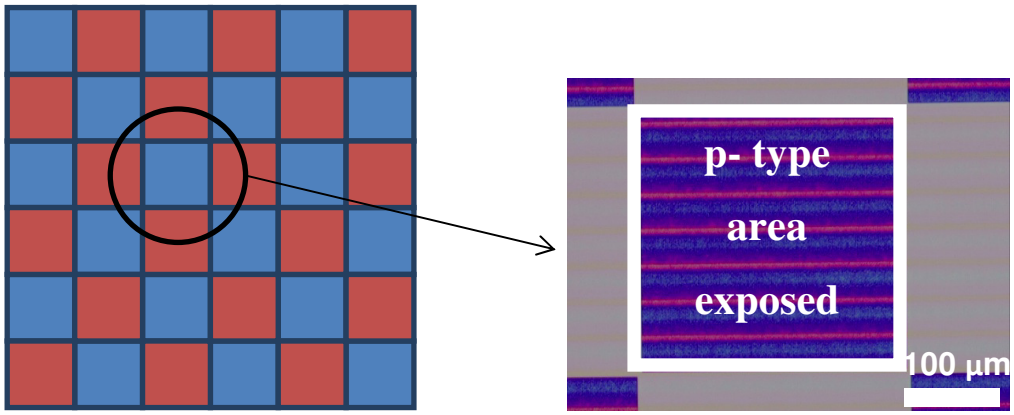


Figure 4.7: Schematic and optical micrograph where the n- type thermoelectric legs are covered in photoresist, leaving the areas to be implanted p- type exposed.

Prior to the ion implantation process, the 2D simulation software – Synopsys TSUPREM4 was used to determine the conditions required to achieve a uniform doping of > $10^{19}cm^{-3}$ [4.1] throughout the length of the SiNW. In particular, the ion implantation and annealing conditions were desired. The use of simulation prior to actual implementation allowed us to optimize the conditions and provided an overview of the final results (Figure 4.8).

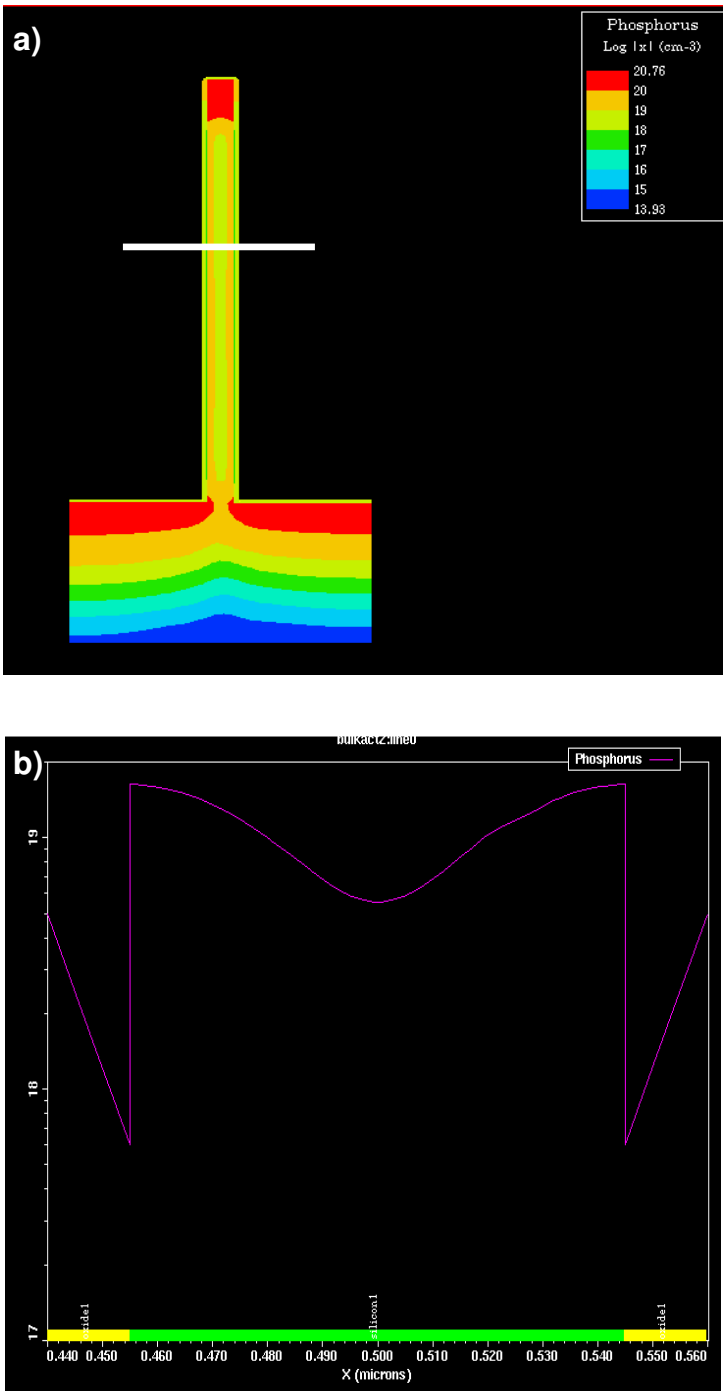


Figure 4.8: a) Simulation profile of the doping concentration in SiNW after optimized ion implantation and annealing, and b) cut-line (indicated) of the doping concentration

From the simulation, the chosen conditions for achieving $>10^{19}cm^{-3}$ throughout the SiNW length are:

Implantation species – BF_2 and Phosporus for p- and n- type respectively

Implantation Dose – 1 x 10^{-14} cm^{-2}, 7^o tilt for 4 directions (rotate 4 x 90^o)

Implantation Energy – 35 keV and 40 keV for BF_2 and Phosporus respectively

Annealing condition – 1050^oC, 30s, N_2 ambient

Each n- and p- type thermoelectric leg is 250 µm × 250 µm and consists of 540 x 540 SiNWs. After the implantation and annealing process, thermocouples (consisting of a pair of n- and p- type thermoelectric legs) were formed by etching selective areas of the SiNW array. In Figure 4.9, the SEM image shows the formation of the thermocouple; the dark area is the location where excess Si has been removed. The residues seen are from the photoresist after the O_2 plasma process which will be completely removed by dipping in a Piranha solution thereafter. From this step, the essential use of SOI wafer for the fabrication can be seen. Without an insulation layer between the SiNW array and substrate, it would not be possible to form islands of isolated thermocouples.

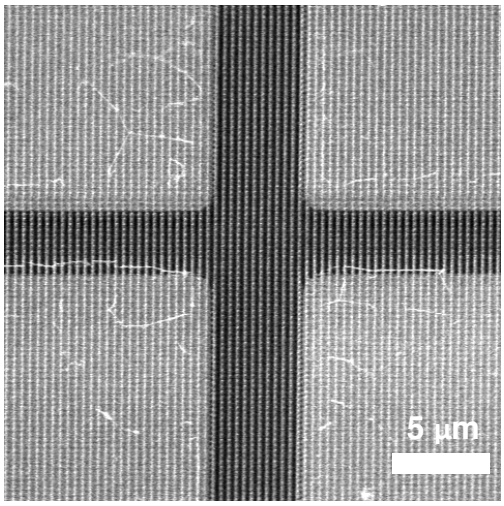
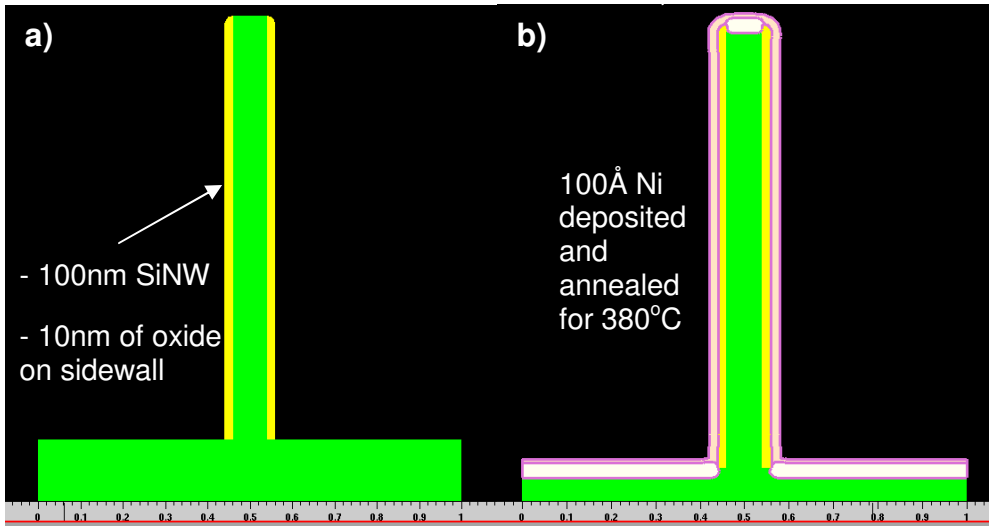


Figure 4.9: SEM image showing the formation of the thermocouple; the dark area is the location where excess Si has been removed. The residues seen are from the photoresist after the O_2 plasma process which will be completely removed by dipping in a piranha solution thereafter.

4.2.3 Nickel Silicidation

A TED is usually formed with its thermoelectric material contacted at both ends by metal electrodes [4.6]. A conventional TED is assembled by bonding the thermoelectric material with the metal traces using a pick-and-place method [4.12]. However, when it comes to using SiNW with our fabrication approach, the pick-and-place method proved to be impractical. In place of it, the popular salicide process commonly used in transistors will be used instead to form both the top and bottom electrodes simultaneously. It is critical that the metal silicide is formed selectively on the top and bottom of the SiNW so as to ensure the length of the thermoelectric material is maintained; the length/thickness of the thermoelectric materials defines the performance of the TED. This Ni silicide process was achieved by first forming an oxide spacer at the sidewalls of the

SiNW via thermal oxidation and an anisotropic oxide etch. Subsequently, a silicide metal – nickel (Ni) was deposited and annealed. Prior to the process, a 2-D process simulation using Synopsys TSUPREM4 was carried out. The process is as described – a thermal oxidation of 100Å was carried out on the SiNW, followed by an anisotropic oxide etch to remove the tip and bottom surface oxide such that only a sidewall spacer is left on the SiNW. Thereafter, 100Å of Ni was deposited and annealed for a predetermined amount of time and temperature. We simulated several annealing conditions to get the desired final profile of the Ni silicide. Figure 4.10(a) shows the simulation model after spacer formation while Figure 4.10(b) to (d) show the Ni silicide profile after annealing conditions of 380^{o}C, 400^{o}C and 420^{o}C for 30s, respectively.



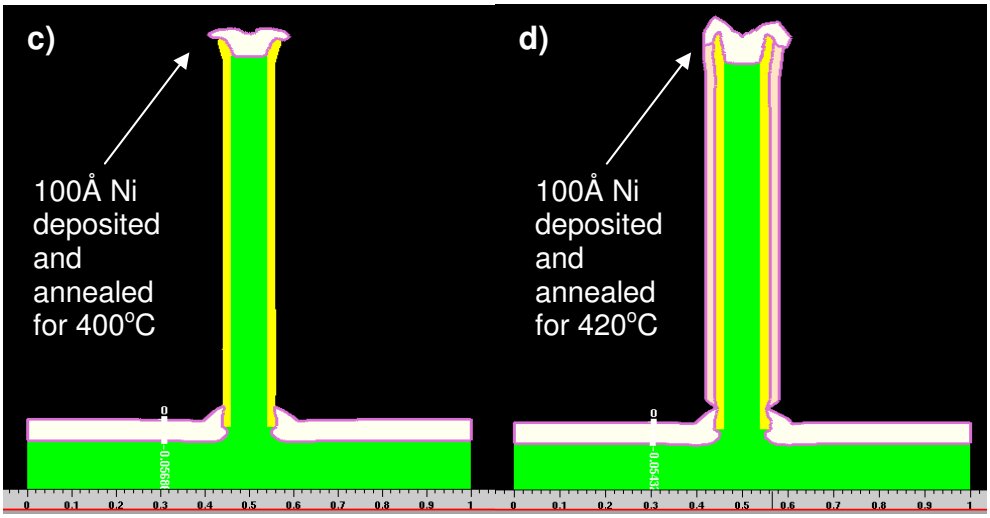


Figure 4.10: TSUPREM4 model of SiNW after a) spacer formation, Ni silicide profile after annealing for b) 380°C, c) 400°C, and d) 420°C for 30 s

In the actual process, annealing condition of 400°C for 30s was chosen due to the desired profile as obtained from the process simulation; A Ni silicide intrusion depth of ~100nm was desired to provide sufficient area of contact to the top metal while not reducing the SiNW length significantly. After the formation of the Ni silicide, unreacted Ni was removed selectively by immersing the wafer in a heated Piranha (H_2SO_4:H_2O_2) solution at 130°C for 5mins. Figure 4.11 shows the SEM images of the SiNW array after a) silicidation process, and b) selective removal of unreacted Ni.

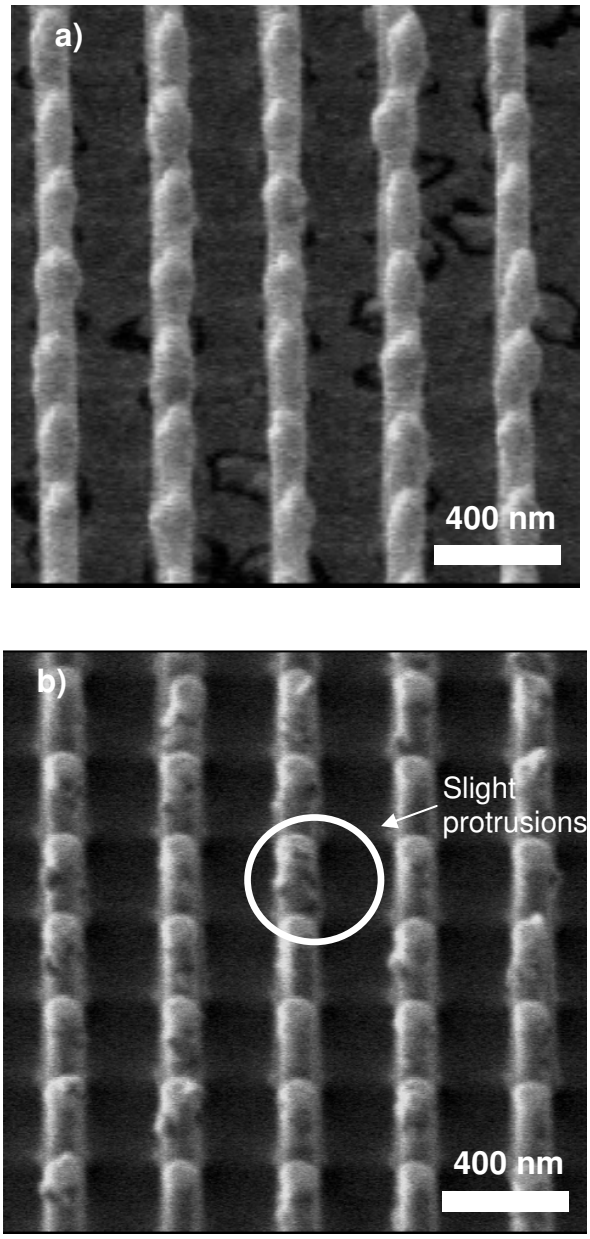


Figure 4.11: SEM images of the SiNW array after a) silicidation process, and b) selective removal of unreacted Ni.

Visually inspecting the SEM image of the SiNW after selective removal of Ni, it was observed that there is slight protrusion of Ni silicide near the tip area, which was similar to the results obtained from the simulation.

4.2.4 Filler material application

The high aspect ratio of the SiNW calls for the use of a supporting material against mechanical damage. The formation of a nanowires composite layer using VLS grown SiNW and paralyne as a filler material has been demonstrated [4.3]. The selection of the filler material requires the capability to fill in between the gaps of densely packed SiNW array while possessing a thermal conductivity value as low as possible. The second aspect of the material having a low thermal conductivity determines the overall thermal conductance of the composite layer which will be further discussed in Chapter 5. In our fabrication process, we have attempted the filling of the SiNW array using oxide (SiO_2) and polyimide; the use of both materials has its own pros and cons.

Oxide as filler material

The choice of SiO_2 as the filler material was natural considering it being a highly compatible CMOS material. It is widely used in the industry, and has a thermal conductivity value (1.4 W/mK) which is comparable to the best SiNW reported [4.1]. In the fabrication, the SiO_2 was deposited using high density plasma (HDP) chemical vapor deposition (CVD) method. Conventional CVD SiO_2 did not fill the gaps well, and created voids after an etchback of the SiO_2 was done to expose the SiNW tips as shown in Figure 4.12.

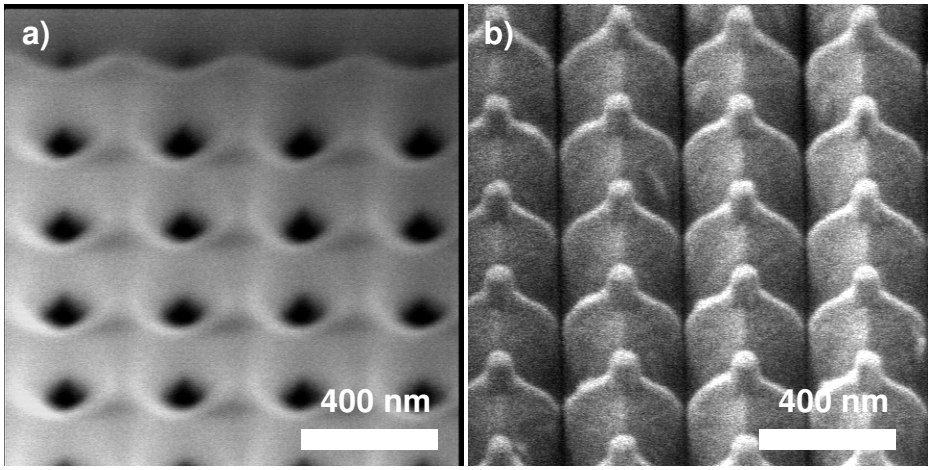


Figure 4.12: SEM images of the SiNW after SiO_2 filling using CVD and SiO_2 etchback a) before SiNW tips were exposed, and b) after SiNW tips have been exposed

The air gaps seen in figure 4.12 is undesirable as it reduces the mechanical integrity of the SiNW array, as well as being incapable of allowing the final top metal traces to be formed only at the tips. For the HDP CVD SiO_2 deposition process, it involved repeated cycles of etching and deposition of SiO_2; this allowed much better filling of SiO_2 in the SiNW array. Figure 4.13 shows the SEM image of the SiNW tips exposed after a HDP SiO_2 etchback process; the etchback process is the same one used for Figure 4.12 (b).

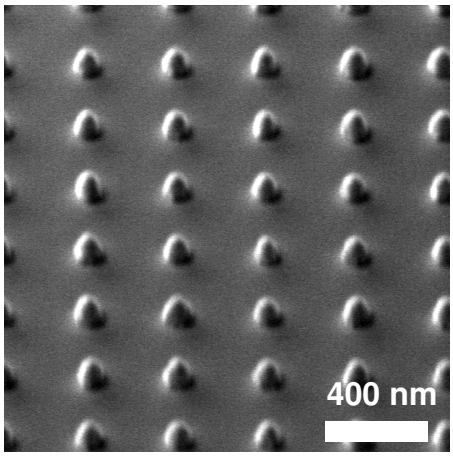


Figure 4.13: SEM images of the SiNW after HDP SiO_2 etchback to expose the SiNW tips. No gaps between the SiNW can be seen

It can be seen in Figure 4.13 that the use of HDP SiO_2 makes a huge difference compared to that shown in Figure 4.12 where conventional CVD SiO_2 was used. No gaps were observed and such a structure allows for the top metal traces to form only at the SiNW tips as desired.

Polyimide as filler material

Polyimide has several advantages over SiO_2 of which the most notable is its lower thermal conductivity. In choosing a suitable polyimide, the viscosity is paramount in ensuring the proper filling in between the gaps of the SiNW. In our process, the polyimide - PI2562 from HD Microsystems was used. PI2562 has a rated thermal conductivity of 0.14W/mK (1 order lower than SiO_2), as well as the lowest rated viscosity (max 2 poise) as compared to the available polyimide available in the market and thus was the natural choice to ensure good filling. The

polyimide was applied via a spin coating process and cured at 380^{o}C for 30 mins in ambient N_2. During the polyimide etch back to expose the SiNW tips, O_2 plasma etching was used and the SEM image after the SiNW tips were exposed is shown in Figure 4.14.

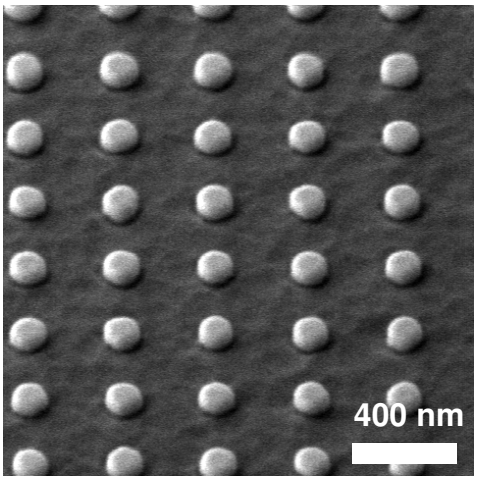


Figure 4.14: SEM images of the SiNW after polyimide etchback using O_2 plasma.

It can be observed from Figure 4.14 that the polyimide filled the gap very well; no voids can be observed. In addition, the SiNW tips have a larger surface area compared to Figure 4.12 where the tips are more pointed. However, the disadvantage of using polyimide as the filler material is that it is not a proper CMOS material. Such a material is used commonly in the backend process to passivate devices at the final step.

After the application of the filler material, the final metallization of the SiNW-based TED was done by aluminum (Al) sputtering followed by an Al etching process to define the metal traces of the device. A final passivation layer by Si_3N_4 deposition completed the TED fabrication; the passivation layer was

necessary for device level characterization to avoid electrical shorting between the thermoelectric legs. A photo of the completed SiNW-based TED is as shown in Figure 4.15. It should be noted that visually, there was no difference between that of SiO_2 and polyimide as the filler material. The completed device had a NW array size of 5mm x 5mm (60% was occupied by the n- and p- doped SiNW array), and consisted of 162 thermocouples. The SiNW in the array had a length of ~1.1µm and diameter of ~80nm.

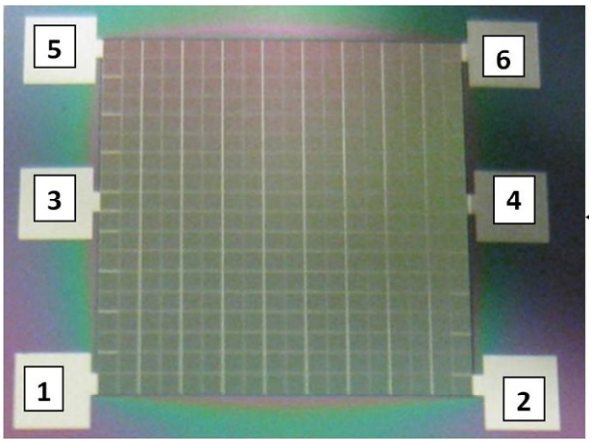


Figure 4.15: A photo image of the completed TED, where it consisted of 18 x 18 thermoelectric legs, and the SiNW array covering an area of 5 mm x 5 mm.The NW in the array had a length of ~1.1 µm and diameter of ~80 nm.

In the design, 6 metal pads were placed at the peripheral of the SiNW-based TED as shown in Figure 4.15. These 6 pads are placed to facilitate powering up different sections of the TED, and to ensure all the thermoelectric legs are connected in the correct manner.

4.3 Problems encountered in the fabrication process

The fabrication of a SiNW-based TED using CMOS compatible process appeared to be straightforward. However, it is worth pointing out that there are a number of limitations. The thickness of a thermoelectric material will affect the device's performance in both power generation mode or in cooling mode [4.13]. One of the limitations encountered in the fabrication process is the ability to form long SiNWs; in the power generation mode, a thick thermoelectric material is desired to sustain a larger temperature gradient, and thus a larger power output. It was presented earlier that the formation of the SiNW array made use of photoresist as the hard mask during the Si etching process. With a maximum thickness of photoresist applied of 2500Å, the longest length of the SiNW achievable is at most 1.5μm. This implies a selectivity ratio of the photoresist and Si of 1:6. Etching beyond this will result in the tips of the SiNW being etched. Figure 4.16(a) and (b) shows respectively the SEM images of the photoresist almost depleting on the SiNW, and etching of the tips once the photoresist has been completely etched off. Owing to the limitations of the DUV lithography process, it was not possible to apply a thicker photoresist to increase the SiNW final length, nor decrease the pitch of the SiNW array.

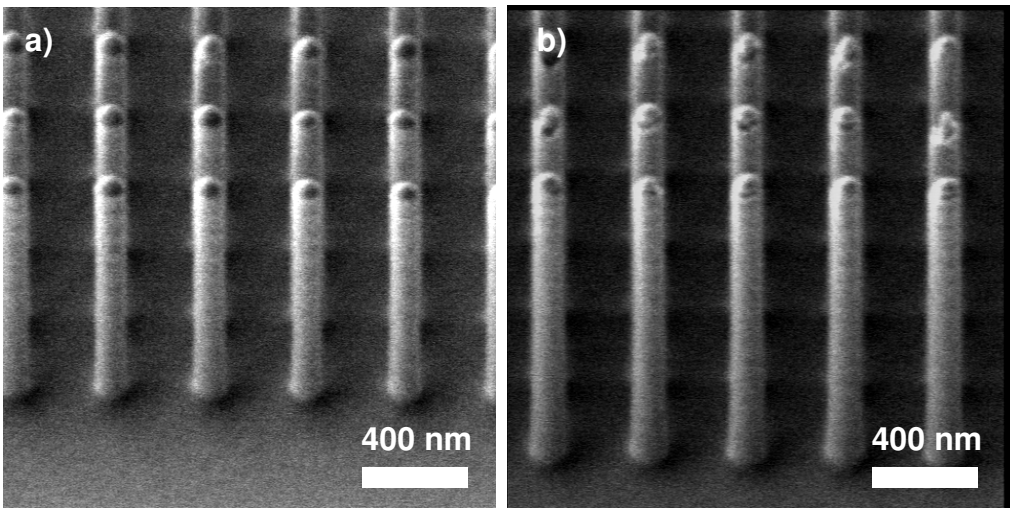


Figure 4.16: SEM images of (a) the photo photoresist almost depleted on the SiNW, and (b) etching of the tips occurred once the photo photoresist is completely depleted.

Nevertheless, the benefits of a longer SiNW in enhancing the performance of a TED cannot be ignored. Although the methods of synthesizing long SiNW using VLS and electroless etching method have been reported in literature, they do not possess the advantage of being CMOS process compatible nor the precision required to assemble a complete device. Instead, lithography technology beyond DUV such as extreme ultraviolet (EUV) or electron beam lithography (EBL) with higher resolution could be a key in bringing the SiNW-based TED technology further [4.14-4.15].

4.4 Chapter summary

In this chapter, we have presented the fabrication of a SiNW-based TED using top down CMOS process. In the design, the same structure as a

conventional bulk material based TED was used but with the thermoelectric legs comprising bundles of SiNW instead. The fabrication of a SiNW-based TED required the use of SOI wafer; this was necessary to isolate individual thermocouples from one another, which would otherwise be shorted if a normal Si wafer was use. Owing to the mechanical weakness of a high aspect ratio structure, two different filler materials – SiO_2 and polyimide - were explored in filling up the air gaps of the SiNW array. In addition, whilst during fabrication, process simulation for SiNW doping (to 1 x 10^{-19} cm^{-3}), and Ni silicidation were carried out to optimize the condition to be used. SEM images at different stages of the fabrication were obtained to confirm the structure of the device. Finally, problems encountered in the fabrication were discussed and mitigating solutions proposed.

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Chapter 5: Characterization of a Silicon Nanowire Based Thermoelectric Device

In this chapter, the techniques used to characterize a silicon nanowire (SiNW) based thermoelectric device (TED) will be discussed. The characterization includes a study at a micro level (individual SiNW) perspective as well as from a macro (device) level perspective. The experimental setup at the micro/macro level will first be presented, followed by the characterization methodology. Finally, the results obtained will be discussed and benchmarked against the state-of–the-art TED.

5.1 Micro-level characterization (Individual silicon nanowire)

5.1.1 Experimental setup

There are several possible ways to measure thermal conductivity, each of them suitable for a limited range of materials and geometries, depending on the thermal properties and the medium temperature. Most thermal conductivity measurement techniques for bulk materials are based on creating a temperature gradient along the sample and monitoring the temperature by thermocouples situated at different locations. Without going into the details, some of the common methods of measuring thermal conductivities of materials are as follows:

1. Measuring either total direct current (d.c.) power or total alternating current (a.c.) power applied at one end, the thermal conductivity can be determined [5.1].

2. Placing the sample between standard materials with known thermal conductivities so that by comparing the temperature gradient, the sample thermal conductivity can be derived [5.2].

3. Time-domain thermo-reflectance method to analyze heat flow in materials [5.3].

4. Thermal bridge approach where the sample is suspended between a MEMS-based heater and sensor islands that incorporate platinum (Pt) serpentine loops for heating and thermometry [5.4].

In this thesis, the last approach is used for measuring the thermal conductivity of the SiNW, being the most suitable technique for nanowires. This method of measuring nanowire (nanotube) thermal conductivity was developed and reported by Shi *et al*. in 2003 [5.4]. It has several advantages such as being straightforward in its measurement principle and accuracy. However, the difficulty of using this method lies in bridging the nanostructures across the heater & sensor islands. Nevertheless, this method has been successfully used to study the thermal properties of nanostructures [5.4-5.6].

The micro-electrothermal system (METS) device was fabricated on a Si wafer with 3000 Å of low stress Si_3N_4 deposited on top using low pressure chemical vapor deposition (LPCVD). A lithography process followed by a SiN etch process were used to define the heater, sensor and the electrode sections.

Thereafter, using electron beam evaporation to deposit a 2000Å layer of Pt and a lift-off process, the heater and sensor in the form of serpentine lines were formed. Finally, a backside potassium hydroxide (KOH) etch was used to release the structure from the bottom Si substrate. The purpose of suspending the structure was to eliminate any thermal loss through the Si substrate during characterization which would otherwise degrade the accuracy of the measurement. Figure 5.1(a) to (d) show the schematics of the micro device fabrication, and (e) shows the scanning electron microscope (SEM) image taken of the completed device.

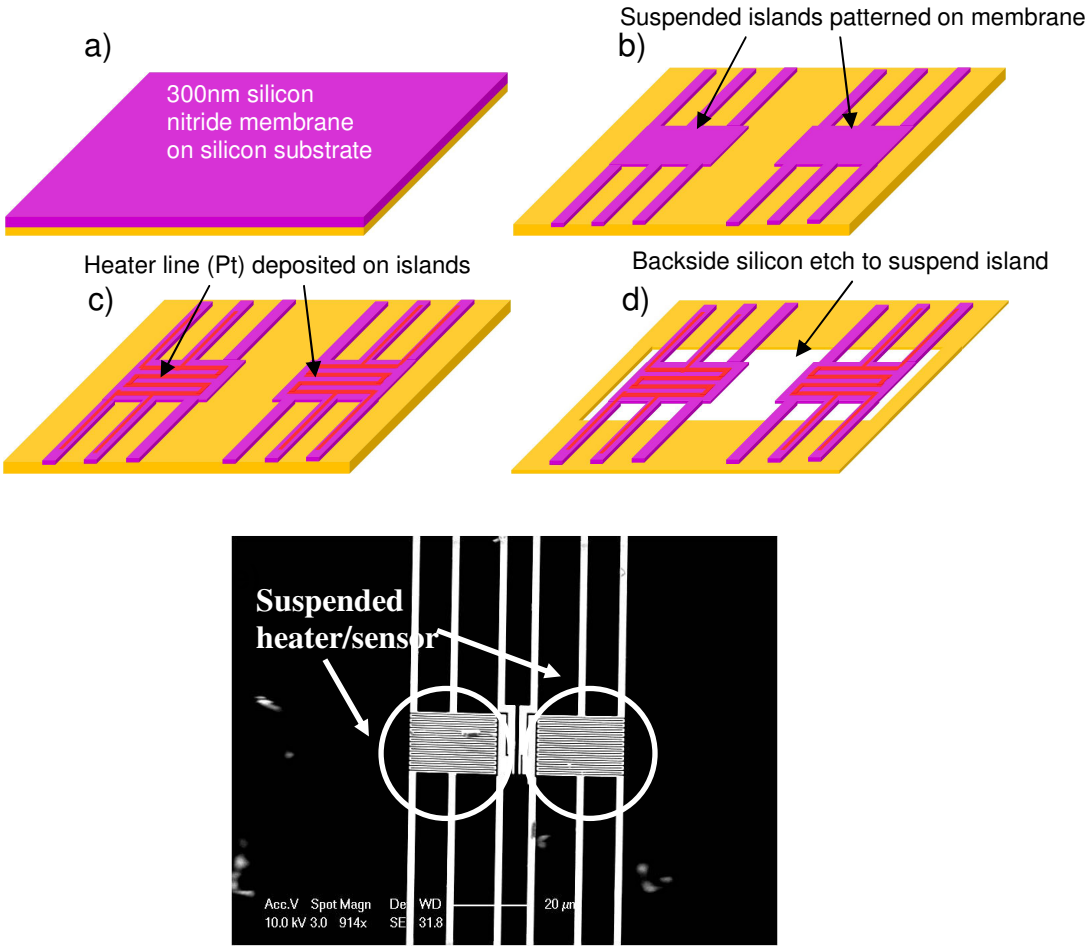


Figure 5.1: (a) to (d) show the schematics of the micro device fabrication with process details indicated, and (e) shows the SEM image taken of the completed device

5.1.2 Individual silicon nanowire sample preparation

In the reported literature of SiNW thermal properties, the SiNW was usually obtained using the vapor liquid solid (VLS) method. However, the same SiNW in the fabricated TED be measured for its thermal conductivity was desired instead of similar dimensions SiNW obtained separately. The fabrication scheme involved the simultaneous nickel (Ni) silicidation of the top and bottom of the SiNW. Making use of the fact that Ni silicide is readily etched by hydrofluoric acid (HF), we first severed the individual SiNW from the substrate by dipping a SiNW-based TED sample into a beaker of HF for 5 mins, following by drying the sample using nitrogen (N_2). Figure 5.2 shows the SEM image taken of n- type SiNW detached from the substrate.

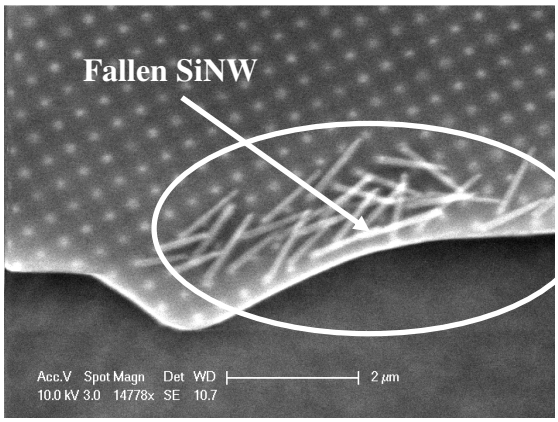


Figure 5.2: SEM image of SiNW fallen onto the substrate after dipping in hydrofluoric acid

From Figure 5.2, it can be seen that a bunch of SiNWs were lying on the substrate after the DHF process. It indicates that the Ni silicide has been etched which

resulted in them detaching from the surface. It was not possible to observe the entire array of SiNW on the substrate as most would have been "lifted" away from the substrate by the wet process.

To place the SiNW on the METS device for thermal measurements, a nano manipulation approach was used. In this approach, a sharp tungsten probe tip (electrochemically etched using KOH) was used to pick up the SiNW while being controlled by a manipulator system (Kleindiek MM3A-EM). The SiNW picked up by the tungsten probe was then transferred to the METS device and bridged between the two electrodes of heater and sensor. The pick-and-place method was performed in a SEM (Philips XL30 FEG) so as to facilitate the clear observations of the SiNW throughout the process. Figure 5.3 shows SEM images during (a) picking up of SiNW using the tungsten probe, (b) successfully placing the SiNW on the microdevice, and c) a close up view of the SiNW successfully placed.

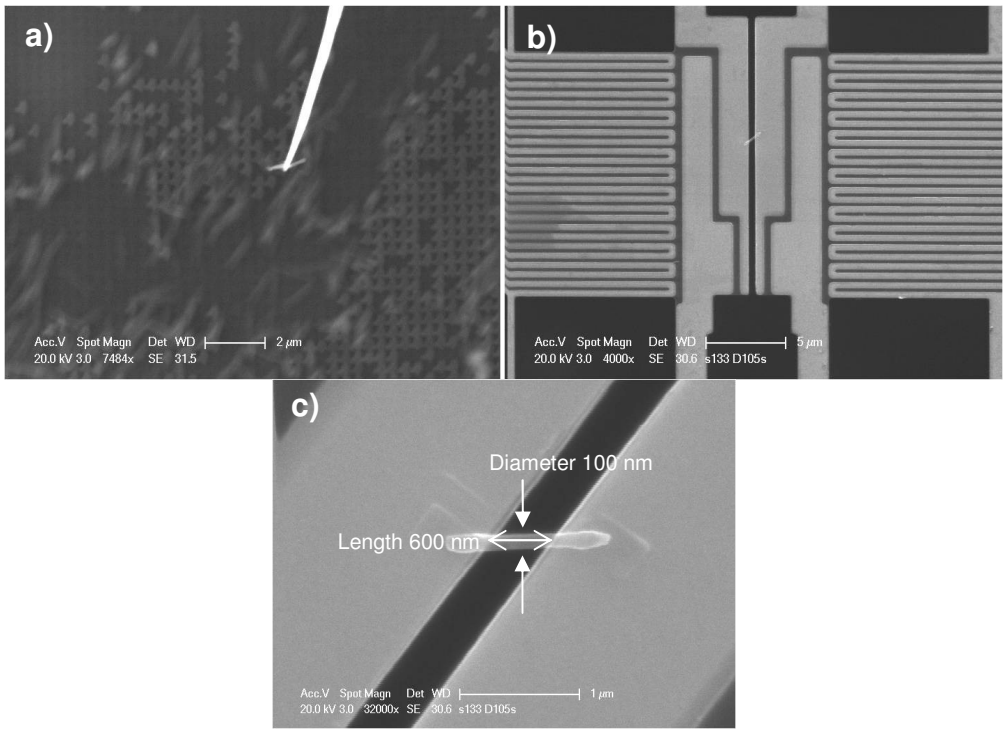


Figure 5.3: (a) Picking up of SiNW using the tungsten probe, (b) successfully placing the SiNW on the microdevice, and c) a close up view of the SiNW successfully placed.

Although the drop-cast method [5.4] can als be used to place the SiNW, the manipulation method was used due to the accuracy in placing the SiNW at the desired location.

5.1.3 Concepts of thermal conductivity measurements

After placement of the SiNW samples, the device was placed in a vacuum chamber with a cryogenic stage attached. Using this setup, the variation of the thermal conductivity with temperature can be measured. In the measurement, three lock-in amplifiers (SR380) and two a.c. & d.c. current sources (Keithley

6221) were connected to the METS device via vacuum electrical feed-through. In order to accurately measure the temperatures, the Pt serpentines were pre-calibrated for their temperature coefficient resistance (TCR) by using a temperature controlled chamber and obtaining a resistance *versus* temperature graph. Figure 5.4 illustrates the schematic of the METS device with the concept of the thermal conductivity measurements explained thereafter [5.4].

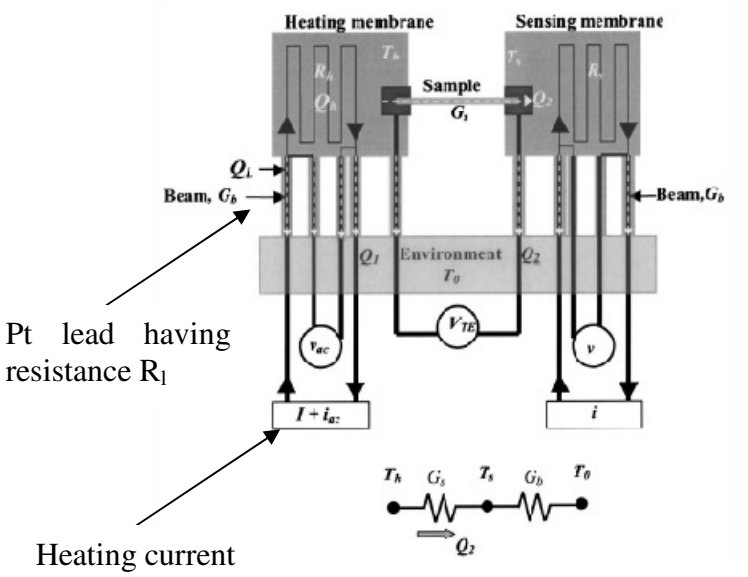


Figure 5.4: Schematic for measurement of thermal conductivity [5.4]

As the current passes through the Pt heater, a joule heat of $Q_h = I^2R_h$ is generated with the Pt heater having a resistance of R_h. The two leads of resistance R_l each on the connecting beams dissipate a total heat of $Q_l = 2I^2R_l$. It was claimed that below 400 K, the radiation losses from the membrane and the five supporting beams to the environment are negligible compared to conduction heat transfer

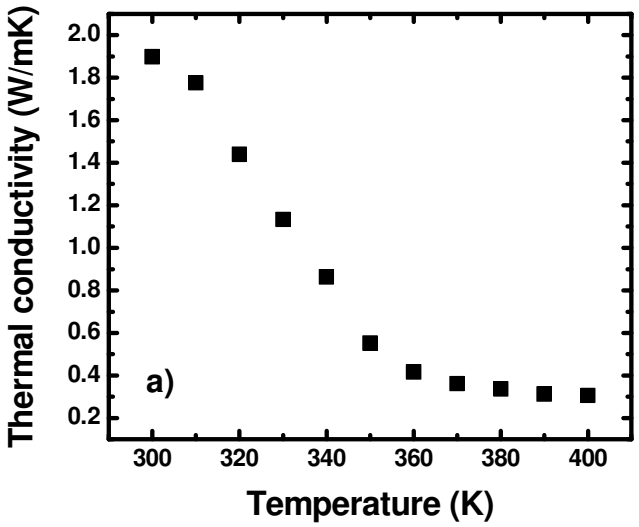
through the five beams; air conduction losses are negligible in vacuum With the knowledge of the total thermal conductance of the five SiN beams to be $G_b = 5\kappa A/L$, where A and L are the area and length of the beams respectively, the beams' thermal conductivity κ_n can be obtained with equation 5.1.

$$\kappa_n = \frac{G_s l_n}{A_n} \quad \text{--- (5.1)}$$

In addition to using both the Pt heater for measurements, another technique that uses the electron beam of the SEM to locally heat up a point on the SiNW sample on METS device was developed by our group [5.7]. This technique makes use of the electron beam to heat up one point of the SiNW while measuring the temperature changes at both ends using the Pt sensors. By doing so, the spatially resolved distribution of thermal resistance along the SiNW can be obtained. However, using this technique, only measurements at room temperature can be performed due to specimen image drift encountered whenever the temperature controlled stage was used. More details on the measurement concepts are described in [5.7]. It is worth pointing out that the thermal conductance measured using this technique has the advantage of decoupling the thermal contacts of the SiNW and the electrodes, and the SiNW itself.

5.1.4 Thermal conductance measurements of silicon nanowire

The thermal conductance of the SiNW was first obtained with varying temperatures. Subsequently, the e-beam technique was used to resolve the intrinsic thermal conductance of the SiNW. In Figure 5.5, we show the results of (a) the temperature dependent thermal conductivity of the SiNW (based on measured dimensions of length – ~600nm and diameter – ~100nm shown in Figure 5.3(c)), while (b) shows the cumulative thermal resistance of the SiNW along its length resolved using the electron beam technique at room temperature. It is worth noting that in order to account for any possible radiation loss across the gap, we also measured the thermal conductance of the same METS device without any SiNW bridging across.



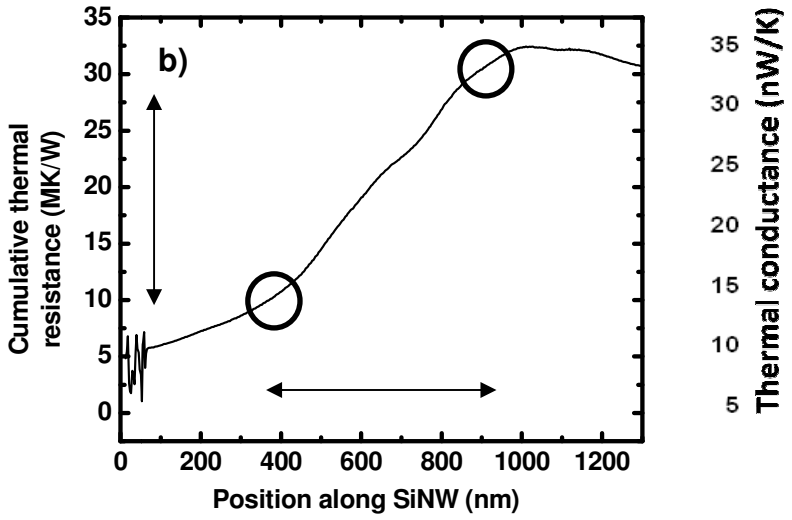


Figure 5.5: a) the temperature dependence thermal conductance of the SiNW, b) cumulative thermal resistance of the SiNW along its length resolved using the electron beam technique at room temperature

In Figure 5.5(a), the thermal conductance is inclusive of the contributions from the SiNW, the thermal contacts at the two ends to the electrodes, as well as from possible radiation across the gap. In Figure 5.5(b), the thermal resistance contribution is solely from the SiNW. Separately, the radiation loss of the METS device was measured to be ~0.8 nW/K at room temperature, which is ~2.5% that of Figure 5.5(a). By correlating the radiation loss to Figure 5.5(a), the thermal conductivity (SiNW and the contacts) was calculated to be 1.9W/mK. In Figure 5.5(b), the intrinsic SiNW thermal resistance can be obtained via the linear portion as highlighted (17 x 10^6 K/W over ~600nm), which translates to a SiNW thermal conductivity of 4.1W/mK. From the calculations, we can see that the thermal contacts' contribution to the measurements were significant, which can be attributed to the short SiNW in our case. Nevertheless, it is quite remarkable to

see that the thermal conductivity of the SiNW used in the fabricated TED to be of the same order as the best measured in [5.8].

5.2 Device level characterization

5.2.1 Experimental setup

Setup 1 – Macro heating setup

In order to characterize the fabricated SiNW-based TED described in chapter 4 at the device level, a home-made heating/cooling setup was prepared to generate a temperature gradient across the SiNW array. The setup consisted of brass heating plate and heat sink with embedded PT100 temperature sensors. The heating plate was operated using a proportional-integral-derivative (PID) controller and the temperature sensors were pre-calibrated (to an accuracy of 0.1^{o}C) using a temperature controlled oven. This setup as compared to the thermal test chip did not have the capability to provide for local heating, but was able to generate a larger temperature gradient across the SiNW layer. Figure 5.6(a) and (b) show the photo images of the whole setup and the heating plate, respectively.

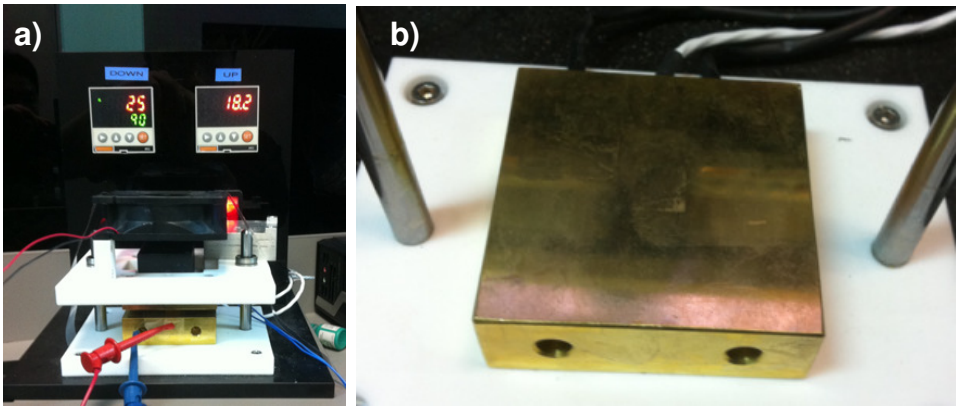


Figure 5.6: Photographs of a) the whole setup with the top display showing the temperature of the heat sink and the heating plate, and b) the heating plate respectively.

Setup 2 – Thermal Test Chip

A second setup using a thermal test chip was fabricated to facilitate the characterization. In this setup, the thermal test chip containing heaters and resistance temperature detector (RTD) was used to provide the heating capability as well as sensing the temperature of the chip real time; the thermal test chip was fabricated on an 8" Si wafer using Cu damascene technology [5.9]. In total, we used three layers of serpentine copper (Cu) lines to define the background heater (1cm x 1cm), local heater (400µm x 400µm) and the RTD (100µm x 100µm). This chip aimed to replicate global heating and local hotspots while monitoring the thermal mapping of the chip. The purpose of the local hotspots was to mimic localized heating in microprocessor chips which are becoming more common as transistors scale down [9]. Such a thermal test chip can be used for the characterization of thermoelectric devices in both cooling as well as power generation. The fabricated thermal test chip was diced and flip chip bonded to a

dedicated printed circuit board (PCB), which acted as a substrate for the test chip. Figure 5.7 shows the photograph of the thermal test chip bonded onto the PCB.

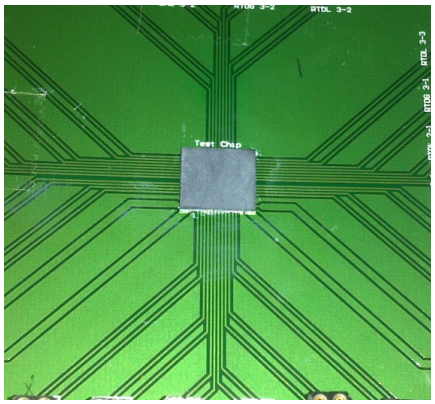


Figure 5.7: Photograph of the fabricated thermal test chip flip-chip bonded onto a dedicated PCB

During characterization, the temperature gradient was generated by powering the heater at the bottom while the top is cooled using forced convection using a standard CPU fan. It is worth pointing out again that while the top temperature was being monitored using a thermocouple probe tip attached to a separately fabricated heat sink (milled out of aluminum block) in the first setup, the second setup used the embedded temperature sensor in the top heat sink to accomplish the same task.

5.2.2 Thermoelectric power characterization

Electrical characterization

The SiNW-based TED was first characterized as a thermoelectric power generator. Prior to measuring the thermoelectric power output, the SiNW-based TED was first tested for electrical continuity to ensure the groups of n- and p-type SiNWs were well connected in a serpentine manner. This was done through I-V measurements (using an Agilent 5156C semiconductor parameter analyzer on a probe station) of the six different metal pads (1-6) connected to it at the sides as shown in the photo image taken in Figure 5.8(a). Figure 5.8(b) shows the measured plot of resistance as function of the number of elements connected in series while the inset shows the I-V characteristics between the six measurement pads.

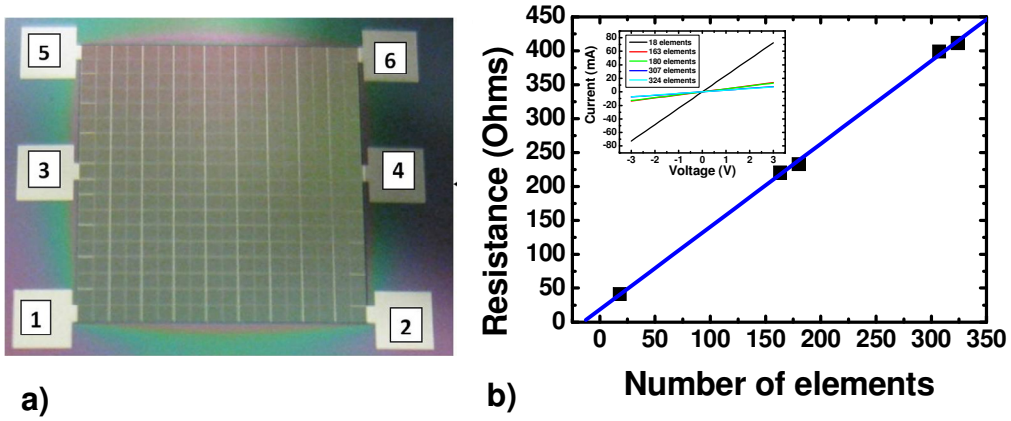


Figure 5.8: a) Photograph taken of the fabricated SiNW-based TED, and b) measured plot of resistance as function of the number of elements connected in series. The inset shows the I-V characteristics between the six measurement pads.

In Figure 5.8(b), the proportionate scaling of the thermoelectric legs' resistance and the linear I-V relationship in the inset confirmed that the thermocouples are linked properly in a serpentine manner, as well as the achievement of ohmic contacts between the thermoelectric legs and top metal. It should be noted here that the resistance values in Figure 5.8(b) included both the SiNW resistance and its contact resistance to the top/bottom metal. On a wafer scale, both the SiO_2 and polyimide filled TEDs had measured electrical resistances ranging from 400Ω to >1000Ω; this result appears to be much larger than what was expected. Considering the doping concentration of the SiNW at 1 x 10^{-19} cm^{-3}, a resistance in the region of 10 Ω (excluding contact resistance) was expected. A separate experiment involving much smaller sets of SiNW was carried out to extract its electrical resistance. The electrical resistance was extracted based on the experiment presented in Chapter 3. This resulted in a single SiNW resistance extracted to be ~3kΩ. Thus, it was concluded that the larger than expected device resistance can be attributed to the large electrical contact resistance. The cause of the large electrical contact resistance will be further addressed below.

Thermal stacks in experimental setup

The first setup was used for thermoelectric power generation characterization. A temperature difference (*dT*) was set up across the SiNW-based TED by powering the heater on in the experimental setup while cooling the top of the setup using a standard CPU fan (forced convection). As described in Chapter

4, the fabrication of the SiNW-based TED required the use of a filler material for both structure integrity and to define the top metal traces. However, the use of a filler material introduced thermal parasitic resistances into the device which would degrade the final thermoelectric power output. Hence, it is important to understand the impact of the filler material inclusion. In the analysis of the effect of filler material, the notion of thermal resistance ($R_{thermal}$) is more commonly used as the dT sustained across a particular layer (in a stack) can be simply expressed as in equation 5.2.

$$dT_{layer} = \frac{R_{layer}}{R_{total}} \times dT_{total} \text{ --- (5.2)}$$

where dT_{layer}, R_{layer}, dT_{total}, R_{total} represent the temperature difference across and thermal resistance of the layer of interest and the whole stack, respectively. Theoretically, the lower the thermal conductivity, the larger the R_{thermal}, and hence the larger the dT that can be sustained across the SiNW layer. This implies that ideally, a material with zero κ will be desired to eliminate any thermal parasitic such that the heat gradient only flows selectively through the SiNW. The R_{thermal} of a layer can be expressed by equation 5.3 while and its effective R_{thermal} of a composite layer containing SiNW with a filler material is expressed by equation 5.4. In addition, by normalizing the thermal conductivity value of the filler material used to that of the SiNW, the relationship between $R_{effective}$ and R_{filler} is shown in Figure 5.9.

$$R_{\text{thermal}} = \frac{l}{\kappa A} \text{ ---------- (5.3)}$$

$$\frac{1}{R_{\text{effective}}} = \left(\frac{\kappa A}{l}\right)_{\text{effective}} = \left(\frac{\kappa A}{l}\right)_{\text{SiNW}} + \left(\frac{\kappa A}{l}\right)_{\text{filler material}} \text{---------- (5.4)}$$

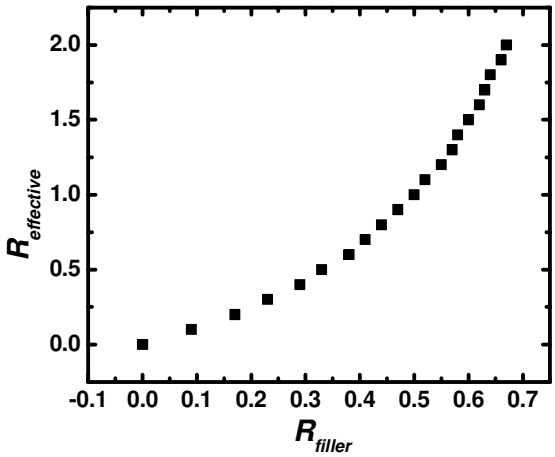


Figure 5.9: Variation of the effective thermal resistance of the composite layer with different thermal resistance values of the filler material (normalized to the thermal resistance value of SiNW)

Essentially, the $R_{effective}$ has a quadratic relationship with R_{filler}. Between the two filler materials – SiO_2 and polyimide which were described in Chapter 4 -- it is evident that polyimide is a better candidate with a thermal conductivity value one order lower than that of SiO_2 (0.14W/mK vs 1.4W/mK) [5.10-5.11]. In the experimental setup, besides the TED under test, we have to consider the different layers present between the heater and heat sink in order to better quantify the temperature distribution.. Figure 5.10 shows a schematic of the thermal layers present in the experimental setup complete with dimensions and their corresponding thermal conductivity values.

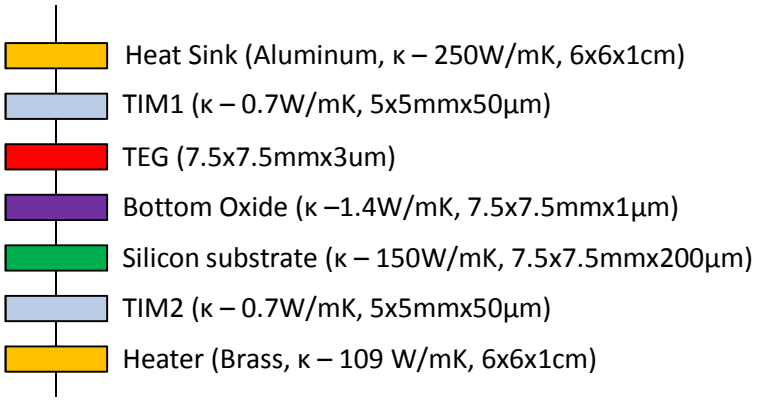


Figure 5.10: Schematic illustration of the different thermal layers of the experimental setup with dimensions and corresponding κ values of materials indicated

where TIM refers to a commercial thermal interface material (Thermalcote II) used and has a rated thermal conductivity of 0.7W/mK.

Thermoelectric power generation

According to the Seebeck effect, an open circuit voltage V_{oc} is generated across a thermoelectric material in the presence of a temperature gradient across its two ends. The specific relationship is given in equation 5.5

$$S = \frac{dV}{dT} \text{ ----- (5.5)}$$

In this characterization, we picked the TED with the lowest measured electrical resistance of 400Ω. The first experimental setup was used because of the ease of the PID controller in controlling the heater's temperature. In order to demonstrate the Seebeck effect, the bottom heater was powered on while the top and bottom temperatures were monitored using the embedded temperature sensors. The heater

temperature was first set to a maximum value of 100°C, and then allowed to cool down gradually to room temperature. This characterization methodology allowed much higher accuracy as compared to setting different temperatures and reading off *dT*; the latter method introduced significant temperature fluctuations due to competition between natural cooling and heating. During the cooling process, *dT* was recorded together with corresponding V_{oc} generated for both the TED with SiO_2 and polyimide as the filler material separately. In Figure 5.11, we show the relationship between a) V_{oc} and varying *dT* between heater and heat sink, a voltage/power *versus* current curve for the b) SiO_2 filled TED, c) polyimide filled TED at *dT* = 70K across the experimental setup, and d) a comparison between the maximum power output between the SiO_2 and polyimide filled TED under varying *dT*. In Figure 5.11(a), an increase in the V_{oc} is clearly observed with an increase in *dT* between heater and heat sink. This observation is in line with the Seebeck effect described in equation 5.5. Although it was found that the length of the SiNW with SiO_2 filler was 0.85µm as compared to 1.1µm with polyimide filler (Figure 5.12), there is a significant difference in the V_{oc} measured between the two, with the latter exhibiting a ~1 order improvement at the same *dT*. At 70K, the TED with SiO_2 as the filler material generated a V_{oc} of 1.5mV while that of the polyimide filled TED generated 27.9mV. In Figure 5.11(b) and (c), the I-V relationship was obtained by varying the external load. It can be seen that the maximum power occurred at the peak of the power curve (red) and it corresponds to a matched load condition, i.e., when the external load had same resistance as the TED.

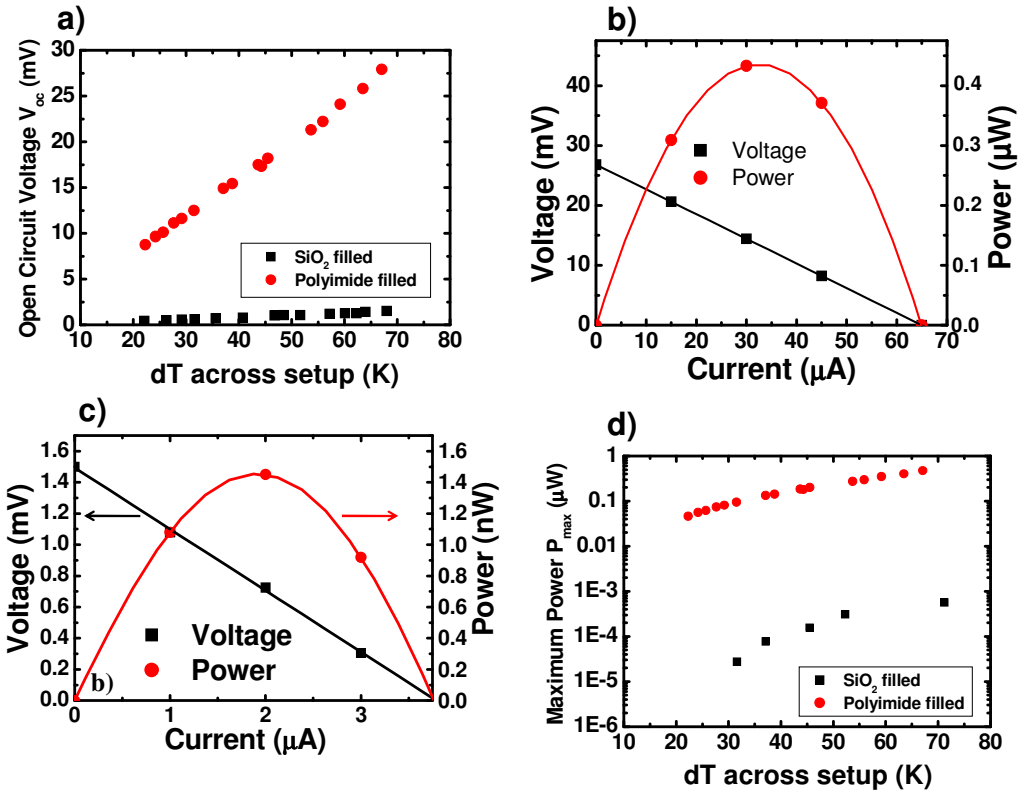


Figure 5.11: Relationship between a) V_{oc} and varying dT across the experimental setup, a voltage/power *versus* current curve for the b) SiO_2 filled TED, c) polyimide filled TED, at 70K across the experimental setup and d) a comparison between the maximum power output between the SiO_2 and polyimide filled TED under varying dT. The length of the SiNW with SiO_2 filler was 0.85µm as compared to 1.1µm with polyimide filler (shown in Figure 5.12)

The maximum power as a function of V_{oc} and the TED's electrical resistance can be expressed as in equation 5.6.

$$P_{max} = \frac{{V_{oc}}^2}{4R_{TED}} \text{ --- (5.6)}$$

The maximum power generated at dT = 70K across the experimental setup for the SiO_2 filled TED and polyimide filled TED were 1.5nW and 0.47µW respectively. Table 5.1 shows the comparison between the polyimide and the SiO2 filled

SiNW-based TED under a temperature difference dT of 70K across the experimental setup.

Table 5.1: Comparison between the polyimide filled SiNW TED and the SiO_2 filled SiNW TED under a temperature difference *dT* of 70K across the experimental setup.

***dT* = 70K (across setup)**	**Polyimide filled SiNW TED (A)**	**SiO_2 filled SiNW TED (B)**	**Ratio (A/B)**
V_{oc} (mV)	27.9	1.5	18.6
I_{sc} (μA)	67.0	3.79	17.7
P_{max} (W)	4.7×10^{-7}	1.5×10^{-9}	313

In Figure 5.11(d), the comparison of the maximum power generated of the two TEDs at different *dT* across the experimental setup shows an improvement of ~2 orders in the polyimide filled TED as compared to the SiO_2 filled TED. This can be explained by the quadratic dependence of P_{max} and V_{oc} as indicated in equation 5.6.

This measurement difference between the two TEDs with different fillers clearly demonstrated the advantage of using polyimide as the filler material, i.e., to sustain a larger *dT* across the SiNW layer which resulted in a larger V_{oc} generated at the same *dT* between heater and heat sink. In the same application and ambient, the polyimide filled TED will be able to "tap" into a larger *dT* to generate a larger power. To better explain this, we attempted to extract the actual *dT* sustained across the SiNW layer through a knowledge of the thermal layers dimensions and the thermal properties of the SiNW measured in the earlier

section. Firstly, through transmission electron microscopy (TEM), we were able to obtain accurately the thickness of the SiNW layer (length of the SiNW). Figure 5.12 shows the TEM image obtained on the cross section of the a) SiO_2 filled, and b) polyimide filled SiNW-based TEDs respectively.

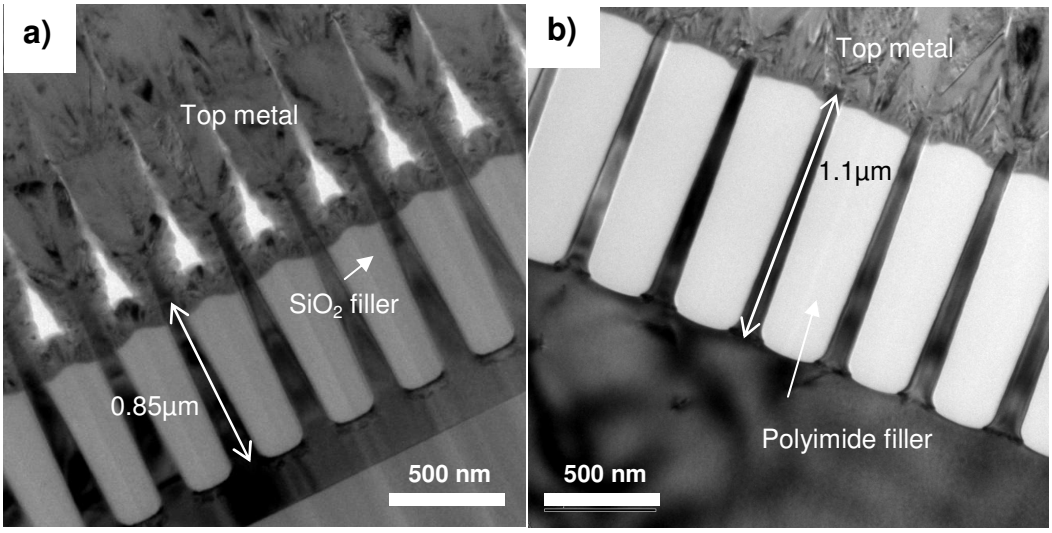


Figure 5.12: TEM image obtained on the cross section of the a) SiO_2 filled, and b) polyimide filled SiNW-based TEDs respectively.

From the TEM images, it can be seen that the desired final structure was obtained and both the filler materials were capable of filling the SiNW array gap well. There is however, a notable difference in the SiNW layer thickness with the SiO_2 filled TED measuring about 0.85µm while the polyimide filled TED at 1.1 µm (~20% difference). In both TEDs, the SiNWs had an average diameter of ~90nm. In addition, we observe from the TEM images that the thickness of the Ni silicide is much less than expected. This contributed to the cause of the large contact resistance which will be discussed in the next section.

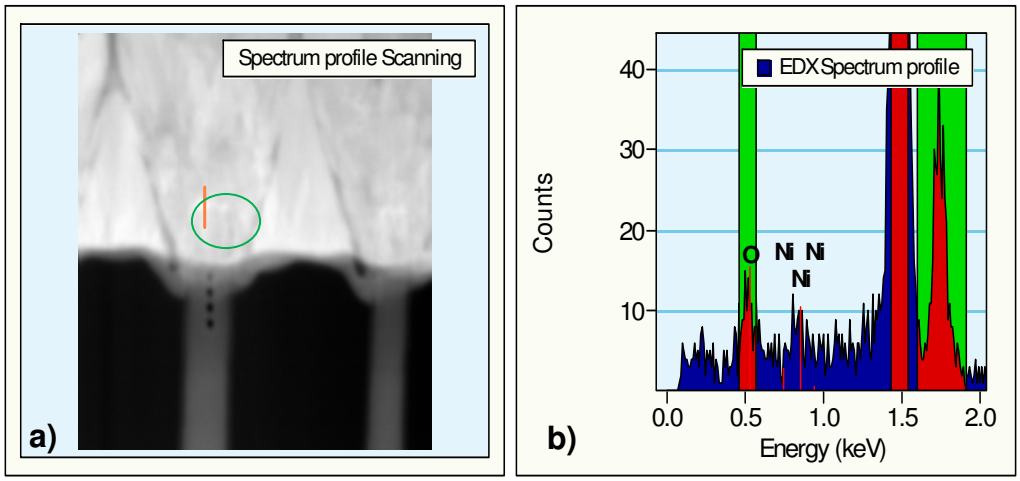
With the knowledge of the TEDs' dimensions as well as the thermal properties – polyimide (0.14W/mK) [5.12], SiO_2 (1.6W/mK), and the SiNW (4.1W/mK), equation 5.2 was used to calculate the $R_{thermal}$ of the TED. There were clearly numerous parasitic resistances in our setup of which, the TIM contributed to a significant portion of the total thermal resistance. Although the $R_{thermal}$ of the TIM is non-trivial, it is essential to ensure there is good thermal contact between the device and heater/heat sink. It is worth pointing out that without a good thermal contact, the presence of air pockets cannot be properly addressed in the thermal calculations. From the calculations, the dT sustained across the SiO_2 and polyimide filled SiNW array (with dT = 70K across the experimental setup) was extracted to be 0.1K and 1.2K respectively. It is thus clear that the choice of polyimide as the filler material was much more superior. With the average Seebeck coefficient of a TED to be $S = \frac{dV}{Ndt}$, where N is the number of thermoelectric legs, the average Seebeck coefficient was calculated to be 47μV/K and 71μV/K for the SiO_2 and polyimide filled TED, respectively; In comparison, bulk Si has a Seebeck coefficient of 150μV/K [5.8]. Nevertheless, it should be noted that the extraction of the Seebeck coefficient was device specific; under the same processing condition, the materials' Seebeck coefficient should be the same. In order to achieve an accurate Seebeck coefficient measurement of the SiNW, alternative methodology has to be looked into for synthesizing a longer SiNW length which can then be measured using the METS device individually. The comparison of the thermoelectric properties between the SiNW-based TEDs (SiO_2 and polyimide) is shown in Table 5.2

Table 5.2: Comparison of the thermoelectric properties of the SiNW-based TEDs

Parameters	SiO_2 filled	Polyimide filled
$R_{effective}$ of composite layer (K/W)	0.01	0.089
dT across composite layer with 70K across setup (K)	0.1	1
Extracted Seebeck coefficient (μV/K) – Device Specific	47	71

Improving electrical contact resistance via nickel silicidation optimization

It was briefly described earlier that the Ni silicide thickness could be the cause of the SiNW-based TED's large resistance. Close-up TEM views of the tip and bottom of the SiNW were obtained, followed by an energy dispersive x-ray spectroscopy (EDX) analysis. The results are shown in Figure 5.13 where a) and b) show the TEM image zoomed in at the tip and the EDX result, respectively; c) and d) on the other hand show the same analysis at the SiNW bottom.



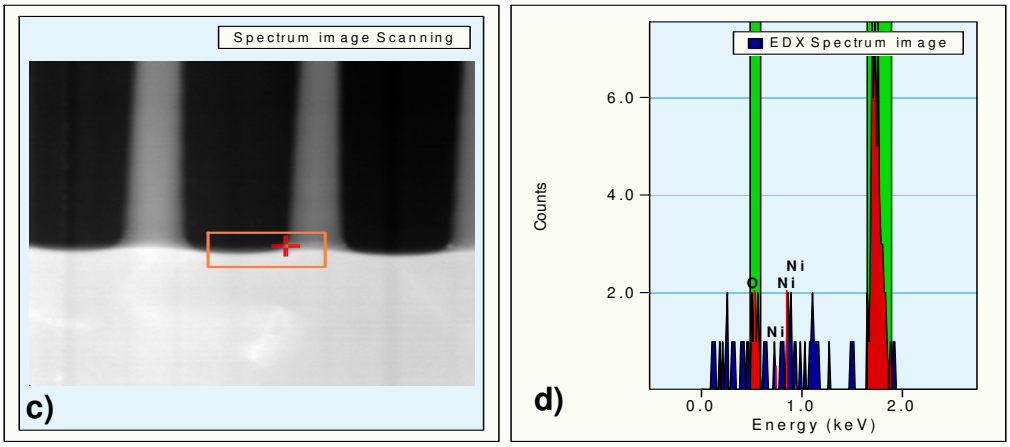


Figure 5.13: a) and b) show the TEM image zoom in at the tip and the EDX result respectively; c) and d) show the same analysis at the SiNW bottom.

It can be seen in Figure 5.13 that although there is the presence of Ni silicide, the Ni content is extremely low. The use of Ni silicide as a contact point between semiconductor and metal is widely used due to its property of having a low sheet resistivity [5.13]. The failure to form sufficient Ni silicide in the SiNW will impact the resistance of the fabricated TED, especially with nanostructures where the contact quality has a much more significant effect as compared to bulk materials [5.14]. In order to verify this hypothesis, we optimized the Ni silicidation process to obtain a larger Ni silicide thickness. A desired thickness with ~100 nm Ni silicide depth was obtained with a thicker Ni (400 Å) deposited prior to annealing at 400^{o}C for 30s. The TEM image of the optimized TED's cross section is shown in Figure 5.14.

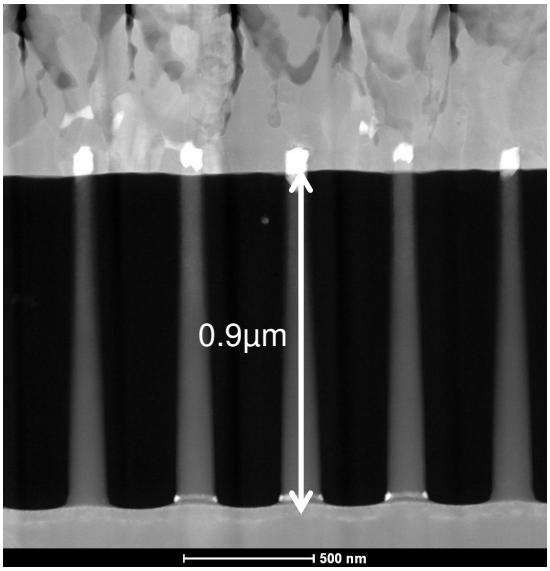


Figure 5.14: TEM image of the optimized TED's cross section showing desired Ni silicide thickness of ~100nm.

The optimized TEDs with optimized Ni silicide thickness were characterized using the same methodology described in the earlier sections. In the new set of measurements, the TEDs with optimized contacts (on the whole wafer) had measured electrical resistances ranging from 61Ω – 400Ω. In comparison, the earlier TEDs had measured electrical resistances ranging from 400Ω to >1000Ω. The TED with the lowest electrical resistance had an improvement of 7 times as compared to the earlier fabricated TEDs. However, there was a reduction of the V_{oc} measured at the same dT (Figure 5.11). The reduction was due to the deeper Ni silicide intrusion which consequently reduced the length of the thermoelectric section (0.9µm *versus*. 1.1µm) as indicated in Figure 5.12 and Figure 5.14. Nevertheless, owing to the significant improvement in the TED overall electrical resistance, the power output was enhanced. Table 5.3 compares the characterized

parameters of the optimized TED and the earlier fabricated TED with SiO_2 and polyimide filler material as indicated.

Table 5.3: Parameters of the optimized TED and the earlier fabricated TED with SiO_2 and polyimide filler material as indicated.

***dT* = 70 K**	**Polyimide filled TED with optimized contacts**	**Polyimide filled TED (previous)**	**SiO_2 filled TED (previous)**
V_{oc} (mV)	17.9	27.9	1.5
I_{sc} (μA)	293	67	3.79
P_{max} (μW)	1.31	0.47	0.0015

From Table 5.3, the impact of the contact resistance as well as the thermal conductivity of the composite layer can be seen clearly. At the current stage, even with a reduction in the electrical contact resistance, the performance of the SiNW-based TED can still be improved through further optimization. Comparing with current state-of-the-art BiTe superlattice based material in Table 5.4 [5.15], it can be seen that our final fabricated SiNW-based TED with optimized contacts has a power output density of the same order ($17kW/m^3$ *versus* $18.1kW/m^3$). This shows the competitiveness of SiNW in thermoelectric power generation. In addition, coupled with the scalability of Si and its low cost, SiNW is a very attractive candidate for further development in this area.

Table 5.4: comparison of SiNW and BiTe based superlattice thermoelectric power generation parameters.

Parameter	TED (SiO_2)	TED (polyimide)	TED (polyimide) – optimized contact	RTI [5.15]	SiNW [5.8]	Bulk Si [5.16]
Volume and diameter of SiNW	5mm x5mm x 3µm			2cm x2.3cm x0.3mm (Bulk supperlattice)	50nm diameter	N/A
	80nm diameter	80nm diameter	80nm diameter			
Material	SiNW (DRIE)			MOCVD BiTe /superlattice	SiNW	Si Bulk
Power output (kW/m^3)	1.9	6.5	17	18.1 (based on 0.0025W/K)	N/A	N/A
Conductivity	2.1×10^4 (n) – Extracted separately (Chapter 3)				5.88×10^4 (n)	2×10^4 (p) 4×10^4 (n)
Seebeck Coefficient (µV/K)	47 (n-/p- ave.) – Device specific	71 (n-/p- ave.) – Device specific	55 (n-/p- ave.) – Device specific	N/A	245 (n)	350 (p) 350 (n)

5.2.3 Thermoelectric cooling

Apart from thermoelectric power generation, the SiNW-based TED was also characterized as a thermoelectric cooler (TEC). It is worth pointing out that only the SiNW-based TED with the optimized Ni silicide profile was characterized as the large contact resistances from the earlier batches would have a larger negative impact as discussed in Chapter 3. Using the electrical measurements on the contact resistance and the resistance of the SiNW, the thermoelectric cooling analysis as presented in Chapter 3 was used to estimate the

expected cooling performance. Figure 5.15 shows the cooling performance curve of the SiNW-based TED with the optimized contacts. The red curve is a polynomial fit of all the data points.

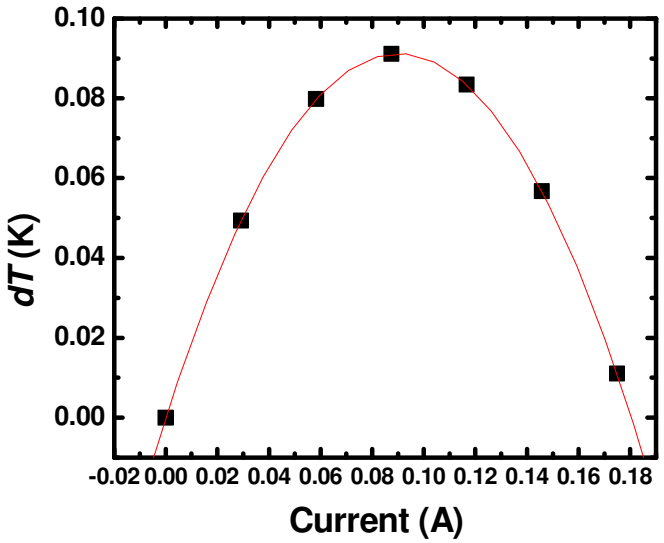


Figure 5.15: Simulated cooling performance curve of the SiNW-based TED with the optimized contact. The curve is a polynomial fit of all the data points.

In the theoretical analysis, we used the electrical parameters obtained during the device characterization, i.e., S = 55μV/K, ρ = 4.7 x $10^{-3}\Omega cm^{-2}$, and κ = 4.1 W/mK, as well as the knowledge of the total number of SiNW in the array. It can be seen that due to the negative impact of the electrical contact resistance, the expected maximum temperature suppression is just below 0.1K.

For the characterization, the second setup was first used with the methodology as described in [5.9]. The background heater of the test chip was powered together with the local heater while passing different current through the TED. However, there was no observation of temperature suppression from the

embedded temperature sensor. The reason for this could be the limited sensitivity of the temperature sensor not being able to register the change. To verify further, a high sensitivity infra-red (IR) camera by FLIR [5.17] was used to capture the surface temperature change as the current through the SiNW-based TED was varied. In this setup, the TED was placed on a metal table to simulate an infinite heat sink scenario, while the camera was positioned directly above the TED to capture the surface temperature as the current through it was varied. The current of the TED was varied using a Keithley 2400 source meter. Figure 5.16 shows the IR images of the TED as the current through it was varied. We can observe the images getting brighter as the temperature was raised. At the indicated point highlighted with a star, the temperature difference *dT* was plotted with respect to the current applied and compared to the simulation analysis in Figure 5.17.

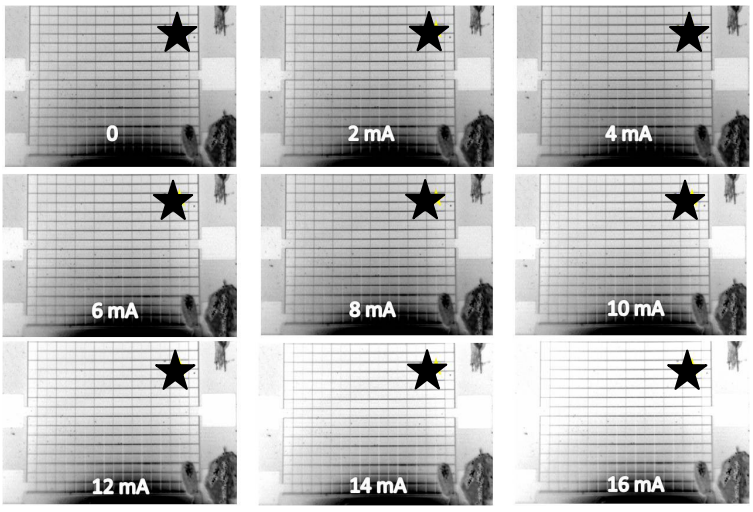


Figure 5.16: IR images of the TED as the current through it was varied. The "star" on the image represented the spot where the surface temperature was monitored.

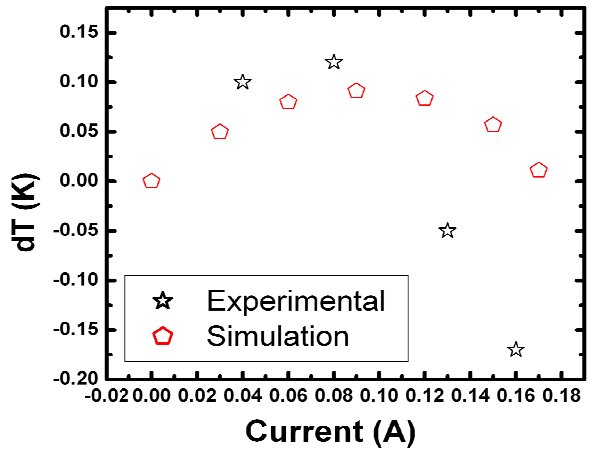


Figure 5.17: Graph comparing the measured result with that of simulation as current varies

This cooling curve observed is reasonable – an initial depression of the temperature due to thermoelectric cooling, followed by a rise in temperature due to Joule heating as current through the SiNW-based TED increases. The maximum temperature depression of the SiNW-based TED was measured to be ~0.1K ± 0.01K, which is close to that of the simulation (Figure 5.15). The small temperature depression can be attributed to the large electrical contact resistance present, which cause significant Joule heating even with a small current applied. However, the current required (scaled to number of SiNW used in TED) was slightly smaller than that of the simulation. This reveals that there is a small percentage of SiNW which did not form proper contacts to the top metal. It is clear that the temperature suppression of current fabricated device is insufficient for practical application. Nevertheless, our approach provides a good platform on which further performance optimization such as improving the contact resistance, SiNW length and density can be built on.

5.3 Chapter summary

In this chapter, the characterization of a SiNW-based TED was done at both the individual SiNW level as well as from a device level. At the nanowire level, we described the fabrication of a suspended METS device which is useful in measuring the thermal properties of nanostructures such as SiNW in our case. SiNW as used in the TED exhibited a low thermal conductivity as compared to bulk Si, which indicates its potential as a suitable thermoelectric material. At the device level, the experimental setup for thermoelectric power generation was presented and TEDs with SiO_2 and polyimide as the filler material were characterized. In the thermoelectric power generation mode, the TED with polyimide as the filler material clearly surpassed the TED with SiO_2 as the filler material. The lower rated thermal conductivity value of polyimide is critical in sustaining a larger temperature difference across the SiNW composite layer. Through optimizing the contacts between SiNW and the top metal, the overall TED resistance was reduced ~7x, which enhanced the power output further. In the thermoelectric cooling mode, the TED with optimized contacts was characterized. IR images measured a temperature depression of ~0.1^{o}C. Further optimization work has to be done to reduce the electrical contact resistance so as to eliminate unwanted Joule heating during operation, and to ensure good yield of good contacts. In particular, better fabrication process will be the key to achieve this goal.

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Chapter 6: Characterization of a Silicon-Germanium Nanowire Based Thermoelectric Device

The study of CMOS compatible nanowire (NW) as a thermoelectric material has been focused mostly on silicon (Si) till date [6.1-6.4]. The investigation of another CMOS compatible NW - silicon germanium (SiGe) is currently limited to SiGe superlattices and $Si_{0.8}Ge_{0.2}$ NW array [6.5-6.6]. Bulk SiGe as opposed to state-of-the-art bismuth/antimony (Bi/Sb) based material is often used for high temperature applications >1000^{o}C [6.7]. In this chapter, the integration of a SiGe NW-based thermoelectric device (TED), followed by the characterization using the platform and methodology established in Chapters 4 and 5 will be discussed. In addition, the growth mechanism of the nickel (Ni) germanosilicide (a by-product by annealing Ni and SiGe) in SiGe NW for contact purpose will be studied.

6.1 Fabrication process

The fabrication steps of the SiGe NW-based thermoelectric device (TED) are similar to those of the SiNW-based TED [6.8-6.9]. The main difference is the incorporation of the SiGe layer (1.2µm) which was done using an epitaxy process prior to the formation of the NW. The Ge concentration in the SiGe layer can be

varied by tuning the GeH_4 gas flow during the epitaxy process. The gas flow condition – Si_2H_4: 10sccm, GeH_4: 260sccm at 550°C was used for a $Si_{0.5}Ge_{0.5}$ layer. Figure 6.1(a) and (b) show the scanning electron microscope (SEM) images of the SiGe NW and SiNW for comparison, respectively.

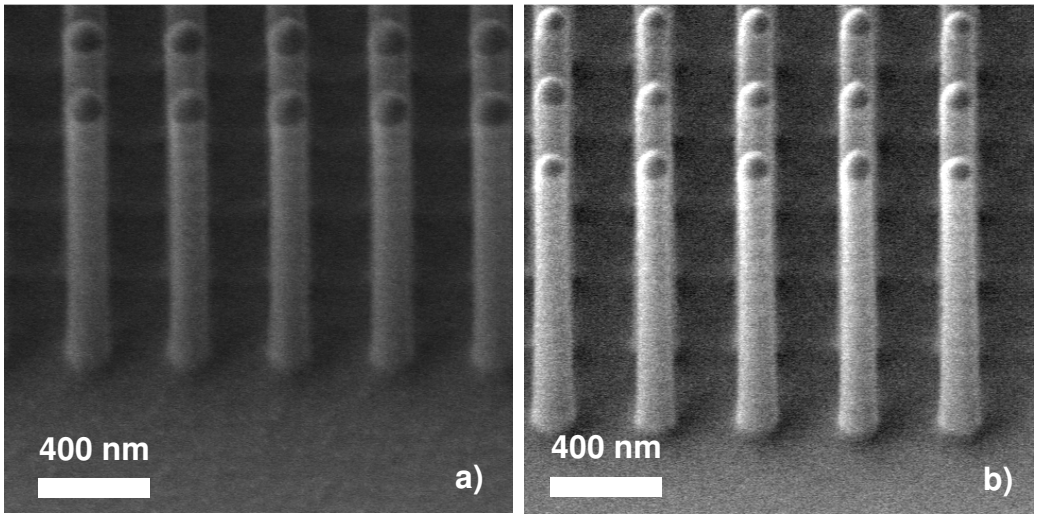

Figure 6.1: SEM images of (a) SiGe NW, and (b) SiNW for comparison purpose.

It can be observed that the epitaxial SiGe layer is of good quality where the surface of the SiGe NW formed appears to be relatively smooth. There was no observable difference in the surface compared to the SiNW. For the remaining fabrication process, the SiGe NW device wafers went through exactly the same steps as those of the SiNW device, i.e., ion implantation to define the n- and p-type bundles of SiGe NWs, formation of top and bottom metallization via a nickel germanosilicidation process, application of polyimide filler between the gaps, formation of the top metal traces using aluminum (Al), and a final layer of silicon nitride (Si_3N_4) as passivation.

Although the steps taken were the same, however due to the different material system, a notable difference was observed after the Ni germanosilicidation process. In the Ni germanosilicidation process, the conditions for nickel deposition and annealing were chosen to be the same as those of the SiNW-based TED – annealing at 400^{o}C for 30s. As shown in Figure 6.2 is the SEM images of the SiGe and SiNW array which were annealed under the said condition after selective removal of the un-reacted Ni using SPM (H_2SO_4:H_2O_2 mixture of 1: 4).

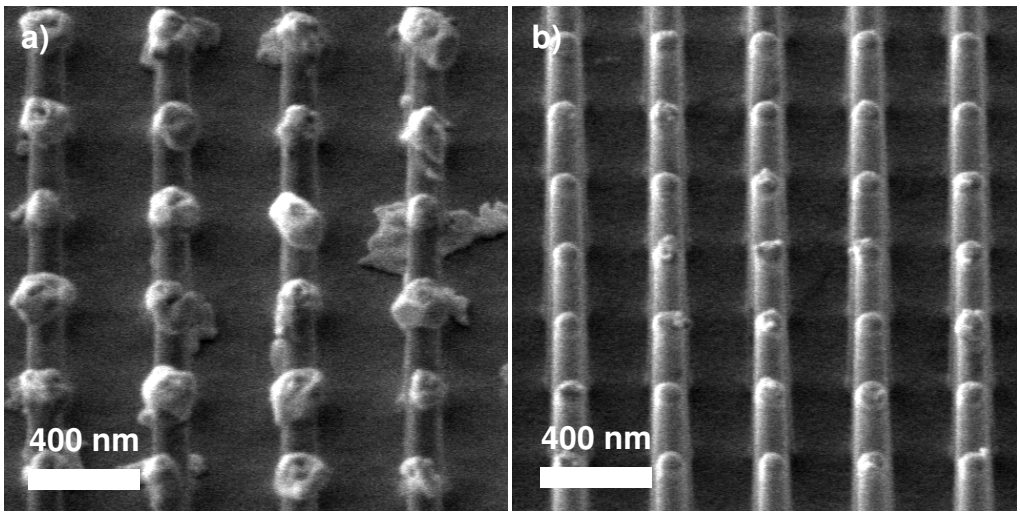

Figure 6.2: a) SEM image of the SiGe NW, and b) SiNW after annealing under 400^{o}C for 30s and having excessive nickel removed using SPM.

From Figure 6.2(a), it can be observed that for the SiGe NW, there were abnormal protrusions of the reacted portions with nickel as compared to the well-formed tips of the SiNW in Figure 6.2(b). It appears that there was a difference in the growth mechanism during the annealing process which we were unable to explain

at that point of time. Subsequently, the SiGe NW array was filled with polyimide and top metal electrodes (Al) linking up the n- and p- type bundles of SiGe NW formed. A final passivation layer using 1000Å of Si_3N_4 completed the fabrication. Apart from the difference in the observed structure of the SiGe NW, there were no other irregularities observed for the other process steps. The SiGe NW-based TED had a NW array size of 5 mm x 5 mm (60% was occupied by the n- and p-doped SiNWs), and consisted of 162 thermocouples. The NW in the array had a length of ~1.1µm and diameter of ~80nm.

6.2 Characterization of a silicon-germanium nanowire-based thermoelectric deivce

The characterization methodology of the SiGe NW-based TED was the same as that for the SiNW-based TED. Initial electrical testing was carried out to obtain the TEDs' resistance, followed by device-level thermoelectric power generation measurements using the experimental setup as described in Chapter 5.

6.2.1 Electrical measurements

I-V measurements were performed on an Agilent 5156C semiconductor parameter analyzer on a probe station. It was surprising that the extracted resistance from the I-V graph was in the region of 10kΩ, and was 2 orders larger

than that of the SiNW-based TED. Figure 6.3 shows the I-V measurements of the SiGe NW-based TEDs across the whole wafer.

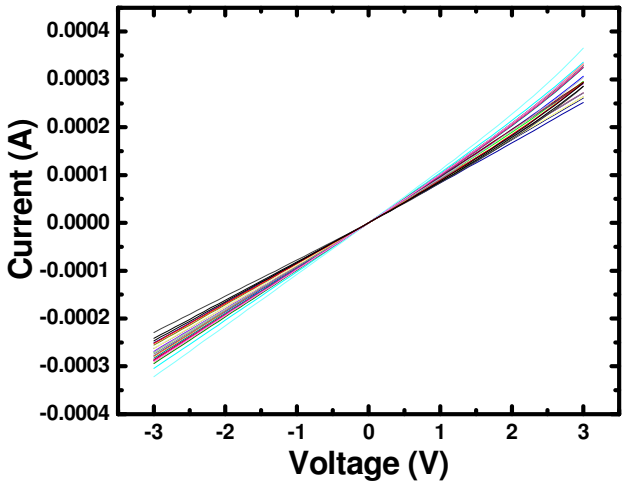

Figure 6.3: I-V measurements of the SiGe NW-based TEDs across the whole wafer. A series of measurements were shown because of the much larger electrical resistance measured as compared to the SiNW-based TED.

In Figure 6.3, almost all the curves indicated an ohmic contact, and the device resistance was extracted using the best fit line of each curve. A total of 25 SiGe NW-based TEDs was measured and resistances ranged from ~10kΩ to 13kΩ. The designed electrical resistance was expected to be the same as the SiNW-based TED but was >2 orders of magnitude larger here. It is clear that the thermoelectric performance of the SiGe-NW based TED would not be comparable to the SiNW-based TED.

6.2.2 Thermoelectric power generation characterization

The SiGe NW-based TEDs were then characterized for the thermoelectric power generation performance. We picked three TEDs of the lowest resistance (10kΩ) and measured their open circuit voltage (V_{oc}) with varying temperature across the experimental setup (Figure 6.4).

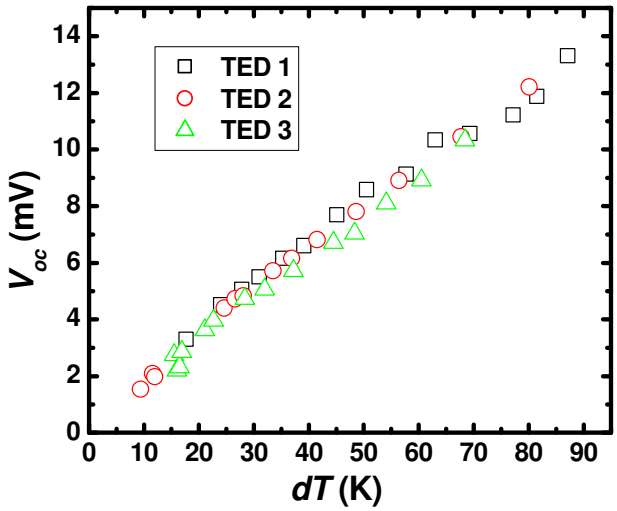

Figure 6.4: Open circuit voltage (V_{oc}) with varying temperature across the experimental setup

It can be seen that the three TEDs had quite consistent thermoelectric power output. At 70K across the experimental setup, the V_{oc} obtained was ~11mV, which is ~40% smaller compared to the SiNW-based TED. Table 6.1 shows the comparison between the SiGe NW-based TED, and the best SiNW-based TED with optimized contacts.

Table 6.1: Comparison of the SiGe NW and SiNW based TED

dT = 70 K	SiGe NW-based TED	SiNW-based TED with optimized Ni silicide
V_{oc} (mV)	11	17.9
I_{sc} (μA)	1.1	293
P_{max} (μW)	3×10^{-3}	1.31

As the other fabrication steps were the same, the smaller V_{oc} is due to a shorter thermoelectric leg, as well as a difference in the Seebeck coefficient in the SiGe NW.

6.2.3 Origin of the large electrical resistance of the silicon-germanium nanowire-based thermoelectric device

To better understand the origin of the large electrical resistance measured of the SiGe NW devices, we obtained the cross section of the SiGe NW-based TED. Figure 6.5(a) and (b) show the dark field TEM images of the SiGe NW and SiNW for reference, respectively.

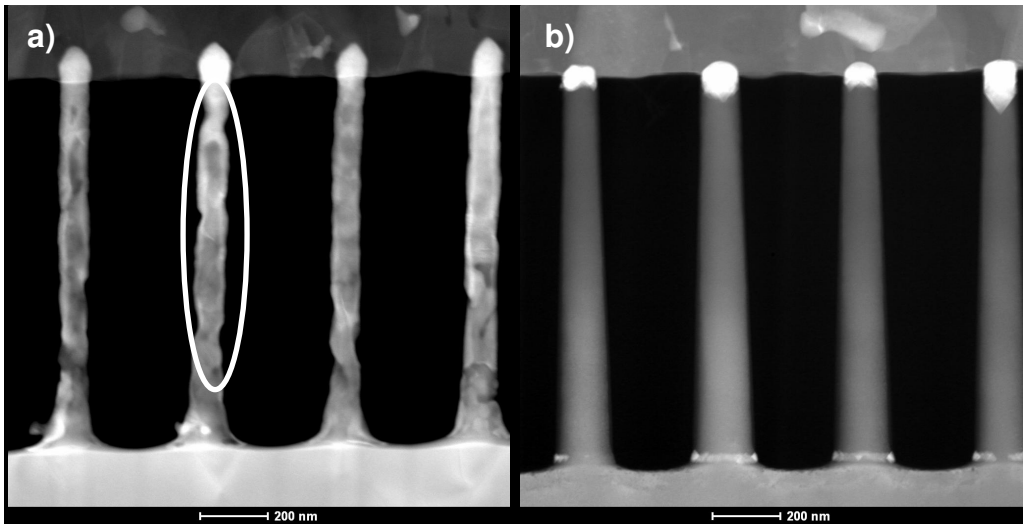

Figure 6.5: Dark-field TEM images of the (a) SiGe NW and (b) SiNW.

It can be observed that the SiGe NW looks very different compared to the SiNW. While the SiNW is smooth throughout its entire length, the SiGe NW's sides appear to be jagged along its length as highlighted. In addition, the Ni intrusion is much deeper. It is reasonable to attribute the extremely large resistance measured to the "constrictions" along the SiGe NW. Such a structure can severely limit the current flow, thus leading to a high resistance. It is clear that the metal silicide growth mechanism in SiNW and SiGe NW are different.

To elucidate the observation, new batches of SiGe NW array were fabricated on test wafers and TEM images obtained after the Ni annealing process. A SiNW reference wafer was fabricated alongside. Figure 6.6 shows the TEM images obtained for the (a) SiGe NW array and (b) SiNW array.

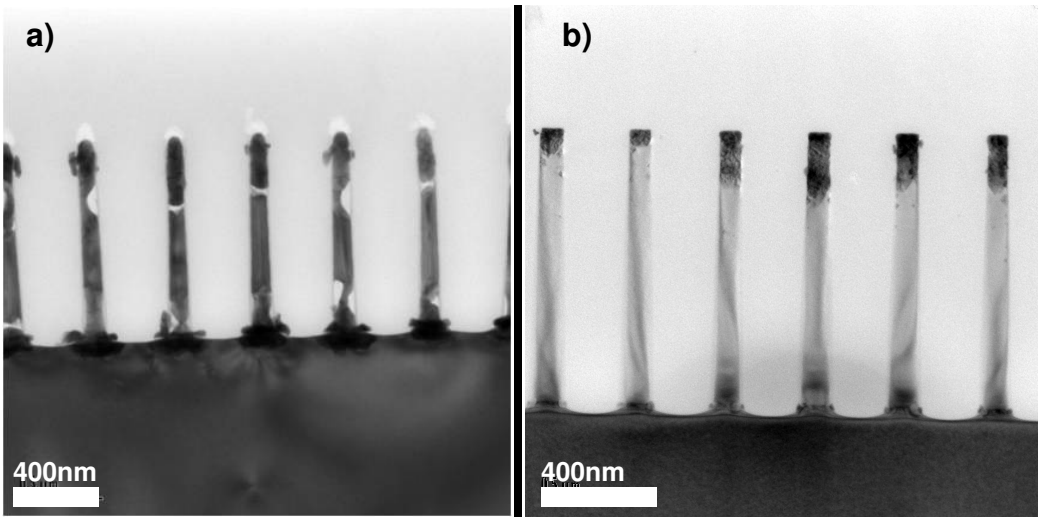

Figure 6.6: TEM image showing a zoom out view of the a) SiGe NW array, and b) SiNW array

It can be observed again that there is a great difference in appearance between the SiGe NW and SiNW. Although we did not observe jagged edges, the constriction re-appeared with voids observed. For the case of SiNW in Figure 6.6(b), the portion with the darker contrast corresponds to the nickel silicide; its overall structure is the same as observed in the dark-field image. On the other hand, the SiGe NW in Figure 6.6(a) tells a different story. Sections of the SiGe NW which resemble voids showed up in all the SiGe NW captured in the image. A zoom-in view of the SiGe NW TEM image was obtained and presented in Figure 6.7. Figure 6.7(a) and (b) show two different sections of the SiGe NW near the tips while Figure 6.7(c) and (d) show two different sections of the SiGe NW near the bottom.

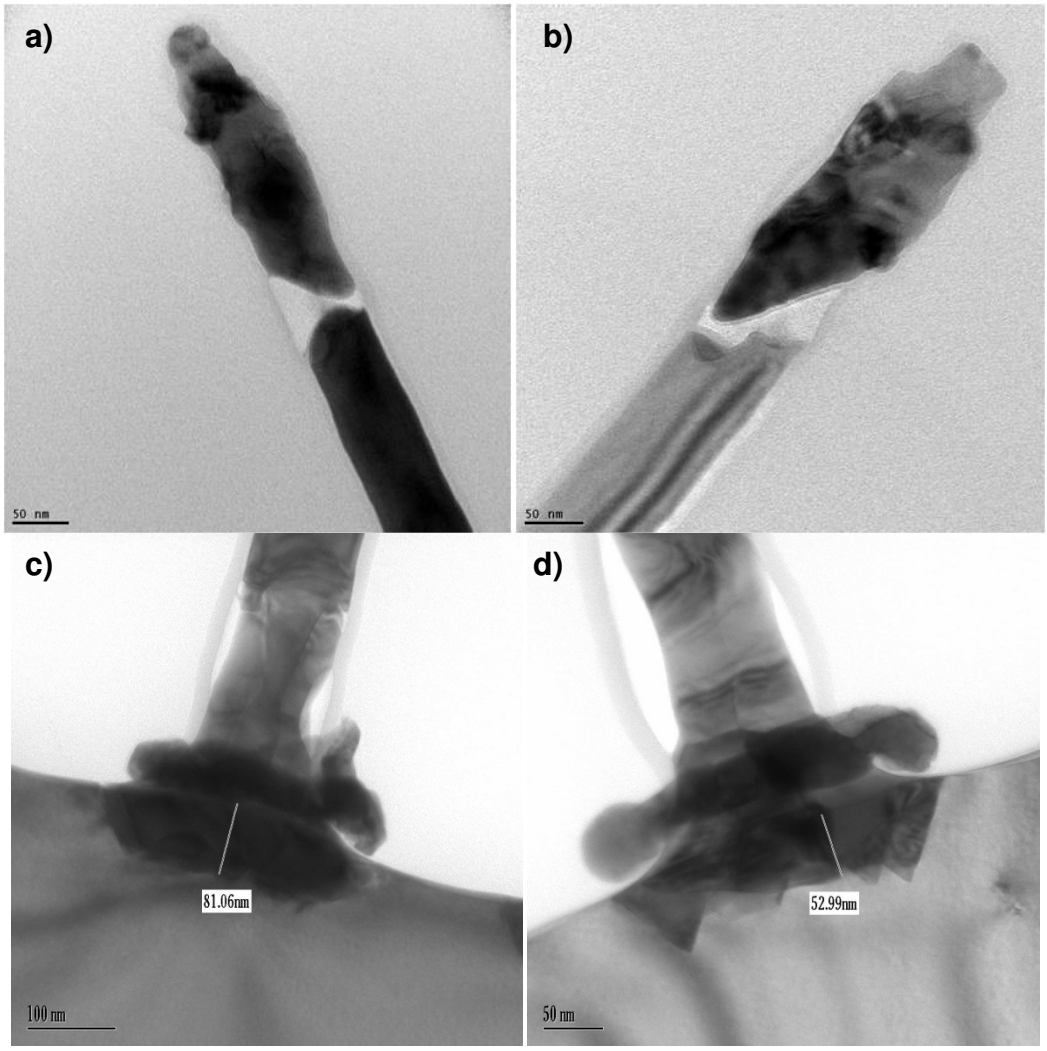

Figure 6.7: TEM images showing the zoom in view of the SiGe NW near the a) tip area 1, b) tip area 2, c) bottom area 1, and d) bottom area 2.

From Figure 6.7, there are several observations. Firstly, a thin oxide spacer of ~15nm can be seen along the length of the SiGe NW. The oxide spacer appears to be continuous throughout. Secondly, nickel germanosilicide formed can be distinguished from the contrast of the SiGe NW image, which indicates success of the annealing process. However, it can be seen that the portions which resemble voids are found near the interface of the different contrast and some kind of

material protrusions appears to be happening near the top and bottom of the SiGe NW. To further investigate and confirm the material composition along the SiGe NW, we perform energy dispersive x-ray spectroscopy (EDX) at different spots along the SiGe NW. Figure 6.8 shows the TEM image of the SiGe NW and the spots (labeled) where the EDX analysis was carried out, while Figure 6.9(a) and (b) shows the result of the EDX analysis of spots 1-7 and 8-11 respectively.

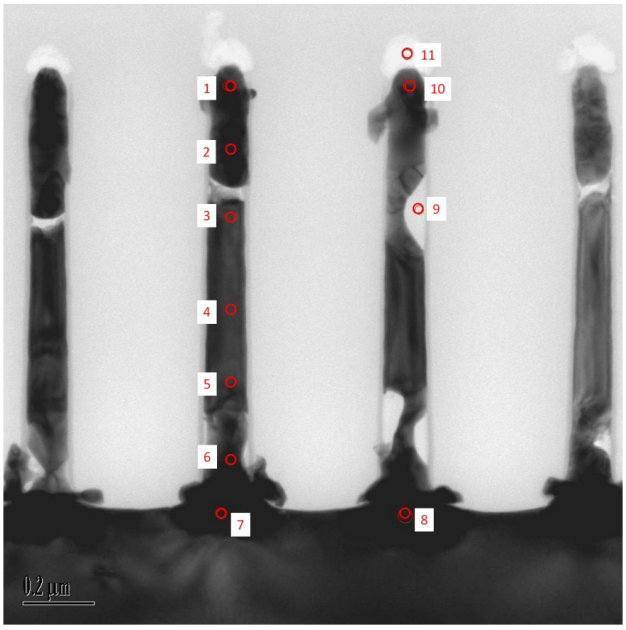

Figure 6.8: TEM images of the SiGe NW array. The labels indicated in the image shows the area where EDX analysis was carried out to find out the material composition of the structure.

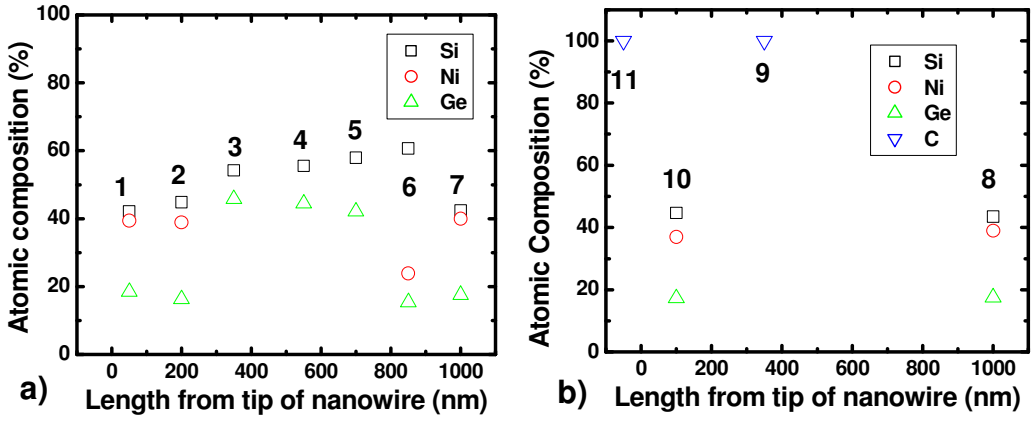

Figure 6.9: TEM images of the SiGe NW array. The numbered red circles indicated in the image shows the area where EDX analysis was carried out to find out the material composition of the structure. a) spot 1 – 7, and b) spot 8 – 11 (indicated).

From Figure 6.9(b), it is observed that the area with the lighter contrast is indeed a void. The presence of carbon (C) is due to the application of polymer during sample preparation for TEM.

A phenomenon of void formation upon annealing nickel with SiGe NW was observed. There have been numerous studies on the reaction of nickel with silicon due to industry's dominant use of nickel silicide to achieve low sheet resistance. On the other hand, studies on the nickel reaction with SiGe are relatively fewer, with none reported on SiGe NW [6.10-6.13]. In the case of nickel silicidation process, it is well-known that nickel is the dominant diffusing species[6.14]. However, for the case of SiGe NW it seems that a different growth mechanism takes place. To better understand the mechanism for the formation of nickel germanosilicide, we designed another experiment for this purpose.

6.3 Growth mechanism of nickel-germanosilicide in silicon-germanium nanowire

In this section, we investigated the growth mechanism of Ni-germanosilicide in $Si_{0.5}Ge_{0.5}$ alloy NW with and without a SiO_2 shell encapsulation. The growth mechanism was observed real-time using transmission electron microscopy (TEM) with *in situ* annealing of the SiGe NW array samples at 200^{o}C, 400^{o}C and 600^{o}C. For SiGe NW without the boundary constraint, material loss leading to void formation was observed at 600^{o}C. In addition, EDX analysis was conducted along the length of the SiGe NW to elucidate the phase transformations after annealing.

6.3.1 Sample preparation

The sample schematic which was desired in this experiment is as shown in Figure 6.10, where an array of SiGe NWs is filled with oxide (SiO_2) and a layer of Ni capped on top of the SiGe NW tips. The choice of using SiO_2 over polyimide was due to the consideration that the sample would be annealed at high temperatures.

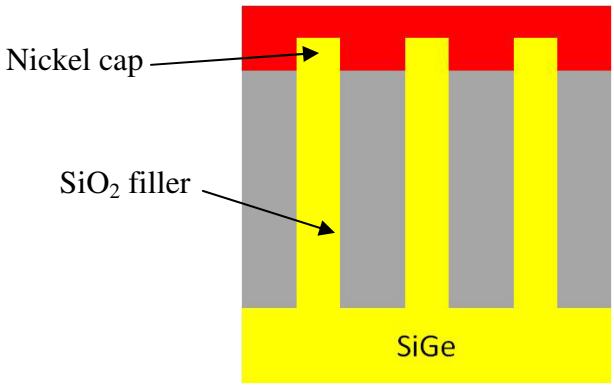

Figure 6.10: Schematic of SiGe NW array sample prepared for *in situ* heating in TEM

A high-quality $Si_{0.5}Ge_{0.5}$ layer (~0.5 µm thick) was first deposited on an 8", Si (100) wafer using the same epitaxy process described earlier. The SiGe NW array was then formed, followed by filling the air gap in between the SiGe NW using high-density-plasma (HDP) SiO_2, and an anisotropic SiO_2 etch to just expose the SiGe NW tip. A ~3000Å thick layer of Ni was then sputtered to make contact with the exposed SiGe NW tip. It is worth pointing that the SiO_2 filler also acted as a shell structure that played a role in exerting a compressive stress on the SiGe NW during annealing when expansion of the SiGe NW occurs [6.15-6.16]. Thereafter, a thin lamella sample of the SiGe NW array for TEM imaging was prepared using focused ion beam milling, before transferring to a Si nitride membrane window grid (SPI Supplies®) to facilitate the *in situ* annealing process. In total, two lamella samples were prepared in which one of the samples had its SiO_2 filler left intact, while the other sample had its SiO_2 filler etched using a vapor hydrofluoric acid process. Figure 6.11 shows TEM images of the prepared samples (a) with the SiO_2 filler intact, and (b) after the removal of the SiO_2 filler.

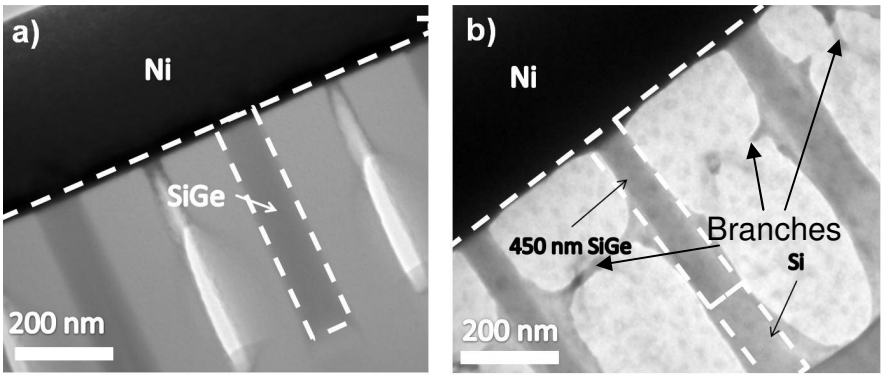

Figure 6.11: TEM image of the prepared samples (a) with the SiO_2 filler intact, and (b) with the SiO_2 filler removed. In figure 6.11 (a), the bright spots are the air gaps which cannot be filled completely by the SiO_2 while in figure 6.11 (b), the observed "branches" are residues of the SiO_2 after the etching process. The darker and lighter contrast along the SiGe NW indicated the SiGe and Si portion respectively.

In Figure 6.11(a), the bright regions in the SiO_2 are the air gaps which could not be filled completely. In Figure 6.11(b), the observed "branches" are residues of the SiO_2 after the etching process. From the TEM images, we can observe that the NW formed has a total length of ~650 nm. The contrast difference indicates that the top ~450 nm is the epitaxy SiGe layer and the bottom 200 nm is from the Si substrate. It should be pointed out that ~50 nm of the SiGe NW tip is embedded in the deposited Ni.

6.3.2 Real-time transmission electron microscope imaging with *in situ* annealing

Real-time TEM imaging with *in situ* annealing was first conducted on the SiGe NW sample without the encapsulation of the SiO_2 shell. The sample was

placed in an ultra high vacuum chamber in the TEM while the *in situ* annealing was carried out using a TEM holder with a heating stage. During the experiment, the temperature of the heating stage was raised to 200°C, 400°C, and 600°C at consecutive stages of annealing, while TEM images were taken at 10s intervals. Figure 6.12(a), (b) and (c) show the TEM images of the SiGe NW sample after having been annealed at 200°C, 400°C and 600°C, respectively, for 500s.

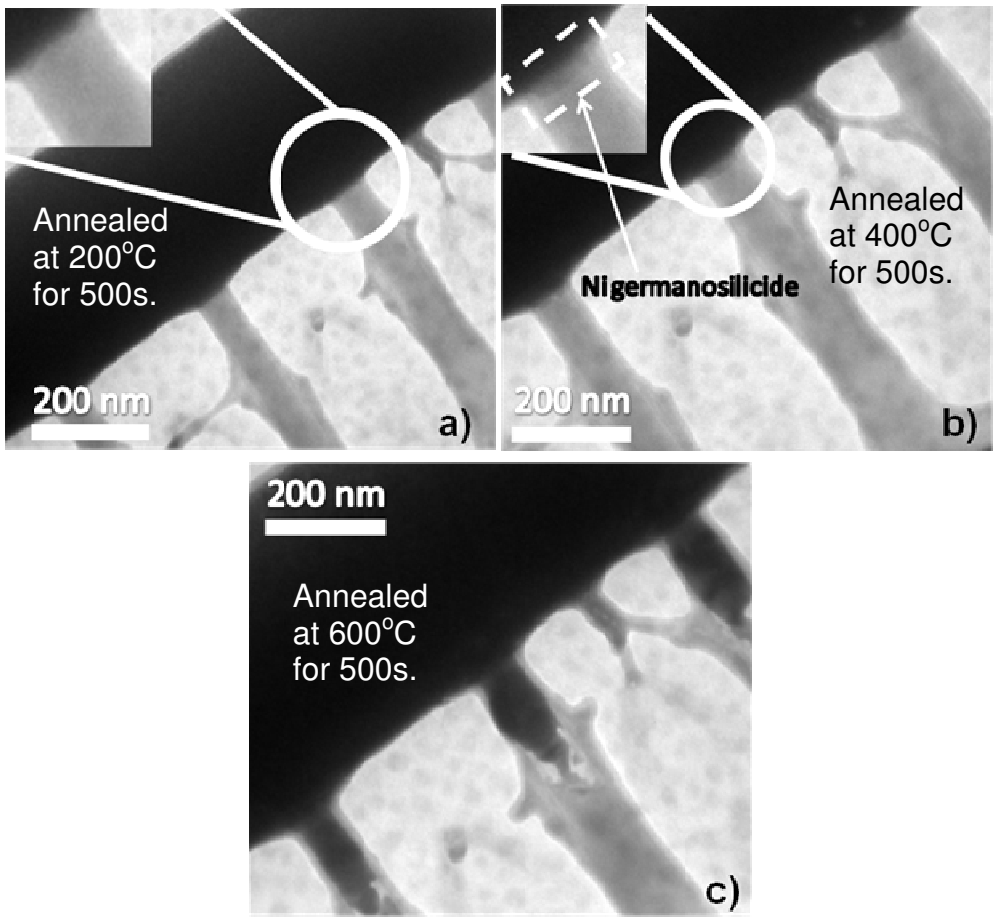

Figure 6.12: TEM images of the SiGe NW sample (without compressive stress) annealed at (a) 200°C, (b) 400°C, and (c) 600°C for 500s. The insets of figure 6.12 (a) and (b) are the magnified view of the SiGe NW near the tip area, which indicated minimal growth of the Ni-germanosilicide at 200°C and 400°C.

The insets of Figure 6.12(a) and (b) show the magnified views of the SiGe NW near the tip area. It can be observed that when the samples were annealed at 200^{o}C and 400^{o}C, the growth rate of Ni-germanosilicide was minimal. On the other hand, the growth rate was considerably faster at 600^{o}C, as shown in Figure 6.12(c). However, we also observed that the formation of Ni-germanosilicide in the SiGe NW was accompanied by voids. This observation could indicate excessive material loss during the annealing process. For a clearer picture of the void formation process, TEM images of the SiGe NWs obtained at different intervals are shown in Figure 6.13 where they represent the SiGe NW at times (a) 10 s, (b) 50 s, (c) 100 s, (d) 150 s, (e) 200 s, and (f) 250 s in the course of annealing.

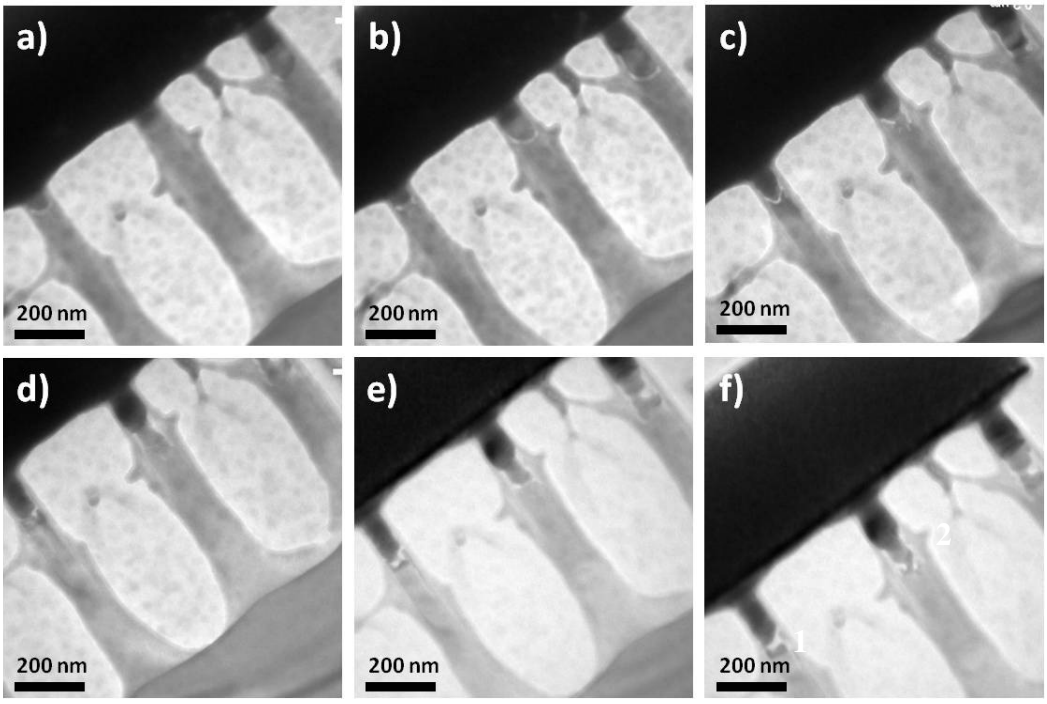

Figure 6.13: TEM images of the SiGe NW at times (a) 10 s, (b) 50 s, (c) 100 s, (d) 150 s, (e) 200 s, and (f) 250 s in the course of annealing (600^{o}C).

In Figure 6.13, we can observe the evolution of the Ni-germanosilicide growth – diffusion of Ni into the SiGe NW, followed by the forming of a neck as the Ni-germanosilicide formed, and eventual void. In Figure 6.14, we show the magnified view of the three SiGe NWs labeled (a) 1, (b) 2 and (c) 3 in Figure 6.13 (f) after the annealing process.

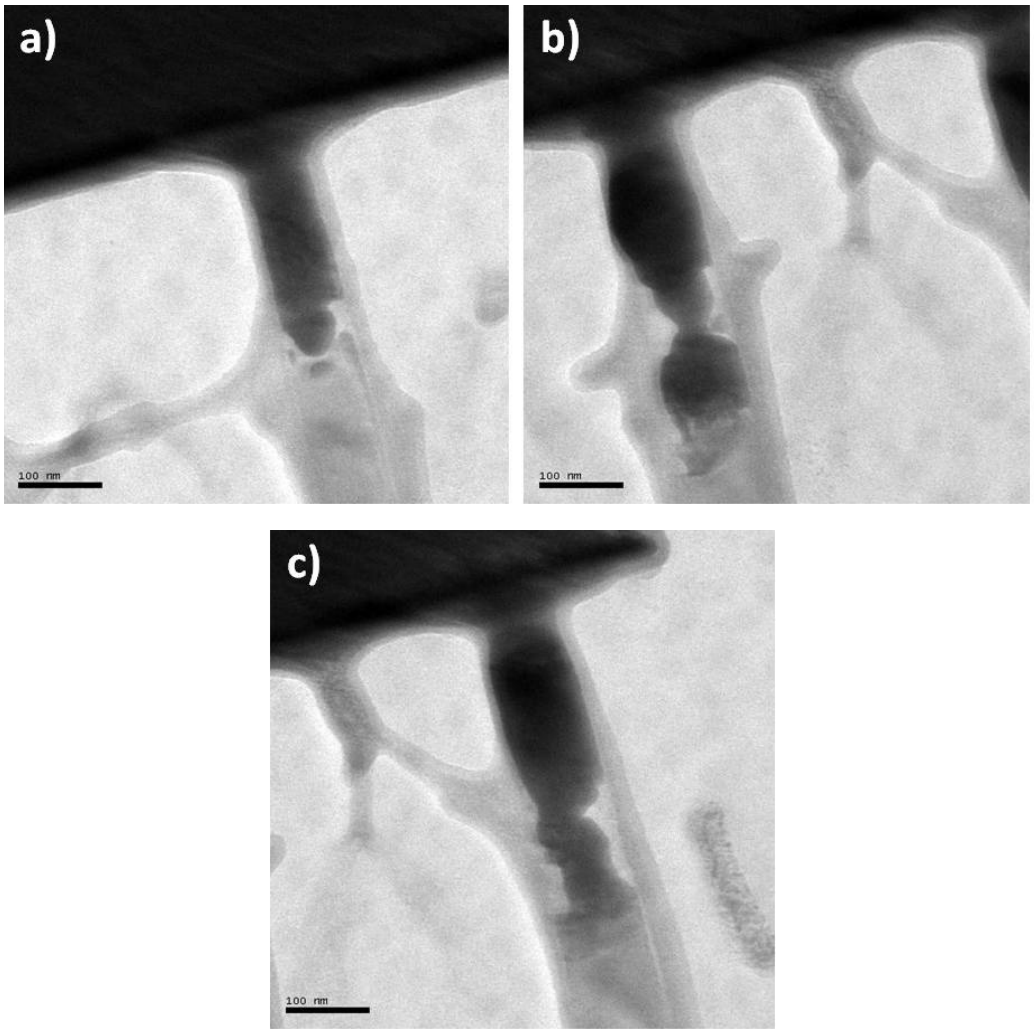

Figure 6.14: TEM images showing the magnified view of the three SiGe NW labeled (a) 1, (b) 2 and (c) 3 in Figure 6.13 (f) after the annealing process.

It is worth pointing out that all the SiGe NWs in the annealed sample exhibited the same visual characteristics. Apart from the void and the filament-like structure, we can also observe that close to the tips of the SiGe NW, there is bulging of excessive material. This observed phenomenon had neither been reported before in relevant literature which studied the interfacial reaction of Ni and SiGe layer [6.17-6.21], nor in the fabrication process of the SiNW TEG [6.8-6.9]. Such a void acts as an open circuit and is detrimental to a device's performance. The same experiment was then conducted on the SiGe NW sample with compressive stress induced, i.e., with SiO_2 filler intact. Similarly at 200^{o}C and 400^{o}C, the growth rate of the Ni-germanosilicide was minimal (figure not shown). However at 600^{o}C, the growth was different from that of the sample without compressive stress induced. Figure 6.15(a) to (c) show the TEM images of the SiGe NW at times (a) 10 s, (b) 200 s, and (f) 500 s while annealing at 600^{o}C.

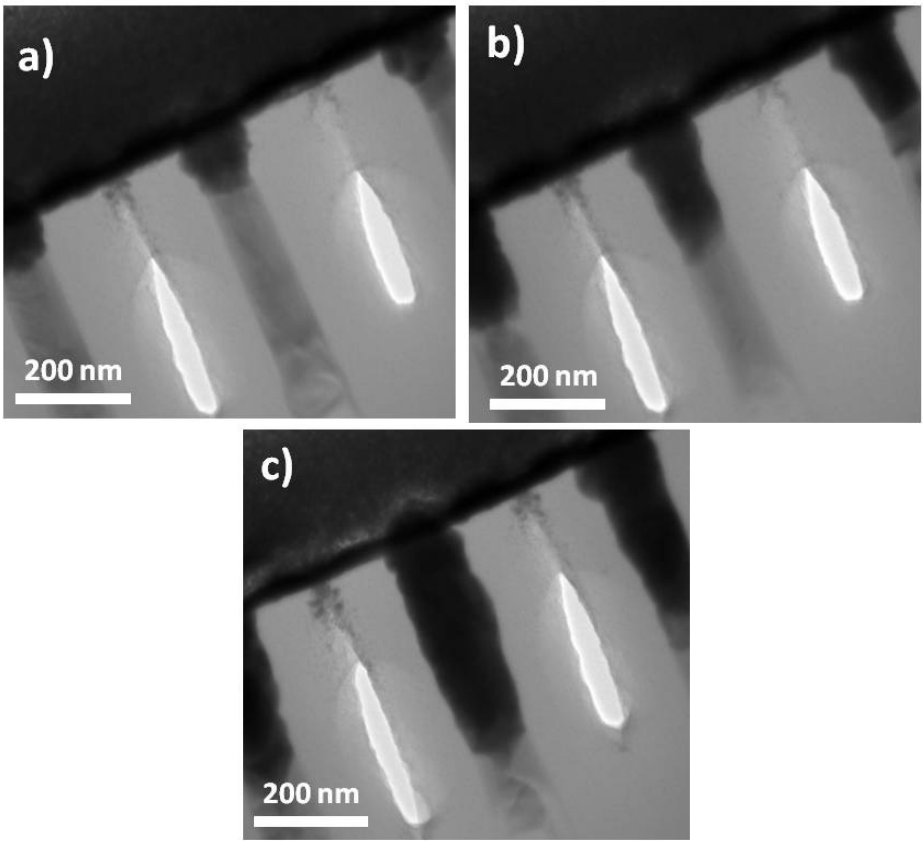

Figure 6.15: TEM images of the SiGe NW at times (a) 10 s, (b) 200 s, and (c) 500 s while annealing at 600^{o}C

As observe from Figure 6.15, the growth of Ni-germanosilicide in the SiGe NW did not result in void formed. The Ni-germanosilicide growth started from the tips and proceeded towards the Si substrate along the SiGe NW. This observation is different from Figure 6.13(c), where voids started forming in the SiGe NW during Ni-germanosilicide growth. It is again worth pointing that no void was observed in all the SiGe NW annealed.

6.3.3 Results and discussion

It is evident from the TEM images that a lack of compressive stress induced as a result of the SiO_2 shell encapsulation on the SiGe NW played a significant role in void generation during the formation of the Ni-germanosilicide. In the reaction between any silicide metal with a bulk SiGe layer, the widely-accepted process model involves the formation of metal-germanosilicide at lower temperature first, followed by the loss of Ge atoms at higher temperatures. Upon prolonged annealing, segregation of Ge atoms into the grain boundaries occurs. This eventually leads to the formation of a SiGe layer at the grain boundaries of the Ni-germanosilicide film, and renders it discontinuous [6.10, 6.13]. However, the extensive works done on SiGe layers do not explain the void observed in the SiGe NW without the SiO_2 shell encapsulation after annealing [6.17-6.21]. In order to better understand the interaction between Ni and the SiGe NW with/without compressive stress induced during annealing, EDX was used to determine the Ni, Si, and Ge composition along both SiGe NW samples before and after the experiment. Figure 6.16 shows the EDX results from the tip along the SiGe NW (a) before annealing, (b) without compressive stress induced, and (c) with compressive stress induced after annealing. For the case of the SiGe NW without compressive stress induced, the EDX result was obtained of the one shown in Figure 6.14(b).

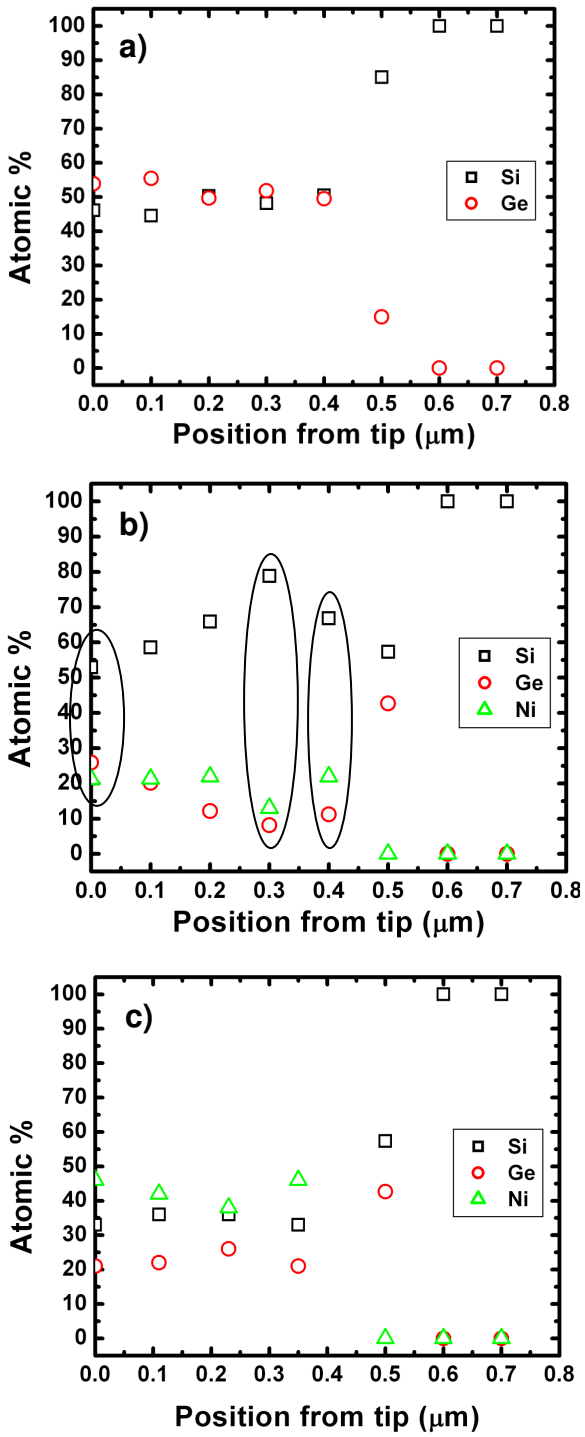

Figure 6.16: EDX results from the tip along the SiGe NW (a) before annealing, (b) without compressive stress induced, and (c) with compressive stress induced after annealing. The ovals (from left) in figure 6.16(b) highlight the composition at the tip, near the void and near the SiGe/Si interface respectively.

In Figure 6.16(a), we observe that a relatively uniform layer of SiGe (Ge concentration ~50%) was achieved in the epitaxy process. From Figure 6.16(b) and (c), we are able to observe the change in the composition of the different materials, i.e., Si, Ge, and Ni, along the SiGe NW without/with compressive stress induced during annealing, respectively. In the case of the SiGe NW without compressive stress induced, we obtained a Ni-germanosilicide composition of $Ni_{0.21}Si_{0.53}Ge_{0.26}$ (0μm, at the tip) to $Ni_{0.14}Si_{0.78}Ge_{0.08}$ (0.3μm, near the void), to $Ni_{0.14}Si_{0.78}Ge_{0.08}$ (0.4μm, near the SiGe/Si interface) as it goes down the length of the SiGe NW to the Ni-germanosilicide-SiGe interface. It can be noticed that there is an increase in the Si concentration as the Ge concentration decreases, and the variation in the Si and Ge concentrations is most significant around the void area by correlating the information from Figure 6.14(b) and Figure 6.16(b). The significant drop in Ge concentration (and void) suggests that Ge atoms out-diffused much faster than the Si and Ni atoms. On the other hand, in the case of the SiGe NW with compressive stress induced during annealing, the Ni-germanosilicide phase remains relatively constant.

Hence, the bulk Ni-germanosilicide model described in references [6.10, 6.13] do not apply for the case of SiGe NW. In the case of the SiGe NW with no compressive induced during annealing, as opposed to the formation of SiGe grains between Ni-germanosilicide grain boundaries, a void was formed instead. In fact, our observations are more in line with the study of Ni germanide formation in Ge NW, where a break in the Ge NW near the Ni germanide-Ge interface was always observed at temperatures > 450^{o}C [6.22]. It is more

reasonable to propose that in the case of SiGe NW without any compressive stress induced during annealing, the Ge atoms in the SiGe NW have a tendency to segregate towards the Ni-germanosilicide-Ni source interface. This effect can be seen in the buldging of Ni-germanosilicide near the tips, which further expands into the surrounding as the interaction continues. The growth mechanism of the Ni-germanosilicide in SiGe NW without the SiO_2 shell encapsulation can be summarized by the schematic in Figure 6.17(a) to (e).

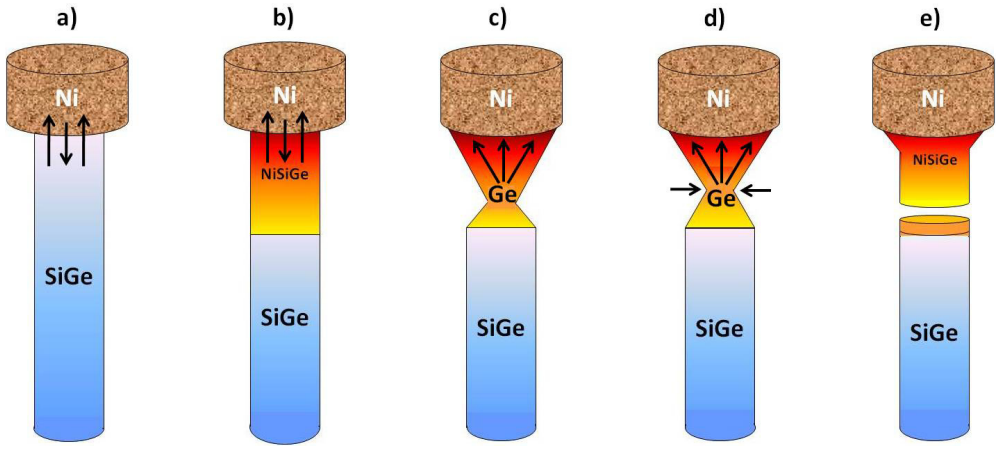

Figure 6.17: Schematic illustrating the formation of Ni-germanosilicide in SiGe NW without SiO_2 shell encapsulation. a) During annealing, Ni and SiGe interdiffuse to form b) Ni-germanosilicide. c) Considering Ge atoms being the dominant diffusion species, a neck in the Ni-germanosilicide starts to form with bulging near the tips. d) Due to the lack of restriction to the out-diffusion of the Ge atoms, the neck formed constricted further while the Ni-germanosilicide further expands into the surrounding, and e) upon prolonged annealing, a break occurs in the SiGe NW.

On the other hand, in the case of the SiGe NW with compressive stress induced during annealing, we can observe that the volume of Ni-germanosilicide formed appears to expand into the surrounding SiO_2 filler along its length. With no void

observed, the expansion in volume is due to the diffusion of Ni atoms into the SiGe NW. Thus, it is reasonable to suggest that a large compressive stress is being exerted by the SiO_2 filler on the SiGe NW. In a stressed structure, the diffusivity (D) of atoms in a material with cubic crystallography can be described by Equation 6.1 [6.16].

$$D = \frac{1}{6} a^2 v f \exp\left(\frac{-G}{k_B T}\right) \text{ --- (6.1)}$$

where a, v, f, and G are the jumping distance, effective vibrational frequency, correlation factor for jumping events away from true random walk, and Gibbs free energy of activation, respectively. It is worth noting that the Gibbs free energy of activation is a summation of the Gibbs free energy of formation of the mobile species and the Gibbs free energy of migration of the mobile species. Equation 6.1 can be transformed into Equation 6.2 via differentiation w.r.t. to the compressive stress (p) experienced by the structure to describe it's relation with D.

$$V^* = \frac{\partial G}{\partial p} = -k_B T \frac{\partial \ln(D)}{\partial p} \text{ --- (6.2)}$$

In Equation 6.2, the rate of change of G with p is known as the activation volume V^*, which can be interpreted as the change of volume as the Ni atom diffuses into

the SiGe lattice for our case; ∂p can be viewed as the change in pressure due to the external force or residual stress in the material. If a large compressive stress on the SiGe NW is induced, the diffusion rate of the atoms will be retarded as compared to the stress-free case. From Figure 6.13(c), it is apparent that the Ni atoms first diffuse in the SiGe lattice through the interstitial sites, thus enlarging the SiGe NW and leads to a positive V^*. This in turn increases the compressive stress on the SiGe NW, and has the effect of suppressing the out-diffusion of Ge atoms towards the Ni source, and creating a void. On the other hand, for the case of the SiGe NW without the encapsulation of the SiO_2 filler, there is no intended compressive stress imposed on the structure during annealing when expansion in volume occurs. Thus, this imposes no restriction to the out-diffusion of the Ge atoms, thereby resulting in the void observed in the process.

6.4 Chapter summary

In this chapter, we have presented on the characterization of a SiGe NW-based TED. I-V measurements revealed very large device resistance as compared to the SiNW-based TED. Cross sectional TEM analysis of the SiGe NW showed that voids were formed at the Ni-germanosilicide region, as well as the occurrence of deep Ni intrusion as compared to the SiNW. With a short effective SiGe NW length and large resistance, the V_{oc} (14mV) and hence, P_{max} (nW) were reduced significantly. To understand the cause of the void observation, we studied the growth mechanism of Ni-germanosilicide with and without compressive stress

induced via SiO_2 filler on the SiGe NW at temperatures of 200°C, 400°C, and 600°C. Using TEM with *in situ* annealing, the SiGe NW without compressive stress induced ended up with void formation. EDX results of the Si, Ge and Ni composition along the SiGe NW show a drastic drop in Ge concentration near the void region. The results show that the loss of material from the sides of the SiGe NW is due to the Ge atoms having a tendency to segregate/out-diffuse from the Ni-germanosilicide towards the Ni source during annealing. On the other hand, annealing of the same SiGe NW with compressive stress induced by the SiO_2 filler as a result of material expansion did not result in void formation. EDX results along the SiGe NW indicated a relative uniform concentration of Si, Ge and Ni throughout. This is in contrast to the EDX result of the first sample, where excessive out-diffusion of the Ge atoms occur due to the lack of any suppression mechanism; the explanation is in line with the diffusivity equation of atoms in a material. As good contacts to all SiGe NWs in the fabrication of a SiGe NW-based thermoelectric device are required, the methodology of using a SiO_2 shell to induce compressive stress on SiGe NW during formation of metal-germanosilicide is effective for void suppression.

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Chapter 7: Summary and Future Works

In this thesis, we presented the development, fabrication, characterization and evaluation of a complete silicon (Si)/silicon-germanium (SiGe) nanowire (NW) based thermoelectric device (TED). Firstly, using finite element analysis (FEA) simulations, the impact of key material parameters in a SiNW-based thermoelectric cooler's (TEC) performance was elucidated for practical applications. The key parameters -- thermal conductivity, length, filling material, and contact resistance are systematically studied. In addition, the effect of contact resistance on the performance of a SiNW-based TEC is complemented with experimentally extracted values from a SiNW-Al system fabricated using CMOS process. It was found that the presence of contact resistance degrades the maximum temperature depression of the TEC and should be properly addressed. Following, a design guideline by taking into account the studied parameters is proposed for a complete SiNW-based TEC for on-chip cooling application.

Secondly, the development of a fabrication scheme for a complete SiNW-based TED using complementary metal oxide semiconductor (CMOS) compatible process was presented. Individual n- and p- type thermoelectric legs consisted of a bundle of SiNWs each, was formed with a combination of high resolution deep ultraviolet (DUV) lithography, dry reactive ion etching process (DRIE), and an ion implantation process. Our approach allowed scaling and precision in the placement of the thermoelectric legs. Two filler materials – high density plasma

silicon dioxide (SiO_2) and polyimide were used for SiNW support and both filled the air gap well. In addition, we also highlighted the problems encountered in the fabrication scheme – the limitations of the SiNW array density (400nm pitch) as well as length of the SiNW achievable (<1.5μm) using our approach. The limitations of the pitch resulted in a larger measured total device's resistance; while the short length of SiNW reduced the temperature difference and Seebeck voltage that can be generated. These limitations impacted the maximum power output that can be generated by the SiNW-based TED.

Thirdly, we discussed the characterization of the fabricated SiNW-based TED at both the micro level (individual NW) and device level. At the micro level, the characterization of individual n- type SiNW used in the TED was carried out using a micro-electrothermal system (METS) device developed by our research group. The METS device consisted of two suspended silicon nitride (Si_3N_4) membrane-islands with platinum (Pt) serpentine lines which served as both heater to increase the temperature, and sensor to monitor the temperature change in the Si_3N_4 membrane-islands. Individual SiNW (from TED) was picked up and placed between the suspended Si_3N_4 membrane using a tungsten tip mounted on a nano-manipulator and a scanning electron microscope (SEM). Our SiNW measured a commendable thermal conductivity of ~4.1W/mK, which is of the same order of the SiNWs reported in notable literature. At the device level, a testing setup which consisted of a heating plate at the bottom and a heat sink on top was used for thermoelectric power characterization; the temperatures were measured using embedded PT100 temperature sensors. For characterization, the SiNW-based

TED was sandwiched between the heating plate and heat sink, while a temperature gradient (*dT*) was generated by powering the heating plate and cooling the heatsink using a CPU fan. Overall, the SiO_2 filled TED generated ~1.5nW of power with *dT* across setup of 70K, while polyimide with an order lower rated thermal conductivity raised the maximum power output by >2 orders to ~0.47μW under the same conditions. Further optimization of the electrical contacts through annealing to form nickel (Ni) silicide at the SiNW tips reduced the device's resistance by seven times, and the maximum power output raised by 3x to ~1.3μW. However, due to the non-trivial electrical contact resistance, infrared imaging of the SiNW-based TED's surface (thermoelectric cooling characterization) only measured a maximum temperature suppression of ~0.1K. Nevertheless, our approach and working demonstration represented the first functional integrated NW-based TED ever reported.

Lastly, the characterization of a SiGe NW-based TED was presented. The SiGe-NW based TED was fabricated based on the platform established for the SiNW-based TED; the only difference being the SiGe layer obtained by an epitaxy process at the starting step. Using the same characterization methodology that of the SiNW-based TED, the SiGe NW-based TED exhibited a >2 order-of-magnitude larger device electrical resistance and an open circuit voltage (V_{oc}) which was ~40% lower. Cross sectional transmission electron microscope (TEM) analysis revealed deep Ni intrusion into the SiGe NW (500nm *versus* 100nm for SiNW) and the formation of constrictions/voids in the Ni germanosilicide region. The deep Ni intrusion reduced the effective length of the thermoelectric legs and

reduced the V_{oc}, while the constriction resulted in the large electrical resistance measured. The growth mechanism of Ni germanosilicide and its composition in SiGe NW was then investigated with and without the effect of compressive stress using TEM with *in-situ* annealing. Energy dispersive X-ray spectroscopy (EDX) along the SiGe NW without compressive stress revealed that there was a drastic drop in Ge concentration near the void region, which can be attributed to the out-diffusion of Ge atoms during annealing. The same analysis was conducted on the SiGe NW with compressive stress applied; this was achieved using a SiO_2 shell to constrain the SiGe NW during annealing.TEM results of the SiGe NW with no voids observed indicated that excessive out-diffusion of the Ge atoms was suppressed. Hence, the methodology of using SiO_2 shell in inducing compressive stress on SiGe NW during contact formation will be critical to eliminate void formation in devices.

The study of Si/SiGe NW-based TED in this thesis gives us a good idea of their potential and limitations as a thermoelectric material, and how favorably it can be compared to state-of-art bismuth/antimony based TED. Using Si/SiGe NW for cooling applications still requires more effort in reducing parasitic. However, the demonstration of the SiNW-based TED to power up in the μW region makes it a notable nano-scale thermoelectric energy harvester for miniaturized electronic devices.

The entire platform – from fabrication to characterization methodology developed -- allows further in-depth optimizations and study to be carried out; a cost effective and efficient Si/SiGe NW-based TED is desired. In summary, future

work in the following will be beneficial to bring the use of a Si/SiGe NW-based TED into reality.

1. Process methodology to synthesize NW array with a higher density to improve the heat load removal capability in a TEC.
2. Process methodology to integrate longer NW in a TED for capturing a larger *dT* for greater thermoelectric power generation/temperature depression.
3. Process optimization to further reduce the electrical contact resistance of a NW-metal system for thermoelectric cooling/power enhancement.
4. Finally, fundamental thermoelectric properties studies to the obtained Si/SiGe NW of different diameters will be interesting to understand how it affects the TED's performance.

List of Publications/Conferences

Publications

[1] **Y. Li**, K. Buddharaju, N. Singh, G. Q. Lo, and S.J Lee, "Chip-Level Thermoelectric Power Generators based on High Density Silicon Nanowire Array Prepared with Top-down CMOS Technology", IEEE Electron Device Letter, 32 (5), May 2011

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