ADVANCED TRANSISTORS FOR SUPPLY VOLTAGE REDUCTION: TUNNELING FIELD-EFFECT TRANSISTORS AND HIGH-MOBILITY MOSFETS

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Declaration

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Guo Pengfei

28 Aug 2013

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Abstract

Due to the excellent scalability, low cost, and high performance, complementary metal-oxide-semiconductor (CMOS) transistors have been widely used in electronics for the past four decades. However, continuous scaling of CMOS devices causes serious power consumption issues as the leakage current and the operation frequency of an integrated circuit (IC) increase. To reduce the power consumption, supply voltage V_{DD} needs to be lowered. Tunneling field-effect transistors (TFETs) and high-mobility $Ge_{1-x}Sn_x$ channel metal-oxide-semiconductor field-effect transistors (MOSFETs) are promising candidates to enable the reduction of V_{DD} and power consumption. In this thesis, TFETs with novel structures and high-mobility $Ge_{1-x}Sn_x$ MOSFETs are explored.

In this thesis, we studied the TFET device physics by analyzing the temperature and strain dependence of the tunneling current, which has not been reported before. In general, bandgap E_G narrowing of silicon (Si) due to uniaxial tensile stress leads to drain current I_{DS} enhancement, while uniaxial compressive stress reduced I_{DS}. The positive temperature coefficient of I_{DS} at low drain bias V_{DS} is due to temperature-induced E_G reduction, and the negative temperature coefficient at higher V_{DS} is due to increased channel resistance which reduces the effective electrical field at the tunneling junction for a given V_{DS}. These results provide guidance for the design of strained TFETs and are also useful for understanding the band-to-band tunneling (BTBT) mechanism in TFETs.

Exploiting heterostructure with staggered (or type II) band alignment at the tunneling junction is a promising approach to realize TFET with high on-state current I_{ON} and small subthreshold swing S. TFETs with two novel heterostructures ($Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}/Si$ and $Ge/In_{0.53}Ga_{0.47}As$) were demonstrated. In the TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}/Si$ heterostructure, the strained $Si_{0.989}C_{0.011}$ layer reduces the tunneling barrier width and contributes to a steep p^+ doping profile of 3 nm/decade, leading to a ~20% enhancement in I_{ON} and ~26% reduction in S as compared to TFET without the $Si_{0.989}C_{0.011}$ layer. For TFET with $Ge/In_{0.53}Ga_{0.47}As$ heterostructure, high source doping concentration (3×10^{20} cm^{-3}) with abrupt doping profile and direct BTBT were achieved, which are beneficial for I_{ON} and S of TFETs. Various process integration challenges for realizing such a TFET were identified and addressed.

High-mobility $Ge_{1-x}Sn_x$ MOSFET is another promising candidate for V_{DD} reduction in future technology nodes. To take full advantage of $Ge_{1-x}Sn_x$ as a channel material, a high-quality and thermodynamically stable gate stack has to be realized. Surface passivation technique using low-temperature Si_2H_6 treatment was investigated. By increasing the thickness of Si passivation layer from 4 to 7 monolayers, effective hole mobility μ_{eff} at an inversion carrier density of 1×10^{13} cm^{-2} was improved by ~19%. $Ge_{0.97}Sn_{0.03}$ pMOSFETs with post metal annealing (PMA) show improved intrinsic transconductance $G_{m,int}$, S, and μ_{eff} as compared to the control devices without PMA. In addition, $Ge_{1-x}Sn_x$ n-channel MOSFETs with low-temperature Si passivation were demonstrated. This was the first demonstration of Si passivation for $Ge_{1-x}Sn_x$ n-channel MOSFETs.

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Symbol	Description	Unit
A_G	Gate area	cm^2
a	Distance between inner and outer rods	cm
C	Capacitance	F/cm^2
C_{11}	Elastic constant	Pa
C_{12}	Elastic constant	Pa
C_{acc}	Capacitance in the accumulation layer	F/cm^2
C_D	Depletion capacitance	F/cm^2
C_{HfO_2}	Capacitance due to HfO_2	F/cm^2
C_{inv}	Capacitance in the inversion layer	F/cm^2
C_{it}	Capacitance associated with interface traps	F/cm^2
C_{OX}	Gate oxide capacitance	F/cm^2
C_{Si}	Capacitance due to Si	F/cm^2
C_{SiO_2}	Capacitance due to SiO_2	F/cm^2
D_{it}	Interface trap density	$cm^{-2}eV^{-1}$
E	Electron energy	eV
E_C	Energy of conduction band edge	eV
E_{CL}	Binding energy of the core-level electron	eV
E_G	Bandgap	eV
E_V	Energy of valence band edge	eV
f	Frequency	Hz
F_C	Fermi-Dirac distribution function for electron	-
F_V	Fermi-Dirac distribution function for hole	-
G_{BTBT}	Band-to-band tunneling generation rate	$cm^{-3}s^{-1}$
$G_{m,int}$	Intrinsic transconductance	S/μm
g_c	Density of states in the conduction band	$eV^{-1}cm^{-3}$
g_v	Density of states in the valence band	$eV^{-1}cm^{-3}$

$\hbar$	Reduced Planck's constant	eV·s
I_{BTBT}	Band-to-band tunneling current	A
I_{CP}	Charge pumping current	A
I_D	Drain current	A/μm
I_{DS}	Drain-to-source current	A/μm
I_{DSat}	Saturation drain current	A/μm
$I_{DS,\max}$	Largest output current	A
$I_{DS,\min}$	Smallest output current	A
$I_{DS,nom}$	Nominal output current	A
I_{OFF}	Off-state current	A/μm
I_{ON}	On-state current	A/μm
I_S	Source current	A/μm
k	Boltzmann constant	eV/K
L	Distance between the two outer rods	cm
L_{CH}	Channel length	μm
L_G	Gate length	μm
$L_{OV,GD}$	Length of gate-to-drain overlap	μm
$L_{OV,GS}$	Length of gate-to-source overlap	μm
L_T	Length of tunneling path	nm
m_e^*	Electron effective mass	kg
m_h^*	Hole effective mass	kg
m_r	Reduced tunneling mass	kg
n	Electron concentration	cm^{-3}
N_A	Acceptor concentration	cm^{-3}
N_{inv}	Inversion carrier density	cm^{-2}
N_D	Donor concentration	cm^{-3}
n_i	Intrinsic carrier concentration	cm^{-3}
n_s	Surface concentration of minority carrier	cm^{-3}
P_{Active}	Active Power	W
$P_{Passive}$	Passive Power	W
Q_f	Fixed oxide charge	C
q	Elementary charge	C
$R_{Channel}$	Channel resistance	Ω
R_D	Drain resistance	Ω

R_S	Source resistance	Ω
R_{total}	Total resistance	Ω
R_{Tunnel}	Tunneling junction resistance	Ω
r_c	Backscattering coefficient	-
S	Subthreshold swing	mV/decade
$S_{T,eff}$	Effective temperature sensitivity	ppm/K
t	Thickness	μm
T	Temperature	K
t_f	Fall time	s
$T_{\max}$	Maximum of the applied temperature	K
$T_{\min}$	Minimum of the applied temperature	K
T_{OX}	Thickness of SiO_2	nm
t_r	Rise time	s
V	Voltage	V
V_a	Voltage amplitude	V
V_{base}	Base level voltage	V
V_{DD}	Supply voltage	V
V_{DS}	Drain voltage	V
V_{FB}	Flatband voltage	V
V_{GS}	Gate voltage	V
V_{leak_floor}	Maximum gate voltage in the off-state leakge floor region	V
V_{TH}	Threshold voltage	V
v_T	Thermal velocity	m/s
W	Gate width	μm
Y	Young's modulus	Pa
y	Vertical displacement	cm
$\Delta\omega$	Raman shift	cm^{-1}
ΔE_C	Conduction band offset	eV
ΔE_G	Bandgap narrowing	eV
ΔE_{CL}^{i}	Core-level binding energy different between two materials at the interface	eV
ΔE_V	Valence band offset	eV
ΔI_{DS}	Change in drain current	μA/μm

ΔL_G	Difference in the gate length	μm
ΔR_{total}	Difference in the total resistance	Ω
$\varepsilon_{tension}$	Uniaxial tensile strain	-
$\varepsilon_{//}$	Biaxial tensile strain	-
ε_{xx}	Lateral strain	-
μ_{eff}	Effective mobility	$cm^2/V{\cdot}s$
ξ	Electric field	V/cm
ξ_{eff}	Effective vertical electric field	V/cm
σ	Stress	Pa
σ_n	Capture cross section of electron	cm^{-2}
σ_p	Capture cross section of hole	cm^{-2}
τ_d	Time delay	s
ω_o	Raman frequency in bulk sample	cm^{-1}

List of Abbreviations

AFM	Atomic force microscopy
Ag	Silver
Al_2O_3	Aluminum oxide
Al	Aluminum
ALD	Atomic layer deposition
As	Arsenic
AsH_3	Arsine
Au	Gold
BJT	Bipolar junction transistor
BOE	Buffered oxide etch
BTBT	Band-to-band tunneling
C	Carbon
CET	Capacitance equivalent thickness
Cl_2	Chlorine
CMOS	Complementary metal-oxide-semiconductor
Cu	Copper
DHF	Dilute hydrofluoric acid
DOS	Density-of-states
EOT	Equivalent oxide thickness
FB-FET	Feedback field-effect transistor
FGA	Forming gas annealing
Ga	Gallium
Ge	Germanium
GeH_4	Germane
GeSn	Germanium-tin
H_2O_2	Hydrogen peroxide
H_2SO_4	Sulfuric acid
HCl	Hydrochloric acid
HfO_2	Hafnium dioxide
HH	Heavy-hole
IC	Integrated circuit
I-MOS	Impact-ionization metal-oxide-semiconductor

ITRS	International Technology Roadmap for Semiconductors
LH	Light-hole
MBE	Molecular beam epitaxy
ML	Monolayer
MOCVD	Metal-organic chemical vapor deposition
MOSFET	Metal-oxide-semiconductor field-effect transistor
N_2	Nitrogen
NH_4OH	Ammonium hydroxide
Ni	Nickel
Ni(GeSn)	Nickel stanogermanide
nMOSFET	N-channel metal-oxide-semiconductor field-effect transistor
nTFET	N-channel tunneling field-effect transistor
PECVD	Plasma enhanced chemical vapor deposition
PMA	Post metal annealing
pMOSFET	P-channel metal-oxide-semiconductor field-effect transistor
RMS	Root-mean-square
RTA	Rapid thermal annealing
sccm	Standard cubic centimeters per minute
SEM	Scanning electron microscope
SF_6	Sulfuric hexafluoride
Si	Silicon
Si_2H_6	Disilane
Si_3H_8	Trisilane
SiGe	Silicon-germanium
SIMS	Secondary ion mass spectrometry
SiO_2	Silicon dioxide
Sn	Tin
SO	Spin-orbit-split-hole
SOI	Silicon-on-insulator
SPM	Sulfuric peroxide mixture
SRH	Shockley-Read-Hall
STT	Surface tunnel transistor

S/D	Source/drain
TaN	Tantalum nitride
TEM	Transmission electron microscope
TFET	Tunneling field-effect transistor
TMGa	Trimethylgallium
UHVCVD	Ultra-high-vacuum chemical vapor deposition
VB	Valence band
XRD	X-ray diffraction
XPS	X-ray photoelectron spectroscopy
$(NH_4)_2S$	Ammonia sulfide

Chapter 1

Introduction

1.1 Background

Continuous scaling of the complementary metal-oxide-semiconductor (CMOS) devices has allowed the number of transistors in an integrated circuit (IC) to approximately double every two years [1]. While the scaling enables higher packaging density per unit chip area and increased circuit speed, it also causes high power consumption in an IC chip, which has become a serious issue as the technology advances [2]-[3]. The power consumption of an IC has two components, active power P_{Active} and passive power $P_{Passive}$, which are given by

$$P_{Active} \propto V_{DD}^2 \cdot f \,, \tag{1.1}$$

$$P_{Passive} \propto I_{OFF} \cdot V_{DD} \,, \tag{1.2}$$

where V_{DD} is the supply voltage, f is the frequency of the circuit, and I_{OFF} is the off-state current of a transistor. Because both P_{Active} and $P_{Passive}$ strongly depend on V_{DD}, scaling-down of V_{DD} is the most effective approach to reduce the power consumption. However, it should be noted that the reduction of V_{DD} alone will cause a decrease in on-state current I_{ON}. As a result, the switching speed of the circuit will be lowered as the switching speed is inversely proportional to the time delay τ_d, which is given by

$$\tau_d \propto \frac{V_{DD}}{I_{ON}}. \tag{1.3}$$

Therefore, V_{DD} reduction without compromising I_{ON} is compulsory for future low power logic applications. For this purpose, two promising technical approaches are explored in this thesis. The first one is to use novel transistors with steep switching characteristics. Another approach is to use devices with high-mobility channel materials. In the following sections, the technological relevance of these two approaches will be discussed in detail.

1.2 Transistor with Steep Switching Characteristics

In a conventional metal-oxide-semiconductor field-effect transistor (MOSFET), the threshold voltage V_{TH} has to be reduced in order to scale down V_{DD} without compromising I_{ON}. However, reducing V_{TH} without scaling the subthreshold swing S will lead to a high I_{OFF} as illustrated in Fig. 1.1. This high I_{OFF} will increase the passive power consumption according to Equation (1.2). In order to address this problem, S of a MOSFET should be lowered at a given I_{ON}. For a conventional n-channel MOSFET (nMOSFET) [Fig. 1.2(a)], the minimum S is determined by the energy distribution of electrons in the source which follows Fermi-Dirac distribution [Fig. 1.2(b)]. Mathematically, S is calculated by

$$S = \ln 10 \frac{kT}{q}\left(1 + \frac{C_D + C_{it}}{C_{OX}}\right) > \ln 10 \frac{kT}{q}, \tag{1.4}$$

where k is the Boltzmann constant, T is the temperature, q is the electronic charge, C_D is the depletion capacitance, C_{OX} is the gate oxide capacitance, and C_{it} is the

capacitance associated with interface traps. According to this Equation, the minimum S of a conventional MOSFET at room temperature (T = 300 K) is 60 mV/decade.

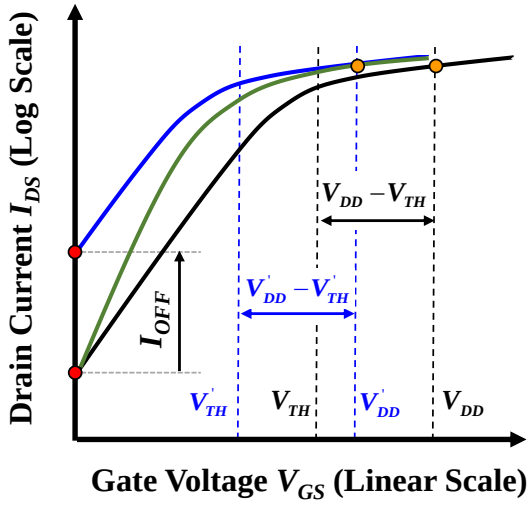


Fig. 1.1. The black curve shows the drain current - gate voltage (I_{DS} - V_{GS}) characteristics of an unscaled MOSFET. As V_{DD} scales down, V_{TH} needs to be reduced in order to maintain the on-state current I_{ON} at the same gate overdrive ($V_{DD} - V_{TH} = V'_{DD} - V'_{TH}$). However, scaling-down of V_{DD} and V_{TH} without reducing S will cause a high I_{OFF} as illustrated by the blue curve. The green curve indicates that the S of the transistor has to be reduced to maintain a low I_{OFF}.

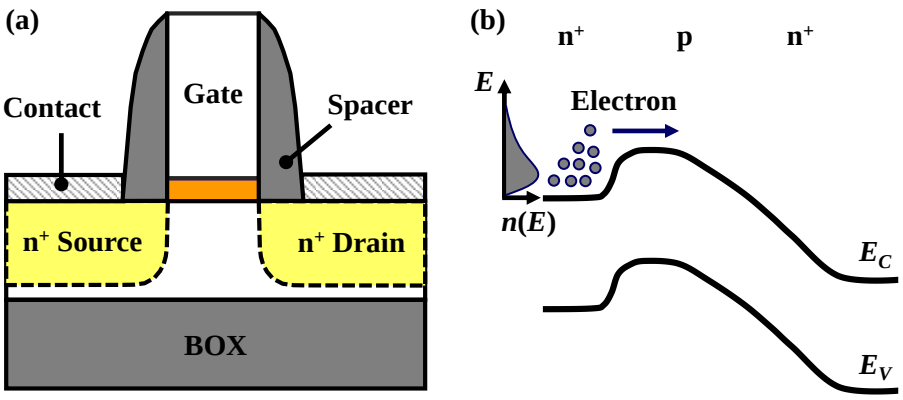


Fig. 1.2. (a) Schematic of a conventional n-channel MOSFET. (b) The energy band diagram along the source-to-drain direction when the MOSFET is at on-state. Fermi-Dirac distribution of the electron concentration in the energy scale $n(E)$ in the source region is illustrated. The electrons in the high energy tail can surmount the energy barrier between source and channel, causing the S of a MOSFET to be higher than 60 mV/decade at room temperature. E_C and E_V are the energies of conduction band edge and valence band edge, respectively.

To achieve *S* smaller than 60 mV/decade, novel transistors with steep switching characteristics have been proposed and explored recently, such as impact-ionization metal-oxide-semiconductor (I-MOS) device [4]-[7], feedback field-effect transistor (FB-FET) [8]-[9], mechanical gate field-effect transistor [10]-[12], and tunneling field-effect transistor (TFET) [13]-[67]. However, some disadvantages are identified for the first three candidates, which hinder their application in circuits. For I-MOS, rapid device degradation remains a concern due to the carrier trapping and creation of interface states over time. In FB-FET, the static power consumption is high as the p^+-i-n^+ diode works in the forward bias regime [8]-[9]. For mechanical gate field-effect transistor, the high operating voltage and intrinsic delay limit its potential applications. In contrast to these three device designs, TFET exploits the gate-controlled band-to-band tunneling (BTBT) mechanism to achieve an *S* less than 60 mV/decade at room temperature. It is projected that V_{DD} of TFET can be well below 0.5 V based on theoretical calculations [51],[48]-[49],[67]. Besides the low V_{DD}, TFET can offer extremely low off-state current. These two merits make TFET the most promising candidate for future ultra-low power applications. In this thesis work, TFET is explored as one approach (device with steep switching characteristics) to address the power consumption issue.

1.2.1 Development of Tunneling Field-Effect Transistor

The phenomenon of BTBT was discovered by Leo Esaki in 1957 [68]. Following the discovery, there has been considerable work done since the 1970s to investigate tunneling transistors. The first lateral surface tunnel transistors (STTs) were proposed by Baba and Uemura based on III-V compound semiconductors in 1992 [69]-[70]. Similar STTs based on silicon (Si) were then demonstrated by Reddick [71] in 1995 and by Koga [72] in 1999. However, both I_{ON} and S of the fabricated devices were very poor. In 2004, Bhuwalka [13] reported a vertical Si TFET employing a heavily doped p^+ delta layer at the tunneling junction, and demonstrated enhanced I_{ON} and steeper S. After that, many studies on Si- or germanium (Ge)-based TFETs have been reported [14],[16]-[17],[20],[22]-[24],[27],[29], [32]-[39] and devices with sub-60 mV/decade S were demonstrated [16],[33],[36]-[37],[39]. At the same time, a number of simulation works on the device design and physical understanding of TFET were performed [15],[18]-[19],[21],[25]-[26],[28], [30]-[31]. Recently, TFETs based on small bandgap III-V materials have attracted attention [47],[50],[52]-[55],[57]-[65]. The transfer characteristics of the key published experimental n-channel and p-channel TFETs are summarized in Fig. 1.3.

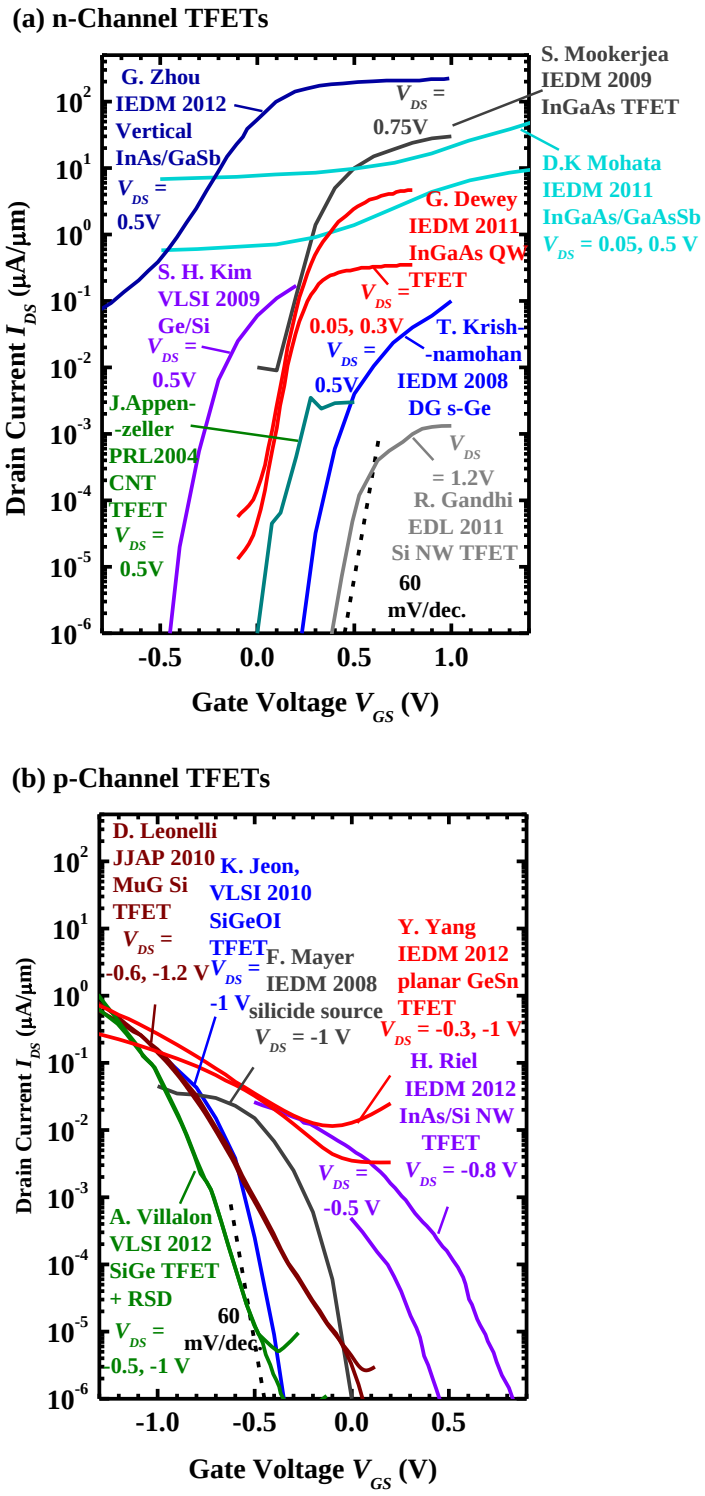


Fig. 1.3. The transfer characteristics of the key published experimental (a) n-channel TFETs and (b) p-channel TFETs.

1.2.2 Working Principle of TFET and Band-to-Band Tunneling

TFET is essentially a gated p-i-n diode, which works on the principle of gate-controlled band-to-band tunneling. Fig. 1.4(a) shows the schematic of an n-channel TFET (nTFET). In an nTFET, the source and drain are doped asymmetrically with p-type and n-type dopants, respectively. The gate controls the length of the tunneling

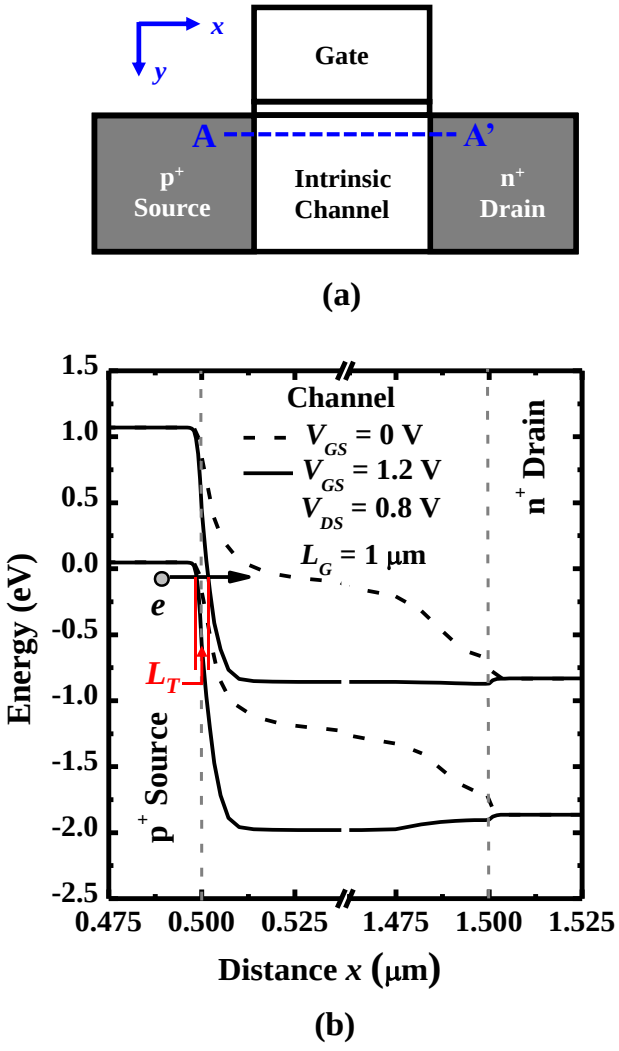


Fig. 1.4. (a) Schematic shows the structure of an n-channel TFET. (b) Simulated energy band diagrams at on-state (V_{GS} = 1.2 V) and off-state (V_{GS} = 0 V) along the source-to-drain direction as indicated by the dashed line A-A' in (a). For this simulation, the device parameters used were: acceptor concentration in the source $N_A = 1 \times 10^{20}$ cm^{-3}, donor concentration in drain $N_D = 1 \times 10^{20}$ cm^{-3}, body doping $N_A = 1 \times 10^{16}$ cm^{-3}, equivalent oxide thickness (EOT) = 0.8 nm, and L_G = 1 μm.

path L_T and hence the tunneling current. Fig. 1.4(b) shows the simulated energy band diagrams of a TFET at both off- and on-states along the line of A - A' in Fig. 1.4(a). In the absence of gate bias, L_T is large and I_{OFF} is determined by the reverse biased p-i-n leakage current. When a positive gate potential is applied, the energy bands in the channel region are lowered and L_T is reduced. Thus valence electrons in the source region will tunnel into the conduction band in the channel, forming the tunneling current [Fig. 1.4(b)].

BTBT is a quantum-mechanical phenomenon, where the valence electrons can tunnel through the forbidden energy gap to the conduction band and leave holes in the valence band. The BTBT generation rate G_{BTBT} can be estimated using Kane's model [73]

$$G_{BTBT} = A\frac{\xi^2}{\sqrt{E_G}}\exp\left(-B\frac{E_G^{3/2}}{\xi}\right), \tag{1.5}$$

where ξ is the electric field and E_G is the bandgap. $A = \frac{q^2 m_r^{1/2}}{18\pi\hbar^2}$ and $B = \frac{\pi m_r^{1/2}}{2q\hbar}$, where $\hbar$ is the reduced Planck's constant, and m_r is the reduced tunneling mass. m_r is related to the electron effective mass m_e^* and hole effective mass m_h^* by $\frac{1}{m_r} = \frac{1}{m_e^*} + \frac{1}{m_h^*}$.

The tunneling current I_{BTBT} depends on the G_{BTBT} and the relationship governing I_{BTBT} and G_{BTBT} is given by [74]

$$I_{BTBT} \propto \int_{E_V}^{E_C}[F_V(E) - F_C(E)]g_c(E)g_v(E)\cdot G_{BTBT}\cdot dE, \tag{1.6}$$

where E is the electron energy, $F_C(E)$ and $F_V(E)$ are the Fermi-Dirac distribution functions for electrons and holes, respectively; $g_c(E)$ and $g_v(E)$ are the density of states in the conduction band and the valence band, respectively. Therefore, a high

electric field at the tunneling junction and materials with small bandgap are required to achieve high G_{BTBT} and I_{BTBT}.

1.2.3 Design Considerations of TFET

Although TFETs have been experimentally realized by many groups, the I_{ON} of TFETs still cannot meet the drive current requirement in the International Technology Roadmap for Semiconductors (ITRS) for low power logic applications [75]. Research efforts to further improve the I_{ON} of TFETs and, at the same time, realize sub-60 mV/decade S are required. The key design considerations of TFET are summarized in Fig. 1.5. In the following sub-sections, each of the key design considerations will be discussed.

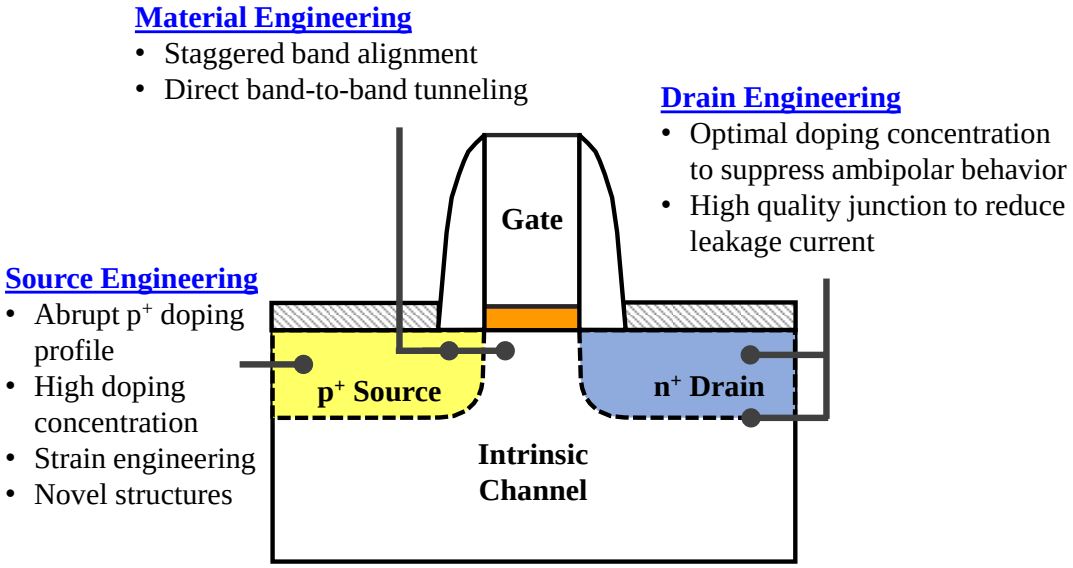


Fig. 1.5. Schematic illustrates the key challenges and design considerations for TFET.

1.2.3.1 Material Engineering

According to Kane's model in Equation (1.5), G_{BTBT} has an exponential dependence on the E_G of the material at the tunneling junction. To achieve high G_{BTBT} and I_{ON}, a material with small E_G is preferred, such as Ge (E_G = 0.66 eV) and III-V materials (for example, InAs with E_G of 0.35 eV). However, E_G of the channel material should not be too small; otherwise, the TFET may suffer from a high off-state leakage current.

Considering the requirements discussed above, employing a heterostructure with staggered (or type II) band alignment at the tunneling junction is a promising approach to realize TFET with high I_{ON} and small S. Compared with a homostructure, a heterostructure with staggered band alignment can reduce the L_T, leading to a higher tunneling current as illustrated in Fig. 1.6. In addition, a low I_{OFF} can be achieved by using a channel material with a large E_G. In this thesis, TFETs with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}/Si$ and $Ge/In_{0.53}Ga_{0.47}As$ heterostructures are fabricated and their electrical characteristics are investigated in detail.

Besides the staggered band alignment, direct BTBT is also desired to achieve a high I_{ON}. It was reported that the tunneling probability of direct BTBT is higher than that of indirect BTBT [76]. This is because indirect BTBT requires the assistance of phonons for the conservation of momentum. For the TFET with $Ge/In_{0.53}Ga_{0.47}As$ heterostructure, direct BTBT is achieved as the $In_{0.53}Ga_{0.47}As$ in the channel is a direct bandgap material. Therefore, valence band electrons in the Ge source can tunnel directly into the conduction band in $In_{0.53}Ga_{0.47}As$ channel without the assistance of phonons.

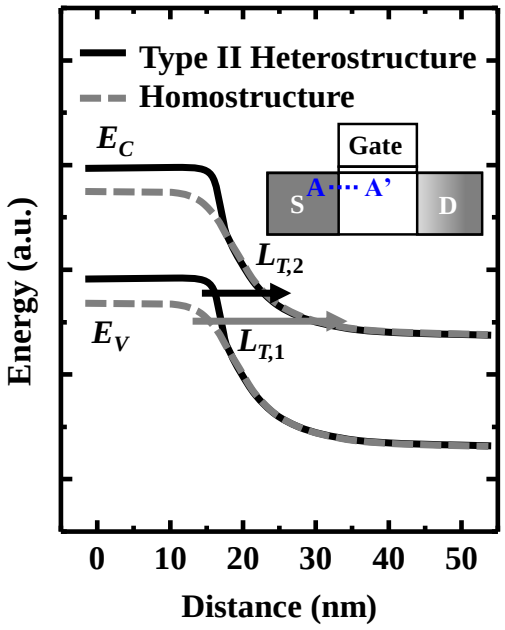


Fig. 1.6. Schematic of energy band diagrams along source-to-drain direction at the tunneling junction regions in two TFETs. The first TFET has a homojunction where the tunneling path length is $L_{T,1}$. The second TFET has a heterojunction with staggered band alignment, and the tunneling path length $L_{T,2}$ is smaller than $L_{T,1}$ under the same bias condition.

1.2.3.2 Source Engineering

In addition to the requirement of small E_G, a high electric field at the tunneling junction is also required to achieve a high I_{ON}. Processing techniques, such as dopant steepening implant [32] and dopant segregation [33], have been demonstrated to realize an abrupt source doping profile and a high electric field at the tunneling junction. In addition, the p^+ doping concentration in the source should be sufficiently high to achieve a small S and a high I_{ON} [19]. In the design of TFETs with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}/Si$ and $Ge/In_{0.53}Ga_{0.47}As$ heterostructures, the requirements of abrupt doping profile and high source doping concentration are taken into consideration.

Strain engineering of the source/channel interface can also be employed to boost the I_{ON} of TFETs, as strain causes the splitting of the energy bands and reduces L_T [29],[77]. In this thesis, the strain dependence of the tunneling current is investigated, which provides important guidance on how TFETs should be strain-engineered.

1.2.3.3 Drain Engineering

The doping concentration in the drain region needs to be carefully designed. A high doping concentration is required to achieve a low series resistance in the drain region. However, high doping concentration can cause ambipolar phenomenon due to the drain-side tunneling, leading to a high I_{OFF} [19],[24],[78]. Therefore, drain doping concentration should be optimized to suppress the ambipolar behavior and yet achieve acceptable series resistance. In addition, the defect density at the drain-body junction should be minimized to suppress I_{OFF}.

1.3 Transistor with High-Mobility Channel Material

As discussed in Section 1.1, the other technical approach to achieve V_{DD} reduction without compromising I_{ON} is to adopt MOSFETs with high-mobility channel materials. As transistors are scaled into deep sub-100 nm regime, quasi-ballistic transport dominates the drive current of the devices. In quasi-ballistic regime, the saturation drain current I_{Dsat} of a MOSFET is limited by the thermal injection velocity and is given by [79]

$$I_{Dsat} = C_{OX} W v_T \left(\frac{1 - r_c}{1 + r_c} \right) \left(V_{GS} - V_{TH} \right), \tag{1.7}$$

where W is the gate width of a transistor, v_T is the thermal injection velocity, and r_c is the backscattering coefficient. It has been found that a higher low field effective mobility μ_{eff} contributes to a larger v_T [80]. Therefore, it is desired to incorporate materials with high μ_{eff} to achieve a high I_{Dsat} as transistors scale down. For example, Ge and III-V compound semiconductors are good candidates for this approach.

The bulk carrier mobilities of some common semiconductors are listed in Table 1.1. Among all the semiconductors, Ge offers the highest hole mobility (1900 $cm^2/V \cdot s$) and decent electron mobility (3900 $cm^2/V \cdot s$). Recently, germanium-tin ($Ge_{1-x}Sn_x$) has attracted great interests as it has even higher carrier mobility than Ge due to the incorporation of substitutional tin (Sn) [81]. Ge- or $Ge_{1-x}Sn_x$-based group IV materials have better compatibilities with the current Si CMOS processing technologies, as compared to III-V compound semiconductors. This enables easier integration of Ge or $Ge_{1-x}Sn_x$ into current Si platform and helps to reduce the cost of

Table 1.1. Electron and hole mobilities of some common semiconductors at room temperature.

Material Properties	Si	Ge	GaAs	InAs	InSb
Electron Mobility ($cm^2/V{\cdot}s$)	1600	3900	9200	40000	77000
Hole Mobility ($cm^2/V{\cdot}s$)	430	1900	400	500	850

introducing new materials. Therefore, $Ge_{1-x}Sn_x$ MOSFETs are developed as another technical option (device with high-mobility channel material) to reduce the high power consumption of an IC chip.

For $Ge_{1-x}Sn_x$ MOSFETs, one of the most critical issues is the poor quality of the native oxides of $Ge_{1-x}Sn_x$ as compared with silicon dioxide (SiO_2) in Si MOSFETs. The high interface trap density D_{it} in the gate stack causes Fermi-level pinning, increases S, degrades the carrier mobility, and creates reliability issues. To fully exploit the benefits of $Ge_{1-x}Sn_x$ alloy, a high-quality and thermodynamically stable gate stack has to be realized.

Surface passivation techniques have been developed to improve the gate dielectric and $Ge_{1-x}Sn_x$ interface quality. $Ge_{1-x}Sn_x$ p-channel MOSFETs (pMOSFETs) with low-temperature Si surface passivation have been demonstrated [82]-[84]. For Si passivated $Ge_{0.947}Sn_{0.053}$ pMOSFETs, a hole mobility of 220 $cm^2/V{\cdot}s$ at an effective vertical electric field ξ_{eff} of 1 MV/cm has been achieved, which is ~55% higher than that of Ge pMOSFETs [82]. $Ge_{0.958}Sn_{0.042}$ pMOSFETs with aqueous ammonia sulfide [$(NH_4)_2S$] passivation were also reported with a high peak hole mobility of 509 $cm^2/V{\cdot}s$ [85]. However, the hole mobility of GeSn pMOSFET with $(NH_4)_2S$ passivation at high electric field is much lower than that with Si passivation.

Therefore, Si passivation is a promising surface treatment technique for $Ge_{1-x}Sn_x$ pMOSFETs. In this thesis, further optimization of the electrical performance of Si passivated $Ge_{1-x}Sn_x$ pMOSFETs is explored by varying the Si passivation layer thickness and post metal annealing condition.

Although $Ge_{1-x}Sn_x$ pMOSFETs with high drive current have been realized, the performance of $Ge_{1-x}Sn_x$ nMOSFETs is still poor and surface passivation techniques are still not well developed. There are only few studies on $Ge_{1-x}Sn_x$ nMOSFETs to date. The $Ge_{0.976}Sn_{0.024}$ nMOSFET demonstrated by Han *et al*. [86] employed $GeSnO_2$ surface passivation formed by a rapid thermal oxidation (RTO) process at 400℃. However, Sn condensation may occur in this process, which can affect the inversion carrier mobility and the *S* of the transistor. GeSn nMOSFETs with Ge capping layer and ozone oxidation were also demonstrated [87]-[88]. Although D_{it} is reduced significantly with the addition of the Ge capping layer, the drive currents of the reported $Ge_{1-x}Sn_x$ nMOSFETs are still much lower than that of $Ge_{1-x}Sn_x$ pMOSFETs. Therefore, further improvement in the drive current of $Ge_{1-x}Sn_x$ nMOSFETs is needed. This requires the development of advanced surface passivation techniques to achieve high-quality gate stack.

1.4 Objectives of Research

The main objective of this thesis is to explore various technology options to enable the reduction of V_{DD} in an IC chip for future technology nodes. This is achieved by employing transistors with novel structure (TFET) and high-mobility MOSFETs ($Ge_{1-x}Sn_x$ MOSFETs). In TFET, the device physics such as the temperature and strain dependence of the tunneling current is studied. TFETs with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}/Si$ and $Ge/In_{0.53}Ga_{0.47}As$ heterostructures are fabricated and characterized, which are promising structures to achieve high I_{ON} and steep S. In $Ge_{1-x}Sn_x$ MOSFETs, gate stack optimization for Si passivated $Ge_{1-x}Sn_x$ pMOSFETs is investigated by varying the Si passivation layer thickness and post metal annealing condition. $Ge_{1-x}Sn_x$ nMOSFETs with Si passivation are also demonstrated. The results of this thesis are part of the research efforts in V_{DD} reduction to sustain the continuous development of the semiconductor industry.

1.5 Outline of Thesis

The main technical contents discussed in this thesis are documented in four Chapters.

Chapter 2 reports the effects of strain and temperature on the tunneling current and discusses the underlying device physics. Based on the unique temperature dependence of the tunneling current, a current biasing circuit employing TFET is proposed, which can achieve a low temperature sensitivity.

Chapter 3 explores the source/channel interface engineering for TFETs with $Si_{0.5}Ge_{0.5}$-source and Si-channel by inserting an undoped $Si_{0.989}C_{0.011}$ layer underneath the $Si_{0.5}Ge_{0.5}$-source. Finite element simulation is employed to examine the strain distribution in the $Si_{0.989}C_{0.011}$ layer and the effects of this layer on the I_{ON} and S of TFETs are investigated. The presence of the strain in the $Si_{0.989}C_{0.011}$ layer increases the conduction band offset between $Si_{0.5}Ge_{0.5}$ and $Si_{0.989}C_{0.011}$ layer, which effectively reduces the tunneling barrier. In addition, the $Si_{0.989}C_{0.011}$ layer suppresses boron diffusion, which helps to realize a steeper boron profile. Electrical results of the fabricated transistors are discussed in detail to affirm the effectiveness of the inserted $Si_{0.989}C_{0.011}$ layer.

Chapter 4 investigates TFETs with novel Ge/$In_{0.53}Ga_{0.47}As$ heterojunction as the tunneling junction. Device concept is explained and the advantages of TFETs with Ge/$In_{0.53}Ga_{0.47}As$ heterojunction are demonstrated using simulation. Process integration and fabrication of such TFETs are described. The band alignment between Ge and $In_{0.53}Ga_{0.47}As$ is measured to identify the band offset between these two materials. The electrical performance of the devices is discussed and the device physics is analyzed by performing multi-temperature measurements.

Chapter 5 summarizes the results of $Ge_{1-x}Sn_x$ MOSFETs with low-temperature Si passivation. The effects of Si passivation layer thickness and post metal annealing temperature on the I_{ON}, S, and μ_{eff} of $Ge_{0.97}Sn_{0.03}$ pMOSFETs are discussed. $Ge_{0.976}Sn_{0.024}$ nMOSFETs with low-temperature Si passivation are demonstrated for the first time. The device performance is benchmarked with those passivated using

$GeSnO_2$. The main issues of the $Ge_{1-x}Sn_x$ nMOSFETs and possible methods to further improve the I_{ON} of the devices are discussed.

An overall conclusion and possible future work are furnished in Chapter 6.

Chapter 2

Study of Strain and Temperature Dependence of Tunneling Current for Tunneling Field-Effect Transistor (TFET)

2.1 Introduction

As discussed in Chapter 1, the device physics of tunneling field-effect transistor (TFET) is different from that of metal-oxide-semiconductor field-effect transistor (MOSFET). Efforts have been devoted to device structure and material optimization to boost the on-state current I_{ON} of TFET [14]-[16],[19],[21],[44],[71],[89]-[92], but there is still a lack of investigation into TFET device physics. There are only a few reports of the dependence of TFET characteristics on stress or strain [30],[77],[93]-[94]. There is also lack of systematic study on the temperature dependence of the electrical characteristics of TFET [50].

In this Chapter, we report the first study of the dependence of the electrical characteristics of TFET on strain under various bias conditions, as well as an examination of the underlying physics of the TFET device by observing the dependence of its current on temperature [29]. Knowing the dependence of TFET performance on applied stress would provide important guidance on how it can be

strain-engineered and also lead to improved understanding of the band-to-band tunneling mechanism. In addition, a temperature independent current biasing circuit, which exploits the unique temperature dependence of TFET, was explored. The proposed circuit can achieve a low temperature sensitivity within ± 120 ppm/K.

2.2 Strain Dependence of Tunneling Current

Double-gate n-channel TFETs as shown in Fig. 2.1 were used for this study. The TFETs were fabricated by a former Ph.D student (Dr. Eng-Huat Toh) in Prof. Yeo's group. For the work in Sections 2.2 and 2.3, the contribution of the author of this thesis is in the characterization and physical study, and not in the device fabrication.

The TFETs were fabricated on 8-inch (001)-oriented silicon (Si)-on-insulator (SOI) substrates, and have gate lengths L_G ranging from 1 to 5 μm. After a reactive ion etch step to define the Si fins, a portion of the silicon dioxide (SiO_2) beneath the fin was etched to facilitate the formation of top-and-bottom gates. After pre-gate cleaning, thermal oxidation at 850 °C was used to form 3 nm SiO_2 gate dielectric. A 100 nm poly-Si film was then deposited by low-pressure chemical vapor deposition system and patterned to form the gate electrode. Photolithography was performed to open the source region. BF_2^+ implantation with a dose of 1×10^{15} cm^{-2} and an energy of 7 keV was done to form the source. Drain was formed by masked As^+ implantation with a dose of 5×10^{14} cm^{-2} and an energy of 6 keV. Dopant activation

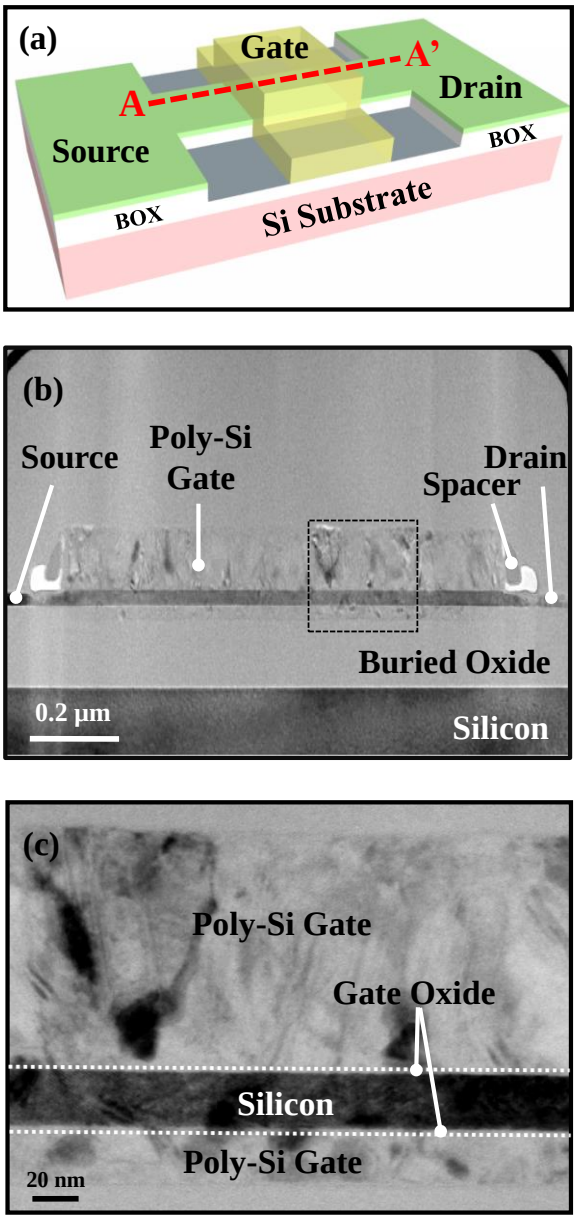


Fig. 2.1. (a) Schematic of a double-gate TFET. (b) TEM image of a TFET device with L_G of 1 µm measured in this experiment. The source-to-drain orientation of the TFET is along [110] direction. Thickness of thermal SiO_2 gate dielectric T_{OX} is 3 nm. 100 nm poly-Si gate electrode was formed by low-pressure chemical vapor deposition. (c) TEM image of the gate stack indicated by the dashed box in (b). The thickness of the body Si is 25 nm as measured from the TEM image. The top and bottom gates are connected together.

was carried out using rapid thermal annealing (RTA) system at 950 °C for 30 s. After that, 20 nm thick silicon nitride layer was deposited to form the gate spacers. Nickel silicide was formed by depositing 10 nm nickel and annealing at 450 °C for 30 s.

Finally, aluminum contacts were formed. Fig. 2.1(a) shows the schematic of a double-gate TFET measured in this experiment. Transmission electron microscope (TEM) analysis was performed along A-A' direction and the cross-sectional view of the TFET is shown in Fig. 2.1(b). The channel orientation of the TFET is along [110] direction. Fig. 2.1(c) shows the zoomed-in view of the gate stack indicated by the dashed box in Fig. 2.1(b), from which the top and bottom gates can be clearly observed. The thickness of the body Si is 25 nm as measured from the TEM image.

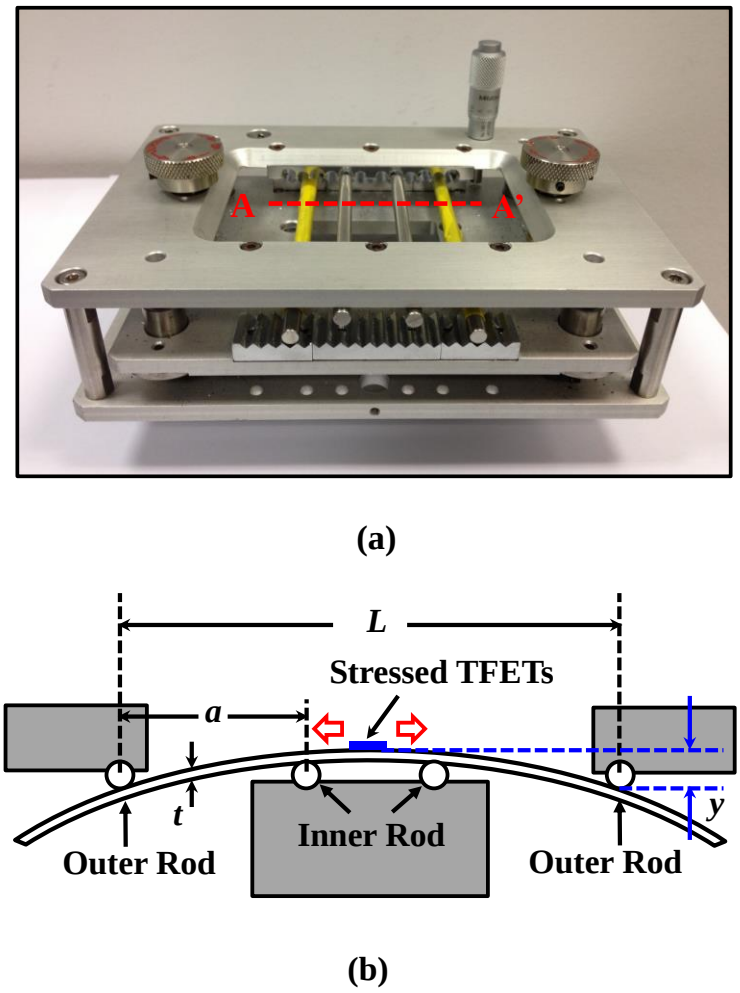


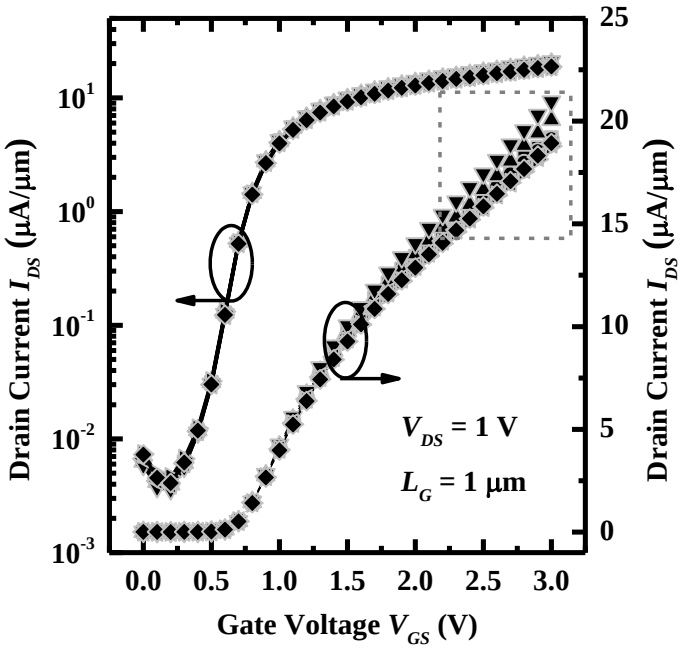
Fig. 2.2. (a) Image of the four-point wafer bending apparatus. (b) Schematic of the wafer bending apparatus along A-A' direction as indicated in (a). Tensile stress is applied to the wafer strip as illustrated. With the same setup, compressive stress can also be applied by bending the wafer strip in opposite direction. The dimension of the wafer strip that this setup can accommodate is 5 ~ 8 cm in length and less than 2 cm in width.

To evaluate the impact of strain on TFET I_{DS} - V_{GS} characteristics, mechanical stress along the channel direction [110] was applied through a four-point wafer bending apparatus as illustrated in Fig. 2.2. The stress σ in the horizontal direction can be calculated by measuring the vertical displacement of the wafer strip using

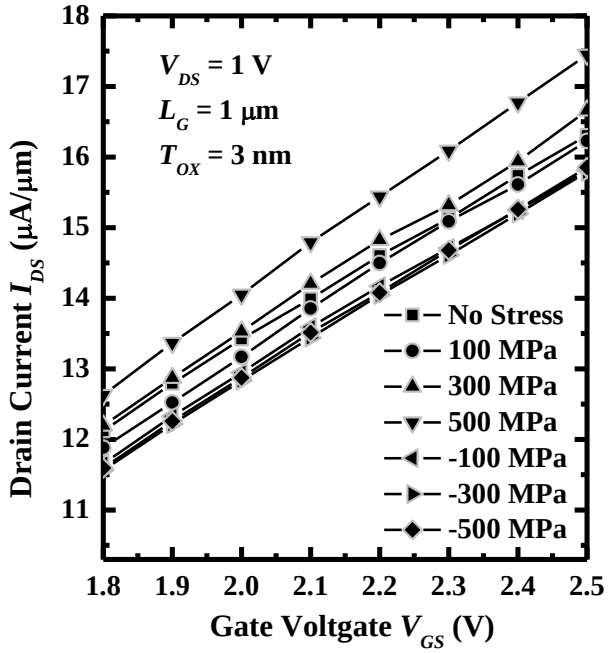
$$\sigma = \frac{YLty}{4a^2\left(\frac{L}{2} - \frac{2a}{3}\right)}, \tag{2.1}$$

where Y is the Young's modulus, L is the distance between the two outer rods, a is the distance between the inner and outer rods, t is the total thickness of the sample and y is the vertical displacement of the wafer strip, which was measured during the experiment. The stress applied ranged from - 500 MPa (compressive) to 500 MPa (tensile).

Strain dependence of the tunneling current is shown in Fig. 2.3. Fig. 2.3(a) shows the I_{DS} - V_{GS} characteristics of a TFET with L_G of 1 μm under different strain conditions at a drain voltage V_{DS} = 1 V. Fig. 2.3(b) is a zoomed-in view of the I_{DS} - V_{GS} curves indicated by the dashed box in Fig. 2.3(a). The ΔI_{DS} / I_{DS} in Fig. 2.4 represents the fractional change in I_{DS} due to stress. When tensile stress is applied, ΔI_{DS} / I_{DS} decreases in the low stress regime followed by a large increase at larger stress. A 4% I_{DS} enhancement is observed at a tensile stress of 500 MPa. However, a decrease in I_{DS} is observed when compressive stress is applied.



(a)



(b)

Fig. 2.3. (a) Linear and log-linear plot shows the I_{DS} - V_{GS} characteristics of a TFET at different strain conditions for V_{DS} = 1 V. (b) Zoomed-in view of the I_{DS} - V_{GS} curves indicated by the dashed box in (a). The legend for each curve is shown in (b). Negative and positive signs are used for compressive and tensile stress, respectively. (a) and (b) have the same legend for each curve.

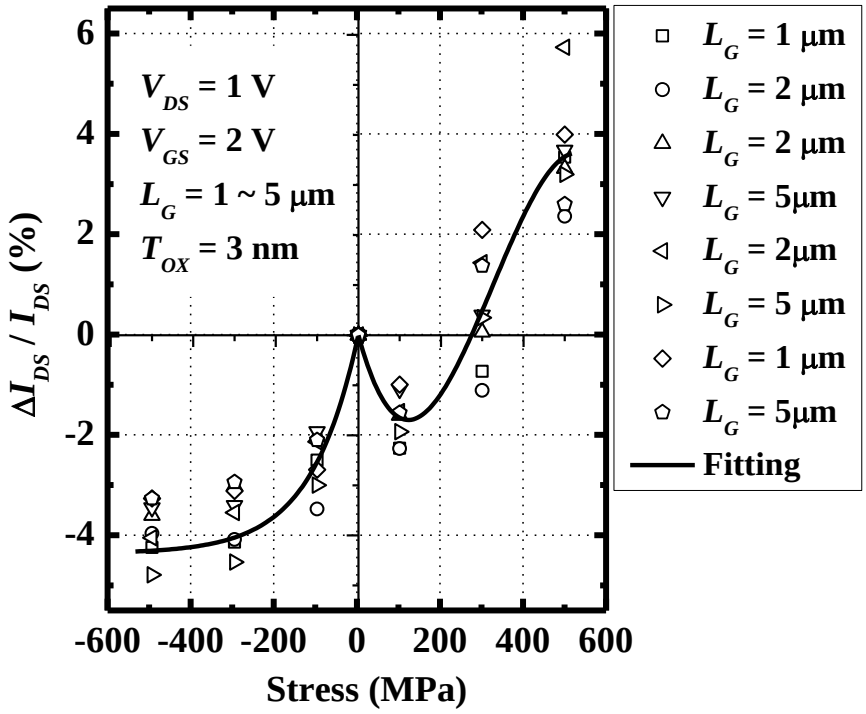


Fig. 2.4. Variation of I_{DS} under uniaxial compressive or tensile stress. Each symbol represents a single device under different stress conditions and 8 devices are shown in this figure. Devices with L_G from 1 μm to 5 μm were characterized at room temperature. For each L_G, the same device was used for all stress values.

To explain the stress effect, we need to consider energy band splitting and carrier redistribution. Tensile stress or strain lifts the six-fold degeneracy at the conduction band minima in Si by lowering the two-fold perpendicular valleys (Δ_2) with respect to the four-fold in-plane valleys (Δ_4). At the same time, the strain also splits the degenerate valence band into heavy-hole (HH), light-hole (LH) and spin-orbit-split-hole (SO) bands with the LH band being shifted up [95]. Therefore, the bandgap E_G of Si is effectively reduced. Fig 2.5 plots the indirect E_G of Si as a function of strain. The reduction in E_G at stress of 500 MPa along [110] direction can be estimated to be around 40 meV [96]-[98], which contributes to the enhancement of I_{DS}. As the TFET devices being characterized have long channels, the effect of strain

on the channel region should also be considered. In the channel region, splitting in the conduction band causes the carriers to preferentially occupy Δ_2 valley which has a light mass for carrier transport on the (100) surface [99], resulting in enhanced electron mobility and hence a larger I_{DS}. The I_{ON} for a TFET is directly related to band-to-band tunneling generation rate G_{BTBT}, as given by Kane's model [73],

$$G_{BTBT} = A\frac{\xi^2}{\sqrt{E_G}}\exp\left(-B\frac{E_G^{3/2}}{\xi}\right), \tag{2.2}$$

where ξ is the electric field, E_G is the bandgap. $A = \frac{e^2 m_r^{1/2}}{18\pi\hbar^2}$ and $B = \frac{\pi m_r^{1/2}}{2e\hbar}$, where e is the electronic charge, $\hbar$ is the reduced Planck's constant, and m_r is the reduced tunneling mass. A relationship governing m_r and the electron effective mass m_e^* and hole effective mass m_h^* is given by $\frac{1}{m_r} = \frac{1}{m_e^*} + \frac{1}{m_h^*}$. Stress affects G_{BTBT} mainly through its impact on B and E_G, since A is a pre-factor while both B and E_G are in the exponent in Equation (2.2). Reduction in m_e^* and m_h^* causes B to decrease, which also contributes to I_{DS} enhancement. However, there is an initial decrease in I_{DS} at tensile stress below 300 MPa. This may be caused by a reduction in carrier density-of-states (DOS) [100], which can reduce the number of available carriers for tunneling from the source side. This mechanism could possibly cause a I_{DS} reduction at low tensile stress.

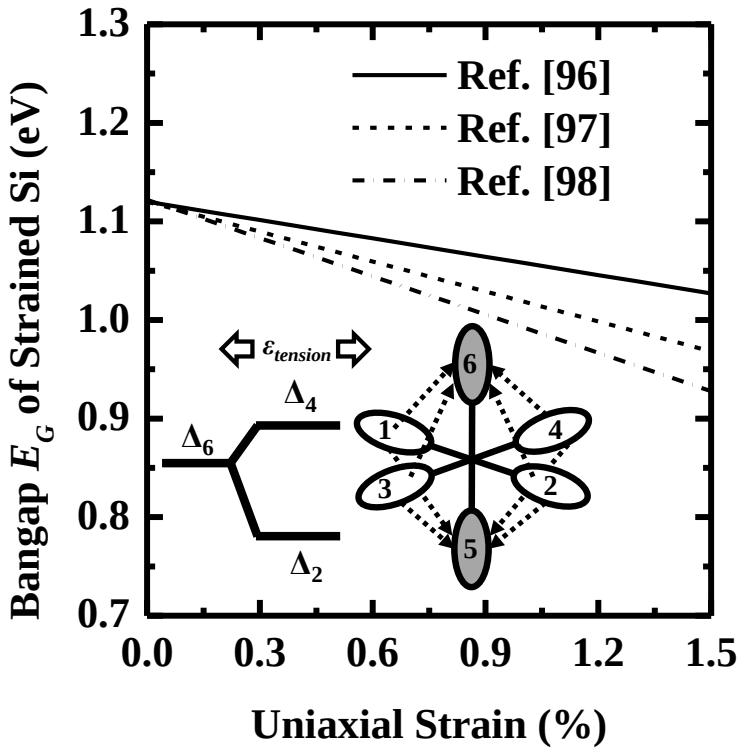


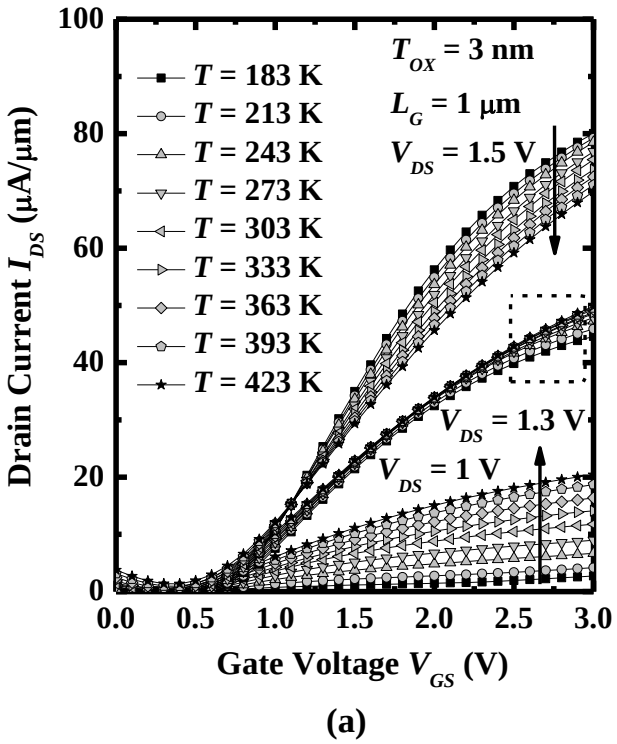
Fig. 2.5. Theoretical results indicate that uniaxial tensile strain reduces the E_G of Si. The inset is a schematic illustration of strain induced conduction band splitting and carrier repopulation among six valleys in Si conduction band under uniaxial tensile strain ($\varepsilon_{tension}$) along [110] direction. The strain makes the carriers preferentially populate in valley 5 and 6, where the effective mass is lower.

Similarly, E_G is also reduced with uniaxial compressive strain as discussed in [101]-[102]. However, DOS is reduced in the presence of compressive strain along the [110] direction. More importantly, the Δ_4 valleys with a higher effective mass move down in energy, leading to reduced electron mobility. Consequently, for a given I_{DS}, the voltage drop across the channel increases. This causes the electric field at the tunneling junction and hence the tunneling current to decrease for a given V_{DS}.

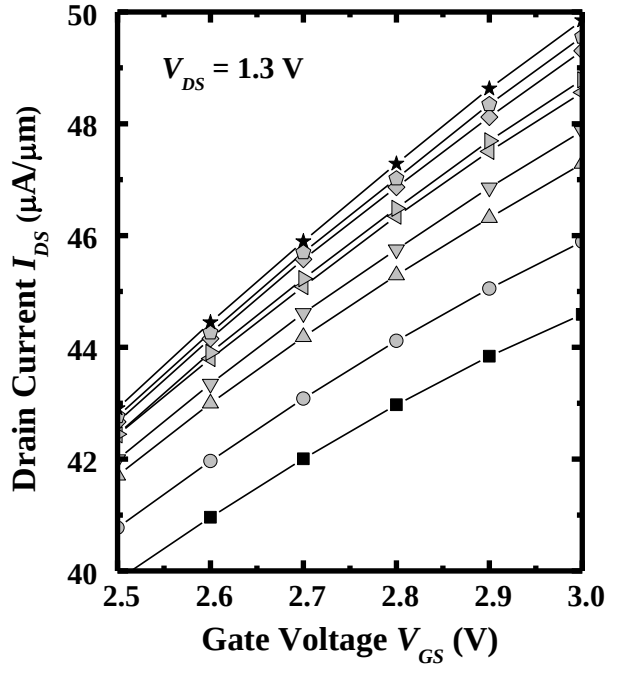
2.3 Temperature Dependence of Tunneling Current

The working principle of TFET is different from that of MOSFET, thus it is a very interesting study to investigate the effect of temperature on the electrical characteristics of TFET. This study is very important for understanding the physics of TFET. The devices employed for this study are from the same batch as those for the study of strain effect. Electrical characterization was performed at temperatures ranging from 183 to 423 K in steps of 30 K.

Fig. 2.6 shows the I_{DS} - V_{GS} characteristics of a TFET under various temperatures at V_{DS} of 1 V, 1.3 V, and 1.5 V. At V_{DS} of 1 V, I_{DS} increases monotonically with increasing temperature. However, when V_{DS} is 1.5 V, I_{DS} decreases with increasing temperature. Fig. 2.7 plots the change in I_{DS} as a function of temperature at various V_{GS} and V_{DS}. It clearly indicates that on-state tunneling current exhibits a positive temperature dependence at low drain bias condition (V_{DS} = 1 V), while the opposite behavior was observed when V_{DS} = 1.5 V. When the device temperature is increased, enhancement of I_{DS} at V_{DS} = 1 V results from bandgap narrowing of Si, while the reduction in I_{DS} at V_{DS} = 1.5 V is attributed to a decrease in electric field at the tunneling junction.



(a)



(b)

Fig. 2.6. (a) I_{DS} - V_{GS} curves at V_{DS} of 1 V, 1.3 V and 1.5 V measured at temperatures from 183 to 423 K in steps of 30 K. The arrows indicate the direction of the change of I_{DS} with increasing temperature. (b) The enlarged I_{DS} - V_{GS} curves in the dashed box in (a) for V_{DS} of 1.3 V.

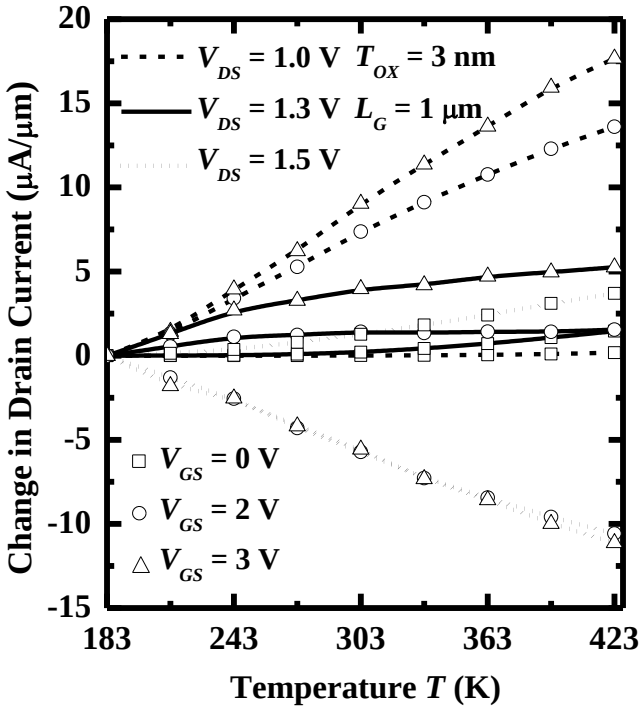


Fig. 2.7. Change in I_{DS} as a function of temperature for V_{GS} of 0 V, 2 V and 3 V. For each bias condition, I_{DS} at 183 K was taken as reference for comparison. It is observed that I_{DS} changes in different directions with different V_{DS} when the temperature is increased.

The temperature dependence of I_{DS} at V_{DS} = 1 V is discussed first. When the TFET is turned on, e.g. at V_{GS} of 2 or 3 V, I_{DS} increases with increasing temperature at V_{DS} of 1 V. This is attributed to E_G reduction of Si as temperature changes. The dependence of E_G on temperature T is given by [74]

$$E_G(T) = E_G(0) - \frac{\alpha T^2}{T + \beta}, \tag{2.3}$$

where α and β are material-dependent constants and $E_G(0)$ is the limiting value of the bandgap at zero Kelvin. For Si, α and β are 4.73×10^{-4} eV/K and 636 K, respectively. As T is increased, E_G is reduced. When T is increased from 183 to 423 K, the reduction of E_G is 61 meV. The exponential factor in Equation (2.2) predominantly determines the dependence of G_{BTBT} on E_G and is responsible for the enhancement in

I_{DS} with E_G reduction. At an electric field of 2 MV/cm in Equation (2.2), G_{BTBT} is increased by 3 times when E_G is reduced from 1.151 to 1.090 eV. This amount of enhancement in G_{BTBT} agrees with the I_{DS} enhancement as shown in Fig. 2.6(a). At V_{GS} = 0 V (i.e. off-state), I_{DS} is constituted by a leakage current and its change with temperature is mainly contributed by thermal generation in the depletion region, and is much smaller than the change in I_{DS} at V_{GS} of 2 or 3 V (on-state). In fact, for V_{GS} below the turn-on or threshold voltage V_{TH}, tunneling is negligible due to the large tunnel barrier width, and I_{DS} is insensitive to temperature. E_G reduction due to temperature does not effectively modulate a non-tunneling I_{DS}. Conversely, for V_{GS} above V_{TH}, carriers tunnel from the valence band to the conduction band through a tunnel barrier, and a reduced E_G leads to appreciable increase in tunneling probability and I_{DS}.

The temperature dependence of I_{DS} at V_{DS} = 1.5 V is discussed next, in which I_{DS} decreases with temperature at on-state. It should be noted that the on-state I_{DS} or I_{ON} is several times higher at V_{DS} = 1.5 V than that at V_{DS} = 1.0 V [Fig. 2.6(a)], and therefore the resistance due to carrier transport through the channel becomes important. Since at V_{DS} = 1.5 V, I_{ON} is larger than that at V_{DS} = 1 V, the voltage drop across the resistance of the channel $R_{Channel}$ is also greater. We have to consider the series resistance associated with the tunneling junction R_{Tunnel} and $R_{Channel}$ as illustrated in Fig. 2.8. At sufficiently large I_{ON}, the voltage drop across $R_{Channel}$ can affect the tunneling current and its effect becomes significant as V_{DS} gets larger. As temperature increases, $R_{Channel}$ increases due to a decrease in carrier mobility, resulting in a reduced voltage drop and peak electric field at the tunneling junction.

This reduces the tunneling current and can dominate over the effect of bandgap reduction. The I_{DS} at V_{DS} = 1.5 V in Fig. 2.7 shows this phenomenon.

We further investigate the temperature sensitivity of I_{DS} for TFETs with different L_G, which is represented by $\Delta I_{DS} / \Delta T$. Fig. 2.9 plots $\Delta I_{DS} / \Delta T$ as a function of L_G at V_{DS} of 1 V. We found that $\Delta I_{DS} / \Delta T$ decreases as L_G increases. This is consistent with the fact that $R_{Channel}$ is proportional to L_G and its effect on I_{DS} becomes more significant as L_G increases. The voltage drop across $R_{Channel}$ increases with L_G, which lowers the electric field at the tunneling junction for a given V_{DS}. Therefore, the temperature sensitivity of I_{DS} drops with increasing L_G.

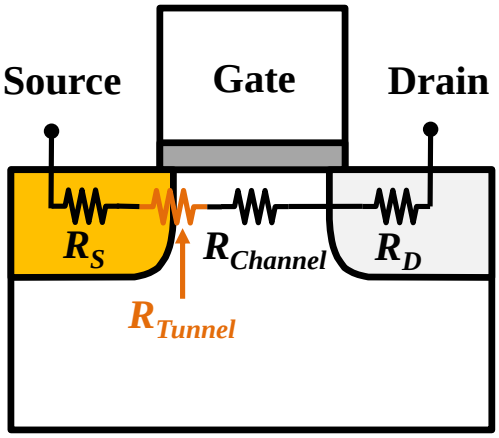


Fig. 2.8. Schematic of a TFET showing the resistance components between source and drain terminals: R_{Tunnel}, $R_{Channel}$, source resistance R_S, and drain resistance R_D. The temperature dependence of the tunneling current is mainly affected by the voltage drop on R_{Tunnel} and $R_{Channel}$.

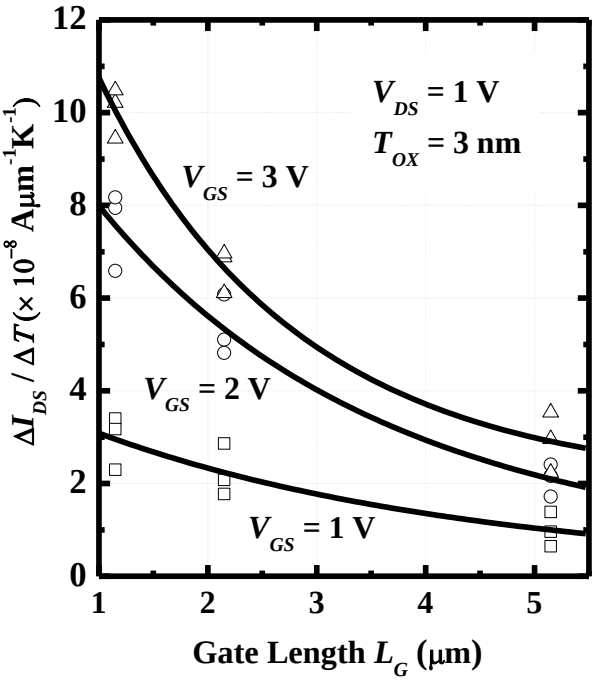


Fig. 2.9. $\Delta I_{DS} / \Delta T$ as a function of L_G at V_{DS} = 1 V. $\Delta I_{DS} / \Delta T$ decreases with L_G, and is attributed to an increased $R_{Channel}$ which reduces the electric field at the tunneling junction for a given V_{DS}.

2.4 Temperature Independent Current Biasing Employing TFET

Compared with MOSFET, electrical characteristics of TFET has a different temperature dependence as discussed in the last section. For low V_{DS}, on-state I_{DS} is mainly determined by the tunneling behavior which exhibits positive temperature coefficient, while at high V_{DS}, the TFET channel resistance presents significant voltage drop and reduces the electric field at the tunneling junction. As increasing temperature leads to increasing channel resistance due to lowering of the carrier mobility, this reduces the available tunneling potential and results in decreasing tunneling current, leading to a negative temperature coefficient. Therefore, there exists an optimum V_{DS} where the positive and negative temperature coefficients due to different mechanisms cancel out each other and attains zero temperature dependency. This property can be potentially exploited to provide a temperature independent current biasing.

To verify the concept, a circuit employing TFET is proposed as shown in Fig. 2.10. In the proposed circuit, the V_{DS} across the TFET device is accurately controlled through a feedback loop employing an operational amplifier and p-channel MOSFET device (MP_1). The resulting I_{DS} of the TFET is then mirrored to another p-channel MOSFET device (MP_2) to create the temperature independent current biasing. It should be pointed out that the magnitude of the temperature independent current can be varied by simply changing the V_{GS} of the TFET. However, this might lead to different optimum V_{DS} to achieve zero temperature dependency.

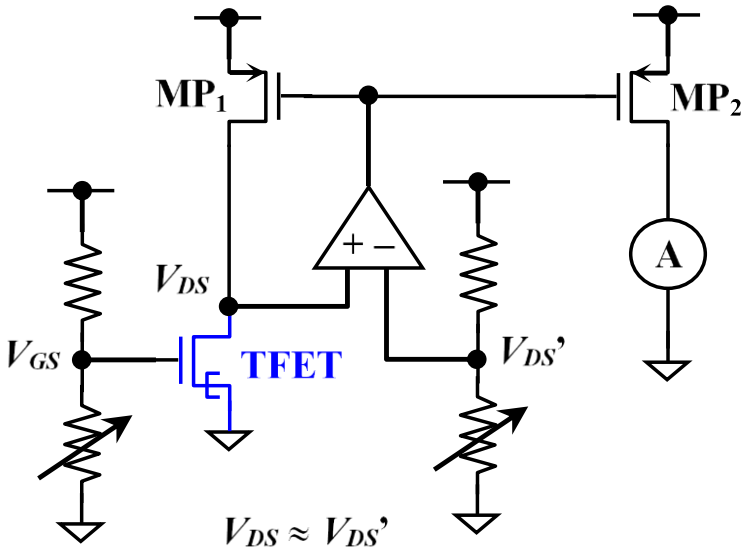


Fig. 2.10. Proposed temperature independent current biasing circuit. V_{GS} of the TFET is controlled by a voltage divider and V_{DS} is approximately equal to V_{DS}'. The output current was measured using a high-precision current meter at the drain terminal of MP_2. TFET device in this circuit has L_G of 5.15 µm and width of 180 nm.

A prototype was constructed where the operational amplifier is realized with Texas Instruments OPA2340PA, the p-channel MOSFETs are realized with Advanced Linear Devices ALD1107, and the in-house TFET device has L_G of 5.15 µm and total width of 180 nm. The circuit is subject to a heating chamber for accurately controlling the temperature. The temperature dependency of the current biasing with V_{GS} = 1.5 V is shown in Fig. 2.11. As illustrated, at higher V_{DS} (V_{DS} = 1.7 V), the current biasing exhibits negative temperature coefficient, whereas it exhibits positive temperature coefficient at lower V_{DS} (V_{DS} = 1 V). At V_{DS} = 1.3 V, the current biasing exhibits almost zero temperature dependency as shown by the horizontal line.

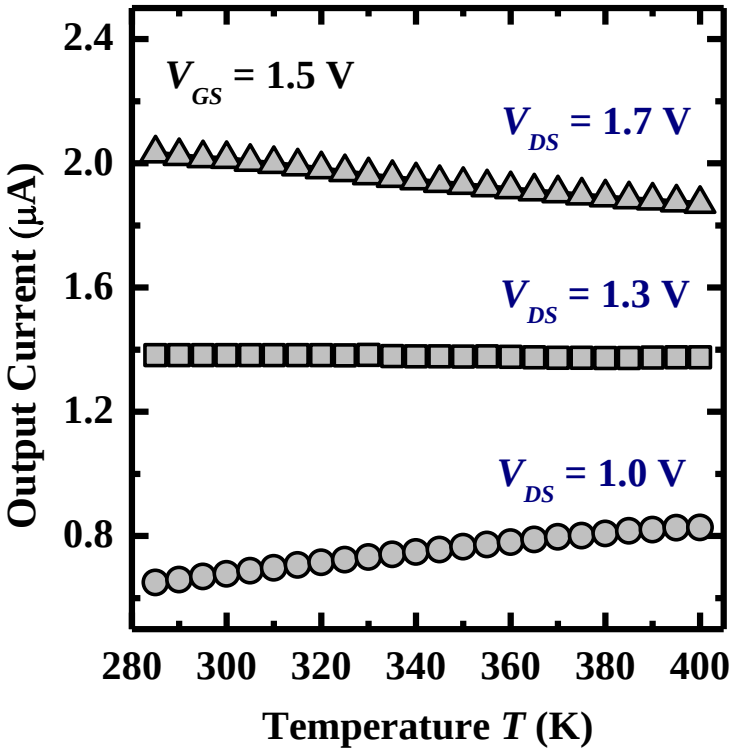


Fig. 2.11. Temperature dependency of the current biasing with various V_{DS} at V_{GS} = 1.5 V. At V_{DS} = 1.7 V, the current biasing exhibits negative temperature coefficient, whereas it exhibits positive temperature coefficient at V_{DS} = 1 V. The output current is almost independent on temperature at V_{DS} = 1.3 V.

The zoomed-in view of the output current together with the temperature sensitivity for V_{DS} = 1.3 V and V_{GS} = 1.5 V are shown in Fig. 2.12. A third-order polynomial, which results in least square errors, is employed to fit the measurement data in order to estimate the temperature sensitivity. The resulting polynomial is as follows

$$I_{DS} = c_1 \times T^3 + c_2 \times T^2 + c_3 \times T + c_4, \tag{2.4}$$

where T is the absolute temperature, c_1 = 3.2083 × 10^{-8}, c_2 = -3.3178 × 10^{-5}, c_3 = 1.1275 × 10^{-2}, and c_4 = 1.1986 × 10^{-1}. Using Equation (2.4), the temperature sensitivity is found to be within ± 120 ppm/K as shown in Fig. 2.12.

The effective temperature sensitivity $S_{T,eff}$ over the entire temperature range

can be found using the following expression [103]

$$S_{T,eff} = \frac{1}{I_{DS,nom}} \frac{I_{DS,\max} - I_{DS,\min}}{T_{\max} - T_{\min}}, \tag{2.5}$$

where $I_{DS,\max}$ and $I_{DS,\min}$ are the largest and smallest output current observed over the entire temperature range, respectively, and $T_{\max} - T_{\min}$ is the temperature range measured, $I_{DS,nom}$ is the nominal output current. The $S_{T,eff}$ in this study is calculated to be about 55 ppm/K. With further fine tuning of the V_{DS}, smaller temperature sensitivity can be achieved. This proves the feasibility of the proposed circuit employing TFET to achieve temperature independent current biasing.

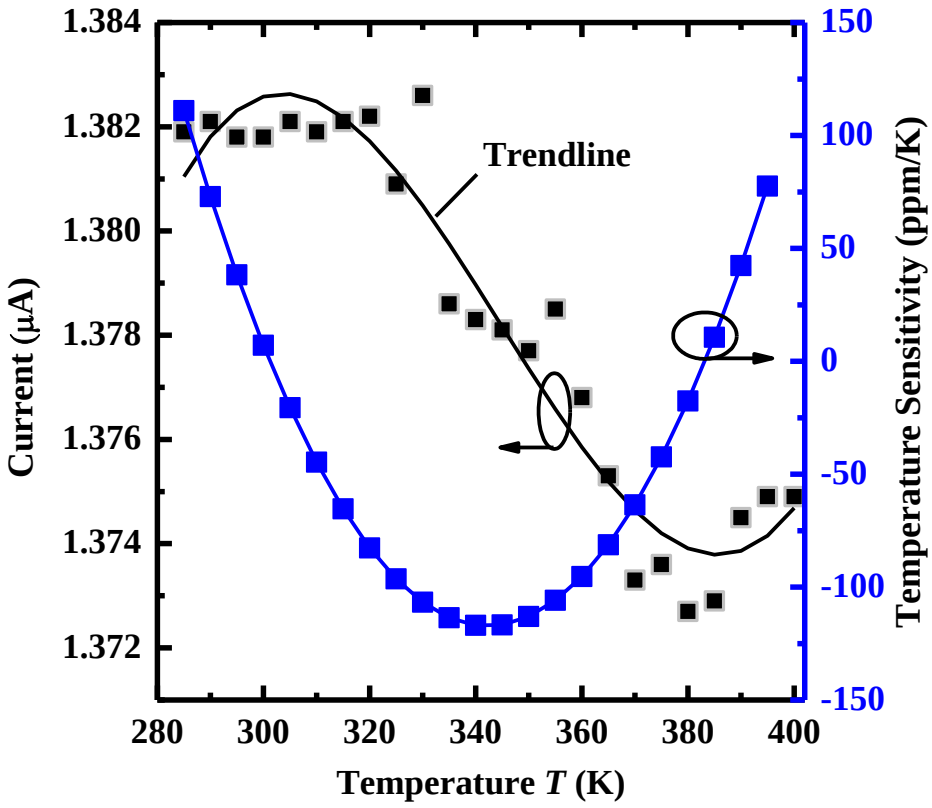


Fig. 2.12. Temperature dependency (left) and temperature sensitivity (right) of the current biasing at V_{DS} = 1.3 V and V_{GS} = 1.5 V. A low temperature sensitivity of ± 120 ppm/K is achieved.

By exploiting the temperature dependency of the tunneling current, a current biasing with low temperature sensitivity within ± 120 ppm/K and effective temperature sensitivity of 55 ppm/K has been achieved. Compared with conventional bandgap biasing technique, our proposed solution provides temperature independent current biasing instead of voltage biasing. In addition, the proposed solution does not need a bipolar junction transistor (BJT). Since the current gain of a BJT is not exactly constant and depends on temperature and collector current, temperature insensitive biasing circuit employing BJT tends to have high temperature sensitivity, which requires complex design to achieve a small temperature sensitivity [103]. Furthermore, the TFET device can be easily integrated into the existing MOSFET fabrication process flow as it has a similar device structure as a conventional MOSFET. These features make the proposed current biasing circuit interesting and attractive.

2.5 Summary

The strain and temperature dependence of TFET I_{DS} - V_{GS} characteristics were studied and the underlying mechanisms were analyzed. In general, E_G narrowing due to uniaxial tensile stress leads to I_{DS} enhancement. On the other hand, uniaxial compressive stress reduces I_{DS}. Methods to induce high tensile strain in TFETs include source/drain stressors [104], strain-transfer structure [104], and high-stress liners [105]. The positive temperature coefficient of I_{ON} at low V_{DS} is due to temperature-induced E_G reduction, and the negative temperature coefficient at higher V_{DS} is due to increased $R_{Channel}$ which reduces the effective electric field at the tunneling junction for a given V_{DS}. Results presented here could be useful for the design of strained short-channel TFETs where the temperature sensitivity is larger and localized strain can be large.

In addition, a temperature independent current biasing circuit, which exploits the unique temperature dependence of the TFET, was proposed. By exploiting the TFET temperature dependence on drain voltage bias, current biasing with low temperature sensitivity within ± 120 ppm/K and effective temperature sensitivity of 55 ppm/K has been achieved. In contrast to the conventional bandgap biasing technique, the proposed solution provides temperature independent current biasing rather than voltage biasing. It also eliminates the need for BJT in the biasing circuit whose quality (current gain) is limited.

Chapter 3

Source-Channel Interface Engineering for Tunneling Field-Effect Transistor (TFET) with p^+ $Si_{0.5}Ge_{0.5}$ Source: Insertion of Strained $Si_{0.989}C_{0.011}$ Layer for Enhancement of Tunneling Current and Subthreshold Swing

3.1 Introduction

Silicon (Si)-based tunneling field-effect transistors (TFETs) have attracted great interests due to the advances of Si processing technology and the ease of integration into the current complementary metal-oxide-semiconductor (CMOS) fabrication process. Simulation [18],[25]-[26],[28],[30]-[31],[66],[107],[112] and experimental [13],[16]-[17],[20],[22]-[23],[29],[32]-[33],[35]-[39],[106],[108]-[111] work on Si-based TFETs have been reported. However, one key disadvantage of Si-based TFETs is the low on-state current I_{ON} caused by the large tunneling barrier as determined by the bandgap E_G of Si. Table 3.1 summarizes the experimental data on Si-based TFETs. Typical I_{ON} values reported range from 0.17 to 12 μA/μm at drain voltage V_{DS} of 1 V and gate voltage V_{GS} of 1 V [16],[33],[37],[39],[106],[110]. To increase I_{ON}, the valence band edge energy E_V in the source can be raised and the

conduction band edge energy E_C in the channel can be lowered to reduce the length of the tunneling path L_T as illustrated in Fig. 3.1. This can be achieved using $Si_{1-x}Ge_x$/Si or Ge/Si source/channel structure design. The $Si_{1-x}Ge_x$/Si and Ge/Si heterojunctions are promising source/channel structures for improving the I_{ON} of Si-based TFETs while preserving a very low off-state current I_{OFF}.

Table 3.1. Summary of device characteristics of Si-based TFETs.

References	V_{DS} (V)	V_{GS} (V)	S (mV/decade)	I_{ON} (μA/μm)	I_{OFF} (nA/μm)
K. Bhuwalka [13]	1.5	8	285	0.1	10^{-2}
W. Y. Choi [16]	1	1	52.8	12	1
W. Y. Choi [17]	1	1.2	220	0.05	3×10^{-2}
V. Nagavarapu [20]	1	0.6	~100	15	0.1
S. H. Kim [22]	0.5	0.2	~40	3	$< 10^{-3}$
F. Mayer [23]	0.8	3	42	0.02	10^{-4}
G. Han [32]	0.9	2	200	12	10^{-2}
K. Jeon [33]	1	1	46	1.2	10^{-4}
G. Han [35]	1	2	85	10	4×10^{-3}
R. Gandhi [36]	1.2	2	50	0.023	1.6×10^{-4}
D. Leonelli [37]	-1.2	-2	160	5	3×10^{-3}
A. Villalon [38]	-1	-2.5	150	428	10^{-2}
Q. Huang [39]	0.05	1	36	2.5×10^{-2}	10^{-4}
Q. Huang [110]	0.6	0.8	67	0.22	1.5×10^{-3}

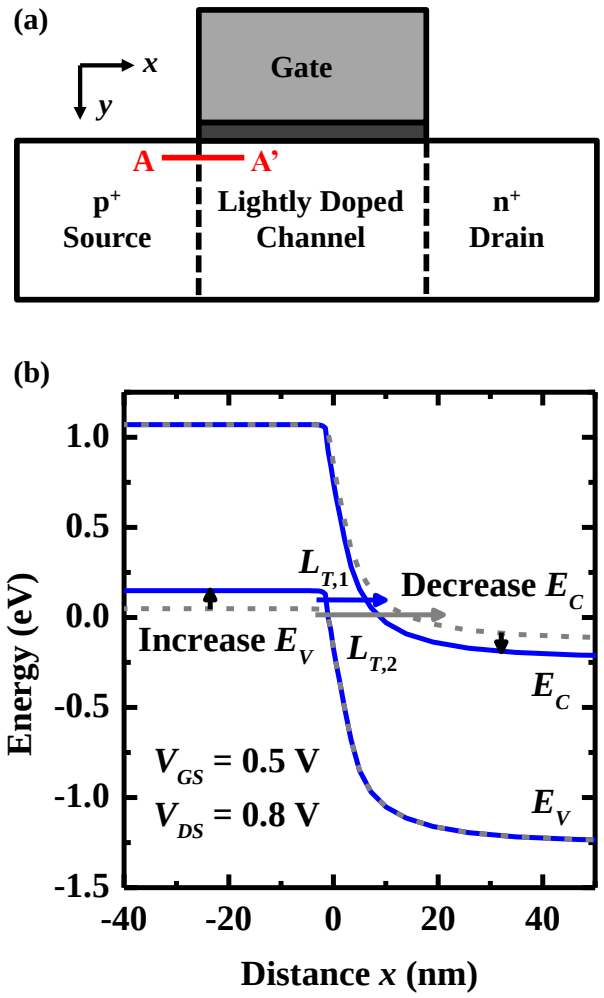


Fig. 3.1. (a) Cross-sectional view of a TFET. (b) Energy band diagram along A-A' direction in the tunneling junction region of a TFET as indicated in (a). Increasing E_V in the source and lowering E_C in the channel can lead to a shorter tunneling path ($L_{T,1} < L_{T,2}$), contributing to an improved drive current.

In addition, an abrupt source doping profile can also contribute to a high I_{ON}. According to the Kane's model [73], the band-to-band tunneling (BTBT) generation rate G_{BTBT} in TFET strongly depends on the electric field at the tunneling junction. A very abrupt source doping profile can reduce the width of the depletion region at the source/channel interface and increase the electric field at the tunneling junction, leading to a high G_{BTBT} and I_{ON}. Techniques to achieve an abrupt source doping

profile, such as dopant steepening implant [32] and dopant segregation [33], have been utilized to fabricate all-Si TFETs.

In this Chapter, we demonstrated *in situ* boron-doped p^+ $Si_{0.5}Ge_{0.5}$ source vertical TFETs with a thin layer of strained $Si_{0.989}C_{0.011}$ (~8 nm) inserted at the tunneling junction and investigated the impact of this $Si_{0.989}C_{0.011}$ layer on the electrical characteristics of TFETs. It was found that $Si_{0.989}C_{0.011}$ layer could help to lower the E_C on the channel side. At the same time, it also contributes to a steep p^+ doping profile in the source by suppressing boron diffusion [113]-[117]. $Si_{0.5}Ge_{0.5}$ source TFET having a $Si_{0.989}C_{0.011}$ layer inserted below the $Si_{0.5}Ge_{0.5}$ source (denoted as TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source) exhibits higher I_{ON} and steeper subthreshold swing S as compared with the one without the $Si_{0.989}C_{0.011}$ layer (denoted as TFET control device).

3.2 Device Concept and Design

Fig. 3.2 shows the schematics of a TFET control device [Fig. 3.2(a)] and a TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source structure [Fig. 3.2(b)]. In the on-state, valence band electrons tunnel from the p^+ $Si_{0.5}Ge_{0.5}$ region and emerge in the strained $Si_{0.989}C_{0.011}$ region in the TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source.

Finite element simulation was employed to examine the distribution of lateral strain ε_{xx} in the tunneling junction region of TFETs, as shown in Fig. 3.3. Lateral compressive strain is induced in the $Si_{0.5}Ge_{0.5}$ layer, while the Si channel is under lateral tensile strain [Fig. 3.3(a)]. With the insertion of a $Si_{0.989}C_{0.011}$ layer, the lateral tensile strain in the channel region becomes larger [Fig. 3.3(b)]. The average strain in a 12 nm × 10 nm region of the $Si_{0.989}C_{0.011}$ layer, as indicated by the red dashed box in

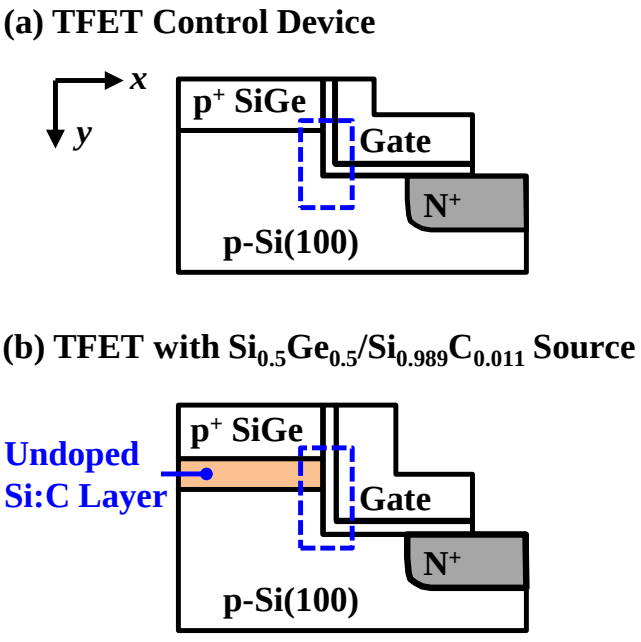
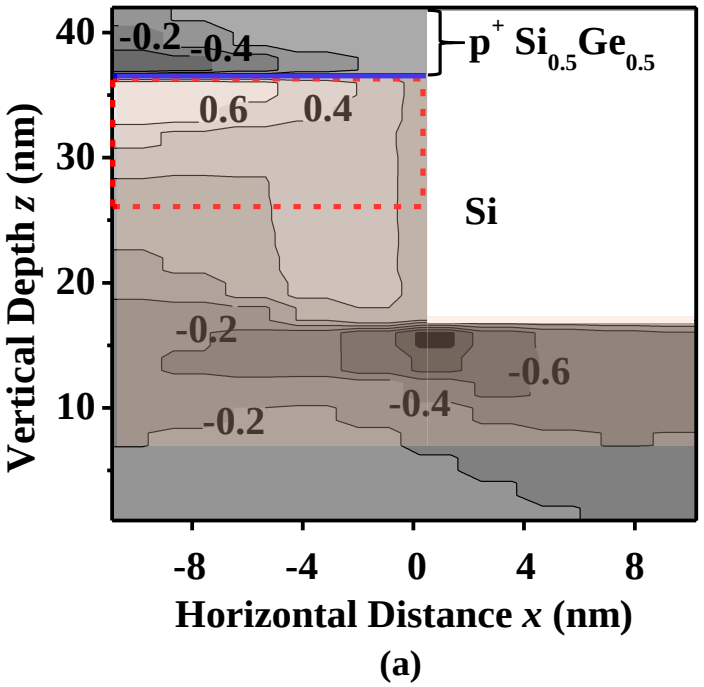


Fig. 3.2. Schematics of (a) vertical TFET with p^+ $Si_{0.5}Ge_{0.5}$ source and (b) TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source. The thin $Si_{0.989}C_{0.011}$ layer underneath the $Si_{0.5}Ge_{0.5}$ is undoped.

Fig. 3.3(b), is ~0.5%. This is larger than that in the Si channel of a TFET control device (~0.4%). The compressive strain in the $Si_{0.5}Ge_{0.5}$ lifts the valence band edge of $Si_{0.5}Ge_{0.5}$, while the tensile strain in the $Si_{0.989}C_{0.011}$ and Si lowers the conduction band edges of $Si_{0.989}C_{0.011}$ and Si, respectively. Due to the larger tensile strain in the $Si_{0.989}C_{0.011}$ layer, the conduction band energy in the channel region of the TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source is lower than that of the TFET control device. As a result, the effective tunneling barrier that valence electrons in the $Si_{0.5}Ge_{0.5}$ need to surmount is reduced, thus contributing to an enhancement of I_{ON}.

The energy band alignments of the $Si_{0.5}Ge_{0.5}$/Si and $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$/Si structures at thermal equilibrium are simulated and shown in Fig. 3.4. A customized simulator was used, which implements a non-local algorithm for accurate calculation of the band-to-band tunneling current [122]-[123]. The presence of substitutional carbon (C) lowers the E_C of $Si_{0.989}C_{0.011}$ by 45 meV as compared with Si. This amount of E_C lowering is further increased to 79 meV in the presence of ~0.5% biaxial tensile strain [118]-[121]. The resulting conduction band offset ΔE_C between $Si_{0.5}Ge_{0.5}$ and $Si_{0.989}C_{0.011}$ or bandgap reduction is expected to contribute to I_{ON} enhancement as the tunneling probability has a near exponential dependence on the bandgap.



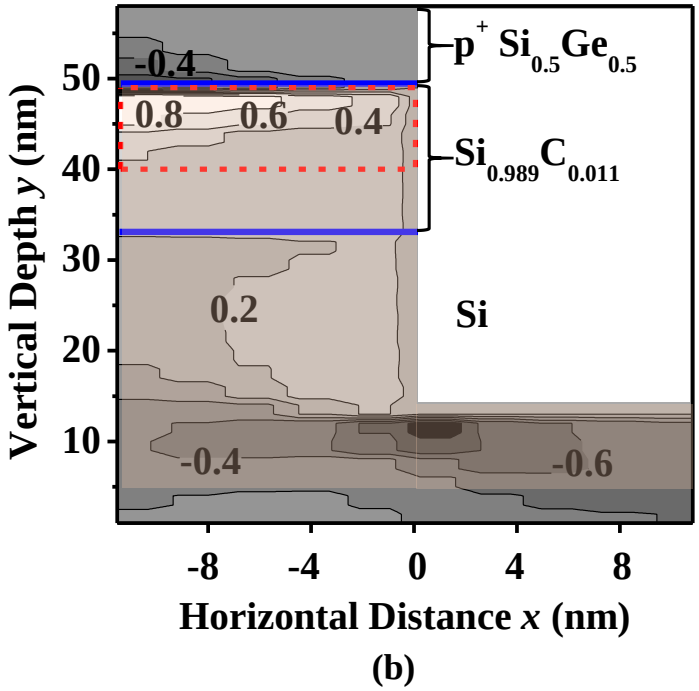


Fig. 3.3. Lateral strain ε_{xx} distribution for (a) TFET control device and (b) TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source for the dashed regions as indicated in Fig. 3.2. The channel regions of these two structures are highlighted in light yellow. Compressive strain is denoted by negative sign. A higher tensile strain is induced in the $Si_{0.989}C_{0.011}$ layer as compared to the Si channel in the TFET control device. The tensile strain in $Si_{0.989}C_{0.011}$ reduces the tunnel barrier and enhances the tunneling probability.

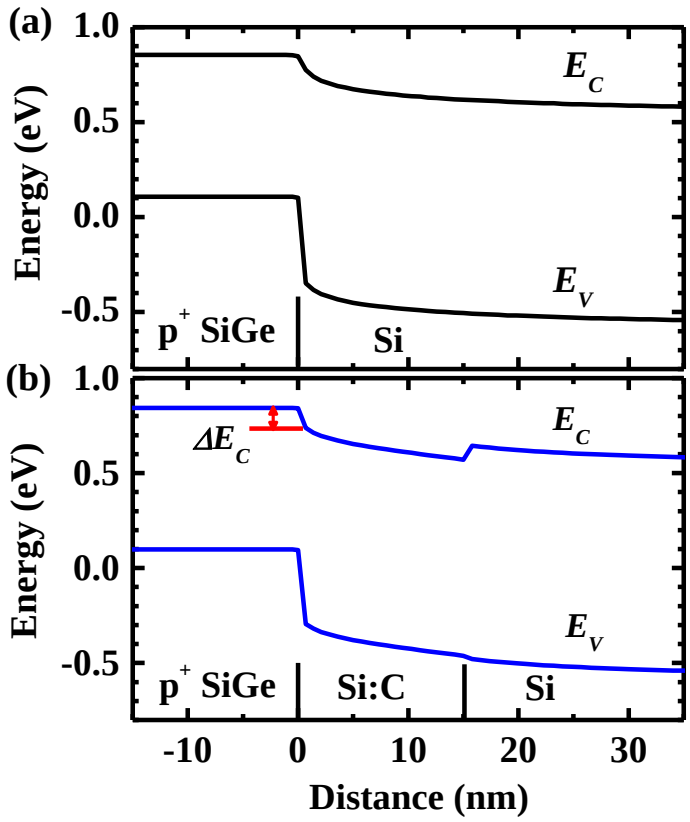


Fig. 3.4. Energy band alignments of (a) $Si_{0.5}Ge_{0.5}$/Si and (b) $Si_{0.5}Ge_{0.5}$/$Si_{0.989}C_{0.011}$/Si structures. The presence of substitutional C lowers the E_C of $Si_{0.989}C_{0.011}$ by 79 meV by taking consideration of the ~0.5% biaxial tensile strain in the $Si_{0.989}C_{0.011}$ layer, which can contribute to I_{ON} enhancement of TFET.

The insertion of an undoped $Si_{0.989}C_{0.011}$ layer underneath the p^+ $Si_{0.5}Ge_{0.5}$ source can also contribute to a steep p^+ dopant profile at the tunneling junction by suppressing boron diffusion. The impact of source doping profile on the tunneling current was investigated. Fig. 3.5 shows the simulated I_{DS} - V_{GS} curves of $Si_{0.5}Ge_{0.5}$ source TFETs with different source doping profiles at V_{DS} of 0.8 V. For this simulation, the device parameters used were: source doping $N_A = 8 \times 10^{20}$ cm^{-3}, drain doping $N_D = 1 \times 10^{20}$ cm^{-3} with a profile of 10 nm/decade into the channel, body doping $N_A = 1 \times 10^{16}$ cm^{-3}, equivalent oxide thickness (EOT) = 0.8 nm, gate length L_G

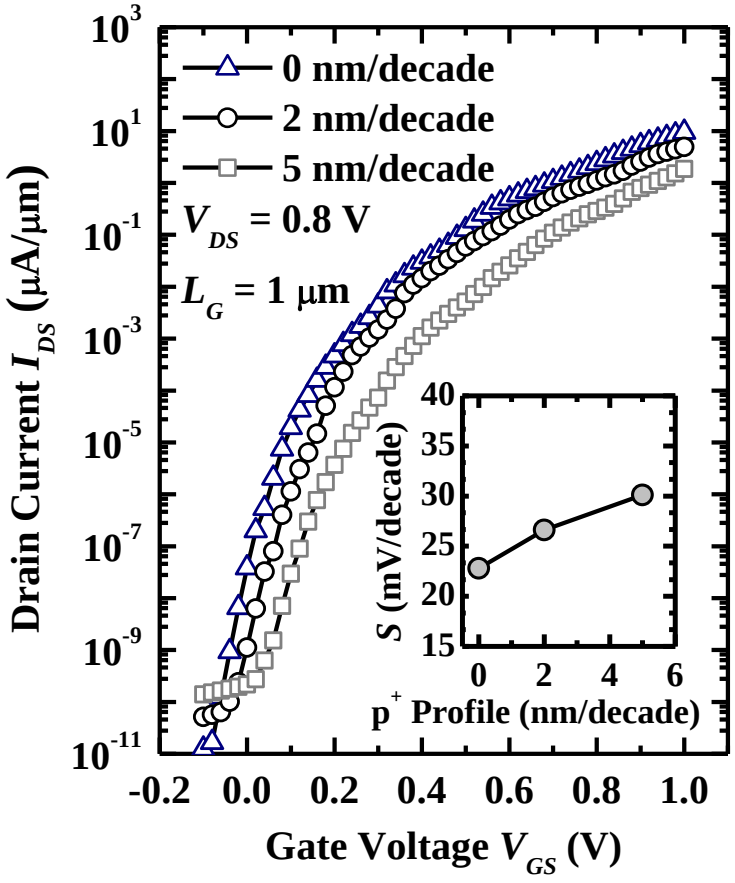


Fig. 3.5. Simulated I_{DS} - V_{GS} curves of $Si_{0.5}Ge_{0.5}$ source TFETs with different source doping profiles. The inset shows the minimum point S as a function of source doping profile. The diffusion of boron into the channel affects the I_{ON} and S of the TFET.

= 1 μm. Fig. 3.5 reveals that both I_{DS} and S degrade as the source doping profile becomes less steep, e.g. varying from 0 nm/decade to 5 nm/decade.

Fig. 3.6 shows the energy band diagrams along the source-to-channel direction at thermal equilibrium for the devices in Fig. 3.5. The local electric field, which is affected by the doping profile, decreases as the doping profile becomes more gradual. As a result, the tunneling width increases, causing both I_{ON} and S to degrade.

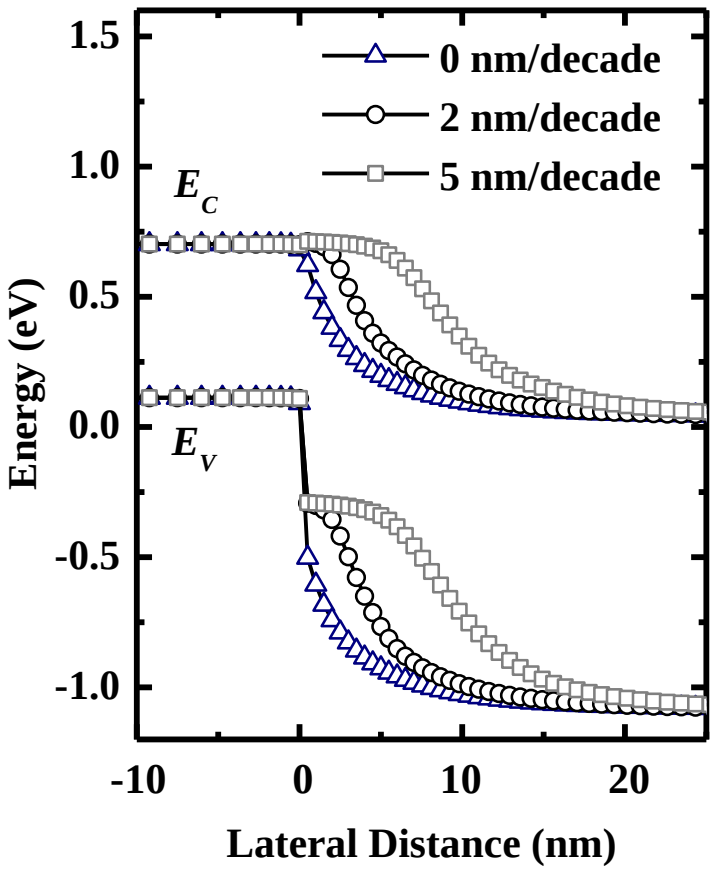


Fig. 3.6. The energy band diagrams along source-to-channel direction for the devices in Fig. 3.5. As the source doping profile changes from 0 to 5 nm/decade, the tunneling width increases, which is responsible for the degradation of I_{ON} and S.

Simulation was performed to compare the performance of TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source and TFET control device. In the control device, the source doping profile was 5 nm/decade into the channel. In the TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source, the $Si_{0.989}C_{0.011}$ layer thickness was 10 nm and the source doping profile was 3 nm/decade. The other device parameters used in this simulation were the same as those in Figs. 3.5 and 3.6. The simulated transfer characteristics of the two TFETs are shown in Fig. 3.7. We define V_{leak_floor} to be the maximum gate voltage in the off-state leakage floor region of the I_{DS} - V_{GS} curve, i.e. just before I_{DS} rises sharply with increasing V_{GS}. Different gate work functions were

chosen for the two devices so that the values of V_{leak_floor} were the same. It can be observed that TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source exhibits a higher I_{DS} and smaller *S*.

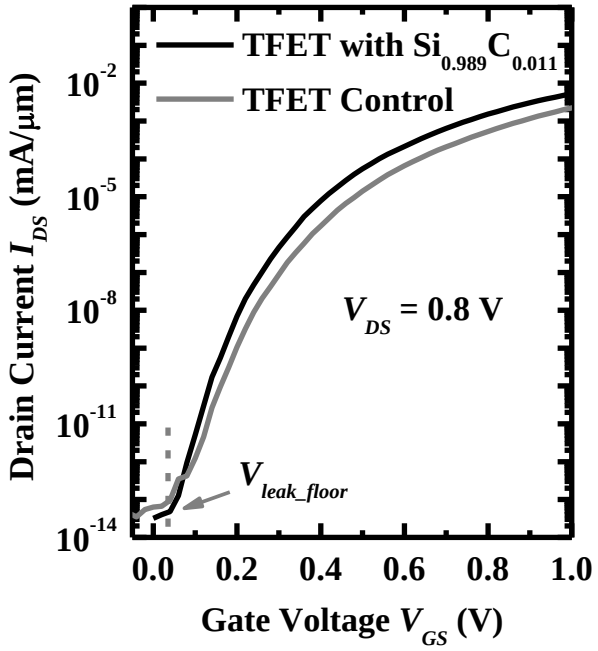


Fig. 3.7. Simulated transfer characteristics of TFET control device and TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source. A higher I_{DS} is obtained by inserting a $Si_{0.989}C_{0.011}$ layer.

3.3 Fabrication of TFETs with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ Source

Fig. 3.8 illustrates the key processing steps for the fabrication of TFETs with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source. A gate-last process was used. The devices were fabricated on 6-inch (100)-oriented p-type Si substrates. Thermal oxide with a thickness of 400 nm was grown and subsequently etched in buffered oxide etch (BOE) solution to define the active area. Next, photolithography was performed to expose the drain region, which was implanted with As^+ at an implant energy of 50 keV and a dose of 1×10^{15} cm^{-2}. Drain dopant activation was done at 1000 ˚C for 60 s in a rapid thermal annealing (RTA) system [Fig. 3.8(a)]. This high temperature step was performed before a subsequent p^+ $Si_{0.5}Ge_{0.5}$ epitaxial growth to avoid excessive boron diffusion.

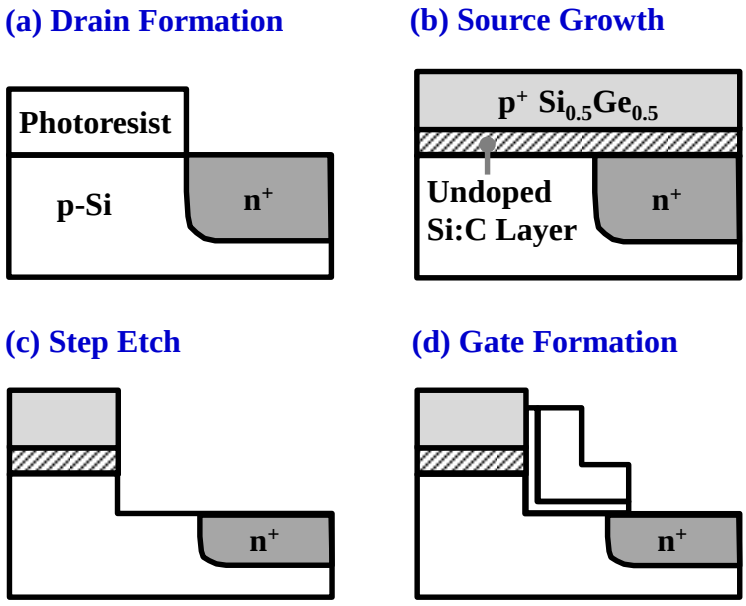


Fig. 3.8. Key processing steps used to fabricate TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source. TFET control device went through the same processing steps without the growth of the undoped $Si_{0.989}C_{0.011}$ layer.

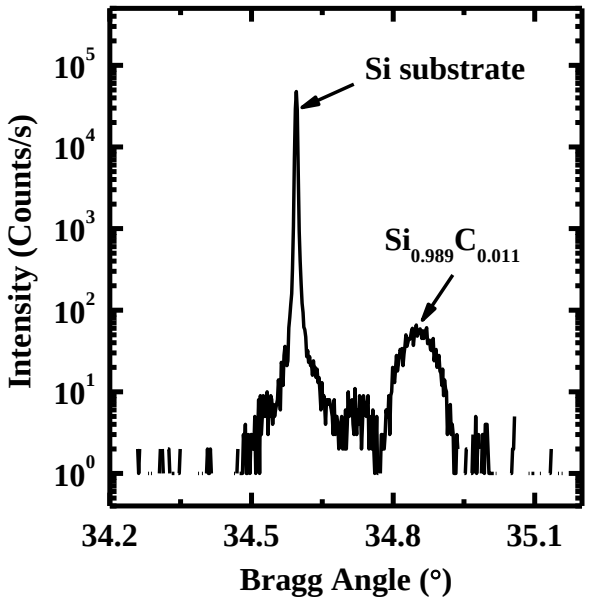


Fig. 3.9. High-resolution XRD spectrum of a blanket Si sample with 40 nm thick Si:C layer. The substitutional carbon concentration was determined to be 1.1%. The well-defined $Si_{0.989}C_{0.011}$ peak indicates the high crystalline quality of the epitaxial $Si_{0.989}C_{0.011}$ film on Si.

After drain formation, the wafers were cleaned in sulfuric peroxide mixture (SPM) solution for 10 minutes and in dilute hydrofluoric acid (DHF) ($HF:H_2O$ = 1:100) for 3 minutes sequentially before being loaded into an ultra-high-vacuum chemical vapor deposition (UHVCVD) system for source structure growth [Fig. 3.8(b)]. On one wafer, an undoped $Si_{0.989}C_{0.011}$ film was grown at 650 ˚C followed by *in situ* boron-doped $Si_{0.5}Ge_{0.5}$ growth at 470 ˚C to form the source. Si_2H_6, SiH_3CH_3, GeH_4 and B_2H_6 gas sources were used as the precursors for Si, C, Ge and boron, respectively. Fig. 3.9 shows the high-resolution x-ray diffraction (XRD) spectrum of the $Si_{0.989}C_{0.011}$ grown on a blanket Si substrate. The substitutional C concentration was found to be 1.1%. The well-defined $Si_{0.989}C_{0.011}$ peak indicates the excellent crystalline quality of the epitaxial film. On another wafer for the control device, the $Si_{0.989}C_{0.011}$ growth was not performed and only p^+ $Si_{0.5}Ge_{0.5}$ was grown. The active

boron concentration in the $Si_{0.5}Ge_{0.5}$ layer was determined to be 2×10^{20} cm^{-3} from Hall measurement.

Table 3.2. Recipes used for $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ etch using a reactive ion etcher.

Recipe Name	RF Power (W)	Substrate Bias (V)	Pressure (mTorr)	Cl_2 Flow Rate (sccm)
A	400	-200	10	200
B	300	-150	10	200

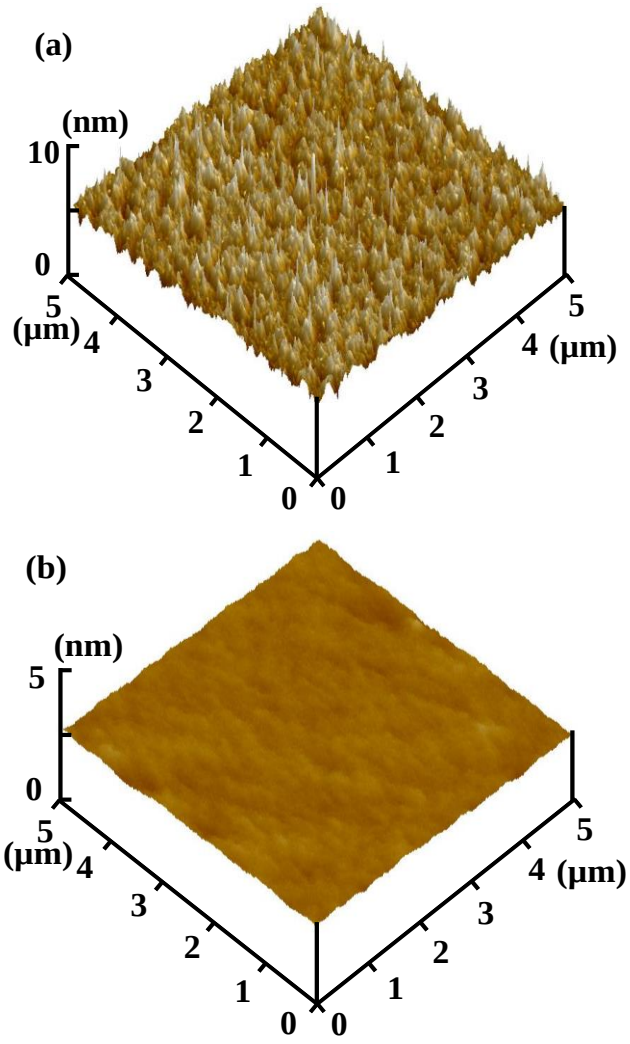


Fig. 3.10. AFM measurements of the Si surface roughness after the Cl_2-based plasma etch that forms the elevated source. (a) RMS surface roughness for a 5 μm × 5 μm area is 2.46 nm using recipe A. (b) A smooth Si surface with RMS surface roughness of 0.19 nm was obtained by reducing the RF power and substrate bias.

After the epitaxial growth step, a 60 nm thick SiO_2 hard mask was deposited on all wafer splits using plasma enhanced chemical vapor deposition (PECVD) at 280 ˚C. A source mask pattern was then lithographically defined to cover the source region, and a vertical step etch using Cl_2-based plasma was performed to remove the $Si_{0.5}Ge_{0.5}$ and $Si_{0.989}C_{0.011}$ layers in the channel and drain regions. This formed the elevated $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source structure [Fig. 3.8(c)]. Table 3.2 reveals the contents of the two recipes (recipe A and B) used in this etch. The surface roughness of the Si channel after etch was measured using atomic force microscopy (AFM) as shown in Fig. 3.10. Recipe A causes a high surface roughness to the Si surface as shown in Fig. 3.10(a). By reducing the RF power and substrate bias, a low root-mean-square (RMS) surface roughness of 0.19 nm over a 5 μm × 5 μm scan area was obtained [Fig. 3.10(b)]. The wafers were then treated in SPM and DHF before gate stack formation. 5 nm thick Al_2O_3 gate dielectric by atomic layer deposition (ALD) and 180 nm thick TaN by reactive sputtering were deposited to form the gate stack. The wafers were then etched in Cl_2-based plasma to form the gate electrode [Fig. 3.8(d)].

Fig. 3.11(a) shows a top-view scanning electron microscope (SEM) image of a ring-type TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source. The SEM image in Fig. 3.11(b) shows the zoomed-in view of the region highlighted by the dashed box in Fig. 3.11(a). Fig. 3.12 depicts the transmission electron microscope (TEM) images of a fabricated TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source. The thicknesses of the $Si_{0.5}Ge_{0.5}$ and $Si_{0.989}C_{0.011}$ layers are 13 nm and 8 nm, respectively [Fig. 3.12(b)]. Fig. 3.12(c) shows

the excellent crystalline quality of the epitaxial $Si_{0.5}Ge_{0.5}$ and $Si_{0.989}C_{0.011}$ layers with no observable defects at the $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ and $Si_{0.989}C_{0.011}/Si$ interfaces.

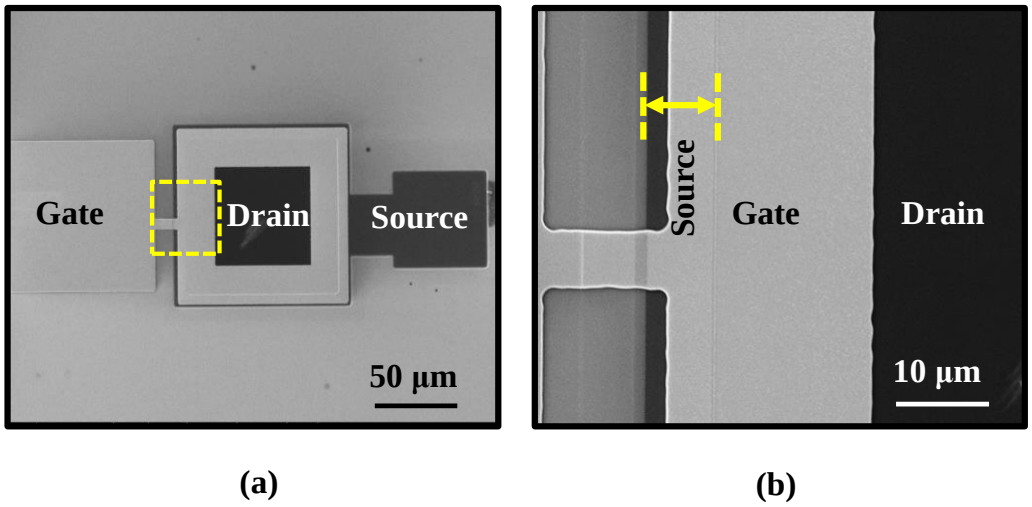


Fig. 3.11. (a) Top-view SEM image of a ring-type TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source. (b) Zoomed-in view of the region highlighted by the dashed box in (a), which shows the source pattern of the TFET.

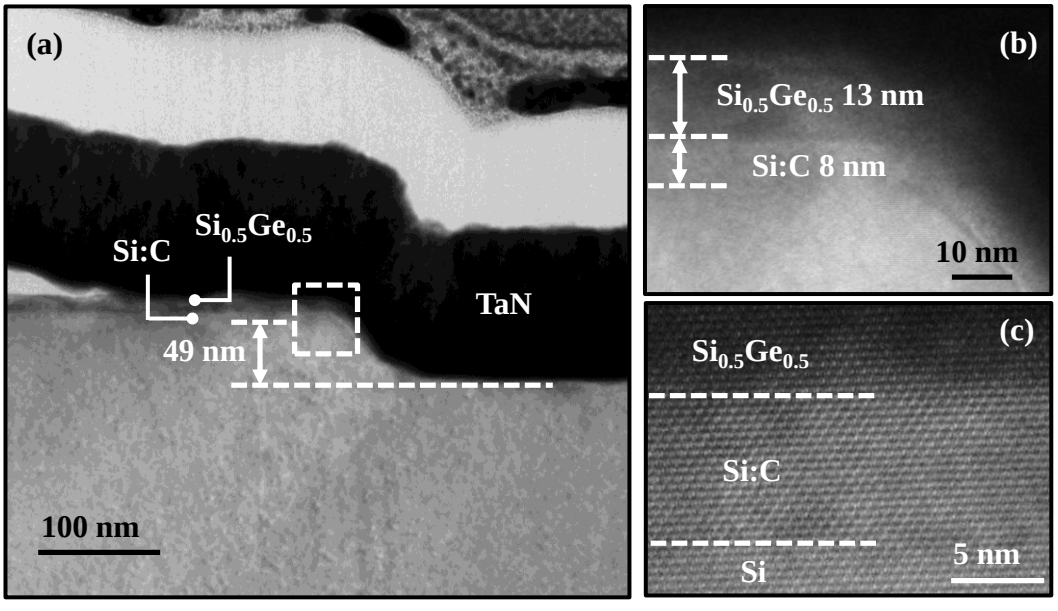


Fig. 3.12. (a) TEM image of a TFET featuring $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source, TaN metal gate, and Al_2O_3 gate dielectric. (b) The thicknesses of the epitaxial $Si_{0.5}Ge_{0.5}$ and $Si_{0.989}C_{0.011}$ layers are 13 nm and 8 nm, respectively. (c) High-resolution TEM image reveals the excellent crystalline quality of the $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}/Si$ structure.

3.4 Electrical Characterization of TFETs

Fig. 3.13 compares the secondary ion mass spectrometry (SIMS) profiles for boron along the vertical direction in the source regions of TFETs with and without $Si_{0.989}C_{0.011}$ layer at the tunneling junction. A low energy Ar^+ beam was used in the SIMS analysis to improve the depth resolution of the boron profile. It can be observed that TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source achieves a steeper boron profile of ~3 nm/decade than the TFET control device. This is because the inserted $Si_{0.989}C_{0.011}$ layer helps to suppress boron diffusion. Boron diffuses by an interstitialcy mechanism in Si [124]. The presence of substitutional C consumes silicon interstitials, which leads to a reduced diffusivity of boron [113] and contributes to a steeper boron profile.

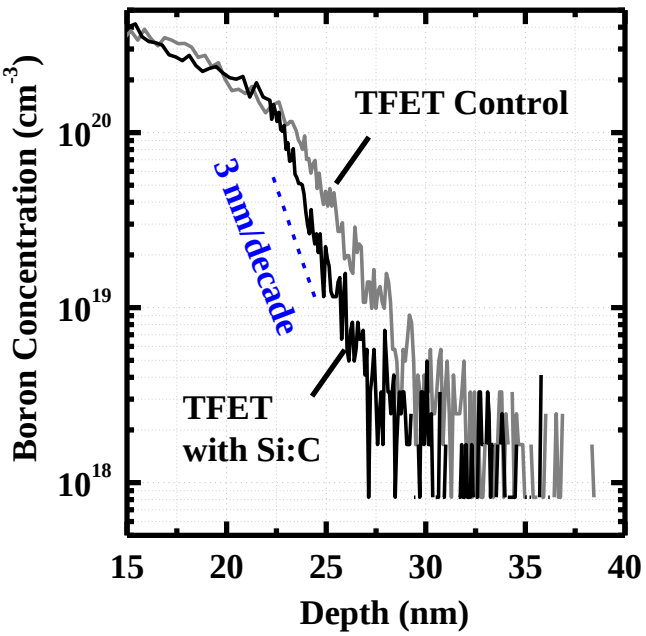
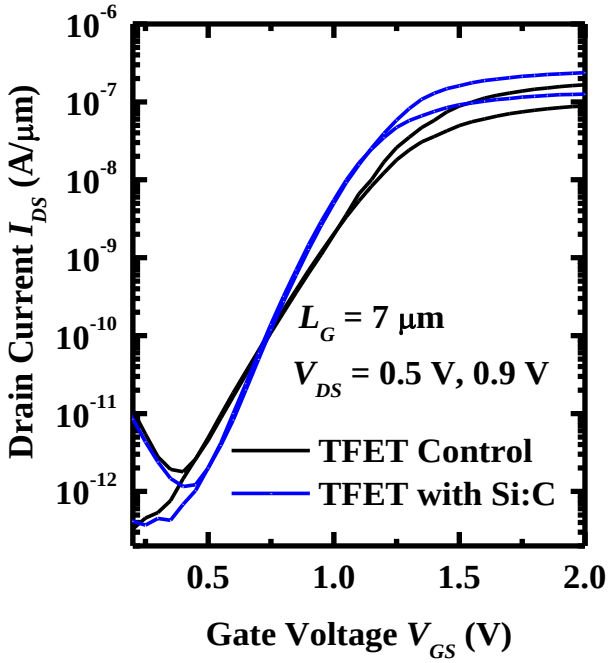


Fig. 3.13. SIMS profiles for boron along the vertical direction in the source regions of TFETs with and without $Si_{0.989}C_{0.011}$ layer. TFET with $Si_{0.989}C_{0.011}$ layer achieves a steeper boron profile as compared to the TFET control device.



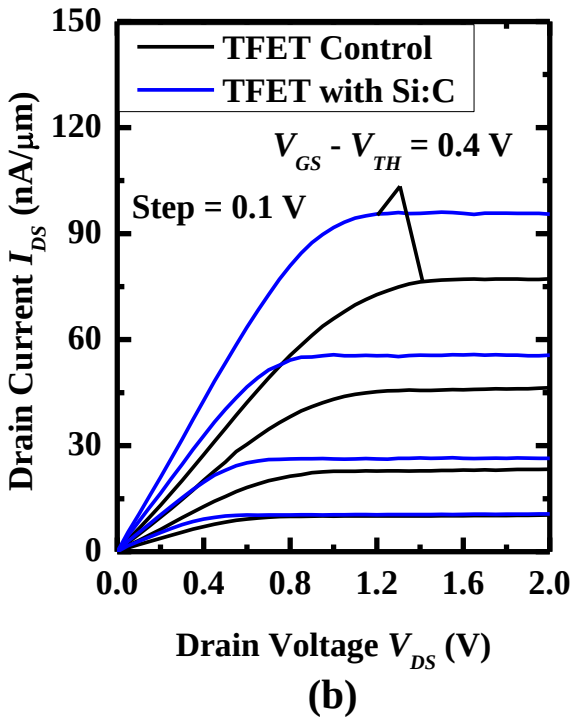


Fig. 3.14. (a) Comparison of the transfer characteristics of TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source and TFET control device. Both devices have L_G of 7 μm. (b) The output characteristics of the same pair of devices as shown in (a).

Fig. 3.14(a) shows the transfer characteristics of a TFET control device and a TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source structure. The insertion of the $Si_{0.989}C_{0.011}$ layer helps to achieve a higher I_{DS} at the same gate overdrive ($V_{GS} - V_{TH}$) and a steeper S. The threshold voltage V_{TH} was defined as the V_{GS} for $I_{DS} = 1 \times 10^{-9}$ A/μm at $V_{DS} = 0.5$ V. The output characteristics of the same pair of devices are shown in Fig. 3.14(b). As discussed in Section 2.3 of Chapter 2, the TFET has a resistance component associated with the tunneling junction R_{Tunnel}, which is dependent on V_{DS} as shown by the energy band diagrams in Fig. 3.15. Therefore, the slope of the I_{DS} - V_{DS} curve in the linear region is not the series resistance as the R_{Tunnel} component also affects this slope.

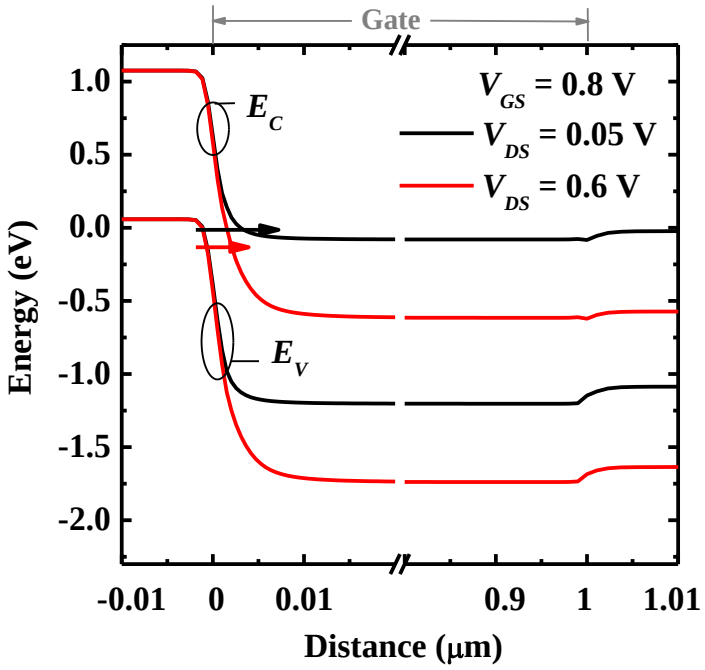


Fig. 3.15. Energy band diagram of a TFET along source-to-drain direction for $V_{DS} = 0.05$ V and $V_{DS} = 0.6$ V. The tunneling barrier width changes with V_{DS} as shown by the black and red arrows.

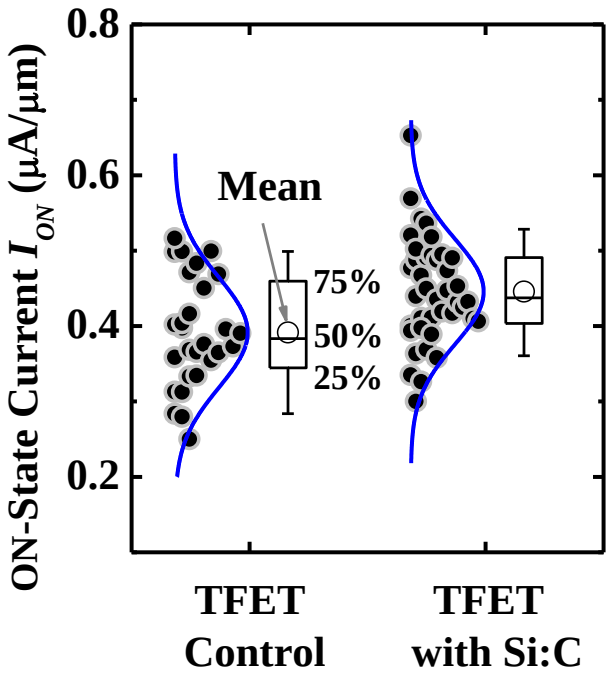


Fig. 3.16. Statistical plot of I_{ON} for TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source and TFET control device. A ~20% enhancement of I_{ON} is obtained due to the insertion of the $Si_{0.989}C_{0.011}$ layer between p^+ $Si_{0.5}Ge_{0.5}$ source and Si channel.

Fig. 3.16 is a statistical plot of I_{ON} for the two splits. I_{ON} was defined as the I_{DS} at $V_{DS} = V_{GS} - V_{TH} = 1$ V. A ~20% enhancement of I_{ON} was observed by inserting a $Si_{0.989}C_{0.011}$ layer underneath the p^+ $Si_{0.5}Ge_{0.5}$ source. This current enhancement is mainly attributed to the presence of the stress/strain in the $Si_{0.989}C_{0.011}$ layer, leading to the increase of conduction band offset between $Si_{0.5}Ge_{0.5}$ and $Si_{0.989}C_{0.011}$. In addition, the insertion of $Si_{0.989}C_{0.011}$ layer can suppress boron diffusion and help to achieve a steeper boron profile, which also contributes to the I_{ON} enhancement. Due to the existence of defects at the $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$/Si interfaces, the measured result shows a lower I_{ON} enhancement as compared to the simulated one (Fig. 3.7). Nevertheless, both simulation and experimental results show that I_{ON} is enhanced by inserting a $Si_{0.989}C_{0.011}$ layer.

The steeper boron profile due to the insertion of $Si_{0.989}C_{0.011}$ layer also contributes to a smaller *S* [20],[32]. Fig. 3.17 is a cumulative probability plot of the average *S* in TFETs with and without $Si_{0.989}C_{0.011}$ layer. The average *S* was found for I_{DS} changing from 5×10^{-12} to 5×10^{-11} A/μm at V_{DS} = 0.5 V. By inserting a $Si_{0.989}C_{0.011}$ layer, the median *S* of the TFETs reduces from 177 mV/decade to 131 mV/decade. Compared to the control devices, TFETs with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source achieve a ~26% improvement in the median *S*.

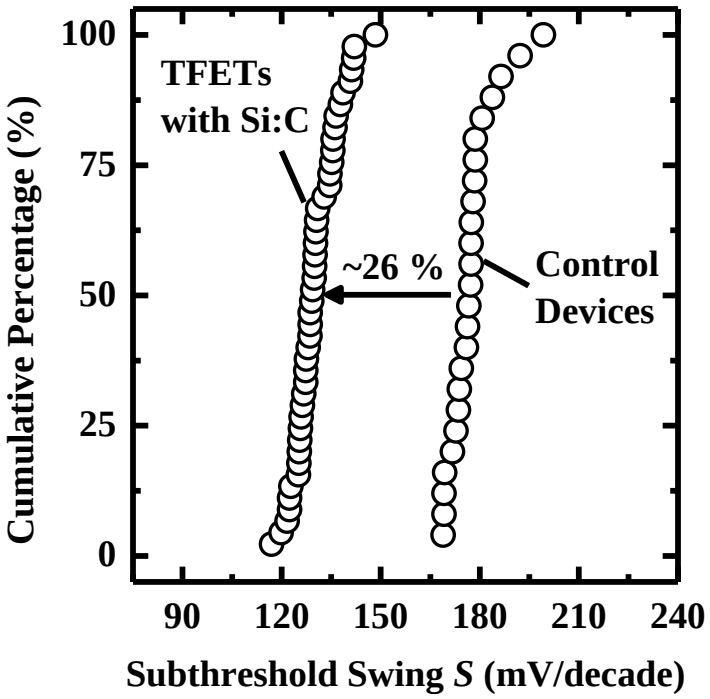


Fig. 3.17. Cumulative probability plot shows the enhancement of *S* due to the insertion of a $Si_{0.989}C_{0.011}$ layer. The median *S* of TFETs with and without $Si_{0.989}C_{0.011}$ layer are 131 mV/decade and 177 mV/decade, respectively. The $Si_{0.989}C_{0.011}$ layer can suppress the boron diffusion and form an abrupt p^+ dopant profile, which contributes to a steeper *S*.

3.5 Summary

In this Chapter, source engineering for TFET with *in situ* boron-doped $Si_{0.5}Ge_{0.5}$ source was investigated and the impact of inserting a strained $Si_{0.989}C_{0.011}$ layer underneath the $Si_{0.5}Ge_{0.5}$ source was explored. Compared with a control device, TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}$ source exhibits an enhanced I_{ON} and S. The presence of strain in the $Si_{0.989}C_{0.011}$ layer increases the conduction band offset between $Si_{0.5}Ge_{0.5}$ and $Si_{0.989}C_{0.011}$, which effectively reduces the tunneling barrier. In addition, the $Si_{0.989}C_{0.011}$ layer suppresses boron diffusion, which helps to realize a steeper boron profile. These factors contribute to the enhanced TFET performance. It is anticipated that higher level of substitutional C concentration in the Si:C layer can be used to further enhance the I_{ON} and S of TFETs.

Chapter 4

Tunneling Field-Effect Transistor (TFET) with Ge/$In_{0.53}Ga_{0.47}As$ Heterostructure as Tunneling Junction

4.1 Introduction

According to Kane's model [73] (Section 1.2.2 of Chapter 1), the band-to-band tunneling generation rate G_{BTBT} in tunneling field-effect transistor (TFET) has a near exponential dependence on the bandgap E_G of the material at the tunneling junction. Although silicon (Si)-based TFETs are more manufacturable due to the advances of Si processing technology as discussed in Chapter 3, the large E_G of Si limits its application in TFET as G_{BTBT} is generally small for Si. Various techniques to boost the on-state current I_{ON} of Si-based TFETs have been proposed, such as use of dopant steepening implant [32], dopant segregation [33], nanowire structure [36],[125]-[126], and strain engineering [30],[77],[93]-[94]. However, none of these techniques has enabled TFETs to achieve a drive current that meets the requirement set in the International Technology Roadmap for Semiconductors (ITRS) for low power logic applications [75].

To achieve a high G_{BTBT} and I_{ON}, small bandgap materials such as germanium (Ge) and III-V materials with E_G less than ~0.7 eV should be employed. Simulation showed that InAs (E_G = 0.35 eV) TFET can achieve a I_{ON} that is ~2 orders of magnitude higher than that of Si TFET [51]. Research effort is now focused on III-V TFETs [47],[50],[52]-[65]. $In_{0.53}Ga_{0.47}As$ TFET, as reported by Mookerjea *et al.*[47], achieved a I_{ON} of 20 μA/μm with a subthreshold swing S of 250 mV/decade at gate voltage V_{GS} of 2.5 V and drain voltage V_{DS} of 0.75 V. Zhao *et al.* [52] further improved the I_{ON} of InGaAs TFET to 40 μA/μm (V_{GS} = V_{DS} = 1 V) with an S of 84 mV/decade by using $In_{0.7}Ga_{0.3}As$, which has a smaller E_G than $In_{0.53}Ga_{0.47}As$.

Another approach to achieve high I_{ON} is by using heterostructures with a staggered band alignment at the tunneling junction as discussed in Section 1.2.3 of Chapter 1. With the staggered band alignment, the length of the tunneling path is effectively reduced, increasing G_{BTBT} and therefore I_{ON}. It was reported that TFET with $In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As$ heterostructure outperforms $In_{0.53}Ga_{0.47}As$ homostructure TFET in terms of I_{ON} and S [61]. Recently, TFET with a high I_{ON} of ~190 μA/μm at V_{GS} of 2.5 V and V_{DS} of 0.75 V was achieved using $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterostructure tunneling junction [62]. TFET with $InAs/Al_{0.45}Ga_{0.55}Sb$ tunneling junction having a staggered band alignment was also experimentally demonstrated [64].

In this Chapter, lateral TFET with $Ge/In_{0.53}Ga_{0.47}As$ tunneling junction was experimentally realized for the first time (Fig. 4.1). The device concept and experimental results are discussed in detail. To fabricate such a TFET, the process module of Ge growth on $In_{0.53}Ga_{0.47}As$ substrate is needed. Ge growth on

$In_{0.53}Ga_{0.47}As$ is an interesting topic because of its potential applications in high-mobility channel metal-oxide-semiconductor field-effect transistors (MOSFETs) and optical devices [127]-[130]. However, it remains a challenge to grow high quality Ge on $In_{0.53}Ga_{0.47}As$ substrate due to the large lattice mismatch of ~3.7% between them. High quality Ge was successfully grown on $In_{0.53}Ga_{0.47}As$ using a metal-organic chemical vapor deposition (MOCVD) tool in this work.

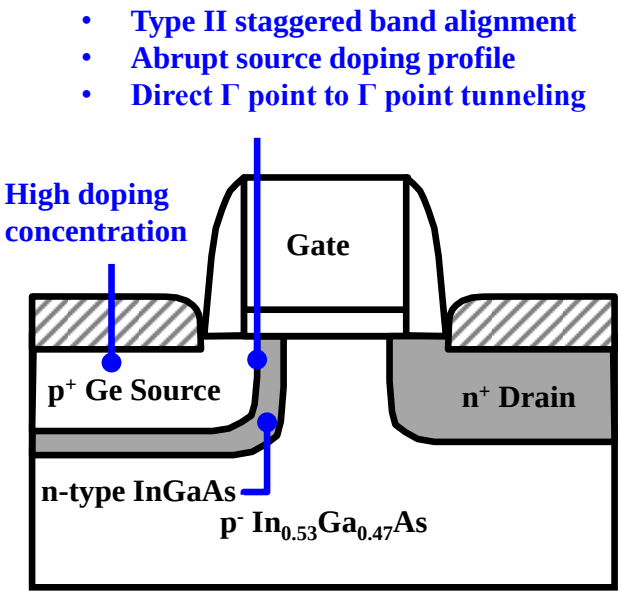


Fig. 4.1. Schematic showing the key features of a TFET with Ge/$In_{0.53}Ga_{0.47}As$ tunneling junction.

4.2 Device Concept and Design

Fig. 4.1 shows a schematic of a lateral TFET with Ge/$In_{0.53}Ga_{0.47}As$ tunneling junction. This structure has several advantages. Firstly, the Ge/$In_{0.53}Ga_{0.47}As$ interface has a staggered band alignment. The energy of the valence band edge in Ge is higher than that in $In_{0.53}Ga_{0.47}As$, which can help to reduce the length of the tunneling path L_T. In TFET, the tunneling current is exponentially dependent on the L_T. With a shorter tunneling path as compared to a homojunction under the same bias condition, a heterostructure tunneling junction with a staggered band alignment can achieve a higher I_{ON}.

Secondly, an abrupt p-type dopant profile at the Ge/$In_{0.53}Ga_{0.47}As$ interface can be formed. The p-type dopant gallium (Ga) in Ge is not a dopant in $In_{0.53}Ga_{0.47}As$; therefore, it is not a problem even if the Ga atoms diffuse from Ge into $In_{0.53}Ga_{0.47}As$. In addition, the diffusion of Ge into $In_{0.53}Ga_{0.47}As$ can result in an n-type $In_{0.53}Ga_{0.47}As$ layer at the tunneling junction since the diffused Ge atoms are n-type dopants in $In_{0.53}Ga_{0.47}As$. The presence of n-type $In_{0.53}Ga_{0.47}As$ layer adjacent to the p^+ Ge source can boost the electric field at the tunneling junction and increase the I_{ON} as illustrated in Fig. 4.2(a) [20],[32].

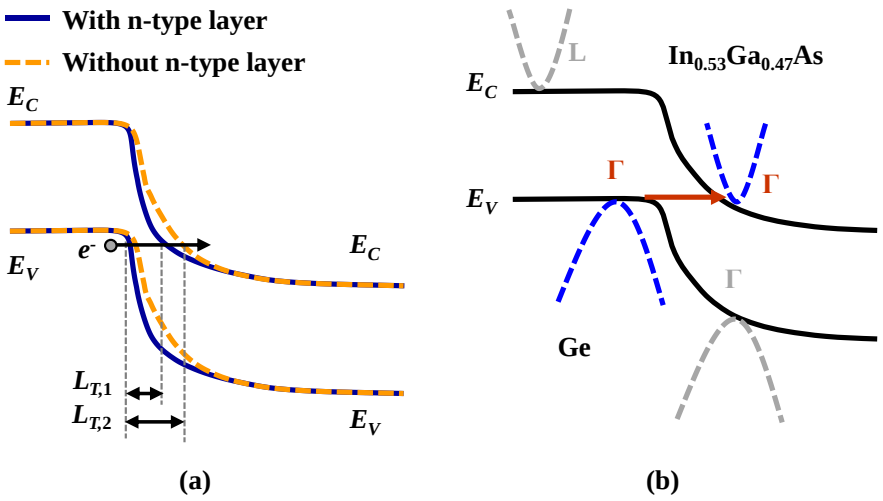


Fig. 4.2. (a) Schematic of energy band diagrams along source-to-drain direction at the tunneling junction regions of two homostructure TFETs. The first TFET has an n-type layer between the p^+ source and the channel, whereas the second TFET does not have such an n-type layer. E_C and E_V are the energies of the conduction band edge and valence band edge, respectively. The presence of the n-type layer in the first TFET contributes to a higher electric field at the tunneling junction as indicated by the steeper slope of the E_C. This higher electric field leads to a shorter $L_{T,1}$ as compared to $L_{T,2}$. (b) Schematic of energy band diagrams along source-to-drain direction at the tunneling junction regions of TFET with Ge/$In_{0.53}Ga_{0.47}As$ heterostructure. Electrons directly tunnel from the Γ point of the valence band in Ge to the Γ point of the conduction band in $In_{0.53}Ga_{0.47}As$.

Thirdly, the tunneling current in this structure is determined by direct band-to-band tunneling (BTBT), where electrons tunnel from the Γ point of the valence band in Ge to the Γ point of the conduction band in $In_{0.53}Ga_{0.47}As$ [Fig. 4.2(b)]. This is because $In_{0.53}Ga_{0.47}As$ in the channel is a direct bandgap material. This direct Γ-to-Γ point tunneling does not require the assistance of phonons and is expected to have a higher tunneling probability than indirect tunneling [76].

Lastly, the epitaxial Ge grown on $In_{0.53}Ga_{0.47}As$ can be *in situ* Ga-doped to form p^+ Ge. The *in situ* doping contributes to a high doping concentration in the Ge source region, which can also help to increase the drive current. Fig. 4.1 summarizes the key features of the device design in this work.

Fig. 4.3 compares the simulated I_{DS} - V_{GS} characteristics of a homojunction $In_{0.53}Ga_{0.47}As$ TFET and a TFET with Ge/$In_{0.53}Ga_{0.47}As$ heterojunction at V_{DS} = 0.5 V. In this simulation, the simulator used implements a non-local algorithm for accurate calculation of the BTBT current across a heterojunction. The details of the simulator can be found elsewhere [122]-[123]. For this simulation, the device parameters used were: source acceptor concentration $N_A = 1 \times 10^{20}$ cm^{-3}, drain donor concentration $N_D = 1 \times 10^{19}$ cm^{-3} with a profile of 10 nm/decade into the channel, body doping $N_A = 1 \times 10^{16}$ cm^{-3}, equivalent oxide thickness (EOT) = 0.8 nm, gate length L_G = 200 nm, the length of gate-to-source overlap $L_{OV,GS}$ and gate-to-drain overlap $L_{OV,GD}$ = 10 nm. A 5 nm thick n-type $In_{0.53}Ga_{0.47}As$ layer ($N_D = 1 \times 10^{18}$ cm^{-3}) with an abrupt doping profile was inserted at the tunneling junction. A homostructure $In_{0.53}Ga_{0.47}As$ TFET was simulated as reference using the same set of parameters without the n-type layer at the tunneling junction.

The S of the TFET with Ge/$In_{0.53}Ga_{0.47}As$ tunneling junction is much smaller than that of the $In_{0.53}Ga_{0.47}As$ TFET. We define V_{leak_floor} to be the maximum gate voltage in the off-state leakage floor region of the I_{DS} - V_{GS} curve, i.e. just before I_{DS} rises sharply with increasing V_{GS}. For a fair comparison, the gate work functions of TFET with Ge/$In_{0.53}Ga_{0.47}As$ tunneling junction and $In_{0.53}Ga_{0.47}As$ homojunction TFET were set to be 4.3 eV and 4.1 eV, respectively, so that the values of V_{leak_floor} were the same. It can be observed that TFET with Ge/$In_{0.53}Ga_{0.47}As$ tunneling junction can achieve a higher I_{ON} as compared to the $In_{0.53}Ga_{0.47}As$ TFET.

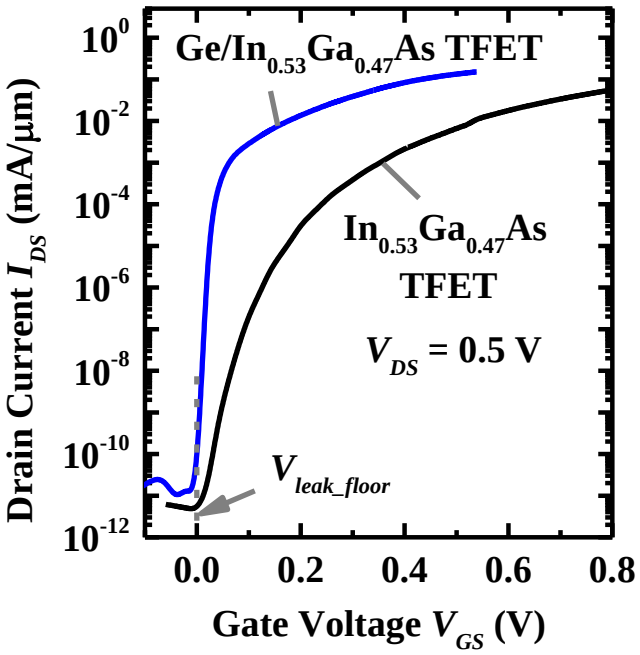


Fig. 4.3. I_{DS} - V_{GS} curves for $In_{0.53}Ga_{0.47}As$ TFET and TFET with $Ge/In_{0.53}Ga_{0.47}As$ tunneling junction at V_{DS} = 0.5 V. Both I_{ON} and S of TFET are improved by employing $Ge/In_{0.53}Ga_{0.47}As$ heterojunction as the tunneling junction.

4.3 Device Fabrication

Fig. 4.4 illustrates some of the processing steps for the fabrication of $In_{0.53}Ga_{0.47}As$-channel TFET with lateral Ge source using a gate-last process. A 2-inch (100)-oriented semi-insulating InP wafer with an overlying 500 nm thick epitaxial p-type $In_{0.53}Ga_{0.47}As$ layer (N_A = ~5 × 10^{16} cm^{-3}) was used as the starting substrate. After degreasing in acetone, isopropanol, and de-ionized water, a 20 nm thick sacrificial aluminum oxide (Al_2O_3) was deposited using an atomic layer deposition (ALD) tool to protect the wafer surface during subsequent processing steps [Fig. 4.4(a)].

Drain was formed by a masked Si^+ implantation at an energy of 40 keV and a dose of 1 × 10^{14} cm^{-2} [Fig. 4.4(b)]. The dopants would be subsequently activated during a Ge epitaxial growth at 650 ˚C. A layer of 200 nm thick silicon dioxide (SiO_2) was then deposited by a plasma-enhanced chemical vapor deposition (PECVD) and patterned to expose the source region. This SiO_2 layer acts as a mask for recess etch of $In_{0.53}Ga_{0.47}As$ by a chlorine (Cl_2)-based plasma process. The wafer was then treated in dilute sulfuric peroxide mixture (SPM) for 10 s to remove a thin layer of $In_{0.53}Ga_{0.47}As$ that was damaged during plasma etching. Pre-epitaxial cleaning using concentrated sulfuric acid (H_2SO_4) (96%) for 1 minute was performed before the wafer was loaded into an MOCVD system for Ge epitaxial growth. A blanket $In_{0.53}Ga_{0.47}As$/InP sample was also included for characterization of the epitaxial Ge film.

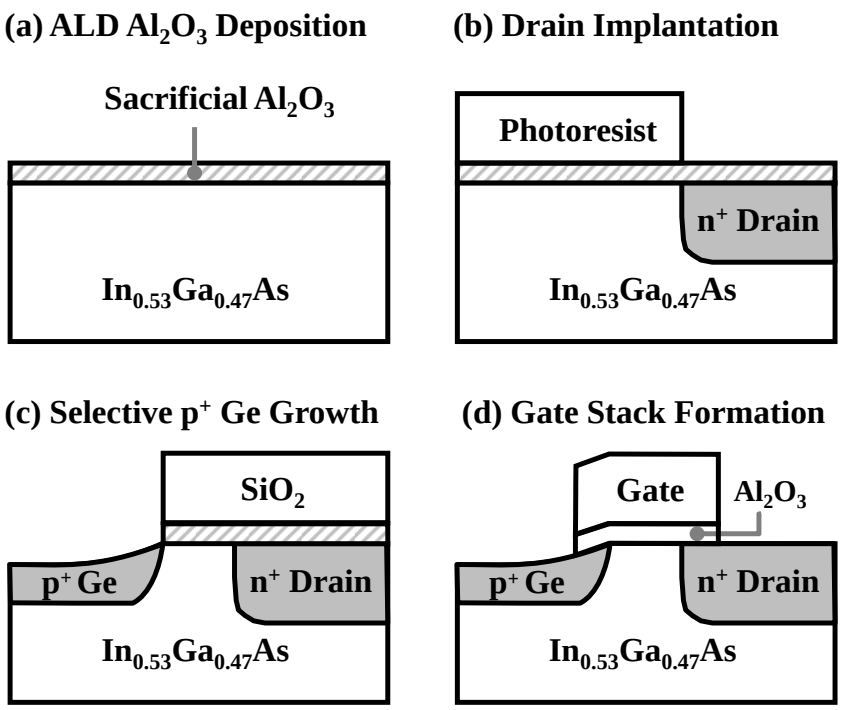


Fig. 4.4. Processing steps used in the fabrication of Ge-source $In_{0.53}Ga_{0.47}As$-channel TFET: (a) deposition of a 20 nm thick sacrificial ALD Al_2O_3; (b) Si^+ implantation to form n^+ doped drain region; (c) recess etching into $In_{0.53}Ga_{0.47}As$ followed by selective growth of p^+ Ge by MOCVD; (d) formation of gate stack comprising TaN on Al_2O_3.

After loading the samples into the MOCVD system, the substrate temperature was ramped up to about 380 ˚C when arsine (AsH_3) was flowed to suppress arsenic (As) out-diffusion. The wafers were then baked at 650 ˚C for 3.5 minutes to remove residual native oxide before Ge growth. Germane (GeH_4) with a flow rate of 20 sccm was used for Ge epitaxial growth. 10 sccm of trimethylgallium (TMGa) was introduced for *in situ* Ga-doping to form p^+ Ge. The pressure of the chamber was 100 mbar during growth [Fig. 4.4(c)].

The thickness of the as-grown Ge epitaxial layer was 50 nm. However, a thin layer of Ge also grew on the SiO_2 in the channel and drain regions. After Ge epitaxial growth, the wafers were treated in the mixture of ammonium hydroxide (NH_4OH,

31% by weight), hydrogen peroxide (H_2O_2, 28% by weight) and H_2O solution ($NH_4OH:H_2O_2:H_2O$ = 1:2:160) for 10 s before the sacrificial Al_2O_3 and SiO_2 on the channel and drain regions were removed using dilute hydrofluoric acid (HF). The final thickness of the epitaxial Ge layer on the source region was 29 nm.

Pre-gate cleaning process comprises native oxide and excess elemental arsenic removal using hydrochloric acid (HCl) and NH_4OH, respectively, and *ex situ* surface passivation using ammonium sulfide [$(NH_4)_2S$] [131]. Gate stack comprising of 5.6 nm of ALD Al_2O_3 and 120 nm of reactive-sputtered tantalum nitride (TaN) was formed. A Cl_2-based plasma was used to define the gate electrode [Fig. 4.4(d)]. Finally, a 10 nm thick nickel (Ni) layer was deposited and annealed at 350 ˚C for 30 s using a lift-off process to form the contact. This completed the device fabrication process.

4.4 Results and Discussion

4.4.1 Material Analysis

X-ray diffraction (XRD) characterization was performed on a blanket Ge/$In_{0.53}Ga_{0.47}As$ sample. Fig. 4.5 shows the XRD results. The well-defined Ge peak indicates the good quality of the epitaxial Ge film. Fig. 4.6 shows the surface roughness measured using atomic force microscopy (AFM). The Ge surface has a low surface roughness with a root mean square (RMS) value of 0.54 nm over a 5 μm × 5 μm scan area.

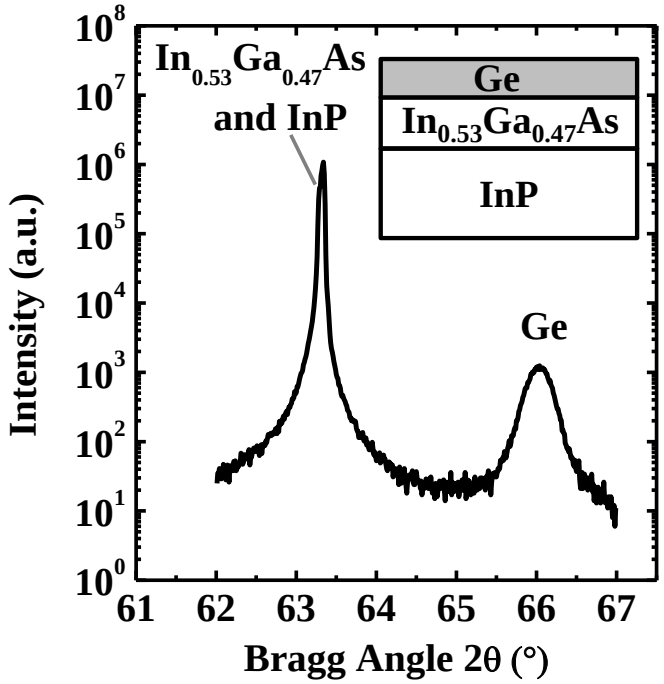


Fig. 4.5. High-resolution XRD curve of a blanket Ge/$In_{0.53}Ga_{0.47}As$ sample. The inset shows the layer structure of this sample. The Ge peak is clearly observed. The peaks from $In_{0.53}Ga_{0.47}As$ and InP substrate appear at the same Bragg angle as they have the same lattice constant.

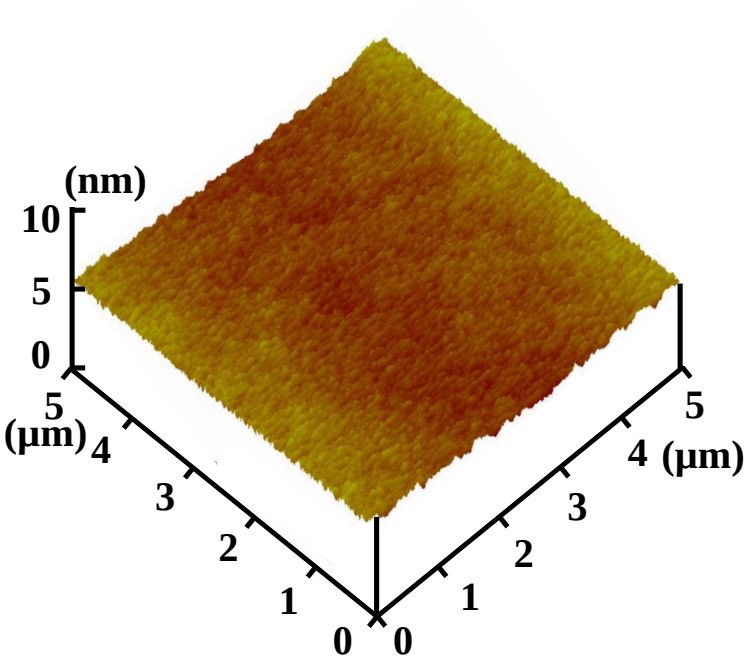


Fig. 4.6. The RMS surface roughness for a 5 μm × 5 μm area is 0.54 nm, indicating that a smooth Ge surface was obtained.

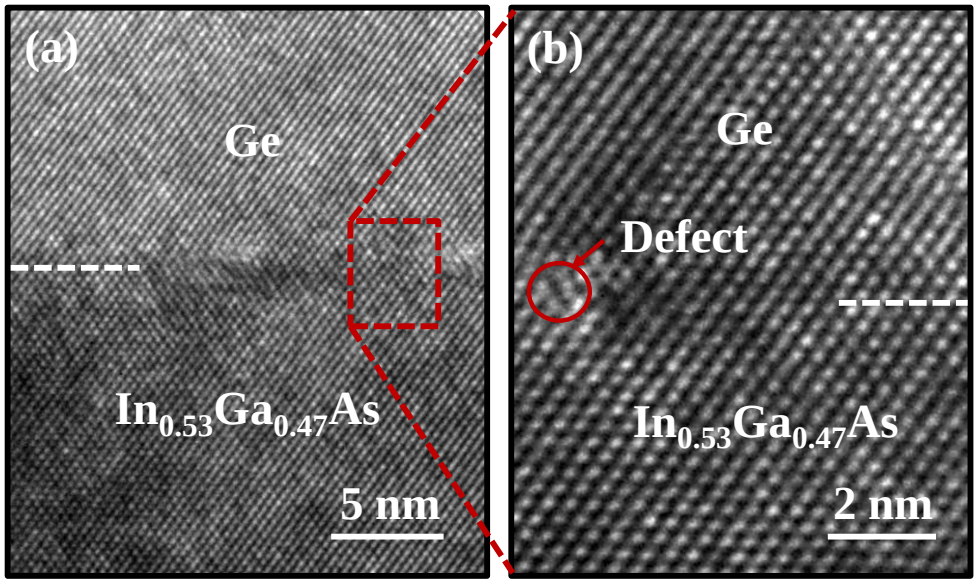


Fig. 4.7. (a) High-resolution TEM image of 50 nm thick Ge epitaxially grown on $In_{0.53}Ga_{0.47}As$ substrate. (b) TEM image at the Ge/$In_{0.53}Ga_{0.47}As$ interface indicated by the dashed box in (a). High quality Ge film was formed and defects were only observed at the interface.

Fig. 4.7 shows the high-resolution transmission electron microscope (TEM) images of a 50 nm thick epitaxial Ge film grown on $In_{0.53}Ga_{0.47}As$ substrate. Fig. 4.7(b) is a zoomed-in view of the Ge/$In_{0.53}Ga_{0.47}As$ interface. High quality Ge with no observable defects was successfully grown. However, some defects are observed at the Ge/$In_{0.53}Ga_{0.47}As$ interface due to the large lattice mismatch between Ge and $In_{0.53}Ga_{0.47}As$. As a result, the Ge film is almost fully relaxed as determined using Raman spectroscopy.

Fig. 4.8 shows the Raman spectra for the $In_{0.53}Ga_{0.47}As$ sample with a 50 nm thick epitaxial Ge layer and for a bulk Ge reference sample obtained using 532 nm laser. The Raman spectra were taken at room temperature in a (001) backscattering geometry. The amount of strain in the epitaxial Ge layer can be calculated from the Raman shift ($\Delta\omega$) relative to the bulk Ge peak using

$$\Delta\omega = b\varepsilon_{//}, \tag{4.1}$$

where $\varepsilon_{//}$ is the biaxial tensile strain and $b = [q - p(C_{12}/C_{11})]/\omega_o$. q and p are the optical photon anharmonic parameters, ω_o is the Raman frequency in bulk Ge, C_{11} and C_{12} are the elastic constants of bulk Ge [132]. Parameter b has a value of - (415 ± 40) cm^{-1} according to Refs. [130] and [133]. The small $\Delta\omega$ of -0.85 cm^{-1} corresponds to a tensile strain of only ~0.2%, indicating that the Ge film is almost fully relaxed.

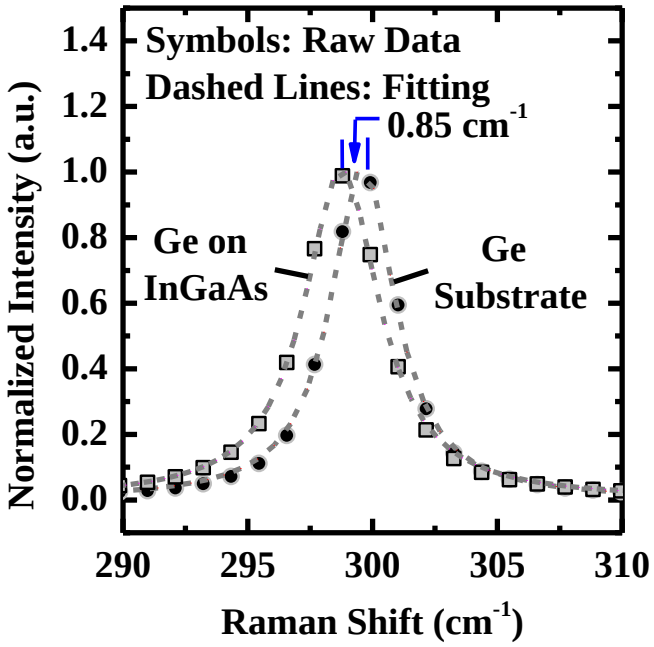


Fig. 4.8. Raman spectra of a bulk Ge sample and an $In_{0.53}Ga_{0.47}As$ sample topped by 50 nm thick Ge film. Lorentzian functions were fitted to the spectra. The small shift of the Ge peak with respect to that of bulk Ge indicates the epitaxial Ge film is almost fully relaxed.

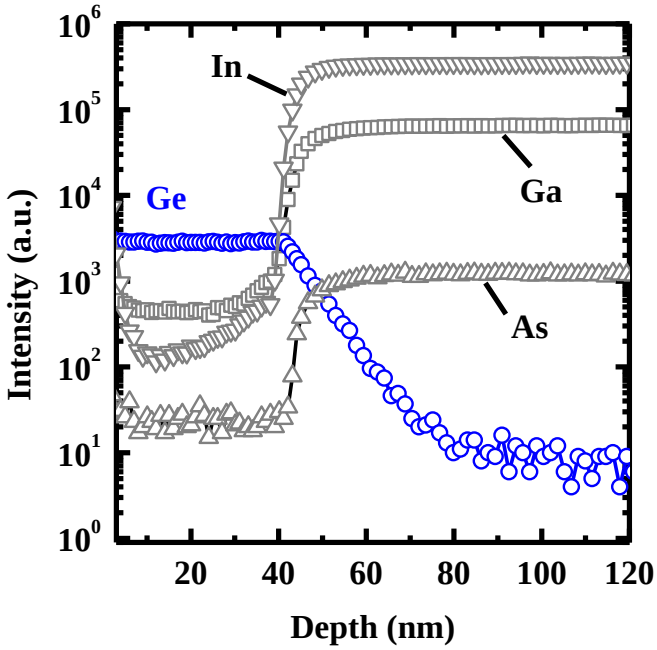


Fig. 4.9. SIMS analysis of the Ge/$In_{0.53}Ga_{0.47}As$ sample indicates that Ge atoms diffuse into $In_{0.53}Ga_{0.47}As$. As a result, an n-type $In_{0.53}Ga_{0.47}As$ layer is formed at the Ge/$In_{0.53}Ga_{0.47}As$ interface. This n-type layer enhances the lateral electric field at the tunneling junction, which can contribute to a higher TFET drive current.

Secondary ion mass spectrometry (SIMS) was performed to examine the Ge profile at the Ge/$In_{0.53}Ga_{0.47}As$ interface, as shown in Fig. 4.9. A low energy Ar^+ beam was used in the SIMS analysis to improve the depth resolution of the Ge profile. It is clearly observed that the Ge profile decays into the $In_{0.53}Ga_{0.47}As$ layer with a slope of 15 nm/decade. It is well known that inter-diffusion of Ge, Ga, and As atoms occurs easily at the Ge/GaAs interface [134]-[136]. As the growth temperature for Ge on $In_{0.53}Ga_{0.47}As$ used in this work is 650 ˚C, it is expected that Ge atoms will diffuse into $In_{0.53}Ga_{0.47}As$ substrate. Since Ge atoms are n-type dopants in $In_{0.53}Ga_{0.47}As$, a p^+ Ge/n-type $In_{0.53}Ga_{0.47}As$/p-type $In_{0.53}Ga_{0.47}As$/n^+ $In_{0.53}Ga_{0.47}As$ (p^+npn^+) structure is formed, which can contribute to improved TFET performance.

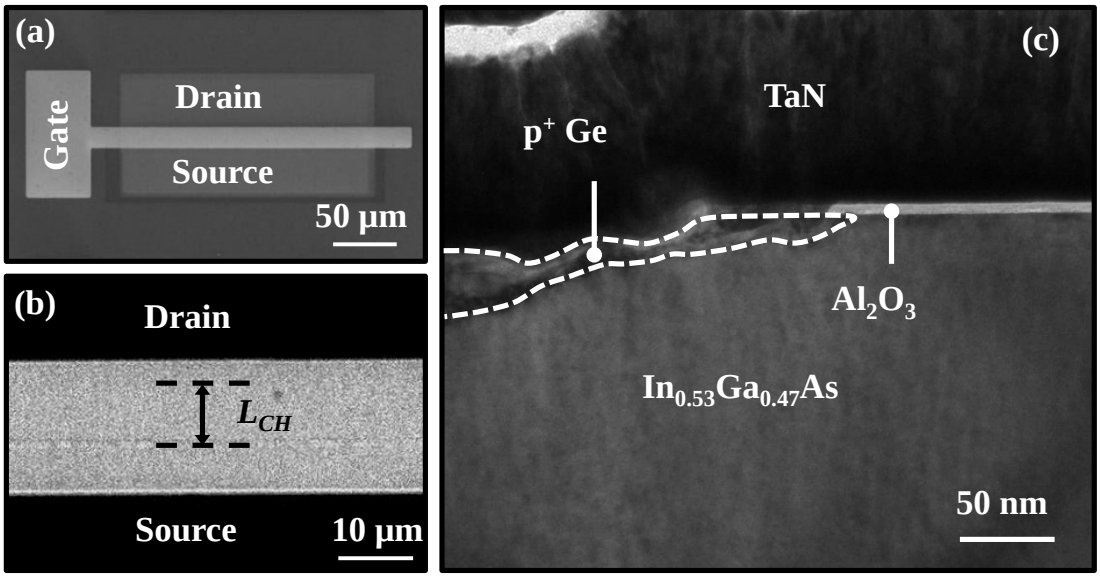


Fig. 4.10. (a) Top-view SEM image of a fabricated TFET. (b) Zoomed-in view of the same device in (a). The gate-to-source overlap $L_{OV,GS}$ of 5 µm is clearly observed. The channel length L_{CH} is 8 µm. (c) TEM image of a fabricated TFET device showing the tunneling junction region.

Hall measurement was carried out on a blanket Ge/$In_{0.53}Ga_{0.47}As$ sample. A hole concentration as high as 3×10^{20} cm^{-3} was achieved in the Ge layer. This high doping concentration shortens the tunneling distance and helps to increase the tunneling rate in a TFET.

Fig. 4.10(a) is a top-view scanning electron microscope (SEM) image of a fabricated Ge-source $In_{0.53}Ga_{0.47}As$-channel TFET. The SEM image in Fig. 4.10(b) clearly shows the gate-to-source overlap region. The channel length L_{CH} of the device is 8 μm. Fig. 4.10(c) is a TEM image of a TFET device showing the tunneling junction region. The thickness of the Al_2O_3 gate dielectric layer is ~5.6 nm. From Fig. 4.10(c), it is observed that the Ge surface is very rough in the tunneling junction region. However, in the source region that is away from the tunneling junction, the Ge surface is still quite smooth as shown by the TEM image in Fig. 4.11. The rough Ge surface in the tunneling junction region could be caused by the rough $In_{0.53}Ga_{0.47}As$ surface due to recess etching in Cl_2-based plasma. In addition, the thinning-down of the Ge layer after epitaxial growth can also roughen the Ge surface. This rough Ge surface may cause a high gate leakage current as the surface roughness can enhance the average electric field inside the gate dielectric [137]-[138]. However, it should not have a large impact on the tunneling current of the device.

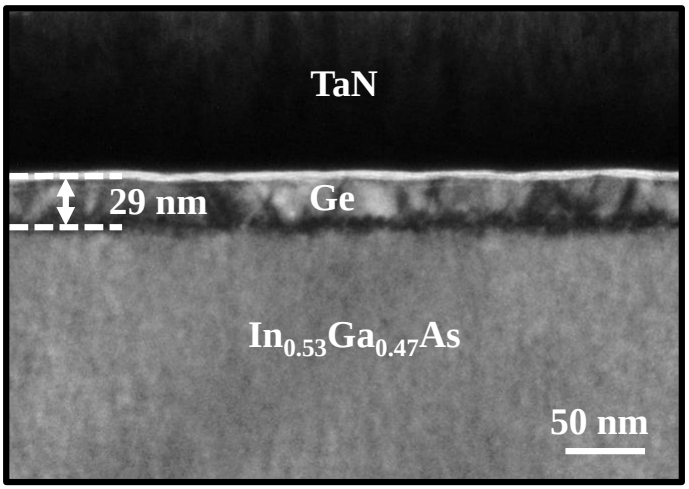


Fig. 4.11. TEM image of the gate-to-source overlap region. Ge film has a smooth surface on the etched $In_{0.53}Ga_{0.47}As$ surface.

4.4.2 Band Alignment Study

The band alignment between Ge and $In_{0.53}Ga_{0.47}As$ is an important device design consideration. However, the band alignment at the Ge/$In_{0.53}Ga_{0.47}As$ interface has not been reported. In this Chapter, the band alignment at the Ge/$In_{0.53}Ga_{0.47}As$ interface was investigated using high-resolution x-ray photoelectron spectroscopy (XPS). Two samples were used to measure the valence band offset ΔE_V between Ge and $In_{0.53}Ga_{0.47}As$. The first comprises 50 nm thick Ge grown on 500 nm thick $In_{0.53}Ga_{0.47}As$. The second is a 500 nm thick $In_{0.53}Ga_{0.47}As$ reference sample.

The measurements were performed on a VG ESCALAB 200i-XL system equipped with a monochromatic Al $K\alpha$ (1486.6 eV) x-ray source. All of the high-resolution spectra were collected in the constant pass energy mode with pass energy of 20 eV. Pure gold (Au), silver (Ag), copper (Cu), and Ni standard samples were used to calibrate the binding energy by setting the Au $4f_{7/2}$, Ag $3d_{5/2}$, Cu $2p_{3/2}$ peaks, and Ni Fermi edge at binding energies of 83.98 ± 0.02 eV, 368.26 ± 0.02 eV, 932.67

± 0.02 eV, and 0.00 ± 0.02 eV, respectively. Before XPS measurement was performed, both samples were subjected to Ar ion sputtering to remove the native oxide. By comparing the XPS spectra before and after sputtering, we note that the XPS peaks corresponding to native oxide disappeared. However, there are no significant changes in the shape and binding energies of the XPS spectra. Hence, the damage due to sputtering does not affect the XPS measurement in this study.

The technique proposed by Kraut *et al.* [139]-[140] has been widely used to study the valence band offset for heterojunction systems [141]-[145]. In this technique, the ΔE_V and conduction band offset ΔE_C between material X and Y can be obtained from

$$\Delta E_V = (E_{CL}^X - E_V^X) - (E_{CL}^Y - E_V^Y) + \Delta E_{CL}^i , \tag{4.2}$$

$$\Delta E_C = (E_G^X + \Delta E_V) - E_G^Y , \tag{4.3}$$

where E_{CL} and E_V are the binding energies of the core-level electron and valence band edge, respectively; the superscripts X and Y in E_{CL}, E_V and E_G refer to material X and Y, respectively; ΔE_{CL}^i is the core-level binding energy difference between the two materials at the interface and it can be found using $\Delta E_{CL}^i = E_{CL}^X - E_{CL}^Y$ from the XPS spectra obtained at the interface between material X and Y as illustrated in Fig. 4.12.

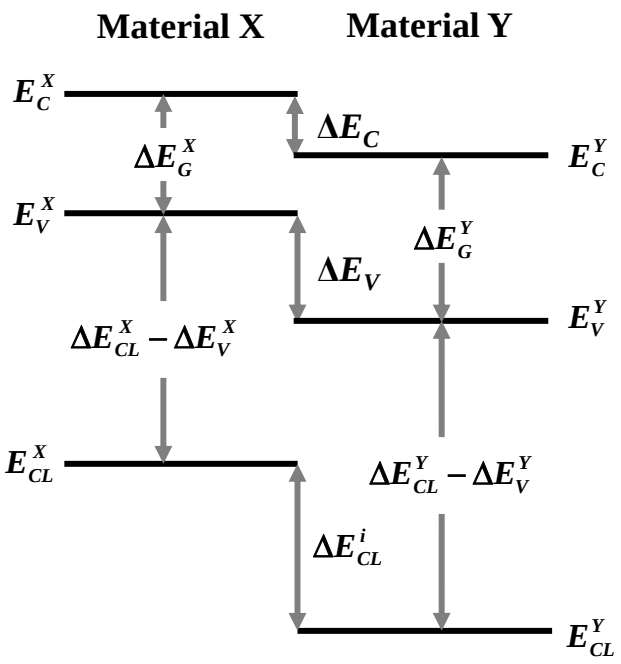
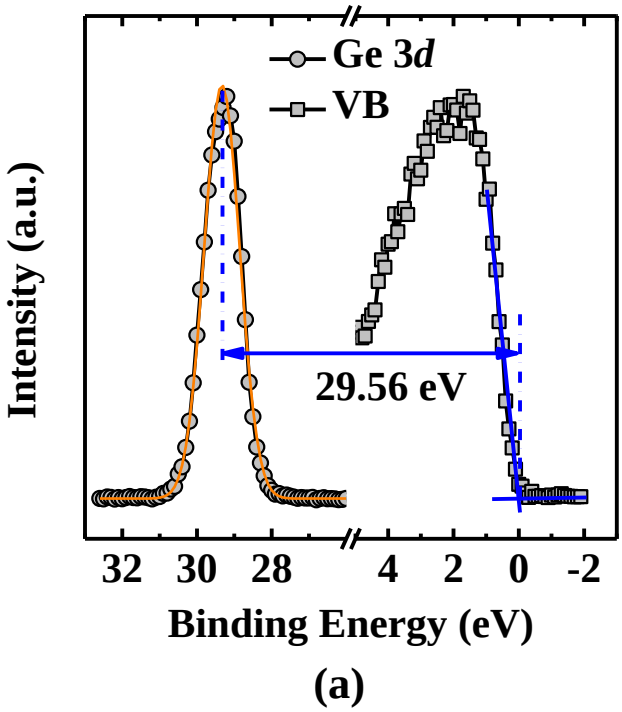


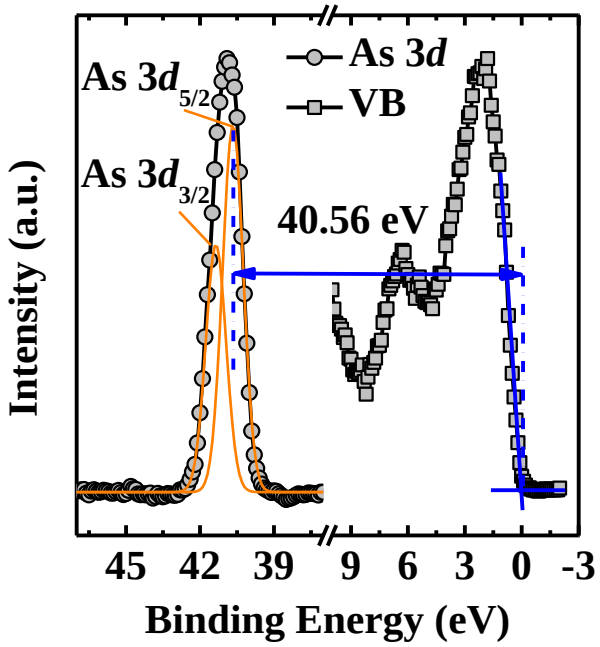
Fig. 4.12. Schematic illustrates the band alignment between material X and Y. ΔE_V and ΔE_C between these two materials can be calculated using the technique proposed by Kraut *et al*. [139]-[140].

The core-level spectra of Ge 3*d* from the top Ge film and As $3d_{5/2}$ from $In_{0.53}Ga_{0.47}As$ were used for the calculation of band offset because of their large information depth (lower binding energy). Therefore, strong signals from the interface and less experimental error are expected. The valence band offset between Ge and $In_{0.53}Ga_{0.47}As$ can be obtained using Equation (4.2) by substituting material X with Ge and Y with $In_{0.53}Ga_{0.47}As$:

$$\Delta E_V = (E_{CL}^{Ge3d} - E_V)^{Ge} - (E_{CL}^{As3d_{5/2}} - E_V)^{In_{0.53}Ga_{0.47}As} + \Delta E_{CL}^i . \qquad (4.4)$$



(a)



(b)

Fig. 4.13. (a) The Ge 3*d* core-level and valence band spectra for 50 nm thick Ge on $In_{0.53}Ga_{0.47}As$. (b) The As 3*d* core-level and valence band spectra for $In_{0.53}Ga_{0.47}As$ reference sample. The valence band maximum is extrapolated from the intersection point between the leading edge of the valence band spectrum and the base line.

Fig. 4.13 shows the valence band (VB) and core-level spectra obtained from the Ge film grown on $In_{0.53}Ga_{0.47}As$ [(Fig. 4.13(a)] and the $In_{0.53}Ga_{0.47}As$ reference sample [(Fig. 4.13(b)]. In Fig. 4.13(a), the valence band edge of the Ge film was determined by the intersection of the regression determined line segments defining the edge and the flat energy distribution curve in the energy gap region. It was found to be around 0 eV as the Ge film has a high concentration of holes. After careful curve fitting, the energy difference between valence band edge and the Ge 3*d* peak was found to be 29.56 eV. The valence band and core-level As 3*d* spectra of $In_{0.53}Ga_{0.47}As$ are shown in Fig. 4.13(b). The As $3d_{5/2}$ and $3d_{3/2}$ doublets were determined to be 40.67 eV and 41.36 eV, respectively. The valence band edge of $In_{0.53}Ga_{0.47}As$ was found to be 0.11 eV. Based on the doping concentration of $In_{0.53}Ga_{0.47}As$ (N_A = ~5 × 10^{16} cm^{-3}), the valence band maximum is calculated to be 0.13 eV below the Fermi-level, which agrees well with the XPS results. The energy difference between valence band edge and the As $3d_{5/2}$ peak from $In_{0.53}Ga_{0.47}As$ was determined to be 40.56 eV as indicated in Fig. 4.13(b).

To calculate the valence band offset, the interfacial core-level binding energy difference ΔE_{CL}^{i} between Ge and $In_{0.53}Ga_{0.47}As$ is needed. The 50 nm thick Ge on the $In_{0.53}Ga_{0.47}As$ sample was thinned down using Ar ion. ΔE_{CL}^{i} was obtained when the Ge layer was thin enough so that signals from both Ge and $In_{0.53}Ga_{0.47}As$ were obtained. The value of ΔE_{CL}^{i} was found to be 11.50 eV as shown in Fig. 4.14.

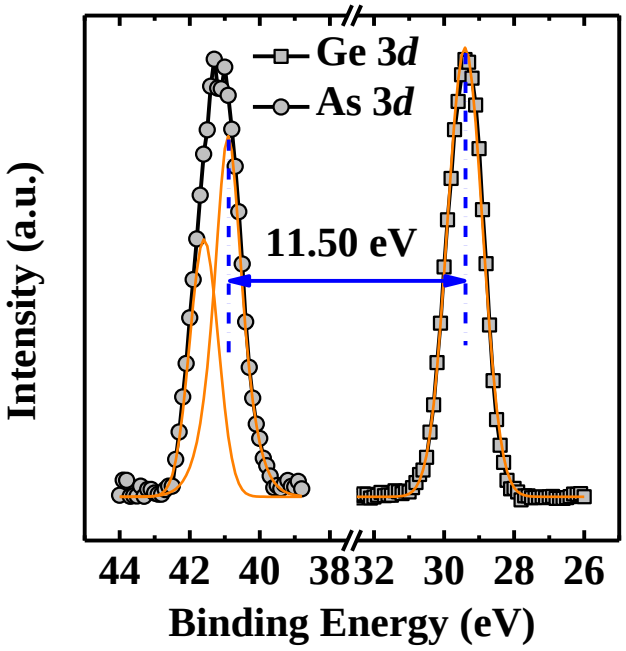


Fig. 4.14. The Ge 3*d* and As 3*d* core-level spectra from the Ge on $In_{0.53}Ga_{0.47}As$ sample after Ge was thinned down by Ar ion. Energy difference between the two core-levels is shown.

Therefore, the ΔE_V between Ge and $In_{0.53}Ga_{0.47}As$ was calculated to be 0.5 ± 0.1 eV. The error was due to the system limitations of the XPS tool. It is worthy to note that there is a small accumulation region in the p^+ Ge film. However, the measured valence band edge of Ge is in fact from the charge neutral region in Ge. This causes the obtained valence band offset to be slightly underestimated by the amount of band bending in Ge, which is very small (~0.02 eV) as compared to the error due to tool limitation.

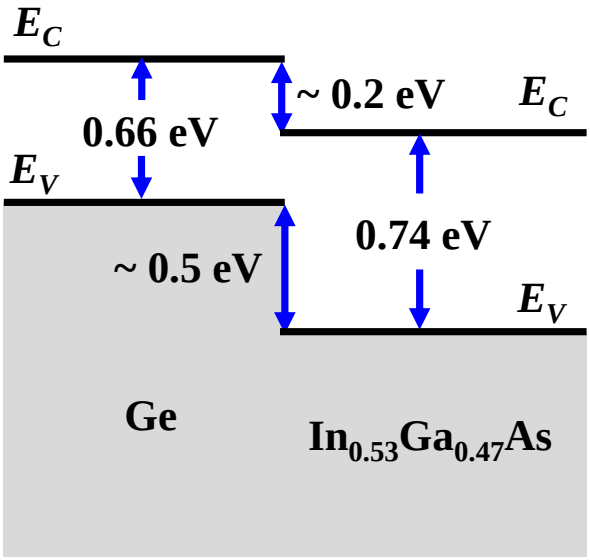


Fig. 4.15. The energy band alignment between Ge and $In_{0.53}Ga_{0.47}As$ is illustrated, showing the conduction band offset of 0.2 ± 0.1 eV and valence band offset of 0.5 ± 0.1 eV. The bandgap narrowing effect due to high doping concentration in Ge was taken into consideration.

The conduction band offset ΔE_C is determined next. From Hall measurement, the hole concentration in the Ge film was determined to be ~3 × 10^{20} cm^{-3}. The bandgap of Ge was estimated to be 0.47 eV taking the bandgap narrowing effect into consideration using

$$\Delta E_G = 8.21\times(N_A\times10^{-18})^{1/3} + 9.18\times(N_A\times10^{-18})^{1/4} + 5.77\times(N_A\times10^{-18})^{1/2}(\text{meV}), \quad (4.5)$$

where ΔE_G is the amount of bandgap narrowing and N_A is the doping concentration in the p-type Ge [146]. The ΔE_G is calculated to be 0.19 eV for N_A = 3 × 10^{20} cm^{-3}. The ΔE_C between Ge and $In_{0.53}Ga_{0.47}As$ can be obtained by a simple subtraction of the bandgap of $In_{0.53}Ga_{0.47}As$ (0.74 eV) from the sum of the valence band offset and bandgap of Ge (~0.47 eV). Therefore, the conduction band offset is found to be ~0.2 ± 0.1 eV. Fig. 4.15 illustrates the band alignment at the Ge/$In_{0.53}Ga_{0.47}As$ interface.

4.4.3 Electrical Characterization of TFETs

The staggered band alignment between Ge and $In_{0.53}Ga_{0.47}As$ makes this heterostructure a suitable candidate for the tunneling junction in a TFET. The large valence band offset contributes to a small tunneling path length, which is beneficial for the drive current of TFET. Fig. 4.16(a) shows the measured transfer characteristics of a fabricated TFET with L_{CH} of 8 µm. The $L_{OV,GS}$ and $L_{OV,GD}$ are 9 µm and 2 µm, respectively. The S of this device is ~177 mV/decade. All the S in this work was found at the steepest part of the I_{DS} - V_{GS} curve at V_{DS} = 0.2 V. The output characteristics of the same device are shown in Fig. 4.16(b).

Fig. 4.17 shows the I_{DS} - V_{GS} characteristics of a TFET measured under various temperatures ranging from 240 to 330 K in steps of 30 K at V_{DS} of 0.2 V. When V_{GS} is less than ~0.25 V, the device is in the off-state. The off-state leakage current I_{OFF} of the device was defined as the I_{DS} at V_{GS} = - 1.0 V.

Fig. 4.18 is an Arrhenius plot of $\ln(I_{OFF}/T^{3/2})$ versus $1/kT$, where k is the Boltzmann constant and T is the temperature. The linear relationship between $\ln(I_{OFF}/T^{3/2})$ and $1/kT$ indicates that the I_{OFF} is mainly due to Shockley-Read-Hall (SRH) generation-recombination current. SRH-dominated leakage current floor is a function of the intrinsic carrier concentration n_i, which is proportional to $e^{-E_G/2kT}$. The slope of the fitted curve is 0.27 eV, which is about half the bandgap of Ga-doped Ge, considering the bandgap narrowing effect. This indicates that the leakage current is dominated by the SRH current from the source side. Furthermore, it is observed that the leakage current is insensitive to the gate voltage, which also suggests the leakage current is dominated by the source-side leakage.

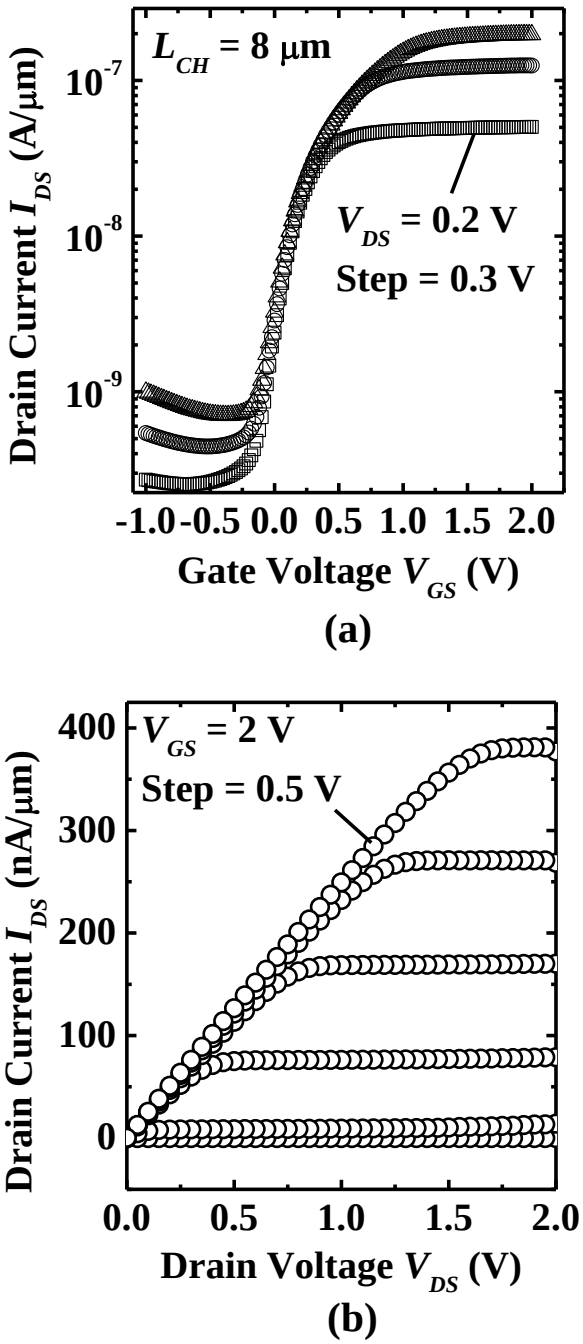


Fig. 4.16. I_{DS} - V_{GS} characteristics of a Ge-source $In_{0.53}Ga_{0.47}As$-channel TFET with L_{CH} of 8 μm. The $L_{OV,GS}$ and $L_{OV,GD}$ are 9 μm and 2 μm, respectively. The minimum point *S* is ~177 mV/decade. (b) I_{DS} - V_{DS} characteristics of the same device in (a). The device performance can be further improved by optimizing the Ge/$In_{0.53}Ga_{0.47}As$ tunneling junction.

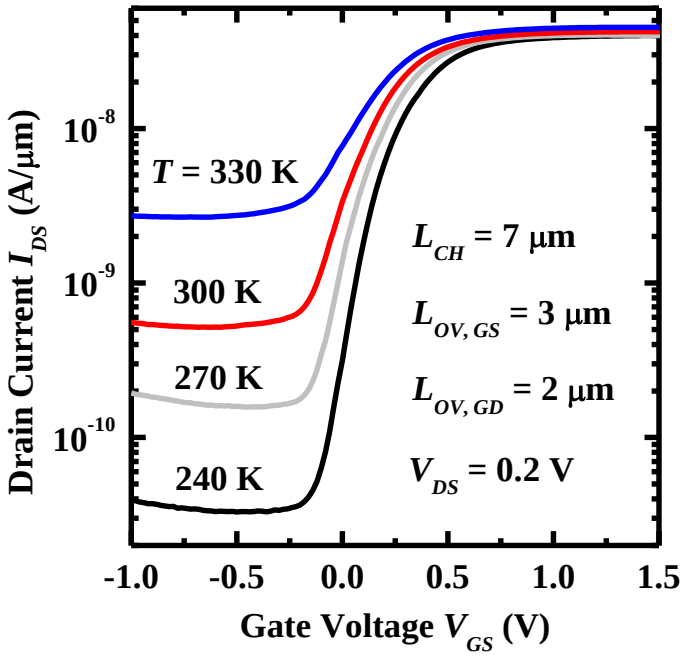


Fig. 4.17. I_{DS} - V_{GS} characteristics of a fabricated TFET under various temperatures ranging from 240 to 330 K in steps of 30 K.

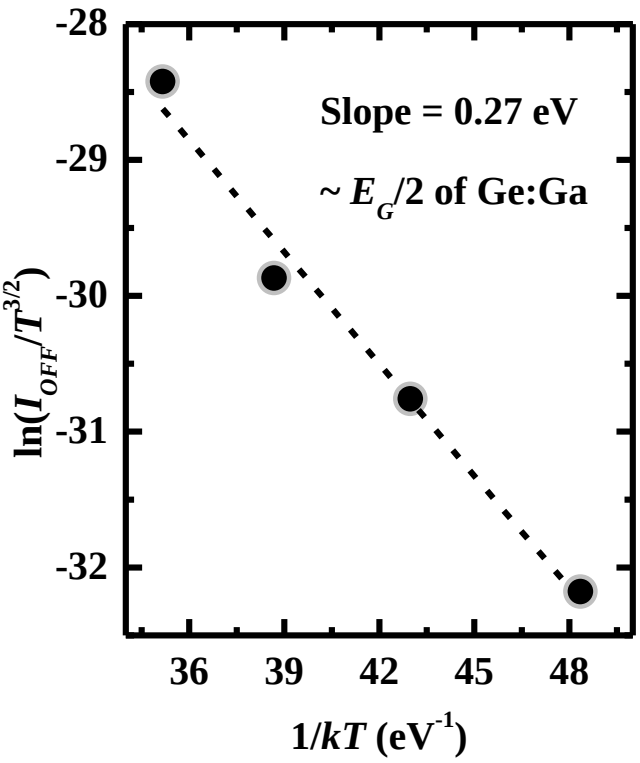


Fig. 4.18. Arrhenius plot of $\ln(I_{OFF}/T^{3/2})$ versus $1/kT$. The slope of the fitted line is ~0.27 eV, which corresponds to the half bandgap of Ge, indicating the off-state leakage current floor is dominated by the SRH generation-recombination current in the source side.

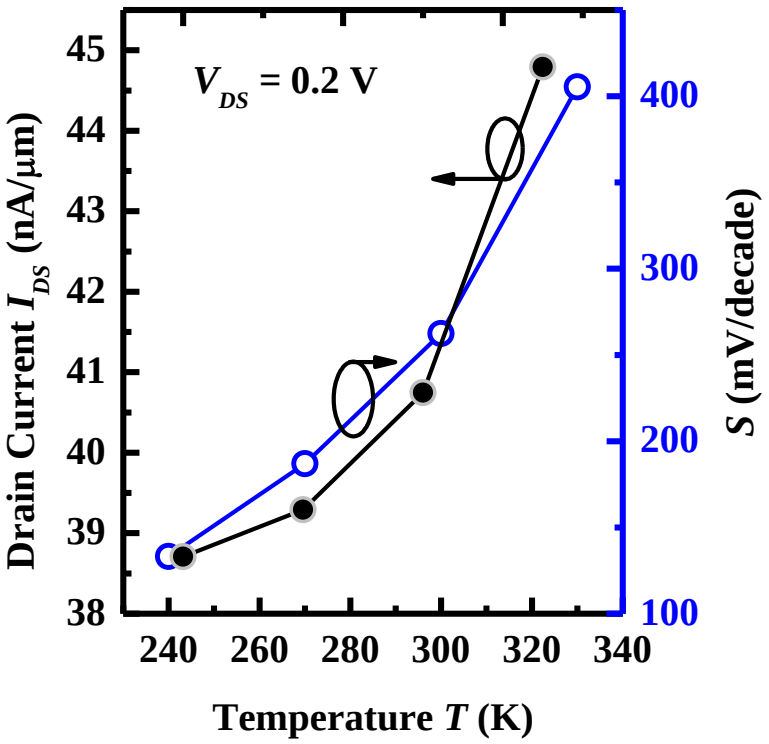


Fig. 4.19. Plot of I_{DS} and S as a function of temperature. The I_{DS} increases as temperature changes from 240 to 330 K, which is mainly due to the bandgap reduction. Due to the trap-assisted tunneling, S has a positive temperature dependence. The discrepancy of the S at room temperature between this transistor and the one in Fig. 4.16 is due to device-to-device variation.

Fig. 4.19 plots the I_{DS} at V_{GS} = 1.0 V and V_{DS} = 0.2 V as a function of temperature. The device is in the on-state under this bias condition and the I_{DS} is determined by the band-to-band tunneling current. In TFET, the G_{BTBT} is modeled using Kane's model [73]

$$G_{BTBT} = A\frac{\xi^2}{E_G^{1/2}}\exp\left(-B\frac{E_G^{1/2}}{\xi}\right), \tag{4.6}$$

where E_G is the energy bandgap of the material in the tunneling region and ξ is the magnitude of the electric field. Parameters A and B are dependent on the properties of the material used and are functions of carrier effective mass. As temperature

increases from 240 to 330 K, there is a monotonic increase in I_{ON}, which is mainly due to the reduction of the bandgap in both Ge and $In_{0.53}Ga_{0.47}As$ at the tunneling junction. From 240 to 330 K, the bandgap of both Ge and $In_{0.53}Ga_{0.47}As$ is reduced by ~33 meV. This amount of bandgap reduction causes the increase in the G_{BTBT}, leading to an increase in the I_{ON}.

The temperature dependence of the minimum point *S* characteristics is also depicted in Fig. 4.19. *S* increases from 133 mV/decade to 228 mV/decade when temperature increases from 240 to 300 K. The positive temperature dependence of *S* could be caused by the trap-assisted tunneling current [50],[58],[147]-[148]. As reported in Ref. [50], trap-assisted tunneling has a strong positive temperature dependence and causes degradation in *S*. The large lattice mismatch between Ge and $In_{0.53}Ga_{0.47}As$ gives rise to defects at the Ge/$In_{0.53}Ga_{0.47}As$ interface, leading to the formation of trap states in the bandgap. Electrons can tunnel from the Ge source region to the $In_{0.53}Ga_{0.47}As$ channel via these trap states, causing the degradation of the *S*. Interface trap states at Al_2O_3/Ge and Al_2O_3/$In_{0.53}Ga_{0.47}As$ interfaces in the tunneling junction region may also increase the *S* of the TFET due to trap-assisted tunneling. There is a sharp increase in *S* when temperature reaches 330 K, which is because *S* was calculated at a relatively large I_{DS} due to the high leakage floor.

Despite the various advantages of the Ge/$In_{0.53}Ga_{0.47}As$ heterostructure, the fabricated TFET suffers from low I_{ON} as compared to the reported InGaAs-based TFETs [47],[52]. Based on the reported contact resistance values of NiGe [149] and Ni-$In_{0.53}Ga_{0.47}As$ [150] formed under similar experimental conditions as this work, we estimated the total resistance in the source and drain regions to be ~140 Ω.

However, the total resistance between source and drain of the TFET in Fig. 4.16 is ~2 × 10^4 Ω, which was calculated using V_{DS}/I_{DS} at V_{DS} = 0.2 V and V_{GS} = 2 V. As discussed in Section 2.3 of Chapter 2, the resistance components between the source and drain terminals of a TFET are source resistance R_S, drain resistance R_D, tunneling junction resistance R_{Tunnel}, and channel resistance $R_{Channel}$. Since R_S and R_D are much lower than the total resistance of the TFET, we believe the low I_{ON} is mainly caused by the high R_{Tunnel} and $R_{Channel}$ of the transistor. The I_{ON} can be further improved. From the TEM image of the tunneling junction region in Fig. 4.10(c), the Ge/$In_{0.53}Ga_{0.47}As$ interface under the gate inclines to the source side, which is not favorable for achieving high I_{ON}. Both simulation and experiment have demonstrated that an extended source structure, i.e. the source/channel interface inclining to the channel, would lead to the establishment of more tunneling paths with shorter lengths, which increases the tunneling current and reduces *S* of the device [33],[66]. Therefore, the source geometry has to be improved to enhance the device performance. The poor I_{ON} and *S* could also be related to the poor interface between Al_2O_3 and $In_{0.53}Ga_{0.47}As$ channel. The trap states at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface can retard the Fermi-level movement of the channel modulated by V_{GS}, which effectively affects the *S* of the TFET. When the TFET is at the on-state, these interface trap states can cause high carrier scattering, leading to a degraded mobility and low I_{ON}. To improve the gate stack quality, Si passivation [131] or InP [151] capping can be employed, which can help to reduce interface trap density and improve the mobility and *S* of the TFET.

In addition, the Ge growth process can also be further improved to reduce the

defect density at the Ge/$In_{0.53}Ga_{0.47}As$ interface, which will suppress the current due to trap-assisted tunneling and contribute to a steeper *S*. The Ge growth conditions can be adjusted, such as reducing the growth temperature and the Ge layer thickness, to achieve a strained Ge layer with lower the defect density at the interface.

4.5 Summary

In this Chapter, high quality Ge grown on $In_{0.53}Ga_{0.47}As$ substrate by MOCVD was achieved. XPS analysis revealed that Ge/$In_{0.53}Ga_{0.47}As$ interface has a staggered band alignment and the energy of the valence band energy in Ge is higher than that in $In_{0.53}Ga_{0.47}As$ by 0.5 ± 0.1 eV. Such a staggered band alignment is useful for application in an n-channel TFET. An $In_{0.53}Ga_{0.47}As$-channel TFET with p^+ Ge-source was fabricated and characterized. Its electrical performance was investigated and the dominant conduction mechanisms in both on- and off-states were studied using multi-temperature measurement. The I_{ON} of the fabricated TFETs can be enhanced by improving the source/channel profile and reducing the interface trap density of the gate stack. In addition, the *S* can be further improved by using a strained Ge epitaxial layer with low defect density.

Chapter 5

Germanium-Tin ($Ge_{1-x}Sn_x$) MOSFETs with Low-Temperature Silicon Surface Passivation

5.1 Introduction

As discussed in Chapter 1, germanium-tin ($Ge_{1-x}Sn_x$) has attracted great interests as an alternative channel material as it has higher carrier mobilities than silicon (Si) and germanium (Ge) [81]-[82],[152]-[153]. Passivation of $Ge_{1-x}Sn_x$ surface and development of a high-quality and thermodynamically stable gate stack are important for realizing high performance $Ge_{1-x}Sn_x$ metal-oxide-semiconductor field-effect transistors (MOSFETs).

$Ge_{1-x}Sn_x$ p-channel MOSFETs (pMOSFETs) with low-temperature (~370℃) Si surface passivation have been demonstrated [82]-[84],[154]. The insertion of a thin Si layer between high-*k* gate dielectric and $Ge_{1-x}Sn_x$ can help to reduce the interface trap density D_{it} in the gate stack of $Ge_{1-x}Sn_x$ pMOSFETs. In addition, the large valence band offset ΔE_V between $Ge_{1-x}Sn_x$ and Si confines the inversion carriers (holes) in the $Ge_{1-x}Sn_x$ channel and contributes to reduced carrier scattering and higher hole mobility.

Si passivation technique has been investigated for Ge pMOSFETs [155]-[168]. It was reported that the interfacial Si layer thickness has significant impact on the

performance of Ge pMOSFETs [164]-[165]. It was found that the hole mobility and drive current of the transistors increase as the thickness of the Si passivation layer is increased from 3 to 8 monolayers (ML). However, when the Si layer is thicker than its critical thickness, crystalline defects such as dislocations or stacking faults can be introduced at the Si/Ge interface or in the Si layer due to the large lattice mismatch between Si and Ge [166]-[167]. Such defects are detrimental to the mobility of carriers. Similar to Ge pMOSFETs, it is worthwhile to study the impact of Si surface passivation layer thickness on the electrical performance of $Ge_{1-x}Sn_x$ pMOSFETs. This has not been reported before and is documented in Section 5.2. In addition, the effects of post metal annealing (PMA) on the electrical characteristics of Si passivated $Ge_{0.97}Sn_{0.03}$ pMOSFETs are also investigated. By performing PMA for $Ge_{0.97}Sn_{0.03}$ pMOSFETs, the interface trap density is reduced, leading to enhanced intrinsic transconductance $G_{m,int}$, smaller subthreshold swing S, and improved effective hole mobility μ_{eff} as compared to transistors without PMA.

Although $Ge_{1-x}Sn_x$ pMOSFETs with good drive current have been demonstrated, there are only few studies on $Ge_{1-x}Sn_x$ n-channel MOSFETs (nMOSFETs) to date [86]-[88]. Moreover, the drive currents of the reported $Ge_{1-x}Sn_x$ nMOSFETs are much lower than those of $Ge_{1-x}Sn_x$ pMOSFETs. Therefore, further improvement in the drive current of $Ge_{1-x}Sn_x$ nMOSFETs is required to enable the realization of complementary logic devices with $Ge_{1-x}Sn_x$ channel material. This requires the development of advanced surface passivation techniques to achieve high-quality gate stack with high electron mobility. Section 5.3 documents the first demonstration of $Ge_{0.976}Sn_{0.024}$ nMOSFETs with Si surface passivation. Si-passivated

devices achieve a higher drive current than those passivated by $GeSnO_2$ [86]. Moreover, the effects of forming gas annealing (FGA) on the electrical characteristics of $Ge_{0.976}Sn_{0.024}$ nMOSFETs are also investigated.

5.2 GeSn pMOSFETs with Si Surface Passivation

In this Section, the fabrication of $Ge_{0.97}Sn_{0.03}$ pMOSFETs with low-temperature Si surface passivation to investigate the impact of Si passivation layer thickness on the transistor electrical characteristics is documented. By increasing the thickness of Si passivation layer from 4 to 7 ML, μ_{eff} at an inversion carrier density N_{inv} of 1×10^{13} cm^{-2} was improved by ~19% ± 4%. This is attributed to reduced carrier scattering by charges found at the interface between the Si layer and the gate dielectric. In addition, the effects of PMA were also investigated. It was observed that the mid-gap interface trap density D_{it} was reduced in devices with PMA. $Ge_{0.97}Sn_{0.03}$ pMOSFETs with PMA have improved $G_{m,int}$, S, and μ_{eff} as compared to the control devices without PMA.

5.2.1 Fabrication of GeSn pMOSFETs

Fig. 5.1(a) shows the key processing steps for the fabrication of $Ge_{0.97}Sn_{0.03}$ pMOSFETs. 4-inch (100)-oriented n-type Ge (donor concentration N_D = ~1×10^{17} cm^{-3}) wafers were used as the starting substrates. After cyclic cleaning using dilute hydrofluoric acid (DHF) ($HF:H_2O$ = 1:50) and deionized water, the wafers were loaded into a molecular beam epitaxy (MBE) system for $Ge_{0.97}Sn_{0.03}$ growth at 180 ˚C.

The base pressure of the growth chamber was 3×10^{-8} Pa. 99.9999% pure Ge and 99.9999% pure tin (Sn) were used as Ge and Sn sources, respectively. The as-grown GeSn films were p-type with an unintentional doping concentration of $\sim 5 \times 10^{16}$ cm^{-3} as obtained by Hall measurement. A 20 nm thick high-quality strained $Ge_{0.97}Sn_{0.03}$ channel layer was grown. The film was fully strained and the substitutional Sn composition was determined to be 3% using high-resolution x-ray diffraction (XRD).

Phosphorus well implantation was carried out at an energy of 20 keV and a dose of 5×10^{12} cm^{-2}. Dopant activation was then performed at 450 ˚C for 3 minutes in nitrogen (N_2) ambient using rapid thermal annealing (RTA). The wafers were then treated in DHF ($HF:H_2O$ = 1:50) before being loaded into an ultra-high-vacuum chemical vapor deposition (UHVCVD) system for Si surface passivation. The UHVCVD system is equipped with a high-vacuum transfer module to prevent the formation of native oxide as illustrated in Fig. 5.2. Sulfur hexafluoride (SF_6) plasma treatment was performed in the first chamber of the UHVCVD system at ~320 ˚C for 50 s to remove any residual native oxide which may be formed before the samples were loaded. Next, Si surface passivation was performed in a second chamber at ~370 ˚C. Disilane (Si_2H_6) with a flow rate of 10 standard cubic centimeters per minute (sccm) was used as the precursor. A low process temperature used for Si surface passivation could help to reduce the likelihood of Ge incorporation/segregation in the Si passivation layer [155]-[156]. The thickness of the Si passivation layer was controlled by varying the Si_2H_6 treatment duration. In this experiment, the Si_2H_6 treatment durations used were 90 and 150 minutes for two experimental splits.

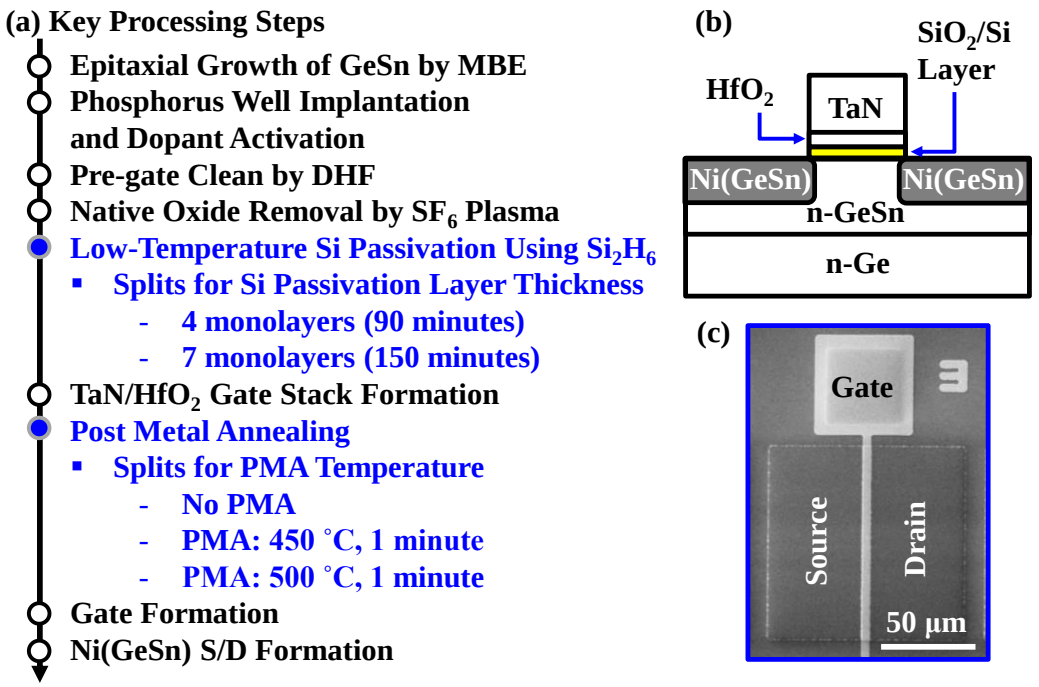


Fig. 5.1. (a) Key processing steps for the fabrication of a metallic S/D $Ge_{0.97}Sn_{0.03}$ pMOSFET with low-temperature Si passivation. (b) Schematic shows the cross-sectional view of a GeSn pMOSFET. (c) Top-view SEM image of a fabricated GeSn pMOSFET with Si surface passivation.

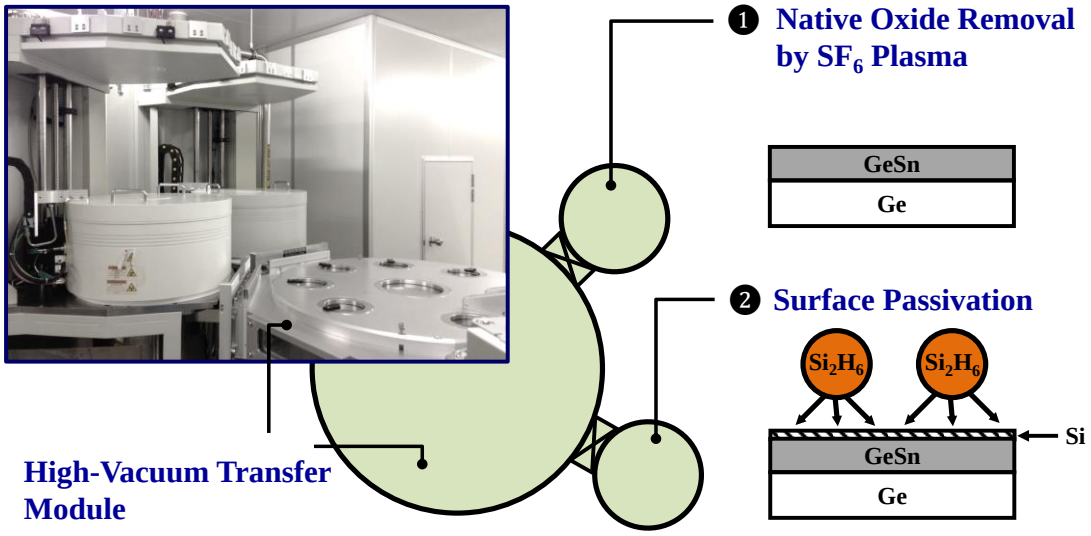


Fig. 5.2. Schematic illustration of an UHVCVD system for Si surface passivation. After pre-gate cleaning, wafers were quickly loaded into the UHVCVD system. In the first chamber, the wafers were cleaned in SF_6 plasma for native oxide removal and Si passivation was performed in the second chamber. The high vacuum transfer module serves to prevent native oxide formation during wafer transfer.

After Si passivation, gate stack comprising ~4.3 nm thick hafnium dioxide (HfO_2) by atomic layer deposition (ALD) and 120 nm thick tantalum nitride (TaN) by reactive sputtering was formed. PMA was then performed at 450 ˚C or 500 ˚C for 1 minute in N_2 ambient. For the control sample, PMA was not done. Gate lithography was carried out and TaN was patterned using chlorine (Cl_2)-based plasma to form the gate electrode. A 50 nm thick silicon dioxide (SiO_2) layer was sputtered and the active region was then exposed. After that, a 10 nm thick nickel (Ni) layer was sputtered and annealed at 350 ˚C for 30 s using RTA to form the self-aligned nickel stanogermanide [Ni(GeSn)] metallic source/drain (S/D). Concentrated sulfuric acid (H_2SO_4) (96%) was used to remove the unreacted Ni film to complete the device fabrication. The schematic in Fig. 5.1(b) illustrates the structure of a $Ge_{0.97}Sn_{0.03}$ pMOSFET with Si surface passivation. A top-view scanning electron microscope (SEM) image of a completed device is shown in Fig. 5.1(c).

5.2.2 Impact of Si Passivation Layer Thickness

High-resolution transmission electron microscope (TEM) images in Fig. 5.3 show the gate stack of the samples with 90 minutes and 150 minutes Si surface passivation. The thickness of the HfO_2 was ~4.3 nm as measured from the TEM images. An ultrathin layer of SiO_2 was formed due to the partial oxidation of the Si passivation layer [84].

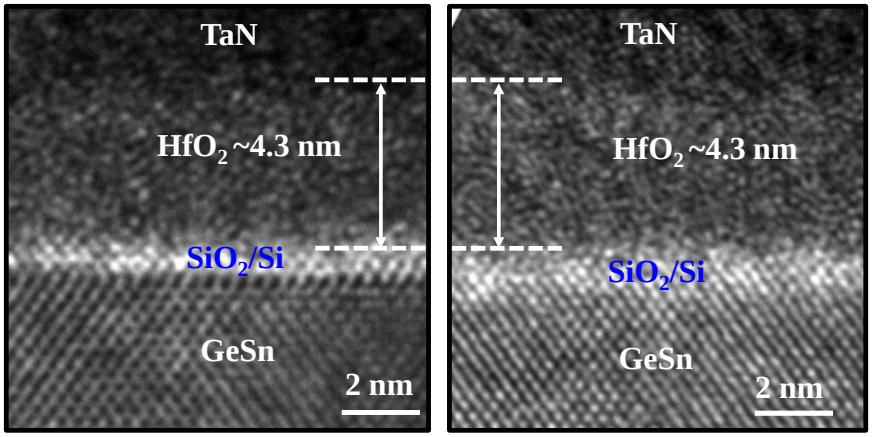


Fig. 5.3. High-resolution cross-sectional TEM images of TaN/HfO_2 stack formed on Si passivated $Ge_{0.97}Sn_{0.03}$ substrates with (a) 90 minutes and (b) 150 minutes Si passivation. An ultrathin SiO_2 was formed due to the partial oxidation of the Si passivation layer. The thickness of the HfO_2 is ~4.3 nm.

Fig. 5.4 shows the split capacitance-voltage (*C* - *V*) characteristics of the $Ge_{0.97}Sn_{0.03}$ pMOSFETs with different Si passivation layer thicknesses, in the inversion regime (where *C* was measured between gate and source/drain terminals) and in the accumulation regime (where *C* was measured between gate and body terminals). The energy band diagrams along the gate-to-channel direction of a $Ge_{0.97}Sn_{0.03}$ pMOSFET in the strong inversion and accumulation regimes are also shown in Fig. 5.4. The valence band offset ΔE_V between Si and $Ge_{0.97}Sn_{0.03}$ is estimated to be 0.59 eV [175], and this large ΔE_V forms an energy barrier for holes. As a result, holes are confined in $Ge_{0.97}Sn_{0.03}$ when the transistor is in the strong inversion regime. Under inversion bias, the total inversion capacitance comprises a series combination of capacitance components due to HfO_2 (C_{HfO_2}), SiO_2 (C_{SiO_2}), Si passivation layer (C_{Si}), and the capacitance in the hole inversion layer (C_{inv}). With a thicker Si passivation layer, the total inversion capacitance is lower. Under

accumulation bias, electrons appear in the Si passivation layer and/or the $Ge_{0.97}Sn_{0.03}$ layer due to the negligible conduction band offset ΔE_C between Si and $Ge_{0.97}Sn_{0.03}$; therefore, the total capacitance comprises a series combination of C_{HfO_2}, C_{SiO_2}, and the capacitance in the electron accumulation layer (C_{acc}), and is independent of the Si passivation layer thickness.

For Si-capped silicon-germanium (SiGe) or Ge channel pMOSFETs, analysis of the inversion and accumulation capacitances is usually done to extract the Si cap thickness [168],[176]-[177]. To extract the Si passivation layer thickness from the *C* - *V* curves, the equivalent oxide thickness (EOT) of the $HfO_2/SiO_2/Si$ gate stack has to be obtained. A quantum-mechanical *C* - *V* simulator was used to fit the measured *C* - *V* curves as shown in Fig. 5.4. In the simulator, the hole and electron distributions were calculated by solving the Schrödinger and Poisson equations self-consistently with the Fermi-Dirac distribution. From the simulated inversion *C* - *V* curves, the EOT of the $HfO_2/SiO_2/Si$ gate stack in the transistors with 150 minutes and 90 minutes Si passivation are extracted to be 1.49 nm and 1.36 nm, respectively. Similarly, the EOT of the gate dielectric (comprising only of HfO_2 and SiO_2) in these two splits is determined to be 1.23 nm from the simulated accumulation *C* - *V* curve. Since the EOT of HfO_2 is 0.86 nm, the thickness of the SiO_2 layer can be estimated to be 0.37 nm (this was formed from 0.16 nm of Si).

As discussed above, the un-oxidized Si layer only contributes to a reduction in the inversion capacitance but not the accumulation capacitance. Thus, the thickness of the un-oxidized Si layer can be obtained from the difference in EOT of the gate stack under inversion and accumulation biases. For the device with 150 minutes Si

passivation, the thickness of the un-oxidized Si is 0.78 nm. Therefore, the as-grown Si layer thickness for 150 minutes Si passivation is 0.94 nm or 7 ML. Using the same method, the total Si layer thickness for the 90 minutes Si passivation can be estimated to be 4 ML. Table 4.1 summarizes the values of the extracted parameters. Fig. 5.5

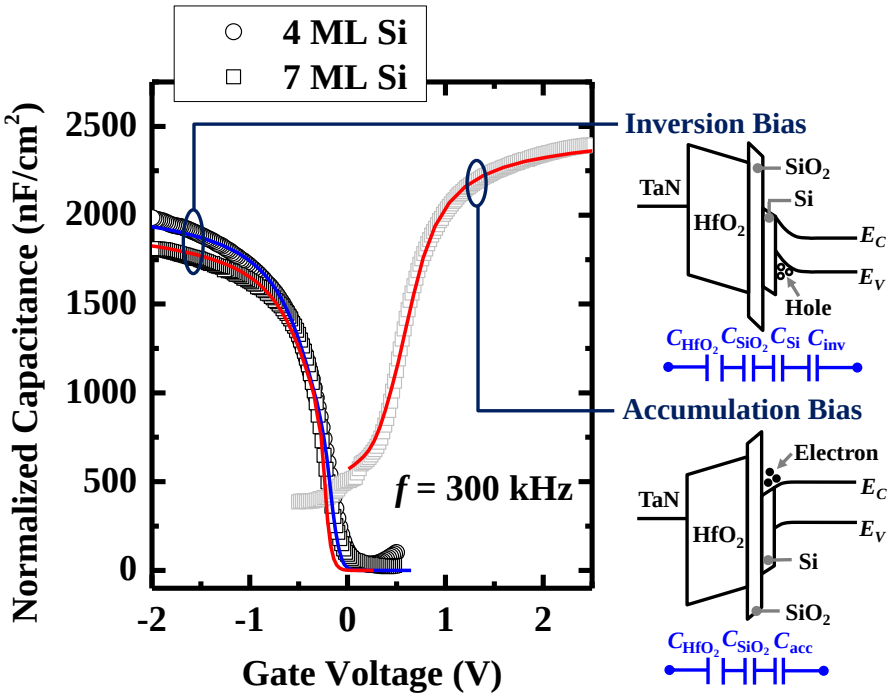


Fig. 5.4. (a) Split *C* - *V* characteristics of the $Ge_{0.97}Sn_{0.03}$ pMOSFETs with 4 and 7 ML Si surface passivation layer. Characterization frequency *f* was 300 kHz. Measured data points are plotted as symbols. The solid curves were obtained using a quantum-mechanical *C* - *V* simulator. The energy band diagrams along gate-to-channel direction of a $Ge_{0.97}Sn_{0.03}$ pMOSFET in the strong inversion and accumulation regimes are shown. E_C and E_V in the energy band diagrams are the conduction band edge and valence band edge, respectively.

Table 4.1. Extraction of the Si layer thicknesses for 90 and 150 minutes Si passivation.

Passivation Time (minutes)	EOT of HfO_2+SiO_2+Si (nm)	EOT of HfO_2+SiO_2 (nm)	Thickness of SiO_2 (nm)	EOT of Un-oxidized Si (nm)	Oxidized Si Thickness (nm)	As-Grown Si Thickness (ML)
90	1.36	1.23	0.37	0.13	0.16	4
150	1.49	1.23	0.37	0.26	0.16	7

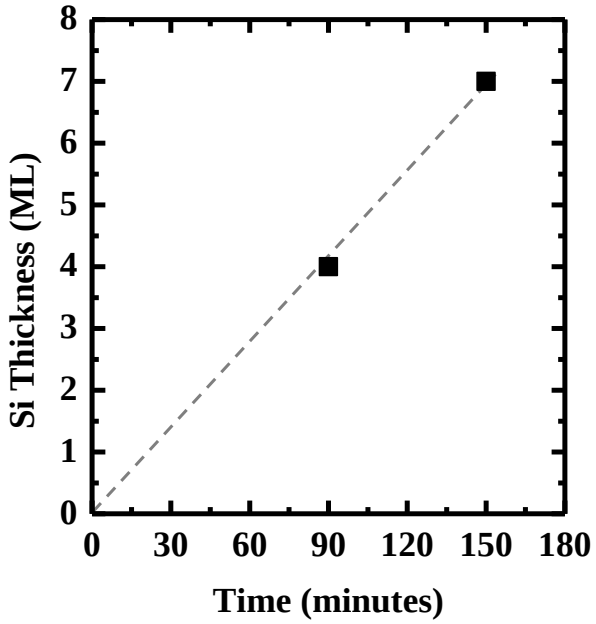


Fig. 5.5. Plot of the Si layer thickness as a function of passivation time, from which the growth rate of the Si layer is calculated to be 2.7 ML per hour.

plots the Si layer thickness versus growth time. The growth rate of the Si passivation layer is 2.7 ML per hour.

Fig. 5.6(a) plots the drain-to-source current - gate voltage (I_{DS} - V_{GS}) characteristics of $Ge_{0.97}Sn_{0.03}$ pMOSFETs with different Si passivation layer thicknesses at drain bias V_{DS} of - 0.1 V and - 0.5 V. The off-state leakage currents I_{OFF} of the two transistors are similar. In addition, it is observed that the threshold voltage V_{TH}, as determined by the maximum transconductance method, does not appreciably change with the Si passivation layer thickness, which agrees with the results for Ge pMOSFETs [178]. The I_{DS} - V_{DS} curves of the same pair of devices are shown in Fig. 5.6(b). The results indicate that drive current of the device with 7 ML Si passivation layer is 10% higher than that with 4 ML Si passivation layer at a gate overdrive ($V_{GS} - V_{TH}$) of - 2 V and V_{DS} of - 2 V. Fig. 5.6(c) shows the $G_{m,int}$ versus

V_{GS} at V_{DS} of - 0.1 V and - 0.5 V for the devices in Fig. 5.6(a). Device with 7 ML Si passivation layer exhibits significant improvement in $G_{m,int}$ as compared to that with 4 ML Si passivation layer. This improvement of $G_{m,int}$ with a larger Si layer thickness is indicative of hole mobility enhancement.

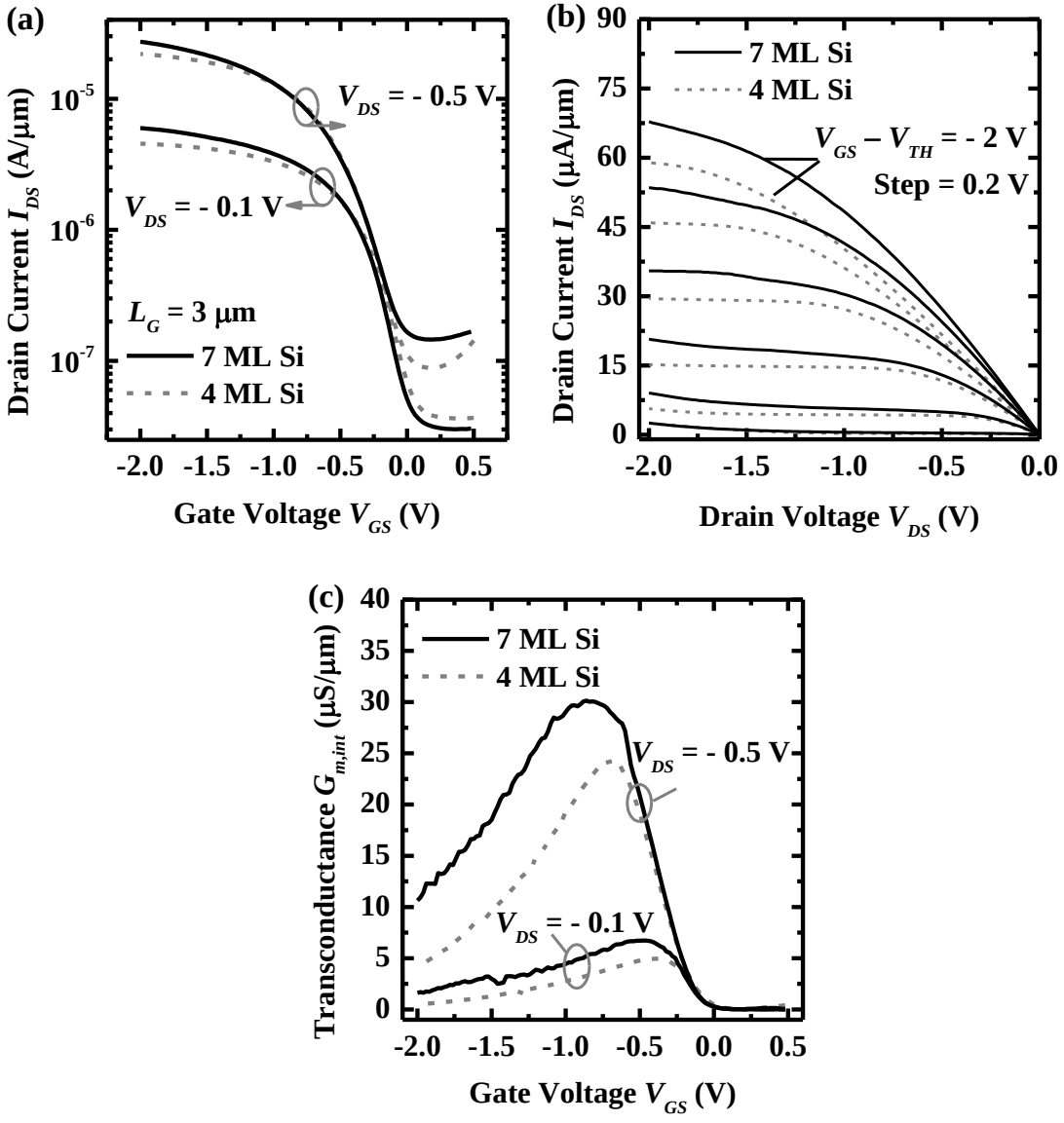


Fig. 5.6. (a) I_{DS} - V_{GS} transfer characteristics of a pair of $Ge_{0.97}Sn_{0.03}$ pMOSFETs with 4 and 7 ML Si passivation layer. (b) I_{DS} - V_{DS} characteristics of the same pair of devices in (a). Device with 7 ML Si passivation layer exhibit a 10% enhancement in I_{DS} at $V_{GS} - V_{TH} = V_{DS}$ = - 2 V as compared to that with 4 ML Si passivation layer. (c) $G_{m,int}$ versus V_{GS} at V_{DS} of - 0.1 V and - 0.5 V for the same device in (a). Device with 7 ML Si passivation layer exhibits a significant improvement in $G_{m,int}$ as compared to that with 4 ML Si passivation layer.

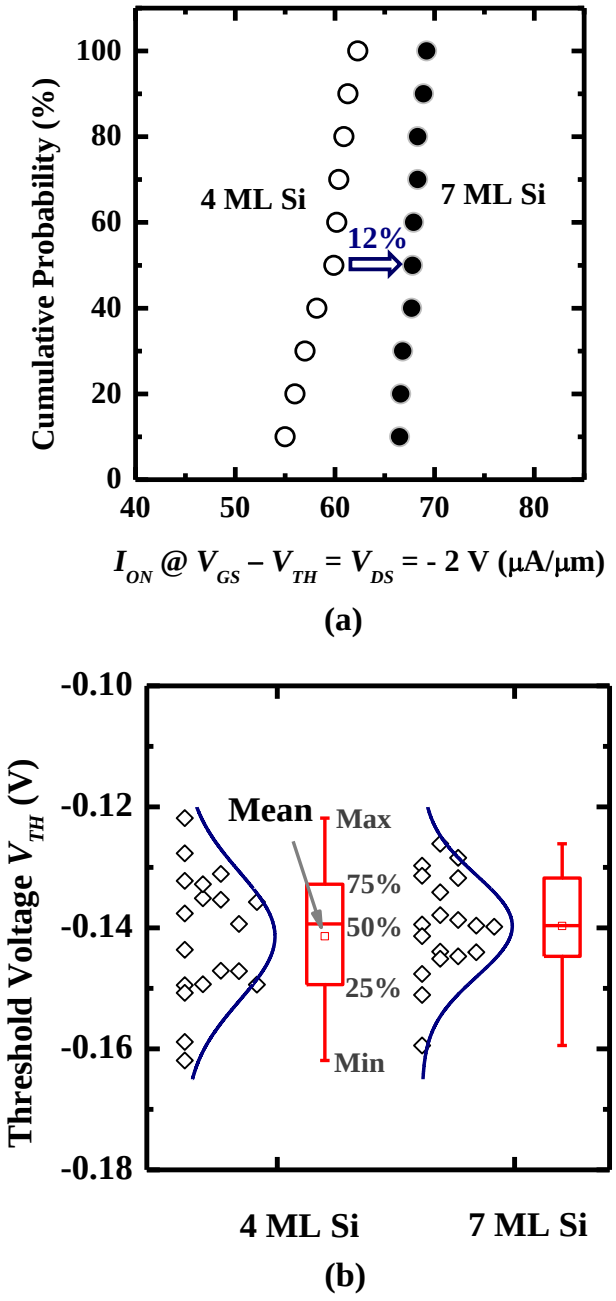


Fig. 5.7. (a) Statistical plots of I_{ON} for $Ge_{0.97}Sn_{0.03}$ pMOSFETs with different Si passivation layer thicknesses. I_{ON} is improved as the thickness of Si passivation layer increases from 4 to 7 ML. 10 devices were measured for each split. (b) V_{TH} does not change with the Si passivation layer thickness. This could possibly be explained by a higher density of negative charges in the gate stack for devices with 7 ML Si passivation layer.

Fig. 5.7(a) is a statistical plot of the on-state current I_{ON} for $Ge_{0.97}Sn_{0.03}$ pMOSFETs with different Si passivation layer thicknesses. I_{ON} was defined as I_{DS} at

V_{DS} of - 2.0 V and $V_{GS} - V_{TH}$ of - 2.0 V. All the transistors in this plot have gate length L_G of 3 μm and gate width W of 100 μm. Devices with 7 ML Si passivation layer exhibit 12% improvement in median I_{ON} as compared to those with 4 ML Si passivation layer, which is attributed to the improvement in hole mobility. Fig. 5.7(b) compares the V_{TH} for the two device splits, showing that V_{TH} is almost independent of the Si passivation layer thickness. A smaller gate capacitance in the inversion bias regime due to a thicker Si passivation layer is expected to shift the V_{TH} in the negative direction, but this was not observed. This could possibly be explained by a higher density of negative charges in the $HfO_2/SiO_2/Si$ gate stack for the device with a thicker Si passivation layer, as negative charges will shift V_{TH} in the positive direction. Ref. [178] also reported a similar observation and explanation for Ge pMOSFETs formed using a low-temperature trisilane (Si_3H_8) passivation process.

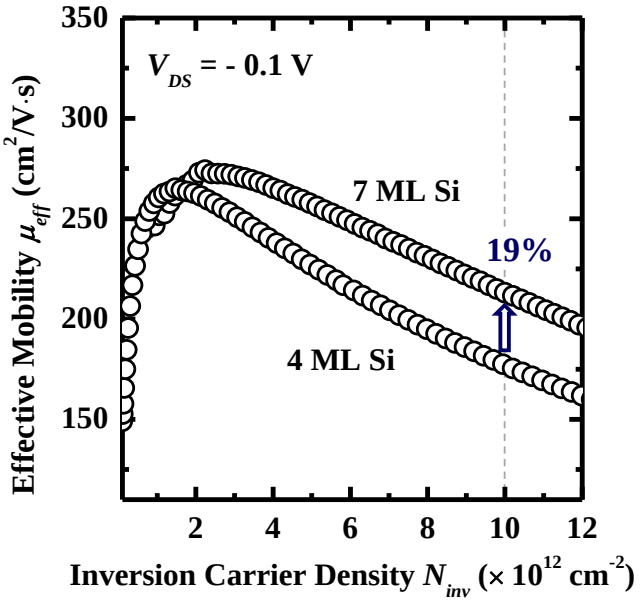


Fig. 5.8. Plot of μ_{eff} versus N_{inv} for $Ge_{0.97}Sn_{0.03}$ pMOSFETs. $Ge_{0.97}Sn_{0.03}$ pMOSFETs with 7 ML Si passivation layer achieve 19% ± 4% enhancement in μ_{eff} at N_{inv} of 1×10^{13} cm^{-2} as compared to devices with 4 ML Si passivation layer. The μ_{eff} was extracted using on a total resistance slope-based approach [179]. The mobility curves were extracted using a few pair of devices.

Fig. 5.8 compares the mobility of the transistors with different Si passivation layer thicknesses. The μ_{eff} was extracted using a total resistance slope-based approach [179]:

$$\mu_{eff} = \frac{1}{WqN_{inv}\frac{\Delta R_{total}}{\Delta L_G}}, \tag{5.1}$$

where N_{inv} is the inversion carrier density obtained from the inversion C - V measurement, q is the elementary charge, ΔR_{total} and ΔL_G are the differences in the total resistance and the L_G, respectively, of two $Ge_{0.97}Sn_{0.03}$ pMOSFETs used for mobility extraction. Fig. 5.8 shows that the μ_{eff} of the transistor with 7 ML Si passivation layer is 19% ± 4% higher than that with 4 ML Si passivation layer at N_{inv} of 1×10^{13} cm^{-2}.

Both physical surface roughness at the Si/GeSn interface and electrically active defects in the gate stack can affect μ_{eff} at high inversion carrier density. It is unlikely that the physical surface roughness at the 7 ML Si/GeSn interface is smaller than that at the 4 ML Si/GeSn interface. If μ_{eff} is limited by the surface roughness scattering, it is expected that the mobility values for the devices with 7 ML Si passivation layer will decrease rapidly with increasing N_{inv} and become closer to those for devices with 4 ML Si layer. However, this behavior is not observed in Fig. 5.8. Therefore, we believe the mobility enhancement is mainly due to reduced carrier scattering contributed by the electrically active defects in the gate stack. With 7 ML Si passivation layer, the interface state charges in the $HfO_2/SiO_2/Si$ stack are further away from the hole inversion layer in $Ge_{0.97}Sn_{0.03}$ as compared to the case with 4 ML Si passivation layer. The larger separation between interface states and inversion

carriers is expected to reduce remote Coulomb scattering in the channel and contribute to an enhanced hole mobility [165],[169].

5.2.3 Effects of Post Metal Annealing

The effects of PMA on the electrical characteristics of $Ge_{0.97}Sn_{0.03}$ pMOSFETs with 7 ML Si passivation layer were investigated. The 7 ML Si passivation layer was selected for further study as it led to a higher mobility and drive current performance as compared to the 4 ML Si passivation layer.

To investigate the change in the interfacial chemical bonding between high-*k* dielectric and $Ge_{0.97}Sn_{0.03}$ before and after PMA, a Si passivated blanket or un-patterned $Ge_{0.97}Sn_{0.03}$ sample with a thin ALD HfO_2 layer (~2 nm) was prepared for x-ray photoelectron spectroscopy (XPS). The measurement was performed using a VG ESCALAB 220i-XL imaging XPS. Monochromatic aluminum (Al) $K\alpha$ x-ray (1486.6 eV) was employed for analysis with photoelectron take-off angle of 90˚ with respect to the surface plane. Pass energy was set to be 20 eV. The binding energy scale was calibrated with pure Ni, gold (Au), silver (Ag), and copper (Cu) standard samples by setting the Ni Fermi edge, Au $4f_{7/2}$, Ag $3d_{5/2}$, and Cu $2p_{3/2}$ peaks at binding energies of 0.00 ± 0.02, 83.96 ± 0.02, 368.21 ± 0.02, and 932.62 ± 0.02 eV, respectively.

The Ge $2p_{3/2}$ and Sn $3d_{5/2}$ core level spectra for the $HfO_2/SiO_2/Si/Ge_{0.97}Sn_{0.03}$ sample before anneal are shown in Fig. 5.9(a) and (b), which provide clear evidence that Si surface passivation eliminates the formation of Ge-O and Sn-O bonds, indicating that the Si passivation layer is effective in preventing the oxidation of the

underlying $Ge_{0.97}Sn_{0.03}$ surface. Both Si-O and Si-Si bonds were observed from the Si 2*p* spectrum [Fig. 5.9(c)], showing that the Si layer was partially oxidized before or during HfO_2 deposition.

The same sample was annealed at 450 ˚C for 1 minute in N_2 ambient, and XPS analysis was performed again. No Ge-O and Sn-O bonds were observed in the sample after anneal, indicating the good thermal stability of the $HfO_2/SiO_2/Si/GeSn$ stack. In addition, the thicknesses of the SiO_2 and Si layer did not change after 450 ˚C annealing as the ratio of the area under SiO_2 peak to that under Si peak remained almost constant before and after anneal. This is further confirmed by using inversion *C* - *V* measurement (Fig. 5.10), which shows that the gate capacitance of the transistor with 450 ˚C PMA in the inversion regime is similar to that of the transistor without PMA. Negligible change in gate capacitance is also observed in the transistor with 500 ˚C PMA.

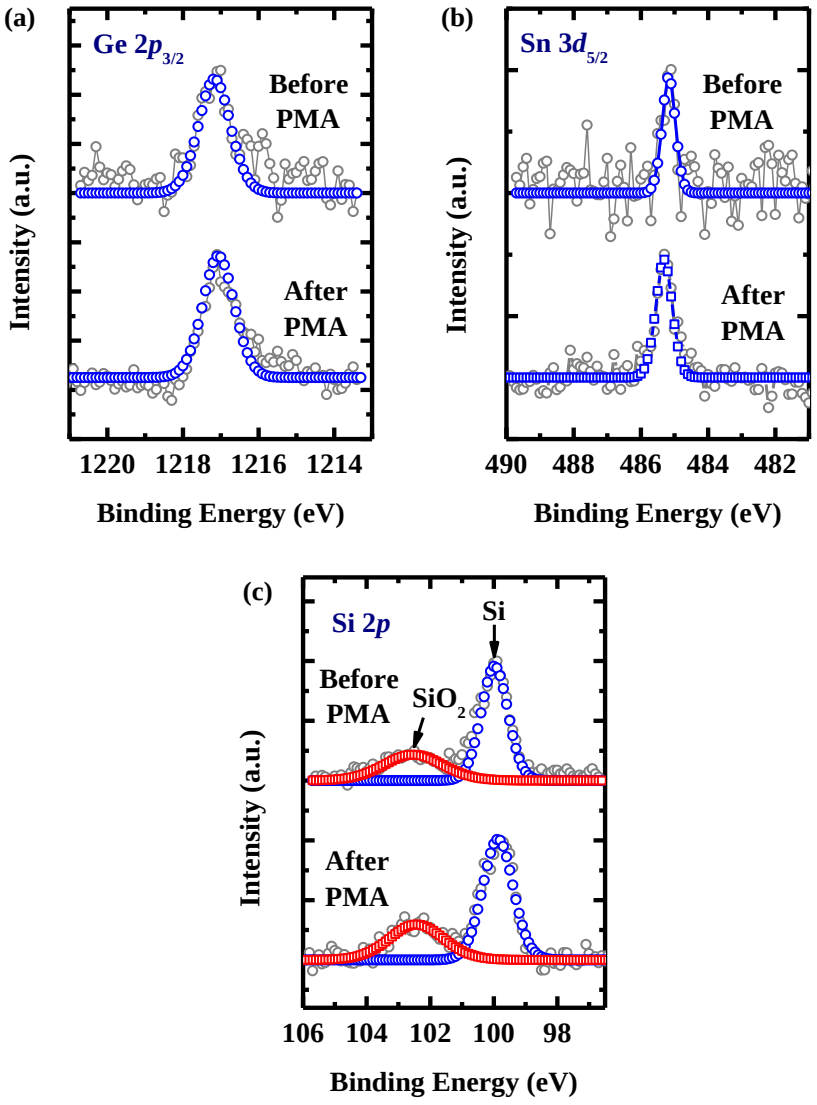


Fig. 5.9. High-resolution XPS spectra reveal the bonding structure at the $HfO_2/SiO_2/Si/GeSn$ interfaces. The grey circles show the raw data and the blue and red symbols are obtained by curve fitting. Ge $2p_{3/2}$ spectra in (a) and Sn $3d_{5/2}$ spectra in (b) show the suppression of Ge-O and Sn-O bonds, contributing to the improved interfacial quality. (c) The existence of both Si-Si and Si-O bonds indicates the Si passivation layer was partially oxidized.

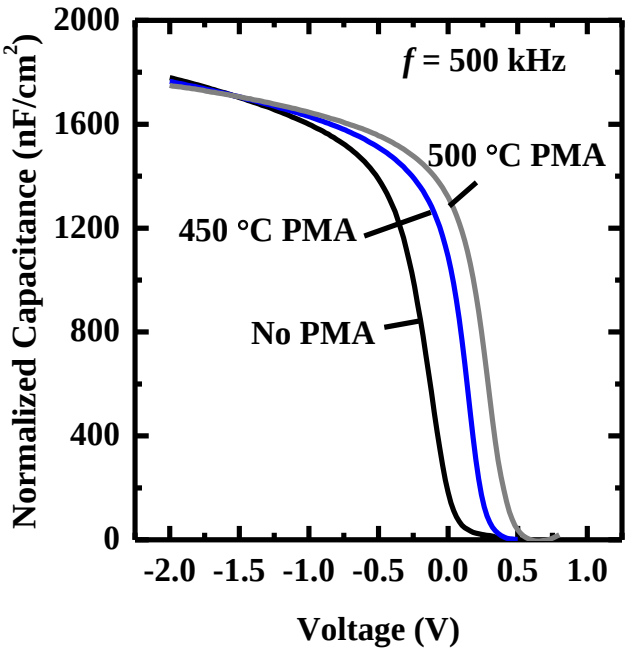


Fig. 5.10. Comparison of inversion *C* - *V* curves among the $Ge_{0.97}Sn_{0.03}$ pMOSFETs with and without PMA. Negligible differences in the gate capacitance in the inversion regime are observed.

Fig. 5.11 shows the I_{DS} - V_{GS} transfer characteristics of the Si passivated $Ge_{0.97}Sn_{0.03}$ pMOSFETs with no PMA, 450 ˚C PMA and 500 ˚C PMA. The L_G and W of these devices are 3 μm and 100 μm, respectively. The drive current of the device with 450 ˚C PMA is higher than that without PMA, and it is further improved by increasing the PMA temperature from 450 ˚C to 500 ˚C. It is also observed that PMA reduces S, and this is mainly attributed to a reduction of D_{it}. In addition, it is noted that V_{TH}, as determined by the maximum transconductance method, shifts towards positive direction for the devices with PMA. In the following paragraphs, the effects of PMA on $G_{m,int}$, S and V_{TH} will be discussed in detail.

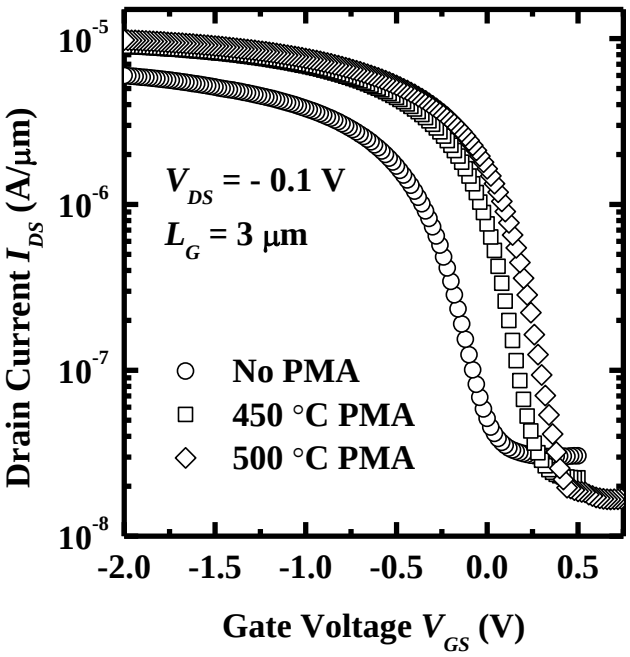


Fig. 5.11. I_{DS} - V_{GS} characteristics of the $Ge_{0.97}Sn_{0.03}$ pMOSFETs with no PMA, 450 ˚C PMA, and 500 ˚C PMA. The L_G and W of these devices are 3 μm and 100 μm, respectively. Both drive current and S are improved for devices with PMA. In addition, PMA causes V_{TH} to shift towards positive direction.

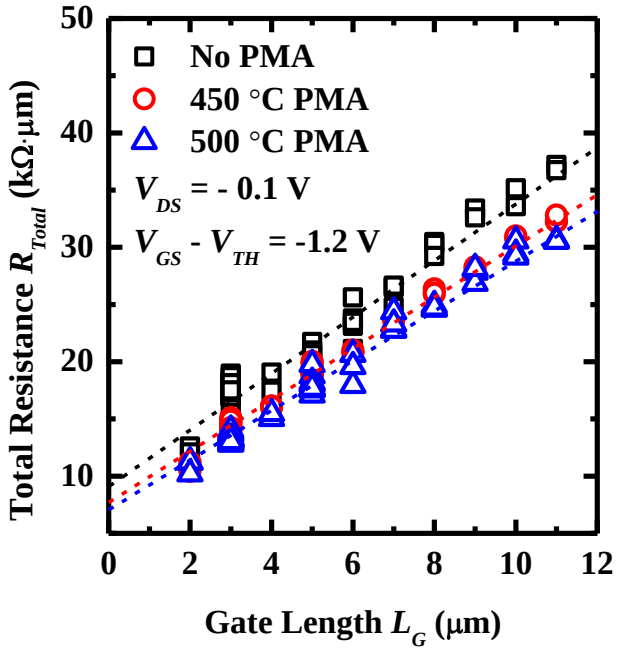


Fig. 5.12. R_{Total} as a function of L_G at $V_G - V_{TH}$ of - 1.2 V and V_{DS} of - 0.1 V. Experimental data points are plotted using symbols. Fitted lines are drawn using dashed lines. The slight difference in the S/D series resistance could be due to process variations.

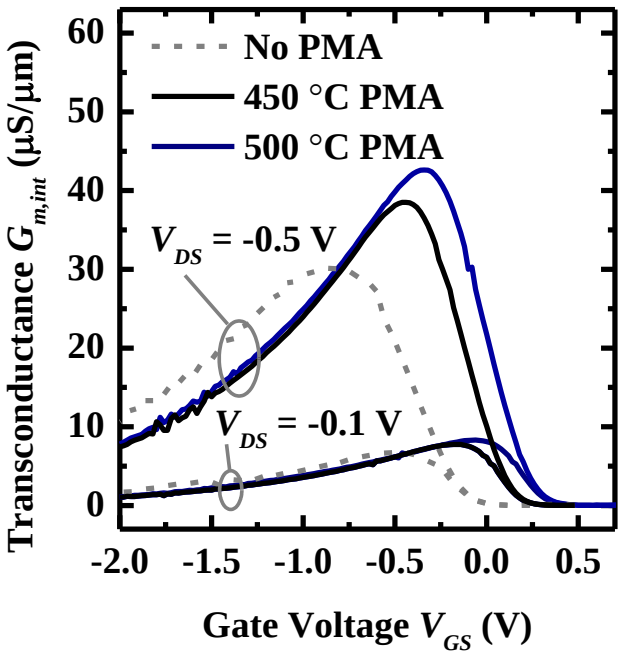


Fig. 5.13. $G_{m,int}$ for $Ge_{0.97}Sn_{0.03}$ pMOSFETs with no PMA, 450 ˚C PMA, and 500 ˚C PMA. Peak $G_{m,int}$ was enhanced for the devices with PMA, indicating the improvement of the gate stack quality.

The total resistance R_{Total} extracted at $V_{GS} - V_{TH}$ of - 1.2 V and V_{DS} of - 0.1 V as a function of L_G is shown in Fig. 5.12. The slight difference in the S/D series resistance R_{SD} could be due to process variations. To correct the effect of R_{SD}, $G_{m,int}$ at V_{DS} = - 0.1 V and - 0.5 V for $Ge_{0.97}Sn_{0.03}$ pMOSFETs with and without PMA was extracted (Fig. 5.13). A ~25% enhancement in the peak $G_{m,int}$ was observed for the devices with 450 ˚C PMA as compared to those without PMA at V_{DS} = - 0.5 V. By increasing the PMA temperature from 450 ˚C to 500 ˚C, the peak $G_{m,int}$ was further enhanced.

Fig. 5.14 shows the statistical plot of S for $Ge_{0.97}Sn_{0.03}$ pMOSFETs with and without PMA. The median S for the devices without PMA is 227 mV/decade, and it reduces to 158 mV/decade in the devices with 450 ˚C PMA. Median S further

improves to 148 mV/decade when the PMA temperature increases to 500 ˚C. The reduction in *S* indicates that the mid-gap D_{it} decreases due to PMA.

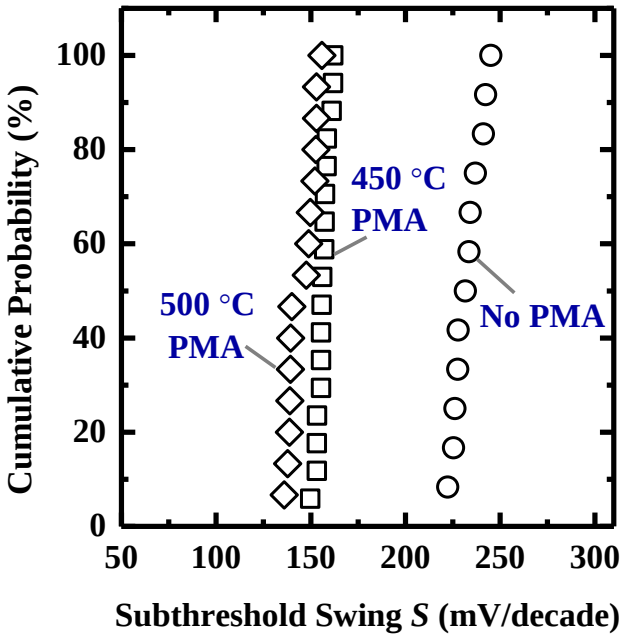


Fig. 5.14. Statistical plot of *S* for $Ge_{0.97}Sn_{0.03}$ pMOSFETs with and without PMA. The median *S* for the devices without PMA is 227 mV/decade. For the devices with 450 ˚C PMA, the median *S* reduces to 158 mV/decade and it further improves to 148 mV/decade when the PMA temperature increases to 500 ˚C. The reduction in *S* indicates that the mid-gap interface state density decreases due to PMA.

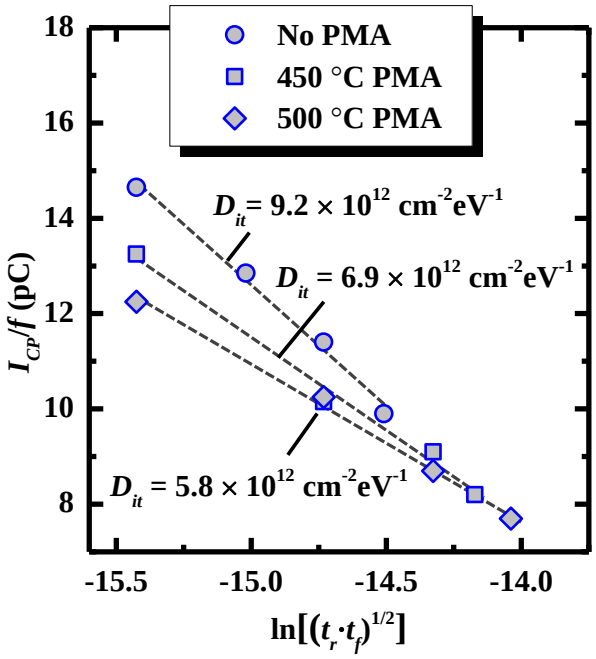


Fig. 5.15. I_{CP}/f as a function of $\ln[(t_r \cdot t_f)^{1/2}]$ provides the mean D_{it} of $Ge_{0.97}Sn_{0.03}$ pMOSFETs. A gentler slope in I_{CP}/f as a function of $\ln[(t_r \cdot t_f)^{1/2}]$ indicates a lower D_{it} level. The mean D_{it} of the sample without PMA is 9.2 × 10^{12} $cm^{-2} \cdot eV^{-1}$ and it reduces to 6.9 × 10^{12} $cm^{-2} \cdot eV^{-1}$ and 5.8 × 10^{12} $cm^{-2} \cdot eV^{-1}$ in the devices with 450 ˚C PMA and 500 ˚C PMA, respectively.

Charge pumping analysis was performed to evaluate the D_{it} in the $HfO_2/SiO_2/Si/GeSn$ stack using the method in Ref. [180]. The characterization was performed by sweeping the base level voltage V_{base} of constant-amplitude trapezoidal gate pulse train from accumulation level to inversion level, while keeping the S/D terminals grounded. The voltage amplitude V_a and frequency f of the gate pulses were 1 V and 200 kHz, respectively. Equal trapezoidal pulse with variable rise time (t_r) and fall time (t_f) ranging from 200 to 800 ns were applied. The charge pumping current (I_{CP}) for trapezoidal gate pulse waveform is expressed as

$$I_{CP} = 2qD_{it} f A_G kT \left[\ln \sqrt{t_r t_f} + \ln \left(\frac{|V_{FB} - V_{TH}|}{V_a} v_T n_s \sqrt{\sigma_n \sigma_p} \right) \right], \qquad (5.2)$$

where T is the temperature, A_G is the gate area of the transistor, k is Boltzmann constant, V_{FB} is the flatband voltage, V_{TH} is the threshold voltage, v_T is the thermal velocity of the carriers, n_s is the surface concentration of minority carriers, σ_n and σ_p are the capture cross sections of electrons and holes, respectively. Based on the above Equation, the mean D_{it} can be extracted from the slope of I_{CP}/f versus $\ln[(t_r \cdot t_f)^{1/2}]$ as shown in Fig. 5.15. The mid-gap D_{it} of the sample without PMA is 9.2 $\times 10^{12}$ $cm^{-2} \cdot eV^{-1}$. It reduces to 6.9 $\times 10^{12}$ $cm^{-2} \cdot eV^{-1}$ and 5.8 $\times 10^{12}$ $cm^{-2} \cdot eV^{-1}$ for the devices with 450 ˚C PMA and 500 ˚C PMA, respectively. It should be noted that the D_{it} measured is contributed by all the interface traps that are electrically active in the $HfO_2/SiO_2/Si/GeSn$ stack. Similar results of D_{it} reduction by PMA in N_2 ambient for Ge pMOSFETs has been reported in Refs. [161] and [181], which are consistent with our observations.

Fig. 5.16 is a statistical plot of V_{TH} for $Ge_{0.97}Sn_{0.03}$ pMOSFETs with L_G ranging from 3 μm to 10 μm. The V_{TH} of the devices with 450 ˚C PMA is 0.1 V, which is higher than that of the devices without PMA. It further increases to 0.2 V for the devices with 500 ˚C PMA. The positive shift of threshold voltage could be due to the reduction in positive fixed oxide charges Q_f in HfO_2 layer caused by the oxygen vacancies [183]. The reduction in Q_f is possibly attributed to the passivation of oxygen vacancies by N_2 during annealing. This threshold voltage shift is not likely to be caused by a change in the work function of TaN gate as it was reported that work function of TaN remains almost constant for processing temperatures below 700 ˚C [184].

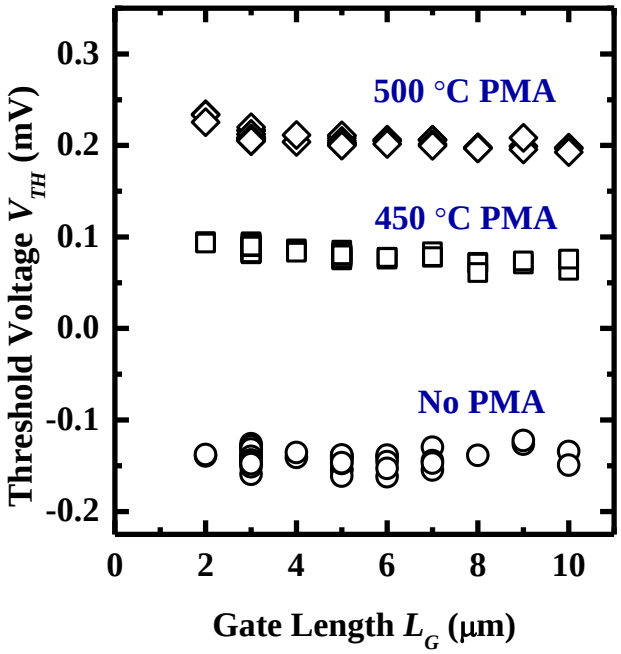


Fig. 5.16. Statistical plot of V_{TH} shows the effects of PMA for $Ge_{0.97}Sn_{0.03}$ pMOSFETs with L_G ranging from 3 μm to 10 μm. The positive shift in V_{TH} is possibly attributed to the reduction of Q_f in HfO_2.

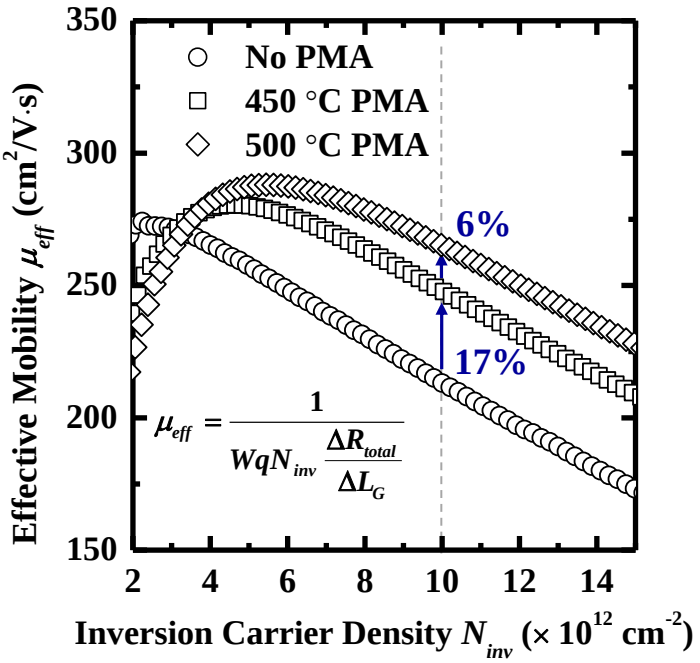


Fig. 5.17. Plot of μ_{eff} versus N_{inv}, showing that PMA enhances the hole mobility for $Ge_{0.97}Sn_{0.03}$ pMOSFETs.

Fig. 5.17 compares the extracted μ_{eff} versus N_{inv}, showing that mobility is enhanced in devices with PMA. Comparing the devices with and without PMA, it was observed that μ_{eff} at N_{inv} of 1×10^{13} cm^{-2} was improved by 17% ± 4% for the device with PMA at 450 ˚C. The μ_{eff} of device with 500 ˚C PMA was further improved by 6% ± 3% as compared to that with 450 ˚C PMA. The enhancement in mobility is mainly attributed to the reduction of D_{it}. With a lower interface charge density, the Coulomb scattering of holes is reduced, leading to an improvement of carrier mobility.

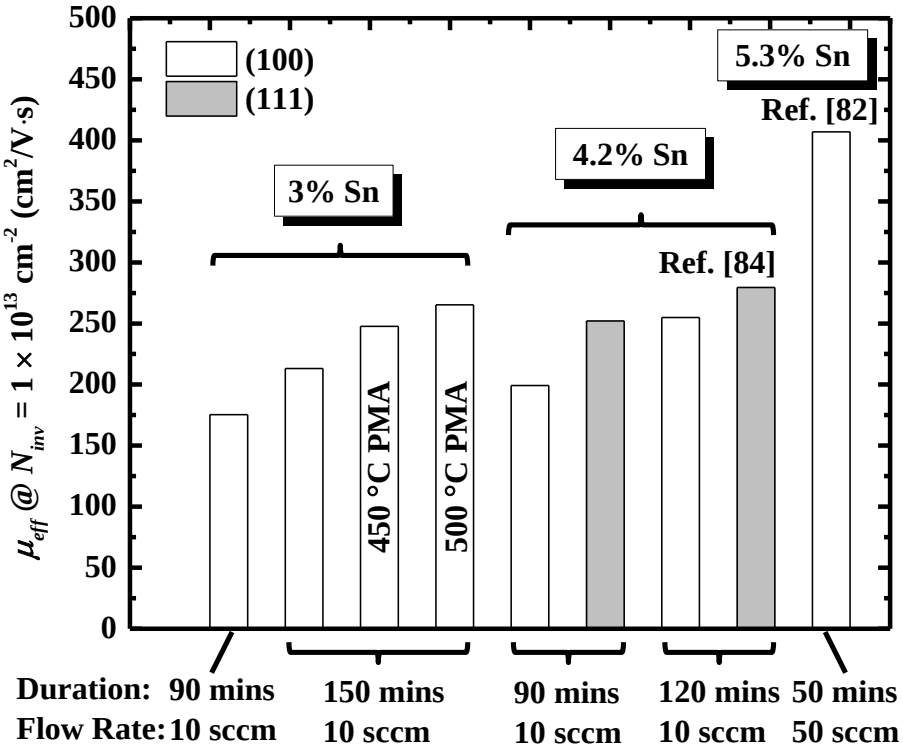


Fig. 5.18. Summary of the hole mobilities extracted at N_{inv} of 1×10^{13} cm^{-2} for Si passivated $Ge_{1-x}Sn_x$ pMOSFETs with different Sn compositions. The conditions for Si passivation (Si_2H_6 flow rates and durations) are shown. The chamber pressure was 5×10^{-7} Torr during processing. In general, the hole mobility increases with increasing Sn composition in the GeSn channel. PMA was not performed for the pMOSFETs in Refs. [82] and [84].

Fig. 5.18 summarizes the hole mobilities of Si passivated $Ge_{1-x}Sn_x$ pMOSFETs with different Sn compositions at N_{inv} of 1×10^{13} cm^{-2}. The hole mobilities of the $Ge_{0.97}Sn_{0.03}$ pMOSFETs in this work follow the trend that hole mobility improves as Sn composition increases. In addition, the benefit of PMA is also observed.

5.3 GeSn nMOSFETs with Si Surface Passivation

In this Section, the results of $Ge_{0.976}Sn_{0.024}$ nMOSFETs with low-temperature (~370 ˚C) Si surface passivation are documented. This was the first time that Si passivation was employed for GeSn nMOSFET fabrication. With Si passivation, a higher drive current was achieved as compared to devices with $GeSnO_2$ passivation [86]. In addition, the effects of FGA on the electrical characteristics of $Ge_{0.976}Sn_{0.024}$ nMOSFETs were investigated. It was found that FGA improves the gate stack quality due to the passivation of interfacial dangling bonds and bulk traps in HfO_2 by hydrogen, leading to an improvement in *S*.

5.3.1 Fabrication of GeSn nMOSFETs

Fig. 5.19(a) shows the key processing steps for the fabrication of $Ge_{0.976}Sn_{0.024}$ nMOSFETs. A gate-last process was used. P-type Ga-doped (100)-oriented Ge wafers with a doping concentration of 5×10^{17} cm^{-3} were used as the starting substrate. A $Ge_{0.976}Sn_{0.024}$ film with a thickness of 170 nm was epitaxially grown using a solid source MBE system at 180 ˚C. This film was fully strained and the substitutional Sn composition was 2.4% (0.35% lattice mismatch with Ge) as determined from high-resolution XRD. The root mean square (RMS) surface roughness of the $Ge_{0.976}Sn_{0.024}$ film for a 10 μm × 10 μm area is 0.37 nm as shown by the atomic force microscopy (AFM) image in Fig. 5.20. Fig. 5.21(a) shows the cross-sectional TEM image of the $Ge_{0.976}Sn_{0.024}$ on Ge substrate. High-resolution TEM image in Fig. 5.21(b) shows the high crystalline quality of the $Ge_{0.976}Sn_{0.024}$ film and

defect-free $Ge_{0.976}Sn_{0.024}$/Ge interface. The as-grown $Ge_{0.976}Sn_{0.024}$ film is p-type with an unintentional doping concentration of ~5 × 10^{16} cm^{-3} as obtained by Hall measurement.

The $Ge_{0.976}Sn_{0.024}$ nMOSFETs fabrication started with alignment mark patterning, after which photolithography was done to expose the S/D regions. Phosphorus was implanted into the S/D regions with a dose of 2 × 10^{15} cm^{-2} and an energy of 20 keV using photoresist as the mask. After photoresist removal, a 50 nm thick SiO_2 capping layer was deposited by sputtering. Activation anneal was then performed at 400 ˚C for 5 minutes in N_2 ambient using a RTA tool. Pre-gate clean using cyclic DHF ($HF:H_2O$ = 1:50) was performed before the wafers were loaded into the UHVCVD system for Si surface passivation. The Si passivation process was the same as the one described in Section 5.2.1. This was followed by the deposition of 5.4 nm thick HfO_2 by ALD and 100 nm thick TaN by sputtering. The TaN gate was then patterned using a Cl_2-based plasma etching. Finally, the S/D regions were opened and metal contacts were formed by evaporating 100 nm thick aluminum (Al) using a lift-off process. Fig. 5.19(b) shows the schematic of a GeSn nMOSFET with Si passivation. A top-view SEM image of a completed device is shown in Fig. 5.19(c).

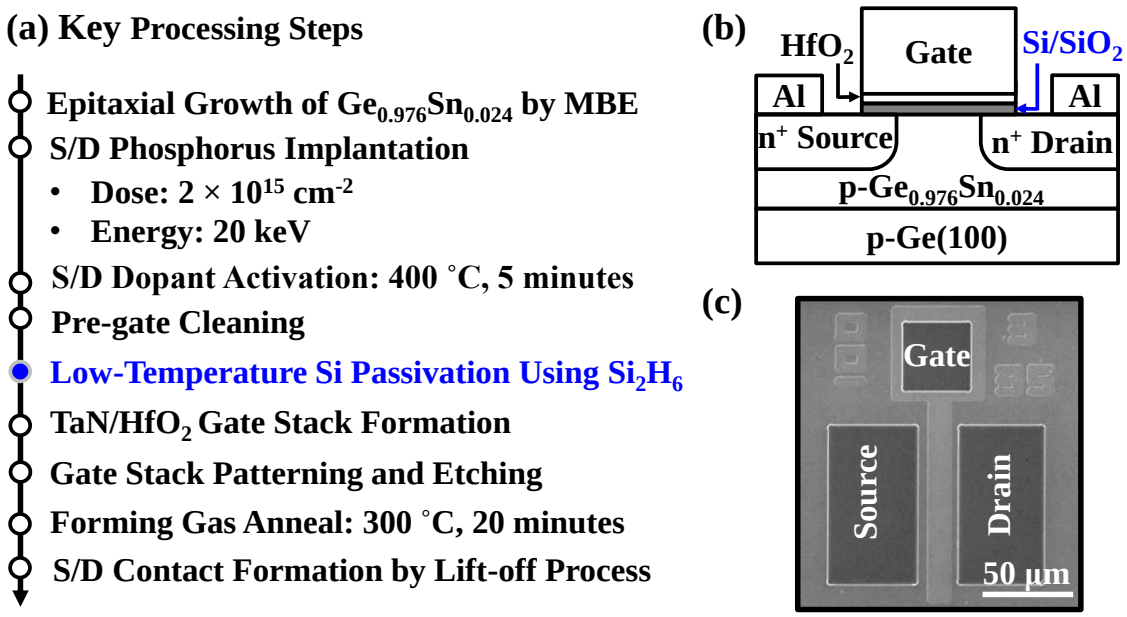


Fig. 5.19. (a) Key processing steps for the fabrication of $Ge_{0.976}Sn_{0.024}$ nMOSFETs. A gate-last process was used. (b) Schematic of a GeSn nMOSFET with Si passivation. (c) Top-view SEM image of a completed device.

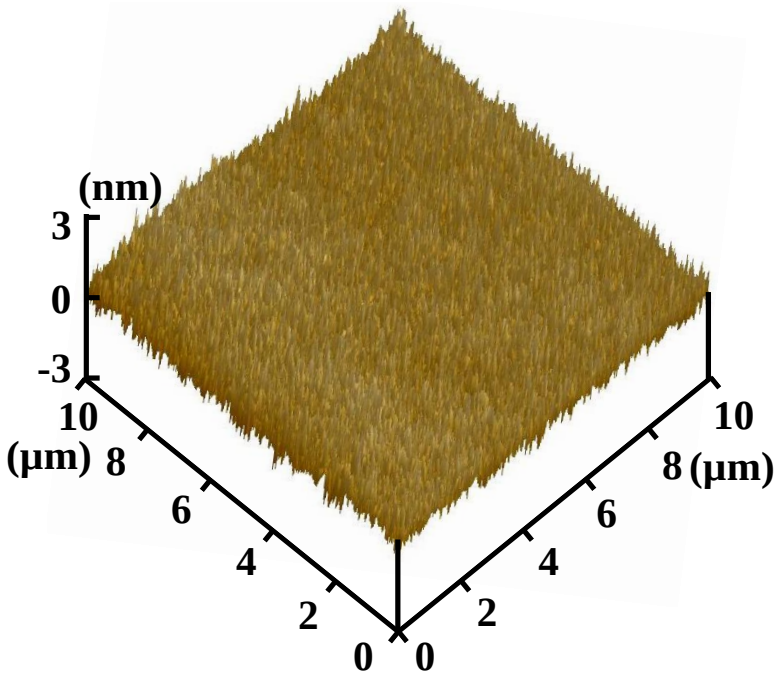


Fig. 5.20. AFM image shows that the RMS surface roughness of the $Ge_{0.976}Sn_{0.024}$ film is 0.37 nm over a 10 µm × 10 µm scanning area.

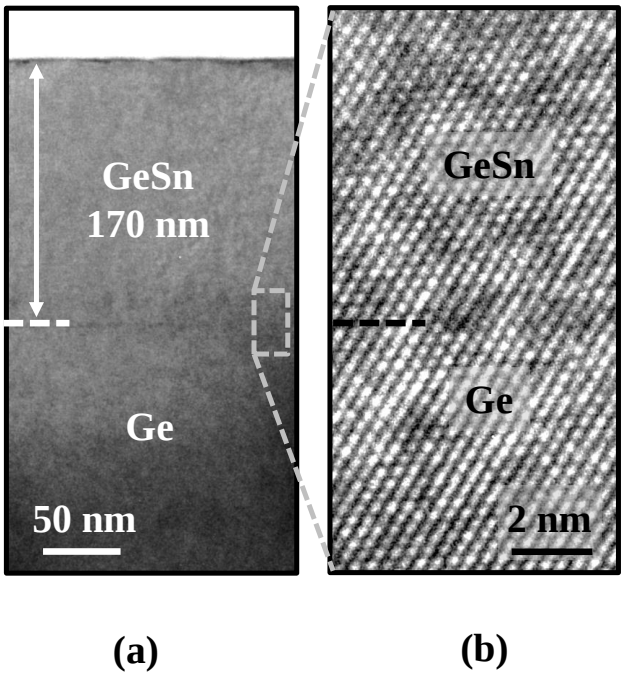


Fig. 5.21. (a) The cross-sectional TEM image of the epitaxial $Ge_{0.976}Sn_{0.024}$ film grown on Ge substrate. The thickness of the $Ge_{0.976}Sn_{0.024}$ film is 170 nm. (b) High-resolution TEM image depicts the high crystalline quality of the GeSn film and defect-free $Ge_{0.976}Sn_{0.024}$/Ge interface.

5.3.2 Electrical Characterization of GeSn nMOSFETs

XPS analysis was performed to examine the interfacial chemical bonding between high-*k* gate dielectric and $Ge_{0.976}Sn_{0.024}$. A Si-passivated p-type $Ge_{0.976}Sn_{0.024}$ sample with 2 nm thick ALD HfO_2 layer was prepared and a $Ge_{0.976}Sn_{0.024}$ sample without Si passivation was also included as a reference. Fig. 5.22 shows the Ge $2p_{3/2}$ and Sn $3d_{5/2}$ core level spectra. No Ge-O bonds are observed from the Ge $2p_{3/2}$ spectrum of the Si passivated sample, which provides clear evidence that Si passivation suppresses the formation of Ge-O bonds. However, no Sn-O peak is observed from the Sn $3d_{5/2}$ spectra for GeSn samples with and without Si passivation. This could be because the concentration of Sn-O bonds is too low to be detected by the XPS system.

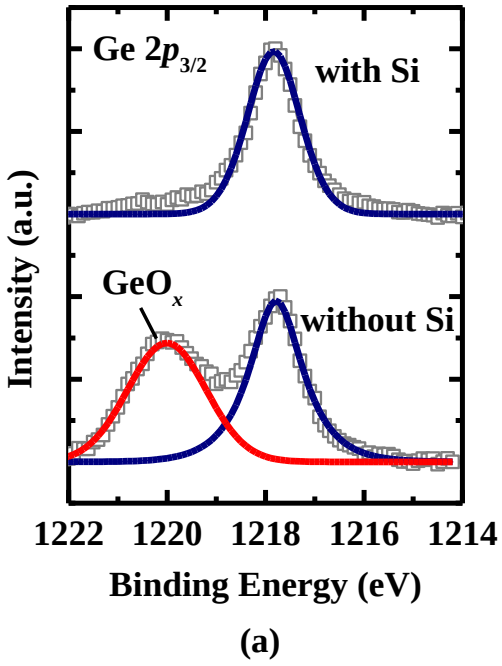


Fig. 5.22. (a) Ge $2p_{3/2}$ and (b) Sn $3d_{5/2}$ spectra obtained from XPS to investigate the interfacial chemical bonding between high-*k* dielectric and $Ge_{0.976}Sn_{0.024}$. The open squares show the raw data and the solid lines are the fitting curves. Ge-O bonds are observed in the Ge $2p_{3/2}$ spectrum from the sample without Si passivation, whereas no Ge-O is observed in the sample with Si passivation. This provides clear evidence that Si passivation eliminates the formation of Ge-O bond. No Sn-O peak is observed from the Sn $3d_{5/2}$ spectra for $Ge_{0.976}Sn_{0.024}$ samples with and without Si passivation.

Fig. 5.23 shows the inversion *C* - *V* characteristics of a $Ge_{0.976}Sn_{0.024}$ nMOSFET. A large frequency dispersion is observed when the frequency *f* varies from 50 kHz to 500 kHz. This suggests that a high level of fast trap charges near the conduction band edge are present in the gate stack. The capacitance equivalent thickness (CET) of the device is estimated to be ~1.8 nm based on the inversion capacitance value measured at *f* of 100 kHz.

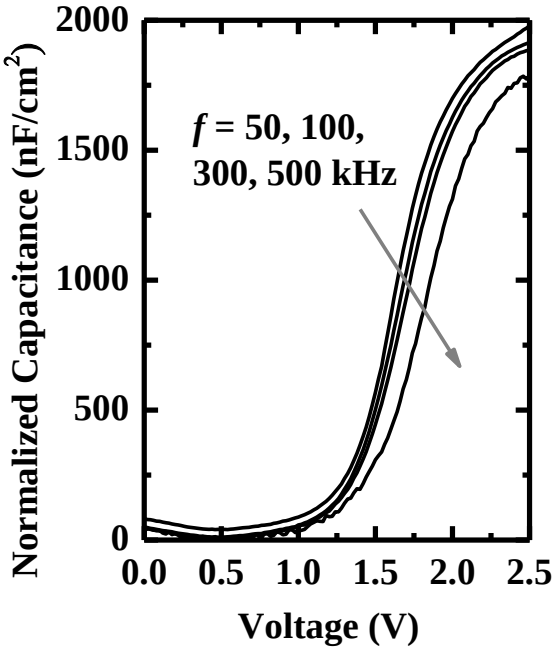


Fig. 5.23. Inversion *C* - *V* characteristics of a $Ge_{0.976}Sn_{0.024}$ nMOSFET. The large frequency dispersion indicates the existence of high density of fast trap charges in the gate stack.

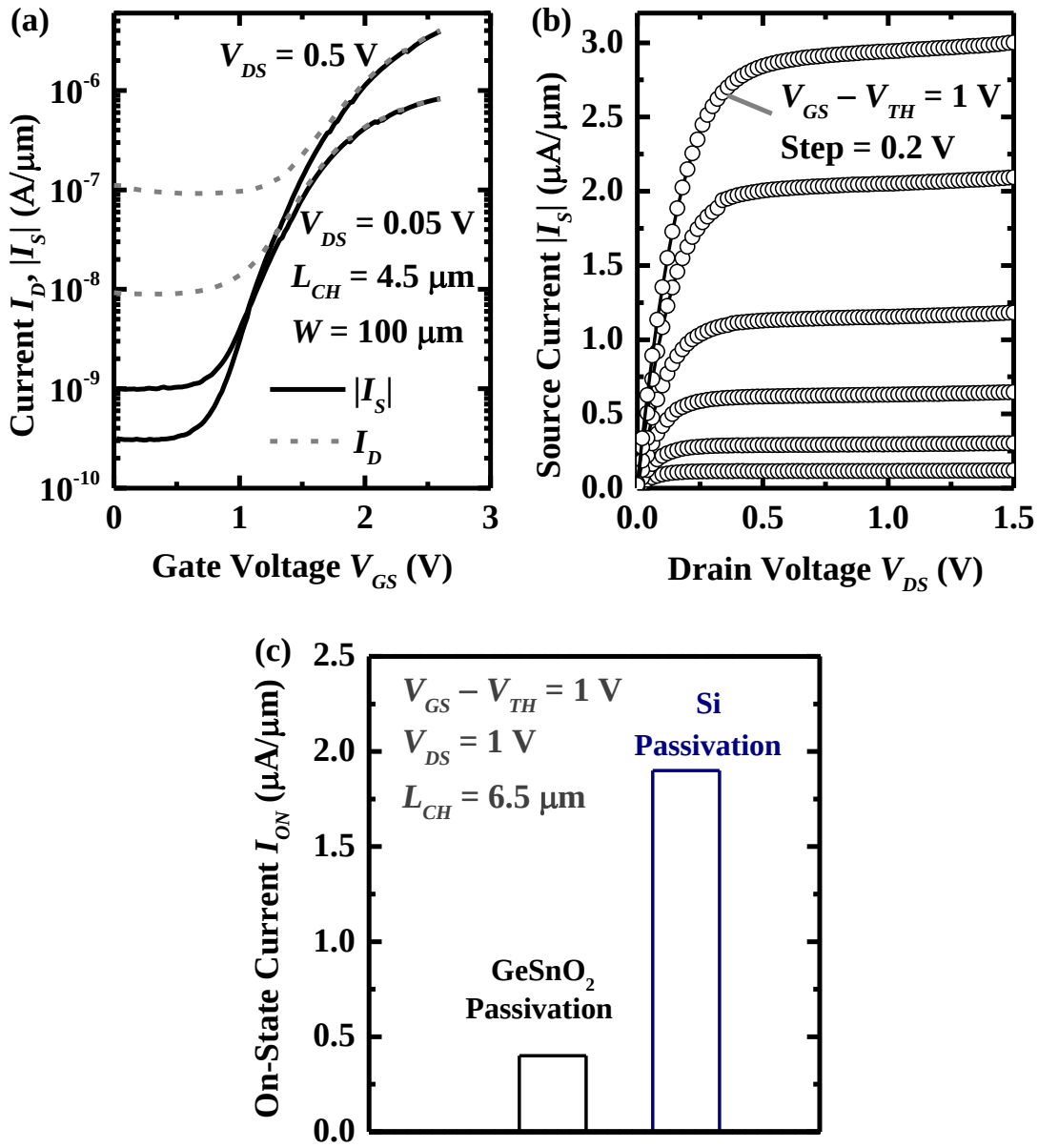


Fig. 5.24. (a) I_D - V_{GS} and $|I_S|$ - V_{GS} transfer characteristics of a typical $Ge_{0.976}Sn_{0.024}$ nMOSFET with L_{CH} of 4.5 μm. The S of this device is ~230 mV/decade. (b) The $|I_S|$ - V_{DS} characteristics of the same device in (a). Good saturation behavior is observed. (c) Device with Si passivation shows a higher I_{ON} as compared to that with $GeSnO_2$ passivation at the same bias conditions.

Fig. 5.24(a) shows the drain current I_D - V_{GS} and source current $|I_S|$ - V_{GS} transfer characteristics of a typical $Ge_{0.976}Sn_{0.024}$ nMOSFET with channel length L_{CH}

of 4.5 μm. The *S* of this device is ~230 mV/decade. The leakage floor of I_D is ~2 orders higher than that of $|I_S|$ under the same V_{DS}. This high leakage floor of I_D is mainly due to the large drain-to-body junction leakage current, which is possibly caused by the defects at this n^+/p junction. The $|I_S|$ - V_{DS} characteristics of the same device are shown in Fig. 5.24(b). The gate overdrive ($V_{GS} - V_{TH}$) was varied from 0 to 1 V in steps of 0.2 V. Excellent saturation behavior is observed. The I_{ON} of this device is 3 μA/μm at $V_{DS} = V_{GS} - V_{TH} = 1$ V. For another device with L_{CH} of 6.5 μm, the I_{ON} is 1.94 μA/μm at the same bias condition. Fig. 5.24(c) compares the I_{ON} of Si passivated $Ge_{0.976}Sn_{0.024}$ nMOSFET with that of $GeSnO_2$ passivated device [86]. At the same bias conditions, device with Si passivation exhibits a higher drive current as compared to that with $GeSnO_2$ passivation (0.4 μA/μm), which could be due to the better interface quality achieved by using Si passivation.

5.3.3 Effects of FGA on the Electrical Characteristics of GeSn nMOSFETs

FGA is widely used to passivate the dangling bonds at the Si/SiO_2 interface in Si CMOS technology. It has also been shown that FGA is effective in reducing the interface trap density and improving the device performance of Ge MOSFETs [161],[186]-[188]. In this experiment, FGA with 10% H_2 and 90% N_2 was performed at 300 ˚C for 20 minutes to investigate its effects on the gate dielectric/$Ge_{0.976}Sn_{0.024}$ interface quality. It was reported that significant amount of Al can diffuse into Ge at a temperature higher than 370 K [189]. If the Al atoms diffuse beyond the n^+ GeSn region, it will cause an electrical short between the source and drain by forming

ohmic contact to the p-type body. To avoid this problem, FGA was performed before the Al contact formation.

Fig. 5.25 shows the inversion *C* - *V* characteristics of a $Ge_{0.976}Sn_{0.024}$ nMOSFET with FGA. A smaller frequency dispersion is observed as compared to device without FGA (Fig. 5.23). This is attributed to the passivation of interfacial dangling bonds and bulk traps in HfO_2 by hydrogen during the FGA process. Fig. 5.26 compares the transfer characteristics of $Ge_{0.976}Sn_{0.024}$ nMOSFETs with and without FGA. It is observed that by performing FGA, *S* of the transistor is improved from ~230 mV/decade to ~190 mV/decade. The statistical plot of *S* in Fig. 5.27 shows that the $Ge_{0.976}Sn_{0.024}$ nMOSFETs with FGA exhibit 10% improvement in *S* as compared to those without FGA. The improvement in *S* indicates that the mid-gap D_{it} is reduced.

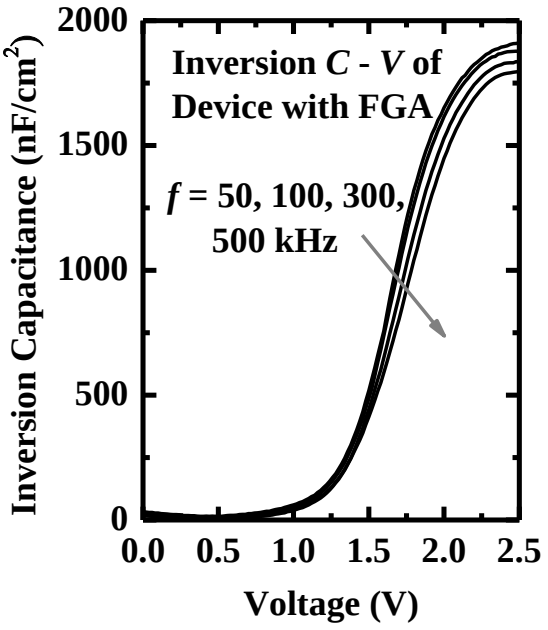


Fig. 5.25. Inversion *C* - *V* characteristics of a $Ge_{0.976}Sn_{0.024}$ nMOSFET with FGA. Passivation of interfacial dangling bonds and bulk traps in HfO_2 by hydrogen during FGA contributes to a smaller frequency dispersion as compared to device without FGA (Fig. 5.23).

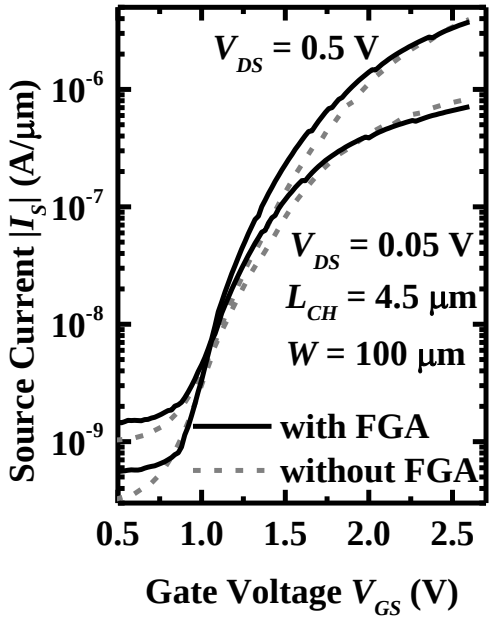


Fig. 5.26. The transfer characteristics of $Ge_{0.976}Sn_{0.024}$ nMOSFETs with and without FGA. It is observed that *S* improves from ~230 mV/decade to ~190 mV/decade by performing FGA.

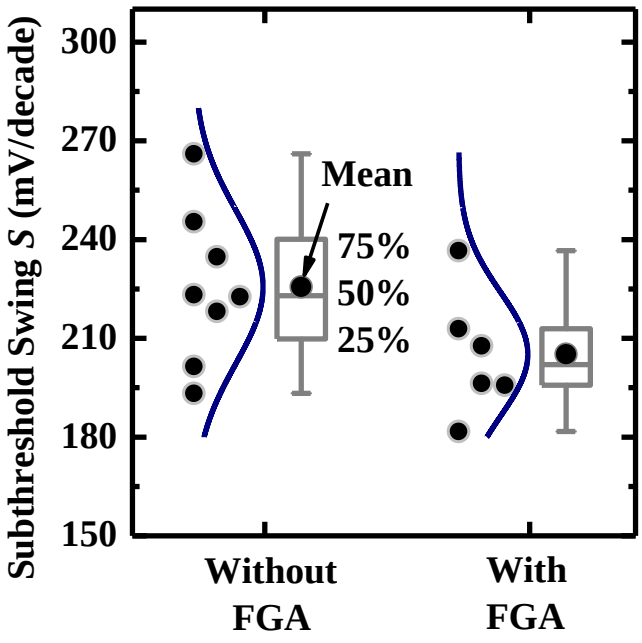


Fig. 5.27. Statistical plot shows the *S* enhancement due to FGA. The mean *S* of the $Ge_{0.976}Sn_{0.024}$ nMOSFETs with FGA is 200 mV/decade. This is 10% lower as compared to that of devices without FGA.

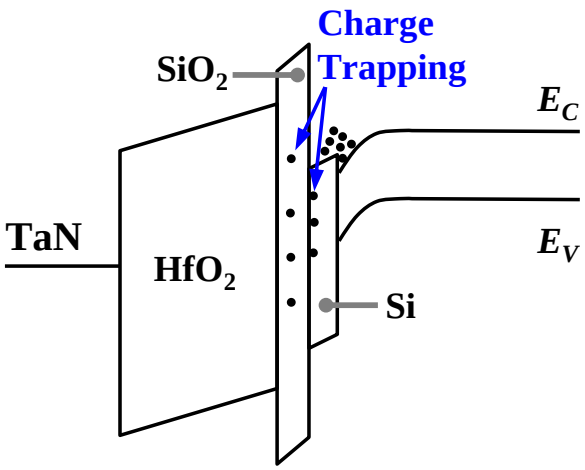


Fig. 5.28. Schematic of the energy band diagram along the gate-to-channel direction of a $Ge_{0.976}Sn_{0.024}$ nMOSFET in the strong inversion regime. The trapped charges can degrade the electron mobility due to Coulomb scattering.

It is noted that the I_{ON} of the $Ge_{0.976}Sn_{0.024}$ nMOSFETs with Si passivation in this work is still quite low. The high interface state density near the conduction band edge could be responsible for the low drive current. It was reported that the D_{it} near the conduction band edge in Si-passivated Ge MOSFETs is high, which affects the electron mobility [190]. In addition, the negligible conduction band offset between $Ge_{0.976}Sn_{0.024}$ and Si will cause charge trapping at the SiO_2/Si interfaces as well as in the bulk of SiO_2 and HfO_2, which will degrade the carrier mobility due to remote Coulomb scattering as illustrated in Fig. 5.28.

The large S/D resistance is another reason for the low drive current. Fig. 5.29 plots the total resistance R_{Total} between source and drain terminals versus L_{CH} for $Ge_{0.976}Sn_{0.024}$ nMOSFETs at V_{DS} = 0.1 V and $V_{GS} - V_{TH}$ = 1 V. The intercept of the fitted line with the vertical axis yields a high S/D resistance (~50 kΩ·μm), which limits the drive current. To reduce the S/D resistance, the n-type dopant concentration in the S/D regions has to be improved. This can be achieved by using

raised S/D structure with *in situ* doping [191]-[192], laser annealing [193] and co-implantation techniques [194].

In addition, the compressive strain in the epitaxial $Ge_{0.976}Sn_{0.024}$ film is also responsible for the low drive current. This is because the compressive strain will cause a reduction in the effective electron mobility [88]. To further improve the drive current of $Ge_{1-x}Sn_x$ nMOSFET, relaxed or tensile strained $Ge_{1-x}Sn_x$ substrate should be employed. Advanced technique to realize fully relaxed and tensile strained Ge_xSn_{1-x} film has been recently demonstrated [195]. This can enable the realization of high mobility $Ge_{1-x}Sn_x$ n-channel transistors.

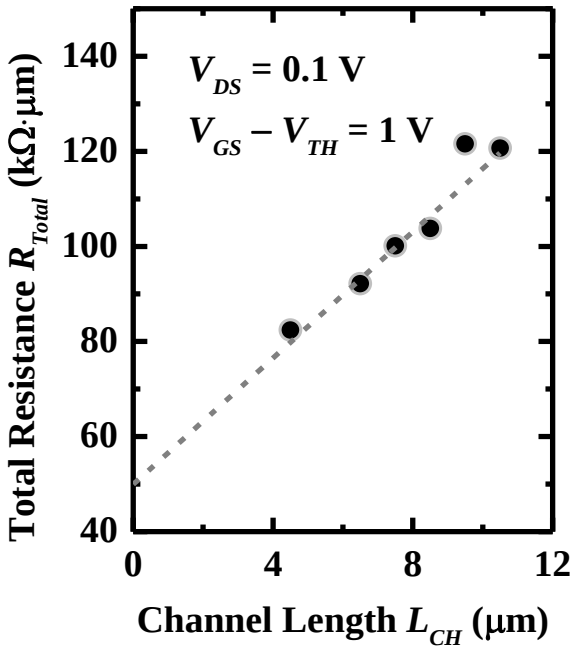


Fig. 5.29. Plot of R_{total} versus L_{CH} for $Ge_{0.976}Sn_{0.024}$ nMOSFETs at V_{DS} = 0.1 V and $V_{GS} - V_{TH}$ = - 1 V. The high S/D resistance limits the drive current of the transistors.

5.4 Summary

In this Chapter, the impact of Si passivation layer thickness on the I_{ON} and μ_{eff} of $Ge_{0.97}Sn_{0.03}$ pMOSFETs was studied. The hole mobility of $Ge_{0.97}Sn_{0.03}$ is improved by increasing the Si passivation layer thickness from 4 to 7 ML, and this is attributed to the reduced Coulomb scattering by trapped charges in the gate stack. In addition, the effects of PMA on $G_{m,int}$, S, and μ_{eff} of the Si passivated $Ge_{0.97}Sn_{0.03}$ pMOSFETs were investigated. By performing PMA for $Ge_{0.97}Sn_{0.03}$ pMOSFETs, the D_{it} was reduced, leading to enhanced $G_{m,int}$, S, and μ_{eff}. The Si passivation layer thickness and PMA conditions are important parameters for the performance enhancement of $Ge_{0.97}Sn_{0.03}$ pMOSFETs.

$Ge_{0.976}Sn_{0.024}$ nMOSFETs with low-temperature Si surface passivation were also demonstrated. Devices with Si surface passivation exhibit higher drive current as compared to those with $GeSnO_2$ passivation. FGA reduces the frequency dispersion of the inversion C - V characteristics and improves the S. This is attributed to the passivation of interfacial dangling bonds and bulk traps in HfO_2 by hydrogen during FGA. Further reduction of D_{it} near the conduction band edge and S/D resistance would be needed to achieve a higher drive current. Relaxed or tensile strained $Ge_{1-x}Sn_x$ substrate can also help to further increase the drive current by improving the electron mobility.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

The power consumption of complementary metal-oxide-semiconductor (CMOS) circuit increases tremendously and becomes a critical issue as the transistor dimensions continue to scale down over the technology generations. To reduce the power consumption, supply voltage V_{DD} has to be lowered without compromising the on-state current I_{ON}. This can be achieved by using advanced transistors with steep switching behavior or employing metal-oxide-semiconductor field-effect transistors (MOSFETs) with high-mobility channel materials.

This thesis focuses on the investigation of potential device candidates, i.e. tunneling field-effect transistor (TFET) and germanium-tin ($Ge_{1-x}Sn_x$) MOSFET, to achieve V_{DD} reduction in future technology nodes. Unlike a conventional MOSFET, TFET exploits the gate-controlled band-to-band tunneling (BTBT) mechanism to realize a subthreshold swing S of less than 60 mV/decade at room temperature. In order to have a more comprehensive understanding of the device physics of TFET, the strain and temperature dependence of the tunneling current was studied in Chapter 2 [29]. As silicon (Si)-based TFETs suffer from low I_{ON} due to the large bandgap of Si, employing heterostructures in TFETs is an effective method to improve the I_{ON}.

TFETs with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}/Si$ (Chapter 2) [197] and $Ge/In_{0.53}Ga_{0.47}As$ (Chapter 3) [198] heterostructures were experimentally demonstrated and the electrical performance of fabricated devices was analyzed in detail. Besides TFET, MOSFET with high-mobility channel material is another technology option to achieve high I_{ON} at a reduced V_{DD}. $Ge_{1-x}Sn_x$ is a promising channel material to realize high-mobility MOSFET as it has higher carrier mobilities as compared with Si and germanium (Ge). Both p-channel [199] and n-channel [200] $Ge_{1-x}Sn_x$ MOSFETs using Si surface passivation technique were demonstrated. The contributions of this thesis are listed in next Section.

6.2 Contributions of This Thesis

6.2.1 Strain and Temperature Dependence of Tunneling Current

For the first time, the dependence of the electrical characteristics of TFET on strain was investigated in Chapter 2 [29]. The results provide guidance on strain engineering of TFET and also understanding of the band-to-band tunneling mechanism. In addition, the underlying physics of the TFET device was probed by observing the dependence of the tunneling current on temperature [29]. Based on the unique temperature dependence of the tunneling current, a temperature independent current biasing circuit employing TFET was proposed and experimentally demonstrated. The demonstrated circuit achieved a low temperature sensitivity within ± 120 ppm/K [196].

6.2.2 TFET with $Si_{0.5}Ge_{0.5}/Si_{0.989}C_{0.011}/Si$ Heterostructure

Vertical $Si_{0.5}Ge_{0.5}$ source TFETs with a thin layer of strained $Si_{0.989}C_{0.011}$ (~8 nm) inserted at the tunneling junction were demonstrated and the impact of this $Si_{0.989}C_{0.011}$ layer on the electrical characteristics of TFETs was investigated in Chapter 3 of this thesis [197]. The insertion of $Si_{0.989}C_{0.011}$ layer lowers the energy of the conduction band edge E_C in the channel. At the same time, it contributes to a steep p^+ dopant profile at the source/channel interface by suppressing boron diffusion. As a result, $Si_{0.5}Ge_{0.5}$ source TFET with $Si_{0.989}C_{0.011}$ layer exhibits higher I_{ON} and steeper S as compared to the one without $Si_{0.989}C_{0.011}$ layer.

6.2.3 TFET with $Ge/In_{0.53}Ga_{0.47}As$ Heterostructure

High quality Ge was successfully grown on $In_{0.53}Ga_{0.47}As$ substrate using a metal-organic chemical vapor deposition tool. X-ray photoelectron spectroscopy analysis revealed that $Ge/In_{0.53}Ga_{0.47}As$ interface has a staggered band alignment and the energy of the valence band edge E_V in Ge is higher than that in $In_{0.53}Ga_{0.47}As$ by 0.5 ± 0.1 eV (Section 4.4.2 of Chapter 4). Therefore, $Ge/In_{0.53}Ga_{0.47}As$ is a promising source/channel structure for TFET. Lateral TFETs with $Ge/In_{0.53}Ga_{0.47}As$ tunneling junction were experimentally realized for the first time (Chapter 4) [198]. The device concept and experimental results were discussed in detail.

6.2.4 $Ge_{1-x}Sn_x$ MOSFET with Si Surface Passivation

In Chapter 5, the fabrication of $Ge_{0.97}Sn_{0.03}$ p-channel MOSFETs (pMOSFETs) with low-temperature Si surface passivation was documented. The impact of Si

surface passivation layer thickness on the electrical performance of $Ge_{0.97}Sn_{0.03}$ pMOSFETs was studied [199]. The effects of post metal annealing on the I_{ON}, S, and hole mobility μ_{eff} of Si passivated $Ge_{0.97}Sn_{0.03}$ pMOSFETs were investigated. In addition, $Ge_{0.976}Sn_{0.024}$ n-channel MOSFETs (nMOSFETs) with Si surface passivation, achieving a higher drive current than devices passivated by $GeSnO_2$, were demonstrated [200]. This was the first demonstration of Si surface passivation for GeSn nMOSFET. Moreover, the effects of forming gas annealing were also investigated.

6.3 Future Directions

6.3.1 I_{ON} Enhancement for TFETs

Novel heterostructures were proposed for TFETs as discussed in Chapter 3 and 4. However, the fabricated TFETs still suffer from low I_{ON} and poor S as compared to the state-of-the-art Si MOSFETs. III-V materials with highly staggered band alignment or broken-gap alignment [57],[201], such as AlGaSb/InGaAs [55],[202] and AlGaAsSb/InGaAs [203] heterostructures, should be considered to further improve the device performance. In addition, innovative source structure designs can also be further explored, such as extended source structure [66] and structure with tunneling in-line with gate field [56],[64].

6.3.2 P-Channel TFETs

Until now, research efforts have been devoted to n-channel TFETs. However, there is still a lack of research in p-channel TFETs. Recently, $Ge_{1-x}Sn_x$-based p-

channel TFET with promising results has been demonstrated [204]. The substitutional tin (Sn) composition of the $Ge_{1-x}Sn_x$ alloy can be optimized to achieve high band-to-band tunneling rate while preserving a low off-state leakage current I_{OFF}. III-V heterostructure, such as InAs/AlGaSb [55], can also be explored for the fabrication of p-channel TFET.

6.3.3 Surface Passivation for GeSn pMOSFETs

The thickness of the Si passivation layer has significant impact on the I_{ON}, S, and μ_{eff} of Si passivated $Ge_{1-x}Sn_x$ pMOSFETs (Chapter 5). It is also worthwhile to study the effects of Si passivation layer growth temperature on the electrical performance of $Ge_{1-x}Sn_x$ pMOSFET. It is anticipated that Ge and tin (Sn) atoms may segregate into the Si layer during the passivation process, which will cause trap states in the gate stack. Si passivation using a lower temperature may help to suppress Ge and Sn segregation. In addition, other novel surface passivation techniques can be explored for $Ge_{1-x}Sn_x$ pMOSFETs, such as high pressure oxidation [205] and plasma post oxidation [206].

6.3.4 Processing Technology of GeSn nMOSFETs

Although GeSn nMOSFETs with Si passivation exhibit a higher I_{ON} as compared to those with $GeSnO_2$ passivation, the I_{ON} of Si passivated GeSn nMOSFETs is still low. There are few possible methods to further improve the drive current of $Ge_{1-x}Sn_x$ nMOSFETs. Firstly, alternative surface passivation techniques that can achieve low interface trap density D_{it} near the E_C of $Ge_{1-x}Sn_x$ nMOSFETs should be further explored. The conduction band offset between the surface

passivation layer and $Ge_{1-x}Sn_x$ should preferably be large to suppress the Coulomb scattering due to the interface trap states in the gate stack. Secondly, the source/drain (S/D) doping concentration can be improved to lower the S/D sheet resistance and reduce the contact resistance between metal contact and $Ge_{1-x}Sn_x$. This can be achieved by using raised S/D structure with *in situ* doping [191]-[192], laser annealing [193], and co-implantation [194] techniques. Lastly, the Sn composition can be further increased to achieve higher electron mobility. In addition, relaxed or tensile strained $Ge_{1-x}Sn_x$ should be realized to further enhance the electron mobility. Advanced technique to achieve relaxed $Ge_{1-x}Sn_x$ has been reported recently [195].

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Appendix

List of Publications

Publications Related to This Thesis Work

[1] **P. Guo**, L. Yang, Y. Yang, L. Fan, G. Han, G. Samudra, and Y.-C. Yeo, "Tunneling field effect transistor: Effect of strain and temperature on tunneling current," *IEEE Electron Device Letters*, vol. 30, pp. 981 - 983, 2009.

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Other Co-authored Publications

[10] G. Han, **P. Guo**, Y. Yang, L. Fan, Y. S. Yee, C. Zhan, and Y.-C. Yeo, "Source engineering for tunnel field-effect transistor: Elevated source with vertical silicon-germanium/germanium heterostructure," *Japanese Journal of Applied Physics*, vol. 50, 04DJ07, 2011.

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