TOPOLOGY STUDIES AND CONTROL OF MICROINVERTERS FOR PHOTOVOLTAIC APPLICATION

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Topology Studies and Control of Microinverters for Photovoltaic Applications

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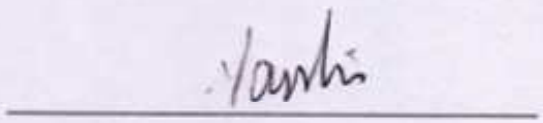
DECLARATION

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

The thesis has also not been submitted for any degree in any university previously.



Li Yanlin

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List of Publication Associated to the Research Work

Journal papers:

1. L. Yanlin and R. Oruganti, "A Low Cost Flyback CCM Inverter for AC Module Application," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 1295-1303, 2012.
2. Li, Y. and Oruganti, R. “A flyback-CCM inverter scheme for photovoltaic AC module application” Australian Journal of Electrical and Electronics Engineering, v6, n3, p301-309, 2009.

Conference papers:

1. L. Yanlin and R. Oruganti, "A low cost high efficiency inverter for photovoltaic AC module application," in *Photovoltaic Specialists Conference (PVSC), 2010 35th IEEE*, 2010, pp. 002853-002858
2. L. Yanlin and R. Oruganti, "A flyback-CCM inverter scheme for photovoltaic AC module application," in *Power Engineering Conference, 2008. AUPEC '08. Australasian Universities*, 2008, pp. 1-6

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CHAPTER 1: INTRODUCTION

1.1 Background

In traditional electric grid system, the central plants to generate electricity are usually placed either close to the energy resources (such as hybroelectric plants) or purposely located far from city areas to prevent the heavy air pollution from affecting the populated areas (such as coal plants). This requires the bulk power to be distributed for a long distance through a transmission & distribution grid from central plants to where the load is connected.

However, due to the emerging oil shortage and increasing concerns on CO2 emission and global warming, various renewable energy resources with zero/negligible emission have been identified as attract alternatives to conventional energy resources.

Solar energy is one of the most promising renewable energy resources in use nowadays. Integration of renewable energy resources to traditional electric grid system brings both benefits and challenges.

On the one hand, because of the ubiquitousness of sunlight, ease of installation, as well as environment-friendly feature (no emission and no noise), PV generation system can be installed conveniently on the roof of buildings in towns and cities, where the major part of energy consumption occurs. In this way, the amount of energy loss in transmitting electricity can be reduced by the distributed power

generation compared with the conventional centralized electricity generation. On the other hand, technical issues such as the power quality and system stability, caused by the interaction between the distributed PV system and grid need to be examined and additional protective devices may be required. Also the intermittency of solar energy resources would place requirement for better energy management through energy storage or additional capacity installation, especially for a large penetration of solar power into the grid.

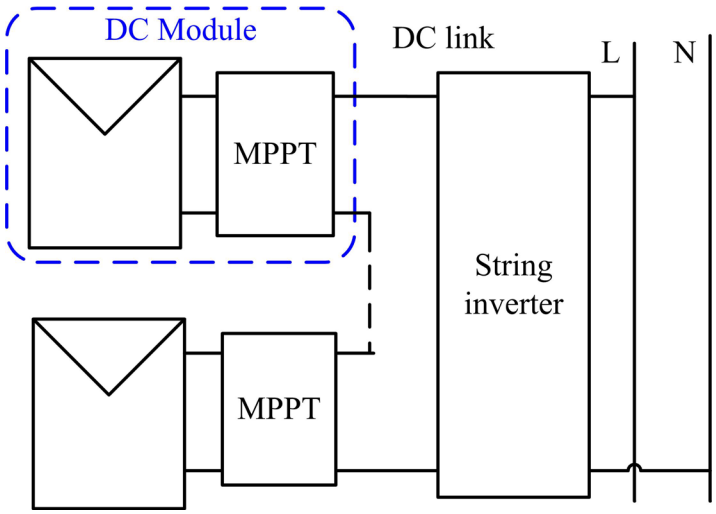


Fig.1.1: DC module and String Inverter

Compared to PV systems based on the processing of the energy output of several PV panels connected directly in series and parallel, power generation based on the processing of energy output of single PV modules individually has become a new trend [1-4] . Here, two major approaches have been noticed in both academic and industry work, viz., “DC module” [5-9] and “AC module”[10-13] based on their output features.

As shown in Fig.1.1, the term “DC module” refers to a PV module connected

to or integrated with an individual Maximum Power Point Tracking (MPPT) converter or "power optimizier" [5-9]. With the MPPT guaranteed by the local converter, the outputs of the DC modules are then connected in series and to a string inverter before feeding into grid.

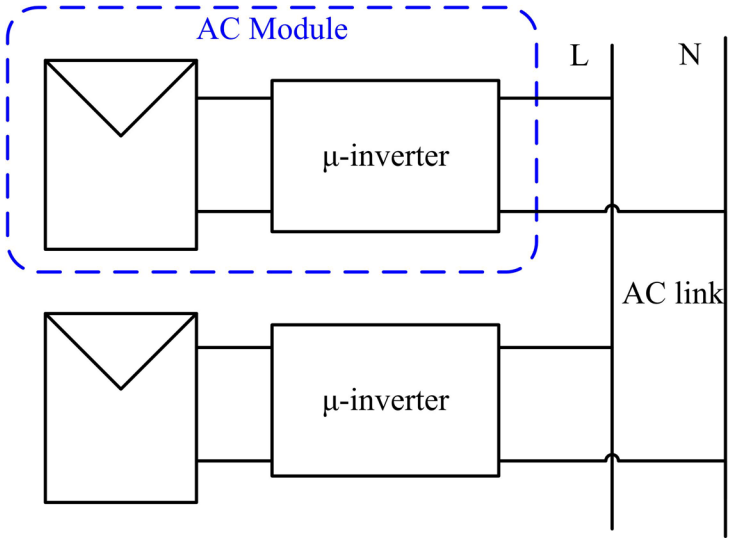


Fig.1.2: AC module and micro-inverter

The concept of an "AC module", which refers to a PV panel with an integrated "microinverter", was conceived 30 years ago by researchers at Caltech's Jet Propulsion Laboratory and Sandia National Lab [13]. As illustrated in Fig.1.2, their vision envisaged AC modules which "will be available at local hardware store and can be as easy to install as a string of light bulbs. [13]"

In both DC and AC module approaches, the maximum power point (MPP) of each panel can be tracked individually. Thus, the effects due to shading and module mismatches and orientation variations are almost totally eliminated and the utilization of the whole PV system is improved. This feature is vital in densely built areas where shading due to adjacent buildings or trees is inevitable. AC modules are

especially suitable for Building Integrated PV (BIPV) systems, where PV panels are integrated with building materials and mounted on the building surfaces whose orientations are all not likely to be the same.

Besides, the AC module approach has its own unique advantages in terms of installation, maintenance and safety. Some of these are outlined below.

(1) According to NEC 690.11[14], "photovoltaic systems with DC source circuits, DC output circuits or both, on or penetrating a building operating at a PV system maximum system voltage of 80 volts or greater, shall be protected by a listed (DC) arc-fault circuit interrupter, PV type, or other system components listed to provide equivalent protection." Such a requirement, does not apply to AC modules with AC output only. Also, no special expertise for DC wiring is needed for installation and maintenance of AC module. This is an important advantage in the acceptance of PV systems among population.

(2) Secondly, the "plug and play" property allows the customers to install a small number of AC modules in the beginning and expand the system easily through paralleling of additional AC modules. There is no need to match the new AC modules with the existing ones in any manner. Different PV technologies can be mixed.

(3) Failure of one module will not influence other modules. The limitation imposed by the 'weakest link' on a PV array of serial/parallel connected modules is eliminated, which would improve system reliability.

(4) If failure of one AC module is detected, the removal and repair work can be carried out without influencing the other modules, again by a non-expert, safely.

All of the above features make the AC module approach, based on microinverters, a promising technology to improve PV penetration into the grid.

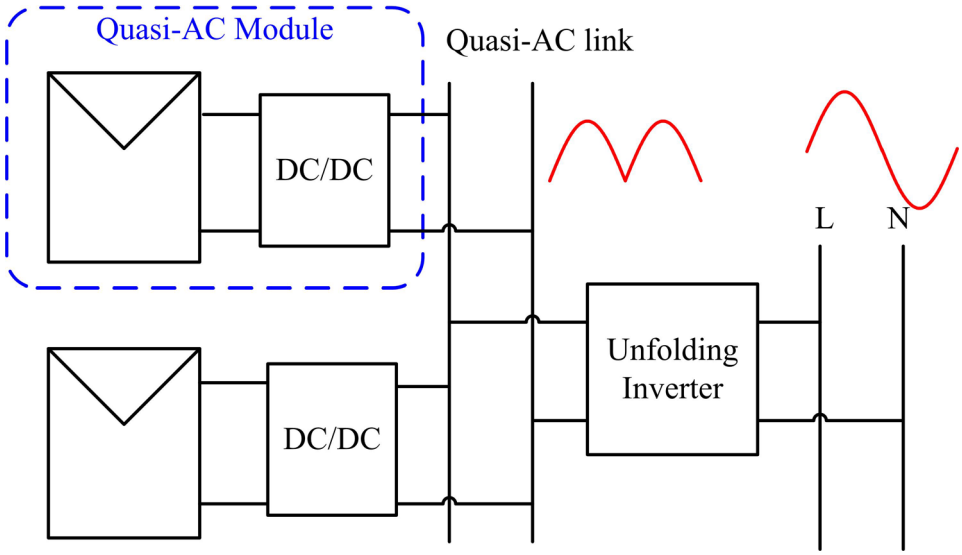


Fig.1.3: Quasi-AC module and unfolding inverter

Other than the above two popular approaches, an alternative "Quasi-AC module" approach has been proposed in [15] (Fig.1.3). A quasi-AC module supplies a unidirectional current but in the shape of a rectified sinusoid. These quasi-AC modules are connected to a quasi-AC link, which, in turn, feeds power to the centralized unfolding inverter. Although different in system structure, the DC/DC converter and its control is similar to that in AC module solution based on unfolding inverter, which will be studied in literature survey in Chapter 2.

1.2 Introduction to Microinverter

A microinverter, generally, refers to a low power inverter designed to handle the output of a single PV module (usually in the range of 100~300W). Its external connections and internal structure are shown in Fig.1.4 .

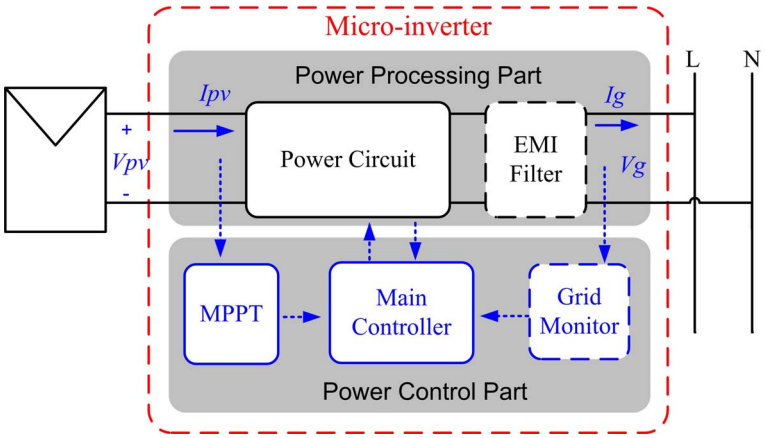


Fig.1.4: System diagram of a microinverter

As illustrated in Fig.1.4, a microinverter consists of two major parts: a power processing part and a power control part.

The power processing part is connected to a PV module on the input side. The PV module converts the photon energy of light into Direct Current (DC) by photovoltaic effect. The PV module output is fed to the power circuit, which converts the DC into Alternating Current (AC) required by the utility. As the fast switching waveforms of the present day inverter technology would generate high frequency electromagnetic noise, an EMI filter is needed between the inverter and the utility to prevent high frequency noise currents from entering the grid and causing interference to other systems connected to the same utility.

The power control part is divided into three function blocks based on the requirements of the PV panel and grid connection.

Among them, MPPT (Maximum Power Point Tracking) is used to obtain the maximum power from the PV panel as the panel's output characteristics changes with environmental conditions.

Grid monitor is connected to the utility to detect its working condition and stop and restart the inverter as and when necessary. It also helps in synchronizing the inverter waveform with the grid voltage waveform. Detailed requirements and specifications are listed in several national and international standards concerning the interconnection of distributed generation systems with the grid and will be discussed later in this chapter.

Receiving the signals from MPPT and Grid monitor, the main controller directly controls the inverter to obtain a sinusoidal output current in phase with the grid voltage and with a low THD (Total Harmonics Distortion).

As an interface between a single PV module and the AC grid, the power circuit of a microinverter needs to cater to the requirements from both sides. Generally speaking, it needs to have 1) MPPT function to match with the PV module, and 2) high voltage boost and DC/AC conversion capability to match with the grid. These requirements are further explained below.

1.2.1. Power Processing Requirements

For the power processing part, the input side requirements are determined by the choice of the PV panel used. The developments in PV technologies focus on improving the conversion efficiency of the PV cell and on reducing the system cost. Various PV cell technologies, based on different materials and fabrication methods are currently under active research. These include silicon based technologies (in the mono-crystalline, poly-crystalline, amorphous and micro-crystalline forms), and technologies based on III-V compounds, organics, nanotechnology and multi-junctions [16, 17]. Despite all the exciting progress in the research laboratories around the world, most of the commercial PV products at present are still based on mono-crystalline and poly-crystalline silicon. It is believed that they would continue to dominate the PV market for at least another decade [18]. This belief is further strengthened by the recent plummeting of the cost of silicon PV modules.

The specifications of the applicable PV panels (above 100W) from several major global manufacturers [19] are listed in Table 1.1. This list, though not a complete list of all the panels available, gives a good idea of the voltage and current ranges of the normally available panels. As shown in Table 1.1, the number of cells per module is in the range of 36 to 72. Each PV cell is actually a p-n junction with a forward voltage around 0.5V, which makes the output voltage to be in the range of 18~36V at MPP.

In order to connect to the grid with AC voltage in the range of 100 ~ 230Vrms, the low input voltage would need to be boosted by up to around 10~20 times. This

variable and high step-up ratio needs to be considered in the selection and design of inverter topology.

Table 1.1: Panel specifications under STC (Standard Test Conditions: Irradiance 1kW/m2, AM1.5 spectrum, module temperature 25 °C)

Manufacturer	Module [1]	MPP Voltage	MPP Current	Number of Cells
Unit		V	A	
Kyocera	KC130TM/GT	17.6	7.39	36
	KD135GX-LP	17.7	7.63	36
	KC175GT	23.6	7.42	48
	KD180GX-LP	23.6	7.63	48
	KC200GT	26.3	7.61	54
	KD 205/210 GX-LP	26.6	7.71/7.9	54
Sharp	NE-Q5E2U	34.6	4.77	72
	NT-175U1	35.4	4.95	72
	ND-187U1F	25.8	7.25	54
	ND-200/ 216	28.42~28.71	7.04~7.53	60
Shell	SP150-P	34	4.4	72
	Ultra 165/175 -PC	35/35.4	4.72/ 4.95	72
Solar World	SW130/140/150 Poly	18.9~20.1	6.9~7.5	40
	SW155/165/175 Poly	34.8~36	4.5~4.9	72
	SW165/175 mono	34.4/35.7	4.8/4.9	72
	SW160~185 mono	35~36.3	4.58~5.1	72
	SW200/210/220 Poly	28.6~29.8	7~7.4	60
Sun Power	SPR-205/215/220	~40.0	5.13~5.53	72
Sun Tech	STP160/165/170/175/180S	34.4~35.6	4.65~5.05	72
	STP 190/200/210	26~26.4	7.31~7.95	54
	STP 260/270/280 S	~35	7.43~7.95	72
BP solar	REW/ BP3-125/130	17.4/17.3	7.2/7.5	36
	REW/BP3-155/160/165/170/175	34.4~36	4.5~4.9	72
	REW/BP4-160/165/170/175	34.3~35.6	4.5~4.9	72
	BP3-210/220/230	28.9~29.2	7.3~7.9	60
	SX3-195/200	24.4.24,5	7.96/8.16	50
Conergy	SC170/175/180M	35.5~36	4.79~5	72
	S 190-210P	26~26.4	7.31-7.95	54
	Powerplus 190-230 P/M	25~30	6.72~7.95	60
	YL 210/220 Wp	29/30	7.2/7.4	60

[1] Usually, the number in the name of PV panel (for example the digits '130' in Kyocera KC130TM/GT) indicates the power level in W.

As each panel would need a separate inverter, a large enough power rating is preferred for AC module application so as to reduce the cost per watt. It is noted that with the increase of power level, the PV module current can reach as high as 8A at MPP in STC (Standard Testing Condition). The low voltage (18~40V) and high current (up to 8A) requirements at the PV side need to be considered in selecting a proper inverter topology.

One more factor to be considered is the voltage ripple seen by the PV panel which will affect its overall efficiency as discussed in the next section. The power topology selection and its design are also influenced by the need to keep this ripple small.

1.2.2. Power Control Requirements

Overall, the power control part is in charge of controlling the power processing part to ensure the requirement for operating at the MPP imposed by the PV module and requirements for the grid connection specified by international standards.

1.2.2.1. Maximum Power Point Tracking (MPPT) Requirement

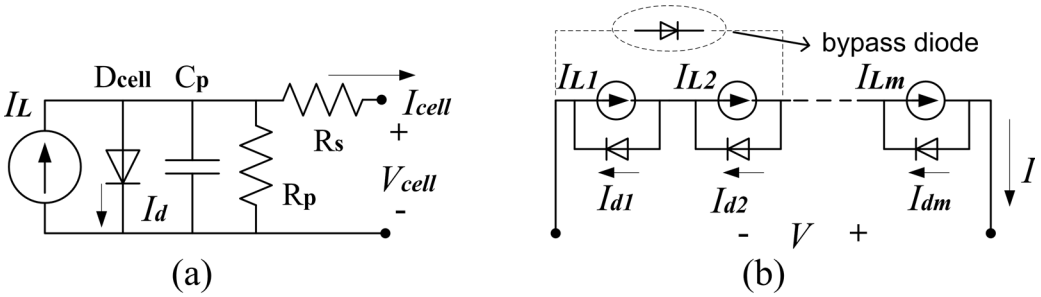


Fig.1.5: Simple electrical model of (a) a PV cell and (b) a PV panel made up of *m* cells in series

A PV cell is actually a large area p-n junction device with provision for external light to fall on the junction region to allow photovoltaic carrier generation. An electrical model that is commonly used to study its electrical characteristics is shown in Fig.1.5 (a). It is mainly composed of a light generated current source I_L and a diode in parallel. The generation of the current I_L involves two key processes [20]. The first is the absorption of incident photons resulting in the creation of electron-hole pairs. The second step is the separation of the electron and the hole by the action of the electric field existing in the p-n junction resulting in the generation of current. This p-n junction, however, also works as an internal load represented by the diode in Fig.1.5.

The parasitic elements shown in Fig. 1.5(a), such as the parallel capacitor C_p, is neglected in our simple analysis.The model of a PV panel made up of *m* cells in series is illustrated in Fig.1.5 (b). In an ideal case, assuming that all cells are perfectly matched, the equation for the I-V curve of the PV panel is obtained as:

$$I = I_L - I_d = I_L - I_o\left[\exp(\frac{V}{m \times nV_t}) - 1\right] \tag{1-1}$$

where, I_o is the reverse saturation current of the diode, m is the number of solar cells in series, n is the ideality factor, and V_t is the thermal voltage of a semiconductor, which is given by $V_t = kT/q = 26mV$ at room temperature where k (=1.38×10^{-23} J/K) is the Boltzmanns constant, T is the absolute temperature (in K) and q (=$1.6\times10^{-19}C$) is the electron charge.

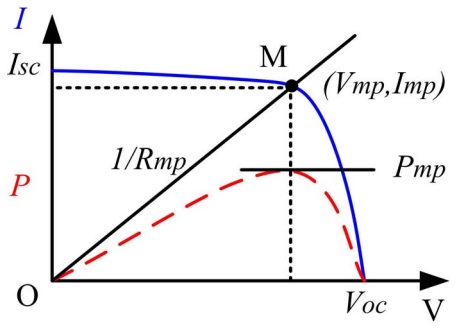


Fig.1.6: PV panel I-V curve (solid) and P-V curve (dashed) without shading

From the electrical model given by (1-1), the current-voltage (I-V) curve and power-voltage (P-V) curve of a PV panel can be obtained as illustrated in Fig.1.6. Here V_{oc} and I_{sc} refer to the open circuit voltage and short circuit current of the panel. The MPP is the point where the peak value of the P-V curve is reached, or the point on the I-V curve that defines the largest possible rectangle area ($=I_{mp}\times V_{mp}$) under it.

It may be noted that the idea behind the model is to reproduce the DC characteristic curve accurately and not the realization of an accurate physical model. An equation similar to the ideal PV equation is used to model the practical PV cell. Here, I_o and mnV_t are replaced with C_1 and C_2. These constants are selected so that the resulting PV characteristics match reasonably with the manufacturer's data. Thus, the parameters of V_{oc}, I_{sc}, V_{mp} and I_{mp} given by the manufacturer's datasheet can be taken as inputs to calculate two unknown parameters C_1 and C_2.

The characteristic resistance R_{mp}, of a PV panel is defined as the ratio of the voltage to current at MPP, equal to one over the slope of the line 'OM' through the MPP:

$$R_{mp} = \frac{V_{mp}}{I_{mp}} \tag{1-2}$$

If the effective load resistance seen by the panel is equal to this characteristic resistance, the maximum possible power is extracted from the panel. It is also noted that by increasing the illumination level, the current available at the MPP increases greatly. Though the MPP voltage does not change much with changing irradiance, it does increase significantly with reduction in temperature. Therefore, in order to make sure the maximum possible power is obtained under varying working conditions, an MPP tracking function must be included in the inverter control system.

The operating temperature of a PV panel will only change slowly due to the large thermal time constants involved, for example, 7~15 min for a BP Solar BP585 85W PV panel[21]. However, changes in irradiance can occur suddenly, e.g. caused by passing clouds [22]. The inverter should be capable of tracking the MPP fast enough during such changes in irradiation.

The maximum power obtainable also depends on the voltage ripple at the terminal of the PV panel. The ripple should be sufficiently small as any operating point deviation from MPP would result in power reduction. In [1], a second-order Taylor series approximation of the current has been used to calculate the average power from the panel when a sinusoidal voltage ripple is added upon the MPP voltage. The results show that the amplitude of the sinusoidal voltage ripple (usually at double the line frequency) should be below 8.5% of the MPP voltage in order to maintain

average operation at 98% of the MPP power. This also needs to be considered in any microinverter topology study.

1.2.2.2. Grid Connection Requirements

Traditionally, "utility electric power systems (grid or utility) were not intended to accommodate active generation at the distribution level [23]". Therefore, several standards have been evolved for dealing with the various issues involved in the interaction between the utility and the distributed generation systems. These standards have been developed by international organizations such as the IEEE (Institute of Electrical and Electronics Engineers) and IEC (International Electrotechnical Commission) , and institutions and utilities local to individual countries such as the National Fire Protection Association, Inc, Underwriter Laboratories, Inc. (UL) in the U.S.A. and the European Committee for Electrotechnical Standardization (CENELEC). Some of the most widely accepted standards include IEEE 1741 [23, 24], IEC 61727 [25], IEC 62109 [26], UL1741 [27] and National Electrical Code (NEC) 690.

According to these standards, the interconnection requirements mainly involve the following: 1) power quality requirement, 2) fault detection and protection, and 3) synchronization and reconnection. We will mainly use IEC61727 in our work as it establishes a unified standard that is widely used in different countries with different grid systems. A summary of the most important requirements from the grid connection point of view is listed in Table 1.2.

Table 1.2: Summary of Grid Connection Requirements (IEC61727)

<table>
<tr><td colspan="6">1) Power Quality Requirements</td></tr>
<tr><td colspan="6">Individual Harmonics in percent of maximum fundamental current (Odd) [1]</td></tr>
<tr><td>Order, h</td><td><11</td><td>11-15</td><td>17-21</td><td>21-33</td><td>THD</td></tr>
<tr><td>percentage</td><td>4.0%</td><td>2.0%</td><td>1.5%</td><td>0.6%</td><td>5%</td></tr>
<tr><td colspan="3">DC current injection</td><td colspan="3">Less than 1% of rated output current</td></tr>
<tr><td colspan="3">Power Factor at above 50% of rated power</td><td colspan="3">>0.9</td></tr>
<tr><td colspan="6">2) Fault Detection and Protection Requirements</td></tr>
<tr><td colspan="2">Type</td><td colspan="2">Abnormal condition</td><td colspan="2">Maximum trip time [3]</td></tr>
<tr><td colspan="2" rowspan="5">Voltage
(at the point of utility connection)</td><td colspan="2">V< 0.5×Vnominal</td><td colspan="2">0.1 s</td></tr>
<tr><td colspan="2">50% ≤ V < 85%</td><td colspan="2">2.0 s</td></tr>
<tr><td colspan="2">85% ≤ V < 110%</td><td colspan="2">Normal Operation</td></tr>
<tr><td colspan="2">110% ≤ V < 135%</td><td colspan="2">2.0 s</td></tr>
<tr><td colspan="2">135% ≤ V</td><td colspan="2">0.05 s</td></tr>
<tr><td colspan="2" rowspan="2">Frequency Range</td><td colspan="2">Within $\pm 1Hz$</td><td colspan="2">Normal Operation</td></tr>
<tr><td colspan="2">Outside the range of $\pm 1Hz$</td><td colspan="2">0.2 s</td></tr>
<tr><td colspan="2">Islanding</td><td colspan="2">Loss of utility</td><td colspan="2">2 s</td></tr>
<tr><td colspan="6">3) Synchronization and Reconnection Requirements</td></tr>
<tr><td colspan="4">Allowed voltage fluctuation range during synchronization [2]</td><td colspan="2">$\pm 5\%$ of prevailing voltage</td></tr>
<tr><td colspan="4">Normal Operation time before Reconnection</td><td colspan="2">20s to 5 min</td></tr>
</table>

[1] Even harmonics are limited to 25% of the odd harmonics.

2 Trip time refers to the time between the abnormal conditions occurring and the inverter ceasing to energize the utility line.

Of the requirements, the grid monitor unit in Fig.1.4 mainly takes care of fault detection/protection and synchronization/reconnection. For example, it disconnects the inverter from the grid when the monitored grid voltage or frequency goes beyond the specified range (see Table 1.2). Alternatively, when the utility grid is down due to a fault or a scheduled maintenance, 'Grid Monitor' should be able to detect the situation and cut down the power from microinverter so as to provide anti-islanding function. When the grid condition is normal again, the grid monitor assists in restarting the inverter and reconnecting to the grid. Besides, the grid monitor also helps in synchronizing the inverter voltage waveform with the grid voltage waveform under normal operating conditions. It is expected to be working all the time even

when the inverter is stopped. This allows it to wake the inverter up when the grid returns to normal.

Power quality requirement is fulfilled by the main controller. It is required that the total harmonic distortion (THD) in injected current, shall be less than 5% at the same PCC. In addition, each individual harmonic shall be less than a specified level. The detailed specifications of maximum individual harmonic current distortion as a percent of the maximum fundamental current are summarized in Table 1.2.

According to IEC 61727, the micro-inverter is not required to be capable of adjusting the power factor. But it shall operate at a power factor above 0.9 when the output is greater than 50% of rated inverter output power.

1.3 Motivation for the Present Work

At present, large power PV generation systems based on string inverters still form the bulk of installed PV systems. The cost of a micro-inverter based system is generally higher than that of a system based on string inverters since every PV module would require one inverter. Besides, for a large array of AC modules, additional monitoring and communication functions will usually become necessary and will add to the system cost. The plummeting cost of a solar panel ($2.29/Wp, lowest around $1/Wp based on [28]) has made the inverter cost a more visible figure ($0.71 /Wp according to [29]) in the total cost of a PV system.

The overall cost of generated energy is not only related to the initial cost of PV system, but also influenced by the efficiency of the inverter as well as its useful

operating lifetime. Therefore, various efforts have been taken in the development of this technology to provide an optimum trade-off between conversion efficiency, lifetime and cost. For example, as pointed out in [30], a study of single-phase PV inverters in industry with different technologies from 1994 to 2002, showed slight drop in inverter efficiencies in certain periods of time. This reduction in PV inverter efficiency indicates a consideration that the PV inverter efficiency may be traded-off in order to reduce cost. Different compromises between cost, efficiency and lifetime have made two approaches to stand out.

The first approach is to use an unfolding-type single stage inverter, most popularly based on flyback converter topology. This topology allows the required voltage level step-up, current shaping, Maximum Power Point Tracking (MPPT) all to be done in a single power processing stage with minimum component count. However, the electrolytic capacitor used on the PV side as the buffer between the constant input power from the PV panel and the pulsating output power to be delivered to the AC grid, is generally taken to be the bottleneck in realizing long system lifetimes. In order to meet long lifetime requirements, such an approach would incur additional cost on thermal management to bring down the temperature of the capacitor in order to prolong its lifetime. Another trade-off in this scheme is between efficiency and cost. Efforts to improve the system efficiency with this approach usually require adding a considerable number of components, through modifications, such as interleaving multiple power converters in parallel, using non-dissipative snubber circuits and using soft switching techniques [31, 32]. Other

efforts to increase the efficiency include but not limited to are control strategies to improve efficiency at light load, such as burst mode operation [33] or PFM (Pulse Frequency Modulation).

However, research in this area has invariably been based on Discontinuous Conduction Mode (DCM) operation of the flyback converter, which results in large RMS and peak current values and low efficiencies. The situation becomes worse with the low terminal voltage of the PV module and also with the increased switching frequency normally adopted to reduce the size of inverter. Before adopting a variety of efficiency improvement technologies, one question to ask would be: can we increase the efficiency by simply changing the circuit operation modes without adding further circuit components? A similar attempt has been found in [6] to use a combined DCM and Boundary Conduction Mode for a flyback microinverter in order to provide a high efficiency solution over a wide power range.

A possible extension here to improve efficiency is to operate the flyback converter in Continuous Conduction Mode (CCM). When operated in CCM, a flyback converter has lower peak currents and hence higher efficiencies. This has been exploited before in both DC/DC power conversion and AC/DC power factor correction applications [7]; however, this approach has not been studied in AC module applications. A major issue, which has perhaps prevented the use of the flyback-CCM scheme in this application earlier, is the presence of a right-half plane (RHP) zero in the duty cycle to output current transfer function. This issue does not

arise in the case of power factor correction circuit using flyback-CCM converter, since here the input current is controlled to follow the grid voltage. In such a power factor correction circuit, the RHP zero only shows up in the output voltage control, which has slower dynamic requirements. Hence, the issues regarding such a flyback-CCM scheme as a potential low cost microinverter need to be investigated and feasibility proven.

The second popular approach for microinverter is to replace the lifetime bottleneck, viz., the electrolytic capacitor, by a film capacitor, which is more reliable. However, a direct replacement with the same capacitance using film capacitors would be very expensive and bulky, hence would be unacceptable. A film capacitor can only be used when a small capacitance (usually below 100μF) is required to perform the power decoupling function. This is usually achieved by choosing or modifying inverter topologies to allow either a large average voltage or a large voltage ripple or both on the decoupling capacitor. As observed in previous publications [34, 35], for this type of approach, the lifetime improvement is achieved at the cost of more component count and reduced conversion efficiency. Recently [36-38], the focus in active power decoupling schemes have shifted from feasibility verification to efficiency improvement. These details will be discussed in Chapter 2. Overall, this approach, although superior in lifetime and reliability, currently still suffers from the drawback of a lower efficiency compared to the first approach, and this needs to be addressed.

1.4 Research Objectives & Thesis Contributions

Overall, the research work reported in this thesis is focused on microinverter topology study to provide a low cost, high efficiency and long lifetime solution, as well as to investigate and solve some of the main control problems associated with the proposed approaches. The key specifications of the microinverter under study are given in Appendix A.

1.4.1 Research Objectives

Specifically, the main objectives of the research work falls into the following categories:

To investigate power topologies which have the potential to achieve high conversion efficiencies at low cost;

To investigate the provision of active power decoupling feature in order to eliminate the usage of an electrolytic capacitor (aimed at increasing system lifetime), while maintaining high system efficiency;

To design a low cost and effective control system for the chosen topologies to achieve multiple control goals including: effective Maximum Power Point Tracking, active power decoupling and output current shaping requirements.

To verify the performance of the proposed topology and control system by simulation and experimental test whenever necessary.

1.4.2 Thesis Contributions

The major contributions of the thesis are as follows:

1. A low cost Flyback-CCM microinverter with indirect current control

A flyback inverter in CCM operation has been proposed and studied both theoretically and experimentally for a PV AC module application. The control challenges, posed by the RHP zero of the transfer function and by the wide variations in operating conditions have all been addressed. Two controller schemes, One Cycle Control (OCC) and Average Current Mode (ACM), have been investigated for indirect output current control of the proposed flyback-CCM inverter. Design considerations, issues and solutions in both control schemes have been discussed. Implementation issues with regard to current sensing using a unidirectional current transformer (CT) have been presented and addressed using bidirectional CT scheme. Experimental results show a satisfactory current tracking performance using Indirect ACC scheme with Total Harmonic Distortion (THD)<5% as required.

As a result, a significant improvement in European & CEC efficiency over the benchmark flyback-DCM scheme has been verified by experiment thereby clearly indicating that the proposed flyback-CCM scheme with indirect ACC can be a viable choice for low/medium power PV AC module applications.

2. A Parallel Power Processing (P3) scheme with active power decoupling

A parallel power processing (P3) scheme, which involves a transformer isolated main converter and a secondary side auxiliary converter, has been proposed with the aim of achieving active power decoupling without compromising on system efficiency. The proposed scheme has been studied with a flyback converter as the main power converter and a simple buck converter as the auxiliary converter. The requirement of the power decoupling capacitance has been investigated first. Different operating modes of the proposed circuit have been explored with pros and cons identified. The reduction of power decoupling capacitance using the pilot topology has been verified by simulation. Finally, component selections for prototype implementation have been highlighted to clarify limitation of certain power devices in the proposed scheme and the operation of each stage has been verified by experiment in DC-DC conversion.

3. Modeling and Control of Parallel Power Processing (P3) scheme.

Small signal modeling of the pilot topology have been carried out to derive the control-to-input voltage transfer function, control-to-output current transfer function and current-to-voltage transfer function. Based on the model results, different control possibilities have been explored for output current control. A control system including an outer power decoupling capacitor voltage control and an inner current tracking control has been presented. An effective usage of one current controller for two plants have been studied and analyzed. Designs of both the current controller

and voltage controller have been presented. Finally, simulation results demonstrate the control effectiveness and the viability of the P3 scheme.

1.5 Thesis Organization

The remaining of the thesis is organized as follows:

Chapter 2 presents a literature survey on different microinverter topologies and control schemes.

Chapter 3 investigates a flyback inverter working in CCM mode rather than the commonly used DCM mode. The analysis and design guideline of the main stage for both DCM and CCM cases are discussed. Verified by both simulation and experiment, the proposed Flyback CCM inverter can obtain a California weighted efficiency of 88%, which is 8% higher than the counterpart of the flyback DCM inverter. On the other side, the power decoupling issue in this type of scheme is identified and analyzed in detail.

Chapter 4 is devoted to controller schemes to address the challenges in output current control of the flyback CCM inverter under a large varying operation conditions. An indirect current control approach is adopted and one linear controller (Average current control) and one nonlinear current controller (One cycle control) are designed and analyzed for AC module applications. The current tracking performances as well as stability are also verified by experiment.

In order to solve the power decoupling issue discussed in Chapter 3, chapter 5 develops a parallel power processing scheme based on flyback converter, which does not need a large DC link capacitance to perform power decoupling function. Different from single stage inverter and cascaded multi-stage inverter, this inverter reduces the power processing stages for the overall power, which helps increase the conversion efficiency as well.

In Chapter 6, small signal modeling of the proposed parallel power processing scheme has been carried out to explore various control possibilities. A dual loop voltage/current control has also been designed and developed for output current shaping control and decoupling capacitor voltage control. The effectiveness of the proposed current/voltage controller has been verified by simulation in both steady state and transient operation.

Chapter 7 summarizes the work presented in the thesis and suggests future work that may be carried out in this area.

CHAPTER 2: LITERATURE SURVEY OF MICROINVERTER TOPOLOGIES

2.1 Introduction

In this chapter, a literature survey of the different microinverter approaches is presented with the main focus on the power circuit topologies. The literature survey has been carried out to obtain an overview of existing solutions generated both in the academia and in the solar PV industry. The surveys present, briefly, the topologies and schemes, their pros and cons, and also identify the current trends and challenges with regard to them.

The survey is divided into two parts in this chapter. Firstly, the basic topologies of microinverters are classified and studied in Section 2.2. In addition, micoinverters with an additional active power decoupling circuit aimed at eliminating the electrolytic capacitor with its short lifetime has been studied separately in Section 2.3

These surveys provide the guidelines for the research work reported in the thesis from Chapter 3 onwards.

2.2 Literature Survey of Microinverter Topologies

A number of reviews about single-phase PV power inverter topologies have been published [1-4] in the past decade, and these provide good overviews of this area.

Among them, review [1] covers comprehensively the major aspects of PV inverters for single phase grid connection. The coverage is not limited to

microinverters only. Firstly, the technical demands due to the PV module, grid and the operator are identified. This is then followed by a historical review beginning from the central inverters of the past to the currently popular string/multi-string inverters and to the AC modules/AC cell inverters of the future. The inverter technologies are classified based on 1) the number of power processing stages in cascade, 2) the placement of the power decoupling capacitor, 3) whether galvanically isolated or non-isolated and if isolation is provided, whether it is with a line frequency transformer or with a high frequency transformer, and 4) the type of grid interface. These classifications are well defined and address the key questions in the design of a PV inverter. In total, seven topologies for microinverters and four for string /multi-string inverters are presented, compared and evaluated in terms of lifetime, component ratings and cost. A more detailed analysis can be found in [2]. Based on the comparison, a power processing scheme adopted by a commercial inverter "Soladin 120" [1], a push pull converter with a line frequency unfolding circuit, was identified as the "most suitable" candidate for a 160W microinverter [1]. The author of this review[1] has also published other reports earlier, including one reviewing four commercial microinverters [4] and another one covering inverters for multiple PV modules [3]. These reports could serve as additional references.

Another comprehensive review [39] is concentrated on microinverter only (which the article refers to as 'Module Integrated Converter (MIC)) of up to 500W power rating. Twenty topologies, all with High Frequency (HF) transformer isolation, are classified into three categories, i.e. MICs with a dc link, a pseudo dc link or

without a dc link. The topologies have been evaluated based on power density, efficiency, reliability and Balance of System (BOS) cost. In this study, the majority (13 out of 20) fall into the category of pseudo dc link type, which was judged to be the most suitable type for the current generation MICs. The third category without a dc link was believed to represent the future trend.

Reviews [40] and [30] are more focused on industry approaches. They discuss the key issues driving PV inverter development in the market with supporting studies, including price and efficiency studies. Both reviews briefly discuss the safety concerns of transformerless inverters due to the PV array not being grounded and point out a lack of international standard on this issue. This point will be further elaborated when discussing transformerless inverters later in the current literature survey as well. Review [40] further presents a number of transformerless topologies and new system concepts such as 'team' concept and 'master-slave' concept, wherein the energy output is increased.

Reviews [41] and [42] are more general in scope, including power processors for a variety of distributed power generation sources, such as PV modules, wind-turbine and fuel cells (the last included in [42] only).

It was noticed during this survey that the PV inverter technology has been changing rapidly with a variety of PV inverter topologies being proposed and investigated. It is quite difficult to provide an overview covering all of them. Therefore, in this survey, the scope is limited to topologies capable of converting a low PV voltage (say, below 40V) to an RMS (Root Mean Squared) grid voltage of up

to around 230V with a power rating between 100W and 300W. These input and output voltage ranges make sure that the studied topologies are all capable of (a) being used with a majority of the crystalline silicon based PV modules in the market and b) universal grid connection with grid RMS voltage value between 100V and 240V. The power rating should not be too low, considering the cost per watt for each PV module. At the higher end, the power rating is limited by the current PV module power ratings available in the market. The objective of this literature survey is to find out the current trends and challenges in microinverter research and development.

Based on the scope specified above, the first question for a microinverter designer would be how to provide the required high voltage amplification (up to 10~20). The required voltage amplification can be provided either with a transformer or without one. Thus, the topology candidates can be classified by the usage of transformers and by the transformer type as shown in Fig.2.1.

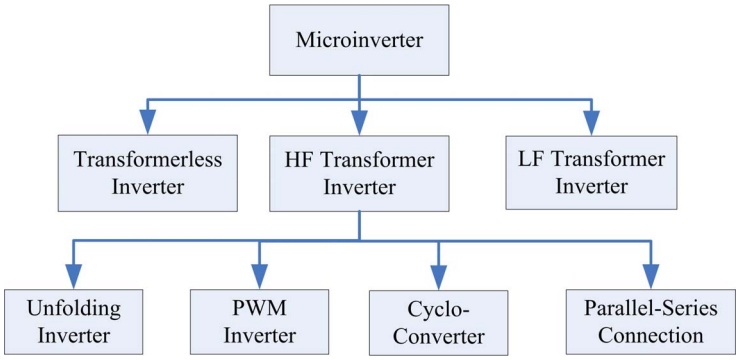


Fig.2.1: Classification of basic microinverters based on 1) usage and type of transformer and then 2) inverter operation mechanisms

As shown in Fig.2.1, the three major types of microinverter are transformerless (or non-isolated) inverters and isolated inverters using either a high frequency (HF) or a low frequency (LF) transformer.

In the past, an LF transformer (at 50 Hz or 60 Hz depending on AC frequency) was often used to provide galvanic isolation and voltage amplification, for example, the earlier commercial microinverter SUNSINE300 [3]. One benefit of this approach is the low voltage stress of the components at the primary side of the transformer [3, 30]. This allows cheap, low voltage MOSFETs with low conduction loss [3] to be used. Such MOSFETs are widely available due to their use in automotive applications [30]. However, such an approach is not favored nowadays because of the transformer's large volume, weight and most importantly cost. Although the LF transformer inverter is still considered for use in centralized/string PV inverters [43], it is no longer considered viable in low power applications, such as in a microinverter. Hence, they are not included in this survey.

The advancements in fast switching semiconductor power device technology and in low cost, high frequency magnetic materials have made HF transformer inverter more cost competitive than LF transformer inverter. A switching frequency at around 20 kHz ~ 200 kHz makes it possible to largely shrink the size and cost of the passive components, e.g. transformer. However, the pursuit of higher power densities through higher switching frequencies is limited by the increasing switching loss of the power semiconductor switches. Supported by soft-switching technologies, numerous new topologies with HF transformers are still being actively proposed and studied with the aim of improving the system efficiency further.

In non-microinverter type of PV inverters, such as a string inverter, it is believed that transformerless inverters generally have higher efficiencies and are also cheaper

than comparable inverters with transformer [40]. The main disadvantage of a transformerless inverter would be the direct connection between PV module and the grid without galvanic isolation, which could raise a safety issue [40]. In the case of a microinverter, it is still not clear whether a transformerless inverter can provide a higher efficiency. In order to meet the large voltage amplification ratio required in a microinverter, multiple power processing stages are usually needed, which increases component count and reduces efficiency. This issue will be further discussed in the next sub-section.

The remainder of the chapter is organized as follows. Firstly, a small group of studies based on transformerless inverters and the key issues in their use will be discussed in Section 2.2.1. After that, selected topologies using HF transformer will be further classified into four sub-groups and discussed individually in Section 2.2.2. The candidate topologies in these two sections are tabulated in Table 2.1. Finally, the focus of Section 2.2.3 would be on the challenges and trends observed in this area.

Table 2.1: Candidate topologies for micro-inverters

Transformerless	HF Transformer micro-inverter				
	UFI with power decoupling at		PWM Inverter	Cycloconverter	Series-parallel connection
	Input side	DC link			
[44-47]	[48-52]	[53]	[9, 54]	[55-57]	[58]

2.2.1. Transformerless Microinverter

Transformerless inverters have gained commercial popularity in grid connected PV systems, especially in Europe [59]. Compared to inverters with HF transformer, a transformerless inverter has certain advantages, such as system compactness, reduced

cost and reduction in overall power loss. In general, the European efficiency of a transformerless inverter is 1% to 3% higher than that of an inverter with HF transformer in the power range between 1 and 5kW [59].

Nevertheless, transformerless inverter has certain limitations. Traditionally, PV inverters in US require galvanic isolation between DC ground and AC ground to prevent transmitting DC faults to grid side [60]. Although this isolation requirement was removed from the National Electric Code (NEC) 690 published in 2005 [61], there is still a safety concern about the leakage current caused by the power conversion system via the distributed parasitic capacitance (shown as lumped capacitors C_{p+} and C_{p-} in Fig.2.2) between the PV connectors and grounded frame. This parasitic capacitance is influenced by weather conditions, module size and cell technology, and its net value has been observed to be around 50-150 nF/kWp for crystalline silicon cells and 1μF/kWp for thin-film cells[59]. The voltage fluctuation between the PV panel and frame ground depends on the inverter topology and switching operation. The fluctuation can be either at line frequency or at switching frequency or both [1] [59] [62]. To prevent the resulting leakage current from posing danger to a person who touches the PV module frames, new safety requirements have been specified in German DIN VDE 0126-1-1 and IEC6210. A Residual Current Monitoring Unit (RCMU) is required to detect DC fault when the leakage current to ground reaches 300mA and disconnect the PV arrays within 0.3s [59]. In order to meet the leakage current requirement, a variety of transformerless topologies have

been published [47, 59, 63-66] to prevent the fluctuation of PV panel voltage with reference to ground.

Another issue with transformerless inverter is related to DC current injection into the grid, which may saturate the power transformers [64]. As mentioned in Chapter 1, many international standards dealing with renewable energy interaction with grid, such as IEEE1547 and IEC61727, specify limits on allowable DC current injection, usually between 0.5% to 1% of the rated current [64].

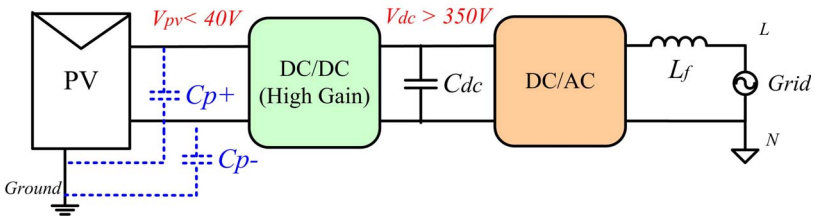


Fig.2.2: Possible System diagram of transformerless microinverter

In addition to the above issues common for PV string inverters and centralized inverters, one more challenge for use of transformerless inverter as microinverter is the high voltage gain requirement. Using a traditional single stage converter to achieve the high voltage gain (from < 40 V DC to > 350 V DC) is not practical. This is because the overall efficiency is reduced greatly at too small or too large duty ratios due to the presence of parasitic elements in the circuit [67]. Due to this, this approach was not considered in the present work.

However, in recent publications [11-13], a promising two stage transformerless approach has been proposed which appears to overcome the above problem of high gain amplification. This is a more recent development in this area, which is not studied in this thesis. However, it is described below for the sake of completeness.

The typical system diagram of the schemes proposed in [11-13] is illustrated in Fig.2.2. It consists of one front-end DC/DC converter with high voltage gain (as shown in Fig.2.3) and a high efficiency DC-AC inverter (for example, a H6 inverter in Fig.2.4).

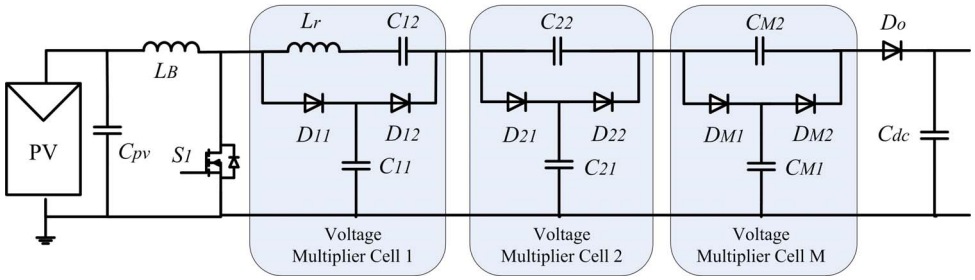


Fig.2.3: High gain boost converter with voltage multiplying cells [44, 45]

As illustrated in Fig.2.3, the front-end DC/DC converter in [44, 45] is based on either one or multiple voltage multiplying cells by placing some pre-charged capacitors in series connection. Detailed description of this boost converter with voltage multiplier cells can be found in [68] while this concept can be further applied for other converters as in [69].

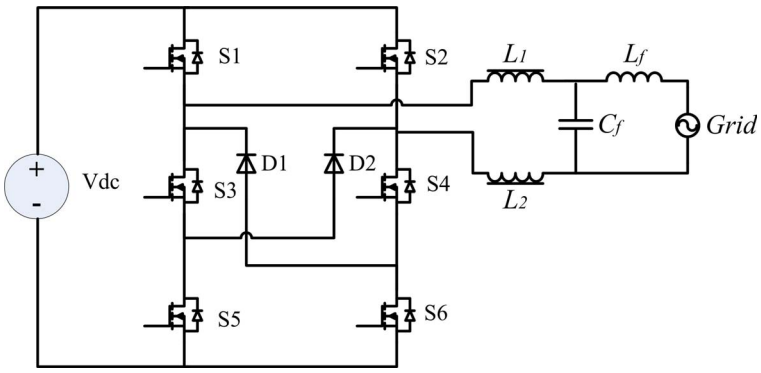


Fig.2.4: H6 type inverter proposed in [46]

The second stage in Fig. 2.2 is the DC/AC conversion stage, which is expected to be able to prevent a large leakage current between the PV module connector and ground. A variety of high efficiency single phase transformerless inverters listed in [47] can be adopted in this consideration, such as the H5 and the HERIC (Highly

Efficient and Reliable Inverter Concept) topologies, which are popularly used as transformerless string inverters. Falling in the same category, a high efficiency H6 type inverter was studied in [46] specifically for microinverter application.

Table 2.2: Summary of Candidate Topologies for Transformerless Microinverter

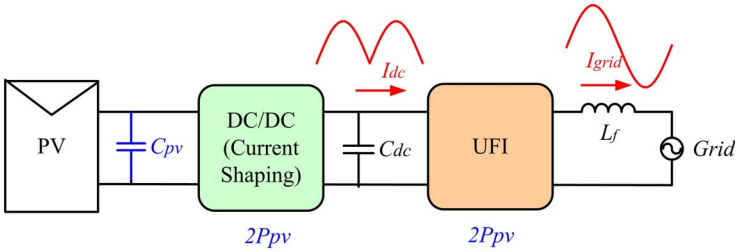
REF	Scheme	V_{pv}	P_{pv}	V_{dc}	V_{rms}	f_s	η
Candidate Topologies for Front-end DC/DC Converter							
[44]	1 voltage multiplier cell	35V	400W	350/450V	-	50kHz	94.3-96% /92.7- 95.4%
[45]	2 voltage multiplier cells	30V	300W	450V	-	75kHz	93.5-95.5%
A Candidate Topology for Second-stage DC/AC Inverter							
[46]	H6 type inverter	-	300W	180/200V	120V	30kHz	97.5-98.4%

Table 2.2 lists the key parameters of the candidate topologies of transformerless microinverter following the two stage approach. Combining the performance of the two individual stages, an overall efficiency around 93% could be achieved.

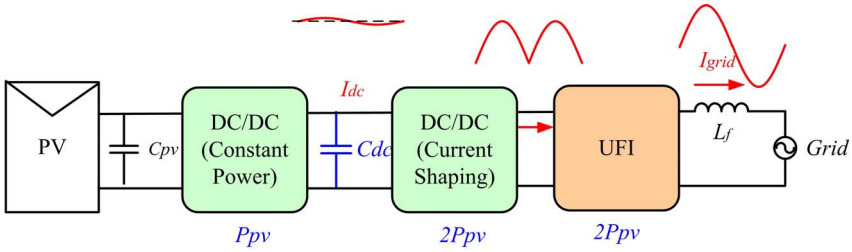
The relative advantages of such transformerless inverters proposed in [11-13] and inverters with HF transformers investigated in the present thesis need to be studied. Such a study could be considered for future research work.

2.2.2. Microinverter with HF transformer

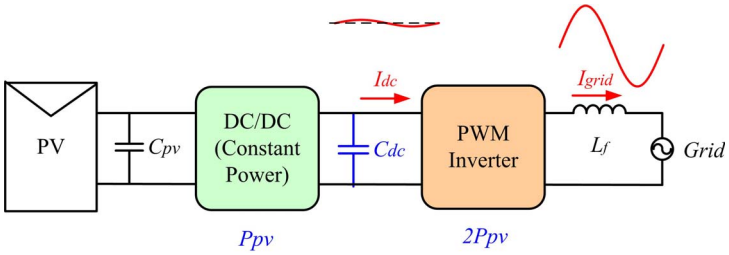
A microinverter with HF transformer isolation is by far the most popular type studied in academia and industry. The use of the transformer provides high gain capability and isolation. Besides, the size and cost of the transformer as well as other passive components used for filtering are also greatly reduced because of high frequency operation.



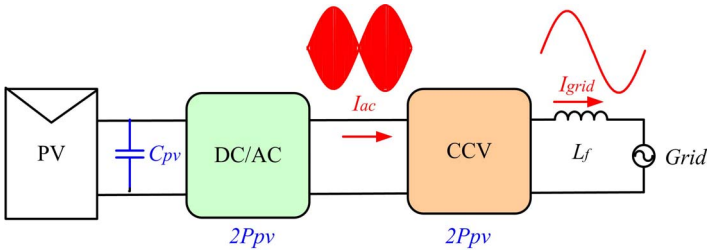
(a.1) Schemes with Unfolding Inverter (UFI) – Input side power decoupling



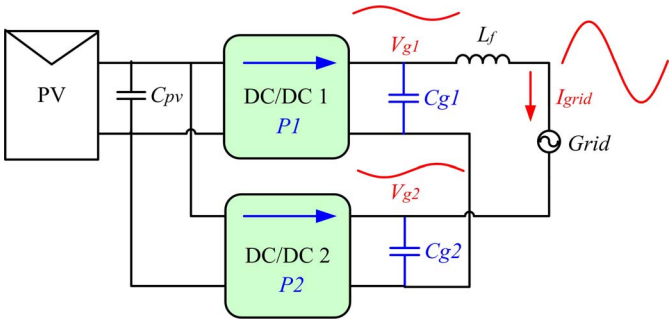
(a.2) Schemes with Unfolding Inverter (UFI) – DC link power decoupling



(b) Schemes with PWM inverter



(c) Schemes with Cycloconverter (CCV)



(d) Schemes using Parallel-Series Connection

Fig.2.5: System diagram of different types of HF transformer microinverters

As shown in Fig.2.1, microinverters with HF transformer can be further classified into four subgroups based on the basic mechanism used to generate AC from DC. These operating mechanisms for DC-AC conversion are illustrated in

Fig.2.5. In all of them, the HF transformer is usually placed inside the PV side converters marked in green color in Fig.2.5. The pros and cons of each subgroup will be first discussed. This will then be followed by a discussion of selected candidates within each category.

The first subgroup (Fig.2.5(a.1) and (a.2)) is characterized by the use of an Unfolding Inverter (UFI) working at line frequency to "unfold" the rectified sinusoidal current generated by the DC/DC current shaping converter into an alternating current. The scheme in Fig.2.5(a.1) uses one (or two) DC/DC power processing stages to boost the voltage level and implement MPPT and current shaping function at the input side. On the other hand, the scheme in Fig.2.5(a.2) uses an input side DC/DC stage to boost up the DC link voltage and perform MPPT for PV module. This is then followed by a DC/DC stage to perform current shaping function. In this scheme, the HF transformer isolation can be placed either in the DC/DC-constant power stage or in the DC/DC-current shaping stage.

The benefits of such approaches using UFI are several. Firstly, due to its low working frequency and zero voltage/zero current switching behavior, the switching loss of the UFI is negligible. As fast switching is not required for such line frequency commutated switches, selection of power semiconductor devices can be focused on devices with the lowest R_{on} (conduction on resistance) value available in the market. Due to this, the conduction loss determined by the RMS current through it is also small. If classified by conversion stages, this UFI stage is commonly not taken as an

extra stage for the same reason. Secondly, this scheme is similar to the Power Factor Correction (PFC) circuits commonly used in AC/DC offline power supplies, with the major difference being in the power flow direction. This similarity makes it possible to use the existing commercially available PFC IC's with slight modifications for the current shaping control.

However, in the scheme with input side power decoupling (Fig. 2.5(a.1)), the instantaneous power imbalance between the input DC (constant) power and the fluctuating output AC power is stored in the PV side capacitor C_{pv}. This requirement brings with it a number of drawbacks. One of them is the large decoupling capacitor required (usually in the range of mF) at the low voltage PV side. This is both because of 1) the large decoupling power (up to P_{pv}) at low frequency to be handled and 2) the low voltage ripple to be maintained at the PV panel terminals to ensure MPPT operation of PV module [1]. A third reason for using a high value capacitor highlighted in the present thesis (Section 3.3.2) is to keep the output current distortion factor low. This necessitates the use of an electrolytic capacitor (e-cap) with larger capacitance on the input side.

This use of an electrolytic capacitor is believed to be the main bottleneck in extending the lifetime of the inverter [1, 34, 53, 70]. Replacing the capacitor with other types of capacitor requires reducing the capacitance value by using an 'active power decoupling' circuit. This topic has been a major trend in current study of microinverter topology. The issue and existing solutions are surveyed in Section 2.3.

Besides the troublesome e-cap problem, the DC/DC stage needs to operate at an instantaneous pulsating power level ranging from $0\sim 2P_{pv}$ requiring the power devices to be overrated. The device utilization factor is reduced, which is not cost effective.

In schemes with an intermediate DC link capacitor (Fig.2.5(a.2)), since the power decoupling function can be realized at the high voltage DC link with a larger tolerance in voltage ripple, a film capacitor with a small capacitance value can be used. Such a capacitor does not have the lifetime problem of the electrolytic capacitor and hence the inverter lifetime can be improved [71]. However, this is achieved with one additional high frequency power conversion stage, which has a negative effect on the overall conversion efficiency.

An alternative to the UFI is the traditional PWM inverter operating at a high switching frequency. As shown in Fig.2.5 (b), this type of microinverter consists of one or more DC/DC converter stages for MPPT and voltage boost and a PWM inverter performing the current shaping and inverting function. Since the 2nd harmonic power is handled by the high voltage DC link capacitor C_{dc} rather than PV side capacitor C_{pv}, a large voltage ripple can be tolerated and a smaller film capacitor can be used. However, a major disadvantage is that due to the cascading of high switching frequency power processing stages, a multiplication of individual efficiencies would lead to less overall efficiency. Therefore, for this type of inverter, the key is to increase the efficiency of both stages.

A third subgroup of microinverter with HF transformer uses a cycloconverter (CCV) for direct AC/AC conversion. Proposed and patented by Hazeltine in 1926 (as cited in [72]), CCV was designed to "convert a constant voltage, constant frequency AC waveform into another AC waveform of a lower frequency by synthesizing the output waveform from segments of the AC supply without an intermediate DC link" [72]. As shown in Fig.2.5(c), schemes using CCV usually consists of a DC/AC stage generating high frequency AC voltage which is then stepped up through a HF transformer and fed to a CCV to obtain the low frequency power. In this scheme, as the current shaping is carried out by the DC/AC high frequency inverter, the second harmonic power is handled by the PV side capacitor, which has the same problems with the first subgroup using UFI.

The last subgroup is based on a parallel-series connection of DC/DC converters to implement the DC/AC conversion. As illustrated in Fig.2.5 (d), the input of the DC/DC converters are connected to the PV module in parallel, while the outputs are back-to-back series connected and placed in series with the grid. Each DC/DC converter produces a high level DC link voltage (> half of peak AC voltage) on which an AC voltage equal to half the grid voltage is superimposed. The back-back series connection of converters cancels the DC offset output while the two AC voltages add up.

The advantage of this scheme is that the decoupling power can be handled by the two high voltage capacitors C_{g1} and C_{g2} at the output side. One example for such a

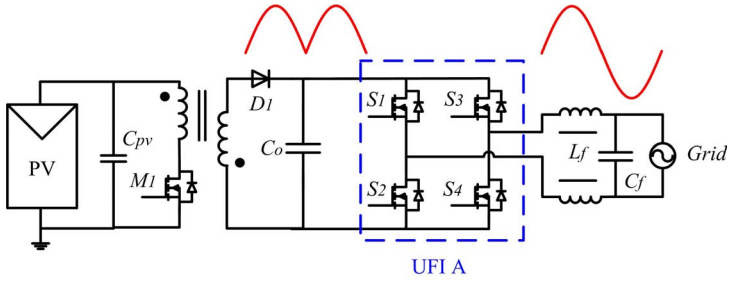
scheme has been proposed in [58] using flyback converters. However, in this approach, due to the series connection at grid side, the two DC/DC converters tend to provide additional power to each other alternately every half of the line cycle, which produces circulating current. This circulating current, will increase the power converter component ratings and also reduce the overall efficiency. Therefore, this scheme will not be considered further.

2.2.2.1. Schemes with Unfolding Inverter (UFI)

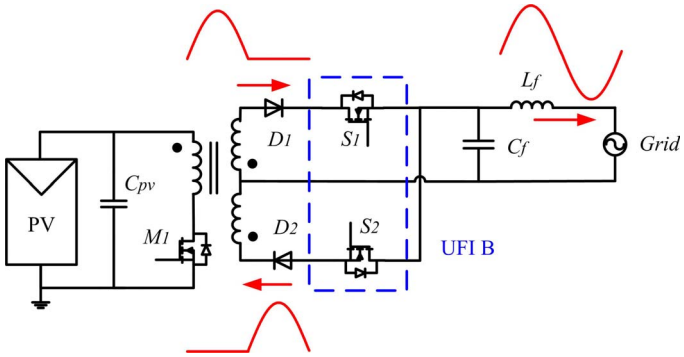
Unfolding inverter (UFI) [73, 74] refers to a low frequency inverter that unfolds the unidirectional current (but shaped like a rectified AC current) into alternating current. It can be implemented using either two or four low frequency switches. Examples of variations in UFI configurations are shown in the microinverter schemes based on a low cost flyback topology shown in Fig.2.6. These unfolding switches are highlighted by the dashed box, and can be implemented by power MOSFETs, IGBTs, or other switches.

The bridge type unfolding inverter (UFI A) shown in Fig.2.6 (a) is the most commonly used UFI topology. Although current/energy flow direction is reversed, this type of inverter is similar to the topologies used in a PFC application, where the current shaping is carried out by a DC/DC converter and the UFI is replaced by a diode bridge rectifier. The major differences compared to a PFC rectifier are that 1) the reverse power flow; 2) DC side specification/requirement and 3) the output

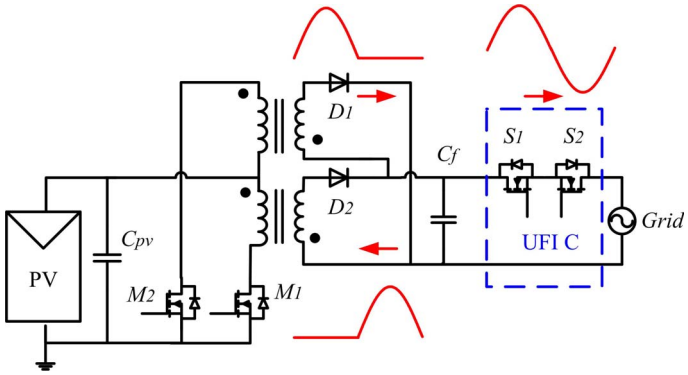
current of the converter, rather than input current needs to be controlled to follow the rectified grid voltage.



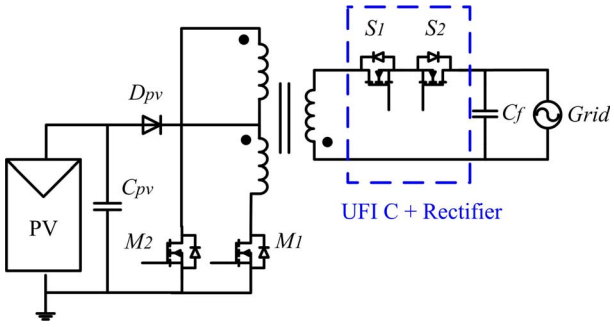
(a) 'Enphase' commercial microinverter scheme using flyback converter [48]



(b) Flyback converter with two output windings and unfolding switches [49, 50]



(c) Two flyback converters with unfolding switches [51]



(d) Flyback converters with two primary side winding and unfolding switches [51]

Fig.2.6: Examples of microinverter with different types of UFI

An overview of single phase PFC circuits can be found in [75] which could provide guideline for consideration in microinverter application. However, further investiagation on a particular PFC circuit is needed to evaluate whether it is applicable for microinverter application. Though popular, UFI A scheme requires four switches.

A second UFI configuration,- UFI B, is found in [49, 50] and shown in Fig.2.6 (b). Only two switches are required at the cost of two output legs of the flyback converter. Each leg would perform current shaping control during either the positive or the negative part of the AC cycle, while the unfolding switches S1 and S2 would be turned on and off alternately at line frequency to generate AC output current.

Another alternative is the UFI C shown in Fig.2.6 (c) with two back-to-back unfolding switches. The primary sides of the two flyback converters are connected in parallel, while the secondary sides are connected so as to handle output current in opposing directions.The scheme in Fig.2.6 (d) [51] is a special case and is worth mentioning. A pair of switches S1 and S2 is placed back to back on the output side, similar to the UFI C shown in Fig.2.6 (c). However, this switch pair S1 and S2 work as the combination of D1, S1 or D2, S2 in Fig.2.6 (b). In positive half cycle, S1 is on all the time while the body diode of S2 works as the rectifier for flyback operation. Similarly in the negative half cycle, S2 is on while the body diode of S1 works at high switching frequency as the rectifier diode. This approach, however, requires power devices of both S1 and S2 with a fast body diode. In [51], two external ultrafast diodes

are placed in parallel with S1 and S2 to avoid their slow body diodes to conduct. Besides, synchronous rectification is also one possible solution for fast rectification. Nowadays, a power device with intrinsic fast body diode is available in market such as Infineon's CoolMOS CFD2, which could make it possible to use the body diode itself as high switching frequency rectifier.

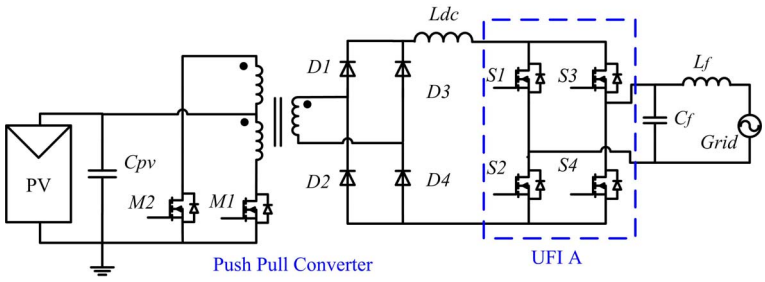
Overall, UFI A is the most popular UFI approach regardless of the power topologies while the use of other types is largely influenced by the power topologies of the front-end converters. The different topologies of the front-end converters are discussed in the following subsections.

1) Input side power decoupling

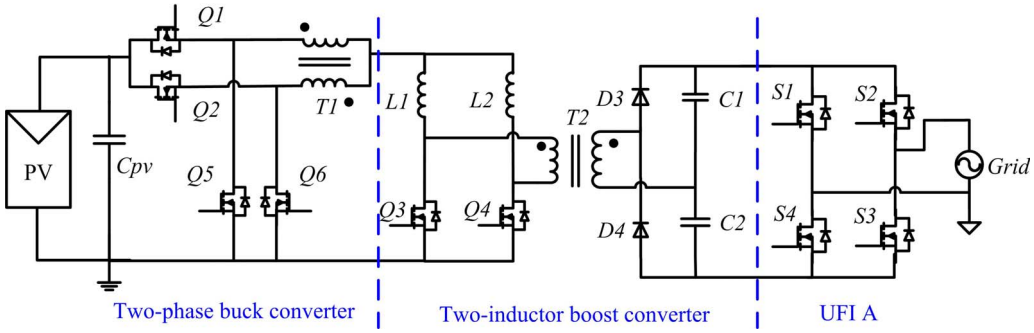
As discussed above, one or more DC/DC converter stages are used on the PV side to implement voltage boost and current shaping functions together. A number of commercial microinverters adopt the configuration in Fig.2.5(a.1) with different isolated DC/DC topologies. For example, Enphase microinverter [48] uses a flyback converter to perform current shaping (Fig.2.6 (a)), while Mastervolt microinverter "Soladin" uses a push pull converter [2] (Fig.2.7(a)) and NKF Electronics microinverter "OK4E" uses a full bridge converter [2].

Other DC/DC converters which have been used include series resonant full bridge converter [2, 76, 77] and two-transistor flyback converter [78]. Schemes which utilize two transistors in series on the PV side (for example, the two-transistor flyback converter in [41]) are not preferred due to the low voltage at the PV side. In this case,

the conduction power loss of the power switch, which accounts for a major part of the total loss, is doubled. Therefore, such topologies are not considered in this survey.



(a) Soladin 120 commercial microinverter using push pull converter [2]



(b) Topology proposed in [52] (lossless snubber circuit is not shown here)

Fig.2.7: Examples of schemes with UFI – Input side power decoupling

For input side power decoupling scheme with UFI, multiple DC/DC stages are usually not the first choice due to the added component count and reduced overall efficiency due to multiple power processing, while still retaining the poor lifetime issue due to the use of a large electrolytic capacitor for power decoupling. Yet, reference [52] provides an exception with a high overall efficiency reported (up to 92%). As illustrated in Fig.2.7 (b), this topology consists of one two-phase buck stage using Interphase Transformer (T1) with a turns ratio of 1:1, one two-inductor boost converter to step up the rectified sinusoidal voltage, followed by a UFI to generate AC voltage. The duty cycles of Q1, Q2 are modulated to generate rectified sinusoidal voltage. Efforts are taken to improve system efficiency using integrated magnetic

components, synchronous rectification, multi-phase operation, non-dissipative snubber circuit and SiC technology [52].

Overall, the schemes with UFI and input side power decoupling have potential as low cost and low loss solutions. But they require large values of input capacitance C_{pv}, which, as was discussed earlier, leads to short inverter lifetime. A compromise between cost and lifetime leads to the use of multiple-stage DC/DC converter with DC link power decoupling. This is discussed in the next subsection.

2) DC Link Power Decoupling

As shown in Fig.2.5 (a.2), at least two DC/DC conversion stages are needed for such a UFI based scheme, where the power decoupling is handled by DC link capacitor C_{dc} with a reduced capacitance due to high DC link voltage and large tolerance of voltage ripple.

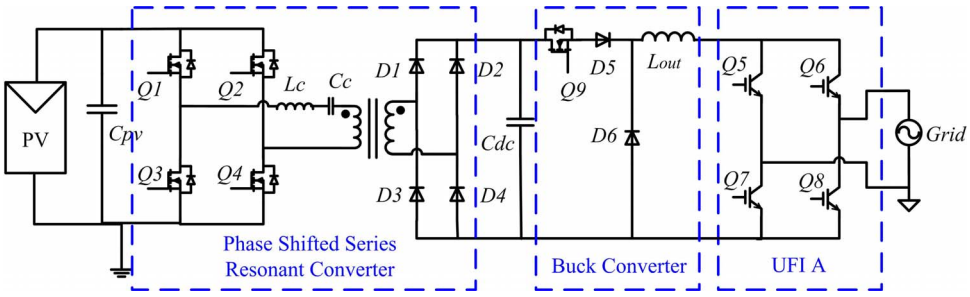


Fig.2.8: Example of multiple-stage microinverter with UFI [53]

A typical example can been found in [53], where the microinverter (Fig.2.8) consists of a transformer isolated phase shifted series resonant converter, a current shaper using a unidirectional buck converter and finally a UFI using IGBTs. The phase shifted series resonant converter works at 25kHz to step up the voltage to 475V.

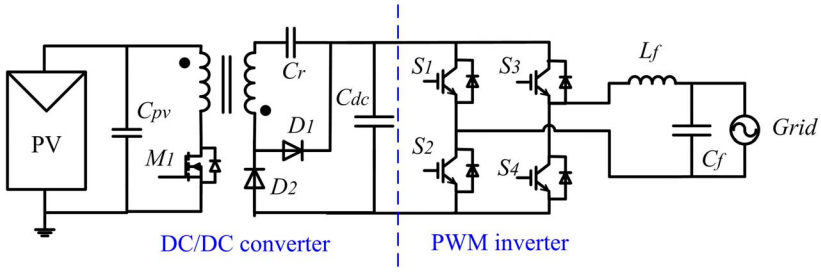
The objective of this reported work was to achieve long lifetime (10 years) with careful thermal management, components selection, failure rate study and reliability test. The maximum efficiency reported in [53] was 89%.

2.2.2.2. Schemes with PWM Inverter

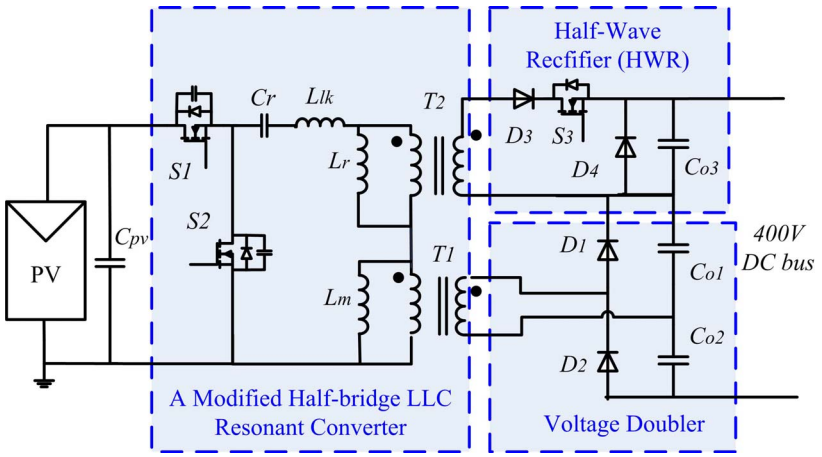
An alternative approach uses conventional Pulse Width Modulated inverter as the interface to the grid. In this approach, as the input voltage of PWM inverter is required to be higher than the maximum grid voltage, a front-end DC/DC converter is necessary to step up the low PV voltage to a high DC link voltage, e.g. above 400V. As illustrated in Fig.2.5 (b), since the front-end DC/DC converter works at constant power from PV while the PWM inverter delivers pulsating power to the AC grid. The power decoupling is handled by the intermediate DC link capacitor. In this respect, this is similar to the case in UFI approach with DC link power decoupling (Fig.2.5 (a.2)). The common disadvantage of such a cascaded scheme is the reduced system efficiency due to multiple processing of power in the cascaded stages. Therefore, in this subgroup, the research focus has been on high efficiency, high gain DC/DC converters and PWM inverters, respectively.

Reference [54] (see Fig. 2.9(a)) has proposed a potential low cost and high efficiency DC/DC converter by adding one diode (D1) and one capacitor (C_r) to a conventional flyback converter. The operation is based on an isolation transformer as a combination of normal transformer and flyback transformer at the same time. Thus, the energy transfer to the secondary side occurs both during the M1 ‘on’ interval and

'off' interval. Component utilization and efficiency can be improved with this approach. At a switching frequency of 50 KHz, an efficiency of 97% has been reported for the DC/DC converter at full power of 260W. The overall efficiency including both DC/DC converter and PWM inverter reaches up to 94.5%.



(a) Topology proposed in [54] with improved flyback DC/DC converter stage



(b) Dual-Mode Topology proposed in [9]

Fig.2.9: Examples of Schemes using PWM Inverters

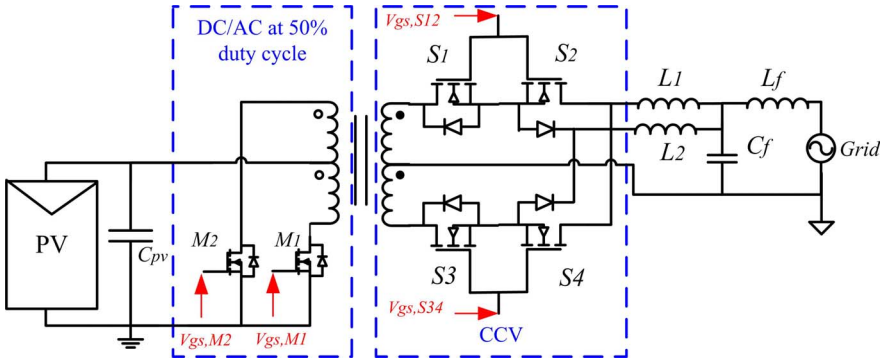
Another high efficiency candidate for the front-end DC/DC converter is a modified dual mode DC/DC converter based on a Half bridge LLC resonant converter with a voltage doubler and Half Wave Rectifier (HWR) as shown in Fig.2.9 (b) [9]. This converter is capable of maintaining a high efficiency for a wide input range under different load conditions by changing operating modes adaptively according to PV module voltage and power. As shown in Fig.2.9 (b), the Half-Wave Rectifier (HWR) connected to the secondary side of transformer T2 can be enabled and

disabled by controlling S3. When S3 is off, the DC/DC converter works in Mode I like a traditional LLC resonant converter together with a voltage doubler. In this mode, inductances L_r and L_{lk} together form the required resonant inductance. Switch S3 is turned on when the PV voltage and power fall below preset thresholds [9]. In this case, the DC/DC converter works in Mode II with HWR to aid in voltage boost and efficiency improvement at light load. A study of the DC gain and power losses have been presented in [9]. A peak efficiency of 96.5% and peak weighted efficiency of 95.8% have been reported with input PV voltage of 32V and output DC link voltage of 400V. Here the peak weighted efficiency refers to the maximum efficiency measured at different input PV voltage and weighted over varying power level. This topology, however, has a large component count. The control aspects have also not been discussed in [9].

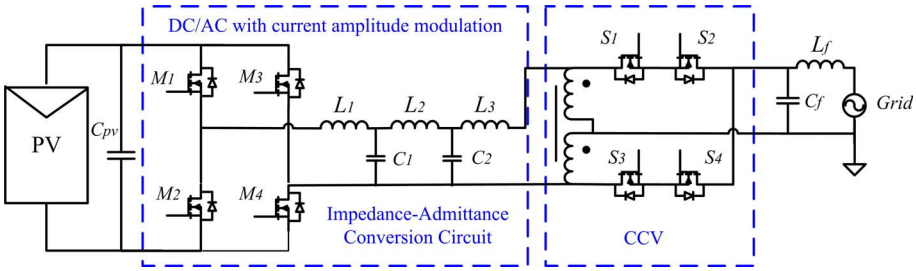
2.2.2.3. Schemes with Cyclo-converter (CCV)

As introduced earlier, CCV was designed to "convert a constant voltage, constant frequency AC waveform into another AC waveform of a lower frequency by synthesizing the output waveform from segments of the AC supply without an intermediate DC link" [72]. It has also found use in other applications such as in fuel cell systems [79, 80]. CCV is commonly used as a Voltage Source Inverter (VSI). Therefore, modification of the CCV to work as a Current Source Inverter (CSI) is required for grid-tied PV systems. Three candidate topologies, which can be used as CSI based on CCV, have been shortlisted below for target microinverter

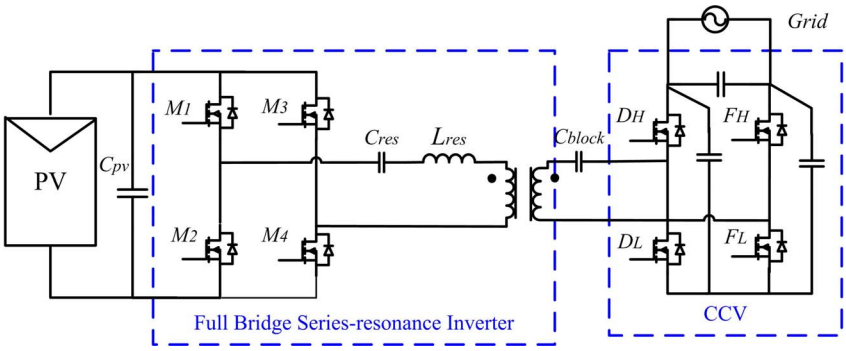
specifications and shown in Fig.2.10. Here, VSI and CSI are defined referring to the output characteristics of an inverter.



(a) Push-pull cyclo-converter inverter [55]



(b) CCV Scheme using Impedance-Admittance Conversion [56]



(c) A Full Bridge Series-Resonance Inverter with CCV [57]

Fig.2.10: Examples of schemes using CCV

Reference [55] proposed a microinverter topology based on a typical CCV (Fig.2.10 (a)). In this scheme, M1 and M2 at the transformer primary side are turned on and off alternatively at 50% duty cycles to generate a high frequency square voltage waveform. At the secondary side, S1/S2 and S3/S4 are controlled with a phase

shift between $V_{gs,M1}/V_{gs,M2}$ and $V_{gs,S12}/V_{gs,S34}$ to ensure unity power factor for grid current.

Reference [56] is based on a different CCV operation. As shown in Fig.2.10 (b), this scheme consists of three conversion stages. The first stage is a full bridge inverter, where the duty cycle of M1 to M4 is directly controlled to generate line frequency AC voltage superposed on high switching AC components. The second stage is an "Impedance-Admittance Conversion Circuit" to convert the modulated voltage into amplitude modulated current. The CCV converter as the third stage works to recover the line frequency AC current by removing the high switching carrier components from the modulated current waveform.

The third candidate [57] adopted a full bridge series-resonant inverter topology followed by four switches D_H, D_L, F_H and F_L. Four power control methods are discussed, including full-bridge phase shift control, cycloconverter phase modulation, frequency control and burst mode for light load conditions. A combination of four methods is adopted to improve the efficiency and a measured CEC efficiency of 95.9% is reported in [57]. However, in this work, DC/AC operation is tested using a manually adjusted DC voltage to simulate grid. The control aspect with regard to output current shaping to achieve unity power factor is not discussed.

Overall, cyclo-converter based inverters generally require more components. Besides, no efficiency results have been noticed for the first two examples. The challenges might be the fast-switching performance limited by the bidirectional

switch pair available. Besides, as the second harmonic power is handled at PV side capacitor, this type of inverter also suffers from issues related to use of electrolytic capacitor.

2.2.3. Major Trends in Microinverter Research

Based on the above study, three broad trends may be observed in the current microinverter research. They are motivated to provide an optimal solution to achieve low cost, high efficiency and long lifetime within a simple topology. These trends will be summarized and discussed in this section. Comparisons between schemes will be made based on published data.

2.2.3.1. Low Cost Solutions

The cost of a micro-inverter based system is generally believed to be higher than that of a system based on string inverters. Besides, for a large array of AC modules, additional monitoring and communication functions will usually become necessary and will add to the system cost. The plummeting cost of a solar panel (lowest around $1/Wp [28]) has made the inverter cost a more visible figure ($0.71 /Wp [29]) in the cost of a PV system.

Evaluation of cost on component level is impractical at prototype stage. As a compromise, a comparison of components counts [1, 39] in the power circuit (including power switches, capacitor and inductors) is commonly adopted to give some indication of cost.

A clear winner for low cost solution is based on flyback converter and UFI as shown in Fig.2.7 (a) and Fig.2.6. These flyback solutions are listed and compared in Table 2.3. Among these solutions, the scheme in Fig.2.6(a) seems to have the lowest component count with a promising maximum efficiency at low power.

Table 2.3: Comparisons of Potential Low Cost Flyback Solutions

Topologies	Ref	Input/Output Voltage [V]	Power Rating [W]	E-cap	Component Count				Switching Frequency [kHz]	Efficiency
					Switch	Diode	Magnetic core	Winding		
Fig.2.6 (a)	[48]	NA	NA	Yes	5	1	1	2	NA	NA
Fig.2.6 (b)	[49]	48/-	100	Yes	3	2	1	3	NA	96% max.
	[50]	50/220	200	Yes					40/variable	89%~97%
Fig.2.6 (c)	[51]	28-46/230	130	Yes	4	2	2	4	NA	84.8%
Fig.2.6 (d)	[51]	28-46/230	130	Yes	4	3	1	3	NA	84.1%

2.2.3.2. High Efficiency Technologies

For a PV inverter, a good maximum efficiency does not necessarily mean good system efficiency. Evaluation of PV inverter performance is usually based on an efficiency figure obtained weighting the efficiency at different power levels. This is due to the nature of PV power, which varies with varying irradiation. European efficiency [1] and California Energy Commission (CEC) efficiency [81] are two efficiency weighting criteria commonly adopted in PV related research work and by the PV industry. Their weighting factors are listed in Table 2.4.

Table 2.4: Weighting Factors for European Efficiency and CEC efficiency

Power Ratio	100%	75%	50%	30%	20%	10%	5%
Euro Efficiency	0.20	-	0.48	0.10	0.13	0.06	0.03
CEC Efficiency	0.05	0.53	0.21	0.12	0.05	0.04	-

The system efficiency not only depends on the topology and scheme, but also on the actual design, choice of components and current technologies. State-of-the-art

commercial microinverters are able to provide maximum efficiency and CEC efficiency up to 96.3% and 96.0% [82-85], respectively. However, with advancement in high efficiency transformerless topologies, the corresponding figures for string inverters and centralized inverters can be up to 98.7% and 98.5%, respectively [86, 87]. As pointed out in [88, 89], these efficiency data are also dependent on input voltage value and can be subject to up to 2% variation over a wide range of input voltage. It shows the need to increase the efficiency of microinverters in order not to place them at significant disadvantages in comparison with string inverters and centralized inverters.

Various research efforts and technologies have been taken to achieve a high weighted efficiency of a micro-inverter. These efforts include but is not limited to: soft switching techniques [31, 32, 36], interleaving or multiphase power converters, non-dissipative snubber circuits [52], and, lastly, light load efficiency improvement, such as burst mode operation [33, 90] or PFM (Pulse Frequency Modulation).

2.2.3.3. Long Lifetime

A major topic in current microinverter study is lifetime improvement. This is because, it is expected that the microinverter lifetime should match that of a PV module to reduce system maintenance and service cost. Nowadays, a PV module manufacturer usually offer a warranty of 25 years on 80% of initial efficiency [42]. However, it is difficult to achieve a lifetime of 25 years for a mircroinverter mainly because of the complexity of the system and the high temperature environment.

According to Arrhenius model [91], a system's lifetime is reduced by half if the temperature increases by 10 degrees Celsius. Since it is attached at the rear side of a PV module, a microinverter is exposed to harsh outdoor operating environment: temperature from -20^{o}C to 80^{o}C [92] and humidity levels from 0% to 100% with salty and corrosive conditions [53]. In order to protect against humidity and corrosion, the microinverter is generally completely sealed, which makes the internal temperature even higher than the environment temperature.

In order to improve the system lifetime, a common approach is to identify the major unreliable components in the systems and replace them with components capable of longer lifetime, if possible. Some suspected components include optocouplers, monolithic isolated DC/DC converters [53] and most noticeable of all, electrolytic capacitor. Thus, 'active power decoupling' (APD) schemes to avoid the use of an electrolytic capacitor across the PV panel is an area of investigation that has attracted vast attention. A literature survey of microinverters with Active Power Decoupling is presented separately in Section 2.3.

2.3 Literature Survey of Active Power Decoupling Schemes

As mentioned before, removal of electrolytic capacitor from microinverter is mainly driven by lifetime considerations and has attracted tremendous research interests in active power decoupling schemes.

Though generally it has been acknowledged that the PV terminal electrolytic capacitor is the weak link in achieving reliable microinverter performance [1, 34, 53, 93], some studies [94, 95] have claimed that microinverter long life can be realized in

spite of using electrolytic capacitor. By keeping the core temperature of the capacitor below 70oC through proper thermal design, it is claimed that the present electrolytic capacitor technology, with a typical continuous lifetime of 8000hrs at 105oC, can indeed operate in the field for 30 years. Another study on temperature environment of microinverter [92] shows that the backside temperature of the solar panel varies around -20~80oC for over 15 years and is below 60 oC for 95% of the time. Thus, it may be possible to achieve extended lifetimes using electrolytic capacitor at the cost of implementing proper thermal management. This claim needs further study and verification, including field tests.

Another reason against the use of electrolytic capacitor is its poor capability to handle a large ripple current due to its intrinsic high Equivalent Series Resistance (ESR). As a result, a large, oversized capacitor bank with a total capacitance value much larger than that required if the high frequency ripple current were not present, will be required. Besides, the high ambient temperature and heat generated by the large current ripple also accelerate the degradation mechanisms in the capacitor, leading to an increase in ESR over the operating life of a capacitor [96]. Consideration of such lifetime ESR degradation requires further over sizing of the electrolytic capacitor, which adds to the system cost as well.

Therefore, ways to substitute the electrolytic capacitors with other more reliable capacitors are actively pursued by microinverter manufacturers [84] and supported by capacitor manufacturers [71]. The first choice for such a substitution at high DC link voltage is a film capacitor, which offers two times higher voltage rating, three times

the ripple current capacity than electrolytic capacitor[71]. However, a limited capacitance per volume of film capacitor technology makes a direct replacement with the same capacitance impractical. Various research efforts have been taken on circuit level to reduce the capacitance required for power decoupling [35, 37, 38, 70, 97, 98], either by adding active power devices in the power circuit or by using additional control methods. These solutions are referred to as Active Power Decoupling (APD) and are surveyed in this section. A review of twelve power decoupling schemes may be found in [97]. It is worth mentioning that although power decoupling using inductor rather than capacitor is also possible with superior reliability, it is not favored as it is a bulky and heavy solution with a high power loss. Some studies related to inductive power decoupling may be found in [99, 100].

The remaining part of Section 2.3 is focused on capacitive power decoupling methods and is organized as follows. Firstly, the power decoupling requirement for single-phase PV inverters (including microinverter) is introduced to provide the necessary background. After that, the active power decoupling solutions are classified into two groups based on whether a DC link capacitor or an AC link capacitor is used. The underlying principle and selected topologies for each group will be presented, with the main focus on circuit operation of the power decoupling part. Finally, these solutions are compared in terms of decoupling capacitance and efficiency at specific operating conditions such as power level, the DC link voltage & voltage ripple.

2.3.1. Power Decoupling Requirement

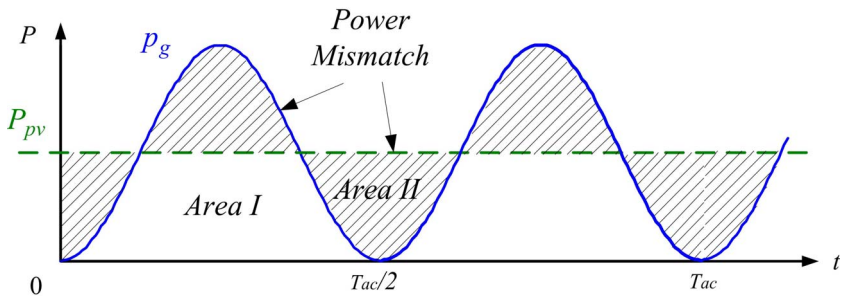


Fig.2.11: Power decoupling requirement for single phase DC/AC inverter (P_{pv} : DC power from PV module; P_g : switching average value of AC power to the grid)

Fig.2.11 illustrates the instantaneous input and output power of a single phase inverter ignoring the high switching frequency ripple. It is necessary that the power mismatch between the constant input power and the pulsating output power be compensated by energy storage elements in the inverter. This is the so called 'power decoupling' requirement to be taken care of in all single-phase inverters.

The size of a decoupling capacitor to handle this power mismatch and can be expressed as [1, 101]:

$$C_{dc} = \frac{P_{pv}}{2\pi f_{ac} \cdot V_C \cdot 2\Delta V_C} \tag{2-1}$$

Equation (2-1) links the power decoupling capacitance C_{dc} required for a given PV power level P_{pv} to the capacitor average voltage V_C and the allowable ripple amplitude ΔV_C. Here, $f_{ac} = 1/T_{ac}$ refers to the line frequency.

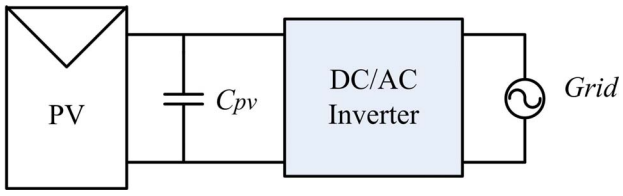


Fig.2. 12: Power Decoupling at PV side

As shown in Fig.2. 12, if the power decoupling capacitor is placed at the PV side, both the values of V_C and ΔV_C are limited by the PV module requirement. As mentioned earlier in Section 1.2.1, the majority of PV modules are based on crystalline silicon technology, and typical MPP voltages are below 40V. In addition, keeping the voltage ripple at the PV module side small is crucial to ensuring a high static MPPT efficiency.

In [1, 2], a measure called the 'utilization ratio' has been defined as the average generated PV power divided by the theoretical MPP power. The relationship between PV module voltage ripple and the utilization ratio has been calculated in [1, 2] using a second-order Taylor approximation. The results indicate that the allowable voltage ripple amplitude should be less than 6% of MPP voltage to ensure operation above 99% of MPP, and less than 8.5% of MPP voltage to ensure operation above 98% of MPP. For example, a PV module with an MPPT voltage of 30V should not allow voltage ripple amplitude above 2.55V, in order to guarantee 98% of maximum power from PV module. In this case, a capacitance of 5.4mF is required for a 200W PV module and a 50Hz system (refer to (2-1)). Such a high capacitance is only feasible with electrolytic capacitor. However, the published studies on selection of the electrolytic capacitor do not consider the requirement from output power quality point of view. This turns out to be a more stringent requirement and is studied in Section 3.3.2 of this report.

In order to reduce the capacitance required for power decoupling to tens of microfarad range, one basic idea is to increase the average capacitor voltage V_C and

the allowable voltage ripple amplitude ΔV_C. In order to achieve this, the power decoupling function is shifted away from the capacitor across the PV panel. A high DC link voltage with a DC link capacitor carries out the power decoupling. Almost all of the reported APD schemes follow this approach.

For comparison of different APD schemes, a 'Capacitance per watt' figure can be obtained from (2-1):

$$\frac{C_{dc}}{P_{pv}} = \frac{1}{4\pi f_{ac} \cdot V_C \cdot \Delta V_C}. \tag{2-2}$$

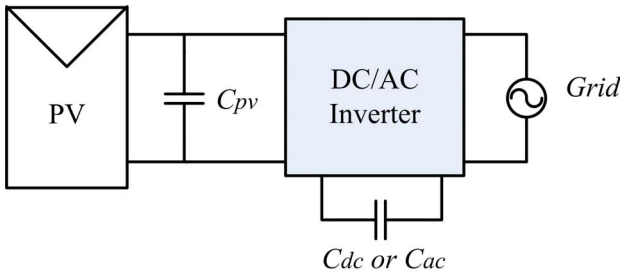


Fig.2.13: System Diagram for APD solutions

It is worth mentioning that, in principle, the cascaded schemes with high voltage DC link in Fig.2.5 (a.2) and (b) can also be taken as an APD scheme as the high voltage DC link capacitor can be implemented by a low capacitance film capacitor with power decoupling control.

A less popular approach, based on an AC link capacitor, has been published in [101, 102] and patented [103]. Here, the decoupling AC capacitor is exposed to bidirectional voltage. According to [103], for a grid voltage in the form of $\sin(2\pi f_{ac} t)$ and a unity output power factor, the decoupling capacitor voltage is given by:

$$V_C(t) = \Delta V_C \cdot \cos\left(2\pi f_{ac} t - \frac{\pi}{4}\right), \tag{2-3}$$

where ΔV_C refers to the voltage amplitude.

In this approach, the capacitance per watt value is given by:

$$\frac{C_{ac}}{P_{pv}} = \frac{1}{\pi \cdot f_{ac} \cdot \Delta V_C^{\,2}} \tag{2-4}$$

Reduction of capacitance requirement can be achieved by increasing the voltage amplitude ΔV_C of the AC link capacitor.

The examples of different APD schemes using DC link and AC link capacitor are tabulated in Table 2.5 and discussed in Section 2.3.2 and 2.3.3, respectively.

Table 2.5: Examples of APD schemes

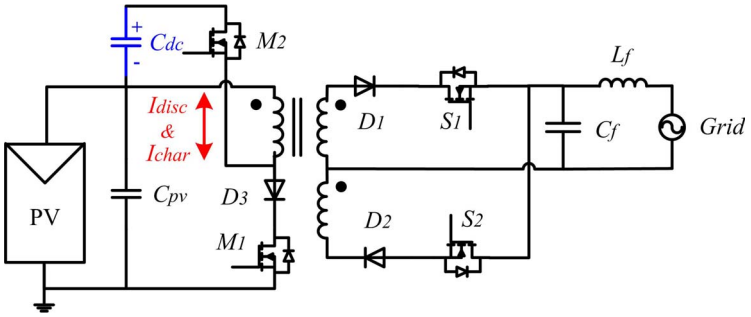
APD using DC link capacitor			APD using AC link capacitor
Flyback Inverter	Push-pull converter	Parallel Active Filter	
[34-37]	[93]	[35, 70, 98, 104]	[101, 102]

2.3.2. APD solutions using DC link Capacitor

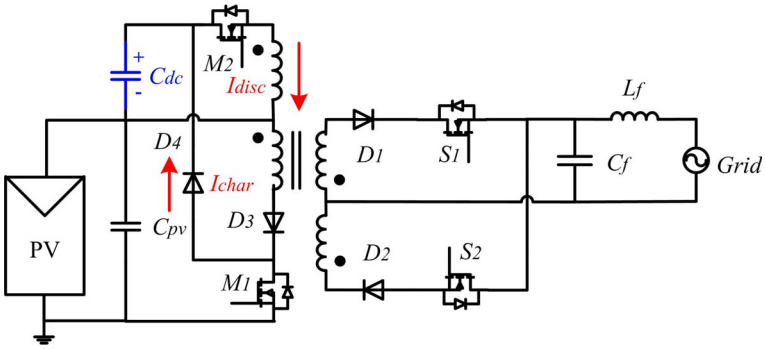
This section concentrates on the topology aspects of different APD implementations using a DC link capacitor. As mentioned earlier, cascaded schemes shown in Fig.2.5 (a.2) and (b) also may be viewed as active power decoupling scheme since the second harmonics capacitor is separated from the PV panel capacitor. The other approaches for the APD will be discussed here.

As mentioned in Section 2.2.2.1, a flyback converter with UFI is a potential low cost microinverter solution but suffers from the poor lifetime due to the power decoupling being done at PV side. Various research efforts have been spent on this topology to include APD without degrading the system efficiency [34-37]. These schemes will be discussed first. Another APD solution has been proposed for a

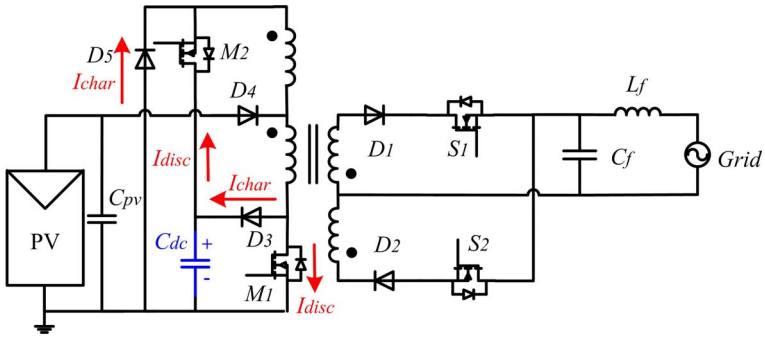
push-pull converter with UFI in [93]. Lastly, parallel active filter schemes, which may be applied to a variety of topologies [35, 70, 98, 104], are surveyed.



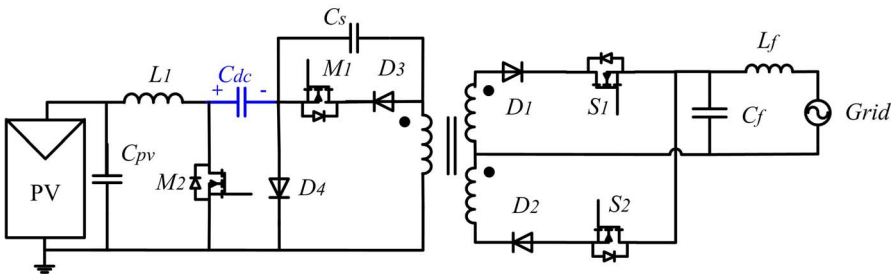
(a) Sequential Magnetizing Modulation (SMM) Scheme [34]



(b) Time-sharing Magnetizing Modulation (TMM) Scheme [35]



(c) A three-port flyback with APD [37]



(d) A soft-switching flyback converter with APD [36]

Fig.2.14: APD proposals for Flyback converter with UFI in Fig.2.7 (b)

Fig.2.14 shows four different APD proposals for one popular microinverter based on a flyback inverter with UFI. The decoupling capacitors have been marked as C_{dc} with polarity indicated.

The Sequential Magnetizing Modulation (SMM) scheme shown in Fig.2.14 (a) actually works as a buck-boost converter (between PV module and DC link capacitor) in series with a flyback inverter (between DC link capacitor and grid). In this case, the magnetizing inductance of the flyback transformer works as the buck-boost inductor with magnetic flux in one polarity to charge the decoupling capacitor first. After the charge current I_{char} reduces to zero, the magnetizing current of the flyback transformer will continue to flow in the opposite direction to discharge the decoupling capacitor to provide unity power factor for grid connection. It was reported in [35] that due to the sequential operation of the two converters within one switching cycle, a small pulse width and large current spike result in a poor efficiency (63%). Another important contributing factor for such a low efficiency could be that all the PV power goes through a two stage power conversion at high switching frequency. The same approach has been applied for a dual-switch flyback microinverter in [105] with a much higher efficiency of up to 86.7%.

In an effort to improve the system efficiency with APD, [35] proposed a Time-sharing Magnetizing Modulation (TMM) Scheme in Fig.2.14 (b). The principal idea is that only the mismatched power (shaded area in Fig.2.11) needs to pass through APD circuit, while the remaining power (unshaded area in Fig.2.11) goes by its original single stage topology. In this way, a 10% efficiency improvement was

achieved compared to SMM scheme in [35]. Besides, charging and discharging of the decoupling capacitor are separated as marked in Fig.2.14 (b). However, the overall efficiency is still low (73%).

Fig.2.14 (c) shows an alternative APD proposed in [37] following the same principal idea given in [35] but with a different circuit implementation. In this scheme, the two unfolding switches S1 and S2 would also participate in high switching modulation during alternative half AC cycles. Charging of decoupling capacitor C_{dc} is like this: assume in positive half cycle, when M1 is turned off, as S1 is not turned on, the magnetizing current of the flyback transformer will continue to flow through a closed loop formed by D3 , D5 and two center tapped transformer windings to charge C_{dc}. After that, S1 is controlled to be on to transfer required power to grid. Similarly, discharging current of C_{dc} flows through a closed loop formed by M1, M2 and two center tapped transformer windings when M1 is on and S1 off in positive half cycle. The highlight of this scheme is an innovative usage of the center tapped primary windings of flyback transformer. By a magnetic coupling between the two primary windings, the power decoupling current to charge and discharge C_{dc} is half of the original current in flyback operation. A lower current in power decoupling circuit, could be the reason for a good efficiency (88% ~ 91.5%) reported in [37].

The three schemes discussed above all utilize the flyback transformer for diverting the decoupled power, basically using buck-boost circuit for power decoupling. The efficiency of a buck-boost circuit is not high as all the energy must be stored in the inductor first and then transferred to the load. A fourth scheme [36] in

Fig.2.14 (d), uses a boost converter instead, which could potentially improve the system efficiency. The circuit operation is straightforward. At the PV side, M2, L1 and D4 works as a boost converter between PV module and DC link capacitor C_{dc}. At the grid side, a dual-switch flyback inverter consists of M1, M2, D3, flyback transformer as well as the secondary side circuits and gets power directly from C_{dc}. Modulation of M1 and M2 are synchronized to ensure a simple control. An efficiency of 85.3% has been reported in [36] with soft-switching technique adopted.

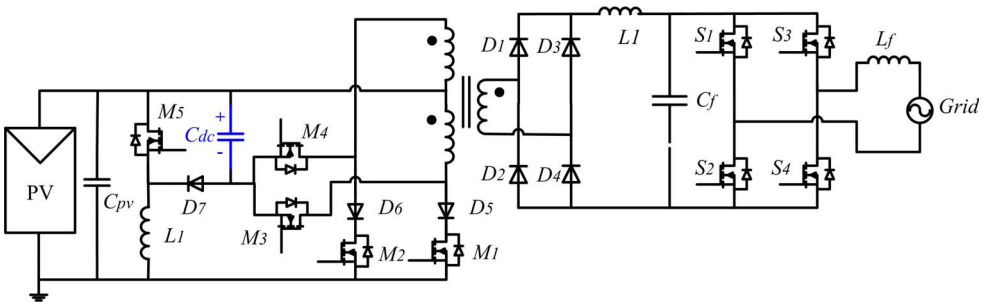
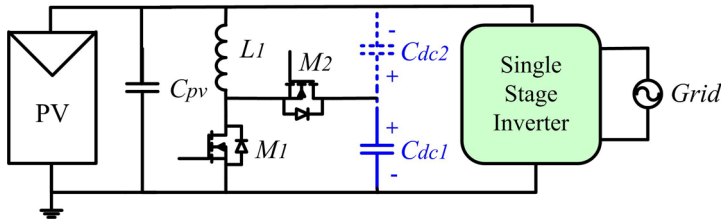


Fig.2.15: Power decoupling scheme [93] for push pull microinverter in Fig.2.7 (b)

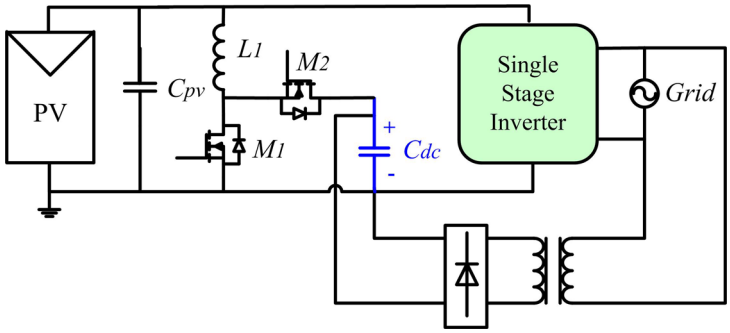
An APD based on a push pull microinverter with a high reported efficiency of up to 94% was proposed in [93] and updated in [38]. The principal idea is to charge extra power from PV module to the decoupling capacitor C_{dc} through a boost converter including M5, D7 and L1 when the instantaneous input power is higher than output power. When the input power is less than the output power, C_{dc} will provide the required decoupled power through another push pull stage formed by M_3 and M_4 at the primary side of the push pull inverter.

Other than the APD modified for a specific type of inverter, parallel active filter scheme at low voltage PV side [35, 70, 104] can be applied for any inverter. As illustrated in Fig.2.16 (a), either a bidirectional boost converter [70, 104] with

decoupling capacitor C_{dc1} or a bidirectional buck-boost converter[35] with decoupling capacitor C_{dc2} can be used.



(a) PAF schemes [35, 70, 104]



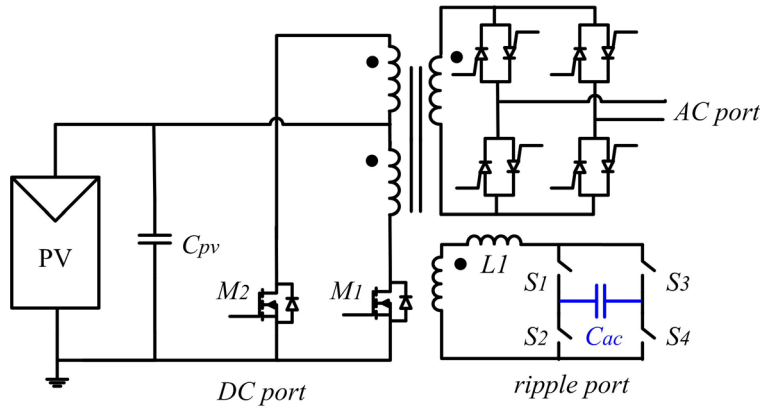
(b) Enhanced configuration of PAF [98]

Fig.2.16: Parallel Active Filter at PV side

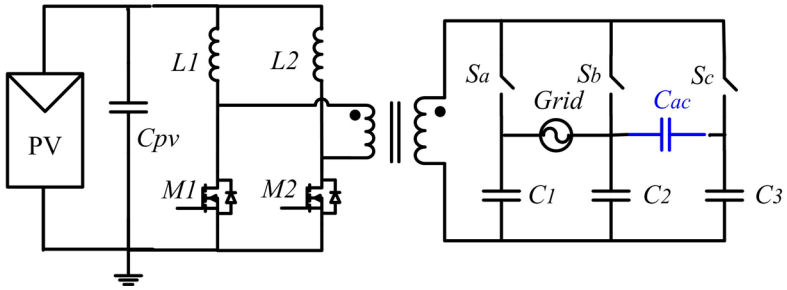
When the output voltage, i.e. the power decoupling capacitor voltage drops to near input voltage, the reverse buck operation of the bidirectional circuit would be affected, which leads to instability of input voltage. In order to prevent this instability, there has been an attempt to restore the capacitor voltage from the grid supply [98]. However, the charging of the power decoupling capacitor is realized at the cost of a distorted net grid current, which consists of the normal operating sinusoidal output current and a capacitor charging current. To address this issue, another effort has been made in [70] by using a new control method called “Virtual Capacitance Method” to restrict the power decoupling capacitor voltage automatically within the desired range. In this case, instead of keeping the input voltage constant, it is allowed to vary with the output voltage (i.e. decoupling capacitor voltage). Therefore, when the output

voltage drops to a critical point, the input voltage follows in a way so that the DC/DC converter is still within its operating range. Reference [70] reports that the proposed Parallel Active Filter circuit was tested with commercial 'Sunny Boy' string inverter and a slight efficiency improvement around 0.2% has been observed. The losses generated by the decoupling circuit are partly compensated by the lower leakage and better ESR in the film capacitor as well as better MPPT efficiency with smaller ripple on the input port. However, this result is achieved with a string inverter with a high input voltage and hence not valid for microinverter with input voltage below 40V.

2.3.3. APD solutions using AC link Capacitor



(a) Topology with ripple port for minimum decoupling capacitance [101]



(b) High frequency link converter with constant power output from PV module[102]

Fig.2.17: Power decoupling using AC link capacitor

For power decoupling with a DC link capacitor, a high DC average voltage V_C is needed to ensure an energy reservoir of $\frac{1}{2}CV_C^2$, which is much larger than the

energy required for power decoupling (i.e. $\frac{1}{2}CV_{C,\max}^2 - \frac{1}{2}CV_{C,\min}^2$). However, for an AC link capacitor, a high DC average voltage is not present and a small decoupling capacitance can be used at a large capacitor voltage ripple.

The basic operation for AC link power decoupling is given by (2-3). As long as the capacitor voltage follows the sinusoidal waveform of AC grid or rectified sinusoidal waveform [101] with a phase shift of π/4, the power decoupling is achieved automatically with desired output current with unity power factor.

Fig.2.17 (a) illustrates a three-port converter using an AC link capacitor [101]. This circuit consists of a voltage–source push-pull interface at DC port, a thyristor bridge at AC port and another bridge circuit at ripple port for the second harmonic power. The detailed operation of the whole system is not provided in [101]. It is surmised that the push pull converter generates a square waveform across the transformer, while the bidirectional bipolar switch pairs at AC port work as a cyclo-converter. The AC port current can be controlled indirectly by controlling the decoupling capacitor voltage, which simplifies the control complexity. The decoupling capacitor at ripple port can also use a DC capacitor with rectified AC voltage by modifying the control of the four switches at ripple port.

Alternatively, another solution shown in Fig.2.17 (b) placed an AC capacitor at grid side, without introduction of additional winding on transformer [102]. In this scheme, the primary side of the transformer works in constant power mode, whereas the duty cycle of three bidirectional switch pairs S_a, S_b and S_c are controlled to ensure volt-sec balance of the transformer and to generate the desired output current at

each leg. Here, capacitor C1~C3 work at high frequency only while the AC link capacitor C_{ac} is with an AC voltage at line frequency.

2.3.4. Discussion of the APD Schemes

Table 2.6: Comparison of APD schemes (at line frequency of 50Hz unless otherwise stated)

FIG	REF	*Vpv/Vrms*	*Ppv*	***Vc***	*ΔVc*	*fs*	*C*	*C/Ppv*	*η*	***PAPD***
		[V]	[W]	**[V]**	[V]	[kHz]	[μF]	[nF/W]	[%]	
APD using DC link capacitor										
Fig.2.14 (a)	[34] [35]	35/100	100	**100**	-	20	50	500	63	**All**
Fig.2.14 (b)	[35]	35/100	100	**100**	35	20	44	440	73	**Partial**
Fig.2.14 (c)	[37]	60/110	100	**150**	20	50	50	500	88~91.5	**Partial**
Fig.2.14 (d)	[36]	30/100	500	**250**	40	20	50	100	~85.3	**Partial**
Fig.2.15	[93]	130/	500	**165**	25-	20	50	100	-	**Partial**
Fig.2.16 (a)	[104]	33.6/220	70	**45**	5	-	500	7100	NA	**Partial**
APD using AC link capacitor										
Fig.2.17 (a)	[101]	/120@60 Hz	100	**NA**	400	-	3.3	33	NA	-
Fig.2.17 (b)	[102]	-/240	212	**NA**	300	10	5.53	26	-NA	-

The different APD schemes discussed above have been tabulated in Table 2.6 based on the corresponding working conditions (such as input and output voltage, power level), key parameters related to power decoupling capacitor (such as V_C and ΔV_C) and performance index (i.e. capacitance per. Watt and efficiency η). The last column indicates the power handled by the APD circuit. If all the DC input power is transferred through the APD circuit, it is marked as "Full". Otherwise, if only the difference between input and output power is converted through the APD circuit such as in [35], it is marked as "Partial". It is noted that partial power process through APD circuit has higher efficiency as shown in Table 2.6.

It is also noticed that the DC link capacitor is usually added to the UFI type inverter with an intermediate average voltage level of 100~250V and a small voltage ripple below 40V as shown in Table 2.6. As a result, a decoupling capacitance per

watt is relatively higher, e.g. around 0.5μF/W. Most of the APD schemes studied are in the power level of 100W with a low grid voltage (100Vrms) and a relatively low switching frequency of 20 kHz.

Besides,, the APD circuits are commonly added at low voltage PV side, which requires power processing at higher current level and hence more power loss. Therefore, it is possible to improve the efficiency of APD scheme by reducing the power processed by the APD circuit and by placing the APD circuit at the high voltage, low current side. Based on this idea, a parallel power processing scheme is proposed and this approach will be investigated in Chapter 5 and chapter 6.

It is also noticed that APD using AC link capacitor is applicable for schemes with either cyclo-converter or PWM inverter. A clear advantage of this method is a low decoupling capacitance needed, e.g. around 30nF/W as shown in Table 2.6 due to a large voltage ripple above 300V. In addition, the power decoupling control and current shaping control can be simplified by using a voltage control of the decoupling capacitor assuming a constant DC power is generated from PV module. However, the schemes require more components as shown in Fig.2.17. The justification for using AC link power decoupling scheme needs to be based on its efficiency performance, which could be one topic to study in the future.

2.4 Conclusions

In this chapter, a detailed literature survey on the existing microinverter topologies has been presented with three trends identified. Another literature survey

on active power decoupling schemes for improving inverter lifetimes reported for microinverter has also been included in Section 2.3.

Based on the literature survey on the microinverter topologies and current trends, it may be concluded that a single stage flyback inverter using UFI, is a promising candidate as a low cost solution. There is a need to increase the conversion efficiency without adding to system complexity. To address this aspect, Chapters 3 and 4 will work on the same flyback inverter topology but with a redesigned flyback transformer and a different operating mode, which will be able to improve the system efficiency considerably.

Based on literature survey on the power decoupling schemes, it has been noticed that the published APDs usually works on intermediate voltage level, which requires more current handling capability and higher decoupling capacitance. There is a need to increase the decoupling capacitor average voltage and voltage ripple further to reduce the capacitance as well as the potential power loss. Accordingly, Chapter 5 and 6 work on a parallel APD scheme which is able to place the decoupling capacitor at the high voltage side, with the aim to achieve a low capacitance and low loss on APD circuit.

CHAPTER 3: AN IMPROVED SINGLE STAGE SCHEME: A FLYBACK-CCM INVERTER

3.1 Introduction

Favored by its simplicity and potential low cost, a single stage inverter based on flyback topology is selected as a starting point for low cost AC module application. In this Chapter, the flyback inverter is designed for operation in continuous conduction mode (CCM) instead of in discontinuous conduction mode (DCM) [31, 32, 48, 49] or boundary conduction mode (BCM) [50, 106]. The design guidelines for the proposed CCM scheme and the benchmark DCM scheme are provided respectively. Besides, the requirements of input capacitors for single stage inverter, based on power decoupling, output power factor and filtering of the switching ripple are also discussed and analyzed. Both the proposed CCM scheme and a DCM benchmark scheme are designed and verified by simulation and experiment.

3.2 Overview – A Popular Flyback Inverter

As mentioned in Chapter 2, among the various schemes derived from the flyback topology, the flyback converter with two secondary side windings is the most popular one, and is therefore chosen as the starting point of the work.

As shown in Fig.3.1, the power stage of the inverter consists of a PV panel, an input capacitor C_{pv}, a flyback converter with two secondary side windings together with a waveform unfolding arrangement, and an LC output filter, whose output is directly connected to the utility grid. The two secondary-side switches S1 and S2 form

an unfolding type inverter and are controlled as per the polarity of the grid voltage to generate the AC current, i_o. In the positive half-cycle, S1 is kept on and S2 off for the entire 180° of the AC cycle, while in the negative half cycle, S2 is kept on and S1 off. In either case, the inverter works as a DC to DC flyback converter with the average output current shaped as a half-sinusoid at the line frequency.

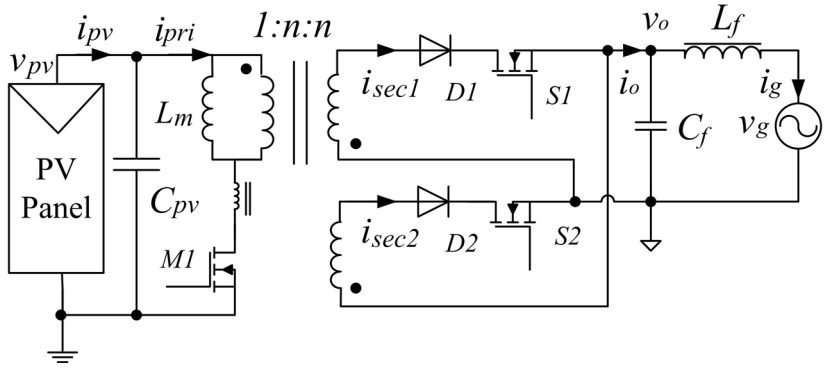


Fig.3.1: A flyback-DCM microinverter

This topology was first introduced as an AC module inverter in [49], where a center-tapped transformer is used instead of two secondary side windings in Fig.3.1. This inverter was designed in DCM operation for a 100W application. Its simplicity and potential low cost has attracted much attention from academia. Two major challenges have been identified by researchers in this field, the first being the need to improve the conversion efficiency and the second being the lifetime issues posed by the use of an electrolytic capacitor to implement C_{pv}.

For the first challenge concerning efficiency, references [32] and [31] have adopted two different switched-capacitor snubber circuits to provide Zero Voltage Transition (ZVT) of the main switch and thus reduce the switching loss due to hard switching. The average efficiency reported in [32] reaches 93.1%. As the switching frequencies used are low (16 kHz in [2]), the reported average efficiency

improvements due to soft-switching (0.3% in [2]) are not apparent. In [31], the reported efficiency is 84%, with efficiency improvement of 2% due to soft-switching. A commercial product [48] based on flyback DCM operation utilizes multiple operating modes to deal with power loss at different power levels. Depending on the DC input current, DC input voltage and AC output current, the inverter transitions between regular flyback mode, interleaved mode (at high current), a quasi-resonant mode similar to [31] (at high output voltage) and even a combined interleaved and quasi-resonant mode. By adding complexity in the power circuit and the controller, a California weighted efficiency (refer to Chapter 2.2.3.2) of 96% has been reported for this scheme[82].

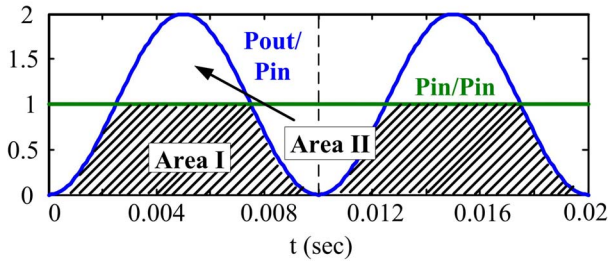
On the other hand, reference [50] has explored the possibility and benefits of operating the flyback inverter in boundary conduction mode (BCM) for larger power levels, with experimental efficiency between 93%~97%. Based on the work in [50] , reference [106] has proposed a dual mode switching strategy combining the advantages of DCM operation at low instantaneous power and BCM operation at higher power levels. No efficiency information has been disclosed in [6], however.

Overall, the bottleneck for this flyback inverter lies in conversion efficiency. Flyback converter in DCM operation suffers from large current stress, which causes high switching power loss. This is especially true for AC module application at medium power level. When operated in Continuous Conduction Mode (CCM), a flyback converter has lower peak currents and hence higher efficiencies. This has been exploited before in both DC/DC power conversion and AC/DC power factor

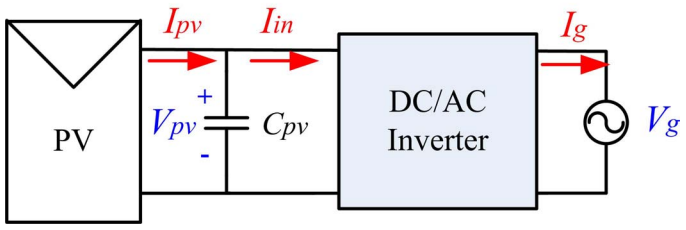
correction applications. However, the control to output current transfer function in a flyback-CCM converter has a RHP (Right Half Plane) zero, which causes difficulty in controlling the output current of the converter effectively. This may have prevented the use of the flyback-CCM converter as a microinverter.

Therefore, in our approach, we investigate the feasibility of a flyback inverter operating (mainly) in CCM mode as a grid connected AC module inverter, with a view to demonstrating that a significant efficiency improvement can be realized without adding to the complexity of both the power and control circuits. Before going into details of flyback operation, the requirements of power decoupling capacitors at PV side are discussed first.

3.3 Design of Input Capacitors at PV Side



(a) Power imbalance between input power and output power



(b) Input capacitor for power decoupling

Fig.3.2: Circuit diagram for PV side capacitor

Fig.3.2 (a) illustrates the need for power decoupling in a single phase DC-AC inverter and Fig.3.2 (b) shows the schematic diagram when this is handled by a PV side capacitor. Since in this scheme, the power decoupling capacitor is placed at the

PV side as shown in Fig.3.2(b), the requirements from both PV side and grid side need to be considered in the choice of the capacitor.

The requirement from the PV side is as follows. A maximum power point tracker (MPPT) is usually included in the inverter so that the PV panel is operated at its maximum power point. It must be ensured that voltage ripple is small so that the PV module operates close to the vicinity of the maximum power point in practice. The maximum voltage ripple allowed to satisfy the MPPT requirement as well as the required decoupling capacitance is discussed in Section 3.3.1.

The requirement from the grid side is as follows. The voltage ripple at the input side has the potential to influence the output current harmonics based on instantaneous power balance between input and output. In order to achieve a THD of output current less than 5%, there is a limit for the PV module voltage ripple as well. This requirement will be discussed in Section 3.3.2.

While analyzing the MPPT requirement and the output power factor requirement, the high frequency switching ripple is ignored. Design of high frequency capacitor filter for switching ripple follows the standard design procedure.

3.3.1. MPPT Requirement

As discussed earlier, the voltage ripple due to the power decoupling must be kept low in order to ensure that the PV panel operates as close to the maximum power point as possible at all times. This is illustrated in Fig.3.3, where the PV voltage ripple around MPPT point leads to the actual average PV output $P_{pv,ave}$ less than the real

MPPT power P_{mp}. The ratio between these two values is defined as PV utilization ratio k_{pv} in [2], which will be studied in the following study.

$$k_{pv} = \frac{P_{pv,ave}}{P_{mp}} \tag{3-1}$$

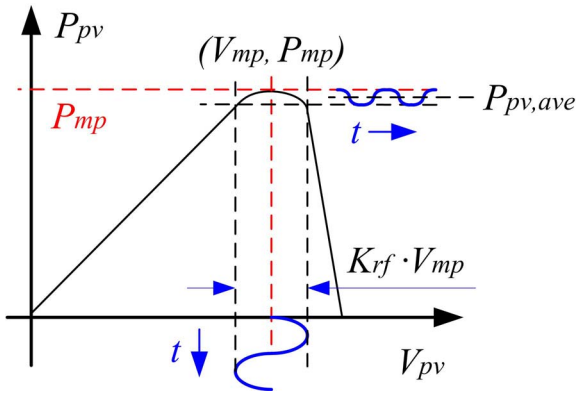


Fig.3.3: The influence of PV voltage ripple to actual PV power

The relationship between the voltage ripple and this PV utilization ratio k_{pv} has been studied in [1, 2], where the PV module current is approximated using a second order Taylor polynomial. As Taylor approximation requires small signal assumption, it is only valid when the voltage ripple is small. Besides, the PV module information used in this calculation is not given, which does not justify the generalization of the conclusion to other PV modules.

In order to find the PV utilization factor, we follow the approach below using mathematical calculation in Matlab. The purpose of this analysis is to find out the maximum allowed voltage ripple in order to ensure a PV utilization ratio above 98%.

Overall, the flow chart to calculate the PV utilization ratio k_{pv} from the PV voltage ripple factor k_{rf} is summarized in Fig.3.4 and will be explained in detail below.

Here, two assumptions have been made for PV voltage and PV current calculation in Fig.3.4 as discussed below.

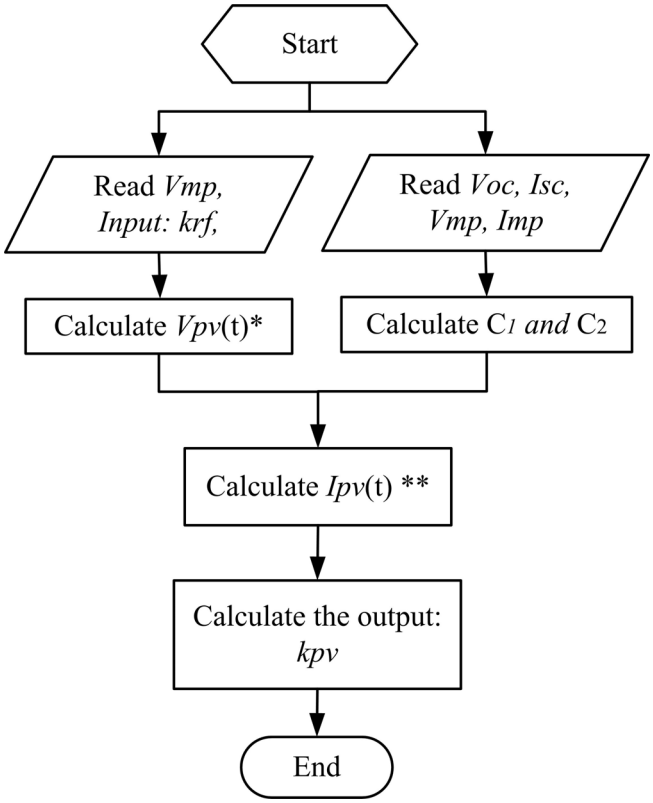


Fig.3.4: Calculation flow chart of ripple factor's influence to PV utilization ratio (* and ** indicates two assumptions for calculation)

Firstly, in an ideal case, the input voltage V_{pv} is fully filtered by the input capacitor and is assumed to be at the Maximum Power Point (V_{mp} and I_{mp}). Power balance over an AC cycle can be represented by:

$$I_{mp} = \frac{V_{rms} I_{rms}}{V_{mp}} \tag{3-2}$$

However, in practice, the decoupled second harmonic power will still show up as a voltage ripple on the capacitor. Assuming zero power loss in the DC-AC inverter and instantaneous power balance between input and output, the input current of the inverter will be pulsating at twice the line frequency.

$$I_{in} = \frac{2V_{rms}I_{rms}\sin^2(\omega t)}{V_{mp}} = 2I_{mp}\sin^2(\omega t) \tag{3-3}$$

Therefore, the input capacitor current can be calculated by:

$$I_c = I_{mp} - I_{in} = I_{mp}\cos(2\omega t) \tag{3-4}$$

Hence the capacitor voltage, i.e. the actual PV voltage can be calculated as:

$$V_{pv} = V_c = V_{mp} + \int \frac{I_c}{C_{pv}} dt = V_{mp}\left(1 + \frac{1}{2}k_{rf}\sin(2\omega t)\right) \tag{3-5}$$

$$k_{rf} = \frac{I_{mp}}{V_{mp}C_{pv}\omega}, \tag{3-6}$$

where, k_{rf} is defined as the ratio of the peak-to-peak voltage ripple versus the average voltage. In (3-5), this ratio refers to the peak-to-peak ripple versus MPPT voltage of the PV module. Here, equation (3-5) is used to calculate the V_{pv} in the flow chart in Fig.3.4.

Secondly, a simple model of a PV panel (as discussed in Chapter 1) given by a current source and m series connected anti-parallel diode is used. It may be noted that the idea behind the model is to reproduce the DC characteristic curve and not the realization of an accurate physical model.

Therefore, the PV module current can be calculated from PV voltage as discussed in Section 1.2.2.1.

$$I_{pv} = I_{sc} - C_1\left[\exp(\frac{V_{pv}}{C_2}) - 1\right], \tag{3-7}$$

where I_{sc} represents the short circuit current of PV module (corresponding to I_L in (1-1)); C_1 and C_2 are used as curve fitting parameters. For different PV modules, the parameters（C_1 and C_2）are different. Usually the operating

conditions at STC (Standard Testing Conditions) i.e. V_{mp}, I_{mp}, V_{oc} and I_{sc} are given in the datasheet provided by the manufacturer.

As shown in Fig.3.4, based on the information above, the variables C_1 and C_2 for selected PV module can be calculated as:

$$C_2 = \frac{V_{oc} - V_{mp}}{\ln\left(\frac{I_{sc}}{I_{sc} - I_{mp}}\right)} \tag{3-8}$$

$$C_1 = \frac{I_{sc}}{\exp\left(\frac{V_{oc}}{C_2}\right) - 1} \tag{3-9}$$

Equation (3-8) and (3-9) can be substituted into (3-7) so as to calculate the actual PV module current based on PV voltage given by (3-5).

Following that, the actual PV power can be obtained as:

$$P_{pv}(t) = V_{pv}(t) \times I_{pv}(t) \tag{3-10}$$

Finally, the PV utilization ratio can be calculated as:

$$k_{pv} = \frac{\int_{t=0}^{T_{ac}} P_{pv}(t)dt}{V_{mp} \cdot I_{mp} \cdot T_{ac}} \tag{3-11}$$

where T_{ac} represents the AC line period.

With k_{pv} calculated from (3-11), the required capacitance can be derived from (3-6) as:

$$C_{pv} = \frac{I_{mp}}{V_{mp} \cdot k_{rf} \cdot \omega} \tag{3-12}$$

Following the approach discussed above, in this work, a Kyocera's 200W PV module is used (given in Chapter 1) to calculate the variation of PV utilization ratio

when the PV voltage ripple factor changes. The result is shown in Fig.3.5, where the parameters used are under NOCT (Nominal Operation Cell Voltage) condition where MPPT voltage is 23.2V, MPPT current is 6.13A, short-circuit current is 6.62A, the open circuit voltage is 29.9V and the AC cycle frequency is 50Hz.

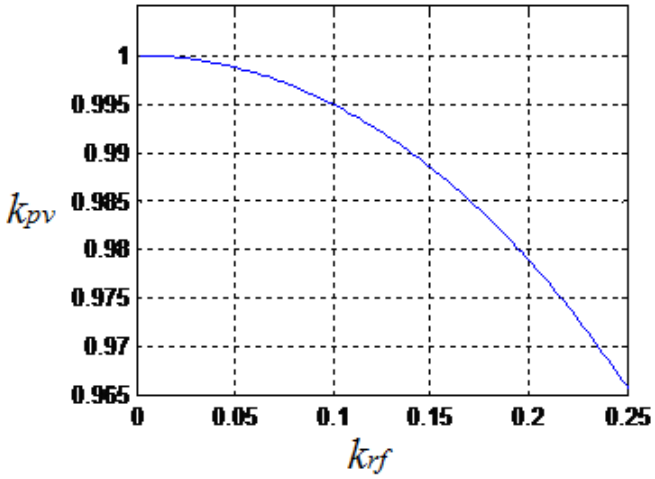


Fig.3.5: PV utilization ratio vs. PV voltage ripple factor for KC200GT at NOCT (Nominal Operating Cell Temperature: 47°C)

According to Fig.3.5, it is noticed that in order to obtain a PV utilization ratio of 99% for a given PV module KC200GT at NOCT condition, a ripple factor below 14% is required. Similarly, a ripple factor below 19% is needed to ensure a static maximum power efficiency of 98%.

Similarly, if designed for the same PV module under STC (Standard Test Condition), the corresponding ripple factor and capacitance required are tabulated in Table 3.1.

Table 3.1: Design of Input Capacitance under Different Conditions

Condition	Utilization Ratio	Ripple Factor	Input Capacitance
STC	99%	12%	7.7mF
	98%	17%	5.4mF
NOTC	99%	14%	6mF
	98%	19.4%	4.4mF

According to calculation in [1] based on a second-order Taylor series approximation, the magnitude of voltage ripple should be below 8.5% to ensure above 98% PV utilization ratio, which corresponds to a ripple factor of 17%. This complies with the calculation result from the approach discussed in this section, although the PV module specification for this result was not mentioned in [1].

3.3.2. Output Power Quality Requirement

According to the calculation in above section and similar studies such as in [1], peak-to-peak voltage ripple up to 17% - 19% of MPPT voltage is possible to achieve above 98% PV utilization ratio. However, in this case, the constant voltage assumption in the instantaneous power balance equation (3-3) is no longer valid, which leads to a distortion of output current.

One example is simulated based on circuit diagram in Fig.3.2 b) with PV module modeled by (3-7) at STD condition with 19% voltage ripple factor. The operating waveforms are shown in Fig.3.6, where it is observed that both PV module voltage and current show a second harmonics reflected from grid side. As a result, the grid current also shows a distortion from sinusoidal waveform.

The following analysis is to find out the theoretical relationship between PV module voltage ripple and the output power quality.

Firstly, a linear approximation of PV module current vs. PV module voltage around MPP is assumed for simplicity of calculation.

$$I_{pvl} = 2 \cdot I_{mp} - \frac{I_{mp}}{V_{mp}} \cdot V_{pv} = I_{mp} - \frac{1}{2} k_{rf} I_{mp} \sin(2\omega t) \tag{3-13}$$

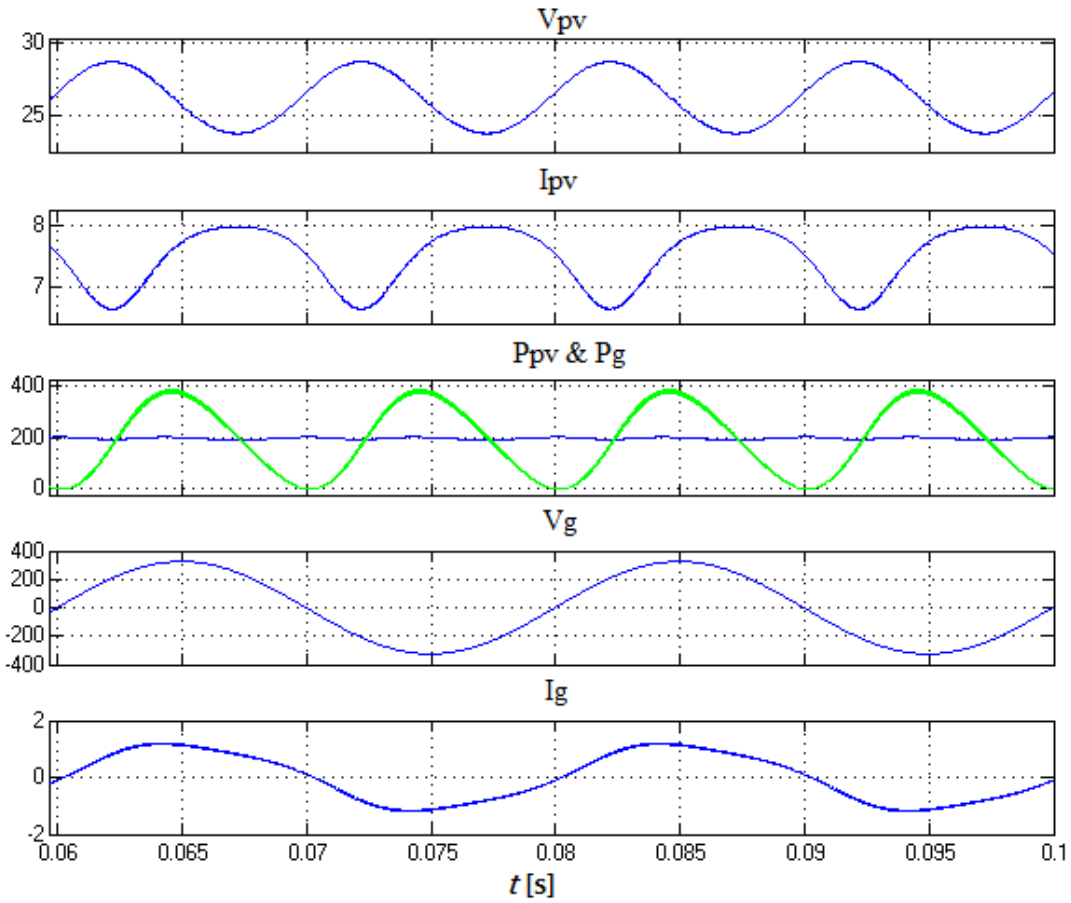


Fig.3.6: Simulation of KC200GT (STC) around MPPT point (*Vmp*=26.3V, *Imp*=7.61A)

According to Fig.3.7, the linear approximation is valid during around 25~27V (corresponding to ripple factor of 7%). For a ripple factor of 19.4% given in Table 3.1 (i.e. 24-29V), there is a slight deviation but the linear approximation can be used as the worst case for simplicity of the voltage ripple factor calculation.

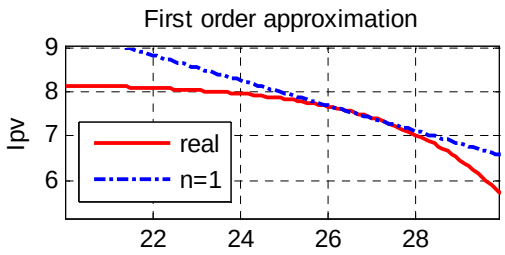


Fig.3.7: Linear (first order Taylor) approximation near MPP for KCT200GT (STD)

For grid-tied inverter with a given sinusoidal grid voltage, the instantaneous power balance equation (3-3) can be changed to:

$$V_{pv} \times \left(I_{pvl} - C_{pv} \frac{dV_{pv}}{dt} \right) = \sqrt{2} V_{rms} \sin(\omega t) \times I_g , \tag{3-14}$$

where V_{pv} is subject to a second harmonics distortion due to the power decoupling capacitance discussed in last section and given by (3-5). PV module current and PV side capacitance for power decoupling can be substituted by (3-13) and (3-12). As a result, the gird current can be calculated as:

$$\begin{aligned} I_g &= \frac{V_{mp} I_{mp}}{\sqrt{2} V_{rms}} \cdot \left(1 + \frac{1}{2} k_{rf} \sin(2\omega t) \right) \left(2\sin(\omega t) - k_{rf} \cos(\omega t) \right) \\ &= \frac{I_{rms}}{\sqrt{2}} \left\{ \left[\left(2 - \frac{1}{4} k_{rf}^2 \right) \sin(\omega t) - \frac{1}{2} k_{rf} \cos(\omega t) \right] - \frac{1}{2} k_{rf} \left(\cos(3\omega t) + \frac{1}{2} k_{rf} \sin(3\omega t) \right) \right\} \\ &= \frac{I_{rms}}{\sqrt{2}} \left[\sqrt{\left(2 - \frac{1}{4} k_{rf}^2 \right)^2 + \frac{1}{4} k_{rf}^2} \sin(\omega t + \varphi) - \frac{1}{2} k_{rf} \sqrt{1 + \frac{1}{4} k_{rf}^2} \sin(3\omega t + \theta) \right] \end{aligned} \tag{3-15}$$

Equation (3-15) indicates that the grid current consists of fundamental frequency and the third harmonic components. The harmonics factor of the third harmonic component is:

$$HF_3 = \frac{I_{3,rms}}{I_{1,rms}} = \sqrt{\frac{1 + \frac{1}{4} k_{rf}^2}{1 + \left(\frac{4}{k_{rf}} - \frac{1}{2} k_{rf} \right)^2}} \tag{3-16}$$

As shown in (3-16), this harmonic is solely determined by PV voltage ripple factor based on our assumptions.

Based on (3-16), the relationship between the PV voltage ripple factor and the output current third harmonic factor is drawn in Fig.3.8. However, it is worth to

mention that this relationship is based on ideal case assumption. In practical implementation, the control dynamics as well as the components or IC non-ideality (such as current sensing, MOSFET driver), will add to the total distortion of output current.

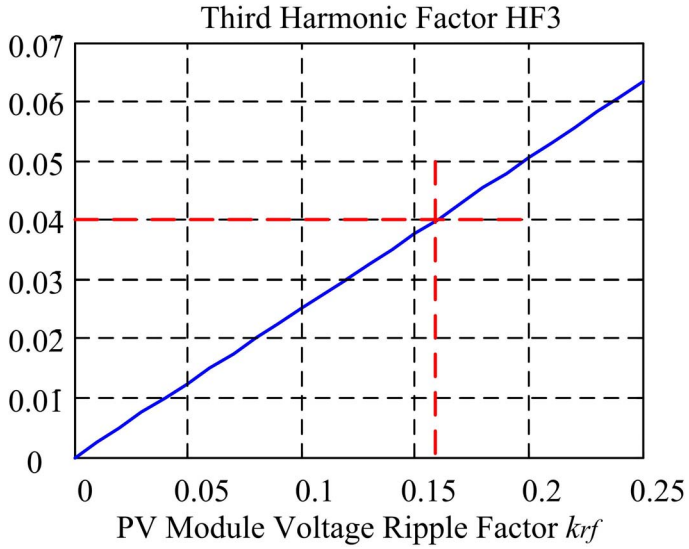


Fig.3.8: Influence of PV voltage ripple factor to third harmonic factor of output current

As introduced in Table 1.2, the third harmonic factor should be below 4% of fundamental component. Therefore, in ideal case, it is recommended to decide the ripple factor and the input capacitance values based on third harmonics factor less than 1~ 2% to allow adequate design margin for hardware implementation and control. This corresponds to a ripple factor between 4%~8% in Fig.3.8, which is much smaller than the values in Table 3.1 required by PV module MPPT requirement discussed in Section 3.3.1.

Based on the ripple factor limit and equation (3-12), the required power decoupling capacitance can be found. In this design, an input capacitance value above 11.6mF is required for PV voltage ripple factor less than 8% under STC.

3.4 Analysis and Design of the Flyback inverter

In order to provide a fair comparison, a flyback inverter designed for DCM operation is used as a benchmark. The quasi-steady state operation over an AC cycle under different power levels is analyzed to serve as the basis for design in Section 3.4.1. Design guidelines for the flyback-DCM inverter and the flyback-CCM scheme are also provided below in Section 3.4.2 and 3.4.3 respectively.

3.4.1. Quasi-steady State Analysis

As the operating condition of the inverter changes slowly during an AC period compared to a switching period, the inverter can be assumed to operate in quasi-steady state around each instant of an AC cycle. It is also assumed that capacitor is large so that the input voltage, V_{pv}, is nearly constant in an AC cycle.

Assuming lossless operation, the power balance equations under both DCM and CCM conditions can be written as:

$$V_{pv} I_{pv} = V_{rms} I_{rms} = P_{pv} \tag{3-17}$$

$$V_{pv} I_{pri} = V_g I_g = 2 V_{rms} I_{rms} \sin^2(\omega t) \tag{3-18}$$

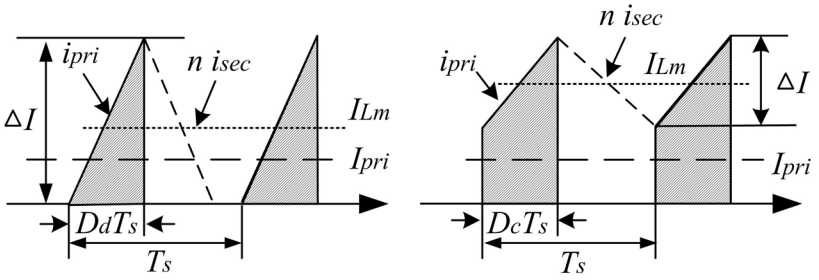
Equation (3-17) is based on the power balance over an AC cycle, and represents the average PV power transferred to the grid. Equation (3-18) represents the instantaneous power balance between input and output in each switching cycle. The mismatch between the dc power of the PV module indicated by (3-17) and the pulsating instantaneous input power of the flyback inverter indicated by (3-18) is

handled by the input capacitor C_{pv} (Fig.3.1). As mentioned before, this capacitor is believed to be the bottleneck for the reliability of most single stage inverters. This will be further discussed in Section 3.3.

Equation (3-18) is not completely true for CCM operation as the transformer core will not be fully demagnetized in CCM operation in each switching cycle. This causes the transformer core to serve as an energy buffer, adding to the order of the system. However, our investigation shows that the effect of this incomplete core demagnetization on the input-output energy balance in each switching cycle is very small and can be neglected, which will be discussed in Section 3.4.4.

3.4.1.1.DCM/CCM Operation over AC cycle

The current waveforms of the magnetizing inductance of a flyback converter operated in DCM and CCM are illustrated below in Fig.3.9.



(a) DCM (b) CCM

Fig.3.9: Current waveforms of magnetizing inductance of flyback transformer

Based on converter operation waveforms, the current ripple in both cases is given by:

$$\Delta I = \frac{V_{pv}}{L_m f_s} D \tag{3-19}$$

Here, D is the duty cycle of primary side switch and f_s is the switching frequency. Also, L_m is the primary side magnetizing inductance of the transformer.

For DCM operation, the primary side average current, I_{pri}, can be shown to be:

$$I_{pri} = \frac{1}{2} D_d T_S \cdot \Delta I = \frac{V_{pv}}{2L_m f_s} D_d^2 \tag{3-20}$$

Here, D_d is the duty cycle in DCM operation.

By substituting (3-17) and (3-18) into (3-20), the duty ratio of the inverter in DCM is obtained.

$$D_d = \frac{|V_g|}{V_{rms}} \sqrt{\frac{2I_{pv} L_m f_s}{V_{pv}}} \tag{3-21}$$

Equation (3-21) shows that in DCM the duty cycle varies according to the (rectified) grid voltage while its amplitude is determined by the ratio of PV module voltage by PV module current. In this case, a simple open loop scheme without current feedback can be adopted. By varying the amplitude of the duty cycle, the ratio of V_{pv} over I_{pv} can be varied in order to seek and operate the system at MPP (Maximum Power Point) [49].

When operated in CCM, by assuming quasi-steady state operation and using inductor volt-seconds balance over a switching period, the duty ratio D_C can be obtained.

$$D_C = \frac{|V_g|}{nV_{pv} + |V_g|} \tag{3-22}$$

Here, the duty cycle in CCM operation only relates to input and output voltage

ratio and the turns ratio of the flyback transformer. It is not directly determined by the current and hence power level. Therefore, for given input/output voltages, once the turns ratio n is fixed, the duty cycle variation in CCM is fixed.

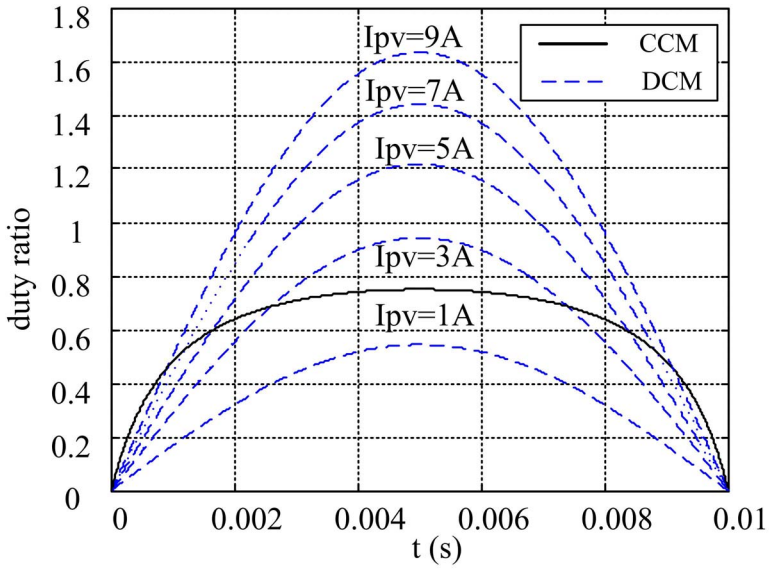


Fig.3.10: Duty Ratio Variations during half an AC cycle for CCM ($L_m = 20\mu H$) and DCM ($L_m = 4\mu H$) operations with $V_{pv} = 27V$, $V_{rms} = 230V$, $n = 4$

The variation of duty ratio over half an AC cycle at different input currents is shown in Fig.3.10 at given value of n and L_m. As indicated by (3-22), the duty cycle of CCM case does not change with input current. Also, a lower turns ratio n would lead to a larger duty ratio.

On the other hand, as indicated by (3-21), the duty ratio in DCM case has nothing to do with turns ratio, but is influenced by L_m at a given specification and chosen frequency f_s. For a given design (L_m and f_s), the duty cycle increases with input current with fixed input voltage. If the instantaneous duty cycle at DCM is below the CCM curve set by the turns ratio in Fig.3.10, the inverter operates in DCM; otherwise, the inverter operates in CCM. In order to make sure that the

inverter works in DCM only, the choice of n and L_m should make sure that the CCM duty cycle curve does not intersect with the DCM curve at the maximum input current (equivalent to the maximum input power at fixed voltage). From Fig.3.10, it can be seen that such a judgment can be made at the maximum duty cycle, which corresponds to the instance of peak AC voltage. Therefore, in the next section, only the instance of the peak AC voltage is considered to simplify the design process.

3.4.1.2. Design Aid Diagram

The maximum duty cycle values (denoted by the '^' symbol) in an AC period occur at the AC peak instants in both cases and can be written as:

$$\hat{D}_d = 2\sqrt{\frac{I_{pv} L_m f_s}{V_{pv}}} \tag{3-23}$$

$$\hat{D}_C = \frac{\sqrt{2}V_{rms}}{\sqrt{2}V_{rms} + nV_{pv}} \tag{3-24}$$

The design condition for the peak duty cycle to occur at the DCM/CCM boundary operation can be derived by equating (3-23) and (3-24).

$$L_{mc} = \frac{V_{pv}}{4I_{pv} f_s \left[nV_{pv} \big/ (\sqrt{2}V_{rms}) + 1 \right]^2} \tag{3-25}$$

Here, L_{mc} is the critical inductance between DCM and CCM operations. When $L_m < L_{mc}$, the flyback inverter works in DCM over all of the AC cycle. When $L_m > L_{mc}$, the flyback inverter operates in CCM partially near the peak AC cycle. In this case, most likely, the designed inverter works in a combined DCM/CCM mode. For example, as shown in Fig.3.10, at lower grid voltage around

zero-crossing points, the flyback operates in DCM mode, the flyback operates in CCM mode when the grid voltage is larger. Based on Fig.3.10, the boundary gird voltage V_{gb}, at which DCM/CCM transition occurs for a given power level P_{pv}, can be derived at the duty cycle crossing point (from (3-21) and (3-22)).

$$V_{gb} = V_{pv}(V_{rms}\sqrt{\frac{1}{2P_{pv}f_sL_m}} - n) \tag{3-26}$$

If $V_{gb} > \sqrt{2}V_{rms}$, the designed flyback inverter operates in DCM over the complete AC cycle; if $0 < V_{gb} < \sqrt{2}V_{rms}$, the designed inverter works in combined DCM/CCM in an AC cycle. Lastly, if $V_{gb} < 0$, the flyback inverter will work in CCM[1] only over the complete AC cycle at the specified PV power level .

Therefore, the flyback magnetizing inductance value to ensure a full CCM operation over an AC cycle can be derived from (3-26) for a specified PV power:

$$L_{m,ccm} > \frac{{V_{rms}}^2}{2n^2V_{pv}I_{pv}f_s} \tag{3-27}$$

Based on (3-27), full CCM operation over AC cycle is possible by designing a large turns ratio n and a large magnetizing inductance L_m. Although practically, the current will inevitably start from zero during the zero-corssing point. Besides, when the power level reduces, the designed inverter will inevitably operate in a combined DCM/CCM manner.

Equations (3-23) ~(3-27) relate the peak control variable $\hat{D}$, the PV module specifications V_{pv}, I_{pv} and the design parameters of the inverter, viz., n, L_m and f_s, under both DCM and CCM conditions.

[1] Thanks to Mr. Fonkwe Edwin from Masdar Institute for pointing out this possibility.

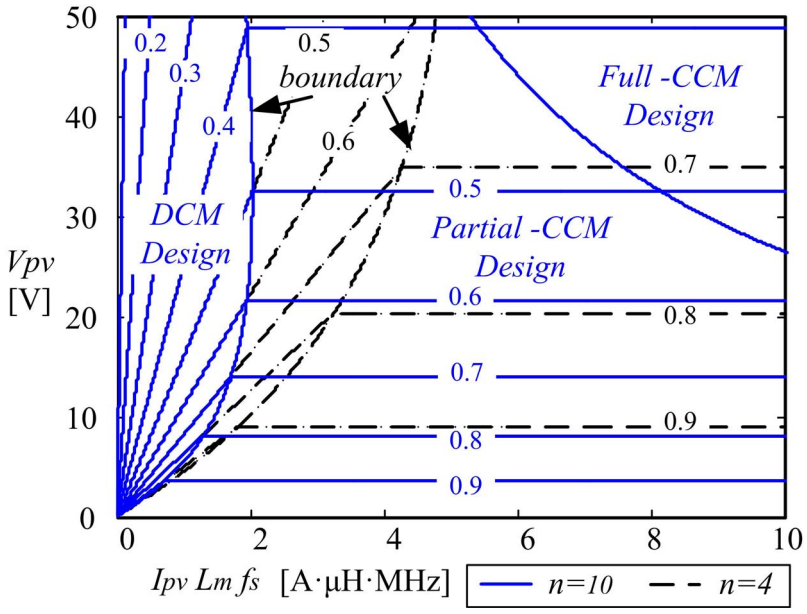


Fig.3.11: Design aid diagram of flyback inverter V_{rms} = 230 V. (The numbers on the lines indicate the peak duty ratios).

A design-aid diagram is shown in Fig.3.11 for an assumed grid voltage of 230 V_{rms} and for two assumed values of the turns ratio, n (= 10 & 4). For the assumed V_{rms} and n values, every point on the graph in Fig.3.11 represents a possible inverter design. For example, $n = 10$, $I_{pv} L_m f_s = 3$ and $V_{pv} = 22V$ represents a partial-CCM design with $\hat{D} = 0.6$.

The curves marked 'boundary' represent the boundary between partial-CCM design and DCM-only design for the two n values assumed.

Another curve on the right top corner represents the boundary between partial-CCM design combined operation and CCM-only design for $n = 10$. For $n = 4$, the required L_m is too large so that it is out of the range of x-axis. The choice of $\hat{D}$ influences the component current stresses as will be discussed in the following sub-sections.

3.4.1.3. Components Stresses

In order to properly select the components as well as to calculate the power loss, the worst case voltage stresses and current stresses as well as the RMS current of individual legs are derived.

The voltage stresses of the semiconductors are the same for both DCM and CCM cases. For example, the pulse-by-pulse and the overall maximum voltage stresses on the main switch M1 are:

$$V_{M1} = V_{pv} + V_g / n \tag{3-28}$$

$$\hat{V}_{M1} = V_{pv} + \sqrt{2}V_{rms} / n \tag{3-29}$$

The instantaneous and overall maximum voltage stresses on the secondary diodes D1 and D2 are:

$$V_{d1,2} = nV_{pv} + V_g \tag{3-30}$$

$$\hat{V}_{d1,2} = nV_{pv} + \sqrt{2}V_{rms} \tag{3-31}$$

The instantaneous and overall maximum voltage stress on the secondary switches S1 and S2 are:

$$V_{S1,2} = 2V_g \tag{3-32}$$

$$\hat{V}_{S1,2} = 2\sqrt{2}V_{rms} \tag{3-33}$$

From (3-29) and (3-31) , it is noted that a larger n increases the voltage stresses of the secondary side diodes D1 and D2, but reduce the voltage stress of the primary side switch M1. Besides, from (3-24) and Fig.3.11, it is found that a smaller

n helps to increase the duty cycle of CCM operation; smaller n also enlarges the duty cycle as well as magnetizing inductance for DCM-only operation.

In DCM operation, the cycle-by-cycle peak primary current is given by:

$$I_{pd} = \Delta I = \frac{V_{pv}}{L_m f_s} D_d \tag{3-34}$$

Substituting the maximum duty cycle from (3-23) into (3-34) , the maximum value of this peak primary current in DCM , i.e. the primary side current stress is obtained as:

$$\hat{I}_{pd} = 2\sqrt{\frac{I_{pv} V_{pv}}{L_m f_s}} \tag{3-35}$$

According to (3-35), the maximum value of the peak primary current stress in DCM depends on the input power $V_{pv} I_{pv}$, f_s and L_m values but not on n. A larger L_m would reduce the primary side current stress; but the inductance value can not be too large so as not to cross over into the CCM operating range.

As shown in Fig.3.9, the average value of magnetizing current of flyback converter in CCM mode is given by:

$$I_{Lm} = \frac{I_{pri}}{D_c} \tag{3-36}$$

The cycle-by-cycle peak primary current in CCM is:

$$I_{pc} = I_{Lm} + \frac{1}{2}\Delta I = \frac{I_{pri}}{D_c} + \frac{V_{pv}}{2L_m f_s} D_c \tag{3-37}$$

Substituting (3-17), (3-18), (3-22) into (3-37), the expression for primary side

cycle peak current is obtained:

$$I_{pc} = I_{pv}V_{pv}\frac{V_g^2}{V_{rms}^2}\left(\frac{n}{V_g}+\frac{1}{V_{pv}}\right)+\frac{1}{2L_m f_s\left(n/V_g+1/V_{pv}\right)} \tag{3-38}$$

According to (3-38), assuming that n and L_m values are chosen and V_{pv} is known, the maximum value of the peak current occurs at the maximum AC voltage $\hat{V}_g = \sqrt{2}V_{rms}$ and maximum input power level (= the rated power $V_{pv}I_{pv}$).

By substituting $\hat{V}_g = \sqrt{2}V_{rms}$ into (3-38), the peak primary current stress is given by:

$$\hat{I}_{pc} = 2I_{pv}V_{pv}\left(n/\sqrt{2}V_{rms}+1/V_{pv}\right)+\frac{1}{2L_m f_s\left(n/\sqrt{2}V_{rms}+1/V_{pv}\right)} \tag{3-39}$$

The corresponding secondary side peak current stresses in DCM and CCM are:

$$\hat{I}_{sd} = \frac{\hat{I}_{pd}}{n} \tag{3-40}$$

$$\hat{I}_{sc} = \frac{\hat{I}_{pc}}{n} \tag{3-41}$$

Equations (3-35), (3-39) - (3-41) indicate the influence of the design parameters n and L_m on the primary side and secondary side current stresses. It is noted that a large L_m is preferred to reduce the current ripple on both sides, while the choice of n is related to voltage stresses trade-off between (3-29) and (3-31) as well.

3.4.2. Design and Control of a Flyback-DCM Inverter

In this part, the design procedure of a flyback-DCM inverter as well as the control scheme for DCM operation will be introduced. This flyback-DCM inverter

will be used as a benchmark to compare with the proposed flyback-CCM inverter in Section 3.5.

For a DCM-only design, as shown in (3-35), the peak primary current depends on the input power $I_{pv}V_{pv}$, f_s and L_m values and not on n. However, n sets the limit for a maximum duty cycle for CCM, which also sets an upper limit L_{mc} for L_m also. According to (3-25), a smaller n would lead to a larger value of L_{mc}. A larger L_m, but less than L_{mc}, would reduce the primary side current. Therefore, in general, a small n and a large L_m are preferred for DCM-only design.

Based on the analysis above, a design process for the flyback inverter working in DCM based on Fig.3.11 is suggested below. The grid voltage in the example given is 230Vrms.

Step 1: Identify PV panel specifications. The PV panel voltage and current values given by the manufacturer correspond to MPP and vary with solar irradiance and temperature. For design purposes, a constant PV voltage is used while the variation of power is considered to be due to current change.

Step 2: Choose a switching frequency considering the trade-off between the switching losses and the transformer size. In our design, 100 kHz is used.

Step 3: Choose an initial transformer turns ratio, n. Start with a small number. This can be tuned later.

Step 4: With the grid RMS voltage value given, find out the peak duty ratio and

L_{mc} from Fig.3.11 or (3-24) and (3-25) .

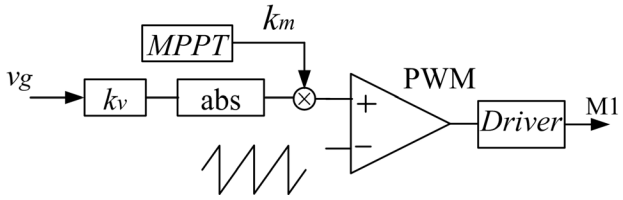
Step 5: Calculate the voltage stresses of the primary and secondary side devices using (3-29), (3-31) and (3-33).

Step 6: Choose L_m ($< L_{mc}$) on Fig.3.11. Note that a larger L_m should be selected to reduce the current stress but certain design margin should be given before it enters CCM operation. Also, the corresponding $\hat{D}$ can be found on the curve of Fig.3.11.

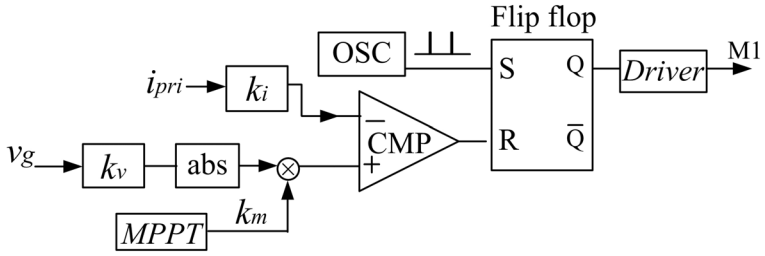
Step 7: Calculate the current stresses using (3-35) and (3-40).

Step 8: Return to Steps 3~7 until the voltage and current stresses are acceptable.

If the primary current stress or the secondary diode voltage stress is too large, n can be reduced. Otherwise, if the secondary side current stress or the primary side voltage stress is too large, n can be increased.



(a) An open-loop current controller



(b) A closed-loop current controller

Fig.3.12: Control Schemes for Flyback-DCM Inverter

As shown in Fig.3.12, current control of flyback-DCM inverter can be either in an open-loop or close-loop based on equation (3-21). According to (3-21), the duty cycle of a flyback-DCM inverter is rectified sinusoidal with its amplitude determined by the ratio of V_{pv} and I_{pv}. This ratio represents input impedance of the inverter R_{in}. When this impedance equals to the characteristics impedance R_{mp} of PV module given by V_{mp}/I_{mp}, the PV module is operated at the Maximum Power Point (MPP). Therefore, the magnitude of rectified sinusoidal duty cycle k_m is determined by MPPT in both controllers.

In Fig.3.12 (a), a commonly used open-loop control scheme is shown, where the duty cycle directly follows the rectified grid voltage while its amplitude is determined by MPPT. This open-loop control takes advantages of the intrinsic current source feature of flyback converter in DCM mode. Although, the disturbance in input voltage will directly affect the THD of output current since there is no feedback control involved.

Or alternatively, a peak current controller (Fig.3.12 (b)) can be used to track the reference current in a close-loop manner. This is based on the instantaneous power balance equation (3-18) plus (3-20) and (3-34), which can be rewritten below:

$$I_{pd} = 2\sqrt{\frac{V_{rms}I_{rms}}{L_m f_s}}\sin(\omega t) \tag{3-42}$$

In this case, the primary side current of flyback converter is sensed and feedback to compare with a rectified sinusoidal peak reference current. As a result, the disturbance in input voltage is taken care of by the control loop.

In the latter part, the open-loop control scheme in Fig.3.12 a) is used for the benchmark flyback-DCM inverter as the purpose is to verify the efficiency improvement in steady state operations.

3.4.3. Design of a Flyback-CCM Inverter

For a CCM design, the peak current stress is related to both n and L_m values as in (3-39). The primary side peak current has the same value as the peak value of the net transformer magnetizing current (primary and secondary sides combined) reflected on to the primary. In (3-39), the first term is the average value of the net magnetizing current, while the second term is half of the peak to peak ripple in the net magnetizing current. A larger n value would lead to a higher average net magnetizing current (first term) while at the same time reducing the current ripple (second term). As the average magnetizing current is larger than the current ripple in CCM operation, in general, a smaller n value is preferable to reduce the primary side current stress.

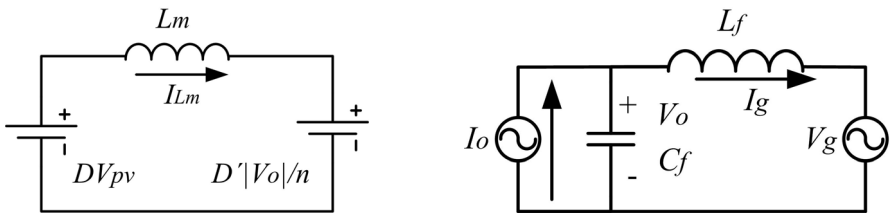
The design guideline for flyback-CCM inverter is similar to the case for DCM operation, with change in Step 6, which is given below.

Step 6: Choose $L_m (> L_{mc})$ based on acceptable primary current stress using (3-39). A larger L_m reduces primary current stress, while increasing transformer size.

3.4.4. Output Current Power Factor

As a grid-tied inverter, the output power factor at the point of connection to grid is expected to be unity. When connected to the grid, the interaction between the PV inverter and grid impedance causes the voltage whether the inverter is connected is distorted and the output power factor will be affected accordingly. Here, for microinverter with power level from 100W-300W, as the output current is around 1~2A (small), the effect of the grid impedance is relatively small. In this study, the grid is taken as an ideal voltage source and the grid impedance is not considered.

In actual operation, the power factor is influenced by many other factors. These include the effects of input capacitor, incomplete demagnetization of flyback transformer and output filter. To simplify the analysis, these effects have been considered separately since the effect of each of them on the power factor is small. The influence of input capacitor has been studied in Section 3.3 and a design margin has been recommended to account for other aspects, which are the incomplete demagnetization of the transformer under CCM and the presence of the output filter. Their effects are now investigated. And in this part, it is assumed that the input capacitor C_{pv} is large enough so that its influence on power factor is negligible.



(a) Flyback-CCM converter (b) Output filter

Fig.3.13: Equivalent circuits for incomplete demagnetization effect and output filter

A. Incomplete Demagnetization's Effect

Firstly, it is assumed that the output filter component values, L_f and C_f are small enough such that the average output current I_o, and average output voltage V_o, of the inverter (see Fig.3.1) are nearly equal to the output current I_g and output voltage V_g respectively. In order to facilitate the analysis, an 'equivalent net transformer current reflected to the primary side', I_{Lm}, is defined as follows.

$$\begin{aligned} I_{Lm} &= I_{pri} \quad when\ M_1\ is\ on \\ &= nI_o \ when\ M_1\ is\ off\ and\ S_1\ on \\ &= -nI_o \ when\ M_2\ is\ off\ and\ S_2\ on \end{aligned} \tag{3-43}$$

The equivalanet circuit of the flyback converter in CCM operation is shown in Fig.3.13 (a). The average change rate of I_{Lm} over a switching period can be determined by considering the net volt-seconds across the inductor over a cycle. (Quasi-steady state operation is not assumed for this step.)

$$L_m \Delta I_L / T_S = L_m dI_L / dt = D \cdot V_{PV} - D' \left| V_o \right| / n \tag{3-44}$$

Here, D' = (1-D) is the duty ratio for the conduction of the secondary side diode. The average primary side current and the average output current can be written as:

$$I_{pri} = DI_L \ \ \& \ \ \left| I_o \right| = D' I_L / n \tag{3-45}$$

Combining (3-44) & (3-45), we get:

$$(L_m I_{pri} / D) \times d(I_{pri} / D) / dt = I_{pri} \cdot V_{PV} - \left| V_o \right| \cdot \left| I_o \right| \tag{3-46}$$

Since V_o and I_o will have to be in phase for the flyback inverter to work

properly,

$$(L_m I_{pri} / D) \times d(I_{pri} / D) / dt = I_{pri} \cdot V_{PV} - V_o \cdot I_o \quad (3\text{-}47)$$

The left-hand side of (3-47) represents the average power (rate of change in energy storage) in the magnetizing inductance during one switching cycle, while the right-hand side represents the difference between the input power and the output power over a switching cycle.

The peak energy stored in the magnetizing inductance E_L can be obtained by integrating left-hand side of (3-47) over an interval of one fourth of the AC cycle period.

$$E_L = 2L_m(nI_{rms} / \sqrt{2} + I_{pv})^2 \quad (3\text{-}48)$$

Given the PV panel and the grid voltage, the peak energy stored in the inductor is dependent on n and L_m. In typical designs of flyback-CCM inverter (e.g. $n = 4$ and $L_m = 20\mu H$ and for a given specification in Appendix A), this value is found to be very small (i.e. < 0.4%) when compared to the energy transferred to the output side over the same interval. Due to this, we can expect the output power factor not to be significantly affected by the energy storage in the magnetizing inductance.

B. Output Filter's Effect

With the effect of L_m neglected, the average output current I_o feeding into the output filter as shown in Fig.3.13 (b) can be represented by $\sqrt{2}I_{rms}\sin(\omega t)$. We assume in this part of the analysis that $\overline{V_g}$ is the reference phasor with zero phase

angle. The voltage $\overline{V}_o$ and current $\bar{I}_g$ can then be written as:

$$\overline{V}_o = \overline{V}_g(1 + j\omega L_f I_{rms}/V_{rms})/(1-\omega^2 L_f C_f) \tag{3-49}$$

$$\bar{I}_g = \overline{V}_g(I_{rms}/V_{rms} - j\omega C_f)/(1-\omega^2 L_f C_f) \tag{3-50}$$

Typically, $\overline{V}_o \approx \overline{V}_g$, since the voltage drop across the inductor L_f will be quite small. In our example, even if L_f is as high as 10 mH, the displacement factor between $\overline{V}_o$ and $\overline{V}_g$ will be above 99.995%. Therefore, it is difficult to control the grid current by controlling the output voltage vector $\overline{V}_o$.

Similarly, with the designed capacitance value of 0.9μF, the displacement factor between $\bar{I}_g$ and $\overline{V}_g$ is 99.7%, which is also neglible.

C. Summary of Effects on Power Factor

In summary, the incomplete demagnetization's effect of flyback transformer on output power factor is shown to be small and hence can be ignored. The displacement factor between the grid current and voltage due to the output filter has also been shown to be quite small. Thus, the only significant factor affecting the power factor is the third harmonics distortion in the grid current due to the PV voltage ripple. This will influence the choice of input capacitor, which has been discussed in Section 3.3.

3.5 Implementations and Experimental Results

The hardware implementations of the designed inverters involve the circuit design, components selection and considerations, which will be discussed in Section

3.5.1. Following that, the proposed flyback-CCM inverter and the benchmark flyback-DCM inverter were firstly tested in DC-DC conversion with a constant voltage load to work as current source inverters. The operating waveforms of flyback-CCM inverter are used as an example and are analyzed in Section 3.5.2. Finally, both inverters were tested in DC-AC conversion with an AC voltage load (for grid connection verification). Their operating waveforms and performance such as efficiency, power factor are compared and analyzed in Section 3.5.3.

3.5.1. Hardware Implementations

In the present work, a flyback inverter was designed for CCM operation for a power level of 200W for the Kyocera solar module KC200GT. Another flyback inverter was designed for DCM-only operation as a benchmark for the same specifications.

Table 3.2 gives the design parameters, components selection of both inverters as well as the respective current and voltage stresses at rated power. For the magnetic components, ferrite cores (Magnetics R material with the lowest loss at 100^{o}C) were used in this work. The resonant frequency of the output filter is 7 kHz which ensures adequate filtering of the switching frequency ripple component. The main difference between CCM and DCM inverters are flyback transformer design and the components used for secondary side diodes. For flyback-CCM inverter, SiC diode is used instead of fast switching Si diode so as to minimize the loss due to reverse recovery current during fast turning off interval. SiC diode is not needed for

DCM inverter since the diode is turned off at zero current every switching cycle and hence the reverse recovery loss does not occur. Besides, the conduction loss of the selected fast switching diode IDD03E60 and SiC diode IDT04S60C are comparable (both with a forward voltage drop of 1.5V at 3A). Thus, the substitution of silicon diode used in DCM inverter benchmark with SiC diode in CCM inverter is justified and the efficiency comparison between flyback-DCM inverter and the proposed CCM inverter is on a fair basis.

Table 3.2: Design of flyback-DCM and CCM inverters for given specifications: (V_{pv}=27V, P_{pv}=0 ~ 200W, V_{rms}=230V)

	CCM Inverter	DCM-Inverter
Operation parameters		
f_s (kHz)	100	100
$\hat{D}$	0.75	0.63
Transformer Design		
n	4	4
L_m (μH)	20	3
EE core	Magnetics 45528	Magnetics 44020
Primary (Litz: 72/28)	6 turns	3 turns
Secondary (Litz:12/28)	24 turns	12 turns
Component Selection and Circuit Design		
M1	FDP2614	FDP2614
S1,S2	IPP90R500C3	IPP90R500C3
D1,D2	IDT04S60C	IDD03E60
C_{pv} (μF)	4700 × 3	4700 × 3
C_f (μF)	0.9	0.9
L_f (μH)	480	480
Voltage and Current Stresses		
$\hat{I}_p$ (A)	24.8	51.6
$\hat{I}_s$ (A)	6.2	12.9
$\hat{V}_{M1}$ (V)	108.3	108.3
$\hat{V}_{d1,2}$ (V)	433.3	433.3
$\hat{V}_{s1,2}$ (V)	650.5	650.5

According to Table 3.2, the calculated current stresses both on the primary and the secondary sides are almost halved in the CCM inverter compared to DCM inverter, which shows a large potential in efficiency improvement.

3.5.2. DC-DC Conversion with DC Voltage Load

Operation of the flyback-CCM inverter was first tested in DC-DC conversion mode with presumed quasi-steady state within an AC cycle. In this test, the inverter output is connected to a DC voltage load (i.e. a DC power supply in parallel with a resistive load). In this way, the inverters worked as a current source inverter (at the output side), rather than a voltage source inverter.

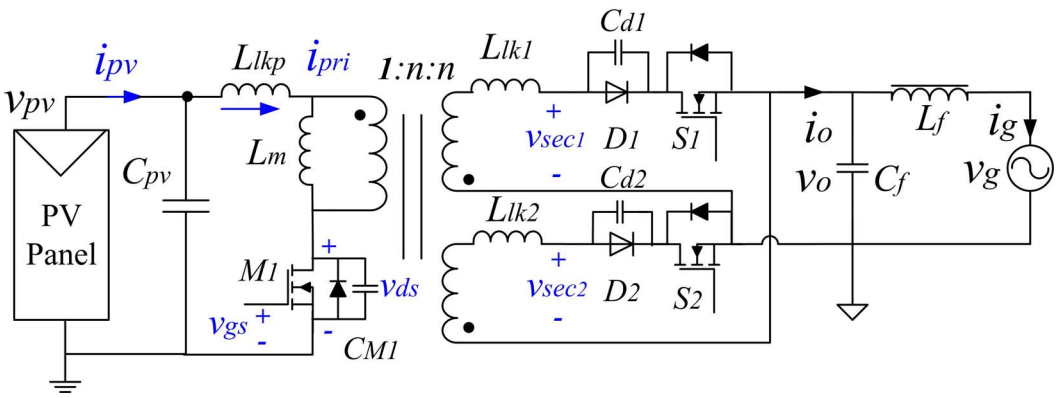
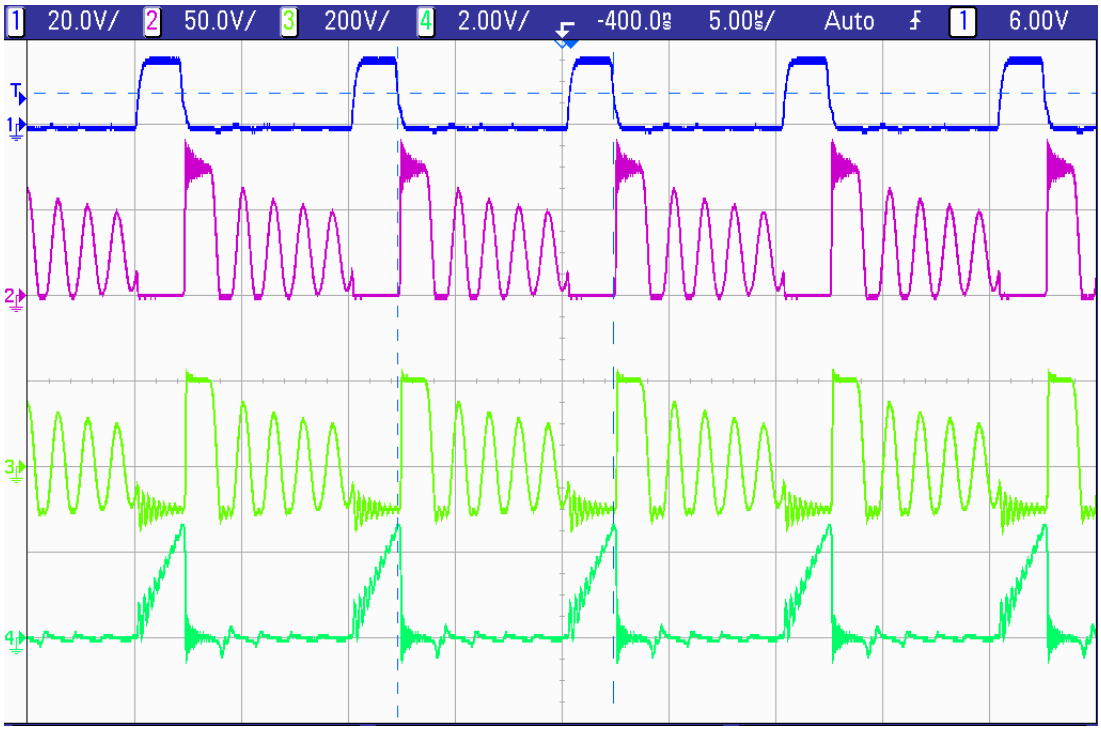
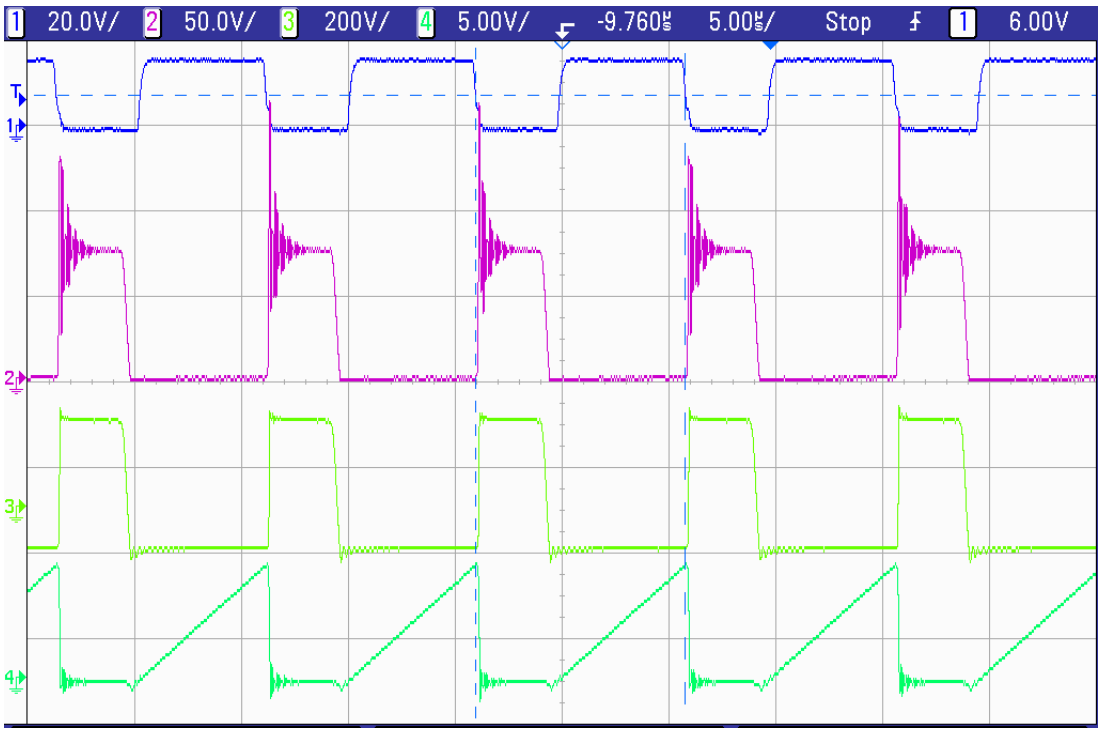


Fig.3.14: Flyback Inverter with parasitic components and measurement waveforms

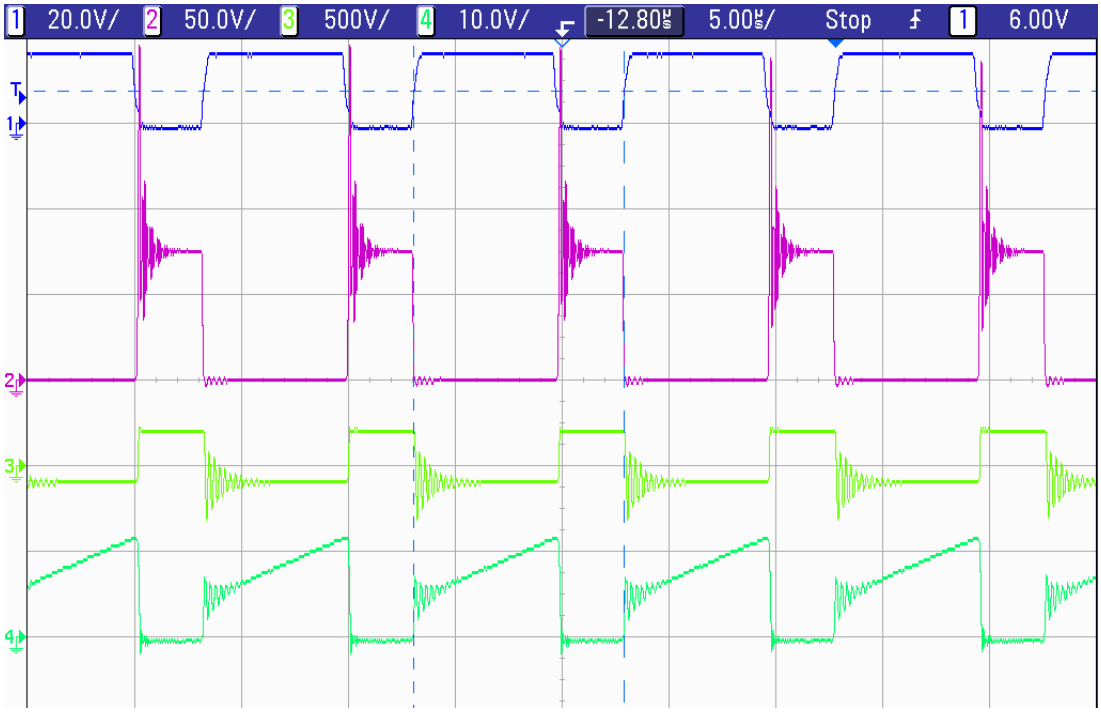
The typical waveforms in DCM, boundary conduction condition between DCM/CCM and CCM modes are illustrated in Fig.3.15. These waveforms are the gate signal v_{gs}, drain-source voltage v_{ds} of M1, the secondary side transformer voltage of the positive leg v_{sec1} and the primary side current i_{pri}, which are indicated in Fig.3.14. Besides, the equivalent circuit parameters and parasitic parameters of the flyback transformer are also shown in Fig.3.14 including the magnetizing inductance L_m (20μH), leakage inductance at primary side L_{lkp} (0.99μH) and at secondary side L_{lk1}/L_{lk2} (14.4μH). Other parastic components include parallel capacitance of the main switch M_1 and two diodes D_1/D_2.



(a) DCM operation $V_{pv} = 25V$, $V_g = 200V$, $D = 20.3\%$ (Ch1: v_{gs} ; Ch2: v_{ds} ; Ch3: v_{sec1} ; Ch4: i_{pri})



(b) Boundary conduction condition $V_{pv} = 25V$, $V_g = 200V$, $D = 60\%$ (Ch1: v_{gs} ; Ch2: v_{ds} ; Ch3: v_{sec1} ; Ch4: i_{pri} [1A/V])



(c) CCM operation $V_{pv} = 25V$, $V_g = 200V$, $D = 67.5\%$ (Ch1: v_{gs}; Ch2: v_{ds}; Ch3: $v_{\text{sec}1}$; Ch4: i_{pri})

Fig.3.15: Operation waveforms of flyback inverter without snubber circuit (positive leg)

The basic flyback operation is shown in Fig.3.15. When the main switch M1 is turned on, its drain source voltage v_{ds} reduces to around zero (actual voltage depends on conduction resistance). At this time, the secondary side diode (either D1 or D2) is subject to a negative voltage and hence is blocked. The primary side current i_{pri} increases. When the main switch M1 is turned off, its drain source voltage v_{ds} increases to input voltage. As the transformer magnetizing current can not be changed abruptly, D1 or D2 is turned on to demagnetize the transformer current.

Besides, it is also observed in Fig.3.15, that when the main switch M1 is turned on, ringing occurs on the transformer primary current i_{pri} and secondary side voltage $v_{\text{sec}1}$ (or $v_{\text{sec}2}$) in both DCM and CCM operations. This is due to a step

change applied to v_{ds} (Ch2 in Fig.3.15 (a) and (c)) during turn-on interval, which causes a resonance between the parasitic capacitance C_{d1} (or C_{d2}) of secondary diode and the leakage inductance L_{lk1} (or L_{lk2}) at the corresponding leg of the flyback transformer. In this case, there are two influencing factors, one of which is the voltage step change value of $v_{\sec 1}$ (or $v_{\sec 2}$) when M1 turns on, the other one is how fast M1 is turned on. For example, when $v_{\sec 1}$ (or $v_{\sec 2}$) reaches zero before turn on, there is no abrupt change. Therefore, no transient oscillation is observed as in Fig.3.15 (b). The turn-on speed of M1 is determined by the MOSFET driver.

When the main switch M1 is turned off, a large overshoot followed by ringing has also been noticed at the primary side current i_{pri} (Ch4) and the main switch drain-source voltage v_{ds} (Ch2). The reason is as follows: when M1 is turned off, the diode D1 (or D2) conducts, which applies a sudden voltage change across the transformer secondary side v_{sec1} (or $v_{\sec 2}$) from $-nv_{pv}$ to v_o. The applied secondary voltage is reflected on the primary side, which causes a resonance between the parasitic capacitance C_{M1} of M1 and the primary side leakage inductance L_{lk} leading to the observed oscillations. A fast turn-off of M1 would cause a larger overshoot. This overshoot would require selection of MOSFET with higher breakdown voltage. Therefore, a snubber circuit to reduce the overshoot as well as provide damping of the resonance is needed.

A third type of ringing at lower frequency is observed in the third interval of DCM operation as shown in Fig.3.15 a) after the current of the secondary side diode

reduces to zero. During this interval, both M1 and D1 (or D2) are off, resulting in a step change of transformer secondary side voltage from v_o back to zero. As a result, a major resonance occurs between L_m and equivalent capacitance (considering both C_{M1} and C_{d1} (or C_{d2})). This resonance shows up at both sides of flyback transformer, the magnitude of which is mainly decided by the voltage step change.

During the resonance in the third interval of DCM operation, when v_{ds} reduces to below zero due to a large voltage step change, it will make the body diode of M1 start to conduct negative current and clamp v_{ds} as well as flyback transformer primary side voltage. As a result, the primary side current waveform i_{pri} increases at the same slope v_{pv}/L_m with conduction period of M1. After the current becomes positive, the body diode of M1 is not conducting anymore and the third interval resonance as described above will continue. This reverse conduction of the main switch body diode is mainly caused by a large resonance voltage due to high voltage load at the output of flyback converter. It leads to current sensing issues using Current Transformer (CT), which will be addressed in Chapter 4.

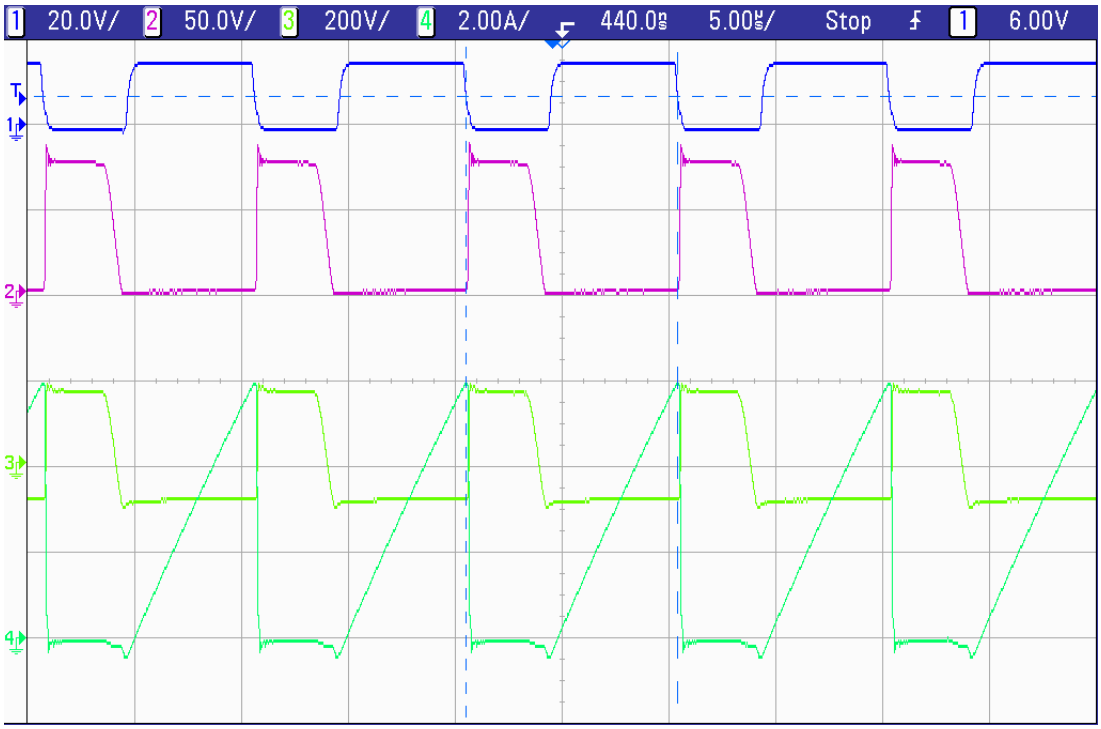
Table 3.3: Snubber circuits parameters for Flyback-DCM and CCM inverters

Inverters	Component	Snubber Capacitor	Snubber Resistors
DCM	M1	1500pF	16Ω
	D1,D2	-	-
CCM	M1	1200pF	50Ω
	D1,D2	330pF	362Ω

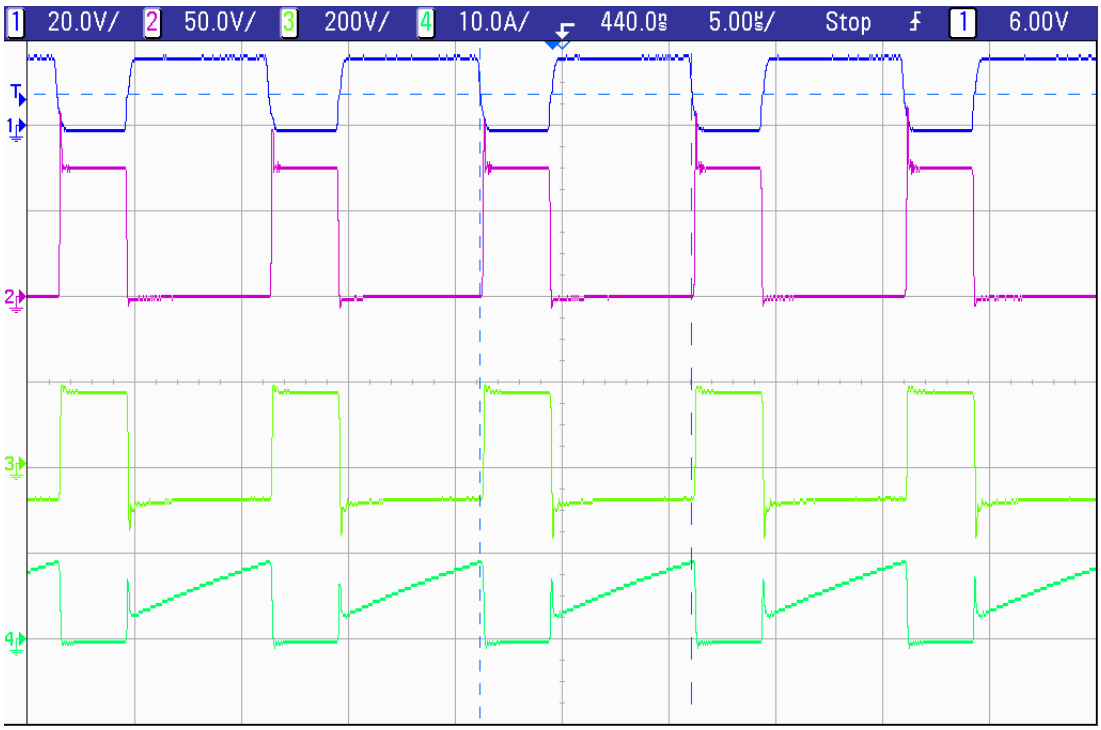
In order to remove the undesired ringing during turning on and turning off, RC dissipative snubber circuits are added in parallel with the main switch M1 as well as the secondary side diodes D1 and D2. The design procedure follows the rule of

thumb method outlined in [108]. The designed parameters for both flyback-CCM inverter and flyback-DCM inverter are given in Table 3.3.

(a) DCM operation $V_{pv} = 25V$, $V_g = 200V$, $D = 19.8\%$ (Ch1: v_{gs}; Ch2: v_{ds}; Ch3: v_{sec1}; Ch4: i_{pri})



(b) Boundary condition $V_{pv} = 25V$, $V_g = 200V$, $D = 60\%$ (Ch1: v_{gs}; Ch2: v_{ds}; Ch3: v_{sec1}; Ch4: i_{pri})



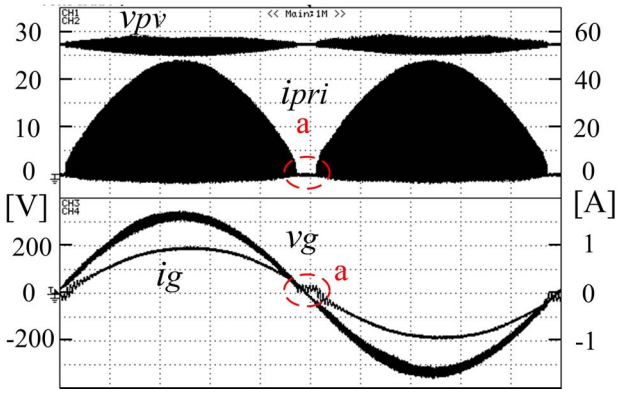
(c) CCM operation $V_{pv} = 25V$, $V_g = 200V$, $D = 66.2\%$ (Ch1: v_{gs}; Ch2: v_{ds}; Ch3: v_{sec1}; Ch4: i_{pri})

Fig.3.16: Operation waveforms of flyback-CCM inverter with snubber circuits

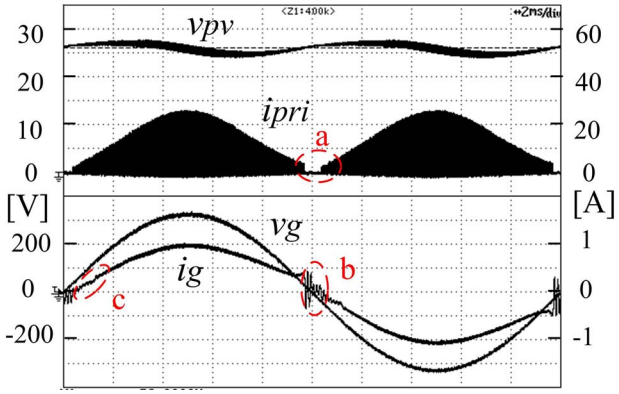
With dissipative RC snubber circuits, the operating waveforms of the flyback-CCM inverter at different operation modes are shown in Fig.3.16. These may be compared to the waveforms in Fig.3.15. The resonance in both turn-on and turn-off intervals are successfully eliminated with overshoot reduced as well. Besides, as shown in Fig.3.16 (a), the frequency of the third interval oscillation (when M1 and D1/D2 are off) in DCM operation is reduced and so does that of the negative current in i_{pri}.

As the dissipative snubber circuit is lossy, it is possible to reduce the ringing using soft-switched scheme or non-dissipative snubber circuit, which is not pursuit here.

3.5.3. DC-AC Conversion with AC Voltage Load



(a) DCM scheme



(b) Proposed CCM-ACM scheme

Fig.3.17: PV side and grid side waveforms with V_{pv}=27V, P_{pv}=200W

The input and output waveforms of the proposed flyback-CCM scheme and also the benchmark scheme at rated power are shown in Fig.3.17. More operating waveforms at different power level will be shown in Chapter 4. As expected, the peak primary current stress in the CCM scheme (25A) is around half of that in the DCM scheme (48A), which agrees with the calculated values in Table 3.2.

As shown in Fig.3.17, distortion of current waveforms in both DCM-only and CCM schemes is noticed around the zero crossing intervals. This is partly caused by a dead time (‘a’) when the AC current goes through zero and the secondary side

operation switches from S1 to S2 and vice versa. Another reason is due to the inability of the PWM IC (SG3524 here) to reach very low duty cycle values. Besides, in CCM, because of the tracking delay of the controller as well as the incomplete demagnetization of the flyback transformer, the secondary side current in Fig.3.17 (b) does not fall to zero during switching between S1 and S2, which makes the output current experience a sudden change，thereby causing oscillation ('b') at the output filter resonant frequency. The distortion at zero-crossing point is found to be the main contributor for THD of output current in both schemes, which makes the THD value of both schemes close to the limit of 5%. This can be improved using discrete comparator to generate small duty cycles around the zero-crossing points. Additionally, when the operation varies between DCM and CCM, the tracking capability of the controller changes. It is reflected as a distortion ('c') in the output current waveform. The conversion efficiency, output power factor and THD of grid current at different power levels were tested using Yokogawa 2531 Digital Power Meter and tabulated in Table 3.4.

Table 3.4: Performance measurement at various power levels ($V_{pv} = 27V$, $P_r = 200W$)

	Para.	5%	10%	20%	30%	50%	75%	100%	η^{*}_{Euro}	η^{**}_{CEC}
DCM	η_i	73.3%	78.4%	80.4%	80.6%	80.1%	79.0%	77.7%	79.4%	79.4%
	PF	0.44	0.72	0.91	0.95	0.98	0.99	1.00	-	-
	THD	8.6 %	8.86 %	8.94%	8.68%	5.58%	4.39%	4.19%	-	-
CCM	η_i	72.9%	79.2%	85.4%	86.2%	88.0%	88.3%	87.4%	86.4%	87.4%
	PF	0.48	0.72	0.88	0.94	0.98	0.99	0.99	-	-
	THD	20.2%	7.6%	4.2%	4.0%	3.8%	3.4%	4.4%	-	-

* $\eta_{Euro} = 0.03 \cdot \eta_5 + 0.06 \cdot \eta_{10} + 0.13 \cdot \eta_{20} + 0.10 \cdot \eta_{30} + 0.48 \cdot \eta_{50} + 0.20 \cdot \eta_{100}$

** $\eta_{Euro} = 0.04 \cdot \eta_{10} + 0.05 \cdot \eta_{20} + 0.12 \cdot \eta_{30} + 0.21 \cdot \eta_{50} + 0.53 \cdot \eta_{75} + 0.05 \cdot \eta_{100}$

At rated power, the total harmonic distortion (THD) is 4.37% for the DCM

scheme and 4.4% for the CCM scheme, while the power factor (PF) is 0.995 and 0.991, respectively. Both the schemes satisfy the requirements of IEC61727 in this regard.

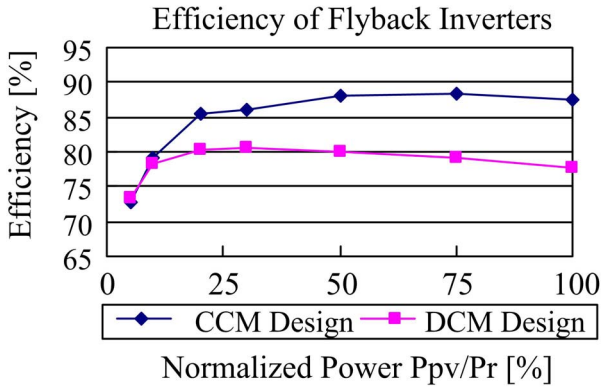


Fig.3.18 Efficiency vs. normalized power (referred to rated power of 200W) for the DCM and CCM scheme

Fig.3.18 shows the marked improvement in efficiency achieved with the proposed CCM scheme over the benchmark DCM scheme. The weighted efficiencies for the solar powered inverter, i.e. European efficiency and California efficiency [81] were found to be 86.4% and 87.4% respectively for the CCM scheme and 79.4% and 79.4% for the DCM scheme. Thus, the proposed CCM approach results in significantly higher efficiencies while still maintaining output current distortion within limits.

3.6 Conclusions

In this chapter, a popularly used flyback inverter has been thoroughly studied in both DCM and CCM operations to provide meaningful insights into the behavior of the designed inverter at different power levels. The design procedure and considerations have been discussed in details. The effectiveness of the proposed

flyback-CCM inverter to improve the conversion efficiency of a benchmark flyback-DCM inverter for a medium power level PV module has been verified experimentally.

However, when operated in CCM, the flyback converter suffers from a RHP (Right Half Plane) zero in the output current control, which, together with other problems, may have prevented its usage in AC module application. Therefore, these control challenges in flyback-CCM inverter schemes will be fully investigated in Chapter 4.

As discussed in Chapter 2, the major concern in this type of inverter lies in the usage of electrolytic capacitor, which is believed to place the limit for overall system lifetime. Although some commercial products still use the controversial electrolytic capacitor due to the reasons discussed in details in Section 2.3, the trend in both academia and industry is to use film capacitor instead. For the benchmark flyback-DCM inverter, a variety of power decoupling circuit has been studied in [34-36, 98, 104]. However, it is noted that all the power decoupling schemes require additional power processing, hence consume more power loss. In addition, these schemes, including the active filters schemes [70, 98, 104] that can be applied to other topologies are mostly placed at low voltage input side. As a result, larger current is processed which is not good option in terms of efficiency. The achievement of both high efficiency and active power decoupling leads to the second proposed scheme, which will be described in Chapter 5.

CHAPTER 4: CONTROL STRATEGIES FOR THE FLYBACK-CCM INVERTER

4.1 Introduction

The control of a microinverter needs to fulfill two basic requirements, viz., MPPT capability required by PV application, and output current shaping and synchronization required by the grid connection. In a single stage inverter such as the flyback inverter discussed in Chapter 3, the control is usually implemented by a dual loop scheme wherein a fast inner control loop tracks the line frequency waveform and a slow outer loop ensures that the operation is maintained at the MPP of the PV module. In general, the adopted MPPT scheme [109, 110], such as the Perturb & Observe method, Incremental Conduction method or the Ripple Correlation method, does not depend much on the inverter scheme adopted. The challenges of the control design for the inverter scheme lie in the output current shaping and these are addressed in this work.

Although designed to operate in CCM at rated power level, the flyback inverter would, in most cases, slip into DCM operation at low instantaneous voltages around the zero-crossing instants of the AC cycle. Thus, in reality, the inverter would operate in a combined CCM/DCM mode over an AC cycle. Moreover, the large variation of power produced by a PV panel due to varying incident radiation would make the combined DCM/CCM operation even more complex. For instance, complete operation in DCM region alone can take place at low power levels.

Therefore, the design of a controller which can take care of the variations in grid voltage, power level and operating modes needs careful consideration.

This chapter is organized as follows. Firstly, the current control techniques commonly used for current tracking in Power Factor Correction (PFC) application are discussed in Section 4.2. The control challenges for direct output current control using Average Current Control (ACC) and One Cycle Control (OCC) are briefly discussed in Section 4.3. In order to address the issues arising in the control of flyback-CCM inverter, an indirect current control scheme is proposed. Two implementations of indirect controller have been investigated. These are described in Section 4.4. After that, the current sensing method used in both controllers is presented in Section 4.5. Simulation and test results for both the proposed indirect current controllers are presented and analyzed in Section 4.6.

4.2 Potential Current Control Techniques

Output current control at twice AC line frequency (100Hz) for microinverter is similar to input current control requirement in PFC application. Conventional current control methods found in PFC application [111] include peak current control, average current control (ACC), hysteresis control and one cycle control (OCC). Among them, peak current control was used in earlier years due to its fast tracking performance (capable of tracking in one switching cycle implementaed by analog circuit). However, as the peak current, not the actual average current is used as feedback signal, there will be an inherent distortion between the controlled current

waveform and the reference signal[111]. Besides, slope compensation is required if the duty cycle goes beyond 50% so as to prevent instability. The technique is also sensitive to switching noise, which requires careful circuit layout and noise filtering. Average Current Control (ACC) is the most commonly used technique nowadays, which is targeted at controlling the actual average current to track the reference waveform. It is less sensitive to switching noises due to current signal filtering and provides reasonably good tracking performance. Hysteresis current control is capable of tracking the reference signal within a pre-determined hysteresis band. However, the switching frequency varies over a line AC cycle with this method, which leads to complexity in output filter design. One Cycle Control (OCC) [112], named so for its fast tracking capability (ability to reach the desired average control within one switching cycle) is well suited for PFC application due to its simple implementation and fast dynamic performance.

The two control methods chosen for the flyback-CCM inverter under investigations are OCC and ACC. Both the methods operate at constant frequency and control the average current. OCC has been selected due to its potential for fast response. Compared to OCC, Average Current Control (ACC) has lower achievable system bandwidth and is slower in terms of dynamic performance. Yet, it is the most popularly used linear controller in a PFC application. It represents a mature technology providing acceptable performance. In this study, both control schemes, i.e. OCC (nonlinear control) and ACC (a linear control) are investigated and compared, with the challenges identified and addressed in the following sections.

When flyback converter is used in a PFC (Power Factor Correction) application, the input current of the converter is usually directly controlled and shaped. In a flyback PV inverter, however, it is the flyback's output current that is to be controlled and shaped. This turns out to be a more challenging control problem, which will be investigated in the next section.

4.3 Problems with Direct Control of Output Current

For grid-tied inverters such as a microinverter, the most obvious way to shape the AC output current is to control the output current directly through feedback. However, it is well known that the flyback converter in CCM operation is a non-minimum phase system [113] which places stringent limits on closed loop dynamic performance. This non-minimum phase behavior shows up as a Right Half Plane zero in the linearized, small signal control to output current transfer function which introduces an additional 90^o phase lag while contributing to a gain increase. It would greatly limit the achievable system bandwidth to be below the RHP zero and can be expected to make the direct current tracking difficult. In this section, the problems with direct output current control using both ACC and OCC are discussed briefly. More details of the design considerations and procedure are available in Appendix B.

4.3.1. Problem with Direct One Cycle Control (DOCC)

A typical OCC circuit consists of a Current Transformer (CT), a diode in series

with a switched capacitor (CT, D_C, C_C and S_C) and an RS flip flop, as shown in Fig.4.1. The basic idea of OCC is to sense the instantaneous current waveform in each switching cycle (for example, using a CT) and integrate the waveform, say using a capacitor. In this way, the capacitor voltage represents the actual average current. Once this voltage reaches a preset reference value, the switch S_C across the capacitor will be turned on to discharge the capacitor and wait for the next switching cycle.

In the beginning, an attempt was made to directly control the secondary side current using Direct One Cycle Control (DOCC) method. The DOCC scheme was implemented as shown in Fig.4.1 and simulated using Simulink/PLECS. In the scheme, two CTs are used to sense the 'net' secondary side current of the flyback converter. The MPPT circuit (not implemented here) generates the factor k_m which determines the magnitude of the output current reference signal v_{iref}, while the shape of the signal v_{iref} is determined by the rectified AC voltage waveshape. A fixed frequency clock generates a pulse to turn off the main MOSFET M1 and the capacitor switch S_C. The current sensing signal starts to charge the capacitor C_C until it reaches the value of the reference signal v_{iref}. This triggers the RS flip flop, whose output is used to turn on the main MOSFET M1 and the capacitor switch S_C. The turning on of the switch Sc discharges the capacitor C_C to zero voltage and the system waits for the next cycle.

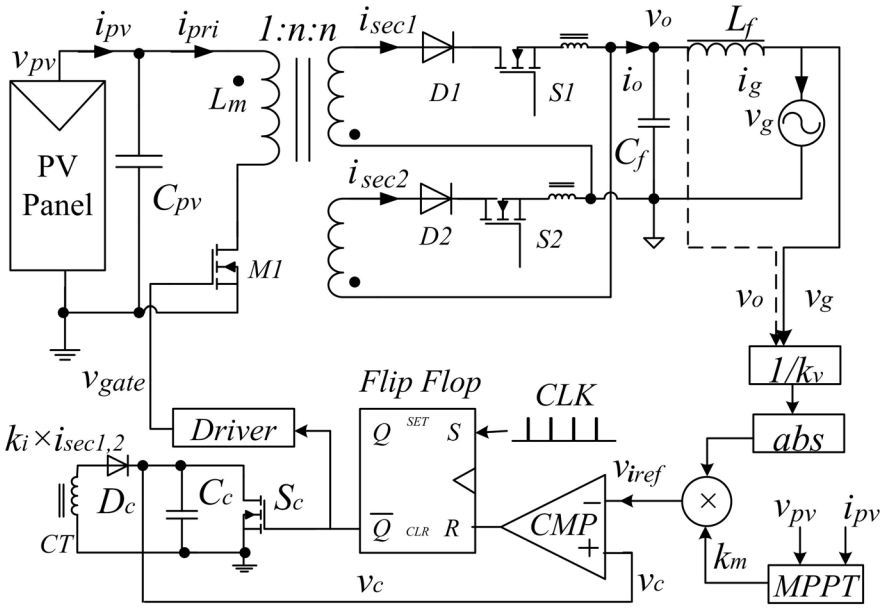


Fig.4.1: Circuit diagram of DOCC

The simulation results are shown in Fig. 4.2. Even though the grid current is bounded and largely follows the sinusoidal reference, the primary side current, i_{pri}, is unstable and increases in an uncontrolled manner, which is unacceptable.

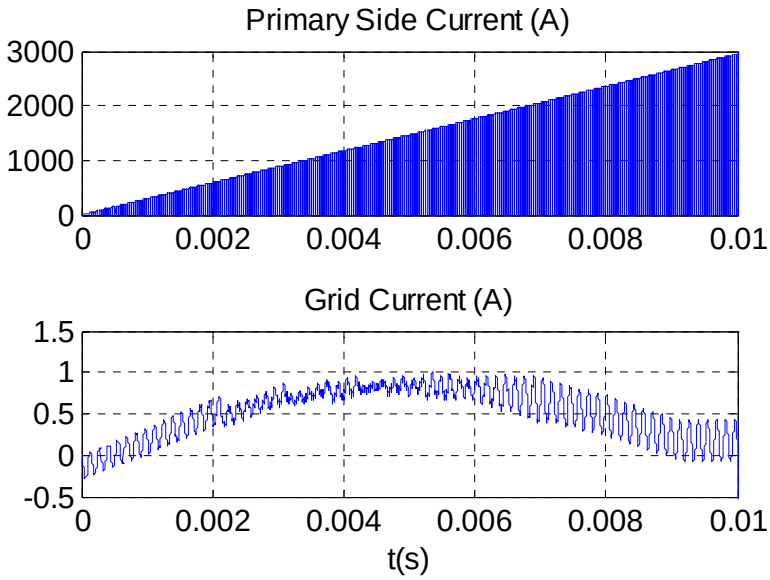


Fig.4.2: Instability of DOCC ($n = 4$, $L_m = 20\mu H$, $V_{pv} = 27V$, $V_{rms} = 230V$)

It is found that the transformer is incompletely demagnetized in one switching cycle in CCM operation. As a result, primary side current build up occurs, which, in a

practical implementation would lead to eventual failure of the components in the circuit. A detailed analysis of this issue can be found in Appendix B.2.

Thus, it is concluded that Direct One Cycle Control is not a viable option as a control method in this application.

4.3.2. Problem with Direct Average Current Control (DACC)

In this section, we investigate the issues involved in directly controlling the secondary side current through ACC method.

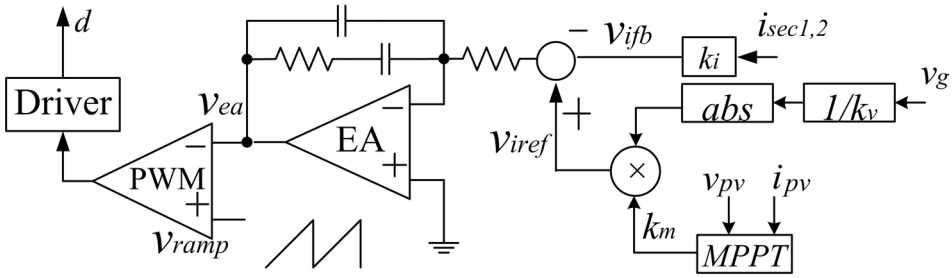


Fig.4.3: Control circuit diagram of DACC scheme

The control scheme adopted is shown in Fig.4.3. As with the DOCC scheme discussed above, the reference current signal is v_{iref}, which is shaped by the grid AC voltage waveform and is in phase with it. The magnitude of v_{iref} is determined by the MPPT. The feedback current v_{ifb} is obtained by sensing the two secondary side currents $i_{\text{sec1,2}}$. The error between the reference v_{iref} and the feedback variable v_{ifb} is fed to the average current controller whose output determines the duty cycle of M_1. A separate averaging filter for the current feedback signal, v_{ifb} is not needed since the current controller, whose gain is very low at the switching frequencies, will act to filter out the switching frequency components.

Due to the existence of RHP (Right Half Plane) zero in the transfer function relating duty ratio to the secondary side current in CCM operation, the bandwidth of the control loop is limited. As indicated earlier, the system operating point varies widely due to both the grid voltage variation over an AC period and to varying power levels due to irradiation changes, resulting in large changes in the RHP zero location. A controller designed to accommodate the worst case RHP zero, which occurs at the peak of AC voltage under maximum load, was found to result in unacceptably low bandwidth (even lower than 100 Hz) when the operation changes to DCM under low instantaneous voltages during the AC cycle. Thus the widely varying RHP zero in CCM operation results in poor tracking performance in the DCM operating zones and hence unacceptable output power quality. Due to this, the inverter was found to be unable to track the reference in DCM operation. The design considerations and procedure are discussed in detail in Appendix B.3. One example of the simulation waveforms is given in Fig.4.4.

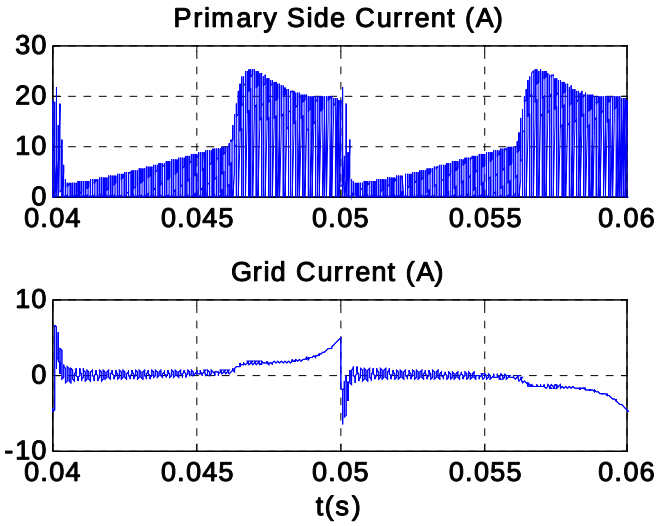


Fig.4.4: A typical waveform of DACC ($n = 4$, $L_m = 20\mu H$, V_{pv}=27V, V_{rms}=230V)

As shown in Fig.4.4, the flyback inverter works in DCM when starting from the

zero crossing instant. Sudden changes of the primary side current waveform are observed at around 0.046s and 0.056s; these are caused by the transition from DCM to CCM operation. In DCM operation, the inverter fails to track the reference signal because of the low gain at low frequency and limited system bandwidth as predicted from the analysis. On the one hand, the transition from DCM to CCM operation is greatly delayed due to the slow response in the DCM region. On the other hand, the accumulated error in the DCM region is carried forward, causing an overshoot when CCM operation starts. This, in turn, unexpectedly increases the magnetizing current of the flyback transformer. As a result, around the grid zero-crossing intervals, the flyback-CCM inverter is unable to demagnetize its current completely and keeps working in CCM, instead of in DCM.

Overall, the grid current is unable to track sinusoidal grid voltage. Hence, the Direct Average Current Control of the output current is also not seen as a viable option in this application.

4.4 Proposed Indirect Current Control Strategy

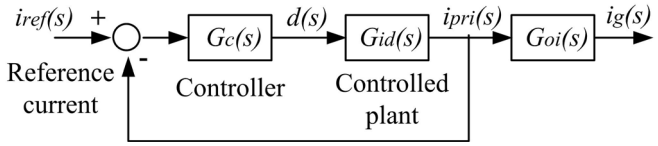


Fig.4.5: Indirect Current Control Diagram

As discussed above, direct current controller design needs to consider the RHP zero in CCM. Such a controller, when used in DCM, will result in poor tracking performance.Therefore, in this work, an indirect current control method is proposed, in which the primary current is sensed and controlled (Fig.4.5) rather than the output

current. The primary current reference signal's magnitude is determined by an external MPPT scheme and its shape is determined by the sensed instantaneous grid voltage by assuming input-output power balance in each switching cycle. As a result, the output current is controlled in an indirect, open-loop manner. Since no RHP zero exists in the control to input current transfer function[114], the problem discussed in Section 4.3 is completely avoided. Based on the study of influence of CCM operation on the output power factor (in Section 3.4.4), this approach is not expected to cause significant distortion problems in the output current waveform.

The same two current controllers studied in Section 4.3 and Appendix B for the direct output current control, viz., OCC and ACC were implemented here. One is a nonlinear control method, OCC, which is capable of a fast dynamic response. The other one is a linear control, ACC, which can potentially give an acceptable tracking performance without stability issues. These two schemes are discussed in Sections 4.4.1 and 4.4.2 respectively.

4.4.1. Indirect OCC Scheme

The proposed scheme based on an Indirect OCC for controlling the primary side current of the flyback-CCM inverter is shown in Fig.4.6. As mentioned in Section 4.3.1, OCC circuit is comprised of a current transformer (CT), a diode D_C, a charge switch S_C, a charge capacitor C_C and an RS flip-flop shown in Fig.4.6. The basic idea behind the OCC is that the perfect tracking of the reference signal can be realized in each switching cycle and no design of compensator is needed.

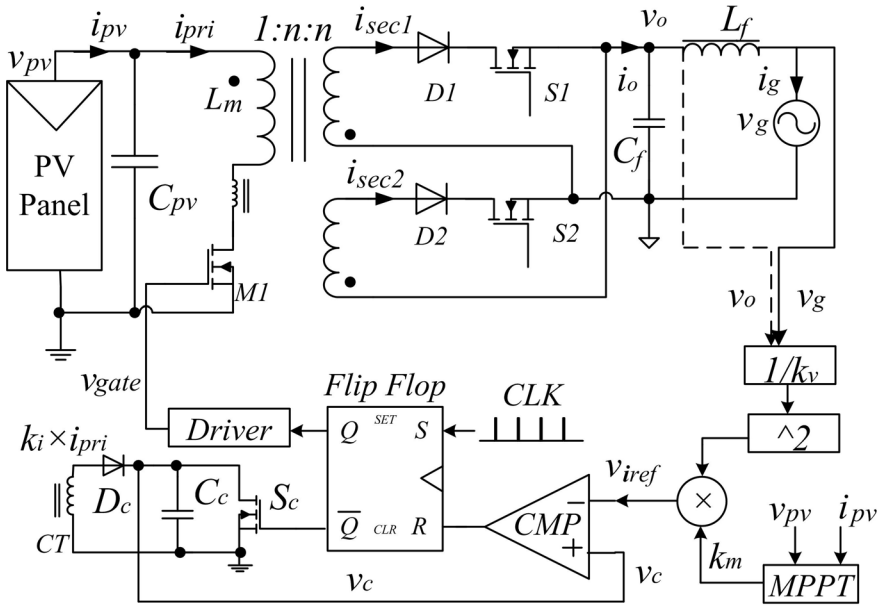


Fig.4.6: Schematic diagram of the proposed IOCC scheme for flyback-CCM inverter

As shown in Fig.4.6, current sensing circuit using CT is placed in series with the main switch M1 in the proposed Indirect OCC at primary side. At the beginning of each switching period, M1 is turned on as determined by a switching frequency clock pulse. At the same time, the charge switch S_C is turned off after momentarily resetting the charge capacitor C_C. The primary current increases and is sensed by a CT (Current Transformer), whose output is fed into the charge capacitor C_C which works as a current integrator. Hence, with a constant switching period, the peak capacitor voltage, $\hat{v}_C$, is proportional to the average primary side current in each switching cycle. Thus,

$$\hat{v}_C = \int_0^{DTs} k_i i_{pri} dt / C_C = k_i I_{pri} / C_C f_s , \tag{4-1}$$

Once the peak capacitor voltage $\hat{v}_C$ reaches the desired value v_{iref}, the flip-flop turns the switch M1 off and at the same time turns on the charge switch S_C to discharge the capacitor C_C. Thus, the average value of the primary current in each switching cycle will be determined by voltage reference v_{iref}. Here, the magnitude of

the reference v_{iref} is determined by MPPT while the shape of its waveform follows the square of the sensed sinusoidal grid voltage based on instantaneous power balance equation as (assuming that MPPT has been reached)

$$v_{iref} = \frac{2v_g i_g}{V_{mp}} = k_m \cdot \left(\frac{v_g}{k_v} \right)^2 \tag{4-2}$$

The capacitance of the charge capacitor C_C can be derived by making (4-1) equals (4-2). Other parameters such as k_m, k_v and k_i are based on scheme implementation.

4.4.2. Indirect ACC Scheme

In this section, an Indirect ACC scheme with primary side current feedback and control is investigated for the designed flyback-CCM inverter. Firstly, the small signal modeling of the plant and the variation of the plant transfer functions are discussed in Section 4.4.2.1. Detailed design procedure of the Indirect ACC scheme with considerations of the large variation due to microinverter application is discussed in Section 4.4.2.2. Following the suggested procedure, a controller has also been designed for the Flyback-CCM inverter designed in Chapter 3 and implemented for performance verification.

4.4.2.1. Small Signal Modeling of Flyback Inverter

Although the flyback inverter discussed in Chapter 3 is a time-varying nonlinear system, it is simplified as a time-invariant linear system by treating it to be

in 'quasi steady state' around each instant of the AC cycle. This is justified due to the relatively slower variation of the AC waveform in comparison to the switching frequency [115]. Due to the variations in output power and instantaneous grid voltage, a set of transfer functions are needed to model all possible operating conditions. The controller design must ensure that the current tracking performance is good and that the close-loop system is stable under all different conditions. The equivalent circuit of the flyback inverter under study is illustrated in Fig.4.7.

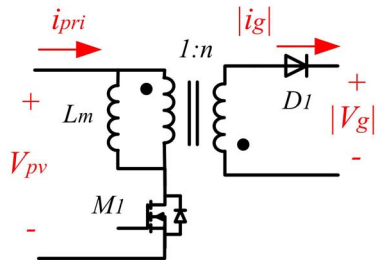


Fig.4.7: Equivalent Circuit of Flyback Inverter for Small Signal Modeling

First of all, it is assumed that the inverter operates ideally without parasitic effects. In order to ensure flyback operation, the output current of flyback converter needs to be with the same polarity of output voltage. Besides, due to the small output current magnitude of microinverter, the voltage drop on the filter inductor is ignorabe. Therefore, as a grid-tied inverter, the output side load of the flyback converter is taken as a voltage sink load with a fixed voltage $|V_g|$. This assumption will be reconsidered in Section 4.6.2.2 while reviewing the test result of the actual system loop gain.

Based on the above assumptions, the plant transfer function $G_{id}(s)$ is derived in terms of power level and grid voltage variation.

According to the quasi-steady state analysis in Section 3.4.1, the proposed flyback-CCM inverter will normally work in combined DCM/CCM operation when the grid voltage or power level changes. For a given inverter design, the boundary grid voltage V_{gb} at which DCM/CCM transition occurs has already been derived in Section 3.4.1 for a given power level, P_{pv}, which is:

$$V_{gb} = V_{pv}(V_{rms}\sqrt{\frac{1}{2P_{pv}f_s L_m}} - n) \tag{4-3}$$

when $|V_g| < V_{gb}$, the inverter works in DCM. In this mode, the quasi-steady state operation has been given by equation (3-20).

Let us assume that a small signal disturbance is added to the quasi-steady state operating waveforms. By replacing D_d & I_{pri} in equation (3-20) by $\overline{D}_d + \widetilde{d}_d$ & $\bar{I}_{pri} + \widetilde{i}_{pri}$ and substituting the quasi-steady state duty cycle $\overline{D}_d$ by equation (3-21), the small signal control-to-primary side current transfer function in DCM can be obtained as:

$$G_{id\_DCM} = \frac{|V_g|}{V_{rms}}\sqrt{\frac{2P_{pv}}{L_m f_s}}\,. \tag{4-4}$$

The transfer function is a simple gain which tends towards zero as the instantaneous grid voltage $|V_g|$ goes towards zero.

When $|V_g| > V_{gb}$, the flyback inverter works in CCM. The small signal control-to-primary side current transfer function [114] is given by:

$$G_{id\_CCM} = \frac{\widetilde{i}_{pri}}{\widetilde{d}_c} = \frac{|V_g|}{nsL_m} + I_{Lm}\,, \tag{4-5}$$

where I_{Lm} represents the switching average current of the magnetizing inductance of the flyback transformer. Using I_{Lm} in equation (3-36) together with the quasi-steady state instantaneous power balance equation (3-18) and the duty cycle equation (3-22), this average current can be derived as:

$$I_{Lm} = \frac{I_{pri}}{D_C} = \frac{\left(|V_g| + nV_{pv}\right)}{V_{pv}} I_g \tag{4-6}$$

Substituting (4-6) and the power balance equation (3-17) into (4-5), the small-signal control-to-primary current transfer function can be obtained in terms of the specifications and converter design as:

$$G_{id\_CCM} = \frac{|V_g|}{nsL_m}(1 - s/s_z) \tag{4-7}$$

$$\text{where } s_z = -\frac{V_{rms}^2 \cdot V_{pv}}{P_{pv} \cdot nL_m \cdot (|V_g| + nV_{pv})} \ . \tag{4-8}$$

According to (4-7) and (4-8), the control-to-primary current transfer function has a pole at origin followed by a varying LHP (Left Half Plane) zero. The variation of the low frequency gain (at $2f_{ac} = 100Hz$) and LHP zero variations over half an AC cycle at four different power levels are illustrated in Fig.4.8. Here, we consider the gain at $2f_{ac}$ since the fundamental of the current reference waveform to be tracked is at a frequency of $2f_{ac}$.

It is observed that the gain at 100 Hz in CCM mode is only related to grid voltage, while the LHP zero varies with both power and grid voltage. Compared to the DCM case, flyback converter in CCM operation has much larger gains at 100Hz at the cost of a smaller phase at lower frequencies. Due to these differences, the design of a

single controller to accommodate both operating modes requires a careful trade-off between tracking performance in DCM operation and stability in CCM operation.

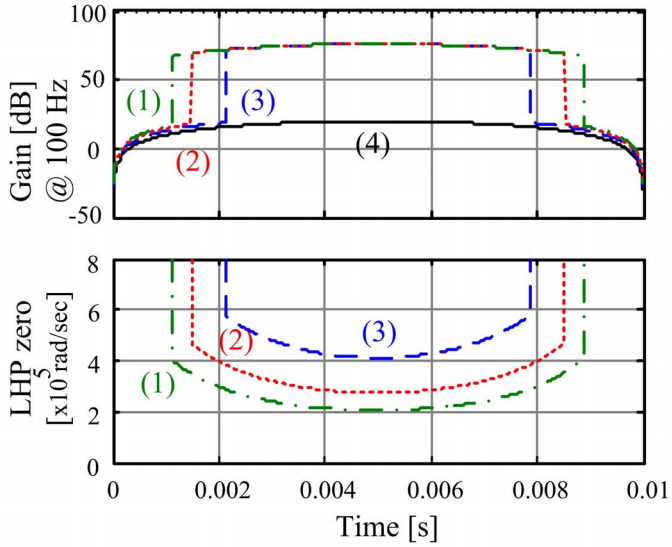


Fig.4.8: Variation of gain (at $2f_{ac} = 100Hz$) and LHP zero with power level of (1) 100%, (2) 75%, (3) 50% and (4) 25% (DCM-only, no LHP zero) at rated power $P_r = 200W$

In order to simplify the controller design process, a few critical plant operating conditions are chosen as reference conditions. The bode plots of selected reference plants are shown in Fig.4.9 .

In CCM operation, at the transition instant between DCM and CCM modes, the smallest 100 Hz gain and the largest LHP zero (see Fig.4.8) occur together. When the PV power is reduced, both the gain at 100 Hz and the LHP zero reduce at the CCM/DCM transition instant, introducing a series of such 'worst case' operating points. Of these cases, the ones under the maximum and minimum power levels are used as the plant references (curves 'A' and 'B' in Fig.4.9). All the other boundary operating cases at other power levels are within the range defined by these two curves. The minimum power level for the designed flyback inverter to work in CCM operation is given by:

$$P_c = \frac{1}{2L_m f_s} \cdot \frac{1}{\left(n/V_{rms} + \sqrt{2}/V_{pv}\right)^2} \tag{4-9}$$

In DCM case, the performance (here, gain as given by (4-4)) becomes poorer as the grid voltage V_g reduces and also as the power level P_{pv} decreases. There is, in fact, no way to compensate for this fully. In our design, operation at full power with a small grid voltage of 10V is considered as a reference case, curve 'C' in Fig.4.9. Though the tracking performance will be poorer at lower voltages and lower power, the main aim is to keep the resulting overall current distortion within acceptable limits at rated power.

The design of Indirect ACC scheme to deal with the varying transfer functions discussed in this part will be presented in the next section.

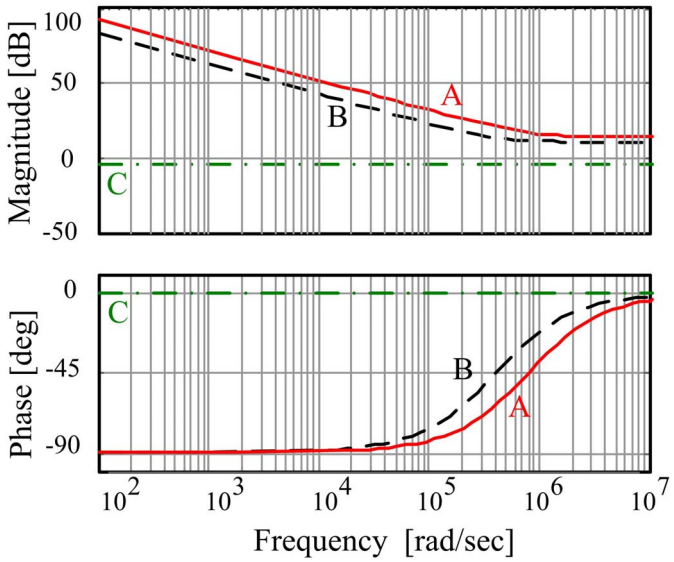


Fig.4.9: Plant references ('A': worst case in CCM at P_c; 'B': worst case in CCM at P_r; 'C': DCM at P_r and $V_g = 10V$)

4.4.2.2. Design of Indirect ACC

The control diagram for the Indirect ACC is illustrated in Fig.4.10, where the primary side current, i_{pri}, (instead of the secondary side current in the Direct ACC discussed in Section 4.2.2) is sensed and compared to current reference signal v_{iref}. The ACC controller implemented in Fig.4.10 by an error amplifier (EA) together with a compensation network, is used to minimize the error between v_{ifb} and v_{iref}. The current reference signal is the same (4-2) as used with the Indirect OCC scheme discussed in Section 4.4.1. The design procedure and considerations of the Indirect ACC are given below.

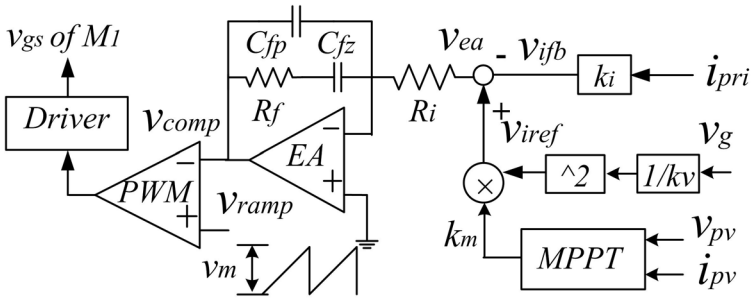


Fig.4.10: Proposed CCM control scheme based on Indirect ACC

Based on the plant transfer functions obtained in Section 4.4.2.1, a type II compensator is chosen for the design.

$$G_C = \frac{k}{s} \cdot \frac{s+z}{s+p} \tag{4-10}$$

The effect that this controller has on the open-loop bode plot of the system is illustrated in Fig.4.11. This controller (curves 'G_{C1}' and 'G_{C2}' in Fig.4.11), is essentially a PI controller together with a single pole filter for the averaging of the current waveform. The integrator increases the low frequency gain and the system

bandwidth in DCM (curve 'C' in Fig.4.11). However, as indicated by curves 'A' and 'B' in Fig.4.11, a pole already exists at origin for the flyback in CCM mode. Together with the controller's integrator, this creates a total phase change of -180^o in the system open loop response at low frequencies. Therefore, in order to provide an adequate phase margin at crossover frequency in CCM, the zero is needed in the compensator, followed by a pole for filtering the high frequency switching components.

The controller is first designed to ensure stability in CCM with as large a bandwidth as is practicable; its performance in DCM is then verified. Also, in Fig.4.11, the poles, p_1 and p_2, have been located at convenient locations so as to make the design ideas visually clearer; they do not correspond to the actual designed controller.

1. Choice of k:

A high k value (see Fig.4.11) is desired to ensure a high gain at twice the line frequency ($2f_{ac}$) and wide bandwidth, especially in DCM operation. However, to prevent bifurcation from occurring, the compensator output, v_{comp}, in Fig.4.10 needs to intersect the ramp signal v_{ramp} once every switching cycle. To ensure this for the primary current control of flyback converter, the upslope of v_{comp} ($= k \cdot V_m \cdot I_{pri}$) must be smaller than the upslope of v_{ramp}, ($= V_m / T_s$) [114]. Therefore, this limit can be expressed as:

$$k < \frac{f_s}{I_{pri}}. \tag{4-11}$$

Equation (4-11) provides an upper limit for k depending on the maximum value of I_{pri}, which occurs at the peak grid voltage and full power. A margin should be provided in the value of k to account for parameter variations. A second upper limit on k is imposed so as to keep the largest loop bandwidth to be less than $f_s/2$, as required by sampling theory. In practice, the largest bandwidth is made even less (say，less than $f_s/4$)

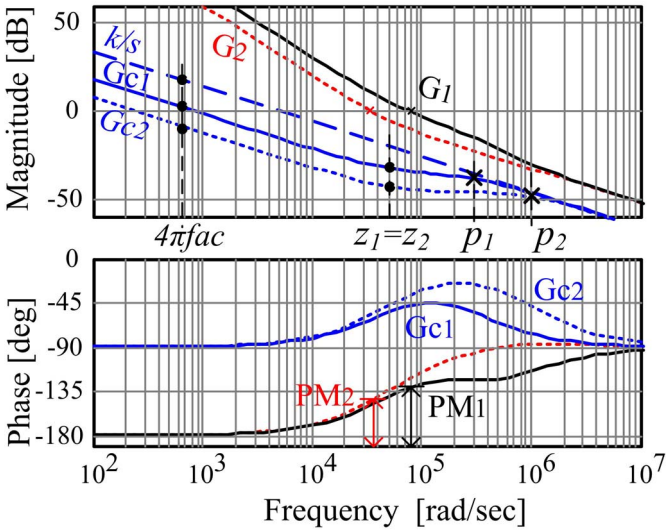


Fig.4.11: Illustration of controller design

2. Choice of z

With the choice of k value, the curve "k/s" (Fig.4.11) is fixed. The zero is then placed at the worst case crossover frequency of the loop response (this loop response includes a controller of k/s only), so as to achieve a 45° phase margin.

3. Choice of p

Two controllers ('G_{C1}' & 'G_{C2}') with the same zero ($z_1 = z_2$) but different pole values ($p_1 < p_2$) have been shown in Fig.4.11. The figure also shows the corresponding open-loop Bode plots ('G1' and 'G2') based on plant 'B' (Fig.4.11). Firstly, it may be noted that the maximum gain at $2f_{ac}$ is limited by the curve k/s.

A larger pole p_2 reduces the controller gain at $2f_{ac}$ (see curve 'G_{C2}') and the loop bandwidth (see curve 'G_2'). Although a large pole value causes a larger phase bump ('G_2' vs. 'G_1'), this does not necessarily lead to a larger phase margin ($PM_1 > PM_2$). Also, the pole should be sufficiently small (say, less than $f_s / 5$) in order to filter out the switching components. On the other hand, if the pole is too close to the zero, it will deteriorate the phase boost provided by the zero.

In our design, the pole p is at 16 kHz, which is sufficiently low to filter the switching components (of 100 kHz) while at the same time ensure a phase margin of 29^o at the boundary conduction condition under the rated power.

The designed controller for the flyback CCM inverter is:

$$G_{C1} = \frac{5000}{s} \cdot \frac{s + 5 \times 10^4}{s + 10^5} \tag{4-12}$$

The controller in (4-12) can be implemented by the compensation circuit in Fig.4.11, where $k_i = 0.47$, $C_{fz} = C_{fp} = 8.6nF$, $R_i = 3.9k\Omega$, $R_f = 2.2k\Omega$ and $V_m = 3V$.

Table 4.1: Theoretical Performance of the designed system at several key operating conditions

P_{pv} (W)	$\lvert V_g \rvert$ (V)	Mode	Gain (dB) @ 100Hz	BW (kHz)	PM(^{o})
200 (P_r)	325	CCM	88.2	23.6	51
	112 (V_{gb})	CCM	78.9	11.3	29
	10	DCM	7.78	0.24	91
51.4(P_c)	325	CCM	88.2	21.0	26
	325	DCM	32.1	4.44	104

The performance of the controller in (4-12) has been analytically verified at a few quasi steady state operating points and tabulated in Table 4.1. Here, P_r is the rated power and P_c is the critical power given by (4-9). Voltage V_{gb} refers to the

grid voltage at the CCM/DCM boundary operation. The largest loop bandwidth, which occurs at rated power and maximum grid voltage, is below $f_s/4$ as discussed before. The phase margins show the system to be stable in all the cases considered. The bandwidth (BW) and the $2f_{ac}$ gain are both generally high in CCM and in DCM at higher voltages. Even at a low grid voltage of 10V in DCM operation, the system has a reasonable bandwidth (0.24 kHz) and gain at $2f_{ac}$ Hz (7.78 dB).

The designed controller has been implemented to verify its tracking performance. The operating waveforms as well as the tested loop gain bode plots will be presented and analyzed in Section 4.6.2.

4.5 Improved Current Sensing using CT

Current sensing plays a key role in the implementation of control scheme. Reference [116] provides a good overview of different current sensing methods, including both non-isolated and isolated solutions.

For current sensing of the primary side current of the flyback-CCM inverter, the key requirements include: low power loss, high noise immunity, large bandwidth (especially for the OCC scheme), high accuracy and sensing gain linearity within an AC cycle in combined DCM/CCM operations over a wide operation range. Non-isolated current sensing using a shunt (resistor) in series with the source terminal of the main switch followed by a current sensing amplifier is one of the possible options. However, this approach tends to be lossier for larger currents especially if

higher sensing accuracy and higher signal-noise ratio are required. Therefore, this is less suitable for the studied scheme (with peak current around 60A for DCM inverter and 30A for CCM inverter). Other non-isolated current sensing methods such as using MOSFET's ON resistance or 'virtual resistor' [116] are not selected due to high measurement errors associated with them. Hall effect sensors and mageneto-resistive devices tends to be less lossy but have a limited bandwidth. In this work, a Current Transformer (CT) based method is used for both the OCC and the ACC schemes due to its low loss, high bandwidth and better signal-to-noise ratio features. The conventional sensing circuit using unidirectional CT with core reset circuit [117] turned out to suffer from poor sensing linearity over an AC cycle. A modified current sensing circuit using bidirectional CT without a core reset [118] was applied to address this issue. This approach successfully improved the sensing accuracy and linearity.

In the following parts, the problem with the conventional unidirectional CT sensing circuit for the targeted application would be introduced and studied first in Section 4.5.1. Modified current sensing circuit using bidirectional CT and its operating waveforms will be described in Section 4.5.2.

4.5.1. Current Sensing Distortion with Unidirectional CT

The first current sensing scheme that was tried was a conventional unidirectional CT based current sensing method. This was tested and found not suitable for primary side current sensing of flyback-CCM inverter.

As shown in Fig.4.12, a conventional unidirectional CT circuit with a secondary side diode and sensing resistor was used in series with the main switch M1 to sense the primary side current of flyback inverter. L_{mct} represents the magnetizing inductance at the CT secondary side, C_w indicates the equivalent capacitance at secondary side and R_w is the secondary side wiring resistance. This approach is commonly used in Switch Mode Power Supply systems [114].

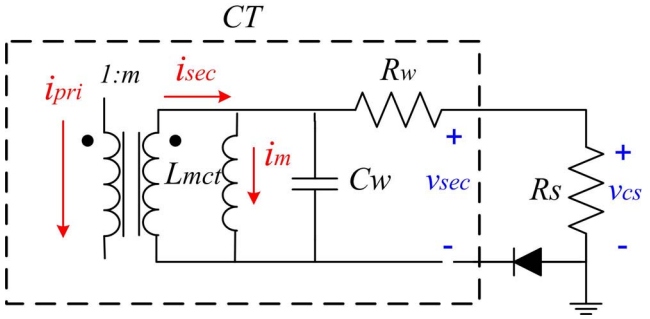


Fig.4.12: Equivalent circuit of current sensing circuit using unidirectional CT

In this design, the CT's turns ratio was 1:100; the measured magnetizing inductance reflected at the secondary side was 50.5mH and sensing resistance R_{cs} was 4.7Ω. Fast switching diode EGP10G was used. The parasitic parameters (i.e. R_w and C_w) are not measured.

Typical operating waveforms over an AC cycle tested with Indirect ACC controller is illustrated in Fig.4.13. Ch1 represents the current sensing signal v_{cs}, Ch2 is the actual primary side current i_{pri}, Ch3 is the drain-source voltage of M1 and Ch4 shows the CT secondary side voltage v_{sec}. The irregular shape of Ch1 and Ch2 are due to the current spikes when the main switch M1 is turned on. From the solid contour parts, it can be noticed that current sensing signal v_{cs} does not match the

actual primary side current exactly. The CT secondary side voltage shows clear irregular shapes especially during the transition between DCM and CCM operations.

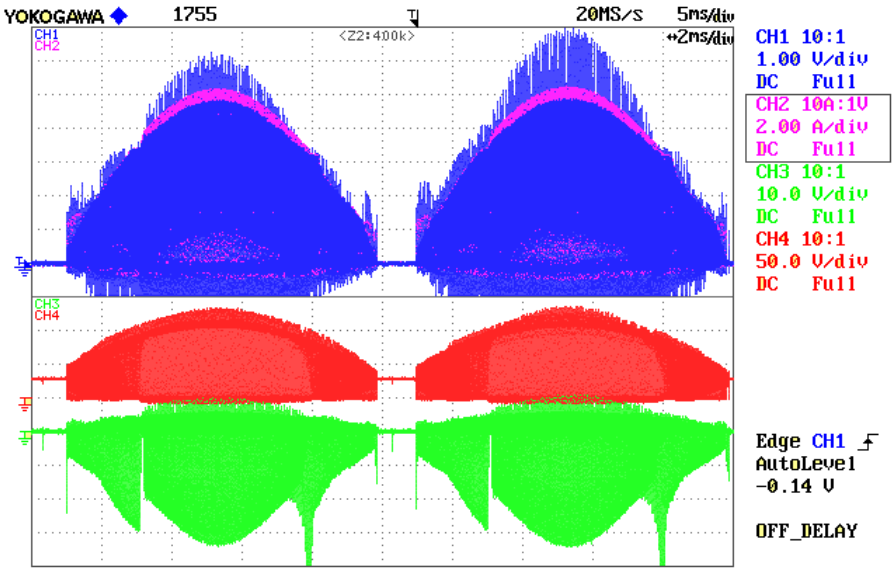


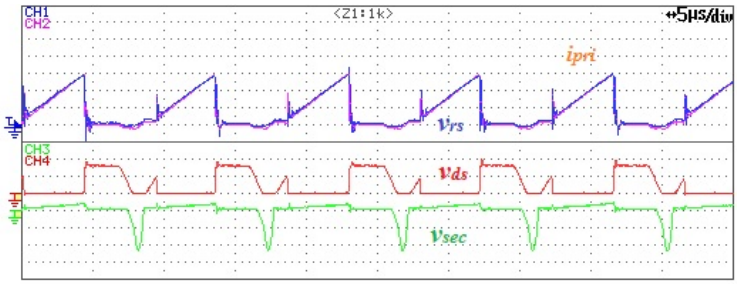
Fig.4.13: Unidirectional CT waveforms over an AC cycle: Ch1: v_{cs} ; Ch2: i_{pri} ; Ch3: v_{ds} ; Ch4: $v_{\sec}$ (experiment)

Enlarged waveforms of Fig.4.13 with the cyclic operations at different points of AC cycle are shown in Fig.4.14.

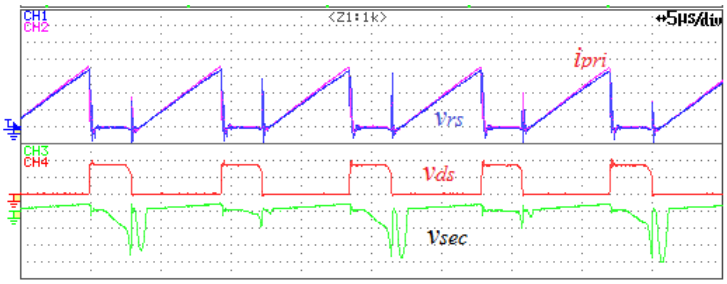
As shown in Fig.4.14, during the current pulse at primary side, the CT secondary side current diverts into magnetizing inductance *Lmct*. When the current pulse ends, the energy stored in this inductance needs to be removed. This core reset prevents the magnetizing current build up and saturate the core. In the test, the secondary side voltage $v_{\sec}$ of CT is measured to reveal the core resetting behariours. As shown in Fig.4.14, the CT core reset behaviors at DCM, CCM and transition between DCM and CCM operations are different.

In DCM mode (Fig.4.14(a)), the CT secondary side voltage $v_{\sec}$ starts to reduce to negative value for core resetting during the third interval when both flyback main

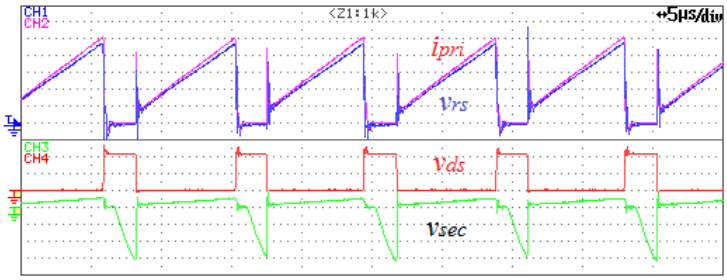
switch M1 and secondary side diodes D1/D2 are turned off. As analyzed in Section 3.5.2, during the oscillation in the third interval, the M1 body diode conducts negative current when M1 drain source voltage falls below zero. This negative current passes though CT primary side and reset the core.



(a) DCM operation



(b) Transition between DCM and CCM



(c) CCM operation

Fig.4.14: Cyclic waveforms of unidirectional CT sensing (zoom-in of Fig.4.13, [5µs/div])

In CCM mode (Fig.4.14(c)), when the current pulse ends, the energy stored in magnetizing inductance are transferred to the parallel capacitance *Cw* in a resonant way.

During the transition between DCM and CCM (Fig.4.14(b)), the resetting behaviors are irregular, which includes both resetting behariour in DCM and CCM operations.

Overall, the main reasons of the current sensing distortion over an AC cycle are summarized as follows. Firstly, the magnetizing current of CT varies within AC cycle, causing error in the average sensed value. Secondly, in DCM operation, the resonance between flyback transformer and switch output capacitor helps to reset CT to negative flux. As a result, in DCM operation, the magnetizing current starting from negative makes the sensed average current more than real value. While in CCM operation, the sensed average current is less than the real value due to positive magnetizing current.

For the ACC scheme, these phenomena, added to the fact that the loop gain of the inverter is much less in DCM than in CCM operation, make the current distortion during the transition between DCM and CCM even more severe.

Due to these reasons, this approach to current sensing was not suitable for the flyback-CCM inverter and hence abandoned.

4.5.2. Current Sensing using Bidirectional CT with Sample & Hold

In order to enable current sensing over a wide operating range, the bidirectional CT technique proposed for DC-DC converter in [118] was adopted and further modified for use in the present application. The basic idea is to get rid of the different core reset behaviors in DCM and CCM over an AC cycle by using a bidirectional CT

and then use sample & hold circuit to retrieve the DC offset and reconstruct the original current being sensed.

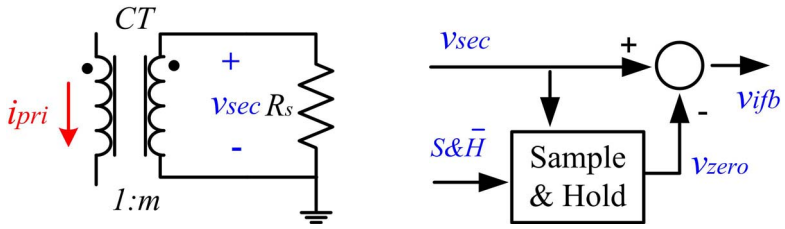


Fig.4.15: Current sensing method using bidirectional CT with Sample & Hold [118]

The current sensing method using bidirectional CT and sample and hold circuit is illustrated in Fig.4.15[118]. Due to the limitations of CT operation at low frequency, the CT is unable to sense the DC component in the primary current. However, this DC offset information is stored in the instantaneous current waveform v_{sec} itself. This DC information then can be retrieved by a sample and hold circuit, which can then be used to reconstruct the actual instantaneous current signal.

The sample and hold signal modified for the flyback-CCM inverter is shown in Fig.4.16, which samples the secondary side voltage of CT during a short interval when D1/D2 is on and holds the value for the rest of the switching cycle. This is different from the original CT circuit in [118], where the sample interval corresponds to the interval when M1 is off.

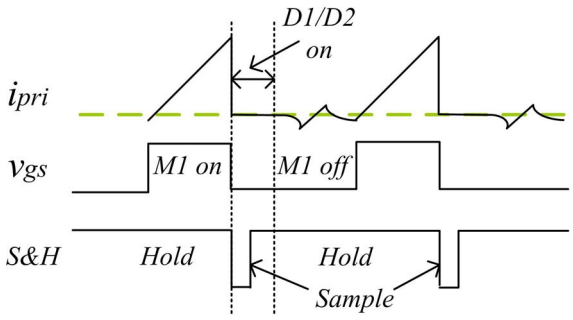


Fig.4.16: Generation of Sample and Hold Signal

As shown in Fig.4.16 and discussed in Chapter 3, in DCM operation, the primary side current does not keep to zero when M1 is turned off. Therefore, instead of sampling during the whole interval when M1 is off as was done in [118], the sample time in the present work is limited to be within the interval when D1 or D2 is on. This is an important consideration to ensure that the primary current is indeed zero when the S&H operates. Without this modification, significant measurement error was found in the current sensing.

As the conducting interval of D1/D2 varies with AC voltage and power level, a constant sample interval is used in all cases, which guarantees the correct zero information is sensed. In this design, a sampling time of 1μs is used. One of the operating waveforms tested is shown in Fig.4.17.

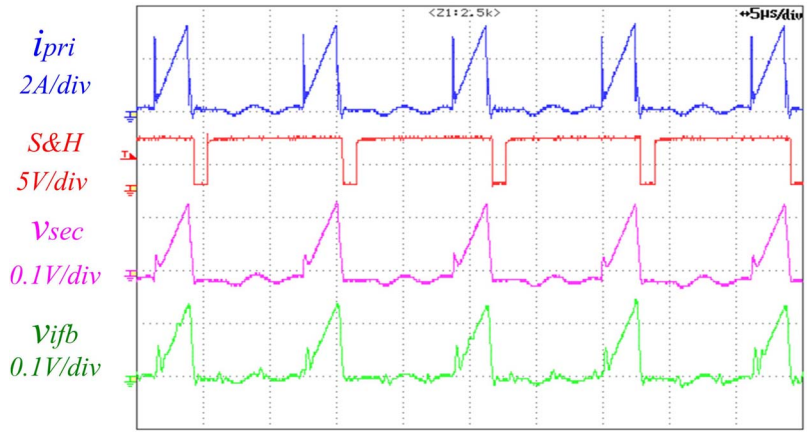
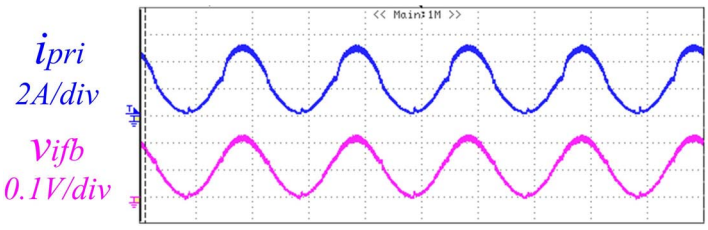


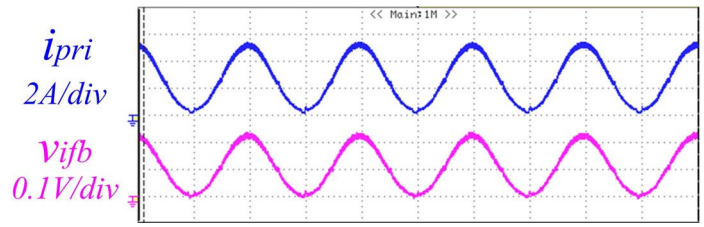
Fig.4.17: Current Sensing Operating Waveforms (experiment)

As illustrated in Fig.4.17, v_{sec} is similar to the primary side current but with a negative DC offset. This negative DC offset in v_{sec} is sampled when S&H signal is low and hold for the rest interval when S&H signal is high. By substracting the DC offset from v_{sec}, the actual current feedback signal v_{ifb} is able to restore the DC information.

Compared to the unidirectional CT scheme, the performance improvement of the modified bidirectional CT scheme is illustrated in Fig.4.18. These waveforms are tested when the flyback-CCM inverter works with designed IACC and the high switching components are removed by setting the internal filter of oscilloscope at 10kHz. The primary side current i_{pri} sensed by current probe is compared with the sensed feedback signal, v_{ifb}. As shown in Fig.4.18 (a), the feedback signal v_{ifb} is sinusoidal and follows the reference signal (not shown here). But the primary side current i_{pri} shows a clear distortion, which is due to the transition between DCM and CCM operation as discussed above. When a bidirectional CT current sensing method is used, the distortion in i_{pri} is largely reduced as shown in Fig.4.18 (b).



(a) with unidirectional CT



(b) with bidirectional CT

Fig.4.18: Current Sensing Operating Waveforms over AC cycle with IACC (experiment: with filter of 10 kHz)

4.6 Results and Analysis

The operation of the system with the two indirect current control schemes discussed in this chapter, IOCC and IACC for the designed flyback-CCM inverter,

were verified by both simulation and experiment. For each scheme, the quasi-steady state operating waveforms and stability aspect will be presented and analyzed. Section 4.6.1 focuses on the results of IOCC scheme, while Section 4.6.2 presents the major results for the IACC scheme.

4.6.1. Verification of the IOCC Scheme

The designed flyback-CCM inverter controlled by IOCC was simulated in PLECS /SIMULINK. A prototype was also built and tested under varying power level. These results are discussed in this part.

4.6.1.1. Simulation Results

As the current of the PV panel operating at the maximum power point changes between zero and its maximum value based on the solar irradiation level and temperature, the micro-inverter is required to work at different power (current) levels in a stable manner.

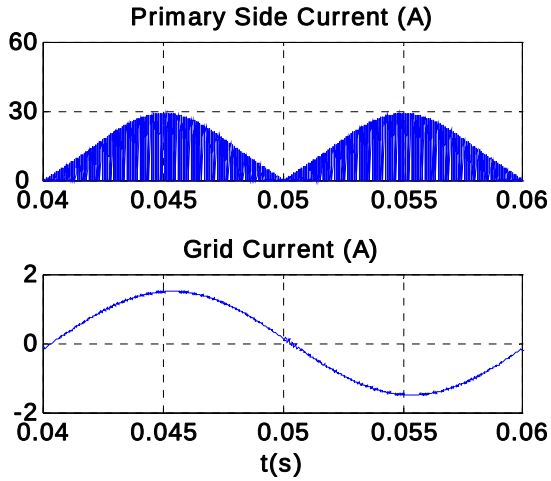
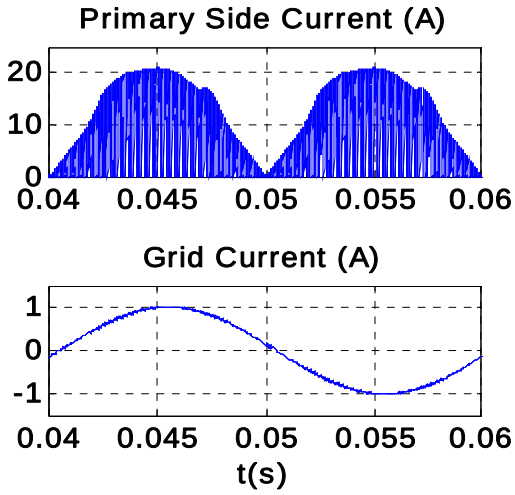
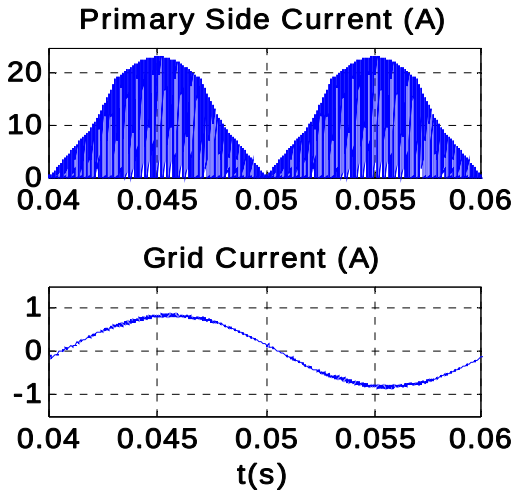


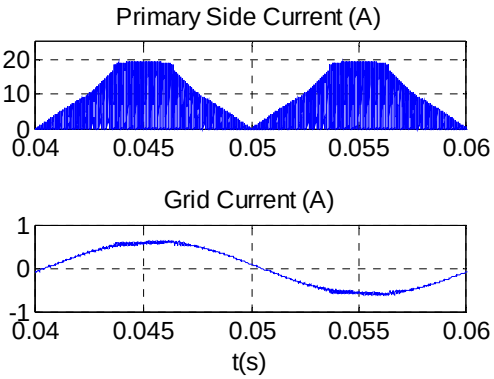
Fig.4.19: Operating waveform at V_{pv}=27V, I_{pv}=9A, V_{rms}=230V, (simulation, THD = 0.80%)



(a) I_{pv} = 6A (THD=1.34%)



(b) *Ipv* = 5A (THD = 2.82%)



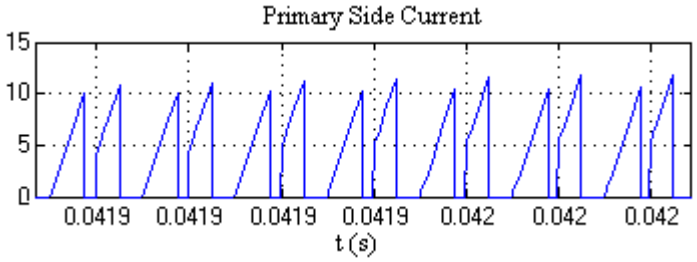
(c) *Ipv* = 3.7A (THD = 6.23%)

Fig.4.20: Irregular operation waveforms at reduced power levels V_{pv}=27V, V_{rms}=230V (simulation)

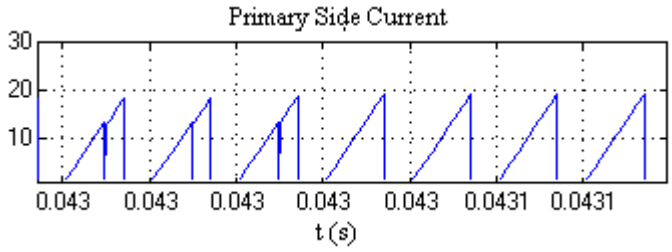
With the proposed IOCC scheme, the simulation result at higher power level demonstrates a good tracking performance as shown in Fig.4.19. However, when the

input power reduces, the simulation results indicated the existence of the nonlinear dynamics during certain intervals in the line cycle at reduced panel currents. Two typical situations encountered in the simulations are shown in Fig.4.20.

It is observed in Fig.4.20 (a) that when PV panel current reduces to 6A, the envelope of the primary side current becomes irregular during some intervals of the line cycle. The waveform in Fig.4.20 (b) corresponding to I_{pv} = 5A is even worse as the peak value of the primary current envelope is larger than the case when I_{pv} = 6A. When I_{pv} reduces to 3.7A, the distortion in the grid current waveform is much larger with THD of 6.23% compared to 1.34% when I_{pv} = 6A and 2.82% when I_{pv} = 5A.



(a) Phenomenon I



(b) Phenomenon II

Fig.4.21: Enlargemnt of two nonlinear dynamic phenomena in Fig.4.20 (simulation)

Fig.4.21 gives a closer view of the primary side current waveforms in Fig.4.20. It is observed that the operation jumps alternately between DCM mode and CCM mode in Fig.4.21 (a), while in Fig.4.21 (b), the duty ratio in DCM becomes close to

unity which makes the switching frequency effectively equal to half of the desired value. It should be mentioned here that in the proposed IOCC, the charge capacitor C_C is reset at the end of every switching cycle. The discharge time is 5% of switching cycle. Therefore, when the duty ratio reaches 95%, M1 is kept on but C_C is discharged to ensure the accurate average current measurement for the next cycle.

4.6.1.2. Experimental Results

The IOCC scheme in Fig.4.6 (discussed in Section 4.4.1) was implemented using a switched integrator circuit as shown in Fig.4.22. The sensed average current signal v_{ifb_ave} can be calculated as:

$$v_{ifb\_ave} = \int_0^{DTs} \frac{v_{ifb}}{R_C C_C} dt = \frac{mR_s}{R_C C_C f_s} I_{pri}. \tag{4-13}$$

This equation represents the experimental implementation of (4-1).

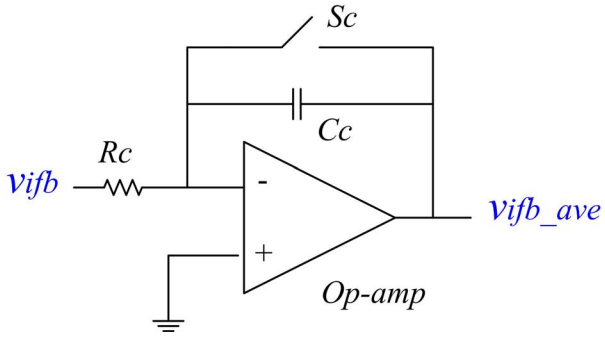


Fig.4.22: Switched Integrator for OCC scheme

In the control circuit, an analog switch CD4066 is used as S_C together with operational amplifier LF351.

The test was carried out using a DC power supply at fixed PV voltage, 27V. An AC voltage source KIKUSUI PCR1000L in parallel with a resistive load is used to

emulate the grid connection. The resistive load is used in parallel to prevent the power from feeding into the AC source. Some typical input and output waveforms are shown in Fig.4.23.

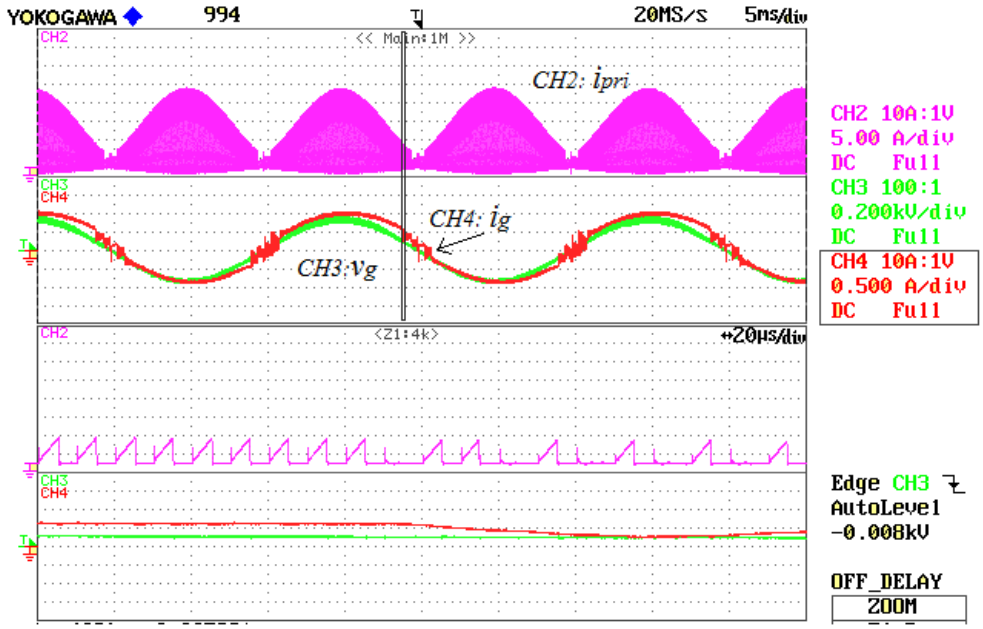


Fig.4.23: Input and output waveforms with IOCC: V_{pv}=27V, I_{pv} =6.7A, V_{rms}=230V (experiment)

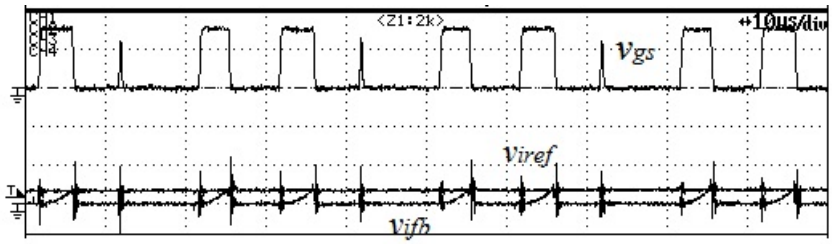


Fig.4.24: Control signals around zero crossing points (v_{gs} [10V/div], v_{iref} and v_{ifb} [0.5V/div])

As shown in Fig.4.23, at higher PV current levels (6.7A DC in this case), the designed IOCC scheme is able to make grid current i_g follow the sinusoidal grid voltage v_g in most part of an AC cycle. However, some switching cycles are missed during zero-crossing, leading to oscillation and distortion, as illustrated in the i_g waveform in Fig.4.23. These missing cycles are found to be due to the sensing noise picked up by large dv_{ds}/dt that occurs when M1 turns on, which hits

the reference signal v_{iref} and resets the RS flip-flop wrongly. One example of the control signal waveforms is given in Fig.4.24 to show this effect. This effect could be reduced by turning on M1 more slowly or by adding an additional filter to v_{ifb}.

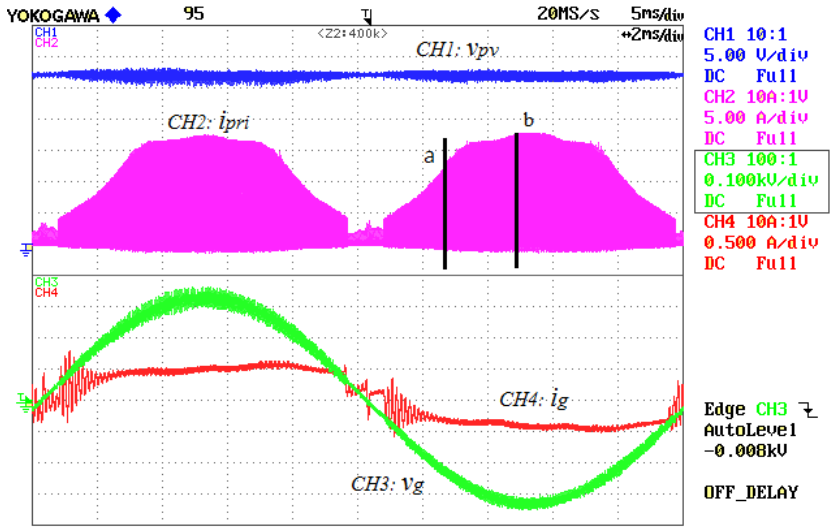
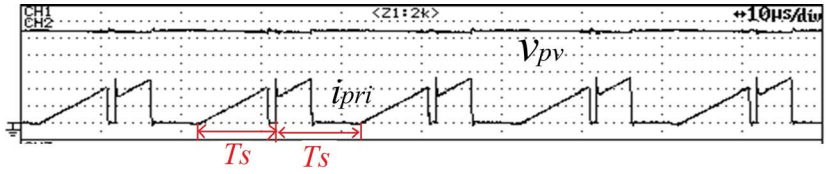
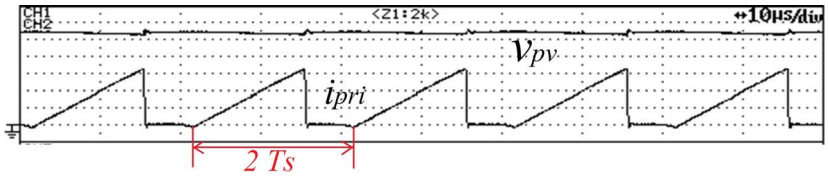


Fig.4.25: Input and output waveforms V_{pv}=27V, I_{pv} =3.7A, V_{rms}=230V (experiment)

Besides, the nonlinear dynamic behaviors noticed in simulation (in Fig.4.20) are also found in experiment as shown in Fig.4.25. The primary side current presents a similar shape to the simulation prediction, but the gird current i_g suffers from a larger distortion over an AC cycle than the simulation result.



(a) Area 'a', phenomenon I (v_{pv} [5V/div] and i_{pri} [5A/div] , 10μs/div)

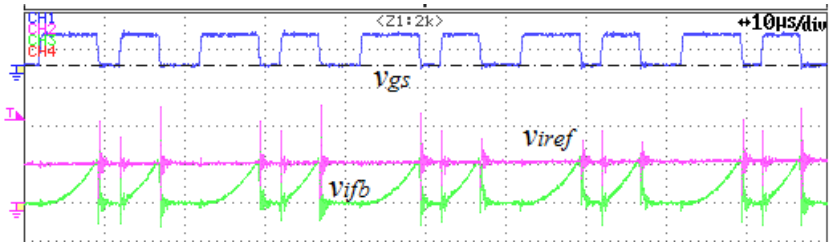


(b) Area 'b', phenomenon II (v_{pv} [5V/div] and i_{pri} [5A/div], 10μs/div)

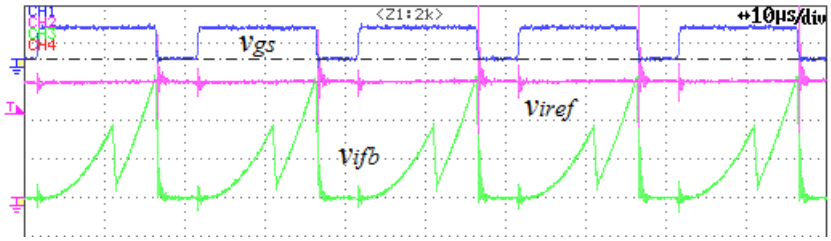
Fig.4.26: Enlargement of two nonlinear dynamic phenomena in Fig.4.25 (experiment)

The operating waveforms around 'a' and 'b' in Fig.4.25 are enlarged and

shown in Fig.4.26. Phenomena I (Fig.4.26 (a)) shows the flyback-CCM inverter working in DCM and CCM alternately every other cycle. This is similar to the simulation results in Fig.4.21 (a). Likewise, phenomena II (Fig.4.26 (b)) shows the duty ratio in DCM becoming close to unity in one cycle followed by a CCM operating cycle. Effectively, the operation is in DCM with the switching frequency at half of the desired value. As a result, the actual average current is less than the reference value, which makes the grid current around the peak grid voltage less than expected.



(a) Phenomenon I (v_{gs} [20V/div], v_{iref} and v_{ifb} [0.5V/div])



(b) Phenomenon II (v_{gs} [20V/div], v_{iref} and v_{ifb} [0.5V/div])

Fig.4.27: Control signals corresponding to Fig.4.26

The control signals for Fig.4.26 are illustrated in Fig.4.27. For phenomenon I, the current feedback signal (switching average) v_{ifb} reaches the reference signal v_{iref} at varying duty cycles in adjacent switching cycles. For phenomenon II, it is shown in Fig.4.27 (b) that v_{ifb} is unable to reach v_{iref} in every other cycle due to DCM operation (Fig.4.26 (b)). In this case, the gate source signal of M1 is kept on

till the next cycle, which makes the switching frequency effectively halved. Overall, the actual current is less than the reference value in the intervals with phenomenon II.

4.6.1.3. Study of Nonlinear Phenomena

To gain an insight into the nonlinear phenomena, the discrete-time cycle-by-cycle mapping method [119], usually obtained by deriving the states of the next switching cycle from the present switching cycle, is applied here.

Let the primary current at the start of the i th cycle be $i_{ini}[i]$. Then the primary current at the end of the turn-on period is

$$i_p[i] = i_{ini}[i] + D[i] \cdot V_{pv} T_s / L_m \tag{4-14}$$

where $D[i]$ represents the duty ratio of the i th cycle, and is determined cycle-by-cycle by the OCC. The value of $D[i]$ can be obtained by solving the equation below ,

$$i_{ini}[i] \cdot D[i] + V_{pv} T_s \cdot D^2[i]/(2L_m) = I_{pri}[i], \tag{4-15}$$

where $I_{pri}[i]$ is the desired average primary current at the i th cycle.

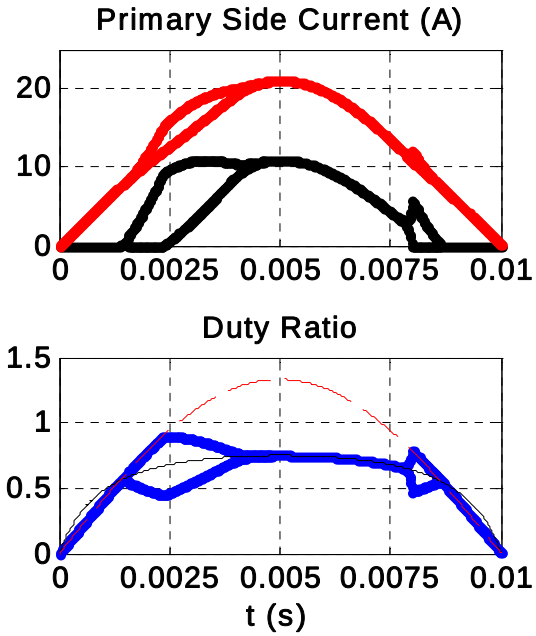
At the end of the switching period, i.e. the beginning of the next switching cycle, the initial primary side current is:

$$i_{ini}[i+1] = i_p[i] - V_g[i] \cdot D'[i] \cdot T_s /(nL_m) \tag{4-16}$$

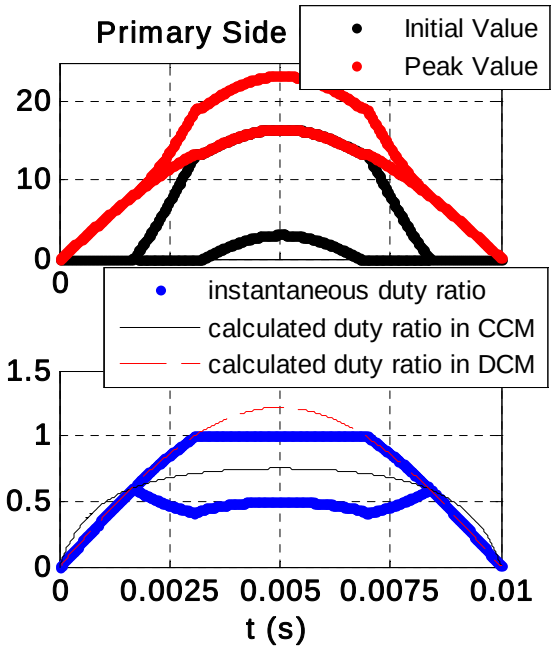
where the instantaneous grid voltage at n th cycle is given by:

$$V_g[i] = \sqrt{2}V_{rms}\sin(\omega \cdot iT_s) \tag{4-17}$$

The duty ratio of the secondary diode at the ith cycle $D'[i]$ is equal to $1-D[i]$ for CCM and $nV_{pv}D[i]/V_g[i]$ for DCM operation.



(a) I_{pv}=6A



(b) I_{pv}=5A

Fig.4.28: Discrete-time mapping of primary side currents and duty ratio at V_{pv}=27V

From (4-15) and (4-16), the uniform sampling of the initial primary current as well as the non-uniform sampling of the peak primary current at each cycle can be derived from the previous cycles. The iterative mapping of the primary current states under the same working conditions used to obtain the simulation waveforms of Fig.4.20 are shown in Fig.4.28.

The upper curves of the primary side currents in Fig.4.28 (a) and (b) represent the peak cycle-by-cycle value and these conform to the envelope of the primary current observed in Fig.4.20. The lower curves represent the initial primary current at the beginning of each cycle, whose value is zero in DCM operation. The duty ratio change over half the AC cycle is also shown in Fig.4.28. The dashed curves (in red) indicate the duty ratio in DCM operation while the thin solid curves (in black) represent the duty ratio calculated from CCM operation at the given working condition. The thick curves (in blue) show the instantaneous duty ratio over the half AC cycle. It is observed in Fig.4.28 (a) that the nonlinear behaviour of the primary current happens during the transitions between DCM and CCM. This behavior, is similar to an identified border collision bifurcation reported in [120], where the bifurcation is due to transition between CCM and DCM in a boost converter. This type of bifurcation is caused by the structural change of the topology (which here is the change in operating modes). A thorough study of bifurcation phenamonen usually requires calculation of the determinant of the Jacobian matrix along the parameter variations, which is out of the thesis scope.

In Fig.4.28 (b), another phenomenon observed in Fig.4.20 (b) is illustrated.

Around the peak value of AC cycle, instead of converging into one curve in CCM operation as shown in Fig.4.28 (a), the branch representing DCM operation hits another line where the duty ratio is one. In this case, the actual working frequency is half of the desired value.

Overall, the nonlinear phenomena are caused due to the fact that OCC is a nonlinear control, of which, the duty ratio is highly dependant on the cycle-by-cycle initial primary current. Its fast tracking capability makes the duty cycle with adjacent switching periods able to change very fast when the flyback inverter enters the CCM operation from DCM mode. This feature makes it operate in DCM and CCM every other cycle. Next part introduces the proposed method to prevent or mitigate the nonlinear dynamic behaviors.

4.6.1.4.Proposed Nonlinear Dynamics Mitigation Method

Both the simulation and experimental results above indicate that the unexpected nonlinear dynamic behaviours would influence the current tracking behavior (phenomenon II) and cause distortion in output current.

Based on the analysis in the previous section, the large variation of adjacent duty cycles is the main reason for the nonlinear phenomena. Therefore, the approach taken is to prevent large changes in duty cycle between successive switching cycles. This can be achieved by directly limiting the allowable maximum change in duty ratio $\Delta D(max)$ from one cycle to the next to a small value for the purpose of realizing a smooth transition between DCM and CCM operations. This method can

be implemented using a low-end microcontroller.

However, if the value of ΔD(max) is too small, the inverter might fail to track the reference signal. In order not to interfere with normal operation of the microinverter, ΔD(max) should be larger than the maximum change of D during the normal tracking of the AC cycle.

The change of duty ratio in half AC cycle under different current level is given in Fig.4.29. It is easy to find that the maximum change of duty ratio in adjacent switching cycles occurs at the zero-crossing point of the AC cycle when operated in DCM mode.

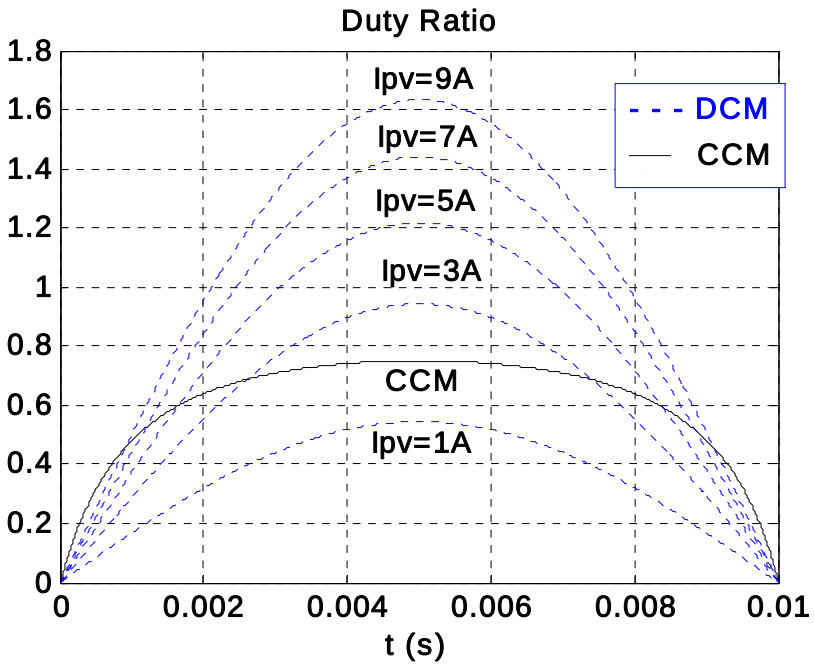


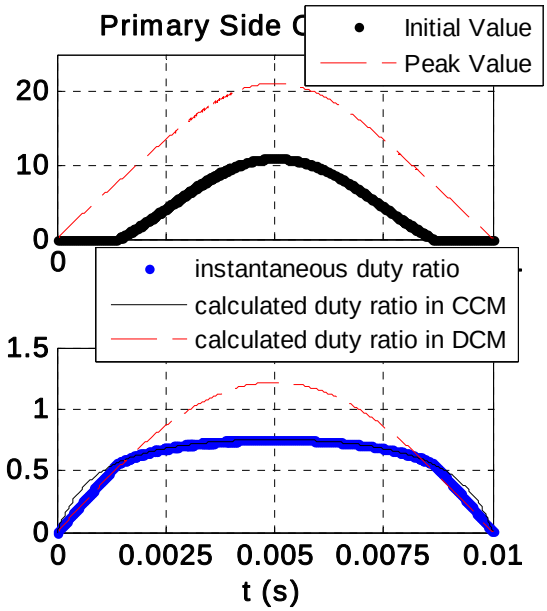
Fig.4.29: Change of duty ratio in half AC cycle

Therefore, the change rate of duty ratio ΔD can be obtained from (4-19):

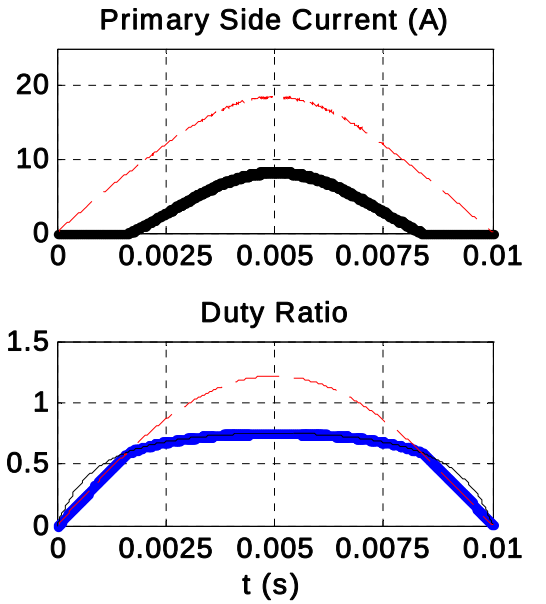
$$\left|\frac{\Delta D}{T_s}\right| = \frac{dD_d}{dt} = 2\omega\sqrt{I_{pv}L_m f_S / V_{pv}}\left|\cos(\omega t)\right| < 2\omega\sqrt{I_{pv}L_m f_S / V_{pv}} \qquad (4\text{-}18)$$

$$\Delta D < 2\omega\sqrt{I_{pv}L_m f_S / V_{pv}} \times T_s \qquad (4\text{-}19)$$

In our design, the maximum duty ratio change between adjacent cycles is 0.63% at the maximum I_{pv} and minimum V_{pv}. Therefore, we choose $\Delta D(\max) = 1\%$.



(a) I_{pv}=6A



(b) I_{pv}=5A

Fig.4.30: Mitigation of bifurcation in Fig.4.28 V_{pv}=27V

By applying the duty cycle variation limit of 1%, to the discrete time mapping, the result is shown in Fig.4.30. Compared to Fig.4.28, the undesired bifurcation is

successfully eliminated in Fig.4.30.

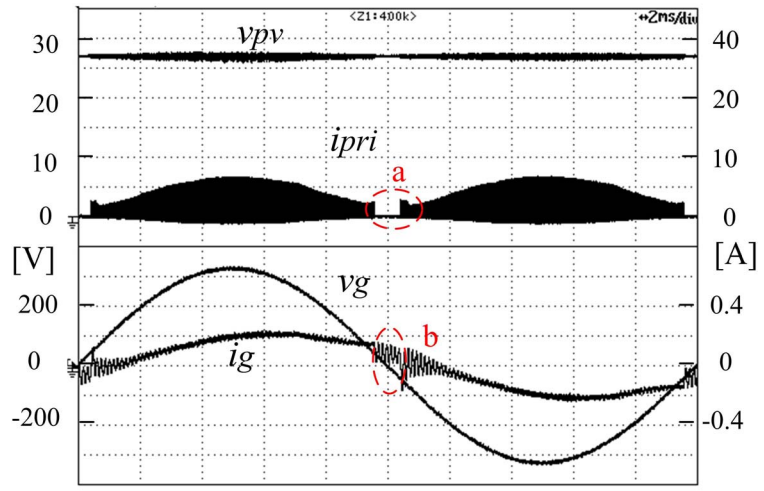
In summary, it is verified by discrete time mapping that the proposed method with duty cycle variation limit is capable of suppressing the nonlinear dynamics on one hand. However, on the other hand, limiting the allowable duty cycle variation also reduces effectively the system bandwidth. In this case, the intrinsic advantage (fast dynamical response) of OCC scheme is compromised. In addition, the implementation of IOCC scheme with limit on change in duty cycle is more complex. One way of doing it is to use analog circuits for OCC and digital controller to implement duty cycle limit, which are more complex compared to analog-only or digital-only approaches.

On the other hand, a comparatively slower controller such as ACC can provide fair enough performance for the target flyback-CCM inverter, while at the same time being easy to implement, as discussed in the next section.

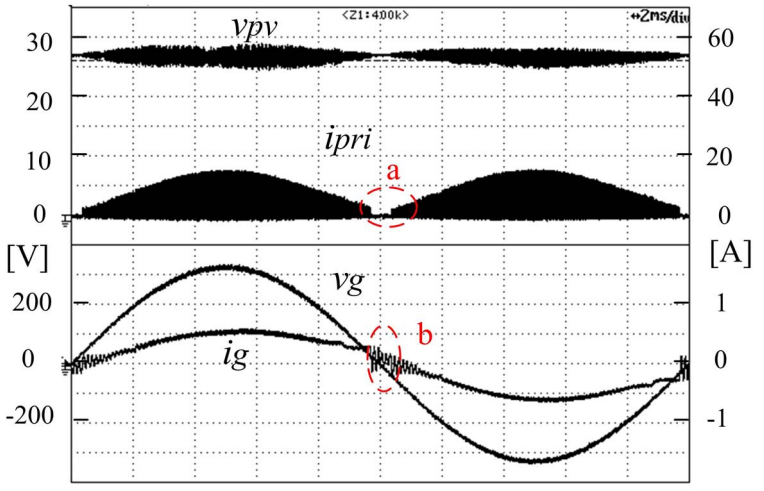
4.6.2. Verification of IACC Scheme

The IACC scheme studied in Section 4.4.2 was implemented and tested with the designed flyback-CCM inverter prototype discussed in Chapter 3. Its current tracking performance as well as its stability will be verified in the following sections.

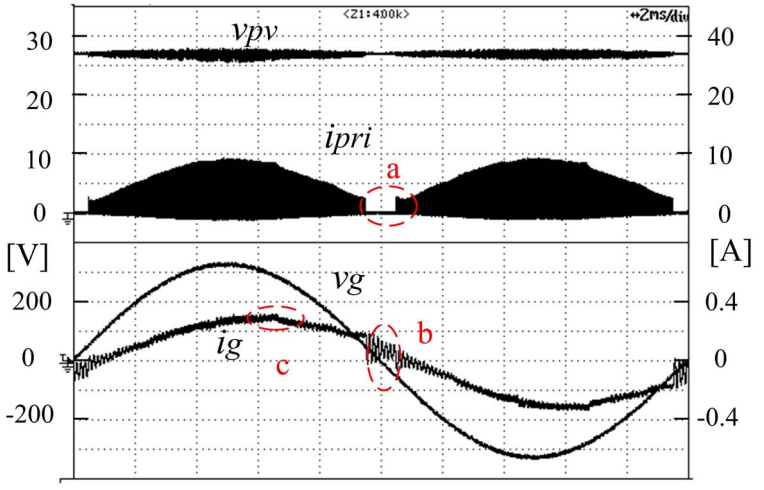
4.6.2.1.DC-AC Operation



(a) V_{pv}=27V, P_{pv}=10W



(b) V_{pv}=27V, P_{pv}=40W



(c) V_{pv}=27V, P_{pv}=100W

Fig.4.31: Current tracking performance (Input and output waveforms)

The designed flyback-CCM inverter with Indirect ACC was tested at varying power levels. Typical operating waveforms are shown in Fig.4.31. The conversion efficiencies at varying power levels and operating waveforms at full power level can be found at Chapter 3.

As shown in Fig.4.31, the distortion of current waveforms is noticed around the zero crossing intervals. This is partly caused by a dead time (‘a’) when the AC current goes through zero and the secondary side operation switches from S1 to S2 and vice versa. Another reason is due to the inability of the PWM IC (SG3524 here) to reach very low duty cycle values. Besides, in CCM, because of the tracking delay of the controller as well as the incomplete demagnetization of the flyback transformer, the secondary side current of flyback converter does not fall to zero during switching between S1 and S2, which makes the output current experience a sudden change，thereby causing oscillation (‘b’) at the output filter resonant frequency. This zero crossing oscillation is one of the main reasons for the lower THD value measured and can be improved using other PWM IC or precision comparator that can reduce the duty cycle to a very low value.

Additionally, when the operation varies between DCM and CCM, the tracking capability of the controller changes. It is reflected as a distortion (‘c’) in the output current waveform.

The output power factor and THD of grid current at different power levels were tested using Yokogawa 2531 Digital Power Meter and shown in Table 3.4. The low

current THD (<5% as required) at power level above 20% of rated power verifies that the scheme has satisfactory tracking performance.

Table 4.2: Output power factor and THD at various power levels ($V_{pv} = 27V$, $P_r = 200W$)

	5%	10%	20%	30%	50%	75%	100%
PF	0.48	0.72	0.88	0.94	0.98	0.99	0.99
THD	20.2%	7.6%	4.2%	4.0%	3.8%	3.4%	4.4%

4.6.2.2. Stability Verification under Quasi Steady State Operation

It must be noted that the stability of the flyback inverter in DCM is not an issue when the system is already stable in CCM, as the open loop phase margin in DCM of 90^o is larger than that of the CCM case.

The stability test of the inverter under CCM operation was carried out by measuring the open loop gain Bode plot under several DC to DC quasi steady state operating conditions. The test setup for loop gain measurement using Agilent 4395A is given in Appendix C. These input and output conditions (voltage and current) were set to correspond to different quasi steady state conditions at different power levels. However, the Bode plots of the inverter corresponding to instantaneous power transfer above the rated power, e.g. $V_g > 2V_{rms}$ at P_r, could not be measured due to the higher power burden involved.

Based on these tests, it was found that the theoretical modeling given by (4-7) and (4-8) (Theo-1) and the experimental results show important differences. One difference is that the theoretical curve has a pole at the origin while the experimental curve has a low frequency pole (and not at origin). Also, the experimental curve

indicates a resonant peak around 7 kHz while the theoretical curve does not contain it.

This led to the determination that the flyback transformer's winding resistance R_{Lm} and the output L-C filter of the inverter could not be ignored in the loop gain modeling. Therefore, considering these two effects, the small signal AC model (Theo-2) of the flyback inverter in CCM operation is derived based on [115] and shown in Fig.4.32.

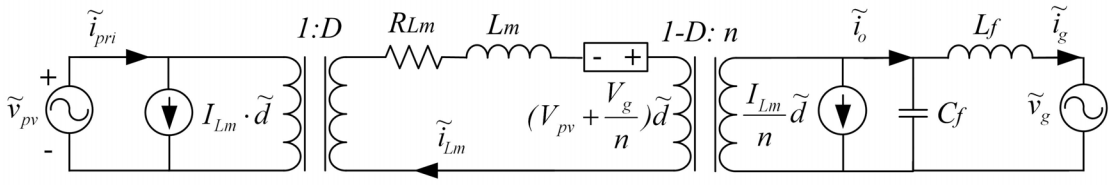


Fig.4.32: Equivalent Circuit of flyback Inverter in CCM operation

From Fig.4.32, the duty cycle to transformer current transfer function can be derived assuming the disturbance from $\tilde{v}_{pv}$ and $\tilde{v}_g$ are zero:

$$\frac{\tilde{i}_{Lm}}{\tilde{d}} = \frac{\left(V_{pv}+\frac{V_g}{n}\right)+\frac{1-D}{n^2}I_{Lm}Z_f}{sL_m+R_{Lm}+\frac{(1-D)^2}{n^2}Z_f} \tag{4-20}$$

$$\text{where } I_{Lm} = I_{pri}+nI_g = \frac{P_{ac}}{V_{pv}}+n\frac{P_{ac}}{V_g} \tag{4-21}$$

$$P_{ac} = 2V_{rms}I_{rms}\sin^2(\omega t) \tag{4-22}$$

$$Z_f = \frac{sL_f}{s^2C_fL_f+1} \tag{4-23}$$

The duty cycle to primary current transfer function G_{id2_CCM} can be calculated by:

$$G_{id2\_CCM} = \frac{\tilde{i}_{pri}}{\tilde{d}} = D \cdot \frac{\tilde{i}_{Lm}}{\tilde{d}} + I_{Lm} \tag{4-24}$$

Substituting (4-20)~(4-23) into (4-24), the modified theoretical model (Theo-2) can be shown to be:

$$G_{id2\_CCM} = \frac{s^3 L_f C_f L_m I_{Lm} + s^2 L_f C_f k_a + s I_{Lm}\left(L_f (1-D)/n^2 + L_m\right) + k_a}{s^3 L_f C_f L_m + s^2 L_f C_f R_{Lm} + s\left(L_f (1-D)^2/n^2 + L_m\right) + R_{Lm}} \tag{4-25}$$

where $k_a = V_g / n + R_{Lm} I_{Lm}$ and $I_{Lm} = I_{pri} + n I_g$ is the flyback transformer magnetizing current at a certain quasi steady state.

One of the tested open loop Bode plots is shown in Fig.4.33 and is compared with the theoretical results (both Theo-1 and Theo-2 models). The value of R_{Lm} was measured to be 0.25Ω. As shown in Fig.4.33, the plot of "Theo-2" agrees better with the experimental results. The pole at origin (according to Theo-1) has shifted, instead, to a low frequency, which is attributed to the presence of the primary winding resistance, R_{Lm}, of the flyback transformer. Also, the influence of the output filter causes a notch around the resonant frequency of 7 kHz.

As the filter resonant frequency is very close to the crossover frequency, multiple gain crossovers occur, both in Theo-2 and in the test curve. The experimental bandwidth of the loop gain (the first crossover) is 6050Hz, close to the estimated 6650Hz bandwidth, while the smaller of the two phase margins is 47^o (during the first crossover), which is higher than the estimated value of 38.3 ^{o} using Theo-2.

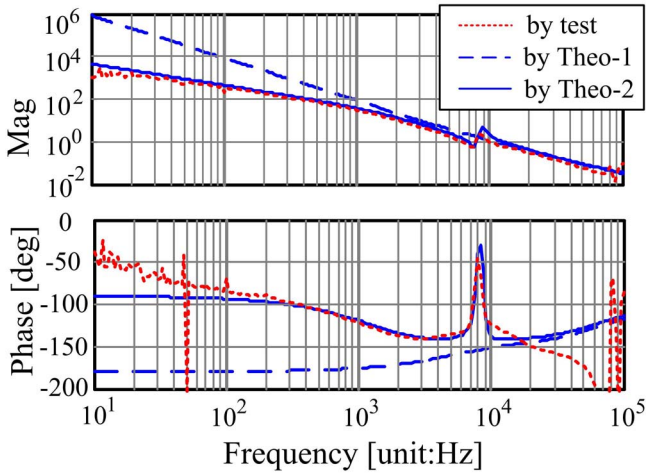


Fig.4.33: Open loop Bode Plots verification with 200W and V_{gb}=112V;($R_{Lm} = 0.25\Omega$ in Theo-2).

In addition, the frequency response tests have also been carried out at selected power levels over the set of worst case conditions defined in Fig.4.9 (between P_c and P_r). Here also, the experimental results confirm the theoretical modeling (Theo-2) and stability of the system.

4.7 Conclusion

Two indirect current controllers, i.e. IOCC and IACC have been studied in this Chapter to control the output current of the proposed flyback-CCM inverter. Based on the simulation and test results presented above, the pros and cons of each scheme are summarized below.

IOCC scheme is easy to design and implement as no compensation network is required, and is capable of tracking the reference signal within one switching cycle. However, it suffers from nonlinear dynamics, which might cause output current distortion at certain power levels. The proposed method to limit the duty cycle variation between adjacent switching cycles is shown to be able to eliminate the

nonlinear phenomena when properly designed. However, this compromises the OCC scheme's benefit of fast dynamic response. In addition, the simplicity of the controller is compromised and one may have to add a digital controller for implementation.

On the other hand, the controller design process in the IACC scheme is more complex, and needs to consider the large variation of plant transfer function under different operating modes and grid voltage/power levels. Besides, the system is slower compared to the IOCC scheme. However, the tracking performance is reasonable and is able to meet the PF and THD requirements at the grid side. In addition, the system is stable in all the quasi-steady state operating points. As has been done in the AC-DC PFC systems, this IACC scheme can be easily implemented as a single chip PWM IC for microinverter application.

In summary, the test results in Chapter 3 and Chapter 4 have verified the viability of the proposed flyback-CCM inverter approach for photovoltaic microinverter applications. The scheme has been shown to improve the weighted efficiency by 8% compared to a benchmark flbyack-DCM inverter. With proper design, conventional ACC can be used to control the primary side current instead of the secondary side current while still being able to meet the requirements specified in the standards. The proposed flyback-CCM inverter with IACC is a feasible low cost solution for microinverter application.

In the next chapter, we will propose and investigate a novel active power

decoupling scheme, which aims to eliminate the requirement of a large electrolytic capacitor without significantly compromising on the overall efficiency of the inverter.

CHAPTER 5: : A PARALLEL POWER PROCESSING (P3) SCHEME– TOPOLOGY STUDY AND DESIGN

5.1 Introduction

As discussed in Section 3.3 and Section 2.4, a major concern with the flyback-CCM inverter studied in Chapter 3 and Chapter 4 is the short lifetime of the large valued input electrolytic capacitor [1] due to the high operating temperature of the microinverter behind the PV module. The problem exists in both the popular flyback-DCM scheme and the flyback-CCM scheme proposed in this work.

As indicated in Section 2.3, a power decoupling circuit [34, 35, 104], such as the active filter in [104], can be added to lessen the impact due to the large electrolytic capacitor. The addition of the power decoupling circuit can be expected to reduce the efficiency somewhat. Therefore, an inverter which can achieve both high efficiency and long lifetime (i.e. including an active power decoupling eliminating the need of a large electrolytic capacitor) is desired. With this consideration, the present chapter proposes and investigates a Parallel Power Processing (P3) scheme, which is aimed to handle both purposes.

The motivation behind the proposal of this scheme will be presented in Section 5.2 together with one 'pilot' topological implementation based on a dual-output flyback converter and an auxiliary buck converter. The analysis and design of this

pilot topology, with focus on the power decoupling capacitance, operation and design of each converter, are presented in Section 5.3. In order to confirm the achieved reduction in the power decoupling capacitance by the application of the additional active power decoupling circuit, the proposed pilot topology is simulated with a PV module model. The scheme's performance is then compared to a popular single stage flyback-DCM inverter in Section 5.4. The prototype of the proposed pilot topology has been built. The implementation issues and experimental results are presented in Section 5.5.

5.2 System Concept and a Pilot Topology

In Section 5.2.1, a parallel power processing scheme with potential for high efficiency operation and active power decoupling capability is introduced. The underlying idea and operating waveforms of the schemes are presented. Following this, a pilot topology is proposed in Section 5.2.2 to implement this parallel power processing scheme.

5.2.1. System Concept

The concept of the proposed topology for microinverter in this chapter is based on the handling of the power decoupling requirement. Therefore, it is necessary to revisit the power decoupling requirement again in this section.

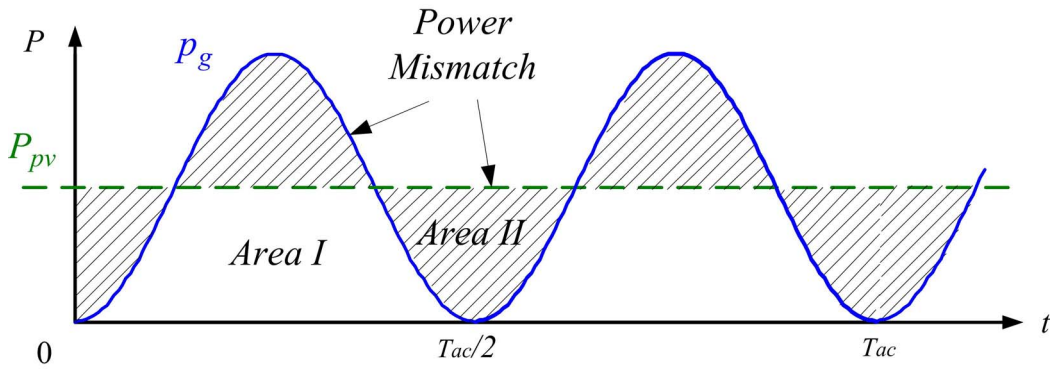


Fig. 5.1: Input and output power mismatch

Based on (3-2) and (3-3), the following power balance equation for a single phase inverter can be obtained.

$$P_g = P_{pv}\left(1-\cos(2\omega t)\right) \tag{5-1}$$

where P_{pv} and P_g represent the switching-period average power from PV module and to the grid, respectively. As has been discussed earlier, (5-1) shows that there is a second harmonic power imbalance between the DC input and AC output power.

As illustrated in Fig.5.1, the energy of "Area I" is directly transferred from the input to output while the energy of "Area II' is required to be stored in an energy storage component and later transferred to the output side.

The proportion of energy in "Area II" in Fig. 5.1 within half an AC cycle can be obtained by:

$$\frac{E_{A2}}{E_{A1}+E_{A2}} = \frac{\int_0^{T_{ac}/4}\sin(2\omega t)dt}{1\times T_{ac}/2} = \frac{1}{\omega\cdot T_{ac}/2} = \frac{1}{\pi} = 31.8\% \tag{5-2}$$

The proportion of energy in "Area I" in Fig. 5.1 within half an AC cycle is:

$$\frac{E_{A1}}{E_{A1}+E_{A2}} = 1 - \frac{E_{A2}}{E_{A1}+E_{A2}} = 68.2\% \tag{5-3}$$

A study of energy flow in conventional APD (Active Power Decoupling) schemes discussed in Chapter 2, reveals that most schemes such as those in [34, 105] add a serial connected APD circuit in the power processing path, which makes all the energy in Area I and II being processed twice. Other schemes such as [35, 37] are able to differentiate the energy in Area I and II and only process the energy in Area II (31.8%) through the additional APD circuits. However, the reported efficiency is limited, perhaps due to its low voltage, high current implementation of the APD circuit. Parallel Active Filter (PAF) schemes [70, 98, 104], which process only the decoupling power in Area II are available, but have the disadvantage of a three stage power processing path for the decoupled power.

Fig.5.2 shows the system diagram of the proposed Parallel Power Processing (P3) scheme, which consists of a dual output main DC/DC converter, an auxiliary DC/DC converter for power decoupling purposes and one UFI stage at line frequency. As indicated in Fig.5.2, the main DC/DC converter processes constant DC power. Therefore only a small capacitance at the PV side is needed for filtering out only high frequency switching waveforms. One output leg of the main DC/DC converter, which carries the required output current directly from input power, is connected to UFI. A parallel second leg is connected to the decoupling capacitor, which feeds the auxiliary DC/DC converter whose output is connected to the UFI. In this way, the excess input

power (Area II) will be transferred via the second leg to the decoupling capacitor and finally to the grid through auxiliary DC/DC converter.

This proposed parallel power processing scheme has been reported in Power Factor Correction applications [121, 122], where the purpose is to achieve fast output voltage control dynamics, In this study for microinverter application, the focus has been placed on the power decoupling capacitance reduction and conversion efficiency. Its advantages are summaried here.

1) 68.2% of the overall energy is directly transferred to the grid side through the main DC/DC conversion stage, while the rest (31.8% of the overall energy) in Area II will go through two high frequency switching conversion stages including the auxiliary DC/DC conversion stage.

2) The power decoupling capacitor is placed at a high DC link voltage, e.g. the secondary side of transformer, in an effort to allow larger voltage ripple, to reduce the power decoupling capacitance and to reduce the current value for active power decoupling circuit, hence reduce the power loss.

3) The main DC-DC converter processes constant DC power which reduces component stresses of the main converter.

The key operating waveforms ignoring the switching ripple (average current over switching period) of the variables marked in Fig.5.2 are illustrated in Fig.5.3. The

waveforms are drawn for the system with specifications given in STC condition in Table A.1.

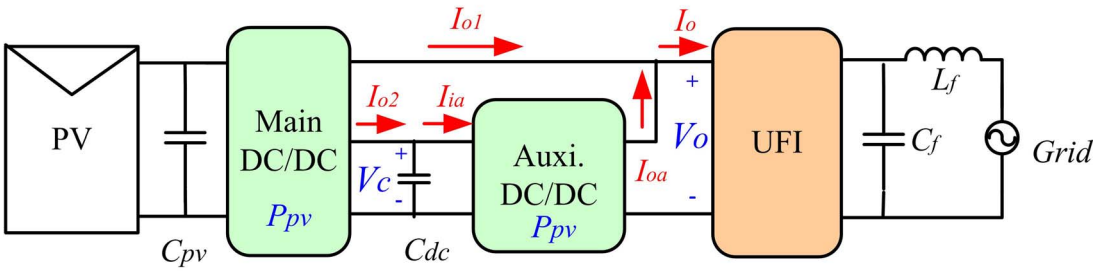


Fig.5.2: Circuit blocks and their inputs and outputs

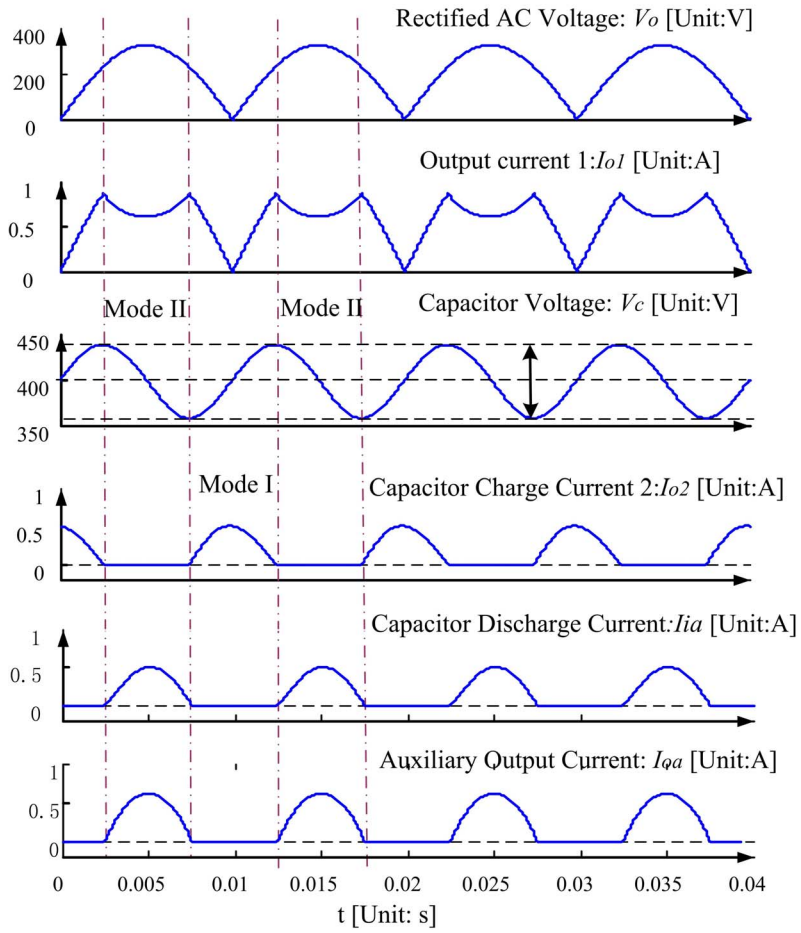


Fig.5.3: Key Operation Waveforms of P3 Schemes

Assume that the input voltage, current and power from the PV module are V_{pv}, I_{pv} and P_{pv}, respectively. Also, let the output voltage, current and power be given by

$V_g (= \sqrt{2} V_{rms} \sin(\omega t))$, $I_g (= \sqrt{2} I_{rms} \sin(\omega t))$ and P_g. Here, ω is the AC line angular frequency (rad/s).

The input voltage and current to UFI are rectified sinusoids and given by:

$$V_o = |V_g| \tag{5-4}$$

$$I_o = |I_g| \tag{5-5}$$

In Fig.5.3, two operating modes are present depending on whether the instantaneous input power is able to meet the instantaneous output power or not. "Mode I" corresponds to the operating mode when $P_{pv} > P_g$. In this mode, the output current, which follows a rectified sinusoid waveform, is supplied by the main DC/DC converter only. At the same time, the decoupling capacitor gets charged and the capacitor voltage increases. During this interval, the auxiliary DC/DC converter is not operating.

When $P_{pv} > P_g$, the scheme operates in Mode II as shown in Fig.5.3. In this mode, the output power from main DC/DC converter is limited by the input power, which generates the current waveform I_{o1} in Fig.5.3. Therefore, there is no excess power to flow into the decoupling capacitor. Rather, the decoupling capacitor supplies power to the output via the auxiliary DC/DC converter to meet the power shortfall and consequently the capacitor voltage reduces.

The general P3 scheme can be implemented with different main DC/DC power converters and with different auxiliary DC/DC converters. In the next subsection, one

particular implementation of the P3 scheme is introduced and this implementation is investigated in the rest of this chapter and in Chapter 6.

5.2.2. A Pilot Power Topology for the P3 Scheme

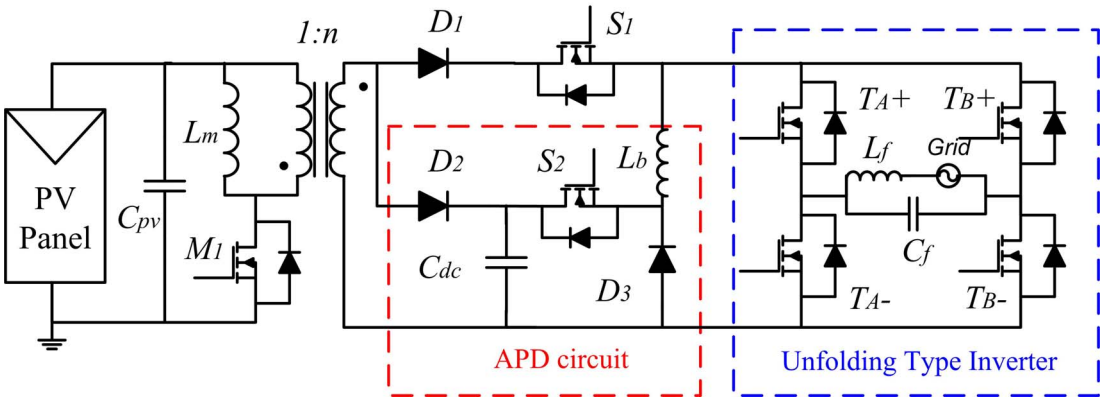


Fig.5.4: A Pilot Power Topology for the P3 Scheme

One pilot topology for the proposed P3 scheme is shown in Fig.5.4, where the power circuit is composed of three stages: flyback converter, APD circuit and unfolding type inverter (UFI). This pilot topology without UFI has been adopted in Power Factor Correction (PFC) application in [121]. For microinverter application, it is necessary to restudy its operation and design for different input/output specifications.

The first stage includes a flyback converter processing 100% of the overall power. The output of the flyback is channeled through two parallel paths with the top path channeling 68.2% of the power while the lower APD circuit is in charge of delivering 31.8% of the power. For ease of control, the flyback converter and the buck converter have both been made to work in DCM mode. The function of the first stage includes MPPT, input and output isolation, output current waveform

shaping and power decoupling.

A flyback converter has been selected as the main DC/DC converter due to the following reasons. The circuit is simple and adding a second leg is easy. In DCM, the input power can be easily controlled regardless of the output characteristics. This makes MPPT control completely independent from the output side control.

A buck converter is a natural fit for the auxiliary DC/DC converter as the AC voltage reduces to zero while the decoupling capacitor voltage is desired to be high. Non-synchronous buck converter is used here as the input voltage is high, which makes the voltage drop on diode relatively small and a reverse energy flow is not desired.

The third stage is an unfolding type inverter which converts the DC current into AC current in phase with the grid voltage. The power loss in this stage is small due to the fact that the switches are switched at low frequency and under zero current zero voltage conditions.

5.3 Operation and Design of the Pilot Topology

This section focuses on the detailed analysis and design of the topology proposed in Section 5.2.2 above. It starts with the selection of the DC link capacitor based on power decoupling requirement and also the limit imposed due to the buck converter operation. Once the decoupling capacitance value and its operating voltage are defined, the input and output specifications of the flyback converter and

buck converter are defined as well. Following that, the operation and design of the main DC/DC converter will be considered in detail. Finally, a brief discussion of the auxiliary DC/DC converter will be presented.

In the analysis below, some assumptions are made to simplify the discussion:

It is assumed that the maximum power point has been reached; therefore, the PV panel is replaced by a constant voltage source at MPP.

The input capacitor is used to filter the high frequency switching ripple only. It is not included here as the input voltage is assumed to be constant.

The unfolding type inverter is not relevant to the system dynamics. Therefore, it is replaced by a rectified sinusoidal voltage source to represent the load.

Lastly, ideal lossless operation of the converters has been assumed.

5.3.1. Design of Decoupling Capacitance

The decoupling capacitance is mainly determined by the power decoupling requirement, which has been discussed earlier in Section 2.3. From (2-2) & (3-5) where k_{rf} is defined as the ratio of the peak-to-peak voltage ripple versus the average voltage, the required capacitance per watt can be presented by:

$$\frac{C_{dc}}{P_{pv}} = \frac{1}{\omega \cdot k_{rf} \cdot V_{C\_dc}^2} \tag{5-6}$$

As the decoupling power is handled by the capacitor,

$$V_C \cdot C_{dc} \frac{dV_C}{dt} = V_{pv} I_{pv} - V_g I_g \tag{5-7}$$

Therefore, the capacitor voltage is given by:

$$\frac{V_C(t)}{V_{C\_dc}} = \sqrt{1 + \frac{P_{pv}}{\omega C_{dc} \cdot V_{C\_dc}^2} \sin(2\omega t)} = \sqrt{1 + k_{rf} \sin(2\omega t)} \tag{5-8}$$

In addition, the selected auxiliary converter topology also places a certain limit on the capacitor voltage value. In this case, due to the use of a buck converter, we need to ensure that $V_C > V_g$ over an AC cycle, which limits the applicable range of the ripple factor.

From (5-7), the following can be derived.

$$[V_C(t)]^2 = V_{C\_dc}^2 \left[1 + k_{rf} \sin(2\omega t)\right] \tag{5-9}$$

The limit of $V_C > V_g$ leads to:

$$1 + k_{rf} \sin(2\omega t) > k_v \sin^2(\omega t), \tag{5-10}$$

where $k_v = \frac{\sqrt{2} V_{rms}}{V_{C\_dc}}$ is defined as a voltage factor.

Equation (5-10) can be further changed to:

$$\left(1 - \frac{k_v^2}{2}\right) + A \sin(2\omega t + \varphi) > 0, \tag{5-11}$$

$$\text{where } A = \sqrt{k_{rf}^2 + \frac{k_v^4}{4}} \text{ and } \tan(\varphi) = \frac{k_v^2}{2k_{rf}} \tag{5-12}$$

In order to make sure (5-11) is valid over an AC cycle the limit placed by the buck converter on the system design is:

$$\left(1-\frac{k_v^2}{2}\right)-A>0 \tag{5-13}$$

Therefore,

$$k_{rf}^2+k_v^2<1 \text{ or } k_v<\sqrt{1-k_{rf}^2} \tag{5-14}$$

The upper limit on k_v imposed by (5-14) can also be viewed as a lower limit on the DC link voltage for a given AC supply voltage.

Combining (5-6) and (5-14), the capacitance per watt is limited to:

$$\frac{C_{dc}}{P_{pv}}<\frac{1}{2\omega\cdot V_{rms}^2}\cdot\frac{1-k_{rp}^2}{k_{rp}} \tag{5-15}$$

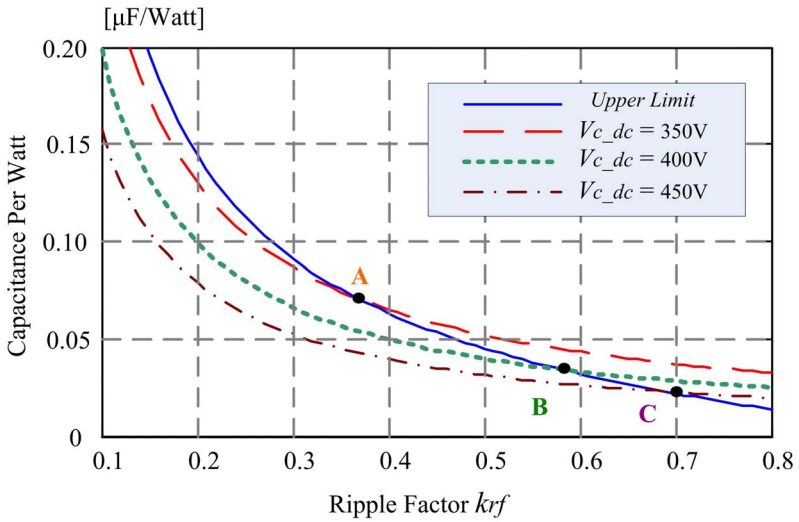


Fig.5.5: Relationship between capacitance/watt and ripple factor for different DC link voltages.

The limit expressed by (5-15) is shown as an upper limit in Fig.5.5 for an AC voltage of 230 V_{rms} at a frequency of 50 Hz. Here, design choices to the left and below the upper limit are acceptable while choices to the right and above the boundary are not. For example, when the decoupling capacitor average voltage is designed to be 350V, the maximum ripple factor allowed is at point "A". Thus the capacitance per watt must be higher than 0.07μF/watt. However, by choosing

V_{C_dc} = 400 V or 450V, the maximum allowable ripple factor can be higher (point "B" and "C"), which corresponds to a lower minimum capacitance of 0.035 or 0.025μF/watt. Thus, by choosing the DC link voltage slightly higher, we can reduce the capacitance requirement significantly.

In the present work, a DC voltage of 400V is selected with a ripple factor of 0.2, which corresponds to a decoupling capacitance around 20μF for power rating of 200W. This design results in a capacitor voltage around 360V to 440V at full power level under steady state condition.

5.3.2. Dual-Output Flyback Converter Design

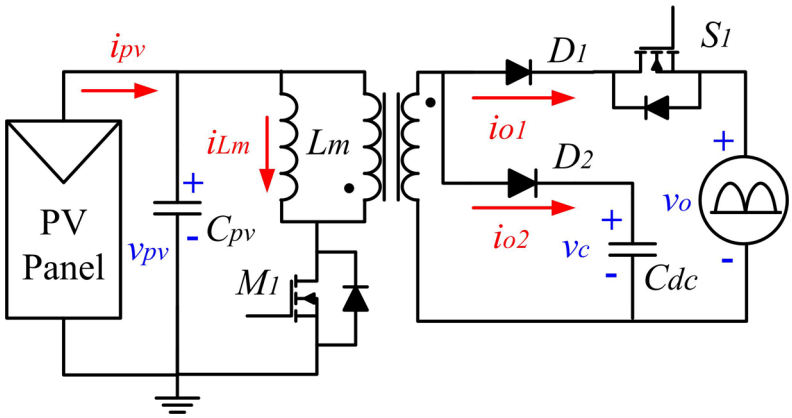


Fig.5.6: Dual Output Flyback Converter

Based on the assumptions mentioned at the start of this section (Section 5.3), the dual-output flyback converter has been redrawn in Fig.5.6.

The flyback converter is designed for DCM operation. The main switch M1 on the input side is used to control the input power from PV panel to ensure that the Maximum Power Point is reached. In this case, the primary side voltage and current of flyback transformer are completely independent from secondary side operation,

which makes MPPT tracking easy and independent from the operation of the secondary side circuit. The secondary side switch S1 is used to control the power flow either to the UFI or to the DC link capacitor. It is placed at the low output voltage port rather than high voltage port, which is critical to ensure the output power flows to low voltage port as long as S1 is on.

Depending on whether the input power is higher than the grid output power or not, the converter operates in two modes. The operating waveforms are illustrated in Fig.5.7. Here, the duty cycle of the switch M1 is d and the conduction duty cycles of diodes D1 and D2 are d_1 and d_2, respectively.

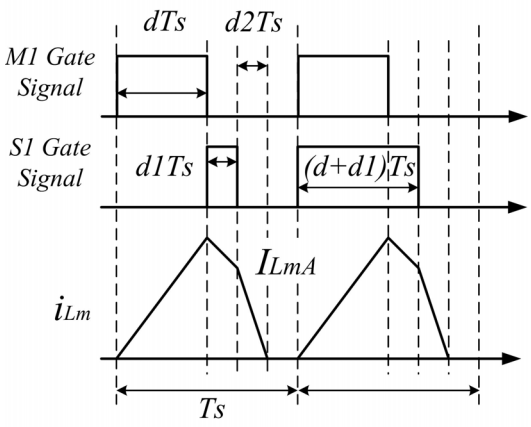
In Fig.5.6, the magnetizing inductance L_m of the transformer has been shown separately across the primary winding for ease of understanding. The current, i_{Lm}, in Fig.5.7 will flow on the primary side during the interval dT_S and during the interval d_1T_S, a current of i_{Lm}/n will flow via the secondary winding.

1) Mode I:

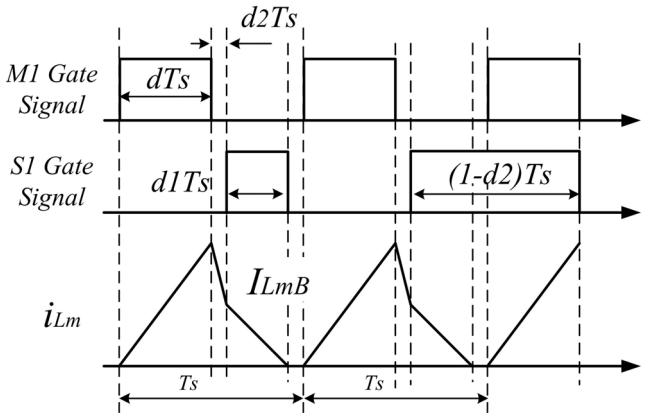
When $P_{pv} > P_g$, the converter works in Mode I in which some of the power ($=P_{pv} - P_g$) from the panel is diverted to the DC link capacitor. During this mode, the auxiliary buck converter is off.

Here, both D1 and D2 conduct within a switching period, thereby transferring power from the panel both to the grid and to the DC link capacitor in each switching period. Depending on the order in which D1 and D2 are made to conduct, two

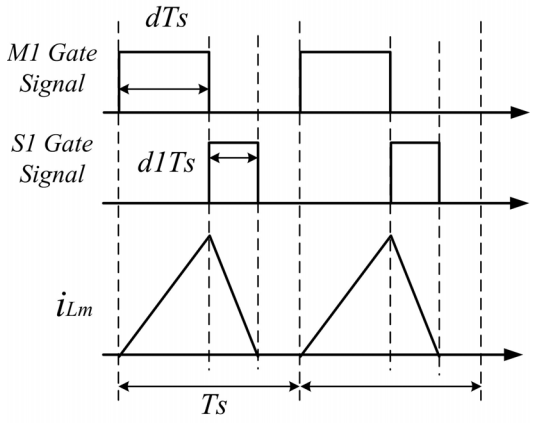
switching sequences (Schemes A & B) are possible.



(a) Mode I ($P_{pv} > P_g$, Scheme A)



(b) Mode I ($P_{pv} > P_g$, Scheme B)



(c) Mode II ($P_{pv} < P_g$, both schemes)

Fig.5.7: Operating waveforms of the Dual-Output flyback converter

In Scheme A (see Fig.5.7 (a)), when M1 is turned off, S1 is turned on immediately and the power flows to the grid output first. After S1 is turned off, the remaining power in the flyback transformer is transferred to the DC link capacitor.

In Scheme B (see Fig.5.7 (b)), when M1 is off, S1 remains off, which causes the energy in the flyback transformer to flow into the DC link capacitor first. After that, switch S1 is turned on, which causes the remaining energy in the flyback transformer to be delivered to the output. Since the output voltage is lower than the DC link capacitor voltage, diode D2 will be reverse-biased automatically.

2) Mode II:

During the interval when $P_{pv} < P_g$, the converter operates in Mode II in which the full panel power is directly transferred to the grid. Diode D2 does not conduct at all in this mode and the converter works as a single-ended flyback converter. The auxiliary buck converter provides the additional power ($= P_g - P_{pv}$) to be fed to the grid. This mode is common for both switching schemes A and B.

5.3.2.1. Design of L_m and n

Mainly, the design of the flyback converter involves the determination of the values of the primary side magnetizing inductance, L_m, and the transformer turns ratio, n.

1) Primary side magnetizing inductance L_m

Based on the DCM operating waveforms of a flyback converter,

$$L_m = \frac{V_{pv}^2 \cdot d^2 \cdot T_s}{2P_{pv}} \tag{5-16}$$

Given the switching frequency, $f_s\ (=1/T_s)$, L_m is determined by the PV panel power to be handled as well as the PV module voltage.

Equation (5-16) is valid for both Mode I & Mode II operation and with both switching schemes.

2) Turns ratio n

Given the magnetizing inductance, L_m, the value of n is chosen so that DCM operation is ensured under all conditions. The worst case for flyback converter in DCM operation is studied below at the maximum input power level $P_{\max}$. As the flyback converter operates in two modes in one AC cycle and has two different switching schemes in Mode I, DCM operation in both modes and for each switching scheme will be guaranteed individually.

Firstly, in Mode II, the flyback converter in both switching schemes works in constant power transfer mode with D2 off all the time. Therefore, the duty cycle d_1 is:

$$d_1 = \frac{nV_{in}}{V_o} d \tag{5-17}$$

In this case, a larger grid voltage leads to smaller d_1. Therefore, the maximum

duty cycle occurs at the minimum grid voltage at this mode, i.e. V_{rms}. Since DCM operation requires $d + d_1 \le 1$, the relationship between n and L_m in this mode can be derived from (5-16) and (5-17).

$$n \le V_{rms}\left[\sqrt{\frac{T_s}{2P_{pv}L_m}} - \frac{1}{V_{pv}}\right] \tag{5-18}$$

In Mode I, the magnetizing current is divided into three pieces as shown in Fig.5.7 a) and b).

Firstly, assuming lossless operation of the flyback converter, the switching-period average power balance between the input and output is given by:

$$V_{pv}I_{pv} = V_o I_{o1} + V_C I_{o2} \tag{5-19}$$

where V_{pv}, V_o and V_C represent the switching-period average voltage of PV panel, output voltage and capacitor voltage. The symbols I_{pv}, I_{o1} and I_{o2} represent the switching period average values of 1) input current, 2) output current through D1,S1 and 3) output current through D2.

Secondly, based on the consideration that the core magnetizing current must be reset to zero in each cycle under DCM, the following equation is obtained.

$$V_{pv}d = V_o\frac{d_1}{n} + V_C\frac{d_2}{n} \tag{5-20}$$

Comparing the current waveforms of the two switching schemes, it is observed that 1) the peak magnetizing current is the same; and 2) the average current of the secondary side diodes is the same in both scheme A and B. As a result, the conduction time of the secondary side diodes in Scheme A is shorter than that in

Scheme B. The design worst cases to ensure that the operating stays in DCM for both the schemes are studied below.

Scheme A

In Scheme A, the secondary side current flows into the lower voltage side (grid side) first. When the grid voltage goes up, the reference current also goes up with the reduction of the capacitor's charging current. As a result, d_1 increases but d_2 reduces. Therefore, it is difficult to find the maximum total conduction duty cycle ($d_1 + d_2$) without more detailed evaluation.

Based on the current waveform in Fig.5.7 a), the capacitor charging current for scheme A can be obtained as:

$$I_{o2} = \frac{V_C}{2L_m} {d_2}^2 T_s \tag{5-21}$$

Inserting (5-16) into (5-21), the duty cycle value d_2 can be found.

$$d_2 = \sqrt{\frac{V_{pv}}{I_{pv}} \frac{I_{o2}}{V_C}} \cdot nd \tag{5-22}$$

According to (5-20), the duty cycle value d_1 is given by:

$$d_1 = \frac{nV_{pv}d - V_C d_2}{V_o} \tag{5-23}$$

In order to maintain DCM operation all the time, $d + d_1 + d_2 \le 1$. Based on (5-23), (5-22) and (5-16),

$$n \le \left(\sqrt{\frac{T_s}{2P_{pv}L_m}} - \frac{1}{V_{pv}} \right) \Bigg/ \left[\frac{1}{V_o} + \left(\frac{1}{V_C} - \frac{1}{V_o} \right) \sqrt{1 - \frac{V_o^2}{V_{rms}^2}} \right] \tag{5-24}$$

Considering (5-18) and (5-24) in mode I and II together, the relationship between L_m and n for switching scheme A can be summarized as:

$$n_A \le \left(\sqrt{\frac{T_s}{2P_{pv}L_m}} - \frac{1}{V_{pv}} \right) \Big/ k_A \tag{5-25}$$

$$k_A = \begin{cases} \dfrac{1}{V_{rms}} & (\text{mode II}) \\ \dfrac{1}{V_o} + \left(\dfrac{1}{V_C} - \dfrac{1}{V_o} \right) \sqrt{1 - \dfrac{V_o^2}{V_{rms}^2}} & (\text{mode I}) \end{cases} \tag{5-26}$$

As the numerator of (5-25) can be considered a constant over an AC cycle, the variation of (5-25) depends on the variation of k_A, which is illustrated in Fig.5.8.

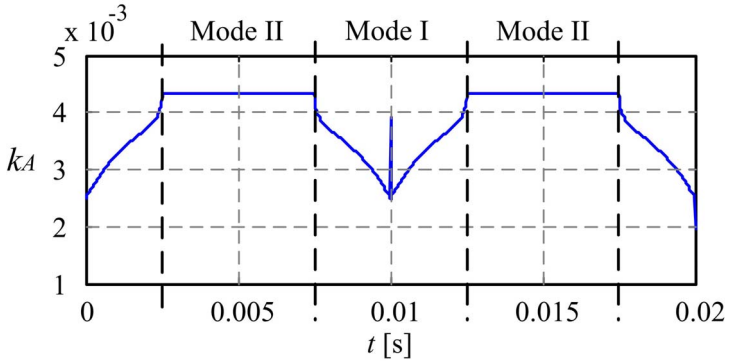


Fig.5.8: Variation of k_A over AC cycle

According to (5-26) and Fig.5.8, the worst case value of k_A (i.e. the maximum value) occurs in Mode II at maximum power level $P_{\max}$. The maximum turns ratio is therefore:

$$n_{\max A} = V_{rms} \left[\sqrt{\frac{T_s}{2P_{\max}L_m}} - \frac{1}{V_{pv}} \right] \tag{5-27}$$

Scheme B

A similar analysis is carried out for scheme B. The conduction duty cycle d_1

of diode D1 is constant at a given power level as shown below.

$$I_{o1} = \frac{V_o}{2n^2 L_m} d_1^2 T_s \tag{5-28}$$

The conduction duty cycle d_2 of the diode D2 is found by:

$$d_2 = \frac{nV_{pv} d - V_o d_1}{V_C} \tag{5-29}$$

The conduction duty cycle d_2 reaches its maximum when $V_o = 0$.

Again, in order to operate in DCM mode, $d + d_2 + d_1 \le 1$. Therefore,

$$n \le \left(\sqrt{\frac{T_s}{2P_{pv} L_m}} - \frac{1}{V_{pv}} \right) \Bigg/ \left[\frac{1}{V_C} + \frac{1}{V_{rms}} - \frac{V_o}{V_C \cdot V_{rms}} \right] \tag{5-30}$$

Considering (5-18) and (5-30) in mode I and II together, the relationship between L_m and n for switching scheme B can be summarized as:

$$n_B \le \left(\sqrt{\frac{T_s}{2P_{pv} L_m}} - \frac{1}{V_{pv}} \right) \Big/ k_B \tag{5-31}$$

$$k_B = \begin{cases} \dfrac{1}{V_{rms}} & (\mathrm{mode\ II}) \\ \dfrac{1}{V_C} + \dfrac{1}{V_{rms}} - \dfrac{V_o}{V_C \cdot V_{rms}} & (\mathrm{mode\ I}) \end{cases} \tag{5-32}$$

Again, the variation of (5-31) over an AC period depends on the variation of k_B, which is illustrated in Fig.5.9.

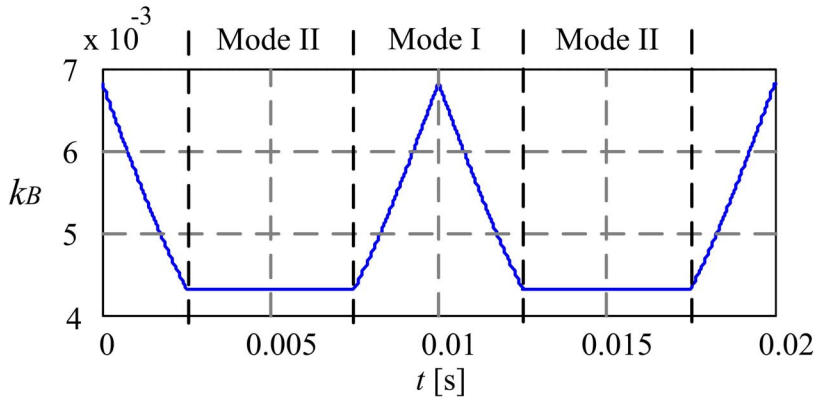


Fig.5.9: Variation of k_B over AC cycle

According to (5-32) and Fig.5.9, the worst case value of k_B (i.e. the maximum value) occurs during the zero crossing of AC cycle in Mode I at maximum power level $P_{\max}$. The maximum turns ratio is therefore:

$$n_{\max B} = \left(\sqrt{\frac{T_s}{2P_{\max} L_m}} - \frac{1}{V_{pv}} \right) \Bigg/ \left(\frac{1}{V_C} + \frac{1}{V_{rms}} \right) \tag{5-33}$$

3) Summary

In summary, the choice of L_m and n should satisfy the equations below based on the input and output specifications.

$$L_m = \frac{V_{pv}^2 \cdot d^2 \cdot T_s}{2P_{pv}} \tag{5-16}$$

$$n_{\max A} = V_{rms} \left[\sqrt{\frac{T_s}{2P_{\max} L_m}} - \frac{1}{V_{pv}} \right] \text{ - Scheme A} \tag{5-27}$$

$$n_{\max B} = \left(\sqrt{\frac{T_s}{2P_{\max} L_m}} - \frac{1}{V_{pv}} \right) \Bigg/ \left(\frac{1}{V_C} + \frac{1}{V_{rms}} \right) \text{ - Scheme B} \tag{5-33}$$

In our study, Kyocera's PV module KC200GT is used to feed power to a grid with RMS value of 230V and 50Hz. A switching frequency of 100 kHz is selected to

reduce the size of magnetic components.

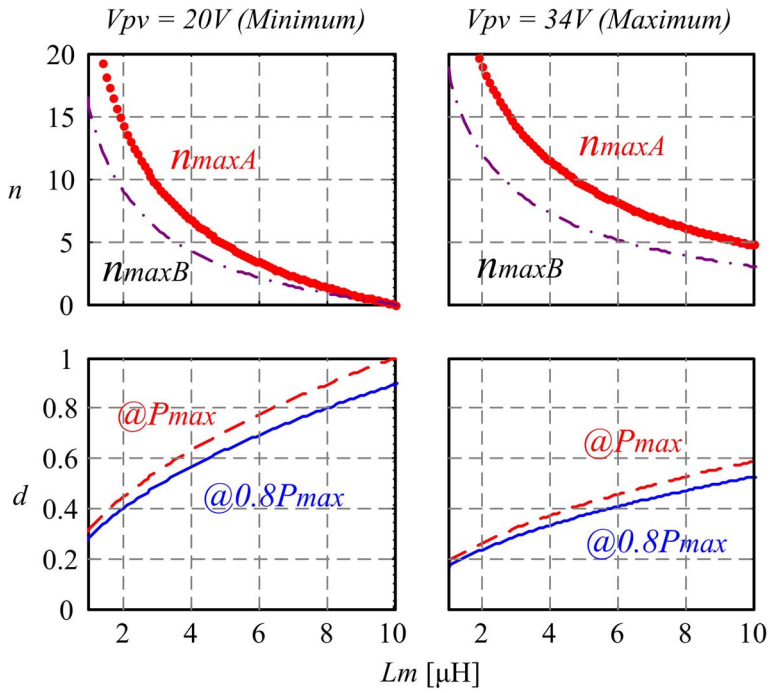


Fig.5.10: Design of L_m and n for KC200GT at min. and max. PV MPPT voltage

The value of L_m is chosen so as to make the duty cycle around 0.5 under NOCT condition at 800W/m^2.

$$L_m = 4\mu H \tag{5-34}$$

This would ensure that narrow duty cycle operation with high peak current is avoided on both the primary and secondary sides. In this case, if scheme A is used, according to (5-27) :

$$n_{\max A} = 6.7 \;\Rightarrow\; n_A = 6 \tag{5-35}$$

If scheme B is used, according to (5-33):

$$n_{\max B} = 4.3 \;\Rightarrow\; n_B = 4 \tag{5-36}$$

5.3.2.2. Component Stresses

Once a preliminary design is carried out, calculation of component stress is necessary to aid selecting both active and passive power components and to evaluate the design.

Firstly, for active components (M1, S1, D1 and D2), the voltage stress can be calculated respectively below:

$$V_{M1} = V_{pv} + V_C / n \quad \text{when} \quad D_1 \text{ is conducting;} \tag{5-37}$$

$$V_{S1} = V_C - V_o \quad \text{when} \quad D_2 \quad \text{is conducting;} \tag{5-38}$$

$$V_{D1} = nV_{pv} + V_o \quad \text{when} \quad M_1 \text{ is conducting;} \tag{5-39}$$

$$V_{D2} = nV_{pv} + V_C \quad \text{when} \quad M_1 \text{ is conducting} \tag{5-40}$$

The peak current and RMS current for M1 are:

$$i_{M_1,p} = \sqrt{\frac{2T_s}{L_m} \cdot P_{pv}} \tag{5-41}$$

$$i_{M_1,rms} = i_{M_1,p} \cdot \sqrt{\frac{d}{3}} \tag{5-42}$$

In Scheme A, the peak and RMS current for S1&D1 is:

$$i_{D_1,p} = \frac{i_{M_1,p}}{n} \tag{5-43}$$

$$i_{D_1,rms} = \frac{1}{n}\sqrt{d_1\left[(i_{D_1,p} - \frac{V_o}{2nL_m}d_1T_s)^2 + \frac{1}{12}\left(\frac{V_o}{nL_m}d_1T_s\right)^2\right]} \tag{5-44}$$

The peak and RMS current for D2 is:

$$i_{D_2,p} = \frac{V_C}{n^2 L_m} d_2 T_s \tag{5-45}$$

$$i_{D_2,rms} = i_{D_2,p} \cdot \sqrt{\frac{d_2}{3}} \tag{5-46}$$

In Scheme B, the equations are changed to:

$$i_{D_1,p} = \frac{V_o}{n^2 L_m} d_1 T_s \tag{5-47}$$

$$i_{D_1,rms} = i_{D_1,p} \cdot \sqrt{\frac{d_1}{3}} \tag{5-48}$$

$$i_{D_2,p} = \frac{i_{M_1,p}}{n} \tag{5-49}$$

$$i_{D_1,rms} = \frac{1}{n}\sqrt{d_2\left[(i_{D_2,p} - \frac{V_C}{2nL_m} d_2 T_s)^2 + \frac{1}{12}\left(\frac{V_C}{nL_m} d_2 T_s\right)^2\right]} \tag{5-50}$$

Table 5.1: Voltage and Current Stresses of MOSFET and Diodes ($L_m = 4\mu H$)

	Scheme A		Scheme B
	$n = 6$	$n = 4$	$n = 4$
Voltage stress (V) [1]			
$\hat{V}_{M1}$	107	144	144
$\hat{V}_{S1}$	400	400	400
$\hat{V}_{D1}$	529	461	461
$\hat{V}_{D2}$	644	576	576
Currents Stress (A) [2]			
$\hat{i}_{M1,p}$	31.6	31.6	31.6
$\hat{i}_{M1,rms}$	12.5	14.5	14.5
$\hat{i}_{D1,p}$	5.3	7.9	11.2
$\hat{i}_{D1,rms}$	1.8	2.5	3.0
$\hat{i}_{D2,p}$	5.3	7.9	7.9
$\hat{i}_{D2,rms}$	1.3	1.6	2.4

[1]: based on $V_{pv,\max} = 34V$; [2]: based on $P_{\max} = 200W$ & $V_{pv,\min} = 20V$

Table 5.1 tabulates the components voltage stress as well as current stress calculated according to (5-37)~(5-50) for different designs in both schemes. It may be noted that Scheme B design with $n = 6$ is not possible.

As shown in Table 5.1, when the same values of n and L_m are used for both schemes, Scheme A has less RMS and Peak current stresses compared to Scheme B. Other than that, Scheme A is able to use a larger turns ratio n, which results in an even less RMS and peak current stresses for secondary side components. Therefore, Scheme A is a more favorable design in terms of potential higher efficiency. Though this is the case, during control study, Scheme B was found to be simpler to control. Hence, Scheme B this has been pursued in this work. This aspect is discussed in greater detail in Chapter 6.

5.3.3. Buck Converter Design

As discussed above and shown in Fig.5.3, the auxiliary DC/DC converter, in this case a buck converter, will only operate in Mode II, i.e., when $P_{pv} < P_g$.

Fig.5.11 shows the simplified circuit diagram of the buck converter in Mode II. In this figure, the main DC/DC converter, i.e. flyback converter is modeled as a current source i_{o1}, which is determined by the input power from flyback converter.

This buck converter is also designed to operate in DCM mode, rather than CCM for several reasons. Firstly, the current is rather small (less than 1A), which does not impose much current stress on components. Secondly, the control transfer

function of the buck converter in DCM is a constant, as is the case with the Main DC/DC flyback converter. In addition, the value of this constant gain is also close to each other. This is useful in the next Chapter to design the current controller, which can be used for both converters.

Following well established techniques, the maximum buck inductance to ensure DCM operation at the full power rating is obtained as given below.

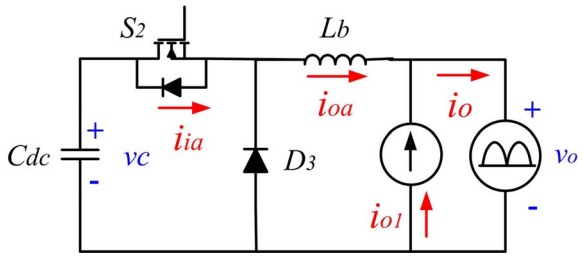


Fig.5.11: Circuit diagram of the auxiliary buck converter

In order to operate in DCM mode, the following equation must be satisfied:

$$d_3 + d_3^{'} < 1 \tag{5-51}$$

where d_3 is the duty cycle of S2 and $d_3^{'}$ is the conduction duty cycle of the rectifier diode D3.

Applying inductor volt-sec balance to L_b,

$$\left(V_C - V_o\right) \cdot d_3 = V_o \cdot d_3^{'} \tag{5-52}$$

The value of d_3 can be calculated based on steady state output current of the buck converter as:

$$I_{o3} = \frac{1}{2}\left(d_3 + d_3^{'}\right) \times \frac{V_o}{L_b} d_3^{'} T_s = \frac{T_s}{2L_b} \cdot \frac{V_C}{V_o} \cdot \left(V_C - V_o\right) \cdot d_3^2 \tag{5-53}$$

The output current of the buck converter I_{o3} can be calculated from the power balance equation in each switching cycle,

$$I_{o3} = \frac{P_g - P_{pv}}{V_o} = \frac{V_o^2 - V_{rms}^2}{R_g V_o} \tag{5-54}$$

Here, the effective load resistance R_g is related to the power level assuming no power loss between input and output:

$$R_g = \frac{V_{rms}}{I_{rms}} = \frac{V_{rms}^2}{P_{pv}} \tag{5-55}$$

Substituting (5-52) to (5-54) into (5-51), it is derived that

$$L_b < \frac{1}{2} R_g T_s \cdot \frac{\left(1 - \frac{V_o}{V_C}\right)}{1 - \frac{V_{rms}^2}{V_o^2}} \tag{5-56}$$

Therefore, the maximum buck inductance to ensure DCM operation at the maximum power level and over an AC cycle is calculated as:

$$L_{b,max} = \frac{1}{2} R_{g,min} T_s \cdot \frac{\left(1 - \frac{V_{o,max}}{V_C}\right)}{1 - \frac{V_{rms}^2}{V_{o,max}^2}} = 4.96 \times 10^{-4} H \tag{5-57}$$

In our design, the chosen buck converter inductance is:

$$L_b = 0.4mH \tag{5-58}$$

5.4 Verification through Simulation

The pilot topology of the P3 scheme was verified by simulation (PLECS/Simulink). The main purpose of the simulation is to verify the effectiveness of the proposed APD scheme, which aims to reduce the required capacitance for power decoupling. Therefore, the PV module is modeled in the simulation using

equations (3-7)-(3-9), whose parameters can be abstracted from the manufacturer's datasheet [123] in order to demonstrate the actual power decoupling operating waveforms in different schemes. The PV module model parameters used are tabulated in Table 5.2

Table 5.2: PV module KC200GT model parameters under STC

Description	Value
Maximum power voltage V_{mp}	26.3V
Maximum power current I_{mp}	7.61A
Open circuit voltage V_{oc}	32.9V
Short circuit current I_{sc}	8.21A
I_s calculated from (3-9)	0.178μA
$m\lambda V_t$ calculated from (3-8)	2.523V

If the APD circuit (including the secondary leg of the flyback converter and the auxiliary buck converter) in the proposed topology is not present, the remaining flyback converter would require a large electrolytic capacitor to provide power decoupling. This flyback inverter is used as the benchmark and the simulation results are presented in Section 5.4.1. Following this, the simulated operating waveforms of the proposed topology with the APD circuit is presented and discussed in Section 5.4.2.

5.4.1. A Flyback-DCM Inverter (without APD)

In this part, a flyback-DCM inverter (similar to the benchmark inverter studied in Chapter 3 but with a different UFI configuration) shown in Fig.5.12 is used as a benchmark to demonstrate the power decoupling requirements for the input capacitance.

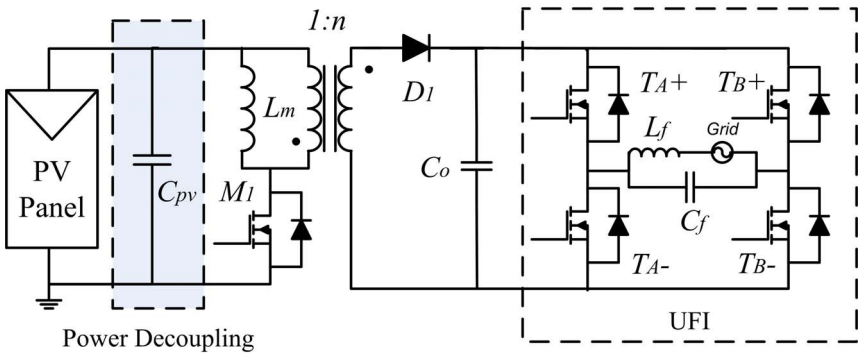


Fig.5.12: Circuit diagram of a flyback-DCM inverter with UFI

The main circuit parameters are tabulated in Table 5.3, which are similar to the parameters used in Table 3.2. It is highlighted here that PV side capacitance uses theoretically calculated value 11.6mF based on MPPT and output power quality requirements discussed in Section 3.3. The circuit in Fig.5.12 is controlled using an open-loop approach (as described in Fig.3.12 (a) in Section 3.4.2), where the duty cycle of switch M1 directly follows a rectified sinusoidal signal in synchronization with the grid voltage.

Table 5.3: Circuit Parameters in Fig.5.12

	Parameters	Value	Unit
PV side capacitance	C_{pv}	4.7/11.6	mF
Flyback magnetizing inductance	L_m	4	μH
Flyback transformer turns ratio	n	4	
Output capacitance	C_o	0.3	μF
Filter capacitance	C_f	0.9	μF
Filter inductance	L_f	500	μH

Two values for PV side capacitance are used in the simulation. One uses a smaller capacitance of 4.7mF as required by power decoupling function as discussed in Section 3.3.1. The input and output operating waveforms of the benchmark is shown in Fig.5.13.

As shown in Fig.5.13, the PV module voltage ripple is 4.5V and the current

ripple is around 1A, which results in the PV power ranging from 190W-200W. The simulated THD value of the output current is 9.33% with a third harmonic factor of 9.29%. This result verifies the study in Section 3.3.1 that the design of the PV side capacitance needs to consider not only the power decoupling requirement, but also THD of the output current.

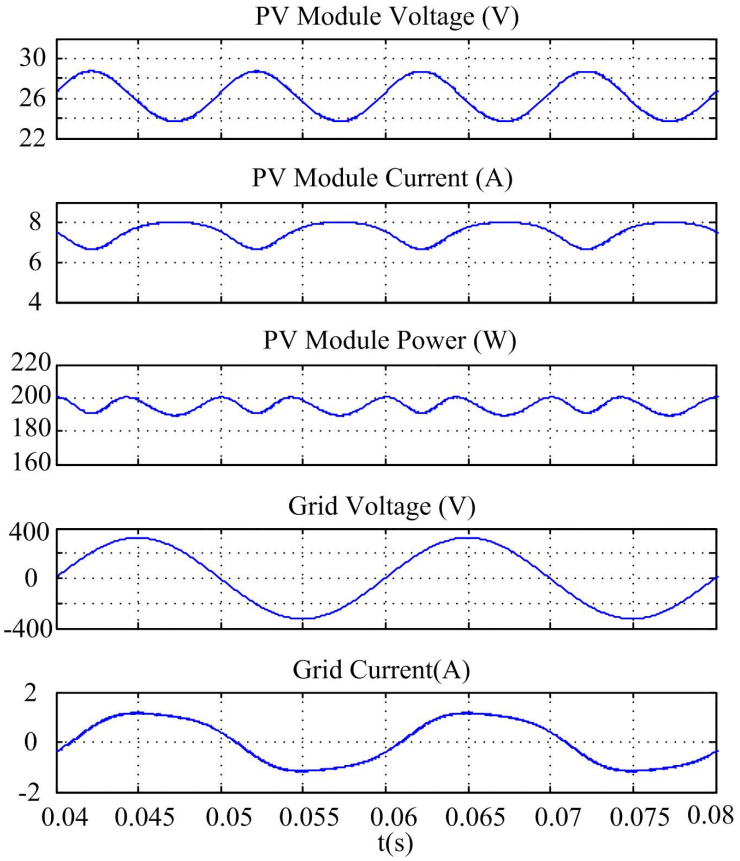


Fig.5.13: Operating waveforms of a flyback-DCM inverter ($C_{pv} = 4.7mF$, $P_{pv} = 200W$, $THD = 9.33\%$, simulation)

When a larger capacitance value is used, i.e. 11.6mF as studied in Section 3.3.2, the input and output operating waveforms are shown in Fig.5.14.

As shown in Fig.5.14, the PV module voltage and current values are subject to a peak-peak voltage ripple of 2V and a peak-peak current ripple of 0.5A at 100Hz

respectively. This corresponds to a voltage ripple factor of 7.6%, which is very close to the calculation result of 8% in Section 3.3.2. As a result, the PV module power is also varying between 197.5 to 200.5W with the average power around 199W at steady state condition.

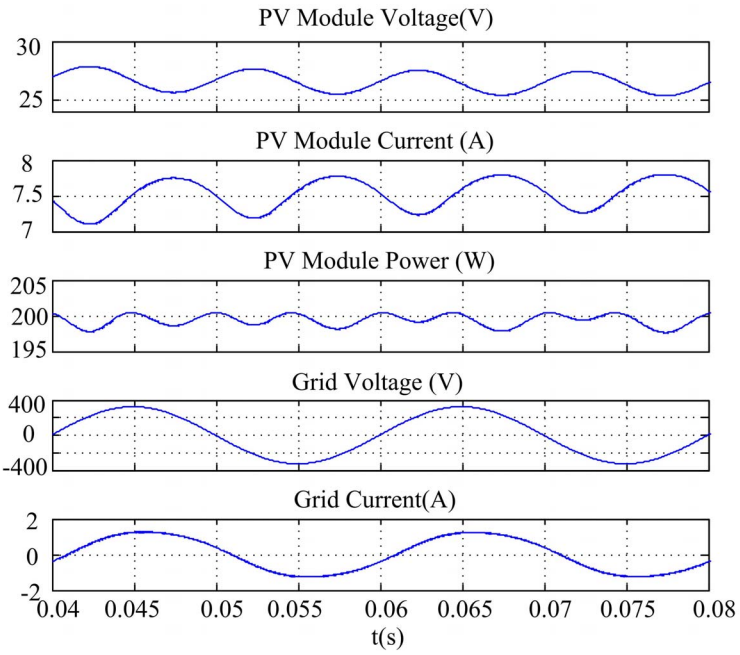


Fig.5.14: Operating waveforms of a flyback-DCM inverter ($C_{pv} = 11.6mF$, $P_{pv} = 200W$, $THD = 4.54\%$,simulation)

The output grid current shows a THD of 4.54% and a third harmonic factor of 3.9%, which is higher than the predicted 2% in Section 3.3.2. The reason for this discrepancy is mainly the control method which influences the PV module current waveform. This means the input decoupling capacitance needs to be increased even further so as to ensure the third harmonic factor of grid current to be below 3%.

Since the power decoupling is carried out at the input PV side capacitor, the main switch M1 works with pulsating power and its instantaneous voltage and

current waveforms are shown in Fig.5.15. The maximum voltage stress and current stress are 112V and 44.8A.

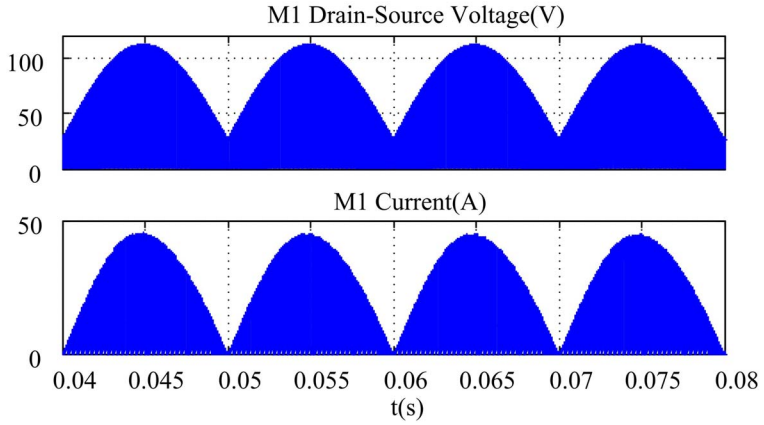


Fig.5.15: Components voltage and current waveforms over AC cycles ($C_{pv} = 11.6mF$, $P_{pv} = 200W$, simulation)

5.4.2. The Pilot Topology (with APD)

The pilot topology studied in Section 5.3 is verified by simulation in this part. Its simulation circuit diagram is redrawn in Fig.5.16 and the main circuit parameters are listed in Table 5.4.

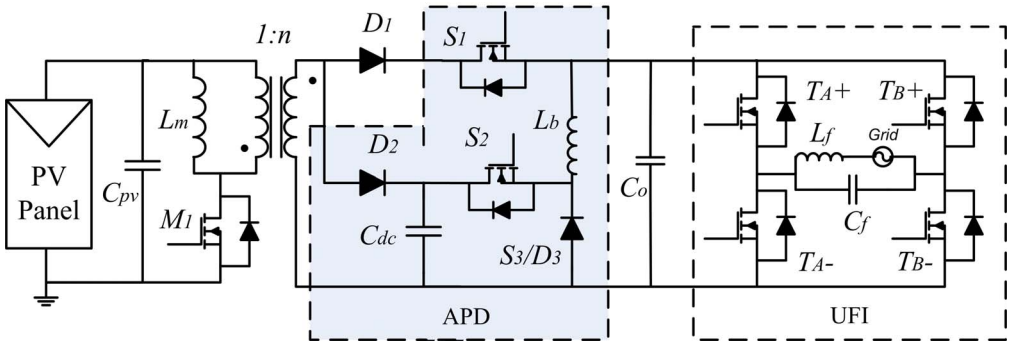


Fig.5.16: Circuit diagram of proposed topology (with APD)

Compared with the benchmark inverter (in Fig.5.12), the main difference is the addition of an APD circuit highlighted in Fig.5.16. In this way, the large electrolytic

capacitor C_{pv} in Fig.5.12 (above 11.6 mF) can be replaced by a film capacitor with relatively smaller capacitance (around 20 μF) so as to filter out the high switching frequency component.

Table 5.4: Circuit Parameters in Fig.5.16

	Parameters	Value	Unit
PV side capacitance	C_{pv}	20	μF
Flyback magnetizing inductance	L_m	4	μH
Flyback transformer turns ratio	n	4	
Power decoupling capacitance	C_{dc}	20	μF
Buck inductance	L_b	0.4	mH
Output capacitance	C_o	0.3	μF
Filter capacitance	C_f	0.9	μF
Filter inductance	L_f	500	μH

In this simulation, the same PV module model in Table 5.2 is used to simulate Kyocera's KC200GT module under STC [123] and its input and output operating waveforms are shown in Fig.5.17. The control of this topology will be discussed in Chapter 6 and the dual-output flyback converter works in Scheme B as discussed above in Section 5.3.2.

As shown in Fig.5.17, the PV module voltage and current do not suffer from 2nd harmonic ripple of the line frequency at 100Hz. Instead, a high switching frequency ripple component is visible in both the PV module voltage and current waveforms. The PV module voltage ripple is around 2V and current ripple is around 0.5A. Similarly, the PV module power varies from 197.5W to 200.5W, with average value around 199W at steady state condition. These high frequency voltage and current ripple components can be further reduced, if required, by increasing the input capacitance.

As expected, the power decoupling capacitor has a peak-to-peak voltage ripple of 80V at 100Hz superposed on the average DC link voltage of 400V, which is the main reason that the input pulsating power at 100Hz is removed. The output current shows a THD of 3.88% with the third harmonic factor below 2.73%, which satisfies the output power factor requirements.

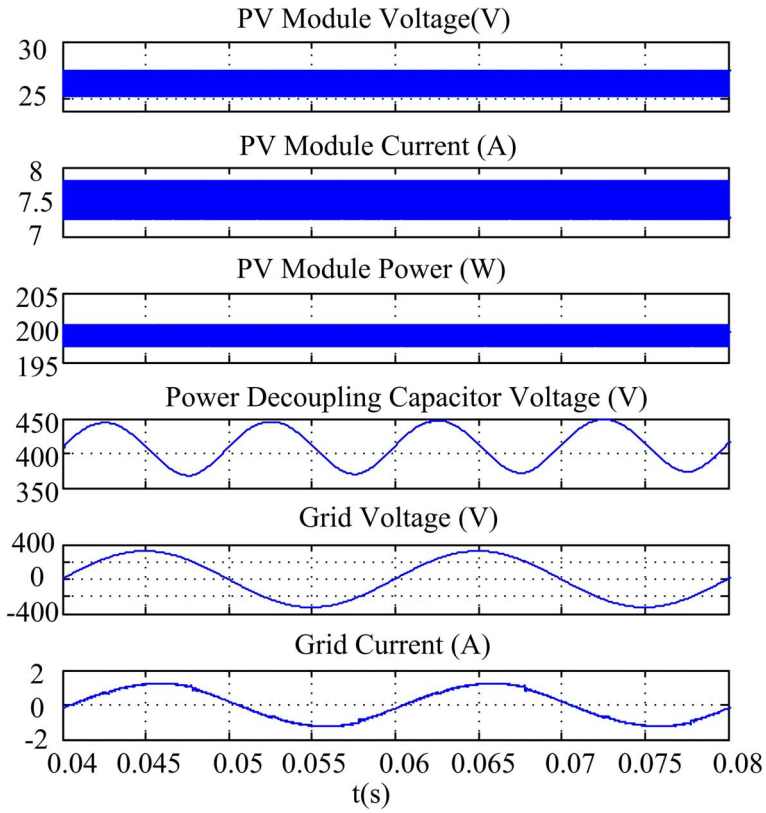


Fig.5.17: Operating waveforms of a flyback-DCM inverter ($P_{pv} = 200W$, $THD = 3.88\%$, Scheme B, Simulation)

The main component voltage and current switching waveforms over AC cycles are shown in Fig.5.18. In the proposed pilot topology, the voltage stress of the main switch M1 is 135V, higher than that of the benchmark inverter without APD (112V) due to a higher decoupling capacitor voltage. The current stress of M1 is 31.6A, which is significantly lower than 44.8A. The main switch M1 and flyback

transformer in both benchmark and the proposed scheme handle the same average power. However, the flyback converter is processing constant power compared to fluctuating power at twice line frequency in the benchmark, which has lower power loss.

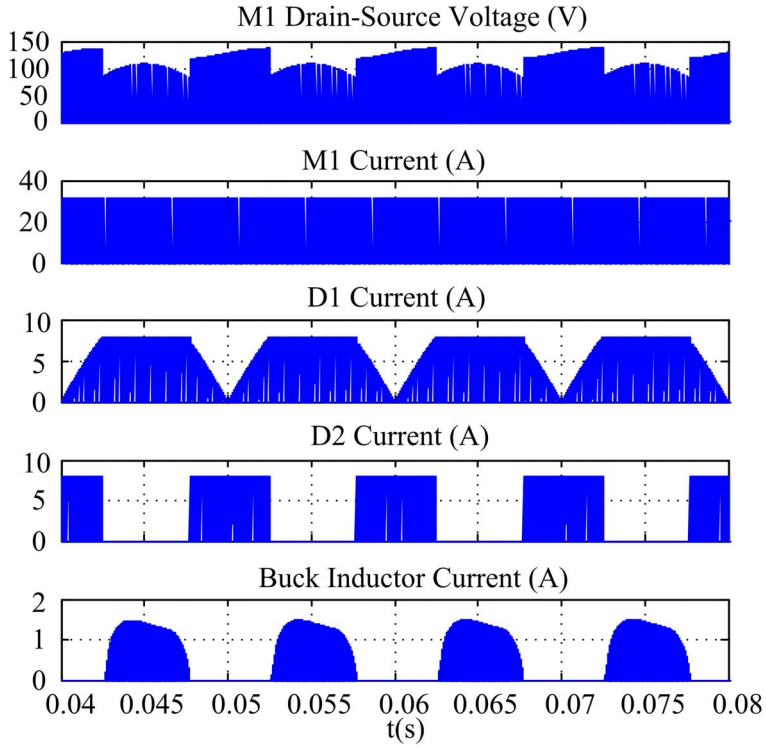


Fig.5.18: Component current and voltage waveforms over AC cycles ($P_{pv} = 200W$,Scheme B, Simulation)

After applying an analog filter in the 'scope' at a cutoff frequency of 1kHz, the average operating waveforms of the main components from simulation are shown in Fig.5.19. The operating waveforms by simulation correspond well with the theoretical average waveforms of the proposed P3 scheme in Fig.5.3.

As shown in Fig.5.19, when the current of D2 is non-zero, the power decoupling capacitor gets charged and the system operates in Mode I.

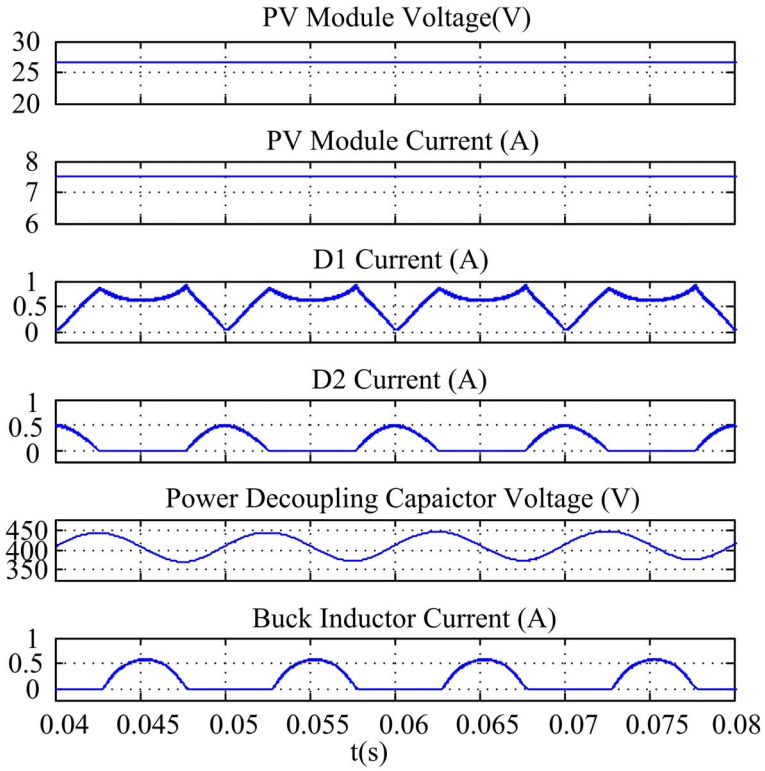
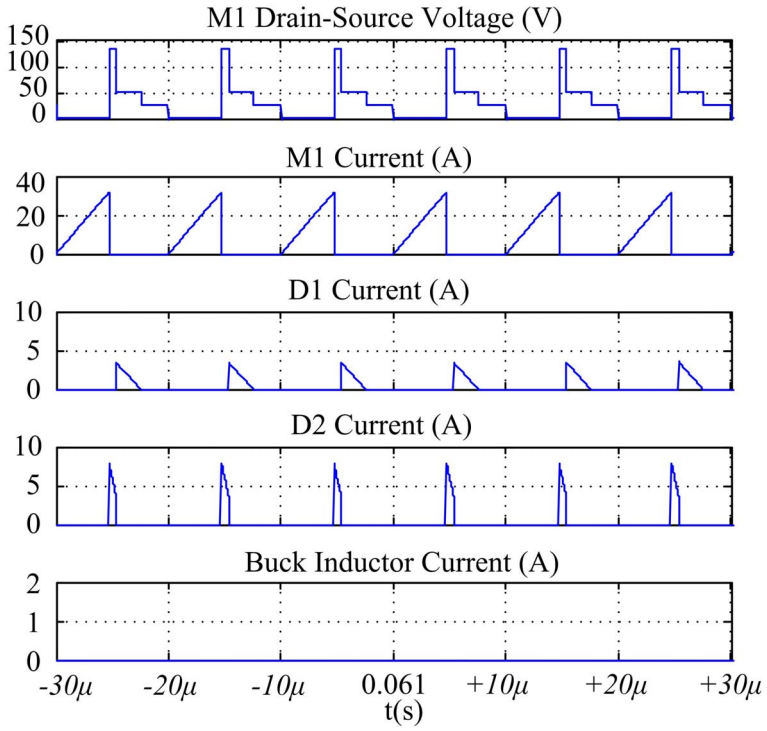


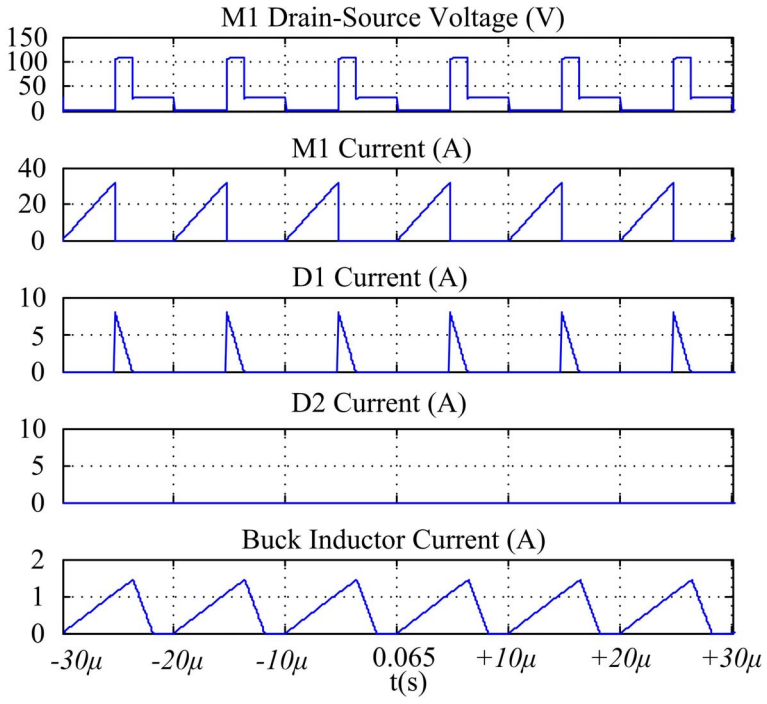
Fig.5.19: Component current and voltage waveforms over AC cycles (with a filter of 1kHz, simulation)

The simulated switching waveforms in Scheme B are shown in Fig.5.20 (a), where the flyback transformer current goes through D2 first and then to D1. In this mode, the buck converter is not active with zero inductor current.

When the current of D2 becomes zero, the power decoupling capacitor gets discharged and the system operates in Mode II. The switching waveforms in this mode are shown in Fig.5.20 (b). The flyback converter converts the constant power from PV module to the grid directly and the buck converter provides the extra power from the decoupling capacitor.



(a) Mode I (Scheme B)



(b) Mode II

Fig.5.20: Switching Waveforms (simulation)

5.5 Implementation, Results and Analysis

A 200W prototype of the proposed pilot topology has been built in the

laboratory for the given specifications and design as shown in Appendix A. The dual-output flyback converter has been designed to operate in Scheme B considering control simplicity, which will be discussed in Chapter 6. The component selection, some hardware implementation issues and solutions are discussed below to provide the guideline and reference for those who meet with the similar issues. Experimental results including both DC-DC operation and DC-AC inversion are also discussed later.

5.5.1. Prototype Implementation

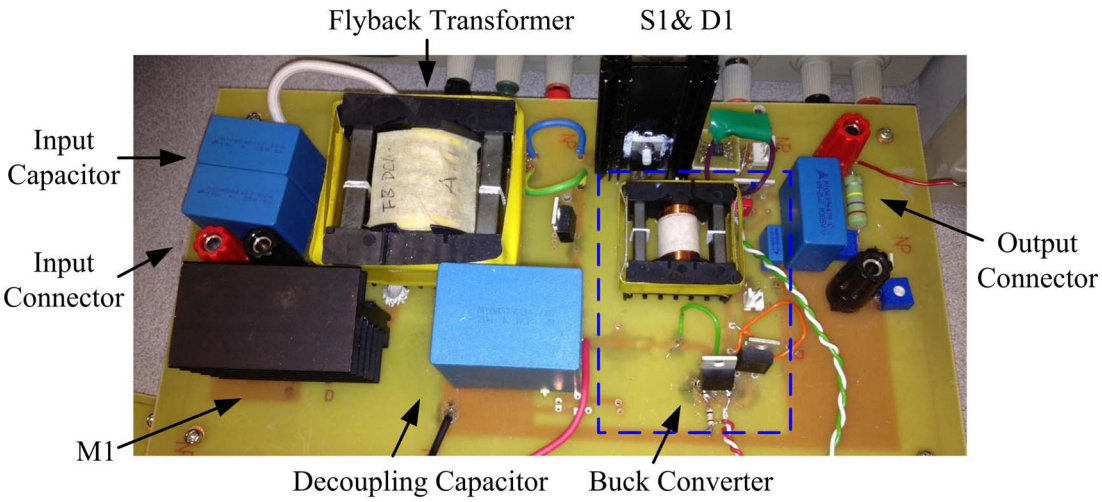
The photos of the prototype are illustrated in Fig.5.21, where two power circuit boards are shown. One of them is the power circuit board of the dual-output flyback converter and the buck converter; the other one is the UFI circuit board.

The details regarding the selected components are given below:

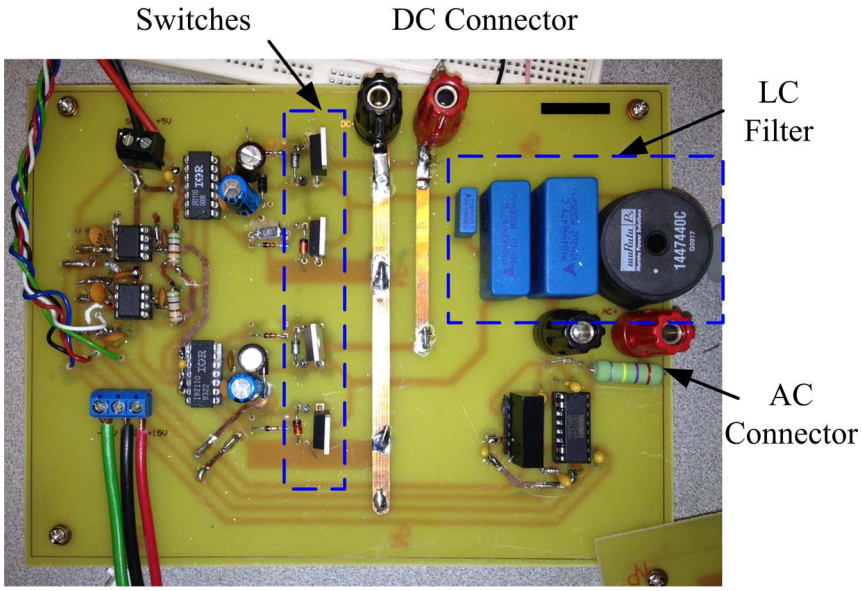
Input side capacitor: 10μF, 250V Film capacitor B32524Q3106K, two capacitors are placed in parallel.

Primary side switch M1: IRFP4668, 200V, 130A MOSFET, $R_{ds,on} = 9.7m\Omega$.

HF transformer: ETD44-3C95 ferrite core (low power loss from 25 to 100^{o}C at frequencies up to 0.5MHz), primary turns N_1=5 turns, 8 strands of SWG 28, secondary turns $N_2 = 20$ turns, 2 strands of SWG 28. Primary side magnetizing inductance $L_m = 4\mu H$. The winding method proposed in [124] is adopted to minimize the leakage inductance.



(a) Dual-output flyback converter and buck converter



(b) UFI (unfolding type inverter)

Fig.5.21: Photos of experimental prototype

Secondary side switch S1: FGP5N60LS, 600V, 5A Field Stop IGBT. Here, IGBT without body diode is selected in order to reduce the current spike of D1 and S1 when M1 is turned off. This aspect is highlighted in Section 5.5.2 below. Handling of this aspect well it is very important to ensure accurate current sensing in order to achieve current shaping control.

Secondary side diodes D1 & D2: IDT04S60C, 600V, 4A SiC diode, 8nC. SiC diode is selected because a low reverse recovery current is required for D2 as it would be turned off at high switching frequency at non-zero value. Selection of D1 will be discussed later together with the component selection of S1.

Power decoupling capacitor: 20uF, 1.1kV film capacitor B32776G0206K.

Buck converter switch S2: CoolMOS IPI60R385CP, 650V, 9A, $R_{ds,on} = 0.385\Omega$.

Buck converter diode D3: IDT04S60C, 600V, 4A SiC diode, 8nC. Here, SiC diode is selected so as to reduce the capacitance across the diode for fast switching.

Buck inductor: ETD29 – 3C95 ferrite core, 80 turns, 1 strand of SWG 26, $L_b = 0.4mH$.

Full bridge UFI switches: IPA60R125CP, 650V, 25A Cool MOS, $R_{ds,on} = 0.125\Omega$

Gate drivers: TC1427 is used to drive primary side MOSFET M1; Opti-isolated IGBT-MOSFET driver FOD3180 is used to drive secondary side MOSFET S1 and IR2110 is used to drive high side MOSFET of buck converter S2.

5.5.2. Dual-Output Flyback Converter in Scheme B: DC-DC Conversion

As discussed in Section 5.3.2, although dual-output flyback converter working

in Scheme A is a more favorable design in terms of a higher efficiency, in this work, Scheme B is pursued due to its simplicity in control. In Scheme B, when the main switch M1 is turned off, the flyback secondary side current is supposed to flow through D2 first and then go through D1 and S1. In this case, selection of D1 and S1 needs careful consideration as discussed below.

Here, the circuit diagram of dual-output flyback converter is drawn in Fig.5.22.

It is noticed that when M1 is conducting, the secondary leg of D1 in series of S1 is under a negative voltage stress following the polarity marked on Fig.5.22. When M1 is turned off and D2 is turned on, the voltage stress across D1 and S2 changes from negative to positive. This switching behavior between positive and negative voltage stress would results in an undesired current spike through S1 and D1 if S1 is not selected properly.

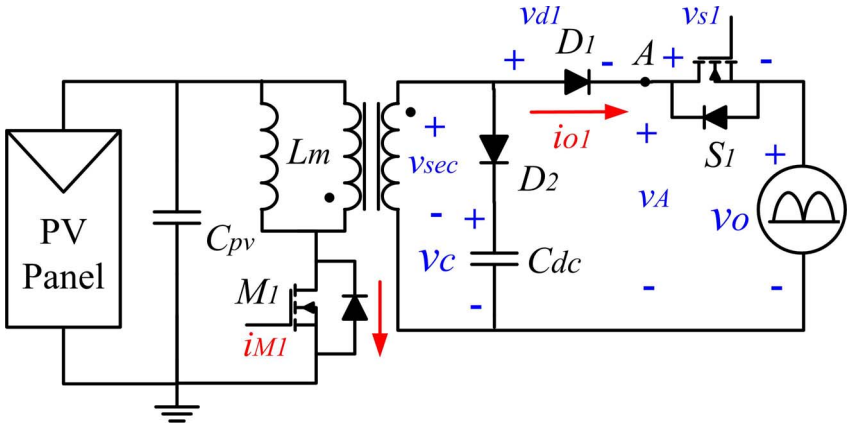


Fig.5.22: Measured Parameters of Flyback Converter in Experiment

A high frequency switching device (CoolMOS SPW24N60C3) is used as S1 to get the waveforms in Fig.5.23. It is found that when M1 is turned off, although D1 and S1 are not supposed to turn on, a current spike still flows through them (the

second waveform from top). The third waveform is the voltage stress across D1 and S1, which transits from negative to positive as discussed above.

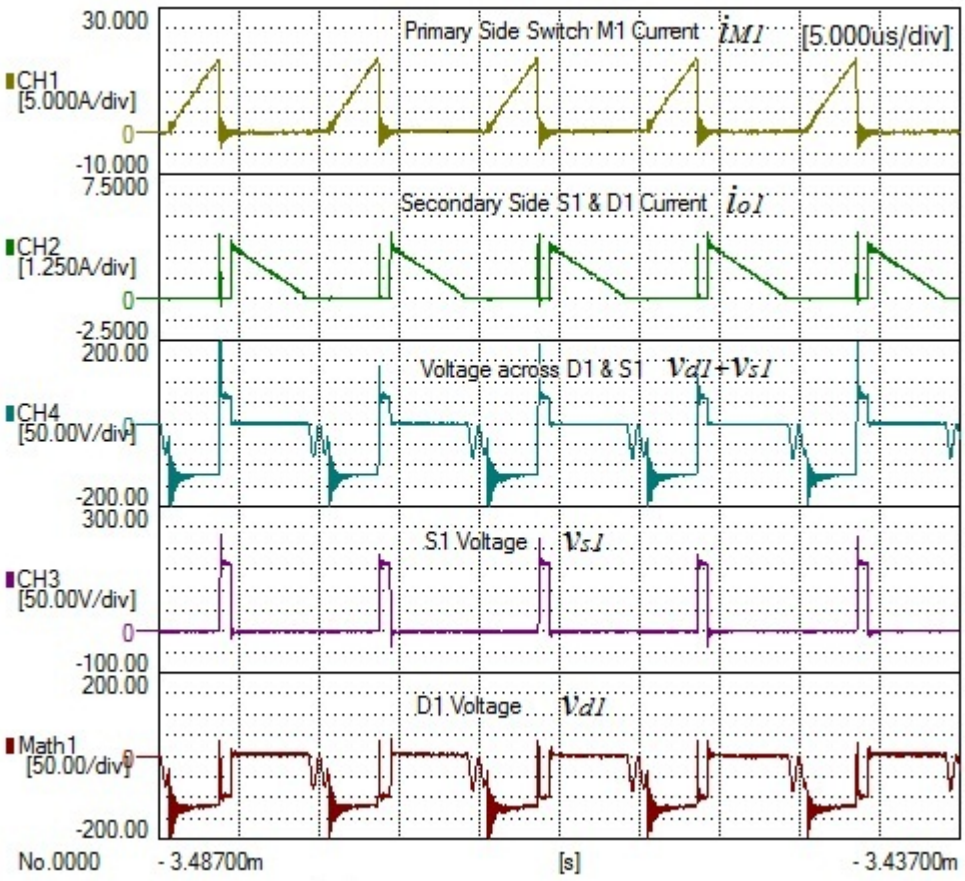


Fig.5.23: Operating waveforms: S1 uses Cool MOS SPW24N60C3 (Scheme B, Experiment, DC-DC Conversion)

An interesting phenomenon is observed in the waveforms of S1 voltage and D1 voltage in Fig.5.23. When M1 is on, D1 is reverse biased to block the negative voltage while S1 voltage is around zero. During the instant when M1 is turned off, it is found that D1 becomes forward-biased in a short interval and then keeps negative during the interval when D2 is conducting. At the same time, S1 is under a higher positive voltage stress than desired value of $v_C - v_o$. This phenomenon can be explained by considering the effective output capacitance of S1 (1060pF for

SPW24N60C3). When voltage across S1 and D1 changes abruptly from negative to positive, a current spike flows through S1 and D1 to charge S1 output capacitor to a higher voltage than $v_C - v_o$. As a result, D1 is forced to be reverse biased and also blocking the path for the discharge current of S1 output capacitor. This current spike was found to cause an error in current sensing and in turn to affect the current tracking performance severely. It should therefore be eliminated.

Based on the above analysis, in order to prevent the current spike during turning off of M1, a switch with a low effective output capacitance should be used. Therefore, an IGBT FGP5N60LS with effective output capacitance of 39pF is used to replace the CoolMOS and the waveforms are shown in Fig.5.24.

Fig.5.24 shows the waveforms of the primary side switch M1 current, diode D1 & switch S1 current, the transformer secondary side voltage v_{sec} and the voltage at node A v_A and the voltage across D1 ($= v_{\text{sec}} - v_A$). It is noticed that the current spike in D1 & S1 current when M1 is turned off is greatly reduced. Besides, when M1 is turned off, D1 voltage becomes zero and S1 voltage (which can be derived from voltage at node A) becomes $v_C - v_o$ as desired.

In addition, the reduction of current spike also requires a diode D1 with a low capacitive charge, which would reduce the discharge current during the abrupt voltage change. In this design, a SiC diode with a total capacitive charge of 8nC was finally used, which provides a fairly good performance as shown in Fig.5.24.

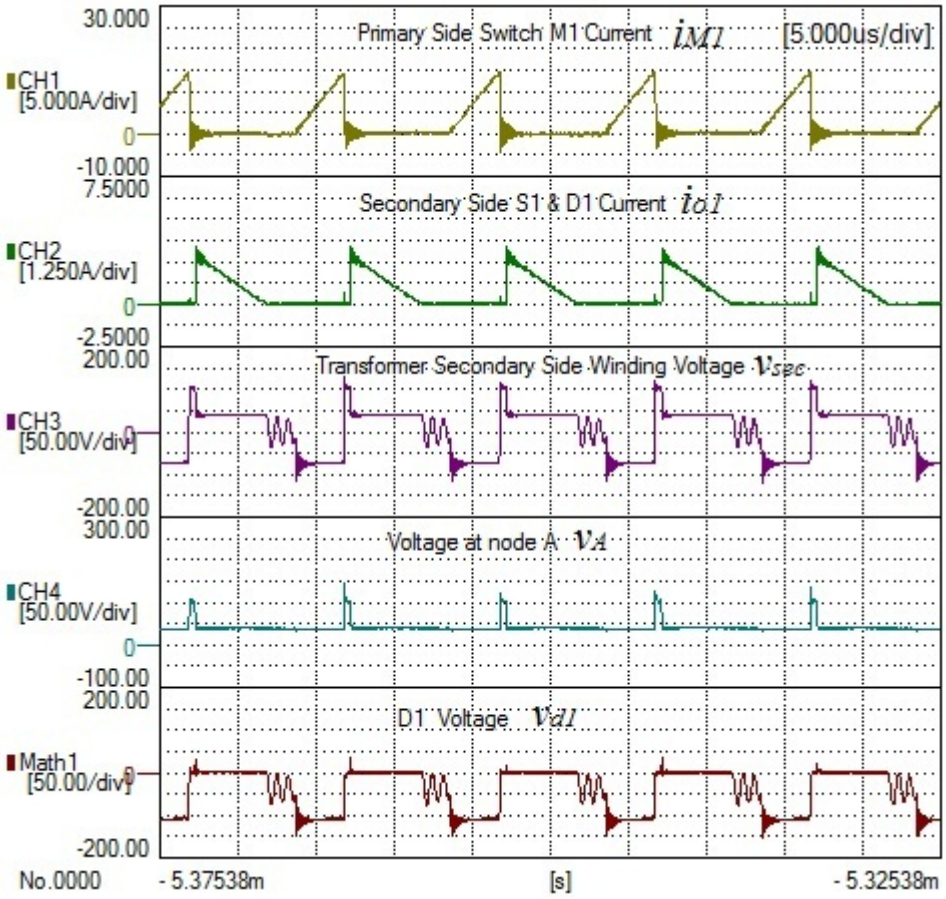


Fig.5.24: Operating waveforms: S1 uses IGBT FGP5N60LS (Scheme B, Experiment, DC-DC conversion)

5.5.3. Buck Converter Operation –DC-DC Conversion

Typical experimental waveforms of the auxiliary buck converter in DCM are shown in Fig.5.25 in DC-DC conversion.

It is noticed that when S2 is turned off, the reverse voltage of D3 v_{d3} reduces to zero slowly. This is due to the nonlinear output capacitance of S2, which is greatly higher under a low voltage stress. This is less important in our case where a high input voltage around 400V is normal operation.

However, it is worth to mention that the resonance current in the buck inductor

current i_{oa} as shown in Fig.5.25 when both S2 and D3 are off DC/AC operation were found to be the main reason for some distortion in the output current waveform. This distortion is intrinsic in DCM operation, which could be eliminated by operating the buck converter in CCM operation.

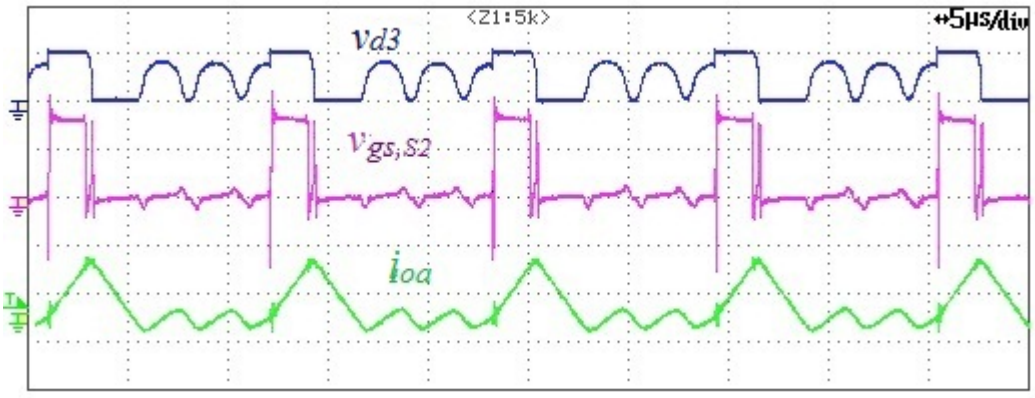
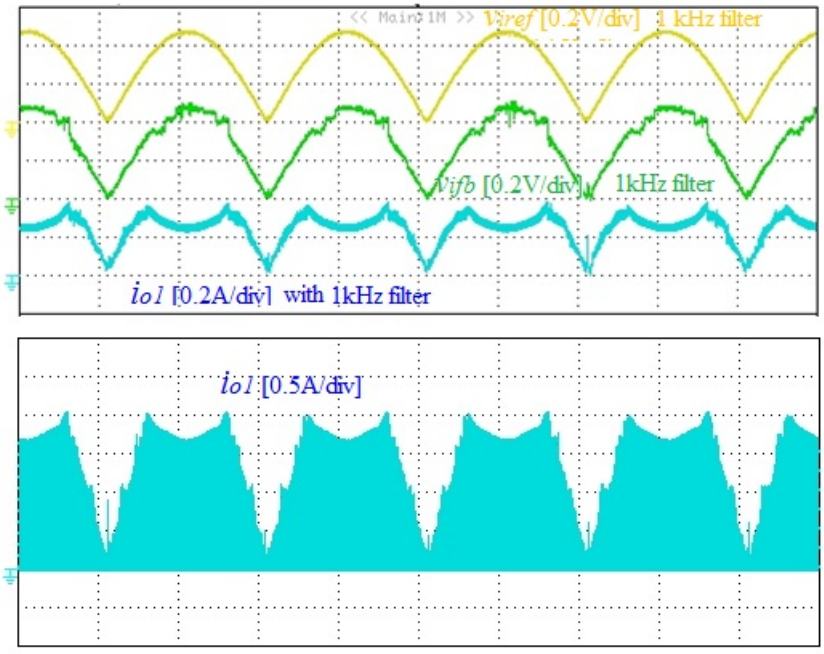


Fig.5.25: Buck Converter Operating Waveforms ($V_{ds,S2}$ [100V/div], $V_{gs,S2}$ [10V/div], I_{oa} [0.2A/div], Experiment, DC-DC conversion)

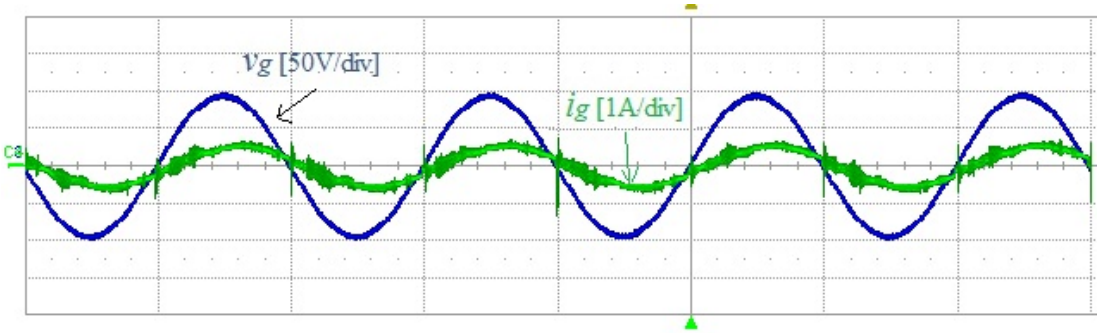
5.5.4. DC-AC Conversion

The designed prototype with output current controller designed in Chapter 6 are tested with a laboratory DC power supply to simulate PV module and an AC power supply PRC1000L in parallel with a 400Ω load resistor to simulate grid connection. The power decoupling capacitor voltage is kept constant by connecting a DC power supply and a 400Ω power resistor in parallel with the capacitor in this test.

One example of the steady state operation waveforms in DC-AC conversion is illustrated in Fig.5.26.



(a) Output current reference signal v_{iref}, feedback signal v_{ifb} and currents of D1/S1 i_{o1} (with or without 1kHz filter)



(b) Grid voltage and current waveforms

Fig.5.26: DC-AC conversion waveforms ($V_{pv} = 27V$, $V_{rms} = 67.5V$, $I_{rms} = 0.39A$, experiment)

Fig.5.26 (a) shows the measured steady state operating waveforms of the output current reference signal v_{iref}, output current feedback signal v_{ifb}, measured S1/D1's current i_{o1} with a filter of 1kHz and instantaneous S1/D1 current. It is shown that when the output current of flyback converter i_{o1} is controlled, it is able to follow the reference value closely. When the desired output power is larger than the input power from PV module, the output current i_{o1} of flyback converter is

saturated at a constant power level as shown in Fig.5.26 (a). This result agrees with earlier theoretic analysis and simulation results. It is also noted that the current feedback waveform during the interval of controlling the output current of buck converter is slightly distorted by staircase disturbance. This has been found to be due to the resonance current between buck inductor and S2/D3 capacitance when both S2 and D3 are off. But still, the feedback signal is tracking the reference signal over an AC cycle and the output grid voltage and current (at lower value) are shown in Fig.5.26 (b). Here, some current spikes during zero-crossing of an AC cycle have been noticed, which causes ringing at the filter resonance frequency. Overall, the output current is sinusoidal with a slight phase shift from the output voltage.

5.6 Conclusions

In this chapter, a parallel power processing scheme has been proposed for a microinverter with active power decoupling function. The basic idea is to achieve long system lifetime and high efficiency by: 1) sending 68% of power through one stage conversion directly to output and sending the rest decoupled power through two-stage conversion; 2) placing active power decoupling circuit at high voltage side.

A pilot topology based on flyback converter in DCM mode and a buck converter has also been identified with two possible switching sequences. The design of flyback converters in both switching schemes has been considered and analyzed. It was found that Scheme A has lower current stresses and lower RMS

current compared to Scheme B, which makes it potentially higher efficiency. However, the decision goes for Scheme B, in order to achieve control simplicity. The control aspects of the proposed pilot topology have been investigated and will be the focus of Chapter 6.

The operation of the proposed inverter has been verified by simulation compared to a flyback-DCM inverter without APD scheme at the power rating of 200W. The large capacitance required for passive power decoupling at PV side (in the range of mF) can be replaced by two capacitors with small capacitance (in the range of μF). The simulation results also verified the feasibility of the proposed topology with APD scheme.

A prototype of the designed pilot topology has been built in laboratory and the implementation issues in power circuits have been addressed in this Chapter and the DC-DC and DC-AC conversion of the proposed pilot topology have been verified by experiment.

The next chapter will focus on the control possibility of the proposed scheme and to design an effective current controller to provide output current shaping control and active power decoupling control.

CHAPTER 6: : A PARRALLEL POWER PROCESSING (P3) SCHEME– CONTROL AND VERIFICATION

6.1 Introduction

As discussed in Chapter 5, the proposed Parallel Power Processing (P3) scheme has two operating modes depending on whether input power is above or below the instantaneous output power. Besides, the dual-output flyback converter can operate in two different switching schemes, which provide control options to be explored.

Overall, the control of the system needs to fulfill three control purposes: 1) to ensure that the PV panel makes maximum power available to the inverter; 2) the average decoupling capacitor voltage is maintained at a predetermined value when the input power changes; 3) to ensure that the output current tracks the rectified sinusoidal voltage so that a low THD and near unity output power factor can be achieved.

In order to achieve these control purposes, this chapter is organized as given below. First of all, the small signal modeling of the proposed topology is discussed using state-space averaging method in Section 6.2. The focus is placed on the frequency response of the input voltage control for MPPT purposes and output current control for current tracking purpose. Following that, the proposed control scheme with emphasis on the dual loop current/voltage control and design is investigated in Section 6.3. The steady state and transient performance of the designed control

scheme have been verified. The results from both simulations and experiments are presented and discussed in Section 6.4.

6.2 Power Stage Modeling

The design of power stage circuit parameters have been discussed in Section 5.3. In this section, the control model of the power stage is developed so as to obtain insight into control possibilities.

As the dual-output flyback converter works in DCM all the time, the flyback transformer is completely demagnetized every switching cycle. Therefore, the input power from PV module is fully controlled by the main switch M_1 only. Modeling of the input stage for MPPT control purpose is described in Section 6.2.1. After that, the scheme models (both Schemes A and B) for output current shaping and control are derived with the state-space averaging method in Section 6.2.2. A discussion about the models and possible control options is included in Section 6.2.3.

Since all the variables are averaged over a switching cycle, unless otherwise mentioned, the Bode diagrams drawn in this section are only valid up to $1/10^{th}$ of the switching frequency.

6.2.1. Input Stage Model for MPPT Control

Among the various MPPT methods published [109, 110, 125, 126], P&O (Perturb & Observe) is still by far the most popular one used in industry based on its implementation simplicity and performance. This method is adopted here for the

proposed P3 scheme. A typical MPPT control diagram with PV voltage control is shown in Fig.6.1.

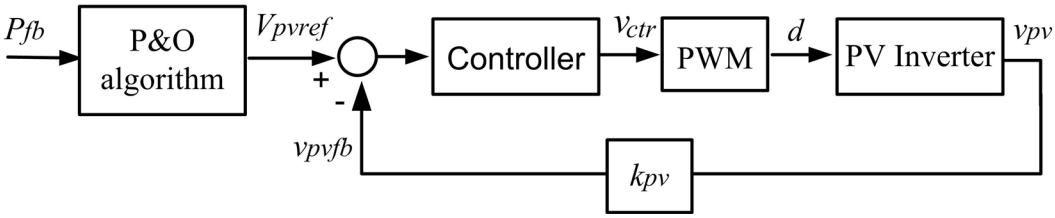


Fig.6.1: A typical MPPT control diagram with voltage control

The MPPT control diagram in Fig.6.1 consists of a P&O algorithm block to generate the perturbation variable (i.e. the reference value for PV module voltage) and a voltage control loop. A typical P&O flow chart for the proposed scheme is shown in Fig.6.2.

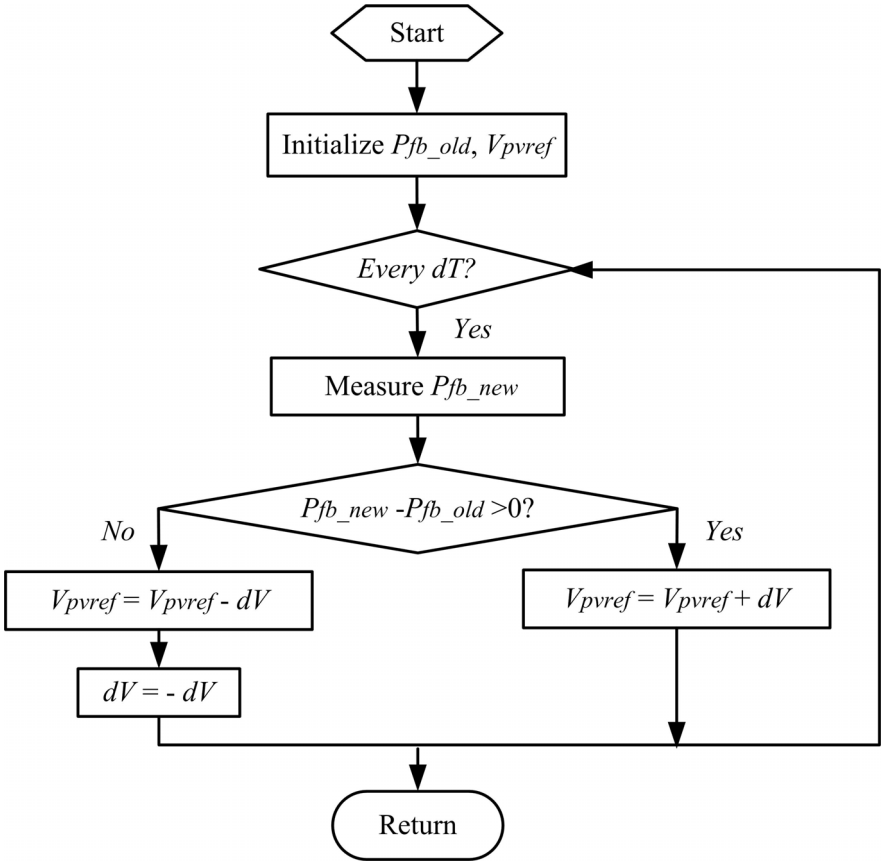


Fig.6.2: A typical P&O flow chart with PV module voltage as reference value

The P&O algorithm shown in Fig.6.2, works as follows.

At periodic intervals of dT, the PV module power, P_{fb_new}, is sensed and compared to the value, P_{fb_old}, previously measured in the last sampling instant. If the previous perturbation of the reference voltage has resulted in an increase in the PV power, the same direction of perturbation is being applied. Or else, the perturbation direction is changed.

The design of the MPPT control involves establishing the observed signal, P_{fb}, the perturbed signal (e.g. V_{pvref} in Fig.6.1), the P&O interval of dT and the step change of perturbation (e.g. dV in Fig.6.1). These will be carried out for the proposed scheme in this section.

6.2.1.1. Define Observed Signal

Firstly, as long as the flyback is ensured to work in DCM mode, the input power from PV module is uniquely determined by the duty cycle of M_1 at steady state operation.

$$P_{pv} = I_{pv}V_{pv} = \frac{1}{2}\frac{V_{pv}^2}{L_m}d^2T_s \tag{6-1}$$

Therefore, the observed signal to represent the PV module power can be given by:

$$P_{fb} = k_1 dV_{pv} \tag{6-2}$$

which is represented by the product of V_{pv} and d, eliminating the need to sense input current.

Or alternatively, it can also be represented by the pulse peak current of M_1 according to (5-41),

$$I_{M_1,p} = \frac{V_{pv}}{L_m} dT_s = \sqrt{\frac{2T_s}{L_m} \cdot P_{pv}} \tag{5-41}$$

However, it requires instantaneous current sense at the interval when M_1 is turned off, which is more complex to implement.

6.2.1.2. Define Perturbed Signal

For the control diagram in Fig.6.1, three variables can be used as the perturbed signal to be controlled, i.e. the PV module voltage, the PV module current and the input resistance of PV inverter.

Normally, PV module voltage is the preferred control variable compared to PV module current for several reasons. First of all, the MPP current changes in proportion to the irradiation level over a wide range, while the MPP voltage varies within a relatively small range, mainly with module temperature [107] (with a small temperature coefficient of the open circuit voltage such as -0.123V/^{o}C for KC200GT). Secondly, the temperature of a PV panel will only change slowly due to the large thermal time constants involved. However, changes in irradiance can occur suddenly, e.g. caused by passing clouds [22].

For the proposed pilot topology, the input of the flyback converter in DCM works as an effective resistor which is suitable for MPPT tracking in PV application. This input resistance can be given by;

$$R_{in} = \frac{V_{pv}}{I_{M1}} = \frac{2L_m}{d^2 T_s} \tag{6-3}$$

which is solely determined by the duty cycle of M_1, regardless of the output voltage and current conditions. When PV module works in MPP, this resistance should be equal to the characteristic resistance of PV module as given by (1-2):

$$R_{mp} = \frac{V_{mp}}{I_{mp}}. \tag{1-2}$$

However, the value of R_{mp} is subject to a relatively large variation and requires a fast dynamics. Therefore, in the next part, the dynamic response of the proposed system for MPPT with PV module voltage control will be studied.

6.2.1.3. Frequency Response for MPPT Control

Determination of the perturbation interval dT and step change value dV involves a trade-off between MPPT static and dynamic performances. On the one hand, a small perturbation interval and a larger step change value would lead to fast tracking speed, but result in larger power loss at steady state. On the other hand, a large perturbation interval and a smaller step change would have less power loss at steady state but will be much slower in tracking the MPP of PV module when the

operating condition changes. This aspect has been well discussed [109, 110] and is not included in this work.

Besides, the maximum achievable perturbation interval is also relevant to the dynamics of the control loop in Fig.6.1, which will be studied for the proposed topology below.

In this study, it is assumed that a preset MPP has been already reached before variation of the power level occurs. The PV module is modeled as a voltage source in series with an incremental resistance, whose value is equal to the characteristics resistance. The equivalent circuit diagram of the proposed topology at the PV side is illustrated in Fig.6.3,

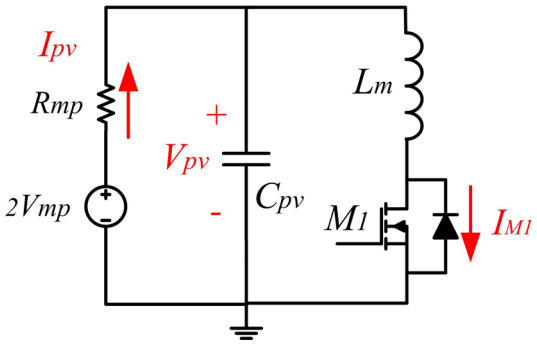
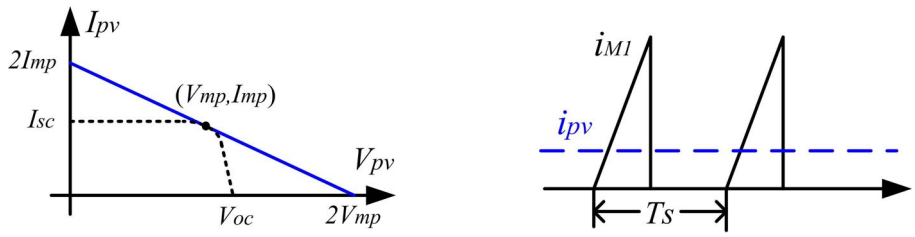


Fig.6.3: Equivalent circuit diagram of the input stage (The secondary side power transfer parts are not shown)



(a) Linear approximation of PV module characteristics (b) Current waveform

Fig.6.4: PV module model and input operation waveforms

The model is generated by linearizing the PV module's current-voltage (*IV*) curve around the MPP as shown in Fig.6.4(a).

$$I_{pv} = 2I_{mp} - \frac{I_{mp}}{V_{mp}} V_{pv} \tag{6-4}$$

The state-space averaging method is used to derive the following equations.

$$C_{pv} \frac{dV_{pv}}{dt} = I_{pv} - I_{M1} \tag{6-5}$$

$$I_{M1} = \frac{V_{pv}}{2L_m} D^2 T_s \tag{6-6}$$

The averaged small-signal model can be derived by substituting $V_{pv} = V_{mp} + \tilde{v}_{pv}$, $d = D + \tilde{d}$ and equations (3-7), (6-6) into (6-5).

The transfer function of the duty cycle to PV module voltage around the MPPT points can be obtained as:

$$G_{dv} = \frac{\tilde{v}_{pv}}{\tilde{d}} = -V_{mp} \sqrt{\frac{V_{mp}}{I_{mp}} \cdot \frac{T_s}{2L_m}} \cdot \frac{1}{1 + sC_{pv}R_{mp}/2} \tag{6-7}$$

Equation (6-7) reveals a single-pole response, where the DC gain depends on the operating conditions such as the PV module voltage and current, and is not dependent on the PV side capacitance value. The pole position, on the other hand, is determined by the PV side capacitance and the incremental resistance of PV module at the MPP.

Based on the parameters shown in Table 6.1, the system frequency response can be illustrated by a Bode diagram, as shown in Fig.6.5.

Table 6.1: Circuit parameters at STC

Description	Value
PV side capacitance C_{pv}	20μF
Flyback magnetizing inductance L_m	4μH
PV module nominal MPP voltage V_{mp}	26.3V
PV module nominal MPP current I_{mp}	7.61A

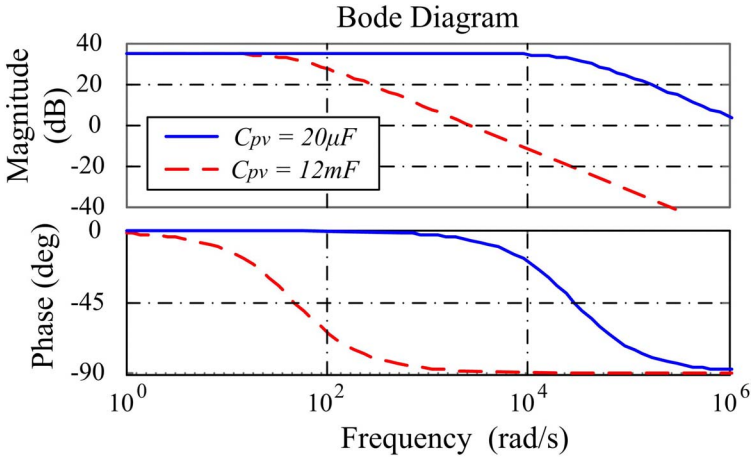


Fig.6.5: Bode diagram of flyback in DCM under nominal operating condition (Duty cycle to PV module voltage transfer function)

With the constant power transferred by the flyback converter, the filter capacitance (20μF) is needed only to filter the switching frequency component. As shown in Fig.6.5, because of this small PV side capacitance, the pole is at a high frequency of 4.6 kHz, which enables a faster close-loop response. On the other hand, as discussed earlier, when no APD scheme is used, the PV capacitance will be much larger (e.g.12 mF) (see Section 3.3) so as to handle the second harmonic power also. In this case, the pole is located at the significantly lower frequency of 7.68 Hz (48 rad/s in Fig. 6.5). Compared to the case without APD scheme, the small capacitance at PV side with APD scheme makes this topology suitable for fast MPPT implementation with a smaller perturbation interval, dT .

6.2.2. Pilot Topology Modeling

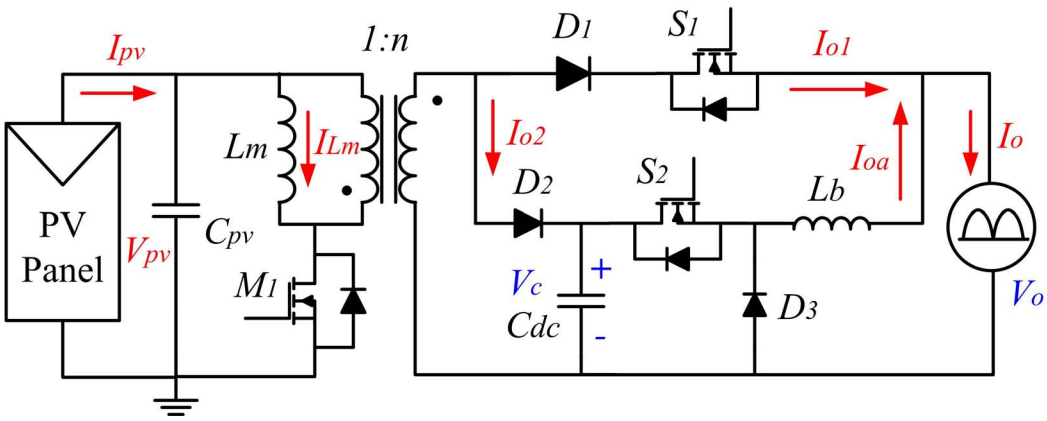


Fig.6.6: Circuit diagram of the P3 pilot topology

The pilot topology of the proposed P3 scheme is redrawn in Fig.6.6. It is assumed that a constant power is drawn from PV panel under a fixed irradiation and temperature and specific operating conditions. The output current shaping and power decoupling control are implemented at the secondary side of the pilot topology. The frequency responses of the dual-output flyback converter discussed in Section 5.3.2 under Scheme A and B operation as well as the buck converter will be studied in this section. The purpose is to investigate the potential control options and find a simple but effective control solution for the proposed topology.

As both converters are designed to work in DCM and the PV side operation is decoupled from the secondary side control, the system under study is a first order system with only one storage component C_{dc}.

As shown in Fig.6.6, the output grid side filter is ignored in the modeling and the UFI operation is taken care of through modeling the load as a rectified AC

voltage sink V_o. It is also assumed that the converter operation is ideal and that the power loss between the input and output is zero. As the switching frequency is much higher than then second harmonic frequency of the line waveform, it is reasonable to assume that the pilot topology works in quasi-steady state at every instant of the AC period in deriving the plant transfer functions.

6.2.2.1. Modeling of Switching Scheme A

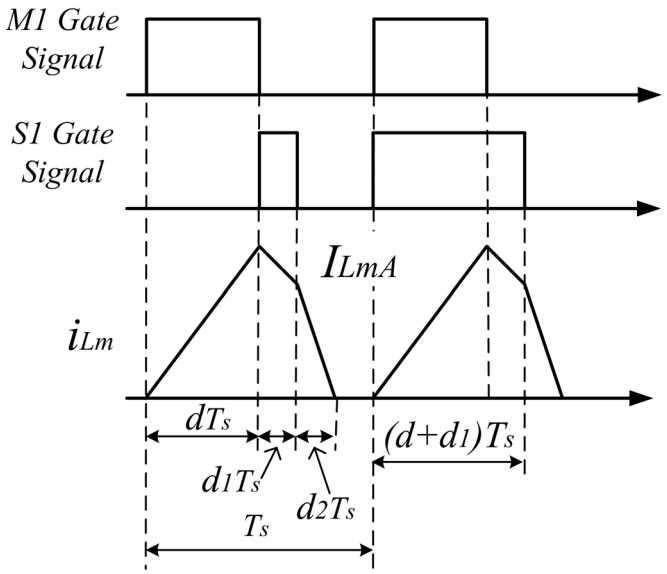


Fig.6.7: Illustration of Flyback converter waveforms in Scheme A

When the dual-output flyback converter works in Scheme A, the waveforms of the gate signals for M1 and S1 and the flyback transformer magnetizing current i_{Lm} are shown in Fig.6.7. In this figure, d_1 represents the duty cycle of D1 and S1, while d_2 represents the duty cycle of D2. During the interval when S1 is on, the slope of current in S1 is equal to i_{Lm}/n.

Therefore, the average current of S1 can be obtained from Fig.6.7:

$$I_{o1} = (\frac{I_{M1,p}}{n} - \frac{V_o}{2n^2 L_m} d_1 T_s) d_1 \tag{6-8}$$

The small signal modeling of the system can be obtained by applying a small signal perturbation on the duty cycle of d_1. Therefore, the transfer function of the control to output current is:

$$G_{id1} = \frac{\tilde{i}_{o1}}{\tilde{d}_1} = \frac{I_{M1,p}}{n} - \frac{V_o T_s}{n^2 L_m} \cdot d_1 = \sqrt{\frac{2T_s}{n^2 L_m} \cdot P_{pv} \cos(2\omega t)} \tag{6-9}$$

It is noticed that this transfer function is a simple gain, which is proportional to the square root of the decoupling power between input and output. With the design parameters $n = 4$, $L_m = 4\mu H$ (see Section 5.4 and Section 5.5) and the PV module parameters at nominal power in Table 5.2, the gain of power plant is drawn in Fig.6.8. The gain of the power plant is larger during zero crossing instants and reduces to zero when flyback converter changes from mode I into mode II.

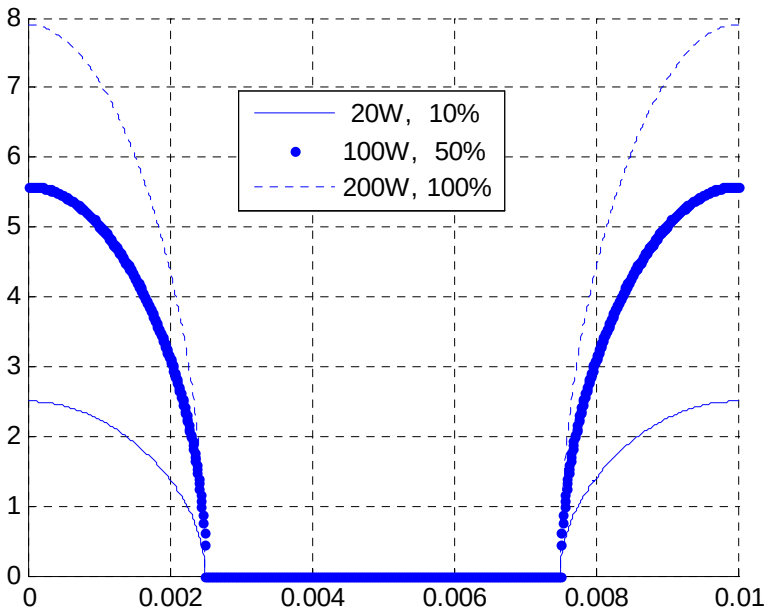


Fig.6.8: The transfer function of (6-9) over an AC cycle

6.2.2.2. Modeling of Switching Scheme B

The gate signal waveforms and the current waveform when the flyback converter works in Scheme B are shown in Fig.6.9.

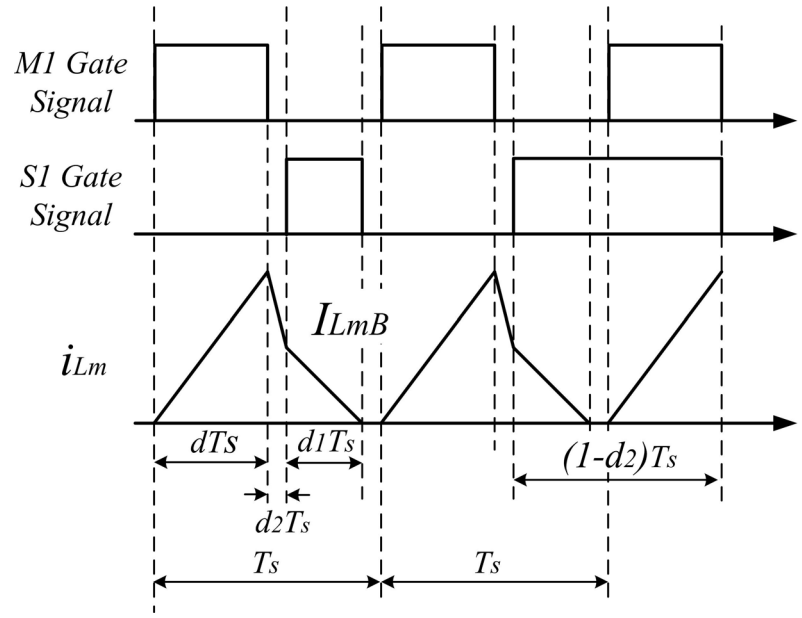


Fig.6.9: Illustration of Flyback converter waveforms in Scheme B

In this case, control of S1 current is mainly done by changing the duty cycle of D2, instead of the duty cycle of S1. The average current of S1 I_{o1} can be derived as a function of d_2, rather than d_1 based on the equations below:

$$I_{LmB} = I_{M1,p} - \frac{V_C}{n^2 L_m} \cdot d_2 \cdot T_s \tag{6-10}$$

$$I_{LmB} = \frac{V_o}{n^2 L_m} \cdot d_1 \cdot T_s \tag{6-11}$$

$$d_1 = \frac{n^2 L_m}{V_o \cdot T_s} \cdot I_{LmB} \tag{6-12}$$

$$I_{o1} = \frac{1}{2} \times I_{LmB} \times d_1 = \frac{1}{2} \cdot \frac{n^2 L_m}{V_o \cdot T_s} \cdot I_{LmB}^2 \tag{6-13}$$

where I_{LmB} is the magnetizing current at the interval when S1 is turned on; $I_{M1,p}$ is the cyclic peak current of M1, equivalent to the cyclic peak magnetizing current; d_1 and d_2 represent the duty cycle of D1/S1 and D2 respectively; n is flyback transformer turns ratio and L_m the magnetizing inductance.

Based on the quasi-steady state equations (6-10)~(6-13), the control-to-output current transfer function of flyback converter in Scheme B can be calculated as:

$$G_{id2} = \frac{\tilde{i}_{o1}}{\tilde{d}_2} = \frac{n^2 L_m}{V_o T_s} \cdot I_{LmB} \cdot \frac{\tilde{i}_{LmB}}{\tilde{d}_2} = -\frac{V_C}{V_{rms}} \sqrt{\frac{2P_{pv}T_s}{n^2 L_m}} \tag{6-14}$$

$$\text{where, } V_o = \sqrt{2}\left|V_{rms}\sin(\omega t)\right|,\ V_C = \sqrt{V_{C,dc}^2 + \frac{P_{pv}}{\omega C_{dc}}\sin(2\omega t)} \tag{6-15}$$

It is noticed that this transfer function is a simple gain with a negative value, which is proportional to the square root of the input DC power. With the design parameters of $n = 4$, $L_m = 4\mu H$ (see Section 5.4 and Section 5.5) and the PV module parameters at nominal power in Table 5.2, the negative gain of power plant over an AC cycle is drawn in Fig.6.10 together with the positive control-to-output transfer function of the buck converter. As shown in Fig.6.10, variation of the negative gain within one AC cycle is limited at a given power level. In addition, variation of the power plant at power levels between 10W to nominal power level of 200W is also limited to a negative value between -3 to -15 for the designed converter. This feature is useful in designing an effective linear controller for current tracking at different power levels.

6.2.2.3. Modeling of the Buck Converter

The buck converter is designed to operate also in DCM so as to provide a similar control-to-output current transfer function to that of a flyback converter. The derivation of the transfer function follows a similar procedure to that discussed above. Its transfer function also is a simple gain and can be shown to be:

$$G_{id3} = \frac{\tilde{i}_{oa}}{\tilde{d}_3} = \frac{1}{V_{rms}} \sqrt{V_c (V_c - V_o)} \cdot \sqrt{\frac{2 P_{pv} T_s}{L_b}} \tag{6-16}$$

This transfer function is a positive gain, similar to the case of flyback converter in Scheme A, which mainly varies with square root of PV module power. Its variation over an AC cycle at power level of 10W and 200W based on the topology design in Chapter 5 has been illustrated in Fig.6.10, where a positive gain variation between 0.5 and 4.5 is shown.

6.2.3. Model Discussion

In the proposed scheme, when $P_{pv} > P_g$, S1 is controlled and S2 is off and when $P_{pv} < P_g$, S2 is controlled and S1 is on all the time. In this way, current shaping is realized by controlling S1 or either S2 depending on the power flow condition. However, a smooth transition between control of S1 and S2 is critical for the design of the control scheme.

The plant transfer function G_{id1} (6-9) in Switching Scheme A is not favorable for the proposed topology. First of all, it is noticed that the gain of power plant has a

large variation over AC cycle, starting from zero during the transition between flyback operation and buck control as shown in Fig.6.8. This will inevitably cause reduction of close-loop gain during the transition intervals and lead to distortion in current shaping. Secondly, both G_{id1} for control of S1 and G_{id3} for control of S2 are positive, which means the duty cycle needs to be increased so as to increase the output current. Therefore, two individual control loops are required for the current shaping and the transition between controls of S1 and S2 can suffer from an integrator wind-up issue. The duty cycle of S1 has a varying upper limit, due to PV power, AC voltage variations as well as DCM operation. It proved to be quite difficult to provide a fixed upper limit for anti-windup. As a result, when flyback converter transits from mode I to mode II, increase of S1 duty cycle is not able to further increase the current any more. However, before the controller for buck converter starts to work, the flyback controller with integrator is still trying to integrate the error and increase the duty cycle of S1 in vain. As a result, when flyback converter changes back from mode II to mode I, there will be a long delay before the duty cycle of S1 reduces to the upper limit value of DCM operation. This will result in a large distortion in the transition periods. These problems were faced when attempting to use Switching Scheme A in simulation.

The plant transfer function G_{id2} in switching scheme B is quite the opposite and is much preferred for a simple linear control of the proposed topology. Firstly, although varying over different power level, the variation of G_{id2} over AC cycle is

relatively small. Secondly, the negative response of G_{id2} does not have the anti-windup issue discussed above. The current shaping plant transfer function of the proposed scheme for an AC cycle at different power levels is illustrated in Fig.6.10.

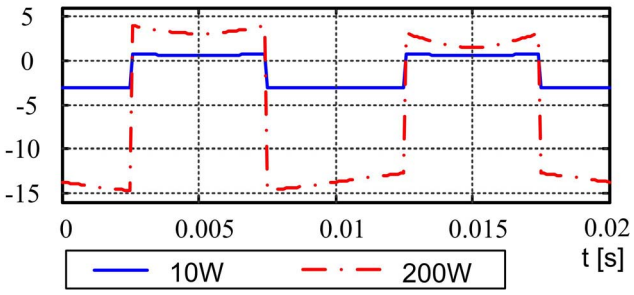


Fig.6.10: Current Transfer Function over an AC cycle (actual gain)

As shown in Fig.6.10, (6-14) to (6-16), both transfer functions are constant within a range, but with different polarity. Flyback converter transfer function is negative, ranging from -3 to -15, while the buck converter transfer function is positive, ranging from 0.5 to 4.5 for power level from 10W to 200W. As a result, the transition between G_{id2} and G_{id3} occurs at zero, regardless of its power level. This nature makes it possible to share a common current controller for two converters, which is discussed in Section 6.3.2.

Therefore, in this work, the scheme B is selected for easy of control. This is inspite of the fact that switching scheme A is preferable from current stress point of view as discussed in Section 5.3.2. Besides, design of a single current controller needs to consider variation of the control-to-output current transfer functions for both converters, with an absolute value between a min. gain of 0.5 and a max. gain of 15. This variation corresponds to operation power level between 10W to 200W.

6.3 Proposed Control Scheme

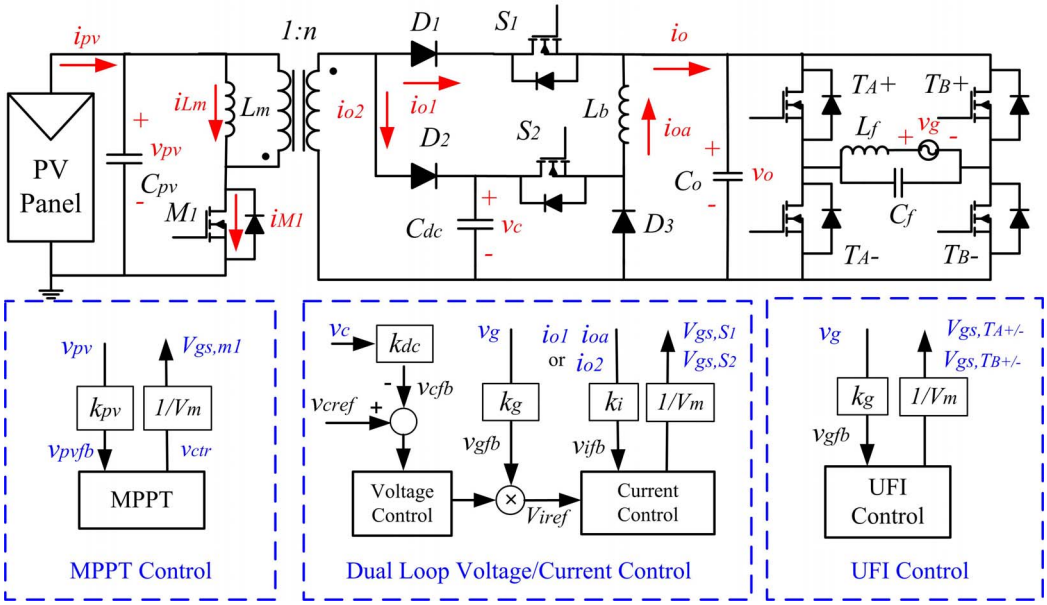


Fig.6.11: Overall Control System for the P3 Pilot Topology

The overall control system for the proposed P3 pilot topology is illustrated in Fig.6.11. Here, three independent control functions are included, i.e. MPPT control, a dual loop voltage/current control and UFI control.

The first block is the MPPT control. As discussed in Section 6.2.1, the flyback converter in DCM operation makes the input power from PV module solely determined by the duty cycle of the main switch M1. This feature decouples the MPPT control from the other control actions at the flyback secondary side.

The second control block in Fig.6.11 is a dual loop voltage/current control, which is the main controller in charge of active power decoupling and output current shaping. In the outer voltage loop, the average value of decoupling capacitor voltage v_C is sensed by a scale factor of k_{dc}. The feedback signal v_{cfb} is then controlled by a slower voltage controller to track the predefined reference voltage. In the internal

current loop, the reference signal for the output current v_{iref} is generated by multiplying the output from the voltage controller and the sensed rectified grid voltage. However, the currents of the two converters are to be controlled separately by changing the duty cycle of S1 and S2, which adds to the control complexity. These control possibilities will be investigated in detail in the next section with a simple control method proposed and studied.

The third control block is to unfold the unidirectional shaped output current into alternating current by turning on T_{A+} and T_{B-} at positive half AC cycle and turning on T_{A-} and T_{B+} at negative half AC cycle. This block, again is independent from the previous two control blocks, which is easy to implement at a very low switching frequency i.e. 100Hz.

Overall, the major control challenge in the proposed scheme is in the second control block, which will be investigated in the next section.

6.3.1. A Dual Loop Voltage/Current Control

As discussed earlier, the major challenge in control of the proposed P3 pilot topology lies in the dual loop voltage/current control to achieve power decoupling and current shaping purposes. In this work, a simple dual loop control scheme is proposed and illustrated in Fig.6.12.

As shown in Fig.6.12, the slower voltage loop controls the DC link (i.e. the decoupling capacitor) voltage v_C to generate the magnitude of the output current.

This magnitude is multiplied by the scaled rectified sinusoidal grid voltage to be the reference signal v_{iref}. An internal current loop is used to control the output current to follow the reference signal.

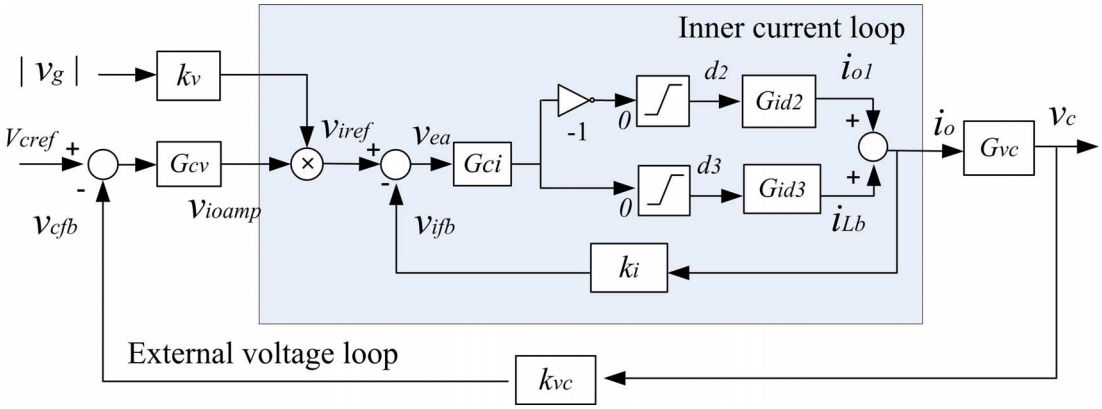


Fig.6.12: Control diagram for dual-loop control

However, in the proposed topology, the output current consists of two components from flyback converter and auxiliary buck converter, which makes current control more complex. In the proposed control diagram shown in Fig.6.12, this challenge is addressed by manipulating flyback converter switching scheme (using Scheme B discussed in Section 5.3.2) so as to use one simple average current controller for two plants. This aspect is presented in Section 6.3.2.

Further discussion follows the conventional design procedure for dual loop controller design, i.e. the current controller for inner current loop firstly (Section 6.3.2) and then the voltage controller for the external voltage loop (Section 6.3.3).

6.3.2. Current Control

As shown in Fig.6.12, a single current controller is proposed to control the net output current obtained by combining the output current of the top path of the

flyback converter (via S1 and D1) and the output current of the buck converter. This is based on the fact that the control of the top path of the flyback converter (via S1 and D1) and the buck converter do not occur at the same time. When the flyback converter output is controlled to perform output current shaping, the buck converter is not operating and the duty cycle d_3 is equal to zero. On the other hand, when the buck converter is actively controlled to shape the output current, the flyback converter top path is transferring full constant power with S1 on all the time. However, a smooth transition between control of flyback converter output and buck converter is critical for the output current shaping performance, especially at varying power levels for PV application.

In order to reduce the control complexity, the flyback output current is controlled by varying the conduction duty cycle of D2 rather than the duty cycle of D1/S1. In this way, one current controller can be used to control the output current of flyback and buck converters due to two reasons. Firstly, the transition between flyback converter and buck converter occurs when either the duty cycle of D2 or the duty cycle of S2 reduces to zero. This is extremely beneficial as the transition condition does not change with either the power level or AC voltage. The second reason is that the two plants to be controlled share similar transfer functions, which makes it possible to share the same current controller over an AC cycle. Following that, the current sensing scheme and corresponding transfer function are discussed in Section 6.3.2.1. An average current controller is designed in 6.3.2.2 following the

standard design procedure [114] considering the varying nature of the plant transfer functions at quasi-steady state.

6.3.2.1. Current Feedback Transfer Function

One current sensing resistor R_{cs} ($0.1\,\Omega$) is placed before the UFI, followed by an isolation amplifier AMC1200 with gain of $A_i = 8$ and minimum bandwidth of f_2 (=60 kHz). As the differential input voltage of the amplifier is limited to be less than 0.25V, the sensed high frequency pulsating voltage of R_{cs} needs to be averaged by an RC filter. The bandwidth f_1 of this analog filter is normally designed to be below 1/10th of the switching ripple in order to provide more than -20dB attenuation on the switching components. In our design, $f_1 = 5.56kHz$. Therefore, the current sensing factor k_i is calculated by:

$$k_i = R_{cs} \cdot A_i \cdot \frac{1}{1 + s/(2\pi f_2)} \cdot \frac{1}{1 + s/(2\pi f_1)} \tag{6-17}$$

Ignoring the sign of the gains in Fig.6.10, the plant transfer functions of flyback and buck converters including the current feedback factor have been illustrated in Fig.6.13. Here, the curve of “Buck min”, “Buck max”, “Flyback min” and “Flyback max” refer to the control-to-output current transfer function at a simple gain of 0.5, 4.5, 3 and 15 respectively as discussed in Section 6.2.3. In this case, design of the output current controller in the next section needs to consider the maximum gain of 15 and the minimum gain of 0.5.

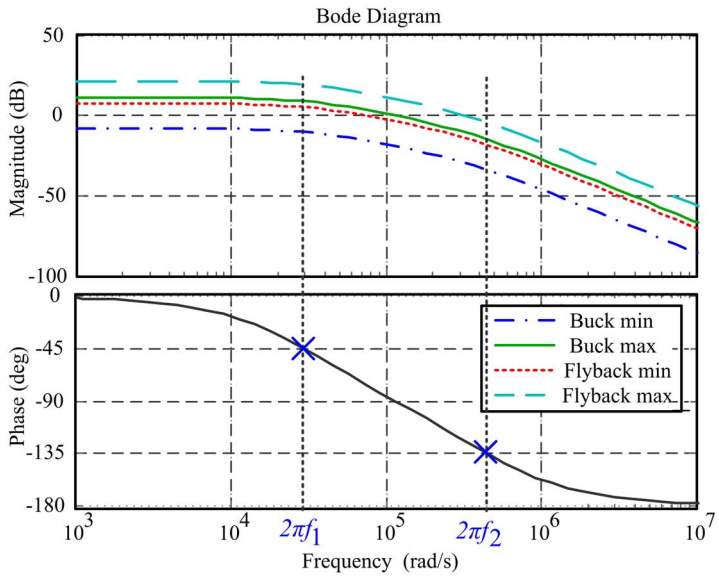


Fig.6.13: Plant transfer functions including current sensing circuit

6.3.2.2. Current Controller Design

Design of the current controller should make sure the open loop transfer functions fulfill the following conditions: 1) Enough gain at 100 Hz; 2) Good attenuation at the switching frequency. 3) A slope of -20dB/decade is preferred at crossover frequency to ensure enough phase margin.

A simple PI controller has been designed below to meet the above conditions.

$$C_i = \frac{7780}{s} + 0.1167 \tag{6-18}$$

The system open-loop and close-loop Bode diagrams are shown in Fig.6.14 for the minimum plant gain of 0.5 and shown in Fig.6.15 for the maximum plant gain of 15 . As shown in Fig.6.14 and Fig.6.15, the close loop system bandwidth ranges from 0.5 kHz to 10 kHz when the plant transfer function varies from 0.5 to 15.

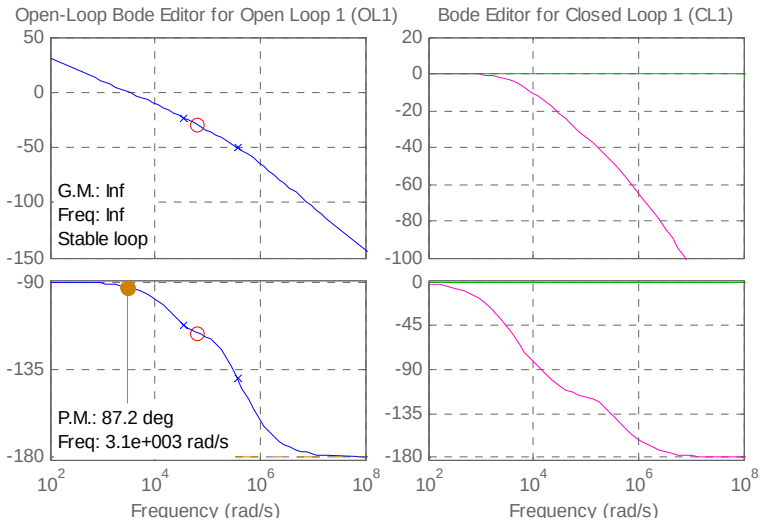


Fig.6.14: Bode diagrams of the designed controller (for the minimum gain of 0.5)

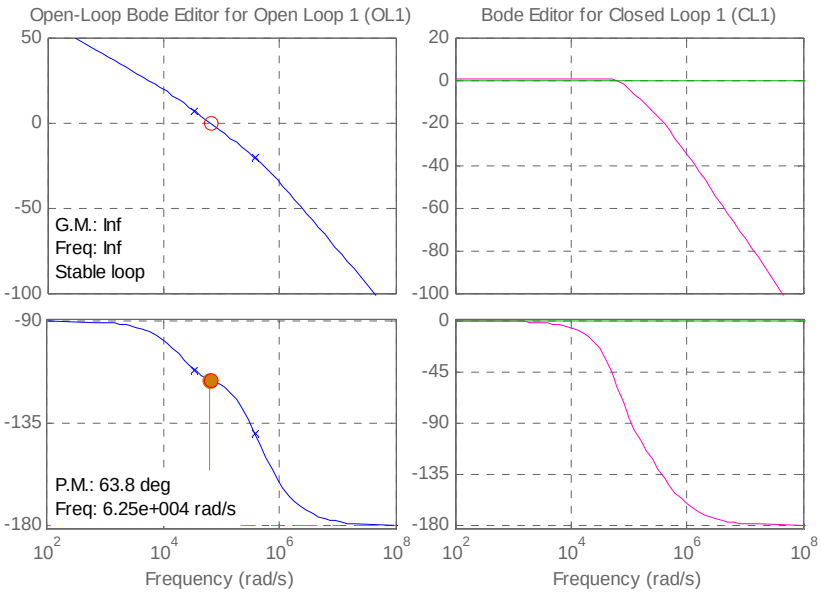


Fig.6.15: Bode diagrams and step response of the designed controller (for the maximum gain of 15)

6.3.3. Voltage Control

Design of the voltage controller in an external control loop around an existing current loop requires a suitable model of the internal current loop, taking into account static gain and dynamic response. This corresponds to a close-loop transfer function G_{io}, which is commonly in the form of:

$$G_{io}(s) = \frac{\tilde{i}_o}{\tilde{v}_{iref}} = \frac{A_o}{1 + s/\omega_{bw}} \tag{6-19}$$

where A_o represents the scale factor of output current versus current reference signal, which is assumed to be one. Here, $\omega_{bw} = 2\pi f_{bw}$, where f_{bw} is the bandwidth of the close loop system, i.e. 0.5~10kHz at nominal operating conditions.

However, as discussed above, this close-loop transfer function varies in terms of power level and AC cycle. Since the voltage loop is a slow loop which is expected to be much less than the current loop tracking speed as so to prevent output current distortion. An equivalent close-loop transfer function $G_{io.eq}$ is used to represent the tracking dynamics over an AC cycle as shown in Fig.6.16, which can be estimated as:

$$G_{io\_eq}(s) = \frac{1}{1 + s/(2\pi f_{bw\_eq})} \tag{6-20}$$

where $f_{bw\_eq} = 0.5kHz$ (considering the worst condition)

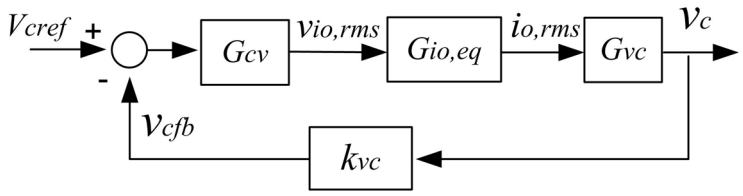


Fig.6.16: Block diagram of the external voltage loop

Therefore, the block diagram for the external voltage control is illustrated in Fig.6.16, where G_{vc} represents the current-to- voltage transfer function of the P3 pilot topology, k_{vc} is the voltage sensing scale which is assumed to be 1 here and G_{cv} is the voltage controller to be designed.

The plant transfer function for the output current versus decoupling capacitor voltage is given by:

$$G_{vc} = \frac{\widetilde{v}_C}{\widetilde{i}_{orms}} = -\frac{V_{rms}}{sC_{dc}V_{C,dc}} \tag{6-21}$$

where $V_{C,dc}$ represents the average voltage of the power decoupling capacitor. Design of the voltage controller follows a typical design procedure. For the system designed in Chapter 5, the voltage controller is designed to be:

$$C_v = \frac{0.004(s/2+1)}{s(s/628+1)} \tag{6-22}$$

The phase margin of the open loop system is 82.8 degree and the bandwidth is 57.2 rad/sec, which is purposely designed to be less than $1/10^{th}$ of $2\pi \cdot 100$ rad/sec in order not to influence the THD of the grid current.

6.4 Results and Analysis

The designed control system discussed above has been verified by simulation using PLECS/SIMULINK and by experiment with prototype.

6.4.1. Simulation Verification

The output current tracking performance of the pilot topology at steady state operation using the designed current controller has been shown in Fig.6.17 and Fig.6.18.

The control signal, the reference output current and feedback current are shown in Fig.6.17. It is noticed that the control signal is positive when the flyback converter is under control. In this case, the output current tracks the reference current closely. When the control signal reduces to zero, the flyback converter works in constant power transfer mode, with all the input power transferred to output through S1/D1.

The control signal further reduces to negative, which starts to control S3 in buck converter to transfer power from power decoupling capacitor to output side. However, a steady state current error has been noticed in comparison of the reference current and actual current of the buck converter output current control. As a result, a slight current distortion has been noticed in the grid current waveform as shown in Fig.6.18. The simulated THD of the gird current is 3.88% at nominal power level of 200W, which satisfy the THD requirement for grid connection.

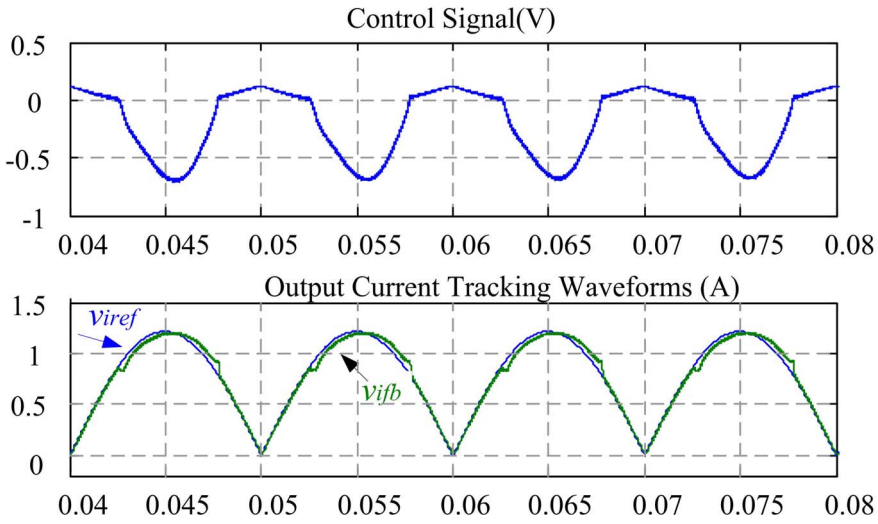


Fig.6.17: Steady State Control Signals ($V_{pv} = 27V$, $P_{pv} = 200W$, Simulation)

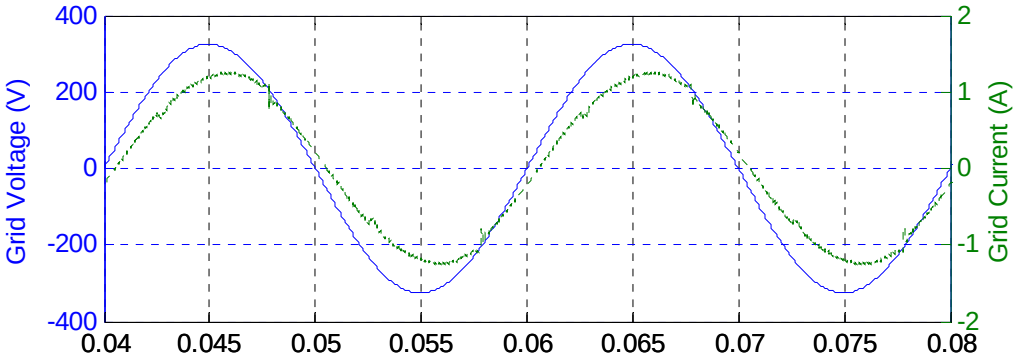


Fig.6.18: Steady State Output Waveforms ($V_{pv} = 27V$, $P_{pv} = 200W$, Simulation)

The transient response of the proposed external voltage controller has also been verified by simulation as shown in Fig.6.19 and Fig.6.20.

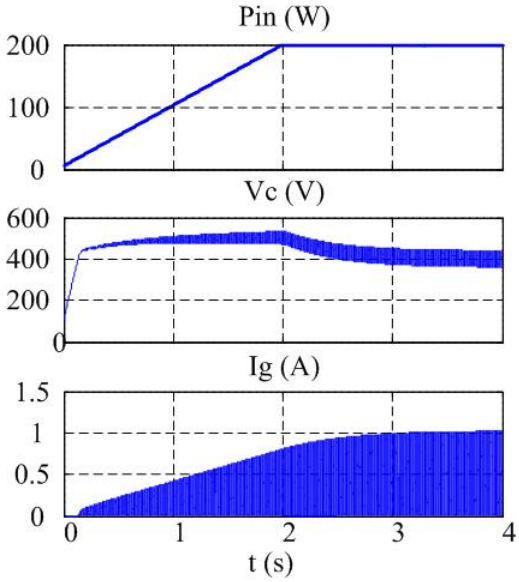


Fig.6.19: Start up waveforms of the P3 scheme with voltage control ($V_{pv} = 27V$, $P_{in} = P_{pv}$, Simulation)

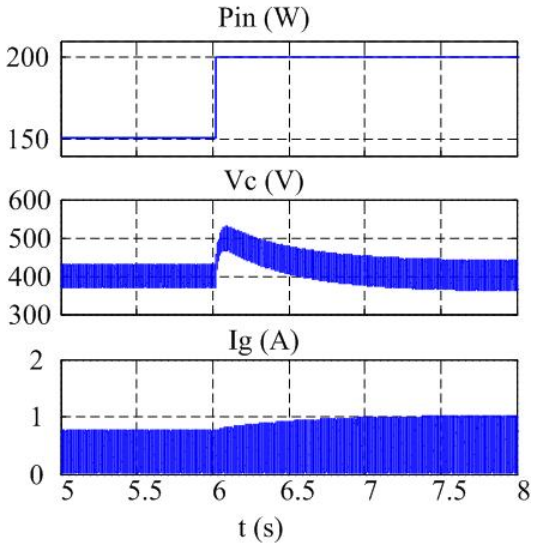


Fig.6.20: Transient waveforms of the P3 scheme with voltage control (Step change of 50W at input power, Simulation)

As shown in Fig.6.19, a soft start of the proposed pilot topology is applied in simulation so as to prevent an overshoot of the power decoupling capacitor voltage.

This soft start is implemented by limiting the input power to linearly increase rather than in a step manner.

As shown in Fig.6.20, when a step change of 50W is applied to the input power of the pilot topology, the voltage controller is able to maintain the power decoupling capacitor voltage at desired 400V.

6.4.2. Experimental Results

Since one current controller is used to control two converters based on the polarity of control signal as shown in Fig.6.7, it is implemented using operational amplifier CA3140 with dual power supplies. Fast comparators AD790 are used to generate the PWM signal from the control signal. As the magnitude of the RAMP signal is 3V, the designed PI controller given by (6-18) is implemented by: $R_s = 6.2k\Omega$, $R_f = 2.2k\Omega$ and $C_f = 6800pF$ as shown in Fig.6.21.

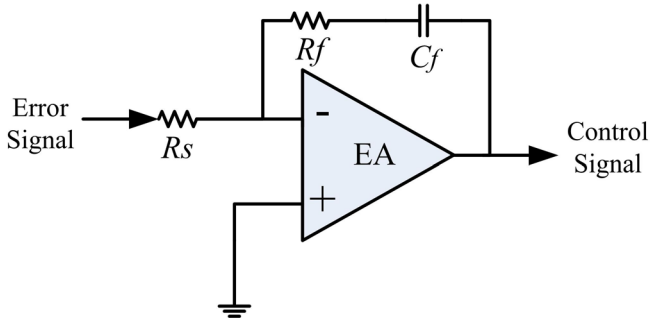


Fig.6.21: Current controller implementation

Close loop control of the output current using the simple PI controller has been tested under different operating conditions. For examples, the flyback converter is tested alone for output current shaping purpose even at low power level and the waveforms are shown in Fig.6.22. It is noticed that the feedback signal tracks the

reference signal for a wide range of AC cycle and the feedback signal follows the actual output current sensed by current probe as well. The control signal is positive in the whole AC cycle as only flyback converter is working.

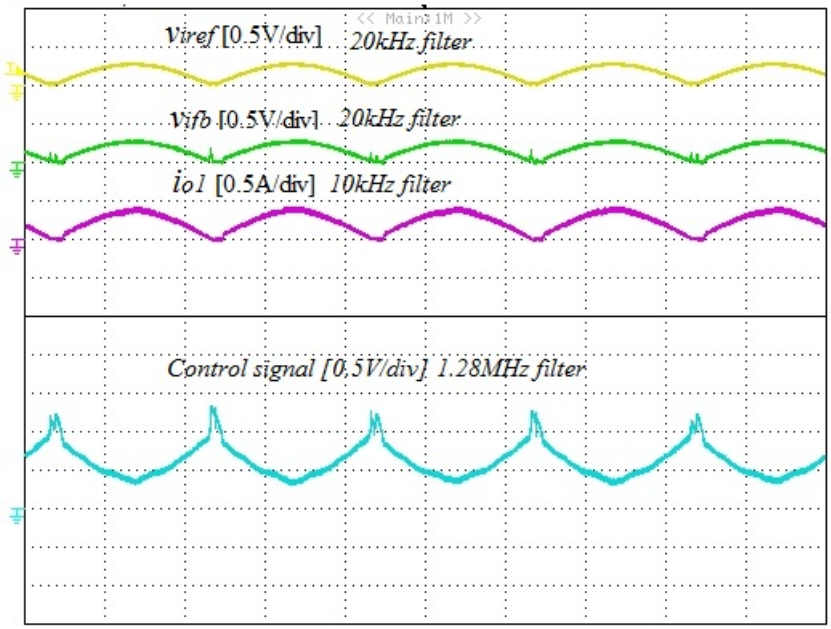


Fig.6.22: Current tracking waveforms with flyback operation only ($V_{pv} = 27V$, $V_{rms} = 50V$, experiment)

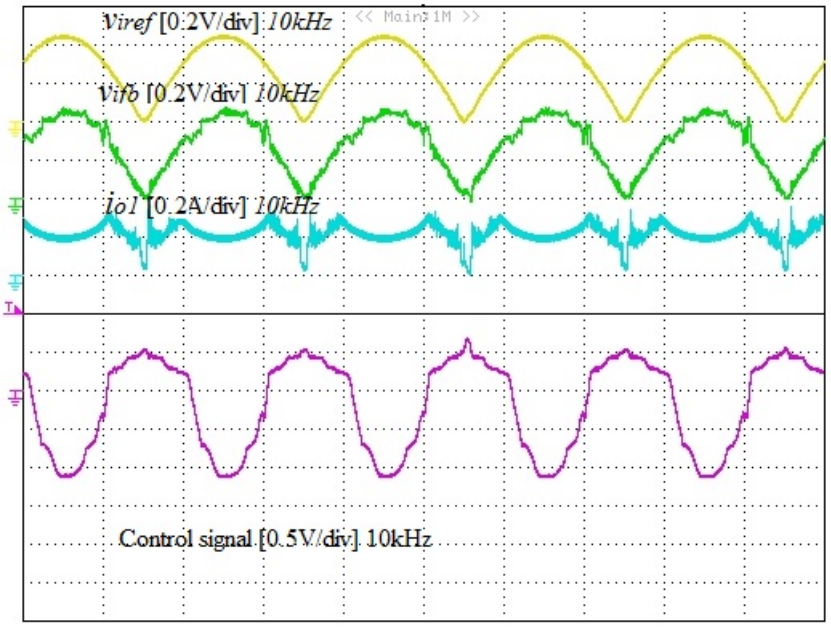


Fig.6.23: Current tracking waveforms ($V_{pv} = 27V$, $V_{rms} = 100V$, experiment)

When the buck converter works alternatively with the flyback converter to control the output current, the current tracking waveforms are shown in Fig.6.23. Firstly, the transition between the flyback control and buck converter control occurs at zero, which is similar to the simulation result in Fig.6.17.

Generally, the overall feedback signal follows the reference signal with some staircase distortion noticed in the output current feedback signal during buck operation. This aspect is due to DCM operation of the buck converter and could be considered for further improvement in future.

Small distortions at zero-crossing points are also observed in flyback converter output current, feedback current signals and control signals. This is most likely caused by jumping of the controller signal between an upper limit and the actual value corresponding to zero duty cycle for S1, which can be eliminated when working at higher power levels as noticed in experiment.

The grid voltage and current waveforms at different operating conditions are also shown in Fig.6.24 and Fig.6.25. It is observed ringing at the resonance frequency of the output filter makes the current waveform bold. But generally the output current follows the sinusoidal grid voltage with a phase shift due to the output filter.

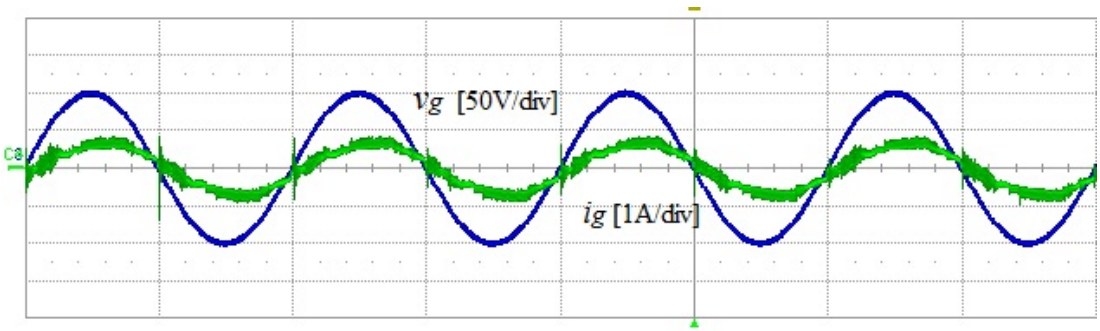


Fig.6.24: Grid voltage and current waveforms ($V_{pv} = 27V$, $V_{rms} = 71V$, $I_{rms} = 0.5A$, experiment)

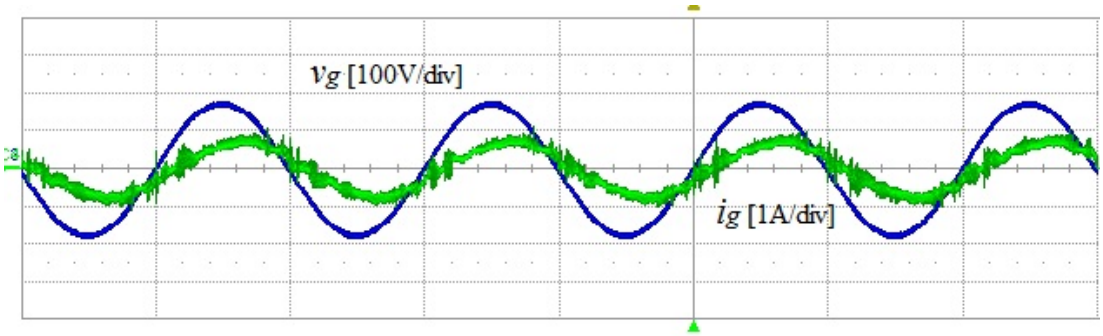


Fig.6.25: Grid voltage and current waveforms ($V_{pv} = 27V$, $V_{rms} = 124.6V$, $I_{rms} = 0.53A$, experiment)

6.5 Conclusions

The control aspect for the pilot topology using the P3 scheme has been investigated in this Chapter. The frequency response of the proposed topology for input voltage control has been carried out. This model will be useful in evaluating the MPPT searching algorithm used. In order to explore the control possibilities for effective output current shaping, small signal modeling of the dual-output flyback converter in Switching Scheme A and B have been carried out to derive the control-to-output current transfer functions. Similarly the control-to-output current transfer function of the buck converter has also been derived. Considering the control simplicity and smooth transition of current shaping control between flyback and buck converter, Switching Scheme B has been selected. Design procedure of one current controller for both converters has been presented first and followed by design of external voltage loop for control of power decoupling capacitor voltage. The steady state operation and dynamic response using the designed dual loop voltage/current control scheme have been verified by simulations. The proposed current control

scheme has been tested with prototype and the experimental results show an overall good tracking behavior.

The proposed scheme has the advantages of non-utilization of short life electrolytic capacitor, and avoidance of excessive additional power processing to accommodate the Active Power Decoupling feature and constant power transfer resulting in low component current stresses in the main DC/DC power converter handling the PV power.

CHAPTER 7: CONCLUSIONS AND FUTURE WORK

7.1 Summary of Conclusions

Though microinverter has become very popular in recent years in photovoltaic applications due to its several potential advantages, such as module level maximum power point tracking, removal of external high voltage DC link, various efforts are still taken to reduce the cost, improve the system efficiency as well as prolong the lifetime simultaneously.

The aim of this thesis was to investigate suitable topologies for the above three performance targets (cost, efficiency and lifetime) and to provide solutions to the problems associated with the proposed topology and its control. The problems identified and the key solutions proposed in this thesis fall under the following five categories:

1. For microinverters using a PV side capacitor for power decoupling, the commonly used capacitance calculation [1] to account for the MPPT requirement was found to be inadequate in accurately meeting the output current THD requirement also. This requirement is found to be more stringent than that imposed by the MPPT requirement and has been studied first time in this thesis.
2. A popular flyback inverter has normally been used as a potential low cost solution. This inverter typically was operated previously in DCM only.

Such a flyback-DCM inverter is known to be more suitable for power levels below 100W due to efficiency considerations. In order to improve the inverter's efficiency at higher power levels, say even above 200W, without adding to the cost of the whole system, a flyback-CCM inverter was proposed and compared to a benchmark flyback-DCM inverter. The issues in the design of the flyback-CCM inverter has been studied and discussed. A weighted efficiency improvement of 8% has been verified by experimental prototype test at full power of 200W and at a high switching frequency of 100 kHz.

3. A major challenge which prevents usage of a flyback-CCM Inverter as a current source microinverter is the presence of an RHP zero in the control-to-output transfer function, which imposes a limit on the closed-loop bandwidth resulting in slow tracking response. In order to meet the output power quality requirement, an indirect output current control scheme, has been proposed and investigated. Two current controllers, i.e. Indirect One Cycle Control (IOCC) and Indirect Average Current Control (IACC), have been applied to implement the indirect output current control and their merits compared. The simple IACC scheme based on the commonly used Average Current Control method has been shown to be able to meet the output quality requirements and make the proposed flyback-CCM inverter a feasible solution for micoinverter.

4. With regard to the lifetime issue of microinverter, one common approach is to replace the bottleneck electrolytic capacitor with a long life film capacitor by using an active power decoupling circuit. However, this could compromise the efficiency. In order to eliminate the use of an remove electrolytic capacitor while maintaining a good efficiency, a parallel power decoupling scheme has been proposed. A pilot topology based on the scheme has also been identified. The topology operation has been verified through simulations. Also, it has been verified that a film capacitor with value of only 20μF is sufficient to provide the power decoupling for a 200W inverter.
5. The major control challenge in the proposed Parallel Power Processing (P3) scheme lies in the smooth transition between controls of the two parallel converters. By choosing the switching sequence of the dual-output flyback converter appropriately, a simple control scheme has been proposed and shown to be able to address this issue with one current controller for both converters through simulations and experiments.

The detailed conclusions are discussed in Secs. 7.2 and 7.3, while suggestions for future work in this area are provided in Sec. 7.4.

7.2 A Low Cost Flyback-CCM Inverter

The first proposed topology for PV microinverter application is based on flyback converter. It is targeted at a low cost and high efficiency solution for medium power levels around 200W.

7.2.1. Study of the Power Decoupling Capacitance at PV side

Both the benchmark flyback-DCM inverter and the proposed flyback-CCM inverter discussed in Chapter 3 require a large power decoupling capacitor at the PV side, which makes the use of an electrolytic capacitor necessary. The power decoupling capacitance per watt has been found to be determined by the PV module average voltage and maximum allowed voltage ripple. The maximum allowed voltage ripple at PV module has been studied in order 1) to ensure above 98% of maximum power of PV module can be extracted and 2) not to cause large output current distortion.

It has been found that the second requirement is stricter than the MPPT requirement, and is the determining factor in the calculation of the power decoupling capacitance. The study method and analysis has been presented in Section 3.3 and verification of the capacitance's influence to the output power factor has been carried out by simulation with a PV module model in Section 5.4.

7.2.2. Analysis and Design of a Flyback CCM Inverer

A flyback CCM inverter was proposed for this application in order to reduce the current stresses in the components and improve efficiency without increasing overall cost or system complexity. Quasi-steady state analyses of the flyback inverter under CCM and also the benchmark flyback-DCM inverter have been carried out in Chapter 3 to provide insight on the converter operation over an AC cycle and to derive the design equations and component stress for both schemes. The trade-offs in the design have been presented and discussed. Efforts have been taken to ensure a fair comparison between a pure DCM scheme and a combined DCM/CCM inverter scheme. These efforts include design of both inverters following the given design procedure and component selections under the same considerations.

7.2.3. Verification of Efficiency Improvement of a Flyback CCM Inverter compared to a flyback-DCM Inverter

The Flyback-CCM inverter is expected to have lower current stresses and higher efficiencies compared to a flyback converter in Discontinuous Conduction Mode (DCM) for a medium power level from 100~300W. Verification of the efficiency improvement of flyback-CCM inverter in DC-AC inversion (for low DC voltage below 40V) has been carried out in this work.

The prototypes for both flyback-DCM inverter and flyback-CCM inverter have been built for a 200W PV module at a switching frequency of 100 kHz. The test

waveforms and results confirm the theoretical predictions. As expected the flyback-CCM inverter operates with significantly lower current stresses. The European efficiency and CEC efficiency of the proposed flyback-CCM inverter have been verified to be 7% ~8% higher than the equivalent of the flyback-DCM inverter by experiment.

7.2.4. Output Current Shaping Control of Flyback-CCM Grid-Connected Inverter

Flyback converter in CCM with input current shaping requirement has found use in PFC (Power Factor Correction) circuits. However, when working as a grid-connected inverter, it is the output current, rather than the input current, that needs to be controlled. In this work, a first attempt was made to directly control the output current of flyback converter in CCM using One Cycle Control and Average Current Control respectively as shown in Appendix B. The control challenges for both controllers have been identified. The main issue was the difficulty in overcoming the limitations imposed by the non-minimum phase characteristic of the output current to duty cycle operation of a flyback-CCM inverter.

In order to solve the problems caused by such direct current control methods, an indirect current control scheme has been proposed in Chapter 4. The indirect output current control scheme was applied using both one cycle control (Indirect OCC) and average current control (Indirect ACC) methods.

The indirect OCC scheme was first studied (in Chapter 4) considering its capability for fast tracking within one switching cycle. However, this scheme was found to suffer from nonlinear dynamics due to its nonlinear features. Study of the nonlinear phenomena has also been carried out using discrete time cycle-by-cycle mapping method and the cause being identified as the transition between DCM and CCM operation. A solution has been proposed to limit the duty cycle variation between adjacent switching cycles. Though the problem is resolved and the Indirect OCC scheme is a viable control option for the flyback-CCM scheme, the fast transient response feature of OCC scheme is compromised due to the limiting of the allowed change in duty cycle in adjacent switching cycles. In addition, the implementation of this scheme would require a digital controller, which may add to the system complexity as OCC is usually implemented using simple analog circuitry.

Since a very large system bandwidth is not needed as proven by Indirect OCC scheme (with the addition of duty cycle change limit), a popular linear controller, viz., average current control (ACC) scheme, was applied next in Chapter 4. The control-to-input current transfer functions have been derived and analyzed with variations of PV power level and AC voltage. A few reference transfer functions have been defined to simplify the process of controller design. A controller design guideline has also been developed to ensure the system stability at varying reference transfer functions. The designed controller is implemented using operational amplifier and used to control the Flyback-CCM inverter designed in Chapter 3. The

effectiveness of the Indirect ACC scheme for output current tracking has been verified by experiments. The analysis, design and experimental results clearly show that the proposed Flyback-CCM inverter together with the proposed Indirect Average Current Control Scheme is a feasible, high efficiency, low cost solution for a microinverter application.

In order to achieve the desired current tracking performance, one implementation issue relates to the current sensing of the primary side current using a unidirectional CT circuit. A solution has been proposed based on a bidirectional CT circuit to get rid of the measurement error caused by reset behavior in unidirectional CT operation over an AC cycle. The effectiveness of the proposed scheme has been verified by experiment and discussed in Section 4.5.

7.3 A Parallel Power Processing Scheme

The second proposed scheme is targeted at a high efficiency microinverter with long lifetime (i.e. without usage of electrolytic capacitor) for medium power levels around 200W.

7.3.1. Proposed Parallel Power Processing (P3) Scheme

A parallel power processing scheme with active power decoupling circuit has been proposed in Chapter 5. It consists of two parallel power conversion paths from DC input to AC output.

The basic idea of the proposal is to achieve long system lifetime and high efficiency by: 1) sending 68% of power through one stage conversion directly to output and sending only the rest decoupled power through two-stage conversion; 2) placing active power decoupling circuit at high voltage side. In addition, a higher ripple voltage can be allowed across the DC link (decoupling) capacitor. These allow the use of non-electrolytic capacitor for power de-coupling purpose, thereby increasing the potential lifetime of the microinverter.

An additional advantage of the proposed scheme is that the main power converter now transfers constant DC power as against the fluctuating (DC plus second harmonic) power transferred by the normal scheme studied in Chapters 3 & 4. This reduces the peak component current stresses in the main power converter.

This scheme can be implemented with various different power converter options. One such option was studied through a Pilot Topology implementation.

7.3.2. A Pilot Topology for Implementing the P3 Scheme

A pilot topology has also been proposed to verify the effectiveness of P3 scheme based on a dual-output main flyback converter and an auxiliary buck converter for processing the decoupled power.

Studies into the design of the dual-output flyback converter and the buck converter have been conducted to ensure DCM operation in both of these converters at all times. DCM operation was chosen so as to simplify the control of the system

under different power level and AC voltage. Two switching schemes of the dual-output flyback converter have been studied, with Switching Scheme A preferred in terms of the component stress and power loss consideration. However, considering the control difficulty between transition of flyback-converter and buck converter, Switching Scheme B was selected and implemented both in simulation and in the experimental prototype. The implementation issues for the pilot topology have been discussed and addressed in Chapter 5. Detailed simulation results have been presented to verify the operation of the proposed system.

7.3.3. Proposal of a Control System for the Pilot Topology

The control aspect for the pilot topology has been investigated in Chapter 6.

In order to explore the control possibilities for effective output current shaping, small signal modeling of the dual-output flyback converter in Switching Scheme A and B has been carried out to derive the control-to-output current transfer functions. Similarly the control-to-output current transfer function of the buck converter has also been derived. The modelling also takes into account the mode of operation, which is dependent upon whether the PV input power is greater than the instantaneous AC output power or not. Considering the control simplicity and smooth transition of current shaping control between flyback and buck converter, Switching Scheme B has been selected. The proposed scheme uses one common current controller for both the operating modes. The design procedure for this single current controller has been presented first. This is then followed by the design of the external voltage loop for

control of the power decoupling capacitor voltage. The steady state operation and dynamic response using the designed dual loop voltage/current control scheme have been verified by simulation. The proposed current shaping control was implemented and the performance of the output current control has been verified experimentally.

The proposed P3 scheme and its pilot implementation based on a flyback converter and an auxiliary buck converter is a promising approach towards realizing a long life microinverter without compromising efficiency significantly.

7.4 Future Work

In each of the issues on microinverters investigated in the thesis, there are further avenues to explore. Some of the areas for further work are summarized here.

7.4.1. Power Loss Distribution Analysis and Efficiency Improvement of the Flyback-CCM Inverter

Although the efficiency improvement of the proposed flyback-CCM inverter has been verified compared to the benchmark flyback-DCM inverter in a fair way, the measured efficiency of 88% can be further improved by carrying out a power loss distribution analysis on the prototype. A theoretical power loss study of active and passive components in the proposed topology could be used to identify the lossiest components and further verified by the experimental measurement. In this way, it may be possible to further improve the efficiency by better implementation or by applying advanced efficiency improvement techniques discussed in Chapter 2. These

techniques include burst mode control at light load condition, interleaving of the multiple inverters, using soft switching technique or non-dissipative snubber circuit.

7.4.2. Solutions to dynamic response problem due to RHP zero in direct output current control of Flyback-CCM Inverter

As discussed in Chapter 3, the slow transient response of the flyback-CCM inverter in direct output current control was due to the combined DCM/CCM operation. As a result, the close-loop bandwidth limit due to the RHP zero in CCM operation makes the close-loop bandwidth much lower than desired twice line frequency in DCM operation.

Small signal dynamic response problem due to RHP zero in CCM operation can be mitigated by designing the magnetizing inductance to be lower. However, this can result in undesirable high current ripple, which was expected to be addressed by CCM inverter approach.

The possible avenue of future work to this problem is to employ an adaptive controller so that in DCM mode, a high gain controller is used to ensure current tracking and in CCM mode the gain is brought down so as to ensure stability. Some control techniques for a large variation of plant transfer functions can be considered, such as gain scheduled PI controller, adaptive (or learning based) controller. Implementation of these controllers using a digital approach can also be considered in

the future. With a digital controller, the indirect current control scheme with One Cycle Control approach can be reconsidered for use as well.

7.4.3. Identification and Solutions to bifurcation problem in IOCC Scheme

Although the proposed reduction method for the nonlinear dynamic behaviour has been verified by discrete time cycle-by-cycle mapping, the proposed solution compromises the dynamic response of One Cycle Control (OCC).

Bifurcation behavior [120, 127, 128] of power converters has been studied in DC-DC converters and Power Factor Correction circuits in order to discover the underlining reason for bifurcation and to identify the parameters range for normal operation. A similar systematic approach could be adopted for the flyback-CCM inverter with IOCC scheme and to identify the design parameters suitable for operation without bifurcation behaviour, if possible.

7.4.4. Complete Experimental Performance Verification of the P3 (Pilot Topology) Scheme

The main aim in the P3 study was to show the feasibility of the proposed P3 scheme to eliminate the need for using an electrolytic capacitor which has been achieved through simulation results. Experimental prototype work can be completed at full rated power and voltages to fully characterize the performance of the proposed scheme.

7.4.5. Explore other topologies under P3 Scheme

The proposed Parallel Power Processing (P3) Scheme can be implemented by different topologies other than those indicated in the pilot topology. For example, a forward converter suitable for operation at higher power level can be considered to replace the flyback converter.

Besides, in the pilot topology, the decoupled power is injected into the output in the form of current. Therefore, an auxiliary DC-DC converter is necessary to convert the energy stored in the power decoupling capacitor to the output current to compensate the imbalance between input and output power. Alternatively, it is possible to inject the decoupled power to the output in the form of voltage, such as the scheme proposed in [129]. One benefit of this scheme is less component count compared to the pilot topology. Future study on this scheme in terms of power decoupling capacitance and conversion efficiency is needed to verify the feasibility of this topology for microinverter with power level of 200W,

7.4.6. Solutions to effective control of the P3 pilot topology in Switching Scheme A

As discussed in Chapter 5, the proposed pilot topology has lower current stress and potential lower power loss when working in Scheme A compared to the studied Scheme B. However, Scheme A was not studied due to the control difficulties when

the output current control changes between flyback and buck converters. Further study in control of Scheme A should be considered in future work.

In this case, two individual current control loops could be used to control the output current independently. One foreseeable difficulty in this current control scheme for Scheme A is the anti-windup problem due to the saturation of one current controller when the other current control is in use. The limit levels of the control signal for effective anti-windup functioning vary with respect to the power level and dynamic conditions. Implementation in digital control could be one solution to effectively identify the varying limits for anti-windup of the controller.

REFERENCES

[1] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *Industry Applications, IEEE Transactions on,* vol. 41, pp. 1292-1306, 2005.

[2] S.B.Kjaer, "Design and Control of an Inverter for Photovoltaic Applications," PhD dissertation, Inst. Energy Technol., Aalborg University, Aalborg East, Denmark.

[3] S. B. Kjaer. *State of the Art Analysis for the 'SolcellelInverter' Project*. Available: http://130.226.56.153/rispubl/NEI/nei-dk-4508.pdf

[4] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "Power inverter topologies for photovoltaic modules-a review," in *Industry Applications Conference, 2002. 37th IAS Annual Meeting. Conference Record of the*, 2002, pp. 782-788 vol.2.

[5] G. R. Walker and P. C. Sernia, "Cascaded DC-DC converter connection of photovoltaic modules," *Power Electronics, IEEE Transactions on,* vol. 19, pp. 1130-1139, 2004.

[6] A. I. Bratcu, I. Munteanu, S. Bacha, D. Picault, and B. Raison, "Cascaded DC-DC Converter Photovoltaic Systems: Power Optimization Issues," *Industrial Electronics, IEEE Transactions on,* vol. 58, pp. 403-411, 2011.

[7] G. R. Walker and J. C. Pierce, "PhotoVoltaic DC-DC Module Integrated Converter for Novel Cascaded and Bypass Grid Connection Topologies — Design and Optimisation," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, 2006, pp. 1-7.

[8] E. Roman, R. Alonso, P. Ibanez, S. Elorduizapatarietxe, and D. Goitia, "Intelligent PV Module for Grid-Connected PV Systems," *Industrial Electronics, IEEE Transactions on,* vol. 53, pp. 1066-1073, 2006.

[9] L. Zhigang, G. Rong, L. Jun, and A. Q. Huang, "A High-Efficiency PV Module-Integrated DC/DC Converter for PV Energy Harvest in FREEDM Systems," *Power Electronics, IEEE Transactions on,* vol. 26, pp. 897-909, 2011.

[10] C. F. A. F. G.W.G. Verhoeve, E.de Held and W.C.Sinke. *Recent Test Rresults of AC-Module Inverters*.
Available: http://www.ecn.nl/docs/library/report/1997/rx97049.pdf

[11] H. Oldenkamp, I. J. de Jong, C. W. A. Baltus, S. A. M. Verhoeven, and S. Elstgeest, "Reliability and accelerated life tests of the AC module mounted OKE4 inverter," in *Photovoltaic Specialists Conference, 1996., Conference Record of the Twenty Fifth IEEE*, 1996, pp. 1339-1342.

[12] R. H. Wills, F. E. Hall, S. J. Strong, and J. H. Wohlgemuth, "The AC photovoltaic module," in *Photovoltaic Specialists Conference, 1996., Conference Record of the Twenty Fifth IEEE*, 1996, pp. 1231-1234.

[13] R. H. Wills, S. Krauthamer, A. Bulawka, and J. P. Posbic, "The AC photovoltaic module concept," in *Energy Conversion Engineering Conference,*

1997. IECEC-97., Proceedings of the 32nd Intersociety, 1997, pp. 1562-1563 vol.3.

[14] N. F. P. Association, "Article 690,Solar Photovoltaic (PV) Systems," in *National Electrical Code, NFPA 70 and NEC 2011*, ed, 2011.

[15] J. S. G. Michael Andrew de Rooij, Oliver Gerhard Mayer, Said Farouk Said EI-Barbari, "Quasi-AC, Photovoltaic Module for unfolder Photovoltaic Inverter," United States Patent US2010/0071742 A1, 2010.

[16] R. W. Miles, K. M. Hynes, and I. Forbes, "Photovoltaic solar cells: An overview of state-of-the-art cell development and environmental issues," *Progress in Crystal Growth and Characterization of Materials,* vol. 51, pp. 1-42, 2005.

[17] L. L. Kazmerski, "Photovoltaics R&D: At the Tipping Point," United States2005.

[18] R. M. Swanson, "A vision for crystalline silicon photovoltaics," *Progress in Photovoltaics: Research and Applications,* vol. 14, pp. 443-453, 2006.

[19] *List of Photovoltaic Companies*. Available: http://en.wikipedia.org/wiki/List_of_photovoltaics_companies

[20] *PVCDROM*. Available: http://pvcdrom.pveducation.org

[21] W. G. H. S. Armstrong, "A thermal model for photovoltaic panels under varying atmospheric conditions," *Applied Thermal Engineering,* pp. 1488-1495, 2010.

[22] E. Radziemska and E. Klugmann, "Photovoltaic maximum power point varying with illumination and temperature," *Transactions of the ASME. Journal of Solar Energy Engineering,* vol. 128, pp. 34-9, 2006.

[23] "IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems," *IEEE Std 1547-2003,* pp. 0_1-16, 2003.

[24] "IEEE Standard Conformance Test Procedures for Equipment Interconnecting Distributed Resources With Electric Power Systems," *IEEE Std 1547.1-2005,* pp. 0_1-54, 2005.

[25] "Photovoltaic (PV) System - Characteristics of the Utility Interface," *IEC 61727,* Dec.1st 2004.

[26] "Electrical Safety of Static Inverters and Charge Controller for Use in Photovoltaic (PV) Power Systems (WG6)," *IEC 62109 Ed.1.0 (CDV)*.

[27] "Inverters, Converters, and Controllers for Use in Independant Power Systems," ed, 2001.

[28] *Module Pricing*. Available: http://solarbuzz.com/facts-and-figures/retail-price-environment/module-prices

[29] *Inverter Prices*. Available: http://solarbuzz.com/facts-and-figures/retail-price-environment/inverter-prices

[30] M. Calais, J. Myrzik, T. Spooner, and V. G. Agelidis, "Inverters for single-phase grid connected photovoltaic systems-an overview," in *Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual*, 2002, pp. 1995-2000.

[31] N. Kasa, T. Iida, and A. K. S. Bhat, "Zero-Voltage Transition Flyback Inverter for Small Scale Photovoltaic Power System," in *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, 2005, pp. 2098-2103.

[32] S. Chandhaket, K. Ogura, M. Nakaoka, and Y. Konishi, "High-frequency flyback transformer linked utility-connected sinewave soft-switching power conditioner using a switched capacitor snubber," in *Power Electronics and Motion Control Conference, 2004. IPEMC 2004. The 4th International*, 2004, pp. 1242-1247 Vol.3.

[33] M. Fornage, "Method and Apparatus For Improved Burst Mode During Power Conversion," United Stataes Patent US20100091532A1, Apr. 15, 2010.

[34] T. Shimizu, K. Wada, and N. Nakamura, "Flyback-Type Single-Phase Utility Interactive Inverter With Power Pulsation Decoupling on the DC Input for an AC Photovoltaic Module System," *Power Electronics, IEEE Transactions on,* vol. 21, pp. 1264-1272, 2006.

[35] T. Hirao, T. Shimizu, M. Ishikawa, and K. Yasui, "A modified modulation control of a single-phase inverter with enhanced power decoupling for a photovoltaic AC module," in *Power Electronics and Applications, 2005 European Conference on*, 2005, pp. 10 pp.-P.10.

[36] G. H. Tan, J. Z. Wang, and Y. C. Ji, "Soft-switching flyback inverter with enhanced power decoupling for photovoltaic applications," *Electric Power Applications, IET,* vol. 1, pp. 264-274, 2007.

[37] H. Haibing, Z. Qian, F. Xiang, Z. J. Shen, and I. Batarseh, "A single stage micro-inverter based on a three-port flyback with power decoupling capability," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 1411-1416.

[38] T. Shimizu and S. Suzuki, "Control of a high-efficiency PV inverter with power decoupling function," in *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on*, 2011, pp. 1533-1539.

[39] L. Quan and P. Wolfs, "A Review of the Single Phase Photovoltaic Module Integrated Converter Topologies With Three Different DC Link Configurations," *Power Electronics, IEEE Transactions on,* vol. 23, pp. 1320-1333, 2008.

[40] J. M. A. Myrzik and M. Calais, "String and module integrated inverters for single-phase grid connected photovoltaic systems - a review," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, 2003, p. 8 pp. Vol.2.

[41] X. Yaosuo, C. Liuchen, K. Sren Baekhj, J. Bordonau, and T. Shimizu, "Topologies of single-phase inverters for small distributed power generators: an overview," *Power Electronics, IEEE Transactions on,* vol. 19, pp. 1305-1314, 2004.

[42] F. Blaabjerg, C. Zhe, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *Power Electronics, IEEE Transactions on,* vol. 19, pp. 1184-1194, 2004.

[43] *SunnyBoy, SMA*. Available:

http://www.sma-america.com/en_US/products/grid-tied-inverters/sunny-boy.html

[44] G. Frattini, G. Petrone, G. Spagnuolo, and M. Vitelli, "AC module design employing low capacitance values," in *Industrial Electronics (ISIE), 2010 IEEE International Symposium on*, 2010, pp. 3444-3449.

[45] E. Mamarelis, G. Petrone, B. Sahan, G. Lempidis, G. Spagnuolo, and P. Zacharias, "What is the best dc/dc converter for an AC module? Experimental analysis of two interesting solutions," in *Industrial Electronics (ISIE), 2011 IEEE International Symposium on*, 2011, pp. 1759-1764.

[46] W. Yu, J. S. Lai, H. Qian, and C. Hutchens, "High-Efficiency MOSFET Inverter with H6-Type Configuration for Photovoltaic Non-Isolated AC Module Applications," *Power Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2010.

[47] S. V. Araujo, P. Zacharias, and R. Mallwitz, "Highly Efficient Single-Phase Transformerless Inverters for Grid-Connected Photovoltaic Systems," *Industrial Electronics, IEEE Transactions on,* vol. 57, pp. 3118-3128, 2010.

[48] M. Fornage, "Method and Apparatus for Converting Direct Current to Alternating Current," US20070221267, 2007.

[49] E. C. T. N. P. Papanikolaou, A.Critsis, D. Klimis, "Simplified High Frequency Converter in Decentralized Grid-connected PV Systems: a novel Low-Cost Solution," in *Proc. EPE03*, 2003.

[50] A. C. Kyritsis, E. C. Tatakis, and N. P. Papanikolaou, "Optimum Design of the Current-Source Flyback Inverter for Decentralized Grid-Connected Photovoltaic Systems," *Energy Conversion, IEEE Transactions on,* vol. 23, pp. 281-293, 2008.

[51] A. Fernandez, J. Sebastian, M. M. Hernando, M. Arias, and G. Perez, "Single Stage Inverter for a Direct AC Connection of a Photovoltaic Cell Module," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, 2006, pp. 1-6.

[52] Q. Li and P. Wolfs, "A Current Fed Two-Inductor Boost Converter With an Integrated Magnetic Structure and Passive Lossless Snubbers for Photovoltaic Module Integrated Converter Applications," *Power Electronics, IEEE Transactions on,* vol. 22, pp. 309-321, 2007.

[53] C. Rodriguez and G. A. J. Amaratunga, "Long-Lifetime Power Inverter for Photovoltaic AC Modules," *Industrial Electronics, IEEE Transactions on,* vol. 55, pp. 2593-2601, 2008.

[54] C. Woo-Young, K. Bong-Hwan, and L. Jih-Sheng, "High-efficiency grid-connected photovoltaic module integrated converter system," in *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, 2009, pp. 731-736.

[55] K. C. A. de Souza, M. R. de Castro, and F. Antunes, "A DC/AC converter for single-phase grid-connected photovoltaic systems," in *IECON 02 [Industrial Electronics Society, IEEE 2002 28th Annual Conference of the]*, 2002, pp. 3268-3273 vol.4.

[56] S. Yatsuki, K. Wada, T. Shimizu, H. Takagi, and M. Ito, "A novel AC photovoltaic module system based on the impedance-admittance conversion theory," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, 2001, pp. 2191-2196 vol. 4.

[57] A. Trubitsyn, B. J. Pierquet, A. K. Hayman, G. E. Gamache, C. R. Sullivan, and D. J. Perreault, "High-efficiency inverter for photovoltaic applications," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, 2010, pp. 2803-2810.

[58] F. B. S.B.Kjaer, "A novel single-stage inverter for the AC module with reduced low - frequency penetration," in *The 10th European Power Electronics and Applications Conference (EPE03)*, 2003.

[59] S. V. Araujo, P. Zacharias, and B. Sahan, "Novel grid-connected non-isolated converters for photovoltaic systems with grounded generator," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 58-65.

[60] W. B. Dan Ton. (2005, Retrieved 2011-06-10). Summary Report on the DOE High-tech Inverter Workshop. Available: http://www1.eere.energy.gov/solar/pdfs/inverter_ii_workshop.pdf

[61] J. Wiles. (2007, Photovoltaic Power Systems and the 2005 National Electrical Code: Suggested Practices. Available: http://www.brooksolar.com/files/PVSuggestPract2005.pdf

[62] M. Kusakawa, H. Nagayoshi, K. Kamisako, and K. Kurokawa, "Further improvement of a transformerless, voltage-boosting inverter for AC modules," in *11th International Photovoltaic Science and Engineering Conference, 20-24 Sept. 1999*, Netherlands, 2001, pp. 379-87.

[63] B. Gu, J. Dominic, J. Lai, C. Chen, and B. Chen, "High Reliability and Efficiency Single-Phase Transformerless Inverter for Grid-Connected Photovoltaic Systems," *Power Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2012.

[64] T. Kerekes, R. Teodorescu, and U. Borup, "Transformerless Photovoltaic Inverters Connected to the Grid," in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, 2007, pp. 1733-1737.

[65] R. Gonzalez, J. Lopez, P. Sanchis, and L. Marroyo, "Transformerless Inverter for Single-Phase Photovoltaic Systems," *Power Electronics, IEEE Transactions on,* vol. 22, pp. 693-697, 2007.

[66] M. Calais, V. G. Agelidis, L. J. Borle, and M. S. Dymond, "A transformerless five level cascaded inverter based single phase photovoltaic system," in *Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual*, 2000, pp. 1173-1178 vol.3.

[67] T. M. U. Ned Mohan, William P. Robbins, Ed., *Power Electronics: Converters, Applications and Design*. p.^pp. Pages.

[68] M. Prudente, L. L. Pfitscher, and R. Gules, "A Boost Converter With Voltage Multiplier Cells," in *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, 2005, pp. 2716-2721.

[69] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "Voltage Multiplier Cells Applied to Non-Isolated DC DC Converters," *Power Electronics, IEEE Transactions on,* vol. 23, pp. 871-887, 2008.

[70] F. Schimpf and L. Norum, "Effective use of film capacitors in single-phase PV-inverters by active power decoupling," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010, pp. 2784-2789.

[71] *Power Film Capacitor Application Guide*. Available: http://www.cde.com/

[72] L. Yazhou, G. T. Heydt, and R. F. Chu, "The power quality impact of cycloconverter control strategies," *Power Delivery, IEEE Transactions on,* vol. 20, pp. 1711-1718, 2005.

[73] A. K. S. Bhat and S. B. Dewan, "Resonant Inverters for Photovoltaic Array to Utility Interface," in *Telecommunications Energy Conference, 1986. INTELEC '86. International*, 1986, pp. 135-142.

[74] A. K. S. Bhat and S. B. Dewan, "Input-output harmonics of line-current-modulated high-frequency link DC to utility power converters," *Power Electronics, IEEE Transactions on,* vol. 4, pp. 253-264, 1989.

[75] J. A. C. Oscar Garcia, Roberto Prieto, Pedro Alou and Javier Uceda, "Single Phase Power Factor Correction: A Survey," *IEEE Transactions on Power Electronics,* vol. Vol.18, pp. Page 749-755, May 2003.

[76] C. Prapanavarat, M. Barnes, and N. Jenkins, "Investigation of the performance of a photovoltaic AC module," *IEE Proceedings-Generation, Transmission and Distribution,* vol. 149, pp. 472-8, 2002.

[77] T. Feng, H. Al-Atrash, R. Kersten, C. Scholl, K. Siri, and I. Batarseh, "A single-staged PV array-based high-frequency link inverter design with grid connection," in *Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE*, 2006, p. 4 pp.

[78] S. Chandhaket, Y. Konishi, K. Ogura, and M. Nakaoka, "Utility AC interfaced soft-switching sinewave PWM power conditioner with two-switch flyback high-frequency transformer," *Electric Power Applications, IEE Proceedings -,* vol. 151, pp. 526-533, 2004.

[79] S. K. Mazumder, R. K. Burra, R. Huang, and V. Arguelles, "A low-cost single-stage isolated differential Cuk inverter for fuel-cell application," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 4426-4431.

[80] S. Yu Jin, C. Se-Kyo, and P. N. Enjeti, "A current-fed HF link direct DC/AC converter with active harmonic filter for fuel cell power systems," in *Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE*, 2004, p. 128 Vol.1.

[81] C. E. Commission. (Feb. 2009). *Emerging renewables program guidebook (9th Edition ed.)*. Available: http://www.energy.ca.gov/

[82] *Enphase Energy*. Available: http://enphase.com

[83] *Microinverters -Involar*. Available: http://www.involar.com/

[84] *Enecsys micro inverters*.

Available: http://www.enecsys.com/products/micro-inverter.php
[85] *Reliable Micro Inverter - Greenray Solar*.
Available: http://www.greenraysolar.com/technology/micro-inverter
[86] *SMA American, LLC*.
Available: http://www.sma-america.com/en_US/home.html
[87] *Solar Inverter - Power-One*.
Available: http://www.power-one.com/renewable-energy/products/solar
[88] L. B. H. Haeberlin, M. Kaempfer and U. Zwahlen, "Total Efficiency - a new Quantity for better characterisation of grid-connected PV inverters," presented at the 20th European Photovoltaic Solar Energy Conference, Barcelona, Spain, 2005.
[89] H. S. F. P.Baumgartner, B. Burger, R. Brundlinger, H. Haberlin, M. Zehner, "Status and relevance of the DC voltage dependency of the inverter efficiency," presented at the 22nd European Photovoltaic Solar Energy Conference and Exhibition,, Fiera Milano, 2007.
[90] C.-H. F. Chao-Hsuan Chuang, Hung-Che Chou, "Light-load efficiency improvement method and appratus for a flyback converter," United States Patent US 7,609,533 B2, 2009.
[91] S. G. Parler, "Deriving Life Multipliers for Aluminum Electrolytic Capacitors," *IEEE Power Electronics Society Newsletter,* vol. Vol.16, pp. 11-12, 2004.
[92] R. S. Balog, K. Yingying, and G. Uhrhan, "A photovoltaic module thermal model using observed insolation and meteorological data to support a long life, highly reliable module-integrated inverter design by predicting expected operating temperature," in *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, 2009, pp. 3343-3349.
[93] F. Shinjo, K. Wada, and T. Shimizu, "A Single-Phase Grid-Connected Inverter with a Power Decoupling Function," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, 2007, pp. 1245-1249.
[94] J. S. Shaffer. (2009). *Evaluation of Electrolytic Capacitor Application in Enphase Microinverters*. Available: http://enphase.com/support/downloads/
[95] M. Fornage, "Reliability Study of Electrolytic Capacitors in a Micro-Inverter," 2008.
[96] Z. Kun, P. Ciufo, and S. Perera, "Lifetime analysis of aluminum electrolytic capacitor subject to voltage fluctuations," in *Harmonics and Quality of Power (ICHQP), 2010 14th International Conference on*, 2010, pp. 1-5.
[97] H. Haibing, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "Power decoupling techniques for micro-inverters in PV systems-a review," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, 2010, pp. 3235-3240.
[98] A. C. Kyritsis, N. P. Papanikolaou, and E. C. Tatakis, "Enhanced Current Pulsation Smoothing Parallel Active Filter for single stage grid-connected

AC-PV modules," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*, 2008, pp. 1287-1292.

[99] K. Tsuno, T. Shimizu, K. Wada, and K. Ishii, "Optimization of the DC ripple energy compensating circuit on a single-phase voltage source PWM rectifier," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, 2004, pp. 316-321 Vol.1.

[100] G. Ertasgin, D. M. Whaley, N. Ertugrul, and W. L. Soong, "Analysis and design of energy storage for current-source 1-ph grid-connected PV inverters," in *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE*, 2008, pp. 1229-1234.

[101] R. S. B. Philip T. Krein, "Cost-Effective Hundred-Year Life for Single-Phase Inverters and Rectifiers in Solar and LED Lighting Applications Based on Minimum Capacitance Requirements and a Ripple Power Port," in *Applied Power Electronics Conference and Exposition,*, 2009, pp. pp. 620-625.

[102] L. Quan, P. Wolfs and S.Senini, "A hard switched high frequency link converter with constant power output for photovoltaic applications," in *Proc. Australiasian Univ. Power Eng. Conf.*, 2002.

[103] R. S. B. Philip T. Krein, JR., "Methods for minimizing double-frequency ripple power in single phase power conditioners," United States Patent US2009/0097283 A1, 2009.

[104] A. C. Kyritsis, N. P. Papanicolaou, and E. C. Tatakis, "A novel Parallel Active Filter for Current Pulsation Smoothing on single stage grid-connected AC-PV modules," in *Power Electronics and Applications, 2007 European Conference on*, 2007, pp. 1-10.

[105] S. B. Kjaer and F. Blaabjerg, "Design optimization of a single phase inverter for photovoltaic applications," in *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual*, 2003, pp. 1183-1190 vol.3.

[106] Y.-H. Ji, D.-Y. Jung, J.-H. Kim, C.-Y. Won, and D.-S. Oh, "Dual mode switching strategy of flyback inverter for photovoltaic AC modules," in *Power Electronics Conference (IPEC), 2010 International*, 2010, pp. 2924-2929.

[107] C. H. a. S. Bowden. *PV CDROM*.
Available: http://www.pveducation.org/pvcdrom

[108] P. C. Todd. (May 1993). *Snubber Circuits: Theory, Design and Application*.

[109] C. Jaen, C. Moyano, X. Santacruz, J. Pou, and A. Arias, "Overview of maximum power point tracking control techniques used in photovoltaic systems," in *Electronics, Circuits and Systems, 2008. ICECS 2008. 15th IEEE International Conference on*, 2008, pp. 1099-1102.

[110] H. P. Desai and H. K. Patel, "Maximum Power Point Algorithm in PV Generation: An Overview," in *Power Electronics and Drive Systems, 2007. PEDS '07. 7th International Conference on*, 2007, pp. 624-630.

[111] G. S. L.Rossetto, P. Tenti, "Control Techniques for Power Factor Correction Converters," in *PEMC*, 1994, pp. 1310-1318.

[112] K. M. Smedley and S. Cuk, "One-cycle control of switching converters," *Power Electronics, IEEE Transactions on,* vol. 10, pp. 625-633, 1995.

[113] J. L.H.Dixon, "The Right-Half-Plane Zero: a Simplified Explanation," Unitrode Power Supply Design Seminar1983.

[114] L. Dixon, "Average current mode control of Switching Power Supplies," *Unitrode Application Note U-140*.

[115] D. M. Robert W. Erickson, *Fundamentals of Power Electronics*, 2nd ed.: Springer, Jan. 2001.

[116] D. Alfano. *Evaluating AC Current Sensor Options for Power Delivery Systems*. Available: https://www.silabs.com/Support%20Documents/TechnicalDocs/Evaluating-AC-Current-Sensor-Options-for-Power-Delivery-Systems.pdf

[117] N. McNeill and N. K. Gupta, "Assessment of the error in the average current sensed by the unidirectional current pulse transformer," *Circuits, Devices & Systems, IET,* vol. 2, pp. 265-276, 2008.

[118] H. Marecar and R. Oruganti, "Fast and Accurate Current Sensing in a Multiphase Buck Converter," in *Power Electronics and Drives Systems, 2005. PEDS 2005. International Conference on*, 2005, pp. 166-171.

[119] D. C. Hamill, J. H. B. Deane, and D. J. Jefferies, "Modeling of chaotic DC-DC converters by iterated nonlinear mappings," *Power Electronics, IEEE Transactions on,* vol. 7, pp. 25-36, 1992.

[120] S. Parui and S. Banerjee, "Bifurcations due to transition from continuous conduction mode to discontinuous conduction mode in the boost converter," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on,* vol. 50, pp. 1464-1469, 2003.

[121] R. Srinivasan, "Single Phase Power Factor Correction - Investigation and Development of Advanced Techniques," National University of Singapore, 1998.

[122] Y. Jiang, "Development of Advanced Power Factor Correction Techniques," PhD thesis, Virginia Polytechnic Institute and State University, 1994.

[123] "KC200GT High Efficiency Multicrystal Photovoltaic Module," Kyocera, Ed., ed.

[124] T. Bhattacharya, V. S. Giri, K. Mathew, and L. Umanand, "Multiphase Bidirectional Flyback Converter Topology for Hybrid Electric Vehicles," *Industrial Electronics, IEEE Transactions on,* vol. 56, pp. 78-84, 2009.

[125] X. Weidong, N. Ozog, and W. G. Dunford, "Topology Study of Photovoltaic Interface for Maximum Power Point Tracking," *Industrial Electronics, IEEE Transactions on,* vol. 54, pp. 1696-1704, 2007.

[126] T. Kitano, M. Matsui, and X. De-hong, "Power sensor-less MPPT control scheme utilizing power balance at DC link-system design to ensure stability and response," in *Industrial Electronics Society, 2001. IECON '01. The 27th Annual Conference of the IEEE*, 2001, pp. 1309-1314 vol.2.

[127] W. Xiaoqun, C. K. Tse, O. Dranga, and L. Junan, "Fast-scale instability of single-stage power-factor-correction power supplies," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 53, pp. 204-213, 2006.

[128] C. K. Tse and M. di Bernardo, "Complex behavior in switching power converters," *Proceedings of the IEEE,* vol. 90, pp. 768-781, 2002.

[129] B. M. T. Ho and S.-H. C. Henry, "An integrated inverter with maximum power tracking for grid-connected PV systems," *Power Electronics, IEEE Transactions on,* vol. Volume 20, pp. Page(s):953 - 962 July 2005.

[130] D. M. Sable, B. H. Cho, and R. B. Ridley, "Use of leading-edge modulation to transform boost and flyback converters into minimum-phase-zero systems," *Power Electronics, IEEE Transactions on,* vol. 6, pp. 704-711, 1991.

[131] K. M. Smedley and S. Cuk, "One-cycle control of switching converters," *Power Electronics, IEEE Transactions on,* vol. 10, pp. 625-633, 1995.

[132] L. Dixon, "Average current mode control of Switching Power Supplies," *Unitrode Application Note U-140*.

Appendix A: Microinverter Specifications

As each PV panel would need a separate inverter, a large enough power rating is preferred for AC module application so as to reduce the cost per watt. Several existing PV modules available in market are tabulated in Table. 1.1 and most of them are with a power level around 200W. Therefore, the study in this thesis is carried out for a power level of 200W. Kyocera PV module KC200GT [123] has been chosen as a representative panel for study purposes. It uses multi crystalline Si technology and has a catalogue conversion efficiency over 16%. Its key specifications are tabulated in Table A. 1.

Table A. 1: Key Specifications of PV Module KC200GT

Parameters	STC[1]	800W/m^2, NOCT[2], AM1.5
Maximum Power P_{mp}	200 W	142 W
Maximum Power Voltage V_{mp}	26.3 V	23.2 V
Maximum Power Current I_{mp}	7.61 A	6.13 A
Open Circuit Voltage V_{oc}	32.9 V	29.9 V
Short Circuit Voltage I_{sc}	8.21 A	6.62 A
Temperature Coefficient of V_{oc}	-0.123 V/^{o}C	
Temperature Coefficient of I_{sc}	0.00318 A/^{o}C	

STC[1]: Irradiance 1000W/m^2, AM1.5 spectrum, module temperature 25^{o}C;
NOCT[2] (Nominal Operating Cell Temperature): 47 ^{o}C.

As shown in Table A. 1, the variation of PV module voltage is mainly influenced by temperature. Theoretically, a voltage variation of ± 6.15 V is expected if a temperature range of -25^{o}C~ 75^{o}C is considered. Thus, in the study through this thesis, a nominal PV module voltage is chosen as 27V, and the PV module MPPT voltage is expected to vary from 20V~34V. The grid side connection under study is with a RMS value of 230V and an AC frequency of 50Hz.

Appendix B: Problems with Direct Output Current Control for Flyback-CCM Inverter

B.1 Introduction

Direct Output Current Control refers to controlling the output current directly to track the desired rectified sine waveform in a closed loop manner. It is well known that the flyback converter in CCM operation is a non-minimum phase system with a right half plane (RHP) zero in the linearized, small signal control to output current transfer function, which would greatly limit the achievable system bandwidth and dynamic response [130]. As discussed in Section 4.3, two current controllers, i.e. One Cycle Control (OCC) and Average Current Control (ACC) have been studied in an effort to directly control the output current of flyback inverter. The difficulties in the direct current control are examined in this appendix.

B.2 Problems with Direct One Cycle Control

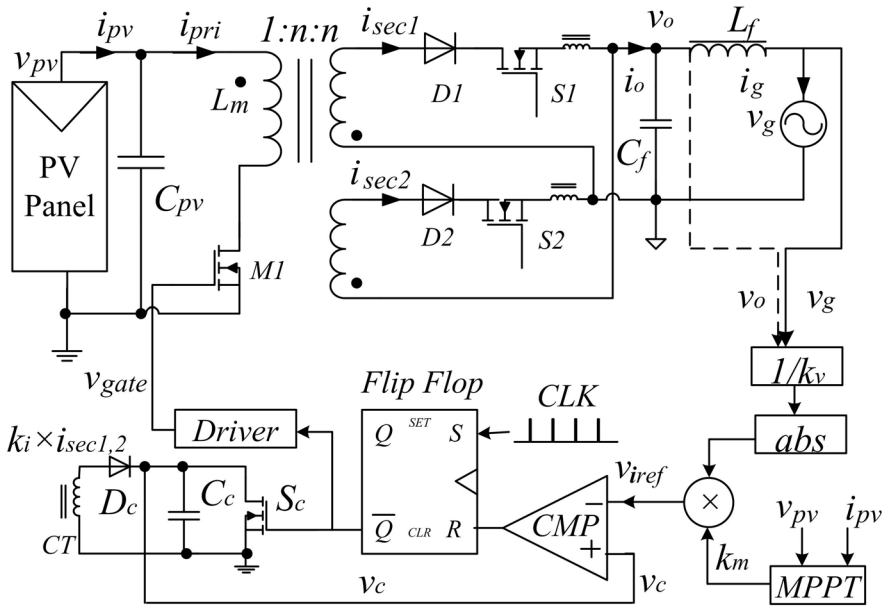


Fig.B. 1: Circuit diagram for direct OCC scheme

One Cycle Control [131] is often used to achieve fast response current control in DC-DC and AC-DC converters. An attempt was first made to directly control and shape the secondary side current using such One Cycle Control (OCC) method. The OCC scheme was implemented as shown in Fig.B. 1.

In the scheme, two CTs are used to sense the 'net' secondary side current of the flyback converter. The MPPT circuit (not implemented here) generates the factor k_m which determines the magnitude of the output current reference signal v_{iref}, while the shape of the signal v_{iref} is determined by the rectified AC voltage waveshape. A fixed frequency clock generates a pulse to turn off the main MOSFET M1 and the capacitor switch S_C. The current sensing signal starts to charge the capacitor C_C until it reaches the value of the reference signal v_{iref}.

Hence, with a constant switching period, the peak capacitor voltage $\hat{v}_C$, is proportional to the average secondary side current in each switching cycle. Thus,

$$\hat{v}_C = k_i I_{\text{sec}1,2} / C_C f_s \tag{B-1}$$

Here, $I_{\text{sec}1,2}$ represents the switching-average current of the secondary side legs.

Once the peak capacitor voltage $\hat{v}_C$ reaches the reference value of v_{iref}, it triggers the RS flip flop, whose output is used to turn on the main MOSFET M1 and the capacitor switch S_C. In this way, the capacitor C_C is discharged to zero and the system waits for the next cycle.

The main circuit parameters of the flyback-CCM inverter are given in Table 3.2. The simulation results are shown in Fig.B. 2.

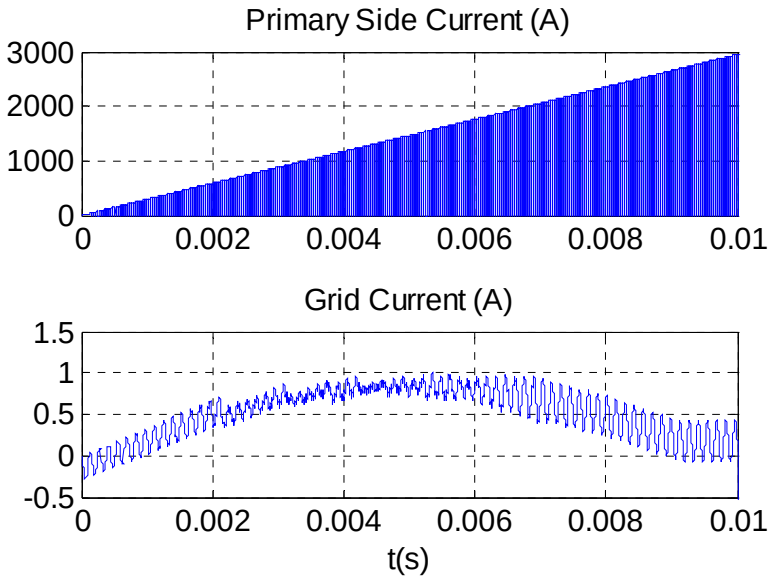


Fig.B. 2: Instability of Direct OCC scheme

Even though the grid current is bounded and largely follows the sinusoidal reference in Fig.B. 2, the primary side current, i_{pri}, is unstable and increases in an uncontrolled manner, which is unacceptable. This is found to be caused by the incomplete demagnetization of flyback transformer in CCM operation. As a result, primary side current builds up, which would lead to eventual failure of the components in the circuit.

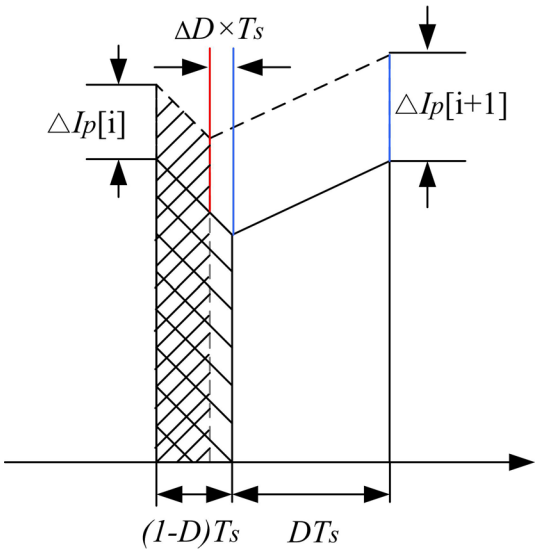


Fig.B. 3: Transformer current reflected to the primary side for stability analysis

In order to study the instability phenomenon, the waveform of the transformer current (both primary and secondary sides) reflected on to the primary side is illustrated in Fig.B. 3. The waveform highlighted with shaded area is the output current portion of the waveform. Let us assume that the waveform reaches steady state at a duty ratio of D. If a disturbance of $\Delta I_p[i]$ occurs at the ith cycle, in order to maintain the same average output current, the propagation of $\Delta I_p[i+1]$ compared to $\Delta I_p[i]$ can be obtained as:

$$\frac{\Delta I_p[i+1]}{\Delta I_p[i]} = 1 + \frac{V_{pv} + V_{grid}/n}{L_m} \cdot \frac{\Delta D \cdot T_s}{\Delta I_p[i]} > 1 \qquad \text{(B-2)}$$

According to Fig.B. 3 and (B-2) , it is noted that when the cyclic peak primary side current is perturbed for any reason, the off-time duty ratio $(1-D)$ is reduced because of charge control (the area under the down-slope is equal to the required secondary side current over one switching cycle). The on-time duty ratio D is increased thereafter, which further increases the cyclic peak primary current at the next cycle. In this way, a positive feedback situation occurs, which causes the instability in current control. Thus, the direct OCC method is not usable in this case.

B.3 Direct Average Current Control

In this section, we investigate the issues involved in directly controlling the secondary side current through average current control method. The control scheme adopted is shown in Fig.B. 4. As in the case of OCC, the reference current signal v_{iref} is shaped by the grid AC voltage waveform and is in phase with it. The

magnitude of v_{iref} is determined by the MPPT, which is not implemented here. The feedback current v_{ifb} is obtained by sensing the two secondary side currents. The error between the reference v_{iref} and the feedback variables v_{ifb} is fed to the average current controller whose output determines the duty cycle of M1. A separate averaging filter for the current feedback signal, v_{ifb}, is not needed since the current controller gain is very low at the switching frequencies, which will act to filter out the switching frequency components.

Due to the existence of RHP (Right Half Plane) zero in the control-to-output current transfer function in CCM operation, the low frequency gain of the controller is limited especially in DCM operation. Due to this, the inverter was found to be unable to track the reference. This problem is discussed in detail in the following three sub-sections.

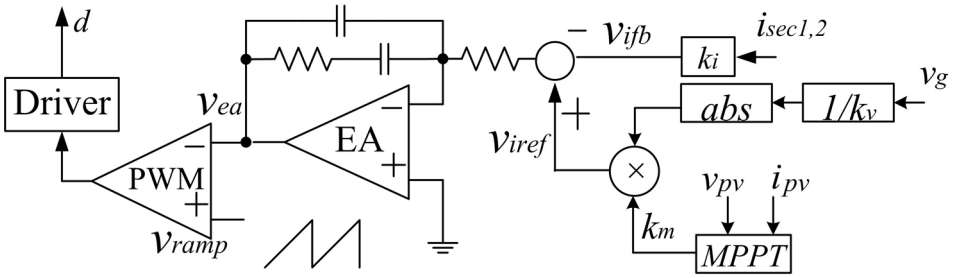


Fig.B. 4: Direct average current control scheme

B.3.1 Plant Models

The same assumptions defined in Section 4.4.2.1 are valid in this part, which include ideal operation of the flyback inverter without considering parasitic components and a constant voltage load. It must be emphasized that in obtaining control-to-output current transfer functions, the converter is assumed to operate in a

DC-DC operating mode with V_g and I_g equal to different switching-period average values in an AC cycle.

In CCM, the control-to-output current transfer function [132] can be derived as:

$$G_{od\_CCM} = \frac{\tilde{i}_{\sec}}{\tilde{d}} = \frac{1}{n}\left(\frac{V_{pv}}{sL_m} - I_{Lm}\right) = \frac{1}{n}\left[\frac{V_{pv}}{sL_m} - (I_{pri} + nI_o)\right] \tag{B-3}$$

where I_{Lm} represents the switching-period average magnetizing current of the flyback transformer reflected at the primary side, which include the primary side current I_{pri} and the reflected average secondary side current nI_o.

This transfer function can be rewritten in the form below to demonstrate its variation in terms of power level P_{pv} and grid voltage V_g:

$$G_{od\_CCM} = \frac{b}{s} \times \left(1 - \frac{s}{z_R}\right) \tag{B-4}$$

where $b = \frac{V_{pv}}{nL_m}$ and $z_R = \frac{V_{pv}}{L_m \cdot (I_{pri} + nI_o)} = \frac{V_{rms}^2 V_{pv}^2}{P_{pv} L_m} \cdot \frac{1}{|V_g| \cdot (|V_g| + nV_{pv})}$.

It is noted from (B-4) that there is an integrator at origin and a RHP zero Z_R, which is derived above considering the instantaneous power balance equation given in (3-18) and the switching-period average output current in (B-5).

$$V_{pv} I_{pri} = V_g I_g = 2V_{rms} I_{rms} \sin^2(\omega t) \tag{3-18}$$

$$I_o \approx I_g = V_g P_{pv} / V_{rms}^2 \tag{B-5}$$

In DCM, the control-to-output current transfer function can be also derived as a function of input power P_{pv}:

$$G_{od\_DCM} == \frac{\tilde{i}_{\sec}}{\tilde{d}} = \frac{V_{pv}}{V_{rms}}\sqrt{\frac{T_s \cdot P_{pv}}{2L_m}} \tag{B-6}$$

The duty cycle of the main switch M1 varies with AC voltage, power level as well as operating modes as given by:

$$\text{DCM:} \qquad D_d = \frac{|V_g|}{V_{rms}}\sqrt{\frac{2I_{pv}L_m f_s}{V_{pv}}} = \frac{|V_g|}{V_{rms}V_{pv}}\sqrt{2L_m P_{pv} f_s} \tag{3-21}$$

$$\text{CCM:} \qquad D_c = \frac{|v_g|}{nV_{pv} + |v_g|} \tag{3-22}$$

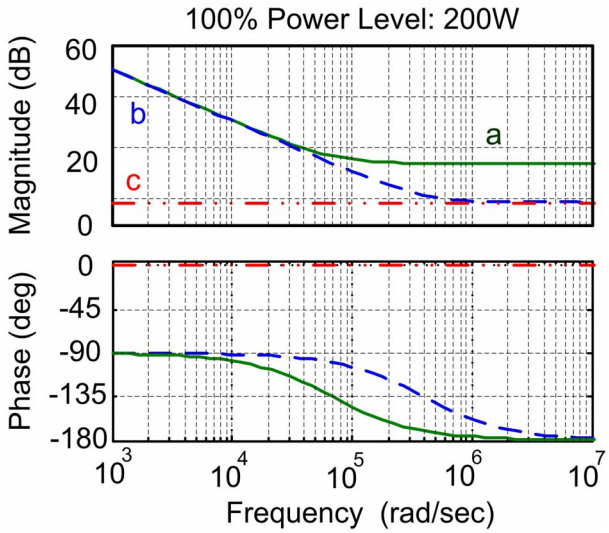
Theoretically, the boundary state between CCM and DCM will occur at certain grid voltage V_{gb}. Under this condition, the duty cycle predicted by (3-21) will equal that predicted by (3-22). From this, it can be shown that:

$$V_{gb} = V_{pv}(V_{rms}\sqrt{\frac{1}{2P_{pv} f_s L_m}} - n) \tag{3-26}$$

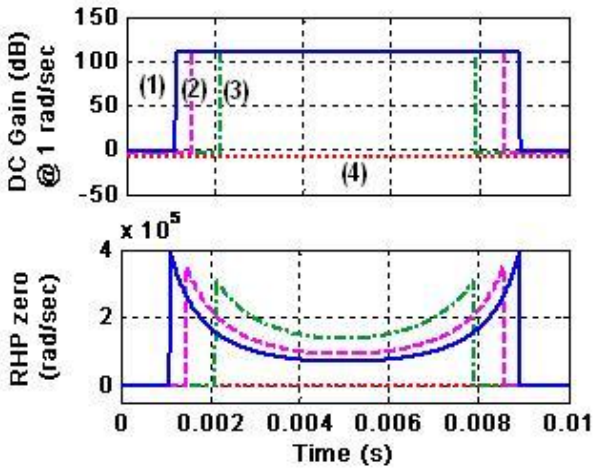
In each half of an AC cycle, the inverter will operate in DCM when $V_g < V_{gb}$ and in CCM when $V_g > V_{gb}$.

Equations (B-4) and (B-6) describe the complete set of plant transfer functions during one AC cycle. The plant transfer function is an integrator with a RHP zero in CCM mode and a constant in DCM mode. These are plotted for a nominal power of 200W in Fig.B. 5 a). Here, plot a and plot b correspond to $V_g = \sqrt{2}V_{rms}$ and $V_g = V_{gb}$. These represent the range of transfer functions under CCM conditions. Plot c corresponds to $V_g < V_{gb}$ and represents the transfer function in DCM condition. At a given power level, when the grid voltage increases from zero to

maximum, the DC gain under DCM operation is a constant before entering CCM mode. During the transition, a sudden change of the DC gain occurs with an additional RHP being introduced (jump from curve c to curve b). In CCM mode, as V_g increases, the DC gain remains constant while the RHP zero moves to lower frequencies.



a) Control-to-output current transfer functions. a: CCM with $V_g = \sqrt{2}V_{rms}$; b: CCM with $V_g = V_{gb}$; c: DCM.



b) Variation of DC gain and RHP zero at (1) 100%, (2) 75%, (3) 50% and (4) 25% of power rating.

Fig.B. 5: The control-to-output current transfer function in terms of AC voltage and power variation

The variation of the DC gain (at 1 rad/sec) and RHP zero over half an AC cycle

are shown in Fig.B. 5 b) at four different power levels. It is noted that the DC gain at 1 rad/sec in DCM (ranging from -7.64dB to -1.62dB for 25% to 100% power levels) is much lower than that of CCM operations (around 110dB). Both gains remain constant with in an AC cycle. When the power level reduces, the DC gain in CCM is not influenced but the gain in DCM reduces with power. The RHP zero reduces with increasing power level and grid voltage. The minimum RHP zero occurs at 6.85×10^4 rad/sec (or 10.9 kHz) at the maximum power level and the maximum grid voltage, which is the worst case to consider in controller design

B.3.2 Controller Design

Since the DCM operation transfer function (B-6) is a mere gain, stability of the closed loop system is not an issue in DCM. Thus, the focus of the controller design is on CCM operation. This is discussed below.

A large DC gain is introduced by adding an integrator at the origin. Besides, one pole and one zero are added at the two sides of the RHP zero to provide enough phase margin and roll-off slope at the cross-over frequency. The design process of the controller is similar to the steps outlined in greater detail in Section 4.4.2.2.

The controller is designed to be: (the pole: $1.47\times10^5\,rad/sec$; zero: $1.68\times10^3\,rad/sec$)

$$C_2=\frac{94.366}{s}\frac{1+5.9\times10^{-4}s}{1+6.8\times10^{-6}s} \tag{B-7}$$

The open-loop and closed-loop bode plots of the inverter working in CCM are

shown in Fig.B. 6.

As shown in Fig.B. 6, the crossover frequency is $3.15kHz\,(1.98\times10^4\,\text{rad/sec})$, which is limited to be less than the minimal RHP zero (10.9kHz) to ensure enough phase margin.

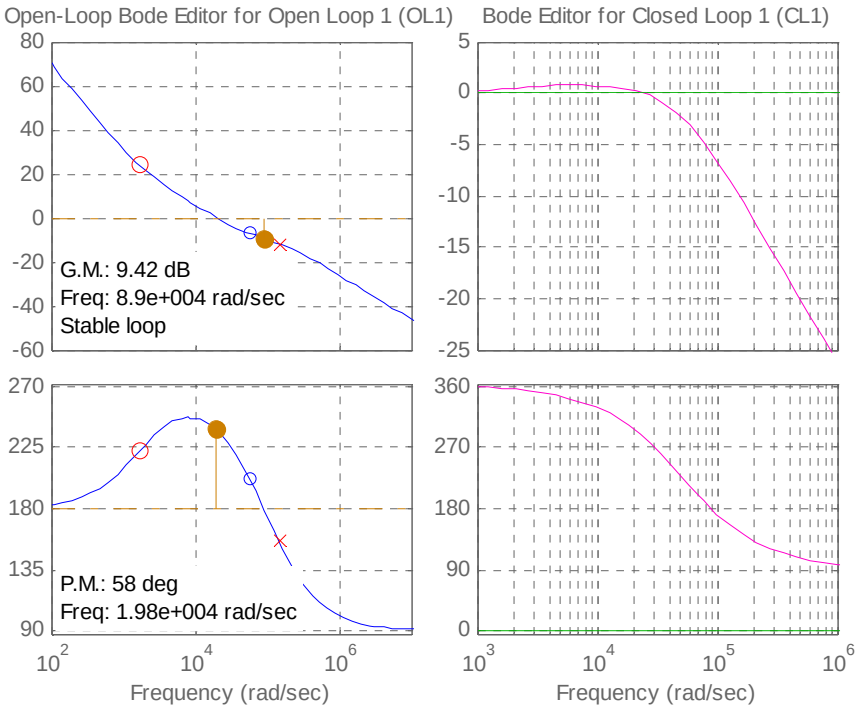


Fig.B. 6: Open-loop and Closed-loop Bode plots for CCM operation (200W, $V_g=\sqrt{2}V_{rms}$)

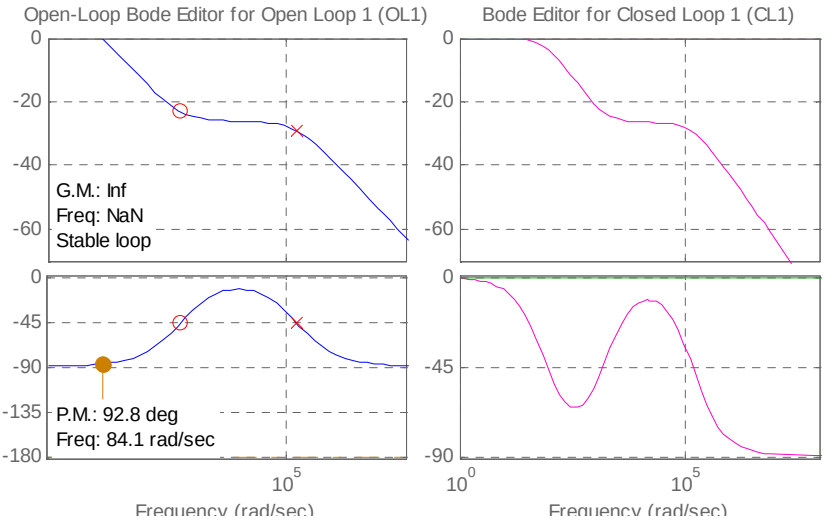


Fig.B. 7: Open-loop and Closed-loop Bode plots for DCM operation (200W)

However, when the flyback inverter works in DCM operation, the open-loop and closed-loop Bode plots with the designed controller can be shown in Fig.B. 7. It is noted that even with an integrator at the origin, DC gain at low frequency is very low and system bandwidth is 84.1 rad/sec (13.4 Hz), which is even less than the desired current shaping frequency of 100Hz.

B.3.3 Current Tracking Performance

Fig.B. 8 presents the simulation waveforms of the primary side current and the grid current obtained using the secondary side average current control.

It is observed that the flyback inverter works in DCM when starting from the zero crossing instant. Sudden changes of the primary side current waveform are observed at around 0.046s and 0.056s; these are caused by the transition from DCM to CCM operation. In DCM operation, the inverter fails to track the reference signal because of the low gain at low frequency and limited system bandwidth as predicted from the analysis. On the one hand, the transition from DCM to CCM operation is greatly delayed due to the slow response in the DCM region. On the other hand, the accumulated error in the DCM region is carried forward, causing an overshoot when CCM operation starts. This, in turn, unexpectedly increases the magnetizing current of the flyback transformer. As a result, around the grid zero-crossing intervals, the flyback-CCM inverter is unable to demagnetize its current completely and keeps working in CCM, instead of in DCM.

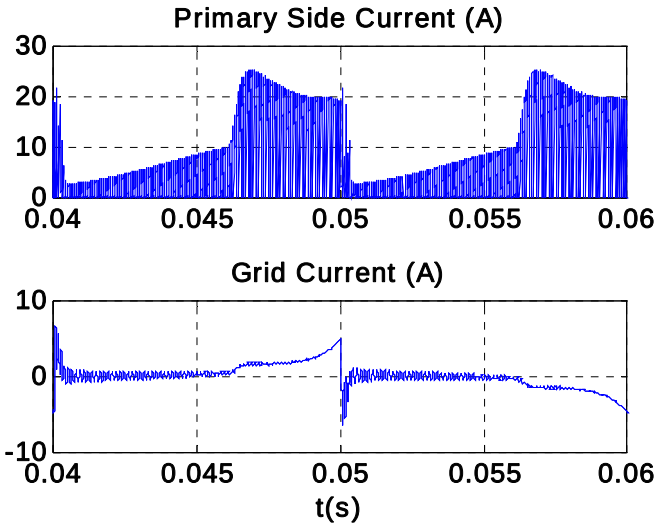


Fig.B. 8: Tacking Performance of the Secondary Side Current Control ($n = 4$, $L_m = 20\mu H$, V_{pv}=27V, V_{rms}=230V, 200W, Simulation)

In conclusion, for DACC scheme, the system operating point varies widely due to both the grid voltage variation over an AC period and to varying power levels due to irradiation changes, resulting in large changes in the RHP zero location. A controller designed to accommodate the worst case RHP zero, which occurs at the peak AC voltage under maximum power, was found to result in unacceptably low bandwidth (even lower than 100 Hz) when the operation changes to DCM under low instantaneous voltages during an AC cycle. Thus the widely varying RHP zero in CCM operation results in poor tracking performance in the DCM operating zones and hence unacceptable output power quality. Therefore, it was concluded that direct output current control using ACC is also not an option to perform the current shaping control.

Appendix C: Impedance Measurement and Loop Gain Tests

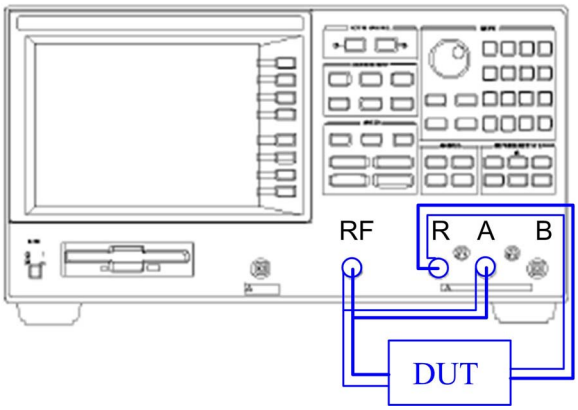
This appendix will discuss the test setup using Agilent 4295A for impedance measurement of the main passive components used in this thesis and for loop gain measurement of the flyback-CCM inverter in Chapter 4.

C.1 Impedance Measurement using Agilent 4395A

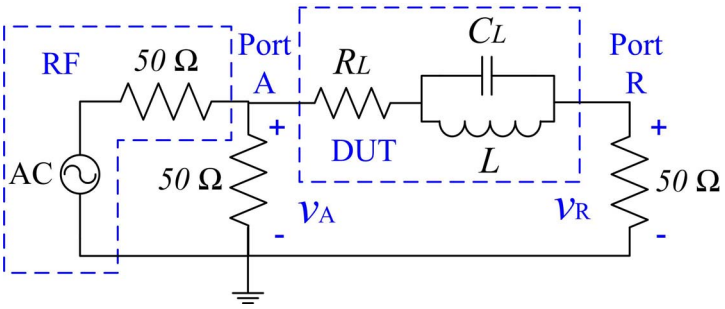
The purpose of the impedance measurement is to find out the parasitic components whose values will have significant influences on the plant transfer function and circuit operation.

Firstly, the test setup using Agilent 4395A and impedance calculation based on measurement results will be introduced. The test result of an inductor is given as an example.

C.1.1 Test Setup



a) Test Setup



b) Equivalent Circuit of Test Setup (DUT: inductor)

Fig.C. 9: Test setup for impedance measurement using 4395A

The test setup for impedance measurement (in the range of 10 kHz to 100 kHz) using Agilent 4395A is shown in Fig.C. 9 a), which is simple without extra component. The Port RF is terminated with Port A and the DUT (Device Under Test) is connected between Port A/RF and Port R.

It is noted that port RF, port A and port R are all ports with impedance of 50Ω. Therefore, the equivalent circuit of the test setup is illustrated in Fig.C. 9 b) and the impedance of the DUT can be obtained as:

$$Z_f = \frac{v_A - v_R}{v_R / 50} = 50 \cdot (\frac{v_A}{v_R} - 1) \qquad \text{(C-8)}$$

where, v_A and v_R correspond to the measurement results at port A and port R respectively.

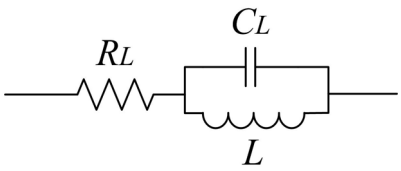
The reason why a NA (Network Analysis) mode is chosen rather than IA (Impedance analysis) mode for these measurements is that the frequency range of IA mode starts from 100kHz, which is higher than the targeted frequency range of plant transfer function.

In order to ensure measurement accuracy, the following guidelines should be followed:

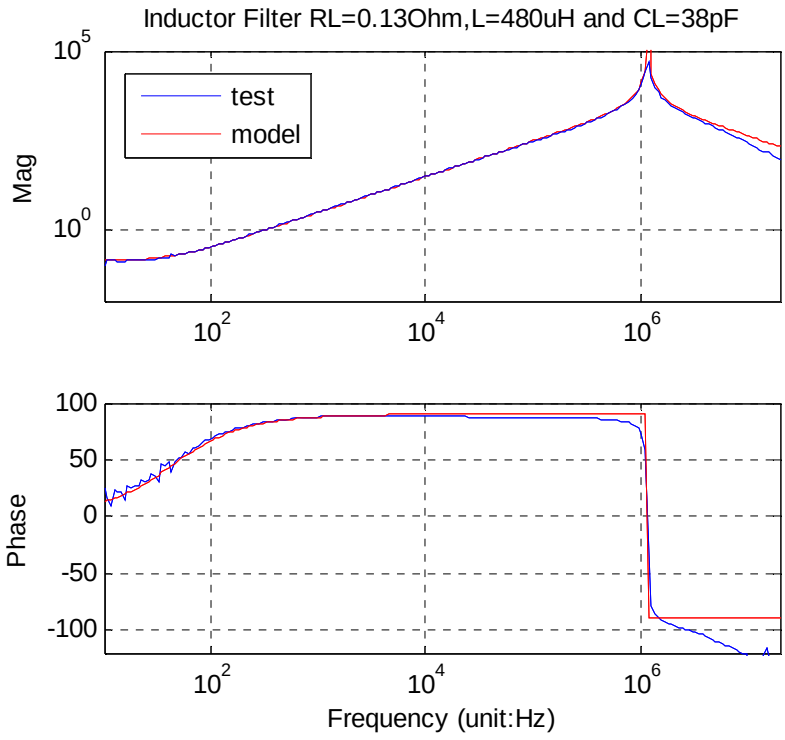
(1) Response calibration is needed every time before measurement.

(2) Change injection power by +-10dB and make sure the impedance curve does not change.

C.1.2 Test Examples



(a) Equivalent circuit of filter inductor



(b) Test result vs. model

Fig.C. 10: Impedance measurement and verification of filter inductor

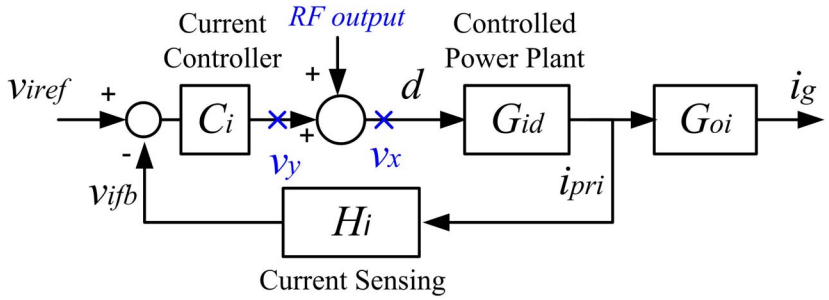
The impedance test of a filter inductor is given here as an example. As shown in Fig.C. 10, the parameters in the equivalent circuit of filter inductor can be derived from measurement result shown in Fig.C. 10 (b). Also included in Fig.C. 10 (b) is the calculated impedance model based on the derived parameters, which shows a good match with measurement result between 10 Hz~100 kHz (interested frequency range). The discrepancy at high frequency is not relevant in this study.

C.2 Loop Gain Test using Agilent 4395A

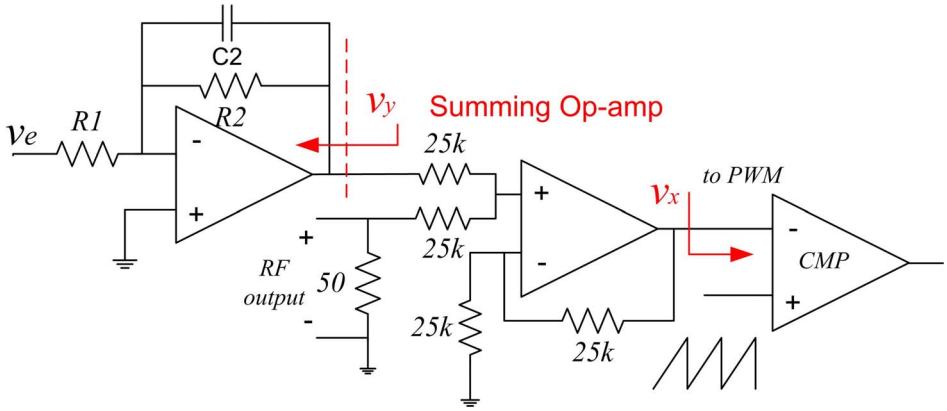
Measurement of loop gain requires injection of a disturbance signal into the close loop and measuring the ratio between the small signals at the input and output sides of the injection. The test setup using Agilent 4395A and test examples will be discussed in this part.

C.2.1 Test Setup

The injection point for flyback-CCM inverter studied in Chapter 4 is shown in Fig.C. 11 (a) . Here, a disturbance signal generated from Agilent 4395A RF port is summed with the controller output signal. The summation circuit using a differential opamp is illustrated in Fig.C. 11 (b). Here, it should be noted that the RF port has an output resistance of 50Ω, which makes the actual injected signal half of the value specified in the instrument. The loop gain can be represented by $\tilde{v}_y / \tilde{v}_x$ with the injected signal sweeping through a wide frequency range.

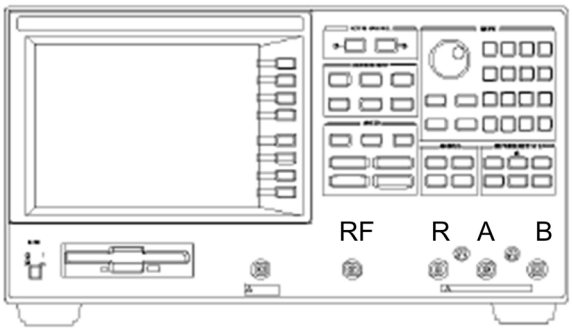


(a) Flyback-CCM Inverter system diagram and injection point

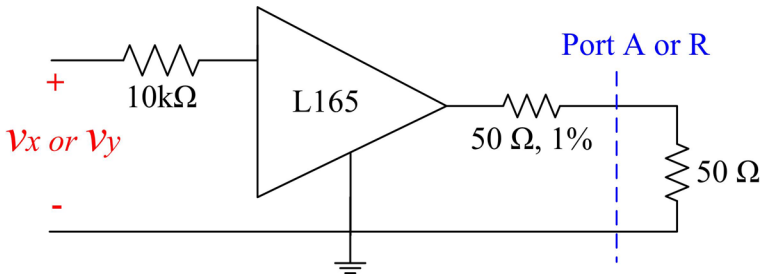


(b) Summation circuit using op-amp

Fig.C. 11: Disturbance injection for loop gain measurement



(a) Front panel of 4395A



(b) Voltage measurement using a self-made voltage follower

Fig.C. 12: Test setup for loop gain measurement

For loop gain measurement of switch mode power supply, a common practice is to use probes with a large impedance of 1MΩ in order not to interfere with the original circuit operation. However, as mentioned in impedance measurement, all the ports in Agilent 4395A (including RF, R, A and B ports shown in Fig.C. 12 (a)) are with a low impedance of 50 Ω, which tends to loading the circuit under test. In order to prevent this effect, an adapter for impedance conversion has been built and its circuit shown in Fig.C. 12 (b). This adapter works as a voltage follower. Its input impedance should be large to prevent loading the circuit under test and at the same time, it should be able to drive a low resistive load of 100Ω. Although most signal op-amps are able to meet the first requirement, they are usually not able to provide the large load driving capability, hence is not used in this circuit. Instead, a power amplifier L165 able to drive a load current up to 3A is used.

The waveforms of input signals v_x, v_y and its corresponding output signals v_R, v_A measured at port R and A are shown in Fig.C. 13. It is noticed that the output signal follows the input signals with half the amplitude.

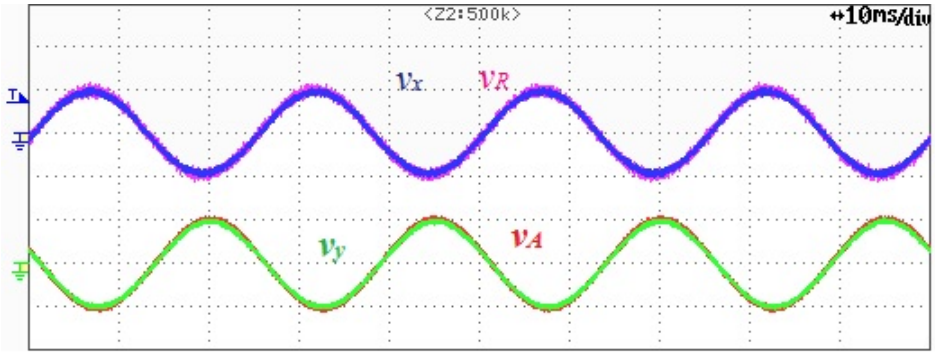


Fig.C. 13: Input and output waveforms of self-made adapter ($v_x[0.1V/div]$;

$v_R[50mV/div]$; $v_y[2V/div]$; $v_A[1V/div]$)

In order to ensure the accuracy of the test results, the guidelines given below should be followed:

(1) Perform response calibration every time before measurement;

(2) Monitor the time domain waveforms (such as Fig.C. 14 and the circuit operation waveforms in Fig.C. 14) to ensure the circuit operating in the desired mode. For example, the primary side current i_{pri} of flyback inverter in Fig.C. 14 already shows a DCM operation. Therefore, if the test purpose is to find out the loop gain in CCM operation, the magnitude of the disturbance signal should be set smaller in order to prevent the converter enters DCM operation.

(3) Change injection power and make sure the impedance curve does not change. This ensures that we are measuring strictly the linearized small signal transfer function.

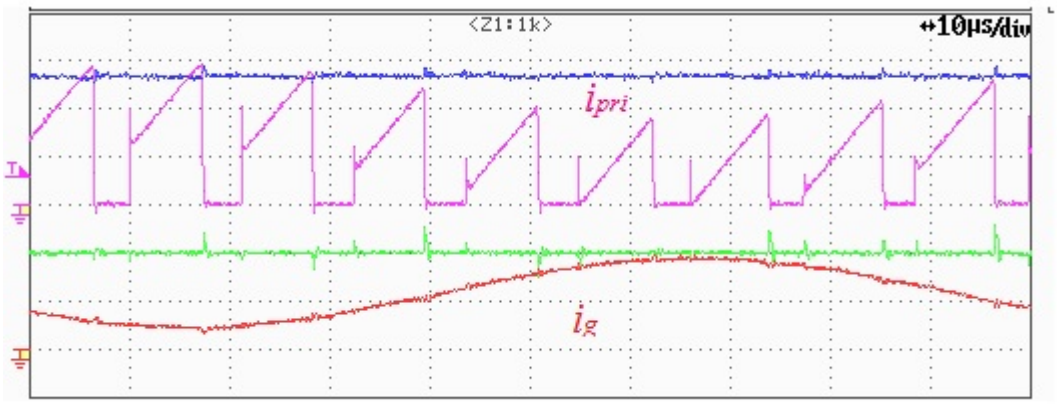


Fig.C. 14: Operation waveforms of the main circuit with injection of disturbance

C.2.2 Loop Gain Test of Flyback-CCM Inverter

As the loop gain of the designed inverter changes with the operating condition, we will measure it under different power levels P_{pv} and at varying instantaneous grid voltages V_g and compare them with theoretical predictions.

Since the test is based on DC-DC operation, and not for DC-AC operation, a conversion of test conditions is needed. As the designed inverter is designed for a full power level of 200W, the instantaneous transfer power will reach 400W at the AC peak conditions. If tested as a DC-DC at this power, the designed inverter may overheat. Therefore, the maximum operating power of the flyback-CCM inverter under DC-DC operation was limited to 200W and the DC output voltage (to represent the instantaneous grid voltage) was limited to below 200V in our test.

The loop gain measurements for two such quasi-steady state operating conditions at 200W are given here as examples. Table C. 1 compares the operating parameters both from theoretical calculations and from measurement results and also indicates the proper injection power from the RF port. The measured loop gains are compared with the theoretical model (theo-2 using equation (4-25)) and shown in Fig.C. 15 and Fig.C. 16.

Table C. 1: Quasi-steady state operating conditions ($V_{pv} = 27V$, $P_{pv} = 200W$)

V_g [V]	D		I_{pri} [A]		I_g [A]		Injection power from RF
	Cal.	Test	Cal.	Test	Cal.	Test	
150	0.58	0.58	3.15	3.2	0.567	0.52	-10dB
200	0.65	0.65	5.6	6.12	0.756	0.737	-10dB

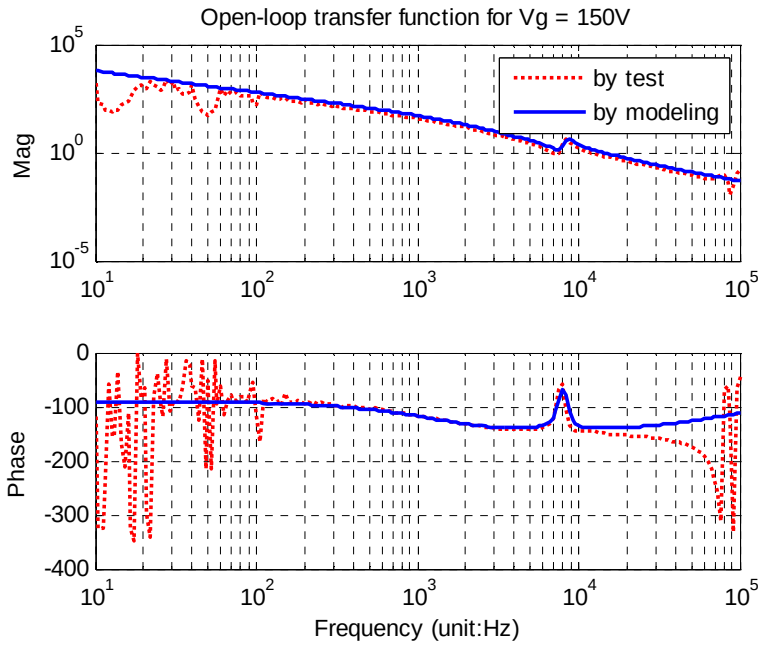


Fig.C. 15: Measured loop gain versus modeling using equation (4-25) (200W, $V_g = 150V$, $R_{Lm} = 0.25\Omega$)

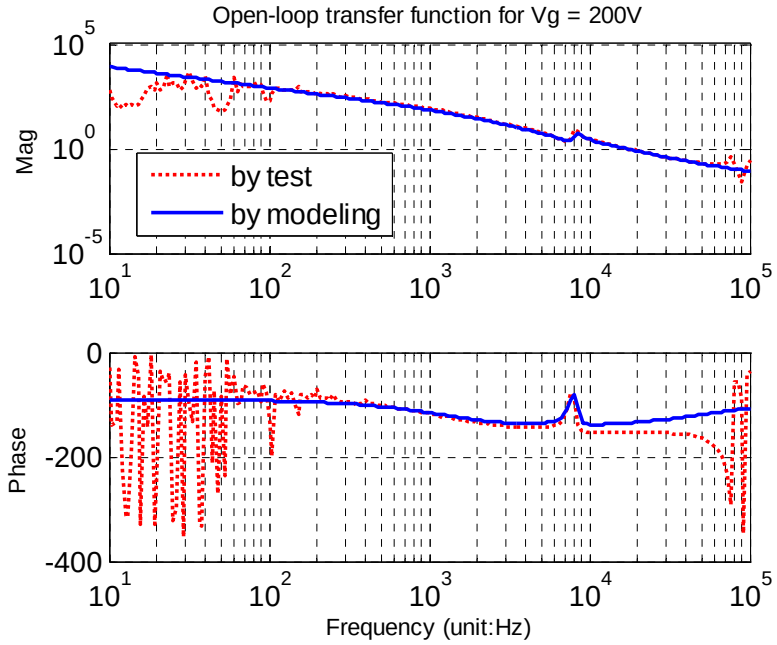


Fig.C. 16: Measured loop gain versus modeling using equation (4-25) (200W, $V_g = 200V$, $R_{Lm} = 0.25\Omega$)

As shown in Fig.C. 15 and Fig.C. 16, modeling using theo-2 model based on equation (4-25) agree with the test results in the frequency range of 100 ~ 10 kHz

(up to the system close-loop bandwidth). The variation of test results at low frequency is because the sweeping speed of the disturbance signal is too fast. To set the sweeping speed lower would eliminate the varying signal at low frequency as shown in Fig. 4.32, but would result in a very slow measurement. The test result at frequency range higher than the system bandwidth is due to limitations of the state space averaged modeling technique employed and is not of interest in our study.