EXTENDING SI CMOS: INGAAS AND GESN HIGH MOBILITY CHANNEL TRANSISTORS FOR FUTURE HIGH SPEED AND LOW POWER APPLICATIONS

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NOTIONAL UNIVERSITY OF SINGAPORE

2013

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HIGH MOBILITY CHANNEL TRANSISTORS

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LOW POWER APPLICATIONS

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A THESIS SUBMITTED

FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

NUS GRADUATE SCHOOL FOR INTEGRATIVE

SCIENCES AND ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2013

Declaration

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Gong Xiao / May 17 2013

Gong Xiao

Acknowledgements

This is perhaps the shortest but most important section of my thesis. First and foremost, I would like to express my earnest gratitude and appreciation to my research advisor, Dr. Yeo Yee Chia, for his encouragement, motivation, and trust throughout my graduate work. He has always been there to give insights into my research work, and I have greatly benefited from his vast knowledge and strong technical expertise. In addition, I have learnt from him how to achieve great things and be humble and nice at the same time. He is undoubtedly one of the most important and helpful people in my life. I am extremely fortunate to work with the finest advisor that one could possibly hope for.

I would like to thank Prof. Gengchiau Liang and Dr. Daniel Chua for serving as members of my Thesis Advisory Committee, and for their valuable guidance and suggestions during the course of my research work.

I am deeply grateful to Prof. Dimitri Antoniadis, who has been an excellent role model. Having discussion with him has been an extremely rewarding experience. He is always kind and generous in sharing his years of success and experience in the field of semiconductors and nanotechnology. This will be a continuous source of inspiration for me throughout my career. I am also grateful to Prof. Yoon Soon Fatt and Dr. Loke Wan Khai from Nanyang Technological University for valuable discussions on III-V epitaxy process.

I would like to thank Mr. Chum Chan Choy, Dr. Deng Jie, and Ms. Teo Siew Lang for their great help with my device fabrication work at the Institute of Materials Research and Engineering.

During my PhD, I have been very fortunate to interact with many outstanding researchers and graduate students in SNDL. Special thanks to Dr. Chin Hock Chun for mentoring me on fabrication and characterization of InGaAs transistors during the initial phase of my research. Special thanks also to Dr. Han Genquan for being a mentor, friend, and great supporter for my research. I enjoyed all the technical and nontechnical discussions we had. I would also like to thank Zhou Qian, Wang Wei, Samuel, Phyllis, Shao Ming, Ivana, Yang Yue, Pengfei, Liu Bin, Xingui, Huaxin, Xinke, Chunlei, Tong Yi, Zhu Zhu, Cheng Ran, Wenjuan, Lanxiang, Eugene, Tong Xin, Yinjie, Sujith, Bai Fan, Guo Cheng, Kain Lu, Kian Hui, Dong Yuan, Xu Xin, and many others. Thank you all for enriching my life and making my years at NUS very enjoyable. I would also like to thank the technical staff of SNDL, namely Mr. O Yan Wai Linn, Mr. Patrick Tang, and Ms. Yu Yi for their support and help.

No words can ever adequately express my deepest thanks and gratitude to my family. To my dad, mum, sister and brother-in-law, thank you for your continuous love, sacrifice, support, and encouragement that have allowed me to pursue my academic dreams. I am eternally grateful to you for being there for me at all times.

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Summary

Extending Si CMOS: InGaAs and GeSn High Mobilty Channel Transistors for Future High Speed and Low Power Logic Application

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As the semiconductor industry approaches the limits of traditional silicon CMOS scaling, the introduction of performance boosters such as novel materials and innovative device structures has become necessary for future high speed and low power logic applications. High mobility materials are being considered to replace Si as the channel materials, in order to achieve higher drive currents at lower operating voltages. In particular, InGaAs and Ge or GeSn have become of great interest due to their high electron and hole mobilities, respectively. This thesis work aims to address various challenges in taking full advantage of the high mobility channel materials for future CMOS logic applications.

For $In_{0.7}Ga_{0.3}As$ N-MOSFETs, a selective epitaxy process using MOCVD was first developed to grow a high quality InGaAs film. The process module was then integrated into a self-aligned gate-first process to fabricate the $In_{0.7}Ga_{0.3}As$ N-MOSFETs. Significant reduction in S/D series resistance was achieved due to

combined contributions from the high S/D doping concentration as well as the structural improvement arising from the raised S/D structure.

Next, the concept and demonstration of two novel surface passivation techniques were exploited to realize high-quality metal gate/high-*k* dielectric stacks on InGaAs: InP capping and low-temperature Si_2H_6 passivation. Introducing an InP capping layer in $In_{0.7}Ga_{0.3}As$ N-MOSFETs was found to reduce the subthreshold swing *S* and increase the drive current. Low-temperature Si_2H_6 passivation was developed to effectively passivate the $In_{0.7}Ga_{0.3}As$ surface, enabling the realization of $In_{0.7}Ga_{0.3}As$ N-MOSFETs with high drive current and *S* comparable to the best reported in the literature. Both interface engineering techniques are highly compatible with a matured high-*k* dielectric deposition process, and provide promising options for interface passivation to exploit the full potential of InGaAs N-MOSFETs.

For GeSn P-MOSFETs, low-temperature Si_2H_6 passivation was first developed to realize a high quality interface between the high-*k* dielectric and the GeSn, as well as excellent transistor NBTI reliability. For the first time, a common gate stack technology comprising 370 ºC Si_2H_6 passivation and TaN/HfO_2 gate stack was proposed and demonstrated for InGaAs and GeSn CMOS devices for cost-effective integration.

Two approaches to further enhance the drive current of GeSn P-MOSFETs were then explored: choice of surface orientation and channel length scaling. The world's first short-channel GeSn P-MOSFETs with self-aligned NiGeSn metal S/D were realized using a gate-first process.

In addition, the uniaxially compressive strained GeSn gate-all-around nanowire (NW) P-MOSFETs with the shortest reported channel length down to 100 nm were demonstrated for the first time using a CMOS-compatible top-down approach. This device structure takes advantage of uniaxial compressive strain for mobility enhancement by etching NWs from a biaxially strained layer, as well as a 3D device architecture for control of short channel effects at extremely scaled dimensions. The GeSn NW formation technology shows promise for integration in future high performance GeSn P-MOSFETs.

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List of Symbols

Symbol	Description	Unit
A_G	Gate area	μm^2
C_D	Depletion capacitance	F
C_{it}	Capacitance due to interface traps	F
C_{ox}	Gate oxide capacitance	F
D_{it}	Interface trap density	$cm^{-2}\cdot eV^{-1}$
E_A	Activation energy	eV
E_{CNL}	Charge neutrality level	eV
E_F	Fermi level	eV
E_G	Bandgap	eV
E_C	Conduction band edge	eV
ΔE_C	Conduction band offset	eV
E_V	Valence band edge	eV
ΔE_V	Valence band offset	eV
E_{ox}	Oxide electric field	V/cm
f	Frequency	Hz
G_D	Drain conductance	S
$G_{m,ext}$	Extrinsic transconductance	S
$G_{m,int}$	Intrinsic transconductance	S
$G_{M, Lin}$	Transconductance at linear region	S
h	Planck's constant	eV·s
I_{CP}	Charge pumping current	A
I_D	Drive current (per unit width)	μA/μm

$I_{D,lin}$	Drain current at liner region (per unit width)	µA/µm
I_{Dsat}	Saturation current (per unit width)	µA/µm
I_{ON}	On-state current (per unit width)	µA/µm
I_{OFF}	Off-state current (per unit width)	A/µm
I_S	Souce current (per unit width)	A/µm
J_{G}	Gate leakage current density	A/cm^2
k	Boltzman's constant	eV/K
L	Contact length	µm
L_{G}	Gate length	nm
L_T	Transfer length	µm
L_{CH}	Channel Length	nm
L_{SD}	Separation between S/D and channel edge	µm
m_n^*	Effective mass	kg
n	Time exponent	s
n_i	Intrinsic carrier concentraion	cm^{-3}
n_s	Surface concentraction of minority carriers	cm^{-3}
N_A	Hole concentration	cm^{-3}
N_D	Electron concentration	cm^{-3}
N_{inv}	Inversion carrier density	cm^{-3}
$N_{D,Imp}$	Active doping concentration achieved by implantation and anneal	cm^{-3}
$N_{D,Raised}$	Active doping concentration achieved by *in situ* doping	cm^{-3}
q	Electronic charge	C
Q_{inv}	Inversion charge density	C/cm^2

Q_f	Fixed charge density	C/cm^2
Q_{ox}	positive oxide charge density	C/cm^2
Q_S	Semiconductor charge density	C/cm^2
R_C	Contact resistance	KΩ·μm
R_{CH}	Channel resistance	KΩ·μm
$R_{S,Co}$	Contact resistance between the metal and the implantation-doped source	KΩ·μm
$R'_{S,Co}$	Contact resistance between the metal and the *in situ* doped raised source	KΩ·μm
$R_{S,Imp}$	Resistance of the implantation-doped source	KΩ·μm
R_{SE}	Source extension resistance	KΩ·μm
$R_{S,Raised}$	Resistance of the *in situ* doped raised source region	KΩ·μm
$R_{S,Total}$	Total Source resistance	KΩ·μm
R_{SD}	Source/drain series resistance	KΩ·μm
R_{sh}	Sheet resistance	Ω/square
R_{Total}	Total resistance	KΩ·μm
S	Subthreshold swing	mV/decade
t_f	Trapezoidal pulse fall time	ns
t_r	Trapezoidal pulse rise time	ns
t	Time	s
T	Temperature	°C
T_{xx}	Stress in *X* direction	N
V_A	Amplitude of trapezoidal pulse	V
V_{FB}	Flatband voltage	V
V_G	Gate voltage	V
V_t	Thermal voltage	V

V_{TH}	Threshold voltage	V
ΔV_{TH}	Threshold voltage shift	V
W_{eff}	Gate or channel width	μm
X_J	Implantation junction depth	nm
X_{Raised}	Height of the raised source	nm
ρ_C	Specific contact resistivity	$\Omega \cdot cm^2$
ρ_{imp}	Resistivity of the implantation-doped source	KΩ·cm
ρ_{Raised}	Resistivity of the *in situ* doped source	KΩ·cm
μ_{eff}	Effective mobility	$cm^2/V \cdot s$
μ_e	Electron mobility	$cm^2/V \cdot s$
μ_h	Hole mobility	$cm^2/V \cdot s$
ϕ_{Bn}	Electron Schottky barrier height	eV
r_c	Backscattering coefficient	
υ_{inj}	Thermal injection velocity	$cm \cdot s^{-1}$
υ_{th}	Thermal velocity	$cm \cdot s^{-1}$
Φ_F	Fermi potential	V
Φ_M	Metal work function	V
Φ_{MS}	Work function difference between metal and semicondcutor	eV
ε_s	Permittivity	F/m
σ_n	Capture cross sections of electrons	cm^2
σ_h	Capture cross sections of holes	cm^2
χ	Electron affinity	eV

Chapter 1

Introduction

1.1 Background

Over the past few decades, complementary metal-oxide-semiconductor (CMOS) technology based on Si has been driven by Moore's Law, i.e. device scaling to enhance performance, increase device density, and reduce cost and power consumption [1]. However, as the gate length L_G of the metal-oxide-semiconductor field-effect-transistor (MOSFET) scales beyond the 90 nm node, the performance gain using the traditional way of scaling becomes more and more difficult. The aggressively scaled gate dielectric sandwiched between the polysilicon (poly-Si) gate and the channel leads to higher and higher gate leakage current. As a result, novel technologies were explored to further enhance the device drive current. Fig. 1.1 shows the manufacturing-development-research pipeline for CMOS technology.

At the 90 nm technology node, SiGe source/drain (S/D) was introduced to induce uniaxial compressive strain in the Si channel of p-channel metal-oxide-semiconductor field-effect-transistors (P-MOSFETs) [2]. This changes the band structure of Si so that the hole mobility in the transport direction is improved. Since then, strain engineering has been adopted by Intel and other companies as an additional performance booster to further extend the CMOS roadmap below the 90 nm node [2]-[12]. At the 45 nm technology node, high-*k* materials were first introduced to replace SiO_2 as the gate dielectric to achieve higher capacitance and

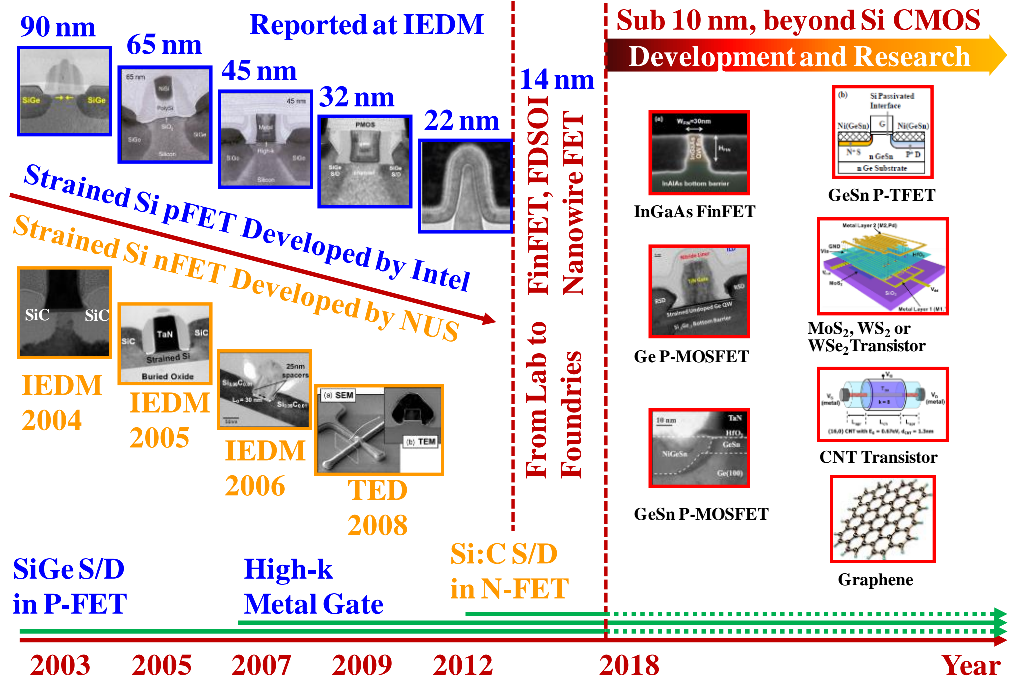


Fig. 1.1. Transistor scaling and manufacturing-development-research pipeline of CMOS technology.

reduce gate leakage current. In addition, metal gate was introduced to replace poly-Si gate to avoid the poly-Si depletion problem for small equivalent oxide thickness (CET) [13].

Although strain engineering has been able to provide the required performance boost after the 90 nm technology node, the continuous scaling of device dimensions and gate pitch pose new challenges to the conventional techniques and materials used for CMOS strain engineering, especially when the technology node reaches 11 nm and beyond [12]. Therefore, the advancement of future CMOS technology will rely increasingly on the innovative employment of materials, processes, and device architectures.

1.2 High Mobility Channel Materials for Future CMOS Applications

When the MOSFET is scaled down to the deep sub-100 nm regime, carrier transport in the extremely scaled device becomes quasi-ballistic. It has been theoretically and experimentally [14]-[17] shown that low-field mobility can still be a good indicator for the current drive in ultra-short-channel MOSFETs, where ballistic or quasi-ballistic transport, rather than saturation velocity, is important.

The drive current of a device operating in the quasi-ballistic regime is limited by the thermal injection velocity [15]-[16], instead of the saturation velocity which determines the performance of a long-channel device. The saturation current of a short channel device can be expressed as

$$I_{Dsat} = C_{ox} W_{eff} \upsilon_{inj} \left(\frac{1-r_c}{1+r_c}\right)(V_{GS} - V_{TH}), \tag{1.1}$$

where C_{ox} is the gate oxide capacitance, W_{eff} is the effective gate width, r_c is the backscattering coefficient which indicates the number of carriers backscattered to the source, V_{GS} is the voltage between the gate and the source, V_{TH} is the threshold voltage, and υ_{inj} is the thermal injection velocity. Experimentally, it was found that υ_{inj} is dependent on low-field mobility, while r_c is inversely proportional to low-field mobility [16]-[17]. For extremely scaled devices operating in the full ballistic regime, r_c is equal to zero. Therefore, incorporating channel materials with higher low-field mobility would achieve higher injection velocity near the source region of a transistor. This could lead to enhanced carrier transport, higher drive current, and shorter transistor delay.

Table 1.1. Key parameters of possible channel materials for future CMOS applications [18]

	Si	Ge	GaAs	InAs	InSb
Band gap (eV)	1.11	0.67	1.43	0.354	0.17
Electron mobility (cm^2/V·s)	1350	3900	8500	40000	77000
Hole mobility (cm^2/V·s)	480	1900	400	500	850
Dielectric constant	11.8	16	12.4	14.8	17.7
Lattice constant (Å)	5.43	5.66	5.65	6.06	6.48

Based on the information in Table 1.1, materials that have the potential to replace Si as the channel material for future high-speed and low-power logic applications can basically be grouped to give three promising options.

The first option is Ge or GeSn alloy for both N-MOSFETs and P-MOSFETs. Ge has substantially higher bulk electron and hole mobilities, approximately two and four times higher than those of Si, respectively. Very good progress has been made in realizing high-performance Ge P-MOSFETs [19]-[26]. Recently, GeSn channel P-MOSFETs were experimentally demonstrated to have higher hole mobility than Ge channel P-MOSFETs [27]-[29]. Simulation results also show that incorporation of Sn into Ge leads to an improvement in electron injection velocity for GeSn channel N-MSOFETs [30]. Ge or GeSn have an advantage over III-V compound semiconductors in terms of process compatibility and easy integration with Si technology. Integrating Ge or GeSn as the channel material in the current CMOS technology would be more straightforward, considering that SiGe has already been

integrated into the S/D regions of current MOSFETs. However, the electron mobility reported in Ge or GeSn N-MOSFETs is still lower than in strained Si N-MOSFETs despite the high electron mobility in bulk Ge or GeSn [30]-[39]. In addition, formation of very low resistance S/D is also very challenging for Ge or GeSn N-MOSFETs. Therefore, the drive current of the Ge or GeSn N-MOSFETs needs substantial improvement for them to be attractive.

The second option is III-V compound semiconductors for both N-MOSFETs and P-MOSFETs. III-V materials, such as As-based or Sb-based compound semiconductors, are particularly attractive for N-MOSFETs due to their very high electron mobility. In fact, high-performance devices based on III-V materials, such as high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs), have been widely used in communications products for many years. However, due to the lack of a thermally stable and high-quality gate stack, III-V-based MOSFET was demonstrated only a decade ago. Since then, extensive efforts and significant progress have been made in the development of III-V N-MOSFETs [40]-[50]. However, As-based compound semiconductors have hole mobilities similar to that of Si, which offers no advantage over Si for P-MOSFETs. Sb-based compound semiconductors offer the highest hole mobilities among all III-V semiconductor materials. Recently, peak hole mobilities of 620 and 910 $cm^2/V\cdot s$ were realized in surface and buried channel InGaSb P-MOSFETs, respectively [51]. However, these values are still much smaller than that of strained Ge P-MOSFETs, which can be as high as 1490 $cm^2/V\cdot s$ [52]. In addition, realizing nanoscale III-V transistors on a Si platform has many process, integration, and cost problems which

may not have an easy solution. The success of any future CMOS technology will depend on its compatibility with the existing Si manufacturing infrastructure. The huge lattice mismatch between As-based or Sb-based compound semiconductors and Si makes it very challenging to integrate them on Si-based substrates with controllable strain levels and acceptable defect density.

The third option is III-V semiconductor for N-MOSFETs and Ge or GeSn alloy for P-MOSFETs. Based on the discussion of the previous two options, As-based or Sb-based compound semiconductors for N-MOSFETs and Ge or GeSn alloy for P-MOSFETs seem to be the most promising combination despite the fact that integrating these two strong contenders under a conventional CMOS process could further complicate the integration and cost issues. Shown in Fig. 1.2 is a simple schematic of an ultimate CMOS using InGaAs N-MOSFET and Ge or GeSn P-MOSFET. The objective of this thesis is to address some of the key front-end issues and develop various advanced technologies to unleash the potential of InGaAs and GeSn high-mobility channel materials for high drive current at scaled supply voltage.

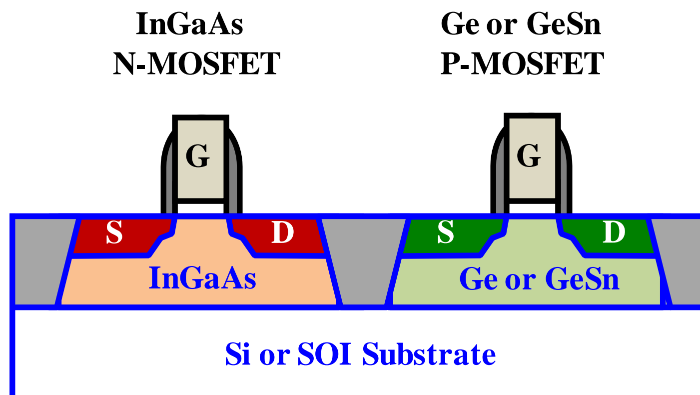


Fig. 1.2. Schematic of an ultimate CMOS structure using InGaAs N-MOSFET and Ge or GeSn P-MOSFET.

1.3 Key Challenges and Issues to Be Addressed for InGaAs N-MOSFETs and GeSn P-MOSFETs

1.3.1 Formation of Low Resistance S/D Regions

The S/D regions of conventional Si MOSFETs are formed by ion implantation, followed by dopant activation anneal. High doping concentration in the S/D reduces series resistance, leading to higher drain current. In III-V materials, such as GaAs and InGaAs, Si is the preferred impurity for obtaining N-type doping due to its moderately low dopant activation temperature, thermal stability, and low diffusivity. However, doping the InGaAs S/D regions by Si implantation and anneal does not achieve sufficiently high doping concentration (i.e. higher than 5×10^{19} cm^{-3}). This is due to the Si solid solubility limit at ~8×10^{18} cm^{-3} [53]. Such a low doping level leads to high S/D series resistance and further limits the S/D junction depth scaling for better control of short channel effects. Although Si and P co-implantation was found to enhance the activation efficiency of the implanted Si in GaAs by 50% [54], the active doping concentration achieved is still not high enough for high-performance InGaAs N-MOSFETs [55]. Other innovative solutions are necessary to boost the S/D doping level to address the S/D series resistance issues.

1.3.2 Formation of High-Quality Gate Stack for InGaAs N-MOSFETs

To realize high-performance InGaAs N-MOSFETs, a high-quality and thermodynamically stable gate stack on InGaAs is needed. When a III-V surface is oxidized, a high density of interface states can be generated, which may cause Fermi-level pinning, increase the subthreshold swing, degrade the electron mobility, and create reliability issues. Gate dielectrics on InGaAs channel have been extensively

investigated, most of which involve high-*k* dielectric formed directly on the InGaAs channel. This usually leads to a high density of interface traps between the high-*k* dielectric and the InGaAs, resulting in significant carrier scattering and mobility degradation [56]. One strategy to mitigate the various interface states between the high-*k* dielectric and the InGaAs surface is to bury the channel beneath a large band gap material to reduce Coulombic scattering from the charged interface and bulk oxide states, as well as remote phonon scattering from oxide phonons.

1.3.3 Formation of High-Quality Gate Stack for GeSn P-MOSFETs

As with InGaAs, one of the most critical issues for Ge P-MOSFETs is the poor quality of the native oxide compared to SiO_2 on Si, which leads to rapid degradation in mobility with decreasing electrical oxide thickness. The solution to solve the problem is to create a high-quality interfacial layer with low interface state density between the gate dielectric and the Ge. The use of a thin Si cap is the most mature of the technologies under investigation, with significant progress over the last decade [57] and particularly in recent times [58]-[60].

Although GeSn has been shown to achieve enhanced hole mobility over Ge, the Sn was found to be segregated to the surface even right after the MBE GeSn growth at a high growth temperature [61]. The situation could be worsened by high process temperatures during the fabrication of GeSn MOSFETs. Segregation of Sn at the high-*k*/GeSn interface would degrade the interface quality between the high-*k* dielectric and the GeSn. This necessitates the use of a low thermal budget process to realize a high quality and thermodynamically stable high-*k*/GeSn interface for transistor fabrication.

1.3.4 Surface Orientation Study for GeSn P-MOSFETs

Use of various surface and channel orientations has been extensively studied in Si CMOS to optimize transistor performance. The introduction of novel device structures, (i. e. FinFETs) enables the transistors to be fabricated on (110) and (111) crystal orientations. Significant hole mobility enhancement of ~160% has been observed for transistors made on a (110)-oriented surface compared to those on a (100)-oriented surface, for both oxynitride and HfO_2 gate dielectrics [62]. It was also found that the low-field electron mobility of N-MOSFETs on (111) substrate is smaller than that on (100) substrate, and the low-field hole mobility of P-MOSFETs on (111) substrate is larger than that on (100) substrate [63]. The dependence of electron mobility on strain, channel direction and substrate orientation were studied for Ge N-MOSFETs [64]. The electron mobility of (111)-oriented Ge N-MOSFETs was calculated to be the highest, and the mobility can be enhanced further by introducing tensile strain into the Ge channel. Experimental results also demonstrate a 50% improvement in electron mobility for (111) substrate orientation compared to (100) orientation [65].

However, all reported GeSn channel N- and P-MOSFETs have so far been for (100) surface orientation [27]-[30],[39]. To explore the full potential of GeSn as a channel material for MOSFET application, it is necessary to investigate the performance of GeSn MOSFETs with other surface orientations.

1.3.5 Fabrication of Multi-Gate GeSn P-MOSFETs

The larger permittivity of InGaAs and GeSn compared to Si leads to lower immunity to short-channel effects. As Si CMOS manufacturing enters a new era with

the "tri-gate" design at the 22 nm node [66], a similar non-planar 3D approach needs to be explored for extremely scaled MOSFETs using InGaAs and GeSn. InGaAs N-MOSFETs [67]-[70] and Ge P-MOSFETs [71]-[77] with 3D structures have been extensively explored recently, with very promising results achieved. However, there has been no report of GeSn P-MOSFETs with similar advanced structures.

In addition, the hole mobility of GeSn is boosted by biaxial compressive strain. Uniaxial compressive strain has recently been experimentally shown to be even more effective in enhancing the hole mobility of Ge than biaxial compressive strain, and this was achieved by nanowire (NW) formation from biaxially strained Ge [77]. The ability to obtain uniaxial compressive strain by etching NWs from a biaxially strained layer, together with the need for 3D device architectures for control of SCEs at extremely scaled dimensions [78], makes it particularly attractive to form short channel GeSn NW P-MOSFETs from biaxially strained GeSn.

1.4 Thesis Outline

The main technical contents discussed in this thesis are documented in five chapters.

In Chapter 2 of this thesis, we report the demonstration of R_{SD} reduction in $In_{0.7}Ga_{0.3}As$ N-MOSFETs by *in situ* SiH_4 doping during the selective epitaxial growth of $In_{0.53}Ga_{0.47}As$ to form the heavily doped raised S/D regions. A selective epitaxy process was first developed, and then integrated into a self-aligned gate-first process to fabricate the $In_{0.7}Ga_{0.3}As$ N-MOSFETs. Significant R_{SD} reduction was achieved due to the combined contributions from the higher S/D doping concentration as well as the raised S/D structure.

In Chapter 3, two advanced technology schemes were explored to realize high-quality gate stack for $In_{0.7}Ga_{0.3}As$ N-MOSFETs. Section 3.2 discusses the realization of InP-capped $In_{0.7}Ga_{0.3}As$ N-MOSFETs formed using a gate first process, in which self-aligned implant and anneal were used to form the S/D regions. The dependence of the electrical characteristics of the transistors on the thickness of the InP cap is investigated. Section 3.3 investigates a low-temperature Si_2H_6 passivation technique, which forms an ultra-thin SiO_2/Si interfacial layer between the high-*k* dielectric and the $In_{0.7}Ga_{0.3}As$ channel.

In Chapter 4, we first investigate and compare the dependence of the electrical characteristics of (100)-oriented $Ge_{0.958}Sn_{0.042}$ P-MOSFETs on different surface passivation techniques (low-temperature Si_2H_6 passivation or room temperature $(NH_4)_2S$ treatment of GeSn) prior to HfO_2 deposition. The negative bias temperature instability (NBTI) of Si_2H_6-passivated GeSn P-MOSFETs is examined. For cost-effective integration in CMOS fabrication, a common gate stack solution for GeSn and InGaAs CMOS is then explored.

Chapter 5 investigates the dependence of the carrier mobility and drive current of $Ge_{0.958}Sn_{0.042}$ P-MOSFETs on surface orientation. Fabrication and characterization of the world's first short-channel $Ge_{0.95}Sn_{0.05}$ P-MOSFETs with L_G down to 200 nm are then discussed.

Chapter 6 discusses the realization of the first uniaxially compressive strained GeSn gate-all-around (GAA) NW P-MOSFETs using a fully CMOS-compatible top-down fabrication process. A novel H_2O_2-based wet etch is developed to realize GeSn NWs. SF_6 treatment and low-temperature Si_2H_6 passivation are used to passivate the

GeSn NWs to achieve a good interface between the high-*k* dielectric and the GeSn channel. The process modules are integrated in a GeSn NW GAA P-MOSFET fabrication flow to realize channel lengths down to 100 nm.

The thesis ends with an overall conclusion and possible future research directions in Chapter 7.

Chapter 2

Source/Drain Engineering for $In_{0.7}Ga_{0.3}As$ N-Channel Metal-Oxide-Semiconductor Field Effect Transistors: Raised Source/Drain with *In Situ* Doping for Series Resistance Reduction

2.1 Introduction

New materials and novel device architectures are needed to extend the performance limits of complementary metal-oxide-semiconductor (CMOS) technology. III-V compound semiconductors such as indium gallium arsenide (InGaAs) have very high electron mobility and are attractive candidates to replace strained Si channel for n-channel metal-oxide-semiconductor field-effect transistors (N-MOSFETs) beyond the 11 nm technology node [42]-[43]. Recent research on InGaAs N-MOSFETs has focused on gate stack and interface engineering, with very promising results obtained [44]-[50],[79]-[89]. To harness the full potential of InGaAs N-MOSFETs, S/D engineering is also an important direction.

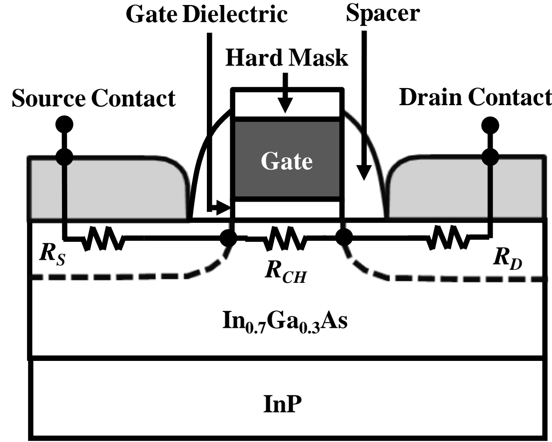


Fig. 2.1. Schematic illustration of the channel resistance (R_{CH}) and the source/drain resistance (R_{SD}) of a transistor in the linear region. The total resistance (R_{Total}) between the source contact and drain contact of the transistor is the summation of these resistance components. The introduction of high mobility InGaAs channel reduces R_{CH}. For further enhancement of drive current, S/D engineering to reduce R_{SD} is also important.

Source/drain (S/D) series resistance R_{SD} can be a performance-limiting factor in CMOS devices with sub-30 nm gate length L_G. As shown in Fig. 2.1, in addition to the channel resistance R_{CH}, the drain current of a transistor is also determined by R_{SD}. The combination of these two resistance components constitute to the total resistance R_{Total} between the source and drain contacts of a transistor in the linear region, which is given by

$$R_{Total} = R_{CH} + R_{SD}. \tag{2.1}$$

In MOSFETs with aggressively scaled L_G and high channel mobility, the channel resistance R_{CH} would be small so that R_{SD} is an important component of the total resistance between source and drain. A higher S/D doping concentration leads to a lower S/D series resistance and higher drive current. Doping InGaAs S/D

regions by Si implantation and anneal does not achieve sufficiently high doping concentration, i.e. higher than 5×10^{19} cm^{-3}. This is due to the saturation of the Si donor solubility at ~8×10^{18} cm^{-3} [53]. Although the Si and P co-implantation was found to enhance the activation efficiency of the implanted Si in GaAs by 50% [54], the active doping concentration achieved is still not high enough for high performance InGaAs N-MOSFETs [55].

InGaAs MOSFETs with raised S/D formed by regrowth by molecular beam epitaxy (MBE) were reported in [90],[91]. InP/InGaAs composite channel MOSFETs with selectively regrown n^+ S/D regions by metal organic vapor-phase epitaxy (MOVPE) were also demonstrated in [92],[93], where a gate-last process was adopted. Active Si doping concentration as high as ~5×10^{19} cm^{-3} was achieved by epitaxial growth with *in situ* doping. In Refs. [90]-[93], the indium composition x in the $In_xGa_{1-x}As$ channel is below 0.7. A higer x in $In_xGa_{1-x}As$ can lead to an increase in bulk mobility, thus increasing the N-MOSFET drive current.

In this Chapter, we report the demonstration of R_{SD} reduction in $In_{0.7}Ga_{0.3}As$ N-MOSFETs by *in situ* SiH_4 doping during the selective epitaxy of $In_{0.53}Ga_{0.47}As$ to form the heavily doped raised S/D regions. Si doping concentration of ~4×10^{19} cm^{-3} was achieved. In addition, a raised S/D structure was realized. A self-aligned gate-first process was utilized to fabricate the InGaAs MOSFETs. By integrating the raised S/D structure into an $In_{0.7}Ga_{0.3}As$ N-MOSFET, significant R_{SD} reduction and drive current improvement were demonstrated. Current-voltage characteristics, transconductance, S/D series resistance, and on- and off- state currents of $In_{0.7}Ga_{0.3}As$ N-MOSFETs were studied in detail. Part of this work was published in Ref. [93].

2.2 Design Concept

Fig. 2.2 shows schematics of the source regions of two MOSFET designs, without [Fig. 2.2 (a)] and with [Fig. 2.2 (b)] *in situ* doped raised source. For the transistor without raised source, the total source resistance is

$$R_{S,Total} = R_{SE} + R_{S,Imp} + R_{S,Co}, \tag{2.2}$$

where R_{SE} is source extension resistance, $R_{S,Imp}$ is the resistance of the implantation-doped source, and $R_{S,Co}$ is the contact resistance between the metal and the implantation-doped source.

For the transistor with raised source, the total source resistance is given by

$$R'_{S,Total} = R_{SE} + R_{S,Imp}//R_{S,Raised} + R'_{S,Co}, \tag{2.3}$$

where $R_{S,Raised}$ is the resistance of the *in situ* doped raised source region, and $R'_{S,Co}$ is the contact resistance between the metal and the *in situ* doped raised source region.

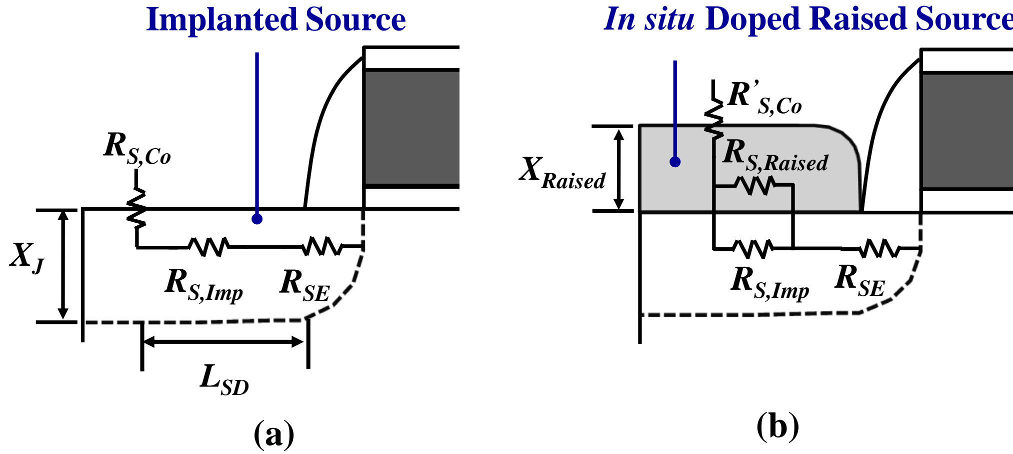


Fig. 2.2. Schematics of the source region of MOSFETs, (a) without *in situ* doped raised source, and (b) with *in situ* doped raised source. The dashed line represents the source-channel n^+/p junction.

First, assuming an ideal box-like doping profile, $R_{S,Imp}$ can be expressed as [94].

$$R_{S,Imp} = \frac{\rho_{Imp} L_{SD}}{W_{eff} X_J}, \tag{2.4}$$

where L_{SD} is the separation between the S/D and channel edge, W_{eff} is the transistor width, X_J is the implantation junction depth, ρ_{Imp} is the resistivity of the implantation-doped source, and is given by

$$\rho_{Imp} = \frac{1}{N_{D,Imp} q \mu_e}, \tag{2.5}$$

where $N_{D,Imp}$ is the active doping concentration achieved by implantation and anneal, and μ_e is the electron mobility.

$R_{S,Raised}$ can be expressed as

$$R_{S,Raised} = \frac{\rho_{Raised} L_{SD}}{W_{eff} X_{Raised}}, \tag{2.6}$$

where X_{Raised} is the height of the raised source, ρ_{Raised} is the resistivity of the *in situ* doped source, and is given by

$$\rho_{Raised} = \frac{1}{N_{D,Raised} q \mu_e}, \tag{2.7}$$

where $N_{D,Raised}$ is the active doping concentration achieved by *in situ* doping.

With introduction of the *in situ* doped source, much larger $N_{D,Raised}$ than $N_{D,Imp}$ can be obtained. Furthermore, a raised structure introduces an additional conducting path parallel to the implanted region. Thus, the resistance can be much smaller than that of the transistor without the raised *in situ* doped source.

Second, the contact resistance R_C between metal and semiconductor depends on the specific contact resistivity ρ_C, the sheet resistance R_{sh}, the transistor width W_{eff}, the length L of the contact hole, and the transfer length L_T. R_C is given by [95]

$$R_C = \frac{\sqrt{\rho_C R_{sh}}}{W_{eff}} \coth(\frac{L}{L_T}) . \tag{2.8}$$

For a metal-semiconductor junction with a high impurity doping concentration, the tunneling process would dominate, and ρ_C is found to be [95]

$$\rho_C \sim e^{\frac{4\pi\sqrt{\varepsilon_s m_n^*}}{h}\frac{\phi_{Bn}}{\sqrt{N_D}}} , \tag{2.9}$$

where ε_s is the permittivity of the semiconductor, m_n^* is the electron effective mass, ϕ_{Bn} is the electron Schottky barrier height, h is Planck's constant, and N_D is the semiconductor doping concentration. It is obvious that R_C is a strong function of N_D. With *in situ* doped source, which has much larger active doping concentration ($N_{D,Raised} >> N_{D,Imp}$), smaller $R'_{S,Co}$ than $R_{S,Co}$ can be achieved.

2.3 Process Development and Device Fabrication

2.3.1 Selective Epitaxy of *In situ* Doped Raised S/D

The key process step or module in the transistor fabrication of this research effort is the selective growth of *in situ* doped $In_yGa_{1-y}As$ by metal organic chemical vapor deposition (MOCVD). The indium composition y in the MOCVD grown $In_yGa_{1-y}As$ is generally different from that of the channel material, because with a smaller y in the epitaxial $In_yGa_{1-y}As$ as compared with that in the channel, the uniaxial tensile strain can be introduced in the channel to enhance the drive current. To obtain the optimal process conditions for the selective growth of $In_{0.53}Ga_{0.47}As$ on $In_{0.7}Ga_{0.3}As$, the initial development was performed to grow $In_{0.4}Ga_{0.6}As$ on $In_{0.53}Ga_{0.47}As$. We found that indium composition y and growth temperature are two important factors affecting the selective epitaxy of InGaAs raised S/D regions.

When the indium composition is low, undesirable three-dimensional growth of InGaAs dots on S/D regions was formed due to huge lattice mismatch with $In_{0.53}Ga_{0.47}As$ [Fig. 2.3 (b)]. The islanding process relieves the stress accumulated at the $In_yGa_{1-y}As$/ $In_xGa_{1-x}As$ heterojunction. When indium composition is increased or lattice mismatch is reduced, two-dimensional growth mode becomes the dominant mechanism [Fig. 2.3 (c)]. However, the low growth temperature would lead to poor selectivity over SiO_2 hardmask and SiON spacer regions due to insufficient desorption of nucleated seeds on the gate lines and spacers. Increasing the growth temperature to 635 ˚C could achieve both high growth selectivity and good $In_{0.4}Ga_{0.6}As$ film quality, as illustrated in [Fig. 2.3 (d)]. It should be pointed out that the growth temperature cannot be too high as it would degrade the quality of high-k

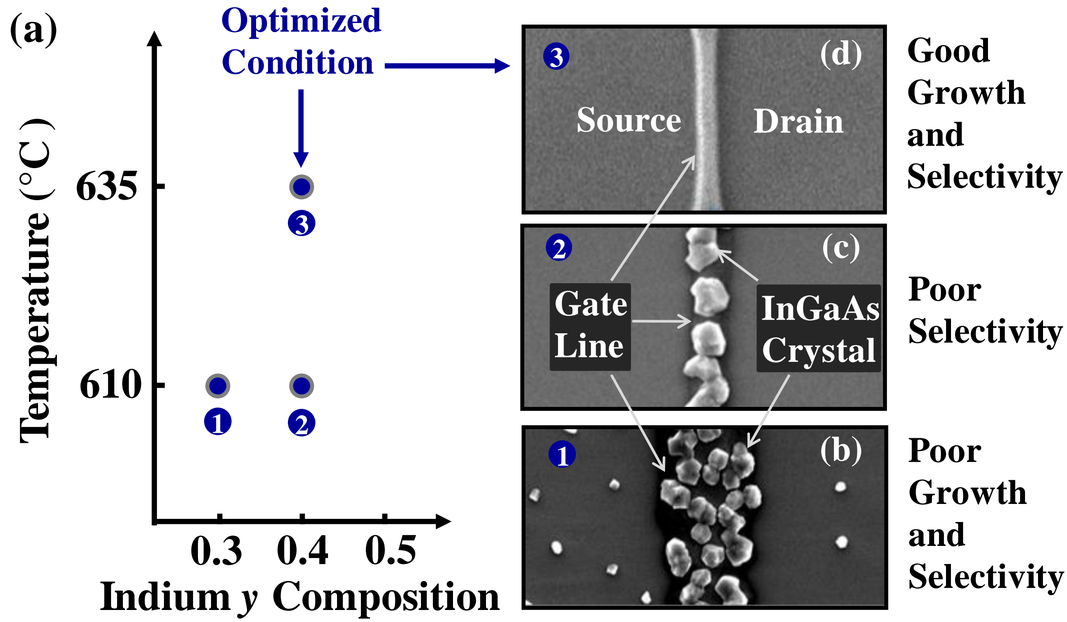


Fig. 2.3. (a) composition and MOCVD growth temperature are the two key factors affecting the growth. SEM images show the $In_{0.4}Ga_{0.6}As$ film quality and selectivity over SiO_2 hardmask and SiON spacer regions: (b) three dimensional growth due to huge lattice mismatch; (c) good quality $In_{0.4}Ga_{0.6}As$ growth with poor selectivity; (d) selective growth was achieved by increasing temperature to enable the desorption of nucleated seeds on the gate lines and spacers.

gate dielectric HfAlO/InGaAs interface, and thus affect the performance of the InGaAs transistors.

In addition, since the selective epitaxy process was carried out right after spacer formation, and the quality of the growth material would be affected by the surface morphology of the starting substrate, the F-based dry etch process used to form the SiON spacer should not roughen the InGaAs surface in the S/D regions. Physical characterization using atomic force microscope (AFM) was performed to investigate the effect of dry etch process on the surface roughness of $In_{0.7}Ga_{0.3}As$. Fig. 2.4 shows 0.872 nm root-mean square (RMS) surface roughness of the

$In_{0.7}Ga_{0.3}As$ after the spacer formation, indicating a good starting surface morphology for the epitaxial growth.

After process optimization, the MOCVD selective growth was chosen to be conducted at 635 ºC and at a chamber pressure of 75 Torr for the growth of $In_{0.53}Ga_{0.47}As$ on $In_{0.7}Ga_{0.3}As$. Trimethylgallium (TMGa), Trimethylindium (TMIn) and tertiarybutylarsine (TBA) were employed as precursors. Flow rates for TMGa, TMIn, and TBA were 16, 130, and 60 sccm, respectively, for the growth of $In_{0.53}Ga_{0.47}As$ on $In_{0.7}Ga_{0.3}As$. SiH_4 was used to achieve *in situ* n-type doping of $\sim 4\times10^{19}$ cm^{-3}, as confirmed by the Hall measurement. This is significantly higher than the n-type doping concentration obtained using Si implant and anneal, which saturates at $\sim 8\times10^{18}$ cm^{-3} [53].

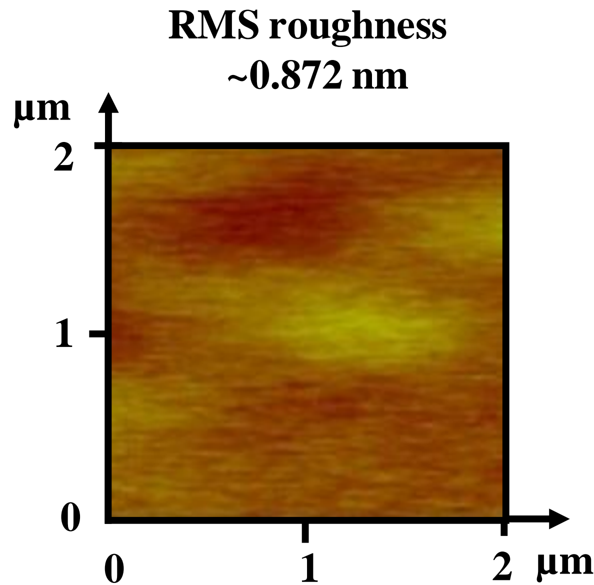


Fig. 2.4. AFM shows RMS surface roughness of the $In_{0.7}Ga_{0.3}As$ surface in the S/D regions after spacer etch, indicating a good growth starting surface. The RMS surface roughness of the pristine $In_{0.7}Ga_{0.3}As/InP$ starting substrate was ~0.32 nm.

2.3.2 Process Flow and Device Fabrication

The process flow for device fabrication is illustrated in Fig. 2.5. The substrates were purchased from an external vendor. A first 500 nm thick $In_{0.55}Ga_{0.45}As$ well layer with a p-type doping concentration N_A of 5×10^{17} cm^{-3} and a second 20 nm thick $In_{0.7}Ga_{0.3}As$ channel layer with a lower N_A of 1×10^{16} cm^{-3} were sequentially grown on InP substrates. High resolution X-ray diffraction (HRXRD) performed on a blanket sample confirms the composition and high crystal quality of the InGaAs epitaxial layers [Fig. 2.6].

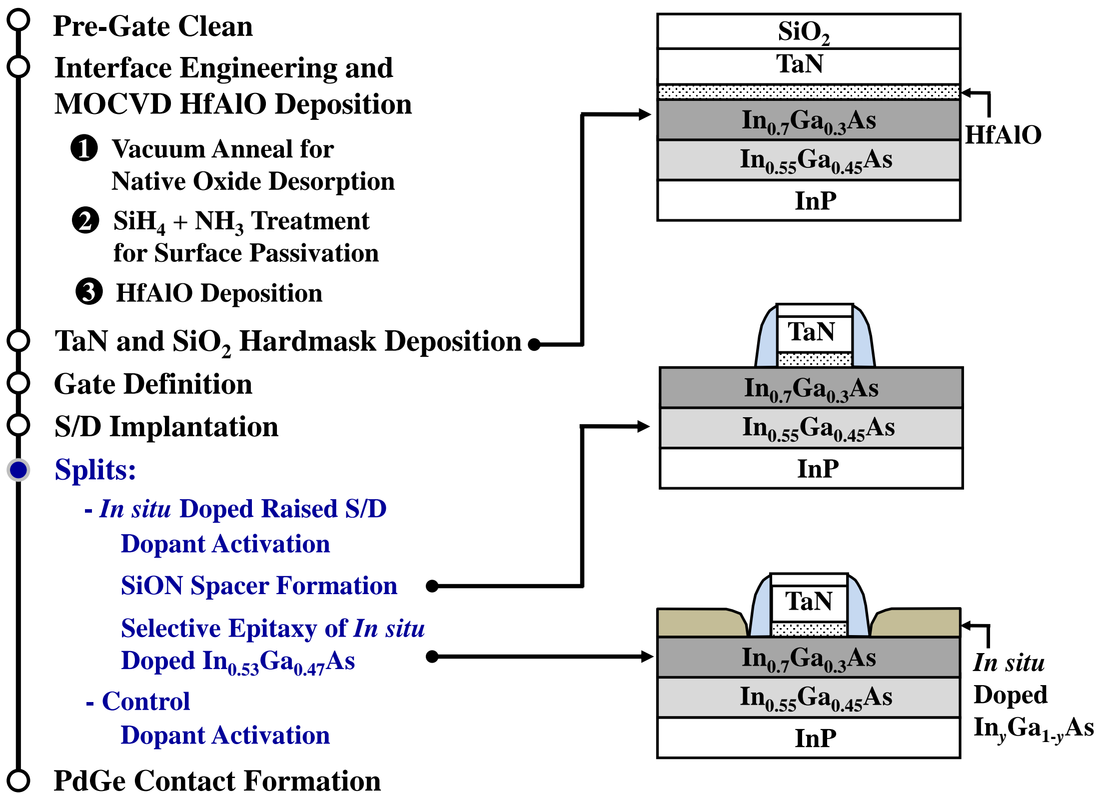


Fig. 2.5. (a) Process sequence employed in the fabrication of $In_{0.7}Ga_{0.3}As$ channel N-MOSFETs with *in situ* doped raised S/D, with cross-section schematics after steps of (b) TaN and SiO_2 hardmask deposition, (c) SiON spacer formation, and (d) selective epitaxy of *in situ* doped $In_yGa_{1-y}As$.

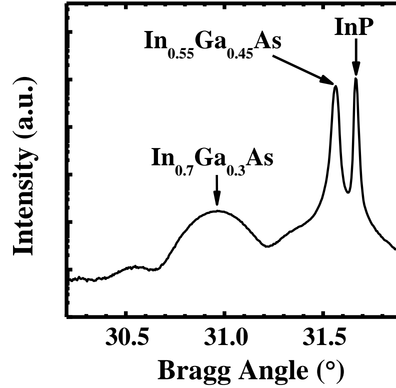


Fig. 2.6. HRXRD shows well-defined $In_{0.7}Ga_{0.3}As$ and $In_{0.55}Ga_{0.45}As$ peaks, indicating high crystalline quality of the epilayers.

Pre-gate clean was performed on the $In_{0.7}Ga_{0.3}As$ surface. The pre-gate clean comprises HCl (HCl:H_2O=1:3) cleaning for 3 minutes to remove the native oxide, NH_4OH (NH_4OH:H_2O=1:10) cleaning for 10 minutes to remove excess elemental arsenic, and a dip in concentrated $(NH_4)_2S$ for 10 minutes followed by 30 s rinse in deionized water for *ex situ* passivation. This leads to the formation of In-S, Ga-S, and As-S bonds to protect the surface from being oxidized during the wafer transfer as well as the subsequent high-*k* deposition [85]. Incomplete removal of S element could diffuse into the InGaAs channel during the subsequent high thermal process, i.e. post deposition anneal (PDA) or S/D dopant activation. It then served as the an n-type dopant in InGaAs channel, leading to negative threshold voltage shift as well as increase in interface trap density. This phenomenon happens when the thermal budget is higher than 600 ˚C. The S-passivated InGaAs surface was found to be thermally stable up to 500 ˚C. Right after this, the samples were quickly loaded into a multiple-chamber MOCVD gate cluster system [85]-[89]. In the first chamber of the gate cluster system, the wafers were annealed at 520 ºC for 60 s at a process pressure of 1×10^{-5} Torr for desorption of any native oxide that could have formed. After vacuum

annealing, the wafers were transferred to a second chamber through the transfer module for SiH_4 and NH_3 passivation under a process pressure of 5 Torr (the flow rates of SiH_4, NH_3, and N_2 were 60, 60 and 250 sccm, respectively). Next, without breaking the vacuum, the wafers were transferred to a third chamber for HfAlO high-*k* dielectric deposition of ~19 nm. The HfAlO high-*k* dielectric film was deposited at 450 ºC using a single cocktail metal organic source, i.e., $HfAl(MMP)_2(OiPr)_5$, as precursor and Ar as the carrier gas [87]. PDA at 500 ºC for 60 s was performed prior to reactive sputter deposition of 100 nm TaN.

70 nm of PECVD SiO_2 was also deposited to cover the top surface of TaN gate electrode for selective epitaxy. This prevents exposure of TaN top surface in a subsequent $In_yGa_{1-y}As$ epitaxy step. After gate lithography and dry etch with Cl_2-based plasma chemistry, S/D regions were formed by Si implant at 30 keV with dose of 1×10^{14} cm^{-2}, and activated at 600 ºC for 60 s. This was followed by silicon oxynitride (SiON) spacer formation to cover the side wall of the gate stack for subsequent selective InGaAs MOCVD epitaxy process to form the raised S/D structures. The MOCVD process was skipped for the control devices. Next, 40 nm of Pd and 90 nm of Ge were deposited on selected contact regions using electron beam evaporation. The ratio of Ge/Pd was chosen to be larger than two so that the excess Ge can be epitaxially grown on the heavily doped InGaAs to form low-resistance ohmic contacts. Finally, rapid thermal anneal (RTA) was performed at 400 ºC for 10 s to complete the device fabrication.

Fig. 2.7 (a) shows the layout of a transistor structure. Scanning electron microscopy (SEM) image in Fig. 2.7 (b) depicts a zoomed-in view of a completed

$In_{0.7}Ga_{0.3}As$ channel N-MOSFET near the gate line region which shows selective epitaxial InGaAs, TaN metal gate and SiON spacers. The SiON spacers cover the sidewalls of the TaN gate and also prevent the raised S/D from electrically contacting the gate sidewalls.

Fig. 2.8 (a) shows the cross-sectional transmission electron microscopy (TEM) image across line A-A' in Fig. 2.7 (b). The height of the raised $In_{0.53}Ga_{0.47}As$ S/D structure is around 60 nm. High-resolution TEM image of the $In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As$ heterostructure in Fig. 2.8 (b) confirms the pseudomorphic epitaxial growth of $In_{0.53}Ga_{0.47}As$ on $In_{0.7}Ga_{0.3}As$. Fast Fourier transform (FFT) diffractogram in Fig. 2.8 (c) reveals the good crystalline quality of $In_{0.53}Ga_{0.47}As$ epitaxial layer.

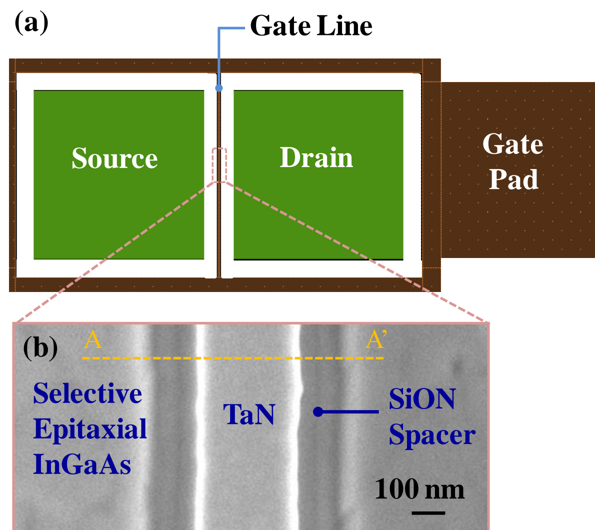


Fig. 2.7. (a) Layout of a transistor structure. (b) SEM image showing the zoomed-in view of the transistor gate line region with selective epitaxial $In_{0.53}Ga_{0.47}As$, TaN metal gate and SiON spacers. The SiON spacers prevent the raised S/D from electrically contacting the gate sidewalls. The cross-section TEM image across line A-A' is shown in Fig. 2.8.

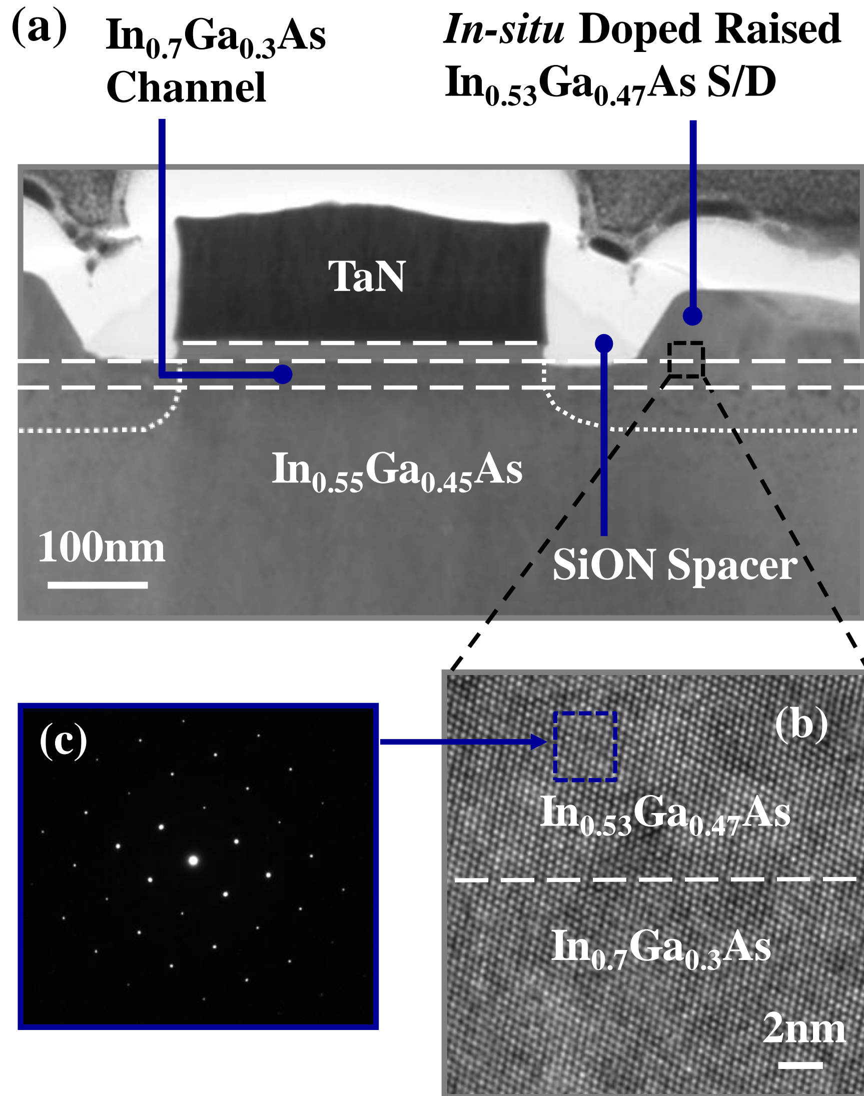


Fig. 2.8. (a) TEM image of a completed $In_{0.7}Ga_{0.3}As$ channel N-MOSFET with selectively grown *in situ* doped raised S/D. (b) High resolution TEM and (c) Fast Fourier transform (FFT) diffractogram, revealing the excellent crystalline quality of the $In_{0.53}Ga_{0.47}As$ epilayer.

2.3.3 Device Characterization and Analysis

Identical equivalent oxide thickness (EOT) of ~7.4 nm was obtained for both control devices as well as devices with raised S/D, as shown in inversion capacitance-voltage (*C-V*) characteristics at a frequency of 100 kHz in Fig. 2.9 (a). Further inversion *C-V* measurement was performed at the frequencies of 10 kHz, 100 kHz, and 1 MHz for the device with raised S/D, as shown in Fig. 2.9 (b). Frequency dependent flat-band voltage shift was observed, this could be due to mid-gap interface traps and the electron trapping during the previous measurement.

Fig. 2.10 (a) plots the I_D-V_{GS} curves of a control $In_{0.7}Ga_{0.3}As$ MOSFET as well as an $In_{0.7}Ga_{0.3}As$ MOSFET with raised S/D. The gate length L_G of the two devices is 700 nm. I_D-V_{DS} characteristics of the same pair of devices with good saturation and pinch-off characteristics are shown in Fig. 2.10 (b). Drive current enhancement of ~10.5% was observed at a gate overdrive V_{GS} - V_{TH} of 2.5 V and V_{DS} of 2.5 V for $In_{0.7}Ga_{0.3}As$ device with the raised S/D structure. This is attributed to the reduction of the S/D series resistance. The performance of the devices is reasonably good considering that equivalent oxide thickness EOT of ~7.4 nm gate dielectric was used. Further improvement in performance can be achieved by reducing the gate dielectric thickness as well as the gate length.

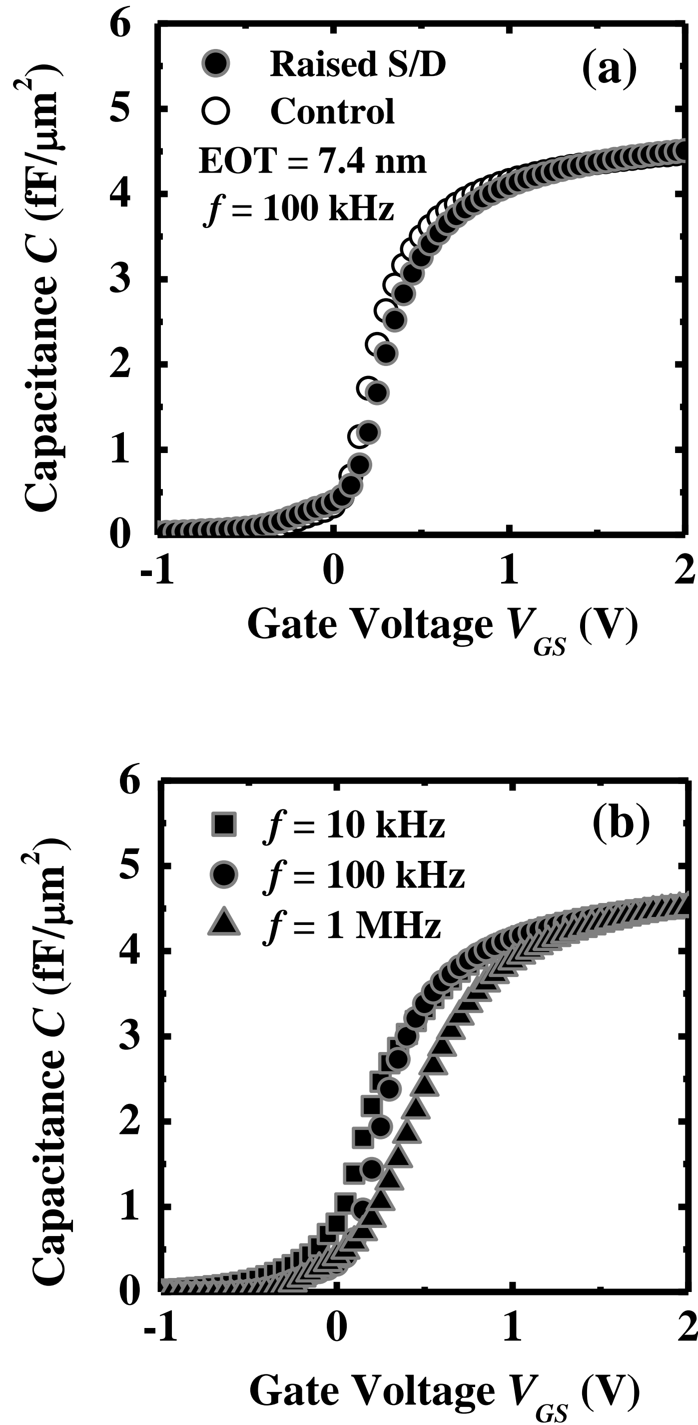


Fig. 2.9. (a) Inversion *C*-*V* curves measured at the frequency of 100 kHz show comparable equivalent oxide thickness EOT for control device and device with raised S/D. (b) *C*-*V* characteristics of the device with raised S/D measured from 10 kHz to1 MHz.

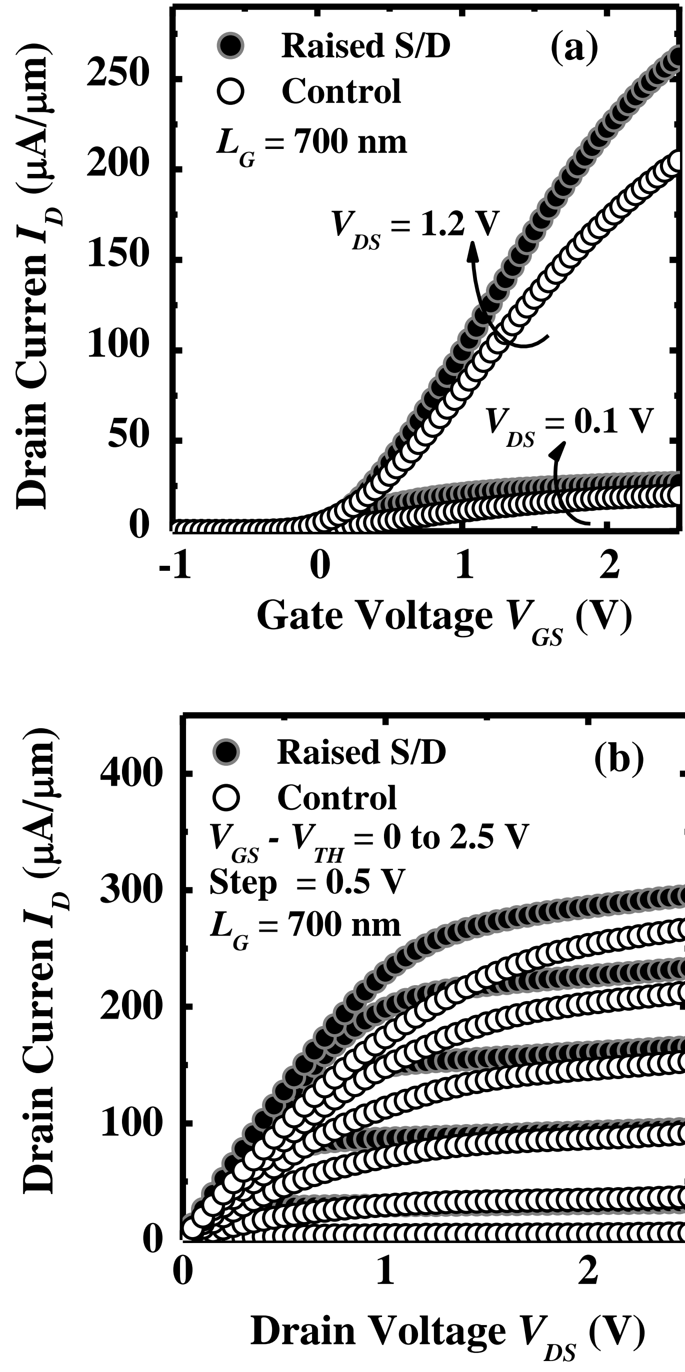


Fig. 2.10. (a) I_D-V_{GS} plot in the linear (V_{DS} = 0.1 V) and saturation (V_{DS} = 1.2 V) regions. (b) I_D-V_{DS} curves of the same pair of devices, showing good saturation and pinch-off characteristics. Drive current is higher for the $In_{0.7}Ga_{0.3}As$ N-MOSFET with raised S/D as compared with the $In_{0.7}Ga_{0.3}As$ N-MOSFET control.

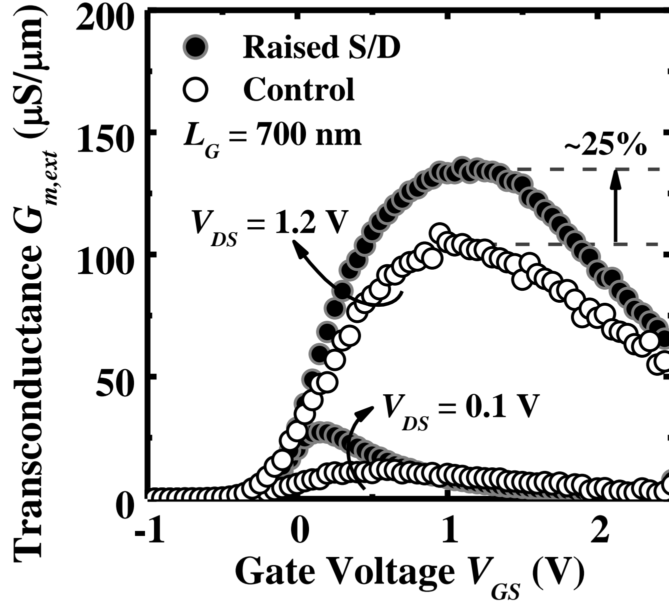


Fig. 2.11. $G_{m,ext}$-V_{GS} curves of the same pair of devices in Fig. 2.10. *In situ* doped raised S/D gives rise to a ~25% enhancement in saturation $G_{m,ext}$ due to source and drain series resistance reduction.

Fig. 2.11 shows the extrinsic transconductance $G_{m,ext}$ versus V_{GS} for both N-MOSFETs. For this pair of devices, the raised S/D architecture with *in situ* doping gives rise to ~25% enhancement in saturation $G_{m,ext}$. The total resistance R_{Total} between S/D measured at low V_{DS} of 0.1 V decreases with increasing V_{GS}, as shown in Fig. 2.12, and approaches the S/D series resistance R_{SD} at high gate overdrive. R_{SD} is the sum of source resistance R_S and drain resistance R_D. Using the extraction method in Ref. [97], the R_{SD} of *in situ* doped raised S/D device and the control were approximated at V_{GS} of 10 V and extracted to be 3.1 and 3.9 kΩ·µm, respectively. Reduced series resistance is a result of combined contributions from the higher S/D doping concentration as well as the structural improvement in the raised S/D that leads to more current spreading in the S/D regions.

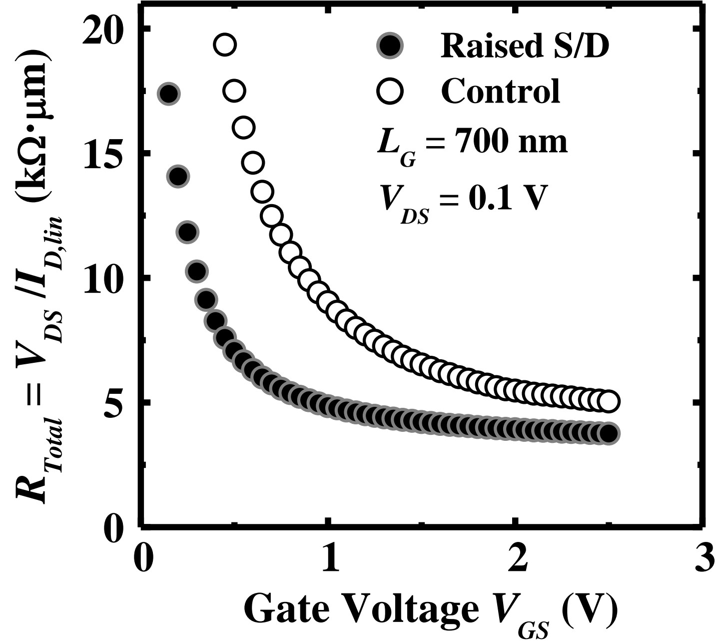


Fig. 2.12. Total resistance in linear regime (V_{DS} = 0.1) at large V_{GS} indicates smaller series resistance of the device with raised S/D than that of control.

The spacer separates the edge of the gate and the edge of the epitaxial InGaAs by 80 nm, as shown in Fig. 2.8 (a). The S/D region underneath the spacer has a sheet resistance of ~63 Ω/□, as extracted from the transmission line measurement (TLM) structure. Therefore, the series resistances contributed by source and drain regions under the spacers add up to be ~10.1 Ω·μm, which is much smaller than the extracted R_{SD} of ~3.1 kΩ·μm. In this work, the gate to contact spacing is ~ 6 μm, and a major component of the R_{SD} is the S/D resistance between the spacers and the PdGe contacts. The resistance of the S/D regions under the spacers may be dominant if a self-aligned contact metallization process is used, and can be reduced by thinning the spacers.

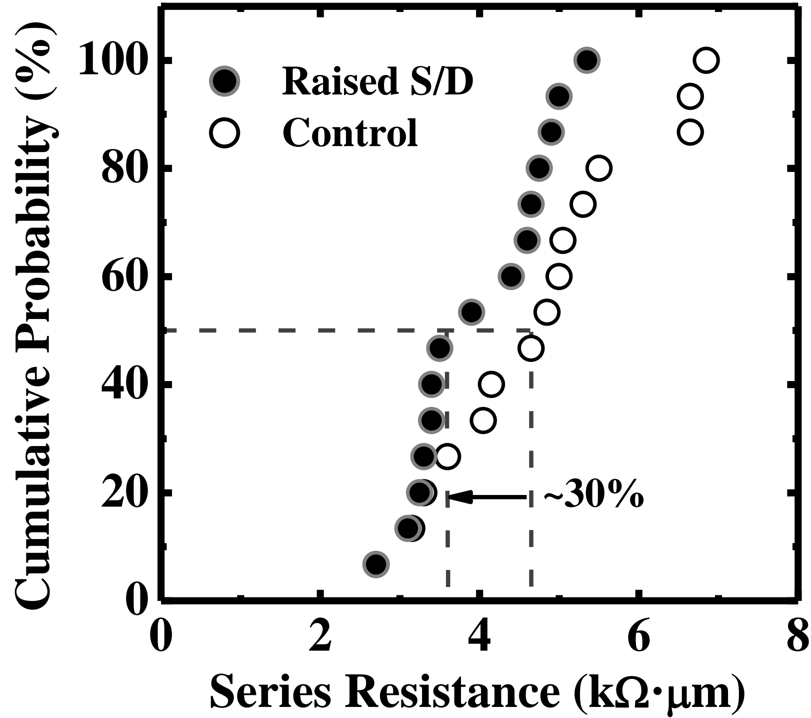


Fig. 2.13. *In situ* doped raised S/D leads to ~30% reduction of the median series resistance. 15 devices for each split were measured. The gate lengths of the devices measured range from 350 to 1000 nm.

Further electrical characterization was performed on a sample size of about 15 devices per split. Fig. 2.13 shows the cumulative distribution of the extracted S/D series resistance. The gate lengths of the devices measured range from 350 nm to 1000 nm. The statistical result shows a ~30% reduction in the median R_{SD}. This contributes to drive current enhancement. Fig. 2.14 plots the off-state leakage current I_{OFF} measured at V_{GS}-V_{TH} of -0.2 V and saturation current I_{Dsat} measured at V_{GS}-V_{TH} of 2 V for the two sets of device. Best fit trend lines for the control devices and devices with raised S/D are shown in dashed and solid lines, respectively. I_{Dsat} enhancement of ~20% at a fixed I_{OFF} of 10^{-6} A/μm was achieved.

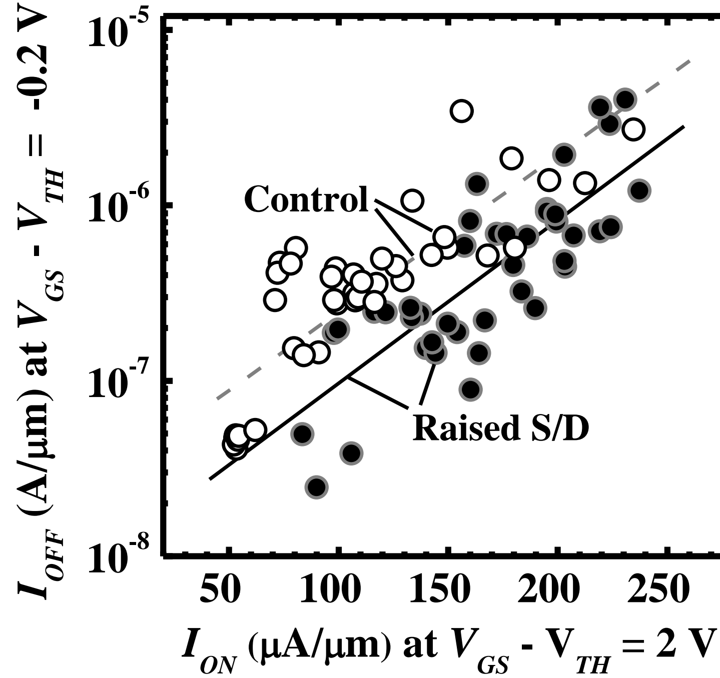


Fig. 2.14. *In situ* doped raised S/D gives ~20% I_{Dsat} enhancement at a fixed I_{OFF} of 10^{-6} A/µm. Devices measured have gate lengths ranging from 350 to 1000 nm. The best fit lines for control devices and devices with raised S/D are plotted in dashed and solid lines, respectively. V_{TH} is the mean threshold voltage for each group of devices. Threshold voltage was extracted at V_{DS} = 1.2 V by extrapolation of the I_D-V_{GS} curve at the V_{GS} which maximizes the transconductance.

Fig. 2.15 benchmarks the normalized peak $G_{m,ext}$ of $In_{0.7}Ga_{0.3}As$ devices with *in situ* doped raised S/D structure in this work with our previous work [47],[98]. The physical HfAlO high-*k* thickness of $In_{0.7}Ga_{0.3}As$ MOSFETs in this work and $In_{0.53}Ga_{0.47}As$ MOSFETs with S/D stressors [47],[98] is ~19 and ~15 nm, respectively. Peak $G_{m,ext}$ was normalized with oxide capacitance C_{ox} to account for the difference in EOT. Despite a larger R_{SD} as compared with that reported in Refs.

47 and 98, higher $G_{m,ext}$ was achived. This is due to higher indium composition of 70% in the channel for improved electron mobility.

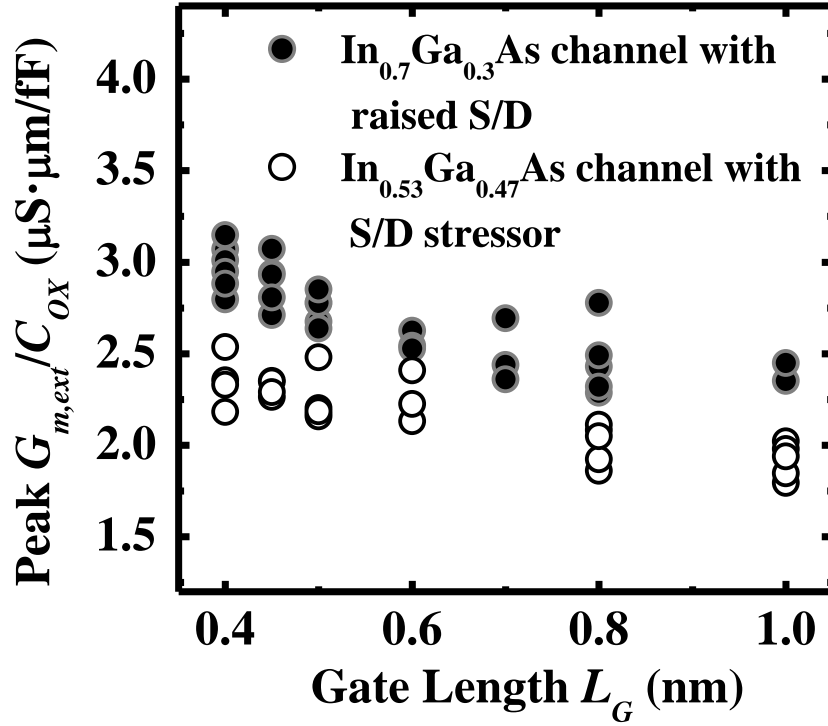


Fig. 2.15. Normalized peak $G_{m,ext}$ (measured at V_{DS} = 1.2 V) versus L_G. $In_{0.7}Ga_{0.3}As$ channel devices with raised S/D show higher normalized peak $G_{m,ext}$ due to higher indium composition of 70% in the channel for improved electron mobility.

2.4 Summary

In this Chapter, raised S/D structure with *in situ* doping process was demonstrated in InGaAs channel MOSFETs with indium composition as high as 70 %. An epitaxy process using MOCVD was first developed to grow high quality $In_{0.53}Ga_{0.47}As$ film on $In_{0.7}Ga_{0.3}As$ substrate with high selectivity over SiO_2. The process module was then integrated into a self-aligned gate-first process to fabricate the $In_{0.7}Ga_{0.3}As$ N-MOSFETs. ~30% R_{SD} reduction was achieved due to combined contributions from the higher S/D doping concentration as well as the structural improvement in the raised structure, leading to ~20% I_{Dsat} enhancement at a fixed I_{OFF} of 10^{-6} A/μm. The S/D engineering approach demonstrated in this Chapter provides a promising option for transistor R_{SD} reduction, which is an important step towards realization of high performance InGaAs channel N-MOSFETs.

Chapter 3

Advanced Gate Stack Technology for $In_{0.7}Ga_{0.3}As$ N-Channel Metal-Oxide-Semiconductor Field-Effect Transistors

3.1 Introduction

High mobility III-V compound semiconductors are attractive as alternative channel materials for extending the performance limits of complementary metal-oxide-semiconductor (CMOS) logic technology [99]-[104]. To realize high performance III-V n-channel metal-oxide-semiconductor field-effect transistors (N-MOSFETs), a high quality and thermodynamically stable gate stack on III-V channel materials is needed. Gate dielectrics on III-V's have been extensively investigated, such as *in situ* molecular beam epitaxy (MBE) growth of $Ga_2O_3(Gd_2O_3)$ [79],[105] and molecular atomic deposition of $Ga_2O_3(Gd_2O_3)/Si_3N_4$ [105], atomic layer deposition (ALD) of Al_2O_3 [44],[81],[91], HfO_2 [45], HfAlO [45], ZrO_2 [46],[83] and $ZrO_2/LaAlO_x$ [46], as well as surface passivation technology employing SiH_4 [87], SiH_4+NH_3 [47], AlON [84], phosphorus [48], and phosphorus nitride P_xN_y [49] with metal organic chemical vapor deposition (MOCVD) of HfAlO or HfO_2.

InGaAs, with a high electron mobility and bandgap E_G in the range of 0.36-1.42 eV, has attracted great interest as a channel material. However, when the high-k dielectric is formed directly on the InGaAs channel, a high density of interface traps (D_{it}) can lead to significant carrier scattering and mobility degradation [50],[56]. Recently, $In_{0.7}Ga_{0.3}As$ channel quantum well field-effect transistors (QWFETs) comprising $TaSiO_x$ gate dielectric on InP cap layer with very high transconductance and drive current were reported [50]. InGaAs channel N-MOSFETs with InP barrier layer and ALD Al_2O_3 [56] or PECVD SiO_2 [93] gate dielectric were also reported. The gate last process was adopted in Refs. [50],[56],[93].

In this Chapter, two advanced technology schemes were explored to realize high quality gate stack for $In_{0.7}Ga_{0.3}As$ N-MOSFETs. Section 3.2 discusses the first demonstration of InP-capped $In_{0.7}Ga_{0.3}As$ N-MOSFETs formed using a gate first process, in which self-aligned implant and anneal were used to form the source and drain (S/D) regions. The gate stack comprising TaN/Al_2O_3 formed on $InP/In_{0.7}Ga_{0.3}As$ was thermally stable after 600 ºC 60 s S/D dopant activation anneal. The thickness of the InP cap was found to have significant impact on the electrical characteristics of the transistors. Section 3.3 investigates the low temperature Si_2H_6 passivation technique which forms an ultra-thin SiO_2/Si interfacial passivation layer (IPL) between the high-k dielectric and the $In_{0.7}Ga_{0.3}As$ channel. When integrated with ALD deposited HfO_2 with a dielectric constant of ~20, a capacitance equivalent thickness (CET) of ~1.7 nm was achieved. Drive current of 320 μA/μm was obtained for a gate length (L_G) of 4 μm at V_{DS} and gate over drive of 2 V, with subthreshold swing S comparable to the best reported in the literature.

3.2 Self-Aligned Gate-First $In_{0.7}Ga_{0.3}As$ N-MOSFETs with an InP Capping Layer for Performance Enhancement

In this Section, self-aligned gate-first $In_{0.7}Ga_{0.3}As$ N-MOSFETs with an InP capping layer was investigated. Significant drive current enhancement was achieved as compared with the transistors without InP capping layer. Excellent Al_2O_3/InP interface quality was realized by Trimethylaluminum (TMA) treatment and ALD deposited Al_2O_3. The results of physical characterization as well as the effect of different InP barrier layer thickness on the electrical characteristics of N-MOSFETs were discussed. Current-voltage (*I-V*) characteristics, transconductance, subthreshold characteristics, contact resistance and on- and off- state currents of $In_{0.7}Ga_{0.3}As$ MOSFETs were studied in detail.

3.2.1 Design Concept

To illustrate the effect of inserting an InP layer between Al_2O_3 and $In_{0.7}Ga_{0.3}As$, the schematics of the $In_{0.7}Ga_{0.3}As$ MOSFETs without and with an InP layer are shown in Fig. 3.1 (a) and (b), respectively. It has been widely reported that, compared with SiO_2/Si, interface between Al_2O_3 and III-V materials has much higher trap density [108]. Two factors would degrade the transistor drive current when Al_2O_3 is formed directly on the $In_{0.7}Ga_{0.3}As$ channel. First, many of the mobile electrons moving from source to drain could be trapped by the high-density $Al_2O_3/In_{0.7}Ga_{0.3}As$ interface traps, leading to reduced number of mobile electrons in the channel. Second, the mobile electrons would be scattered by the charged traps at the $Al_2O_3/In_{0.7}Ga_{0.3}As$ interface which reduces the electron mobility. When inserting an InP capping layer as shown in Fig. 3.1 (b), two interfaces, Al_2O_3/InP and

$InP/In_{0.7}Ga_{0.3}As$, exist in the composite gate stack structure. The 0.41 eV conduction band offset ΔE_C at the $InP/In_{0.7}Ga_{0.3}As$ interface confines the electron to flow in the $In_{0.7}Ga_{0.3}As$ channel, as shown in the band diagram across line A-A' [Fig. 3.1 (b)] of an $In_{0.7}Ga_{0.3}As$ MOSFET operated at strong inversion [Fig. 3.1 (c)]. Traps at the relatively poor Al_2O_3/InP interface are now moved away from the channel, reducing the Coulomb scattering, and realizing enhanced mobility and drive current.

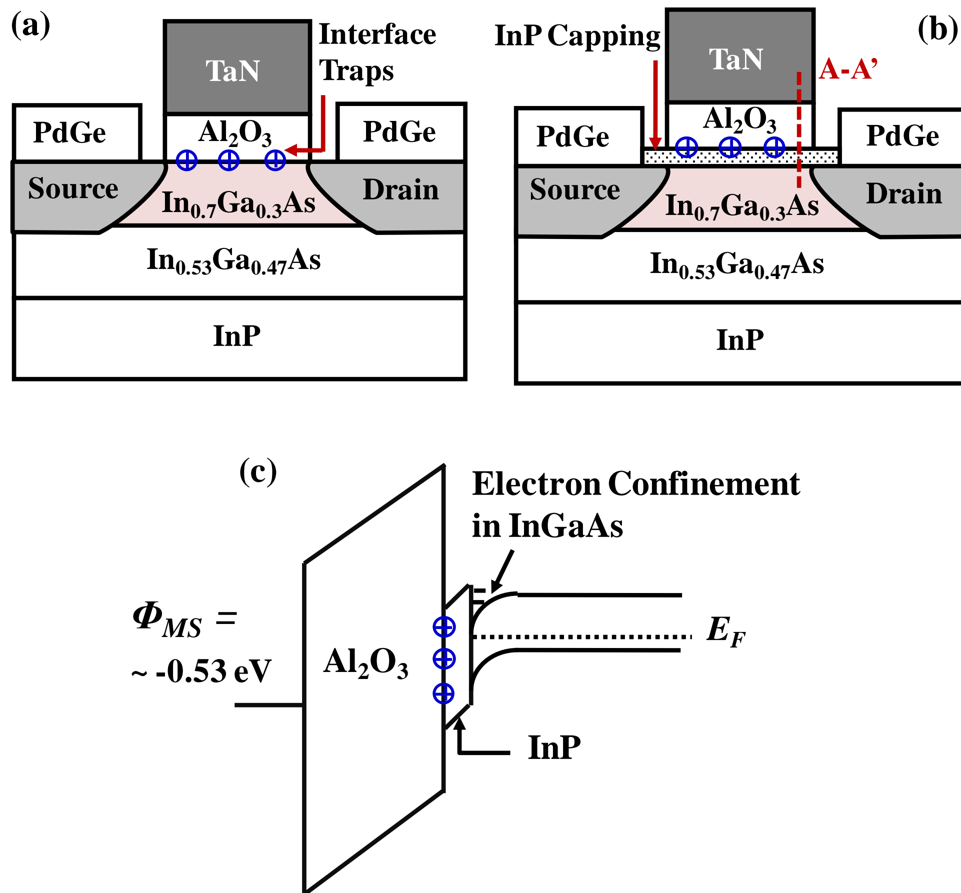


Fig. 3.1. Schematics showing the $In_{0.7}Ga_{0.3}As$ N-MOSFETs (a) without and (b) with an InP layer. (c) Band alignment across A-A' of an $In_{0.7}Ga_{0.3}As$ N-MOSFET with InP capping layer operating in the strong inversion regime. The InP cap confines the electrons moving in the $In_{0.7}Ga_{0.3}As$ channel and moves the interface traps away from the channel.

3.2.2 High Quality and Thermally Stable Al_2O_3/InP Interface

It was reported in Ref. [108] that the Al_2O_3/InP interface has a lower D_{it} than the HfO_2/InP interface, and the transistor drive current and transconductance depend significantly on the high-*k*/InP interface quality. To develop the recipe of realizing a good Al_2O_3/InP interface, InP MOS capacitors were fabricated. The process flow for fabricating the InP capacitor and the schematic of a completed device structure are shown in Fig. 3.2 (a) and (b), respectively.

After a two-step pre-gate cleaning process by native oxide removal using HF (1:100) for 60 s and surface passivation using diluted $(NH_4)_2S$ solution ($(NH_4)_2S$:H_2O = 1:4) for 10 minutes, the InP substrate with a n-type doping N_D of 2×10^{17} was loaded into an ALD system (Savannah 200) where TMA treatment was done with a pulse duration of 30 ms for 50 cycles at a temperature of 250 ºC. This was followed by the deposition of 8 nm of Al_2O_3 with TMA and H_2O as precursors, and N_2 as the carrier gas. Post-gate dielectric deposition anneal (PDA) at 400 ºC for 60 s was performed prior to reactive sputter deposition of TaN. After gate patterning by Cl-based dry etch, Pt was sputtered as the back contact to complete the capacitor fabrication.

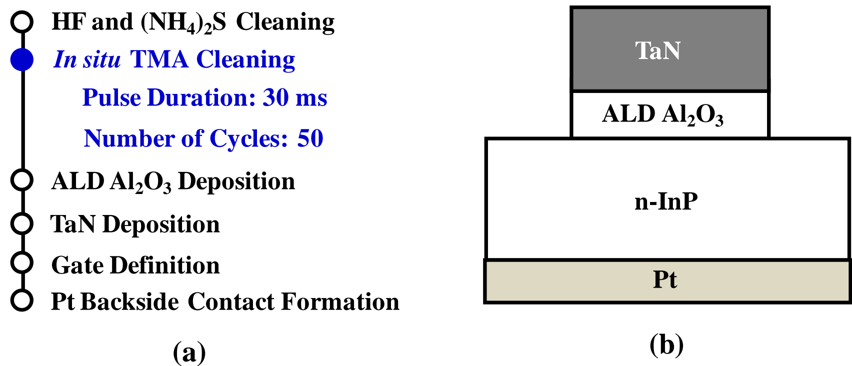


Fig. 3.2. (a) The process flow for fabricating the InP capacitor, with the TMA cleaning step. (b) The schematic of a completed InP capacitor.

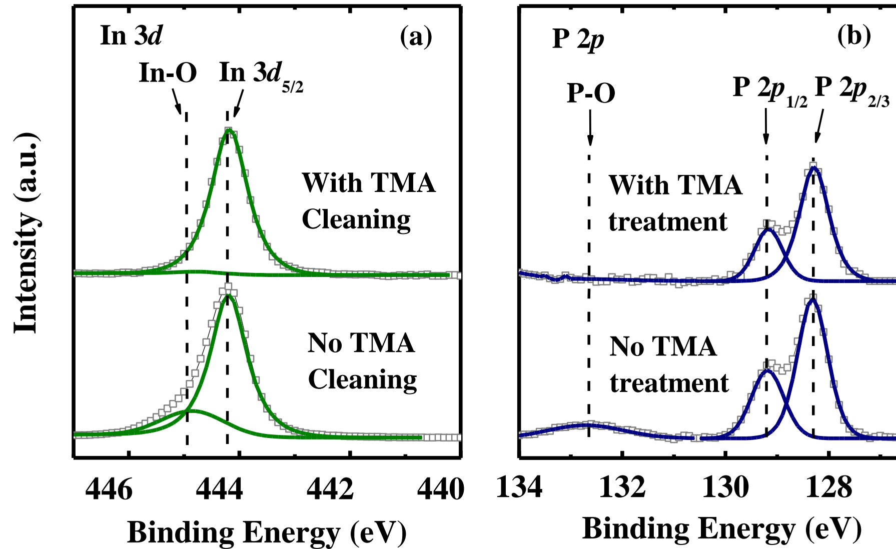


Fig. 3.3. (a) In 3*d* and (b) P 2*p* XPS spectra show that both In-O and P-O bonds were significantly reduced, indicating the effect of TMA surface treatment on the reduction of native oxide.

(a) Native Oxide Removal by TMA Surface Treatment

The key step to achieve a good Al_2O_3/InP interface is the TMA surface treatment because it can effectively reduce the native oxides that formed on the surface of III-V materials which would act as defective states in the bandgap and play a critical role in the degradation of transistor performance. X-ray photoelectron spectroscopy (XPS) analysis was employed to study the interfacial chemical bonding between Al_2O_3 and InP.

Fig. 3.3 (a) and (b) show the In 3*d* and P 2*p* XPS spectra, respectively, of a sample with a 2 nm thick Al_2O_3 directly deposited on pre-gate cleaned InP, and a sample with both pre-gate cleaning and TMA treatment prior to Al_2O_3 deposition. Both P-O and In-O bonds were significantly reduced, indicating the effect of TMA surface treatment on the reduction of native oxide.

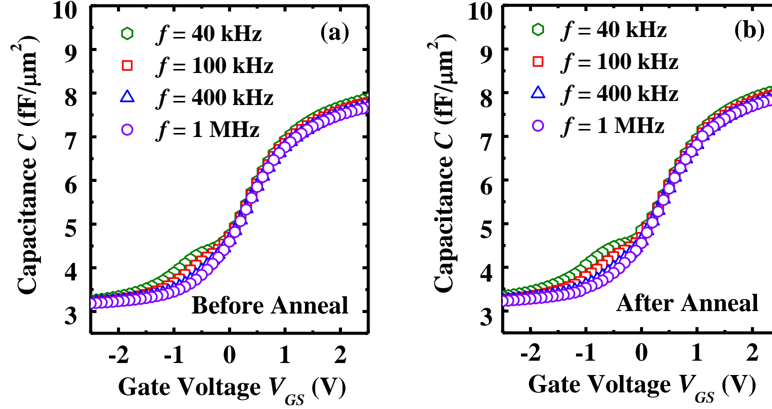


Fig. 3.4. *C-V* characteristics of an InP capacitor (a) before and (b) after thermal annealing at 600 ºC for 60 s. Characterization frequencies *f* ranging from 40 kHz to 1 MHz were used. The CET was extracted to be ~4.3 nm.

(b) Thermal Stability of TaN/Al_2O_3/InP Stack

To implement the MOSFET fabrication using the gate first process, the TaN/Al_2O_3/InP gate stack should withstand the highest thermal budget in the MOSFET fabrication process, which is 600 ˚C for 60 s used for the S/D dopant activation anneal. The InP MOS capacitor was annealed at 600 ˚C for 60 s to check the thermal stability of the TaN/Al_2O_3/InP stack.

Shown in Fig. 3.4 (a) and (b) are the *C-V* characteristics of the InP MOS capacitor before and after annealing, respectively, with frequency *f* ranging from 40 kHz to 1 MHz. Similar *C-V* characteristics with negligible frequency dispersion were observed. The bump observed at low frequency could be due to the incomplete removal of the native oxide as well as the interface defects between Al_2O_3 and InP. The slightly larger capacitance at strong inversion after annealing could be attributed to the densification of the Al_2O_3 dielectric. There is also no significant increase in the gate leakage current as shown in Fig. 3.5, indicating the good thermal stability of the TaN/Al_2O_3/InP stack.

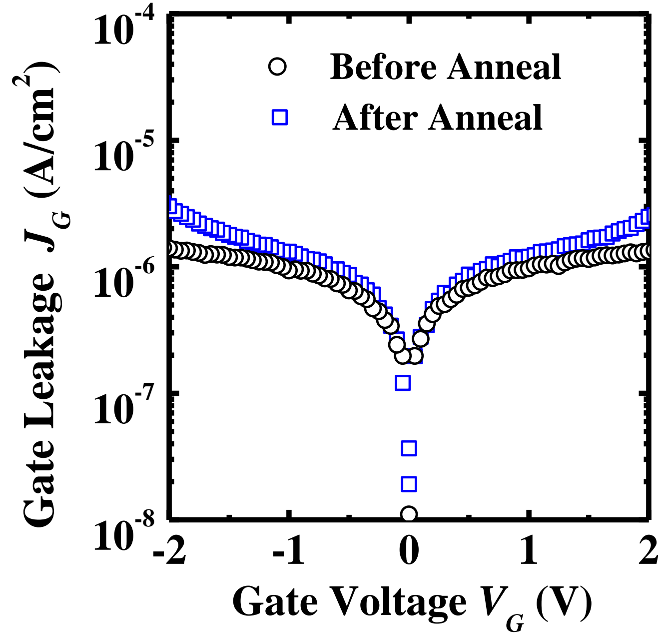


Fig.3.5. Gate leakage current density J_G increases slightly after the thermal annealing, showing good thermal stability under the condition of dopant activation anneal.

3.2.3 Fabrication and Electrical Characterization of Self-Aligned Gate-First $In_{0.7}Ga_{0.3}As$ N-MOSFETs with an InP Capping Layer

(a) Device Fabrication

Fig. 3.6 shows the process flow for fabricating the $In_{0.7}Ga_{0.3}As$ N-MOSFETs without InP capping, with 2 and 4 nm InP capping layers. Two-inch InP substrates were used as starting materials. A 500 nm $In_{0.53}Ga_{0.47}As$ layer with p-type doping concentration N_A of 2×10^{17} cm^{-3}, and a 12 nm $In_{0.7}Ga_{0.3}As$ channel layer with N_A of 2×10^{16} cm^{-3} were sequentially grown by an external vendor. On two wafers, 2 or 4 nm of undoped InP was grown on the $In_{0.7}Ga_{0.3}As$ channel layer. On a third wafer (control), no InP was grown.

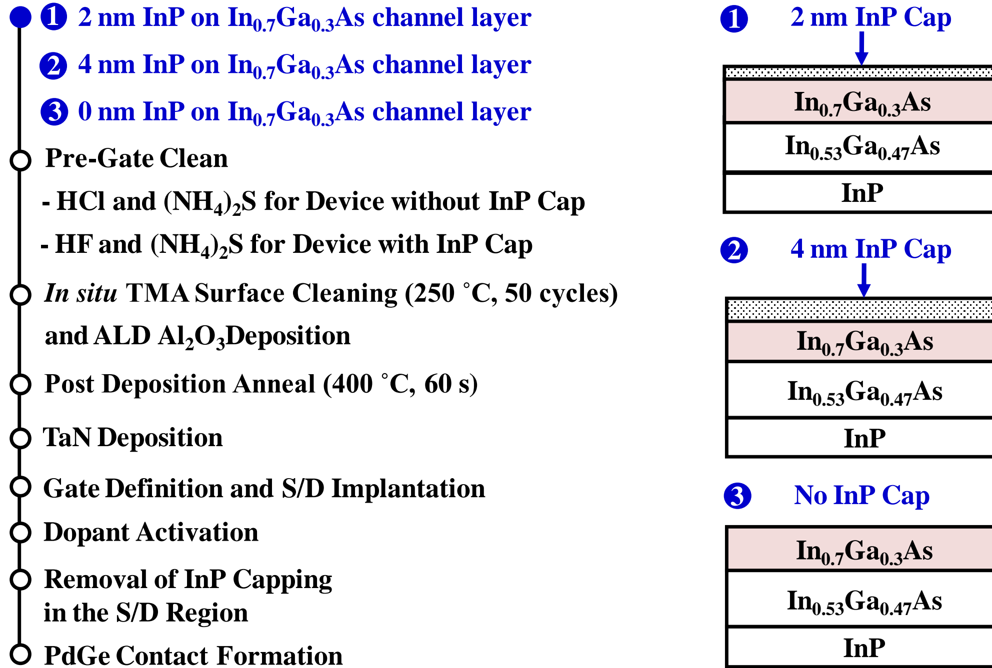


Fig. 3.6. The process flow for fabricating $In_{0.7}Ga_{0.3}As$ N-MOSFETs without InP capping, and with 2 or 4 nm InP capping layers. All steps were performed by the author except for the InP cap growth.

The pre-gate cleaning process was performed using HCl (1:3) solution for 3 minutes for the sample without the InP capping layer and HF (1:100) solution for 60 s for samples with the InP capping layer. After that, *ex situ* surface passivation using diluted $(NH_4)_2S$ solution ($(NH_4)_2S$:H_2O = 1:4) for 10 minutes was done. All samples were then loaded into an ALD system where native oxide removal by TMA was performed prior to deposition of 6.3 nm of Al_2O_3 to ensure a high quality Al_2O_3/InP interface. PDA at 400 ºC for 60 s was performed prior to reactive sputter deposition of TaN.

After gate definition, S/D regions were formed by Si implant at energy of 30 keV and dose of 1×10^{14} cm^{-2}, and activated at 600 ºC for 60 s. Dilute HCl solution

(1:1) was then used to remove the InP capping layer in S/D regions. This was followed by the HF (1:100) dip to remove the native oxide on the surface of the heavily doped $In_{0.7}Ga_{0.3}As$ S/D regions. Finally, E-beam evaporation of 40 nm thick Pd and 90 nm thick Ge were performed, and followed by rapid thermal anneal at 400 ºC for 10 s to form the PdGe contact.

(b) Results and Discussion

Fig. 3.7 (a) shows the cross-sectional TEM image of a completed $In_{0.7}Ga_{0.3}As$ N-MOSFET with a $TaN/Al_2O_3/InP$ gate stack. A 2 nm thick InP capping layer exists between Al_2O_3 and the $In_{0.7}Ga_{0.3}As$ channel as shown in Fig. 3.7 (b). The high resolution TEM in Fig. 3.7 (c) shows the sharp interface between Al_2O_3 and InP.

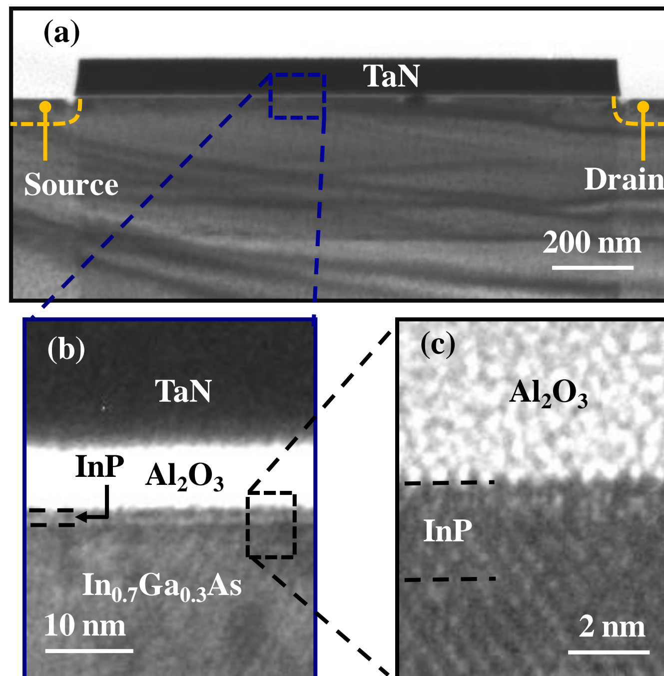


Fig. 3.7. (a) The cross-section TEM image of a completed $In_{0.7}Ga_{0.3}As$ N-MOSFET with channel and S/D regions. (b) TEM image showing the $TaN/Al_2O_3/InP/In_{0.7}Ga_{0.3}As$ stack with sharp Al_2O_3/InP interface after a 600 ºC 60 s dopant activation anneal, as shown in the high resolution TEM image in (c).

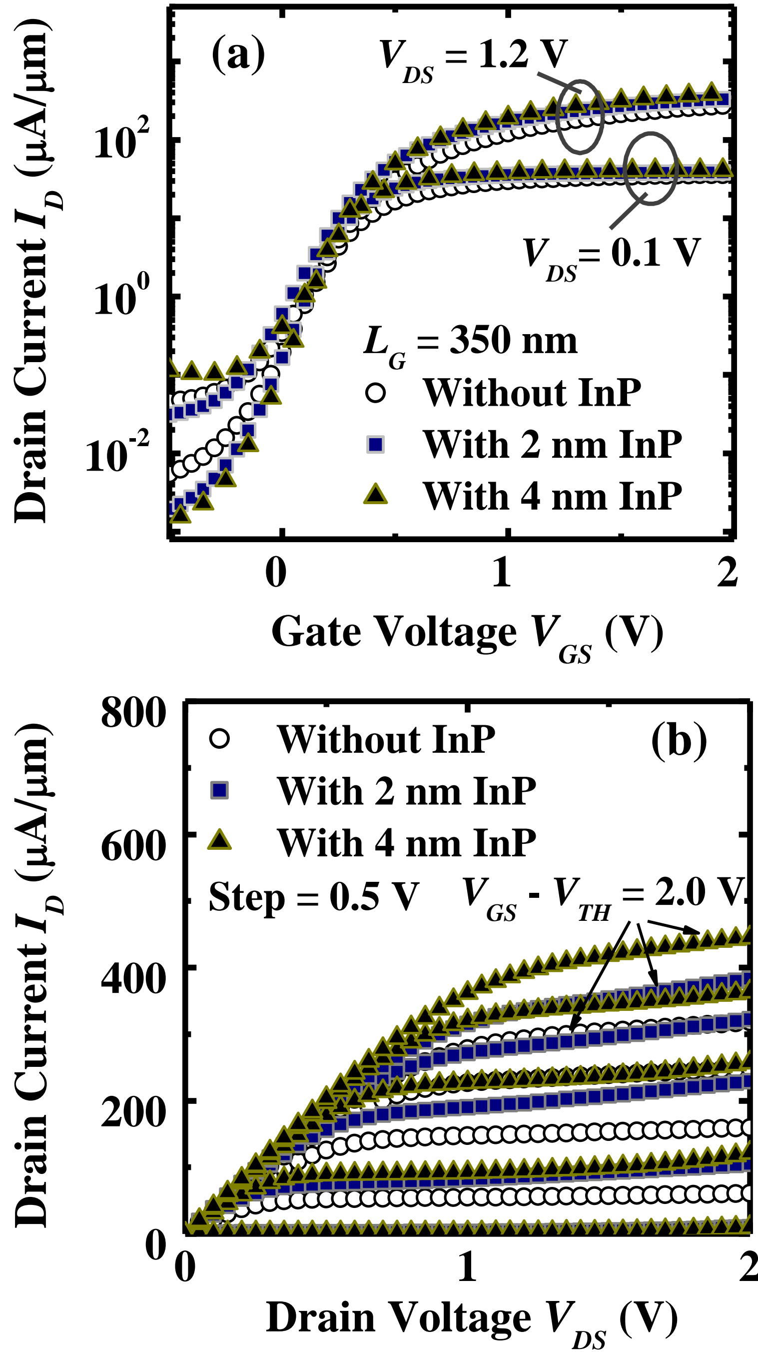


Fig. 3.8. (a) I_D–V_{GS} curves of $In_{0.7}Ga_{0.3}As$ N-MOSFETs without InP cap, with 2 nm InP cap, and with 4 nm InP cap, having subthreshold swing S of 167, 138 and 132 mV/decade, respectively. (b) I_D–V_{DS} output characteristics of the same set of MOSFETs in (a), showing excellent saturation and pinch-off characteristics. Higher I_{Dsat} was observed in MOSFETs with the InP cap, indicating improved carrier mobility due to reduced interface trap scattering.

Fig. 3.8 (a) plots the I_D-V_{GS} transfer characteristics of transistors having L_G of 350 nm in the linear (V_{DS} = 0.1 V) and saturation (V_{DS} = 1.2 V) regions versus gate voltage V_{GS}. $In_{0.7}Ga_{0.3}As$ MOSFETs without InP cap, with 2 nm InP cap, and with 4 nm InP cap have subthreshold swings S of 167, 138 and 132 mV/decade, respectively. Fig. 3.8 (b) shows the I_D-V_{DS} output characteristics of the same set of transistors in Fig. 3.8 (a). Devices with the InP cap have a higher saturation drain current I_{Dsat} as compared with the control. This is attributed to reduced carrier scattering due to interface traps, giving improved carrier mobility. I_{Dsat} is higher in the device with a thicker InP capping layer despite a smaller gate-to-channel capacitance. A significant improvement in the peak transconductance in the linear region $G_{m,lin}$ was achieved for MOSFETs with InP capping over the control, as shown in Fig. 3.9. The current of the transistors with InP capping fabricated in this thesis is lower than that in Ref. 50, this is due the much larger CET and channel length.

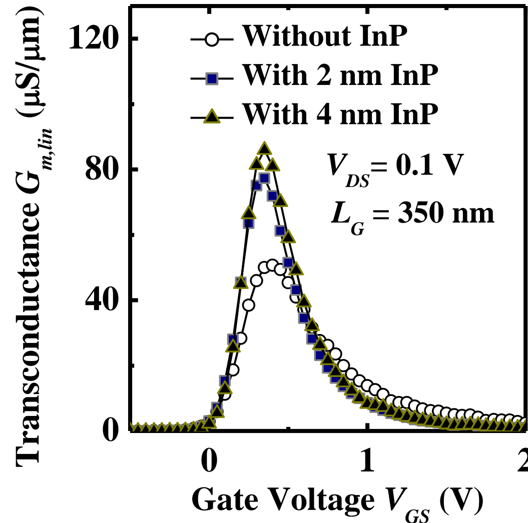


Fig. 3.9. $G_{m,lin}$-V_{GS} curves show significant $G_{m,lin}$ improvement due to the insertion of an InP capping layer.

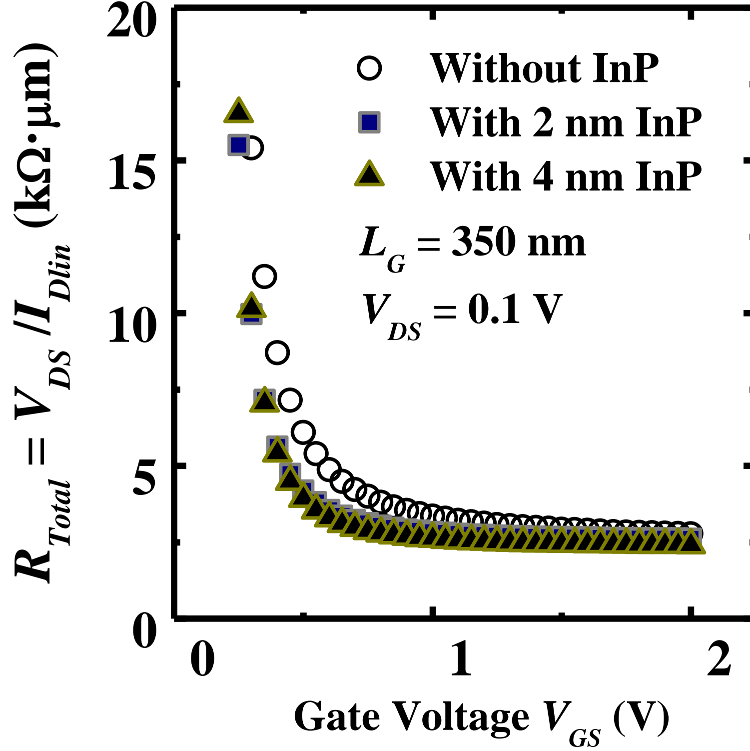


Fig. 3.10. R_{Total} versus V_{GS} plot shows that R_{SD} for all devices are similar, as PdGe contacts were formed similarly on all splits, i.e. on $In_{0.7}Ga_{0.3}As$ S/D regions following the removal of InP capping.

To consider the effect of S/D series resistance R_{SD}, the total resistance R_{Total} between S/D measured at V_{DS} of 0.1 V is plotted as a function of V_{GS} in Fig. 3.10. R_{Total} decreases with increasing V_{GS} and R_{SD} is approximated at a large V_{GS}, i.e. 10 V [97].

The extracted R_{SD} is ~2.25 kΩ·µm for all three samples. This indicates that the InP capping layer was successfully removed in S/D regions before PdGe ohmic contact formation. Removal of InP capping layer in S/D regions ensures that the PdGe ohmic contact is formed on $In_{0.7}Ga_{0.3}As$ (E_G = 0.58 eV) rather than on InP (E_G = 1.35 eV). This achieves the same contact resistance on all device splits.

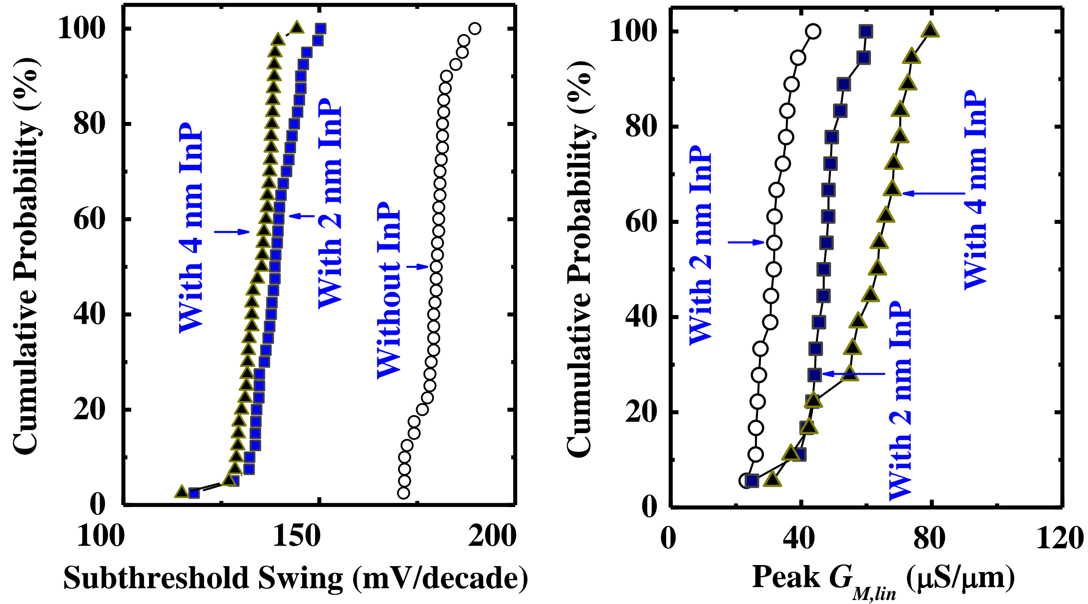


Fig. 3.11. (a) The median S is reduced by ~40 mV/decade for devices with 2 nm InP capping layer as compared with the control (without InP cap). Larger reduction is observed for devices with 4 nm InP cap. (b) Cumulative distribution of $G_{m,lin}$ shows ~48% and ~85% enhancement in the median $G_{m,lin}$ for devices with 2 nm and 4 nm thick InP cap, respectively, with respect to the control.

Extensive electrical characterization was performed on a large sample size. Subthreshold swing S is an important factor considered in the evaluation of the gate stack interface quality. Fig. 3.11 (a) summarizes the statistical distribution of S characteristics for InGaAs MOSFETs with and without InP capping. The insertion of 2 nm InP reduces the median S by ~40 mV/decade as compared with the control. A larger reduction in S is observed for devices with 4 nm InP capping layer. Fig. 3.11 (b) plots the cumulative distribution of $G_{m,lin}$. The statistical results show a ~48% enhancement in the median $G_{m,lin}$ for devices with 2 nm InP cap as compared with the control. The enhancement is increased to ~85% with a 4 nm InP cap.

Fig. 3.12 compares the off-state leakage current I_{OFF} versus drain current I_{Dsat} at V_{DS} of 1.2 V. More than 20 MOSFETs with L_G ranging from 0.35 to 2 μm were characterized for each device split. We observed I_{Dsat} enhancement of ~32% and ~50% over the control at a fixed I_{OFF} of 3×10^{-7} A/μm for MOSFETs with 2 nm and 4 nm InP capping layer, respectively.

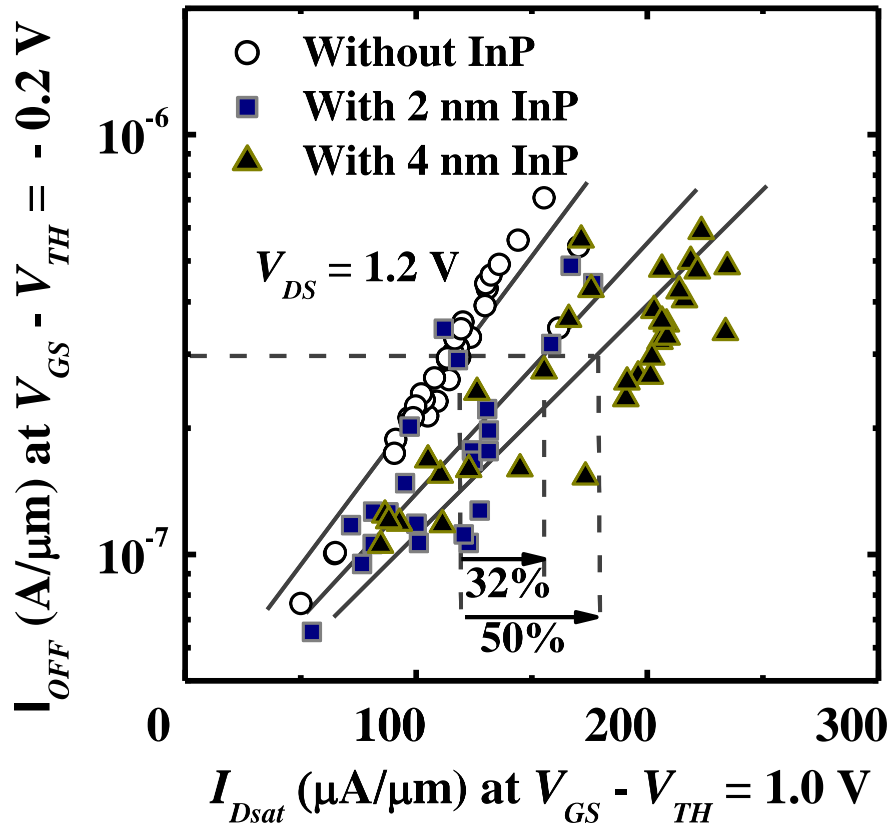


Fig. 3.12. Plot of off-state leakage current I_{OFF} versus on-state drain current I_{Dsat} at V_{DS} of 1.2 V, showing I_{Dsat} enhancement of ~32% and ~50% at a fixed I_{OFF} of 3×10^{-7} A/μm for N-MOSFETs with 2 nm and 4 nm InP cap, respectively. Gate length of devices measured ranges from 0.35 to 2 μm.

3.3 Self-Aligned Gate-First $In_{0.7}Ga_{0.3}As$ N-MOSFETs with Sub-400 °C Si_2H_6 Passivation and HfO_2 High-*k* Gate Dielectric

For InGaAs to be used as an N-MOSFET channel material in sub-11 nm technology nodes and beyond, an optimal gate stack requires not only a thermodynamically stable MOS stack with low interface trap density (D_{it}) but also small equivalent oxide thickness (EOT), i.e. sub-1 nm, with low gate leakage current. In this Section, we investigate a novel low temperature Si_2H_6 surface passivation technique to realize high-quality metal gate/high-*k* dielectric stack on $In_{0.7}Ga_{0.3}As$. By employing SF_6 treatment for native oxide removal and low temperature Si_2H_6 passivation, an ultra-thin SiO_2/Si interfacial passivation layer (IPL) was formed between high-*k* dielectric and $In_{0.7}Ga_{0.3}As$. This IPL could effectively passivate the $In_{0.7}Ga_{0.3}As$ surface. When integrated with the ALD deposited HfO_2 with a dielectric constant of ~20, $In_{0.7}Ga_{0.3}As$ N-MOSFETs with a capacitance equivalent thickness (CET) of ~1.6 nm were demonstrated.

3.3.1 Design Concept

The concept of inserting a SiO_2/Si layer between HfO_2 and $In_{0.7}Ga_{0.3}As$ is similar with that of InP discussed in Section 3.2. A high-quality Si passivation layer can be formed on $In_{0.7}Ga_{0.3}As$ by an ultra-high vacuum chemical vapor deposition (UHVCVD) tool. The 0.5 eV ΔE_C at the Si/$In_{0.7}Ga_{0.3}As$ interface confines the electron to flow in the $In_{0.7}Ga_{0.3}As$ channel, as shown in the band diagram across line B-B' of an $In_{0.7}Ga_{0.3}As$ N-MOSFET operated at strong inversion in Fig. 3.13.

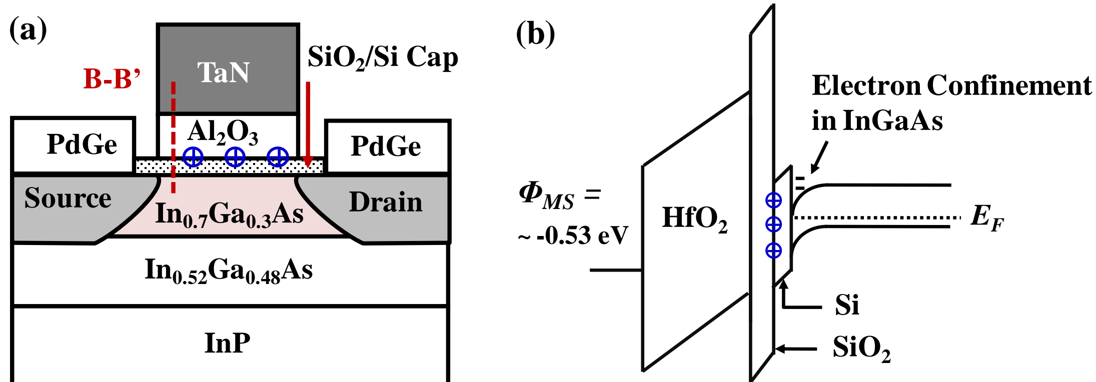


Fig. 3.13. (a) The schematic showing a Si_2H_6 passivated $In_{0.7}Ga_{0.3}As$ N-MOSFET. An ultrathin SiO_2/Si layer was formed between HfO_2 dielectric and the $In_{0.7}Ga_{0.3}As$ channel. (b) Band alignment across line B-B' of an $In_{0.7}Ga_{0.3}As$ MOSFET with Si_2H_6 passivation operated at strong inversion. The Si layer confines the electrons moving in the $In_{0.7}Ga_{0.3}As$ channel and moves the interface traps away from the channel. In addition, larger tunneling barrier height seen by electrons helps to reduce the gate leakage current as compared with HfO_2 alone.

Interface traps are now moved away from the channel, leading to reduced Coulomb scattering. In addition, an ultra-thin interfacial SiO_2 formed due to oxidation of a part of the Si layer helps to reduce the gate leakage current because of the larger tunneling barrier height for electrons as compared with HfO_2 alone.

3.3.2 Device Fabrication and Characterization

(a) Device Fabrication

Fig. 3.14 (a) shows the key steps for fabricating $In_{0.7}Ga_{0.3}As$ N-MOSFETs with the gate stack formation process highlighted in Fig. 3.14 (b). P-type (100)-oriented $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As/InP$ substrates were used. The doping concentration N_A of the 20-nm-thick $In_{0.7}Ga_{0.3}As$ channel layer is ~5×10^{16} cm^{-3}. The

pre-gate cleaning process for InGaAs comprises native oxide removal using diluted HCl ($HCl:H_2O$ = 1:3) for 3 minutes and excess elemental arsenic removal by ammonium hydroxide (NH_4OH) for 10 minutes.

After pre-gate cleaning, the InGaAs substrates were quickly loaded into an ultra-high vacuum tool equipped with a high-vacuum transfer module (base pressure of ~1×10^{-7} Torr) to prevent the formation of native oxide, which occurs rapidly upon exposure to low vacuum or atmosphere. SF_6 plasma treatment was first done at 300 °C for 50 s with a flow rate of 10 sccm in one chamber to remove native oxide which may have formed. Next, without breaking vacuum, Si_2H_6 treatment was carried out in a second chamber at 370 °C for 50 minutes with a flow rate of 50 sccm and at a base process pressure of ~1×10^{-7} Torr to form a high-quality Si passivation layer. This was followed by deposition of ~3.6 nm of HfO_2 at 250 °C in an ALD tool using tetrakis [dimethylamido] hafnium and H_2O as precursors, and N_2 as the carrier gas.

After reactive sputter deposition of ~ 100 nm TaN to form the gate electrode, gate lithography and gate etch using a Cl_2-based plasma process were performed. The source and drain regions were formed by implantation of Si at energy of 20 keV and a dose of 1×10^{14} cm^{-2}, and followed by an rapid thermal annealing (RTA) at 600 ºC for 60 s. Finally, CMOS-compatible PdGe were integrated to complete the device fabrication.

(a) Process Flow

- $In_{0.7}Ga_{0.3}As$ Grown on $In_{0.52}Al_{0.48}As$ on InP by MBE (External Vendor)
- Pre-gate Cleaning by HCl and NH_4OH
- ❶ Native Oxide Removal by SF_6 Plasma
  - Temperature: 300 °C
  - Duration: 50 s
  - SF_6 Flow Rate: 10 sccm
- ❷ Si_2H_6 Passivation
  - Temperature: 370 °C
  - Duration: 50 minutes
  - Si_2H_6 Flow Rate: 50 sccm
- ❸ ALD HfO_2 Deposition (3.6 nm)
- ❹ TaN Deposition
- Gate Definition
- S/D Implant and Dopant Activation
- PdGe Contact Formation

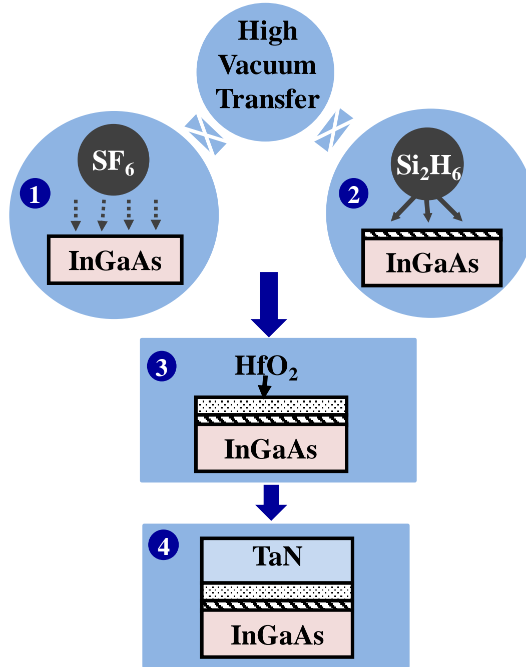


Fig. 3.14. (a) Process sequence showing the key steps employed to fabricate the $In_{0.7}Ga_{0.3}As$ N-MOSFETs. A low temperature Si_2H_6 passivation was incorporated. (b) Schematics illustrating the gate stack formation process. After the SF_6 treatment in the first chamber of a UHVCVD system for native oxide removal and low temperature Si_2H_6 passivation in a second chamber, the sample was then loaded into an ALD system for HfO_2 deposition, and followed by the TaN deposition in a reactive sputter tool.

(b) Materials Characterization

High-resolution XRD curves in Fig. 3.15 show that the indium composition in InGaAs is ~70%, with the film fully strained. In addition, well-defined $In_{0.7}Ga_{0.3}As$ peak indicates excellent crystalline quality of the channel material. Physical characterization using atomic force microscopy (AFM) was performed after the step of SF_6 treatment but before Si_2H_6 passivation to examine the morphology of InGaAs surface.

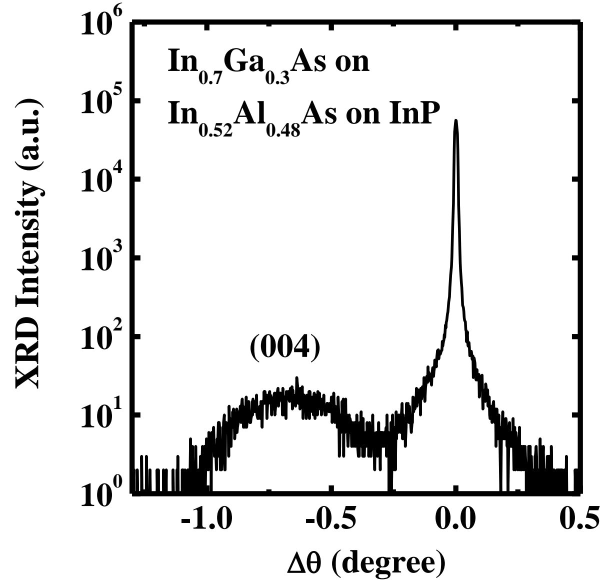


Fig. 3.15. High-resolution XRD curves show an indium composition of 70% in InGaAs. The well-defined $In_{0.7}Ga_{0.3}As$ peak indicates excellent crystalline quality of the channel material.

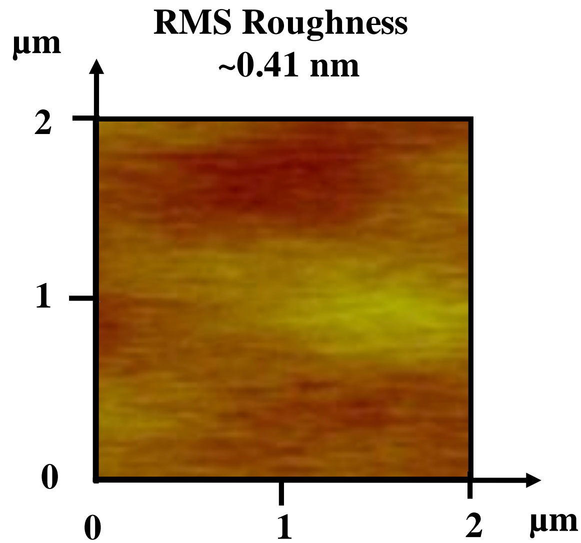


Fig. 3.16. AFM image of the $In_{0.7}Ga_{0.3}As$ surface after SF_6 treatment at 300 °C for 50 s. The AFM scan area is 2 µm by 2 µm. The small RMS roughness value indicates that good surface morphology was preserved after the native oxide removal by SF_6 treatment.

The SF_6 treatment removes the native oxides on InGaAs surface that might not be completely removed during pre-gate cleaning, but should not roughen the substrate surface as this would increase surface roughness scattering and reduce the high-field mobility in the transistors. The root-mean-square (RMS) surface roughness of InGaAs substrate after SF_6 treatment was measured to be ~0.41 nm, as shown in Fig. 3.16. RMS value of the sample before SF_6 treatment is ~0.35 nm. This indicates that a good surface morphology was preserved. TEM micrograph in Fig. 3.17 (a) shows the TaN/HfO_2/SiO_2/Si stack formed on $In_{0.7}Ga_{0.3}As$. Good uniformity and flat interface between SiO_2/Si cap and $In_{0.7}Ga_{0.3}As$ were observed._ The high-resolution TEM image in Fig. 3.17 (b) confirms the presence of an ultra-thin interfacial layer between the HfO_2 dielectric and $In_{0.7}Ga_{0.3}As$. The HfO_2 thickness is around 3.6 nm.

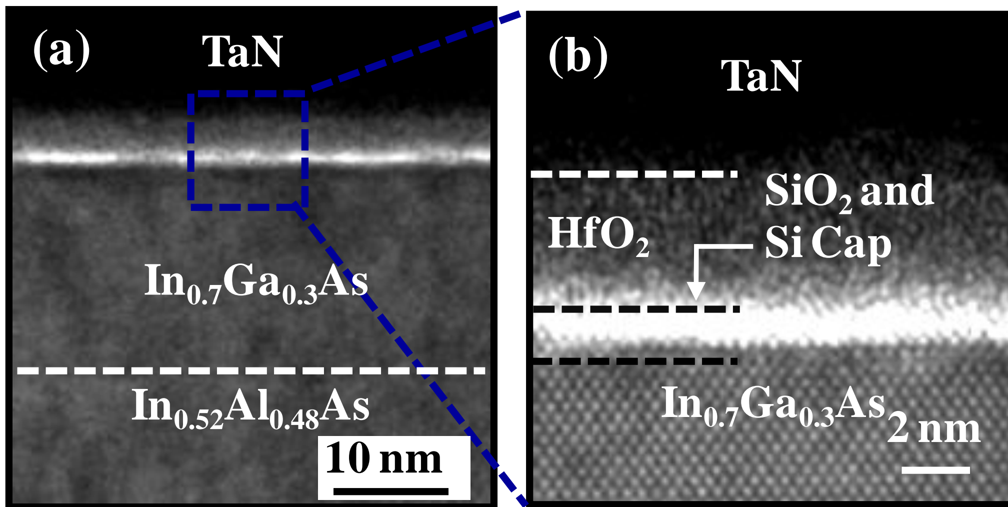


Fig. 3.17. (a) The cross-sectional TEM image of the TaN/HfO_2/SiO_2/Si gate stack on $In_{0.7}Ga_{0.3}As$. The high-resolution image in (b) reveals the existence of an ultra-thin SiO_2/Si interfacial layer between the HfO_2 and the $In_{0.7}Ga_{0.3}As$ channel material. HfO_2 is ~3.6 nm thick.

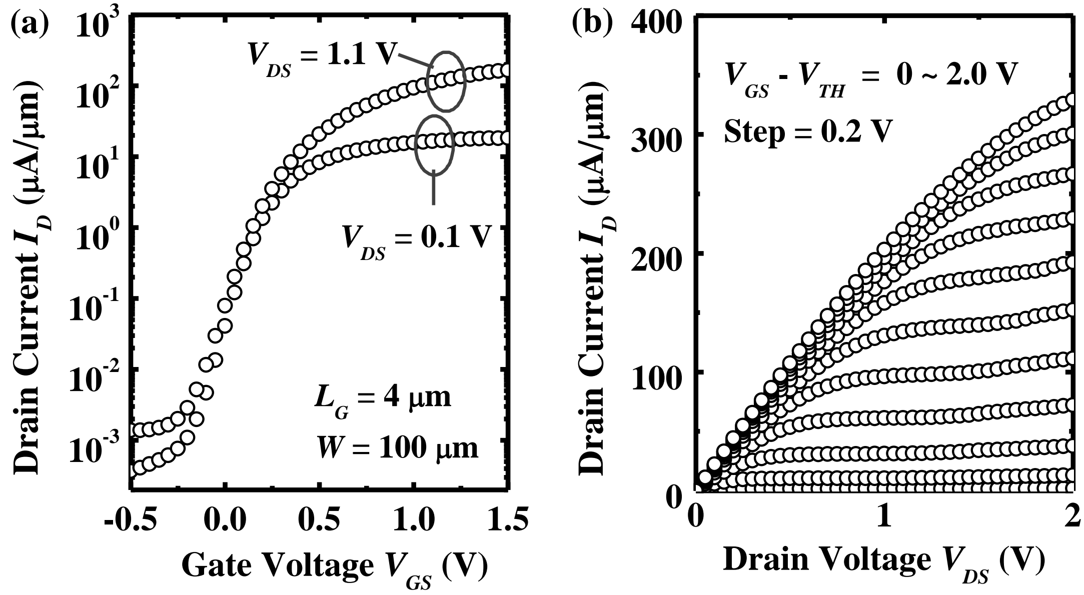


Fig3.18. (a) I_D-V_{GS} curves showing excellent transfer characteristics of an $In_{0.7}Ga_{0.3}As$ N-MOSFET. (b) I_D-V_{DS} output characteristics of the same transistor in (a). Very high drive current was achieved at a gate length L_G of 4 μm, attributed to the excellent interface quality due to Si_2H_6 passivation and the EOT scaling.

(c) Electrical Characterization

I_D-V_{GS} curves in Fig. 3.18 (a) show the excellent transfer characteristics of an $In_{0.7}Ga_{0.3}As$ N-MOSFET with subthreshold swing S of ~102 mV/decade. I_{on}/I_{off} ratio of ~5 orders was achieved and is attributed to the presence of a semi-insulating InAlAs layer under the InGaAs channel which reduces the transistor off-state leakage current. I_D-V_{DS} output characteristics of the same transistor are plotted in Fig. 3.18 (b). Excellent saturation and pinch-off characteristics were observed. The $In_{0.7}Ga_{0.3}As$ N-MOSFET shows drive current of ~320 μA/μm at V_{DS} and V_{GS}-V_{TH} of 2 V for a L_G of 4 μm. The high drive current achieved can be attributed to the good gate stack interface quality by low temperature Si_2H_6 passivation and the small EOT.

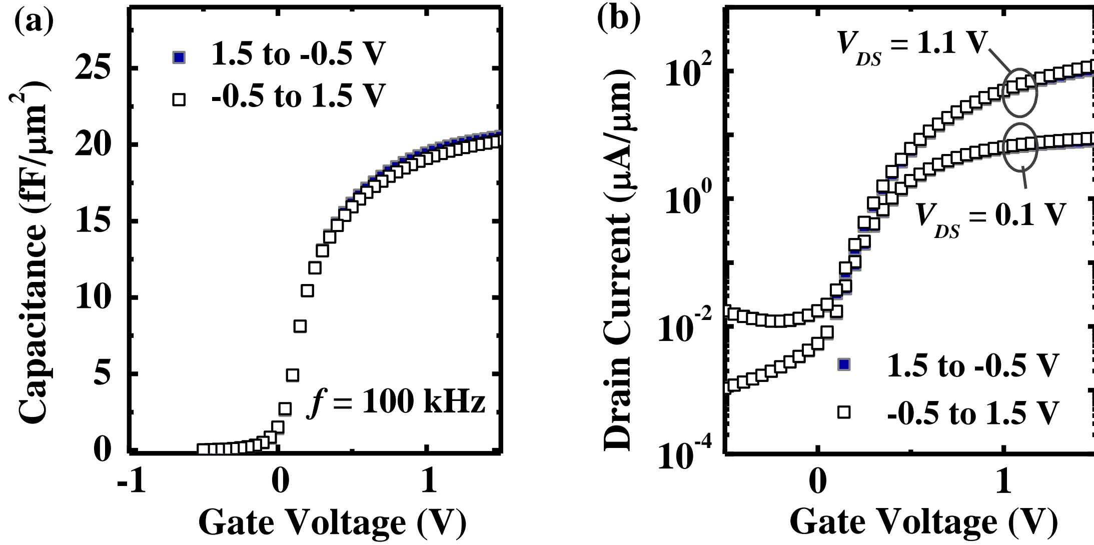


Fig. 3.19. (a) Inversion *C-V* curves measured at 100 kHz for InGaAs N-MOSFET yield a CET of ~1.7 nm. Forward and backward sweeps were applied to investigate the *C-V* hysteresis, which is found to be negligible. This indicates good interface and the gate dielectric quality and is consistent with the negligible hysteresis in the I_D-V_{GS} characteristics shown in (b).

Next, inversion *C-V* characteristics of the InGaAs N-MOSFET were investigated, as shown in Fig. 3.19 (a). The capacitance equivalent thickness of this MOSFET is ~1.7 nm. Due to the low density of states (DOS) in the Γ valley of InGaAs, the Fermi level can rise high above the conduction band edge at strong inversion, moving the charge centroid further away from the gate dielectric/channel interface for InGaAs as compared with Si. Therefore, the capacitance at strong inversion for InGaAs N-MOSFET might be smaller than that for Si N-MOSFET with the same EOT. In addition, this capacitance value for the InGaAs N-MOSFET might be larger than the theoretical calculated value that excludes interface trap density [109]. The D_{it} inside the conduction band of InGaAs N-MOSFETs was found to be high [109]. When these interface traps also respond to the AC signal during the *C-V*

measurement, higher capacitance value is expected. *C-V* curves show negligible hysteresis, consistent with the negligible hysteresis of the *I-V* curves in Fig. 3.19 (b). This indicates good gate dielectric quality with low density of oxide traps, as well as excellent interface quality due to low-temperature Si_2H_6 passivation.

The gate leakage current was measured by grounding the source and drain and applying voltage on the gate electrode. Gate leakage current density J_G of less than 10^{-4} A/cm^2 at a gate bias of $V_{TH}\pm1$ V was measured as shown in Fig. 3.20. Although the inserted SiO_2 has smaller permittivity and is thinner than HfO_2, the tunneling barrier seen by electrons is much higher for SiO_2 than for HfO_2. The low J_G indicates the potential for further scaling of the EOT which can be realized by scaling down the HfO_2 thickness.

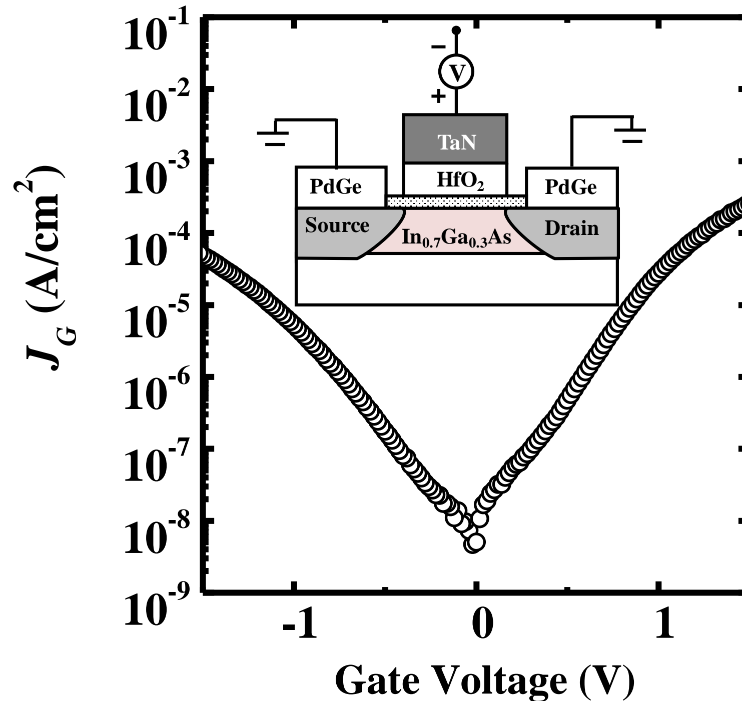


Fig. 3.20. Small gate leakage current density J_G was measured. J_G was normalized by gate area. There is potential for further scaling of the EOT.

Room temperature charge pumping analysis was conducted to evaluate the mid-gap D_{it}. The charge pumping characterization was performed by sweeping the base level V_{base} of constant- amplitude trapezoidal gate pulse train from accumulation level to inversion level. The amplitude V_A and frequency f of the gate pulses are 1 V and 200 kHz, respectively. Charge pumping current I_{CP} for trapezoidal gate pulse waveform [110] is expressed as

$$I_{CP} = 2qD_{it} fA_G kT \left[\ln\sqrt{t_r t_f} + \ln\left(\frac{|V_{FB} - V_{TH}|}{V_A} v_{th} n_s \sqrt{\sigma_n \sigma_p} \right) \right], \qquad (3.1)$$

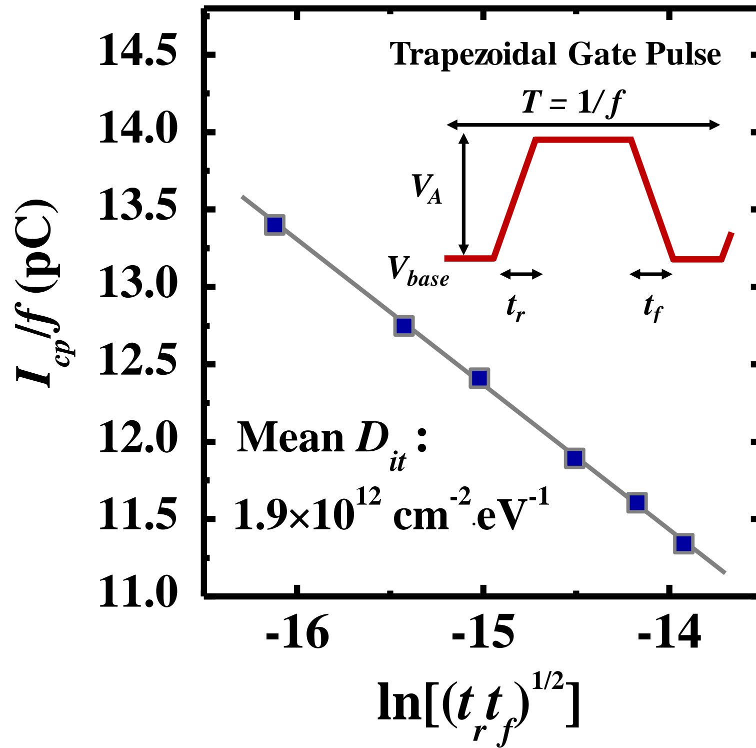


Fig. 3.21. Room temperature charge pumping measurement was performed to extract the mid-gap D_{it}. Constant-amplitude trapezoidal gate pulse train was swept from accumulation to inversion level with rise and fall time of gate pulses ranging from 100 ns to 1000 ns. By extracting the slope in I_{CP}/f as a function of $\ln[(t_r \cdot t_f)]$, the mean D_{it} of the InGaAs N-MOSFETs was obtained to be 1.9×10^{12} cm$^{-2}\cdot$eV^{-1}.

where q is electronic charge, A_G is transistor gate area, k is Boltzmann constant, V_{FB} is flatband voltage, V_{TH} is threshold voltage, v_{th} is the thermal velocity of the carriers, n_s is the surface concentration of minority carriers, σ_n and σ_p are capture cross sections of electrons and holes, respectively. The charge pumping current I_{CP} divided by f is plotted as a function of $\ln[(t_r \cdot t_f)]$ for equal trapezoidal pulse rise time t_r and fall time t_f, *with* t_r and t_f ranging from 100 to 1000 ns. Based on equation (3.1), the mean D_{it} over the energy range swept by the trapezoidal gate pulse with V_A of 1 V was extracted from the slope of I_{CP}/f versus $\ln[(t_r \cdot t_f)]$, as shown in Fig. 3.21. The mean D_{it} for the InGaAs N-MOSFET was found to be 1.9×10^{12} cm^{-2}·eV^{-1}.

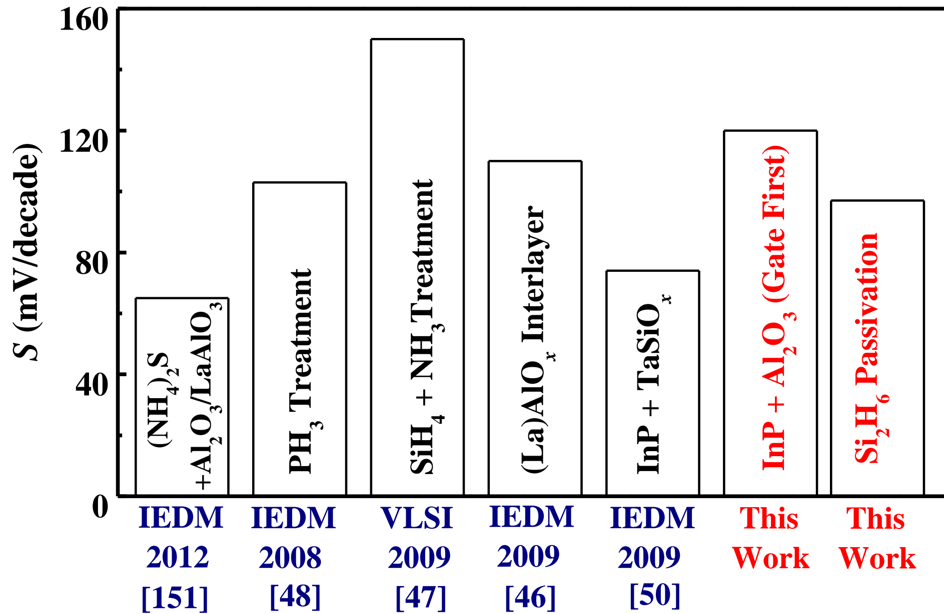


Fig. 3.22. Benchmarking of S of InGaAs N-MOSFETs achieved by different surface passivation techniques. Low-temperature Si_2H_6 passivation demonstrated in this work leads to the realization of InGaAs N-MOSFETs with S comparable to the best reported values. The S of the transistors with InP cap can be reduced by reducing EOT.

3.4 Comparison and Discussion of Two Advanced Gate Stack Techniques: InP Capping and Si_2H_6 Passivation

3.4.1 Benchmarking of Subthreshold Swing

Subthreshold swing is an important parameter to consider in the evaluation of the gate stack interface quality. Fig. 3.22 compares the effect of different passivation techniques in literature on the *S* of InGaAs N-MOSFETs. Low-temperature Si_2H_6 passivation demonstrated in Section 3.3 leads to the realization of InGaAs N-MOSFETs with *S* comparable to the best reported [46],[47],[48],[50],[151]. In Ref. 151, $(NH_4)_2S$ passivation was used to passivate the InGaAs surface before Al_2O_3 deposition to prevent the InGaAs from being oxidized during wafer transfer as well as ALD process. The first TMA pulse can help to reduce the native oxides further. In addition, three-dimensional structure was adopted. Volume inversion might happen with the nanowire dimension, which helps to mitigate the effect of interface traps on *S* of the transistors. In Ref. 47 and 48, $(NH_4)_2S$ passivation was also introduced. An interfacial layer was formed between the high-*k* and InGaAs to reduce the formation of InGaAs oxides. The concept used in Ref. 50 is similar to the concept introduced in this thesis. In their transistor fabrication, a gate last process was introduced to minimize the degradation of interface quality due to high thermal budget. In addition, $TaSiO_x$ with a permittivity of more than 25 was used as the high-*k* dielectric.

The *S* of the transistors with InP cap is slightly larger than that of Si_2H_6 passivated devices. This could be due to the larger thickness and smaller dielectric constant of Al_2O_3 as compared with HfO_2, leading to much larger C_{ox} for transistors with InP cap. The *S* of a MOSFET is given by

$$S = 2.3\frac{kT}{q}(1+\frac{C_{it}+C_D}{C_{ox}}), \quad (3.2)$$

where C_{ox} is the gate oxide capacitance, C_{it} is the capacitance due to interface traps and is given by qD_{it}, and C_D is the capacitance due to the substrate depletion layer. The S of the transistors with InP capping can be improved if Al_2O_3 thickness can be scaled down or a gate dielectric with higher permittivity is introduced.

3.4.2 Effect of InP or Si Thickness on the Drive Current of InGaAs N-MOSFETs

The effect of inserting an InP capping or Si layer on the drive current enhancement of InGaAs N-MOSFETs is significant, as evidenced by previous discussions. This is attributed to the improved carrier mobility. The drive current of a transistor with sub-100 nm L_G can be expressed as

$$I_{Dsat} = C_{ox}W(V_{GS} - V_{TH})\upsilon_{inj}, \quad (3.3)$$

where C_{ox} is the gate oxide capacitance, W is transistor width, and υ_{inj} is the carrier injection velocity at the source. υ_{inj} is correlated to the low field carrier mobility. Although the insertion of an InP cap or Si layer enhances the carrier mobility, it also decreases the C_{ox}. Therefore, an optimal InP or Si thickness should exist to give the largest product of C_{ox} and υ_{inj}, and thus drive current. In addition, the optimal InP or Si thickness strongly depends on the choice of high-k gate dielectrics as well as the high-k/InP or high-k/SiO_2/Si interface quality.

3.4.3 Comparison of Integration Challenges and Options for InP Capping and Si_2H_6 Passivation.

Table 3.1 shows a comprehensive comparison of the two advanced techniques in terms of the gate stack quality for higher drive current and better *S* as well as the integration challenges and options. Both InP capping and Si_2H_6 passivation are promising to achieve high quality interface between high-*k* and InGaAs channel, and have the potential to be scaled down to sub-1 nm EOT. In addition, both techniques are highly compatible with the high-*k* deposition tools in current Si technology. To be integrated into multi-gate structures to control short channel effects, a conformal layer of InP or Si is needed to wrap around the InGaAs channel. One advantage of the Si_2H_6 passivation is that it can also effectively passivate the Ge or GeSn surface for P-MOSFET. This provides a cost effective option for future CMOS application employing InGaAs as the n-channel material and Ge or GeSn as the p-channel material. Details of this point will be discussed in Section 4.4 of the next Chapter.

Table 3.1. Comparison of InP capping and Si_2H_6 passivation techniques in terms of the gate stack quality for higher drive current and better subthreshold characteristics as well as the integration challenges and options.

	Good Gate Stack Quality	Potential to Scale Down to Sub-1 nm EOT	Compatibility with High-*k* Dielectric Deposition Tools in Current Si Technology	Ease of Integration into Multi-gate Structure	Common Passivation Technique for Ge or GeSn P-FETs
InP Capping	Yes	Yes	Yes	Yes	No
Si_2H_6 Passivation	Yes	Yes	Yes	Yes	Yes

3.5 Summary

In this Chapter, two advanced gate stack techniques were explored for $In_{0.7}Ga_{0.3}As$ N-MOSFETs by a self-aligned gate-first process: InP capping or low temperature Si_2H_6 passivation.

To realize $In_{0.7}Ga_{0.3}As$ N-MOSFETs with InP capping, TMA treatment was first developed to achieve a good Al_2O_3/InP interface. The TaN/Al_2O_3 gate stack formed on InP/$In_{0.7}Ga_{0.3}As$ is thermally stable after a 600 ºC 60 s dopant activation anneal. Introducing 2 or 4 nm of InP capping layer in $In_{0.7}Ga_{0.3}As$ N-MOSFETs was found to reduce S, increase transconductance, and increase I_{Dsat}.

Next, low temperature Si_2H_6 passivation was investigated to effectively passivate the $In_{0.7}Ga_{0.3}As$ surface by forming an ultrathin SiO_2/Si interfacial layer with good surface morphology between HfO_2 and $In_{0.7}Ga_{0.3}As$. When integrated with the ALD deposited HfO_2, CET of ~1.7 nm was achieved with the gate leakage current density of less than 10^{-4} A/cm^2 in the gate voltage range of -1 to 1 V. Drive current as high as 320 μA/μm at V_{DS} and V_{GS}-V_{TH} of 2 V was achieved for a L_G of 4 μm, with S comparable to the best reported in the literature. These can be attributed to the good gate stack interface quality by low temperature Si_2H_6 passivation and the small EOT.

Finally, we compared and discussed the two advanced gate stack techniques in terms of the electrical characteristics and the integration challenges. Both techniques are promising options to realize high quality gate stack for high performance InGaAs channel N-MOSFETs.

Chapter 4

Germanium-Tin (GeSn) P-Channel MOSFETs with High Hole Mobility and Excellent NBTI Reliability Realized by Low Temperature Si_2H_6 Passivation

4.1 Introduction

While InGaAs has high electron mobility, and is attractive as an alternative channel material for n-channel metal-oxide-semiconductor field-effect transistors (N-MOSFETs), its bulk hole mobility is only ~400-500 $cm^2/V \cdot s$, and is similar to that of Si (~430 $cm^2/V \cdot s$) [111]. Ge offers superior bulk hole mobility of approximately 4 times higher than Si, making it promising as an alternative channel material for p-channel metal-oxide-semiconductor field-effect transistors (P-MOSFETs) for future high performance and low power logic application. In the past few years, various surface passivation techniques have been explored to realize high mobility Ge P-MOSFETs, with very good progress achieved [19]-[26], [112]-[121].

Recently, compressively strained GeSn channel P-MOSFETs have been shown to achieve higher hole mobility than Ge channel P-MOSFETs [27]-[29]. Development of high-*k*/GeSn gate stack with high-quality interface and small

capacitance equivalent thickness (CET) is needed to exploit the full potential of GeSn as a P-MOSFET channel material.

In this Chapter, we first investigated and compared the dependence of the electrical characteristics of (100)-oriented $Ge_{0.958}Sn_{0.042}$ P-MOSFETs on different surface passivation techniques: low temperature Si_2H_6 passivation or room temperature $(NH_4)_2S$ treatment of GeSn prior to high-*k* gate dielectric (HfO_2) deposition. A comprehensive study using GeSn channel having a fixed Sn composition and a given high-*k* gate dielectric was performed. Better subthreshold characteristics and higher drive current were achieved by low temperature Si_2H_6 passivation. The negative bias temperature instability (NBTI) reliability of Si_2H_6 passivated GeSn P-MOSFETs was then examined in Section 4.3. For cost effective integration in complementary metal-oxide-semiconductor (CMOS) fabrication, Section 4.4 developed a common gate stack solution for GeSn and InGaAs CMOS, featuring low temperature Si_2H_6 passivation, single TaN metal gate, and sub-1.75 nm CET. The key results of this Chapter are summarized in Section 4.5.

4.2 Si_2H_6 and $(NH_4)_2S$ Passivation Techniques and Effect on the Electrical Characteristics of GeSn P-Channel MOSFETs

4.2.1 GeSn Growth and Material Characterization

The starting substrate was a 4 inch n-type Ge(100) wafer. GeSn film was epitaxially grown on Ge using solid source molecular beam expitaxy (MBE) tool at 180 ˚C. After cleaning in dilute HF ($HF:H_2O$ = 1:10), the Ge wafer was loaded into the growth chamber and baked at 650 ˚C for 30 minutes for native oxide removal. The growth chamber has a very low base pressure of 3×10^{-8} Pa. After pre-epi baking, *in situ* reflection high-energy electron diffraction (RHEED) patterns revealed well-developed 2×1 reconstruction, indicating that the surface was free of native oxide and very smooth. $Ge_{1-x}Sn_x$ alloy was then grown by evaporating 99.9999% pure Ge and 99.9999% pure Sn from the effusion cells. The deposition rate of Ge and Sn can be adjusted by changing the temperature of effusion cells. The Ge deposition rate was maintained at ~0.022 nm/s, while the Sn deposition rate was set to obtain the desired Sn composition. The growth was monitored by the RHEED system. The above-mentioned MBE growth was performed by our collaborator at Chinese Academy of Sciences.

Fig. 4.1 shows a high-resolution transmission electron microscope (HRTEM) image of a 10 nm-thick $Ge_{0.958}Sn_{0.042}$ film grown on (100)-oriented Ge substrate. Defect-free $Ge_{0.958}Sn_{0.042}$/Ge interface was observed. High-resolution X-ray diffraction (XRD) curve in Fig. 4.2 shows the well-defined GeSn peak. The substitutional Sn composition of the GeSn film is ~4.2%. In addition, very smooth GeSn surface was observed, as indicated by the root-mean-square (RMS) surface

roughness of ~0.26 nm in the atomic force microscopy (AFM) image shown in Fig. 4.3.

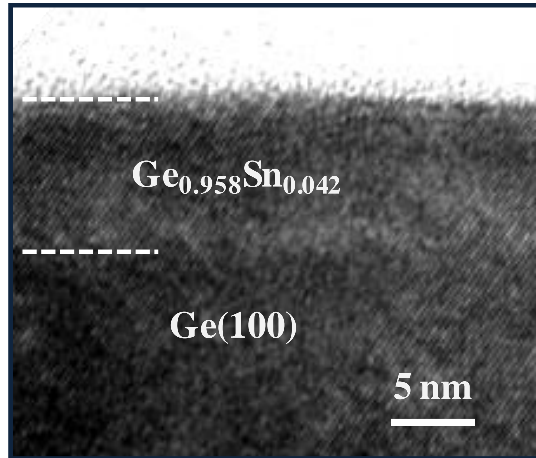


Fig. 4.1. High-resolution TEM image of a 10 nm-thick $Ge_{0.958}Sn_{0.042}$ film grown on (100)-oriented Ge substrate.

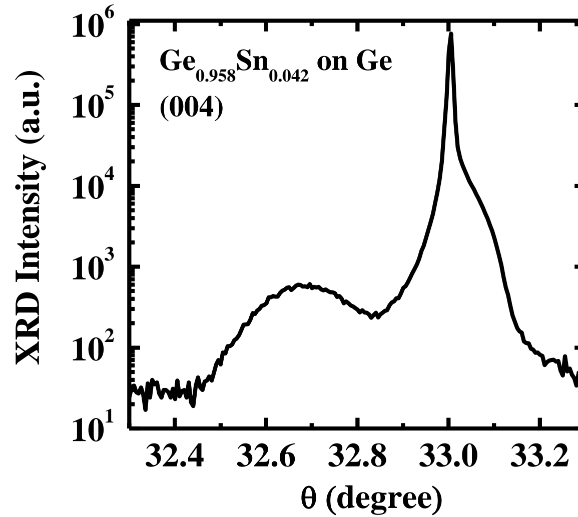


Fig. 4.2. High-resolution XRD (004) curve shows well-defined GeSn peak. The substitutional Sn composition of the GeSn film is ~4.2%.

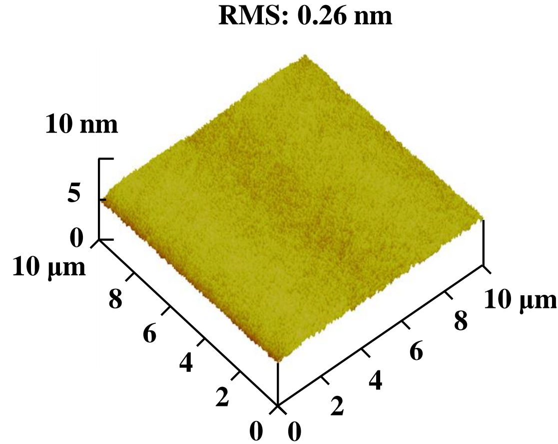


Fig. 4.3. AFM image shows the smooth surface of the as-grown GeSn film with RMS surface roughness of 0.26 nm. The scan area is 10 × 10 μm^2.

4.2.2 Fabrication of $Ge_{0.958}Sn_{0.042}$ P-MOSFETs

The process flow for fabricating $Ge_{0.958}Sn_{0.042}$ P-MOSFETs is illustrated in Fig. 4.4. After the growth of 10 nm-thick $Ge_{0.958}Sn_{0.042}$ film, phosphorus well implant was performed at energy of 20 keV and a dose of 5×10^{12} cm^{-2}, and activated at 450 °C for 3 minutes to convert the as-grown GeSn from p-type to n-type.

A cyclic clean was used for the pre-gate cleaning process of $Ge_{0.958}Sn_{0.042}$ substrates. This involves 5 cycles' treatment of the wafers, with deionized water for 30 s followed by HF acid (HF:H_2O = 1:50) for 30 s in each cycle. After that, two surface passivation splits were introduced. A first set of samples was passivated using $(NH_4)_2S$ solution for 10 minutes at room temperature. A second set of samples was immediately loaded into an ultra-high vacuum tool equipped with a high-vacuum transfer module (base pressure of ~1×10^{-7} Torr). SF_6 plasma treatment was first done at 300 °C for 50 s in one chamber to remove any native oxide that may have been formed. Next, without breaking vacuum, samples were transferred to the second

chamber where Si_2H_6 treatment was carried out at 370 °C for 120 minutes at a flow rate of 10 sccm to form a high-quality Si passivation layer.

All samples were then loaded into an atomic layer deposition (ALD) tool for the deposition of ~4.5 nm-thick HfO_2 at 250 °C using tetrakis hafnium and H_2O as precursors. This was followed by the reactive sputter deposition of 100 nm of TaN and 10 nm of SiO_2. After gate definition with optical lithography and a F-based plasma etch, 50 nm of SiO_2 was deposited and patterned to expose the active region, including source/drain (S/D) regions, and a portion of the gate pad. ~10 nm of Ni was then sputtered onto the samples and rapid thermal annealed at 350 °C for 30 s to form the NiGeSn metallic S/D. The device fabrication process was finally completed by selective removal of the unreacted Ni by concentrated H_2SO_4 solution.

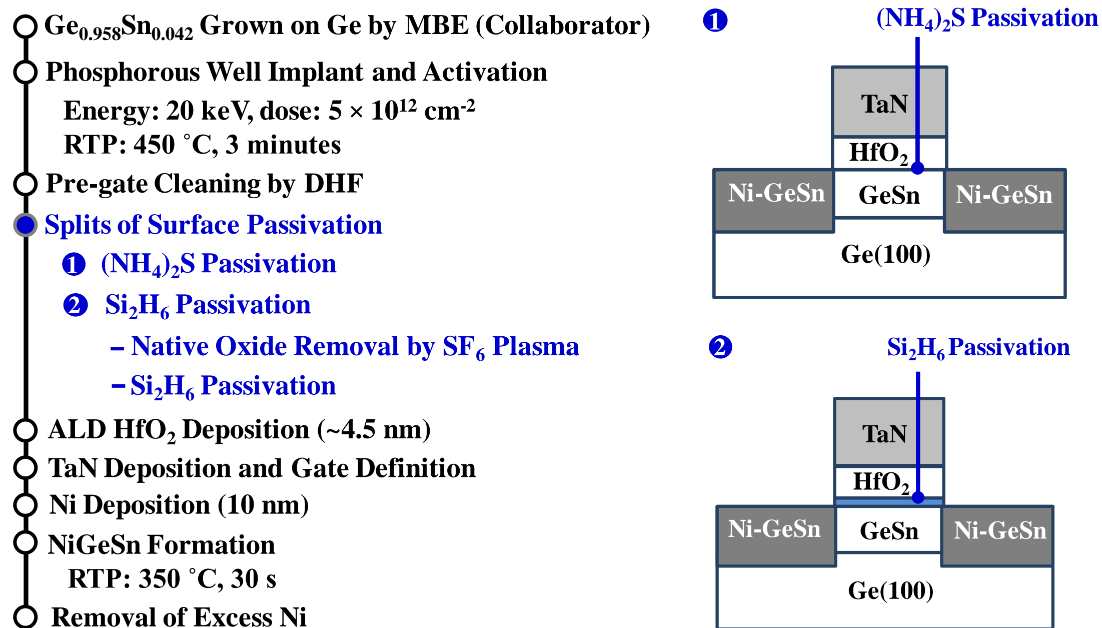


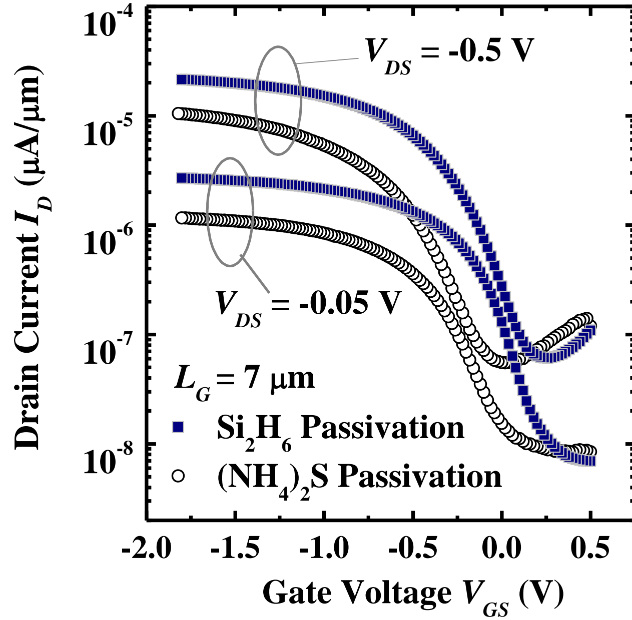
Fig. 4.4. The process flow for fabricating $Ge_{0.958}Sn_{0.042}$ P-MOSFETs. Two splits of surface passivation of $Ge_{0.958}Sn_{0.042}$ were introduced prior to HfO_2 deposition: low-temperature Si_2H_6 passivation or room temperature $(NH_4)_2S$ treatment. All steps were performed by the author except for the $Ge_{0.958}Sn_{0.042}$ growth.

4.2.3 Results and Discussion

Fig. 4.5 (a) shows the I_D-V_{GS} curves of a pair of $Ge_{0.958}Sn_{0.042}$ P-MOSFETs with Si_2H_6 passivation and $(NH_4)_2S$ passivation. Both transistors have a gate length L_G of 7 µm. The Si_2H_6-passivated transistor shows improved subthreshold swing S over the one with $(NH_4)_2S$ passivation. The threshold voltage V_{TH} of the $(NH_4)_2S$-passivated transistor is left-shifted as compared with that of the Si_2H_6-passivated one. This could be due to more positive fixed charges or more donor-like interface traps for the $(NH_4)_2S$-passivated transistor. I_D-V_{DS} output characteristics of the same pair of transistors are plotted in Fig. 4.5 (b). Good saturation and pinch-off characteristics were observed. Drive current of the device with Si_2H_6 passivation is 75% higher than that with $(NH_4)_2S$ passivation at a gate overdrive of -1.2 V and V_{DS} of -1.5 V.

Inversion C-V characteristics of $Ge_{0.958}Sn_{0.042}$ P-MOSFETs passivated by two different techniques are shown in Fig. 4.6. C-V curves were measured at a frequency of 100 kHz. The transistor with Si_2H_6 passivation shows 6 fF/µm^2 smaller inversion capacitance due to the additional SiO_2/Si interfacial layer formed. The CET of the Si_2H_6-passivated transistor was extracted to be ~1.82 nm, while that of the $(NH_4)_2S$-passivated transistor is ~1.38 nm. It could be possible that the native oxide of GeSn still exists at the HfO_2/GeSn interface for the $(NH_4)_2S$-passivated device.

Fig. 4.7 plots the cumulative distribution of the S of GeSn P-MOSFETs with two different passivation techniques. The devices have gate lengths ranging from 5 to 10 µm. $Ge_{0.958}Sn_{0.042}$ P-MOSFETs with Si_2H_6 passivation have a median S that is



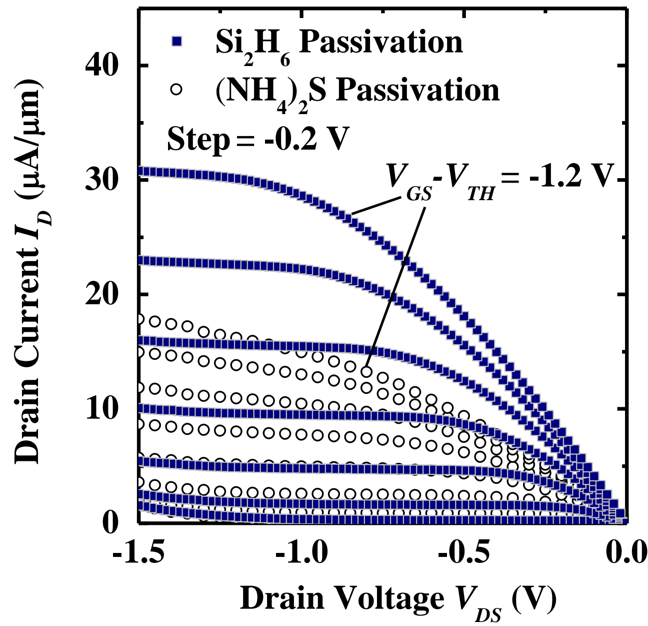


Fig. 4.5. (a) I_D-V_{GS} curves showing transfer characteristics of GeSn P-MOSFETs with Si_2H_6 passivation and $(NH_4)_2S$ treatment. Smaller S was observed for the Si_2H_6-passivated transistor, indicating a lower mid-gap interface trap density. (b) I_D-V_{DS} characteristics show that the Si_2H_6-passivated GeSn P-MOSFET has 75% higher drive current than the $(NH_4)_2S$-passivated device at a gate over drive of -1.2 V and V_{DS} of -1.5 V.

~50 mV/decade lower than that of transistors with $(NH_4)_2S$ passivation. The subthreshold swing of a MOSFET is given by

$$S = 2.3\frac{kT}{q}(1+\frac{C_{it}+C_D}{C_{ox}}), \tag{4.1}$$

where C_{ox} is the gate oxide capacitance, C_{it} is the capacitance due to interface traps and is given by qD_{it}, and C_D is the capacitance due to the substrate depletion layer. With the same amplitude of C_D and smaller C_{ox} for the Si_2H_6-passivated device as compared with that of the $(NH_4)_2S$-passivated device, the reduced S clearly shows that Si_2H_6 passivation could achieve much better interface quality with smaller mid-gap interface trap density between HfO_2/GeSn.

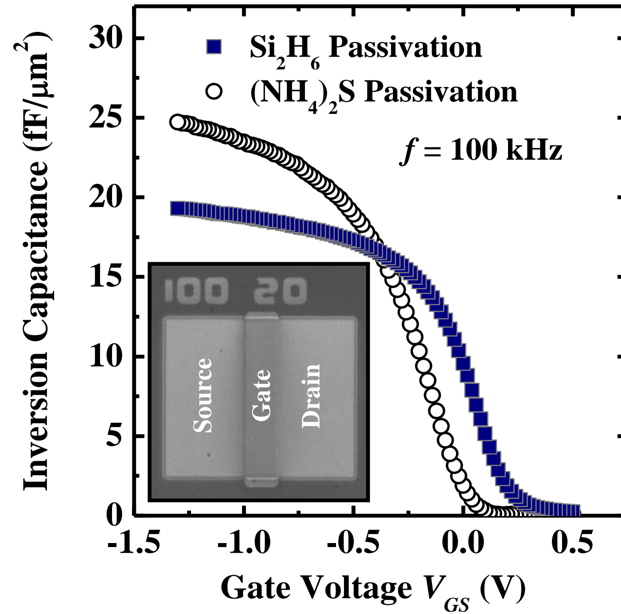


Fig. 4.6. Inversion *C-V* characteristics of $Ge_{0.958}Sn_{0.042}$ P-MOSFETs with Si_2H_6 passivation and $(NH_4)_2S$ treatment. The Si_2H_6-passivated device shows 6 fF/μm^2 smaller inversion capacitance due to the formation of the ultrathin SiO_2/Si interfacial layer. CET values were extracted to be ~1.82 and ~1.38 nm for Si_2H_6-passivated transistor and $(NH_4)_2S$-passivated one, respectively. The SEM image shows the layout of a GeSn transistor.

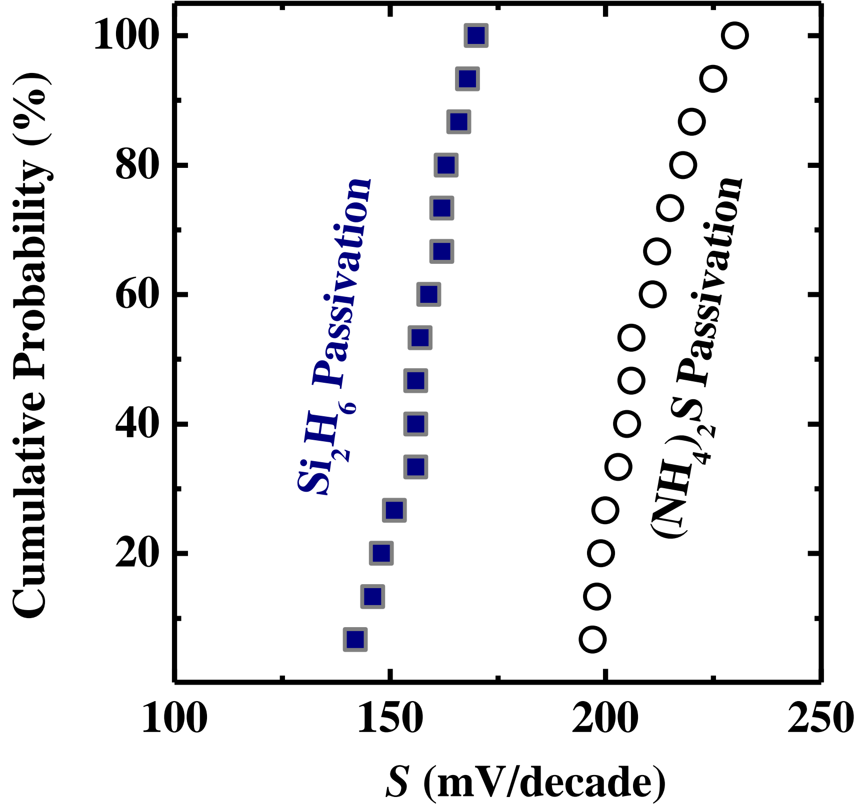


Fig. 4.7. Despite a smaller C_{ox}, GeSn P-MOSFETs with Si_2H_6 passivation have a median S that is ~50 mV/decade lower than that of transistors with $(NH_4)_2S$ passivation. The S was extracted at V_{DS} of -50 mV.

Fig. 4.8 shows the effective carrier mobility μ_{eff} of $Ge_{0.958}Sn_{0.042}$ P-MOSFETs as a function of the inversion carrier density N_{inv}. μ_{eff} was extracted by using the I_D-V_{GS} characteristics at a low V_{DS} of -50 mV, and N_{inv} in the channel was obtained by integrating the measured inversion C-V curves shown in Fig. 4.6. We observed much higher hole mobility for Si_2H_6-passivated device in the entire N_{inv} range. Insertion of a Si layer provides high-quality Si/GeSn interface and, at the same time, moves the interface traps further away from the channel, leading to reduced carrier scattering due to interface trap charges. Therefore, despite a slightly larger CET, Si_2H_6-

passivated devices have significant drive current improvement over the $(NH_4)_2S$-passivated device, as shown in Fig. 4.5 (b). The enhancement in mobility is larger at low inversion carrier density. At high inversion carrier density, the trapped charges at the interface are screened by the inversion carriers. This mitigates the effect of interface traps on the mobility.

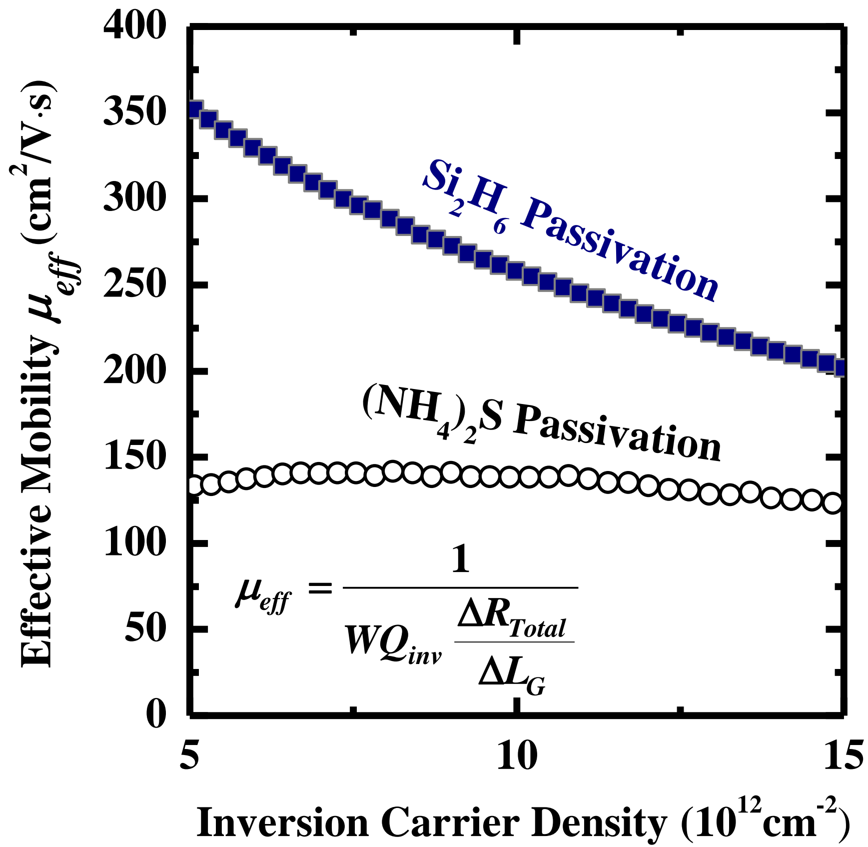


Fig. 4.8. μ_{eff} versus inversion carrier density N_{inv} of the GeSn P-MOSFETs with Si_2H_6 passivation and $(NH_4)_2S$ passivation. Si_2H_6-passivated devices show higher hole mobility in the entire N_{inv} range.

Fig. 4.9 (a) and (b) compare the effect of different passivation techniques on the subthreshold swing and effective carrier mobility of GeSn P-MOSFETs, respectively. The effective mobility is taken at N_{inv} of $1\times10^{13}/cm^2$, which is the typical value of the state-of-the-art Si MOSFET when the device is in the 'on' state. Low-temperature Si_2H_6 passivation in this work enables the realization of GeSn P-MOSFETs with the smallest S and highest hole mobility reported so far.

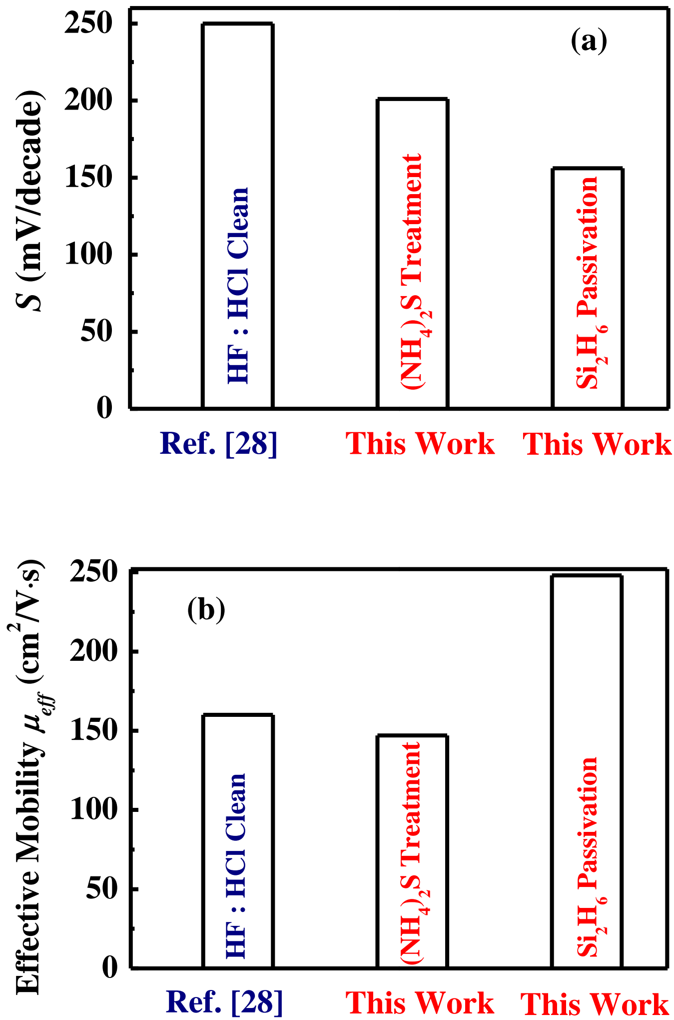


Fig. 4.9. Low temperature Si_2H_6 passivation in this work enables the realization of GeSn P-MOSFETs with (a) the smallest S and (b) highest hole mobility reported.

4.3 Negative Bias Temperature Instability Study of Si_2H_6 Passivated GeSn P-MOSFETs

The phenomenon of negative bias temperature instability (NBTI) has been known since 1966 [122]. It has been a persistent reliability concern for CMOS technology for generations because of increased gate electric field due to the scaling of CET as well as increased chip operating temperature [123]. For a P-MOSFET operated at strong inversion regime, as shown in Fig. 4.10, NBTI results from creation of both interface trap states (D_{it}) and oxide trapped charges (D_{ot}) by a negative bias at elevated temperature. As a result, transistors exhibit changes in electrical characteristics over time [124],[125]. A typical observation is the shift of the threshold voltage. It depends on temperature, oxide electric field and stress time, and can expressed by

$$\Delta V_{TH} = A e^{\gamma E_{ox}} e^{-E_A/kT} t^n , \quad (4.2)$$

where A is a constant, γ the electric field factor, E_{ox} is the oxide electrical filed, E_A the activation energy and n the time exponent. The shift of threshold voltage is also accompanied by the degradation of mobility, drive current and transconductance.

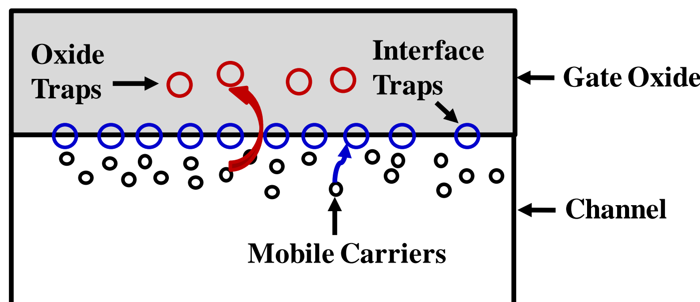


Fig. 4.10. The schematic showing the mechanism of NBTI under stress due to creation of interface trap states and oxide trapped charges by a negative bias.

Although GeSn P-MOSFETs have been demonstrated with different surface passivation techniques and high-*k* dielectrics, there has been no study on the NBTI reliability of GeSn P-MOSFETs so far. In Section 4.2, we demonstrated that the low temperature Si_2H_6 passivation is a promising option to realize high performance GeSn P-MOSFETs. In this Section, the first investigation of NBTI study on GeSn P-MOSFETs with Si_2H_6 passivation was further performed. The transistors show excellent NBTI reliability with small shift of V_{TH}, and negligible degradation of S and peak transconductance.

4.3.1 NBTI Characterization Method

NBTI stress measurement was performed using the measure-stress-measure technique [125]. The set-up for the observation of NBTI degradation is schematically depicted in Fig. 4.11. The source, drain and substrate contacts were grounded, while the gate was negatively biased. Devices were stressed with several gate overdrive conditions, and up to 1000 s of stress time. Due to the symmetry of source and drain, no channel hot carriers were generated. For channel material with small bandgap, the source and drain junction leakage is usually high. If only the drain current is traced, the effect of gate stack quality degradation on the electrical characteristics of a transistor, i.e. off-state leakage current and subthreshold swing, could be masked by the high junction leakage current. Therefore, in this study, stress was interrupted at various stress durations, and source current as a function of gate voltage was measured to monitor the degradation of the gate stack quality.

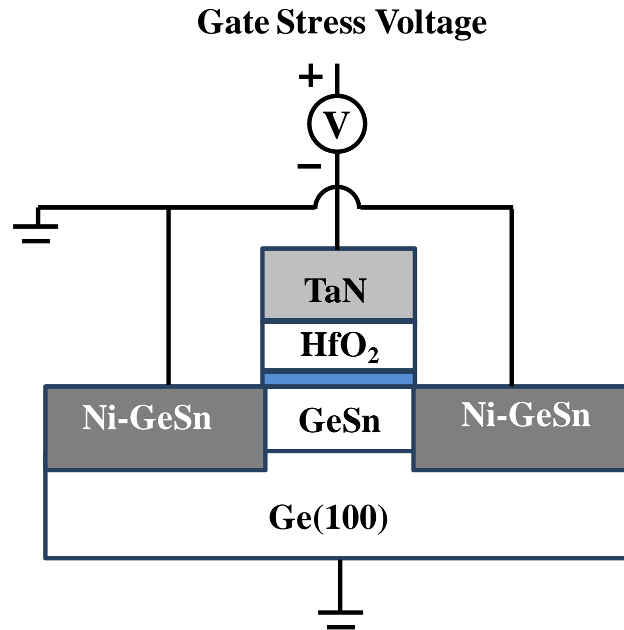


Fig. 4.11. The set-up for NBTI measurement. The gate was negatively biased while the source, drain and substrate contacts were grounded. Gate stress voltage was applied at room temperature, and source current as a function of gate voltage was measured at different stress durations. Due to the symmetry of the source and drain, no channel hot carriers are generated.

4.3.2 Results and Discussion

Shown in Fig. 4.12 are the I_S-V_{GS} curves at linear region (V_{DS} = -0.05 V) of a GeSn P-MOSFET measured under V_{GS} stress of -2.0 V for various stress durations. The transistor has gate width of 100 μm and gate length of 7 μm. Very small degradation in off-state leakage current and S after 1000 s stress was observed. As illustrated in Equation 4.1, the S of a transistor depends strongly on the number of interface trap density near the mid-gap which is swept across when the P-MOSFET goes from accumulation to inversion. The small change in S indicates that few interface traps were generated near the mid-gap during the NBTI stress.

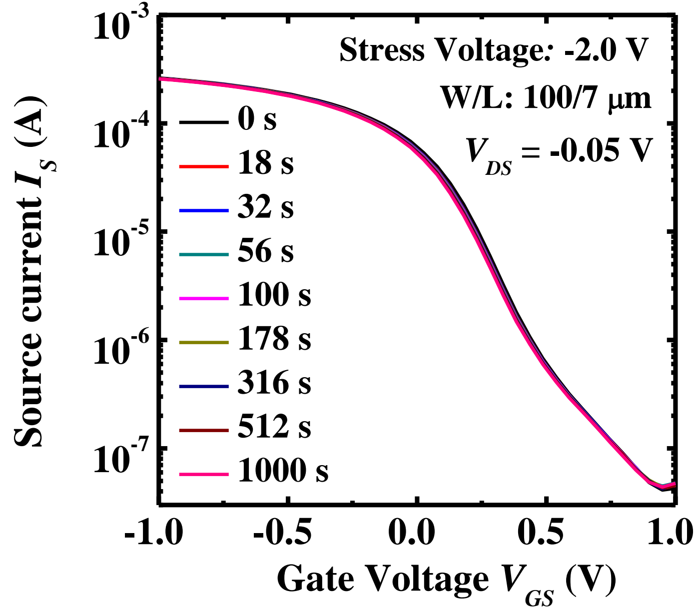


Fig. 4.12. I_S-V_{GS} curves at V_{DS} of -0.05 V of a GeSn P-MOSFET measured after V_{GS} stress of -2.0 V for various stress durations. Very small degradation in off-state leakage current and *S* after 1000 s stress was observed, indicating that very few interface traps were generated near the conduction band and mid-gap during NBTI stress.

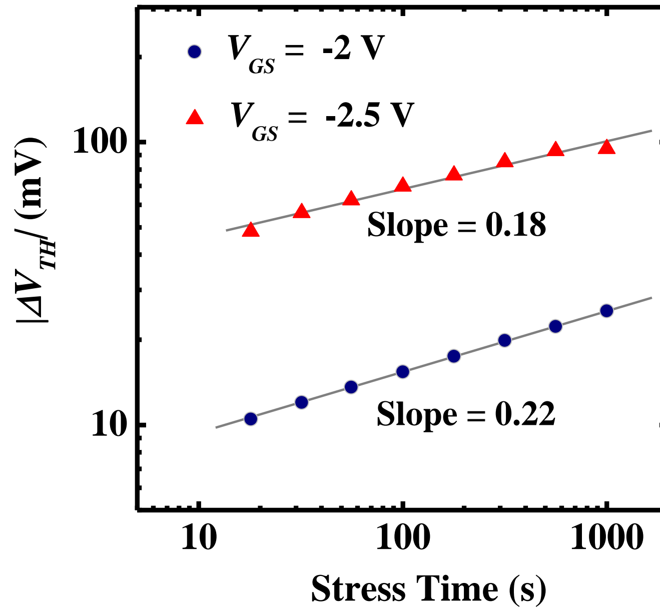


Fig. 4.13. The threshold voltage shift ΔV_{TH} as a function of stress time at two different stress voltages shows power law dependence on time.

Fig. 4.13 shows the V_{TH} shift ΔV_{TH} of GeSn P-MOSFETs as a function of stress time with two gate stress voltages. V_{TH} was extracted at a constant current of 10^{-5} A. The V_{TH} measured at different stress voltages shifts toward the negative direction, indicating that positive charges were generated during the stress. In addition, ΔV_{TH} shows power law dependence on time, as predicted by the Equation 4.2. The time exponent n of the V_{TH} shift under V_{GS} stress of -2 and -2.5 V is 0.22 and 0.18, respectively. The time exponent is not strongly dependent on the magnitude of the stress voltage, which suggests that few oxide traps were generated in the range of stress biases used for this study [126]. This is consistent with the negligible hysteresis observed in the inversion *C-V* characteristics of a GeSn P-FET, as shown in the Fig. 4.14.

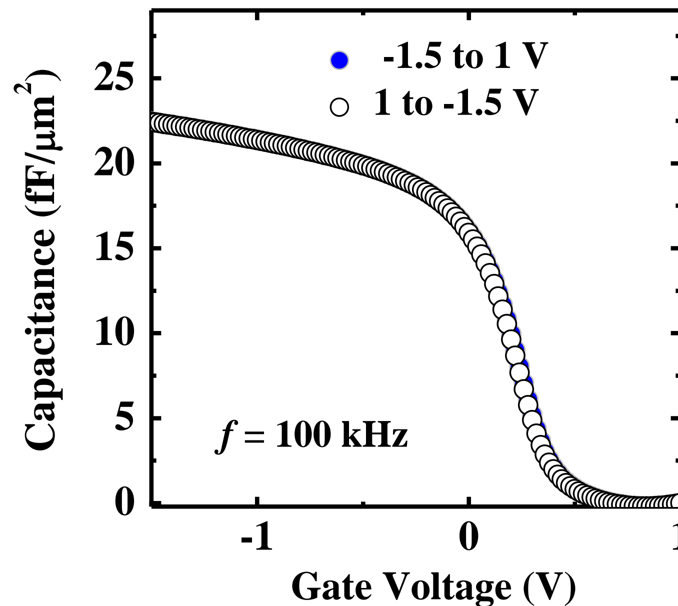


Fig. 4.14. Negligible hysteresis was observed in the inversion *C-V* characteristics of a GeSn P-MOSFET measured at frequency of 100 kHz. This indicates excellent gate dielectric quality with few oxide traps and mobile charges.

The P-MOSFET threshold voltage is given by

$$V_{TH} = \varphi_{MS} - 2\varphi_F - \frac{Q_S}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{it}(2\phi_F)}{C_{ox}}, \tag{4.3}$$

where Φ_{MS} is the work function difference between the gate and channel material, Φ_F is the Fermi potential, Q_S is the semiconductor charge density, Q_{ox} is the positive oxide charge density, C_{ox} is the oxide capacitance per unit area. Q_{it}, shown to be dependent on the surface potential, is given by

$$Q_{it} = qD_{it}\Delta E = qN_{it}, \tag{4.4}$$

where ΔE is the energy range over which interface traps are active.

Since neither gate nor substrate doping density nor oxide thickness changes during stress, the shift of threshold voltage should be due to change in Q_{ox} and Q_{it}

$$\Delta V_{TH} = -\frac{\Delta Q_{ox} + \Delta Q_{it}}{C_{ox}} = -\frac{q(\Delta N_{ox} + \Delta N_{it})}{C_{ox}}. \tag{4.5}$$

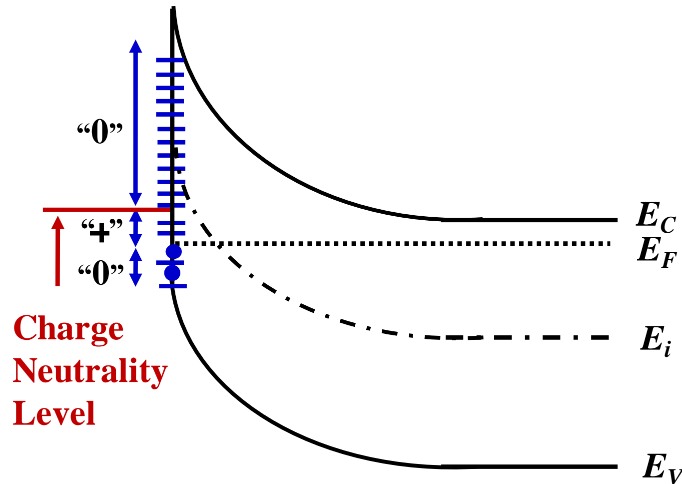


Fig. 4.15. Band diagram of the GeSn P-MOSFET channel showing the occupancy of interface traps and various charge polarities with net positive interface trap charges at inversion. Each of the small horizontal line represents an interface trap. It is either occupied by an electron (solid circles) or occupied by a hole (unoccupied by an electron).

Interface traps are electrically active defects with an energy distribution throughout the GeSn bandgap. They act as generation/recombination centers and contribute to increased leakage current as well as reduced mobility, drain current, and transconductance. Since the electrons or holes occupy interface traps, they become charged and contribute to threshold voltage shift. The surface potential dependence of the occupancy of interface traps of a GeSn P-MOSFET is illustrated in Fig. 4.15.

In this band diagram, the charge neutrality level E_{CNL} of GeSn is drawn to be close to the valence band E_V as researchers reported that E_{CNL} of Ge lies around 0.09 eV above the valence band [127]. For simplicity, we assume that interface traps located above E_{CNL} are acceptor-like, and donor-like for those located below E_{CNL}. Therefore, for a GeSn P-MOSFET at strong inversion as shown in Fig. 4.15, with electrons occupying states below the Fermi energy, the states above the E_{CNL} are neutral (unoccupied acceptors designated by "0"). The states between E_V and E_F are also neutral (occupied donors designated by "0"). However, the fraction of interface traps between the Fermi level and E_{CNL} is unoccupied donors, leading to positively charged interface traps (designated by "+"). As a result, interface traps in GeSn P-MOSFETs generated during NBTI stress are positively charged at strong inversion, leading to negative threshold voltage shift [128],[129].

Oxide charges can consist of various entities, including mobile charges, oxide trapped charges, i.e., electrons and/or holes, and fixed charges. Oxide charges are located within the oxide and may communicate with the conduction and valence bands of the channel material. However, it is generally believed that hole trapping is the dominant mechanism and that the hole traps or their precursors may exist in the

insulator prior to the stress [124]. The traps are positively charged when occupied by holes and neutral when unoccupied.

M. F. Li *et al.* demonstrated that there are two degradation components under stress: a ΔV_{TH}^{ox} component caused by oxide trapped charges, and a ΔV_{TH}^{it} due to interface trap generation [130]. The former component has a power law slope of ~0.05, and the later has a slope of ~0.17. The power low slope of GeSn P-MOSFETs under NBTI stress in this study is ~0.18-0.22, which is close to 0.17. The time delay between stress and measurement in this expeiremnt is 3 ms. This indicates that the dominant degradation mechanism could be the generation of interface traps.

Shown in Fig 4.16 is the transconductance at linear region $G_{M, Lin}$ as a function of V_{GS} measured under NBTI stress of -2.0 V for various stress durations. Since the peak $G_{M, Lin}$ is strongly affected by D_{it} near the valence band of GeSn, very small degradation in peak $G_{M, Lin}$ suggests that few interface traps were generated near GeSn valence band.

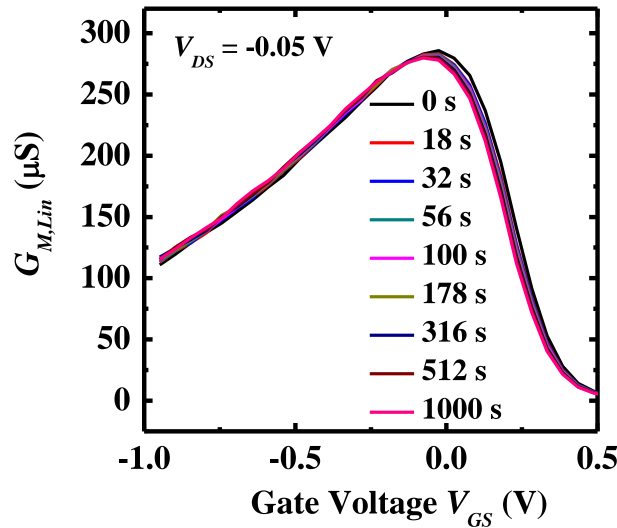


Fig. 4.16. Very small degradation in peak $G_{M, Lin}$ suggests that few interface traps were generated near the GeSn valence band under NBTI stress.

4.4 Towards High Performance $Ge_{1-x}Sn_x$ and $In_{0.7}Ga_{0.3}As$ CMOS: Common Gate Stack Featuring Sub-400 °C Si_2H_6 Passivation, Single TaN Metal Gate, and Sub-1.75 nm CET.

As discussed previously, InGaAs and GeSn, due to their high electron mobility and high hole mobility, respectively, would be a good combination as alternative channel materials to replace strained silicon for high performance and low power CMOS application beyond 11 nm technology node. In addition, low temperature Si_2H_6 treatment could effectively passivate both InGaAs and GeSn surfaces. For cost-effective integration in CMOS fabrication, a common surface passivation and gate stack formation process is preferable. In this Section, we demonstrate low-temperature Si_2H_6 treatment as a common passivation technique for $In_{0.7}Ga_{0.3}As$ N-MOSFETs and $Ge_{0.97}Sn_{0.03}$ P-MOSFETs. In addition, a common gate stack formation process, featuring ALD-deposited HfO_2 and single TaN metal gate, was also incorporated. The $Ge_{0.97}Sn_{0.03}$ P-MOSFET and $In_{0.7}Ga_{0.3}As$ N-MOSFET show drive currents of ~65 and ~131 µA/µm, respectively, at $|V_{DS}|$ and $|V_{GS}-V_{TH}|$ of 1 V for a gate length L_G of 4 µm. At an inversion carrier density N_{inv} of 10^{13} cm^{-2}, $Ge_{0.97}Sn_{0.03}$ P-MOSFETs and $In_{0.7}Ga_{0.3}As$ N-MOSFETs show hole and electron mobilities of ~230 and ~495 cm^2/V·s, respectively. At N_{inv} of 10^{13} cm^{-2}, hole and electron mobility values of ~346 and ~705 cm^2/V·s were achieved. Symmetric V_{TH} was realized by choosing a metal gate with mid-gap work function, and CET of less than 1.75 nm was demonstrated with gate leakage current density (J_G) of less than 10^{-4} A/cm^2 at a gate bias of V_{TH}±1 V.

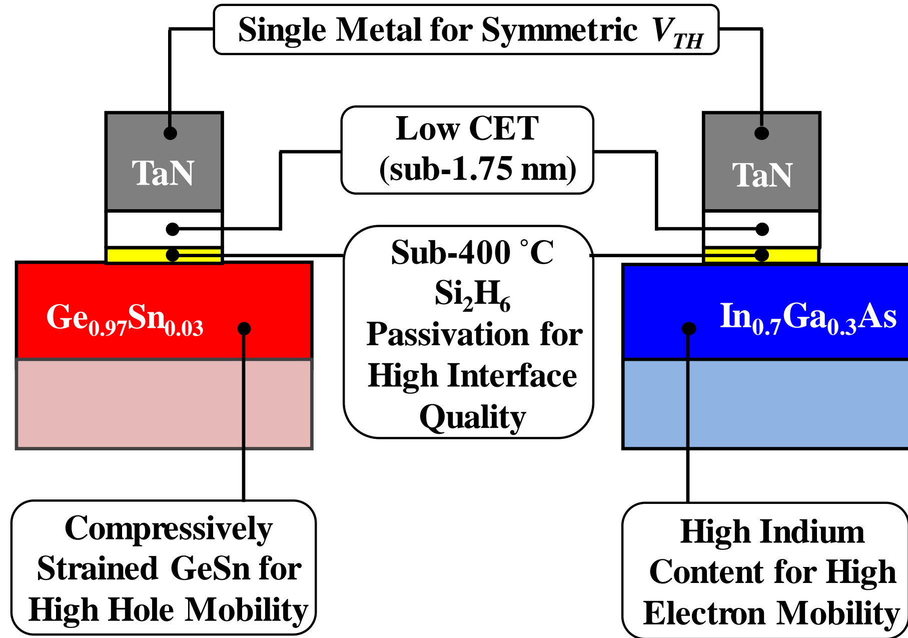


Fig. 4.17. Key highlights of the common gate stack technology for $Ge_{0.97}Sn_{0.03}$ P-MOSFETs and $In_{0.7}Ga_{0.3}As$ N-MOSFETs. Channel materials were selected for scaling up MOSFET performance, and also to enable achievement of symmetric V_{TH} using a single TaN metal gate.

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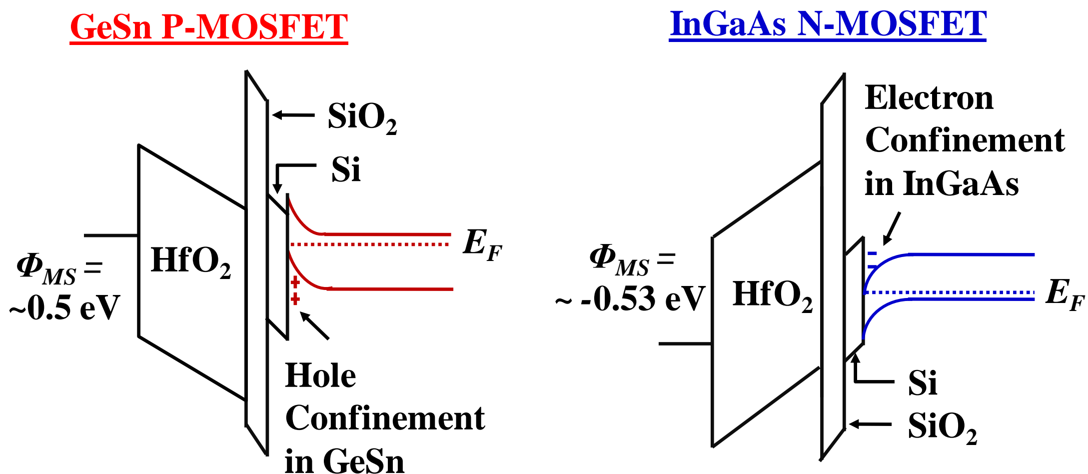


Fig. 4.18. Band alignments of the GeSn P-MOSFET and InGaAs N-MOSFET operating in the strong inversion regime. Si_2H_6 passivation technique was used to achieve high interface quality, transport carrier confinement, and low gate leakage current.

4.4.1 Design Concept of $TaN/HfO_2/SiO_2/Si$ Stack on InGaAs and GeSn

Key features of the novel gate stack technology are shown in Fig. 4.17. First, $Ge_{0.97}Sn_{0.03}$ and $In_{0.7}Ga_{0.3}As$ were chosen as the channel materials for P- and N-MOSFETs, respectively. Second, low CET for high-performance transistors was realized by introducing HfO_2 with high permittivity (~20) in this work.

Third, sub-400 °C Si_2H_6 treatment was used to passivate the interface between the gate dielectric and the channel. Fig. 4.18 illustrates the band alignments of the Si_2H_6-passivated GeSn P-MOSFET and InGaAs N-MOSFET operating in the strong inversion regime. The ~0.5 eV valence band offset (ΔE_V) at the $Si/Ge_{0.93}Sn_{0.03}$ interface confines the flow of holes in the $Ge_{0.93}Sn_{0.03}$ channel, and ~0.6 eV conduction band offset (ΔE_C) at the $Si/In_{0.7}Ga_{0.3}As$ interface confines the electron flow in the $In_{0.7}Ga_{0.3}As$ channel. The values of ΔE_V and ΔE_C were obtained by calculation without the consideration of the strain effect between Si and $Ge_{0.97}Sn_{0.03}$ or $In_{0.7}Ga_{0.3}As$ [131]. Insertion of a Si layer provides high-quality $Si/In_{0.7}Ga_{0.3}As$ and $Si/Ge_{0.93}Sn_{0.03}$ interfaces and, at the same time, moves the interface traps further away from the channel, leading to reduced carrier scattering. In addition, an ultra-thin interfacial SiO_2 formed due to oxidation of part of the Si layer helps to reduce the gate leakage current because of the larger tunneling barrier height for both holes and electrons as compared with HfO_2 alone.

Last, a single metal gate material (TaN) with a work function of ~4.6 eV was chosen to achieve symmetric V_{TH}, as shown in the plot of calculated flat-band voltage (V_{FB}) as a function of metal work function (Φ_M) in Fig. 4.19. In the calculation, the

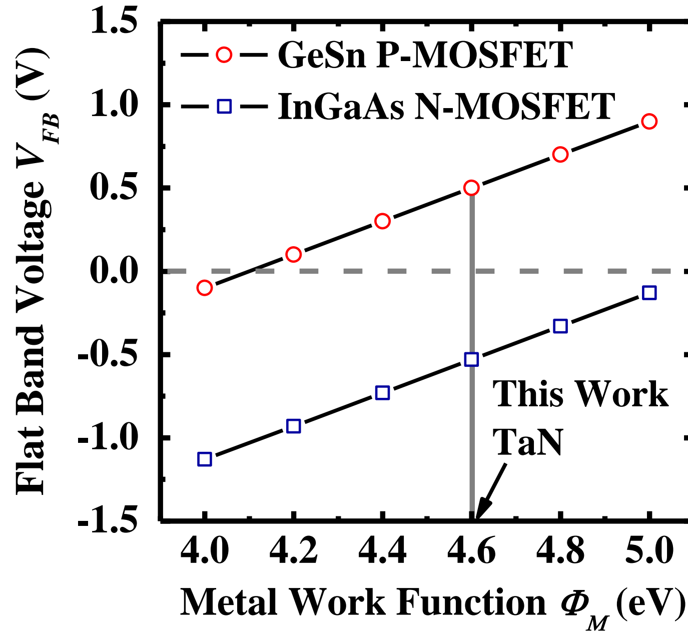


Fig. 4.19. Symmetric V_{TH} can be achieved by using a single TaN metal gate with mid-gap work function, as illustrated by the calculated flat-band voltage V_{FB} as a function of Φ_M without considering the effect of the fixed charges and bulk charges in the gate oxide.

Table 4.1. Parameters used in the calculation of flat-band voltage V_{FB} as a function of metal work function Φ_M shown in Fig. 4.19.

	Bandgap (eV)	Electron Affinity (eV)	Channel Doping Concentration (#/cm^3)	Intrinsic Carrier Concentration (#/cm^3)
$Ge_{0.97}Sn_{0.03}$	0.61	4.0	1×10^{17}	2×10^{13}
$In_{0.7}Ga_{0.3}As$	0.58	4.665	5×10^{16}	1×10^{13}

effect of fixed charges and bulk charges in the gate oxide is not considered. The V_{FB} of GeSn P-MOSFETs V_{FB}^{GeSn} is given by

$$V_{FB}^{GeSn} = \Phi_M - (\chi^{GeSn} + \frac{E_G^{GeSn}}{2} - V_t \ln(\frac{N_d^{GeSn}}{n_i^{GeSn}})) , \quad (4.6)$$

where V_t is the thermal voltage, χ^{GeSn} is the electron affinity, E_G^{GeSn} is the bandgap, N_d^{GeSn} is the channel doping concentration, and n_i^{GeSn} is the intrinsic carrier concentration for GeSn.

The V_{FB} of InGaAs N-MOSFETs V_{FB}^{InGaAs} is given by

$$V_{FB}^{InGaAs} = \Phi_M - (\chi^{InGaAs} + \frac{E_G^{InGaAs}}{2} + V_t \ln(\frac{N_a^{InGaAs}}{n_i^{InGaAs}})) , \quad (4.7)$$

where χ^{InGaAs} is the electron affinity, E_G^{InGaAs} is the bandgap, N_d^{InGaAs} is the channel doping concentration, and n_i^{InGaAs} is the intrinsic carrier concentration for InGaAs. Detailed parameters used in the calculation are shown in Table 4.1.

4.4.2 Device Fabrication

The process flow for fabricating GeSn P-MOSFETs and InGaAs N-MOSFETs is shown in Fig. 4.20. For all steps of common gate stack formation, the GeSn and InGaAs wafers were process together. Details of the gate stack formation process have been discussed in Section 4.2 of this Chapter. All steps were performed by the author except for the substrate growth.

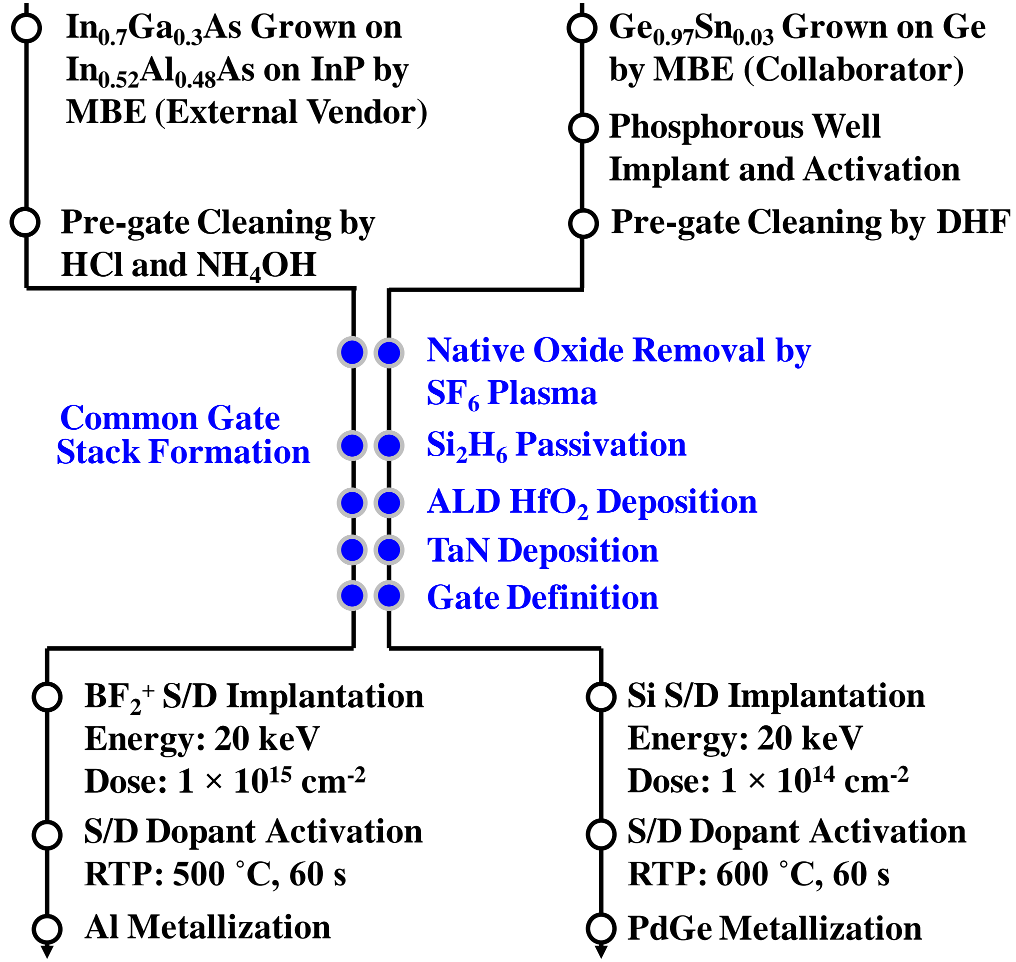


Fig. 4.20. The process flow for fabricating GeSn P-MSOFETs and InGaAs N-MOSFETs. In all steps of common gate stack formation highlighted in blue, the GeSn and InGaAs wafers were process together.

4.4.3 Electrical Characterization

I_D-V_{GS} curves in Fig. 4.21 (a) show the good transfer characteristics of a $Ge_{0.97}Sn_{0.03}$ P-MOSFET and an $In_{0.7}Ga_{0.3}As$ N-MOSFET with subthreshold swing S of 156 and 102 mV/decade, respectively. The V_{TH} of the P- and N-MOSFETs is well-tuned and near 0 V. I_D-V_{DS} output characteristics of the same pair of transistors are plotted in Fig. 4.21 (b). Excellent saturation and pinch-off characteristics were

observed. The GeSn P-MOSFET and N-MOSFET InGaAs show drive currents of ~65 and ~131 μA/μm, respectively, at $|V_{DS}|$ and $|V_{GS}-V_{TH}|$ of 1 V for a L_G of 4 μm. The high drive currents achieved can be attributed to the good gate stack interface quality and the small CET.

The gate leakage current was measured by grounding the source and drain and applying voltage on the gate electrode. Gate leakage current density J_G of less than 10^{-4} A/cm^2 at a gate bias of $V_{TH}\pm1$ V was measured for both GeSn and InGaAs devices (Fig. 4.22). Although the inserted SiO_2 has smaller permittivity than HfO_2, the tunneling barrier seen by both electrons and holes is much higher for SiO_2 than for HfO_2. The low leakage current density indicates the potential for further scaling of the CET. This can be done by scaling down the HfO_2 thickness during ALD deposition.

Fig. 4.23 shows the μ_{eff} of $Ge_{0.97}Sn_{0.03}$ P-MOSFETs and $In_{0.7}Ga_{0.3}As$ N-MOSFETs as a function of inversion carrier density N_{inv}. μ_{eff} was extracted by using the I_D-V_{GS} characteristics at a low $|V_{DS}|$ of 100 mV. At an inversion carrier density N_{inv} of 10^{13} cm^{-2}, $Ge_{0.97}Sn_{0.03}$ P-MOSFETs and $In_{0.7}Ga_{0.3}As$ N-MOSFETs show hole and electron mobilities of ~ 230 and ~495 cm^2/V·s, respectively. At N_{inv} of 10^{13} cm^{-2}, hole and electron mobility values of ~346 and ~705 cm^2/V·s were achieved. It is worth pointing out that the extracted μ_{eff} by split C-V could appreciably underestimate the actual mobility of mobile carriers in the channel, especially for InGaAs MOSFETs with high D_{it} in the conduction band [132]. This is because N_{inv}

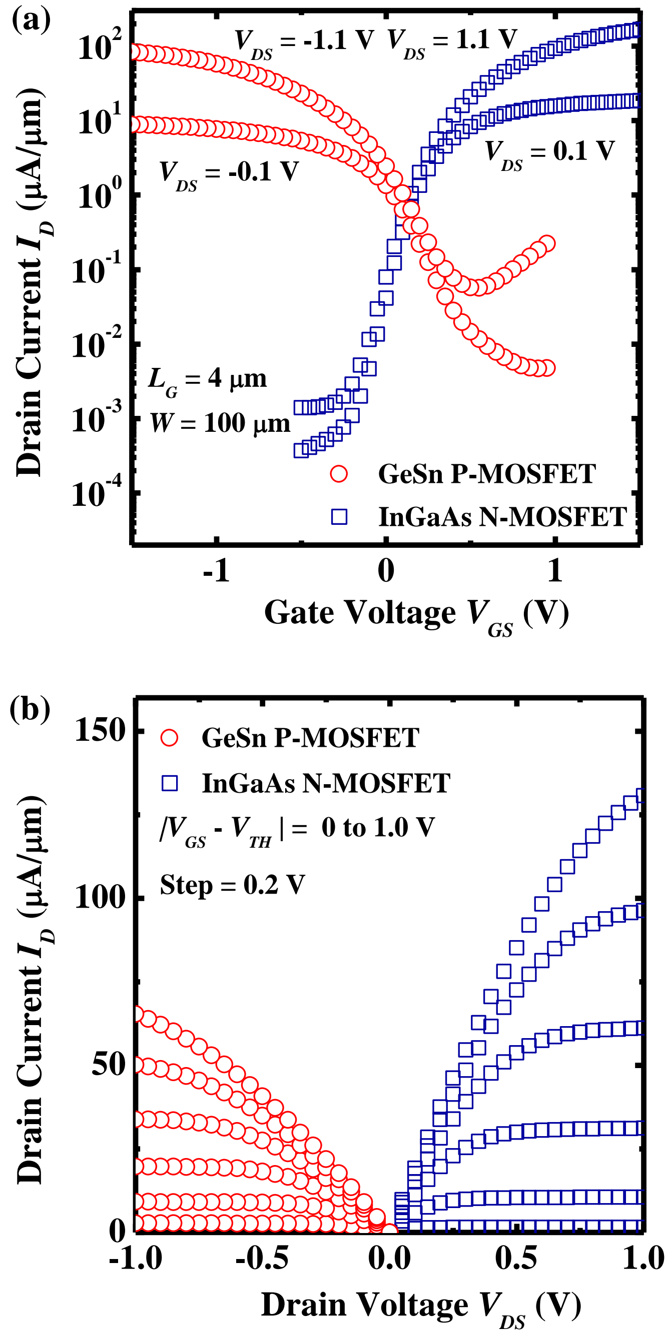


Fig. 4.21. (a) I_D-V_{GS} curves showing well-behaved transfer characteristics of an InGaAs N-MOSFET and a GeSn P-MOSFET. The V_{TH} is symmetric and well-tuned to around 0 V. (b) I_D-V_{DS} output characteristics of the same pair of transistors in (a), showing excellent saturation and pinch-off characteristics. Very high drive currents were achieved at a gate length L_G of 4 µm, attributed to the excellent interface quality due to Si_2H_6 passivation and the CET scaling.

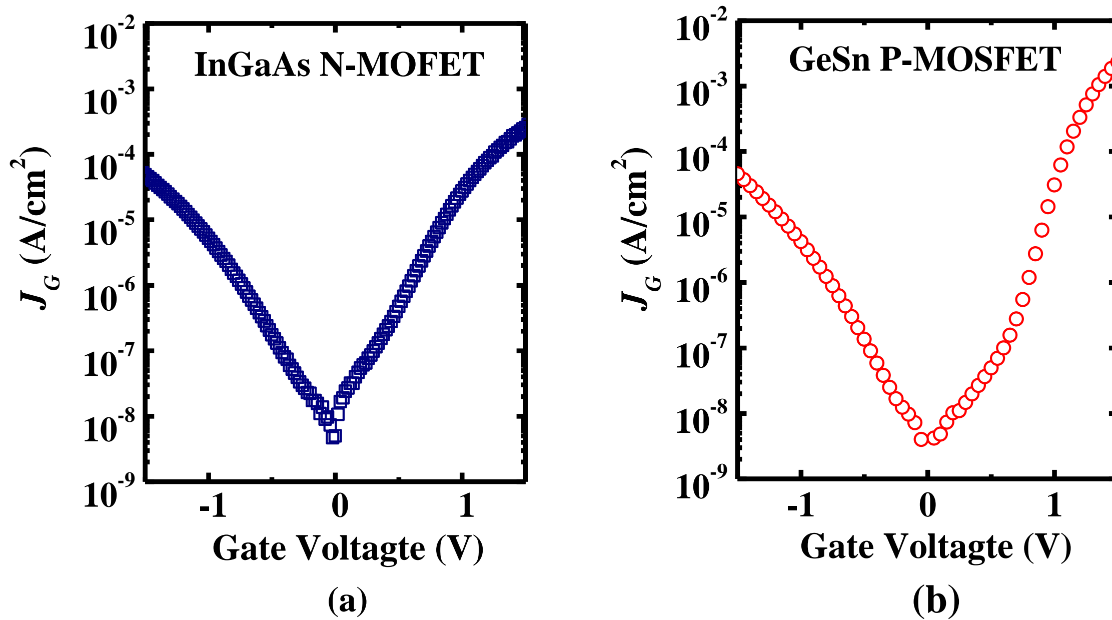


Fig. 4.22. Gate leakage current was measured by grounding the S/D and applying voltage on the gate electrode. J_G of less than 10^{-4} A/cm^2 at a gate bias of V_{TH}±1 V was obtained for both InGaAs and GeSn devices, indicating the potential for further scaling of the CET. The low gate leakage current is attributed to the higher tunneling barrier height seen by both electrons and holes for SiO_2 than for HfO_2.

obtained by integrating the measured inversion *C-V* curves could be much larger than the number of actual mobile carriers flowing in the channel [109].

Fig. 4.24 shows the peak extrinsic transconductance $G_{m,ext}$ measured at a $|V_{DS}|$ of 0.6 V as a function of gate length. Peak $G_{m,ext}$ values scale well with the gate length for both GeSn P-MOSFETs and InGaAs N-MOSFETs. In addition, InGaAs N-MOSFETs exhibit more than 2 times higher peak $G_{m,ext}$ than GeSn P-MOSFETs. This is due to the higher effective carrier mobility of the InGaAs channel than that of the GeSn channel.

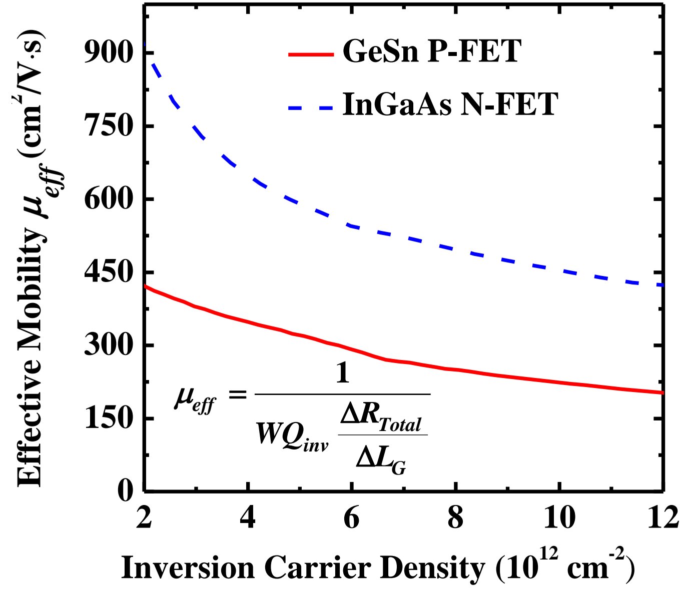


Fig. 4.23. Effective carrier mobility μ_{eff} versus inversion carrier density N_{inv} of GeSn P-MOSFETs and InGaAs N-MOSFETs extracted by split *C-V* method. Hole and electron mobility values of ~230 and ~495 cm^2/V·s were achieved at N_{inv} of 10^{13} cm^{-2} for GeSn P-MOSFETs and InGaAs N-MOSFETs, respectively.

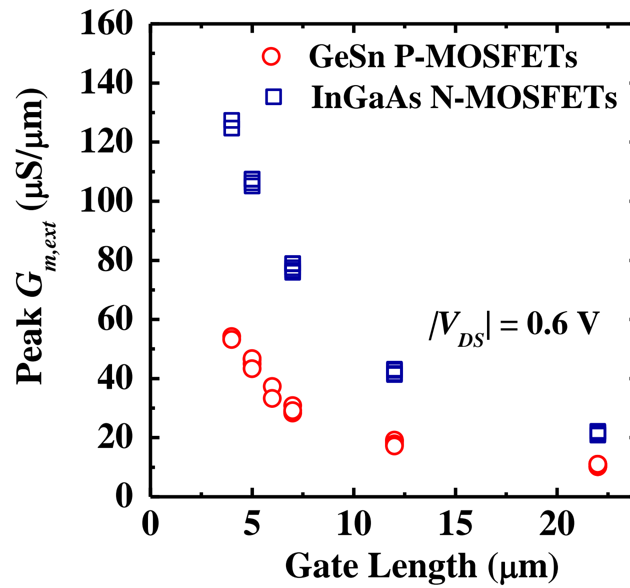


Fig. 4.24. The peak $G_{m,ext}$ values scale well with the gate length for both GeSn P-MOSFETs and InGaAs N-MOSFETs. InGaAs N-MOSFETs have 2 times higher peak $G_{m,ext}$ than GeSn P-MOSFETs due to the higher effective carrier mobility.

4.5 Summary

In this Chapter, the dependence of device performance on different surface passivation techniques was studied. Better interface quality between $HfO_2/Ge_{0.958}Sn_{0.042}$ was achieved by employing low-temperature Si_2H_6 passiavtion. GeSn P-MOSFETs with Si_2H_6 passiavtion exhibit smaller subthreshold swing, higher transconductance, and effective carrier mobility as compared with $(NH_4)_2S$-passivated devices.

NBTI measurement was then performed to investigate the reliability of Si_2H_6-passivated GeSn P-MOSFETs. Excellent NBTI reliability was achieved with very small V_{TH} shift as well as negligible degradation of S and peak transconductance. The extracted power law slope of ~0.18 indicates that generation of oxide trapped charges is the dominant degradation mechanism under NBTI stress.

Finally, we demonstrated a common gate stack technology comprising sub-400 ºC Si_2H_6 passivation and TaN/HfO_2 gate stack for InGaAs and GeSn CMOS devices. When integrated with $In_{0.7}Ga_{0.3}As$ for N-MOSFETs and compressively strained $Ge_{0.97}Sn_{0.03}$ for P-MOSFETs, symmetric V_{TH}, low gate leakage, and very high drive current were achieved. This common gate stack technology is promising for future high-performance CMOS employing InGaAs and GeSn as channel materials.

Chapter 5

Performance Enhancement for GeSn P-Channel Metal-Oxide-Semiconductor Field-Effect Transistors: Surface Orientation and Gate Length Scaling

5.1 Introduction

In Chapter 4, low temperature Si_2H_6 passivation has been developed to achieve a thermodynamically stable high-k/$Ge_{1-x}Sn_x$ interface with low interface trap density D_{it}. In addition, small capacitance equivalent thickness (CET) with low gate leakage current was realized by incorporation of the HfO_2 gate dielectric and TaN metal gate. However, all reported $Ge_{1-x}Sn_x$ channel p-channel metal-oxide-semiconductor field-effect transistors (P-MOSFETs) reported has so far been for (100) surface orientation [27]-[29]. It is well known that the choice of optimal crystal surface orientation for drive current improvement is also important, and this has been well investigated for Si [63],[133],[134] and Ge MOSFETs [65],[135]. To explore the full potential of $Ge_{1-x}Sn_x$ as a P-MOSFET channel material, it is necessary to investigate the performance of $Ge_{1-x}Sn_x$ P-MOSFETs with other surface orientations.

In addition, all efforts made for $Ge_{1-x}Sn_x$ P-MOSFETs have been for transistors with gate length L_G larger than 2 μm.

In this Chapter, two techniques were explored to enhance the drive current of $Ge_{1-x}Sn_x$ P-MOSFETs. Section 5.2 investigates the dependence of carrier mobility and drive current I_{Dsat} of $Ge_{0.958}Sn_{0.042}$ P-MOSFETs on surface orientations. $Ge_{0.958}Sn_{0.042}$ P-MOSFETs with implantless NiGeSn metal source/drain (S/D) were fabricated on (100)- and (111)-oriented $Ge_{0.958}Sn_{0.042}$ substrates. The channel orientations for (100)- and (111)-oriented $Ge_{0.958}Sn_{0.042}$ P-MOSFETs are [110] and $[\bar{1}\bar{1}2]$, respectively. We found that, with similar S/D series resistance R_{SD} and subthreshold swing S, $Ge_{0.958}Sn_{0.042}$ P-MOSFETs with (111) surface orientation show higher effective hole mobility, I_{Dsat}, and peak intrinsic transconductance $G_{m,int}$ than $Ge_{0.958}Sn_{0.042}$ P-MOSFETs with (100) orientation. Section 5.3 discusses the world's first short channel $Ge_{0.95}Sn_{0.05}$ P-MOSFETs with L_G down to 200 nm. Drive current of ~680 μA/μm was achieved at V_{DS} of -1.5 V and V_{GS}-V_{TH} of -2 V, with peak $G_{m,int}$ of ~295μS/μm at V_{DS} of -0.6 V.

5.2 $Ge_{0.958}Sn_{0.042}$ P-MOSFETs Fabricated on (100) and (111) Surface Orientations with Sub-400 ˚C Si_2H_6 Passivation

5.2.1 Device Fabrication

The process flow for fabricating $Ge_{0.958}Sn_{0.042}$ P-MOSFETs is shown in Fig. 5.1. A $Ge_{0.958}Sn_{0.042}$ film with a thickness of ~10 nm was epitaxially grown on n-type Ge(100) and Ge(111) substrates using a solid-source molecular beam epitaxy (MBE) system at 180ºC. The substitutional Sn composition is 4.2%. Phosphorus well implant was performed at energy of 20 keV and dose of 5×10^{12} cm^{-2}, and was activated at 450 ºC for 180 s to convert the as-grown $Ge_{0.958}Sn_{0.042}$ from p-type to n-type. A cyclic clean was used for pre-gate cleaning, which involves treating the wafers with deionized water followed by hydrofluoric (HF) acid ($HF:H_2O$ = 1:50) in each cycle. The $Ge_{0.958}Sn_{0.042}$ substrates were then immediately loaded into an ultra-high vacuum tool equipped with a high-vacuum transfer module (base pressure of ~1×10^{-7} Torr). SF_6 plasma treatment was first done at 300 °C for 50 s in one chamber to remove any native oxide that may have been formed. Next, without breaking vacuum, Si_2H_6 treatment was carried out in a second chamber at 370 °C for 120 minutes at a flow rate of 10 sccm to form a high-quality Si passivation layer.

This was followed by deposition of ~4.5 nm-thick HfO_2 at 250 °C in an atomic layer deposition (ALD) tool using tetrakis [dimethylamido] hafnium and H_2O as precursors, and N_2 as the carrier gas. TaN metal and SiO_2 hardmask were then sputtered. After gate lithography, a F-based plasma etch was used for gate definition. 50 nm of SiO_2 was deposited and patterned to expose the active region (including

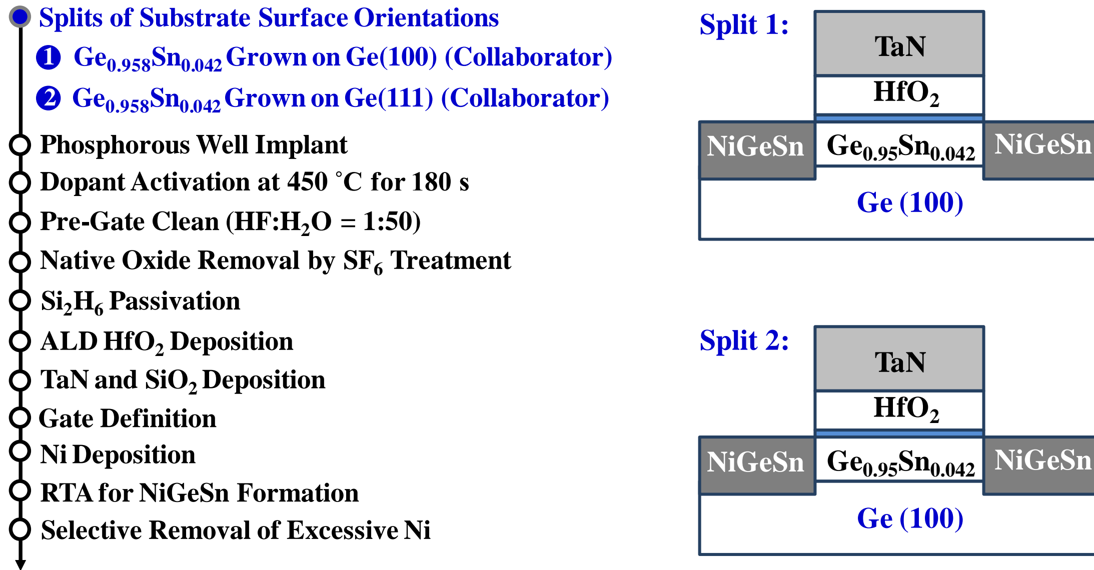


Fig. 5.1. The process flow for fabricating $Ge_{0.958}Sn_{0.042}$ P-MOSFETs. Two splits of substrate surface orientations were introduced: $Ge_{0.958}Sn_{0.042}$ on Ge(100) or Ge(111). All steps were performed by the author except for the $Ge_{0.958}Sn_{0.042}$ growth.

S/D regions) and a portion of the gate pad. 10 nm-thick Ni was sputter-deposited, and a 350 °C 30 s rapid thermal anneal (RTA) formed NiGeSn metallic S/D regions. Finally, to complete the device fabrication, excess Ni was selectively removed.

5.2.2 Material Characterization

High-resolution transmission electron microscope (HRTEM) images of $TaN/HfO_2/SiO_2/Si$ stack on $Ge_{0.958}Sn_{0.042}$ substrates with (100) and (111) surface orientations are shown in Fig. 5.2 (a) and (b), respectively. A uniform and ultra-thin SiO_2/Si interfacial layer were observed for both surface orientations: The $Ge_{0.958}Sn_{0.042}$ surface was fully covered with a very thin (~ a few monolayers) and uniform Si layer from the Si_2H_6 treatment, and part of the Si

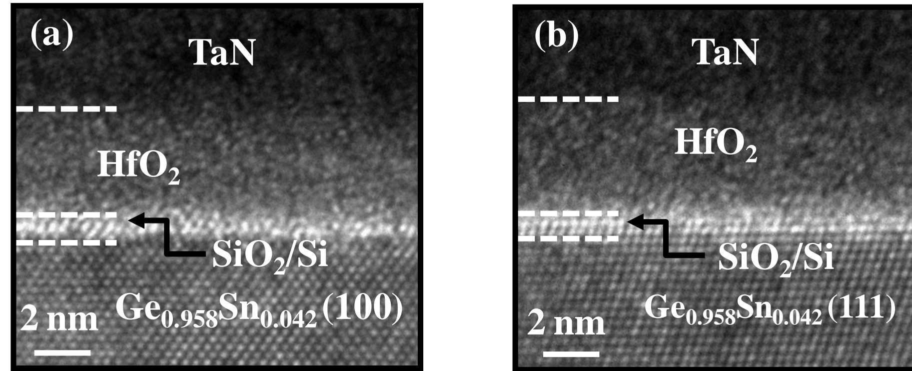


Fig. 5.2. High resolution cross-sectional TEM images of the TaN/HfO_2/SiO_2/Si stack on (a) (100)-oriented and (b) (111)-oriented $Ge_{0.958}Sn_{0.042}$ surfaces, respectively. A uniform and ultra-thin SiO_2/Si interfacial layer between the HfO_2 and $Ge_{0.958}Sn_{0.042}$ was formed.

layer was oxidized during the subsequent thermal process. In addition, the HfO_2 remains amorphous after device fabrication.

To investigate the effect of Si_2H_6 passivation on the interfacial chemical bonding characteristics between the high-k gate dielectric and $Ge_{0.958}Sn_{0.042}$, samples with ~2 nm of HfO_2 formed on $Ge_{0.958}Sn_{0.042}$ surfaces with and without Si_2H_6 passivation were prepared for XPS analysis. Fig. 5.3 (a) and (b) show the Ge $2p_{3/2}$ and Sn $3d_{5/2}$ core level spectra, respectively, of (100)-oriented $Ge_{0.958}Sn_{0.042}$ sample without Si_2H_6 passivation. Fig. 5.3 (c) and (d) show the Ge $2p_{3/2}$ and Sn $3d_{5/2}$ core level spectra, respectively, of (100)- and (111)-oriented $Ge_{0.958}Sn_{0.042}$ samples with Si_2H_6 passivation. Obvious suppression of the Ge-O bond and Sn-O bond by the Si_2H_6 passivation was observed. The binding energy of Ge-O bond is in the range of ~1220-1221.5 eV, and that of Sn-O bond is ~486.7 eV. Although there might be a weak Ge-O peak for the Si_2H_6-passivated $Ge_{0.958}Sn_{0.042}$ surfaces, both Ge-O and Sn-O peaks are reduced as compared with those for the unpassivated $Ge_{0.958}Sn_{0.042}$ surfaces.

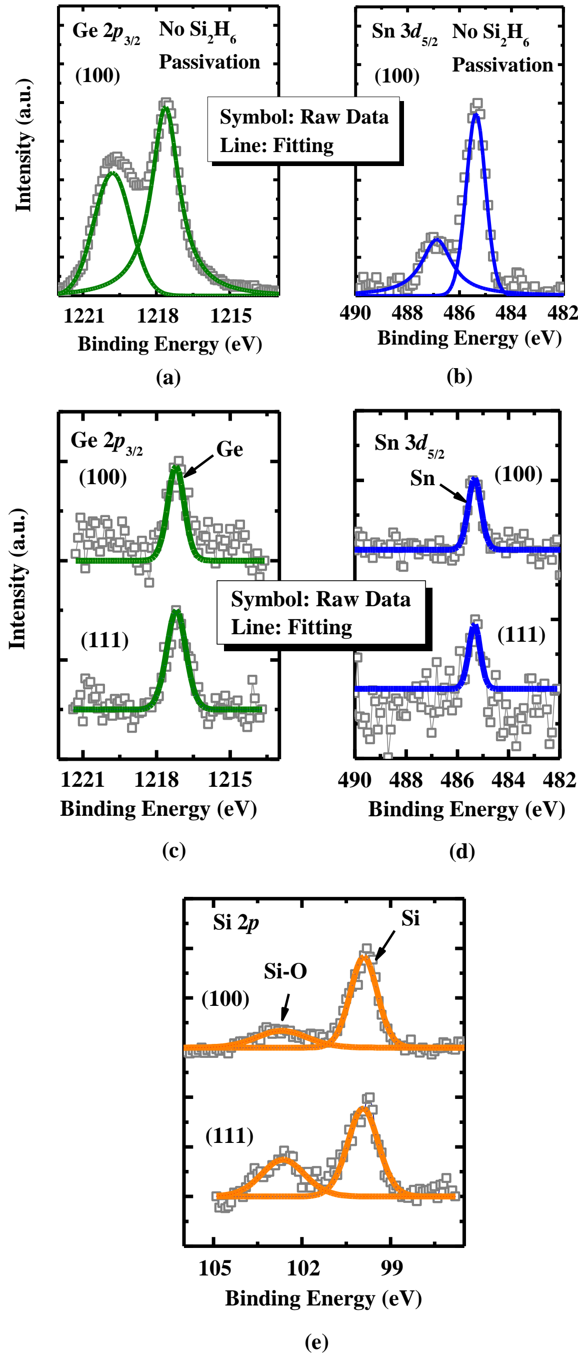


Fig. 5.3. (a) Ge $2p_{3/2}$ and (b) Sn $3d_{5/2}$ core level spectra of (100)-oriented $Ge_{0.958}Sn_{0.042}$ sample without Si_2H_6 passivation show high intensity of Ge-O and Sn-O peaks. Si_2H_6 passivation can effectively suppress the formation of Ge-O and Sn-O bonds for both (100)- and (111)-oriented $Ge_{0.958}Sn_{0.042}$ surfaces, as shown in (c) and (d). Part of the Si layer was oxidized during the subsequent HfO_2 dielectric deposition process, as indicated by the existence of the Si-O peak in the Si $2p$ spectra shown in (e).

In addition, examination of the Si 2*p* spectra in Fig. 5.3 (e) reveals the formation of Si-O bond in the Si_2H_6-passivated sample, suggesting that part of the Si layer was oxidized during the subsequent HfO_2 dielectric deposition process.

5.2.3 Electrical Characterization

I_D-V_{GS} curves in Fig. 5.4 show transfer characteristics of the $Ge_{0.958}Sn_{0.042}$ P-MOSFETs with (100) and (111) surface orientations. Both transistors have a L_G of 3.5 µm. Similar subthreshold swing S of ~130 mV/decade was observed, indicating similar mid-gap interface trap density D_{it} for the two orientations. The mid-gap D_{it} values are extracted to be 2.3×10^{12} and 2.5×10^{12} $cm^{-2}\cdot eV^{-1}$ for (100)- and (111)-oriented $Ge_{0.958}Sn_{0.042}$ P-MOSFETs, respectively, by room temperature charge pumping method [Fig. 5.5]. Details of the extraction method have been described in Section 3.3 of Chapter 3. This S is the smallest value reported so far for

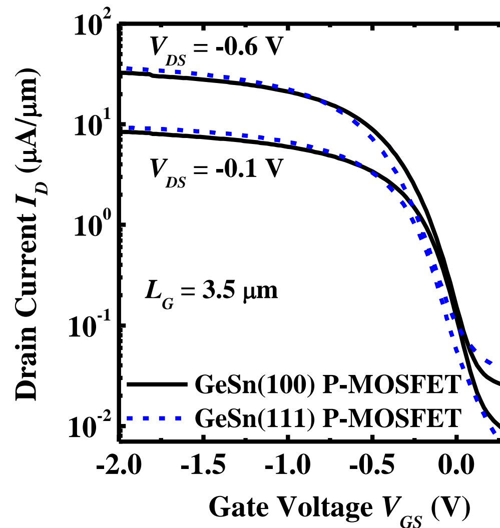


Fig. 5.4. I_D-V_{GS} curves showing excellent transfer characteristics of $Ge_{0.958}Sn_{0.042}$ P-MOSFETs with (100) and (111) surface orientations. Similar S was observed, indicating similar mid-gap interface trap density.

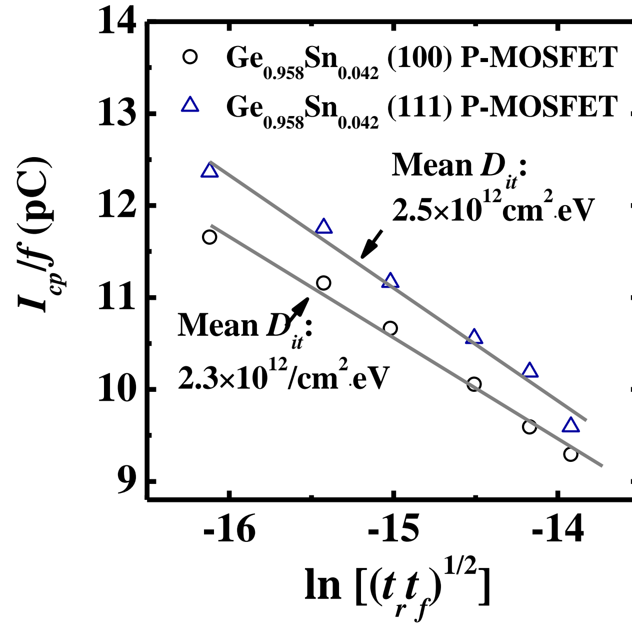


Fig. 5.5. Mid-gap D_{it} was extracted to be 2.3×10^{12} and 2.5×10^{12} $cm^{-2}\cdot eV^{-1}$ for (100)- and (111)-oriented $Ge_{0.958}Sn_{0.042}$ P-MOSFETs, respectively, by room temperature charge pumping measurement.

$Ge_{0.958}Sn_{0.042}$ channel P-MOSFETs. This value is still higher than that of the best reported Ge P-MOSFET. It could possibly be reduced by optimizing the Si_2H_6 passivation module, e. g. passivation temperature and duration, but this has not been explored yet. The threshold voltage of (111) surface-orientation devices is slightly left-shifted as compared with that of the (100) surface-orientation ones, as indicated in Fig. 5.6 which shows V_{TH} values of a large set of transistors as a function of L_G. This could be due to more positive fixed charges at the high-k/$Ge_{0.958}Sn_{0.042}$ interface for the (111)-oriented devices.

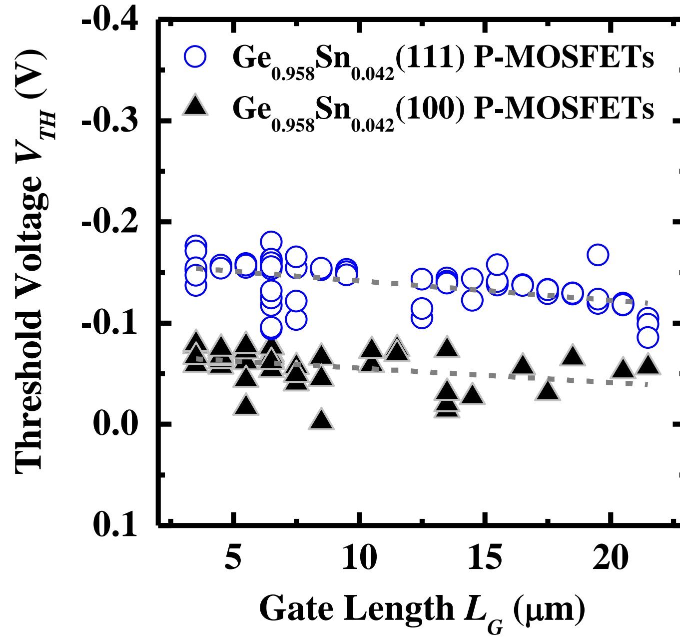


Fig. 5.6. The V_{TH} values of $Ge_{0.958}Sn_{0.042}$ P-MOSFETs on the (111) substrate are left-shifted as compared with those of transistors on the (100) substrate. This could be due to more positive fixed charges at the high-*k*/GeSn interface for the (111)-oriented devices.

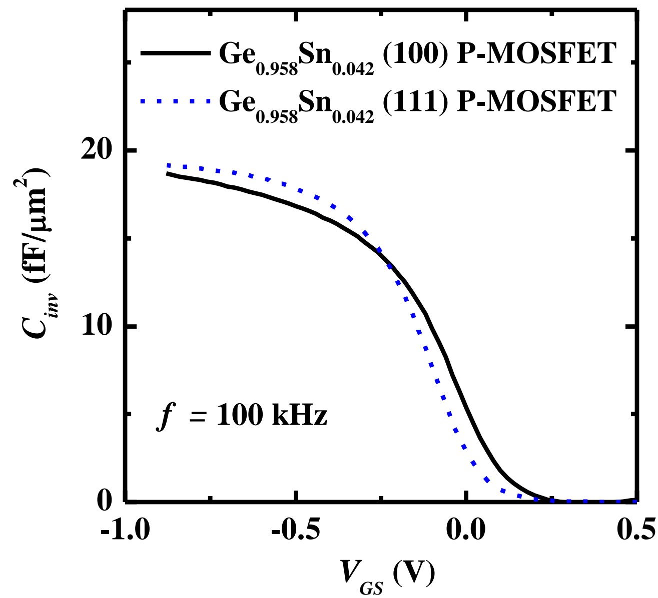


Fig. 5.7. Inversion *C-V* characteristics measured at a frequency of 100 kHz. The CET is extracted to be ~1.8 nm based on the inversion capacitance value. Slightly larger inversion capacitance was observed for (111)-oriented transistor as compared with the (100)-oriented one.

Inversion *C-V* characteristics measured at a frequency of 100 kHz are shown in Fig. 5.7. The capacitance equivalent thickness (CET) is extracted to be ~1.8 nm based on the inversion capacitance value. Slightly larger inversion capacitance was observed for the (111)-oriented $Ge_{0.958}Sn_{0.042}$ P-MOSFET as compared with the (100)-oriented one. The inversion capacitance was determined by three parameters. First, the HfO_2 thickness. Since the HfO_2 deposition for samples with both orientations was done in the same run, the HfO_2 thickness of the two samples should be the same. Second, the thickness of SiO_2/Si interfacial layer which was formed due to the Si_2H_6 passivation and oxidation of part of the Si passivation layer. In Fig. 5.3 (e), the stronger intensity of Si-O bond for (111)-oriented $Ge_{0.958}Sn_{0.042}$ sample could indicate a thicker SiO_2/Si interfacial layer formed on the $Ge_{0.958}Sn_{0.042}$ surface with (111) orientation. Third, the inversion charge centroid which describes the shift of the inversion charges away from the oxide-semiconductor interface due to the quantum confinement.

To study the dependence of the inversion charge centroid on the surface orientations of $Ge_{0.958}Sn_{0.042}$, simulation was performed using Nextnano. Shown in Fig. 5.8 is the inversion hole density as a function of distance from the channel surface for $Ge_{0.958}Sn_{0.042}$ P-MOSFETs with (100) and (111) surface orientations. It clearly shows that the inversion charge centroid is closer to the $Ge_{0.958}Sn_{0.042}$ channel surface for the (111)-oriented $Ge_{0.958}Sn_{0.042}$ P-MOSFET at an inversion carrier concentration of 5×10^{12} cm^{-2}. This is due to larger density of states for (111)-oriented $Ge_{0.958}Sn_{0.042}$ substrate.

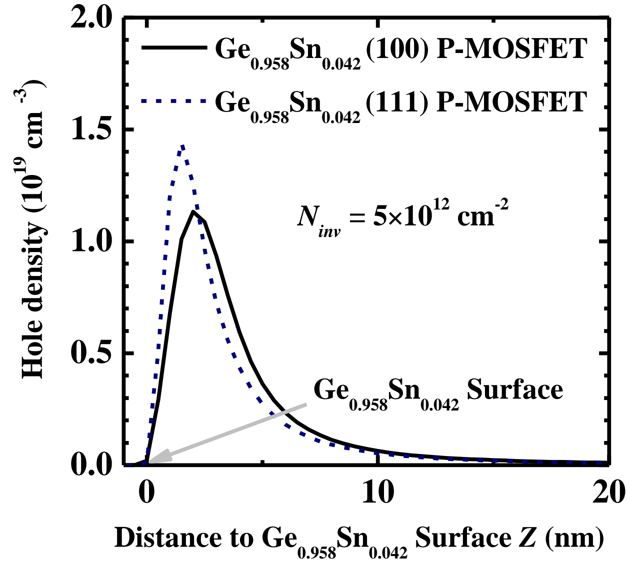


Fig. 5.8. Simulation shows that $Ge_{0.958}Sn_{0.042}$ P-MOSFET with (111) orientation has an inversion charge centroid closer to the $Ge_{0.958}Sn_{0.042}$ surface at an inversion carrier density of 5×10^{12} cm^{-2}. This is due to larger density of states for (111)-oriented $Ge_{0.958}Sn_{0.042}$.

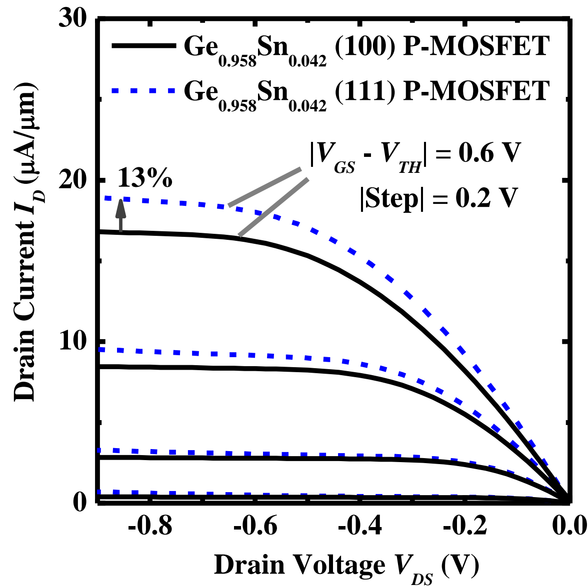


Fig. 5.9. I_D-V_{DS} characteristics show that (111)-oriented $Ge_{0.958}Sn_{0.042}$ P-MOSFET has 13% enhancement in drive current over the (100)-oriented device at a gate over drive of -0.6 V and V_{DS} of -0.9 V.

The second and third parameters are the competing ones. Although (111)-oriented $Ge_{0.958}Sn_{0.042}$ substrate has a thicker SiO_2/Si interfacial layer, its inversion charge centroid is closer to the $Ge_{0.958}Sn_{0.042}$ surface as compared with the (100)-oriented one. The overall effect is that $Ge_{0.958}Sn_{0.042}$ P-MOSFET with (111) orientation has a slightly larger inversion capacitance.

Fig. 5.9 shows the I_D-V_{DS} curves of the same pair of devices in Fig. 5.4. Both transistors show good pinch-off and saturation characteristics. I_{Dsat} is 13 % higher for (111) orientation than for (100) orientation at a gate overdrive of -0.6 V and V_{DS} of -0.9 V.

Next, the impact of R_{SD} and carrier mobility on I_{Dsat} difference was evaluated. Large numbers of transistors were measured with L_G ranging from 3.5 to 20.5 μm. Shown in Fig. 5.10 is the total resistance R_{Total} extracted at a gate overdrive of -1.2 V and V_{DS} of -0.1 V as a function of L_G. From the R_{Total} versus L_G plot, the intercept of a fitted line with the *y*-axis yields the value of R_{SD}. R_{SD} values of ~5.5 and ~5.8 kΩ·μm were obtained for (100)- and (111)-oriented surfaces, respectively. The high R_{SD} values could be due to the high contact resistance between NiGeSn and GeSn [136]. As reported in Ref. 136, the contact resistivity of NiGeSn/$Ge_{0.947}Sn_{0.053}$ is 1.6×10^{-5} Ω·cm^2. The NiGeSn contact formation recipe used in this work is the same as that in Ref. 136. This value is quite high as compared with the requirement for logic application well beyond the 11-nm technology node, i. e. in the order of 10^{-8} Ω·cm^2. Further research is needed to reduce the contact resistance.

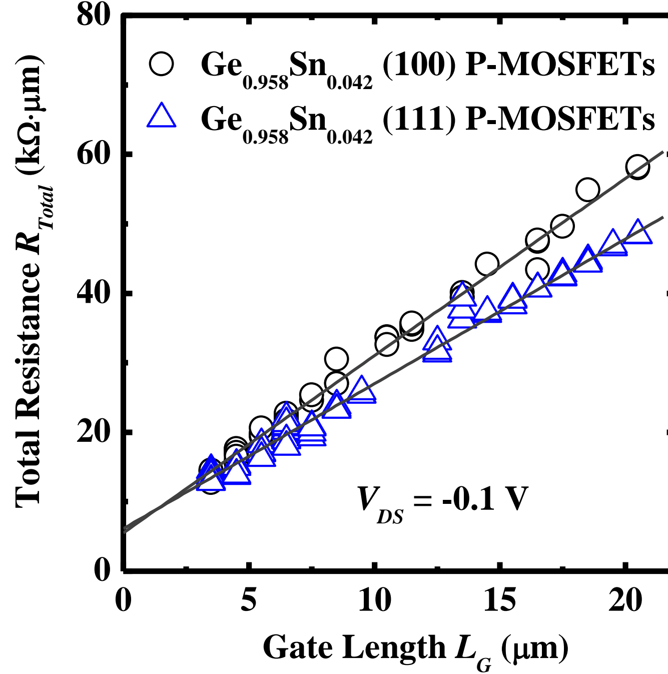


Fig. 5.10. Total resistance R_{Total} as a function of gate length at V_{GS}-V_{TH} of -1.2 V and V_{DS} of -0.1 V. Experimental data points are plotted using circles or triangles. Fitted lines are drawn using solid lines. Similar series resistance was observed for devices with two different surface orientations. (111)-oriented devices exhibit a smaller $\Delta R_{Total}/\Delta L_G$ slope, indicating higher carrier mobility.

The slope of $\Delta R_{Total}/\Delta L_G$ as a function of L_G is related to the effective hole mobility μ_{eff} of the transistors which is given by

$$\mu_{eff} = \frac{1}{W_{eff} Q_{inv} (\Delta R_{Total} / \Delta L_G)}, \tag{5.1}$$

where W_{eff} is the channel width and Q_{inv} is the inversion charge density [137]. The smaller $\Delta R_{Total}/\Delta L_G$ for devices on (111)-oriented substrate indicates an 18% enhancement in mobility as compared with devices on (100)-oriented surface.

μ_{eff} as a function of inversion carrier density N_{inv} is further extracted by split C-V method, as shown in Fig. 5.11. μ_{eff} was extracted based on a total resistance

slope-based approach. Higher μ_{eff} was observed for the (111)-oriented $Ge_{0.958}Sn_{0.042}$ P-MOSFET. V_{GS}-V_{TH} of -1.2 V used in Fig. 5.10 corresponds to N_{inv} of 1.1×10^{13} cm^{-2} in Fig. 5.11. μ_{eff} values at N_{inv} of 1.1×10^{13} cm^{-2} for (100)- and (111)-oriented $Ge_{0.958}Sn_{0.042}$ P-MOSFETs are 226 and 270 cm^2/V·s, respectively. This gives ~19 % higher mobility for $Ge_{0.958}Sn_{0.042}$ P-MOSFETs with (111) surface orientation than with (100) surface orientation, consistent with the result shown in Fig. 5. 10.

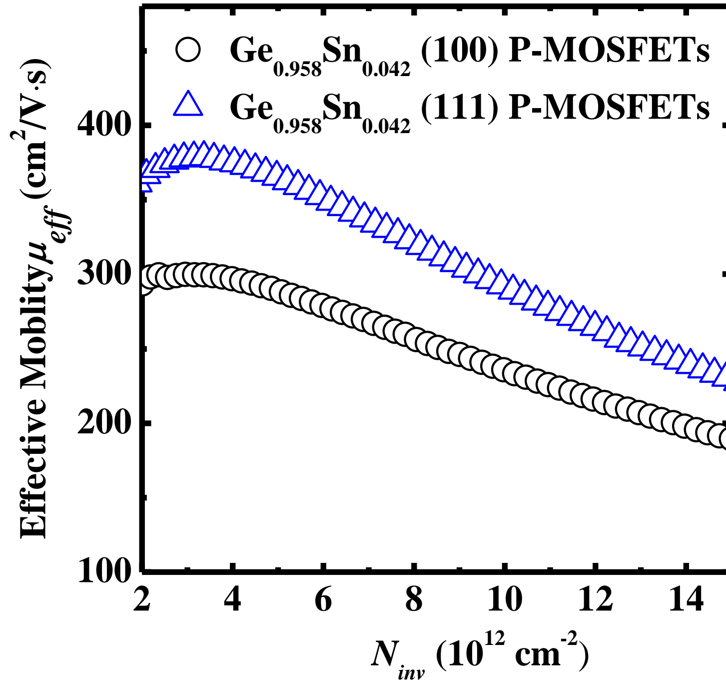


Fig. 5.11. μ_{eff} as a function of N_{inv} extracted by split *C-V* method. Higher μ_{eff} was observed for the (111)-oriented $Ge_{0.958}Sn_{0.042}$ P-MOSFET. μ_{eff} values at N_{inv} of 1.1×10^{13} cm^{-2} for (100)- and (111)-oriented $Ge_{0.958}Sn_{0.042}$ P-MOSFETs are 226 and 270 cm^2/V·s, respectively. This gives ~19 % higher mobility for $Ge_{0.958}Sn_{0.042}$ P-MOSFETs with (111) surface orientation than with (100) surface orientation, constant with the result shown in Fig. 5. 10.

A similar trend was predicted in Ref. [138], where Monte Carlo simulation was done to obtain the mobility of (100)- and (111)-oriented bulk Ge under biaxial compressive strain, accounting for scattering from inelastic acoustic and optical phonons. A ~15% increase of hole mobility was observed in Fig. 3 of Ref. 138 for (111)-oriented Ge surface as compared with the (100)-oriented one at 0.5 to 1.0% biaxial compressive strain. The data of the (100)- and (111)-oriented surfaces is reproduced in Fig. 5.12. In our experiment, the 10 nm-thick $Ge_{0.958}Sn_{0.042}$ channel has a Sn composition of 4.2%, and it is under 0.6% biaxial compressive strain.

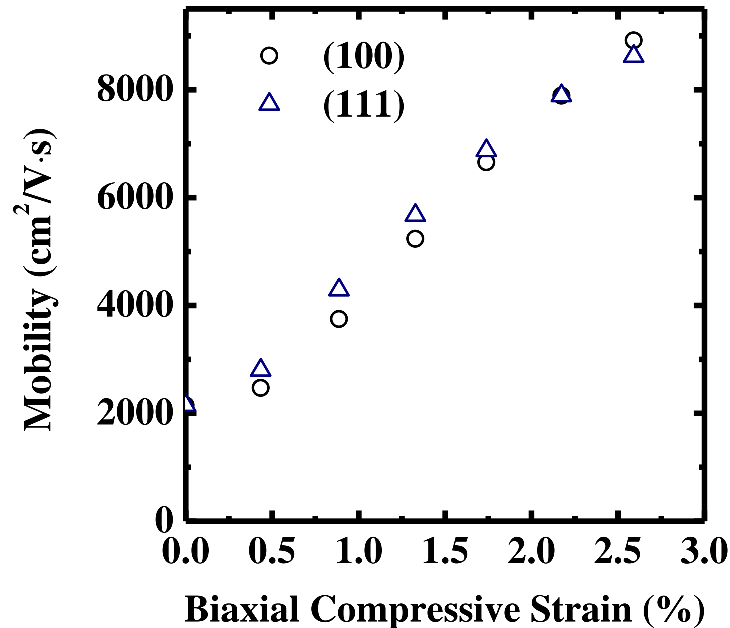


Fig. 5.12. Monte Carlo simulation in Ref. 138 predicts ~15% increase of hole mobility for (111)-oriented Ge surface as compared with the (100)-oriented one at 0.5 to 1.0% biaxial compressive strain (Data reproduced from Fig. 3 of Ref. 138). Scattering from inelastic acoustic and optical phonons was accounted for.

Peak intrinsic transconductance, $G_{m,int}$, was extracted at V_{DS} of -1 V for a large number of devices. $G_{m,int}$ was extracted by

$$G_{m,int} = \frac{G_{m,ext}}{1 - 0.5 \cdot R_{SD} \cdot G_{m,ext}} \tag{5.2}$$

where $G_{m,ext}$ is the measured extrinsic transconductance and R_{SD} is the value extracted in Fig. 5.10. Shown in Fig. 5.13 is the peak $G_{m,int}$ at V_{DS} of -1 V as a function of L_G. Although there is some scatter in the data, the (111)-orientation devices clearly have a higher peak $G_{m,int}$.

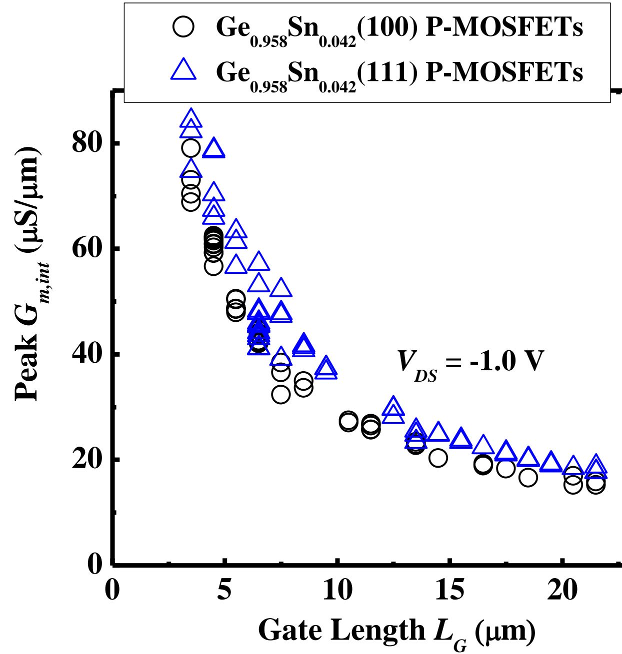


Fig. 5.13. The plot of peak $G_{m,int}$ at V_{DS} of -1.0 V as a function of L_G clearly shows that (111)-oriented $Ge_{0.958}Sn_{0.042}$ P-MOSFETs have higher peak $G_{m,int}$ values over (100)-oriented devices.

5.3 Fabrication and Characterization of Short channel $Ge_{0.95}Sn_{0.05}$ P-MOSFETS

5.3.1 Device Fabrication

The process flow for fabricating the world's first $Ge_{0.95}Sn_{0.05}$ short channel P-MOSFET is shown in Fig. 5.14 (a). To control the short channel effects, n-type doped (100)-oriented Ge wafer with a high doping concentration N_D of 1×10^{18} cm^{-3} was used as the starting substrate. An unintentionally doped $Ge_{0.95}Sn_{0.05}$ film with a thickness of 30 nm was grown by MBE at a temperature of 180 ˚C. Sn composition was further increased to 5% to scale up the hole mobility. After the phosphorus well implantation at energy of 25 KeV and a dose of 7×10^{12} cm^{-2}, the dopants were activated by rapid thermal annealing at 400 ˚C for 5 minutes. Following that, gate stack formation, including pre-gate cleaning, Si_2H_6 passivation, HfO_2 deposition and TaN deposition, was done using the same recipes discussed in Section 2 of this Chapter.

A fine gate pattern using single layer NEB-22 is defined by E-beam lithography and followed by the gate etching using Cl-based gas. The halo implant was then performed at energy of 80 KeV and a dose of 5×10^{13} cm^{-2} with a tilt angle of 15 ˚. This was followed by BF_2^+ S/D extension implant at energy of 10 KeV and a dose of 5×10^{14} cm^{-2}. SiON spacer formation was then done comprising the SiON deposition by plasma enhanced chemical vapor deposition (PECVD) and the F-based reactive etching. After the boron deep S/D implantation at energy of 10 KeV and

(a) Process Flow for Short Channel $Ge_{0.95}Sn_{0.05}$ P-MOSFET Fabrication

- $Ge_{0.95}Sn_{0.05}$ Grown on Ge(100) by MBE
- Phosphorous Well Implant and Activation
- Pre-gate Cleaning by DHF
- Native Oxide Removal by SF_6 Plasma
- Si_2H_6 Passivation
- HfO_2/TaN Stack Deposition
- Gate Patterning and Etch
- Arsenic Halo Implant
  Energy: 80 keV, Dose: 5×10^{13} cm^{-2}, 15° tilt
- BF_2^+ S/D Extension Implant
  Energy: 10 keV, Dose: 5×10^{14} cm^{-2}
- Spacer Formation
- B Deep S/D Extension Implant
  Energy: 9 keV, Dose: 2×10^{15} cm^{-2}
- Dopant Activation
  RTP: 500 °C, 60 s
- NiGeSn Metallization

(b) Schematic of a Completed Short Channel $Ge_{0.95}Sn_{0.05}$ P-MOSFET

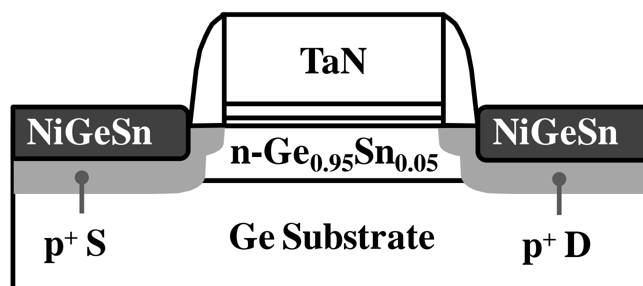


Fig. 5.14. (a) Process flow for fabricating short channel $Ge_{0.95}Sn_{0.05}$ P-MOSFET, with a schematic of the completed device structure shown in (b). Advanced modules, such as halo implant and S/D extension implant, were introduced to control the short channel effects.

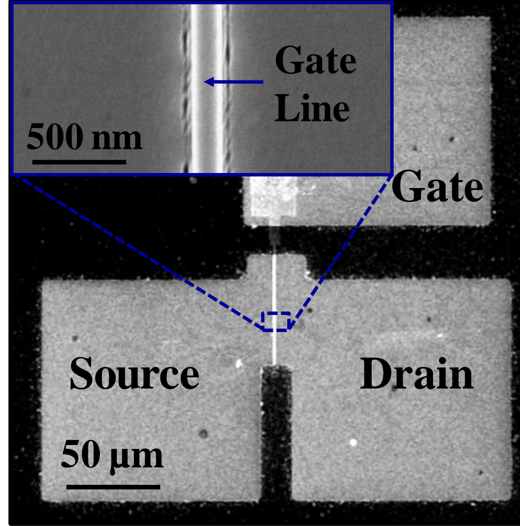
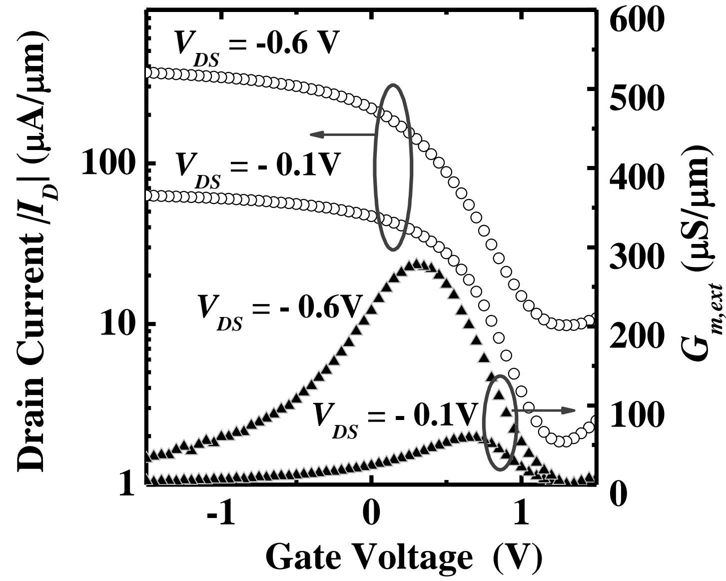


Fig. 5.15. Top-view SEM image showing a completed short channel $Ge_{0.95}Sn_{0.05}$ P-MOSFET with source, drain and gate pads. The transistor has gate width of 50 μm. The zoom-in image of the region highlighted by dotted line shows the gate length of 200 nm.

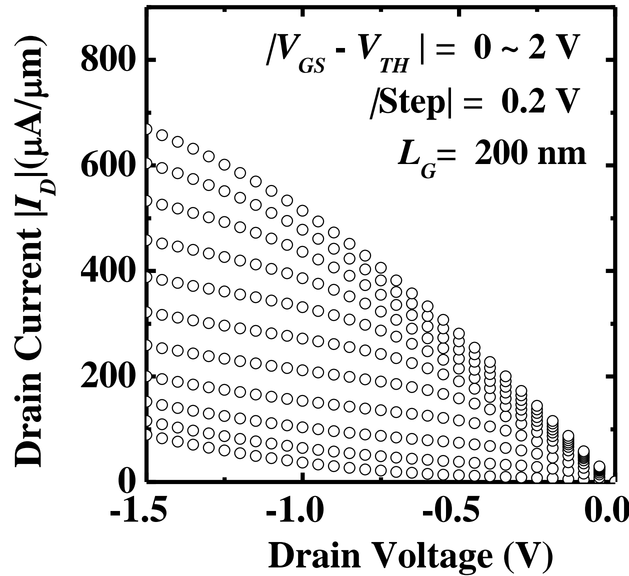
dose of 2×10^{15} cm^{-2}, all dopants were then activated by RTA at 500 ˚C for 60 s. Finally, NiGeSn metallic S/D was formed to complete the transistor fabrication. Top-view SEM image in Fig. 5.15 shows a completed short channel $Ge_{0.95}Sn_{0.05}$ P-MOSFET, with the inset showing the gate length of 200 nm.

5.3.2 Electrical Characterization

Plots of I_D and extrinsic transconductance $G_{m,ext}$ versus V_{GS} for a $Ge_{0.95}Sn_{0.05}$ P-MOSFET with L_G of 200 nm are shown in Fig. 5.16 (a). This device has the shortest L_G reported so far for $Ge_{1-x}Sn_x$ P-MOSFETs. Decent transfer characteristics were observed. $G_{m,ext}$ was measured to be 295 μS/μm at V_{DS} of -0.6 V. The extracted S is affected by the high off-state current, resulting from the high junction leakage current due to the small band gap of $Ge_{0.95}Sn_{0.05}$. To improve the drain induced barrier lowering (*DIBL*), a more highly doped Ge substrate or a GOI substrate can be



(a)



(b)

Fig. 5.16. (a) I_D-V_{GS} and $G_{m,ext}$-V_{GS} curves of a $Ge_{0.95}Sn_{0.05}$ P-MOSFET with L_G of 200 nm. Decent transfer characteristics were observed. Improvement in subthreshold swing, I_{on}/I_{off} ratio, and *DIBL* can be achieved by device structure optimization, e.g. by growing the $Ge_{1-x}Sn_x$ channel layer on GeOI substrate. (b) I_D-V_{DS} output characteristics show that drive current of ~680 μA/μm was realized at V_{GS}-V_{TH} of -2.0 V and V_{DS} of -1.5 V.

used. I_D-V_{DS} curves in Fig. 5.16 (b) show drive current of more than 680 μA/μm at V_{GS} -V_{TH} of -2.0 V and V_{DS} of -1.5 V.

The drive current is severely affected by the high S/D series resistance R_{SD}. Fig. 5.17 plots the total resistance R_{Total} versus V_{GS} for the same device in Fig. 5.16. The R_{Total} of a transistor measured at low drain bias decreases with increasing gate bias V_{GS}, and approaches R_{SD} at large V_{GS}. R_{SD} is the sum of the source resistance R_S and drain resistance R_D, where R_S is equal to R_D due to device symmetry. The extracted R_{SD} is around 1.7 kΩ·μm. This value is quite high as compared with other NiGe contacts reported [57], and could be due to un-optimized dopant activation and metal S/D formation conditions.

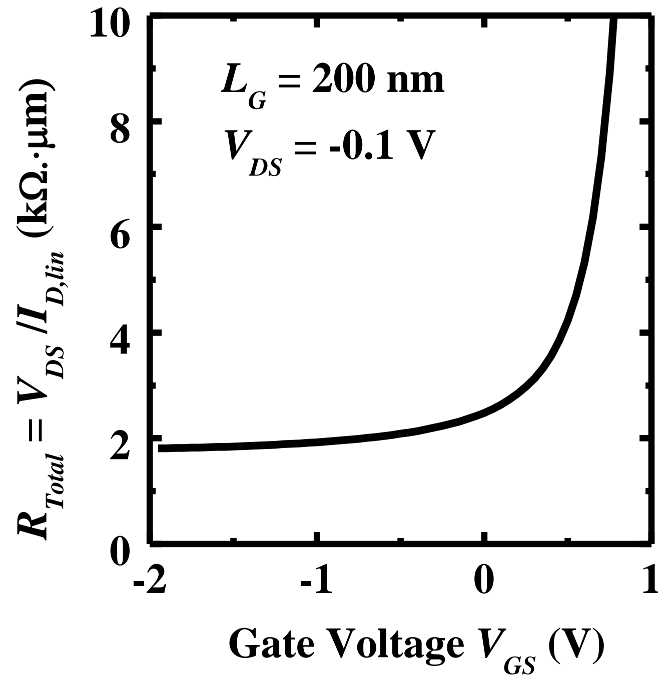


Fig. 5.17. R_{Total} measured at V_{DS} of -0.1 V as a function of V_{GS} for a $Ge_{0.95}Sn_{0.05}$ device with L_G of 200 nm. R_{SD} was extracted to be ~1.7 kΩ·μm.

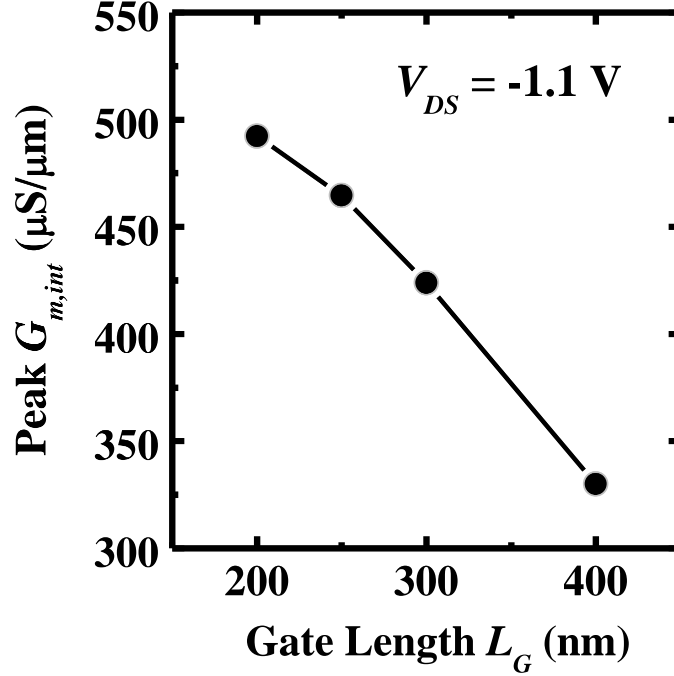


Fig. 5.18. Peak $G_{m,int}$ at V_{DS} of -1.1 V as a function of L_G shows the good scalability of $Ge_{0.95}Sn_{0.05}$ short channel devices, with the highest peak $G_{m,int}$ of ~492 µS/µm achieved at L_G of 200 nm.

As $G_{m,ext}$ is affected by both carrier mobility and R_{SD}, in order to take out the effect of R_{SD}, the intrinsic transconductance $G_{m,int}$ was extracted using [139]:

$$G_{m,int} = \frac{G_m^0}{1-(R_S+R_D)\cdot G_D(1+R_S\cdot G_m^0)}, \tag{5.3}$$

$$G_m^0 = \frac{G_{m,ext}}{1-R_S\cdot G_{m,ext}}, \tag{5.4}$$

where G_D is the measured drain conductance. Shown in Fig. 5.18 is the peak $G_{m,int}$ at V_{DS} of -1.1 V as a function of L_G. The highest peak $G_{m,int}$ value of ~492 µS/µm was obtained at L_G of 200 nm. With reduction of R_{SD} and further gate length scaling, higher drive current and transconductance are expected. It should be noted that

although the effect of R_{SD} has been taken out, when L_G scales from 400 nm to 200 nm, the peak $G_{m,int}$ only increases from 325 to 492 μS/μm (not a ratio of 2). This should be due to the degradation of carrier mobility when the transistor gate length reaches nanometer dimensions in which the ballistic transport can be an important limitation of the mobility. Similar observations have also been reported in Si MOSFETs [140],[141]. For ultimate short nanometer devices, the channel conductivity may be determined not by the carrier scattering time, but by the transit time that is of the order of L_G/v_{th} where v_{th} is the carrier thermal velocity and L_G is the transistor gate length [141].

5.4 Summary

In this Chapter, two techniques were explored for further enhancing the drive current of $Ge_{1-x}Sn_x$ P-MOSFETs: choice of substrate surface orientation and transistor gate length scaling.

In Section 5.2, $Ge_{0.958}Sn_{0.042}$ P-MOSFETs with implantless NiGeSn metal S/D were fabricated on (100)- and (111)-oriented substrates. The dependence of device performance on the crystal orientation of $Ge_{0.958}Sn_{0.042}$ P-MOSFETs was studied. Low-temperature Si_2H_6 treatment was effective in passivating both $Ge_{0.958}Sn_{0.042}$ (100)- and (111)-oriented surfaces. We found that the (111) $Ge_{0.958}Sn_{0.042}$ crystal orientation gives higher hole mobility and drive current.

In Section 5.3, the first short channel $Ge_{0.95}Sn_{0.05}$ P-MOSFETs with self-aligned NiGeSn metal S/D were realized using a gate-first process. A transistor with L_G of 200 nm demonstrates decent transfer characteristics and high intrinsic transconductance of ~295 μS/μm at V_{DS} of -0.6 V. Mobility degradation was observed for transistors with L_G less than 400 nm.

Chapter 6

Uniaxially Strained Germanium-Tin Nanowire Gate-All-Around P-Channel Metal-Oxide-Semiconductor Field-Effect Transistors Enabled by a Novel Top-Down Nanowire Formation Technology

6.1 Introduction

Germanium-Tin (GeSn) p-channel metal-oxide-semiconductor field-effect transistors (P-MOSFETs) with encouraging drive current performance have been demonstrated [27]-[29], and are promising candidates to replace Si P-MOSFETs at 11 nm technology node and beyond. Much attention has been focused on the interface engineering between the high-*k* dielectric and GeSn channel to reduce the interface trap density (D_{it}), which is critical for realizing steep subthreshold swing S and large drive current. However, utilizing advanced device structures such as non-planar three-dimensional (3D) structure becomes equally important as device dimension reaches sub-100 nm regime, because they can give benefits of improved control of short channel effects (SCEs), enhanced volume inversion in the channel region, and a lower off-state leakage current. As Si complementary metal-oxide-semiconductor

(CMOS) manufacturing enters a new era with the "tri-gate" design at 22 nm node, similar non-planar 3D approach needs to be explored for its high mobility channel counterparts. InGaAs n-channel metal-oxide-semiconductor field-effect transistors (N-MOSFETs) [67]-[70],[141] and Ge channel P-MOSFETs [71]-[77] with 3D structures have been extensively explored recently, with very promising results achieved. However, there has been no report of GeSn P-MOSFETs with similar advanced structures. In addition, uniaxial compressive strain has recently been experimentally shown to be even more effective in enhancing the hole mobility of Ge than biaxial compressive strain, and this was achieved by nanowire (NW) formation from biaxially strained Ge [77]. The ability to obtain uniaxial compressive strain by etching NWs from a biaxially strained layer, together with the need for 3D device architectures for control of SCEs at extremely scaled dimensions, makes it particularly attractive to form short channel GeSn NW P-MOSFETs from biaxially strained GeSn, which has not been reported before.

In this Chapter, uniaxially compressive strained GeSn GAA NW P-MOSFETs with HfO_2/WN gate stack using a fully CMOS compatible top-down fabrication method was demonstrated for the first time. A novel H_2O_2-based wet etch was developed to realize GeSn NWs. SF_6 treatment and low temperature Si_2H_6 passivation were used to passivate the GeSn NWs to achieve good interface between high-k dielectric and GeSn channel. The process modules were integrated in a GeSn NW GAA P-MOSFETs fabrication flow to realize channel length (L_{CH}) down to 100 nm. Drive current I_{Dsat} of over 600 μA/μm was obtained with peak intrinsic transconductance $G_{m,int}$ of ~573 μS/μm at V_{DS} of -1 V. Simulations show that uniaxial

compressive strain leads to a significant reduction of the hole effective mass and an increase in the separation between light hole (LH) and heavy hole (HH) bands of GeSn compared to unstrained and biaxially compressive strained GeSn, which could enhance hole mobility.

6.2 Novel Process Technology for $Ge_{1-x}Sn_x$ Nanowire Formation

To realize $Ge_{1-x}Sn_x$ GAA NW P-MOSFETs, one of the critical steps is to form the $Ge_{1-x}Sn_x$ NW. In this Section, $Ge_{1-x}Sn_x$ NW formation process was developed using a top-down two-step process: SF_4-based dry etch followed by H_2O_2-based wet etch.

The starting substrate comprises $Ge_{1-x}Sn_x$ film with a thickness of ~35-50 nm grown on n-type Ge(100) using molecular beam expitaxy (MBE) tool at 180 ˚C. A 20 nm-thick SiO_2 layer was deposited by sputter before patterning a single layer NEB 22 resist by E-beam lithography (EBL). A SF_6-based reactive-ion etch (RIE) was then performed to etch away the SiO_2 and stop at the $Ge_{1-x}Sn_x$ surface. Right after that, a mixed etching gas comprising SF_6 and CHF_3 was then used to etch the $Ge_{1-x}Sn_x$ film and ~150 nm of the underneath Ge layer in the same chamber. The etch rate of the $Ge_{1-x}Sn_x$ and Ge layer was measured to be ~60 nm/minute. Detailed recipe for etching $Ge_{1-x}Sn_x$ and Ge layers in the RIE tool is shown in Table 6.1.

Table 6.1. Recipe used to etch the $Ge_{1-x}Sn_x$ film and the underneath Ge layer in the RIE tool.

Chamber Pressure (mTorr)	**25**
RF Power (W)	**150**
DC Power (W)	**150**
Flow Rate of Ar (sccm)	**75**
Flow Rate of CHF_3 (sccm)	**50**
Flow Rate of SF_6 (sccm)	**25**

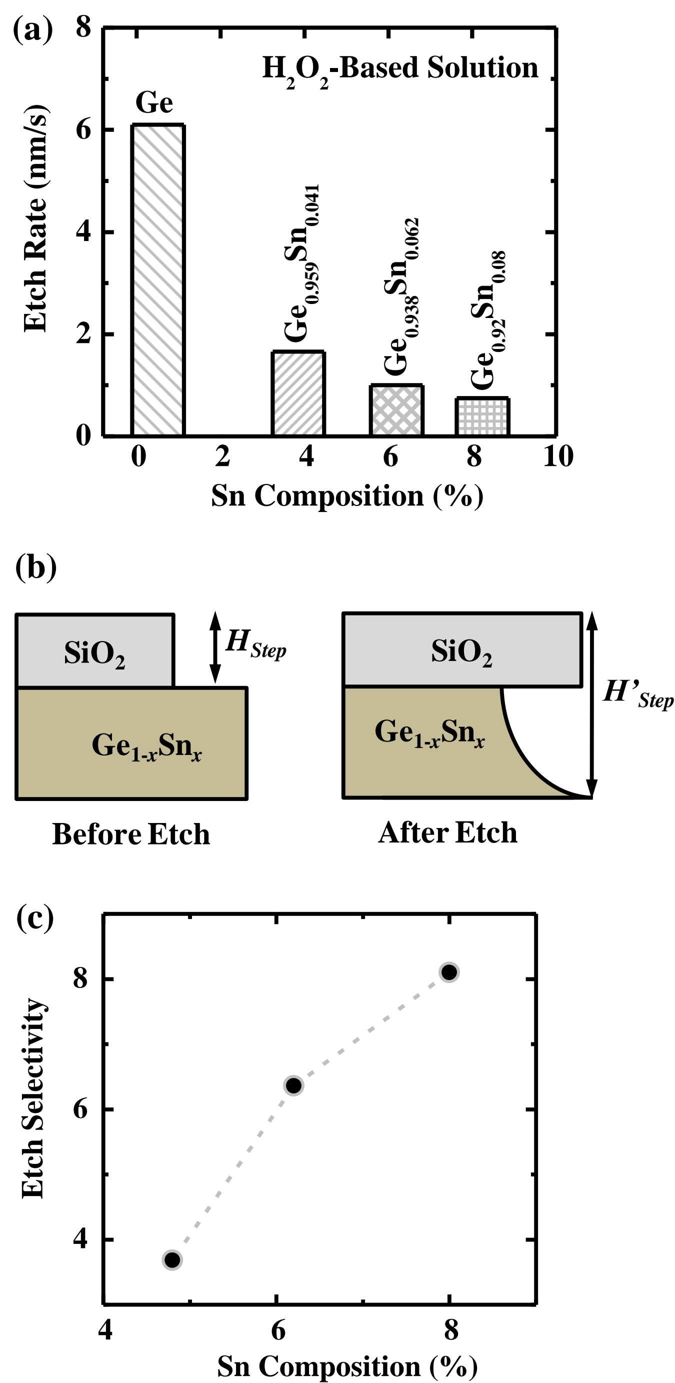


Fig. 6.1. (a) The etch rate of $Ge_{1-x}Sn_x$ decreases with increasing Sn composition. The wet etch rate is calculated as the step height difference before and after the wet etch over the etch time, as illustrated by the schematics shown in (b). Good etch selectivity of Ge with respect to $Ge_{1-x}Sn_x$ is demonstrated, as shown in (c).

After that, the Ge layer underneath the $Ge_{1-x}Sn_x$ fin was selectively etched by a H_2O_2-based solution at room temperature, releasing the $Ge_{1-x}Sn_x$ film from the Ge substrate. The volume ratio of the mixed etchant NH_4OH: H_2O_2: H_2O is 1 : 2 : 160. The weight percentage values of the NH_4OH and H_2O_2 chemicals are 28% and 31%, respectively. Fig. 6.1 (a) summarizes the wet etch rate of $Ge_{1-x}Sn_x$ films with different Sn composition ranging from 0 to 8 %. The wet etch rate is calculated as the step height difference before and after the wet etch over the etch time, as illustrated by the schematics shown in Fig. 6.1 (b). With increasing Sn composition from 0 to 8%, the etch rate slows down from ~6 to 0.75 nm/s. The etch selectivity of Ge over $Ge_{1-x}Sn_x$, defined as the etch rate of Ge divided by the etch rate of $Ge_{1-x}Sn_x$, is calculated to increase from 1 to 8.1, as shown in Fig. 6.1 (c). Since the wet etch process etches Ge at a much faster rate as compared to $Ge_{1-x}Sn_x$ alloys with Sn composition larger than 4%, the Ge region under the $Ge_{1-x}Sn_x$ patterns can be eventually removed.

Finally, a 2-minute dip in diluted HF (HF: H_2O = 1: 50) was performed to fully remove the SiO_2 hard mask. Fig. 6.2 (a) shows a top-view *scanning electron microscope* (SEM) image of a $Ge_{1-x}Sn_x$ NW test structure after the selective wet etch and SiO_2 removal. The tilt-view SEM in Fig. 6.2 (b) confirms the successful release of the $Ge_{1-x}Sn_x$ NW with very good selectivity [Fig. 6.3 (c)]. SEM images of samples with multiple parallel $Ge_{1-x}Sn_x$ NWs are also shown in Fig. 6.2 (d).

So far, the reason for the dependence of the etch rate of $Ge_{1-x}Sn_x$ on Sn composition is not fully understood. One possible reason to explain this may be as follows: Ge and Sn can be oxidized by the H_2O_2-based solution in which GeO_2 and

SnO_2 would be formed on the $Ge_{1-x}Sn_x$ surface. GeO_2 can be dissolved in H_2O but SnO_2 cannot. Therefore, the SnO_2 covering the surface of the $Ge_{1-x}Sn_x$ could protect the $Ge_{1-x}Sn_x$ surface from being etched quickly. Increasing the Sn composition would increase the percentage of SnO_2 on the $Ge_{1-x}Sn_x$ surface. Therefore, a higher Sn composition gives a slower etch rate of the $Ge_{1-x}Sn_x$.

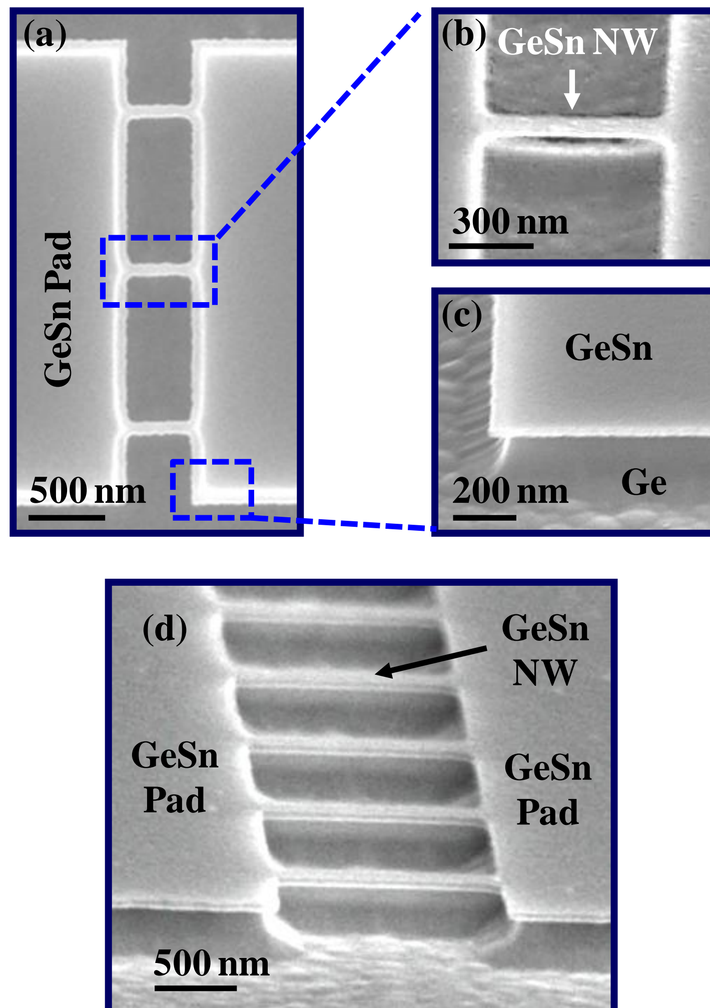


Fig. 6.2. (a) Top-view SEM image of a GeSn NW test structure after selective wet etch and SiO_2 removal. (b) Tilt-view SEM confirms the GeSn NW release, with (c) very good selectivity achieved. (d) Tilt-view SEM image with multiple parallel GeSn NWs formed.

6.3 Uniaxially Strained Germanium-Tin (GeSn) Nanowire

In Si CMOS technology, strain engineering has been extensively explored to change the band structure of Si channel and enhance the drive current [143]-[147]. In this Section, two dimensional (2D) finite element numerical simulations were performed to investigate the stress profile in the GeSn NW. The Sn composition of the GeSn NW simulated is 4.2%. The simulated NW has length, width, and height of 500, 50 and 50 nm, respectively. The boundary conditions are such that the bottom of the Ge substrate is rigid in the vertical direction, and the sides of the domain are assumed to have horizontal displacements. Isotropic approximation was used in the stress simulation.

The stress contour in the longitudinal and transverse directions of the $Ge_{0.959}Sn_{0.041}$ NW is shown in Fig. 6.3 (a) and (b), respectively. Uniaxial longitudinal compressive stress was induced in the $Ge_{0.959}Sn_{0.041}$ NW. Larger stress was observed at the top surface of the $Ge_{0.959}Sn_{0.041}$ NW where the inversion layer would be formed in GeSn GAA NW P-MOSFETs. This could be contributing favorably to drive current and carrier transport enhancement. Asymmetric stress in Ge NW P-MOSFETs was found to enhance the hole mobility significantly as compared with biaxial stress [77]. Fig. 6.4 shows the average longitudinal stress in the region where inversion charge flows, i.e. top 5 nm of the NW surface. The magnitude increases with smaller NW length, indicating scalability of this structure.

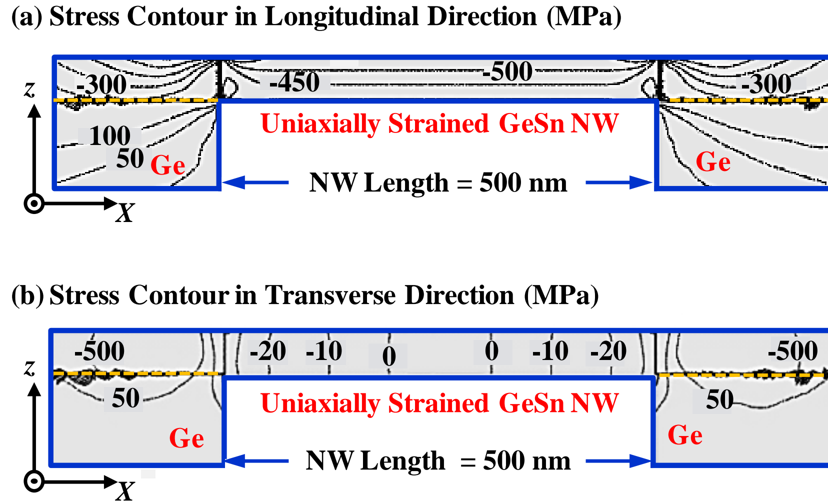


Fig. 6.3. Stress contour in (a) longitudinal and (b) transverse directions of the $Ge_{0.959}Sn_{0.041}$ NW. Uniaxial longitudinal compressive stress was induced in the $Ge_{0.959}Sn_{0.041}$ NW. Larger stress was observed at the top surface of the $Ge_{0.959}Sn_{0.041}$ NW where the inversion layer would be formed.

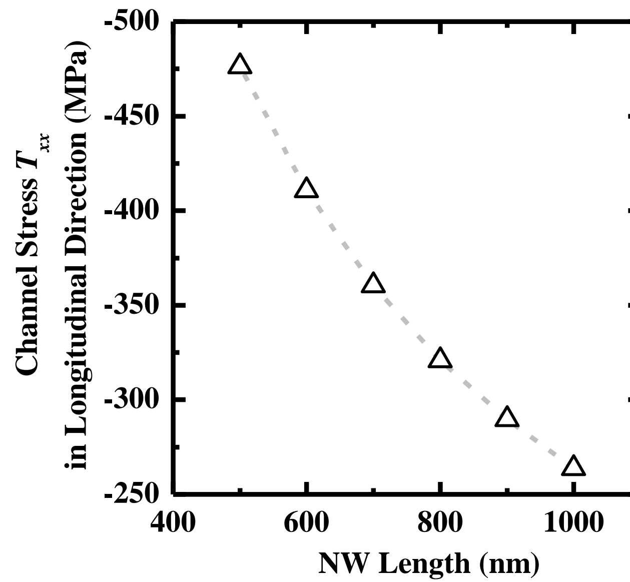


Fig. 6.4. Average longitudinal stress magnitude in the region where inversion charge flows, i.e. top 5 nm of the NW surface. The magnitude increases with smaller NW length, indicating scalability of this structure.

6.4 Reduction in Effective Mass and Interband Scattering by Uniaxial Compressive Strain

In order to study the effect of strain on the band structure of $Ge_{0.959}Sn_{0.041}$, simulation was perfromed using Nextnano. Fig. 6.5 (a)-(c) show the 3D equi-energy surfaces (E = 30 meV) of $Ge_{0.959}Sn_{0.041}$ topmost valence band with no strain, 0.63% biaxial compressive strain, and 0.63% uniaxial compressive strain along [110] direction, respectively. The corresponding E-k diagrams of three cases are shown in Fig. 6.5 (d)-(f).

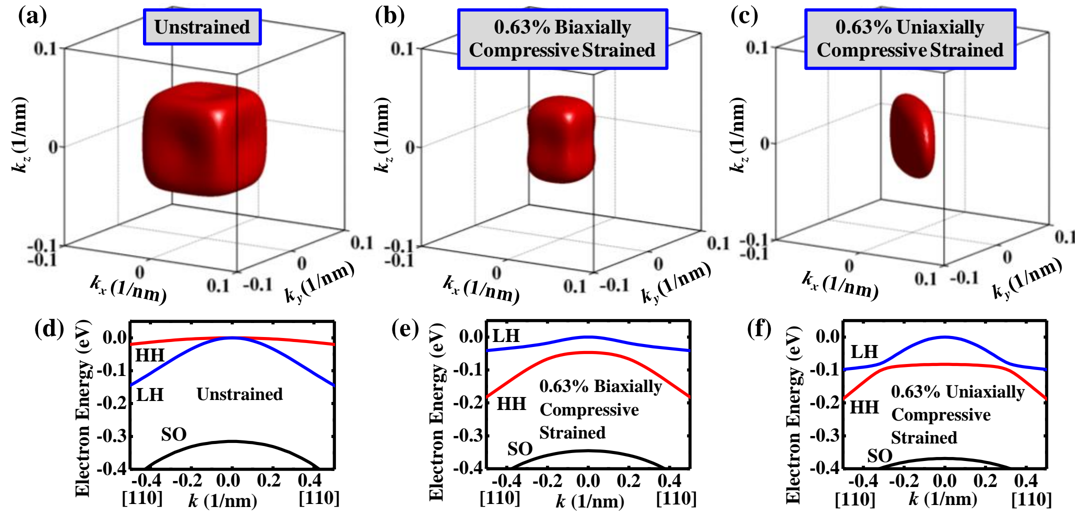


Fig. 6.5. 3D equi-energy surfaces (E = 30 meV) of $Ge_{0.959}Sn_{0.041}$ top valence band with (a) no strain, (b) with 0.63% biaxial compressive strain, and (c) with 0.63% uniaxial compressive strain along [110] direction. As shown in the E-k diagrams of $Ge_{0.959}Sn_{0.041}$ in (d), (e), and (f), the uniaxial strain not only leads to more warping of the topmost valence band, but also increases separation between bands of LH and HH, as compared with unstrained and biaxial strain cases. Both effects are beneficial to enhance the hole mobility of $Ge_{0.959}Sn_{0.041}$.

Two effects induced by uniaxial compressive strain are beneficial to enhance the hole mobility of $Ge_{0.959}Sn_{0.041}$, as compared with unstrained and biaxial compressive strain cases. First, more bandwarping induced by uniaxial compressive strain produces reduced effective mass for the topmost valence band where holes primarily occupy, as shown in Fig. 6.6. Second, the uniaxial compressive strain increases light hole (LH) to heavy hole (HH) band separation, reducing the inter-valley scattering.

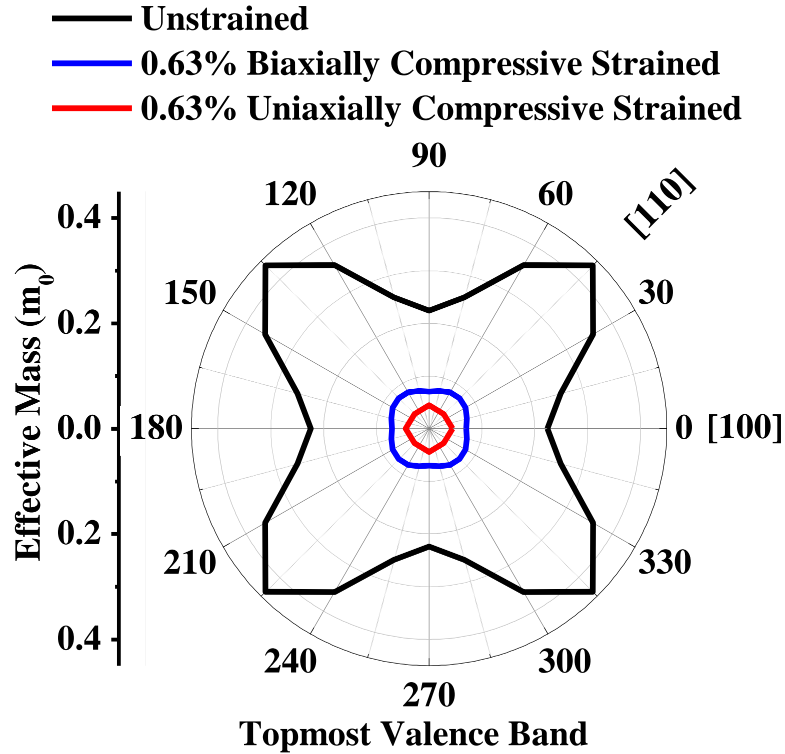


Fig. 6.6. Uniaxial compressive strain can realize significant reduction of effective mass of the topmost valence band where holes primarily occupy. This leads to higher hole mobility as compared with the unstrained and biaxial compressive strain cases.

6.5 Fabrication and Characterization of $Ge_{0.959}Sn_{0.041}$ GAA NW P-MOSFETs

6.5.1 Device Fabrication

Fig. 6.7 (a) summarizes the process flow for fabrication of the $Ge_{0.959}Sn_{0.041}$ GAA NW P-MOSFETs. The 3D schematics in Fig. 6.7 (b), (c), (d), and (e) show the structures after the steps of source/drain (S/D) formation, $Ge_{0.959}Sn_{0.041}$ fin definition, $Ge_{0.959}Sn_{0.041}$ NW formation, and the gate definition, respectively.

$Ge_{0.959}Sn_{0.041}$ film with a thickness of ~35 nm was first epitaxially grown on n-type Ge(100) using solid source MBE system at 180 ºC. Phosphorus well implant was performed at energy of 20 keV and a dose of 7×10^{12} cm^{-2}, and activated at 450 ºC for 180 s. A SiO_2 layer of ~20 nm was deposited by sputter, and a dummy resist gate pattern was defined by EBL. BF_2^+ implant was then performed at energy of 30 keV and a dose of 1×10^{15} cm^{-2}, and activated at 500 ºC for 60 s. The dummy gate pattern defined the channel length L_{CH}, and was subsequently removed. Fin lithography was performed by EBL before a F-based plasma etch to define the fins. A H_2O_2-based solution removed the Ge under the $Ge_{0.959}Sn_{0.041}$ fin to form the $Ge_{0.959}Sn_{0.041}$ NWs. This is a key enabling process (details were discussed in Section 2 of this Chapter).

A cyclic process was used for pre-gate cleaning, which involves treating the wafers with deionized water followed by hydrofluoric (HF) acid (HF:H_2O = 1:50) in each cycle. After pre-gate clean, samples were loaded into an ultra-high vacuum tool for native oxide removal by SF_6 plasma and sub-400 ºC *in situ* Si_2H_6 passivation to form a high-quality Si passivation layer. This was followed by deposition of 7 nm-

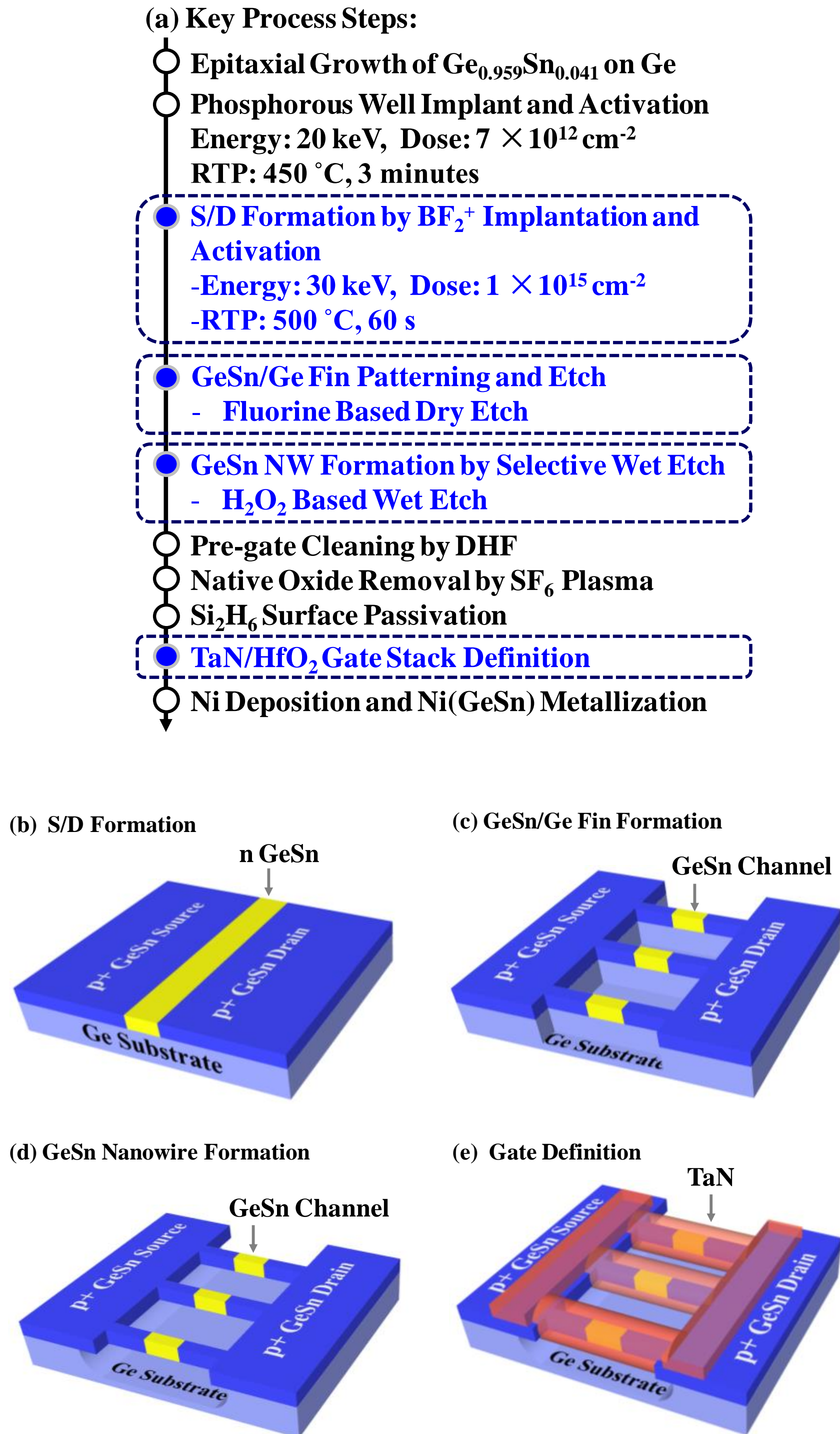


Fig. 6.7. (a) Key process steps for fabricating GeSn GAA NW P-MOSFETs. The 3D schematics show the structures after the steps of (b) S/D formation, (c) GeSn fin definition, (d) removal of Ge under GeSn, and (e) gate definition.

thick HfO_2 by atomic layer deposition (ALD) tool at temperature of 250 ºC. ~200 nm WN metal was deposited by sputter as the gate electrode. Gate etch process was performed using F-based plasma etch. The F-based dry etching chemistry provides excellent selectivity between WN and HfO_2, giving a damage-free gate dielectric. Finally, Ni was deposited at the S/D contact regions and followed by rapid thermal anneal (RTA) at 350 ºC for 30 s to form the NiGeSn metal contact.

Fig. 6.8 shows the high-resolution transmission electron microscope (HRTEM) image of ~35 nm $Ge_{0.959}Sn_{0.041}$ film on Ge(100). Defect free $Ge_{0.959}Sn_{0.041}$/Ge interface and the high crystallinity of the $Ge_{0.959}Sn_{0.041}$ film were observed. High resolution X-ray diffraction (XRD) (004) and (224) curves in Fig. 6.9 show that the substitutional Sn composition is ~4.2% and the film is fully strained. The well-defined peaks indicate excellent quality of the $Ge_{0.959}Sn_{0.041}$ channel material. In the device fabrication, the choice of Sn composition is important as a high Sn composition increases the selectivity between $Ge_{1-x}Sn_x$ over Ge, but could also increase the off-state current due to the lower bandgap with higher Sn composition.

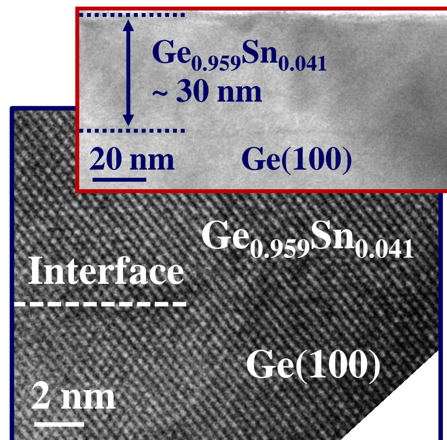


Fig. 6.8. HRTEM images of epitaxial $Ge_{0.959}Sn_{0.041}$grown on Ge(100) substrate show the defect free interface and high quality $Ge_{0.959}Sn_{0.041}$ film.

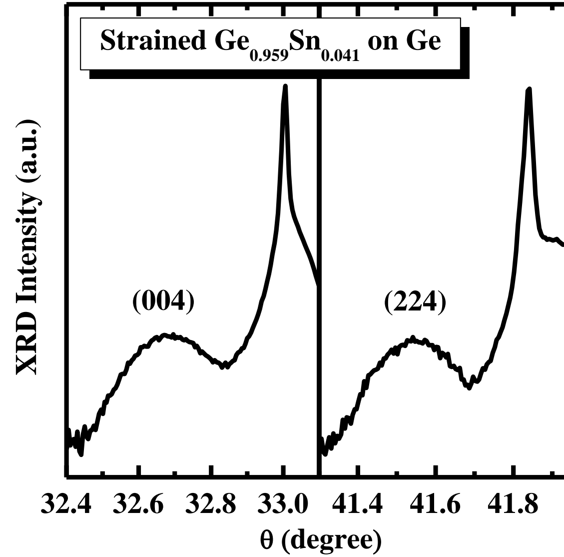


Fig. 6.9. HRXRD (004) and (224) curves show that the GeSn film has a 4.2% substitutional Sn. The well-defined peaks indicate excellent quality of the $Ge_{0.959}Sn_{0.041}$ channel material.

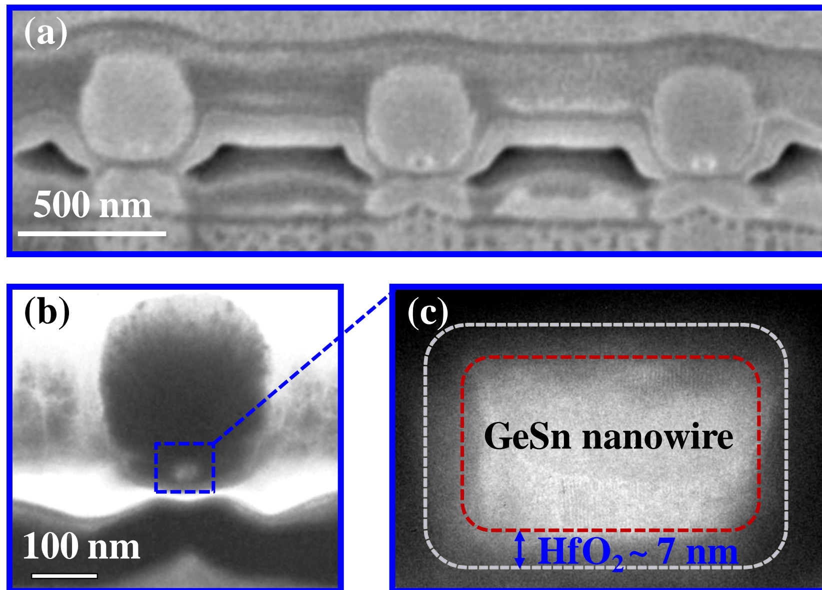


Fig. 6.10. (a) Cross-sectional SEM image shows GeSn GAA MOSFETs with 3 parallel wires. (b) TEM image of one GeSn NW wrapped by high-*k* HfO_2 and WN metal. The GeSn NWs were released and surrounded by WN/HfO_2. (c) HRTEM shows a GeSn NW with width of 50 nm and height of ~35 nm.

Fig. 6.10 (a) shows the cross-sectional *SEM* of the GeSn GAA MOSFETs with 3 parallel wires. The TEM image in Fig. 6.10 (b) clearly shows that the GeSn NW was released and surrounded by the high-*k*/metal gate stack. GeSn NW with width of ~50 nm and height of ~35 nm was realized with the novel NW formation process, as shown in Fig. 6.10 (c).

6.5.2 Electrical Characterization

Fig. 6.11 (a) shows the I_D-V_{GS} curves of a GeSn GAA NW P-MOSFET with L_{CH} of 500 nm. Decent transfer characteristics were achieved. Output characteristics of the same P-MOSFET are shown in Fig. 6.11 (b). The current is normalized by the total perimeter of 15 NWs.

Fig. 6.12 (a) shows the extrinsic and intrinsic transconductance of a P-MOSFET with L_{CH} of 250 nm at V_{DS} of -1 V, with high peak $G_{m,int}$ of ~465 µS/µm. High I_{Dsat} of ~490 µA/µm at an overdrive of -2 V and V_{DS} of -2 V was obtained, as shown in the I_D-V_{DS} plot of the same transistor in Fig. 6.12 (b).

The transconductance and drive current are severely affected by the high S/D series resistance R_{SD}. Fig. 6.13 plots the total resistance R_{Total} versus V_{GS} for the same device in Fig. 6.11. The R_{Total} of a transistor measured at low drain bias decreases with increasing gate bias V_{GS}, and approaches R_{SD} at large V_{GS} of 5 V. The extracted R_{SD} is around 3.3 kΩ·µm. This value is quite high as compared with other NiGe contacts reported [22]. The high R_{SD} is due to the long extension resistance between channel edge and S/D pads, and can be reduced with raised or epitaxial S/D. Higher

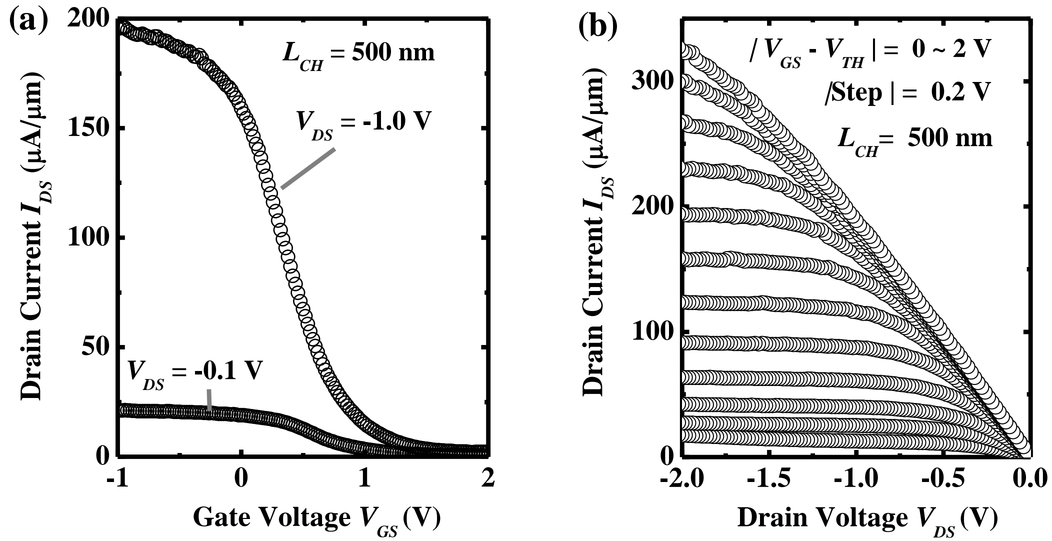


Fig. 6.11. (a) I_D-V_{GS} plot showing decent transfer characteristics of a GeSn GAA NW MOSFET with L_{CH} of 500 nm. (b) Output characteristics of the same transistor shown in (a). The current is normalized by the total perimeter of 15 NWs.

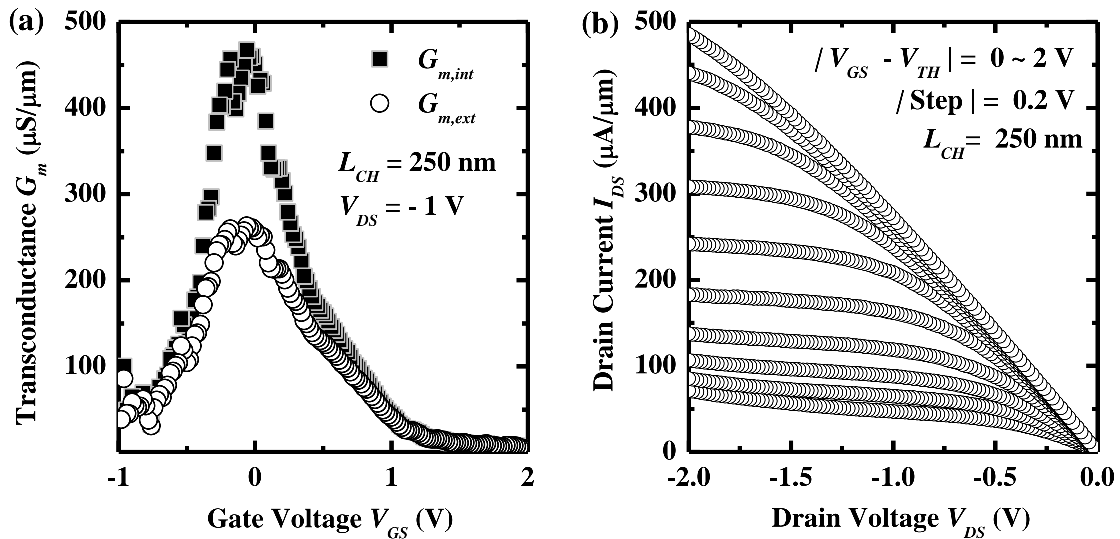


Fig. 6.12. (a) G_m-V_{GS} curves for a GeSn GAA NW P-MOSFET with L_{CH} of 250 nm show high peak $G_{m,int}$ of 465 µS/µm at V_{DS} of -1 V. Drive current of ~500 µA/µm was achieved at V_{GS}-V_{TH} of -2 V and V_{DS} of -2 V, as shown in the I_D-V_{DS} plot of the same transistor shown in (a).

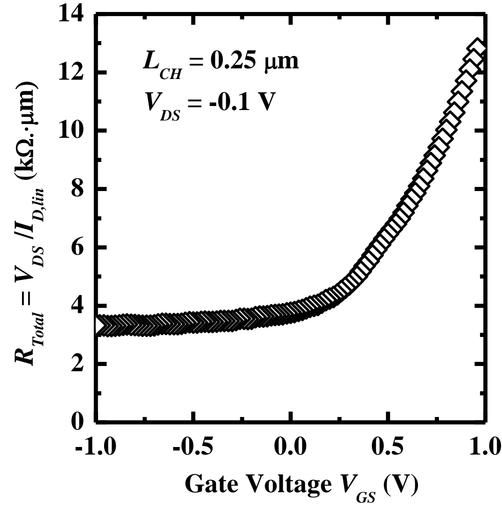


Fig. 6.13. R_{Total} measured at V_{DS} of -0.1 V as a function of V_{GS} for a GeSn GAA NW MOSFET with L_{CH} of 250 nm. R_{SD} was extracted to be ~3.3 kΩ·μm.

I_{Dsat} is expected with further device optimization, e.g. scaling of capacitance equivalent thickness (CET) and R_{SD} reduction.

Fig. 6.14 (a) and (b) show the scaling metrics of the peak $G_{m,int}$ at V_{DS} of -1 V, and I_{Dsat} at an overdrive of -2 V and V_{DS} of -2 V, respectively, for transistors with L_{CH} ranging from 100 nm to 500 nm. Peak $G_{m,int}$ was extracted using [139]:

$$G_{m,int} = \frac{G_m^0}{1-(R_S+R_D)\cdot G_D(1+R_S\cdot G_m^0)}, \quad (6.1)$$

$$G_m^0 = \frac{G_{m,ext}}{1-R_S\cdot G_{m,ext}}, \quad (6.2)$$

where G_D is the measured drain conductance. With a L_{CH} of 100 nm, $G_{m,sat}$ of 573 μS/μm was obtained at V_{DS} of -1 V. I_{Dsat} at an overdrive of -2 V and V_{DS} of -2 V was higher than 600 μA/μm was also achieved. Similar trend of mobility degradation was observed when the L_{CH} scales to sub-350 nm.

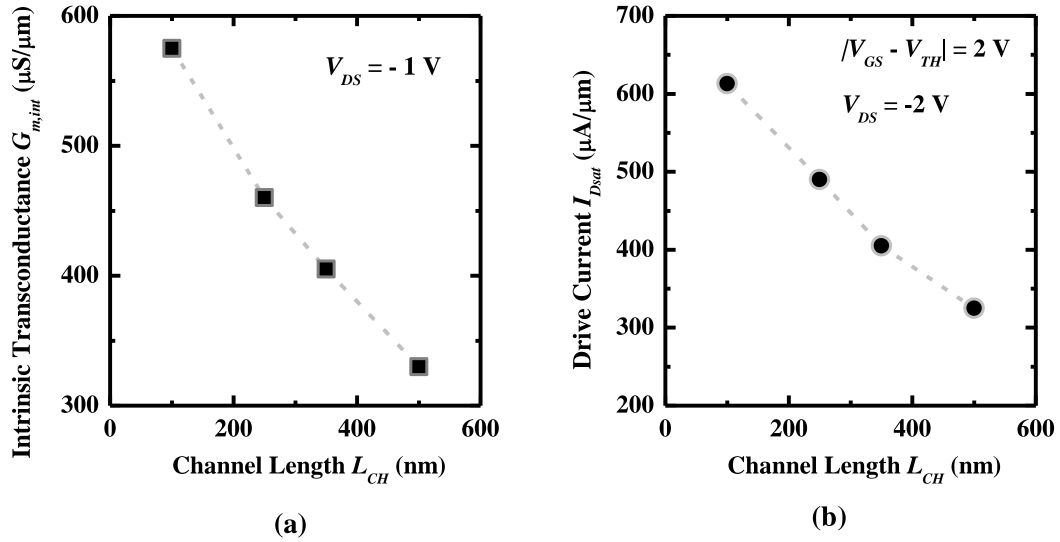


Fig. 6.14. (a) Peak $G_{m,int}$ at V_{DS} of -1.1 V, and (b) I_{Dsat} at an overdrive of -2 V and V_{DS} of -2 V as a function of L_{CH}. Degradation in carrier mobility was observed when the transistor scales to sub-350 nm.

6.6 Summary

In this Chapter, we discussed the first GeSn GAA NW P-MOSFETs realized using CMOS compatible process modules.

In Section 6.2, a top-down two-step etch process including a novel wet etch with high selectivity of Ge over GeSn was developed to enable the realization of GeSn NWs. It was observed that a higher Sn composition in GeSn leads to a slower etch rate of GeSn in H_2O_2-based solution. Section 6.3 studies the stress contour of the GeSn NW by finite element simulation. The impact of NW length on the stress profile was also evaluated. Simulation results in Section 6.4 show that the uniaxial compressive strain could achieve significatnt reduction in hole effective mass and interband scattering, as compared with unstrained and biaxial compressive strained cases. In Section 6.5, the first GeSn GAA NW P-MOSFETs with NW width of 50 nm, height of 35 nm, and L_{CH} down to 100 nm, were realized with good I_{Dsat}. This technology is a promising option for future extremely-scaled high performance P-MOSFETs with GeSn as the channel material.

Chapter 7

Conclusion and Future Work

7.1 Conclusion and Contributions of This Thesis

As continuous transistor scaling and performance improvement of conventional Si metal-oxide-semiconductor field-effect transistors (MOSFETs) are facing grand challenges, novel technologies and device structures are required to further enhance the drive current of the MOSFETs at a reduced supply voltage. This thesis has sought to explore the potential of InGaAs as alternative n-channel material and GeSn as p-channel material to enable a new class of nanometer-scale transistors for future high performance and low power logic applications. The major conclusion and contributions of this work are elucidated here.

7.1.1 Raised Source/Drain (S/D) with *In situ* Doping for Series Resistance Reduction of $In_{0.7}Ga_{0.3}As$ N-MOSFETs

Raised S/D structure with *in situ* doping process was demonstrated in InGaAs channel N-MOSFETs with indium composition as high as 70 %. A selective epitaxy process using metal organic chemical vapor deposition (MOCVD) was first developed to grow high quality InGaAs film. The process module was then integrated into a self-aligned gate-first process to fabricate the $In_{0.7}Ga_{0.3}As$ N-MOSFETs. Significant S/D series resistance (R_{SD}) reduction was achieved due to combined contributions from the high S/D doping concentration as well as the

structural improvement in the raised S/D structure. This technique is attractive to reduce the R_{SD} of InGaAs N-MOSFETs to explore the full potential of InGaAs as an n-channel material for future technology nodes.

7.1.2 Advanced Gate Stack Technologies for $In_{0.7}Ga_{0.3}As$ N-MOSFETs

The concept and demonstration of novel surface passivation techniques were exploited to realize high-quality metal gate/high-*k* dielectric stacks on InGaAs. For the first time, the realization of InP-capped $In_{0.7}Ga_{0.3}As$ N-MOSFETs formed using a gate-first process was achieved. The TaN/Al_2O_3 gate stack formed on $InP/In_{0.7}Ga_{0.3}As$ is thermally stable after 600 ºC 60 s dopant activation anneal. Introducing InP capping layer in $In_{0.7}Ga_{0.3}As$ N-MOSFETs was found to reduce the subthreshold swing *S* and increase the drive current. In addition, low temperature Si_2H_6 passivation was developed to effectively passivate the $In_{0.7}Ga_{0.3}As$ surface. When integrated with the atomic layer deposition (ALD) deposited HfO_2 to realize $In_{0.7}Ga_{0.3}As$ N-MOSFETs, capacitance equivalent thickness (CET) of ~1.6 nm with low gate leakage current density was achieved, and *S* comparable to the best reported in the literature was obtained. Both interface engineering techniques are highly compatible with a matured high-*k* dielectric deposition process, and provide promising options for interface passivation to explore the full potential of InGaAs channel N-MOSFETs.

7.1.3 GeSn P-MOSFETs with High Hole Mobility and Excellent Negative Bias Temperature Instability (NBTI) Reliability Realized by Low Temperature Si_2H_6 Passivation

Low temperature Si_2H_6 passivation was developed to realize GeSn P-MOSFETs, which exhibit smaller *S* and higher effective carrier mobility as compared with $(NH_4)_2S$-passivated ones. The Si_2H_6-passivated GeSn P-MOSFETs also show excellent NBTI reliability with very small threshold voltage (V_{TH}) shift as well as negligible degradation of *S* and peak transconductance. For the first time, a common gate stack technology comprising 370 ºC Si_2H_6 passivation and TaN/HfO_2 gate stack was proposed and demonstrated for InGaAs and GeSn complementary metal-oxide-semiconductor (CMOS) devices for cost effective integration. Symmetric V_{TH}, low gate leakage, and very high drive current were achieved for InGaAs N-MOSFETs and GeSn P-MOSFETs.

7.1.4 Performance Enhancement for GeSn P-MOSFETs: Surface Orientation and Gate Length Scaling

The dependence of device performance on the crystal orientation of $Ge_{0.958}Sn_{0.042}$ P-MOSFETs was studied for the first time. $Ge_{0.958}Sn_{0.042}$ (111) crystal orientation gives higher hole mobility and drive current as compared with (100) orientation. The results open new avenues to improve the drive current of GeSn P-MOSFETS by choice of surface orientations. In addition, the world's first short-channel GeSn P-MOSFETs with self-aligned NiGeSn metal S/D were realized using a gate-first process. A transistor with gate length L_G of 200 nm demonstrates decent transfer characteristics and high peak intrinsic transconductance $G_{m,int}$ of ~295 μS/μm

at V_{DS} of -0.6 V. The results illustrate the potential of GeSn as a promising p-channel material for future high performance and low power logic application.

7.1.5 Uniaxially Strained GeSn Gate-All-Around (GAA) Nanowire (NW) P-MOSFETs

The uniaxially compressive strained GeSn GAA NW P-MOSFETs with the shorted reported channel length L_{CH} down to 100 nm were demonstrated for the first time. The uniaxially compressive strained GeSn NW with a width of 50 nm and a height of 35 nm was fabricated using a CMOS compatible top-down approach. The devices achieve a record high peak $G_{m,int}$ of 573 μS/μm at V_{DS} of -1.0 V for GeSn P-MOSFETs. Simulations show that uniaxial compressive strain leads to a significant reduction of the hole effective mass and an increase in the separation between light hole (LH) and heavy hole (HH) bands of GeSn compared to unstrained and biaxially compressive strained GeSn, which could enhance hole mobility. The GeSn NW formation technology shows promise for integration in future high performance GeSn P-MOSFETs.

7.2 Future Directions

7.2.1 Integration of InGaAs and GeSn on Silicon Substrates

Given the maturity and the advanced state of silicon manufacturing technology, it is very unlikely that any materials other than silicon will be used for the overall substrate in mainstream manufacturing [78]. Therefore, integration of potential new channel materials (perhaps InGaAs as n-channel material and Ge or GeSn as p-channel material) into the Si platform in a cost effective way is every important.

7.2.2 Novel Strain Techniques to Enhance the Hole Mobility of GeSn P-MOSFETs

The simulation results in Chapter 6 show that both biaxial and uniaxial compressive stress are effective in reducing the hole effective mass of the topmost valence band and increasing the LH to HH band separation of GeSn. Novel techniques which are able to induce the compressive stress in the GeSn channel could experimentally be explored to enhance the hole mobility of GeSn P-MOSFETs, i.e. silicon nitride (SiN) liner stressor [148],[149] or diamond like carbon (DLC) [150], which were found to be beneficial to boost the hole mobility of Si P-MOSFETs due to the introduction of compressive stress to the Si channel.

7.2.3 Extremely Scaled GeSn P-MOSFETs

So far, the smallest L_G realized in GeSn P-MOSFETs is 100 nm. In order to have a better and more compressive assessment of GeSn as the potential channel material for P-MOSFETs in future technology nodes, it is necessary to fabricate the extremely scaled GeSn P-MOSFETs, i.e. with L_G of less than 30 nm, to study the carrier transport characteristics by extracting the source injection velocity and backscattering coefficient. These are two important parameters which determine the drive current of transistors with extremely scaled L_G **Error! Reference source not ound.**

7.2.4 Ultrathin body and NW GeSn P-MOSFETs

Due to much smaller bandgap values of InGaAs with high indium composition and GeSn as compared with Si, high off-state leakage current due to band to band tunneling (BTBT) could be a potential problem for transistors with

extremely scaled L_G, because it degrades subthreshold characteristics and increases the power consumption of transistors. Additional mobility improvement achieved by beneficial strain usually has side effect of further degrading the bandgap values. Fabricating these devices in a quantum-confined system (ultrathin body or NW structures), where the quantum confinement generates strong quantization of the energy levels and a larger effective bandgap, could be a good solution. InGaAs GAA NW N-MOSFETs with a NW width of 20 nm were recently demonstrated to show excellent off-state and *S* characteristics [151]. Although the world's first GeSn GAA NW P-MOSFETs have been demonstrated in Chapter 6, the dimensions of the GeSn NW need to be scaled down to give more quantum confinement effects. In addition, off-state and *S* characteristics still require improvement.

7.2.5 Gate Stack Technology and Strain Engineering for GeSn N-MOSFETs with High Electron Mobility

Given the high electron mobility of bulk GeSn, it is still necessary to work on GeSn N-MOSFETs. Although GeSn N-MOSFETs have recently been reported [30],[38],[39], the electron mobility still needs substantial improvement. One direction is to explore innovative gate stack formation technologies on GeSn. The other direction is to enhance electron mobility by strain engineering.

References

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Appendix

List of Publications

Journal Publications

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