ADVANCED SILICON AND
GERMANIUM TRANSISTORS FOR FUTURE
P-CHANNEL MOSFET APPLICATIONS

LIU BIN

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Declaration

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Liu Bin

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Summary

Continual scaling of silicon (Si) complementary metal-oxide-semiconductor (CMOS) into deep sub-20 nm regime meets some immense challenges which hinder the CMOS development. The motivation of this thesis work is to provide feasible solutions to the short term and long term technical challenges faced by the CMOS technology.

Strain engineering has been used as an effective performance booster since 90 nm technology node. The smaller space available in between the gate electrodes due to aggressive pitch scaling makes the volume of the stressor material become smaller. This would directly compromise strain induced in the channel and performance enhancement. To address this challenge, new diamond-like carbon (DLC) liner stressor with direct integration onto p-channel field-effect transistors (p-FETs) was developed in this work. Without the SiO_2 adhesion layer which was used in previous DLC works, the new DLC liner stressor technique provides better scalability and possibly higher performance enhancement. Successful integrations of the new DLC liner stressor were demonstrated on both short channel planar p-FETs and more advanced and scaled nanowire p-FETs. Substantial performance enhancement was achieved.

Negative Bias Temperature Instability (NBTI) which is one of the most important reliability issues of the state of the art p-FETs, could lead to severe performance degradation of p-FETs, causing threshold voltage shift and drain current degradation. Reported data in the literature on NBTI study of strained p-FETs suggest strain could degrade NBTI performance of p-FETs. In this thesis, NBTI

study was performed using an advanced home-made ultra fast measurement setup on p-FETs with different levels of channel strain, investigating the strain effect on NBTI characteristics. In consistent with other reports, strain induced by DLC was found to degrade NBTI performance of p-FETs. Both strain induced device reliability degradation and drive current enhancement should be carefully considered when designing the transistors.

Ultimately new channel material with high carrier mobility is needed to replace Si for future transistors operating in quasi-ballistic regime in the long term perspective. Germanium (Ge) which has very high carrier mobility is considered as a promising alternative channel material for the future CMOS applications. In this work, we developed high performance Ge multiple-gate FETs (MuGFETs) based on Ge on insulator (GeOI) substrates to have high performance transistors with good short channel control. Si CMOS compatible process modules were developed. Sub-400 ℃ low temperature Si passivation was adopted to form high quality gate stack. Implantless metallic Schottky barrier (SB) source/drain (S/D) was integrated for the first time into Ge MuGFETs to have low S/D series resistance. Effects of fin doping and backside interface charge of GeOI substrates on device electrical characteristics were investigated. High drive current was achieved in this work for Ge MuGFETs fabricated by top-down approaches.

Besides SB S/D, *in-situ* doped raised S/D (RSD) was also developed for the first time for Ge MuGFETs on GeOI using selective epitaxial growth of highly p^+ doped Ge. Good device transfer characteristics and short channel control was achieved on Ge MuGFETs with RSD. Device NBTI reliability was investigated for Ge MuGFETs for the first time.

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List of Symbols

Symbol	Description
A	Cross-sectional area
A^*	Effective Richardson constant
C	Capacitance
C_D	Depletion capacitance
C_{it}	Interface traps capacitance
C_{OX}	Gate oxide capacitance
D_{EFF}	Effective diameter
D_{it}	Interface trap density
E_{eff}	Effective vertical electrical field
G_{AM}	Gain of the amplifier
G_M	Transconductance
$G_{MLinMax}$	Linear saturation transconductance
G_{MSat}	Saturation transconductance
$G_{MSatMax}$	Peak saturation transconductance
H_{FIN}	Fin height
H_{REC}	Oxide recess height
I_{DLin}	Linear drain current
I_{DSat}	Saturation drain current
I_G	Gate leakage current
I_{GP}	G peak intensity
I_{MIN}	Minimum drain current
I_{OFF}	Off-state current
I_{ON}	On-state current
I_{DS} or I_D	Drain current
I_{TP}	T peak intensity

L_G	Gate length
L_{GSP}	Gate spacing
L_{PITCH}	Gate pitch
m^*	Hole effective mass
N	Doping concentration
Q_{DEP}	Depletion charge
Q_{IT}	Interface trap
Q_{OX}	Fixed oxide charge
R_{CH}	Channel resistance
R_{EXT}	External series resistance
R_{RSD}	Raised S/D resistance
R_{SPACER}	Resistance due to n-type doped Ge under the spacer
R_{TOTAL}	Total resistance
S	Subthreshold swing
S_{xx}	The stress along the current flow direction
T	Temperature
T_{BOX}	Buried oxide thickness
t_{DLC}	DLC thickness
T_{HM}	Hardmask thickness
T_{OX}	Oxide thickness
V	Voltage
V_{DD}	Supply voltage
V_{DS}	Drain voltage
V_{GS} or V_G	Gate voltage
V_{stress}	Gate stress voltage
V_{sub}	Substrate bias
V_{TH}	Threshold voltage
$V_{TH,lin}$	Linear threshold voltage

$V_{TH,sat}$	Saturation threshold voltage
W	Nanowire linewidth
W_{EFF}	Effective gate width
W_{FIN}	Fin width
W_G	Gate width
W_{SP}	Spacer width
ΔV_{TH}	Threshold voltage shift
ΔV_{TH}^{it}	Threshold voltage shift component due to interface trap generation
ΔV_{TH}^{ox}	Threshold voltage shift component due to oxide charge trapping
μ_{max}	Highest carrier mobility in bulk semiconductor
$\pi_{\parallel}$	Piezoresistance coefficients for the longitudinal direction
$\pi_{\perp}$	Piezoresistance coefficients for the transverse direction
ρ	Resistivity
$\sigma_{\parallel}$	Longitudinal stresses
$\sigma_{\perp}$	Transverse stresses
υ_{inj}	Thermal injection velocity
ϕ_{BH}	Effective hole barrier height
Φ_{MS}	Metal-semiconductor work function different
ψ_S	Surface potential
$\Delta\mu$	Strain induced mobility change
μ_{eff}	Effective mobility

List of Abbreviations

ALD	Atomic layer deposition
AOI	Angle of incident
As	Arsenic
B	Boron
CD	Critical dimension
CESL	Contact etch stop layer
CET	Capacitance equivalent thickness
CMOS	Complementary metal-oxide-semiconductor
CNL	Charge neutrality level
CVD	Chemical vapour deposition
DHF	Dilute hydrofluoric acid
DIBL	Drain induced barrier lowering
DIW	Deionized water
DLC	Diamond-like carbon
DSS	Dopant segregation Schottky
EBL	Electron beam lithography
EOT	Equivalent oxide thickness
FCVA	Filtered cathodic vacuum arc
FGA	Forming gas anneal
FIB	Focused ion beam
GAA	Gate-All-Around
Ge	Germanium
GeO_2	Germanium dioxide
GeOI	Germanium on insulator
GeON	Ge oxynitride

HRTEM	High resolution transmission electron microscopy
IV	Current-voltage
MOSCAP	Metal-oxide-semiconductor capacitors
MOSFET	Metal-oxide-semiconductor field-effect transistor
MuGFET	Multiple-gate field-effect transistors
NBTI	Negative bias temperature instability
NiGe	Nickel germanide
OCD	Optical critical dimension
P	Phosphorus
P-FET	P-channel field-effect transistor
PR	Photoresist
RCWA	Rigorous coupled wave analysis
RDF	Random dopant fluctuation
RIE	Reactive ion etcher
RSD	Raised source/drain
RTP	Rapid thermal processing
S/D	Source/drain
SB	Schottky barrier
SCE	Short channel effect
SE	Spectroscopic ellipsometry
SEM	Scanning electron microscopy
Si	Silicon
SiC	Silicon carbon
SiGe	Silicon germanium
SiN	Silicon nitride
SRIM	Stopping and range of ions in matter
SS	Subthreshold swing
TEM	Transmission electron microscopy

TOF SIMS	Time-of-Flight Secondary Ion Mass Spectrometry
UFM	Ultra fast measurement
UHV	Ultra-high vacuum
VLS	Vapour-liquid-solid

Chapter 1

Introduction

1.1 Background

Metal-oxide-semiconductor field-effect transistor (MOSFET) is the basic element of integrated circuits. For a long period of time, device miniaturization, which scales MOSFET gate length L_G, gate width W_G, and oxide thickness T_{OX}, is the main driver to enhance complementary metal-oxide-semiconductor (CMOS) performance [1]. The motivation to scale down the size of MOSFETs is to improve the circuit speed and increase packing density for a given area of microchip. Classical scaling was sufficient to deliver device performance improvement, before CMOS entered the sub-100 nm regime. For device with sub-100 nm L_G, classical scaling meets immense challenges due to some fundamental limits. Innovations on materials and device structures for MOSFET applications have become additional and more important drivers for CMOS development. Fig. 1.1 demonstrates a three dimensional (3D) schematic of a MOSFET with semiconductor on insulator substrate, showing some of the important engineering innovations/techniques which have been or will be used for performance improvement. Liner stressor technology which is to induce strain in the channel of a MOSFETs has been used to enhance carrier mobility and drive current. Novel dielectric material has been employed for effective oxide thickness and gate leakage current reduction. Raised source/drain (S/D) is an effective and widely adopted way to reduce device parasitic resistance. New

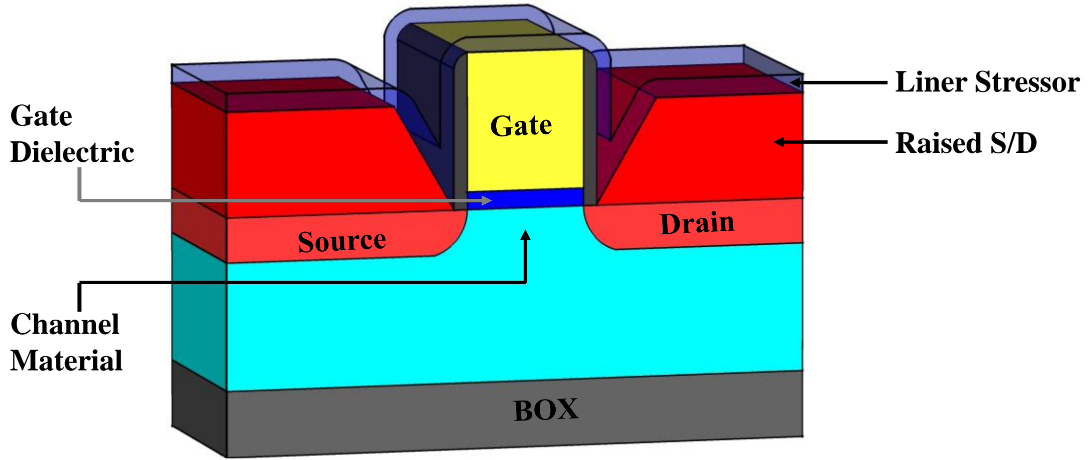


Fig. 1.1. 3D schematic of a MOSFET, showing liner stressor, gate dielectric, channel material, and raised S/D engineering for performance improvement of CMOS. BOX is barrier oxide of the semiconductor on insulator substrate.

materials with high carrier mobility, such as germanium, is expected to replace silicon (Si) as channel material for future CMOS applications.

1.1.1. CMOS Strain Engineering

One problem caused by geometric scaling of MOSFET is mobility degradation due to large vertical electrical field. In practical CMOS scaling, the supply voltage is not scaled down as rapidly as the other transistor parameters (L_G, W_G, and T_{OX}), increasing the vertical electrical field as the transistor size shrinks. Effective mobility could be represented by

$$\mu_{eff} = \mu_0 \left(\frac{E_{eff}}{E_0}\right)^{-1/3}, \quad (1\text{-}1)$$

where μ_0 and E_0 are empirical constants, and E_{eff} is the effective vertical electrical field [2]. From Equation 1-1, mobility degrades as electrical field increases. Larger vertical electrical field would result in enhanced surface scattering, which will reduce

carrier mobility. Fig. 1.2 shows that electron mobility degrades as CMOS technology progresses into more advanced technology nodes [3].

In addition, any increase of channel doping to have better short channel effect (SCE) also degrades carrier mobility, which is due to enhanced impurity scattering. The empirical relationship between carrier mobility and channel doping suggests

$$\mu = \mu_0 e^{-P_c/N} + \frac{\mu_{max}}{(N/C_r)^{\alpha}+1} - \frac{\mu_1}{(C_s/N)^{\beta}+1}, \tag{1-2}$$

where μ is the carrier mobility, μ_{max} is the highest carrier mobility in bulk semiconductor, P_c, μ_{max}, μ_1, μ_0, C_r, C_s, α, and β are the empirical parameters with positive values obtained by fitting the experimental results, and N is doping concentration [4]. Carrier mobility decreases as doping concentration increases.

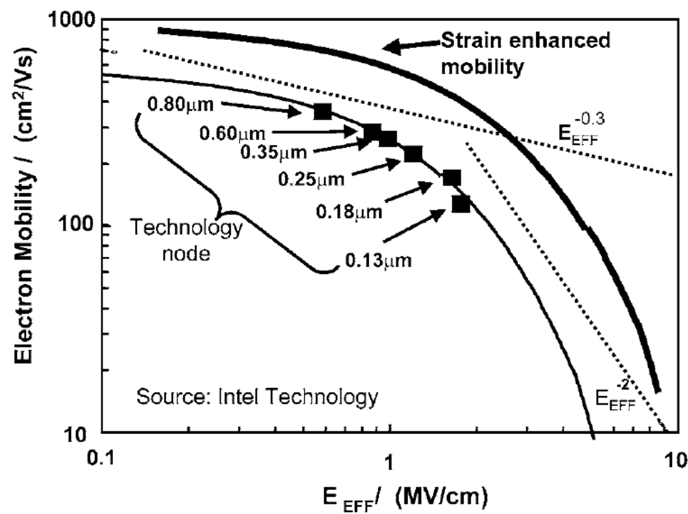
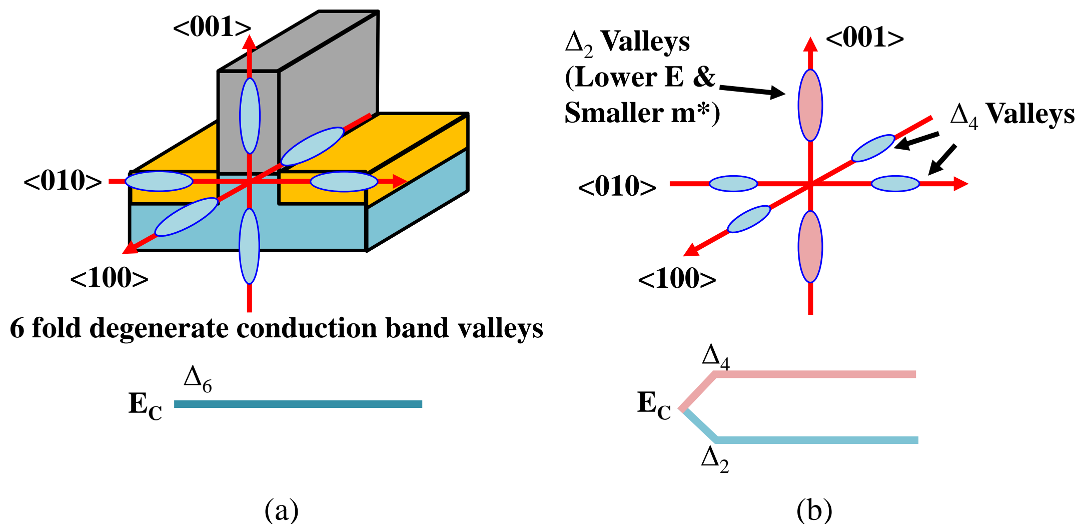


Fig. 1.2. Mobility versus technology scaling trend for Intel process technologies [3].



(a) (b)

Fig. 1.3. (a) 6 fold degenerate conduction band valleys of Si without strain; (b) Strain induces Δ_2 and Δ_4 splitting. Electrons tend to stay in Δ_2 valleys in which the in-plan effective transport mass is lower [5].

To compensate for the mobility loss due to CMOS geometric scaling, incorporation of mobility booster is needed for further advancement of CMOS beyond sub-100 nm technology nodes. Starting from 90-nm technology node in year 2002, strain engineering has been adopted by Intel and other companies as an additional performance booster to further extend the CMOS roadmap to sub-100 nm regime [3, 6-14]. Application of strain to the Si channel could significantly improve carrier mobility, which directly results in enhancement of transistor drive current. It is believed that strain engineering will still be used as one of the major performance boosters for next a few technology nodes.

Strain could enhance both electron and hole mobilities. Two types of mechanical strain were considered for integration into CMOS technology: biaxial and uniaxial. The mechanism of the electron mobility enhancement due to biaxial and uniaxial strain is the same: strain splits the six-fold [Fig. 2 (a)] degenerate conduction band valleys into two groups. One group is the lower energy two-fold Δ_2 valleys with

lower in-plan effective transport mass, and the other one is the higher energy four-fold Δ_4 valleys which are perpendicular with respect to Δ_2 valleys, as shown in Fig. 2 (b). Electrons tend to populate into the Δ_2 valleys, resulting in smaller transport mass and higher electron mobility.

For hole mobility enhancement, biaxial and uniaxial strain could lead to different valence band shifts and warping, as shown in Fig. 1.4, resulting in different mechanisms in enhancing the hole mobility. Low conductivity effective mass (in-plane) and high out-of-plane effective mass are mainly responsible for uniaxial strain induced hole mobility enhancement, while the reduction of intervalley scattering plays a more important role in enhancing hole mobility for the case of biaxial strain. Uniaxial strain could enhance carrier mobility even at a low stress level, while biaxial strain could only enhance mobility at a relatively large stress level [15, 16]. It has been demonstrated that uniaxial strain could provide significantly larger carrier mobility enhancement and lower threshold voltage shift, as compared with biaxial strain [6, 15, 16]. Therefore, uniaxial strain technology has been adopted by industry from 90-nm technology node and beyond [3, 12, 17].

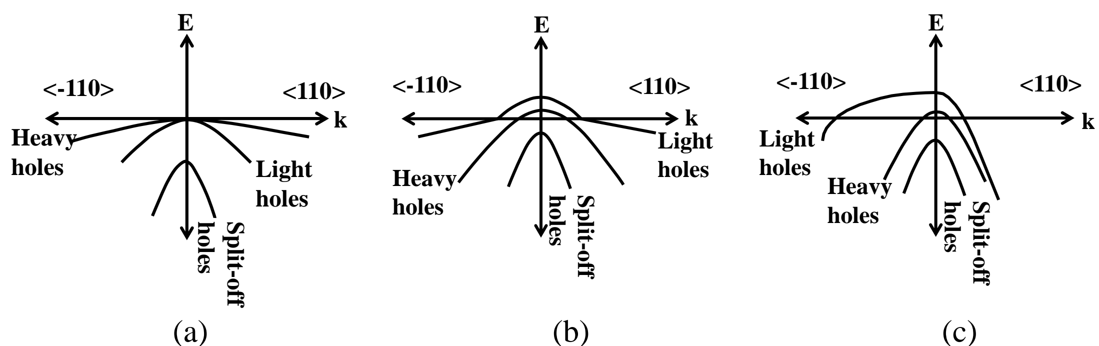


Fig. 1.4. Simplified valance band structure for longitudinal in-plane direction of (a) unstrained [18], (b) uniaxial strained Si [15], and (c) biaxial strained Si [15].

The carrier mobility change due to strain can simply be expressed as:

$$\frac{\Delta\mu}{\mu} \approx \left|\pi_{\|}\sigma_{\|} + \pi_{\perp}\sigma_{\perp}\right|, \quad (1\text{-}3)$$

where μ is the carrier mobility, $\Delta\mu$ is the strain induced mobility change, the subscripts $\|$ and $\perp$ refer to the directions parallel (longitudinal) and perpendicular (transverse) to the direction of the current flow in the MOSFETs, respectively, $\sigma_{\|}$ and $\sigma_{\perp}$ are the longitudinal and transverse stresses, respectively, $\pi_{\|}$ and $\pi_{\perp}$ are the piezoresistance coefficients for the longitudinal and transverse directions, respectively [3]. For uniaxial strain, the stress component parallel to the current flow direction is the primary stress component of interest. Basically, a larger strain would lead to a higher carrier mobility enhancement.

Several techniques to induce uniaxial strain in the channel for performance enhancement have been well studied, including silicon germanium (SiGe) or silicon carbon (SiC) source and drain (S/D) stressor and silicon nitride (SiN) liner stressor technologies. SiGe or SiC S/D stressor techniques induce strain due to the lattice mismatch between S/D and channel. SiN liner stressor or contact etch stop layer (CESL) technology makes use of the intrinsic stress in the SiN film to induce strain in the channel. SiN liner stressor has been demonstrated to be a cost-effective approach to induce strain in p-FETs for drive current improvement [3, 6-14]. The commonly reported compressive stress in SiN liner so far is in the range of 1~3.5 GPa [6, 8-11, 13].

Although strain engineering has provided enough performance booting since 90 nm technology node, the continuous scaling of device dimension and gate pitch poses new challenges to the conventional techniques or materials used for CMOS

strain engineering, especially when the technology node reaches 22 nm and beyond. The smaller space available between two transistor gates decreases the "volume/quantity" for strain materials, such as SiN liner stressor or SiGe S/D. This will in turn decreases the stress coupling into channel, results in smaller channel strain and reduced performance enhancement [19]. Diamond-like carbon (DLC), which has much larger intrinsic stress, was explored to be used together with a SiO_2 adhesion layer as liner stressor to address the challenges faced by conventional SiN liner stressor technology. DLC could provide the same or even larger amount of channel strain with thinner liner thickness, as compared with SiN film [20-22]. Significant performance enhancement was observed from DLC strained p-FETs with different device structures, including planar FETs and FinFETs.

The existence of SiO_2 adhesion layer or "buffer" layer, however, could degrade the stress coupling, resulting in smaller channel strain and degraded stress coupling. It was reported that the performance enhancements due to the same SiN liner stressor appears to decrease when a HfO_2 "buffer" layer is inserted between the SiN liner and underlying transistor [23], indicating the "buffer" degrade the stress in the channel. There is a strong need to remove this SiO_2 adhesion/buffer layer for better stress coupling, further developing the DLC liner stressor technology.

1.1.2. Negative Bias Temperature Instability of Strained p-FETs

With the use of thinner gate oxide and new gate dielectric materials in advanced CMOS technology nodes, new reliability issues emerge, among which the negative bias temperature instability (NBTI) is considered as one of the most significant reliability concerns [24-28]. NBTI occurs in p-FETs in which the gates are electrically stressed with a negative voltage, resulting in transistor parameter

degradation. NBTI becomes more severe at elevated temperatures, as its name suggests. The transistor parametric manifestation of NBTI includes threshold voltage V_{TH} shift or increase, as well as degradation of linear drain current I_{DLin}, saturation drain current I_{DSat}, and transconductance G_M.

One of the most important manifestations of NBTI is threshold voltage shift. The threshold voltage of a MOSFET is normally expressed by the equation below, considering the interface traps,

$$V_{TH} = \Phi_{MS} + \psi_S + \frac{Q_{DEP}}{C_{OX}} - \frac{Q_{OX}}{C_{OX}} - \frac{Q_{IT}}{C_{OX}}, \tag{1-4}$$

where Φ_{MS} is the metal-semiconductor work function, ψ_S is the surface potential, Q_{DEP} is the depletion charge, Q_{OX} is the fixed oxide charge, Q_{IT} is the interface trap, and C_{OX} is the gate oxide capacitance. Any change in the charge level at the SiO_2/Si interface would result in threshold voltage shift. Generation of interface traps at SiO_2/Si interface is believed to be one of the reasons causing NBTI [24, 27]. Hole trapping in pre-existing defects could be anther contributing factor which changes the charge level at the interface [27, 29-32]. Beside changing V_{TH}, interface generation could also result in additional surface scattering, causing hole mobility to decrease. Threshold voltage increase and mobility degradation lead to decrease of drain current I_D and transconductance G_M, as suggested by the following two equations

$$I_D = \frac{W_G}{2L_G} \mu_{eff} C_{OX} (V_{GS} - V_{TH})^2, \tag{1-5}$$

$$G_M = \frac{W_G}{L_G} \mu_{eff} C_{OX} (V_{GS} - V_{TH}), \tag{1-6}$$

where W_G is the gate width, L_G is the gate length, and μ_{eff} is the effective carrier mobility [24]. The intrinsic delay of a transistor can simply be expressed as,

$$\tau = \frac{C_{OX}}{I_D} V_{DD}, \quad (1\text{-}7)$$

where V_{DD} is the supply voltage. The increase of V_{TH} and decrease of drain current will unavoidably lead to degradation of the intrinsic delay of a transistor and the performance of the whole circuit.

When new strain engineering techniques are considered for possible integration in manufacturing, their impact on device reliability should be investigated. Although there are some publications claiming that strain has negligible effects on NBTI performance of p-FETs [33-35], most publications in the literature demonstrated that strained p-FETs have more severe NBTI degradation, as compared with unstrained control p-FETs [23, 36-44]. Various reasons were proposed for the degraded NBTI performance of strained p-FETs. As we are developing the new DLC strain engineering technology, examination on the NBTI reliability of strained p-FETs with DLC liners stressor should be performed, in addition to the investigation on device performance enhancement due to strain. Device reliability and performance enhancement must be carefully considered when designing transistors with strain.

1.1.3. Germanium as an Alternative Channel Material for Future CMOS Applications

1.1.3.1. Why Ge?

Further development of the strain engineering is more of a near-term solution for the challenges faced by CMOS technology. More fundamental problems need to

be solved when the CMOS road map further advances to deep-100 nm regime, especially when gate length is scaled to 10 nm or smaller and the device dimension approaches atomic level. When MOSFET is scaled to deep sub-100 nm, carrier transport in the extremely scaled device is quasi-ballistic. The drive current of a device operating in quasi-ballistic regime is limited by the thermal injection velocity [45, 46], instead of the saturation velocity which determines the performance of a long channel device. Saturation current of a short channel device can be expressed as

$$I_{DSAT} = C_{OX} W_G \upsilon_{inj} \left(\frac{1 - r_c}{1 + r_c}\right)(V_{GS} - V_{TH}), \tag{1-8}$$

where C_{OX} is the gate oxide capacitance, W_G is the gate width, r_c is the backscattering coefficient which is a measure of the number of carriers that backscatter to the source, V_{GS} is the gate voltage, and V_{TH} is the threshold voltage, and υ_{inj} is the thermal injection velocity. For extremely scaled devices operating in full ballistic regime, r_c is equal to zero. The υ_{inj} was experimentally found to be proportional to low field mobility [47, 48]. Higher low field mobility leads to higher injection velocity which in turn results in higher drive current. Therefore, high mobility channel material is desirable to further improve the device performance. Ultimately, exploring new channel material with high carrier mobility to replace Si is deemed as a long term solution to continue Moore's law to sub-10 nm regime.

Germanium (Ge) is one of the most promising channel materials to replace Si in future low power and high performance CMOS applications, as it has very high carrier mobilities, especially hole mobility. Table 1.1 compares material characteristics of potential channel materials for future CMOS applications, showing

Table 1.1. Material characteristics of potential channel materials for future CMOS applications [49].

	Si	Ge	InP	GaAs	InAs	InSb
Band gap (eV)	1.11	0.67	1.34	1.43	0.354	0.17
Breakdown field (MV/cm)	0.3	0.1	0.5	0.06	0.04	0.001
Electron mobility ($cm^2/V\cdot s$)	1350	3900	5400	8500	40000	77000
Hole mobility ($cm^2/V\cdot s$)	480	1900	200	400	500	850
Thermal conductivity (W/cm·K)	1.3	0.58	0.68	0.55	0.27	0.18
Lattice constant (Å)	5.43	5.66	5.87	5.65	6.06	6.48

that Ge has very high electron mobility and the highest hole mobility among all group IV and III-V semiconductor materials.

1.1.3.2. Gate Stack for Ge MOSFETs

Achieving good high-κ/Ge gate stack with low interface charge density D_{it} and relatively low equivalent oxide thickness (EOT) is essential to fabricate high performance Ge MOSFETs. Direct deposition of high-κ dielectric on Ge without any intentionally formed interfacial layer normally results in high gate leakage current as well as high hysteresis [50], due to high interface defect density [51]. Ge surface passivation with ultra-thin (a few monolayer) Si or SiO_2/Si, Ge dioxide (GeO_2), Ge oxynitride (GeON), and surface treatments using chemistries, such as ammonium sulphide ($(NH_4)_2S$, phosphine PH_3, have been investigated on MOS capacitors and transistors. High performance Ge planar p-FETs fabricated using various passivation techniques were reported in the literature. For example, R. Zhang *et. al.* demonstrated

GeO_2 passivated long channel Ge p-FETs with low field mobility up to 526 $cm^2/V\cdot s$ [52]. J. Mitard *et. al.* of IMEC reported high performance sub-100 nm Ge p-FETs with high on-state current and hole mobility of more than 200 $cm^2/V\cdot s$ [53]. R. Pillarisetty *et. al.* of Intel demonstrated short channel strained Ge p-FETs with hole mobility of ~770 $cm^2/V\cdot s$ at an inversion hole density of 5×10^{12} cm^{-2} (three times higher than the state of the art strained Si devices) [54]. Si passivation was used in the last two studies.

Comparing with Ge p-FETs, the gate stack of Ge n-FETs is not well developed yet. The larger interface charge density D_{IT} near the conduction band edge poses great challenges to the fabrication of high performance Ge n-FETs. The drive current achieve by the Ge n-FETs is lower than those reported by n-FETs with other high mobility channel materials such as InGaAs [55-57], which is partially due to the poor interface quality. Novel surface passivation technique reported recently, such as high pressure oxidation of Ge [58] and plasma post oxidation [59], could possibly enhance the performance of Ge n-FETs.

1.1.3.3. Other Challenges of Ge Devices

Besides gate stack engineering, there are some other process challenges faced by Ge devices, including doping of S/D and reduction of leakage current.

P-type doping of Ge is not an issue, as active boron (B) concentration by B ion implantation with preamorphization of Ge and anneal could reach up to 5.7×10^{20} cm^{-3} which is good enough for S/D applications. N-type doping for Ge, on the other hand, faces great challenges, as normal n-type dopants (such as arsenic and phosphorus) can only reach active doping concentrations of 2×10^{19} cm^{-3} to 5×10^{19} cm^{-3} [60]. Solid phase diffusion, gas phase doping [55], spin-on dopant [61], *in-situ* n^+ doping [62],

and ion co-implantation [63] (such as antimony and phosphorus together) were proposed recently to achieve high active n-type concentration in Ge.

Another challenge of Ge devices is the high leakage current, which is for both p-FETs and n-FETs. The leakage current in Ge device is contributed by Shockley-Read-Hall recombination (SRH), trap assisted tunneling (TAT), and band to band tunneling (BTBT) [64], among which BTBT contribute a significant portion of the leakage current. The large BTBT is due to the small bandgap of Ge. The solution suggested to reduce the leakage current is to use lower supply voltage for the devices [64].

1.1.3.4. Germanium Multiple-Gate Field-Effect Transistors

As the dimensions of MOSFETs are continuously scaled down, the control of the channel potential and current flow by the gate electrode is reduced due to the close proximity between the source and the drain. Although reducing junction depth, thinning gate oxide thickness, and increasing channel doping concentration could reduce SCE, practical limits on tuning these parameters makes it almost impossible to scale the MOSFETs to sub-20 nm using the conventional bulk planar transistor structure. Multiple-gate device structures were proposed and demonstrated to help improve gate electrostatic control in ultra-scaled MOSFETs, as the additional gates provide better control of channel potential [65-67]. Starting from 22 nm technology node, Si channel multiple-gate field-effect transistors (MuGFETs) or FinFETs have been used for high volume CMOS production.

As discussed earlier in Sub-section 1.1.3.1, Ge is a promising alternative channel material for future CMOS application. High mobility Ge channel FET with multiple-gate structures could be adopted to achieve high drive current and good short

channel control at sub-20 nm technology nodes. Besides forming high quality gate stack, a few other technical challenges would need to be addressed specially for Ge MuGFET fabrication.

For Ge MuGFET or FinFET fabrication, two substrate options are available, namely Ge on bulk Si substrate and Ge on insulator (GeOI) substrate. The earlier option is probably cheaper, as compare with the latter, due to simpler substrate manufacture processes. However, few bulk Ge MuGFETs were reported in the literature so far due to a few technical challenges, such as forming high quality Ge fins on Ge on Si substrate. G. Wang *et. al.* of IMEC demonstrated Ge growth in narrow shallow trench isolation (STI) on Si substrate recently [68]. Laser anneal was shown by them to improve the Ge crystalline quality. The Ge fins obtained by such technique could potentially be used for bulk Ge FinFET fabrications, although there is no device demonstration yet. Most publications on Ge MuGFETs are fabricated on germanium on insulator substrates, as the process to fabricate devices on GeOI substrate is simpler. In addition, employment of GeOI substrate also eliminates any drain to body leakage current. GeOI substrate is a good vehicle to test various process modules.

Another challenge to fabricate high performance MuGFETs is to control S/D series resistance, as the employment of narrow fins for short channel control could result in large S/D series resistance. Different approaches were used to reduce the series resistance for Si FinFETs, including Schottky barrier (SB) metal S/D and epitaxially grown raised S/D. The former is to make use of the low resistance of metal [69], while the latter is to increase the contact area of S/D regions [70]. Neither

of these two techniques was realized on Ge MuGFETs on GeOI substrate yet at the time when this thesis work was written.

P-channel Ge MuGFETs or nanowire FETs were fabricated by a few research groups by both bottom-up [71-73] and top-down [74-80] approaches in the past a few years. However, compared with the very well established and highly manufacturable Si FinFET/MuGFET fabrication process, the process development of Ge MuGFETs requires more efforts. There is a strong need to further advance the state of the art Ge MuGFET technology.

1.2 Thesis Outline and Original Contributions

Aiming to solve some of the near term and long term challenges faced by CMOS scaling, this thesis work develops several exploratory technology options to engineering different components of transistors, and the main technical contents discussed are documented in four chapters, *i.e.* Chapter 2 to 5. The technical topic covered in each chapter is illustrated in Fig. 1.5.

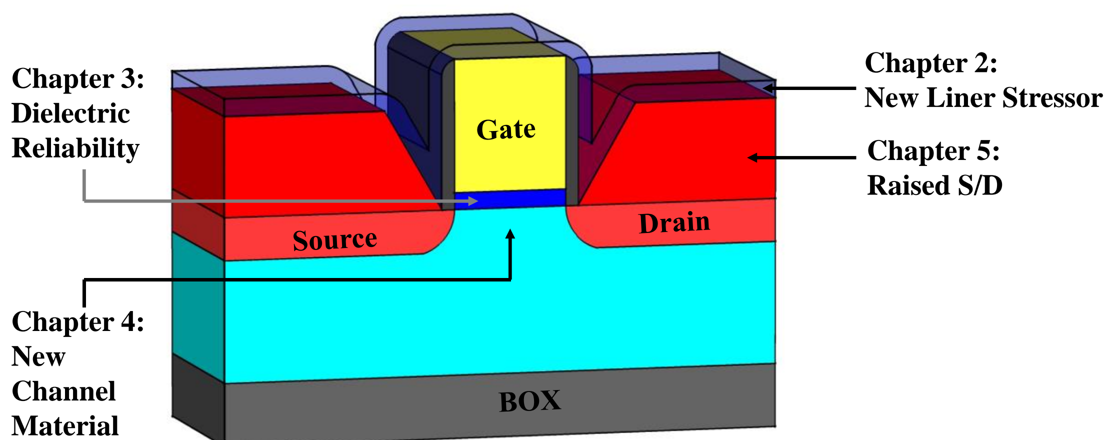


Fig. 1.5. Technical aspects covered in this thesis work.

In Chapter 2 of this thesis, new development work for the DLC liner stressor technology is performed. Taurus process simulation is conducted first to investigate the effect of the SiO_2 layer used in previous DLC technology. Raman spectroscopy and electrical characterization of DLC films developed under different process conditions is performed in order to get DLC film with high intrinsic stress and high electrical resistivity for direct integration on p-FETs. Direct deposition of the DLC liner stressor is realized for the first time on short channel planar p-FETs and more advanced Si nanowire p-FETs in this Chapter. Electrical characterization is performed to investigate the performance enhancement due to DLC liner stressor. DLC thickness effect on performance enhancement is discussed.

In Chapter 3, gate dielectric reliability, *i.e.* NBTI, of strained p-FETs with DLC liner stressor is investigated using an improved ultra fast measurement method (UFM) for the first time. Detailed UFM measurement setup is discussed. NBTI data collected by conventional DC measurement and UFM technique are compared. NBTI behaviors of p-FETs with different levels of channel strain are investigated. Recovery behavior of drain current and transconductance, as well as gate length dependence of NBTI, are also discussed. Device lifetime is projected.

In Chapter 4, we move on from strain engineering of Si devices to explore more advanced devices with Ge as channel material for possible future CMOS applications. High performance omega-gate (Ω-gate) Ge MuGFETs with low temperature disilane (Si_2H_6) passivated channel, high-κ/metal gate stack, and self-aligned metallic SB nickel germanide (NiGe) S/D are fabricated on GeOI substrate. Detailed Si CMOS compatible fabrication process is discussed in this Chapter. The effects of fin/channel doping and backside interface charge of GeOI substrate on the

electrical characteristics of Ge MuGFETs are investigated. Low temperature characterization of Ge MuGFETs is performed. Device scaling behaviour is also reported. The device performance achieved in this work is compared with the data in the literature.

Performance of Ge MuGFETs with raised S/D (RSD) is explored in Chapter 5. Process optimization and material characterization for selective epitaxial growth of boron doped Ge (Ge:B) RSD on patterned GeOI substrates is first performed. Integration of RSD into Ge MuGFETs is then demonstrated. Electrical results of Ge MuGFETs with RSD are documented in this Chapter. First NBTI investigation of Ge MuGFETs with RSD is also conducted.

The thesis ends with an overall conclusion and possible future research directions in Chapter 6.

Chapter 2

A New Diamond-like Carbon (DLC) Ultra-High Stress Liner Technology for Direct Deposition on P-Channel Field-Effect Transistors

2.1. Background

Liner stressor or contact etch stop layer (CESL) technology is an effective engineering technique to induce strain in p-FETs for drive current improvement [3, 6-14, 81]. Silicon Nitride (SiN) and Diamond-Like Carbon (DLC) stress liners were demonstrated for mobility enhancement of metal-oxide-semiconductor field-effect transistors (MOSFETs) in previous studies [3, 6-14, 20-22, 81-83]. SiN is the most commonly used liner stressor reported in the literature, and has been employed in CMOS production for transistor performance enhancement since the 90-nm technology node [3, 81]. The commonly reported compressive stress in SiN liner to enhance p-FETs so far is in the range of 1 to 3.5 GPa [6, 8-11, 13, 14].

Due to the aggressive gate pitch reduction (illustrated in Fig. 2.1) in CMOS scaling, the effective channel stress induced by the current SiN stress liner decreases [8, 20], making the SiN liner technology less effective in boosting device performance. Therefore, there is a strong need to develop a new liner stressor with higher intrinsic stress to maintain a certain level of channel stress for future CMOS applications.

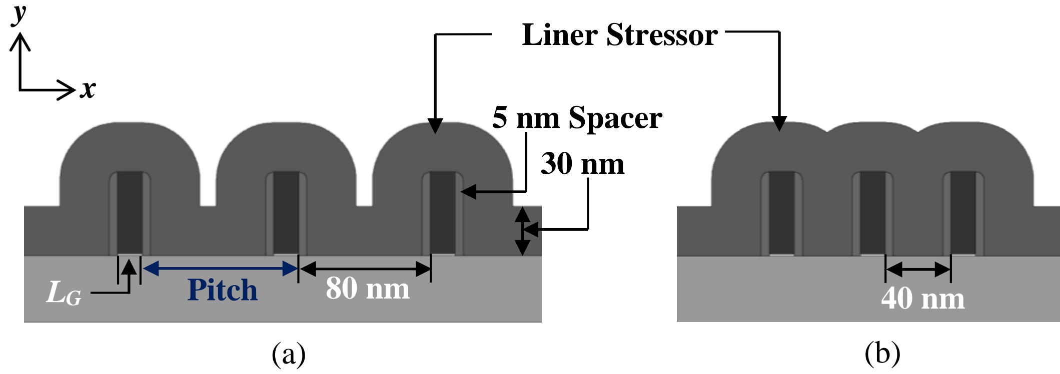


Fig. 2.1. Stacked MOSFETs with gate spacing L_{GSP} of (a) 80 nm, and (b) 40 nm, demonstrating gate spacing (or pitch, pitch = gate spacing + gate length) scaling. Gate length L_G, spacer width W_{SP}, and SiN liner thickness T_{SiN} are kept the same as 15 nm, 5 nm, and 30 nm, when scaling the pitch.

DLC liner stressor technology was first developed by Tan *et. al.* [20] in 2007 to address the scaling challenges faced by the SiN liner technology. DLC is well known for its high hardness, resistivity, wear resistance, and chemical inertness. It has been widely used in hard disk industry as protective overcoats [84-87]. Depending on the deposition condition, DLC film could have a much higher intrinsic compressive stress (~5 GPa to ~7 GPa) than the conventional SiN (≤ 3.5 GPa). DLC liner can induce high levels of stress in transistor channels. DLC has been demonstrated as a high-stress liner on Si p-channel MOSFETs with various device structures, including planar, SOI, and multi-gate MOSFETs [20, 21, 82, 83]. DLC has also been combined with other stressors such as silicon germanium (SiGe) source and drain (S/D) stressors [22].

However, at the initial stage of development for the DLC liner technology, a silicon dioxide (SiO_2) liner was inserted between DLC liner and the underlying p-FET for possible improvement of adhesion [83], as shown by the transmission electron microscopy (TEM) image in Fig. 2.2. The SiO_2 liner increases the total thickness of

the liner layer, but hardly contributes any stress to the channel region. This compromises the scalability and process simplicity of DLC technology, and may also reduce the channel stress induced by the DLC liner, especially when the SiO_2 layer is too thick.

In this work, the first demonstration of the direct deposition of DLC high stress liner on advanced nano-scale p-FETs, including nanowire p-FETs, for performance enhancement is reported. Table 2.**1** highlights reports of SiN and DLC liner stressors in the literature and the important contributions of this thesis work. Stress simulation is conducted to study scaling behaviour of different liner stressors, and the results demonstrate that there is a need to eliminate the SiO_2 liner for increased stress effects. Process development of direct DLC deposition technique will be discussed in this Chapter. The performance enhancement brought by the improved DLC liner technology for planar Si p-FETs and advanced nanowire p-FETs will be investigated and reported.

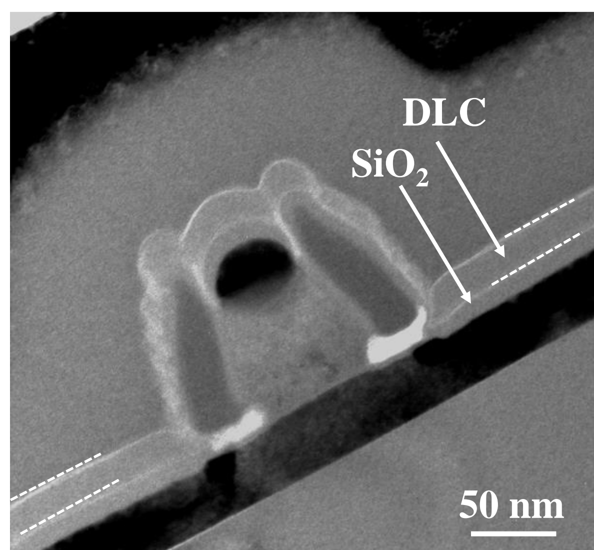


Fig. 2.2. TEM image of a SOI p-FET with SiO_2 liner + DLC stress liner, taken from previous work [83]. A SiO_2 layer was used between the transistor and DLC film for possible adhesion improvement.

Table 2.1. Comparison between typical SiN and DLC works in the literature and the current work.

Work	Liner Material	Stress (GPa)	Device Structure	Organization
Ref. [6]	SiN	-2.0	Planar p-FETs	Fujitsu
Ref. [9]	SiN	-3.0	Planar p-FETs with SiGe S/D	AMD and IBM
Ref. [10]	SiN	-2.0	Planar p-FETs with SiGe S/D	SONY
Ref. [11]	SiN	-1.4	Double-Gate FinFETs	University of Florida and SEMATECH
Ref. [13]	SiN	-3.5	SOI p-FETs	IBM and GLOBALFOUNDRIES
Ref. [14]	SiN	-2.4	Planar p-FETs with SiGe S/D	Applied Materials and IMEC
Ref. [20]	DLC/SiO_2	-6.5	SOI p-FETs	NUS
Ref. [21]	DLC/SiO_2	-6.0	Tri-gate FinFETs	NUS
Ref. [22]	DLC/SiO_2	-5.0	Planar p-FETs with SiGe S/D	NUS
This work	DLC	-5.0	Planar p-FETs (*First Demonstration of p-FETs with directly Deposited DLC Liner*)	NUS
This work	DLC	-7.0	Nanowire p-FETs with DSS S/D (*World First Nanowire p-FETs with DLC Liner Stressor*)	NUS

2.2. Simulation of Nanoscale FETs with Different Liner Stressors

In this Section, stress simulations were conducted using Taurus TSUPREM-4 to study scaling behaviors of different stress liners. The absence or presence of a SiO_2

layer below the high stress liner layer is investigated. Instead of single MOSFET structure, stacked devices shown in Fig. 2.1 are used in the simulation study. The stacked device structure is closer to device layout designs typically found in logic circuits. The stress component in the current flow direction, i.e. along x direction, is the stress component of interest, because this stress component is mainly responsible for hole mobility and drain current enhancement for transistors with stress liner. The stress along the current flow direction here after will be referred to as "S_{xx}". As the stress induced by liner stressor could approximately be considered as uniaxial stress, the stress or strain mentioned hereafter in this thesis is along the longitudinal direction unless otherwise stated.

For stress simulation, the Si bulk region of the device was assumed to be rigid body. The anisotropic elastic model was used for the Si substrate. All ambient interfaces are considered as free surfaces, while the reflective surfaces at the sides of the domain are considered as fixed. There is no slippage at an interface between materials [88].

Fig. 2.1 shows stacked MOSFET structure with a gate spacing L_{GSP} of (a) 80 nm, and (b) 40 nm, illustrating reduction of L_{GSP}. Gate pitch L_{PITCH} is defined as the sum of L_{GSP} and gate length L_G. L_G and spacer width W_{SP}, are kept the same as 15 nm and 5 nm, respectively, when scaling the pitch. For a W_{SP} of 5 nm and a liner stressor thickness T_{Liner} of 30 nm, the liner starts to completely fill the space between the gates when L_{GSP} is scaled down to 70 nm and below.

Fig. 2.3 shows simulated average channel stress along the channel direction induced by 20 nm SiN (gray circles), 30 nm SiN (open squares), and 20 nm DLC (red triangles) versus gate spacing L_{GSP}. The intrinsic stress of SiN is assumed to be 3 GPa

which is a common stress value reported for SiN liner. The intrinsic stress of DLC is 6 GPa which can be easily achieved for DLC films. The Young's Modulus and Poisson Ratio of DLC were assumed to be 760 GPa and 0.20, respectively [89]. The Young's Modulus and Poisson Ratio of SiN were assumed to be 192 GPa and 0.30, respectively [88]. The stress shown in Fig. 2.3 is the average of stress values taken 3 nm below top Si surface along the gate (15 nm) of the transistor in the middle of the MOSFET stack in Fig. 2.1. For SiN liners with the thicknesses of 20 nm and 30 nm, it can be clearly observed that channel stress starts to decrease when the gate space is completely filled by the stress liner. The advantage of a thicker SiN liner starts to vanish once the gate space is completely filled, and the channel stress becomes smaller as the gate pitch further reduces. Therefore, a new liner stressor with higher intrinsic stress which is capable of maintaining or even scaling up the compressive stress in the Si channel while scaling down L_{GSP} is desirable.

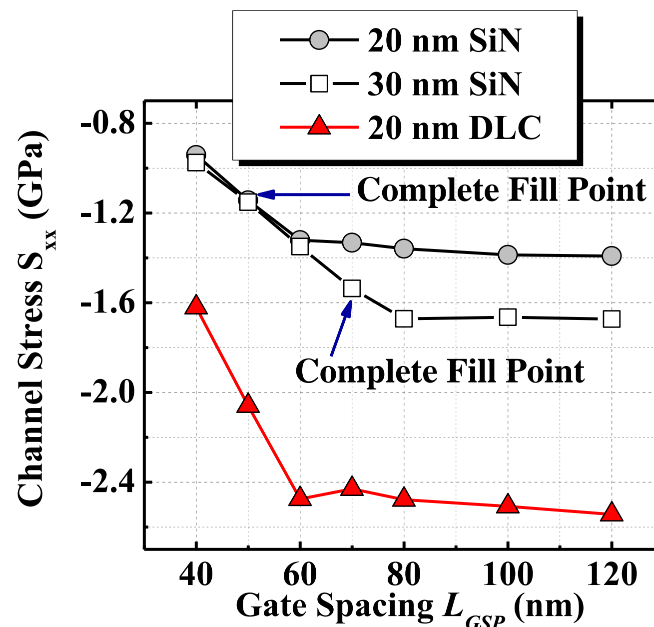


Fig. 2.3. Simulated average channel stress (S_{xx}) caused by 20 nm SiN (grey circles), 30 nm SiN (open squares), and 20 nm DLC (red triangles) for different gate spacing. The intrinsic stresses for SiN and DLC liner stressors are 3 GPa and 6 GPa, respectively.

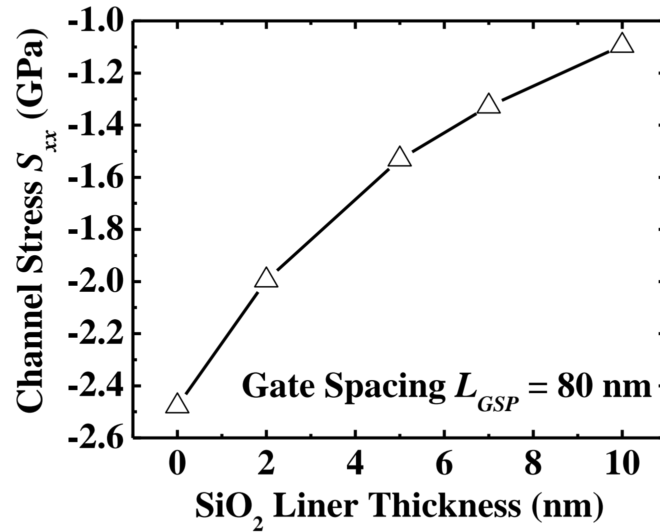


Fig. 2.4. Average channel stress for 20 nm-DLC strained devices with different SiO_2 liner thicknesses. Channel stress decreases as SiO_2 liner thickness increases.

It could be observed from Fig. 2.3 that a thinner DLC liner of 20 nm can achieve higher channel stress even than a thicker SiN of 30 nm does. DLC liner stressor with 6 GPa stress could help maintain large channel stress even the gate space is fully filled by the liner, showing that DLC has better scalability than SiN and could be a good strain engineering candidate for future technology nodes where L_{GSP} and L_{PITCH} will be extremely small.

Next, the effect of SiO_2 liner thickness is examined by simulation. Fig. 2.4 shows the average channel stress for devices with 20 nm DLC and L_{GSP} of 80 nm, but different SiO_2 liner thicknesses. The average channel stress induced by a 20 nm DLC liner decreases as the SiO_2 liner thickness increases. This is expected as a thicker SiO_2 moves the DLC liner further away from channel and reduces the mechanical stress coupling. The simulation results in the current work are consistent with experimental results in Ref. [23] by C.-S. Lu *et. al.* The performance enhancements due to the same SiN stress liner appears to decrease if a HfO_2 “buffer” layer is

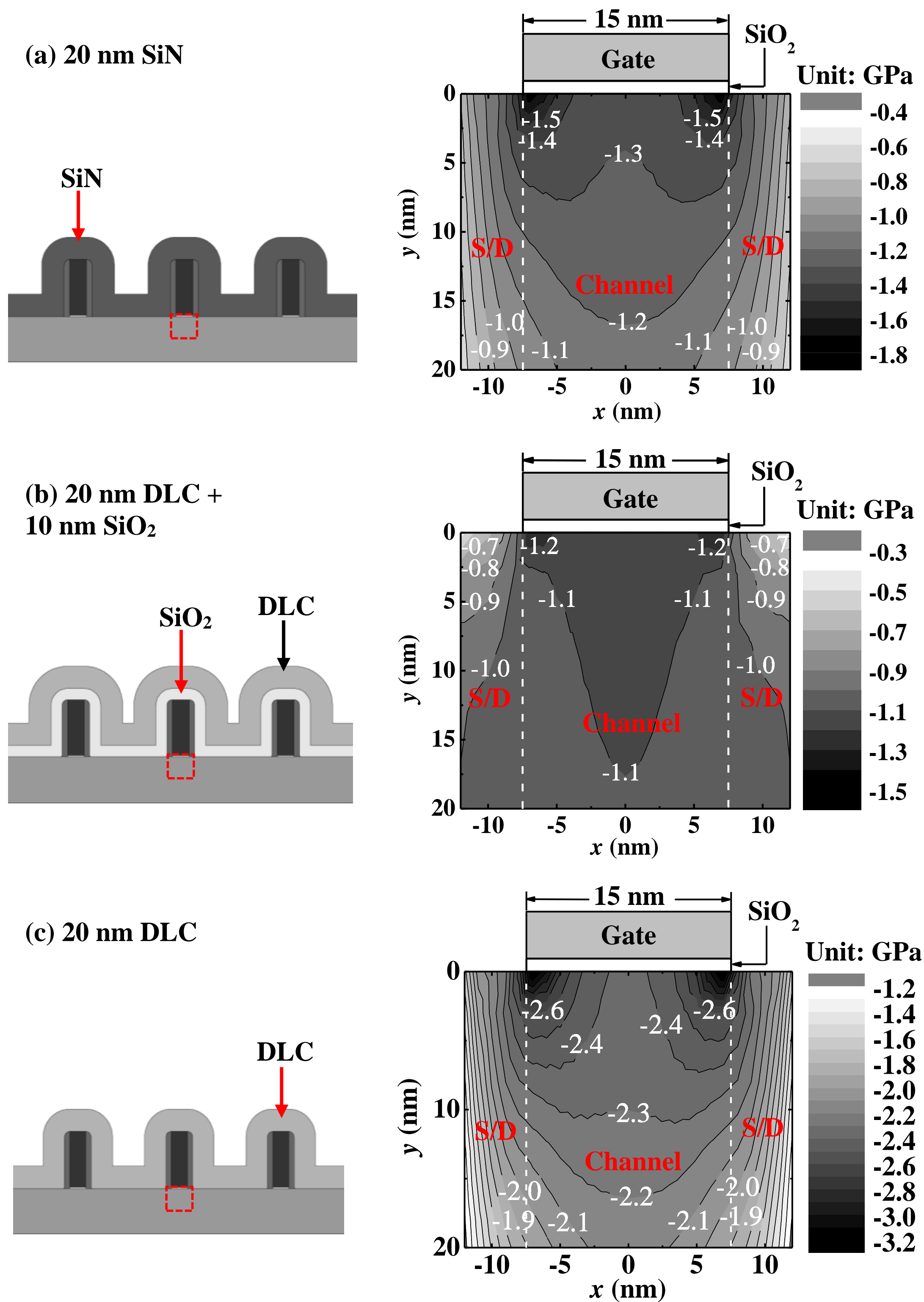


Fig. 2.5. Simulated 2D S_{xx} stress profiles of devices with (a) 20 nm SiN, (b) 20 nm DLC + 10 nm SiO_2, and (c) 20 nm DLC. L_{GSP} is 80 nm. The rectangles on the left of each figure indicate the location where the stresses are extracted.

inserted between the SiN liner and underlying transistor [23], indicating the "buffer" degrades the stress in the channel.

Fig. 2.5 shows two dimensional (2D) S_{xx} profiles of three transistors with (a) 20 nm SiN, (b) 20 nm DLC + 10 nm SiO_2, and (c) 20 nm DLC. The transistor with only 20 nm DLC has the largest channel stress among the three transistor structures. The one with 20 nm DLC + 10 nm SiO_2 has the smallest stress, even lower than that with SiN liner, despite DLC having a much larger intrinsic stress as compared with

SiN liner. From Fig. 2.4 and Fig. 2.5, it can be concluded that the 10 nm SiO_2 layer reduces the channel stress induced by the same DLC liner stressor, and the existence of SiO_2 layer makes DLC technology less effective. Therefore, it is desirable to eliminate the SiO_2 liner to achieve the maximum channel stress for a given stress liner and better scalability. This is the motivation of this work.

2.3. Characterization of Diamond-Like Carbon

DLC characterization will be reported in this Section. The DLC films used in this work are deposited using a Filtered Cathodic Vacuum Arc (FCVA) system [86, 87, 90]. Carbon film deposited by FCVA system is amorphous carbon containing high sp^3 content. Fig. 2.6 shows a simplified schematic of a FCVA system. In the FCVA, the carbon ions are generated through vacuum arc discharge between the cathode (pure graphite source) and the anode. An electric-magnetic-field is generated along the torus duct. This tool design can effectively filter out unwanted macroparticles and neutral atoms, only allowing carbon plasma to go through the duct to the substrate [90]. The energies of carbon ions used for DLC deposition can affect the DLC film characteristics and can be adjusted by the substrate bias.

DLC deposition rates were first calibrated against different deposition conditions, such as currents and substrate biases. Fig. 2.7 (a) shows the dependence of deposition rate on arc current. The deposition rate was found to be highly dependent on the arc current. This is expected, as the arc current controls the carbon flux density generated at the source. The higher the arc current, the larger the carbon flux density. Fig. 2.7 (b) shows the effect of substrate bias on DLC deposition rate. The deposition rate has little dependence on the substrate bias, which is consistent with data reported in the literature [86]. This is because that the substrate bias hardly changes the carbon flux density and only alters the energies of incoming carbon ions.

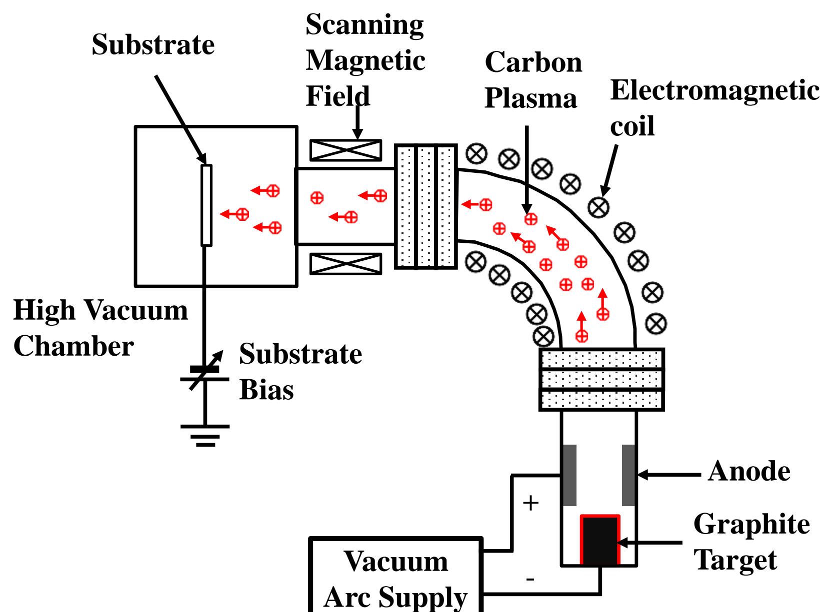


Fig. 2.6. Schematic of a FCVA system.

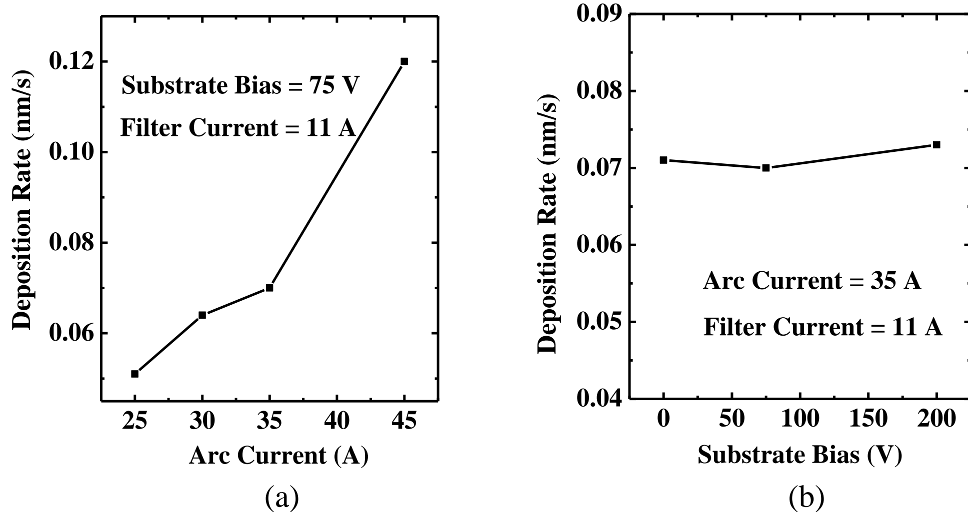


Fig. 2.7. Deposition rate of FCVA machine is plotted against (a) arc current and (b) substrate bias.

In order to directly deposit DLC film onto Si transistors, highly insulating DLC film is needed to avoid any possible leakage path in DLC film. Conductive DLC film leads to gate to source/drain (S/D) leakage, as the film covers gate and S/D at the same time. The substrate bias during DLC deposition changes the carbon ion energy and has strong impact on the properties of DLC deposited by FCVA system, such as sp^3 content, and stress, etc. In this work, DLC films were deposited on bulk Si substrates using FCVA system at different substrate biases to investigate the impact of the substrate bias on DLC characteristics. The thickness of the films is ~25 to ~30 nm. The DLC films were characterized using electrical measurement and ultraviolet UV Raman Spectroscopy at a wavelength of 325 nm.

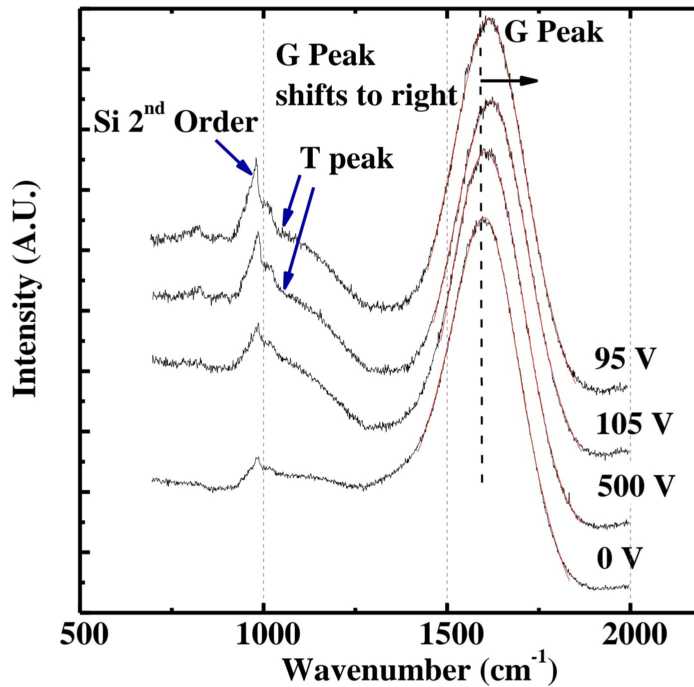


Fig. 2.8. UV (325 nm) excited Raman spectra of DLC films formed using different substrate biases. Referring to curves from bottom to top, the G peak position shifts to right, indicating an increase in sp^3 content.

A higher sp^3 content in DLC generally gives a more insulating film (lower conductivity) and higher intrinsic stress. DLC films with high sp^3 content show two peaks in their UV Raman spectra, a very weak peak at ~1060 cm^{-1} (referred to as "T" peak) [91], and a more visible one at ~1600 cm^{-1} (referred to as "G" peak) (Fig. 2.8), having intensities I_{TP} and I_{GP}, respectively. The G peak is due to bond stretching of sp^2 atoms, while the T peak, which is only visible in UV Raman spectra, is due to the C-C sp^3 vibrations [91]. The peak observed at ~980 cm^{-1} in Fig. 2.8 is due to the second order phonon scattering from the Si substrate.

It has been empirically demonstrated that sp^3 content in DLC films is related to the position of G peak, as well as I_{TP}/I_{GP} [some publications used $I_{TP}/(I_{TP}+I_{GP})$] . A

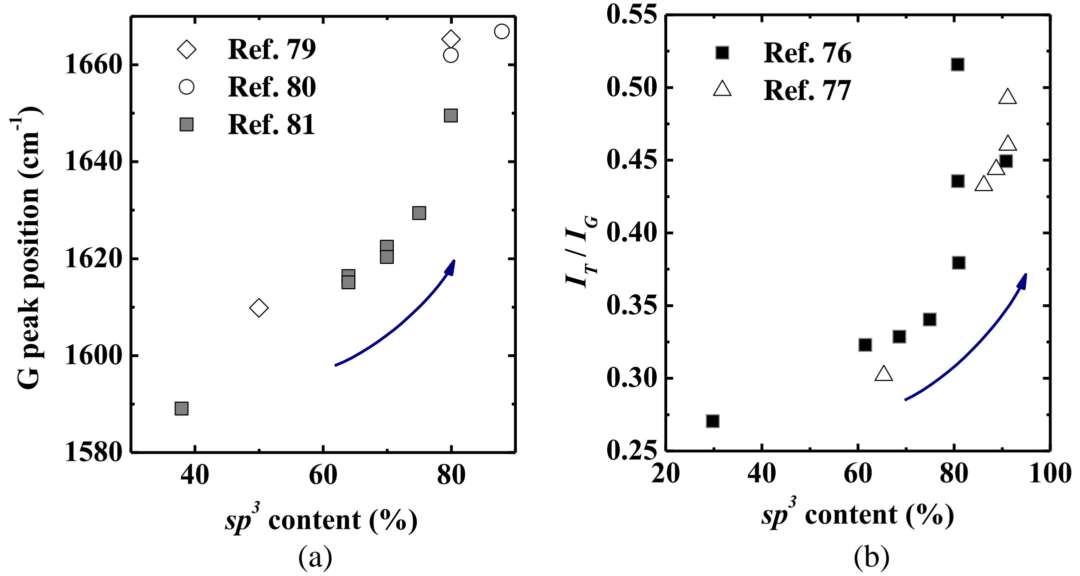


Fig. 2.9. (a) G peak position and (b) I_{TP}/I_{GP} of the ultraviolet Raman microscopy as a function of sp^3. Fig. 2.9 (a) is extracted from Ref. [92], [93-95], and Fig. 2.9 (b) is extracted from Ref. [91, 92].

G peak position further to the right and a higher I_{TP}/I_{GP} generally leads to higher sp^3 content [91, 92, 96], as indicated by Fig. 2.9 (a) and (b) extracted from [91, 92], [93-95].

Fig. 2.10 (a) shows the G peak position versus substrate bias plots obtained in this work. It is observed that the substrate bias V_{sub} of 95 V has the right-most G peak position, possibly indicating the highest sp^3 content and resistance. Fig. 2.10 (b) shows I_{TP}/I_{GP} versus substrate bias, showing the substrate biases of 95 V and 105 V lead to very similar and the highest I_{TP}/I_{GP}. Based on the results in Fig. 2.10 (a) and (b), the substrate biases of 95 V and 105 V may lead to the highest sp^3 content in DLC. It must be pointed out that the T peak intensity may be contaminated by the large Si peak at ~980 cm^{-1}, so there may be some inaccuracy in the I_{TP}/I_{GP} ratios. Further analysis need to be performed to confirm the conclusion that a substrate bias V_{sub} of 95 V leads to the highest sp^3 content and highest resistance.

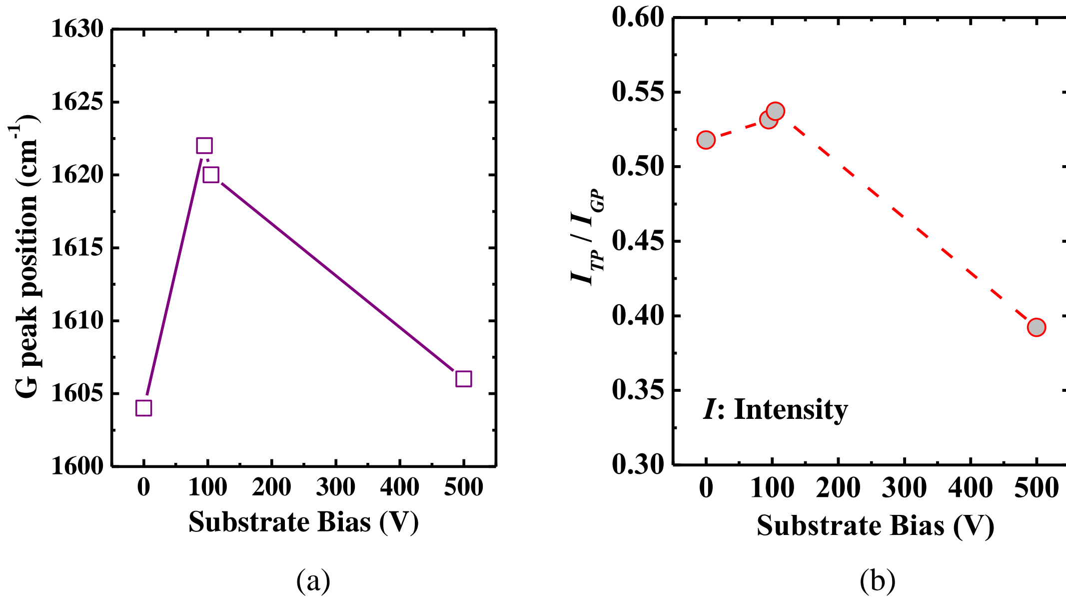


Fig. 2.10. (a) G peak position and (b) I_{TP}/I_{GP} versus substrate bias, obtained in this work. For the substrate bias of 95 V, the right-most G peak position was obtained, possibly indicating highest sp^3 content.

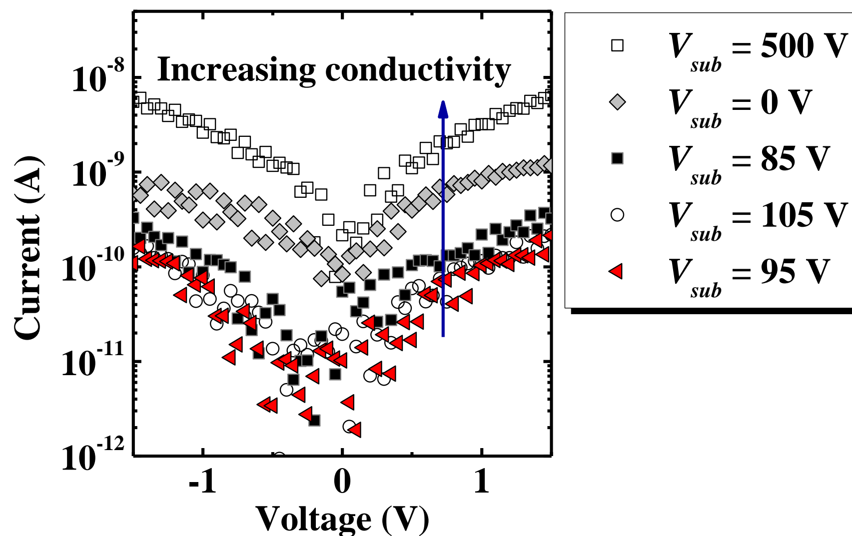


Fig. 2.11. Current versus voltage characteristics of DLC films deposited using different V_{sub}. The current-voltage data were obtained by placing two probes spaced ~100 μm apart.

Electrical characterization was performed on the blanket DLC films deposited on Si samples which have similar size to further verify that the V_{sub} of 95 V leads to the highest resistance. Sheet resistance measurement was performed, but did not get

any meaningfully data, as sheet resistance of DLC film is too large. The samples were characterized by a semiconductor analyser which has a much higher resolution. Two probes were landed on DLC film to measure the current versus voltage characteristics of the DLC films using the semiconductor analyser. The distance between the two probes is approximately 100 μm and is maintained the same across all DLC samples in order to fairly compare the resistance of all samples. Fig. 2.11 shows the current-voltage plots for DLC films deposited under different V_{sub}, demonstrating that the V_{sub} of 95 V leads to the highest resistance. Therefore, the V_{sub} of 95 V was selected for device integration.

Besides high resistivity, another important factor affects the direct realization of DLC on transistors is adhesion between DLC and parts of transistor. It was found in this work that surface cleanliness of the sample has a large impact on adhesion of DLC on devices. Therefore, strict measures of wafer cleaning, drying, and transfer to vacuum chamber of FCVA system were adopted to achieve better adhesion between DLC liner and the underlying p-FETs.

2.4. Integration of DLC on Si Planar p-FETs for Performance Enhancement

2.4.1 Device Fabrication

P-FETs used in this study were fabricated on eight-inch bulk Si substrates. Schematics of p-FETs studied here are shown in Fig. 2.12 (a) - (c). After forming the gate stack comprising pre-doped poly-Si on ~2.6 nm thermal silicon oxide (SiO_2), source/drain (S/D) extension implant was performed. SiN spacers were then formed with a SiO_2 spacer liner, followed by deep S/D implant. Ni (~5 nm) was deposited by sputtering and annealed in a Rapid Thermal Processing (RTP) system to form ~11.5

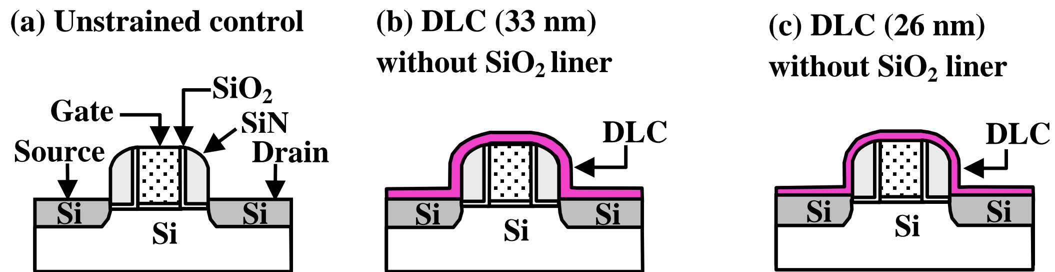


Fig. 2.12. Device cross-sections of (a) unstrained control p-FET, (b) p-FET with ~33 nm DLC liner, and (c) p-FET with ~26 nm DLC liner.

nm NiSi on S/D and poly Si gate. This finished the fabrication of the control device, as shown in Fig. 2.12 (a). For strained p-FETs shown in Fig. 2.12 (b) and (c), S/D contact pads was patterned with photoresist (PR) while the rest areas are exposed, followed by direct DLC deposition with a substrate bias of 95 V onto the devices. DLC deposition conditions were optimized in consideration of intrinsic stress, resistivity, and adhesion, as discussed earlier. Lift-off process was performed lastly to expose the contact area for electrical characterization. DLC thicknesses of ~33 nm [Fig. 2.12 (b)] and ~26 nm [Fig. 2.12 (c)] were used to study the DLC thickness effect on electrical performance of p-FETs. DLC having ~5 GPa intrinsic compressive stress was adopted in this work. Strict measures of wafer cleaning was adopted for better adhesion between DLC liner and the underlying p-FETs. The sample was quickly loaded into the FCVA chamber as soon as it was cleaned.

Fig. 2.13 (a) shows a transmission electron microscopy (TEM) image of a p-FET (L_G = ~85 nm) with a ~33 nm thick DLC liner directly deposited on top. Good adhesion between the DLC liner and the p-FET was observed. Fig. 2.13 (b) shows a high resolution TEM (HRTEM) of S/D region with DLC directly on top of NiSi/Si

stack. Devices with gate length L_G of 85 nm to 150 nm were fabricated and characterized.

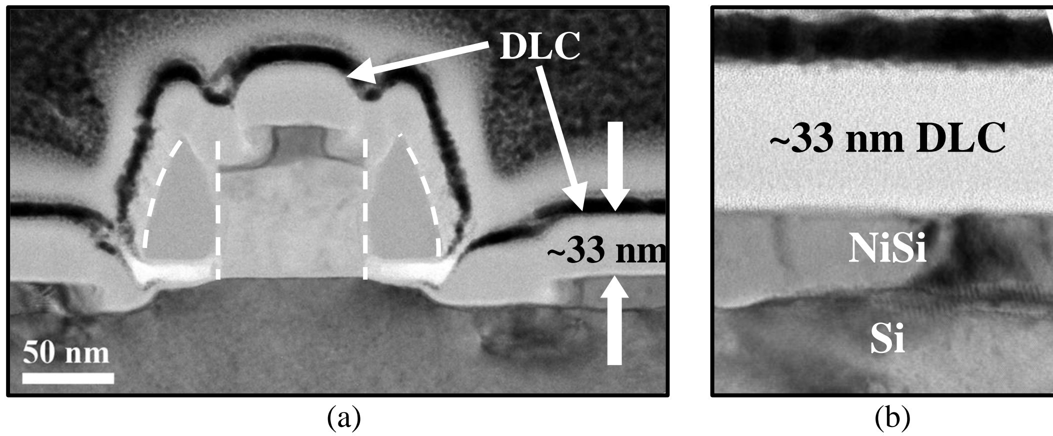


Fig. 2.13. (a) TEM image of a p-FET with ~33 nm DLC liner. DLC liner is directly deposited on the p-FET without a SiO_2 liner. Good adhesion is observed. (b) HRTEM of DLC on NiSi/Si of the S/D region.

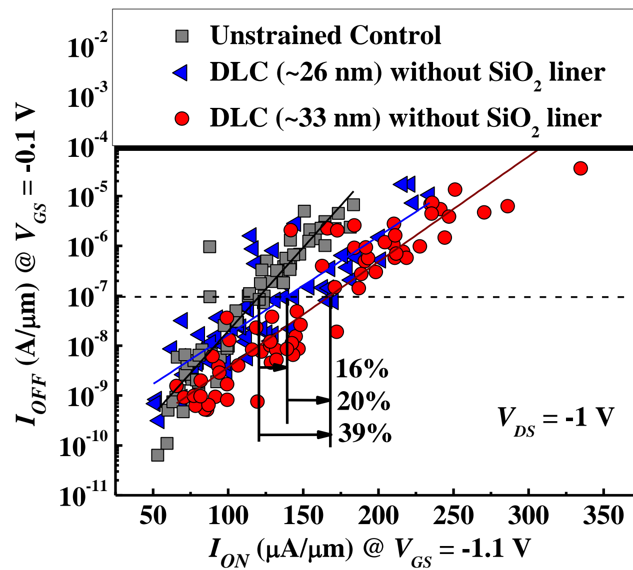


Fig. 2.14. I_{OFF} versus I_{ON} for p-FETs with different DLC liner thicknesses and control p-FET. P-FETs with DLC liner of ~33 nm and ~26 nm have 39 % and 16 % higher I_{ON}, respectively, than the control.

2.4.2 Results and Discussion

Fig. 2.14 compares the off-state current I_{OFF} versus on-state current I_{ON} characteristics of p-FETs without DLC liner and with DLC liners having various thicknesses. I_{ON} is taken at gate voltage V_{GS} = -1.1 V and drain voltage V_{DS} = -1 V, and I_{OFF} is taken at V_{GS} = -0.1 V and V_{DS} = -1 V. Direct deposition of DLC liner with a thickness of ~33 nm and ~26 nm gives rise to 39 % and 16 % I_{ON} enhancement at a fixed I_{OFF} of 1×10^{-7} A/μm, respectively, as compared with the unstrained control p-FETs.

The on-state current enhancement achieved is a result of mobility increment. The longitudinal uniaxial compressive stress in the channel leads to valence sub-bands warping, splitting, and up-shifting of light hole band. The curvature modulation due to stress results in smaller effective hole mass along the channel

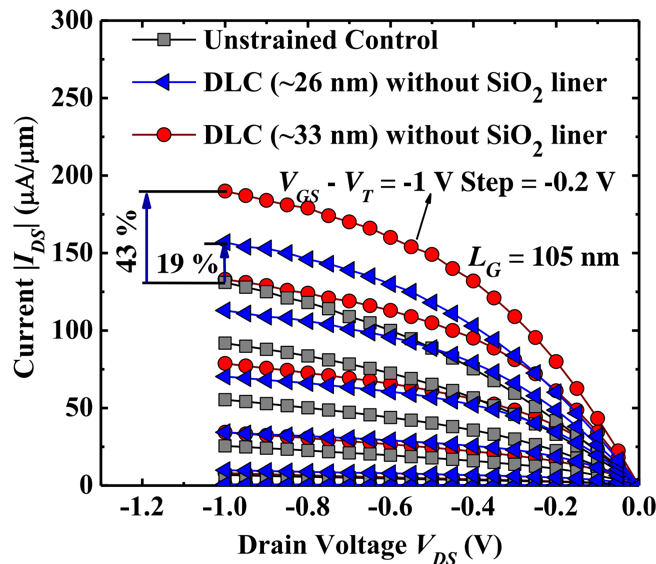
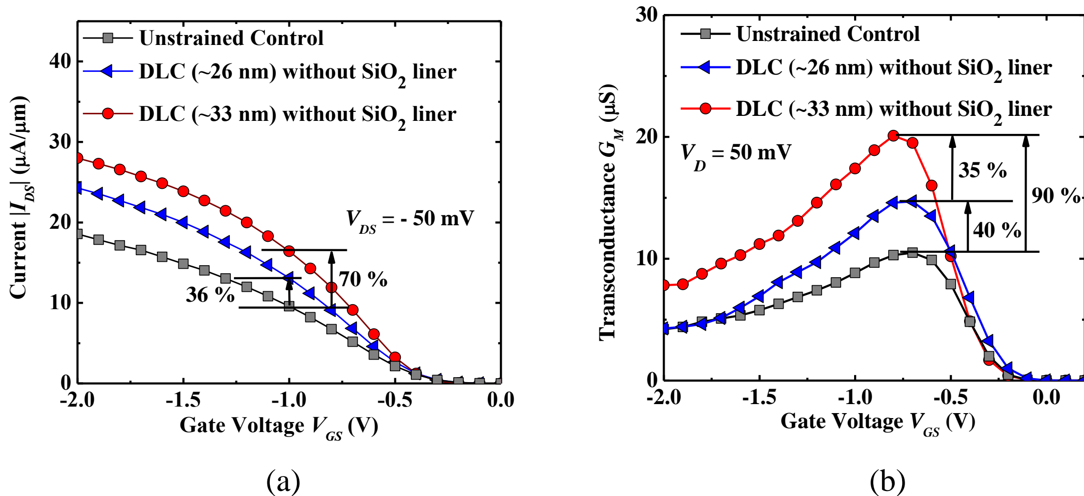


Fig. 2.15. $|I_{DS}|$ versus V_{DS} plots for unstrained p-FET and strained p-FETs with 26 nm and 33 nm DLC liner. P-FETs with ~33 nm DLC liner and ~26 nm DLC liner show 43 % and 19 % higher I_{on}, respectively, than a control at a gate overdrive of -1 V.

direction, leading to higher carrier mobility. In addition, the separation between the light hold and heavy hole sub-bands reduces inter-sub-band scattering, further contribute to carrier mobility enhancement.

Drain current $|I_{DS}|$-V_{DS} characteristics in Fig. 2.15 demonstrates that the p-FET with ~33 nm DLC liner has a 43 % drain current enhancement for over the control p-FET at V_{DS} = -1 V and gate over drive V_{GS} - threshold voltage V_{TH} of -1 V. The p-FET with ~26 nm DLC shows a 19 % saturation drain current improvement. Fig. 2.16 (a) shows that at V_{DS} = -50 mV and V_{GS} = -1 V, the linear drain current enhancement is 70 % and 36 % for p-FETs with a DLC liner thickness of ~33 nm and ~26 nm. Fig. 2.16 (b) compares the transconductance G_M of strained and unstrained p-FETs. A peak transconductance enhancement of ~90 % was observed on p-FET with ~33 nm DLC liner, indicating substantial hole carrier mobility enhancement.

The experimental results that a thicker DLC liner stressor leads to higher performance enhancement. This is consistent with theoretical predication. The



(a) (b)

Fig. 2.16. (a) $|I_{DS}|$ versus V_{GS} for different p-FETs at V_{DS} = -50 mV. P-FETs with DLC liner of ~33 nm and ~26 nm have 70 % and 36 % higher I_{DS} than control p-FET, respectively. (b) Peak transconductance increases by 40 % and 90 % for p-FETs with ~26 nm and ~33 nm DLC liners, respectively, as compared with control.

change of the carrier mobility caused by strain in a transistor channel can simply be expressed as:

$$\frac{\Delta\mu}{\mu} \approx \left| \pi_{\parallel}\sigma_{\parallel} + \pi_{\perp}\sigma_{\perp} \right|, \qquad (2\text{-}1)$$

where μ is carrier mobility, $\Delta\mu$ is mobility change due to strain effect, the subscripts $\parallel$ and $\perp$ refer to the directions parallel (longitudinal) and perpendicular (transverse), respectively, to the direction of the current flow in the MOSFETs, $\sigma_{\parallel}$ and $\sigma_{\perp}$ are the longitudinal and transverse stresses, respectively, $\pi_{/\!/}$ and $\pi_{\perp}$ are the piezoresistance coefficients for the two directions, respectively [3]. Strain in a transistor channel induced by a high stress liner is considered as uniaxial strain, so longitudinal strain is mainly responsible for the carrier mobility enhancement. Larger strain in the longitudinal direction could lead to a higher carrier mobility enhancement. In this work, the channel strain induced by the 33 nm DLC liner is believed to be higher, as compared with that due to the 26 nm DLC. Therefore, it is expected that the thicker DLC liner stressor leads to higher performance enhancement.

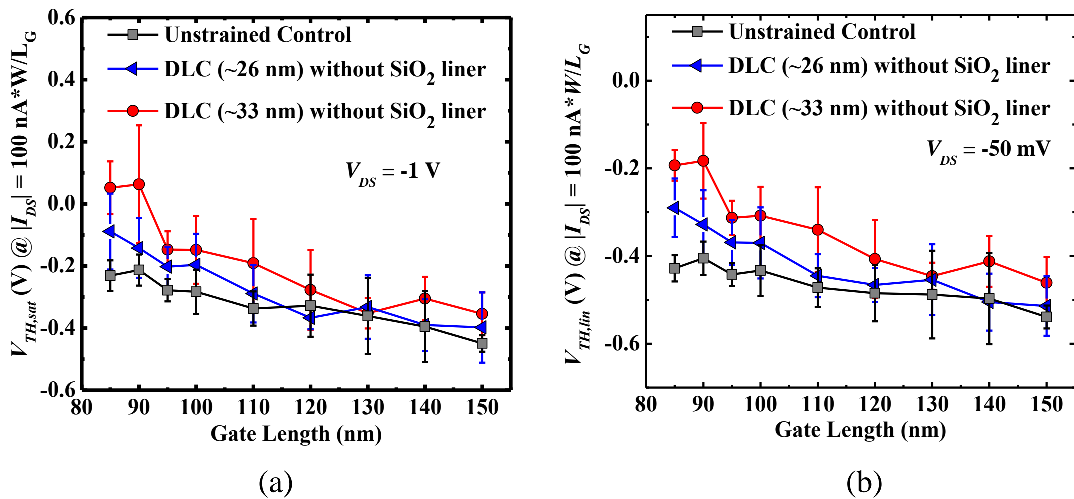


Fig. 2.17. (a) $V_{TH,sat}$ versus gate length L_G and (b) $V_{TH,lin}$ versus L_G, showing that higher strain leads to smaller $V_{TH,sat}$, as well as $V_{TH,lin}$. The error bar is the standard derivation. Larger channel strain results in smaller threshold voltage.

Fig. 2.17 (a) compares saturation threshold voltage $V_{TH,sat}$ of p-FETs with and without DLC liner. $V_{TH,sat}$ is taken as the V_{GS} where $|I_{DS}|$ = 100 nA $\times W_G/L_G$, where W_G is the gate width. It can be observed that a thicker DLC liner, presumably giving a higher channel stress, generally gives a smaller $V_{TH,sat}$. Similarly, Fig. 2.17 (b) shows that a higher channel stress results in smaller linear threshold voltage $V_{TH,lin}$. The decrease of V_{TH} of strained p-FETs with DLC liner stressor is mainly due to band gap narrowing of Si caused by strain in the channel [15]. The threshold voltage of a long channel transistor can be simply expressed as:

$$V_{TH} = \Phi_{MS} + \psi_S + \frac{Q_{DEP}}{C_{OX}} - \frac{Q_{OX}}{C_{OX}}, \qquad (2\text{-}2)$$

$$\Phi_{MS} = \Phi_M - (\chi' + \frac{E_G}{2e} - \phi_{fn}), \qquad (2\text{-}3)$$

where Φ_M is metal work function, χ' is the modified electron affinity (electron affinity difference between channel material and oxide), E_G is semiconductor band gap, ϕ_{fn} is bulk pontential, ψ_S is surface potential, Q_{DEP} is depletion charge, and Q_{OX} is oxide charge. Φ_{MS} is a function of semiconductor bandgap. Any change in Si band gap due to strain will lead to change in Φ_{MS} and V_{TH}.

Fig. 2.18 demonstrates that there is no significant difference in drain induced barrier lowering (DIBL) among the strained and unstrained p-FETs. The DLC liner stressor does not affect the short channel characteristics.

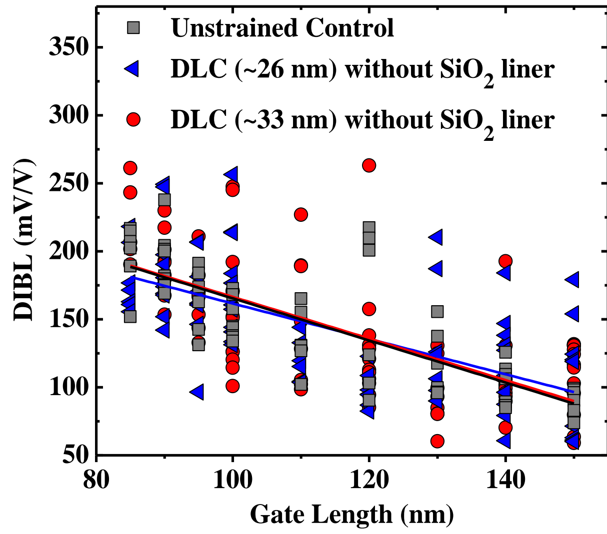


Fig. 2.18. DIBL versus gate length for p-FETs with and without DLC liner.

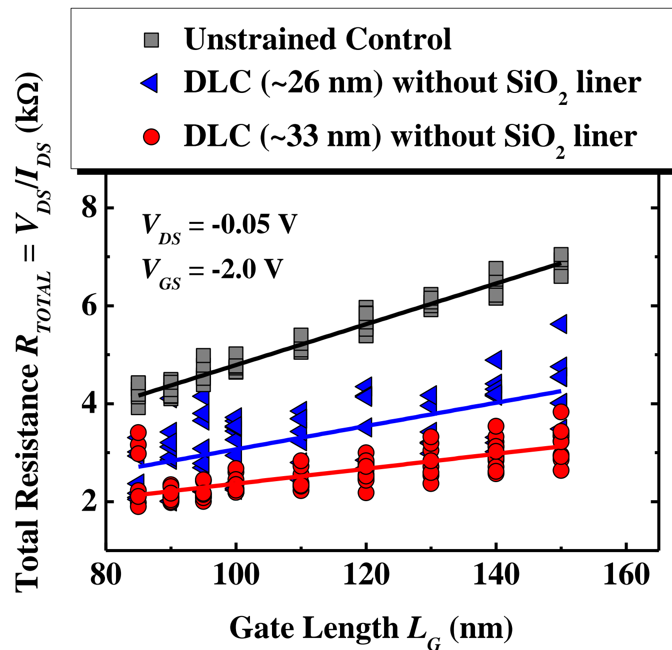


Fig. 2.19. R_{TOTAL} versus gate length L_G plots for the three splits. Devices with 33 nm DLC liner have the smallest R_{TOTAL} among the three splits.

Fig. 2.19 shows total resistance R_{TOTAL} versus L_G characteristics for the three different splits. R_{TOTAL} is calculated as V_{DS} divided by I_{DS}, where V_{DS} = -0.05 V. The lines shown in this figure are the best fit lines. I_{DS} was taken at V_{GS} = -2.0 V at which

the devices are at strong inversion. Devices with 33 nm DLC liner have the smallest R_{TOTAL} among the three splits. Hole mobility can be expressed as Equation 2-4 [97]:

$$\mu = \frac{1}{W\,Q_{INV}\,\dfrac{dR_{TOTAL}}{dL}}, \tag{2-4}$$

where μ is carrier mobility, W is the gate width, and Q_{INV} is the inversion charge density. From this equation, it can be concluded that the smaller $\frac{dR_{TOTAL}}{dL}$ is, the larger the mobility is. From Fig. 2.19, p-FETs with ~26 nm and ~33 nm DLC show smaller $\frac{dR_{TOTAL}}{dL}$ as compared with the control p-FETs, demonstrating higher hole mobility.

Fig. 2.20 shows that at a fixed DIBL of 150 mV/V, the saturation drain current taken at a gate overdrive (V_{GS} - $V_{TH,sat}$) of -1 V is enhanced by 56 % and 25 % for p-FETs with DLC liner thicknesses of ~33 nm and ~26 nm, respectively. This further demonstrates that direct deposition of DLC liner onto Si p-FETs can lead to

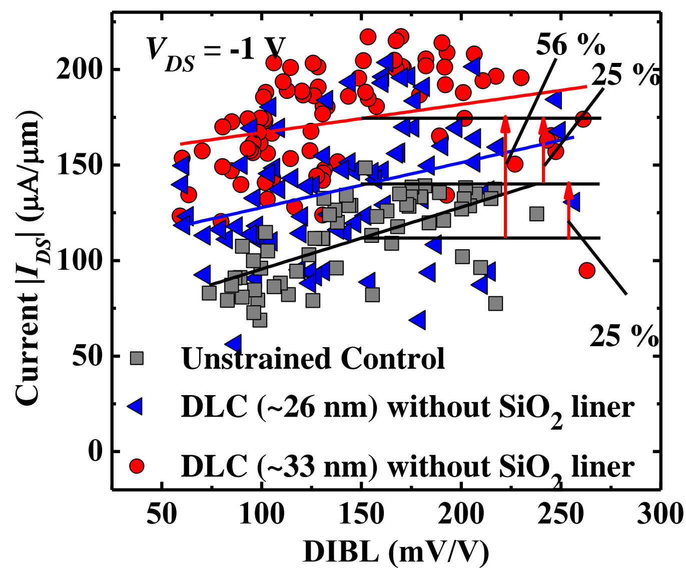


Fig. 2.20. At a fixed DIBL of 150 mV/V and V_{DS} of -1 V, DLC liner provides up to 56 % I_{DS} (taken at V_{GS}-V_{TH} = -1 V) enhancement.

significant performance enhancement. The I_{DS} variations at different DIBL are due to Random Dopant Fluctuation (RDF) [98, 99], nanowire linewidth variation, and gate length variation (lithography and trimming related). RDF could primarily cause threshold voltage variations, which in turn leads to drive current variations of the devices. The linewidth variation of the Si nanowire, which could be due to lithography and nanowire formation related process, could also results in change of device drive current, as the effective channel width changes with the linewidth. Lastly, variation of gate length could also leads to current variations.

2.5. Integration of DLC High Stress Liner on Advanced Nanowire p-FETs

2.5.1 Background

Nanowire FET enables CMOS device scaling to sub-10 nm gate lengths L_G [100-109], due to its excellent control of short channel effects (SCE). Realizing high drive current I_{ON} in Si nanowire FET requires high channel mobility and reduced external series resistance R_{EXT}. R_{EXT} reduction using Dopant Segregation Schottky (DSS) source/drain (S/D) [110-112] was recently demonstrated for the nanowire device structure [113]. However, there is limited work on strain engineering for Si nanowire p-FETs [107, 114] , especially on the impact of liner stressor on performance. The integration of Diamond-Like-Carbon (DLC) liner stressor with high compressive stress with Si p-FETs for performance enhancement was demonstrated [20-22, 82, 83, 115]. The impact of DLC high stress liner on the performance of nanowire p-FETs have not been investigated so far.

In this Section, the first realization of strained Gate-All-Around (GAA) nanowire p-FETs with a DLC liner stressor will be reported. DLC liner stressors of

Fig. 2.21. Process flow used to fabricate nanowire p-FETs with DLC liner stressor.

different thicknesses were formed on nanowire p-FETs with DSS S/D. DLC stressors were deposited with the direct deposition technique developed previously.

2.5.2 Device Fabrication

The key process to fabricate nanowire p-FETs is shown in Fig. 2.21. Silicon-on-insulator wafers were used as starting substrates, on which active patterns with sub-100 nm Si lines were formed. Free-standing or suspended Si nanowires with a linewidth of at least 17 nm were formed by thermal oxidation and SiO_2 removal [116]. SiO_2 gate dielectric (~2.6 nm) was formed on the nanowires by thermal oxidation, followed by conformal deposition of poly-Si, gate lithography, and dry etch to form the gate stack. Two step ploy Si gate etch process was adopted to remove the poly Si under the nanowire outside the gate region. Table 2.2 shows the two recipes used for poly Si gate etch of nanowire p-FETs [117]. The first step (which is also be referred to as main gate etch) is standard poly Si gate etch process which is normally

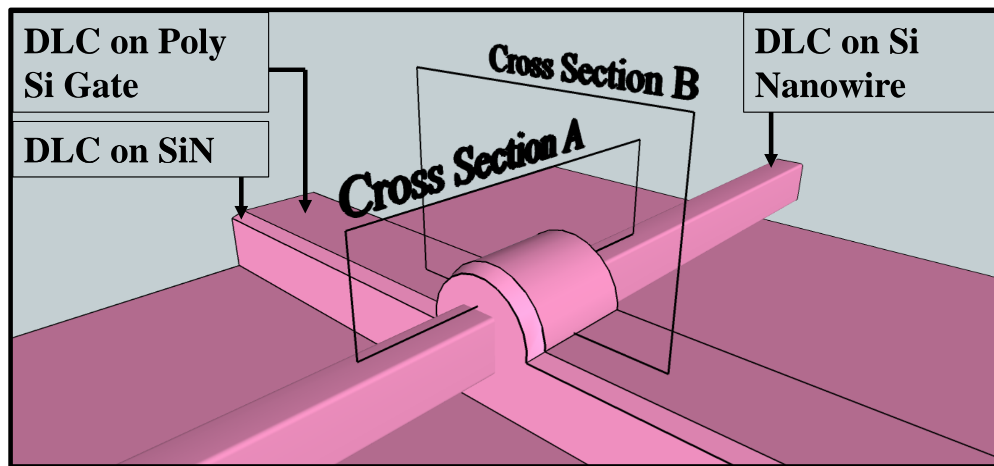
Table 2.2. Gate etch recipes for poly Si gate etch (main etch for removing poly Si in planar region) and poly Si spacer removal etch (over etch step). The poly Si over etch recipe employs HBr and smaller power to achieve a much higher etch selectivity of poly Si over thermal oxide.

Recipe Name	Cl_2 (sccm)	HBr (sccm)	He-O_2 (sccm)	Power (W)	Pressure (mTorr)
Main Poly Si Gate Etch	60	0	10	400	70
Poly Si Over Etch	0	35	5	75	80

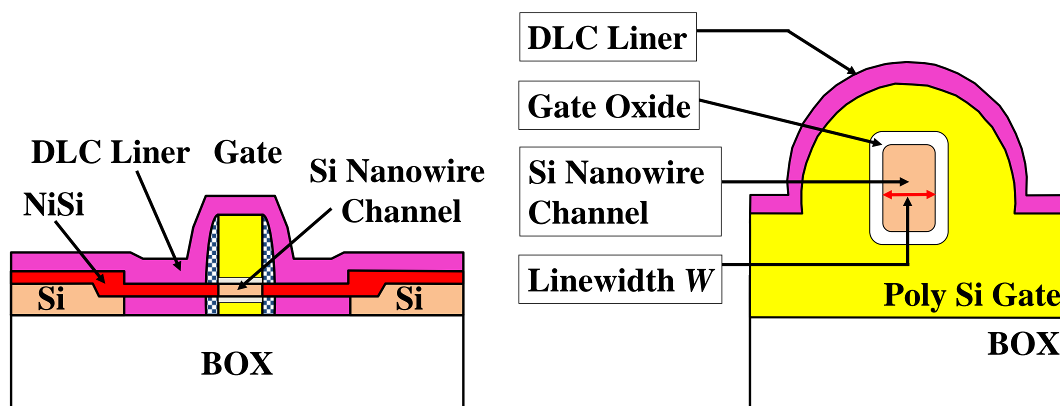
used for planar MOSFETs. Cl_2 and He-O_2 were used in the main poly Si gate etch recipe. Once the etch endpoint was detected, the etch process was switches to poly Si over etch process which makes use of HBr and He-O_2 to get high etch selectivity of thermal oxide over poly Si. The power and pressure of the poly Si over etch recipe was also reduce to have larger etch selectivity. L_G ranges from 55 to 115 nm.

S/D Extension implant (BF_2 dose of 10^{13} cm^{-2} and energy of 7 keV), silicon nitride spacer formation, and heavy S/D implant (BF_2 dose of 3×10^{15} cm^{-2} and energy of 30 keV, and BF_2 dose of 1×10^{15} cm^{-2} and energy of 15 keV) were done. The spacers were trimmed, followed by dopant segregation implant (BF_2 dose of 1×10^{15} cm^{-2} and energy of 7 keV), rapid thermal annealing at 950 ℃ for 1 s. 4 nm of Ni was deposited and silicidation was performed at 450 ℃ 30 s. Excess Ni was removed to complete the fabrication of control nanowire p-FETs.

For the strained nanowire p-FET splits, additional process steps of DLC liner stressor deposition and patterning were performed. DLC thickness t_{DLC} of 20 nm and



(a)



(b) (c)

Fig. 2.22. (a) 3D schematic of nanowire p-FET covered with DLC stress liner (violet in color). (b) Images of cross section A along the direction as shown in (a) of nanowire p-FET. (c) Images of cross section B of nanowire p-FET.

40 nm were used. The DLC deposition was performed using a FCVA system [20-22, 82, 83, 115]. A substrate bias of 95 V was used to achieve high sp^3 content, high film stress, and low conductivity for the DLC film, as described earlier. The intrinsic stress of DLC with t_{DLC} of 20 nm was obtained to be ~7 GPa from wafer curvature measurement.

Fig. 2.22 (a) shows 3D schematic of the nanowire p-FET covered with DLC stress liner represented by violet color film. The DLC liner covers everywhere of the transistor except for the contact pads. Fig. 2.22 (b) and (c) are the cross sectional

schematics in the longitudinal (cross section A) and transverse (cross section B) directions.

Fig. 2.23 (a) shows a tilted-view Scanning Electron Microscopy (SEM) image of a strained p-FET with DLC liner stressor directly deposited on top. No delamination of the high stress DLC liner was observed, indicating good adhesion between the DLC liner and underlying nanowire p-FET. A focused ion beam (FIB) cut was performed in the direction perpendicular to the nanowire for TEM analysis. Fig. 2.23 (b) shows the cross-sectional TEM image of a p-FET with DLC liner stressor having t_{DLC} of 40 nm.

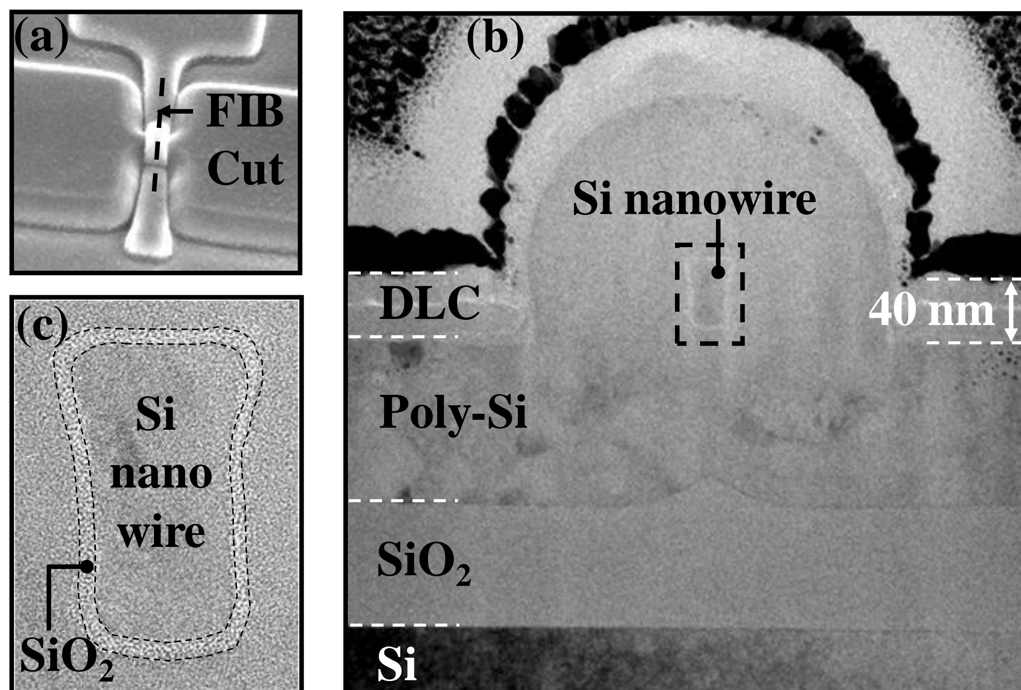


Fig. 2.23. (a) Top view SEM image shows a DLC-coated nanowire FET. A FIB cut was performed in a direction perpendicular to the channel or nanowire, as indicated by the dashed line, for TEM imaging. (b) Cross-sectional TEM image shows excellent adhesion of DLC liner on the poly-Si gate which surrounds the Si nanowire. (c) Analysis of the high resolution TEM (HRTEM) image shows that the nanowire has a linewidth W of 17 nm and a perimeter of 110 nm. The gate oxide thickness is 2.6 nm.

The DLC liner adheres very well with the underlying nanowire p-FET. Fig. 2.23 (c) shows a high resolution TEM (HRTEM) image of the nanowire. It is rectangular in shape, has a linewidth W of 17 nm and a perimeter P of ~110 nm. We define a parameter termed as the effective diameter D_{EFF} which is the diameter of a nanowire with a circular cross section and having a circumference that is equal to the perimeter of the rectangular nanowire. From Fig. 2.23 (c), the nanowire has a D_{EFF} of ~35 nm.

2.5.3 Results and Discussion

Fig. 2.24 (a) and (b) show the cumulative plots of I_{ON} of unstrained and strained p-FETs with W of 17 and 37 nm, respectively. I_{ON} is defined to be the drain current I_{DS} at a gate voltage V_{GS} of -1.2 V and a drain voltage V_{DS} of -1.2 V. P-FETs with DLC liner stressors have larger I_{ON} than the control devices. The DLC liner induces a longitudinal compressive stress along the nanowire, enhancing the hole mobility. For W of 17 nm, the median I_{ON} values for devices with t_{DLC} of 0, 20 and 40 nm are 14.8 μA, 17.6 μA, and 19.3 μA, respectively. A median I_{ON} of 19.3 μA for t_{DLC} = 40 nm translates to a normalized I_{ON} of 1135 μA/μm and 175 μA/μm when taken with respect to W and P, respectively. I_{ON} is higher for t_{DLC} = 40 nm than for t_{DLC} = 20 nm. DLC liner stressors enhance I_{ON} of devices with W of 37 nm similarly [Fig. 2.24 (b)]. Generally, a thicker DLC liner stressor induces a larger compressive stress in the channel, leading to a larger enhancement of hole mobility. This observation is consistent with theoretical prediction in Equation 2-1 described in Section 2.4.

The I_{ON} enhancement is slightly larger for a smaller W. This trend is also observed in numerical simulations, where the compressive stress in the nanowire

increases as W decreases. S. Mayuzumi *et. al*. demonstrated experimentally by UV-Raman spectroscopy characterization that the channel stress induced by the same SiN compressive (-2 GPa) stress liner on a transistor with a narrower gate width of 1 μm is larger than that with a wider gate width of 10 μm [118]. This is consistent with the observation in this work. The normalized drain current of nanowire p-FETs with a linewidth of 17 nm is lower than that of devices with a smaller nanowire dimension (diameter = ~12 nm) as shown in Ref. [113]. Similar observations have been reported elsewhere [116, 119-121]. It has been proposed that the volume inversion effect is responsible for the enhanced normalized I_{ON} (with respect to diameter or circumference) as nanowire dimension decreases [122].

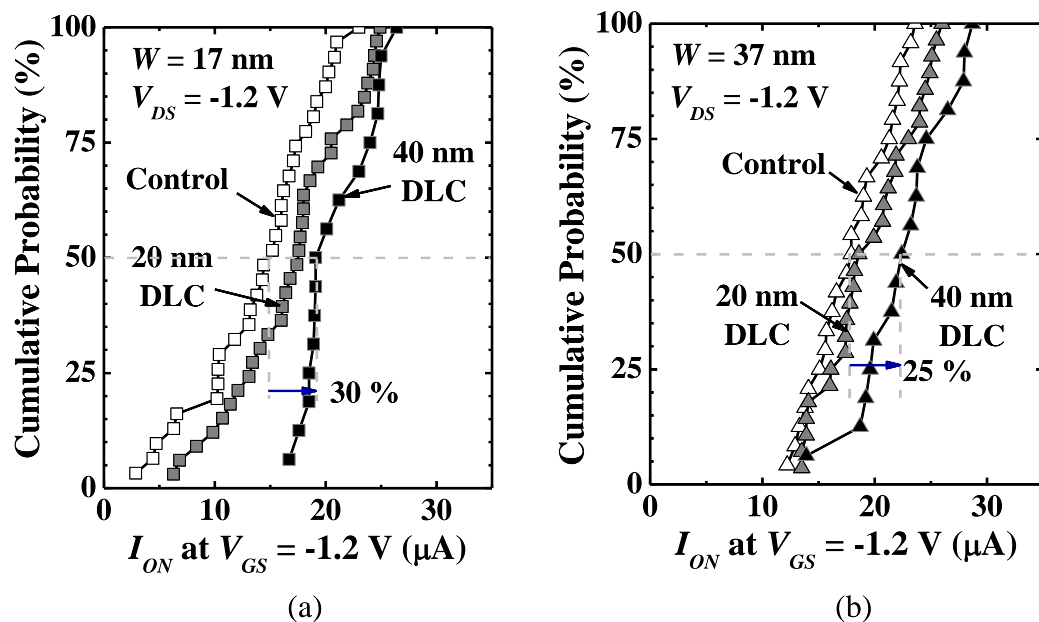


Fig. 2.24. Cumulative plot of I_{ON} of nanowire p-FETs with linewidth W of (a) 17 nm and (b) 37 nm. Devices with L_G ranging from 55 nm to 115 nm were characterized. The DLC liner enhances the I_{ON} of nanowire p-FETs, with higher I_{ON} enhancement for a thicker DLC liner.

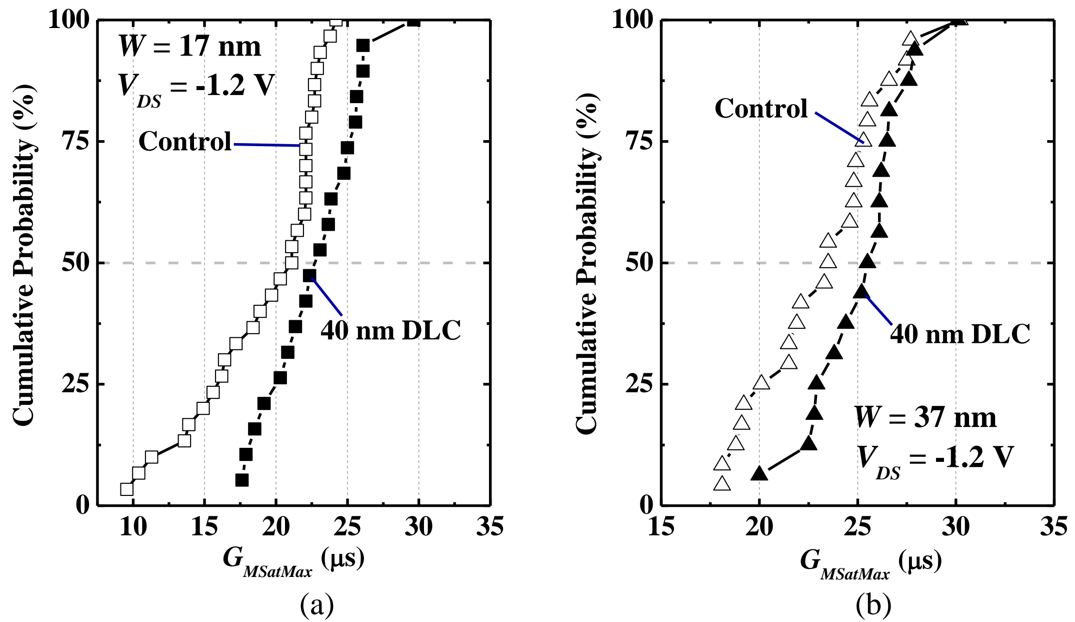


Fig. 2.25. Cumulative plots of peak saturation transconductance $G_{MSatMax}$ at V_{DS} = -1.2 V for strained p-FETs with 40 nm DLC and unstrained control p-FETs with the nanowire linewidth W of (a) 17 nm and (b) 37 nm.

Fig. 2.25 (a) and (b) demonstrate the peak saturation transconductance $G_{MSatMax}$ enhancement induced by 40 nm DLC liner stressor on p-FETs with W of 17 nm and 37 nm, respectively. Substantial median $G_{MSatMax}$ enhancement was observed for devices with W of 17 nm and 37 nm, indicating hole mobility enhancement caused by uniaxial compressive stress in the channel region.

Fig. 2.26 plots I_{ON} versus Drain Induced Barrier Lowering (DIBL) for strained and unstrained p-FETs with W of 37 nm. I_{ON}-DIBL plot is another graph to examine performance enhancement by DLC liner stressor. The lines drawn in Fig. 2.26 are best fit lines of the data points. At a fixed DIBL of 100 mV/V, p-FETs with 40 nm DLC and 20 nm DLC show I_{ON} enhancement of 22 % and 11 %, respectively, over the control devices. This demonstrates the substantial performance enhancement achieved by the DLC liner stressor for a given DIBL.

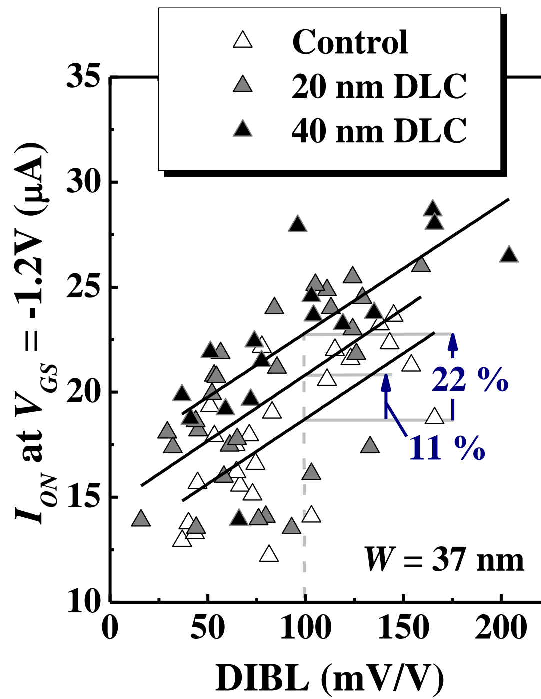


Fig. 2.26. I_{ON}-DIBL plot for strained and unstrained p-FETs with the same nanowire linewidth W of 37 nm. For each device split, a best fit line (solid) is drawn. Devices strained with DLC liner stressor show higher I_{ON} for a given DIBL.

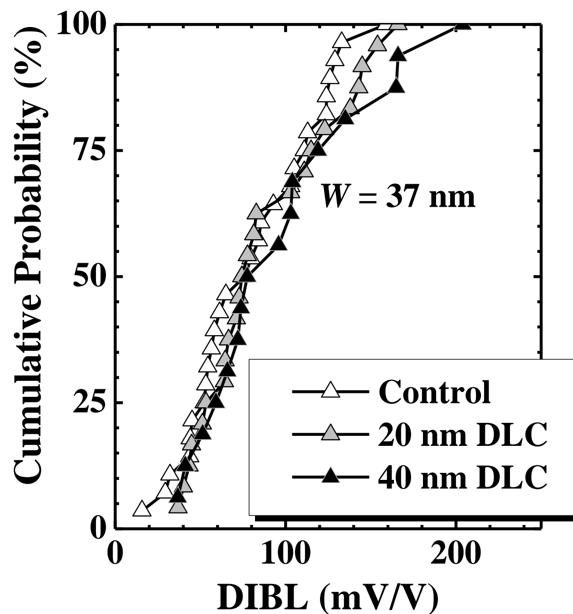


Fig. 2.27. Cumulative plot of DIBL for all three device splits, showing excellent match in control of short channel effects. The median DIBL values for all three devices splits are the same.

The distribution plots of DIBL are shown in Fig. 2.27, which are very well-matched for all splits. The median DIBL for all three splits are ~80 mV/V. DIBL is

well-controlled due to the gate-all-around device architecture. Integration of DLC liner stressor does not appear to compromise the control of short channel effects or introduce much additional device variability (Fig. 2.27). The main contributors to the scatter or spread in I_{ON}-DIBL plot are random dopant fluctuation (RDF) [98, 99], L_G variation, and nanowire linewidth variation due to aggressive linewidth trimming processes used.

Fig. 2.28 shows I_{DS}-V_{GS} characteristics in log-linear scale. Devices with and without DLC liner show similar DIBL and subthreshold swing SS of ~95 mV/decade, further demonstrating that DLC liner stressor does not change device short channel characteristics. Fig. 2.29 (a) plots I_{DS} against V_{GS} - V_{TH} for unstrained p-FET and p-FETs with t_{DLC} of 20 nm and 40 nm DLC, demonstrating substantial I_{DS} enhancement at a fixed gate over drive V_{GS} - V_{TH}. In Fig. 2.29 (b), transconductance G_{MSat} versus

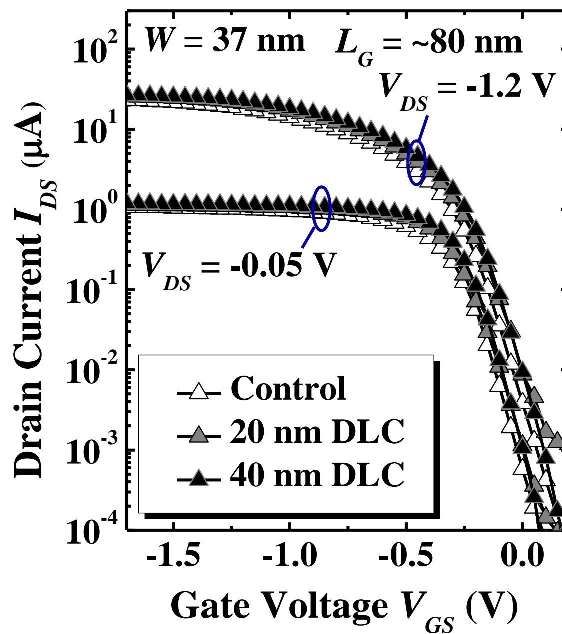


Fig. 2.28. I_{DS}-V_{GS} characteristics in log-linear scale. Devices with and without DLC liner show similar DIBL and subthreshold swing (~95 mV/decade). P-FETs with DLC liner stressor have larger I_{DS} for a fixed V_{GS}.

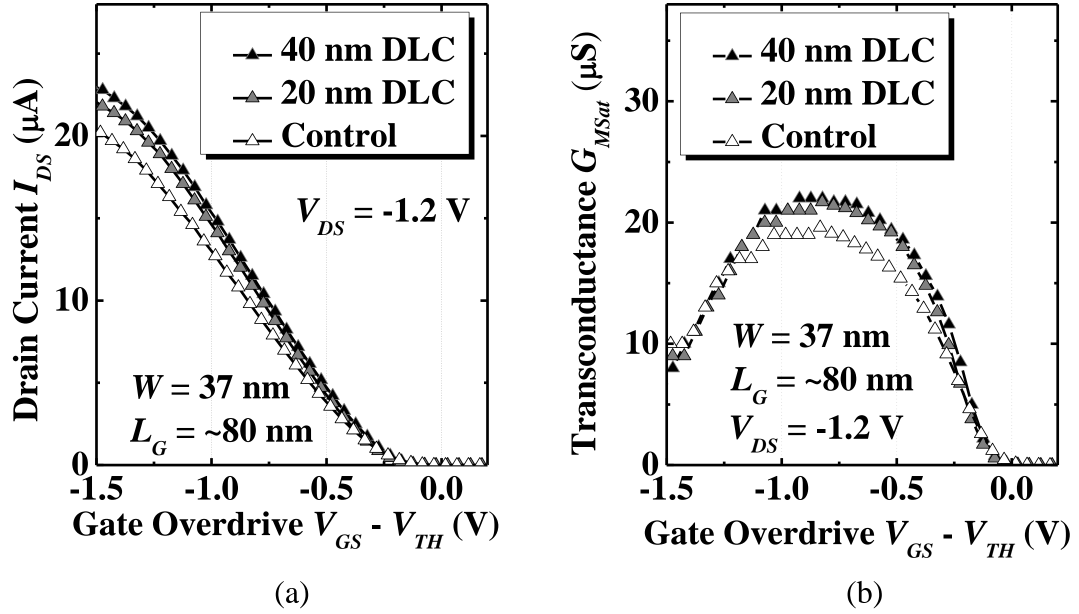


Fig. 2.29. (a) Drain current I_{DS} and (b) transconductance G_{MSat} of control p-FET without DLC liner (white symbol), p-FET with 20 nm thick DLC (grey symbol), and p-FET with 40 nm thick DLC (black symbol) as a function of gate over-drive (V_{GS} - $V_{TH,sat}$) at V_{DS} = -1.2 V. $V_{TH,sat}$ is the threshold voltage. The nanowire width W is 37 nm, and the gate length is 80 nm.

V_{GS} - V_{TH} curves are plotted for various p-FETs. It is demonstrated that the p-FETs with t_{DLC} of 20 nm and 40 nm show G_{MSat} enhancement over the control device, indicating enhancement of hole mobility by the compressive channel stress induced by DLC liner stressor.

Compressive stress in the channel causes shift and warping of valence band structure, and reduces the in-plane hole effective mass m^*. The reduced m^* leads to carrier mobility enhancement. Bandgap narrowing and shift of valence band edge lead to V_{TH} shift in p-FETs[123], as discussed earlier. Fig. 2.30 demonstrates that average V_{TH} shifts are ~40 mV and ~80 mV for p-FETs with t_{DLC} of 20 nm and 40 nm, respectively, as compared with unstrained control. V_{TH} shift of 40 mV caused by 20 nm DLC with an intrinsic stress of 7 GPa observed here is comparable with V_{TH} shift due to a 3.5 GPa SiN compressive liner with a thickness of 50 nm in Ref. [13]. The

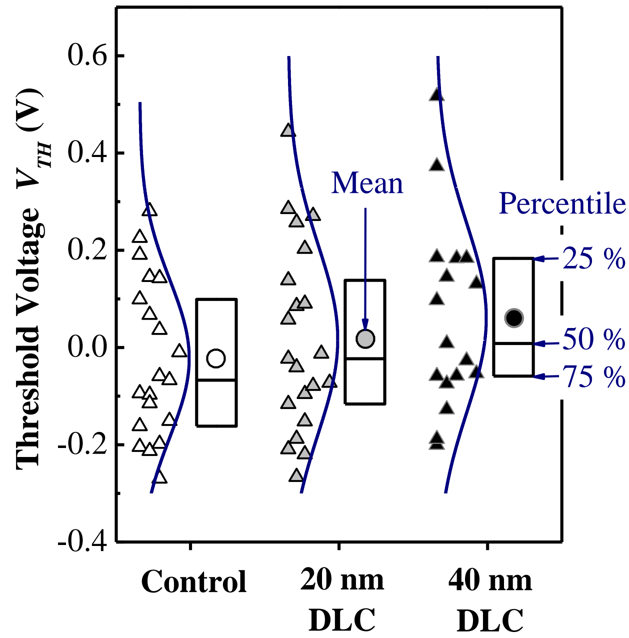


Fig. 2.30. The average threshold voltage shifts induced by 20 nm and 40 nm of DLC are 40 mV and 80 mV, respectively.

stress-thickness product of the 20 nm DLC (140 GPa×nm) is comparable with the 50 nm SiN liner (175 GPa×nm). The estimated channel stress leading to a V_{TH} shift of 40 mV is ~750 MPa. The high stress-thickness product was achieved with a much thinner DLC liner in this work, as compared with much thicker SiN liner in other reports.

2.6. Summary

By doing Taurus process simulation, it is demonstrated in Section 2.2 that the existence of SiO_2 adhesion layer in between the DLC liner and the underlying p-FETs degrades the channel stress induced by the DLC liner.

DLC material development to get high resistance and high stress DLC film for direct integration of DLC onto p-FETs without inserting the SiO_2 adhesion layer is

discussed in Section 2.3. Raman and electrical characterization of DLC films is reported.

The first demonstration of a DLC compressive-stress liner *directly deposited* on planar p-FETs is reported in Section 2.4. The new DLC technology does not employ a SiO_2 adhesion layer, providing better liner stressor scalability, simpler process integration and possibly higher channel stress, as compared with prior work. A drive current enhancement of 39 % was reported for strained planar p-FETs integrated with DLC liner, over unstrained control p-FETs.

In addition, we also demonstrated the first integration of DLC liner stressor on Gate-All-Around Si nanowire p-FETs in Section 2.5. DLC liner stressors with two thicknesses were employed to investigate the effect of liner thickness on device performance. Substantial enhancement in I_{ON} and $G_{MSat,max}$ were observed for nanowire p-FETs with DLC liner as compared with devices without the liner. Short-channel effects for all devices are comparable. A thicker DLC liner stressor leads to higher performance enhancement. Direct deposition of DLC liner shows good compatibility with extremely scaled nanowire transistors.

Chapter 3

NBTI Reliability of P-channel Transistors with Diamond-Like Carbon Liner

3.1 Background

Negative Bias Temperature Instability (NBTI) could lead to severe degradation of p-channel Field-Effect Transistor (p-FET) parameters, including threshold voltage V_{TH}, linear drain current I_{DLin}, saturation drain current I_{DSat}, and transconductance G_M, as discussed in Chapter 1. It is considered as one of the most significant reliability concerns for the state of the art integrated circuits [24-28].

Strain engineering is used as complementary metal-oxide-semiconductor (CMOS) performance booster in production since the 90 nm technology node [3, 81], and has brought significant drive current or speed enhancement for short-channel transistors. It is one of the key drivers for CMOS scaling and further extension of the Moore's Law. Due to the importance of strain engineering in modern integrated circuits, it is vital to have good understanding on how strain affects device reliability, such as NBTI. When a new strain engineering technology is considered for manufacturing, impact on device reliability should be investigated.

Although there are some reports claiming that strain has negligible effects on device NBTI performances [33-35], most publications in the literature suggest that strain has adverse effects on NBTI [23, 36, 37, 39-44]. Quite a few research groups

demonstrated that strained p-FETs with different structures suffer from more NBTI degradation, as compared with unstrained control p-FETs. H. S. Rhee *et. al.* [37] from Samsung and C.-S. Lu *et. al.* [23] from National Chiao Tung University proposed that high hydrogen content in compressive SiN liner and mechanical strain itself lead to more severe NBTI. E. Morifuji *et. al.* of Toshiba [36] and G. Thareja *et. al.* of UT Austin [39] suggested that increasing mechanical strain in the channel makes Si-H bonds at Si-SiO_2 interface easier to break, which causes strained transistors to be more vulnerable to NBTI. Strain induced enhancement of hole tunneling probablity was suggested to be another possible reason that degrades NBTI performance of biaxially strained p-FETs by T. Irisawa *et. al.* [40]. S.S. Chung of National Chiao Tung University proposed the enhanced impact ionization in strained devices is responsible for the higher NBTI degradation of FETs with S/D stressor (n-FETs with SiC S/D and p-FETs with SiGe S/D) in a series of papers [38, 124, 125]. They also suggested that stress liner induced vertical strain could lead to additional degradation.

Conventional compressive SiN liner stressor used to induce strain in p-FETs is facing serious scaling challenges. To address the scaling challenges, diamond-Like carbon (DLC) liner stressor technology was recently demonstrated to introduce very high levels of compressive stress in p-FETs for hole mobility and drive current I_{ON} enhancement [20-22, 82, 83]. The magnitude of stress in DLC, e.g. 5-7 GPa, is much higher than that of the conventional SiN liner [10, 13, 14]. In addition, the DLC liner has excellent thickness scalability and permittivity. The characteristics of DLC make it a promising candidate for further strain engineering. However, DLC is a new CMOS material as far as integration in MOSFET fabrication process is concerned. An important question to answer is whether the very high level of channel strain

induced by DLC would lead to serious reliability issues. It is unknown if the new DLC liner would introduce reliability issues, e.g. NBTI, in p-FETs. The NBTI reliability of p-FETs with DLC liner has never been investigated before.

In this Chapter, the first investigation of NBTI of unstrained p-FETs and p-FETs with DLC liner stressor is documented. It was demonstrated that degradation of NBTI could recovery at a very fast speed, as fast as 100 ns [29, 32, 126-128]. In order to more accurately capture NBTI degradation characteristics of a strained transistor with DLC liner, an ultra-fast measurement method (UFM) [measurement time $T_{measure}$ = ~2.2 micro second (μs)] was adopted in this work. A UFM setup similar to that in Ref. [129] was adopted, except that an improved high speed and low noise amplifier (DHPCA-100) was employed in this work. To the author's best knowledge, this was the first NBTI study on the effect of high stress liner on NBTI using UFM technique. Table 3.1 shows a few typical investigations of strain effects on NBTI available in the literature. Novelty and contribution of the current work are highlighted.

Detailed UFM setup will be discussed in this Chapter. NBTI results obtained by UFM and conventional current-voltage (IV) measurement method will be compared. Threshold voltage V_{TH} shift, drain current I_D degradation, and transconductance G_M loss under NBT stress for devices with different levels of channel strain, including p-FETs with SiGe S/D and p-FETs with DLC liner stressor, are reported. It is observed that transistors with higher channel strain generally have higher NBT degradation when stressed at the same gate stress voltage V_{stress}. Possible reasons for this observation are discussed. The NBTI recovery behavior of unstrained and strained devices is then investigated. Gate length L_G dependence of NBTI for

Table 3.1. Comparison table summarizes some works on strain effect on NBTI degradation in the literature.

Work	Year	Device Structure	Methods	Observation	Organization
[38]	2005	Biaxially strained Si on SiGe p-FETs	Charge pumping and gated-diode measurement	Strain degrades NBTI	National Chiao Tung University and UMC
[37]	2005	P-FETs with compressive SiN liner	DC Measurement	Compressive strain degrades NBTI	Samsung and Applied Materials
[39]	2006	Biaxially strained SOI p-FETs	DC Measurement	Compressive strain degrades NBTI	The University of Texas at Austin
[42]	2007	P-FETs with tensile and compressive SiN liner	DC Measurement	Compressive strain degrades NBTI	National Cheng Kung University and UMC
[40]	2007	Biaxially strained Si n-FETs and p-FETs	Charge pumping and DC Measurement	NBTI is degraded by biaxial tensile strain	Toshiba
[41]	2008	P-FETs with tensile SiN liner	DC Measurement	Tensile strain degrades NBTI for small L_G devices	National Cheng Kung University and UMC
[43]	2009	P-FETs with tensile and compressive SiN liner	Charge pumping and DC Measurement	Compressive SiN degrades NBTI, as compared with tensile SiN	Nanyang Technological University and Chartered Semiconductor[1]
This work	2009	P-FETs with SiGe S/D and p-FETs with DLC	UFM (*First UFM study of strain effect on NBTI*)	Compressive strain degrades NBTI	NUS
[44]	2011	SOI p-FETs with compressive SiN liner	Charge pumping and on-the-fly measurement	Compressive strain degrades NBTI	National Tsing Hua University

[1] Chartered Semiconductor Manufacturing is now GLOBALFOUNDRIES.

Table 3.2. Equipment used in UFM and their functions.

Equipment	Function
Function/Pulse Generator	To provide gate voltage pulse V_{GS} to transistors
Coaxial Cables and Wires	To transmit voltage signal
Digital Oscilloscope	To measure transistor current-voltage characteristics
Current-Voltage Amplifier	To amplified the original low drain current of the transistors
Home-Made Probe Holder	To reduce signal propagation delay

strained p-FETs with DLC will also be reported. In addition, the NBTI lifetime of p-FETs strained with DLC is projected using both the E_{ox} power law model and exponential V_{stress} model.

3.2 Measurement Setup

Conventional semiconductor analyser cannot measure transistor transfer characteristics, such as I_D versus gate voltage V_{GS} characteristics, at a very high speed (e.g., less than 1 ms) due to the long integration time (typically 0.1 s to 10 s). Therefore, DC method will not be able to capture a significant amount of threshold voltage shifts of NBTI [29, 32, 126-128], and UFM needs to be performed to accurately characterize NBTI.

Table 3.2 shows a list of equipment used in the UFM setup in this work, and Fig. 3.1 (a) shows a simplified circuit setup of the UFM setup. In order to accurately capture NBTI degradation characteristics of a transistor, pulse measurement technique is adopted. A pulse generator which is capable to output voltage pulse with a pulse

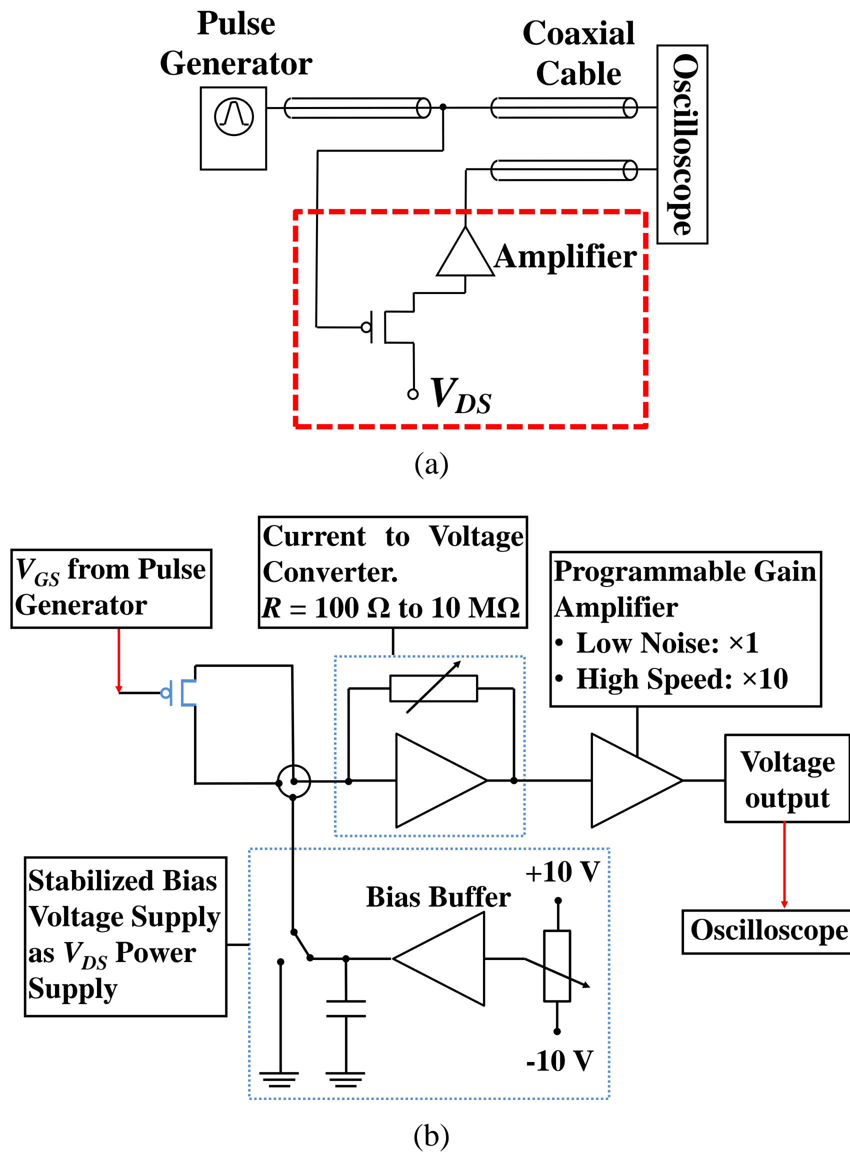


Fig. 3.1. (a) Simplified circuit schematic illustrating the Ultra-Fast Measurement (UFM) setup. The input terminal of the amplifier is at ground potential. Source to drain currents of the devices are almost the same. (b) Detailed connection setup of the part highlighted by the red dashed box in Fig. 3.1 (a).

width of less than 50 nanoseconds (ns) was employed to supply V_{GS} to transistors, as shown in Fig. 3.1 (a). An Infiniium Oscilloscope which has four input channels, a bandwidth of 500 MHz, and a sample rate of 2 GSa/s on all channels is used. Due to the sensing limit (or resolution) of the oscilloscope and the relative low current of our

transistors (a few tens of μA), an amplifier was introduced into the measurement setup to amplify the signal before it was collected by the oscilloscope. The input impedance of the oscilloscope, the output impedance of the pulse generator, the output impedance of the amplifier, and impedance of the co-axial cables are all 50 Ω. High speed and low noise current-voltage amplifier (DHPCA-100) was used to get more accurate and lower noise signals. Compared with the setup used by C. Shen *et. al.* [130], the new circuit adopting the new amplifier with adjustable gain also makes characterization of transistors with different current levels much easier and more convenient, as no more change of gain resistance is needed.

Fig. 3.1 (a) shows that the gate voltage V_{GS} is provided by the pulse generator and transistor current passing through the amplifier was monitored by the oscilloscope. Fig. 3.1 (b) shows the detailed connection setup of the part highlighted in the red box in Fig. 3.1 (a). Drain voltage was supplied by the built-in bias voltage supply of the amplifier, as shown in Fig. 3.1 (b).

In order to reduce the signal propagation delay due to wires and cables in the measurement circuit, home-made probe holders employing shorter signal transmission wires, instead of conventional probe holders using much longer cables to transmit signals, were used here. A photo of the probe holders is shown in Fig. 3.2. Using these home-made probe holders also facilitates the changing of probe tips, as compared with the measurement setup by C. Shen *et. al.* [130].

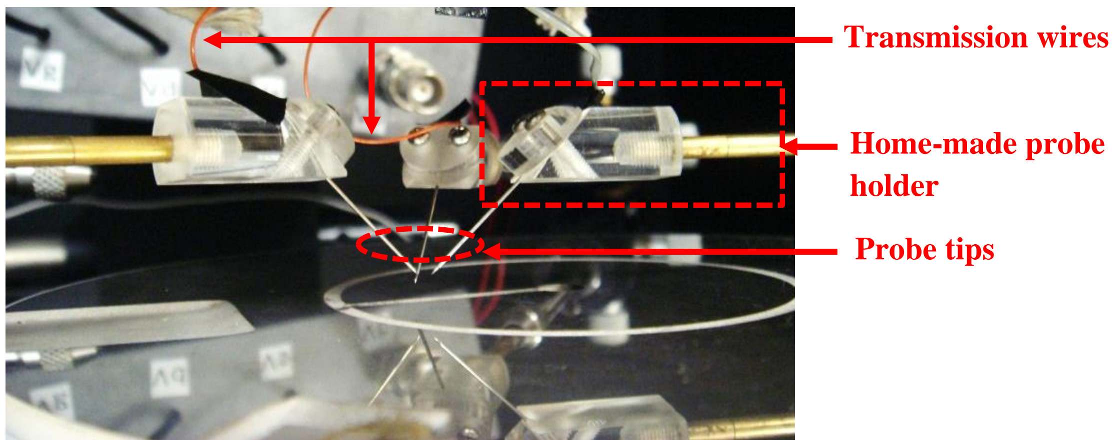
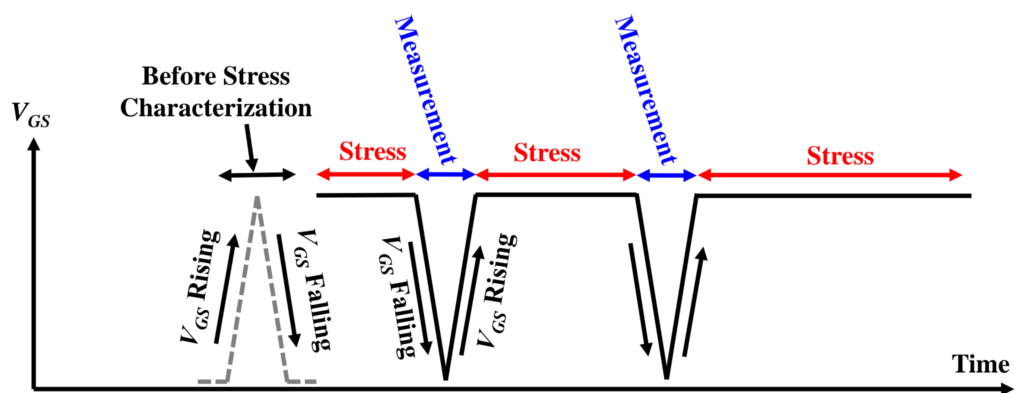
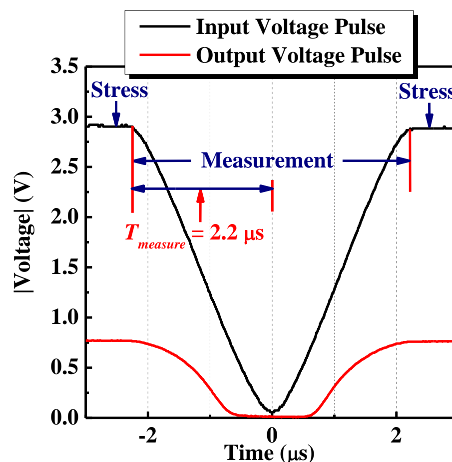


Fig. 3.2. Photo of home-made probe holders and connection of probe tips and transmission wires used to characterize the nano-scale transistors in this work. The probes were mounted to the micromanipulators of a conventional probe station. Short signal transmission wires were used to reduce the propagation delay.



(a)



(b)

Fig. 3.3. (a) Input waveform used for NBTI characterization. Initial characterization (before stress) and characterization during stress phase is illustrated. (b) Input (black line) and output (red line) voltage pulse during stress-measurement-stress cycle. Each measurement cycle containing two $|I_D|$-V_{GS} measurement swipes only takes ~4.4 μs, which could help minimize the interrupt to NBT stress and reduce recovery of V_{TH}.

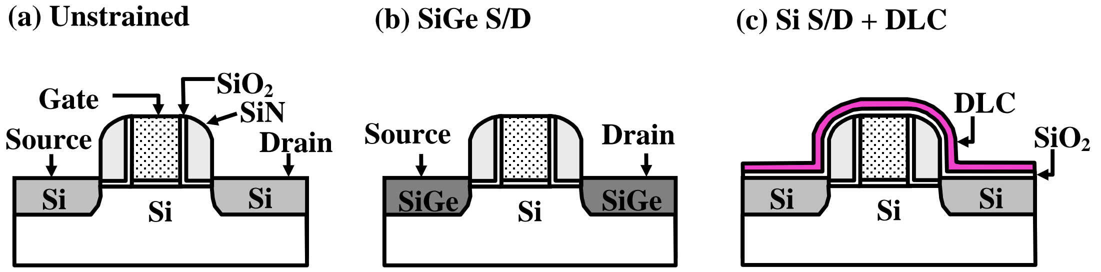


Fig. 3.4. Schematics of (a) unstrained p-FET with Si S/D, (b) strained p-FET with SiGe S/D, and (c) strained p-FET with Si S/D and DLC liner stressor. Devices in (a), (b), and (c) will be referred to as "unstrained p-FET", "p-FET with SiGe S/D", and "p-FET with Si S/D + DLC", respectively.

Fig. 3.3 shows the input voltage pulse (black line) during stress-measurement-stress (SMS) characterization cycles. The time used to measure one $|I_D|$-V_{GS} ($T_{measure}$) in this work is ~2.2 μs. A full measurement cycle including a falling edge and a rising edge takes ~4.4 μs. The red line in Fig. 3.3 is the output voltage V_{out} coming from a transistor. V_{out} is effectively the product of a transistor drain current I_D (unit: ampere A) and gain of the amplifier G_{AM} (ranging from 10^2 to 10^7 V/A).

3.3 Device Fabrication

P-FETs used in this work were fabricated on 8-inch bulk Si substrates. Schematics of p-FETs studied here are shown in Fig. 3.4 (a) - (c). After forming gate stack comprising pre-doped p^+ poly-Si gate on ~3 nm SiO_2 gate dielectric, S/D extension and SiN spacers were formed. For p-FETs in Fig. 3.4 (b), S/D recess etch (~60 nm) and selective epitaxial growth (~72 nm) of silicon germanium $Si_{0.75}Ge_{0.25}$ were performed to form $Si_{0.75}Ge_{0.25}$ S/D stressors. For p-FETs in Fig. 3.4 (c), DLC film (~27 nm) without hydrogen doping was deposited over 10 nm SiO_2 layer using a filtered cathodic vacuum arc (FCVA) deposition system. A substrate bias of 95 V

was employed to achieve high compressive stress in the channel. The intrinsic compressive stress of the DLC was ~5 GPa. Contacts were then formed to complete the device fabrication.

3.4 Results and Discussion

3.4.1 P-FET Performance Enhancement due to Strain

The p-FETs in Fig. 3.4 (a) - (c) were characterized. Off-state current I_{OFF} versus on-state current I_{ON} characteristics show that at a given I_{OFF} of 10^{-7} A/μm, the I_{ON} enhancements of p-FETs with SiGe S/D and p-FETs with DLC liner stressor are 11% and 22% [shown in Fig. 3.5], respectively, as compared to unstrained p-FETs. I_{ON} was taken at V_{GS} = -1.1 V and V_{DS} = -1.0 V. It is know that

$$\Delta\mu/\mu \approx \left|\pi_{\|}\sigma_{\|} + \pi_{\perp}\sigma_{\perp}\right|, \tag{3-1}$$

where μ is carrier mobility, Δμ is mobility change due to strain, the subscripts || and ⊥ refer to the directions parallel (longitudinal) and perpendicular (transverse), respectively, to the direction of the current flow in the MOSFETs, $\sigma_{\|}$ and $\sigma_{\perp}$ are the longitudinal and transverse stresses, respectively, $\pi_{\|}$ and $\pi_{\perp}$ are the piezoresistance coefficients for longitudinal and transverse directions, respectively [3]. Based on the electrical results and theoretical prediction of mobility enhancement due to channel strain in Equation 3-1, the devices with DLC liner presumably have larger channel strain as compared with those with SiGe S/D.

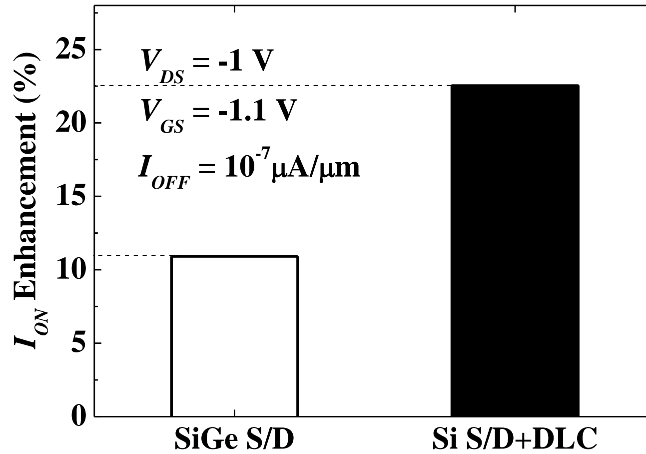


Fig. 3.5. I_{ON} enhancement for the strained p-FETs over the unstrained control p-FET. I_{ON} enhancements of p-FETs with SiGe S/D and p-FETs with DLC liner stressor are 11% and 22%, respectively, as compared to unstrained p-FETs.

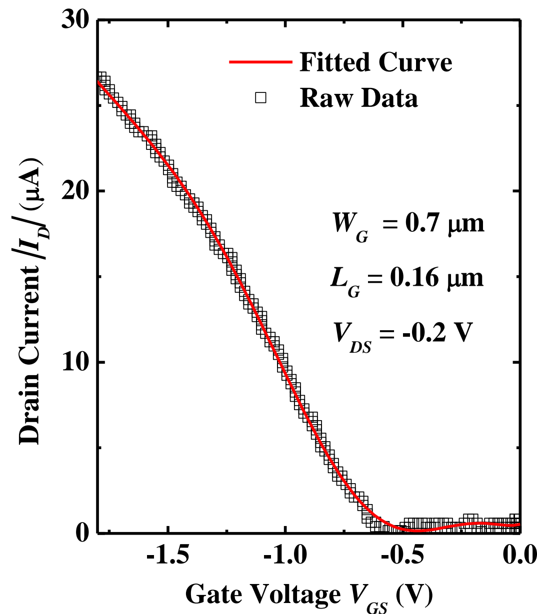


Fig. 3.6. $|I_D|$-V_{GS} of a p-FET measured by UFM method represented by open square and $|I_D|$-V_{GS} curve (red line) obtained by performing polynomial fits [131] on the raw data. Good fitting was achieved.

3.4.2 Comparison between DC and UFM Techniques

Fig. 3.6 shows measured (open square) and fitted (red lines) drain I_D versus gate voltage V_{GS} of a Si control p-FET characterized by UFM technique with a

measurement time of 2.2 μs (half pulse). $|I_D|$-V_{GS} curve represented by the red line is obtained by performing polynomial fits [131] on raw data (open squares) collectedmusing UFM. The fitting of the original raw $|I_D|$-V_{GS} curves results in smoother $|I_D|$-V_{GS} curves, which helps reduce the scattering in the data and yet maintains relatively good accuracy. The polynomial fit was performed using the data processing software Origin 8.0.

Fig. 3.7 (a) and (c) compare $|I_D|$-V_{GS} characteristics in linear-linear scale of two similar Si p-FETs measured by conventional DC measurement method and UFM technique, respectively. The curves shown in Fig. 3.7 (c) are fitted results of the raw data. Fig. 3.7 (a) shows that conventional DC measurement suggests that the threshold voltage V_{TH} has little shift after 10 s NBT stress V_{stress} of -2.9 V. On the other hand, UFM results in Fig. 3.7 (c) indicate a significant V_{TH} shift of a similar transistor after being stressed at same V_{stress} for the same period of time. It can be clearly observed that UFM technique captures a significant amount of V_{TH} shift which cannot be detected by conventional DC measurement method. This demonstrates that results measured by UFM reflect the total threshold voltage shift more accurately, while DC measurement method could only reflect the slow component of V_{TH} shift [32].

Fig. 3.7 (b) and (d) show the $|I_D|$-V_{GS} characteristics in log-linear scale of the same two Si p-FETs measured by conventional DC measurement method and UFM technique, respectively. Visible V_{TH} shift was observed on UFM extracted $|I_D|$-V_{GS} curve in log-linear scale. However, UFM method does not capture the off-state drain current very well when compared with the $|I_D|$-V_{GS} curves in Fig. 3.7 (b) and (d) at low gate voltage V_{GS}. This is because the digital oscilloscope is only capable of accurately

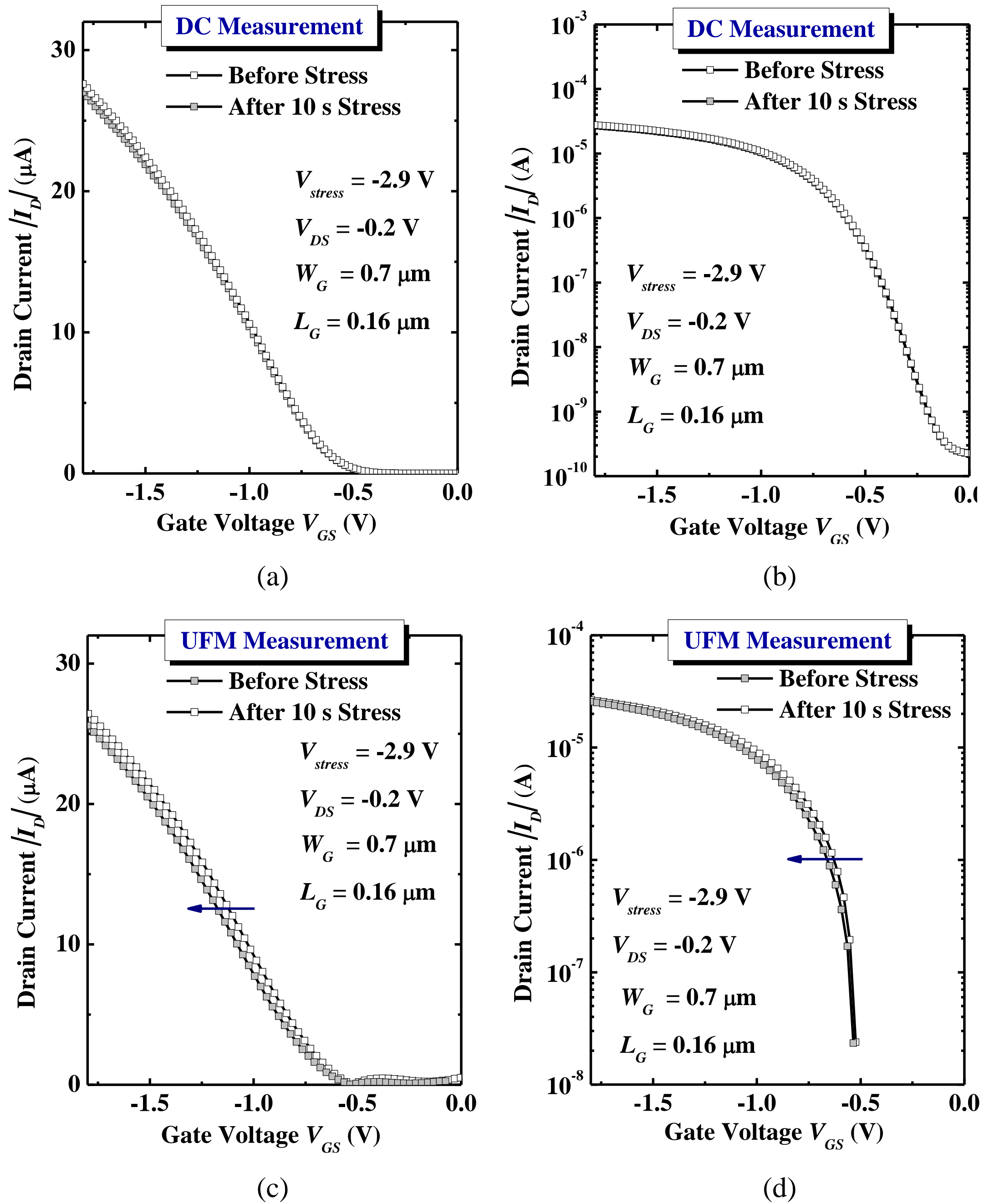


Fig. 3.7. $|I_D|$-V_{GS} characteristics in linear-linear scale of two Si p-FETs measured by (a) conventional DC measurement method and (c) UFM technique. (b) and (d) are the corresponding $|I_D|$-V_{GS} characteristics in log-linear scale.

capturing signals in the same order (μA) of magnitude. Signals in lower orders (<100 nA) of magnitude are largely contaminated by noise. Nevertheless, this limitation of UFM setup does not affect the NBTI results, as the threshold voltage can be extracted

using linear-linear plots and the extraction is hardly influenced by the current at low V_{GS}.

3.4.3 UFM NBTI Characterization of Strained and Unstrained p-FETs

Fig. 3.8 (a) shows fitted $|I_D|$-V_{GS} characteristics of strained and unstrained p-FETs measured at V_{DS} = -0.2 V before and after being stressed at V_{stress} = -2.9 V. All three transistors have the same gate length L_G of ~300 nm and gate width W_G of ~700 nm. The transistors were electrically stressed by the same gate stress voltage V_{stress} of -2.9 V, and characterized by UFM technique. $|I_D|$-V_{GS} curves before NBT stress and after 1000 s stress were shown for each p-FET. The V_{DS} of -0.2 V was selected to bias the transistors in the linear region and yet achieve a relatively large current (as compared with V_{DS} of -0.05 V or -0.1 V) for the oscilloscope to capture. The device with DLC liner stressor shows the highest $|I_D|$ among the three devices for a fixed V_{GS}, and p-FET with SiGe S/D has the second largest $|I_D|$.

All three devices show very visible threshold voltage shifts after V_{stress} of -2.9 V for 1000 s. The p-FET with DLC liner stressor experienced the largest V_{TH} shift (ΔV_{TH}) among the three transistors, while p-FET with SiGe S/D shows the second largest ΔV_{TH}. The $|I_D|$-V_{GS} plots of the three devices are shown separately in Fig. 3.8 (b) - (d) for clarity. At a fixed V_{GS} of -1.5 V, the p-FET with DLC liner stressor is shown to have a drain current I_D degradation of 12 % after being stressed for 1000s, while the p-FET with SiGe S/D and the control p-FET have I_D degradation of 11 % and 9 %, respectively.

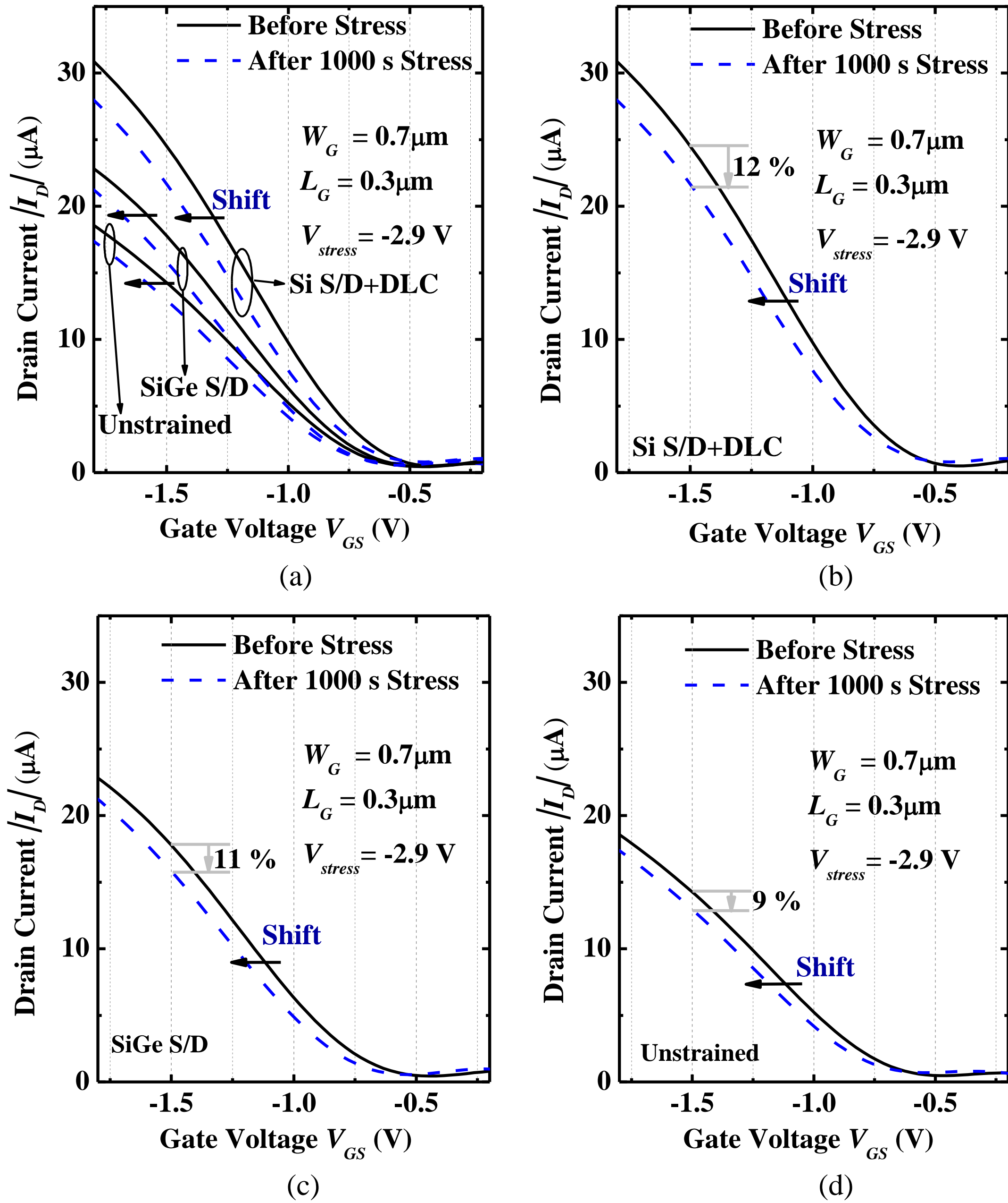


Fig. 3.8. (a) Consolidated $|I_D|$-V_{GS} characteristics of different devices before and after 1000 s NBT stress. V_{DS} = -0.2 V. $|I_D|$-V_{GS} curves of unstrained p-FET, p-FET with SiGe S/D, and p-FET with Si S/D and DLC liner are shown separately in (b), (c), and (d), respectively, for clear demonstration.

Fig. 3.9 shows transconductance G_M-V_{GS} plots for the control p-FET, p-FET with SiGe S/D, and p-FET with DLC high stress liner before any NBT stress. G_M is obtained by differentiating the $|I_D|$-V_{GS} curves with respect to V_{GS}, i.e. $G_M = dI_D/dV_{GS}$. P-FETs with DLC liner and SiGe S/D show 65 % and 27 % higher peak G_M,

respectively, as compared with the control, indicating substantial hole mobility enhancement due to strain in the channel.

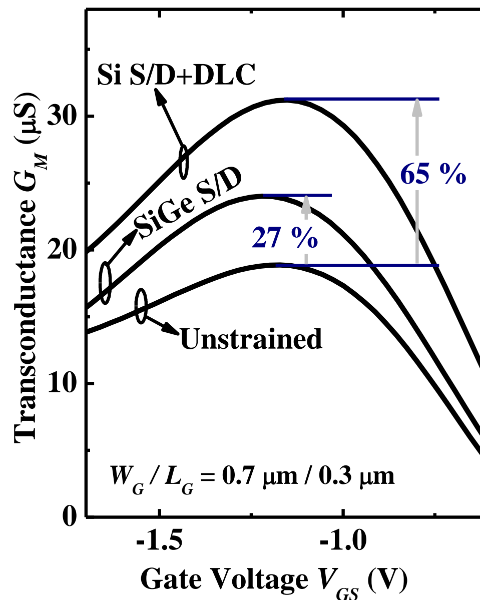


Fig. 3.9. Transconductance G_M versus V_{GS} plot for various p-FETs. P-FETs with DLC liner and SiGe S/D show 65 % and 27 % higher G_M, respectively, as compared with the control.

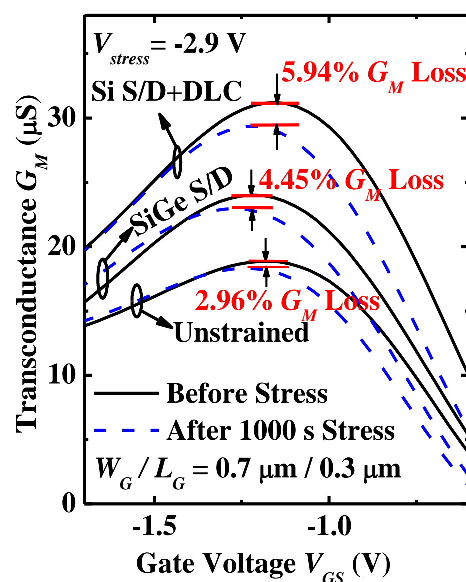


Fig. 3.10. G_M losses for various p-FETs after being stressed at V_{stress} = -2.9 V for 1000 s. G_M degradation is largest for the p-FET with Si S/D and DLC liner.

G_M losses caused by NBT stress at -2.9 V for 1000 s for all p-FETs are shown in Fig. 3.10. G_M losses of 5.94 %, 4.45%, and 2.96% were observed on p-FET with DLC liner, p-FET with SiGe S/D, and control p-FET, respectively. Device with a larger peak G_M or a larger channel strain suffers from a larger G_M loss after being stressed at the same voltage V_{stress} of -2.9 V. G_M degradations for a p-FET with DLC liner and a control p-FET, which were both stressed at V_{stress} of -2.5 V for 1000 s, are shown in Fig. 3.11. G_M degradations due to different NBT stress show consistent trend, namely p-FETs with DLC liner stressor have larger degradation when being stressed at the same V_{stress}, as compared with the controls. In addition, it is also observed that a lower V_{stress} leads to smaller NBT degradation.

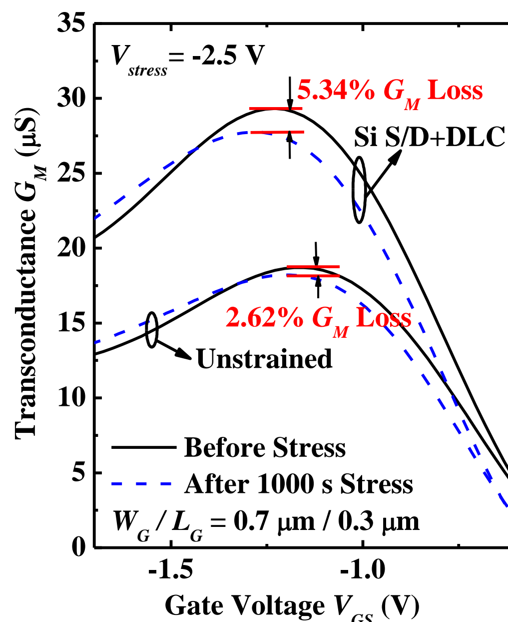


Fig. 3.11. G_M losses for various p-FETs after being stressed at V_{stress} = -2.5 V for 1000 s. G_M degradation is larger for the p-FET with Si S/D and DLC liner, as compared with the control. Comparing with G_M losses at V_{stress} = -2.9 V, G_M losses at V_{stress} = -2.5 V is smaller in terms of percentage for the same kind of device.

Fig. 3.12 compares ΔV_{TH} under different NBT stresses for the strained and unstrained p-FETs. V_{TH} degradation is the largest for p-FETs with DLC liner stressor, followed by p-FETs with SiGe S/D, and the trend is similar to that observed for $|I_D|$ and G_M losses in Fig. 3.8 to Fig. 3.11. It can be seen that a device with higher strain suffers from more severe NBTI degradation under the same gate stress V_{stress}. Several research groups had similar observations on their strained devices characterized with different NBTI measurement techniques, including conventional DC measurement, on-the-fly IV measurement, and charge pumping [23, 36, 37, 39-44]. Devices in these publications include Si p-FETs with SiGe S/D, biaxially strained SOI p-FETs, and p-FETs with SiN liner stressor.

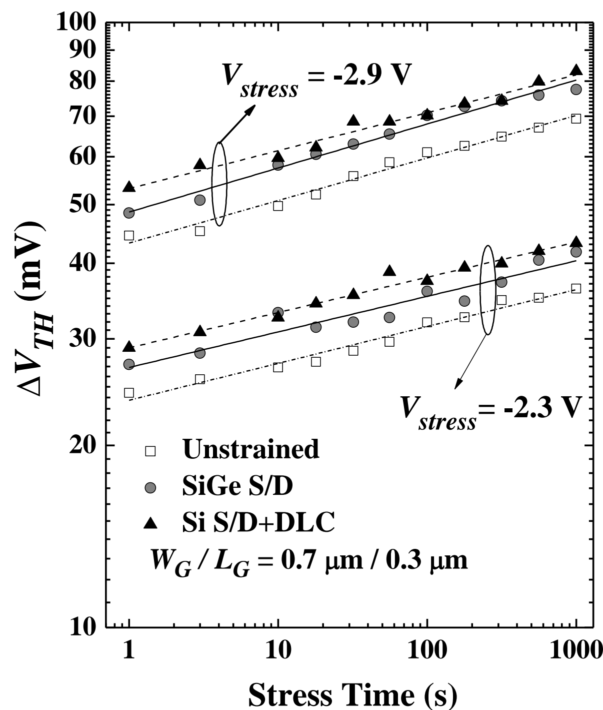


Fig. 3.12. V_{TH} shift as a function of stress time for various p-FETs. For the same NBT stress voltage V_{stress}, V_{TH} shift is larger for a p-FET with a higher strain or I_{on}. P-FETs in order of increasing I_{on} performance and ΔV_{TH} due to NBTI stress are unstrained p-FET, p-FET with SiGe S/D, and p-FET with Si S/D and DLC liner. For the p-FET with Si S/D and DLC liner, the time exponent for ΔV_{TH} varies from 0.063 to 0.058 when V_{stress} varies from -2.9 V to -2.3 V.

Next, a few plausible explanations will be discussed for the observed strain enhanced NBTI degradation. Several groups that studied NBTI of p-FETs with compressive SiN stress liner have attributed the enhanced NBTI degradation partially or fully to the high hydrogen (H) content in the SiN film [37, 132, 133]. The high H content could passivate the Si dangling bond at Si-SiO_2 interface by forming Si-H bonds, leading to better initial interface before NBT stress. These Si-H bonds, however, can easily be broken upon electrical stress, resulting in more V_{TH} shift. In this work, this factor most probably can be ruled out, as neither the DLC deposition process using FCVA system nor the SiGe S/D growth introduces additional Si-H bonds for the strained p-FETs. It could be assumed that the H contents across all the three device splits are about the same.

The high compressive strain induced by either SiGe S/D or DLC liner stressor could lead to more oxide traps at the Si-SiO_2 interface, as compared with the unstrained p-FETs [44]. The possibly more "preexisting" oxide traps of strain devices may enhance the NBTI degradation process by trapping more holes when the transistors are being stressed, as suggested by Y.-T. Chen *et. al.* in Ref. [44]. This will result in more V_{TH} shift. The significant amount of V_{TH} shift due to hole trapping to the oxide traps can be captured by UFM.

The channel strain dependence of NBTI degradation observed could suggest yet another possibility, in addition to the one mentioned above. It is possible that Si-H bond energy at the Si-SiO_2 interface decreases with strain, as suggested in a few publications [36, 37, 39, 134]. This makes Si-H bonds in a strained device easier to break upon electrical stress. The breaking of Si-H bonds could result in more interface trap generation, and possibly more hole trapping. The larger G_M degradation

of p-FETs with higher strain observed in this work suggests that interface trap generation in p-FETs with higher strain is higher, consistent with the model suggested in Ref. [36, 37, 39, 134].

It should be noted that the slight worse NBTI performance of strained p-FETs cannot hinder the application of strain engineering as an important performance booster. Careful consideration of the trade-off between performance enhancement and reliability degradation would result in devices with good drive current performance and acceptable NBTI performance.

Power law slopes found in this work are in the range of ~0.058 to ~0.072, which is not in the range of 0.16 - 0.25 predicted by conventional Reaction-Diffusion (R-D) model of NBTI degradation. The results, however, are consistent with the two-component NBTI model [32]. M.-F. Li *et al.* demonstrated that V_{TH} degradation under NBT stress is contributed by two components, a ΔV_{TH}^{ox} component caused by oxide charge trapping, and a ΔV_{TH}^{it} component due to interface trap generation [32]. The former component has a power law slope of ~0.05, and the later has a slope of ~0.16. Oxide charge trapping is believed to only be captured by fast measurement. In addition, longer measurement time $T_{measure}$ in UFM normally lead to larger power law slops [29, 126]. The net effect of the two components is the smaller power law exponents (less than or close to 0.1) observed in this work and some of the other fast measurement studies [29, 126-128, 135].

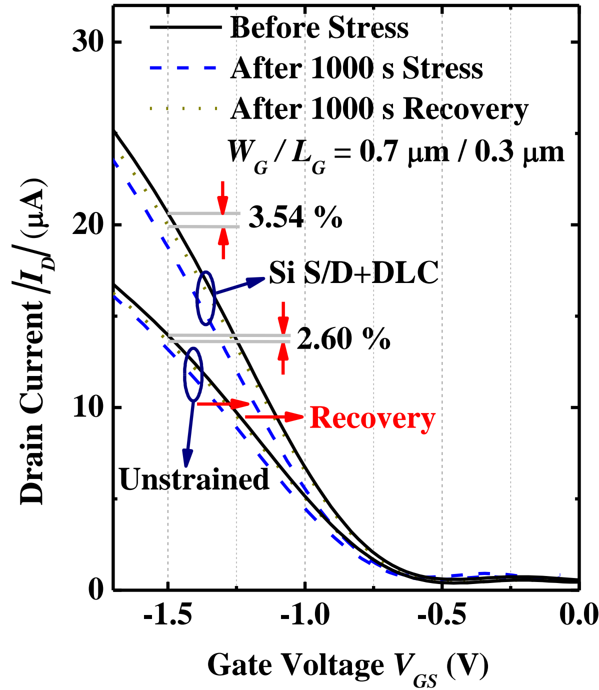


Fig. 3.13. $|I_D|$–V_{GS} recovery of unstrained p-FET and p-FET with Si S/D and DLC liner, after V_{stress} of -2.5 V was removed. Visible recovery of threshold voltage and $|I_D|$ recoveries were observed on both devices.

3.4.4 Recovery of NBTI

Recovery of NBTI of different devices will be discussed in this Section. Fig. 3.13 shows $|I_D|$-V_{GS} characteristics of unstrained p-FET and p-FET with DLC liner after 1000 s NBT stress at V_{stress} = -2.5 V (blue curves) and after 1000 s of removal of the NBT stress (dark yellow curves). These are the same two devices shown in Fig. 3.11. During the recovery phase, no V_{stress} was applied to the gate electrode. The devices were just characterized at certain time point during the 1000 s recovery period. Substantial V_{TH} recoveries were observed on both of the transistors. $|I_D|$ at a fixed V_{GS} also recovers after removal of the NBT stress. The device with strain shows larger amount of V_{TH} recovery. However, p-FET with DLC liner still has a slightly larger $|I_D|$ degradation (3.54%) with respect to the original value at V_{GS} = -1.5 V, even after the 1000 s recovery. A 2.6 % $|I_D|$ degradation was observed for control p-FET.

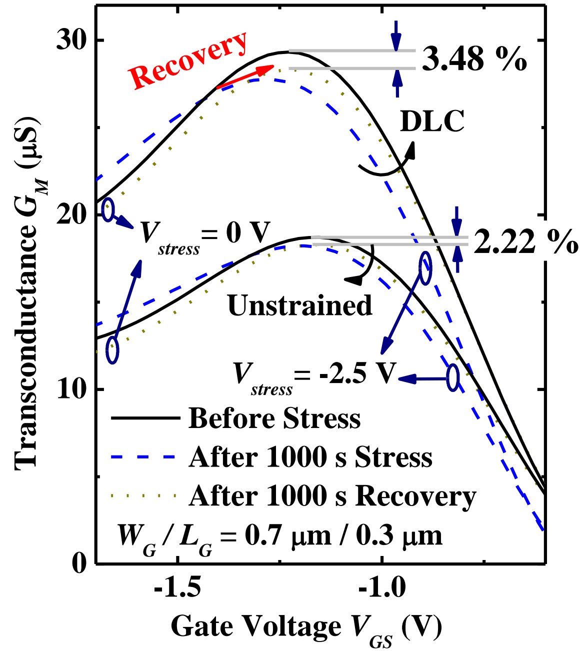


Fig. 3.14. G_M recovery after being stress at -2.5 V for 1000 s for unstrained control p-FET and p-FET with DLC liner. The results are consistent with drain current recovery.

The G_M recoveries of the same two transistors are shown in Fig. 3.14. The G_M-V_{GS} curves after 1000 s removal of NBT stress were compared with the G_M-V_{GS} plots before stress and after 1000 s stress. The p-FET with DLC liner which suffered from more G_M degradation during stress phase still shows larger G_M loss with respect to the value before stress after 1000 s recovery. This could be an indication of the degraded interface of the strained p-FET.

Fig. 3.15 tracks the ΔV_{TH} during a 1000 s stress phase and during a subsequent recovery phase where stress was removed. It is observed that G_M recovery takes place right after the stress is removed for both unstrained p-FET and p-FET with DLC liner. The recovery rate observed in this work is significant, and may be due to several factors. First, the UFM technique gives a higher ΔV_{TH} than that obtained by the DC

measurement technique at the end of the stress phase, and ΔV_{TH} values in recovery phase are comparable using either technique, thus leading to a higher V_{TH} recovery rate during the recovery phase as observed using UFM. Secondly, the V_{TH} recovery rate also increases with decreasing nitrogen content in the gate oxide or with lower NBT measurement temperature [131, 136, 137]. The thermal oxide without any nitrogen gate dielectric used in this work could be another reason for the high recovery rate.

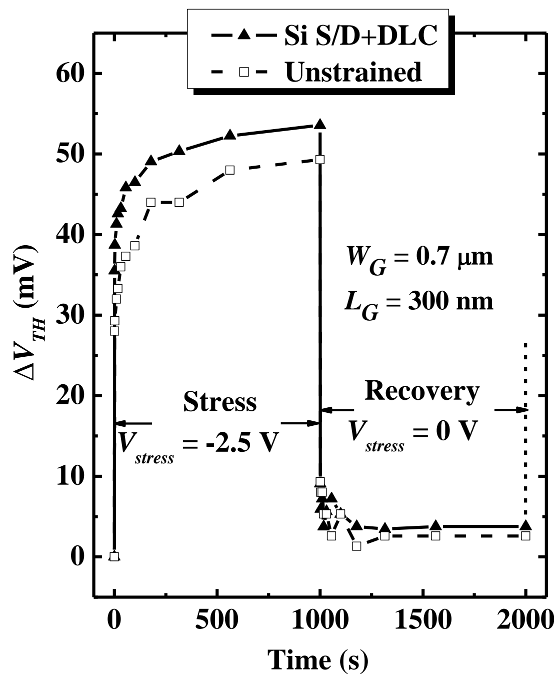


Fig. 3.15. ΔV_{TH} in stress phase (V_{stress} = -2.5 V) and recovery phase. ~80% of ΔV_{TH} recovers within 1 s after the stress is removed, suggesting that traditional DC measurement underestimates the V_{TH} shift.

3.4.5 Gate length dependence of NBTI

Gate length L_G dependence of ΔV_{TH} for both strained and unstrained devices was observed (Fig. 3.16). Generally, threshold voltage before NBT stress (*i.e.* at $t = 0$ s) decreases as gate length decreases, for both strained and unstrained p-FETs. For unstrained p-FETs, ΔV_{TH} decreases when L_G increases from 200 nm to 550 nm. This is consistent with previous studies with regard to L_G dependence of V_{TH} shift in unstrained devices [138, 139]. The more severe degradation near the gate edge and the gate-S/D overlap region, as compared with the channel region, was proposed to be the reason for the observed gate length dependence of NBTI degradation [138, 139]. The gate etch process and S/D implantation experience by the device may lead to more damages near the gate edge and the gate-S/D overlap region, and in turn more severe NBTI degradation.

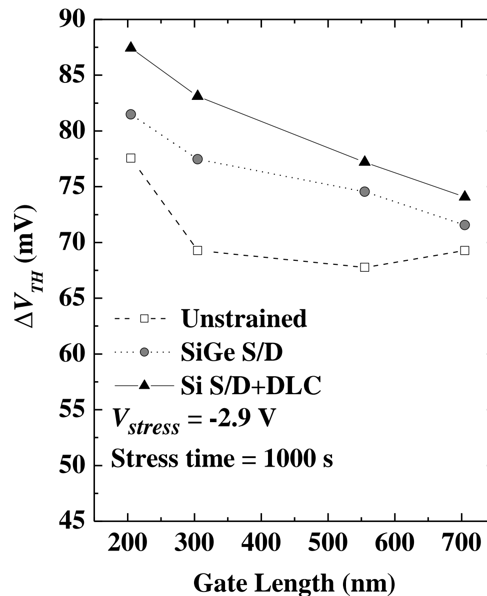


Fig. 3.16. Gate length L_G dependence of ΔV_{TH} for strained and unstrained p-FETs. ΔV_{TH} generally increases with decreasing L_G for strained p-FETs.

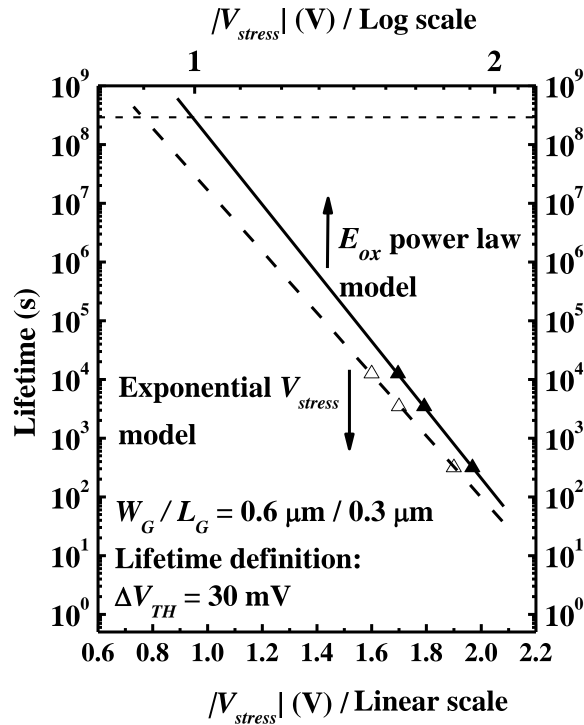


Fig. 3.17. NBTI lifetime projection of strained p-FET with Si S/D and DLC liner, showing that it has a lifetime of 10 years at V_G = -0.99 V using E_{ox} power law model. The exponential V_{stress} model suggests a lifetime of 10 years at V_G = -0.76 V.

For strained devices, ΔV_{TH} always decreases with increasing L_G from 200 nm to 700 nm. The decrease of channel strain caused by increase of L_G may be one of the factors that lead to this NBTI gate length dependence of strained devices observed in this work. It should be noted that smaller L_G devices actually experience larger oxide field when stress at the same V_{stress}, as compared with the longer channel devices. This could contribute to the larger ΔV_{TH} observed on small L_G devices.

3.4.6 NBTI Lifetime Projection for p-FETs with DLC liner

The lifetimes of p-FETs with Si S/D and DLC liner are evaluated using the E_{ox} power law model and exponential V_{stress} model [140, 141]. Fig. 3.17 shows that the NBTI lifetime of strained p-FETs at V_G = -0.99 V has a lifetime of 10-years using E_{ox}

power law model. The exponential V_{stress} model, on the other hand, suggests a lifetime of 10 years at V_G = -0.76 V. UFM measurement performed in this study examines the worst case of NBTI degradation because the DC NBT stresses were applied on p-FETs. NBTI degradation was demonstrated to be less under dynamic stress which is closer to the circuit operating condition, as compared with DC stress [127]. Therefore, under more realistic operating conditions, the device lifetime of p-FETs with DLC liner would probably be much better than the prediction performed here. Note, however, that a relatively thick SiO_2 gate dielectric (~ 3 nm) was used in this study, and further NBTI evaluation using state-of-the-art gate dielectric with lower equivalent SiO_2 thickness would be needed.

3.5 Summary

In this Chapter, a modified UFM setup employing the DHPCA-100 amplifier for NBTI characterization was introduced. Detailed measurement setup was discussed. NBTI data collected by conventional DC measurement and UFM technique were compared, demonstrating that the UFM technique could capture the fast V_{TH} degradation component due to hole trapping. NBTI of p-FETs with DLC liner having ultra-high compressive stress was investigated for the first time using the UFM technique. Under the same NBT stress V_{stress}, larger ΔV_{TH} and drain current and transconductance loss were observed for p-FETs with a higher channel strain. Possible explanations were discussed. Power law exponents ranging from ~0.058 to ~0.072 were observed in this work. Recovery behaviors of drain current and transconductance were shown. Channel length dependence of NBT degradation was discussed. NBTI lifetime was extrapolated using both E_{ox} power law model and exponential V_{stress} model for strained p-FETs with DLC liner stressor.

Chapter 4

High Performance Multiple-Gate Field-Effect Transistors formed on Germanium-on-Insulator Substrate

4.1 Background

Besides strain engineering, which has been used as an effective performance booster for silicon (Si) based complementary metal-oxide-semiconductor (CMOS) as discussed in Chapter 2 and 3, adoption of new channel materials is expected for future advanced technology nodes. As scaling of CMOS enters the sub-20 nm regime, carrier transport in the transistor is quasi-ballistic and the drive current will be ultimately limited by the injection velocity [45, 46], instead of the saturation velocity in the case of long channel devices. The injection velocity is experimentally found to be proportional to low field mobility [47]. Therefore, high mobility channel material is desirable for future low voltage and high speed CMOS application. Germanium (Ge) is considered as one of the most promising channel materials to replace Si in future CMOS applications due to its high carrier mobilities, especially hole mobility [53, 54, 142-147].

Starting from the 22 nm technology node, silicon (Si) channel Multiple-Gate Field-Effect Transistors (MuGFETs) or FinFETs have been used for high volume CMOS production, as the additional gates provide improved short channel control for extremely scaled devices [65-67]. High mobility Ge channel FET with multi-gate

structure [72-79] could be adopted to achieve high drive current and good short channel control at sub-20 nm technology nodes. Germanium-on-Insulator (GeOI) substrate is a good platform for realizing high performance Ge MuGFETs [148]. Although Ge planar FETs have been studied, integration of 3D Ge MuGFETs with high-κ metal gate on GeOI substrate is not well explored or developed yet.

Before the first Ge FinFET or MuGFET was fabricated by top-down fabrication approach which is more compatible with existing CMOS manufacturing process, Ge MuGFETs or nanowire FETs were fabricated by various research groups by bottom-up approaches [71-73]. Two of the most popular bottom-up methods to form Ge nanowire are "supercritical fluid-liquid-solid (SFLS)" technique and "vapour-liquid-solid (VLS)" technique (also called "chemical vapour deposition (CVD)" technique) [149]. These bottom-up approaches not only yield extremely scaled Ge nanowires with wire diameters down to a few tens of nanometres (nm), but also avoid etch damages to the Ge surface. Ge nanowire FETs with good performance were achieved by D. Wang *et. al.* [71] and L. Zhang *et. al.* [72] of Stanford University, J. Xiang *et. al.* of Harvard University [73], and T. Burchhart *et. al.* of Vienna University of Technology [150].

Despite the good results achieved for Ge nanowire FETs made by bottom-up techniques, there is still a strong need to develop Ge MuGFETs using top-down approaches. Bottom-up techniques face great manufacturing challenges for now and it is difficult to fabricate a large number of Ge MuGFETs with the state of the art bottom-up approaches. Top-down fabrication approaches are more compatible with the existing CMOS manufacturing processes.

The first Ge FinFET fabricated by top-down approach was by J. Feng *et. al.* of Stanford University in year 2007 [74], almost 9 years after Si FinFETs were demonstrated [66]. Due to the very large fin and unoptimized gate stack, the control of short-channel effects and drive current of this device are not good. A few more papers were published on Ge FinFETs or MuGFETs in recent years [75], including Gate-All-Around (GAA) FETs [76-78] and Ge MOSFETs with curved channel surface [79]. Compared with the very well developed and highly manufacturable Si FinFET process, process development of Ge MuGFETs falls much behind. There is a strong need to further advance the current Ge MuGFET technology.

MuGFET or FinFET structures employing aggressively scaled fin dimensions may suffer from high series resistance due to the small contact area of source/drain (S/D) region. Schottky Barrier (SB) metallic S/D structure was proposed to be used to reduce S/D series resistance [69],[70]. The benefits of metallic S/D of a SBMOSFET include low parasitic resistance, low process temperature, abrupt junction, and high frequency response [69],[70].

In this work, we report omega-gate (Ω-gate) MuGFETs formed on GeOI substrates, featuring low temperature disilane Si_2H_6 passivated channel, high-k gate dielectric and metal gate stack, and self-aligned metallic Schottky-Barrier (SB) nickel germanide (NiGe) source/drain (S/D). This was the first Ge SB MuGFET with metallic NiGe S/D when we reported the results in October 2012 [151]. Detailed process integration will be discussed in this Chapter. High performance multiple-gate Ge transistors are fabricated using Si CMOS compatible process modules developed in this work. On-state current (I_{ON}), transconductance (G_M), drain induced barrier

lowering (DIBL), and subthreshold swing (SS) are reported. The effects of fin doping on Ge MuGFET performance is also investigated.

4.2 Operation of Schottky Barrier MOSFET (SBMOSFET)

In a SBMOSFET [Fig. 4.1 (a)], the source and drain are made of metal, instead of doped semiconductor as in a conventional MOSFET [Fig. 4.1 (b)]. The operation of a SBMOSFET is different as compared with a conventional MOSFET with doped S/D. In this Section, the operation principle of SBMOSFET will be briefly discussed.

Fig. 4.2 (a) - (d) show band diagrams of p-channel SBMOSFET under different bias conditions. When gate voltage $V_{GS} = 0$ V, and drain voltage $|V_{DS}| > 0$V, electron would travel from drain to source by tunneling through two barriers [as illustrated by Fig. 4.2 (b)], resulting in reverse leakage current. When device operates at subthreshold regime ($|V_{GS}| < |V_{TH}|$, $|V_{DS}| > 0$V), hole will be emitted into channel via thermionic emission, contributing to current flow. Further increasing $|V_{GS}|$ above $|V_{TH}|$ [as shown in Fig. 4.2 (d)] will make the device operate at on-state. More holes are injected into channel via thermionic, thermionic-field, and field emissions into the

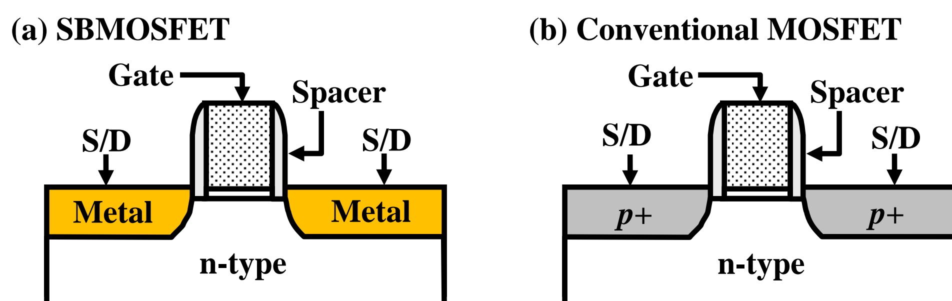


Fig. 4.1. Device schematics of (a) SBMOSFET, and (b) conventional MOSFET.

channel from the metal source at this state. Field emission could take place when the valence band of the semiconductor channel is lifted above the quasi-Fermi level of metal source.

Fabrication of p-channel SBMOSFET does not need any S/D implantation and dopant activation processes, which simplifies device fabrication and saves process cost. In addition, elimination of dopant activation process also reduces the thermal budget experienced by the gate stack, avoiding any possible gate stack degradation due to high temperature annealing. This is especially important for Ge devices, as gate stack on Ge substrate could be easily degraded by high temperature annealing due to either dielectric (e.g., GeO_2) degradation or Ge out diffusion. More importantly, replacing doped semiconductor (normally Si or Ge) with metal (typically metal silicide) could also lead to series resistance reduction (due to low resistance of metal) and abrupt metal-semiconductor junction [69, 152]. Achieving low series resistance is important to achieve high drive current in FinFETs or nanowire FETs.

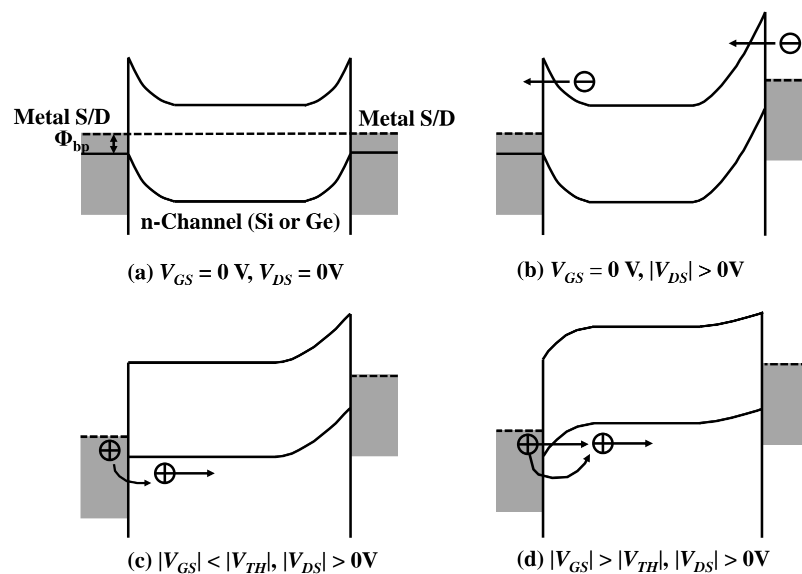


Fig. 4.2. Operation of a SBMOSFET. (a) $V_{GS} = 0$ V, $V_{DS} = 0$V; (b) $V_{GS} = 0$ V, $|V_{DS}| > 0$V; (c) $|V_{GS}| < |V_{TH}|$, $|V_{DS}| > 0$V; (d) $|V_{GS}| > V_{TH}$, $|V_{DS}| > 0$V.

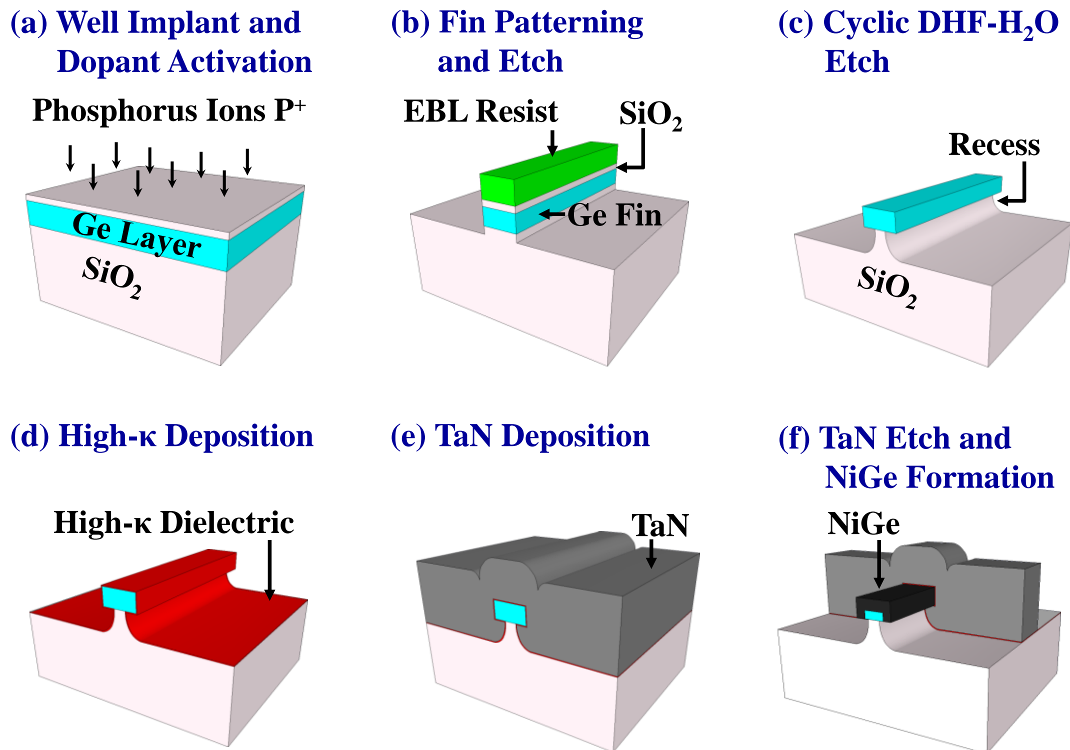
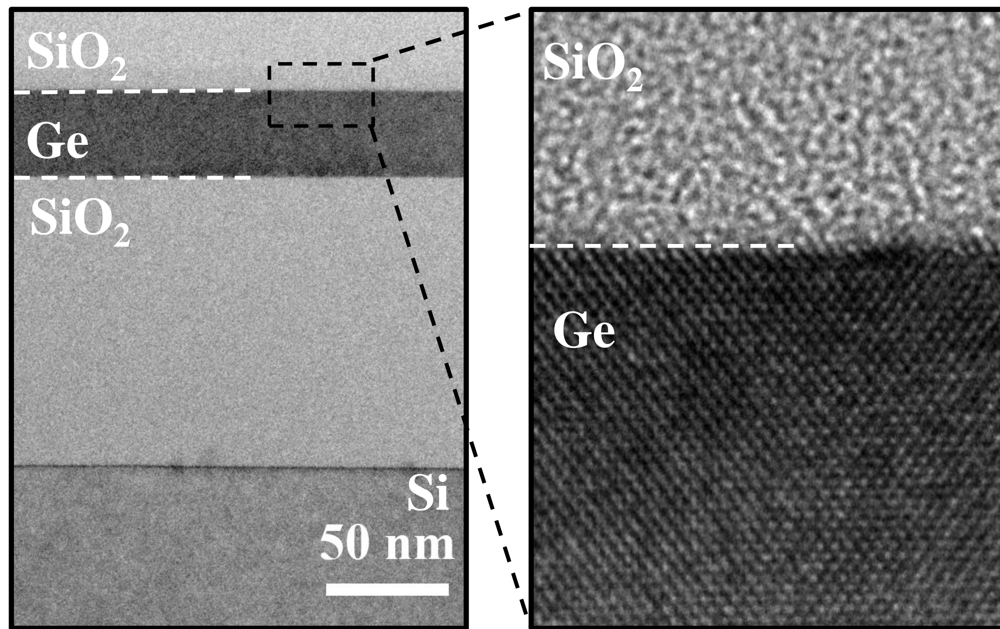


Fig. 4.3. 3D schematics demonstrating key process steps to fabricate Ge MuGFETs on GeOI substrate. (a) N-well implant and dopant activation; (b) Fin patterning and etch; (c) Cyclic DHF-H_2O etch; (d) High-k deposition; (e) TaN deposition; (f) TaN etch and NiGe formation.

4.3 Device Fabrication

Fig. 4.3 shows the 3D schematics illustrating the key process steps used to fabricate Ge MuGFETs. The corresponding device structure formed after each of the key process steps is shown. Fig. 4.3 (a) - (f) correspond to (a) n-well implant and dopant activation, (b) fin patterning and etch, (c) cyclic dilute hydrofluoric acid DHF-H_2O etch, (d) high-κ deposition, (e) TaN deposition, and (f) TaN etch and NiGe formation.

High quality GeOI samples were formed by SmartCut™ technology, and used as starting substrates. A zoomed-out Transmission Electron Microscopy (TEM) image of GeOI used is shown in Fig. 4.4 (a). Fig. 4.4 (b) shows a high resolution TEM (HRTEM) of the GeOI substrate, demonstrating good Ge crystalline quality.



(a) (b)

Fig. 4.4. (a) Zoomed-out TEM of high quality GeOI wafer used in this work. (b) HRTEM of the GeOI substrate, demonstrating good Ge crystalline quality.

4.3.1 N-channel Formation

After depositing a 10 nm SiO_2 capping layer, phosphorus (P) well implant was performed to dope the Ge layer n-type [as shown in Fig. 4.3 (a)]. Two different P doses (8×10^{12} cm^{-2} and 1.6×10^{13} cm^{-2}) were used on separate samples to study the effect of well or fin doping concentration on the electrical performance of Ge MuGFETs. Devices with P dose of 8×10^{12} cm^{-2} and 1.6×10^{13} cm^{-2} will be referred to as "device with low fin doping" and "device with high fin doping", respectively. The same implant energy of 30 keV was used for both of the implant splits. Based on the Stopping and Range of Ions in Matter (SRIM) [153] simulation results shown in Fig. 4.5, the whole Ge layer will receive P implant and become n-type. The dopants were activated using a 600 ℃ 60 s anneal in a Rapid Thermal Processing (RTP) system [154].

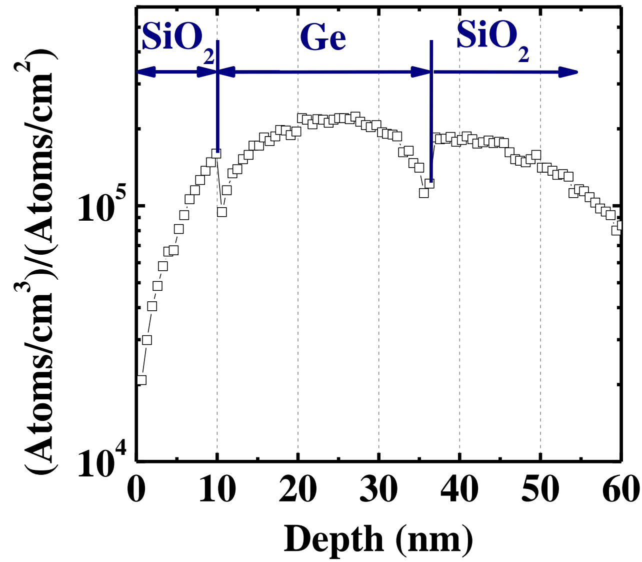


Fig. 4.5. SRIM simulation of as implanted P profile with an implant energy of 30 keV. GeOI sample surface was protected with a 10 nm SiO_2 layer during implantation.

Time-of-Flight Secondary Ion Mass Spectrometry (TOF SIMS) analyses were performed on two blanket GeOI samples with a P doses of 8×10^{12} cm^{-2} and 1.4×10^{13} cm^{-2} and dopant activation at 600 ℃ for 60 s, and results are shown in Fig. 4.6. A sample with P implant dose of 1.4×10^{13} cm^{-2}, instead of 1.6×10^{13} cm^{-2}, was used for SIMS analysis, as all samples with P dose of 1.6×10^{13} cm^{-2} were used for device fabrication. Due to low P concentrations, P signals are at noise level in Ge layers of both of the samples. GeP signals which could reflect P concentrations are shown for both samples (Fig. 4.6). Based on the SIMS intensity, it could be observed that P concentration in the sample with a P dose of 1.4×10^{13} cm^{-2} is visibly higher than the one with a P doses of 8×10^{12} cm^{-2}. It was also observed that P has a box-like profile after being activated at 600 ℃ for 60 s.

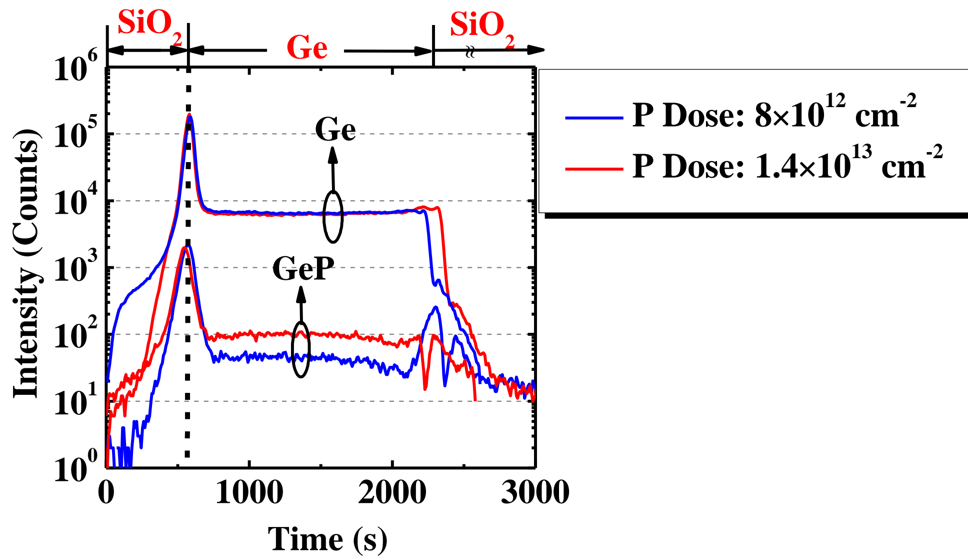


Fig. 4.6. SIMS analyses on two GeOI samples with P doses of 8×10^{12} cm^{-2} and 1.4×10^{13} cm^{-2}. A sample with P implant dose of 1.4×10^{13} cm^{-2} instead of 1.6×10^{13} cm^{-2} was used for SIMS analysis, as all sample with P dose of 1.6×10^{13} cm^{-2} was used for device fabrication.

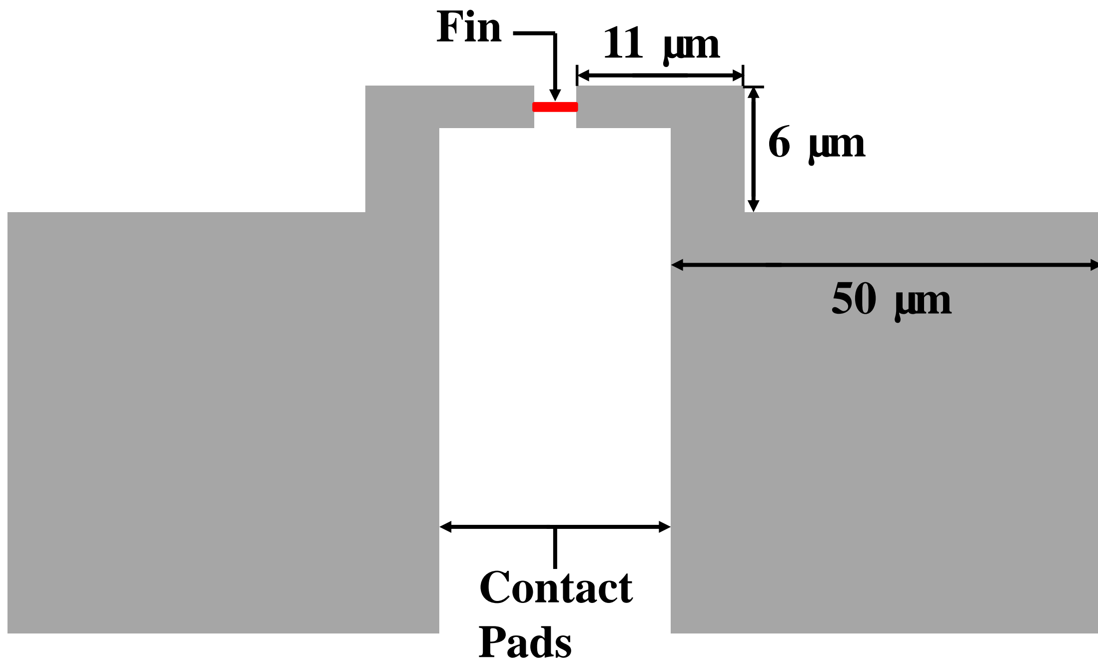


Fig. 4.7. Layout of the Ge active region used for EBL. The layout was divided into two different layers, “”fin layer” and “contact pads” layer, during EBL definition. EBL doses were optimized for these two layers so that optimum accuracy is achieved for the fin layer, while maximum writing speed is achieved for the contact pads layer.

4.3.2 Ge Fin Formation

After n-well formation, Ge fins were defined by electron beam lithography (EBL) and dry-etched using chlorine-based plasma chemistry [Fig. 4.3 (b)]. Due to low throughput of EBL, different EBL doses were used for Ge fin definition and for contact pads definition, so that the shape of the fins was very well defined with great accuracy and the big contact pads were completed in the shortest time possible, as illustrated by Fig. 4.7. The fin etch was performed using a Lam etcher. The source power and substrate bias used in etch process were optimized to have controllable etch rate and vertical Ge sidewall profile. A cross-sectional SEM image of a Ge fin test structure right after fin etch and resist stripping in oxygen plasma is shown in Fig. 4.8.

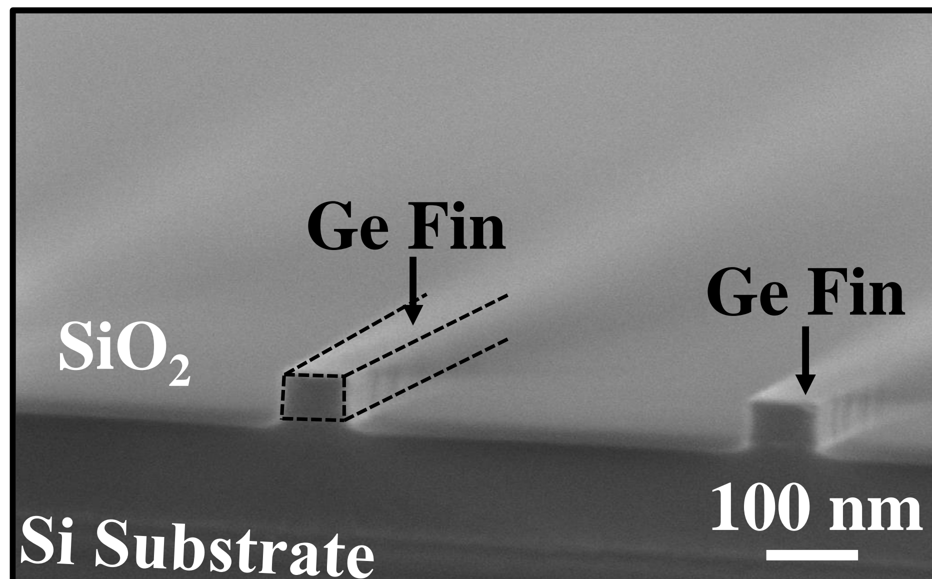


Fig. 4.8. Cross-sectional SEM image of a Ge fin test structure right after fin etch. The EBL resist was removed by oxygen plasma in an asher tool.

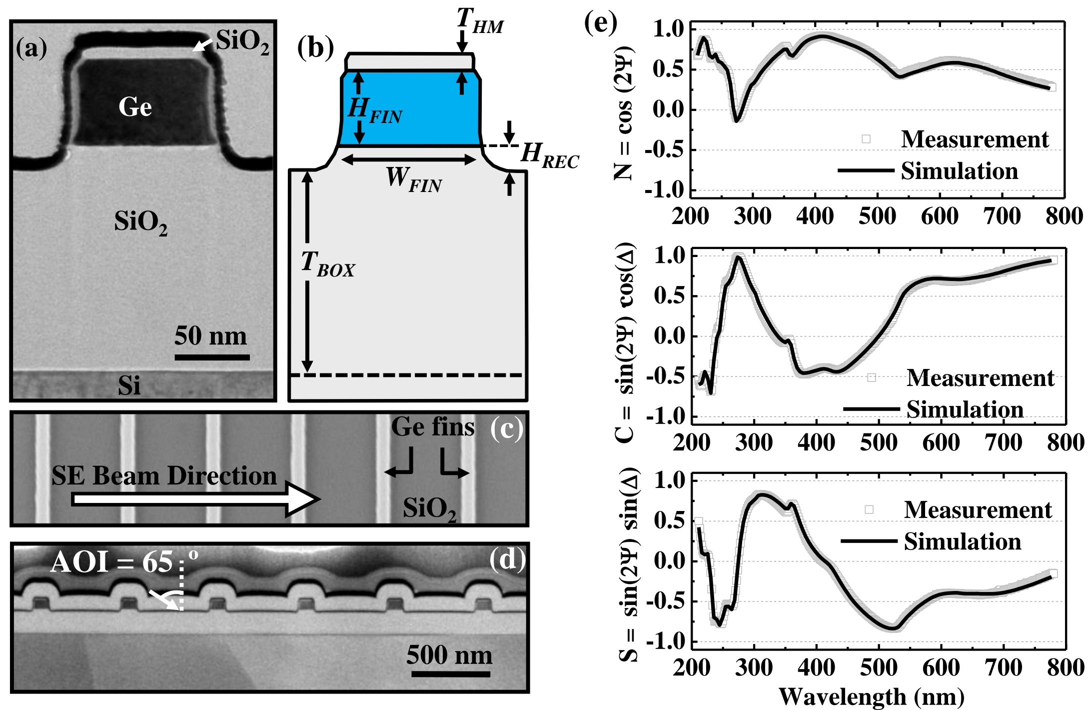


Fig. 4.9. (a) TEM image showing the cross-section of a Ge fin test structure. (b) Schematic illustrating five key floating or fitting parameters in the OCD model. These parameters are useful for monitoring key process variations. (c) SEM top view of the periodic grating of the Ge fin structure used in the OCD analysis. SE beam was oriented perpendicular to the Ge fin during data collection. (d) Zoomed-out cross-sessional TEM image of the OCD test structure. (e) Comparison of measured (symbols) and simulated (lines) $N(\Psi)$, $C(\Psi, \Delta)$, and $S(\Psi, \Delta)$ spectroscopic spectra, where Ψ is the angle whose tangent is the ratio of the magnitudes of the total reflection coefficients, and Δ is the change in phase difference between s-polarization and p-polarization before and after reflection from the sample [155]. Excellent spectral fitting was achieved.

4.3.3 OCD Characterization of Ge Fins

Non-destructive in-line characterization of Critical Dimension (CD) and profile of the Ge fin structure was performed by scatterometry Optical CD (OCD) measurement in Nanometrics Inc. in USA. The OCD characterization was done in collaboration with Nanometrics, and this is the first time that the non-destructive OCD technique was used to characterize Ge fins.

TEM was used to examine the cross-section of a Ge fin test structure [Fig. 4.9 (a)]. A schematic in Fig. 4.9 (b) illustrates the key parameters of interest in the OCD model to monitor key process variations. The five floating or fitting parameters include fin width (W_{FIN}), fin height (H_{FIN}), buried oxide thickness (T_{BOX}), oxide recess height (H_{REC}), and hardmask thickness (T_{HM}). The OCD measurement was carried out by spectroscopic ellipsometry (SE), with the propagation of optical beam oriented perpendicular to the periodic Ge fin grating structure, as shown in Fig. 4.9 (c). The Angle of Incident (AOI) is 65 °, as indicated in Fig. 4.9 (d). A zoomed-out cross-sessional TEM image of the Ge fin test structure is shown in Fig. 4.9 (d). Fig. 4.9 (e) shows the measured (symbols) and best fitted (lines) spectra simulated from Rigorous Coupled Wave Analysis (RCWA) and adjustment of model parameters [156].

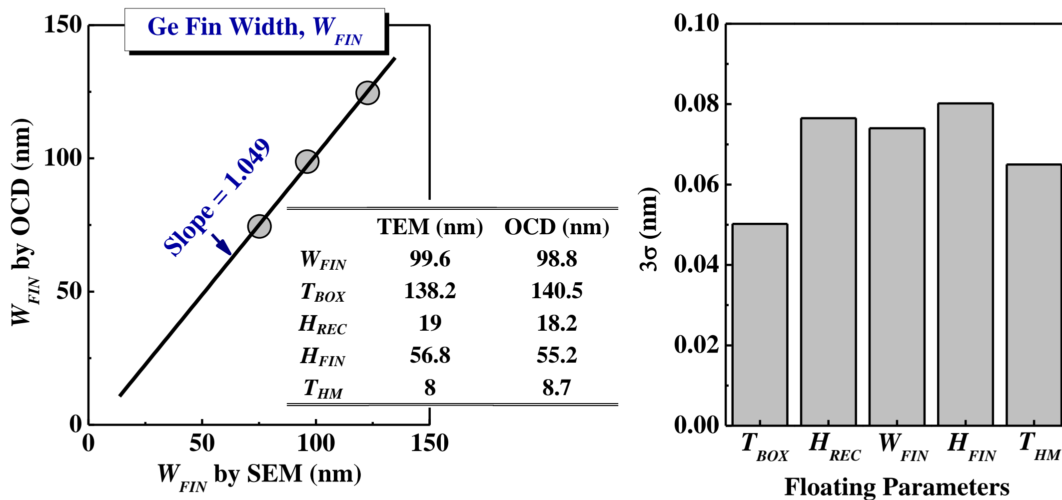
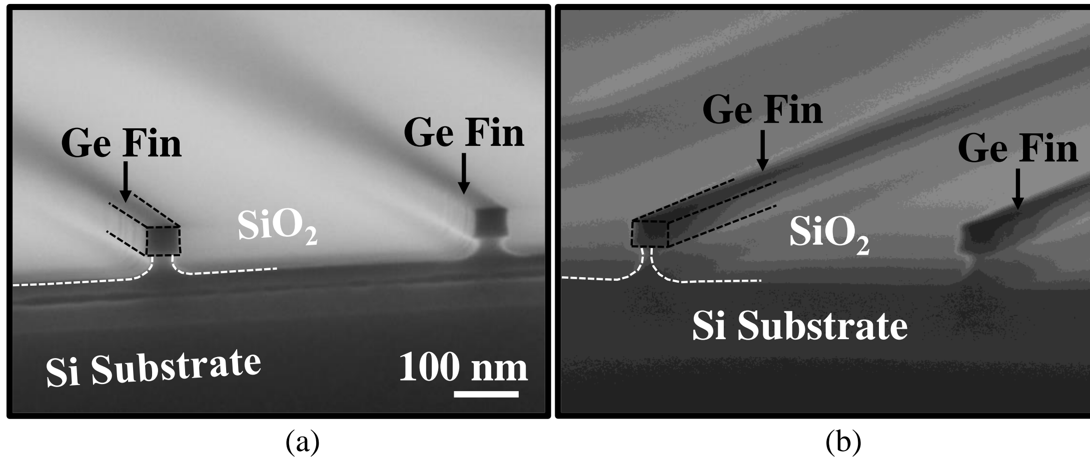


Fig. 4.10. (a) The correlation of fin width measured by OCD and by SEM is excellent with Coefficient of Determination, R^2 of 0.997 and slope of 1.049. In addition, OCD parameters were also compared with those obtained by TEM analysis, and a good match was achieved. (b) Ten independent OCD measurements were performed on the same site, and the 5 OCD parameters (T_{BOX}, H_{REC}, W_{FIN}, H_{FIN}, T_{HM}) were extracted. σ is the standard deviation of each OCD parameter obtained from the measurements. A low 3σ for all floating parameters indicates the good static precision or repeatability of the OCD characterization.



(a) (b)

Fig. 4.11. (a) Cross-sectional SEM image of a Ge fin test structure after fin etch and 150s DHF (1:50):DIW cyclic etch. The encroachment of SiO_2 layer can be clearly seen. (b) Cross-sectional SEM image of a Ge fin test structure after fin etch and longer DHF:DIW etch (270 s), as compared with that used in Fig. 4.11 (a). More encroachment of SiO_2 layer was achieved.

Fig. 4.10 (a) reveals excellent correlation on fin width between OCD and SEM. Coefficient of Determination, R^2 of 0.997 and slope of 1.049 were obtained. All other parameters from OCD also match well with those from TEM [inset of Fig. 4.10 (a)]. Excellent static precision, with 3σ lower than 0.1 nm (σ is the standard deviation of each OCD parameter obtained from the measurements), was achieved in all parameters, as shown in Fig. 4.10 (b).

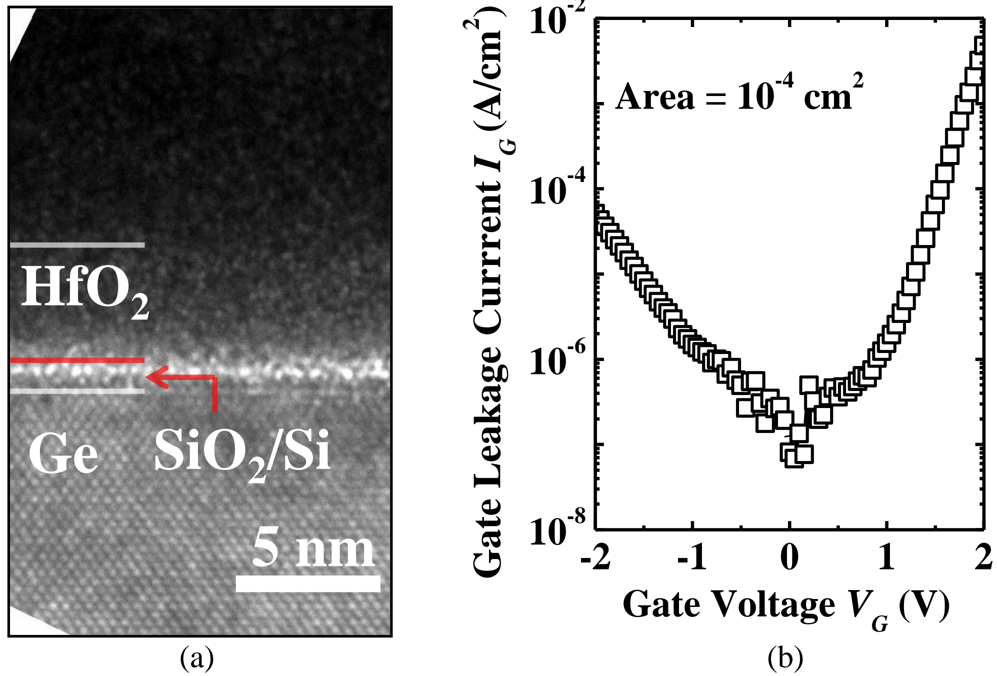
4.3.4 Formation of SiO_2 Undercuts

After formation of Ge fins, a cyclic dilute hydrofluoric acid (DHF) and deionized water (DIW) clean was performed to remove native oxide and to undercut the SiO_2 beneath the Ge fin. The rinse time in DHF or DIW was 15 s and the total clean time was 150 s. The undercut step enables the formation of a Ω-shaped metal gate, as illustrated in Fig. 1 (c). Fig. 4.11 (a) shows a cross-sectional SEM image of a Ge fin test structure after fin etch and DHF clean. SiO_2 undercut can clearly be

observed. A longer dip time in DHF could lead to more encroachment of SiO_2 layer, as shown in Fig. 4.11 (b). Gate-all-around (GAA) structure could be fabricated by dipping the sample for even a longer time to remove completely the SiO_2 underlying the Ge fin.

4.3.5 Gate Stack Formation

After DHF cleaning, the samples were loaded into an ultra-high vacuum (UHV) tool for pre-gate SF_6 plasma clean of 50 s to remove any residual native oxide on the Ge surface. *In situ* Si_2H_6 treatment was then performed to form a high quality Si passivation layer at a temperature of less than 400 ℃ to avoid any Si and Ge inter-diffusion [53] [157, 158]. Gate stack comprising of ~4 nm HfO_2 and TaN was then deposited by atomic layer deposition (ALD) and sputtering, respectively [Fig. 4.3 (d) and (e)]. Fig. 4.12 (a) shows HRTEM of TaN/HfO_2/SiO_2/Si stack formed on bulk Ge (100) substrate, demonstrating that the Si passivation layer was partially oxidized. In a separate experiment involving Si_2H_6 treatment of $Ge_{0.97}Sn_{0.03}$ surface, which is similar to Ge, data obtained using X-ray Photoelectron Spectroscopy indicates the presence of both SiO_2 and Si beneath the HfO_2. Fig. 4.12 (b) shows the gate leakage current I_G as a function of gate voltage V_G of a metal gate pad having an area of 10^{-4} cm^2 which was formed on bulk Ge substrate. Very low gate leakage current density of ~1.5×10^{-6} A/cm^2 was obtained from the Si_2H_6 passivated gate stack at a gate voltage V_G of -1 V, indicating the high quality of the gate stack.



(a) (b)

Fig. 4.12. (a) HRTEM of gate stack formed on bulk (100) Ge substrate, clearly showing the SiO_2/Si passivation. (b) Gate leakage current I_G *vs.* gate voltage V_G plot of a gate pad with an area of 10^{-4} cm^2 formed on bulk Ge substrate.

4.3.6 Gate Etch

Upon finishing gate stack, gate patterning was performed by EBL, followed by gate etch. Due to the topology of the vertical fin channel, metal gate spacers are usually formed adjacent to the Ge fin after the normal gate etch process used for planar devices, as illustrated in Fig. 4.13. These metal spacers are not desirable, as they not only lead to possible gate-to-source/drain short, but also reduce the source/drain (S/D) contact area when NiGe contact is formed. It is essential to maintain as large a contact area as possible to reduce contact resistance for MuGFETs. Therefore, it is crucial to remove the metal gate spacers to achieve a lower contact resistance.

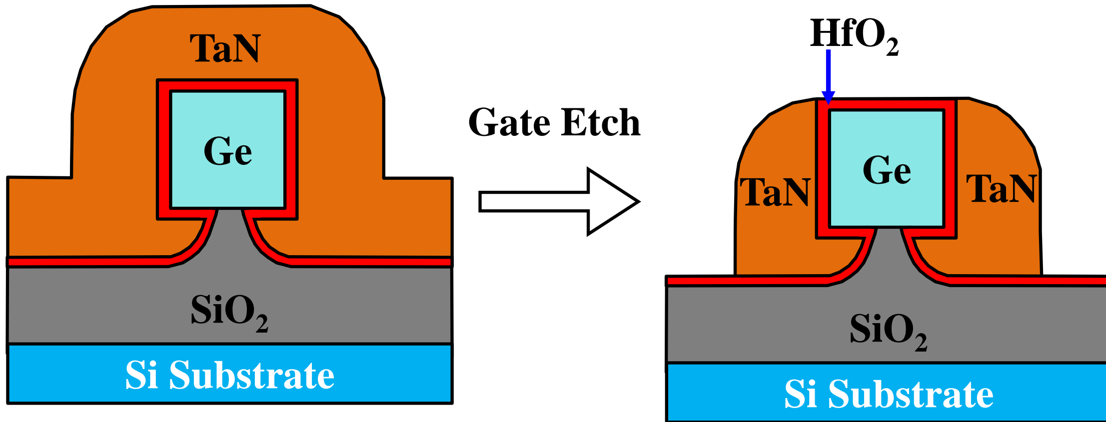


Fig. 4.13. Schematics demonstrating TaN spacer formation adjacent to Ge fin after a normal gate etch process used for planar MOSFETs.

Table 4.1. Gate etch recipes for TaN gate etch (main etch for removing TaN in planar region) and TaN spacer removal etch (over-etch step). The TaN spacer removal etch recipe employs CHF_3 to achieve a much higher etch selectivity of TaN over HfO_2.

Recipe Name	Cl_2 (sccm)	Ar (sccm)	CHF_3 (sccm)	He-O_2 (sccm)	Substrate Bias (W)
TaN Gate Etch Recipe	200	0	0	0	200
TaN Spacer Etch Recipe	120	40	80	10	80

In this work, a two-step gate etch process was developed, of which the first etch step employs the TaN gate etch recipe while the second step employs a TaN spacer removal recipe. Table. 4.1 shows the recipes used in this work. In the TaN spacer removal step, CHF_3 was used to enhance the TaN:HfO_2 etch selectivity. Fluorine-based plasma could suppress the HfO_2 etch rate by forming HfO_XF_Y, which is much more difficult to remove, on the HfO_2 surface [159]. Moreover, the substrate bias in the TaN spacer removal recipe was purposely reduced to achieve better

selectivity of TaN:HfO_2 and to increase the degree of isotropy in the etching of TaN underneath the Ge fin. Fig. 4.14 (a) and (b) show two schematics demonstrating TaN spacer removal from the sidewalls of the Ge fin using the new TaN spacer etch recipe. As the TaN spacer etch recipe utilizes a lower substrate bias, the etch of TaN by this recipe is more isotropic, as compared with the normal TaN gate etch recipe, which makes etching of the TaN underneath the Ge fin possible.

Fig. 4.15 (a) and (b) show two cross-sectional schematics of NiGe formed on Ge fins (non-gate region) without and with metal gate spacers removed, illustrating the benefit of removing TaN spacers adjacent to the Ge fin. Tilted SEM images of the gate regions of two transistors without and with removal of the TaN spacer by the sidewalls of the Ge fin are shown in Fig. 4.16 (a) and (c), respectively. Fig. 4.16 (b) and (d) are the zoomed-in SEM images of the regions as highlighted by the rectangles in Fig. 4.16 (a) and (c), respectively. The TaN spacers along the Ge fin of the device in Fig. 4.16 (a) are demonstrated to be fully etched using the TaN spacer removal recipe developed in this work.

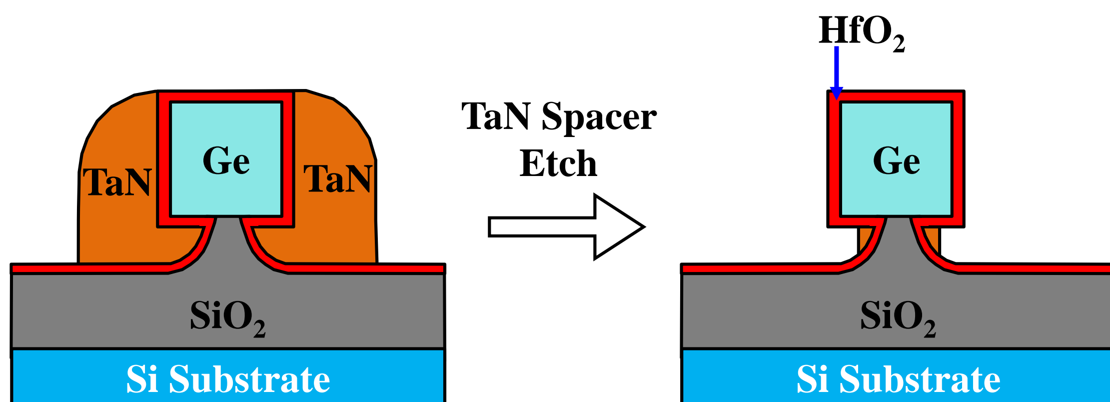


Fig. 4.14. Schematics demonstrating TaN spacer removal from the sidewalls of the Ge fin using the new TaN spacer etch recipe.

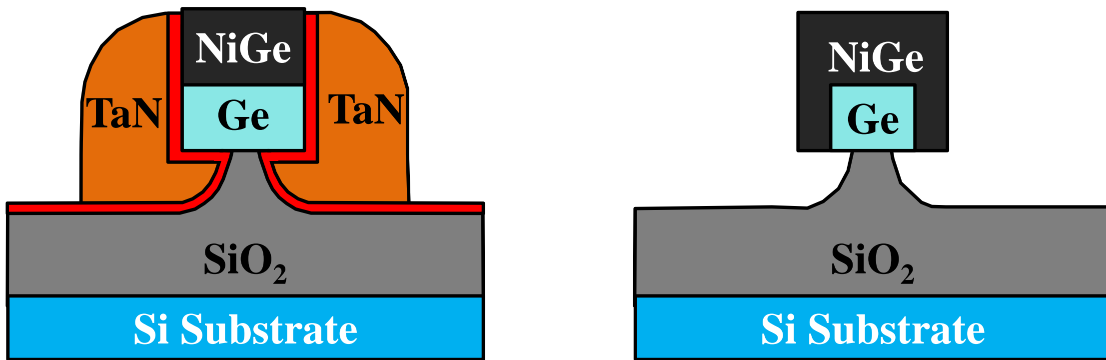


Fig. 4.15. Schematics of NiGe formation on Ge fin (non-gate region) (a) without and (b) with removal of metal spacers. Successful removal of TaN spacers adjacent to the Ge fin leads to a larger NiGe contact area. This is crucial to maintain a relatively small source/drain resistance for Ge MuGFETs.

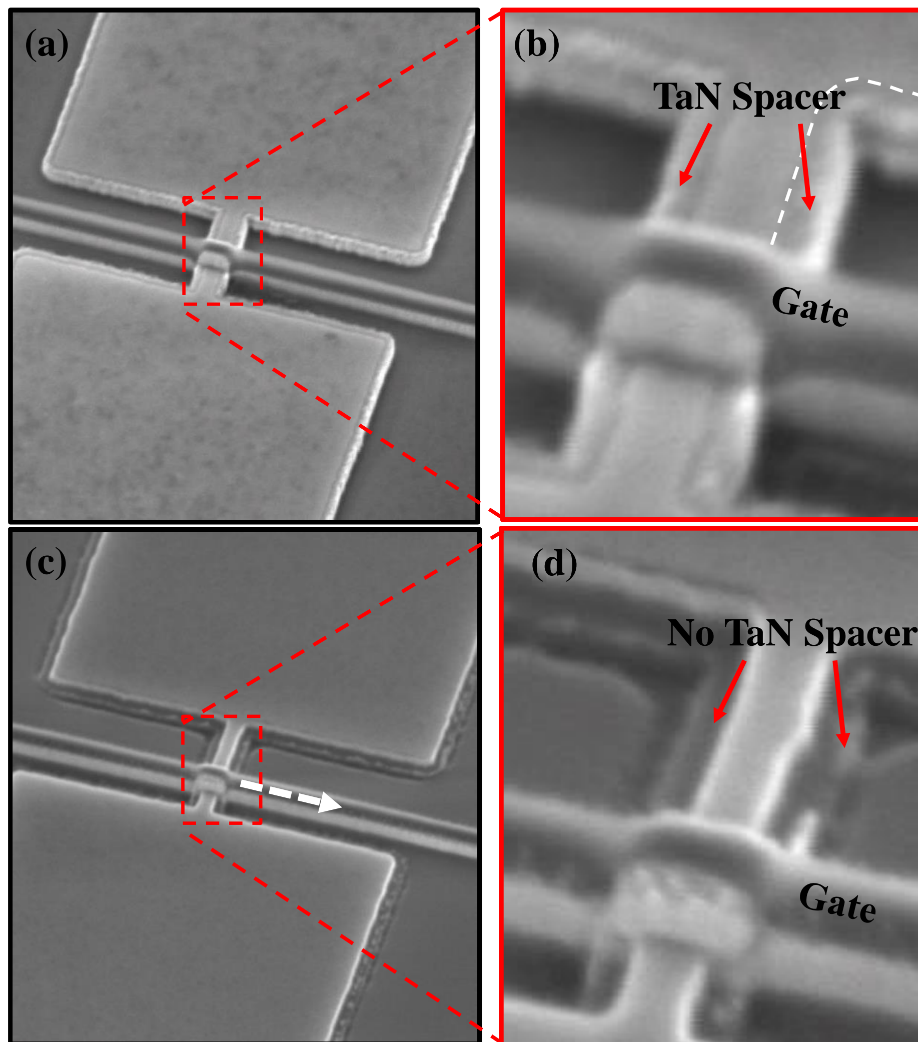


Fig. 4.16. Tilted SEM of gate regions of two transistors (a) without and (c) with removal of the TaN spacer by the sidewall of the Ge fin. (b) and (d) are the corresponding zoom-in SEM images of the regions as indicated by the rectangles in (a) and (c), respectively.

4.3.7 Contact Formation

After gate etch, 10 nm Ni was deposited by sputtering, followed by a two-step sub-400 ℃ annealing process (250 ℃ / 330 ℃) [60, 160] to form the self-aligned NiGe metallic S/D. The excess Ni was removed by sulphuric acid (H_2SO_4) at room temperature. Fig. 4.17 shows a TEM image of NiGe formed on a Ge fin with a fin width W_{FIN} of ~55 - 60 nm. The NiGe formation on both of the sidewalls of Ge fin is clearly demonstrated, as the TaN spacers along the fin side walls were removed. The TaN under the Ge fin was partially removed by the TaN spacer etch recipe, longer over etch time is required to fully remove the TaN under the Ge fin.

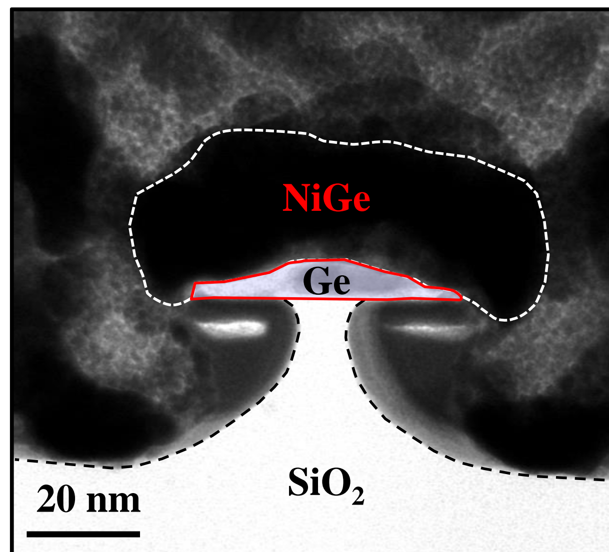
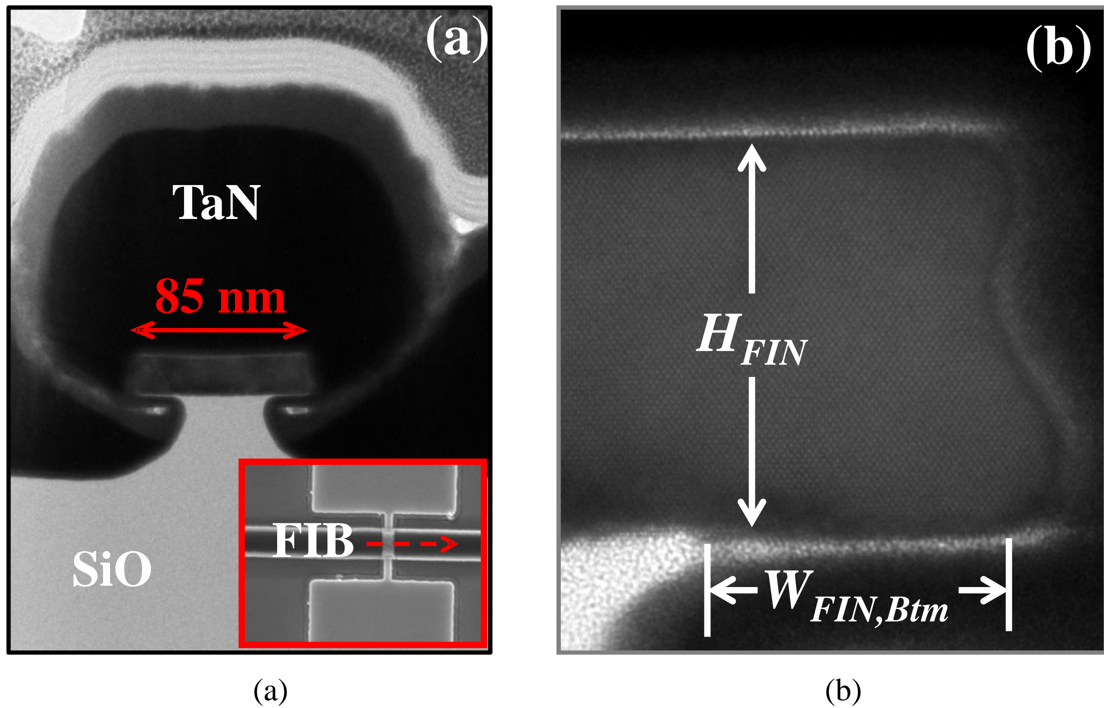


Fig. 4.17. TEM image of NiGe formed on Ge fin, showing NiGe formed on the side wall of the fin.



(a) (b)

Fig. 4.18. (a) TEM image of the Ω-gate Ge MuGFET with a W_{FIN} of ~85 nm. (b) HRTEM of the right half of the fin. The rounded fin corners were due to the SF_6 plasma cleaning. A Si passivation layer can be seen on (100) surface.

Fig. 4.3 (f) shows a 3D device structure of the transistor fabricated in this work. Fig. 4.18 (a) shows a TEM image of a MuGFET with FIB cut direction indicated in the inset SEM image. The Ω-shaped metal gate wraps around the Ge fin which has a fin height H_{FIN} of ~23 nm and a fin width W_{FIN} of ~85 nm. The Ω-shaped metal could provide better gate control as compared with normal tri-gate structure. Devices with W_{FIN} from ~60 nm to ~85 nm and physical gate length L_G from ~90 nm to ~380 nm were fabricated. Fig. 4.18 (b) shows a HRTEM image of the fin region. The SiO_2/Si passivation can be seen on the (100) top surface.

4.4 Results and Discussion

4.4.1 Inversion C-V Characterization

The inversion capacitance *C* versus voltage *V* (*C*-*V*) plot of a long channel transistor fabricated on bulk Ge substrate using the same gate stack formation process that was used for the MuGFETs is shown in Fig. 4.19. The capacitance equivalent thickness (CET) of this device is ~1.7 nm.

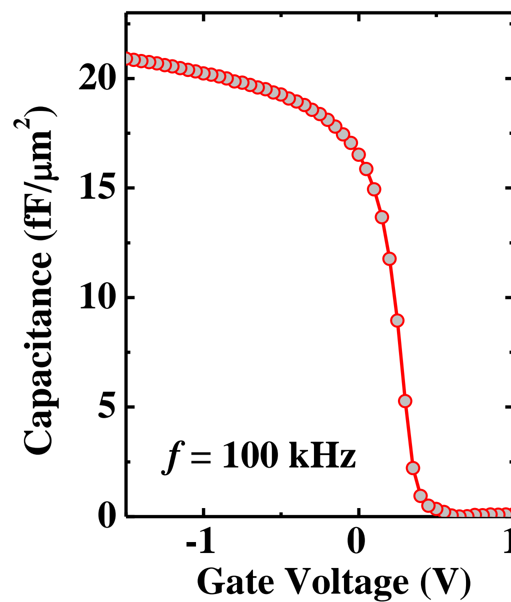


Fig. 4.19. Inversion *C*-*V* measured on a long channel transistors fabricated on bulk Ge substrate using the same gate stack formation process as the MuGFETs.

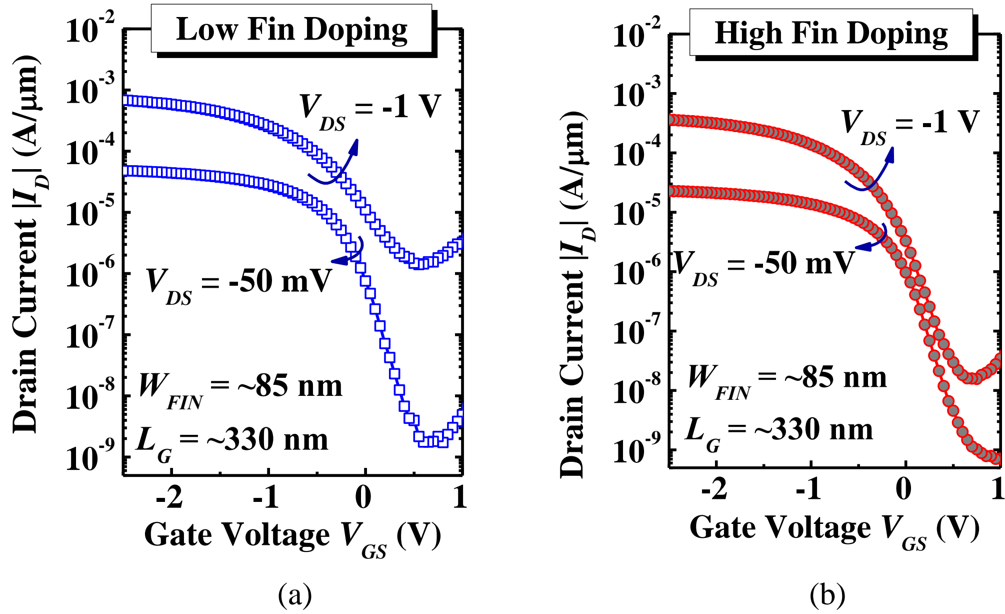


Fig. 4.20. $|I_D|$-V_{GS} characteristics of two MuGFETs having the same physical L_G of ~330 nm and the same W_{FIN} of ~85 nm, but different phosphorus implant doses for n-well formation: (a) 8×10^{12} cm^{-2} and (b) 1.6×10^{13} cm^{-2}.

4.4.2 Short Channel Effects of Devices with Low and High Fin Doping

All devices were characterized by direct probing on NiGe metal pads of the S/D regions and gate pads. Fig. 4.20 (a) and (b) show the drain current $|I_D|$ versus gate voltage V_{GS} curves for two Ge MuGFETs which have a same L_G of ~330 nm and a same W_{FIN} of ~85 nm, but received with two different P implant doses of 8×10^{12} cm^{-2} (low fin doping) and 1.6×10^{13} cm^{-2} (high fin doping) during n-well formation. The values of drain current reported in this work are normalized by the total effective channel width W_{EFF}, where W_{EFF} is calculated as W_{FIN} + 2 H_{FIN} + 2 $W_{FIN,Btm}$ [$W_{FIN,Btm}$ is illustrated in Fig. 4.18 (b)]. W_{EFF} of these two devices in Fig. 4.20 are ~165 nm. At V_{DS} = -50 mV, both devices demonstrate similar subthreshold swing SS, and show good I_{ON}/I_{OFF} ratio of more than 10^4. At V_{DS} = -1 V, the device with high fin doping still has a good I_{ON}/I_{OFF} of more than 4 orders, while the device with low fin doping shows higher off-state leakage current which leads to poor I_{ON}/I_{OFF} ratio. The high

off-state leakage current at low V_{GS} could interfere with the extraction of SS as much of the subthreshold region may not be observed due to a high leakage floor. As a result, the device with lower fin doping has a higher SS than the device with higher fin doping at V_{DS} of -1 V. In addition, the MuGFET with higher fin doping exhibits a smaller DIBL of 107 mV/V, as compared with the MuGFET with low fin doping.

Fig. 4.21 shows the cumulative plots of I_{MIN} at V_{DS} = -50 mV for devices with different fin dopings. I_{MIN} is taken as the minimum drain current in the $|I_D|$-V_{GS} plot. Devices with high fin doping and low fin doping demonstrate median I_{MIN} of ~0.65 nA/μm and ~1.15 nA/μm, respectively. Low leakage current observed may be partially due to a suppressed ambipolar behaviour (as confirmed by invisible plateaus under the n-FET bias conditions [161]), which is consistent with high contact resistance between NiGe and n-Ge estimated from literature [162], where Ge has similar n-type doping concentration as in this work.

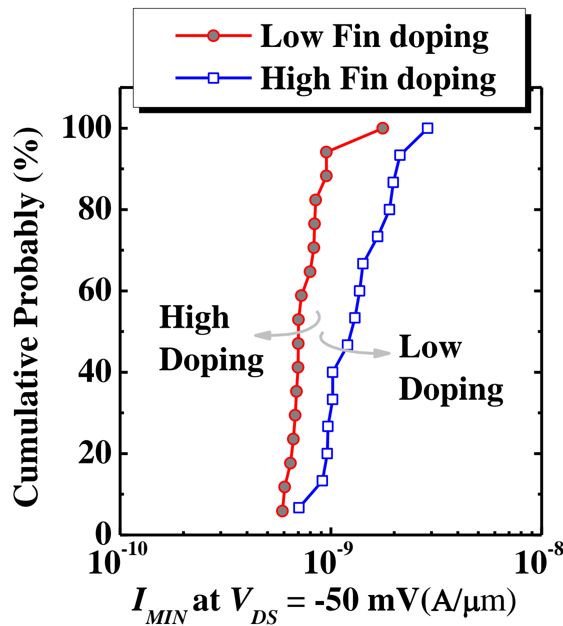


Fig. 4.21. Cumulative plot of I_{MIN} for MuGFETs with different fin dopings at V_{DS} = -50 mV. I_{MIN} is the minimum value of $|I_D|$ in the $|I_D|$-V_{GS} plot at V_{DS} = -50 mV. MuGFETs with high fin doping show slightly lower I_{MIN} as compared with those with low fin doping.

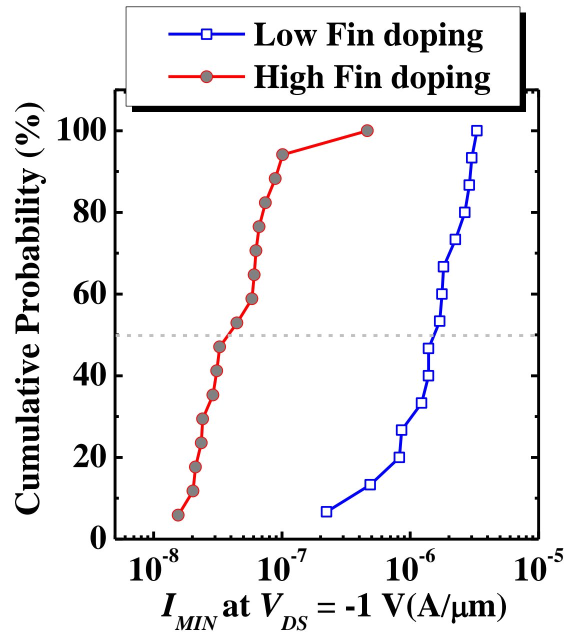


Fig. 4.22. Cumulative plot of I_{MIN} at V_{DS} = -1 V for MuGFETs with different fin dopings. MuGFETs with high fin doping show significantly lower I_{MIN} as compared with those with low fin doping.

Fig. 4.22 shows the cumulative plots of I_{MIN} at V_{DS} = -1 V for devices with different fin doping concentrations, demonstrating that devices with higher doping have lower I_{MIN}. MuGFETs with low and high fin doping show median I_{MIN} of 1.55×10^{-6} A/μm and 3.84×10^{-8} A/μm, respectively. It could be concluded that additional channel doping helps reduce off-state leakage current of Ge MuGFETs on GeOI substrates.

Fig. 4.23 shows DIBL-L_G characteristics of MuGFETs with low and high fin doping. DIBL increases as L_G scales down for both splits. The devices with higher doping have lower DIBL. A device with high fin doping and a gate length of ~90 nm has a DIBL of ~330 mV/V. Increasing channel doping could reduce the NiGe/n-Ge depletion length, which in turn leads to better short channel effects (SCEs). This, however, is believed not to be the only reason that leads to better SCEs. Another

important factor which is related to the nature of GeOI substrate will be discussed later. The Ge fin widths fabricated in this work ranges from ~60 nm to 85 nm. The relatively large fin width may result in slightly compromised short channel control from the tri-gate structure. Further trimming down the width of the Ge fin to sub-50 nm could be performed to have better short channel control.

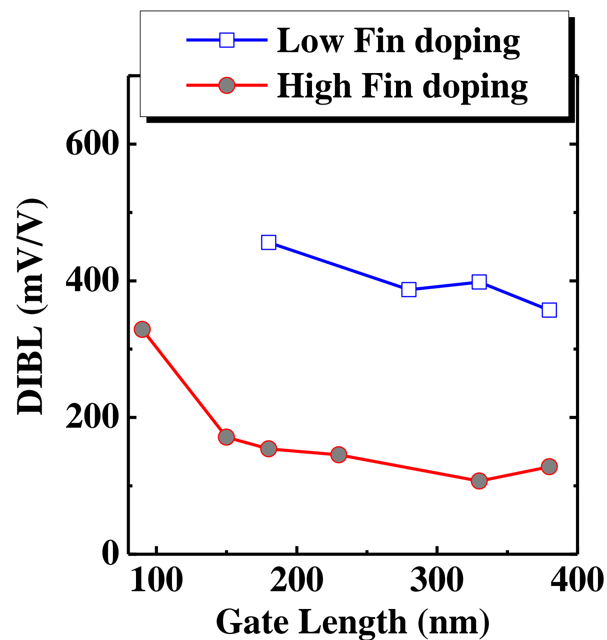


Fig. 4.23. DIBL-L_G characteristics of MuGFETs with low and high fin doping. DIBL increases as L_G scales down. Device with high fin doping and a gate length of ~90 nm has a DIBL of ~330 mV/V.

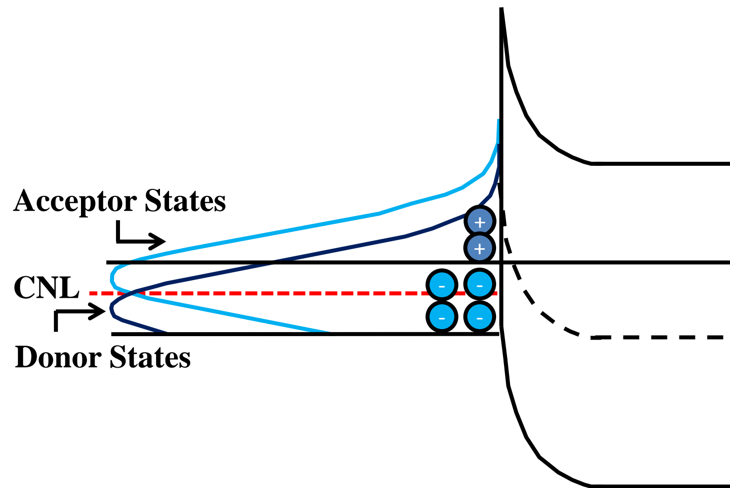


Fig. 4.24. Band diagram of n-type Ge under the influence of interface charges.

4.4.3 Low Temperature Characterization of Ge MuGFETs

Despite the use of multi-gate structure and small fin dimension (~23 nm × ~85 nm), the device with low Ge fin doping has poor control of short channel effects. This could be due to negative charges at the unpassivated Ge-SiO_2 interface at the backside of Ge layer, as discussed in the literature [163-165]. The charge neutrality level (CNL) of Ge is near the valence band minimum. The negative charges contributed by filled acceptors below the Fermi level is larger than the positive charge due to empty donors above the Fermi level, resulting in a net negative charge at the Ge-oxide interface [163], as illustrated by Fig. 4.24. Depending on n-type Ge doping concentration and the backside negative charge density, the charges could possibly induce weak-to-strong surface inversion of n-type Ge even without a gate bias. Taking a backside interface charge density of 5×10^{12} $eV^{-1}\cdot cm^{-2}$ for an example, active channel doping concentrations of ~2×10^{17} cm^{-3} and ~4×10^{17} cm^{-3} will result in surface potentials of ~0.278 eV and ~0.158 eV, respectively, as extracted from Fig. 3 (b) of Ref. [163]. The increase in surface potential of ~80 mV caused by decrease of doping

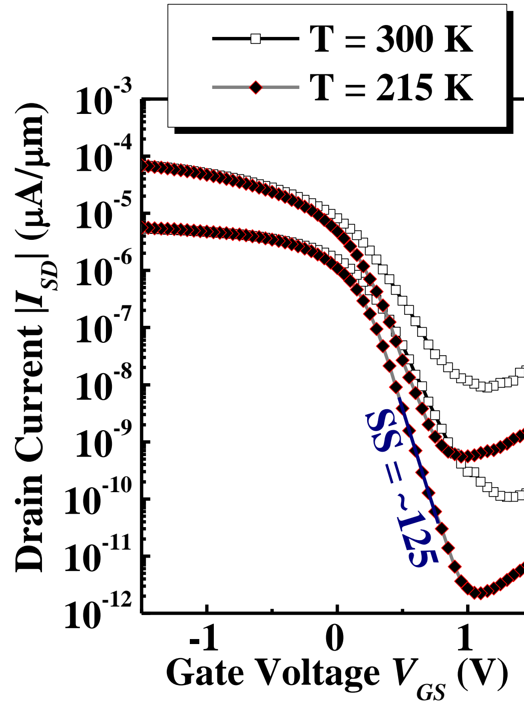


Fig. 4.25. $|I_D|$-V_{GS} characteristics of a MuGFET with high fin doping at different temperatures of 300 K, and 215 K. Lower temperature results in smaller leakage current, leading to smaller SS and DIBL.

concentration will result in more than 10 times increase in the leakage current. This leads to an increase in the extracted DIBL and SS. The backside negative interface charges could possibly lead to a source-to-drain leakage current path and poor short channel control, especially when the effective n-type channel doping is low. From the experimental data, the effect of the backside inversion of the GeOI substrate could be important in determining the short channel effects of the devices with low channel doping.

Low temperature characterization was performed on a MuGFET with high doping to study the backside interface charge effect. Fig. 4.25 shows the $|I_D|$-V_{GS} characteristics of a MuGFET at different temperatures of 300 K and 215 K. Lowering

temperature leads to smaller off-state leakage current, resulting in smaller SS and DIBL. At lower temperature, the probability of electron tunnelling from drain to source decreases, resulting in smaller reverse leakage current. In the meantime, trap assisted tunnelling (TAT) and Schottky Read Hall (SRH) recombination are also reduced [165], which further contributes to the reduction of leakage current. In addition, it was also suggested that interface charge density decreased with temperature [166], which in turn reduces any backside leakage current due to backside negative interface charges.

When a SBMOFET is operating at the subthreshold regime, the current of SB-MOSFET can theoretically be modelled using a thermionic emission equation

$$I_D = -AA^*T^2 e^{-q\phi_{BH}/kT} \left(e^{qV_{DS}/kT} - 1\right), \tag{4-1}$$

where A is the cross-sectional area, A^* is the effective Richardson constant, T is temperature, ϕ_{BH} is effective hole barrier height, and V_{DS} is the drain voltage. Schottky barrier height could be estimated by using different I_D measured at different temperatures. The following Equation 4-2 describes temperature dependence of barrier height of a SBMOSFET, as suggested by [167],

$$\frac{I_{D,T1}}{I_{D,T2}} \approx \frac{T_1^2}{T_2^2} e^{-q\phi_{BH}(1/T_1 - 1/T_2)/k}, \tag{4-2}$$

where $I_{D,T1}$ and $I_{D,T2}$ are the drain current at temperature T_1 and T_2, respectively. Fig. 4.26 shows the extracted hole barrier height versus gate voltage V_{GS}. As V_{GS} becomes larger (more negative), the band diagram is pulled up, making the hole barrier height become smaller. Barrier width thinning due to large negative V_{GS} results in larger tunnelling current, which contributes to effective barrier height reduction.

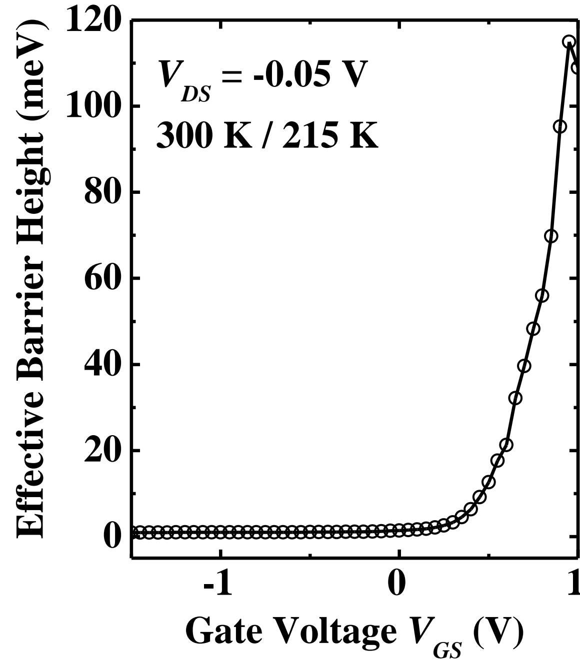


Fig. 4.26. Effective Schottky barrier height versus V_{GS} at V_{DS} = -0.05 V. The curve was extracted using I_D-V_{GS} characteristics measured at 215 K and 300 K.

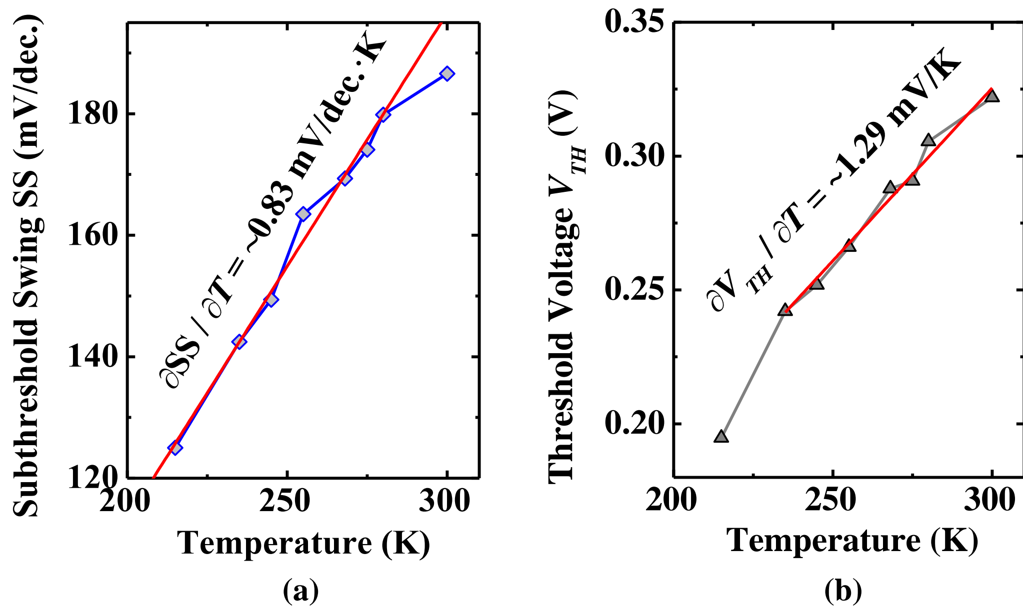


Fig. 4.27. (a) SS-Temperature T and (b) V_{TH}-T plots for a MuGFET with high doping and W_{FIN} of ~85 nm. The red lines in (a) and (b) are best fit lines.

Temperature dependences of SS and V_{TH} are shown in Fig. 4.27 (a) and (b), respectively. The slope of $\partial SS/\partial T$ observed is ~0.83 mV/decade·K, which is much

larger than the theoretical predicted value of ~0.2 mV/decade·K. This is believed due to both the HfO_2-Ge and SiO_2-Ge interface charges. V_{TH}-T plot in Fig. 4.27 (b) indicates a $\partial V_{TH} / \partial T$ of ~1.29 mV/K. The larger temperature dependence of V_{TH}, as compared with the theoretical value corresponding to channel doping of ~10^{17}-10^{18} cm^{-3}, further suggests the existence of backside interface charge effect on device performances [168, 169]. This is because the backside charges could result in larger slope of $\partial V_{TH} / \partial T$ [168, 169].

The backside charges at the Ge-SiO_2 interface poses new challenge to integration of FinFETs/MuGFETs on GeOI substrate. The experimental data in this work indicate one possible direction to overcome the problem, i.e. doping the Ge, especially the first a few monolayer of Ge at the backside. The Ge region near the buried oxide could be doped more heavily to have better short channel control. Increasing fin doping results in substantial leakage current reduction especially at a high drain voltage, e.g. V_{DS} = -1 V, and better short channel control. This is because higher fin doping could help prevent the formation of surface inversion by providing more space charges to balance the negative interface charges [163]. Another possible approach is to passivate the backside Ge surface with Si, as suggested by [164]. Si passivation was demonstrated to be able to significantly reduce the off-state leakage current of MOSFETs on GeOI substrate.

4.4.4 Drive Current and Transconductance of MuGFETs with Different Dopings

Although additional doping results in better short channel effects, high fin doping leads to performance degradation in terms of drive current as well as transconductance due to the more severe impurity scattering [170, 171]. This

phenomenon was also observed in Si FinFETs [172, 173]. The empirical relationship between channel doping concentration and carrier mobility can be expressed as [4],

$$\mu = \mu_0 e^{-P_c/N} + \frac{\mu_{max}}{(N/C_r)^{\alpha}+1} - \frac{\mu_1}{(C_s/N)^{\beta}+1}, \tag{4-3}$$

where μ is carrier mobility, μ_{max} is the highest carrier mobility in bulk semiconductor (μ_{max} is 1900 $cm^2V^{-1}s^{-1}$ for holes in Ge), P_c, μ_{max}, μ_1, μ_0, C_r, C_s, α, and β are empirical parameters with positive values obtained by fitting the experimental results, and N is doping concentration. Carrier mobility decreases as doping concentration increases. The values of P_c, μ_{max}, μ_1, μ_0, C_r, C_s, α, and β for Ge were reported by G. Hellings *et. al* [171]. Assuming a reference total doping concentration (including both active and non-active dopants) of 1×10^{18} cm^{-3}, a 1 to 2 times higher channel doping concentration with respect to the reference doping value could lead up to ~50 % carrier mobility degradation.

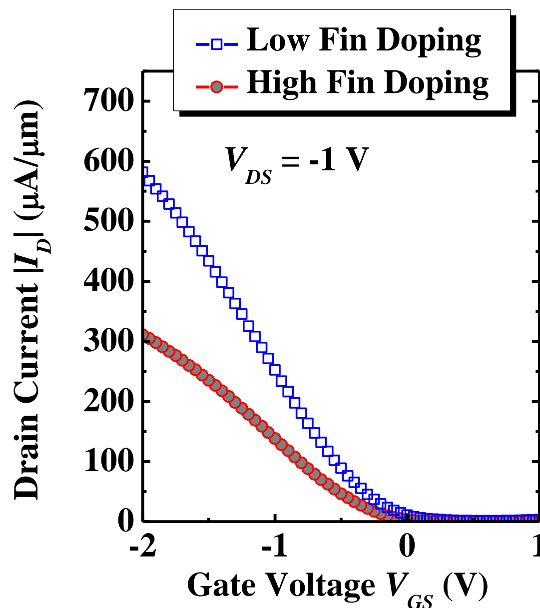


Fig. 4.28. $|I_D|$-V_{GS} characteristics at V_{DS} = -1 V of MuGFETs having the same L_G and W_{FIN}, but different P doping concentrations. Device with a low fin doping has a higher drain current at a fixed V_{GS}.

Fig. 4.28 shows $|I_D|$ versus V_{GS} characteristics at V_{DS} = -1 V of the same two Ge MuGFETs with a same L_G of ~330 nm and a same W_{FIN} of ~85 nm in Fig. 4.20, but received with two different P implant doses, demonstrating the device with low fin doping has a higher drain current at a fixed V_{GS}. G_{MSat} versus V_{GS} at V_{DS} = -1 V plots in Fig. 4.29 demonstrate the device with low fin doping has higher saturation transconductance G_{MSat}. The additional doping leads to G_{MSat} degradation for MuGFETs with L_G of ~330 nm. As expected, a higher fin doping degrades the current as well as the transconductance, even though it leads to better control of short channel effects. This is partially caused by the increased carrier scattering due to the additional dopants in the channel.

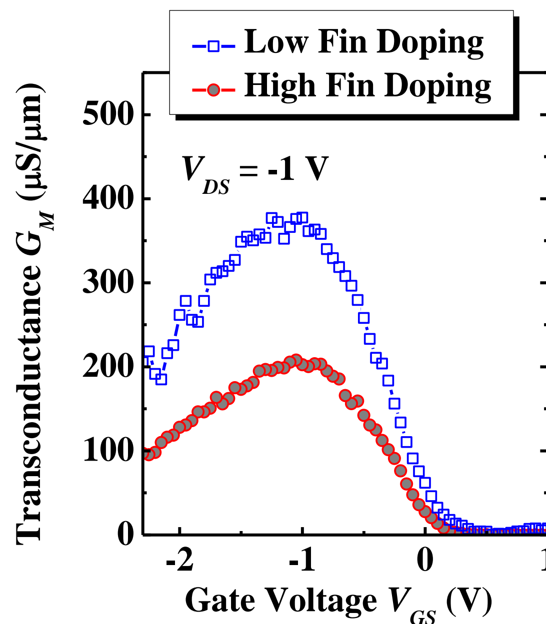


Fig. 4.29. G_M-V_{GS} characteristics at V_{DS} = -1 V of MuGFETs having the same L_G and W_{FIN}, but different phosphorus doping concentrations. Device with a low fin doping has a higher peak saturation transconductance.

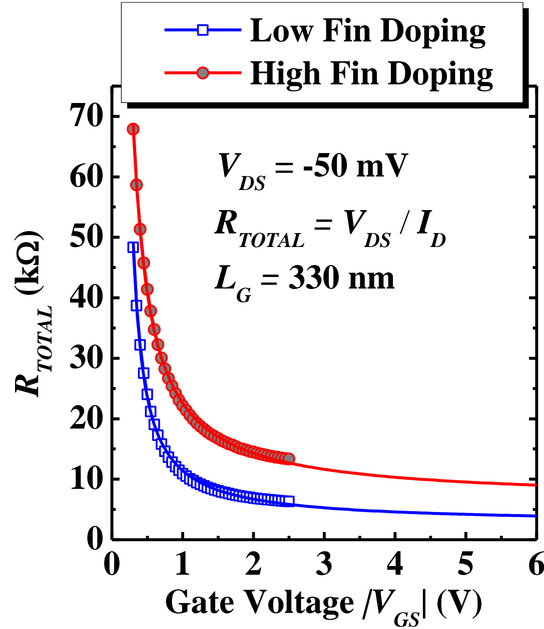
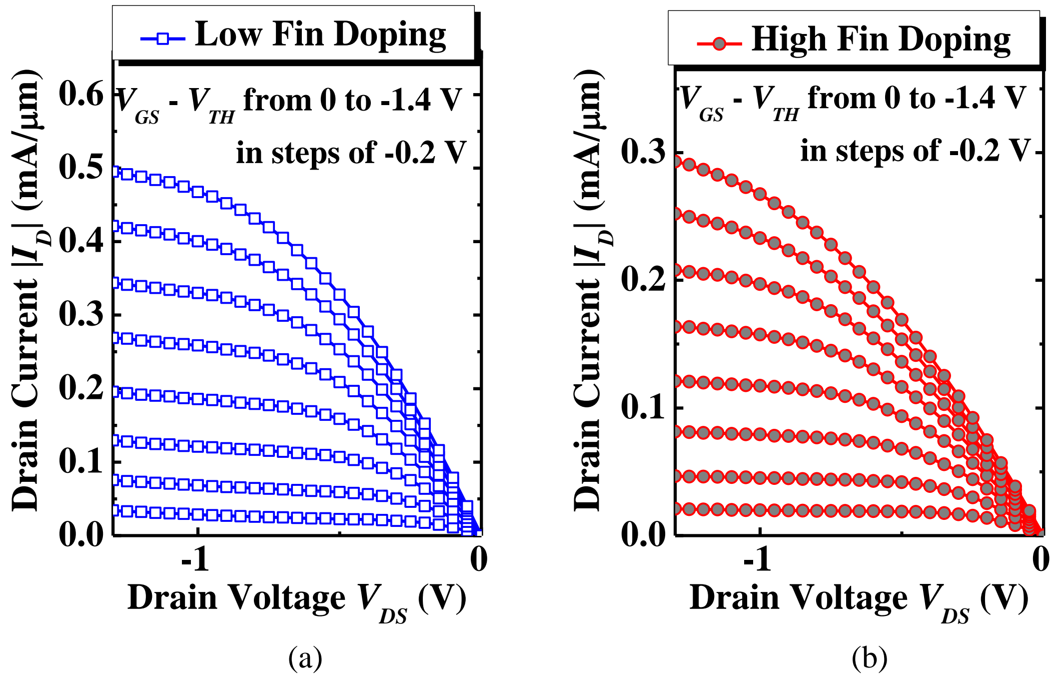


Fig. 4.30. R_{TOTAL}-$|V_{GS}|$ plots of the same two devices of Fig. 4.20, showing that the device with a low fin doping has a lower extrapolated R_{SD}.

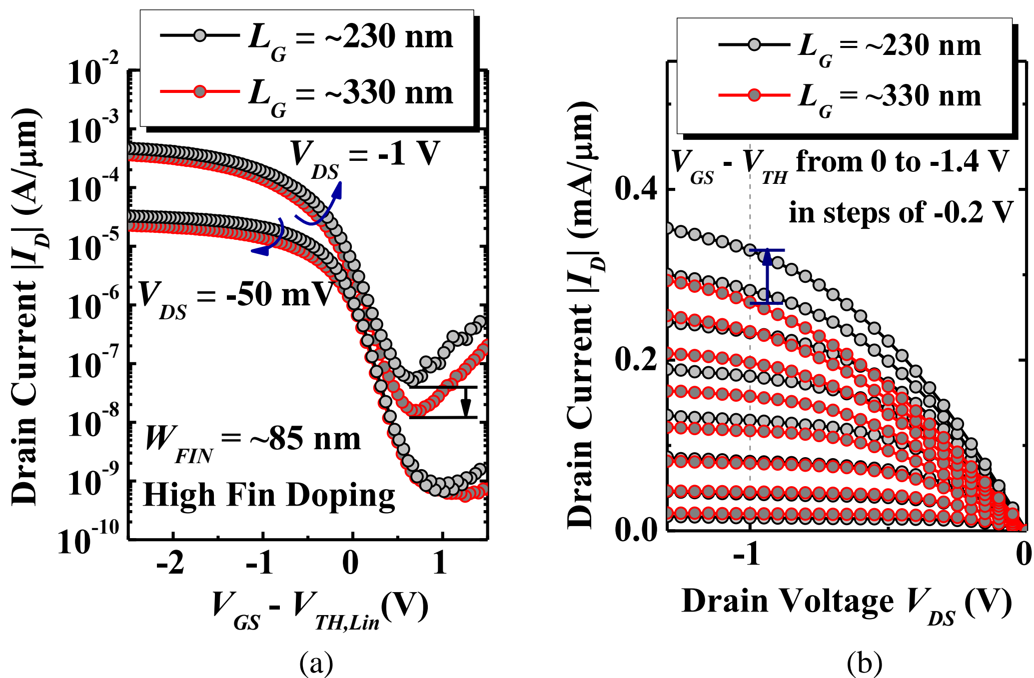
In addition, it is also observed that the device with higher fin doping has a larger source-to-drain series resistance R_{SD}, as demonstrated by the total resistance R_{TOTAL}-$|V_{GS}|$ plot in Fig. 4.30. R_{TOTAL} is extracted using V_{DS} / I_D, where V_{DS} = -50 mV. The formation of NiGe on sidewall of Ge fin helps maintain R_{SD} as low as possible. It was demonstrated by a few groups that increase the n-type doping of Ge could result in lower electron barrier height and higher hole barrier height [174, 175]. The possible higher hole barrier caused by the additional P doping of the high fin doping device split could possibly contribute to the higher R_{SD} of device with high fin doping.

The enhanced carrier scattering induced by additional fin doping and higher R_{SD} results in smaller on-state current I_{ON} of the MuGFET with high fin doping. As observed from the $|I_D|$-V_{DS} characteristics in Fig. 4.31 (a) and (b), devices with low and high fin doping show I_{ON} of 330 μA/μm and 197 μA/μm, respectively, at V_{DS} = -1 V and V_{GS} - V_{TH} = -1 V.



(a) (b)

Fig. 4.31. $|I_D|$-V_{DS} plots of the two devices with (a) low and (b) high fin doping, showing that the device with a low fin doping has a higher drain current at the same V_{DS} and V_{GS} - V_{TH}.



(a) (b)

Fig. 4.32. (a) $|I_D|$-(V_{GS} - $V_{TH,Lin}$) and (b) $|I_D|$-V_{DS} characteristics of two MuGFETs receiving the same P implant dose of 1.6×10^{13} cm^{-2} but with different L_G of ~330 nm and ~230 nm.

4.4.5 Scaling of Ge MuGFETs with Metal S/D

Fig. 4.32 (a) compared $|I_D|$-(V_{GS} - $V_{TH,Lin}$) of two MuGFETs with the same high P dose of 1.6×10^{13} cm^{-2} but with different L_G of ~330 nm and ~230 nm. The two devices show similar SS at V_{DS} = -0.05 V. The MuGFET with smaller L_G of ~230 nm shows slightly larger DIBL, and higher off-state leakage current at V_{DS} = -1 V, as compared with the one with larger L_G of ~330 nm. Visible drain current enhancement was observed when scaling the gate length from ~330 nm to ~230 nm. $|I_D|$-V_{DS} of the same two devices shown in Fig. 4.32 (b) demonstrates that the MuGFET with L_G of ~230 nm has a larger drive current at a fixed gate overdrive and V_{DS}, as compared with the one with L_G of ~330 nm.

Fig. 4.33 shows peak linear transconductance $G_{MLinMax}$ versus L_G for devices with low and high fin doping. It could be observed that $G_{MLinMax}$ increases as L_G scales down for both of the splits. Similarly, $G_{MSatMax}$ also scales well with L_G, as

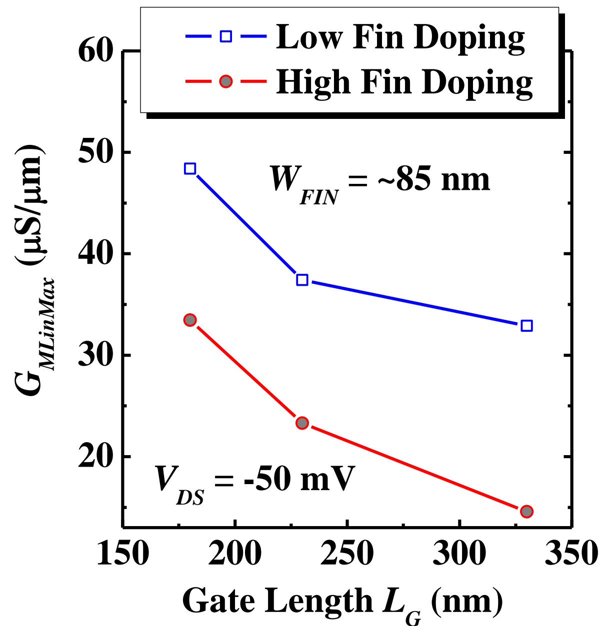


Fig. 4.33. Peak linear transconductance $G_{MLinMax}$ versus L_G for devices with low and high fin doping. $G_{MLinMax}$ increases as L_G scales down.

demonstrated by Fig. 4.34. Fig. 4.35 shows I_{ON} versus L_G for devices with different dopings, with I_{ON} taken at V_{GS} - V_{TH} = -1 V and V_{DS} = -1 V. It is observed that I_{ON} increases as gate length scales down. Further scaling of L_G will lead to higher transconductance and drive current, demonstrating good scalability of Ge MuGFETs. It is worth pointing out that the transconductance degradation observed on devices with high fin doping is larger than the theoretical prediction by Equation 4-3 which predicts a mobility degradation of up to 50 %. The higher series resistance of the device with high doping is believed to contribute to drive current.

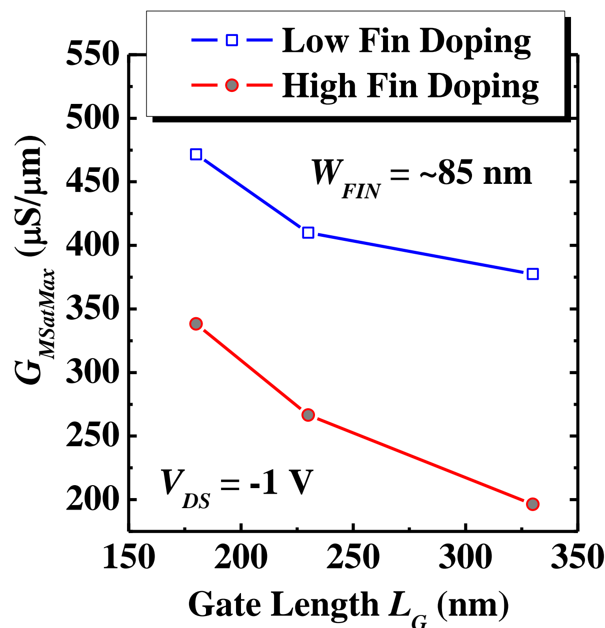


Fig. 4.34. Peak Saturation transconductance $G_{MSatMax}$ versus L_G for devices with low and high fin doping. $G_{MSatMax}$ increases as L_G scales down.

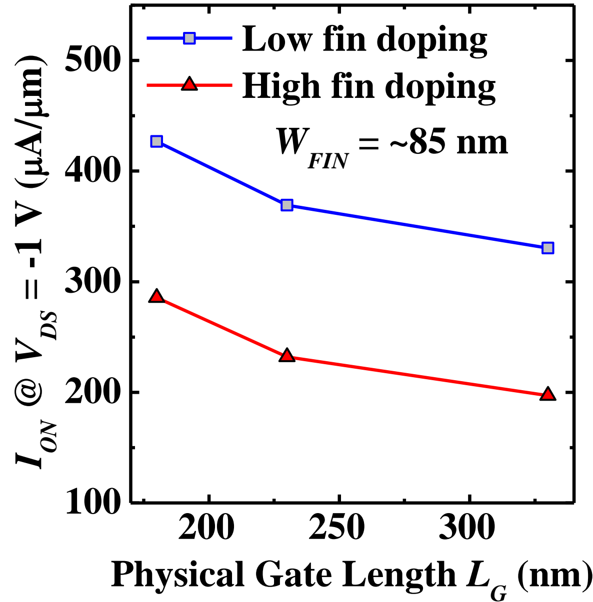


Fig. 4.35. I_{ON} versus L_G for devices with different dopings, with I_{ON} taken at V_{GS} - V_{TH} = -1 V and V_{DS} = -1 V.

Devices fabricated in the current work have large variations. The device variations could be due to random dopant fluctuation (RDF) [176, 177], Ge fin height and fin width variation, and gate length variation (lithography and etching related). It has been demonstrated that RDF could be suppressed by reducing the channel doping of the device [178]. Utilizing Ge fins with smaller dimensions [179] or adoption of GAA structure could help achieve good short channel control with low or even no channel doping, resulting in good RDF. In addition, using thinner oxide could also result in smaller fluctuations of device performance. The fin height variation which is mainly caused by the initial Ge layer thickness of the GeOI substrate is believed to be one of the main sources for device variations, especially drive current and transconductance variations. Current and transconductance degradations due to higher channel doping are slightly different at different L_G, and this could be due to the deviations caused by the factors mentioned.

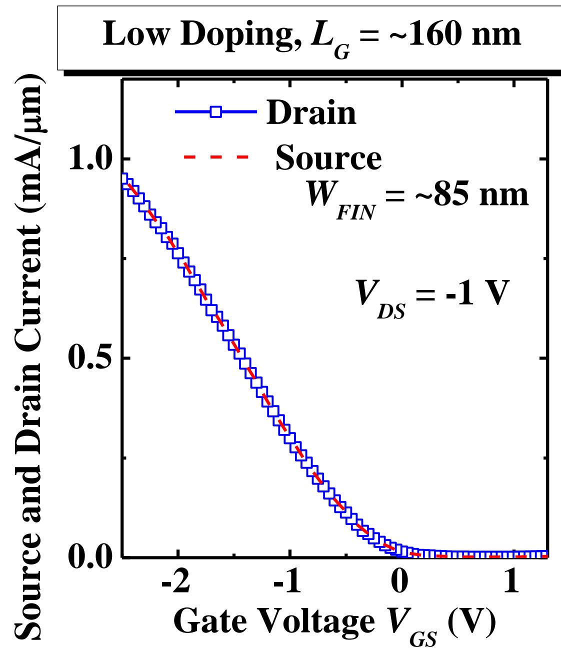


Fig. 4.36. Source and drain current (left axis) vs. V_{GS} characteristics at V_{DS} = -1 V of a device with low fin doping, a L_G of ~160 nm, and a W_{FIN} of ~85 nm.

4.4.6 Device Performance of Short Channel Ge MuGFETs

In this sub-section, the performance of a device with shorter channel length and low fin doping is discussed. Fig. 4.36 shows the source and drain current *vs.* V_{GS} at V_{DS} = -1 V of a device with a L_G of ~160 nm, and a W_{FIN} of ~85 nm. Almost identical source and drain currents were observed, which is due to the employment of GeOI substrate. At V_{DS} = -1 V and V_{GS} - V_{TH} = -2 V (V_{TH} is taken using maximum transconductance method at V_{DS} = -1 V), a very high saturation current of ~920 µA/µm was achieved. Fig. 4.37 shows G_M *vs.* V_{GS} characteristics of the same device. A high peak saturation transconductance $G_{MSatMax}$ of ~490 µS/µm was achieved. At V_{GS} - V_{TH} = -1 V and V_{DS} = -1 V, this device demonstrates a high I_{ON} of 450 µA/µm as shown by $|I_D|$-V_{DS} plots in Fig. 4.38.

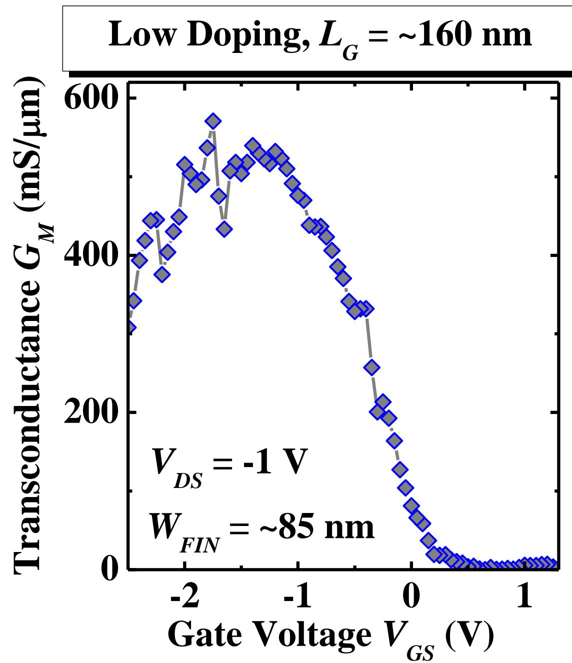


Fig. 4.37. G_M versus V_{GS} characteristics at V_{DS} = -1 V of a device with low fin doping, a L_G of ~160 nm, and a W_{FIN} of ~85 nm.

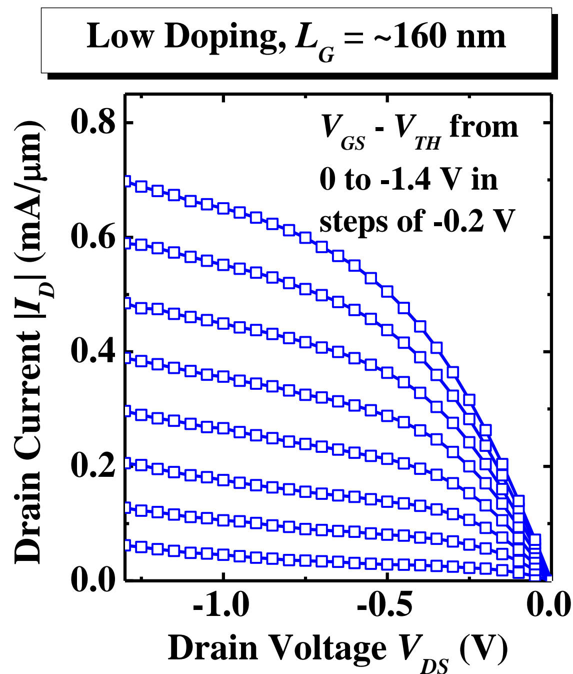
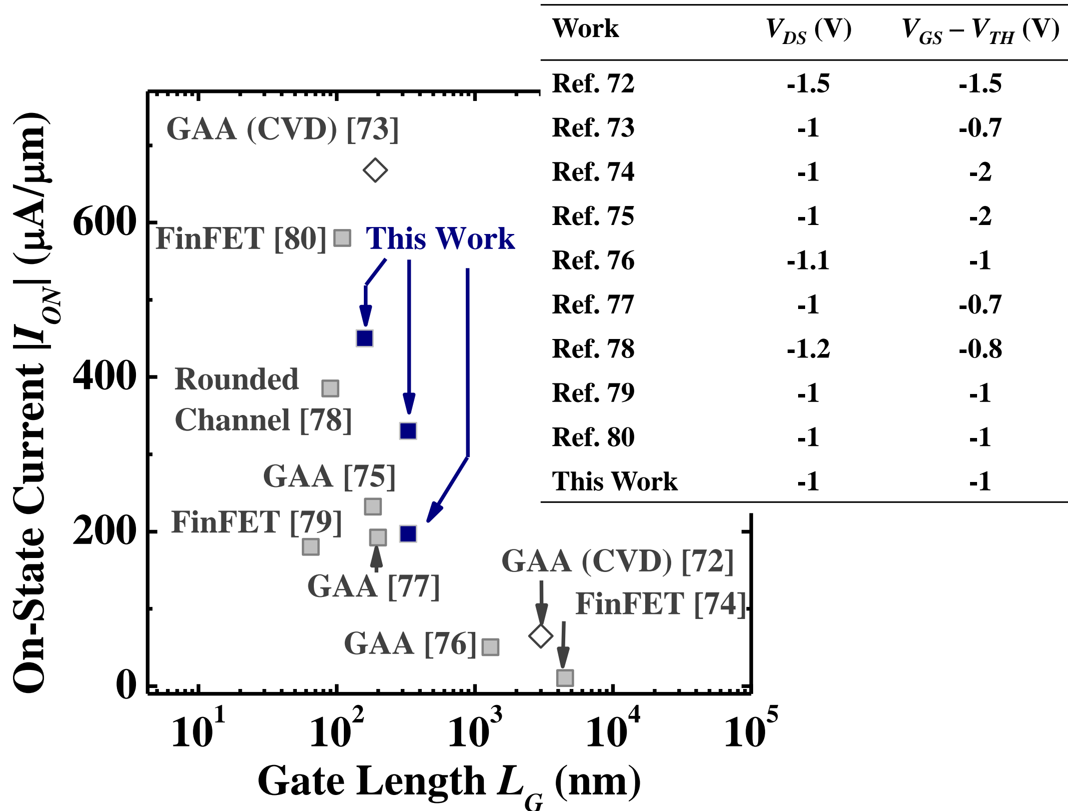


Fig. 4.38. $|I_D|$-V_{DS} characteristics of the same device, showing high I_{ON} of ~450 µA/µm at V_{GS} - V_{TH} = -1 V and V_{DS} = -1 V.



Work	V_{DS} (V)	$V_{GS} - V_{TH}$ (V)
Ref. 72	-1.5	-1.5
Ref. 73	-1	-0.7
Ref. 74	-1	-2
Ref. 75	-1	-2
Ref. 76	-1.1	-1
Ref. 77	-1	-0.7
Ref. 78	-1.2	-0.8
Ref. 79	-1	-1
Ref. 80	-1	-1
This Work	-1	-1

Fig. 4.39. Comparison of on-state current I_{ON} of the devices in this work with other Ge multiple-gate devices in the literature at similar V_{DS} and gate over-drive [72-80]. I_{ON} is among the highest for transistors fabricated by top-down approaches (in squares) [74-80]. Transistors fabricated using bottom-up approaches (Ge nanowire grown by CVD) [72, 73] are plotted in diamonds.

4.4.7 Benchmarking of Ge MuGFETs

Drive current performances of Ge MuGFETs in this work are compared with those Ge MuGFETs reported in the literature at similar but not exactly the same V_{DS} and gate over-drive [72-80] [see I_{ON}-L_G (log scale) plot in Fig. 4.39]. V_{DS} and gate over-drive used in each report are shown in the inset of Fig. 4.39. All current values are normalized by W_{EFF} or perimeter for fair comparison. Devices reported by Ref. 61 and 62 were fabricated by bottom-up methods (i.e. Ge fins were formed by CVD

method and no etching was used). Devices in the other publications [74-79] were formed by top-down fabrication techniques which are more compatible with the existing CMOS manufacturing processes. Ref. 67 reported I_{ON} of 385 μA/μm at V_{DS} = -1.2 V and $V_{GS} – V_{TH}$ = -0.8 V. At V_{DS} = -1.2 V and $V_{GS} – V_{TH}$ = -0.8 V, our device has an I_{ON} of ~380 μA/μm. The on-state currents achieved in the current work are among the highest for Ge MuGFETs fabricated by top down approaches, which could be partially attributed to the high quality of GeOI substrate, good gate stack formed, and low S/D resistance.

4.5 Summary

In conclusion, we demonstrated the integration of high performance Ge Schottky barrier MuGFETs on GeOI substrate using CMOS compatible process modules in this Chapter. Operation of SBMOSFET was discussed. Detailed process flow to fabricate Ge MuGFETs using top-down approach was documented. Devices with high and low fin doping concentrations show good I_{ON}/I_{OFF} ratio and transconductance. The MuGFETs with high fin doping are demonstrated to have better short channel control, but the heavier fin doping degrades drive current and transconductance. A very high on-state current was reported for Ge MuGFETs. Further optimization of Ge MuGFETs fabrication process could lead to even better gate control while maintaining or even further improving the high drive current achieved. Ge MuGFET on GeOI substrates fabricated by a Si CMOS compatible fabrication process provides good scalability, and could be a good candidate for future CMOS applications.

Chapter 5

Germanium Multiple-Gate Field-Effect Transistor with *in situ* Boron Doped Raised Source/Drain

5.1 Background

As discussed in Chapter 4, Ge is a promising alternative channel material for sub-14 nm complementary metal-oxide-semiconductor (CMOS) technology, due to its high carrier mobilities and process compatibility with Si CMOS. High performance Ge devices have been fabricated on either Ge bulk or GeOI substrates. The Multiple-Gate Field-Effect Transistor (MuGFET) or FinFET architecture offers excellent control of short channel effects [66] and has been adopted at the 22 nm technology node and beyond [67]. To achieve higher drive current and better control of short-channel effects, Ge MuGFETs have been realized by various techniques in the past a few years [72-74, 76-78, 151].

FinFET or MuGFET structures employing narrow fins are known to have high series resistance due to the small contact area of source/drain (S/D) region. Besides the adoption of metallic S/D structure to reduce series resistance as discussed in Chapter 4, epitaxial raised source/drain (RSD) structure was also demonstrated to reduce the series resistance of Si MuGFETs by increasing the S/D contact areas [70, 180]. Although the RSD structure is widely used in Si MOSFETs or MuGFETs [65, 70, 181-183], there are few publications on Ge MOSFETs with RSD for performance

enhancement in the literature [54, 184]. R. Pillarisetty *et. al.* of Intel reported high performance Ge planar p-FETs with *in-situ* p^+ doped Si_xGe_{1-x} RSD [54]. H.-Y. Yu *et. al.* of Stanford University reported planar Ge gate last n-MOSFETs with *in-situ* n^+ doped Ge S/D [184]. To the author's best knowledge, there was no exploration of Ge MuGFETs or FinFETs on GeOI substrate with RSD structure in the literature at the time when this thesis was being written.

The performance of Ge MuGFETs with NiGe metallic S/D was studied in Chapter 4. In this Chapter, we report the first demonstration of p-channel Ω-gate Ge MuGFET with *in situ* boron (B) doped RSD. High-quality GeOI substrates were used as starting substrates. Process development of Ge:B epitaxial growth on patterned GeOI samples is reported. Heavily B-doped raised Ge S/D is successfully integrated in Ge MuGFETs. Electrical characteristics of Ge MuGFET with RSD structure are discussed.

5.2 Epitaxial Growth of Ge on Patterned GeOI Substrates

It was demonstrated that Ge out diffusion at moderate temperature (≥ 400 ℃) into high-k dielectrics of Ge MOS capacitors (MOSCAPs) results in higher interface charge density and higher gate leakage current [157, 185-190]. In order to be integrated into Ge MOSFETs, epitaxial growth of raised Ge should preferably be done at temperature less than 400 to 500 ℃ to avoid Ge diffusion through Si or GeO_2 passivation layer. Epitaxial growth of Ge on GeOI substrates was developed at temperature ranging from ~300 to ~450 ℃ in this work.

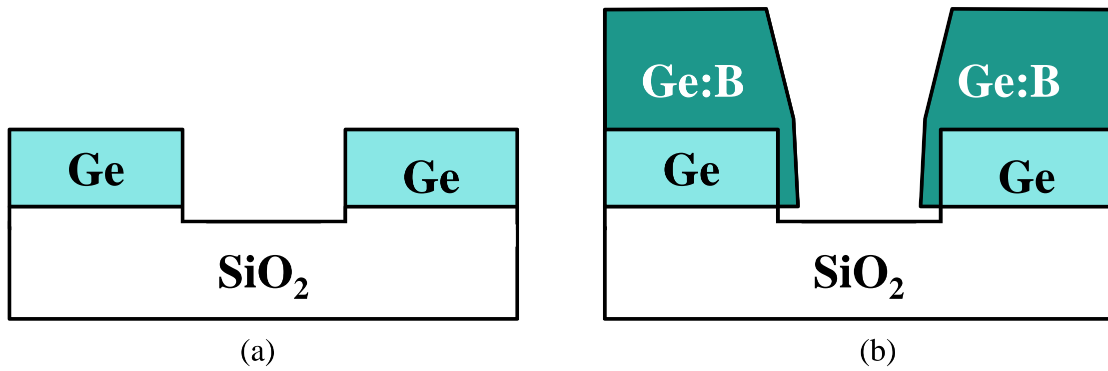


Fig. 5.1. Patterned GeOI structure schematic (a) before, and (b) after raised Ge:B growth.

High quality 8-inch Germanium-on-insulator (GeOI) wafers manufactured by SmartCut™ technology were used as starting substrates. GeOI test samples were first patterned using optical lithography, and the exposed Ge regions were dry-etched using chlorine-based plasma chemistry. The photoresist was stripped in oxygen plasma. The samples were then cleaned by dilute hydrofluoric acid DHF (1:100) for 100 s before being loaded into an ultra-high vacuum (UHV) tool for epitaxial growth of Ge. The GeOI sample structure before and after raised Ge:B growth are shown in Fig. 5.1 (a) and (b), respectively. Fig. 5.2 (a) shows a top-view scanning electron microscopy (SEM) image of a patterned GeOI sample before epitaxial growth.

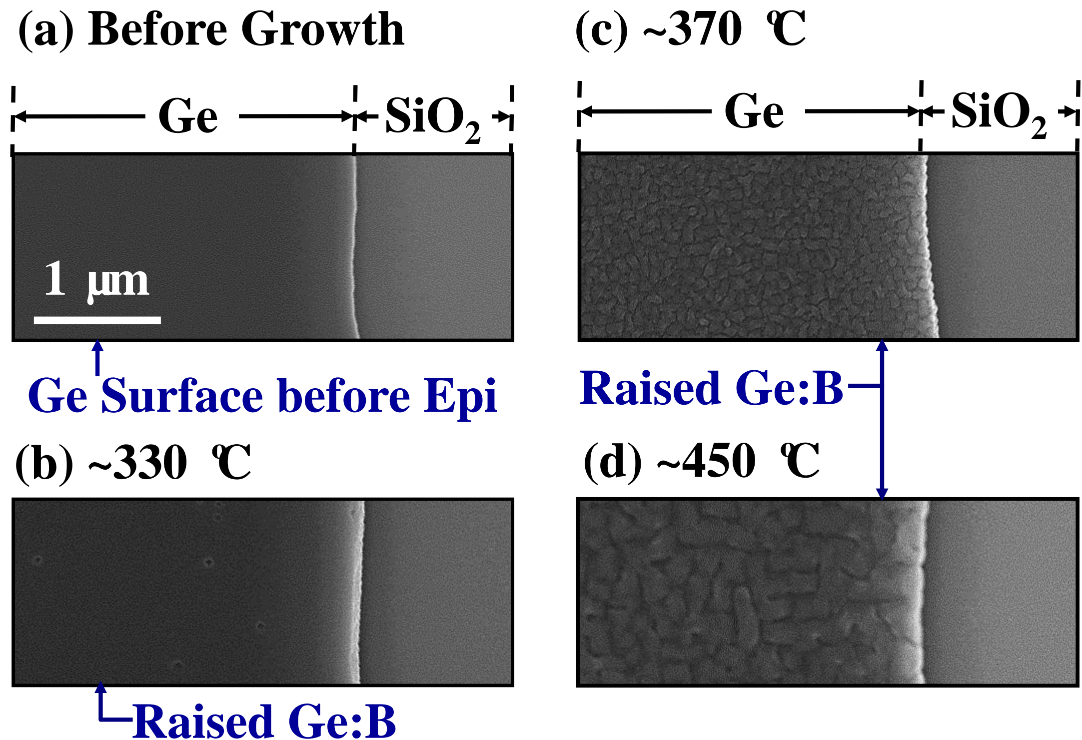


Fig. 5.2. Top-view SEM images of GeOI samples (a) without Ge growth, and with Ge epitaxial growth at (b) ~330 ℃, (c) ~370 ℃, and (d) ~450 ℃. All SEM images have the same magnification. Growth temperature of ~330 ℃ leads to the best Ge crystalline quality.

Fig. 5.3 shows the chamber configuration of the UHV tool used in this work for raised Ge:B growth. After surface cleaning, samples were transferred from cleaning chamber to growth chamber without breaking vacuum. It is very important to maintain vacuum when transferring samples to prevent any native oxide formation on Ge surfaces, as the oxide will prevent Ge:B growth.

In situ Sulfur Hexafluoride (SF_6) plasma clean was performed first in the UHV tool in hydrogen (H_2) ambient for 30 s with a RF power of 200 W to remove any native oxide on the Ge surface. The flow rates for SF_6 and H_2 were 10 cubic centimeters per minute (sccm) and 500 sccm, respectively. Selective growth of Ge

using Germane (GeH_4) was then performed in the growth chamber of the same UHV system without breaking the vacuum. Diborane (B_2H_6) gas was also introduced during growth to dope the Ge layer grown with a high concentration of B. Different growth temperatures were used to investigate the effect of temperature on Ge:B growth, while the gas flow rates of GeH_4 and B_2H_6 were fixed at 6:1 during growth.

Ge:B growth rates on Ge(001) surface of GeOI samples was found to increase with temperature in this work, as illustrated by Fig. 5.4. The thickness of the Ge:B grown is measured by a step profiler. High decomposition rate of GeH_X and fast desorption of H_2 from the growth surface at an elevated temperature is responsible for the enhanced growth rate.

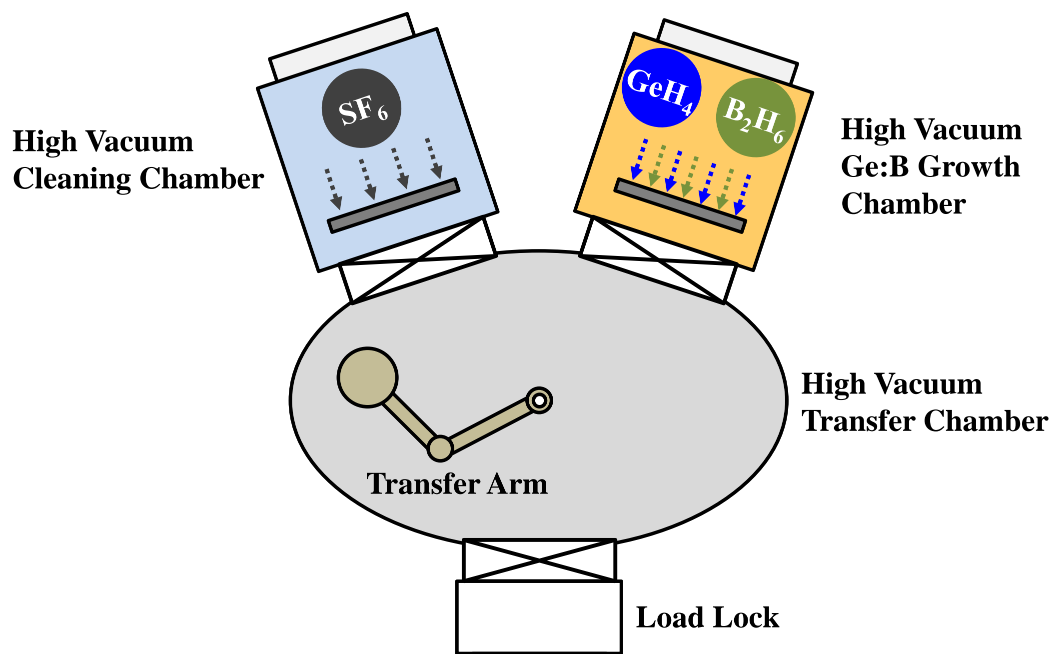


Fig. 5.3. Chamber configuration of the UHV tool used for epitaxial growth of Ge:B. Samples were transferred from cleaning chamber to growth chamber without breaking vacuum.

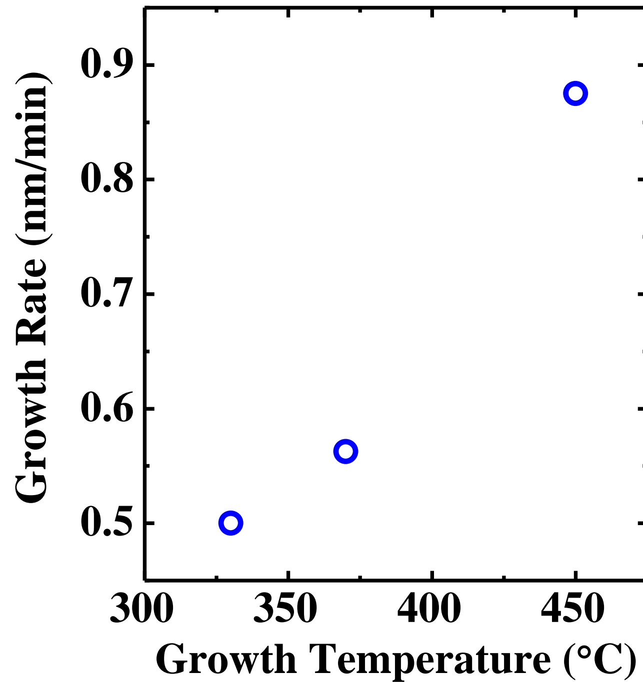


Fig. 5.4. Ge:B growth rates on Ge(001) surface of GeOI substrates at different temperatures. Higher temperature results in higher growth rate.

Fig. 5.2 (b), (c) and (d) show top-view SEM images of three GeOI samples with Ge:B epitaxial growth at ~330 ℃, ~370 ℃, and ~450 ℃, respectively. The growth of Ge:B by the UHV tool is highly selective for all temperatures. No Ge is grown on SiO_2 regions, which is confirmed by both SEM inspection and electrical characterization by probing the p^+ Ge grown and neighboring SiO_2 regions. It could be observed from the SEM images that the growth temperature of ~330 ℃ gives the best surface quality, while higher growth temperature of ~370 ℃ and ~450 ℃ lead to Ge layers with very rough surfaces which may negatively affect the subsequent metallization [nickel germanide (NiGe) formation] step. Y. Moriyama *et. al.* [191], T. R. Bramblett *et. al.* [192], and H. Akazawa *et. al.* [193] also separately reported that

higher growth temperature resulted in a rougher surface. The size of the "grain" formed at ~370 ℃ and ~450 ℃ were found to increase with temperature, as illustrated by Fig. 5.2 (c) and (d). At a low temperature of ~330 ℃, the energy of Ge adatoms is low, and the Ge surface morphology is maintained flat during the layer-by-layer growth. Higher growth temperature, on the other hand, results in highly mobile Ge adatoms with high surface diffusion [192, 193], and two-dimensional nucleation could take place everywhere on the Ge surface [192]. The non-uniform nucleation results in (113) facet formation which in turn leads to rough surface topologies.

Transmission electron microscopy (TEM) analysis was performed to further examine the quality of Ge:B grown at ~330 ℃. TEM image in Fig. 5.5 (a) and HRTEM image in Fig. 5.5 (b) confirm that the epitaxial growth of Ge:B on Ge at ~330 ℃ is single crystalline. The growth temperature of ~330 ℃ was selected for device integration, as this low temperature results in good surface quality and does not degrade the gate stack quality.

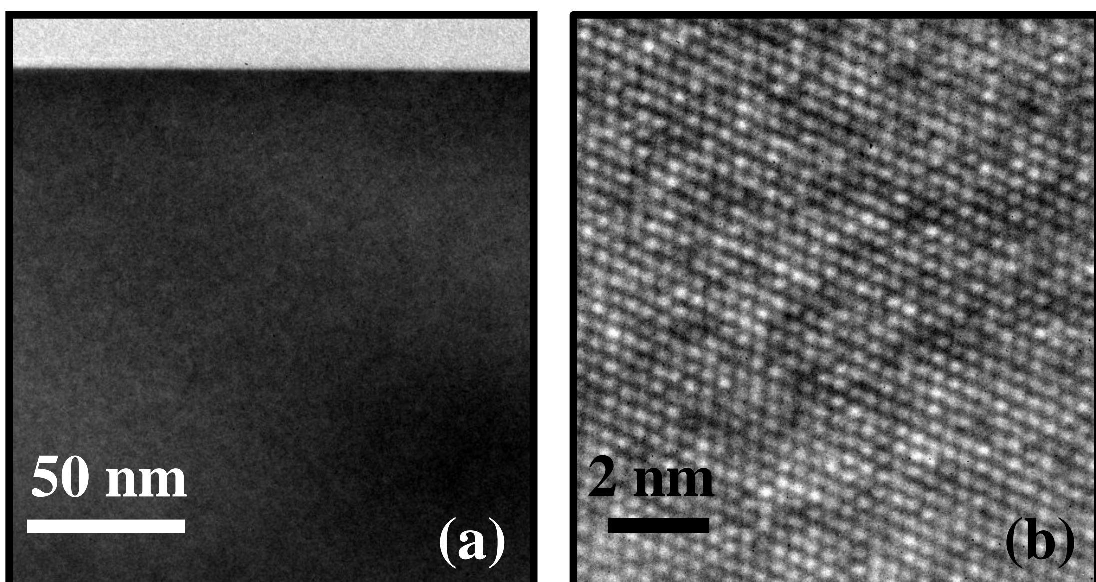


Fig. 5.5. (a) Zoomed-out TEM and (b) high resolution TEM (HRTEM) image of Ge:B growth on Ge substrate. Good crystalline quality was observed.

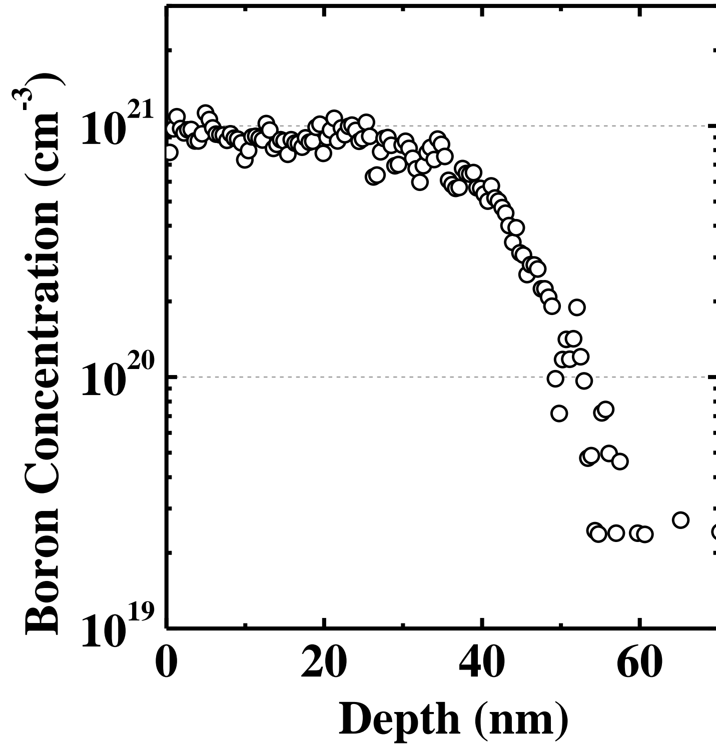
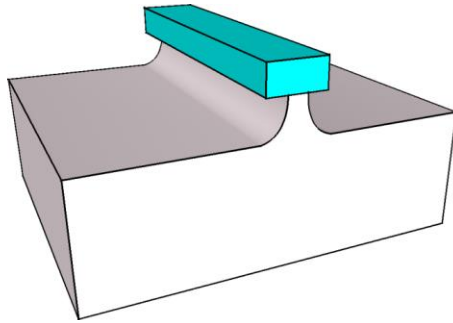
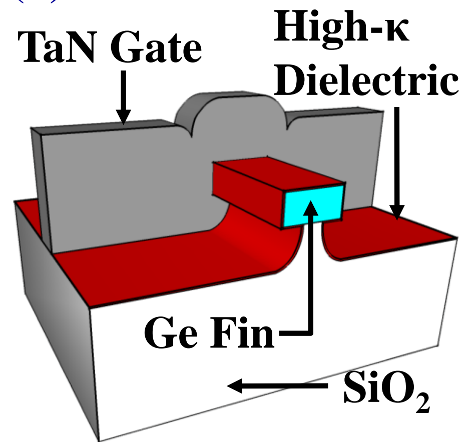
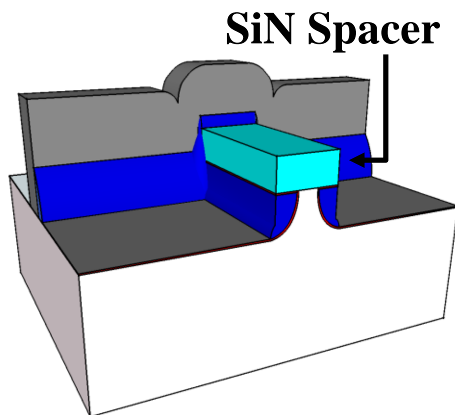


Fig. 5.6. SIMS analysis showing B profile of Ge:B grown on the GeOI sample at ~330 ℃. High concentration of B (~9×10^{20} cm^{-3}) was achieved by *in situ* doping.

Secondary ion mass spectrometry (SIMS) analysis was performed on the sample with Ge:B grown on Ge at ~330 ℃. Fig. 5.6 shows the B concentration versus depth profile, indicating a high concentration of B (~9×10^{20} cm^{-3}) in the grown Ge:B layer. The active B concentration was estimated to be ~6×10^{19} cm^{-3} by micro four point probe measurement.







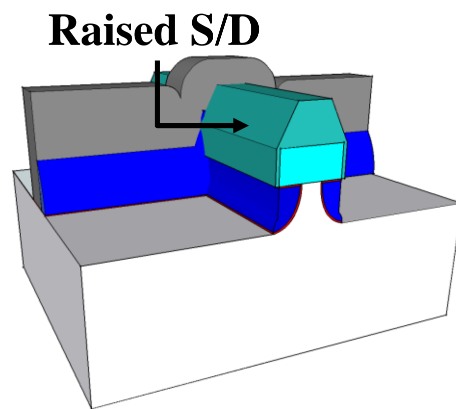


Fig. 5.7. Three-dimensional (3D) schematics showing key process steps in the fabrication of Ge MuGFETs with RSD, including (a) Fin formation, (b) TaN etch, (c) SiN spacer formation, and (d) Raised S/D growth.

5.3 Device Fabrication

Ge MuGFETs were fabricated using similar process flow as described in Chapter 4 and Ref. [151], except for additional SiN spacer formation and RSD growth processes. GeOI sample with a Ge layer thickness of ~35 nm was used as starting substrate for device fabrication. The sample was doped n-type using a 30 keV phosphorus (P) implant and annealed at 600 °C for 60 s for dopant activation. A box-like P profile was achieved after dopant activation, as demonstrated in Chapter 4. Ge

fins were defined by electron beam lithography (EBL) and dry etch, followed by a pre-gate cyclic DHF (1:50) and deionized water (DIW) clean. The sample structure after DHF clean is illustrated by Fig. 5.7 (a).

The samples were then loaded into the UHV tool for further surface cleaning by SF_6 plasma, followed by *in situ* Si_2H_6 passivation at ~370 ℃ to form a Si passivation layer. The Si passivation layer was partially oxidized, forming SiO_2/Si passivation layer on top of Ge. Gate stack consisting of ~4 nm HfO_2 and ~110 nm TaN was deposited by atomic layer deposition (ALD) and magnetron sputtering, respectively, followed by gate patterning by EBL. A two-step gate etch process was used in this work to remove TaN spacer along the Ge fins in order to avoid any short between gate and S/D regions and enable growth of Ge on the sidewalls of Ge fin. The recipes used for TaN gate etch and TaN spacer removal were described in Chapter 4. Fig. 5.7 (b) shows a 3D schematic of the MuGFET after gate etch and TaN spacer removal.

Silicon nitride (SiN) spacer was formed by depositing SiN on the sample using plasma-enhanced chemical vapour deposition (PECVD) and dry-etch using reactive-ion etching (RIE). DHF (1:100) etch for 100 s was then performed to remove the high-κ layer on S/D regions, clean the Ge surface, and trim the SiN spacer down to ~10 nm and below. Note the RIE etch and DHF trimming of SiN spacer were both time controlled. PECVD SiN film etch rates using RIE and DHF were calibrated using blanket SiN on Si samples which have similar size as the device sample. The final SiN spacer thickness was estimated by measuring the SiN thickness on the blanket samples using ellipsometer. The 3D device schematic after spacer formation and trimming is illustrated in Fig. 5.7 (c).

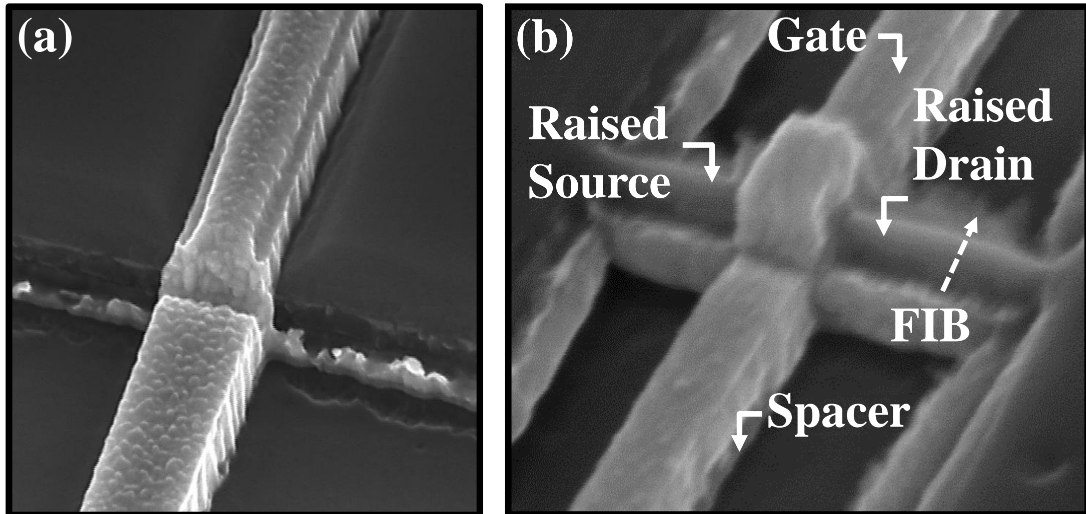


Fig. 5.8. (a) A tilted-SEM image of a planar test transistor with a long gate width of ~50 µm after RSD growth, indicating visible Ge raised S/D growth. (b) A tilted-SEM image of a MuGFET after RSD growth, indicating the SiN spacer, the TaN gate, and the RSD regions.

The sample was then loaded into the UHV system for further SF_6 plasma cleaning for 50 s which recess etched around ~2 to 3 nm Ge. The sample was transferred to the growth chamber of the UHV tool for Ge:B RSD epitaxial growth at ~330 ℃. The gas flow rates of were kept the same as described in the previous Section. Lastly, forming gas anneal (FGA) was performed in a furnace with the flow rate of H_2 over nitrogen N_2 equals to 1:9 at 300 ℃ for 20 mins to reduce off-state leakage current [60]. This completed the device fabrication. Fig. 5.7 (d) shows a 3D schematic illustrating the final device structure after RSD growth.

Fig. 5.8 (a) shows a tilted-view SEM image of a planar test transistor structure with large device width on GeOI substrate, clearly portraying the Ge grown on top of the original Ge surface. A tilted-view SEM image in Fig. 5.8 (b) depicts a MuGFET

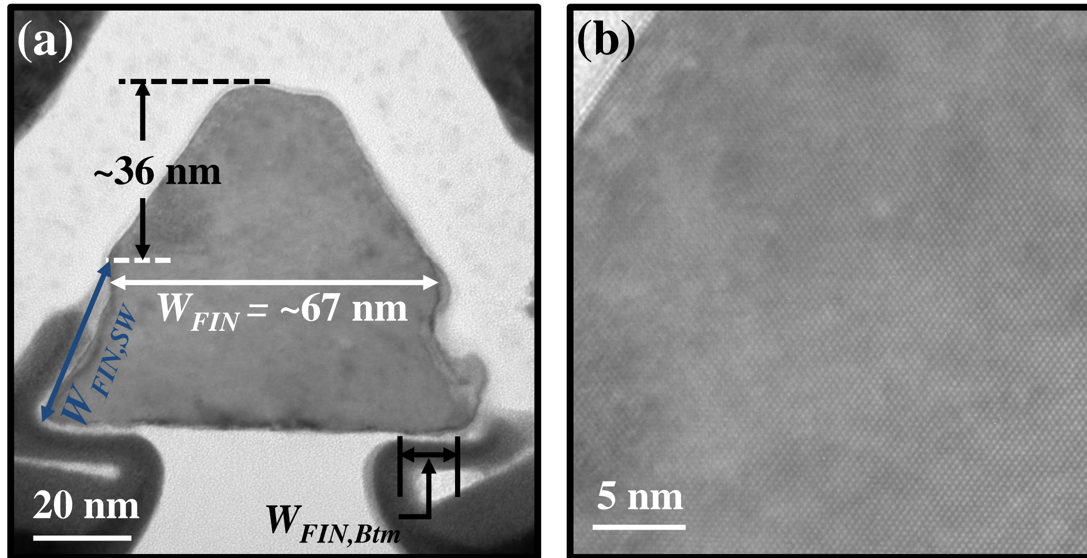


Fig. 5.9. (a) A TEM image of the Ge fin after selective growth of Ge:B raised S/D, showing ~36 nm Ge grown. (b) High resolution TEM of the RSD Ge region, showing good crystalline quality.

after RSD growth, showing the SiN spacer, the TaN gate, and the RSD regions. A TEM image of the Ge fin after raised S/D growth is shown in Fig. 5.9 (a). The original fin width W_{FIN} measured from top fin surface and fin height H_{FIN} are ~67 nm and ~32 nm, respectively. ~36 nm B doped Ge was grown. HRTEM image shown in Fig. 5.9 (b) confirms that the Ge RSD is single crystalline. MuGFETs with a fin width W_{FIN} of ~67 nm were fabricated.

It was observed that the thickness of Ge:B grown on the sidewall of the Ge fin is much thinner as compared with that on the top Ge(001) surface. Various studies on silicon (Si) or silicon germanium (SiGe) epitaxial growth on Si in the literature reported that Si or SiGe growth rate is faster on Si(001) surface, as compared with Si(110) and Si(111) surfaces [194-197]. M. Okada *et. al.* [195] and M. L. Lee *et. al.*

[196] attributed the slower growth rate on Si(110) or Si(111) to the slower desorption rate of hydrogen for Si(110) or Si(111), as compared with that for Si(001). The possibly higher hydrogen coverage on the growth surface of Si(110) or Si(111) prohibits growth of Si or SiGe on these surfaces, resulting in smaller growth rate. Similarly, it could be expected that the hydrogen desorption rate on Ge(110) would be slower than that for Ge(001), which in turn leads to smaller growth rate of Ge:B on Ge(110) surface, as compared with Ge(001). Although the sidewalls of the Ge fin are not perfectly Ge(110), the same analogy could probably be applied to the case of Ge:B growth on Ge fin sidewalls. As long as the growth of Ge:B on the top Ge(001) surface is thick enough to meet the requirement of increasing the S/D contact area, the slower Ge:B growth rate on the sidewalls of Ge fin would not hinder the integration of RSD into Ge MuGFETs.

5.4 Results and Discussion

5.4.1 Electrical Characterization of Ge MuGFETs with RSD

The inversion capacitance C versus voltage V (C-V) plot at a frequency f of 100 kHz of a long channel planar transistor fabricated using the same gate stack formation process that was used for the MuGFETs is shown in Fig. 5.10. The capacitance equivalent thickness (CET) of this device is ~1.8 nm.

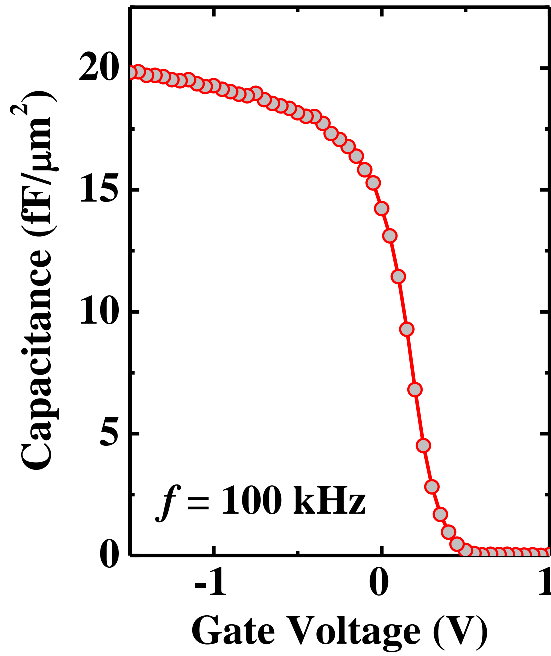


Fig. 5.10. Inversion *C-V* measured at a frequency *f* of 100 kHz of a long channel planar transistor fabricated using the same gate stack formation process as the MuGFETs.

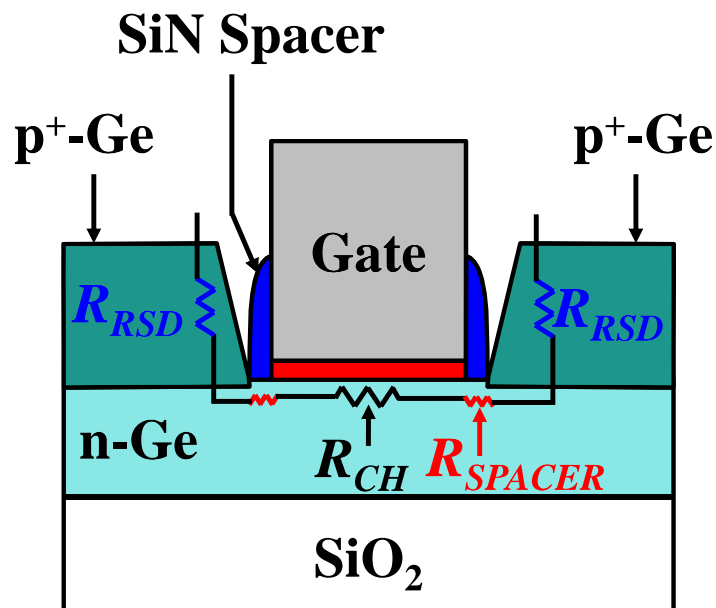


Fig. 5.11. Two-dimensional (2D) schematic showing the cross-sectional structure of the Ge MuGFET with RSD. RSD resistance R_{RSD}, resistance due to lightly n-type doped Ge under the spacer R_{SPACER}, and channel resistance R_{CH} are shown.

Fig. 5.11 shows a 2D schematic of the final device structure, illustrating the various resistance components. As the main motivation of this work is to examine the feasibility of integrating RSD into Ge MuGFETs, the Ge region under the spacer was not implanted with B for process simplicity. The control of SiN spacer trimming is important to reduce the resistance due to the Ge regions under the spacers, especially when the Ge regions under the spacers are not p^+ doped. A slim spacer is desirable to reduce the resistance due to the lightly n-type doped regions under the spacers, R_{SPACER}. Etching the SiN spacer too aggressively in DHF, on the other hand, could have the spacer completely removed. This will lead to short between the metal gate and RSD.

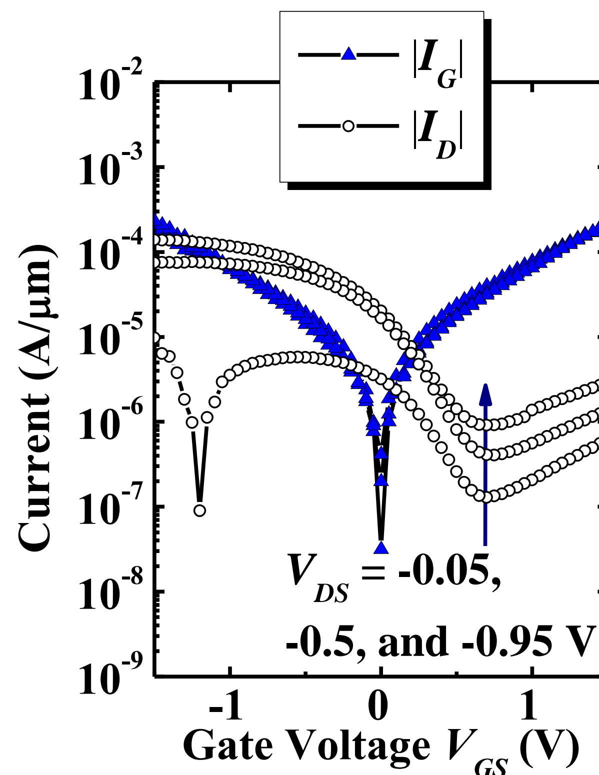


Fig. 5.12. $|I_D|$ and $|I_G|$ versus V_{GS} characteristics of a Ge MuGFET with RSD. SiN spacer was fully etched before Ge:B growth, which results in gate to S/D short.

The MuGFETs fabricated were characterized by direct probing on the metal gate and B doped p^+ S/D pads. Fig. 5.12 shows the drain current $|I_D|$ and gate leakage current $|I_G|$ versus gate voltage V_{GS} plots for a Ge MuGFET with RSD. The SiN spacer of this MuGFET was completely removed due to excessive dip in DHF before the sample was loaded into the UHV tool for Ge:B growth. The device was characterized at drain voltage V_{DS} of -0.05 V, -0.5 V and -0.95 V. It could be observed that the device exhibits high gate leakage current I_G. The gate leakage current mainly flows from the gate electrode to the source terminal due to the short caused by Ge:B growth.

Fig. 5.13 shows $|I_D|$-V_{GS} plots for a Ge MuGFET with RSD and slim SiN spacer. The existence of the slim SiN spacer prevents short between gate electrode and p^+ Ge:B RSD. The device was measured at V_{DS} of -0.05 V, -0.5 V and -0.95 V, and demonstrates good transfer characteristics. The gate length L_G, W_{FIN}, and

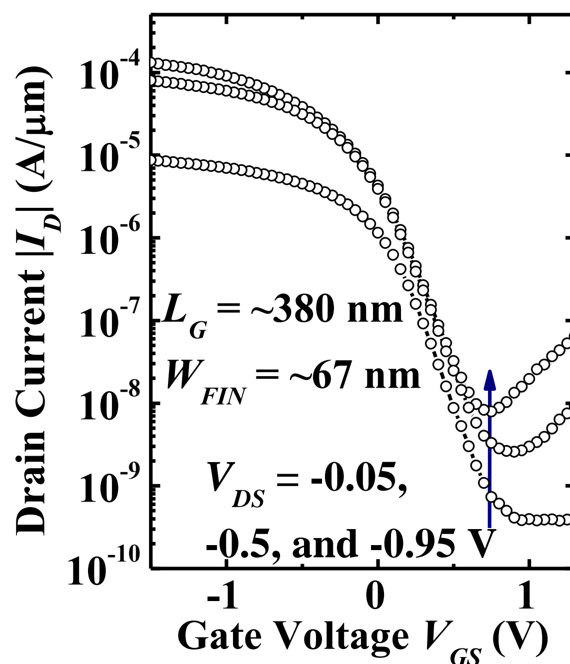


Fig. 5.13. $|I_D|$ versus V_{GS} characteristics of a Ge MuGFET with RSD and slim SiN spacer. I_{ON}/I_{OFF} ratio of more than 10^4 was achieved for all V_{DS}.

effective gate width W_{EFF} are ~380 nm, ~67 nm, and ~167 nm, respectively. W_{EFF} is the sum of W_{FIN}, $2\times W_{FIN,Btm}$ and $2\times W_{FIN,SW}$, as indicated in Fig. 5.9 (a). The subthreshold swing (S) at V_{DS} of -0.05 V and -0.95 V are ~190 mV/decade and ~200 mV/decade, respectively. Drain induced barrier lowering (DIBL) of this device is ~106 mV/V, demonstrating good short channel control. High on-state current over off-state current (I_{ON}/I_{OFF}) ratio of more than 10^4 was achieved for V_{DS} of -0.05 V,-0.5 V, and -0.95 V, where I_{OFF} was taken as the minimum drain current from the $|I_D|$-V_{GS} plots.

The $|I_G|$-V_{GS} plot shown in Fig. 5.14 demonstrates that the device with SiN spacer before RSD growth has much lower I_G, as compared with that of the device shown in Fig. 5.12 of which the gate and S/D are shorted. Transconductance G_M-V_{GS} characteristics at various V_{DS} of the same device are shown in Fig. 5.15. Peak G_M of ~108 μS/μm and 7.2 μS/μm were achieved at V_{DS} = -0.95 V and -0.05 V, respectively.

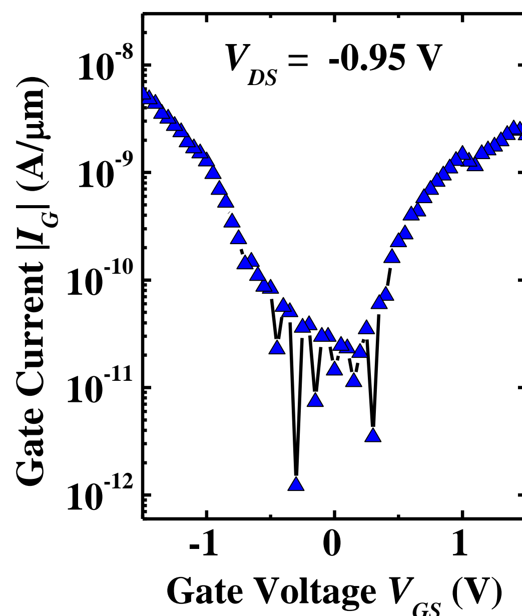


Fig. 5.14. $|I_G|$ versus V_{GS} characteristics of a Ge MuGFET with RSD and slim SiN spacer. Low gate leakage current was achieved.

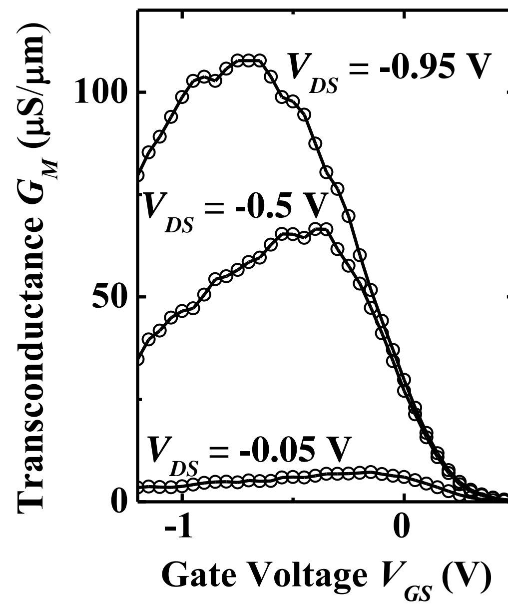


Fig. 5.15. Transconductance G_M-V_{GS} characteristics at V_{DS} of -0.05 V, -0.5 V and -0.95 V of the same device. At V_{DS} = -0.95 V, a peak G_M of ~108 μS/μm was obtained.

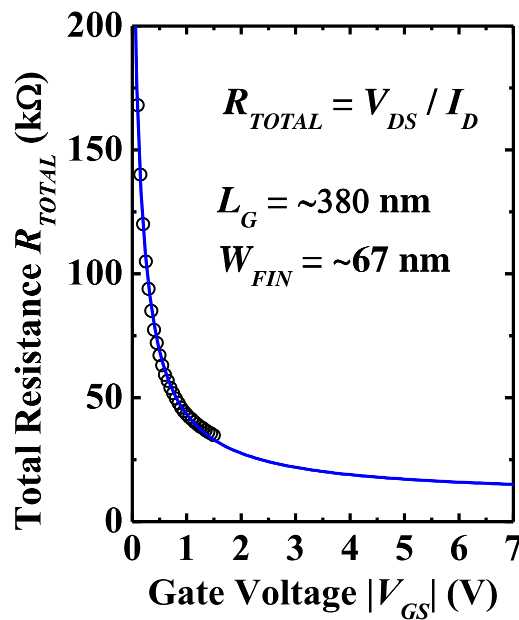


Fig. 5.16. R_{TOTAL}-|V_{GS}| plot at V_{DS} = -0.05 V of the MuGFET with RSD. R_{TOTAL} = V_{DS} / I_D. The blue line is the best fitted line.

Total resistance R_{TOTAL}-|V_{GS}| plot at V_{DS} = -0.05 V of the same MuGFET with RSD structure is shown in Fig. 5.16. R_{TOTAL} is defined as V_{DS} divided by I_D. The blue

line is the best fitted line. At $|V_{GS}|$ = 7 V, the device shows a series resistance R_{SD} of ~15 kΩ, or ~2.5 kΩ·μm after normalization with respect to W_{EFF} of ~167 nm. The relatively high series resistance of the device is partially attributed to the absence of metal contacts on the p^+ S/D regions, the relatively large probe-to-gate-edge spacing of ~10 μm, and the lightly n-doped Ge regions under the SiN spacers.

$|I_D|$-V_{DS} characteristics of the MuGFET are shown in Fig. 5.17. The threshold voltage V_{TH} was extracted by maximum transconductance method from $|I_D|$-V_{GS} plot. At a gate overdrive V_{GS} - V_{TH} = -1.0 V and V_{DS} = -1.0 V, the device with a gate length L_G of ~380 nm demonstrates an I_{ON} of 101 μA/μm. Employment of self-aligned NiGe on the raised p^+ S/D regions and doping the Ge regions under the spacers could further reduce the series resistance and improve the drive current of the Ge MuGFETs.

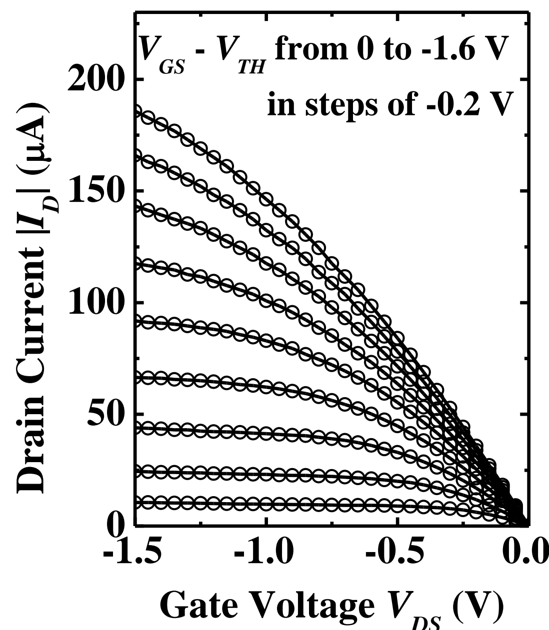


Fig. 5.17. $|I_D|$-V_{DS} characteristics of the MuGFET. At a gate overdrive V_{GS} - V_{TH} = -1 V and V_{DS} = -1 V, the device with a L_G of ~380 nm demonstrates an I_{ON} of 101 μA/μm.

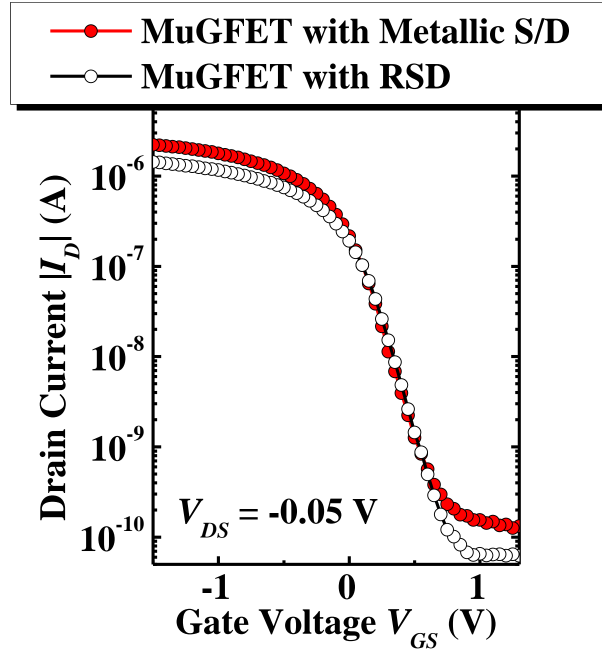


Fig. 5.18. |I_D|-V_{GS} characteristics of two Ge MuGFETs with different S/D structures at V_{DS} = -0.05 V. Ge MuGFET with metallic S/D (red) shows similar subthreshold swing as Ge MuGFET with RSD (black), while the later has slightly smaller leakage current.

5.4.2 Comparison of Ge MuGFETs with Different S/D Structures

In this Subsection, the performance of the Ge MuGFETs with RSD is compared with Ge MuGFETs with Schottky barrier (SB) metallic S/D. Fig. 5.18 shows |I_D|-V_{GS} characteristics of two Ge MuGFETs with different S/D structures at V_{DS} = -0.05 V. The two devices are with the same L_G of ~380 nm, and similar W_{FIN}. Ge MuGFET with metallic S/D (red) shows similar subthreshold swing S as Ge MuGFET with RSD (black), indicating similar interface charge densities of these two devices. The later has smaller leakage current, which is believed to be due to lower revere leakage current of p-n junction, as compared with metal-semiconductor junction [2]. It should be noted that the drain current difference between these two devices could be due to a few factors, including S/D series resistance and CET

differences. The earlier is believed to be due to the different S/D structures, i.e. RSD versus metal S/D, used for the two device splits, while the latter is possibly caused by the ALD process variation. The CET of the MuGFET with RSD is ~1.8 nm while the CET for the device with metal S/D is ~1.7 nm, as reported in Chapter 4.

R_{TOTAL}-$|V_{GS}|$ plots of the same two devices shown in Fig. 5.19 indicate that the device with metallic S/D (red) has smaller R_{TOTAL} at a fixed V_{GS}, as compared with the Ge MuGFET with RSD (black). The solid black and red lines are the best fit lines for MuGFETs with RSD and metallic S/D, respectively. The larger R_{TOTAL} of the device with RSD could be attributed to the absence of metallization on top of p^+ Ge:B S/D regions, and the series resistance due to the lightly n-type doped Ge regions under the spacers, as illustrated in Fig. 5.11. The latter is believed to contribute significantly to the series resistance.

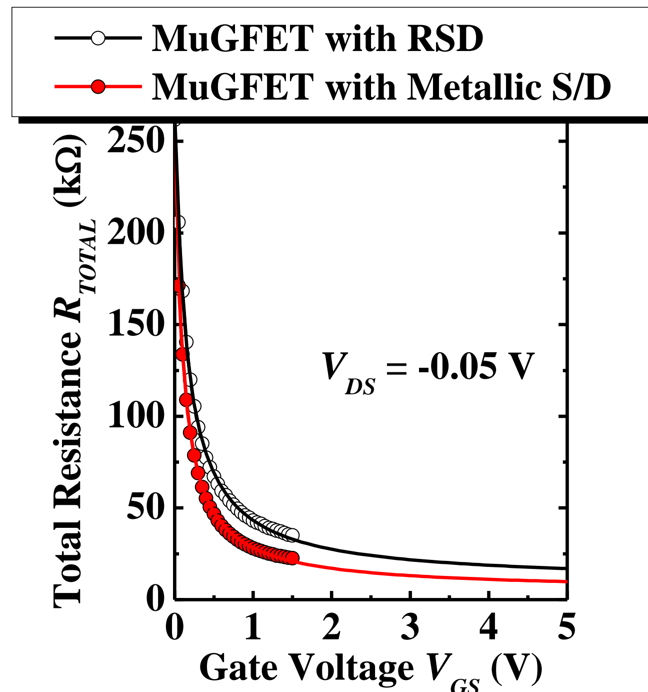


Fig. 5.19. R_{TOTAL}-$|V_{GS}|$ plots of the same two devices of Fig. 5.18, showing that the device with metallic S/D (red) has smaller R_{TOTAL} at a fixed V_{GS}, as compared with the Ge MuGFET with RSD (black).

Fig. 5.20 shows Technology Computer Aided Design (TCAD) simulation of source-channel band diagrams when the device with RSD is at off-state (black) and on-state (red). The SiN spacer width is ~4 nm. The n-type channel doping (including the Ge region under the spacer) and p-type S/D doping are 5×10^{17} and 5×10^{20} cm^{-3}, respectively. It could be observed that a small bump exists between the source and channel when the device is at on-state, which is due to the lightly doped Ge region under the SiN spacer. This is because that the lightly n-type doped Ge region under the SiN spacer is not controlled by the gate. The barrier will contribute to the series resistance. Fig. 5.21 compares on-state band diagrams of two devices with 4 nm and 9 nm SiN spacer. As the spacer becomes smaller, the barrier that the holes need to surmount in order to inject into the channel becomes smaller. Doping the Ge regions under the spacer will eliminate the barrier.

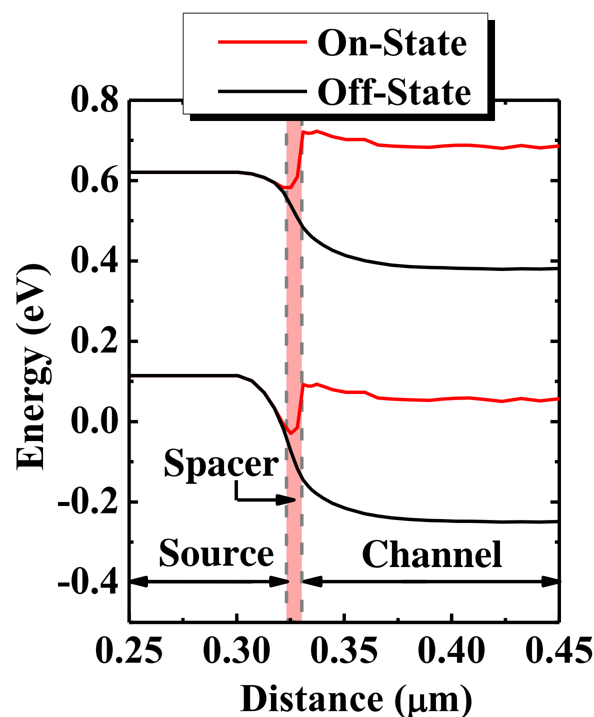


Fig. 5.20. TCAD simulated source-channel band diagrams when the device channel is at off-state (zero gate bias) and on-state (strong inversion). It could be observed that a small bump/barrier exists between the S/D and channel when the device is at on-state due to the lightly doped Ge region under the SiN spacer.

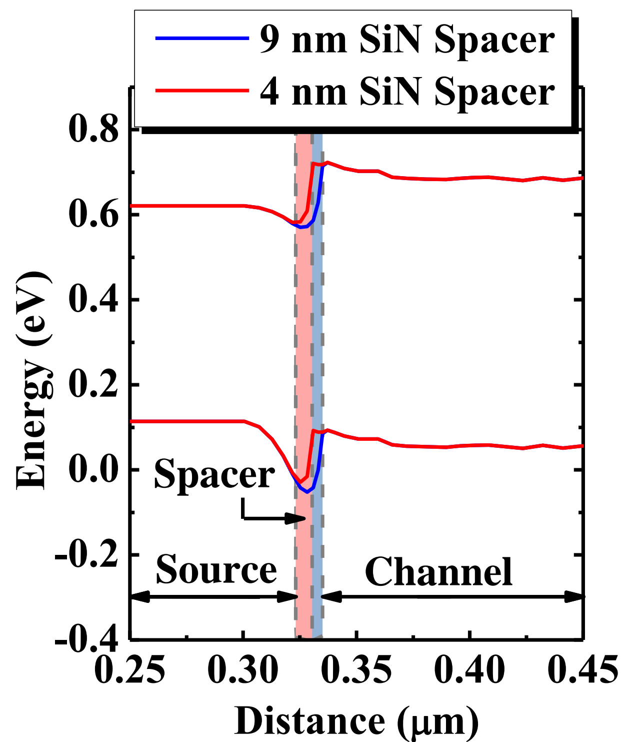


Fig. 5.21. On-state band diagrams of two devices with 4 nm and 9 nm SiN spacer. The barrier that the holes need to surmount in order to inject into the channel becomes smaller, as the spacer becomes smaller.

As the main motivation of this work is to examine the flexibility of integrating RSD into Ge MuGFETs, the S/D implant condition is not optimized yet. Further improvement of the S/D extension implant and successful integration of NiGe on RSD could further improve the device performance.

5.4.3 NBTI of Ge MuGFETs with RSD

Negative Bias Temperature Instability (NBTI) is an important reliability issue for state of the art p-FETs, as discussed in Chapter 3 of this thesis. NBTI of Ge MuGFETs with RSD was examined in this work to investigate the gate stack reliability of Ge MuGFETs. This is the first NBTI study of Ge MuGFET with Si

passivated high-κ/metal gate stack. Although NBTI of Ge planar MOSFETs with high- κ metal gate has been reported, there was no NBTI study on Ge FinFETs or MuGFETs prior to this study. DC measurement technique was employed in the current NBTI characterization of Ge MuGFETs to mainly study the slow component of NBTI degradation [32] (mainly interface trap generation effect, and some hole trapping effect) of Ge MuGFETs with high-κ dielectric. NBTI characterization was done by electrically stress the gate with a high voltage while keeping the S/D and the substrate terminals grounded. $|I_D|$-V_{GS} curves were collected at different time points by a semiconductor analyzer during the stress phase to examine the transistor characteristic shift due to NBT stress. Fig. 5.22 shows the measurement set up used in this NBTI study.

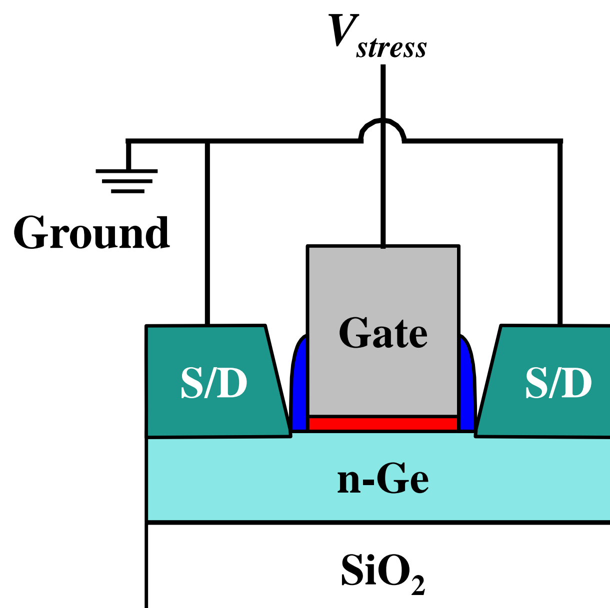


Fig. 5.22. NBTI characterization set up. The gate was electrically stressed with a large voltage V_{stress} while the S/D terminals were grounded. The device was stressed for 1000 s before the stress was removed to study the recovery behaviour.

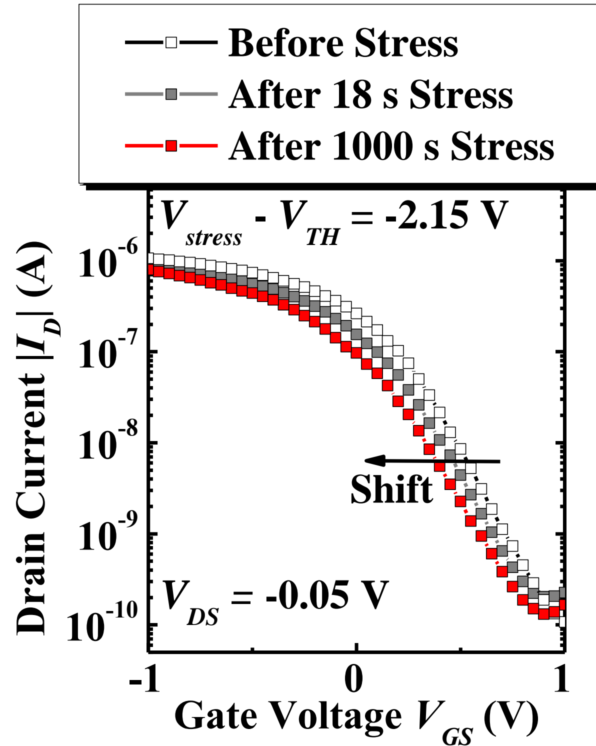


Fig. 5.23. $|I_D|$-V_{GS} characteristics at V_{DS} = -0.05 V of a Ge MuGFET before NBT stress, after being stress for 18 s, and after being stressed for 1000 s . V_{stress} - V_{TH} = -2.15 V.

Fig. 5.23 shows $|I_D|$-V_{GS} characteristics of a Ge MuGFET before NBT stress, after being stress for 18 s, and after being stressed for 1000 s. The gate length L_G of this device is ~330 nm. The NBT stress V_{stress} is applied such that V_{stress} - V_{TH} = -2.15 V. V_{DS} is biased at -0.05 V when measuring $|I_D|$-V_{GS}. It could be observed that $|I_D|$-V_{GS} curve shifts to the left with V_{TH} becoming more negative after NBT stress, indicating positive charge trapping and interface trap generation. The drain current I_D at a fixed V_{GS} was also observed to decrease after NBT stress. The increase of V_{TH} is believed to be caused by both interface trap generation and charge trapping [32], as discussed in Chapter 3. As the gate stack is TaN/HfO_2 on SiO_2/Si passivated Ge, the NBT degradation mechanism is similar with that of devices with SiO_2 or SiON gate dielectrics [198]. It should be noted that most of V_{TH} shift captured by DC

characterization technique is from interface state generation. The majority portion of hole trapping is believed to detrap very fast upon the removal of V_{stress}. As the measurement speed of DC characterization technique is not fast enough, majority part of V_{TH} shift caused by hole trapping will not be captured.

The S of the device is ~220 mV/decade before NBT stress, and becomes ~234 mV/decade after being stressed at V_{stress} - V_{TH} = -2.15 V for 1000 s. S of a MOSFET could be described by the following equation:

$$S = \ln(10)\frac{kT}{q}(1+\frac{C_{it}+C_D}{C_{ox}}) = \ln(10)\frac{kT}{q}(1+\frac{qD_{it}+C_D}{C_{ox}}), \qquad (5\text{-}1)$$

where C_{ox} is the gate oxide capacitance, C_D depletion capacitance, D_{it} is the interface trap density, and C_{it} is the interface traps capacitance with $C_{it} = qD_{it}$. The increase of S observed is believed to be due to interface trap generation caused by NBT stress [28].

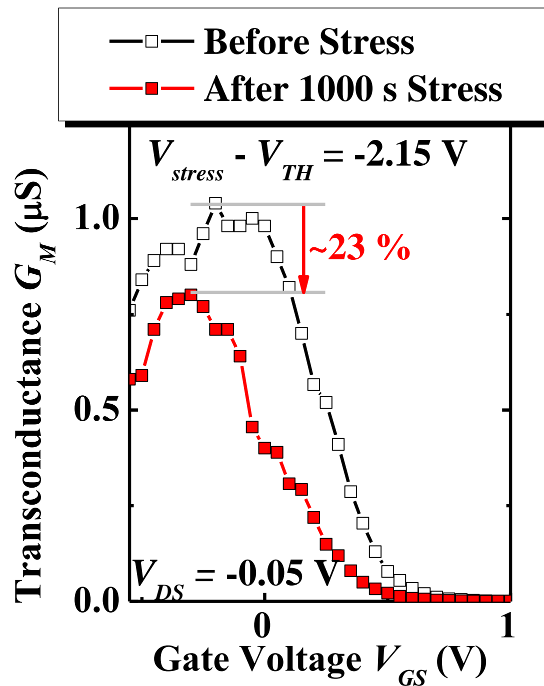


Fig. 5.24. G_M-V_{GS} characteristics of a Ge MuGFET before NBT stress, and after being stressed for 1000 s. 23 % G_M degradation was observed.

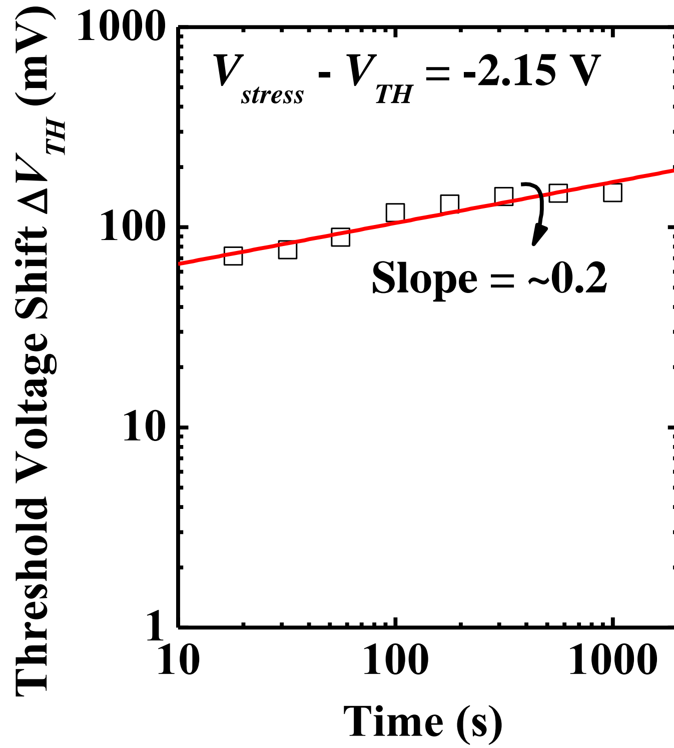


Fig. 5.25. Time evolution of threshold voltage shift ΔV_{TH}. V_{stress} - V_{TH} = -2.15 V. The power law slope extracted by linear fit ΔV_{TH}-time is ~0.2.

Transconductance G_M degradation due to NBT stress of 1000 s at V_{stress} - V_{TH} = -2.15 V is shown in Fig. 5.24. ~23 % G_M degradation was observed. Interface trap generation due to NBT stress could results in additional surface scattering, causing hole mobility to decrease [199]. The degradation of hole mobility could manifest as G_M degradation, which is based on the following equation:

$$G_M = \frac{W_G}{L_G} \mu_{eff} C_{OX} (V_{GS} - V_{TH}), \qquad (5\text{-}2)$$

Any mobility degradation will directly result in G_M reduction.

Time evolution of threshold voltage shift ΔV_{TH} of the device under the stress condition of V_{stress} - V_{TH} = -2.15 V is shown in Fig. 5.25. The red line is the best fit line. ΔV_{TH} increases as the stress time increases. The power law slope/exponent

obtained is ~0.2 which is similar for devices with SiO_2 or SiON gate dielectrics measured with DC technique [200].

Recovery behaviour of Ge MuGFET was also studied by measuring $|I_D|$-V_{GS} characteristics at V_{DS} = -0.05 V after removal of gate stress V_{stress}. Fig. 5.26 compares $|I_D|$-V_{GS} characteristics of a Ge MuGFET before NBT stress, after 1000 s stress, and after the stress was removed for 1000 s (1000 s recovery), demonstrating that the device recovered from NBT degradation once the gate stress was removed. *S* of the device was also observed to become smaller after 1000 s recovery, as compared with that after 1000 s stress.

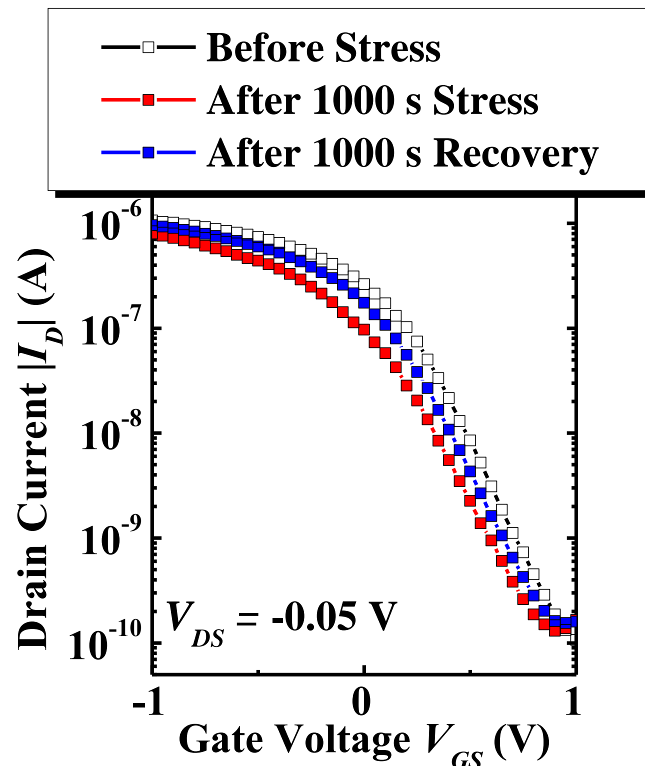


Fig. 5.26. $|I_D|$-V_{GS} characteristics of a Ge MuGFET before NBT stress, after 1000 s stress, and after 1000 s recovery.

A ~46 % G_M recovery was obtained 1000 s after the NBT stress was removed from the gate, as demonstrated by Fig. 5.27. G_M recovery rate $R_{GM,RC}$ was calculated as

$$R_{GM,RC} = \frac{G_{M,RC1000} - G_{M,ST1000}}{G_{M,0} - G_{M,ST1000}}, \tag{5-3}$$

where $G_{M,0}$, $G_{M,ST1000}$, and $G_{M,RC1000}$ are transconductance of the device before NBT stress, after 1000 s stress, and after 1000 s recovery. The G_M recovery indicates hole mobility recovery due to repassivation of interface traps.

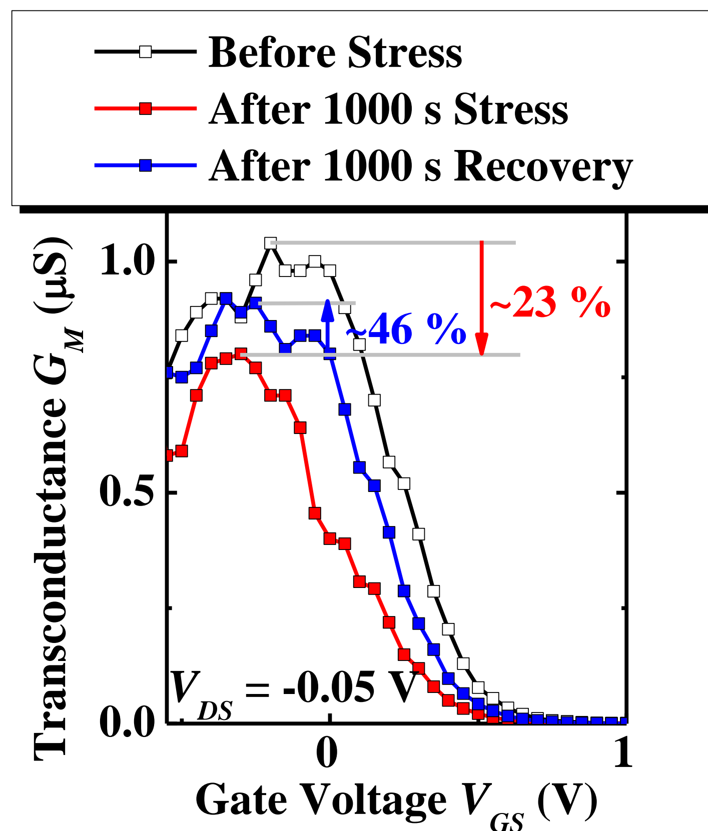


Fig. 5.27. G_M recovery after removal of NBT stress of V_{stress} - V_{TH} = -2.15 V. 46 % of G_M degradation recovered after 1000 s of removal of the gate stress.

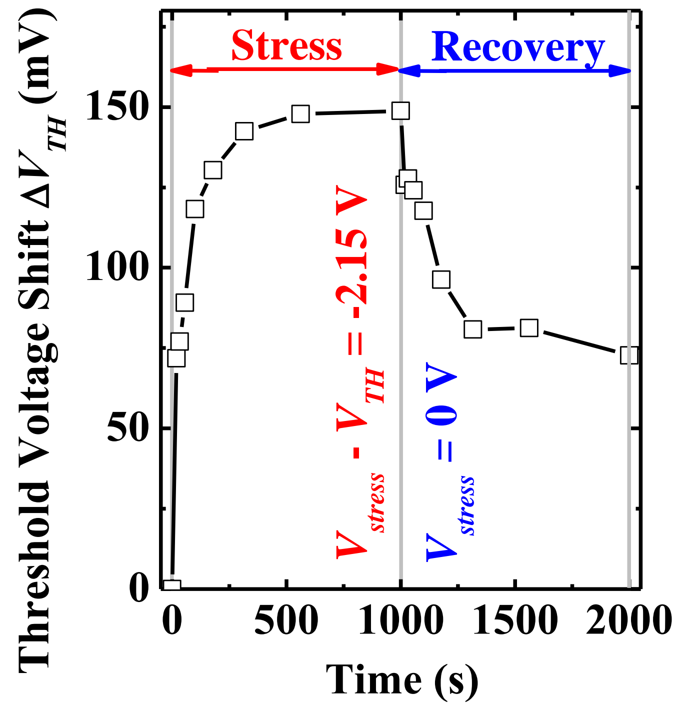


Fig. 5.28. V_{TH} shift as a function of time at stress phase and recovery phase. V_{TH} recovery was observed upon removal of gate stress V_{stress}.

V_{TH} shift as a function of time for stress phase, as well as recovery phase, is shown in Fig. 5.28. It could be observed that ΔV_{TH} increases with stress time during the stress phase. Once the gate stress was removed, V_{TH} started to recover. A significant amount of V_{TH} shift recovered 1000 s after the removal of gate stress.

5.5 Summary

First demonstration of Ω-gate p-channel Ge MuGFETs on GeOI substrate with *in situ* B doped p^+ RSD was reported. Process optimization for selective epitaxial growth of Ge:B RSD on patterned GeOI substrates was discussed. SEM and SIMS characterization of Ge:B grown was reported. Electrical characteristics of a Ge MuGFET with RSD were reported. Short channel effects were well controlled and high I_{ON}/I_{OFF} ratios of more than 10^4 were achieved for V_{DS} ranging from -0.05 V to -

0.95 V. The Ge MuGFET with RSD was also compared with the Ge MuGFET with metallic S/D. Further optimization of the S/D implant and integration of NiGe metallization could further improve the device performance.

NBTI characteristics of Ge MuGFETs with RSD were studied and reported. This is the first NBTI study of Ge MuGFETs. It was shown that Ge MuGFETs with TaN/HfO_2/SiO_2/Si gate stack have similar NBT degradation behaviour as MOSFETs with SiO_2 or SiON gate dielectrics. Upon NBT stress, threshold voltage of Ge MuGFETs becomes more negative, G_M becomes smaller, and S becomes larger. Interface trap generation is believed to be mainly responsible for the transconductance and S degradation. Transistor parameters were observed to recover after the NBT stress was removed.

Chapter 6

Conclusion and Future Work

6.1 Conclusion and Contributions of This Thesis

The motivation of this thesis work is to address some of the near term and long term technical challenges faced by the scaling of silicon (Si) complementary metal-oxide-semiconductor (CMOS). By integrating new materials and device structures, this work provides helpful engineering solutions for further advancement of CMOS, and accesses feasibility of the solutions.

Improvements in the performance or drive current of Si CMOS have traditionally been realized through device miniaturization. CMOS scaling meets immense challenges, and strain engineering has been adopted as an additional performance booster to keep the CMOS advancement, starting from 90 nm technology node in year 2003. Application of strain to the Si channel could significantly improve carrier mobility, which will directly result in enhancement of transistor drive current. It is believed that strain engineering will still be used in near term as one of major performance boosters for next a few technology nodes.

Among all the strain engineering techniques, silicon nitride (SiN) liner stressor technique is a cost-effective approach to induce large amount of strain into Si channel, and has been widely used. The continuous scaling of device dimension and gate pitch, however, poses new challenges to the conventional strain engineering techniques or materials, especially when the technology node reaches 22 nm and

beyond. The smaller space available for strain materials such as SiN liner stressor or SiGe S/D stressor decreases the stress coupling into channel [19], leading to smaller channel stress and compromised performance enhancement. Diamond-like carbon (DLC), which has much larger intrinsic stress than SiN, was explored to be used together with a SiO_2 adhesion layer as liner stressor material to address the challenges faced by conventional SiN liner stressor technology. The existence of SiO_2 adhesion layer degrades the stress coupling, resulting in smaller channel stress. It is desirable to remove this adhesion layer. In Chapter 2 of this thesis, further development work for the DLC liner stressor technology was performed. Characterization of DLC films was conducted to get film with high intrinsic stress and high resistivity for direct deposition of DLC on p-channel field-effect transistors (p-FETs). Direct deposition of the DLC liner stressor was applied for the first time on short channel planar Si p-FETs and more advanced Si nanowire p-FETs. The first realization of direct integration of DLC on Si p-FETs demonstrates that the SiO_2 adhesion layer is not needed for DLC technology, further improving the scalability of DLC liner stressor technology. This thesis also reported the first nanowire p-FETs with DLC liner stressor. This is one of the few works done in the literature on straining extremely scaled nanowire p-FETs for performance enhancement, demonstrating that liner stressor technique works well on advanced nanowire devices. Substantial transconductance and drive current enhancements were achieved by applying DLC liner stressor on planar and nanowire p-FETs.

When a new strain engineering technology is considered for manufacturing, its impact on device reliability should be investigated. Negative Bias Temperature Instability (NBTI) which could lead to severe degradation of p-FET parameters is considered as one of the most significant reliability concerns for the state of the art

integrated circuits. In Chapter 3, NBTI of strained p-FETs with DLC liner stressor was investigated using a improved ultra fast measurement (UFM) method employing an advanced low noise and high speed amplifier. This was the first NBTI investigation of strained p-FETs with DLC liner stressor. It was demonstrated that strained p-FETs with DLC liner stressor have more severe parameter degradations, as compared with the unstrained control. This, however, will not hinder the application of advanced strain techniques. Careful consideration on both performance enhancement and device reliability degradation induced by strain engineering should be taken when designing devices employing strain engineering [201]. In addition, detailed UFM measurement setup was discussed in Chapter 3. The ease of assembly and use characterization setup is not only useful to accurately investigate BTI characteristics of devices, but could also be used to do pulse current-voltage measurement of MOSFETs.

Ultimately, exploring new channel material with high carrier mobility to replace Si is deemed as a long term solution to extend the CMOS road map. When CMOS is scaled to deep sub-100 nm technology nodes, carrier transport in the transistor is quasi-ballistic and the drive current will be ultimately limited by the injection velocity [45, 46], rather than the saturation velocity which determines the performance of long channel transistors. The injection velocity was experimentally found to be proportional to low field mobility [47, 48]. Therefore, high mobility channel material is desirable for future CMOS applications. Germanium (Ge) is considered as one of the most promising channel materials to replace Si in future low power and high performance CMOS applications due to its high carrier mobilities, especially hole mobility. Multiple-Gate Field-Effect Transistors (MuGFETs) or FinFETs have been used for high volume CMOS production starting from 22 nm

technology node, as the additional gates provide improved short channel control for extremely scaled devices [65-67]. In Chapter 4 of this thesis work, high performance omega-gate (Ω-gate) Ge MuGFETs with low temperature Si_2H_6 passivated channel, high-κ gate dielectric and metal gate stack, and self-aligned metallic Schottky-Barrier (SB) nickel germanide (NiGe) source/drain (S/D) were fabricated on GeOI substrate. This is the first demonstration of Ge MuGFETs with NiGe S/D. Detailed Si CMOS compatible fabrication process was discussed in this Chapter. The effects of fin/channel doping on Ge MuGFET performance were also investigated. The on-state current achieved in this work are among the highest for Ge MuGFETs fabricated by top down approaches, which could be partially attributed to the high quality of GeOI substrate, good gate stack formed, and low S/D series resistance. Fine tuning of the channel implant and Ge surface passivation could further improve the control of short channel effects of Ge MuGFETs and improve the drive current.

FinFET or MuGFET structures employing narrow fins are known to have high series resistance due to the small contact area of S/D regions. Besides the employment of Schottky barrier metallic S/D structure to reduce series resistance (discussed in Chapter 4), epitaxial raised source/drain (RSD) structure was also demonstrated to reduce the series resistance of Si MuGFETs by increasing the S/D contact areas [70, 180]. In Chapter 5, we developed Ge MuGFETs with RSD. Process optimization for selective epitaxial growth of boron doped Ge (Ge:B) RSD on patterned GeOI substrates was first performed. Integration of RSD into Ge MuGFETs was then successfully demonstrated. To the author's best knowledge, there was the first Ge MuGFETs on GeOI substrate with RSD. Short channel effects of the devices are well controlled due to the adoption of multiple-gate structure, and high I_{ON}/I_{OFF} ratio of more than 10^4 was achieved. First NBTI characteristics of Ge

MuGFETs with RSD were investigated and reported in this Chapter as well. It was shown that Ge MuGFETs with TaN/HfO2/SiO_2/Si gate stack have similar NBT degradation behaviour as MOSFETs with SiO_2 or SiON gate dielectrics. Transistor parameters were observed to degrade upon NBT stress, and recover after the NBT stress was removed. Interface trap generation is believed to be mainly responsible for the transconductance and subthreshold swing degradation observed.

6.2 Future Directions

In summary, this thesis work has developed several exploratory technology options, such as novel strain engineering technique and advanced device architectures with new channel material, to address some of the near term, as well as long term, technical challenges faced the CMOS technology. Experimental data obtained demonstrate that DLC is a promising liner stressor material for the near term strain engineering application for p-FETs, and Ge MuGFET with either SB NiGe S/D or RSD is a promising candidate for future sub-14 nm technology node CMOS applications. Further investigations and optimizations of the relevant technologies developed in this thesis are needed. Some of possible future research directions are highlighted in this Section.

For the study of DLC as liner stressor material, further investigation could be performed on how the back-end process could affect the strain of DLC film, as it was reported that annealing of DLC could reduce the intrinsic stress [202]. Therefore, deposition temperature of pre-metal dielectric (PMD) and intermetal dielectric (IMD) should be optimized in order to maintain the stress of DLC liner stressor and good dielectric quality.

The compressive stress induced by DLC is beneficial not only to Si channel p-FETs but also to Ge channel devices. Wafer bending study on Ge p-FETs, as well as theoretical calculation, demonstrated that compressive stress along the longitudinal direction could enhance the performance of Ge p-FETs [203, 204], which is the same as in Si p-FETs. Therefore, it is expected that application of liner stressor on Ge p-FETs, including Ge MuGFETs, could bring substantial performance enhancement. Successful integration of stress liner into Ge MuGFETs will be an important milestone for Ge device development towards CMOS application. In addition, NBTI study of Ge p-FETs with DLC liner stressor could also be an interesting research direction to investigate the reliability of strained Ge devices.

Besides applying strain to Ge MuGFETs, work could also be done on further improving performance of Ge MuGFETs with NiGe S/D, as well as Ge MuGFETs with RSD. As demonstrated in Chapter 4, backside interface charges negatively affect the short channel control of Ge p-MuGFETs. For both of the device structures, further process development could be done to fabricate gate-all-around FETs to passivated the backside of the Ge layer and avoid the backside interface charge effects. This will further improve the gate control.

Although III-V is widely considered as a more promising channel material than Ge for future n-FET application [147], due to some technical challenges of fabricating high performance Ge n-FETs, such as dopant activation in Ge, and gate stack formation. It is still worth exploring the possibility of using Ge n-MuGFETs in future CMOS, as Ge also has very high electron mobility. Using Ge for both n- and p-FETs application could also simplify the starting wafer preparation and save the total process cost. Novel surface passivation technique reported recently, such as high

pressure oxidation of Ge [58] and plasma post oxidation [59], could be employed on Ge n-MuGFETs to have high quality gate stack. Solid phase diffusion, gas phase doping [55], spin-on dopant [61], *in-situ* n^+ doping [62], and ion co-implantation [63] (such as antimony and phosphorus together) could be used to have good n^+-p junction for MuGFET application.

References

[1] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of Solid-State Circuits,* vol. 9, pp. 256-268, 1974.

[2] D. A. Neamen, *Semiconductor physics and devices: basic principles*: McGraw-Hill, 2003.

[3] S. E. Thompson, M. Armstrong, C. Auth, M. Alavi, M. Buehler, R. Chau, S. Cea, T. Ghani, G. Glass, T. Hoffman, C. H. Jan, C. Kenyon, J. Klaus, K. Kuhn, M. Zhiyong, B. McIntyre, K. Mistry, A. Murthy, B. Obradovic, R. Nagisetty, N. Phi, S. Sivakumar, R. Shaheed, L. Shifren, B. Tufts, S. Tyagi, M. Bohr, and Y. El-Mansy, "A 90-nm logic technology featuring strained-silicon," *IEEE Transactions on Electron Devices,* vol. 51, pp. 1790-1797, 2004.

[4] G. Masetti, M. Severi, and S. Solmi, "Modeling of carrier mobility against carrier concentration in arsenic-, phosphorus-, and boron-doped silicon," *IEEE Transactions on Electron Devices,* vol. 30, pp. 764-769, 1983.

[5] V. Chan, R. Ken, I. MeiKei, Y. Sam, M. Rajeev, T. Young Way, Y. Min, and Qiqing, "Strain for CMOS performance improvement," in *IEEECustom Integrated Circuits Conference*, 2005, pp. 667-674.

[6] S. Pidin, T. Mori, K. Inoue, S. Fukuta, N. Itoh, E. Mutoh, K. Ohkoshi, R. Nakamura, K. Kobayashi, K. Kawamura, T. Saiki, S. Fukuyama, S. Satoh, M. Kase, and K. Hashimoto, "A novel strain enhanced CMOS architecture using selectively deposited high tensile and high compressive silicon nitride films," in *IEEE International Electron Devices Meeting (IEDM)*, 2004, pp. 213-216.

[7] S. Tyagi, C. Auth, P. Bai, G. Curello, H. Deshpande, S. Gannavaram, O. Golonzka, R. Heussner, R. James, C. Kenyon, S. H. Lee, N. Lindert, M. Liu, R. Nagisetty, S. Natarajan, C. Parker, J. Sebastian, B. Sell, S. Sivakumar, A. St Amour, and K. Tone, "An advanced low power, high performance, strained channel 65nm technology," in *IEEE International Electron Devices Meeting (IEDM)*, 2005, pp. 1070-1072.

[8] A. Oishi, O. Fujii, T. Yokoyama, K. Ota, T. Sanuki, H. Inokuma, K. Eda, T. Idaka, H. Miyajima, S. Iwasa, H. Yamasaki, K. Oouchi, K. Matsuo, H. Nagano, T. Komoda, Y. Okayama, T. Matsumoto, K. Fukasaku, T. Shimizu, K. Miyano, T. Suzuki, K. Yahashi, A. Horiuchi, Y. Takegawa, K. Saki, S. Mori, K. Ohno, L. Mizushima, M. Saito, M. Iwai, S. Yamada, N. Nagashima, and F. Matsuoka, "High performance CMOSFET technology for 45nm generation and scalability of stress-induced mobility enhancement technique," in *IEEE International Electron Devices Meeting (IEDM)*, 2005, pp. 229-232.

[9] B. F. Yang, K. Nummy, A. Waite, L. Black, H. Gossmann, H. Yin, Y. Liu, B. Kim, S. Narasimha, P. Fisher, H. V. Meer, J. Johnson, D. Chidambarrao, S. D. Kim, C. Sheraw, D. Wehella-gamage, J. Holt, X. Chen, D. Park, C. Y. Sung, D. Schepis, M. Khare, S. Luning, and P. Agnello, "Stress dependence and poly-pitch scaling characteristics of (110) PMOS drive current," in *IEEE Symposium on VLSI Technology (VLSI)*, 2007, pp. 126-127.

[10] S. Mayuzumi, J. Wang, S. Yamakawa, Y. Tateshita, T. Hirano, M. Nakata, S. Yamaguchi, Y. Yamamoto, Y. Miyanami, I. Oshiyama, K. Tanaka, K. Tai, K. Ogawa, K. Kugimiya, Y. Nagahama, Y. Hagimoto, R. Yamamoto, S. Kanda, K. Nagano, H. Wakabayashi, Y. Tagawa, M. Tsukarnoto, H. Iwamoto, M. Saito, S. Kadomura, and N. Nagashima, "Extreme high-performance n- and p-MOSFETs boosted by Dual-metal/high-k gate damascene process using top-cut dual stress liners on (100) substrates," in *IEEE International Electron Devices Meeting (IEDM)*, 2007, pp. 293-296.

[11] S. Suthram, M. M. Hussain, H. R. Harris, C. Smith, H. H. Tseng, R. Jammy, and S. E. Thompson, "Comparison of uniaxial wafer bending and contact-etch-stop-liner stress induced performance enhancement on double-gate FinFETs," *IEEE Electron Device Letters,* vol. 29, pp. 480-482, 2008.

[12] C. C. Wu, D. W. Lin, A. Keshavarzi, C. H. Huang, C. T. Chan, C. H. Tseng, C. L. Chen, C. Y. Hsieh, K. Y. Wong, M. L. Cheng, T. H. Li, Y. C. Lin, L. Y. Yang, C. P. Lin, C. S. Hou, H. C. Lin, J. L. Yang, K. F. Yu, M. J. Chen, T. H. Hsieh, Y. C. Peng, C. H. Chou, C. J. Lee, C. W. Huang, C. Y. Lu, F. K. Yang, H. K. Chen, L. W. Weng, P. C. Yen, S. H. Wang, S. W. Chang, S. W. Chuang, T. C. Gan, T. L. Wu, T. Y. Lee, W. S. Huang, Y. J. Huang, Y. W. Tseng, C. M. Wu, E. Ou-Yang, K. Y. Hsu, L. T. Lin, S. B. Wang, T. M. Kwok, C. C. Su, C. H. Tsai, M. J. Huang, H. M. Lin, A. S. Chang, S. H. Liao, L. S. Chen, J. H. Chen, P. S. Lim, X. F. Yu, S. Y. Ku, Y. B. Lee, P. C. Hsieh, P. W. Wang, Y. H. Chiu, S. S. Lin, H. J. Tao, M. Cao, and Y. J. Mii, "High performance 22/20nm FinFET CMOS devices with advanced high-K/metal gate scheme," in *IEEE International Electron Devices Meeting (IEDM)*, 2010, pp. 27.1.1-27.1.4.

[13] M. Cai, K. Ramani, M. Belyansky, B. Greene, D. H. Lee, S. Waidmann, F. Tamweber, and W. Henson, "Stress Liner Effects for 32-nm SOI MOSFETs With HKMG," *IEEE Transactions on Electron Devices,* vol. 57, pp. 1706-1709, 2010.

[14] L. Washington, F. Nouri, S. Thirupapuliyur, G. Eneman, P. Verheyen, V. Moroz, L. Smith, X. P. Xu, M. Kawaguchi, T. Huang, K. Ahmed, M. Balseanu, L. Q. Xia, M. H. Shen, Y. Kim, R. Rooyackers, K. De Meyer, and R. Schreutelkamp, "pMOSFET with 200% mobility enhancement induced by multiple stressors," *IEEE Electron Device Letters,* vol. 27, pp. 511-513, 2006.

[15] S. E. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, "Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs," in *IEEE International Electron Devices Meeting (IEDM)*, 2004, pp. 221-224.

[16] Y. Sun, S. E. Thompson, and T. Nishida, *Strain Effect in Semiconductors: Theory and Device Applications*: Springer, 2009.

[17] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C. H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McLntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," in *IEEE International Electron Devices Meeting (IEDM)* 2007, pp. 247-250.

[18] S. E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Z. Y. Ma, B. McIntyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. El-Mansy, "A logic nanotechnology featuring strained-silicon," *IEEE Electron Device Letters,* vol. 25, pp. 191-193, 2004.

[19] K. J. Kuhn, "Moore's Law Past 32nm: Future Challenges in Device Scaling," in *International Workshop on Computational Electronics*, 2009, pp. 1-6.

[20] K.-M. Tan, M. Zhu, W.-W. Fang, M. Yang, T.-Y. Liow, R. T. P. Lee, K. M. Hoe, C.-H. Tung, N. Balasubramanian, G. S. Samudra, and Y.-C. Yeo, "A New Liner Stressor with Very High Intrinsic Stress (> 6 GPa) and Low Permittivity Comprising Diamond-Like Carbon (DLC) for Strained P-Channel Transistors," in *IEEE International Electron Devices Meeting (IEDM)*, 2007, pp. 127-130.

[21] K.-M. Tan, W.-W. Fang, M. Yang, T.-Y. Liow, R. T. P. Lee, N. Balasubramanian, and Y.-C. Yeo, "Diamond-Like Carbon (DLC) Liner: A New Stressor for P-Channel Multiple-Gate Field-Effect Transistors," *IEEE Electron Device Letters,* vol. 29, pp. 750-752, 2008.

[22] K.-M. Tan, M. Yang, W.-W. Fang, A. E. J. Lim, R. T. P. Lee, T.-Y. Liow, and Y.-C. Yeo, "Performance Benefits of Diamond-like Carbon Liner Stressor in Strained P-Channel Field-Effect Transistors With Silicon-Germanium Source and Drain," *IEEE Electron Device Letters,* vol. 30, pp. 250-253, 2009.

[23] C.-S. Lu, H.-C. Lin, Y.-H. Chen, and T.-Y. Huang, "Improved NBTI in SiN-Capped PMOSFETs with Ultra-thin HfO2 Buffer," in *International Symposium on VLSI Technology, Systems and Applications*, 2007, pp. 1-2.

[24] D. K. Schroder and J. A. Babcock, "Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing," *Journal of Applied Physics,* vol. 94, pp. 1-18, 2003.

[25] M. A. Alam, H. Kufluoglu, D. Varghese, and S. Mahapatra, "A comprehensive model for PMOS NBTI degradation: Recent progress," *Microelectronics Reliability,* vol. 47, pp. 853-862, 2007.

[26] M. A. Alam and S. Mahapatra, "A comprehensive model of PMOS NBTI degradation," *Microelectronics Reliability,* vol. 45, pp. 71-81, 2005.

[27] A. E. Islam, H. Kufluoglu, D. Varghese, S. Mahapatra, and M. A. Alam, "Recent Issues in Negative-Bias Temperature Instability: Initial Degradation, Field Dependence of Interface Trap Generation, Hole Trapping Effects, and Relaxation," *IEEE Transactions on Electron Devices,* vol. 54, pp. 2143-2154, 2007.

[28] J. H. Stathis and S. Zafar, "The negative bias temperature instability in MOS devices: A review," *Microelectronics Reliability,* vol. 46, pp. 270-286, 2006.

[29] C. Shen, M. F. Li, C. E. Foo, T. Yang, D. M. Huang, A. Yap, G. S. Samudra, and Y. C. Yeo, "Characterization and Physical Origin of Fast Vth Transient in NBTI of pMOSFETs with SiON Dielectric," in *IEEE International Electron Devices Meeting (IEDM)*, 2006, pp. 1-4.

[30] C. R. Parthasarathy, M. Denais, V. Huard, G. Ribes, E. Vincent, and A. Bravaix, "New Insights into Recovery Characteristics Post NBTI Stress," in *44th Annual IEEE International Reliability Physics Symposium*, 2006, pp. 471-477.

[31] V. Huard, M. Denais, F. Perrier, N. Revil, C. Parthasarathy, A. Bravaix, and E. Vincent, "A thorough investigation of MOSFETs NBTI degradation," *Microelectronics Reliability,* vol. 45, pp. 83-98, Jan 2005.

[32] M.-F. Li, D. Huang, S. Chen, T. Yang, W. J. Liu, and Z. Liu, "Understand NBTI Mechanism by Developing Novel Measurement Techniques," *IEEE Transactions on Device and Materials Reliability,* vol. 8, pp. 62-71, 2008.

[33] A. Shickova, B. Kaczer, P. Verheyen, G. Eneman, E. S. Andres, M. Jurczak, P. Absil, H. Maes, and G. Groeseneken, "Negligible Effect of Process-Induced Strain on Intrinsic NBTI Behavior," *IEEE Electron Device Letters,* vol. 28, pp. 242-244, 2007.

[34] A. E. Islam, J. H. Lee, W. H. Wu, A. Oates, and M. A. Alam, "Universality of interface trap generation and its impact on I_D degradation in strained/unstrained PMOS transistors under NBTI stress," in *IEEE International Electron Devices Meeting*, 2008, pp. 107-110.

[35] A. Shickova, P. Verheyen, G. Eneman, R. Degraeve, E. Simoen, P. Favia, D. O. Klenov, E. San Andres, B. Kaczer, M. Jurczak, P. Absil, H. E. Maes, and G. Groeseneken, "Reliability of Strained-Si Devices With Post-Oxide-Deposition Strain Introduction," *IEEE Transactions on Electron Devices,* vol. 55, pp. 3432-3441, 2008.

[36] E. Morifuji, T. Kumamori, M. Muta, K. Suzuki, I. De, A. Shibkov, S. Saxena, T. Enda, N. Aoki, W. Asano, H. Otani, M. Nishigori, K. Miyamoto, F. Matsuoka, T. Noguchi, and M. Kakumu, "New considerations for highly reliable PMOSFETs in 100 nm generation and beyond," in *IEEE Symposium on VLSI Technology*, 2001, pp. 117-118.

[37] H. S. Rhee, H. Lee, T. Ueno, D. S. Shin, S. H. Lee, Y. Kim, A. Samoilov, P. O. Hansson, M. Kim, H. S. Kim, and N. I. Lee, "Negative bias temperature instability of carrier-transport enhanced pMOSFET with performance boosters," in *IEEE International Electron Devices Meeting (IEDM)*, 2005, pp. 709-712.

[38] S. S. Chung, Y. R. Liu, S. J. Wu, C. S. Lai, Y. C. Liu, D. F. Chen, H. S. Lin, W. T. Shiau, C. T. Tsai, S. C. Chien, and S. W. Sun, "A new insight into the degradation mechanisms of various mobility-enhanced CMOS devices with different substrate engineering," in *IEEE International Electron Devices Meeting (IEDM)*, 2005, pp. 559-562.

[39] G. Thareja, F. Z. J. Lee, A. V. Y. Thean, V. Vartanian, and B. Y. Nguyen, "NBTI Reliability of Strained SOI MOSFETs," presented at the 32nd International Symposium for Testing and Failure Analysis (ISTFA), 2006.

[40] T. Irisawa, T. Numata, E. Toyoda, N. Hirashita, T. Tezuka, N. Sugiyama, and S. Takagi, "Physical Understanding of Strain Effects on Gate Oxide Reliability of MOSFETs," in *IEEE Symposium on VLSI Technology (VLSI)*, 2007, pp. 36-37.

[41] J. C. Liao, Y. K. Fang, Y. T. Hou, C. L. Hung, P. F. Hsu, K. C. Lin, K. T. Huang, T. L. Lee, and M. S. Liang, "Strain effect and channel length dependence of bias temperature instability on complementary metal-oxide-semiconductor field effect transistors with high-k/SiO_2 gate stacks," *Applied Physics Letters,* vol. 93, p. 092101, 2008.

[42] M. S. Chen, Y. K. Fang, T. H. Lee, C. T. Lin, Y. T. Chiang, J. Ko, Y. K. Sheu, T. L. Shen, and W. Y. Liao, "Effect of etch stop layer stress on negative bias temperature instability of deep submicron p-type metal-oxide-semiconductor field effect transistors with dual gate oxide," *Japanese Journal of Applied Physics,* vol. 47, pp. 2624-2627, 2008.

[43] Z. Q. Teo, D. S. Ang, K. S. See, and P. Z. Yang, "Effect of mechanical strain on the NBTI of short-channel p-MOSFETS: Role of impactionization," in *IEEE International Reliability Physics Symposium*, 2009, pp. 1019-1022.

[44] Y. T. Chen, K. M. Chen, W. K. Yeh, J. S. Yuan, and F. S. Yeh, "Impact of SOI Thickness on FUSI-Gate CESL CMOS Performance and Reliability," *IEEE Transactions on Device and Materials Reliability,* vol. 11, pp. 44-49, 2011.

[45] M. Lundstrom, "Elementary scattering theory of the Si MOSFET," *IEEE Electron Device Letters,* vol. 18, pp. 361-363, 1997.

[46] M. S. Lundstrom, "On the mobility versus drain current relation for a nanoscale MOSFET," *IEEE Electron Device Letters,* vol. 22, pp. 293-295, 2001.

[47] A. Lochtefeld and D. A. Antoniadis, "On experimental determination of carrier velocity in deeply scaled NMOS: how close to the thermal limit?," *IEEE Electron Device Letters,* vol. 22, pp. 95-97, 2001.

[48] A. Lochtefeld, I. J. Djomehri, G. Samudra, and D. A. Antoniadis, "New insights into carrier transport in n-MOSFETs," *IBM Journal of Research and Development,* vol. 46, pp. 347-357, 2002.

[49] B. H. Lee, J. Oh, H. H. Tseng, R. Jammy, and H. Huff, "Gate stack technology for nanoscale devices," *Materials Today,* vol. 9, pp. 32-40, 2006.

[50] C. Chi On, H. Kim, D. Chi, P. C. McIntyre, and K. C. Saraswat, "Nanoscale germanium MOS Dielectrics-part II: high-κ gate dielectrics," *IEEE Transactions on Electron Devices,* vol. 53, pp. 1509-1516, 2006.

[51] M. Houssa, E. Chagarov, and A. Kummel, "Surface Defects and Passivation of Ge and III–V Interfaces," *MRS Bulletin,* vol. 34, pp. 504-513, 2009.

[52] R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, and S. Takagi, "High mobility Ge pMOSFETs with ~1nm thin EOT using $Al2O_3$/GeO_X/Ge gate stacks fabricated by plasma post oxidation," in *IEEE Symposium on VLSI Technology (VLSI)*, 2011, pp. 56-57.

[53] J. Mitard, B. De Jaeger, F. E. Leys, G. Hellings, K. Martens, G. Eneman, D. P. Brunco, R. Loo, J. C. Lin, D. Shamiryan, T. Vandeweyer, G. Winderickx, E. Vrancken, C. H. Yu, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, M. M. Heyns, and Ieee, "Record I_{ON}/I_{OFF} performance for 65nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability," in *IEEE International Electron Devices Meeting (IEDM)*, 2008, pp. 873-876.

[54] R. Pillarisetty, B. Chu-Kung, S. Corcoran, G. Dewey, J. Kavalieros, H. Kennel, R. Kotlyar, V. Le, D. Lionberger, M. Metz, N. Mukherjee, J. Nah, W. Rachmady, M. Radosavljevic, U. Shah, S. Taft, H. Then, N. Zelick, and R. Chau, "High mobility strained germanium quantum well field effect transistor as the p-channel device option for low power (Vcc = 0.5 V) III–V CMOS architecture," in *IEEE International Electron Devices Meeting (IEDM)*, 2010, pp. 6.7.1-6.7.4.

[55] K. Morii, T. Iwasaki, R. Nakane, M. Takenaka, and S. Takagi, "High performance GeO_2/Ge nMOSFETs with source/drain junctions formed by gas phase doping," in *IEEE International Electron Devices Meeting (IEDM)*, 2009, pp. 1092–1094.

[56] H.-Y. Yu, M. Kobayashi, W. S. Jung, A. K. Okyay, N. Yoshio, and K. C. Saraswat, "High performance n-MOSFETs with novel source/drain on selectively grown Ge on Si for monolithic integration," in *IEEE InternationalElectron Devices Meeting (IEDM)*, 2009, pp. 1-4.

[57] N. Wu, Q. Zhang, N. Balasubramanian, D. S. H. Chan, and C. Zhu, "Characteristics of Self-Aligned Gate-First Ge p- and n-Channel MOSFETs Using CVD HfO_2 Gate Dielectric and Si Surface Passivation," *IEEE Transactions on Electron Devices,* vol. 54, pp. 733-741, 2007.

[58] L. Choong Hyun, T. Nishimura, K. Nagashio, K. Kita, and A. Toriumi, "High-Electron-Mobility Ge/GeO_2 n-MOSFETs With Two-Step Oxidation," *IEEE Transactions on Electron Devices,* vol. 58, pp. 1295-1301, 2011.

[59] R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, and S. Takagi, "Al2O_3/GeOx/Ge gate stacks with low interface trap density fabricated by electron cyclotron resonance plasma postoxidation," *Applied Physics Letters,* vol. 98, pp. 112902-1-112902-3, 2011.

[60] D. P. Brunco, B. De Jaeger, G. Eneman, J. Mitard, G. Hellings, A. Satta, V. Terzieva, L. Souriau, F. E. Leys, G. Pourtois, M. Houssa, G. Winderickx, E. Vrancken, S. Sioncke, K. Opsomer, G. Nicholas, M. Caymax, A. Stesmans, J. Van Steenbergen, P. W. Mertens, M. Meuris, and M. M. Heyns, "Germanium MOSFET Devices: Advances in Materials Understanding, Process Development, and Electrical Performance," *Journal of the Electrochemical Society,* vol. 155, pp. H552-H561, 2008.

[61] M. Jamil, J. Mantey, E. U. Onyegam, G. D. Carpenter, E. Tutuc, and S. K. Banerjee, "High-Performance Ge nMOSFETs With n^+-p Junctions Formed by "Spin-On Dopant"," *IEEE Electron Device Letters,* vol. 32, pp. 1203-1205, 2011.

[62] Y. Cai, R. Camacho-Aguilera, J. T. Bessette, L. C. Kimerling, and J. Michel, "High phosphorous doped germanium: Dopant diffusion and modeling," *Journal of Applied Physics,* vol. 112, p. 034509, 2012.

[63] J. Kim, S. W. Bedell, and D. K. Sadana, "Improved germanium n^+/p junction diodes formed by coimplantation of antimony and phosphorus," *Applied Physics Letters,* vol. 98, p. 082112, 2011.

[64] K. Romanjek, L. Hutin, C. Le Royer, A. Pouydebasque, M. A. Jaud, C. Tabone, E. Augendre, L. Sanchez, J. Hartmann, H. Grampeix, V. Mazzocchi, S. Soliveres, R. Truche, L. Clavelier, P. Scheiblin, X. Garros, G. Reimbold, M. Vinet, F. Boulanger, and S. Deleonibus, "High performance 70nm gate length Germanium-On-Insulator pMOSFET with high-κ/metal gate," in *38th European Solid-State Device Research Conference*, 2008, pp. 75-78.

[65] X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," in *IEEE International Electron Devices Meeting (IEDM)*, 1999, pp. 67-70.

[66] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and H. Chenming, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Transactions on Electron Devices,* vol. 47, pp. 2320-2325, 2000.

[67] C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. McIntyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki, and K. Mistry, "A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *IEEE Symposium on VLSI Technology (VLSI)*, 2012, pp. 131-132.

[68] G. Wang, E. Rosseel, R. Loo, P. Favia, H. Bender, M. Caymax, M. M. Heyns, and W. Vandervorst, "Ge instability and the growth of Ge epitaxial layers in nanochannels on patterned Si (001) substrates," *Journal of Applied Physics,* vol. 108, pp. 123517-8, 2010.

[69] J. M. Larson and J. P. Snyder, "Overview and status of metal S/D Schottky-barrier MOSFET technology," *IEEE Transactions on Electron Devices,* vol. 53, pp. 1048-1058, 2006.

[70] J. Kedzierski, I. Meikei, E. Nowak, T. S. Kanarsky, Z. Ying, R. Roy, D. Boyd, D. Fried, and H. S. P. Wong, "Extension and source/drain design for high-performance FinFET devices," *IEEE Transactions on Electron Devices,* vol. 50, pp. 952-958, 2003.

[71] D. W. Wang, Q. Wang, A. Javey, R. Tu, H. J. Dai, H. Kim, P. C. McIntyre, T. Krishnamohan, and K. C. Saraswat, "Germanium nanowire field-effect transistors with SiO2 and high-kappa HfO2 gate dielectrics," *Applied Physics Letters,* vol. 83, pp. 2432-2434, 2003.

[72] L. Zhang, R. Tu, and H. Dai, "Parallel Core−Shell Metal-Dielectric-Semiconductor Germanium Nanowires for High-Current Surround-Gate Field-Effect Transistors," *Nano Letters,* vol. 6, pp. 2785-2789, 2006.

[73] J. Xiang, W. Lu, Y. Hu, Y. Wu, H. Yan, and C. M. Lieber, "Ge/Si nanowire heterostructures as high-performance field-effect transistors," *Nature,* vol. 441, pp. 489-493, 2006.

[74] J. Feng, R. Woo, S. Chen, Y. Liu, P. B. Griffin, and J. D. Plummer, "P-Channel Germanium FinFET Based on Rapid Melt Growth," *IEEE Electron Device Letters,* vol. 28, pp. 637-639, 2007.

[75] K. Ikeda, M. Ono, D. Kosemura, K. Usuda, M. Oda, Y. Kamimuta, T. Irisawa, Y. Moriyama, A. Ogura, and T. Tezuka, "High-mobility and low-parasitic resistance characteristics in strained Ge nanowire pMOSFETs with metal source/drain structure formed by doping-free processes," in *IEEE Symposium on VLSI Technology (VLSI)*, 2012, pp. 165-166.

[76] S.-H. Hsu, C.-L. Chu, W.-H. Tu, Y.-C. Fu, P.-J. Sung, H.-C. Chang, Y.-T. Chen, L.-Y. Cho, W. Hsu, G.-L. Luo, C. W. Liu, C. Hu, and F.-L. Yang, "Nearly defect-free Ge gate-all-around FETs on Si substrates," in *IEEE International Electron Devices Meeting (IEDM)*, 2011, pp. 35.2.1-35.2.4.

[77] J. W. Peng, N. Singh, G. Q. Lo, D. L. Kwong, and S. J. Lee, "CMOS Compatible Ge/Si Core/Shell Nanowire Gate-All-Around pMOSFET Integrated with HfO2/TaN Gate Stack," in *IEEE International Electron Devices Meeting (IEDM)*, 2009, pp. 38.2.1-38.2.4.

[78] J. Feng, G. Thareja, M. Kobayashi, S. Chen, A. Poon, Y. Bai, P. B. Griffin, S. S. Wong, Y. Nishi, and J. D. Plummer, "High-Performance Gate-All-Around GeOI p-MOSFETs Fabricated by Rapid Melt Growth Using Plasma Nitridation and ALD Al_2O_3 Gate Dielectric and Self-Aligned NiGe Contacts," *IEEE Electron Device Letters,* vol. 29, pp. 805-807, 2008.

[79] C. Le Royer, A. Pouydebasque, K. Romanjek, V. Barral, M. Vinet, J. M. Hartmann, E. Augendre, H. Grampeix, L. Lachal, C. Tabone, B. Previtali, R. Truche, and F. Allain, "Sub-100nm high-K metal gate GeOI pMOSFETs performance: Impact of the Ge channel orientation and of the source injection velocity," in *International Symposium on VLSI Technology, Systems, and Applications*, 2009, pp. 145-146.

[80] M. J. H. v. Dal, G. Vellianitis, G. Doornbos, B. Duriez, T. M. Shen, C. C. Wu, R. Oxland, K. Bhuwalka, M. Holland, T. L. Lee1, C. Wann, C. H. Hsieh, B. H. Lee, K. M. Yin, Z. Q. Wu, M. Passlack, and C. H. Diaz, "Demonstration of scaled Ge p-channel FinFETs integrated on Si," in *IEEE International Electron Devices Meeting (IEDM)*, 2012, pp. 521-524.

[81] H. S. Yang, R. Malik, S. Narasimha, Y. Li, R. Divakaruni, P. Agnello, S. Allen, A. Antreasyan, J. C. Arnold, K. Bandy, M. Belyansky, A. Bonnoit, G. Bronner, V. Chan, X. Chen, Z. Chen, D. Chidambarrao, A. Chou, W. Clark, S. W. Crowder, B. Engel, H. Harifuchi, S. F. Huang, R. Jagannathan, F. F. Jamin, Y. Kohyama, H. Kuroda, C. W. Lai, H. K. Lee, W. H. Lee, E. H. Lim, W. Lai, A. Mallikarjunan, K. Matsumoto, A. McKnight, J. Nayak, H. Y. Ng, S. Panda, R. Rengarajar, M. Steigerwalt, S. Subbanna, K. Subramanian, J. Sudijono, G. Sudo, S. P. Sun, B. Tessier, Y. Toyoshima, P. Tran, R. Wise, R. Wong, I. Y. Yang, C. H. Wann, L. T. Su, M. Horstmann, T. Feudel, A. Wei, K. Frohberg, G. Burbach, M. Gerhardt, M. Lenski, R. Stephan, K. Wieczorek, M. Schaller, H. Salz, J. Hohage, H. Ruelke, J. Klais, P. Huebler, S. Luning, R. van Bentum, G. Grasshoff, C. Schwan, E. Ehrichs, S. Goad, J. Buller, S. Krishnan, D. Greenlaw, M. Raab, and N. Kepler, "Dual stress liner for high performance sub-45nm gate length SOICMOS manufacturing," in *IEEE International Electron Devices Meeting (IEDM)*, 2004, pp. 1075-1077.

[82] K.-M. Tan, M. Zhu, W.-W. Fang, M. Yang, T.-Y. Liow, R. T. P. Lee, K. M. Hoe, C.-H. Tung, N. Balasubramanian, G. S. Samudra, and Y.-C. Yeo, "A High-Stress Liner Comprising Diamond-Like Carbon (DLC) for Strained p-Channel MOSFET," *IEEE Electron Device Letters,* vol. 29, pp. 192-194, 2008.

[83] K.-M. Tan, M. Yang, T.-Y. Liow, R. T. P. Lee, and Y.-C. Yeo, "Ultra High-Stress Liner Comprising Diamond-Like Carbon for Performance Enhancement of p-Channel Multiple-Gate Transistors," *IEEE Transactions on Electron Devices,* vol. 56, pp. 1277-1283, 2009.

[84] H.-C. Tsai and D. B. Bogy, "Characterization of diamondlike carbon films and their application as overcoats on thin-film media for magnetic recording," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 5, pp. 3287-3312, 1987.

[85] P. M. McGuiggan, S. M. Hsu, W. Fong, D. Bogy, and C. S. Bhatia, "Friction measurements of ultra-thin carbon overcoats in air," *Journal of Tribology-Transactions of the Asme,* vol. 124, pp. 239-244, Apr 2002.

[86] H. Inaba, K. Furusawa, and S. Sasaki, "Filtered Cathodic Vacuum Arc Process Conditions and Properties of Thin Tetrahedral Amorphous Carbon Films," *Japanese Journal of Applied Physics,* vol. 43, pp. 2681-2685, 2004.

[87] P. J. Martin and A. Bendavid, "Review of the filtered vacuum arc process and materials deposition," *Thin Solid Films,* vol. 394, pp. 1-14, 2001.

[88] *Taurus TSUPREM, Taurus Process Reference Manual*: Version X-2005.10, 2005.

[89] A. C. Ferrari, J. Robertson, M. G. Beghi, C. E. Bottani, R. Ferulano, and R. Pastorelli, "Elastic constants of tetrahedral amorphous carbon films by surface Brillouin scattering," *Applied Physics Letters,* vol. 75, pp. 1893-1895, 1999.

[90] X. Shi, B. K. Tay, H. S. Tan, L. Zhong, Y. Q. Tu, S. R. P. Silva, and W. I. Milne, "Properties of carbon ion deposited tetrahedral amorphous carbon films as a function of ion energy," *Journal of Applied Physics,* vol. 79, pp. 7234-7240, 1996.

[91] A. C. Ferrari and J. Robertson, "Resonant Raman spectroscopy of disordered, amorphous, and diamondlike carbon," *Physical Review B,* vol. 64, p. 075414, 2001.

[92] K. W. R. Gilkes, S. Prawer, K. W. Nugent, J. Robertson, H. S. Sands, Y. Lifshitz, and X. Shi, "Direct quantitative detection of the sp^3 bonding in diamond-like carbon films using ultraviolet and visible Raman spectroscopy," *Journal of Applied Physics,* vol. 87, pp. 7283-7289, 2000.

[93] K. W. R. Gilkes, H. S. Sands, D. N. Batchelder, J. Robertson, and W. I. Milne, "Direct observation of sp^3 bonding in tetrahedral amorphous carbon using ultraviolet Raman spectroscopy," *Applied Physics Letters,* vol. 70, pp. 1980-1982, 1997.

[94] X. Shi., D. Flynn, B. K. Tay, S. Prawer, K. W. Nugent, S. R. P. Silva, Y. Lifshitz, and W. I. Milne, "Mechanical properties and Raman spectra of tetrahedral amorphous carbon films with high sp^3 fraction deposited using a filtered cathodic arc," *Philosophical Magazine B-Physics of Condensed Matter Statistical Mechanics Electronic Optical and Magnetic Properties,* vol. 76, pp. 351-361, Sep 1997.

[95] Y. Lifshitz, "Hydrogen-free amorphous carbon films: correlation between growth conditions and properties," *Diamond and Related Materials,* vol. 5, pp. 388-400, 1996.

[96] A. C. Ferrari, "Determination of bonding in diamond-like carbon by Raman spectroscopy," *Diamond and Related Materials,* vol. 11, pp. 1053-1061, 2002.

[97] K. Rim, S. Narasimha, M. Longstreet, A. Mocuta, and J. Cai, "Low field mobility characteristics of sub-100 nm unstrained and strained Si MOSFETs," in *International Electron Devices Meeting (IEDM)*, 2002, pp. 43-46.

[98] A. Martinez, N. Seoane, A. R. Brown, J. R. Barker, and A. Asenov, "Variability in Si Nanowire MOSFETs Due to the Combined Effect of Interface Roughness and Random Dopants: A Fully Three-Dimensional NEGF Simulation Study," *IEEE Transactions on Electron Devices,* vol. 57, pp. 1626-1635, 2010.

[99] C. Shin, X. Sun, and T.-J. K. Liu, "Study of Random-Dopant-Fluctuation (RDF) Effects for the Trigate Bulk MOSFET," *IEEE Transactions on Electron Devices,* vol. 56, pp. 1538-1542, 2009.

[100] F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu, C.-C. Huang, T.-X. Chung, H.-W. Chen, C.-C. Huang, Y.-H. Liu, C.-C. Wu, C.-C. Chen, S.-C. Chen, Y.-T. Chen, Y.-H. Chen, C.-J. Chen, B.-W. Chan, P.-F. Hsu, J.-H. Shieh, H.-J. Tao, Y.-C. Yeo, Y. Li, J.-W. Lee, P. Chen, M.-S. Liang, and C. Hu, "5nm-gate nanowire FinFET," in *IEEE Symposium on VLSI Technology (VLSI)*, 2004, pp. 196-197.

[101] H.-Y. Chen, C.-C. Chen, F.-K. Hsueh, J.-T. Liu, C.-Y. Shen, C.-C. Hsu, S.-L. Shy, B.-T. Lin, H.-T. Chuang, C.-S. Wu, C. Hu, C.-C. Huang, and F.-L. Yang, "16nm functional 0.039 μm^2 6T-SRAM cell with nano injection lithography, nanowire channel, and full TiN gate," in *IEEE International Electron Devices Meeting (IEDM)*, 2009, pp. 958-960.

[102] J. W. Sleight, S. Bangsaruntip, G. Cohen, A. Majumdar, Y. Zhang, S. Engelmann, N. Fuller, L. Gignac, S. Mittal, J. Newbury, T. Barwicz, M. M. Frank, and M. Guillorn, "High performance and highly uniform metal high-k gate-all-around silicon nanowire MOSFETs," in *ECS Transactions*, 2010, pp. 179-189.

[103] H. Lee, S.-W. Ryu, J.-W. Han, L.-E. Yu, M. lm, C. Kim, S. Kim, E. Lee, K.-H. Kim, J.-H. Kim, D.-i. Bae, S. C. Jeon, K. H. Kim, G. S. Lee, O. Jae Su, Y. C. Park, W. H. Bae, J. J. Yoo, J. M. Yang, H. M. Lee, and Y.-K. Choi, "A nanowire transistor for high performance logic and terabit Non-Volatile memory devices," in *IEEE SymposiumVLSI Technology (VLSI)*, 2007, pp. 144-145.

[104] S. D. Suk, S.-Y. Lee, S.-M. Kim, E.-J. Yoon, M.-S. Kim, M. Li, C. W. Oh, K. H. Yeo, S. H. Kim, D.-S. Shin, K.-H. Lee, H. S. Park, J. N. Han, C. J. Park, J.-B. Park, D.-W. Kim, D. Park, and B.-I. Ryu, "High performance 5nm radius Twin Silicon Nanowire MOSFET (TSNWFET) : fabrication on bulk si wafer, characteristics, and reliability," in *IEEE International Electron Devices Meeting (IEDM)*, 2005, pp. 717-720.

[105] L. Chang, C. Yang-kyu, D. Ha, P. Ranade, X. Shiying, J. Bokor, H. Chenming, and T. J. King, "Extremely scaled silicon nano-CMOS devices," *Proceedings of the IEEE,* vol. 91, pp. 1860-1873, 2003.

[106] H. Lee, L.-E. Yu, S.-W. Ryu, J.-W. Han, K. Jeon, D.-Y. Jang, K.-H. Kim, J. Lee, J.-H. Kim, S. C. Jeon, G. S. Lee, J. S. Oh, Y. C. Park, W. H. Bae, H. M. Lee, J. M. Yang, J. J. Yoo, S. I. Kim, and Y.-K. Choi, "Sub-5nm All-Around Gate FinFET for Ultimate Scaling," in *IEEE Symposium onVLSI Technology (VLSI)*, 2006, pp. 58-59.

[107] T. Y. Liow, K. M. Tan, R. Lee, M. Zhu, B. L. H. Tan, G. S. Samudra, N. Balasubramanian, and Y. C. Yeo, "5 nm gate length Nanowire-FETs and planar UTB-FETs with pure germanium source/drain stressors and laser-free Melt-Enhanced Dopant (MeltED) diffusion and activation technique," in *IEEE Symposium on VLSI Technology (VLSI)*, 2008, pp. 36-37.

[108] J. Appenzeller, J. Knoch, M. T. Bjork, H. Riel, H. Schmid, and W. Riess, "Toward Nanowire Electronics," *IEEE Transactions on Electron Devices,* vol. 55, pp. 2827-2845, 2008.

[109] K. E. Moselund, M. Najmzadeh, P. Dobrosz, S. H. Olsen, D. Bouvet, L. De Michielis, V. Pott, and A. M. Ionescu, "The High-Mobility Bended n-Channel Silicon Nanowire Transistor," *IEEE Transactions on Electron Devices,* vol. 57, pp. 866-876, Apr 2010.

[110] Z. Jing, T. Yu, R. Wang, R. Huang, Y. Wang, B. Chen, J. Liu, X. Zhang, and Y. Wang, "High-Performance Si Nanowire Transistors on Fully Si Bulk Substrate From Top-Down Approach: Simulation and Fabrication," *IEEE Transactions on Nanotechnology,* vol. 9, pp. 114-122, 2010.

[111] A. Kinoshita, "Dopant segregated Schottky S/D and application to high performance MOSFETs," in *International Workshop on Junction Technology*, 2009, pp. 34-37.

[112] A. Kinoshita, T. Kinoshita, Y. Nishi, K. Uchida, S. Toriyama, R. Hasumi, and J. Koga, "Comprehensive study on injection velocity enhancement in Dopant-Segregated Schottky MOSFETs," in *IEEE International Electron Devices Meeting (IEDM)*, 2006, pp. 1-4.

[113] H.-S. Wong, L.-H. Tan, L. Chan, G.-Q. Lo, S. G., and Y.-C. Yeo, "Gate-all-around quantum-wire field-effect transistor with Dopant Segregation at Metal-Semiconductor-Metal heterostucture," in *IEEE Symposium on VLSI Technology (VLSI)*, 2009, pp. 92-93.

[114] M. Li, K. H. Yeo, Y. Y. Yeoh, S. D. Suk, K. H. Cho, D.-W. Kim, D. Park, and W.-S. Lee, "Experimental Investigation on Superior PMOS Performance of Uniaxial Strained <110> Silicon Nanowire Channel By Embedded SiGe Source/Drain," in *IEEE International Electron Devices Meeting (IEDM)*, 2007, pp. 899-902.

[115] B. Liu, M. C. Yang, and Y.-C. Yeo, "A new diamond-like carbon (DLC) ultra-high stress liner technology for direct deposition on p-channel field-effect transistors," in *the 2009 International Conference on Solid State Devices and Materials*, 2009, pp. 773-774.

[116] J. Kedzierski, J. Bokor, and C. Kisielowski, "Fabrication of planar silicon nanowires on silicon-on-insulator using stress limited oxidation," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 15, pp. 2825-2828, 1997.

[117] J. Peng, "Top-down engineered silicon and germanium nanowire MOSFET," Ph.D. dissertation, Department of Electrical and Computer Engineering, National University of Singapore, Singapore, 2010.

[118] S. Mayuzumi, S. Yamakawa, D. Kosemura, M. Takei, Y. Tateshita, H. Wakabayashi, M. Tsukamoto, T. Ohno, A. Ogura, and N. Nagashima, "Channel-Stress Enhancement Characteristics for Scaled pMOSFETs by Using Damascene Gate With Top-Cut Compressive Stress Liner and eSiGe," *IEEE Transactions on Electron Devices,* vol. 56, pp. 2778-2784, 2009.

[119] E. M. Kirsten, B. Didier, T. Lucas, P. Vincent, D. Paolo, and M. I. Adrian, "Local volume inversion and corner effects in triangular gate-all-around MOSFETs," in *36th European Solid-State Device Research Conference*, 2006, pp. 359-362.

[120] S. D. Suk, M. Li, Y. Y. Yeoh, K. H. Yeo, K. H. Cho, I. K. Ku, H. Cho, W. Jang, D.-W. Kim, D. Park, and W.-S. Lee, "Investigation of nanowire size dependency on TSNWFET," in *IEEE International Electron Devices Meeting (IEDM)*, 2007, pp. 891-894.

[121] E. B. Ramayya, D. Vasileska, S. M. Goodnick, and I. Knezevic, "Electron Mobility in Silicon Nanowires," *IEEE Transactions on Nanotechnology,* vol. 6, pp. 113-117, 2007.

[122] L. Ge and J. G. Fossum, "Analytical modeling of quantization and volume inversion in thin Si-film DG MOSFETs," *IEEE Transactions on Electron Devices,* vol. 49, pp. 287-294, 2002.

[123] W. Zhang and J. G. Fossum, "On the threshold Voltage of strained-Si-$Si_{1-x}Ge_x$ MOSFETs," *IEEE Transactions on Electron Devices,* vol. 52, pp. 263-268, 2005.

[124] S. S. Chung, E. R. Hsieh, D. C. Huang, C. S. Lai, C. H. Tsai, P. W. Liu, Y. H. Lin, C. T. Tsai, G. H. Ma, S. C. Chien, and S. W. Sun, "More Strain and Less Stress-The Guideline for Developing High-End Strained CMOS Technologies with Acceptable Reliability," in *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, 2008, pp. 435-438.

[125] M. H. Lin, E. R. Hsieh, S. S. Chung, C. H. Tsai, P. W. Liu, Y. H. Lin, C. T. Tsai, and G. H. Ma, "A new observation of strain-induced slow traps in advanced CMOS technology with process-induced strain using random telegraph noise measurement," in *IEEE Symposium on VLSI Technology (VLSI)*, 2009, pp. 52-53.

[126] S. Deora and S. Mahapatra, "A study of NBTI in HfSiON/TiN p-MOSFETs using ultra-fast on-the-fly (UF-OTF) I_{DLIN} technique," in *15th International Symposium on the Physical and Failure Analysis of Integrated Circuits*, 2008, pp. 1-4.

[127] T. Yang, M. F. Li, C. Shen, C. H. Ang, Z. Chunxiang, Y. C. Yeo, G. Samudra, S. C. Rustagi, and M. B. Yu, "Fast and slow dynamic NBTI components in p-MOSFET with SiON dielectric and their impact on device life-time and circuit application," in *IEEE Symposium on VLSI Technology (VLSI)*, 2005, pp. 92-93.

[128] J.-H. Lee and A. S. Oates, "Characterization of NBTI-Induced Interface State and Hole Trapping in SiON Gate Dielectrics of p-MOSFETs," *IEEE Transactions on Device and Materials Reliability,* vol. 10, pp. 174-181, 2010.

[129] C. Shen, M. F. Li, X. P. Wang, Y.-C. Yeo, and D. L. Kwong, "A fast measurement technique of MOSFETI I_d-V_g characteristics," *IEEE Electron Device Letters,* vol. 27, pp. 55-57, 2006.

[130] C. Shen, "Threshold voltage instabilities in MOS transistors with advanced gate dielectrics," Ph.D. dissertation, Department of Electrical and Computer Engineering, National University of Singapore, Singapore, 2009.

[131] S. Rangan, N. Mielke, and E. C. C. Yeh, "Universal recovery behavior of negative bias temperature instability [PMOSFETs]," in *IEEE International Electron Devices Meeting (IEDM)*, 2003, pp. 14.3.1-14.3.4.

[132] I. S. Han, H. H. Ji, O. S. You, W. H. Choi, J. E. Lim, K. J. Hwang, S. H. Park, H. S. Lee, D. B. Kim, and H. D. Lee, "New observation of mobility and reliability dependence on mechanical film stress in strained silicon CMOSFETs," *IEEE Transactions on Electron Devices,* vol. 55, pp. 1352-1358, 2008.

[133] C.-Y. Lu, H.-C. Lin, Y.-F. Chang, and T.-Y. Huang, "DC and AC NBTI Stresses in PMOSFETs with PE-SiN Capping," in *44th Annual IEEE International Reliability Physics Symposium*, 2006, pp. 727-728.

[134] J. R. Shih, J. J. Wang, W. Ken, P. Yeng, and J. T. Yue, "The study of compressive and tensile stress on MOSFET's I-V, C-V characteristics and it's impacts on hot carrier injection and negative bias temperature instability," in *41st Annual IEEE International Reliability Physics Symposium Proceedings*, 2003, pp. 612-613.

[135] V. D. Maheta, E. N. Kumar, S. Purawat, C. Olsen, K. Ahmed, and S. Mahapatra, "Development of an Ultrafast On-the-Fly I_{DLIN} Technique to Study NBTI in Plasma and Thermal Oxynitride p-MOSFETs," *IEEE Transactions on Electron Devices,* vol. 55, pp. 2614-2622, 2008.

[136] G. Gupta, S. Mahapatra, L. Leela Madhav, D. Varghese, K. Ahmed, and F. Nouri, "Interface-Trap Driven NBTI for Ultrathin (EOT~12Å) Plasma and Thermal Nitrided Oxynitrides," in *IEEE International Reliability Physics Symposium Proceedings*, 2006, pp. 731-732.

[137] Y. J. Lee, Y. C. Tang, M. H. Wu, T. S. Chao, P. T. Ho, D. Lai, W. L. Yang, and T. Y. Huang, "NBTI effects of pMOSFETs with different nitrogen dose implantation," in *IEEE International Reliability Physics Symposium Proceedings*, 2004, pp. 681-682.

[138] G. Cellere, M. G. Valentini, and A. Paccagnella, "Effect of channel width, lenth. and latent damage on NBTI," in *International Conference on Integrated Circuit Design and Technology*, 2004, pp. 303-306.

[139] T. Yamamoto, K. Uwasawa, and T. Mogami, "Bias temperature instability in scaled p^+ polysilicon gate p-MOSFET's," *IEEE Transactions on Electron Devices,* vol. 46, pp. 921-926, 1999.

[140] S. Tsujikawa, T. Mine, K. Watanabe, Y. Shimamoto, R. Tsuchiya, K. Ohnishi, T. Onai, J. Yugami, and S. Kimura, "Negative bias temperature instability of pMOSFETs with ultra-thin SiON gate dielectrics," in *IEEE International Reliability Physics Symposium Proceedings*, 2003, pp. 183-188.

[141] H. Aono, E. Murakami, K. Okuyama, A. Nishida, M. Minami, Y. Ooji, and K. Kubota, "Modeling of NBTI saturation effect and its impact on electric field dependence of the lifetime," *Microelectronics Reliability,* vol. 45, pp. 1109-1114, 2005.

[142] K. Saraswat, C. O. Chui, T. Krishnamohan, D. Kim, A. Nayfeh, and A. Pethe, "High performance germanium MOSFETs," *Materials Science and Engineering B-Solid State Materials for Advanced Technology,* vol. 135, pp. 242-249, 2006.

[143] L. Gomez, C. Ni Chléirigh, P. Hashemi, and J. L. Hoyt, "Enhanced Hole Mobility in High Ge Content Asymmetrically Strained-SiGe p-MOSFETs," *IEEE Electron Device Letters,* vol. 31, pp. 782-784, 2010.

[144] M. Heyns, A. Alian, G. Brammertz, M. Caymax, Y. C. Chang, L. K. Chu, B. De Jaeger, G. Eneman, F. Gencarelli, G. Groeseneken, G. Hellings, A. Hikavyy, T. Y. Hoffmann, M. Houssa, C. Huyghebaert, D. Leonelli, D. Lin, R. Loo, W. Magnus, C. Merckling, M. Meuris, J. Mitard, L. Nyns, T. Orzali, R. Rooyackers, S. Sioncke, B. Soree, X. Sun, A. Vandooren, A. S. Verhulst, B. Vincent, N. Waldron, G. Wang, W. E. Wang, and L. Witters, "Advancing CMOS beyond the Si roadmap with Ge and III/V devices," in *IEEE International Electron Devices Meeting (IEDM)*, 2010, pp. 13.1.1-13.1.4.

[145] R. Zhang, P. C. Huang, N. Taoka, M. Takenaka, and S. Takagi, "High mobility Ge pMOSFETs with 0.7 nm ultrathin EOT using $HfO_2/Al_2O_3/GeO_x/Ge$ gate stacks fabricated by plasma post oxidation," in *IEEE Symposium on VLSI Technology (VLSI)*, 2012, pp. 161-162.
[146] R. Pillarisetty, "Academic and industry research progress in germanium nanodevices," *Nature,* vol. 479, pp. 324-328, 2011.
[147] K. J. Kuhn, "Considerations for Ultimate CMOS Scaling," *IEEE Transactions on Electron Devices,* vol. 59, pp. 1813-1828, 2012.
[148] T. Akatsu, C. Deguet, L. Sanchez, F. Allibert, D. Rouchon, T. Signamarcheix, C. Richtarch, A. Boussagol, V. Loup, F. Mazen, J.-M. Hartmann, Y. Campidelli, L. Clavelier, F. Letertre, N. Kernevez, and C. Mazure, "Germanium-on-insulator (GeOI) substrates—A novel engineered substrate for future high performance devices," *Materials Science in Semiconductor Processing,* vol. 9, pp. 444-448, 2006.
[149] J. Tang, C.-Y. Wang, F. Xiu, Y. Zhou, L.-J. Chen, and K. L. Wang, "Formation and Device Application of Ge Nanowire Heterostructures via Rapid Thermal Annealing," *Advances in Materials Science and Engineering,* vol. 2011, p. 16, 2011.
[150] T. Burchhart, C. Zeiner, Y. J. Hyun, A. Lugstein, G. Hochleitner, and E. Bertagnolli, "High performance Omega-gated Ge nanowire MOSFET with quasi-metallic source/drain contacts," *Nanotechnology,* vol. 21, 2010.
[151] B. Liu, X. Gong, G. Han, P. S. Y. Lim, Y. Tong, Q. Zhou, Y. Yang, N. Daval, C. Veytizou, D. Delprat, B. Y. Nguyen, and Y. C. Yeo, "High-Performance Germanium Ω-Gate MuGFET With Schottky-Barrier Nickel Germanide Source/Drain and Low-Temperature Disilane-Passivated Gate Stack," *IEEE Electron Device Letters,* vol. 33, pp. 1336-1338, 2012.
[152] S. Zhu, J. Chen, M. F. Li, S. J. Lee, J. Singh, C. X. Zhu, A. Du, C. H. Tung, A. Chin, and D. L. Kwong, "N-type Schottky barrier source/drain MOSFET using ytterbium silicide," *IEEE Electron Device Letters,* vol. 25, pp. 565-567, 2004.
[153] J. F. Ziegler, "SRIM-2003," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms,* vol. 219-220, pp. 1027-1036, 2004.
[154] C. O. Chui, L. Kulig, J. Moran, W. Tsai, and K. C. Saraswat, "Germanium n-type shallow junction activation dependences," *Applied Physics Letters,* vol. 87, pp. 091909-091909-3, 2005.
[155] H. G. Tompkins and W. A. McGahan, *Spectroscopic Ellipsometry and Reflectometry: A User's Guide*: John Wiley & Sons, 1999.
[156] P. L. Jiang, H. Chu, J. Hench, and D. Wack, "Forward solve algorithms for optical critical dimension metrology," in *Metrology, Inspection, and Process Control for Microlithography XXII*, San Jose, CA, 2008.
[157] F. E. Leys, R. Bonzom, B. Kaczer, T. Janssens, W. Vandervorst, B. De Jaeger, J. Van Steenbergen, K. Martens, D. Hellin, J. Rip, G. Dilliway, A. Delabie, P. Zimmerman, M. Houssa, A. Theuwis, R. Loo, M. Meuris, M. Caymax, and M. M. Heyns, "Thin epitaxial Si films as a passivation method for Ge(100): Influence of deposition temperature on Ge surface segregation and the high-k/Ge interface quality," *Materials Science in Semiconductor Processing,* vol. 9, pp. 679-684, 2006.

[158] G. Eneman, B. De Jaeger, G. Wang, J. Mitard, G. Hellings, D. P. Brunco, E. Simoen, R. Loo, M. Caymax, C. Claeys, K. De Meyer, M. Meuris, and M. M. Heyns, "Short-channel epitaxial germanium pMOS transistors," *Thin Solid Films,* vol. 518, pp. S88-S91, 2010.

[159] M. H. Shin, S. W. Na, N. E. Lee, T. K. Oh, J. Kim, T. Lee, and J. Ahn, "Dry etching of TaN/HfO2 gate stack structure by Cl2/SF6/Ar inductively coupled plasma," *Japanese Journal of Applied Physics,* vol. 44, pp. 5811-5818, 2005.

[160] D. P. Brunco, K. Opsomer, B. De Jaeger, G. Winderickx, K. Verheyden, and M. Meuris, "Observation and suppression of nickel germanide overgrowth on germanium substrates with patterned SiO_2 structures," *Electrochemical and Solid State Letters,* vol. 11, pp. H39-H41, 2008.

[161] L. Hutin, M. Vinet, T. Poiroux, C. Le Royer, B. Previtali, C. Vizioz, D. Lafond, Y. Morand, M. Rivoire, F. Nemouchi, V. Carron, T. Billon, S. Deleonibus, and O. Faynot, "Dual metallic source and drain integration on planar Single and Double Gate SOI CMOS down to 20nm: Performance and scalability assessment," in *IEEE International Electron Devices Meeting (IEDM)*, 2009, pp. 3.1.1-3.1.4.

[162] L. Hutin, C. Le Royer, C. Tabone, V. Delaye, F. Nemouchi, F. Aussenac, L. Clavelier, and M. Vinet, "Schottky Barrier Height Extraction in Ohmic Regime: Contacts on Fully Processed GeOI Substrates," *Journal of the Electrochemical Society,* vol. 156, pp. H522-H527, 2009.

[163] P. Tsipas and A. Dimoulas, "Modeling of negatively charged states at the Ge surface and interfaces," *Applied Physics Letters,* vol. 94, pp. 012114-3, 2009.

[164] K. Romanjek, E. Augendre, W. Van Den Daele, B. Grandchamp, L. Sanchez, C. Le Royer, J. M. Hartmann, B. Ghyselen, E. Guiot, K. Bourdelle, S. Cristoloveanu, F. Boulanger, and L. Clavelier, "Improved GeOI substrates for pMOSFET off-state leakage control," *Microelectronic Engineering,* vol. 86, pp. 1585-1588, 2009.

[165] W. Van Den Daele, E. Augendre, C. Le Royer, J. F. Damlencourt, B. Grandchamp, and S. Cristoloveanu, "Low-temperature characterization and modeling of advanced GeOI pMOSFETs: Mobility mechanisms and origin of the parasitic conduction," *Solid-State Electronics,* vol. 54, pp. 205-212, 2010.

[166] W. Van Den Daele, C. Le Royer, E. Augendre, J. Mitard, G. Ghibaudo, and S. Cristoloveanu, "Detailed investigation of effective field, hole mobility and scattering mechanisms in GeOI and Ge pMOSFETs," *Solid-State Electronics,* vol. 59, pp. 25-33, 2011.

[167] W. F. Yang, S. J. Lee, G. C. Liang, R. Eswar, Z. Q. Sun, and D. L. Kwong, "Temperature Dependence of Carrier Transport of a Silicon Nanowire Schottky-Barrier Field-Effect Transistor," *IEEE Transactions on Nanotechnology,* vol. 7, pp. 728-732, 2008.

[168] P. C. Karulkar, "Ultra-thin SOI MOSFETs at high temperature," in *IEEE International SOI Conference*, 1993, pp. 136-137.

[169] G. Reichert, C. Raynaud, O. Faynot, F. Balestra, and S. Cristoloveanu, "Submicron SOI-MOSFETs for high temperature operation (300-600K)," *Microelectronic Engineering,* vol. 36, pp. 359-362, 1997.

[170] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proceedings of the IEEE,* vol. 55, pp. 2192-2193, 1967.

[171] G. Hellings, G. Eneman, R. Krom, B. De Jaeger, J. Mitard, A. De Keersgieter, T. Hoffmann, M. Meuris, and K. De Meyer, "Electrical TCAD Simulations of a Germanium pMOSFET Technology," *IEEE Transactions on Electron Devices,* vol. 57, pp. 2539-2546, 2010.

[172] K. Endo, Y. Ishikawa, Y. Liu, M. Masahara, T. Matsukawa, S. I. O'Uchi, K. Ishii, H. Yamauchi, J. Tsukada, and E. Suzuki, "Experimental Evaluation of Effects of Channel Doping on Characteristics of FinFETs," *IEEE Electron Device Letters,* vol. 28, pp. 1123-1125, 2007.

[173] C. H. Lin, R. Kambhampati, R. J. Miller, T. B. Hook, A. Bryant, W. Haensch, P. Oldiges, I. Lauer, T. Yamashita, V. Basker, T. Standaert, K. Rim, E. Leobandung, H. Bu, and M. Khare, "Channel doping impact on FinFETs for 22nm and beyond," in *IEEE Symposium on VLSI Technology (VLSI)*, 2012, pp. 15-16.

[174] M. Mueller, Q. T. Zhao, C. Urban, C. Sandow, U. Breuer, and S. Mantl, "Schottky-barrier height tuning of Ni and Pt germanide/n-Ge contacts using dopant segregation," in *9th International Conference on Solid-State and Integrated-Circuit Technology*, 2008, pp. 153-156.

[175] D. Z. Chi, H. B. Yao, S. L. Liew, C. C. Tan, C. T. Chua, K. C. Chua, R. Li, and S. J. Lee, "Schottky barrier height in germanide/Ge contacts and its engineering through germanidation induced dopant segregation," in *International Workshop on Junction Technology*, 2007, pp. 81-86.

[176] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub 50 nm MOSFETs: a statistical 3D 'atomistic' simulation study," *Nanotechnology,* vol. 10, pp. 153-158, 1999.

[177] X. Tang, V. K. De, and J. D. Meindl, "Intrinsic MOSFET parameter fluctuations due to random dopant placement," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 5, pp. 369-376, 1997.

[178] A. Asenov and S. Saini, "Polysilicon gate enhancement of the random dopant induced threshold voltage fluctuations in sub-100 nm MOSFETs with ultrathin gate oxide," *IEEE Transactions on Electron Devices,* vol. 47, pp. 805-812, 2000.

[179] G. Leung and C. O. Chui, "Variability Impact of Random Dopant Fluctuation on Nanoscale Junctionless FinFETs," *IEEE Electron Device Letters,* vol. 33, pp. 767-769, 2012.

[180] A. Dixit, A. Kottantharayil, N. Collaert, M. Goodwin, M. Jurczak, and K. De Meyer, "Analysis of the parasitic S/D resistance in multiple-gate FETs," *IEEE Transactions on Electron Devices,* vol. 52, pp. 1132-1140, 2005.

[181] J. Kedzierski, E. Nowak, T. Kanarsky, Y. Zhang, D. Boyd, R. Carruthers, C. Cabral, R. Amos, C. Lavoie, R. Roy, J. Newbury, E. Sullivan, J. Benedict, P. Saunders, K. Wong, D. Canaperi, M. Krishnan, K. L. Lee, B. A. Rainey, D. Fried, P. Cottrell, H. S. P. Wong, M. Ieong, and W. Haensch, "Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation," in *IEEE International Electron Devices Meeting (IEDM)*, 2002, pp. 247-250.

[182] G. Sery, S. Borkar, V. De, and Acm, "Life is CMOS: Why chase the life after?," in *39th Design Automation Conference*, 2002, pp. 78-83.

[183] Y.-K. Choi, N. Lindert, P. Xuan, S. Tang, H. Daewon, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "Sub-20 nm CMOS FinFET technologies," in *IEEE International Electron Devices Meeting (IEDM)*, 2001, pp. 19.1.1-19.1.4.

[184] H.-Y. Yu, M. Kobayashi, J.-H. Park, Y. Nishi, and K. C. Saraswat, "Novel Germanium n-MOSFETs With Raised Source/Drain on Selectively Grown Ge on Si for Monolithic Integration," *IEEE Electron Device Letters,* vol. 32, pp. 446-448, 2011.

[185] W. P. Bai, N. Lu, and D. L. Kwong, "Si interlayer passivation on germanium MOS capacitors with high-κ dielectric and metal gate," *IEEE Electron Device Letters,* vol. 26, pp. 378-380, 2005.

[186] Y. Kamata, Y. Kamimuta, T. Ino, and A. Nishiyama, "Direct Comparison of ZrO_2 and HfO_2 on Ge Substrate in Terms of the Realization of Ultrathin High-κ Gate Stacks," *Japanese Journal of Applied Physics,* vol. 44, pp. 2323–2329, 2005.

[187] N. Lu, W. Bai, A. Ramirez, C. Mouli, A. Ritenour, M. L. Lee, D. Antoniadis, and D. L. Kwong, "Ge diffusion in Ge metal oxide semiconductor with chemical vapor deposition HfO_2 dielectric," *Applied Physics Letters,* vol. 87, pp. 051922-3, 2005.

[188] Q. C. Zhang, N. Wu, D. M. Y. Lai, Y. Nikolai, L. K. Bera, and C. X. Zhu, "Germanium incorporation in HfO_2 dielectric on germanium substrate," *Journal of the Electrochemical Society,* vol. 153, pp. G207-G210, 2006.

[189] E. Huger, U. Tietze, D. Lott, H. Bracht, D. Bougeard, E. E. Haller, and H. Schmidt, "Self-diffusion in germanium isotope multilayers at low temperatures," *Applied Physics Letters,* vol. 93, pp. 162104-3, 2008.

[190] K. Kita, T. Takahashi, H. Nomura, S. Suzuki, T. Nishimura, and A. Toriumi, "Control of high-k/germanium interface properties through selection of high-k materials and suppression of GeO volatilization," *Applied Surface Science,* vol. 254, pp. 6100-6105, 2008.

[191] Y. Moriyama, N. Hirashita, K. Usuda, S. Nakaharai, N. Sugiyama, E. Toyoda, and S. Takagi, "Study of the surface cleaning of GOI and SGOI substrates for Ge epitaxial growth," *Applied Surface Science,* vol. 256, pp. 823-829, Nov 2009.

[192] T. R. Bramblett, Q. Lu, N. E. Lee, N. Taylor, M. A. Hasan, and J. E. Greene, "Ge(001) gas-source molecular beam epitaxy on Ge(001)2×1 and Si(001)2×1 from Ge_2H_6: Growth kinetics and surface roughening " *Journal of Applied Physics,* vol. 77, pp. 1504-1513, 1995.

[193] H. Akazawa, "Morphological switching in synchrotron-radiation-excited Ge homoepitaxy: Transition from kinetic roughening to smoothing," *Journal of Applied Physics,* vol. 97, pp. 106105-3, 2005.

[194] N. Sugiyama, Y. Moriyama, S. Nakaharai, T. Tezuka, T. Mizuno, and S. Takagi, "Kinetics of epitaxial growth of Si and SiGe films on (1 1 0) Si substrates," *Applied Surface Science,* vol. 224, pp. 188-192, 2004.

[195] M. Okada, M. Kondo, H. Ikeda, S. Zaima, and Y. Yasuda, "Hydrogen effects on $Si_{1-x}Ge_x$/Si heteroepitaxial growth by Si_2H_6- and GeH_4-source molecular beam epitaxy," *Japanese Journal of Applied Physics,* vol. 36, pp. 7665-7668, 1997.

[196] M. L. Lee, D. A. Antoniadis, and E. A. Fitzgerald, "Challenges in epitaxial growth of SiGe buffers on Si (111), (110), and (112)," *Thin Solid Films,* vol. 508, pp. 136-139, 2006.

[197] V. Destefanis, J. M. Hartmann, A. Abbadie, A. M. Papon, and T. Billon, "Growth and structural properties of SiGe virtual substrates on Si (1 0 0), (1 1 0), and (1 1 1)," *Journal of Crystal Growth,* vol. 311, pp. 1070-1079, 2009.

[198] S. Zafar, Y. H. Kim, V. Narayanan, C. Cabral, V. Paruchuri, B. Doris, J. Stathis, A. Callegari, and M. Chudzik, "A Comparative Study of NBTI and PBTI (Charge Trapping) in SiO_2/HfO_2 Stacks with FUSI, TiN, Re Gates," in *IEEE Symposium on VLSI Technology (VLSI)*, 2006, pp. 23-25.

[199] S. Zafar, A. Kumar, E. Gusev, and E. Cartier, "Threshold voltage instabilities in hig-κ gate dielectric stacks," *IEEE Transactions on Device and Materials Reliability,* vol. 5, pp. 45-64, 2005.

[200] D. Varghese, D. Saha, S. Mahapatra, K. Ahmed, F. Nouri, and M. Alam, "On the dispersive versus arrhenius temperature activation of nbti time evolution in plasma nitrided gate oxides: measurements, theory, and implications," in *IEEE International Electron Devices Meeting (IEDM)*, 2005, pp. 684-687.

[201] S. S. Chung, E. R. Hsieh, D. C. Huang, C. S. Lai, C. H. Tsai, P. W. Liu, Y. H. Lin, C. T. Tsai, G. H. Ma, S. C. Chien, and S. W. Sun, "More strain and less stress- the guideline for developing high-end strained CMOS technologies with acceptable reliability," in *IEEE International Electron Devices Meeting (IEDM)*, 2008, pp. 435-438.

[202] A. C. Ferrari, B. Kleinsorge, N. A. Morrison, A. Hart, V. Stolojan, and J. Robertson, "Stress reduction and bond stability during thermal annealing of tetrahedral amorphous carbon," *Journal of Applied Physics,* vol. 85, pp. 7191-7197, May 1999.

[203] M. Kobabyashi, J. Mitard, T. Irisawa, T. Y. Hoffmann, M. Meuris, K. Saraswat, Y. Nishi, and M. Heyns, "Experimental demonstration of high source velocity and its enhancement by uniaxial stress in Ge PFETs," in *IEEE Symposium on VLSI Technology (VLSI)*, 2010, pp. 215-216.

[204] T. Krishnamohan, K. Donghyun, T. V. Dinh, A. t. Pham, B. Meinerzhagen, C. Jungemann, and K. Saraswat, "Comparison of (001), (110) and (111) uniaxial- and biaxial- strained-Ge and strained-Si PMOS DGFETs for all channel orientations: Mobility enhancement, drive current, delay and off-state leakage," in *IEEE International Electron Devices Meeting (IEDM)*, 2008, pp. 899-902.

Appendix A

List of Publications

Journal Publications

1. **B. Liu**, K.-M. Tan, M. Yang, and Y.-C. Yeo, "NBTI reliability of p-channel transistors with diamond-like carbon liner having ultra-high compressive stress," *IEEE Electron Device Letters*, vol. 30, no. 8, pp. 867-869, Aug. 2009.
2. R. Cheng, **B. Liu**, and Y.-C. Yeo, "Carrier transport in strained p-channel field-effect transistors with diamond-like carbon liner stressor," *Applied Physics Letters*, vol. 96, no. 9, 092113, Mar. 2010.
3. **B. Liu**, H.-S. Wong, M.-C. Yang, and Y.-C. Yeo, "Strained silicon nanowire p-channel FETs with diamond-like carbon (DLC) liner stressor," *IEEE Electron Device Letters*, vol. 31, no. 12, pp. 1371 -1373, Dec. 2010.
4. X. Liu, **B. Liu**, E. K. F. Low, W. Liu, M. Yang, L.-S. Tan, K. L. Teo, and Y.-C. Yeo, "Local stress induced by diamond-like carbon liner in AlGaN/GaN MOS-HEMTs and impact on electrical characteristics," *Applied Physics Letters*, vol. 98, no. 18, 183502, May 2011.
5. S.-M. Koh, E. Y.-J. Kong, **B. Liu**, C.-M. Ng, G. S. Samudra, and Y.-C. Yeo, "Contact resistance reduction for strained n-FinFETs with silicon-carbon source/drain and platinum-based silicide contacts featuring tellurium implant and segregation," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 3852 - 3862, Nov. 2011.
6. L. Wang, G. Han, S. Su, Q. Zhou, Y. Yang, P. Guo, W. Wang, Y. Tong, P. S. Y. Lim, **B. Liu**, E. Y.-J. Kong, C. Xue, Q. Wang, B. Cheng, and Y.-C. Yeo, "Thermally stable nickel-platinum stanogermanide contacts for germanium-tin channel MOSFETs," *Electrochemical and Solid-State Letters*, vol. 15, no. 6, pp. H179 - H181, Mar. 2012.
7. Y. Tong, **B. Liu**, P. S. Y. Lim, and Y.-C. Yeo, "Selenium segregation for effective Schottky barrier height reduction in NiGe/n-Ge contacts," *IEEE Electron Device Letters*, vol. 33, no. 6, pp. 773 - 775, Jun. 2012.
8. **B. Liu**, X. Gong, G. Han, P. S. Y. Lim, Y. Tong, Q. Zhou, Y. Yang, N. Daval, C. Veytizou, D. Delprat, B.-Y. Nguyen, and Y.-C. Yeo, "High performance germanium Ω-Gate MuGFET with Schottky-barrier nickel germanide source/drain and low temperature disilane passivated gate stack," *IEEE Electron Device Letters*, vol. 33, no. 10, pp. 1336 - 1338, Oct. 2012.

9. L. Wang, S. Su, W. Wang, Y. Yang, Y. Tong, **B. Liu**, P. Guo, X. Gong, G. Zhang, C. Xue, B. Cheng, G. Han, and Y.-C. Yeo, "Germanium-tin n^+/p junction formed using phosphorus ion implant and 400 ℃ rapid thermal anneal," *IEEE Electron Device Letters*, vol. 33, no. 11, pp. 1529 - 1531, Nov. 2012.
10. Y. Tong, G. Han, **B. Liu**, Y. Yang, L. Wang, W. Wang, and Y.-C. Yeo, "Ni($Ge_{1-x}Sn_x$) ohmic contact formation on n-type $Ge_{1-x}Sn_x$ using selenium or sulfur implant and segregation," *IEEE Trans. Electron Devices*, 2013.
11. Xiao Gong, Genquan Han, **Bin Liu**, Lanxiang Wang, Wei Wang, Yue Yang, Eugene Yu-Jin Kong, Shaojian Su, Chunlai Xue, Buwen Cheng, and Yee-Chia Yeo, "Sub-400 ℃ Si_2H_6 Passivation, HfO_2 Gate Dielectric, and Single TaN Metal Gate: A Common Gate Stack Technology for $In_{0.7}Ga_{0.3}As$ and $Ge_{1-x}Sn_x$ CMOS", accepted by *IEEE Trans. Electron Devices.*
12. **B. Liu**, X. Gong, C. Zhan, G. Han, H.-C. Chin, M.-L. Ling, J. Li, Y. Liu, J. Hu, N. Daval, C. Veytizou, D. Delprat, B.-Y. Nguyen, and Y.-C. Yeo, "Germanium Multiple-Gate Field-Effect Transistors formed on Germanium-on-Insulator Substrate", accepted by *IEEE Trans. Electron Devices.*
13. **B. Liu**, C. Zhan, R. Cheng, P. Guo, Q. Zhou, N. Daval, C. Veytizou, D. Delprat, B.-Y. Nguyen, and Y.-C. Yeo, "Germanium Multiple-Gate Field-Effect Transistor with *in situ* Boron Doped Raised Source/Drain", accepted by *IEEE Trans. Electron Devices.*

Conference Publications

1. **B. Liu**, K.-M. Tan, M.-C. Yang, and Y.-C. Yeo, "Negative bias temperature instability of p-channel transistors with diamond-like carbon liner having ultra-high compressive stress," *Proc. 46th Annual International Reliability Physics Symposium*, Montreal, Quebec, Canada, Apr. 26-30, 2009, pp. 977-980.
2. **B. Liu**, M. C. Yang, and Y.-C. Yeo, "A new diamond-like carbon (DLC) ultra-high stress liner technology for direct deposition on p-channel field-effect transistors," *Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials*, Sendai, Japan, Oct. 7-9, 2009, pp. 773-774.
3. **B. Liu**, P. S. Y. Lim, and Y.-C. Yeo, "Effect of strain on negative bias temperature instability of germanium p-channel field effect transistor with high-k dielectric," *Proc. 47th Annual International Reliability Physics Symposium*, Anaheim, CA, USA, May 2 - 6, 2010.
4. **B. Liu**, G. Han, M.-C. Yang, Q. Zhou, S.-M. Koh, and Y.-C. Yeo, "Synthesis of high quality graphene using diamond-like carbon (DLC) as solid carbon source," *Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials*, Tokyo, Japan, Sep. 22 - 24, 2010, pp. 123 - 124.

5. X. Liu, **B. Liu**, E. K. F. Low, H.-C. Chin, W. Liu, M. Yang, L. S. Tan, and Y.-C. Yeo, "Diamond-like carbon (DLC) liner with high compressive stress formed on AlGaN/GaN MOS-HEMTs with in situ silane surface passivation for performance enhancement," *IEEE International Electron Device Meeting 2010*, San Francisco CA, Dec. 6 - 8, 2010, pp. 261 - 264.
6. **B. Liu**, M. Yang, C. Zhan, Y. Yang, and Y.-C. Yeo, "Bias temperature instability (BTI) characteristics of graphene field-effect transistors," *International Symposium on VLSI Technology, Systems and Applications* (*VLSI-TSA*), Hsinchu, Taiwan, Apr. 25 - 27, 2011, pp. 22 - 23.
7. S.-M. Koh, E. Y. J. Kong, **B. Liu**, C.-M. Ng, P. Liu, Z.-Q. Mo, K.-C. Leong, G. S. Samudra, and Y.-C. Yeo, "New tellurium implant and segregation for contact resistance reduction and single metallic silicide technology for independent contact resistance optimization in n- and p-FinFETs," *International Symposium on VLSI Technology, Systems and Applications* (*VLSI-TSA*), Hsinchu, Taiwan, Apr. 25 - 27, 2011, pp. 74 - 75.
8. Y. Ding, R. Cheng, S.-M. Koh, **B. Liu**, A. Gyanathan, Q. Zhou, Y. Tong, P. S.-Y. Lim, G. Han, and Y.-C. Yeo, "A new $Ge_2Sb_2Te_5$ (GST) liner stressor featuring stress enhancement due to amorphous-crystalline phase change for sub-20 nm p-channel FinFETs," *IEEE International Electron Device Meeting 2011*, Washington, DC, USA, Dec. 5 - 7, 2011, pp. 833 - 836.
9. Y. Tong, **B. Liu**, P. S. Y. Lim, Q. Zhou, and Y.-C. Yeo, "Novel selenium implant and segregation for reduction of effective Schottky barrier height in NiGe/n-Ge contacts," *International Symposium on VLSI Technology, Systems and Applications* (*VLSI-TSA*), Hsinchu, Taiwan, Apr. 23-25, 2012.
10. G. Han, Y. Yang, P. Guo, C. Zhan, K. L. Low, K. H. Goh, **B. Liu**, E.-H. Toh, and Y.-C. Yeo, "PBTI characteristics of n-channel tunneling field effect transistor with HfO_2 gate dielectric: New insights and physical model," *International Symposium on VLSI Technology, Systems and Applications* (*VLSI-TSA*), Hsinchu, Taiwan, Apr. 23-25, 2012.
11. **B. Liu**, X. Gong, G. Han, P. S. Y. Lim, Y. Tong, Q. Zhou, Y. Yang, N. Daval, M. Pulido, D. Delprat, B.-Y. Nguyen, and Y.-C. Yeo, "High performance Ω-gate Ge FinFET featuring low temperature Si_2H_6 passivation and implantless Schottky-barrier NiGe metallic source/drain,"*2012 Silicon Nanoelectronics Workshop* (*SNW*), Honolulu HI, USA, June 10-11, 2012.
12. R. Cheng, Y. Ding, S.-M. Koh, A. Gyanathan, F. Bai, **B. Liu**, and Y.-C. Yeo, "A new liner stressor (GeTe) featuring stress enhancement due to very large phase-change induced volume contraction for p-channel FinFETs," *Symp. on VLSI Tech. 2012*, Honolulu HI, USA, Jun. 12 - 14, 2012, pp. 93 - 94.
13. X. Gong, S. Su, **B. Liu**, L. Wang, W. Wang, Y. Yang, E. Kong, B. Cheng, G. Han, and Y.-C. Yeo, "Towards high performance $Ge_{1-x}Sn_x$ and $In_{0.7}Ga_{0.3}As$ CMOS: A novel common gate stack featuring sub-400 ℃ Si_2H_6 passivation, single TaN metal gate, and sub-1.3 nm EOT," *Symp. on VLSI Tech. 2012*, Honolulu HI, USA, Jun. 12 - 14, 2012, pp. 99 - 100.

14. Y. Tong, S. Su, **B. Liu**, L. Wang, P. S. Y. Lim, W. Wang, K. L. Low, G. Zhang, C. Xue, B. Cheng, G. Han, and Y.-C. Yeo, "Nickel stanogermanide ohmic contact on n-type germanium-tin ($Ge_{1-x}Sn_x$) using Se and S implant and segregation," *International Conference on Solid-State Devices and Materials*, Kyoto, Japan, Sep. 25 - 27, 2012.
15. Y.-C. Yeo, G. Han, X. Gong, L. Wang, W. Wang, Y. Yang, P. Guo, **B. Liu**, S. Su, G. Zhang, C. Xue, and B. Cheng, "Tin-incorporated source/drain and channel materials for field-effect transistors," *222nd Electrochemical Society Meeting*, Honolulu, HI USA, Oct. 7 - 12, 2012.
16. **B. Liu**, X. Gong, C. Zhan, G. Han, N. Daval, M. Pulido, D. Delprat, B.-Y. Nguyen, and Y.-C. Yeo, "Effect of fin doping concentration on the electrical characteristics of germanium-on-insulator multi-gate field-effect transistor," *222nd Electrochemical Society Meeting*, Honolulu, HI USA, Oct. 7 - 12, 2012.
17. X. Gong, S. Su, **B. Liu**, L. Wang, W. Wang, Y. Yang, E. Kong, B. Cheng, G. Han, and Y.-C. Yeo, "Negative bias temperature instability study on $Ge_{0.97}Sn_{0.03}$ P-MOSFETs with Si_2H_6 passivation and HfO_2 high-k and TaN metal gate," *222nd Electrochemical Society Meeting*, Honolulu, HI USA, Oct. 7 - 12, 2012.
18. R. Cheng, X. Gong, P. Guo, F. Bai, Y. Yang, **B. Liu**, K. H. Goh, S. Su, G. Zhang, C. Xue, B. Cheng, G. Han, and Y.-C. Yeo, "Top-down GeSn nanowire formation using F-based dry etch and H_2O_2-based wet etch," *43rd Semiconductor Interface Specialist Conference*, San Diego, CA, USA, Dec. 6-8, 2012.
19. H.-C. Chin, M.-L. Ling, **B. Liu**, X. Zhang, J. Li, Y. Liu, J. Hu, Y.-C. Yeo, "Metrology solutions for high performance germanium multi-gate field-effect transistors using optical scatterometry," *Proceedings of SPIE*, vol. 8681, *Metrology, Inspection, and Process Control for Microlithography XXVII*, San Jose, CA USA, Feb. 24-28, 2012.
20. E. Kong, X. Gong, P. Guo, **B. Liu**, and Y.-C. Yeo, "Novel technique for conformal, ultra-shallow, and abrupt n^{++} junction formation for InGaAs MOSFETs," *International Symposium on VLSI Technology, Systems and Applications* (*VLSI-TSA*), Hsinchu, Taiwan, Apr. 22-24, 2013.
21. P. Guo, C. Zhan, Y. Yang, X. Gong, **B. Liu**, R. Cheng, W. Wang, J. Pan, Z. Zhang, E. S. Tok, G. Han, and Y.-C. Yeo, "Germanium-tin (GeSn) n-channel MOSFETs with low temperature silicon surface passivation," *International Symposium on VLSI Technology, Systems and Applications* (*VLSI-TSA*), Hsinchu, Taiwan, Apr. 22-24, 2013.
22. C. Zhan, W. Wang, X. Gong, P. Guo, **B. Liu**, Y. Yang, G. Han, and Y.-C. Yeo, "(110)-oriented germanium-tin ($Ge_{0.97}Sn_{0.03}$) p-channel MOSFETs," *International Symposium on VLSI Technology, Systems and Applications* (*VLSI-TSA*), Hsinchu, Taiwan, Apr. 22-24, 2013.
23. H.-C. Chin, **B. Liu**, X. Zhang, M.-L. Ling, C.-H. Yip, Y. Liu, J. Hu, and Y.-C. Yeo, "Metrology solutions using optical scatterometry for advanced CMOS: III-

V and Germanium multi-gate field-effect transistors," *Proceedings of SPIE*, *Optical Measurement Systems for Industrial Inspection VIII*, Munich, Germany, May, 2013.

24. Y. Ding, X. Tong, Q. Zhou, **B. Liu**, A. Gyanathan, Y. Tong, and Y.-C. Yeo, "A new expandible ZnS-SiO_2 liner stressor for n-channel FinFETs," *Symp. on VLSI Tech. 2013*, Kyoto, Japan, Jun. 11-13, 2013.
25. X. Gong, G. Han, S. Su, R. Cheng, P. Guo, F. Bai, Y. Yang, Q. Zhou, **B. Liu**, K. H. Goh, G. Zhang, C. Xue, B. Cheng, and Y.-C. Yeo, "Uniaxially strained germanium-tin (GeSn) gate-all-around nanowire PFETs enabled by a novel top-down nanowire formation technology," *Symp. on VLSI Tech. 2013*, Kyoto, Japan, Jun. 11-13, 2013.