SCANNING THERMAL MICROSCOPY METHODOLOGY FOR ACCURATE AND RELIABLE THERMAL MEASUREMENT

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SUMMARY

The rapid scaling of semiconductor devices coupled with demand for increasing interconnect density, current density, power consumption and introduction of new materials such as low-k dielectric with poor thermal conductivity exacerbates device reliability with increasing temperature dependence. The introduction of multi-core processor with an ever increasing array of sensors such as accelerometer, gyroscope and proximity sensor into portable devices has also placed greater focus on the thermal budget.

There is therefore a need for thermal characterization and measurement of these devices and materials. Scanning Thermal Microscopy is one thermal measurement technique with great spatial and thermal resolution to be compatible with advance technology node and beyond. However, since it is a probe based technique and due to its sensitivity, topography artifacts are easily coupled into the thermal measurement due to changing thermal contact area between the scanning probe and the device-under-test (DUT). It is also affected by thermal drift and overall heating of the DUT during the whole measurement process.

The proposed setup introduces another lock-in amplifier into the measurement system. This has allowed for the compensation of varying thermal contact area at each measurement point, eliminating the effect of topography coupling into the thermal measurement. Furthermore, any effect from thermal drift and overall heating of the DUT will be limited to the dwell time of the thermal probe at each data collection point. The setup has been demonstrated successfully on an electromigration structure and sensitive down to a current supply of 7 mA (0.264 MA/cm^2). This has enabled the sensitive Scanning Thermal Microscopy technique to be more accurate and reliable for thermal analysis. Calibration of the setup shows a sensitivity of about 0.584 V/K at the output of the first lock-in amplifier.

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List of Abbreviations

ITRS	International Technology Roadmap for Semiconductor
DRAM	Dynamic Random Access Memory
NA	Numerical Aperture
MPU	Microprocessor
SThM	Scanning Thermal Microscopy
SJEM	Scanning Joule Expansion Microscopy
PID	Proportional-integral-derivative
AFM	Atomic Force Microscope
LIA	Lock-In Amplifier
SPM	Scanning Probe Microscope
SFM	Scanning Force Microscope
STM	Scanning Tunneling Microscope
EOM	Electro-optic Modulator
DUT	Device-Under-Test
ECU	Electronic Control Unit
CH1	Channel 1
Ag	Silver
Pt	Platinum
a.c.	Alternating current
1D	1-directional
SLIA	Single Lock-In Amplifier
EM	Electromigration

TC	Time Constant
RMS	Root Mean Square
VCO	Voltage-Controlled Oscillator
PSD	Phase Sensitive Detector
DC	Direct Current
LPF	Low Pass Filter
SNR	Signal –to-Noise Ratio
DLIA	Double Lock-in Amplifier
SNPEM	Scanning Near-Field Photon Emission Microscopy
PET	Poly (ethylene terephthalate)
EC	Electrocaloric
MLC	Multilayer capacitor
NPM	Nullpoint method

List of Symbols

$\boldsymbol{j}$	Irradiance with dimension of energy flux
$\boldsymbol{\varepsilon}$	Emissivity
σ	Stefan-Boltzmann constant
T	Absolute temperature
λ	Wavelength
l	Mean free path
C	Capacitance
V	Voltage supply
f	Frequency
$R_{probe}(T)$	Resistance of probe at temperature T
R_0	Resistance of tip at ambient temperature T_0
α_{probe}	Coefficient of resistivity of the probe
ω	Angular frequency
ω_p	Angular frequency of DUT biasing
ΔT_n	Thermal measurement noise
T_s	Sample/substrate Temperature
T_a	Ambient Temperature
R_c	Cantilever thermal resistance
R_t	Tip resistance
R_{ts}	Probe-sample resistance

C_p	Specific heat capacity
κ	Thermal conductivity
Δv_0	Change in output voltage
$\Delta R_4(T)$	Resistance change of the resistive probe
K_R	Wheatstone bridge sensitivity
R^2	Linear regression goodness of fit
$P(t)$	Power of periodic pulsed heating
P_0	Peak power of unipolar rectangular current bias
C_{th}	Thermal capacitance
R_{th}	Thermal resistance
t_p	DUT biasing period
ΔT_m	DC joule heating of sample
τ_{th}	Sample thermal time constant

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Chapter 1: Introduction

1.1 Scaling Trend

The semiconductor industry has been and is still experiencing a rapid pace of downscaling which has kept pace with Moore's Law prediction of doubling the transistor density on a manufactured die every 24 months. According to the 2012 International Technology Roadmap for Semiconductors (ITRS) [1] where industry-wide consensus on semiconductor trends is presented, the DRAM half-pitch is predicted to scale by approximately 0.7 times every 3 years as shown in Fig. 1.1.

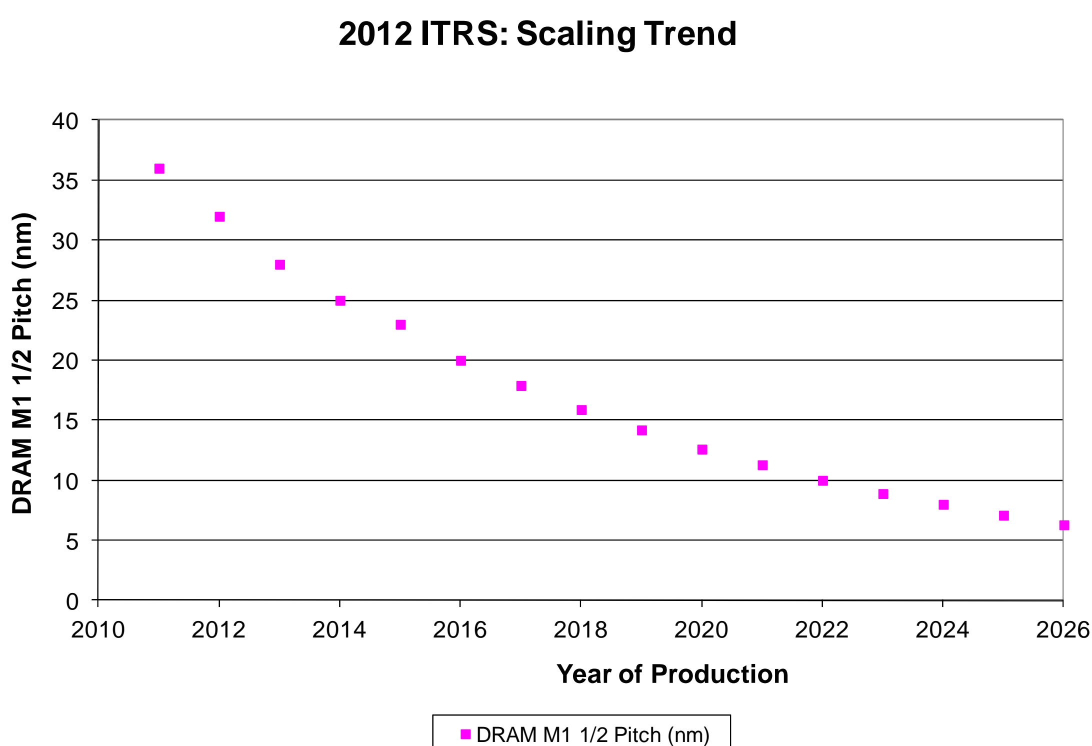


Figure 1.1: DRAM M1 ½ Pitch Scaling Trend

This downscaling has facilitated the reduction of cost per function and allowed for the continued market growth for integrated circuits. The MPU density is also expected to

double every 2 years till 2013 and then expected to continue doubling on a 3 year cycle. Meanwhile, the DRAM bits/chip continues doubling on a 3 year cycle as well. However, this traditional/geometrical scaling is getting very challenging. This can be easily observed in foundries where one of the bottlenecks and cost is the lithography tools. A current 193 nm immersion lithography machine can cost up to US$40 million per unit. Furthermore, it is limited by numerical aperture (NA) to resolve 32 nm half pitch and requires creative lithography solutions such as double patterning or exposure. This allows the pitches to be split into larger ones, but at the expense of almost twice the lithography cost.

Other than the traditional scaling or geometrical scaling as called for in Moore's Law, equivalent scaling such as introduction of stress into the channel to improve transistor performance, innovative processing such as using tri-gate or gate-all-around transistors are taking an even more significant role in the future trends of microelectronics. More innovative methods being explored include the use of nanowires and nanotubes for electron transport, using III-V compounds as replacement for silicon transistors or the use of photons in optoelectronics to transmit data.

1.2 Thermal Management

With an increase in the complexity of microelectronic circuits, the power density also increases with more heat generated per device. Heat generation and conduction can influence the reliability of semiconductor devices and interconnects. Thermal management is therefore becoming an increasingly important factor in the performance

of advanced microelectronic devices. Hence, understanding and controlling the heat transfer by being able to characterize the thermal behaviour is of significant interest in practical applications concerned with heat management.

1.2.1 Thermal Transport

Heat is the transfer of energy from one body to another as a result of thermal contact. Thermal contact facilitates the transfer of energy namely by three modes, conduction, convection and radiation. In electronic devices, electron flow occurs in metals and semiconductors. For heat, it flows through all materials.

Convection is the main heat transfer mechanism in liquids and gases. It consists of fluid flow between hot and cold regions and heat transfer by conduction. As for radiation, it can occur without any medium in the form of electromagnetic waves. Stefan-Boltzmann law states that the total energy radiated per unit surface area per unit time is proportional to the fourth power of temperature as shown in Eqn. 1.1.

$$j = \varepsilon \sigma T^4 \qquad (1.1)$$

where j is irradiance with dimension of energy flux (energy per unit area per unit time), ε is emissivity ($\varepsilon = 1$ in the case of a perfect black body), σ is the Stefan-Boltzmann constant and T is the absolute temperature.

In solids at the microscopic level, thermal transport is predominately through conduction by two energy carriers. Electrons flow in metals, and phonons (lattice vibration) in insulators and semiconductors [2]. Table 1.1 lists the typical range of values for the

length and time scales of electrons and phonons. This also defines the physical resolution limits for thermal measurements.

Table1.1: Typical Length and Time Scales for Energy Carriers In Solids at Room Temperature [2]

	Electrons In Metal	Phonons in Insulators and Semiconductors
Wavelength, λ [nm]	0.1 – 1	1 – 5
Mean Free Path, l [nm]	10	10 – 100
Relaxation Time, τ [s]	(10 – 100) x 10^{-15}	(1 – 10) x 10^{-12}
Propagation speed, υ [m/s]	10^6	(3- 10) x 10^{-3}

Although thermal conductivity is an intrinsic property, studies have shown that the thermal conductivity of thin films is also affected by film thickness and microstructure. A reduction in thermal conductivity of 10% for films in the 1 μm range [3] and up to 50% reduction for films on the order of 100 nm [4] compared to bulk silicon have been observed. Doping also affects silicon films' thermal conductivity [5] while grain boundary scattering is a factor for thermal conductivity reduction in polysilicon films [6][7][8]. When the hotspot is less than the phonon mean free path, localized heating occurs, resulting in significant increase in thermal resistance for conduction. Therefore, thermal characterization is essential as its behaviour can be drastically different from its bulk performance.

Cahill [9] has provided a comprehensive review of the theory, experiments and simulation models of the current understanding of thermal transport at nanoscale level. In the area of computational approach to heat transfer, numerical solutions of Fourier's law [10] to calculation based on the Boltzmann transport equation [11][12] to atomic level simulations have been discussed and reviewed.

1.2.2 Thermal Transport of Probe In Contact with Sample

In the context of a thermal probe in contact with a sample, the relative contribution of the various heat transfer mechanisms had been studied extensively by Shi et al. [13][14] using a thermocouple based probe as shown in the following schematic diagram.

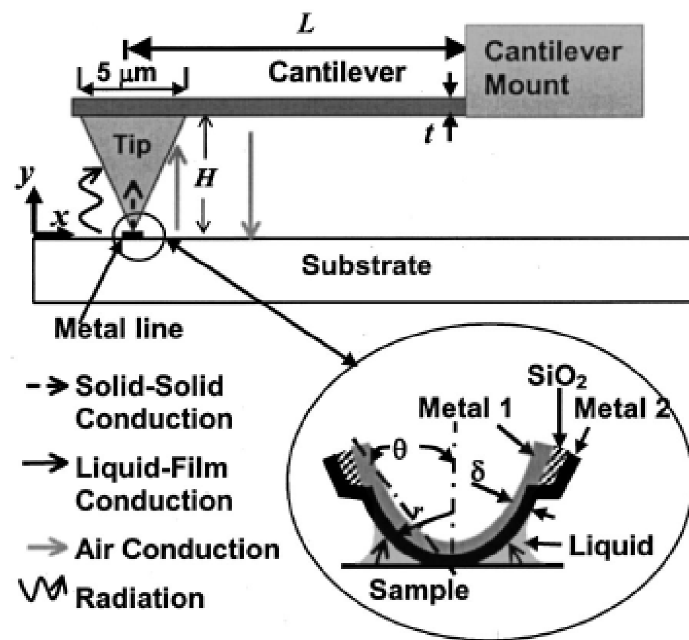


Figure 1.2: Schematic diagram of a SThM probe in contact with a Joule heated metal line. Also shown are various tip-sample heat transfer mechanisms. [14]

The various heat transfer mechanisms include

- solid-solid conduction at the probe contact
- conduction through the air gap between the probe and the sample
- radiation
- heat conduction through the liquid meniscus formed at the probe-sample junction.

The liquid meniscus is formed from water molecules and/or contaminations adsorbed on the sample and probe surfaces.

To determine the relative contribution of various probe-sample heat transfer mechanisms, Shi et al. [14] Joule heated a 350 nm wide line above room temperature and recorded the cantilever deflection and probe temperature simultaneously as the sample was raised towards and then retracted from the thermal probe. The following plot shows the cantilever deflection and temperature response.

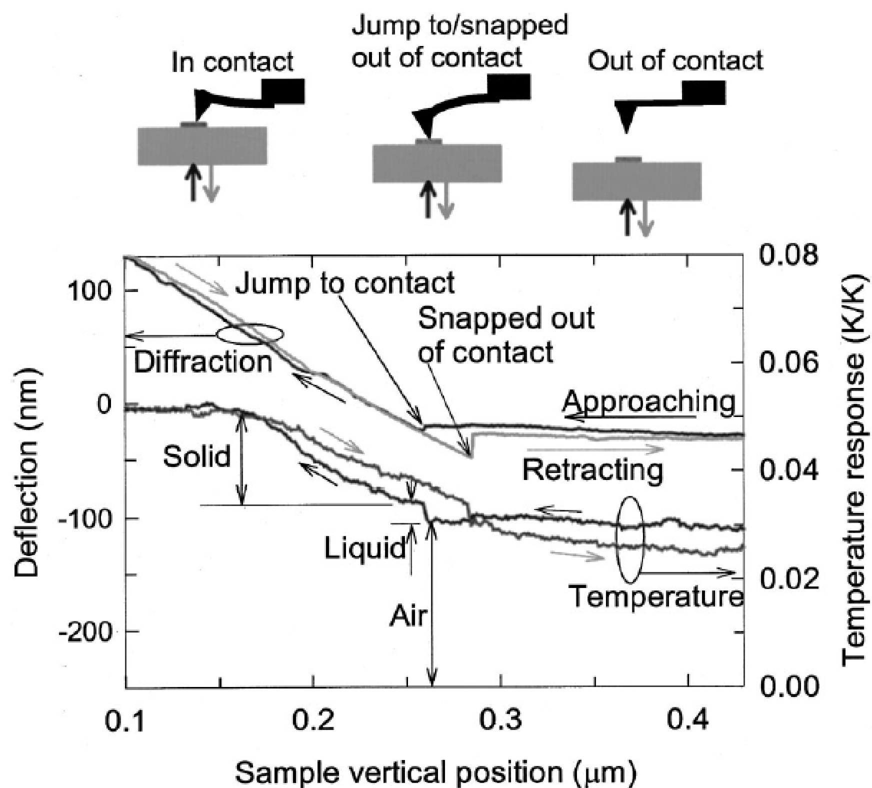


Figure 1.3: Cantilever deflection and temperature response of the probe as a function of sample vertical position when the 350 nm wide line was raised towards and then retracted from the tip

In the initial approaching phase before contact (no deflection of cantilever), the temperature response is mostly due to air conduction between the probe and the sample.

Radiation contribution is negligible when both sample and probe are close to room temperature [15]. Studies by Lee et al. [16] and Kim et al. [17] also concluded that radiative heat transport is insignificant even when contact is made. The temperature response due to air conduction increases slowly as the probe-sample distance is reduced.

Before the sample made solid-solid contact to the probe, the adsorbed liquid layers on the tip and the sample bridged each other. This liquid bridge pulled the probe down by van der Waals force and is labeled as "jump to contact" in Fig. 1.3. At the same time, the temperature response observed a small spike due to thermal conduction through the liquid bridge.

As the sample is raised further, the solid-solid contact force also increases linearly. This is accompanied by corresponding gradual increase in the temperature response until the deflection reached 100 nm higher. The temperature response then flattens out. The linear increase in temperature response is attributed to the increase in contact area due to roughness on the surface of the probe and sample. As the contact size approached the diameter of the asperity, the contact area could not be increased with increasing contact force, thus resulting in no further increase in temperature response. Therefore, probe sample heat transfer is favored by solid-solid contact and water meniscus with averaged radii of 20-50 nm and 100-200 nm respectively. [18][19] The spatial resolution of the probe is determined by the characteristic length of the predominant heat transfer mechanism between the probe sample interaction.

Duvigneau [20] has also studied the thermal transport around nanoscale contact area between heated AFM probe tip and polymer films. He investigated the lateral heat transport using polarized light microscopy and AFM imaging of the temperature-induced crystallization of poly (ethylene terephthalate) (PET) films in the region near the probe tip. Heated probe induced crystallization of amorphous PET resulted in the formation of near circular semicrystalline domains. The periphery of the domain boundaries was considered as a surface isotherm at 133 °C. The radii of the observed lateral surface isotherms ranged from 2.2 ± 0.5 to 18.7 ± 0.5 μm as was revealed with AFM and polarized light microscopy for heated AFM probe tip temperatures between 200 and 300 °C and contact times varying from 20 to 120 s. The heat transport in the z direction into the polymer films was observed to occur to depths of over 1000 μm.

1.2.3 Thermal Challenges

Recently, there is a great proliferation of portable devices such as tablets and smart phones integrated with many features. They are expected to handle intensive graphical capabilities that were once the realm of desktop computers. They need to be able to handle multiple types of mobile network (e.g. GSM, EDGE, LTE) and support various wireless protocols. Furthermore, they come with an ever increasing array of sensors such as an accelerometer, gyroscope and proximity sensor. This calls for low power, high performance devices with stringent requirement for thermal management. The trend of introducing multiple cores for microprocessors and graphical processing units makes thermal management one of the key challenges to be addressed.

The thermal issue is even more pronounced in the area of interconnects in terms of requirement and innovation. Conductor resistivity is increased as interconnect line width approaches the electron mean free path. Low-k materials are introduced as dielectrics to have low RC delay but have poor thermal conductivity. This is made worse with the use of porous materials especially for κ value <2. The requirement for increasing current density of interconnects means greater reliability issues such as electromigration (EM).

The power consumption P is related to chip operating frequency f as follows:

$$P = CV^2 f \tag{1.2}$$

where C is the capacitance, V is the supply voltage and f is the chip operating frequency.

According to the latest ITRS (2012) update, the on-chip clock frequency is projected to increase 1.08 times every 3 years as shown in Fig. 1.4. This is down from the previously (ITRS 2009) more aggressive projection of 1.7 times. However, it still means projected increasing power consumption.

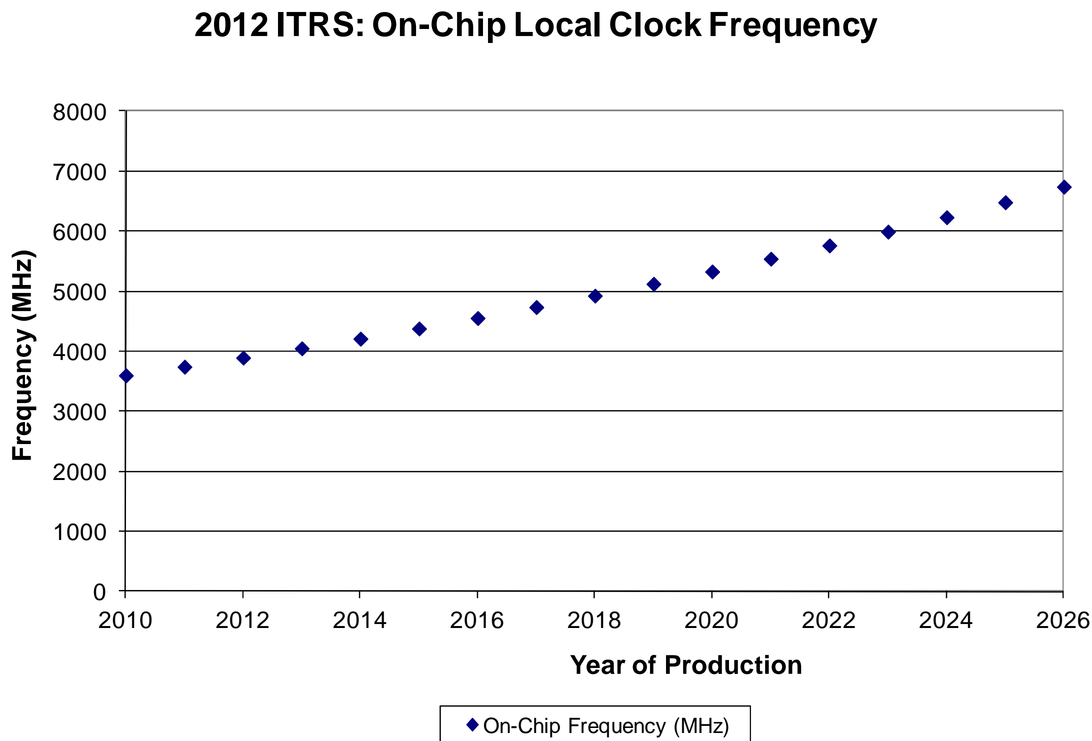


Figure 1.4: On-Chip Frequency Trend

Together with the increase in interconnect density, number of metal layers, current density and power consumption; failures are exacerbated since reliability has a strong dependence on temperature. Furthermore, operating temperature affects the performance of semiconductor devices. This can be observed in the increased leakage and reduced maximum operating frequency of microprocessors as temperature increases. The transconductance of transistors is also affected by increasing temperature. An increase of the ambient temperature of surface-passivated GaN-based field-effect transistors from 25 °C to 250 °C degrades the saturation current and transconductance by 33 % [21].

It is thus of major importance to future technological growth to be able to perform temperature measurements and characterization of thermal properties of new materials

and at nanoscale regime where the physics may be entirely different from its bulk properties. The understanding of thermal transport physics, determination of thermal properties and the measurement of temperature with spatial resolution at sub-100 nm scale is critical for the analysis of reliability failures at these nodes. As a result, there is a need for a comprehensive technique for the localization and characterization of these thermal issues with spatial resolution of the order of the critical defect size with sufficient thermal resolution.

1.3 Project Motivation

Measurement techniques based on scanning probe microscopy have enabled direct observation of various phenomena on nanoscale devices and structures with high spatial resolution. One of such techniques, Scanning Thermal Microscopy (SThM), has the ability of measuring temperature and thermophysical properties with a nanoscale spatial resolution. However, there are some inherent issues associated with current SThM measurement system and these include temperature drift and topography artifacts. The motivation of this project is therefore to develop a SThM methodology to provide a more accurate thermal profile of devices being characterized. The double lock-in (DLI) technique for SThM is also proposed to reduce these issues by essentially performing per point compensation of local condition at each probe location.

This thesis is organized and presented as follows:

Chapter 2 provides a literature review of thermal measurement techniques with specific focus on AFM based SThM measurement. The use of double lock-in signal enhancement technique and some of its current applications is also discussed.

Chapter 3 begins with an overview of the various types of bridges available. It then proceeds to discuss the Wheatstone bridge used for thermal detection in the experimental setup. A systematic approach to balance the ac bridge is also covered before proceeding to look into the bridge response in terms of linearity and sensitivity. Efforts geared towards achieving a stable bridge setup are also covered.

Chapter 4 discusses the rest of the instrumentation that goes into the setup of the resistance based SLIA SThM. The two modes of configurations available to the SLIA SThM, temperature and thermal conductivity measurement, are also covered. This includes calibration done for the temperature measurement mode. The chapter concludes with emphasis on the importance of achieving a level scanning plane between the thermal probe and the DUT so as to achieve accurate thermal measurement.

Chapter 5 covers some of the temperature and thermal conductivity measurement applications performed on samples such as the electromigration test structure and unshielded type hard disk TFC PMR head.

Chapter 6 highlights the two main issues affecting thermal probe based SThM. These are the problem of topography artifacts as well as temperature drift in the overall measurement system with some amount of settling time required after equipment powerup. Various algorithms are also discussed on processing the acquired thermal signals so as to minimize the noise coupled into the measurement as a result of temperature drift.

Chapter 7 introduces the double lock-in technique for SThM aimed at overcoming the issues highlighted in the previous chapter. The theoretical and mathematical models are provided. A systematic approach to optimization of the various parameters for enhancement of detection sensitivity is also discussed.

Chapter 8 demonstrates the application of the DLI SThM using an electromigration sample to study the sensitivity of the double lock-in measurement with respect to single lock-in setup for a DUT under various heating current.

Chapter 9 concludes the thesis and summarizes the key contribution of this research project.

Chapter 10 proposes potential future work for an equivalent setup tailored for thermal conductivity measurement.

Chapter 2: Literature Review

2.1 Review of Thermal Measurement Techniques

As highlighted in the previous chapter, the scaling of electronic devices and requirement of ever increasing operating frequencies, increasing current and interconnect density results in thermal budget concerns. This affects the performance and accelerates thermal related failures and reliability issues. Thus there is an ever increasing requirement for localization and characterization of these thermal issues. There are many ways in which the temperature can be measured. It can be through temperature related material properties such as thermal expansion coefficient, luminosity and resistance. The device operating conditions such as PN junction forward voltage and threshold voltage are also strong functions of temperature. A large variety of thermal measurement techniques thus exist by association with these parameters.

Thermal measurement can be broadly categorized into 3 main groups of electrical, optical and physical contact. [22]

Electrical means can include using the forward voltage of a PN junction [23] for temperature monitoring. Examples include use in bipolar transistors [24], power MOSFETs [25] and laser diodes [26]. The threshold voltage can also be used to correlate with temperature [27] and has been used to measure the temperature of power Insulated Gate Bipolar Transistors [28]. Thermal voltage noise is induced when the rate of current flow through an electrical resistor fluctuates due to phonon scattering. The thermal voltage noise is proportional to the square root of temperature [29]. Measurement of this

thermal noise voltage yields the temperature of the resistor. Bunyan et al. [29] fabricated silicon on insulator MOSFET with multiple body contacts along the length of the body. By measuring the thermal noise voltage associated with the resistor between two body contacts, the average temperature of the silicon island is obtained. These electrical means are useful for acquiring the average temperature of a device without requiring physical access. The major advantage of using temperature sensitive electrical parameter for thermometry is that it can be performed on packaged devices, and is useful for temperature measurement of layers that are buried deep below the device surface. However, they cannot provide detailed thermal micrographs for further characterization. There is also the impact of non-isothermal temperature distribution in the device on the measured electrical parameter.

Optical techniques explore the temperature dependence of the optical properties near the surface of the sample. High temporal resolution can be achieved as there is no thermal mass or electrical capacitance involved as in the electrical techniques. Temperature measurement can be modeled as a function of the radiation emitted due to external stimulation, commonly known as luminescence [30]. The source of mobile carriers can be through injection across a PN junction (Electroluminescence) [30] or by external optical excitation (Photoluminescence) [31][32]. A resolution of 0.5 – 1 μm and 1 K is claimed.

Recently, Aigouy et al. [33] have developed a scanning thermal probe microscope that operates in liquid environments. The thermal sensor is a fluorescent particle glued at the

end of a sharp tungsten tip. Since light emission is a strongly thermally sensitive effect, the measurement of the particle fluorescence variations allows the determination of the temperature. No electrical wiring of the probe is needed. The sample is a 35 nm thick Ni microheater (4 µm wide and 40 µm long) connected to two Ni pads on which electrical connections are made. The whole structure was passivated with a 100 nm thick SiO_2 layer. Figure 2.1 shows the result obtained at 0 and 13 mA supply current.

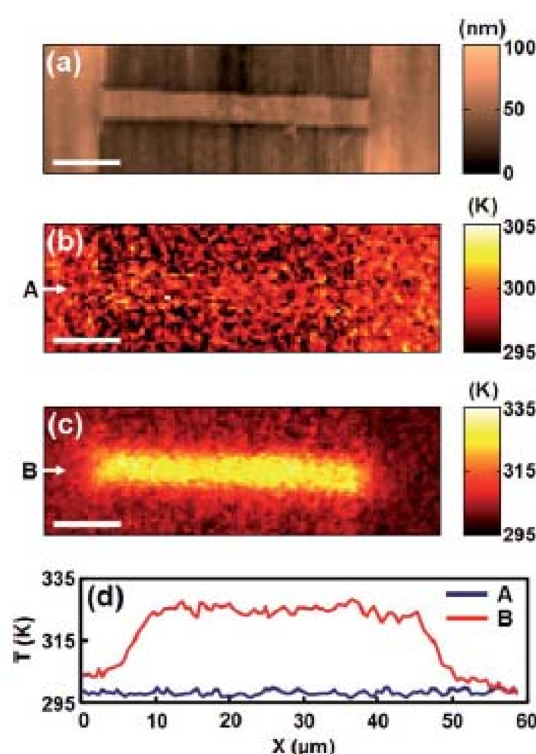


Figure 2.1: (a) Topography and (b) PL intensity ratios converted to temperature for i = 0 mA and (c) i = 13 mA. The scale bar is 10 µm. (d) The curves are cross sections extracted from the images in (b) and (c) in directions A and B.

The scans were performed in approximately 30 min. For i = 0 mA, the PL intensity ratio does not exhibit any contrast and the temperature is 298 K (Fig. 2.1(b)). For i = 13 mA, the image clearly reveals a temperature increase along the stripe where Joule effect occurs (Fig. 2.1(c)).

As for Raman scattering, the spectra of the scattered photon will be dependent upon the temperature of the crystal. Spatial and temperature resolutions of 1 μm [34] and 1-2 K [35] have been reported respectively. Thermoreflectance is another optical means using the intensity of reflected photon which is temperature dependent. Very fast measurement time of 10 ns [36] has been reported with spatial resolution of 1 μm [37]. Finally, there is infrared thermography [38][39], where temperature is measured by relating to the radiation intensity of the heated DUT according to Planck's blackbody law. This allows for fast acquisition. From Wien's displacement law, blackbody radiation peaks at a wavelength of about 10 μm at room temperature, which gives a resolution that makes infrared thermography appropriate for qualitative thermal mapping for hotspot detection over relatively large areas of an integrated circuit surface. One application shown by Kondo and Hinode [40] was to monitor the long timescale interconnect electromigration process as shown in Fig. 2.2. Real time interconnect temperature distribution was monitored for 10^3 seconds. Temperature of the cathode side rose by more than 100 K due to void formation.

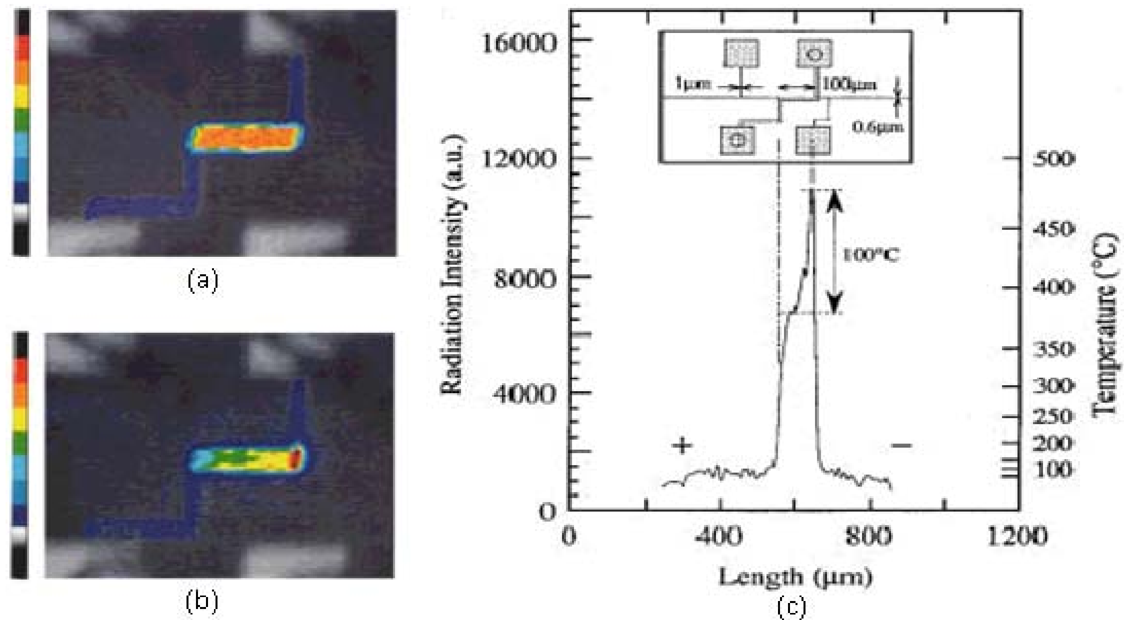


Figure 2.2: Thermograph image of an interconnect after accumulated for 10s [40]
(a) before electromigration (b) after electromigration (c) Temperature profile of (b)

Yet, great effort in calibration and adjustment factor have to be considered according to the emissivity of the various materials on the DUT since none of these will be acting like an ideal blackbody. However, the main concern with optical technique is the diffraction limit. This places a natural limit on how high a spatial resolution can be achieved.

The final category of thermal measurement requires physical thermal contact with the DUT. Liquid crystal thermography [41] is such a technique and is useful for fast localization of hot spots, especially with advances in thermochromic liquid crystals allowing for good thermal resolution. It is essentially a localization technique by means of determining the relative temperature across a sample and useful if the area of concern is large. Spatial resolution of 1 μm [42] and temperature resolution of 0.1 K [43] have been demonstrated. Scanning probe microscopy is another group of thermal measurement

techniques requiring thermal contact. It has the advantage over optical methods without the constraint of having resolution limited by the Rayleigh criterion. This allows for much improved spatial resolution which is only limited by the physical size or the actual thermal contact the probe makes with the DUT. The SThM technique is able to provide one of the best spatial resolutions while providing reasonable temperature resolution. It is also very versatile, allowing for various configurations and is able to characterize various aspects of the DUT such as local temperature or its thermal conductivity. This makes it a suitable choice to be used as a thermal analysis tool that is compatible with advances in microelectronic devices.

2.2 AFM based SThM Measurement

As highlighted earlier, one obvious advantage of near-field probe based techniques over far-field optical techniques is that resolution is not diffraction limited but dependent on the effective contact area of the probe with device under test (DUT). Another benefit is the simultaneous capture of topography information which is useful when doing thermal analysis. This allows for direct visualization and knowledge of where and how the thermal profile responds across the DUT.

In scanning thermal microscopy (SThM), an AFM-based system is preferred over an STM-based system as it allows for application on a variety of materials such as insulators, semiconductors and metals. The AFM-based system does not rely on the presence of a tunneling current from a conductive surface. It is also very versatile where various types of sensors can be placed at the probe tip, allowing for different configurations and studying of the different aspects of localized thermal characteristics.

At the microscopic level, the contact area increases linearly with contact force between two rough surfaces [44]. At sufficiently large contact forces, the contact size between the sample and asperity on the probe end approached the asperity diameter, and could not increase further with contact force. The constant contact force feedback mechanism of the AFM allows for the applied force of probe on sample to be consistent. This eliminates the concern of contact force related resistance change influencing the measured thermal signals. This is especially important when the thermal sensor is resistance based. However, varying contact area (at constant contact force) due to changing topography

across the DUT will still be unavoidable and be coupled with the thermal signals. This issue was also noted by Christofferson [45] in his measurement of the temperature distribution across a microcooler device. In the measurement, he noted that the thermal micrograph of the cooler surface produces a noisy thermal map. This is attributed to the surface of the processed device having some roughness. This surface roughness affects the effective thermal contact between scanning probe tip and sample.

Before going into the various types of scanning thermal microscopes available, a typical scanning thermal system can be broadly grouped into the following components [46]:

i. The thermal probe as a near-field temperature sensor;
ii. A source of heat which may be external or internal to the sample and may be incorporated into the probe itself;
iii. A cantilever whose deflection senses the force that acts between the probe and sample;
iv. One or more feedback systems such as force feedback or thermal feedback.

Fig. 2.3 shows a flow chart of the various types of scanning thermal microscopes available.

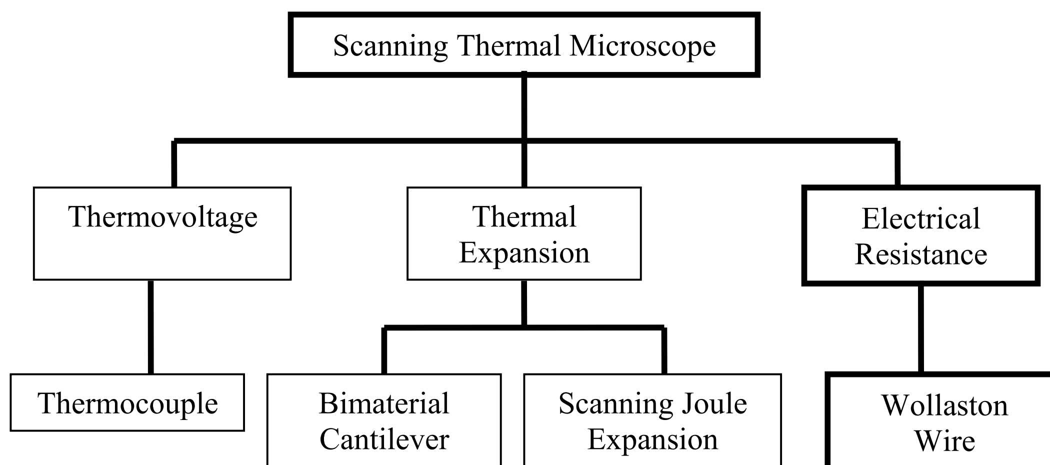


Figure 2.3: Flow Chart of Various Scanning Thermal Microscopy System

They are classified according to the mechanism used to correlate with temperature changes such as thermovoltage, thermal expansion or resistance change [47]. A more detailed description of each category is described in Section 2.2.1 – 2.2.3.

2.2.1 Thermovoltage

Thermovoltage-based technique uses a thermocouple at the tip of the scanning probe and can be used either in the non-contact mode or contact mode in a STM or AFM system. The thermal noise limit for thermocouple measurements and its corresponding noise-equivalent spatial resolution (NESR) have been discussed by Majumdar [47]. The thermal noise limit determines the theoretical minimum temperature resolution that the thermocouple is able to distinguish. It is dependent on parameters such as measured temperature, electrical resistance of thermocouple junction and bandwidth of measurement.

There are many thermovoltage based techniques available; this includes the Scanning Thermal Profiler [48], Tunneling Thermocouple [49], Wire Thermocouple [50], Thin-Film Probes [51] and Micromachined Schottky Diodes [52]. These techniques have good spatial resolution down to the nanometer regime. The limitation of thermal profiler is that feedback signal for topography is coupled to temperature measurement. Disadvantage of tunneling thermocouple is the requirement of a conducting surface or a surface treated with a metallic film. This will reduce the candidates for thermal analysis as it may result in shorts on certain devices and makes it impossible for thermal analysis. Some of the thermocouple probes either have too low a melting point or are too soft, deforming under contact after a few measurements. Also, thermocouple probes essentially only allow for measurement of local temperature but not local thermal conductivity. Thus thermal analysis application may be limited. Another limitation for thermocouple probe lies with gas conduction being the dominant heat transfer mechanism, thus requiring the technique to be applied in vacuum to achieve improved spatial resolution.

Nakabeppu et al. [53] carried out the active temperature measurement under 0.1 Pa by putting the AFM into a vacuum chamber to detect thermal information through the small contact region. A multi-functional thermal cantilever in the fabrication stage before depositing the gold film on its reverse is used as shown in Fig. 2.4. Nickel and chromium metal lines comprise the differential thermocouple, electric heater, and another thermocouple in about 150 μm region on the SiO_2 cantilever of 260 μm length.

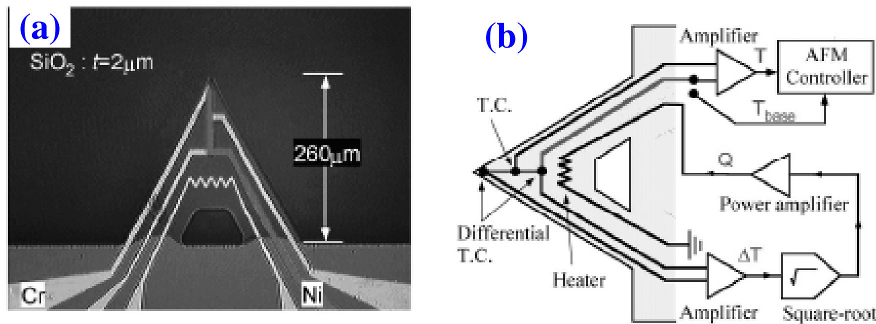


Figure 2.4: (a) SEM of multi-function micro thermal cantilever, and (b) block diagram of thermal feedback system

In order to eliminate the influence of the heat transfer through the air, Kim et al. [54] developed a double scan technique to measure the temperature of the sample from the tip-sample heat transfer only. In the first scan, the topography of the sample and the thermoelectric signal from the SThM probe (Fig. 2.5), which has a nanothermocouple junction at the end of tip, are measured simultaneously by scanning the probe on the sample surface in controlled force-contact mode.

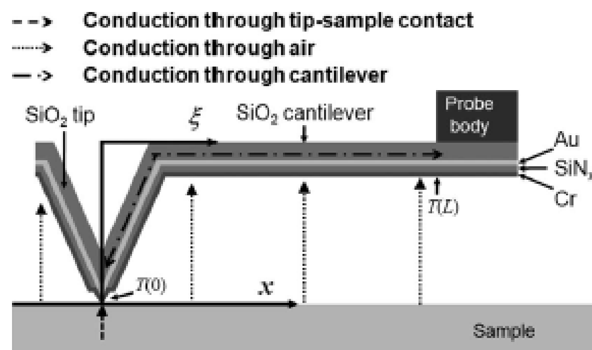


Figure 2.5: Schematic diagram of SThM probe in contact with sample and various heat transfer paths around the probe.

The thermoelectric signal measured at this time, is the signal that is due both to the heat transfer through the tip-sample contact and the one through the air. In the second scan, the SThM probe is scanned along the same line as the first scan at a constant height

above the sample surface using the topography data obtained from the first scan. The thermoelectric signal measured at this time is due to the heat transfer through the air only. Then, the difference between the thermoelectric signal obtained in the first scan by contact mode and the signal in the second scan by lift mode is the signal due to the heat transfer through the tip-sample contact only. Figure 2.6 shows schematically the principle of quantitative thermal profiling with the double scan technique.

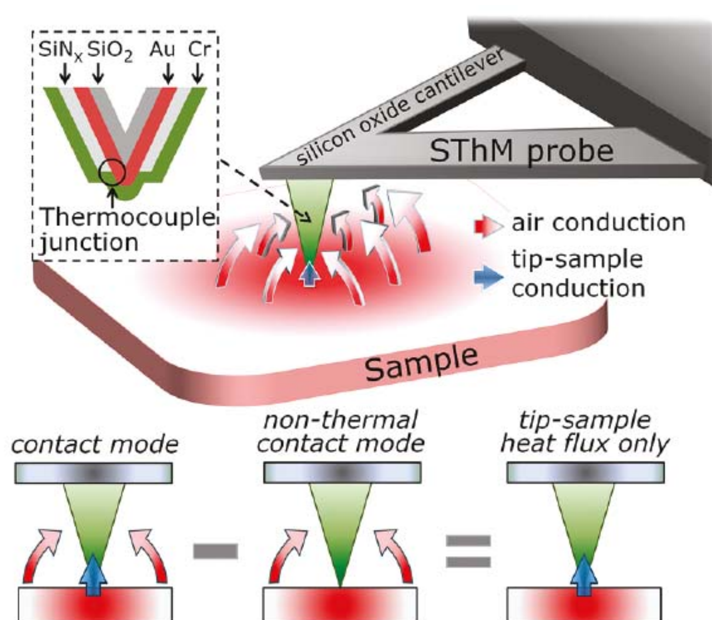


Figure 2.6: Schematic on principle of quantitative thermal profiling using double scan technique [55]

However, if the thermal conductance of the tip-sample thermal contact is disturbed due to abrupt changes in the surface topography and/or surface properties such as hydrophilicity, quantitative measurement becomes difficult. To overcome this limitation, Chung et al. [56] developed the nullpoint method (NPM) by which one can quantitatively measure the local temperature of a sample with SThM, independent of disturbances in the tip-sample

thermal conductance. The experimental setup for NP SThM is show in Fig. 2.7 (a); where a thermocouple probe (Fig. 2.7 (b)) is used to scan across the sample surface.

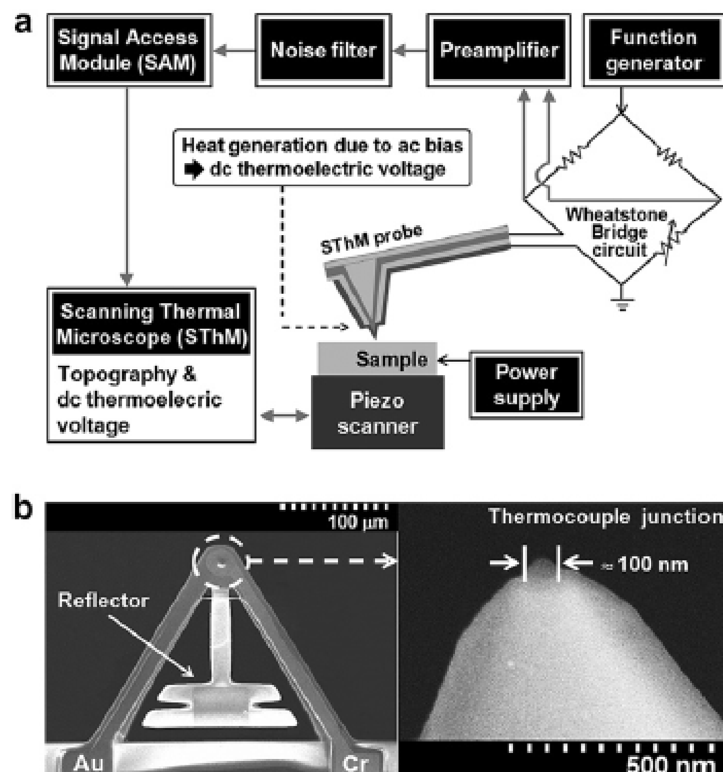


Figure 2.7: (a) A schematic diagram of the experimental setup for NP SThM. (b) SEM images of the SThM probe used in the experiment. The diameter of the thermocouple junction integrated at the apex of the tip is about 100 nm, and the tip radius is about 50 nm. [57]

For NP SThM, the probe is operated in the active mode where the probe is being heated while temperature of the tip is being measured. The technique also requires two temperature profiles to be obtained by scanning the SThM probe at two different heights above the sample at each position on the sample. This adds to the complexity of the technique.

2.2.2 Thermal Expansion

The thermal expansion approach to thermal measurement has the advantage that it can be operated without a dedicated sensor such as a thermocouple at the end of the sharp AFM tip. The effective spatial resolution achieved will be close to that of AFM measurement. Bimaterial Cantilever [58][59] and Scanning Joule Expansion Microscopy (SJEM) [60][62] are two such techniques utilizing the effect of thermal expansion.

In the Bimaterial Cantilever Technique, the variation of deflection of the Al-coated SiN cantilever with temperature is used. This is achieved due to a mismatch between the thermal expansion coefficients of the two materials. Therefore, the cantilever probe has to be designed to provide maximum deflection. However, the limitation lies in the requirement that most of the heat flow has to be through the probe for greatest sensitivity since the whole cantilever now acts as the temperature sensor. This technique has to be operated in vacuum as gas conduction is significant under ambient condition.

SJEM measures the local thermal expansion of an electrically heated sample, independent of the heat transfer between the tip and sample. Figure 2.8 shows a schematic of the SJEM setup [60].

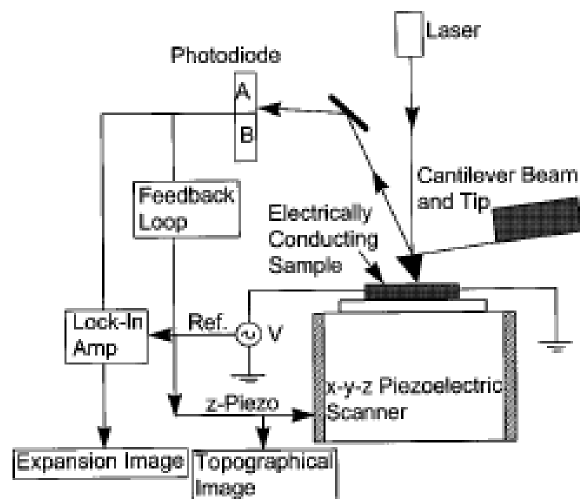


Figure 2.8: (a) Schematic setup for scanning joule expansion microscopy

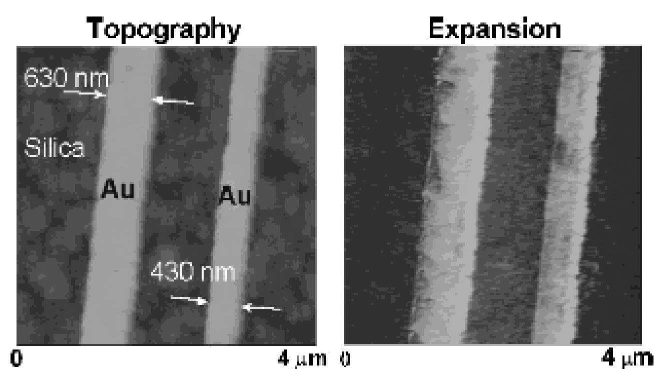


Figure 2.8: (b) Topography and thermal expansion micrographs of two 160 nm thick gold lines at current density of 5.9 MA/cm^2

A sinusoidal or pulsed voltage at a frequency different from AFM feedback is applied to the sample, which produces joule heating and a temperature rise, resulting in sample thermal expansion. The expansion signal is captured by a photodiode and is passed through a lock-in amplifier tuned to the Joule heating frequency. The main advantages are usage of a typical Si tip and avoidance of requirement for heat transfer to the scanning tip for expansion detection. This allows for spatial resolution similar to that of a typical AFM tip. Sub-100 nm spatial resolution can be easily achieved in an ambient

environment. However, this technique is applicable only to electrically conducting samples since the sample has to be heated electrically to determine the expansion signal. Further limitation is that for measurement of temperature distribution, the sample surface needs to be coated with a thin uniform layer of polymer. Otherwise, the thermal signal will be affected by different degree of expansion attributed to different material across the sample, each with their expansion factor. This requires detailed calibration to be carried out before any quantitative thermal analysis can be done.

Recently, Grosse et al. [61] reported the measurement of the temperature distribution at the contacts of working grapheme transistors with a spatial resolution of ~10 nm by SJEM. This is achieved by measuring the amplitude distribution of the steady periodic temperature field with a heating frequency of 65 kHz.

2.2.3 Electrical Resistance

The use of resistive SThM offers many potential applications for micro-thermal and micro-spectroscopic analysis [46]. Some of the applications include use in thermal impedance tomography [63], scanning thermal expansion microscopy [64] where DUT biasing is not required, and near-field photothermal infrared spectroscopy [65]. Quantitative analysis of the heat dissipation characteristics in current-carrying GaN nanowires with diameters of ~ 40-60 nm is also investigated. [66] Thermal conductivity of silicon nanowires is studied [67] and concluded that there is no significant reduction in comparison with bulk Si for nanowires with diameters ranging from 200 to 380 nm. Spatial resolution of around 100 nm is achieved.

Kar-Narayan et al. [68] even used the SThM for measuring the electrocaloric (EC) temperature change in a multilayer capacitor (MLC) based on $BaTiO_3$. EC effects are thermal changes that arise in electrically insulating materials due to changes of applied electric field. A thin Pt track deposited on the tip of an AFM functions as a resistance thermometer. Figure 2.9 shows a schematic of the measurement setup.

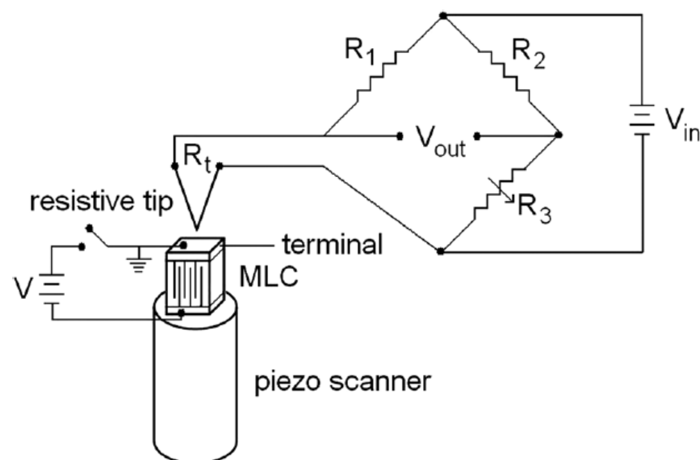


Figure 2.9: MLC and SThM schematic for EC measurement

SThM is performed with the tip approximately 5 μm above the MLC terminal, in order to avoid electrical contact, and in order to avoid destructive contact with the ~ 10 μm rough surface. The results of the measurement are shown in Fig. 2.10.

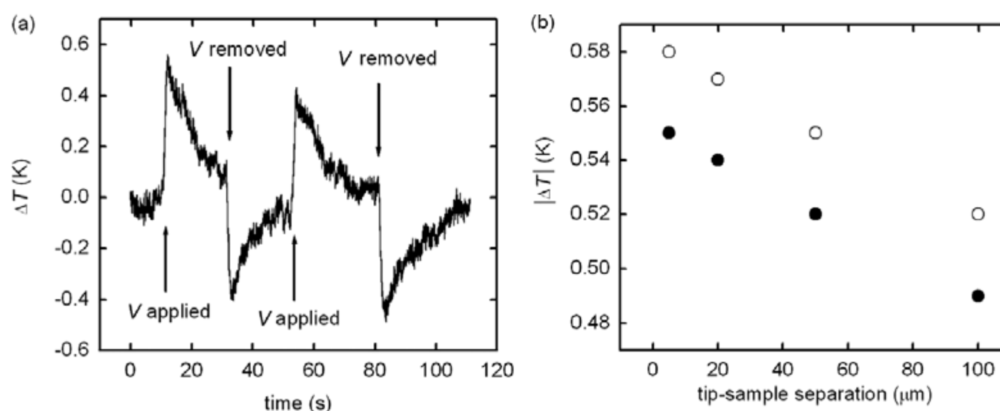


Figure 2.10: SThM measurements of EC effects in an MLC. (a) Temperature change ΔT versus time, on applying and removing V=200V as indicated. (b) EC heating (open circles) and cooling (closed circles) as a function of tip-sample separation.

Figure 2.10 (a) shows the increase in MLC temperature by about 0.58 K on application of 200 V across the MLC terminals. The EC heat subsequently dissipated over ~ 20s. Upon removal of the voltage, an EC cooling of ~ 0.55 K is observed. This leads the MLC to absorb heat from the SThM scanner over ~ 20 s duration. Increasing the tip-terminal separation to ~ 100 μm reduced the measured value of ΔT by ~ 10% as shown in Fig. 2.10 (b).

The benefit of this resistive approach to thermal measurement lies in the flexibility of the technique. It can be conducted under ambient condition in passive mode for temperature measurement or active mode for thermal conductivity measurement.

The two modes of operation for the resistive probe based thermal microscopy are shown in Fig. 2.11.

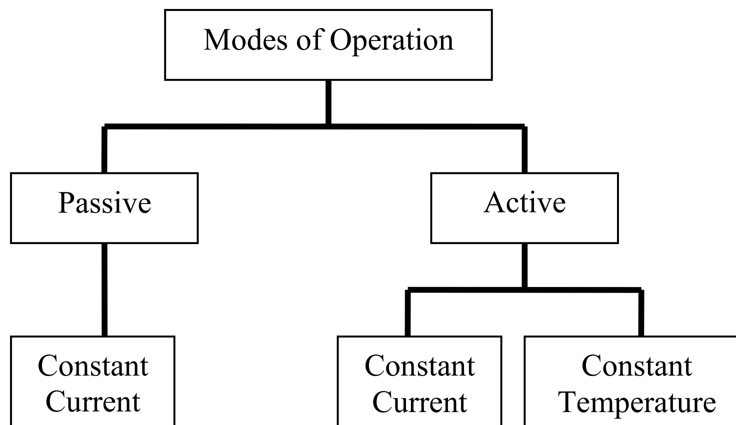


Figure 2.11: Modes of Operation for Resistive Based Scanning Thermal Microscopy (SThM)

Under both passive and active operation, any modes of biasing (dc, ac or both) can be applied. The advantage of using ac biasing allows the integration of lock-in technique to significantly improve the signal-to-noise ratio as well as the reduction of dc thermal drift.

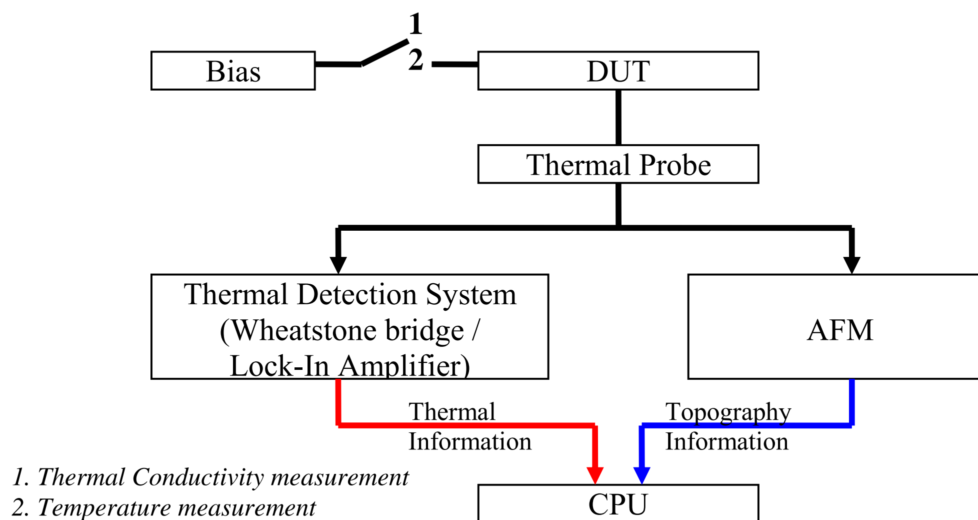


Figure 2.12: Block Diagram for Passive/Active SThM Measurements

Fig. 2.12 shows the typical components that go into the setup for thermal measurement by electrical resistance. A detailed description of the setup used in this research is provided in Chapter 4.

In passive mode, the sample is biased to generate local temperature variation. Temperature measurement is carried out by passing a small constant current through the resistive probe to induce a probe temperature that is below the DUT temperature. A high frequency current may be used to reduce the 1/f noise. Heat flows from the sample to the resistive probe during raster-scanning and changes the resistance of the probe according to Eqn. 2.1.

$$R_{probe}(T) = R_o[\alpha_{probe}(T - T_o) + 1] \qquad (2.1)$$

where $R_{probe}(T)$ is the resistance of the probe at temperature T, R_0 is the resistance of the probe at ambient temperature T_0 and α_{probe} is the coefficient of resistivity of the probe.

Since constant current passes through the resistive probe, there will be a voltage change in response to the resistance change of the probe which relates to the thermal signal. This voltage change can be further amplified by the Wheatstone bridge and lock-in amplifier components. The resistive probe thus functions as a scanning thermometer to determine the local surface temperature variation. Temperature resolution down to 5 mK has been demonstrated as estimated by noise analyses and confirmed with temperature measurement on test structures [69]. Some applications carried out with the resistive probe includes backside study of ULSI device [69], study of glass transition temperature [70] and thermal measurement of thin membrane micromachined rf power sensor [71].

In active mode, DUT thermal conductivity measurement is possible with a current passing through the probe to induce Joule heating. The direction of heat flow in this case is from the resistive tip which now acts as a heater down to the unbiased DUT. This technique makes use of the frequency dependence of the resulting temperature oscillation from the constant current carrying resistive probe to determine the local thermal conductivity. Changes in the heat flux between the resistive probe and sample is detected as changes in probe resistance.

In constant temperature configuration, the probe resistance is maintained by varying the voltage applied to the probe through a feedback loop as shown in the following figure.

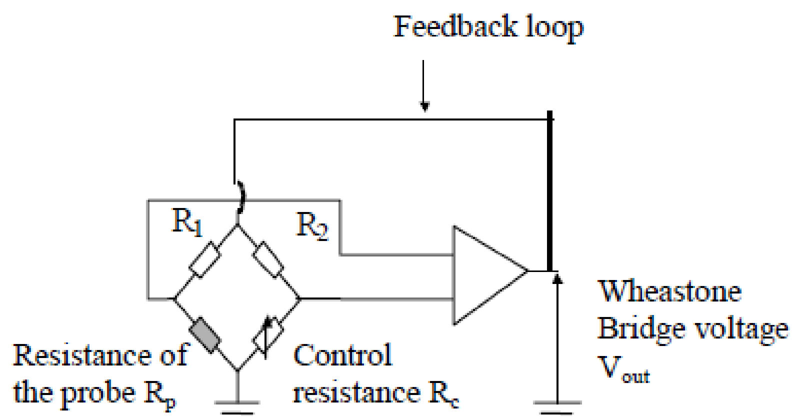


Figure 2.13: Representation of the electronic circuit of the SThM with feedback loop for constant temperature operation [72]

A similar closed loop system using electrical temperature dithering (Fig. 2.14) is implemented by Lee et al. [73] to keep the average temperature of the probe tip constant while synchronously detecting variations in the second harmonic of the modulated signal as the tip is scanned across the sample surface.

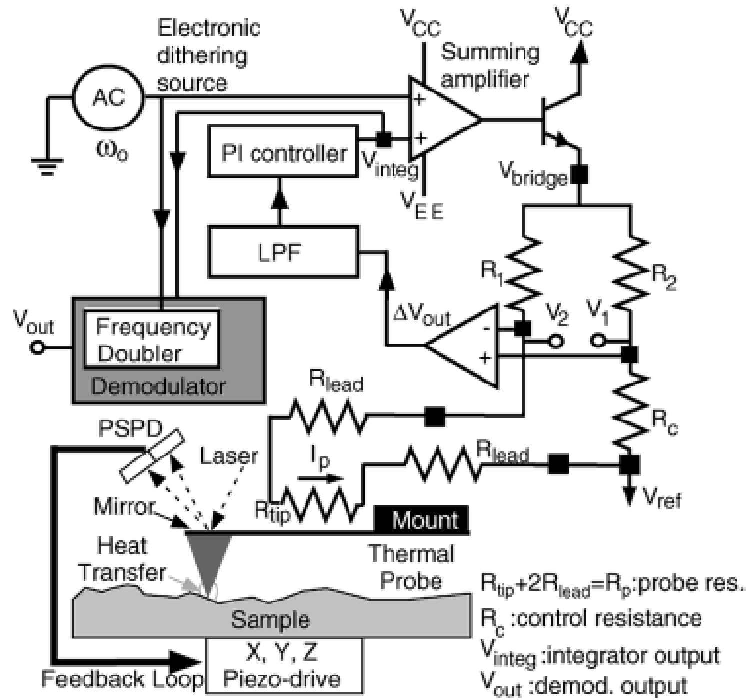


Figure 2.14: Schematic of scanning thermal microscopy equipped with a servo-controlled interface circuit using electrical temperature dithering and an ultracompliant micromachined thermal sensor

The error voltage between bridge nodes is amplified by an instrumentation amplifier and then fed into the PI controller, which provides compensation current I_p to keep the bridge balanced. Since the average probe temperature increases or decreases with the compensation power, the probe resistance R_p is adjusted by I_p until the bridge regains balance. The PI controller is realized by using an integrator, an inverting amplifier, a summing amplifier, and a current buffer. High integral gain of 1–2 $\times 10^4$ is chosen to achieve a fast response time.

The constant temperature configuration has the advantage of fast probe response time with no need for new thermal equilibrium to be satisfied. However, the constant current

configuration is preferred. This is because the constant current configuration is simpler and has a setup similar to that of the passive mode for temperature measurement without additional voltage feedback loop.

Local thermal conductivity can then be extracted based on the 3ω technique developed by Cahill [74]. Quantitative thermal conductivity of silver has been determined to be 437 $Wm^{-1}K^{-1}$ with an accuracy of 2% compared to literature value of 429 $Wm^{-1}K^{-1}$ [75]. Hinz et al. [76] also used the SThM in active mode to determine the thermal conductivity of a 3 nm thick HfO_2 film on a silicon substrate with a spatial resolution of around 25 nm. A micro fabricated silicon cantilever with sharp heatable tip is used.

2.2.4 Resistive Thermal Probes

The design of a resistive probe has a significant impact on SThM performance. Spatial and thermal resolutions of resistive-based SThM are dependent on tip sharpness, tip-sample heat transfer mechanism and thermal design of the probe [77]. Taking into consideration the thermal contact resistance at the probe sample interface where heat flows through, a thermal resistance network has been modeled by Cahill as shown in Fig. 2.15 [77].

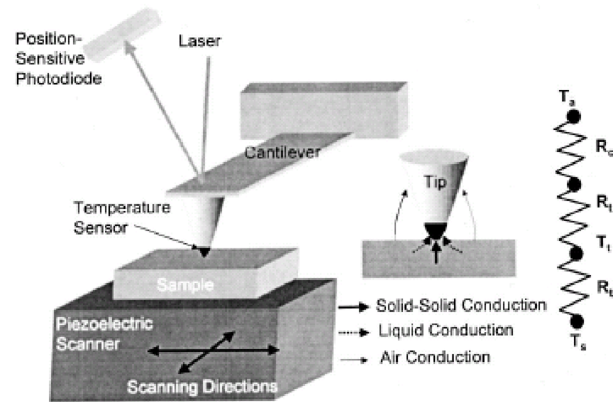


Figure 2.15: Thermal Transport of a Simple Thermal Resistance Network Model [77]

The thermal resistance network can be written as follows:

$$T_t = T_s + (T_a - T_s)/(1+\phi) \tag{2.2}$$

where T_t is tip temperature, T_s is sample temperature, T_a is ambient temperature, ϕ is $(R_c + R_t)/R_{ts}$, R_c is cantilever thermal resistance, R_t is tip resistance and R_{ts} is tip-sample resistance.

Thermal resistance due to cantilever and tip are a result of conduction through the tip and cantilever material as well as the surrounding air. As for the tip-sample resistance, it is from the total contribution of liquid, air and solid-solid conduction.

From Eqn. 2.2, the changes in sample temperature can be related to changes in tip temperature by

$$\Delta T_t / \Delta T_s = \phi/(1+\phi) \tag{2.3}$$

This relationship shows that for the tip temperature to accurately track the sample temperature, ϕ has to be large such that Eqn. 2.3 tends to 1. A large ϕ value corresponds

to a small tip-sample resistance as compared to resistance of the cantilever and the tip. Therefore, a large ϕ is essential for better SThM performance.

The spatial resolution Δx of the probe sample system is as follows:

$$\Delta x = \Delta T_n /(dT_t / dx) = \frac{\Delta T_n}{(dT_s / dx)}(\frac{1+\phi}{\phi}) \tag{2.4}$$

where ΔT_n is thermal measurement noise, dT_t / dx is the measured temperature gradient along the sample surface.

Eqn. 2.4 suggests that a large measured temperature gradient along the sample surface leads to improved spatial resolution of SThM. Meanwhile, small values of ϕ (which may be due to much larger tip-sample resistance compared to tip resistance) lead to poor spatial resolution of SThM.

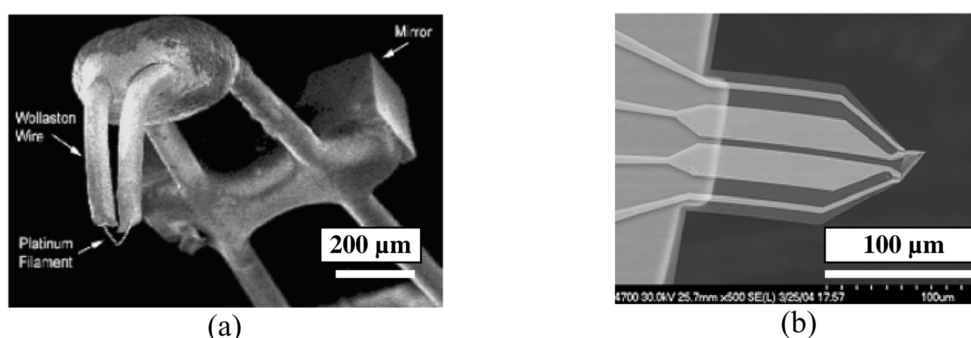


Figure 2.16: (a) Wollaston probe [46] and (b) nanofabricated thermal probe [78]

The Wollaston probe as shown in Fig. 2.16 (a) was first introduced in 1994 [79][80]. It has a thin platinum/rhodium core of 5 µm diameter. Fig. 2.16 (b) shows a nanofabricated thermal probe where the resistive element of NiCr and Pd is lithographically patterned on the AFM tip. This tip has a radius of only 100 nm, much smaller than the 2.5 µm of the

commonly used Wollaston thermal probe. It also has a comparable thermal coefficient of resistance of about 0.00123 K^{-1}.

Despite the relatively thicker Wollaston probe, it has been demonstrated to achieve spatial resolution as fine as 30 nm on a sample of GaAs-based tunnelling diode [81]. Efforts by Brown [82] to modify the Wollaston probe by mounting a micron-sized diamond pyramid on the tip revealed no obvious improvement. Therefore, achieving a good thermal resolution does not solely depend on having the sharpest probe tip with high aspect ratio. For a sharp tip, the thermal contact with the DUT may be greatly reduced. This leads to inefficient solid-solid thermal transport which is the basis on which the probe based measurement methodology functions. Altes [83] has managed to demonstrate that a Wollaston probe is able to provide a better qualitative thermal conductivity micrograph compared with a modified probe with additional tungsten carbide tip deposited at the apex. This is due to the long deposited tip negating benefits of near field condition of the line heat source created by the loop of the Wollaston probe.

The time response of the probe is another important factor to be considered when performing thermal analysis. The thermocouple is reported to have a response time of about 5 ms, which is about comparable to that of liquid crystal thermography [84]. The Wollaston resistive probe however has a much better time response. Buzin [84] has determined the time constant of the Wollaston probe to be 200 µs in air. Another study by Ezzahri [86] determined the Wollaston probe’s time constant to be about 185 µs.

Therefore, the resistive Wollaston probe with a faster response time allows for more sensitive analysis compared to the thermocouple.

Other thermal probe variants include the design of probe incorporated with a grooved cantilever structure to compensate for the bilayer thermal bending that normally occurs during SThM of hot samples [87] and a dual cantilever resistive probe [88].

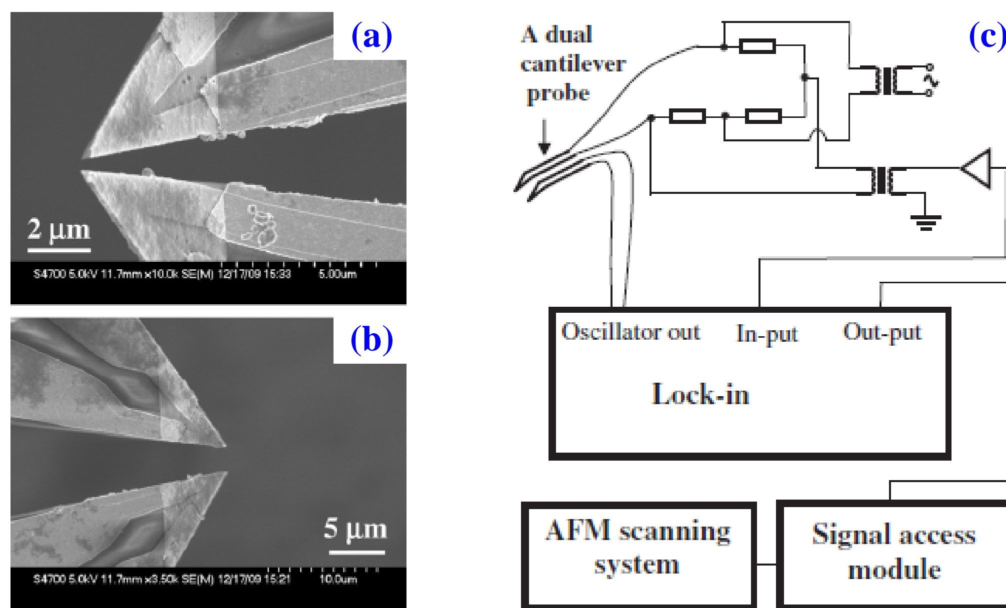


Figure 2.17: (a) SEM images of batch fabricated dual cantilever probes with tip-to-tip spacing of 300 nm and (b) 2 µm, (c) schematic of experimental setup for thermal scan with a dual cantilever resistive probe

In the dual probe (Fig. 2.17 (c)), one is used as local heater and a second one nearby detects the thermal diffusivity at a microscopic scale. Various types of dual probes have been fabricated in one batch (Fig. 2.17 (a), (b)) to allow experimental determination of the optimal sensor type for the measurement. Thermal scans with the dual cantilever probes have been performed in atmosphere, and contrast in thermal imaging indicating the difference of thermal conductivity is shown, although the contrast is weak. Test of

these probes under vacuum indicates strong thermal coupling through air between the two probes in the dual cantilever probes, resulting in weak contrast in atmosphere.

A novel four-terminal thermoresistive nanoprobe was developed by Wielgoszewski et al. [89] for performing thermal measurements in standard static-mode AFM. The setup also requires the use of a modified Wheatstone bridge as shown in Fig. 2.18.

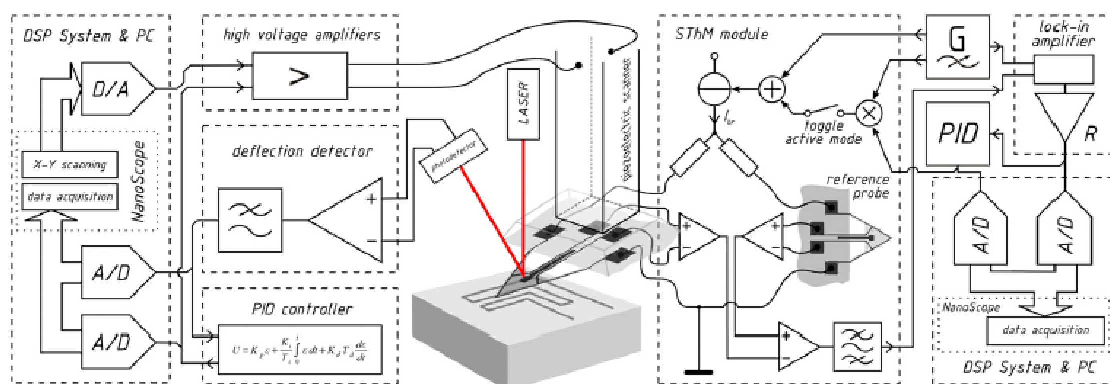


Figure 2.18: Schematic of scanning thermal microscope using a novel four-terminal thermoresistive nanoprobe with a modified Wheatstone bridge setup

The use of four-terminal thermoresistive nanoprobe makes the temperature read-out more accurate [90] as the measurement is less susceptible to parasitic heat radiation from the sample to the nanoprobe. Also, only the exact tip resistance is measured with the modified Wheatstone bridge setup, without any contribution from possible instability of other resistance components.

2.3 Double Modulation for Topography Noise Decoupling

Despite the many benefits of probe based thermal measurement technique like being able to overcome the diffraction limits which is limiting optical techniques; there is one issue that keeps surfacing. That is the problem of topography related artifacts due to the variation in effective probe thermal contact area across the DUT. This can lead to the thermal signal coupling with topography signal, resulting in erroneous thermal information. An example of such topography-related artifacts is observed by Soudi et al. [66] during the characterization of nanowires and reproduced in Fig. 2.19.

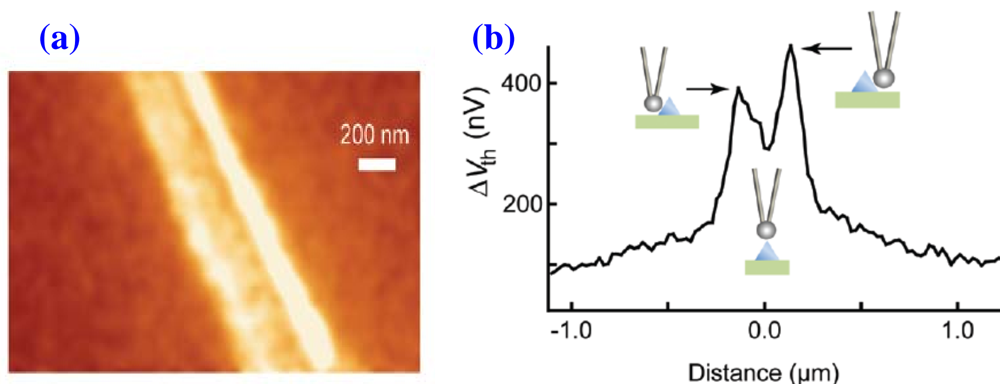


Figure 2.19: (a)SThM micrograph showing the "double-line" – like structure and (b) the corresponding profile across the nanowire

Figure 2.19 (a) shows a "double-line" like feature in the thermal micrograph with a darker region (smaller ΔV_{th}) being sandwiched between two brighter lines (larger ΔV_{th}). ΔV_{th} is the thermal signal detected using the lock-in technique. The author suggested that this is due to the triangular cross section of GaN nanowires: when the tip is on the top of the apex, the thermal coupling between the tip and the nanowire is rather poor compared to that when the tip is on one of nanowire facets, leading to a lower ΔVth (Fig. 2.19 (b)).

Furthermore, normal wear to the thermal probe may result in further variation in effective thermal contact area between measurements.

The usual averaging method for noise reduction does not help since the effective thermal contact area is unique at every point in the measurement. In this situation, it may be beneficial to introduce a modulation to the excitation signal. In this way, the controlled fluctuation of the thermal signal can be picked up against the constant topographic feature at the measurement point. Since the thermal probe is already modulated for increased signal-to-noise performance, two lock-in amplifiers have to be deployed to extract the thermal signal of interest.

The application of double modulation has been used in various fields for signal recovery. Goree [91] applied a form of double lock-in detection in a plasma diagnostics experiment. The weak coherent radio frequency signal is recovered with reduced noise and improved SNR compared to single lock-in method. Jang et al. [92][93] has also applied similar double lock-in concept for the detection of glucose concentration through the use of magnetic optical rotatory effect (MORE). The first lock-in is used to extract the proportional amplitude of the detected signal at the required frequency. The second lock-in is used to extract the slow varying ac component of the detected signal. Together, the two lock-in amplifiers managed to achieve twice the sensitivity compared to a single MORE setup. Aoki et al. [94][95] has also managed to adapt the double lock-in technique for the study of photoluminescence in amorphous semiconductors. Due to the strong electromagnetic interference between the rf lock-in amplifier and the electro-optic

modulator (EOM) driver at high frequency, the author introduced an optical chopper. In this way, the photoluminescence signal can be decoupled from the interference by a 2nd lock-in detection at the chopper frequency. As a result, photoluminescence lifetime distribution spanning almost 11 decades from 2 ns to 160 s was measured. In another application, Kwang et al. [96] successfully employed the double lock-in system in a Brillouin optical correlation domain analysis system to enlarge the measurement range while improving the noise figure.

A variant of the double modulation, double lock-in methodology can be applied to SThM. Successful integration will help to mitigate the inherent issue of topography coupling into thermal signal captured due to changing effective thermal probe – sample contact area.

Chapter 3: Wheatstone Bridge

The Wheatstone Bridge [97][98] is the key component in getting relevant thermal data such as temperature or thermal conductivity from the sample by measuring the change in probe resistance. Charles Wheatstone was one of the first scientists to understand and make practical use of Ohm's law [99]. He described in his lecture the use of "differential resistance measurer" which is the present day DC Wheatstone bridge. This is essentially an electrical circuit which is first put into the null position before the resistance change in one arm is determined from the corresponding voltage output.

The effectiveness of the null method of measurement has resulted in variations of the Wheatstone bridge to measure impedance, capacitance and inductance. The benefit of measuring the unknown parameter such as resistance, allows for correlation (and thus measurement) with physical phenomena such as force (strain gauge measurement) and temperature (thermal measurement). Another advantage of using the bridge circuit to measure resistance is that the voltage level of the power source is of secondary importance. A greater supply voltage may increase measurement precision as it is easier to detect imbalance in the circuit. However, unlike other types of resistance measurement schemes, there is no fundamental error introduced as a result of lesser or greater power supply voltage.

3.1 Various Configurations of Wheatstone Bridge

There are various configurations of bridges available for determining the unknown parameter. In the case of Maxwell bridge (Fig. 3.1), it is used to measure the unknown inductance in terms of calibrated resistance and capacitance.

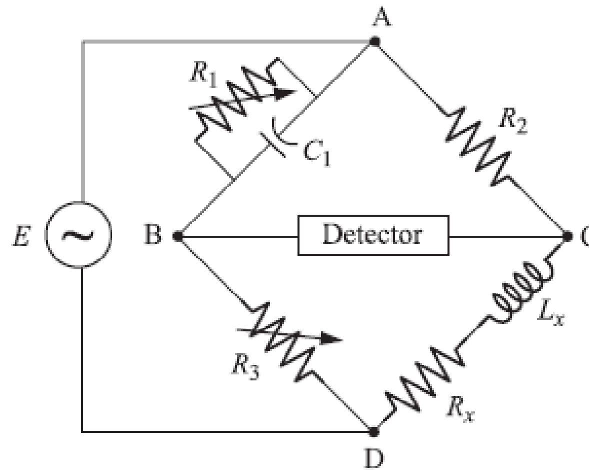


Figure 3.1: Schematic of Maxwell bridge for inductance measurements

The positive phase angle of unknown inductive impedance can be compensated by the negative phase angle of capacitive impedance when put in the opposite arm, and the circuit is balanced. This means there is no potential difference across the detector and hence, no current flows through it. The unknown inductance then becomes known in terms of this capacitance. The balanced equations are also independent of frequency.

Another advantage of using the Maxwell bridge to measure inductance rather than a left-right symmetrical inductance bridge is the elimination of measurement error due to mutual inductance between two inductors. It can be difficult to shield magnetic fields and a small amount of coupling between coils in a bridge can introduce substantial errors. Without a second inductor in the Maxwell bridge, the problem is eliminated.

To avoid the difficulties associated with determining the precise value of a variable capacitance, sometimes a fixed-value capacitor is installed and more than one resistor is made variable. The capacitive reactance in the bridge exactly opposes the inductive reactance of the load when the bridge is balanced, allowing the load's resistance and reactance to be determined. Maxwell bridge is used where either the mutual inductance between the load and the know bridge components, or stray electromagnetic interference, distorts the measurement results.

Kelvin Double bridge is a variant of the Wheatstone bridge used for measuring very low resistance, R_x. Figure 3.2 shows a schematic of the Kelvin bridge. [100]

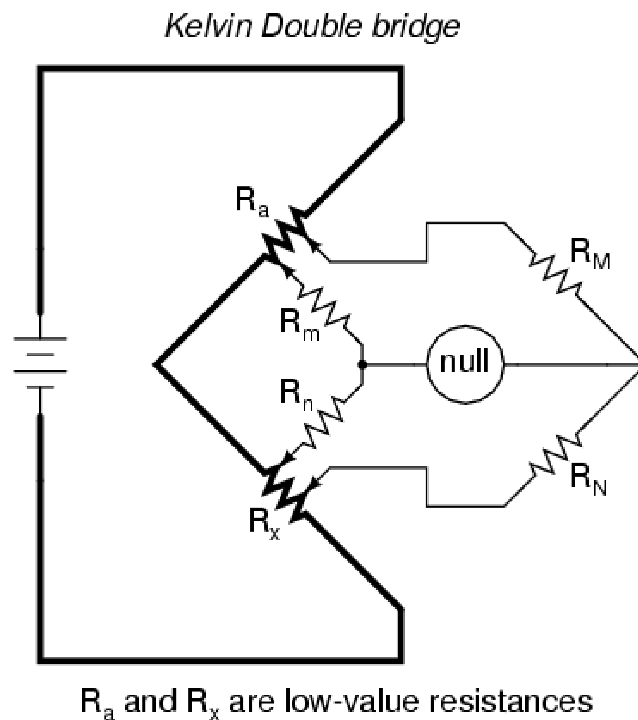


Figure 3.2: Schematic of a Kelvin Double bridge

The low value resistors (R_a and R_x) are represented by thick-line symbols and the wires connecting them to the voltage source are similarly drawn thicker in the schematic. By making the left half of the null detector more resistive than the thicker wire connecting between R_a and R_x, stray voltage drops within the null detector bridge circuit is minimized. To determine R_x, the resistance arm ratio R_m/R_n is set equal to ratio R_M/R_N. Rheostat arm resistor R_a is then adjusted until the null detector indicates balance, and R_x can then be determined by the following equation:

$$R_x = R_a (R_N/R_M) \tag{3.1}$$

Another type of circuit is the Fontana bridge. [101] This is implemented as a wide frequency band voltage-to-current converter used for making electromechanical transducers.

3.1.1 Current vs Voltage Sources

Wheatstone bridge may be driven by constant voltage or current sources. Current drive, although not as popular as voltage drive, has an advantage because the wiring resistance does not introduce errors in the measurement. Moreover, large excitation voltages can result in higher power dissipation, causing possible sensor resistor self-heating errors. On the other hand, low excitation voltage requires more gain to increase the sensitivity to noise.

Typically, constant-voltage excitation is used for strain and pressure sensors, while constant current excitation is used to excite resistive sensors such as RTDs or thermistors. Current excitation is generally preferable due to its better noise immunity.

3.1.2 D.C. vs A.C. Excitation

As highlighted in section 3.1, bridges can have d.c. or a.c. excitation. The advantage of using d.c. excitation source includes easy implementation and low cost. However, d.c. excitation has inherent difficulty of separating the actual signal from unwanted d.c. errors due to offsets and parasitic induced thermocouple effects. Uncontrolled d.c. offset variation may be due to temperature drift and both thermal and 1/f noise sources. On the other hand, although a.c. excitation is more difficult to implement, there are many benefits. A.C. excitation is able to remove offset errors, average out 1/f noise and eliminate effects due to parasitic thermocouples. With better immunity to 1/f noise, lower excitation may be used, thus reducing the self heating effects of current flow in resistive sensors. Operating in a narrow bandwidth under a.c. excitation, the system is also more resistant to rf interference than d.c. excitation.

3.2 Wheatstone Bridge for Thermal Detection

The bridge system adopted in this work is a symmetrical a.c. bridge with constant current source working on the principle of magnifying the potential drop over small change in resistance (due to a change in temperature or thermal conductivity) in the measurement arm. The sensitivity depends on proper shielding and noise reduction measures incorporated into the system. The schematic in Figure 3.3 shows the integration of the

Wheatstone Bridge with the Lock-In Amplifier (LIA) to obtain a high signal-to-noise ratio.

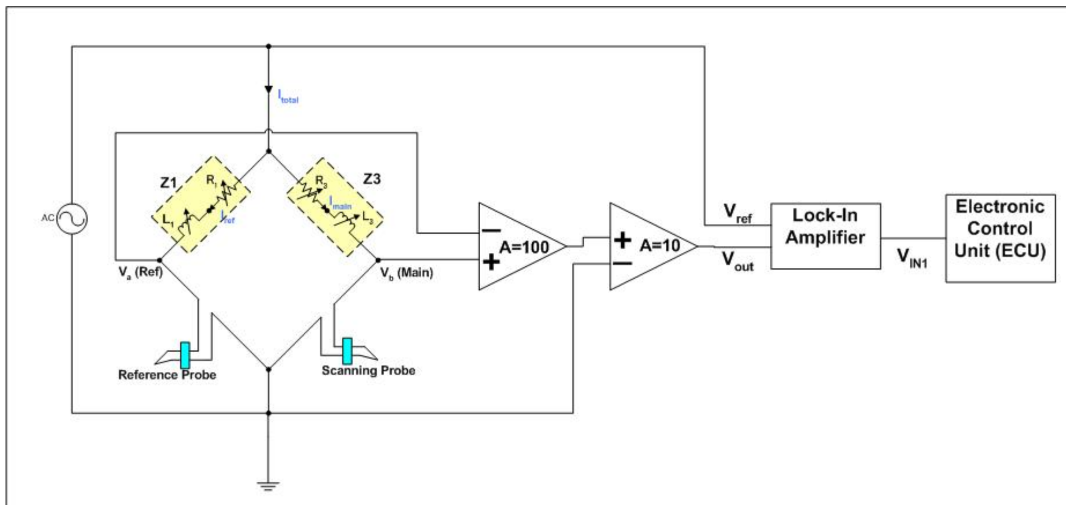


Figure 3.3: Schematic of SThM Setup (Wheatstone Bridge, LIA, ECU)

The use of the reference probe allows for compensation due to minor changes in the environmental conditions while the output of the Bridge is amplified 1000 times through the use of instrumentation amplifiers. This large magnification is necessary because only small voltage change is involved. The instrumentation amplifier provides the circuit with better gain accuracy and does not unbalance the bridge. Excellent common mode rejection can also be achieved. Voltage change is due to resistance change in the scanning probe which is a consequence of the thermal interaction with the sample. With proper shielding, the Wheatstone Bridge arrangement together with the use of appropriate operational amplifiers is able to provide the SLIA SThM with a sensitivity of 5 mK and a spatial resolution of 30 nm.

3.2.1 A.C. Bridge Theory and Balancing

A simplified diagram of the Wheatstone Bridge layout where the thermal probes are replaced by their electrical equivalent of a resistor and inductor in series is shown in Figure 3.4.

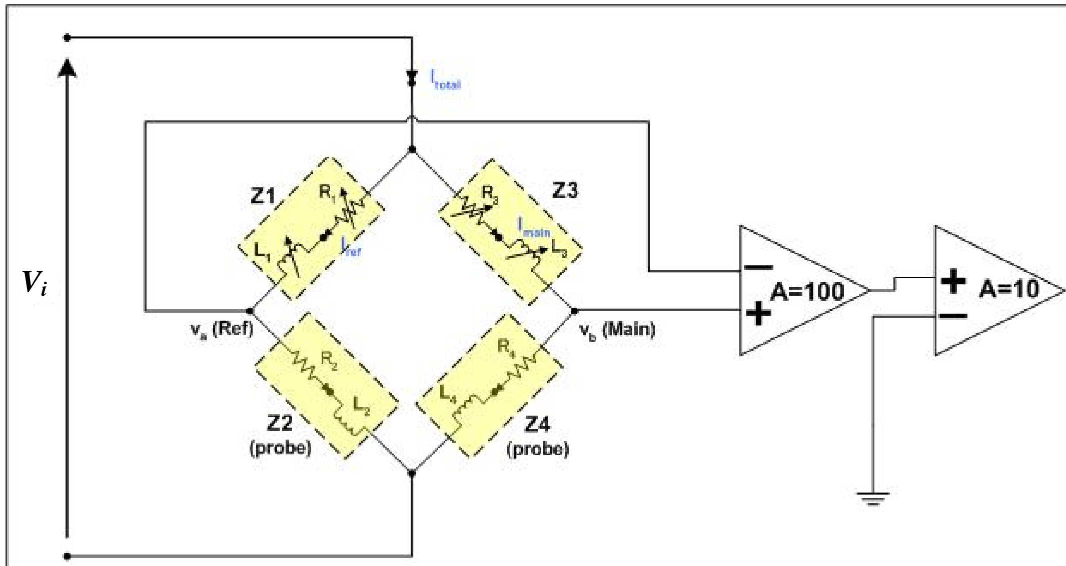


Figure 3.4: Schematic of the Wheatstone Bridge with Integrated Operational Amplifier

For a balanced Wheatstone Bridge, the output voltage, $V_b - V_a = 0$, therefore

$$\frac{Z_1}{Z_2} = \frac{Z_3}{Z_4} \tag{3.2}$$

Since this is an a.c. bridge, there are two balanced conditions, the amplitude and the phase. This ensures the balancing of the in-phase and out-of-phase components of the signal.

Expanding Equation (3.2),

$$\frac{R_1 + j\omega L_1}{R_2 + j\omega L_2} = \frac{R_3 + j\omega L_3}{R_4 + j\omega L_4}$$

$$[(R_1R_4 - R_2R_3) + \omega^2(L_2L_3 - L_1L_4)] + j\omega(R_1L_4 + R_4L_1 - R_2L_3 - R_3L_2) = 0 \quad (3.3)$$

As both thermal probes are of similar impedance, the variable resistors and inductors on both sides of the upper arms are adjusted to their mid-point before the thermal probe is landed on the DUT. Upon landing, there is an offset of the Wheatstone Bridge voltage output due to resistance change of the thermal probe.

The bridge is brought to the null position through a series of iterative balancing steps. Firstly, the bridge is balanced by the tuning of the variable resistors with the signal generator set to a low frequency of about 1 Hz. At low frequency, the inductance is nearly 0. Then the signal generator is set to the desired frequency of operation where the bridge is balanced by tuning the variable inductors. These two steps are repeated until the best possible null position is achieved. Thermal measurement can then be proceeded to achieve the possible full range of experimental output without overloading the amplifiers.

3.2.2 Linearity

The linearity of the Wheatstone Bridge relates to how the output voltage of the Wheatstone Bridge varies linearly with the change in the resistance of the resistive probe Z_4 as a function of temperature change. The output voltage v_0 of the Wheatstone Bridge is given by:

$$v_0 = v_b - v_a = v_i\left(\frac{R_4 + j\omega L_4}{R_3 + R_4 + j\omega(L_3 + L_4)} - \frac{R_2 + j\omega L_2}{R_1 + R_2 + j\omega(L_1 + L_2)}\right) \quad (3.4)$$

where v_i is the input voltage and ω is the voltage excitation frequency.

The change in output voltage due to a resistance change of the scanning resistive probe $\Delta R_4(T)$ as a result of variation in local thermal properties, is then given by

$$\Delta v_0 = v_i \frac{(R_3 + j\omega L_3)\Delta R_4(T)}{\{[R_3 + R_4 + \Delta R_4(T)] + j\omega[L_3 + L_4]\}\{[R_3 + R_4] + j\omega[L_3 + L_4]\}} \tag{3.5}$$

where Δv_0 is the change in output voltage and $\Delta R_4(T)$ is the resistance change of the resistive probe.

Since $\Delta R_4(T) << (R_3+R_4)$, Eqn. 3.5 can be simplified as follows:

$$\Delta v_0 \approx \frac{v_i(R_3 + j\omega L_3)}{[(R_3 + R_4) + j\omega(L_3 + L_4)]^2}\Delta R_4(T) \tag{3.6}$$

Eqn. 3.6 shows that the change in output voltage of the Wheatstone Bridge Δv_0 is linearly proportional to resistance change of the resistive probe $\Delta R_4(T)$. Furthermore, since the change in probe resistance varies linearly with temperature, a linear correlation of temperature change with Wheatstone Bridge output can be established, allowing for easy temperature calibration.

3.2.3 Sensitivity

An important parameter for Wheatstone Bridge characterization is the sensitivity of the Wheatstone Bridge (without any operational amplifiers). This Wheatstone Bridge sensitivity K_R is defined as the change in Wheatstone Bridge voltage output, Δv_o per unit change in scanning probe resistance, $\Delta R_4(T)$.

Assuming purely resistive elements with constant current flowing through each resistive probe in the Wheatstone Bridge, the sensitivity K_R can be expressed as:

$$K_R = I_1 \frac{R_3}{R_3 + R_4(T)} = I_1 \frac{p}{p+1} \tag{3.7}$$

where I_1 $(= I_{main} = I_{ref})$ is the constant current flowing through the resistive probe, $R_4(T)$ is resistance of the temperature sensitive resistive probe and p is the arm ratio $(R_3/R_4(T))$ of the Wheatstone Bridge.

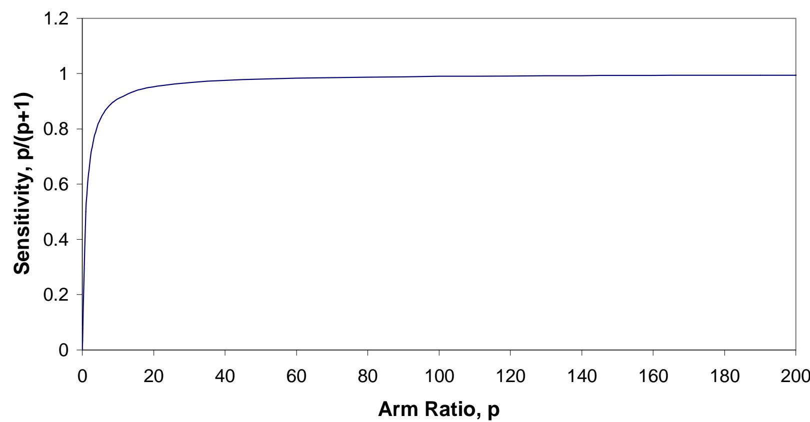


Figure 3.5: A Plot of Sensitivity against Arm Ratio

Figure 3.5 shows the Wheatstone Bridge sensitivity for different value of arm ratio. It can be observed that the sensitivity of the Wheatstone Bridge asymptotically tends to 1 for increasing arm ratio, p. The sensitivity reaches 0.98 at an arm ratio of 50. For this project,

an arm ratio of 50 is chosen. An arm ratio larger than 50 is not selected mainly due to two reasons. Firstly, it does not provide any significant improvement to overall sensitivity. Secondly, a much larger voltage source has to be supplied in order to provide the necessary current for thermal measurement.

Considering the use of variable inductance in an ac Wheatstone Bridge, similar analysis shows that in order to achieve arm ratio p $\geqslant$ 50, there is an additional requirement that

$$\frac{L_3}{L_4} \geq 50.$$

3.2.4 Stability

Wiring resistance and noise pickup are among the biggest problems associated with sensor based application. Great effort and instrumentation considerations have been expended to eventually arrive at the final bridge configuration as described in section 3.2.

There are few key areas to take note in the design and handling of the Wheatstone bridge in order for optimum performance. One consideration is the proper shielding of the Wheatstone bridge. It is necessary that all possible noise sources are eliminated or minimized since the bridge is working with low signal level in the mv range. Therefore, all connections between the bridge and the various instruments should make use of co-axial cables so as to prevent any pickup of electrical noise from the environment. The variable inductors should also be properly shielded by housing in a metal fixture as shown in Fig. 3.6.

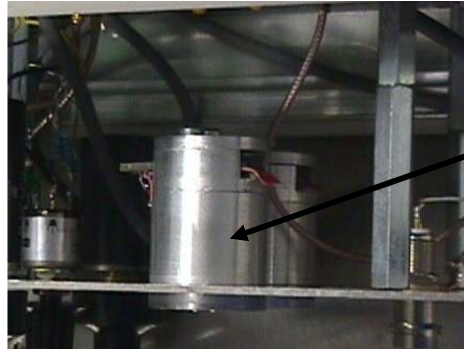


Figure 3.6: Metal housing for the variable inductor

Furthermore, an insulating material should be used for adjusting the variable inductors while the use of metal piece such as screw driver should be avoided so as to achieve an actual inductance value during balancing of the bridge. The Wheatstone bridge is also housed in an aluminium casing which is grounded to provide additional shield for the circuit within.

There should be no dry joints within the bridge circuit, especially at the input of the first instrumentation amplifier where any noise introduced can be magnified 1000 times by subsequent amplifier. The pins of the thermal probe should also be soldered to the co-axial cable to minimize any noise due to loose connections rather than using commercial connectors to secure the thermal probes to the bridge setup. This ensures good thermal contact and reduces thermocouple effect during operation. Furthermore, the thermal probe degrades over time and should be changed, as it impacts the ability of the bridge to be stabilized after null condition is set.

Care should also be exercised when handling the Printed Circuit Board (PCB). The pins of the instrumentation and operational amplifiers are very sensitive and can be easily affected by ESD if handled with bare hands.

Also, the choice of the frequency used and its harmonics should not be close to the power line frequency and its harmonic so as to minimize noise pickup from the power supply which inadvertently affects the measurement. Noting that the mains frequency can range from 48 Hz to 52 Hz [102], these frequencies and its respective harmonics should be avoided during the selection of frequency for measurement.

Finally, it is necessary to ensure that the experimental setup does not come into contact with the sunlight (close the blinds) which can definitely affect the thermal measurement. Furthermore, ventilation fans of the various instruments should not face the thermal probes as it affects the air circulation and introduces additional convectional current interferences to the thermal measurements. It was also observed that the offset in the balanced bridge started to increase when the air conditioner in the experiment room was turned on.

Taking into account the above considerations, the eventual balanced Wheatstone bridge is able to stabilize after a settling time of approximately 20 min as shown in Fig. 3.7.

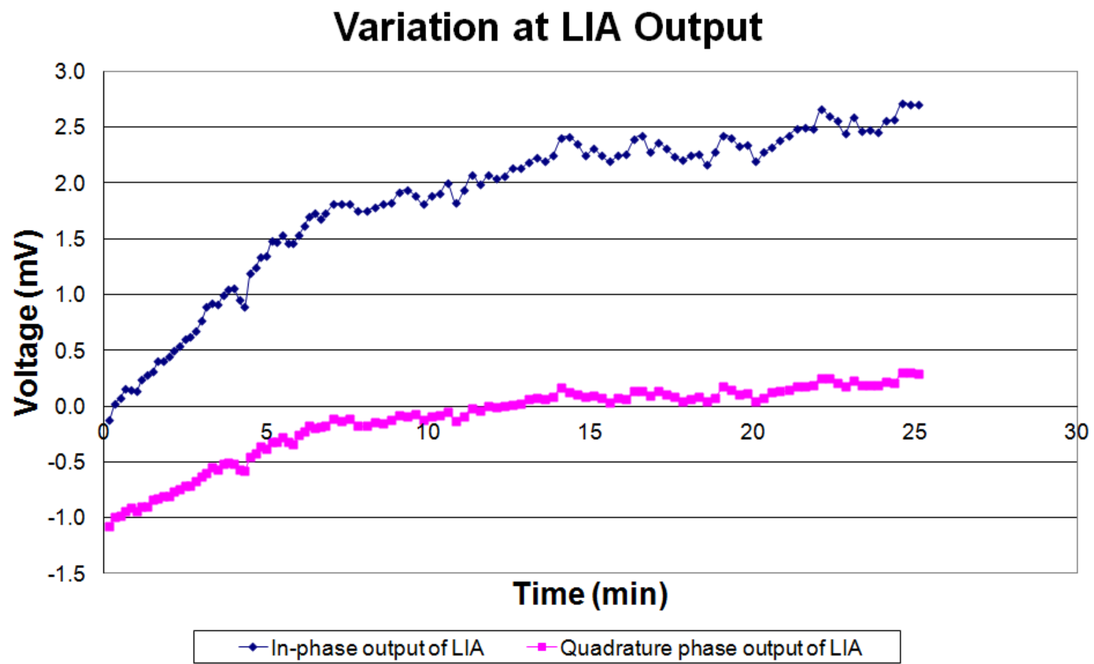


Figure 3.7: Behaviour of Wheatstone bridge output variation to reach the balanced condition

Chapter 4: SLIA SThM Setup and Configuration

This chapter first provides a description of the components that are essential for the thermal characterization work with the single lock-in amplifier (SLIA) SThM system. The PID feedback system is investigated in order to develop a systematic approach to achieve optimal thermal contact between probe and sample. The passive temperature measurement configuration and calibration methodology are discussed to calibrate the thermal probe for temperature measurement. This is followed by a discussion of the active mode where qualitative thermal conductivity measurement is achieved using the 3ω method. The proper setup of the experiment to achieve a parallel scanning plane with respect to the DUT, essential for optimized thermal measurement, is also discussed.

4.1 SThM Experimental Setup

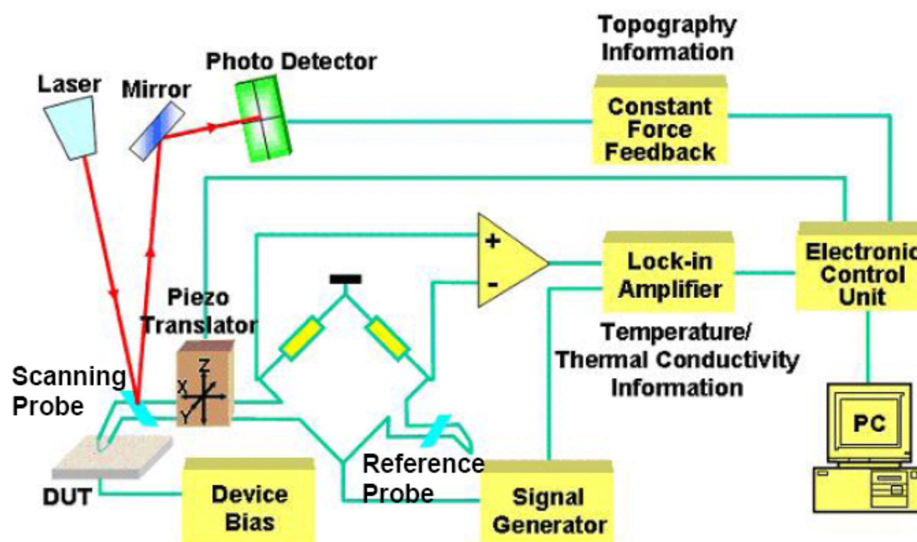


Figure 4.1: Schematic Setup for Passive/Active SThM Measurements

The SThM setup for this project is shown in Fig. 4.1. The key components include an Atomic Force Microscope (AFM), a Wheatstone Bridge, a Lock In Amplifier (LIA) and a function generator.

4.1.1 Scanning Probe Microscope (SPM)

The TopoMetrix Explorer Scanning Probe Microscope (SPM) is chosen due to its portability and flexibility to be used under ambient conditions. It has a maximum scan area of 100 µm by 100 µm with a height range of up to 10 µm. In this work, the contact Scanning Force Microscope (SFM) mode is used. One of the main advantages of the contact mode is its ability to image non-conductive samples as compared to the Scanning Tunneling Microscope (STM) which requires a conducting surface. Thus samples with passivation layer can still be studied without the need for a conductive coating. Coating the surface with a conducting layer may result in a change in the thermal distribution of the DUT.

4.1.2 Optical Topography Detection System

The topography detection system is based on optical means using the laser-mirror-photodetector system. In the contact-mode, as the probe tip scans across the sample surface, varying topographic features cause the cantilever to deflect to different extent. This results in the laser reflecting off the mirror on the probe tip to shift. This minute deflection of the laser position (caused by changes in the topographic features) is magnified by another mirror in the AFM system before striking the four-section photodetector. In this way, the angular deflection of the cantilever, and thus the

topography, can be calculated from the difference in the laser position on the photodetector. The overall system has a vertical sensitivity of 10 Å.

4.1.3 Resistive Thermal Probe

The resistive thermal probe (from VEECO Metrology Group) used is a Wollaston wire containing a 5 µm diameter platinum-rhodium core surrounded by a 75 µm diameter silver cladding as shown in Fig. 4.2.

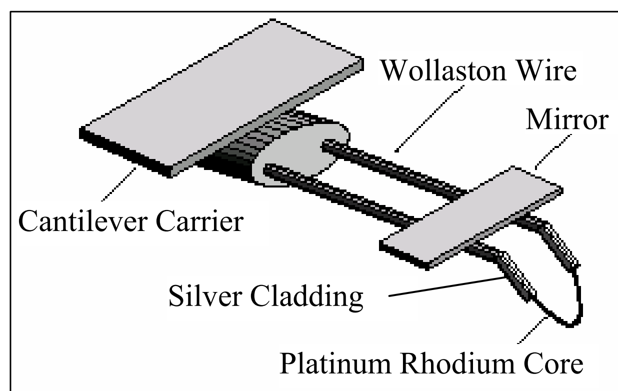


Figure 4.2: Schematic of Resistive Wollaston Wire Probe

The thermal probe consists of a mirror for reflecting the laser beam from the AFM to facilitate the capturing of topographic information. The probe serves both as a heat source (for thermal conductivity measurement) as well as a temperature sensor (for temperature measurement) in the SThM. The Wollaston wire is etched at the loop region to expose a platinum-rhodium core with a length of about 200 µm. The material properties of the Silver, Platinum and Platinum/Rhodium used in the thermal probe are as shown in Table 4.1.

Table 4.1: Material Properties of Thermal Probe [103]

	Specific Heat Capacity, C_p ($kJ \cdot kg^{-1} \cdot K^{-1}$)	Thermal Conductivity, κ ($W \cdot m^{-1} \cdot K^{-1}$)
Silver, Ag	0.235	429
Platinum, Pt	0.133	71.6
Platinum/Rhodium (Pt90/Rh10)	0.13 - 0.24	38

The thick silver cladding provides mechanical support for the thermal probe during scanning while the high thermal conductivity of silver allows heat to be conducted efficiently away from the thermal probe to the thermal detection system (Wheatstone Bridge). The exposed platinum-rhodium core with a very low specific heat capacity makes it an ideal material to be sensitive to thermal variation across the DUT being probed. The Rhodium in the alloy provides the probe with the mechanical strength and improves the overall corrosion resistance.

The effective contact radius can be as small as 30 nm on a relatively flat sample despite the core having a thickness of 5 μm [104]. All the probes available have a resistance of about 2.5 Ω ± 4% and inductance value of 1.85 μH ± 5%. Care has to be exercised when handling the probes as they can be bent easily, thus affecting thermal measurement. Besides, a current of not more than 20 mA is allowed to pass through the probes.

4.1.4 Lock-In Amplifier (LIA)

Lock-in detection methodology has been extensively applied in various industries and scientific research to improve detection sensitivity. It enhances signal to noise measurement by using bandwidth narrowing to reduce broadband noise in order to recover the embedded weak signal [105][106][107].

The use of LIA allows for the extraction of signals at the frequency of interest from the output of the Wheatstone bridge which is discussed in chapter 3. It also allows for the filtering of unwanted noise signals at other frequencies and harmonics, such as those generated by the power lines at 50 Hz, which would otherwise interfere with the measurement. The technique employed in LIA is based on phase sensitive detection [106]. Another advantage of LIA is its ability to lock in to harmonics of the reference frequency which is useful for various measurement techniques such as the 3ω technique for thermal conductivity measurement. A more detailed treatment of the signals from the LIA is discussed in subsequent chapter 7 using the double lock-in scheme. The output signal of the LIA, *CH1* feeding into the Electronic Control Unit (ECU) is related to the output of the Wheatstone Bridge, V_{out} by Equation (4.1). The objective is to use the smallest sensitivity available while ensuring the full range of V_{out} does not overload *CH1* beyond 10 V.

$$CH1 = \frac{V_{out}}{sensitivity} \times (2.5) \tag{4.1}$$

where *sensitivity* is the sensitivity of the LIA and must be $\geq \frac{1}{3} V_{out}$. This ensures enough margins for variation in thermal measurement over the course of the experiment without overloading the ECU while using the full sensitivity allowable by the LIA.

4.2 PID Feedback System

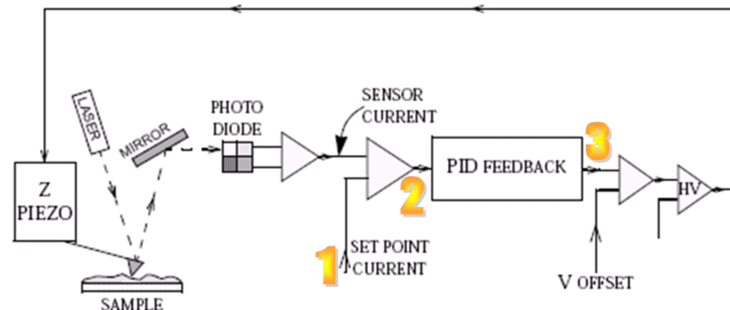


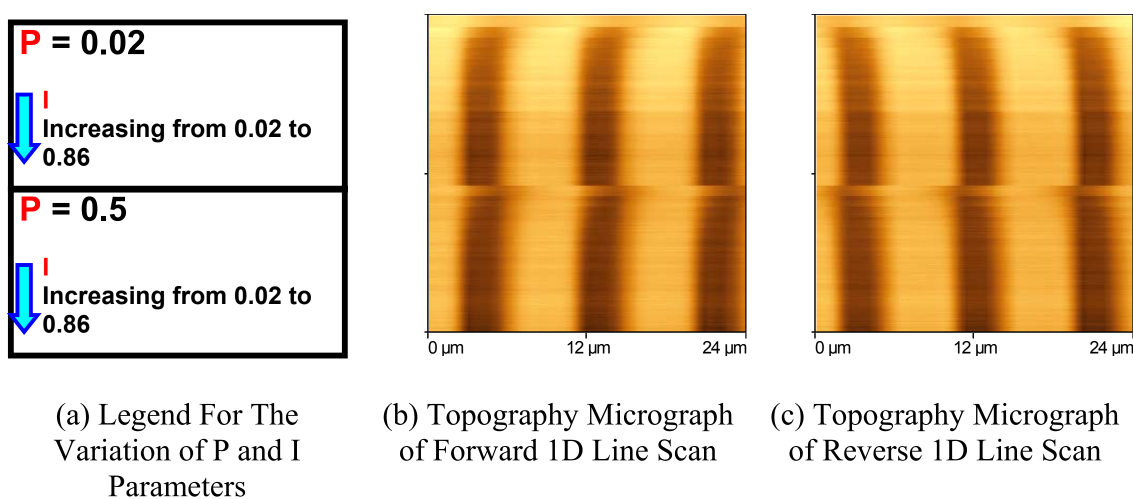
Figure 4.3: Closed-Loop PID Feedback in AFM [108]

The closed-loop PID feedback used in the AFM system is shown in Fig. 4.3. An initial set point current value is used. The error signal, the difference between set point and sensor current, is fed into the PID feedback which outputs a signal to adjust the Z-piezo to the appropriate height.

There is currently no systematic way of getting the optimal setting from the AFM PID feedback system from a survey of the literature. Only general guides are available with the consensus that a suitable setting is arrived at instinctively and through experienced use with the AFM system. In order to achieve a consistent measurement with the AFM system, a systematic procedure of achieving the optimized feedback parameters for each probe-sample configuration is preferred. In the proposed methodology, a series of 1-directional (1D) line scans is performed at various PID setting to generate a contour plot where the optimized PID setting is determined. From the result, an insight into how the parameters interact to give the optimized topography micrograph can be understood. A

strategy to achieve optimized result is then developed and applied to different samples used.

In the proposed methodology, a standard calibration grid is used with the resistive probe to determine the optimal PID parameter for this resistive probe-calibration grid system. The variables that need to be taken into consideration are thermal probe scan speed, PID parameters and sample used. The choice of using calibration grid is because its material properties and topography are well documented. The experiment is conducted by carrying out 1D line scan of the calibration grid with known feature dimension while keeping one of the PID parameters constant and varying the other two. Both forward and reverse line scan are performed. Figure 4.4 shows an example of topography micrographs obtained by keeping parameter D constant and varying both the P and I parameters with a line scan rate of 24 μm/s. D is kept constant as it does not have as much effect on acquired micrograph as compared to P and I.



(a) Legend For The Variation of P and I Parameters

(b) Topography Micrograph of Forward 1D Line Scan

(c) Topography Micrograph of Reverse 1D Line Scan

Figure 4.4: Topography Micrographs of 1D Line Scan

At a line scan rate of 24 μm/s, it can be observed that a low value for parameter I results in delayed response of the topography information. This is shown in Fig. 4.4 (b) where

the feature appears drifted to the right in the direction of forward line scan at low value of I. Similarly in Fig. 4.4 (c), the feature appears drifted to the left in the direction of reverse line scan.

From a collection of the various line scan done with different PID parameters on the line, space and height feature of the calibration grid, contour maps are generated to determine the parameters that are able to achieve these known features.

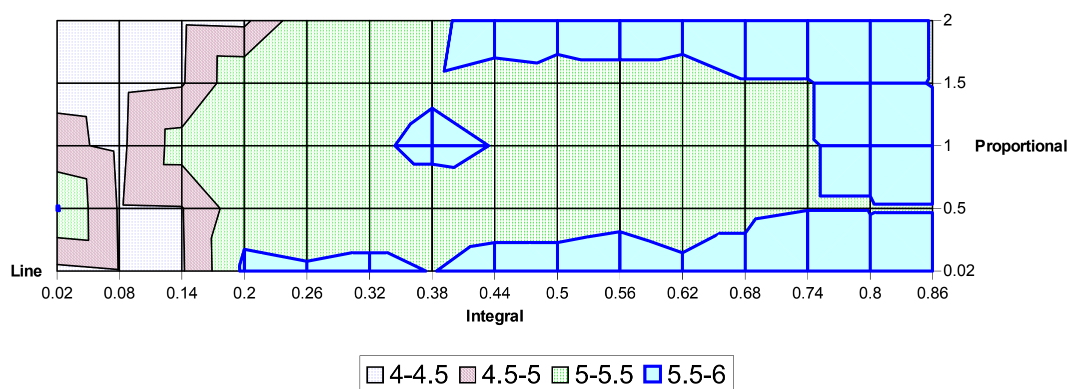


Figure 4.5: Proportional and Integral Optimization for a Line Feature

Figure 4.5 shows an example of such a contour map for a line feature of 6.2 µm. The optimal P and I parameters are determined when the measured line feature is within 10% of the stated value in the calibration grid data sheet.

An analysis of results obtained leads to the following conclusion:

i. Accurate height profile is achieved without much adjustment of the PID parameters

ii. The choice of Proportional (P) parameter does not seem to affect the acquisition of accurate Line/Space features provided an appropriate Integral (I) gain is chosen

iii. Optimized parameters (scan speed and PID) are selected when

a. Forward and reverse topography line scan matches without any drift in the direction of scan

b. The system is able to capture sharp features with high aspect ratio

c. The captured topography is not significantly reduced from known measurement

Most importantly, the results show that when the forward and reverse topography line traces coincide, the parameters used can be assumed to be optimized for the selected probe-sample setup. Keeping this information in mind, optimal PID setting for every probe-sample combination can be confidently achieved so that the corresponding thermal measurement simultaneously obtained is accurate and repeatable.

4.3 SLIA Temperature Measurement (Quantitative)

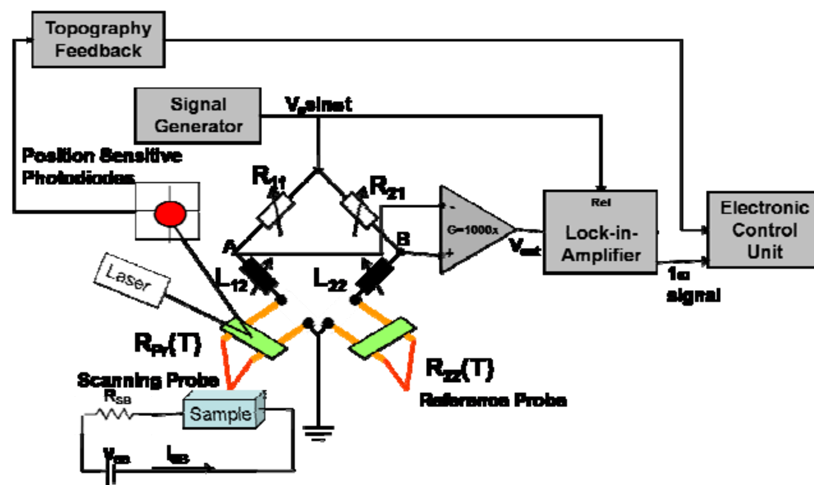


Figure 4.6: Schematic setup for SLIA temperature measurement

Figure 4.6 shows the setup for SLIA temperature measurement. A small a.c. current of frequency 98.7 kHz and amplitude of 3.2 mA is supplied to the bridge. The Wheatstone bridge is first balanced by adjusting the variable resistors and variable inductors. This is

to reduce the influence of the stray impedances, and to improve the sensitivity of the bridge. The current passing through the probe can be as low as 1.6 mA to minimize self-heating of the tip.

When the DUT is biased, the increase in device surface temperature results in heat transfer to the probe tip. The temperature of the tip increases, resulting in a linear increase of the probe resistance R. The voltage drop across the probe is increased and this voltage change is amplified 1000 times by the low noise differential amplifiers. The output of the amplifiers is measured by the lock-in amplifier at the bridge current reference frequency to improve the signal to noise ratio. The resistive component of the output of the lock-in amplifier is connected to the ECU of the AFM, which forms the thermal image with the voltage signal. The calibration of the voltage signal to the actual sample surface temperature is discussed in section 4.3.1.

4.3.1 SLIA Temperature Calibration

Temperature calibration is required before any quantitative thermal measurement can be conducted. In this section, the conversion from voltage scale as acquired from the thermal measurement system into temperature scale is discussed.

Previously, various temperature calibration schemes were carried out as shown in the schematics in Fig. 4.7.

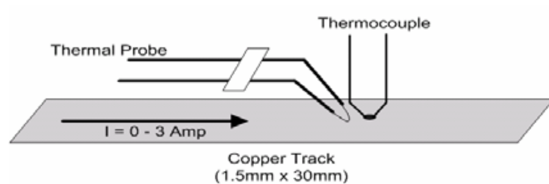


Figure 4.7 (a): Temperature calibration with a thick copper track and thermocouple

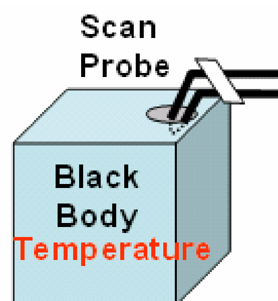


Figure 4.7 (b): Temperature calibration with a black body

In one scheme (Fig. 4.7 (a)), various current intensities are passed along a thick copper track with width of about 1.5 mm. The temperature of the copper track is monitored with a thermocouple fixed nearby. The thermal probe is placed in contact with the copper track while measurements are taken. The thermal probe (sensor), the copper track (non-calibrated heater) and the thermocouple (sensor) constitute a three-element calibration system. A relationship between measurements taken (voltage reading) and temperature change (with varying current supplies) is thus established. However, there are a few short-comings with this scheme.

Firstly, there is difficulty in maintaining a constant contact force between thermocouple and copper track due to the surface roughness of the copper track. This makes the temperature measurement very unreliable. Secondly, due to the large size of the thermocouple used, the average temperature of the contact area is captured whereas the thermal probe is measuring local temperature at the nanoscopic scale. Finally, there is also the problem of current leakage from the copper track through the resistive thermal probe which is exposed and conducting at the point of contact unless proper isolation is provided. Overall, these affect the accuracy of measurements taken.

In another scheme (Fig. 4.7 (b)), the whole thermal probe is placed inside a black body where the temperature can be controlled. The thermal probe (sensor) and the black body (calibrated heater) are a two-element calibration system, thus reducing errors involved in the heat transfer between elements. This setup allows for a direct correlation between thermal probe measurement and temperature. Here, there is no issue of thermocouple contact force variation and no large thermal mass of thermocouple involved. The setup is also easily achieved and consistent results can be obtained. However, there is one major difference between this calibration scheme and actual experimental condition. In this calibration scheme, there is no point contact of the thermal probe on the DUT as the whole thermal probe is being heated up in the black body. Thus the thermal probe resistance change due to contact force of probe on DUT is not considered. Furthermore, the whole thermal probe is also not heated up in actual experimental condition (where the arms of the thermal probe are acting as heat sink to increase the sensitivity of the thermal probe in actual situation), and this results in calibration error.

The eventual calibration tool adopted after consideration of the actual experimental conditions is shown in Fig. 4.8.

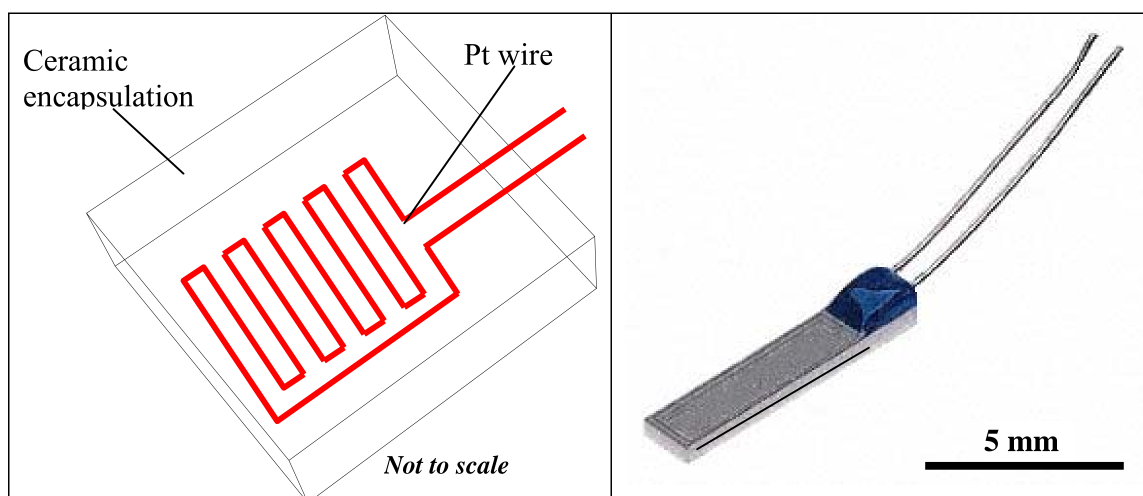


Figure 4.8: Temperature calibration with platinum resistance thermometer (PT100). Schematic (left) and actual (right).

Here, a platinum resistance thermometer, PT100 thin film (DM503) is used. This is produced by the deposition of a platinum film onto a flat ceramic substrate, the platinum being sealed to provide protection. Its ice point resistance is 100 Ω with a temperature range of -50 °C to 500 °C that is well within the actual experimental temperature range required. It has a thermal response of 0.1s. This scheme allows the thermal probe to be positioned onto the PT100 with the help of the AFM, offering a consistent point contact spot where local temperature can be measured. This also ensures that a constant contact force is maintained by the use of the AFM.

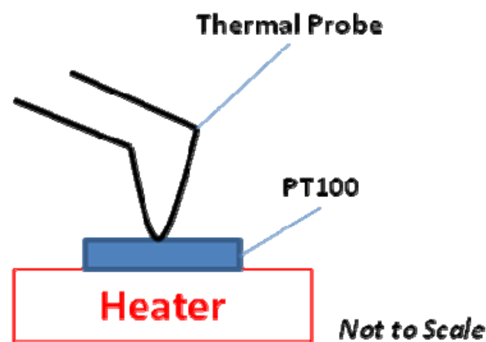


Figure 4.9: Schematic of SThM Calibration Scheme

The resistance of the PT100 is verified by placing it in an ice bath and agrees well with the conversion chart provided in the data sheet. Both the thermal probe (sensor) and the PT100 (DUT / sensor) form a two-element calibration system. The temperature of the heated PT100 is determined from its resistance reading. Concurrently, the equivalent SLIA voltage outputs due to changes in thermal probe resistance at various PT100 temperatures are measured and calibrated accordingly. This calibration scheme offers the closest match to actual experimental condition and is easily set up to give a consistent read out.

4.3.2 Results for Single Lock-In Temperature Calibration

Temperature measurement is performed with a thermal probe current of 1.64 mA at a frequency of 98.7 kHz. This is the lock-in frequency and is chosen to be sufficiently high to avoid interference from the power line (50/60 Hz), to reduce 1/f noise as well as to allow for short thermal signal acquisition time. This frequency is also compatible with the bandwidth of the LIA. A low current is chosen to ensure that the thermal probe does not experience self heating which may result in thermal runaway issues, thus affecting the

temperature of the DUT being measured. The temperature of the PT100 is determined by passing a low fixed current through it and measuring its resistance. The low current ensures there is no self heating of the PT100. The equivalent temperature of the PT100 is read off from the conversion chart provided. In this way, the temperature of the PT100 can be set by passing the desired current through the heater stage. A plot of Wheatstone Bridge measurement voltage against PT100 temperature is obtained for a temperature range between room temperature at 25 °C and 90 °C as shown in Fig. 4.10.

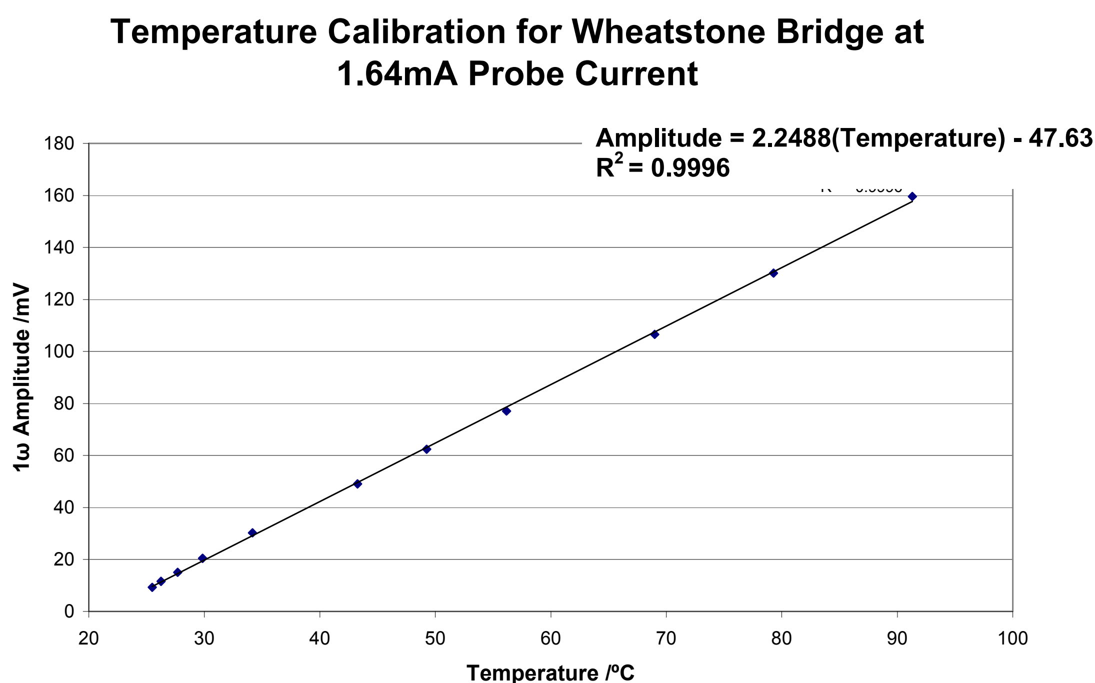


Figure 4.10: Temperature calibration plot for single lock-in setup

From the calibration plot, a temperature sensitivity of 2.25 mV/K is determined with a thermal probe current of 1.64 mA at 98.7 kHz. The data points collected show good linear fit with the linear regression goodness of fit, R^2 value of 0.9996. Another set of calibration plot with a temperature sensitivity of 11.49 mV/K is also achieved for a higher thermal probe current of 8.45 mA at 98.7 kHz. This also verified the linearity

between sensitivity and thermal probe current as shown in Eqn. 3.7. A 5.15 times increase in thermal probe current results in approximately 5.11 times increase in temperature sensitivity.

4.4 SLIA Thermal Conductivity Measurement (Qualitative)

Thermal conductivity is an important property in many advanced applications. There are many factors which may be tied to the thermal conductivity of the sample such as the sample doping profile as investigated by Lee Teck Hock [109] or using thermal conductivity as a function of porosity [110]. Also, with the thermal conductivity data, important information may be obtained to provide greater knowledge in the processing of new materials so as to achieve efficient heat dissipation in the increasingly closely packed integrated circuits where heat dissipation is becoming a major issue in device reliability.

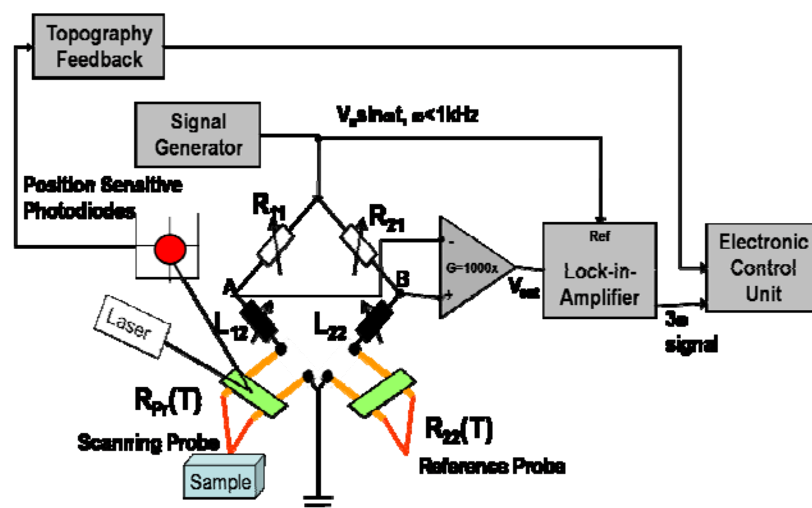


Figure 4.11: Schematic setup for SLIA thermal conductivity measurement

Figure 4.11 shows the setup for thermal conductivity measurement. The 3ω method as developed by Cahill [111] is used. Cahill developed the 3ω method with a straight line

heat source. In this setup, the probe can be assumed to behave like a line heat source because of the small contact area of the probe with the sample. Figure 4.12 shows a graphical explanation of this 3ω method.

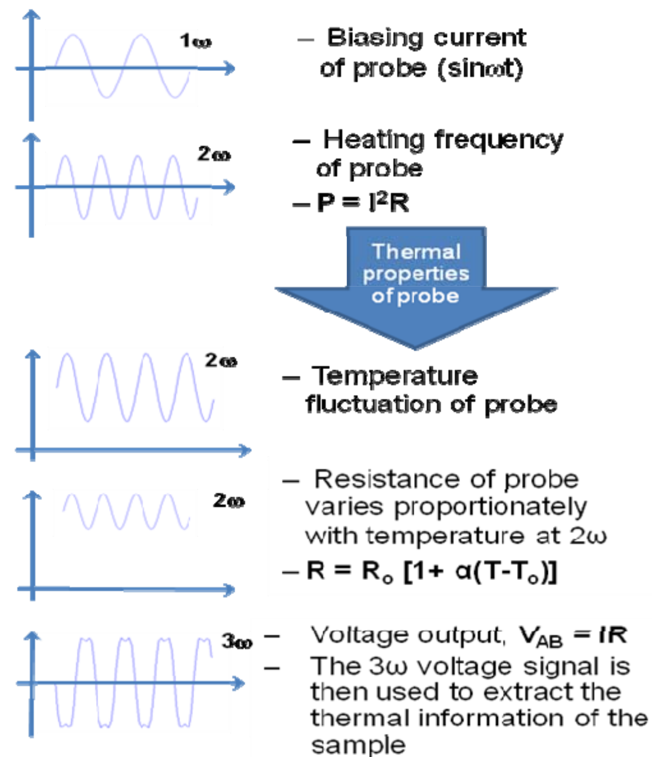


Figure 4.12: Graphical Explanation of 3ω Method [112]

A brief derivation of the technique is discussed here. Firstly, assume the thermal probe is heated by a sinusoidal current with angular frequency given by Equation (4.2).

$$i(t) = i_0 \sin(\omega t) \qquad (4.2)$$

where

$i(t)$ = Periodic Current Supplied

$i_0(t)$ = Amplitude of Supplied Current

This probe is then brought into contact with the sample under study. Since the probe is at a higher temperature than the sample which is not biased, a temperature gradient is created causing the heat flux to flow into the sample. The resultant heat flux or diffusive thermal wave has an angular frequency of 2ω (since the heating power is proportional to the square of the supplied current).

The amplitude of this thermal wave, ΔT at a distance, r from the thermal probe (heat source) is given by Equation (4.3) provided the diffusion length of the thermal wave is large compared with the width of the heat source.

$$\Delta T = \frac{P}{\pi\kappa}[\frac{1}{2}\ln(\frac{2D}{r^2}) - 0.5772 - \frac{j\pi}{4} - \frac{1}{2}\ln(\omega)] \propto \frac{1}{\kappa} \qquad (4.3)$$

where

P = Amplitude of the heating power per unit length

D = Thermal Diffusivity of the material $(=\frac{\kappa}{\rho_d C})$

This diffusive thermal wavelength λ, is also known by Cahill as the thermal penetration depth and is given by equation (4.4).

$$\lambda = (\frac{D}{2\omega})^{\frac{1}{2}} = (\frac{\kappa}{2\rho_d C\omega})^{\frac{1}{2}} \qquad (4.4)$$

where

λ = Thermal Wave Length

ω = Angular Frequency

ρ_d = Density

C = Specific Heat

It is observed that by changing the modulating frequency ω, the thermal wavelength and thus the penetration depth can be varied. As the Opsal-Rosencwaig theory [113] demonstrates, a surface temperature probe is able to provide information of the thermal

feature as long as the feature is within the range of the thermal wave. This allows for nondestructive depth profiling of the subsurface features.

The resistance of the resistive thermal probe depends almost linearly on its temperature according to Equation (4.5).

$$R_{pt}(T) = R_0[\alpha_{pt}(T - T_0) + 1] \tag{4.5}$$

where

R_o = Resistance of Tip at T_o

α_{pt} = Coefficient of Resistivity of Pt

Since the heating power oscillates with frequency 2ω (i^2R), the electrical resistance, *R(t)* also changes with 2ω according to Cahill [114] as shown in Equation (4.6).

$$\begin{aligned} R(t) &= R_{dc} + \Delta R(t) = R_{dc} + \frac{dR}{dT}\Delta T \frac{1}{2}[1 - \cos(2\omega t)] \\ &= R^*_{dc} - \frac{dR}{dT}\Delta T \frac{1}{2}\cos(2\omega t) \end{aligned} \tag{4.6}$$

where

R^*_{dc} = D.C. Resistance

$\frac{dR}{dT}$ = Coefficient of Resistivity of the Thermal Probe, α_{pt}

Therefore, voltage drop across the thermal probe, *U(t)* is obtained by combining Equation (4.2) and (4.6) as follows.

$$\begin{aligned} U(t) &= i(t)R(t) \\ &= R^*_{dc} i_0 \sin(\omega t) - i_0 \sin(\omega t)\frac{dR}{dT}\frac{\Delta T}{2}\cos(2\omega t) \\ &= R^*_{dc} i_0 \sin(\omega t) - i_0 \frac{dR}{dT}\frac{\Delta T}{4}[\sin(3\omega t) - \sin(\omega t)] \\ &= (R^*_{dc} i_0 + i_0 \frac{dR}{dT}\frac{\Delta T}{4})\sin(\omega t) - i_0 \frac{dR}{dT}\frac{\Delta T}{4}\sin(3\omega t) \end{aligned} \tag{4.7}$$

From Equation (4.7), it is observed that the voltage drop across the thermal probe consists of two components, the first and third harmonic of the modulation current.

The third harmonic component is independent of the D.C. resistance of the thermal probe and therefore the overall temperature of the probe and the sample. However, it is related to ΔT which in turn is inversely proportional to the thermal conductivity of the sample.

Therefore, a qualitative study of the contrast in thermal conductivity of the sample can be done by incorporating a Wheatstone Bridge and Lock In Amplifier setup and extracting the third harmonic component of the voltage drop across the thermal probe.

4.5 Proper Sample Mounting and Leveling for Accurate Thermal Measurement

For better measurement accuracy, any sample mounted onto the stage should be secured and not be shifted during the thermal acquisition process. Also, it should be noted that the thermal micrograph is usually coupled with topography artifacts due to the dependence of the effective contact area with topographic features. Thus, it is of paramount importance to ensure that the sample is as level as possible with respect to the thermal probe scanning plane. Without doing so, additional topographic effects in addition to existing ones are introduced into the measurement due to increased surface area of contact as illustrated in Figure 4.13.

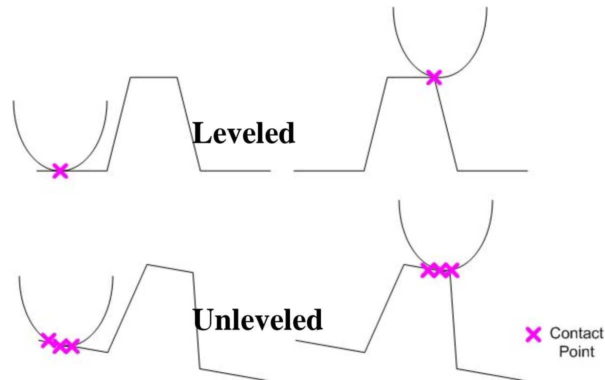


Figure 4.13: Increased Contact Area due to Unleveled Sample

The increased contact area would increase the heat flux away from the thermal probe and create the illusion of a higher thermal conductivity surface.

In physical leveling, initial line scan of a known flat region on the sample is done both vertically and horizontally and any tilt profile observed is minimized to ensure that the field of scan of the thermal probe is parallel to the plane of the sample as illustrated in Figure 4.14.

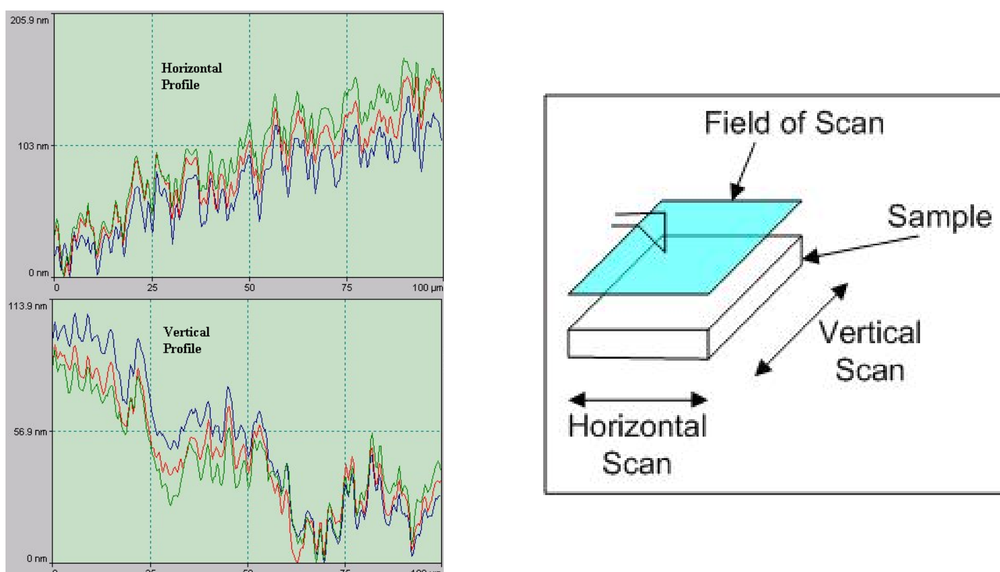


Figure 4.14: Physical Leveling of Sample

By doing this physical leveling, the need to perform additional software leveling using SPMLab™ provided with the explorer AFM system is avoided. This is important as any software leveling method done may introduce artifacts which are not present on the actual sample. The reason for these artifacts is because one of the methods the software uses for leveling is the 1-dimensional line of best fit method which might not be suitable in the presence of certain topography such as a step height.

As illustrated in Figure 4.15, what is originally a good topography profile of a step height has become a valley after inappropriate software leveling is carried out.

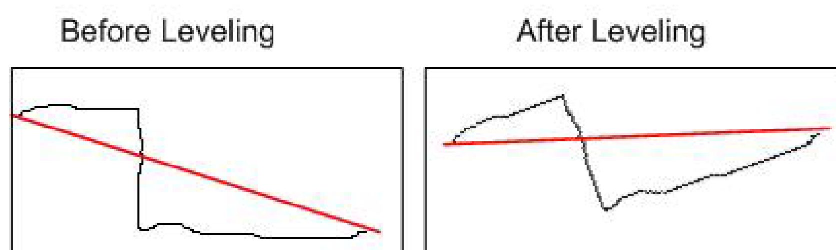


Figure 4.15: Artifact Due to Leveling

However, this does not mean avoiding the use of software leveling since using only physical leveling may not be a realistic target due to some extremely small scale dimensions involved (1 µm or less). Furthermore, proper use of software leveling helps to bring out any minor feature present. As shown in Figure 4.16, appropriate software leveling reduces the sample height from 4.9 µm to 1.63 µm (Circle A) and brings out the small defect present in the sample (Circle B).

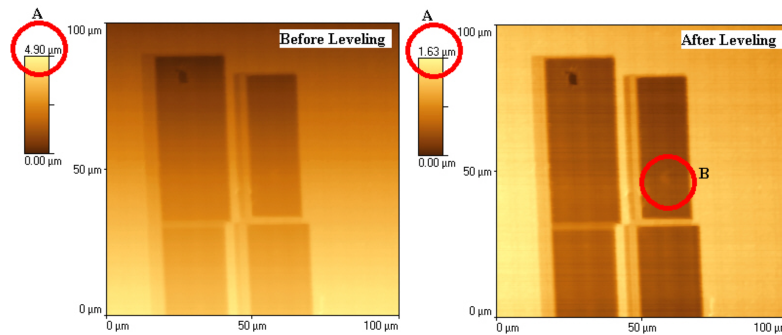


Figure 4.16: Effect of Leveling

The following chapter discusses some of the applications of the SLIA SThM in terms of temperature and thermal conductivity measurement.

Chapter 5: SLIA SThM Applications

This chapter describes some of the applications that have been performed with the SLIA SThM. Both temperature measurement in passive mode and thermal conductivity measurement in active mode were used.

5.1 Electromigration Test Structure (Temperature)

This section discusses the application of the temperature mode of SLIA SThM. An electromigration (EM) test structure is stressed by a large current flow at an elevated temperature to induce voiding in the aluminium interconnect. Optical micrograph of the void that is created at the corner of the interconnect is shown in the inset of Fig. 5.1. A current of 60 mA is subsequently passed through the aluminium interconnect to allow mapping of the thermal distribution around the voiding location by the SThM.

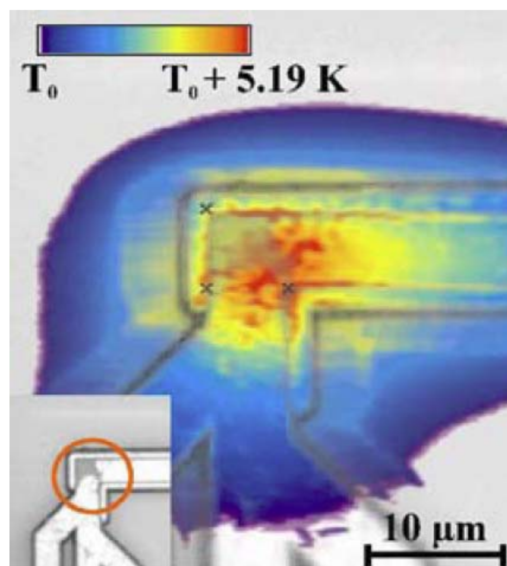


Figure 5.1: Thermal micrograph overlaid with optical micrograph of a biased interconnect with presence of a void. [115]

Overlay of the temperature micrograph with the optical micrograph in Fig. 5.1 clearly shows the temperature distribution in the vicinity of the void. The presence of void at the corner of the interconnect structure resulted in current crowding and increased temperature of about 5 K measured compared to interconnect further away from the void location. The location where the current crowding occurs through the remaining aluminium interconnect can also be clearly visualized from the temperature peak captured.

5.2 Hard Disk Write Head Heater Coil (Temperature)

Higher recording density of hard disk drive demands smaller head-disk clearance and thus lower flying height. Thermal flying height control (TFC) makes use of the protrusion caused by an embedded thermal actuator to control the head-disk spacing and this is currently the industry standard in flying height control. [116][117]

At present, studies on the TFC have been focused on the protrusion of the slider in the vertical direction and the flying height itself, and little has been reported on the lateral shift of the read/write head in the down-track and cross-track directions caused by the heating current as well as writing current induced heating effects. The AFM and SLIA SThM are used to study the lateral shift of the read/write head induced by the thermal actuated protrusion. Under non-flying static testing condition (where higher temperature increase and larger expansion occur) during AFM and SThM measurements, the shift effects as well as the hidden asymmetry in head structures and heating profiles for

fabricated production head gimbal assembly (HGA) are amplified and thus able to be clearly identified.

Fig. 5.2 (a) shows an optical micrograph of an unshielded type [118] hard disk TFC perpendicular magnetic recording (PMR) head where the heater coil is located beneath the highlighted region. The two white strips are the return poles of the hard disk write-head with a higher thermal conductivity than the surrounding materials. A cross-sectional schematic is provided in Fig. 5.2 (b).

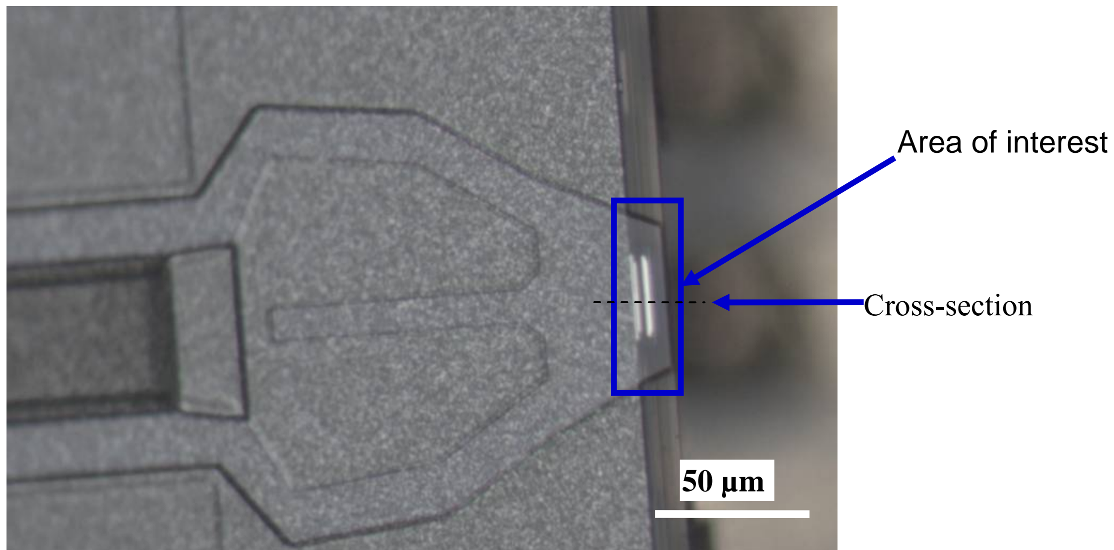


Figure 5.2 (a): Optical micrograph of an unshielded type hard disk TFC PMR head

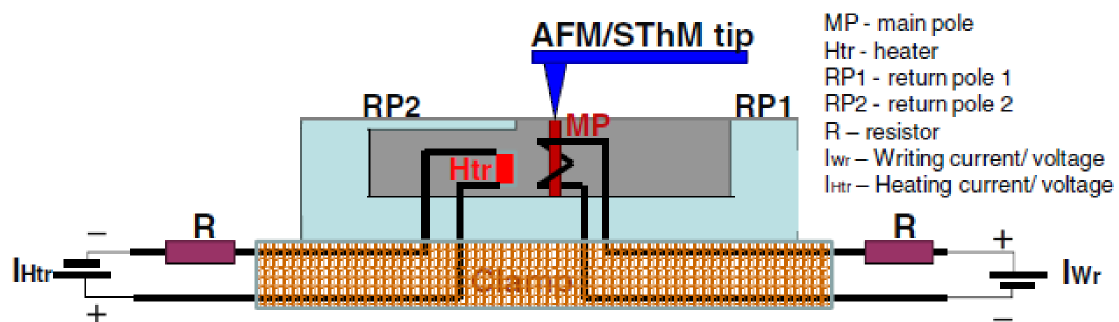


Figure 5.2 (b): Schematic of AFM/SThM measurements of TFC perpendicular head with cross-sectional view of head structure illustrated. (MP: main pole; RP1: return pole 1 (leading or bottom side); RP2: return pole 2 (trailing or top side); Htr: heater; IWr: writing current/voltage source; IHtr : heating current/voltage source; R: resistor).

As shown in Fig. 5.2 (b), the micrometre-sized heater coil was located near the write/read head elements and embedded into the insulating materials (Al_2O_3) under the air bearing surface (ABS).

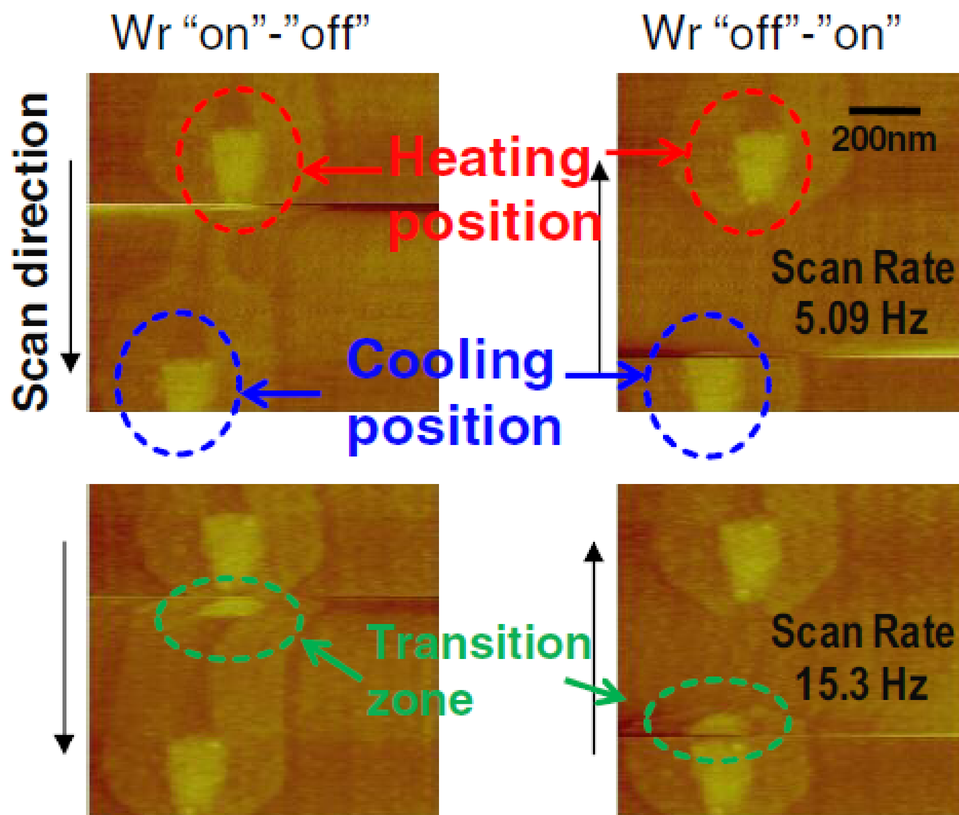


Figure 5.3: AFM images of TFC PMR head during writing current on and off. (Image size: 1 μm by 1 μm; height contrast: 50 nm.)

Figure 5.3 shows typical AFM images of the TFC PMR head when write current (writing power ~20 mW supplied by a dc voltage source applied to the write head through a resistor of ~47.5 Ω) was turned on and off. Left images were captured with horizontal fast scan direction and downward slow scan direction (the write current to the write coil of the write head was switched off at the write pole leading edge position); right images were captured with upward slow scan direction (the write current to the write coil of the write head was switched on at the pole trailing edge position). Bottom images were for faster line scan rate (15.3 Hz) than those upper images (scan rate = 5.09 Hz). Both the heated and the cooled positions of the main pole were captured in a single AFM scan, and

are delineated by circles (red and blue circles, respectively). Lateral head shift (in both down-track and cross-track directions) is clearly observed as evidenced by the different cooling and heating positions. Due to the expansion/contraction of the head, the main poles were laterally shifted (from heating/cooling position to cooling/heating position) as observed.

To obtain the temperature rise so as to explain the significant down-track and cross-track shift of the PMR head observed by AFM, a SLIA SThM was further used to measure the change in temperature before and after thermal activation as well as the localized temperature distribution around the active region.

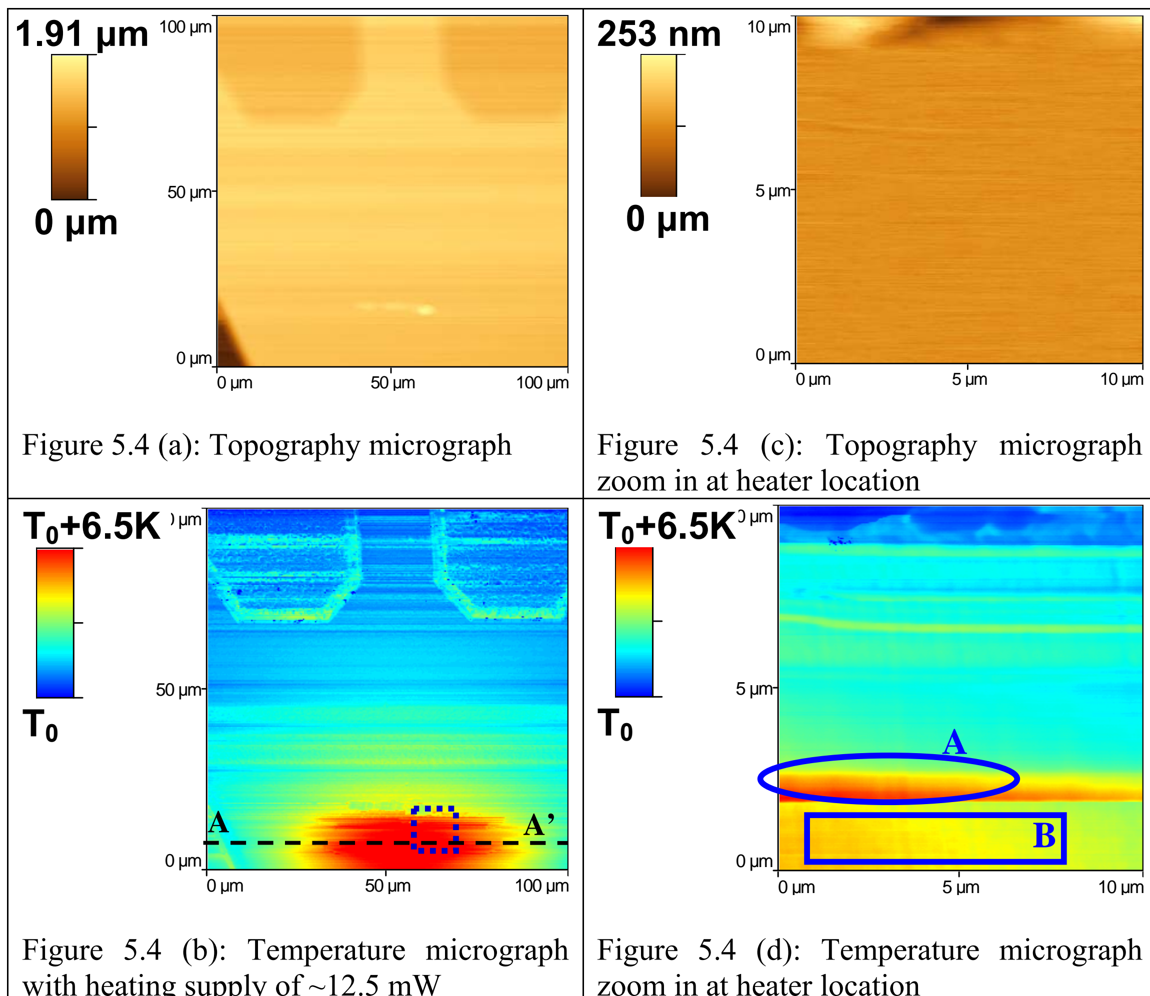


Figure 5.4 (a): Topography micrograph

Figure 5.4 (c): Topography micrograph zoom in at heater location

Figure 5.4 (b): Temperature micrograph with heating supply of ~12.5 mW

Figure 5.4 (d): Temperature micrograph zoom in at heater location

Fig. 5.4 (a) and (b) show the topography and temperature micrographs respectively of the TFC PMR head with heater coil supplied with a heating power of 12.5 mW. At this resolution, the whole heater coil location and its surrounding are captured as one large heated region without much detailed information being resolved. However, a temperature contrast of 6.5 K can be observed.

At a higher resolution with smaller scan area, further details are revealed. Fig. 5.4 (c) and (d) show a zoom-in 10 μm by 10 μm section of the heater coil region denoted by the dotted box in Fig. 5.4 (b). From the topography micrograph in Fig. 5.4 (c), an expansion of about 253 nm is detected within this smaller scan area although the return pole location cannot be distinguished. From the temperature micrograph in Fig. 5.4 (d), the return pole location can be clearly observed at region A which has a higher temperature than the surrounding. This is because region A is made of a higher thermal conductivity material and is being heated up faster than the surrounding. At region B, the outward spreading of heat from the heater coil to the surrounding can also be visualized from the captured temperature contour.

To characterize the actual temperature rise, a heater on and off experiment was carried out. Figure 5.5 shows SThM micrograph and temperature profiles versus time during heater on and off (heater power ~33 mW) conditions.

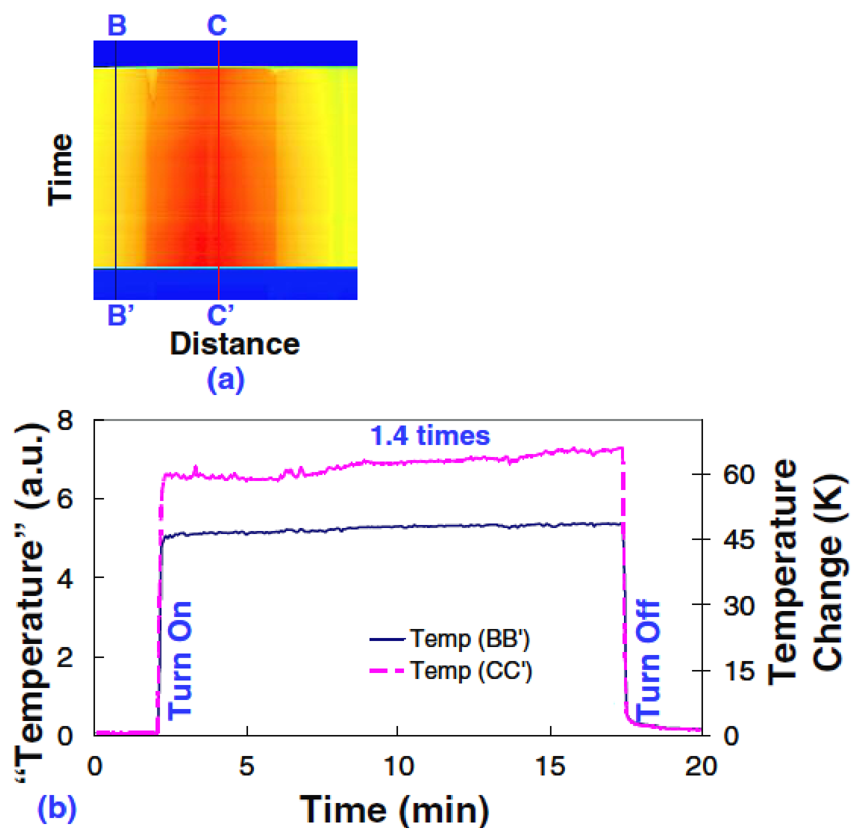


Figure 5.5: SThM image and temperature profiles versus time during heater on and off (heater power ~33 mW). (a) Thermal micrograph of TFC perpendicular head along similar line as AA' in Fig. 5.4 (b) over time (horizontal axis of distance from left to right is 100µm; vertical axis of time from top to bottom is 20 min); (b) thermal line profiles at the centre (CC') and off-centre (BB') of the heat source as a function of time.

A similar line location like AA' as shown in Fig. 5.4(b) (the line passes through the point where the highest temperature was detected) was chosen to study the actual temperature rise. In Fig. 5.5 (a), the SLIA SThM was set to repeatedly scan across this line location over the measurement time of 20 min. After about 2 min into the measurement, the heater was supplied with a power of ~33 mW (heater turn-on) as the thermal measurement continued for ~15 min. Before the end of the thermal measurement, the heater power was turned off. The thermal micrograph showing the same line location over time was obtained and is shown in Fig. 5.5 (a). This micrograph shows the temperature contrast

between the heater-off and heater-on states. There is ~18 K temperature difference between the higher temperature centre position (CC') and the lower temperature off-centre position (BB') over time. Figure 5.5 (b) shows the thermal line profiles (temperature change over time) at the higher temperature centre position (CC') and the lower temperature off-centre position (BB') through the heater-off, heater-on and then heater-off period. It can be seen that there is a sharp and fast temperature change immediately after heater turn-on and turn-off as compared with the small and slow temperature change over the duration of the heater on for ~15 min. The highest temperature change of ~66 K is detected between the two states (on and off) of the heater. The hotter centre position along CC', with an average temperature change of ~66 K, is about 1.4 times larger than the cooler off-centre position along BB', with an average temperature change of ~48 K. The observed large temperature change is consistent with the previous report of more than 42 K temperature increase observed for a non-flying head. [119] This large temperature change is able to account for the significant shift observed in the main pole under the non-flying condition.

5.3 Electromigration Test Structure Characterizations (Thermal Conductivity) [120]

Here, the SThM system is used to study electromigration (EM) phenomena. The EM test structure is made up of interconnects of different width and length, terminated by bond pads or vias. There are 3 major blocks of passivated meander aluminium interconnects with widths of 5.3 µm, 3 µm and 0.7 µm. The sample was placed on a hot plate of temperature 513 K and stressed at a constant d.c. current of 50 mA to induce the

formation of electromigration defects. The various types of defects detected include extrusion and subsurface voids.

5.3.1 Extrusion

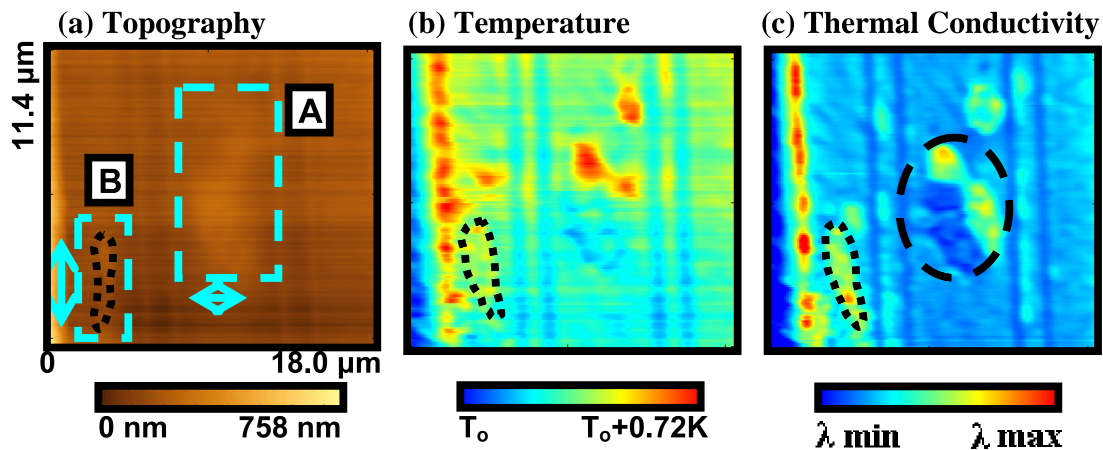


Figure 5.6: Micrographs of an EM sample

Figure 5.6 (a), (b) and (c) shows the topography, temperature and thermal conductivity micrographs of extrusion defects respectively. In region A of the topography micrograph, a smooth "bump" with a peak height of around 100 nm is detected. From the corresponding temperature micrograph, regions of local heating are detected. The increase in temperature is likely due to current crowding resulting in joule heating in the defective region. The same region in the corresponding thermal conductivity micrograph shows similar features with peaks at where the hot spots are detected. A closer look at the "bump" region is shown in Fig. 5.7.

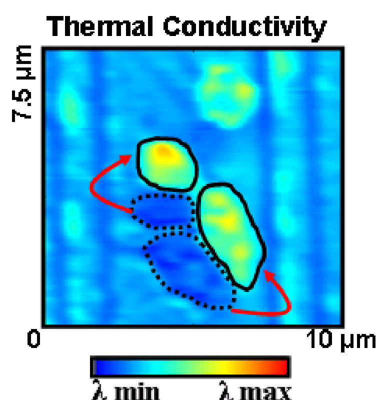
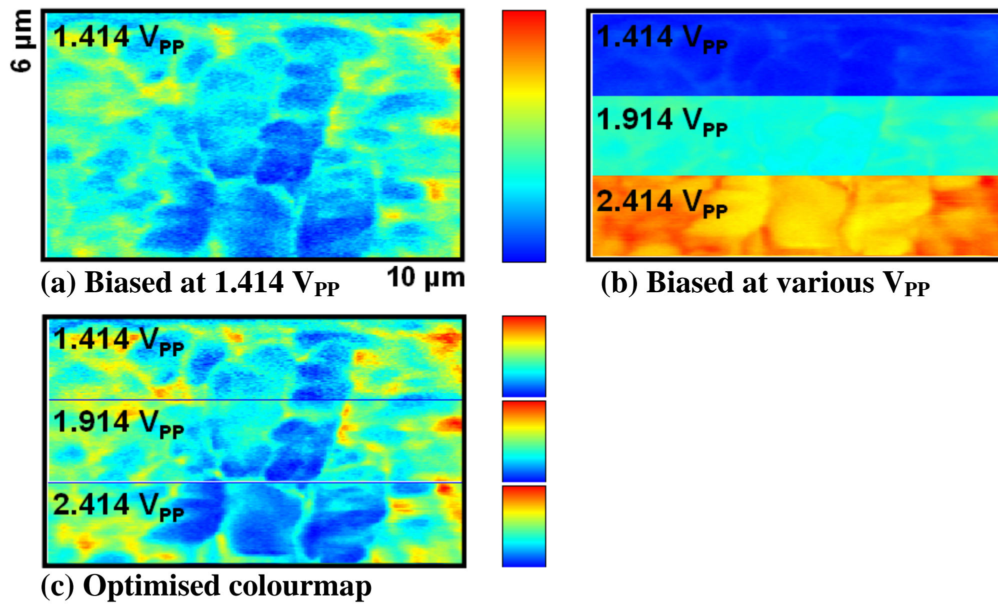


Figure 5.7: Thermal Conductivity Micrograph

The dotted lines highlight regions of low thermal conductivity while the bold lines mark out regions of high thermal conductivity. The shape of the two low thermal conductivity regions seems to fit the corresponding two regions of high thermal conductivity indicating mass transport phenomenon of electromigration. In this scenario, aluminium atoms are transported due to collision with electrons during high current stressing of the sample under elevated temperature, hence resulting in increased packing density further up the interconnect. This increases the thermal conductivity because of increased heat conduction by lattice vibration and electron transport. Consequently, the region where the materials had been moved away suffered a drop in thermal conductivity due to increased porosity resulting in poorer heat conduction.

One consideration to note is that regions of hot spots in Fig. 5.6(b) showed up as regions of high thermal conductivity in Fig. 5.6(c) were obtained using the 3ω technique. The assumption was that hot spot locations were supposed to register a lower thermal conductivity. To verify that the temperature micrograph did indeed contain heating information, the following experiment was conducted.



(a) Biased at 1.414 V_{PP} **(b) Biased at various V_{PP}**

(c) Optimised colourmap

Figure 5.8: Heating of DUT in dynamic mode

To ensure that there was no progressive heating of the sample, dynamic heating was incorporated where an a.c. current was used to heat up the sample rather than d.c.. From Fig. 5.8(b), it can be clearly observed that the sample is heated up with increasing bias. However, once the colourmap for each band is optimized as shown in Fig. 5.8(c), the micrograph obtained is similar to that biased at a single voltage of 1.414 V_{PP} (Fig. 5.8(a)). One conclusion that can be made is that the experimental setup and biasing parameters used are able to result in heating of the sample.

A proposed explanation for the similarities between temperature and thermal conductivity micrographs is as follows.

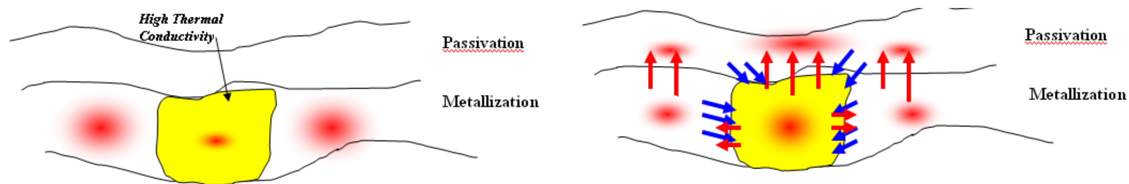


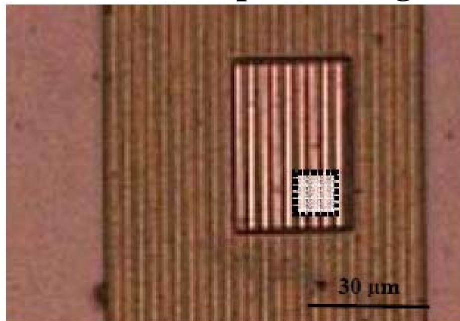
Figure 5.9: Heat Flow Proposal

High thermal conductivity region acts as a heat sink (Fig. 5.9), thus progressively gets heat from low thermal conductivity region and redistributes it to its surrounding. Passivation above high thermal conductivity region heats up due to its inability to lose heat rapidly while the underlying high thermal conductivity region continues to be an efficient transport for heat source.

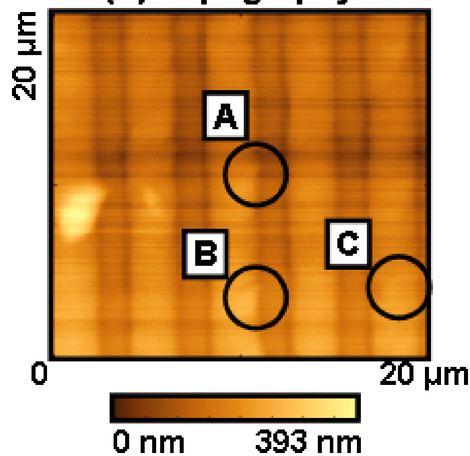
A strip-like outgrowth of about 100 nm in height and 2 μm in length is shown in region B of Fig. 5.6(a). In the corresponding thermal conductivity micrograph in Fig. 5.6(c), the higher thermal conductivity than surrounding is registered over a much larger area. A possible explanation for this could be due to formation of an extrusion in the underlying metal track resulting in a small bump appearing in the topography. This may be the reason for the higher thermal conductivity covering a larger area as observed in the micrograph.

5.3.2 Subsurface Void

(a) Reflected Optical Image



(b) Topography **(c) Thermal Conductivity**



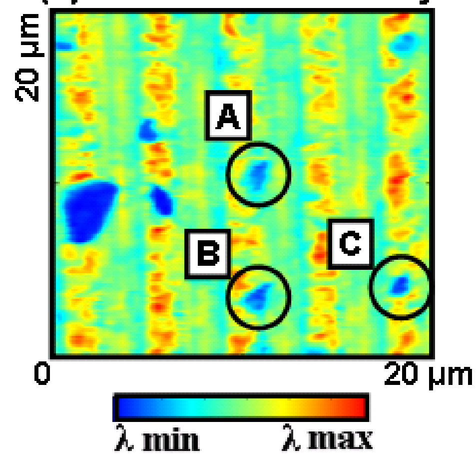


Figure 5.10: Micrographs of an EM sample with subsurface voids

Fig. 5.10(a) shows the reflected optical image of another electromigration sample with part of the passivation layer thinned by FIB. Each metal line has a width of about 3 µm. The topography and thermal conductivity micrographs are shown in Fig. 5.10(b) and Fig. 5.10(c) respectively. In Fig. 5.10(c), low thermal conductivity regions marked A, B and C, are not apparent in the topography micrograph. Furthermore, this drop in thermal conductivity is not due to topographic effect since the sharp decrease does not occur for every peak in the topography as shown in the horizontal line profile cutting across feature B and C in Fig. 5.11.

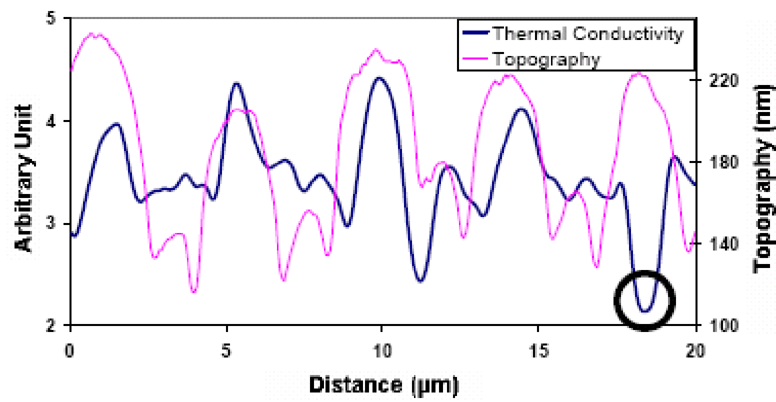


Figure 5.11: Line Profile of Topography and Thermal Conductivity

Therefore, regions where there is a sudden decrease in thermal conductivity can be attributed to the formation of subsurface voids. From the thermal conductivity image in Fig. 5.10(c), void C appears to have a lateral dimension of around 600 nm.

Chapter 6: SLIA SThM Limitation and Optimization

Despite the benefits and detailed thermal information which are provided by the SThM system, there are some limitations and considerations which have to be taken care of when analyzing the results obtained. This chapter discusses the two critical issues affecting the conventional SThM measurement technique. One of them is the coupling of topography information into the thermal signal due to variation in effective contact area between the probe and sample. These topography artifacts are common problem which is usually associated with scanning probe-based techniques. Another limitation is the temperature drift of the overall measurement system resulting in reduced sensitivity in the results obtained. Some amount of settling time is required before any thermal measurement can be performed. This chapter concludes by proposing some post processing algorithms for the thermal signal acquired in order to minimize the noise introduced by temperature drift of the system.

6.1 Topography Artifacts

Topography artifacts can be easily coupled into the thermal micrographs, especially when measurement is carried out across features with step height differences (either a protrusion or a hole). These result in different areas of the thermal probe coming into contact with the sample being measured at different probe locations.

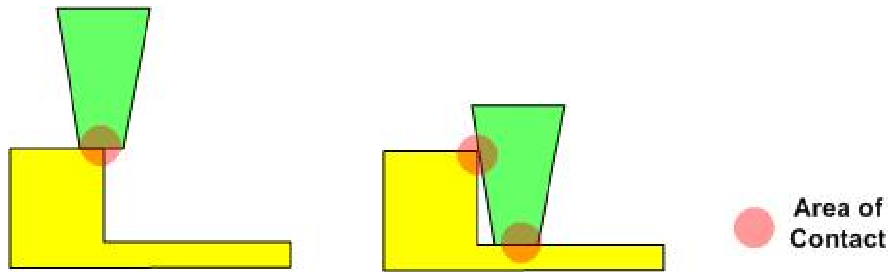


Figure 6.1: Schematic showing increased area of contact (topographic artifact) due to step change in topography

As shown in Fig. 6.1, the change in the thermal probe's area of contact with the sample when encountering topography changes at different locations of the sample lead to variation of heat transfer unless enough time is provided for equilibrium to be established. This may not be possible as it results in longer measurement time when acquiring thermal micrographs of sufficient resolution. Even if time is allowed for equilibrium to be established, thermal resolution is sacrificed since the heat would have spread and presence of any hot spot may not be easily and accurately localized.

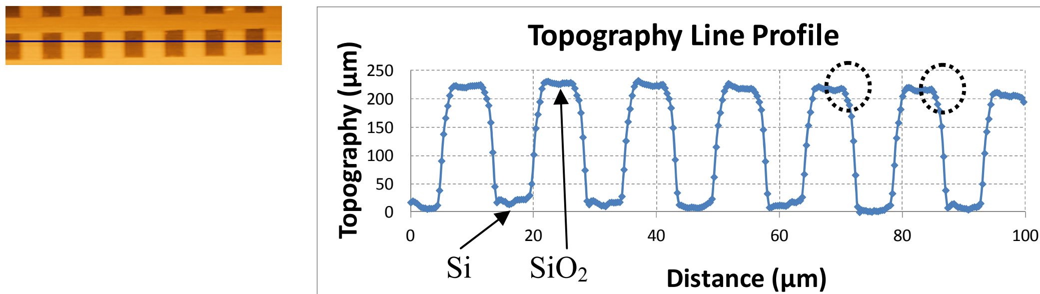


Figure 6.2 (a): Topography micrograph (left) and corresponding line profile (right) of calibration grid

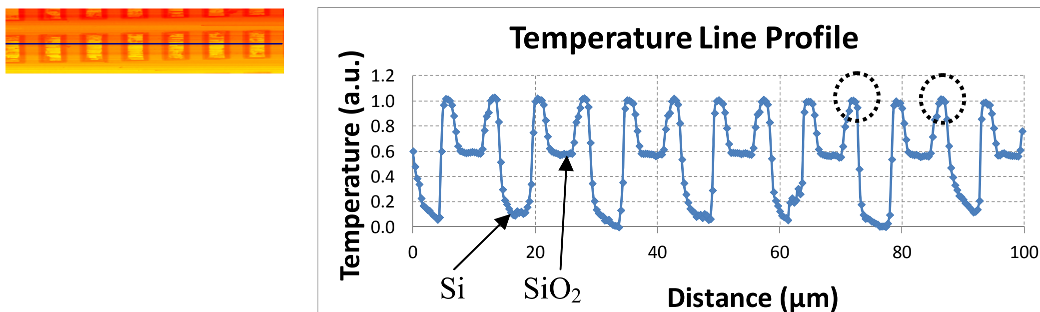


Figure 6.2 (b): Temperature micrograph (left) and corresponding line profile (right) of calibration grid

Figure 6.2 shows the topography and temperature micrographs of a calibration grid and its corresponding line profiles. The calibration grid consists of square holes of Si within the SiO_2 surface. It can be observed from the temperature line profile in Fig. 6.2 (b) that there are regions of higher temperature (marked out by dotted circles) and these are at the edge of the step feature in Fig. 6.2 (a) (similarly marked out by dotted circles). These are clearly topography artifacts due to reduced area of contact between thermal probe and calibration grid similar to the left schematic of Fig. 6.1. As the calibration grid is not heated, the reduced area of contact means the least amount of heat loss from thermal probe to calibration grid, thus giving rise to highest thermal signal compared to other locations on the grid. The observed lower thermal signal from Si compared to SiO_2 is

reasonable since Si has a much higher thermal conductivity compared to SiO_2 (Si: ~148 $Wm^{-1}K^{-1}$; SiO_2: ~ 1.4 $Wm^{-1}K^{-1}$). Thus Si at the bottom of the grid is able to draw more heat away from the thermal probe when compared to SiO_2 at the surface of the grid.

6.2 Temperature Drift During Thermal Measurement

During temperature measurement, small temperature drift in the Kelvin range is common during the initial preparation of the measurement setup. This is usually associated with temperature gradients and transients in the various instruments used for the SThM setup. Some settling time is required for the measurement system, sample and the environment to stabilize before accurate and sensitive thermal measurement can be achieved. Another strategy to reduce the temperature drift is to have instrumentation with symmetrical design such as the use of reference thermal probe for the non-measuring arm of the Wheatstone bridge. Care is taken to ensure that the setup is not facing the cooling vent of any equipment which may affect the ambient temperature surrounding the measurement setup.

Figure 6.3 shows the optical micrograph of an EM sample used for thermal measurement characterization. In the following measurement, the aluminium tracks were not biased when thermal measurement was performed.

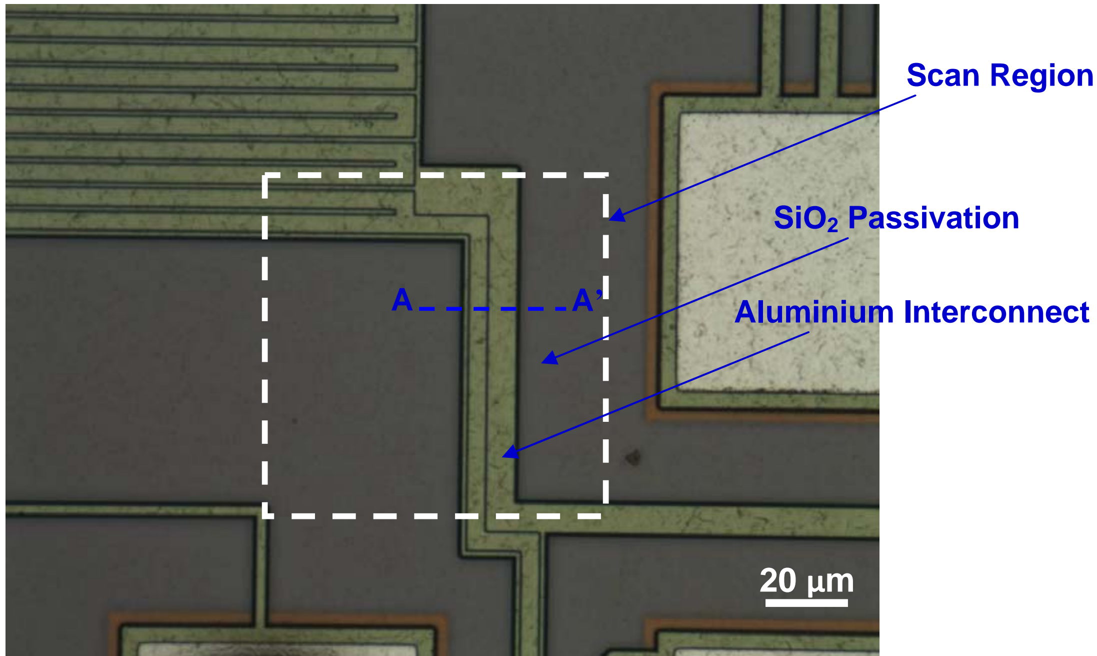


Figure 6.3: Optical micrograph of an electromigration (EM) sampled used for thermal measurement.

Fig. 6.4 shows the various thermal micrographs obtained from the unbiased EM sample at different settling time from initial SLIA SThM setup.

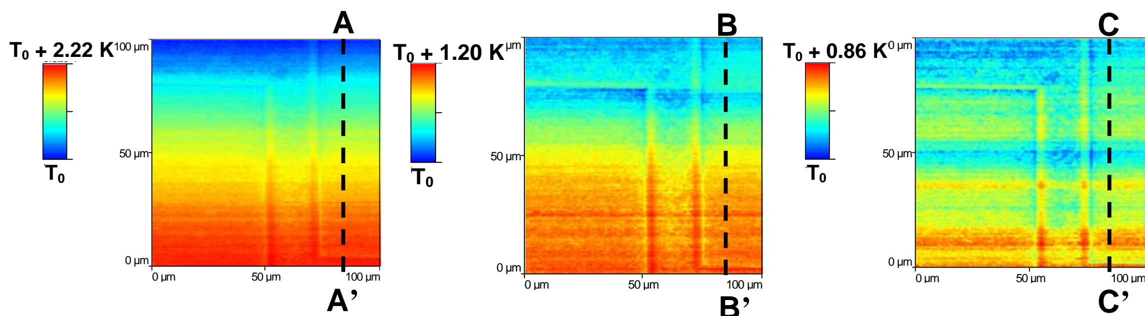


Figure 6.4 (a): Thermal micrograph obtained 30 min from start of experiment.

Figure 6.4 (b): Thermal micrograph obtained 60 min from start of experiment.

Figure 6.4 (c): Thermal micrograph obtained 90 min from start of experiment.

Each thermal micrograph has an acquisition time of 20 min. Therefore, measurement for Fig. 6.4 (a) begins after 10 min of settling time from SThM setup and completes after 30

min of settling time. Similarly, thermal acquisition for Fig. 6.4 (b) and (c) are completed at the end of 60 min and 90 min of settling time. Since the sample is not biased and the whole surface should be in thermal equilibrium, the expectation is there should not be any temperature contrast along the surface of the SiO_2 passivation as indicated by the dotted lines in Fig. 6.4. However, temperature contrast can be observed due to temperature drift of the whole measurement system.

Temperature line profiles along AA', BB' and CC' of Fig. 6.4 (a), (b) and (c) respectively representing thermal measurement taken with increasing settling time are plotted in Fig. 6.5 to characterize the temperature drift during each temperature micrograph measurement time of 20 min.

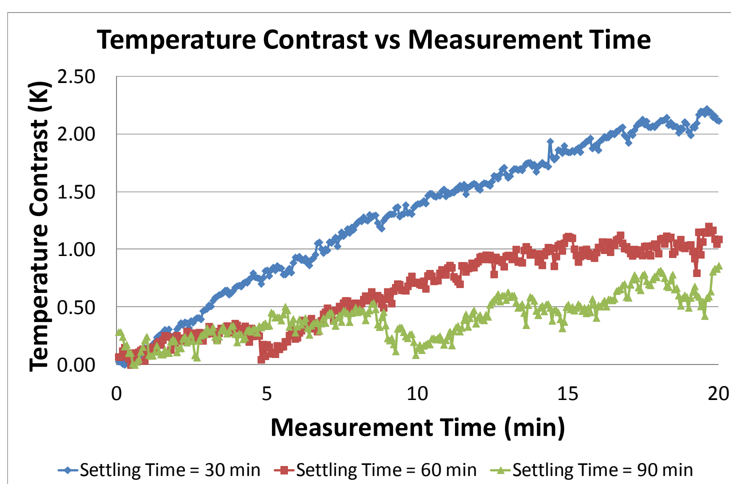


Figure 6.5: Temperature line profiles Along AA', BB' and CC' of Fig. 6.4 at various settling time after equipment setup

From Fig. 6.5, temperature contrast of about 2.22 K is observed along the SiO_2 surface (AA' in Fig. 6.4 (a)) within 30 min of settling time. The temperature drift reduces to 1.2 K (BB' in Fig. 6.4 (b)) after 60 min. This temperature drift is further reduced to 0.86 K

after 90 min from the start of the experiment. This means an uncertainty of 0.86 K after 90 min of setup time.

Figure 6.6 provides an alternative plot showing the temperature delta from the SLIA SThM measurement of the unbiased sample with increasing setup settling time.

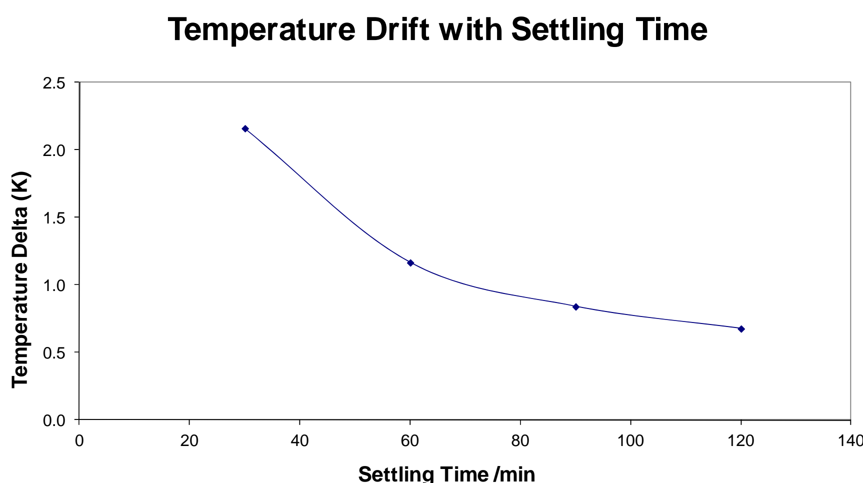


Figure 6.6: Plot of temperature delta at increasing SLIA SThM settling time

From Fig. 6.6, it can be clearly observed that the temperature delta is decreasing with increasing settling time. For sensitive temperature measurement of less than 1 K, long settling time of up to 90 min is required for the SLIA SThM setup to be stabilized assuming the thermal acquisition time is maintained at 20 min.

Marinello et al. [121] had also carried out a similar study on the thermal drift from different commercial SPMs during the initial warming-up phase. In the study, 6 different SPMs operating in the contact mode were characterized. The SPMs were analysed using

infrared camera, which was positioned in close proximity of the tested SPM to measure the temperature gradients and transients of the instrument body. Average temperature measurements were compared and reproduced in Fig. 6.7.

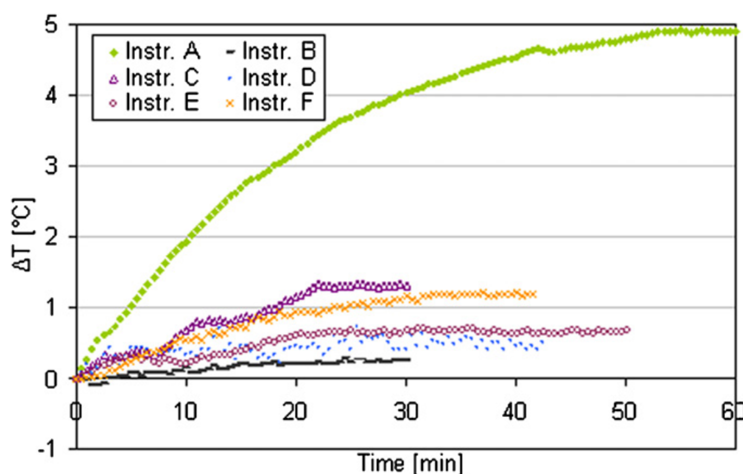


Figure 6.7: Average temperature variation measured immediately after instruments were turned on and actuated up to stabilization [121]

It was determined that the maximum temperature variation can be expected from the initial 30 min immediately after instruments were turned on. Temperatures delta of 0.3 to 4 K with temperature drifts ranging between 0.9 x 10^{-2} and 16 x 10^{-2} $Kmin^{-1}$ were documented. This is in line with the 2.22 K temperature delta or 11 x 10^{-2} $Kmin^{-1}$ (over a thermal acquisition time of 20 min) drift observed in the SLIA SThM experiment during the initial 30 min setup time. This also corresponds to the settling time of ~20 min required for the Wheatstone bridge setup as discussed in section 3.2.4.

The positional drift with respect to setup time is also investigated and presented in Fig. 6.8. Measurement is done by continuously performing a 1D topography measurement across the step profile as indicated along AA' in Fig. 6.3.

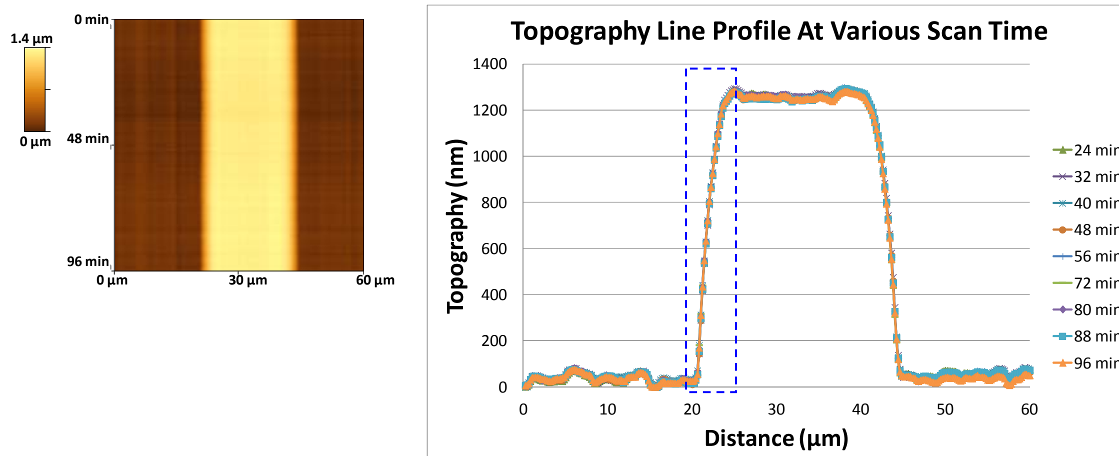


Figure 6.8 (a): 1D topography micrograph of measurement time vs distance along AA' in Fig. 6.3

Figure 6.8 (b): Line profiles at various measurement time

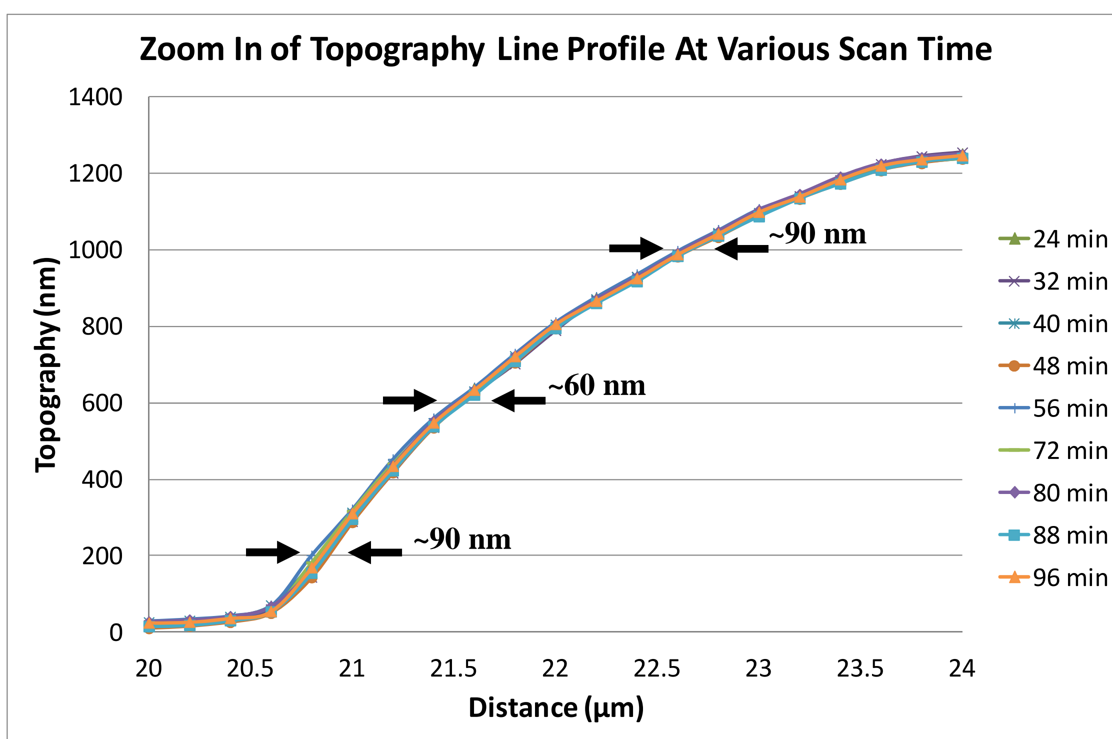


Figure 6.8 (c): Zoom in of Fig. 6.8 (b) along step profile between 20 and 24 µm

Figure 6.8 (a) shows the time vs distance micrograph of the step height being measured. From the topography micrograph in Fig. 6.8 (a) and the corresponding line profiles at various measurement times in Fig. 6.8 (b), it can be clearly observed that there is minimum positional drift occurring within one thermal acquisition set, even though the total acquisition time was extended to 96 min. Figure 6.8 (c) shows a zoom in view of the line profiles indicated in Fig. 6.8 (b) and estimated an average drift of 80 nm during the whole 96 min acquisition time.

6.3 Thermal Signal Recovery Where Temperature Drift Exists

This section explored various ways to recover the thermal signal where temperature drift is also coupled into the acquired signal. Various options are explored and it is determined that the algorithm of thermal signal "Normalization" is able to recover the temperature information from the noise introduced by the coupled temperature drift.

The sample used in this experiment is the commercially available CA3083 general purpose high current NPN transistor array. The unit is decapped and one of the BJT is used for investigation.

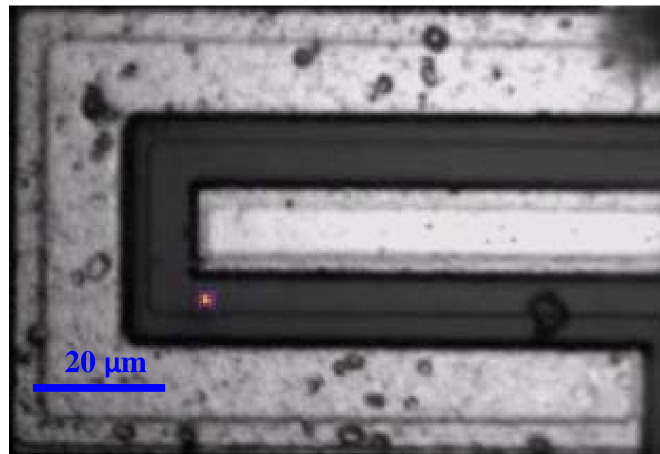


Figure 6.9: BJT with emission spot detected with a cooled CCD camera (PEM)

Figure 6.9 shows the defective BJT where an emission spot was detected with the PEM system. This unit was further investigated at the emission spot with the scanning near-field emission microscopy (SNPEM). The acquired micrographs at a PN junction reverse bias of 5.52V with 10 µA of leakage current are as shown in Fig. 6.10.

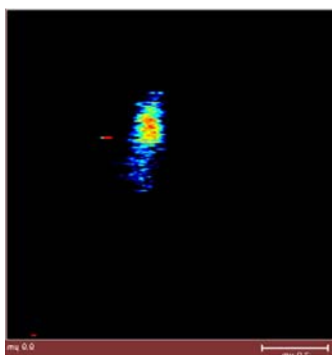


Figure 6.10 (a): SNPEM Micrograph

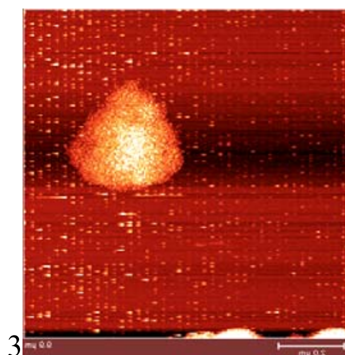


Figure 6.10 (b): Topography

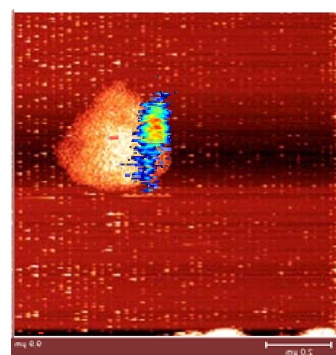


Figure 6.10 (c): Overlay of SNPEM with Topography

The presence of a localized emission spot suggests that the same location will experience a higher local temperature as well. Thus it is suitable to be used with the SLIA SThM. A topography micrograph of the same location is acquired with the thermal probe as shown in Fig. 6.11.

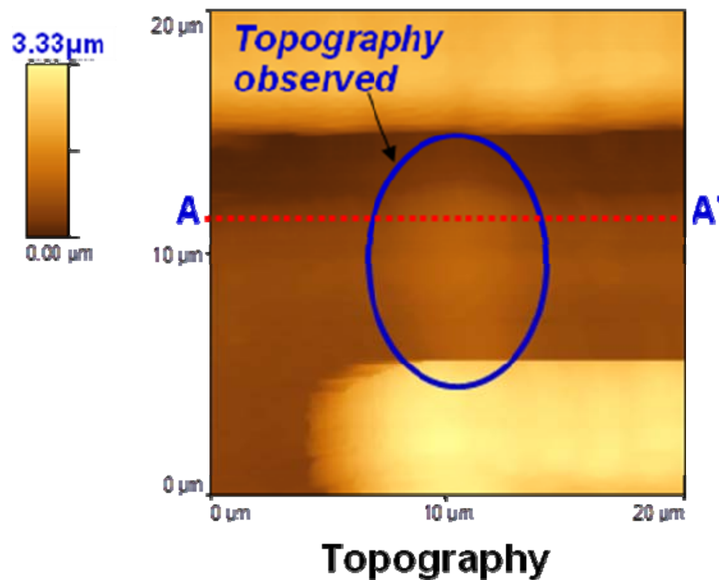


Figure 6.11: Topography of emission spot as acquired with thermal probe

Due to the larger size of the thermal probe compared to the probe used in SNPEM, the topography is not as sharp but appears more "spread out" with poorer spatial resolution. However, the defective location can still be identified from the topography micrograph captured with the thermal probe.

From this topography micrograph, a 1D line scan along AA' is performed to map the temperature around the protrusion region of the PN junction at various leakage currents. Figure 6.12 shows the topography and corresponding temperature profiles at various leakage current levels.

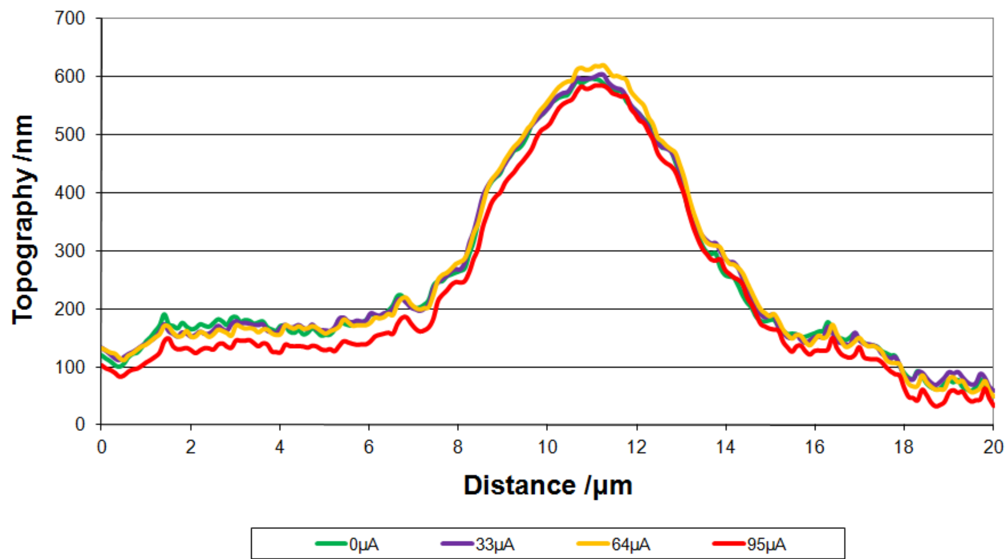


Figure 6.12 (a): Topography profiles of PN junction at various leakage current

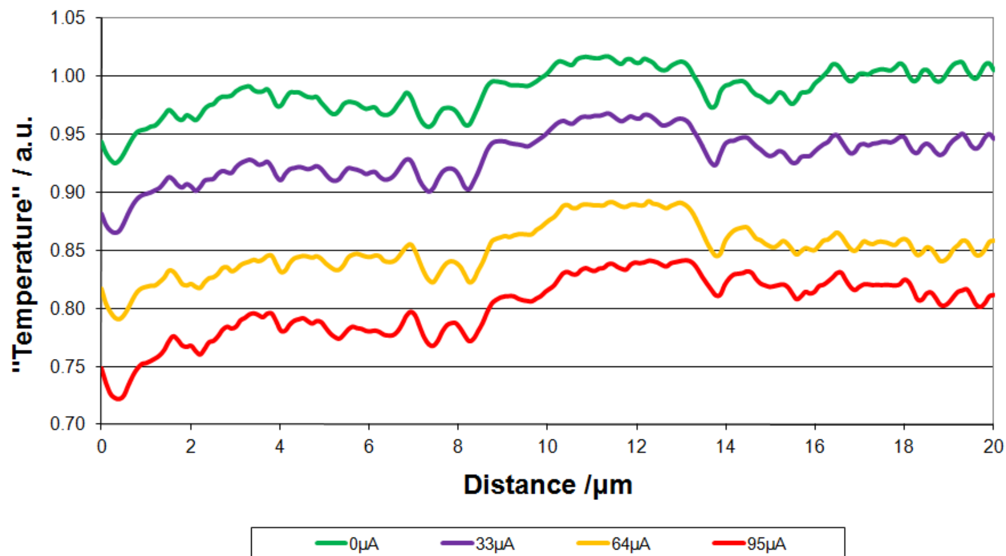


Figure 6.12 (b): Temperature profiles of PN junction at various leakage current

It can be clearly observed from the topography profiles (Fig. 6.12 (a)) that there is no significant shift in topography measurement over the various line scans. This shows that the DUT is secured properly and leveled with the scanning plane of the thermal probe. However, the temperature profiles in Fig. 6.12 (b) observed significant temperature drift during measurement. The temperature drift occurs during each line scan from left to right. This can be seen by the gradual increase in thermal signal obtained, even when the DUT is not biased as represented by the 0 μA line profile. The temperature line profile observed for 0 μA leakage current can be explained by the different contact area of the thermal probe across the DUT. Temperature drift also occurs across the different temperature profiles.

In order to isolate the temperature information around the emission spot from the coupled temperature drift occurring during thermal signal acquisition, various strategies are explored.

6.3.1 Temperature Leveling

One option is to implement some form of temperature leveling similar to what is usually done during topography leveling by software algorithm. In order for this to be done, there must be at least a point along the temperature line profile where it is reasonable to expect that there is no temperature change caused by the leakage current. If more locations along the profile can be assumed to have no temperature change, then the temperature leveling can be done with more confidence.

Figure 6.13 shows the two possible leveling algorithms.

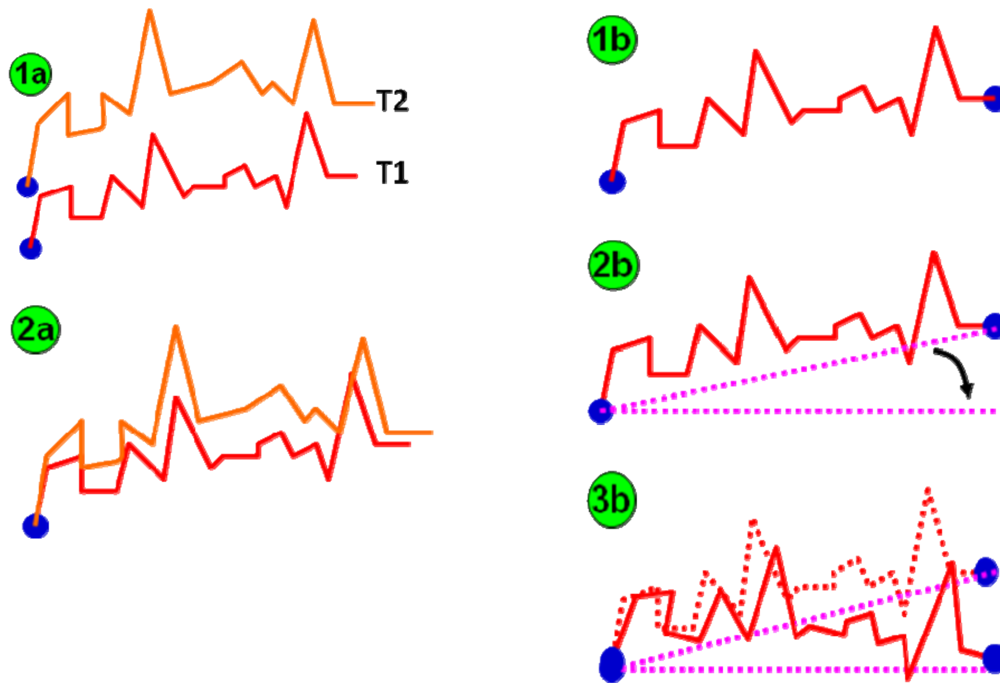


Figure 6.13 (a): 1 Point leveling algorithm   Figure 6.13 (b): 2 Points leveling algorithm

In 1 point leveling, a location along the temperature profile is identified to have no temperature change regardless of increasing DUT leakage current. This is indicated by the blue circle as shown in Fig. 6.13 (a) 1a. Once such a point can be identified and located, the 1 point leveling algorithm simply align this point in the two temperature profiles and temperature comparison between the two bias levels can be compared. Note however that this does not try to compensate for the temperature drift occurring within the line profile. This is demonstrated by the schematics in Fig. 6.13 (a) 2a where the temperature profiles still observe a gradual increase from left to right.

In 2 point leveling, as the name implies, two locations within the temperature line profiles have to be identified to have similar temperature as shown in Fig. 6.13 (b) 1b. Once this is achieved, a line equation is formed with these 2 points. The slope of this line equation represents the amount of drift within a line scan present in the temperature profile. It can also be due to the d.c. heating of the DUT during the line scan. The eventual temperature is achieved by leveling this line profile, effectively removing the temperature drift within the line scan as well (Fig. 6.13 (b) 3b).

Thus, 2 point leveling has the added benefit of removing temperature drift occurring within a temperature profile. This also means that theoretically, 2 point leveling is able to extract small local temperature variation even with large background d.c. heating and temperature drift.

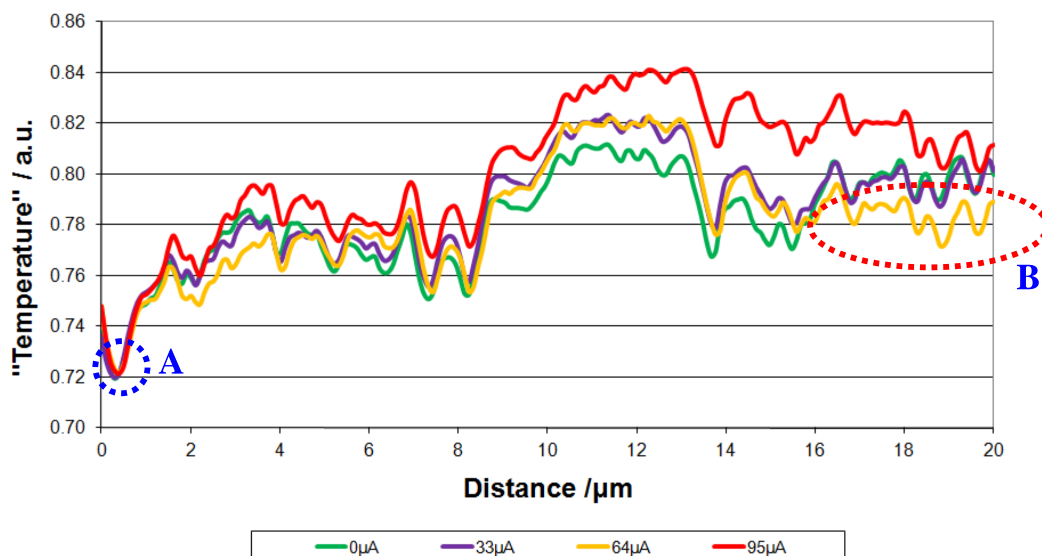


Figure 6.14 (a): 1 point leveling for temperature profiles at various leakage current

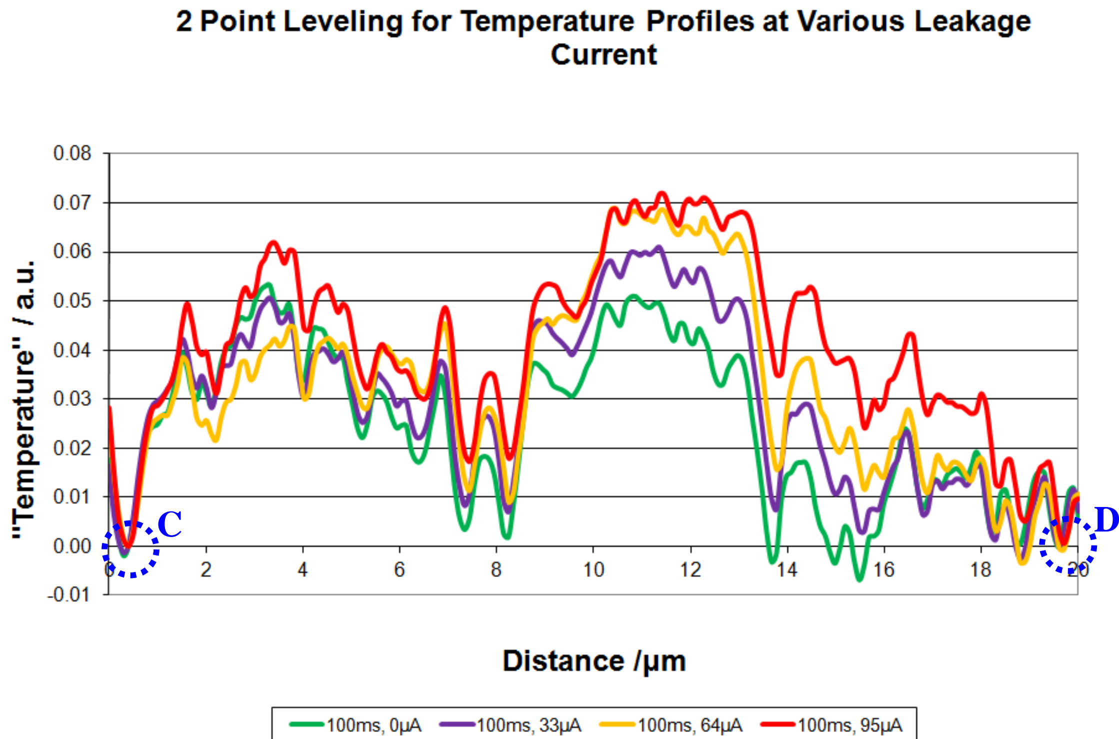


Figure 6.14 (b): 2 point leveling for temperature profiles at various leakage current

Figure 6.14 shows the temperature profiles of Fig. 6.12 (b) after temperatures leveling are done. In Fig. 6.14 (a) where 1 point leveling is done for location highlighted at A, it can be observe that in general, the higher the leakage current, the higher the temperature profile will rise as expected. However, there are some artifacts introduced such as the one highlighted at region B of Fig. 6.14 (a). It shows the temperature profile at a leakage current of 64 μA being the lowest among the various temperature profiles, even for the profile where DUT is not biased.

Figure 6.14 (b) shows the result of 2 point leveling algorithm as implemented for Fig. 6.12 (b). The two chosen points are near the ends of either side with assumption that they

should have the same temperature. The resultant temperature profiles obtained with 2 point leveling shows a more consistent increase in temperature measured with increasing leakage current. However, some artifacts as a consequence of the mathematical manipulation can still be observed such that the temperature profile for DUT without bias can be higher than the other profiles where the DUT is biased. Finally, temperature normalization is another algorithm that can be implemented to filter out unwanted noise signal that are coupled into the measurement.

6.3.2 Temperature Normalization

This algorithm makes use of the temperature profile obtained when the DUT is not biased. In the unbiased state, the temperature information obtained is the sum of the local thermal properties as well as any topography coupling effect due to different probe sample contact area. Therefore, by normalizing the temperature profiles obtained at various leakage currents (Fig. 6.12 (b)) over this unbiased temperature profile, the relative temperature variation between the various biasing conditions can be determined. This is plotted in Fig. 6.15.

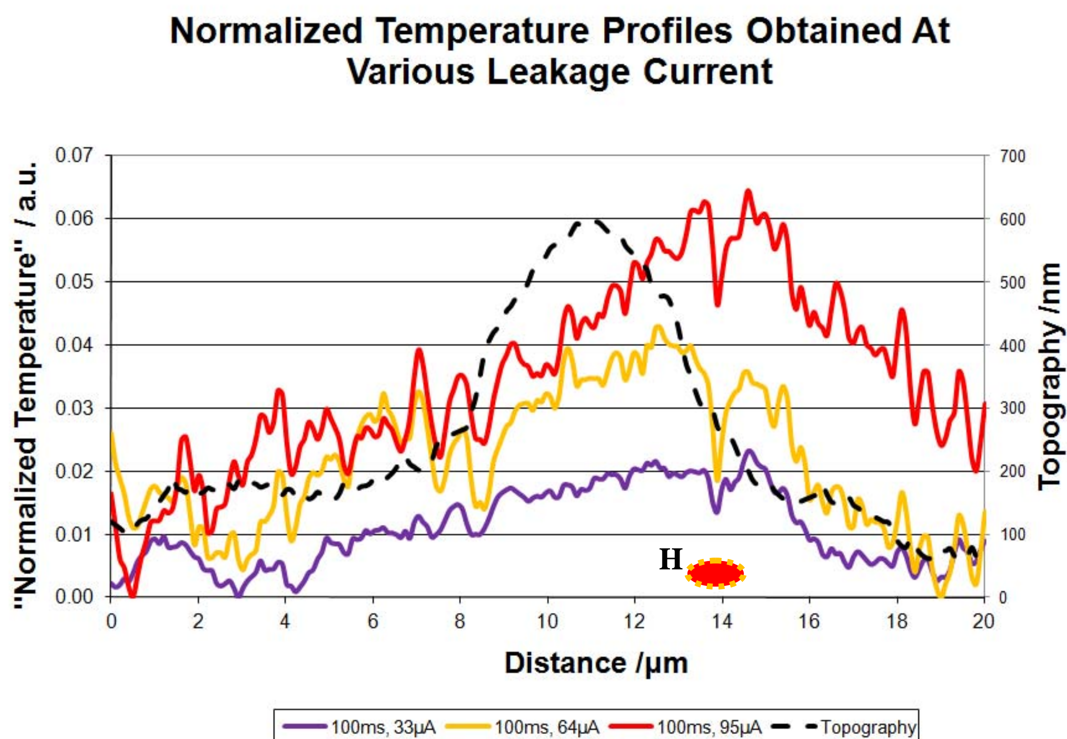


Figure 6.15: Normalized temperature profiles at various leakage current

From Fig. 6.15, it can be observed that the normalized temperature profiles look much different from those obtained purely by temperature leveling. It is more typical of temperature profiles where there is a localized hotspot as estimated at location H in Fig. 6.15. This localized hotspot is skewed to the right side of the topography feature. This estimated hotspot location coincides with the emission spot obtained by SNPEM which also appears on the right side of the topography feature as shown in Fig. 6.10 (c).

This shows that a more accurate depiction of the local temperature variation can be provided by normalizing with an unbiased temperature profile. The following chapter proceeds to discuss a modified setup that is able to achieve similar objective without the tedious and complicated data processing required after thermal signal acquisition.

Chapter 7: Double Lock-In Technique for SThM

This chapter begins with an introduction of the double lock-in setup for temperature measurement. This is followed by a discussion of the theoretical model and hypothesis for the DLIA technique. Some of the parameters such as the dwell time of the thermal probe, the lock-in amplifier's time constant (TC) filtering parameter, the stability of measurement and DUT biasing frequency are investigated to understand its influence on thermal measurement.

7.1 Double Lock-In Experimental Setup

The double lock-in experimental setup is shown in Fig. 7.1.

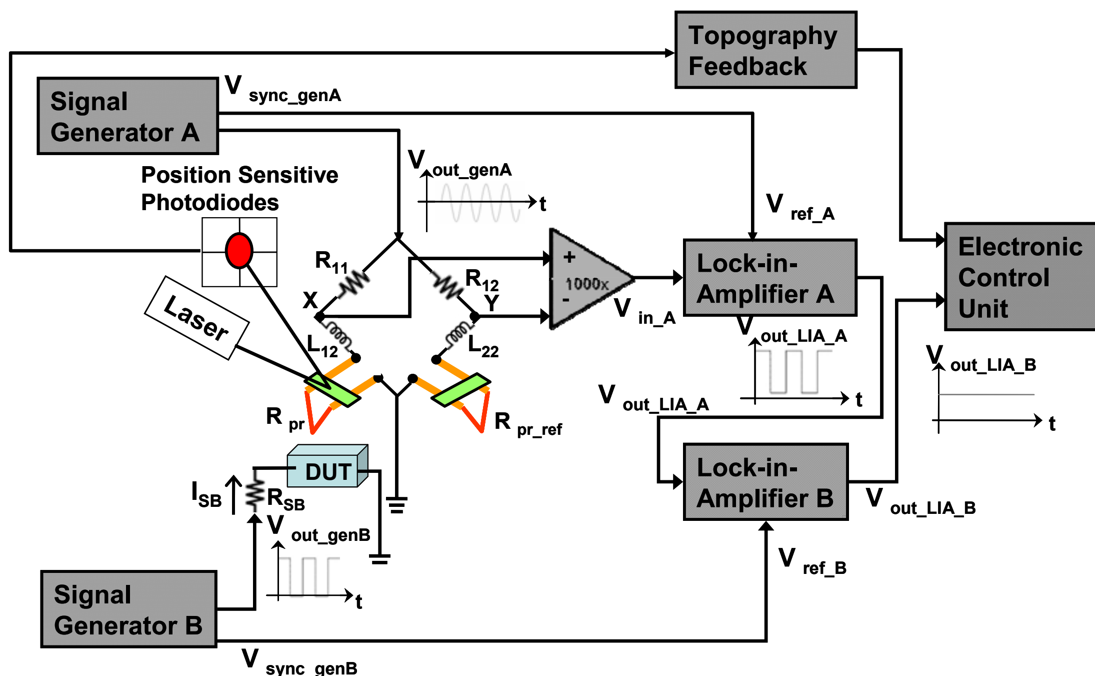


Figure 7.1: Double Lock-In Experimental Setup

The two main differences between the double lock-in setup with the single lock-in setup are:

i. The DUT is biased with a square wave unipolar current source instead of the typical sinusoidal current source. This square wave unipolar current source is also at a much lower (by ~3 orders) frequency than the Wheatstone bridge biasing frequency.

ii. A second lock-in amplifier (LIA_B) is introduced to take the output thermal signal of the first lock-in amplifier (LIA_A). This allows for the extraction of intentionally excited thermal signal response from the DUT.

In this setup, the Wheatstone bridge is biased at a very high frequency of 98.7 kHz similar to the single lock-in setup. LIA_A locks into this biasing frequency which serves as the sampling frequency for the biased DUT. The DUT itself is biased with a square wave unipolar current source as shown in Fig. 7.2 (a). The DUT biasing frequency is at least 3 orders lower than Wheatstone Bridge biasing frequency to fulfill the Nyquist condition and prevent aliasing, taking into account the non-ideal filters used. This allows the thermal probe, with a higher biasing frequency, at one arm of the Wheatstone Bridge to track changes in DUT thermal signal accurately. The DUT in turn heats up with temperature variation as shown in Fig. 7.2 (b). LIA_B locks into the lower DUT switching frequency so as to decouple and extract the effects of the heating due to the intentionally introduced thermal biasing.

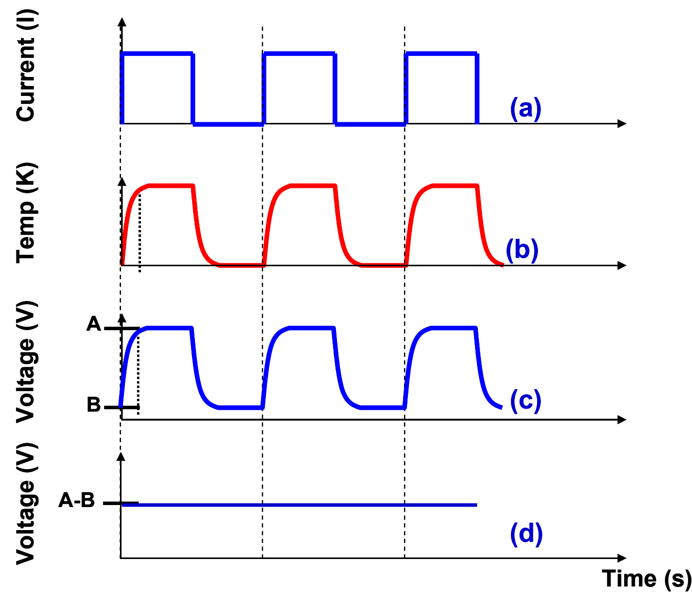


Figure 7.2: Illustration of thermal signal through two lock-in amplifiers: (a) Current Bias of DUT under unipolar biasing, (b) temperature of DUT due to unipolar biasing, (c) voltage output of LIA_A that is passed into LIA_B and (d) voltage output of LIA_B

The DUT switching frequency is chosen to ensure that the DUT is able to respond accordingly to the heating and cooling cycle provided by the unipolar biasing. For a DUT that heats up slowly as a result of a larger thermal time constant, a lower DUT biasing frequency is used. This biasing scheme is different from previous work done [122] where the DUT was biased with an AC voltage and the thermal wave generated at the 2nd harmonic was measured. In the existing setup, the static DUT temperatures at the two biasing levels provided by the square wave current source are measured by LIA_A. At each DUT biasing level, $V_{out_LIA_A}$ is the RMS DC voltage corresponding to the local DUT temperature. Thus, $V_{out_LIA_A}$ in Fig. 7.2 (c) acquires a similar waveform as that used for DUT biasing. If the biased DUT switching frequency is too fast for it to respond accordingly, the waveform at $V_{out_LIA_A}$ would appear very different to the initial DUT biasing waveform.

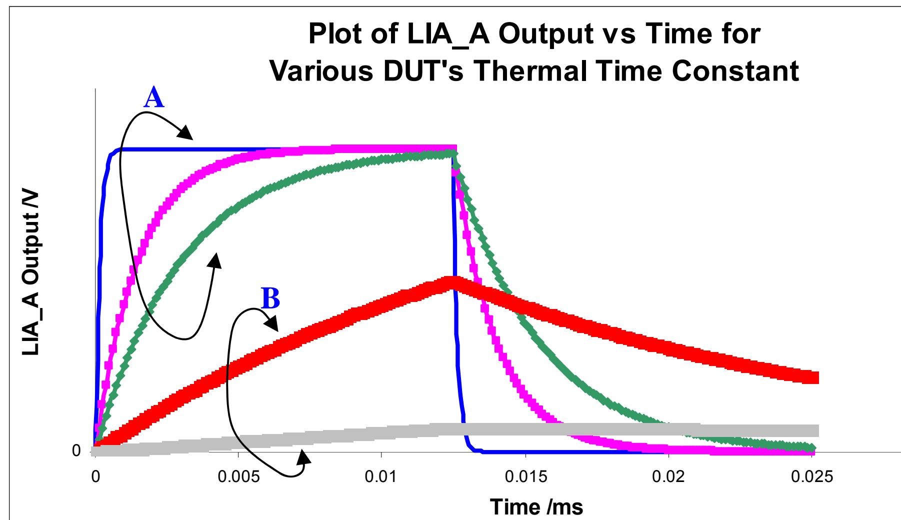


Figure 7.3: Illustration of LIA_A's Output vs Time at Various DUT's Thermal Time Constant for DUT Biasing Frequency of 40 Hz

Figure 7.3 shows two groups of waveform that can be achieved for a fixed DUT biasing frequency. If the LIA_A output is similar to group A, then the biasing frequency is acceptable. In this situation, LIA_A output which tracks the DUT heating, shows that the DUT has reached the maximum heating according to the biased condition. In group B, it is obvious that the DUT biasing is too fast for it to achieve maximum heating condition, thus reducing the potential thermal signal significantly.

When this occurs, the DUT biasing frequency has to be reduced to ensure accurate and reliable thermal measurement. Otherwise, the double lock-in result will be erroneous as it will be measuring the DUT temperature at different stages of DUT heating and cooling and not at the predetermined levels as provided for by the unipolar biasing. It is necessary for the DUT to reach its final heating temperature for a particular biased condition so as to extract the intended thermal information. A good sanity check would be for the output

waveform at $V_{out_LIA_A}$ to be similar to the DUT biasing waveform with similar rising and falling edges.

The amplitude of $V_{out_LIA_A}$ corresponds to the local DUT temperature difference between the two DUT biasing levels. This square wave output signal at DUT switching frequency is then sent into LIA_B which is locked in at the DUT biasing frequency. Since the lock-in amplifier is a narrow bandwidth filter, higher harmonics of the square wave input signal are effectively filtered out. The output of LIA_B, $V_{out_LIA_B}$ would be a signal that corresponds to the amplitude of its square wave input. This amplitude effectively means that LIA_B performs a “point-by-point thermal signal subtraction” at the two bias levels of the square wave. In order to achieve optimum LIA_B output, the thermal probe dwell time is fixed at multiples of the DUT switching period. This ensures that for the dwell duration of the probe, it is measuring equal amount of DUT heating and cooling cycle. Any difference in thermal measurement at different probe location is due to other factors such as distance away from heat source, local material properties rather than the point in time when thermal measurement is taken. This ensures that the thermal measurement is consistent and repeatable.

7.2 Double Lock-In Theoretical Treatment

The thermal model by J.S. Suehle [123] is used as it describes a first order system with one thermal time constant. For a purely resistive line subjected to periodic pulsed heating, the power *P(t)* dissipated is given by Eqn. 7.1 [124]:

$$P(t)dt = \alpha dT + \beta(T - T_s)dt \qquad \text{Eqn. (7.1)}$$

where T_s is the substrate temperature, α is the thermal capacitance (C_{th}) and 1/β the thermal resistance (R_{th}).

Letting t_p be the DUT biasing period, the particular solution for Eqn. 7.1 can be derived assuming the biasing condition of Fig. 7.2(a).

For $0 < t \le \frac{t_p}{2}$, the particular solution of Eqn. 7.1 with the boundary condition of $T = T_s$ when t = 0 is

$$e^{\frac{\beta}{\alpha}t}T(t) = \frac{P_0}{\beta}e^{\frac{\beta}{\alpha}t} + T_s e^{\frac{\beta}{\alpha}t} - \frac{P_0}{\beta}$$

$$T_1(t) = T_s + \frac{P_0}{\beta}(1 - e^{-\frac{\beta}{\alpha}t}) \qquad \text{Eqn. (7.2)}$$

where P_0 is the peak power value of the unipolar rectangular current bias as shown in Fig. 7.2 (a).

For $\frac{t_p}{2} \le t < t_p$, the general solution of Eqn 7.1 is

$$e^{\frac{\beta}{\alpha}t}T(t) = T_s e^{\frac{\beta}{\alpha}t} + D$$

$$T_2(t) = T_s + De^{-\frac{\beta}{\alpha}t} \qquad \text{Eqn. (7.3)}$$

where D is a constant.

The particular solution of Eqn. 7.3 with the boundary condition of $T_1(\frac{t_p}{2}) = T_2(\frac{t_p}{2})$ is

$$T_2(t) = T_s + \frac{P_0}{\beta}[e^{\frac{\beta}{\alpha}(\frac{t_p}{2}-t)} - e^{-\frac{\beta}{\alpha}t}]$$ Eqn. (7.4)

Eqn. 7.2 and 7.4 can be simplified further with the following definition [124].

- Sample thermal time constant, $\tau_{th} = \alpha / \beta = C_{th} \times R_{th}$
- DC joule heating of sample, $\Delta T_m = T_m - T_s = P_0 / \beta$

$$T_1(t) = T_s + \Delta T_m (1 - e^{-\frac{t}{\tau_{th}}}) \qquad \text{for } 0 < t \le \frac{t_p}{2}$$ Eqn. (7.2a)

$$T_2(t) = T_s + \Delta T_m [e^{\frac{1}{\tau_{th}}(\frac{t_p}{2}-t)} - e^{-\frac{t}{\tau_{th}}}] \qquad \text{for } \frac{t_p}{2} \le t < t_p$$ Eqn. (7.4a)

With an appropriate temperature model for the duration of the biasing period, t_p established, the voltage changes across the various stages of the double lock-in setup can be investigated.

From Eqn. 3.6, output voltage of the Wheatstone bridge Δv_0 is observed to be linearly proportional to the resistance change of the resistive probe $\Delta R_4(T)$. Furthermore, this resistance change is related to temperature change by the following relation:

$$\Delta R_4(T) = \alpha R_4(T_s) \Delta T(t)$$

$$R_4(T(t)) - R_4(T_s) = \alpha R_4(T_s)[T(t) - T_s]$$ Eqn. (7.5)

where $R_4(T_s)$ is the resistance of the resistive probe at the start of the experiment, α is the temperature coefficient of resistance of the Wollaston probe.

Eqn. 3.6 is thus expanded to include the sinusoidal form of v_i ($v_i = V_0 \sin\omega_1 t$, where ω_1 is the Wheatstone Bridge biasing frequency) and Eqn. (7.5).

$$\Delta v_0(t) = V_{in_A}(t) = \frac{v_i(R_3 + j\omega_1 L_3)}{[(R_3 + R_4) + j\omega_1(L_3 + L_4)]^2}\Delta R_4(T)$$

$$V_{in_A}(t) = E_1(V_0 \sin\omega_1 t)\alpha R_4(T_s)[T(t) - T_s] \qquad \text{Eqn. (7.6)}$$

where $E_1 = \dfrac{(R_3 + j\omega_1 L_3)}{[(R_3 + R_4) + j\omega_1(L_3 + L_4)]^2}$.

For the DUT biasing period $0 < t \le \frac{t_p}{2}$, using Eqn. 7.2a and 7.6, the input signal $V_{in_A}(t)$ before lock-in amplifier A in Fig. 7.1 can be expressed as follows.

$$V_{in_A}(t) = E_1(V_0 \sin\omega_1 t)\alpha R_4(T_s)[T_1(t) - T_s]$$

$$= E_1(V_0 \sin\omega_1 t)\alpha R_4(T_s)\Delta T_m(1 - e^{-\frac{t}{\tau_{th}}})$$

$$= E_1(V_0)\alpha R_4(T_s)\Delta T_m(1 - e^{-\frac{t}{\tau_{th}}})\sin\omega_1 t$$

$$= E_1 E_2 \Delta T_m(1 - e^{-\frac{t}{\tau_{th}}})\sin\omega_1 t,\ 0 < t \le \frac{t_p}{2} \qquad \text{Eqn. (7.7)}$$

where $E_2 = V_0 \alpha R_4(T_s)$.

Before proceeding further, it is appropriate to introduce the various functional blocks of a typical lock-in amplifier as shown in the schematic in Fig. 7.4.

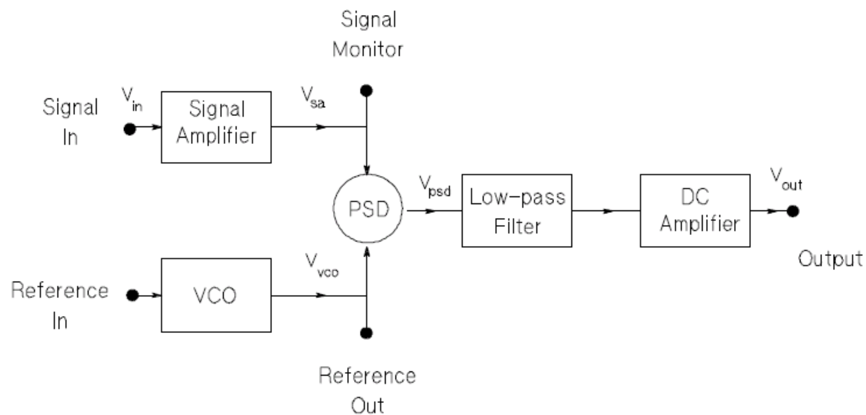


Figure 7.4: Lock-In Amplifier Schematic [125]

The input signal is passed into the signal amplifier with appropriate notch filters to remove noise introduced by the power lines. Reference signal is fed into the voltage-controlled oscillator (VCO) and these two signals are multiplied using a digital phase sensitive detector (PSD). The resultant output signal has frequency components that are sum and difference of the input and reference signal frequencies. One advantage of using a digital PSD over an analog one is very low harmonic content down to -120 dB. This ensures that the output of the PSD does not contain any unwanted frequency component. From the digital PSD output, the thermal signal passes through a low-pass filter. This allows for the filtering of higher frequency components from the output signal before being amplified with a DC amplifier. The cut off frequency of the low pass filter is determined by the time constant setting of the lock-in amplifier. Thus, only the initial signal locked in at reference frequency appears at the output as a DC signal.

The following treatment will be using reference voltage for LIA_A as $V_{ref_A} = \sin \omega_1 t$, which is at the same frequency as the Wheatstone Bridge biasing.

i. At the LIA's PSD output, V_{PSD_A}

$$V_{PSD_A}(t) = V_{ref_A} \times V_{in_A}(t)$$

$$= \sin\omega_1 t \times E_1 E_2 \Delta T_m (1 - e^{-\frac{t}{\tau_{th}}}) \sin\omega_1 t$$

$$= E_1 E_2 \Delta T_m (1 - e^{-\frac{t}{\tau_{th}}})[\frac{1}{2} - \frac{1}{2}\sin 2\omega_1 t],\ 0 < t \le \frac{t_p}{2}$$ Eqn. (7.8)

ii. At the output of the low-pass filter, assuming suitable time constant setting is chosen to filter off signal of higher harmonics and allowing only the DC component through,

Eqn. (7.9)

$$V_{LPF_A}(t) = \frac{1}{2} E_1 E_2 \Delta T_m (1 - e^{-\frac{t}{\tau_{th}}}),\ 0 < t \le \frac{t_p}{2}$$

For the subsequent DUT biasing period $\frac{t_p}{2} < t \le t_p$, using Eqn. 7.4a and 7.6, the input signal $V_{in_A}(t)$ before lock-in amplifier A in Fig. 7.1 can be expressed as follows

$$V_{in_A}(t) = E_1(V_0 \sin\omega_1 t)\alpha R_4(T_s)[T_2(t) - T_s]$$

$$= E_1 E_2 \Delta T_m [e^{\frac{1}{\tau_{th}}(\frac{t_p}{2} - t)} - e^{-\frac{t}{\tau_{th}}}]\sin\omega_1 t,\ \frac{t_p}{2} < t \le t_p$$ Eqn. (7.10)

i. At the LIA's PSD output, V_{PSD_A}

$$V_{PSD_A}(t) = V_{ref_A} \times V_{in_A}(t)$$

$$= \sin\omega_1 t \times E_1 E_2 \Delta T_m [e^{\frac{1}{\tau_{th}}(\frac{t_p}{2} - t)} - e^{-\frac{t}{\tau_{th}}}]\sin\omega_1 t$$

$$= E_1 E_2 \Delta T_m [e^{\frac{1}{\tau_{th}}(\frac{t_p}{2} - t)} - e^{-\frac{t}{\tau_{th}}}][\frac{1}{2} - \frac{1}{2}\sin 2\omega_1 t],\ \frac{t_p}{2} < t \le t_p$$ Eqn. (7.11)

ii. At the output of the low-pass filter,

$$V_{LPF_A}(t) = \frac{1}{2}E_1E_2\Delta T_m[e^{\frac{1}{\tau_{th}}(\frac{t_p}{2}-t)} - e^{-\frac{t}{\tau_{th}}}],\ \frac{t_p}{2} < t \le t_p$$ Eqn. (7.12)

Thus the LIA_A output can be summarized as follows:

$$V_{out_LIA_A}(t) = \begin{cases} V_{LPF_A}(t) = \frac{1}{2}E_1E_2\Delta T_m(1-e^{-\frac{t}{\tau_{th}}}),\ 0 < t \le \frac{t_p}{2} \\ V_{LPF_A}(t) = \frac{1}{2}E_1E_2\Delta T_m[e^{\frac{1}{\tau_{th}}(\frac{t_p}{2}-t)} - e^{-\frac{t}{\tau_{th}}}],\ \frac{t_p}{2} < t \le t_p \\ V_{out_LIA_A}(t) = V_{out_LIA_A}(t+nT) \end{cases}$$ Eqn. (7.13)

where n is an integer.

The output of LIA_A is a square wave as shown in Fig. 7.2 (c) and reproduced in Fig. 7.5 (a). An oscilloscope capture of the LIA_A output is presented in Fig. 7.5 (b).

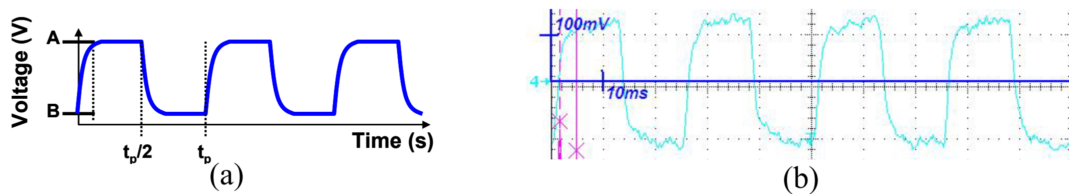


Figure 7.5: (a) LIA_A output with period t_p and (b) LIA_A output captured from an oscilloscope

This output signal, $V_{out_LIA_A}(t)$ can be approximated by the fourier series expansion as shown below.

$$f(t) = a_0 + \sum_{n=1}^{\infty}(a_n \cos n\omega t + b_n \sin n\omega t)$$

$$V_{out_LIA_A}(t) = a_0 + \sum_{n=1}^{\infty}(a_n \cos n\omega_p t + b_n \sin n\omega_p t) \qquad \text{Eqn. (7.14)}$$

where

$$a_0 = \frac{1}{t_p}\int_0^{t_p} V_{out_LIA_A}(t)dt$$

$$a_0 = \frac{1}{2t_p} E_1 E_2 \Delta T_m [\frac{t_p}{2} + t_{th} e^{t_p / t_{th}} - t_{th} e^{-t_p / 2t_{th}}]$$

$$a_n = \frac{1}{t_p}\int_0^{t_p} V_{out_LIA_A}(t)\cos(n\omega_p t)dt$$

$$b_n = \frac{1}{t_p}\int_0^{t_p} V_{out_LIA_A}(t)\sin(n\omega_p t)dt$$

Since LIA_B is locked into the biasing frequency, ω_p of the DUT, only this frequency at LIA_A output is considered while higher harmonics will be filtered out by the LPF of LIA_B.

Taking LIA_B reference frequency as $V_{ref_B} = \sin \omega_p t$ and considering only n=1 for Eqn. 7.14,

i. At LIA_B's PSD output

$$V_{PSD_B}(t) = V_{ref_B} \times V_{out_LIA_A}(t)$$
$$= \frac{1}{2}b_1 + \frac{1}{2}a_1 \sin(2\omega_p t) - \frac{1}{2}b_1 \cos(2\omega_p t) \quad \text{Eqn. 7.15}$$

ii. LIA_B output after LPF assuming effective filtering of all frequency components

$$V_{LPF_B}(t) = \frac{1}{2}b_1$$

$$= \frac{1}{8\pi} E_1 E_2 \Delta T_m [2 + \frac{\omega_p^2 t_{th}^2}{\omega_p^2 t_{th}^2 + 1}(e^{-t_p/t_{th}} - e^{-t_p/2t_{th}} - 2)] \quad \text{Eqn. 7.16}$$

where $\omega_p = 2\pi f_p = \frac{2\pi}{t_p}$.

7.3 Thermal Interpretation of Double Lock-In Scheme

In Fig. 7.2 (c), $V_{out_LIA_A}$ approximates a square wave with the two voltage levels corresponding to the local temperature of the DUT at each biasing state as explained from the single lock-in setup. Therefore, the amplitude of this square wave corresponds to the local temperature difference due to DUT biasing at the thermal probe location. The biasing scheme used is such that one of the DUT biasing level is at 0V as shown in Fig. 7.2 (a). Since there is a period when no DUT biasing occurs, it means that there is no heating of the DUT during this period. "Voltage level B" measured at $V_{out_LIA_A}$ is then due to factors other than DUT heating such as effective probe-DUT contact area (topography artifacts), temperature drift of the setup and the surface condition. "Voltage

level A" measured at $V_{out_LIA_A}$ will be due to a combination of DUT biasing as well as factors just mentioned.

$V_{out_LIA_A}$ is then sent into LIA_B which measures its amplitude and output an equivalent DC signal. Thus LIA_B measures the thermal difference at the two biasing conditions of the DUT. Factors due to topography influence and temperature drift of the setup, which are constant during the two DUT biasing states, are removed from $V_{out_LIA_B}$. This includes any noise introduced by the measurement environment such as thermal noise from the measuring equipment. The main contributing factor to $V_{out_LIA_B}$ that remains will be the local temperature difference as a result of the two DUT biasing states.

This allows the double lock-in setup to give an accurate temperature map of the biased DUT with significantly reduced topographic artifacts and ambient influence. Any long term system temperature drift is also reduced by the "subtraction" effect of LIA_B and restricted to the duration of the DUT biasing period.

7.4 Double Lock-In Characterization

This section examines the parameters which affects the double lock-in thermal measurement. These are the dwell time of the thermal probe during thermal scan, and the effect of time constant (TC) parameter for thermal signal filtering. The repeatability of the double lock-in measurement as well as temperature calibration are also discussed.

The sample used for characterization of the double lock-in system is the electromigration sample as shown in the following figure.

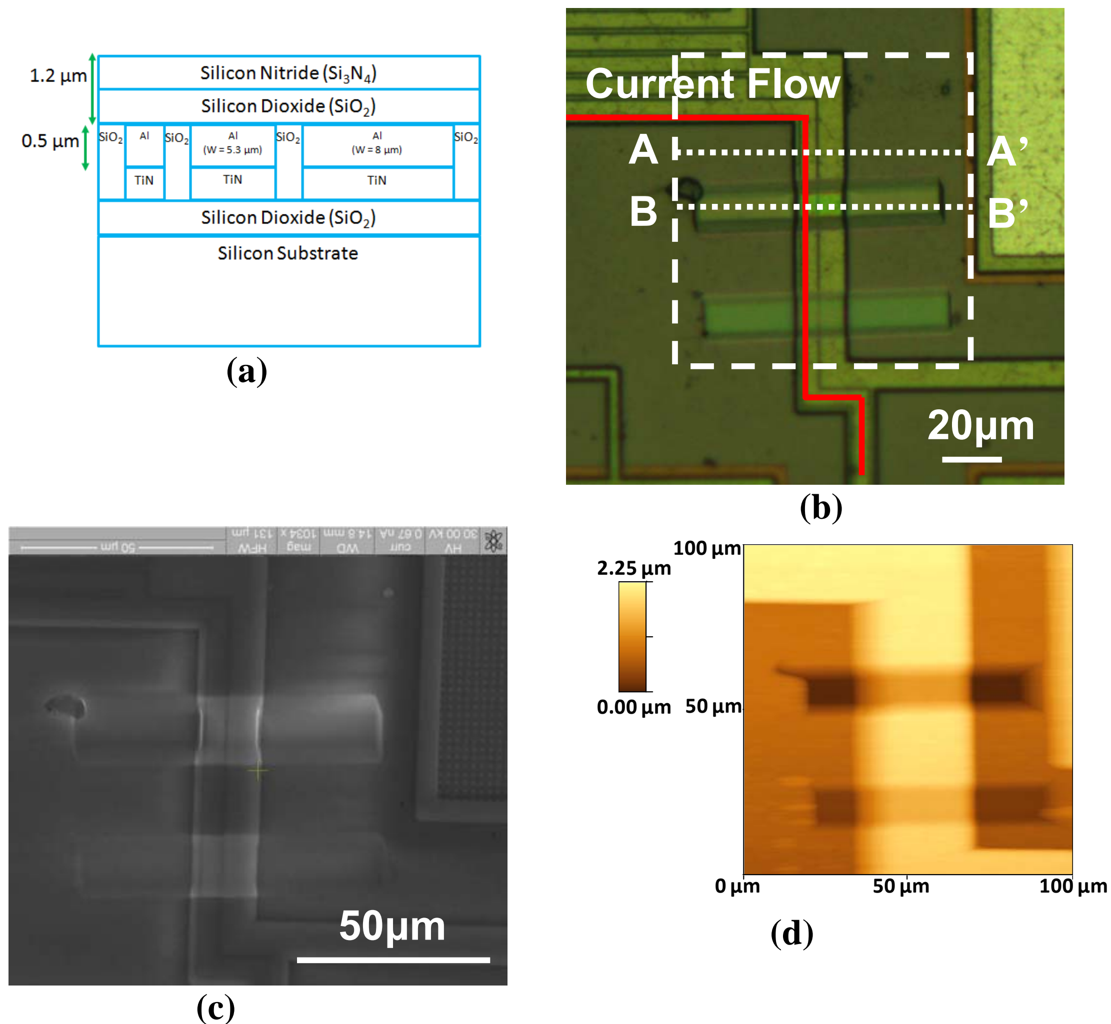


Figure 7.6: (a) Schematic of sample cross section (not FIB), (b) optical image of sample surface where biased interconnect and scanned location is indicated, (c) SEM top view of sample and (d) topography micrograph of scanned location

At the region of interest as indicated in Fig. 7.6 (b), there are 3 aluminium interconnects with width of 1 µm, 5.3 µm and 8 µm respectively. These interconnects have a thickness of 0.5 µm. There is also a passivation layer of 1.2 µm thick. The sample is designed such that a single interconnect line can be biased as shown in Fig. 7.6(b) or the whole comb interconnect structure can be biased where neighbouring biased interconnects are

separated by grounded interconnect. Further, the sample has various thickness of passivation removed by FIB as indicated by the two rectangular blocks and this will be discussed in more details subsequently. The corresponding SEM and topography micrographs are provided in Fig. 7.6 (c) and (d) respectively. It is important to note that due to the shape and size of the thermal probe, the topography appears wider and more convex than the actual sample.

7.4.1 Thermal Time Constant Extraction of DUT

Figure 7.5 (b) shows the thermal signal captured from the output of LIA_A. As discussed in the previous section, the thermal signal obtains a waveform similar to that used for biasing (Fig. 7.2 (a)) the interconnect. The waveform shows the exponential heating and cooling of the DUT throughout the biasing duration.

Using the waveform obtained together with the mathematical formulation derived in Eqn. 7.13, the thermal time constant of the DUT can be extracted. Figure 7.7 shows a plot of a period of the waveform captured as well as theoretical plots for various thermal time constant values.

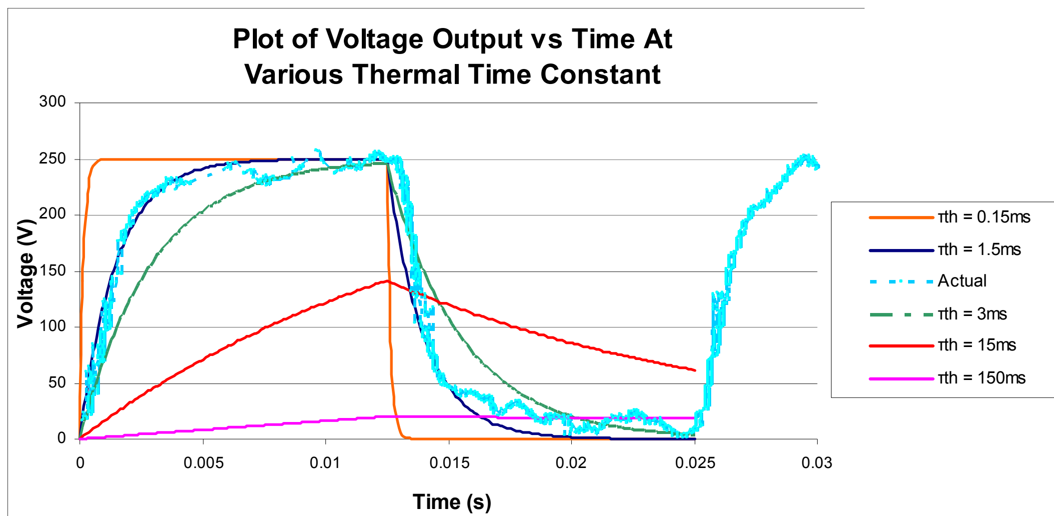


Figure 7.7: Plot of Voltage Output vs Time at Various DUT's Thermal Time Constant

The DUT thermal time constant of about 1.5 ms is extracted though fitting various values with respect to the actual waveform obtained.

7.4.2 Dwell Time of Thermal Probe

To investigate the effect of thermal probe dwell time on the acquired thermal measurement, a 1-directional (1D) line scan along BB' in Fig. 7.6 (b) is performed. This span across two interconnects where only one of them is biased as illustrated in Fig. 7.8.

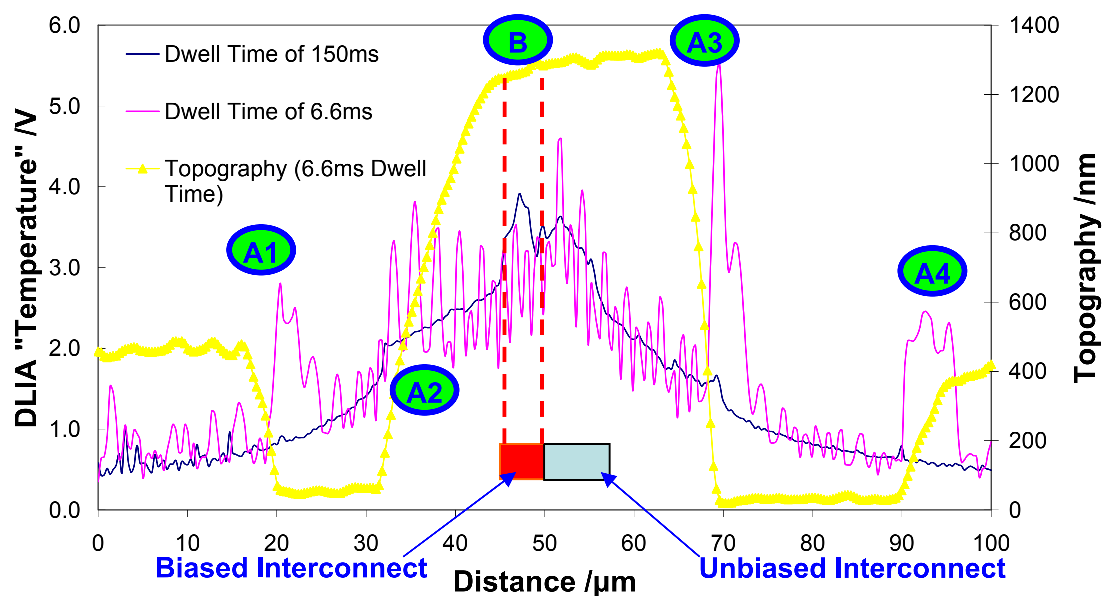


Figure 7.8: 1D thermal and topography line profile across a biased interconnect along BB' in Fig. 7.6 (b)

Figure 7.8 shows two thermal line profiles with different thermal probe dwell time overlaid with the topography line profile. The interconnect is biased at a frequency of 20 Hz or an equivalent period of 50 ms. One set of reading is obtained with a thermal probe dwell time well below this period at 6.6 ms while another set of reading is measured at a dwell time of 150 ms, 3 times longer than the biasing period.

For the short dwell time of 6.6 ms, the thermal signal obtained is very noisy compared to the thermal signal captured with dwell time of 150 ms. This is due to the probe moving to a different location before the interconnect can complete a heating cycle. This results in the DLIA setup not being able to determine the temperature change between the two biasing levels applied to the interconnect. There is also significant coupling of topography information in the thermal signal as can be observed at location A1, A2, A3

and A4 in Fig. 7.8. Whenever there is a step height variation, the thermal signal experiences a pronounced spike which is clearly not the expected measurement output. There are two consequences with scanning at a much faster rate than the DUT biasing frequency.

1) The thermal measurement includes temperature change due to topography variation rather than the heating effect of interest.

2) As the overall double lock-in system is effectively averaging measurement over the DUT biasing frequency, this results in loss of spatial resolution despite reducing overall measurement time.

For the thermal probe dwell time of 150 ms, which is 3 times the interconnect heating cycle, the thermal signal obtained is much cleaner without any obvious topography coupling. The thermal information obtained is free from any topographic artifacts. This is a more accurate representation of the heating effect being studied. It is able to pick up the biased interconnect from the unbiased one as observed by the peak at location B in Fig. 7.8.

This shows that an appropriate thermal probe dwell time that is multiple of the DUT heating cycle is essential to providing an accurate thermal profile of the heating situation being characterized. This also ensures minimum coupling of topography information, providing a more accurate representation of the actual DUT thermal condition.

7.4.3 Effect of LIA Time Constant (TC) Parameter

This section studies the effect of lock-in amplifier's time constant on the thermal signal acquired. For this study, the thermal probe is placed by means of the AFM onto the biased interconnect while the output of LIA_B is monitored under various TC settings. The interconnect is biased with a unipolar current source with wave form similar to Fig. 7.2 (a) at a frequency of 40 Hz.

Figure 7.9 shows the LIA_B's output signal and its respective spectrum obtained under various LIA_B's TC.

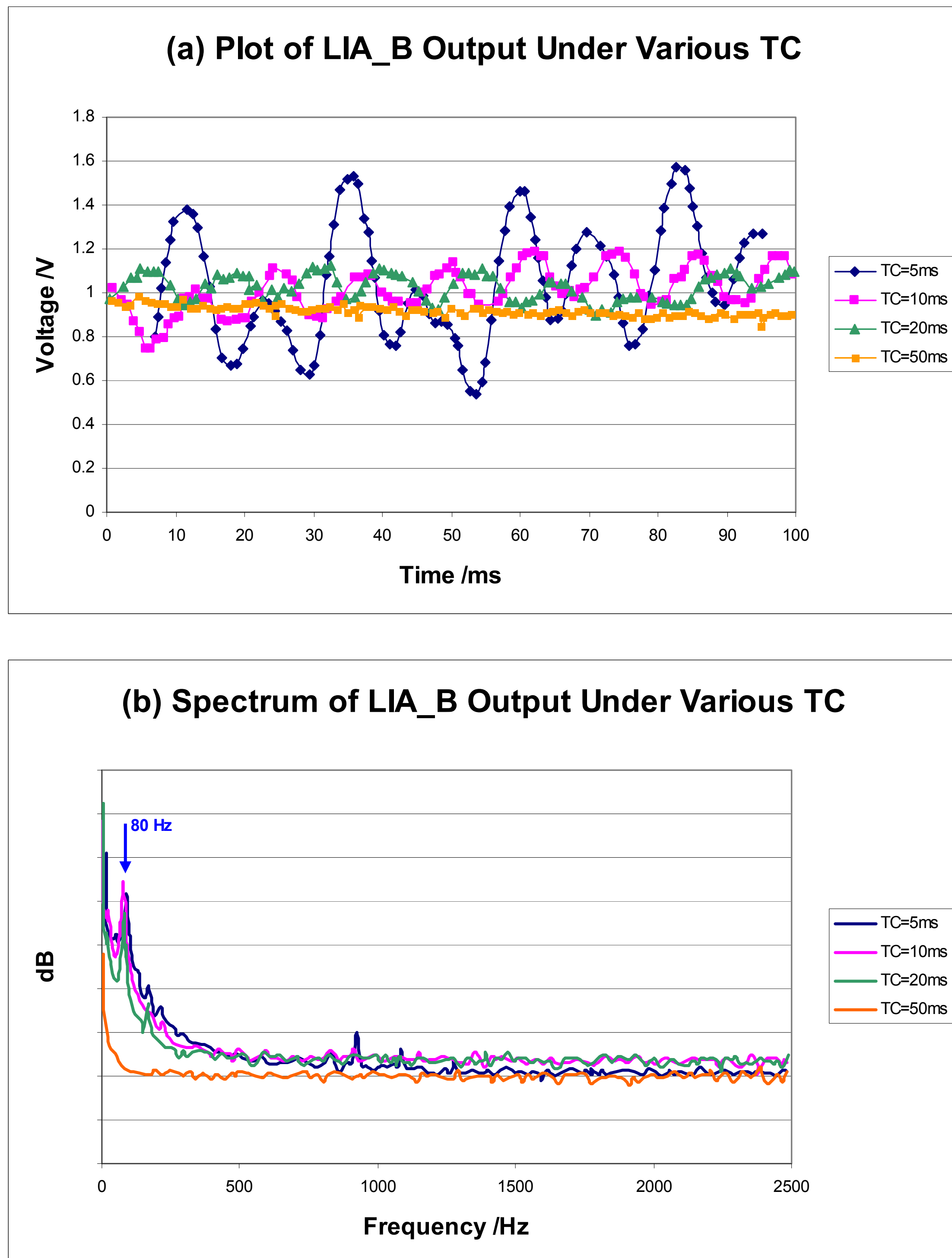


Figure 7.9: (a) Thermal Signal at The Output of LIA_B at Various TC and (b) its Equivalent Spectrum

From the voltage signal captured in Fig. 7.9 (a), it can be observed that at small TC such as 5 ms, the output is oscillatory in nature instead of equivalent to the DC signal as expected. From its corresponding spectrum in Fig. 7.9 (b), it can be observed that this is due to the presence of the 2nd harmonic signal at 80 Hz. Thus the contribution to the voltage oscillation is due to ineffective filtering of the 2nd harmonic component after LIA_B's PSD unit. At a TC of 50 ms, the voltage output is relatively flat as expected and no 80 Hz component or even higher harmonics can be observed from the spectrum captured.

To further quantify the signal obtained, the signal-to-noise ratio (SNR) is calculated and extrapolated. Here, the SNR is defined as the ratio of the signal mean over its standard deviation. At 50 ms where all higher harmonics signal are totally filtered off, the SNR achieved is about 40. The plot of SNR vs t_p/TC is created as shown in Fig. 7.10. From the plot, it can be calculated that a t_p/TC ratio of at most 10.6 is required in order to have a SNR of more than 2.

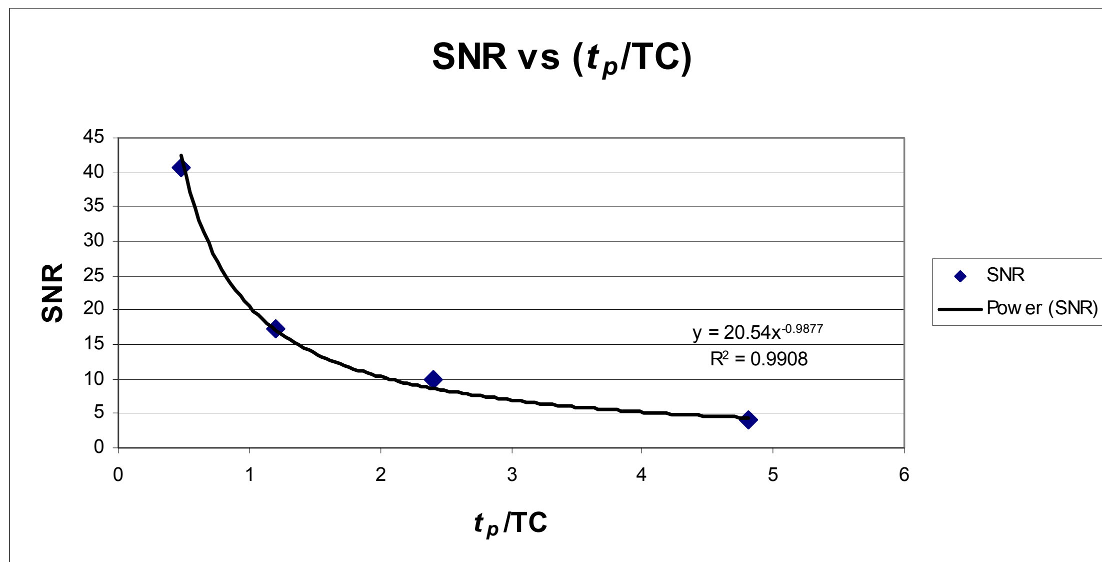


Figure 7.10: Plot of SNR vs ratio of (t_p/TC)

Also, the output of the filter used in the lock-in amplifier usually takes about 5 TC to stabilize. Since there are two lock-in used, it is necessary to ensure that the TC of LIA_B should be at least 5 TC of LIA_A's TC. Figure 7.11 shows two sets of thermal signal captured for different ratio of LIA_B to LIA_A's TC.

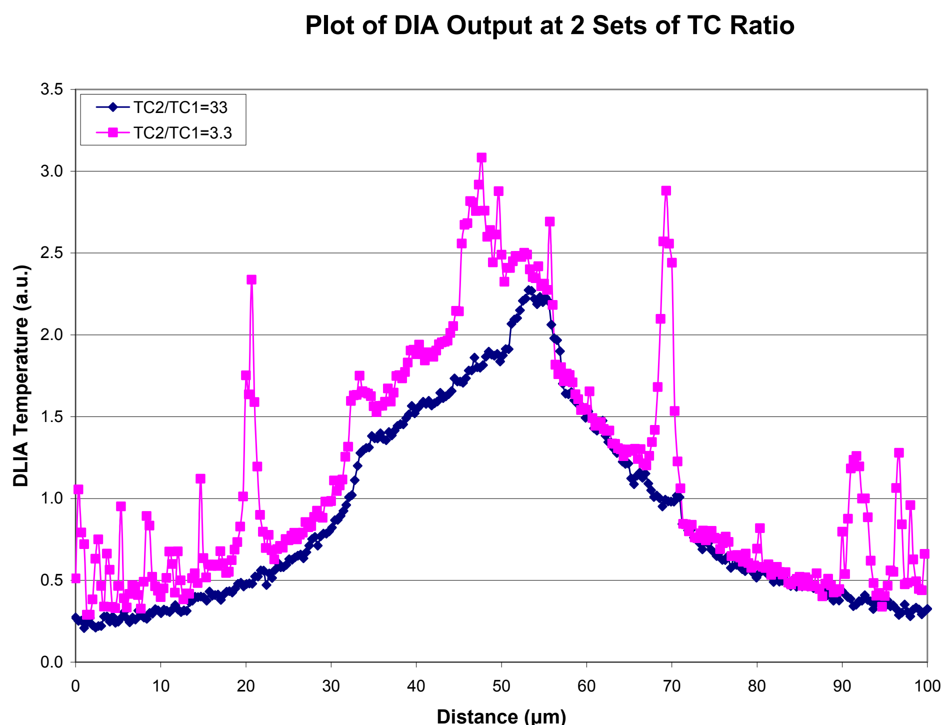


Figure 7.11: Plot of DLIA Output at Various Sets of TC Ratio

It is observed that when the ratio of LIA_B to LIA_A TC used is around 3.3, which is less than the desired ratio of 5, there are random signal spikes making the thermal measurement very noisy and unstable. These signal spikes are especially prominent whenever there is presence of some topography variation. This is due to insufficient settling time allowed at the output of LIA_A. Thus before the output signal at LIA_A is able to reach a steady state, LIA_B begins to process this output signal. If the thermal probe scan rate is slow, this will not be an issue. However, since the DLIA system has to be optimized to complete thermal measurement within the shortest possible time for the already slow raster scanning process, LIA_B will be averaging signals over two different probe locations. As different surface profiles are encountered, the initial large change in thermal signal encountered by the thermal probe is translated into noisy spikes at the

DLIA output, matching closely the topography profile obtained. In the situation where sufficient TC ratio is catered for, the thermal signal obtained is much more stable and without those noisy spikes.

7.4.4 Repeatability of Double Lock-In Result

The repeatability of the DLIA measurement system is quantified by repeating the thermal measurement on separate occasion.

Using the same electromigration sample as shown in Fig. 7.6, a series of 125 Hz unipolar currents at various biasing levels is applied while thermal measurement is performed. Since the measurement is performed on separate occasion, best possible effort is done to ensure the exact same location is selected so that direct overlay of the two thermal signals can be carried out.

The line profiles in the following figure are thermal measurements obtained with a 125 Hz current at 1 mA, 10 mA and 20 mA respectively.

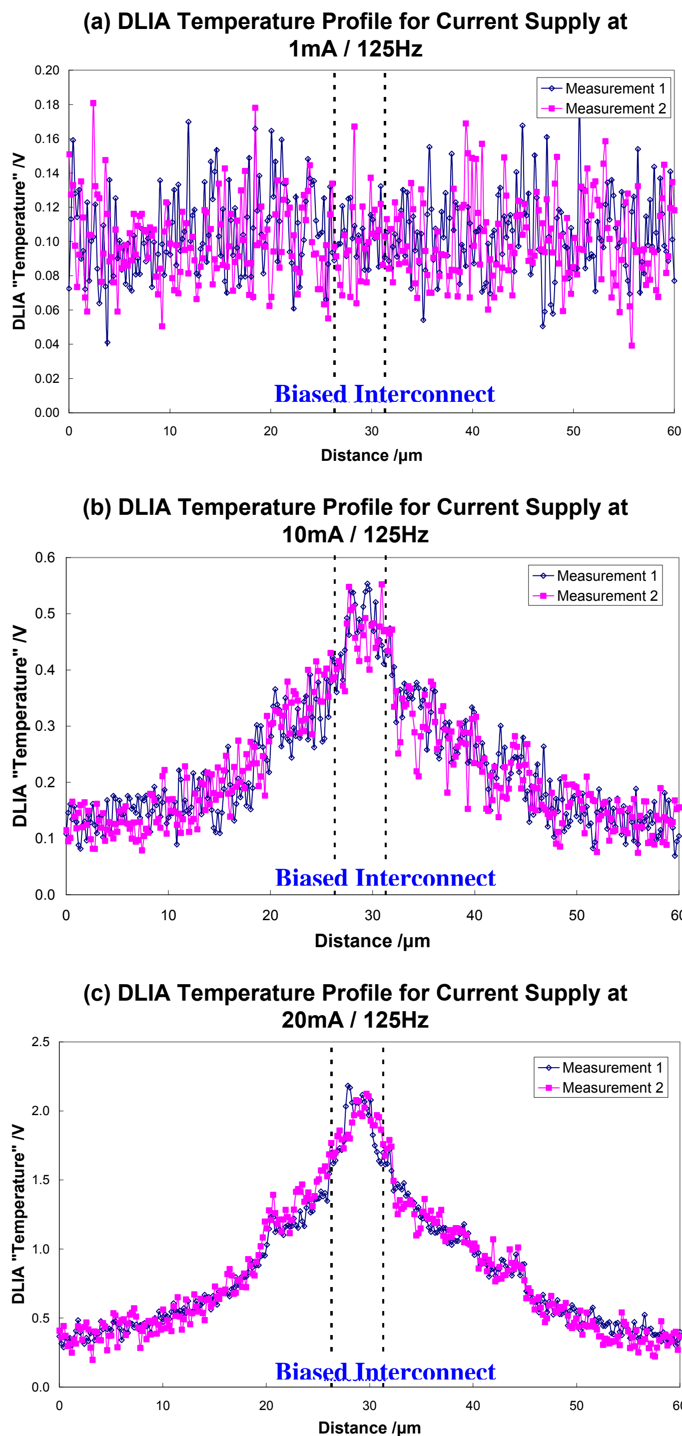


Figure 7.12: Thermal Line Profiles Across a 125 Hz Biased Interconnect for Two Separate Measurements on different days at (a) 1 mA, (b) 10 mA and (c) 20 mA

For a current bias of 1 mA in Fig. 7.12 (a), the thermal signal generated is too small to be measurable. Whatever signal output observed is essentially due to the presence of electronic and systematic noise. Using this as the basis for the minimum noise level in the DLIA setup, the Signal-to-Noise (SNR) can be determined. This SNR is determined by taking the square of the ratio of RMS amplitude of signal over noise. The result is summarized in the following table.

Table 7.1: RMS and SNR of the Thermal Signal Measured

		Noise Level @ 1mA Supply	10 mA Supply	20 mA Supply	Ratio of RMS_Sig_{20mA} / RMS_Sig_{10mA}
RMS of selected signal (between 26.3 to 31.3 µm)	Mmt 1 /V	0.102	0.47	1.882	4.00
	Mmt 2 /V	0.103	0.453	1.891	4.17
	Difference /mV	1	17	9	
SNR	Mmt 1 /V		21.2	340	
	Mmt 2 /V		19.3	337	

From the average of the 2 sets of RMS signal of biased interconnect, a measurement delta of about 13 mV is obtained. When the current supply is increased to 20mA, the SNR is observed to increase significantly as expected. It is also observed that when the current supply is doubled, the ratio of their RMS thermal signal turns out to be a factor of 4. This is in total agreement with the power law of $P \propto I^2$, demonstrating the direct correlation of the RMS signal with the heating situation experienced by the interconnect.

Thus measurement repeatability down to a delta of 13mV is demonstrated with the DLIA setup. The thermal signal captured is also in agreement with the power law.

7.4.5 Effect of DUT Biasing Frequency on Double Lock-In Thermal Signal

With a known DUT thermal time constant, it is most desirable to find out the fastest DUT biasing frequency and yet, which can still allow the DUT to heat up to a stable level for an accurate thermal analysis. A faster DUT biasing frequency means overall reduction of the thermal signal capture time.

Various thermal line profiles across the biased interconnect are plotted for various DUT biasing frequencies and shown in Fig. 7.13.

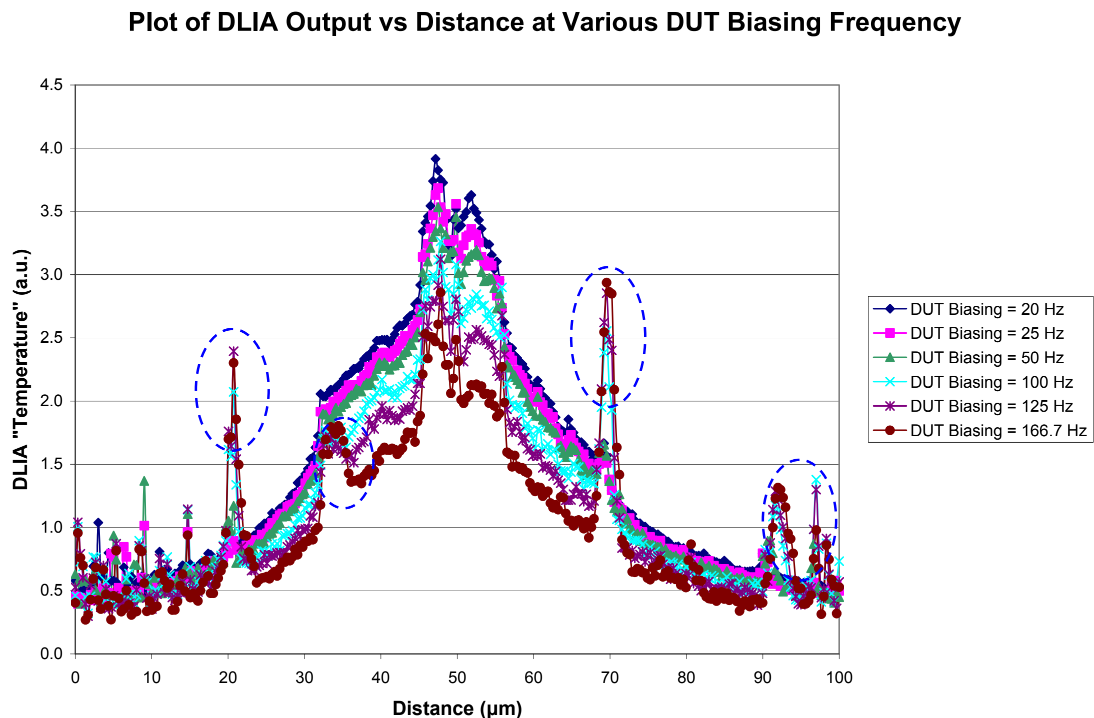


Figure 7.13: Thermal Line Profile Plots at Various DUT Biasing Frequency

From Fig. 7.13, two observations can be made. Firstly, the peak of the thermal signal is observed to be decreasing with increasing DUT biasing frequencies. Secondly, there seems to be more topographic artifacts coupled into the thermal signal at increased DUT biasing frequencies from 100 Hz and beyond as highlighted by the four dotted ovals.

A clearer picture of why this occurs can be understood from the theoretical formulation in Eqn. 7.16. A plot of Eqn. 7.16 for various thermal time constant is shown in Fig. 7.14.

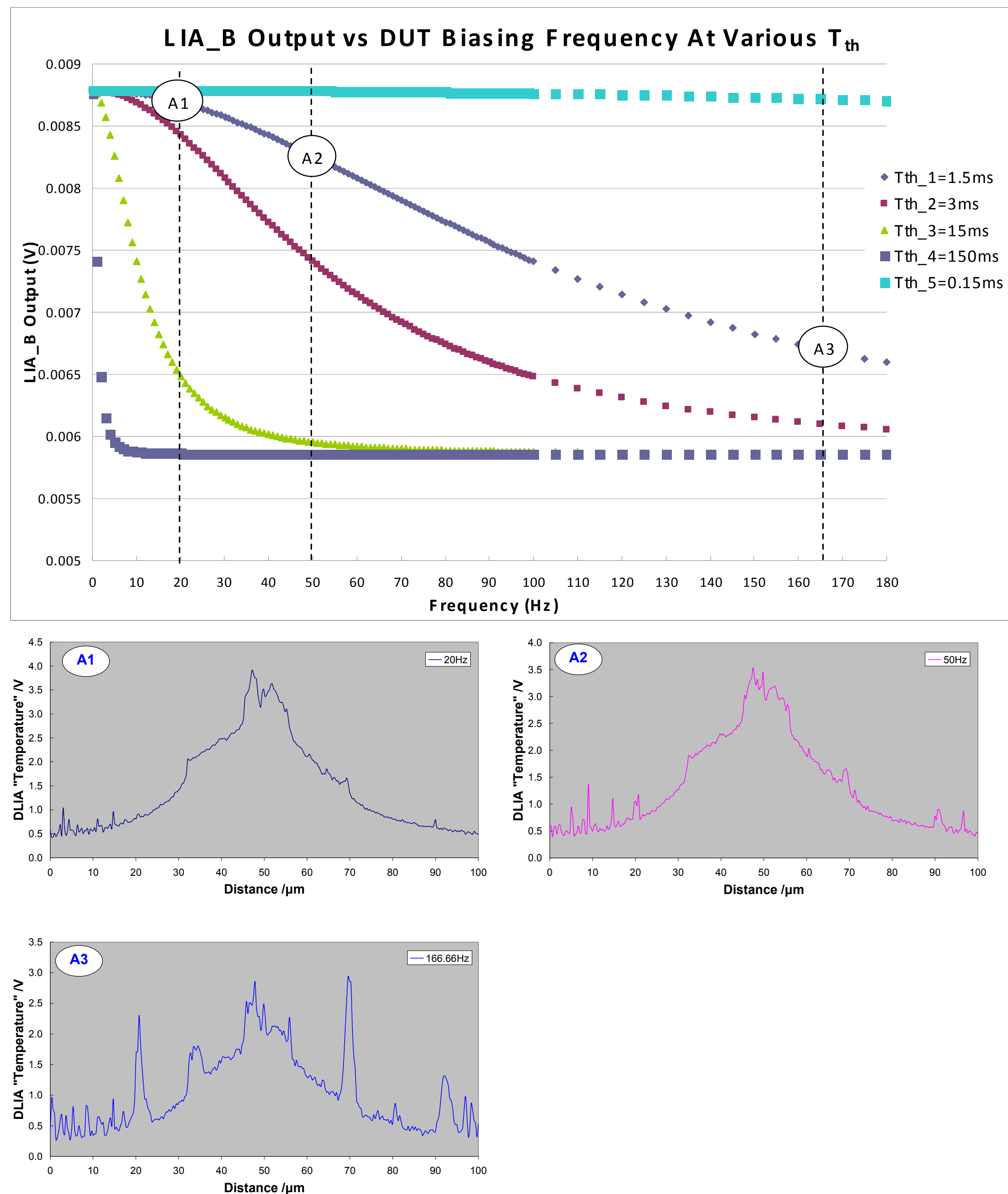


Figure 7.14: Plot of LIA_B Output vs DUT Biasing Frequencies and Selected Thermal Line Profile at various DUT Biasing Frequencies

From the plot in Fig. 7.14, it can be clearly observed that the LIA_B output signal decreases with increasing DUT biasing frequencies. Furthermore, the rate at which the

LIA_B thermal signal output drops with frequency also depends on the DUT thermal time constant. The thermal signal drop is more drastic with larger thermal time constant. Looking at the thermal line profile of A3 vs A1, it is easy to understand that with increasing DUT biasing frequency and decreasing thermal output, topographic artifacts start to overwhelm and be coupled into the thermal signal.

A plot of LIA_B output vs ratio of DUT biasing period over DUT thermal time constant is shown in the following figure.

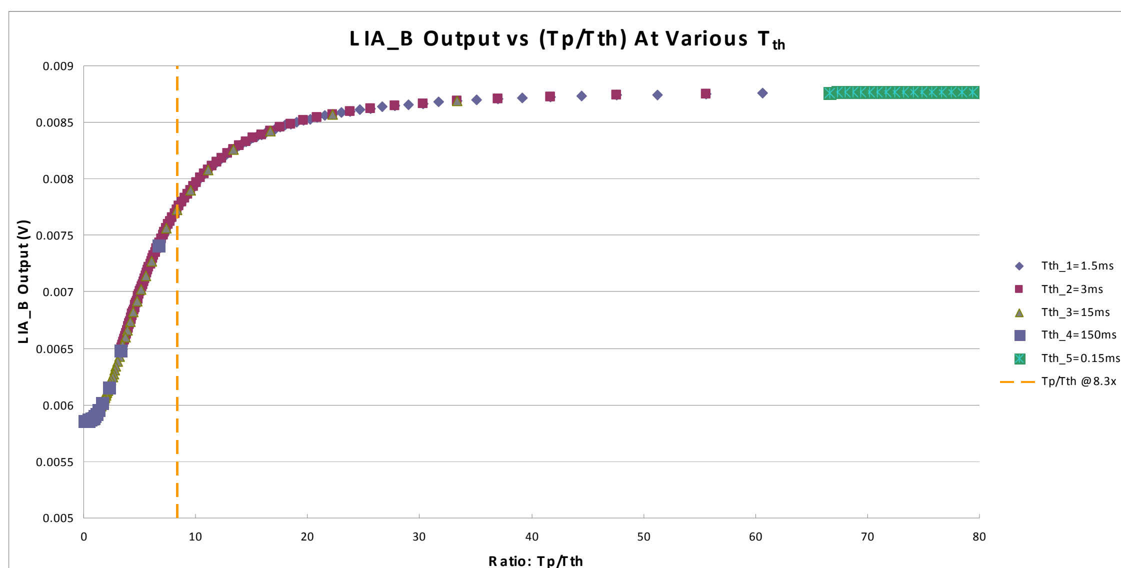


Figure 7.15: Thermal Line Profile Plots vs Ratio of DUT Biasing Period Over Thermal Time Constant

From the plot, it can be found that the LIA_B thermal signal output is reduced by a factor of *e* at a biasing period over thermal time constant ratio of 8.3. For instance, thermal profile at A3 in Fig. 7.14 has a ratio of 4. This means that the thermal signal is reduced drastically such that topographic-induced artifact signals overwhelm the thermal signal being measured.

7.5 Summary

A theoretical model with the fundamental concept of on-the-fly “point-by-point thermal signal subtraction” is discussed. A mathematical model is also developed to explain for the exponential heating and cooling observed.

The DLIA setup has been used to extract the thermal time constant of the DUT of ~ 1.5ms by means of curve fitting. Other aspects of the setup parameters include the requirement for dwell time of the thermal probe that is multiple of the DUT heating cycle. The effect of the choice of time constant for the two lock-in amplifiers is discussed and it is desirable for the ratio of LIA_B vs LIA_A TC to be more than 5. The stability and robustness of the DLIA setup are also investigated with a repeatability delta of 13 mV demonstrated.

The effect of decreasing thermal signal with increasing DUT biasing frequency has also been discussed. In the worst case scenario at higher biasing frequency, the thermal signal may be reduced to such extend that topography artifacts are coupled with it.

Chapter 8: Double Lock-In Technique Application

The previous chapter discusses the theory, mathematical formulation and some considerations for the parameters and constraints required for proper application of the double lock-in technique. This chapter shall proceed to apply the technique with an in-depth study of the electromigration sample previously mentioned in Fig. 7.6.

8.1 Effect of Varying DUT Heating Current

This section compares and studies the sensitivity of the double lock-in measurement with respect to single lock-in setup for a DUT under various heating current. A portion of the DUT where two interconnect lines lay next to each other as shown in Fig. 7.6 (b) is identified for investigation. Only one of the interconnect is biased. The two lines are indistinguishable in the topography measurement as they are capped by a layer of passivation. Any difference in thermal measurement is due to thermal influence of the interconnect line that is biased.

Figure 8.1 shows the topography and thermal micrographs for both measurement setup where one of the interconnect is biased using a current source. Measurement is taken by repeatedly scanning the same line location, AA’ in Fig. 7.6 (b) over time. In the single lock-in setup, a DC supply is used with increasing current level from 1mA to 50mA. For double lock-in setup, a unipolar square heat source at 125 Hz is used instead with peak current level increasing from 1mA to 50mA. Effective interconnect heating will be higher for the DC biased condition used in the single lock-in setup.

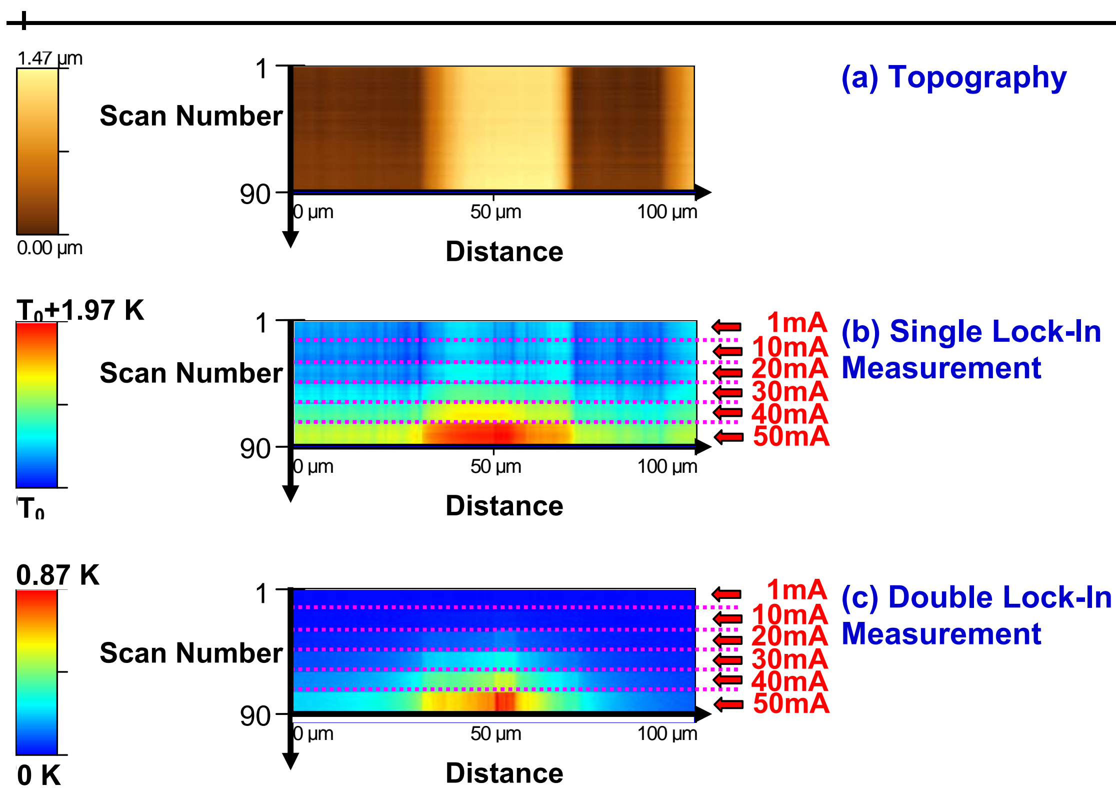


Figure 8.1: 1-Dimensional Micrographs for (a) Topography, (b) Single Lock-In Thermal and (c) Double Lock-In Micrograph of DUT at Various Heating Current

Figure 8.2 shows the corresponding line profile (AA') obtained at various bias levels from both set of thermal measurement setups.

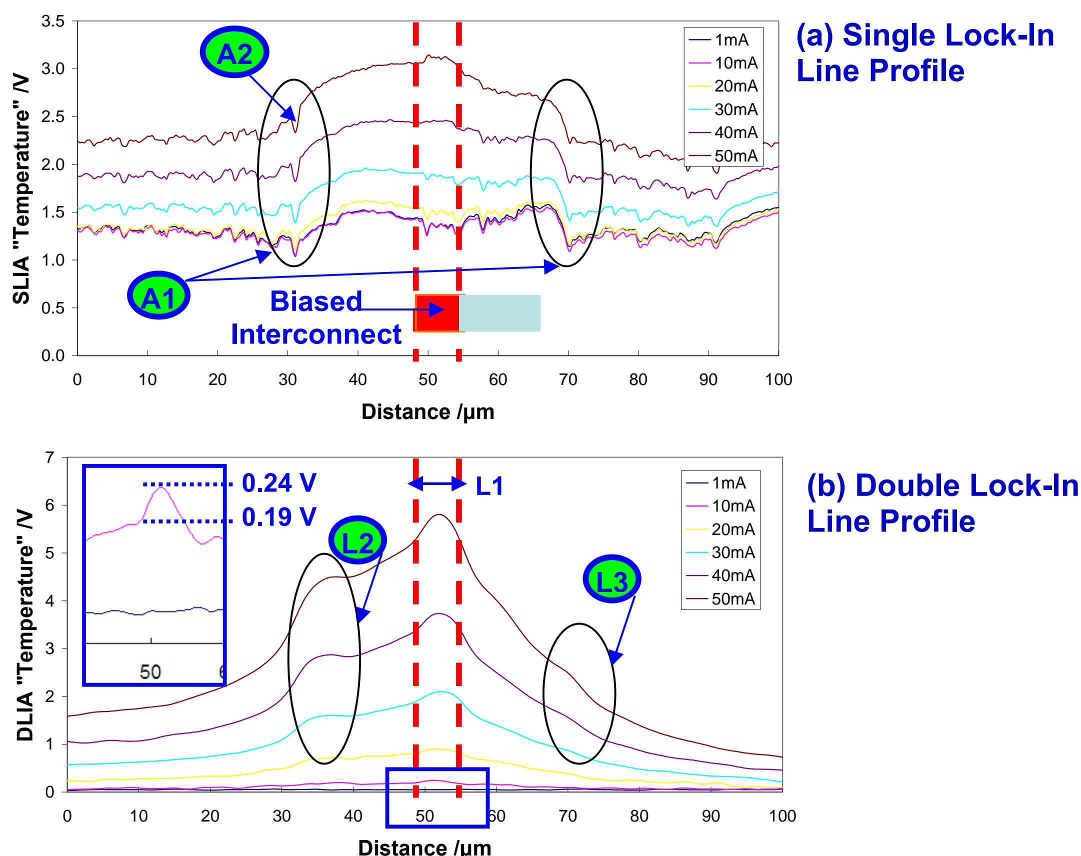


Figure 8.2: Thermal Line Profiles Obtained from (a) Single and (b) Double Lock-In Measurement under Various Heating Current

In Fig. 8.1 (a), it is observed that the topography is relatively flat over the two interconnects. From the thermal signal in the single lock-in setup (Fig. 8.1 (b)), the biased interconnect is indistinguishable from the unbiased interconnect. At low biasing current of less than 30 mA, the two raised interconnects are captured in the thermal measurement. This is observed even down to a current of 1 mA, where the heating effect is minimal and observed feature is clearly an artifact attributed to topography coupling. A look at the thermal line profile plot in Fig. 8.2 (a) clearly shows the limitation of the single lock-in setup in the presence of a surface with much topography variation. At location A1, the observed thermal signal is due to thermal probe encountering a step height during

measurement. This affects the effective thermal probe contact area with the DUT, thus resulting in the increased thermal signal captured. The slight dip in thermal signal observed at A2 can be attributed to the instance when the thermal probe begins lifting off the bottom of the DUT following the step profile encountered.

Even at a DC bias level of 40 mA (1.51 MA/cm^2), the non-thermal contribution by the raised topography is still too large for the heated interconnect to be detected. Heating from the biased interconnect is captured in the thermal signal only when a DC level of 50 mA (1.89 MA/cm^2) is applied. Despite this, the thermal signal from the biased interconnect at 50 mA is only about 2% higher than the non-thermal signal contribution from topography.

To determine the effective temperature increase due to DUT biasing, multiple measurements at various DUT biasing currents are taken. A single measurement can only provide the temperature contrast within the scanned region and not the temperature contrast between biased and unbiased state of the DUT. To achieve the temperature contrast between biased and unbiased state of the DUT, two separate measurements are taken and subtracted. This gives rise to two issues. Firstly, the second measurement may not be aligned perfectly with the first set of measurement. The alignment accuracy is dependent on the accuracy of the atomic force microscope and any physical movement of the DUT after each scan. Secondly, the accuracy of the temperature contrast obtained is also dependent on how fast the second measurement is taken. This is because the overall temperature drift of the setup due to environmental conditions can only be minimized but

not totally eliminated. Therefore, it is desirable to have the second measurement taken immediately after the first one.

In the double lock-in setup, the thermal signal as shown in Fig. 8.1 (c) is able to clearly pick up the biased interconnect. There is enough resolution to distinguish the 5 μm line from the unbiased interconnect even at low ac biasing current. The equivalent thermal line profile in Fig. 8.2 (b) shows that the biased interconnect can even be detected down to an AC biasing level of 10 mA. This is clearly observed in the inset of Fig. 8.2 (b). The 10 mA AC biased interconnect shows an increase of 26.3% compared to its surrounding reading. The thermal line profiles obtained do not have a high correlation with topography but is more closely related to the heated interconnect.

It is also observed that location L2 of Fig. 8.2 (b) has a higher temperature compared to location L3. This is because location L3 is on the right side where there is an 8μm wide unbiased interconnect. This large interconnect is able to conduct heat away from the biased interconnect much more effectively than location L2 on the left side where there is only a 1 μm wide unbiased interconnect. This explains the asymmetry of the thermal profiles obtained with the right hand side of the biased interconnect having a steeper gradient compared to the left hand side.

Since the DLIA setup is measuring the actual heating process, the thermal signal should follow the Joule's first law, which is also known as the Joule Effect. It states that the rate of heat dissipation is proportional to the square of the current and its resistance.

$$V_{out_LIA_B} = E_3 I^2 R \qquad \text{Eqn. (8.1)}$$
$$Lg(V_{out_LIA_B}) = 2Lg(I) + Lg(E_3 R)$$

where $V_{out_LIA_B}$ is the DLIA measured thermal signal, E_3 is the empirical constant of proportionality, I is the current bias applied to the DUT and R is the resistance of the DUT considered.

Taking the average of the DLIA thermal signal over the biased interconnect as shown by L1 in Fig. 8.2 (b), a plot of Lg ($V_{out_LIA_B}$) vs Lg (I) is done for DUT current bias of 1mA up to 20 mA at 1 mA interval.

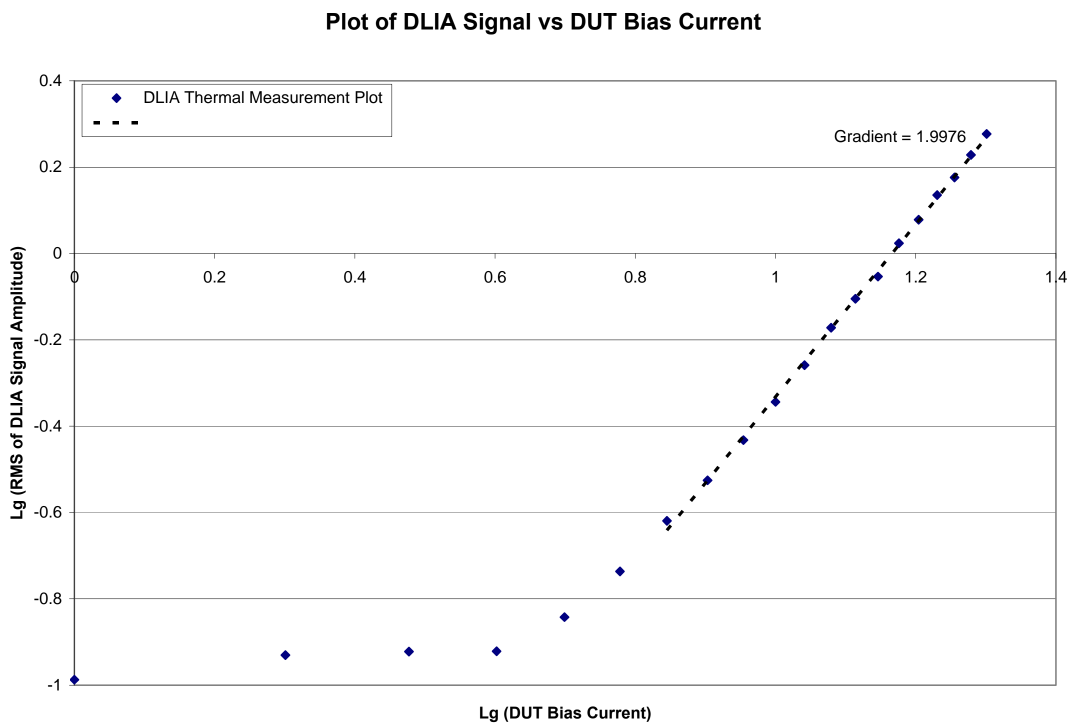
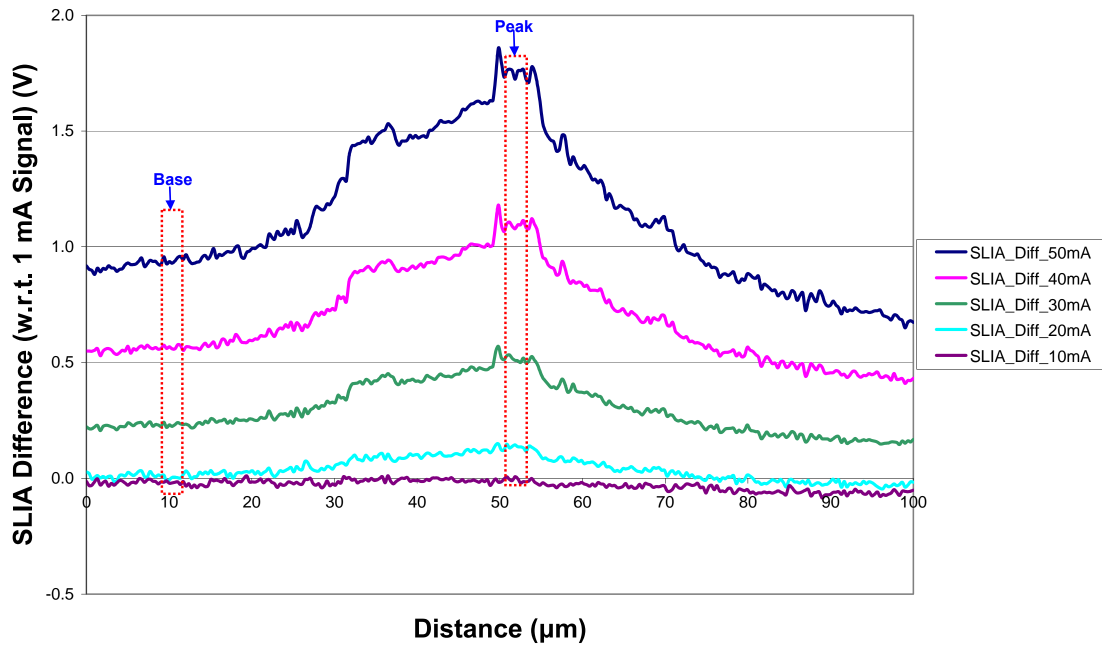


Figure 8.3: Plot of Lg ($V_{out_LIA_B}$) vs Lg (I) for DUT current bias from 1 mA up to 20 mA at 1 mA interval

At current bias of up to 4 mA, the plot does not appear to response to DUT current bias with the expected slope factor of 2 as the amount of heating is too weak to be captured by the system. From 5 mA of DUT biasing current onwards, the DLIA setup is sensitive enough to capture the heating effect. Considering data points starting from 7 mA onwards, a gradient of 2 can be achieved. This is in agreement with the factor of 2 expected if the DLIA signal captured is to follow the Joule Effect. Thus the DLIA system is sensitive down to a current of 7 mA (0.264 MA/cm^2).

8.2 Experimental Verification of Double Lock-In Model and Temperature Calibration

Since the SLIA measurement in Fig. 8.2 (a) is done by performing repeated 1D line scan while varying the DUT biasing condition at fixed interval, the concerns highlighted in the previous section regarding subtracting of SLIA thermal signal between biased and unbiased state are minimized. Also, since at 1 mA DUT current supply, there is effectively no thermal signal captured. Thus any signal output from the SLIA can be assumed to be due to the DUT topography, its interaction with the thermal probe as well as the ambient condition during the measurement. If so, taking the difference of SLIA 50 mA and 1 mA thermal signal should give similar result as DLIA thermal signal at 50 mA bias. Figure 8.4 compares the SLIA difference signal with that obtained from DLIA measurement.



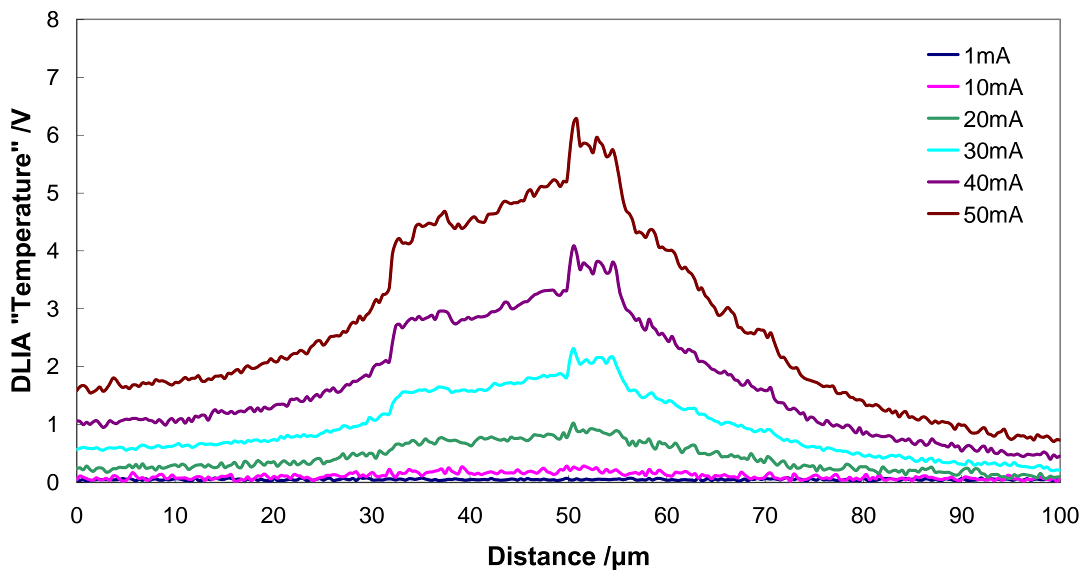


Figure 8.4: (a) SLIA Difference Thermal Signal and (b) DLIA Thermal Signal At Various Current Supply

Figure 8.4 (a) which is the difference signal from the SLIA measurement now looks similar to Fig. 8.4 (b) which is from the DLIA setup. The various features along the thermal profile can now be observed from both sets of measurement. This further proves the theory behind the DLIA setup. Furthermore, it shows that the DLIA is able to easily and accurately measure the temperature change in one measurement step. Similar result if acquired from the SLIA setup, has to be done with great care and longer measurement time with data crunching required.

Considering the 50 mA thermal profile, taking the difference of the SLIA difference thermal signal between the peak and base location in Fig. 8.4 (a) gives the effective temperature increase due to biased interconnect. This returns a value of about 0.864 V. Considering the LIA's sensitivity setting of 20 mV for a full range of 10 V, and using the calibration factor of 2.25 mV/K, a converted temperature rise of 0.77 K ($0.864 x \frac{20}{10} x \frac{1}{2.25}$) is calculated. This agrees well with the simulation done on similar electromigration structure and shown in Fig. 5.9 which shows a 0.761 K temperature increase for a 50 mA current supply [126].

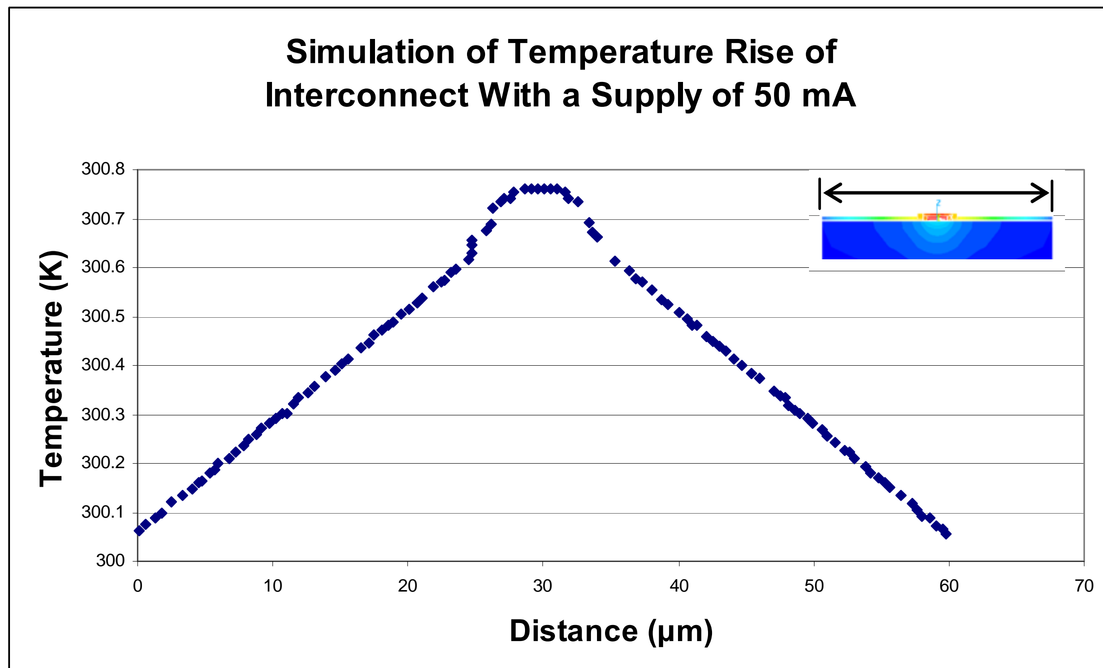


Figure 8.5: Simulation of Temperature Rise of Interconnect With a Supply of 50 mA Current

The good agreement between simulation result and the SLIA difference thermal signal shows that this set of readings can be used to determine the calibration factor or temperature sensitivity for the DLIA setup. The temperature calibration for DLIA measurement is thus created from the derived temperature as calculated from Fig. 8.4 (a) and the DLIA thermal signal from Fig. 8.4 (b) and shown in Figure 8.6.

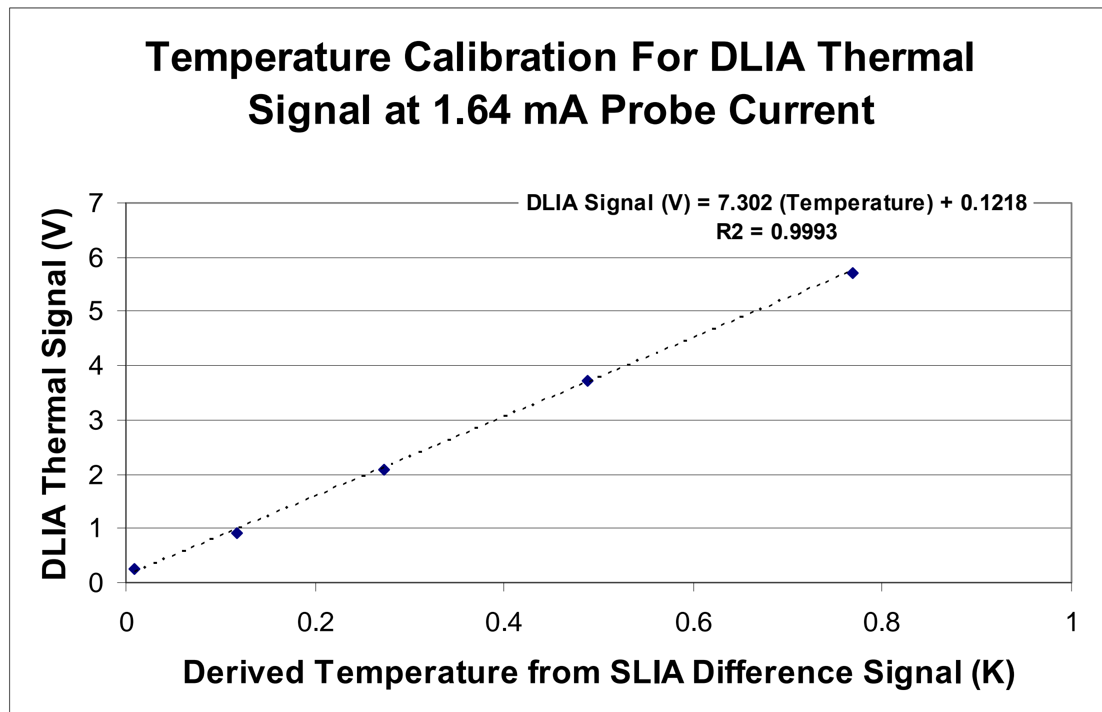


Figure 8.6: Temperature Calibration Plot for DLIA Setup

The plot shows a nicely fitted linear plot with the linear regression goodness of fit, R2 value of 0.9993 with a DLIA temperature sensitivity of 7.3 V/K.

Figure 8.7 shows the schematic of the various stages in the thermal signal path from Wheatstone bridge to output of LIA 2. A DLIA temperature sensitivity of 7.3 V/K at the output of LIA 2 (stage 5 in Fig. 8.7) translates to a sensitivity of 584 mV/K at stage 4 before the DC amplifier, considering the choice of 200 mV sensitivity setting used.

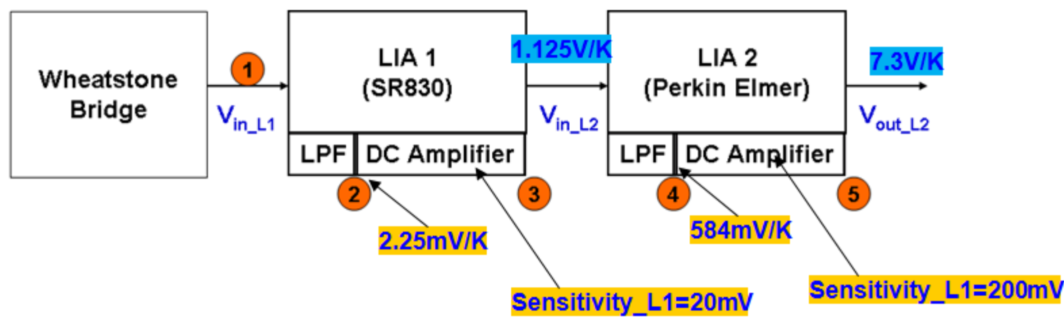


Figure 8.7: Schematic of the various stages in the thermal signal pathway

8.3 Summary

The performance of the DLIA setup to various current supplies for the DUT is investigated, with an achievable sensitivity value down to 7 mA (0.264 MA/cm^2). The sensitivity to underlying non-conducting feature is also observed in the asymmetric thermal profile of the DUT. Comparisons with the difference signal methodology of the SLIA thermal signals and the observed close similarity between the two, further verify the validity of the theoretical model developed for DLIA. Here, the advantage of the DLIA setup for characterizing temperature change with a single measurement compared to the multiple measurement required in the SLIA setup is also demonstrated.

Chapter 9: Conclusion

The continuous drive in the shrinkage of microelectronic devices to increase current density and on-chip clock frequency, together with the introduction of novel structures and materials with poor thermal conductivity such as SOI and low-K materials, can lead to performance and reliability issues which are thermal related. This calls for the need to have thermal measurement and characterization techniques that are compatible with the device requirements of advanced technology nodes.

A literature survey of thermal measurement tools found the probe-based SThM technique to be most compatible for smaller devices since its resolution is not diffraction limited as far-field optical methods. Its key element is the thermal probe and its spatial resolution is governed by probe-sample interaction which depends on the probe size. However, all probe-based thermal systems suffer from topography-thermal coupling artifact due to a change in the effective thermal contact area with the DUT. Besides, there is also the problem of thermal drift due to certain time duration required for capturing of the thermal signals. With a sensitive system, this would only get worse. With that, the identified shortcomings of conventional SThM methodology were addressed theoretically and experimentally in this project using the double lock-in amplifiers.

A theoretical treatment for the DLI setup was first carried out to account for the thermal signals obtained at various stages of the DLI setup. This allows for the thermal interpretation of on-the-fly “pixel-by-pixel thermal signal subtraction” algorithm that the setup is actually performing. Monitoring the signal output at LIA_A allows for a quick

sanity check that the system is operating under the correct conditions of DUT biasing and LIA_A parameters. Characterization of the system then follows to optimize the various parameters. This includes having the thermal probe dwell time to be multiple of the DUT heating cycle. The choice of time constant settings on the two LIA and their interactions with the DUT biasing are also evaluated. It is found that the ratio of the DUT biasing period to the LIA_B TC has to be less than 10.6 to achieve a stable thermal signal output. Furthermore, the TC of LIA_B should be at least 5 times that of LIA_A's TC for accurate thermal measurement without the interference from topography-thermal coupling.

The application of the DLIA setup on an EM structure shows that the thermal signal decreases at increasing DUT biasing frequencies and this agrees well with the mathematical model developed. It also demonstrates that a ratio of DUT biasing period over thermal time constant of more than 8.3 is required to ensure that the thermal signal is sufficient to overcome the effect of topography coupling. The DLIA system also demonstrates sensitivity down to a current of 7 mA (0.264 MA/cm^2). This means that the DLIA system is able to capture the DUT heating down to a current of 7 mA. On the other hand, the thermal signals obtained with SLIA were overwhelmed by the topography coupling artifacts. Besides, the DLIA system also demonstrates the ability to capture the actual heating process by having the thermal signal in agreement with the Joule Effect. In addition, the ability of the DLIA setup for characterizing temperature change with a single measurement compared to the multiple measurements required in the SLIA setup is also demonstrated.

Chapter 10: Recommendation for Future Work

In this chapter, it is proposed that the DLIA setup can be modified to be implemented for quantitative thermal conductivity analysis as a future research work.

In quantitative thermal conductivity measurement using the 3ω method [127], the voltage signal at 2 different frequencies is required before the thermal conductivity can be determined. It is hoped that the modified DLIA setup for thermal conductivity measurement can achieve quantitative values with just a single measurement.

The concept is to integrate the frequency shift keying frequency modulation scheme into the modified DLIA setup so as to achieve results from 2 different frequencies in a single measurement. It also makes use of the dual reference mode available to the Perkin Elmer 7280. However, it comes with 3 restrictions. Firstly, one of the reference signals have to be external while the other to be derived from the internal oscillator. Secondly, the maximum operating frequency is 20 kHz. Finally, both signals must be passed through the same input signal channel. That is the signals are derived from the same detector.

The proposed schematic setup focusing on the Wheatstone bridge and excluding the AFM system is shown in Fig. 10.1.

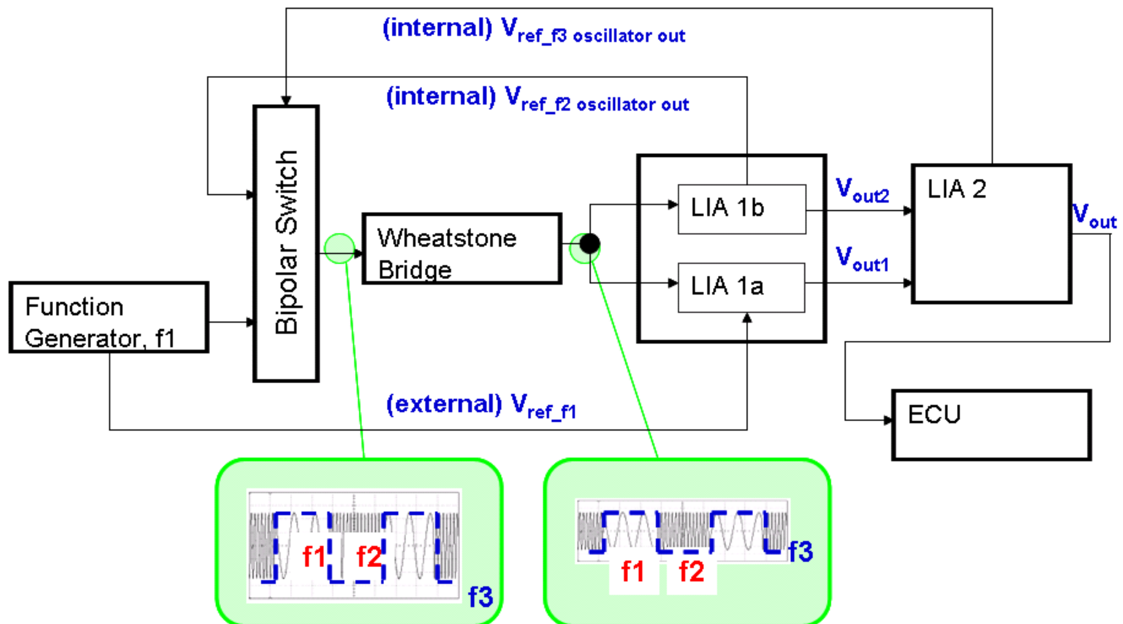


Figure 10.1: Schematic of proposed DLIA setup for quantitative thermal conductivity measurement.

Thus, it is hoped that with the proposed setup, the V_{out} signal from LIA 2 will be able to provide the quantitative thermal conductivity readings in a single measurement.

References:

[1] http://www.itrs.net

[2] Cahill D.G., Goodson K., Majumdar A., “Thermometry and Thermal Transport in Micro/Nanoscale Solde-State Devices and Structures”, Journal of Heat Transfer, vol 124, pg. 223 – 241, 2002

[3] Asheghi M., Touzelbaev N., Goodson K.E., Leung Y.K., Wong S.S., “Temperature-Dependent Thermal Conductivity of Single-Crystal Silicon Layers in SOI Substrates”, J. Heat Transfer, vol. 120, pg. 30-36, 1998

[4] Ju Y.S., Goodson K.E, “Phonon Scattering in Silicon Films with Thickness of Order 100 nm”, Appl. Phys. Lett., vol. 74, pg. 3005-3007, 1999

[5] Asheghi M., Kurabayashi K., Kasnavi R., Goodson K.E., “Thermal Conduction in Doped Single-Crystal Silicon Films”, J. Appl. Phys., vol. 91, pg. 5079-5088, 2002

[6] Von Arx M., Paul O., Baltes H., “Process-Dependent Thin-Film Thermal Conductivities for Thermal CMOS MEMS”, J. Microelectromech. Sys., vol. 9, pg 136-145, 2000

[7] Uma S., McConnell A.D., Asheghi M., Kurabayashi K., Goodson K.E., “Temperature Dependent Thermal Conductivity of Undoped Polycrystalline Silicon”, Int. J. Thermophys., vol. 22, pg. 605-616, 2001

[8] McConnell A.D., Uma S., Goodson K.E., “Thermal Conductivity of Doped Polysilicon Layers”, J. Microelectromech. Sys., vol. 10, pg. 360-369, 2001

[9] Cahill D.G., Ford W.K., Goodson K.E., Mahan G.D., Majumdar A., Maris H.J., Merlin R., Phillpot S.R., “Nanoscale thermal transport”, Journal of Applied Physics, vol 93, pg. 793-818, 2003

[10] Carslaw H.S. and Jaeger J.C., "Conduction of Heat in Solids", Oxford University Press, New York, pg 109-112, 1959

[11] Ziman J.M., "Electrons and Phonons", Clarendon, Oxford, 1960

[12] Majumdar A., "Microscale Heat Conduction in Dielectric Thin Films", J. Heat Transfer, vol 115, pg. 7-16, 1993

[13] Shi L., Kwon O., Miner A.C., Majumdar A., "Design and Fabrication of Probes for Sub-100 nm Scanning Thermal Microscopy", J. of MEMS, 10, pg. 370-378, 2001

[14] Shi L., Majumdar A., "Thermal Transport Mechanisms at Nanoscale Point Contacts", ASME J. Heat Transfer, Vol. 124, pg. 329-337, 2002

[15] Majumdar A., "Scanning Thermal Microscopy", Annu. Rev. Mater. Sci., 29, pg. 505-585, 1999

[16] Lee J., Wright T.L., Abel M.R., Sunden E.O., Marchenkov A., Graham S., King W.P., "Thermal Conduction from Microcantilever Heaters in Partial Vacuum", J. Appl. Phys. 2007, 101, 014906

[17] Kim K.J., Park K., Lee J., Zhang Z.M., King W.P., "Nanotopographical Imaging Using a Heated Atomic Force Microscope Cantilever Probe", Sens. Actuators A, 136, pg. 95–103, 2007

[18] Gomes S., Trannoy N., Grossel P., "D.C. Thermal Microscopy: Study of the thermal exchange between a probe and a sample", Meas. Sci. Technol., vol. 10, pg. 805-811, 1999

[19] Lefevre S., Volz S., Chapuis P.O., "Nanoscale heat transfer at contact between a hot tip and a substrate", Int. J. Heat Mass Transf., vol. 49, pg. 251, 2006

[20] Duvigneau J., Schonherr H., Vancso G.J., "Nanoscale Thermal AFM of Polymers: Transient Heat Flow Effects", ACSNANO, vol. 4, 11, pg. 6932-6940, 2010

[21] Liu W.L., Turin V.O., Balandin A.A., Chen Y.L., Wang K.L., "The Ambient Temperature Effect on Current-Voltage Characteristics of Surface-Passivated GaN-Based Field-Effect Transistors", MRS Internet Journal of Nitride Semiconductor Research, vol 9, 4 pages, 2004

[22] Blackburn D.L., "Temperature Measurements of Semiconductor Devices – A Review", SEMI-THERM, pg. 70-80, 2004

[23] Sze S.M., "Physics of Semiconductor Devices", John Wiley and Sons, 1981

[24] Chang Y.H., Wu Y.T., "Measurement of Junction Temperature in Heterojunction Bipolar Transistors", International Caracus Conference on Devices, Circuits and Systems, pg. 1-4, 2000

[25] Donarski R.J., "Pulsed I-V and Temperature Measurement System for Characterisation of Microwave FETs", IEEE International Microwave Symposium Digest, pg. 1523-1526. 1995

[26] Piccirillo A., "Complete Characterisation of Laser Diode Thermal Circuit by Voltage Transient Measurements", Electronics Letters, vol. 29, pg. 318-320, 1993

[27] Baliga and B.J., "Modern Power Devices", John Wiley and Sons, 1987

[28] Jakopovic Z., Bencic Z., Kolonic F., "Important Properties of Transient Thermal Impedance for MOS-Gated Power Semiconductors", International Symposium on Industrial Electronics, vol. 2, pg. 574-578, 1999

[29] Bunyan R.J.T., Uren M.J., Alderman J.C., Eccleston W., “Use of Noise Thermometry to Study the Effects of Self-Heating in Submicrometer SOI MOSFET’s”, IEEE Electron Device Lett., Vol. 13, pg. 279-281, 1992

[30] Schuemeyer F., Fitch R., Dettmer R., Gillespie J., Bozada C., Nakano K., Sewel J., Ebel J., Jenkins T., Liou L.L., “Thermal Studies on Heterostructure Bipolar Transistors Using Electroluminescence”, IEEE Cornel Conference on High Performance Devices, pg. 45-50, 2000

[31] Landesman J.P., Floriot D., Martin E., Bisaro R., Delage S.L., Braun P., ”Temperature Distributions in III-V Microwave Power Transistors Using Spatially Resolved Photoluminescence Mapping”, IEEE Caracas Conferences on Devices, Circuits and Systems, pg. 1-8, 2000

[32] Kim Q., Srark B., Kayali S., “A Novel, High Resolution Non-Contact Channel Temperature Measurement Technique”. IRPS, pg. 108-112, 1998

[33] Aigouy L., Lalouat L., Mortier M., Low P., Bergaud C., “A scanning thermal probe microscope that operates in liquids”, Rev. Sci. Instrum., Vol. 82, 036106, 2011

[34] Kuball M., Hayes J.M., Uren M.J., Martin I., Birbeck J.C.H., Balmer R.S., Hughes B.T., “Measurement of Temperature in Active High Power AlGaN/GaN HFETs Using Raman Spectroscopy”, IEEE Electron Device Letters, vol. 23, pg. 7-9, 2002

[35] He J., Mehrotra V., Shaw M.C., “Ultra High Resolution Temperature Measurement and Thermal Management of RF Power Devices Using Heat Pipes”, Symposium on Power Semiconductor Devices and ICs, pg. 145-148, 1999

[36] Ju Y.S., Goodson K.E., "Short-Timescale Thermal Mapping of Interconnects", IRPS, pg. 320-324, 1997

[37] Claeys W., Dilhaire V., Quintard V., Dom J.P., Danto Y., "Thermoreflectance Optical Test Probe for the Measurement of Current-Induced Temperature Changes in Microelectronic Components", Quality and Reliability Engineering International, vol. 9, pg. 303-308, 1993

[38] Hefner A., Berning D.W., Blackburn D.L., Chapuy C., "A High-Speed Thermal Imaging System for Semiconductor Device Analysis",IEEE Semiconductor Thermal Measurement and Management Symposium, pg. 43-49, 2001

[39] Yasuda A., Yamaguchi H., Tanabe Y., Owada N., Hirasawa S., "Direct Measurement of Localized Joule Heating in Silicon Devices by Means of Newly Developed High Resolution IR Microscopy", IRPS, pg. 245-249, 1991

[40] Kondo S., Hinode K., "High-Resolution Temperature Measurement of Void Dynamics Induced by Electromigration in Aluminum Metallization", Appl. Phys. Lett., Vol. 67, pg. 1606-1608, 1995

[41] Azar K., Farina D., "Measuring Chip Temperatures With Thermochromic Liquid Crystals", Electronics Cooling, 1997

[42] Jeong P., Moo W.S., Lee C.C., "Thermal Modeling and Measurement of GaN-Based HFET Devices", IEEE Electron Device Letters, vol. 24, pg. 424-426, 2003

[43] Chaudhari A.M., Woudenberg T.M., Albin M., Goodson K.E., "Transient Liquid Crystal Thermometry of Microfabricated PCR Vessel Arrays", Journal of Microelectromechanical Systems, vol. 7, pg. 345-355, 1998

[44] Cooper M.G., Mikic B.B., Yovanovich M.M., "Thermal Contact Conductance", Int. Journal of Heat and Mass Transfer, Vol. 12, pg. 279-300, 1969

[45] Christofferson J., Maize K., Ezzahri Y., Shabani J., Wang X., Shakouri A., "Microscale and Nanascale Thermal Characterization Techniques", Journal of Electronic Packaging, Vol. 130, pg. 1 – 6, 2008

[46] Pollock H.M., Hammiche A., "Micro-Thermal Analysis: Techniques and Applications", J. Phys D: Appl Phys 34, R23 – R53, 2001

[47] Majumdar A., "Scanning Thermal Microscopy", Annu. Rev. Mater. Sci., 29, pg. 505-585, 1999

[48] Williams C.C., Wickramasinghe H.K., "Scanning Thermal Profiler", Appl. Phys. Lett., 49(23), pg. 1587-1589, 1986

[49] Weaver J.M.R., Walpita L.M., Wickramasinghe H.K., Nature 342, pg. 783-785, 1989

[50] Majumdar A., Carrejo J.P., Lai J., "Thermal Imaging using the Atomic Force Microscope", Appl. Phys. Lett., 62(20), pg. 2501-2503, 1993

[51] Luo K., Shi Z., Varesi J., Majumdar A., "Sensor Nanofabrication, Performance and Conduction Mechanisms in Scanning Thermal Microscopy", J. Vac. Sci. Technol. B 15(2), pg. 349-360, 1997

[52] Leinhos T., Stopka M., Oesterschulze E., "Micromachined Fabrication of Si Cantilevers with Schottky Diodes Integrated in the Tip", Appl. Phys. A 66, pg. 65-69, 1998

[53] Nakabeppu O., Suzuki T., "Microscale temperature measurement by scanning thermal microscopy", J. Therm. Anal. Cal, Vol. 69, pg. 727-737, 2002

[54] Kim K., Chung J., Won J., Kwon O., Lee J.S., Park S.H., Chio Y.K., "Quantitative scanning thermal microscopy using double scan technique", Appl. Phys. Lett., Vol. 93, 203115, 2008

[55] Kim K., Chung J., "Quantitative Measurement with Scanning Thermal Microscope by Preventing the Distortion Due to the Heat Tranafer through the Air", ACSNANO, Vol. 5, pg. 8700-8709, 2011

[56] Chung J., Kim K., Hwang G., Kwon O., Jung S., Lee J., Lee J.W., Kim G.T., "Quantitative temperature measurement of an electrically heated carbon nanotube using the null-point method", Rev. Sci. Instrum., Vol. 81, 114901, 2010

[57] Chung J., Kim K., Hwang G., Kwon O., Choi Y.K., Lee J.S., "Quantitative temperature profiling through null-point scanning thermal microscopy", Int. J. Thermal Sciences, 62, pg. 109-113, 2012

[58] Gimzewski J.K., Gerber C.H., Meyer E., Schlittler R.R., Chem. Phys. Lett., 217, pg. 589, 1994

[59] Nakabeppu O., Chandrahood M., Wu Y., Lai J., Majumdar A., "Scanning thermal imaging microscopy using composite cantilever probes", Appl. Phys. Lett., 66(6), pg. 694-696, 1995

[60] Varesi J., Majumdar A., "Scanning joule expansion microscopy at nanometer scales", Appl. Phys. Lett., 72(1), pg. 37-39, 1998

[61] Grosse K.L., Bae M.H., Lian F.F., Pop E., King W.P., "Nanoscale Joule Heating, Peltier Cooling and Current Crowding at Graphene-Metal Contacts", Nat. Nanotechnol., 6, pg. 287–290, 2011

[62] Igeta M., Banerjee K., Wu G., Majumdar A., "Thermal Characteristics of Submicron Vias Studied by Scanning Joule Expansion Microscopy", Electron Device Letter 21(5), pg. 224-226, 2000

[63] Smallwood R., Metherall P., Hose D., Delves M., Pollock H., Hammiche A., Hodges C., Mathot V., Willcocks P., "Tomographic imaging and scanning thermal microscopy: thermal impedance tomography", Thermochimica Acta, Vol. 385, pg. 19-32, 2002

[64] Hammiche A., Price D.M., Dupas E., Mills G., Kulik A., Reading M., Weaver J.M.R., Pollock H.M., "Two new microscopical variants of thermomechanical modulation: scanning thermal expansion microscopy and dynamic localized thermomechanical analysis", Journal of Microscopy, Vol. 199, pg. 180-190, 2000

[65] Hammiche A., Pollock H.M., Reading M., Claybourn M., Turner P.H., Jewkes K., "Photothermal FT-IR Spectroscopy: A Step Towards FT-IR Microscopy at a Resolution Better Than the Diffraction Limit", Applied Spectroscopy, Vol. 53, pg. 810-815, 1999

[66] Soudi A., Dawson R.D., Gu Y., "Quantitative Heat Dissipation Characteristics in Current-Carrying GaN Nanowires Probed by Combining Scanning Thermal Microscopy and Spatially Resolved Raman Spectroscopy", ACSNANO, Vol. 5, pg. 255-262, 2011

[67] Puyoo E., Grauby S., Rampnoux J.M., Rouviere E., Dilhaire S., "Scanning thermal microscopy of individual silicon nanowires", J. of Applied Phys., 109m 024302, 2011

[68] Kar-Narayan S., Crossley S., Moya X., Kovacova V., Abergel J., Bontempi A., Baier N., Defay E., Mathur N.D., "Direct electrocaloric measurements of a multilayer capacitor using scanning thermal microscopy and infra-red imaging", Appl. Phys. Lett., 102, 032903, 2013

[69] Fiege G.B.M., Feige V., Phang J.C.H., Maywald M., Görlich S., Balk L.J., "Failure Analysis of Integrated Devices by Scanning Thermal Microscopy (SThM)", Microe. Reliab. 38, pg. 957-961, 1998

[70] Hammiche A., Reading M., Pollock H.M., Song M., Hourston D.J., "Localized Thermal Analysis Using a Miniaturized Resistive Probe", Rev. Sci. Instru. 67(12), pg. 4268-4274, 1996

[71] Altes A., Mutamba K., Heiderhoff R., Hartnagel H.L., Balk L.J., "Scanning Near Field Thermal Microscopy on a Micromachined Thin Membrane", Superlattices and Microstructures 25, pg. 465-476, 2004

[72] David L., Gomes S., Galland P., Vassort B., Raynaud M., "Characterisation of thin films using scanning thermal microscopy", ECTP, 12 pages, 2005

[73] Lee J., Gianchandani Y.B., "A Temperature-Dithering Closed-Loop Interface Circuit for a Scanning Thermal Microscopy System", J. of Microelectromechanical Systems, Vol. 14, pg. 44-53, 2005

[74] Cahill D.G., "Thermal Conductivity Measurement from 30 to 750 K: the 3ω Method", Rev. Sci. Instrum. 61, pg. 802-808, 1990

[75] Fiege G.B.M., Altes A., Heiderhoff R., Balk L.J., "Quantitative Thermal Conductivity Measurements with Nanometre Resolution", J. Phys. D, Vol. 32(5), pg. L13-L17, 1999

[76] Hinz M., Marti O., Gotsmann B., Lantz M.A., Dürig U., “High resolution vacuum scanning thermal microscopy of HfO_2 and SiO_2”, Appl. Phys. Lett., 92, 043122, 2008

[77] Cahill D.G., Goodson K., Majumdar A., “Thermometry and Thermal Transport in Micro/Nanoscale Solid-State Devices and Structures”, Journal of Heat Transfer, Vol. 124, pg. 223-241, 2002

[78] http://www.parkAFM.com

[79] Dinwiddie R.B., Pylkki R.J., West P.E., “Thermal conductivity contrast imaging with a scanning thermal microscope”, Thermal Conductivity 22, pg. 668-677, 1994

[80] Maywald M., Pylkki R.J., Balk L.J., “Imaging of local thermal and electrical conductivity with scanning force microscope”, Scanning Microscopy 8(2), pg. 181-188, 1994

[81] Balk L.J., Maywald M., Phlkki R.J., “Nanoscopic Detection of the Thermal Conductivity of Compound Semiconductor Materials by Enhanced Scanning Thermal Microscopy”, 9th Oxford Conference on Microscopy of Semiconducting Materials (Inst. Of Phys. Conf. Ser. No. 146), pg. 655-658, 1995

[82] Brown E., Hao L., Cox D.C., Gallop J.C., “Scanning thermal microscopy probe capable of simultaneous electrical imaging and the addition of a diamond tip”, Journal of Physics, vol. 100, pg. 1-5, 2008

[83] Altes A., “Quantitative Dynamic Near-Field Microscopy of Thermal Conductivity”, Ph.D Thesis, University of Wuppertal, 2004

[84] Csendes A., Szekely V., Rencz M., “Thermal Mapping With Liquid Crystal Method”, 31, pg. 281-290, 1996

[85] Buzin A.I., Kamasa P., Pyda M., Wunderlich B., "Application of a Wollaston wire probe for quantitative thermal analysis", Thermochimica Acta 381, pg. 9-18, 2002

[86] Ezzahri Y., Patino Lopez L.D., Chapuis O., Dilhaire S., Grauby S., Claeys W., Volz S., "Dynamical behavior of the scanning thermal microscope (SThM) thermal resistive probe studied using Si/SiGe microcoolers

[87] Zhang Y., Dobson P.S., Weaver J.M.R., "High temperature imaging using a thermally compensated cantilever resistive probe for scanning thermal microscopy", J. Vac. Sci. Technol. B, 30, 010601, 2012

[88] Zhang Y., Dobson P.S., Weaver J.M.R., "Batch fabricated dual cantilever resistive probe for scanning thermal microscopy", Vol. 88, pg 2435-2438, 2011

[89] Wielgoszewski G., Sulecki P., Janus P., Grabiec P., Zschech E., Gotszalk T., "A high-resolution measurement system for novel scanning thermal microscopy resistive nanoprobes", Meas. Sci. Technol., 22, 094023, 2011

[90] Wielgoszewski G., Sulecki P., Gotszalk T., Janus P., Szmigiel D., Grabiec P., Zschech E., "Microfabricated resistive high-sensitivity nanoprobe for scanning thermal microscopy", J. Vac. Sci. Technol. B, 28, C6N7–11, 2010

[91] Goree J., "Double lock-in detection for recovering weak coherent radio frequency signals", Rev. Sci. Instrum, 56, pg. 1662-1664, 1985

[92] Jang S.H., Fox M.D., "Double Lock-in Concept for MORE Glucose Detection", IEEE Annual Northeast Biomedical Conference, pg. 122-124, 1999

[93] Jang S.H., Yang Z., Fox M.D., "Double Lock-in Amplifier Faraday Rotation Glucometer", IEEE Annual Northeast Bioengineering Conference, pg. 107-108, 2000

[94] Aoki T., "Nanosecond QFRS study of photoluminescence in amorphous semiconductors", Journal of material science, 14, pg. 697-701, 2003

[95] Aoki T., Ideda K., Urashima T., Kaneko T., Saitou D., Kobayashi., "Photoluminescence lifetime distributions of amorphous and porous semiconductors, and organic luminescent materials; wideband quadrature frequency resolved spectroscopy extending over 11 decades", CCECE, pg. 211-214, 2005

[96] Kwang Y.S., Kazuo H., "Enlargement of measurement range in a brillouin optical correlation domain analysis system using double lock-in amplifiers and a single-sideband modulator", IEEE Photonics Technology Letters, pg. 499-501, 2006

[97] Eftaxias K., Vallianatos F., "A new approach to the optimum wire setting in a Wheatstone bridge", Phys. Edu., pg. 320-321, 1994

[98] O'Dea J., Fleming P., "The conflicting conditions for precision and sensitivity in a Wheatstone bridge", Phy. Edu., pg. 389-390, 1995

[99] Stig E., Eng. Sci. And Edu. Journal, "The Genesis of the Wheatstone Bridge", pg. 37–40, 2001

[100] http://www.allaboutcircuits.com/vol_1/chpt_8/10.html

[101] Fontana G., "Compensated Current Injection Circuit, theory and applications", Rev. Sci. Instrum., pg. 1332-1337, 74, 2003

[102] Williams A.J. and Rosser K.E., "A comparison of A.C. and D.C. Wheatstone Bridges for the Purpose of High Precision Temperature Measurement", NPL Report, CIRM 42, Centre for Ionising Radiation Metrology

[103] Haynes W.M., CRC Handbook of Chemistry and Physics, 91st Edition (Internet Version 2011), CRC Press/Taylor and Francis, Boca Raton, FL.

[104] Balk L.J. et al., "Microscopy of Semiconducting Materials", Inst. Phys. Conf. Ser., 146, pg. 655-658, 1995

[105] Meade M.L., "Lock-in amplifiers: principles and applications", Peter Peregrinus Ltd, 1983

[106] "Model SR830 DSP Lock-In Amplifier", Stanford Research Systems, pp.3-1, 2002

[107] Perkin Elmer, "Model 7280 Wide Bandwidth DSP Lock-in Amplifier", Instruction Manual, 2005

[108] THERMOMICROSCOPES Explorer^{TM} Instrument Operation Manual

[109] Lee T.H., "Characterization of MOS Devices by Scanning Thermal Microscopy (SThM)", ISTFA, 2001

[110] Chuan Hu et al, "Thermal Conductivity Study of Porous low-k Dielectric Materials", Appl. Phys. Letter, 77, pp. 145-147, 2000

[111] Cahill, D.G., "Thermal Conductivity Measurement from 30 to 750K: the 3ω Method", Review of Scientific Instruments, Vol. 61, pp. 802-808, 1989

[112] Chris Dames, Department of Mechanical Engineering, University of UC Riverside, http://www.engr.ucr.edu/~cdames/research.html, 2007

[113] Opsal J. and Rosencwaig A., "Thermal-wave Depth Profiling: Theory", J. Appl. Phys., 53, pp. 4240-4246, 1982

[114] Cahill D.G. et al, "Heat Transport in Micron Thick Si:H films", Philosophical Magazine B, 71, pp. 677-682, 1995

[115] Wu E.X.W., Zheng X.H., Phang J.C.H., Balk L.J., Lloyd J.R., "Characterization of Interconnect Defects due to Electromigration using Scanning Thermal

Microscopy", Conference Proceedings of the 29th International Symposium for Testing and Failure Analysis, pg. 419-424, 2003

[116] Meyer D., Kupinski P.E., Liu J.C., 1999 US Patent US5991113

[117] Suk M., Miyake K., Kurita M., Tanaka H., Saegusa S., Robertson N., "Verification of thermally induced nanometer actuation of magnetic recording transducer to overcome mechanical and magnetic spacing challenges", IEEE Trans. Mag., 41, pg. 4350-4352, 2005

[118] Chen Y.J., Leong S.H., Huang T.L., Ng K.W., Hu S.B., Yuan Z.M., Ng V., "A comparative study of write field distribution of trailing-edge shielded and unshielded perpendicular write heads by quantitative magnetic force microscopy", Appl. Phys. Lett., 92, 162505, 2008

[119] Lim M.J., Leong S.H., Hg K.W., Chen Y.J., Huang T.L., Ong C.L., Santoso B., Yuan Z.M., "Observation and Study of Off-Track Effect Induced by Thermal Actuated Protrusion of Slider", 53rd Magnetism and Magnetic Materials Conf. (Austin, TX) paper CW-10, 2008

[120] Ho H.W., Altes A., Phang J.C.H., Balk L.J., "Characterization of Interconnect Defects Using Scanning Thermal Conductivity Microscopy", ISTFA, 2004

[121] Marinello F., Balcon M., Schiavuta P., Carmignato S., Savio E., "Thermal drift study on different commercial scanning probe microscopes during the initial warming-up phase", Meas. Sci. Technol., 22, 094016, 2011

[122] Hendarto E., Altes A., Heiderhoff R., Phang J.C.H., Balk L.J., "Investigation on the thermal distribution of nMOSFETs under different operation modes by scanning thermal microscopy," IEEE IRPS, pg. 294-299, 2005

[123] Suehle J.S., Schafft H.A., “Current Density Dependence of Electromigration t_{50} Enhancement Due To Pulsed Operation”, IEEE IRPS, pg. 106-110, 1990

[124] Arnaud L., Reimbold G., Waltz P., “Influence of Pulsed DC Current Stress On Electromigration Results in AlCu Interconnections: Analysis of Thermal and Healing Effects”, Microelectronics Reliability 39, pg. 773-784, 1999

[125] Stanford Research System SR830 Manual

[126] Zheng X., “Characterization of Electromigration Defects Using Scanning Thermal Microscopy”, M.Eng, 2004

[127] Altes A., Heiderhoff R., Balk L.J., “Quantitative Dynamic Near-Field Microscopy of Thermal Conductivity”, Journal of Physics D: Applied Physics,37, pg. 952-963, 2004

List of Publications

[1] Ho H.W., Phang J.C.H., Altes A., Balk L.J., "Characterization of Interconnect Defects Using Scanning thermal Conductivity Microscopy", ISTFA, pg. 363-368, 2004

[2] Ho H.W., Zheng X.H., Phang J.C.H., Balk L.J., "Reliable And Accurate Temperature Measurement Using Scanning Thermal Microscopy With Double Lock-In Amplification", IRPS, pg. 804-807, 2009

[3] Chen Y., Leong S., Huang T., Ho H.W., Ng V., Phang J., "Atomic force microscopy (AFM) and scanning thermal microscopy (SThM) studies of thermal response of perpendicular recording head to writing and heating currents", Intermag, CC09, 2009

[4] Chen Y.J., Leong S.H., Huang T.L., Ho H.W., Ng V., Phang J.C.H., "Thermal effects inducted lateral head shift of thermal flying height control perpendicular magnetic recording head", J. Phys. D: Appl. Phys., vol 43, pg. 1-5, 2010