SELF-ALIGNED SOURCE AND DRAIN CONTACT ENGINEERING FOR HIGH MOBILITY III-V TRANSISTOR

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SELF-ALIGNED SOURCE AND DRAIN CONTACT ENGINEERING FOR HIGH MOBILITY III-V TRANSISTOR

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Declaration

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Zhang Xin Gui

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Abstract

Self-Aligned Source and Drain Contact Engineering

For High Mobility III-V Transistor

by

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Driven by tremendous advances in lithography the semiconductor industry has followed Moore's law by shrinking transistor dimensions continuously for the last 40 years. The big challenge going forward is that continued scaling of Si transistors will be more and more difficult because of both fundamental limitations and practical considerations as the transistor dimensions approach 10 nm. Among several emerging nanoscale devices, III-V MOSFETs are the most attractive devices due to their high electron mobility, low supply voltage, and potential heterogeneous integration on Si substrates. To take the full advantages of III-V MOSFETs, low-resistance source/drain (S/D) is required. However, III-V transistors currently have large S/D series resistance limiting the device drive current as they lack advanced S/D contact technologies. This thesis documents work performed on self-aligned S/D contact engineering for III-V n-MOSFETs.

In this thesis, novel self-aligned metallization, analogous to the salicidation process in Si CMOS, was developed for III-V n-MOSFETs to address the high S/D resistance issue. New contact materials such as NiGeSi, Ni-InGaAs were developed

and the key characteristics of these new contact materials were determined and identified. Various process integration challenges for realizing self-aligned S/D contacts were identified and addressed. Technology demonstrations of these new materials integrated as III-V S/D contacts in a self-aligned manner were also realized. In particular, NiGeSi and Ni-InGaAs were integrated in GaAs and InGaAs planar n-MOSFETs, respectively, using a salicide-like process and leading to reduced series resistance.

For achieving better electrostatic control than planar n-MOSFETs, novel III-V FinFETs were explored. S/D resistance engineering was also carried out for the FinFETs. With well designed FinFETs structure and metallization process, self-aligned contacts such as Ni-InGaAs and Mo were realized on *in-situ* heavily doped III-V S/D. The combination of heavily doped S/D and self-aligned contacts leads to low series resistance for InGaAs FinFETs. Series resistance as low as 250 Ω·μm was obtained, and this is the lowest value reported-to-date for InGaAs non-planar n-MOSFETs. This affirms the effectiveness of the S/D resistance engineering concept of combining heavily doped S/D and self-aligned contacts. The availability of self-aligned contact technology is an important step towards realization of high performance III-V logic transistors.

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Symbol	Description	Unit
A^*	Richardson constant	$Acm^{-2}K^{-2}$
C_d	Depletion capacitance	F
C_{ox}	Gate oxide capacitance	F
d	Contact spacing	μm
D_{sp}	Spacing between probe and channel	μm
D_{IT}	Interface state density	$cm^{-2}eV^{-1}$
D_n	Diffusion coefficient for electron	cm^2s^{-1}
D_p	Diffusion coefficient for hole	cm^2s^{-1}
E_F	Fermi level	eV
E_C	Conduction band edge	eV
E_V	Valence band edge	eV
G_d	Drain conductance	S
$G_{m,ext}$	Extrinsic transconductance	S
$G_{m,int}$	Intrinsic transconductance	S
h	Planck's constant	eVs
I_D	Drive current (per unit width)	μA/μm
I_{Dlin}	Linear drain current (per unit width)	μA/μm
I_G	Gate current (per unit width)	A/μm
I_{ON}	On state current (per unit width)	μA/μm
I_{OFF}	Off state current (per unit width)	A/μm
$J_{S,Schottky}$	Reverse current density of Schottky diode	A/cm^2
$J_{S,PN}$	Reverse current density of PN diode	A/cm^2
J_G	Gate leakage current density	A/cm^2
k	Boltzman's constant	eV/K
L	Contact length	μm
L_G	Gate length	nm
L_T	Transfer length	μm
L_{CH}	Channel Length	nm
$L_{As\text{-}print}$	As-printed channel Length	nm
L_{SD}	Spacing between contact and channel	μm
$L_{overlap}$	Gate-to-source overlap length	nm
L_n	Electron diffusion length	m

L_p	Hole diffusion length	m
m_n^*	Effective mass	kg
n_{po}	Minority electron concentration	cm^{-3}
N_A	Hole concentration	cm^{-3}
N_D	Electron concentration	cm^{-3}
p_{no}	Minority hole concentration	cm^{-3}
q	Electronic charge	C
Q_f	Fixed charge density	C/cm^2
R_C	Contact resistance	Ω·μm
R_{CH}	Channel resistance	Ω·μm
R_S	Source resistance	Ω·μm
R_{cap}	InGaAs cap resistance	Ω·μm
R_D	Drain resistance	Ω·μm
R_{SD}	Source/drain series resistance	Ω·μm
R_{metal}	Metal resistance	Ω·μm
R_{sh}	Sheet resistance	Ω/square
$R_{sh,InGaAs}$	InGaAs sheet resistance	Ω/square
R_{III-V}	III-V resistance	Ω·μm
$R_{Ni-InGaAs}'$	Ni-InGaAs resistance	Ω
$R_{Ni-InGaAs}$	Ni-InGaAs resistance	Ω·μm
R_{side}	Barrier and spreading resistance	Ω·μm
R_T	Total resistance	Ω·μm
S	Subthreshold swing	mV/decade
$t_{Ni-InGaAs}$	Ni-InGaAs thickness	nm
T	Temperature	℃
T_d	Desorption Temperature	℃
T_{InGaAs}	InGaAs step height	nm
T_{mask}	SiO_2 mask thickness	nm
T_{total}	Total step height	nm
T_{Mo}	Mo thickness	nm
T_{ox}	Equivalent oxide thickness	nm
V_{FB}	Flatband voltage	V
V_G	Gate voltage	V
V_T or V_T'	Threshold voltage	V

ΔV_T	Threshold voltage shift	V
W	Contact width	μm
W_{eff}	Channel width	μm
W_{fin}	Fin width	nm
W_{top}	Fin top channel width	nm
W_{side}	Fin sidewall width	nm
ρ_C	Specific contact resistivity	$\Omega \cdot cm^2$
ρ_{III-V}	III-V resistivity	μΩ·cm
$\rho_{Ni-InGaAs}$	Ni-InGaAs resistivity	μΩ·cm
ρ_{Mo}	Mo resistivity	μΩ·cm
μ_{eff}	Effective mobility	$cm^2\ V^{-1}s^{-1}$
μ_e	Electron mobility	$cm^2\ V^{-1}s^{-1}$
μ_h	Hole mobility	$cm^2V^{-1}s^{-1}$
ϕ_S	Surface potential	eV
ϕ_{Bn}	Schottky barrier height	eV
Φ_{MS}	Work function difference between metal and semicondcutor	eV
ε_s	Permittivity	F/m

Chapter 1

Introduction

1.1 Silicon Transistor Scaling: Benefits and Challenges

The success of complementary metal-oxide-semiconductor (CMOS) technology is due to its scalability, which has enabled the number of transistors on integrated circuit (IC) chips to be increased exponentially during the past four decades [1.1],[1.2]. Continued scaling of the transistor dimension is required in order to achieve significantly higher packing density per unit chip area, reduction of cost per function, and improvement in circuit speed performance. A 45 nm process technology based on high-*k*, metal gate, and strained Silicon (Si) was introduced in 2007 [1.3]. Scaling of this technology continued to the 32 nm technology node in 2009 [1.4]. In the year of 2011, FinFET structure was also introduced to enable the scaling further down to the 22 nm technology node [1.5].

As transistors are aggressively scaled in accordance with Moore's law to sub-20 nm dimensions, it becomes increasingly difficult to maintain the required device performance. Currently, the increase in drive current for faster switching speed at lower supply voltage is largely at the expense of an exponentially growing leakage current, which leads to a large standby power dissipation [1.1]. If we look forward to the sub-10 nm node and beyond, the transistors are in the order of a few atoms across and continued shrinking of physical feature size will be imposed by fundamental

limits of Si properties. Therefore, there is an important need to explore novel channel materials and device structures that would provide us with equivalent scaling for CMOS.

1.2 High Electron Mobility of III-V Materials

To address the scaling challenges, both industry and academia have been investigating alternative materials and device architectures, among which III-V compound semiconductors stand out as promising candidates for future logic applications. This is because their light electron effective mass lead to high electron mobility and high on-current, which would translate into high device performance at low supply voltage. As seen in Table 1.1, III-V compound semiconductors have significantly smaller electron effective mass and higher electron mobility compared to Si [1.7].

Table 1.1. Carrier mobility, effective mass, bandgap and permittivity of some commonly used semiconductors [1.7].

	Si	**Ge**	**GaAs**	**$In_{0.53}Ga_{0.47}As$**	**InAs**	**InSb**
Electron mobility (cm^2/Vs)	1350	3900	8500	14000	33000	77000
Hole mobility (cm^2/Vs)	460	1900	400	400	460	850
Electron effective mass ($/m_0$)	0.19	0.082	0.067	0.05	0.027	0.013
Bandgap (eV)	1.12	0.66	1.42	0.74	0.36	0.17
Permitivity	11.8	16	12.4	13.9	14.8	17.7

1.3 Challenges of III-V CMOS Technology

III-V compound semiconductors have been heavily researched since they have been widely used in communications and optoelectronics industries. There are still a lot of challenges to be overcome before III-V logic transistors manufacturing becomes viable [1.7]. The intrinsic properties of III-V materials may add to the challenge of successful device realization. The success of III-V in potential CMOS technology will mainly depend on: 1) heterogeneous integration of III-V on Si in a cost-effective way, 2) formation of low leakage and thermally stable gate dielectric with low interface state density, 3) realization of low-resistance source and drain, and 4) p-channel materials with reasonably high hole mobility. These technical challenges are illustrated in Fig. 1.1, discussed and summarized in the following Sections.

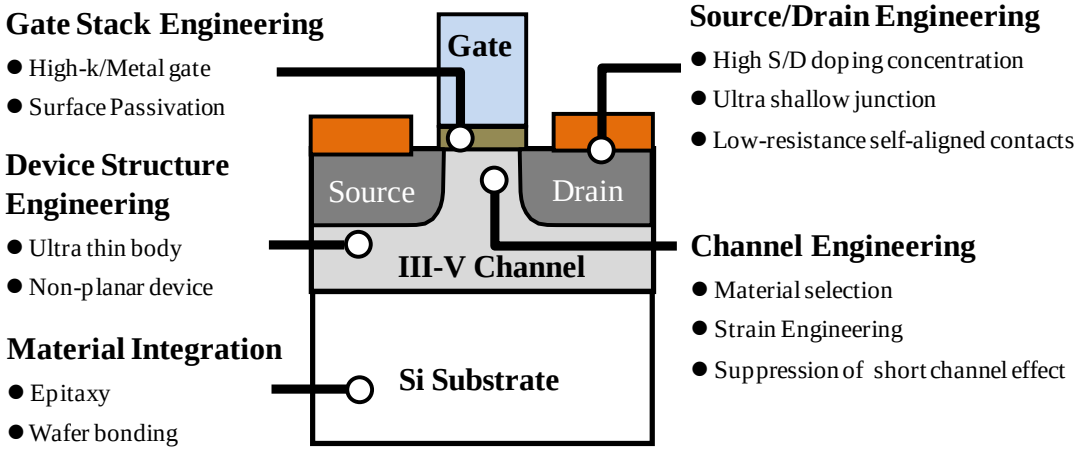

Fig. 1.1. Schematic illustration of the key technical challenges faced in the realization and integration of high mobility III-V CMOS on Si substrates for future logic applications.

1.3.1 Formation of High-Quality Gate Dielectric

Native oxide surface of III-V, for instance GaAs, consists of several oxides such as As_2O_3, As_2O_5, Ga_2O_3, Ga_2O_5, and Ga_2O [1.8],[1.9]. Unlike SiO_2 on Si, the native oxides of GaAs have very poor electrical properties and result in Fermi-level pinning and high interface state density (D_{IT}) [1.10].

Deposition of gate dielectric on III-V is being studied using various *in-situ* and *ex-situ* deposition methods. Passivation techniques such as *in-situ* molecular beam epitaxy (MBE) growth of gallium-gadolinium oxide (GGO) [1.11], metal organic chemical vapor deposition (MOCVD) of HfAlO and HfO_2 with SiH_4, NH_3, or PH_3 plasma treatment [1.12],[1.13], atomic layer deposition (ALD) of Al_2O_3, HfO_2, ZrO_2, (La)AlO_x/ZrO_2, and $TaSiO_x$ [1.14]-[1.21] employing Si, or InP capping layer [1.22]-[1.25] have been developed to reduce interface trap density and to unpin the III-V interfaces. However, the reported D_{IT} values on various MOS devices are still higher than 1×10^{11} $cm^{-2}eV^{-1}$ [1.7]. Further reduction of D_{IT} is still needed. In addition, thermally stable high-*k* dielectric is highly desirable to ensure that it remains high quality after subsequent thermal process steps such as S/D dopant activation anneal (600 - 800 ℃).

1.3.2 III-V Integration on Si Substrates

Bulk III-V substrates are costly, brittle, and difficult to make in large wafer sizes. Direct epitaxial growth of III-V materials on Si substrates is desirable for heterogeneous integration with Si CMOS technology. However, this poses serious

challenges due to the large mismatch in lattice constant (e.g. 8% between $In_{0.53}Ga_{0.47}As$ and Si), large mismatch in coefficient of thermal expansion, and the generation of polar/non-polar interfaces between III-V and Si. These challenges are being addressed by the use of III-V buffer layer growth, either on blanket or on patterned Si wafers, which reduces the number of defects reaching the active device layers [1.26]-[1.29].

Direct wafer bonding can be regarded as another promising technology to integrate III-V materials on Si, since the transfer of III-V semiconductor optical devices to Si wafers has been reported [1.7]. High quality III-V on insulator (III-V-OI) on Si was demonstrated recently using an electron-cyclotron-resonance (ECR) oxygen plasma-assisted direct wafer bonding process [1.30],[1.31]. Such III-V-OI substrates can provide process advantages for realizing new device structures such as III-V ultrathin body devices, FinFETs, and nanowire MOSFETs. However, the bonding of InGaAs on Si substrates is at the cost of sacrificing InP substrates [1.31] which are also costly. A cost-effective integration technology is still desired.

1.3.3 Channel Material Engineering

In general, III-V materials have significantly smaller bandgap compared to Si (Table 1.1). Due to the small bandgap in these high mobility materials, the band-to-band tunneling leakage current can become excessive and can ultimately limit the scalability of III-V MOSFETs. Therefore, ternary compound semiconductors such as InGaAs have received much attention due to their tunable and moderate bandgap.

Another point to note is that most III-V materials suffer from low hole mobility (Table. 1.1), although GaSb and InGaSb offer slightly higher hole mobility [1.32]. There is lack of p-channel materials with reasonably good carrier transport properties and there is a need to explore new III-V channel materials for p-MOSFETs.

1.3.4 New Device Structure Engineering

FinFET structure has been introduced for Si CMOS at the 22 nm technology node and would probably be extended to sub-20 nm technology nodes [1.5]. FinFET structure could provide improved short-channel effects (SCEs) control, enhanced volume inversion in the channel region, lower leakage current, and reduced device variability arising from random dopant fluctuation if low channel doping concentration is used. III-V FinFETs have been widely researched since the first III-V FinFET was experimentally demonstrated in 2009 [1.33]. III-V FinFETs are more scalable than III-V planar n-MOSFETs [1.33]-[1.39]. It is highly possible that III-V transistors will be used in the form of FinFETs in sub-10 nm nodes [1.1].

1.3.5 Source/Drain Resistance Engineering

A. Concept of Source/Drain Resistance Engineering

The drive current of a transistor is determined by device total resistance (R_T), which is the combination of transistor channel resistance (R_{CH}) and source/drain (S/D) series resistance (R_{SD}). To achieve high drive current, small R_T is desired and R_T can be express as:

$$R_T = R_{CH} + R_{SD}. \tag{1.1}$$

Schematic of a transistor in Fig. 1.2 shows the R_T between source and drain terminals is the summation of R_{CH}, source resistance (R_S), and drain resistance (R_D), where R_{SD} = R_S + R_D. R_{SD} will dominate R_T of a transistor if R_{CH} dramatically reduces with channel length scaling and channel mobility enhancement [1.40]. R_{SD} is projected to be comparable to R_{CH} at the 22 nm technology node and this implies that device performance would ultimately be limited by R_{SD} [1.41] beyond 22 nm technology node.

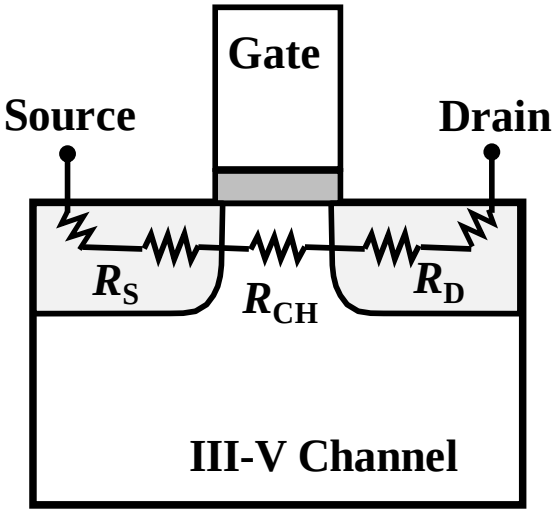

Fig. 1.2. Schematic of a transistor biased in the linear region, showing that total resistance R_T between source and drain terminals includes channel resistance R_{CH}, source resistance R_S and drain resistance R_D.

B. Components of Transistor Source/Drain Resistance

As illustrated in Fig. 1.3, the R_{SD} of a conventional III-V transistor can be mainly divided into two separate resistance components: 1) resistance of doped III-V S/D ($R_{III\text{-}V}$), and 2) contact resistance (R_C) between metal contact and III-V semiconductors. Assuming an ideal box-like doping profile, the resistance of the doped III-V S/D can be expressed as [1.42]:

$$R_{III-V} = \frac{\rho_{III-V} L_{SD}}{W_{eff} X_J}, \tag{1.2}$$

and

$$\rho_{III-V} = \frac{1}{N_A q \mu_h + N_D q \mu_e} \approx \frac{1}{N_D q \mu_e}, \tag{1.3}$$

where $\rho_{III\text{-}V}$ is the resistivity of doped III-V S/D, L_{SD} is separation between S/D contacts and channel, W_{eff} is device width, X_J is S/D junction depth, N_D and N_A are electron and hole carrier concentration, respectively, μ_e and μ_h are electron and hole carrier mobility, respectively. It is noticed that $R_{III\text{-}V}$ is strongly dependent on W_{eff}, X_J, L_{SD} and N_D (or N_A).

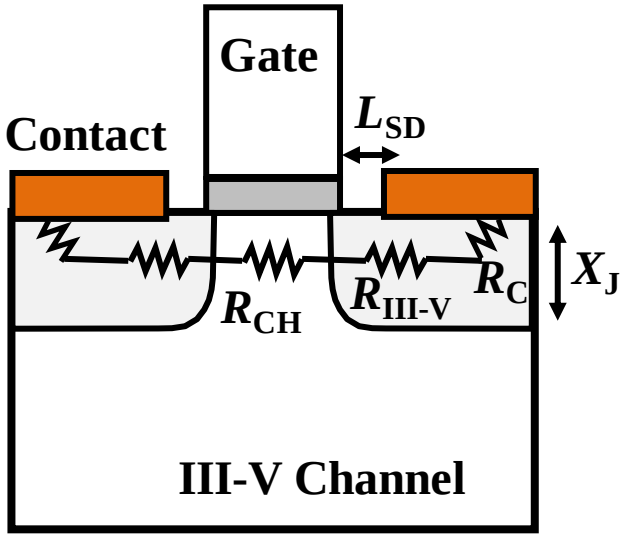

Fig. 1.3. Schematic of a conventional III-V transistor showing various resistance components that contribute to device R_{SD}, where $R_{SD} = 2(R_C + R_{III\text{-}V})$.

R_C depends on the specific contact resistivity (ρ_C), the sheet resistance of semiconductor (R_{sh}), the width W_{eff}, length (L) of the contact hole, and transfer length (L_T). R_C is given by [1.43]:

$$R_C = \frac{\sqrt{\rho_C R_{sh}}}{W_{eff}} \coth(\frac{L}{L_T}) . \tag{1.4}$$

For a metal-semiconductor junction with a high impurity doping concentration, the tunneling process will dominate and ρ_C is found to be [1.43]:

$$\rho_C \sim \exp[\frac{4\pi\sqrt{\varepsilon_s m_n^*}}{h} \frac{\phi_{Bn}}{\sqrt{N_D}}], \tag{1.5}$$

where π is the ratio of a circle's circumference to its diameter, ε_s is permittivity of a semiconductor, m_n^* is effective mass, ϕ_{Bn} is the schottky barrier height, h is Planck's constant, and N_D is semiconductor doping concentration. It is obvious that R_C is a strong function of N_D.

In summary, R_{III-V} and R_C are the two primary S/D resistance components of a typical III-V transistor and are strongly dependent on W_{eff}, X_J, N_D and L_{SD}. A small X_J is preferred to alleviate SCEs. In a FinFET, W_{eff} should also be kept small in order to achieve good control of SCEs. Small X_J and W_{eff} would lead to high R_{III-V} and R_C. Therefore, engineering the other parameters such as N_D and L_{SD} becomes important. Increased N_D and reduced L_{SD} could help reduce R_{III-V} as well as R_C, and thus reduce S/D series resistance.

C. State-of-Art III-V n-MOSEFTs Contact Technology

High mobility III-V n-MOSFETs require the shallow (small X_J), abrupt and highly doped (large N_D) n^+ source/drain. Si is widely used as the n-type dopant in III–V materials because of its negligible diffusivity which allows the realization of very abrupt junctions [1.44]. However, the maximum n-type carrier concentration in III-V materials, for instance InGaAs, with Si as dopants can only reach ~7×10^{18} cm^{-3} by direct Si implantation due to the low solid solubility limitation [1.45]. This doping level is far from the state-of-art doping concentration (in the order of 10^{21} cm^{-3}) achieved for Si. To obtain an active doping concentration over 5×10^{18} cm^{-3} in InGaAs, an activation anneal temperature of ~700 ℃ is required [1.45]. However, in certain device processing schemes a limited thermal budget is imposed. As an example, in a gate-first processing flow, the thermal stability of the gate stack limits the maximum activation anneal temperature. It becomes obvious that III-V transistors will suffer more from R_{SD} as compared with Si transistors since low N_D would result in high R_{SD}. *In-situ* doping is required to boost the S/D doping level to reduce R_{SD} [1.46],[1.47].

Gold-based contact materials such as TiPtAu and NiAuGe [1.12],[1.30], [1.33],[1.37],[1.48], [1.49] are commonly used for III-V MOSFETs. However, gold is a contaminant in Si CMOS technology and it may not be used for integration of III-V transistors in a Si CMOS process. Therefore, development of new contact materials which are low-resistance and CMOS compatible is highly desirable.

Unlike nickel salicide in Si CMOS process which is integrated based on a self-aligned technology [1.50], S/D contacts for III-V MOSFETs are non-self-aligned

and usually formed by direct deposition and patterning of metals using a lift-off process [1.12],[1.30],[1.33],[1.37],[1.48],[1.49]. Large spacing L_{SD} between the S/D contacts and the transistor channel is introduced and this gives a high $R_{III\text{-}V}$ resulting from the sheet resistance of III-V S/D [Equation (1.2)]. $R_{III\text{-}V}$ would contribute a significant portion to R_{SD} considering the high $\rho_{III\text{-}V}$ of III-V S/D due to the low N_D. Solutions to minimize this contribution will be even more crucial for the adoption of III-V FinFETs in the future technology generations. This is because device operation in a FinFET relies on the use of narrow fins (small W_{eff}) to control SCEs and the narrow fins would result in increased $R_{III\text{-}V}$ [Equation (1.2)]. The metallization of these narrow fins to maintain low sheet resistance at the S/D regions will be crucial for resistance reduction. Therefore, self-aligned S/D contacts which are adjacent to the gate stack could generate high conductivity path for local wiring and are desired to drastically reduce R_{SD}. A self-aligned contact technology would also reduce L_{SD} and provide better scalability for transistor footprint.

For the widespread adoption of the III-V MOSFETs in future CMOS technology generations, innovative S/D contact solutions for III-V planar MOSFETs or FinFETs must be developed to alleviate the concerns of high R_{SD}.

1.4 Objectives of Research

The objectives of this research are to address the source/drain resistance issue in nanoscale III-V planar n-MOSFETs and FinFETs. The main focus of this thesis is placed on exploring low-resistance, CMOS compatible contact materials as well as

developing new process technologies to realize self-aligned metallization for III-V n-MOSFETs. An extensive evaluation of contact technology options across various III-V n-MOSFETs such as GaAs planar transistors, InGaAs planar transistors, and InGaAs FinFETs is carried out to achieve low series resistance and high drive current. Ultimate motivation of realizing CMOS compatible, low-resistance self-aligned contacts for III-V n-MOSFETs was obtained. The results of this research will provide technology options for self-aligned metallization in III-V n-MOSFETs for the future technology generation nodes.

1.5 Thesis Organization

The III-V contact technologies developed in this thesis are documented in 4 Chapters. In Chapter 2, a NiGe-based self-aligned contact metallization technology for GaAs was developed. It is a "salicide-like" process and comprises a selective epitaxy of GeSi film on n^+ GaAs and a two-step metallization process. The NiGeSi ohmic contact technology is compatible with GaAs n-MOSFETs fabrication and was used for the integration of GaAs transistor. The demonstration of the "salicide-like" contact technology for III-V n-MOSFET is an important step towards realization of high performance logic devices based on III-V materials.

In Chapter 3, we developed a self-aligned Ni-InGaAs contact technology suitable for InGaAs n-MOSFETs. Ni-InGaAs as a new contact material was formed at low temperature, and its material and electrical properties were comprehensively studied showing promising results. This self-aligned Ni-InGaAs contact technology

was used in the integration of InGaAs planar n-MOSFETs and good electrical characteristics were achieved.

In Chapter 4, we realized InGaAs FinFETs using a gate-last process and also integrated Ni-InGaAs contacts in the FinFETs using a self-aligned metallization process developed in Chapter 3. With a well designed device structure, we achieved the combination of *in-situ* heavily doped n^+ InGaAs S/D and self-aligned Ni-InGaAs contacts. The InGaAs FinFETs shows low S/D series resistance and high drive current.

In Chapter 5, we introduced non-alloyed Mo contact for InGaAs FinFETs for achieving further reduction of series resistance. Mo show low contact resistance on *in-situ* doped S/D. By using a novel gate-last fabrication process, Mo contacts were formed and self-aligned to the device channel. Lowest series resistance of ~250 $\Omega\cdot\mu m$ was achieved for the InGaAs FinFETs. Integration of forming gas annealing (FGA) improved dual high-*k* dielectric HfO_2/Al_2O_3 in InGaAs FinFETs was also carried out to further improve the performance of InGaAs FinFETs.

Finally, the main contributions of this thesis and suggestions for future work are summarized in Chapter 6.

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Chapter 2

Self-Aligned NiGeSi Contacts for GaAs Channel n-MOSFETs

2.1 Introduction

III-V materials such as Gallium Arsenide (GaAs) have significantly higher electron mobility than Silicon (Si) and are attractive channel material candidates for n-channel metal-oxide-semiconductor field-effect transistors (n-MOSFETs) in future high-speed and low-power logic applications [2.1]-[2.16]. To realize high-performance III-V n-MOSFETs, low channel resistance and low parasitic series resistance (R_{SD}) in the source/drain (S/D) regions are required. Series resistance in the S/D regions includes the resistance in the doped S/D and the contact resistance R_C between the doped S/D and the contact material.

Contacts for III-V n-MOSFETs can be formed by direct deposition and patterning (e.g. lift-off) of metals on the doped S/D, with or without a subsequent alloying annealing [2.17]-[2.23]. Contact metallization in III-V n-MOSFETs is usually non-self-aligned with respect to the gate stack, unlike the self-aligned salicidation process in Si MOSFETs [2.24]. A spacing between the contact metal and the gate stack leads to increased R_{SD} that compromises drive current (I_{ON}) performance. III-V n-MOSFETs with self-aligned contacts are thus needed for reduction of R_{SD} and for scaling down transistor footprint [2.25],[2.26]. A height

selective etching process has been developed to achieve self-aligned contact for III-V n-MOSFETs [2.15],[2.16],[2.26]. However, the integration in Ref. [2.15], Ref. [2.16] and Ref. [2.26] relies on precise control of the etching back process which is very challenging and might not be suitable for manufacturing. A self-aligned metallization process, which is easy to control and analogous to the salicidation process in Si complementary metal-oxide-semiconductor (CMOS) technology, is still needed for III-V n-MOSFETs [2.27]-[2.29].

In this Chapter, we report the first demonstration of GaAs n-MOSFETs with self-aligned contact technology [2.28],[2.29]. The self-aligned contact was formed using a salicide-like process which is compatible with CMOS process flow. A new epitaxy process was developed to selectively form a thin continuous germanium-silicon (GeSi) layer on GaAs S/D regions. Nickel was deposited and the first annealing was performed to initiate the reaction between Ni and GeSi. Unreacted metal was removed by a selective wet etching. A second high temperature annealing diffuses Ge and/or Si atoms into GaAs to form heavily doped n^+ GaAs regions, and a novel self-aligned nickel germanosilicide (NiGeSi) ohmic contact was achieved. Finally, GaAs n-MOSFETs with the new self-aligned NiGeSi contacts were realized and characterized. Good electrical performance was achieved.

2.2 Development of Self-Aligned NiGeSi Contacts Technology

NiGe-based contact is attractive due to the low resistivity of NiGe (22 μΩ·cm) as compared with PdGe (30 μΩ·cm), the low cost of Ni, and the low germanide formation temperature [2.30]-[2.32] that is compatible with III-V materials. High contact formation temperatures could degrade the interface between III-V semiconductors and the gate dielectric. Transfer Length Method (TLM) test structures [2.33],[2.34] were fabricated for extraction of R_C using a process flow shown in Fig. 2.1 in the development of the self-aligned metallization technology. A thin continuous high-quality GeSi layer was first selectively grown on Si-doped n^+ GaAs regions [Fig. 2.1(b)]. Second, a two-step germano-silicide process was developed to form NiGeSi ohmic contacts on n^+ GaAs. Next, diluted hydrochloric acid (HCl) was employed for selective removal of unreacted Ni [Fig. 2.1(c)-(d)].

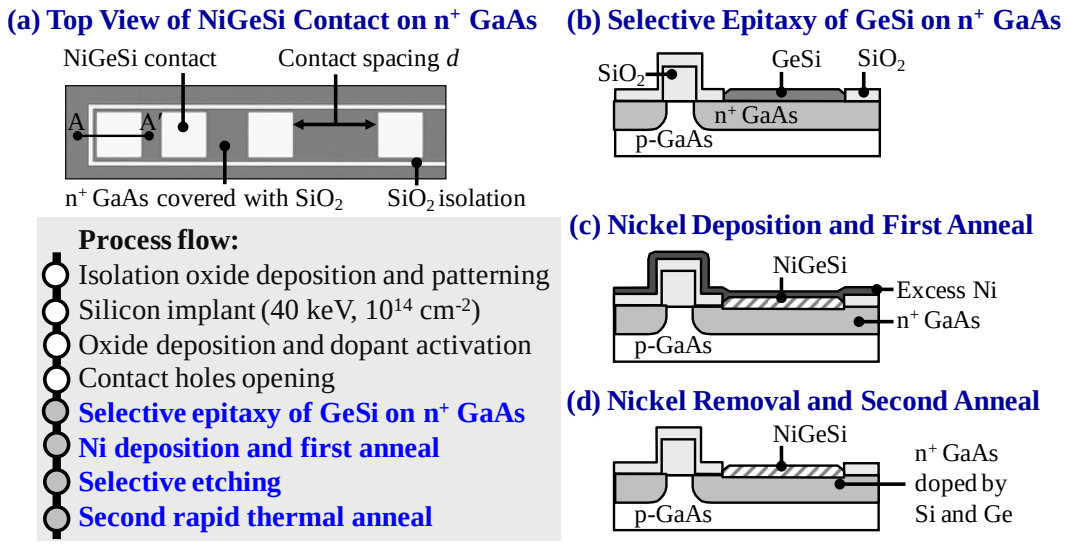

Fig. 2.1. (a) The plan-view optical microscopy image of a TLM structure. The self-aligned ohmic contact formation process comprises (b) selective epitaxy of GeSi on n^+ GaAs in a contact hole, (c) Ni deposition and a first thermal annealing for NiGeSi formation, (d) removal of excess Ni and a second thermal annealing to form the NiGeSi ohmic contact.

P-type (N_A ~5×10^{16} cm^{-3}) GaAs (100) substrates were used to fabricate the TLM test structures. A plasma-enhanced chemical vapor deposition (PECVD) SiO_2 isolation pattern was formed by wet etch using diluted hydrofluoric acid (HF) and then Si was implanted at an energy of 40 keV and a dose of 1×10^{14} cm^{-2}. The contact holes have dimensions of 100 μm ×100 μm. A thin capping layer of SiO_2 (~50 nm) was deposited before dopant activation annealing was performed at 850 ℃ for 10 s. Secondary Ion Mass Spectrometry (SIMS) characterization was carried out for both as-implanted sample and sample after dopant activation annealing to examine Si profiles. The profiles were shown in Fig. 2.2 (circles). We notice that implanted Si peak position is at depth of ~40 nm and Si dopants show negligible diffusion during the dopant activation annealing. Then SiO_2 cap was patterned and etched to define contact holes that exposed the n^+ GaAs surface for contact formation.

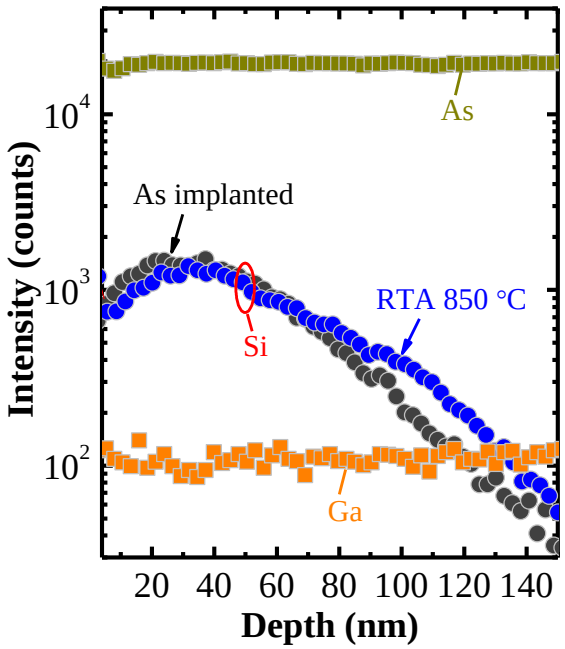

Fig. 2.2. SIMS analysis was performed to obtain the Si profiles (circles) of the samples before and after dopant activation annealing. Si dopants show negligible diffusion even after the dopant activation annealing at 850 ℃.

2.2.1 Selective Epitaxy of Germanium-Silicon (GeSi) on GaAs

An epitaxy process using ultra-high vacuum chemical vapor deposition (UHVCVD) was employed to selectively form a continuous GeSi film (~40 nm) on the n^+ GaAs surface in the contact holes [2.35]. The wafers were annealed in vacuum at desorption temperature (T_d) of 650 ℃ for native oxide desorption before being loaded into a GeSi growth chamber. Epitaxial growth was performed at 565 ℃ using Silane (SiH_4) and Germane (GeH_4) as precursors with the flow rate of 3 sccm and 5 sccm, respectively. The chamber pressure was maintained at 30 mTorr during the growth. SiH_4 flow was introduced during growth in an attempt to overcome the islanding issue which occurs when only GeH_4 precursor was used. Fig 2.3 plots the thickness of GeSi grown as a function of growth time. The growth was in the island mode at the initial stage (< 25 minutes) with slow growth rate. After that it entered into the blanket mode with a higher growth rate, implying the existence of growth incubation time during the expitaxy [2.35]. For eventual transistor integration, a target thickness of less than 50 nm is desired and the growth time is ~30 minutes.

It is found that growth of GeSi have a flatter surface morphology as compared to growth of pure Ge [2.35]. Ge islanding gives a discontinuous Ge film on n^+ GaAs and would cause Ni penetration into GaAs during a subsequent contact metallization step. This is expected to result in a non-uniform contact and high junction leakage due to Ni diffusion. It has been reported that NiGe formed on single crystalline Ge exhibits better uniformity and thermal stability than that formed on polycrystalline Ge [2.36]. Therefore, a continuous GeSi film with good single crystalline quality is crucial for NiGeSi contact formation.

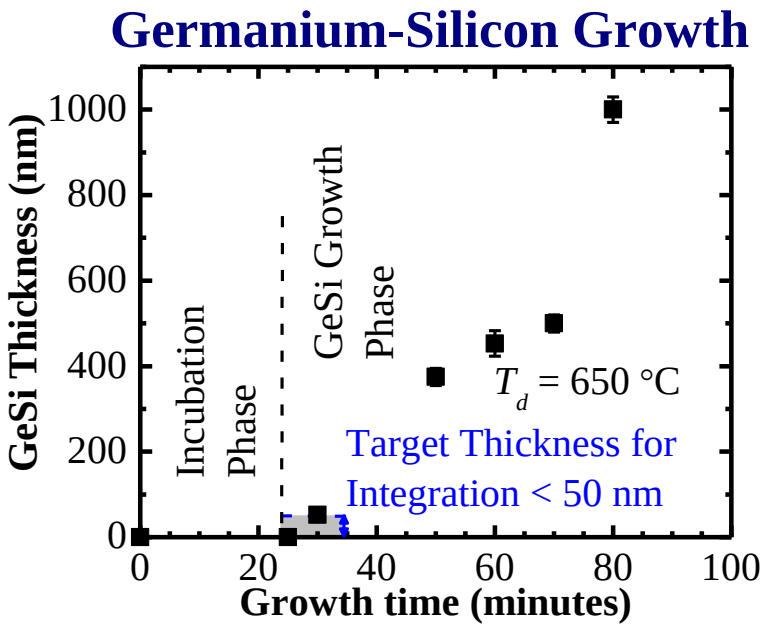

Fig. 2.3. Plot of GeSi thickness as a function of growth time. An incubation phase with a very slow growth rate is observed in the first 25 minutes. Once the growth enters into the growth phase, the growth rate for GeSi is much faster (> 10 nm/minute).

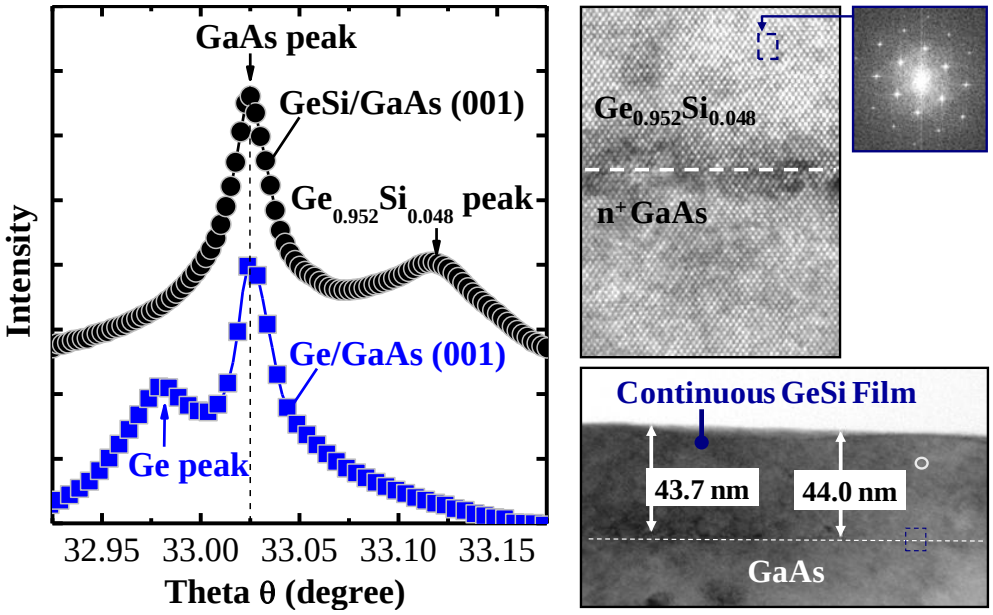

Fig. 2.4. (a) High resolution XRD shows that 4.8 atomic percent of Si was incorporated in GeSi. GeSi formed on GaAs is under tensile strain. (b) TEM images show the formed GeSi/GaAs heterostructure, and a diffractogram of a selected region enclosed by the dashed box indicates the good crystalline quality of GeSi.

The (004) diffraction peaks of the Ge and GeSi grown were clearly observed from the high resolution X-Ray Diffraction (XRD) plot [Fig. 2.4 (a)]. The values of full-width-at-half-maximum (FWHM) are 0.02 and 0.037 degree for the Ge and $Ge_{0.952}Si_{0.048}$ films, respectively, suggesting that the crystal quality is better for a smaller lattice mismatch between the epilayer and GaAs. XRD spectra indicates that Ge (lattice constant = 5.6577 Å) film on GaAs (lattice constant = 5.6537 Å) is under a slight compressive strain with $2\theta = 32.981°$ while fully relaxed Ge has a 2θ of 33.0°. However, GeSi film on GaAs is fully tensile strained with $2\theta = 33.118°$ and the composition is extracted to be $Ge_{0.952}Si_{0.048}$ by fitting XRD spectra using X'Pert Epitaxy. Peak shift of Raman spectroscopy from 301 cm^{-1} for Ge/GaAs to 298.9 cm^{-1} for GeSi/GaAs was also observed, consistent with the strain and composition of the epilayers.

Transmission Electron Microscopy (TEM) images in Fig. 2.4(b) indicate that the single-crystalline GeSi was uniformly formed with a thickness of ~44 nm and was free from dislocations. A zoomed-in view in Fig. 2.4(b) also shows the abrupt interface between GeSi and GaAs. Fast Fourier transform (FFT) diffractogram [Fig. 2.4(b)] also reveals the good crystalline quality of the GeSi epitaxial layer.

2.2.2 Two-Step Metallization Process for NiGeSi Contacts Formation

Single crystalline GeSi film (40~50 nm) was grown on blanket GaAs substrate followed by deposition of Ni (~30 nm) by sputtering. The structure of the sample is illustrated in the Fig. 2.5 inset. The Ni/GeSi/GaAs wafer was then cut into pieces and each piece went through rapid thermal annealing (RTA) at a fixed temperature for 60 s for the formation of NiGeSi. The RTA temperature ranges from 150 ℃ to 600 ℃. The sheet resistance (R_{sh}) of NiGeSi formed at various annealing temperatures was investigated. A four-point probe was used to measure R_{sh}. XRD was performed to analyze the nickel germanide phase transformation.

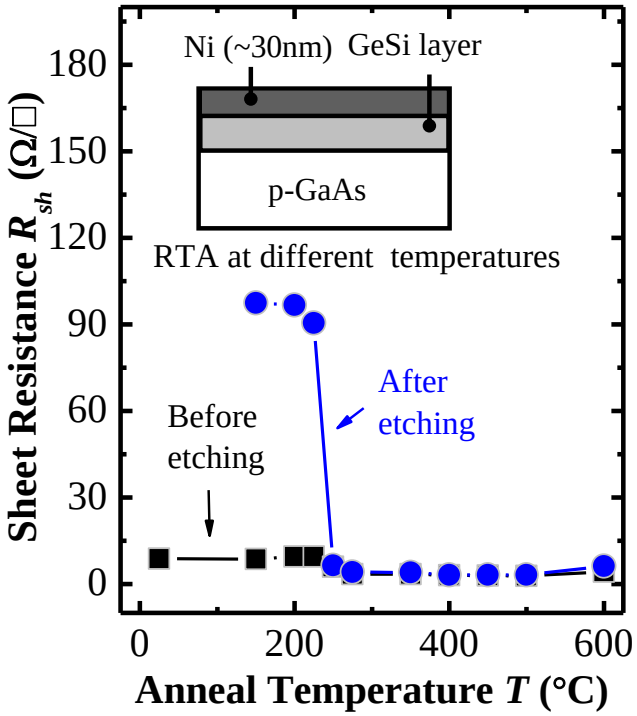

Fig. 2.5. Sheet resistance versus annealing temperature for ~30 nm Ni on blanket GeSi/GaAs sample. The annealing time was fixed at 60 s. The sheet resistance values of annealed samples with and without selective etching in HCl are indicated by square and circle symbols, respectively. Nickel germanosilicide formed at above 250 ℃ has a low sheet resistance. At temperatures below 225 ℃, no reaction between Ni and GeSi took place.

Fig. 2.5 shows the R_{sh} of NiGeSi/GaAs samples right after RTA (square symbols) at different temperatures. The R_{sh} of the as-deposited sample was 8.7 Ω/□. After annealing at 200 ℃ to 225 ℃, R_{sh} was slightly increased to 9.5 Ω/□, due to Ni consumption and Ni_5Ge_3 formation (Fig. 2.6). Ni_5Ge_3 has a higher resistivity than the deposited Ni film. Nickel monogermanide (NiGe), a low resistivity phase, started to form at 250 ℃ and R_{sh} decreased to 5.9 Ω/□. Both Ni_5Ge_3 and NiGe phases exist when the samples were annealed at 250 ℃. When the annealing temperature was increased above 275 ℃, only the NiGe phase existed, and the lowest R_{sh} of 2.8 Ω/□ was achieved at annealing temperatures of 450 ℃ and 500 ℃. NiGe (111), (121), (120), (021). (211), (002), and (301) peaks can be observed (Fig. 2.6). When the annealing temperature was increased further to 600 ℃, R_{sh} increased to 4.3 Ω/□, due to the effects of agglomeration [2.36].

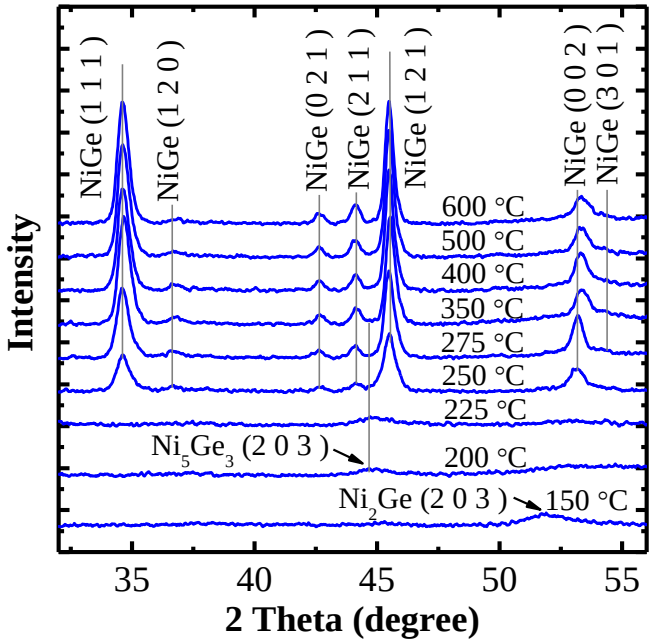

Fig. 2.6. XRD spectra shows nickel germanide phases formed from 150 ℃ and 600 ℃. The spectra indicates that NiGe started to form at annealing temperature of 250 ℃ and confirms that only NiGe phase was formed at annealing temperatures above 275 ℃.

A selective etch process for removing excess Ni was developed to enable integration of self-aligned NiGeSi S/D contacts for GaAs n-MOSFETs. Dilute HCl (HCl: H_2O = 1: 10) could achieve good etch selectivity of Ni over nickel germanide and thus was employed to remove the unreacted Ni. The R_{sh} values of NiGeSi/GaAs samples after the HCl etch are also shown in Fig. 2.5 (circle symbols). The R_{sh} increased significantly to ~95 Ω/□ after the selective etch for samples which were annealed below 225 ℃. This is because most of the Ni was still unreacted and was removed by the subsequent HCl dip. However, Ni was completely consumed and nickel germanide (Ni_5Ge_3 and NiGe) was formed when the annealing temperature was over 250 ℃, giving low R_{sh} even after the selective etch step.

A two-step contact metallization process for ohmic contact formation on n^+ GaAs was conceived in this Chapter. A brief dilute HF dip was performed to remove the native oxide of GeSi prior to sputtering of Ni (~30 nm). A first anneal at the temperature of 250 ℃ was then performed to consume all of the Ni on GeSi by forming nickel germanide (Ni_5Ge_3 and NiGe). Unreacted Ni on SiO_2 was subsequently selectively removed by HCl. After the first annealing, we found that the nickel germanide does not form an ohmic contact to the underlying GaAs yet. A second high temperature RTA at 500 ℃ was then performed to convert the nickel germanide phases into the nickel monogermanide (NiGe) phase, which achieves an ohmic contact with GaAs and also a low R_{sh}.

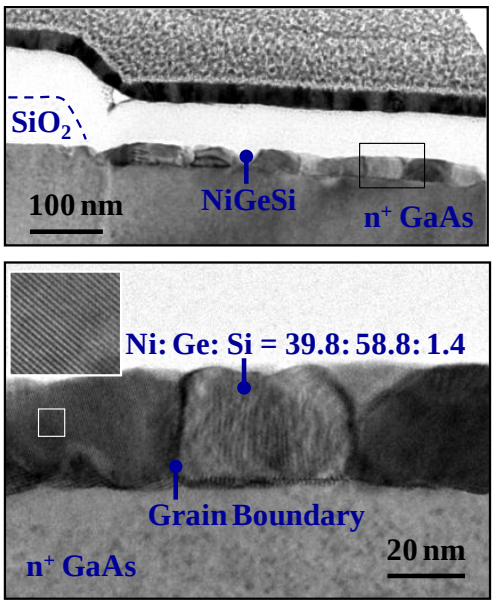

Fig. 2.7. Cross-sectional TEM image (top) of a TLM structure shows the formation of poly-crystalline NiGeSi on n^+ GaAs that is not covered by SiO_2. No Ge or NiGeSi was observed on the SiO_2 region, which confirmed the selectivity of GeSi epitaxy. A zoomed-in view (bottom) showing several grains of NiGeSi. A high-resolution TEM image of a portion of a NiGeSi grain is shown on the inset.

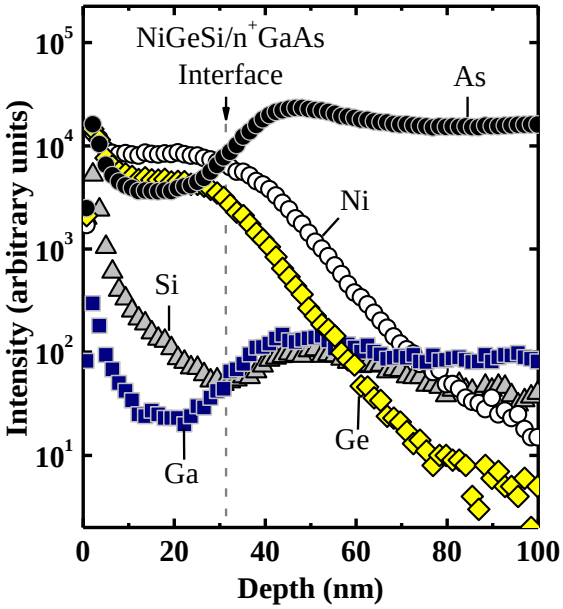

Fig. 2.8. SIMS analysis of NiGeSi contact on n^+ GaAs showing the elemental distribution of Si, Ge, Ga, As, and Ni. The interface between NiGeSi and GaAs is indicated by the dashed vertical line. The NiGeSi thickness is ~30 nm.

Fig. 2.1(a) shows the top-view of a TLM structure with NiGeSi contacts on n^+ GaAs. TEM analysis of a portion (A-A') of the TLM structure (Fig. 2.7) clearly shows the poly-crystalline structure of NiGeSi, which has a thickness of ~30 nm. No nickel germanide was observed on the SiO_2 region, indicating good selectivity of GeSi epitaxy. High Resolution TEM image shows good uniformity of the NiGeSi layer and several grains of NiGeSi could be observed clearly, showing a distinct interface between NiGeSi and GaAs. Energy Dispersive x-Ray Spectrometry (EDX) indicates the approximate NiGeSi atomic composition ratio of Ni: Ge: Si = 39.8: 58.8: 1.4. SIMS analysis performed on the NiGeSi/n^+GaAs contact shows the elemental distribution of Ga, As, Ni, Ge, and Si, as plotted in Fig. 2.8. A NiGeSi layer was clearly observed and the gray dashed line represents the estimated position of the NiGeSi/GaAs interface. The thickness of NiGeSi obtained from SIMS characterization is quite consistent with that obtained from TEM in Fig. 2.7.

2.2.3 Electrical Characterization and Discussion

After the first annealing at 250 ℃ and selective removal of unreacted Ni, the current-voltage (*I-V*) curve measured between two adjacent germanosilicide (Ni_5Ge_3, NiGe) contacts in a TLM structure does not show ohmic behavior as shown in Fig. 2.9(a). A second high temperature annealing at 500 ℃ converted the nickel germanide phases into a low resistivity nickel monogermanide phase, and probably helped to drive Ge and/or Si atoms diffusion into GaAs. Therefore ohmic contact was achieved after the second high temperature annealing. Ge has been also reported to dope GaAs heavily through interdiffusion between Ge and GaAs [2.22]. A Ge-rich

GaAs interfacial layer right beneath the NiGeSi was also detected by EDX. For a metal-semiconductor junction with a high impurity doping concentration, increasing the n-type doping concentration in GaAs can help to achieve ohmic contact with low specific contact resistivity ρ_C since the tunneling process will dominate ρ_C. Specific contact resistivity ρ_C can be written as [2.34]:

$$\rho_C \sim \exp[\frac{4\pi\sqrt{\varepsilon_s m_n^*}}{h}\frac{\phi_{Bn}}{\sqrt{N_D}}], \tag{2.1}$$

where π is the ratio of a circle's circumference to its diameter, ε_s is permittivity of semiconductor, m_n^* is effective mass, ϕ_{Bn} is the schottky barrier height, h is Planck's constant, and N_D is semiconductor doping concentration. ρ_C is a very strong function of N_D. Contact resistance R_C depends on the specific contact resistivity ρ_C, the sheet resistance of the S/D region R_{sh}, the width W and length L of the contact hole, and the transfer length L_T, as given by [2.34]:

$$R_C = \frac{\sqrt{\rho_C R_{sh}}}{W}\coth(\frac{L}{L_T}). \tag{2.2}$$

To further understand the ohmic contact formation, a model was proposed to explain the mechanism of NiGeSi contacts in this Chapter. The first low temperature (250 ℃) annealing helps Ni react with GeSi to form nickel germanide compound. However, at this stage, the contact is still not ohmic yet, as shown in Fig. 2.9(a). During the second annealing at higher temperature (500 ℃), mono-nickel germanide was formed and GeSi will diffuse into the underlying GaAs and form a heavily doped n^+ GaAs interfacial layer. From the band diagram illustrated in Fig. 2.9(b), such a heavily doped n^+ GaAs layer can enhance the field emission of electrons through the barrier and therefore ohmic contact was formed.

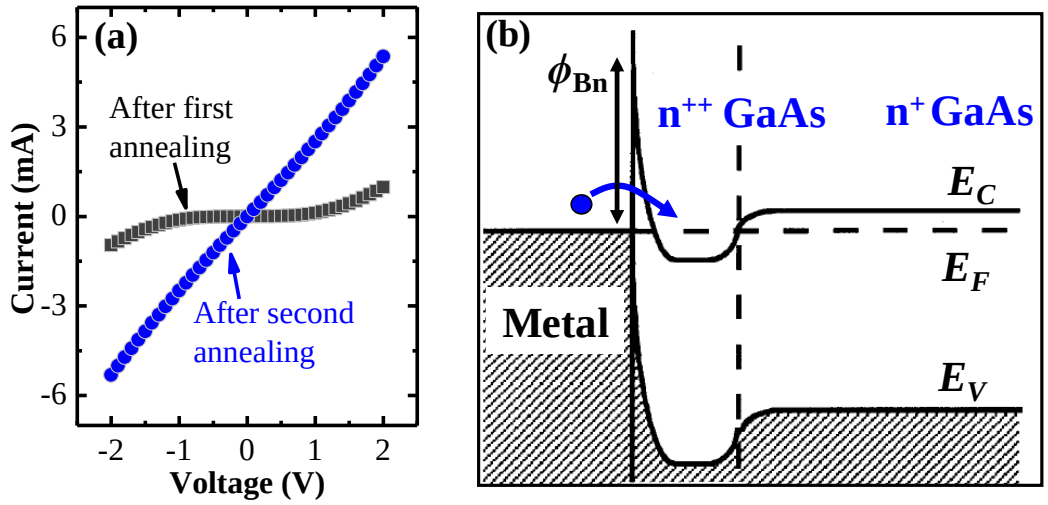

Fig. 2.9. (a) *I-V* characteristics of NiGeSi before and after the second annealing. (b) Band diagram shows that a heavily doped n^+ GaAs layer can enhance the field emission of electrons through the barrier. This helps formation of an ohmic contact.

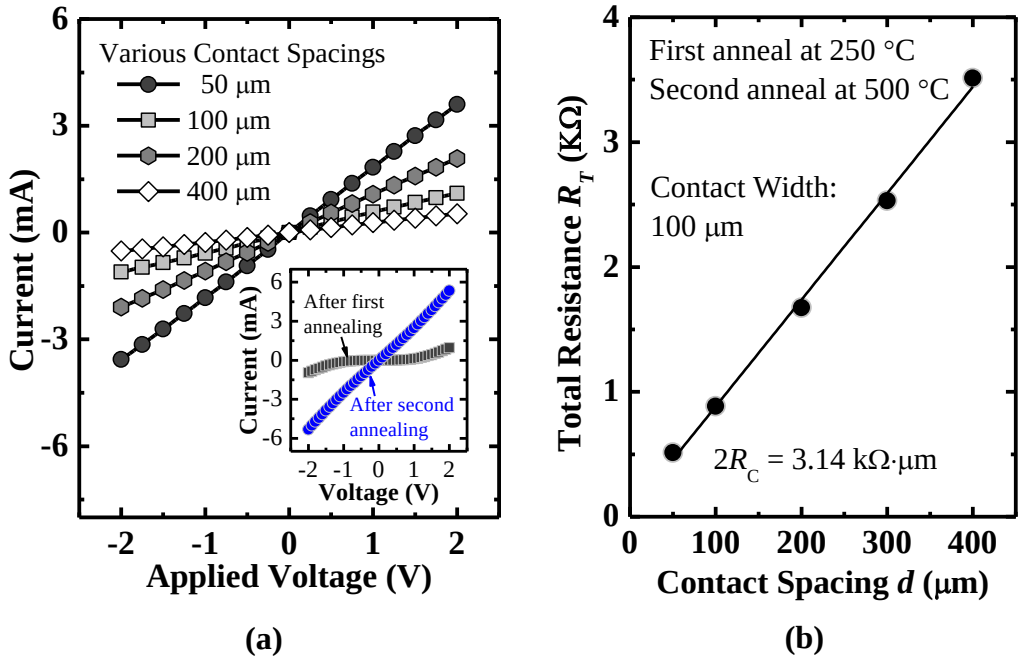

Fig. 2.10. (a) *I-V* curves measured between NiGeSi contacts with different contact spacing d formed on n^+ GaAs. Excellent ohmic behavior is observed. (b) Plot of total resistance R_T between two NiGeSi contacts as a function of the contact spacing d. The extracted contact resistance R_C is 1.57 kΩ·μm.

After the two-step metallization, NiGeSi ohmic contacts were obtained, as shown in Fig. 2.10(a). *I-V* characteristics were measured between two adjacent NiGeSi/n^{+}GaAs contact pads separated by various contact spacings *d*. The total resistance R_T between two contacts decreases linearly with decreasing *d*. By plotting R_T versus *d*, as shown in Fig. 2.10(b), one can extract the contact resistance R_C from the intercept of the linear fitting line with the vertical axis and the sheet resistance $R_{sh,GaAs}$ of the doped substrate from the line slope. Extracted R_C and $R_{sh,GaAs}$ were ~1.57 kΩ·μm and 852 Ω/□, respectively. Both contact length *L* and contact width *W* of the TLM are 100 μm and thus the assumption of $L > 1.5L_T$ is valid, where L_T is transfer length. The specific contact resistivity ρ_C could be obtained by $\rho_C \approx R_C L_T W$ [2.34]. The calculated $\rho_C = 2.9 \times 10^{-5}\ \Omega\cdot cm^2$.

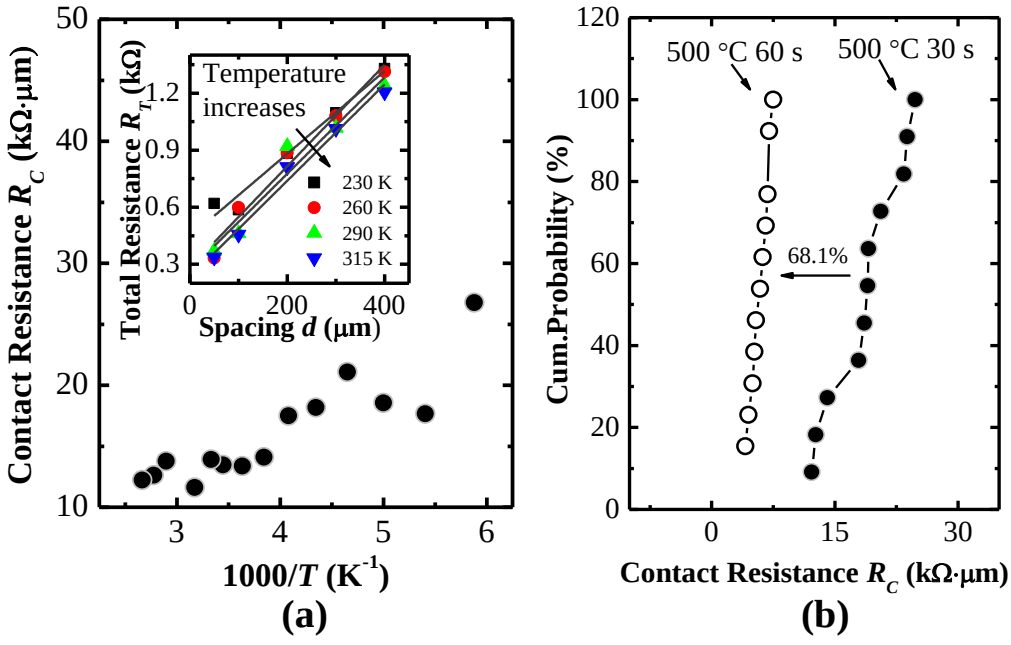

Fig. 2.11. (a) Reduction of R_C with increasing measurement temperature was observed due to increased charge injection by thermionic emission. Inset shows R_T as a function of *d* at various temperatures. (b) Cumulative distribution of contact resistance gives the statistical summary of R_C. 68.1% R_C reduction was achieved by extending the second annealing duration.

Low temperature measurement was performed to investigate the effect of temperature (T) on R_C as shown in Fig. 2.11(a). The inset shows total resistance R_T as a function of contact spacing d at various temperatures. R_C was found to decrease with increasing temperature from 170 K to 375 K, due to higher thermionic emission rate at elevated temperature. For thermionic emission, the temperature dependence of specific contact resistivity ρ_C could be described as [2.34]:

$$\rho_C = \frac{k}{qA^*T}\exp(\frac{q\phi_{Bn}}{kT}), \tag{2.3}$$

where k is Boltzmann's constant, q is electronic charge, A^* is Richardson's constant, and ϕ_{Bn} is Schottky barrier height. From Equation (2.3), ρ_C is strongly dependent on the measurement temperature and a higher temperature would lead to a lower contact resistance. This is in good agreement with our observation in Fig. 2.11(a).

We found that extending the duration of the second annealing could further improve the contact resistance as well as the contact resistance variation. Statistical data indicates that increasing the duration of the second annealing (500 ℃) from 30 s to 60 s leads to a 68.1% reduction in R_C [Fig 2.11(b)]. This is probably because the longer second annealing could further facilitate the diffusion of Ge and/or Si atoms into GaAs and lead to even higher doping in GaAs interfacial layer. The increased doping would result in lower contact resistance as indicated by abovementioned Equations (2.1) and (2.2).

2.3 Device Integration and Characterization

2.3.1 Integration of Self-aligned NiGeSi Contacts on GaAs n-MOSFETs

The schematic and key process steps for integrating self-aligned NiGeSi contacts in a GaAs channel n-MOSFET are shown in Fig. 2.12. Undoped (100) GaAs substrates served as starting substrates. Prior to high-*k* dielectric deposition, hydrochloric acid (HCl：H_2O = 1: 3) and ammonium hydroxide (NH_4OH: H_2O = 1: 10) solutions were used to remove native oxide and excess arsenic on the GaAs surface. Ammonium sulfide [$(NH_4)_2S$] solution was used for passivating the GaAs surface, effectively suppressing surface oxidation. After pre-gate cleaning, the wafers were quickly loaded into a multiple-chamber gate cluster system, where a 600 ˚C vacuum anneal (VA), SiH_4 and NH_3 passivation (570 ˚C), and MOCVD deposition (576 ˚C) of HfAlO (~25 nm) were performed. After post-gate dielectric deposition anneal at 525 ˚C for 60 s, ~130 nm tantalum nitride (TaN) was deposited by sputtering and ~ 30 nm PECVD SiO_2 hard mask was deposited on top of TaN. The purpose of the SiO_2 hard mask is to cover the top surface of the TaN gate during the GeSi growth on GaAs S/D. This also prevented the possible contamination of the growth chamber during the GeSi growth. Then, SiO_2/TaN layer was patterned by optical lithography and finally etched by Cl_2-based plasma to form the gate electrode.

S/D implantation (Si: 10 keV, 1×10^{14} cm^{-2} and 50 keV, 1×10^{14} cm^{-2}) was carried out. After the device was capped with a thin layer of SiO_2, an 850℃ RTA was used to activate the implanted Si dopant. The capped SiO_2 layer was used to prevent the III-V elements from out diffusion during the high temperature thermal annealing and was removed by dilute HF subsequently. Then, SiON spacer was

formed by deposition of SiON and CHF_3 based plasma etch. The developed selective epitaxy process was employed to form single-crystalline GeSi (~40 nm) on the GaAs S/D regions after *in-situ* surface cleaning and treatment, as illustrated in Fig. 2.12(b). Good GeSi morphology and selectivity over the SiO_2 hard mask and SiON spacer can be achieved. Then, the two-step metallization process was carried out to form self-aligned NiGeSi contacts, as shown in Fig. 2.12(c). After Ni (~30 nm) deposition, a first RTA at 250 ˚C was performed followed by selective wet etch of unreacted Ni. After that, a RTA at 500 ˚C for 60 s was done to realize NiGeSi ohmic contacts.

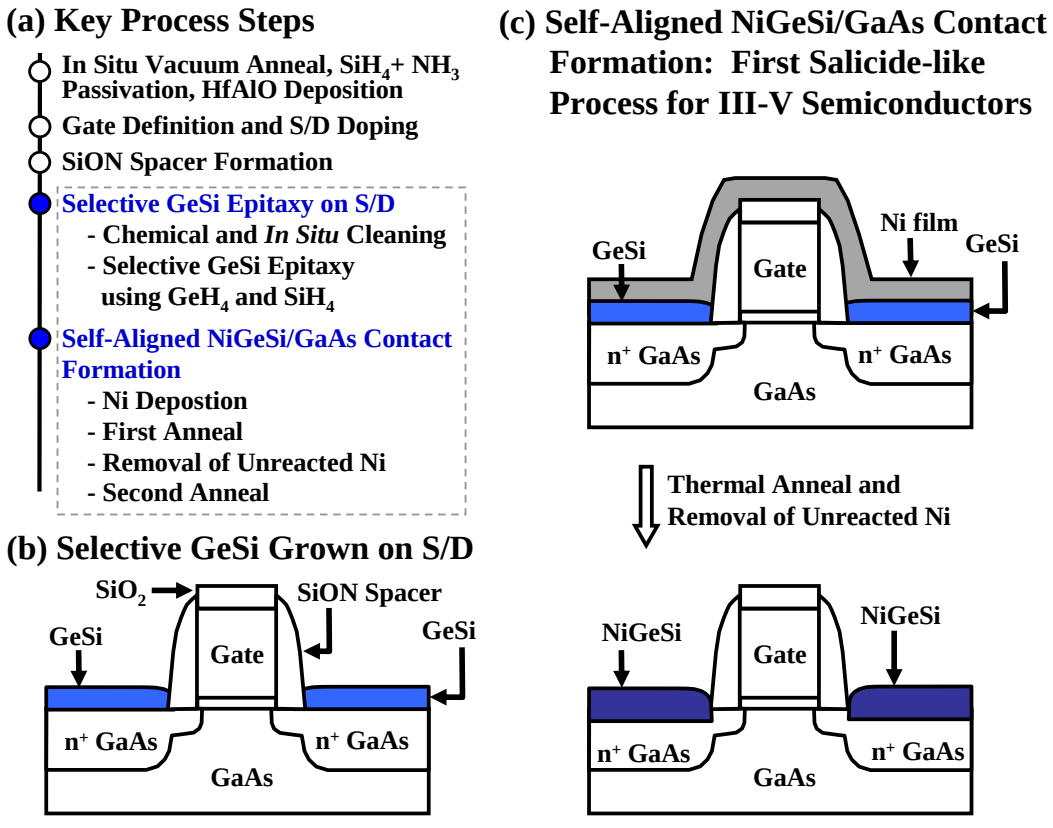

Fig. 2.12. (a) Key process steps for first technology demonstration of III-V n-MOSFETs with 'salicide-like' self-aligned contact. (b) An epitaxy process for forming thin continuous GeSi layer on GaAs S/D regions was employed, followed by (c) Ni deposition and a novel two-step annealing process to form NiGeSi ohmic contacts on GaAs.

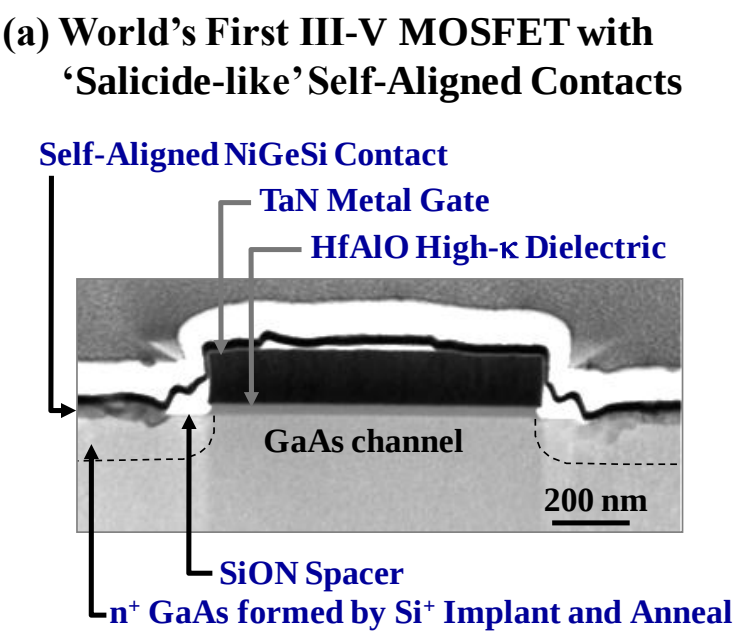

Fig. 2.13. (a) TEM image of the world's first III-V n-MOSFET with 'salicide-like' self-aligned contacts. NiGeSi ohmic contacts were formed adjacent to the gate. TaN metal-gate on HfAlO high-κ dielectric stack was used. (b) Zoomed-in view of the NiGeSi formed on the Si implanted and annealed n^+ GaAs S/D regions. A SiH_4+NH_3 passivation technique was used to form high-quality gate dielectric on GaAs. Insets show high resolution TEM images of NiGeSi and gate stack.

2.3.2 Device Characterization and Analysis

Fig. 2.13 shows TEM images of a GaAs transistor with self-aligned NiGeSi contacts. The device has a gate length of 800 nm and gate width of 100 μm. TaN metal gate and HfAlO high-*k* dielectric with thickness of ~130 nm and ~25 nm were observed. The NiGeSi contacts are well-formed and self-aligned to the gate and spacers, as shown in Fig. 2.13(a). The dash line indicates the GaAs n^+ junction formed by Si implantation and dopant activation annealing. A zoomed-in view of the gate stack and self-aligned NiGeSi contact is shown in Fig. 2.13(b). High resolution TEM image indicates that the NiGeSi is poly-crystalline and has a thickness of ~40 nm. EDX was performed showing that the approximate Ni: Ge atomic ratio is ~ 44: 56.

The devices with self-aligned contacts were electrically characterized and show good output characteristics. Fig. 2.14(a) shows the threshold voltage (V_T) dependence on device gate length L_G. V_T was extracted using the linear extrapolation method at low drain voltage V_D of 0.1 V. V_T roll-off was observed for devices with gate length ranging from 0.2 to 0.7 μm. The statistical distribution of subthreshold swing (*S*) of over 30 GaAs n-MOSFETs is shown in Fig. 2.14(b), indicating an average value of ~270 mV/decade. There is still much room to further improve *S* by scaling down equivalent oxide thickness (EOT) since the 25-nm HfAlO has a large EOT of ~7 nm, which could be described by [2.37]:

$$S = \ln(10)\frac{kT}{q}(1+\frac{C_d}{C_{ox}}), \qquad (2.4)$$

where *k* is Boltzmann's constant, *T* is temperature, *q* is electronic charge, C_d is depletion layer capacitance, and C_{ox} is gate dielectric capacitance.

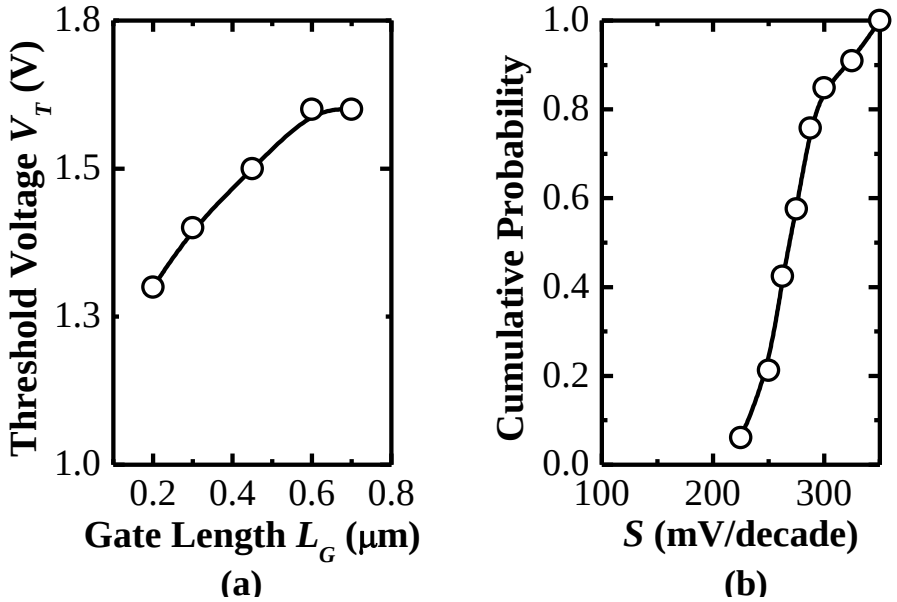

Fig. 2.14. (a) Dependence of the threshold voltage on the gate length L_G, and (b) statistical plot of the subthreshold swing S extracted at V_D = 0.1 V for a set of 33 n-MOSFETs with L_G ranging from 0.2 to 1 μm.

Fig. 2.15(a) plots the I_D-V_G characteristics of a n-MOSFET with gate length of 500 nm and gate width of 100 μm, showing good transfer characteristics with on-state/off-state drain current ratio of over 10^4. Drain voltage of 0.1 V and 0.8 V were applied. Fig. 2.15(b) plots the I_D-V_D characteristics of the same device, showing good saturation and pinch-off characteristics. Gate overdrive V_G-V_T was varied from 0 V to 2.5 V in steps of 0.5 V. I_D-V_D curves of another GaAs transistor with a smaller gate length of 300 nm also shows good output characteristics. We notice a significant increase in drive current when the device gate length was reduced from 500 nm to 300 nm (Fig. 2.16). A reduced transistor gate length improves the device current drive capability. The device with a 300 nm gate length also shows worse short channel effects as compared with the device with 500 nm gate length in Fig. 2.15. This is expected when the device gate length is scaled down [2.37].

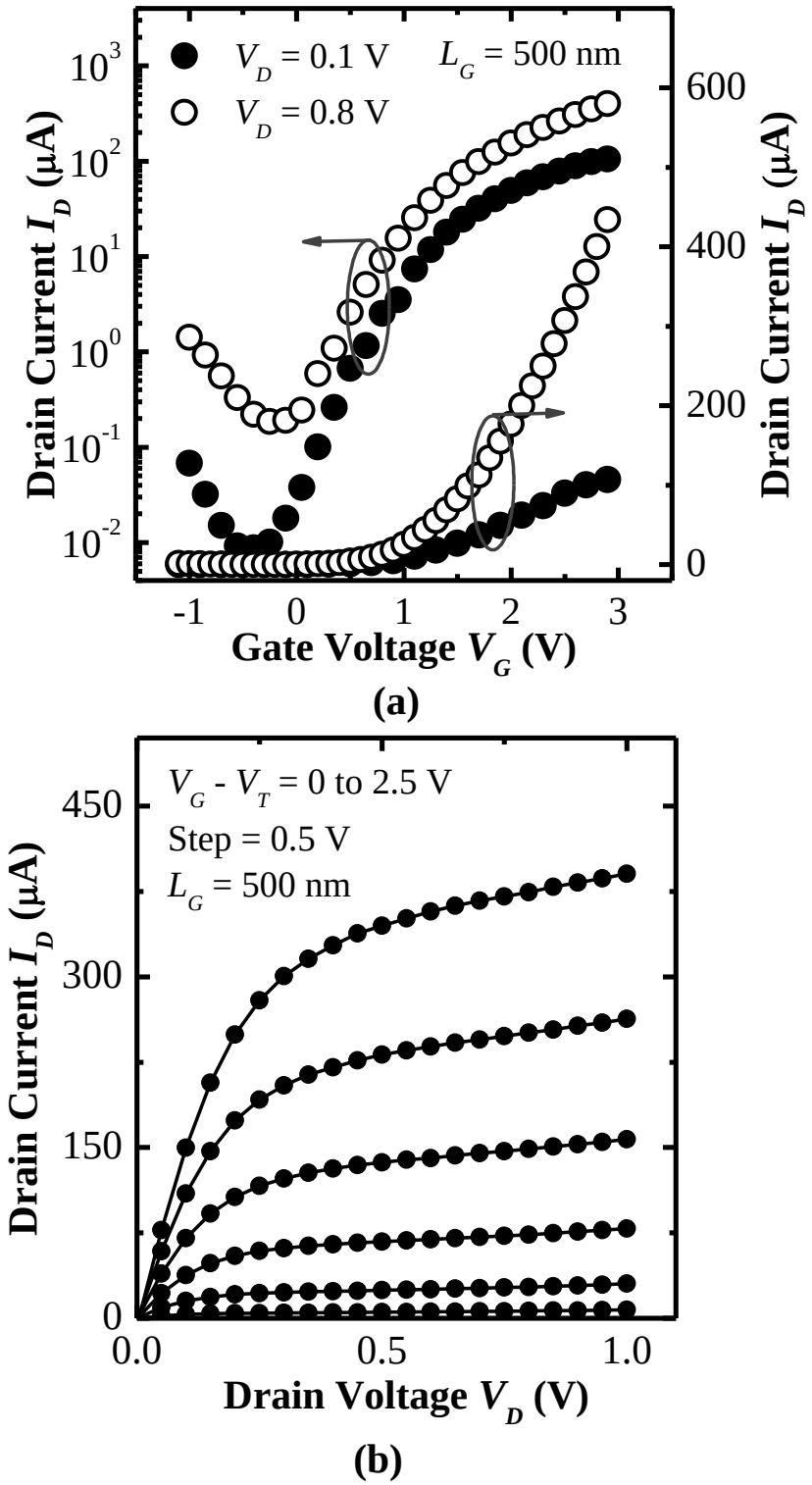

Fig. 2.15. (a) I_D-V_G curves of an inversion-mode GaAs n-MOSFET with self-aligned NiGeSi contacts, gate length of 500 nm, and gate width of 100 μm, showing good transfer characteristics. (b) I_D-V_D plot of the same device at various gate overdrive.

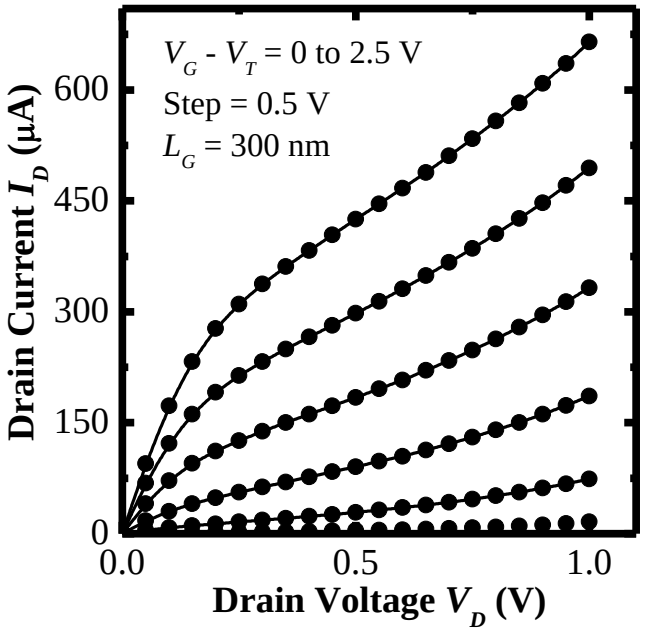

Fig. 2.16. I_D-V_D curves of another GaAs transistor with self-aligned NiGeSi contacts, showing good output characteristics. Device has a gate length of 300 nm, and a gate width of 100 μm, showing higher drive current as compared with the device in Fig. 2.15.

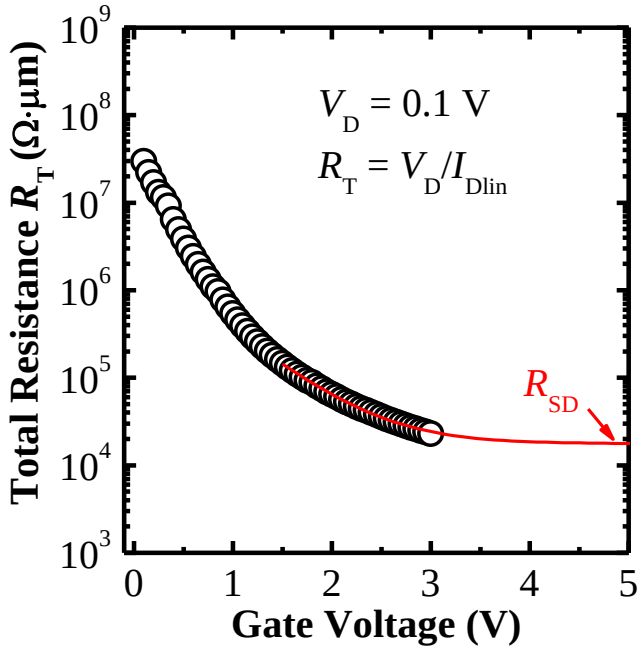

Fig. 2.17. Total resistance R_T as a function of gate voltage for the same device in Fig. 2.15. $R_T = V_D/I_{Dlin}$ and I_{Dlin} is drain current at linear regime (V_D = 0.1 V). Device channel resistance was modulated by applied gate voltage, leading to reduction of device total resistance with increased gate voltage.

Fig. 2.17 plots the total resistance (R_T) in the linear regime (V_D = 0.1 V) as a function of gate voltage for the same device in Fig. 2.15. The equation for the solid curve (red line) in Fig. 2.17 is given by [2.34]:

$$R_T = R_{SD} + R_{CH} = R_{SD} + L_G[W_{eff}\mu_{eff}C_{ox}(V_G-V_T)]^{-1}, \qquad (2.5)$$

where R_{CH} is channel resistance, L_G and W_{eff} are the device gate length and gate width, respectively, μ_{eff} is channel effective mobility, C_{ox} is gate dielectric capacitance, and V_G-V_T is gate overdrive. Equation (2.5) was used to fit the data points as shown by circles in Fig. 2.17. During the data fitting, μ_{eff} is assumed to be constant in the region of strong inversion. This would lead to a slight overestimation of extracted R_{SD}. The fitted curve was extrapolated to a large V_G = 5 V to obtain the value of R_{SD}, which is ~17 kΩ·μm. The obtained average R_C from a number of TLM structures (second annealing at 500 ℃, 60 s) is ~6 kΩ·μm as obtained from Fig. 2.11(b). The NiGeSi contact resistance in the source and drain regions would contribute ~12 kΩ·μm which takes up 70% of the device series resistance R_{SD}. The rest of the resistance components contributing 30% of R_{SD} come from NiGeSi sheet resistance, n^+ GaAs sheet resistance under spacer and spreading resistance in n^+ GaAs source and drain regions. As a first demonstration, the devices with self-aligned NiGeSi contacts still suffer from high R_{SD} and large EOT, leading to a low drive current in this Chapter. Further device optimization is still needed to achieve better drive current performance. In Ref. [2.15] and Ref. [2.16], InGaAs transistors have self-aligned Mo contacts on n^+ InAs S/D formed by MBE regrowth. Although the authors expected a R_{SD} of 600 Ω-um from the TLM data, yet the actual device electrical characteristics

showed an extremely high R_{SD} of over 1000 kΩ-um. The high R_{SD} is due to the inability to regrow low resistance epitaxial InGaAs and a gap region with no regrowth next to the gate, as explained by the authors. In Ref. [2.26], gold based material (NiAuGe) was used as the S/D contact material and the device showed relatively low R_{SD} of 1.4 kΩ-um. Although these contact technologies may achieve even lower R_{SD} with further optimization, yet the integration in Ref. [2.15], Ref. [2.16] and Ref. [2.26] relies on precise control of the etching back process. This is very challenging and might not be suitable for manufacturing. In addition, gold based contact material is not CMOS compatible.

Gate leakage current density J_G was measured by sweeping the gate voltage with the source and drain grounded, as illustrated in Fig. 2.18 inset. The low gate dielectric leakage current density suggests that the metallization process did not degrade the gate stack. This indicates that the self-aligned metallization process is compatible with the GaAs transistor fabrication process and promising for future device integration.

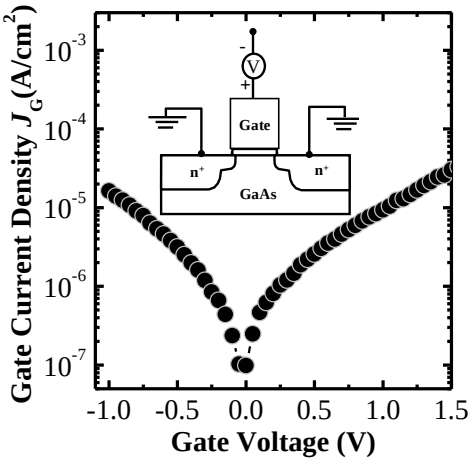

Fig. 2.18. Small gate leakage current density J_G was measured and normalized by gate area, indicating that the thermal steps of metallization are compatible with the TaN/HfAlO gate stack.

2.4 Summary

A self-aligned ohmic contact metallization technology for GaAs was developed. A continuous and single crystalline GeSi film was selectively grown on n^+ GaAs for forming a NiGe-based contact using a two-step metallization process. Ohmic contact behavior of NiGeSi on n^+ GaAs regions was obtained and contact resistance R_C as low as 1.57 kΩ·μm was also achieved from TLM structures. The NiGeSi ohmic contact technology is compatible with GaAs n-MOSFETs fabrication and was used for the integration of GaAs transistor. The devices with self-aligned NiGeSi contacts show good transfer and output characteristics. This Chapter demonstrated the availability of self-aligned contact technology for III-V n-MOSFETs, which is an important step towards realization of high performance logic devices based on III-V materials.

2.5 References

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Chapter 3

Self-Aligned Ni-InGaAs Contacts for InGaAs Channel n-MOSFETs

3.1 Introduction

Indium Gallium Arsenide (InGaAs) has even higher electron mobility than GaAs and is more attractive as a channel material for n-channel MOSFETs (n-MOSFETs) beyond the 22 nm technology node [3.1]-[3.17]. Much progress and very promising results on gate stack and interface engineering for InGaAs n-MOSFETs have been achieved recently [3.18]-[3.29]. To realize high performance InGaAs channel n-MOSFETs, reliable and low-resistance ohmic contacts to n^+ InGaAs source/drain (S/D) also need to be developed [3.30]-[3.46]. In addition, self-alignment of the S/D contacts to the gate electrode is desirable for reduced S/D access resistances and for achieving reduced transistor footprint.

In Chapter 2 of this thesis, a self-aligned NiGeSi contact metallization comprising selective epitaxy of GeSi and two-step metallization has been developed for GaAs n-MOSFETs. However, this technology is not suitable for InGaAs n-MOSFETs integration due to two reasons: 1) Selective growth of GeSi on InGaAs is very challenging; 2) The thermal budget of GeSi growth process (650 ℃ for oxide desorption and 565 ℃ for growth) is too high for the InGaAs gate stack if a gate-first fabrication process is used. Therefore, a self-aligned metallization process for

InGaAs n-MOSFETs as simple as and similar to the salicidation process in Si CMOS technology is still unavailable and strongly desired.

In this Chapter, we report the development of a self-aligned Nickel Indium Gallium Arsenide (Ni-InGaAs) metallization process for InGaAs channel n-MOSFETs. The self-aligned metallization process comprises conversion of sputtered Ni film on InGaAs into a uniform Ni-InGaAs film by rapid thermal annealing (RTA) and removal of unreacted Ni by selective wet etch. Ni-InGaAs contacts were characterized by using high resolution Transmission Electron Microscopy (TEM), Energy-dispersive X-ray spectroscopy (EDX), X-Ray Diffraction (XRD) and Secondary Ion Mass Spectroscopy (SIMS). The electrical properties of the contacts were also investigated by microscopic 4-point probe and Transfer Length Method (TLM) test structures. The self-aligned Ni-InGaAs contacts were finally integrated in InGaAs channel n-MOSFETs with dopant-less S/D (i.e. metallic S/D, no Si doping in S/D) and doped S/D, respectively. Both devices show good transfer and output characteristics. As compared with transistors with metallic Ni-InGaAs S/D, devices with Ni-InGaAs contacts formed on Si-doped S/D show significantly improved off-state current I_{OFF}. Device series resistance (R_{SD}) was extracted and various resistance components that contributed to R_{SD} were also investigated.

3.2 Development of Self-Aligned Ni-InGaAs Contact Technology

3.2.1 Reaction of Ni with InGaAs

Starting substrates comprise a 500 nm thick p-type $In_{0.53}Ga_{0.47}As$ (N_A ~2×10^{16} cm^{-3}) grown on bulk InP and were purchased from an expitaxy vendor. After native oxide removal in hydrochloric acid (HCl: H_2O = 1: 3), 30 nm of Ni was deposited on the wafer by sputtering. The wafer was then cut into pieces, and each piece went through RTA at a fixed temperature for 60 s in N_2 ambient. The anneal temperature was varied among the samples.

Sheet resistance R_{sh} was measured by 4-point probe right after the Ni-on-InGaAs (denoted as "Ni/InGaAs") samples were annealed at various temperatures (150 - 400 ℃). Fig. 3.1 shows the R_{sh} of Ni/InGaAs samples as a function of annealing temperatures (squares). The sample structure is illustrated in the inset. R_{sh} of the samples is similar to that of the as-deposited Ni/InGaAs sample (~11 Ω/square) when RTA temperature is below 250 ℃. However, R_{sh} increases to ~18 Ω/square when annealing temperature is at or above 250 ℃, indicating that reaction between Ni and InGaAs is initiated at about 250 ℃. The reaction converts the deposited Ni film into a Ni-InGaAs film which has higher resistivity than Ni and thus leads to an increase of R_{sh}. The reaction between Ni and InGaAs was controlled by diffusion of Ni atoms into InGaAs during RTA and a similar reaction between Ni and InAs was also reported by Chueh *et al.* [3.47]. Ni reacts with InAs to form a compound of Ni, In, and As which forms an ohmic contact on n-type InAs [3.48].

As a low temperature of ~250 ℃ is used for Ni-InGaAs formation, a metallization process involving Ni-InGaAs would incur a low thermal budget. This is

advantageous for maintaining the integrity of the gate stack on InGaAs using a gate-first fabrication process flow.

A wet etch was also developed to selectively remove unreacted Ni. In our etch study, it is found that the etch rate of Ni-InGaAs film in concentrated HCl (37% weight per volume) is less than 5 nm/minute while the etch rate of Ni is over 60 nm/minute. An etch selectivity of ~15 for Ni over Ni-InGaAs can be achieved by using concentrated HCl [3.49]. Ni-InGaAs samples exhibit low sheet resistance even after etching in concentrated HCl for 30 s, as shown in Fig. 3.1 (circles). However, for Ni/InGaAs annealed at or below 250 ℃, there was no metallic film on the sample surface after the HCl etch. The R_{sh} measured is huge (> 20 kΩ/square), and is that of p-InGaAs.

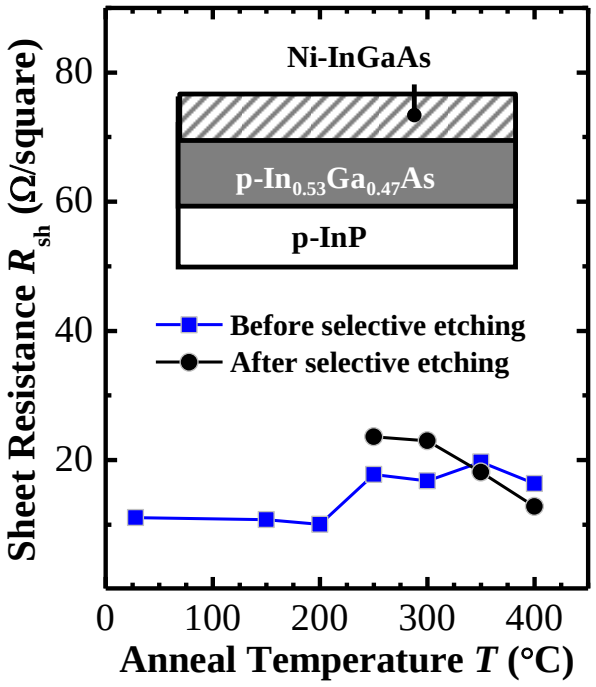

Fig. 3.1. Sheet resistance of the Ni/InGaAs samples was measured right after annealing at different temperatures (squares) for 60 s. After selective etch, sheet resistance was also measured (circles). Ni-InGaAs is formed when the temperature is above 250 ℃ and shows a low sheet resistance even after the selective etching in concentrated HCl solution.

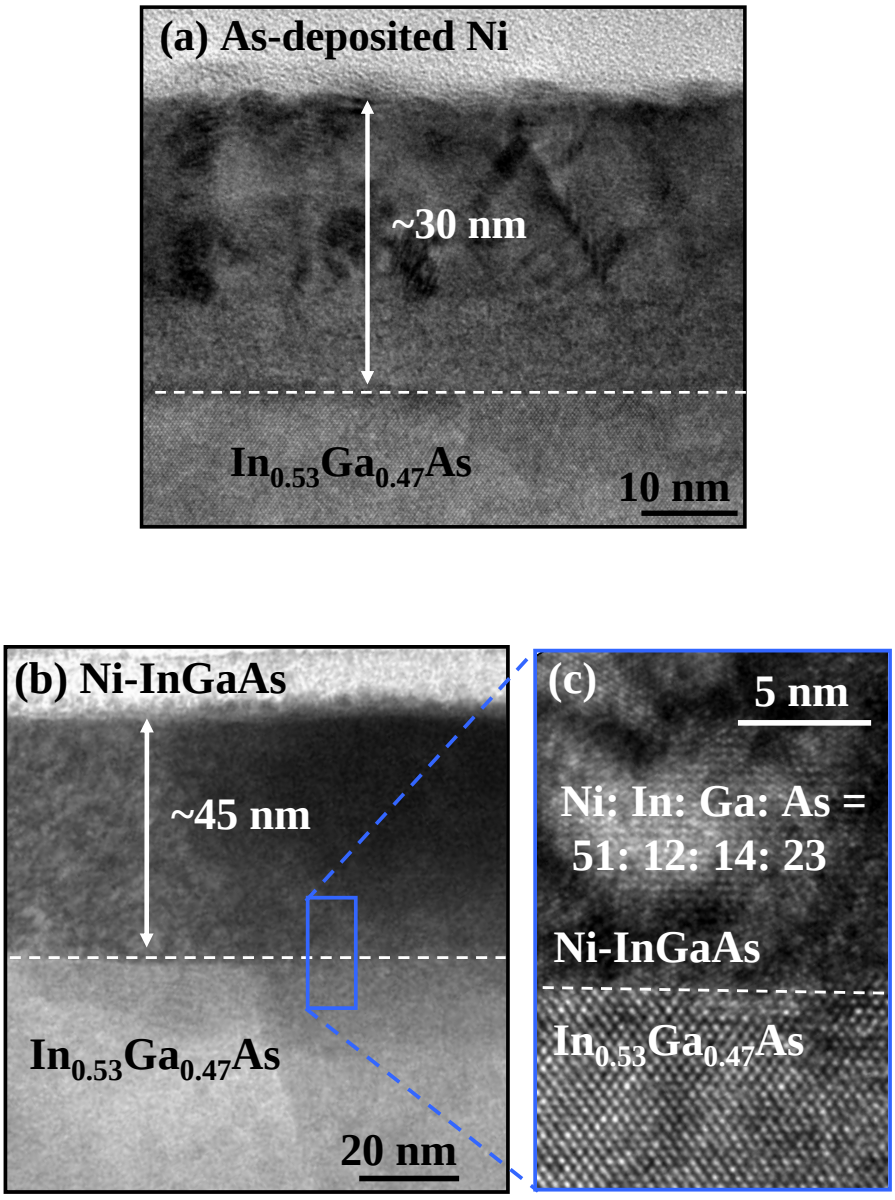

Fig. 3.2. (a) A ~30 nm polycrystalline Ni film was deposited on InGaAs substrate. (b) After RTA at 250 ℃ for 60 s, a ~45 nm Ni-InGaAs film was uniformly formed with darker contrast with respect to the substrate. (c) High resolution TEM shows the zoomed-in view of the Ni-InGaAs/InGaAs interface, featuring a very abrupt interface. Ni-InGaAs has a crystalline structure with an approximate atomic composition of Ni: In: Ga: As = 51: 12: 14: 23.

Fig. 3.2(a) shows a TEM image of ~30 nm as-deposited Ni on single crystalline p-InGaAs. The Ni film has a poly-crystalline structure. After RTA at 250 ℃ for 60 s, the 30 nm Ni reacted InGaAs to form a ~45 nm thick Ni-InGaAs film with good uniformity, as shown in Fig. 3.2(b). The contrast between Ni-InGaAs and InGaAs is good, and the interface between Ni-InGaAs and InGaAs can be clearly seen in Fig. 3.2(b). A high resolution TEM in Fig. 3.2(c) shows a zoomed-in view of the interface. The Ni-InGaAs layer also has a crystalline structure. EDX characterization at localized spots in the Ni-InGaAs film was performed to check the Ni-InGaAs composition. The Ni-InGaAs layer was found to have a Ni: In: Ga: As atomic ratio of 51: 12: 14: 23.

XRD General Area Detector Diffraction System scan (GADDS) was performed on as-deposited Ni/InGaAs sample as well as Ni/InGaAs samples after 200 and 250 ℃ annealing. The XRD spectrum is shown in Fig. 3.3(a). As-deposited Ni/InGaAs sample as well as Ni/InGaAs sample annealed at 200 ℃ for 60 s show the Ni (111) peak. The ring in the distributed intensity (inset A) indicates the poly-crystalline nature of the Ni film. This implies that Ni does not react with InGaAs at 200 ℃ and is confirmed by TEM characterization. However, when Ni/InGaAs went through a 250 ℃ anneal, the Ni (111) peak disappears and a new peak related to Ni-InGaAs is observed. The high intensity and well defined spot as shown in inset B indicate that the Ni-InGaAs has a preferred orientation. SIMS in Fig. 3.3(b) shows the elemental distribution of Ni, In, Ga, and As for Ni-InGaAs formed using a 250 ℃ 60 s anneal. The SIMS profile also shows a uniform elemental distribution in Ni-

InGaAs. The vertical grey line indicates the estimated position of the interface between Ni-InGaAs film and the InGaAs substrate.

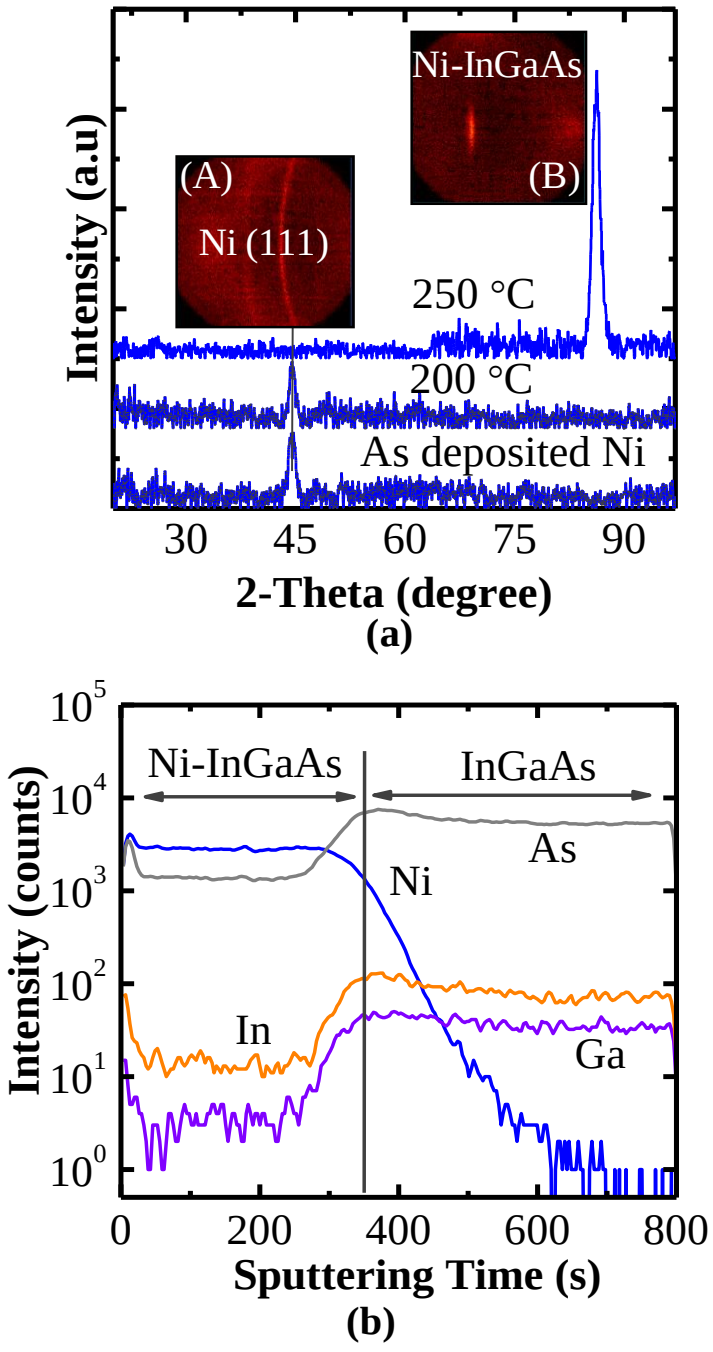

Fig. 3.3. (a) XRD indicating that as-deposited Ni/InGaAs sample and Ni/InGaAs sample annealed at 200 ℃ for 60 s have ploy-crystalline Ni and that Ni-InGaAs was formed after the sample was annealed at 250 ℃. (b) SIMS profile shows the elemental distribution and confirms the formation of Ni-InGaAs.

3.2.2 Electrical Properties of Ni-InGaAs Contacts

The electrical properties of Ni-InGaAs film were further investigated. Sheet resistance mapping of the ~45 nm thick Ni-InGaAs film was performed using a microscopic 4-point probe, in which the adjacent probe tips are separated by ~10 μm (Fig. 3.4). R_{sh} measurement was taken at 121 locations in a 11×11 matrix with a separation of 100 μm in both *x* and *y* directions. The distribution of R_{sh} of Ni-InGaAs in a 1 mm × 1 mm area is plotted in Fig. 3.4. R_{sh} values range from 20.4 to 22.4 Ω/square with an average of 21.3 Ω/square. The R_{sh} distribution is tight with standard deviation smaller than 0.4 Ω/square across the 1 mm × 1 mm area. This is consistent with the TEM results indicating a very uniform Ni-InGaAs thickness ($t_{Ni\text{-}InGaAs}$). Using $\rho_{Ni\text{-}InGaAs} = R_{sh} \times t_{Ni\text{-}InGaAs,}$ the resistivity of the Ni-InGaAs film was calculated to be ~96 μΩ·cm (R_{sh} value of 21.3 Ω/square and $t_{Ni\text{-}InGaAs}$ of 45 nm were used).

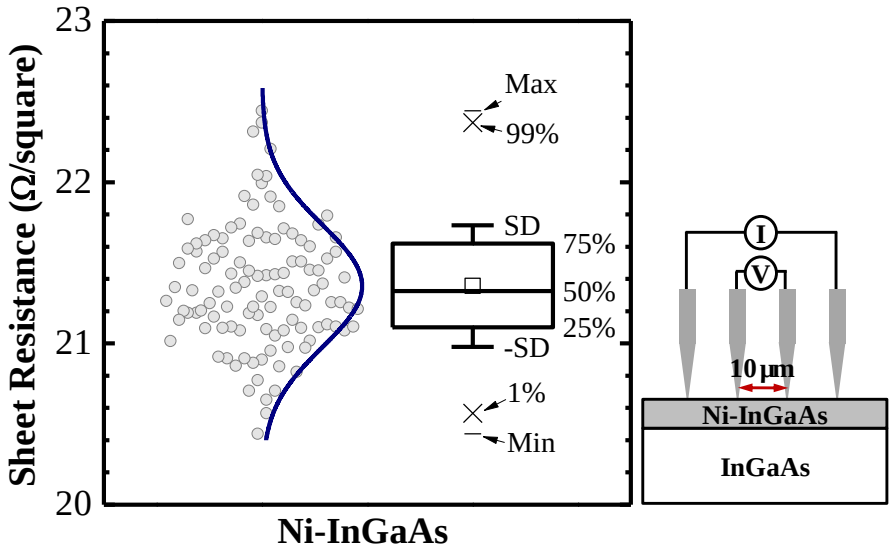

Fig. 3.4. The cumulative plot shows R_{sh} distribution in area of 1 mm × 1 mm for the Ni-InGaAs film. R_{sh} mapping was performed using microscopic 4-point probe. R_{sh} distribution ranges from 20.4–22.4 Ω/square, with an average of 21.3 Ω/square.

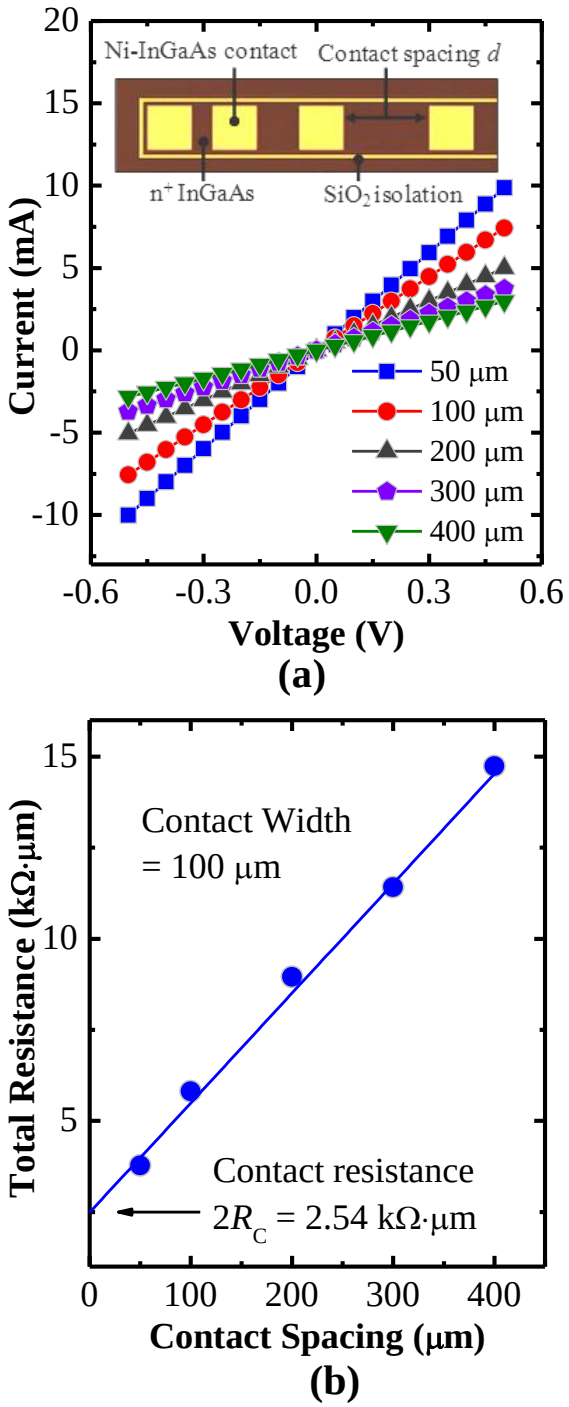

Fig. 3.5. (a) The inset shows the top view of the TLM structure with Ni-InGaAs contacts formed on n^+ InGaAs, as obtained by optical microscopy. *I-V* characteristics were measured between two adjacent Ni-InGaAs contact pads separated by various contact spacings *d*, showing good ohmic behavior. (b) Contact resistance R_C was extracted from the intercept of the linear fitting line with the vertical axis and the sheet resistance $R_{sh,InGaAs}$ of the n^+ InGaAs from the line slope.

The work function of Ni-InGaAs and the band alignment between Ni-InGaAs and InGaAs were investigated using photoelectron spectroscopy and the vacuum work function of Ni-InGaAs is obtained to be ~5.1 eV using ultra-violet spectroscopy (UPS) [3.50]. In addition, it was observed that the Fermi level of Ni-InGaAs is pinned to near the conduction band of InGaAs. For Ni-InGaAs formed on p-type InGaAs, this gives a Schottky contact with a hole barrier height of 0.8 ± 0.1 eV [3.50]. Ni-InGaAs would tend to form an ohmic contact on n-type InGaAs.

TLM test structures were fabricated to enable the extraction of contact resistance R_C of Ni-InGaAs on n^+ InGaAs. Si-doped n-InGaAs well was formed by Si^+ implant at an energy of 40 keV and a dose of 1×10^{14} cm^{-2}. The projected Si^+ implant depth and straggle are 40 nm and 21 nm as simulated by Stopping and Range of Ions in Matter (SRIM) [3.51]. A thin capping layer of SiO_2 (~30 nm) was then deposited before dopant activation at 600 ℃ for 60 s. The purpose of the SiO_2 was to prevent dopant out-diffusion during dopant activation anneal. The active carrier concentration N_D at similar Si^+ implant and activation annealing condition has been reported to be $\sim2\times10^{18}$ cm^{-3} [3.52]. The SiO_2 capping layer was patterned and etched to define contact holes that exposed the n^+ InGaAs surface for Ni-InGaAs contact formation. Fig. 3.5(a) inset shows the top view of the TLM structure with Ni-InGaAs contacts formed on n^+ InGaAs, as obtained by optical microscopy.

I-V characteristics were measured between two adjacent Ni-InGaAs contact pads separated by various contact spacings *d*, showing good ohmic behavior [Fig. 3.5(a)]. By plotting the total resistance between two contacts R_T versus spacing *d*, as shown in Fig. 3.5(b), the contact resistance R_C can be extracted from the intercept of

the linear fitting line with the vertical axis and the sheet resistance $R_{sh,InGaAs}$ of the doped substrate can also be extracted from the line slope. R_C and $R_{sh,InGaAs}$ were obtained to be ~1.27 kΩ·μm and 30.4 Ω/square, respectively. Both contact length L and contact width W of the TLM are 100 μm and thus the assumption of $L > 1.5L_T$ is valid, where L_T is transfer length. The specific contact resistivity ρ_C could be obtained by $\rho_C \approx R_C L_T W$. The calculated $\rho_C = 5.4 \times 10^{-4}$ Ω·cm^2.

Ni-InGaAs/p-InGaAs Schottky diodes and Ni-InGaAs/n-InGaAs/p-InGaAs diodes were fabricated, as illustrated in the inset of Fig. 3.6. Ni-InGaAs shows good rectifying behavior on p-InGaAs with forward current/reverse current ratio of over ~4 orders of magnitude (Fig. 3.6). Ni-InGaAs/n-InGaAs/p-InGaAs diodes show a lower reverse current as compared with Ni-InGaAs/p-InGaAs Schottky diodes. The PN diodes also show better saturation of the reverse current. There is an important difference between a Schottky diode and a PN junction diode in the magnitudes of the reverse-saturation current density. The reverse-saturation current density of the Schottky barrier diode $J_{S,Schottky}$ is given [3.53]:

$$J_{S,Schottky} = A^* T^2 \exp(\frac{-q\phi_{Bn}}{kT}), \qquad (3.1)$$

where A^* is the effective Richardson constant for thermionic emission, ϕ_{Bn} is Schottky barrier height, T is temperature, q is electronic charge, and k is Boltzmann's constant. The ideal reverse-saturation current density of the PN junction diode $J_{S,PN}$ can be written as [3.53]:

$$J_{S,PN} = \frac{qD_n n_{po}}{L_n} + \frac{qD_p p_{no}}{L_p}, \qquad (3.2)$$

where q is electronic charge, n_{po} (or p_{no}) is thermal equilibrium minority electron (or hole) carrier concentration in p (or n) region, D_n and D_p are diffusion coefficient for electron and hole, respectively, L_n and L_p are electron and hole diffusion lengths, respectively.

The forms of the Equations (3.1) and (3.2) are vastly different, and the current mechanism in the two diodes is different. The higher reverse current of Ni-InGaAs/p-InGaAs Schottky diodes is mainly contributed by thermionic emission of majority carriers (holes) over a barrier, which is 1 - 2 orders of magnitude higher than the drift current of minority carriers in the n-InGaAs/p-InGaAs junction (Fig. 3.6).

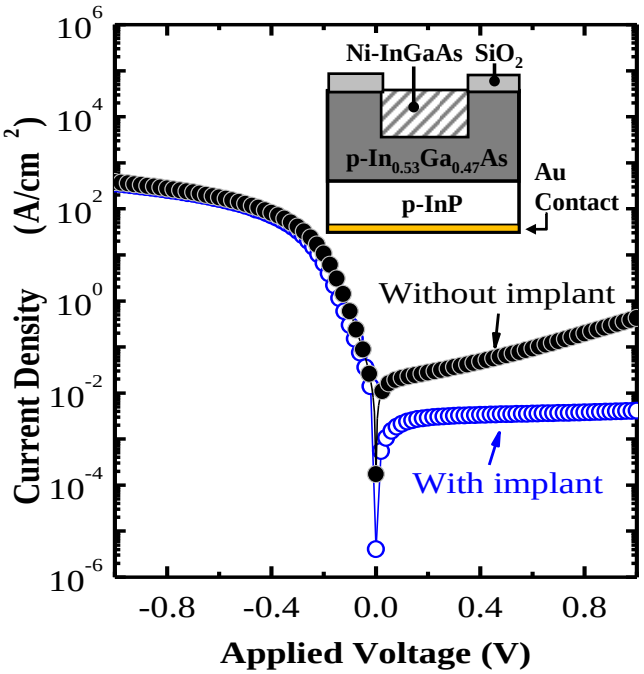

Fig. 3.6. Ni-InGaAs/p-InGaAs Schottky diodes and Ni-InGaAs/n-InGaAs/p-InGaAs diodes were fabricated, as illustrated in the inset. Ni-InGaAs shows good rectifying behavior on p-InGaAs with forward current/reverse current ratio of over ~4 orders of magnitude. Ni-InGaAs/n-InGaAs/p-InGaAs diodes show a much lower reverse saturation current as compared with Ni-InGaAs/p-InGaAs Schottky diodes.

3.3 Device Integration and Characterization

3.3.1 Integration of Self-aligned Ni-InGaAs Contacts on InGaAs n-MOSFETs

The process flow for transistor fabrication is summarized in Fig. 3.7(a). The device structure for InGaAs channel n-MOSFETs with self-aligned Ni-InGaAs contacts is also illustrated in Fig. 3.7 (b), (c) and (d). The starting substrates are 2-inch p-type (N_A ~1×10^{19} cm^{-3}) InP wafers. A 500 nm thick $In_{0.53}Ga_{0.47}As$ with p-type (Zn doped) doping concentration N_A of 2×10^{17} cm^{-3} and a 20 nm thick $In_{0.7}Ga_{0.3}As$ with N_A of 2×10^{16} cm^{-3} were sequentially grown by molecular beam epitaxy by an external vendor. Before high-*k* dielectric deposition, exactly the same pre-gate cleaning process for GaAs transistor, as described in Chapter 2, was performed for the substrate. HCl, ammonium hydroxide (NH_4OH) and ammonium sulfide $(NH_4)_2S$ solutions were used for cleaning and treating the InGaAs surface. The samples were then quickly loaded into an atomic layer deposition (ALD) tool and ~7 nm of aluminum oxide (Al_2O_3) was deposited. ~100 nm TaN was deposited by sputtering, patterned by optical lithography and finally etched by Cl_2-based plasma to form the gate electrode.

After gate stack (TaN-on-Al_2O_3, denoted as "TaN/Al_2O_3") formation, one batch of devices (implanted devices) went through Si^+ S/D implant at an energy of 40 keV and a dose of 1×10^{14} cm^{-2}. After the devices were capped with a thin layer of SiO_2, dopant activation anneal was performed at 600 ℃ for 60 s. The other batch of devices (control devices) did not receive Si^+ implant and dopant activation anneal. Both batches of devices subsequently went through the same salicide-like self-aligned metallization process. ~30 nm Ni was firstly deposited on the device samples, as

illustrated in Fig. 3.7(b). Ni film was uniformly deposited over the gate stack and S/D regions. The horizontal dotted line indicates the Ni/InGaAs interface and the dashed line indicates the n-InGaAs well formed by Si^+ implant [Fig. 3.7(b)]. Then, RTA at 250 ℃ for 60 s was done to initiate Ni reaction with InGaAs. The deposited Ni in S/D regions was completely consumed as Ni-InGaAs was formed during the thermal anneal, as shown in Fig. 3.7(c).

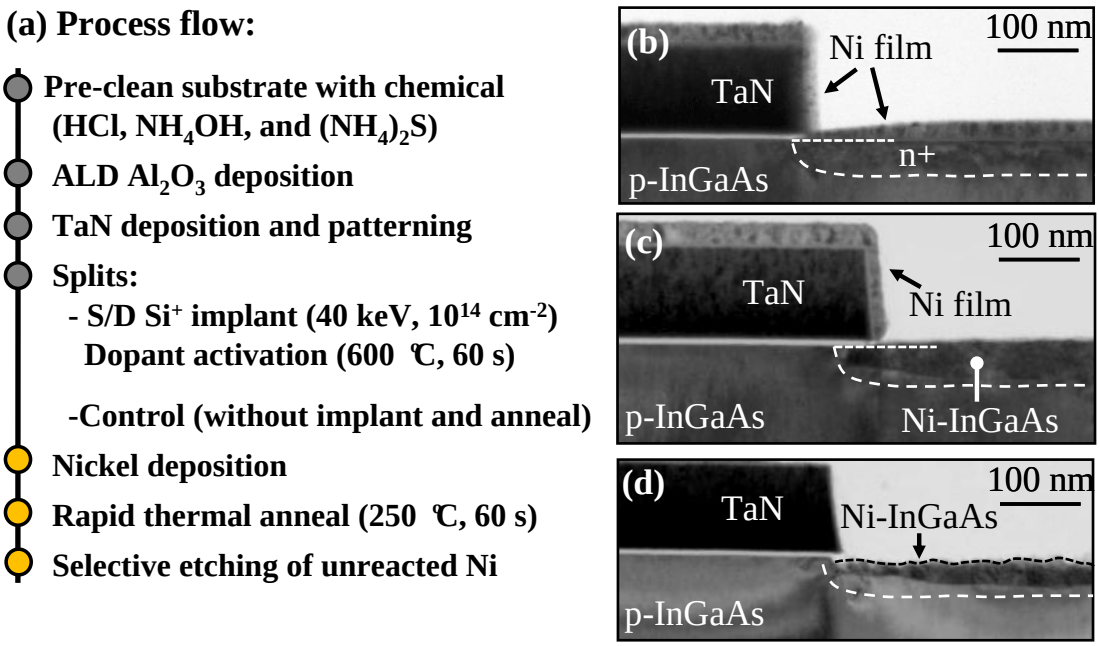

Fig. 3.7. Process flow for fabricating InGaAs channel n-MOSFETs with self-aligned Ni-InGaAs contacts. S/D implant and dopant activation annealing were performed for one batch of devices (implanted devices), while the other batch of devices (control devices) skipped both the implant and activation annealing. (b) Ni was uniformly deposited on the gate and S/D regions of the device sample. (c) After thermal annealing, Ni diffuses into InGaAs and reacts with InGaAs by forming Ni-InGaAs. Ni-InGaAs formed on the surface of InGaAs shows a darker contrast with the InGaAs substrate. (d) Unreacted Ni over gate stack was selective removed by a selective wet etch using HCl solution. The cross-section TEM image shows the final structure of an InGaAs device with self-aligned Ni-InGaAs contacts.

The Ni-InGaAs contact appears as a darker region formed on the surface of InGaAs, lying adjacent and well aligned to the TaN/Al_2O_3 gate stack.

The reaction between Ni and InGaAs was controlled by diffusion of Ni atoms into InGaAs during the thermal annealing. In the case of $TiSi_2$ and CoSi, the dominant diffusing species is Si. The movement of Si atoms into the metal film has a potential issue in Si MOSFETs as silicidation may also occur on the sides of spacers and this phenomenon is known as creep-up [3.54]. The possibility of salicide bridges forming between the gate and S/D is high when the creep-up is significant. However, the Ni-InGaAs metallization proceeds by the movement of Ni into the InGaAs substrate as seen from Fig. 3.7(c), similar to NiSi formation. In addition, Ni does not react with TaN metal gate, as compared with Ti, Co and Ni that would react with polysilicon gate in Si CMOS process flows where gate spacers are not used. The bridging issue that would cause gate-to-S/D shorts does not occur even without use of spacers when the salicide-like Ni-InGaAs metallization process is integrated in metal-gate InGaAs n-MOSFETs. The fabrication process was completed by removal of unreacted Ni over the gate stack in HCl solution [Fig. 3.7(d)].

TEM image in Fig. 3.7(d) shows the final cross-section structure of an InGaAs channel n-MOSFETs with self-aligned Ni-InGaAs contacts. The self-aligned Ni-InGaAs contact appears as a darker region formed on the surface of the InGaAs substrate, lying adjacent and well aligned to the TaN/Al_2O_3 gate stack. A continuous Ni-InGaAs layer with good morphology was formed, showing good contrast with respect to the underlying InGaAs layer. The Ni-InGaAs layer thickness is measured to be ~30 nm, and is uniform over the entire S/D regions. EDX was performed to

obtain Ni-InGaAs atomic composition. Atomic concentration versus depth as plotted in Fig. 3.8 shows a uniform composition across the whole Ni-InGaAs layer.

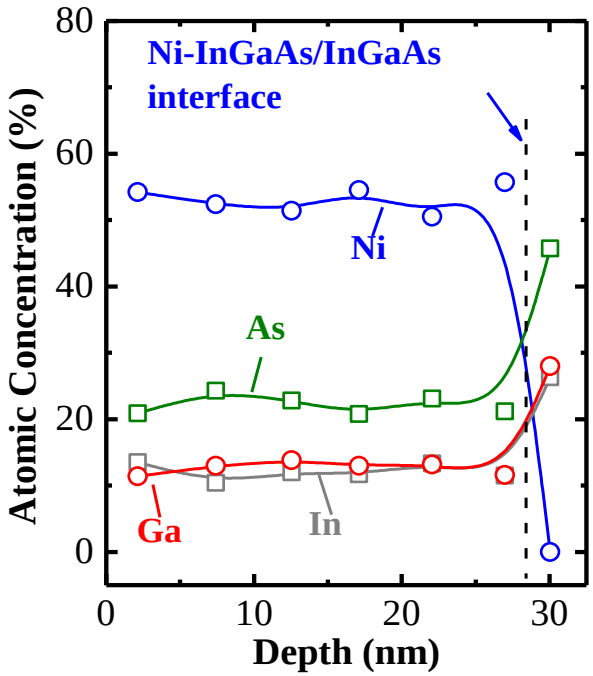

Fig. 3.8. EDX characterization at localized spots in the Ni-InGaAs region was performed to obtain the Ni-InGaAs composition. Atomic concentration versus depth shows a uniform composition ratio of Ni: In: Ga: As = 51: 12: 14: 23 through the entire Ni-InGaAs layer.

3.3.2 Device Characterization and Analysis

Both implanted and control InGaAs channel n-MOSFETs were electrically characterized. Fig. 3.9(a) shows the I_D-V_G transfer characteristics of devices with a gate length (L_G) of 1 μm. The device gate length was confirmed using SEM. The

devices show an on-state/off-state drain current ratio of 10^3~10^5. Device with S/D implant shows significantly lower off-current I_{OFF} as compared with the device without S/D implant. The higher I_{OFF} of the devices with Ni-InGaAs S/D is due to the high reverse current of Ni-InGaAs/p-InGaAs Schottky diode. Therefore, forming n-InGaAs/p-InGaAs junction in the S/D regions helps to suppress the junction leakage significantly. This was explained in Section 3.2 of this Chapter. We also examined the gate leakage current for both devices and they show comparable gate current below the level of ~10^{-11}A/μm [Fig. 3.9(a)].

The individual threshold voltage V_T for a device in the linear regime (V_D = 0.1 V) was determined by maximum transconductance ($G_{m,ext}$) method [3.55]. The I_D-V_D output characteristics of the transistors at various gate overdrive $V_G - V_T$ from 0 to 2.5 V in steps of 0.5 V are plotted in Fig 3.9(b). Both devices exhibit good saturation and pinch-off characteristics. The drain current of a long channel MOSFET with doped S/D is determined by the drift current that flows from the source to the drain. In a long channel MOSFET with metallic S/D (or Schottky S/D), a Schottky barrier height exists at the metal-semiconductor interface, and the drain current could be additionally limited by carrier emission across the source-to-channel Schottky barrier and/or across the channel-to-drain energy barrier, depending on the terminal biases. The channel-to-drain energy barrier exists at low V_D, but disappears at higher V_D. This might explain the observation that at low V_D the device with metallic S/D shows a lower drain current than the device with doped S/D, but both devices show similar drain current at higher V_D.

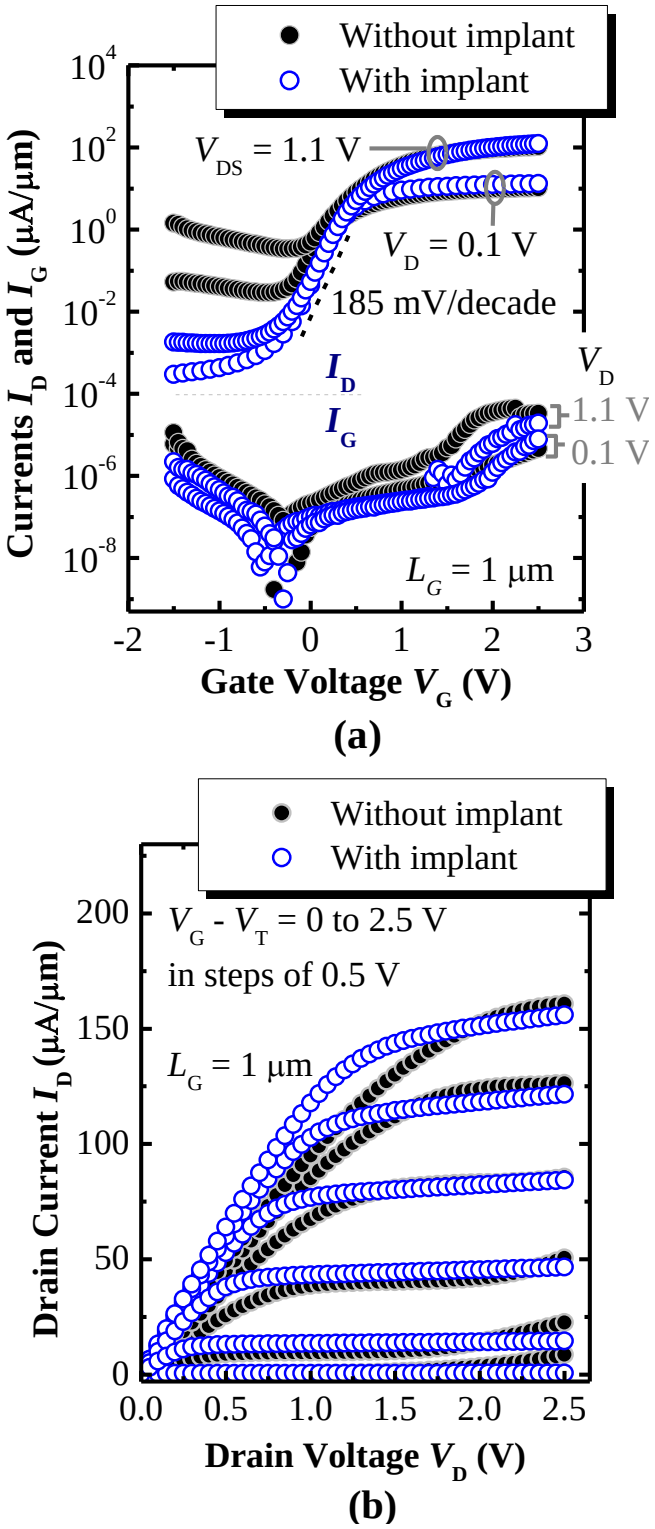

Fig. 3.9. (a) I_D - V_G transfer characteristics of implanted and control $In_{0.7}Ga_{0.3}As$ channel n-MOSFETs with gate length of 1 μm. I_{OFF} for the implanted device is significantly reduced as compared with the control device. Gate leakage current I_G is also plotted. (b) I_D - V_D output characteristics of the transistors at various gate overdrives.

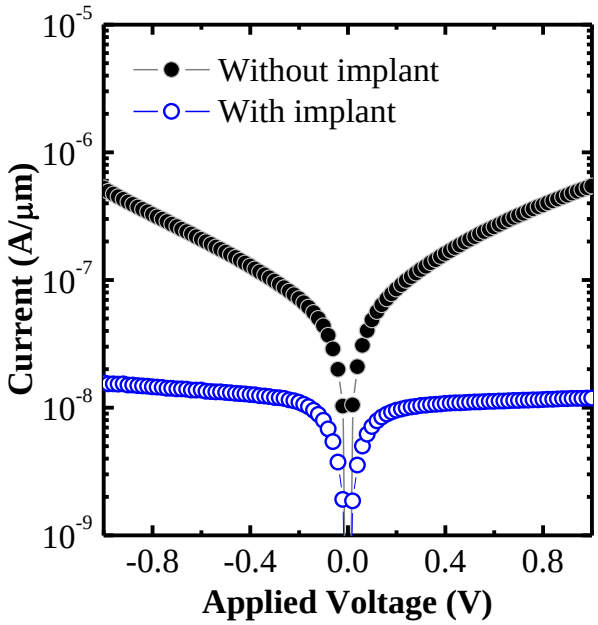

Fig. 3.10. *I-V* characteristics of source-to-drain back-to-back diodes for both devices. The current was normalized by gate width W_{eff} = 100 μm. Device with implanted S/D shows a much lower junction leakage current (reverse-saturation current).

I-V characteristics of source-to-drain back-to-back diodes for both devices were measured and plotted in Fig. 3.10. The current was normalized by device gate width W_{eff} = 100 μm. Device with implanted S/D shows a much lower junction leakage current. V_T' is the mean threshold voltage of a group of devices with or without S/D implant. I_{OFF} was defined at gate overdrive V_G - V_T' of -0.3 V and I_{ON} was defined at gate overdrive V_G - V_T' of 1.8 V. Fig. 3.11(a) and (b) compare I_{ON}-I_{OFF} characteristics of two groups of devices in the linear and saturation region, respectively. The gate length of the devices ranges from 1 μm to 20 μm. I_{OFF} was significantly suppressed for devices with Si doped S/D. Over 5 times and 30 times reduction of I_{OFF} is observed in the linear and saturation region, respectively.

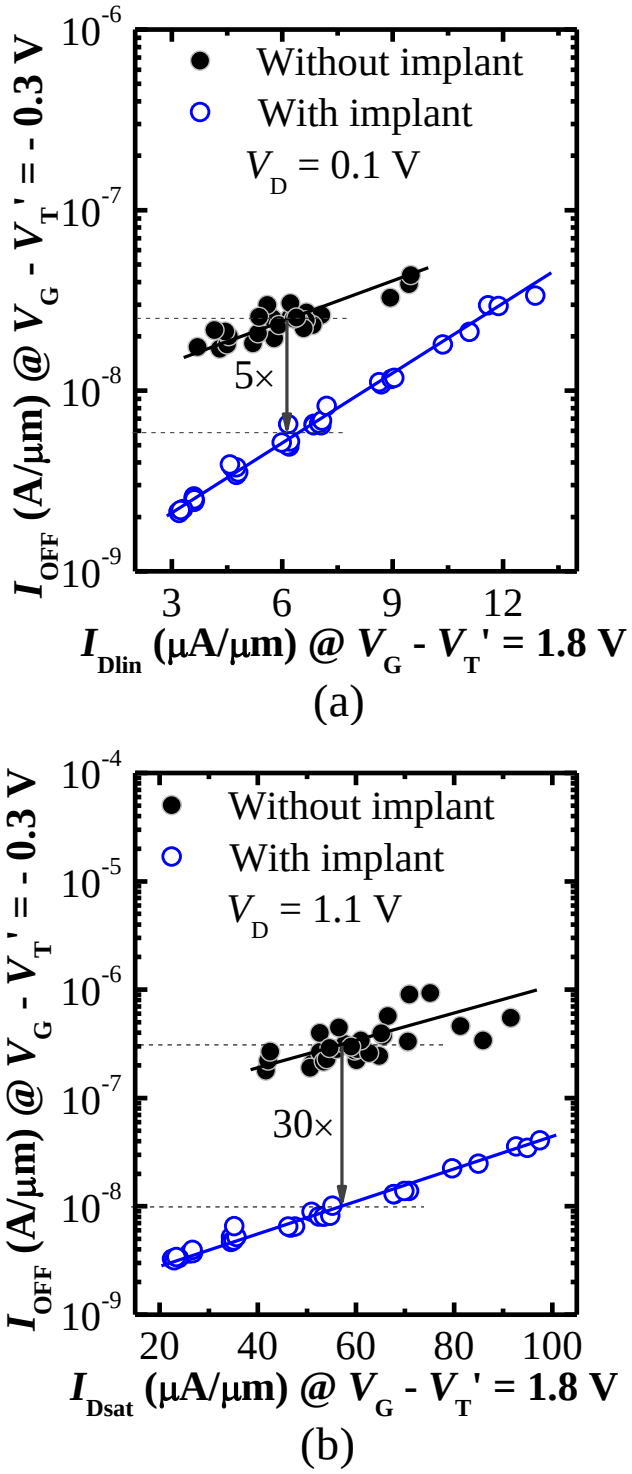

Fig. 3.11. (a) I_{ON}-I_{OFF} characteristics of implanted and control devices in the linear region (V_D = 0.1 V). I_{OFF} and I_{ON} are defined at gate overdrives V_G - V_T' of -0.3 V and 1.8 V, respectively. (b) I_{ON}-I_{OFF} characteristics in the saturation region (V_D = 1.1 V). I_{OFF} was significantly suppressed for devices with n^+ S/D implant. Over 5 times and 30 times reduction of I_{OFF} was observed in the linear and saturation region, respectively.

The intrinsic transconductance ($G_{m,int}$) of a transistor can be extracted from extrinsic transconductance $G_{m,ext}$ using[3.53],[3.56]

$$G_{m,\text{int}} = \frac{G_{m,ext}}{1 - G_{m,ext}R_S - G_d R_{SD}}, \tag{3.3}$$

where R_{SD} is the total series resistance given by $R_{SD} = R_S + R_D$. Source parasitic resistance R_S and drain parasitic resistance R_D are assumed to be equal. The extraction of individual R_{SD} for devices will be discussed later. G_d is the measured drain conductance defined by $G_d = \partial I_D / \partial V_D$. For a long channel device operated in saturation region, Equation (3.3) can be simplified to [3.53],[3.56]

$$G_{m,\text{int}} = \frac{G_{m,ext}}{1 - G_{m,ext}R_S}, \tag{3.4}$$

since the drain conductance G_d can be assumed to be zero. This assumption was reasonable for a long channel MOSFET, as observed in Fig. 3.9(b).

Fig. 3.12 plots the $G_{m,ext}$ (solid circles) and $G_{m,int}$ (open circles) for the same pair of devices in Fig. 3.9. Both devices show comparable $G_{m,ext}$ of ~75 μS/μm and $G_{m,int}$ of ~95 μS/μm at applied drain voltage of 1.1 V. We note that peak intrinsic transconductance and on-state current are low, and this is primarily due to the large gate length and large EOT (~3.5 nm) of the gate dielectric. The R_{SD} of individual devices was extracted using the same method as described in Chapter 2. Fig. 3.13 plots the total resistance R_T in the linear regime (V_D = 0.1 V) as a function of gate voltage for the same pair of devices in Fig. 3.9. R_T could be written as [3.55]:

$$R_T = R_{SD} + L_G[W_{eff}\mu_{eff}C_{ox}(V_G - V_T)]^{-1}, \tag{3.5}$$

where L_G is gate length, W_{eff} is gate width, μ_{eff} is channel effective mobility, C_{ox} is

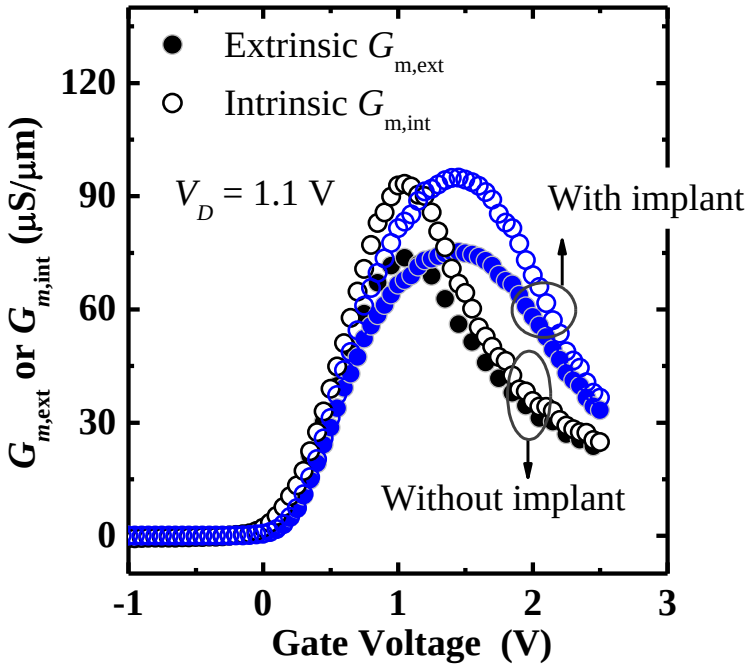

Fig. 3.12. $G_{m,ext}$ (solid circles) and $G_{m,int}$ (open circles) was plotted for control and implanted devices. Both devices show comparable extrinsic and intrinsic transconductane at V_D of 1.1 V.

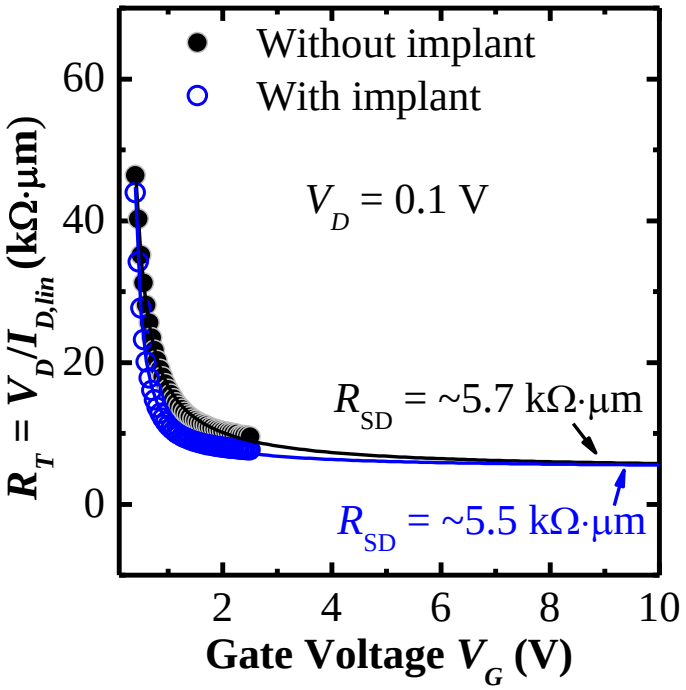

Fig. 3.13. Total resistance R_T in the linear regime (V_D = 0.1 V) as a function of gate voltage for the same pair of devices in Fig. 3.9. Equation (3.5) was used to fit the data points (circles). The fitted solid curves were extrapolated to V_G = 10 V to obtain the value of R_{SD}.

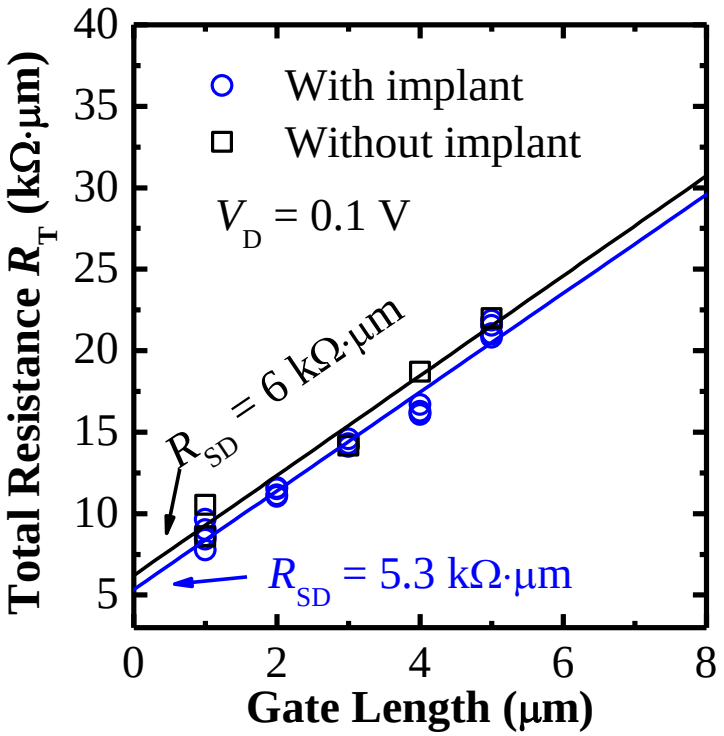

Fig. 3.14. R_T in the linear regime (V_D = 0.1 V) as a function of L_G at a specified gate overdrive $V_G - V_T$ of 1.8 V. Equation (3.5) was used to fit the data points (circles and squares). The fitted curves were extrapolated to L_G = 0 to obtain the value of R_{SD}. The obtained R_{SD} values for control and implanted device are ~6 and 5.3 kΩ·μm, respectively.

gate oxide capacitance, and V_G-V_T is gate overdrive. Equation (3.5) was used to fit the experimental data points (circles) and the fitted solid curves were extrapolated to a large V_G = 10 V to obtain R_{SD}. The obtained R_{SD} for control device and implanted device are ~5.7 and 5.5 kΩ·μm, respectively (Fig. 3.13).

Fig. 3.14 also plots the R_T in the linear regime (V_D = 0.1 V) as a function of L_G at a specified $V_G - V_T$ of 1.8 V. Gate length L_G was confirmed by SEM inspection. Equation (3.5) was used to fit the data points (squares and circles). The fitted curves

were extrapolated to $L_G = 0$ to obtain the value of R_{SD}. The obtained R_{SD} values for control and implanted devices are ~6 kΩ·μm and 5.3 kΩ·μm, respectively. These values are extracted from a group of devices and are quite consistent with the individual R_{SD} we obtained in Fig. 3.13 using a R_T versus V_G method.

Fig. 3.15(a) shows the device layout. The device source or drain region has an area of 100 μm × 100 μm. The schematic of a device cross section [Fig. 3.15(b)] along (A-A') shows that the device R_{SD} has main contributions from Ni-InGaAs sheet resistance $R_{Ni\text{-}InGaAs}$ and Ni-InGaAs contact resistance $R_{C,}$ which can be described by:

$$R_{SD} = R_{Ni\text{-}InGaAs} + R_C. \quad (3.6)$$

The obtained Ni-InGaAs contact resistance R_C from TLM structures is ~1.27 kΩ·μm [Fig. 3.5]. The Ni-InGaAs R_C in the source and drain regions would contribute a total resistance of $2R_C$ = ~2.5 kΩ·μm to R_{SD}. The S/D probes are ~50 μm (D_{sp} = ~ 50 μm) away from the device channel as the probes were landed in the center of the S/D regions during the measurement. Based on the device S/D geometry shown in Fig. 3.15, Ni-InGaAs resistance could be calculated as:

$$R_{Ni\text{-}InGaAs}' = (D_{sp}/W_{eff}) \times R_{sh,Ni\text{-}InGaAs}, \quad (3.7)$$

and $$R_{Ni\text{-}InGaAs} = W_{eff} \times (D_{sp}/W_{eff}) \times R_{sh,Ni\text{-}InGaAs} = D_{sp} \times R_{sh,Ni\text{-}InGaAs}, \quad (3.8)$$

where $R_{Ni\text{-}InGaAs}'$ is Ni-InGaAs resistance (Ω) before normalization and $R_{Ni\text{-}InGaAs}$ is the resistance (Ω·μm) after normalized by the device gate width W_{eff} = 100 μm. Sheet resistance $R_{sh,Ni\text{-}InGaAs}$ = 30 Ω/square for 30 nm thick Ni-InGaAs film in S/D regions. Based on Equation (3.8), the calculated $2R_{Ni\text{-}InGaAs}$ = ~3 kΩ·μm.

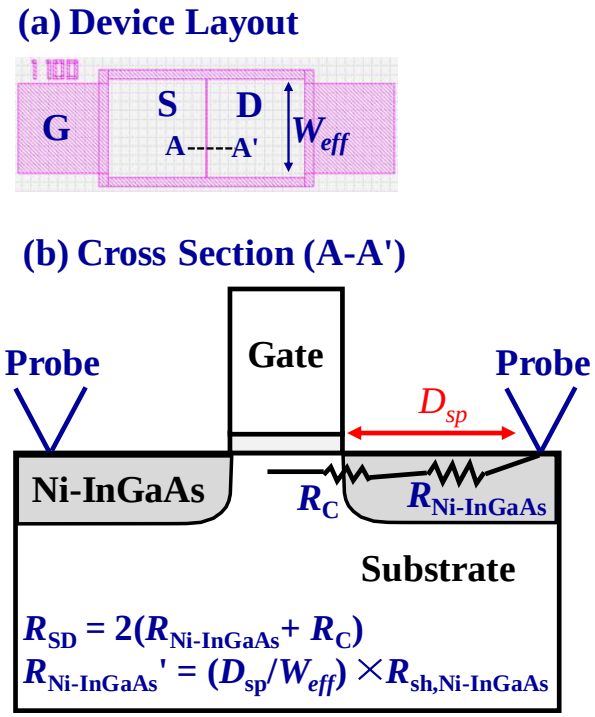

Fig. 3.15. (a) The device layout showing that the source or drain has an area of 100 μm × 100 μm. (b) The schematic of the device cross section (A-A') shows that series resistance R_{SD} includes Ni-InGaAs sheet resistance and Ni-InGaAs contact resistance.

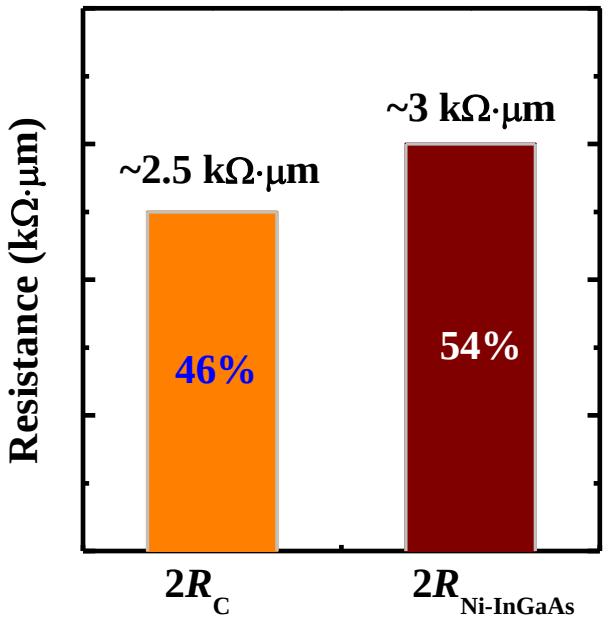

Fig. 3.16. Ni-InGaAs resistance and Ni-InGaAs contact resistance are the main resistance components of the transistor R_{SD} and they lead to a contribution of 46% and 54 % to $R_{SD,}$ respectively.

Fig. 3.16 shows the resistance contribution of Ni-InGaAs sheet resistance and Ni-InGaAs contact resistance, the sum of which is ~5.5 kΩ·μm and is in good agreement with the extracted R_{SD} (5.3 ~ 6 kΩ·μm). In this case, Ni-InGaAs sheet resistance and Ni-InGaAs contact resistance lead to a contribution of 46% and 54 % to the device total $R_{SD,}$ respectively. We should note that the Ni-InGaAs sheet resistance component could be further reduced by moving the probe closer the device channel (reduced D_{sp}) during the measurement. We compared the R_{SD} of this work with the values reported in other works. Various contact materials were used and integrated on either implanted or *in-situ* doped S/D. Lowest R_{SD} were achieved in this work among the transistors with implanted S/D. We noticed that the transistors with *in-situ* doped S/D shows much lower R_{SD}, due to their much higher S/D doping concentration. Ni-InGaAs contact resistance could also be reduced by using a heavily doped (N_D = 5×19 cm^{-3}) S/D, which shall be discussed in next Chapter.

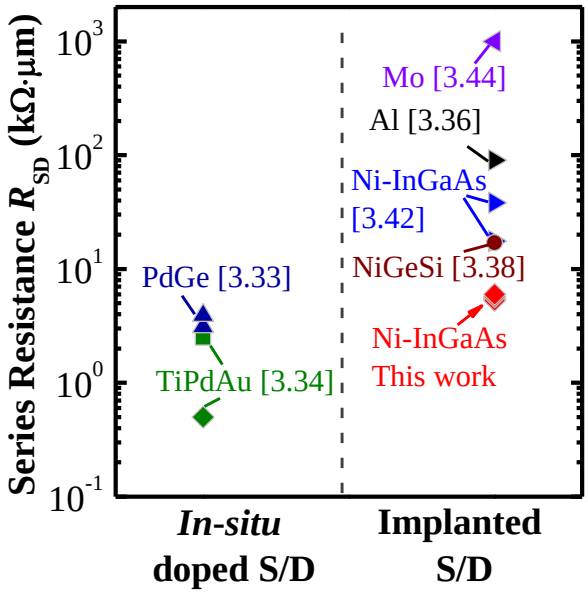

Fig. 3.17. R_{SD} of this work is the lowest among the reported R_{SD} values for transistors with implanted S/D. It is found that transistors with *in-situ* doped S/D show much lower R_{SD}.

3.4 Summary

A salicide-like self-aligned Ni-InGaAs contact technology for InGaAs n-MOSFETs was developed in this Chapter. Ni-InGaAs contacts were studied comprehensively by means of material and electrical characterization. This self-aligned contact technology was used in the fabrication of InGaAs channel n-MOSFETs. InGaAs channel n-MOSFETs with self-aligned metallic Ni-InGaAs S/D as well as Si-doped S/D with Ni-InGaAs contacts were realized and characterized. Both devices show good electrical characteristics. Implanted devices exhibit significantly lower I_{OFF} compared with devices without implant (metallic S/D). Device series resistance R_{SD} was investigated and was mainly contributed by Ni-InGaAs sheet resistance and Ni-InGaAs contact resistance. In summary, the self-aligned contacts are promising for future InGaAs n-MOSFETs integration in high performance low power logic applications.

3.5 References

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Chapter 4

InGaAs FinFETs with Self-Aligned Ni-InGaAs Contacts

4.1 Introduction

InGaAs channel non-planar MOSFETs (FinFETs, Multiple-gate FETs, Tri-gate FETs, or Gate-all-around FETs) could be adopted as n-channel logic transistors in sub-10 nm technology nodes [4.1]-[4.7]. Purdue University demonstrated the first InGaAs FinFET in year 2009 [4.1]. After that, our group at the National University of Singapore (NUS) [4.2] and Intel Corporation [4.3],[4.4] also reported InGaAs Multiple-gate and Tri-gate n-MOSFETs. Purdue University recently also demonstrated InGaAs channel gate-all-around (GAA) n-MOSFETs [4.5]. These results indicate that InGaAs non-planar n-MOSFETs have improved electrostatics and can achieve much better control of short-channel effects (SCEs) than InGaAs planar n-MOSFETs.

High quality high-*k* gate dielectric interface with small equivalent oxide thickness (EOT) on the InGaAs fin was demonstrated by Intel [4.4]. The Tri-gate FETs exhibit impressive electrical characteristics, showing subthreshold swing *S* of 95 mV/decade and drain induced barrier lowering (DIBL) of ~50 mV/V at a channel length L_{CH} of 60 nm [4.4]. Aggressive scaling of fin width in FinFETs for control of SCEs may lead to high source/drain (S/D) series resistance (R_{SD}) and R_{SD} will affect

the drive current performance. However, there is still lack of research for R_{SD} engineering for InGaAs FinFETs. Table 4.1 summarizes the state-of-art S/D contact technologies for InGaAs non-planar MOSFETs. Conventional implantation (e.g. Si, Se) and dopant activation anneal are usually used to form n-type S/D doping and the doping concentration (N_D) is at the level of ~2×10^{18} cm^{-3} [4.8]. *In-situ* Si-doped InGaAs can achieve much higher N_D of over 1×10^{19} cm^{-3} [4.9],[4.10]. Materials such as NiAuGe and PdGe have been employed as S/D contacts for InGaAs FinFETs and are usually formed by a non-self-aligned method [4.1]-[4.5]. International Technology Roadmap for Semiconductors (ITRS) requires R_{SD} below 131 Ω·μm for III-V multiple-gate n-MOSFETs [4.11]. However, the reported values of R_{SD} of InGaAs non-planar n-MOSFETs are still higher than 1000 Ω·μm, as shown in Table 4.1.

Table 4.1. State-of-art S/D contact technologies for InGaAs non-planar n-MOSFETs.

InGaAs Non-planar Devices	**S/D Doping Method**	**Contact Materials**	**Self-Aligned Contacts**	**R_{SD} (Ω·μm)**	**Reference**
FinFETs (Purdue, 2009)	ion-implantation	NiAuGe	no	1200	[4.1]
Multiple-gate (NUS, 2011)	ion-implantation	PdGe	no	~1000	[4.2]
Tri-gate (Intel, 2010 & 2011)	*in-situ* doped	not reported	no	not reported	[4.3], [4.4]
GAA (Purdue, 2011)	ion-implantation	NiAuGe	no	1150	[4.5]

Development of reliable, CMOS compatible, and low-resistance S/D ohmic contacts is needed for InGaAs FinFETs in order to realize high drive current performance. In addition, self-alignment of the S/D contacts to the gate electrode is desirable for reduced S/D access resistance and for continual scaling of the transistor footprint [4.11]-[4.19]. However, there is no report of integration of low-resistance, self-aligned S/D contacts in InGaAs FinFETs.

In this Chapter, a gate-last fabrication process for InGaAs FinFETs is developed and the integration of self-aligned Ni-InGaAs contacts in the FinFETs with sub-100 nm channel lengths L_{CH} is demonstrated [4.6],[4.7]. The gate-last FinFET process development involves the design of III-V layer structure, selective wet etch of n^+ InGaAs, and plasma etch of InGaAs fin. The process development will be discussed in detail. The FinFET fabrication process also includes a salicide-like Ni-InGaAs metallization process [4.15]-[4.18] documented in Chapter 3. The metallization process converts deposited Ni on n^+ InGaAs into a uniform Ni-InGaAs film by rapid thermal annealing (RTA) and removal of unreacted Ni by selective wet etch. Ni-InGaAs contacts formed on *in-situ* doped n^+ InGaAs S/D show low contact resistance (R_C) and low sheet resistance (R_{sh}). With the integration of self-aligned Ni-InGaAs contacts, the InGaAs FinFETs show good drive current performance. The FinFET device has a R_{SD} of ~364 Ω·μm and resistance contributions from various resistance components were analyzed. Knowing the contribution of each resistance component provides guidance for further R_{SD} engineering.

4.2 Process Development for Fabrication of InGaAs FinFETs

4.2.1 Design of III-V Layer Structure

Fig. 4.1 illustrates the III-V layer structure that was used for fabrication of InGaAs FinFETs. 2-inch semi-insulating InP wafers served as the starting substrates. 300 nm undoped $In_{0.52}Al_{0.48}As$, 50 nm undoped $In_{0.53}Ga_{0.47}As$, 2 nm undoped InP, and 30 nm n^+ $In_{0.53}Ga_{0.47}As$ were sequentially grown by molecular beam epitaxy by an external vendor. The top n^+ $In_{0.53}Ga_{0.47}As$ layer was *in-situ* doped with Si and was used as device S/D. The active carrier concentration N_D is as high as 5×10^{19} cm^{-3} which would help reduce device R_{SD}. Undoped InP (2 nm) serves as an etch stop layer and a capping layer for the undoped $In_{0.53}Ga_{0.47}As$ channel. InP capping has been reported to increase channel electron mobility in InGaAs devices [4.20],[4.21]. The $In_{0.53}Ga_{0.47}As$ channel layer has a thickness of 50 nm and will be etched into fins. The undoped $In_{0.52}Al_{0.48}As$ (300 nm) has a large bandgap (1.47 eV) and was used as underlying barrier layer to reduce the device source-to-drain leakage.

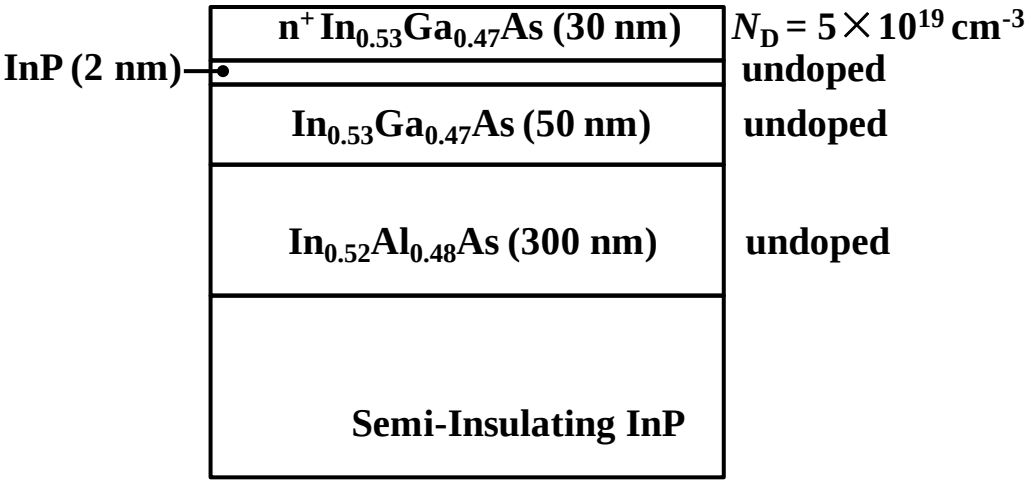


Fig. 4.1. Layer structure of III-V wafer for $In_{0.53}Ga_{0.47}As$ FinFET fabrication. The III-V layers were grown on 2-inch semi-insulating InP substrate by molecular beam epitaxy.

4.2.2 Selective Wet Etch of n^+ InGaAs

To separate source and drain regions as well as to expose the channel layer for gate stack formation, a selective wet etch process is needed to recess a portion of the n^+ InGaAs in the channel region. The wet etch should stop on the InP layer. Citric acid/hydroperoxide (denoted as $C_6H_8O_7/H_2O_2$) based chemical could achieve selective etch of InGaAs over InP [4.22]. In this Chapter, an etch experiment was performed to confirm the etch selectivity and obtain the etch rate of InGaAs. The etch experiment was performed at room temperature using a mixture of $C_6H_8O_7$ and H_2O_2. First, the purchased anhydrous citric acid crystals were dissolved in deionized water (DI H_2O) at a ratio of 1 g of $C_6H_8O_7$ to 1 ml of H_2O. This $C_6H_8O_7/H_2O$ mixture was named "aqueous citric acid" in this experiment. Next, the aqueous citric acid was mixed with H_2O_2 (30% weight per volume) approximately 5 minutes before conducting the wet etch. A volume ratio of $C_6H_8O_7$: H_2O_2 = 20: 1 was chosen to achieve a target etch rate of about 60 nm/minute. This would enable a good time control for etching 30 nm of n^+ InGaAs.

A wafer with 500 nm thick InGaAs layer on top of InP substrate was used for the wet etch experiment. A 35 nm SiO_2 layer (T_{mask} = 35 nm) was deposited by electron beam evaporation, patterned and etched as an etch mask, as illustrated in Fig. 4.2(a). Then, the sample was cut into small pieces and each sample was dipped in $C_6H_8O_7/H_2O_2$ (20: 1) solution for different durations of 0.5, 1, 2, and 3 minutes. After that, surface profiler was used to measure the total step height T_{total} of SiO_2 and InGaAs for each sample. The InGaAs step height T_{InGaAs} could be obtained using

$$T_{InGaAs} = T_{total} - T_{mask}. \quad (4.1)$$

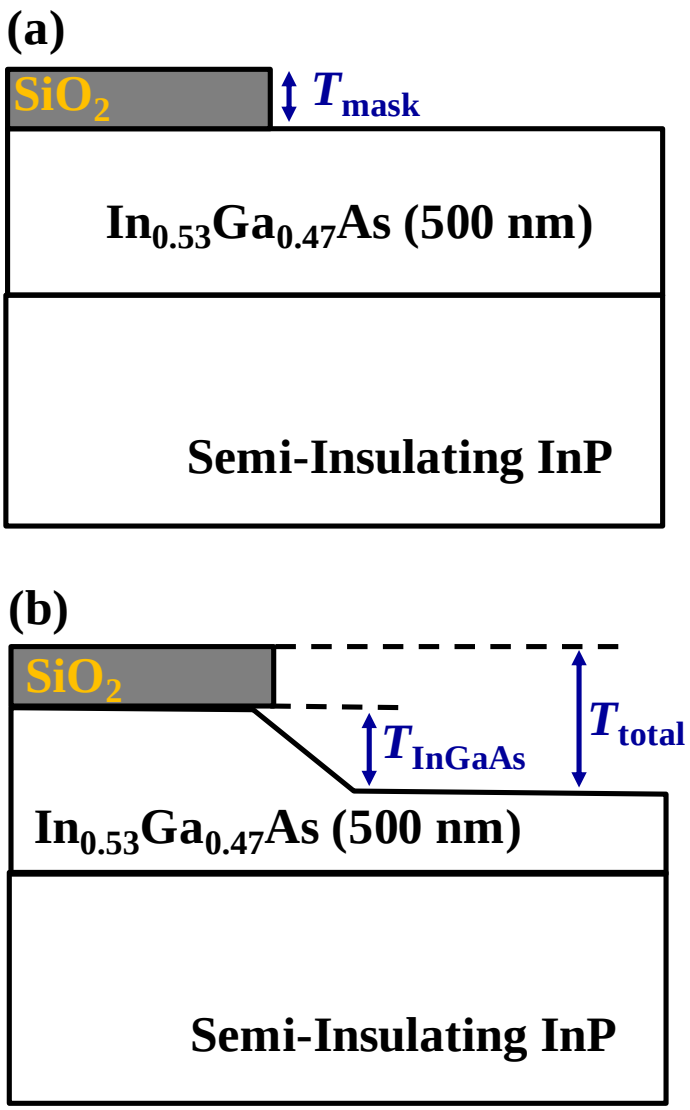


Fig. 4.2. (a) The wafer used in this etch experiment has a 500 nm thick InGaAs layer on InP substrate. SiO_2 layer with thickness T_{mask} of 35 nm was deposited by electron beam evaporation and was etched as an etch mask. (b) The sample was dipped in $C_6H_8O_7/H_2O_2$ solution for different durations. The etch step height T_{InGaAs} of InGaAs was measured by surface profiler**.**

InGaAs step height T_{InGaAs} as a function of etch time is plotted in Fig. 4.3. The points (squares) are the measured experimental data and the solid curve is a linear line fit of the data points. The etch rate of InGaAs in $C_6H_8O_7/H_2O_2$ (20: 1) solution was

obtained from the slope of the fitted line to be ~73 nm/minute (1.2 nm/s). This etch rate is slow enough to allow good time control for the etching of 30 nm of InGaAs layer. It takes 6 ~ 7 minutes to etch away the 500 nm thick InGaAs layer and a T_{InGaAs} of ~ 500 nm was observed. After that, the sample was dipped in $C_6H_8O_7/H_2O_2$ for another 5 minutes and no further increase in the step height was observed. This means that $C_6H_8O_7/H_2O_2$ (20: 1) does not etch InP or etches InP at a much slower rate [4.22]. Good etch selectivity of InGaAs with respect to InP was observed. Chemical etch of most III-V semiconductor materials usually proceeds by an oxidation-reduction reaction at the semiconductor surface, followed by dissolution of the oxide material, resulting in removal of the semiconductor material [4.22]. In this etchant system, H_2O_2 acts as the oxidizing agent and $C_6H_8O_7$ dissolves the resulting oxide.

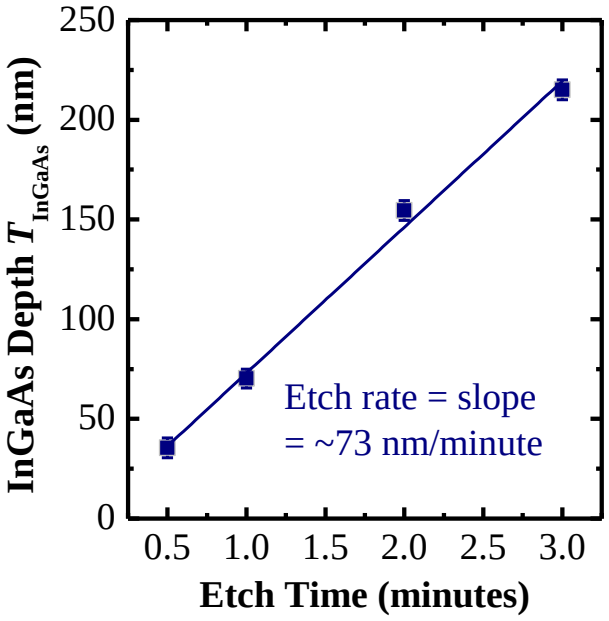


Fig. 4.3. T_{InGaAs} as a function of etch time. The measured step height from a surface profiler has an error less than 10 nm. Multiple measurements were done at each etch time and the obtained step height shows small standard deviation.

4.2.3 Plasma Etch of InGaAs Fin

To realize InGaAs fin structure, plasma etch of InGaAs needs to be developed. Chlorine (Cl_2) is one of the common gases that can be used for etching InGaAs. The spontaneous chemical etch rates of InGaAs at room temperature in Cl_2 are negligible and the practical removal rates are only obtained under ion-assisted conditions [4.23]-[4.25]. Table 4.2 summarizes the possible etch products and their volatilities for InGaAs etched in a Cl_2-based plasma [4.23]. It is noticed that $InCl_x$ has a boiling point of ~600 ℃ and has a much lower volatility as compared with $GaCl_3$ and $AsCl_3$ [4.23]. The etch process could be facilitated at elevated temperatures. However, raising the process temperature to ~600 ℃ is impractical for most of the etchers.

Table 4.2. Possible etch products and their volatilities for InGaAs etched in Cl_2-based plasma [4.23].

Substance	Boiling Point (˚C)	Melting Point (˚C)
$GaCl_3$	201	78
$AsCl_3$	130	-8.5
$InCl_3$	600	586
$InCl_2$	550	235
InCl	608	225

Table 4.3. Recipe that was used for InGaAs etch. Ar was introduced to Cl_2 to facilitate the etch process.

Temperature (˚C)	RF Power (W)	Substrate Bias (V)	Pressure (mTorr)	Cl_2 /Ar Flow Rate (sccm)
25	400	-200	10	200/100

In this Chapter, we introduced a noble gas additive Ar to Cl_2 plasma in order to facilitate the ignition of the discharge at low pressure and also enhance the efficiency of desorption of etch products by ion bombardment [4.24]. InGaAs etch was performed at room temperature and the etch recipe used is shown in Table 4.3. RF power and substrate bias are 400 W and -200 V, respectively. The process pressure was maintained at 10 mTorr. Cl_2 has a flow rate of 200 sccm and Ar has a flow rate of 100 sccm. InGaAs wafers were patterned with photoresist and then etched for 40, 50 and 70 s using the above recipe. After etch, photoresist was stripped and etch step height T_{InGaAs} was measured by surface profiler. T_{InGaAs} (squares) as a function of etch time is plotted in Fig. 4.4. The etch rate is about 2.4 nm/s as obtained from the slope of the linear fit line (solid line).

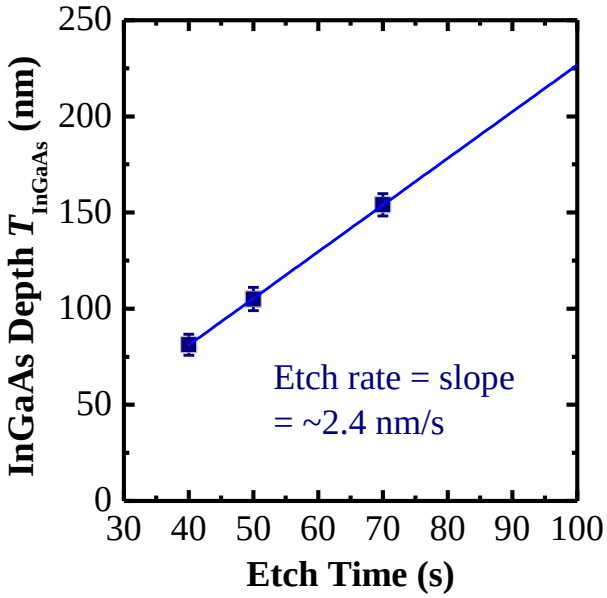


Fig. 4.4. T_{InGaAs} as a function of etch time. Surface profiler was used to measure the step height. Multiple measurements were performed at each etch time and the obtained step height shows small standard deviation. The solid line is a linear line fit of the measured data (squares).

We need to note that typical ion energies in reactive ion etching (RIE) are ~200 eV which is well above the atomic displacement threshold in III-V material (15 – 50 eV) [4.25]. Therefore, the process inevitably leads to substantial introduction of point defects. In this Chapter, a wet etch was used to remove the damaged region right after the fin formation, which will be discussed later.

4.2.4 Electrical Properties of Ni-InGaAs Contacts

Ni-InGaAs formation was discussed in detail in Chapter 3. In this Chapter, Ni-InGaAs contacts was formed on *in-situ* Si-doped n^+ InGaAs and TLM test structures were fabricated to extract the R_C. The n^+ InGaAs has a N_D of 5×10^{19} cm^{-3} and this doping concentration is over 10 times higher than the S/D doping (~2×10^{18} cm^{-3}) achieved by Si implant in Chapter 3. The higher N_D allows the achievement of lower R_C since R_C is a strong function of N_D, as discussed in Chapter 2 [Equations (2.1) and (2.2)]. The starting substrate for TLM fabrication is illustrated in Fig. 4.5.

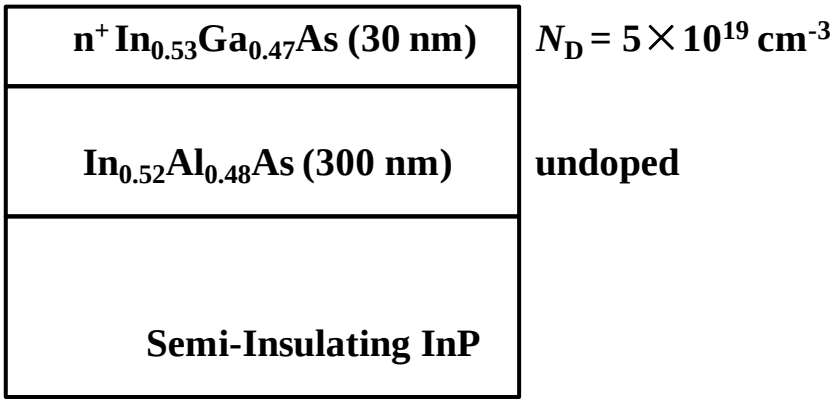


Fig. 4.5. The layer structure of III-V substrate for TLM fabrication. This is different from the sample used for FinFET fabrication. The wafer has n^+ $In_{0.53}Ga_{0.47}As$ (100 nm) with N_D of 5×10^{19} $cm^{-3}$and undoped $In_{0.52}Al_{0.48}As$ (300 nm) layers grown on 2-inch InP substrate.

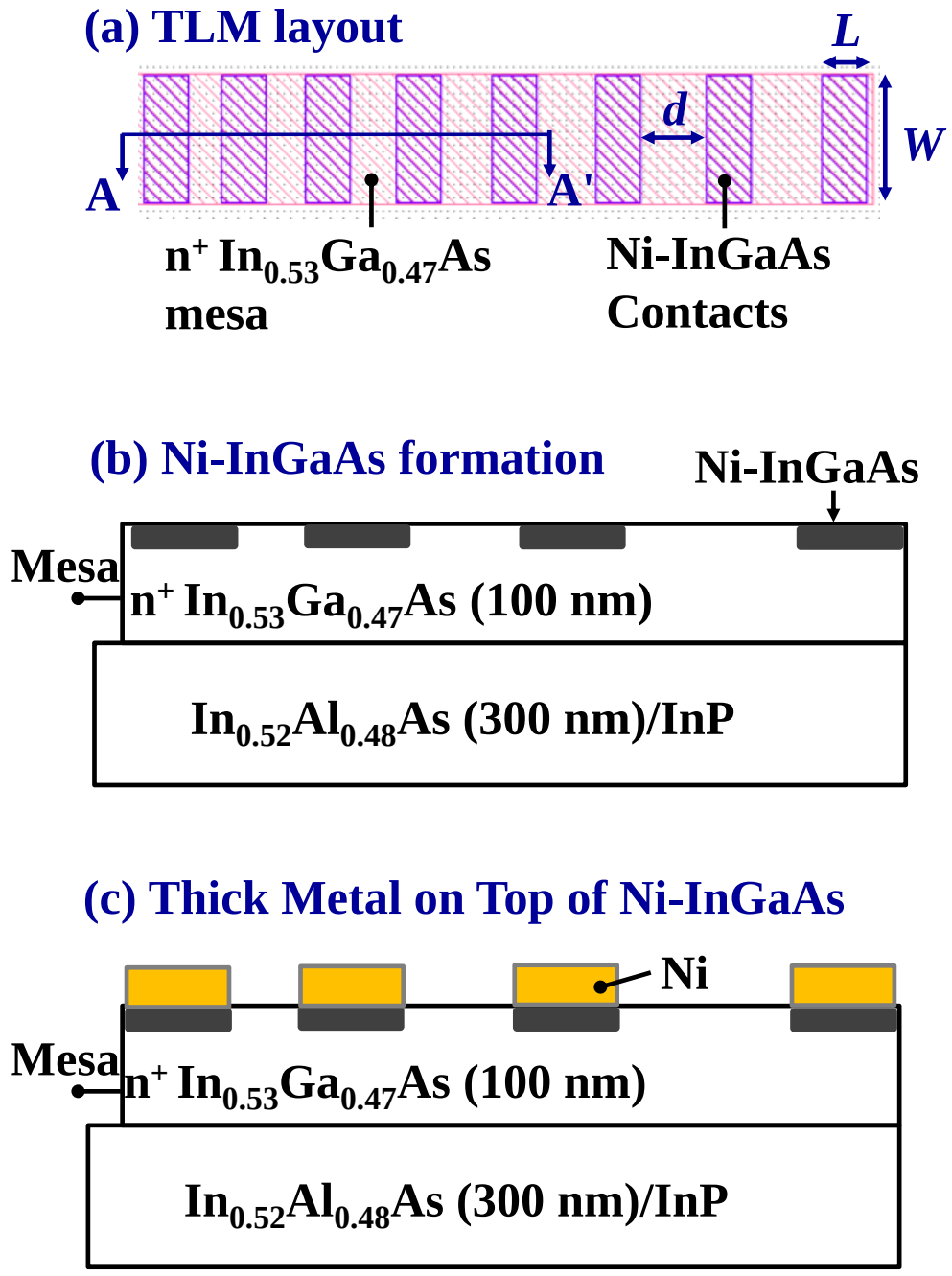


Fig. 4.6. (a) Layout of TLM test structure. Contact width and contact length are *W* and *L*, respectively. *d* is contact spacing. Before Ni-InGaAs formation, n^+ InGaAs mesa was formed by wet etch. (b) Cross-section of the TLM structure along A-A' illustrates Ni-InGaAs formation on top of n^+ InGaAs. (c) A thick Ni layer (300 nm) was deposited on top of Ni-InGaAs to reduce metal resistance.

The first step for TLM fabrication is to form n^+ InGaAs mesa by wet etch using $C_6H_8O_7/H_2O_2$ (20: 1). Fig. 4.6(a) shows the layout of a TLM structure and the cross-section along A-A' was shown in (b) and (c). After mesa formation, Ni pads with thickness of ~30 nm were deposited on n^+ InGaAs using a lift-off process. RTA at 250 ℃ for 60 s was performed to initiate the reaction between Ni and n^+ InGaAs and form Ni-InGaAs [Fig. 4.6(b)]. Finally a thick layer of Ni (~300 nm) was deposited on top of Ni-InGaAs by electron beam evaporation [Fig. 4.6(c)]. The thick metal reduces metal resistance and improves the accuracy of R_C extraction. The R_C measured from a TLM structure includes the metal resistance and the metal resistance is negligible when the R_C is large [4.26]. However, for small R_C the metal resistance may no longer be negligible and could substantially affect the accuracy of R_C extraction. Therefore, a thick metal on top of Ni-InGaAs is deposited to reduce the metal resistance.

The TLM structures were electrically characterized. Fig. 4.7(a) inset shows the current-voltage characteristics measured from adjacent Ni-InGaAs contacts with different contact spacing d in a TLM structure. Good ohmic behavior is observed. The total resistance R_T between two Ni-InGaAs contacts as a function of d is also plotted in Fig. 4.7(a). The solid line is the linear fit of these data points. The intercept at contact spacing $d = 0$ is $R_T = 2R_C$, giving Ni-InGaAs R_C of 79 Ω·μm. The sheet resistance for n^+ InGaAs is obtained from the slope of fitted line to be ~14 Ω/square. The intercept at $R_T = 0$ is $-d = 2L_T$ giving transfer length L_T of ~2.1 μm. Both contact length L and contact width W of the TLM are 100 μm and thus the assumption of $L > 1.5L_T$ is valid. The specific contact resistivity ρ_C could be obtained

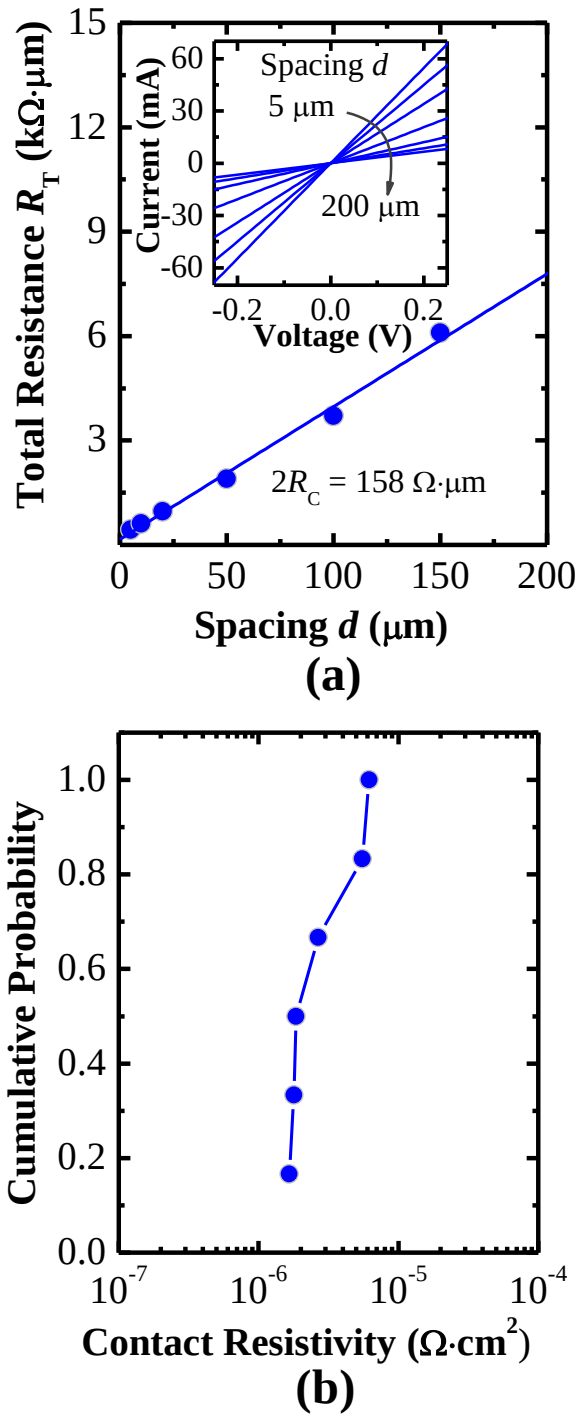


Fig. 4.7. (a) Plot of R_T between two Ni-InGaAs contacts as a function of contact spacing d. d varies from 5 to 200 μm. The solid line is the linear fit of the data points. The current-voltage characteristics measured from adjacent Ni-InGaAs contacts is shown in the inset. (b) Cumulative plot showing a tight distribution of ρ_C measured from 10 TLM test structures. ρ_C is extracted to be in the order of 1×10^{-6} Ω·cm^2.

by [4.26]

$$\rho_C \approx R_C L_T W . \qquad (4.2)$$

The calculated specific contact resistivity ρ_C is ~1.6×10^{-6} Ω·cm^2. Statistical plot in Fig. 4.7(b) shows a tight distribution of ρ_C measured from a number of TLM structures. It shows that Ni-InGaAs contacts on n^+ InGaAs have a low ρ_C in the order of 1×10^{-6} Ω·cm^2, similar to the value reported in Ref. [4.27].

4.3 Device Integration and Characterization

4.3.1 Integration of InGaAs FinFETs with Self-Aligned Ni-InGaAs Contacts

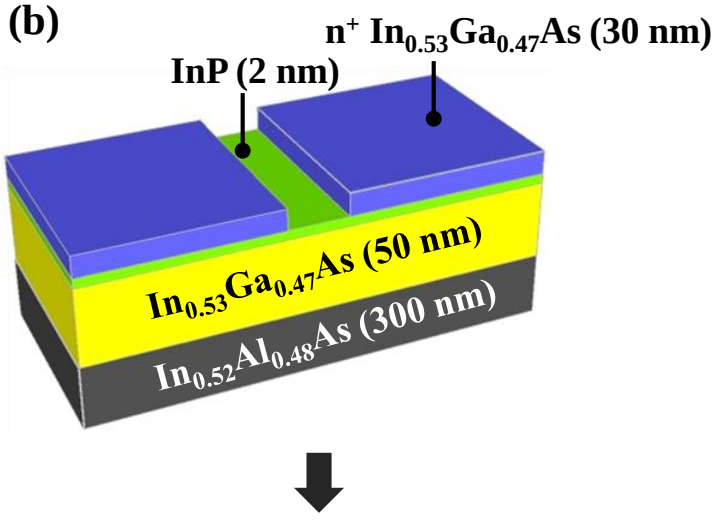
The fabrication process for InGaAs FinFET is summarized and illustrated in Fig. 4.8. The channel region was patterned by electron beam lithography (EBL) using a positive photoresist (ZEP 520A). InGaAs channel was exposed [Fig. 4.8(b)] by wet etch of n^+ InGaAs using $C_6H_8O_7/H_2O_2$ (20: 1) solution which allows selective etch of InGaAs with respect to InP. Then, InGaAs fins were patterned using a negative photoresist (NEB 22) and formed by Cl_2-based plasma etch [Fig. 4.8(c)], as documented in Section 4.2.3. Fin sidewalls could be damaged during the plasma etch. A quick dip of about 5 s in $C_6H_8O_7/H_2O_2$ (20: 1) solution was used to remove the damaged regions of the InGaAs fins.

Prior to high-*k* dielectric deposition, diluted hydrofluoric acid (HF) was used to remove any native oxide on the InGaAs surface. Ammonium sulfide [$(NH_4)_2S$] solution was used for passivating the InGaAs surface for suppression of surface oxidation. The samples were then loaded into an ALD tool for Al_2O_3 deposition (~6 nm). Next, ~70 nm TaN metal layer was deposited by sputtering, patterned by EBL, and etched by Cl_2-based plasma [Fig. 4.8 (d)]. After TaN etch, the remaining Al_2O_3 on S/D regions was removed by diluted HF. The samples subsequently went through the salicide-like Ni-InGaAs metallization process [4.15]-[4.18]. About 13 nm of Ni was deposited by electron beam evaporation, followed by a RTA at 250 ˚C for 60 s in N_2 ambient. The fabrication process was completed with selective removal of unreacted Ni in concentrated HCl solution [4.28]. The final structure of the FinFET formed is shown in Fig. 4.8(e).

(a) Process flow:

- Patterning of n^+ $In_{0.53}Ga_{0.47}As$
  - Electron beam lithography
  - Wet etch of n^+ $In_{0.53}Ga_{0.47}As$
- $In_{0.53}Ga_{0.47}As$ Fin Formation
  - Electron beam lithography
  - Dry etch of $In_{0.53}Ga_{0.47}As$ fins
  - Wet etch for damage removal
- Gate Stack Formation
  - Substrate pre-clean
  - Al_2O_3 and TaN deposition (250 ˚C)
  - TaN patterning and dry etch
- Self-Aligned Metallization
  - Ni deposition followed by anneal (250 ˚C)
  - Selective wet etch of unreacted Ni

(b)



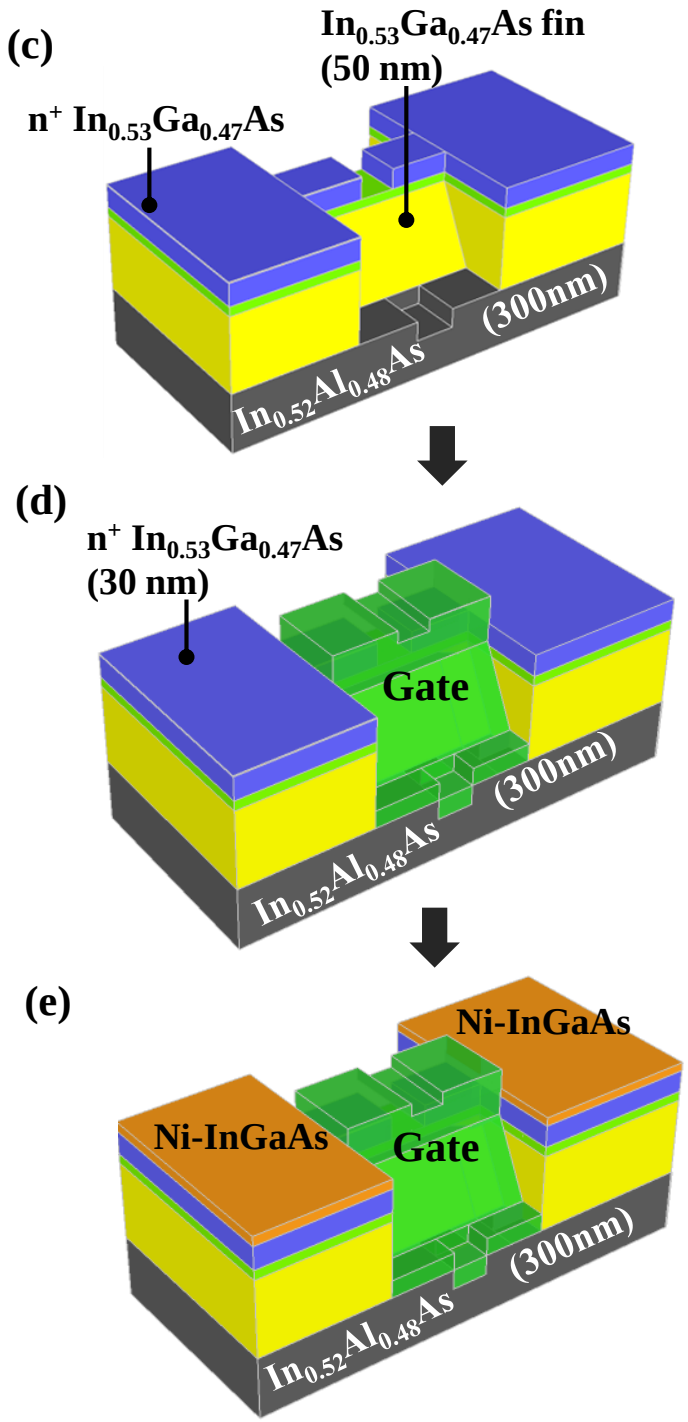


Fig. 4.8. (a) Process flow for fabricating InGaAs FinFETs with self-aligned Ni-InGaAs contacts. The key steps include (b) recess etch of n^+ InGaAs, (c) plasma etch of InGaAs fin, (d) gate stack formation, and (e) self-aligned metallization.

4.3.2 Device Characterization and Analysis

Scanning Electron Microscopy (SEM) image in Fig. 4.9 shows the top view of an InGaAs FinFET device. Fig. 4.9(a) is a zoomed-out view of the device and it shows the device layout. The ring-shaped gate line is used for device S/D isolation during the self-aligned Ni-InGaAs metallization. A zoomed-in view of the device channel region is shown in Fig. 4.9(b). The recessed part of the n^+ InGaAs layer defines the device channel L_{CH} and also separates the source and drain. The recess pattern of the n^+ InGaAs layer was transferred to the InAlAs layer during the dry etch of the InGaAs fin, thus forming trenches adjacent to the fin. InGaAs fin and gate line are oriented in the horizontal and vertical directions, respectively [Fig. 4.9(b)].

Transmission Electron Microscopy (TEM) image in Fig. 4.10(a) shows the device cross-section along the dashed line A - A' in Fig. 4.9(b). The Ni-InGaAs contact appears as a darker layer, uniformly formed on the surface of n^+ InGaAs and aligned to the gate electrode. The clear interface between Ni-InGaAs and InGaAs can be observed in a zoomed-in view in Fig. 4.10(b). Ni-InGaAs has a thickness of about 20 nm with sheet resistance of ~43 Ω/square. Fig. 4.11(a) shows the cross-section of the device along the dashed line B - B' as indicated in Fig. 4.9. The formed InGaAs fin has a trapezoid shape with a top width of 80 nm and bottom width of 170 nm. The height of InGaAs channel is ~50 nm. A zoomed-in view in Fig. 4.11(b) shows that the Al_2O_3 and TaN layers were uniformly deposited on the top and sidewalls of the InGaAs fin. The top surface of the fin is capped by 2 nm of InP while the InGaAs fin sidewalls are not capped by InP.

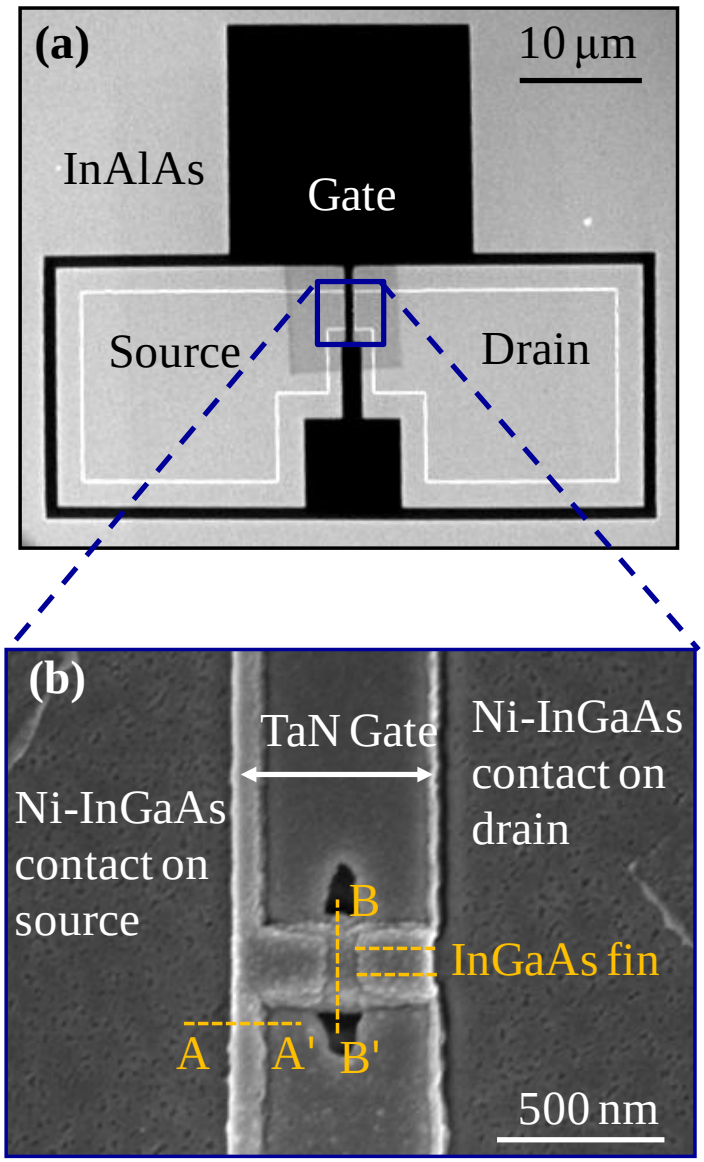


Fig. 4.9. (a) SEM image shows the zoomed-out view of a FinFET device. The gate line surrounding source and drain region is sitting on InAlAs barrier layer. (b) Zoomed-in view of the device channel region. The Ni-InGaAs contacts are formed on n^+ InGaAs and aligned to the TaN gate. The n^+ InGaAs recess region defines the device channel. The InGaAs fin is oriented in the horizontal direction. The cross-section views along A - A' and B - B' are shown in Fig. 4.10 and Fig. 4.11, respectively.

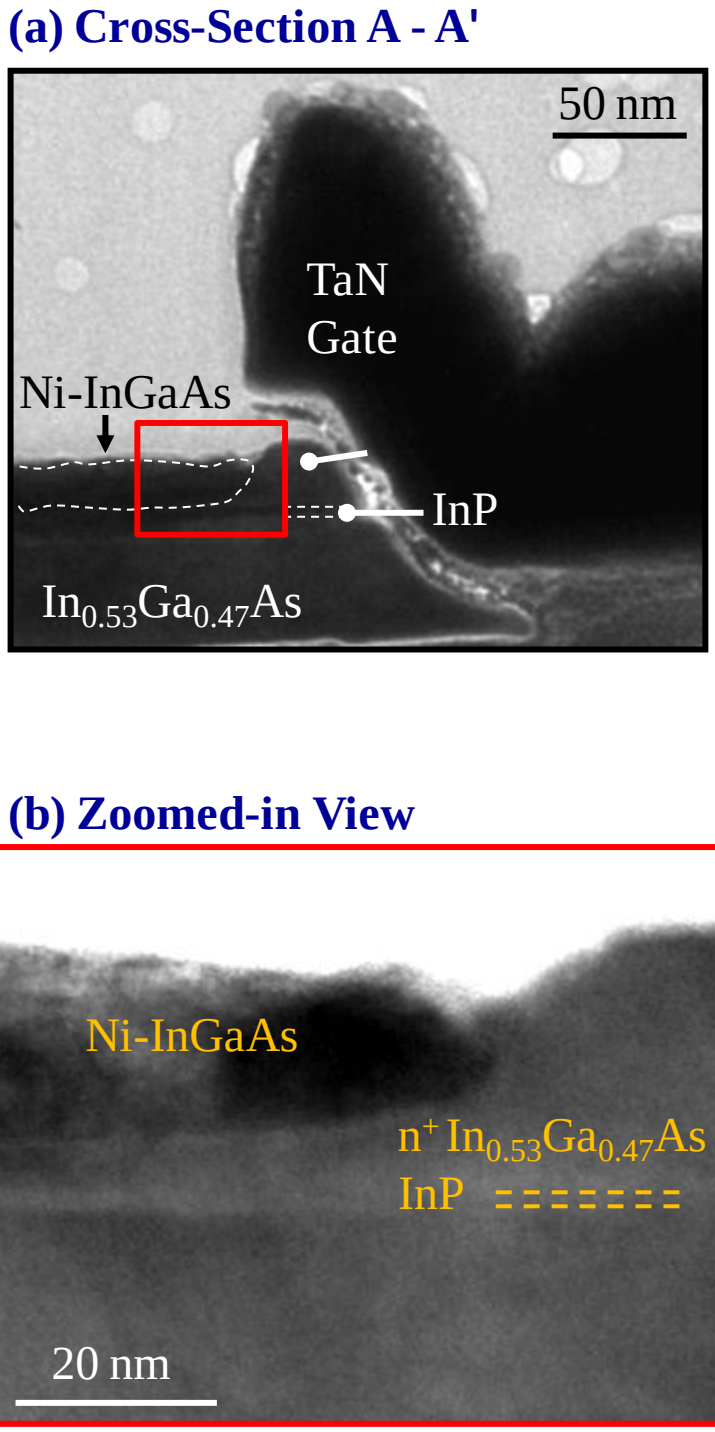


Fig. 4.10. (a) TEM image shows the device cross-section along A - A' in Fig. 4.9(b). Ni-InGaAs contact was uniformly formed on n^+ InGaAs and well aligned to the TaN gate. (b) Zoomed-in view of the rectangular region shows that the Ni-InGaAs layer has clear interface and shows good contrast with respect to n^+ InGaAs.

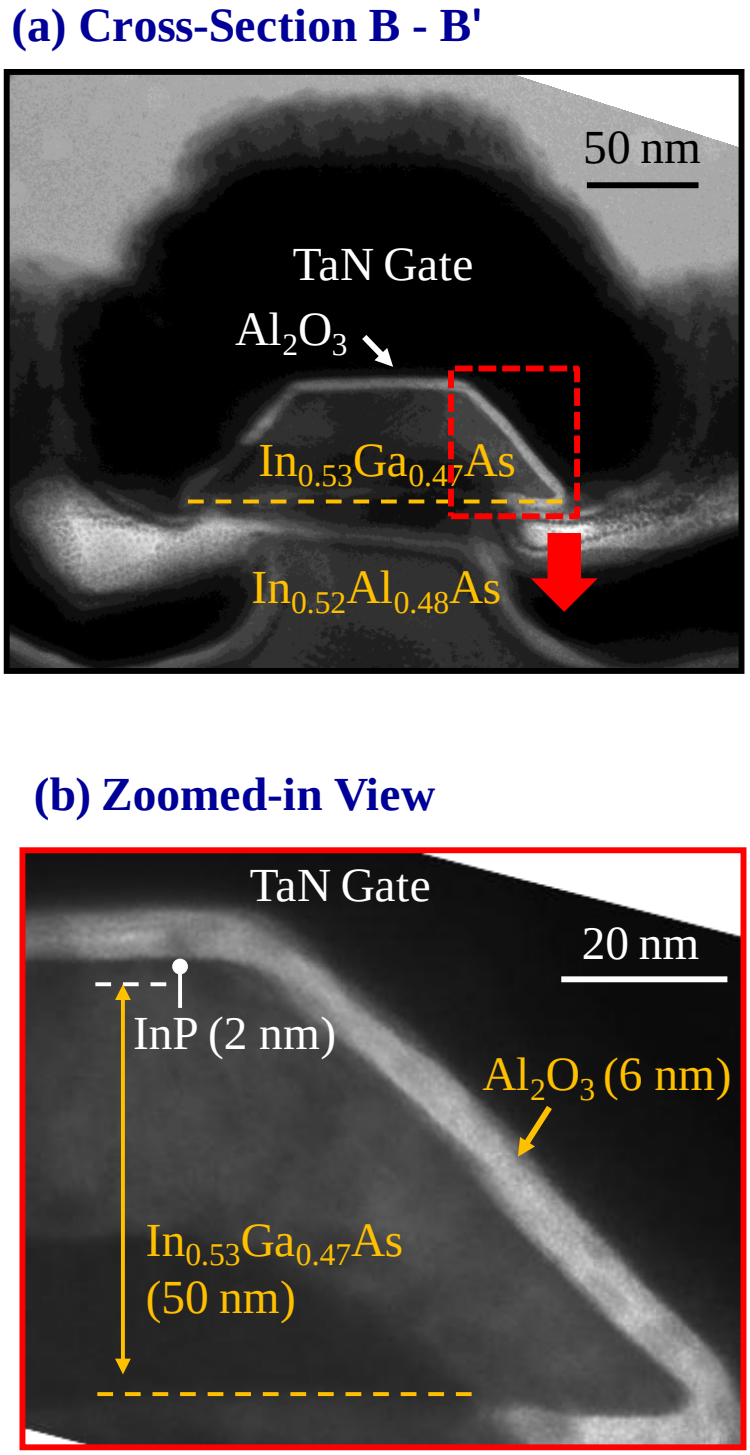


Fig. 4.11. (a) TEM shows the device cross-section along dashed line B - B' in Fig. 4.9(b). The InGaAs fin is in the shape of a trapezoid. Undercutting of the InAlAs layer beneath the InGaAs fin is observed due to the $C_6H_8O_7/H_2O_2$ dip after InGaAs fin etch [4.22]. (b) Zoomed-in view of the InGaAs fin sidewalls, showing that the Al_2O_3 and TaN were uniformly deposited on the top and sidewalls of the fin. The Al_2O_3 has a thickness of ~ 6 nm.

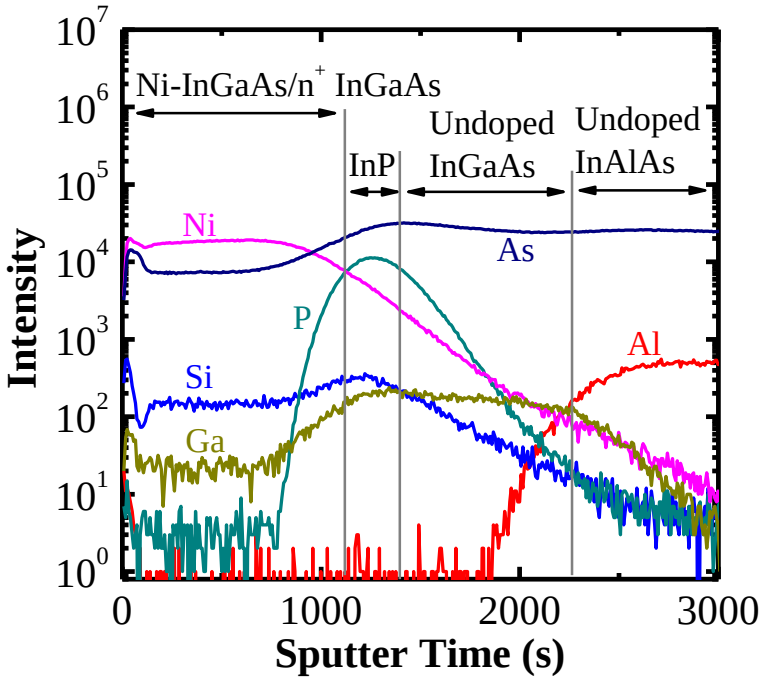


Fig. 4.12. SIMS profile shows the distribution of elements such as Ni, Si, Ga, As, Al, and P in the S/D regions. A uniform Ni-InGaAs layer on n^+ InGaAs was observed. The vertical gray lines are the estimated positions of materials interfaces.

Secondary Ion Mass Spectrometry (SIMS) was performed in device S/D regions and the elemental profile is shown in Fig. 4.12. The distribution of elements confirms the formation of Ni-InGaAs on the surface of n^+ InGaAs S/D. A uniform Ni profile (the pink curve) within Ni-InGaAs layer is observed. The blue curve also shows a uniform Si dopant profile in n^+ InGaAs layer. The vertical gray lines indicate the approximate positions of materials interfaces.

Fig. 4.13(a) shows the drain current versus gate voltage (I_D -V_G) plot of an InGaAs FinFET with L_{CH} of 50 nm. Drain voltage V_D of 0.05 and 0.5 V were applied. The device exhibits good transfer characteristics and shows substhreshold swing S of 169 mV/decade at V_D of 0.05 V. Extrinsic transconductance versus gate voltage ($G_{m,ext}$ - V_G) in Fig. 4.13(b) indicates peak $G_{m,ext}$ of 590 μS/μm at V_D of 0.5 V. I_D–V_D

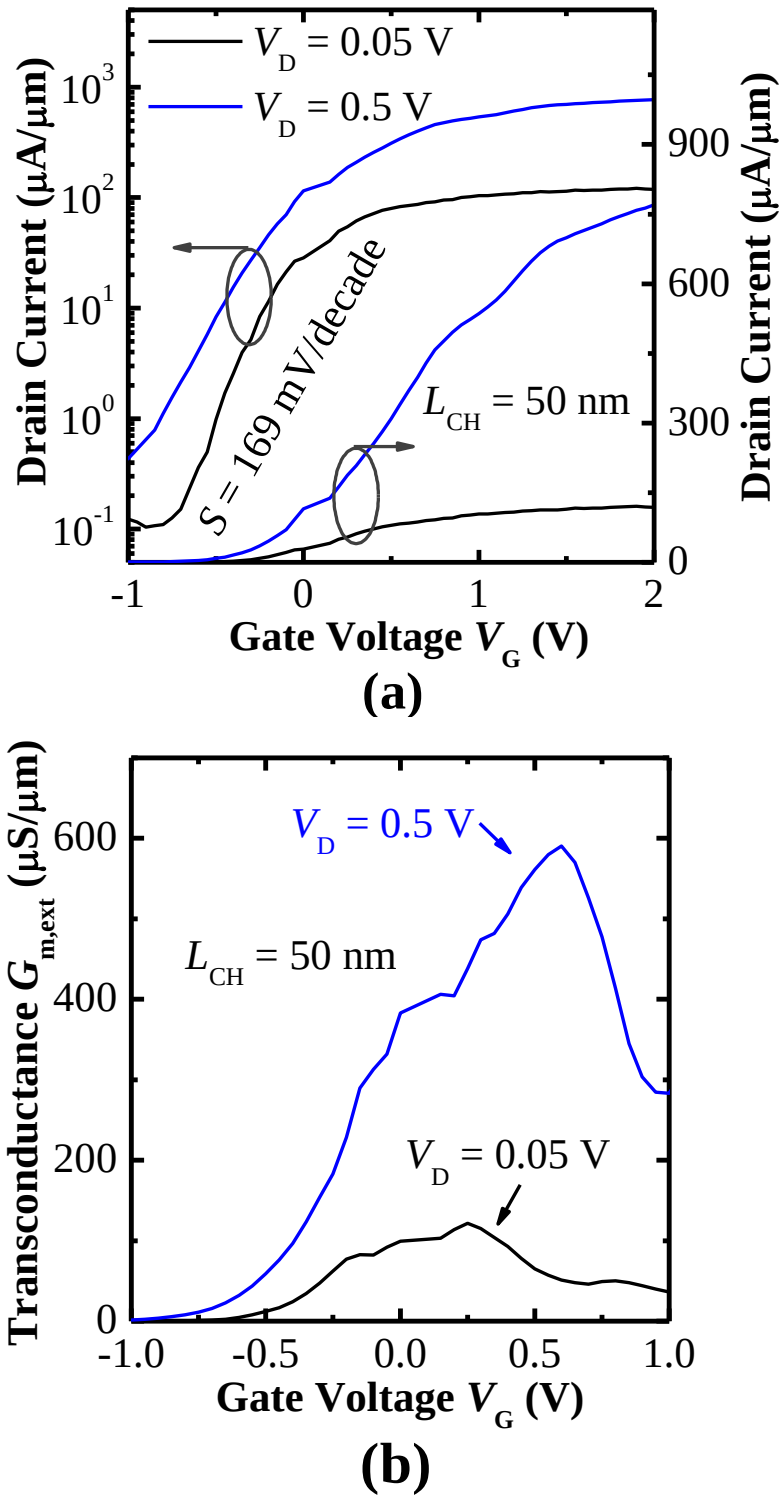


Fig. 4.13. (a) I_D–V_G curves of an InGaAs FinFET with channel length L_{CH} of 50 nm. The device shows good transfer characteristics with subthreshold swing S of 169 mV/decade and on-state/off-state drain current ratio of ~10^3. (b) $G_{m,ext}$–V_G of the device shows a peak $G_{m,ext}$ of 590 μS/μm at V_D of 0.5 V.

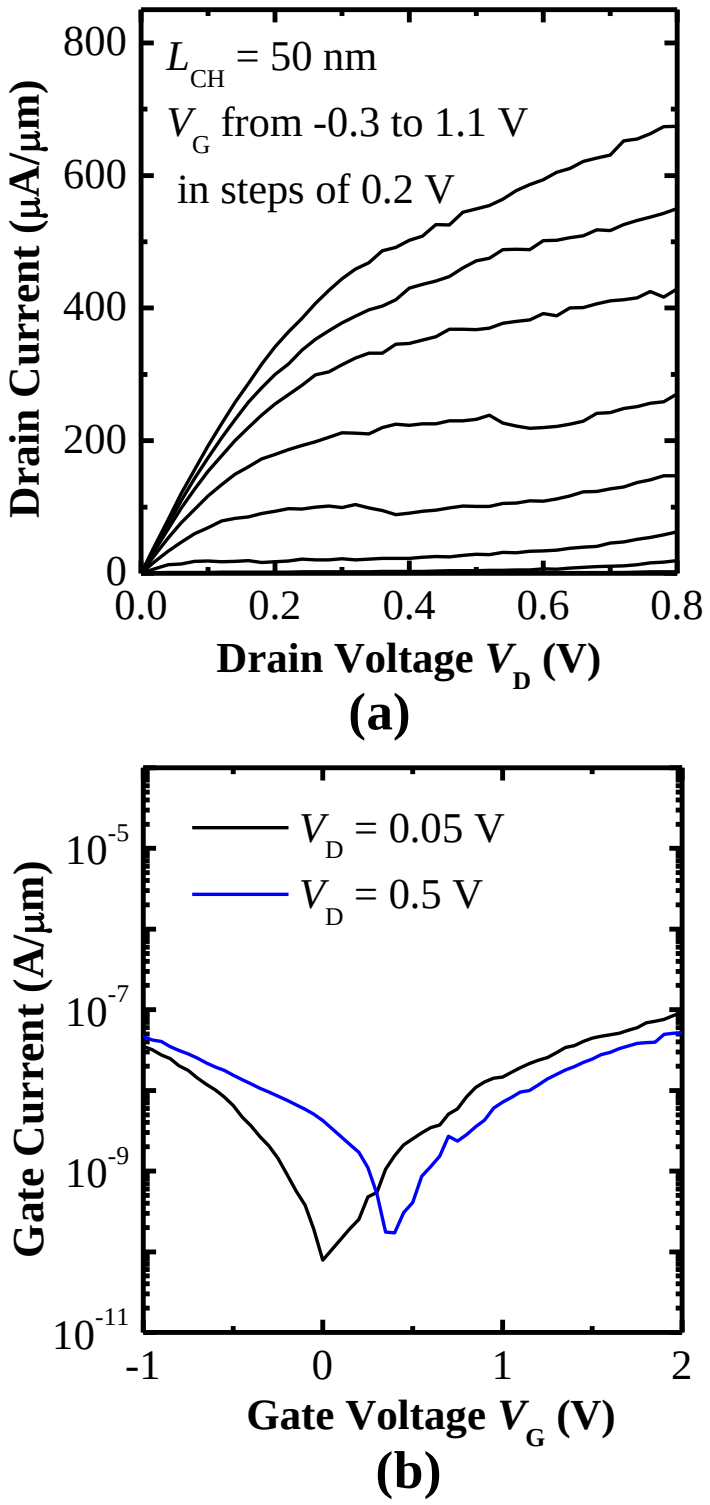


Fig. 4.14. (a) I_D –V_D curves of the same device in Fig. 4.13 show good output characteristics. Drive current of 411 μA/μm was obtained at V_D of 0.7 V and V_G of 0.7 V. (b) I_G-V_G of the device shows low gate leakage current below the level of 1×10^{-7} A/μm.

[Fig. 4.14 (a)] curves of the same device in Fig. 4.13 show good saturation and pinch-off characteristics. The gate voltage was varied from -0.3 V to 1.1 V in steps of 0.2 V. Drive current of 411 μA/μm was achieved at V_D of 0.7 V and V_G of 0.7 V. Drive current and $G_{m,ext}$ were normalized by the effective width W_{eff} of the device, which is the sum of the widths contributed by the InGaAs fin top channel (W_{top}) and two sidewalls channel ($2W_{side}$) [4.29]. W_{eff} is ~0.2 μm as obtained from TEM in Fig. 4.11. The obtained drive current and $G_{m,ext}$ are quite good considering the large EOT of ~3 nm used. Gate leakage current versus gate voltage (I_G-V_G) of the device is plotted in Fig. 4.14(b), showing gate leakage current of 3 to 4 orders of magnitude lower than the drive current.

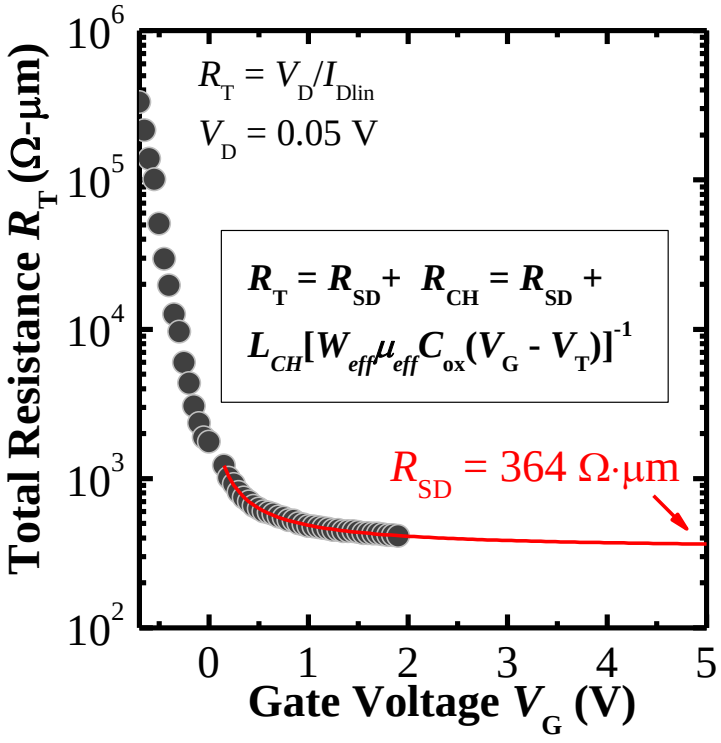


Fig. 4.15. R_T in the linear regime (V_D = 0.05 V) as a function of V_G. $R_T = V_D/I_{Dlin}$, where I_{Dlin} is the drain current in linear regime. The solid curve is given by Equation (4.3), and was used to fit the data points (circles). The fitted curve was extrapolated to V_G = 5 V to obtain R_{SD}.

In Fig. 4.15, the total resistance R_T in the linear regime (V_D = 0.05 V) as a function of V_G is plotted. The equation for the fitted curve (solid curve) is given by [4.26]

$$R_T = R_{SD} + R_{CH} = R_{SD} + L_{CH}[W_{eff}\mu_{eff}C_{ox}(V_G\text{-}V_T)]^{-1}, \quad (4.3)$$

where L_{CH} is channel length, W_{eff} is device effective width, μ_{eff} is channel effective mobility, C_{ox} is gate oxide capacitance, and V_G-V_T is gate overdrive. The fitted curve was extrapolated to V_G = 5 V and low R_{SD} of 364 Ω·μm was obtained. R_{SD} represents the sum of series resistance component in the source R_S and in the drain R_D, i.e. R_{SD} = $2R_S = 2R_D$. We calculated the device channel resistance R_{CH} using

$$R_{CH} = R_T - R_{SD}. \quad (4.4)$$

At V_D of 0.05 V, R_{CH} are 265, 192, and 136 Ω·μm at applied V_G of 0.5, 0.7, and 0.9 V, respectively, as shown in Table 4.4. Although the device has a low R_{SD} of 364 Ω·μm in this Chapter, R_{SD} is larger than R_{CH} when the device is operated at V_G equal to or greater than 0.5 V. In this case, R_{SD} will dominate R_T. Table 4.4 shows that R_{SD} takes up almost 73% of R_T at applied V_G of 0.9 V. Further reduction of R_{SD} is needed to improve the device drive current performance.

Table 4.4. Contributions of series resistance R_{SD} to device total resistance R_T.

V_G (V)	R_T (Ω·μm)	R_{CH} (Ω·μm)	R_{SD} (Ω·μm)	R_{SD}/R_T (%)
0.5	629	265	364	58
0.7	556	192	364	65
0.9	500	136	364	73

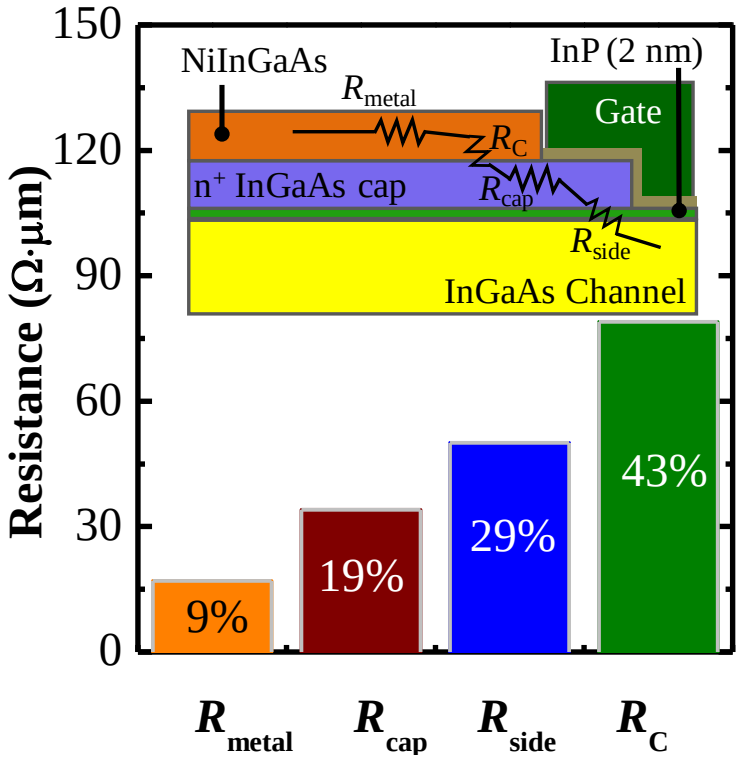


Fig. 4.16. Estimated resistance components of the source resistance R_S (R_{SD} = $2R_S$ = $2R_D$ = 364 Ω·μm). R_C and R_{side} are the dominant source resistance in this self-aligned FinFET structure. The percentages shown are the percentage contributions of the various components to R_S.

The plot in Fig. 4.16 shows the estimated component elements of the source resistance R_S. In order to evaluate the individual resistance contributions, each component of R_S should be normalized to the effective width W_{eff} of the device, as was done for R_{SD}. Ni-InGaAs resistance (R_{metal}) is calculated to be about 17 Ω·μm based on the Ni-InGaAs sheet resistance (~43 Ω/square) and the device source geometry as shown in Fig. 4.9. Another resistance component is the n^+ InGaAs cap resistance (R_{cap}) between Ni-InGaAs contact and InGaAs channel due to the gate-to-source overlap. N^+ InGaAs has a thickness of 30 nm and a sheet resistance ($R_{sh,InGaAs}$) of ~55 Ω/square. The length of gate-to-source overlap ($L_{overlap}$) is ~250 nm and the

top width (W_{top}) of n^+ InGaAs is ~ 80 nm. The n^+ InGaAs cap resistance can be calculated by

$$R_{cap} = (L_{overlap}/W_{top}) \times R_{sh,InGaAs}. \quad (4.5)$$

The calculated R_{cap} value is ~172 Ω. After the resistance was normalized by W_{eff}, R_{cap} is 34 Ω·μm. Ni-InGaAs contact resistance R_C in source is about 79 Ω·μm, as obtained from the TLM structures. The remaining resistance (denoted as R_{side}) is ~52 Ω·μm, which includes InP barrier resistance and spreading resistance in source. From the above calculation, it is found that R_C and R_{side} take up 29% and 43% of total source resistance R_S, respectively. R_C and R_{side} dominate the R_S in this self-aligned FinFET structure. Reduction of InP (2 nm) thickness and doping InGaAs fin could further reduce the barrier resistance [4.3] and spreading resistance. Another option is to employ new contact materials such as non-alloyed Molybdenum (Mo) which has been reported to show almost 1 order of magnitude lower R_C (7 Ω·μm) on n^+ InGaAs [4.30]. The integration of self-aligned Mo contacts for InGaAs FinFETs will be discussed in next Chapter.

Fig. 4.17(a) benchmarks R_{SD} of this Chapter with reported values for InGaAs planar and non-planar devices. Ref. [4.31] reported the lowest R_{SD} of 93 Ω·μm for InGaAs planar MOSFETs, which already meets the R_{SD} requirement of 131 Ω·μm for III-V n-MOSFETs, as documented in ITRS [4.11]. However, the reported series resistances R_{SD} for InGaAs non-planar devices are over 1000 Ω·μm as shown in Table 4.1 and above the ITRS requirement. Much lower R_{SD} of 364 Ω·μm for InGaAs FinFETs is reported in this Chapter. This is due to self-alignment of the Ni-InGaAs contacts and its low R_C on *in-situ* doped n^+ InGaAs S/D.

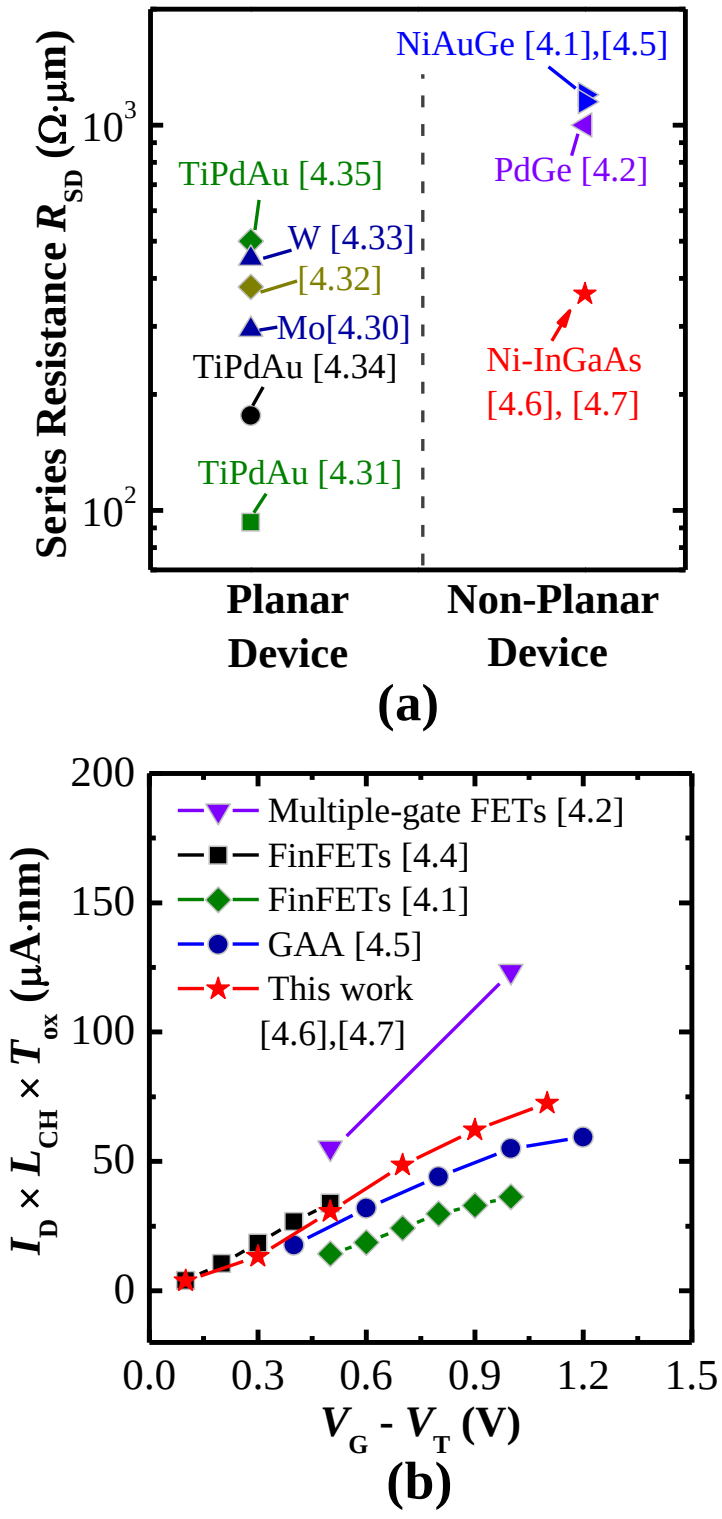


Fig. 4.17. (a) Much lower R_{SD} was obtained in this Chapter as compared with other reported R_{SD} for InGaAs non-planar devices with non-self-aligned contacts. (b) Plot of $I_D \times L_{CH} \times T_{ox}$ versus overdrive V_G–V_T for InGaAs non-planar n-MOSFETs reported in the literature and in this Chapter.

The saturation drive current of a transistor could be expressed as [4.36]:

$$I_D = \frac{W_{eff}\,\mu_{eff}\,\varepsilon_{ox}\,(V_G - V_T)^2}{2L_{CH} \times T_{ox}}, \qquad (4.6)$$

where L_{CH} is channel length, T_{ox} is equivalent oxide thickness (EOT), W_{eff} is device effective width, μ_{eff} is channel effective mobility, ε_{ox} is permittivity of SiO_2, and V_G-V_T is gate overdrive. Fig. 4.16(b) shows $I_D \times L_{CH} \times T_{ox}$ versus overdrive $V_G - V_T$ of InGaAs non-planar devices reported in the literature as well as the devices in this Chapter. Drive current performance in this Chapter is comparable to that of the best reported $In_{0.53}Ga_{0.47}As$ non-planar n-MOSFETs. The device in Ref. [4.2] has $In_{0.7}Ga_{0.3}As$ channel with a higher electron mobility, which may explain the much better drive current performance than the rest of the devices with $In_{0.53}Ga_{0.47}As$ channel. The drain induced barrier lowering of the device reported here is high (491mV/V), and is attributed to the undoped InGaAs fin, large fin width and large EOT. Better control of short-channel effects could be achieved by reducing the fin width and the EOT.

4.4 Summary

In this Chapter, a gate-last process for InGaAs FinFETs fabrication was introduced, with the successful development of selective wet etch of n^+ InGaAs, plasma etch of InGaAs fin, and self-aligned Ni-InGaAs metallization. Sub-100 nm InGaAs FinFETs with self-aligned Ni-InGaAs contacts formed on n^+ InGaAs source/drain were demonstrated. Good transfer and output characteristics were obtained. The device exhibits low series resistance R_{SD} of 364 Ω·μm, due to the self-alignment of Ni-InGaAs contacts and the low contact resistance R_C of Ni-InGaAs on n^+ InGaAs S/D. Various resistance components for series resistance and their contributions were analyzed. Ni-InGaAs contact resistance was found to be the dominant resistance component, contributing 43% to the device series resistance. Further work on contact resistance engineering is needed and will be carried out in next Chapter.

4.5 References

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Chapter 5

InGaAs FinFETs with Self-Aligned Non-Alloyed Molybdenum Contacts

5.1 Introduction

Several groups have demonstrated InGaAs channel non-planar n-MOSFETs in the past 3 years [5.1]-[5.7]. To reduce the source/drain (S/D) parasitic resistance (R_{SD}), a salicide-like, CMOS compatible self-aligned Ni-InGaAs metallization was recently developed for InGaAs FinFETs [5.6],[5.7], as documented in Chapter 4. By examining the state-of-art S/D contact technologies of InGaAs channel non-planar n-

Table 5.1. State-of-art S/D contact technologies for InGaAs non-planar n-MOSFETs.

InGaAs Non-planar Devices	**S/D Doping Method**	**Contact Materials**	**Self-Aligned Contacts**	**R_{SD} (Ω·μm)**	**Reference**
FinFETs (Purdue, 2009)	ion-implantation	NiAuGe	no	1200	[5.1]
Multiple-gate (NUS, 2011)	ion-implantation	PdGe	no	~1000	[5.2]
Tri-gate (Intel, 2010 & 2011)	*in-situ* doped	not reported	no	not reported	[5.3], [5.4]
GAA (Purdue, 2011)	ion-implantation	NiAuGe	no	1150	[5.5]
FinFETs (NUS, 2012)	***in-situ* doped**	**Ni-InGaAs**	**Yes**	**364**	**[5.6], [5.7]**

MOSFETs summarized in Table 5.1, it is noticed that a combination of *in-situ* doped S/D and self-aligned contact would help to reduce S/D R_{SD} greatly.

In Chapter 4, InGaAs FinFETs with S/D Ni-InGaAs contacts self-aligned to the gate stack was realized [5.6],[5.7]. The devices show much lower R_{SD} of 364 Ω·μm among the reported InGaAs non-planar n-MOSFETs. This is primarily attributed to the low contact resistance R_C of Ni-InGaAs and self-alignment of Ni-InGaAs to the gate stack. However, an analysis of the resistance components reveals that Ni-InGaAs has a R_C of 79 Ω·μm and contributes a significant portion ($2R_C$ = 158 Ω·μm) of ~43% to R_{SD} [5.7]. Therefore, reduced R_C between metal contact and n^+ InGaAs is needed to further reduce R_{SD}. Another resistance component for the FinFET structure discussed in Chapter 4 is the n^+ InGaAs cap resistance ($2R_{cap}$ = 68 Ω·μm) between Ni-InGaAs contact and InGaAs channel due to the gate-to-source/drain overlap. The n^+ InGaAs cap resistance contributes ~19% to R_{SD} [5.7]. A FinFET structure with S/D metal contact self-aligned to the InGaAs channel is also needed to reduce the resistance resulting from n^+ InGaAs.

In Section 5.2 of this Chapter [5.8], non-alloyed Molybdenum (Mo) is used as metal contacts formed on *in-situ* doped n^+ InGaAs S/D. Mo contact shows very low R_C on n^+ InGaAs [5.9],[5.10]. A novel gate-last process was designed to achieve the self-alignment of Mo contacts to InGaAs channel. By realizing such FinFET structure, R_{SD} as low as ~250 Ω·μm was achieved and this is the lowest value reported-to-date for InGaAs channel non-planar n-MOSFETs [5.8].

Various high-*k* dielectrics have been explored for InGaAs FinFETs to achieve good interface and small equivalent oxide thickness (EOT) [5.1]-[5.7], as summarized in Table 5.2. InGaAs FinFETs with $TaSiO_x$ achieves small *S* of ~95 mV/decade and small EOT of 1.2 nm at a channel length L_{CH} of 60 nm [5.4]. Al_2O_3 also has good interface quality with InGaAs but the dielectric constant of Al_2O_3 is only ~9 which is not high enough for aggressive EOT scaling. The smallest reported EOT for Al_2O_3 dielectric in InGaAs non-planar n-MOSFETs is still larger than 2 nm. To scale down EOT, a dual high-*k* HfO_2-on-Al_2O_3 stack (denoted as HfO_2/Al_2O_3) formed by atomic layer deposition (ALD) has been used in InGaAs planar n-MOSFETs. Good interface quality and small EOT can be achieved for HfO_2/Al_2O_3 due to the combined benefits of good interface quality of Al_2O_3 and high dielectric constant of HfO_2 [5.11]-[5.15]. Recent studies reveal that forming gas annealing (FGA) can further improve Al_2O_3 or HfO_2 dielectric quality by reducing the fixed oxide charge density (Q_f) as well as interface trap density (D_{IT}) [5.16]-[5.19].

Table 5.2. State-of-art gate stack technologies for InGaAs non-planar n-MOSFETs.

InGaAs Non-planar Devices	**Deposition Tool**	**High-*k* Materials**	**EOT (nm)**	***S* (mV/decade)** / **L_{CH} (nm)**	**Reference**
FinFETs (Purdue, 2009)	ALD	Al_2O_3	2~3	200	[5.1]
				100	
Multiple-gate (NUS, 2011)	MOCVD	HfAlO	5~6	~230	[5.2]
				130	
Tri-gate (Intel, 2010 & 2011)	ALD	$TaSiO_x$	1.2	~95	[5.3], [5.4]
				60	
GAA (Purdue, 2011)	ALD	Al_2O_3	~4.5	150	[5.5]
				50	
FinFETs (NUS, 2012)	ALD	Al_2O_3	~3	169	[5.6], [5.7]
				50	

In Section 5.3 of this Chapter, the integration of a dual high-k HfO_2/Al_2O_3 in InGaAs FinFETs with small EOT of ~1nm is described. Forming gas annealing at 300 ℃ for 30 minutes was performed for the FinFETs to further improve the quality of HfO_2/Al_2O_3 dielectric. FGA leads to significant improvement of subthreshold swing S and drive current. The InGaAs FinFETs with FGA show subthreshold swing S of 176 and 115 mV/decade at L_{CH} of 50 and 150 nm, respectively.

5.2 InGaAs FinFETs with Mo Contacts Self-Aligned to Channel

5.2.1 Molybdenum Contacts on n^+ InGaAs

TLM test structures were fabricated for the extraction of Mo contact resistance R_C on n^+ $In_{0.53}Ga_{0.47}As$. The starting substrate has 100 nm thick n^+ $In_{0.53}Ga_{0.47}As$ with doping concentration N_D of 5×10^{19} cm^{-3} and 300 nm thick

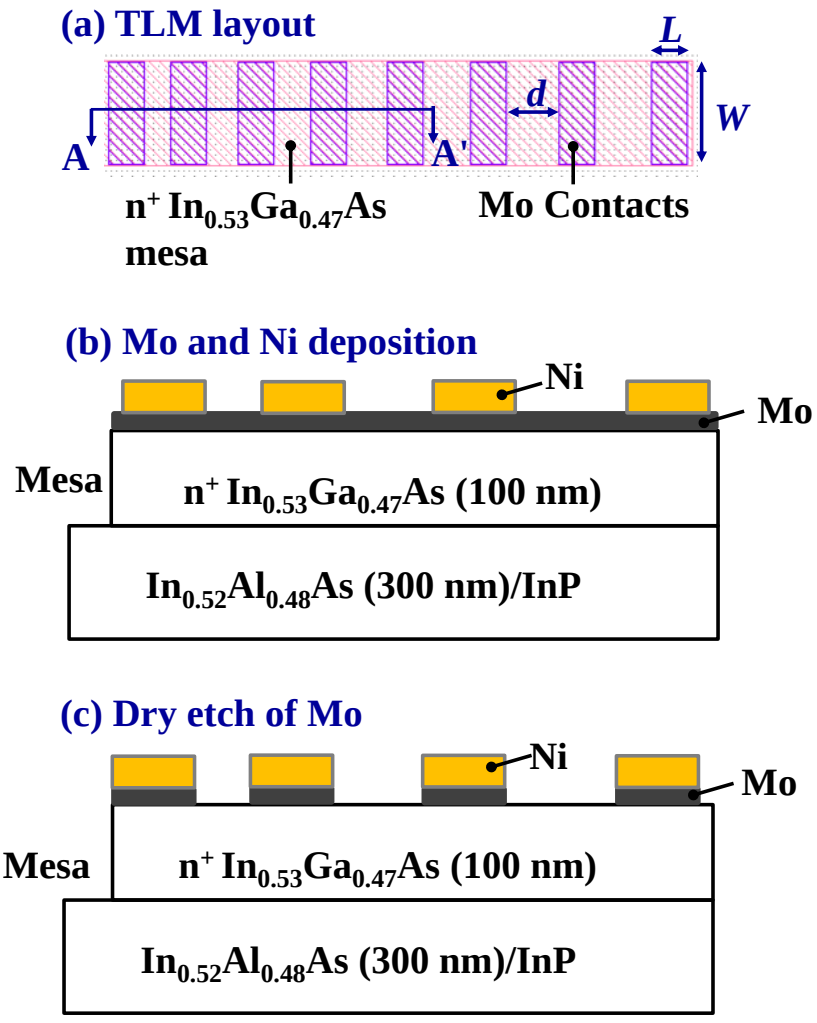


Fig. 5.1. (a) Layout of TLM test structure. *L*, *W*, *d* are contact length, width and spacing, respectively. (b) Cross-section of the TLM structure along A-A'. Blanket Mo film was sputtered on the substrate, followed by deposition of Ni pads (300 nm) using a lift-off process. (c) Mo layer was etched in Cl_2-based plasma using Ni as an etch mask. Finally, n^+ InGaAs mesa was formed by wet etch in citric acid based solution.

undoped $In_{0.52}Al_{0.48}As$ grown on InP. Fig. 5.1(a) shows the layout of a TLM structure. Both contact width W and contact length L are 100 μm. Contact spacing d varies from 5 to 200 μm. The wafer was dipped in hydrochloric acid (HCl: H_2O = 1: 3) to remove native oxide on the n^+ InGaAs surface. After that, the sample was quickly loaded into a sputtering chamber for ~40 nm Mo deposition. Ni pads with thickness of 300 nm were also deposited and patterned using a lift-off process, as shown in Fig. 5.1(b). Next, Mo film was etched by Cl_2-based plasma using Ni as an etch mask [Fig. 5.1(c)], since Cl_2 plasma almost does not etch Ni. The etch recipe is the same as the InGaAs fin etch recipe documented in Chapter 4 (Table 4.3). The etch rate for Mo and n^+ InGaAs are ~10 nm/s and ~2.4 nm/s, respectively. An etch selectivity of 4~5 is achieved for Mo with respect to n^+ InGaAs. The final step for TLM fabrication is to form n^+ InGaAs mesas by wet etch in the mixture of citric acid and H_2O_2 solution. The wet etch process was developed and documented in Section 4.2.1 of Chapter 4.

The fabricated TLM was electrically characterized. Fig. 5.2(a) plots total resistance R_T between two Mo contacts as a function of contact spacing d. The circles are experimental data and the solid curve is linear line fit. R_C extracted from the intercept (d = 0) is ~24 Ω·μm, which is comparable to the value reported in Ref. [5.9]. Fig. 5.2(a) inset shows plot of R_T versus d in logarithm scale. The vertical axis of R_T is plotted in logarithm scale to enable the observation of the intercept ($R_T = 2\ R_C$) which is ~48 Ω·μm. Statistical plot in Fig. 5.2(b) compares the specific contact resistivity ρ_C of Mo and Ni-InGaAs on n^+ InGaAs measured from a number of TLM structures. Mo contacts shows ρ_C in the order of $1\times10^{-7}\ \Omega\cdot cm^2$ and is about 10 times lower than that of Ni-InGaAs ($1\times10^{-6}\ \Omega\cdot cm^2$) [5.6],[5.7].

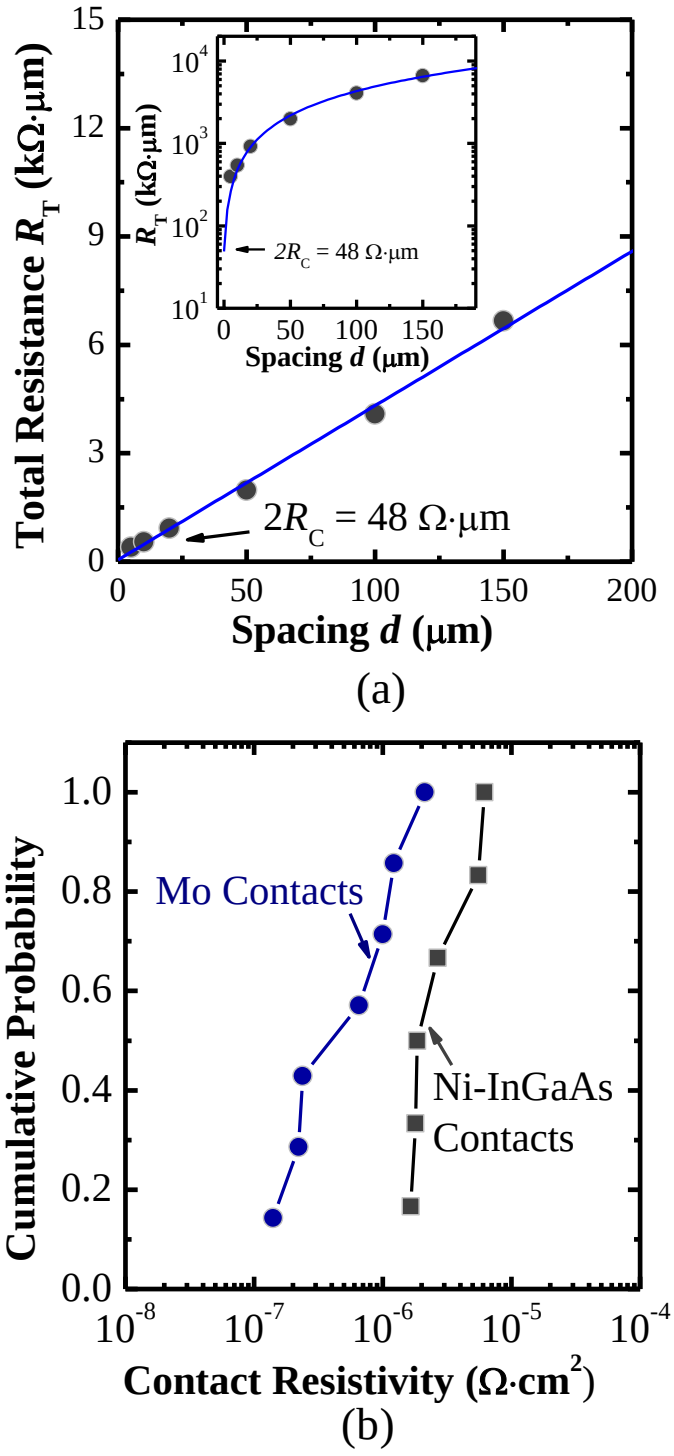


Fig. 5.2. (a) Total resistance R_T versus contact spacing d of a TLM. Mo contact shows low R_C of ~24 Ω·μm on n^+ InGaAs. The inset shows R_T versus d in logarithm scale. (b) Statistical plot shows the distribution of ρ_C for Mo and Ni-InGaAs contacts on n^+ InGaAs. Mo contact has a ρ_C ~10 times lower than that of Ni-InGaAs.

5.2.2 Integration of InGaAs FinFETs with Mo Contacts Self-Aligned to Channel

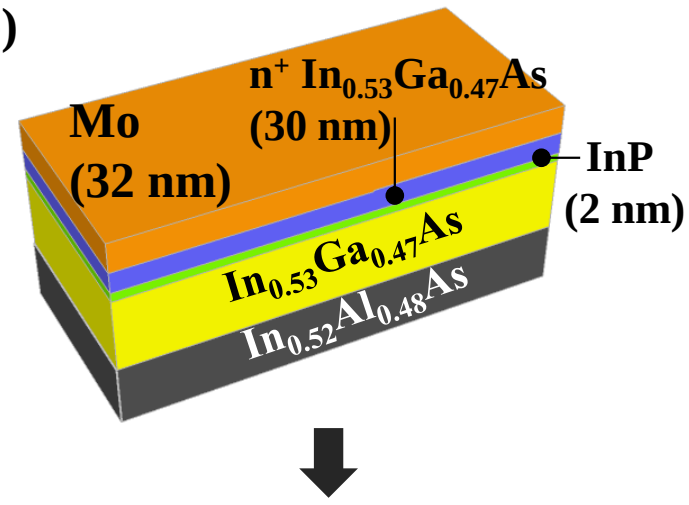
The process flow for the fabrication of InGaAs FinFETs with self-aligned Mo contacts is summarized in Fig. 5.3(a). InP wafers served as the starting substrates. Sequential epitaxy of 300 nm of undoped $In_{0.52}Al_{0.48}As$, 50 nm of undoped $In_{0.53}Ga_{0.47}As$ channel, 2 nm of undoped InP, and 30 nm of n^+ $In_{0.53}Ga_{0.47}As$ (N_D = 5×10^{19} cm^{-3}) was done by an external vendor. After native oxide removal in HCl solution, the sample was loaded into a sputtering chamber for Mo (~32 nm) deposition [Fig. 5.3(b)]. Mo-contacted S/D was patterned by electron beam lithography (EBL) using a positive photoresist (ZEP 520A) and formed by dry etch of Mo and wet etch of n^+ InGaAs [Fig. 5.3(c)]. The wet etch of n^+ InGaAs stops on InP and defines device channel. Then, InGaAs fins were patterned by EBL using a negative photoresist (NEB 22) and etched by Cl_2-based plasma [Fig. 5.3(d)]. Etch damage on InGaAs fin sidewalls was removed by wet etch in citric acid based solution.

After pre-gate clean in diluted hydrochloric acid (HF), and $(NH_4)_2S$ solution, the sample was loaded into an ALD tool for deposition of ~6.7 nm Al_2O_3. 70 nm TaN metal layer was deposited by sputtering. The gate electrode was then patterned by EBL using NEB 22 and etched using Cl_2-based plasma. After the remaining Al_2O_3 in the S/D regions was removed by diluted HF, device fabrication was completed. Final structure of a FinFET device with self-aligned Mo contacts is shown in Fig. 5.3(e).

(a) Process flow:

- Self-Aligned Mo Contacts and S/D Formation
  - Mo deposition by sputtering
  - Electron beam lithography
  - Dry etch of Mo
  - Wet etch of n^+ $In_{0.53}Ga_{0.47}As$
- $In_{0.53}Ga_{0.47}As$ Fin Definition
  - Electron beam lithography
  - Dry etch of $In_{0.53}Ga_{0.47}As$ fin
  - Wet etch for damage removal
- Gate Stack Formation
  - Substrate pre-clean
  - Al_2O_3 and TaN deposition
  - Electron beam lithography
  - Dry etch of TaN gate

(b)



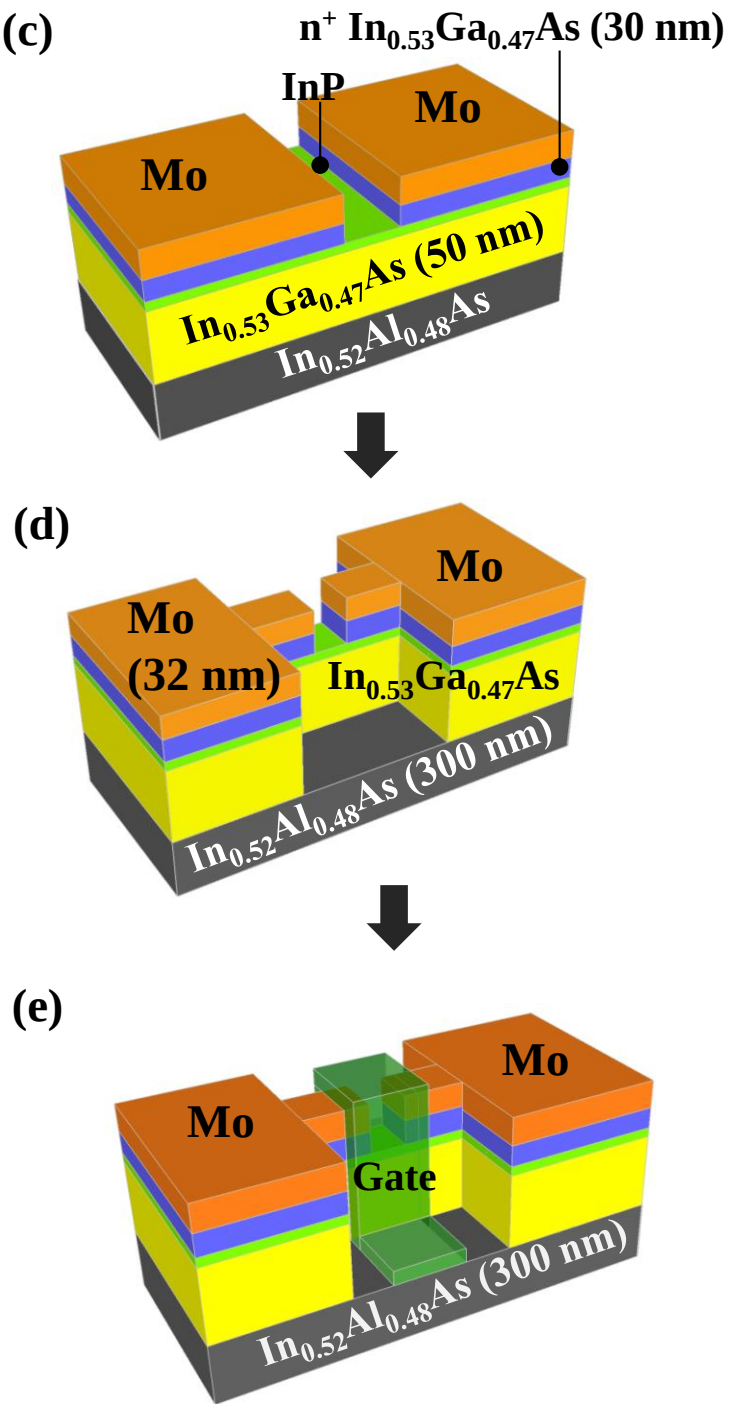


Fig. 5.3. (a) Process flow for fabrication of a novel InGaAs FinFET with Mo contacts self-aligned to channel. The key steps include (b) blanket deposition of Mo, (c) dry etch of Mo and wet etch of n^+ InGaAs, (d) dry etch of InGaAs fin, and (e) gate stack formation.

5.2.3 Device Characterization and Discussion

Scanning Electron Microscopy (SEM) in Fig. 5.4(a) is a zoomed-out view of an InGaAs FinFET. The top view shows the device layout. A zoomed-in view of the channel region shows that the device has 5 fins oriented in the horizontal direction [Fig. 5.4(b)]. The recess of Mo and n^+ InGaAs defines the device channel. Mo contacts were formed on top of n^+ InGaAs in the S/D regions. TaN gate line is oriented in the vertical direction.

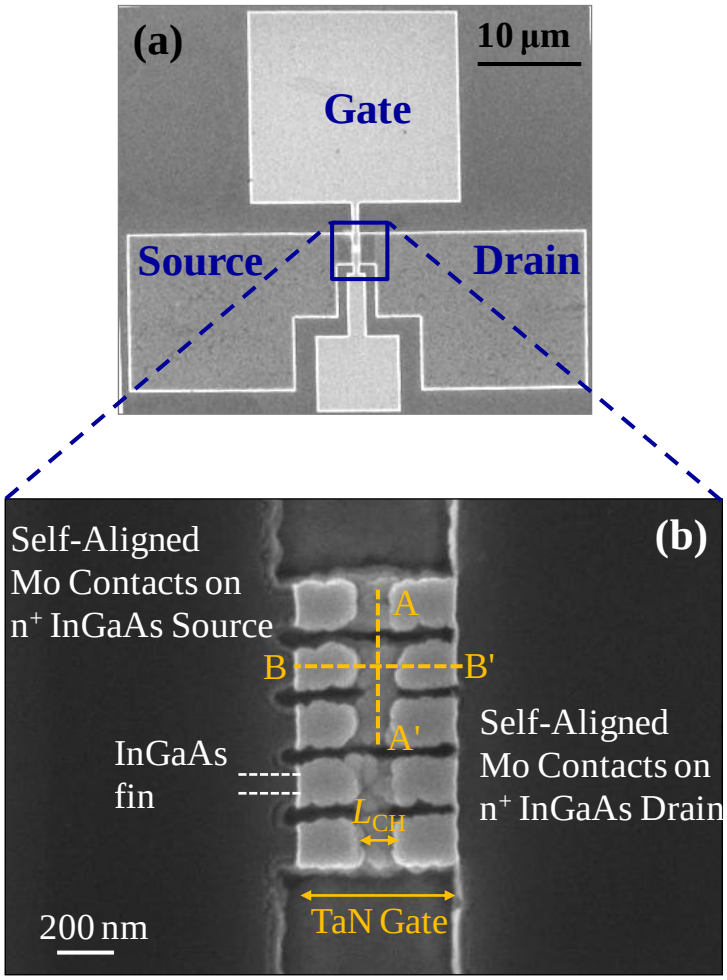


Fig. 5.4. (a) SEM shows layout of an InGaAs FinFET with Mo contacts on n^+ InGaAs S/D. The dimension of S/D big pads is about 15 µm ×15 µm. (b) A zoomed-in view shows the device channel region. The width of recessed n^+ InGaAs defines L_{CH} of the device.

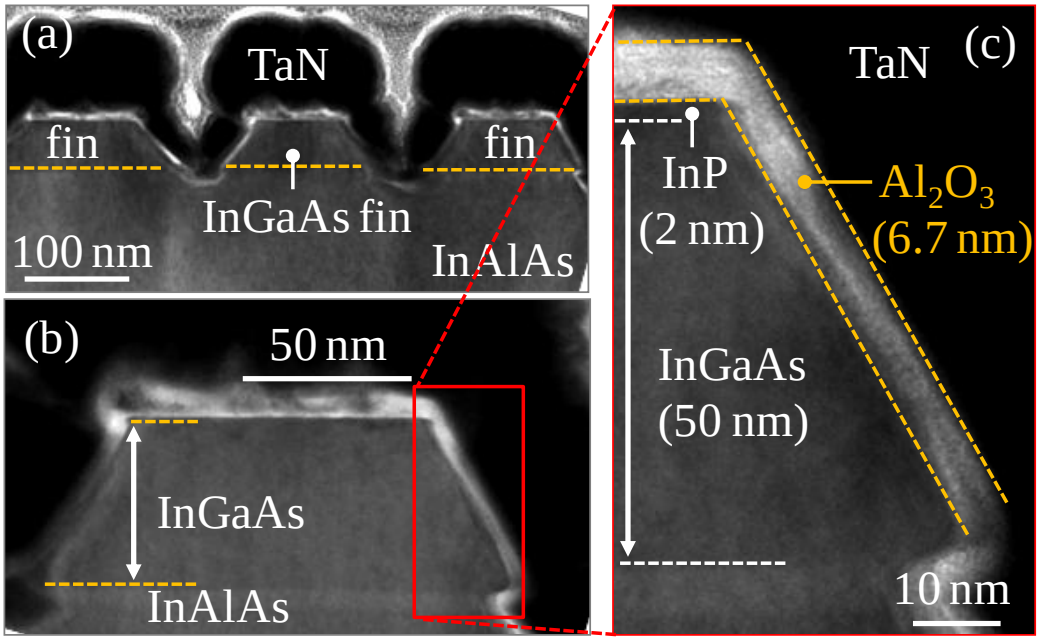


Fig. 5.5. (a) Cross-section of an InGaAs FinFET across the fins [A - A' in Fig. 5.4(b)]. InGaAs fins sitting on InAlAs layer were observed. (b) Zoomed-in view of an InGaAs fin shows the fin structure and dimension. (c) Zoomed-in view of the rectangular region indicates the conformally formed gate stack on the top and sidewalls of the InGaAs fin.

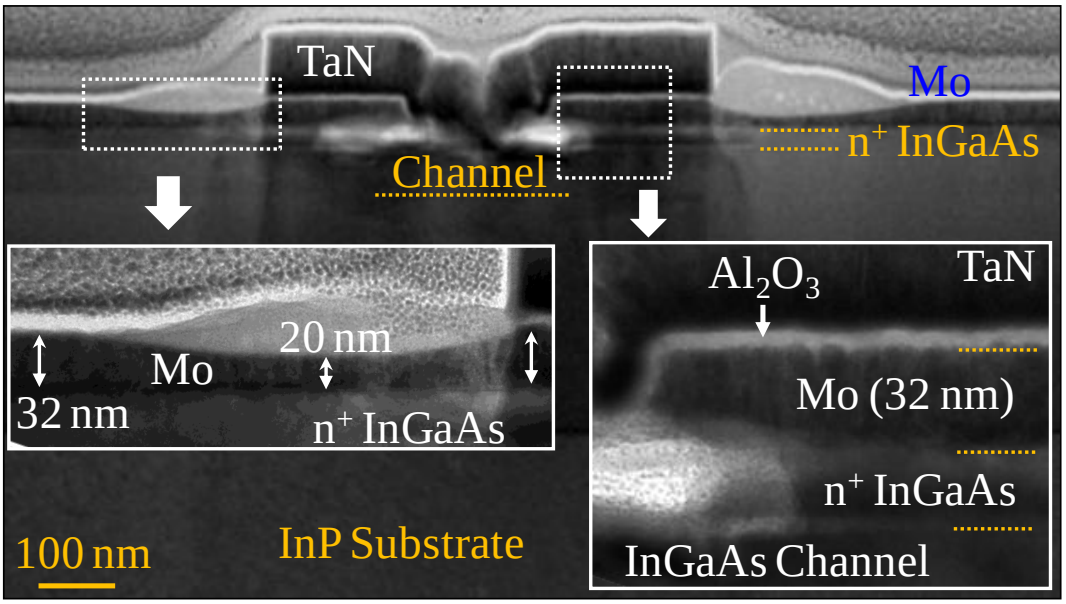
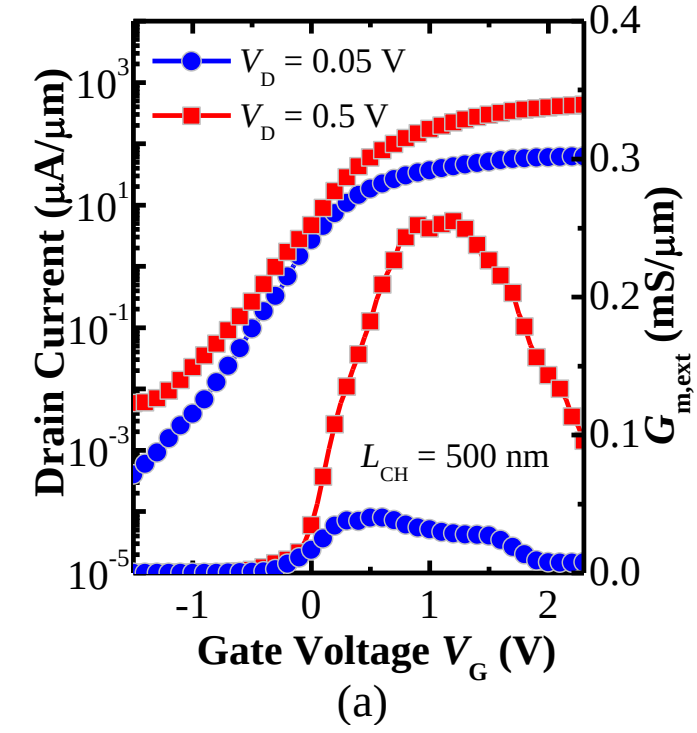


Fig. 5.6. TEM images show the device cross-section along the fin [B - B' in Fig. 5.4(b)]. Mo contacts were observed on the surface of n^+ InGaAs S/D and aligned to InGaAs channel. The zoomed-in views of the S/D regions are shown by the insets.

TEM image in Fig. 5.5(a) shows a device cross-section along the dashed line A - A' in Fig. 5.4(b). The InGaAs fins are well formed and have top width of ~80 nm, bottom width of ~125 nm, and height of 52 nm [Fig. 5.5(b)]. A zoomed-in view of the rectangular region shows the 2 nm InP capping layer on top of the fin and that TaN/Al_2O_3 was conformally formed on the fin top and sidewalls surfaces [Fig. 5.5(c)]. Fig. 5.6 shows a device cross-section along the dashed line B - B' in Fig. 5.4(b). The Mo contacts appear as a darker layer on top of n^+ InGaAs and are well aligned to the InGaAs channel. Mo layer has a thickness of about 32 nm in the device S/D regions, as shown in Fig. 5.6 (inset). Mo layer thickness is not uniform in the entire S/D regions and slightly recessed near the edge of TaN gate. This is probably caused by the TaN gate etch process using Cl_2-based plasma, since Cl_2 plasma etches Mo in a very fast rate, as documented in Section 5.2.1 of this Chapter.

In Chapter 4 [5.7], Ni-InGaAs contacts to the S/D were formed aligned to the TaN gate electrode and there is a separation between the channel and S/D Ni-InGaAs contacts due to the gate-to-S/D overlap. The InGaAs channel and S/D Ni-InGaAs contacts were connected by an n^+ InGaAs capping layer with thickness of 30 nm and sheet resistance of ~55 Ω/square. This n^+ InGaAs capping layer contributes $2R_{cap}$ = 68 Ω·μm to R_{SD} [5.7]. The non-alloyed Mo contacts were formed aligned to the InGaAs channel in this Chapter, and thus help reduce the resistance resulting from n^+ InGaAs capping. The zoomed-in view of the S/D regions in Fig. 5.6 (inset) confirms the good alignment of Mo contacts to the InGaAs channel.

Fig. 5.7(a) shows drain current versus gate voltage (I_D-V_G) and extrinsic transconductance versus gate voltage ($G_{m,ext}$ - V_G) of a single-fin InGaAs FinFET with



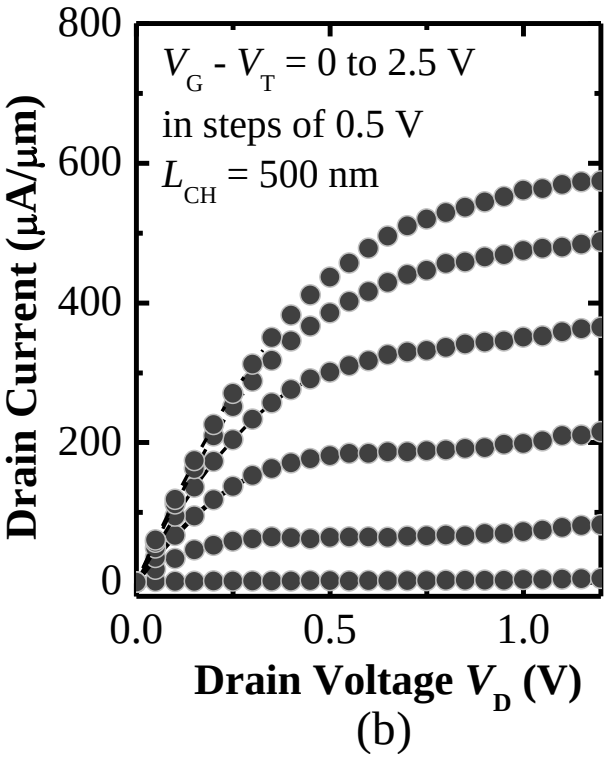


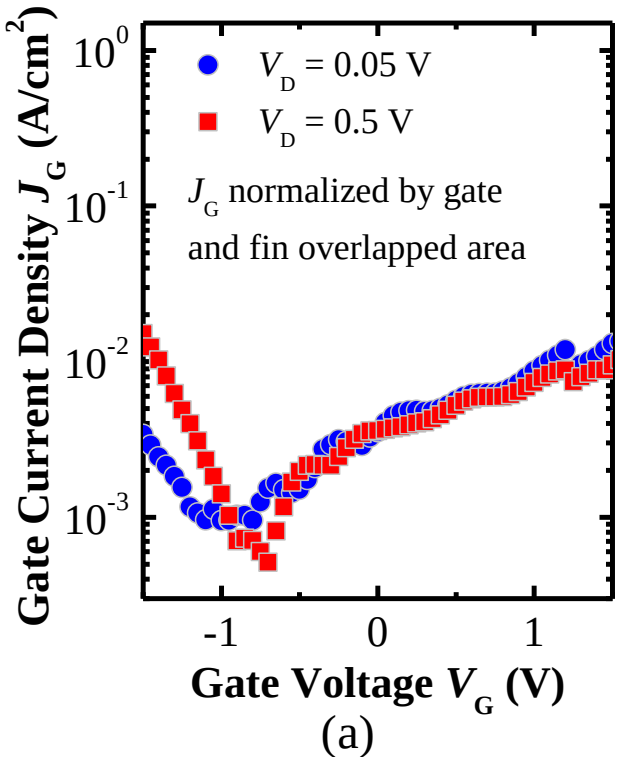
Fig. 5.7. (a) I_D–V_G and $G_{m,ext}$–V_G of a single-fin InGaAs FinFET with L_{CH} = 500 nm and W_{fin} = 90 nm, showing I_{ON}/I_{OFF} of over 10^5. Drain voltage V_D of 0.05 and 0.5 V were applied. (b) I_D–V_D characteristics of the same device showing good saturation and pinch-off characteristics.

channel length L_{CH} of 500 nm and fin width W_{fin} of 90 nm. The I_D and $G_{m,ext}$ values were normalized by the device effective width W_{eff} which is the sum of top channel W_{top} and two sidewalls channel $2W_{side}$. W_{eff} is about 200 nm, as obtained from the TEM in Fig. 5.5. Good transfer characteristics with on-state/off-state drain current ratio (I_{ON}/I_{OFF}) of over 10^5 were observed. Peak $G_{m,ext}$ of 255 μS/μm was obtained at V_D of 0.5 V and this value is reasonable, considering the large L_{CH} of 500 nm and large EOT of ~3 nm. The device has a subthreshold swing S of 286 mV/decade and drain induced barrier lowering (DIBL) of 77 mV/V. Better S could be achieved by reducing the fin width and EOT. Drain current versus drain voltage (I_D-V_D) [Fig. 5.7(b)] of the same device demonstrates good saturation and pinch-off characteristics. The gate overdrive $V_G - V_T$ was varied from 0 to 2.5 V in steps of 0.5 V. Fig. 5.8(a) shows low gate leakage current density J_G which was normalized by gate and fin overlapped area. Low J_G is expected because of thick gate dielectric Al_2O_3 (~6.7 nm) and the low thermal budget in this gate-last process. There is only one thermal step which is the ALD deposition of Al_2O_3 and HfO_2 at temperature of 250 ℃.

Fig. 5.8(b) plots the peak $G_{m,ext}$ of devices with different L_{CH} at V_D = 0.5 V, showing that reduced transistor L_{CH} improved the device $G_{m,ext}$. Fig. 5.9(a) plots the total resistance R_T in the linear regime (V_D = 0.05 V) as a function of as-printed channel length $L_{As\text{-}printed}$ at three specified gate overdrive $V_G - V_T$ of 1, 1.5, 2 V. The equation for the fitted lines is given by [5.20]

$$R_T = R_{SD} + R_{CH}$$

$$= R_{SD} + (L_{As\text{-}printed} - \Delta L)[W_{eff}\mu_{eff}C_{ox}(V_G - V_T)]^{-1}, \qquad (5.1)$$



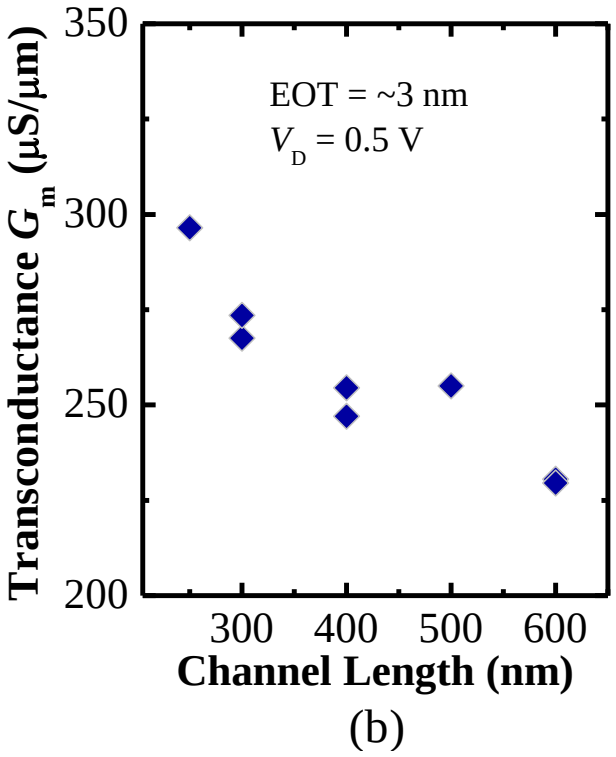
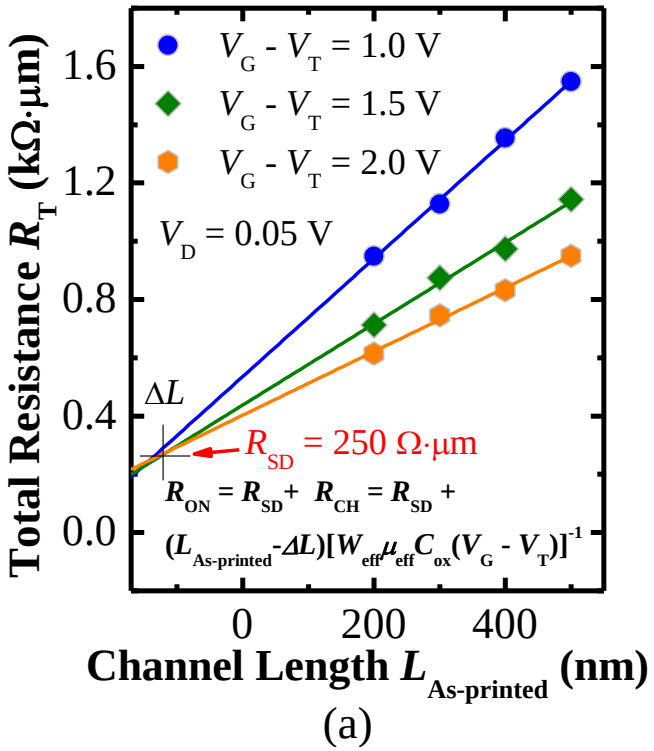
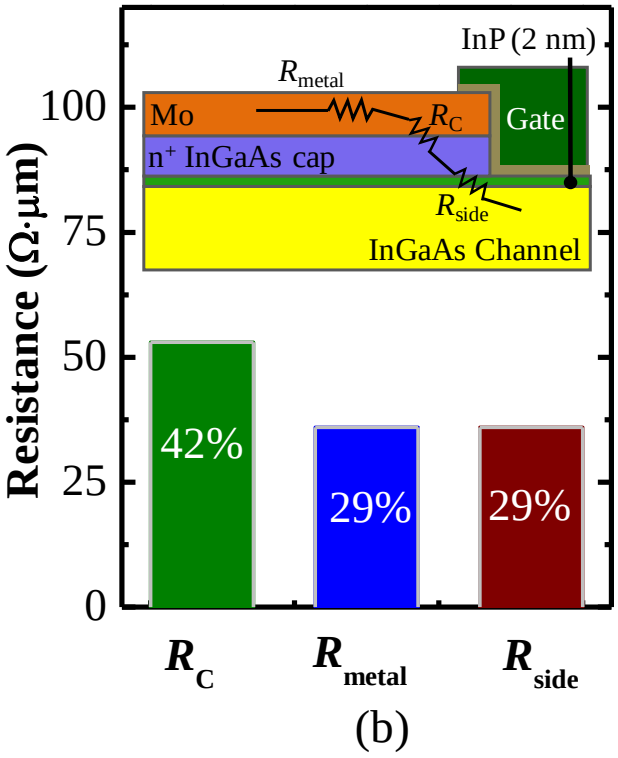


Fig. 5.8. (a) J_G as a function of V_G showing low gate leakage current density below 1×10^{-2} A/cm^2. (b) Peak $G_{m,ext}$ of FinFETs with different L_{CH} (W_{fin} = 90 nm). The applied drain voltage is 0.5 V.



(a)



(b)

Fig. 5.9. (a) R_T–$L_{As\text{-}printed}$ of InGaAs FinFETs. R_T was obtained at a specified V_G-V_T in the linear regime (V_D = 0.05 V). R_{SD} was extracted from the intersection of the fitted lines. (b) The plot indicates the estimated component elements (R_C, R_{metal}, R_{side}) of R_S. The percentages shown are the percentage contributions of the various components to R_S.

and was used to fit the data points (solid symbols). ($L_{\text{As-printed}}$ - ΔL) is device actual channel length L_{CH}, W_{eff} is device effective width, μ_{eff} is channel effective mobility, and C_{ox} is gate dielectric capacitance. The three fitted curves were extrapolated to show an intersection point. The intersection gives the R_{SD} of ~250 Ω·μm which is the lowest value reported-to-date for InGaAs non-planar n-MOSFETs. The intersection also gives a negative value of ΔL = -100 nm, which means the actual L_{CH} is 100 nm larger than $L_{\text{As-printed}}$, as obtained by [5.20]

$$L_{\text{CH}} = L_{\text{As-printed}} - \Delta L. \qquad (5.2)$$

This is also confirmed by cross-sectional TEM. The fact that L_{CH} is larger than $L_{\text{As-printed}}$ is due to the lateral etch in the step of removal of n^+ InGaAs by wet etch, which defines the device channel length L_{CH}. All the L_{CH} values mentioned in this Chapter are the actual L_{CH} after correction and $L_{\text{As-printed}}$ in Fig. 5.9(a) represents the as-printed channel length.

The plot in Fig. 5.9(b) shows the estimated component elements of the source resistance R_{S} ($2R_{\text{S}} = 2R_{\text{D}} = R_{\text{SD}}$). Mo resistance ($R_{\text{metal}}$) is calculated to be about 36 Ω·μm based on the Mo sheet resistance and the device source geometry as shown in Fig. 5.4(a). The sputtered Mo layer has a thickness T_{Mo} of 32 nm and shows high sheet resistance R_{sh} of ~40 Ω/square. Mo resistivity ρ_{Mo} could be obtained by [5.20]

$$\rho_{\text{Mo}} = R_{\text{sh}} \times T_{\text{Mo}}. \qquad (5.3)$$

The calculated resistivity is ρ_{Mo} = ~128 μΩ·cm and is 25 times higher than the reported value of 5~6 μΩ·cm in Ref. [5.21]. This could be due to an un-optimized metal sputtering process [5.22]. R_{C} of Mo contacts is ~24 Ω·μm, as obtained from TLM structures. The contact width W_{C} is equal to fin width $W_{\text{C}} = W_{\text{fin}}$ = 90 nm since

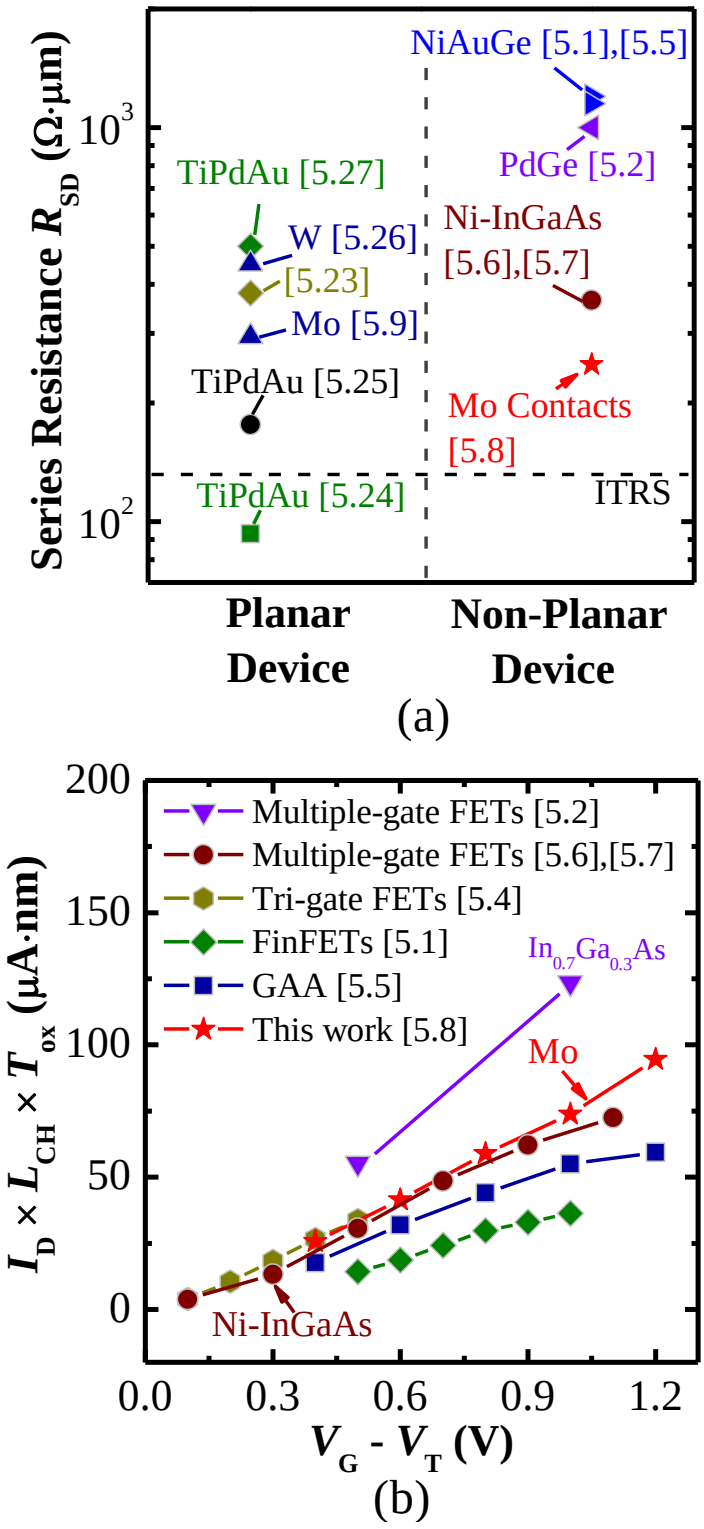


Fig. 5.10. (a) Lowest R_{SD} of 250 Ω·μm is obtained in this Chapter as compared with reported InGaAs non-planar devices with non-self-aligned or self-aligned contacts. (b) Drive current benchmarking by plotting $I_D \times L_{CH} \times T_{ox}$ versus V_G–V_T of InGaAs non-planar n-MOSFETs reported in the literature as well as the devices in this Chapter.

Mo only contacts the top surface of n^+ InGaAs but not the sidewalls of the InGaAs fin. Therefore, the contribution from Mo contact resistance is R_C/W_{fin} = 267 Ω and it is 53 Ω·μm after being normalized to device effective width W_{eff} = ~200 nm. The remaining resistance (denoted as R_{side}) is ~36 Ω·μm, which includes InP barrier resistance and spreading resistance in source. From the calculation, we observe that $R_{metal,}$ and R_{side} are comparable and almost have equal contribution of 29% to the total source resistance R_S. Mo contact resistance contributes ~53 Ω·μm and it takes up 42% of R_S.

Fig. 5.10(a) benchmarks R_{SD} of this work with reported values for InGaAs channel planar and non-planar n-MOSFETs. Low R_{SD} of 364 Ω·μm for InGaAs FinFETs was achieved by using self-aligned Ni-InGaAs S/D contacts in Chapter 4 [5.6],[5.7]. Lowest R_{SD} of ~250 Ω·μm for InGaAs non-planar n-MOSFETs was achieved in this Chapter, with contribution from self-alignment of the Mo contact to InGaAs channel and low R_C of Mo on *in-situ* doped n^+ InGaAs S/D. Further reduction of R_{SD} is possible by optimizing the device structure and fabrication process. To benchmark the drive current performance of the devices in this Chapter with reported InGaAs non-planar n-MOSFETs, $I_D \times L_{CH} \times T_{ox}$ as a function of overdrive $V_G - V_T$ is plotted in Fig. 5.10(b). T_{ox} is equivalent oxide thickness. Drive current performance of the FinFETs in this Chapter is comparable to that of the best reported non-planar n-MOSFETs with $In_{0.53}Ga_{0.47}As$ channel.

5.3 InGaAs FinFETs with FGA Improved HfO_2/Al_2O_3 Dielectric

5.3.1 Integration of InGaAs FinFETs with HfO_2/Al_2O_3 Dielectric

The InGaAs FinFET fabrication process is similar as that discussed in Section 5.2.2 of this Chapter and summarized in Fig. 5.11(a). Mo contacted S/D and InGaAs fin were formed before gate stack formation [Fig. 5.11(b)-(d)]. Then, pre-gate cleaning was performed and the samples were loaded into an ALD tool for HfO_2/ Al_2O_3 deposition. 3 cycles of Al_2O_3 deposition (growth rate: 1.16 Å/cycle) and 40 cycles of HfO_2 deposition (growth rate: 1.0 Å/cycle) were sequentially done at 250 ℃ using Trimethylaluminum (TMA) and Tetrakis Diethylamido Hafnium (TDEAH) as precursors, respectively. The physical thickness of HfO_2/Al_2O_3 is about 4.4 nm, which was obtained by an ellipsometer. Tungsten Nitride (WN) metal layer (~60 nm) was deposited by sputtering, patterned by EBL and etched by CF_4-based plasma [Fig. 5.11(e)]. After WN etch, photoresist was stripped by oxygen plasma and the remaining HfO_2/Al_2O_3 in the S/D regions was removed by dilute HF.

At this stage, the fabrication for control devices (without FGA) was completed and these devices could be measured. The final structure of the device is shown in Fig. 5.11(e) with $WN/HfO_2/Al_2O_3$ gate stack and self-aligned Mo S/D contacts. A 30-minute FGA with Hydrogen (H_2) and Nitrogen (N_2) flow rate ratio of H_2: N_2 = 1: 9 was performed at 300 ℃ for the other batch of devices using a furnace tube. Capacitors on lightly p-doped (2×10^{16} cm^{-3}) Si with exactly the same gate stack as FinFET devices were also fabricated for extraction of EOT of the gate dielectric.

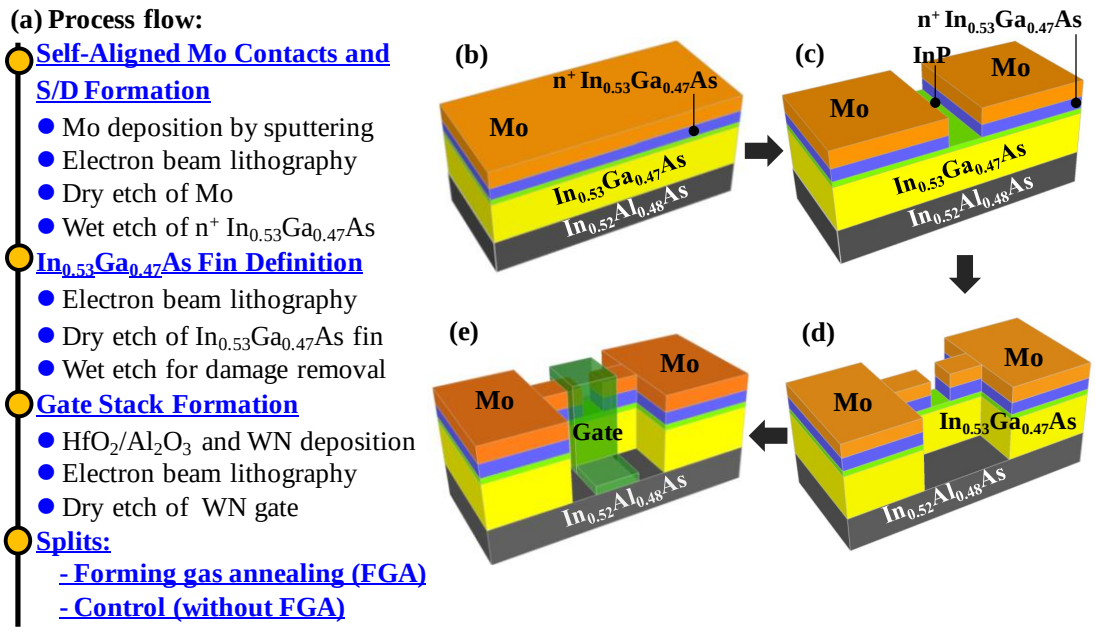


Fig. 5.11. (a) Process flow for fabrication of InGaAs FinFETs with HfO_2/Al_2O_3 high-*k* stack and self-aligned Mo contacts. The process involves (b) Mo deposition, (c) self-aligned Mo-contacted S/D formation, (d) fin formation, (e) gate stack ($WN/HfO_2/Al_2O_3$) formation. There are 2 splits after the gate stack formation. One batch of devices went through FGA while the other batch of devices skipped FGA.

5.3.2 Device Characterization and Discussion

Si capacitor was measured and the accumulation capacitance density versus gate voltage was illustrated in the inset of Fig. 5.12(a). Measured data points are plotted in circles and fitted using simulated *C-V* curve (blue line) with quantum mechanical effects taken into account. The extracted EOT is ~1 nm. This EOT extracted from Si capacitors may be slightly different from that of InGaAs FinFET devices due to a difference in the high-*k*/substrate interfacial layer.

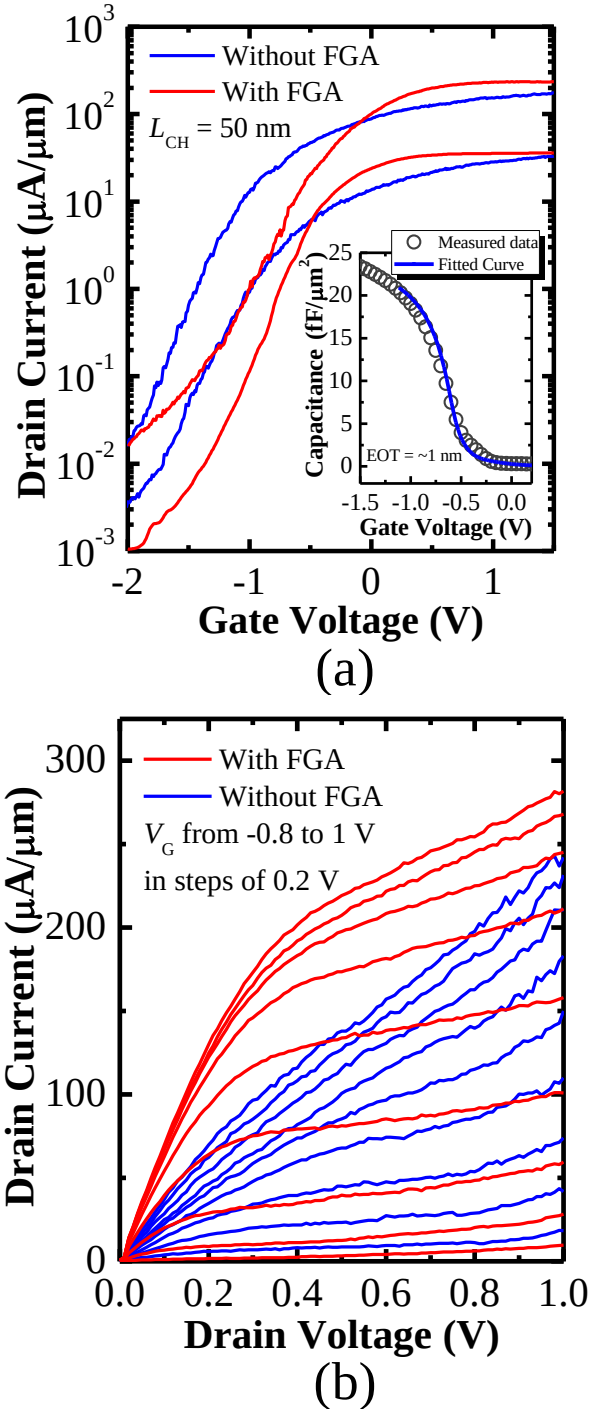


Fig. 5.12. (a) Capacitance density versus gate voltage measured from a Si capacitor was illustrated in the inset, indicating ~1 nm EOT of the high-*k* dielectric. I_D–V_G curves of InGaAs FinFET devices (with and without FGA) with L_{CH} of 50 nm and fin width of ~80 nm, showing good transfer characteristics. (b) I_D –V_D curves of the same pair of devices show good saturation and pinch-off characteristics. FGA device shows significant enhancement of drive current as compared with control device.

Both control (without FGA) and FGA FinFET devices were electrically characterized. I_D-V_G and I_D–V_D curves in Fig. 5.12(a) and (b) compares the electrical characteristics of a FGA device with a control device. Both devices have channel length L_{CH} of 50 nm and fin width W_{fin} of ~80 nm. In Fig 5.12(a), drain voltages V_D of 0.05 V and 0.5 V were applied. Both devices exhibit good transfer characteristics with on-state/off-state drain current ratio of over 10^4. A maximum transconductance method was used to extract the device threshold voltage V_T in the linear regime (V_D = 0.05 V). V_T of a long channel transistor could be written as [5.28]:

$$V_T = V_{FB} + \phi_s + \frac{\sqrt{2qN_A\varepsilon_s\phi_s}}{C_{ox}}$$

$$= \Phi_{MS} - \frac{Q_f}{C_{ox}} + \phi_s + \frac{\sqrt{2qN_A\varepsilon_s\phi_s}}{C_{ox}}, \qquad (5.4)$$

where V_{FB} is flat band voltage, ϕ_s is channel surface potential, q is electronic charge, N_A is substrate doping, ε_s is the permittivity of semiconductor, C_{ox} is gate oxide capacitance, Q_f is fixed oxide charge density in dielectric, and Φ_{MS} is the work function difference between metal and semiconductor. The V_T for control and FGA devices shown in Fig. 5.12(a) is -0.8 V and -0.52 V, respectively. The apparent positive shift of V_T after FGA indicates the presence of positive fixed charges within as-deposited HfO_2/Al_2O_3 dielectric film. Those charges were significantly reduced after FGA at 300 ℃ for 30 minutes, leading to positive V_T shift of 0.28 V [Fig. 5.12(a)]. An average V_T shift of 0.24 V was also observed for the batch of devices with FGA as compared with the batch of devices without FGA, as illustrated in Fig 5.13(a). It has been reported that the observed fixed charges in Al_2O_3 is due to Al and O dangling bonds in the film and the hydrogen (H) from FGA can passivate those

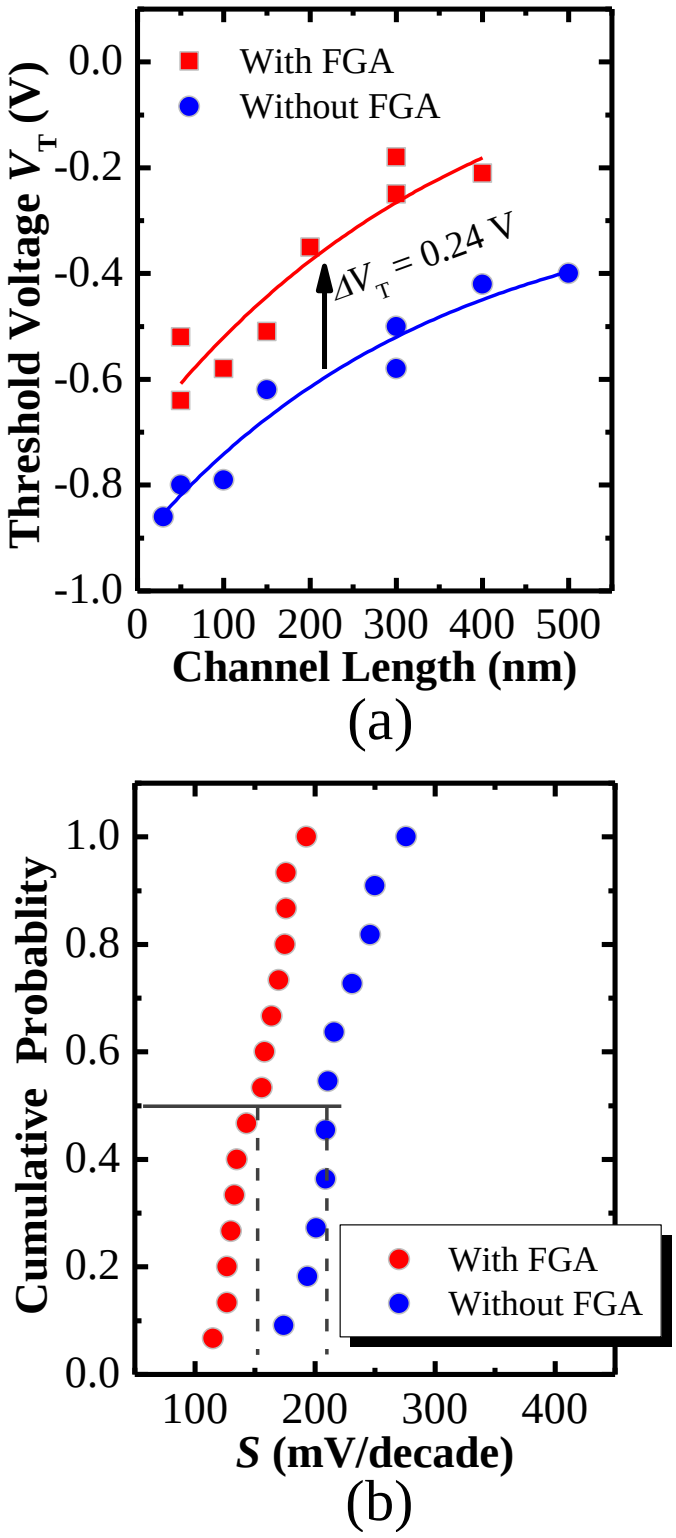


Fig. 5.13. (a) V_T versus L_{CH}, showing an average V_T shift of ~0.24 V after FGA. V_T roll-off is also observed for both bathes of devices. (b) Cumulative plot shows the distribution of S, indicating large improvement of S by FGA.

dangling bonds by forming Al-H and O-H bonds [5.16]. The fixed charges in HfO_2 were also observed and may also similarly come from oxygen vacancies as reported in Ref. [5.14]. The reduction of fixed charges in this Chapter is attributed to passivation of dangling bonds in as-deposited Al_2O_3 and HfO_2 layers by hydrogen during the FGA.

Large improvement of the subthreshold swing *S* was obtained by FGA. In Fig 5.12(a), *S* of the device is reduced from 300 mV/decade to 176 mV/decade after FGA. The distribution plot of *S* in Fig. 5.13(b) also shows an obvious improvement of the average *S* from 210 mV/decade to 150 mV/decade, indicating better interface quality due to FGA. It has been reported that FGA could help passivate the interface trap of $Al_2O_3/In_{0.53}Ga_{0.47}As$ and thus reduce interface trap density [5.18],[5.19]. Drain current enhancement was also observed for devices with FGA. In Fig. 5.12(b), drain current of the device increases from 241 μA/μm to 281 μA/μm at $V_D = V_G = 1$ V after FGA. I_D as a function of L_{CH} of the two batches of devices is plotted in Fig. 5.14(a), with L_{CH} varying from 30 to 400 nm. I_D is defined at V_G-V_T = 1 V and V_D = 0.5 V. An average enhancement of 48% is observed for the batch of devices with FGA [5.14(a)]. We believe the drive current enhancement is due to enhanced channel electron mobility by reducing the interface scattering, since FGA reduces the interface trap density [5.18],[5.19].

Fig. 5.14(b) plots J_G-V_G of the devices with and without FGA, showing that FGA at 300 ℃ did not increase the gate dielectric leakage current density. J_G is in the level of 1×10^{-3} A/cm^2. Device R_{SD} was extracted from the plot of the R_T versus V_G in the linear regime (V_D = 0.05 V). Equation (5.1) is used to fit the measured data

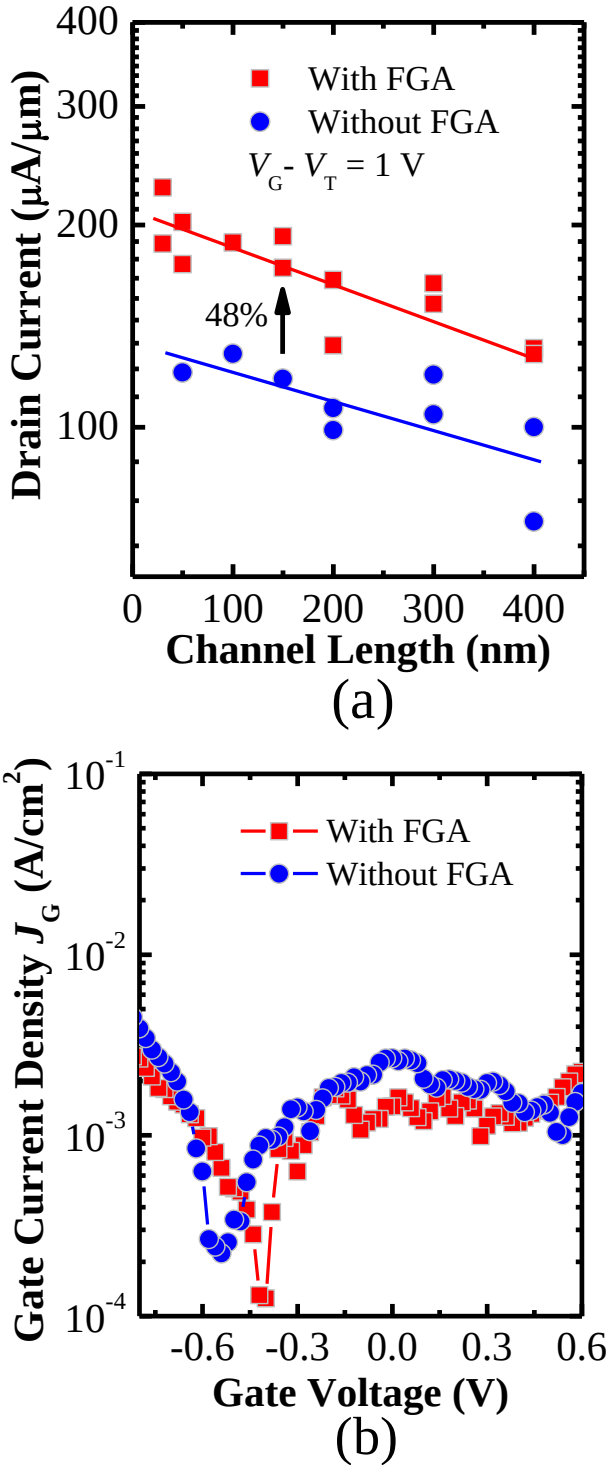


Fig. 5.14. (a) Drain current, which was defined at $V_G - V_T = 1$ V and $V_D = 0.5$ V, is plotted as a function of L_{CH}. Devices with FGA show about 48% enhancement of the drive current as compared with the devices without FGA. (b) J_G-V_G of the devices with and without FGA, showing comparable low gate leakage current density. Gate leakage current was normalized by the overlapped area of gate and fins.

points and extrapolated to a large V_G to obtain the value of R_{SD}. R_{SD} as low as ~240 Ω·μm was obtained for control devices, as shown in Fig. 5.15. However, the degradation of R_{SD} for FGA devices was observed. The FGA devices show obvious increased R_{SD} of over 1000 Ω·μm. One possible explanation is that FGA (300 ℃ for 30 minutes) degrades Mo contacts on n^+ InGaAs and leads to a higher R_C. Another possibility is that Mo/InGaAs interface was oxidized when the wafer was unloaded and exposed to air at temperature of 300 ℃. Further experiment is needed to investigate this.

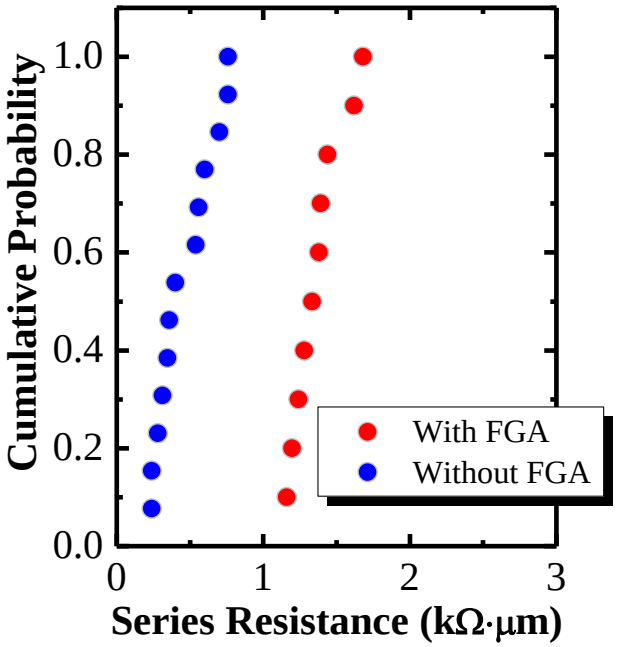


Fig. 5.15. Statistical plot shows that R_{SD} increased after FGA. This is probably due to the degradation of Mo contacts by FGA, leading to a higher R_C.

5.4 Summary

InGaAs FinFETs with Mo contacts self-aligned to channel were realized using a gate-last fabrication process (Section 5.2). Electrical properties of Mo contacts on n^+ InGaAs were studied. The InGaAs FinFET with self-aligned Mo contacts demonstrates good transfer characteristics with high I_{ON}/I_{OFF} ratio of 10^5 and good performance. The devices show low R_{SD} of 250 Ω·μm due to the self-alignment of Mo contacts as well as its low contact resistance. Dual high-*k* dielectric HfO_2/Al_2O_3 was integrated in InGaAs FinFETs and small EOT of ~1 nm was achieved (Section 5.3). FGA at 300 ℃ was performed to improve HfO_2/Al_2O_3 dielectric and leads to significant improvement drive current and subthreshold swing *S*.

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Chapter 6

Conclusion and Future Work

6.1 Conclusion

Geometrical scaling of conventional silicon (Si) transistors is reaching its fundamental limits after four decades of device scaling. New channel materials such as III-V compound semiconductors and new device structures such as FinFETs are needed to sustain the equivalent scaling of transistors. Among several technical challenges faced by advanced III-V MOSFETs, reduction of parasitic resistance is one of the most important.

It is the objective of this thesis to explore new contact technologies to address the source/drain (S/D) resistance issue in nanoscale III-V n-MOSFETs. Various process technologies coupled with new materials have been proposed and experimentally realized in this thesis. In particular, this thesis introduces a few self-aligned metallization technologies to enable the reduction of S/D series resistance for GaAs and InGaAs transistors. This will ultimately result in enhanced device performance. The seminal contributions of this thesis are listed in next Section.

6.2 Contributions of This Thesis

6.2.1 Self-Aligned NiGeSi Metallization for GaAs Planar n-MOSFETs

NiGeSi contact was developed for GaAs transistors using a self-aligned metallization [6.1]-[6.4]. The metallization process, comprising a selective epitaxy of GeSi film on n^+ GaAs and a two-step anneal process, is a "salicide-like" process and is compatible with GaAs transistors fabrication. The demonstrated GaAs transistors with self-aligned NiGeSi contacts show good transfer and output characteristics.

6.2.2 Self-Aligned Ni-InGaAs Contacts for InGaAs Planar n-MOSFETs

A self-aligned Ni-InGaAs contact technology suitable for InGaAs n-MOSFETs was developed [6.5]-[6.9]. Ni-InGaAs contact was formed at low temperature of 250 ℃. Its physical and electrical properties were comprehensively studied, and promising results were shown. This self-aligned Ni-InGaAs contact technology was used in the integration of InGaAs planar n-MOSFETs and good electrical characteristics were achieved.

6.2.3 InGaAs FinFETs with Self-Aligned Ni-InGaAs Contacts

A gate-last process for fabricating InGaAs FinFETs was introduced, with the successful incorporation of selective wet etch of n^+ InGaAs, plasma etch of InGaAs fin, and self-aligned Ni-InGaAs metallization. InGaAs FinFETs with self-aligned Ni-InGaAs contacts formed on *in-situ* doped n^+ InGaAs source/drain were demonstrated [6.10],[6.11]. The devices exhibit low series resistance of 364 Ω·μm, due to the self-

alignment of Ni-InGaAs contacts and the low contact resistance of Ni-InGaAs. Good drive current performance was also achieved.

6.2.4 InGaAs FinFETs with Self-Aligned Non-Alloyed Mo Contacts

InGaAs FinFETs with Mo contacts self-aligned to channel were realized using a well designed gate-last fabrication process [6.12]. Electrical properties of Mo contacts on n^+ InGaAs were studied. The InGaAs FinFETs with self-aligned Mo contacts demonstrate good transfer characteristics with high on-state/off-state drive current ratio of 10^5 and good drive current performance. The devices show low series resistance of ~250 Ω·μm due to the self-aligned Mo contacts as well as the low contact resistance of Mo.

6.2.5 InGaAs FinFETs with Forming Gas Annealing (FGA) Improved HfO_2/Al_2O_3

Dual high-*k* dielectric HfO_2/Al_2O_3 which benefits from the good interface quality of Al_2O_3 and high dielectric constant of HfO_2 was integrated in InGaAs FinFETs. Small EOT of ~1 nm was achieved. Forming gas annealing at 300 ℃ was performed to further improve HfO_2/Al_2O_3 dielectric quality and to improve device drive current and subthreshold swing *S*.

6.3 Future Directions

In summary, this thesis focuses on developing solutions to address the source/drain resistance issue, which is one of key technical challenges of III-V MOSFETs for advanced CMOS logic applications. This thesis has conceptualized and embarked on the development of several contact technology options to realize low-resistance, self-aligned contacts for III-V n-MOSFETs and improve the transistor drive current performance.

The silicide-like NiGeSi contact technology developed for GaAs transistors in Chapter 2 is robust and results in good yield of devices. However, this technology involves GeSi epitaxy process which has very high thermal budget. This makes this technology complicated, costly, and also less suitable for a gate-first fabrication process, since high thermal budget is easy to degrade the III-V gate stack. Some devices with high gate leakage current were observed due to the high thermal budget, which compromises the yield of devices.

The Ni-InGaAs contact technology developed in Chapter 3 and 4 simplifies the metallization process. With the simplified integration process, the cost and thermal budget is well controlled, leading to improved yield. This technology is very promising for future application and companies such as IBM are working on it. The problem for Ni-InGaAs is that obtained specific contact resistivity is still high and in the level of $1\times10^{-6}\ \Omega\cdot cm^2$, even with the benefit of high doping concentration using *in-situ* doping technology. The specific contact resistivity in the state-of-the-art Si technology has been pushed down to the level of $1\times10^{-8}\ \Omega\cdot cm^2$ and therefore further reduction of the specific contact resistivity is strongly desired for this technology.

The technology we developed in Chapter 5 is a simple non-alloyed Mo contact technology which does not require any thermal anneal step. Mo contact shows promising specific contact resistivity in the level of 1×10^{-7} $\Omega\cdot cm^2$ in this thesis and U. Singisetti *et al* [6.13] even reported Mo shows specific contact resistivity of $\sim1.3\times10^{-8}$ $\Omega\cdot cm^2$. In addition, Mo contact is CMOS compatible and also thermal stable on InGaAs up to ~ 600 ˚C [6.13], which means the Mo contact can withstand the subsequent thermal steps in the backend processing. The simple process and also excellent electrical properties make Mo contact technology very promising for application in III-V transistors.

Preliminary assessment has been verified that these contact technologies are very promising for adoption in future technology nodes. Nevertheless, several issues have been opened up in this thesis and deserve further investigation. Some of the suggestions for future directions in the field of III-V MOSFETs are highlighted in this Section.

6.3.1 Contact Resistance Reduction

Chapter 2, 3, and 4 developed self-aligned NiGeSi and Ni-InGaAs contacts for GaAs and InGaAs transistors, showing promising results. However, the contact resistance of NiGeSi and Ni-InGaAs is not low enough and thus it contributes a significant portion to the device series resistance. Further reduction of contact resistance is desired by increasing substrate doping or by employing new contact materials.

6.3.2 Thermal Stability of Contacts

Ni-InGaAs contact is not thermally stable when process temperature is above 400 ℃. Further work can focus on improving the thermal stability of Ni-InGaAs. Chapter 5 also reveals that Mo contact might be degraded after forming gas annealing at 300 ℃ for 30 minutes. Further work could be carried out to study the FGA effect on Mo contact as well as the thermal stability of Mo contact.

6.3.3 Reliability Study for III-V MOSFETs

In this work, reliability or lifetime study has not performed for III-V transistors. Further work can focus on studying the reliability of III-V transistors with high-*k*/metal gate and various self-aligned contacts.

6.3.4 Self-Aligned Contacts for III-V p-MOSFETs

Due to the attractive electron mobility, existing development of self-aligned contact technology are mainly focused on n-channel MOSFETs. Further work can focus on exploring self-aligned contacts for III-V p-channel devices such as GaSb and InGaSb p-MOSFETs.

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Appendix

List of Publications

Journal Publications

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[6] **X. Zhang**, H. X. Guo, Z. Zhu, X. Gong, and Y.-C. Yeo, "$In_{0.53}Ga_{0.47}As$ FinFETs with self-aligned molybdenum contacts and HfO_2/Al_2O_3 gate dielectric," *Solid-State Electronics*, 2013 (to appear).

Conference Publications

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