ULTRAFAST PHASE-CHANGE FOR DATA STORAGE APPLICATIONS

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ULTRAFAST PHASE-CHANGE FOR DATA STORAGE APPLICATIONS

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Dedicated to my dearest

Mum & Dad

May all who seek and persevere,

Succeed in his/her endeavors

DECLARATION

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Loke Kok Leong Desmond

5th February 2013

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c	Specific heat capacity
d_s	Diameter of small active device region
d_l	Diameter of large active device region
j	Heat flow
k	Thermal conductivity
k_B	Boltzmann constant
m	Fragility
n	Number of interfaces
t	Time
t_o	Onset time of crystallization
t_{GST}	Pulse width of the cells with GST
t_{SLL}	Pulse width of the cells with SLL structures
u	Speed of crystal growth
r	Radius
x	Material size
A	Surface of nucleus
B	Bandwidth
C	System memory capacity
D	Atomic mobility/ diffusion coefficient
E_{as}	Activation energy barriers of phase-change material in small device region
E_{al}	Activation energy barriers of phase-change material in large device region
G_v	Difference in G between two phases per unit volume
I_{ss}	Steady-state nucleation rate
N_e	Cycle endurance
N_g	Fraction of exterior grain
N_l	Crystallization rates of phase-change material in large device region
N_s	Crystallization rates of phase-change material in small device region
T	Absolute temperature
T_g	Glass-transition temperature
T_l	Liquidus temperature
T_{life}	Life span

T_C	Temperature at cold end
T_H	Temperature at hot end
Q	Joule heat per unit volume
V	Volume of nucleus
V_{th}	Threshold voltage
AFM	Atomic force microscope/microscopy
AIMD	Ab initio molecular dynamics
CD	Compact disk
CI	Cell interface
CPU	Central processing unit
CMOS	Complementary metal-oxide-semiconductor
CRAM	Chalcogenide random access memory
DVD	Digital versatile disk
DRAM	Dynamic random access memory
EDS	Energy dispersion spectroscopy
EDX	Energy dispersive x-ray spectrometry
FHWM	Full width half maximum
FinFET	Fin-shaped field-effect transistor
GI	Grain interface
GST	Germanium antimony tellurium
HDD	Hard disk drive
L1	Level 1
L2	Level 2
L3	Level 3
MP3	MPEG-1 audio layer 3
MLC	Multi-level cell
NVM	Nonvolatile memory
NGST	Nitrogen-doped germanium antimony tellurium
OUM	Ovonic unified memory
PT	Peak temperature
PC	Phase-change
PCM	Phase-change memory
PRAM	Phase-change random access memory

PCRAM	Phase-change random access memory
RAM	Random access memory
SLC	Single-layer cell
SLL	Superlattice-like
SSD	Solid-state drive
SILC	Stress-induced leakage current
SIMS	Secondary ion mass spectrometry
SRAM	Static random access memory
SONOS	Silicon-oxide-nitride-oxide-semiconductor
TEM	Transmission electron microscopy
TANOS	Tantalum nitride-alumina-nitride-oxide-semiconductor
USB	Universal serial bus
XPS	X-ray photoelectron spectroscopy
α	Wear-leveling efficiency/ amorphous
σ	Interfacial energy per unit surface area/ interface conductance
η	Liquid viscosity
ρ	Density
θ	Wetting angle
Δ	Change operator
∇	Gradient operator

CITATIONS TO PUBLISHED WORK

Journal Publications

1. D. Loke & T. H. Lee, W. J. Wang, L. P. Shi, R. Zhao, Y. C. Yeo, T. C. Chong, and S. R. Elliott, "Breaking the Speed Limits of Phase-Change Memory," *Science* **336***,* 1566 (2012).

2. W. J. Wang & D. Loke, L. P. Shi, R. Zhao, H. X. Yang, L. T. Law, L. T. Ng, K. G. Lim, Y. C. Yeo, T. C. Chong, and A. L. Lacaita, "Enabling Universal Memory by Overcoming the Contradictory Speed and Stability Nature of Phase-Change Materials," *Nature Scientific Reports* **2**, 360 (2012).

3. D. Loke, L. P. Shi, W. J. Wang, R. Zhao, H. X. Yang, L. T. Ng, K. G. Lim, T. C. Chong, and Y. C. Yeo. "Ultrafast Switching in Nanoscale Phase-Change Random Access Memory with Superlattice-like Structures," *Nanotechnology* **22**, 254019 (2011). (*Invited Paper)

4. D. Loke, L. P. Shi, W. J. Wang, R. Zhao, L. T. Ng, K. G. Lim, H. X. Yang, T. C. Chong, and Y. C. Yeo, "Superlattice-like Dielectric as a Thermal Insulator for Phase-Change Random Access Memory," *Applied Physics Letters* **97**, 243508 (2010).

5. W. J. Wang, L. Shi, R. Zhao, D. Loke, H. X. Yang, K. G. Lim, H. K. Lee, and T. C. Chong. "Nanoscaling of Phase Change Memory Cells for High Speed Memory Applications," *Japanese Journal of Applied Physics* **48**, 04C060 (2009).

Conference Publications

1. W. J. Wang & D. Loke, L. T. Law, L. P. Shi, R. Zhao, M. H. Li, L. L. Chen, H. X. Yang, Y. C. Yeo, A. O. Adeyeye, T. C. Chong, and A. L. Lacaita, "Engineering Grains of $Ge_2Sb_2Te_5$ for Realizing Fast-Speed, Low-Power, and Low-Drift Phase-Change Memories with Further Multilevel Capabilities," *IEEE International Electron Device Meeting,* San Francisco, CA USA, December 10-12 (2012).

2. S. R. Elliott, D. Loke, and T. H. Lee, “A Strategy to Achieve Sub-nanosecond Write Speeds: Ab initio Molecular-dynamics Simulations of Nucleation in GST,” *Materials Research Society Spring Meeting*, San Francisco, CA USA, April 9-12 (2012). (*Invited Paper)

3. J. M. Skelton, D. Loke, T. H. Lee, S. R. Elliott, “Ab initio Molecular Dynamics Simulation of Multilevel Crystallisation in $Ge_2Sb_2Te_5$, *Materials Research Society Spring Meeting*, San Francisco, CA USA, April 9-12 (2012).

4. D. Loke, L. P. Shi, W. J. Wang, R. Zhao, L. T. Ng, K. G. Lim, H. X. Yang, T. C. Chong, and Y. C. Yeo, "Nano Superlattice-like Materials as Thermal Insulators for Phase-Change Random Access Memory," *Materials Research Society Fall Meeting,* Boston, MA USA, Nov. 28-Dec. 2 (2012), pp. 1404.

5. J. M. Skelton, T. H. Lee, D. Loke, and S. R. Elliott, “Ab Initio Molecular Dynamics Study of Phase Change Materials,” *10th International Conference on Materials Chemistry*, Manchester, UK, July 4-7 (2011).

6. L. P. Shi, R. Zhao, D. Loke, W. J. Wang, J. M. Li, H. X. Yang, H. K. Lee and Y. C. Yeo. "Investigation on Scaling Limitation of Phase Change Random Access Memory," *Materials Research Society Spring Meeting*, San Francisco, CA USA, April 25-28 (2011). (*Invited Paper)

7. D. Loke, W. J. Wang, L. Shi, R. Zhao, H. X. Yang, K. G. Lim, L. T. Ng, H. K. Lee, Y. C. Yeo, and T. C. Chong. "Perspectives of Nanostructured Phase-Change Materials for High Speed Non-Volatile Memory," *Materials Research Society Spring Meeting*, San Francisco, CA USA, April 5-9 (2010).

8. D. Loke, W. J. Wang, L. Shi, R. Zhao, H. X. Yang, K. G. Lim, L. T. Ng, H. K. Lee, Y. C. Yeo, and T. C. Chong. "Ultrafast Phase-Change RAM and Correlation between Phase-Change Speed and Cell Size," *4th MRS-S Conference on Advanced Materials*, Singapore, March 17-19 (2010).

Patents

1. D. Loke, H. X. Yang, R. Zhao, and W. J. Wang, "Superlattice-like Dielectric as a Thermal Insulator in Lateral-type Phase-Change Random Access Memory," (filed in 2011).
2. W. J. Wang, R. Zhao, D. Loke, L. P. Shi, and M. H. Li, "Methodology for PCRAM Initialization, Erase and Multilevel Programming," (filed in 2010).

Chapter 1

Introduction

1.1 Motivation for New Nonvolatile Memory

Nonvolatile memories (NVM) are used in our everyday lives for a wide range of applications, such as to store music on MP3 players, photos on digital cameras, text messages on mobile phones, and documents on USB thumb drives. This has been made possible with Flash memory like NOR and NAND Flash. Flash memory has grown in less than three decades to become a $20 billion-dollar-per-year titan in the semiconductor industry [1.1]. This has been made possible by the tremendous increase in the system functionality that can be delivered in the same package size for early portable devices.

The Flash memory market has grown rapidly due to the relentless scaling of devices as predicted by Moore's Law [1.2]. The concept is based on achieving higher densities at a similar cost to realize more functionality, which attracts new investment for the additional research and development needed to implement the "next size smaller" device. This has been employed for Flash memory with great success over the last few decades, and should also be true in the near future. However, the long-term scalability of Flash memory device is unclear at the moment. This is due to the increased importance of device-to-device variations, and the dependence on the continued lithographic innovation, which are also common in many portions of the semiconductor industry. In addition, Flash also faces a tradeoff between the scaling of lateral device dimension and the reduction of stress-

induced leakage current (SILC) that is incurred by programming with large voltages across ultrathin oxides [1.3-1.5]. There are also challenges to maintain the coupling between the control and floating gates, and minimize the cell-to-cell parasitic interference between the stored charges when the Flash device dimension decreases. To address these issues, alternative cell designs such as silicon-oxide-nitride-oxide-semiconductor (SONOS) [1.6], and the advanced tantalum nitride-alumina-nitride-oxide-semiconductor (TANOS) [1.7-1.10] cell structures have been employed. However, the TANOS structures cannot help in further scaling of NOR Flash due to the channel hot-electron injection problem [1.11].

To further increase the device packing density, multi-level cell (MLC) NAND Flash was introduced to allow more bits to be stored in multiple levels using the same number of transistors. However, the MLC NAND Flash with the TANOS structure introduced new problems, such as the device-to-device variations, stochastic or "shot-noise" effects, random telegraphic noise, and reduction in the number of stored electrons that differentiate one stored level from the next [1.4,1.12,1.13]. These problems make MLC Flash difficult to manufacture. These few-electron problems escalate with further scaling. To address these problems, researchers have employed advanced schemes such as FinFET Flash or 3-D stacking of Flash memory [1.14-1.19]. Although these schemes may have better device performance or lower cost per unit of storage, they are more difficult to fabricate than the conventional Flash.

It remains very difficult for Flash to continue scaling to sub-10 nm technology nodes. Flash researchers are already facing a lot of challenges to maintain device specifications, such as the write/erase performance, write endurance, and data

retention, let alone to improve them. Also, as Flash struggles to maintain the current levels of reliability and performance while increasing density, new applications created based on these specifications are barely adequate [1.20].

Flash has also been employed in solid-state drive (SSD) applications in recent years [1.21]. There has been a considerable time lag between the introduction of Flash-based SSD, and the widespread use of Flash in consumer applications. This is due to the need to build system controllers and computer codes that can avoid the unnecessary writes, perform the static/dynamic wear-leveling and pipeline writes, and maintain the pre-erased blocks to hide the poor write/erase and endurance performance of Flash [1.22,1.23]. Thus, the cost of manufacturing Flash-based SSD is high as it typically uses the single-layer cell (SLC) Flash, rather than MLC Flash, which has a lower cycle endurance and slower write speed [1.24].

Hence, there is a need for a new NVM that has a higher scalability than NAND Flash to reach the higher densities needed in future technology nodes. There is also a need for a NVM that has a better write/erase performance and higher cycle endurance than Flash, to reduce the cost of NVM-based SSD. A NVM that combines high performance, high density and low cost would bring even greater benefits in terms of streamlining or simplifying the memory/storage hierarchy throughout the computing platforms, all the way up to high-performance computing. The new NVM could replace multiple memories such as SRAM, DRAM, Flash, and hard disk drives (HDD), and become a so-called “universal memory”.

For more than a decade, a number of promising NVM candidates have been proposed as a possible Flash “replacement” [1.25]. The candidates range from

technologies that have reached the market after successful integration in CMOS fabs (phase-change, ferroelectric and magnetic RAM), to novel ideas that are at the proof-of-concept stage (racetrack memory and organic RAM), to technologies that are somewhere in between (resistance RAM, and solid-electrolyte memory). These candidates have both strengths and weaknesses. In general, the strengths and weaknesses of the NVM candidates are better understood as they progress towards real device integration. And as research gives way to development, new weaknesses tend to be revealed. In contrast, by avoiding these known pitfalls, fresh new technologies are immediately attractive, at least until their own unique weaknesses are discovered.

1.2 What is PCRAM?

Phase-change random access memory (PCRAM) is a nonvolatile memory technology that uses the reversible switching of a phase-change (PC) material between amorphous and crystalline states for data-storage applications.

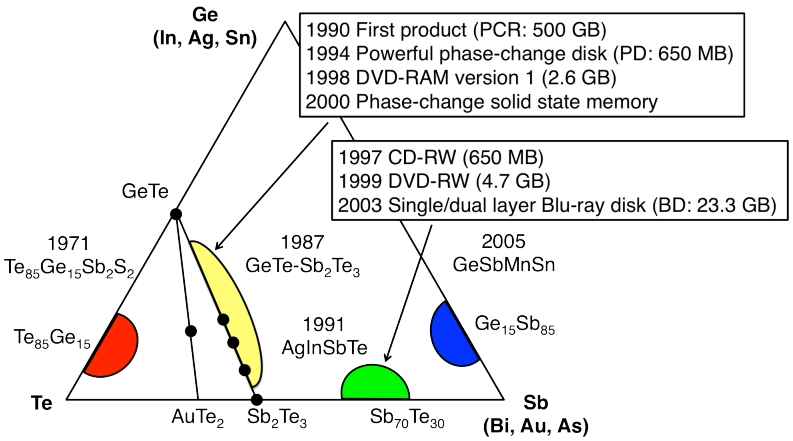

Fig. 1.1. Diagram of the phase-change alloys and their historical applications [1.34].

It possesses near-ideal memory attributes like non-volatility, fast programming speed, good scalability and high overwriting cycles [1.20,1.26-1.29]. The concept is based on the reversible switching effect of chalcogenide materials first discovered by S. R. Ovshinsky in 1968 [1.30]. It was then known as the ovonic unified memory (OUM) [1.31], and was made up of semiconductor–like chalcogenide alloys containing one or more elements from group VI of the periodic table. An example is the commonly used $Ge_2Sb_2Te_5$ (GST) alloy. PC materials were first used in optical disk memory to make re-writable CDs, DVDs and Blu-ray discs [1.32-1.35] (Fig. 1.1), before being exploited in the early 2000s by semiconductor industries to create solid-state memories known today as PCRAM, PCM, CRAM or PRAM [1.36-1.43].

1.3 Operating Principle of PCRAM

In general, PC materials can exist in 2 states, either in the crystalline state (low resistance) or the amorphous state (high resistance). In a conventional PCRAM structure, a small volume of the PC material near the electrode is used as a programmable resistor for storing information, as illustrated in Fig. 1.2.

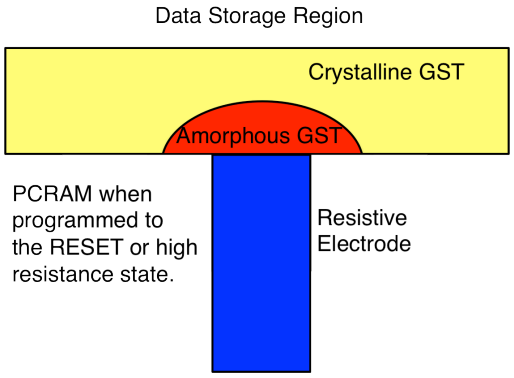

Fig. 1.2. Data storage region in a PCRAM cell [1.31].

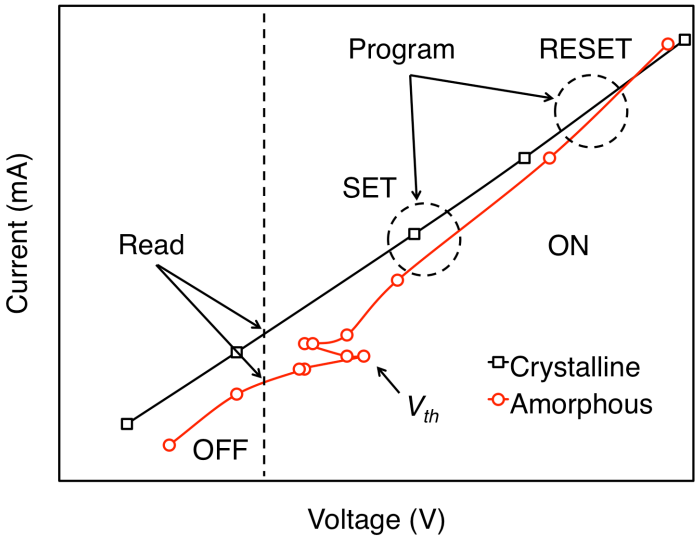

Fig. 1.3. *I-V* characteristics of PCRAM.

To program PCRAM, a current pulse applied at a voltage above the switching threshold V_{th} is required to drive the PCRAM from the amorphous state to the crystalline state (Set process), or from the crystalline state to the amorphous (Reset process), depending on the current magnitude applied (Fig. 1.3). The voltage "snap-back" at V_{th} is a unique characteristic of the PCRAM, as a result of the threshold-switching mechanism. To read the data, a small current is applied to measure the resistance level of the crystalline and amorphous states.

For the Set process, an electrical pulse of low voltage amplitude and long duration is required to heat the PC material above the glass-transition temperature (~300 ºC) for crystal formation. In contrast, for the Reset process, an electrical pulse of high voltage amplitude and short duration is required to heat the PC material beyond the melting point (~650 ºC) before it quenches quickly into the disordered state, as shown in Fig. 1.4.

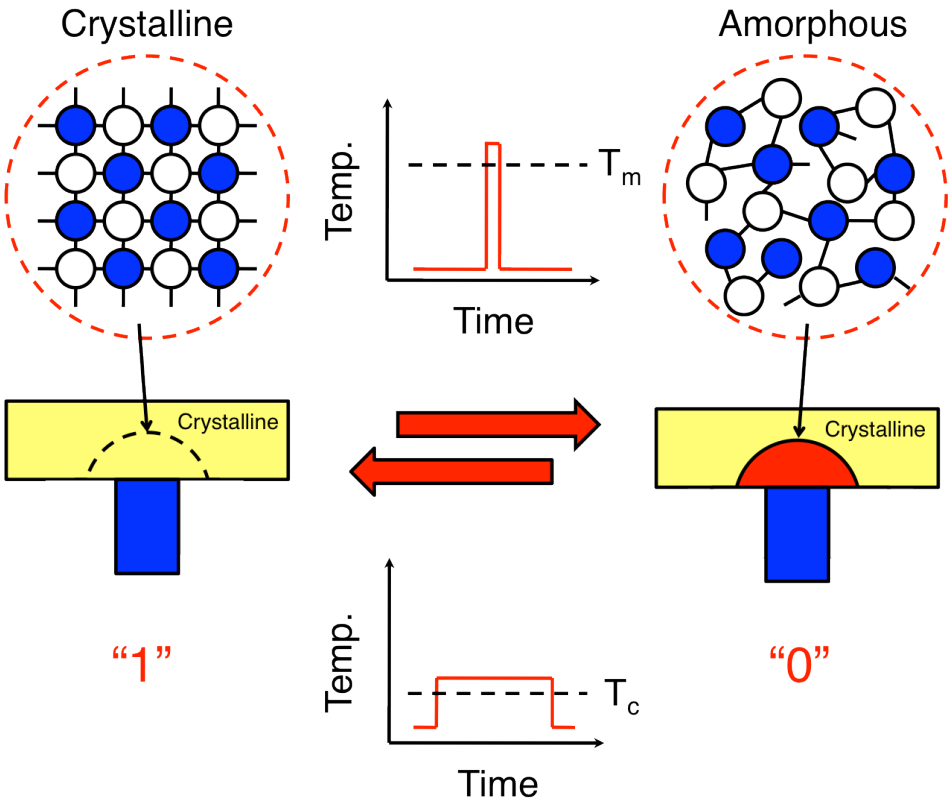

Fig. 1.4. Reversible electrical phase switching of PCRAM.

1.4 PCRAM Applications

As mentioned earlier, one of the greater motivations to develop a new NVM is not only to have a better device performance than Flash, but also to develop a universal memory that can work across multiple layers of the existing memory hierarchy in modern computers, as shown in Fig. 1.5.

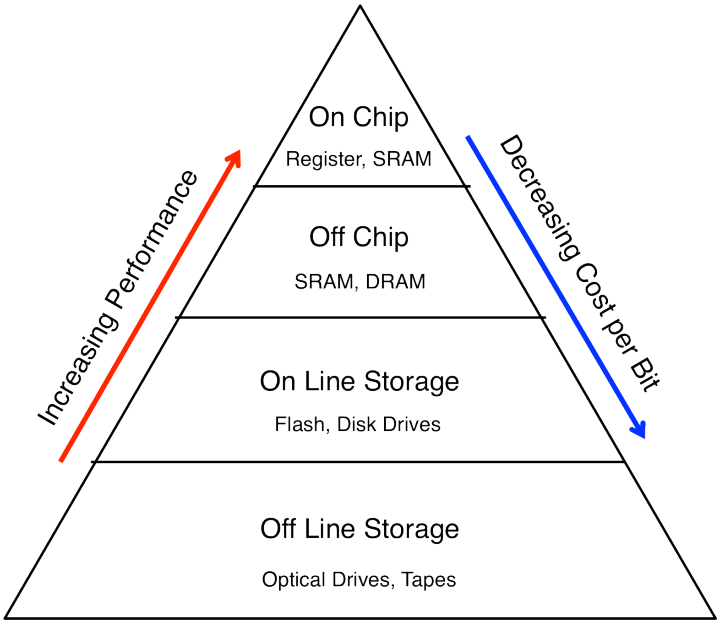

Fig. 1.5. Memory hierarchy in computers. The hierarchy spans orders of magnitude in read-write performance, ranging from the small numbers of expensive yet high-performance memory devices (on chip) to the large numbers of low-cost yet very slow storage devices (off line storage) [1.20].

The memory hierarchy is designed to bridge the performance gap between the fast central memory devices and the slower storage devices, while keeping the overall system cost down, as depicted in Fig. 1.6. Currently, there is a gap of more than 3 orders of magnitude between the access time of the fast memory devices, and the write-cycle time of the slow storage devices. This continues to widen rapidly. It is thus important to develop a universal memory that can perform the functions of both the memory and storage devices, while maintaining low cost. This will boost the overall speed of computer systems.

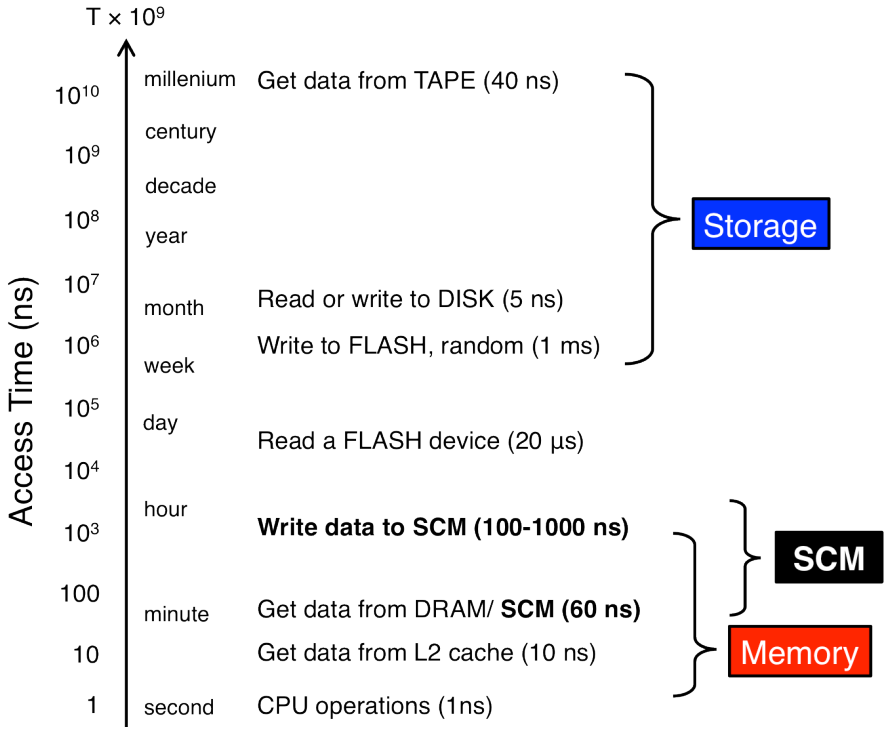

Fig. 1.6. Access times for different memory and storage devices, both in nanoseconds and in terms of human perspective. For the latter, all times are scaled by 10^9 so that the fundamental unit of a single CPU operation is analogous to a human making a one second decision. In this context, writing data to Disk can require more than "1 month" and retrieving data from an offline tape cartridge takes "1000 years" [1.20]. SCM refers to storage class memory.

PCRAM has the potential to replace the fast memory units such as SRAM and DRAM. SRAM and DRAM are typically embedded close to the central processor unit (CPU), serving as high-performance level 1 (L1) and level 2 (L2) cache memories, and video RAM and level 3 (L3) cache memories, respectively [1.44]. A typical SRAM cell has six CMOS transistors, two p-type MOSFETs, and four n-type MOSFETs, covering more than 120 F^2 (F is the minimum feature size, and F = P/2, with P being the minimum pitch allowed by the considered lithography) in chip real estate per bit. State-of-the-art DRAM cells occupy 6 F^2 in chip area. PCRAM competes favorably with both SRAM and DRAM in terms of the cell size. Such small cell sizes (6 F^2) have already been demonstrated in

PCRAM using a diode-select device [1.45]. PCRAM also competes favorably with DRAM in terms of scaling into future technology nodes. This is because DRAM is facing scaling limitations such as write-caused inference (write requests interfere with read requests), device leakage, and challenges in the integration of high-aspect ratio capacitors in very small spaces. As such, DRAM has already fallen behind NAND Flash and standard CMOS logic technologies in terms of scaling to the 45 nm node, and is expected to fall even further behind in future technology nodes. In terms of endurance, the required write endurance for SRAM is about 10^{18}. For DRAM, the required write endurance can be estimated using the following equation:

$$N_e = T_{life} \frac{B}{\alpha C}, \tag{1.1}$$

where N_e is the cycle endurance, T_{life} is the life span of the system, B is the bandwidth, is the wear-leveling efficiency, and C is the system memory capacity. Assuming a typical server with a ten-year life span, 1 GB/s bandwidth, 10 % wear-leveling efficiency, and 16 GB capacity, the endurance requirement for DRAM is approximately 10^8, which is within the reach of PCRAM (10^{12}) [1.46,1.47]. More recently, researchers have found that lowering the total energy delivered in a Reset pulse can increase the PCRAM endurance [1.48]. This reveals a possible method for PCRAM to achieve SRAM-like endurance in the future. Both SRAM and DRAM have high power consumption. For instance, DRAM requires a substantial amount of power to simultaneously address multiple banks within a chip (for every bit that passes into or out of the DRAM chip, 8 or even 16 devices are being internally accessed, read, and then re-written), and to re-write

after each read access (periodic refresh). Thus, by being nonvolatile, PCRAM is already a lower-power alternative to both SRAM and DRAM, despite the relatively high power of PCRAM write operations, which can be further reduced via structural and material modifications [1.36-1.42]. The most challenging issue for PCRAM is to achieve the speed performance of both SRAM and DRAM. Embedded SRAM and DRAM devices typically run at the clock speed of a CPU, and their access time is less than 10 ns. The performance limiter for PCRAM is the Set speed, which in turn depends on the crystallization speed. Although researchers have demonstrated the use of Set pulses shorter than 10 ns [1.49-1.52], real device applications tend to use Set pulses varying from 50 to 500 ns [1.53]. This is mainly due to the emphasis on achieving a high thermal stability of the amorphous phase at the expense of crystallization speed.

PCRAM also has the potential to replace slow storage devices such as Flash, SSD, and HDD. NOR Flash is used for embedded logic applications that require fast access to data that is modified only occasionally [1.7]. In contrast, NAND Flash is used for low-cost mass-storage applications with slower random access time, which require high-density and a block-based architecture [1.19]. NOR and NAND Flash occupy chip areas of about 10 F^2 and 4 F^2, respectively [1.19]. NAND Flash can employ 2-4 bits per physical memory cell in MLC Flash to further increase the effective number of bits per unit area in a chip [1.19]. As mentioned earlier, Flash-based SSD is already rapidly replacing the HDD, where cost and reliability are important. PCRAM has already demonstrated small cell sizes very close (4-6 F^2) to that of NAND Flash. Multi-level storage is also possible for PCRAM with the demonstration of both 2 and 4 bits per cell

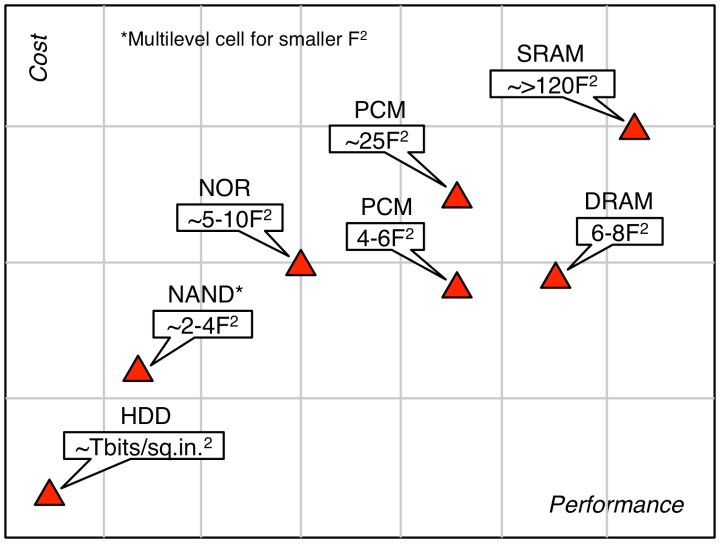

Fig. 1.7. Schematic of cost and performance of different memory and storage devices. PCM has the potential to be a storage class memory, bridging the large gap in cost and performance between the memory and storage devices [1.20].

[1.54,1.55]. In terms of speed, NOR Flash has a read time of a few tens of ns, and a write time of around 10 μs. In contrast, PCRAM has both fast read and write times of several 10 ns.

Currently, the industry has proposed the use of PCRAM as a storage class memory (SCM) [1.22-1.23] to bridge the gap in the access times between the memory and storage devices. The idea is to develop a SCM that has both the high performance and robustness of a solid-state memory, and the low cost and non-volatility of conventional hard-disk magnetic storage. Researchers have further proposed to divide SCM into two segments: 1. A slower variant, referred to as S-class SCM, which would operate much like a Flash-based SSD, but with better endurance and write performance. 2. A faster variant, referred to as M-class SCM, which would operate fast enough to be synchronous with memory operations, and has a lower power-per-unit capacity and lower-cost-per-capacity, so that it could be connected to the memory controller. Both variants are intermediate stopgap

measures to the access time difference problem, as shown in Fig. 1.7. A universal memory is still very much desired.

1.5 Challenges in PCRAM

Overall, the key limitation for PCRAM is the data-transfer speed. A faster PCRAM speed is very much required to match or better the speed of existing fast memory devices such as SRAM and DRAM. This would enable PCRAM to bridge the large gap in the access times between memory and storage devices, and function as a universal memory.

Besides achieving a fast PCRAM speed, it is also important to consider the power consumption of PCRAM to fully leverage its good scalability properties, and to achieve the high density needed for a universal memory. The integration of PCRAM into an array architecture typically requires the use of an access device, which can be a diode [1.56], field-effect transistor [1.57], or a bipolar junction transistor [1.55]. These devices are needed to minimize the leakage current that would otherwise arise from the non-selected cells in the array. It is essential to know whether these access devices can provide sufficient current to Reset a PCRAM cell. While a diode can provide a current-to-cell size advantage over a planar transistor down to the 16 nm node [1.58], the diode is more prone to write disturbs due to the bipolar turn-on of the adjacent cells [1.45]. In terms of performance, a 5.8 F^2 PCRAM diode cell fabricated using the 90 nm technology can be operated with a current of 1.8 mA [1.45]. In contrast, a 90 nm 10 F^2 tri-

gate field-effect transistor can only supply approximately half as much current [1.45].

Another important consideration is the cycle endurance of PCRAM. Endurance is one of the strengths of PCRAM, especially in comparison with Flash, where the stress-induced leakage current (SILC) limits the Flash endurance to 10^4-10^5 write-erase cycles. Single PCRAM devices can demonstrate up to 10^{12} Set-Reset cycles without significant degradation of resistance contrast [1.26]. However, large-scale PCRAM integration studies only show endurance numbers in the range of 10^8-10^9 cycles [1.59,1.60]. This is still far from what is necessary for a DRAM replacement without wear-leveling (Equation 1.1).

1.5 Aim of Research

Material dimensions reduced to the nanoscale can show very different properties from the materials in a bulk form. This can be attributed to the high surface area to volume ratio of nanoscale materials, which makes it possible to achieve new size-related effects. One example is the "quantum size effect", where the electronic properties of solids are modified due to the large reduction in the particle size. This effect does not come into play by going from the macro to micro dimensions; it only becomes pronounced when the nanometer size range is reached.

In this thesis, the nanoscale effects in PC materials and functional materials are studied to increase the PC speed, and to achieve low power consumption and high endurance at the same time. In a PCRAM device, the crystallization speed is much slower than the amorphization speed due to the trade-off between the crystallization

speed and thermal stability of the amorphous phase [1.33]. It is very important to increase the crystallization speed, as it determines the overall data transfer speed of PCRAM. Also, the power consumption of PCRAM is high due to the high thermal energy needed to melt and quench the PC material during the Reset process. A lower Reset power is needed to achieve a higher packing density. In addition, PCRAM has limited cycle endurance. It has to achieve a higher cycle endurance to become a DRAM-replacement. These would pave the way for PCRAM to become a broadly applicable memory device.

1.6 Organization of Thesis

This thesis is organized into 5 main chapters, beginning with the current chapter on the introduction of nonvolatile memory, and the emergence of PCRAM. The potential applications, and the challenges to be overcome were also presented.

The aim of Chapter 2 is to provide an overview of the current state of research on the speed of PC materials. The chapter also provides a review of the theories, mechanisms, and models related to the speed of PC materials, as well as the associated power and endurance factors. It motivates the study of nanoscale effects in PC materials, as well as the other functional materials, which are employed to address the main challenge this thesis is concerned with: How to achieve fast and stable PC?

In Chapter 3, the focus is on the study of the pre-structural ordering (incubation) effects of nanostructural units in PC materials, and the exploitation of this finding to achieve sub-nanosecond switching in PCRAM. Experimental

demonstration of the incubation effect is presented. The microscopic origin of the incubation effect is also discussed in this chapter.

Moving on to Chapter 4, a study of nanostructured PC materials is presented. Based on studies and understanding, nanostructured PC materials are employed to achieve both fast-speed and high-endurance in PCRAM simultaneously. A detailed study on the switching mechanism in nanostructured PC materials is also discussed and presented.

Chapter 5 decribes the study of nanoscale PC materials with superlatticelike (SLL) structures to achieve fast switching speeds, while maintaining low-power consumption in PCRAM. The device characteristics and performance of PCRAM with the SLL structures are presented. Studies of interface and thermal-confinement effects in the SLL structures are also provided.

In Chapter 6, the properties of nanoscale SLL dielectric are studied. This understanding is used to achieve fast speed, as well as low power, and high endurance in PCRAM. Material and electrical characterization studies are provided. The effects of interface and other factors are also discussed.

At the end of the thesis, the main results are summarized in chapter 7. An outlook on possible future research is also presented.

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Chapter 2

PCRAM Review

This chapter reviews the speed performance of PC materials and devices. It begins with an introduction to the history, limitations, and speed of PCRAM. This is followed by a study of the mechanisms, theories, factors, and models for fast phase transitions. Towards the end, the power and endurance of PCRAM will also be discussed.

2.1 Speed of PCRAM

Speed is an important factor for PCRAM as it determines the data-transfer rate in a computer system. The data-transfer rate, together with the cycle endurance, determines the possible applications and markets that could be considered for PCRAM. Three processes, known as Set, Reset, and Read, determine the overall speed performance of PCRAM. In the early days, PC materials crystallized too slowly for them to be technologically competitive with other memory materials. They had very slow transitions times, in the microsecond to millisecond timescales [2.1]. It was only in the late 1980's that crystallization times on nanosecond timescales were achieved, as a result of the emergence of new PC materials from the GeTe-Sb_2Te_3 pseudobinary system [2.2]. This led to the widespread use of PC materials in optical rewriteable disc technology, and later in PCRAM devices.

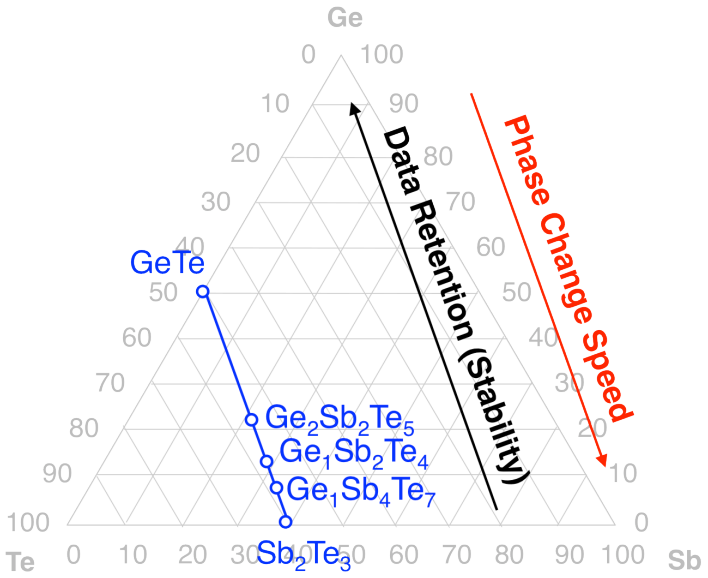

Fig. 2.1. Speed and stability properties of PC materials.

However, it is challenging to increase the speed of PCRAM due to the contradictory nature between the crystallization speed and thermal stability of the PC materials [2.2] (see Fig. 2.1). In general, PC materials with high crystallization speeds have a lower crystallization temperature, causing the data stored in an amorphous bit to be easily lost through unintentional crystallization. It is thus very important to find new methods to increase the crystallization speed of PC materials without compromising the stability of the amorphous phase.

2.1.1 Amorphization Speed

Amorphization (Reset) involves the transformation of a PC material from the crystalline phase to the amorphous phase. It requires Joule heating of the PC material above its melting temperature, followed by rapid cooling below the crystallization temperature to solidify the material. The amorphization process is

generally fast. The shortest electrical pulses achieved for Reset were of a few hundred ps [2.3,2.4].

2.1.2 Crystallization Speed

Crystallization (Set) involves the transition of a PC material from the amorphous phase to the crystalline phase. It is much slower than the amorphization process. The Set process for a PCRAM device involves threshold switching, Joule heating, crystal nucleation, and growth. Since the latter two processes are the slowest, they determine the overall speed of PCRAM devices. The shortest electrical pulses demonstrated for Set were in the range of 1-10 ns [2.4-2.7].

2.1.3 Read Speed

Read operation depends on the speed at which the amorphous and crystalline states can be reliably distinguished. It is determined by circuit considerations, such as the capacitance of the bit-line being charged up, and leakage from the unselected devices. Read operations are generally performed in 1-10 ns [2.8].

2.2 Threshold Switching Mechanism

While many researchers supported the idea that PC is a thermal effect [2.9-2.10], there are also researchers who advocated that PC is an electronic process known as threshold switching [2.11]. Although initially suggested by Ovshinsky [2.1], Adler was the first to show that the switching of chalcogenides may not be thermal,

provided that the carrier generation driven by the field and carrier concentration competes with the strong Shockley-Hall-Read recombination via localized states [2.11-2.12]. However, his model remains theoretical, and a link between the model and the atomic structure of chalcogenides is still lacking.

Pirovano *et al.* further developed the threshold switching theory by employing semiconductor concepts [2.13]. Figure 2.2 shows the proposed bandgap models for crystalline and amorphous $Ge_2Sb_2Te_5$ (GST) alloys, based on their long-range and intermediate-range structural ordering, respectively. In the models, they suggest the crystalline and amorphous materials have respective bandgaps of 0.5 and 0.7 eV. Threshold switching occurs due to the competing roles of impact ionization and recombination via valence alternation pairs. During threshold switching, the carrier recombination increases at a slower rate than the carrier generation under a strong electric field. The free carriers reside in the localized states before they recombine. As a result, the free-carrier concentration increases rapidly to induce a high current at the threshold voltage for switching to occur. Although the theories and simulation results are in agreement with the *I-V* characteristics of GST, there is a lack of experimental evidence for impact ionization in GST.

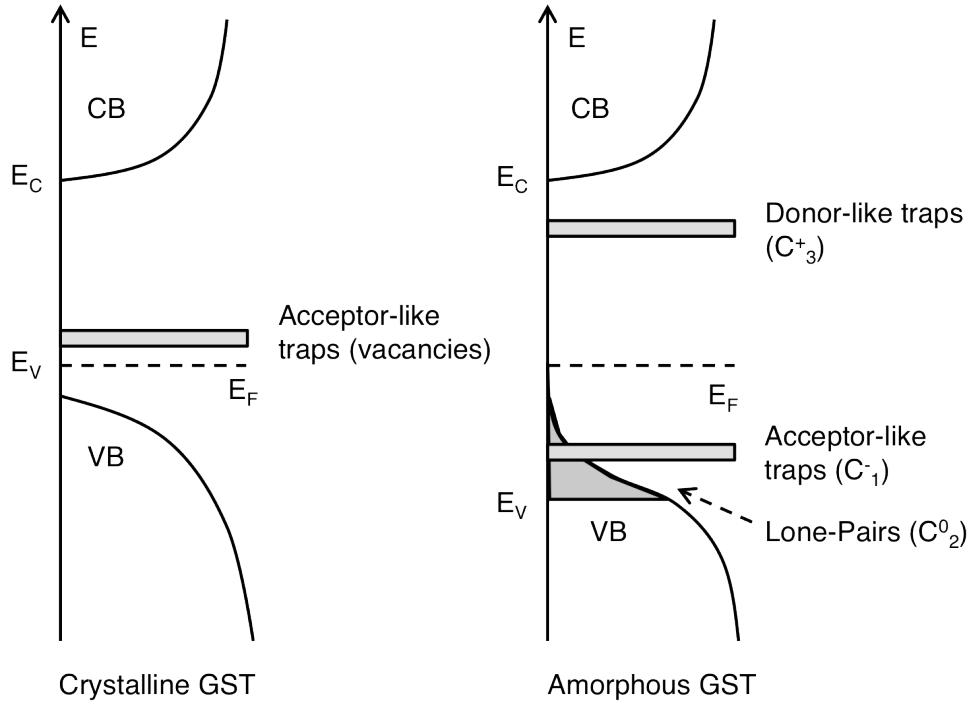

Fig. 2.2. Schematic band diagram of GST in crystalline and amorphous states [2.13].

2.3 Crystallization Theory

2.3.1 Homogenous Nucleation

Nucleation and growth processes govern the crystallization kinetics of PC materials [2.14-2.19]. Nucleation involves the formation of small crystalline nuclei in the amorphous matrix, and growth involves the subsequent expansion of a phase front separating the amorphous and crystalline regions.

The driving force for crystallization is the gain in free energy below the melting temperature. The reversible work for crystal cluster formation $\Delta G(r)$ for a spherical crystalline cluster of radius r within an undercooled melt is given by [2.14-2.16]:

$$\Delta G(r) = V(r) \cdot \Delta G_v + A(r) \cdot \sigma \quad , \tag{2.1}$$

where V and A are respectively the volume and surface area of the nucleus, G_v is the free energy difference between the parent and crystalline phases per unit volume, and σ is the interfacial energy per unit surface area. The critical nucleus size or radius is:

$$r_c = \frac{2\sigma}{|\Delta G_v|} \tag{2.2}$$

At the critical nucleus size, $\Delta G(r)$ is a maximum. This means that only nuclei larger than the critical nucleus size can gain sufficient energy and grow. For nuclei smaller than the critical nucleus size, the nuclei tend to dissolve the interface is removed, reducing the free energy of the system. A steady-state distribution of subcritical clusters is formed after an incubation time period [2.20]. From the steady-state distribution, the steady-state nucleation rate I_{ss} given by [2.15,2.16]:

$$I_{SS} \propto \eta(T)^{-1} \exp\left(-\frac{\Delta G(r_c)}{k_B T}\right) \tag{2.3}$$

is derived. η is the liquid viscosity, T is the absolute temperature, and k_B is the Boltzmann constant. For nuclei larger than the critical nucleus size, the speed of growth u in the framework of classical crystallization theory is:

$$u(T) = \frac{\partial r}{\partial t} \propto \frac{T}{\eta(T)}\left[1 - \exp\left(-\frac{\Delta G(T)}{k_B T}\right)\right] \tag{2.4}$$

2.3.2 Heterogeneous Nucleation

Heterogeneities such as foreign phases and impurities can promote nucleation, and affect the activation energy for crystallization [2.21]. This can be considered in the framework of the crystallization theory. The critical work for heterogeneous cluster formation is governed by [2.22,2.23]:

$$\Delta G^{het} = \frac{16\pi}{3}\frac{\sigma^3}{(\Delta G_v)^2}\cdot f(\theta) \quad , \tag{2.5}$$

where θ is the wetting angle. The exposed volume fraction $0 \leq f(\theta) \leq 1$ relative to a sphere of the same radius r is [2.23]:

$$f(\theta) = \frac{(2+\cos\theta)(1-\cos\theta)^2}{4} \tag{2.6}$$

Impurities and interfaces can both catalyze nucleation, but also impede growth. If heterogeneous sites play a dominant role, crystallization shifts from being triggered in the whole volume of the material to the vicinity of these heterogeneous sites.

2.3.3 Crystallization Factors

2.3.3.1 Temperature

The maximum probability of nucleation and growth is known to occur at different temperatures. Generally, one of the processes is dominant, leading to the sub-classification of crystallization mechanisms into nucleation-dominated and

growth-dominated. There are 3 temperature regions important in the study of the crystallization mechanisms.

Both liquidus and glass-transition temperatures (see Fig. 2.3) define the three temperature regions. The liquidus temperature (T_l) is the maximum temperature at which crystals can co-exist with the melt or liquid-phase of a material. Above T_l, the material is liquid at equilibrium, while upon-continuous cooling, the liquid may crystallize at T_l and show a decrease in specific volume. On the other hand, a liquid that survives below T_l without crystallization form an undercooled liquid. During further cooling, both viscosity and diffusion of the undercooled liquid may become substantially high and small, respectively, such that the time-scales for atomic rearrangement (crystallization) become infinitely long. At this point, which is known as the glass-transition temperature (T_g), the liquid becomes frozen, which results in glass formation.

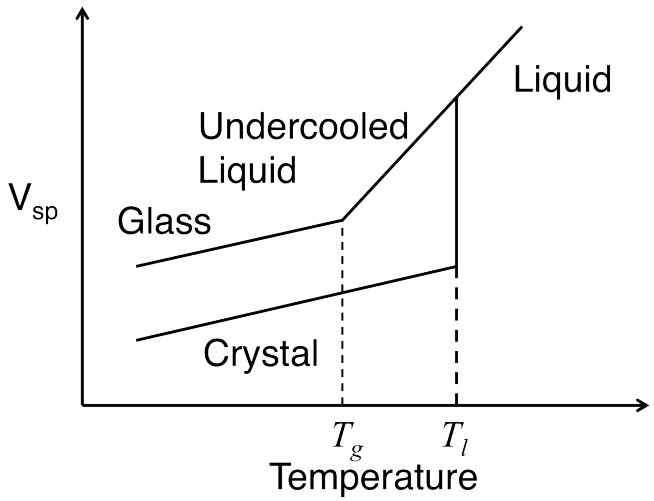

Fig. 2.3. Schematic of specific volume (V_{sp}) as function of temperature for a liquid that can both crystallize and form a glass. T_g and T_l refer to the glass transition and liquidus temperatures, respectively.

The first region is located below T_l. The small driving force for crystallization enables the study of the undercooling of droplets using differential thermal analysis. The maximum undercooling can be defined as $\Delta T_u = T_l - T_c$, where T_c is the temperature at which crystallization occurs upon the application of a constant cooling rate. This is combined with measurements of the heat of fusion to derive limits for the interfacial energy and steady-state nucleation rate. The steady-state nucleation rates of GST and Ge_4SbTe_5 were found to be higher than those of $Ge_{12}Sb_{88}$ and AgInSbTe [2.24]. For this reason, the former materials were classified as nucleation-dominated materials, while the latter were classified as growth-dominated materials [2.25].

The second region is located around T_g. In this region, crystallization occurs very slowly. This enables direct observation of nucleation and growth, which were demonstrated using transmission electron microscopy and atomic force microscopy [2.26-2.29]. These studies showed that the growth velocities of GST, Ge_4SbTe_5, and AgInSbTe have an exponential temperature dependence, which relates to their data-retention properties (for example, the stability of the amorphous phase for 10 years at 80 °C).

The third region is located between T_l and T_g. In this region, crystallization occurs rapidly. This makes it highly challenging to study the crystallization properties of PC materials. Two approaches have been adopted. One approach involves the study of PC materials under the operating conditions in an optical or electronic PC device. By using specialized equipment to spatially and temporally resolve the phase-transition, the performance properties of a PC material, for example the minimum crystallization time, minimum power, and degree of

change in optical reflectivity, can be obtained [2.3]. The other approach involves the study of the morphology of a crystallized bit using transmission electron microscopy [2.27,2.30]. This reveals the distribution and shape of the crystallites, from which the distribution of nuclei and their growth can be inferred.

2.3.3.2 Growth at Crystalline-Amorphous Rim

During the amorphization of a bit, a crystalline rim is typically created due to the small temperature gradients, and thus spatial differences in cooling rate. This prevents amorphization beyond a certain distance from the laser spot or heating element in an optical or electronic PC device. Growth at the crystalline rim plays an important role in PCRAM devices.

2.3.3.3 Initial Amorphous Configuration

The initial configuration of the amorphous phase affects the crystallization properties of PC materials. Crystallization of an as-deposited phase was observed to be different from the re-crystallization of a melt-quenched phase [2.31-2.33]. It was also noted that structural units (i.e. of the metastable distorted rocksalt structure), such as 4-fold rings, planes and cubes present in the as-deposited phase, which are not present in the melt-quenched phase, may vanish after the first PC cycle.

2.3.3.4 Feature Size

Nucleation and growth can be observed in large volumes of PC materials in optical recording. The crystallization speeds of nucleation-dominated PC materials, which recrystallize predominantly by nucleation inside the amorphous region and have high nucleation rates, do not show volume dependence; the time needed to crystallize an amorphous bit does not depend on the volume of the PC material. In contrast, growth-dominated PC materials, which recrystallize by growth from rim of the amorphous region and have high growth rates, show volume dependence; a faster crystallization time is achieved in PC materials with smaller volumes [2.5]. However, the sub-classification of the materials becomes less useful for small volumes, where geometries and interfaces play a more important role. In small volumes, growth becomes dominant in the crystallization process.

2.3.3.5 Material Interfaces

Interfaces between materials can affect the crystallization process in optical and electronic PC devices [2.34-2.36]. PC materials sandwiched between different dielectric films can exhibit different nucleation processes, and can have different activation energies for crystallization [2.34]. The crystallization process of amorphous GST film sandwiched between dielectric films was studied by measuring the changes in the transmittance of the samples. Single-layer amorphous GST films were observed to crystallize in two stages: nucleation, followed by growth. These two processes were distinguished by their exothermal

crystallization patterns. Si_3N_4 and Ta_2O_5 were found to accelerate nucleation, while SiO_2 was observed to inhibit it. Also, ZnS and ZnS with 20 mol % SiO_2 were observed to promote nucleation, even in the grain growth process. Wettability measurements indicate that surface reactivity and chemical affinity are the factors responsible for these effects.

The choice of electrode materials in PCRAM devices also affects crystallization behavior [2.36]. For instance, in PC films less than 5 nm thick, the crystallization temperature is strongly influenced by the selection of the interface material [2.36].

2.4 Phase-Change Models

There have been numerous studies on the material properties of PC materials in both crystalline and amorphous phases. However, the switching kinetics of PC materials is still not well understood. To improve the understanding of PC kinetics, atomistic models such as the umbrella-flip and structural ordering models were developed.

2.4.1 The Umbrella-Flip Model

Kolobov and co-workers proposed a so-called “umbrella-flip” model to explain the crystallization of GeSbeTe-based systems [2.37]. They postulate that crystallization occurs via a flip of the Ge atom from a tetrahedral site to an octahedral site, which explains why the switching of GST is fast and stable. PC

may not require the rupture of strong covalent bonds, and the transition can be diffusionless. The Te sublattice and the local structure around Sb atoms are preserved. It explains why PC can be easily reversed. The material does not have to be transformed into a truly liquid state, and bond rupture is due to electronic excitation. The amorphous structure is well-defined in the model, enhancing the reversibility of the transition.

Further simulations and experiments were performed to test the model. They showed that, while tetrahedrally coordinated Ge atoms are present in the amorphous phase, they only make up a third of all the Ge atoms [2.38]. These tetrahedral Ge atoms mostly form homopolar Ge-Ge or Ge-Sb bonds, instead of the Ge-Te bonds as proposed in the umbrella-flip model. The crystallization kinetics are also dependent on the structural configuration of the amorphous phase. The results obtained from the as-deposited samples are less relevant, as the PC material is crystallized from the melt-quenched state during read/write operations. Another problem with this model is that it requires a certain atomic order or distortion pattern. Otherwise, the coordination number of Ge would exceed four upon flipping from the octahedral site [2.39]. Furthermore, this model cannot be applied to PC materials that do not contain Ge.

2.4.2 Structural Ordering Model

The amorphous and crystalline phases have common structural features such as AB-alternation and preferentially octahedral coordination [2.40]. The amorphous phase resembles a largely disordered variation of the crystalline phase. It has a

pronounced disorder that destroys the medium-range order, and removes the resonant behavior of covalent bonds in the crystalline phase.

The structural evolution of the amorphous phase can be modeled using ring statistics. Four-membered rings with ABAB-alternation, resembling those in the crystalline structure, can be observed in the amorphous phase. Hegedus and Elliott [2.40] have performed ab initio molecular dynamics on GST, simulating the complete PC cycle (melt-quenching followed by re-crystallization). From their results, a time-resolved evolution of wrong bonds and near-regular fourfold rings (i.e. near-planar, near rectangular four-membered rings of atoms) was obtained. Crystallization resulted in a decrease in the number of wrong bonds. In contrast, the number of near-regular fourfold rings increases. This provides a simple model for the phase-transition of GST. This method can also be applied to other PC materials to gain valuable insights into their crystallization mechanisms.

2.5 Amorphization Theory

Understanding amorphization is essential to achieving both fast crystallization and amorphization. Amorphous PC materials can be formed via a melt-quench process. During the melt process, the PC material is heated and transformed from a solid phase to a liquid phase. Subsequent quenching occurs, and the liquid becomes increasingly rigid. If the glass-transition temperature is passed, and given that crystallization does not occur, the atomic mobility D becomes too small for the structural re-arrangement to reach thermal equilibrium. The undercooled liquid is "frozen" into a glassy or amorphous phase. The glass-transition temperature is

commonly defined as the temperature where the viscosity equals 1×10^{12} Pa s [2.41]. The atomic mobility of a liquid is inversely related to the viscosity η via the Stokes-Einstein equation:

$$D(T) \propto \frac{T}{\eta(T)} \tag{2.7}$$

The quenched glass is not in thermal equilibrium, and is subjected to relaxation of the structure to an equilibrium state, known as "ageing" effects. Glasses can be sub-classified into easy glass formers and poor glass formers. The former can be formed under a slow cooling rate, while the latter can only be formed by fast quenching.

The ease of glass formation is linked to the viscosity of the materials [2.42,2.43]. A high viscosity results in low atomic mobility and impedes crystallization. In contrast, a low viscosity allows for high mobility and promotes crystallization. The viscosity of a material is temperature dependent. A material is defined as being a strong liquid if its temperature dependence is Arrhenius-like. Conversely, a material is defined as being fragile [2.42] if it exhibits a behavior empirically described by the Tamann-Vogel-Fulcher ansatz:

$$\eta(T) = \eta_0 \cdot \exp\left(\frac{A}{(T - T_0)}\right), \tag{2.8}$$

where η_0, A, and T_0 are constants. As a measure of the deviation from Arrhenius behavior, the fragility m is introduced as a steepness index at T_g:

$$m = \frac{\partial(\log_{10}\eta)}{\partial\left(T_g / T\right)}\Big|_{T=T_g} \tag{2.9}$$

Given that viscosity is fixed at both the glass-transition temperature T_g and the liquidus temperature T_l, a strong liquid is less likely to crystallize at slower cooling rates than is a fragile liquid. Thus, a link between fragility and ease of glass formation can be drawn. It should be noted that a fragile liquid appears to be a desirable property for a PC material since crystallization speed would increase with temperature (above T_g). However, this is only reasonable if the use of a fragile liquid does not severely inhibit the amorphization process.

2.6 Power Consumption of PCRAM

Amorphization affects the power needed to Reset a PCRAM device. Currently, the Reset power is high due to the large thermal energy required to melt a PC material. The Reset current is much higher than the Set current, and it determines the overall power of PCRAM devices. Reducing the Reset current is very important. It would enable the integration of PCRAM with small Si transistors.

In a conventional mushroom-type cell, the PC material and top electrode are planar layers deposited on a plug-type bottom heater contact (see Fig. 1.2). The region of the PC material involved in the phase transition is a hemispherical volume on top of the heater. To reduce the Reset current, it is important to improve the thermal properties of the cell. This is typically achieved via two methods: 1. Increase Joule heating in the cell, and/or 2. Improve the thermal confinement of the cell.

Joule heating can be increased by injecting current through a smaller cross-sectional area, via a reduction of the contact area between the PC material and

heater, to obtain a higher current density. This was achieved by scaling the diameter of the heater plug in the mushroom-type cells [2.44], or by using a conductive liner as a heater in edge-contact [2.45], μTrench [2.46], or ring-contact cells [2.47].

Another approach to increasing Joule heating is by structuring the PC material into a narrow cross section in bottle-neck [2.48], and self-heating pillar cells [2.49]. Further improvements were achieved by increasing the resistivity of the PC material through nitrogen or oxygen doping [2.44,2.50]. A highly resistive layer, such as TiON, was also inserted between the PC material and the bottom heater to increase Joule heating in the resistive layer [2.51].

To improve the thermal confinement of PCRAM devices, a confined cell structure was proposed [2.52]. In this structure, the PC material was deposited in a pore etched back in the heater. The confined cell structure not only concentrates the active volume, but also surrounds a large part of this volume by a dielectric layer with a low thermal conductivity. However, this approach requires conformal deposition of the PC material. An alternative method was later developed to structure the PC material, rather than the heater, to form the plug- or pillar-type cells [2.53].

Better thermal confinement was also achieved by increasing the thickness of the PC material. This can reduce the heat flow from the bottom heater to the top electrode heat sink [2.52]. However, this increases the threshold voltage required to Set the PCRAM. A lateral-type cell structure was also proposed to improve the thermal confinement of the cells [2.54]. It benefits from having a heating zone

that is separated from the electrode contacts, and a capping layer comprising of a thermally-insulating dielectric.

Material modifications can also improve the thermal-confinement of the cells. Different insulating materials, such as porous dielectric, were employed to reduce heat dissipation [2.55]. It should be noted that the improved thermal isolation should not prevent the rapid quenching of the melt, and inhibit the amorphization process.

2.7 PCRAM Endurance

The endurance of PCRAM is strongly influenced by the Reset and Set processes. Repeated Reset and Set operations can lead to two types of device failure. These failures are known as “stuck-Reset” and “stuck-Set” [2.56,2.57].

In a stuck-Reset failure, the PCRAM cell shows a sudden increase in its resistance to a very high resistance level, which is much more resistive than the Reset state. The cell can no longer be switched from this high resistance state to the low resistance state. This can occur after degradation in the resistance contrast, but also with no prior indication that a failure is imminent. This can be attributed to void formation or delamination at the heater-to-GST material interface in the cell, which prevents current from passing through the device.

In a stuck-Set failure, a gradual degradation of the resistance contrast is normally observed during a repeated Set-Reset cycling. The resistance level of the Reset state decreases, and the Reset pulse becomes less effective at switching the cell to a consistent high-resistance level (or creating an amorphous plug in the

cell). Eventually, the cell cannot be switched, regardless of the Reset pulse applied, and the cell remains in the Set state.

The factors contributing to the stuck-Set failure were studied. The stuck-Set failure was attributed to a change in the Reset conditions [2.58]. The pulse amplitude and duration were found to affect the endurance of a PCRAM device, with the pulse duration having the stronger impact. By using Reset pulses ranging from 10 ns to 10 μs, Goux and co-workers showed that a higher endurance can be achieved in Ge-doped SbTe PC bridge devices by reducing the Reset pulse duration [2.58]. Their data suggests the endurance of PCRAM scales inversely with $t_m^{3/2}$, where t_m is the time spent melting the PC material. The results also suggest that the gradual cell degradation associated with the stuck-Set failure is strongly correlated with the melting process in the Reset operation.

The material properties of the failed cells were studied using energy dispersion spectroscopy (EDS), secondary ion mass spectrometry (SIMS), and energy dispersive x-ray spectrometry (EDX) [2.59-2.70]. The composition of the PC material was observed to change during the cycling process. Studies on mushroom-type GST cells showed an agglomeration of Sb at the bottom electrode at the expense of Te. The behavior of Ge remains unclear.

The results suggest that a change in the composition of PC materials during cycling results in a steady decrease in the dynamic resistance of the active region, shifting the required Reset current to larger values. This leads to a stuck-Set failure if the Reset pulse is not adaptively increased, or to a stuck-Reset failure if the Reset pulse energy is increased to compensate.

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Chapter 3

Sub-Nanosecond Switching in Phase-Change Memory Incubated with Nanostructural Units

In the preceding Chapter, a review of the speed performance of PCRAM was presented. PCRAM operations are generally fast and in the order of nanosecond timescales. However, despite efforts to increase the crystallization speed, it has been difficult to lower it below 1 nanosecond.

The study presented in this Chapter aims to overcome this limitation through controlling the crystallization kinetics of a PC material by the application of a constant low voltage, leading to the incubation of nanostructural units in the PC material. The fastest crystallization and reversible switching speeds possible are examined. The PC kinetics in PCRAM devices and the structural origin of the incubation-assisted increase in crystallization speed are also investigated. This will pave the way for achieving a broadly applicable memory device, capable of nonvolatile operations beyond GHz data-transfer rates.

3.1 Concept of Incubation

According to classical nucleation theory, the nucleation of small crystallites and their subsequent growth are the two main distinct processes in crystallization [3.1-3.3]. The nucleation rate is faster at lower temperatures, while rapid growth

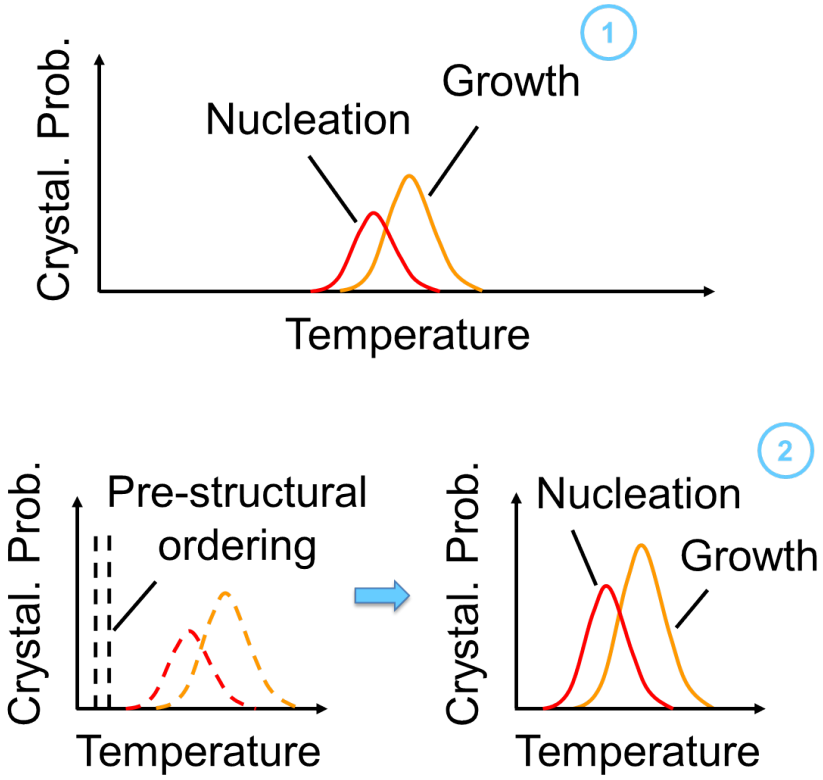

Fig. 3.1. Schematics of the crystallization probability as a function of temperature for PC materials. The nucleation and growth processes are accelerated when there is pre-structural ordering (from method 1 to 2).

occurs higher temperatures [3.4]. These processes can be stimulated and altered to control the speed of crystallization, as shown in Fig. 3.1.

The approach is based on the idea of providing a constant, weak electric field to induce thermal pre-structural ordering (incubation of ordered clusters in the amorphous matrix) via Joule heating, enabling faster nucleation and growth upon application of a subsequent stronger electrical pulse, while maintaining the high stability of the amorphous phase by controlling the cluster-size distribution (Fig. 3.2). This thermal-incubation model is very different from the model of Karpov *et al.* [3.5], which assumes a direct electrical-field-induced modification of the crystal-nucleation barriers in $Ge_2Sb_2Te_5$.

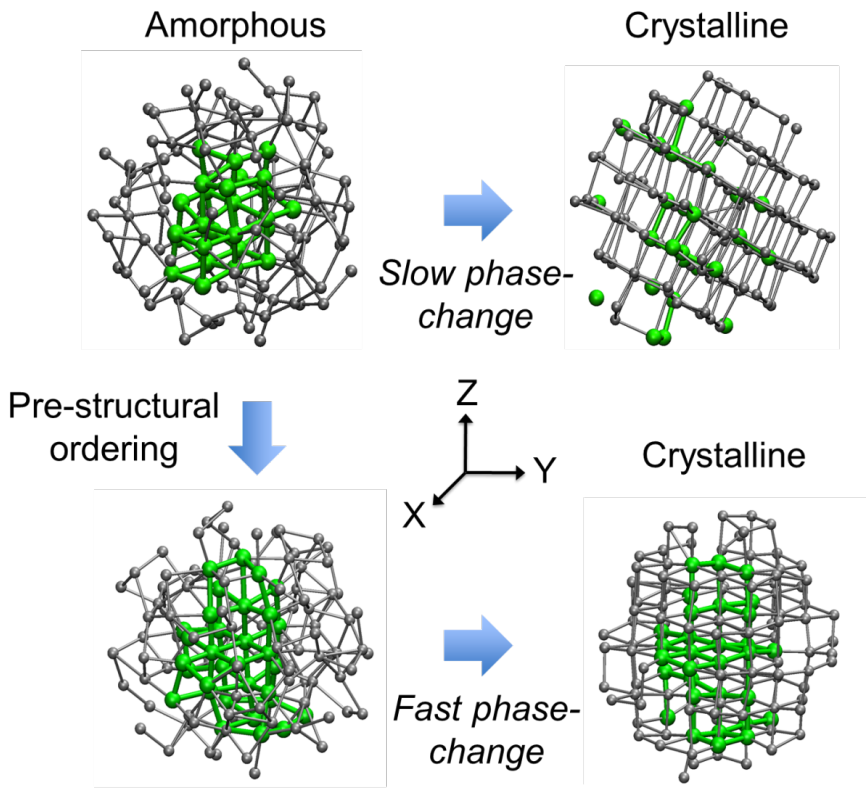

Fig. 3.2. Pre-structural ordering effects on the crystallization of PC materials. Simulated model configurations demonstrating the atomic rearrangements during the phase transition, with and without pre-structural ordering.

3.2 Methodology

3.2.1 Device Fabrication

Pore-like structured PCRAM cells (with GST as the PC material) were experimentally fabricated and used to study the incubation effects on the crystallization speed (Fig. 3.3). 4-inch Si wafers with 1 μm thick SiO_2 were used as the starting material in the PCRAM fabrication. The bottom electrode was first patterned and deposited with 200 nm thick TiW, followed by the deposition of 30 nm dielectric material. Vias were etched in the dielectric material to form the active device region, and the diameter of the vias is defined as the cell size. To

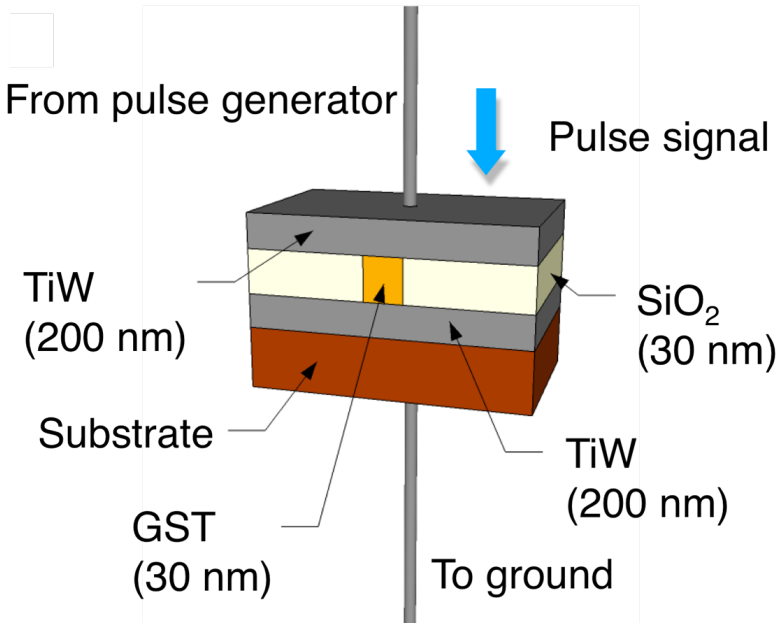

Fig. 3.3. Schematic of the PCRAM structure with the pulse signal delivered to heat and crystallize the PC material (GST).

study the size-dependent switching speed, PCRAMs with cell sizes varying from 50 to 300 nm were employed. The vias were filled with 30 nm of GST. Finally, 200 nm of TiW was deposited and patterned to form the top electrode.

3.2.2 Electrical Characterization

To study the ultrafast switching effects, a weak electric field, equivalent to ~0.3 V, for tailoring the crystallization kinetics (hereafter referred to as the incubation field), was employed to achieve optimal switching properties, without activating spontaneous crystallization (Fig. 3.4).

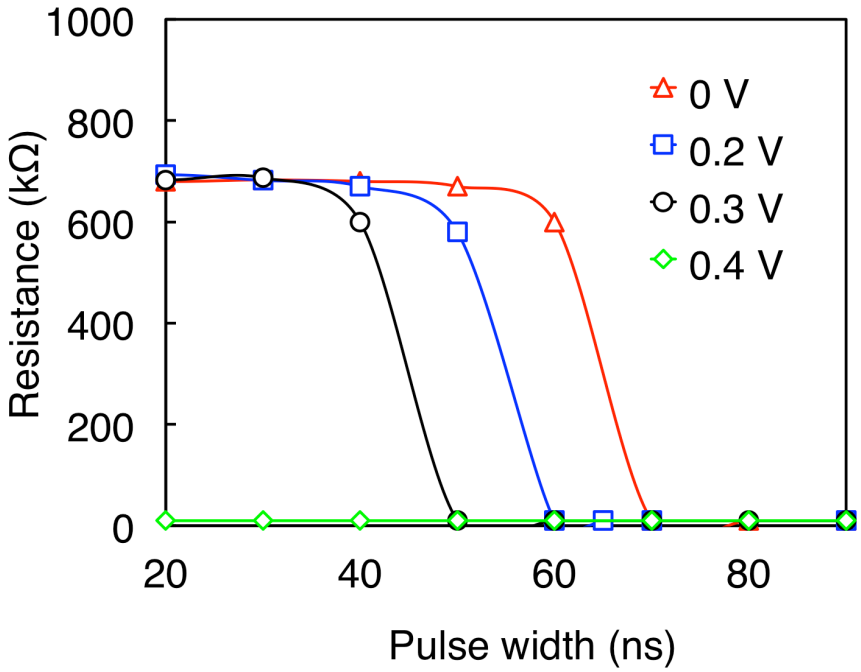

Fig. 3.4. Dependence of the resistance on pulse width employed for a cell, at different incubation conditions. The resistance decreases abruptly at shorter pulse widths as the incubation field increases (0.1-0.3 V). As the field exceeds 0.3 V, a low resistance level is obtained, regardless of the pulse width employed, due to spontaneous crystallization. The cell size is 300 nm.

Subsequent electrical pulses varying in length from several hundred ps to several tens of ns were employed to switch the cells, as shown in Fig. 3.5. The full-width half-maximum (FWHM) values of the pulses were used to characterize the switching speeds of the cells (Appendix A).

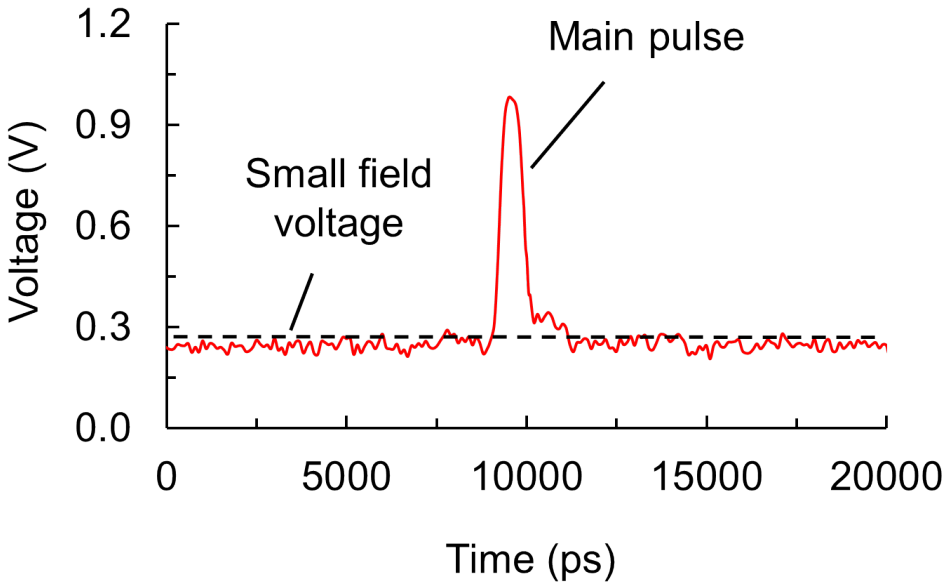

Fig. 3.5. Waveform of a small-field incubation voltage and main pulse applied to Set the PCRAM. A small voltage is first applied to initiate pre-structural ordering, followed by a main pulse to induce crystal nucleation and growth of the PC material.

3.3 Device Performance

3.3.1 Crystallization Behavior

The incubation field, even with the small amount of thermal energy delivered by it, can significantly promote the nucleation and growth of PC materials. The nucleation and growth times can be characterized by the minimum electrical pulse width needed to switch the cell from the amorphous to crystalline state [3.6], also known as the Set process. When the incubation field is applied to a cell (Fig. 3.6), much faster nucleation and growth is observed, as evident in the significant decrease in pulse width by ~5 ns; calculated from the difference between pulse widths required by the cells with and without incubation, at different voltage levels (0.7, 0.8, and 0.95 V). For the fastest nucleation and growth, the shortest

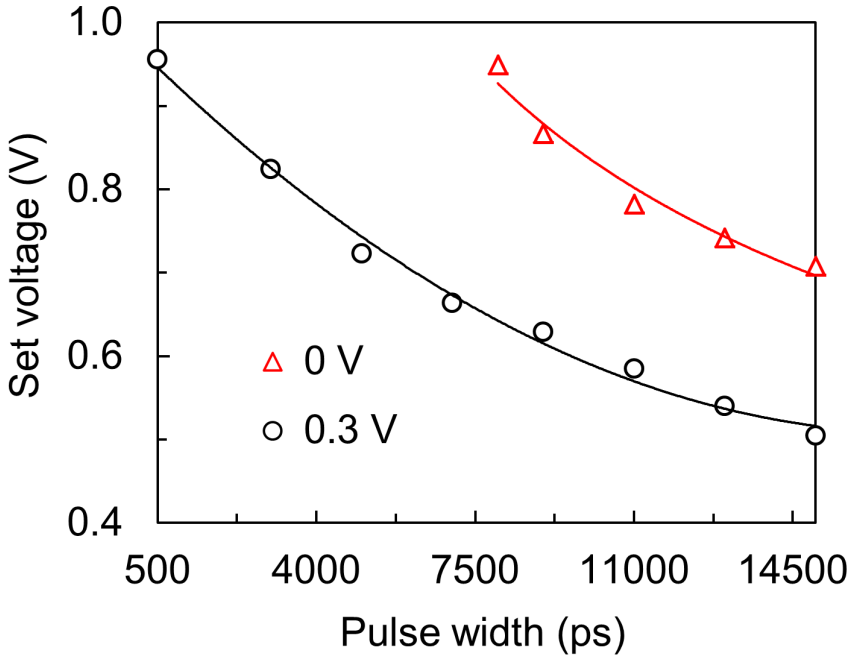

Fig. 3.6. Dependence of minimum voltage on the pulse width achieved by a PCRAM cell (50 nm) under incubation field conditions (0.3 V). The fastest speed achieved was 500 ps.

pulse was found to be 500 ps. This is approximately an order of magnitude faster than the fastest switching speeds previously achieved in GST/GeTe cells with similar cell sizes under full recrystallization conditions, using the voltage-peak FWHM as a measure of the pulse duration [3.7,3.8].

3.2.2 Effect on Amorphization Process

Fast crystallization speeds facilitated by an incubation field can be achieved without affecting the amorphization of PC materials (Reset process). The Reset process under an incubation field is also very fast. Amorphization speeds as fast as 500 ps were also achieved, as shown in Fig. 3.7.

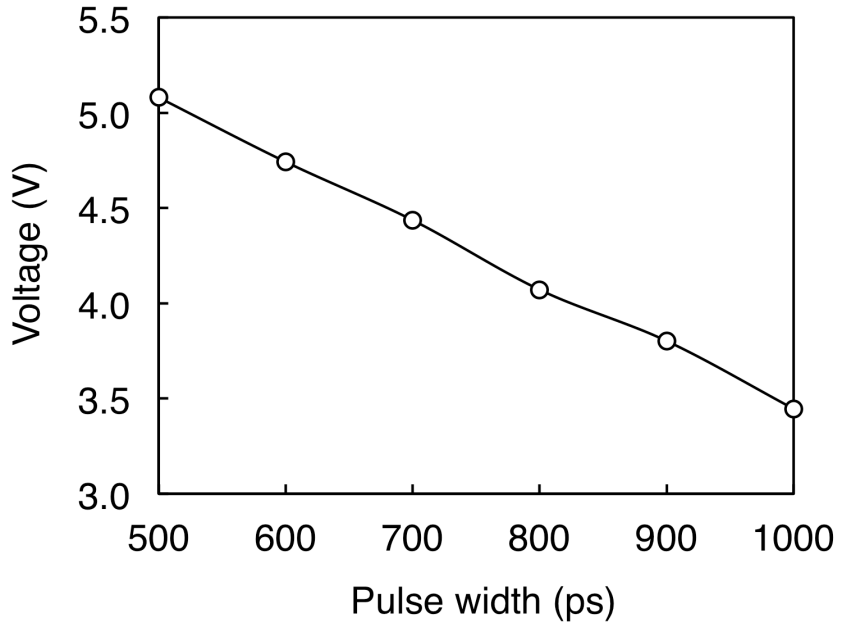

Fig. 3.7. Dependence of the minimum Reset voltage on pulse width exhibited by a cell (50 nm) under an incubation field (0.3 V). The pulse width decreases as the voltage increases. The fastest speed achieved was 500 ps.

3.2.3 Reversible Switching Performance

More importantly, upon applying the incubation field, it was found that a cell can be switched reversibly and stably with both Set and Reset pulses of 500 ps for 10^4 cycles (Fig. 3.8). Both the resistance of the amorphous state and the Reset/Set resistance ratio are relatively constant during the cycling experiment. These results show that both fast speed and stability of the amorphous phase can be achieved simultaneously.

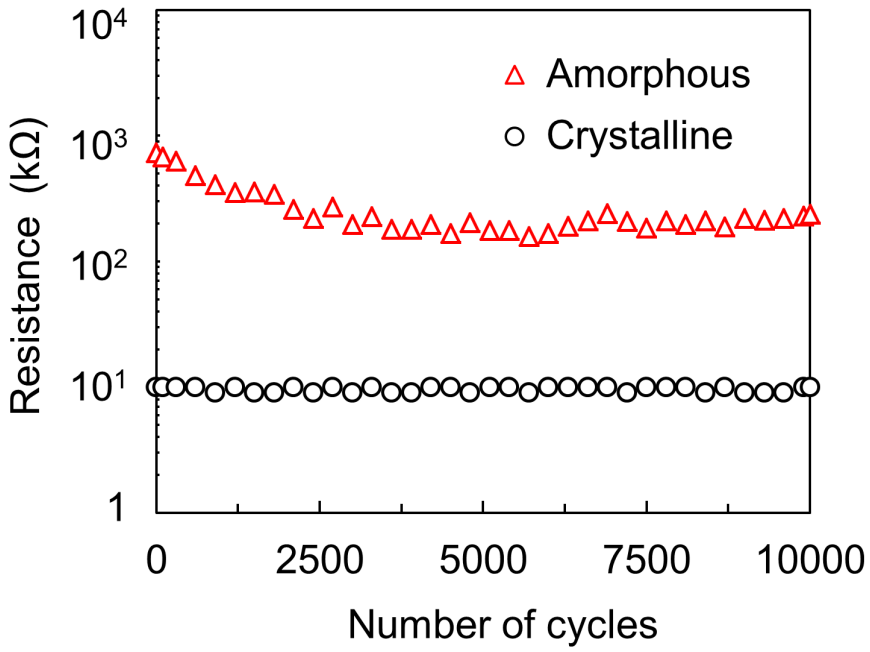

Fig. 3.8. Reversible switching of PCRAM. Fast and stable switching with 500 ps pulses for both Set (1 V) and Reset (6.5 V) is observed for 10^4 cycles.

3.2.4 Interplay between Cell Size and Incubation Field

Even faster crystallization is observed when the incubation field is applied to cells with smaller feature sizes. In general, PC materials are divided into two groups, depending on the crystallization mechanism. For nucleation-dominated crystallization, a large number of crystalline nuclei are formed in the amorphous region. For growth-dominated crystallization, the transformation of the amorphous region is dominated by the growth of the crystalline phase from the crystalline rim surrounding the amorphous region or the growth at the interface between the PC material and dielectric sidewalls in optical or electrical PC devices [3.8-3.10].

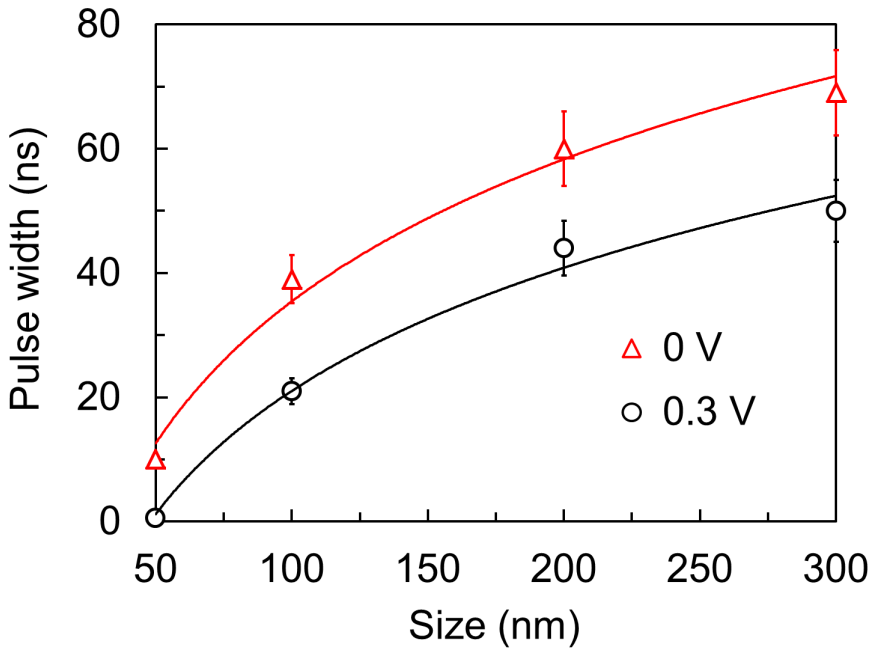

Fig. 3.9. Size-dependent switching speed of PCRAM. Shorter pulse widths were achieved when the cell size is decreased for a fixed applied Set voltage pulse (1 V). The pulse width further decreases when the incubation field (0.3 V) is applied, further improving the speed of PCRAM.

Growth-dominated crystallization can be characterized by the strong dependence of crystallization time on the size of the amorphous/active region (in this case, cell size). This growth-dominance effect can be seen in Fig. 3.9 where, under no incubation field, the pulse width for Set reduces from 70 to 10 ns as the cell size decreases (300 to 50 nm). A very different effect is observed when an incubation field is applied. It was found that the pulse width decreases even more significantly as the cell size decreases (by 28 % at 300 nm and by 95% at 50 nm). This suggests a much faster nucleation and growth induced by a combination of size and incubation effects.

3.3.5 Incubation Field Dependent Crystallization Speed

One of the key findings of this study is that it is possible to control the crystallization speed (nucleation and growth time) by varying the intensity of the incubation field. This implies, notably, that nucleation and growth can be further accelerated via stronger incubation fields. Figure 3.10 shows the pulse width needed to Set a cell (300 nm) at different incubation fields. The pulse width is observed to decrease from 70 to 50 ns as the incubation field increases (0 to 0.3 V), revealing a dependence of crystallization speed on the intensity of the incubation field. Previous works on GST [3.11] and AgInSbTe [3.12, 3.13], using optical (laser pump-probe) stimulation and direct thermal-annealing treatment, have also shown that the crystal-nucleation rate can be manipulated. However, the crystallization times achieved in those studies were only of the order of several tens of nanoseconds to a few microseconds. There are similarities and differences between data obtained for Figs. 3.10 and 3.4. For instance, both data from Figs. 3.10 and 3.4 were consistent; they show a decrease in pulse width as the incubation voltage is increased. In addition, the pulse widths observed at each incubation voltage were similar, as they were obtained from cells with the same cell-size (300 nm). But unlike Fig. 3.4, which shows data from a set of switching tests more specifically to study the incubation voltage at which spontaneous crystallization occurs, Fig. 3.10 shows more data from different sets of switching tests in a broader investigation on the correlation between pulse width and incubation voltage.

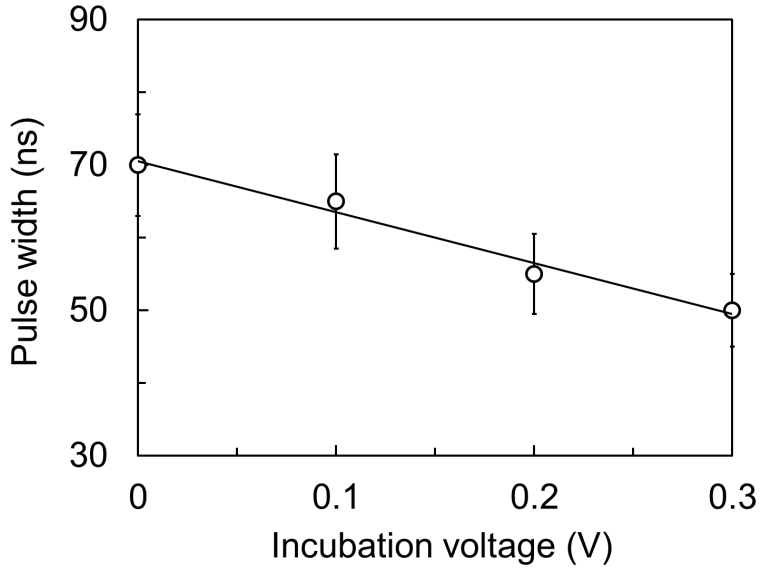

Fig. 3.10. Minimum pulse width vs incubation field (voltage) for a PCRAM cell (300 nm). The pulse width reduces as the incubation field increases, revealing the incubation-dependent crystallization speed of PC materials. Data obtained from 3 tests on the cell at each incubation voltage.

3.3.6 Power Consumption

The experimental findings show that ultrafast crystallization can be achieved by applying an incubation electrical field. The additional energy needed to apply the incubation field is much smaller than that for crystallization as the incubation voltage applied is much less than the typical threshold switching voltage (0.5-1V). Furthermore, the incubation field can be applied after a Reset process for a minimum time. One approach could be to implement a Reset-coupled-with-incubation pulse that serves to not only Reset but also incubate the cell (see Fig. 3.11). Another approach is to apply a Reset pulse followed by a separate incubation field. The Set process can be applied immediately or subsequent after the Reset-coupled-with-incubation pulse or incubation field (it should be noted that in real-device operations, the Set process is normally not applied immediately

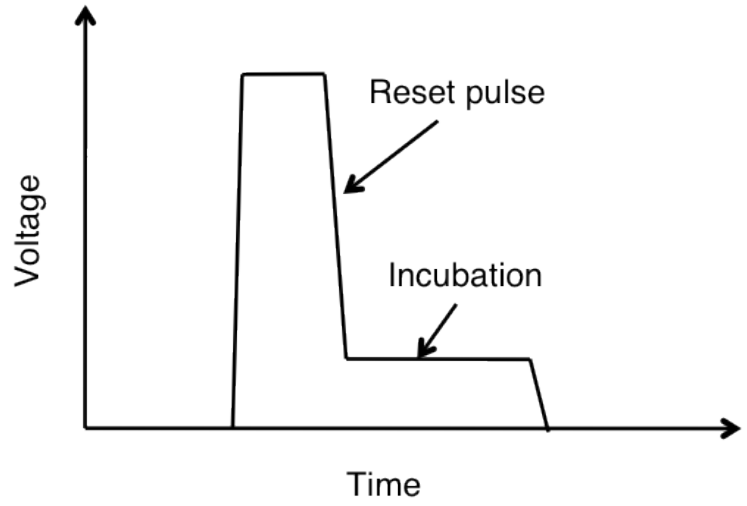

Fig. 3.11. Schematic of a Reset electrical pulse coupled with an incubation field.

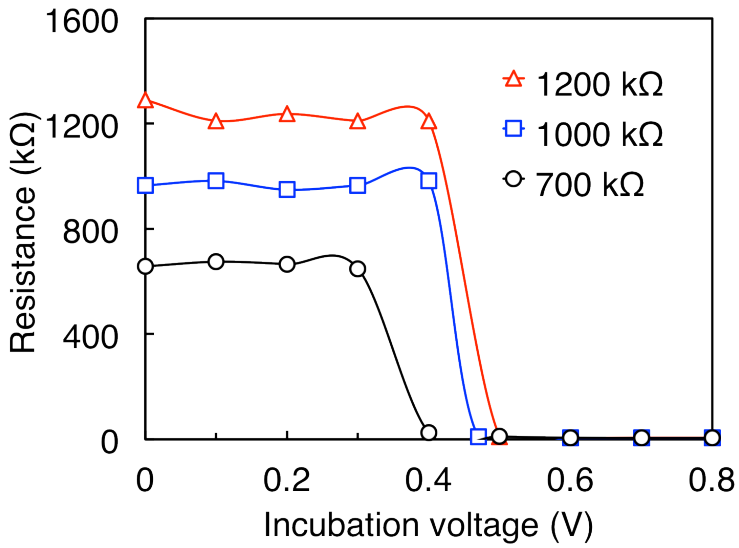

Fig. 3.12. Resistance versus incubation voltage of a PCRAM cell (1 μm). As the high resistance level decreases, a lower bias is required to Set the cell.

after the Reset process). These approaches can reduce the extra energy needed, in contrast to applying the incubation field consistently, on waiting for the Set process in real device operations. To further reduce the energy required, the PCRAM can also be operated from a lower resistance level (Fig. 3.12).

3.4 Ab Initio Molecular-Dynamics Simulation

The microscopic origin of the ultrafast crystallization resulting from the application of an incubation field was investigated by performing ab initio molecular-dynamics (AIMD) simulations on 180-atom models of GST (See Appendix B). To simulate the crystallization process upon the application of incubation fields and/or electrical pulses, two temperatures of 420 K and 600 K were applied to the GST models to mimic the respective annealing/Joule-heating processes (hereafter, annealing at 420 K being referred to as 'pre-annealing').

The detailed procedure for simulating the amorphous-to-crystal phase transition is shown in Fig. 3.13. For a more complete (statistical) analysis, three amorphous (a-) models (models 1-3), obtained by independently quenching different configurations of liquid GST, were studied. The basic structural units of crystalline GST (i.e. of the metastable distorted rocksalt structure), such as 4-fold rings, planes, and cubes, were used to characterize the local structural order and the crystallization process during annealing.

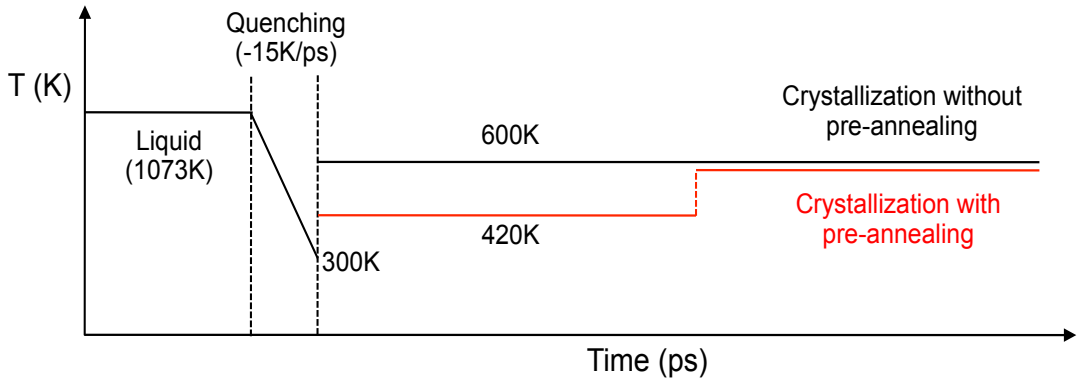

Fig. 3.13. Temperature profiles used for the AIMD simulations with or without pre-annealing.

To investigate the effect of applying an incubation field on the crystallization behavior, one of the a-models (3) was first pre-annealed at 420 K for 270 ps and subsequently annealed at 600 K. For comparison, the same model was also annealed at only 600 K. The crystallization process in both cases was examined by studying the evolution of the number of cubes; the onset time (t_o) of crystallization is defined here as the starting point of the increase in size of the stable cube cluster, while the end of crystallization was considered to be the time when no further growth in the number of cubes is observed.

3.4.1 Structural Evolution

Much faster crystallization is observed for the pre-annealed model, as shown in Fig. 3.14. The t_o for the pre-annealed model is much shorter (~80 ps) compared to that for the non-pre-annealed model (~350 ps). A similar shortening in t_o is also observed for another model that was pre-annealed for a longer time. The corresponding changes in atomic structure for these two different annealing routes are shown in Fig. 3.2, which explains the origin of the faster crystallization. Before t_o, there were significant thermal fluctuations upon annealing at 600 K that resulted in the disruption of the initial cluster in the non-pre-annealed model. After a period of repeated generation and annihilation of transient clusters (defined here as an incubation time), a stable cluster (having a different orientation from the initial one) formed and grew as the model crystallized. This was not the case for the pre-annealed models; the initial ordered structure (further grown during pre-annealing) maintained its shape and grew along its original

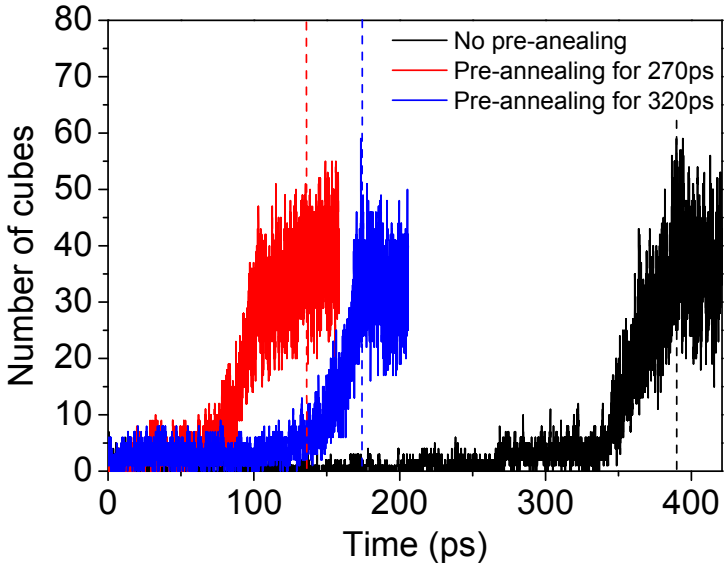

Fig. 3.14. Variation of the number of cubes during annealing at 600K with different durations of pre-annealing.

symmetry axis throughout the crystallization. Thus, the shortening in t_o for the pre-annealed models can be associated with shorter incubation times for nucleation and growth, which is triggered by the structural ordering during pre-annealing.

3.4.2 Crystallization Mechanism

The amorphous models (models 1-3) were pre-annealed at 420 K for 270 ps. Figure 3.15 shows that these models have initially different degrees of structural order; model 3 has the greatest population of more highly connected planes and cubes (being the most ordered), while the smallest number of such structural units was found in model 1 (being the least ordered). In this sense, our models altogether, eventually, describe the structural evolution of an amorphous system having various degrees of local structural order. The predominant structural-

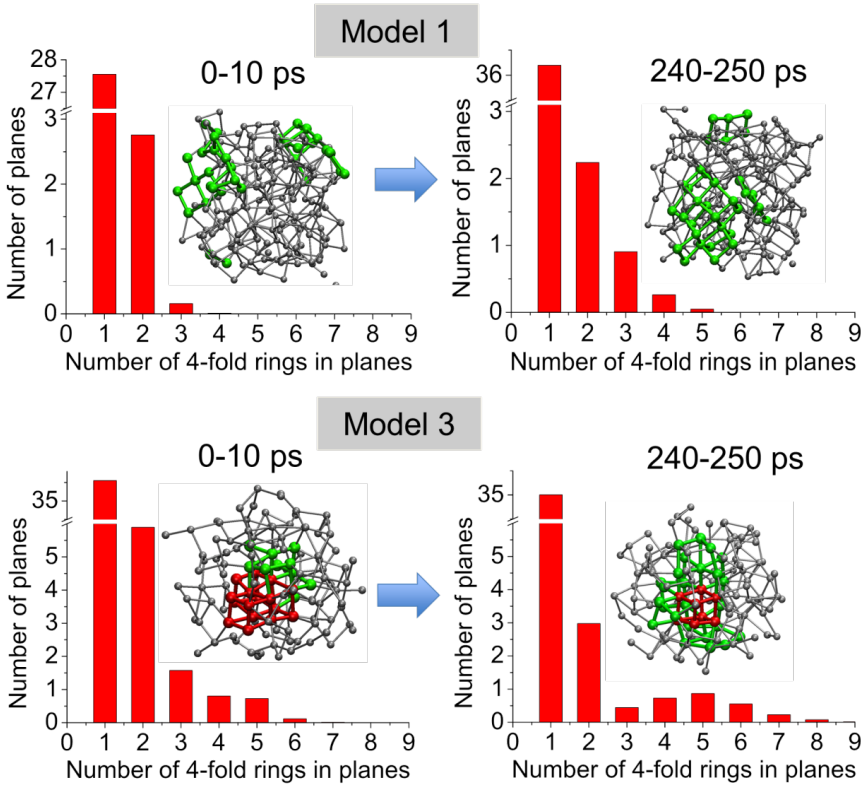

Fig. 3.15. Population of 4-fold rings and planes, composed of different numbers of 4-fold rings, in model 1 before and after pre-annealing. The number of planes was averaged over the time interval denoted in the figure. A similar change in the distribution of the number of planes is seen in model 3. Atoms colored green are in planes; red atoms are in cubes.

ordering mechanism was found to be the formation and growth of clusters of planes of 4-rings (i.e. a structural feature of the rocksalt structure of the crystalline phase of GST), indicative of an overall medium-range ordering in the amorphous phase.

3.4.3 Stability of Incubated State

This pre-structural ordering is stable in nature. Figure 3.16 shows the mean-squared displacements of atoms during the two-step annealing. The diffusion

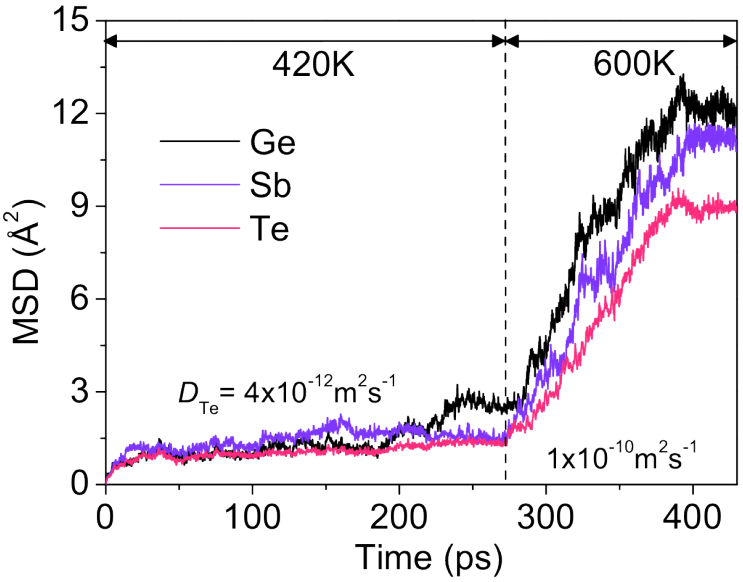

Fig. 3.16. Mean-squared displacement data for each type of atom during two successive annealing steps at 420 K and then at 600 K (model 3). Diffusion coefficients for Te atoms, calculated at each annealing temperature, are shown as an example.

coefficient (*D*) at 420 K is estimated to be about two orders of magnitude smaller than at 600 K. The structural ordering in a-GST at 420 K was found to be rather diffusionless; the formation and/or growth of a cluster of planes occurs mostly via cooperative (bond-rotational) movements (over much less than interatomic distances) of a few relevant atoms, which is in direct contrast to the structural ordering at 600 K, which is induced by bond-breaking diffusional processes. This difference in behavior is most likely due to insufficient thermal energy being available at 420 K to overcome the energy barrier for diffusion. Consequently, the growth speed and the size of clusters at this low temperature should be kinetically limited, in spite of the driving force for nucleation (i.e. free-energy difference) being greater than at higher temperatures [3.14].

3.5 Conclusion

Rapid crystallization times, as well as high amorphous-state stability, can be achieved through an electrically-induced incubation process in PCRAM devices, which alters the crystallization kinetics of a-GST. This method is, in principle, applicable to all types of PC materials and memory-device structures, so that an appropriate combination of programming schemes and PC materials opens opportunities for optimizing PCRAM device performance.

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Chapter 4

Fast-Speed and High-Endurance Switching in PCRAM with Nanostructured Phase-Change Materials

Studies on the incubated nanostructural units in PC materials in the preceding chapter have enabled us to achieve sub-nanosecond PC speeds in PCRAM. Since the ultimate goal is to develop PCRAM for a broad range of memory applications, it is equally important for PCRAM to achieve both fast speed and high endurance simultaneously. Although fast speed and high endurance can be achieved separately, it is still unclear whether PCRAM can demonstrate both of these qualities at the same time.

The present chapter aims to address this issue by controlling the PC mechanism using nanostructured PC materials. The change in the PC mechanism with device size, and its impact on the PC speed, are studied. The grain size-dependent PC speed is also investigated. Finally, the nano-thermal and electrical effects on the speed, stability, and endurance of PCRAM cells are evaluated. These findings lead to a feasible solution to achieve a universal memory.

4.1 Properties of Nanostructured Phase-Change Materials

It is well known that when materials are reduced to nanoscale dimensions, they show very different properties. Nanoscale effects can influence the crystallization

temperature, melting temperature, and other material properties vital to PCRAM operations [4.1-4.4]. They can have a significant impact on the PC mechanism, which may allow the achievement of fast speed and high endurance at the same time.

Nitrogen-doped GST (NGST) is an intrinsically stable PC material and has a higher endurance compared to GST, due to the fact that the excess nitrogen atoms segregate to the grain boundaries [4.5-4.7]. However, it has a slower crystallization speed, in the hundred ns timescales, insufficient to achieve the high writing speeds required for DRAM applications. Despite this, the grain-size of NGST can be controlled and reduced to form grains with very small sizes [4.8,4.9]. In this study, a novel approach to achieve both high speed and high endurance via the exploration of the PC mechanisms and grain features of PC materials is presented.

4.2 Methodology

4.2.1 Device Fabrication

Pore-like structured PCRAM cells with different NGST grain and cell sizes were fabricated to study the device performance of PCRAM with nanostructured materials, as shown in Fig. 4.1. SiO_2-on-Si substrate was used as the starting material, on which an electrode comprising of 200 nm thick TiW was formed. A 30 nm thick SiO_2 dielectric layer was subsequently deposited and etched to form pores with diameters ranging from 25 to 200 nm, which were used to define the

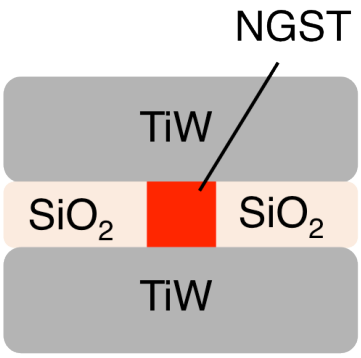
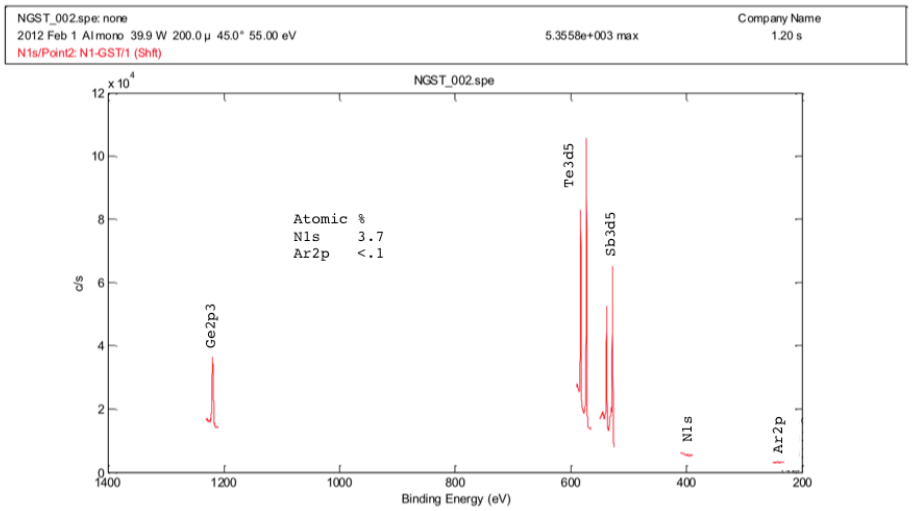


Fig. 4.1. Schematic diagram of a PCRAM cell with NGST.

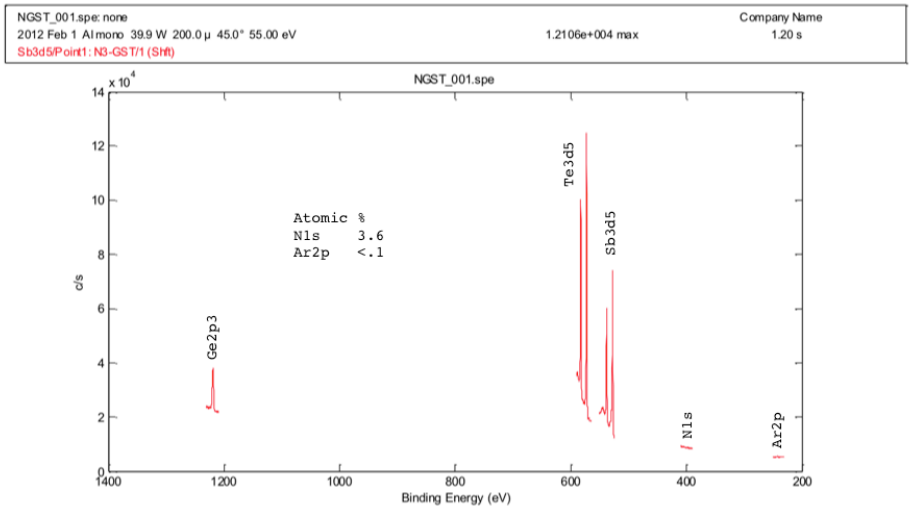
PCRAM cell sizes. The pore was filled with 40 nm of NGST. Finally, a 200 nm thick TiW top electrode was deposited and patterned to complete the structure.

NGST with grain-sizes of 5 nm and 9 nm were employed to study the effect of grain-size on the switching speed of PCRAMs. NGST films with 5 and 9 nm grain-sizes were deposited using DC magnetron sputtering of a composite $Ge_2Sb_2Te_5$ target and flowing N_2 gas concurrently in a Balzers Cube sputtering system, via a reactive sputtering process. The nitrogen concentration in the films was kept consistent by using a constant N_2/Ar gas flow rate of 0.2. The nitrogen and argon flow rates were 3 and 15 SCCM, respectively. The NGST films with grain-sizes of 5 and 9 nm were characterized using X-ray photoelectron spectroscopy (XPS), and the nitrogen concentration in both the films was found to be almost the same at around 3.5 at%. The XPS data for the NGST films with 5 and 9 nm grain-sizes also showed their compositions to be identical within experimental error (Fig. 4.2).

The sputtering power was varied to obtain NGST films with different grain-sizes. The grain-size was found to be smaller when a lower sputtering power was



(a)



(b)

Fig. 4.1. X-ray photoelectron spectroscopy of the Ge $2p_3$, Sb $3d_5$, Te $3d_5$, N $1s$, and Ar $2p$ spectra for NGST films with grain-sizes of (a) 5 nm and (b) 9 nm, respectively.

used. NGST films with a 5 nm grain-size were obtained when a sputtering power of 0.1 kW was used, while films with a 9 nm grain -size were obtained with a sputtering power of 0.3 kW. The pressure was kept constant at around 10^{-7} mbar. TEM was employed to characterize the average grain-size of the NGST films. The

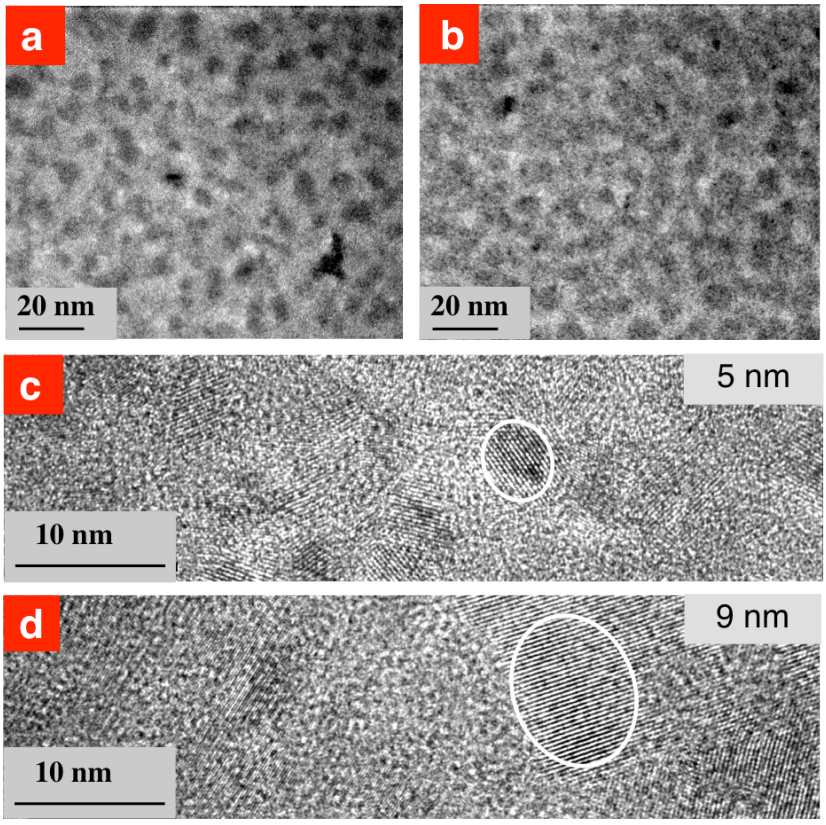


Fig. 4.3. TEM images of the as-deposited amorphous NGST films obtained with a sputtering power of (a) 0.1 and (b) 0.3 kW, and the annealed crystalline NGST films with grain-sizes of (c) 5 and (d) 9 nm.

NGST films were characterized in their amorphous and crystalline phases, as shown in the TEM images in Figs. 4.3 a) and b), and Figs. 4.3 c) and d), respectively.

4.2.2 Electrical Characterization

The PCRAM performance was investigated using an in-house PCRAM testing system (see Appendix A). To study the switching speed of the PCRAM cells, electrical pulses with durations of several 100 ps to several 10 ns, and voltages from 0 to 7 V, were applied from the pulse generator to the PCRAM cells. The

waveform of the pulse was measured just before the PCRAM cell, and the full-width half-maximum (FWHM) time duration of the waveform was used to characterize the switching speed of the PCRAM cells (see Appendix A).

4.3 Device Performance

4.3.1 Grain and Cell Size-Dependent Phase-Change Speed

The PC speeds of PCRAM cells with different grain and cell sizes were examined by finding the shortest electrical pulse required for switching the cells from the crystalline state to the amorphous state (Reset), and from the amorphous state to the crystalline state (Set), respectively (see Figs. 4.4). The cells were switched reversibly between 10 kΩ and 300 kΩ with constant Reset and Set voltages of 5 V and 1 V, respectively. Over the entire cell-size range from 200 nm down to 25 nm, the PC speed becomes faster as the cell-size is reduced. For a given cell-size, the cells with a grain-size of 5 nm have faster PC speeds than those with a grain-size of 9 nm. The larger cells, in the range of 100-200 nm, require pulse-widths of a few ns to Reset, and several tens of ns to Set. Moving to the smaller cells, in the range of 25-100 nm, much shorter pulses were needed for both Reset and Set. The grain-size effect on the PC speed is different in these two cell-size regions. In the 100-200 nm range, although the PC speed is dependent on the grain-size, the speed difference between the 5 nm and 9 nm grain-sizes is almost constant. However, in the 25-100 nm range, not only the PC speeds, but also the speed differences between the two grain-sizes increase significantly as the cell-size decreases. Cells with 5 nm grains require much shorter pulses to switch, as

compared to cells with 9 nm grains, when the cell-size is reduced. This is more clearly observed for the Set process, which determines the speed of PCRAM. The speed increase for a grain-size reduction from 9 nm to 5 nm, at a cell-size of 200 nm, is only about 3 %. In contrast, the increase at a cell-size of 25 nm is as high as 400 %.

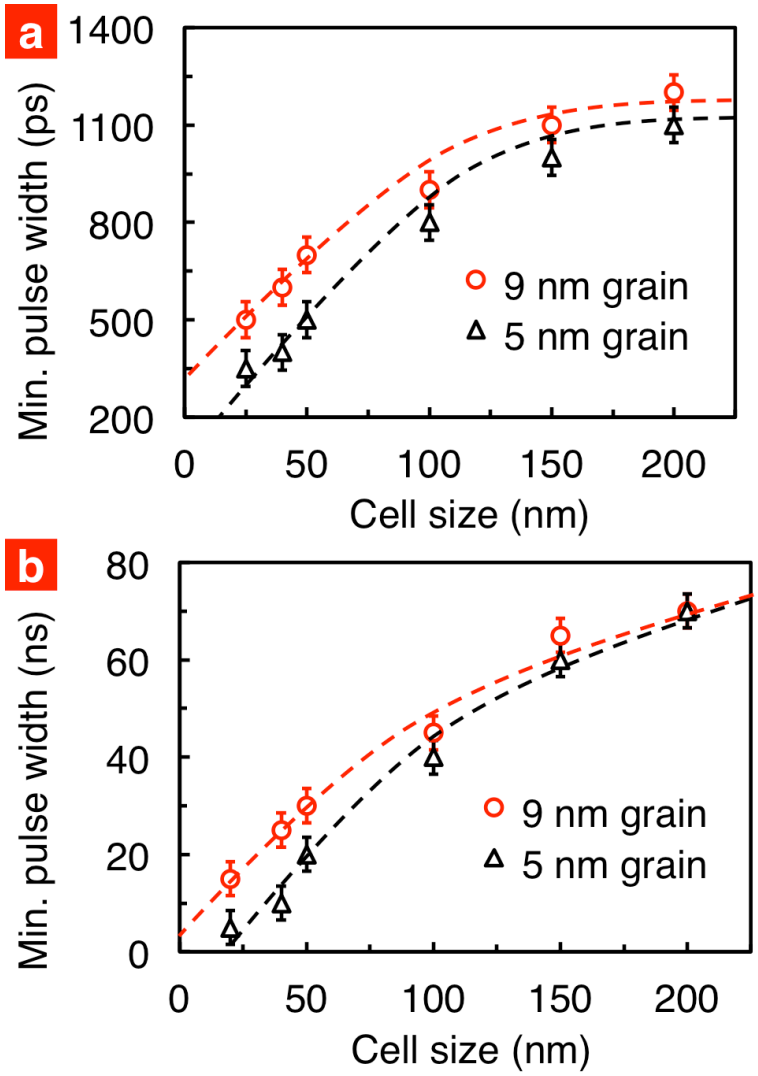


Fig. 4.4. Correlation between the minimum pulse-width achieved and cell-size for (a) Reset and (b) Set. As the cell-size decreases, the cells with a grain-size of 5 nm can be switched with much shorter pulse-widths compared to the cells with a grain-size of 9 nm, with a reduction of up to 400 %.

4.3.2 Correlation between Voltage and Pulse-Width

Figure 4.5 shows the dependence of the switching voltage on the pulse width achieved to Reset and Set the PCRAM cells with grain and cell sizes of 5 nm and 25 nm, respectively. As the pulse width decreases, the minimum voltage required to switch the cell increases. The shortest Reset and Set pulses achieved were 350 ps and 3 ns, respectively.

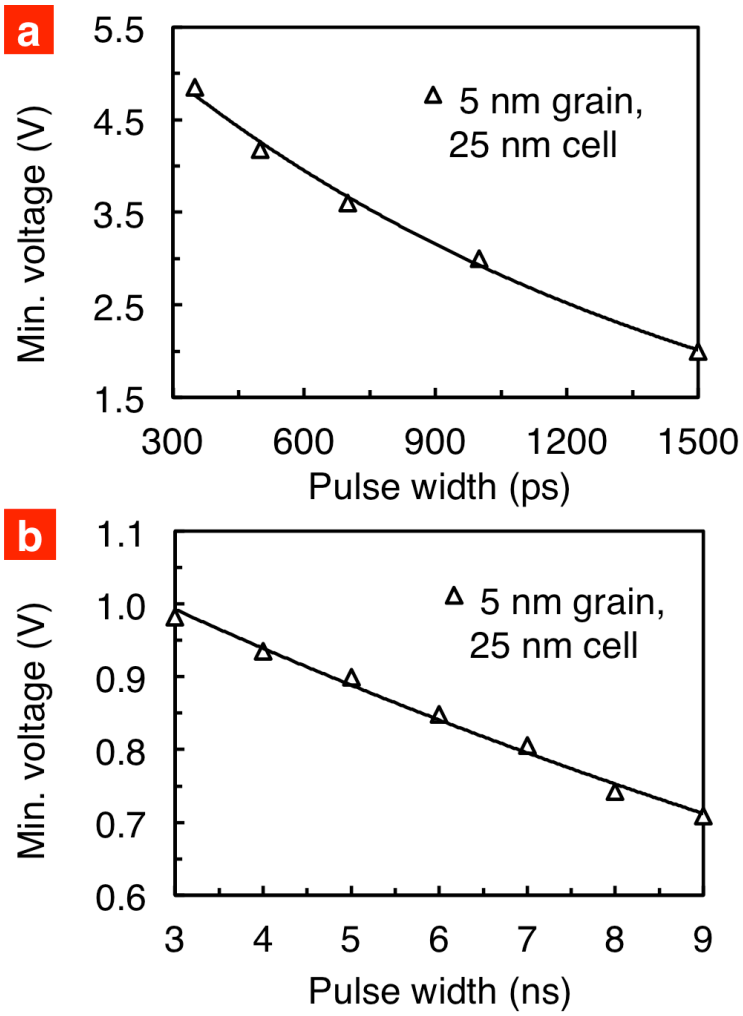


Fig. 4.5. Dependence of the minimum voltage on pulse-width required to (a) Reset and (b) Set a 25 nm cell with a 5 nm grain-size. The shortest pulse widths achieved were 350 ps and 3 ns for Reset and Set, respectively.

4.3.3 Cycling Endurance

The endurance of PCRAM under fast switching conditions was studied for a cell with grain/cell sizes of 5/25 nm, respectively (see Fig. 4.6). The cells can be switched reversibly and stably for 10^8 cycles using Reset and Set pulses as short as 6 ns and 9 ns, respectively. To the best of our knowledge, this is the first time that 10^8 cycles has been achieved with Set and Reset pulses shorter than 10 ns, which is at the level of DRAM speed. This demonstrates that PCRAM can achieve both fast speed and high stability at the same time, by reducing both the cell and grain sizes simultaneously.

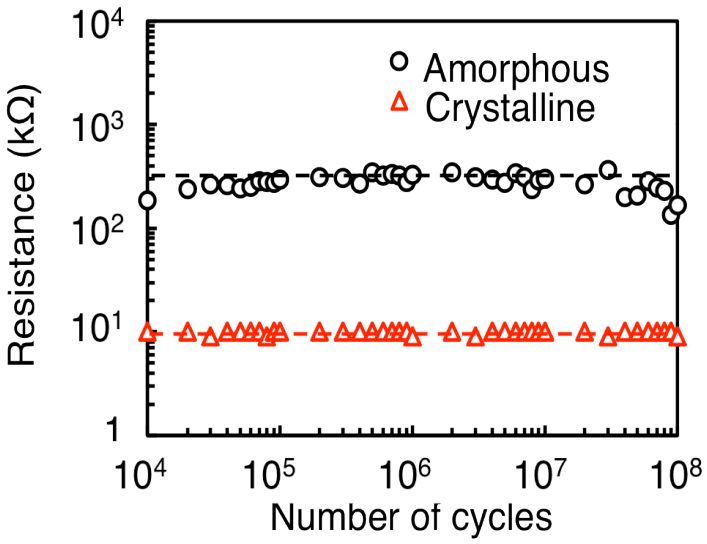


Fig. 4.6. Cycling endurance of a cell with grain and cell sizes of 5 nm and 25 nm, respectively. Stable and reversible switching for 10^8 cycles was achieved with short Reset and Set pulses of 6 ns and 9 ns, respectively. This demonstrates that both high speed and high stability can be achieved at the same time.

4.4 Theoretical Study of Interplay between Grain and Cell Sizes

4.4.1 Numerical Calculations

In a PCRAM cell, a reduction in the cell-size limits the number of grains and increases the ratio of interface areas to volumes. As shown in Fig. 4.7, the NGST material in a nanocell has two types of interfaces: a) the cell-interface (CI), which exists between dissimilar materials, and b) the grain-interface (GI), which separates differently oriented grains of the same material. The CI has a higher interface-area-to-volume ratio when the cell-size is smaller. NGST has many grains and grain boundaries, and the boundary between the adjacent grains forms the GI. The interplay between the two interfaces (CI and GI) at the nanoscale can be studied from the perspective of grains in the material-interface system. When the diameter of the cell is reduced, there will be a larger decrease in the number of grains in the inner cores (interior grain) compared to that at the CI (exterior grain).

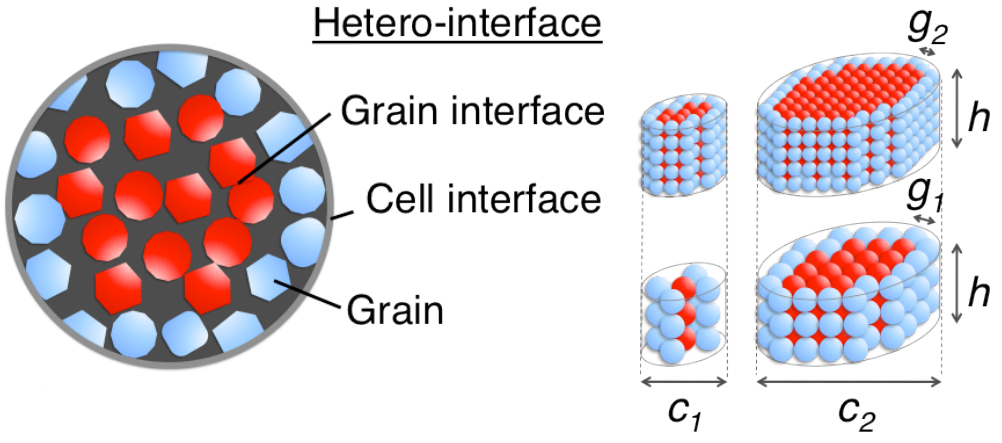


Fig. 4.7. Schematic diagram showing the higher interface-area-to-volume ratio of cells when both the grain and cell sizes decrease.

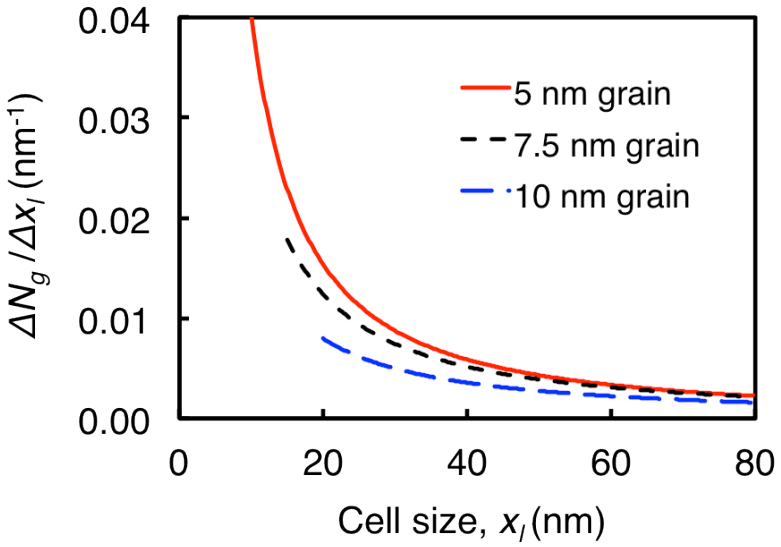


Fig. 4.8. Numerical calculations show that the ratio $\Delta N_g/\Delta x$ increases when both the grain and cell sizes reduce. As the cell-size falls below 40 nm, the increase in $\Delta N_g/\Delta x$ was observed to be faster for the cells with smaller grain-sizes.

To investigate the change in PC mechanism, a numerical study was conducted on the change in the effective contact-area-to-volume ratio of the PC material with decreasing cell-size. The relative change in the fraction of exterior grain (ΔN_g) with respect to the change in material size (Δx) at different grain and material sizes was studied. To simplify the calculations, the grains of the PC material were assumed to be identical and spherical in shape. They were packed to form cylindrical shapes with varying lateral and vertical material-sizes, both from 10 to 90 nm. Various grain-sizes from 5 to 10 nm were studied. From these numerical calculations, it can be seen that the ratio $\Delta N_g/\Delta_x$ is small when either or both the grain and cell sizes are large (see Fig. 4.8). As both grain and cell sizes become smaller, the value of $\Delta N_g/\Delta x$ increases sharply. The difference in $\Delta N_g/\Delta x$ for NGST with various grain-sizes becomes larger as the cell-size decreases, meaning that the overall interfacial boundary area increases significantly.

4.4.2 Finite-Element Simulation

Thermal simulations, using the ANSYS software (see Appendix C), were carried out to study the temperature distribution in PCRAM cells with varying cell and grain-sizes during Reset. Figure 4.9 shows the simulated temperature distribution in the PCRAM cells after activation by a constant voltage pulse (30 ns, 0.8 V) (also see Appendix C for material parameters). In the simulation, the grains of the PC material were assumed to be identical and closely packed. Grains of 5 and 9 nm were represented by 5×5 and 9×9 nm squares, respectively. Cell-sizes of 30 and 150 nm were employed. The thermal conductivity of the grain boundary was

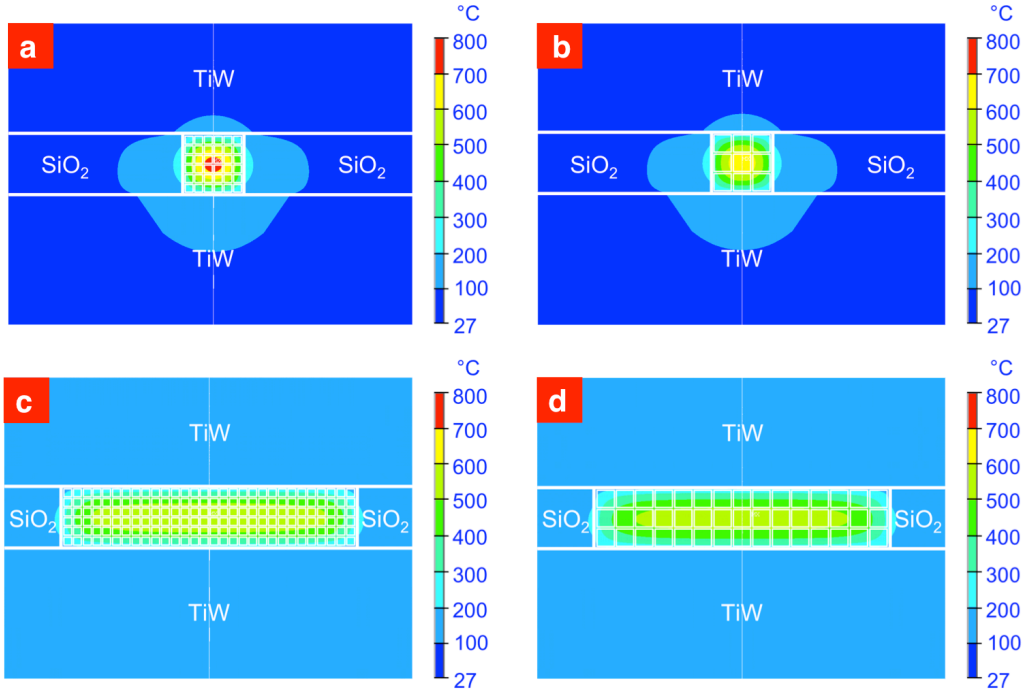


Fig. 4.9. Simulated temperature distributions in a (a) 30 nm cell with 5 nm grains, (b) 30 nm cell with 10 nm grains, (c) 150 nm cell with 5 nm grains, and (d) 150 nm cell with 10 nm grains. The thermal conductivity of the grain boundary was assumed to be two times lower than that of the grains of the phase-change material.

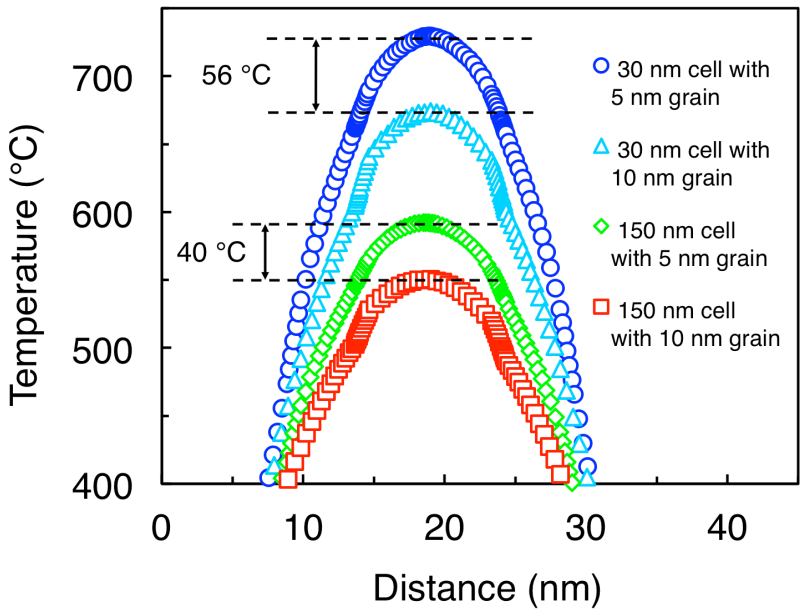


Fig. 4.10. Calculated temperature profiles of PCRAM cells after constant voltage pulse activation. A higher peak temperature is observed in the cells with smaller grain and cell sizes.

assumed to be 2 times lower than that of the grain, considering the relative thermal conductivity of nitride compounds at the grain boundary compared to that of the bulk PC material [4.10-4.12].

From the calculations, the peak temperature is observed to increase as the cell-size decreases, as shown in Fig. 4.10. A further increase in the peak temperature was achieved as the grain-size decreases. Such observations indicate sharp changes in the thermal properties of the PCRAM cells, which can be related to a change in the PC mechanism.

4.5 Mechanism Discussion

4.5.1 Electronic Switching Effect

It is of interest to study why higher crystallization speeds can be achieved in a PC material with an intrinsically stable amorphous phase, through the scaling of the cell and grain sizes. Generally, the fractions of CI and GI will increase when the cell-size decreases. For an NGST cell with a smaller grain-size, the fractions of CI and GI will increase more sharply when the cell-size is reduced, resulting in a much higher effective contact-area-to-volume ratio. It is known that imperfections exist at interfaces [4.13,4.14]. At both CIs and GIs, such imperfections can include broken or loosely bonded atomic structures. The electrons in the atomic structures can be excited and become free electrons when energy is supplied. Free electrons can also be generated via impact ionization [4.15,4.16]. In a typical process, whereby an electrical pulse is applied to a PCRAM cell, there is a probability of electrons being excited to the high energy conduction bands. This initiates a series of impact ionization processes, and generates a high concentration of free electrons to switch the material [4.17,4.18]. At the same time, a large number of ions will be left in the material. These ions can be distorted from their original equilibrium positions due to the strong repulsive Coulomb force between them [4.19,4.20]. This pronounced displacement of ions can induce a permanent structural change [4.21]. Since materials with both smaller grain and cell sizes have a larger fraction of interface areas, a higher concentration of free electrons can be generated, which can in turn induce more pronounced displacement of ions, resulting in a rapid change in the atomic structure [4.22].

4.5.2 Crystallization Theory

Based on classical crystallization theory, the crystallization of small dimensional materials can be classified as either nucleation-dominated or growth-dominated, according to the relative contribution of nucleation and growth [4.23-4.25]. In a nucleation-dominated material, crystallization occurs mainly via the nucleation of crystallites. For a growth-dominated material, crystallization occurs mainly by nuclei-growth. NGST is known to be a nucleation-dominated material. Usually, heterogeneous nucleation rates are observed to be far higher than the homogeneous nucleation rates [4.26,4.27], due to the smaller activation energy at the interface. Figures 4.11 and 4.12 show that in a PCRAM cell, hetero-crystallization, which includes the hetero-nucleation and subsequent growth at the boundary between the PC material and other materials, and the interfacial-growth at the crystalline (*c)*- and amorphous (*a)*- interface of a PC material, occurs in addition to the homogeneous nucleation and nuclei growth:

$$I^{homo\text{-}nucl.} + I^{growth} + H^{interfacial\text{-}growth} + H^{hetero\text{-}nucl.\text{-}growth} \quad , \qquad (4.1)$$

where $I^{homo\text{-}nucl.}$ is the inherent homogenous nucleation, I^{growth} is the inherent nuclei growth, $H^{interfacial\text{-}growth}$ is the interfacial-growth at the *c*- and *a*- interfaces of the PC material, and $H^{hetero\text{-}nucl.\text{-}growth}$ is the heterogeneous nucleation and subsequent growth at the boundary between the PC material and another material, as well as at the grain boundaries. With a decrease in the cell and grain sizes, the

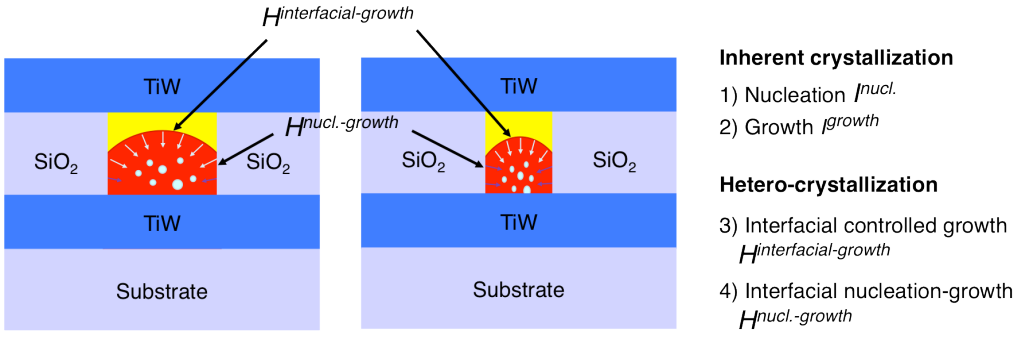


Fig. 4.11. Schematic diagram of the phase-change mechanisms in a PCRAM cell that contribute to the phase-switching process for different cell-sizes.

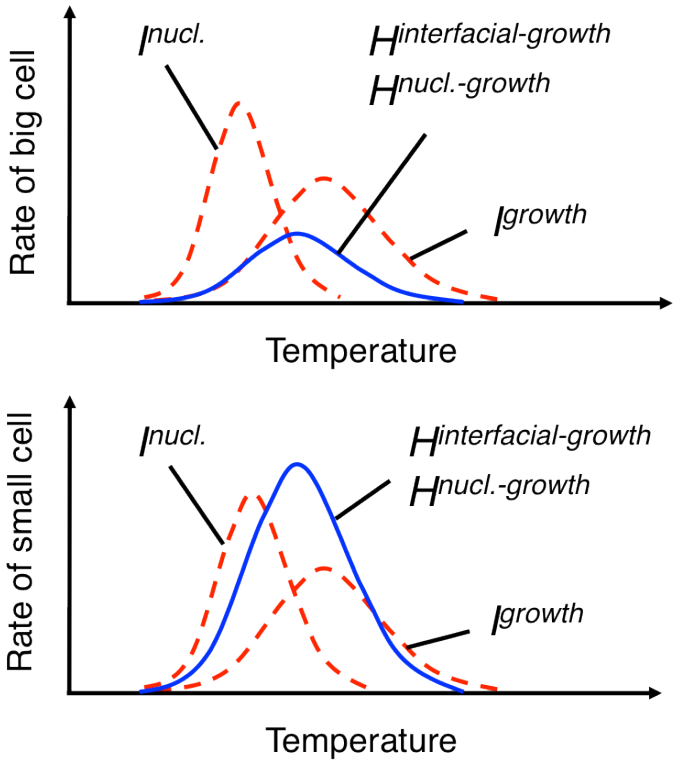


Fig. 4.12. Schematic diagrams showing the change in phase-change mechanism. As the cell-size decreases, the mechanism changes from being nucleation-dominated to being a growth-dominated crystallization process.

hetero-crystallization rate (3rd and 4th terms in Eq. 1) will increase dramatically, and become the dominant mechanism.

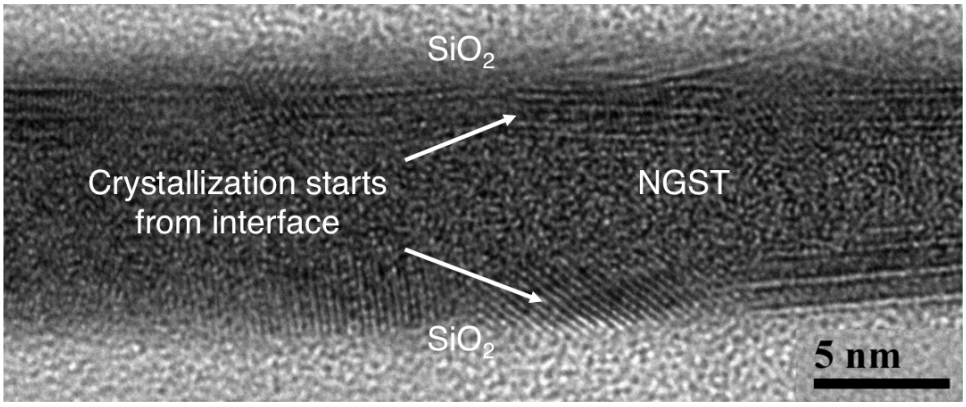
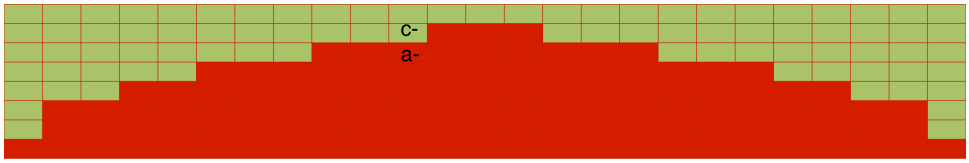


Fig. 4.13. TEM characterization of an NGST film deposited on SiO_2-on Si, and capped with sputtered SiO_2. The NGST films were annealed at 280 °C for 3 min. The crystallization starts from the interface, and the grains have different crystalline fringe orientations.

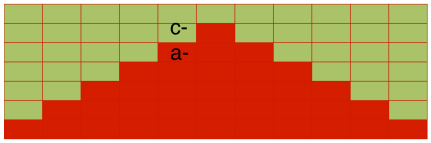
In order to validate this mechanism, a TEM study was conducted. The TEM characterization image in Fig. 4.13 shows the crystallization of an NGST film. It can be clearly seen that the crystallization occurs mostly at the interface, and the grains have different crystalline fringe orientations.

4.5.3 Periodic Bond Chain Theory

The Periodic Bond Chain (PBC) theory is often used to predict the morphology of crystals [4.28]. According to this theory, the crystal morphology is controlled by a set of uninterrupted chains of strong bonds formed in the crystal lattice. The formation of a crystal is dominated by the relative growth rate of the various faces, which is proportional to the attachment energy. By calculating the attachment energy, the morphology of a crystal can be derived. The attachment energy is defined as the energy released per mole when a new layer is deposited on a crystal face.



(a) Large radius of curvature



(b) Small radius of curvature

Fig. 4.14. Illustration showing the effect of PBC on the radius of curvature in a single crystal. Dependence of the number of strong bonds on the interface curvature with (a) a larger radius of curvature, and (b) a smaller radius of curvature.

In this study, the relationship between the statistical number of strong bonds and the radius of curvature of the boundary between the amorphous and crystalline phases is considered. Figure 4.14 shows that the statistical number of strong bonds increases as the radius of curvature becomes smaller. Since the relative growth rate is proportional to the number of strong bonds, the growth rate will increase. In a PCRAM cell, the radius of curvature of the boundary between the *a*- and *c*-phases becomes smaller as the cell-size reduces. A smaller radius of curvature will increase the statistical number of strong bonds, therefore facilitating the interfacial-growth $H^{interfacial\text{-}growth}$ at the *c*- and *a*- interface.

4.5.4 Size-Dependent Crystallization Effects

The effect of grain-size on PC speed can be understood by a combined view of thermal, crystallization, and electrical effects. To study these effects, the dependence of the resistance on the annealing temperature of NGST films was

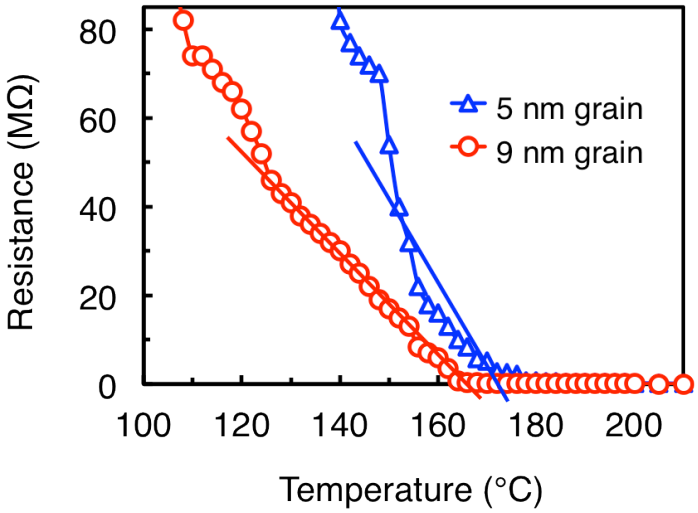


Fig. 4.15. Dependence of the resistance on the annealing temperature of NGST films. A sharper fall in resistance at higher temperatures is observed for NGST films with 5 nm grains compared to that of NGST films with 9 nm grains.

investigated (see Fig. 4.15). An in-house film-resistance measurement system was used to measure the resistance of NGST films during annealing. The annealing temperature was varied from 100 to 300 °C. A sharper fall in the resistance at higher temperatures is observed for NGST films with 5 nm grains compared to that of NGST films with 9 nm grains. This indicates that the smaller grain-size films have a higher "switch-on" temperature, but a faster growth rate.

The crystallization behavior of PC materials upon 1- to 3-dimensional scaling has been well studied [4.1-4.4]. The effect of scaling on the crystallization process was studied at the device level. The size-dependent crystallization temperature of PCRAM cells was investigated, as shown in Fig. 4.16. The crystallization temperature was determined by observing the onset of the resistance drop from the Reset state to the Set state. It can be observed that the crystallization temperature decreases with the cell-size, which facilitates faster crystallization. It should be noted that the scaling effect on the crystallization behavior in

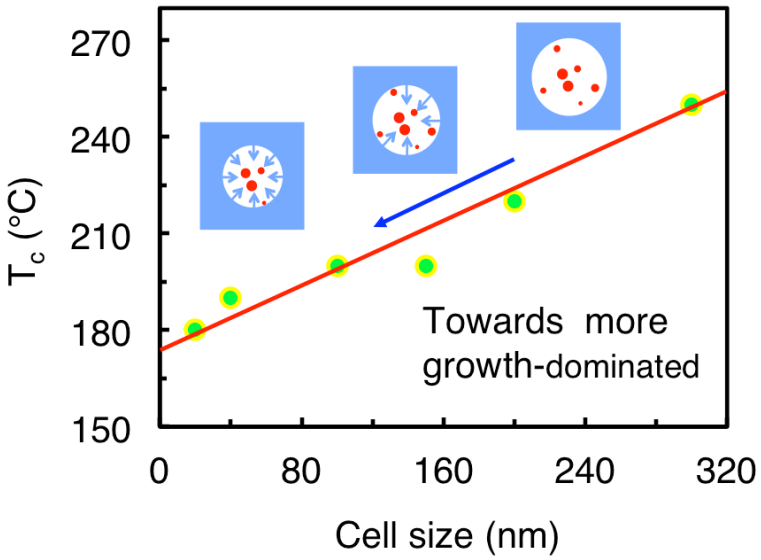


Fig. 4.16. Cell-size-dependent crystallization temperature of PCRAM. The crystallization temperature becomes lower as the cell-size is decreased.

2-dimensions (film thickness) is different to that in 3-dimensions (PC nanoparticles/nanostructures). In 2-dimensions, the crystallization temperature of the PC material increases as the thickness decreases [4.2,4.3]. In contrast, in 3-dimensions, the crystallization temperature of the PC material decreases as the diameter decreases [4.4]. This could be due to the fact that heterogeneous nucleation occurs easily at non-uniform interfaces, but with difficulty at flat interfaces [4.29].

4.5.5 Size-Dependent Amorphization Effect

In the amorphization process, the time needed to form the amorphous area is proportional to the cell-size. This effect was studied by simulating the size of the heating zone upon pulse activation using finite element methods (see Appendix C), as shown in Fig. 4.17. Reset pulses with varying durations (10-30 ns) were

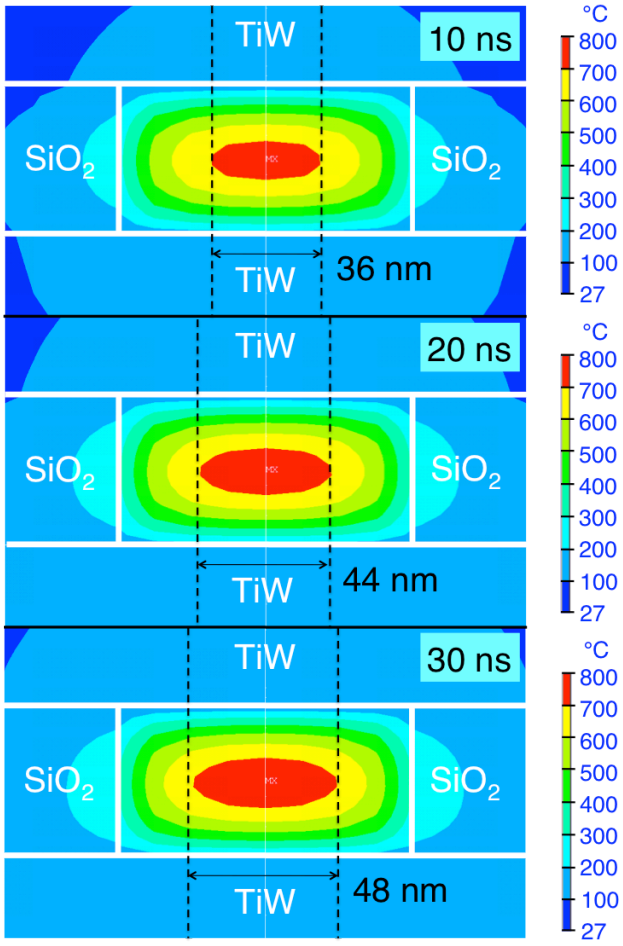


Fig. 4.17. Simulated temperature profiles of PCRAM on the time-scale of several tens of ns. A shorter time was needed to phase-change a smaller active region.

applied to the cells (also see Appendix C for material parameters). The voltage was kept constant at 1.0 V. It is observed the heating zone becomes smaller as the pulse duration decreases. For complete amorphization to occur, the cell-size should be equal to or smaller than the heating zone. This means that if a smaller cell is used, it can be completely amorphized with a shorter pulse. This effect is consistent with what is observed in the experiments. Therefore, by reducing the cell-size, the amorphization speed will be increased.

4.5.6 Grain-Size Distribution

It should be noted that the statistical grain-size distribution is expected not to undergo significant changes during a read/write process. This is mainly due to the fact that the PC material in a PCRAM cell can be switched without going through the classical melting process [4.30,4.31]. In a related report [4.30], Kolobov and co-workers have provided an explanation as to why the switching in $Ge_2Sb_2Te_5$ is fast and stable. This is because the crystallization-amorphization process may not necessarily require the rupture of strong covalent bonds. The Te sublattice can be partially preserved, as well as the local structure around the Sb atoms, and this is a possible reason as to why the transformation is fast and reversible. The material does not have to be transformed into a truly liquid state, and bond rupture is postulated to be due to electronic excitation. Also, the amorphous structure, at the local level, can be well defined, enhancing the reversibility of the transition. These indicate that PCRAM can be switched without undergoing a classical melting process. Also, the effects of nitrogen-doping in PC optical media have been well studied and accepted [4.1]. In NGST, nitrogen atoms are preferentially bound to Ge in both amorphous and crystalline GST [4.3,4.32,4.33]. As the amount of incorporated nitrogen atoms increases, excess nitrogen atoms can segregate to the grain boundaries in the form of nitrides [4.3]. These nitrides are known to inhibit crystal growth, and hence maintain a large number of grain boundaries. During the write process, the GST microcrystal grains melt at around 600 °C. However, the interfacial nitrides remain in the solid phase because their melting temperature is much higher than that of GST. It is also observed that the

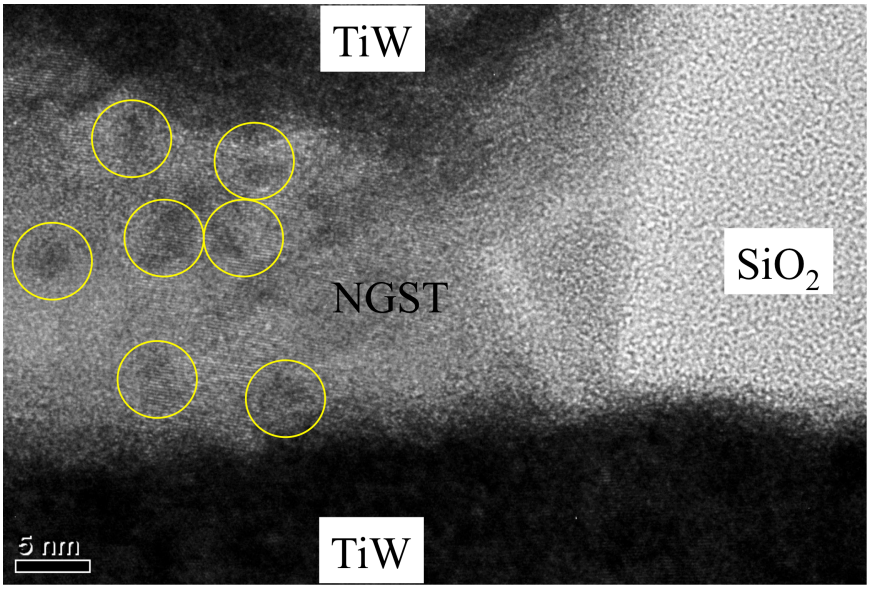


Fig. 4.18. TEM image of a PCRAM cell with a grain size of 5 nm that had been switched for 5000 cycles. The grain-size of the NGST in the cell is observed to be around 5 nm, showing that the grain-size remains practically unchanged after cycling.

grain-size is practically unchanged after the PCRAM cell had been switched for 5000 cycles (see Fig. 4.18). This is the main reason why the overwriting cycle of a PC optical disk can be increased from 10^4 to 10^6 by doping nitrogen into GST [4.1]. The duration of the programming pulses used in this work is less than 10 ns, which is much shorter than that used in the optical disk. Thus, it can be inferred that the grain-size distribution in this work would be even better preserved than in an optical disk. This has been indirectly confirmed by the overwriting of a PCRAM cell for 10^8 cycles (see Fig. 4.5).

4.6 Solutions to Making a Universal Memory

Based on these results, a possible approach to achieving a universal memory is proposed as follows: 1. Select a PC material with good stability and endurance; 2. Reduce the cell-size to achieve fast speed and high endurance at the same time; 3. Further increase the speed by reducing the grain-size, which also facilitates the filling of nanoscale pores in the fabrication of the PCRAM; 4. In addition, if the manufacturing issues with developing I-shape PCRAM with excellent thermal confinement can be overcome, even lower operating powers can be expected.

4.7 Conclusion

In conclusion, the change in the PC mechanism with scaling has enabled us to overcome the fundamental limitations that arise from the trade-off between the speed and stability properties of PC materials. As the cell-size is reduced, hetero-crystallization, which includes the interfacial-growth at the phase boundary between the crystalline and amorphous phases, and the heterogenous nucleation and subsequent growth at the boundary between the PC material and another material, will become the dominant PC mechanism, regardless of the type of PC material. Futhermore, higher speeds are achieved as the grain-size decreases. These findings allow us to utilize PC materials with a good stability to achieve both fast PC speed and high endurance simultaneously. A feasible solution is thus proposed to achieve a universal memory.

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Chapter 5

Ultrafast-Speed and Low-Power Switching in Nanoscale Phase-Change Materials with Superlattice-like Structures

In the preceding two chapters, fast speed and high endurance switching were achieved in PCRAM. Furthermore, the material physics and mechanisms behind these effects were elucidated through experiments and simulations. For PCRAM to become a universal memory, it needs not only a fast switching speed, but also a low-power consumption. It is thus important to study how fast speed, as well as low-power consumption, can be achieved in PCRAM.

It is the aim of this chapter to study nanoscale PC materials with superlattice-like (SLL) structures, in a bid to achieve fast switching speed while maintaining low-power consumption in PCRAM cells. In this study, the correlation between the size, switching speed, and voltage of PCRAM cells with SLL structures is investigated. The crystallization, thermal conductivity, and resistivity effects in the SLL structures are also studied. These findings will open up new possibilities for fast-speed and low-power PCRAM devices.

5.1 Concept and Theory

An effective approach to achieving fast switching speed and low operating power is to reduce both the size of the PCRAM cell and employ PC materials with a low

thermal conductivity and a high crystallization temperature. In a PCRAM cell, the size of the active device region plays an important role by defining the volume of the PC material involved in the phase transformation. On the other hand, the thermal conductivity and crystallization temperature of the PC material influence the thermal confinement and data retention properties of PCRAM. Despite their importance, few studies have been performed to investigate the effects of both device scaling and material modifications on the switching speed and power consumption of PCRAM. Only fast switching of sub-100 nm $Ge_2Sb_2Te_5$ (GST) and GeTe PCRAM cells in several nanoseconds has been demonstrated [5.1,5.2].

Nanostructured materials have switching properties that are significantly different from the bulk materials. In a PCRAM cell, higher heterogeneous crystallization rates can be achieved in nanostructured PC materials due to their high surface-area-to-volume ratios [5.3]. Nanoscale active device regions or volumes of PC materials can also have lower phase-transition temperatures than bulk materials due to greater phonon softening effects [5.4-5.6]. Materials with superlattice-like (SLL) structures have lower thermal conductivities than bulk materials with the same composition [5.7]. They have good thermal confinement properties due to phonon-scattering effects at the interfaces [5.8]. PC materials with SLL structures can be formed from alternating layers of Sb_2Te_3 and GeTe, which have fast switching speed and good data retention [5.7,5.9], respectively, as shown in Fig. 2.1. Considered collectively, a PCRAM cell with both a smaller active device region and a SLL Sb_2Te_3/GeTe structure may have a faster switching speed and a lower operating power than a cell with a larger active device region or one

with pure GST. In this study, the interplay between the switching speed, operating voltage and cell-size of PCRAM cells with SLL structure was investigated.

5.2 Methodology

Pore-like PCRAM cells with the SLL structure outlined above were fabricated to investigate their electrical performances, as shown in Fig. 5.1. For comparison, PCRAM cells comprising only GST were also fabricated. SiO_2-on-Si substrates were used as the starting materials, on which 200 nm of TiW as the bottom electrode was formed. An insulating layer (30 nm) comprised of SiO_2 was subsequently deposited. To study the size-dependent switching speed and operating power of the PCRAM cells, pores with diameters (cell size) ranging from 40 nm to 400 nm were formed in the insulating layer. The pores were filled with 35 nm of GST, or the SLL material. The SLL structure was formed by depositing alternating layers of GeTe and Sb_2Te_3, with the mole ratio of GeTe and Sb_2Te_3 at 2:1, which has the same overall composition as $Ge_2Sb_2Te_5$. Five periods were deposited, each comprised of a layer of GeTe (3 nm) and a layer of Sb_2Te_3 (4 nm). Finally, a TiW top electrode (200 nm) was deposited and patterned to complete the PCRAM cell structure.

The electrical properties of the cells were studied using an in-house testing system (see Appendix A). Voltages and pulse widths ranging from 0-7 V and 100 ps-100 ns were employed, respectively. The cells were switched reversibly between 10 kΩ to around 300 kΩ.

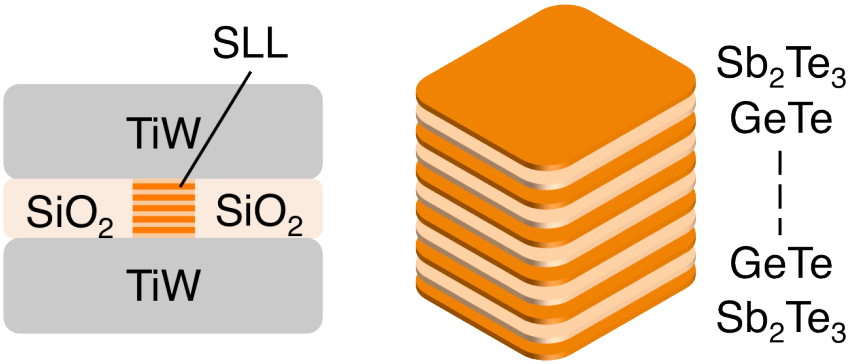

Fig. 5.1. Schematic diagram of a PCRAM cell with SLL structures. The SLL structure is formed from alternate nano-layers of Sb_2Te_3 and GeTe.

5.3 Device Performance

5.3.1 Size-Dependent Phase-Change Speed

The size-dependent switching speed of the SLL and GST cells was studied by investigating the shortest pulse-width required to switch the cells from the crystalline state to the amorphous state (Reset), and from the amorphous state to the crystalline state (Set) (see Fig. 5.2). Constant Reset and Set voltages of 5 V and 1 V were employed, respectively.

In this study, shorter Reset and Set pulse-widths were achieved as the cell-size of the SLL cells was decreased. At large cell-sizes, from around 400 to 150 nm, gradual reductions of the pulse-widths by around 300 ps and 20 ns were observed for Reset and Set, respectively. A sharper decrease in the pulse-widths was observed as the cell-size decreases. Despite a smaller reduction in the cell-sizes from 150 to 40 nm, larger decreases of the pulse-widths by 600 ps and 40 ns were achieved for Reset and Set, respectively. This can be attributed to the emergence of nanosize effects. The shortest Reset and Set pulse-widths achieved were 300 ps and

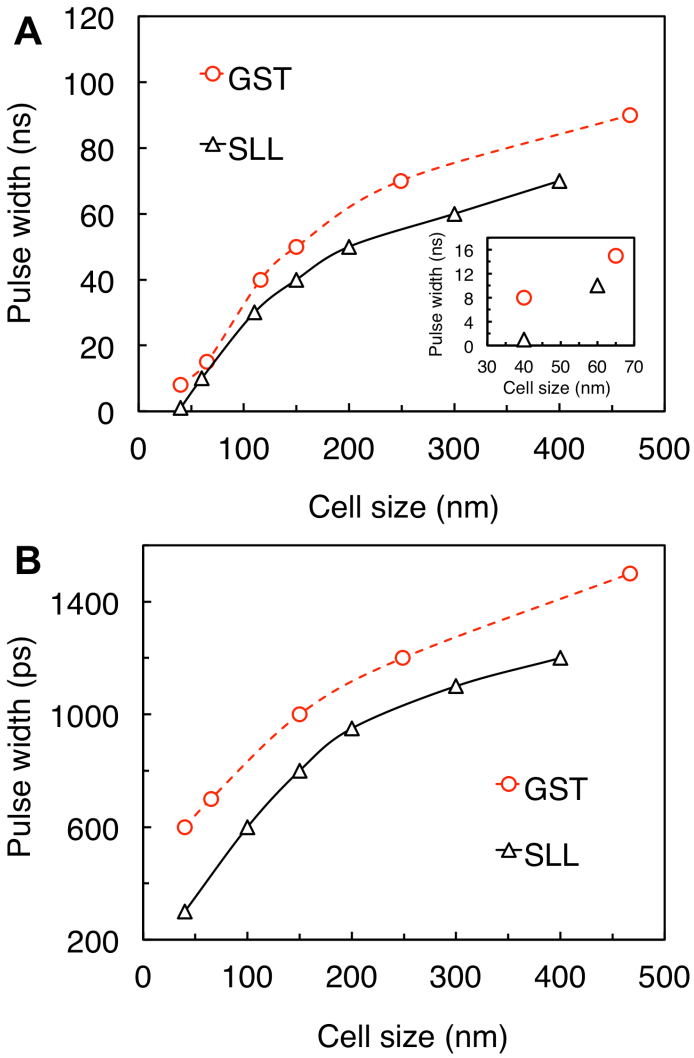

Fig. 5.2. Size-dependent switching speeds of the SLL and GST cells. Both the SLL and GST cells were found to require significantly shorter pulse-widths to (a) Reset and (b) Set as the cell sizes were reduced. Shorter pulse-widths were required to switch the SLL cells than to switch the GST cells. The shortest Reset and Set pulse-widths achieved were 300 ps and 1 ns, respectively, which were achieved in the 40 nm SLL cells.

1 ns, respectively. These were observed in the 40 nm SLL cell. For the GST cells, similar trends were also observed. SLL cells were found to require shorter pulse-widths than the GST cells. The difference between the Reset pulse-widths required to switch the SLL and GST cells was about 200 ps, and was relatively consistent for the range of cell-sizes studied. In contrast, a smaller relative difference between the

Set pulse-widths of the SLL and GST cells was observed as the cell-size was reduced. The difference was about 20 ns for cell-sizes ranging from 400 to 200 nm. For cell sizes less than 100 nm, the differences were a few ns, which suggests the dominance of different mechanisms for different cell-size regions.

5.3.2 Correlation between Voltage and Pulse Width

Figure 5.3 shows the dependence of the voltage on the pulse-width applied to the SLL and GST cells. It was obtained by studying the minimum voltage required to switch the cells between 10 kΩ and 300 kΩ.

In this investigation, SLL cells with a smaller cell-size were found to have a lower operating voltage. Low Reset and Set voltages were achieved in the cells with a cell-size of 40 nm, and these were respectively about 1 V and 0.2 V lower than those achieved in cells with a cell-size of 150 nm. This was observed for Reset and Set pulse-widths ranging from 5 to 10 ns, and 100 to 200 ns, respectively. Higher voltages were observed as the Reset and Set pulse-widths decrease below 5 and 100 ns, respectively. Considering a fixed applied voltage, this could be due to insufficient energy being delivered by electrical pulses with shorter pulse-widths. A similar study was also carried out on the GST cells. Compared to the GST cells, the SLL cells can be switched with lower voltages. Differences between the Reset voltages of SLL and GST cells were as large as 1 V for pulse-widths ranging from 5 to 10 ns, and this was greater than the differences between the Set voltages of the SLL and GST cells for pulse-widths ranging from 100 to 200 ns. The lowest Reset voltage achieved in the 40 nm SLL

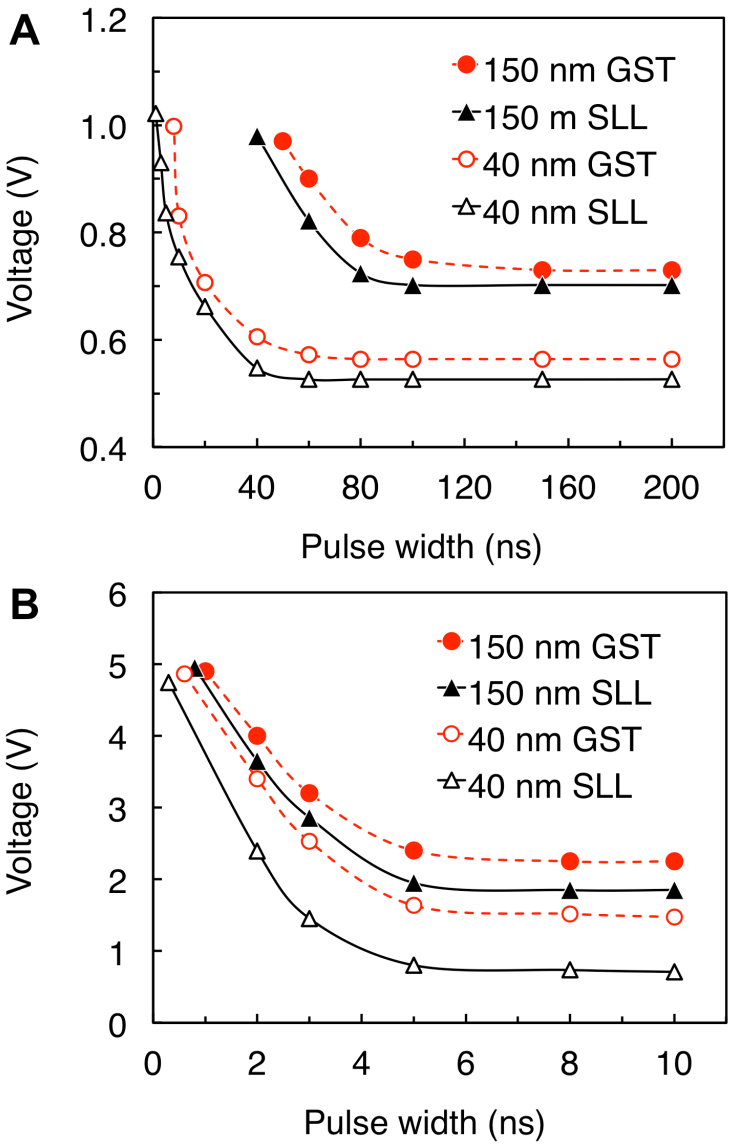

Fig. 5.3. Dependence of the switching voltage on the pulse-width applied to both the SLL and GST cells, with selected cell sizes of 40 nm and 150 nm for (a) Reset and (b) Set. 40 nm SLL cells show the best performance; they require lower operating voltages than similarly-sized GST cells.

cells was 0.9 V, much lower than the 1.6 V required for the 40 nm GST cells. Lower Set voltages were also achieved for the 40 nm SLL cells (0.5 V) compared to those obtained for the 40 nm GST cells (0.6 V).

5.3.3 Cycle Endurance

Nanoscale SLL cells are observed to have high cycle endurance, as shown in Fig. 5.4. In this study, 40 nm SLL cells were found to switch reversibly and stably for more than 10^7 cycles. The cells were switched between 10 kΩ and 300 kΩ with Reset and Set voltages of 2.5 V and 0.9 V, respectively.

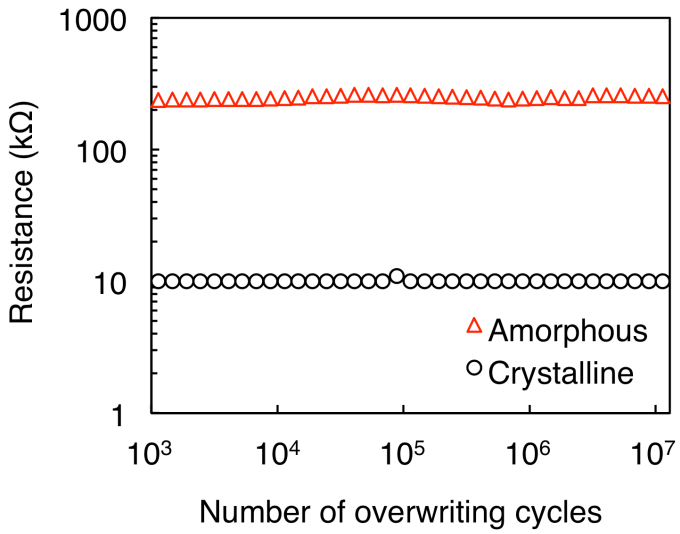

Fig. 5.4. Cycle endurance of a 40 nm SLL cell. Stable and reversible switching of the cell was observed for 10^7 overwriting cycles.

5.3.4 Stability of the Amorphous Phase

To study the data-retention properties of the SLL cells, the crystallization temperatures of the 40 nm SLL and GST cells were investigated (see Fig. 5.5). The cells were heated at different temperatures for a fixed period of time and the lowest temperature (crystallization temperature) required to switch the cells from a high resistance of several MΩ to a low resistance of several tens of kΩ was

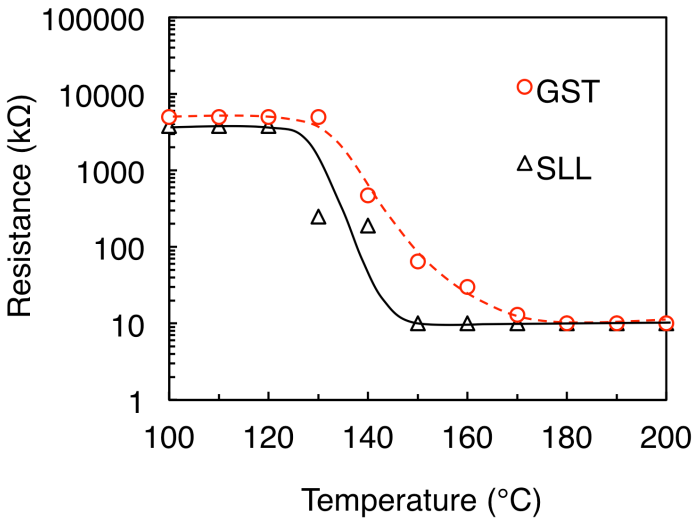

Fig. 5.5. Correlation between the cell resistance and the applied temperature for 40 nm SLL and GST cells. The cells have crystallization temperatures of 150 °C and 170 °C, respectively, which are both higher than room temperature.

recorded. The 40 nm SLL and GST cells were found to have crystallization temperatures of 150 °C and 170 °C, respectively, which were both higher than room temperature. This observation shows that small SLL cells can have both fast switching speeds and good data-retention properties at the same time.

5.4 Finite-Element Simulation

Finite-elment simulations (see Appendix C) were employed to study the temperature distributions in the SLL and GST cells. Figures 5.6 shows the simulated temperature distributions in the SLL and GST cells after constant voltage-pulse activation (30 ns, 0.5 V) for Reset (also see Appendix C for material parameters). In these simulations, the thermal conductivity of the SLL material was assumed to be 2 times lower than that of GST, considering the relative

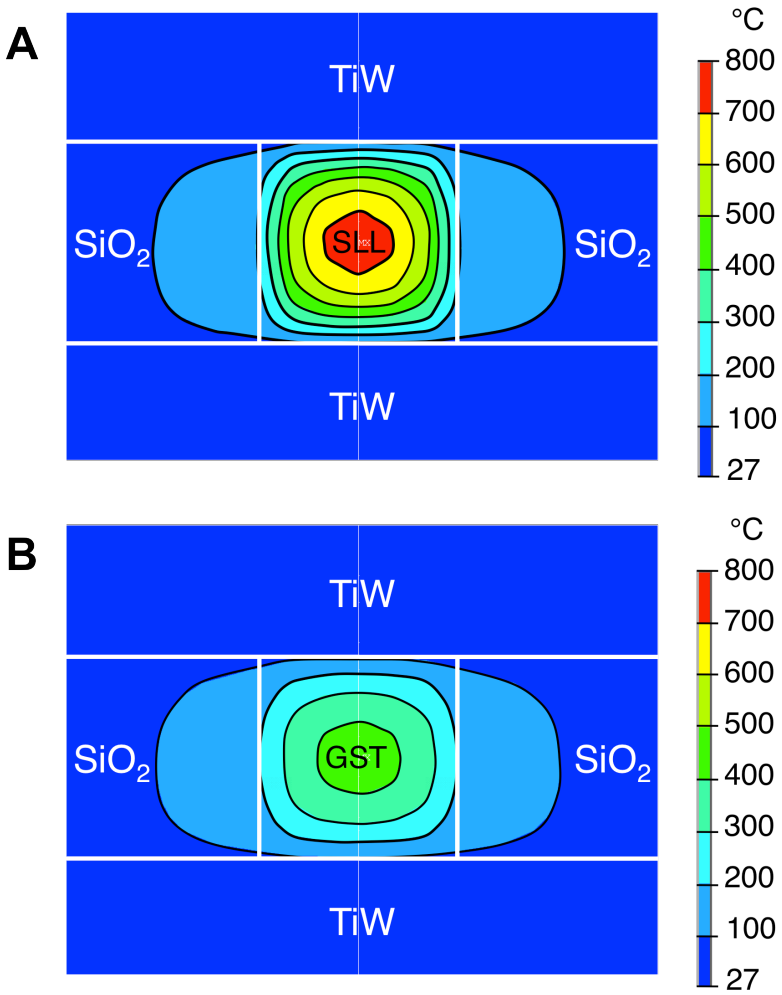

Fig. 5.6. Simulated temperature distributions in the SLL and GST cells after constant voltage-pulse activation. SLL cells (a) were found to have higher peak temperatures than GST cells (b). The thermal conductivity of the SLL material was assumed to be 2 times lower than that of the GST.

thermal conductivities of superlattice materials compared to those of bulk materials [5.7]. From these calculations, the SLL cells were observed to have a higher peak temperature compared to that of the GST cells. Such an observation reinforces the experimental findings that the SLL cells require a lower Reset voltage than the GST cells.

5.5 Mechanism Discussion

5.5.1 Interface Effects

The fast switching speed achieved in the SLL cells can be attributed to the higher surface-area-to-volume ratios of cells with smaller cell sizes, which leads to a greater amount of heterogeneous crystallization than in cells with a larger cell size. Assuming the active device region to have a cylindrical geometry with a constant height, the relative heterogeneous crystallization rates, N_s/N_l of the PC material in the active device regions with small and large cell sizes can be obtained from [5.10,5.11]:

$$N_s/N_l = (d_l/d_s) \exp [(E_{al} - E_{as})/kT], \quad (5.1)$$

where d_s/d_l and E_{as}/E_{al} are the respective diameters and crystallization activation energies of the PC material in the small and large active device regions, k is the Boltzman constant, and T is the temperature. For a given PC material, the difference $E_{al} - E_{as}$ would be small regardless of the difference in diameter [5.11], and may be ignored. Taking N_l and d_l at a fixed reference, a reduction in the diameter d_s of the cell would thus result in an increase in the crystallization rate N_s at a constant temperature. This means that cells with a smaller cell size would be able to crystallize with a shorter pulse width compared to cells with a larger cell size, for a fixed Set voltage. Comparing PCRAM cells with different materials, the SLL cells require a shorter crystallization pulse-width than the GST cells, which could be due to the low crystallization temperature of Sb_2Te_3 [5.12]. Sb_2Te_3 has a rhombohedral lattice of the tetradymite (Bi_2Te_2S) type (space group R3m), with a lower

crystallization temperature (between 90 °C and 100 °C), which enables it to crystallize first. The crystallites in the Sb_2Te_3 layer at the interface between Sb_2Te_3 and GeTe can serve as a crystallization center or nucleus for the crystallization of GeTe. Thus, this can significantly reduce the energy barrier for the crystallization of GeTe, which has a cubic rocksalt-type structure with a high crystallization temperature of 189 °C [5.13].

In this study, a sharp decrease in the switching pulse-width was observed as the cell-size is reduced. To investigate this effect, the percentage decrease in the pulse-width required to switch SLL cells, compared to GST cells of the same cell size, was plottted, as shown in Fig. 5.7. The percentage decrease was calculated as the ratio of the difference between the pulse-widths achieved by the SLL and GST cells to the pulse-width achieved by the GST cells for a given cell size shown in Fig. 5.2. At large cell sizes, there is a small and relatively constant percentage decrease in the pulse-width. This shows that the faster switching speed achieved is mainly related to the fast crystallization of the PC materials in the SLL structure. As the cell size is reduced, an increasingly larger percentage decrease in the pulse-widths is observed. Both heterogeneous crystallization at the interface between the SLL structure and the surrounding materials, and the presence of crystallization centres at the interfaces between the SLL layers, may play important roles in this phenomenon. These two interface effects may possibly combine to increase the crystallization speed of the SLL cells.

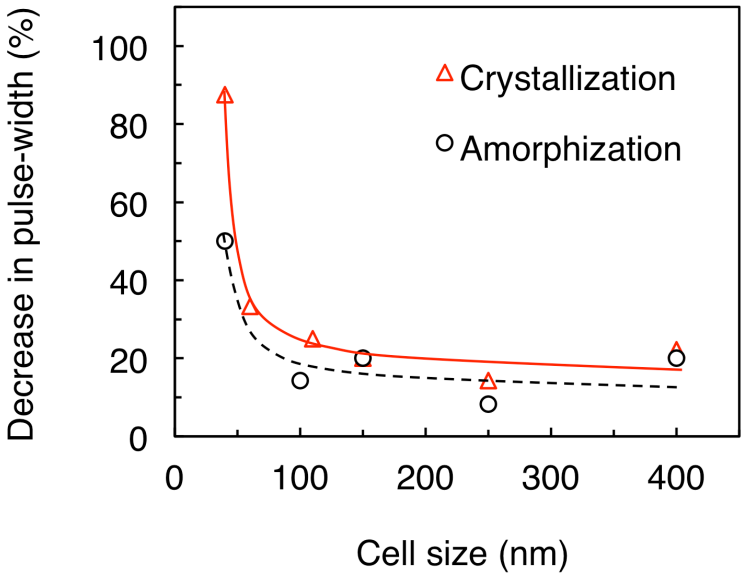

Fig. 5.7. Percentage decrease in the required pulse-widths for SLL and GST cells with different cell-sizes $(t_{GST} - t_{SLL})/t_{GST}$. A sharper drop in the pulse-width is observed as the cell-size is reduced.

5.5.2 Thermal-Confinement Effects

The most likely reason for the reduction in the operating voltage is the lower thermal conductivity of the SLL material compared to that of the bulk GST. Theoretically, the thermal conductivities of superlattice structures in both the in-plane and cross-plane directions are significantly different in the bulk materials due to interface phonon scattering and phonon-confinement effects [5.14,5.15]. Experimentally, a significant reduction in the thermal conductivities of the superlattices in both the in-plane and cross-plane directions is also observed [5.16,5.17]. The thermal conductivity of SLL materials is related to the SLL structure or the thickness of the SLL periods, and can be as low as 30 % of that of bulk materials [5.7].

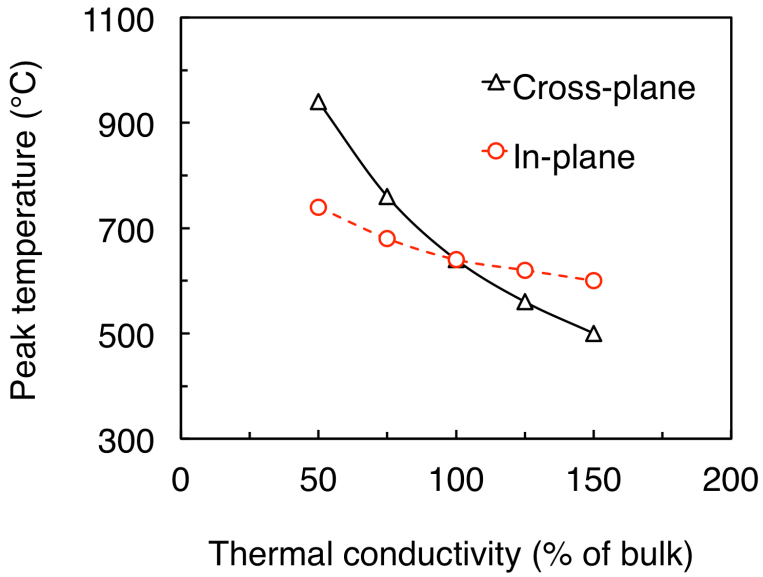

Fig. 5.8. Simulated peak temperature vs change in thermal conductivities of the SLL in the in-plane and cross-plane directions. Higher peak temperatures are observed by reduction of the thermal conductivity of the phase-change layer in the cross-plane direction, compared to when it is reduced in the in-plane direction.

In SLL structures, the thermal conductivity is anisotropic in nature. To study this effect on the thermal performance of PCRAM, finite element simualtions were performed on PCRAM cells with varying thermal conductivities in the in-plane and cross-plane directions, separately (see Fig. 5.8). Simulations revealed that higher peak temperatures were achieved when the thermal conductivity of the SLL was reduced in the cross-plane direction compared to that in the in-plane direction. Together with a reduction in the cell size, good overall thermal confinement in both the horizontal and vertical directions may account for the low operating voltage achieved in the SLL cells. Furthermore, the SLL structure has a high resistivity, which can generate more heat and increase the heating efficiency in the SLL cells.

5.6 Conclusion

In conclusion, PCRAM cells with fast switching speed and low operating power can be achieved by both reducing the size of the active device regions and by the use of SLL structures. Fast Reset and Set speeds of 300 ps and 1 ns, respectively, were achieved in 40 nm SLL cells, which can be attributed to interface effects at the cell boundaries and within the SLL structures. Further research into the use of PCRAM cells with smaller dimensions, and also SLL structures with lower thermal conductivities and higher crystallization temperatures, would be of great importance. It would enable PCRAM to achieve fast speed and low power for advanced memory applications.

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Chapter 6

Fast-Speed, Low-Power, and High-Endurance Switching in PCRAM with Nanoscale Superlattice-like Dielectrics

The fast-speed, high-endurance, and low-power switching demonstrated in the preceding chapters suggest that PCRAM could fulfill the main requirements of a universal memory. To be a true DRAM-replacement, a fast PCRAM with a higher endurance is still needed. It is thus important to study alternative methods to achieve fast speed, low power, and high endurance in PCRAM.

The present chapter aims to study the use of nanoscale superlattice-like (SLL) dielectrics as thermal insulators in PCRAM cells. The speed, power, and endurance performances of the cells with SLL dielectric are investigated. Thermal simulations of the cells with SLL dielectric and other functional materials are studied. The effects of interfaces and thermal-confinement arising from the SLL dielectric are also discussed. These demonstrate the effectiveness of SLL dielectrics for advanced memory applications.

6.1 Concept of Nanoscale Superlattice-like Dielectrics

To reduce the power and improve the speed of PCRAM, one of the most effective methods is to provide better thermal confinement within the cell. This could be realized through careful design of the dielectric surrounding the PC material. In a

PCRAM device, the dielectric is a key functional material that serves not only to define the active device region, but also to provide thermal and electrical insulation. In spite of its importance, very few dielectric materials have been studied and employed in PCRAM, examples being SiO_2 and Al_2O_3 [6.1,6.2]. This is due to difficulties in finding alternative materials with low thermal conductivities, as well as compatibility with the other functional materials in PCRAM. A nanoscale SLL dielectric with excellent thermal-confinement properties may be employed to resolve the above issues. An SLL material comprises two alternating nano-layers of non-crystalline materials [6.3]. In this study, dielectrics with SLL structures were investigated, and examined for its impact on providing better thermal confinement for achieving low-power and high-speed PCRAM.

Most SLL structures have good thermal-confinement properties [6.4]. Similar to conventional superlattice structures, they possess lower thermal conductivities than bulk materials with the same composition due to interface phonon-scattering effects [6.5]. An SLL dielectric may be formed with alternate nano-layers of amorphous $Ge_2Sb_2Te_5$ (α-GST) and SiO_2. These materials adhere well to each other, and also to the other functional materials in PCRAM devices. α-GST is reported to have a low thermal conductivity of 0.2 W/mK, which is about 7 times lower than that of SiO_2 [6.6-6.8]. However, α-GST has a low electrical resistivity of 4.16×10^4 Ωcm, and is thus unsuitable as an electrical insulator. On the other hand, SiO_2 is an excellent electrical insulator with a high resistivity of 1×10^{16} Ωcm [6.9]. When α-GST and SiO_2 are stacked periodically, a SLL dielectric is

formed, which may have thermal and electrical insulating properties superior to either α-GST or SiO_2 alone.

6.2 Methodology

PCRAM cells with an SLL dielectric comprising of α-GST and SiO_2 were fabricated and studied in this work (Fig. 6.1). SiO_2-on-Si substrates were used as the starting materials, on which a 200 nm of TiW as the bottom electrode was formed. An insulating layer (70 nm) comprising either a SLL or SiO_2 as the dielectric was deposited and patterned by lift-off. To study the dependence of device performance on the number *N* of periods in the SLL structure, 2, 4, and 7 periods of α-GST/SiO_2 were employed to form the SLL dielectric. Each period comprises a layer of α-GST (3 nm) and a layer of SiO_2 (32, 14, and 7 nm). The insulating layer has a via of 1 μm diameter, which exposes a portion of the bottom electrode, thus defining the active device region. The via was filled with 50 nm of GST, which was employed as the active PC material. A TiW top electrode (200 nm) was deposited and patterned to complete the PCRAM cell structure.

The electrical properties of the cells were studied using the in-house testing system (see Appendix A). Electrical voltages and pulse widths ranging from 0-7 V and 5-100 ns were employed, respectively. The cells were switched reversibly between the respective low- and high-resistance levels of 10 kΩ and 1 MΩ during the measurements.

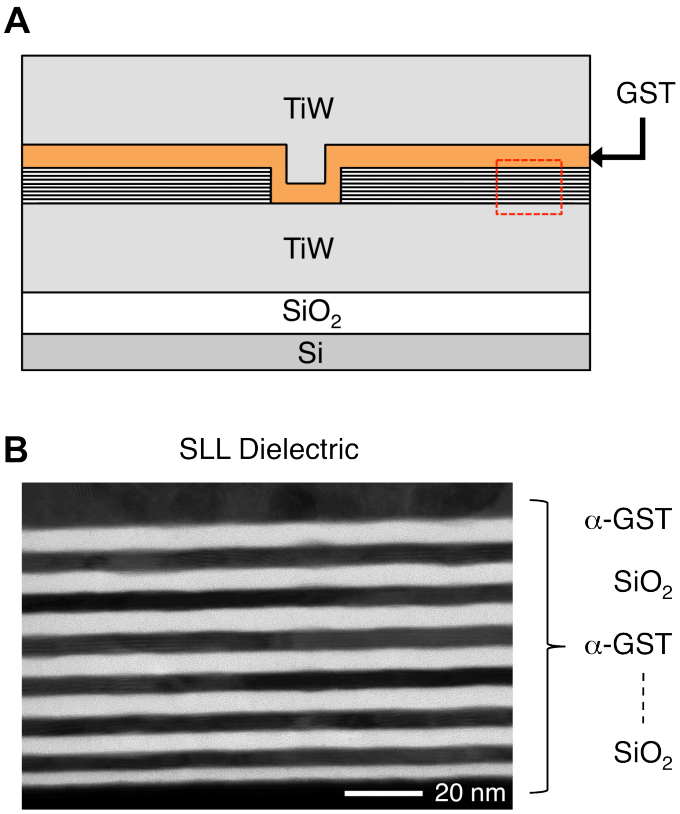

Fig. 6.1. Schematic diagram of the (a) PCRAM cell, and (b) TEM image of a GST/SiO_2 superlattice-like dielectric structure.

6.3 Device Performance

6.3.1 Correlation between Current and Pulse Width

The dependence of current on pulse duration required to switch PCRAM cells with a 7-period SLL dielectric and a single layer of SiO_2 dielectric were studied (see Fig. 6.2). The switching current was investigated by measuring the current that passed through a reference resistor (R_{load}), which was connected in series with the PCRAM cell (see Appendix A). Electrical pulses with varying durations were employed and the smallest currents required to switch the cells from the high resistance state to the low resistance state (Set), and from the low-resistance state

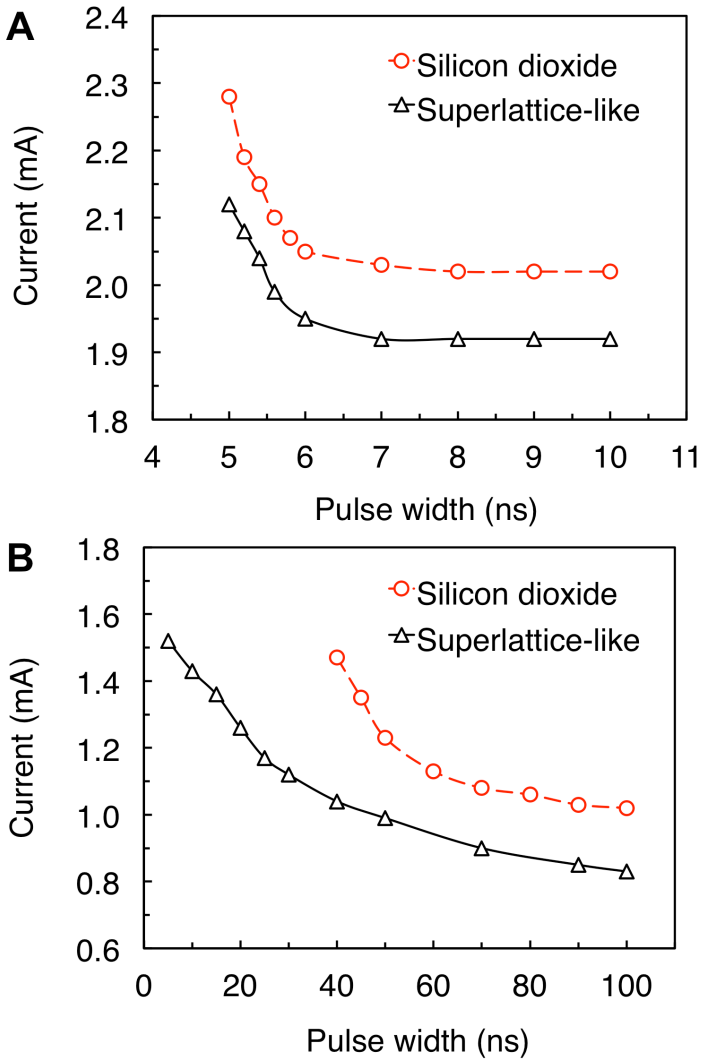

Fig. 6.2. Dependence of current on pulse-width required to (a) Reset and (b) Set cells with a 7-period SLL dielectric and a single layer of SiO_2 dielectric. Cells with the SLL dielectric require a lower current and shorter pulse-width to switch. Pulse-widths as low as 5 ns can switch the cells with the SLL dielectric.

to the high-resistance state (Reset) were recorded. The cells with the SLL dielectric can Set with a shorter pulse-width than the cells with the SiO_2 dielectric. Interestingly, despite having a large cell dimension of 1 μm, the cells with the SLL dielectric can switch with a pulse-width of just 5 ns, closely matching the times required to switch sub-100 nm cells with conventional dielectric materials [6.10]. When longer pulse-widths were used, both the cells required smaller

currents to Reset. Reset currents as low as 1.9 mA can be achieved for the cells with the SLL dielectric, which were lower than those required to Reset the cells with the SiO_2 dielectric. Similar observations were also made when the cells were Set.

6.3.2 Size-Dependent Set Speed and Reset Power

To study the correlation between the pulse duration and current with the number of periods in the SLL dielectric, the shortest Set pulse-width and the lowest Reset current required to switch the cells with the SLL dielectric with periods ranging from 2 to 7 were studied. A constant current of 1.5 mA and a pulse-width of 5 ns were applied for Set and Reset, respectively. It was observed that, as the number of period increases, the pulse-width required to Set the cell decreases sharply, by up to 5 times over the range of periods studied, as shown in Fig. 6.3. The Reset current also decreases with the number of periods in the SLL dielectric. Figure 6.4 shows that the Reset current decreases by 5-10 % as the number of period increases from 2 to 7. Overall, Figs. 6.3 and 6.4 show that both set pulse-width and reset current decrease with number of periods in the SLL dielectric. This indicates that faster crystallization and better-thermal confinement were achieved in the cells with higher number of SLL-dielectric periods. The degree of reduction for both set pulse-width and reset current was generally high, despite a smaller percentage decrease in the reset current, which should further reduce, if needed, by increasing the number of SLL-dielectric periods.

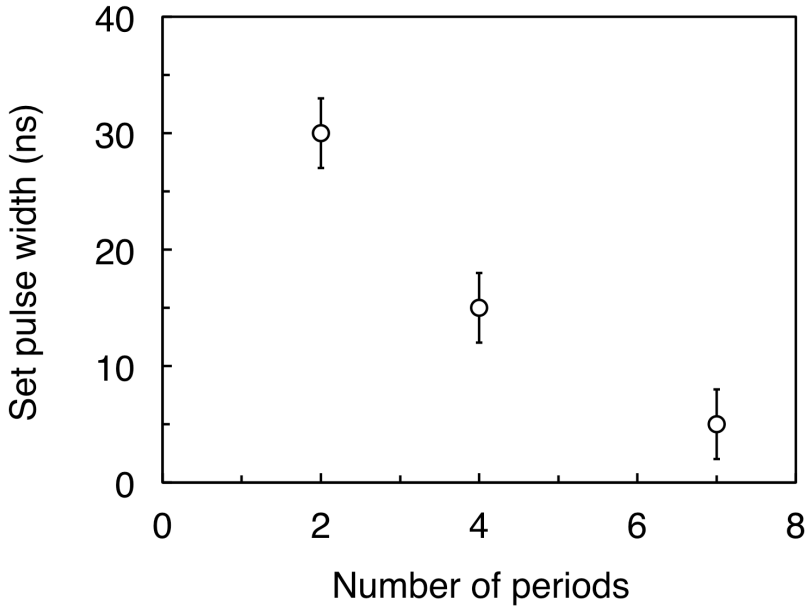

Fig. 6.3. Correlation between the Set pulse-width and the number of periods in the SLL dielectric. A shorter pulse-width was achieved as the number of periods in the SLL dielectric is increased.

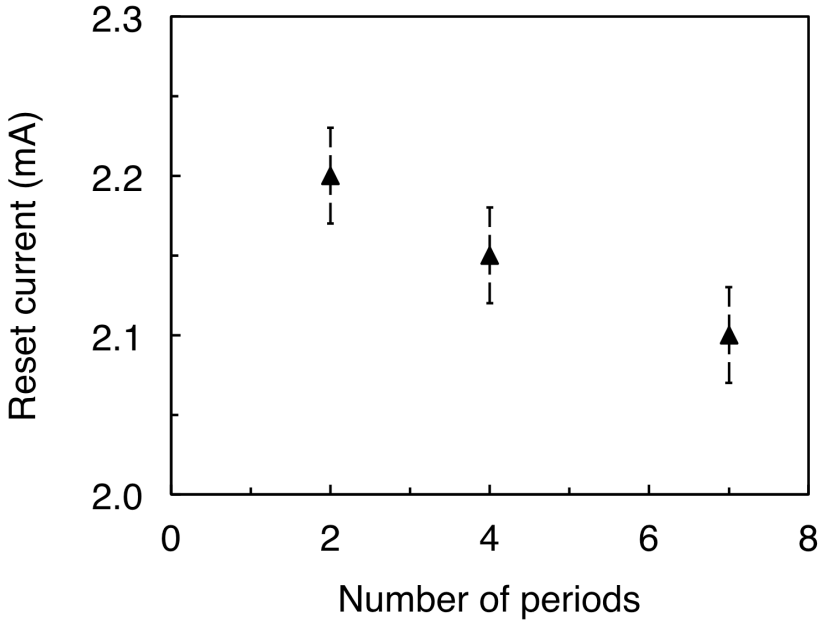

Fig. 6.4. Correlation between the Reset current and the number of periods in the SLL dielectric. A lower current was achieved as the number of periods in the SLL dielectric is increased.

6.3.3 Cycle Endurance

Cells with SLL dielectric not only have good performance in terms of power and speed, but also high cycle-endurance (see Fig. 6.5). Reversible switching of the cells with a SLL dielectric was observed, with an excellent contrast maintained for 10^9 overwriting cycles. The cells were switched between low- and high-resistance states of about 10 kΩ and 2 MΩ, with Reset and Set pulse-widths of 5 ns and 200 ns, respectively. Since device stability is related to cycle endurance, the high number of overwriting cycles achieved shows that PCRAM with SLL dielectric has good device stability. Such a demonstration also indicates that the SLL dielectric has good electrical-insulation properties, and does not cause early device failure.

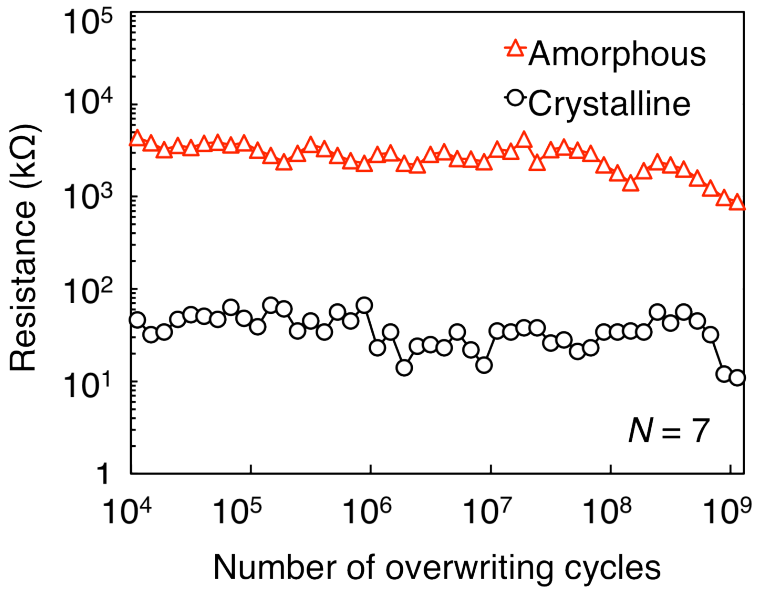

Fig. 6.5. Endurance performance of a PCRAM cell with a SLL dielectric. The cell has good dielectric breakdown properties, which enables it to achieve stable and reversible switching for 10^9 cycles.

6.3.4 Property of SLL Dielectric after Cycling

The SLL dielectric also has good material properties. Figure 6.6 shows that there is still a clear separation between the GST and SiO_2 layers in a cell that has been switched many times between the amorphous and crystalline states. There is also no observable delamination of the GST and SiO_2 layers. This further shows that the SLL dielectric does not cause early device failure, and supports the fact that PCRAM cells with SLL dielectric can support high endurance, as demonstrated by the cells switching reversibly and stably for 10^9 cycles.

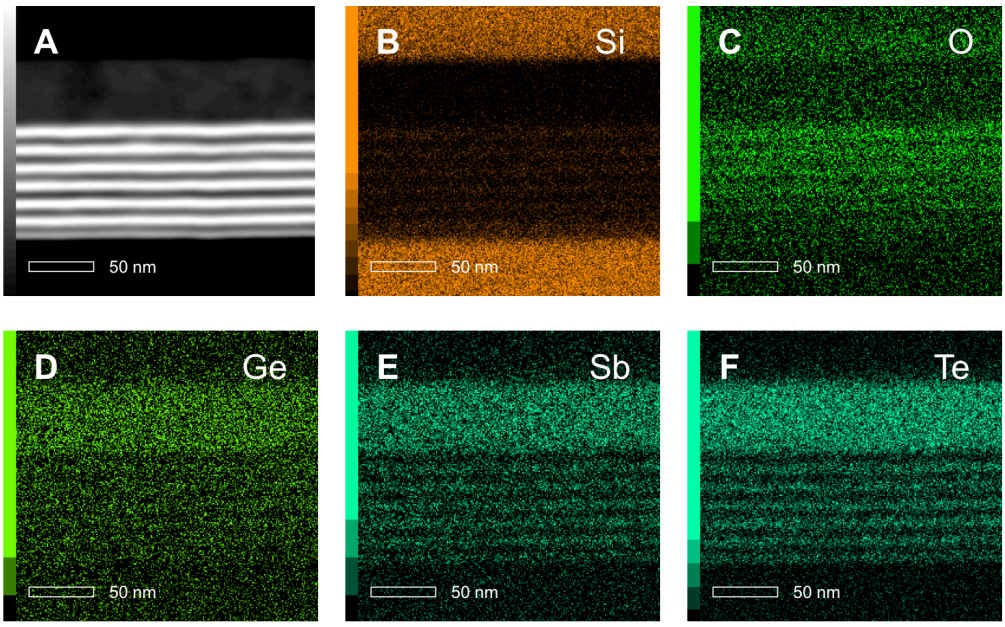

Fig 6.6. Experimental study of the material properties of the SLL dielectric. (a) Scanning transmission electron microscopy (STEM) image of the SLL dielectric, and energy-dispersive x-ray spectroscopy (EDX) images of (b) Si, (c) O, (d) Ge, (e) Sb, and (f) Te. These images show no observable delamination of the GST and SiO_2 layers.

6.4 Finite-Element Simulation

6.4.1 Effect of Superlattice-like Dielectrics

The thermal properties of the PCRAM cells were examined using finite-element simulations (see Appendix C) to calculate the temperature profiles of cells with a SLL dielectric or a SiO_2 dielectric after Reset (see Fig. 6.7). In a PCRAM cell, the electrode/PC-material interface plays an important role in the heat-generation process [6.11,6.12]. To simplify the calculations, the effects of the electrode/PC-material interface were not considered in this study, in order to better compare the effects of the dielectric materials on the cell performance. In the simulations, the thermal conductivities of the materials employed were important parameters, with values shown in Table 6.1. Considering the low thermal conductivities achieved in superlattice structures [6.13], the thermal conductivity of the SLL dielectric was assumed to be 20 % of that of the SiO_2 dielectric. From the simulations, a higher peak temperature (PT) was observed in the active device region of the cell with the SLL dielectric compared to that of in the cell with the SiO_2 dielectric. For a given amount of thermal energy input, the steep temperature gradient in the lateral direction of the SLL dielectric is mainly due to its low thermal conductivity. A simulation was also performed to study the effects of the heat transport on the performance of the cells with SLL dielectrics. The cells were found to have a slightly higher PT when the thermal conductivity of the SLL dielectric is reduced in the cross-plane direction compared to that in the in-plane direction. This is possibly related to the greater amount of heat flow towards the vertical direction of the SLL dielectric.

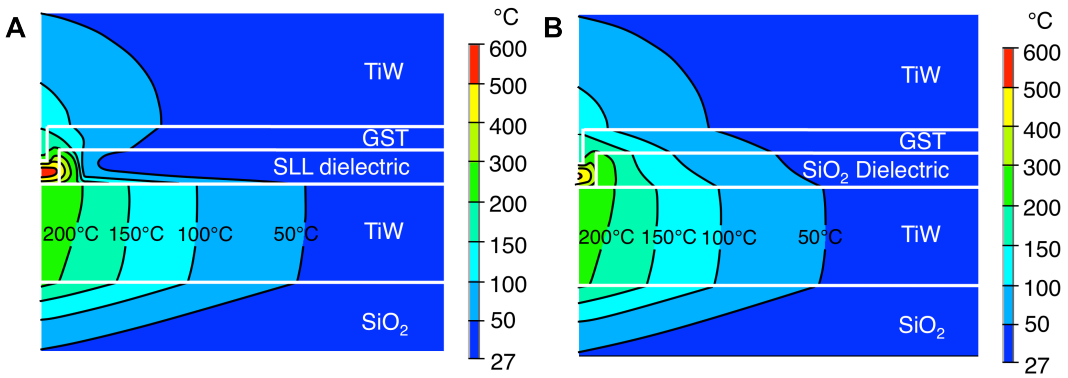

Fig. 6.7. Simulation of the temperature profiles in PCRAM cells with (a) a SLL dielectric and (b) a SiO_2 dielectric. The thermal conductivities of the SLL and SiO_2 dielectric used were 0.28 W/mK and 1.4 W/mK, respectively. Good thermal confinement is observed in the cell with the SLL dielectric.

Table 6.1. Material thermal parameters.

Material	Thermal conductivity (W/mk)
c-GST	0.20[a]
TiW	60.0[b]
SiO_2 dielectric	1.40[c]
SLL dielectric	0.28

[a]Reference 6.6.
[b]Reference 6.7.
[c]Reference 6.8.

6.4.2 Thermal Conductivity of Phase-Change Materials

The interplay between the SLL dielectric, functional materials, and cell structures was further studied. Understanding the interplay between the materials and structures is very important, as it would enable better control of the thermal properties of the SLL dielectric, and improve the thermal confinement in a PCRAM device.

A higher PT can be achieved via scaling of the SLL dielectric, which also corresponds to a reduction of the SLL layer thickness. The variation of the SLL

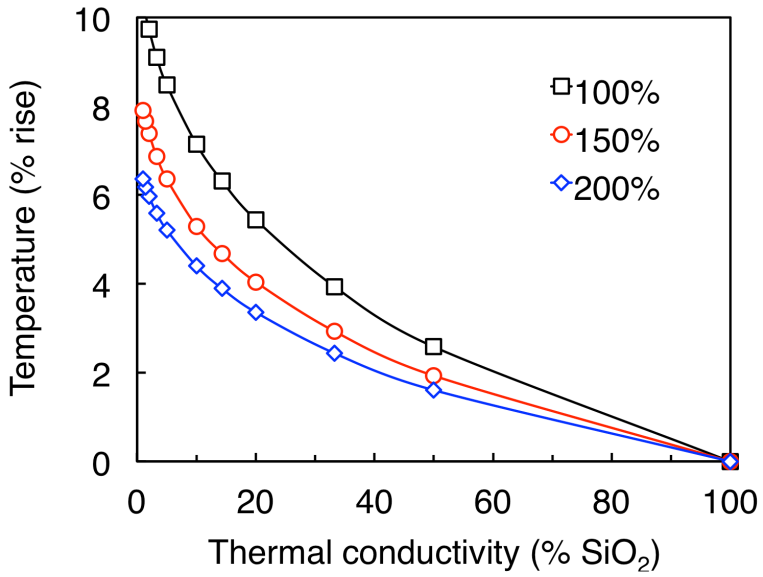

Fig. 6.8. Simulated peak temperature as a function of the thermal conductivity of the SLL dielectric (defined as a percentage of the thermal conductivity of the SiO_2 dielectric), for different PC materials. Higher peak temperatures are observed when a PC material with a lower thermal conductivity is used. The cell has a u-shaped device structure, and a cell size of 100 nm.

layer thickness is known to have a large effect on the thermal conductivity of the SLL structure [6.14,6.15]. To study the size-dependent properties of the SLL dielectric, the rise in PT as a function of its thermal conductivity was investigated, as shown in Fig. 5.8. The rise in PT was calculated as the ratio of the PT in the cell with the SLL dielectric to the PT in the cell with the SiO_2 dielectric. A higher rise in PT is observed as the thermal conductivity of the SLL dielectric is reduced. The rise in PT becomes even more significant when the thermal conductivity of both the SLL and the PC material is decreased. For instance, the percentage rise in PT for a cell with GST is much higher (from 0 to 9.74 %) compared to that for a cell with a PC material with a thermal conductivity that is twice that of GST (from 0 to 6.36 %), as the thermal conductivity of the SLL dielectric is reduced from 100 to 1 %.

6.4.3 Cell-Size Effects

The PT can also be controlled by varying the PCRAM cell size. Figure 6.9 shows that the rise in PT becomes more significant when both the thermal conductivity of the SLL structure, and the cell size are decreased.

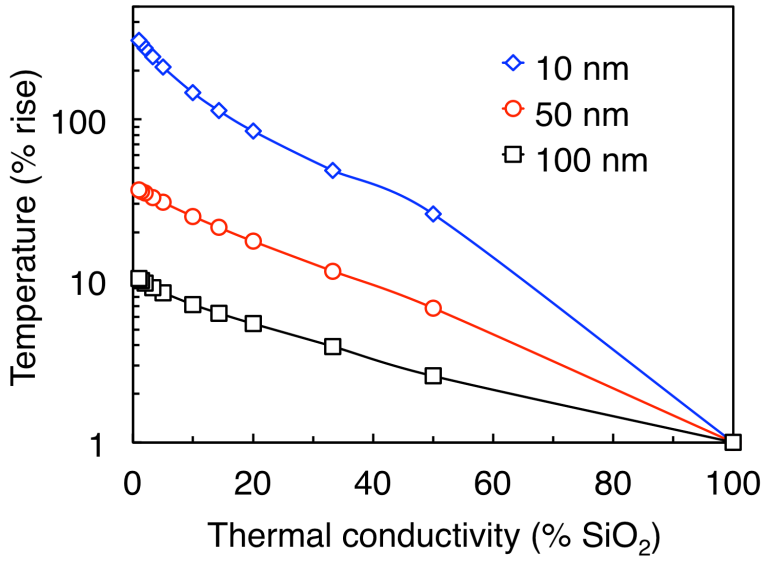

Fig. 6.9. Simulated peak temperature as a function of the thermal conductivity of the SLL dielectric (defined as a percentage of the thermal conductivity of the SiO_2 dielectric), for different cell sizes. Higher peak temperatures are observed when smaller cell sizes are used. The cell has a u-shaped device structure.

6.4.4 Effects of Device Structure

Modification of the PCRAM structure can also control the PT. The rise in PT becomes more significant when both the low-thermal-conductivity SLL structure, and the u-shaped device structures are used (see Fig. 6.10).

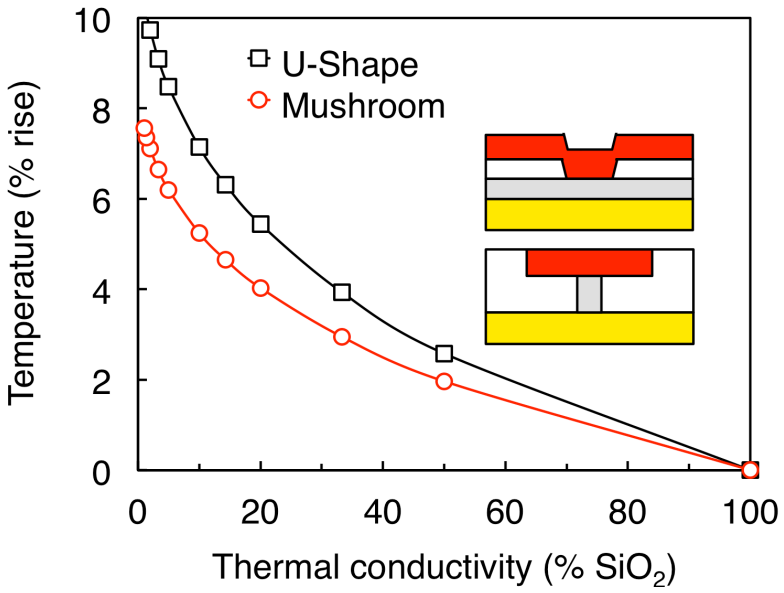

Fig. 6.10. Simulated peak temperature as a function of the thermal conductivity of the SLL dielectric (defined as a percentage of the thermal conductivity of the SiO_2 dielectric), for different device structures. Higher peak temperatures are observed when u-shaped structures are used. The cell size is 100 nm. The top and bottom insets show the u-shaped and mushroom device structures, respectively.

6.4.5 Substrate Effects

The PT can also be controlled by varying the substrate used during the PCRAM fabrication. Figure 6.11 shows that the rise in PT becomes more significant when both the low-thermal-conductivity SLL structure, and a substrate with thermal oxide are employed.

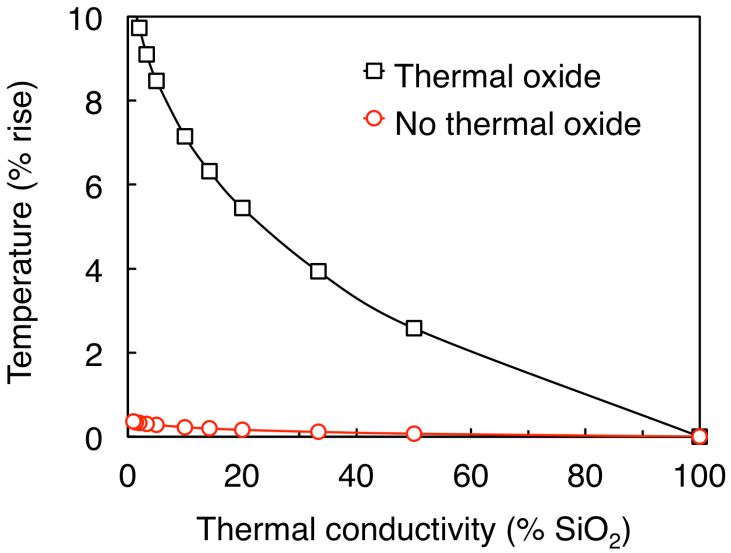

Fig. 6.11. Simulated peak temperature as a function of the thermal conductivity of the SLL dielectric (defined as a percentage of the thermal conductivity of the SiO_2 dielectric), for different substrates. Higher peak temperatures are observed when substrates with thermal oxide are used. The cell has a u-shaped device structure, and a cell size of 100 nm.

6.5 Mechanism Discussion

6.5.1 Interface Effects

Interfaces are known to have atomic-scale defects that act as efficient phonon-scattering centres. When more interfaces are generated, a greater amount of phonon scattering occurs across the dielectric, which reduces the phonon mean free path and hence heat flow in the in-plane and cross-plane directions [6.16]. In the superlattice system, the net heat flow is inversely related to the number of interfaces in the superlattice structure. The heat flow in the cross-plane direction is governed by the equation [6.17]:

$$j = \frac{\sigma}{n}\left(T_H - T_c\right), \tag{6.1}$$

where n is the number of interfaces, σ is the interface conductance and $T_H - T_C$ is the temperature difference at the interface. Since σ and $T_H - T_C$ are constant as all the interfaces are found between the α-GST and SiO_2, an increase in the number of interfaces will lower the heat flow in the cross-plane direction and reduce the net heat flow in the SLL dielectric. It is known that no crystallization of α-GST occurs when the thickness of the α-GST films is less than around 3 nm [6.18]. As α-GST layers with thicknesses of about 2-3 nm were employed in this study, little or no crystallization of α-GST should occur in the SLL dielectric. The resulting low thermal conductivity would enable the cells with a SLL dielectric to switch with lower currents and shorter pulse-widths than the cells with a SiO_2 dielectric.

6.5.2 Thermal-Confinement Effects

Good thermal confinement of the SLL dielectric can be attributed to the interface-scattering mechanism. This can be studied via the dependence of the PT on the anistropic thermal conductivity of the SLL dielectric, as seen in Fig. 6.12. The PT is observed to be slightly higher as the thermal conductivity of the SLL dielectric is reduced in the cross-plane direction (580 °C at 75 %, 617 °C at 25 %) compared to that in the in-plane direction (577 °C at 75%, 598 °C at 25 %). This indicates an overall good thermal confinement in both the in- and cross-plane directions, with a slight dominance of the interface-scattering mechanism in the cross-plane direction. The PT difference (between the in- and cross-plane directions at low thermal conductivity) of the SLL dielectric was also observed to be smaller than that in the

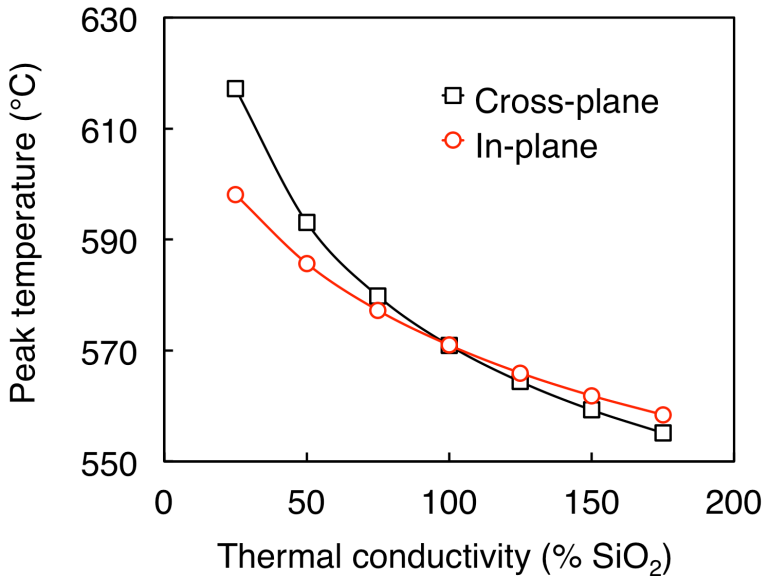

Fig. 6.12. Thermal-confinement properties of SLL dielectrics. Relatively higher peak temperatures are observed as the thermal conductivity of the SLL dielectric is reduced in the cross-plane direction compared to that in the in-plane direction. The overall good thermal confinement in both the in- and cross-plane directions would reduce the energy required for Reset. The cell has a pore device structure, and a cell size of 100 nm.

$GeTe/Sb_2Te_3$ SLL material that was reported previously [6.19]. A smaller PT difference indicates a better control of the heat flow within the cell structure.

6.6 Conclusion

In summary, a SLL dielectric can be employed as a thermal insulator due to its low thermal conductivity. This enables PCRAM cells with a SLL dielectric to operate with lower currents and shorter electrical pulse-widths than cells with a SiO_2 dielectric. PCRAM technology would benefit greatly from further research on SLL dielectrics with lower thermal conductivities, as this would potentially accelerate the development of low power and high speed PCRAM devices.

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Chapter 7

Summary and Outlook

PCRAM is an exciting and promising nonvolatile memory technology due to its high scalability, fast speed, low power, and high endurance. These qualities have made PCRAM a potential universal memory that can perform the functions of many different classes of memory. Although PCRAM has many outstanding qualities, there exists a trade-off between crystallization speed and thermal stability of the amorphous phase. This severely limits the speed of PCRAM devices. Overcoming this limitation is vital for PCRAM to become a universal memory. In this thesis, nanoscale effects in PC materials, as well as in the other functional materials, were exploited to achieve fast-speed, low-power, and high-endurance performance.

Reviews of the current state of PCRAM research, and of the fundamentals and theories related to the switching speed of PC materials were presented in Chapter 2. These highlighted the complexity of the PC process, and the many factors affecting the speed of PCRAM. However, the PC mechanism is still unclear, and the proposed models remain inadequate to fully explain the general switching behavior of PC materials. These studies also revealed the requirements for fast speed, as well as low power and high endurance in PCRAM.

In Chapter 3, a study of incubated PC materials with nanostructural units was presented. The PC speed was found to increase with the applied incubation field. A

crystallization speed of 500 ps was achieved, as well as high-speed reversible switching using 500 ps pulses. Ab initio molecular dynamics simulations revealed the PC kinetics in PCRAM devices, and the structural origin of the incubation-assisted increase in crystallization speed.

Studies of nanostructured PC materials were presented in Chapter 4, where this understanding was used to achieve both fast speed and high endurance in PCRAM. As the device size is reduced, the PC mechanism was found to change from a material inherent-crystallization mechanism to a hetero-crystallization mechanism, which resulted in a significant increase in switching speed. Reducing the grain-size can further increase the PC speed. The effect of grain-size on switching speed becomes increasingly significant at smaller device sizes. By exploiting nano-thermal and electrical effects, fast switching, good stability, and high endurance were demonstrated.

Chapter 5 presented a study of nanoscale PC materials with superlattice-like (SLL) structures, and the impact of these materials on achieving fast PC speeds, while maintaining low-power consumption in PCRAM devices. The correlation between the size, speed, and power of the SLL cells was investigated. Small SLL cells were found to switch shorter pulses and lower powers compared to large SLL cells. Fast amorphization and crystallization speeds of 300 ps and 1 ns were achieved in the SLL cells, respectively. Both speeds were much faster than those observed in the GST cells. SLL cells also required lower switching voltage than the GST cells. These effects can be attributed to fast heterogeneous crystallization, low thermal conductivity, and high resistivity of SLL PC materials.

In Chapter 6, nanoscale SLL dielectrics were exploited to achieve fast switching, as well as low power and high endurance in PCRAM. In this study, PCRAM cells with a SLL dielectric required lower currents and shorter pulses to switch compared to cells with a SiO_2 dielectric. As the thickness of the SLL period is reduced, the power and speed of the cells is improved further, due to better thermal-confinement in the SLL dielectric. A fast switching of 5 ns was observed even in large 1-μm cells. A high endurance of 10^9 cycles was also achieved.

Various future research opportunities were highlighted in the respective chapters. A particular follow-up project of this thesis is the study of fast switching in multilevel PCRAM. It is known that as devices continue to shrink, their ultimate-scaling limits will be reached eventually. This means that multilevel PCRAM may become the next most feasible solution to further increase data-storage capacity. It is thus important to investigate fast PC in multilevel PCRAM, for instance, how switching speed could be affected by reliability factors, such as: (i) intrinsic-randomness associated with each write attempt, (ii) resistance drift, (iii) variability during lifetime of PCRAM array, and (iv) crystallization of amorphous phase. Among them, factors such as resistance-drift and crystallization-of-amorphous-phase would likely represent fundamental storage-capacity limitations, as in the maximum number of bits that can be stored in a cell, which may not be overcome but only be mitigated.

Another follow-up project could be the study of fast switching in 3-dimensional (3-D) stacked PCRAM, which is another approach to increase data-storage. This concept is based on the building of multiple layers of PCRAM

devices, which are stacked and integrated in 3-dimensions above the silicon wafer. It would be interesting to study how fast switching can be achieved in these devices, especially the effect of fast switching on Reset current, which is currently too high for the integration of PCRAM with poly-silicon diodes or non-silicon access devices, thus posing a key limitation for this technology.

PCRAM continues to be highly promising for next-generation data-storage devices. In principle, the methods discussed in this thesis are applicable to all types of PC materials and device-structures, such that an appropriate combination of materials and structures open opportunities for optimizing device performance. This would pave the way for achieving a broadly applicable memory device, capable of nonvolatile, fast, stable, and low-power operations.

Appendix A

Electrical Characterization

The PCRAM device performance was investigated using an in-house PCRAM testing system [A.1] that comprises mainly of a picosecond pulse generator (Picosecond Pulse Labs), a digital oscilloscope (Agilent Technologies), and a probe station, as shown in Fig. A.1.

The picosecond pulse generator has the specifications of pulse durations ranging from 100 ps to 10 ns, rise time of 65 ps, and voltage amplitude up to 7.5 V. The PCRAM is connected to the generator/oscilloscope via low-capacitance cables (~0.2-3 pF) and a low resistor of 50 Ω. The upper limit of the time constant of the RC circuit is estimated to be ~several 10 ps. To study the ultrafast switching effects, the PCRAMs were constantly biased with a small voltage, and

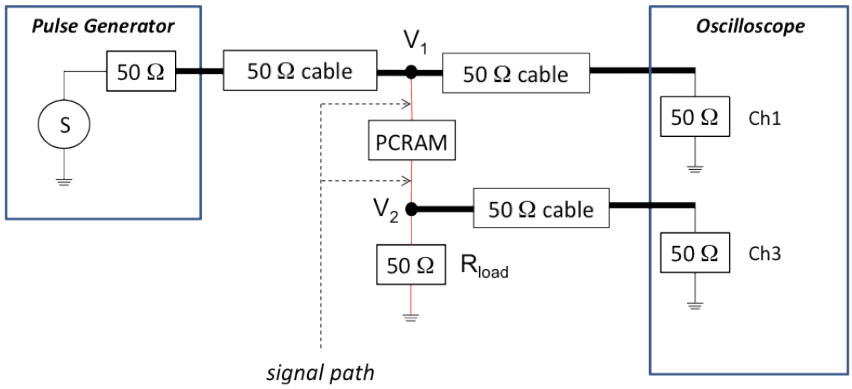

Fig. A.1. Schematic of the experimental/measurement setup. To study the switching effects of the PCRAM, a pulse generator is programmed to deliver a short electrical pulse to the PCRAM cell. The waveforms of the pulses at a point before and after the PCRAM cell were measured at V_1 and V_2, respectively.

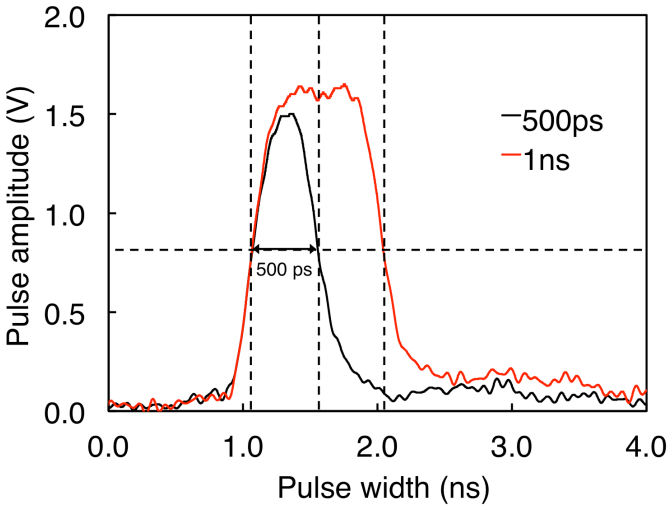

Fig. A.2. Waveforms of the electrical pulse applied to the PCRAM cells. Electrical pulses with pulse widths (full-width, half-maximum) down to 500 ps were employed to switch the cells. The pulse waveforms were measured/obtained at V_1 (Fig. S1).

subsequent electrical pulses were applied to switch the PCRAMs. The full-width, half-maximum time duration (FWHM) of the pulse (Fig. A.2) was measured at V_1 (Fig. A.1), and this was used to characterize the speed of the PCRAM switching.

The waveform of the pulse obtained at V_1 also reflects the exact voltage pulse that is applied to the PCRAM, taking into account the capacitance/inductance of the probe/circuitry/connectors. Figure A.3 further shows the waveforms of the pulse signal measured before (V_1) and after (V_2) the PCRAM. From the measurement results, we can clearly see that the FWHMs of the waveforms measured at V_1 and V_2 are almost the same. More specifically, the difference in the FWHMs in the case of the 500 ps pulse is only about 4 %, which is within the measurement error of the oscilloscope with a frequency of 10 GHz. As the signal measured at V_2 has passed through the PCRAM, this confirms that the duration of the pulse experienced by the PCRAM is almost identical to that of the pulse

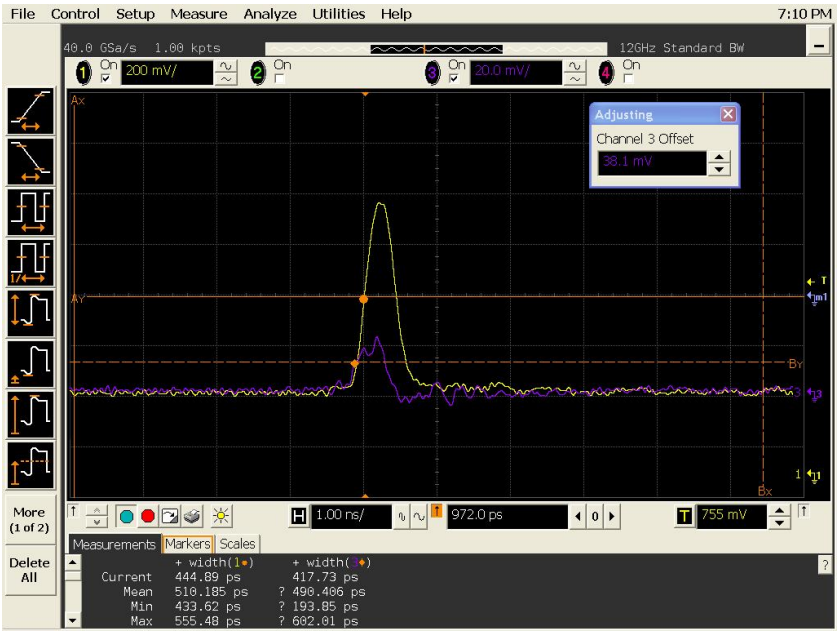

Fig. A.3. Waveforms of the applied 500 ps pulse signal at a point before (V_1) and after (V_2) the PCRAM cell. The yellow waveform shows the pulse signal measured at V_1. The purple waveform shows the pulse signal measured at V_2. As the signal measured at V_2 has passed through the PCRAM, this confirms that the duration of the pulse experienced by the PCRAM is almost identical to that of the pulse entering the PCRAM.

entering the PCRAM. A comparison of the shapes of the pulses measured at V_1 and V_2 also confirms that the parasitic-capacitance effects in the circuit/PCRAM are negligible.

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Appendix B

Ab initio Molecular-Dynamics Simulations

1. Computational Procedures

Constant-volume ab initio molecular-dynamics (AIMD) simulations were performed using the Vienna Ab initio Simulation Package (VASP) [B.1]. The 180-atom models of $Ge_2Sb_2Te_5$ were simulated in cubic supercells with periodic boundary conditions. The projector augmented-wave (PAW) method [B.2] with the Perdew-Burke-Ernzerhof (PBE) exchange-correlation functional [B.3] was used. The energy of the models was calculated at the gamma point with a plane-wave energy cutoff of 175 eV, and the time step was 3 fs. The temperature was controlled by velocity scaling. A density (6.11 g/cm^3) intermediate between the amorphous and crystalline phases was used, mimicking capped cells. The outer s and p electrons for Ge, Sb, and Te atoms were considered as valence electrons.

An atomic configuration was first mixed at 3000 K for 13 ps and then maintained at 1073 K for 60 ps. Three amorphous configurations (models 1, 2, and 3) were obtained by quenching three liquid configurations of GST (each having different configurations) to room temperature with a quench rate of -15 K/ps. The calculated pair-correlation functions of the amorphous configurations showed overall agreement with experiment, except for the slight overestimation of the first pair-correlation peak (~0.1-0.2 Å), presumably due to the well-known feature of the PBE functional [B.4]. These amorphous models were then pre-

annealed at 420 K for 270 ps. The pre-annealed model 3 was further annealed at 600 K and then compared with the model 3 that was annealed at 600 K without pre-annealing.

2. Definition of Structural Units

Based on the metastable rocksalt structure of crystalline GST, we defined three structural units: 4-fold rings, planes, and cubes. 4-fold rings were defined when four atoms form a square, with an average bond angle of 90°. A maximum deviation of 20° was allowed in the bond angle and in the plane angle between two parallel triangles (consisting of three atoms) that share a diagonal in 4-fold rings. Connected 4-fold rings are defined as a plane when at least two parallel 4-fold rings share an edge. Cubes have six 4-fold rings. Each ring shares its four edges with four adjacent 4-fold rings with an average plane angle of 90°. A cut-off distance of R_{cut} = 3.5 Å between atoms was used to define these structural units.

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Appendix C

Finite-Element Simulations

The simulations were performed using the ANSYS-based integrated software [C.1] for the analysis and design of PCRAMs (Fig. C.1). The thermal distribution of the PCRAM was calculated for different applied voltages (0.1-1.0 V), and pulse widths (10-30 ns). The material properties (see Table C.1) were assumed to be independent of the temperature. Heat is mainly generated in the PC layers.

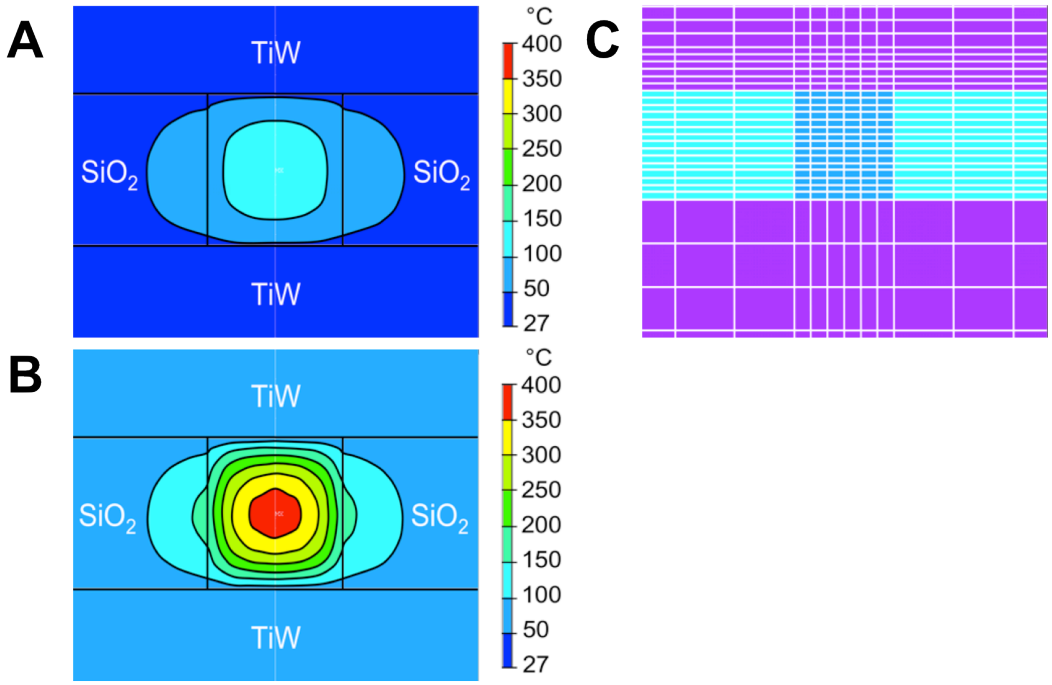

Fig. C.1. Simulated temperature distributions in a PCRAM cell obtained at: (a) low voltage and (b) high voltage. A higher peak temperature is observed in the PCRAM as the voltage increases. (c) Schematic of the mesh used to simulate the PCRAM structure. Closer mesh lines were drawn in the phase-change region for better accuracy in the calculations.

Table C.1. Material parameters.

Material	Thermal Conductivity (W/mK)	Density ($\times 10^3$ kg/m^3)	Specific heat ($\times 10^2$ J/kgK)
GST	0.20	6.15	2.10
TiW	60.0	14.8	1.37
SiO_2	1.40	2.65	6.70

The thermal transfer obeys the standard heat-conduction equation:

$$\nabla \bullet k\nabla T + Q = \rho c \frac{\partial T}{\partial t} \tag{C.1}$$

where ∇ is the gradient operator, k, the thermal conductivity, c, the specific heat, ρ, the density, t, the time, T, the temperature and Q, the Joule heat per unit volume and per unit time, which is called the heat density.

References:

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