High Performance Lateral Phase Change Random Access Memory

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Declaration

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

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Abstract

Phase change random access memory (PCRAM) is one of the best candidates for next generation non-volatile memory. Lateral PCRAM presents one of the best device structures for achieving high device performance. This dissertation presents the solutions to achieve high performance lateral PCRAM devices.

Chapter 1 introduces the background of this work, providing a comprehensive description of the semiconductor memory technology, including volatile and non-volatile memories. For non-volatile memory, flash memory, ferroelectric random access memory (FeRAM), spin torque transfer random access memory (STT-MRAM) and PCRAM are compared. PCRAM technology is emphasized and described in detail. Lateral type PCRAM devices shows superior device performance than other types of PCRAM devices. This chapter introduces the development history, the advantages and disadvantages of the lateral PCRAM. It is found that the lifetime of lateral PCRAM devices is poor than other structure PCRAM devices.

To study the weakness of the poor lifetime of the lateral PCRAM devices, the failure mechanism of the lateral PCRAM devices are discussed in Chapter 2. Vertical and lateral PCRAM devices with the same materials at the same dimension are compared. As the structures of vertical and lateral PCRAM devices are different, the mechanical properties should be different. Hence, the plastic deformations of confined and lateral PCRAM are investigated through both experiments and simulations. It was found that the lifetime of lateral PCRAM devices is poor and the plastic deformation is large. For confined PCRAM devices, the lifetime is better and the plastic deformation is small. Simulation has been done to investigate the thermo-mechanical analysis for both confined and lateral PCRAM based on finite element method. Simulation results show that lateral PCRAM has much better thermal confinement than confined PCRAM, which cause heat accumulation and temperature

increment during overwriting. And the thermal expansion in phase change material of lateral PCRAM device is much larger than that of confined PCRAM. This could be caused by the soft dielectric cover in lateral PCRAM. Hence, the weak structure of lateral PCRAM is the reason for large plastic deformation and early failure.

To improve the lifetime of lateral PCRAM, superlattice-Like (SLL) structure is proposed to limit plastic deformation in phase change material. In Chapter 3, the concept of growth-dominant SLL structure phase change medium is proposed. Using growth-dominant SLL medium in lateral PCRAM, better lifetime and lower RESET current were achieved. It was found that the lifetime of lateral PCRAM reached about 5.3×10^6 cycles and the RESET current reached 1.5 mA.

Power consumption is one of the key issues for PCRAM devices. In Chapter 4, edge-contact structure is proposed for lateral PCRAM to reduce the RESET current. Simulation results show that better thermal confinement achieved in lateral PCRAM devices in edge-contact structure. Both the normal and edge-contact lateral PCRAM with growth-dominant SLL medium were fabricated and compared. With the edge-contact structure, the RESET current is decreased from 1.5 mA (normal structure) to 1.2 mA, and the resistance ratio between the RESET and SET states is increased from 20 (Normal) to above 100 times.

In Chapter 5, multi-level lateral PCRAM devices were investigated based on lateral PCRAM with growth-dominant SLL structure. Testing results show that multiple states can be achieved by applying different programming pulses to change the volume of the active regions in lateral PCRAM devices. Heat accumulation in lateral PCRAM devices can affect the programming volume during cycle endurance test. The different states are thus not stable. Hence, a new SLL structure incorporating a phase change material and a dielectric material was proposed to achieve discrete and stable multi-level lateral PCRAM devices. Lateral PCRAM devices with this new SLL structure were fabricated and tested. Testing results

showed that discrete intermediate states could be achieved. Simulations were also done to investigate the working mechanism.

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Chapter 1 Introduction

Consumer electronics products, including cell phone, digital camera, iPad and notebook, are supporting the growing demand for nonvolatile memories (NVMs) [1，2]. Currently, NVMs such as Flash memory are facing severe scalability limitations. New memories are being explored for next generation NVM technologies. Phase Change Random Access Memory (PCRAM) is considered as one of the best candidates for the next generation NVMs technology, because of its superior device performance and good scalability [3]. Many PCRAM structures have been studied to improve the device performance. Lateral PCRAM represents one of the best structures for PCRAM devices. This chapter will briefly review the existing memory technologies and provide a detailed description of the PCRAM technology and lateral PCRAM devices.

1.1 Introduction to Semiconductor Memories

Semiconductor memories constitute the most attractive segment in the global semiconductor market. They occupy one-third of the entire semiconductor market and maintain the fastest growing rate. There are two categories of semiconductor memories: volatile memories and non-volatile memories. Volatile memories do not retain their data when the power supply is turned off. There are two main types of volatile memories: Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM). DRAM is the most cost- and space-efficient memory because each DRAM cell consists of only one transistor and one capacitor [4]. DRAMs have occupied the largest

market segment of the semiconductor memory market for more than 10 years as shown in Figure 1.1 [5]. SRAM is the fastest memory with a lower standby current compared to DRAM. However, a SRAM cell consists of four or six transistors [6], resulting in a very low chip density and relatively high cost. SRAM had been ranked the second in the semiconductor memory market for a long period of time. However, its market share fell to the third largest due to the fast development of NVMs [5]. Non-volatile memories are memories that retain their data even when the power supply is turned off. Currently, the most successful and dominant technology for NVM is Flash memory. It can store data for at least 10 years when the power supply is turned off.

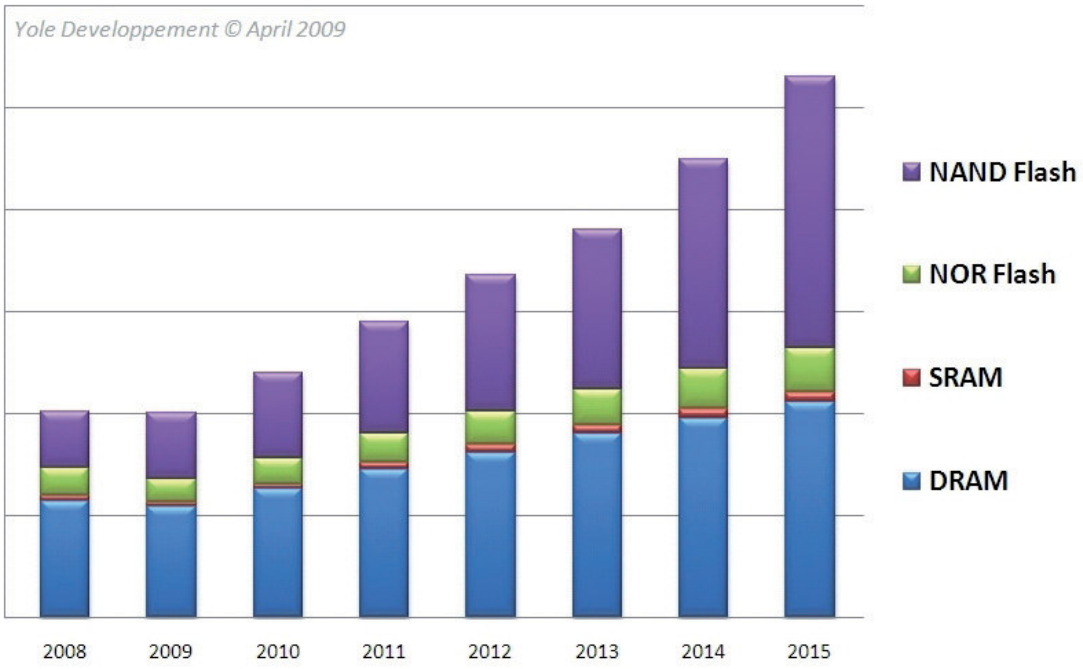


Figure 1.1 Forecast of the semiconductor memory market by Yole Development [5].

Since 1999, Flash memory has exceeded SRAM and occupied the second largest segment of the market for semiconductor memories. It is predicted that Flash memory will occupy the top position in the future [5, 7]. Figure 1.2 (a) shows the conventional

structure of Flash memory. Conventional Flash memory faces three problems: (1) relatively long programming time of 1 μs to 1 ms [8]; (2) limited cycle endurance of less than 10^6 [9]; and, (3) its scaling limitation [10, 11]. Flash memory faces scaling limitation due to the tunneling of electron through the floating gate, which causes the data to be lost easily. To obtain a 10-year retention time, the tunneling thickness of conventional Flash memory must be larger than 6-7 nm in consideration of the direct tunneling, or 8-9 nm in consideration of the stress induced leakage current. Moreover, read current reduction will cause a reduction of the effective width and affect the access time [12]. To overcome the scaling limitation of Flash memory, advanced Flash memory technologies, such as SONOS (silicon-oxide-nitride-oxide-silicon), TANOS (Si-Oxide-SiN-Al_2O_3-TaN), nano-crystal and FinFETs, were proposed.

However, it is difficult to achieve long data retention because of both charge loss and direct hole tunneling for SONOS as shown in Figure 1.2 (b) [13, 14]. To solve the problems in SONOS, high-k oxide Al_2O_3 and TaN gate with high work function are utilized [15]. Figure 1.2 (c) shows a TANOS structure [16] comprising of tantalum (metal), aluminum oxide (high k material), nitride, oxide and silicon. However, the data retention of TANOS is still an issue when the device continues to scaling. Another approach is the nano-crystal device, as shown in Figure 1.2 (d). It has been extensively investigated to overcome the scaling limitation by the tunneling oxide thickness. The drawbacks of nano-crystal include the low threshold voltage shift, data retention capabilities, and the intrinsic scalability of nano-crystals [17, 18].

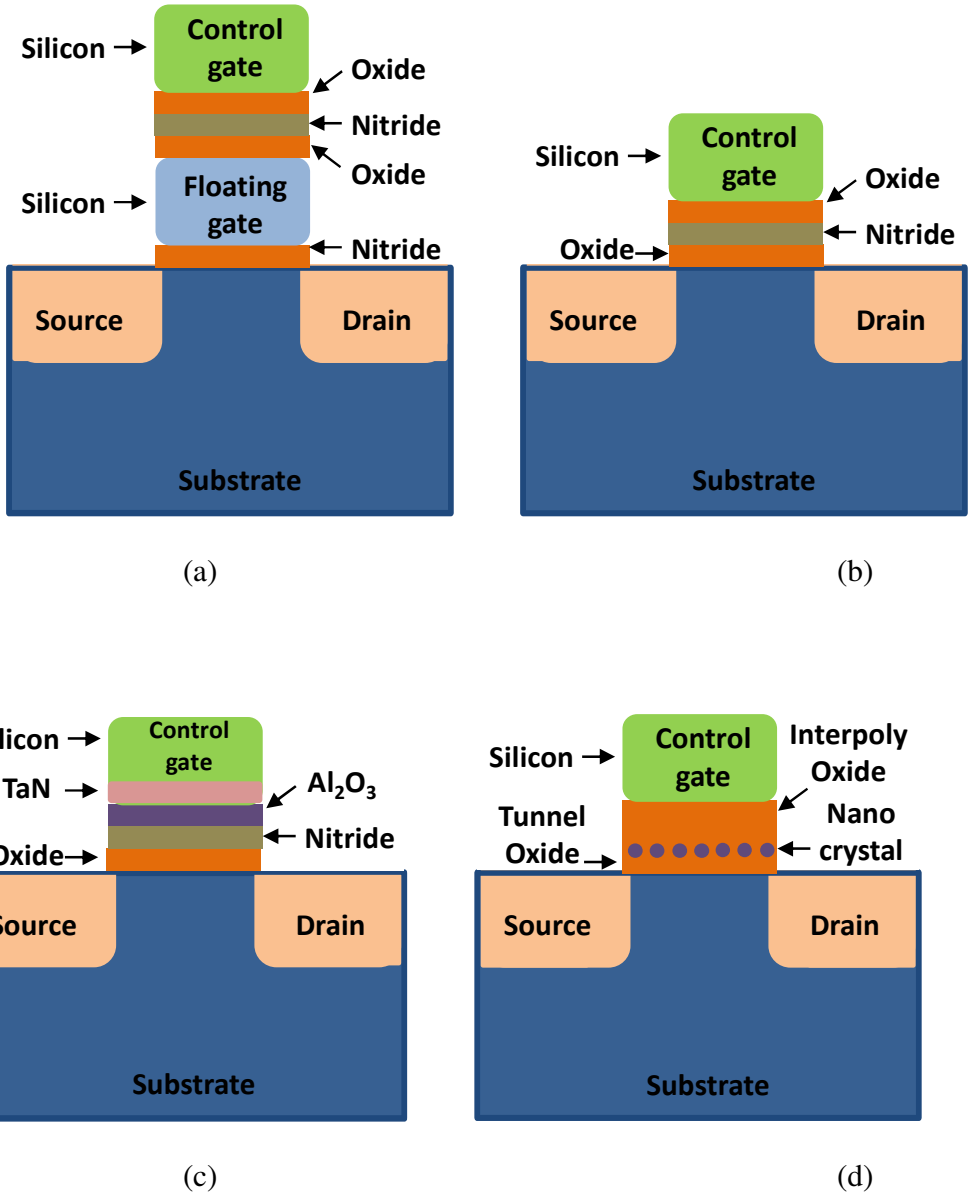


Figure 1.2 Schematic structure of (a) conventional Flash cell, (b) SONOS, (c) TANOS and (d) nano-crystal Flash cell

Beyond around 10 nm, the intrinsic limitation of electron tunneling remains a problem for the Flash memory technology. Even if SONOS Flash and nano-crystal Flash memory can be designed to improve the scalability limitation of Flash memory to further

technology nodes, neither of them is expected to significantly improve the other weaknesses of Flash memory technology, such as the slow writing speed and relatively poor cycle endurance [11, 19]. In order to achieve better device performance and scalability, alternative memory concepts other than charge-based storage are demanded to boost the NVM industry. Generally, four technologies have been widely investigated: Ferroelectric Random Access Memory (FeRAM), Spin Torque Transfer Magnetoelectric Random Access Memory (STT-MRAM), Resistive Random Access Memory (RRAM), and PCRAM [20].

FeRAM is one of the most commercially successful NVM alternatives, having been used in the Sony PlayStation 2 system. In the sandwich structure of FeRAM, ferroelectric materials are polarized spontaneously by an electrical field [21]. The polarization occurs as a lattice deformation of the cubic form, corresponding to a hysteresis loop. $Pb(Zr_xTi_{1\_x})O$, also known as PZT, which is the most popular ferroelectric material. In PZT, Ti atoms can be displaced by an electric field into two stable positions, which induces two different charges across the ferroelectric capacitor. The difference between the two charges is utilized for memory function. Furthermore, the two states are stable at a zero applied voltage.

Compared to FeRAM, STT-MRAM cell comprises of a transistor and a resistor 1T/1R [22], rather than a capacitor. The adoption of a magnetic tunnel junction (MTJ) is coupled to magneto-resistive materials that exhibit changes in the electric resistance when a magnetic field is applied. STT-MRAM has the advantages of fast writing speed, and low writing voltage. Moreover, the structure is radiation-hard with an unlimited read/write endurance, which makes STT-MRAM suitable for intensive storage

applications. However, it suffers from a small read signal and difficult process integration with CMOS.

RRAM cells generally have a capacitor-like metal-insulator-metal (MIM) structure, comprising of an insulating or resistive material 'I' sandwiched between two (possibly different) electron conductors 'M' [23, 24]. The materials 'I' are oxides or higher chalcogenides which typically show some ionic conductivity. These MIM cells can be electrically switched between at least two different resistance states, after an initial electroforming cycle, which is usually required to activate the switching property. By applying appropriate programming or write voltage pulses, a cell in the high-resistance (OFF) state can be SET to a low-resistance (ON) state, and RESET back to the OFF state. RRAM shows the advantages of low power consumption, good scalability and logic compatibility. However, the challenges for RRAM are too many materials in research, poor endurance and uniformity, and integration issues with transistor or diode.

The performances of different volatile and non-volatile memories are shown in Table 1.1 [11, 25]. From this table, it can be concluded that PCRAM is superior in speed, density, scalability, and maturity compared to the other NVMs candidates. It represents one of the best candidates for use in different NVMs applications, matching both high densities as well as high performance specifications. PCRAM further possesses multilevel storage capabilities. In the following sections, the PCRAM technology will be introduced in detail.

Table 1.1 Comparison of performances between volatile (DRAM and SRAM) and non-volatile (Flash, FeRAM, MRAM, RRAM and PCRAM) memory devices [11, 25, 26]

Memory Type	DRAM	SRAM	Flash-NOR (Embedded)	Flash-NAND (stand-alone)	FeRAM	STT-MRAM	RRAM	PCRAM
Cell type	1T1C	6T/ 4T	1T	1T	1T1C	1(2)T1R	1T1R	1T(D)1R
Cell size (F^2)	6	140	10	4	22	20	8	4
Volatility	Volatile	Volatile	NV	NV	NV	NV	NV	NV
Write cycle	>1E16	>1E16	1E5	1E4	1E14	1E12	1E12	1E9
Read time (ns)	<10	0.2	15	0.1ms	40	35	50	12
Read/ write Voltage (V)	1.8/2.5	1/1	1.8/10	1.8/15	1.5~3.3/ 1.5~3.3	1.8/ 1.8	0.15/0.6	1.2/ 3
Write/ Erase time (ns)	<10	0.2	1us/10ms	1ms/ 0.1ms	65	35	10	10/100
Direct over-write	Yes	Yes	No	No	Yes	Yes	Yes	Yes
Data retention time	64ms	long	10yrs	10yrs	10ys	>10yrs	>1yrs	>10yrs
Programming energy	Medium	Medium	High	Low	Medium	Medium	Low	Low
CMOS logic compatibility	Bad	Good	Ok, but High V need	Ok, but High V need	Ok, but High V need	OK	OK	Good
Scalability	Fair	Poor	Poor	Fair	Poor	Fair	Good	Good
Scalability limit	Capacitor	6T/ 4T	Tunnel oxide/ HV	Tunnel oxide/ HV	Polarizable capacitor	Current density	Filament	Lithography
Relative cost per bit	Low	High	Medium	Medium	High	Medium	Low	Low
Maturity	Product @ 36nm	Product @ 45nm	Product @ 45nm	Product @ 22nm	Product @ 180nm	Under development	Under development	Sample @ 20nm

1.2 Phase change random access memory

1.2.1 Phase-change materials

Phase-change materials can exist in the amorphous or crystalline phases. The two phases differ substantially in their electrical and optical properties (As shown in Figure

1.3). Generally, phase-change material has a high resistivity and low reflectivity in amorphous state, while low resistivity and high reflectivity in the crystalline state [27]. Ovshinsky was first to propose the use of these differences in properties to store information in the 1960s [28]. He demonstrated that a chalcogenide alloy $Te_{48}As_{30}Si_{12}Ge_{10}$ can be switched repeatedly between a high-conductivity state and a low-conductivity state [29]. He also proposed a large number of possible solid-state memory device configurations on the basis of phase change switching [30]. Early attempts to develop this concept into a viable storage technology were hindered as the phase change alloys showed long crystallization times in the microsecond range and required rather large switching currents in the hundred milli-ampere range [31].

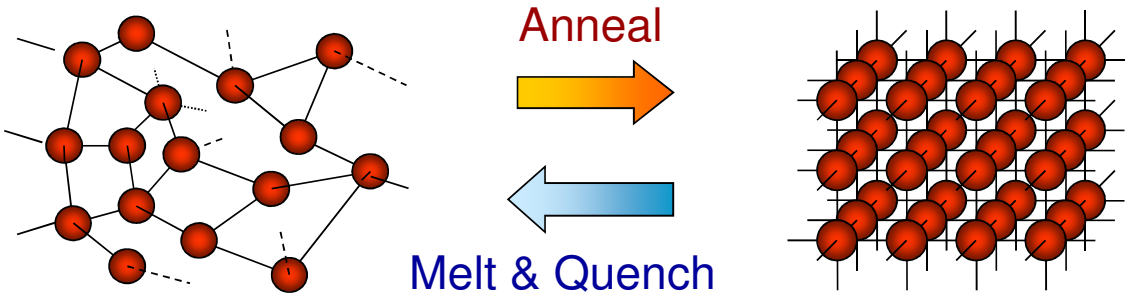


Figure 1.3 Amorphous and crystalline state change for phase change materials

Phase-change research and development received a great boost when Yamada et al [32] discovered a new class of fast-switching phase change materials in 1987. They discovered the materials on the pseudo-binary line between GeTe and Sb_2Te_3. These materials showed promising properties, which enables rewritable phase-change optical storage technology, which is still very successful today. From Figure 1.4, the

crystallization time required for the materials on the pseudo-binary line between GeTe and Sb_2Te_3 can be observed. These phase-change materials show small degradation after repeatedly write and erase cycles, and good overwriting characteristics. This can be explained by the existence of the stoichiometric compounds such as $Ge_2Sb_2Te_5$ or $GeSb_2Te_4$ on the GeTe-Sb_2Te_3 pseudo-binary composition line. These materials do not segregate easily upon repeatedly writing and erasing. This discovery renewed interests in PCRAM devices.

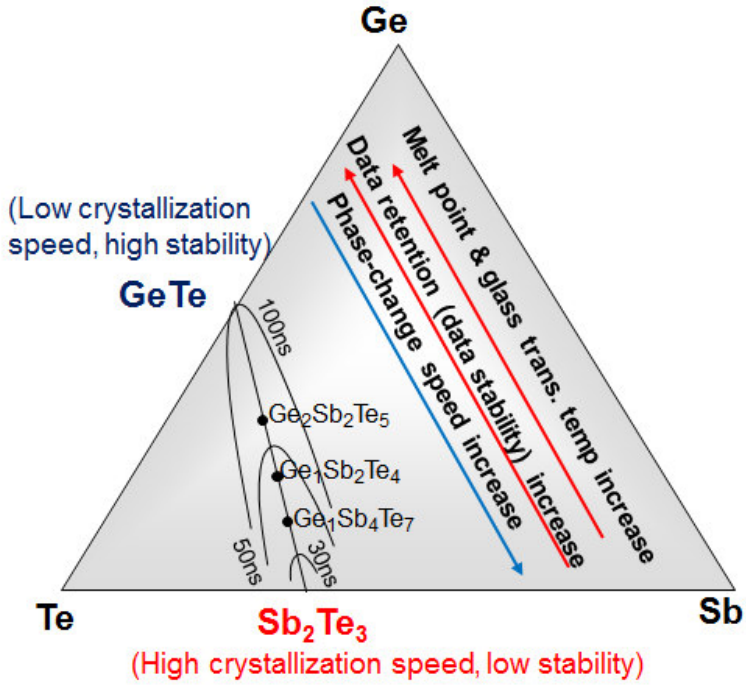


Figure 1.4 The GeTe-Sb_2Te_3 pseudo-binary system, the compounds on the line between Sb_2Te_3 and GeTe are the most popular materials used in phase change technologies

1.2.2 Principles of Phase change random access memory

PCRAM, also known as Ovonic Unified Memory, is based on the rapid reversible switching effect in chalcogenide glasses. Currently, the most popular phase-change material is Germanium-Antimony-Tellurium (GeSbTe) alloy, which is also used in optical re-writable discs. Electrical pulses are used to switch the phase-change materials between the amorphous and crystalline states. Figure 1.5 shows a conventional PCRAM cell with a mushroom-type structure. The transition from the low conductive amorphous state to the high conductive crystalline state is generally referred to as SET process, while the transition from the high conductive crystalline state to the low conductive amorphous state is referred as RESET process. From Figure 1.5, it can be seen that the small amorphous volume of phase change material in the active region acts as a programmable resistor. This amorphous region is in series with the crystalline region of the PCRAM cell and it determines the resistance of the cell between the top electrode contact (TEC) and the bottom electrode contact (BEC). The rapid and reversible structural change results in a pronounced difference in the resistivity of the phase-change material [19]. The resistivity of the amorphous and crystalline states is different. Thus, the resistance of PCRAM cell can be changed beyond 2 orders of magnitude when the device is SET or RESET. Its high and low resistances are measured and recorded as “0” and “1”.

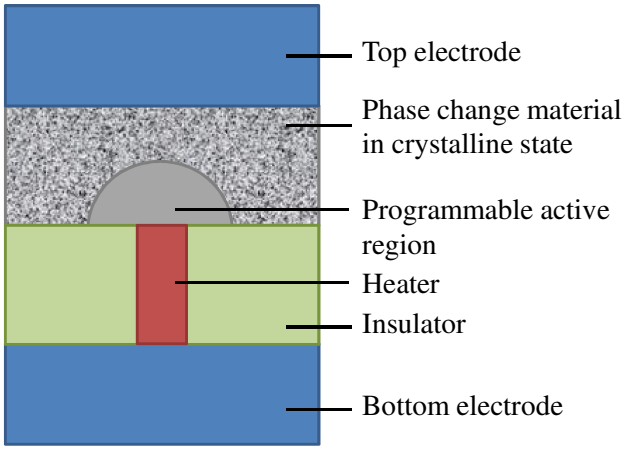


Figure 1.5 The cross-section schematic of the conventional PCRAM cell with a mushroom-type structure. The electrical current passes through the phase change material between the top electrode and heater.

During the RESET process, a short duration and high current pulse is applied to heat the phase-change material above the melting temperature. The phase-change material cools rapidly (10^9 K/s) and is quenched into the amorphous state. To convert the material back to the crystalline state, a long duration and low current pulse is used to heat the material between the crystallization temperature and its melting temperature. The duration of the SET pulse should be longer than that required to crystallize the phase-change material. Figure 1.6 shows the SET and RESET processes for a PCRAM device. A much lower current is used to read the cell.

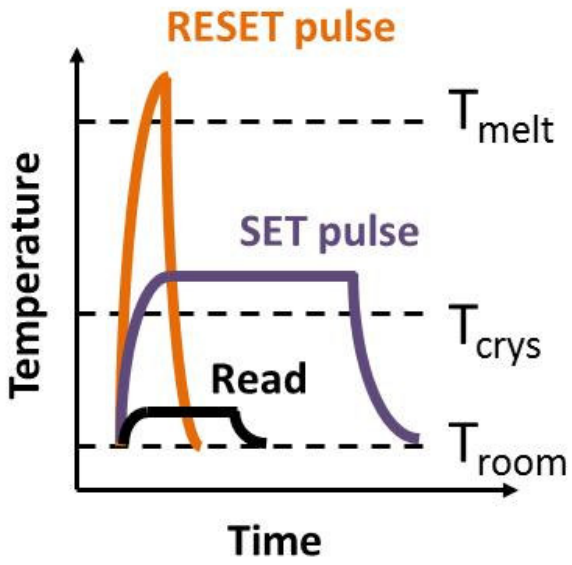


Figure 1.6 Read, SET and RESET processes of the PCRAM cell.

The I-V characteristics of PCRAM devices in the SET and RESET states are shown in Figure 1.7. The SET and RESET states have a large resistance contrast when the applied voltage is below the threshold switching voltage V_{th}. PCRAM devices have a high resistance in RESET state below V_{th} (subthreshold region). They show an electronic threshold switching behaviour at V_{th} with a negative differential resistance. If the voltage pulse removed very quickly, the PCRAM device can change back to the high resistance state. If the voltage is applied for duration longer than the crystallization time, the switching of the PCRAM cell from the RESET state to the SET state is complete and the cell resistance is low for an applied voltage larger than V_{th}. The above-mentioned electronic threshold switching effect is critical for the SET process of PCRAM devices [33-38]. This electronic threshold switching phenomenon is critical for a successful SET programming of the PCRAM devices. When the PCRAM cell is in the RESET state, the

resistance of the PCRAM cell is high and the current cannot provide sufficient Joule heat to crystallize the PCRAM cell. Under the electronic threshold switching effect, the resistance of the phase-change material changes to the dynamic resistance, which is much lower [39-42]. This enables SET programming.

For PCRAM, the RESET process consumes the largest power since the cell needs to reach the melting temperature which is much higher than the crystallization temperature. Moreover, the RESET current is also determined by various material properties, such as the resistivity and thermal conductivity, as well as the device structure. The operating speed is limited by the SET programming time because it takes a longer time to fully crystallize the amorphous region than the RESET process.

1.2.3 RESET current reduction of PCRAM

Many PCRAM memory chips have been developed and demonstrated [43-47]. During the development of PCRAM memory chips, extensive research on reliability [48-51], process compatibility [52] and scalability [53] were carried out. However, the high RESET current is still a key issue that limits the adoption of PCRAM in many applications. The high RESET current imposes stringent requirements on the current delivered by the memory cell selector that is integrated in series with the PCRAM devices. In order to provide the current required to switch the PCRAM devices, the area of the memory cell selector may not be scaled down as fast as the memory cell itself, thus the size of the cell selection device becomes the limiting factor for the device density and annihilates the scaling advantage of PCRAM technology. Therefore, reducing the RESET

current is important for achieving both high-density and low power consumption. Engineering of material aspects, device scaling and device structure have been proposed to reduce the RESET current.

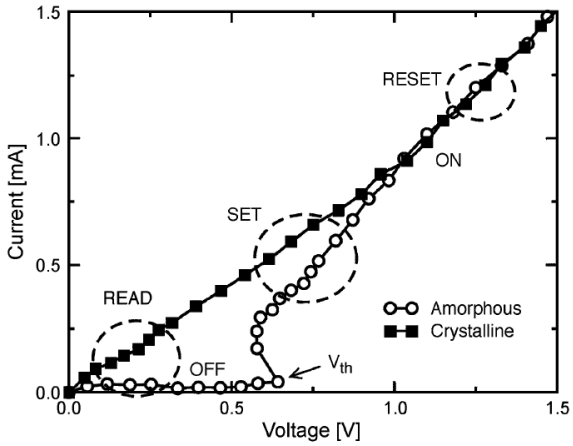


Figure 1.7 I-V characteristics of SET and RESET state of PCRAM devices. The RESET state shows switching behavior at the threshold voltage V_{th} [19].

Material engineering has been the most important approach to reduce the RESET current of PCRAM devices. Until now, a lot phase-change materials have been applied in PCRAM devices. Doping of Bismuth [54], Nitrogen [55-57], Oxygen [58], Si [59] and Si-Co [60], SiO_x [61, 62] into the phase-change materials was found to be helpful in reducing the programming current, and enhancing the device reliability. Studies on the performance of other materials or structures, such as superlattice-like phase-change structure [63-66], superlattice phase change structure [67-70], AgInSbTe [72], GeTeAsSi [73], GeTeBi [74, 75], GeSbCu/Ag [76], GeTeAs [77], In-Te [78], AsSbTe [79], SeSbTe [80], PbGeSb [81], SnGeSbTe [82], SiSb [83], $Sn_{12}Sb_{88}$ [84], Ga_2Te_3 [85], $In_3Sb_1Te_2$ [86], Ga–Sb–Te [87], $Al_{1.3}Sb_3Te$ [88] were carried out. After finding the criterion facilitates

the search for new phase-change materials [89], researchers took big steps with the ability to design novel phase-change materials [91-92].

To reduce the RESET current, the second approach is to scale down the contact area through lithography scaling to increase the heater thermal resistance [53]. The feature size of the conventional PCRAM with mushroom-type structure (As shown in Figure 1.5) is limited by lithography and process capability [53], [93].

The third method to reduce the RESET current is through innovative device structures to reduce the effective bottom electrode contact (BEC)/GST interface to the sub-lithographic regime. The edge-contact-type cell was first fabricated using a 0.24μm technology and demonstrated a very low reset current 200 μA [94]. However, this lateral structure occupies a large layout area. Later, reset current reduction using the μTrench structure was demonstrated in a 180 nm technology [95]. The contact area of the μTrench cell is defined by the vertical heater thickness (defined by film deposition) in one direction and the μTrench width in the other direction. When PCRAM device is scaled down to the 90 nm technology, the μTrench structure demonstrates a RESET current of 400 μA for a 400 nm^2 contact area [96]. Although the μTrench cell can achieve a low programming current by effectively reducing the BEC/GST area, it still requires lithography to define the GST dimension for a small contact with the underlying heater. To realize an ultrasmall lithography-independent contact area, the cross-spacer PCRAM architecture was demonstrated using a 180 nm technology [97]. By replacing the μTrench width by the thickness of both the phase-change material and the low-temperature oxide spacer sidewalls, this fully lithography-independent process leads to an ultralow reset

current of 80 μA for a 500 nm^2 cell [97]. Another issue associated with the μTrench device is the alignment tolerance.

The Wall structure, utilizing the self-aligned (SA) approach, was hence developed with a 90 nm technology [98]. The Wall structure simplifies the overall process integration by reducing one critical mask and depositing the phase-change material on a flat surface. A 200 μA reset current was obtained for a 0.0108 μm^2 cell at the 45 nm technology node [98].

The pore structure is another lithography-independent technology that gives a small contact area and low reset current [99]. The pore diameter can be accurately defined by an intentionally created keyhole with conformal deposition. A RESET current less than 250 μA was realized for a pore PCRAM cell with a patterned 40 nm diameter.

Similar to the device structures that evolve from the μTrench cells, the ring-shaped contact is another effective approach for decreasing the contact area and hence the reset current. In a ring-shaped contact cell, the current flows through the perimeter of the contact hole instead of the entire contact area. Since the area of the ring-type contact is only linearly dependent on the diameter of the contact and the thickness of the deposition metal, it not only has a linear relationship with the resolution of the lithographic capability compared to the quadratic relationship of a conventional contact, but also shows more robust characteristics against contact size variation [100, 101]. To improve the flatness of the ring-type contact (avoiding recessed core dielectrics inside the contact hole), a non-recessed ring-type contact cell was demonstrated using a 90 nm technology and it shows a 450 μA reset current for a patterned 60-nm diameter contact hole [102].

Along with the reduction of the contact area of the PCRAM cell, another way to reduce the programming current is through current localization and thermal environment optimization. Evolving from the conventional planar (mushroom) structure to the confined cell structure, the reset current is localized in the thermally isolated cell and can be significantly decreased by 65% even without contact area reduction [52]. Also, the thermal disturbance between adjacent cells is greatly improved for the confined cell, which illustrates the importance of thermal environment. Lateral PCRAM is another promising approach to achieve good thermal confinement, and low RESET current, which will be discussed in detail in the next section.

1.3 Lateral PCRAM

Recently, lateral PCRAM devices (also named as phase-change bridge memory) have attracted a lot of interest. This new structure was proposed by Philips in 2005 [103]. This lateral PCRAM has an ultrathin line of phase change material surrounded by a dielectric (SiO_2). Figure 1.8 shows their lateral PCRAM structure. Compared to a vertical PCRAM, lateral PCRAM has three advantages [103]. Firstly, it allows the removal of electrodes from the active region, hence the constraints on the thermal stability of electrode does not exist anymore. Secondly, because the active region is surrounded by the dielectric, which has a lower thermal conductivity, this lateral PCRAM dissipates less power and current. Thirdly, the fabrication involves less additional lithography steps compared to vertical type PCRAM devices.

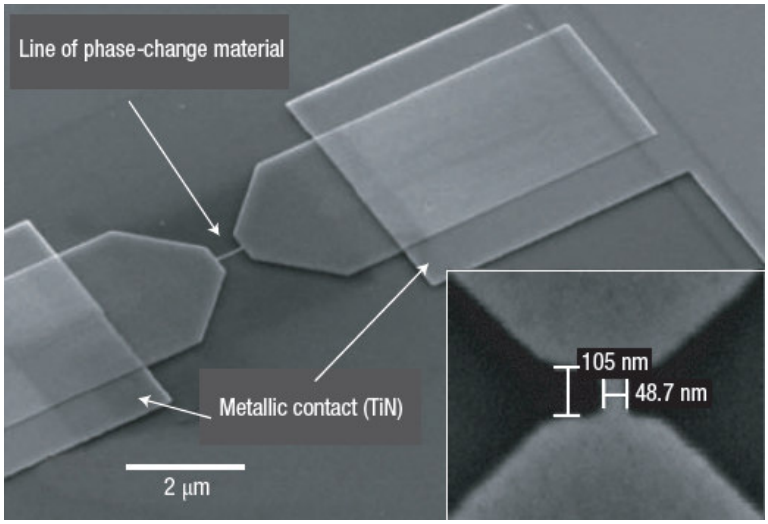


Figure 1.8 Scanning electron micrograph of a lateral PCRAM memory cell (length 500 nm, width 50 nm) made after structuring of the phase-change layer, which is done by electron-beam lithography [*103*].

With so many advantages, a lot of researchers have put their efforts on this lateral PCRAM structure. The lateral PCRAM concept was first reported in 2004 by F. Merget et al to achieve low power operation [104]. They fabricated the lateral PCRAM based on $Ge_2Sb_2Te_5$ but the cell size was very large. Hence the performance was not impressive, and only static switching was used to predict the device performance. Lateral PCRAM gained little attention until in 2005 when M. H. R. Lankhorst et al from Philips reported their first successful lateral PCRAM devices in *Nature Materials [103]*. They fabricated the lateral PCRAM device with doped-SbTe phase-change material with different line sizes. They found that the RESET current reduces as the line size decreases. For lateral PCRAM devices with lines 100×25×25nm (L×W×H), the RESET current is around 200 μA. The SET speed can be less than 100ns using growth-dominant doped-SbTe phase change material, which is much faster than the SET speed of $Ge_2Sb_2Te_5$. However, this

device only shows a lifetime of around 10^6 overwriting cycles.

In 2006, Y.C. Chen et al from Macronix reported an ultra-thin phase-change bridge (PCB) memory device using GeSb [105]. In this work, lateral PCRAM with a 3 nm thick GeSb bridge was demonstrated (As shown in Figure 1.9). The RESET current of the PCB device scales consistently with the cross-sectional area ($W \times H$) and minimum RESET current can be as low as 140 μA. Thus the phase-change bridge device provides a unique path for scaling of cross-sectional area without excessively aggressive sub-lithographic patterning. However, the overwriting cycle is limited. Only 10^5 cycles were demonstrated.

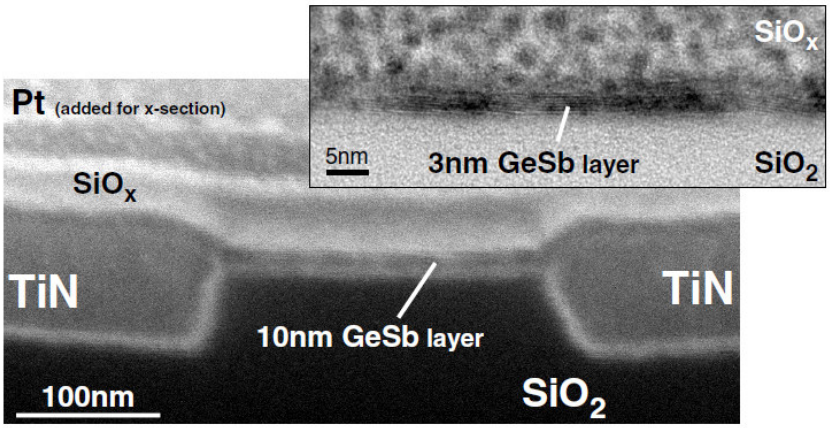


Figure 1.9 TEM of an ultra-thin PCB memory cell test structure with a 10 nm (3 nm) thick doped GeSb layer [105].

You et al reported lateral PCRAM based on N-doped Sb_2Te_3 to achieve ultralow RESET current [106, 107]. In 2007, Castro et al from NXP reported their finding of Thermo-Electric Thomson Effect in lateral PCRAM [108]. Lateral PCRAM with Indium selenide nanowire [109], GeSb nanowire [110, 111], Bi_2Te_3 Nanowires [112, 113], $Ge_2Sb_2Te_5$ nanowires [114, 115] were investigated. Lateral PCRAM based on multi-layer

SbTeN phase change was reported for multi-state storage [116-118]. Lateral PCRAM based on a $Ge_2Sb_2Te_5$ core shell hetero-structure phase change nanowire was reported as multistate memory [115]. Krebs et al reported the threshold field of phase-change materials measured using phase change bridge devices [119]. Goux et al investigated the degradation of the REST switching during endurance testing of a phase-change line cell and found that the degradation extent strongly depends on the reset pulse width but little on the reset amplitude [120]. Hong et al did the failure analysis for lateral PCRAM with $Ge_2Sb_2Te_5$ based on spectro-microscopic investigation [121]. In situ Scanning Electron Microscopy and Transmission Electron Microscopy Observation of structure change in phase change lines were also reported [122, 123]. The scaling issues of Nanowire Phase-Change Memory were investigated [124].

Carbon nanotubes have been utilized as electrodes for lateral PCRAM to achieve low programming current [125-127]. PCRAM bits with single-wall and small-diameter multi-wall carbon nanotubes (As shown in Figure 1.10) can achieve programming currents of 0.5 microampere (SET) and 5 microamperes (RESET), two orders of magnitude lower than present state-of-the-art devices. Pulsed measurements enable memory switching with very low energy consumption. However, only 200 overwriting cycle was demonstrated.

Although lateral PCRAM can achieve very low programming current and fast switching, it still shows poor lifetime although many doped phase-change materials were applied in lateral PCRAM compared to vertical PCRAM. Hence, high performances such as low power consumption, high endurance and even multi-level storage capability are needed.

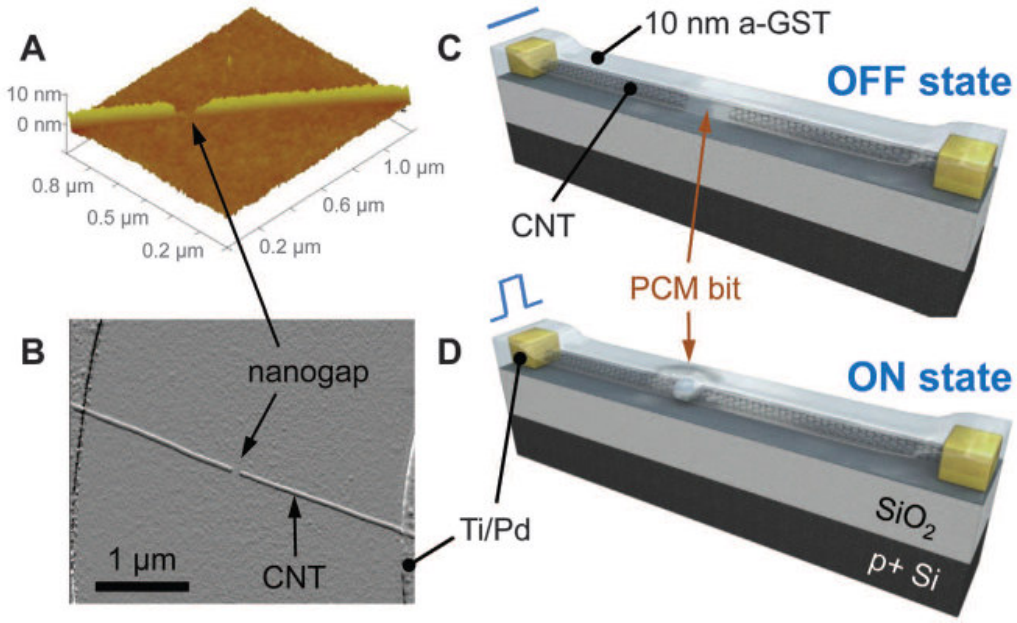


Figure 1.10 Schematics of CNT-PCRAM device. (A) AFM imaging of nanogap created after CNT breakdown under electrical stress. (B) AFM image of an as-fabricated device. (C and D) On/Off state of device obtained after deposition of GST thin film [127].

1.4 Objectives

This thesis aims to study the lifetime limitation of lateral PCRAM and achieve a high performance lateral PCRAM device. In the previous sections, the failure analysis of lateral PCRAM devices will be investigated. Through comparison of the thermal and deformation difference in confined PCRAM and lateral PCRAM devices, we will find out why lateral PCRAM devices have poor lifetime. Solutions were proposed to improve the lifetime and other aspects.

The objectives of this work are listed below:

(1) Investigating the failure issues of lateral PCRAM devices to find out the cause for the failure and providing solutions for extending the lifetime.

(2) Proposing growth-dominant superlattice-like structure phase change medium for lateral PCRAM devices to achieve longer lifetime and together with lower RESET current

(3) Proposing edge-contact lateral PCRAM structure with GeTe/Sb_7Te_3 superlattie like structure phase change medium to achieve even lower RESET current

(4) To realize multi-level storage in lateral PCRAM devices based on superlattice-like structure

1.5 Thesis organization

This thesis attempts to achieve a high performance lateral PCRAM device. The failure analysis, material engineering and structure engineering were conducted. Chapter 2 focuses on exploring the failure mode and failure analysis of lateral PCRAM. To provide a comprehensive analysis of the failure issue, both confined PCRAM and lateral PCRAM devices with the same phase change material $Ge_2Sb_2Te_5$ were fabricated. Overwriting cycle test has been done for both vertical and lateral PCRAM devices, and the failure mode was investigated. Then plastic deformation of confined PCRAM and lateral PCRAM was measured with atomic force microscopy (AFM). It was found that the plastic deformation of lateral PCRAM is much larger than that of confined PCRAM. To find the reason, simulations have been done for electrical, thermal and mechanical effects of confined PCRAM and lateral PCRAM. The simulation results show that lateral

PCRAM has better thermal confinement and heat does not conduct away easily. Hence, the temperature will increase faster as heat accumulates. The second issue for lateral PCRAM is that the phase-change material is covered by a dielectric material, while the phase change material of the confined PCRAM device is covered by a metal layer. As metals (large Young's modulus) are harder than dielectric materials (small young's modulus), the expansion of the phase-change material is larger in the lateral PCRAM devices than in the confined PCRAM devices. In consideration of the two factors, the expansion of phase-change layer in lateral PCRAM is very serious. If the expansion reaches a specific extent, atomic bonds will break in the phase-change material and plastic deformation appear, which will cause the lateral PCRAM devices fail.

The research in Chapter 2 shows that the failure mode of lateral PCRAM is "stuck SET". Plastic deformation is the possible cause of the failure. In Chapter 3, the effort is to find ideal phase-change medium that can reduce plastic deformation. Growth-dominant SLL phase-change medium is proposed for lateral PCRAM devices. GeTe and Sb_7Te_3 were employed to form the Superlattice-Like structure. The crystallization temperature of GeTe, Sb_7Te_3 and GeTe/Sb_7Te_3 superlatiice-like structure were investigated using exothermal resistance measurement. Superlattice-Like structures were designed to form with different thickness ratio of GeTe to Sb_7Te_3 for achieving optimized device performance. Lateral PCRAM devices with GeTe/ Sb_7Te_3 superlattice-like structure were fabricated and tested. Testing results showed that the lateral PCRAM devices with GeTe/ Sb_7Te_3 Superlattice-Like structure can achieve an endurance of more than 10^6, and the RESET current can be as low as 1.5mA when the thickness ratio of GeTe to Sb_7Te_3 is 1.6.

Based on the results in Chapter 3, an edge-contact lateral PCRAM with a SLL structure medium was proposed to further reduce the RESET current in Chapter 4. An thin dielectric layer was deposited on the electrodes in the edge-contact lateral PCRAM devices. The contact area was made smaller than the conventional lateral PCRAM structure. Based on simulation results, it is found that better thermal confinement was achieved for edge-contact structure. The RESET current of edge-contact lateral PCRAM can be lowered to 1.2mA.

In Chapter 5, multi-level lateral PCRAM devices were investigated. Firstly, the multi-level effect was investigated based on the lateral PCRAM devices with growth-dominant Superlattice-Like structure (the same as Chapter 3). Testing results shows that multiples states can be achieved by different programming pulses to change the volume of the active region. Heat accumulation in this lateral PCRAM device during repeated cycling affects the programming volume. Thus, the "multi-states" were not stable. Hence, a new Superlattice-Like structure incorporated with phase-change material and dielectric material was proposed to achieve discrete and stable multi-level states for lateral PCRAM devices. Lateral PCRAM devices with this new Superlattice-Like structure was fabricated and tested. Discrete intermediate states were achieved. Simulations were also done to investigate the working mechanism.

Chapter 6 summarizes the research findings of this dissertation, ranging from the failure analysis, phase change material engineering, structure engineering and multi-level investigation for lateral PCRAM. The results in this dissertation should provide a reference for the development of high performance lateral PCRAM.

Chapter 2 Failure Analyses of Lateral PCRAM Devices

2.1 Introduction

Although many phase-change materials were employed in lateral PCRAM devices, the highest endurance reported is still about 3 orders of magnitude smaller than that of vertical PCRAM [103]. Both vertical PCRAM and lateral PCRAM devices operate via the reversible switching of the phase-change material between the amorphous and crystalline states induced by electric pulses [28, 32, 92, 103, 128, 129]. But why lateral PCRAM fails much faster than confined PCRAM?

Many researchers have extensively studied the failure mechanism of vertical PCRAM devices [130-133]. The failure mode of the mushroom-type PCRAM is categorized into two types: “Stuck RESET” (Open mode failure) and “Stuck SET” (Short mode failure). The first failure mode, Stuck RESET, is observed when a PCRAM device gets stuck in a high resistance condition. This is mainly due to the void formation at the interface of bottom electrode and phase-change layer [133]. The second failure mode, Stuck SET, is observed when the resistance of a PCRAM device gets stuck in a highly conductive condition. It is believed that this failure mode is mainly caused by GeSbTe element segregation and diffusion of these elements. It was found that Ge was depleted at the bottom electrode when stuck SET occurs [133].

In this chapter, the failure mode of lateral PCRAM will be investigated. Based on the failure mode of lateral PCRAM, the cause of failure for lateral PCRAM will be investigated further. For a reference, confined PCRAM with the same phase-change material was fabricated and investigated for comparison.

2.2 Experiment

2.2.1 Experiment design

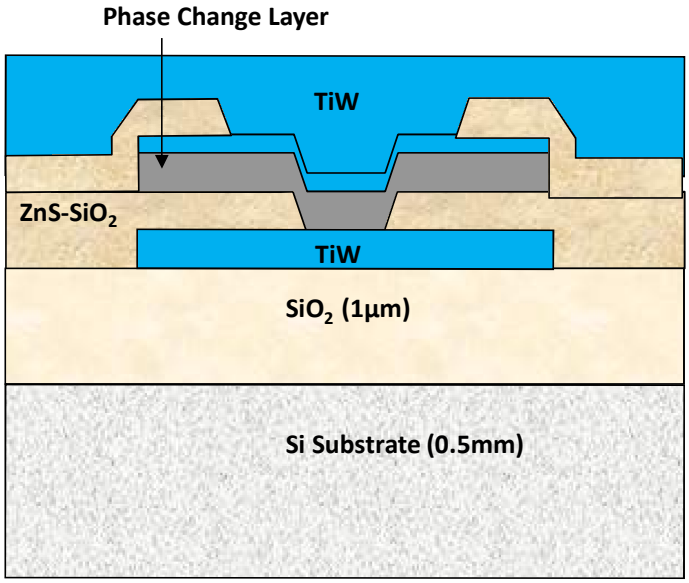
Both confined and lateral PCRAM devices were fabricated using $Ge_2Sb_2Te_5$ as phase-change material, and TiW as electrode material, with similar dimensions. The cycle endurance test of these devices was examined. Failure modes of lateral PCRAM were also investigated. As the structures of confined and lateral PCRAM are different, the thermal and mechanical effects in these devices should be different. Hence, the plastic deformation of confined and lateral PCRAM was measured with atomic force microscopy (AFM) for comparison.

2.2.2 Confined and lateral PCRAM device structure

The schematic cross-section of confined PCRAM cells is shown in Figure 2.1(a). It comprises of five layers. The bottom layer is made up of a 200 nm thick TiW electrode, on which a 100 nm thick ZnS-SiO_2 film is deposited, and etched to form a pore with diameter of 1 μm. The pore is filled with a 50 nm thick phase-change material $Ge_2Sb_2Te_5$ with a 10 nm TiW on top. TiW was used to enhance the electrical contact and prevent the phase-change material from ambient oxidization. This is followed by the deposition of a 100 nm thick ZnS-SiO_2 thin film, which is used to isolate the top electrode from the side

wall of the phase-change layer. It confines the heat and controls the thermal conditions of the memory cells. Finally, a 200 nm thick TiW top electrode is deposited to complete the structure. Figure 2.1(b) shows the top view of the completed confined PCRAM cell.

The schematics cross-section of lateral PCRAM is shown in Figure 2.2(a). The two 100 nm thick TiW electrodes were separated by 0.5 μm. A 50 nm thick $Ge_2Sb_2Te_5$ phase-change bridge covered with 35 nm ZnS-SiO_2 is formed to connect the two electrodes. The width of the phase change bridge is 1 μm. The covered ZnS-SiO_2 helps to prevent the phase-change material from ambient oxidation. Lastly, a 200 nm thick ZnS-SiO_2 was deposited to cover and protect the phase-change bridge. All devices were fabricated on silicon wafers with a 1μm thick thermal oxide. Figure 2.2(b) shows the top view of completed lateral PCRAM cell.



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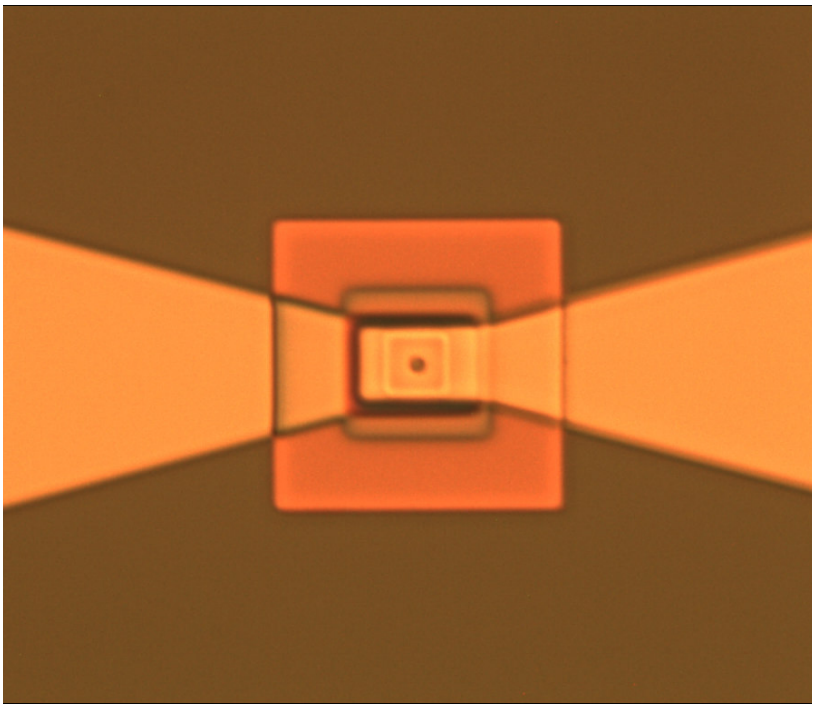
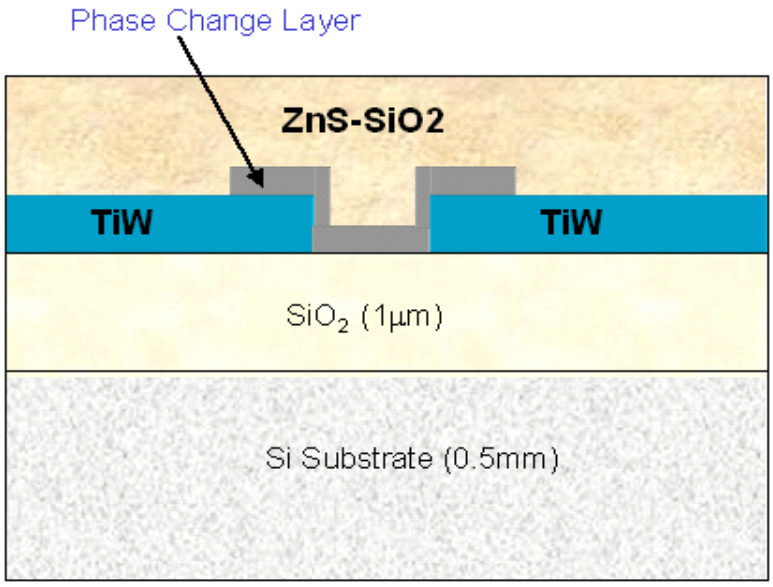
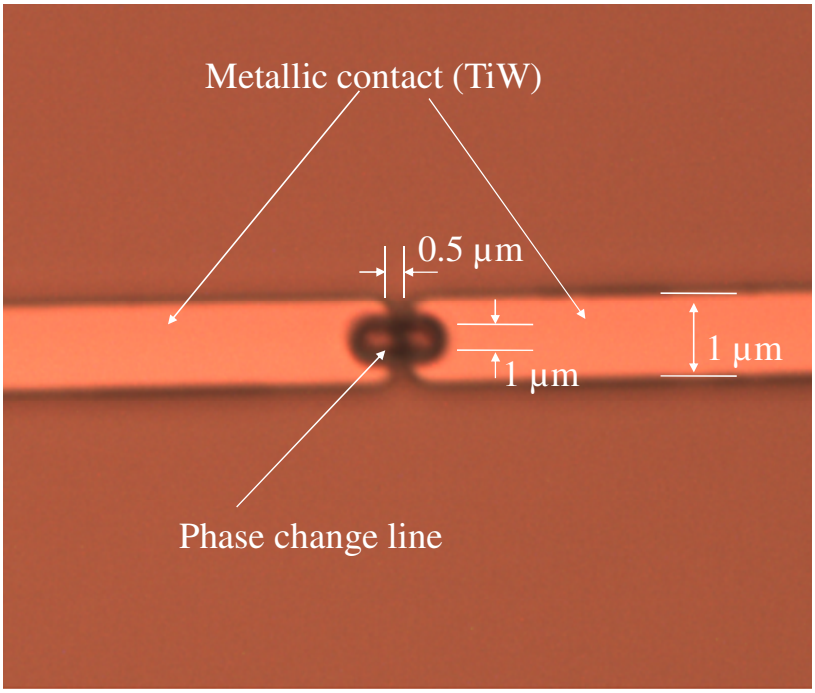


(b)

Figure 2.1 (a) Schematic cross section of confined PCRAM cell and (b) Microscope image of top view of fabricated confined PCRAM cell



(a)



(b)

Figure 2.2 (a) Schematic cross section of lateral PCRAM cell and (b) Microscope image of top view of fabricated lateral PCRAM cell

2.2.3 General fabrication process and equipments

The fabrication process for both the confined and lateral PCRAM is shown in Figure 2.3. These process steps are standard semiconductor processes. The first step involves the spin-coating of a resist on the thermal-oxide-on-silicon wafer. This is followed by the use of the i-line stepper (Canon) to expose and pattern the resist. After exposure, the wafer is developed using a developer to obtain the patterns. Physical vapor deposition (Balzers sputtering system) is used to deposit the thin films on the patterned wafer. Finally, the wafer is placed in a solution to lift-off the resist. It is further inspected under the microscope.

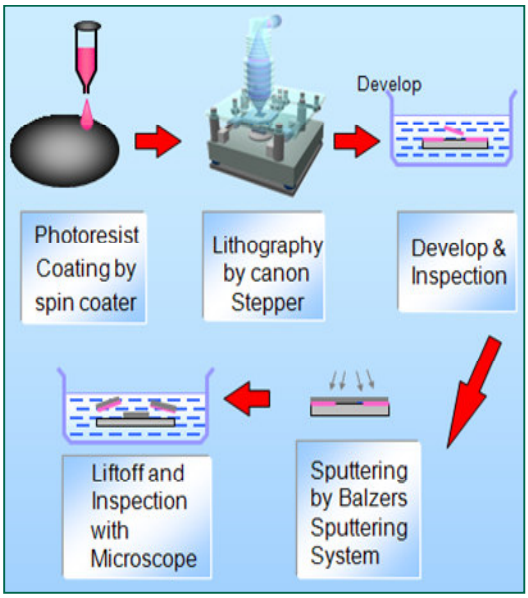


Figure 2.3 Fabrication process for both confined and lateral PCRAM devices

Lithography is the process of transferring a pattern from a mask to the substrate. The detailed procedures for lithography include HMDS (Hexamethyldisilazane) coating, photoresist coating, pre-baking, exposure, post-baking, and photoresist developing. The

Canon i-line aligner was used in lithography process. The pattern on the reticle (mask) is five times larger. A quasi-monochromatic, spatially incoherent light source is used to illuminate the mask. The source is homogenized to ensure a highly uniform intensity distribution on the plane of the mask. A condenser lens can be controlled to adjust the degree of coherence of the illuminating beam. A reduction lens collects the light transmitted through the mask, usually at a magnification of 0.2. A typical wafer can have many copies of the mask pattern as the stepper calculates the wafer size and exposes it multiple times. The Canon stepper and its main parameters are as follows (Also see Figure 2.4): wavelength is 365nm, numerical aperture (NA) is 0.52, overlay is around 0.1μm, depth of focus is 0.8 μm and resolution is around 0.5 μm. The main resist used for Canon stepper is Pfi-26A. The resist thickness is around 1.1 μm. It was obtained by spin-coating the wafer at a spin speed of 5000rpm for 45s.

i-line Stepper λ	365 nm
NA	0.52
sigma	0.6
Overlay	approx 0.1um
Depth of focus	0.8 um
field size	20 umX20 um
i- line resist	PFI-26A (1um thick @5000 rpm)
Resolution	0.5 um

(a) (b)

Figure 2.4 (a) lithography tools of Canon Stepper FPA 2000i1 and (b) its specifications and parameters

The Balzers sputtering machine was used to deposit the thin films for the confined and lateral PCRAM devices. It has three chambers where target materials can be placed (Figure 2.5). A high negative voltage is applied to the target to be sputtered. An electrical gas discharge leads to the formation of positive argon ions, which would be accelerated in the direction of the coating material. The colliding positive ions would knock off atoms from the surface of the target material, which would be deposited on the surface of the sample. Chamber 1 and 3 are the DC sputtering chambers for metal or semiconductor material while chamber 2 is the RF sputtering chamber for dielectric materials. The highest power for the sputtering is 5 kW.

With the three sputtering chambers, three different films can be deposited with Balzers sputtering system. Many targets are available, such as metals (TiW, W, Cu, TiAl, Al, Cr, Au, Ag), dielectrics (SiO_2, Si_3N_4, ZnS-SiO_2, SiC), and semiconductors (Ge, GeTe, Sb_2Te_3, Sb_7Te_3, $Ge_2Sb_2Te_5$). To fabricate the confined and lateral PCRAM devices, $Ge_2Sb_2Te_5$, ZnS-SiO_2 and TiW were deposited from chambers 1, 2 and 3 of the Balzers sputtering system respectively. The deposition condition and deposition rate of these materials are listed in Table 2.1.

Table 2.1 Thin film deposition conditions for the Balzers sputtering system

Chamber	Target	Sputtering Power (kW)	Ar flow rate (sccm)	Deposition Rate (nm/s)
1	$Ge_2Sb_2Te_5$	0.15	15	1.832
2	$(ZnS)_{0.2}$-$(SiO_2)_{0.8}$	1	15	2.105
3	Ti_3W_7	0.5	20	1.537

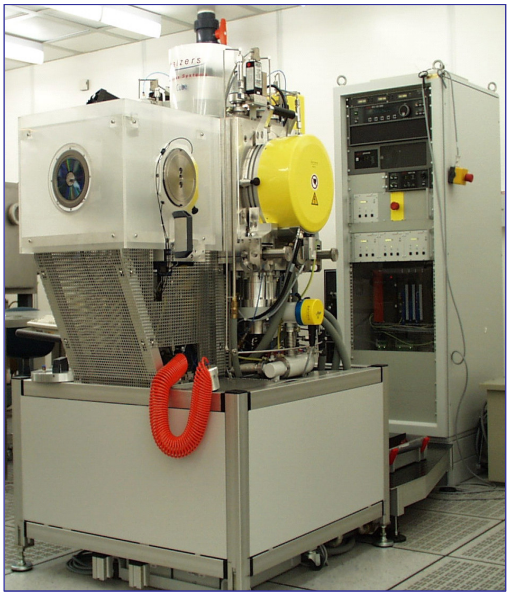


Figure 2.5 Thin film deposition tool using the Balzers Cube Sputtering System

2.2.4 Cycle endurance of confined and lateral PCRAM devices

The PCRAM tester was used to characterize the electrical performance of the PCRAM devices. The schematic diagram of the PCRAM tester can be seen in Figure 2.6. The main circuit components include pulse generator, oscilloscope and test board. The pulse generator controls the duration and amplitude of applied pulse. The pulse duration and voltage amplitude can be varied from 5 to 900 ns, and 0 to 14V, respectively. Using this tester, the SET, RESET and endurance cycle tests can be conducted.

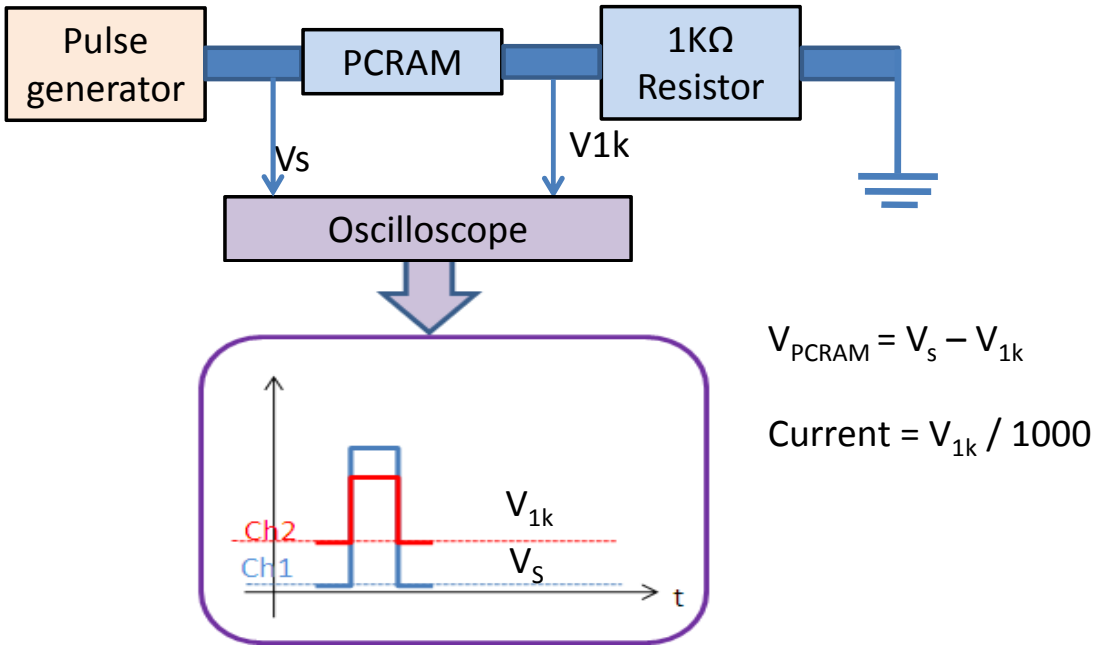


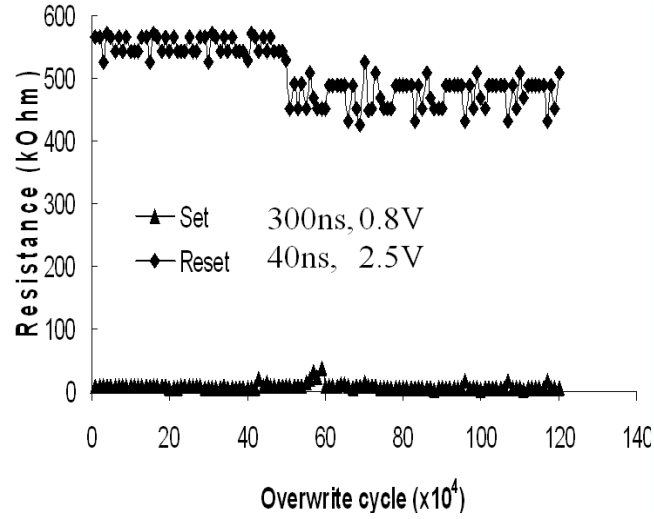
Figure 2.6 Schematic diagram of the testing system

Cycle endurance tests were conducted for both the confined and lateral PCRAM devices using the above-mentioned PCRAM tester. The optimized SET and RESET pulse conditions were obtained for both the confined and lateral PCRAM devices. For confined PCRAM, the SET pulse of 300 ns/0.8V and RESET pulse of 40 ns/2.5V were applied, respectively. The endurance test results for confined PCRAM are shown in Figure 2.7(a). From the figure, it can be seen that the endurance of confined PCRAM device exceeds 10^6. Further studies shows that the endurance cycle of confined PCRAM with $Ge_2Sb_2Te_5$ can reach about 10^8 to 10^9 and the devices fail in stuck SET mode [134]. For lateral PCRAM, the optimized SET and RESET pulses were 200 ns/1.2 V and 60 ns /6.5 V, respectively. The endurance test results are shown in Figure 2.7(b). The lifetime of the lateral PCRAM device with $Ge_2Sb_2Te_5$ is poor. The lateral PCRAM can only switch for about one hundred times, before getting stuck in SET state. It cannot be further switched

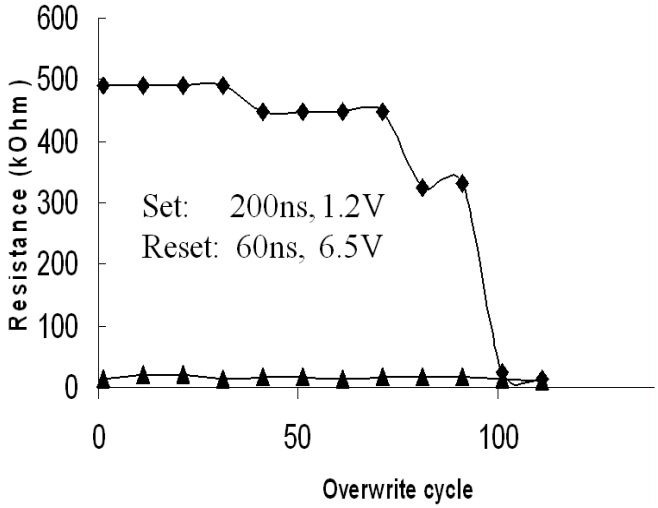
to the RESET state. To check the plastic deformation of lateral PCRAM device, the SET and RESET pulses were continued to apply after it failed.

The materials used in the vertical and lateral PCRAM devices are the same. But only their structures are different. With the different structure between vertical and lateral PCRAM devices, the thermal and mechanical effects of these devices during writing/erasing should be different. It is very difficult to measure the thermal profile inside the confined PCRAM and lateral PCRAM devices. However, the plastic deformation can be measured with an atomic force microscopy (AFM).

There are two types of deformation: elastic deformation and plastic deformation. Elastic deformation involves the stretching of the atomic bonds, which do not break. When elastic deformation reaches the elastic limit, plastic deformation occurs. Plastic deformation involves the breaking of atomic bonds by the movement of dislocations [135, 136]. That means that the emerging of plastic deformation may accelerate the failure of PCRAM devices. Thus, it is important to study the plastic deformation in the phase-change layer of vertical and lateral PCRAM devices.



(a)



(b)

Figure 2.7 Cycle endurance of (a) confined and (b) lateral PCRAM devices

2.2.5 Plastic deformation measurement for confined and lateral PCRAM devices

Atomic force microscopy (AFM) was employed to study the plastic deformation of phase-change layer in PCRAM devices. AFM was first developed by Binnig and

Gerber (IBM), and Quate (Stanford) in 1986. The mechanism is based on the measurement of the atomic forces between the probe (cantilever tip) and the sample by using a laser to detect lever motion. There are two kinds of scanning modes: contact mode and tapping mode. For contact mode, the image is formed by scanning and using feedback loop to maintain constant tip-sample force during scanning. For tapping mode, the image is formed by scanning and using feedback loop to maintain constant tip oscillation during scanning. Figure 2.8 shows the schematic of the AFM setup. AFM can characterize both insulators and conductors down to the nanometer resolution.

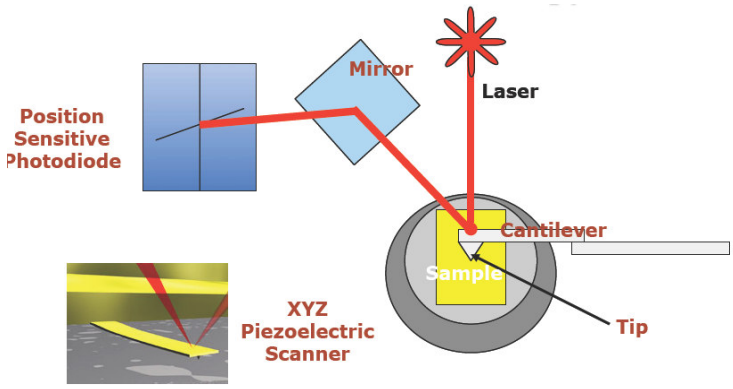


Figure 2.8 Schematic of the AFM setup

During scanning, a probe is bought in close proximity to the surface. The force is detected by the deflection of a spring, usually a cantilever (diving board). Forces between the probe tip and the sample are sensed to control the distance between the tip and the sample. The AFM uses a sharp tip attached to the end of a cantilever to raster scan across an area, while the laser and photodiode are used to monitor the tip force on the surface. A feedback loop between the photodiode and piezo-crystal maintains a constant force during contact mode, and constant amplitude during intermittent contact mode.

At short probe-sample distances, the forces are repulsive. At large probe-sample distances, the forces are attractive. The AFM cantilever can be used to measure both attractive and repulsive forces. Using attractive interaction between the surface and the tip, the non-contact mode is operated within the van der Waal radii of the atoms. The oscillating cantilever is kept near its resonant frequency (~ 200 kHz) to improve sensitivity. Figure 2.9 shows the DI3100 AFM system.

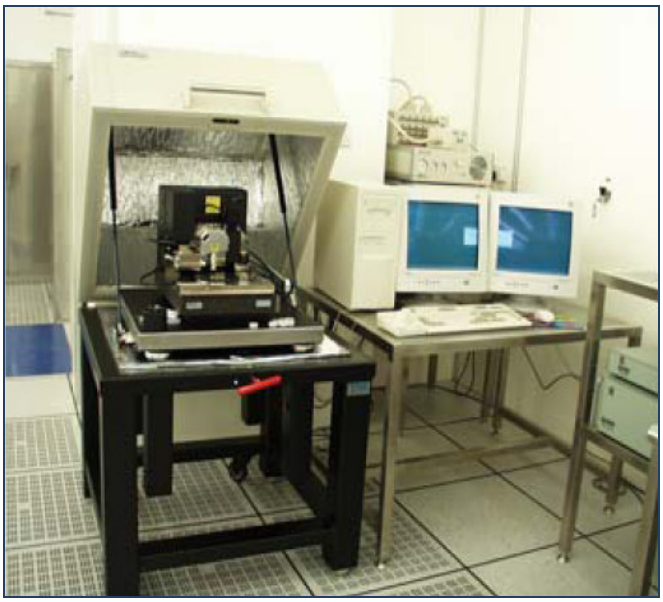
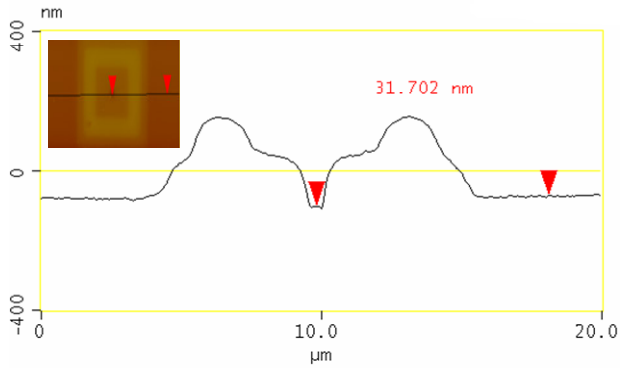
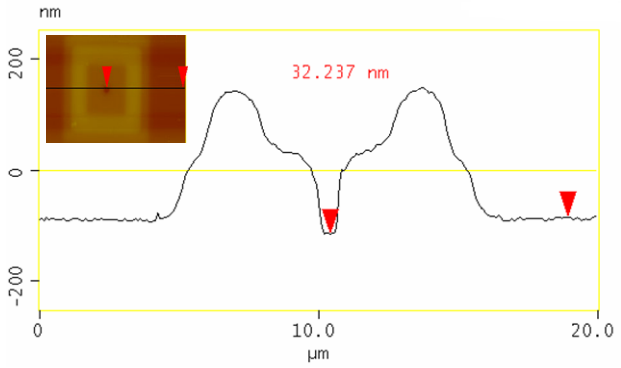


Figure 2.9 Atomic force microscopy of DI 3100 system

Plastic deformation of phase-change layer in the confined and lateral PCRAM devices was measured using the AFM after similar level endurance cycles. The plastic deformation of both devices was measured after 0, 10^3 and 10^6 overwriting cycles respectively. Figure 2.10 shows the measured AFM profiles of confined PCRAM device after 0 and 10^6 cycles. It can be observed that the plastic deformation is very small and can be ignored after 10^6 endurance cycles for confined PCRAM.



(a)



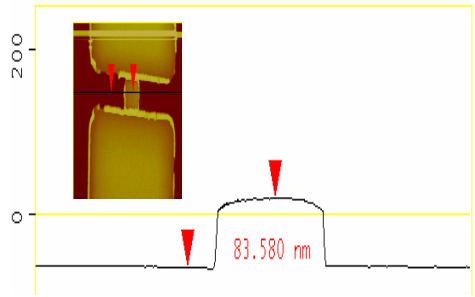
(b)

Figure 2.10 Profile of confined PCRAM device after (a) 0 and (b) 10^6 overwriting cycles

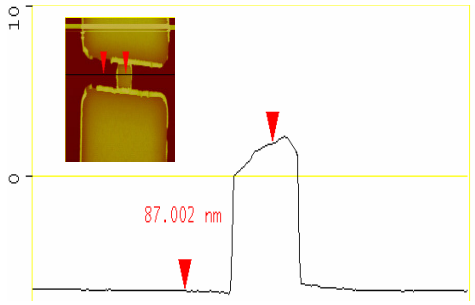
However, the plastic deformation of phase-change layer for lateral PCRAM devices reached about 4 nm after 10^3 overwriting cycles. After 10^6 overwriting cycles, the surface of phase change layer became extremely rough, and the plastic deformation reached up to 56 nm (see Figure 2.11). It can be observed that the plastic deformation increases and accumulates with more overwriting cycles.

Comparing the measured plastic deformation in the confined and lateral PCRAM devices, it can be concluded that the plastic deformation in lateral PCRAM devices is

much larger than that in confined PCRAM devices undergoing with the same overwriting cycles.



(a)



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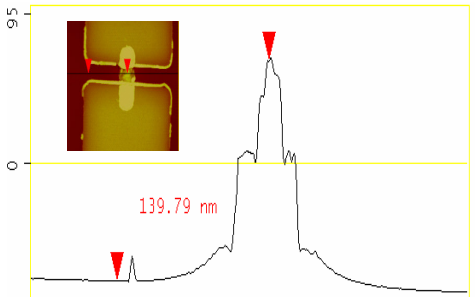


(c)

Figure 2.11 Profiles of the phase-change line for lateral PCRAM devices after (a) 0, (b) 10^3 and (c) 10^6 overwriting cycles

2.3 Modeling and Simulation

To examine the factors dominating the lifetime of confined and lateral PCRAM devices, thermo-mechanical simulation and analysis were performed using finite element method (FEM). The thermal effect and elastic deformation of confined and lateral PCRAM during repeated cycling were studied. If the elastic deformation exceeds the elastic limit, plastic deformation occurs. Hence, the investigation of elastic deformation can be used to qualitatively analyze which device structure has a larger plastic deformation. The thermo-mechanical modeling of PCRAM is described in the following section.

2.3.1 Simulation model

The thermal model can be expressed by fundamental equations based on the linear transient thermal conduction [137], as follows:

$$\rho c \frac{\partial T}{\partial t} - \frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right) - \frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right) - \frac{\partial}{\partial z}\left(k_z \frac{\partial T}{\partial z}\right) - Q = 0 \tag{2.1}$$

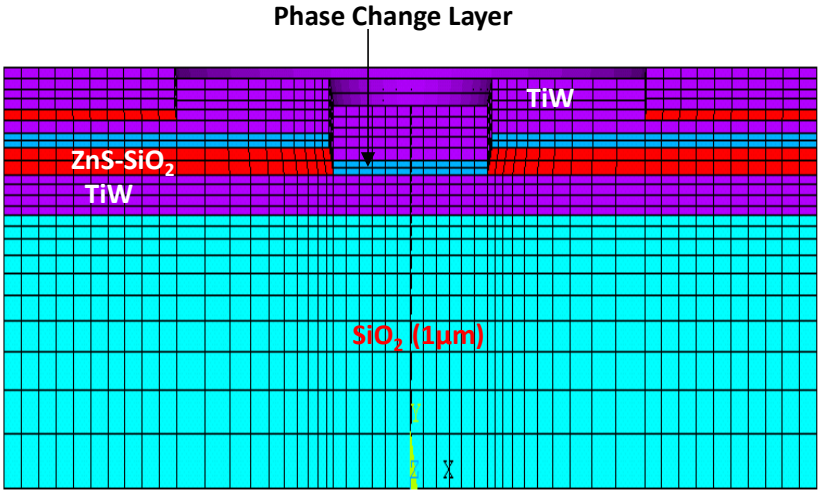
where ρ is density; c is specific heat; T is temperature; k_x, k_y, k_z are thermal conductivities in three dimensions; Q is the Joule heat per unit volume and per unit time, which is called heat density; t is time; x, y, z are coordinates. It can be further simplified into a static field analysis since the voltage applied on the electrodes remains unchanged. In the static field analysis, the Joule heating density distribution can be described as:

$$Q = \frac{1}{n}\sum_{i=1}^{n}[\sigma]\{j_i\}\{j_i\} \tag{2.2}$$

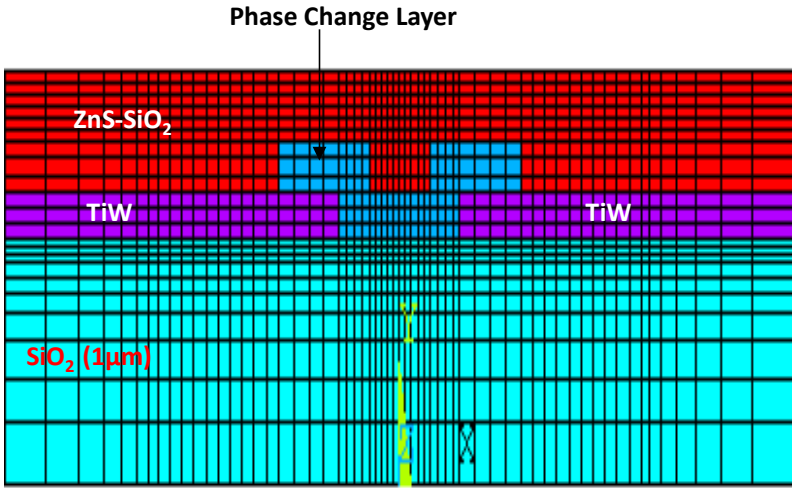
where n is the number of integration points, $[\sigma]$ is the resistivity matrix and $\{J_i\}$ is the total current density in the element at integration point i.

2.3.1 Simulation conditions

The RESET process was simulated because it requires a higher input energy than the SET process for device operation. It is essential to examine the thermal and mechanical effects of phase-change materials heated to melting point in both confined and lateral PCRAM devices with the same materials. For confined PCRAM, the boundary condition imposed on the top surface of the top electrode, and the bottom of the 1 μm thick SiO_2 was set to 27°C. For lateral PCRAM device, the boundary condition imposed on the surface of the top dielectric and the bottom of the 1 μm thick SiO_2 was set to 27°C. Prior to applying the voltage pulse, both the confined and lateral PCRAM devices were assumed to be in thermal equilibrium with its surroundings. Figure 2.12 shows the finite element model of the confined and lateral PCRAM devices. The model size is about the same as the fabricated devices.



(a)



(b)

Figure 2.12 Finite element models for (a) confined and (b) lateral PCRAM.

In this simulation, three overwriting cycles were simulated. To simplify the simulation, each overwriting cycle was comprised of a 50 ns RESET pulse, followed by a 50 ns cooling time (to replace SET pulse). The schematic of these pulses are plotted in

Figure 2.13. With the simulation of three overwriting cycles, the thermal and deformation accumulation effects can be investigated.

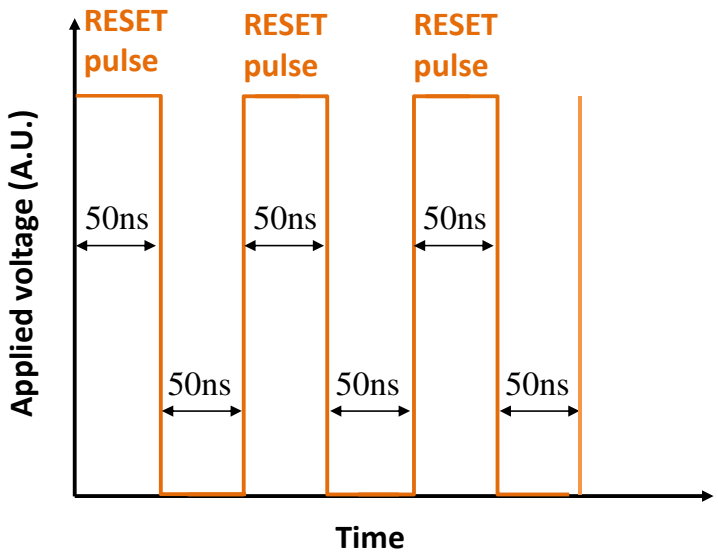


Figure 2.13 Three overwriting cycles with 50ns RESET pulse and 50ns cooling time.

The thermal properties of the materials were assumed to be independent of temperature. The electrical properties of the materials in the structure were also assumed to be isotropic homogeneous and independent of temperature. Latent heating is not considered because it is much smaller than Joule heating. The details of material properties are listed in Table 2.2 [137, 138].

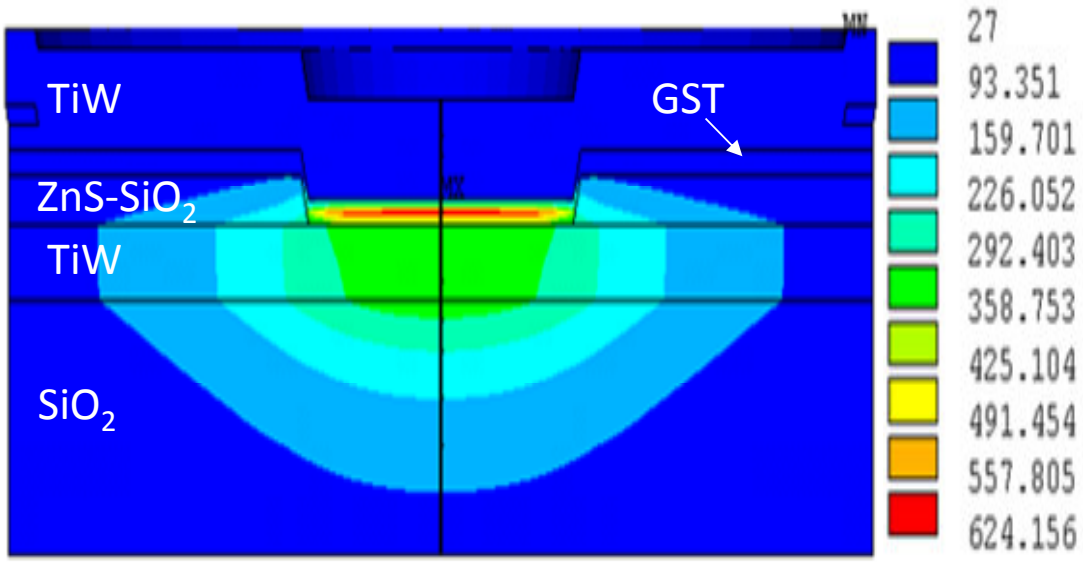
Table 2.2 Properties of materials used in PCRAM devices

Material type	Density (Kg/m^3)	Thermal Conductivity (J/mKs)	Heat Capacity (J/KgK)	Resistivity (Ωm)	Elastic Modulus E (GPa)	Poisson Ration ν	CTE (10^{-6}/ K)
SiO_2	2648	1.4	1171	1.2×10^{18}	25	0.21	6.5
TiW	14828	21	137	7×10^{-7}	450	0.18	9.1
$Ge_2Sb_2Te_5$	6150	0.5	210	1.773	30	0.19	18
ZnS-SiO_2	3650	0.21	560	$1x\ 10^{17}$	20	0.33	6.3

CTE: coefficients of thermal expansion

2.3.2 Thermal effect in confined and lateral PCRAM devices

The simulated temperature distributions in the confined and lateral PCRAM devices were obtained. Figure 2.14(a) shows the cross-section view of the temperature distribution in the confined PCRAM device after activation by 3rd RESET pulse. From Figure 2.14(a), it can be observed that the high temperature region (red colour) is mainly confined inside the phase-change layer. In the confined PCRAM device structure, Joule heating raises the temperature within the phase-change layer, with the peak temperature located near the center of the phase-change region. As the phase change layer is only 50 nm thick, the active region is very near to the electrodes. The TiW metal electrodes have high thermal conductivity, which can rapidly conduct heat away from the phase-change layer. It can be observed that the temperature inside the top electrode is very low. Compared to top electrode, the temperature inside bottom electrode is higher. This is because the top electrode conducts heat to the top surface boundary while the bottom electrode conducts heat towards the bottom thermal oxide. Hence, heat conduction through the top electrode will be much faster. After the simulated three overwriting cycles, the cross-section view of the temperature distribution for confined PCRAM device can be seen in Figure 2.14(b). It is noted that heat dissipated rapidly within 50ns. The peak temperature drops from 624^{o}C to 170^{o}C. More importantly, the zone with the highest temperature is moved towards the bottom electrode and the thermal oxide. As the temperature within the phase change material already drops to almost baseline temperature, the heat accumulation will not affect the next RESET pulse much.



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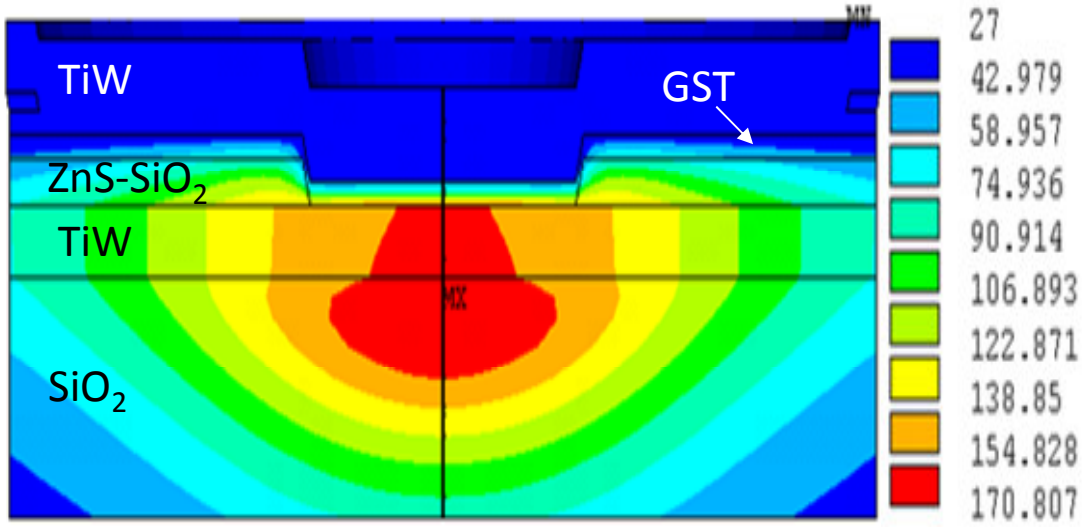
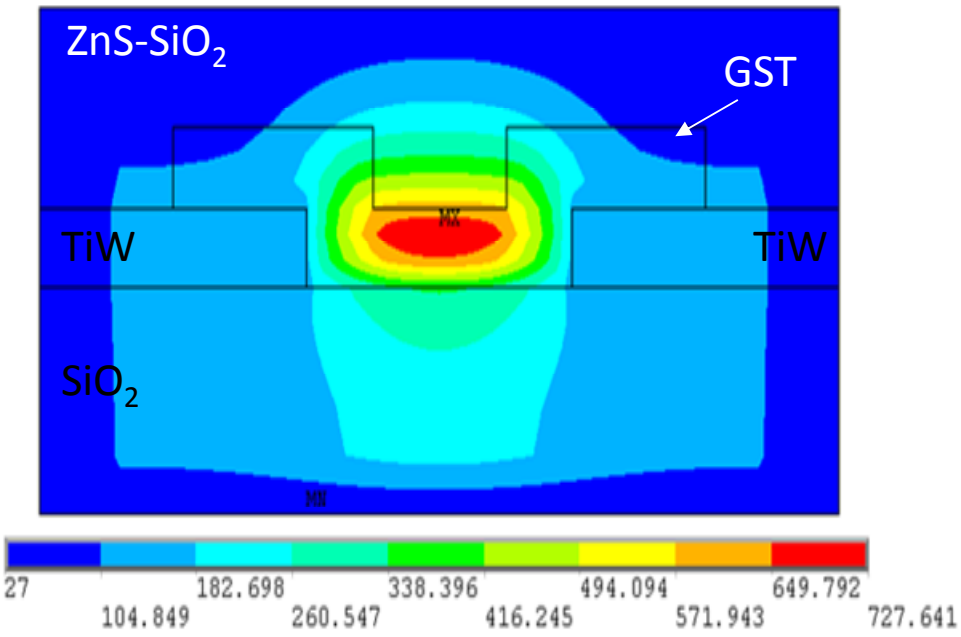


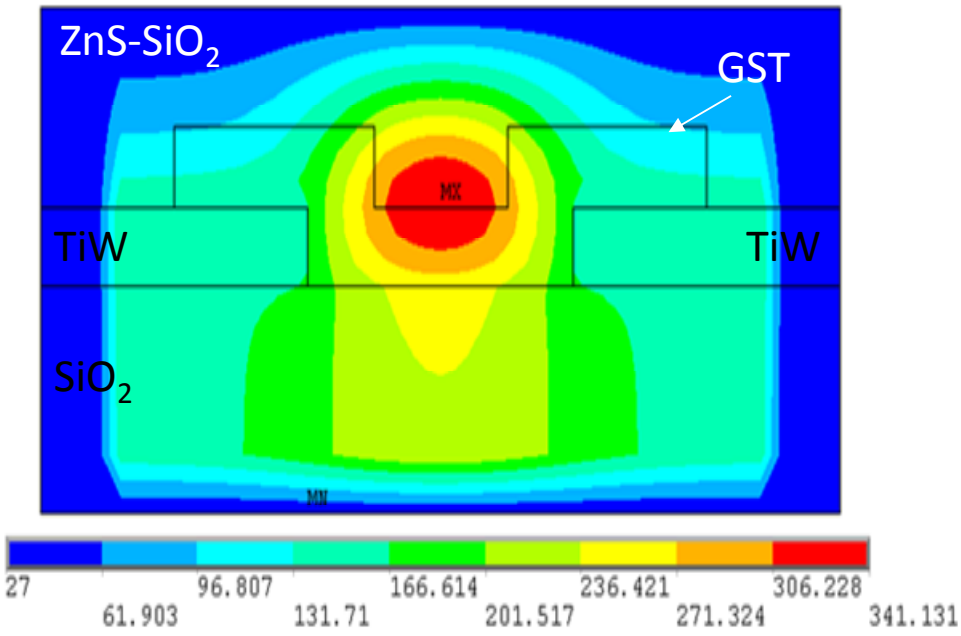
(b)

Figure 2.14 Temperature distributions in the confined PCRAM device after (a) the 3rd RESET pulse and (b) 3rd cooling pulse.

Compared to the confined PCRAM device, the lateral PCRAM device shows a different thermal distribution. Figure 2.15 (a) shows the cross-section view of the temperature distribution in a lateral device after the 3rd RESET pulse. From Figure 2.15 (a), it can be observed that the high temperature region (red colour) is mainly confined inside the phase-change layer during RESET pulse. In the lateral PCRAM device structure, Joule heating raises the temperature within the phase-change layer, with the peak temperature located near the top interface between the phase-change layer and the ZnS-SiO_2 dielectric surface. The high temperature region is located further away from two TiW electrodes, and near to dielectric materials. Hence, the heat dissipates away mainly through top and bottom dielectrics. The ZnS-SiO_2 dielectric and thermal oxide have low thermal conductivities, which cannot conduct heat away easily. It is observed that the temperature inside the top dielectric is very high. This is because the top dielectric ZnS-SiO_2 has a lower thermal conductivity than the thermal oxide. After the third RESET and cooling cycles, the cross-section view of the temperature distribution in the lateral PCRAM device can be seen in Figure 2.15(b). It is noted that heat cannot be dissipated within 50ns. The peak temperature drops from 727^{o}C to 341 ^{o}C. More seriously, the zone with the highest temperature is still located inside the phase-change layer. Hence, heat accumulation will affect next RESET pulse. This can be solved if the interval between two writing pulse is long.



(a)

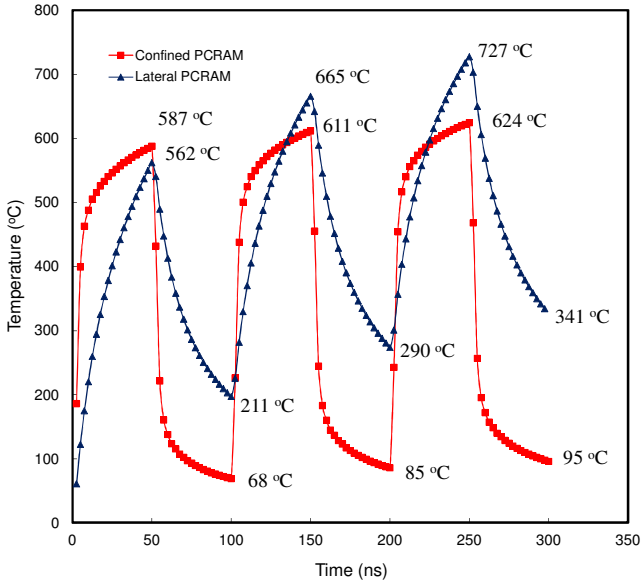


(b)

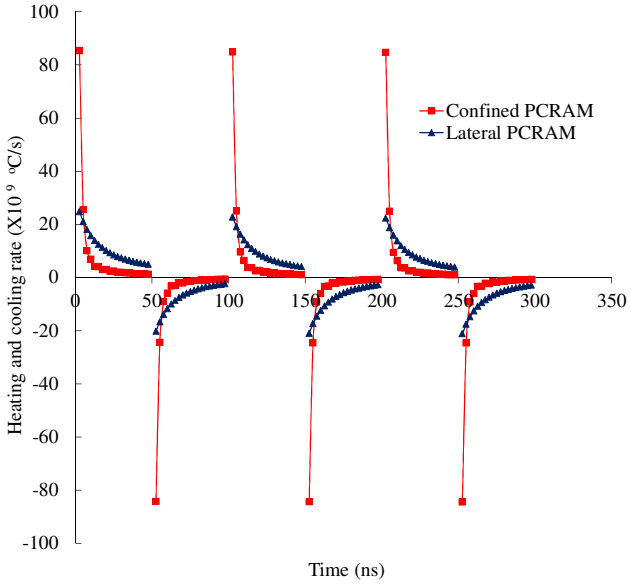
Figure 2.15 Temperature distributions in the lateral PCRAM device after (a) the 3rd RESET pulse and (b) the 3rd cooling pulse.

To investigate the heat accumulation effect inside the phase-change layer, the temperature profiles, heating rates, and cooling rates for the active region are plotted in Figure 2.16. It is found that the heating and cooling rates for the confined PCRAM are about 4 times higher than that of the lateral PCRAM devices. The peak heating rates for the confined and lateral PCRAM devices are 8.53×10^{10} and 2.48×10^{10} ^{o}C/s, respectively. At the same time, the peak cooling rates for the confined and lateral PCRAM devices are 8.42×10^{10} and 2.03×10^{10} ^{o}C/s, respectively. The large difference for the confined and lateral PCRAM devices was mainly caused by the different device structures. For confined PCRAM, the active region of phase-change material is sandwiched by metal layers. The metal layers have better thermal conductivity, and can conduct the Joule heat faster. For the lateral PCRAM device, the distance between the active region and the metal electrode is much larger and Joule heat is mainly dissipated into the top and bottom dielectric layers. As the thermal conductivity of the dielectric material is much lower than that of the metal electrode, the heating and cooling rates for the lateral PCRAM device are much slower than those of the confined PCRAM device. Hence, for lateral PCRAM device, heat cannot dissipate quickly. Heat accumulates and the temperature in the device increases with more overwriting cycles. The peak temperatures in the lateral PCRAM device for the three consecutive writing are 562, 665 and 727^{o}C respectively. For the confined PCRAM device, the temperature distribution profile is more uniform during overwriting cycles due to higher heating and cooling rates. The peak temperatures of the confined PCRAM device for the three consecutive cycles are 587, 611 and 624^{o}C respectively. Comparing the peak temperature of the confined and lateral PCRAM

devices during overwriting cycles, it can be seen that the temperature increment in the lateral PCRAM device is more than that of the confined PCRAM device.



(a)



(b)

Figure 2.16 (a) Temperature profiles, and (b) heating and cooling rates in the active region of the confined and lateral PCRAM devices for 3 overwriting cycles.

2.3.3 Deformation effect and analysis

To compare the thermal elastic deformation in the confined and lateral PCRAM devices, the temperature of active region was set to the melting point of 600^{o}C. High temperatures in the phase-change layer can result in the expansion of the confined and lateral PCRAM devices. The simulated thermal elastic deformation results are shown in Figure 2.17. It can be seen that the thermal elastic deformation of the active region in the lateral PCRAM device is about 3 times larger than that of the confined PCRAM device. For the confined PCRAM device, the deformation is in the in-plane direction, while for the lateral PCRAM device, the deformation is in the cross-plane direction. This is due to the elastic modulus of the TiW metal electrode being much larger than that of the ZnS-SiO_2 dielectric [138]. It implies that the phase-change layer is covered by a hard material in the confined PCRAM device, but is covered by a soft material in the lateral PCRAM device. Hence, it is easier for the phase-change layer to expand vertically in the lateral PCRAM device than in the confined PCRAM device.

As mentioned above, deformation is elastic and reversible unless the elastic limit is exceeded. Plastic deformation occurs when the elastic limit is exceeded. For the confined PCRAM device, the peak temperature is very uniform during overwriting cycles, and the elastic deformation is very small. Hence, elastic deformation in the confined PCRAM device will remain at a small level even with more overwriting cycles. It will be very difficult to exceed the elastic limit for the confined PCRAM device. For the lateral PCRAM device, the peak temperature increases rapidly with cycling and the elastic deformation is large even under 600^{o}C temperature load. Therefore, the elastic deformation in the lateral PCRAM device will increase very fast with continuous cycling.

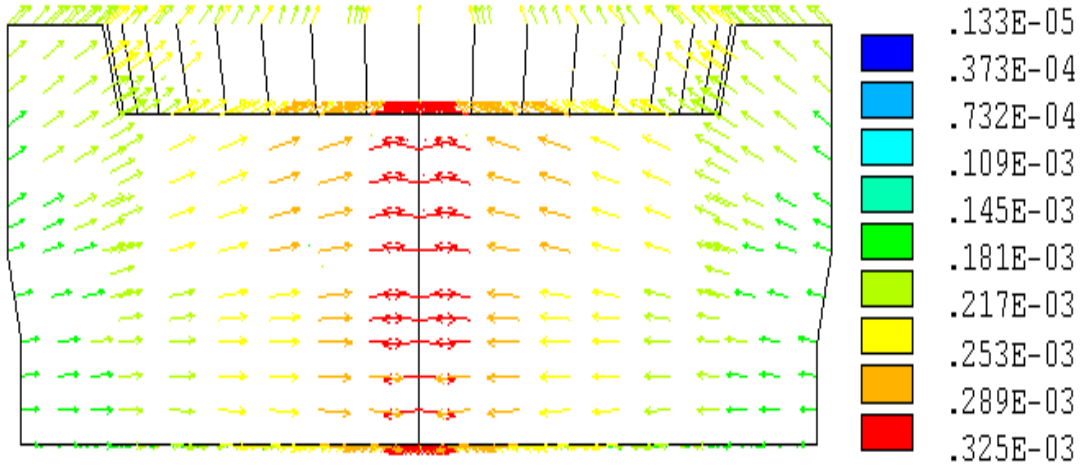
It is much easier for the elastic deformation in the lateral PCRAM device to exceed the elastic limit than that in the confined PCRAM device with overwriting cycles. When the elastic limit is exceeded, plastic deformation of the lateral PCRAM device occurs, and accumulates with overwriting cycles. The deformation is irreversible. As the deformation in the lateral PCRAM device is in the vertical direction, "swelling" of the bridge in the lateral PCRAM device will emerge when plastic deformation accumulates. This result is in good agreement with the AFM measurements for the lateral PCRAM device.

2.4 Failure analysis of lateral PCRAM devices

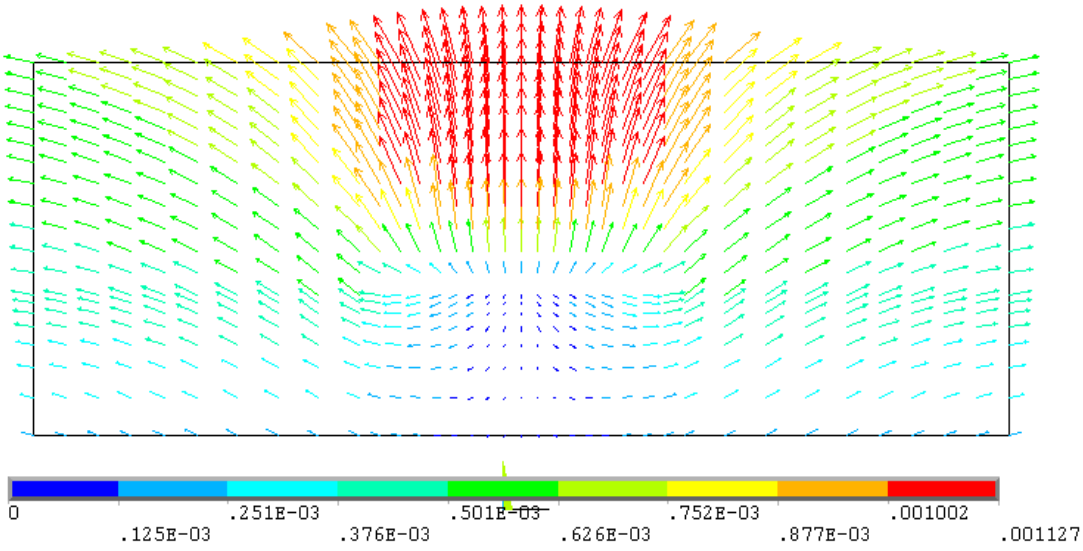
Based on the experimental and simulation results, it can be concluded that the temperature of active region in lateral PCRAM devices is higher than that of confined PCRAM devices during cycling. As segregation and diffusion are highly dependent on temperature, the segregation of phase change materials and the diffusion between phase change material and metal or dielectric materials are much faster in lateral PCRAM devices than that in confined PCRAM devices. This is one possible reason that lateral PCRAM devices fail faster than confined PCRAM devices with the same phase change material $Ge_2Sb_2Te_5$.

From both the experimental and simulation results, it can be also concluded that the lateral PCRAM device has a larger thermal and plastic deformation in the phase-change layer during cycling. Since plastic deformation occurs in the phase-change layer of the lateral PCRAM device, this means that atom bonds are broken within $Ge_2Sb_2Te_5$. This is consistent with lifetime testing results. Hence, it can be concluded that the failure of the lateral PCRAM device is mainly caused by plastic deformation. High temperature

and large plastic deformation in phase-change layer of the lateral PCRAM device accelerates the failure process.



(a)



(b)

Figure 2.17 Simulated elastic deformation fluxes in the (a) confined and (b) lateral PCRAM devices.

2.5 Summary

Experiments showed that the confined PCRAM device has a longer lifetime than the lateral PCRAM device with the same phase-change material and cell size. The failure mode of the lateral PCRAM device is stuck SET. Simulation results showed that temperature of active region in lateral PCRAM devices is higher than that of confined PCRAM devices during cycling. Both experimental and simulation results showed that the thermal and plastic deformation in the lateral PCRAM device is much larger than that in the confined PCRAM device during cycling. Hence, high temperature and large plastic deformation are two possible factors that accelerate the failure of the lateral PCRAM devices. To extend the lifetime of the lateral PCRAM device, it is better to minimize heat accumulation effect and plastic deformation in phase change layer during cycling. The heat accumulation effect issue can be solved by employing longer interval between two pulses during cycling as the heat can dissipate with enough cooling time. Hence, the major problem to extend cycle endurance for lateral PCRAM devices is plastic deformation, employing phase-change materials or structures that limit the thermal and plastic deformation would be a possible way to extend the lifetime of lateral PCRAM. This will be addressed in the next chapter.

Chapter 3 $GeTe/Sb_7Te_3$ Superlattice-Like Structure and its Applications in Lateral PCRAM

3.1 Introduction

Plastic deformation is identified as the possible reason for the failure of the lateral PCRAM device in Chapter 2. Bulk $Ge_2Sb_2Te_5$ is not an ideal phase-change material for the lateral PCRAM device as it does not limit plastic deformation. New phase change materials are needed for lateral PCRAM devices to achieve better endurance.

It was reported that superlattice structure can improve the Young's modulus [139-141] and resist the plastic deformation. Kim et al. studied the Synthesis of CrN/AlN superlattice coatings with various composition (Cr/Al at.%) and superlattice period (λ) using closed field unbalanced magnetron sputtering method [139]. Figure 3.1 shows the cross-sectional HR-TEM images of CrN/AlN superlattice film deposited at the 0.5 kW of Cr target power. The mechanical properties of CrN, AlN, and CrN/AlN superlattice films were measured and the results were listed in Table 3.1. From Table 3.1, it can be seen that the maximum hardness and plastic deformation resistance (H^3/E^2) of CrN/AlN superlattice film, when the atomic concentration ratio of Cr to Al is 0.98 and the superlattice period (λ) is 4.8 nm, are approximately 37 and 0.48 GPa, respectively. These values are 1.6 and 2.5 times higher than those of the CrN single layer coating (23.5 and 0.17 GPa), respectively. These enhancement effects in superlattice films could be attributed to the resistance to dislocation glide across interface between the CrN and AlN

layers. With the enhancement of mechanical properties, the plastic deformation of superlattice films can be reduced compared to bulk films.

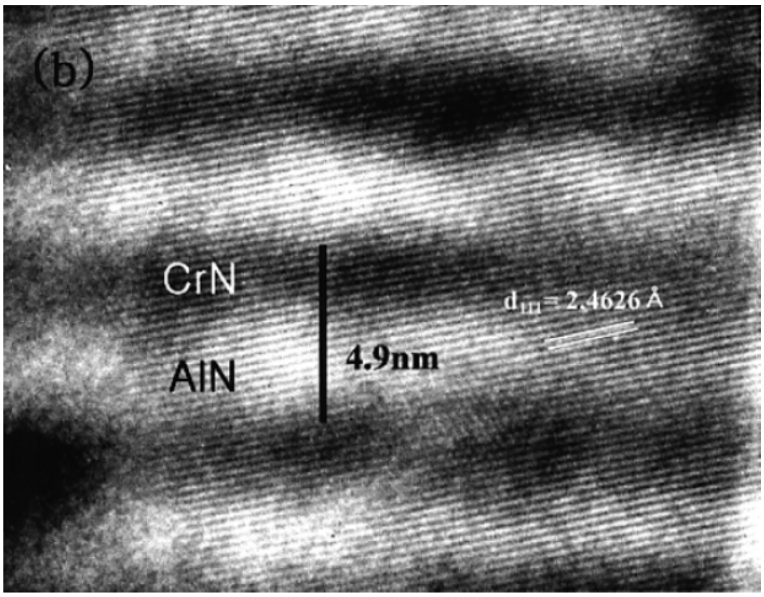


Figure 3.1 The cross-sectional HR-TEM images of CrN/AlN superlattice film deposited at the 0.5 kW of Cr target power [139].

Table 3.1 Mechanical constants of CrN film, AlN film and CrN/AlN superlattice films deposited at different values of Cr target power [139]

A	AlN	CrN	CrN/AlN (Cr=0.5 kW)	CrN/AlN (Cr=0.6 kW)	CrN/AlN (Cr=0.8 kW)	CrN/AlN (Cr=1 kW)
Cr/Al (at.%)	–	–	0.97	1.38	1.89	2.14
λ (nm)	–	–	4.9	6.3	9.7	12.5
H (GPa)	23.6	26.1	37.3	35.2	32.0	31.6
E (GPa)	258.18	319.33	328.26	341.46	342.78	350.56
H^3/E^2 (GPa)	0.197	0.174	0.481	0.374	0.278	0.256

λ, superlattice periods; H, hardness; E, elastic modulus and H^3/E^2, plastic deformation resistance.

Superlattice structure also shows other advantages. It has been found that the thermal conductivities can be reduced significantly in both in-plane and cross-plane directions in super-lattice structure experimentally and theoretically [142-144]. The electrical properties of super-lattice structure are dependent on the periods and thickness of the incorporated materials [145, 146].

Based on the superlattice structure properties in mechanical effects, it is expected that plastic deformation can be reduced by employing superlattice structure in lateral PCRAM devices. Hence, the endurance of lateral PCRAM devices can be extended if superlattice structure is employed. Phase change materials with such kind of superlattice structure are defined as superlattice-like (SLL) structure as phase change material may exist in amorphous state. This structure was first proposed by Chong *et al*. in 2002 in optical recording to increase both the crystallization speeds, and data transfer rates (DTR) [63]. In their experiments, GeTe and Sb_2Te_3 thin films were alternatively deposited to form the recording layer. The phase-change optical disk with SLL structure and red light demonstrated an excellent recording property with the DTR as high as 140 Mbit/s [63]. SLL structures can provide a new approach to improve the performance of PCRAM devices. By artificial structuring, rather than doping, it utilizes interface effect and nanoscale effects to improve material properties.

According to the established classical crystallization theory, crystallization is dependent on two distinct processes: the nucleation of small crystallites, followed by the subsequent growth. Phase change materials are classified into two types: nucleation-dominant (ND) and growth-dominant (GD) (as shown in Figure 3.2). ND and GD phase change materials are distinguished by the relative contributions of nucleation and

subsequent growth to the overall crystallization process. ND phase-change materials, such as $Ge_2Sb_2Te_5$, are used in vertical PCRAM devices [103, 147], while GD phase change materials, such as doped SbTe [103], doped GeSb [105] and doped Sb_2Te [129], are used in lateral PCRAM devices. Compared to the ND phase-change materials, GD phase-change materials have faster growth speeds, and lower threshold fields. Despite having above-mentioned properties, GD materials have their own weaknesses, such as data instability, and poor resistance ON/OFF ratio. There is an extensive search for an ideal GD phase-change material for lateral PCRAM devices. In addition to the immense effort in searching for new bulk phase change materials with better properties, researchers are also investigating the use of structure engineering to improve PCRAM device performance, e.g. by adopting an artificial SLL structure. In fact, ND SLL phase change structure consisting of alternating layers of GeTe and Sb_2Te_3 has been successfully applied in confined PCRAM and demonstrated both low power consumption and good stability [64]. ND GeTe/Sb_2Te_3 SLL structure, however, cannot be applied directly in a lateral PCRAM device due to the difficulties in achieving stable amorphization or crystallization [148].

In this chapter, we propose the concept of GD superlattice-like (SLL) phase change structure that incorporates one ND and one GD, or two GD binary phase-change materials, which shows fast and crystal growth dominant in crystallization process. GeSbTe system is the most popular phase change material. Hence, GeTe and Sb_7Te_3 were selected to form the GD SLL structure in this work. Detailed thin film studies of GeTe, Sb_7Te_3, and GeTe/Sb_7Te_3 SLL phase-change structure were conducted. A lateral

PCRAM device employing such GeTe/Sb_7Te_3 SLL phase-change structure was also fabricated and tested.

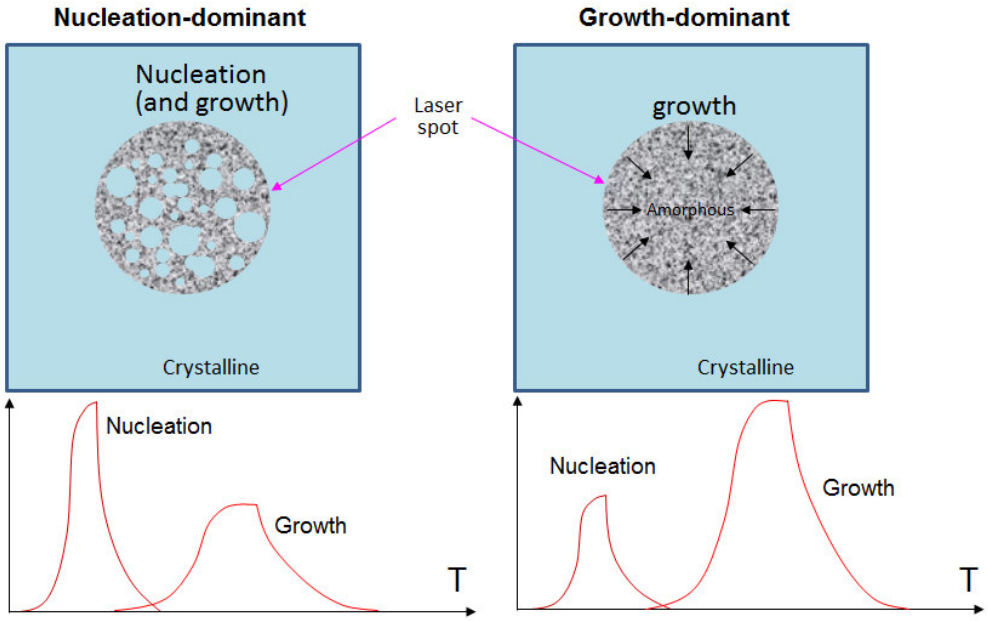


Figure 3.2 Schematic drawing of the two crystallization mechanisms: nucleation-dominant and growth-dominant.

3.2 Growth-dominant SLL structure

3.2.1 Growth-dominant SLL structure concept

As shown in Figure 3.3, the concept of SLL structure is to alternatively deposit two phase-change materials, each with different electrical, thermal, and crystallization properties. The SLL structure can be further defined as a growth-dominant SLL structure if one or both of the phase-change materials are selected from growth-dominant phase-change materials, and the SLL structure shows the growth-dominant property during crystallization process.

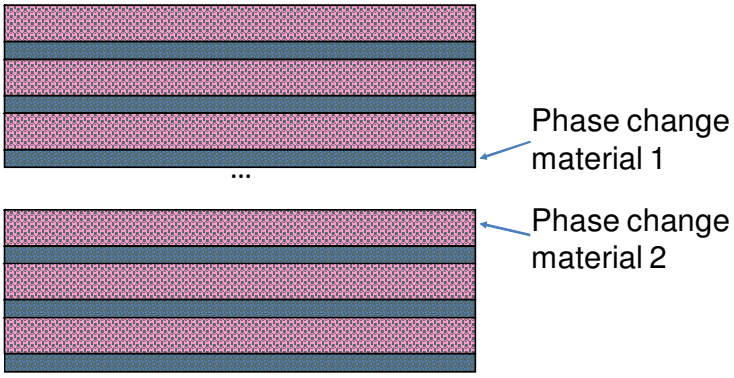


Figure 3.3 Schematic drawing of the SLL structure

GeSbTe-based phase change materials are widely used in PCRAM devices. Here, we select phase-change materials from this system to form growth-dominant SLL structures. Experimental measurements show that nucleation-dominant crystallization mechanism exists in GeTe and growth-dominant crystallization mechanism exists in Sb_7Te_3. GeTe has both high crystallization and melting temperature, which makes it very stable [149, 150]. However, it has a large bandgap, which results in a slow crystallization speed [151]. For eutectic Sb_7Te_3, it has both low crystallization and melting temperature, which results in a trade-off between high crystallization speed and poor thermal stability [152, 153]. GeTe and Sb_7Te_3 are not suitable for lateral PCRAM devices when used separately. In this work, we fabricate lateral PCRAM devices with SLL structure incorporated with GeTe and Sb_7Te_3. Figure 3.4 shows the process flow employed to fabricate the SLL structures incorporated with GeTe and Sb_7Te_3.

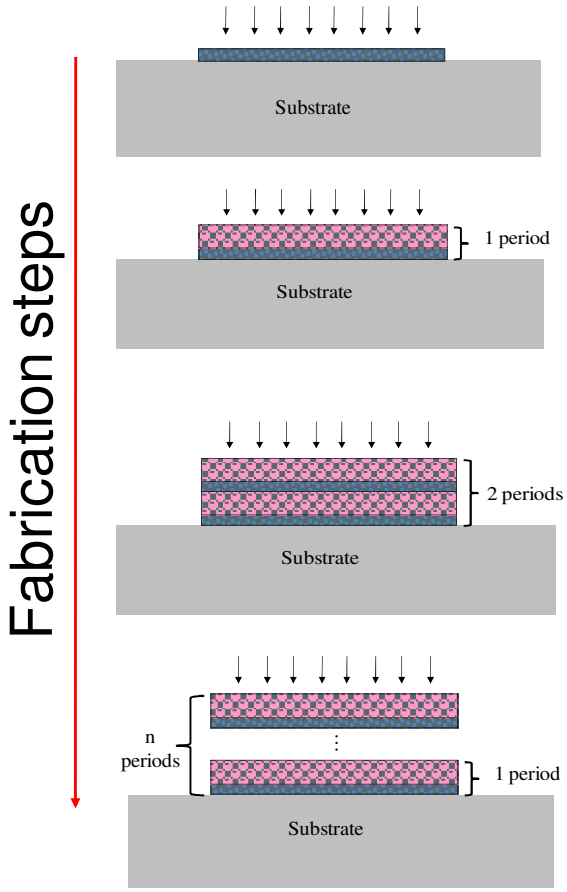


Figure 3.4 Process flow employed to fabricate the SLL structures.

3.2.2 Thin film study of bulk GeTe and Sb_7Te_3

In this work, GeTe and Sb_7Te_3 were selected to form the GD SLL structure. Studies on individual GeTe and Sb_7Te_3 thin films were conducted. The thin films were deposited on Si wafer with 1-µm-thick thermal oxide layer using the Balzers DC magnetron sputtering system with a base pressure of 10^{-6} mbar and a working pressure of 10^{-3} mbar. The thin films were deposited at room tempreature, and the deposition rates are listed in Table 3.2.

.

Table 3.2 Thin film deposition conditions for Balzers sputtering system

Chamber	Target	Sputtering Power (kW)	Ar flow rate (sccm)	Deposition Rate (nm/s)
1	GeTe	0.1	15	1.414
3	Sb_7Te_3	0.15	15	1.747
2	$ZnS\text{-}SiO_2$	1	15	2.105
3	Ti_3W_7	0.5	20	1.537

GeTe and Sb_7Te_3 films with different thicknesses covered by 100 nm $ZnS\text{-}SiO_2$ films were prepared. Two 100 nm TiW electrodes were embedded in the GeTe and Sb_7Te_3 films for the measurement of resistance by the multimeter. The resistivity was calculated via $R \times \frac{d \cdot W}{L}$, where R is the measured resistance by multimeter, L and W are film length and width, which are shown in Figure 3.5, while d is the film thickness of the GeTe and Sb_7Te_3 films.

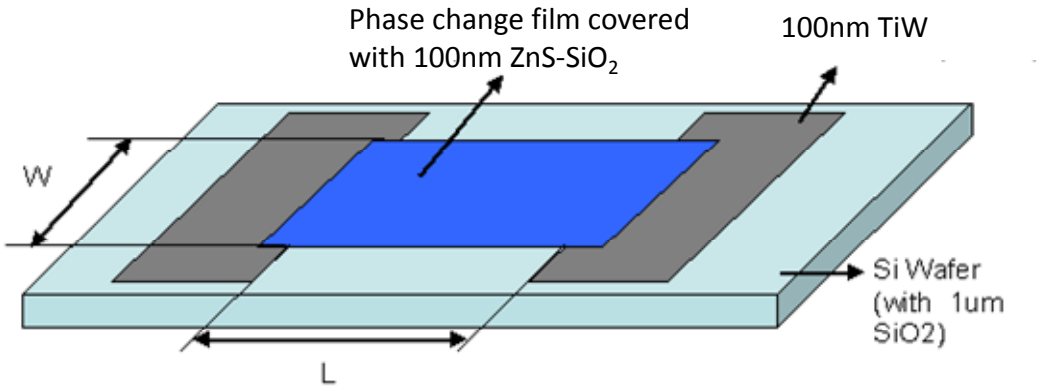


Figure 3.5 Schematics of a sample for ETTM measurements.

Crystallization behaviors of these samples were investigated with an exothermal resistance measurement (ETTM). The ETTM is used to measure the change in material properties (electrical, optical, and so on) when the temperature is increased or decreased. It is an important tool for studying the activation energy and thermally-induced material property changes. Figure 3.6 shows the setup for the ETTM measurements. The samples were uniformly heated using the Micromanipulator^{TM} H-1000 thermal Chuck System. The temperature was raised from the ambient temperature to 320 ˚C.

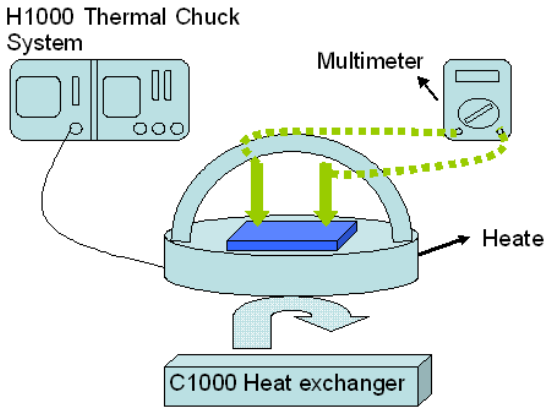


Figure 3.6 Set-up for the in-situ thermal-electrical resistance measurement system; the resistance of samples is monitored during thermal annealing.

As crystallization temperatures of phase-change materials are highly dependent on film thicknesses, detailed investigations on the crystallization behaviors of respective individual homogeneous GeTe and Sb_7Te_3 films with thickness ranging from 2.5 to 50 nm were performed using the ETTM at a constant heating rate of 5 ^{o}C/min. The values of electrical resistance versus temperature are shown in Figure 3.7 and Figure 3.8. As the

temperature increases, the resistance of the films decreases. The gradual decrease in resistance can be attributed to the temperature-dependent ionization in semiconductor materials [130]. At the crystallization temperature (T_x), a sharp drop in resistance is generally observed. The abrupt resistance decline is due to the rearrangement of atomic structures. As shown in Figure 3.7 and Figure 3.8, both GeTe and Sb_7Te_3 show a single-threshold behavior, indicating that both of them have only one crystallization state which makes them an ideal candidate for lateral PCRAM [103]. It can be seen that both materials display similar trends with higher T_x for smaller thicknesses. Such observation of higher T_x with decreasing film thickness was also reported for $Ge_2Sb_2Te_5$ [155]. At a film thickness of 2.5 nm, both GeTe and Sb_7Te_3 show negligible change in resistivity even at a high temperature of 320 ^oC. This indicates the absence of phase transition and implies that the critical thickness below which no phase-change can be induced is around 2.5 nm for the GeTe and Sb_7Te_3 film sandwiched by ZnS-SiO_2. The absence of phase-change is due to the fact that effective interface energy for films below 2.5 nm is too high to maintain a stable nucleus for crystallization to occur [156]. Such critical thickness for phase transition is in fact not uncommon, as it has been reported previously. For instance, Raoux reported that $Ge_2Sb_2Te_5$ thin films capped by Al_2O_3 have a thickness limitation of 3.6 nm [157, 158].

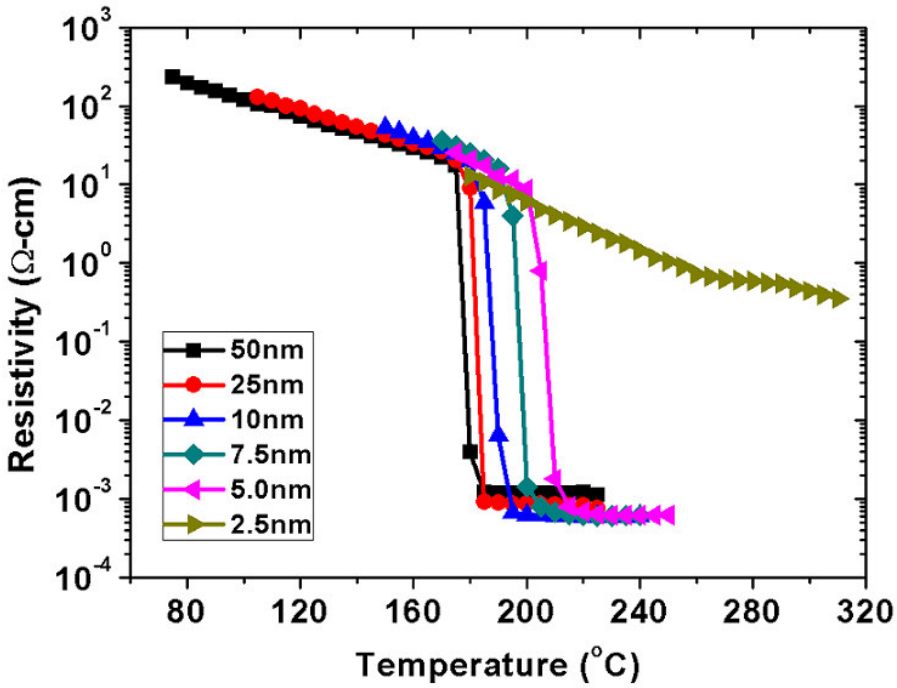


Figure 3.7 Temperature dependent resistivity of GeTe films at different thickness.

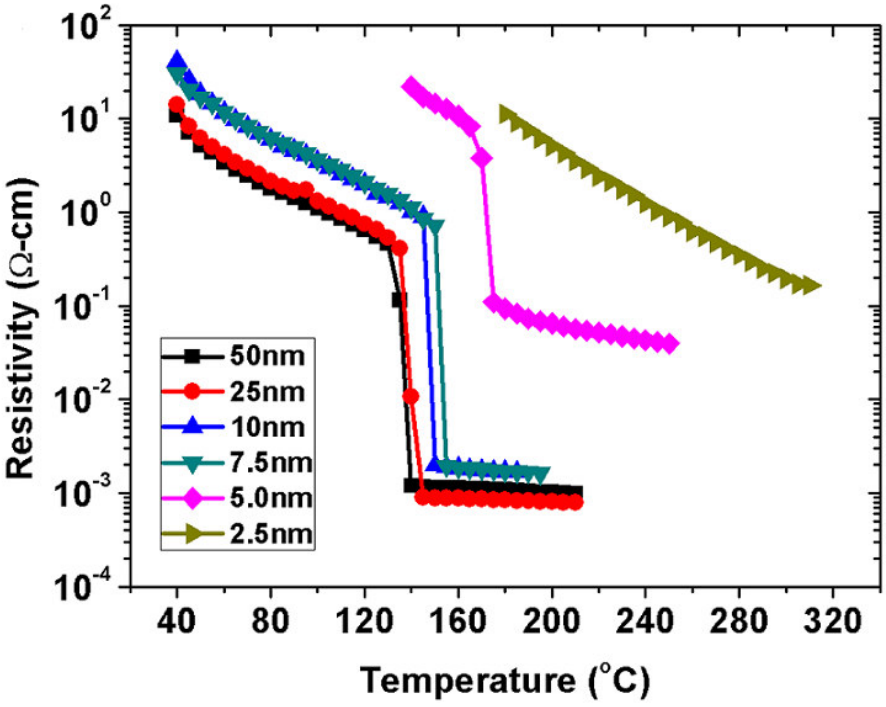


Figure 3.8 Temperature dependent resistivity of Sb_7Te_3 films at different thickness.

Upon close examination, it can be seen from Figure 3.7 that the resistivity of GeTe at both amorphous and the crystalline states remains fairly similar for different film thicknesses, as indicated by the almost overlapping curves at the two states. The resistivity of Sb_7Te_3, on the other hand, increases as the film thickness decreases for both amorphous and the crystalline states. Such increase in the resistivity with decreasing film thickness is especially prominent for the single homogeneous Sb_7Te_3 films in the crystalline state (Figure 3.8). This coupled with the fact that Sb_7Te_3 has a lower resistivity in the amorphous state as compared to GeTe, means that the resistivity differences of Sb_7Te_3 between the amorphous state and crystalline states at decreasing film thickness would be increasingly smaller than those of GeTe. As shown in Figure 3.9, the resistivity ratio of GeTe is around 10^4 at a thickness of 50 nm while that of Sb_7Te_3 at the same thickness is 10^3. For a thickness of 5 nm, the resistivity ratio remained at approximately 10^4 for GeTe, but decreased to 10^2 for Sb_7Te_3. The different resistivity ratios for GeTe and Sb_7Te_3 in this case are beneficial for SLL applications in lateral PCRAM as it can allow more freedom in designing the ON/OFF resistance ratio of the memory device. If a higher ON/OFF resistance ratio is needed, the SLL structure can be incorporated with a thinner GeTe and a thicker Sb_7Te_3. Conversely, if a lower ON/OFF resistance ratio is needed, the SLL structure can be incorporated with a thicker GeTe and a thinner Sb_7Te_3.

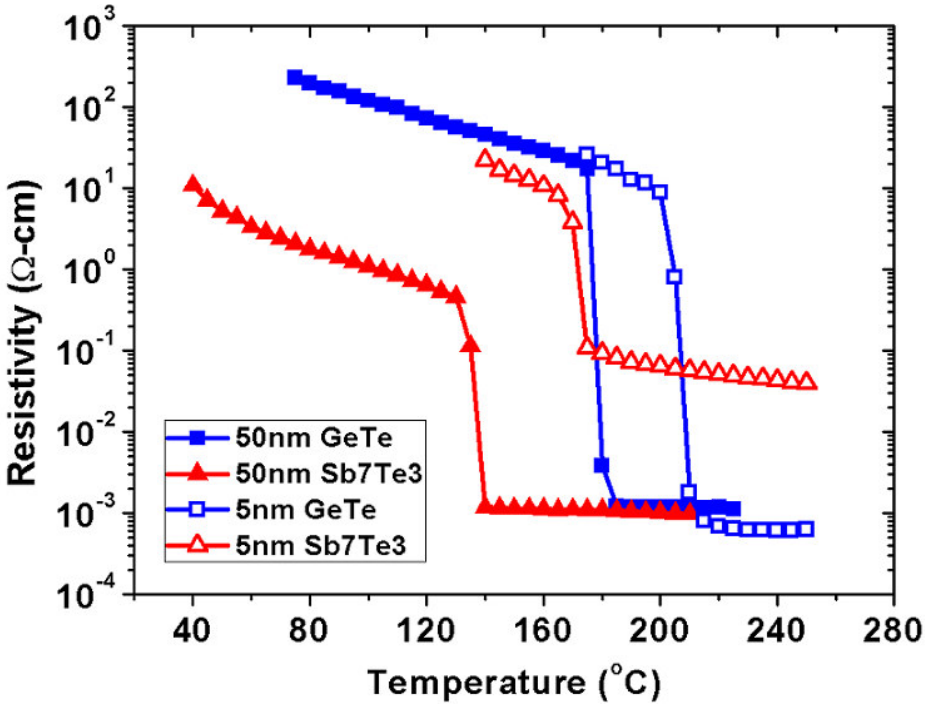


Figure 3.9 Comparison of the crystallization behaviors for GeTe and Sb_7Te_3 films with different thickness.

Figure 3.10 summarizes the dependence of the crystallization temperature T_x of both GeTe and Sb_7Te_3 on the film thickness. It can be seen that the T_x of both GeTe and Sb_7Te_3 increases with decreasing film thickness. In particular, while small increments in T_x are observed for the relative thick films (> 10 nm), the change in the T_x is much more prominent when the film thickness is reduced below 10 nm for both GeTe and Sb_7Te_3, as evident by the much steeper gradients presented by the two curves. Also, at each thickness, the T_x of GeTe is higher than that of Sb_7Te_3. The difference in T_x, however, gradually becomes smaller as the thickness decreases. For example, the gap between the two T_x is about 40 ^oC for a film thickness of 50 nm, and it decreases to approximately 35 ^oC for a film thickness of 5 nm.

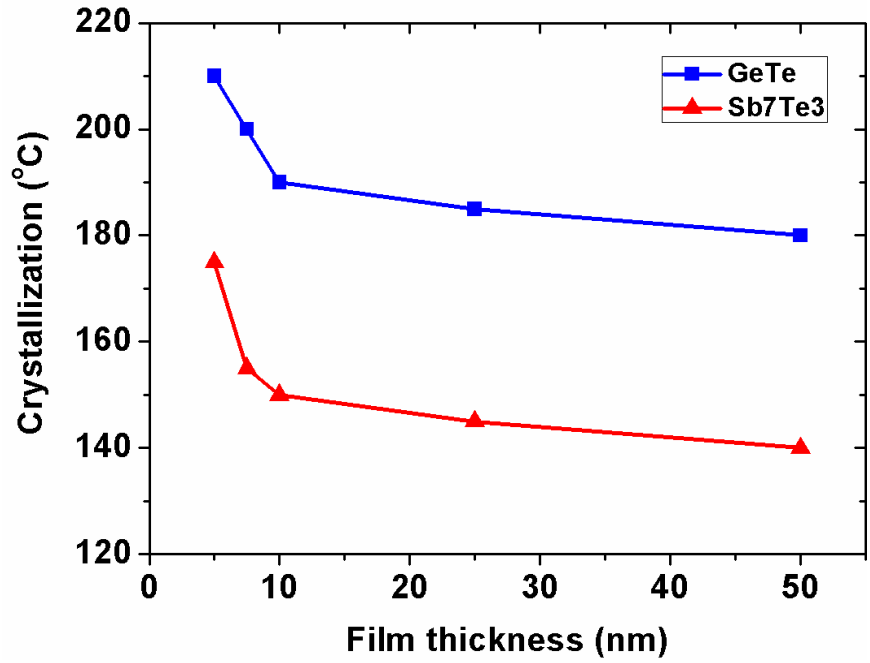


Figure 3.10 Crystallization temperature of GeTe and Sb_7Te_3 dependent on film thickness.

To check the trend of crystallization temperature when film thickness is below 10 nm, the logarithm value of Tx (Ln(Tx)) dependent on thickness is plotted in Figure 3.11. The Ln(Tx) value increases almost linearly with decreasing film thickness when the film thickness is less than 10nm for both GeTe and Sb_7Te_3. This indicates that crystallization temperature increases almost exponentially with decreasing film thickness for both GeTe and Sb_7Te_3. As SLL structures consist of GeTe and Sb_7Te_3 films with thickness less than 10 nm, this nanometer scale effect may be useful in the application of SLL structure.

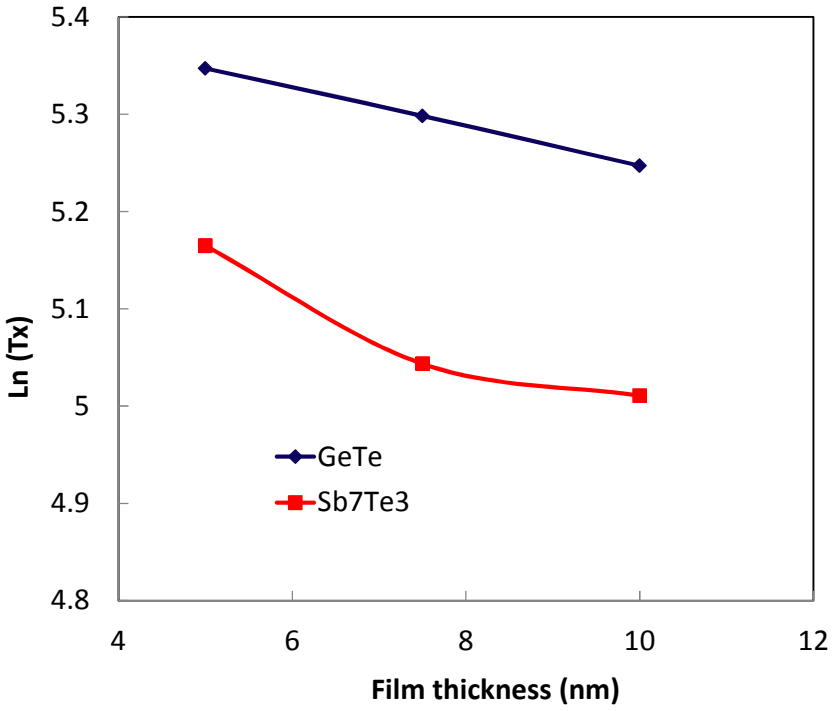


Figure 3.11 The logarithm value of Tx (Ln(Tx)) dependent on film thickness of GeTe and Sb_7Te_3 when film thickness is below 10 nm.

3.2.3 GeTe/Sb_7Te_3 SLL structure properties manipulation

GeTe/Sb_7Te_3 SLL structures were fabricated by depositing GeTe and Sb_7Te_3 films alternatively. The thickness of each layer was determined as the product of the sputtering rate and the sputtering duration, while the number of periods (one period consists of one GeTe layer and one Sb_7Te_3 layer) was controlled by the number of cycles of the alternation. In order to obtain a comprehensive study of SLL phase-change structures, the thickness ratio of GeTe and Sb_7Te_3 was varied from 1:1, 1.4:1, 1.6:1, 2:1, 3:1, and 4:1, respectively. The thickness (i.e. GeTe + Sb_7Te_3) of each period and the number of the periods were fixed at 12.5 nm and 4. The corresponding film thickness of GeTe and Sb_7Te_3 with different thickness ratio is listed in Table 3.3. The total thickness

of the entire SLL structure was kept at 50 nm. The SLL structure is covered with 100 nm thick ZnS-SiO_2. The GeTe/Sb_7Te_3 SLL structure fabricated in this work is shown in Figure 3.12, where the thicness ratio of GeTe and Sb_7Te_3 is 2. In this case, the GeTe/Sb_7Te_3 SLL structure consists of 4 periods, with each period having a ~8.3 nm thick GeTe layer and a ~4.2 nm thick Sb_7Te_3 layer. TEM image of the SLL structure shows that the interfaces of the sub-layers are very clear.

Table 3.3 List of the different thickness ratios in the SLL structures and their corresponding film thickness of GeTe and Sb_7Te_3.

Thickness ratio	**GeTe (nm)**	**Sb_7Te_3 (nm)**
1	6.25	6.25
1.4	7.3	5.2
1.6	7.7	4.8
2	8.33	4.17
3	9.375	3.125
4	10	2.5

Crystallization behaviors of these GeTe/ Sb_7Te_3 SLL structures were measured. ETTM was carried out at a heating rate of 5^{o}C/min. Figure 3.13 shows the dependence of the resistance of GeTe/Sb_7Te_3 SLL structures on the annealing temperature. From Figure 3.13, it can be seen that the crystallization temperature of SLL increases with the thickness ratio of GeTe to Sb_7Te_3, which means that the crystallization temperature can be controlled by SLL structure engineering. This can be explained in two aspects.

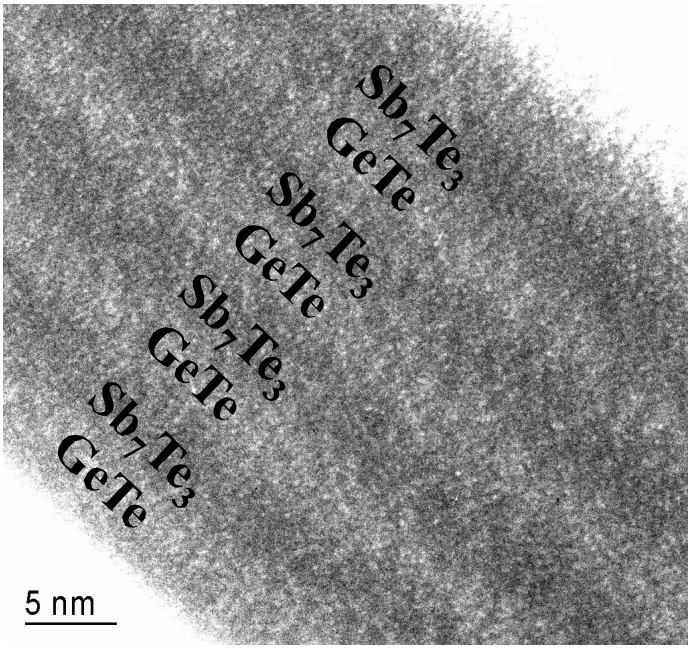


Figure 3.12 TEM image of a 50 nm thick GeTe/Sb_7Te_3 SLL structure phase-change medium at a thickness ratio of 2.

One is from composition of compound alloys as seen in Figure 3.14. GeTe has higher crystallization temperature and Sb_2Te_3 has lower crystallization temperature. Yamada et al has found that the compound consisting of GeTe and Sb_2Te_3 has higher crystallization temperature when more GeTe composition exists in the compound [154]. It is predicted that more GeTe in the compound can increase the bandgap and the crystallization temperature. Similarly in this work, the GeTe composition increases when GeTe/Sb_7Te_3 thickness ratio increases for GeTe/Sb_7Te_3 SLL structure. The crystallization temperature of GeTe/Sb_7Te_3 SLL structure increases when GeTe/Sb_7Te_3 thickness ratio increases.

The other aspect is that crystallization temperature is thickness dependent, where thinner films has higher crystallization temperatures. As the thickness ratio increases, the

thickness of the Sb_7Te_3 sub layer decreases while that of the GeTe sub layer increases. Thus, crystallization temperature of thin Sb_7Te_3 film increases. The overall effect is that crystallization temperature of SLL structure increases as thickness ratio increases. As a result, both the stability and data retention time of the SLL structures are improved. However, the crystallization time might be longer.

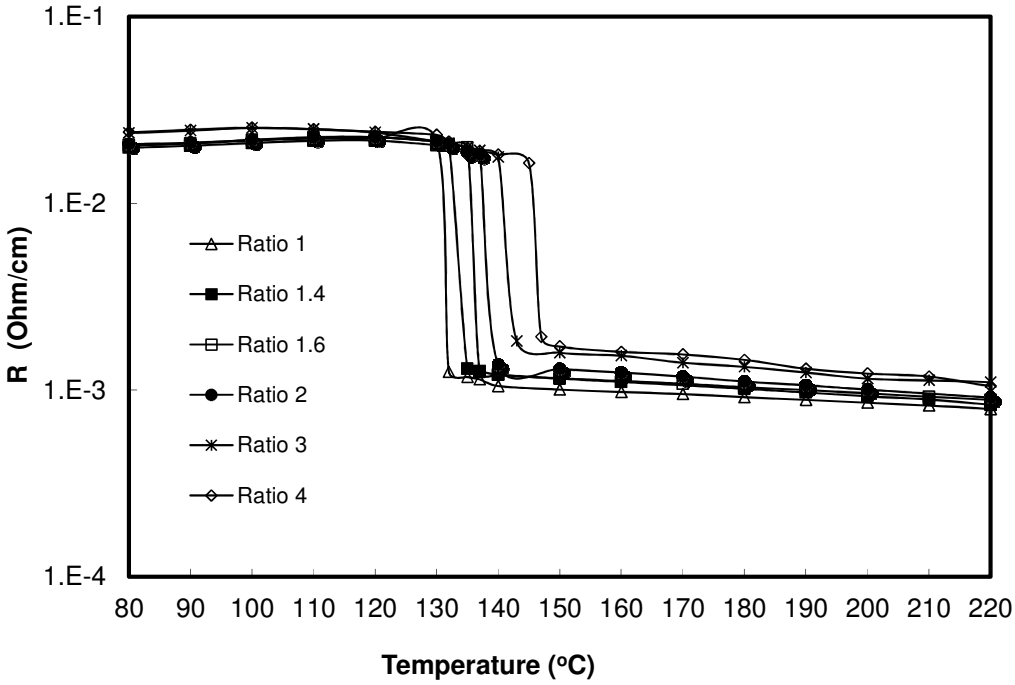


Figure 3.13 Crystallization behaviors of GeTe/ Sb_7Te_3 SLL structures measured via ETTM method.

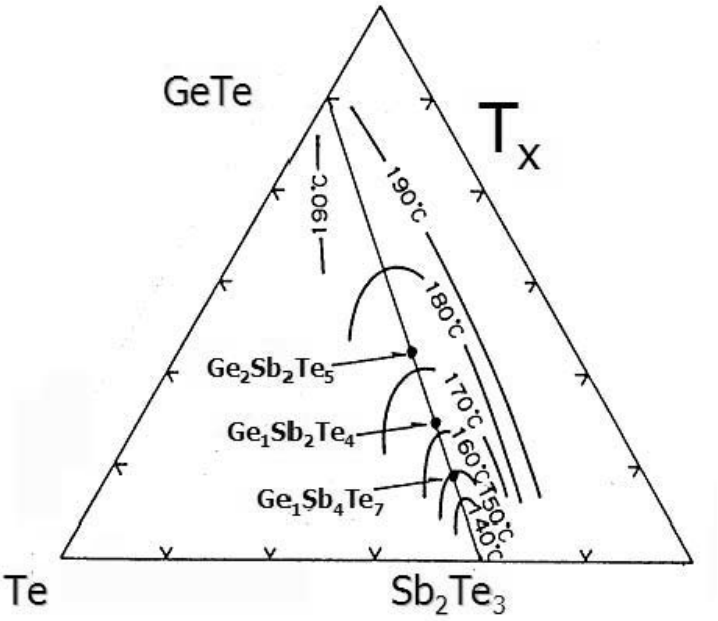


Figure 3.14 Compositional dependencies of the crystallization temperature T_x of Ge-Sb-Te thin films [154]

Melting (T_m) temperatures of SLL structures is another important parameter since it has strong influences on RESET current for lateral PCRAM devices. To measure the T_m of the GeTe/Sb_7Te_3 SLL structures, a phase-change temperature tester based on the reflectivity of the phase change films was employed. Figure 3.15 shows the setup for phase change temperature tester. The basic mechanism is to heat up the sample in a vacuum chamber. The vacuum level is 0.01 Torr. A laser beam is directed onto the surface of the sample, and a sensor detects the reflected laser. When the sample crystallizes (or melts), the optical contrast of the phase-change material changes abruptly, and this produces a corresponding increase (or decrease) in the measured reflected signal. Figure 3.16 shows the reflected laser signal at different temperatures for the SLL structure at a thickness ratio (GeTe to Sb_7Te_3) of 2.0 for a constant heating rate of 30^{o}C/min. The corresponding T_x and T_m in this case are 155 and 551^{o}C, respectively.

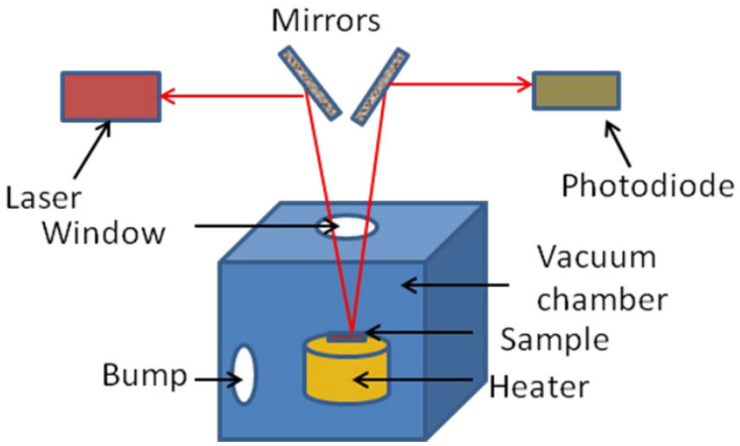


Figure 3.15 Schematic diagram of the setup for phase-change temperature tester.

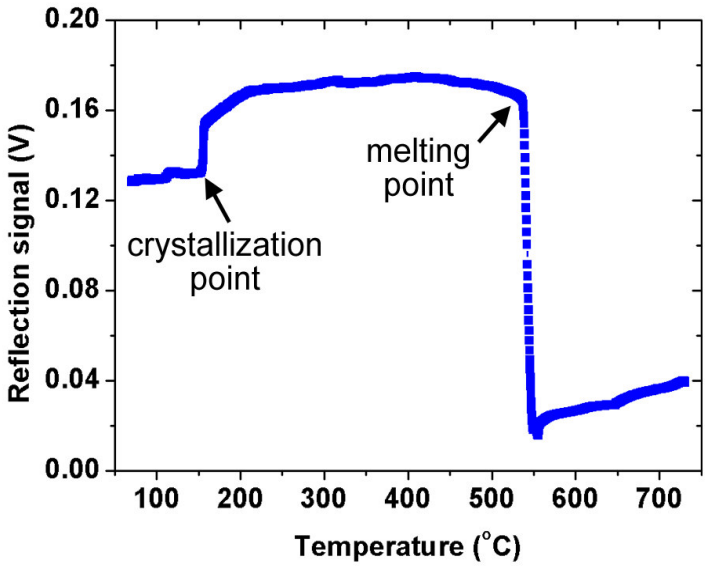


Figure 3.16 Working mechanism of the phase-change temperature tester.

Crystallization of GeTe/Sb_7Te_3 SLL structures with different thickness ratios were obtained and plotted in Figure 3.17. As depicted in Figure 3.17, the crystallization temperature first increases gradually from 153 to 159°C as the thickness ratio increases from 1.0 to 3.0 before the sudden increase to 185°C at the corresponding thickness ratio

of 4.0. The crystallization temperature of GeTe/Sb_7Te_3 SLL structures increases with the thickness ratio of GeTe/Sb_7Te_3.

The measured crystallization temperature with phase change temperature tester is different with the ETTM testing results. There are two different aspects. The first is the testing method is different. The results from Fig.3.13 are tested from setup of Fig. 3.7, which include a multi-meter. There is a small bias voltage applied when measuring the resistance of phase change material. When bias applied, the activation energy and crystallization temperature will drop [159]. The second difference is that the heating rate is different. The results from Fig.3.13 and Fig.3.17 are tested for 5°C/min and 30°C/min separately.

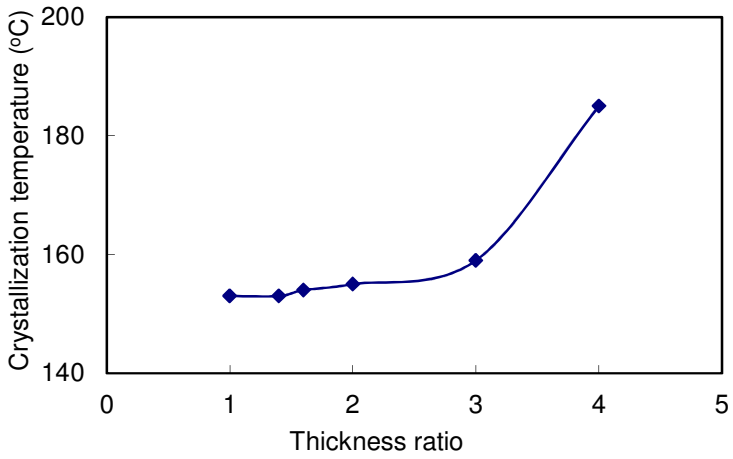


Figure 3.17 Crystallization temperature of GeTe/Sb_7Te_3 SLL structures at different thickness ratios measured by the phase change temperature tester. The heating rate is 30°C/min.

The melting temperature is of particular interest here since it determines the RESET current of PCRAM. The melting temperatures of 50nm thick GeTe/Sb_7Te_3 SLL

structures at different thickness ratios were measured by the phase change temperature tester. The melting temperatures of GeTe/Sb_7Te_3 SLL structures at different thickness ratios were obtained and plotted in Figure 3.18. With thickness ratio increasing from 1 to 1.6, the melting temperature of GeTe/Sb_7Te_3 SLL structures decreases. When thickness ratio is larger than 1.6, the melting temperature of GeTe/Sb_7Te_3 SLL structures increases with thickness ratio. Interestingly, melting temperature exhibits a local minimum of 535^{o}C for the thickness ratio of 1.6. There are two possible reasons. The first possible reason exists in the combination of thickness dependent melting temperature and transition area in the interfaces of GeTe/Sb_7Te_3 SLL structures. As the melting temperature of GeTe is much higher than Sb_7Te_3, the melting temperature of GeTe/Sb_7Te_3 SLL structures will be mainly determined by Sb_7Te_3 sub layer in the GeTe/Sb_7Te_3 SLL structures. With thickness ratio increasing, the sub layer thickness of Sb_7Te_3 decreases. As the melting temperature of phase change material is thickness dependent and thinner film has lower melting temperature [27], the melting temperature of thinner Sb_7Te_3 film will be lower. That is the reason that the melting temperature of GeTe/Sb_7Te_3 SLL structures decreases with thickness ratio increasing from 1 to 1.6. If the thickness of Sb_7Te_3 film decreases further, the interface effect will be obvious. Figure 3.19(a) shows the schematic diagram of an ideal SLL structure. With the implantation and diffusion effect, the interface GeTe/Sb_7Te_3 SLL structures will be not ideal and a transition area consisting of Ge, Sb and Te atoms will be formed (see Figure 3.19(b)). When the Sb_7Te_3 film thickness is less or equal to the transition area, the melting temperature of GeTe/Sb_7Te_3 SLL structures will be determined by the GeSbTe transition area. As GeSbTe has higher melting temperature than Sb_7Te_3, it is reasonable that the melting

temperature of GeTe/Sb_7Te_3 SLL structures will be higher. This could be the reason that melting temperature of GeTe/Sb_7Te_3 SLL structures increases with thickness ratio increasing from 1.6 to 4.

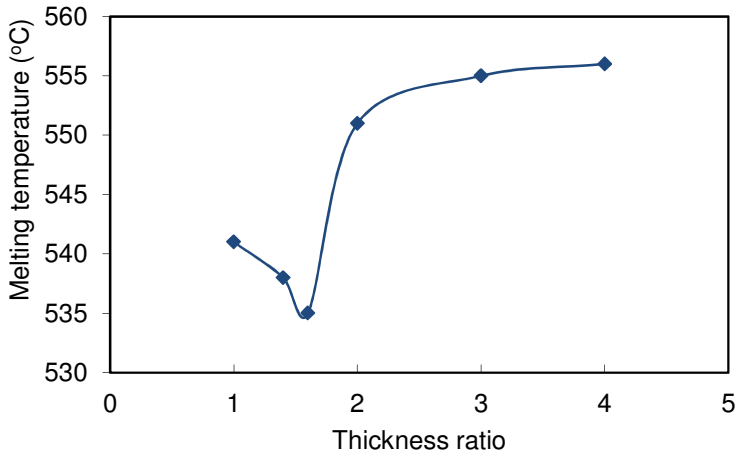


Figure 3.18 Melting temperature of GeTe/Sb_7Te_3 SLL structures at different thickness ratios measured by the phase change temperature tester. The heating rate is 30°C/min.

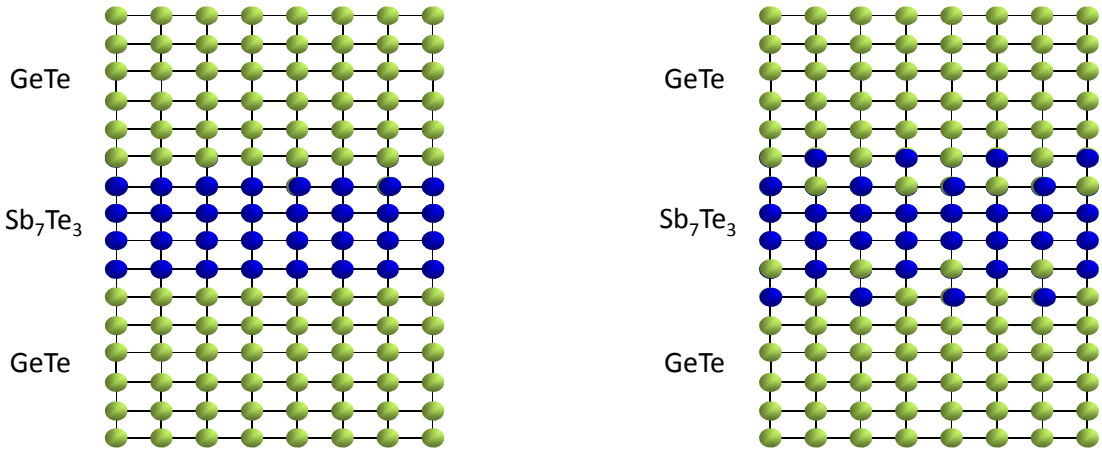


Figure 3.19 Schematic of GeTe/Sb_7Te_3 SLL structures in (a) ideal structure and (b) reasonable structure.

The second possible reason is attributed to the phase diagram of GeTe-Sb_7Te_3. Figure 3.20 shows GeTe-Sb_2Te_3 pseudobinary phase diagram done by Abrikosov [160] and Yamada [161]. Compound consisting of GeTe and Sb_2Te_3 has different melting temperature when more GeTe composition exists in the compound. With GeTe composition increasing, the melting temperature of compound decreases at first and then increase. Our result is similar with this trend.

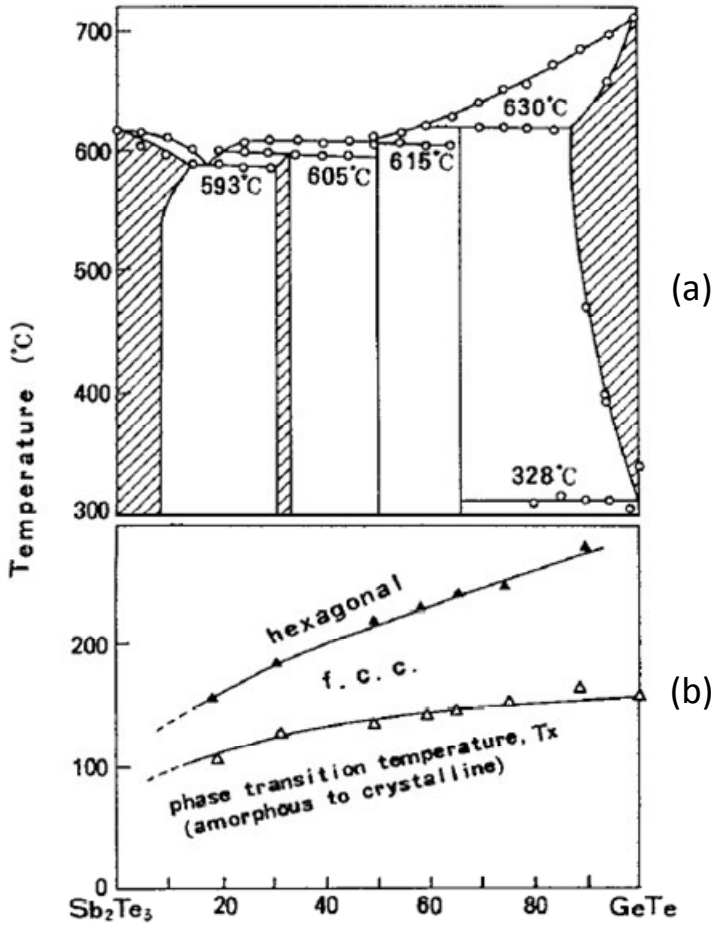


Figure 3.20 (a) GeTe-Sb_2Te_3 pseudobinary phase diagram from Abrikosov [160] and (b) phase transition temperatures of GeTe-Sb_2Te_3 pseudobinary amorphous alloy films [161].

3.3 GeTe/Sb_7Te_3 SLL structure applications in lateral PCRAM

3.3.1 Lateral PCRAM with GeTe/Sb_7Te_3 SLL structure

Schematics of the lateral PCRAM device with SLL structure, and the ternary alloy phase diagram are shown in Figure 3.21. The two component phase-change materials are GeTe and Sb_7Te_3. Canon stepper lithography of 1 μm technology was used to pattern the lateral PCRAM cells and Balzers Magnetron Sputtering System was used to deposit the thin films. Two 100 nm thick TiW electrodes were deposited on each side of the SLL structure. The electrodes were separated by 0.5 μm. The SLL structure is 3 μm long and 1 μm wide, and is capped with a 200 nm thick ZnS-SiO_2 (As seen in Figure 3.21). In this work, a pair of GeTe/Sb_7Te_3 was defined as a period, and 4 periods were grown for each lateral PCRAM device. Total thickness of the SLL structure is 50 nm. Each period was designed to be 12.5 nm. The fabricated lateral PCRAM cells were characterized by a self-developed tester system as mentioned in section 2.2.4.

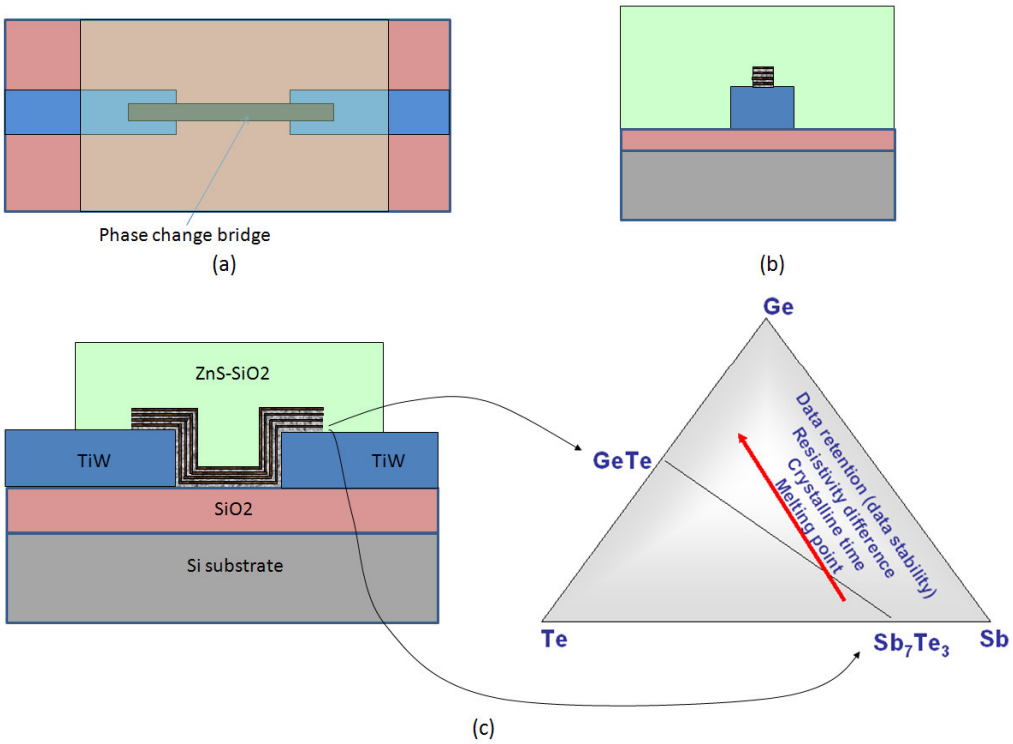


Figure 3.21 (a) Top, (b) side, and (c) cross-sectional view of a lateral PCRAM device with SLL structure, and ternary alloy phase diagram

3.3.2 Testing of lateral PCRAM devices with GD SLL structure

Program window of PCRAM devices is important for determining the Read, SET (from the amorphous to crystalline state) and RESET (from the crystalline to amorphous state) zones. The program window of lateral PCRAM devices with SLL structure at different thickness ratios was measured. The RESET amplitude was fixed at 2.4 mA while the SET current was increased from 0 mA at an intervals of 0.1 mA. For both RESET and SET, the pulse width was fixed at 30 ns. Figure 3.22 shows the programming window of the lateral PCRAM devices with SLL structure of different thickness ratios. From Figure 3.22, it can be observed that varying the thickness ratio can control the

program window of lateral PCRAM with SLL structure. The lateral PCRAM devices with SLL structure incorporated different thickness ratios can be SET to the crystalline state, and RESET to the amorphous state with 30 ns pulses.

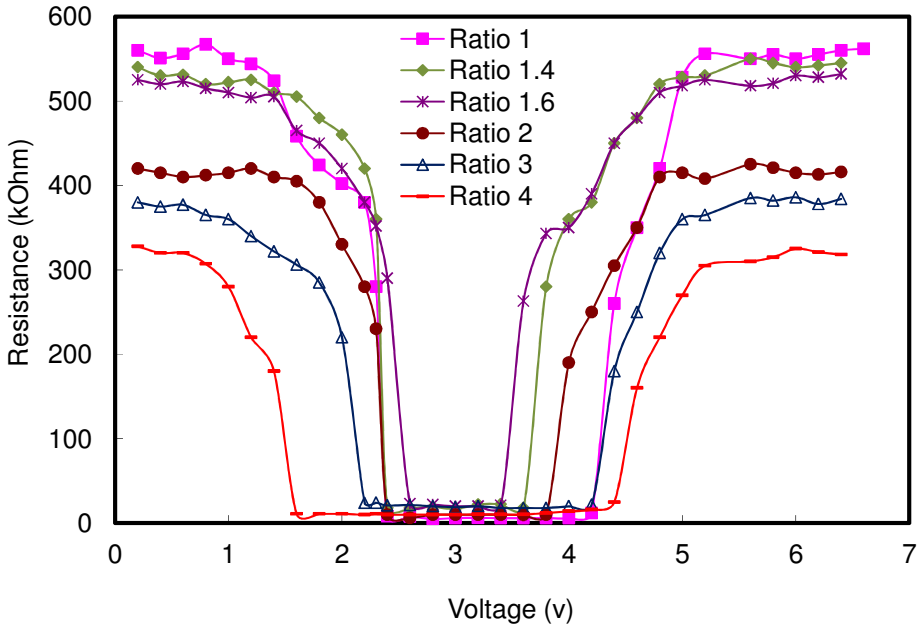


Figure 3.22 Programming window of the SLL lateral PCRAM devices with different thickness ratios as a function of current. For both RESET and SET, the pulse width was fixed at 30 ns

The SET and RESET currents were summarized in Figure 3.23. The SET current decreases as the thickness ratio increases. In contrast, the RESET current first decreases as the thickness ratio increases from 1 to 1.6, and then increases as the thickness ratio increases from 1.6 to 4. It can be seen that the RESET current reaches a minimum of 1.5 mA. The programming window is the narrowest at the thickness ratio of 1.6. As the RESET current is the most critical parameter for PCRAM devices, the above results

showed that SLL structures at a thickness ratio of 1.6 is the optimized structure for lateral PCRAM devices referred to RESET current.

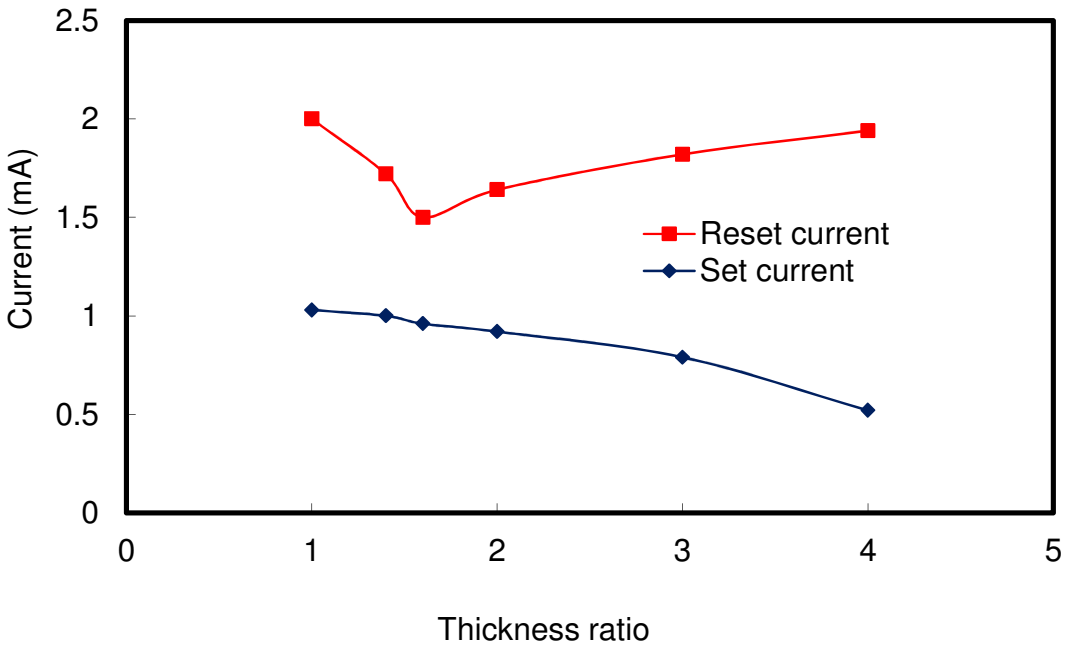


Figure 3.23 Dependence of the lowest SET and RESET currents of the SLL lateral PCRAM devices on thickness ratio. For both RESET and SET, the pulse width was fixed at 30 ns.

Figure 3.24 shows the typical U-shaped SET and S-shaped RESET curves for the lateral PCRAM devices with GeTe/Sb_7Te_3 SLL structure at the thickness ratio of 1.6 obtained using 30 ns square pulses. The pulse width (i.e. the SET speed) in this case is 30 nanoseconds, which is faster than the previous reported values [103] even though our cell size is 20 times larger. The fast switching speed may be attributed to the fact that Sb_7Te_3 has very fast crystallization speeds, which provides crystal growth seed for GeTe and avoid the long nucleation time for GeTe. The SET and RESET current are 1.0 mA and 1.5 mA, respectively.

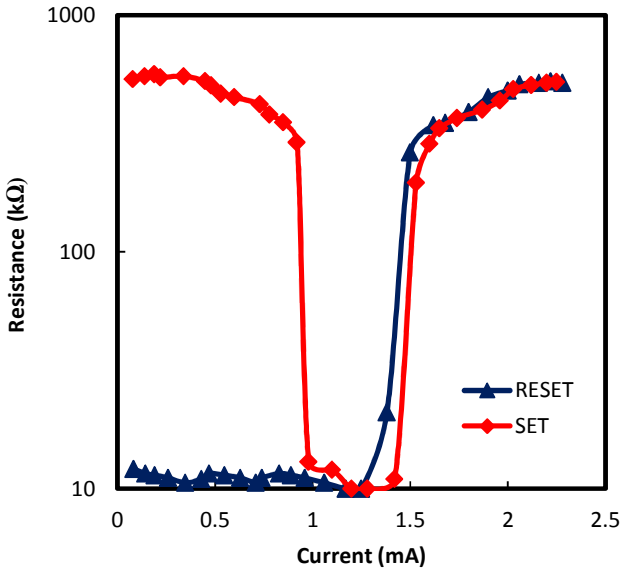


Figure 3.24 U-shaped SET and S-shaped RESET curves for lateral PCRAM devices with GeTe/Sb_7Te_3 SLL structure at the thickness ratio of 1.6. For both RESET and SET, the pulse width was fixed at 30 ns.

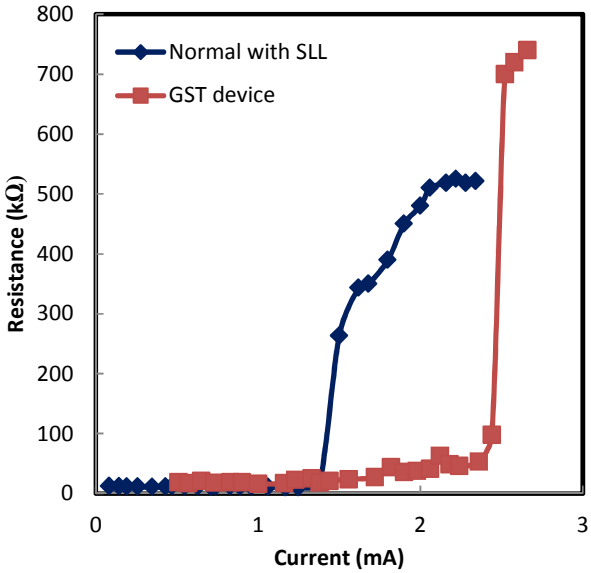


Figure 3.25 S-shaped RESET curves for lateral PCRAM devices with GeTe/Sb_7Te_3 SLL structure at the thickness ratio of 1.6 and $Ge_2Sb_2Te_5$

The results were compared with lateral PCRAM devices with $Ge_2Sb_2Te_5$ and other reports. For lateral PCRAM devices with $Ge_2Sb_2Te_5$, the RESET current is around 2.5 mA (as seen in Figure 3.25). Compared to lateral PCRAM devices with $Ge_2Sb_2Te_5$, the RESET current is about 40% lower. It was found that the RESET current of the lateral PCRAM device with SLL structure at thickness ratio of 1.6 is at the same level compared to that of reported results (Philips and IBM devices), but with a cell size that is about 20 times larger (refer to Table 3.4). There are two possible reasons for the low RESET current. The first reason is that the phase-change medium with SLL structure demonstrates a lower thermal conductivity, and provides better thermal isolation for the cell such that less power is needed to reach the melting temperature. Another possible reason is related to thickness dependent melting temperature of Sb_7Te_3 and GeTe film. RESET current is the lowest because the melting temperature of the SLL structure is the lowest at a thickness ratio of 1.6.

Table 3.4 RESET current comparison between lateral PCRAM devices with SLL structure and other devices

	Contact area (μm^2)	Cross-Section (nm^2)	line length (nm)	RESET pulse Width (ns)	RESET current (mA)
Philips (2005) [103]	≥ 8	2500	500	30	≥ 1
IBM (2007) [105]	≥ 0.1	2500	50	\	≥ 1
Lateral PCRAM with $Ge_2Sb_2Te_5$	1.1	50000	500	60	2.5
Lateral PCRAM with SLL structure	1.1	50000	500	30	1.5

3.3.3 Endurance of lateral PCRAM with GD SLL structure

Cycle endurance of lateral PCRAM devices with SLL structure incorporating different thickness ratios was investigated. Figure 3.26 shows the cycle endurance of lateral PCRAM device as a function of thickness ratio using SET conditions of 120 ns/0.38 mA and RESET conditions of 30 ns/2.2 mA (SET and RESET optimized condition for most devices). From Figure 3.26, it can be observed that the highest cycle endurance (about 20k cycles) is achieved in SLL lateral PCRAM cell at a thickness ratio of 1.6. It indicates that lateral PCRAM with SLL structure incorporating a thickness ratio of 1.6 has the best lifetime. The results suggest that SLL structure incorporated with GeTe and Sb_7Te_3 should have a thickness ratio of 1.6 to achieve both the low RESET current, and long cycle endurance.

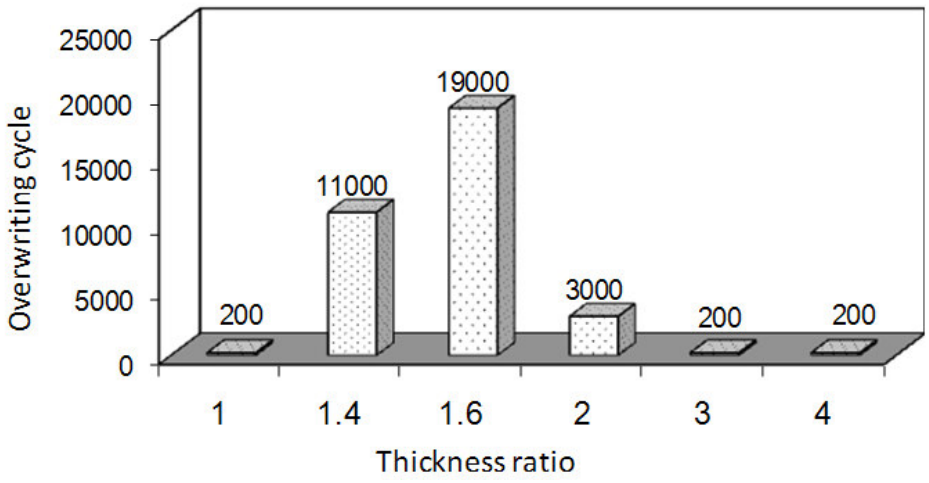


Figure 3.26 Cycle endurance of lateral PCRAM device as a function of thickness ratio using SET conditions of 120 ns/0.38 mA and RESET conditions of 30 ns/2.2 mA.

Cycle endurance testing was further conducted to find the longest lifetime achievable using the optimized SET and RESET conditions for the lateral PCRAM devices with SLL structure of thickness ratio 1.6. It was found that cycle endurance of 5.3×10^6 cycles can be achieved with SET current amplitude of 1.16 mA and RESET current amplitude of 2.2 mA (Figure 3.27). The pulse width for both SET and SET is 30 ns. The resistance ratio between the RESET and SET states is still more than 20 at 5.3×10^6 cycles.

Hence, it can be concluded that the endurance of lateral PCRAM can be improved by applying SLL structure. The possible reason is that the mechanical properties of SLL structure are improved compared to bulk materials and the deformation is smaller. Hence, the endurance of lateral PCRAM is improved.

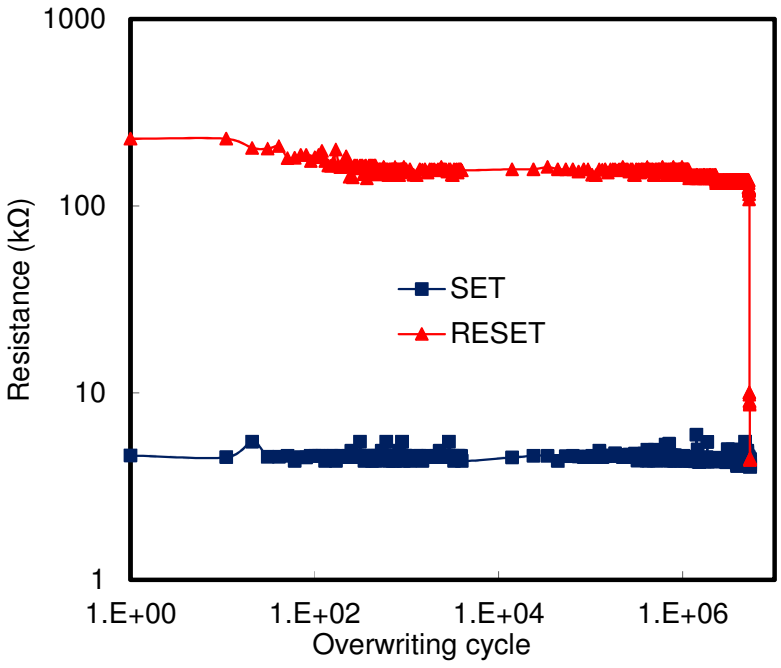


Figure 3.27 Cycle endurance of lateral PCRAM device at a thickness ratio of 1.6 using SET conditions of 30 ns/1.16 mA and RESET conditions of 30 ns/2.2 mA.

3.3.4 Transient effect of lateral PCRAM with SLL structure

Transient current waveform during a crystallization process in a vertical phase-change memory device can be measured and analyzed [162]. In that work, two time parameters, the delay and current recovery times, were measured from the transient waveform which provides the link between crystallization kinetics and the transient phase change effect. This transient measure with two time parameters has been used to identify the crystallization differences between nucleation and growth dominated materials. This allows for quantitative assessment of material and device engineering effects on crystallization in phase change memory. In this work, the transient effect of lateral PCRAM devices with GD SLL structure at a thickness ratio of 1.6 was measured and analyzed.

Table 3.5 lists the details of the SET conditions, RESET and SET resistances, delay and recovery times for lateral PCRAM devices with SLL structure of thickness ratio 1.6. The lateral PCRAM device was RESET to around 500 kΩ with RESET pulse width of 20 ns, and pulse-amplitude of 2.3 mA. The SET pulse amplitude varies from 1.2 to 1.7V. The SET pulse width was kept constant at 400 ns. All the pulses can SET the device to crystalline state, and the SET resistance is around 10 kΩ. Current waveforms acting on the devices were captured after different SET pulses were applied.

Table 3.5 List of SET conditions, RESET and SET resistance, delay and recovery time

Pulse width (ns)	Applied Voltage (V)	SET Current (mA)	RESET Resistance (kΩ)	SET Resistance (kΩ)	Delay time (ns)	Recovery time (ns)
400	1.2	0.17	507	12	175	225
400	1.3	0.2	550	11	150	250
400	1.4	0.23	520	9	130	270
400	1.5	0.26	510	7	80	320
400	1.6	0.32	523	6	70	330
400	1.7	0.36	530	6	60	340

Figure 3.28 shows the different current waveforms with different applied pulse amplitudes. From Figure 3.28, the transient effect can be observed clearly and it was found that delay time would increase with a lower voltage being applied. The delay time and current recovery times under different SET voltages were summarized in Figure 3.29. It can be observed that the current recovery time is always longer than the delay time under different SET pulse voltages, which confirms that SLL structure incorporated with GeTe and Sb_7Te_3 are fully GD phase-change medium. With increasing the SET voltage, the delay time will be even shorter, while crystal growth time will be longer.

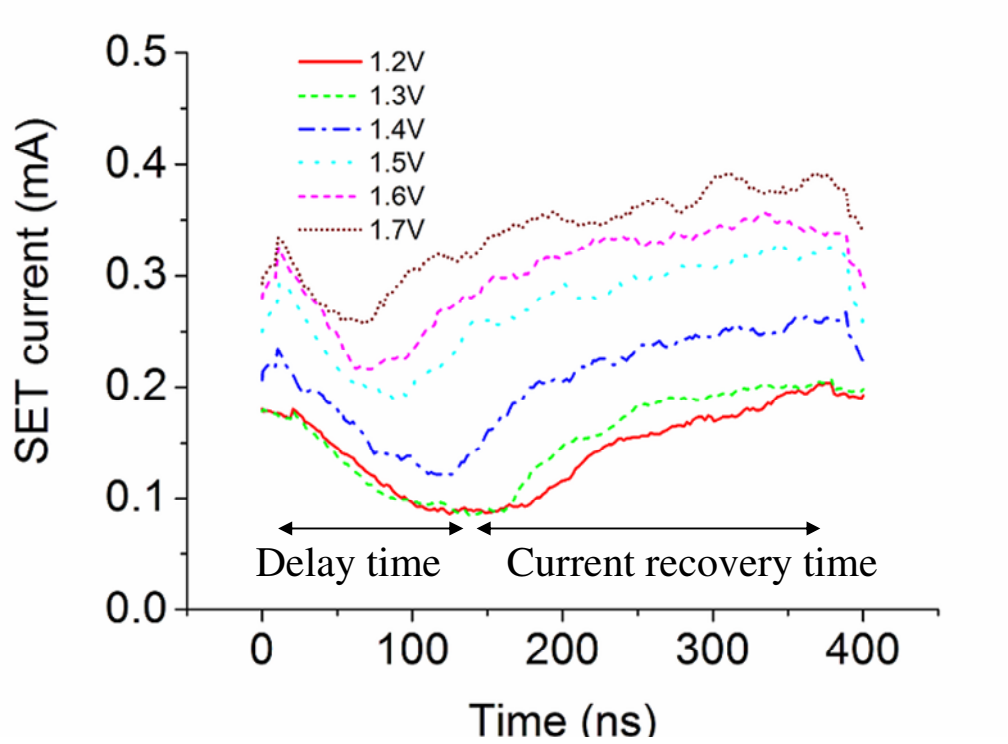


Figure 3.28 Transient effects of lateral PCRAM devices.

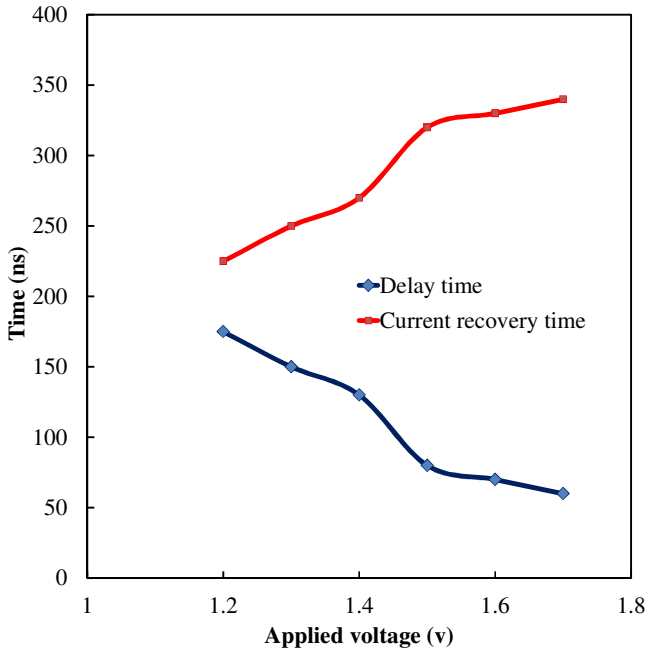


Figure 3.29 Delay time and current recovery time of the SLL lateral PCRAM device at a thickness ratio of 1.6 under different SET voltages.

3.4 Thermal simulation for lateral PCRAM with SLL structure

Thermal simulation was also done to investigate the effect of SLL structure application in lateral PCRAM devices. As the material properties of SLL structures is difficult to be measured, thermal simulation of lateral PCRAM devices was performed based on material properties of the $Ge_2Sb_2Te_5$. The simulation model and material parameters employed were the same as those presented in section 2.4.1. As the thermal conductivity of SLL structure can be reduced about 70% compared to bulk materials [64, 143], we simulated the thermal distribution of lateral PCRAM devices with phase-change materials varying the thermal conductivity. Thermal conductivity of the phase-change material was varied from 100% to 25% in only x or y direction, and in both the x and y directions. Figure 3.30 to Figure 3.33 show the temperature distributions in lateral PCRAM devices as the thermal conductivity of phase-change material is varied from 100% to 25% in both the x and y directions. From these figures, it can be observed that the higher peak temperature can be achieved in the lateral PCRAM device by reducing the thermal conductivity of the phase-change materials. As the thermal conductivity was reduced by 0, 25, 50, and 75% in both x and y directions, the peak temperatures achieved in the lateral PCRAM device were 636, 705, 819 and 1070^{o}C, respectively. This means that a lower power is needed to reach the melting temperatures of phase-change material with lower thermal conductivities, enabling the lateral PCRAM device with SLL structure to achieve a lower RESET current.

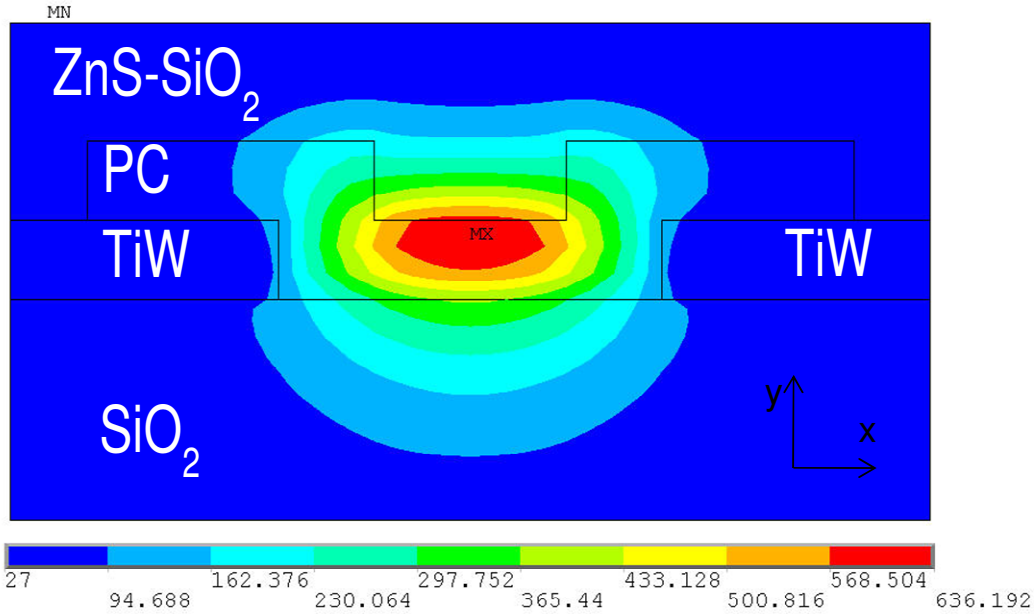


Figure 3.30 Temperature distribution of lateral PCRAM when a phase-change material has a thermal conductivity Tx=Ty=100%.

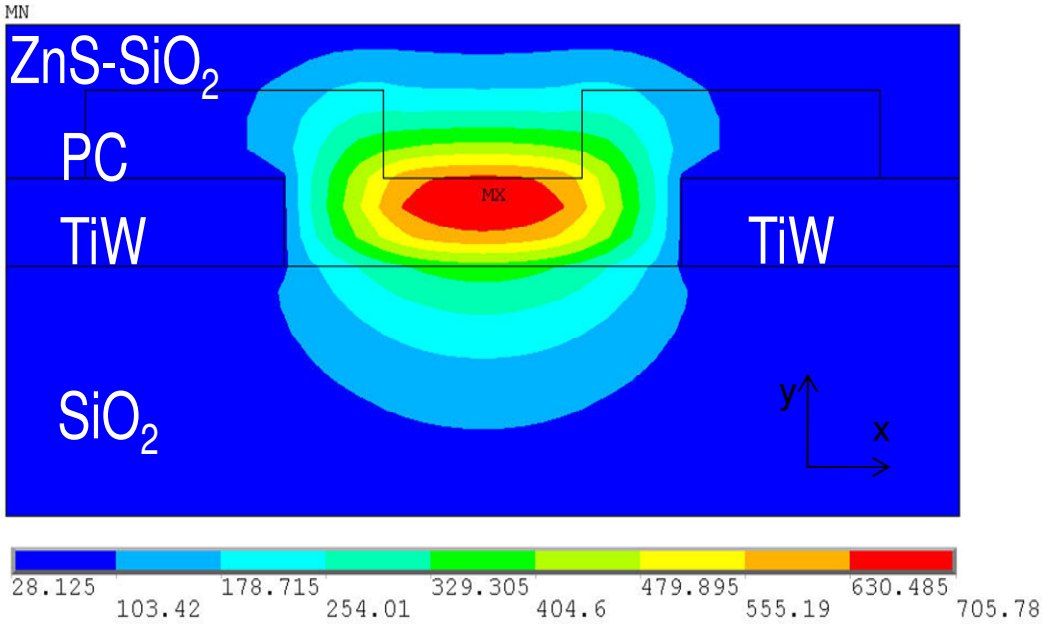


Figure 3.31 Temperature distribution of lateral PCRAM when a phase-change material has a thermal conductivity Tx=Ty=75%.

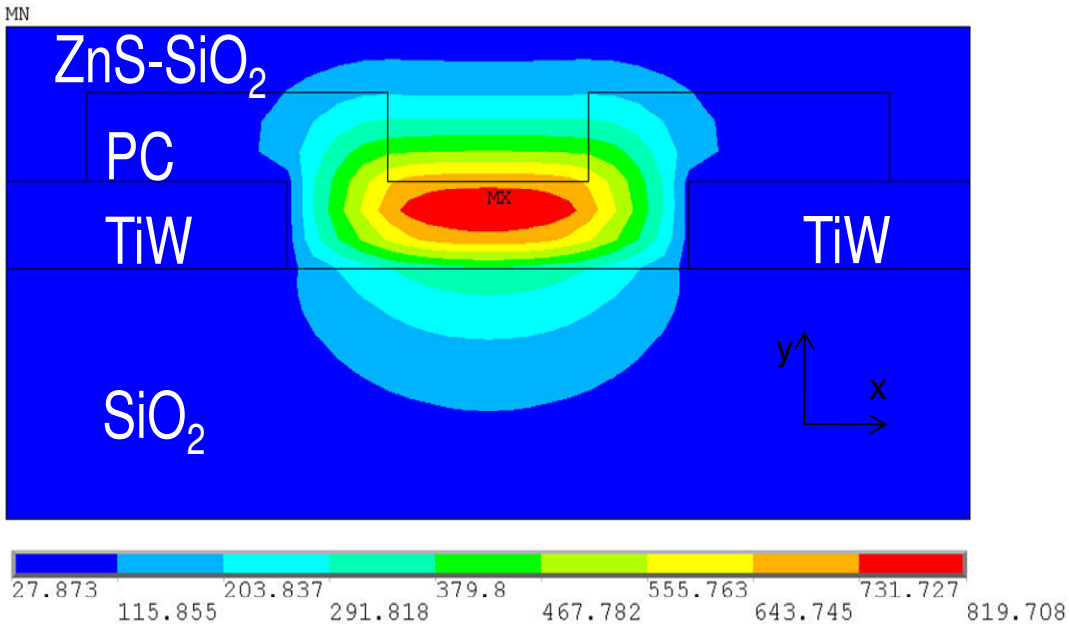


Figure 3.32 Temperature distribution of lateral PCRAM when a phase-change material has a thermal conductivity Tx=Ty=50%.

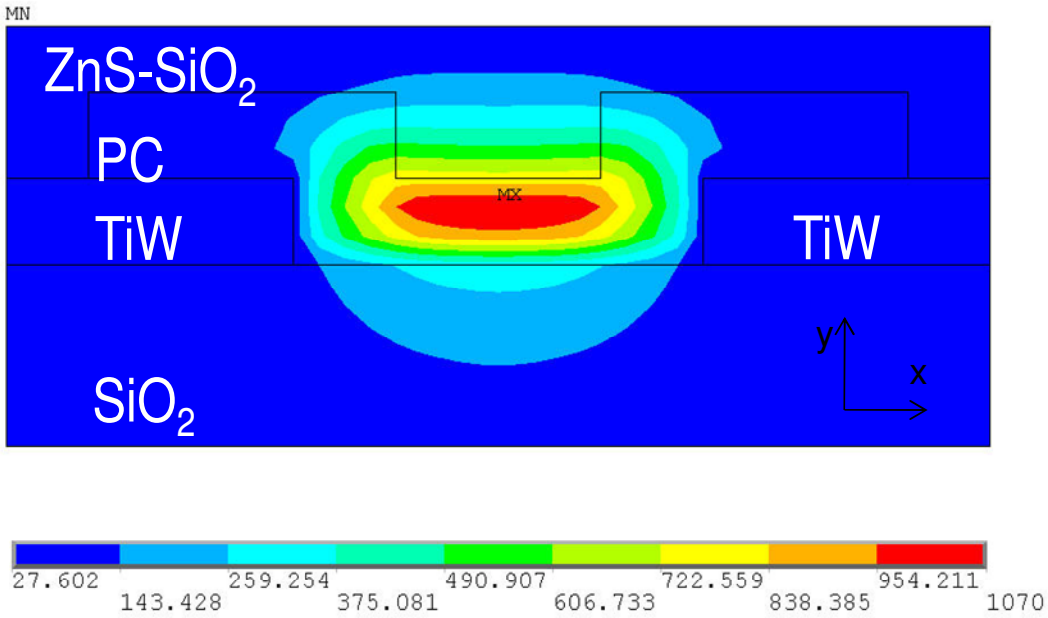


Figure 3.33 Temperature distribution of lateral PCRAM when a phase-change material has a thermal conductivity Tx=Ty=25%.

Peak temperatures of lateral PCRAM devices using phase-change materials with different thermal conductivities are summarized in Figure 3.34. It can be seen that the peak temperature changed slightly when thermal conductivity of the phase-change materials is reduced by 0, 25, 50, and 75% in x-direction. The corresponding peak temperatures were 636, 654, 671 and 685^{o}C, respectively. In contrast, the peak temperature increases significantly when thermal conductivity of the phase-change materials is reduced by 0, 25, 50, and 75% in y-direction. The corresponding peak temperatures were 636, 686, 771 and 967 ^{o}C, respectively. It means that it is more effective to vary the thermal conductivity of the phase-change materials in the y-direction than that in the x-direction for reducing the power consumption in lateral PCRAM devices. The effect becomes more obvious when the thermal conductivity of the phase-change materials is reduced by 0, 25, 50, and 75% in both x- and y-directions. The peak temperatures were higher of 636, 705, 819, and 1070^{o}C, respectively.

From the simulation results, it can be summarized that the reduction of thermal conductivities of phase-change materials in the y-direction is more effective than in the x-direction for reducing power consumption in lateral PCRAM devices. Since the thermal conductivities of SLL structures can be reduced in both x- and y-directions, lateral PCRAM devices with the SLL structure can potentially achieve very low power consumption.

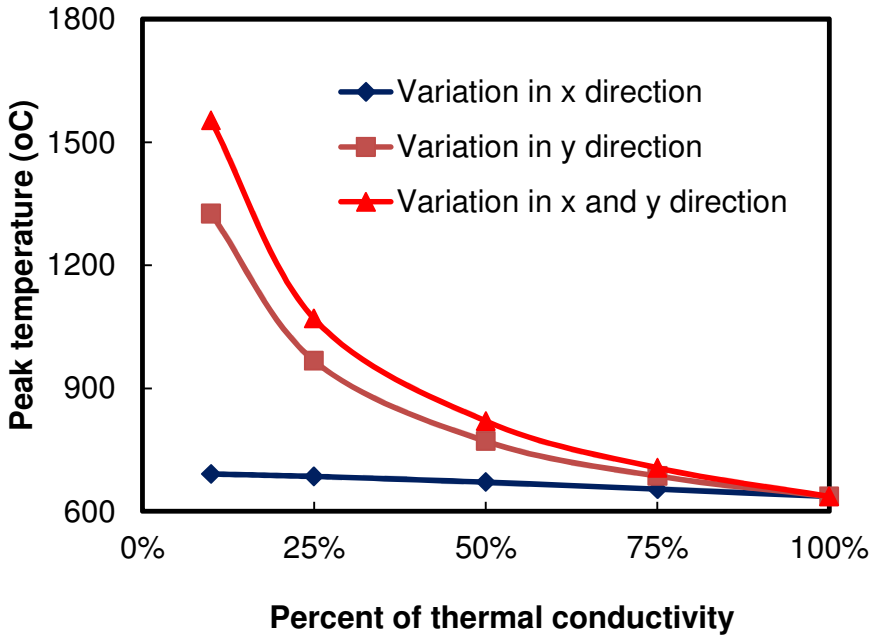


Figure 3.34 Thermal conductivity dependent peak temperature of phase-change materials.

3.5 Summary

To decrease the plastic deformation and extend the lifetime of lateral PCRAM devices, SLL structure was proposed to apply in lateral PCRAM device. The concept of GD SLL phase-change structure with two binary phase change materials was proposed and realized by the incorporation of GeTe and Sb_7Te_3. The crystallization temperature of bulk GeTe, bulk Sb_7Te_3 and GeTe/Sb_7Te_3 SLL structure were measured by ETTM. The crystallization temperature and resistivity of GeTe, Sb_7Te_3 and GeTe/Sb_7Te_3 SLL structure are thickness dependent, thinner films have higher crystallization temperature. No phase-change was observed when the GeTe and Sb_7Te_3 film thickness of less than 2.5 nm is employed. Crystallization of GeTe/Sb_7Te_3 SLL phase change structure shows a single-threshold, indicating that it is an ideal candidate for lateral PCRAM devices. Both the crystallization and melting temperatures of GeTe/Sb_7Te_3 SLL phase change structure

were measured with a phase change temperature tester. It was found that the T_x and T_m of the GeTe/Sb_7Te_3 SLL phase-change structure could be tuned by varying the thickness ratio of GeTe/Sb_7Te_3. The crystallization temperature of GeTe/Sb_7Te_3 SLL phase change structure increases with thickness ratio. GeTe/Sb_7Te_3 SLL structure built at a thickness ratio of 1.6 (GeTe to Sb_7Te_3) exhibited the lowest melting temperature of 535 ^oC. By incorporating GeTe/Sb_7Te_3 SLL phase change structure with the optimal thickness ratio of 1.6 into a lateral PCRAM device, stable SET/RESET behavior was demonstrated. A low RESET current of 1.5 mA and fast SET pulse of 30 ns were achieved, which is comparable with the results of previous reports, even though the cell size employed in this work is significantly larger by 20 times. The low RESET current of lateral PCRAM device results from the low thermal conductivity of SLL structure, which is confirmed by thermal simulations. High endurance above 10^6 cycles with a consistent ON/OFF ratio of 20 was demonstrated by the SLL lateral PCRAM devices. The transient effect study on the lateral PCRAM devices with SLL structure was conducted, which confirms that the GeTe/Sb_7Te_3 SLL structure is growth-dominant phase change material. Thermal simulation shows that SLL structure may reduce the power consumption due to the better thermal confinement.

Chapter 4 Edge-Contact Lateral PCRAM with SLL Structure Phase Change Medium

4.1 Introduction

In Chapter 3, growth-dominant SLL structure was proposed to apply in lateral PCRAM devices to extend the endurance. But power consumption of PCRAM devices is still one of the key issues for its application in portable consumer electronics. Hence, it is important to further decrease the power consumption by optimizing the structure of lateral PCRAM devices.

Lateral PCRAM structure is a promising structure for reducing the RESET current of PCRAM [103-108]. However, the lateral PCRAM structure is still not optimized. The contact area between the phase-change line and electrodes is large as it includes both top and edge contacts (see Figure 3.21). Hence, the heat loss is high and this results in a large RESET current. To achieve high density data storage, the size of the lateral PCRAM cells needs to be further reduced. If the bridge size becomes smaller and distance of electrodes becomes shorter, this problem will worsen as the active region is nearer to the electrodes, which inhibits the reduction of lower power consumption when the size of lateral PCRAM devices reduces. New structures for lateral PCRAM devices are required.

Edge-contact structure presents a good solution to reduce the RESET current of PCRAM as it reduces the contact area between phase change material and bottom electrode (see Figure 4.1) [94]. With this structure, the contact area between the phase-

change material and electrode layers is only determined by the electrode width and thickness. As the electrode thickness can be less than several ten nanometers, the contact area can be reduced significantly. Results have shown that edge-contact structures can be used to improve the thermal confinement in edge-contact type PCRAM, and reduce its RESET current. However, this structure only reduces the contact area between the bottom electrode and phase-change layer. The contact area between the top electrode and phase-change layer is not confined at all. With PCRAM cell size scaling, active region is nearer to both top and bottom electrodes. If the contact area of phase-change layer to top electrode is large, heat still can be dissipated via the top electrode. The contact areas to both top and bottom electrodes are critical to determine the RESET current.

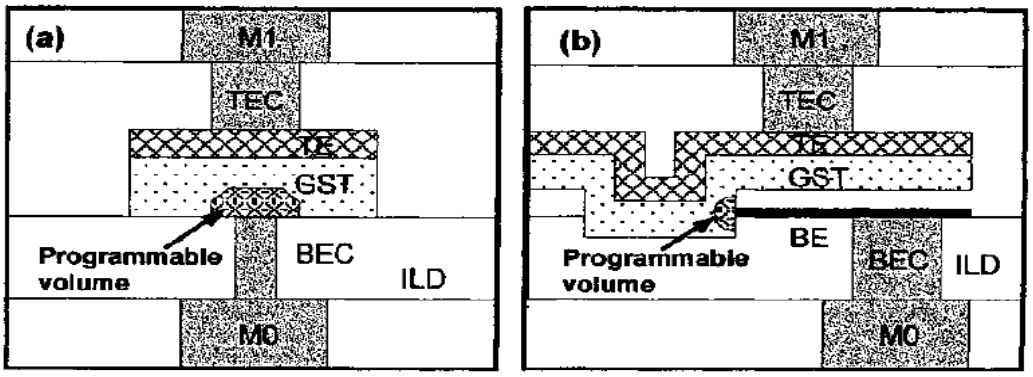


Figure 4.1 (a) Bottom contact PCRAM device and (b) Edge contact PCRAM device [94].

Until now, there is no report about the use of edge-contact structure in lateral PCRAM with SLL structure. In this Chapter, we develop a new edge-contact lateral PCARM with GeTe/Sb_7Te_3 SLL structure to reduce the RESET current.

4.2 Edge-contact lateral PCRAM structure

Referred to the edge-contact PCRAM structure, edge-contact lateral PCRAM structure was proposed. Figure 4.2 shows the schematic diagram of the edge-contact

lateral PCRAM. A thin dielectric layer is inserted between the phase-change material and the top of electrodes. The contact area between phase change material and both electrodes is thus significantly reduced. The contact area is only controlled by the thickness of the electrode, and the width of the phase-change bridge.

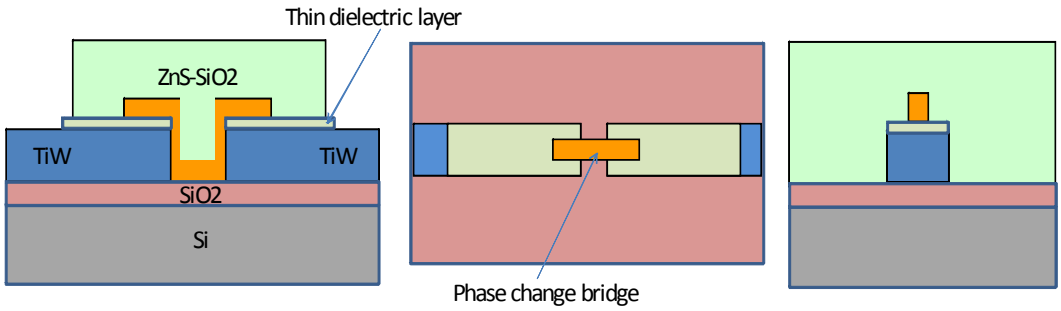
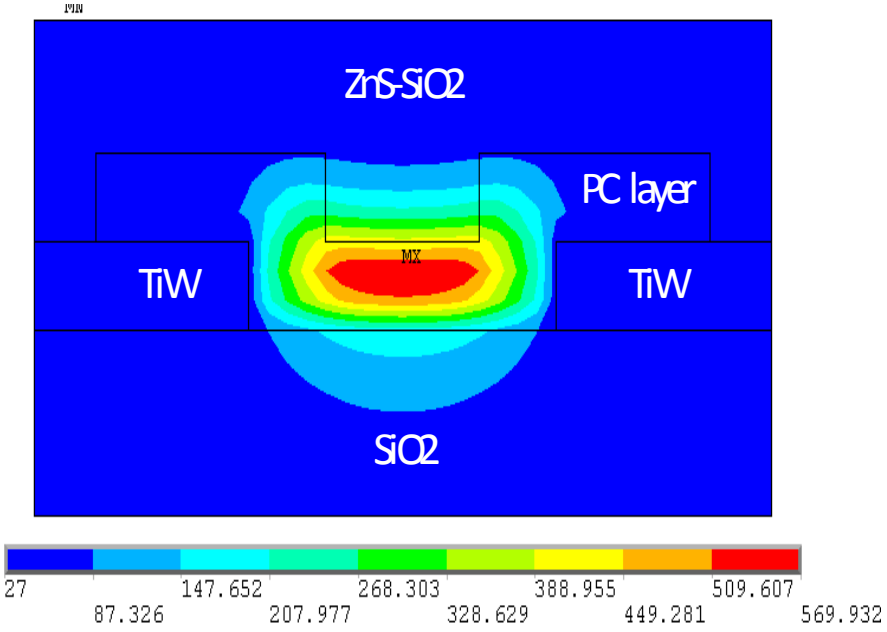


Figure 4.2 (a) Cross-section view, (b) top view, and (c) side view of the edge-contact lateral PCRAM device

4.3 Thermal simulation of edge-contact lateral PCRAM

Thermal simulations were performed on normal and edge-contact lateral PCRAM devices. The simulation model and material parameters were identical to those described in section 2.4. For the normal lateral PCRAM device, two 100 nm thick TiW electrodes were formed on each side of the phase-change line structure. The electrodes were separated by 0.5 µm. The $Ge_2Sb_2Te_5$ phase-change line structure is 3 µm long and 1 µm wide, and capped with a 200 nm thick ZnS-SiO_2 (see Figure 3.21). For the edge-contact lateral PCRAM device, the structure is identical to that of the normal lateral PCRAM device, except that a 30nm thick ZnS-SiO_2 is inserted between the phase-change material and bottom electrode (see Figure 4.2). The same power is applied to both the structures.



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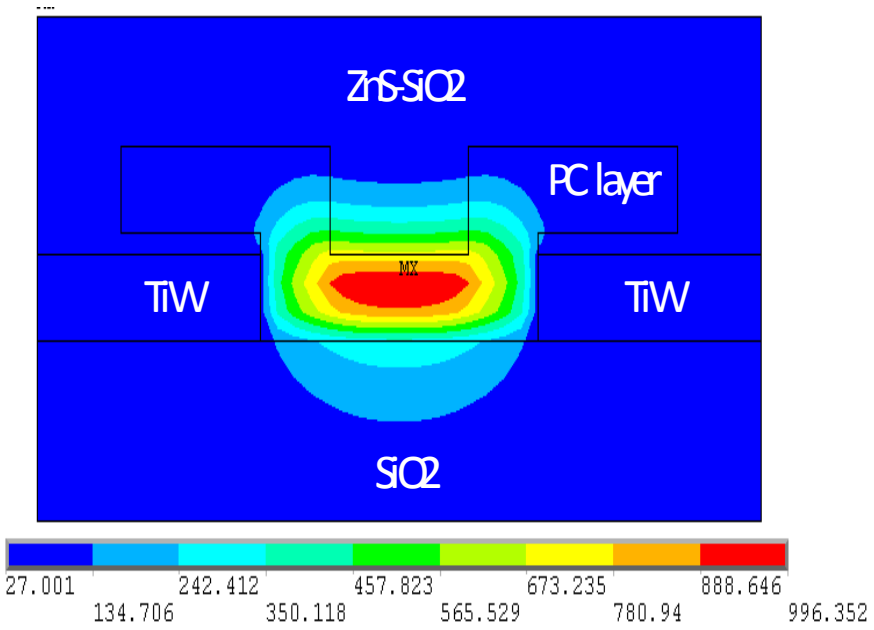


(b)

Figure 4.3 Simulated temperature of the (a) normal and (b) edge-contact lateral PCRAM cells. The pulse duration is 30ns and the same current amplitude is applied.

Thermal distributions of the normal and edge-contact lateral PCRAM devices are shown in Figure 4.3. The simulation results show that the peak temperature in the edge-contact device (996 ^{o}C) is much higher than that of the normal device (570 ^{o}C) (see Figure 4.2). This suggests that the edge-contact lateral PCRAM device has a better thermal confinement, and can be operated at a lower RESET current than the normal lateral PCRAM device.

4.4 Experimental results

4.4.1 Edge-contact lateral PCRAM device with SLL structure

Edge-contact lateral PCRAM devices with GeTe/Sb_7Te_3 SLL structure were fabricated. Schematics of the edge-contact lateral PCRAM device with SLL structure and the ternary alloy phase diagram are shown in Figure 4.4. The two component phase change materials are GeTe and Sb_7Te_3. The edge-contact lateral PCRAM devices with GeTe/Sb_7Te_3 SLL medium were fabricated using the identical fabrication process and equipments as described in Chapters 2 and 3. For comparison, normal lateral PCRAM cells with GeTe/Sb_7Te_3 SLL structure were also fabricated. Two 100 nm thick TiW electrodes were deposited, and they were separated by 0.5 μm. For the edge-contact lateral PCRAM devices, thin ZnS-SiO_2 film (30 nm) was deposited on top of the two electrodes. The GeTe/Sb_7Te_3 SLL medium was capped with a 200 nm thick ZnS-SiO_2, which had a length and width of 3 μm and 1 μm, respectively (see Figure 4.4). In this work, a pair of GeTe/Sb_7Te_3 was defined as a period, and each period had a thickness of 12.5 nm. Four periods were grown, and the total thickness of GeTe/Sb_7Te_3 SLL medium is 50 nm. In Chapter 3, normal lateral PCRAM devices with SLL structure showed the

best performance when the thickness ratio of GeTe to Sb_7Te_3 is 1.6. Hence, GeTe/Sb_7Te_3 SLL structure at a thickness ratio of 1.6 is also applied in the edge-contact lateral PCRAM devices.

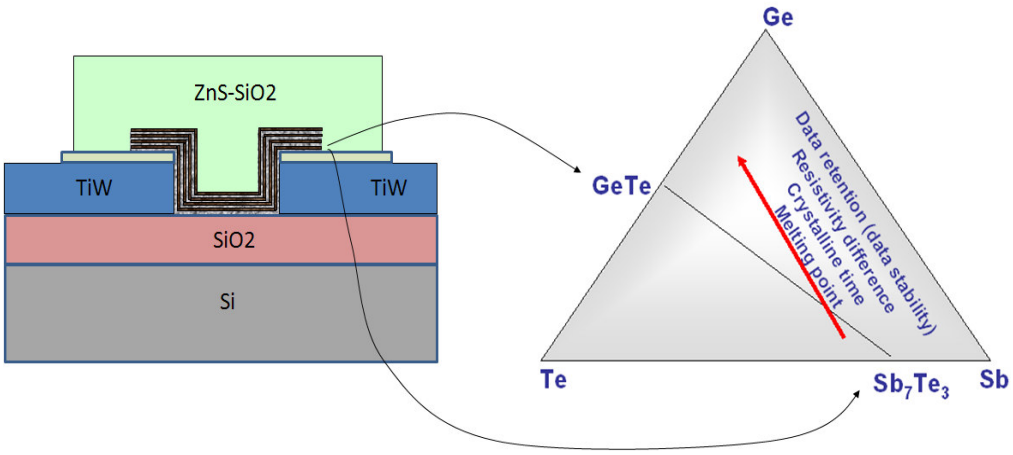


Figure 4.4 Schematics of the edge-contact lateral PCRAM with SLL structure medium, and the ternary alloy phase diagram

4.4.2 *I-V* curve of edge-contact lateral PCRAM

Both the normal and edge contact lateral PCRAM devices with SLL structure were tested with the Keithley semiconductor characterization system. Figure 4.5 shows the *I-V* curves for SET and RESET states by sweeping the current from 0 to 100 μA. From Figure 4.5, it can be seen that the threshold voltage V_{th} of the edge-contact lateral PCRAM cell is larger than that of normal lateral PCRAM. However, the threshold current I_{th} of the edge-contact lateral PCRAM is much lower (around 3.0 μA) than that of normal lateral PCRAM devices (around 12.0 μA). This implies that the edge-contact lateral PCRAM can operate with lower current.

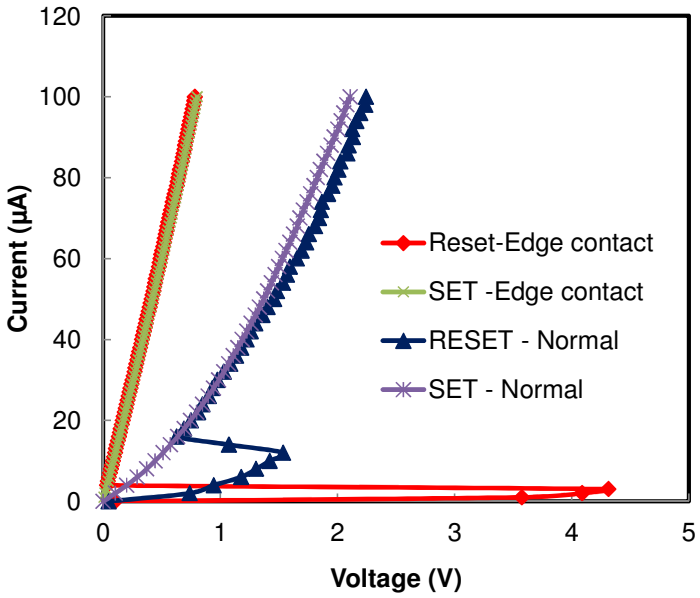


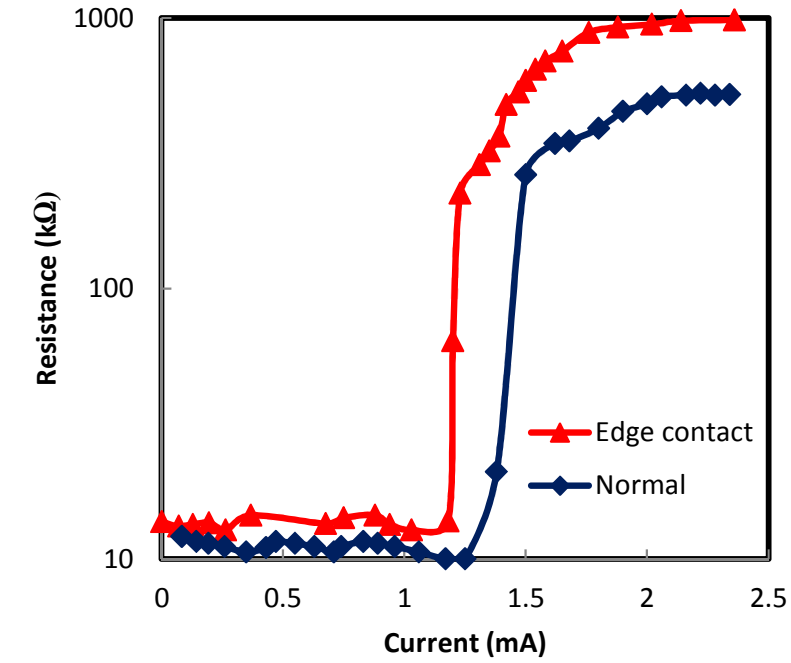
Figure 4.5 *I-V* characteristics of the SET and RESET states in the normal and edge-contact lateral PCRAM device with SLL structure.

4.4.3 RESET and SET R-I curve of edge-contact lateral PCRAM devices

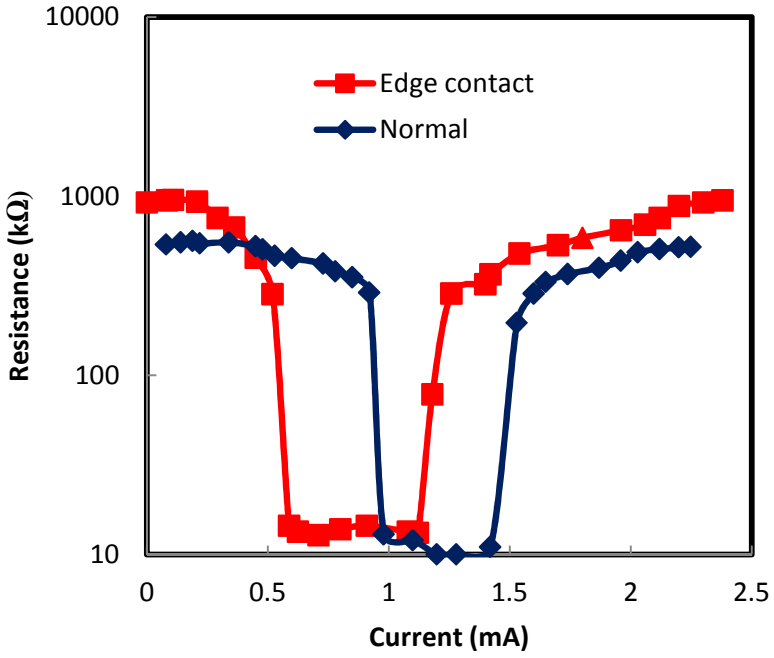
Both the normal and edge-contact lateral PCRAM devices with SLL structure were also tested using a self-developed PCRAM tester, as shown in Chapter 2. The RESET and SET resistance-current (R-I) curves are plotted in Figure 4.6 (a) and (b). The pulse duration is kept constant at 30 ns. From Figure 4.6 (a), it can be seen that the RESET current for the edge-contact lateral PCRAM device is 1.2 mA whereas that for the normal lateral PCRAM device is 1.5 mA. The RESET current reduction is about 20% with the edge-contact structure. From Figure 4.6 (b), it can be seen that the SET current for the edge-contact lateral PCRAM device is 0.6 mA while that for the normal lateral PCRAM device is 0.98 mA. The SET current reduction is about 40% with the edge-contact structure. This agrees well with the simulation results.

We compared the results obtained in previous work and in this work (see Table 4.1). Although the cross-section area of the edge-contact lateral PCRAM with SLL medium is about 20 times larger than the others, their RESET currents are comparable. It could be interpreted by two possible reasons. One is the edge-contact lateral structure has a smaller contact area between phase change material and both electrodes, which improves the thermal confinement. Hence, heat cannot be dissipated easily from phase change layer to electrodes. This was confirmed by the thermal simulations. The other reason lies in the SLL structure. Its thermal conductivity is reduced due to interface phonon scattering within the super-lattice structure. Thus the thermal confinement inside phase change layer is improved. Heat cannot be conducted outside of phase change layer easily. Based on these two factors, edge-contact lateral PCRAM devices obtain the improved thermal confinement and can be operated with lower RESET current.

From Figure 4.6 (b), it can be observed that both the normal and edge-contact lateral PCRAM devices with SLL structure can be SET to the crystalline state with a 30 ns pulse easily. For the normal lateral PCRAM devices, the SET current ranges from 0.98 to 1.42 mA, while that for the edge-contact lateral PCRAM is between 0.59 and 1.12 mA. The SET process for the lateral PCRAM devices with SLL structure is fast maybe due to that fact that Sb_7Te_3 have fast crystallization speed. The GeTe/Sb_7Te_3 SLL structures are growth-dominant phase change material and the crystal growth speed is much faster than nucleation speed. Hence the crystallization process is much faster and the SET process can be finished in shorter time.



(a)



(b)

Figure 4.6 (a) RESET, and (b) SET R-I curves (with 30 ns pulse) for the normal and edge-contact lateral PCRAM with SLL structures.

Table 4.1 RESET current comparison between the edge-contact lateral PCRAM devices with SLL structure and other devices

		Contact area (μm^2)	Cross-Section (nm^2)	line length (nm)	RESET pulse Width (ns)	RESET current (mA)
Philips (2005) [103]		≥ 8	2500	500	30	≥ 1
IBM (2007) [105]		≥ 0.1	2500	50	\	≥ 1
This work	Lateral PCRAM with $Ge_2Sb_2Te_5$	1.1	50000	500	60	2.5
	Normal Lateral PCRAM with SLL	1.1	50000	500	30	1.5
	Edge- contact Lateral PCRAM with SLL	0.1	50000	500	30	1.2

Figure 4.7 shows the RESET *R-I* curve for the edge-contact lateral PCRAM device with different pulse widths varying from 10 to 50 ns. It can be seen that the edge-contact lateral PCRAM device can be RESET from around 10 to 1000 kΩ with pulse width longer or equal to 20 ns. RESET process cannot be realized with a 10 ns pulse even with very high current amplitudes. When longer RESET pulse is employed, RESET current becomes lower. For pulse widths of 20, 30 and 50 ns, the corresponding RESET currents are 1.76, 1.23 and 1.03 mA, respectively.

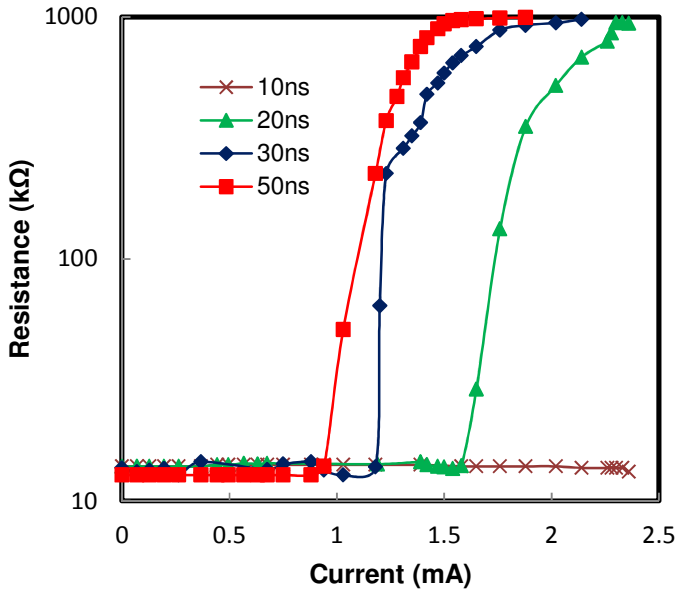


Figure 4.7 RESET *R-I* curve of the edge-contact lateral PCRAM devices with SLL structures switched with different pulse widths.

Figure 4.8 shows the SET *R-I* curves for the edge-contact lateral PCRAM devices switched with different pulse widths varying from 10 to 50 ns. It can be observed that the edge-contact lateral PCRAM device cannot be SET to the crystalline state when pulse width is less or equal to10 ns even being applied with very high current amplitudes. If pulse width is longer or equal to 30 ns, the device can be SET from about 1000 to 10 kΩ. With a longer pulse width is employed, the SET current becomes lower. For 30 and 50 ns SET pulses, the corresponding SET currents are 0.59 and 0.45 mA.

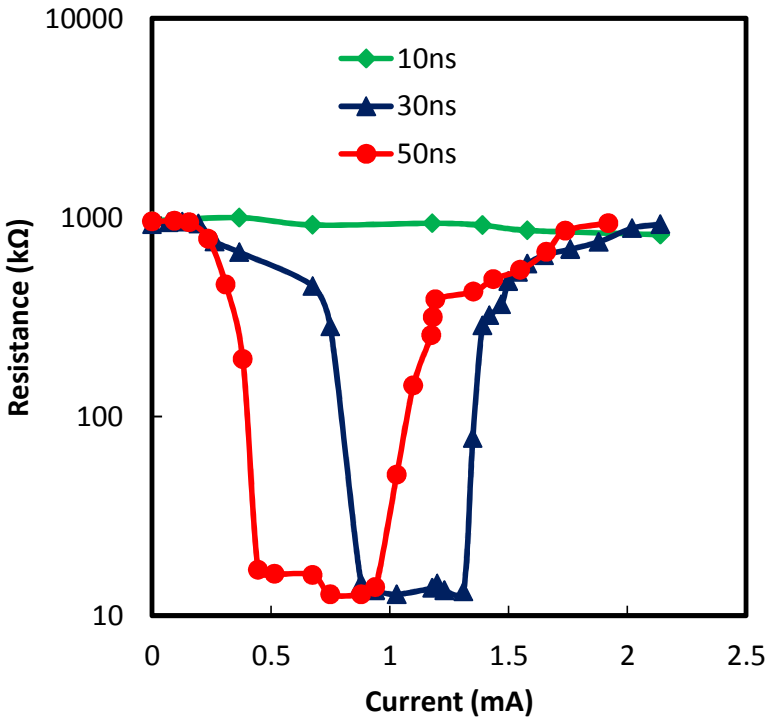


Figure 4.8 SET *R-I* curves of the edge-contact lateral PCRAM devices with SLL structures switched with varying pulse widths.

4.4.4 Cycle endurance of edge-contact lateral PCRAM devices

Cycle endurance tests were performed on both the normal and edge-contact lateral PCRAM devices with SLL structure. Figure 4.9 shows the cycle endurance results for both the normal and edge-contact lateral PCRAM devices with SLL structure. Both normal and edge-contact lateral PCRAM devices with SLL structure can achieve endurance higher than 10^5 times. It can be observed that the edge-contact structure lateral PCRAM devices have a better device's stability. After 10^5 cycles, the RESET/SET resistance ratio for normal device is only above 20, while that for edge-contact device is above 100. With this high RESET/SET resistance ratio advantage, edge-contact lateral PCRAM devices can be used for a special applications, for instance as a switch.

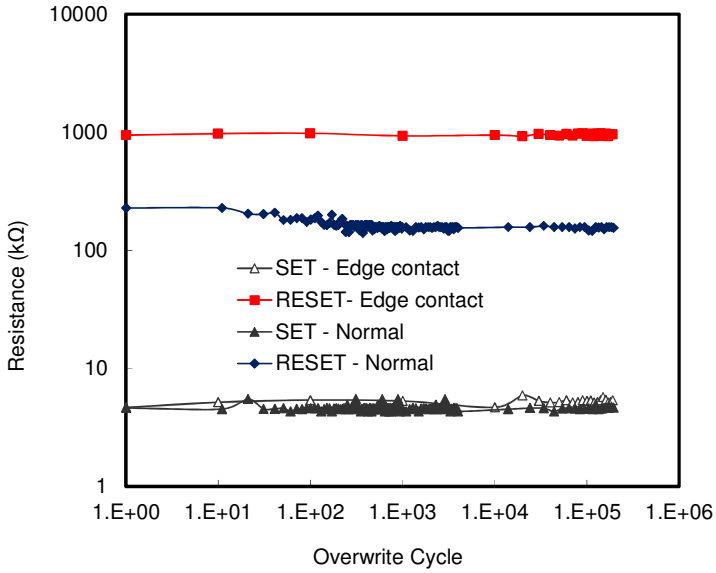


Figure 4.9 Cycle endurance of normal and edge-contact lateral PCRAM devices with SLL structure. Lifetime is more than 10^5 overwriting cycles.

4.5 Summary

Edge-contact lateral PCRAM devices with GeTe/Sb_7Te_3 SLL medium was proposed and demonstrated. Based on the simulation results, it can be observed that the thermal confinement can be improved with the edge-contact structures. Both normal and edge-contact lateral PCRAM devices with GeTe/Sb_7Te_3 SLL medium were fabricated and compared. Using edge-contact structures, RESET current was decreased to 1.2 mA from 1.5 mA (normal structure). The resistance ratio between the RESET and SET states is increased to above 100 times from 20 times (Normal structure). Good stability and resistance ratio after 10^5 overwriting cycles were achieved.

Chapter 5 Multi-level lateral PCRAM with SLL structure

5.1 Introduction

One of the most critical factors to hinder PCRAM devices occupying the market is its cost. To lower the cost of PCRAM devices, it is important to increase the PCRAM device density and storage capacity. Lateral PCRAM devices also meet same issues. To increase data storage capacity of lateral PCRAM devices, three methods can be used: 1. To increase area density through scaling; 2. To increase volume density with 3D stack technology; 3. To apply multi-level programming to store multi-bits per cell. The first method will meet obstacles because phase-change bridges cannot shrink unlimitedly. The reported phase-change bridges were already shrunk to around ten nanometers [103, 105] and the efforts to increase data storage capacity through further scaling of lateral PCRAM devices will face problems, such as (i) process technology and (ii) phase-change material physical limitation [155]. For process technology, it is limited by many factors, such as lithography and deposition technologies. For the second method, 3D stack technology is very complicated for non-volatile memories and high performance diode is needed. It is very time costly to develop 3D stack technology. With many years development, 3D stack flash memory is almost mature [163]. However, it is at the initial development stage for phase change random access memory [164]. Compared to the first two methods, multi-level data storage can increase the storage capacity of PCRAM more significantly.

Actually, several methods have been proposed to implement the multi-level storage in mushroom structure PCRAM [165]. For lateral PCRAM devices, You Yin et al reported their multi-layer SbTeN/TiN stack structure to achieve multi-level storage [107]. With the TiN application for the stack structure, the RESET resistance is too low and the RESET current will be higher. In this work, we proposed two solutions to realize multi-level storage for lateral PCRAM based on GeTe/ Sb_7Te_3 SLL structure and a novel super-lattice like (SLL) structure incorporating a phase-change material and a dielectric material.

5.2 Multi-level effect in lateral PCRAM device with GeTe/Sb_7Te_3 SLL structure

5.2.1 RESET and SET R-I curve results and analysis

Multi-level effect has been investigated based on lateral PCRAM devices with GeTe/ Sb_7Te_3 SLL structure. The optimum thickness ratio of GeTe to Sb_7Te_3 is 1.6, as described in Chapter 3. Figure 5.1 shows the RESET and SET *R-I* curves of lateral PCRAM devices with SLL structure at a thickness ratio of 1.6. Constant pulse widths of 30ns were employed. It can be observed that both RESET and SET *R-I* curves have a very smooth slope. Many intermediate states can be achieved when different pulse amplitudes are applied. For RESET, different RESET resistances of 263, 350 450 and 520 kΩ can be achieved with 30 ns pulses of 1.5, 1.68, 1.9 and 2.22 mA. The initial SET resistance is kept constant at 20kΩ. This can be attributed to the change in the amorphous volume in the SLL structure when different RESET pulse amplitudes were employed. RESET involves the change in the active region from a crystalline state to an amorphous

state. When a higher RESET current is used, both the melting region and amorphous volume will be larger. The resistance of lateral PCRAM devices will be higher.

For SET, different SET resistance of 450, 380 290 and 22 kΩ can be achieved with 30ns pulses of 0.6, 0.78, 0.92 and 1.1 mA. The initial RESET resistance is kept constant at 550 kΩ. This could be explained by the difference in the crystallization volume in the SLL structure when different SET pulse amplitudes were employed. SET involves the change in the active region from an amorphous state to a crystalline state. When a higher SET current is employed, the volume over the crystalline temperature and below melting temperature will be larger. The crystallization volume is larger and the resistance of the lateral PCRAM device becomes lower. Hence, proper selection of RESET and SET pulses enables the achievement of multi-level states in lateral PCRAM devices with GeTe/ Sb_7Te_3 SLL structure.

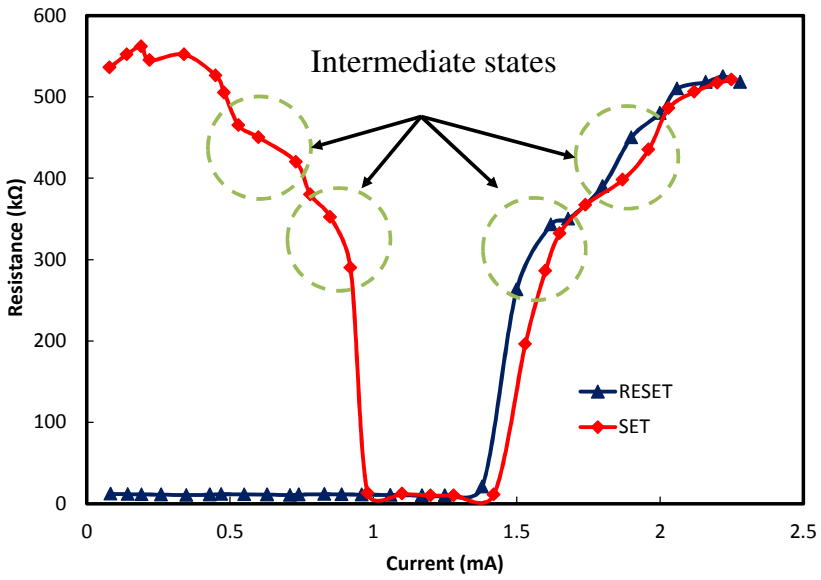


Figure 5.1 RESET and SET *R-I* curves of lateral PCRAM devices with GeTe/ Sb_7Te_3 SLL structure using a thickness ratio of 1.6. The pulse width is kept constant at 30 ns.

5.2.2 Multi-level effects of lateral PCRAM devices with GeTe/Sb_7Te_3 SLL structure

As mentioned in section 5.2.1, many intermediate states can be achieved in lateral PCRAM. In this section, different pulses were applied to investigate whether multi-level storage can be realized in lateral PCRAM devices with GeTe/ Sb_7Te_3 SLL structure. Figure 5.2 shows the overwriting cycle of a lateral PCRAM device with GeTe/ Sb_7Te_3 SLL structure with three different pulses. Figure 5.2 shows that three different resistance levels can be achieved using these three different pulses applied. The corresponding resistance levels are around 30, 100, and 350 kΩ. The corresponding pulse conditions are of 800 ns / 0.34 mA, 30 ns/1.9 mA and 50 ns/2.34 mA, respectively.

However, the drawback of this design is that different states are realized via the change in the amorphous or crystalline volumes in the GeTe/ Sb_7Te_3 SLL structure. During overwriting, the heat can be accumulated and the active volume may change, which will cause the resistance to change. This can cause the different states to become unstable. Figure 5.2 shows that the resistance of lateral PCRAM devices changes after 20 overwriting cycles. Level 2 and 3 are two levels with different RESET pulses. Then different amorphous volumes are achieved and the devices will have different resistance. As heat cannot be conducted away quickly after the first RESET pulse, the base temperature will increase for second RESET pulse. Then the amorphous volume will be affected for level 3. Hence, the resistance of level 3 will be affected sometimes. A more stable approach is needed to achieve multi-level storage for lateral PCRAM devices.

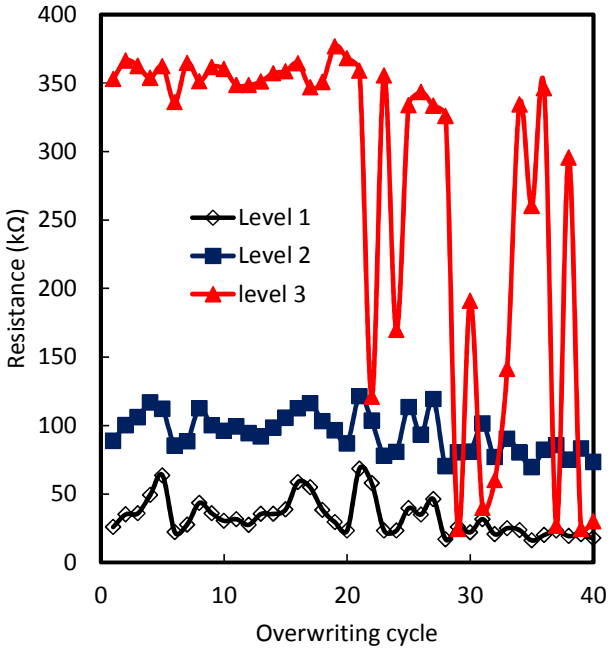


Figure 5.2 Overwriting cycle of multi-level lateral PCRAM devices with GeTe/Sb_7Te_3 SLL structure.

5.3 Edge-contact Lateral PCRAM with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure

5.3.1 New SLL structure concept

SLL structure incorporated with GeTe and Sb_7Te_3 were developed for lateral PCRAM devices to achieve better lifetime, lower power consumption and multi-level storage [148]. To obtain more stable multi-states, SLL structures were modified to achieve discrete multi-level storage for edge-contact lateral PCRAM devices. A dielectric material is proposed to replace one of the phase-change material components in the SLL structure. As the several phase-change layers were separated by dielectrics, it can be considered as many phase-change bridges are connected by the two electrodes. N-dope

Sb_7Te_3 and high thermal insulating ZnS-SiO_2 were selected to form this SLL structure. Schematic diagram of this SLL structure is shown in Figure 5.3. In order to form the new SLL structure, N-doped Sb_7Te_3 and ZnS-SiO_2 were deposited periodically on the substrate. Figure 5.4 shows the SEM image of this SLL structure. The interface between N-doped Sb_7Te_3 and ZnS-SiO_2 can be clearly seen from the SEM image.

As the thermal conductivity of ZnS-SiO_2 is low, heat can be confined in small separate regions and the melting region can be controlled within specific phase-change bridges, which enables programming the selected phase-change bridges. Hence, the different states can be achieved when different phase change bridges in the SLL structure were SET or RESET. In this section, we investigate multi-level storage using N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure in lateral PCRAM devices.

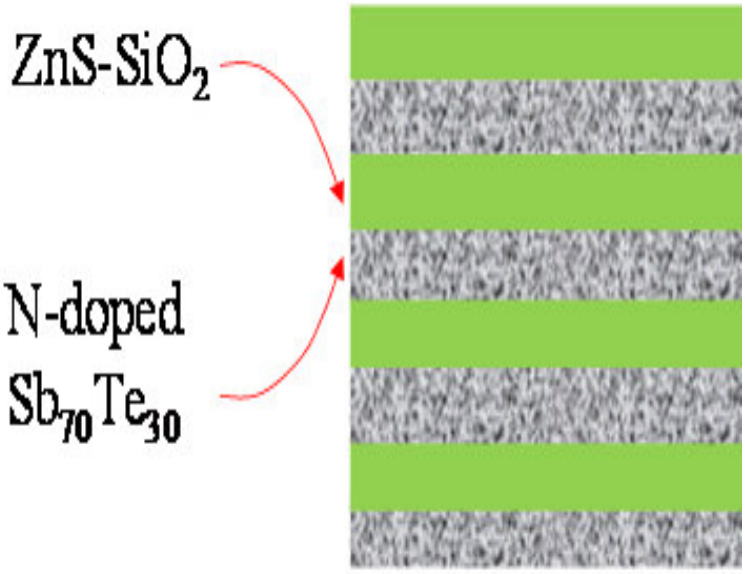
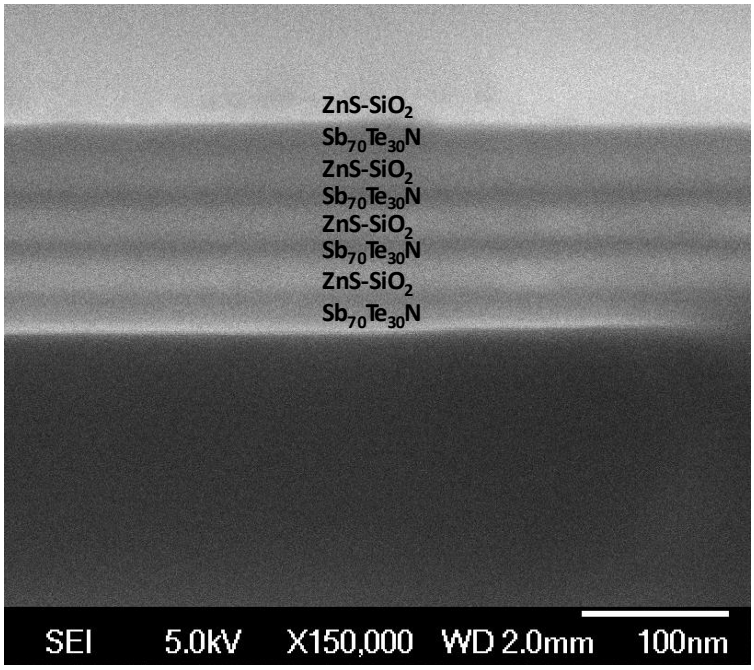


Figure 5.3 Schematic diagram of N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure



(b)

Figure 5.4 SEM image for N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure

5.3.2 Device structure and fabrication process of the edge-contact lateral PCRAM with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure

Figure 5.5 shows the schematic of the lateral PCRAM devices with the N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure. N-doped Sb_7Te_3 (N2/Ar flow rate is 2.5 /15sccm) and ZnS-SiO_2 were selected as the phase-change material and dielectric to form the phase-change bridge. The phase-change bridge consists of 4 cycles of 10 nm N-doped Sb_7Te_3 and 10 nm ZnS-SiO_2.

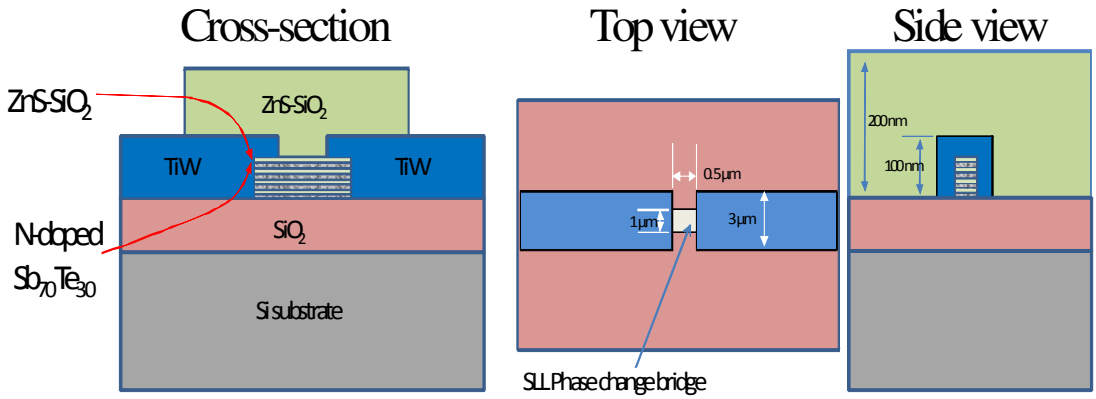


Figure 5.5 Schematic of the lateral PCRAM cell with the new SLL structure

The detail fabrication process steps for the lateral PCRAM devices with the N-doped Sb_7Te_3/ZnS-SiO_2 SLL structure can be seen in Figure 5.6. The process details and equipment used for each step is the same as that in Chapter 2. The first fabrication step is to form the phase-change bridge, which has a length and width of 3 μm and 1 μm. 4 periods of N-doped Sb_7Te_3 (10 nm in thickness) and ZnS-SiO_2 (10 nm in thickness) were deposited on the silicon substrate with a 1 μm thick thermal oxide. The second fabrication step is to form the two electrodes. Two 100 nm thick TiW electrodes were deposited, and they were separated by 0.5 μm. Then the contact area of electrodes to N-doped Sb_7Te_3 is only through the edge of the phase change bridge. This edge-contact structure implies that this device can achieve lower power consumption. The third step is to form the protective layer on the active region. A 200 nm thick ZnS-SiO_2 was deposited to cover the SLL structure phase change bridge.

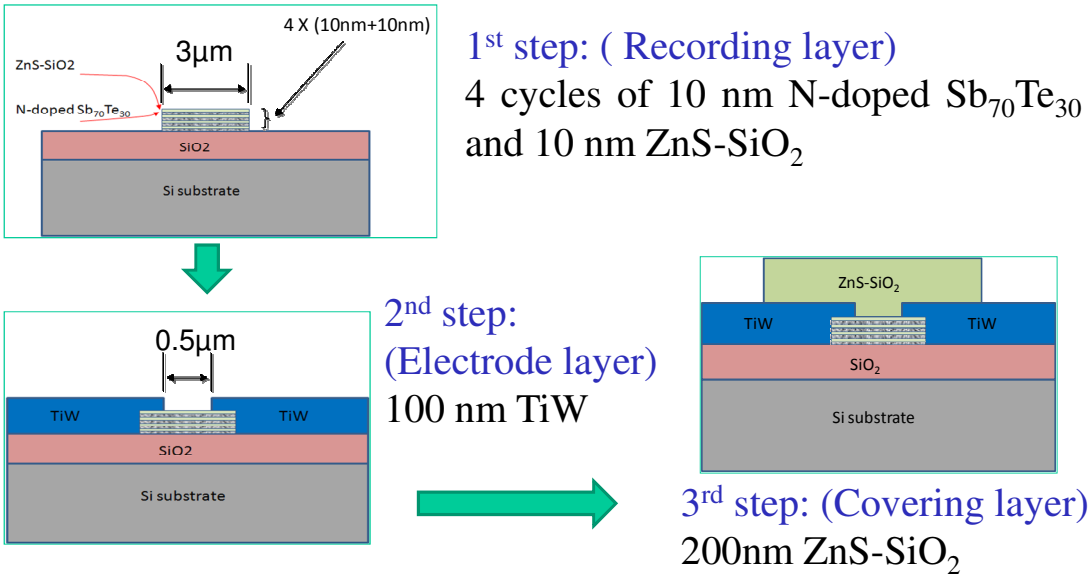


Figure 5.6 Fabrication steps for the lateral PCRAM devices with the N-doped Sb_7Te_3 and $ZnS\text{-}SiO_2$ SLL structure.

5.3.3 Static testing for I-V curve

Edge-contact lateral PCRAM devices with N-doped Sb_7Te_3 SLL structure were characterized using the Keithley semiconductor characterization system. Figure 5.7 shows the *I-V* curves for the devices with initial (i) amorphous state and (ii) crystalline state. The lateral PCRAM device current and voltage were measured when the current was swept from 0 to 200 μA. From Figure 5.7, it can be seen that the I-V curve of the amorphous state exhibits three apparent S-shaped switching at the voltages of around 2.05, 2.77 and 3.95 V, respectively. Correspondingly, the estimated device resistance *R* (*R* = *V*/*I*) shows three sudden drops, as shown in Figure 5.7. The three resistance drops were from the high-resistance state (‘0’ state) to the intermediate-resistance state (‘1’ state and ‘2’ state), and from the intermediate state to the low-resistance state (‘3’ state),

respectively. *I-V* curves for the crystalline state show that resistance remained almost constant after the third switching. It means that the low resistance state ('3' state) is stable, and no more states exist. Hence, it can be concluded that there are total 4 resistance levels appearing in this device referred to static testing results.

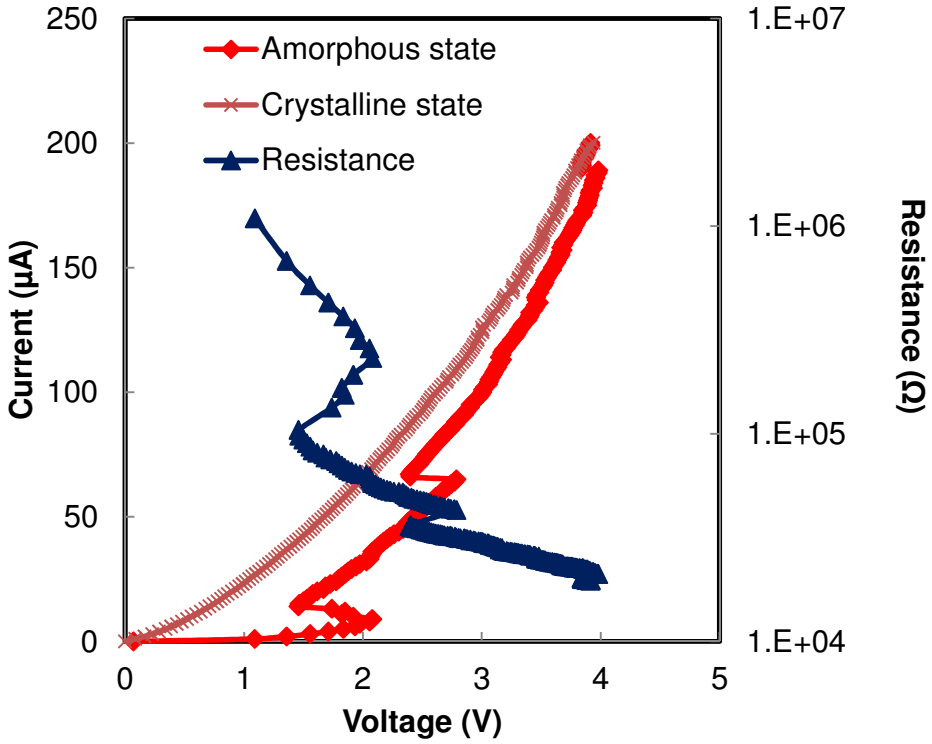


Figure 5.7 Static *I-V* curves of lateral PCRAM devices with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure.

5.3.4 Dynamic pulse testing for RESET R-V curve

The RESET and SET R-V curves of lateral PCRAM devices with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure were obtained using a self-built PCRAM tester as described in Chapter 2. The pulse width was kept constant at 60 ns. The RESET and SET

R-V curves are plotted in Figure 5.8. It can be observed that device resistance is initially of about 200 kΩ, and it remained stable for pulses ranging from 0 to 3.4 V. First switching occurred when the applied pulse was above 3.4 V, and the device resistance stayed at around 500 kΩ. Second switching took place at around 5.2 V, and the device resistance increased to around 1600 kΩ. Third switching took place at around 7 V, and the device resistance increased to around 2400 kΩ. It can be clearly seen from Figure 5.8 that the voltage-resistance states and programming windows are stable and large. The programming voltages to achieve the different states of "2" to "0" are 3.4 -5.0V, 5.2 - 6.8V and above 7.0V, respectively. The high resistance state can be reversibly switched to the low resistance state by applying a 400 ns voltage pulse at an amplitude of 1.6 V. Using dynamic pulse testing, 4 stable resistance levels were also achieved in the lateral PCRAM devices with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure.

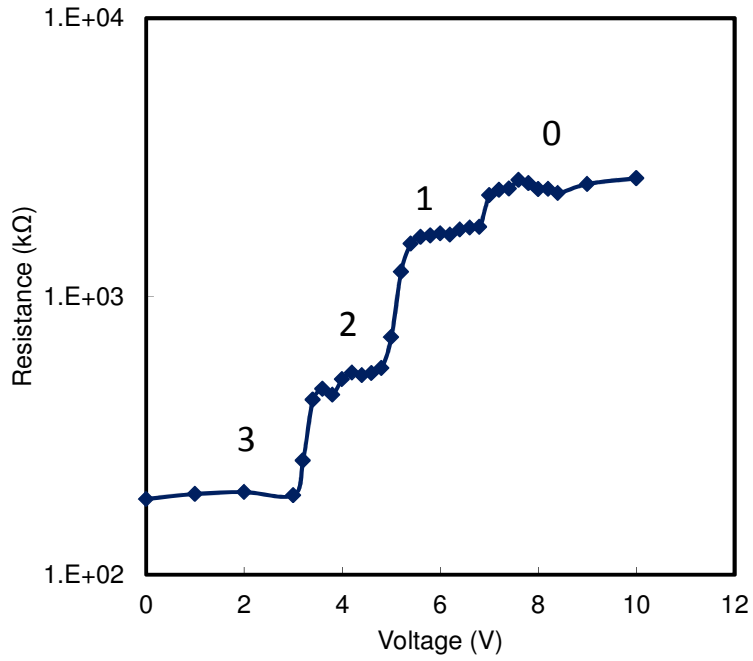


Figure 5.8 Dynamic pulse test R-V curve of lateral PCRAM with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure.

5.3.5 Multi-level storage mechanism investigation based on simulation

To investigate the multi-level storage mechanism in the lateral PCRAM devices with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure, electrical and thermal simulations were performed based on finite element method. Figure 5.9 shows the finite element model for the lateral PCRAM with SLL structure based on N-doped Sb_7Te_3 and ZnS-SiO_2. As the material properties of N-doped Sb_7Te_3 are dependent on the film thickness and nitrogen concentration, electrical and thermal simulations were done based on $Ge_2Sb_2Te_5$ material properties. The detail material properties used in this simulation are listed in Table 2.2. It is assumed that the melting temperature T_m and transition temperature T_x of N-doped Sb_7Te_3 are 600 ^oC and 200-400 ^oC, respectively. The initial state of the phase-change layer is assumed to be crystalline.

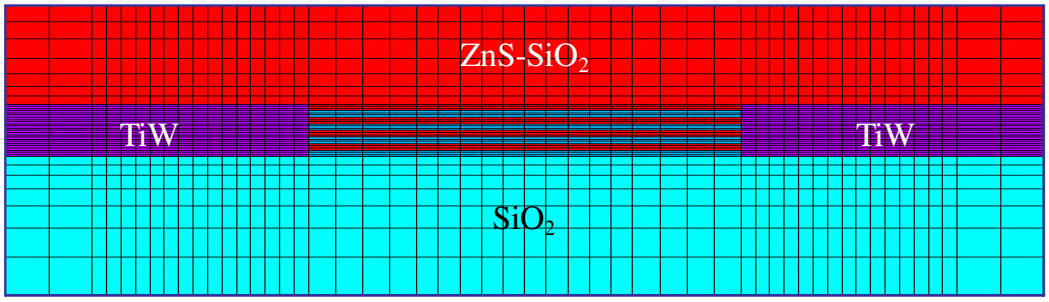
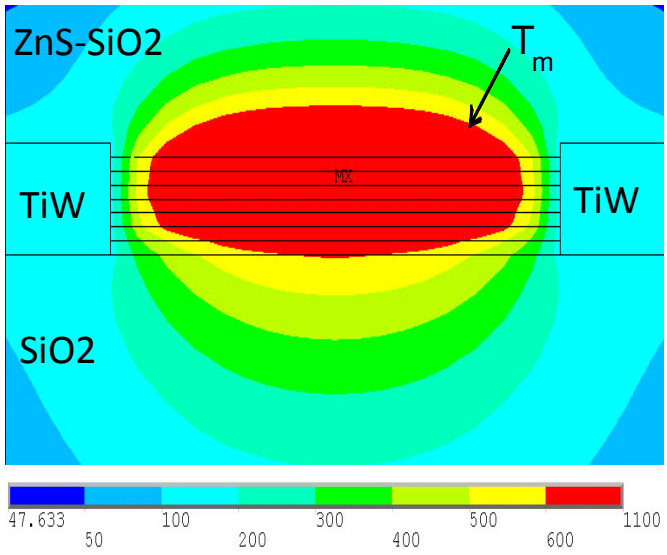


Figure 5.9 FEM model for the lateral PCRAM device with the new SLL structure

By applying different pulses, different temperature distributions in lateral PCRAM devices with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure were achieved (As seen in Figure 5.10(a) – Figure 5.13(a)). Figure 5.10(a) shows that the peak temperature region over melting temperature spreads across all the 4 layers of N-doped Sb_7Te_3 layers

when a pulse at an amplitude of 10V, and duration of 60 ns is applied. Figure 5.10(b) shows the corresponding state of the N-doped Sb_7Te_3 phase-change layers. It can be seen that all the 4 phase-change bridges are in the amorphous state. When a pulse with an amplitude of 8.5V, and duration of 60 ns is applied, the peak temperature region over melting temperature only spreads across 3 phase-change bridges (see Figure 5.11(a)). Hence, the corresponding state is that 3 of the 4 phase-change bridges are in amorphous state and the bottom 1 phase-change bridge is in crystalline state (See Figure 5.11(b)). When a pulse with an amplitude of 7.8V, and duration of 60 ns is applied, the peak temperature region over melting temperature only spreads across 2 phase-change bridges (see Figure 5.12(a)). The corresponding state in Figure 5.12(b) shows that 2 of the 4 phase-change bridges are RESET to amorphous state and the other 2 are still in crystalline state. Hence, different states of all 4, 3 and 2 of N-doped Sb_7Te_3 lines in amorphous state can be achieved when different pulses with amplitudes of 10V, 8.5V and 7.8V, and duration of 60 ns are applied. Ideally, the peak temperature spreading across 1 layer of N-doped Sb_7Te_3 lines can be also obtained. However, it cannot be achieved even with different pulse amplitudes at a fixed pulse duration of 60 ns. A possible reason is that the dielectric layer in between the N-doped Sb_7Te_3 layers is only 10 nm, and it is difficult to confine heat to activate only 1 layer. When a SET pulse with an amplitude of 4.5V, and duration of 400 ns is applied, the temperature distribution is shown in Figure 5.13(a). It can be seen that the region with temperatures between 200 to 400 ^{o}C is almost spread across all the 4 phase-change bridges. That means all 4 phase-change layers can be SET to the crystalline state (see Figure 5.13(b)).



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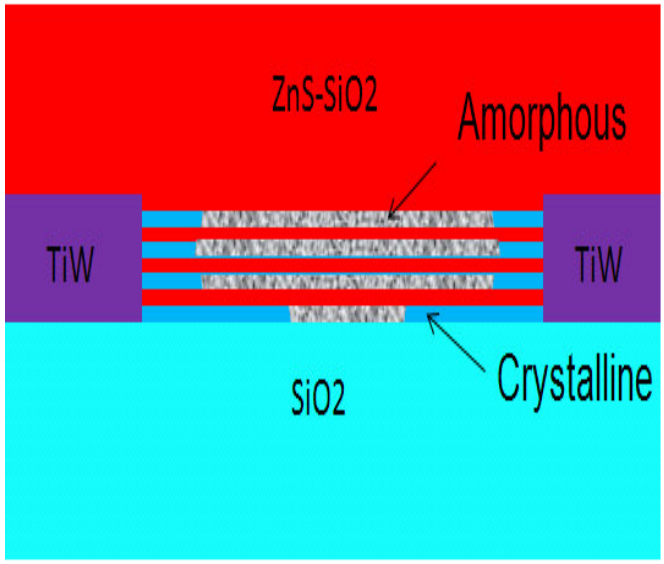
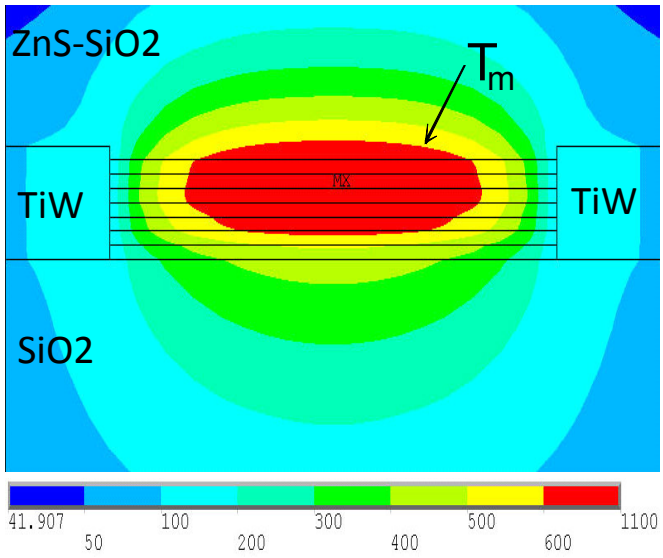


(b)

Figure 5.10 (a) Simulated temperature distribution in a lateral PCRAM device with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure when a RESET pulse at an amplitude of 10V, and duration of 60 ns is applied; and (b) the corresponding states of the 4 phase-change layers. All 4 phase-change layers are in the amorphous state, which corresponds to highest resistance state: “0”.



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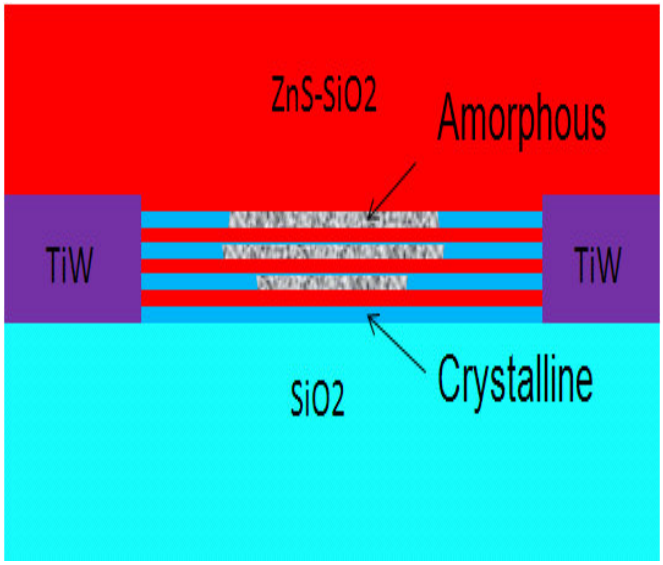
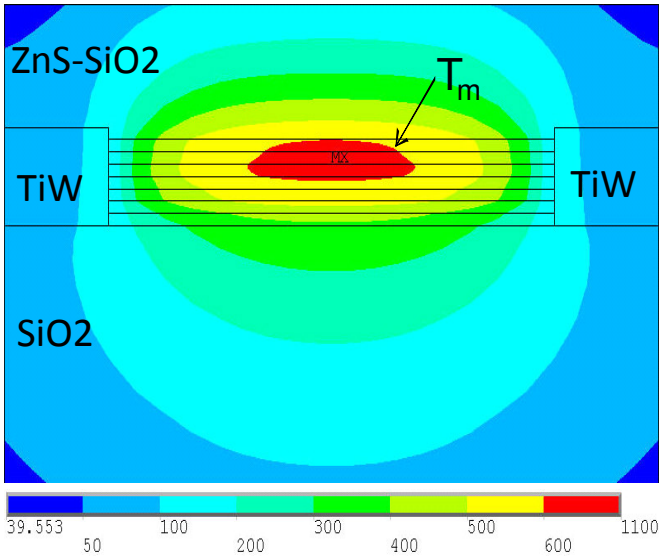


(b)

Figure 5.11 (a) Simulated temperature distribution in a lateral PCRAM device with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure when a RESET pulse at an amplitude of 8.5V, and duration of 60 ns is applied; and (b) the corresponding states of the 4 phase-change layers. Only 3 phase-change layers are in the amorphous state, which corresponds to highest resistance state: "1".



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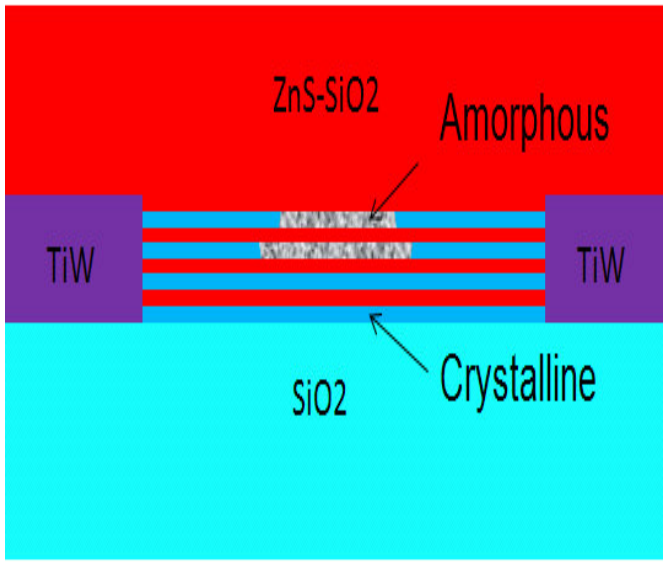
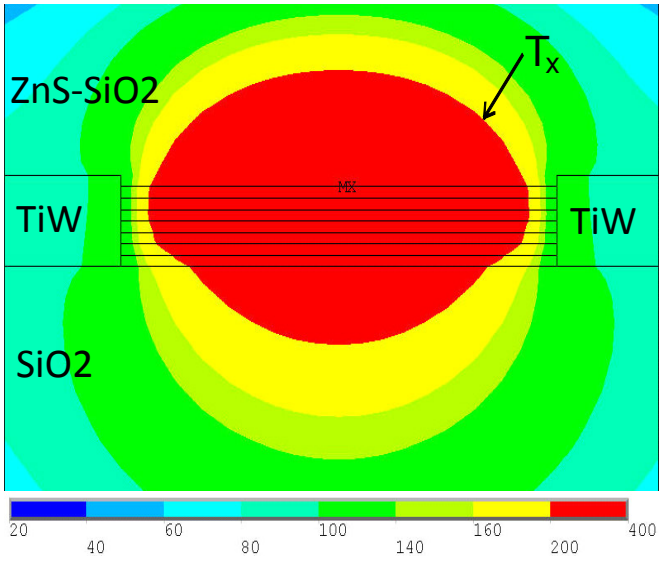


(b)

Figure 5.12 (a) Simulated temperature distribution in a lateral PCRAM device with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure when a RESET pulse at an amplitude of 7.8V, and duration of 60 ns is applied; and (b) the corresponding states of the 4 phase-change layers. Only 2 phase-change layers are in the amorphous state, which corresponds to highest resistance state: "2".



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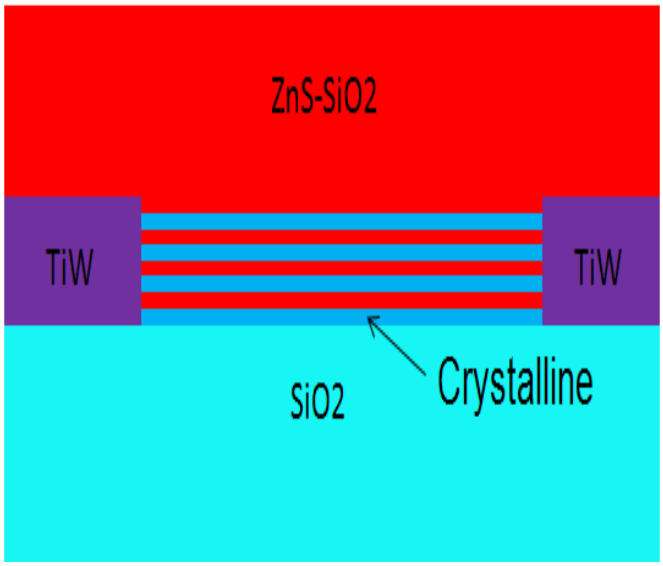

(b)

Figure 5.13 (a) Simulated temperature distribution in a lateral PCRAM device with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure when a SET pulse at an amplitude of 4.5V, and duration of 400 ns is applied; and (b) the corresponding states of the 4 phase-change layers. All 4 phase-change layers are in the crystalline state, which corresponds to highest resistance state: “3”.

As phase-change materials have a higher resistivity in the amorphous state (around 100 times) than in the crystalline state, the amorphous N-doped Sb_7Te_3 layers have a higher resistance than the crystalline N-doped Sb_7Te_3 layers. Parallel circuit model was used to describe the SLL structure system for simplification (see Figure 5.14). If we define the resistance of the amorphous and crystalline layer as R_H and R_L, the simulated 4 states correspond to 4 R_H, 3 R_H and 1 R_L, 2 R_H and 2 R_L, and 4 R_L in the parallel circuit. The resistance of the parallel circuit corresponding to the 4 states will have 4 different resistance levels: $R_H/4$, $R_HR_L/(R_H+3R_L)$, $R_HR_L/(2R_H+2R_L)$ and $R_L/4$, which means that multiple states exist in the lateral PCRAM device with SLL structure. The multiple states enable multi-level storage for lateral PCRAM devices with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure. As a result, we demonstrated the possibility of multi-level data storage in the lateral PCRAM devices with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure.

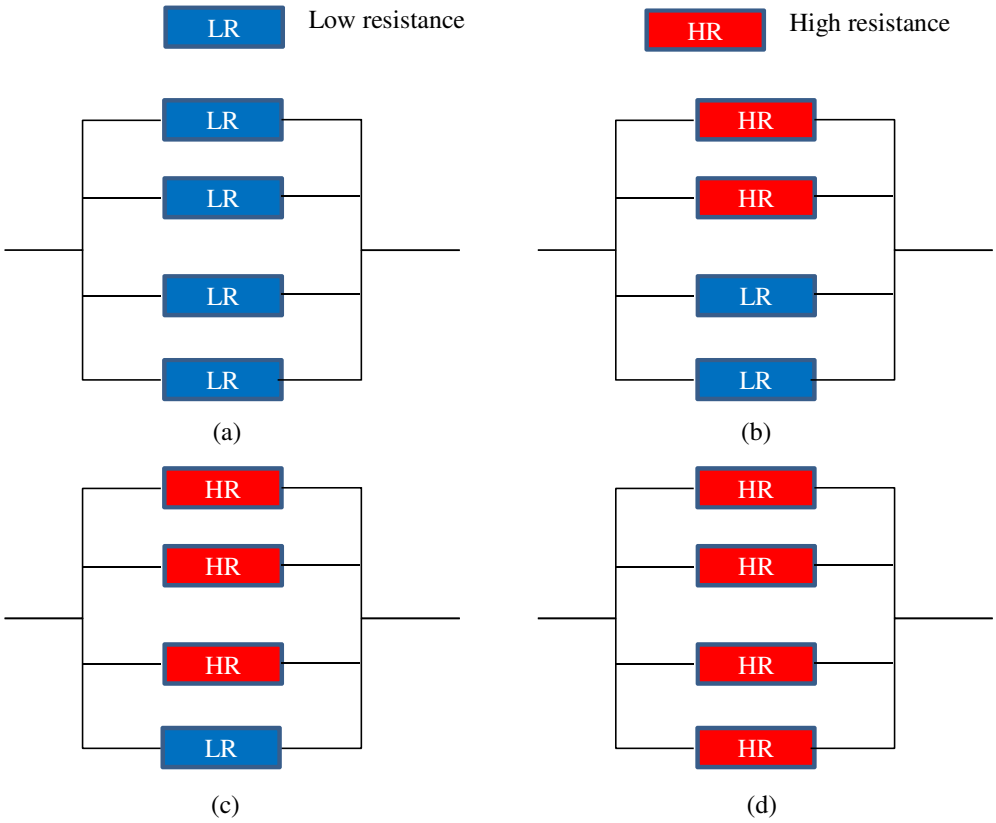

Figure 5.14 Parallel circuit modeling for the lateral PCRAM devices with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure. (a) All 4 phase-change layers are in the crystalline state; (b) 2 phase-change layers are in the amorphous state while the other 2 are in crystalline state; (c) 3 phase-change layers are in the amorphous state while the other 1 is in crystalline state; (d) All 4 phase-change layers are in the amorphous state.

5.3.6 Discussion

The multi-level data storage by SLL structure presented above has three advantages. Firstly, the multiple levels will be stable during cycle endurance using discrete resistance levels. From both the testing and simulation results, it can be seen that the difference between the different resistance levels is large. Hence, this multi-level

design can achieve discrete resistance levels, which makes it more stable during multi-level writing and reading.

Secondly, edge-contact lateral PCRAM devices with SLL structure have low power consumption. The lateral PCRAM devices with N-doped Sb_7Te_3 and ZnS-SiO_2 SLL structure have an edge-contact structure for the phase-change materials and electrodes. As edge-contact structures can reduce power consumption effectively [166], this multi-level lateral PCRAM is expected to operate with low power consumption.

Thirdly, the resistance states or levels of lateral PCRAM can be manipulated with the periods of the SLL structure. With increasing the periods of N-doped Sb_7Te_3 and ZnS-SiO_2 in the SLL structure, more phase change bridges will be involved in the data storage [167]. Hence, more intermediate resistance levels can be achieved for lateral PCRAM devices with more periods in the SLL structure.

5.4 Summary

In this chapter, multi-level lateral PCRAM devices were investigated based on GeTe/ Sb_7Te_3 SLL structure. Multi-level storage can be realized via different writing schemes. However, the resistances of the intermediate states are not discrete and the intermediate states are not stable during overwriting. Hence, a lateral PCRAM device with SLL structure incorporating N-doped Sb_7Te_3 and ZnS-SiO_2 was proposed and demonstrated. Both current sweep and pulse mode dynamic resistance tests show that discrete multiple states can be achieved in the device, which can be used for multi-level data storage. Simulations reveal the operating mechanism of multi-level storage. More

intermediate states can be realized by increasing the periods of N-doped Sb_7Te_3 and ZnS-SiO_2, which enables a promising solution to increase the data storage capacity for lateral PCRAM devices significantly.

Chapter 6 Conclusions and future work

6.1 Conclusions

PCRAM is considered as one of the best candidates for next-generation non-volatile memories due to its superior memory qualities [49]. Lateral PCRAM is one of the best PCRAM structures due to its advantages of simple fabrication process, easy integration with CMOS and low RESET current as compared to the vertical PCRAM [103-108]. This thesis aims to find solutions to achieve high performance lateral PCRAM devices and a main focus is to improve the cycle endurance.

This thesis firstly conducted the failure analysis of lateral PCRAM devices in Chapter 2 and tried to find the factors affecting the endurance. Both vertical and lateral PCRAM devices with the same phase-change material $Ge_2Sb_2Te_5$ were tested and compared. Lateral PCRAM devices were found to fail faster in "stuck SET" mode. Both experimental measurement and thermo-mechanical simulation have been done to check the difference in vertical and lateral PCRAM devices. Lateral PCRAM devices have larger plastic deformation during overwriting than confined PCRAM devices. This is because that phase change layer is covered by soft $ZnS\text{-}SiO_2$ dielectric material for lateral PCRAM devices instead of hard metal TiW material for confined PCRAM devices. Plastic deformation involves of atomic bond breakage, which will accelerate the failure of lateral PCRAM devices. This finding is significant in the design of lateral PCRAM device structure to extend cycle endurance. To extend the cycle endurance of lateral PCRAM devices, the plastic deformation must be decreased, which can be implemented by enhancing the mechanical properties of lateral PCRAM devices, such as increasing

Young's modulus of phase change materials or covering dielectric materials, adding hard metal layer over the covering dielectric layer and so on.

To improve the cycle endurance of lateral PCRAM devices, the method of increasing the Young's modulus of phase change materials is adopted in Chapter 3. SLL structure phase change material is proposed for lateral PCRAM devices to enhance mechanical property and reduce plastic deformation. GeTe and Sb_7Te_3 are selected to form the SLL structure. The material properties of bulk GeTe film, bulk Sb_7Te_3 film and GeTe/Sb_7Te_3 SLL structure have been investigated. It is found that both the resistivity and crystallization temperature of bulk GeTe and Sb_7Te_3 films are thickness dependent. Thinner film corresponds with larger resistivity and higher crystallization temperature. The thickness to reach phase change limitation is around 3 nm for both bulk GeTe and Sb_7Te_3 films. Through adjusting the thickness ratio of GeTe to Sb_7Te_3, the resistivity, crystallization and melting temperature of GeTe/Sb_7Te_3 SLL structure can be manipulated. This is a significant finding for another material engineering method to achieve ideal phase change material besides doping method. With increasing the thickness ratio of GeTe to Sb_7Te_3, the resistivity and crystallization temperature of GeTe/Sb_7Te_3 SLL structure increase, while melting temperature is the lowest at thickness ratio 1.6 due to the possible compound formation. Lateral PCRAM devices with GeTe/Sb_7Te_3 SLL structure were fabricated and tested. The performance of lateral PCRAM devices also relies on the thickness ratio of GeTe/Sb_7Te_3 SLL structure. When the thickness ratio is 1.6, the cycle endurance is the longest and the RESET current is lowest among all the lateral PCRAM devices. The cycle endurance can be higher than 5×10^6 cycles, which implies that the cycle endurance is improved with SLL structure

application in lateral PCRAM devices. The RESET current is as low as 1.5 mA, which is much lower compared to similar size scale lateral PCRAM devices. This implies that GeTe/Sb_7Te_3 SLL structure reduce the power consumption of lateral PCRAM devices with its good thermal confinement. The SET process can be as short as 30 ns, which may be due to the fast crystal growth speed of Sb_7Te_3. The crystallization process of GeTe/Sb_7Te_3 SLL structure is growth-dominant by checking the transient effect during SET process. Overall, the lateral PCRAM devices can achieve high performance of high cycle endurance, low RESET current and fast switching speed with the application of growth-dominant GeTe/Sb_7Te_3 SLL structure.

After finding a suitable phase change material for lateral PCRAM devices, this thesis also tried to improve the structure of lateral PCRAM devices in Chapter 4. An edge-contact structure was proposed to apply in lateral PCRAM devices to reduce the power consumption. Better thermal confinement can be achieved for edge-contact lateral PCRAM device with smaller contact area between phase-change materials to electrodes based on thermal simulation. The edge-contact lateral PCRAM devices with GeTe/Sb_7Te_3 SLL structure ware fabricated and tested. Using the edge-contact structure, the RESET current is reduced from 1.5 mA (normal structure) to 1.2 mA and the resistance ratio between the RESET and SET states is increased from 20 times (Normal structure) to above 100 times. Good stability and resistance ratio after 10^5 overwriting cycles were achieved. The RESET speed and SET speed can be as short as 10 and 30 ns, respectively. Hence, a lateral PCRAM device with high speed, even lower RESET current and high endurance is achieved.

To increase the capacity of memory, multi-level cells were investigated for lateral PCRAM devices in Chapter 5. For lateral PCRAM with GeTe/Sb_7Te_3 SLL structure, multiple states can be achieved by employing different programming pulses to change the volume of the active region. However, the multiple states achieved in these lateral PCRAM devices are not stable as heat accumulation during overwriting may affect the programming volume. Hence, a new SLL structure incorporating a phase-change material and a dielectric material was proposed to achieve discrete and stable multi-level storage for the edge-contact lateral PCRAM devices. Multiple discrete-like intermediate states were achieved in lateral PCRAM devices with this new SLL structure incorporating N-doped Sb_7Te_3 and ZnS-SiO_2. The different levels are related to the different numbers of activated phase-change layers in the amorphous and crystalline states through simulation studies.

In conclusion, the failure analysis of lateral PCRAM devices has been conducted. Plastic deformation is the possible cause for failure of lateral PCRAM devices. The “soft” structure in lateral PCRAM devices cause the large plastic deformation. This finding is significant in the design of lateral PCRAM device structures to achieve higher endurance. Based on this finding, the lateral PCRAM device with GeTe/Sb_7Te_3 SLL structure was proposed with high performance of high speed, low RESET current, high endurance and multi-level effects. Moreover, the RESET current can be even lower with edge-contact structure application and multi-states can be more stable with new SLL structure incorporating N-doped Sb_7Te_3w and ZnS-SiO_2. These high performances can make lateral PCRAM as a competent candidate for high density PCRAM chip and product.

6.2 Future work

This dissertation covers several research topics in lateral PCRAM devices, such as failure analysis, phase-change material engineering, structural engineering and multi-level programming. These results provide a reference for the development of high performance lateral PCRAM devices. This thesis also presents some initial results and more detailed investigation and characterization will be required for evaluation of novel material and structure for lateral PCRAM devices. Possible future works are highlighted in the following.

In this thesis, all the lateral PCRAM devices are fabricated based on the 1μm lithography technology node (Canon stepper). Hence, the lateral PCRAM device size is around 1μm. As the performance (especially the RESET current) is highly dependent on the device size, scaling of lateral PCRAM devices can further enhance the performance of lateral PCRAM devices. In the future, nanoscale lateral PCRAM devices can be fabricated and investigated with the help of advanced lithography technologies, such as e-beam and NSOM. Nanoscale lateral PCRAM devices can further reduce the RESET current and increase the switching speed.

GeTe/Sb_7Te_3 SLL structure was proposed for lateral PCRAM. In the future, other combinations can be made based on other phase-change materials, such as GeTe/GeSb, GeTe/AgInSbTe, GeSb/Sb_7Te_3, AgInSbTe/Sb_7Te_3, and GeSb/AgInSbTe. Effects of different thickness ratios can be further investigated.

Edge-contact lateral PCRAM devices were successfully demonstrated. A thin dielectric layer is inserted between the metal electrode and phase-change layer to reduce programming power. This work only investigates the effect of TiW electrode, and ZnS-SiO_2 dielectric layers with a fixed layer thickness. More optimization work can be

performed. In addition, dielectric films with lower thermal conductivities can be employed.

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14. D. Loke, W. J. Wang, L. Shi, R. Zhao, **H. X. Yang**, K. G. Lim, L. T. Ng, H. K. Lee, Y. C. Yeo, and T. C. Chong. "Perspectives of nanostructured phase change materials for high speed non-volatile memory", *Materials Research Society Spring Meeting*, April 5 - 9 (2010)
15. D. Loke, W. J. Wang, L. Shi, R. Zhao, **H. X. Yang**, K. G. Lim, L. T. Ng, H. K. Lee, Y. C. Yeo, and T. C. Chong. "Ultrafast phase-change RAM and correlation between phase-change speed and cell size", *4th MRS-S Conference on Advanced Materials*, March 17 - 19 (2010)

Invited talks

Yang Hongxin, Shi Luping, Lee Hock Koon, Zhao Rong, Li Jianming, Lim Kian Guan, Ng Lung Tat and Chong Tow Chong. "Growth-dominant SuperLattice-like Phase Change Medium and its application in lateral phase change random access memory", *International Symposium on Integrated Functionalities* (ISIF) 2010, San Juan, Puerto Rico (USA)June 16, 2010

Patents

SG Application No: 201103620-9. Singapore patent issued on May 27th, 2011.

Invention: Superlattice-like Dielectric as a Thermal Insulator in Lateral-type Phase-Change Random Access Memory

Inventors: Desmond Loke, **Hongxin Yang,** Rong Zhao and Weijie Wang.

US Patent Application No. 13/474,985

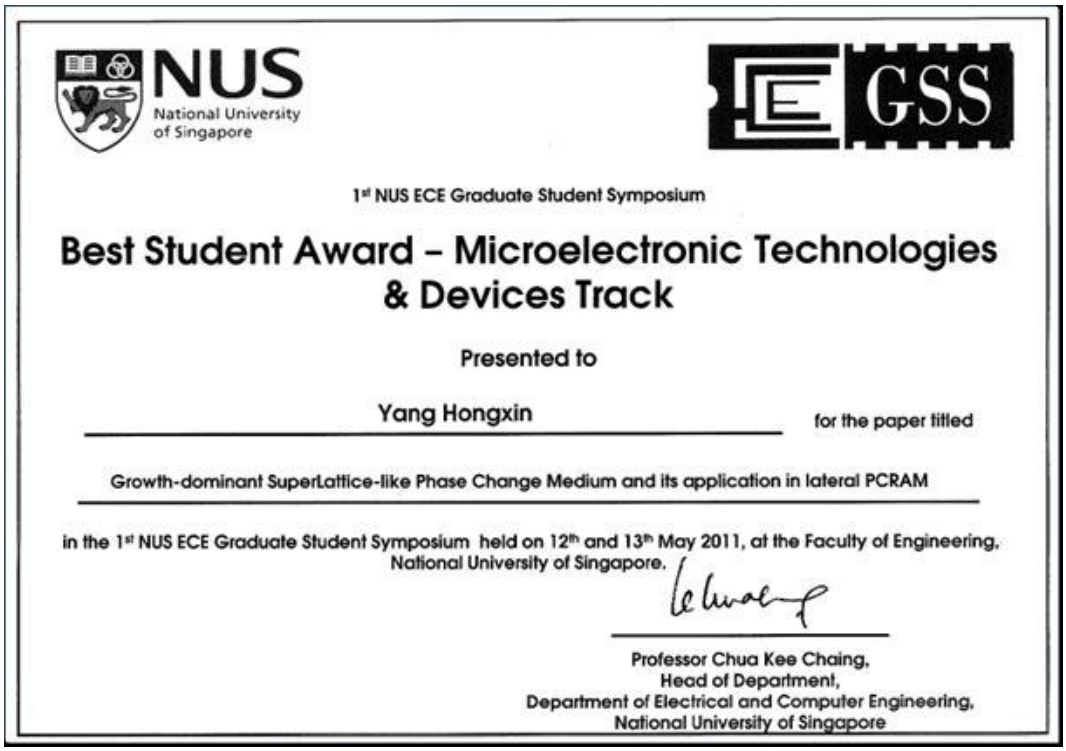
Invention: A Phase-Change Memory and A Method of Programming The Same

Inventors: Desmond Loke Kok Leong, **Yang Hongxin**, Zhao Rong, Wang Weijie

Applicant: Agency For Science, Technology And Research

Awards

Best student award- Microelectronic Technologies & Device track for 1st NUS ECE graduate student symposium (GSS) and IEEE Reliability/CPMT/ED Singapore Chapter Awards (2011)



NUS National University of Singapore

GSS

1st NUS ECE Graduate Student Symposium

Best Student Award – Microelectronic Technologies & Devices Track

Presented to

Yang Hongxin for the paper titled

Growth-dominant SuperLattice-like Phase Change Medium and its application in lateral PCRAM

in the 1st NUS ECE Graduate Student Symposium held on 12th and 13th May 2011, at the Faculty of Engineering, National University of Singapore.

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