INVESTIGATIONS INTO REAL TIME CONTROL AND INTERCONNECTION OF MICROGRID TO ELECTRIC POWER SYSTEM

Xiaoxiao Yu

NATIONAL UNIVERSITY OF SINGAPORE

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Xiaoxiao Yu

(*B. Eng(Hons.), Huazhong Univ. of Sci. & Tech., China*)

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Contents

Summary

Soaring power demand and enormous carbon emission from conventional power generators create a need for clean technology to facilitate the integration of renewable resources. Therefore, new electrical power distribution system that allows for easy integration of more renewable sources into grid is required. Microgrid is such new paradigm distribution power system. Microgrid is a cluster of energy sources (AC or DC), storage systems and loads that present itself as a single entity to the electrical power system. Contrary to traditional power system, microgrid enables bidirectional power flow with electric power system (EPS), and can operate in islanding mode.

The research aims to investigate and solve some of the major real time control problems associated with interconnection of microgrid under various EPS conditions, such as normal, balanced and unbalanced fault. The thesis first proposes a modular and reconfigurable multifunctional power converter building block (PCBB) to facilitate the connection of hybrid (DC+AC Bus) microgrid to Area EPS. Through combined active power and reactive power control, the PCBB can facilitate both the connection between DC and AC bus within microgrid and the connection of hybrid microgrid to Area EPS simultaneously. It achieves power (P) and power quality (P,Q) control of the system. Real time digital simulation results demonstrate that with proposed controller for PCBB, the microgrid can function

properly both in Area EPS-connected mode and stand-alone mode; moreover, it can smoothly transit between the two modes.

For high power microgrid, transitioning to islanding mode under low voltage fault might lead to considerable generation loss and unstable operation of local EPS. This thesis proposes digital controlled power converter building block (PCBB) to enable the distributed generators inside microgrid to ride through EPS low voltage fault. The simulation and experimental results show that when EPS experiences fault and microgrid is feeding power toward it, the proposed control system will limit the output current of PCBB to avoid tripping off and thermal breakdown. The PCBB is able to maintain smooth power injection when EPS has asymmetrical fault and negative sequence voltage component. Once the fault is cleared, PCBB returns to normal operation to continue feeding the same power as prefault to avoid network instability.

As the power level of microgrid increases, the power conversion system capacity needs to be expanded. Multiple interfacing inverters could be paralleled to feed the local load with power from distributed generators and energy storage. With redundant inverter modules, the system reliability improves. The thesis derives mathematical models to calculate the reliability indices and cost of parallel redundant inverter systems. A novel methodology to design the structure of parallel redundant inverter system to achieve tradeoff between system reliability and cost is proposed. A dynamic power distribution control scheme is proposed for parallel inverters to achieve improved efficiency and thermal profile. At last, the thesis proposes a hybrid control architecture to achieve real time wireless control of inverter interfaced distributed generators in microgrid. The stability analysis

shows the schemes proposed are stable for n paralleled interfacing inverters in low voltage microgrid. Both simulation and real time test results validate the proposed control strategies.

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Chapter 1

Research Background and Problem Definition

1.1 Introduction

This chapter starts with the emerging issues with current power system infrastructure and presents the necessity to improve the conventional control and energy management of distribution power system. Subsequently, the nonconventional distribution power system paradigm, microgrid, is introduced. The distinctive features and challenges of microgrid as compared to conventional power distribution system are discussed. Afterwards, the motivation and contribution of the work are emphasized. Finally, the broad outline of the thesis is given.

1.2 Emerging Issues with Current Power System Infrastructure

The power demand has been soaring with the development of the economy in recent few decades. Fig. 1.1 shows the electricity consumption growth of the whole world in recent 20 years and estimation in the future [1]. As shown in Fig. 1.1, the world electricity consumption will increase more than 40% in next 25 years. The electric power generation system is being expanded to accommodate the increasing power demand. Fig. 1.2 shows the world power generation growth trend [1]. To meet the growing energy requirement, we would still have to rely on fossil fuels, though the contribution of renewable sources will increase. According to the estimation made by Energy Information Administration, the total carbon emission by 2030 is projected to be around 40 billion metric tons [1]. Therefore, it is of great importance to develop clean technologies to facilitate the integration of renewable sources.

Renewable sources have potential to address the problems of rapid increase in power consumption, diminishing of fossil fuels and intensive emission of green house gases introduced by traditional generators. However, their intermittent nature causes various problems. Fig. 1.3 shows a typical solar radiation curve for Singapore [2]. Fig. 1.4 shows the wind speed and energy distribution of a US wind farm [3]. It is clear that the energy availability fluctuates and will peak at times that may not necessarily coincide with the demand peak in Fig. 1.5. Energy stor-

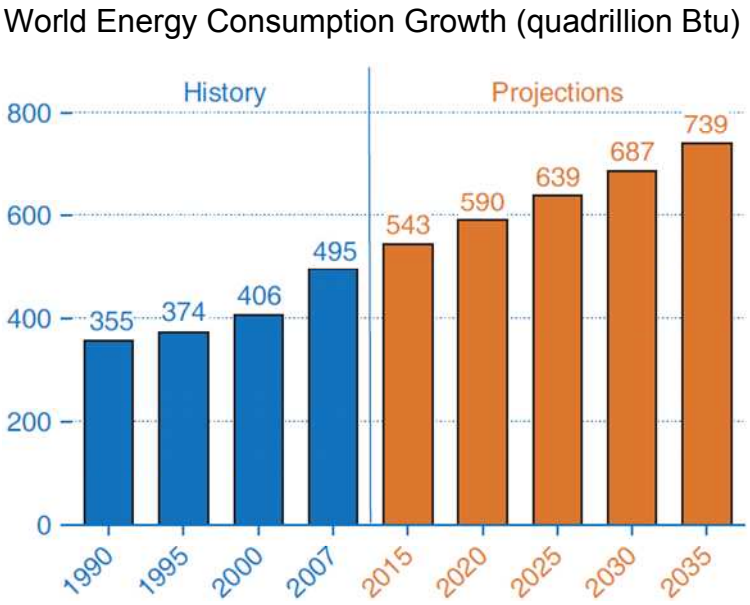


Figure 1.1: World Power Generation Growing Trend (Source:[1])

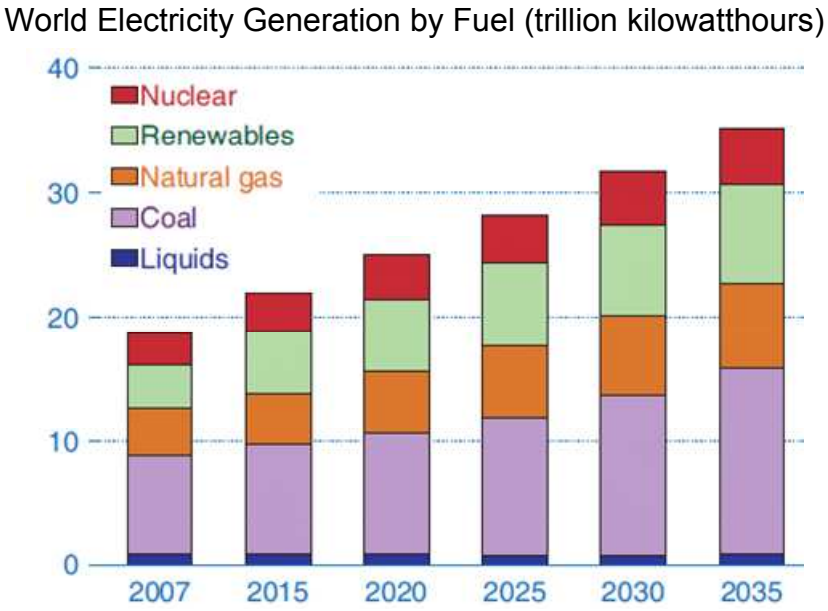


Figure 1.2: Growth in World Electrical Power Generation (Source:[1])

age and demand response are two solutions to this problem caused by intermittent nature of renewable energy sources.

Since energy storage is a very expensive solution for high power applications, demand response is fast becoming a viable load management tool to achieve gen-

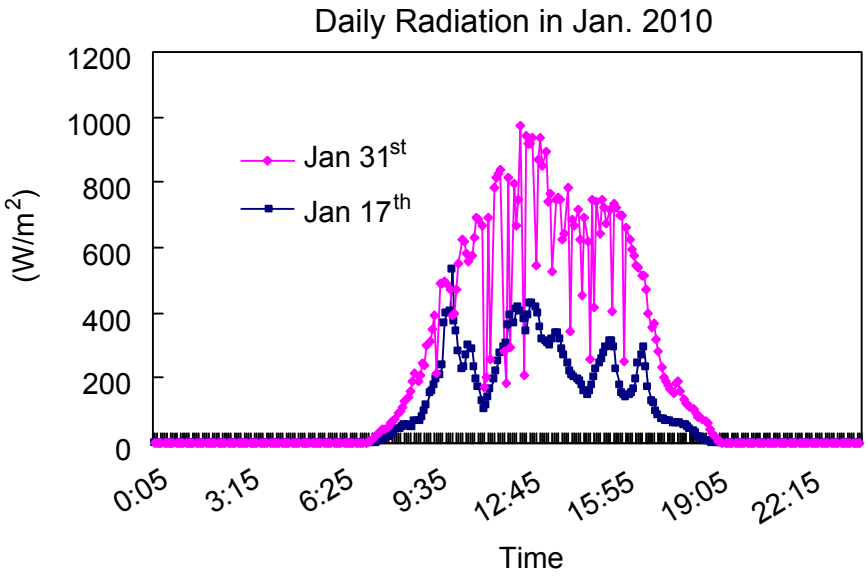


Figure 1.3: Daily Solar Radiation of Singapore in January 2010 (Source:[2])

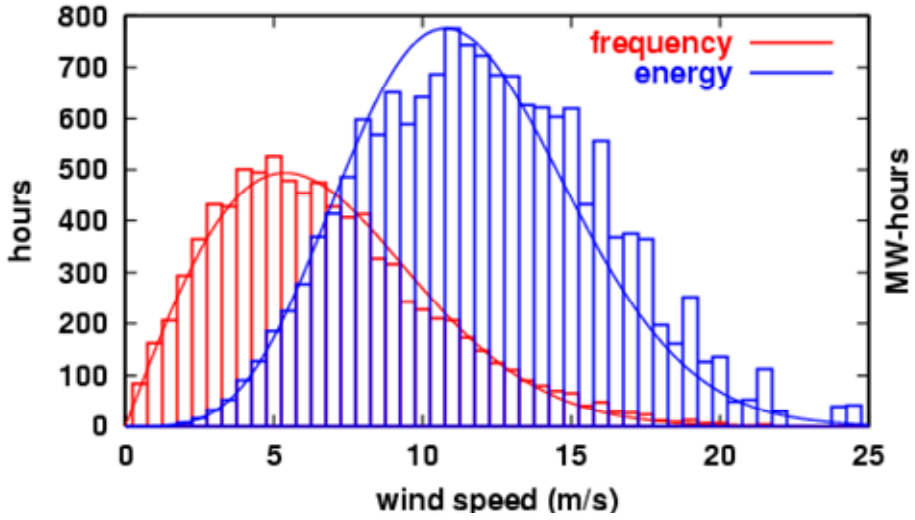


Figure 1.4: Wind Speed and Energy Distribution of 2002 at the Lee Ranch Facility in Colorado (Source:[3])

eration and demand balance [11]. Demand response allows the utility to control selected high-load devices in a rolling type of operation during high-demand periods. Therefore, the difference between generation and demand during peak hours is reduced and the energy storage system required can be sized down.

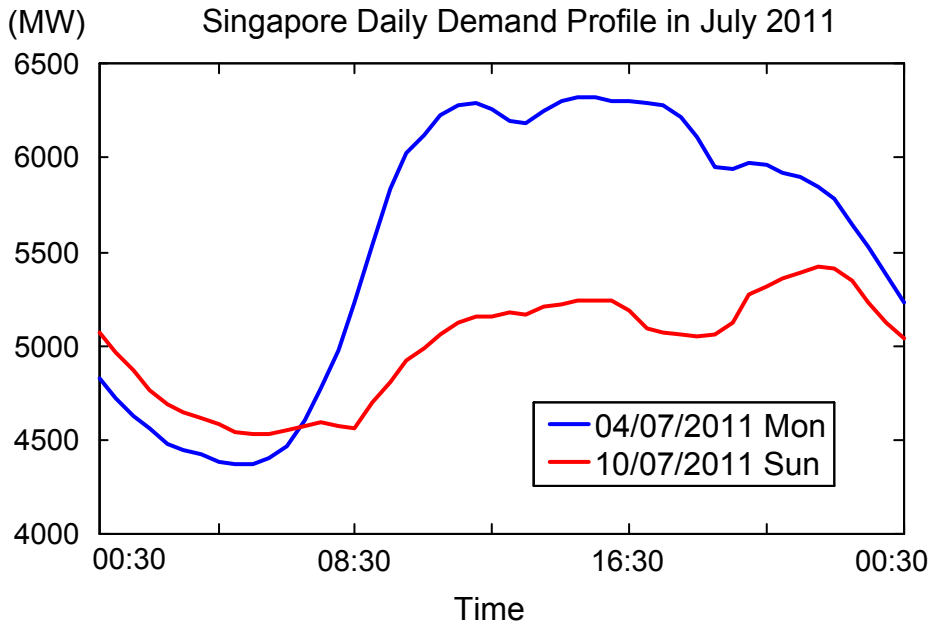


Figure 1.5: Daily Load Profile in Singapore (Source:[4])

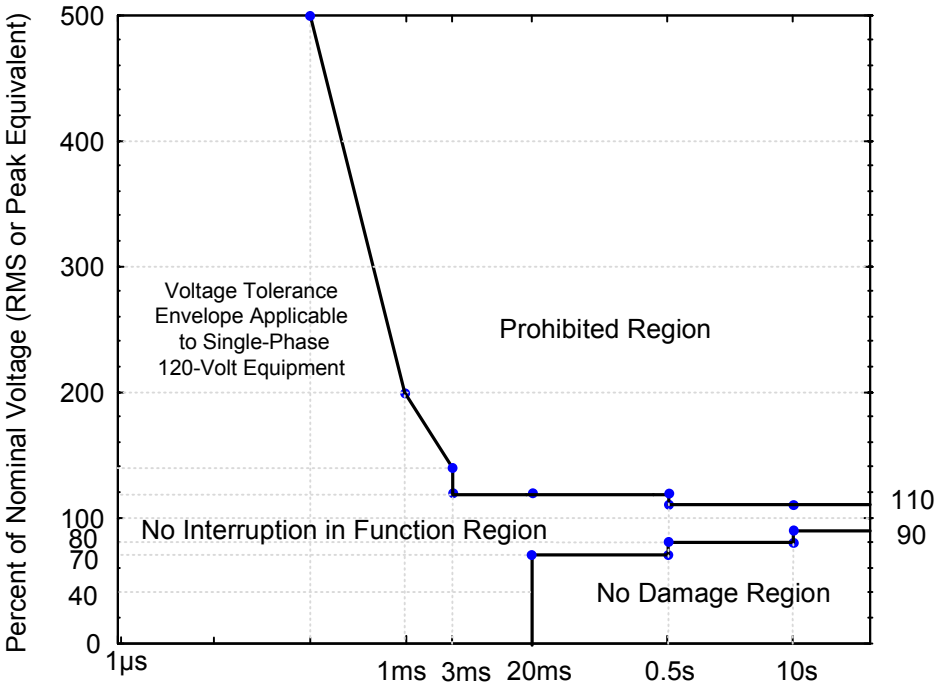


Figure 1.6: The ITI Curve (Source:[5])

Besides soaring demand of electricity, another emerging issue faced by current power system is the demand to improve system reliability and power quality. Most power quality issues relate to electronic equipment. The Information Technology

Table 1.1: Typical Number of Facility Voltage Incidents per Year

Voltage Deviation	$< 0.02s$	up to $3s$
$110 - 120\%$	> 700	$0 - 6$
$106 - 110\%$	> 700	$0 - 200$
$87 - 106\%$	Normal	Normal
$70 - 87\%$	> 240	$20 - 140$
$25 - 87\%$	> 240	$0 - 16$

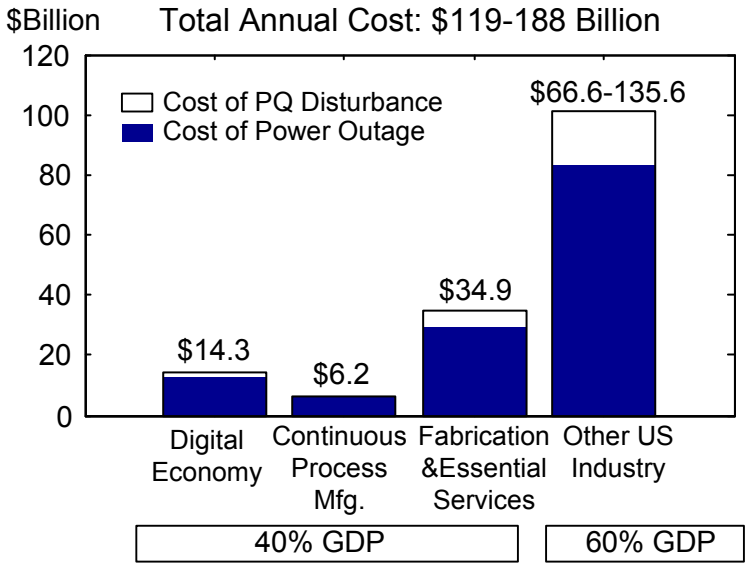


Figure 1.7: Cost of Power disturbances and Power Outage in Industrial and Digital Economy Companies in US (Source:[6])

Industry Council published a curve that describes the ac input voltage envelope that electronic equipment can tolerate [5]. The curve is shown in Fig. 1.6. Table 1.1 shows the voltage incidents statistics collected from power quality survey reports of Electric Power Research Institute, Canadian Electric Associations and National Power Laboratory [12]-[14]. The voltage sag events of long time duration will lead to malfunction of electronic equipment. Fig. 1.7 shows the considerable cost of power disturbances and power outages to industrial and digital economy companies [6]. Fig. 1.8 shows the power interruptions cost $79 billion annually to U.S. electricity consumers [7]. Fig. 1.9 shows the cost of various power quality

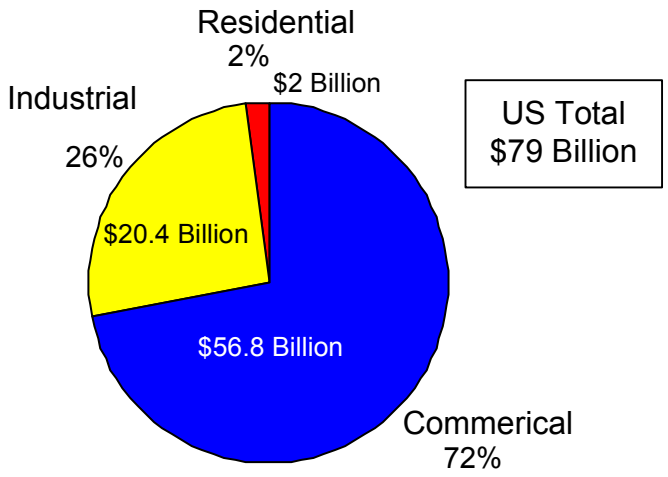


Figure 1.8: Cost of Power Interruptions by Customer Class Estimated by EPRI (Source:[7])

phenomena in Europe and total amount exceeds €150 Billion per year [8]. Therefore, it is necessary to modernize current power system to improve both the power capacity and the power quality.

Another issue with existing centralized power system is vulnerability to terrorist attack. The centralized power stations might become potential attack targets of terrorists. The growing concern over terrorist attack in some countries calls for a more robust energy grid, which is less dependent on centralized power stations [15]. In addition, expansion of the centralized radial network is expensive and complex.

In 2004, Microgrid was proposed by Prof. Lasseter as a new paradigm distribution power system to facilitate the interconnection of renewable energy sources and improve power system reliability and power quality [16].

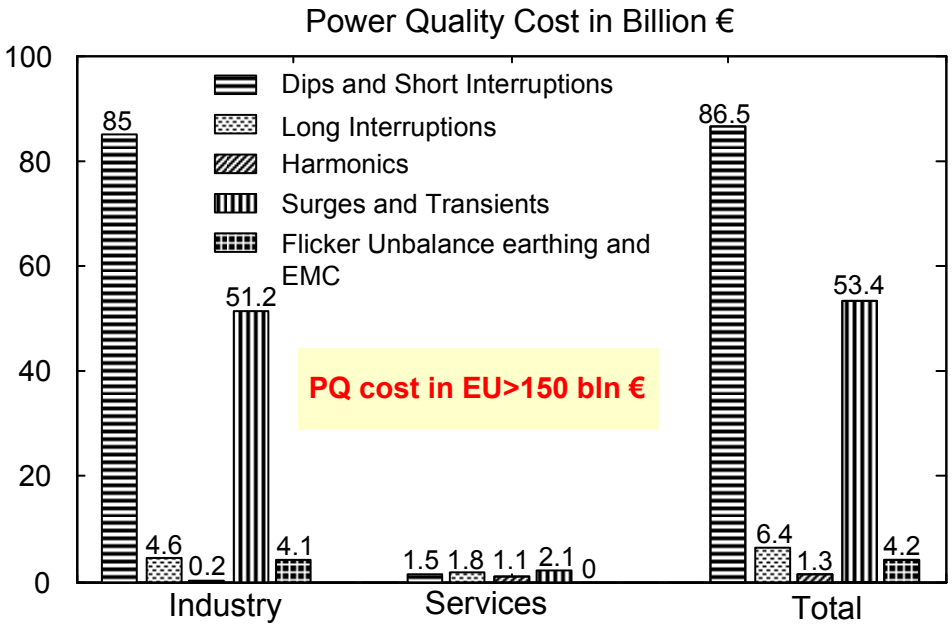


Figure 1.9: Extrapolation of PQ Cost to EU Economy in LPQI Surveyed Sectors (Source:[8])

1.3 Microgrid Concept and Challenges

Microgrid has been defined as a cluster of microsources, storage systems and loads which presents itself to the grid as a single entity that can respond to central control signals [16].

Fig. 1.10 shows the general architecture of microgrid. A microgrid consists of microsources that could be conventional or renewable. Microturbines, diesel generators, etc could fall under conventional sources. PV, solar thermal, wind, fuel cells, etc are some examples of nonconventional energy sources. A microgrid could also have combined heat and power (CHP) capability to meet the heating/cooling needs of the community. Microgrid central controller (MGCC) manages the energy for the microgrid. Each source will have a microsource controller (MSC) that

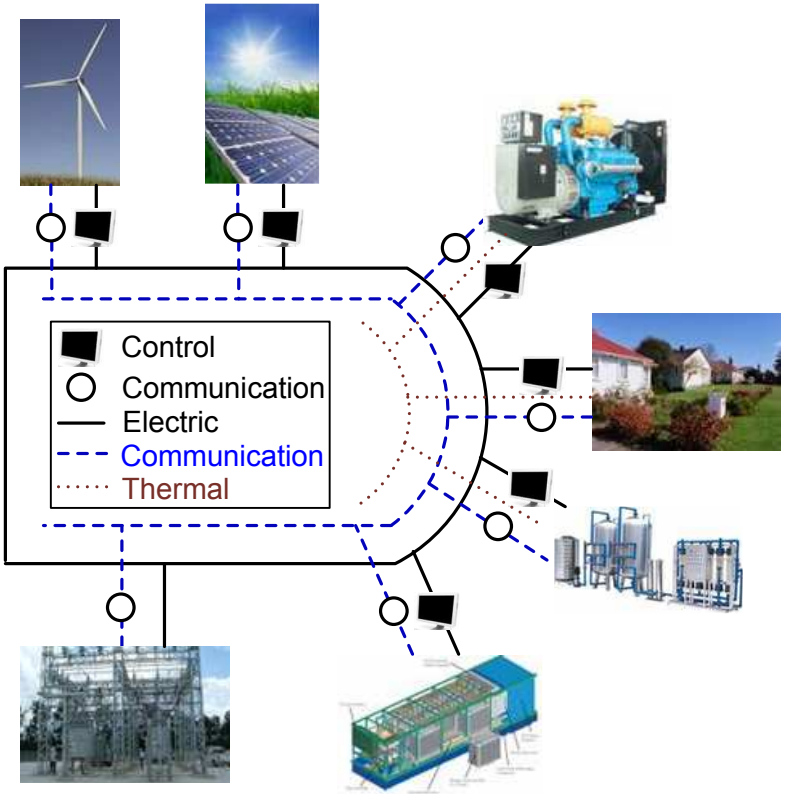


Figure 1.10: General Architecture of Microgrid

controls the output. Storage systems can be added to the MG to balance the demand and supply.

As a new paradigm for distribution power system, the power rating of microgrid ranges from few hundreds kW to few MW [17]. It provides a way to connect renewables to the grid and can be designed to meet specific user demands. In addition, it provides a low cost solution to power system expansion. For traditional power system, renovation of power generation, transmission and distribution networks is required to meet the increasing power demand. Compared with the costly expansion scheme for conventional power system, microgrid allows expansion only at distribution level to enhance system capacity.

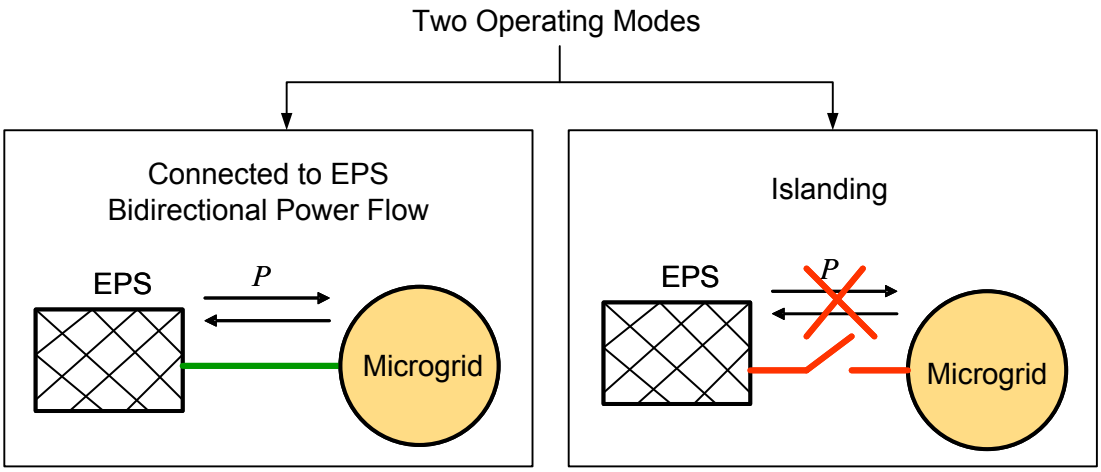


Figure 1.11: Two Operating Scenarios of Microgrid

Another important characteristic of microgrid different from conventional distribution power system, is the bidirectional power flow capability. Microgrid could buy and sell power to EPS based on the reserve and EPS demand. Furthermore, microgrid is able to function as an autonomous power island as shown in Fig. 1.11. When electric power system meets severe disturbance and fault, microgrid is able to disconnect from EPS and sustain the local load with distributed generation and storage. The islanding operation functionality helps improve power system reliability. Smooth transition of microgrid between EPS connected operation mode and islanding mode is important to sustain the normal operation of critical load.

Unlike synchronous generators, the distributed generators in microgrid mainly produces DC or variable frequency AC voltage. Hence we need power conversion technologies to interconnect the sources with the load and the EPS. Power Electronics play a major role in facilitating this connection. Fig. 1.13 shows various types power converters required to facilitate the interconnection of microgrid to EPS.

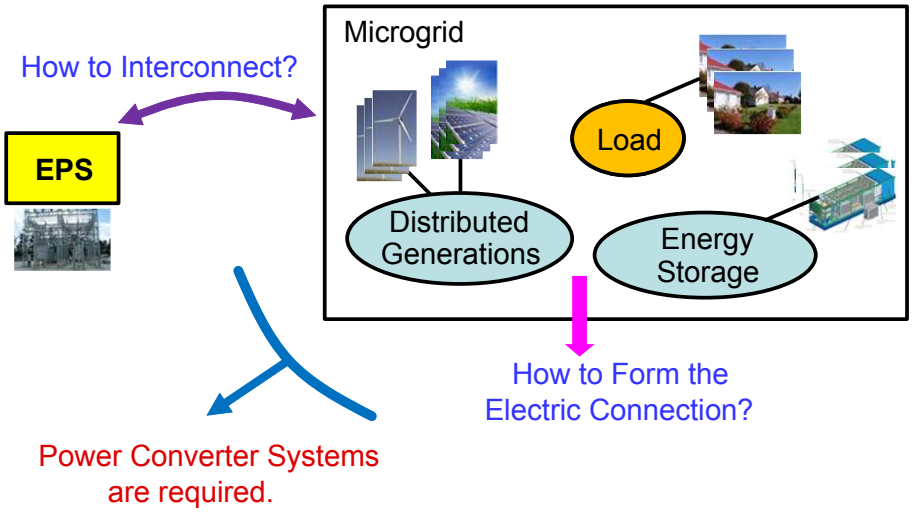


Figure 1.12: Power Converters are Required to Tackle Microgrid Challenges

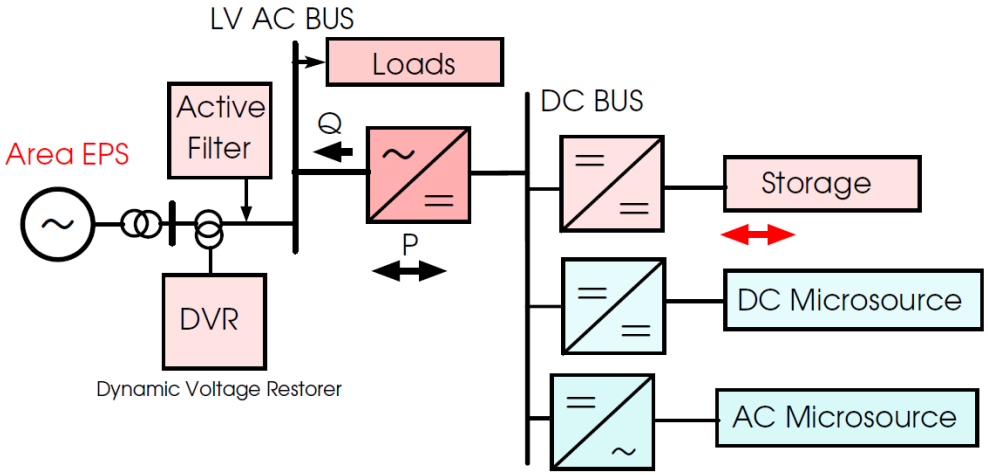


Figure 1.13: The Different Types of Power Converters Required to Facilitate the Interconnection of Microgrid (Source:[9])

The power electronics interface of distributed generators and energy storage system requires modification of not only control structure, but also protection scheme. According to manufacturers' standards, the traditional synchronous generators could withstand up to around 10 times nominal current during short circuit fault. However, the power converters only allow a maximum of twice nominal current owing to the small transductance of silicon transistors. The limited short

circuit current capability brings contraints to microgrid protection. It is important to design the microgrid interface with protection scheme to minimize the contribution of microgrid to fault current sensed in the transmission grid.

Besides control and protection, reliability is another concern about power electronics interface. Compared with other components of microgrid, the reliability of power converter is much lower. Take the PV generator discussed in [18] as an example, the service life time of PV module has been increased to 552 years, i.e. for a batch of 552 PV modules, there will be one failure [19]. However, the service life time of inverter system is usually limited within 1-10 years [19], [20]. Therefore, to improve the overall system reliability, improving the power conversion system reliability is the key.

1.4 Research Objectives

The overall purpose of the research is to investigate and solve some of the major real time control problems associated with interconnection of microgrid under various EPS conditions, such as normal, balanced and unbalanced fault.

The main objectives of the research work are as follows:

- To develop a power electronic building block architecture with interconnectivity and reconfigurability to facilitate the interconnection of microgrid
- To investigate and propose power regulation schemes for reconfigurable con-

verters to perform various power processing functions

- To enhance reliability and upgrade power level of power processing system for high power microgrid

1.5 International Standards on Interconnection of Distributed Generators and Microgrid

The thesis aims to solve problems related to interconnection of microgrid with electric power system. Traditionally, electric power systems were not intended to accommodate active generation at the distribution level [17]. In order not to disturb the proper operation of the electric power system, many grid operators and international research agencies have published standards and regulations. The standards and grid codes could guide the control system design and hardware implementation of grid connected distributed generators and microgrid.

These standards have been developed by some international organizations such as the IEEE and IEC (International Electrotechnical Commission) as well as institutions and utilities local to individual countries such as the National Fire Protection Association, Inc, Underwriter Laboratories, Inc. (UL) in the U.S. and the European Committee for Electrotechnical Standardization (CENELEC).

The most influential standard is the **IEEE1547** series standard developed by IEEE Standards Coordinating Committee 21 (SCC21). The standard establishes

the criteria and requirements pertaining to interconnection of distributed resources with EPS [21]. The guide applies to all distributed resource systems of aggregate capacity below 10MVA. The standard specifies the constraints for power quality, grid synchronization, islanding detection, and response to EPS abnormal conditions. The limitation of major performance matrices are listed in Table 1.2, 1.3, 1.4, 1.5.

Table 1.2: IEEE 1547 Standard Synchronization Parameter Limit

Aggragate Rating of DR (kVA)	Frequency Difference (Hz)	Voltage Difference (%)	Phase Angle Difference (^{o})
$0 \sim 500$	0.3	10	20
>500-1,500	0.2	5	15
>1500-10,000	0.1	3	10

Table 1.3: IEEE 1547 Standard Voltage Variation Level and Clearing Time

Voltage Rating (% of base voltage)	Clearing time (s)
$V < 50$	0.16
$50 \leq V < 88$	2.00
$110 < V < 120$	1.00
$V \geq 120$	0.16

Table 1.4: IEEE 1547 Standard Frequency Variation Level and Clearing Time

DR size	Frequency range (Hz)	Clearing time (s)
$\leq 30kW$	> 60.5	0.16
	< 59.3	0.16
$\geq 30kW$	> 60.5	0.16
	$< \{59.8 - 57.0\}$	Adjustable 0.16 to 300
	< 57.0	0.16

Table 1.5: IEEE 1547 Standard on Current Quality

Individual harmonic order h (odd harmonics)	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h$	Total demand distortion (TDD)
Percent (%)	4.0	2.0	1.5	0.9	5.0

Even harmonics are limited to 25% of the odd harmonic limits shown

The **IEEE1547** Std requirement on power quality applies to system voltages from 120V to 69kV. Such requirement is drawn directly from the most restrictive

harmonic requirement **IEEE519** Std. Specifically, **IEEE1547** requirement on current harmonics only applies to the harmonic current at PCC because of the DR serving linear loads. The harmonic current contribution at PCC from nonlinear load is excluded.

As mentioned earlier, distributed generators have limited short circuit current capability. Previously, when EPS meets low voltage faults, the distributed generators are immediately tripped off and will be reconnected after fault is cleared. In recent years, the penetration level of distributed generation has been increasing, in particular, wind power generation is becoming an important electricity source in many countries. Tripping off distributed generators during fault might cause massive generation loss and lead to network instability. Therefore, distributed generators have been required to maintain active power delivery and reactive power support to the grid by many countries.

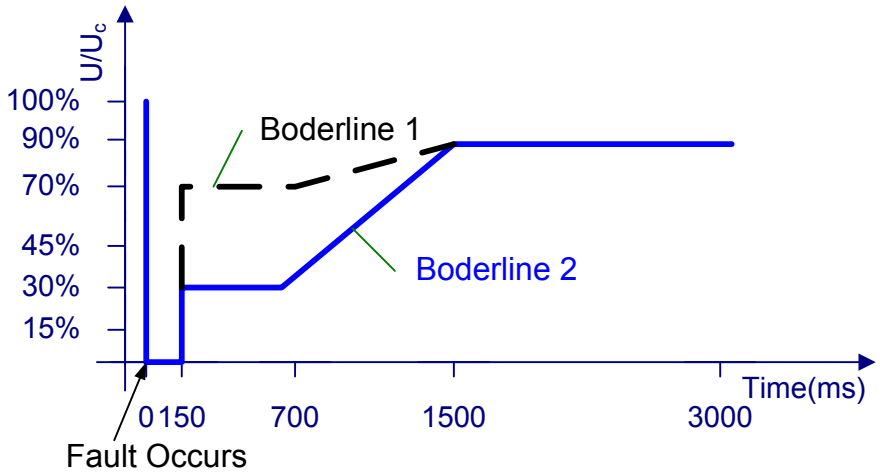


Figure 1.14: Grid Code Fault Ride-through Requirement of a Type-2 Generating Plant at the Network Connection Point

German grid operator E.ON Netz first published grid code on fault ride

through for wind generation system in 2004 [22]. Fig. 1.14 shows the specifications of the fault ride through requirement updated in 2009. Other countries such as US, UK, Canada, Ireland, Denmark, etc have also published grid codes on fault ride through with similar specifications [23]-[28]. [29] specifies the fault ride through requirement for type-2 generating plant (all other plants but the ones connected to the network through synchronous generators) the same as E.ON as shown in Fig. 1.14.

As shown in Fig. 1.14, the DG systems must maintain stable operation when voltage dips are above boderline 1, and must coordinate with the network operator when voltage dips are between borderline 1 and 2, while immediately trip off when voltage dips are below borderline 2.

Considering microgrid is connected to distribution power system level, the distribution grid code on fault ride through is followed in this thesis [30] to design the fault ride through scheme for microgrid. According to the fault ride through requirement of this standard, active power is maintained as porportional to the voltage level, and reactive power is maintained maximum within the converter constraint.

1.6 Thesis Contributions

The major contributions of the thesis are summarized as follows:

• A modular and reconfigurable multifunctional power converter building block is proposed to interconnect microgrid to electric power system.

Through combined active power and reactive power control, the PCBB can facilitate both the connection between DC and AC bus within microgrid and the connection of microgrid to Area EPS simultaneously. It achieves power (P) and power quality (P,Q) control of the system. The main functions of the PCBB include compensating the current harmonics produced by nonlinear load in the microgrid, mitigating the voltage sag or swell of the electrical power system (EPS) at the point of common coupling (PCC) and facilitating the islanding and re-closure of microgrid when a severe fault happens to the EPS. To enable the PCBB to work efficiently and effectively, an adaptive PLL is designed to achieve accurate synchronization with grid; a synchronous rotating frame (SRF) based $6n^{th}$ order high bandwidth controller is applied to control the current harmonics compensation; a cascaded PI controller is used to regulate the voltage sag/swell compensation. With proposed control strategies applied, the interconnection requirement of IEEE 1547 Std and power quality requirement of IEEE 519 Std can be both satisfied.

• A simplified and effective fault ride through scheme is proposed to enable microgrid to maintain active power injection under EPS low voltage fault.

This thesis proposes a simplified control strategy for PCBB to achieve fault ride through (FRT) of microgrid based on instantaneous P&Q theory. The control system incorporates a fault current limiting (FCL) algorithm as well. With

proposed control scheme, the PCBB is able to sustain the power flow between microgrid and EPS under both balanced and unbalanced fault conditions. Once the fault is cleared, the microgrid will inject the same power as prefault. The grid code on FRT as shown in Fig. 1.14 is satisfied. Compared with other FRT strategies, the proposed scheme does not require complex calculations and achieves both fault ride-through and fault current limitation. In addition, the instantaneous power control strategy achieves minimal power variation and power drop during fault.

• A dynamic power distribution scheme for paralleled power inverter modules to facilitate the efficient operation of islanded microgrid.

When microgrid is operated with heavy load, with the proposed instantaneous error current correction method and cascaded proportional resonant voltage controller, paralleled power inverter modules produce a high quality voltage supply to the load with equally distributed power. When microgrid is operated under light load, the proposed dynamic power distribution scheme optimizes the system efficiency by dropping partial power modules. Time sharing scheme is also included in the control scheme to improve the system thermal profile. Dynamic electro-thermal models are employed in the control system implementation.

• A hybrid control architecture is proposed to achieve wireless power sharing control of the paralleled interfacing inverters of DGs in a low voltage microgrid .

The inverters are divided into blocks according to their geographical location. To control the power sharing of inverter blocks located in wide range, a

modified droop-control method is applied. For paralleled inverter modules placed physically nearby, the proposed dynamic power distribution scheme is applied to increase the system operating efficiency and life span. Virtual resistor is employed to improve the power sharing accuracy of droop control. The proposed modified droop-control scheme does not require complex computations. It offers both good steady-state and dynamic performances, even when the paralleled inverters have large impedance mismatch.

- This thesis proposes a framework to determine the parallel redundant inverter system structure in terms of reliability and cost optimization.

This thesis derives mathematical models for reliability and cost evaluation of single and parallel redundant inverter systems. The reliability models of parallel redundant inverters under different architectures and control strategies are derived. With the reliability and cost models, a novel methodology to determine the system architecture to optimize system reliability and cost is proposed. Sensitivity of the proposed models is investigated. The methodology is applicable to all parallel converter systems, such as parallel AC/DC rectifiers, DC/DC converters, etc.

1.7 Organization of the Thesis

This thesis is organized into seven chapters:

Chapter 1 introduces some of the basic concepts related to smart grid and

microgrid. Control and Operation of Microgrid, power electronics techniques applied to interconnect microgrid and microgrid protection are discussed in this chapter. It also outlines the research objectives and the scope of the thesis.

In **chapter 2**, design and control of a modular, multifunctional power converter building block to interconnect microgrid to electric power system is presented.

Chapter 3 proposes a simplified fault ride through scheme for high power microgrid. All the fault ride through schemes are compared from power variation, current quality, hardware constraints and control complexity aspects. The advantages and limitations of the proposed scheme is explored in details. Both simulation and experimental results are provided to validate the control scheme.

Chapter 4 presents research conducted on controlling parallel connected interfacing inverters of Microgrid. A novel dynamic power distribution scheme is proposed to achieve circulating current mitigation, improved light load efficiency and reliability of the parallel inverter system. Stability of the proposed dynamic power distribution scheme applied to n parallel inverters is proved. Experimental results of two parallel inverter system are provided.

In **chapter 5**, reliability, efficiency and cost models of microgrid interfacing inverter are derived based on the data collected from military handbook on reliability [31], manufacture datasheet and technical reports of international consulting companies. The models are extended to multiple parallel inverters as well.

With the cost-reliability models, a novel way to determine the system architecture to optimize system reliability and cost is proposed. The advantages of dynamic power distribution scheme in improving system reliability and reducing cost are quantitatively evaluated.

Chapter 6 investigates the decentralized real time control of microgrid. A hybrid control architecture is proposed to achieve real time wireless control of inverter interfaced distributed generators within microgrid. The stability of the proposed hybrid control architecture applied to n paralleled inverters in low voltage microgrid is proved. Both simulation and real time test results validate the proposed control strategies.

Chapter 7 summarizes the research work described in the thesis and explains some future work.

Chapter 2

Multifunctional Power Converter Building Block to Facilitate the Connection of Microgrid to Electric Power System

2.1 Introduction

This chapter proposes a multifunctional power converter building block (PCBB) to facilitate the connection of microgrid to electric power system. With combined active power and reactive power control (P+Q) scheme proposed, the PCBB can facilitate both the connection between DC and AC bus within microgrid, and the connection of microgrid to Area EPS simultaneously. It achieves both power (P) and power quality (P, Q) control of the system. Both offline and real time digital simulation results are provided to demonstrate that with proposed PCBB and control scheme, the microgrid can function properly both in Area EPS-connected mode and stand-alone mode; moreover, it can smoothly transit between the two operating scenarios.

2.2 Issues Concerning Interconnection between Microgrid and EPS

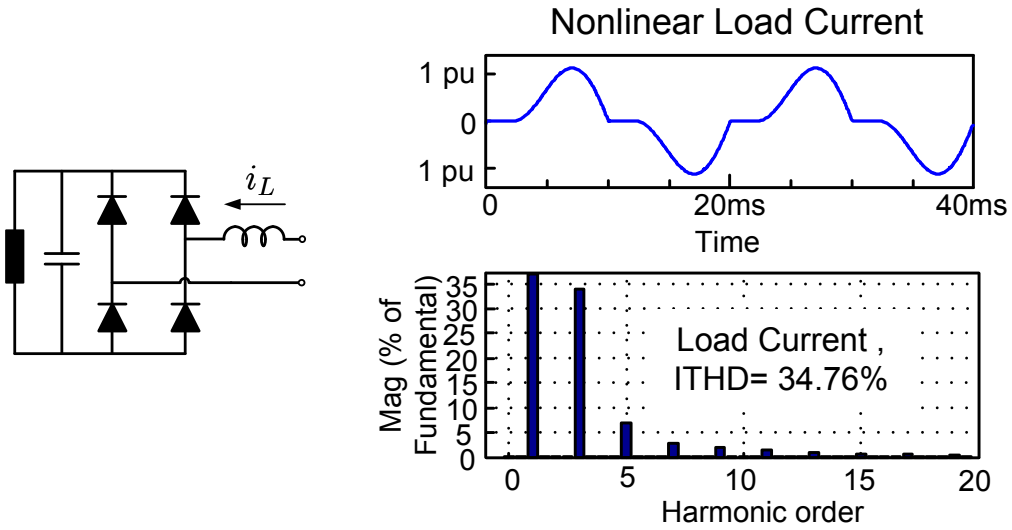


Figure 2.1: The Current Drawn by a Typical Single-phase Nonlinear Rectifier Load

Regarding connecting the microgrid to electric power system, some issues need to be addressed. Firstly, nonlinear load inside microgrid will produce current harmonics that pollute the power quality at PCC. A typical and widely used single phase nonlinear load is modeled as a rectifier feeding a capacitor. This type of load can generate multiple orders of current harmonics as shown in Fig. 2.1. These harmonics will reduce the power quality at PCC if no compensation is provided. The harmonics will distort the line current and produce at TDD much higher than 5%, which is not allowed according to IEEE 519 Std [32]. Secondly, if EPS is in abnormal condition, like voltage sag or swell, or more serious condition, such as power outage, the normal operation of the load inside microgrid will be affected [33]. Especially for those critical nonlinear loads, voltage harmonics and instability

will cause serious problems. On the other hand, if serious problems occur inside microgrid, for instance, the current surges over the limit, the interconnection of microgrid also affects other loads or systems connected to EPS.

In this chapter, a power converter building block (PCBB) is proposed to solve the various issues related to connecting microgrid to EPS.

2.3 Introduction to Proposed Power Converter Building Block (PCBB)

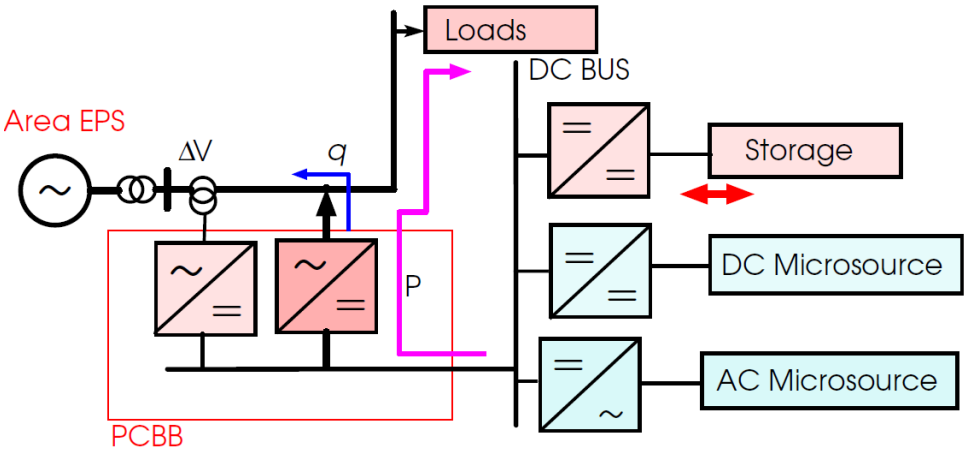


Figure 2.2: Proposed PCBB Facilitates the Connection of Microgrid to Area EPS

Fig. 2.2 shows the structure of the proposed mutifunctional power converter building block. The PCBB is installed at the point of common coupling to interconnect microgrid to EPS.

The PCBB consists of two voltage source inverters. One inverter is connected to EPS in parallel and the other is connected to EPS in series through an isolation transformer. Both of the two PCBB inverters are connected to the DC bus of

Table 2.1: Control Objectives of the PCBB Power Converters in Fig. 2.2

	Control Objectives	
2-3 Power Converters of PCBB	EPS-Connected	Islanding
shunt PCBB converter	Active Power Injection to Load (P_L) Active Power Injection to EPS (P_{EPS}) Reactive Power Compensation of the load (Q_L)	Active and Reactive Power Injection to Load (P_L and Q_L)
series PCBB converter	EPS voltage sag/swell compensation at PCC	

microgrid. The topology of the PCBB looks similar to a single-phase UPQC [34], [35]. However, the function and physical structure is different. The DC link of PCBB is not a stand-alone energy storage element as UPQC, but connected to the DC bus of microgrid.

The proposed PCBB facilitates both the connection between DC and AC bus within microgrid, and the connection of microgrid to Area EPS simultaneously. Table. 2.1 lists the functions of the two PCBB inverters under different operating scenarios of microgrid. The control objectives of PCBB to achieve the functions are listed in Table. 2.1.

Fig. 2.3 shows the basic configuration of PCBB, including power components, control and measurement system. The control system design will be discussed in depth in next section.

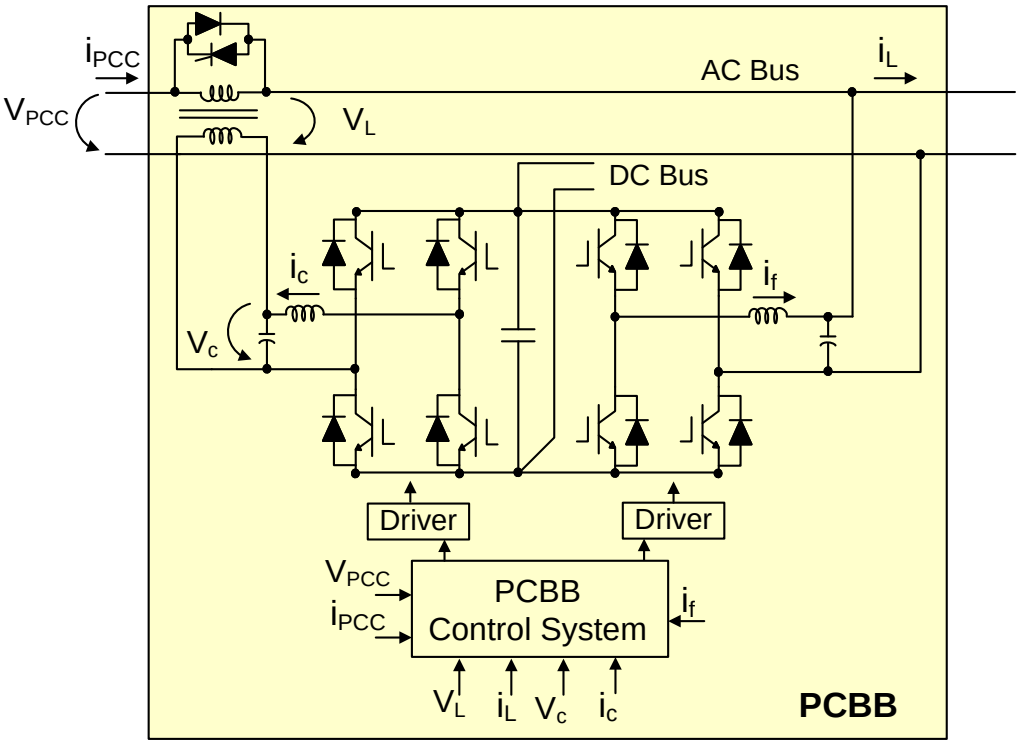


Figure 2.3: Basic Configurations of Proposed PCBB

2.4 Combined Active and Reactive Power Control Scheme with Simulation Verification

As shown in Table. 2.1, for different operating scenarios of microgrid, the control objectives of PCBB are different. This section proposes a combined active and reactive power control scheme for PCBB to achieve the multiple objectives.

When hybrid microgrid is connected to Area EPS, the shunt converter of PCBB is controlled in such a way that it will both compensate the reactive power of the load and supply active power to the load and Area EPS. The system equivalent circuit with the control scheme is shown in Fig. 2.4.

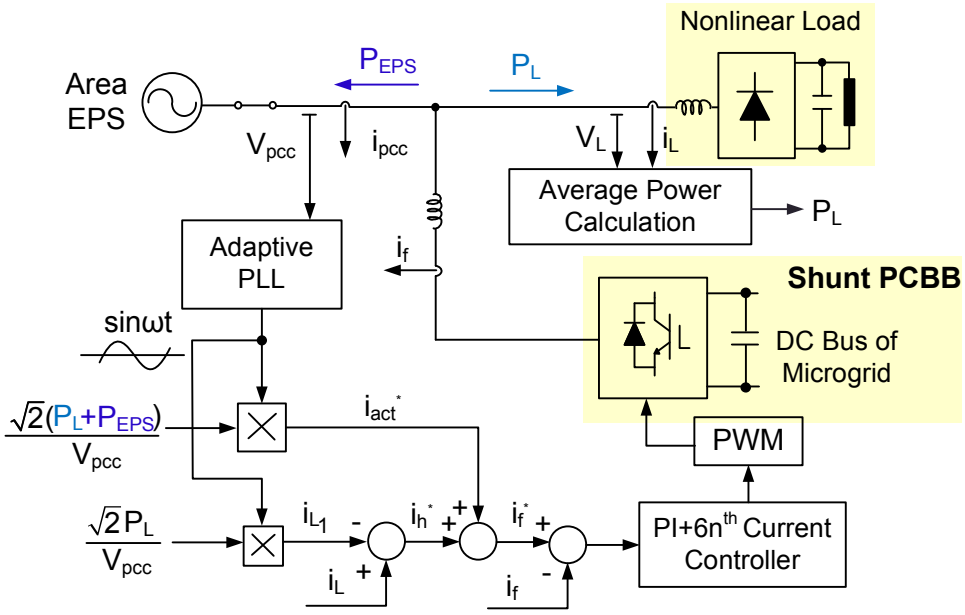


Figure 2.4: The EPS-connected Microgrid Equivalent Circuit and Combined PQ Control Scheme of PCBB

The control system consists of the following parts: the load harmonic current detection unit, the required active current generation unit, the current control system, and the PWM generator. The first two units generate the current reference $i_f{}^*$. A survey of the possible solutions to current reference generation is presented as follows.

2.4.1 Current Reference Generation

As discussed in previous section, the shunt PCBB will be responsible for compensating the load reactive power and current harmonics, as well as providing active power to load and EPS as required. Therefore, the current reference generation block of the PCBB control system includes:

- Load harmonic current detection
- Grid voltage synchronization
- Active current reference generation

2.4.1.1 Survey of Methods to Generate Reference Current

(1) Load harmonic current detection

The load harmonic current i_h^* detection unit in PCBB control system is the same as compensation reference generation unit for shunt active power filters [36]. Various methods regarding acquiring load current harmonics have been reported in literature. These methods can be classified into two categories: time domain and frequency domain. Here, time domain method is selected owing to its fast dynamic performance and simple implementation.

For time domain reference current generation of shunt active power filter, three different methods have been proposed with different compensation objectives [36]-[38]. [36] derives the instantaneous active and reactive power theory for three phase circuits. In this section, the instantaneous active and reactive power theory for single phase circuit will be derived based on [38]. To further clarify the difference among the three methods, some basic power quantities are predefined.

Instantaneous power is given as:

$$p(t) = v(t)i(t) \tag{2.1}$$

Active power is defined as:

$$P(t) = \frac{1}{T_c} \int_{\tau=t-T_c}^{t} p(\tau) d\tau \tag{2.2}$$

where T_c can be zero, one fundamental cycle, one-half cycle, or multiple cycles, depending on the compensation objective and the passive components' energy storage capacity [36].

According to Fryze's idea of non-active power [38], non-active power is defined as the unused power that causes increased line current and losses, greater generation requirements for utilities, and other negative effects to connected power system and equipment. For single phase power system with inductors, capacitors and nonlinear elements, non-active power is the power that circulates back and forth between the source and loads. The active and non-active current of single-phase circuit are expressed as:

$$i_p(t) = \frac{P(t)}{V_P^2(t)} v_p(t) \tag{2.3}$$

$$i_q(t) = i(t) - i_p(t) = i(t) - \frac{P(t)}{V_P^2(t)} v_p(t) \tag{2.4}$$

$$V_P(t) = \sqrt{\frac{1}{T_c} \int_{\tau=t-T_c}^{t} v_p^2(\tau) d\tau} \tag{2.5}$$

where $v_p(t)$ is the reference voltage that can be the voltage itself, the fundamental component of the voltage, or other quantity dependent on the compensation objective. After defining these key quantities, three time-domain reference current generation methods for shunt active filters are differentiated as follows.

For **sinusoidal single-phase circuit**, $v_s = V_s sin(\omega t)$, $i_L = I_L sin(\omega t - \alpha)$. Under such condition, the conventional reactive power theory can be applied to generate the non-active current for compensation, as given below:

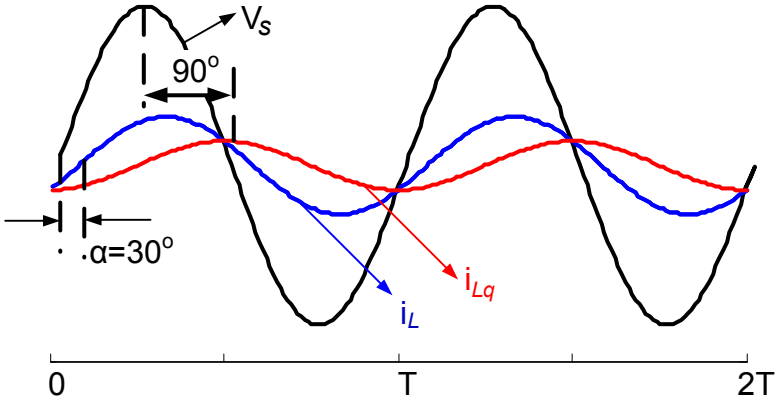


Figure 2.5: Nonactive current in Sinusoidal Single Phase Circuit

$$i_{Lq} = -I_L sin\alpha cos(\omega t) \tag{2.6}$$

For **non-sinusoidal single-phase circuit**, both load current and voltage contains harmonic components. $v_s = v_{S_1}(t) + v_h(t) = V_{S_1} sin(\omega t) + V_h sin(\omega_n t + \beta_h)$, and $i_L = I_{L_1} sin(\omega t - \alpha) + I_h sin(\omega_h t + \beta_h - \alpha_h)$, According to (2.4), the load active current and non-active current are derived as follows:

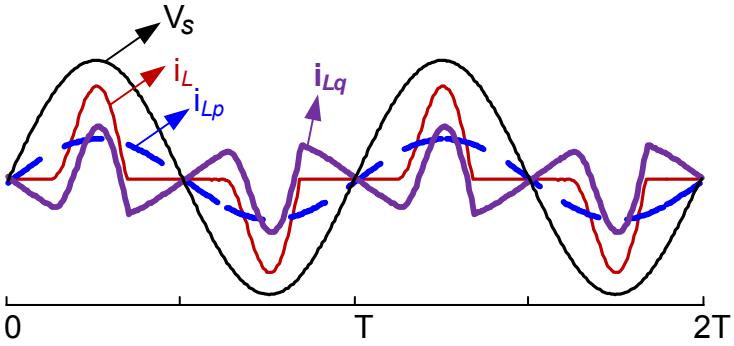


Figure 2.6: Nonactive current in Non-sinusoidal Single Phase Circuit

$$i_{Lp}(t) = \frac{V_{S_1}I_{L_1}cos\alpha + V_{S_1}I_h cos\alpha_h}{V_{S_1}^2 + V_h^2}[V_{S_1}sin(\omega t) + V_h sin(\omega_h t + \beta_h)] \quad (2.7)$$

$$\begin{aligned} i_{Lq}(t) &= -I_{L_1}sin\alpha cos(\omega t) - I_h sin\alpha_h cos(\omega_h t + \beta_h) \\ &+ \frac{V_h^2 I_{L_1}cos\alpha - V_{S_1}V_h I_h cos\alpha_h}{V_{S_1}^2 + V_h^2} sin(\omega t) \\ &+ \frac{V_{S_1}^2 I_h cos\alpha_h - V_{S_1}V_h I_{L_1} cos\alpha}{V_{S_1}^2 + V_h^2} sin(\omega_h t + \beta_h) \end{aligned} \quad (2.8)$$

Although the average power due to i_{Lq} is zero, the source current will not be sinusoidal unless the non-active current in (2.8) is compensated. Under the scenario that the source voltage is distorted, to guarantee unity power factor, we choose $v_P = v_{S_1}$ in (2.4). By doing so, the load active and non-active current is derived as:

$$i_{Lp}(t) = (I_{L_1}cos\alpha + \frac{V_h I_h cos\alpha_h}{V_{S_1}}) \cdot sin(\omega t) \quad (2.9)$$

$$\begin{aligned} i_{Lq}(t) &= -I_{L_1}sin\alpha cos(\omega t) - \frac{V_h I_h}{V_{S_1}} cos\alpha_h \cdot sin(\omega t) \\ &+ I_h sin(\omega_h t + \beta_h - \alpha_h) \end{aligned} \quad (2.10)$$

(2.9) shows that the active current is a sine wave, and the non-active current shown in (2.10) contains all harmonic current and fundamental reactive current. After compensation, the source current will become sinusoidal [39]. Such compensation objective is desired for most circuits, especially for the circuit contains rectifier type nonlinear load, which will pollute the source current with multiple orders of harmonics.

Single-phase circuit with distorted and non-periodic current is a rare case in power system and often indicate fault occurrence. For a load generating non-sinusoidal and non-periodic current, the equations (2.2), (2.9) and (2.10) can also be used to generate the compensation reference [39]. The generated $i_p(t)$ will be sinusoidal and in phase with reference voltage. The nonactive current will be the distorted current components and only consume reactive power.

(2) Grid Voltage Synchronization Methods for Single-phase Circuit

Generating a pure sine wave in phase with grid voltage is important for reference current generation. There are two types of grid voltage synchronization strategies: zero crossing detection (ZCD) and phase locked loop (PLL) [40], [41]. The strength and weakness of various voltage synchronization methods are discussed below.

ZCD is easy to implement and can be realized both in software and hardware. However, it does not provide instantaneous phase angle information of the grid, and is sensitive to noise. Therefore, for circuit with harmonics, it is not a desirable choice.

The diagram of **standard PLL** is shown in Fig. 2.7. The standard PLL has been the most widely applied technique for grid voltage synchronization. It has the advantage of easy implementation and good robustness. However, it shares the common disadvantage with ZCD, i.e. low susceptibility to harmonics and noise.

Moreover, the transient response is limited by the PI feedback control.

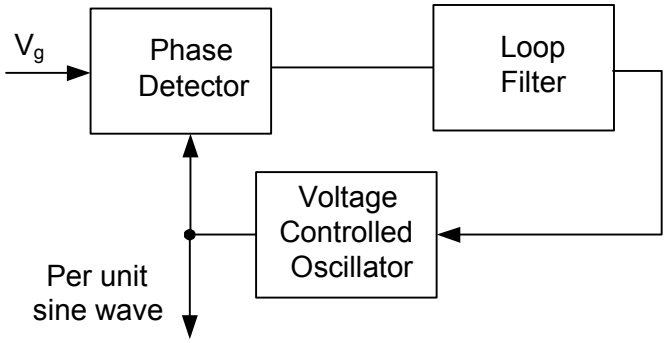


Figure 2.7: Block Diagram of Standard Single-phase PLL

The block diagram of **Adaptive PLL** is shown in Fig. 2.8 [42]. Compared to standard PLL, the adaptive PLL involves of more complex computations to tune the parameters, and is not appropriate for analogue implementation. However, it owns many promising characteristics, such as the capability of detecting all grid parameters, fast dynamic performance and high robustness.

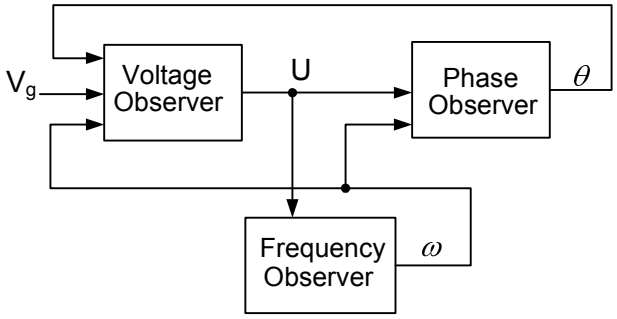


Figure 2.8: Block Diagram of Adaptive PLL

The diagram of **transformed three-phase PLL** is shown in Fig. 2.9. In a three-phase system, the grid frequency, phase angle and amplitude can be easily obtained from the voltage space vector. However, for a single-phase system, due to the lack of a quadrature signal, acquiring the phase angle information is much more difficult. Various methods have been proposed for virtual quadrature signal

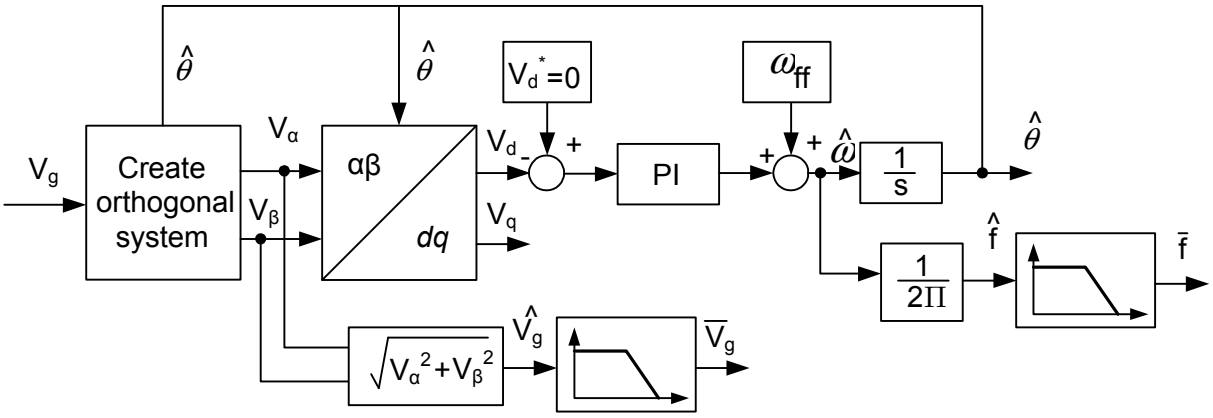


Figure 2.9: Block Diagram of single phase PLL, which imitates three phase PLL

generation, including $1^{st}/2^{nd}$ order filter, inverse park transformation, hardware phase shifter [40], [41].

(3) Active Current Reference Generation

The active current is absorbed by load or both EPS and Load. When the DGs inside microgrid has more than enough power to meet the load requirement, the active current from the shunt PCBB converter will feed both load side and EPS side. The active current reference is given by:

$$i^*_{act} = \frac{P_{EPS} + P_L}{V_g} sin\omega_1 t \tag{2.11}$$

When DGs output power is not enough to feed the load inside microgrid, both EPS and DGs will feed the load. The reference active current equation is same as (2.11), but the P_{EPS} is a negative value.

2.4.1.2 Current Reference Generation Approach Used in the Thesis

In this thesis, the harmonic current $i_h{}^*$ is obtained by subtracting the fundamental load current i_{L_1} from the actual load current i_L. The circuit belongs to the non-sinusoidal single-phase type. The time domain harmonic detection procedures are as follows:

1. Derivation of the RMS value of the fundamental active current of nonlinear load following (2.3)

$$I_{L_1} = \frac{\frac{1}{T_c}\int_{\tau=t-T_c}^{t} v_{PCC}(\tau) i_L(\tau) d\tau}{V_S} \tag{2.12}$$

2. Extract the synchronized sinusoidal waveform from v_{PCC} through PLL

$$i_{L_1}(t) = \sqrt{2} I_{L_1} sin(\omega_0 t) \tag{2.13}$$

3. Generate the non-active current to compensate

$$i_h(t) = i_L(t) - i_{L_1}(t) \tag{2.14}$$

The compensated line current i_{pcc} should be in phase with voltage at PCC to guarantee the unity power factor. Therefore, an adaptive PLL is utilized to achieve grid voltage synchronization. Compared with other grid synchronization strategies, the adaptive PLL has the advantages of fast transient response and low

susceptibility to harmonics. Fig. 2.10 shows the diagram of the adaptive PLL adopted.

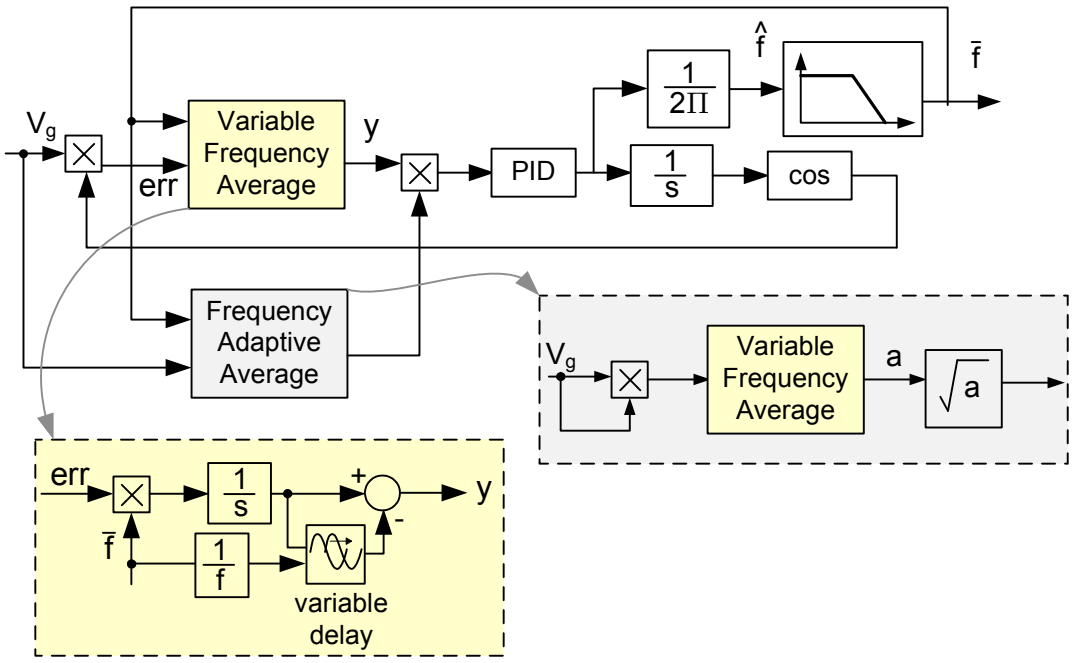


Figure 2.10: Block Diagram of Single Phase Frequency Adaptive PLL

The variable frequency average block is used to eliminate the harmonics. It will eliminate the second order harmonics introduced by fault as well as EPS voltage harmonics. The frequency controller input is multiplied by a gain which is frequency adaptive.

The active current reference $i_{act}{}^{*}$ is determined by the active power required by load and Area EPS, which can be calculated with (2.11).

2.4.2 Digital Current Control System Design

The objective of the current controller is to regulate the output current of the shunt PCBB converter, i_f, to follow the reference current $i_f{}^*$. Because many rectifier type nonlinear loads will generate multiple order harmonics, the controller is required to have high enough bandwidth to cover major order harmonics.

2.4.2.1 Review of Current Control Techniques

Various control techniques have been applied to regulate the output current of voltage source inverters. For example, standard PI control [34], [43], [44], deadbeat control [45], hysteresis control [46], proportional resonant control [47]-[49], etc. These controllers could be classified into linear controllers and nonlinear control techniques. Both control approaches have strength and limitations [50], [51]. The choice of current control scheme depends on the application, as well as the design requirements.

With the linear controllers, the inverter system could always have constant switching frequency, which simplifies the passive filter design and harmonic damping. Simplified techniques, such as bode plots and root locus, can be used to analyze the system stability. However, the design of linear current control algorithms is based on the generalization of the control problem around a specific operating point. Therefore, application of these schemes is probably best suited to problems where the load characteristics are well defined and are not subject to significant

variation.

Among nonlinear control algorithms, hysteresis control is most widely applied owing to its simplicity and fast dynamic response. Unlike the linear regulators, hysteresis control produces the switching signals by directly comparing the reference and output. However, the switching frequency of hysteresis control is variable. Therefore, it alters the harmonic spectrum of the output current. A number of research work tries to develop hysteresis controllers with fixed switching frequency [52]-[54]. However, the implementation of these controllers is significantly more complex.

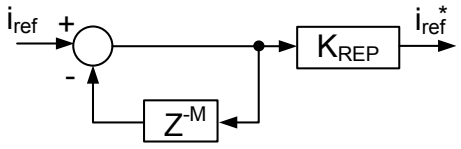


Figure 2.11: General implementation of the repetitive controller

Another popular nonlinear control scheme is repetitive control [55], [56]. It represents the reference signal in terms of laplace or z-transform and then adds it to the original system model. If the reference signal is sinusoidal, the digital implementation of repetitive control becomes simple. Fig. 2.11 shows the implementation diagram of repetitive controller for sinusoidal reference input [56]. Only a suitably sized delay and a positive feedback is required. However, when the reference signal is not sinusoidal, such as active power filter, the controller becomes quite complex. In addition, though repetitive control achieves zero steady state error, the narrow bandwidth leads to poor transient performance.

The fuzzy logic approach has also attracted attention in current control applications [57], [58]. The heuristic controller uses fuzzy membership functions to describe the control law. The nonlinear control surface of a fuzzy logic regulator defines appropriate sensitivity for each operating point, and thereby improves tracking performance and reduces transient overshoot. Fuzzy logic current controllers have been reported with improved transient performance compared to conventional linear controllers [57], [58]. However, these controllers are sensitive to variations of the fuzzy membership shapes. Systematic approach to design the fuzzy membership functions has not been reported.

In this thesis, linear current control strategies are adopted owing to the constant switching frequency, simplified digital implementation, as well as convenient stability and robustness analysis.

The most widely applied linear controller is PI controller. However, it has the disadvantages of phase delay and amplitude error in steady-state. Moreover, it could only provide very limited bandwidth, which is not able to cover the major harmonic orders. To overcome such drawback, proportional resonant (PR) controller is proposed [59]. Though slightly more complex, PR controller owns many advantages compared to PI controller. It displays a good steady state performance with zero steady state error [60]. Compared with predictive current control [61], PR controller is more robust to parameter variations. Furthermore, it is quite easy and straightforward to be digitally implemented as PI controller. Other advantages of applying PR controller to the applications in this thesis are discussed as follows.

The transfer function of ideal PR controller is:

$$G_{PR}(s) = K_P + \frac{2K_I s}{s^2 + \omega^2} \tag{2.15}$$

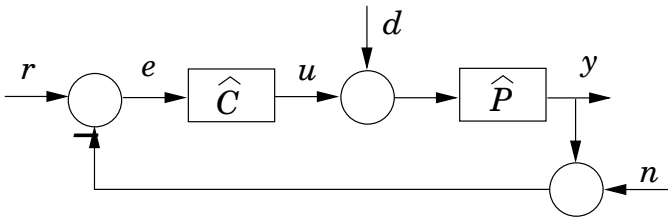


Figure 2.12: Diagram of a Typical Feedback Control System

Fig. 2.12 shows the diagram of a typical unity feedback loop, where e is the tracking error. When noise n and disturbance d are zero, e equals the reference input r, minus the plant output y. $\widehat{C}$ and $\widehat{P}$ are the controller transfer function and plant transfer function respectively. Define the open loop transfer function $\widehat{L} = \widehat{P}\widehat{C}$, the transfer function from reference input r to tracking error e is:

$$\begin{aligned} \widehat{S} &= \frac{1}{1+\widehat{L}} \\ &= \frac{1}{1+\widehat{P}\widehat{C}} \end{aligned} \tag{2.16}$$

To achieve asymptotic tracking, given a reference r, $e(\infty) = 0$ must be guaranteed.

The Laplace transform of a unit step reference is $\frac{1}{s}$. According to (2.16), the

error transfer function becomes:

$$\begin{aligned} e(s) &= r(s)\widehat{S} \\ &= \frac{1}{s}\widehat{S} \end{aligned} \tag{2.17}$$

Therefore, following final value theorem,

$$\begin{aligned} e(\infty) &= se(s)|_{s=0} \\ &= \widehat{S}(0) \end{aligned} \tag{2.18}$$

According to (2.16), when controller $\widehat{C}$ has an integrator, the close loop transfer function will have a zero $s = 0$, and asymptotic tracking is achieved. Therefore, integrator is capable of asymptotic tracking when the system has a step reference input.

However, when the system has a sinusoidal input, $sin(\omega t)$, the error transfer function becomes

$$e(s) = \frac{\omega}{s^2 + \omega^2}\widehat{S} \tag{2.19}$$

To achieve asymptotic tracking, the controller must have a pole at $s = j\omega$, and pure integrator in $\widehat{C}$ is not able to achieve asymptotic tracking. Therefore, in this thesis, resonant controller with a pole at $s = j\omega$ is adopted.

Similarly, if we let $r = n = 0$, the output transfer function is

$$\begin{aligned} y(s) &= \frac{\widehat{P}}{1+\widehat{L}} d(s) \\ &= \frac{\widehat{P}}{1+\widehat{P}\widehat{C}} d(s) \end{aligned} \tag{2.20}$$

To achieve asymptotic regulation, we need $y(\infty) = 0$ for a sinusoidal disturbance input. Therefore, should $\widehat{P}$ possess a zero or $\widehat{C}$ possess a pole at $s = j\omega$. Therefore, resonant controller is preferred over integrator to achieve asymptotic tracking and asymptotic regulation.

PR controller also owns advantage in digital implementation to substitute PI controller. A PI controller introduces infinite gain at DC. Therefore, the DC offset in the sampling and ADC circuit and/or the numerical error caused by the limited word-size of the DSP will be accumulated and eventually leads to output saturation. In some cases, the ideal integrator of PI controller cannot function in practical case. To solve such problem, the ideal integrator is approximated by a low pass filter with a limited gain, or high pass filter with a low cutoff frequency to filter the DC output as in (2.21), (2.22). For PR controller, these problems are alleviated.

$$G_I(s) = \frac{K_I}{1+\frac{s}{\omega_c}} \tag{2.21}$$

$$G_{RI}(s) = \frac{2K_I\omega_c s}{s^2+2\omega_c s+\omega^2} \tag{2.22}$$

When the PI and PR controller are digitally implemented, a sample delay in the feedback loop will be introduced. The sample delay will reduce the phase margin significantly, and thus can cause instability. PR controller has better stability because it has no phase lag at DC. Therefore, PR controller has been preferred by many researchers [41], [49], [59].

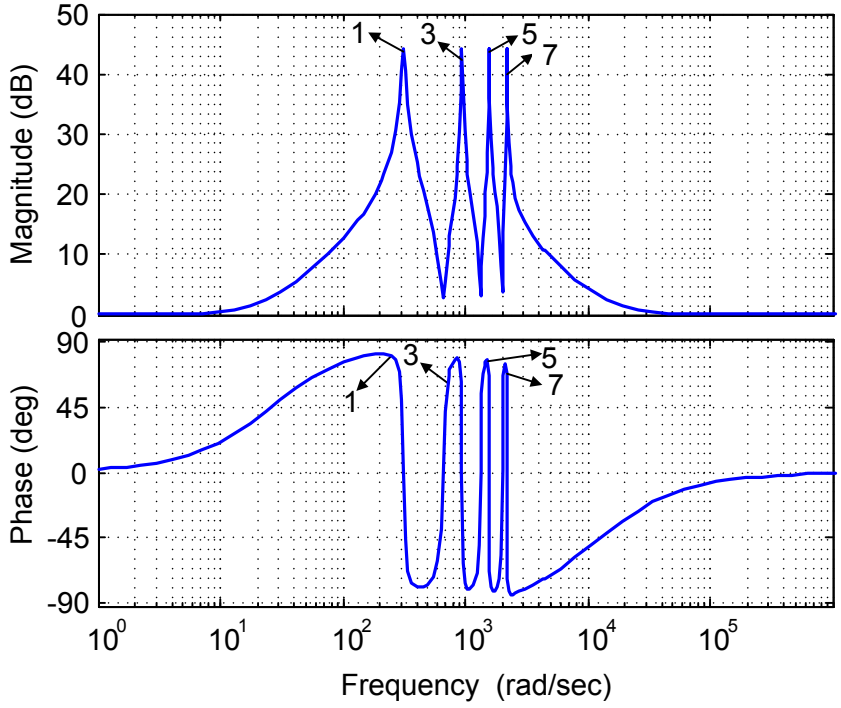


Figure 2.13: Bode plot of $G_{Rh}(s)$

To compensate high order harmonics, such as 3^{rd}, 5^{th}, 7^{th} order harmonic current, high order resonant controllers can be implemented. The transfer function of resonant controller becomes:

$$G_{Rh}(s) = \sum_{h=1,3,5,7} \frac{2K_I hs}{s^2 + (h\omega)^2} \tag{2.23}$$

with low pass filter for anti-windup,

$$G_{Rh}(s) = \sum_{h=1,3,5,7} \frac{2K_I h\omega_c s}{s^2 + 2\omega_c s + (h\omega)^2} \tag{2.24}$$

Fig. 2.13 shows the bode plot of resonant controller. It is clearly seen that the controller induces very high gain at each resonant frequency.

2.4.2.2 PI+6nth Current Control Scheme

For PCBB current control system, we employ synchronous rotating frame based PI+$6n^{th}$ Resonant Controller [62], [63], owing to its advantage of compensating multiple order harmonics with fewer resonant controllers [62], [63].

As the synchronous reference frame (SRF) rotates synchronously with the grid voltage vector, it transforms the variables at fundamental frequency into dc values; therefore, the filtering and control can be more easily achieved, and PI controller will not produce phase or amplitude error for the fundamental component in SRF. Moreover, it requires less resonant controllers to compensate high order harmonics. For instance, both the 5^{th} order harmonics in positive sequence, and the 7^{th} order harmonics in negative sequence, will become 6^{th} order harmonics in opposite rotating direction after transformation. Thus, one 6^{th} order resonant filter can do the compensation tasks for both 5^{th} and 7^{th} order harmonics. Furthermore, all the $(6n-1)^{th}$ and $(6n+1)^{th}$ order harmonics will be transformed to $6n^{th}$ order but in opposite rotating direction. So the number of resonant controllers used to filter these high order harmonics could be reduced to half.

$$G_{PI+6n^{th}}(s) = K_P + \frac{K_I}{1+\frac{s}{\omega_c}} + \frac{2K_I\omega_c s}{s^2+2\omega_c s+(6\omega_0)^2} \tag{2.25}$$

To apply the SRF PI+$6n^{th}$ RES controller to our single-phase system, we need to build a rotating reference frame first. The method in [64] is used to create virtual axes to build a rotating reference frame for single-phase system.

The general block diagram of the current control scheme is shown in Fig. 2.14. (2.26) gives the transfer function of the PCBB shunt converter with output filter.

$$G(s) = \frac{1}{Ls+R} \tag{2.26}$$

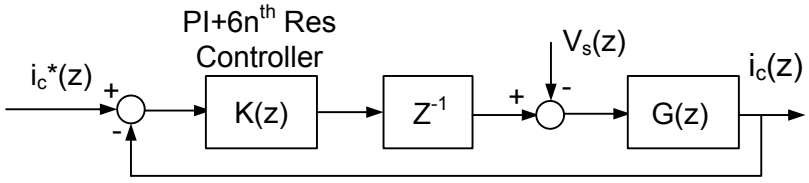


Figure 2.14: Block diagram of current control scheme for the shunt PCBB converter with plant model

In order to design the digital controller, the continuous transfer function of the model is discretized through step-invariant transformation. (2.27) gives the z-domain transfer function of the system.

$$G(z) = \frac{bz^{-1}}{1-az^{-1}} \tag{2.27}$$

where $b = \frac{1}{R}(1 - e^{-\frac{RT_s}{L}})$, $a = e^{-\frac{RT_s}{L}}$, and T_s is the sampling time.

The computational delay is also included in the system model as shown in Fig. 2.14; and it is represented by a unit lag.

The continuous transfer function of PI+$6n^{th}$ resonant controller is given in (2.25). Through z-transform, the sampled $6n^{th}$ Resonant Controller is given by (2.28):

$$K_{I6}(z) = K_{I6}\frac{T_s[cos(6\omega_0 T_s)z - 1]}{z^2 - 2cos(6\omega_0 T_s)z + 1} \tag{2.28}$$

where ω_0 is the fundamental frequency of the voltage at PCC.

Since the delay involved in the digital system implementation will affect the performance and stability of the controlled system [65], [66], it should be properly considered during the digital controller design. Predictive current control can solve such problem; however, it adds more complexity to plant modeling and load parameter estimation. In [67], a more simplified and practical method is proposed to handle the delay issue. Rather than reference current prediction, [67] uses a scheme predicting only the harmonic components in the modulating signal. It predicts the output of the resonant integrator by moving the zero of the transfer function in the plane with the following formula:

$$K_{I6}(z) = K_{I6}\frac{T_s[cos(6\omega_0 T_s)z - 1]}{z^2 - 2cos(6\omega_0 T_s)z + 1} \tag{2.29}$$

$$\rightarrow K_{I6}(z) = K_{I6}\frac{T_s[z - cos(6\omega_0 T_s)]}{z^2 - 2cos(6\omega_0 T_s)z + 1} \tag{2.30}$$

2.4.2.3 Simulation Results

To demonstrate the validity and soundness of the controller proposed, MATLAB/SIMULINK is used simulate the system under three different conditions. First, the PCBB shunt converter only compensates the harmonic current of the load; second, the PCBB supplies both the reactive power and partial active power to the load within microgrid; third, the PCBB supplies the full power to the load and injects active power to the Electric Power System through PCC. The corresponding simulation results are shown in Fig. 2.15. We can see that the PCBB can not only effectively compensate the current harmonics injected by nonlinear load but also feed active power to load and Area EPS. The TDD of the line current at PCC decreases from 60.54% to around 2%. The compensated line current TDD at PCC satisfies the requirement of IEEE 1547 Std [17], which allows a maximum 5% current demand distortion.

Compared with other combined PQ control schemes in previous literature [68]-[70] proposed for single DG system, the control method proposed in this chapter for microgrid has many advantages: first, the current reference generation unit using time domain method produces faster dynamic response and the adaptive

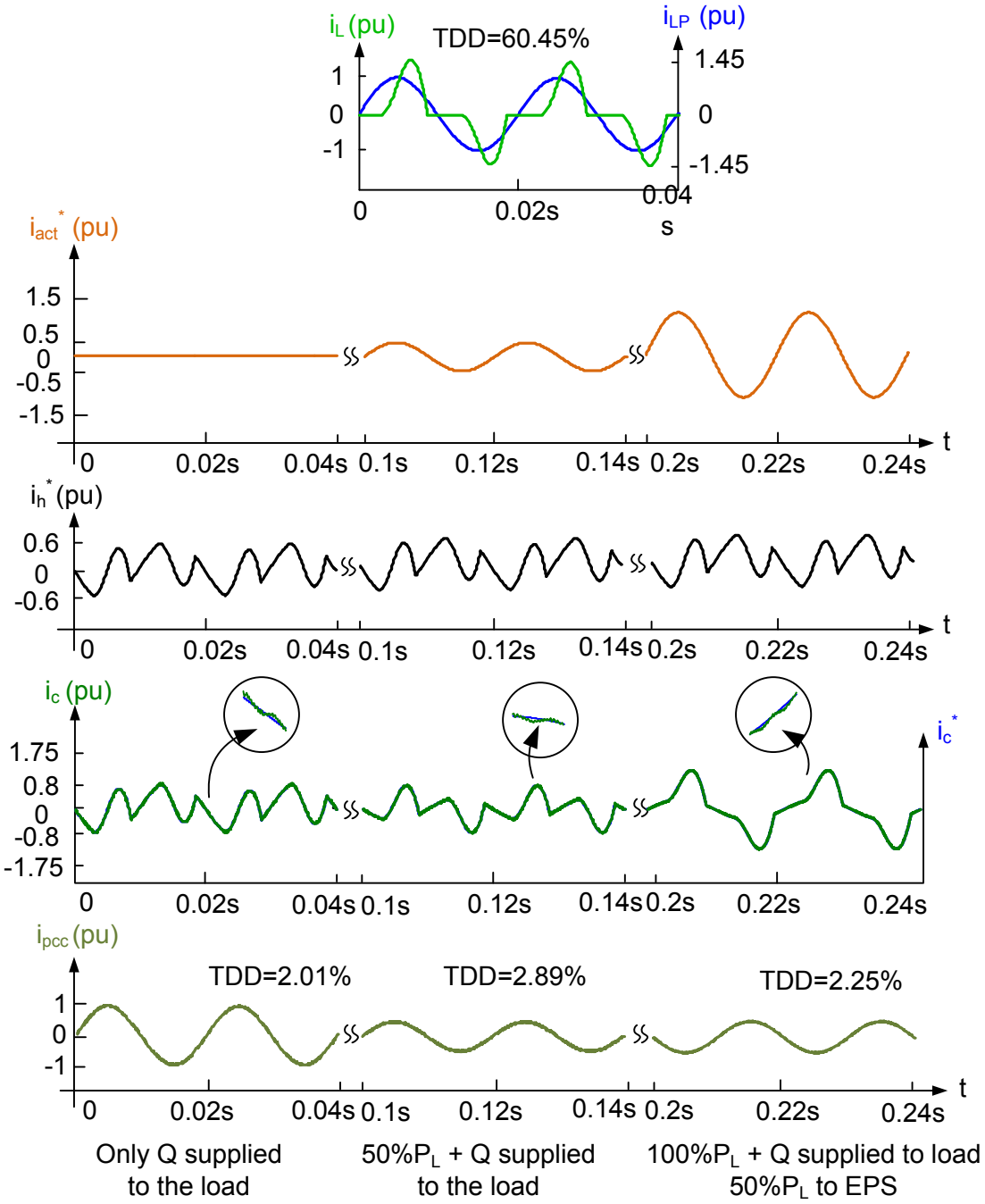


Figure 2.15: The Simulation Results of the System Operating under EPS-connected Mode

PLL has outstanding performance under voltage distortion; second, the SRF based $PI+6n^{th}$ RES controller displays better steady-state performance under nonlinear load condition.

2.4.2.4 Stability and Robustness Analysis

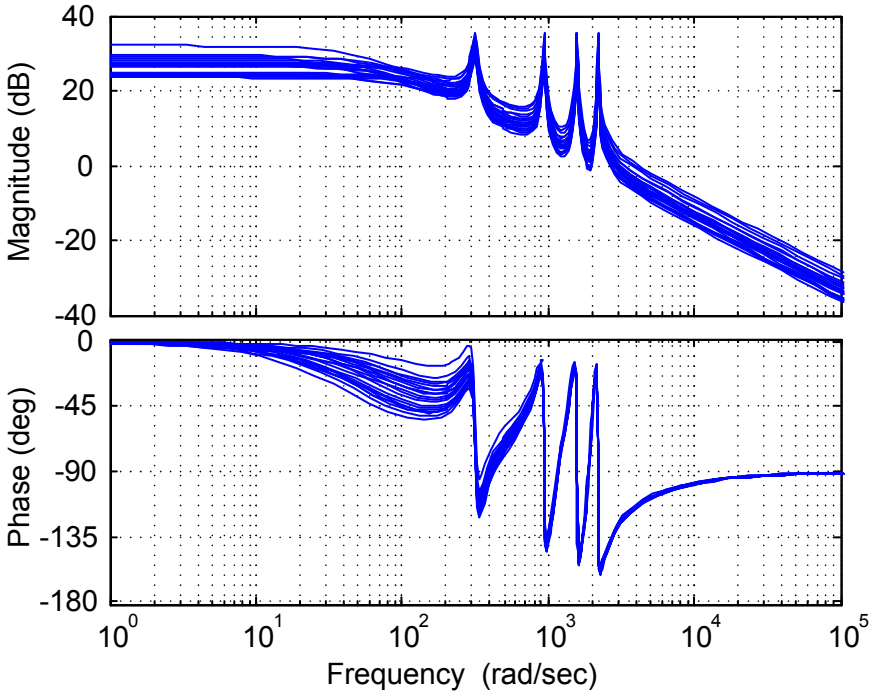


Figure 2.16: Bode plots of 20 Open Loop Shunt PCBB Systems with PR controller with 50% Parameters (L,R) variation

Fig. 2.16 shows the bode plots of 20 open loop transfer functions of shunt PCBB with 50% parameter variations. The frequency response demonstrates the robust stability of the proposed control scheme.

2.4.3 Additional Operating Condition of Microgrid

2.4.3.1 EPS Sag/Swell Mode

When EPS has a sag or swell, the series part will act as a dynamic voltage restorer to compensate the sag or swell, and the shunt part continues with the previous functions. Fig. 2.17 depicts the equivalent circuit of the hybrid microgrid

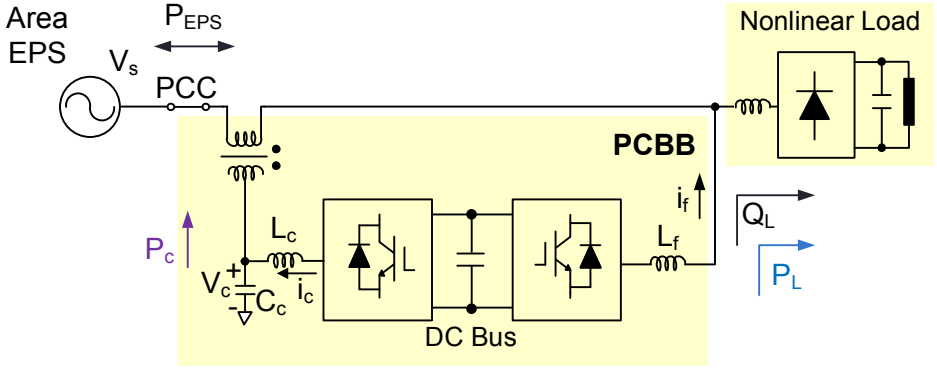


Figure 2.17: Equivalent circuit of hybrid microgrid with PCBB when EPS experiences sag/swell

with PCBB during EPS sag/swell mode.

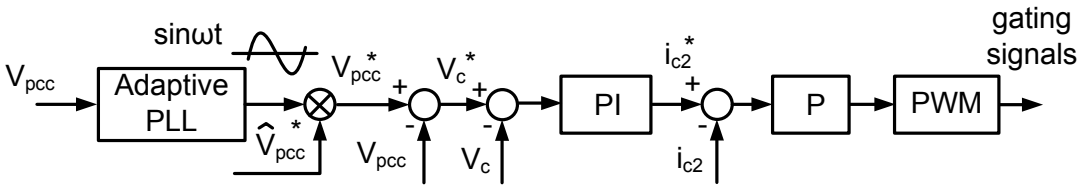


Figure 2.18: Block diagram of cascaded control scheme for the series PCBB converter

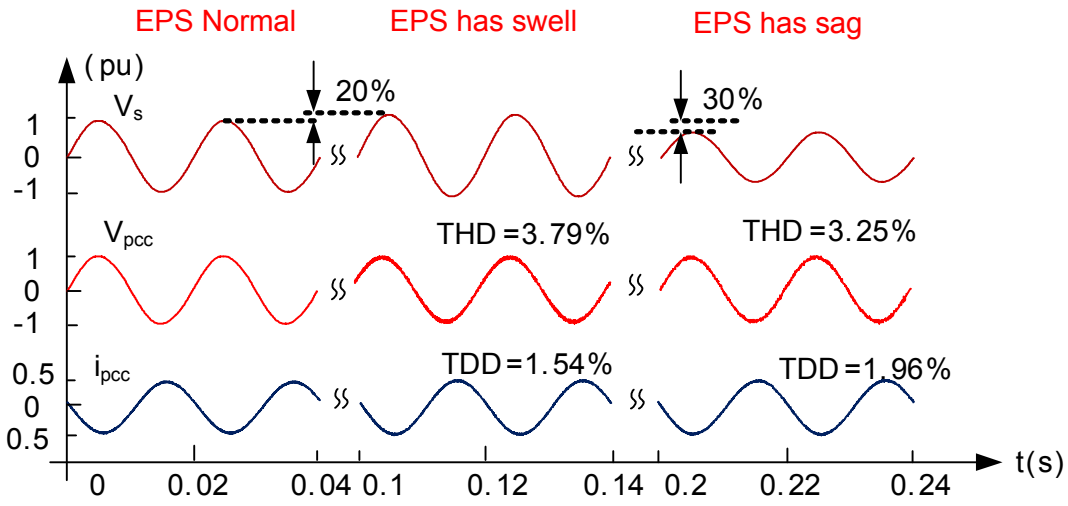


Figure 2.19: The Simulation Results of the System Operating under EPS Sag/Swell Mode

As the voltage quality has an impact on the performance of the shunt part in current harmonics compensation [71], cascaded PI control strategy is applied to

improve the dynamic performance of the voltage compensation. Fig. 2.18 shows the cascaded control scheme applied to the series PCBB converter. Shunt PCBB converter remains regulated with combined PQ control strategy. The DC link of the PCBB will provide power for both shunt and series converter. Since the DC link is connected to the DC bus of the microgrid, which is fed by renewable energy sources, the PCBB could compensate a relatively longer duration of voltage sag/swell. This is an advantage of the PCBB proposed in this chapter compared with traditional single energy storage element based DC link in dynamic voltage restorer and UPQC. Simulation results in Fig. 2.19 demonstrates the ride-through ability of microgrid under EPS voltage sag and swell condition with the assistance from PCBB.

2.4.3.2 Islanding Mode

When severe fault like power outage occurs at PCC, the PCBB should island the microgrid from Area EPS smoothly and quickly. Once the islanding event is detected, the static switch is opened and the shunt part of PCBB shifts from current regulation to voltage regulation. After the fault is cleared, the control system will detect an instant when the phase difference between voltage vectors of the two power systems is close to zero, and then close the static switch to shift microgrid back to EPS-connected operation. Simultaneously, the control mode of shunt PCBB converter transfers back to current regulation.

During islanding mode, only shunt PCBB converter functions, and the control

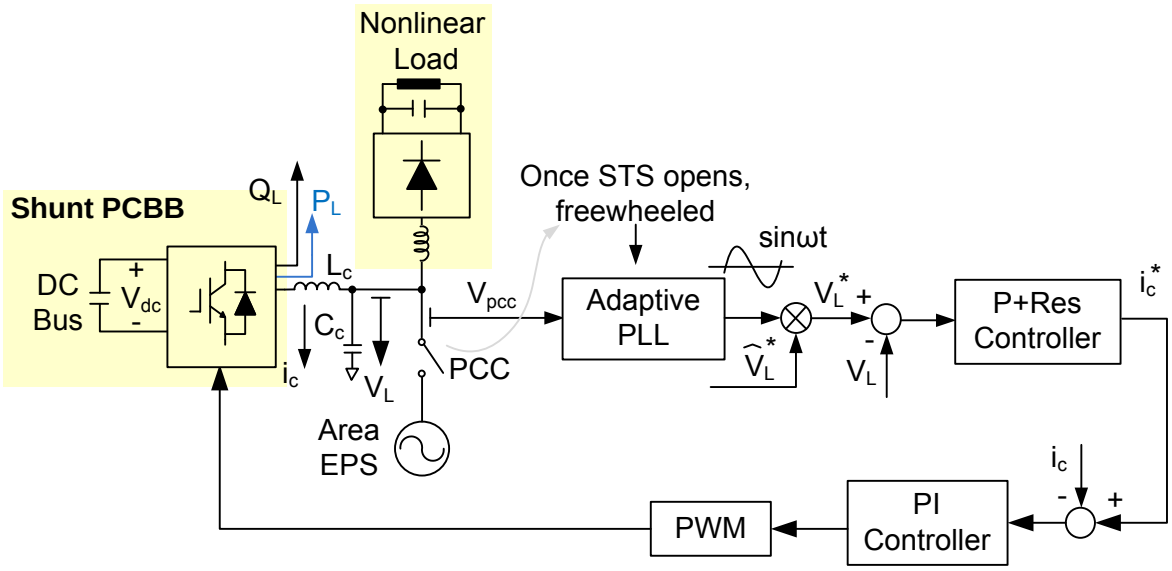


Figure 2.20: The Equivalent Circuit of the Whole System in Islanding Mode and Corresponding Voltage Regulation Scheme of PCBB Shunt Part

objective of the shunt converter is to provide a high quality output voltage to local load. Fig. 2.20 shows the system equivalent circuit and voltage regulation strategy in islanding mode. To produce a high quality output voltage, the outer loop of the controller uses a proportional with 1^{st} order resonant controller. The resonant controller introduces a relatively high gain at the fundamental frequency of the nominal load voltage. The inner current loop is used to limit the output current and improve the control dynamics.

The digital PR controller in the outer loop can be designed in a similar fashion to the resonant controller used for current control. (2.31) gives the transfer function of digital PR controller.

$$K_v(s) = K_P + K_{I1}\frac{T_s[z - cos(\omega_0 T_s)]}{z^2 - 2cos(\omega_0 T_s)z + 1} \tag{2.31}$$

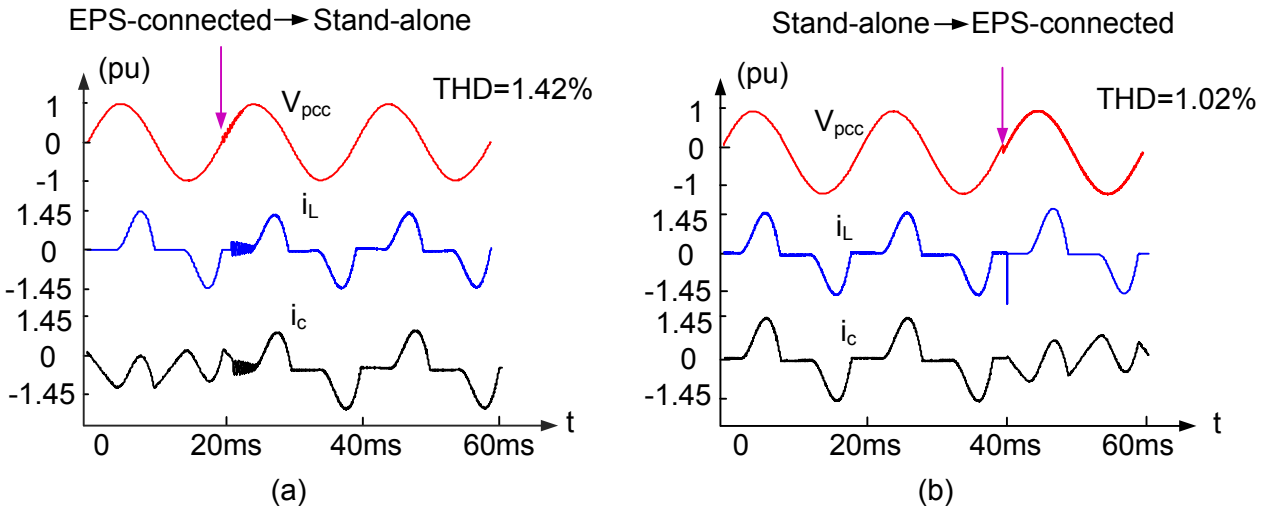


Figure 2.21: The Simulation Results of the System Operating in Islanding Mode

To demonstrate the ability of PCBB in facilitating the islanding operation of microgrid and transitioning microgrid between parallel mode and islanding mode, we simulate the system for two cases. Case 1: microgrid transitions from parallel mode to islanding mode; Case 2: microgrid transitions from islanding mode back to parallel mode. From the simulation results in Fig. 2.21, it is clear to see that the THD of the output voltage is below 1.5%, much lower than the 5% THD limit set by UL1741 [72] for islanded power system. Moreover, the simulation results also demonstrate that the transition process of microgrid between different operation modes is seamless with the assistance of PCBB.

2.4.3.3 Stability and Robustness Analysis

Fig. 2.22 shows the bode plots of 20 open loop transfer functions of series PCBB with 50% parameter variation. Fig. 2.23 shows the bode plots of 20 open loop transfer functions of shunt PCBB in islanding mode with 50% parameter

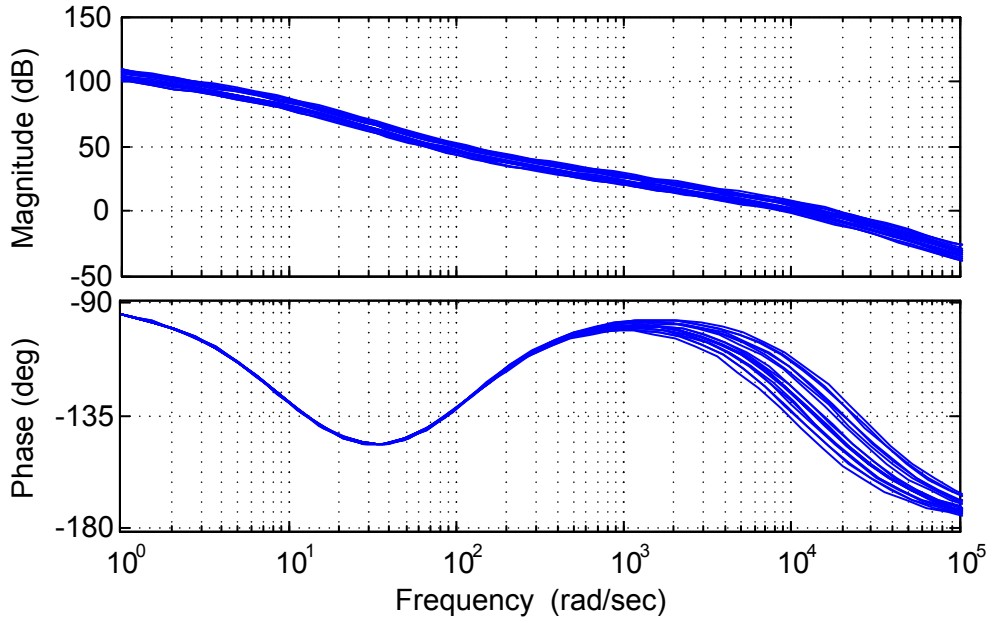


Figure 2.22: Bode plots of 20 Open Loop Controlled Series PCBB Systems with 50% Parameters (L,C) variation

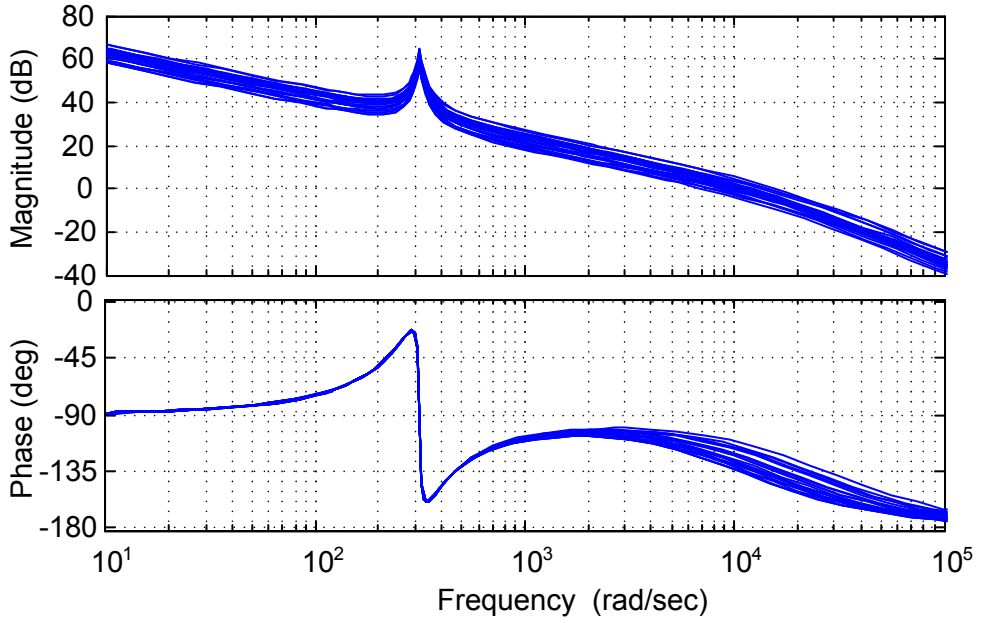


Figure 2.23: Bode plots of 20 Open Loop Controlled Shunt PCBB Systems during Islanding Mode with 50% Parameters (L,C) variation

variation. The frequency responses demonstrate the robust stability of the proposed control strategies.

2.4.3.4 Islanding Detection and Anti-islanding

Fig. 2.24 summarizes the islanding detection methods reported in literature [73], [74]. The anti-islanding schemes can be divided into four categories: passive local detection methods, active local detection methods, utility level method and the use of communications between the utility and inverter side [73], [74]. Passive local detection methods are mostly relay based methods. Such method has a common disadvantage known as non detectable zone (NDZ). NDZ is the range of local loads for which the islanding prevention method under consideration can be made to fail to detect islanding. Considering the anti-islanding requirement, methods with NDZ should be excluded.

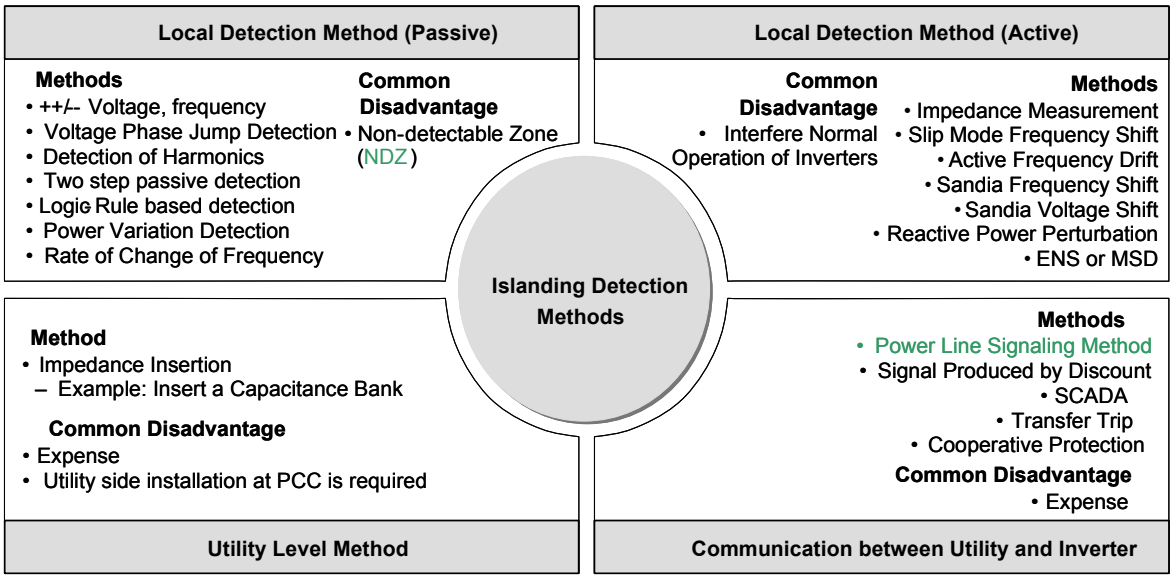


Figure 2.24: Literature Review of Islanding Detection Methods

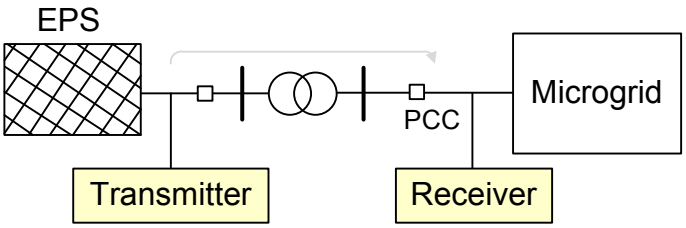


Figure 2.25: Simplified Diagram of Communication Based Islanding Detection Scheme

Fig. 2.25 shows the communication based islanding detection scheme [75]. As shown in Fig. 2.25, the power line communication system includes transmitters at the EPS side and receivers at the microgrid side. The power lines are used as a communication channel. If the power line communication signals disappears, this indicates the microgrid is islanded from the EPS. The microgrid should cease injecting power to EPS and transition to islanding operation.

Compared with other active detection methods, the communication approach is preferred for islanding detection of microgrid system for two reasons:

- It will not affect the stability of the system since no perturbation is introduced to the control scheme.
- The cost of sensors is not high for the proposed microgrid since the renewable sources and energy storage elements are connected to DC bus, in other words, the number of converters (PCBB) connected to EPS is limited.

2.4.4 Seamless Transition between Three Operating Modes

Seamless transition between different operating scenarios is important to sustain the normal operation of critical loads. Because the shunt PCBB is operated as current compensator in EPS connected operation mode, while as a voltage source inverter in islanding mode, special considerations must be given when switching between different operating scenarios.

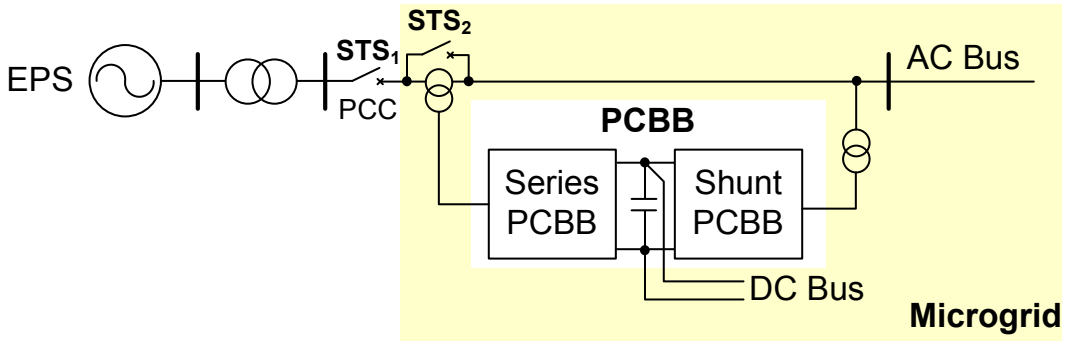


Figure 2.26: Simplified Diagram of Microgrid Connected to EPS through PCBB

The procedures of shifting microgrid from EPS connected mode to EPS Sag/Swell mode and islanding mode are shown in Fig. 2.27. First, the microgrid controller detects whether fault happens at PCC. According to IEEE 1547 Std [17], when the RMS value of PCC voltage exceeds the range between 88 $\sim$ 110% of base voltage, or frequency variation is beyond $-0.7 \sim +0.5$Hz, EPS is considered in fault condition. If fault is detected and PCC voltage is dipped less than 50% or swelled below than 20%, microgrid is shifted to EPS Sag/Swell mode. Otherwise, microgrid is shifted to islanding mode.

When microgrid is shifted to EPS Sag/Swell mode, the gating signal of static

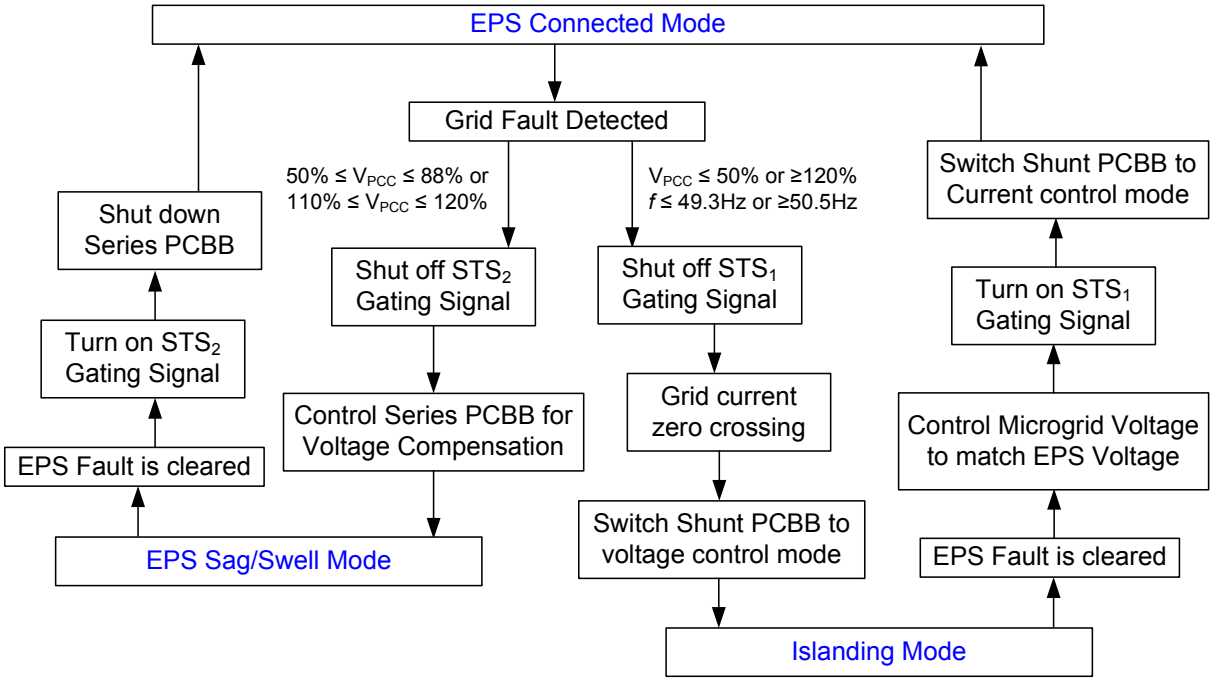


Figure 2.27: Procedures of Transitioning Microgrid between Different Operating Modes through Controlling PCBB

switch STS_2 is shut off and series PCBB is controlled to compensate the voltage sag or swell. The detailed control scheme has been illustrated in **2.4.3.1** on page 46. Once the EPS voltage is monitored to be back to normal, the series PCBB stops functioning, and STS_2 is turned on to shift microgrid to EPS connected operation mode.

When microgrid is shifted to islanding mode, [76] described the procedures. First, the gating signal of static switch at PCC, STS_1 is shut off. At the moment the grid current crosses the first zero, the shunt PCBB is switched from current control to voltage control. The detailed control scheme is described in **2.4.3.2** on page 48. When the fault with EPS is cleared, PCBB is controlled to synchronize the load voltage to EPS voltage. When the voltages of EPS and microgrid are

locked in both magnitude and frequency, STS_1 is turned on and shunt PCBB is switched back to current control mode. Microgrid is shifted back to EPS connected operation mode.

2.4.5 Real Time Digital Simulation Results

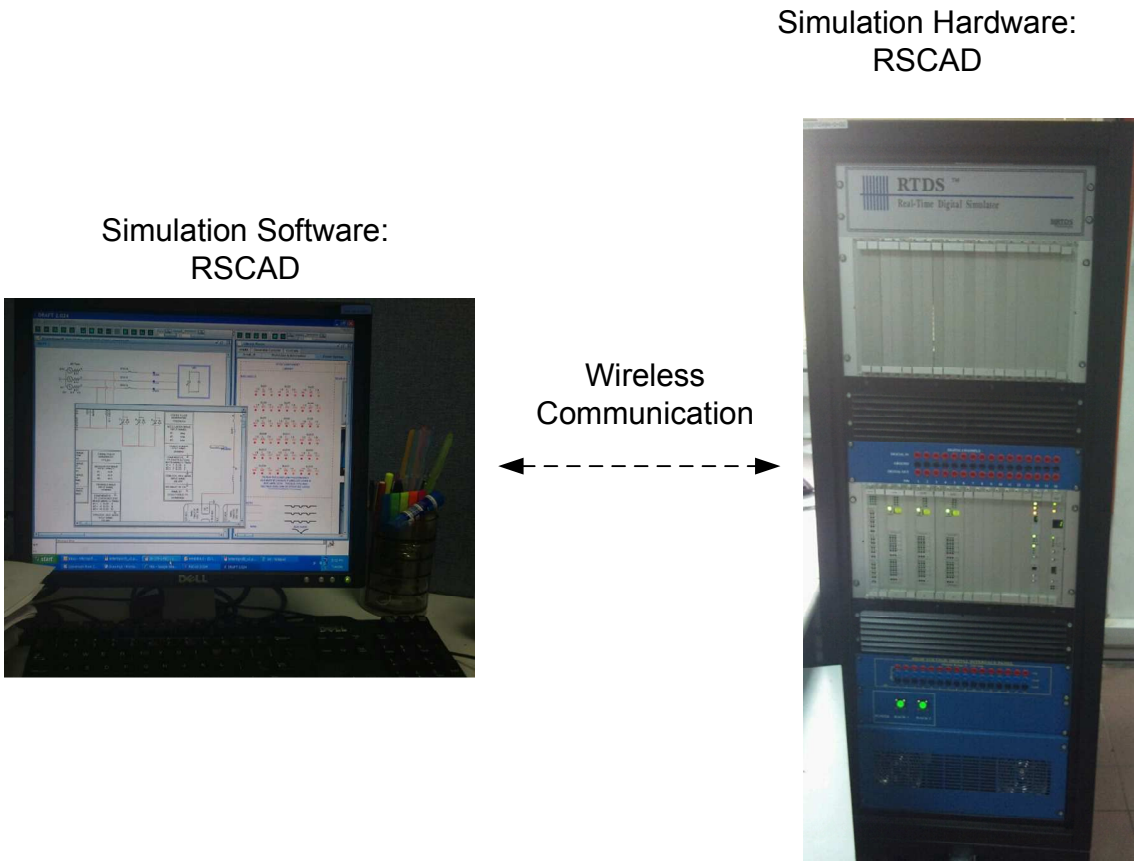


Figure 2.28: RTDS System Set Up

The proposed multifunctional PCBB with digital control scheme has been offline simulated with MATLAB/SIMULINK. Similar offline simulation can also be performed with other commercial softwares including PSCAD/EMTDC, DigSilent/PowerFactory, etc. Although these softwares demonstrate powerful performance in simulating high switching frequency devices as well as control logics and

algorithms, they share some common disadvantages. The first disadvantage is the low speed of execution time, especially the simulation of circuits with high frequency switching devices. Though simplified or average model can be used to reduce the simulation complexity, investigation of the system electromagnetic transient performance becomes difficult. Secondly, these offline simulators are not able to reproduce the run-time behavior of the digital controllers. They are only capable of simulating predefined events instead of performing real time events to the system under simulation. Therefore, potential design bugs in the real time environment might not be discovered.

To further validate the proposed digital controlled PCBB in real time environment, real time digital simulation is performed with RTDS [77]. The RTDS simulator is fully digital electromagnetic transient power system simulator that operates in real time [77]. As Fig. 2.28 shows, RTDS contains both software and hardware. The software, RSCAD, is a real time version of PSCAD. The software provides simulation models and software packages for power and control circuit, analog input/output, digital input/output, etc. With RSCAD, both draft file and run-time file are generated. The draft file is used to deploy the power and control circuit to be simulated. The run-time provides the functions of monitoring the circuit variables, controlling and modifying system parameters, executing new tasks in real time.

After the draft file and run-time file are compiled, the simulation command will be sent to the hardware simulator. The RTDS hardware simulator includes

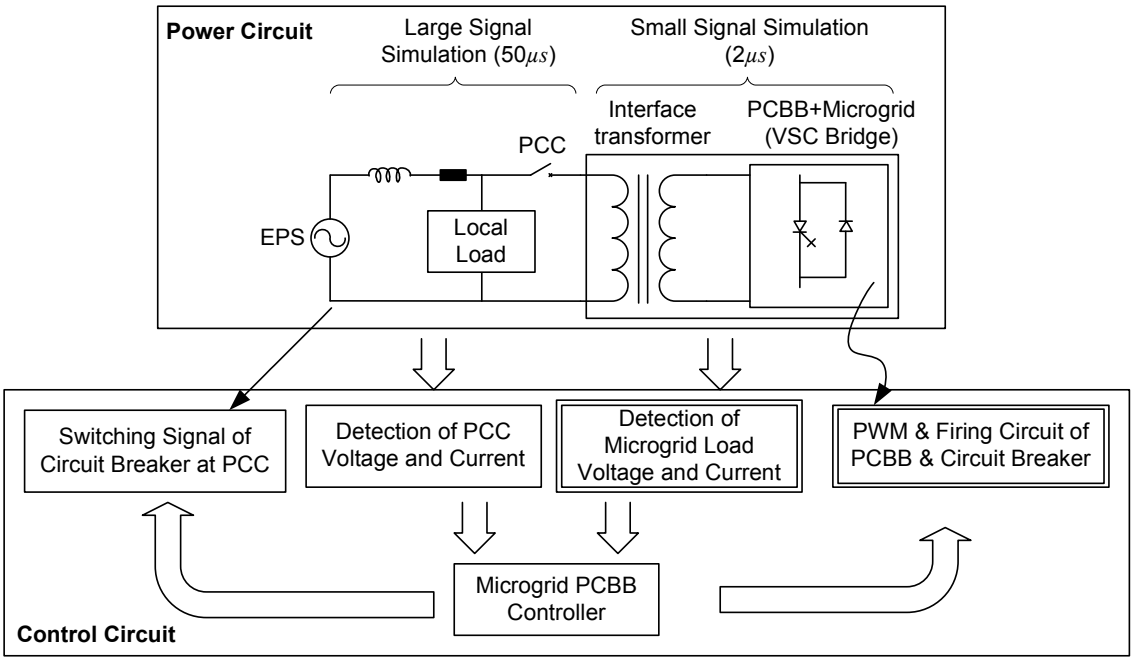


Figure 2.29: Implementation of Digital Controlled PCBB in RSCAD

powerful parallel processors, which are able to simulate the complex power circuit in real time. The gigahertz processor card (GPC) allows $1.4\mu s \sim 2.5\mu s$ small step simulation [78]. With the powerful processor, high frequency switching devices are able to be simulated with detailed models in real time.

Fig. 2.29 shows how to implement the proposed circuit and control strategies in RSCAD. The high frequency switching devices, such as PCBB and nonlinear load in microgrid are simulated in small time step, $2\mu s$. The rest components and control circuits are simulated in large time step, $50\mu s$. To interface the two parts simulated in different time scale, interface transformer models provided in RSCAD are embedded in between.

Fig. 2.30 shows two sets of real time simulation results of three phase PCBB connecting microgrid to EPS. In the first set transient simulation, as shown in Fig.

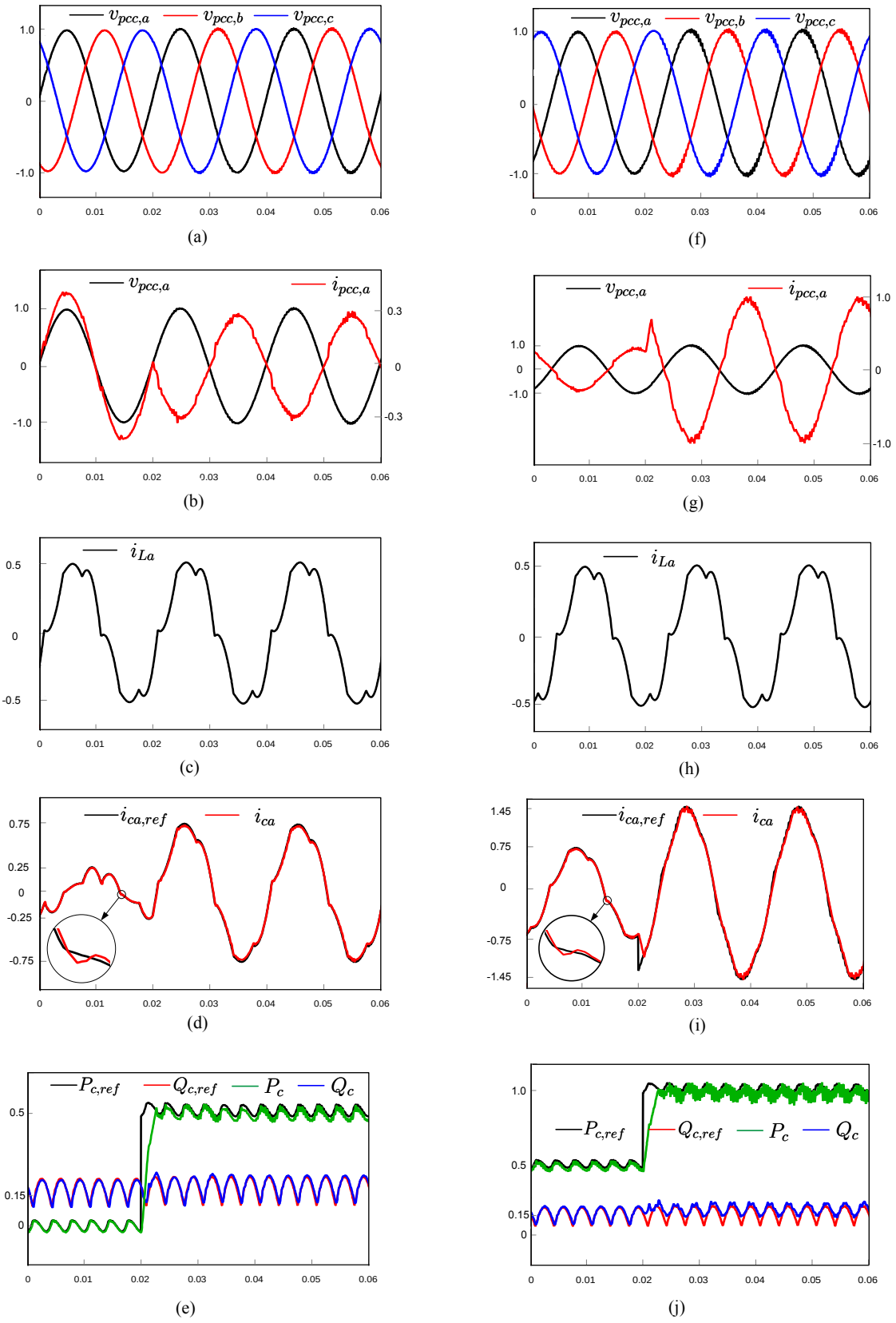


Figure 2.30: The Real Time Simulation Results of Proposed Combined Active and Reactive Power Control of PCBB: (a) PCC voltage, (b) PCC voltage and current of Phase A, (c)load current of Phase A, (d)current reference and actual output current of shunt PCBB, (e) the power reference and actual power output of shunt PCBB when microgrid transits from reactive power compensation to combined active power generation and reactive power compensation; (f)-(j) are the same measured variables when microgrid steps up 50% of the active power generation.

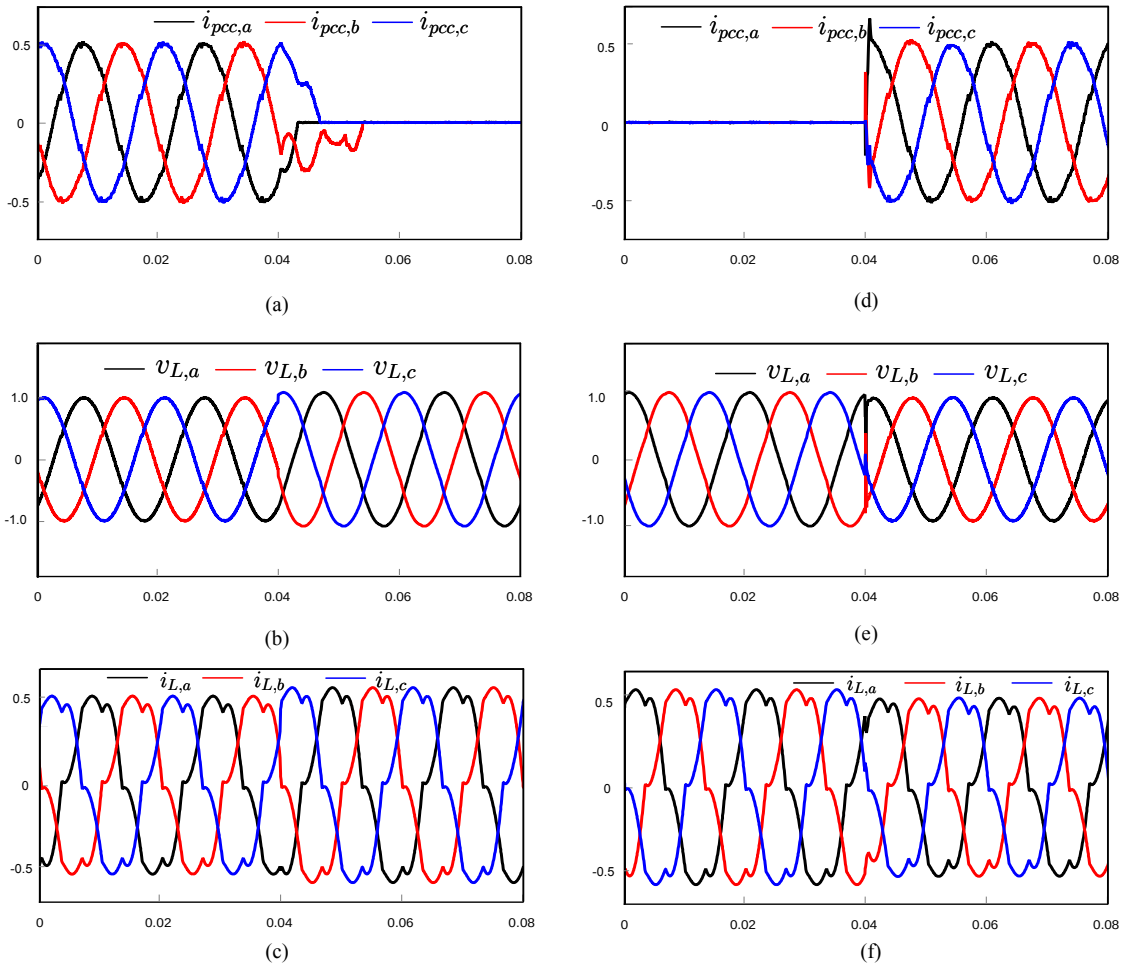


Figure 2.31: The Real Time Simulation Results of Microgrid Transitioning between EPS Connection Operation and Islanding Operation: (a) PCC current, (b) Load Voltage, (c)load current when microgrid transits from EPS connected operation mode to islanding mode; (d)-(f) are the same waveforms captured when microgrid transits back from islanding mode to EPS connected operation mode

2.30.(a)-(e), the PCBB first serves as active power filter to compensate the reactive power of load, then supplies power to both microgrid and EPS. Fig. 2.31.(f)-(j) show the transient simulation results when the active power output from PCBB doubles. With the reactive power compensation by shunt PCBB, the total demand distortion of current at PCC is 2.98%, within the 5% limit of IEEE 519 Std and IEEE 1547 Std. Fig. 2.31 shows the transient simulation results of PCBB changes between EPS connected operation mode and islanding operation mode. The PCBB changes between current control mode and voltage control mode. The simulation results demonstrate the capability of the proposed control strategy in smoothly transitioning the microgrid between different operating scenarios.

2.5 Summary

In this chapter, a multifunctional power converter building block is proposed to interface the microgrid to EPS. With the proposed combined active and reactive power control scheme, the microgrid is able to function normally regardless of the condition of Area EPS. Moreover, the PCBB can not only compensate the current harmonics produced by the nonlinear loads, but also provide active power to both load and Area EPS by exploiting the renewable sources and energy storage inside microgrid. Stability and robustness of the proposed control system is proved. Both offline and real time digital simulation results verify the effectiveness of the control strategies.

Chapter 3

Fault Ride Through Ability Enhancement of High Power Microgrid

3.1 Introduction

To enable the distributed generators inside microgrid to ride through low voltage fault of electric power system (EPS), this chapter proposes digital controlled power converter building block (PCBB). When EPS experiences fault and microgrid is feeding power toward it, the proposed control system will limit the output current of PCBB to avoid tripping off and thermal breakdown. Moreover, the proposed control scheme enables the PCBB to maintain smooth power injection when EPS has asymmetrical fault and negative sequence voltage component. Once the fault is cleared, PCBB returns to normal operation to continue feeding the same power as prefault to avoid network instability. Both simulation and experimental results are provided to validate the proposed fault ride-through scheme of microgrid.

3.2 Introduction to Fault Ride Through of Microgrid

As a distributed power system connected to area electric power system, microgrid has the ability to operate in both grid connected mode and islanding mode. When microgrid is in grid connected operation mode and microgrid central controller detects EPS has fault, the static switch at PCC opens and the system becomes an autonomous power island. Such protection measure ensures the continuous normal operation of microgrid, especially the critical load. However, if the fault happens when microgrid is injecting considerable power to EPS, tripping off microgrid and transitioning it to islanding mode will cause massive generation loss and instability issues to the power network.

As shown in Fig. 3.1, microgrid consists of various types of distributed generators, such as solar generators, microturbines, diesel generators, etc. For example, if one microgrid has ten 500kW diesel generators, the net generation capacity will amount to 5MW. Tripping off microgrid when it is injecting such amount of power to EPS is likely to introduce instability. Currently, most small DGs like diesel generators do not have fault ride-through capability. Therefore, enhancing the fault ride-through (FRT) capability of microgrid is important, especially for high power microgrid connected to EPS.

Instead of providing FRT capability to every single DG inside microgrid, this

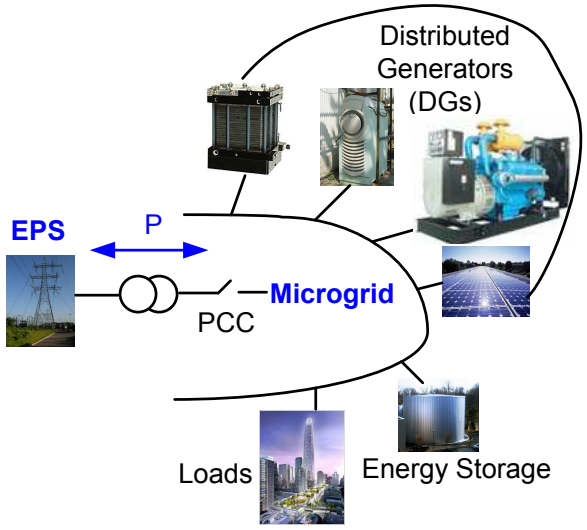


Figure 3.1: General Architecture of Grid Connected Microgrid

chapter chooses to enhance the microgrid FRT capability at PCC. In [79], a series interfacing inverter is proposed to compensate the voltage dip up to 30% of nominal voltage to enhance the FRT of microgrid. However, for fault which dips the voltage at PCC beyond 30%, the strategy is not able to achieve fault ride-through.

Along with FRT, fault current limitation is another important requirement for all DGs at distribution level [80]. Many distributed generators are interfaced by inverters. The limited short-circuit capability of inverters requires the solution proposed for FRT to achieve fault current limitation as well. FRT has been proposed for high power wind and PV generation systems [81]. All the control strategies available to DGs are listed and compared in [82] and [83]. However, fault current limitation has not been addressed. In this chapter, we will compare the different control strategies from fault current limitation requirement aspect.

The fault happening to EPS can be classified into symmetrical fault and

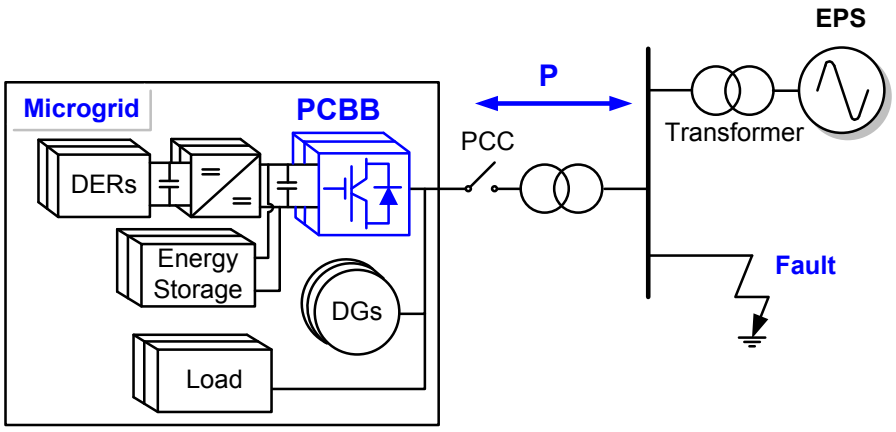


Figure 3.2: Single Line Diagram of Microgrid under EPS Fault

asymmetrical fault. Compared with symmetrical fault, asymmetrical fault will introduce negative sequence component to voltage at PCC. Under such unbalanced condition, instantaneous active power reactive power theory [36] can still be used to calculate the power at PCC. Symmetrical component theory [84] is another classic way of calculating power especially for unbalanced electric system. Compared with instantaneous P&Q theory, though more computation intensive, symmetrical component method provides a way to extract the negative sequence component of the current, i^n. Through compensating i^n, the output current of inverter can be maintained sinusoidal during asymmetrical fault. Although compensating the negative sequence component greatly improves the power quality during fault, the power pulsation introduced not only stresses the DC link capacitor but also risks network stability. In addition, compensating the negative sequence component poses more stringent requirement on fault current limitation. Both the instantaneous P&Q theory and symmetrical component theory will be addressed with details in the following sections.

3.3 Comparison of Fault Ride-through Strategies

The power flow from microgrid to EPS at PCC is defined as:

$$\begin{aligned} P &= \mathbf{v}\cdot\mathbf{i} = [v_a \quad v_b \quad v_c]^T \cdot [i_a \quad i_b \quad i_c] \\ &= v_a i_a + v_b i_b + v_c i_c \end{aligned} \tag{3.1}$$

$$\begin{aligned} Q &= \mathbf{v}\perp\cdot\mathbf{i} = [v_a \quad v_b \quad v_c]_\perp \cdot [i_a \quad i_b \quad i_c] \\ &= \frac{1}{\sqrt{3}}[(v_a - v_b)i_c + (v_b - v_c)i_a + (v_c - v_a)i_b] \end{aligned} \tag{3.2}$$

where $\mathbf{v} = [v_a \quad v_b \quad v_c]$ is the voltage vector at PCC and $\mathbf{i} = [i_a \quad i_b \quad i_c]$ is the current vector at PCC. The equations above hold during both normal and fault conditions. However, when fault happens, the voltage vector at PCC will contain both positive sequence and negative sequence components. In order to analyze the effect of negative sequence component to power flow equations, symmetrical component analysis method is used here [84]. The power flow equations (3.1), (3.2) become

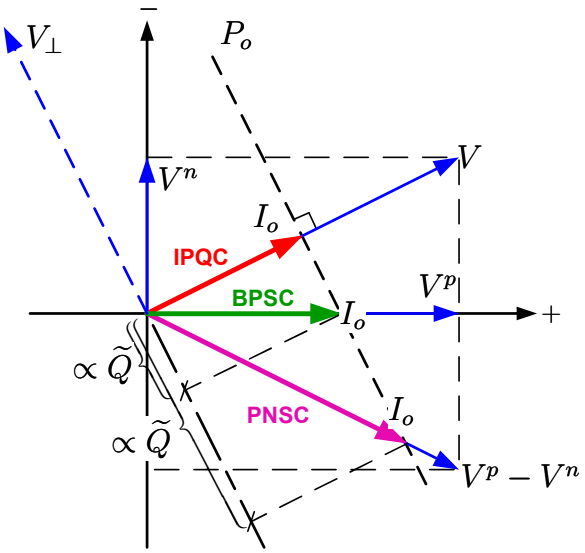
$$P = \mathbf{v}\cdot\mathbf{i} = (v^p + v^n)\cdot(i^p + i^n) = \overline{P} + \widetilde{P} \tag{3.3}$$

$$Q = \mathbf{v}_\perp\cdot\mathbf{i} = (v^p_\perp + v^n_\perp)\cdot(i^p + i^n) = \overline{Q} + \widetilde{Q} \tag{3.4}$$

$$\widetilde{P} = v^n i^p + v^p i^n \tag{3.5}$$

$$\widetilde{Q} = v^n_\perp i^p + v^p_\perp i^n \tag{3.6}$$

where v^p and v^n are the positive and negative sequence components of the voltage vector; $\overline{P}$ and $\overline{Q}$ are the constant active and reactive power; $\widetilde{P}$ and $\widetilde{Q}$ are the 2^{nd}



- IPQC: Instantaneous Power Control Method
- BPSC: Balanced Positive Sequence Control Method
- PNSC: Positive and Negative Sequence Control Method

Figure 3.3: Different Methods of Current Reference Calculation for PCBB Under EPS Fault

order oscillating powers caused by the negative sequence component in the reactive current. The two components of $\widetilde{P}$ and $\widetilde{Q}$ are in phase quantities oscillating at twice the fundamental grid frequency. Here, the zero sequence components are assumed zero.

Fig. 3.3 shows the voltage and current vectors under asymmetrical fault conditions. As shown in the figure, to regulate the output current of PCBB under asymmetrical conditions, we could choose to align the current vectors with the PCC voltage vector (IPQC [36]), postive sequence of the voltage vector (BPSC [82], [83]), or the difference vector of the positive and negative sequence components

(PNSC [84]). As Fig. 3.3 shows, IPQC aligns the current vector with the voltage vector. Therefore, the power pulsation (3.5), (3.6) is mitigated when EPS voltage is unbalanced and has negative sequence component.

The maximum allowed pulsating power for the voltage source inverter system is

$$\widetilde{P}_{pk} = \omega_1 V_{dc} C_{dc} \Delta v_{dc} \tag{3.7}$$

where ω_1 is the fundamental angular frequency, V_{dc} is the average DC link voltage, C_{dc} is the DC link capacitance and Δv_{dc} is the maximum allowed DC link voltage variation. Since BPSC and PNSC will generate power pulsation and the inverter system allows limited pulsating power output, under unbalanced voltage conditions, the power injected from microgrid to EPS is reduced compared with IPQC scheme. Therefore IPQC is competitive in limiting fault current and maintaining system stability especially under severe fault conditions.

The most severe prefault case is when the microgrid is injecting full power to EPS. As shown in Fig. 3.3, the minimum amplitude of the voltage vector of instantaneous power control is $|V|$. For balanced positive sequence control, it is the amplitude of the positive sequence voltage $|v^p|$. While for positive and negative sequence control method, the minimum amplitude of the voltage vector is the difference between the positive sequence component v^p and negative sequence component v^n, $|v^p| - |v^n|$. (3.8)-(3.10) provide the maximum output currents of PCBB under the three different control schemes.

$$I_{max,IPQC} = \frac{P_{inv}}{3/2|V|} \tag{3.8}$$

$$I_{max,BPSC} = \frac{P_{inv}}{3/2|V^p|} \tag{3.9}$$

$$I_{max,PNSC} = \frac{P_{inv}}{3/2|V^p| - |V^n|} \tag{3.10}$$

The maximum current output of PCBB must be within the maximum current limitation of the inverter, normally 1.5 times nominal value. We can conclude that for same level of current limitation, IPQC will inject the highest power level among the three methods. Therefore, the power drop during fault will be the smallest, which is desirable in maintaining network stability.

One weakness with IPQC compared to BPSC and PNQC is the output current distortion under unbalanced voltage conditions. However, the grid codes of the FRT requirement for interconnecting DGs do not pose a limit on the current quality during fault [28]. The circuit breakers trip based on the RMS sensing of the current. Therefore, all three control strategies will satisfy the requirement of maintaining PCBB connected during the fault as long as the over current limitation algorithms are installed. To enhance the ride-through capability and maintain system stability under grid fault conditions, reducing power variation and drop is more essential. Therefore, IPQC is preferred over the other two control strategies. In addition, IPQC reduces computation complexity since it does not require the sequence components extraction. The next part will present the details of applying IPQC to PCBB to achieve fault ride-through of microgrid.

3.4 Proposed Control Strategy for PCBB to Achieve FRT and FCL

3.4.1 Modeling of Electric Power System and Interface Transformer

As shown in Fig. 3.2, microgrid connects to the distribution power system through interface transformer. Instead of modeling the electric power system as an ideal sinusoidal voltage sources, detailed modeling of the electric power system will give a more accurate evaluation of the proposed control scheme. Additionally, with the models of the electric power system and isolation transformer, the relation between effect of EPS fault and voltage at PCC can be investigated.

Fig. 3.4 shows the hierarchical power system architecture. Microgrid is supposed to be connected to the distribution system busbar. As shown in the figure, the complex architecture can be simplified to the Thevenin equivalent circuit. With the knowledge of the short circuit fault level, the fault impedance can be calculated following 3.11, 3.12.

$$Z_{HV} = \frac{V_{HV}^2}{S_{SC}} \tag{3.11}$$

$$Z_{LV} = \frac{V_{LV}^2}{V_{HV}^2} Z_{HV} \tag{3.12}$$

where S_{SC} is the short circuit power level the connected EPS; Z_{LV} is the equivalent

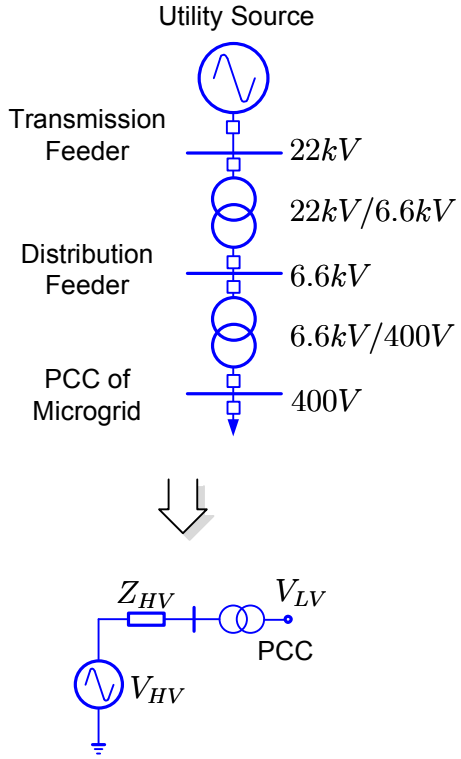


Figure 3.4: Power System Architecture and Simplified Model

Table 3.1: Short Circuit Impedance Value at Different Grid Capacities

Short Circuit Power (kW)	Resistance (pu)	Inductance (pu)
20,000	0.001	0.003
10,000	0.002	0.0059
5,000	0.0039	0.0118
1,000	0.0197	0.0592
500	0.0395	0.1185

impedance at the low voltage side. The short circuit impedance values for different grid capacities are listed in Table 3.1 [85], [86].

Fig. 3.5 displays the isolation transformer model and the equivalent EPS model at PCC, where L_i' is the grid inductance; L_l' is the transformer leakage inductance; L_g' is the total effective grid inductance at transformer high voltage side; V_g and L_g are the equivalent grid voltage and grid inductance at the transformer low voltage side. (3.13)-(3.15) give the relationship among the variables.

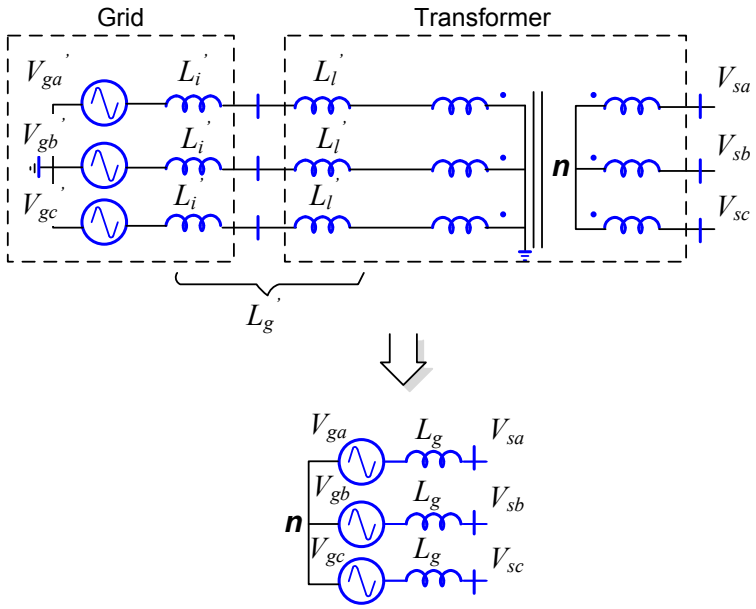


Figure 3.5: Modeling of the grid voltage and impedance at PCC

$$V_{g,abc} = \frac{1}{N} V'_{g,abc} \tag{3.13}$$

$$L'_g = L'_i + L'_l \tag{3.14}$$

$$L_g = \frac{L'_g}{N^2} \tag{3.15}$$

3.4.2 Proposed Control Scheme for PCBB to Enable Fault Ride-through of Microgrid

Fig. 3.6 shows the control scheme applied to PCBB. Instantaneous P&Q theory is used to calculate the current reference for the control system [36]. Applying clarke transformation to the voltage vector and current vector at PCC,

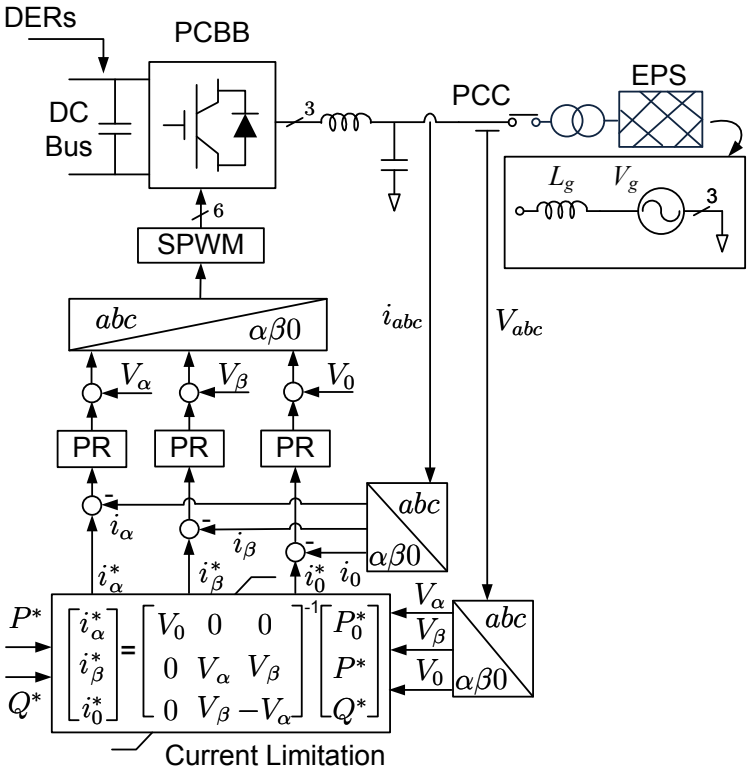


Figure 3.6: Proposed Control Scheme for PCBB

$$v_{\alpha\beta 0} = \mathbf{T} v_{abc} \tag{3.16}$$

$$i_{\alpha\beta 0} = \mathbf{T} i_{abc} \tag{3.17}$$

$$\mathbf{T} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{3.18}$$

The instantaneous active and reactive power in $\alpha\beta 0$ coordinate become:

$$\begin{bmatrix} P_0 \\ P \\ Q \end{bmatrix} = \begin{bmatrix} v_0 & 0 & 0 \\ 0 & v_\alpha & v_\beta \\ 0 & v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} \tag{3.19}$$

Therefore, the current reference in $\alpha\beta 0$ coordinate is derived as:

$$\begin{bmatrix} i^*_\alpha \\ i^*_\beta \\ i^*_0 \end{bmatrix} = \begin{bmatrix} v_0 & 0 & 0 \\ 0 & v_\alpha & v_\beta \\ 0 & v_\beta & -v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} P^*_0 \\ P^* \\ Q^* \end{bmatrix} \tag{3.20}$$

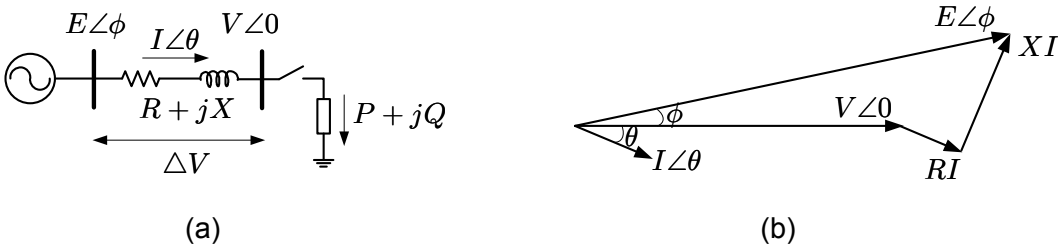


Figure 3.7: Voltage Sag Analysis Diagram: (a) The Simplified Circuit Diagram between Microgrid and EPS; (b) System Phasor Diagram [10]

(3.20) indicates the active and reactive power can be selectively compensated. During normal operation, the reactive power reference should be set to zero to maintain the power quality and unity power factor at PCC. However, during fault recovery period, reactive power could be injected to provide voltage support at PCC.

Fig. 3.7 illustrates the voltage relationship between microgrid and EPS, when microgrid is injecting power to EPS. In Fig. 3.7.(a), $E\angle\phi$ is the voltage of microgrid; $V\angle 0$ is the voltage of EPS; $I\angle\theta$ is the current injected from microgrid to EPS; $R+jX$ is the line impedance; $P+jQ$ is the power injected from microgrid to EPS; $\triangle V$ is the voltage difference between microgrid and EPS.

According to Fig. 3.7.(b), the relationship between the different quantities can be derived as follows:

$$\begin{aligned} E^2 &= (V + RIcos\theta + XIsin\theta)^2 + (XIcos\theta - RIsin\theta)^2 \\ &= (V + RIcos\theta + XIsin\theta)^2 \end{aligned} \tag{3.21}$$

If we neglected the harmonic content in voltage and current,

$$\begin{aligned} P &= VIcos\theta \\ Q &= VIsin\theta \end{aligned} \tag{3.22}$$

Substituting (3.22) into (3.21),

$$E = V + (\frac{RP}{V} + \frac{XQ}{V}) \tag{3.23}$$

Therefore, the difference voltage $\triangle V$ is achieved as

$$\triangle V = E - V = \frac{RP}{V} + \frac{XQ}{V} \tag{3.24}$$

(3.24) shows the voltage dip is related to both active power and reactive power. At transmission level, where X is much greater than R, the voltage dip is closely related to reactive power. Therefore, most grid codes on fault ride through at medium voltage level put reactive power compensation as the first priority [23]-[28]. However, at distribution system level and low voltage level, where X is not much greater than R, or even lower than R, the voltage dip is related to both reactive power and active power. The distribution code requires the inverter interfaced distributed generators to maintain active power support during fault [30], [87]. In the mean time, reactive power output is maximized within the constraints of the inverter power rating, fault magnitude and duration. Since microgrid is connected

at the distribution level, the fault ride through requirement from distribution code [30] is followed in this thesis. The active power is maintained as porportional to the voltage level, and reactive power is maintained maximum within the converter constraint.

3.4.3 Controller Design

PR controllers are designed for PCBB to track the reference current following the procedures in Chapter II. Voltage feedforward is added to improve dynamic performance and disturbance rejection. (3.8) is implemented to limit the fault current.

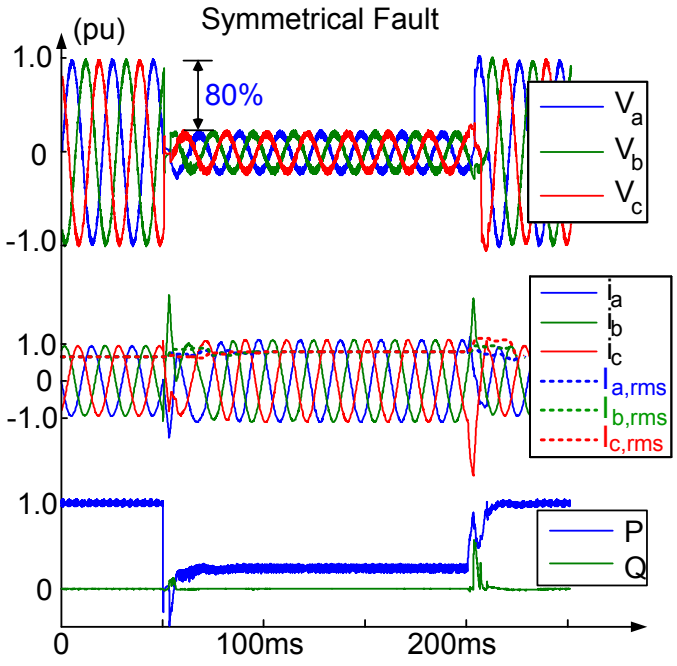


Figure 3.8: Simulation Result of PCBB Riding Through Symmetrical Low Voltage Fault

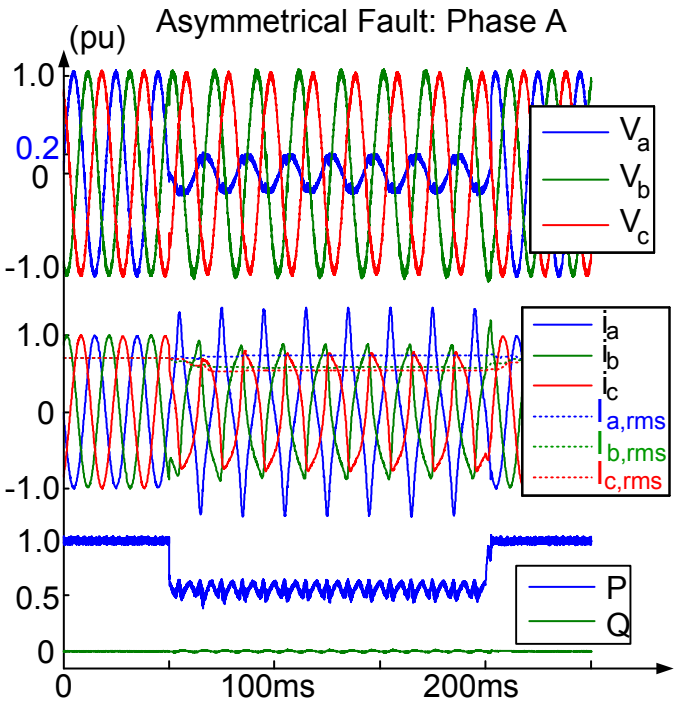


Figure 3.9: Simulation Results of PCBB Riding Through Asymmetrical Low Voltage Fault

3.5 Simulation Results

To validate the proposed control strategy in fault ride-through and fault current limitation, the system under both symmetrical and asymmetrical fault are simulated. Fig. 3.8 and Fig. 3.9 show the output power and currents of PCBB under symmetrical and asymmetrical fault when PCBB is exporting full power. As shown in the simulation results, during the fault, the RMS values of the currents shown by the dashlines do not go beyond the nominal values. The active or reactive power have no second order oscillations during both symmetrical and asymmetrical fault.

3.6 Experimental Results

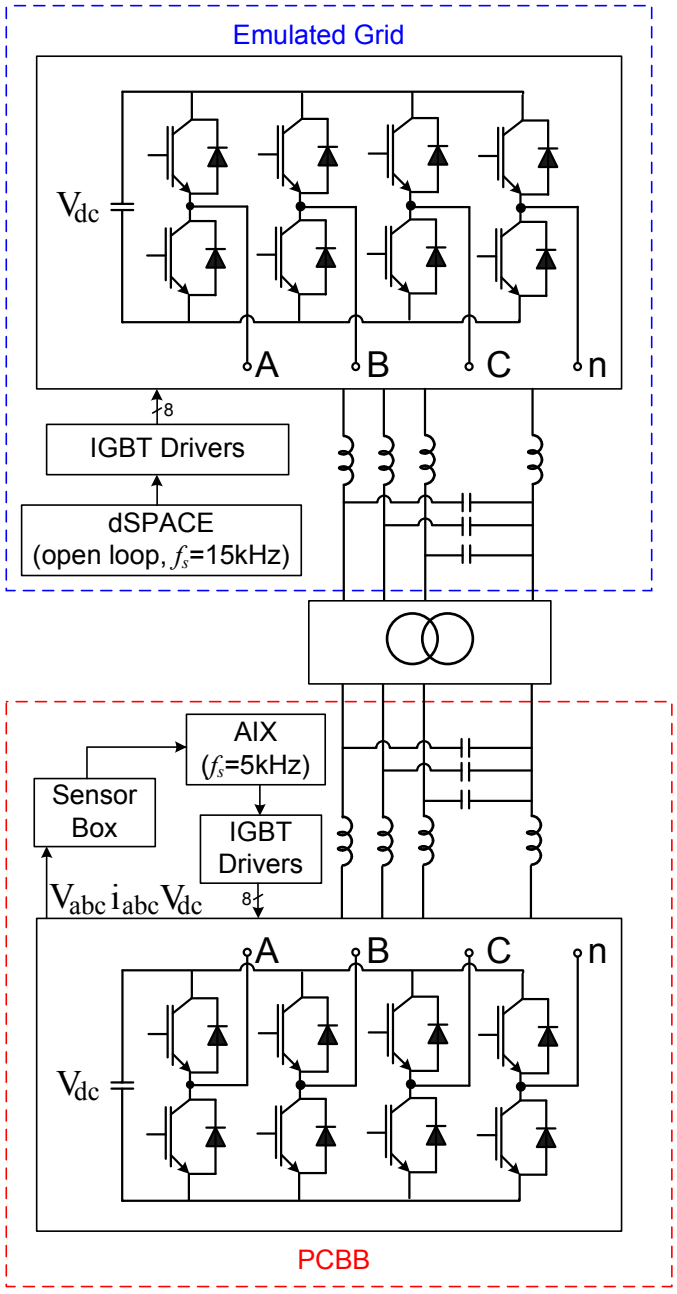


Figure 3.10: Block Diagram of the Laboratory Prototype

The proposed FRT scheme is experimentally tested on a laboratory setup. The setup include three major components, the grid emulator, the tested PCBB hardware and PCBB digital control system. Fig. 3.10 shows the block diagram of

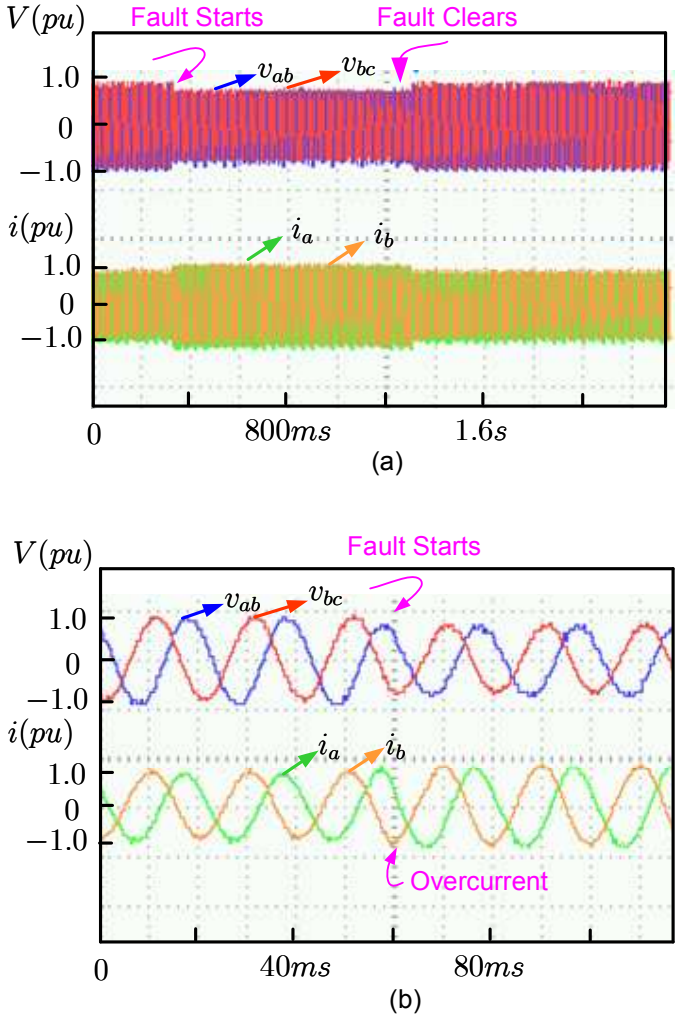


Figure 3.11: When EPS Has Balanced Fault and PCBB Has no FRT Capability: (a) PCC Voltage and PCBB Output Current; (b) Large Time Duration Display

the experimental setup. The grid emulator is a three phase VSI system, designed specifically to test grid connected converter systems. It can produce a variable frequency, variable magnitude three phase voltage output and can be programmed to simulate voltage dips and fault. The proposed control scheme for PCBB is implemented with AIX DSP control system [88]. The DC input of the PCBB is emulated by a diode rectified AC.

Fig. 3.11 shows the PCBB output current when EPS has balanced fault.

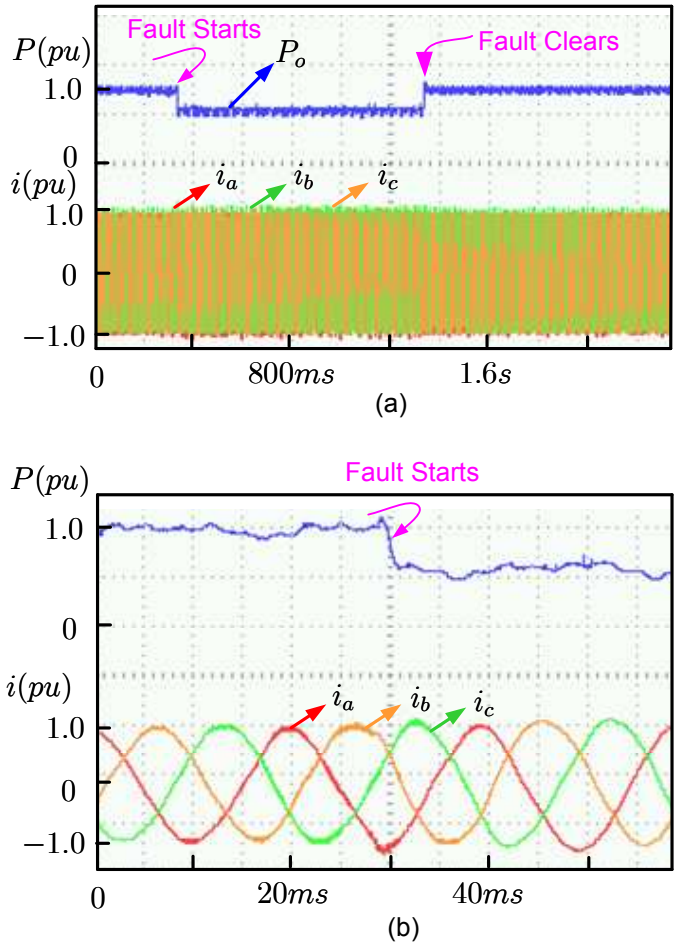


Figure 3.12: When EPS Has Balanced Fault and PCBB Has FRT Capability: (a) PCBB Output Power and Output Current; (b) Large Time Duration Display

Without fault current limitation, the output current will go beyond the limit when PCBB is injecting full power to EPS before fault happens. Fig. 3.12 and Fig. 3.13 demonstrate the dynamic response of the proposed control scheme of PCBB under both balanced and unbalanced fault conditions. With the proposed FRT scheme, the output current of PCBB will be kept below limit during fault conditions and PCBB maintains smooth power injection to EPS during fault. The experimental results show the proposed scheme successfully achieves fault ride-through.

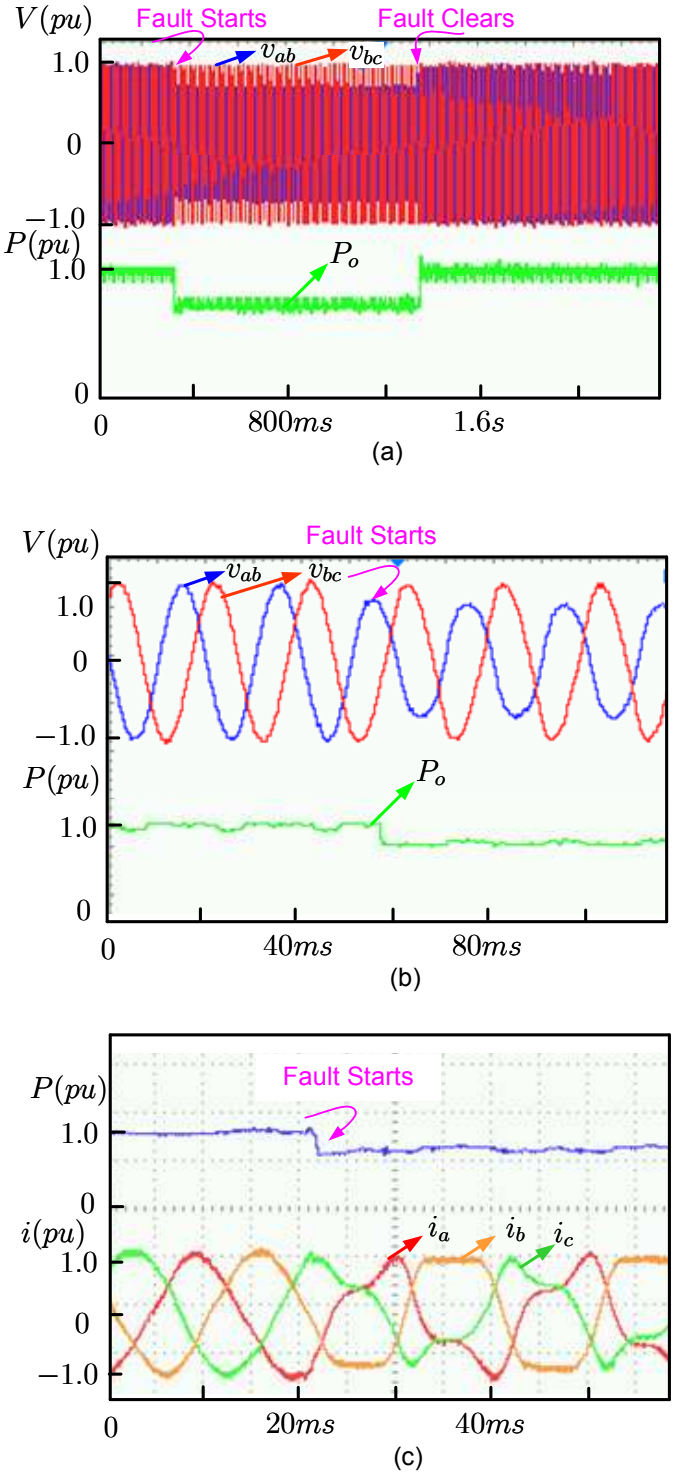


Figure 3.13: When EPS Has Unbalanced Fault and PCBB Has FRT Capability: (a) PCC Voltage and PCBB Output Power; (b) Large Time Duration Display; (c) PCBB Output Power and Output Current

3.7 Summary

A control strategy is proposed for the microgrid interfacing inverter (PCBB) to facilitate the low voltage fault ride-through when microgrid is injecting a considerable amount of power to EPS. As demonstrated by the simulation results, the proposed control strategy enables the PCBB to maintain smooth power injection to EPS without exceeding the current limit when symmetrical or asymmetrical fault happens to EPS. Compared with other FRT strategies, the proposed scheme does not require complex calculations and achieves both fault ride-through and fault current limitation. In addition, the instantaneous power control strategy achieves minimal power variation and power drop during fault. Both simulation and experimental results are provided to validate the proposed control scheme.

Chapter 4

Dynamic Power Distribution for Parallel PCBB Operation

4.1 Introduction

As the power level of microgrid increases, the power rating of PCBB must be increased as well to accommodate the increased power to be processed. To expand the system power level, multiple interfacing inverters could be paralleled to feed the local load with power from DGs and ESS. The size and number of the power inverters required will depend on the fluctuating power flow within microgrid. The multiple paralleled interfacing inverters can be implemented by modular Power electronics building blocks (PEBBs) [89]. PEBB is a plug-n-play power electronics module with both networking and stand-alone functionality. By using such modular standardized components, production costs, design and testing time can be reduced [90]. Fig. 4.1 shows the H-Bridge topology, one fundamental structure of PEBB.

When microgrid is operated under heavy load condition, parallel inverters

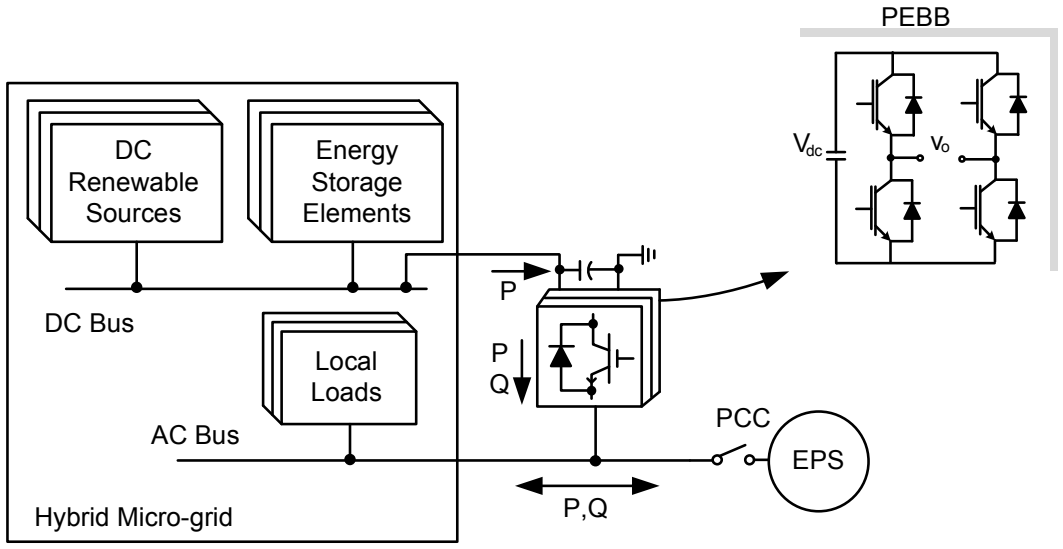


Figure 4.1: Hybrid Micro-grid with PEBB based Power Conversion System

equally share the power demand. As shown in Fig. 4.1, when microgrid is operating in grid following mode, the voltage at PCC is decided by EPS. The inverters are regulated in current control mode to provide the active and reactive power required. Therefore, by equally distributing the reference current to the controller of each inverter, power balance can be achieved. When microgrid is operating in grid forming mode, i.e. islanding mode, the parallel inverters should form the voltage supply for the local load. Under such condition, the inverters work in voltage control mode. Without proper control strategy, current will circulate among the parallel inverters due to impedance mismatch. The circulating current might cause some inverters to be over thermal stressed and damaged.

Most research regarding parallel inverter control has been focused on equal power distribution and circulating current minimization. Little attention has been paid to control the paralleled inverters to improve system efficiency and thermal

profile. In this chapter, we propose a dynamic power distribution scheme for the parallel PEBBs to achieve system efficiency optimization. Instead of fixing the power sharing ratio of each PEBB to a static value, the control system will determine the power sharing ratio of each module in a dynamic fashion according to the load and thermal condition. When microgrid is operating under light load condition, instead of equally distributing the power demand among all the inverters, we propose a dynamic module dropping technique to improve the system efficiency at low load. In addition, time sharing scheme is also proposed for the paralleled inverter modules to improve the system thermal management. When microgrid is operating under heavy load situation, a simplified instantaneous error current correction strategy with cascaded proportional resonant (PR) derivative controller is proposed to equally distribute the power among paralleled inverters quickly and accurately.

4.2 Modeling and Control of Parallel Inverter System

Fig. 4.1 shows the general structure of a low voltage microgrid, which consists of renewable energy sources, energy storage, load and interfacing inverters. When the static switch at PCC opens, the microgrid transits to islanding mode operation. Under such operating scenario, the paralleled inverter modules should form a high quality voltage supply to sustain the load operation.

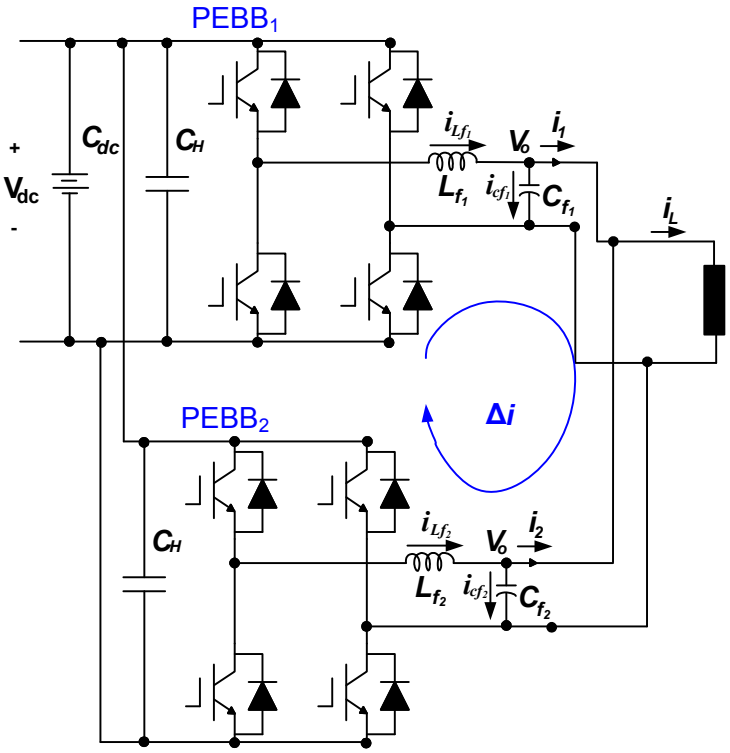


Figure 4.2: The Equivalent Circuit of Two Paralleled PEBBs with Linear Load in Islanded Microgrid

Table 4.1: Output Filters Parameter Setting of the Simulated Parallel PEBBs

L_{f_1}	C_{f_1}	L_{f_2}	C_{f_2}
0.2Ω $1mH$	$20\mu F$	0.4Ω $1.2mH$	$23\mu F$

Fig. 4.2 shows the equivalent circuit of a microgrid with linear load and two paralleled single-phase interfacing inverters.

Fig. 4.3 shows the voltage control system block diagram of each PEBB. The PEBB system transfer function is:

$$G(s) = \frac{1}{Ls+R}\frac{1}{Cs} = \frac{1/LC}{s(s+R/L)} \tag{4.1}$$

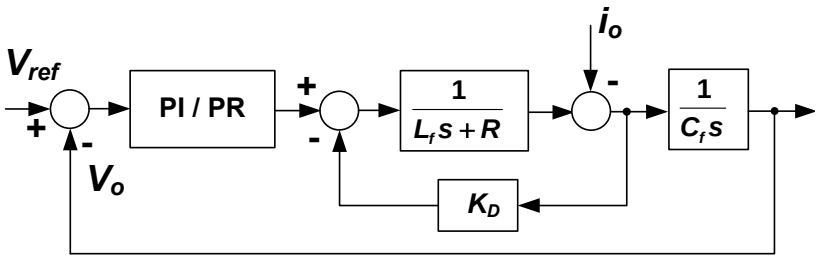


Figure 4.3: Block Diagram of Voltage Control System

First of all, pole placement method is used to design a common PID controller for the second order system. The PID controller transfer function is:

$$G_{PID}(s) = K_p(1 + \frac{1}{T_i s} + T_d s) = K_P + \frac{K_I}{s} + K_D s \tag{4.2}$$

The transfer function of the closed-loop system is derived as:

$$G_{cl}(s) = \frac{G(s)G_{PID}(s)}{1 + G(s)G_{PID}(s)} = \frac{\frac{1}{LC}(K_P s + K_I)}{s^3 + (\frac{R+K_D}{L})s^2 + \frac{K_P}{LC}s + \frac{K_I}{LC}} \tag{4.3}$$

Therefore, the characteristic equation is:

$$s^3 + (\frac{R + K_D}{L})s^2 + \frac{K_P}{LC}s + \frac{K_I}{LC} = 0 \tag{4.4}$$

With three controller parameters and a 3^{rd} order closed-loop system, the poles can be freely assigned. Using the (ξ, ω_n) parametrization, long with a 3^{rd} pole at $-a\omega_n$, we set the characteristic equation to be:

$$(s^2 + 2\xi\omega_n s + \omega_n^2)(s + a\omega_n) = s^3 + (2\xi + a)\omega_n s^2 + (2\xi a + 1)\omega_n^2 s + a\omega_n^3 \tag{4.5}$$

Here, we choose $\xi = 0.707$. With a switching frequency of 5kHz, the characteristic frequency is chosen to be 200Hz to ensure both the stability and fast dynamic response. To minimize the effect of the 3^{rd} pole to the system response and reduce the control design complexity, a is chosen to be 10 to place the 3^{rd} pole 10 times far away from the pair of conjugate poles. Comparing Eq. 4.4 and Eq. 4.5, the controller gains are yielded as:

$$K_P = LC(2\xi a + 1)\omega_n^2 \tag{4.6}$$

$$K_I = LCa\omega_n^3 \tag{4.7}$$

$$K_D = L(2\xi + a)\omega_n - R \tag{4.8}$$

Although the PID controller works well for second order system, it has difficulties in achieving asymptotic tracking and asymptotic regulation of the sine wave voltage reference as proved in Chapter II on page 39. Therefore, resonant controller [59], [47] replaces the integrator to achieve a high gain at 50Hz. The transfer function of PR controller is:

$$G_{PR}(s) = K_P + \frac{K_R s}{s^2 + \omega^2} \tag{4.9}$$

The parameter of the resonant controller K_R can be tuned following naslin polynomial approach [91], [59]. The frequency response comparison of 20 open loop system with PID controller and proportional resonant derivative controller is shown in Fig. 4.4. The resonant controller in the outer loop introduces a high gain

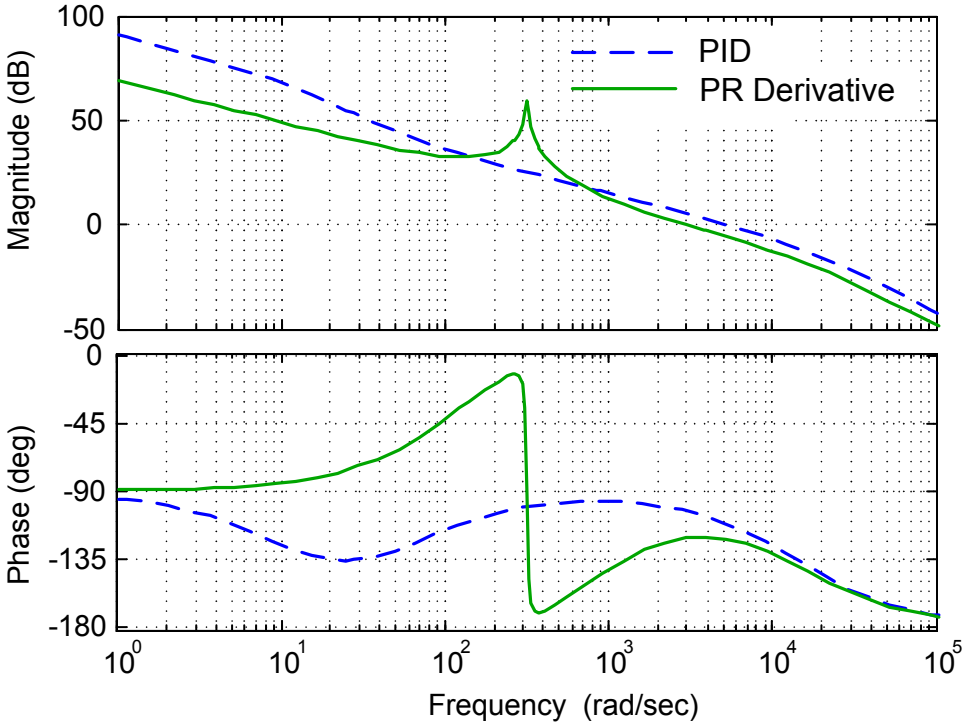


Figure 4.4: Frequency Response Comparison of the open loop system with PID controller and PRD controller

at the fundamental frequency as shown in Fig. 4.4. Accordingly, voltage tracking error in steady state will be minimized.

Although the output filter parameter of each PEBB is different, it is unrealistic to design the optimized proportional resonant derivative controller parameters for each PEBB control system separately. Here, we vary the system parameters R, L, C in the range of 50% and test the system robustness. Fig. 4.5 shows the bode plot of the open loop system with 50% parameter variation. The designed control system shows good robustness.

Fig. 4.6 shows the simulation results of two paralleled PEBBs feeding linear load in a microgrid with the proportional resonant derivative controller designed

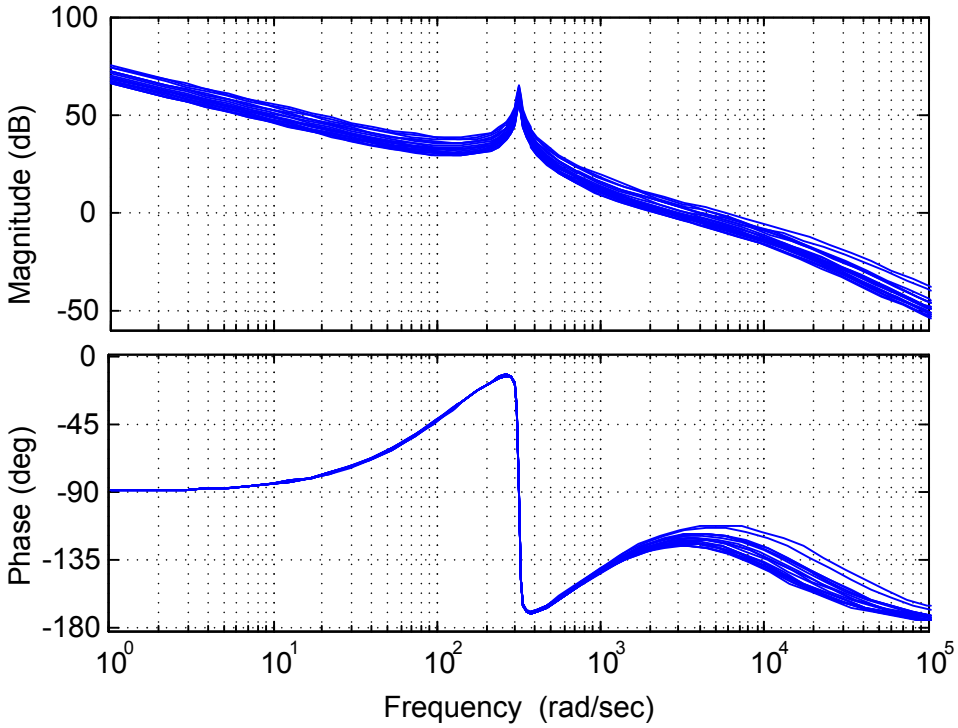


Figure 4.5: Bode plots of The Open Loop System with PRD controller When System Parameters (L, R, C) have 50% variation

above. The output filter parameters of the two PEBBs are shown in Table. 4.2. As Fig. 4.6 shows, though the output voltage is well regulated, circulating current flows between the two parallel modules owing to output impedance mismatch. The current circulation will lead to power unbalance between the paralleled PEBBs. Therefore, it might cause the output current of some modules to exceed the limit.

4.3 Literature Review of Circulating Current Minimization Techniques

The simplest way to balance the current among multiple paralleled voltage source inverters is to add power sharing inductors [92], [93] as shown in Fig. 4.7.

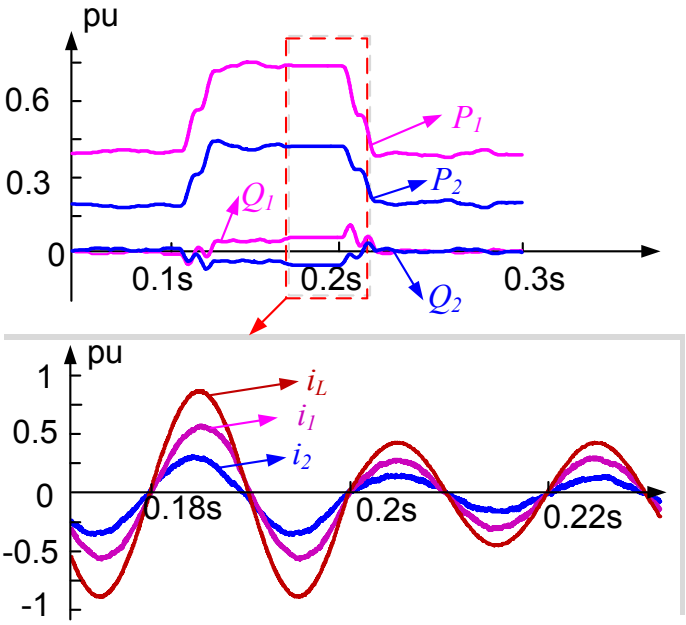


Figure 4.6: Simulation Results of System in Fig.4.2

The disadvantages of this method is that, in practice, the extra inductors will cause power loss and introduce delay and sag to the load end voltage. Moreover, the inductors will be very bulky in high power application.

Many control methods have been proposed to achieve equal power distribution for paralleled inverters system. As discussed in [94], the most popular methods are $f - P$ and $v - Q$ droop control, power deviation control and current minor loop control. The advantage for droop control [95]-[98] is its wireless feature and the disadvantage is slow dynamics. The resistive characteristics of low voltage microgrid line impedance makes droop control difficult to be applied to control the paralleled inverters of microgrid. Compared with droop control, the disadvantage with power deviation control [99], [100] and current minor loop control [101]-[105] is the information requirement for total load power or the output power of each inverter module; However, they will not disturb the frequency of the inverter output

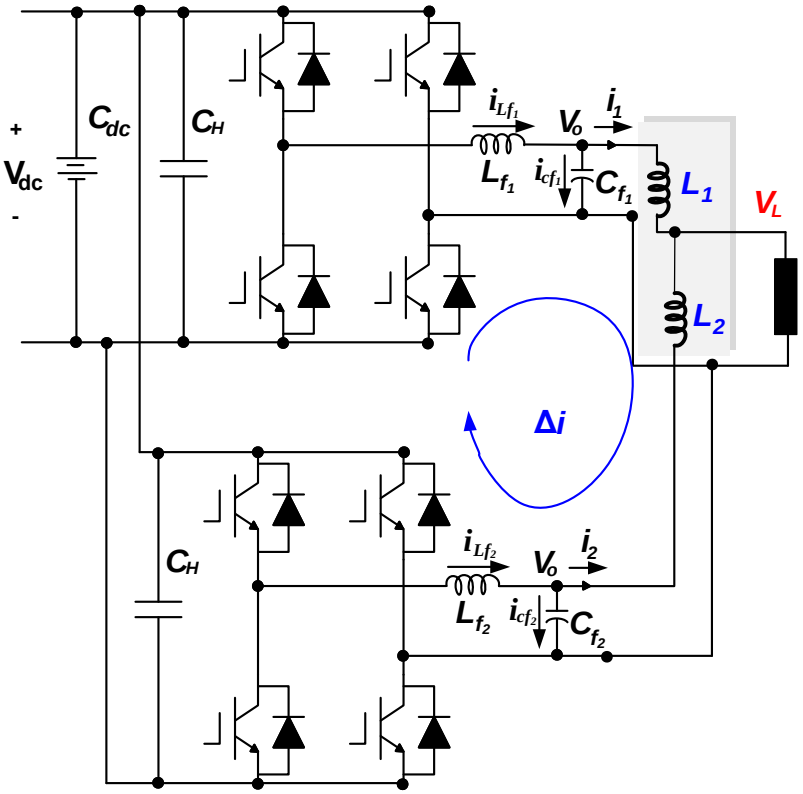


Figure 4.7: The Scheme of Adding Power Sharing Inductors to Balance Power among Paralleled Converters

voltage and offers better dynamic performance. Therefore, for distributed power system permitting control communication, current minor loop control is the most attractive option.

4.4 Proposed Instantaneous Error Current Correction Control

To minimize the circulating current among the paralleled PEBBs when they are feeding a microgrid with high load, an instantaneous error current correction control strategy is proposed, as shown in Fig. 4.8. To balance the power among

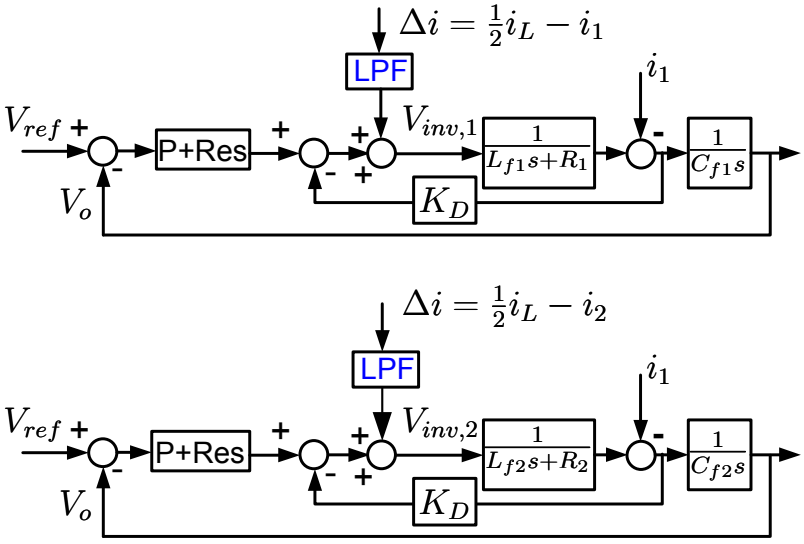


Figure 4.8: Proposed Instantaneous Error Current Correction Control Scheme

paralleled inverter modules, an additional error current compensation loop is introduced to the existing cascaded voltage control scheme. Because of the switching interference among multiple paralleled inverter modules, the inverter output current will contain amount of harmonics. These harmonics will affect the error current compensation performance. Therefore, instead of directly feeding the error current to the current minor loop, a low pass filter is introduced to remove the high order harmonics.

$$G_{LPF}(s) = \frac{K_{LPF}}{\frac{s}{\omega_c} + 1} \tag{4.10}$$

where ω_c is the cut off frequency.

The error current can be viewed as a disturbance to the voltage controlled system. Therefore, the low pass filter can be designed to enhance the disturbance rejection capability of the control system. According to Fig. 4.8, the close loop transfer function from disturbance to output without the low pass filter is derived

as follows:

$$G_{d1}(s) = \frac{\frac{\frac{1}{Ls+R}}{1+\frac{1}{Ls+R}K_D}\frac{1}{Cs}}{1+(K_P+\frac{K_R s}{s^2+\omega^2})(\frac{\frac{1}{Ls+R}}{1+\frac{1}{Ls+R}K_D}\frac{1}{Cs})} \tag{4.11}$$

With a low pass filter, the transfer function is transformed to:

$$G_{d2}(s) = \frac{\frac{K_{LPF}}{\frac{s}{\omega_c}+1}\frac{\frac{1}{Ls+R}}{1+\frac{1}{Ls+R}K_D}\frac{1}{Cs}}{1+(K_P+\frac{K_R s}{s^2+\omega^2})(\frac{\frac{1}{Ls+R}}{1+\frac{1}{Ls+R}K_D}\frac{1}{Cs})} \tag{4.12}$$

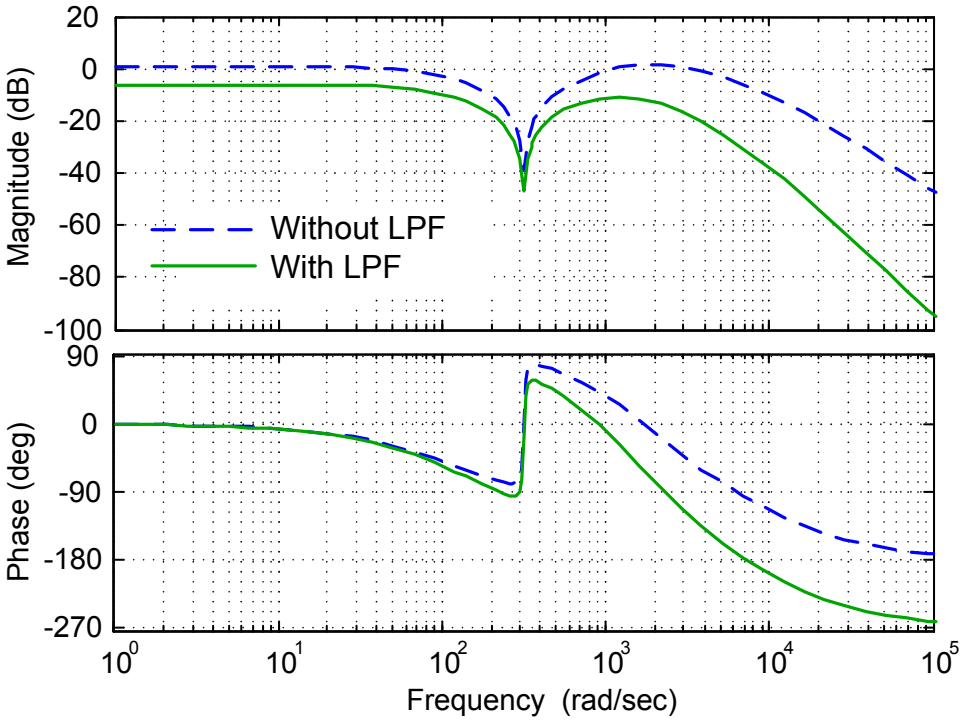


Figure 4.9: Frequency Response Comparison of the Close Loop System with and without LPF in Disturbance Transfer Function

Looking at the bode plot of $G_{d1}(s)$ shown in Fig. 4.9, the gain margin is beyond 0dB at low frequency. Therefore, the low pass filter should be designed to decrease the gain at low frequency. Here the cut-off frequency ω_n is designed to be 150Hz, near to the system characteristic frequency.

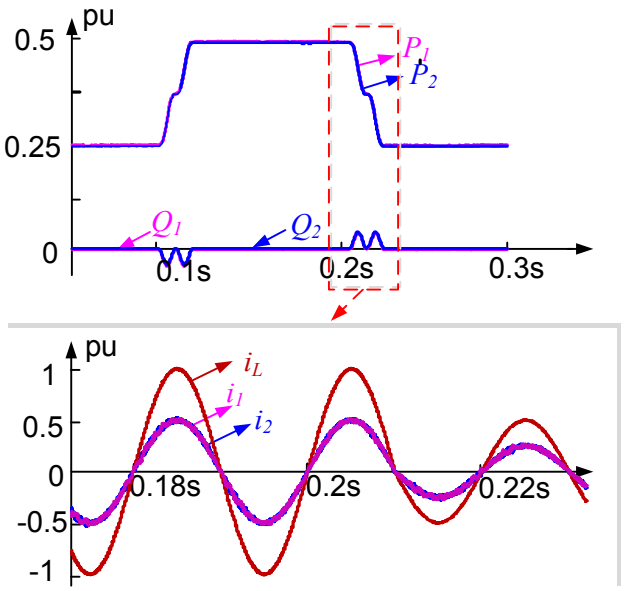


Figure 4.10: Simulation Results of System in Fig.4.2 with Proposed Error Current Correction Control Scheme in Fig.4.8

Fig. 4.10 and Fig. 4.11 show the simulation results of applying the proposed instantaneous error current correction scheme to the paralleled interfacing inverters in islanded microgrid with linear and nonlinear load. Compared to the results in Fig. 4.6, the power is equally distributed between the two paralleled PEBBs with impedance mismatch. Good steady state and dynamic performance are obtained.

4.5 Practical Implementation of Parallel Inverters with Error Current Correction Scheme

4.5.1 Conducted EMI Noise with Parallel Inverters

For inverters with isolated DC sources as shown in Fig. 4.12.(a), the proposed current sharing controller with limited bandwidth can minimize the circulating

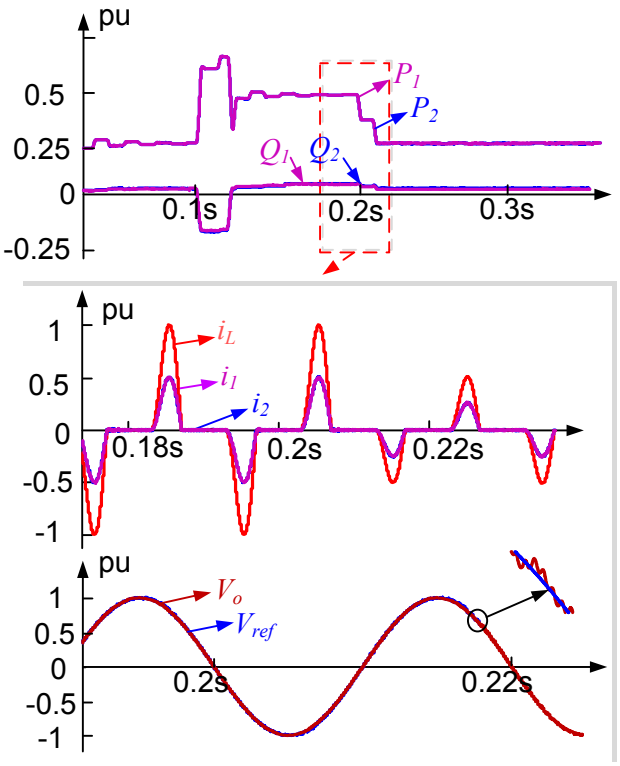


Figure 4.11: Simulation Results of Paralleled Inverters Feeding Nonlinear Load with Proposed Error Current Correction Control Scheme in Fig.4.8

current [106]. However, for inverters sharing common DC bus without output isolation as shown in Fig. 4.12.(b), the conducted noise current will also circulate between the parallel inverters as shown in Fig. 4.13. In addition, the mismatch between $L_{f_{11}}$ and $L'_{f_{11}}$ further increases the common mode conducted noise. The mismatched output impedance parameters of the two inverters are shown in table 4.2.

Such intensive noise current circulating between the two inverters are introduced by the fast switching of inverters. The rapid changing $\frac{di}{dt}$ and $\frac{dv}{dt}$ introduces conducted noise. The conducted noise current will flow through the two inverters as shon in Fig. 4.12.(a). The output LC filter will filter high frequency switch-

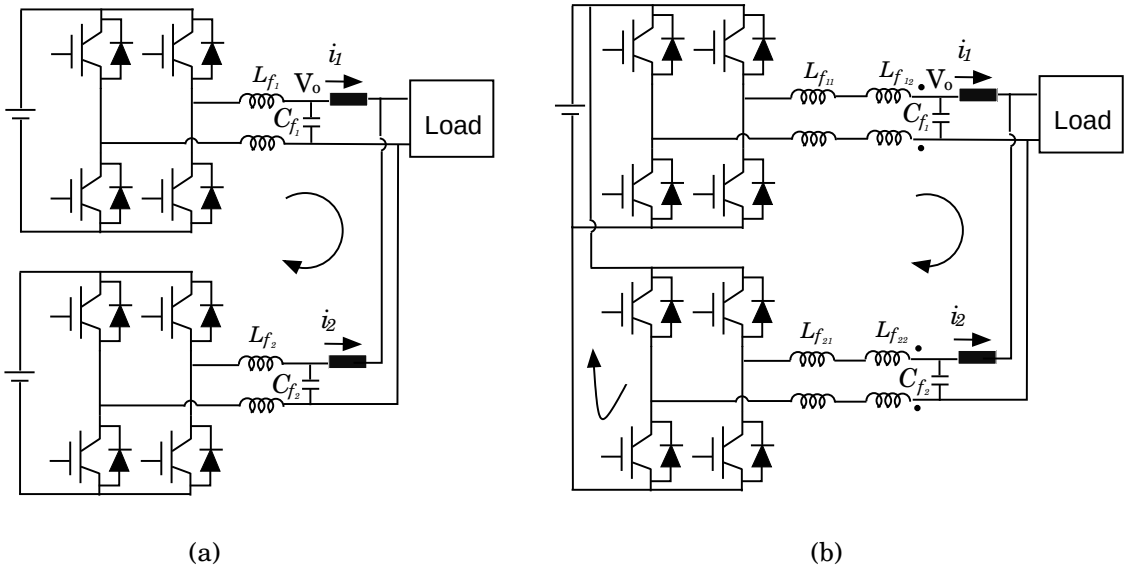


Figure 4.12: Two topologies of Parallel Connected Inverters: (a) Two inverters have independent DC source (b) Two inverters share the same DC link

ing harmonic current. However, residual current ripple and spikes will continue circulating among the inverters due to the non-ideality of the passive filters.

Interleaved modulation scheme facilities the differential mode noise further reduction. By synchronizing the paralleled inverters and aligning their modulation carrier waveforms with $\frac{360^\circ}{N}$ phase shift, the noise voltage can be reduced. However,

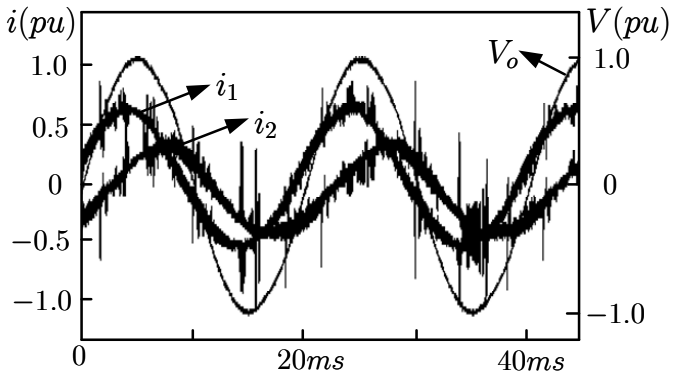


Figure 4.13: Experimental Results of the Unbalance Current Sharing between Two Parallel Inverters Without Isolation

any module failure incurs control scheme failure of all other modules in parallel. In addition, when system is to upgrade to higher power level, the control schemes for all other modules need to be updated as well. In this thesis, the interleaved modulation scheme is not investigated.

4.5.2 Common Mode Coil to Suppress the Intensive Conducted EMI of Parallel Inverters Sharing Common DC Link

To prevent the high frequency harmonic current from circulating among paralleled inverter modules, several approaches have been proposed:

- Separate Input DC sources
- Output Isolation Transformer Installation
- Interphase Reactor Installation
- Common Mode Inductor

The first approach tries to isolate the parallel inverters from DC input. Although this method breaks the circulating path of the conducted current, it is not applicable when multiple DC sources are not available. Isolation transformer and interphase reactor methods are actually the same approach since the interphase reactor is actually an autotransformer. With isolation transformer installation, the inverter output current will be separated from the DC and high frequency harmonic

components. Since the core material of isolation transformer is easily available and low cost, isolation transformer method has been recommended in many research publications [94], [107], [108]. However, in the aspect of design and optimization, isolation transformer is not desired due to large size, high power loss, high EMI and saturation problems, especially when the system power level is not high.

Compared with isolation transformer, common mode inductor has the advantages of small size, low power loss and very good EMI filtering capability [109], [110], [111]. The high impedance of the common mode inductor blocks the noise propagation path. Therefore, common mode inductor is an ideal way of blocking the high frequency conducted current from circulating among the paralleled inverters. However, when the power rating of the inverter system is high, using common mode choke to suppress the common mode noise becomes challenging. First the leakage inductance of the common mode choke will possibly saturate the common mode inductor at high power. Therefore, to design the common mode inductor, the value of nominal input current must be considered carefully. Second, the core material of the common mode inductor is very expensive. Ferrites and nanocrystalline have been the two most popular core materials for common mode inductor. Ferrite cores have been widely used in implementing EMI filters due to its high permeability, wide operating frequency range and high volume resistivity. Therefore, ferrite cores are very suitable for high frequency applications. However, when the system power level increases, the size and volume of ferrite become very big. Nanocrystalline is more suitable for high power application owing to its much

higher permeability and higher thermal stability.

In the laboratory prototype of the parallel inverter system, common mode inductor approach is adopted to suppress the common mode noise as the system aggregate power is relatively low. In the next part, the detailed design procedures of common mode inductors for parallel inverter system will be presented.

4.5.3 Common Mode Coil Choke Design

As mentioned above, the first step to design a common mode coil choke is to select a proper core material. According to power level and budget limitation, ferrite or nanocrystalline is chosen. For ferrite cores, manganese zinc ferrite core is preferred owing to much higher permeability in frequency below 50MHz compared to Nickel Zinc core. For core shapes, toroids are preferred over other shapes for low cost and high permeability.

The following procedures of designing common mode inductors follow the standard inductor design process. The parameters required for common mode inductor design include frequency, input current and inductance value. Firstly, according to the application requirement, attenuation to circuit noise will be fixed. Next, the inductance value is calculated according to the desired attenuation factor [112]. Once the inductance is fixed, the core size the number of wiring are calculated.

The flowchart of the design process is shown in Fig. 4.14. The common mode

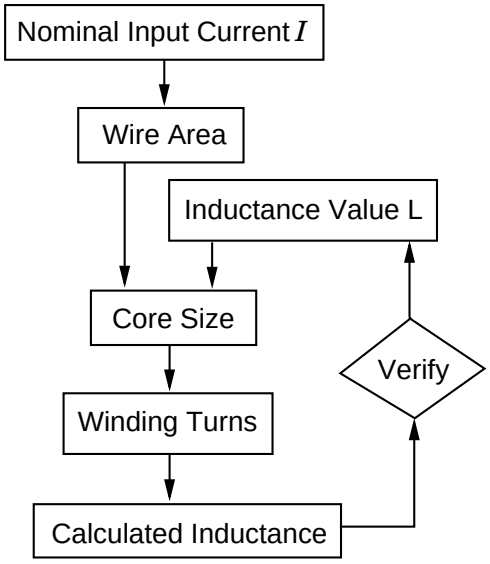


Figure 4.14: Flow Chart for the Common Mode Inductor Design Procedure

choke design has only two inputs, inductance value and peak current. According to the peak current rating $\widehat{I}$, wire size is calculated by

$$A_{wire} = \frac{\widehat{I}}{400A/cm^2} \tag{4.13}$$

With the calculated wire size and considering insulation, a wire with slighter larger area is selected.

According to energy balance,

$$\frac{1}{2}L\widehat{I}^2 = \frac{1}{2}\int \widehat{B}Hdv \tag{4.14}$$

Assuming uniform flux density and linear magnetics of the core, the above equation is simplified as:

$$L\widehat{I}^2 = \frac{\widehat{B}^2}{\mu} A_c l_c \tag{4.15}$$

where A_c is the core size and l_c is the circumferential area, which is calculated as follows:

$$l_c = \pi(d_o - d_w) \tag{4.16}$$

in which, d_o is the core diameter and d_w is the wire diameter. With (4.15) and (4.18), a proper size toroid core could be selected.

The last step is to calculate the number of turns according to the desired inductance and selected core.

$$N = 1000\frac{L}{A_L} \tag{4.17}$$

Where A_L is the inductance factor defined as $mH/1000$ turns, which can be retrieved from datasheet.

The last step before manufacturing the common mode choke is to verify that the achievable inductance based on the core and wire selection will not be considerably lower than desired value with the following equation:

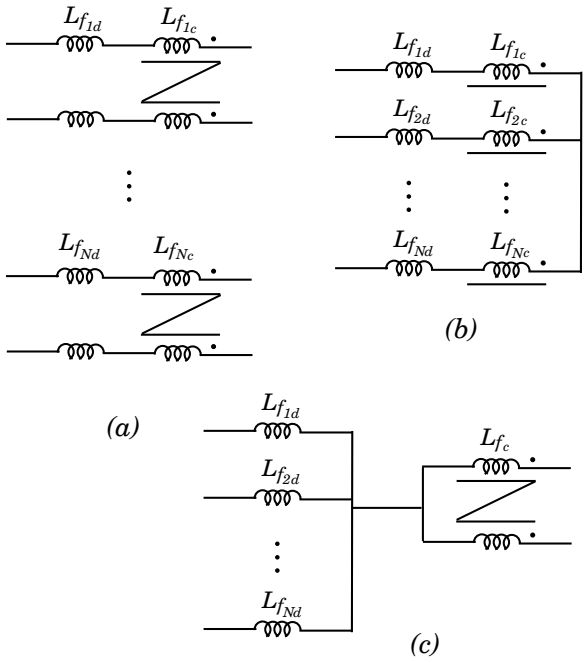


Figure 4.15: Three Options of Installing Common Mode Inductors in Parallel Converters

$$L_{max} = \frac{NA_c\widehat{B}}{\widehat{I}} \tag{4.18}$$

If the calculated L_{max} is lower than desired L, a larger core will be selected and the whole design process will be repeated.

4.5.4 Experimental Results

Following the design procedures, the previous experiment set up with common mode inductors in the output filter is implemented. Three options exist in implementing common mode inductor for parallel inverters as shown in Fig. 4.15. According to the results published in [113], the option (c) gives the best system

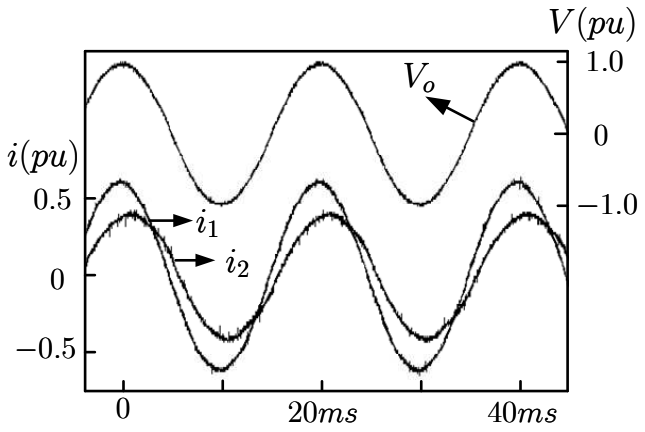


Figure 4.16: Experimental Results of the Unbalance Current Sharing between Two Parallel Inverters With Common Mode Inductors

performance. When system power level is not very high, (c) is a good option. However, considering system upgrade and power level expansion, (a) is preferred over (b) and (c), in which all the common mode inductors share a common core. In the experiment, the way of connection in (a) is selected. Fig. 4.12(b) shows the system topology.

Table 4.2: Output Filter Parameters of The Two Paralleled Inverters

L_{f_1}	C_{f_1}	L_{f_2}	C_{f_2}
$5.4mH$ 1.3Ω	$10\mu F$	$4.6mH$ 0.5Ω	$8\mu F$

Comparing the experimental waveforms shown in Fig. 4.13 with Fig. 4.16, we could see the high frequency current ripples and spikes are suppressed by common mode chokes. Next, the current sharing control scheme in [114] is implemented to balance the output power of the two inverters. Fig. 4.17 and Fig. 4.18 show the balanced current output of the two parallel inverter with output impedance mismatch.

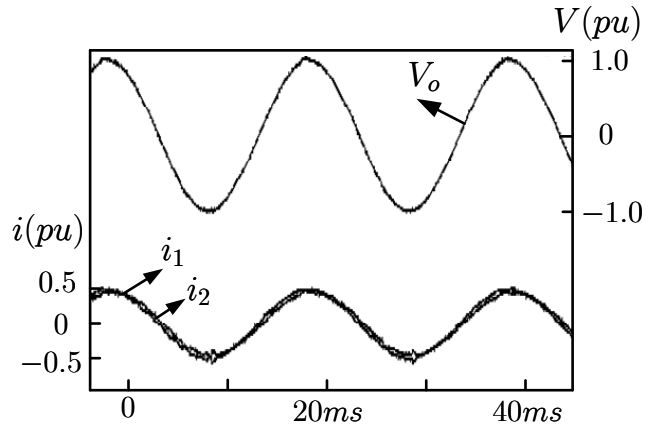


Figure 4.17: Experimental Results of the Balanced Current Sharing between Two Parallel Inverters With Impedance Mismatch

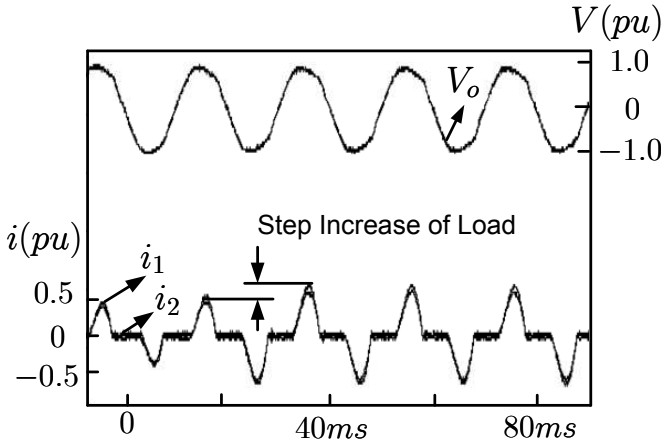


Figure 4.18: Experimental Results of the Balanced Current Sharing between Two Parallel Inverters Feeding Nonlinear Load

4.6 Dynamic Power Distribution Scheme for Parallel PCBB to Achieve Increased Efficiency and Life Span

4.6.1 Introduction to Dynamic Power Distribution Scheme

In this section, a dynamic power distribution scheme is proposed for parallel PCBBs to achieve efficiency optimization. When both inverters function simultaneously, balanced power sharing is important. However, it is not always the best solution to operate all the paralleled modules simultaneously, especially at light load.

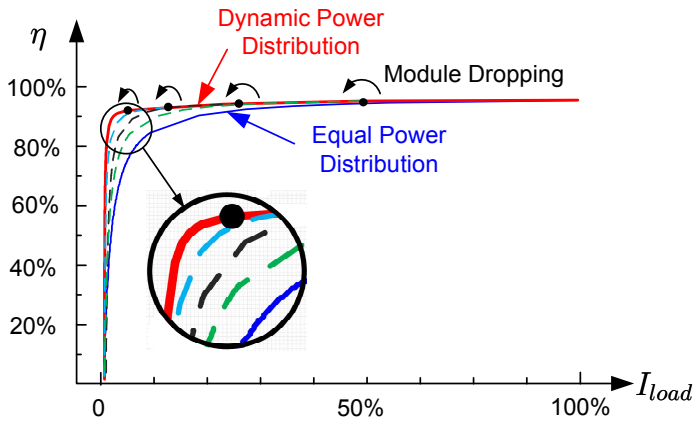


Figure 4.19: Theoretical Efficiency Curves of Paralleled Inverters System with Equal Power Distribution and Proposed Dynamic Power Distribution Strategies

Fig. 4.19 shows the theoretically estimated efficiency curves from single inverter to multiple paralleled inverters based on the dynamic electrical thermal models derived in [115]. According to Fig. 4.19, it is more efficient to run partial modules when load is not full. By dropping modules, system efficiency improves about

$10 - 25\%$ when system load is below 30% of peak.

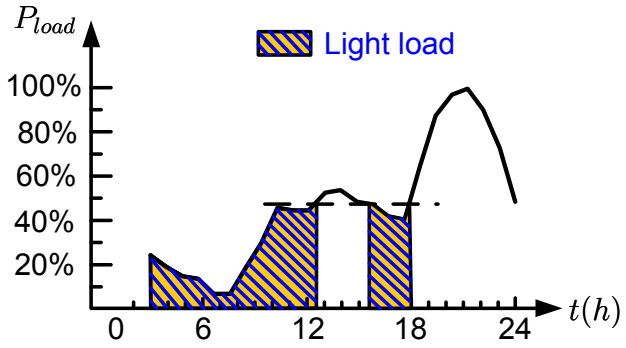


Figure 4.20: Rough Estimation of the One Day Load Profile of a Residential Microgrid

Looking at the one day residential load profile in Fig. 4.20, the load is below half of the peak for the majority of time. Therefore, a dynamic inverter dropping control scheme is proposed to improve system efficiency. Studies show that, the power cycling mean time to failure (MTTF) of an inverter decreases as the device junction temperature increases [116]. To reduce the junction temperature, the load must be reduced. In this chapter, instead of reducing peak junction temperature of the device, the thesis reduces the time for the device exposed to peak junction temperature. For the parallel inverter system, the proposed control system operates the inverters by turns to serve the load when the system is not operating at full load. Such time sharing scheme will help improve the system life span.

To facilitate the implementation of dynamic power distribution scheme, dynamic electro-thermal models are developed to evaluate the parallel inverter system efficiency and temperature in real time [115].

4.6.2 Control System Design

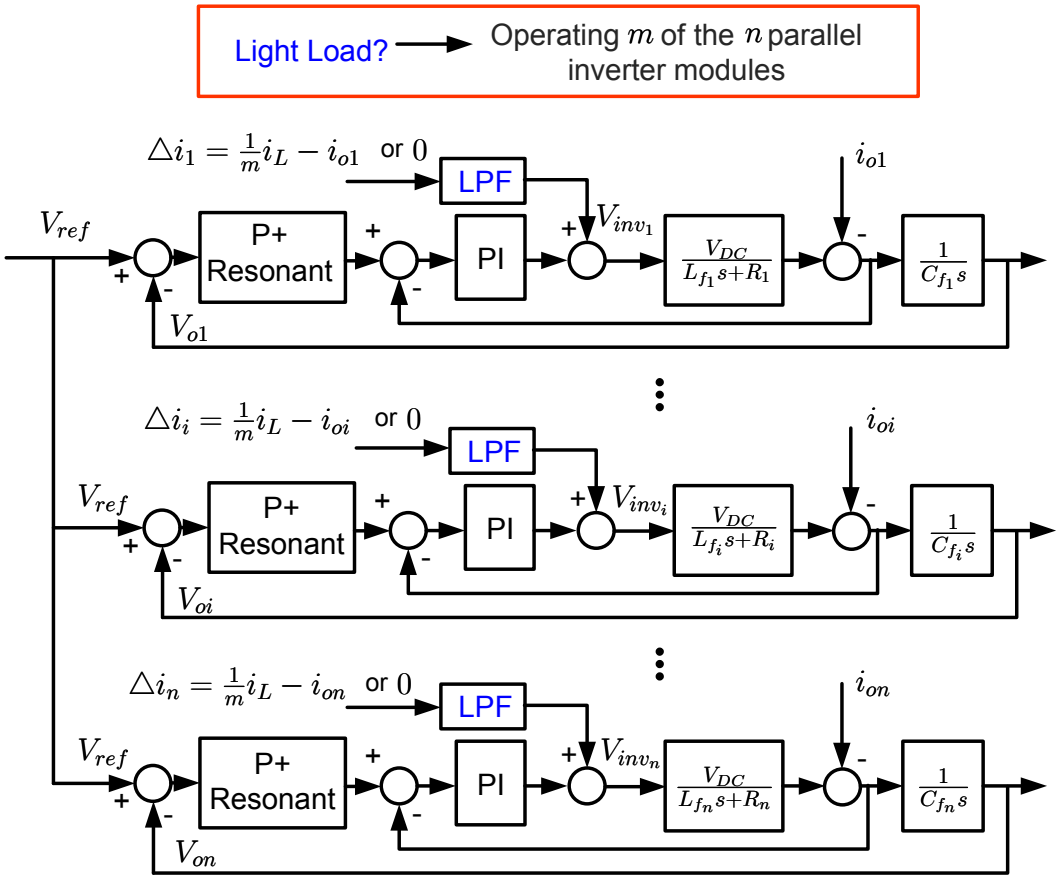


Figure 4.21: Proposed Dynamic Power Distribution Scheme

Fig. 4.21 shows the proposed dynamic power distribution scheme. The control system first decides the number of inverter modules to operate according to load condition. When n paralleled inverters are not running at full load, operating m ($m \leq n$) modules of the paralleled inverters will produce optimized efficiency without getting overloaded when:

$$m =](\frac{P_{load}}{P_o})[\tag{4.19}$$

where P_{load} is the total power of the load, P_o is the maximum power of each inverter module. The ceiling function, $]x[$, rounds up the result to the nearest larger integer.

The feedback error current value Δi for the control system of each inverter, as shown in Fig. 4.21, is derived as:

$$\begin{aligned} \Delta i_i &= \frac{i_L}{m} - i_i \\ {}_i &= 1, \cdots, m \end{aligned} \tag{4.20}$$

To minimize the circulating current among the paralleled operating inverter modules, the error current compensation control as described in last section is utilized.

4.6.3 Stability Analysis

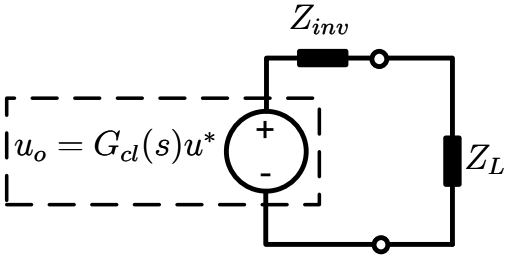


Figure 4.22: Equivalent circuit of controlled parallel voltage source inverters feeding load

Fig. 4.22 shows the equivalent circuit of the controlled parallel inverters feeding load, where Z_{inv} is the equivalent output impedance of the paralleled inverters, which is equivalent to the sum of the m paralleled operating inverters. Z_L is the equivalent load impedance. Since the two subsystems are connected in series, the overall input-to-output transfer function of the cascaded system is given by (4.21) [117], [118].

$$G_T(s) = \frac{G_{cl}(s)}{1 + \frac{Z_{inv}}{Z_L}} \tag{4.21}$$

where $G_{cl}(s)$ is the input-to-output transfer function of the inverter. According to Fig. 6.4, the system transfer functions are derived as:

$$\begin{aligned} G_{op}(s) &= G_{PR}(s)\frac{G_{PI}(s)\frac{V_{DC}}{L_f s+R}}{1+G_{PI}(s)\frac{V_{DC}}{L_f s+R}}\frac{1}{C_f s} \\ G_{cl}(s) &= \frac{G_{op}(s)}{1+G_{op}(s)} \end{aligned} \tag{4.22}$$

where $G_{PR}(s)$ is the outer loop voltage controller and $G_{PI}(s)$ is the inner current loop controller. Although the output impedances of all the inverters in parallel are different, the same controller can be used for each one. Fig. 4.5 shows the bode plots of twenty controlled inverter systems with 50% parameter variation. It is shown that the controller has good robustness regarding parameter variation. According to the Frequency Response of the Open-Loop System, we could conclude that the close loop system transfer function $G_{cl}(s)$ is guaranteed stable.

Since $G_{cl}(s)$ has been proved stable, to prove the stability of the n paralleled inverters, we only need to make sure $Z_{inv} \ll Z_L$ [117], [118]. Z_{inv} is the equivalent impedance of m paralleled inverter modules, $Z_{inv} = Z_{inv,1}//.../Z_{inv,m}$. Therefore, to prove $Z_{inv} \ll Z_L$, we choose the worst case and prove $Z_{inv,i} < Z_L$.

According to Fig. 6.4, the equivalent output impedance of $Z_{inv,i}$ is

$$Z_{inv,i} = -\frac{V_o}{i_1}|_{V_{ref}=0} = \frac{1}{\frac{G_{PR}(s)G_{PI}(s)}{L_f s+R} + \frac{G_{PI}(s)C_f s}{L_f s+R} + C_f s} \tag{4.23}$$

Fig. 4.23 shows the frequency response of the output impedance transfer

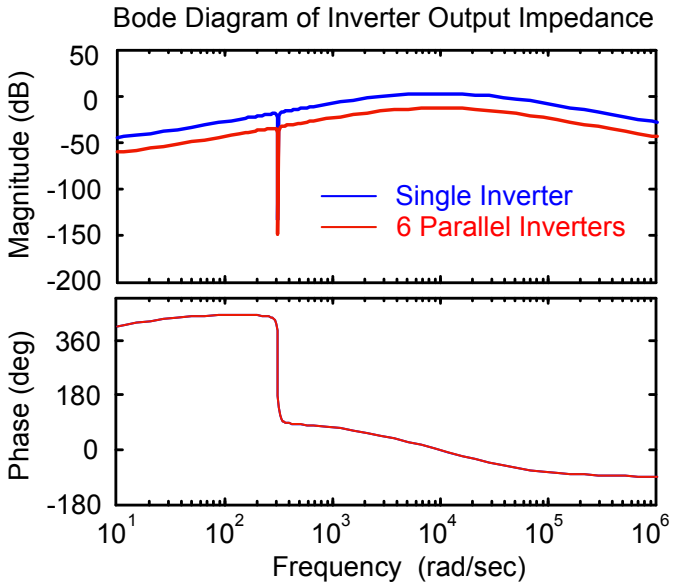


Figure 4.23: Frequency response of the output impedance of proposed controlled voltage source inverter

function of one inverter and six paralleled inverters. Since the paralleled inverters are used to feed the load in islanding microgrid, Z_L will always be a positive impedance. Therefore, the proposed control dynamic power distribution scheme can maintain $Z_{inv} < Z_L$ and guarantee the stability of the n paralleled inverter system.

4.6.4 Verification by Simulation

Fig. 4.24 shows the simulation results of the system reconfiguring from two paralleled inverters operation to single inverter. For two inverters in parallel, when the system is between half load and full load, the error current to correct for each inverter is $\frac{1}{2}i_L - i_{oi}$. When the system is under half of the peak load, only one of the two inverters operates, the error current for the operating inverter is $i_L - i_{oi}$ and

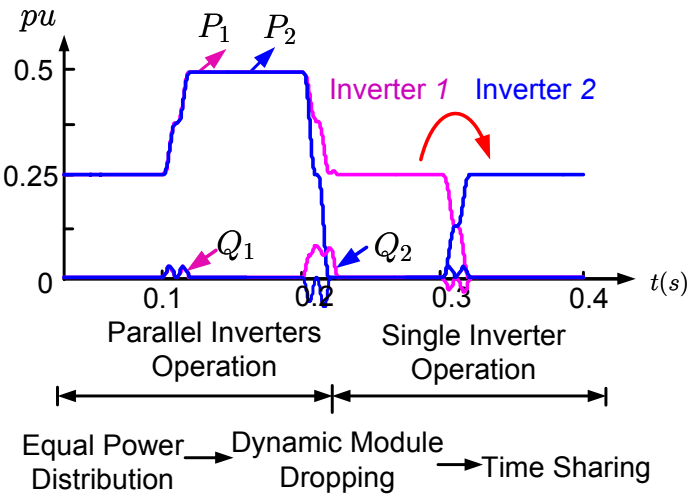


Figure 4.24: Simulation results of paralleled inverters inside the same block controlled by proposed dynamic power distribution scheme under various load conditions

for the stand by inverter, $\triangle i_{oi} = 0$. As shown in Fig. 4.24, the transition process is smooth. For the dynamic module dropping scheme and time sharing scheme, good steady state and dynamic performance are observed.

4.6.5 Hardware in the loop real time test

The set up is comprised of hardware controller, RTDS, and a work station. The hardware controller digitally implements the proposed dynamic power distribution scheme. As mentioned in Chapter II, RTDS is used to simulate the microgrid with parallel inverters in real time. RTDS is a fully digital electromagnetic transient power system simulator that operates in real time. The advantage of RTDS is that it can represent the dynamics of a system close to a practical system since it is designed to simulate systems in real time with small step size on multiple parallel

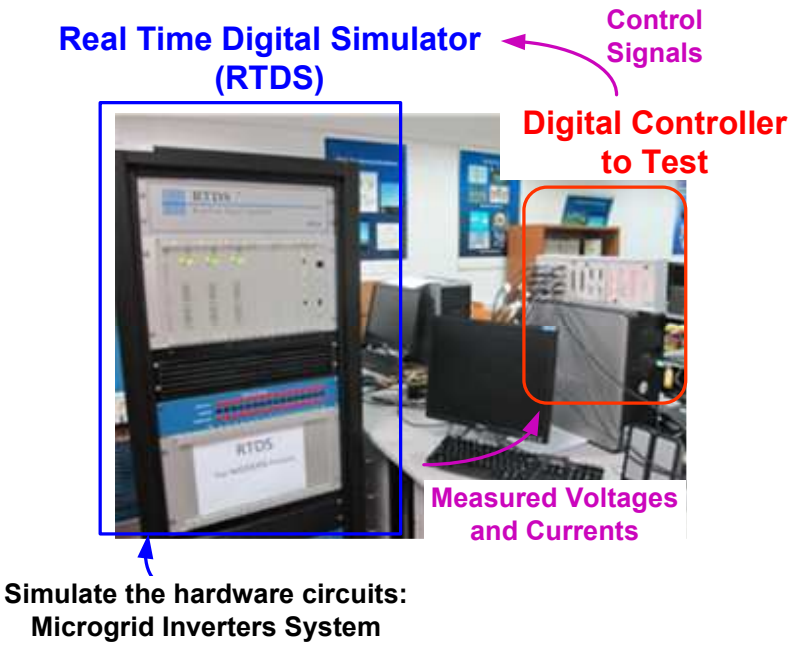


Figure 4.25: Laboratory Setup for Hardware Controller in the Loop Test with Real Time Digital Simulator (RTDS)

running digital signal processors [77]. Such arrangement as shown in Fig. 4.25 is commonly referred to as "hardware-in-the-loop test", where a hardware controller is physically integrated within a plant simulated by RTDS to test the controller performance in real time. The system parameters are set the same as given in Table. 4.2.

Fig. 4.26 shows the real time test result of the steady state performance of the proposed dynamic distribution scheme. The output currents of the two paralleled inverters are well balanced. Fig. 4.27 shows the dynamic performance of the power distribution scheme in transferring the system from paralleled inverter operation to single inverter operation when the load decreases. Smooth and fast transient performance is observed.

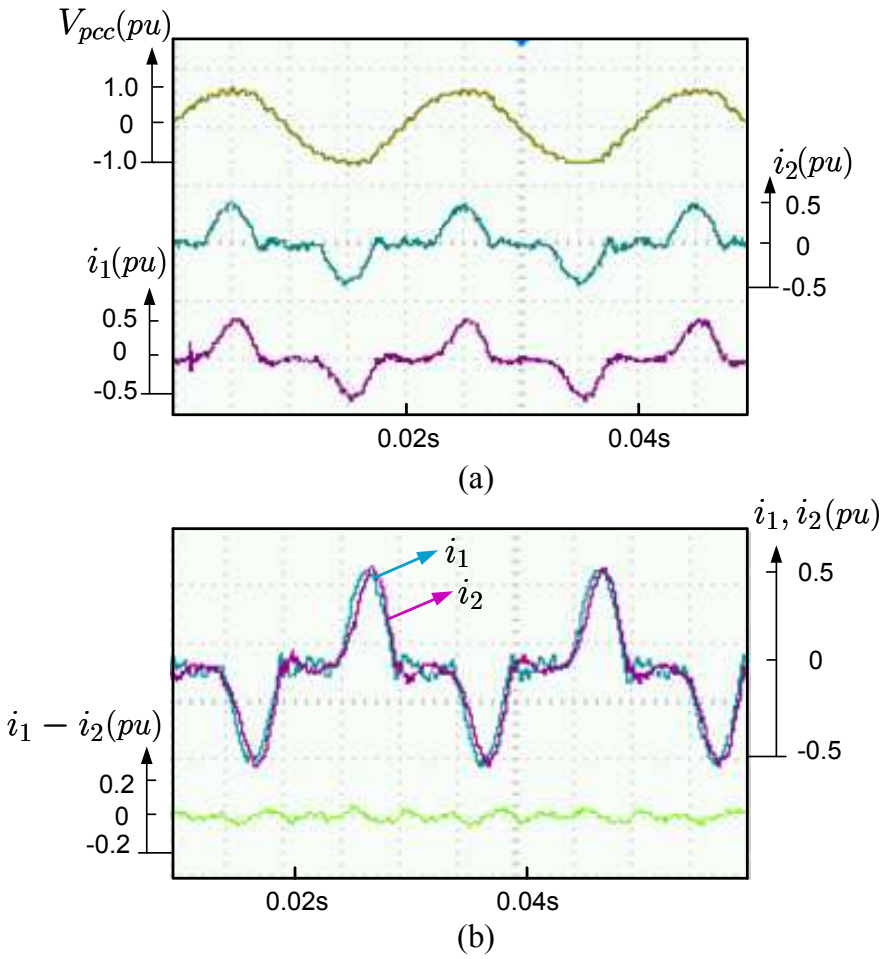


Figure 4.26: Steady State Performance Real Time Test Results of the Equal Power Sharing Control Strategy

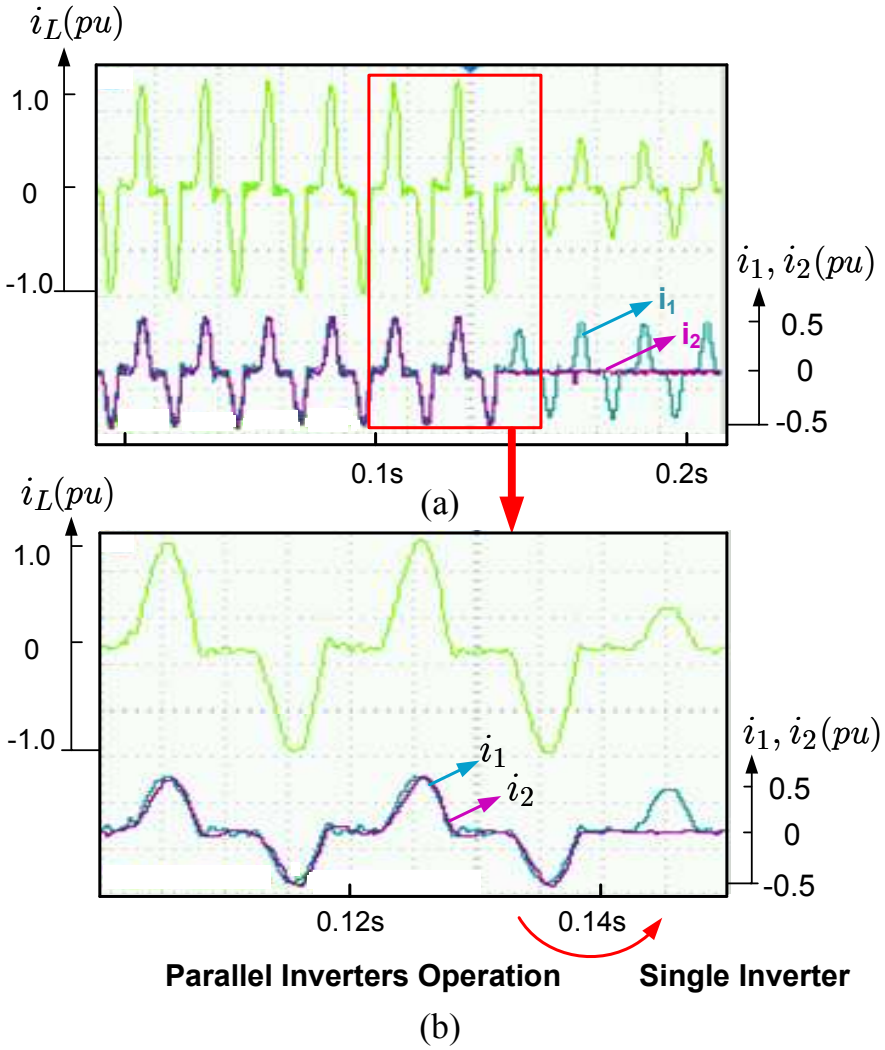


Figure 4.27: Dynamic Performance Real Time Test Results of the Proposed Dynamic Module Dropping Scheme

4.7 Summary

In this chapter, a novel power sharing and time sharing strategy is proposed to increase the system operating efficiency and life span. The stability of the proposed dynamic power distribution control architecture applied to n paralleled inverters is proved. Both simulation and real time test results demonstrate the viability of the proposed control strategies. Digital current sharing controller with common mode inductor method is proposed to suppress the circulating currents among the parallel inverters sharing the same DC link. Experimental results validate the proposed scheme.

Chapter 5

Reliability, Efficiency Improvement and Cost Optimization of PCBB

5.1 Introduction

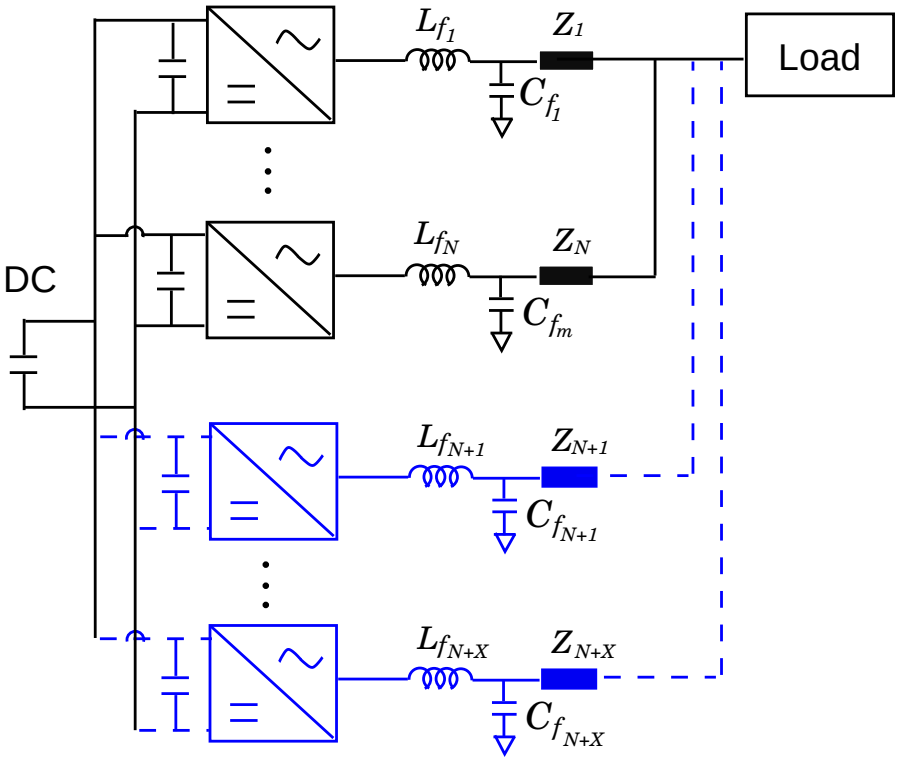


Figure 5.1: System Architecture of N Parallel Inverters with X Redundancy

As discussed in previous chapters, power converter building block performs

multiple functions to ensure the normal operation of microgrid under different operating scenarios. Therefore, the reliability of PCBB is important in terms of system operation and cost. In addition, compared to the other components of microgrid, the reliability of power converter is much lower. Take the PV generator discussed in [18] as an example, the failure rate of PV module is much lower compared to inverter module [19], [20]. Therefore, to improve the overall system reliability, evaluating and improving the power conversion system reliability is the key.

To achieve expanded power level and system redundancy, $N+X$ type of parallel connected inverter systems are employed as shown in Fig. 5.1. The power of the N parallel inverters add up to the peak power of the load, and the rest X converters serve as back up for redundancy consideration. By using redundant inverters, the system reliability will be increased significantly. In addition, to implement a high power system with parallel connected inverters, the repair and replacement cost of each failure will be reduced.

Research has shown that when the number of redundant inverters X increases to certain value, the reliability of the system will not improve much [119], [106], [120]. Though informative, those qualitative analysis does not give a solution on how to determine X in a distributed power system to achieve maximum reliability and minimum cost. In this chapter, mathematical models are derived to quantitatively evaluate the reliability and cost of parallel redundant inverter systems. A framework to determine N and X by optimizing system cost and reliability is proposed.

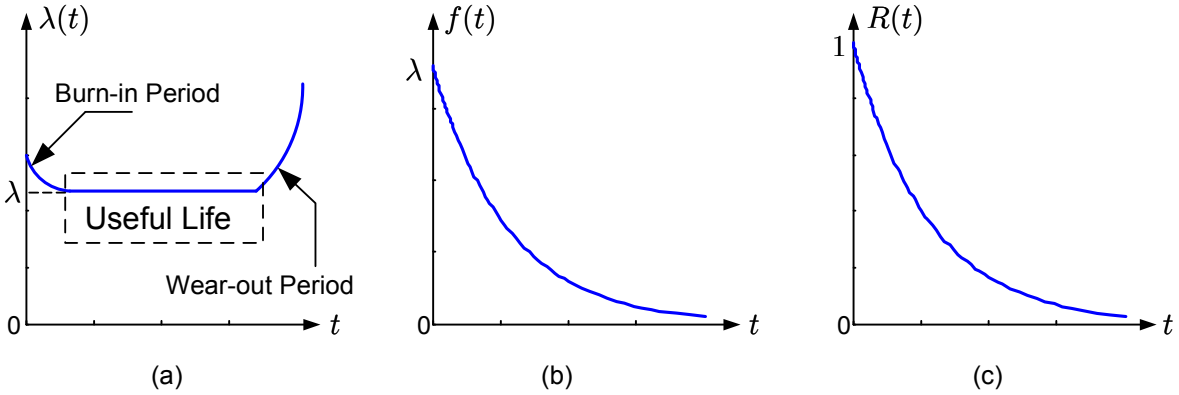


Figure 5.2: Plots of Exponential Distributed System Reliability Indices: (a) The Failure Rate, (b) The Power Density Function and (c) The Reliability Function

In last chapter, the control strategies to balance the power among the parallel PCBB modules have been discussed with detailed implementation procedures. Qualitative analysis has shown that with proposed dynamic power distribution scheme, the parallel inverter system is able to achieve higher efficiency and longer life span. In this chapter, we will quantitatively compare this novel power distribution scheme with conventional scheme in terms of reliability and cost.

5.2 Fundamentals of Reliability Analysis

Before looking into the reliability evaluation of a complete inverter system, we first introduce some basic terminology and definitions related to reliability evaluation [121], [122].

λ, **failure rate** is the frequency of a component fails. Most engineering components, especially semiconductor devices, follow the bathtub shape failure rate curve as shown in Fig. 5.2.(a). Actually, the failure rate varies over the life cycle

of the system. However, during most of the time, the failure rate of the system maintains constant. Therefore, we could approximate the system by exponential distribution with failure rate λ [31]. The IEEE Standard 1240 [123] took the same assumption during evaluating the reliability of HVDC converter stations with exponential distribution.

Failure rate under operating conditions is different from base failure rate for electric and electronic equipment and it is affected by various factors, such as operating voltage, current, temperature, etc [31], [124], [125].

$$\lambda = \lambda_{ref} \times \pi_U \times \pi_I \times \pi_T \tag{5.1}$$

where λ_{ref} is the failure rate under reference conditions;

π_U is the voltage dependence factor;

π_I is the current dependence factor;

π_T is the temperature dependance factor.

μ, **repair rate** is the frequency of a component getting repaired. For exponential distribution, repair rate is also constant.

$f(t)$, **probability density function** gives the probability a component fails at time t. For exponential distribution,

$$f(t) = \lambda e^{-\lambda t} \tag{5.2}$$

Fig. 5.2.(b) shows the probability density function of exponential distribution.

$R(t)$, **reliability** or **survival function** calculates the probability a component survival beyond time t. As shown in Fig. 5.2.(c), the system reliability decreases exponentially as time increases.

$$R(t) = e^{-\lambda t} \tag{5.3}$$

MTTF, **mean time to failure** is the mean up time of a system. For system with much higher repair rate than failure rate, MTTF can be approximated by MTBF, mean cycle time of the system. For exponential distribution,

$$MTBF \approx MTTR = \frac{1}{\lambda} \tag{5.4}$$

MTTR, **average time that the system is in repair condition**, is the mean down time of a system. For exponential distribution,

$$MTTR = \frac{1}{\mu} \tag{5.5}$$

A, **Availability**, refers to the probability of the system being found in operating states.

$$A = \frac{MTTF}{MTTF + MTTR} = \frac{\mu}{\mu + \lambda} \tag{5.6}$$

U, **Unavailability**, is the probability of the system being found in down states.

$$U = \frac{MTTR}{MTTF + MTTR} = \frac{\lambda}{\mu + \lambda} \tag{5.7}$$

5.3 Reliability Modeling of Power Conversion System

5.3.1 Reliability Model of Single PCBB

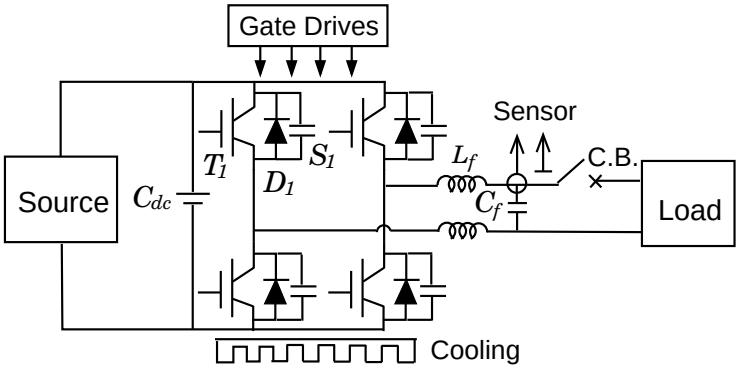


Figure 5.3: Practical Single-Phase IGBT Inverter with Output Filter

Fig. 5.3 shows the detailed structure of a practical single phase inverter system, which include IGBTs, Diodes, snubbers, gate drivers, voltage and current sensors, DC link capacitors, circuit breaker, cooling system and output filter. To evaluate the inverter system reliability, we need the information of failure rate

Table 5.1: The Failure Rate of Each Component of A Practical Single Phase System (230V, 5kW)

Part Name of the Inverter System	Failure Rate (per million hours)
DC link Capacitor C_{dc}	$\lambda_1 = 3.03$
IGBT T_1	$\lambda_2 = 0.9$
Diode D_1	$\lambda_3 = 0.8$
Snubber S_1	$\lambda_4 = 0.001$
Passive Filter Inductance L_f	$\lambda_5 = 0.038$
Passive Filter Capacitance C_f	$\lambda_6 = 0.87$
Voltage Sensor	$\lambda_7 = 0.56$
Current Sensor	$\lambda_8 = 0.5$
Circuit Breaker (C.B.)	$\lambda_9 = 3.3$
Cooling System	$\lambda_{10} = 1.36$
Gate Drive (Power Supply)	$\lambda_{11} = 1.0$

and repair rate of each component. For power semiconductors and inverter systems, the reliability parameters are not uniform for different power ratings and manufacturers. In this thesis, the failure rates of the components come from the following sources: the military handbook on reliability [31] released in 1995, IEC Standard 61709 published in 1994 [124], IEC Standard 62380 published in 2004 [125], and the field data provided [126], [127]. Physics-of-failure has been proposed as a more accurate reliability prediction method [128], [129]. However, all possible failure mechanisms of voltage source inverter components have not been identified. Therefore, the data for a complete voltage source inverter system are not available. The failure rate of the whole piece hardware is calculated as:

$$\begin{aligned} \lambda_{tot} &= \lambda_1 + 4 \times (\lambda_2 + \lambda_3 + \lambda_4 + \lambda_{11}) + 2 \times \lambda_5 + \sum_{i=6}^{10} \lambda_i \\ &= 0.18/year \end{aligned} \tag{5.8}$$

In this thesis, the repair rate of the inverter system is set as 24 days following the field test data of the high power PV inverter system installed in Atlanta, Georgia [126]. For inverters of different power rating or manufacturers, the repair rate might be quite different since it is affected by multiple factors including failure detection, failure diagnosis, maintenance personal traveling, spare parts installation, system repair and system restart. However, the framework of reliability evaluation and cost optimization to optimize the parallel inverter architecture is the same. The influence of different parameters on the models derived will also be investigated in terms of sensitivity analysis later.

Among the various reliability indices discussed previously, we select failure rate and availability as system reliability evaluation indices. Failure rate and availability respectively decides the maintenance and repair cost, and system down time cost, which are the two major costs during a system operation.

5.4 Reliability Analysis of Parallel Connected PCBBs

To evaluate the parallel inverter system reliability under different topology and control strategies, we take a 100kW power conversion system as an example.

5.4.1 Case Study I: Reliability of Single Inverter Operation

When the whole system is implemented with single inverter, the system failure rate and availability are calculated with (5.8) and (5.6).

$$\lambda_{tot,1} = 0.18/year \tag{5.9}$$

$$MTBF_1 = \frac{1}{\lambda_{tot,1}} \approx 5.5 years \tag{5.10}$$

$$\mu_1 = 365/24 = 15.2/year \tag{5.11}$$

$$A_1 = \frac{\mu_1}{\mu_1 + \lambda_{tot,1}} = 0.9883 \tag{5.12}$$

5.4.2 Case Study II: Reliability of $N + X$ Parallel Inverters

For a parallel system of $N + X$ architecture as shown in Fig. 5.1, the system operates when N of the total $N + X$ converters operate. If we assume the failure of the parallel inverters are independent, the system satisfies the $k - out - of - n$ reliability model [130]. The system reliability function becomes:

$$R_{N+X} = \sum_{j=N}^{N+X} \binom{N+X}{N} R^j (1-R)^{N+X-j} \tag{5.13}$$

The failure rate of the $N + X$ parallel inverter system is derived as:

$$\lambda_{N+X} = \frac{1}{MTBF_{N+X}} = \frac{1}{\frac{1}{\lambda} \sum_{j=N}^{N+X} \frac{1}{j}} \tag{5.14}$$

Fig. 5.4 shows the failure rate plot of a $N + X$ parallel inverter system as N and X vary.

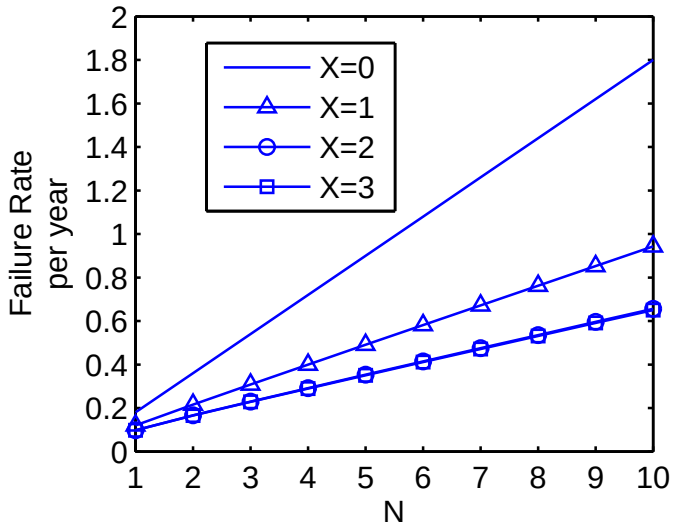


Figure 5.4: Failure Rate Variation of an $N + X$ Redundant Parallel Inverter System

The availability of the overall system becomes:

$$A_{N+X} = \sum_{j=N}^{N+X} \binom{N+X}{N} A^j U^{N+X-j} \tag{5.15}$$

The system availability of $N + X$ parallel inverter system as N and X vary is shown in Fig. 5.5.

Taking the example in case study I, if we implement the power conversion system with 3 parallel inverters with 1 redundant inverter, according to (5.14) and (5.15),

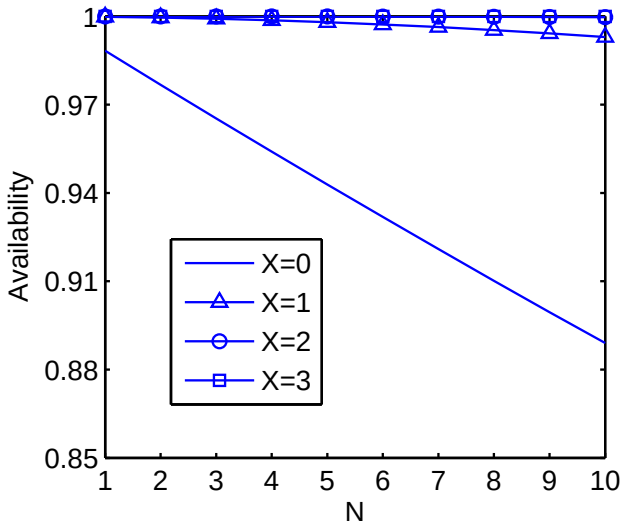


Figure 5.5: Availability of an $N + X$ Redundant Parallel Inverter System

$$\lambda_{3+1} = \frac{1}{\frac{1}{\frac{1}{0.18}\times(\frac{1}{3}+\frac{1}{4})}} = 0.309/year \tag{5.16}$$

$$MTBF_{3+1} = \frac{1}{\lambda_{3+1}} \approx 3.24 years \tag{5.17}$$

$$\mu_{3+1} = \mu_1 = 15.2/year \tag{5.18}$$

$$A_{3+1} = \sum_{j=3}^{3+1} \binom{3+1}{3} A_1^j U_1^{3+1-j} = 0.9992 \tag{5.19}$$

where λ_{3+1}, $MTBF_{3+1}$, μ_{3+1} and A_{3+1} are the equivalent system failure rate, mean life cycle, repair rate and availability of the redundant parallel inverters respectively.

Compared with single inverter operation in case study I, though parallel inverter operation increases system failure rate, the probability of the system in success state has been greatly increased. Such merit is very important especially when system power scale is large and down time cost per day is significant.

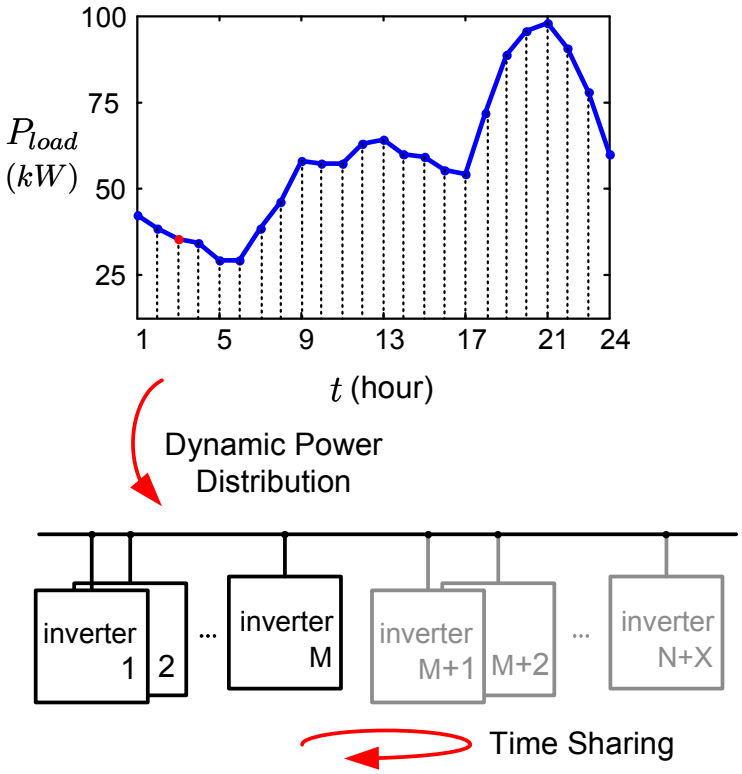


Figure 5.6: Illustration of Dynamic Power Distribution Scheme

5.4.3 Case Study III: Reliability of $N+X$ Parallel Inverters under Dynamic Power Distribution Scheme

Fig. 5.6 shows the principle of dynamic power distribution scheme discussed in Chapter IV [114]. At any point of operation, the control system will selectively operate part (M) of the total $N + X$ inverters to achieve maximum operating efficiency. In addition, when the load is not full capacity, the parallel operating inverters will serve the load by turns with the idle modules to improve the system thermal profile. If we implement the dynamic power distribution scheme to the 3+1 100kW parallel redundant inverter system, the average operating time of each inverter becomes

$$\overline{T} = \frac{\overline{P_{load}(t)}}{P_{max}} T_{tot} \approx 0.45 T_{tot} \tag{5.20}$$

Therefore with the same type of inverters, dynamic power distribution scheme will increase the mean time between failure of each inverter. The reliability indices of each inverter under dynamic power distribution scheme are recalculated:

$$\lambda_{DPG} = \frac{\overline{P_{load}(t)}}{P_{max}} \times \lambda = 0.082/year \tag{5.21}$$

$$MTBF_{DPG} = \frac{1}{\lambda_{DPG}} = 12.2 years \tag{5.22}$$

$$\mu_{DPG} = \mu_1 = 15.2/year \tag{5.23}$$

$$A_{DPG} = \frac{\mu_{DPG}}{\mu_{DPG} + \lambda_{DPG}} = 0.9946 \tag{5.24}$$

$$\tag{5.25}$$

where $MTBF_{DPG}$, λ_{DPG}, μ_{DPG} and A_{DPG} are the mean life cycle, failure rate, repair rate and availability of individual inverter within the parallel inverter system under dynamic power distribution. For a 3+1 redundant parallel inverter system, the equivalent reliability indices are derived following (5.14) and (5.15):

$$\lambda_{3+1,DPG} = \frac{1}{\frac{1}{\frac{1}{0.082}\times(\frac{1}{3}+\frac{1}{4})}} = 0.14/year \tag{5.26}$$

$$MTBF_{3+1,DPG} = \frac{1}{\lambda_{3+1}} \approx 7.11 years \tag{5.27}$$

$$\mu_{3+1,DPG} = \mu_1 = 15.2/year \tag{5.28}$$

$$A_{3+1,DPG} = \sum_{j=3}^{3+1} \binom{3+1}{3} A_{DPG}^{j}(1-A_{DPG})^{3+1-j}$$
$$= 0.9998 \tag{5.29}$$

Comparing the reliability analysis results with those in case study I and II, we could see that the dynamic power distribution scheme will not only increase the system availability but also reduce the system failure rate. Therefore, both system maintenance cost and downtime cost can be minimized.

As Fig. 5.4 and Fig. 5.5 show, regardless of N, the system failure rate and availability will not change much after the redundancy of the system increased to 3. Though reliability analysis gives information on how to design the system architecture and control scheme, the reliability information alone does not provide the optimal architecture of a $N+X$ system. In next section, we will discuss about the impact of reliability to system cost and how to design (N,X) to optimize system total cost.

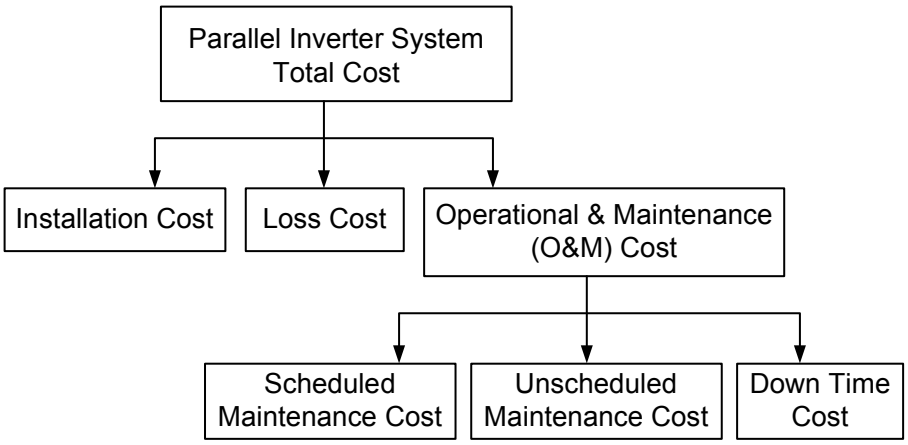


Figure 5.7: Diagram of the Total Cost of Parallel Inverter System

5.5 Cost Analysis and System Architecture Optimization

Fig. 5.7 shows the components of the total system cost of a parallel inverter system. As shown in the figure, the power conversion system cost include initial installation cost, operational and maintenance cost and power loss cost.

The installation cost of the system includes the investment cost of power converter systems and cooling systems. The cooling system is assumed to be 10% of the converter system cost. The cost of inverter is assumed to be proportional to the rating of the system. According to the survey of solarbuzz [131], the cost of inverter per capacity is $\$715/kW$. Therefore, the total installation cost of a PkW parallel inverter system with N major parallel inverters and X redundant modules becomes

$$C_{int} = 715 \times P \times (1 + \frac{X}{N}) \tag{5.30}$$

The operational and maintenance (O&M) cost of a power conversion system consists of three parts: scheduled maintenance cost, unscheduled maintenance cost and down time cost. The scheduled maintenance cost refers to the average annual O&M cost, which is $5\% - 6\%$ of the investment cost [132]. Therefore the scheduled O&M cost for a parallel inverter system of 20 years warranty is derived as

$$C_{O\&M,s} = C_{int} \times 5\% \times 20 = C_{int} \tag{5.31}$$

The unscheduled maintenance cost refers to the cost incurred by system random failure. The unscheduled maintenance cost includes not only the replaced parts and labor cost, but also the travel cost of the technical support staff. Therefore, the unscheduled O&M cost of the power conversion system operating in 20 years becomes

$$C_{O\&M,u} = \lambda_{N+X} \times 20 \times (C_{part} + C_{lt} \times MTTR) \tag{5.32}$$

$$C_{part} = 715 \times P \times \frac{1}{N} \tag{5.33}$$

where λ_{N+X} is the equivalent failure rate of the parallel inverter system as shown in (5.14); C_{part} is the cost of one inverter module, and C_{lt} is the cost of labor and travel per repair. The labor travel cost per power capacity per day per failure is estimated to be $\$300/kW\dot{d}ay$ [132]. MTTR is the mean repair time of the system as shown in (5.5). Therefore, the unscheduled maintenance cost is generated as

$$C_{O\&M,u} = \frac{1}{\frac{1}{\lambda}\sum_{j=N}^{N+X}\frac{1}{j}} \times 20 \times (715 \times P \times \frac{1}{N} + m \times \frac{1}{\mu}) \tag{5.34}$$

The down time cost is related to the power scale of the system. Assuming for a 100kW system, the per day cost is around \$1000. Therefore, the total downtime cost within 20 years becomes

$$\begin{aligned} C_{down} &= 20 \times (1 - A_{N+X}) \times 1000 \times 365 \\ &= 20 \times (1 - \sum_{j=N}^{N+X} \binom{N+X}{N} A^j U^{N+X-j}) \\ &\quad \times 365000 \end{aligned} \tag{5.35}$$

The power loss cost is also assumed to be $10/kW \cdot h$. Therefore, the power loss cost of a system in 20 years life time is equivalent to

$$C_{loss} = (1 - \eta) \times P \times 0.87 \times 24 \times 365 = (1 - \eta) \times P \times 7591 \tag{5.36}$$

With (5.30), (5.31), (5.34), (5.35), and (5.36), the total cost of the whole system becomes

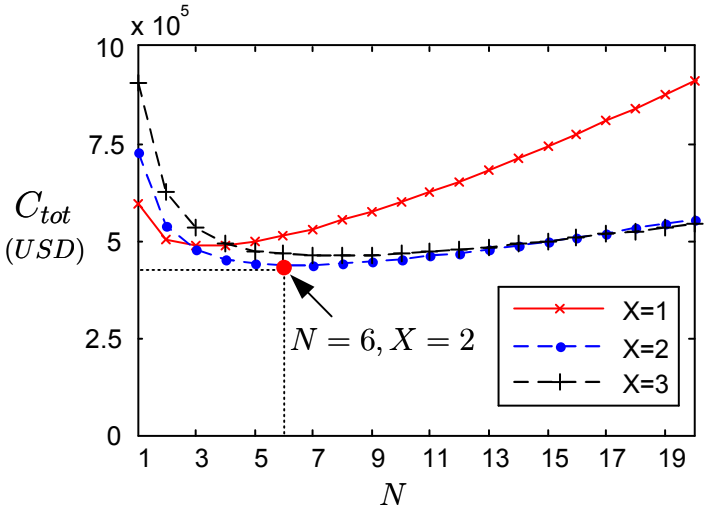


Figure 5.8: Total cost of the 100kW Power Inverter System under Different Degree of Redundancy

$$\begin{aligned} C_{tot}(N,X) &= C_{int} + C_{O\&M,s} + C_{O\&M,u} + C_{down} + C_{loss} \\ &= 715 \times P \times (1 + \frac{X}{N}) \times 2 \\ &+ \frac{1}{\frac{1}{\lambda}\sum_{j=N}^{N+X}\frac{1}{j}} \times 20 \times (715 \times P \times \frac{1}{N} + m \times \frac{1}{\mu}) \\ &+ 20 \times (1 - \sum_{j=N}^{N+X} \binom{N+X}{N} A^j U^{N+X-j}) \\ &\quad \times 365000 + (1-\eta) \times P \times 7591 \end{aligned} \tag{5.37}$$

Therefore, by minimizing $C_{tot}(N,X)$, the optimal system architecture with N parallel inverters and X redundant inverters can be obtained. Since the reliability analysis shows that the system failure rate and availability won't change much when $X > 3$ regardless the value of N, we could solve (5.37) is a much simplified way through finding the minimal value of C_{tot} under $X = 1, 2, 3$.

The previous case in reliability analysis is taken as an example here also. The system power rating $P = 100kW$, failure rate and repair rate of individual inverter are $0.18/year$ and $15.2/year$ respectively. By optimizing C_{tot}, $N = 6$ and $X = 2$ are found. The simulation results of system total cost under different degree of redundancy is shown in Fig. 5.8. As indicated in Fig. 5.8, the system cost is minimized when $N = 6$ and $X = 2$.

5.5.1 Dynamic Power Distribution Scheme Reduces System Cost

With dynamic power distribution scheme as shown in Fig. 5.6, the control system will select the number of operating inverters according to load condition to minimize the system power loss. According to [114], under light load conditions, the system efficiency can be increased by $10\% - 15\%$. The average efficiency increment is approximately 3%. In addition, the system failure rate decreases and availability increases.

Considering the same 100kW parallel inverter system with optimal structure $N = 6, X = 2$, the reduction of system total cost (5.37) is calculated as

$$\Delta C_{tot} = C_{tot}(6,2) - C_{tot_{DPG}}(6,2) = \$46244 = 9\% C_{tot}(6,2) \tag{5.38}$$

where $C_{tot}(6,2)$ is the system total cost under conventional equal current sharing control scheme, when system has 6 major modules and 2 redundant modules;

$C_{tot_{DPG}}(6,2)$ is the system total cost when dynamic power distribution scheme is applied. The 9% cost reduction shows adopting dynamic power distribution scheme will not only improve the parallel inverter system reliability but also minimize the system cost.

5.6 Sensitivity Analysis

In previous section, in terms of minimizing the total cost function (5.38), the optimized solution to system architecture, $N = 6$, $X = 2$ is obtained. In this section, sensitivity analysis is carried out to investigate the impact of parameter variation on the proposed reliability and cost models.

Table 5.2: The Quantifiable Variables Values of a $6 + 2$ Parallel Inverter System Cost

Quantifiable Variables	Value
λ_{6+2}	$0.41/yr$
μ_{6+2}	$15.15/yr$
System Power Rating	100 kW
Labor/Travel Cost	$\$300/kW\dot{d}ay$
Inverter Cost	$\$715/kW$

The procedures of conducting sensitivity analysis of the important parameters to the cost function are as follows:

1. Identify the key variables.

2. Calculate effects of changing variables.

To quantify the sensitivity of the variables, sensitivity indicator for each vari-

able with respect of the system total cost is calculated. The sensitivity indicator is calculated as [133]:

$$SI = \frac{(NPV_b - NPV_I)/NPV_b}{(X_b - X_I)/X_b} \tag{5.39}$$

where NPV_b is the net present value in the base case; NPV_I is the net present value in the sensitivity test; X_b is the variable value in the base case; and X_I is the variable value in the sensitivity test.

3. Analyze the effects of changing key variables. The larger the sensitivity indicator, the more influence of the variable change to the net present value. Under some cases, when SI is overlarge, the cost-optimized solution does not hold under slight variable change.

The key variables to system cost optimization with base values are listed in Table 5.2. The optimized structure $N = 6$, $X = 2$ is the base case. The base net present value NPV_b calculated with (5.38) equals to $\$4.51 \times 10^5$.

Table 5.3: Numerical Sensitivity Analysis Results

Item	Change	NPV	SI
Base Case		$\$4.51 \times 10^5$	
λ_{6+2}	+10%	$\$4.67 \times 10^5$	0.34
μ_{6+2}	+10%	$\$4.46 \times 10^5$	-0.12
System Power Rating	+10%	$\$4.90 \times 10^5$	0.87
Labor/Travel Cost	+10%	$\$4.57 \times 10^5$	0.13
Inverter Cost	+10%	$\$4.73 \times 10^5$	0.48

To conduct the sensitivity analysis, we calculate the sensitivity indicators of all the variables with (5.39). The calculated sensitivity indicators are listed in Table 5.3. The absolute values of all the sensitivity indicators are less than 1, i.e. 10%

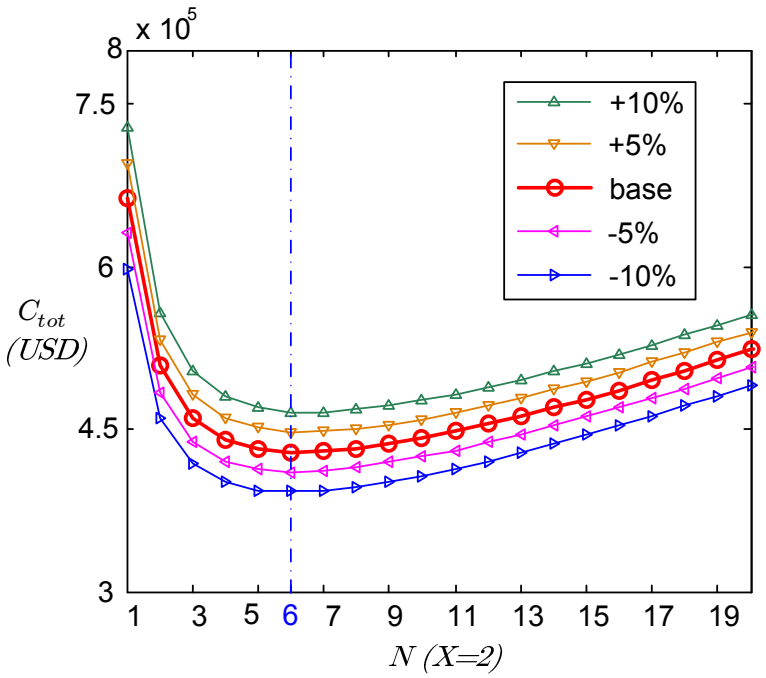


Figure 5.9: System Total Cost Curves vs. System Structure When System Power Rating Changes within 10%

change of each variable will lead to less than 10% variation of system total cost. Therefore, even the system parameter reflects slight variation, the system cost will still be minimized at $N = 6$, $X = 2$.

The SI values in Table 5.3 shows that the system cost is most sensitive to system power rating. Fig. 5.9 shows the system cost curves under various system power ratings. Within 10% variation of system maximum power rating, $N = 6$, $X = 2$ always gives the optimal structure.

Fig. 5.10 shows plots of system cost when inverter cost has up to 30% variation. Compared with the results shown in Fig. 5.9, Fig. 5.10 shows that the system optimized architecture will not be the same when parameter varies in a wide range. When inverter cost decreases 30%, parallel inverter modules N should be decreased

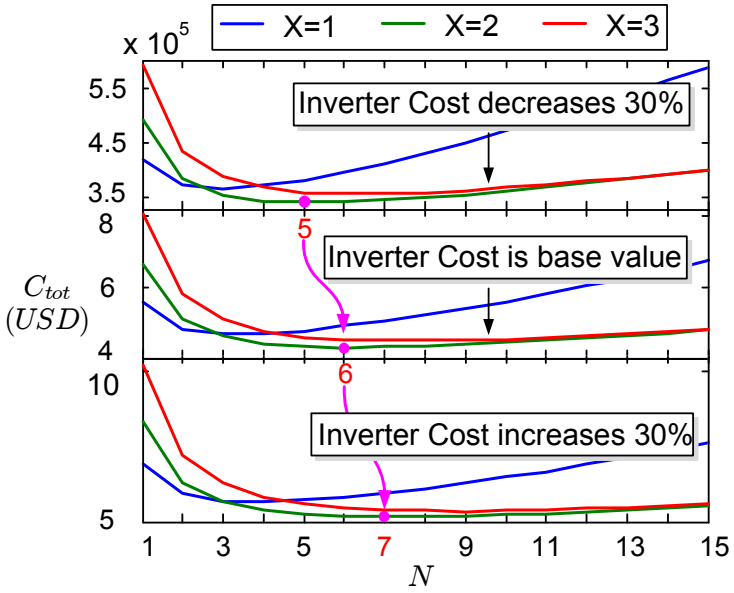


Figure 5.10: System Total Cost Curves vs. Inverter Cost Varies up to 30%

to 5 to minimize system total cost; When inverter cost increases 30%, parallel inverter modules N should be increased to 7 to achieve optimization. Therefore, for a parallel redundant inverter system, if inverter cost varies up to 30% during operating time, for the system structure, N can be chosen from 5 to 7. Such multiple points optimization of the system cost can also be conducted when other variables fluctuate in a wide range following the same methodology. This is not a complete optimization, but just shows how cost variations impacts parallel connections. For complete optimization, the variation range of all parameters need to be considered.

5.7 Power Density Comparison

Compared to single inverter system, a potential benefit brought by redundant parallel inverter system is the possibility of achieving compact design and high

power density. Many companies have adopted paralleling modular inverters to significantly improve the system power density as shown in Fig 5.11 [134]-[136]. The system is mounted by modular inverter racks and each rack has its own cooling system. Such design not only reduces the system volume significantly but also facilitates system power level upgrade.

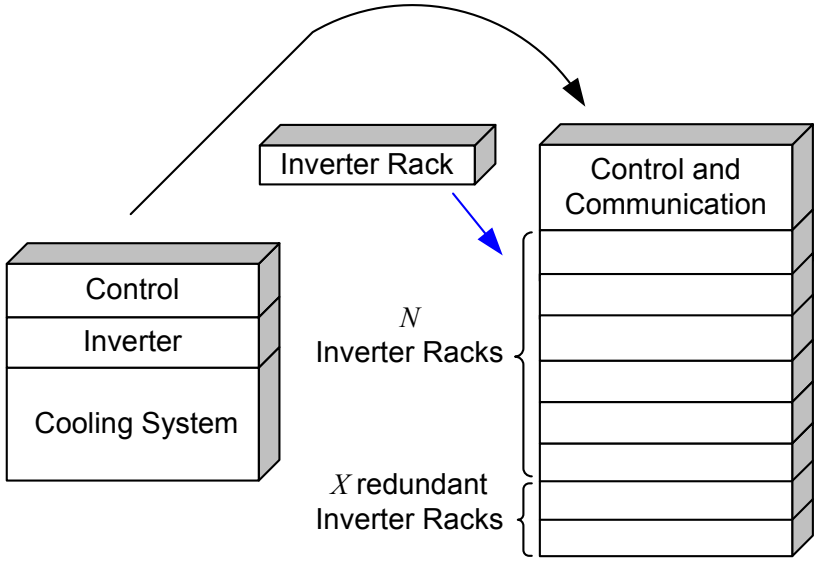


Figure 5.11: Rack Mounted Parallel Modular Inverter System

The system volume of the rack mounted redundant parallel inverter system in Fig. 5.11 is equivalent to:

$$vol_{tot} = vol_N + vol_X + vol_e \tag{5.40}$$

$$= vol_N + \frac{vol_N}{N}X + vol_e \tag{5.41}$$

where vol_{tot} is the system volume; vol_N is the volume of the major N inverter racks in parallel; vol_X is the volume of the backup X inverter racks; and vol_e stands for the volume of system controller, package, wiring and circuit breakers.

In order to quantify the effect of redundancy on the rack stacked system power

density as shown in Fig. 5.11, we take the 100 kW system as an example. Provided the power density of PWM inverter module is approximately $1MW/m^3$ [136]-[138], the volume of the inverter stack is

$$vol_N = \frac{100kW}{1MW/m^3} = 0.1m^3 \tag{5.42}$$

Assuming vol_e is $0.02m^3$, around 20% of the 100 kW inverter stack volume, the whole system volume becomes

$$vol_{tot} = (\frac{0.1X}{N} + 0.12)m^3 \tag{5.43}$$

Let the system volume under $N = 1$, $X = 1$ be the base case,

$$vol_{tot,N=1,X=1} = 0.22m^3 = 1pu \tag{5.44}$$

the system volumes under different parallel redundant structures are plotted as shown in Fig. 5.12. The system volume decreases as N increases and X decreases. For example, when $N = 6$, the system volume increases 10% when the number of redundant inverter racks X increases from one to two. Since system power density is equivalent to P_o/vol_{tot}, system power density decreases 10% when X increases from 1 to 2; however, system failure rate is decreased 40% and system total cost reduces 13.9% according to calculations following (16), (39). Therefore, properly increasing the degree of redundancy maximizes the system reliability and minimizes system cost as proven in previous two sections.

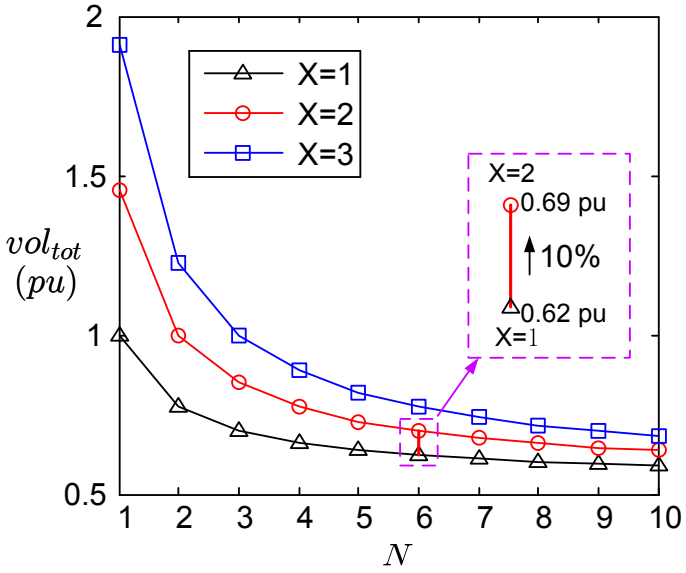


Figure 5.12: Redundant Parallel Inverter System Volume under Different Degree of Redundancy

5.8 Summary

This chapter proposes mathematical models for reliability and cost evaluation of single and parallel inverter systems. The reliability models of parallel inverters under different architectures and control strategies are developed. With the reliability and cost models, a novel methodology to determine the system architecture to optimize system reliability and cost is proposed. The cost analysis and reliability results show that dynamic power distribution control scheme achieves higher reliability and lower operational cost compared to conventional average current sharing control method. Sensitivity analysis is carried out to investigate the influence of parameter variation on derived system reliability and cost models. At last, power densities of various system architectures are compared.

Chapter 6

Wireless Droop Control of Distributed Generators in a High Power Microgrid

6.1 Introduction

In previous two chapters, extensive analysis and investigation have been conducted on parallel operation of the inverter interface of microgrid. Though cost effective and high performance, the proposed dynamic distribution scheme has constraint on the control system interconnection of individual inverters. For distributed generators located in a wide range in high power microgrid, control communication or interconnection might not be easily accessible.

In this chapter, a hybrid control architecture is proposed to control the interfacing inverters of a low voltage microgrid. The inverters are divided into several blocks according to their geographic location. To automatically distribute power among the inverter blocks, wireless droop control method is applied. For inverters located in the same block, the proposed dynamic power distribution control method

is applied to balance their output power and optimize the system efficiency. In this hybrid control architecture, the droop control is modified from the conventional one according to the line impedance characteristics of LV microgrid. A simplified virtual impedance method is used to improve the power balance accuracy. Such modified droop control scheme offers both good steady state and dynamic performance even when the paralleled inverters have large impedance mismatch. In addition, it does not require complex computations.

6.2 Literature Survey

Although droop control does not ensure constant frequency and amplitude of microgrid voltage, the advantage in avoiding control interconnections makes it a competitive solution for controlling high power microgrid inverters.

However, the resistive impedance characteristic of LV microgrid will affect the performance of conventional droop controller. In addition, the number of parallel inverters will influence the system stability and performance [100].

To adapt the droop control strategy to resistive LV microgrid, modified droop control methods have been widely published in literature [98], [139], [140]-[141]. The modifications basically focus on two aspects. First, to decouple the coupling terms between active and reactive power due to resistive impedance [140]. Second, to balance the power shared among paralleled inverter modules [98], [139], [141]. Due to the difficulties in impedance measurement and detection, the modified droop

control cannot totally decouple the active and reactive power. In addition, the decoupling process influences the accuracy in power sharing and introduces circulating current problem among paralleled distributed generators since virtual active and reactive power are controlled instead of the actual power components. In [141], a large virtual inductor is added to the inverter voltage control loop to change the inverter output impedance characteristic from mainly resistive to inductive. However, the large virtual inductor makes the output voltage of the inverter drop severely. To limit the voltage drop brought by the large virtual inductor, [139] proposes dynamic adjustment of the droop ratio to compensate for the voltage drop. Such method requires complex computations and impacts the system stability. [98] proposes to transform the P and Q in a rotating frame, by continuously adjusting the frame angle to achieve minimum output current and accurate power sharing. The slow dynamics caused by added minor current droop makes the scheme difficult to use in practice.

6.3 Proposed Hybrid Control Architecture for Distributed Interfacing Inverters of Microgrid

Fig. 6.1 shows the system configuration and hybrid control architecture of a distributed AC microgrid, which consists of various inverter interfaced distributed generators. According to the geographical location, the inverters are separated into blocks denoted by the dashline box in Fig. 6.1. For such inverter blocks

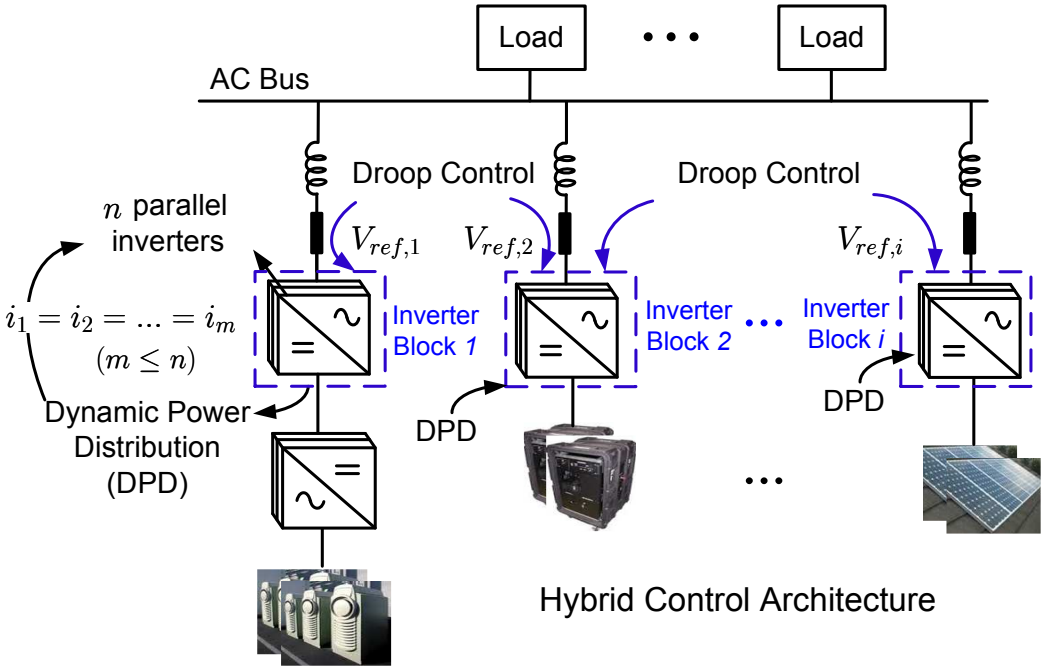


Figure 6.1: Distributed Low Voltage AC Microgrid with Hybrid Control Architecture

located physically apart, modified wireless droop control strategy is applied to achieve power balance. Inside each inverter block, the parallel inverters located near each other are controlled with dynamic power distribution scheme. The proposed dynamic power distribution scheme will facilitate the parallel inverters to achieve balanced power sharing as well as increased system efficiency.

In this hybrid control architecture, the droop control will generate the reference voltage $V_{ref,i}$ for each inverter block to achieve automatic power distribution. Inside the block, the dynamic power distribution scheme will selectively control m of the n paralleled inverters to operate according to the load condition. The output voltages of the m inverters are controlled to track $V_{ref,i}$, and power among the inverters are equally balanced, i.e. $i_1 = i_2 = \cdots = i_m$.

Table 6.1: Impedance Values for Overhead, Twisted A1. Cables

Cable Type	R (Ω/km)	X (Ω/km)	$\frac{R}{X}$
Twisted Cable, $4 \times 50mm^2$	0.642	0.1	7.7
$4 \times 120mm^2$	0.255	0.096	0.85
$4 \times 150mm^2$	0.208	0.096	0.31

6.3.1 Design of Primary Wireless Droop Control of Paralleled Inverter Blocks

The power flowing from each generator unit to the AC bus can be expressed as below [142]:

$$\begin{aligned} P &= (\frac{EV}{Z}cos\delta - \frac{V^2}{Z})cos\theta + \frac{EV}{Z}sin\delta sin\theta \\ Q &= (\frac{EV}{Z}cos\delta - \frac{V^2}{Z})sin\theta - \frac{EV}{Z}sin\delta cos\theta \end{aligned} \tag{6.1}$$

where δ is the power angle between the inverter output voltage E and AC bus voltage V; Z and θ are the amplitude and phase of the output line impedance.

Since the typical low voltage line impedance R/X ratio is around 7.7 as shown in Table. 6.1 [143], [144], we approximate θ to be 0 instead of $\frac{\pi}{2}$ in conventional droop control system design. With such approximation, (6.1) is simplified as [144]:

$$\begin{aligned} P &= \frac{V}{R}(E - V) \\ Q &= -\frac{EV}{R}sin\delta \end{aligned} \tag{6.2}$$

Fig. 6.2 shows the droop characteristic of LV microgrid. To maintain a large $\frac{R}{X}$ ratio to enhance the decoupled relationship between P and Q, virtual

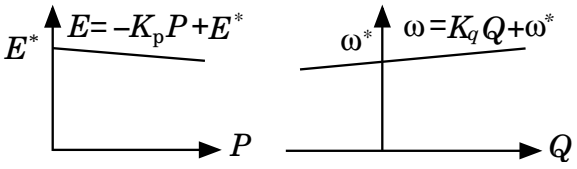
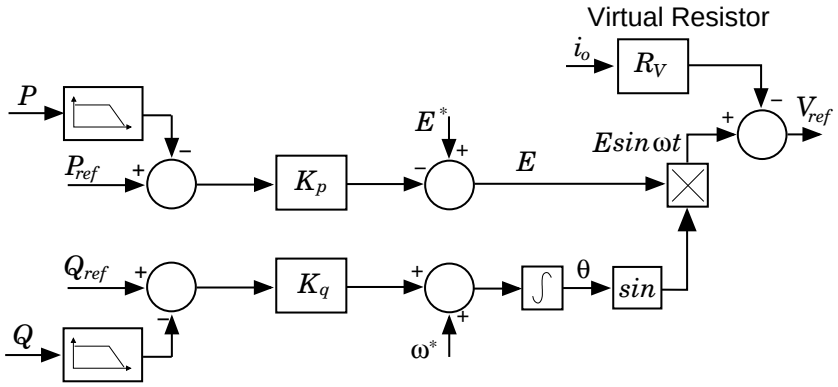


Figure 6.2: Droop Characteristics of LV Microgrid with Mainly Resistive Line Impedance



i_o is the output current of the inverter block

Figure 6.3: Proposed Droop Control Method for LV Microgrid

resistor method is used to improve the active power sharing [145]. The virtual impedance method has been reported with satisfactory performance in wireless droop control of paralleled DC/DC converters [146]-[149] and parallel inverters [145]. [145] proposes to design the virtual impedance for each major harmonic order current component separately. Such current component separation process greatly increases the computation complexity. In addition, the accuracy of the current components extraction will affect the current sharing accuracy and system stability. In this chapter, we propose a simplified approach to modify the droop control with virtual resistor method as shown in Fig. 6.3. The effect of virtual resistor is to subtract a small portion from the original output voltage reference. Therefore, it is important to design the virtual resistor R_V to not only improve the

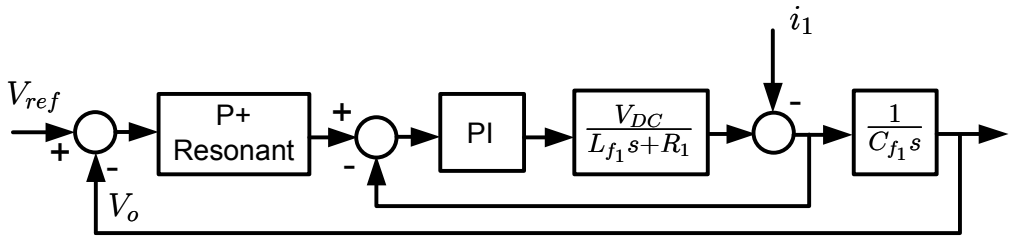


Figure 6.4: Cascaded Voltage Control Scheme to Interfacing Inverters

current sharing but also limit the voltage drop within small range. In this chapter, the virtual resistor is chosen to drop the output voltage within 5%. The generated V_{ref} is then sent to the control system of each inverter inside the inverter block.

The individual inverter is controlled with cascaded proportional resonant voltage control method as shown in Fig. 6.4 [59]. Resonant controller is used to replace integrator to achieve a high gain at 50Hz. The transfer function of PR controller is [59]:

$$G_{PR}(s) = K_P + \frac{K_R s}{s^2 + \omega^2} \tag{6.3}$$

The control parameters of the resonant controller are tuned following naslin polynomial approach [91]. With a switching frequency of 5kHz, the characteristic frequency of the control system is chosen to be 200Hz to ensure both the stability and fast dynamic response.

6.3.2 Proof of Stability

The root loci analysis of microgrid shows that the dominant poles are decided by the droop controller [145], [150], [151]-[153]. The droop controller obtains the

measured active and reactive power through a low pass filter as shown in Fig. 6.3. The voltage controller shown in Fig. 6.4 for fundamental and harmonic components has a high bandwidth. Therefore, the microgrid stability can be examined by analyzing the droop controller.

Linearizing the droop characteristic equation (6.2), we obtain:

$$\begin{aligned} \triangle P &= \frac{V}{R}\triangle E \\ \triangle Q &= -\frac{V}{R}(\triangle E \cdot \sin\delta + \triangle\delta \cdot E\cos\delta) \end{aligned} \tag{6.4}$$

Linearizing the droop controller proposed in Fig. 6.3, yields:

$$\begin{aligned} \triangle E &= -K_p \cdot P \cdot \frac{\omega_c}{s+\omega_c} \\ \triangle\omega &= s\triangle\delta = K_q \cdot Q \cdot \frac{\omega_c}{s+\omega_c} \end{aligned} \tag{6.5}$$

where ω_c is the cut-off frequency of the low pass filter. Substituting the expressions for $\triangle P$ and $\triangle Q$ in (6.4) to (6.5), the droop controller equations are derived as follows.

$$\begin{aligned} \triangle E &= -\frac{K_p \cdot \omega_c}{s+\omega_c}\frac{V}{R}\triangle E \\ \triangle\omega &= -\frac{\omega_c s}{s+\omega_c}\frac{V}{R}(\triangle E\sin\delta + \triangle\delta E\cos\delta) \end{aligned} \tag{6.6}$$

Solving (6.6), the system characteristic equation is obtained:

$$s^3 + \frac{\omega_c}{R}(2R + K_p V \cos\delta)s^2 + \frac{\omega_c}{R}(\omega_c + K_p\omega_c V \cos\delta + K_q V E \cos\delta)s + \frac{\omega_c}{R}K_q\omega_c V E(\cos\delta + \frac{K_p V}{R}) = 0 \quad (6.7)$$

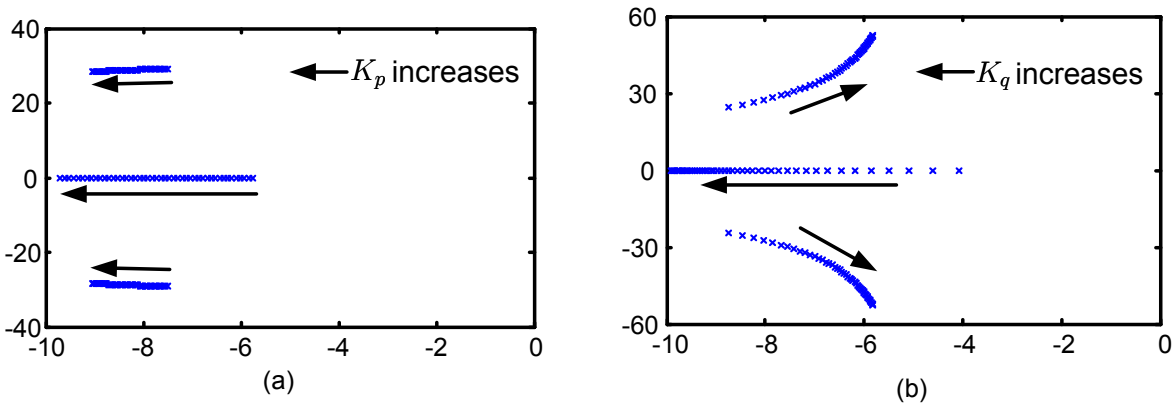


Figure 6.5: Root Loci of the Characteristic Equation (6.7): (a) $5 \cdot 10^{-5} \leq K_p \leq 5 \cdot 10^{-4}$, $K_q = 10^{-4}$ (b) $5 \cdot 10^{-5} \leq K_q \leq 5 \cdot 10^{-4}$, $K_p = 10^{-4}$

Fig. 6.5 shows the root loci of the system characteristic equation as K_p and K_q increase respectively. The stability of the system is proved as all the eigenvalues of the system characteristic equation are on the left handside of the plane.

The secondary control of the individual inverter within one block in a dynamic power distribution fashion has been discussed in Chapter IV, which is not duplicated here.

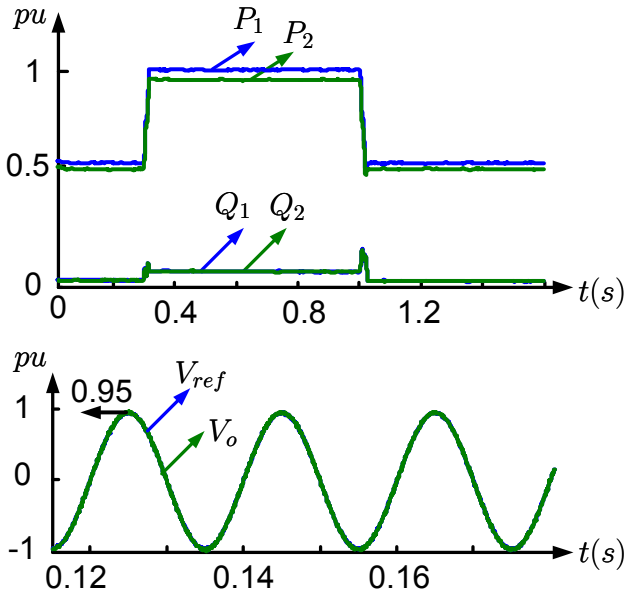


Figure 6.6: Simulation Results of Proposed Droop Control Method in Sharing Power among Two Inverter Blocks

6.4 Simulation Results

Fig. 6.6 shows the simulation results of two paralleled inverter blocks in an islanded microgrid controlled by proposed droop control method. The output impedance parameters, as shown in Table. 6.2, are set according to the typical low voltage line parameters provided in [143]. The line impedance of the two inverters have 50% mismatch. It is clearly seen that the proposed droop control method achieves satisfactory power sharing and smooth transient performance. In Fig. 6.7, the proposed droop control shows accurate power sharing performance in controlling paralleled inverter blocks feeding nonlinear load in LV microgrid.

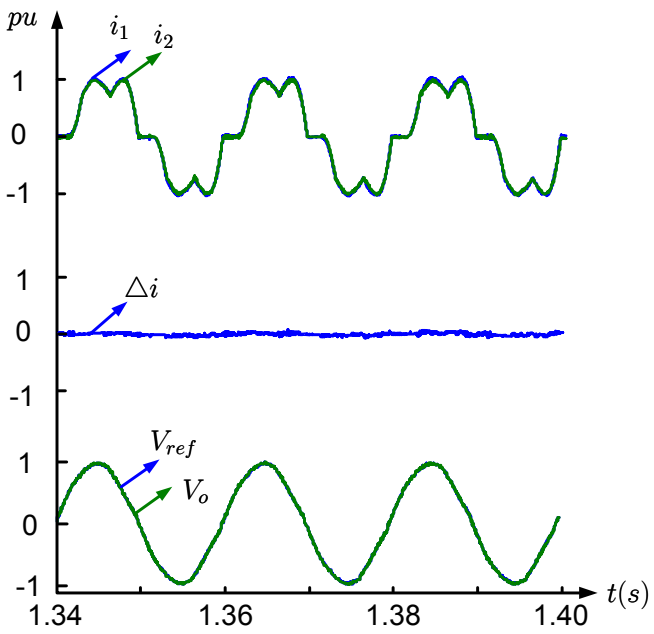


Figure 6.7: Simulation results of paralleled inverter blocks feeding nonlinear load in LV microgrid with proposed droop control method

Table 6.2: Impedance parameters of the two paralleled inverter blocks controlled by droop schemes

Impedance	L	R
inv_1	$13\mu H$	0.02Ω
inv_2	$26\mu H$	0.04Ω

6.5 Hardware in the Loop Testing Results

The hardware in the loop setup is the same as shown in Chapter IV. As Fig. 6.8 shows, the hardware controller dSPACE, digitally implements the proposed hybrid control architecture. RTDS is used to simulate the microgrid with paralleled inverter blocks in real time. The locally measured voltage and current signals, v_1, v_2 and i_1, i_2 of the two inverter blocks are sent to dSPACE. To prevent possible interference between digital controller and RTDS, isolation amplifier is implemented

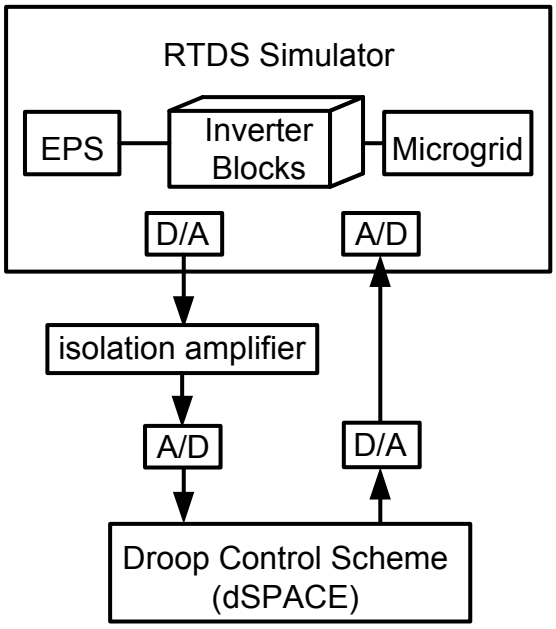


Figure 6.8: Diagram of "Hardware in the loop" System Setup to Validate the Proposed Hybrid Control Architecture

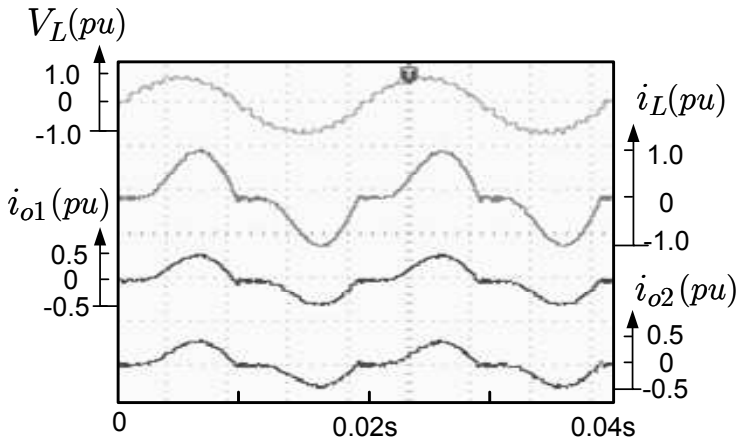


Figure 6.9: Real Time Test Results of the Steady State Performance of the Proposed Modified Droop Control in Controlling two Paralleled Inverter Blocks with 50% Line Impedance Difference

in between. With the measurement signals, the dSPACE calculates the voltage reference signals for the inverter blocks, V_{ref_1} and V_{ref_2}. With the voltage reference signals transmitted from dSPACE, the controllers of inverters located inside the inverter block will generate the PWM signals with the internal cascaded voltage controller. Fig. 6.9, 6.10 show the steady state and dynamic performance of the proposed droop scheme in controlling two paralleled inverter blocks feeding nonlinear load in a low voltage resistive microgrid. The modified droop control scheme demonstrates the ability to achieve balanced power sharing control despite the 50% impedance mismatch of the two inverter blocks.

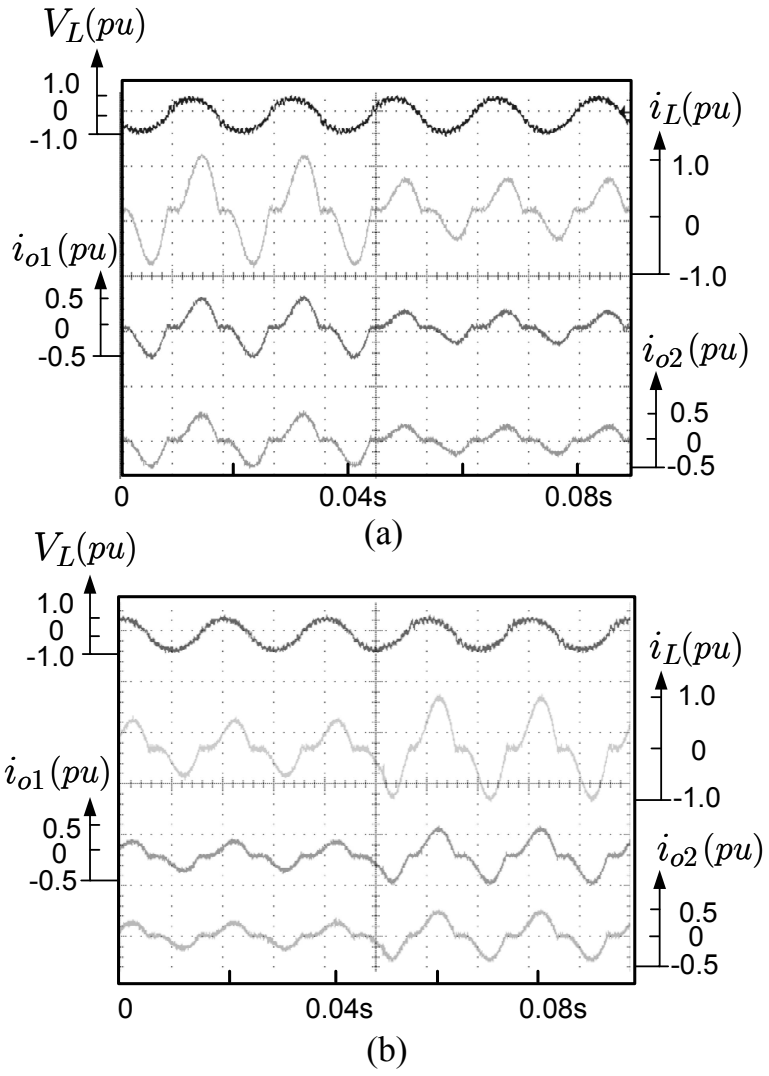


Figure 6.10: Real Time Test Results of the Dynamic Performance of the Proposed Modified Droop Control in Controlling Two Paralleled Inverter Blocks with 50% Line Impedance Difference: (a)Load Increases from 50% to 100%,(b)Load Decreases from 100% to 50%

6.6 Summary

This chapter proposes a hybrid control architecture for the parallel interfacing inverters of distributed generators in a low voltage islanded microgrid. The inverters are divided into blocks according to their geographical location. To control the power sharing of inverter blocks located in wide range, a modified droop control method with virtual resistor scheme is applied. For paralleled inverter modules placed within one block, dynamic power distribution strategy is used to increase the system operating efficiency and life span. The stability of the proposed hybrid control architecture applied to n paralleled inverters in low voltage microgrid is proved. Both simulation and real time test results demonstrate the viability of the proposed control strategies.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

Microgrid is a systematic approach to interconnect renewable energy resources, energy storage and loads within a certain area. Microgrid has distinct advantages over traditional power system infrastructure which makes it a preferred paradigm of distribution power system for future smart grid. Compared to conventional distributed power systems, microgrid has unique features in operating scenarios, system architecture, control structure and protection scheme. The thesis focuses on real time control strategies to achieve efficient and effective energy management of microgrid. In addition, the thesis investigates design, control and implementing a modular intelligent power electronics interfacing system to interconnect microgrid to electric power system.

The thesis first proposes a multifunctional power converter building block to interconnect microgrid to electric power system. A combined active and reactive power control strategy is applied to the power converter building block to achieve

energy management within microgrid. With the proposed control strategy, the microgrid is able to supply high quality power to electric power system, mitigate the harmonics from critical load and compensate the EPS voltage dip at PCC to maintain the voltage quality for local loads. In addition, the control system is capable of transferring the microgrid from connecting to EPS to autonomous island seamlessly when EPS experiences severe fault.

To realize the multiple functions of the interfacing inverter system of microgrid, control system design is important. The small signal modeling of the interfacing voltage source inverter is derived. In order to achieve high performance real time active and reactive power control, resonant controller with feedforward is applied. The grid synchronization requirements of distributed generation and microgrid from major international standards are investigated. To fast and accurately monitor the EPS voltage and frequency at PCC, adaptive PLL is employed to synchronize microgrid with EPS. The detailed modeling and controller design procedures for the multifunctional power converter building block are included in Chapter 2.

For high power microgrid connected to electrical power system, disconnection of microgrid from EPS might cause abundant generation loss. The sudden generation loss might lead to network instability. The grid code and international standards relevant to fault ride through requirements of distributed generators are investigated. In order to sustain the operation of distributed generators during EPS low voltage fault, the proposed power converter building block incorporates

fault ride through and fault current limitation techniques. Through comparing various alternative control strategies, a simplified fault ride through and fault current limited control strategy based on instantaneous power theory is proposed for the microgrid interfacing inverter. Chapter 3 presents the detailed system modeling, control and hardware implementation procedures. To test the system performance under unbalanced fault, a three phase four wire unbalanced grid emulator is implemented.

Power converter building block plays a key role to ensure the normal operation of microgrid under various operating scenarios. As the power level of microgrid increases, the power conversion system capacity must be increased as well. To expand the system power level, multiple interfacing inverters could be paralleled to feed the local load with power from DGs and ESS. The size and number of the power inverters required will depend on the fluctuating power flow within microgrid. Mathematical models of reliability and cost of parallel PCBB system are derived. A novel methodology to size the number of parallel inverters to achieve tradeoff between system reliability and cost is proposed. The parallel system efficiency, reliability and cost under different system architecture and control strategies are quantitatively evaluated and compared.

Since in practical applications, the output impedance of the parallel inverter modules are not possible to match exactly, an instantaneous error current correction control scheme is implemented to balance the power shared among parallel inverter modules. In addition, a dynamic power distribution strategy is proposed

to improve the light load efficiency and increase system life span. To validate the proposed dynamic power distribution scheme, a hardware in the loop testing system is implemented. The system setup and technical details are covered in Chapter 4.

To share the power among distributed generators located physically apart in microgrid, decentralized control without communication requirement is necessary. The thesis proposed a modified droop control strategy to share the load demand among inverter interfaced distributed generators in low voltage microgrid. Together with dynamic power distribution scheme, a hybrid control architecture is formed for the power conversion systems of microgrid. Chapter 6 presents the detailed design procedures of the proposed hybrid control scheme. Stability of the proposed wireless decentralized control scheme applied to n parallel inverters is proved. Hardware in the loop test results validate the scheme proposed.

It is believed that the models, methodologies, results and discussion presented in this thesis should assist researchers and engineers to implement the control and power conversion systems for microgrid.

7.2 Future Work

Regarding the real time controller design for islanded microgrid, this thesis assumed the loss of power supply probability is zero. For microgrid planning and sizing, the loss of power supply probability might not be zero in order to achieve

cost reduction and fuel minimization. The instantaneous power supply might not be sufficient to satisfy the load demand. Therefore, active load control is desired to conduct load shedding to maintain network stability. Combining demand dispatch and the proposed droop control scheme in Chapter 6 can improve the system reliability and increase the penetration of renewable energy sources for islanded microgrid.

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List of Publications

Journals

1. Xiaoxiao Yu and Ashwin M Khambadkone, "Reliability Analysis and Cost Optimization of Parallel Inverter System", *IEEE Transactions on Industrial Electronics*, Vol. 59, Oct. 2012, pp 3881-3889.

2. Xiaoxiao Yu, Ashwin M Khambadkone, Huanhuan Wang and Terence Siew, "Control of Parallel Connected Power Converters for Low-Voltage Microgrid-Part I: A Hybrid Control Architecture", *IEEE Transactions on Power Electronics*, Vol. 25, Dec. 2010, pp 2962-2970.

3. Huanhuan Wang, Ashwin M Khambadkone and Xiaoxiao Yu, "Control of Parallel Connected Power Converters for Low Voltage Microgrid-Part II: Dynamic Electro-Thermal Modeling", *IEEE Transactions on Power Electronics*, Vol. 25, Dec. 2010, pp 2971-2980.

Conferences

1. Xiaoxiao Yu, Ashwin M Khambadkone, Huanhuan Wang and Terence Siew, "A Hybrid Control Architecture for Low Voltage Microgrid", *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 2010.

2. Huanhuan Wang and Ashwin M Khambadkone, Xiaoxiao Yu, "Dynamic Electro-Thermal Modeling in Power Electronics Building Block (PEBB) Applications", *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 2010.

3. Xiaoxiao Yu, Huanhuan Wang and Ashwin M Khambadkone, "Control of Paralleled PEBBs to Facilitate the Efficient Operation of Microgrid", *IEEE International Symposium on Industrial Electronics (ISIE)*, July 2010.

4. Xiaoxiao Yu, Ashwin M Khambadkone and Huanhuan Wang "Control of Paralleled Power Converter Modules to Facilitate the Efficient Operation of Microgrid", *IEEE International Power Electronics Conference (ECCE Asia)*, June 2010.

5. Xiaoxiao Yu and Ashwin M Khambadkone, "Combined Active and Reactive Power Control of Power Converter Building Block to Facilitate the Connection of Micro-grid to Electric Power System", *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 2009.

6. Xiaoxiao Yu and Ashwin M Khambadkone, "Multi-functional Power Converter Building Block to Facilitate the Connection of Micro-grid", *IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Aug. 2008.