Low-Pass Sigma Delta Modulator for High Temperature Operation

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Summary

Low pass ΣΔ modulators have been applied in many applications primarily for digitizing analog signals from environment. Compared to Nyquist rate ADCs (analog-to-digital converter), ΣΔ ADCs have several advantages, such as high resolution and low process influence. On the other hand, in many industrial applications such as oil drilling process and hybrid vehicles, the electronic control circuits are required to operate at high temperature environment (typically above 200 ^{o}C), in which the commercial circuits are not capable of. This requires special design considerations dedicated for high temperature environment.

In this work, a design of 3rd-order ΣΔ modulator has been presented in details. It is capable to operate in high temperature environment (above 200 ^{o}C). The input signal bandwidth is 250 Hz and sampling frequency is 128 kHz. It applies switched capacitor CIFB architecture with additional feed forward path to minimize the signal swing of internal stages. Meanwhile, by applying several high temperature design techniques, issues caused by the decrease of mobility and threshold voltage have been resolved. Over the temperature range from 0 ^{o}C to 300 ^{o}C, the designed fully differential amplifier shows a steady gain above 63dB and the overall system achieves a steady SNR of 87 dB.

Acknowledgement

First of all, I would like to thank my supervisor, Professor Xu Yong Ping, for his valuable guidance and help during the course of this project. His expertise in circuit design and measure greatly helped me overcome the obstacles to accomplish this work. Thanks for all his effort in teaching and guiding me in the progress of this project.

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Chapter 1 **Introduction**

1.1 Background

In recent years, following the rapid development of semiconductor industry, electronics have been adopted in various applications. For typical applications such as consumer electronic products, home appliances, bio-medical devices and automated manufacturing machines, functional specific electrical systems are designed to monitor and control the operation. Generally, such systems sense the physical signals using a sensor and feed the sensed electrical signals to the processor. The processor processes the sensed data based on application specific algorithms and sends control signal to the actuator which performs the operation back [1]. This is explained in Figure 1-1.

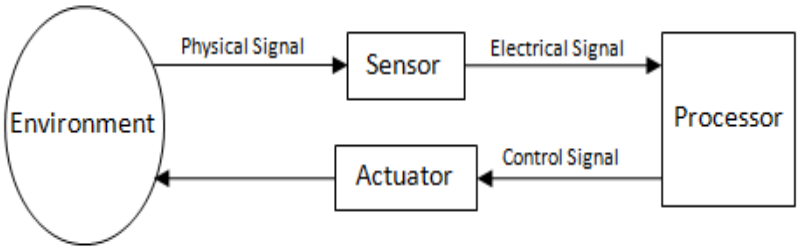


Figure 1-1 Electrical System

Among various steps in the process, sensing has always been a crucial step since the quality of the sensed data directly affects the system performance. Generally, for a sensor, the sensing quality is usually relied on an analog-to-digital converter(ADC), which converts the input signals(usually come in an analog format, such as sound, temperature, light and so on) into digital signals in order to be processed by the processor. In many applications, high resolution of A/D conversion is required, which leads to the promotion

of ΣΔ ADC. It applies ΣΔ modulation techniques and is able to achieve a resolution as high as above 16-bit ENOB [2].

On the other hand, operating temperature is a major limitation for the performance of electronic circuits that operate in harsh environments. This is because many physical parameters of silicon such as carrier concentrations and carrier mobilities, vary as temperature changes. This implies that electronic circuit is dedicated to operate within a pre-defined temperature range. Generally, for commercial electronic circuits, the operating temperature is within the range of 0 ^{o}C to 85 ^{o}C. For military applications, the operating temperature is within the range of -55 ^{o}C to 125 ^{o}C [3]. However, there is an increasing demand [4] [5] [6] of circuits which works in a wider temperature range. For example, in many industrial applications, such as oil drilling, aerospace and hybrid vehicles, circuits are required to operate in the temperature as high as above 200 ^{o}C [7], in which the available circuits are not capable of.

1.2 Thesis Organization

As motivated by the above mentioned demand of high temperature circuits, this work presents a switched capacitor based high temperature low pass ΣΔ modulator. Chapter 2 introduces the fundamentals of A/D conversion and the operational principle of ΣΔ modulator.

Chapter 3 studies the high temperature issues which may affect the circuit performance. Some effective high temperature design techniques are introduced to minimize the high

temperature effects. In addition, a study of SOI CMOS process fundamentals is also presented.

Chapter 4 introduces the fundamental concepts of switched capacitor circuits. The issues associated with CMOS switch are studied in detail. Techniques such as bottom plate sampling are introduced in order to minimize the non-ideal effects. Moreover, a switched capacitor based integrator is studied in details and the transfer function is derived.

Chapter 5 firstly reviews some previously reported designs and analyzes the pros and cons of individual design. Subsequently, a top-level design of high temperature low pass ΣΔ modulator is presented. With the proposed specification, the system level design and modeling is done using MatLab.

Chapter 6 presents the circuit level implementation of the low pass ΣΔ modulator. The details of every circuit block are shown together with the simulation results. In addition, the post-layout simulation result is shown. Discussion and analysis of the performance are also presented.

Chapter 7 summarized the major achievements of this work. Some suggestions on future improvement have been proposed.

Chapter 2 **Fundamentals of A/D Conversion and ΣΔ Modulation**

2.1 Concept of Sampling

An analog-to-digital converter is a circuit block that converts the continues-time (analog) signal into discrete-time (digital) signal. According to the Nyquist sampling theory, in order to reconstruct the input signal with no error, the sampling frequency f_s must be at least twice of the input signal bandwidth f_B, which is given by

$$f_s > 2f_B$$

The sampling frequency f_s, which equals to twice of f_B, is called Nyquist sampling rate. The Nyquist sampling theory can be explained in Figure 2-1. Theoretically, the input signal spectrum with bandwidth of f_B is shown in Figure 2-1a, which is symmetric about the y axis. After being sampled, the spectrum is copied and shifted to be centered at f_s, $2f_s$, $3f_s$ and so on as shown in Figure 2-1b. Therefore, for f_s less than twice of f_B, the two adjacent spectrums will overlap near the end of the band, which distorts the original signal spectrum. This is shown in Figure 2-1c. In this case, the original signal spectrum can never be reconstructed error-freely. This overlapping of spectrums is called aliasing. However, as shown in Figure 2-1d, when Nyquist sampling rate is used, there is an enough gap between two adjacent spectrums. It ensures that the signal spectrum is not distorted so that the original signal can be recovered by an anti-aliasing filter [8].

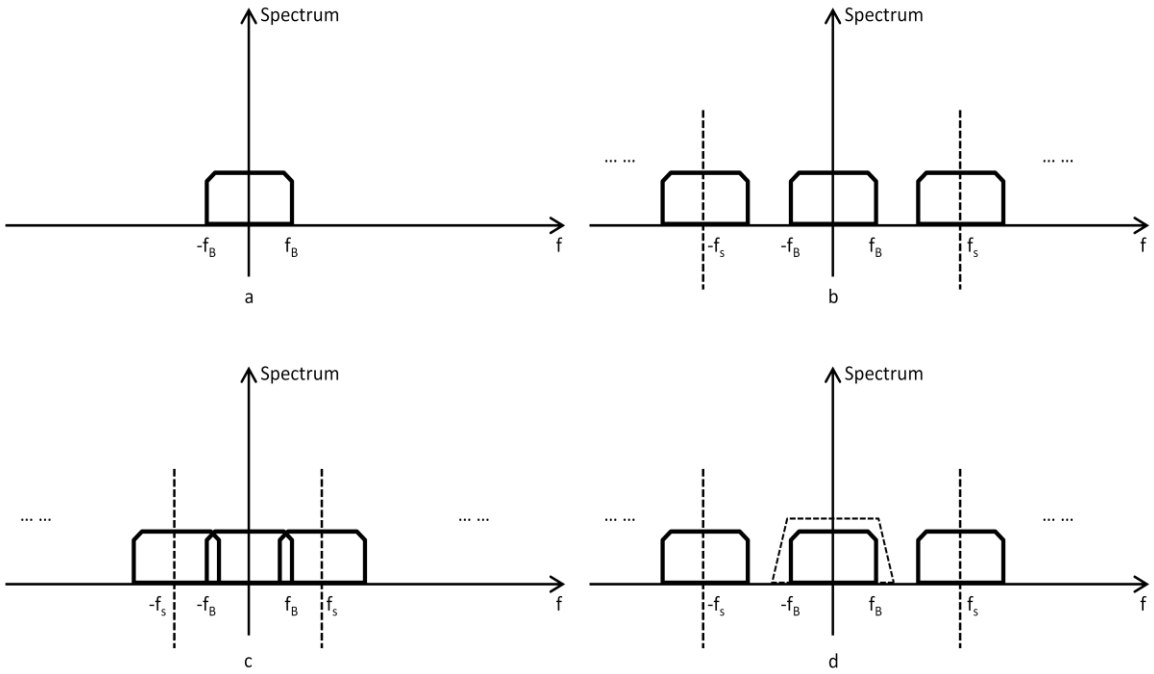


Figure 2-1 Nyquist Sampling Theorem

There are different types of ADCs. However, based on the sampling frequency, they can be divided into two categories, namely Nyquist rate ADCs and oversampling ADCs. For a Nyquist rate ADC, the sampling frequency is twice of the input single bandwidth. In real application, however, a sampling frequency slightly higher than Nyquist sampling rate is selected in order to ease the performance requirement of anti-aliasing filter. An example is shown in Figure 2-2.

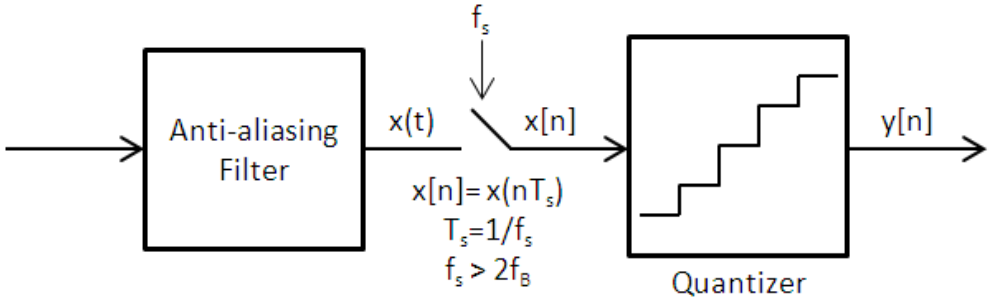


Figure 2-2 Nyquist Rate ADC

2.2 Quantization

Quantization is a process to convert the analog signal into digital signal, as depicted in Figure 2-2. For an N bit quantizer, the output signal can have 2^N levels as shown in Figure 2-3. However, since the quantization levels are discrete and finite, the quantization process is embedded with quantization noise. Generally, for an N bit quantizer, the step size can be expressed as equation (2.1) [9], which correspond to one LSB (Least Significant Bit). For large value of N, the step size can be approximated to $FS/2^N$. As shown in Figure 2-3, when the input analog signal sweeps from the minimum value to maximum value, the instantaneous quantization error ranges from -0.5LSB to +0.5LSB. As shown in (2.2), by applying a linear model of the quantization process, with input of *x*, the quantization error *e* is a simple addition to the output *y*. Hence, the quantization error is approximated as white noise with zero mean [10]. Therefore, the variance, which corresponds to the power of the quantization error, can be expressed as equation (2.3) [11]. Furthermore, for a full scale sinusoidal input, the peak SNR (signal to noise ratio) can be expressed as equation (2.4). As a key performance parameter of ADC, a high SNR has been a challenge for ADC design [9].

$$\Delta = \frac{FS}{2^n - 1} \approx \frac{FS}{2^n} \qquad (2.1)$$

$$y = kx + e \qquad (2.2)$$

Where

x is the input analog signal
k is the coefficient corresponding to the slope of line l as shown in Figure 2-3a
e is the quantization error
y is the output digital signal

$$P_n = \sigma_e^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \qquad (2.3)$$

$$SNR_{max} = 10\log\left(\frac{FS/8}{P_n}\right) \cong 6.02N + 1.76\ (dB) \qquad (2.4)$$

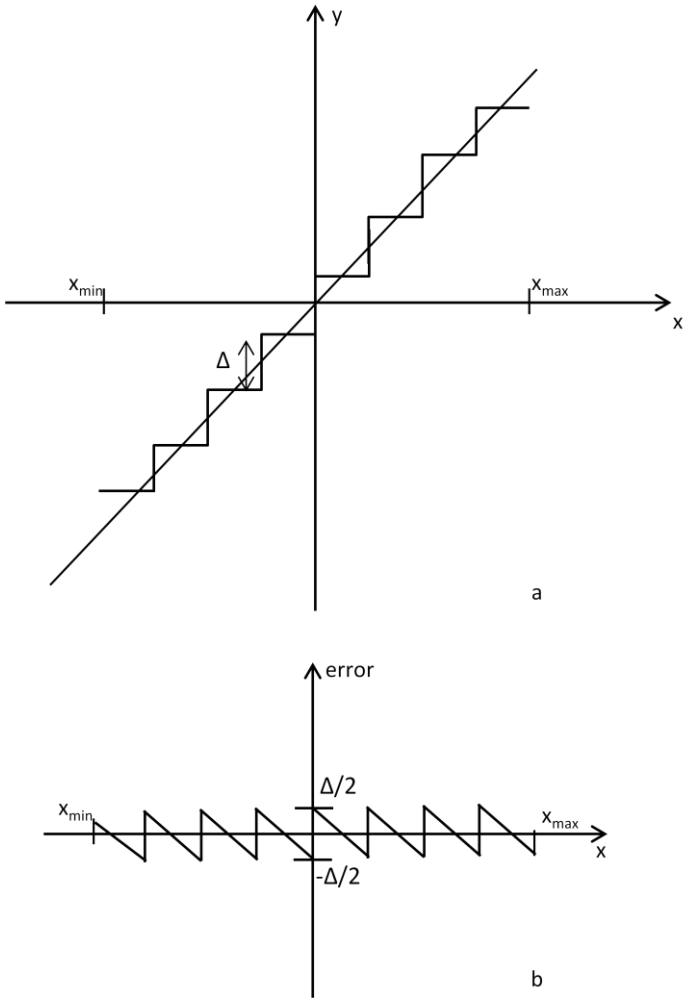


Figure 2-3 Concept of quantizer

2.3 Introduction to ADCs

2.3.1 Nyquist Rate ADC

There are many types of Nyquist rate ADCs. For example, flash ADC, as shown in Figure 2-4 [12], uses resistors chain to divide the reference voltage V_{ref} into eight voltages (0V, $V_{ref}/7$, $2V_{ref}/7$, $3V_{ref}/7$ … V_{ref}). If the input voltage is $0.5V_{ref}$, it is higher than $3V_{ref}/7$ and lower than $4V_{ref}/7$. Those comparators which connect to $V_{ref}/7$, $2V_{ref}/7$ and $3V_{ref}/7$ output 1 and the rest output 0. The encoder finally encodes the comparators output to binary code 3'b011.

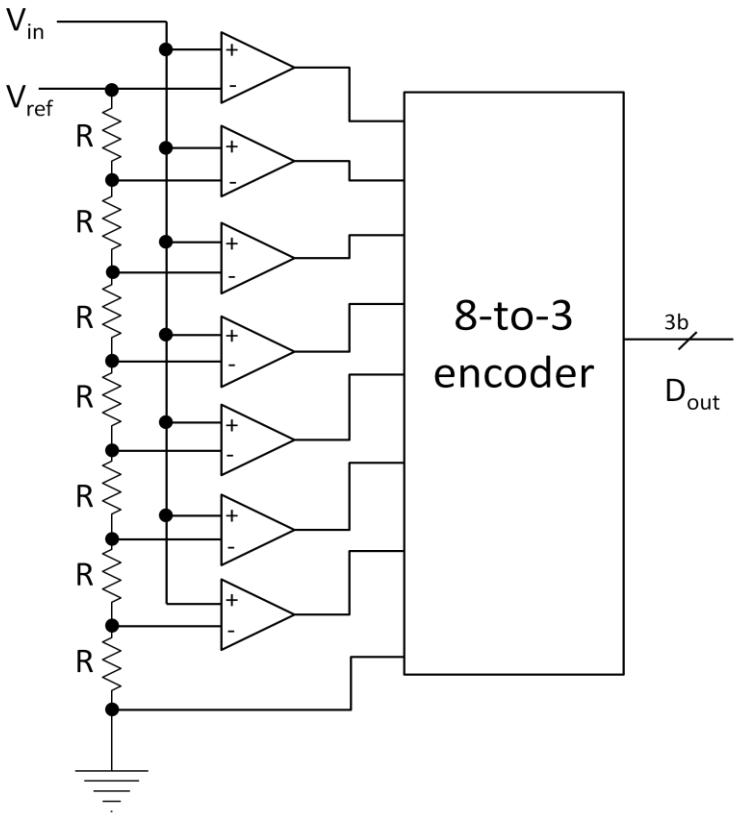


Figure 2-4 3-bit flash ADC schematic

In a practical flash ADC as well as other Nyquist rate ADCs, in order to achieve a good linearity and high SNR, the matching of the circuit elements (resistors, capacitors or transistors) must be accurate. However, due to some conditions, such as process variation and parasitic, the inaccuracy is limited to above 0.02%. In another word, the maximum achievable SNR is less than 80 dB.

2.3.2 Oversampling ADCs

An oversampling ADC samples the input signal at a frequency much higher that the Nyquist sampling rate. The OSR (oversampling ratio) is defined as equation (2.5). As depicted in Figure 2-5, the ADC samples the input signal at a frequency of f_s. After quantization and filtering, the output digital signal goes through a down-sampling process to Nyquist rate.

$$OSR = \frac{f_s}{2f_b} \qquad (2.5)$$

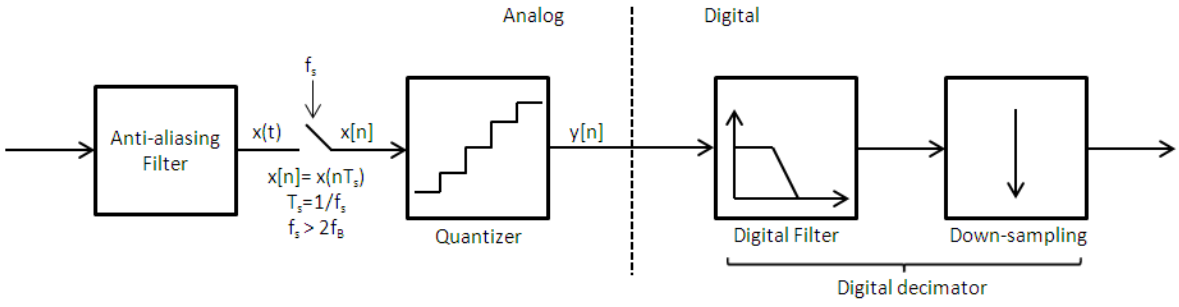


Figure 2-5 Oversampling ADC

The oversampling ADC with N-bit quantizer contributes the same total quantization noise power as a Nyquist rate ADC with a same quantizer does. As explained in Figure 2-6a, the

total quantization noise power is evenly distributed between $-f_B$ and f_B for a Nyquist rate ADC. Therefore, the in-band quantization noise power is equivalent to the total quantization noise power. As shown in Figure 2-6b, for an oversampling ADC, since the sampling frequency is increased to f_s, the same amount of total quantization noise power spreads from $-f_s$ to f_s. Therefore, the quantization noise level is lowered and the in-band quantization noise power is decreased. The in-band quantization noise power is expressed as equation (2.6). Hence, the SNR is derived as shown in (2.7). As a general rule of thumb, for every doubling of the OSR, the SNR increases by 3 dB (ENOB increases for 0.5b).

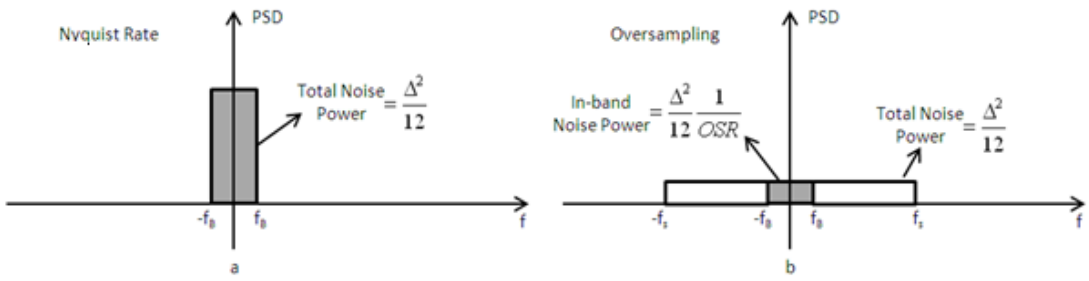


Figure 2-6 Quantization noise PSD of Nyquist rate (a) and oversampling (b) ADCs

$$P_{no} = \int_{-f_s}^{f_s} \frac{\sigma_e^2}{f_s} df = \sigma_e^2 \frac{2f_B}{f_s} = \frac{\Delta^2}{12}\frac{1}{OSR} \qquad (2.6)$$

$$SNR_{max} = 10\log\left(\frac{FS/8}{P_{no}}\right) \cong 6.02N + 1.76 + 10logOSR\ (dB) \qquad (2.7)$$

2.3.3 ΣΔ ADC

A ΣΔ ADC is built on top of oversampling ADC. The main difference is that the original quantizer is replaced by a ΣΔ modulator, as shown in Figure 2-7. Generally, a ΣΔ

modulator consists of a loop filter, a quantizer and a DAC (digital-to-analog converter). Instead of digitizing the input signal directly, it integrates (low pass filtering) the error between the input and output signals, digitizes the integrated signal and feedbacks to input again. A linear model of discrete-time ΣΔ modulator is shown in Figure 2-8.

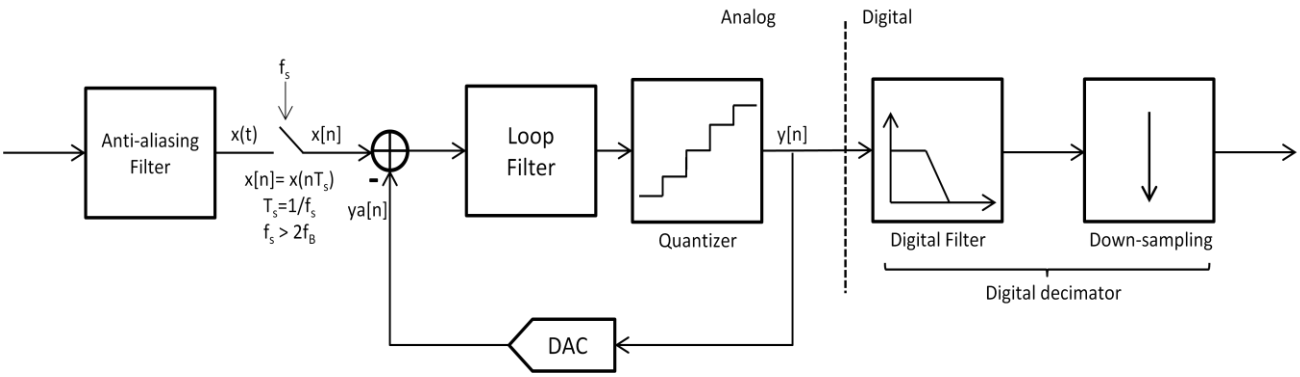


Figure 2-7 ΣΔ ADC block diagram

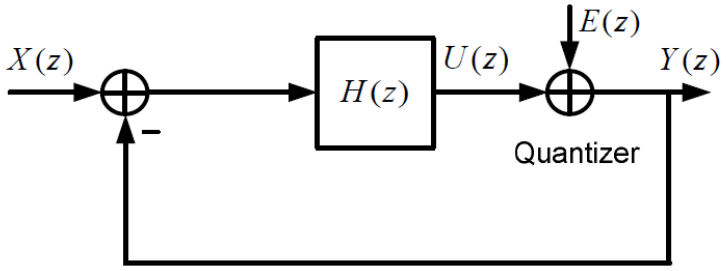


Figure 2-8 Linear model of ΣΔ modulator

$$Y(Z) = \big(X(Z) - Y(Z)\big) \times H(Z) + E(Z) \qquad (2.8)$$

$$=> \quad Y(Z) = \frac{H(Z)}{1 + H(Z)} X(Z) + \frac{1}{1 + H(Z)} E(Z) \qquad (2.9)$$

In this linear model, the loop filter's transfer function is H(Z). The quantizer is modeled as an ideal quantizer with quantization noise E(Z) as suggested in equation (2.1). The output

Y(Z) can be derived as shown in equations (2.8) and (2.9). The input signal component is multiplied by an $STF(Z) = \frac{H(Z)}{1+H(Z)}$ term, while the noise component is multiplied by an $NTF(Z) = \frac{1}{1+H(Z)}$ term. STF(Z) is referred to signal transfer function and NTF(Z) is referred to noise transfer function. In ideal case, if the gain of H(Z) is designed to be a large value, STF(Z) is approximated to be one and NTF(Z) is approximated to be zero. Therefore, during ΣΔ modulation, the noise component is suppressed and the signal component is maintained the same. This process is referred as noise shaping [13]. A comparison of Nyquist ADCs, oversampling ADCs and ΣΔ ADCs is shown in Figure 2-9 [14].

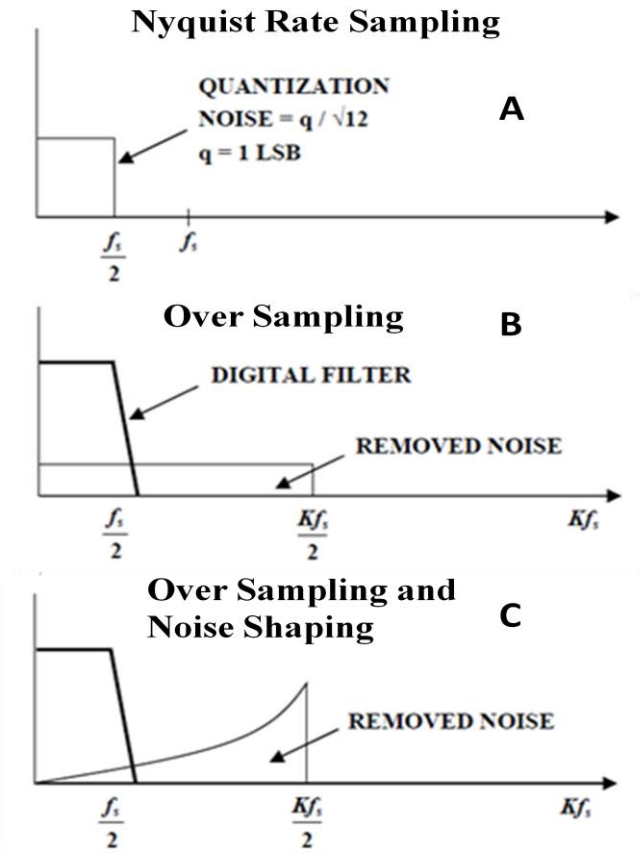


Figure 2-9 Comparison of Nyquist ADCs, oversampling ADCs and ΣΔ ADCs [14]

2.4 Fundamentals of ΣΔ modulator

For a 1st-order single loop ΣΔ modulator as shown in Figure 2-10, the loop filter H(Z) is simply an integrator with a pole at DC. By applying the linear model, the transfer function is shown in equation (2.10). For STF(Z) = Z^{-1}, the resulting input signal is delayed by one clock cycle. For NTF(Z) = 1- Z^{-1}(high pass filter), the low frequency noise is suppressed and the high frequency noise remains unchanged.

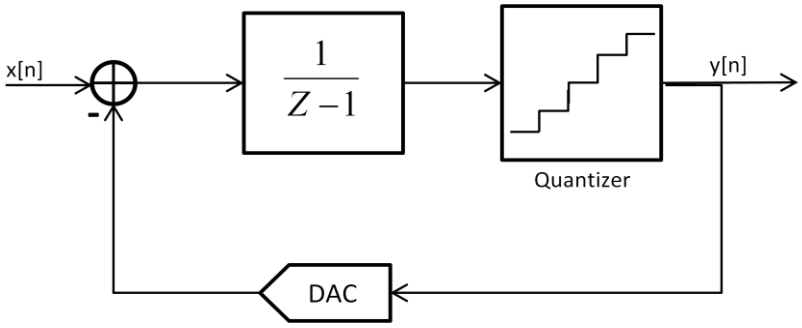


Figure 2-10 1st-order single loop ΣΔ modulator block diagram

$$Y(Z) = X(Z)Z^{-1} + E(Z)(1 - Z^{-1}) \qquad (2.10)$$

$$with\ STF(Z) = Z^{-1}\ and\ NTF(Z) = 1 - Z^{-1}$$

Noise shaping can be viewed as a process that transfers the low frequency band quantization noise into high frequency band, however, the total quantization noise power is maintained the same. Since the high frequency noise is out of signal band, after ΣΔ modulation, a decimation filter can be added to remove the high frequency noise component. The signal and in-band noise (been greatly suppressed) is preserved.

2.5 Parameters and Classification of ΣΔ modulator

2.5.1 Design Parameters of ΣΔ modulator

In order to characterize different ΣΔ modulators, several modulator-related parameters are proposed, namely OSR, order and quantization levels. OSR defines the sampling speed with respect to the input signal bandwidth. Intuitively, ΣΔ modulator periodically corrects the output by feeding back the sampled error between input and output signals. As a result, the average value of the output bit stream is converging to the input signal level. Therefore, a higher OSR implies that a larger number of cycles the system takes to correct the input. Hence, a longer bit stream is generated and a more accurate result is achieved. As discussed previously in equation (2.7), for every doubling of the OSR, the SNR increases by 3 dB.

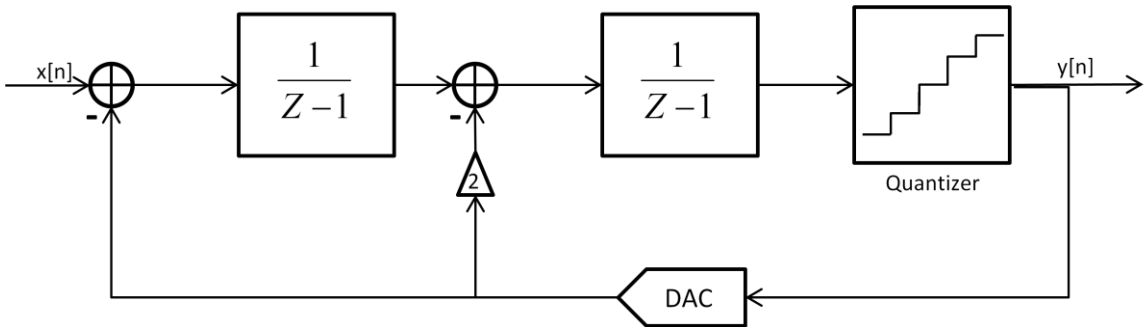


Figure 2-11 2nd order ΣΔ modulator block diagram

The order of a ΣΔ modulator corresponds to the order of NTF(Z). Figure 2-11 shows the block diagram of a 2nd-order ΣΔ modulator. The modulator transfer function is derived as shown in equation (2.11). A higher order of NTF(Z) implies a higher order of high pass filter, which suppresses the in-band quantization noise to a lower lever. Generally, for a L-th order modulator with NTF(Z) of $(1- Z^{-1})^L$, the total power of in-band quantization noise can be expressed as equation (2.12).

$$Y(Z) = X(Z)Z^{-2} + E(Z)(1 - Z^{-1})^2 \tag{2.11}$$

$$with\ STF(Z) = Z^{-2}\ and\ NTF(Z) = (1 - Z^{-1})^2$$

$$P_{no} = \int_{-f_B}^{f_B} \frac{\sigma_e^2}{f_s} |1 - Z^{-1}|^{2L} df = \int_{-f_B}^{f_B} \frac{\sigma_e^2}{f_s} \left| 2\sin\left(\frac{\pi f}{f_s}\right) \right|^{2L} df$$

$$\approx \sigma_e^2 \frac{\pi^{2L}}{2L+1} \left(\frac{2f_B}{f_s}\right)^{2L+1} = \frac{\Delta^2}{12} \frac{\pi^{2L}}{2L+1} \frac{1}{OSR^{2L+1}} \tag{2.12}$$

Thus, the peak SNR can be obtained as

$$SNR_{max} \cong 6.02N + 1.76 + (2L+1)10logOSR - 10\log\left(\frac{\pi^{2L}}{2L+1}\right)(dB) \qquad for\ N > 3 \tag{2.13}$$

If a single-bit quantizer (N=1) is used, the peak SNR is

$$SNR_{peak} = 1.76 + (2L+1)10logOSR - 10\log\left(\frac{\pi^{2L}}{2L+1}\right)(dB) \tag{2.14}$$

As shown in equation (2.13) and (2.14), for every doubling of OSR, the peak SNR increases by 3(2L+1) dB, corresponding to L+0.5 bit of resolution.

As shown in Figure 2-12 [15], for a 1st order ΣΔ modulator, from high frequency to low frequency, the quantization noise level is decreasing in a slope of -20 dB/decade. For a 2nd order ΣΔ modulator, the slope is -40 dB/decade. Generally, for an N-th order ΣΔ modulator, the slope is -20N dB/decade.

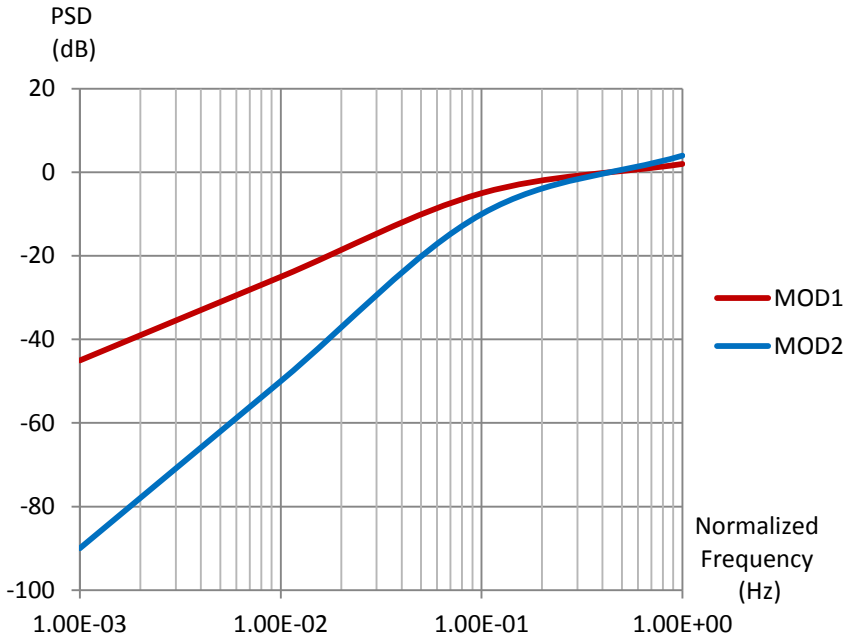


Figure 2-12 PSD of NTF (Z) for 1st-order (MOD1) and 2nd order (MOD2) modulators [15]

The quantization level is defined by the quantizer. An N-bit quantizer has a quantization level of 2^N. Generally, a quantizer with more quantization levels feeds back a more precise output to the input. Hence, the modulation is more efficient. As suggested by equation (2.13), an increase of 1 bit corresponds to 6 dB increase in the SNR. However, as the bit increased, the linearity of the quantizer may decrease, which results in a major trade off.

As shown in equation (2.13), different combinations of OSR, order and quantization level yield different SNRs. From system design point of view, the target SNR defines the requirement of OSR, order and quantization level. This can be explained in Figure 2-13 [16], which shows the limits of achievable SNR for various combinations of OSR, order and quantization level.

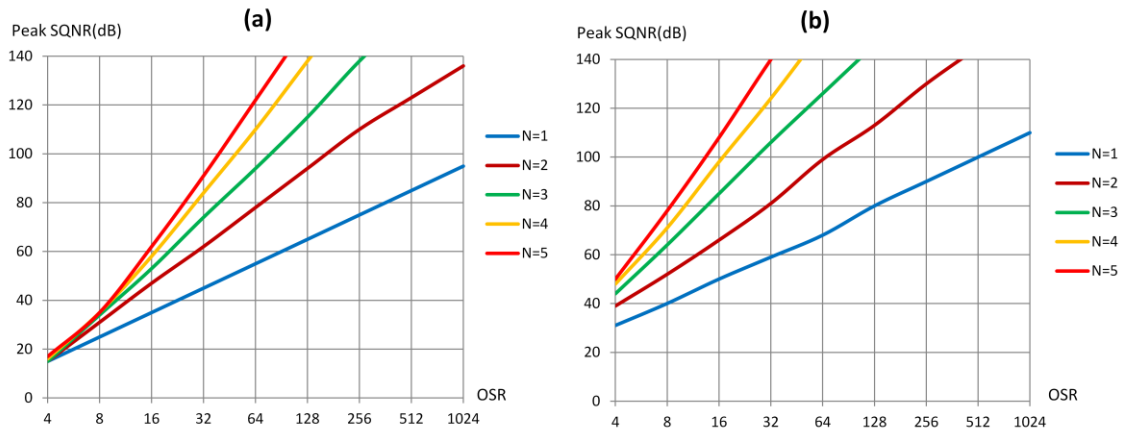


Figure 2-13 Empirical SNR limits for quantization bits =1 (a) and 2(b) [16]

2.5.2 Classification of ΣΔ modulator

ΣΔ modulators can be classified in many ways. Some commonly used criterions are listed down as shown in Table 2-1.

Table 2-1 Classification of ΣΔ modulators

Criterion	Classifications	
Sampling Method	Discrete-Time	Continuous-Time
Order	first order, second order… n-th order	
Quantization Bits	N=1, 1.5, 2 … n	
Loop Filter Type	Low Pass	Band Pass

2.6 Stability issue

In ΣΔ modulator, the traditional BIBO (Bounded Input, Bounded Output) criterion does not applied. This is because for a practical quantizer, the output is bounded by the supply rails. In the case of an unstable loop, the output becomes clipped. Generally, the stability

condition of a ΣΔ modulator depends on both the input signal and the order of the modulator.

For an ideal modulator, if the linearity of the quantizer is ignored, for a large input signal when the input of the first integrator is positive at every cycle, the output of the integrator keeps increasing without bound and the system becomes unstable [17]. This is illustrated in Figure 2-8, if

$$X(Z) - Y(Z) > 0 \qquad (2.15)$$

Then

$$U(Z) = H(Z)[X(Z) - Y(Z)] \to \infty \qquad (2.16)$$

Therefore, a stable system requires a limitation of input signal magnitude, which is called the stable input range. In normal modulator operation, the loop filter is required to remain linear and the quantizer is required to remain not severely overloaded. In practice, the stable input range is primarily determined by the NTF(Z) and the number of quantization levels.

On the other hand, the order of the modulator also affects the stability. For Figure 2-8, the loop filter's output U(Z) can be expressed as equation (2.17),

$$U(Z) = Y(Z) - E(Z) = STF(Z)X(Z) + [NTF(Z) - 1]E(Z) \qquad (2.17)$$

As the order L of NTF(Z) increases, a large gain of [NTF(z)-1] may occur, which leads to a huge amplification of quantization noise. As a result, the internal signal may change rapidly and oscillation may happen. Therefore, in order to obtain a stable operation of modulator, the NTF(Z) should be carefully designed.

To help determine the suitable NTF(Z) in order to meet the stability requirement, the Lee criterion [18] states

For a single bit ΣΔ modulator with an NTF(Z) is likely to be stable if

$$\max_{\omega}\left|NTF(e^{j\omega})\right| < 1.5 \qquad (2.18)$$

It is the most widely-used approximation criterion in determining the stability condition of the modulator. However, it is only an empirical conclusion which is neither necessary nor sufficient. It is used in the early modeling phase. The actually stable operating condition of the system requires to be verified by simulation.

2.7 Noise analysis

Noise is one of the major factors that affect the modulator's performance. In addition to the quantization noise introduced by quantizer, flicker noise and thermal noise are the primary sources of noise as shown in Figure 2-14.

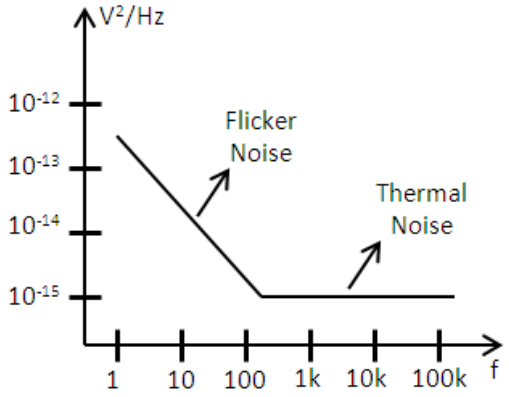


Figure 2-14 Noise PSD profile

2.7.1 Flicker Noise

Flicker noise is due to trapping and releasing of charge carriers when they move in the channel. It can be modeled as a voltage source connected in series at the gate. As shown in Figure 2-14 and equation (2.19) [19], the noise power is inversely proportional to frequency. It implies that most of the noise power is concentrated at low frequency [19].

$$S_{vf}(f) = \frac{K}{WLC_{ox}f}\left(\frac{V^2}{Hz}\right) \qquad (2.19)$$

To reduce flicker noise, one option is to increase the area of the transistor since the noise power is inversely proportional to the product of width W and length L. In some technologies, K of PMOS is smaller than that of NMOS. Therefore, PMOS transistor is more preferable to be used as input device. To further suppress flicker noise, techniques like correlated double sampling (CDS) and chopper stabilization can be applied. In most of the cases, these methods can reduce the flicker noise to a point where thermal noise becomes dominate. Hence, thermal noise is resulted to be the major contribution of noise.

2.7.2 Thermal noise

Thermal noise is resulted from the random fluctuation of current, which is caused by thermal motion of the charge carriers in the channel of devices. Thermal noise for a resistor or a MOSFET operating in triode region is approximately constant throughout the frequency spectrum. In practice, it can be modeled as a noise source in series of an ideal noise-free resistor as shown in Figure 2-15. The PSD of the noise voltage is expressed in equation (2.20) [19].

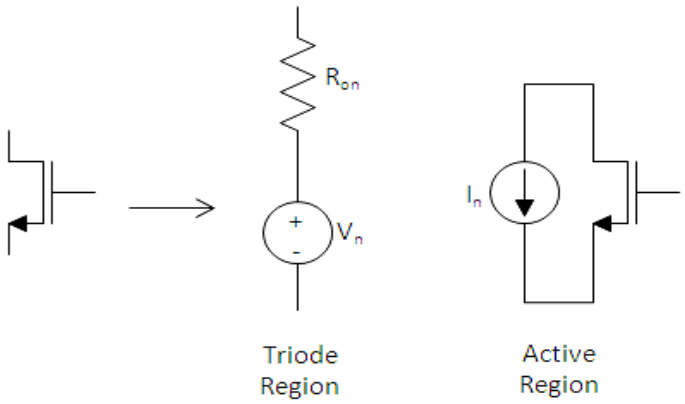


Figure 2-15 Thermal Noise Model of NMOS transistor

$$S_{vt}(f) = 4kTR_{on} \quad (V^2/Hz) \qquad (2.20)$$

For a MOSFET operating in active region, thermal noise can be modeled as a noise current source in parallel with a noise-free MOSFET as shown in Figure 2-15. The PSD of the noise voltage is expressed in (2.21) [19].

$$S_{it}(f) = \frac{8}{3}kTg_m \quad (A^2/Hz) \qquad (2.21)$$

2.8 Performance Metrics

SNR is one of the key performance parameters for all ADCs. The definition of SNR is shown in equation (2.22). This equation indicates that the peak SNR (highest achievable SNR) is achieved when the maximum input signal power is reached. However, the stability condition described in section 2.6 must be satisfied. In order to achieve a high SNR, the noise power must be reduced. This can be achieved by increasing the OSR and order of the loop filter as explained in section 2.5.

$$SNR = 10\log_{10}\left(\frac{\mathrm{P_{signal}}}{\mathrm{P_{noise}}}\right)\ (\mathrm{dB}) \qquad (2.22)$$

DR (dynamic range) measures the minimum detectable signal of an ADC. It is defined as the ratio of the largest achievable signal power to the smallest achievable signal power as shown in equation (2.23). The smallest achievable signal power is obtained when the signal level is the same as noise level. Furthermore, if the signal level is decreased below the noise floor, it is undetectable. Therefore, DR is directly related to the noise floor and hence the SNR. For an N-bit ideal ADC, DR is equal to SNR. In practical case, DR can be obtained from the plot in Figure 2-16.

$$DR = \frac{P_{max}}{P_{min}}\ (dB), where\ P_{min} = P_{signal} = P_{noise}\ (SNR = 0\ dB) \qquad (2.23)$$

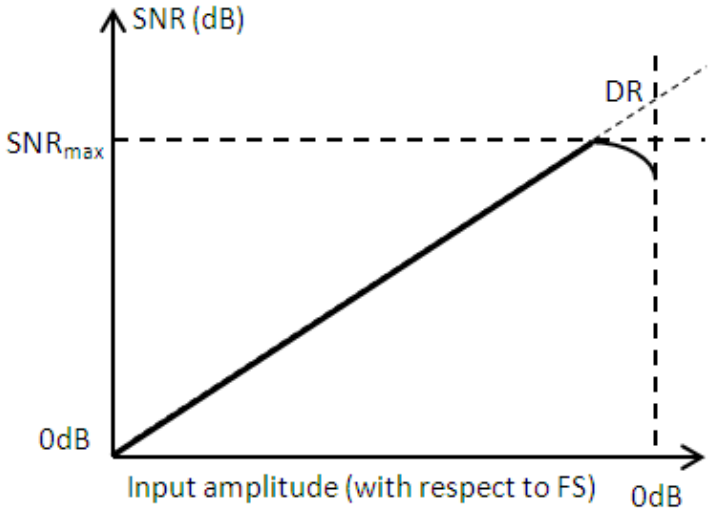


Figure 2-16 Definitions of maximum SNR and DR

ENOB (effective number of bits) measures the resolution of the ADC by specifying the output effective bits. It is defined as equation (2.24). This definition is applicable for all

types of ADCs. Hence, it is usually used to cross compare the resolution of Nyquist ADCs and ΣΔ ADCs.

$$ENOB = \frac{SNR_{max} - 1.76}{6.02}\ (bits) \qquad (2.24)$$

Harmonic distortion is known as those overtone signals with integer number multiples of signal frequency as shown in Figure 2-17. It is due to the non-ideality of the circuit blocks, such as the non-linear gain of amplifiers and insufficient settling time for the sampling capacitor.

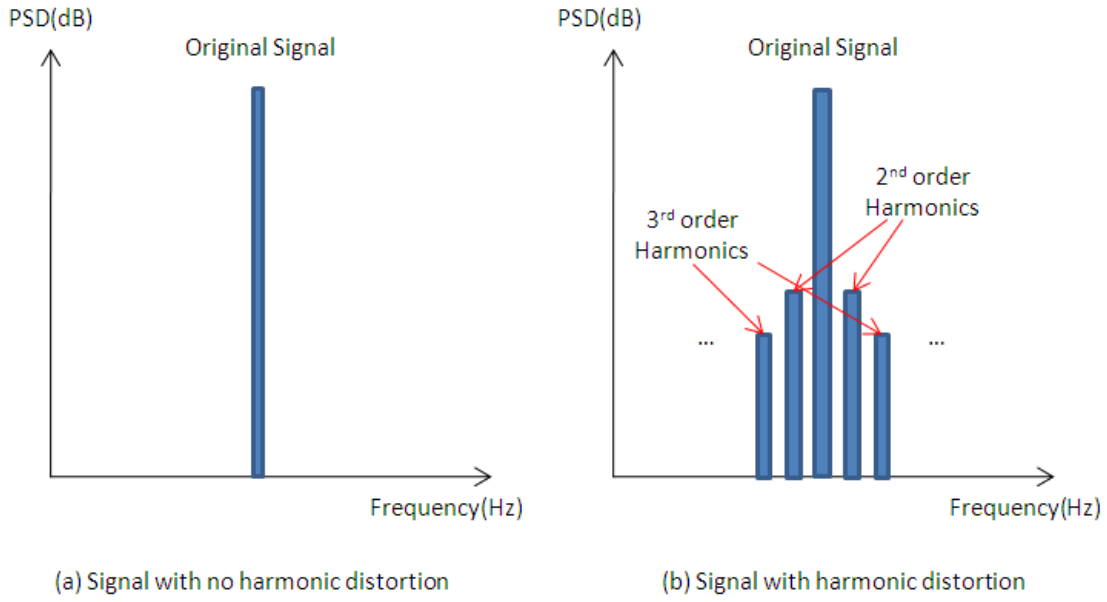


Figure 2-17 Harmonic distortion

Chapter 3 **High Temperature Circuit Design**

3.1 Background

In industrial applications such as offshore oil drilling, the operational temperature can be ranged from 0 ^{o}C to above 200 ^{o}C. The device physical behavior over such wide temperature range varies significantly, which may lead to circuit malfunction. There are primarily two temperature-sensitive parameters that affect the circuits. They are studied in details in this section.

3.2 Temperature Effect on Threshold Voltage

Threshold voltage is defined in equation (3.1) [20]. In this equation, many terms are related to temperature so that the relationship between threshold voltage and temperature is not clearly seen. A detailed analysis of every term is shown below [20]:

$$V_{th} = 2\emptyset_b + \frac{Q_b}{C_{ox}} + V_{fb} \qquad (3.1)$$

$$V_{fb} = \emptyset_{ms} - \frac{Q_{fc}}{C_{ox}} \qquad (3.2)$$

Q_b is the total charge stored in depletion layer. It can be expressed as equation (3.3).

$$Q_b = \sqrt{2\varepsilon_{si} \times q \times N_A \times 2\emptyset_b} \qquad (3.3)$$

Q_{fc} is the fixed charge due to surface states which arises from the imperfection in silicon oxide interface and doping. C_{ox} is the gate oxide capacitance. Hence, the Qss/Cox does not vary with temperature once the device is made.

Φms is the work function difference between gate material and substrate. It is defined as (3.4). Eg can be expressed as equation (3.5) [21]. Moreover, from the empirical data, Eg can be simplified as 3.6. For temperature above 300 K, the temperature dependence of Eg can be ignored since the variation amount is too small [21].

$$\emptyset_{ms} = -\left(\frac{E_g}{2q} + \emptyset_b\right) \qquad (3.4)$$

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \qquad (3.5)$$

$$E_g(T) = 1.165 - 5 \times 10^{-7} T^2 \ \ (T < 300℃)$$

$$or\ 1.205 - 2.829 \times 10^{-4} T \ \ (T > 300℃) \qquad (3.6)$$

Φ_b is referred as Fermi potential, which is the potential difference between the Fermi level and the intrinsic level of the device channel. It can be expressed as (3.7). n_i is the intrinsic carrier concentration which is expressed in (3.8). By substituting (3.8) into (3.7), a linear relationship between Φb and temperature can be obtained as (3.9).

$$\emptyset_b = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \qquad (3.7)$$

$$n_i = \sqrt{N_V N_C} e^{-E_g/2kT} \qquad (3.8)$$

$$\emptyset_b = \frac{kT}{q} \ln\left(\frac{N_A}{\sqrt{N_V N_C}}\right) + \frac{kT}{q} \times \frac{E_g}{2kT} = \frac{kT}{q} \ln\left(\frac{N_A}{\sqrt{N_V N_C}}\right) + \frac{E_g}{2q} \qquad (3.9)$$

Subsequently, the equation (3.1) can be expanded to (3.10) [22]. As shown in (3.10), two terms are associated with temperature, namely $\emptyset_b$ and $\sqrt{\emptyset_b}$. The term $\sqrt{\emptyset_b}$ can be ignored due to the value of the coefficient. Therefore, only $\emptyset_b$ term is associated with

temperature and hence a linear relationship between threshold voltage and temperature can be approximated. A simple simulation is carried out as shown in Figure 3-1. The plot matches with the approximation [22].

$$V_{th} = \emptyset_b + \frac{2\sqrt{\varepsilon_{si} \times q \times N_A \times \emptyset_b}}{C_{ox}} - \frac{E_g}{2q} - \frac{Q_{fc}}{C_{ox}} \qquad (3.10)$$

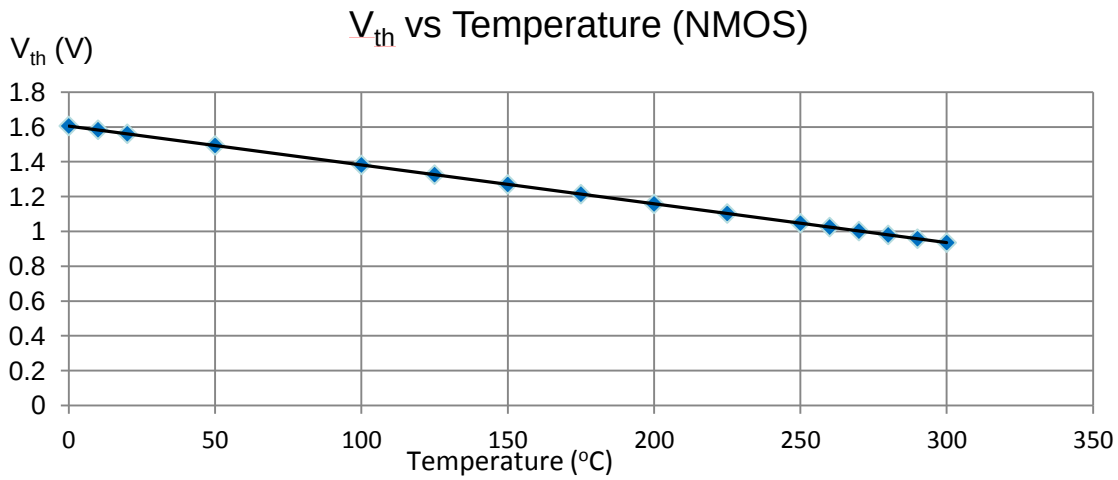


Figure 3-1 Simulation of V_{th} against temperature

Practically, the threshold voltage changes in a slope of -2 mv/ ^{o}C to -4 mv/ ^{o}C when temperature increases linearly. Quantitatively, the threshold voltage can be extracted from curve and expressed as equation (3.11).

$$V_{thn} = 2.216 - 2.235 \times 10^{-3}T \ \ (V) \qquad (3.11)$$

3.3 Temperature Effect on Mobility

Theoretically, electrons (holes) in a doped semiconductor at a certain temperature have thermal energies which allow them to travel in any direction. However, if an electric field

E is applied across the semiconductor, the free electrons (holes) are forced to move against (following) the direction of electric filed E. During the trip, the electrons (holes) accumulate momentum under a force F (F=-qE) during the mean free flight and loses momentum when they collide with an impurity atom or been scattered. By equating these two momentums, the drift velocity can be obtained as (3.12) [23].

$$-qE\tau_c = m_e v_d \qquad (3.12)$$

$$\mu_e = \frac{v_d}{E} = \frac{q\tau_c}{m_e} \qquad (3.13)$$

$$\mu_h = \frac{v_d}{E} = \frac{q\tau_c}{m_h} \qquad (3.14)$$

τ_c is the mean free time, which is defined as the average distance that a charge carrier travels before been scattered. m_e is the effective mass of electron. v_d is the drift velocity. Mobility is defined by the ratio of the drift velocity to the applied electric field as shown in (3.13) and (3.14). τ_c is primarily affected by two scattering mechanisms, namely the lattice scattering and impurity scattering.

Lattice scattering is the scattering of the charge carriers with atoms in a lattice. Theoretically, as temperature increases above 0 K, atoms which form the lattice start to vibrate and cause the variation of potential and emission of phonons. Phonons transfer energy between atoms and charge carriers. When temperature increases, the vibration becomes more intense. As a result, more phonons are emitted and the mobility is decreased.

Impurity scattering results from the ionized impurities (donors and acceptors). As the charge carrier travels through the lattice, it is deflected by the donors and acceptors due to the Coulomb force. The scattering effect depends on the speed of the charge carrier and the impurity concentration (doping concentration). As temperature increases, the speed of the charge carrier increases and also the impurity atoms are ionized. When temperature is above a certain value, the effect of impurity scattering becomes insignificant compared to lattice scattering.

As an overall effect, mobility decreases as temperature increases. Experimentally, the relationship between mobility and temperature is shown in equation (3.15) [24]. A simulation of mobility change against temperature is shown in Figure 3-2.

$$\mu_{eff}(T) \approx \mu_{eff}(T_0) \times \left(\frac{T}{T_0}\right)^{-1.5} \qquad (3.15)$$

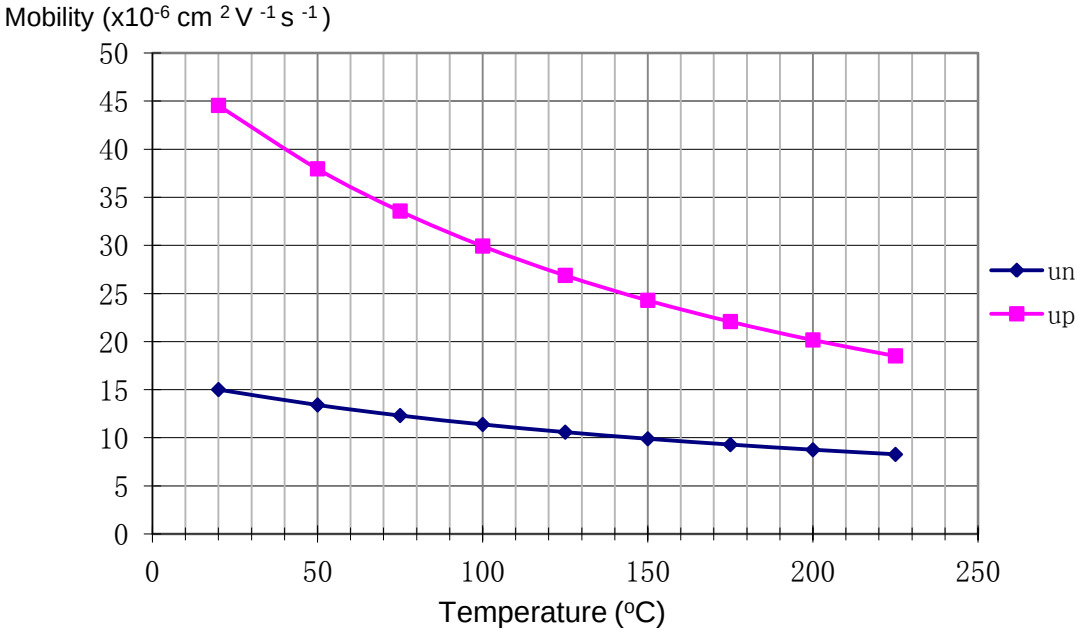


Figure 3-2 Simulation of mobility against temperature

3.4 Temperature Effect on Passive Components

Passive components, namely resistors and capacitors, are subject to the variation of temperatures. Their relationships with temperature are modeled using temperature coefficients as shown in equation (3.16) and (3.17) [25]. The temperature coefficients are subject to processes. In most of the cases, the 2nd-order temperature coefficients are too small and can be neglected. This results in the approximation of a linear relationship with temperature. Figure 3-3 shows a simulation of resistance against temperature [25].

$$R_T = R_{T_0} \times [1 + TC1 \times (T - T_0) + TC2 \times (T - T_0)^2] \qquad (3.16)$$

$$C_T = C_{T_0} \times [1 + TC1 \times (T - T_0) + TC2 \times (T - T_0)^2] \qquad (3.17)$$

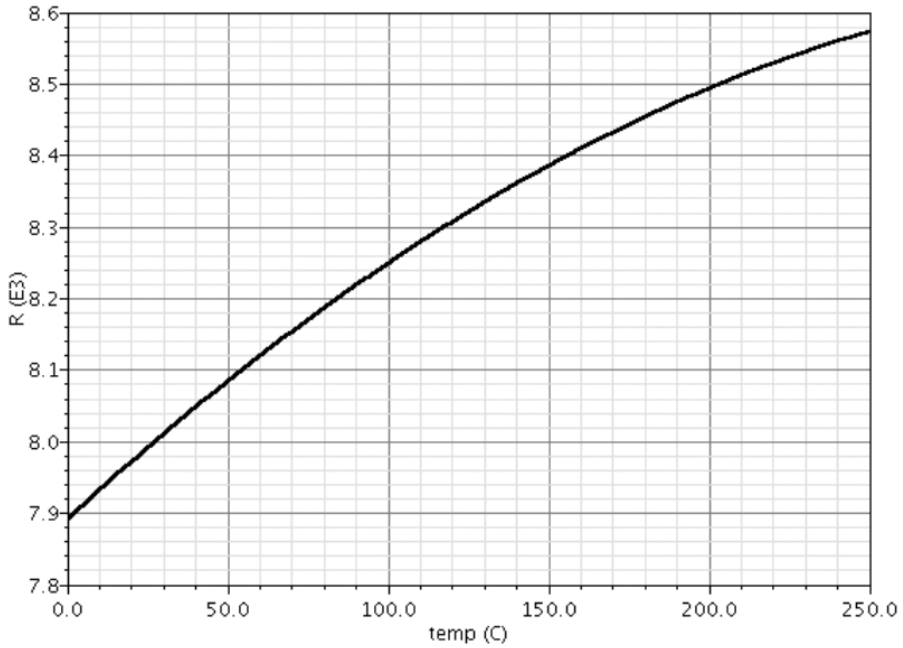


Figure 3-3 Plot resistance against temperature

3.5 SOI process

Silicon on Insulator (SOI) CMOS technology has been adopted from late 1990's. Unlike the conventional bulk CMOS process, SOI process employs a layer of electrical insulator

between the substrate and the silicon device layer as shown in Figure 3-4B [26]. This structural difference introduces several advantages compared to bulk CMOS as shown in Figure 3-4A, which significantly improves the performance of the circuits. Due to the existence of the insulator layer, the junction capacitance is gradually reduced as well as the leakage current. As a result, the power dissipation is reduced significantly. Meanwhile, the SOI structure isolates the device not only from the substrate, but also from each other. On contrary, the latch up problem in bulk CMOS process is resolved in SOI process since the bottom of the device is fully covered by insulator. This eliminates the substrate noise and crosstalk and improves the circuit performance, especially for analog circuits. Moreover, since the junction leakage has been significantly reduced, SOI based circuit is reported to be capable of operating in high temperature environment. Therefore, in this work, SOI CMOS process is chosen for design and fabrication [27].

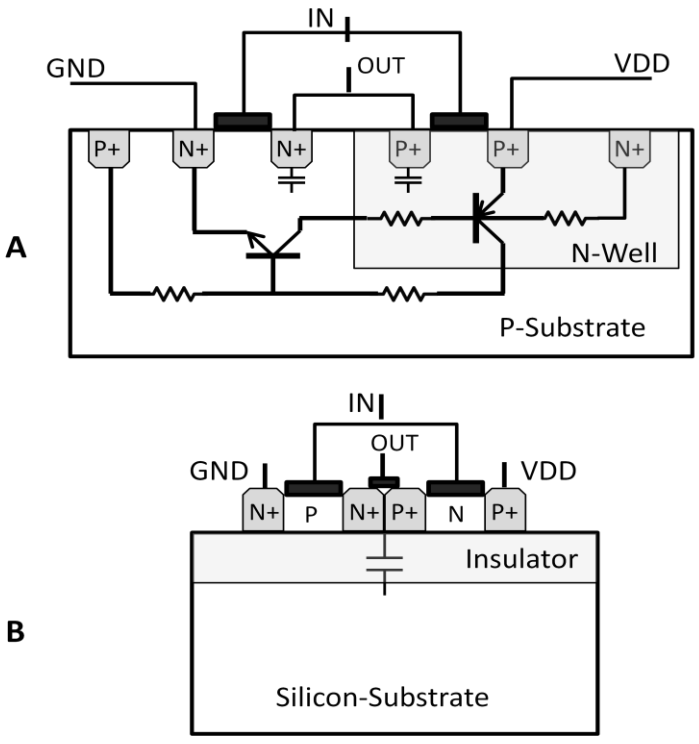


Figure 3-4 Cross section of bulk CMOS inverter (A) and SOI CMOS inverter (B) [23]

3.6 High temperature design techniques

As introduced in section 3.2 and 3.3, the decreases of threshold voltage and mobility are the major concerns for analog circuit design in high temperature environment. In Figure 3-1, when temperature changes from 0 ^{o}C to 200 ^{o}C, the threshold voltage decreases by over 60%. One challenge is that the biasing points of the transistors need to be carefully selected in order to maintain all transistors saturated. Moreover, as threshold voltage decreases, the overdrive voltage increases which leads to the quadratic increase of biasing current. On the other hand, the decrease of mobility against temperature increase is neither linear nor quadratic as shown in equation (3.15). This makes it difficult to develop compensation techniques. Since both threshold voltage and mobility change at the same time when temperature varies, it is difficult to eliminate the effects caused by the two parameters at the same time. Moreover, compared to threshold voltage which shows a linear dependence of temperature, the temperature dependence of mobility is neither linear nor quadratic. As a result, the compensation becomes difficult.

In this section, some high temperature design techniques are studied in details in order to resolve the high temperature issues.

3.6.1 Zero temperature coefficient biasing

As shown in Figure 3-1 and Figure 3-2, it is observed that, both the threshold voltage and mobility decrease while temperature increases. However, the decrease of V_{th} leads to the increase of drain current while the decrease of mobility leads to the decrease of drain current. Therefore, there should be a point where the two effects are cancelled and the drain current remains constant. Such a point is called ZTC (Zero Temperature Coefficient)

biasing point [28]. Figure 3-5 shows a plot from the simulation of the drain current by sweeping the gate voltage at different temperatures. The ZTC point is the intersection of all curves.

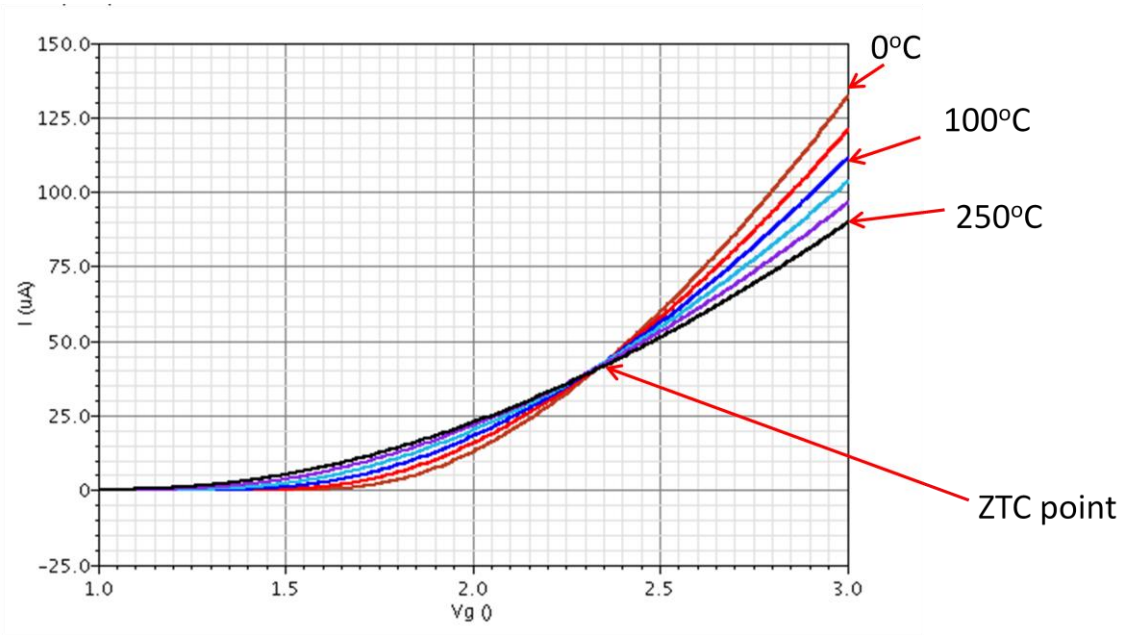


Figure 3-5 Simulated drain current under DC sweep of gate voltage at different temperatures

An analytical expression of ZTC biasing voltage is shown in equation (3.18). In this expression, p_0 and q_0 are the parameters extracted from equation (3.11). m denotes the power dependence of I_d with Vgs – Vth. When m = 1, the resulted Vgs (ZTC) corresponds to the ZTC biasing voltage in linear region. When m = 2, the resulted Vgs (ZTC) corresponds to the ZTC biasing voltage in saturation region. T1 and T2 correspond to the minimum and maximum temperatures of the operational temperature range. This expression is as good as an approximation which involves a least squares minimization. In practice, the calculated value of V_{gs} is accurate with maximum 10% error [28].

$$V_{gs}(ZTC) \approx -\frac{1}{6}p_0(T_1 + T_2) \times (2m - 3) + q_0 \qquad (3.18)$$

By applying ZTC biasing at gate, the estimated drain current can be expressed in equation (3.19) and (3.20) [28].

$$I_d(ZTC) \approx \mu_{eff}(T_0) C_{ox} \frac{W}{L} \times \frac{T_0}{1.5} p_0 V_{DS} \quad (linear\ region) \qquad (3.19)$$

$$I_d(ZTC) \approx \frac{1}{2} \mu_{eff}(T_0) C_{ox} \frac{W}{L} \times (\frac{mT_0}{1.5} p_0)^2 \quad (saturation\ region) \qquad (3.20)$$

Although ZTC biasing is effective in stabilizing the drain current against temperature variations, limitation has been found during applications. It is observed that the ZTC biasing voltage is usually much high than threshold voltage. For example, as shown in Figure 3-6, at room temperature, V_{th} is 1.5 V and the calculated V_{gs} (ZTC) is about 2.3 V. This leads to a large overdrive voltage and puts a limitation of high drain-source voltage V_{out} for saturation, which limits the output swing. Therefore, ZTC biasing technique is not applicable when large output swing for cascode stage amplifier is required.

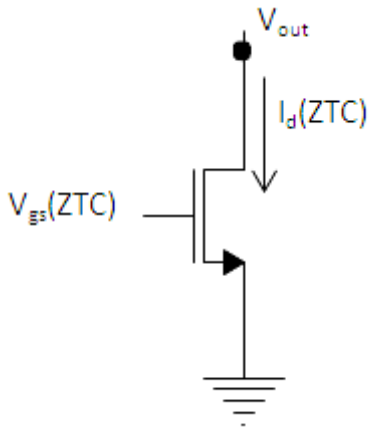


Figure 3-6 Transistor biased at ZTC biasing point

3.6.2 Constant gm (transconductance) biasing circuit:

Besides the ZTC biasing technique which provides a constant current over the temperature range, constant gm biasing is another effective method in high temperature circuit design. In this technique, instead of generating a temperature independent current, a constant gm is more of the interest for stable amplifier AC performance over the temperature range.

The constant gm biasing circuit is shown in Figure 3-7 [29]. It comprises of two PMOS transistors (M3 and M4) and two NMOS transistors (M1 and M2). M1 and M2 are connected in current-mirror configuration which gives (3.21).

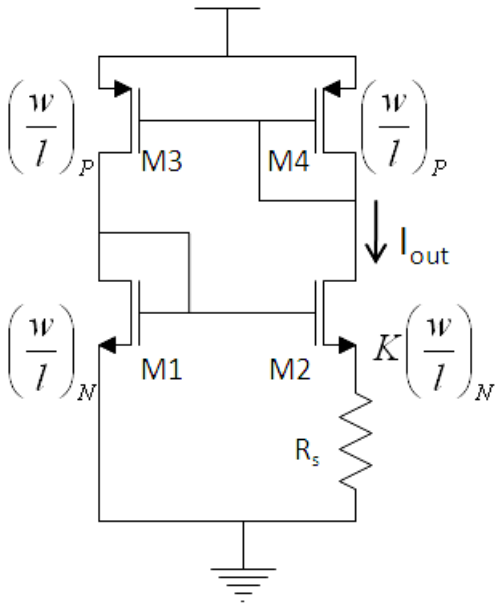


Figure 3-7 Constant gm biasing circuit

$$V_{gs1} = V_{gs2} + I_{out}R_s \qquad (3.21)$$

$$\therefore \sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}} + V_{th1} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox}K(W/L)_N}} + V_{th2} + I_{out}R_s \qquad (3.22)$$

If body effect is ignored, the threshold voltages of M1 and M2 are the same. This leads to equation (3.23).

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}}\left(1-\frac{1}{\sqrt{K}}\right)=I_{out}R_s \qquad (3.23)$$

$$\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}\left(1-\frac{1}{\sqrt{K}}\right)^2={I_{out}}^2{R_s}^2 \qquad (3.24)$$

After dividing both sides by I_{out} and rearranging,

$$I_{out}=\frac{2}{\mu_n C_{ox}(W/L)_N {R_s}^2}\left(1-\frac{1}{\sqrt{K}}\right)^2 \qquad (3.25)$$

For a normal transistor working in saturation, the gm is given by (3.26).

$$g_m=\sqrt{2\mu_n C_{ox}(W/L)_N} \qquad (3.26)$$

Substitute (3.25) in (3.26),

$$g_m=\frac{2}{R_s}\left(1-\frac{1}{\sqrt{K}}\right) \qquad (3.27)$$

The obtained gm as shown in equation (3.27) [29] is mobility and process independent. It only depends on K and R_s. K is the aspect ratio parameter which is only affected by mismatch. R_s is the resistor which is linearly dependent of temperature. The temperature compensation for resistor is covered in next section.

Constant gm biasing technique only keeps a constant transconductance but does not provide a constant current. Therefore, transistors which are not biased by constant gm

biasing circuit should be designed to be saturated in different temperatures. Another issue of constant gm biasing circuit is that it may not be turned on during circuit start up. In equation (3.24), when both left hand side and right hand side are divided by I_{out}, the I_{out} is assumed to be non-zero. However, when the circuit is switched on, it may go to the state when no currents flow through M1 and M2, which could also be a stable state. In order to solve this issue, a start up circuit is added in as shown in Figure 3-8. It forces a small current to flow through path M5 and inject into the drain of M1. Once there is current in path M1, the double current-mirror feedback architecture forces I_{out} to reach the desired current.

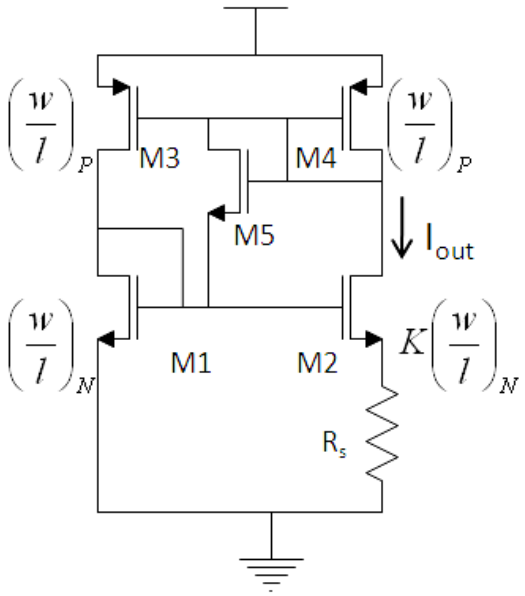


Figure 3-8 Constant gm biasing circuit with start-up transistor

3.6.3 Resistor Temperature Coefficients Cancelling

As introduced in section 3.4, the temperature dependence of resistor can be approximated as a linear equation with TC (temperature coefficients). In modern processes, materials can be of either negative or positive TC. With the series combination of the two materials

and proper sizing, the overall resistance can be temperature independent. The concept is shown in Figure 3-9.

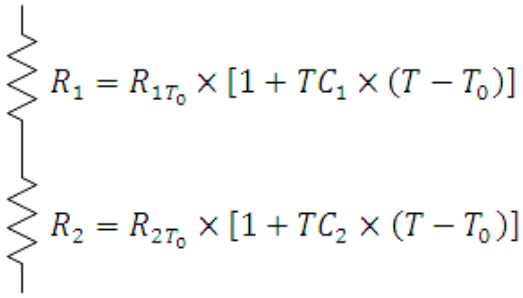


Figure 3-9 Series connection of two resistors with different TC

If it is assumed that TC_1 is positive and TC_2 is negative, the total resistance R_{total} as shown in (3.26) is independent of temperature if the sizes of R_{1T0} and R_{2T0} satisfy equation (3.27). A simulation result of two serially connected resistors with opposite temperature coefficients is shown in Figure 3-10. The two resistors are properly sized to cancel temperature effect. The combined resistance shows a 1.13% variation from temperature range 0 ^{o}C to 250 ^{o}C. Compared to the resistance shown in Figure 3-3 (variation of 8.6%), the improvement is significant.

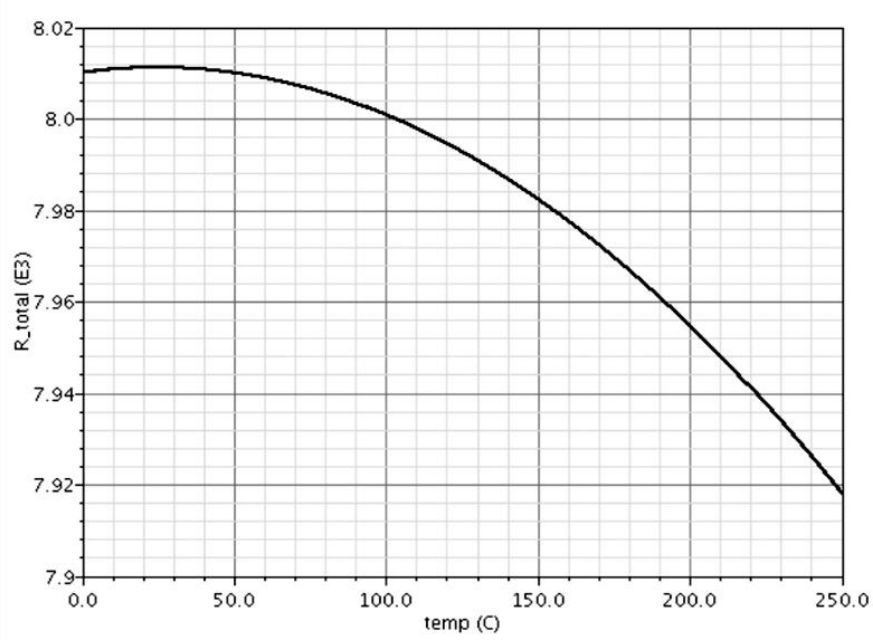


Figure 3-10 Simulation of R_{total}

$$R_{total} = R_1 + R_2 = R_{1T_0} + R_{2T_0} + (T - T_0)\left(R_{1T_0}TC_1 + R_{2T_0}TC_2\right) \quad (3.26)$$

$$R_{1T_0}TC_1 = -R_{2T_0}TC_2 \quad (3.27)$$

Chapter 4 **Switched Capacitor Circuit Fundamentals**

4.1 Concept of Switched Capacitor Circuit

In many applications such as discrete-time filters and charge pumps, switched capacitor circuit is one of the major circuit elements. The fundamental operating concept is based on charge redistribution between capacitors [30]. As shown in Figure 4-1, at phase 1 when S1 is switched on and S2 is switched off, charges are stored at C_s as shown in equation (4.1).

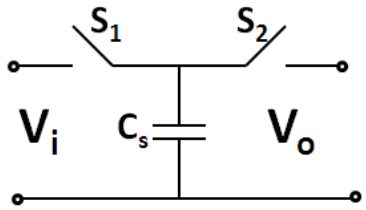


Figure 4-1 Switched capacitor circuit

$$q_i = C_s V_i \qquad (4.1)$$

At phase 2 when S1 is switched off and S2 is switched on, charges are transferred out. The remaining charges are expressed as (4.2).

$$q_o = C_s V_o \qquad (4.2)$$

The transferred charges Δq is

$$\Delta q = q_o - q_i = C_s(V_o - V_i) \qquad (4.3)$$

As current *I* can be expressed as equation (4.4)

$$I = \frac{\Delta q}{\Delta t} \qquad (4.4)$$

Therefore,

$$I = \frac{C_s(V_o - V_i)}{\Delta t} = C_s(V_o - V_i) \times f \qquad (4.5)$$

It means that if switches S1 and S2 are switched on/off in frequency of f, constant current *I* is generated. The equivalent resistance R is (4.6) [30].

$$R = \frac{V}{I} = \frac{V_o - V_i}{C_s(V_o - V_i) \times f} = \frac{1}{C_s f} \qquad (4.6)$$

4.2 CMOS Switches

Simple switch is built on either PMOS or NMOS. For a simple NMOS switch as shown in Figure 4-2a, when $V_g = V_{dd}$, the switch is on. For $V_{in} = V_{dd}$ and $V_{out} = 0$, C is charging. However, for the switch to be turned on, V_g must be larger than V_{th}. Therefore, the maximum value of V_{out} can only be $V_{dd} – V_{th}$. In addition, when body effect is considered, V_{th} is increased. This further decreases maximum value of V_{out}. For PMOS switch, the same analysis is applied. The result is that the minimum value of V_{out} is V_{th} when V_g =0 and V_{in} = 0. In order to achieve a full range of V_{out}, CMOS transmission gate is adopted. As shown in Figure 4-2b, it comprises of a PMOS and a NMOS. When V_{ctrl} is 0V, both transistors are switched off. When V_{ctrl} is 5V, the output voltage V_{out} follows input voltage V_{in}. For V_{in} larger than $V_{dd} – V_{th}$, NMOS is in cutoff region. PMOS is in saturation region. C is charged through PMOS and the maximum value can reach V_{dd}. Similarly for V_{in} smaller than V_{th}, PMOS is in cutoff region and NMOS is in saturation region, C is discharged through NMOS and the minimum value can reach 0V. Therefore, full range of V_{out} can be achieved by using transmission gate [29].

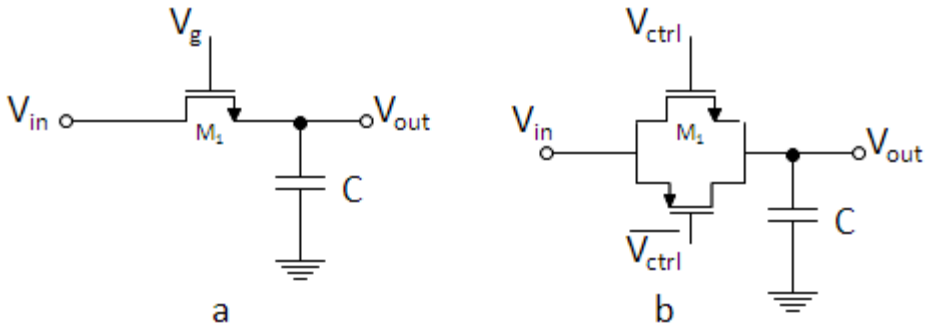


Figure 4-2 NMOS switch (a) and transmission gate switch (b)

The on-resistance of NMOS switch and PMOS switch are defined in equations (4.7) and (4.8). Therefore, the total on-resistance of transmission gate is calculated using $R_{on\text{-}N} \parallel R_{on\text{-}P}$. Figure 4-3 shows the on-resistance of PMOS switch, NMOS switch and transmission gate as a function of input voltage. The maximum on-resistance of transmission gate is obtained when input voltage is at the center when both transistors are in saturation. To reduce the on-resistance, the aspect ratios of NMOS and PMOS are required to be increased. However, this will increase the area of the transistors and the increase of parasitic capacitance will lead to a reduction in bandwidth. In this work, since the sampling frequency is not very high, the requirement on-resistance is not stringent.

$$Linear\ Region:\ \ R_{on} = \frac{2}{k[2(V_{dd} - |V_{th}| - (V_{dd} - V_{out}))]} \tag{4.7}$$

$$Saturation\ Region:\ \ R_{on} = \frac{2(V_{dd} - V_{out})}{k(V_{dd} - V_{out} - |V_{th}|)^2} \tag{4.8}$$

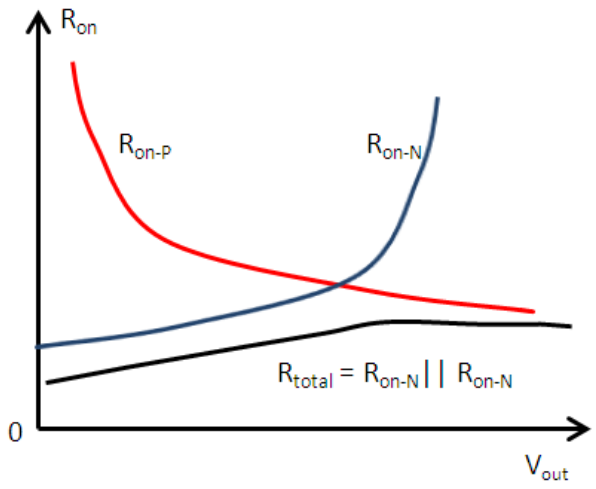


Figure 4-3 On-resistance of transmission gate switch

4.3 Non-Ideal Effects of CMOS Switches

4.3.1 Charge Injection

Charge injection is one of the major error mechanisms in switched capacitor circuits. It is introduced by the non-ideality of the switch [31]. As shown in Figure 4-4, the switch is built by a single NMOS transistor. When the switch M1 is on, a channel is formed at the oxide-silicon interface. Charges are stored inside the inversion layer. When M1 is turned off, charges exit through the source and drain. The charge injection to V_{in} does not have much effect. However, the charge injection to capacitor introduces additional charges Δq which is considered as offset to the sampled output signal. Moreover, the amount of charges injected to the capacitor is too difficult to be determined since it depends on many parameters such as threshold, process variation and clock transition time. In switched capacitor circuit, charge injection is one of main sources of non-linearity.

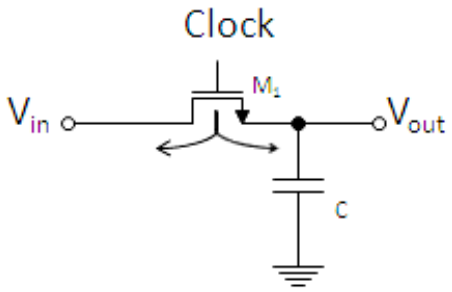


Figure 4-4 Charge injection of MOS switch

4.3.2 Clock Feedthrough

As shown in Figure 4-5, the clock signal is coupled with the sampling capacitor through the gate-source capacitor. Similar to charge injection, it introduces offset to the sampled output signal. The offset voltage can be express in equation (4.9), where C_{ov} is the overlap capacitance per unit width [31].

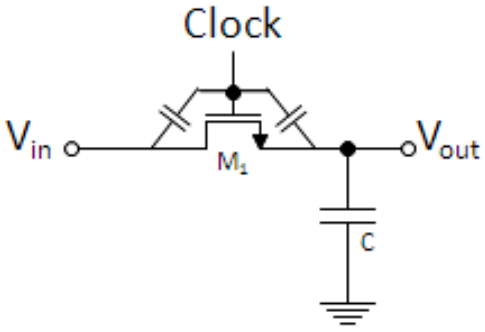


Figure 4-5 Clock feed through of MOS switch

$$\Delta V = V_{g_{M1}} \frac{WC_{ov}}{WC_{ov} + C} \qquad (4.9)$$

Clock feedthrough is independent of the input level and embedded as a constant offset to the circuit. Its effect depends on the size of the switch as well as the size of the sampling capacitor.

4.3.3 Bottom plate sampling technique

The bottom plate sampling technique [32] is an effective way to reduce the effect of charge injection. As shown in Figure 4-6, two switches S1 and S2 are placed at the two plates of the capacitor. During the sampling phase, both switches are turned on, which is the same as phase one of Figure 4-1. However, at the transition to hold phase, there is a small delay between S1 and S2. As the bottom plate of C is connected to ground, when S2 is switched off first, a fixed amount of charge is injected on to C. After a small delay, switch S1 is switched off. Since the bottom plate of C is already opened, no charge will be injected on C. Therefore, compared to normal switched capacitor circuit as shown in Figure 4-1, bottom plate sampling technique samples a fixed amount of charges on C. It can be modeled as a DC offset to the output which does not affect the linearity. Moreover, such DC offset can be further reduced in a fully differential circuit topology.

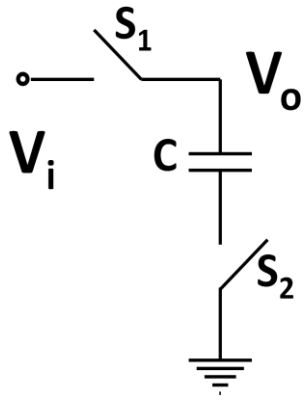


Figure 4-6 Bottom plate sampling techniques

4.4 Switched capacitor integrator

4.4.1 Switched Capacitor Integrator Operation Principle

An integrator is a circuit block performing a time domain integration of input voltage. In frequency domain, the integration process is a form of 1st-order low pass filtering. A

traditional continuous-time RC integrator [33] is shown in 4-7. The derivation of transfer function is shown in equations (4.10), (4.11), (4.12) and (4.13). As shown in (4.13), the output voltage is an integration of the input voltage with a time constant $R_{in}C$.

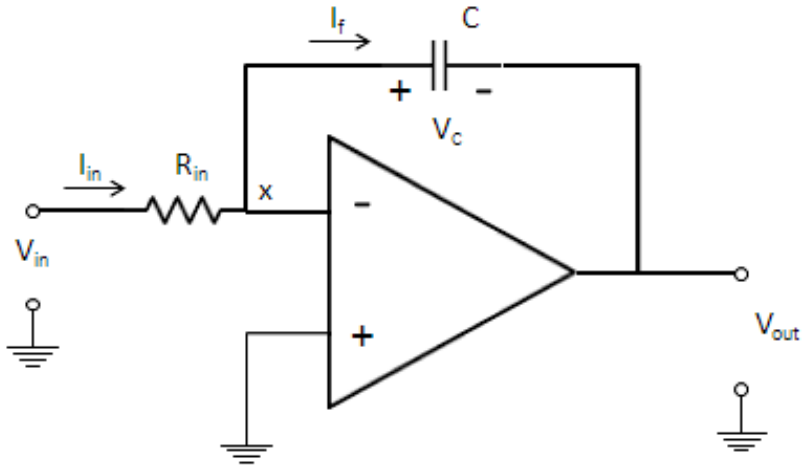


Figure 4-7 RC integrator schematic

$$V_c = \frac{Q}{C} = V_x - V_{out} = -V_{out} \qquad (4.10)$$

$$\therefore -\frac{dV_{out}}{dt} = \frac{dQ}{Cdt} \qquad (4.11)$$

$$I_{in} = I_f = \frac{V_{in}}{R_{in}} = -\frac{CdV_{out}}{dt} \qquad (4.12)$$

$$V_{out} = -\frac{1}{R_{in}C}\int_0^t V_{in}dt \qquad (4.13)$$

The switched capacitor based implementation of integrator is achieved by replacing the input resistor with a switched capacitor. Figure 4-8 shows the integrator architecture which replacing R_{in} with switched capacitor C_s. The fundamental concept is to sample and transfer charges from input to feedback capacitor C_{fb} through the median C_s[34].

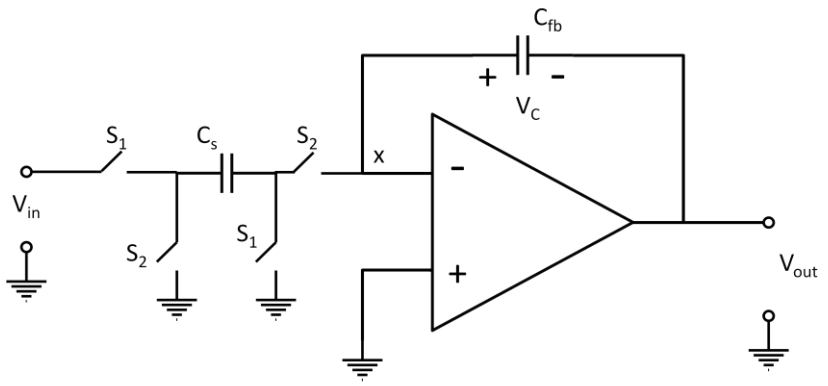


Figure 4-8 Switched capacitor integrator

At phase one (t= -T), switches S1 are switched on while switches S2 are switched off as shown in Figure 4-9. The capacitor C_s follows Vin and stores the charges. Capacitor keeps the previous charges at t= -1.5T. Therefore,

$$Q_s[(n-1)T_s] = C_s V_{in}[(n-1)T_s] \qquad (4.14)$$

$$Q_{fb}[(n-1)T_s] = Q_{fb}[(n-1.5)T_s] \qquad (4.15)$$

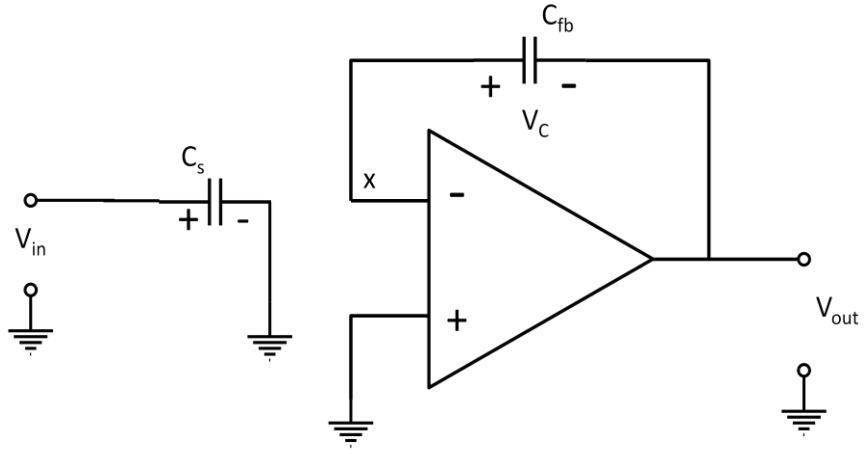


Figure 4-9 Clock phase 1

At phase two (t= -0.5T), switches S1 are switched off while S2 are switched on as shown in Figure 4-10. The capacitor C_s transfers the charges (previously stored in phase one) onto C_{fb}. Therefore,

$$Q_s[(n-0.5)T_s] = 0 \qquad (4.16)$$

$$Q_{fb}[(n-0.5)T_s] = Q_{fb}[(n-1)T_s] - C_s V_{in}[(n-1)T_s] \qquad (4.17)$$

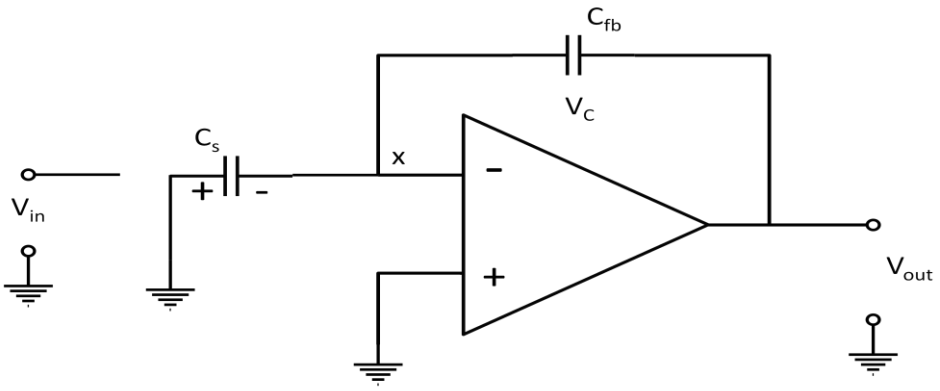


Figure 4-10 Clock phase 2

At the 2nd phase one,

$$Q_s[(n)T_s] = C_s V_{in}[(n)T_s] \qquad (4.18)$$

$$Q_{fb}[(n)T_s] = Q_{fb}[(n-1)T_s] - C_s V_{in}[(n-1)T_s] \qquad (4.19)$$

By substituting (4.20) and (4.21),

$$V_{out} = -\frac{Q_{fb}}{C_{fb}} \qquad (4.20)$$

$$V_{out} = \frac{Q_s}{C_s} \qquad (4.21)$$

Equation (4.22) can be obtained,

$$-V_{out}C_{fb}[(n)T_s] = -V_{out}C_{fb}[(n-1)T_s] - C_sV_{in}[(n-1)T_s] \qquad (4.22)$$

After applying Z-transform, the transfer function of switched capacitor integrator is shown in (4.25). It is a form of 1st order digital low pass filter with gain of C_s/C_{fb} [34].

$$V_{out}[(n)T_s] - V_{out}[(n-1)T_s] = \frac{C_s}{C_{fb}}V_{in}[(n-1)T_s] \qquad (4.23)$$

$$V_{out}(1 - Z^{-1}) = \frac{C_s}{C_{fb}}V_{in}Z^{-1} \qquad (4.24)$$

$$\frac{V_{out}}{V_{in}} = \frac{C_s}{C_{fb}}\frac{Z^{-1}}{(1 - Z^{-1})} = \frac{C_s}{C_{fb}}\frac{1}{Z - 1} \qquad (4.25)$$

4.4.2 Non-ideality due to finite gain of amplifier

The transfer function (4.25) is derived based on the assumption of an ideal amplifier. In practice, however, the actual gain of the amplifier is finite. Therefore, equation (4.25) should be modified to (4.26) [35].

$$\frac{V_{out}}{V_{in}} = \frac{\beta}{Z - (1 - \alpha)} \qquad (4.26)$$

$$with \quad \beta = \frac{C_s/C_{fb}}{1 + \frac{1}{A_0}(1 + \frac{C_s}{C_{fb}})}$$

$$\alpha = \frac{\beta}{A_0} \approx \frac{C_s/C_{fb}}{A_0}$$

The finite gain of amplifier A_0 reduces the gain of the integrator (with factor of β) and causes integrator leakage (with factor of α). In a switched capacitor modulator, such non-ideal effects will lead to the degradation of performance [35].

Chapter 5 **Design of High Temperature ΣΔ Modulator**

5.1 Review of Previously Published High Temperature ΣΔ Modulators

A 2nd-order single stage modulator and a 3rd-order 2-1 MASH cascaded ΣΔ modulator were proposed in [36] as shown in Figure 5-1. Both modulators adopt switched capacitor architecture with single bit quantization and OSR of 256. The 3rd-order MASH modulator utilizes the 2nd-order modulator as its 1st stage. The 2nd stage comprises of a 1st-order ΣΔ modulator. Besides, it also adopts a software based error cancellation block in 3rd-order MASH modulator. The chip is fabricated using 5V 1.5 μm double-poly standard CMOS process.

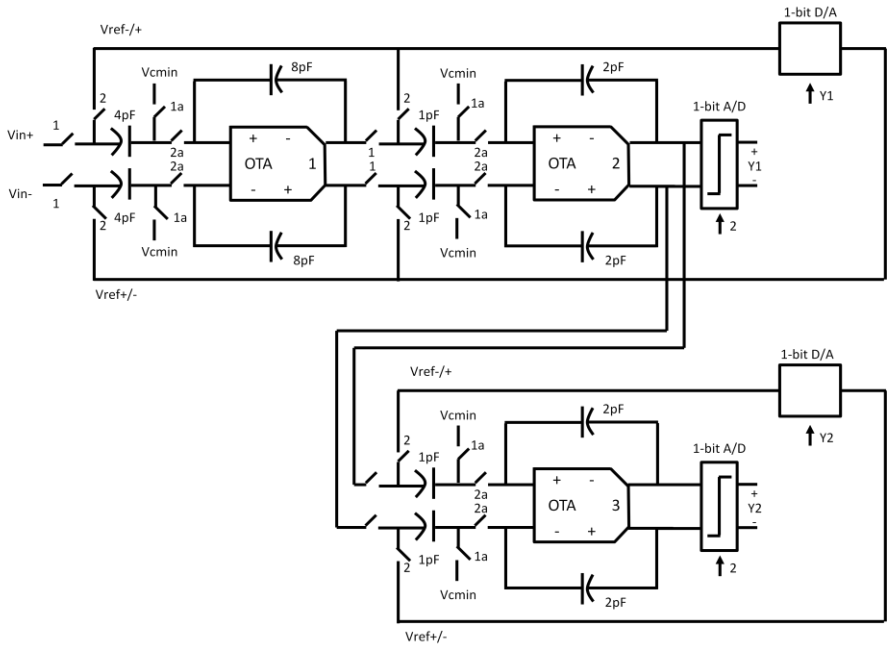


Figure 5-1 System schematic of a 2nd order single stage modulator and a 3rd order 2-1 MASH cascaded ΣΔ modulator [36]

In the implementation of the integrator, a fully differential folded cascode amplifier is applied. The common-mode feedback circuit adopts switched capacitor architecture with minimum sized transmission gate switches in order to limit the high temperature leakage current. A latched comparator is used for the single bit quantizer. The circuit is tested at different temperatures. The result is shown in Table 5-1. The amplifier shows a gain of 64 dB at room temperature and 53 dB at 255 ^{o}C.

Table 5-1 Amplifier open-loop gain at different temperatures [36]

Temperature (^{o}C)	U1 Gain (dB)	CMFB Clock Frequency	Temperature (^{o}C)	U2 Gain (dB)	CMFB Clock Frequency
25	64	256KHz	26	63	256KHz
78	64	256KHz	79	62	256KHz
183	63	256KHz	163	55	256KHz
239	55	3.2MHz	230	54	3.2MHz
255	53	3.2MHz	251	53	3.2MHz

As shown in Table 5-2, the overall system shows a maximum SNDR of 88 dB at 223 ^{o}C and 80 dB at 255 ^{o}C. In room temperature, the SNDR decreased to around 75 dB.

Table 5-2 Experimental SNDR at different temperatures and input amplitudes [36]

Temperature (oC)	Max SNDR (dB)
25	75
100	79
166	83

223	88
255	80

In this design, a 5V 1.5 μm standard CMOS process is chosen which brings some process related disadvantages such as high temperature leakage current and substrate latch up. Moreover, the chosen architecture does not have a feed forward path. This may lead to large swing of the internal nodes. The chosen architecture of amplifier is folded cascode which ensures the high DC gain and driving strength. However, the output swing is limited which may lead to the limitation of dynamic range. The switched capacitor based common-mode feedback circuit also suffers from the high temperature troop. As shown above, the gain of the amplifier varies about 11 dB from room temperature to 255 ^{o}C. The 3rd-order modulator does not show a superior performance over 2nd-order modulator since it is more sensitive to amplifier common-mode voltage drift. Some effective high temperature design techniques should be implemented to compensate the high temperature issues.

Another 2nd-order modulator and a 4th-order 2-2 cascade modulator were proposed in [37] as shown in Figure 5-2. Similar to [36], both modulators adopt switched capacitor architecture with single bit quantization and OSR of 256. The 4th-order modulator is built with a 2nd-order modulator as the first stage, followed by another 2nd-order modulator. The chip is fabricated using 0.5 μm SOS CMOS process.

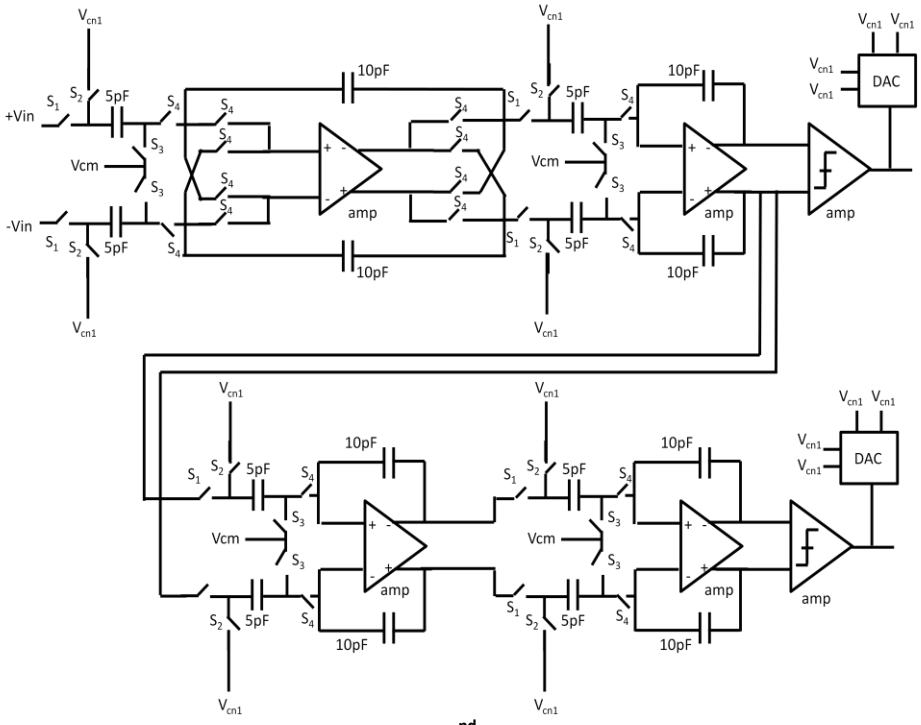


Figure 5-2 System schematic of a 2nd-order single stage modulator and a 4th order 2-2c cascaded modulator [37]

In this implementation, it employs the chopper circuit configuration for the first stage integrator, which is helpful in reducing low frequency noises. Fully differential folded cascode amplifier architecture with a modified wide swing cascode biasing circuit is proposed. It applies a continuous-time common-mode feedback method to control the output common-mode voltage.

The circuit is tested at 25 ^{o}C, 150 ^{o}C and 200 ^{o}C. The result is shown in Table 5-1. The amplifier shows a gain of 2298 (67 dB) at 25 ^{o}C and 1117 (61 dB) at 200 ^{o}C. The peak SNDR achieved is 92.3 dB at 25 ^{o}C and 80.6 dB at 200 ^{o}C.

Table 5-3 Summary of measurement results [37]

Parameter	T= 25 ^{o}C	T= 150 ^{o}C	T= 200 ^{o}C
Opamp Measurement Summary			
Gain	2298	1611	1117
GBW	7.85 MHz	5.60 MHz	4.99 MHz

Slew Rate (V/us)	4.4	4.4	4.4
Power(mW)	4.39	4.36	4.51
Modulator Measurement			
Peak SNR (dB)	92.7	86.9	81.1
Resolution (bits)	15.5	14.9	13.5
Peak SNDR (dB)	92.3	86.7	80.6

In this design, instead of standard CMOS process, a 0.5 μm SOS CMOS process is chosen. This reduces the substrate latch up as well as high temperature leakage current. Similar to [36], it adopts fully differential folded cascode architecture for integrator. Moreover, it uses a modified wide swing cascode biasing circuit and continues time common-mode feedback circuit. As a result, the amplifier shows a more consistent performance over the temperature range. However, the drawback of low output swing of folded cascode architecture still affects the performance of the overall system since the SNDR dropped about 12 dB from 25 ^{o}C to 200 ^{o}C. The 4th order modulator and 2nd-order modulator show similar performance for OSR larger than 128 due to the dominance of noises other than quantization noise. Some effective high temperature design techniques should be implemented to compensate the high temperature issues.

Both works have proposed switched capacitor based high temperature ΣΔ modulators with high resolution. However, in the design aspect, both designs tend to over design to compensate the temperature changes rather than applying some high temperature techniques to resolve the high temperature issues. This results in the relatively huge degradation in performance over the temperature range (above 10dB in SNDR). In addition, the measurements are done only up to 250 ^{o}C. Therefore, this work is proposed to demonstrate a constant modulator performance over the temperature range. Moreover, the maximum measurement temperature is pushed to 300 ^{o}C.

5.2 System Level Design of Sigma Delta Modulator

In this research, a discrete-time switched capacitor based 3rd-order low pass ΣΔ modulator is designed as a sub-circuit of an ADC. Furthermore, the ADC is employed in a high temperature data acquisition system dedicated for oil-drilling application. As shown in Figure 5-3, the system senses temperature, pressure and so on from the environment. The sensed signal bandwidth from sensor is up to 200 Hz. Subsequently, it digitizes the signal and sends to digital controller for process control. The required resolution of digitized signal is as high as 16 bits. In order to meet the requirement, the target design specification for the ΣΔ modulator is shown in Table 5-2.

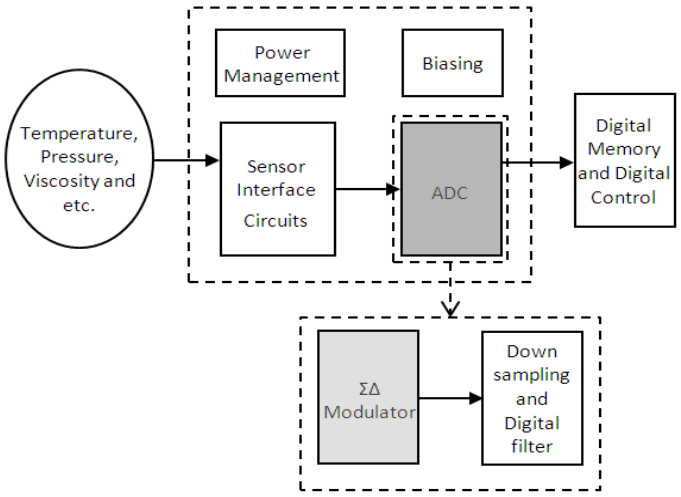


Figure 5-3 High temperature data acquisition system block diagram

Table 5-4 Design Specification

ΣΔ modulator			
OSR	256	Input Bandwidth	250 Hz
Order	3	Clock Frequency	128kHz
Quantizer	1 bit	SNR	102 dB

Power Supply	0V-5V	ENOB	17 bits
Input DC	2.5V	Power Consumption	<35mW
Input Maximum Amplitude	1.5V	Temperature Range	up to 225 ^{o}C (simulation model limit)
Amplifier			
Power Supply	0V-5V	UG Bandwidth	>2MHz
Input DC	2.5V	Gain	>60 dB
Input Maximum Amplitude	1.5V	Phase Margin	>60^{o}
Load Capacitance	10 pF	Power Consumption	<6mW

5.2.1 MatLab Model Construction and Simulation

In order to efficiently develop the ΣΔ modulator model and consistently evaluate the modulator performance, Schreier's Delta-Sigma Toolbox [38] is used. The Delta-Sigma Toolbox is a MatLab library which contains nearly 100 functions and supports NTF synthesis, modulator simulation and SNR estimation and so on.

After substituting the OSR, order and quantization level into the *synthesizeNTF()* funtction from Delta-Sigma Toolbox, the NTF and STF is shown in equations (5.1) and (5.2) respectively. The corresponding loop transfer function is shown in equation (5.3).

$$NTF = \frac{(Z-1)(Z^2-2Z+1)}{(Z-0.6694)(Z^2-1.531Z+0.6639)} \qquad (5.1)$$

$$STF = \frac{0.79978(Z^2-2Z+1.055)}{(Z-0.6694)(Z^2-1.531Z+0.6639)} \qquad (5.2)$$

$$H(Z) = \frac{0.79978(Z^2 - 1.64Z + 0.6948)}{(Z-1)(Z^2 - 2Z + 1)} \qquad (5.3)$$

The poles and zeros of the NTF(Z) are plotted in Figure 5-4.

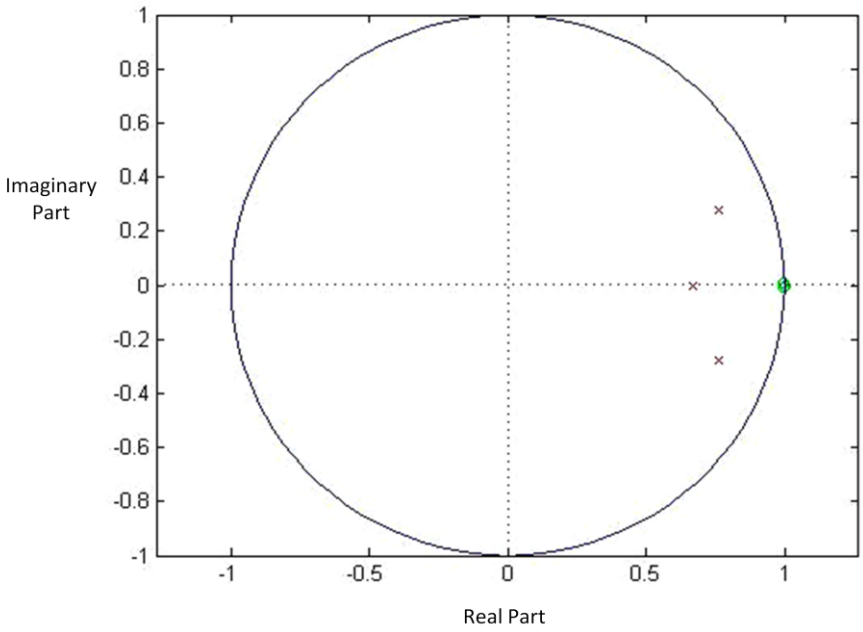


Figure 5-4 Poles and zeros of NTF (Z)

The PSD based on the time domain simulation result of transfer function is shown in Figure 5-5. The in band noise level is below 140 dB and the slope is 60 dB/dec. The SNR of 135 dB can be achieved in a 250 HZ bandwidth.

To realize the transfer function with the corresponding architecture, *realizeNTF()* function from Delta-Sigma Toolbox can be used. Generally, for a particular architecture, its transfer function is abstracted as a polynomial with coefficients matrix [a g b c] as shown in equation (5.4). By equating it with equation (5.3), [a g b c] can be calculated and used to construct the SimuLink model as shown in Figure 5-6. The corresponding coefficients can be calculated as shown in Table 5-3.

$$H'(Z) = \begin{bmatrix} \Sigma a_n \\ \Sigma g_{n'} \\ \Sigma b_{n''} \\ \Sigma c_{n'''} \end{bmatrix} \sum Z^m \qquad (5.4)$$

Where m, n, n', n'' and n''' are integers associated to the architecture

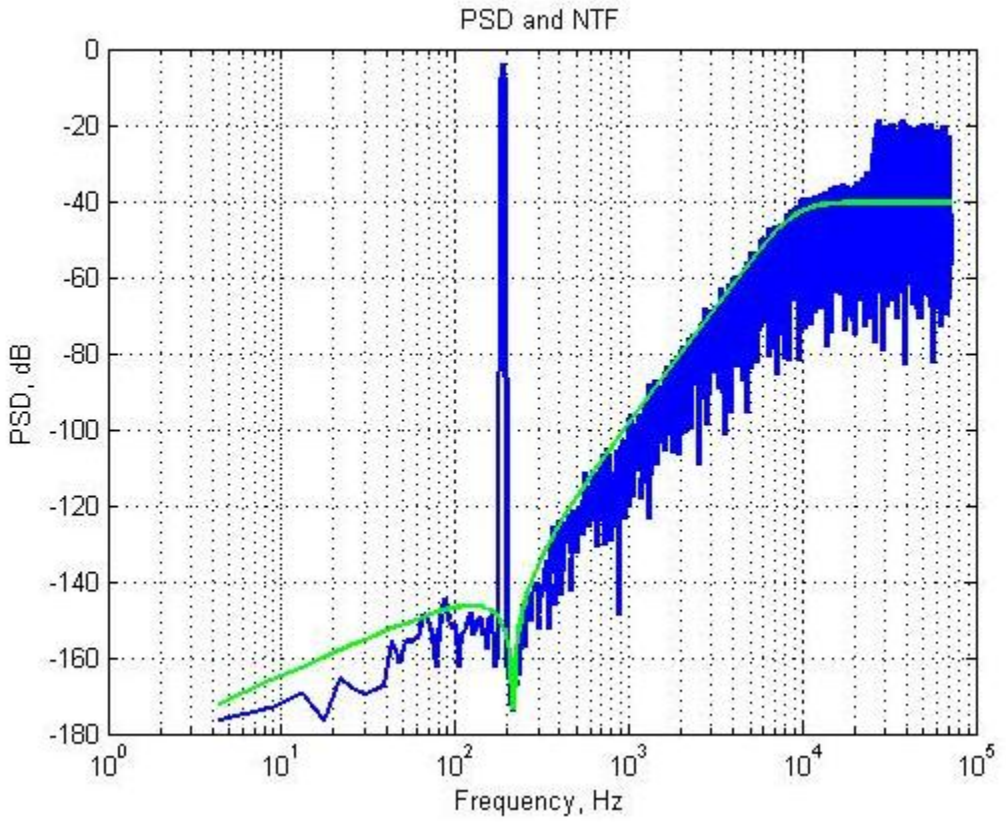


Figure 5-5 NTF (green) and PSD (blue) of transfer function simulation

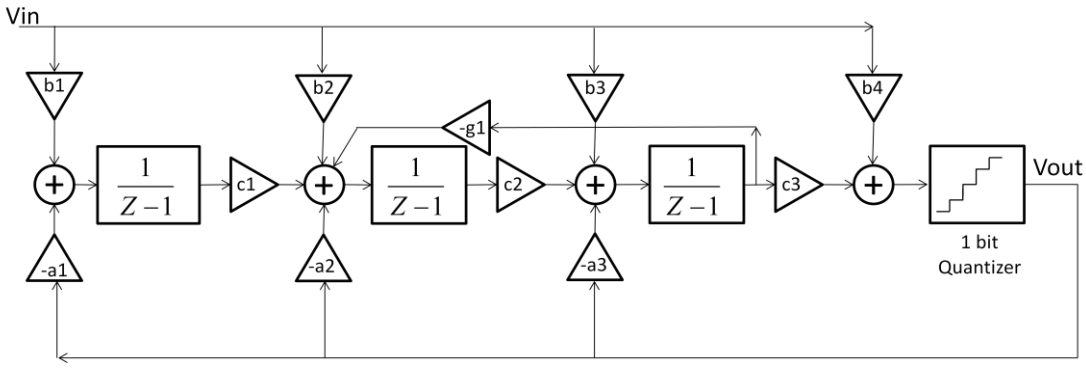


Figure 5-6 Full CIFB architecture

Table 5-5 Calculated unscaled coefficients

a1	**0.044**	**b1**	**0.044**
a2	**0.288**	**b2**	**0**
a3	**0.800**	**b3**	**0**
g1	**0.00009**	**b4**	**0**
c1	**1**	**c2**	**1**
c3	**1**		

5.2.2 SimuLink Model Construction and Optimization

The SimuLink model shows an ideal model of the ΣΔ modulator and all internal signals are not bounded. However, in practice, power supply imposes the upper and lower limits for all internal signals. Therefore, the coefficients obtained need to be properly scaled to ensure that all internal signals are bounded, especially for the outputs of integrators. This can be achieved by using *scaleABCD()* function. Moreover, in order to achieve the maximum dynamic range of modulator, the internal integrator's output signal amplitude needs to be minimized. This can be achieved by manipulating the *xlim* parameter in *scaleABCD()* function [39]. In addition, it is noticed that coefficient g_1 is relatively too small to be realized in practice since it corresponds to the ratio of the input capacitance to the feedback capacitance in a switched capacitor ΣΔ modulator. The presence of the g_1 path creates the notch near the end of the signal band as shown in Figure 5-6. If the path is ignored, the notch in the PSD curve will not be present and the SNR is decreased by about 17 dB. To further improve the architecture, a feed forward path from the input signal to

the input of the 3rd stage integrator is added in order to balance the internal signal swings of each stage, which effectively improves the dynamic range of the modulator. The final architecture is shown in Figure 5-7, with coefficients tabulated in 5-3. The simulated PSD is shown in Figure 5-8 and the peak SNR obtained is 118dB.

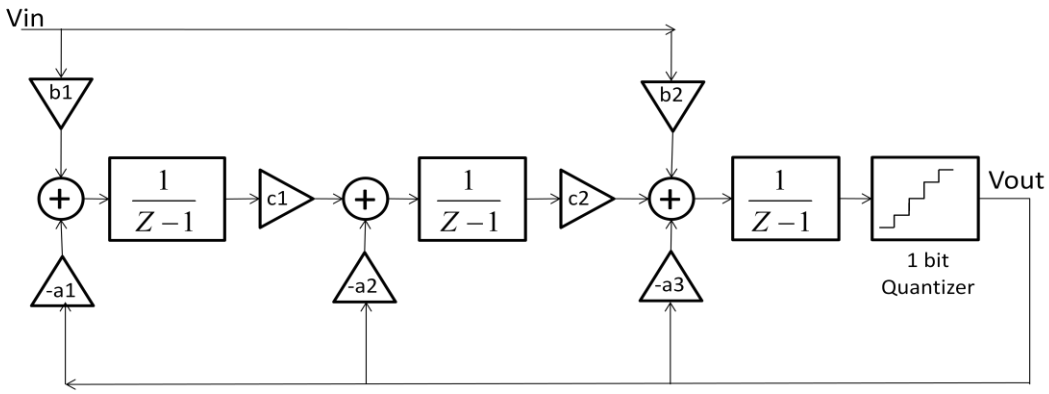


Figure 5-7 Finalized modulator block diagram

Table 5-6 Finalized coefficients after scaling

a1	**0.132**	**b1**	**0.132**
a2	**0.108**	**b2**	**0.44**
a3	**0.44**	**c1**	**0.12**
		c2	**1.48**

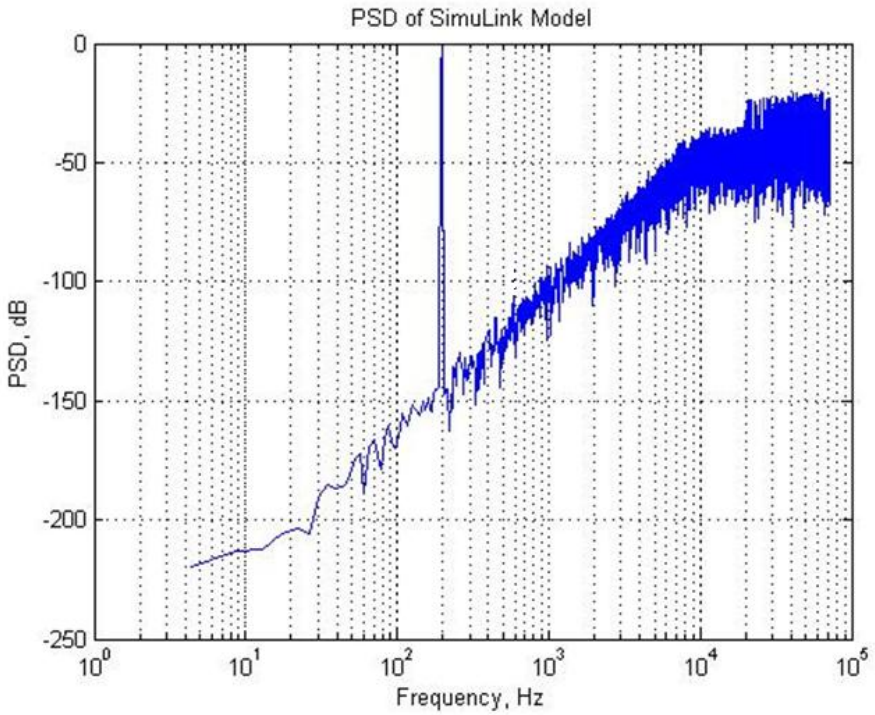


Figure 5-8 PSD of SimuLink model simulation

Chapter 6 **Circuit Implementation**

6.1 Top Level Circuit Schematic

The top level circuit is shown in Figure 6-1. The mapped circuit schematic based on MatLab model is shown in Figure 5-8. The integrators are built on switched capacitor based fully differential amplifiers. During operation, the capacitors are charging or discharging as controlled by different clock signals. There are three stages of integrators which are built on switched capacitor circuit. Each integrator's gain is defined by the ratio between the input capacitor and feedback capacitor. The gain is set according to the coefficients in MatLab model. The output is digitized using a single bit quantizer and then fed back to each stage accordingly.

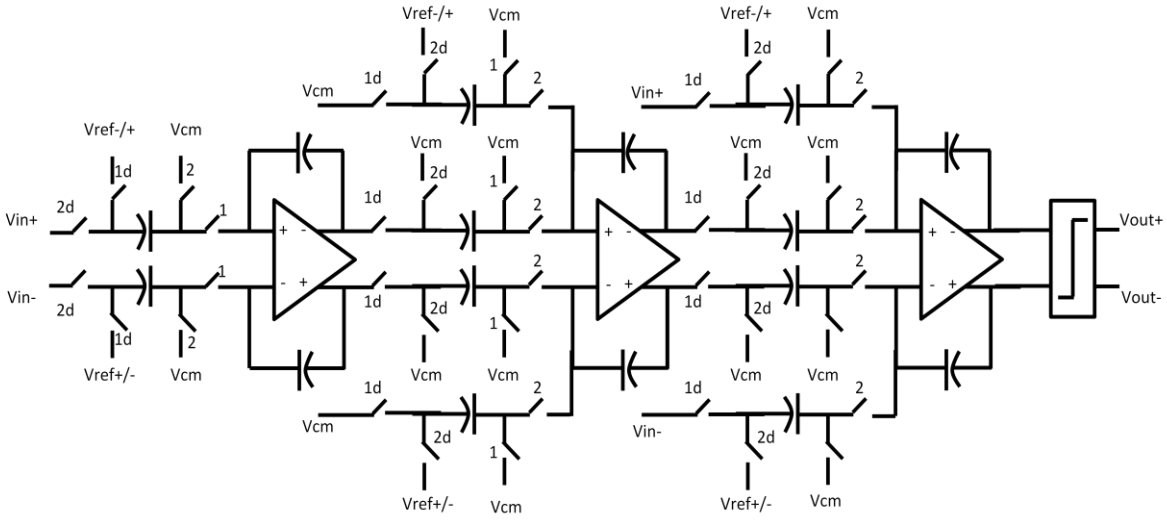


Figure 6-1 Modulator schematic

6.2 Sizing the capacitor

As introduced in section 2.7, thermal noise is the primary source of noise. Therefore, the sizing of the capacitance is based on the estimation of thermal noise [40]. Moreover, it is suggested that a large portion of thermal noise is contributed by the input switches of the first integrator. The thermal noise of the input switches is expressed in equation (6.1) [40].

$$\overline{V_n^2} = \frac{kT}{OSR \times C} \qquad (6.1)$$

In order to achieve SNR = 110 dB with a full scale sine wave input, it is required that [41]

$$V_n^2 = \frac{kT}{OSR \times C} \leq \frac{(0.5V_{dd})^2}{2 \times 10^{SNR/10}} = 3.125 \times 10^{-10}\ V^2 \qquad (6.2)$$

Therefore,

$$C_{min} = 1.04\ pF\ for\ T = 300℃$$

As equation (6.2) shows, at a typical temperature, a 10 dB increase of SNR requires ten times the value of capacitance. In this design, an SNR of 102 dB is required, which corresponds to the minimum capacitance of 1.04pF (corresponding to 110 dB of SNR).

6.3 Design of Fully differential Amplifier

In this work, in order to achieve a stable resolution as high as 17 bits from room temperature to 225 ^{o}C, the amplifier is required to have a constant gain above 60 dB within the temperature range. To achieve this, either folded cascode amplifier or two-stage amplifier can be chosen.

6.3.1 Analysis of Folded cascode amplifier

A typical folded cascode amplifier is capable of achieving high DC gain and bandwidth [42]. However, it suffers from low output swing, which is crucial in this work. As shown in Figure 6-2, in order for all the transistors in the output rail operating in saturation, equation (6.3) must be satisfied. It indicates $2V_{od}$ (V_{od} is the over-drive voltage which equals the difference between V_{gs} and V_{th} as shown in equation (6.3)) for the positive direction (M8 and M10) and $2V_{od}$ for the negative direction (M4 and M6). As temperature rises, the threshold voltage decreases, which leads to the increase of V_{od}. As shown in Figure 3-1, the variation of the threshold voltage can be up to 0.5V. As a result, the output swing decreases about 2V from room temperature to 225 ^{o}C. It affects the modulator's performance because the decrease of output swing will cause the internal integrator output saturate. Hence, the dynamic range is degraded.

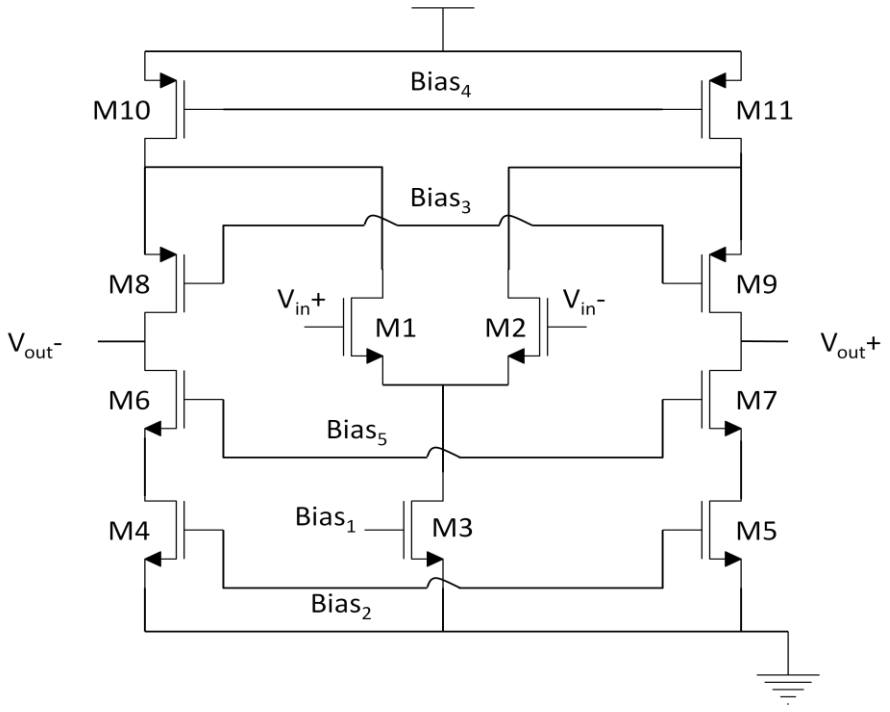


Figure 6-2 Schematic of folded cascode fully differential amplifier

$$V_{ds} > V_{gs} - V_{th} = V_{od} \qquad (6.3)$$

$$2V_{od} \leq V_{out\pm} \leq V_{dd} - 2V_{od} \qquad (6.4)$$

In addition, a folded cascode topology requires complex biasing circuitry since it has more transistors. As a result, it is difficult to achieve proper biasing condition for all the transistors at different temperatures over the temperature range.

6.3.2 Two-Stage amplifier

As an alternative architecture, a two-stage amplifier can also achieve a gain as high as 60 dB [43]. As shown in Figure 6-3, M1 and M2 form the input differential pair. Nodes A and B are the outputs of the first stage amplifier and they are connected to the gates of M3 and M4 respectively. M3 and M4 are the output stage amplifiers. Compared to the cascode architecture, one of the major disadvantages of two-stage architecture is the need for compensation. It is shown in Figure 6-3 where the capacitors C1 and C2 form the compensation paths. However, in high temperature applications, the tolerance for the variations of threshold voltage is higher than folded cascode architecture since the output stage has fewer transistors. For temperature changes from 0 ^{o}C to 225 ^{o}C, the output swing shrinkage of two-stage architecture is half of that in folded cascode architecture. Since the number of transistors of the output rail is fewer, two-stage architecture requires simpler biasing circuitry. Moreover, the two-stage architecture is more noise immune than the folded cascode architecture. Therefore, unlike the previously reported works, two-stage amplifier architecture is chosen to implement the fully differential amplifier.

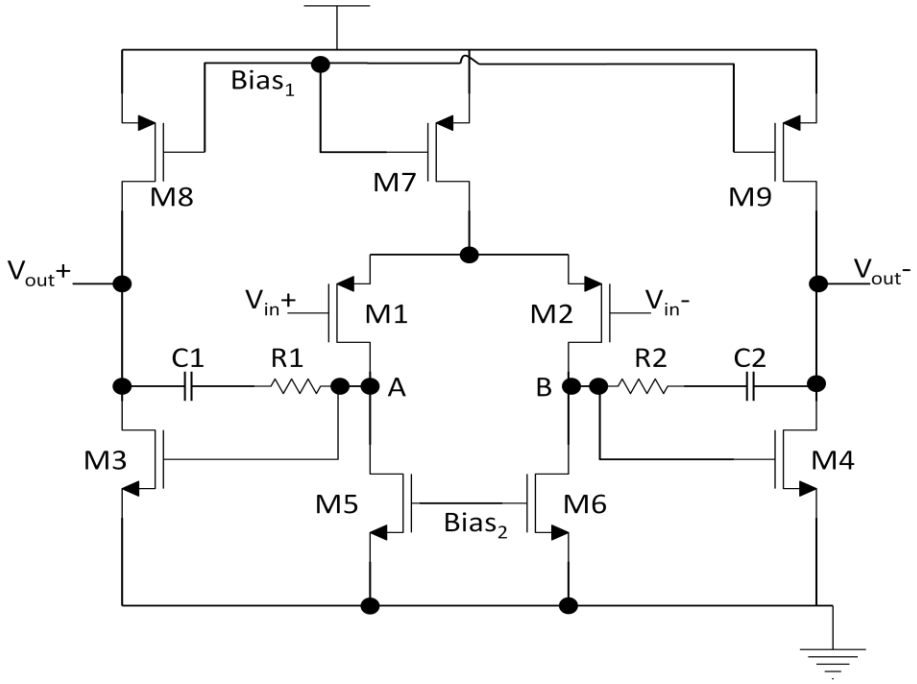


Figure 6-3 Schematic of two stage fully differential amplifier

6.3.3 Common-Mode Feedback

For a fully differential amplifier, a common-mode feedback (CMFB) circuit is required in order the control the output common-mode voltage [44]. As shown in Figure 6-4, a CMFB circuit takes in the differential output signal and obtains the common-mode voltage. Subsequently, the sensed common-mode voltage is compared with the reference voltage. The result of the comparison is a correction signal which is fed into the amplifier. The correction signal tunes the output common-mode voltage to follow the reference voltage. There are primarily two types of CMFB circuit, namely the discrete-time and continuous-time CMFB circuits.

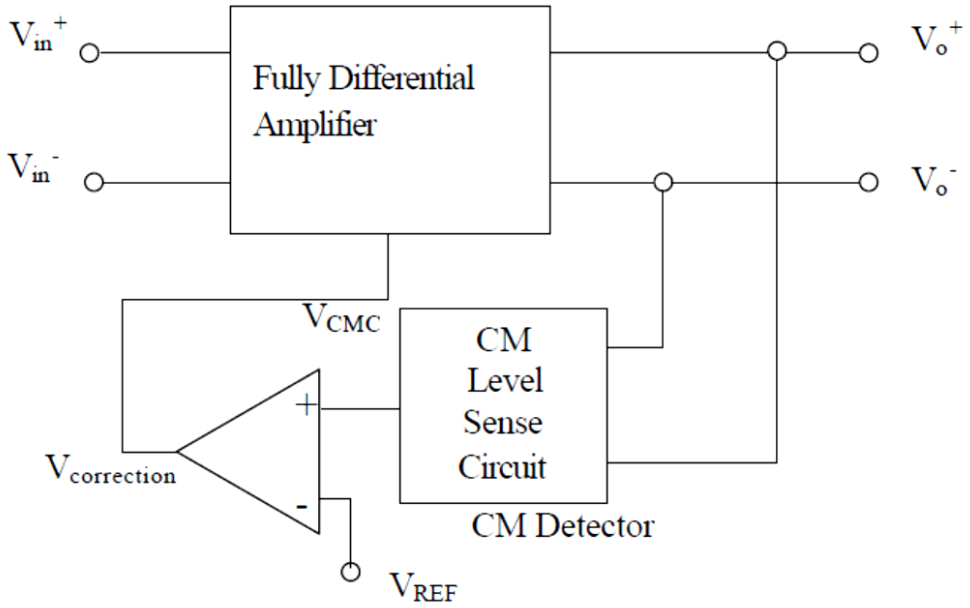


Figure 6-4 Concept of common-mode (CM) feedback

In order to sense the common-mode voltage, two equivalent resistors are applied as shown in Figure 6-5. In this implementation, the resistance must be large enough in order to maintain the amplifier performance unaffected. Alternatively, a switched capacitor can be used to replace the resistor. The equivalent resistance of a switched capacitor is shown in equation (4.6).

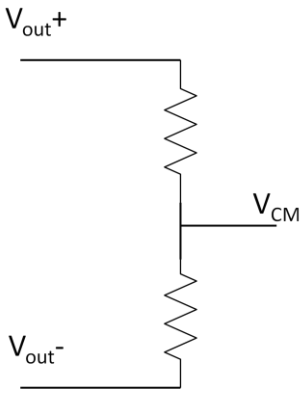


Figure 6-5 Circuit which calculates the output common-mode voltage

6.3.3.1 Switched Capacitor CMFB Circuit

A switched capacitor based CMFB circuit [45] is shown in Figure 6-6. In phase 1, clock φ_1 is on and clock φ_2 is off. Capacitors C3 and C4 are charged to reference voltage V_{cm} and $V_{ref.}$ The charge error Δq based on V_{ref} is distributed on C3 and C4. At phase 2, clock φ_1 is off and clock φ_2 is on, C3 and C1 are in parallel and similar for C4 and C2. The nodes A and B are connected to the differential output and are force to be at voltage $V_{out}+$ and $V_{out}-$ respectively. Previously stored charges Δq redistribute according to the voltages at node A and B. A voltage offset is then added to the control signal V_{cmfb} which is connected back to amplifier to tune the output common-mode voltage. In order to obtain a large equivalent resistance, both the sampling frequency and switching capacitance need to be selected properly [44].

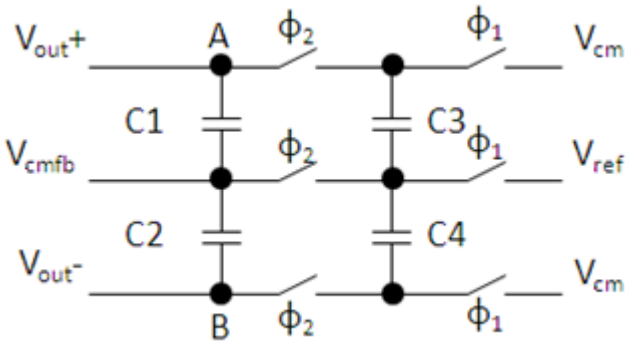


Figure 6-6 Switched capacitor based CMFB circuit

Despite of the simplicity of switched capacitor CMFB circuit, it has several drawbacks. One of the major drawbacks is the voltage droop in high temperature environment as shown in Figure 6-7. This may be results from the charge leakage to the substrate as well as the switch transistors. This voltage droop has been mentioned in [36] in section 5.1.1. The droop voltage depends on the capacitance as well as the switch transistor size. This is

because a large capacitance will store more charge and a small switch transistor size will limit the leakage. One of the techniques to reduce this effect is to increase the clock frequency which charge the capacitors more frequently and reduce the drooping time. Moreover, the switched capacitor CMFB circuit has inherited switching spikes and the induced noise level is relatively high. This is not acceptable in high resolution modulator design.

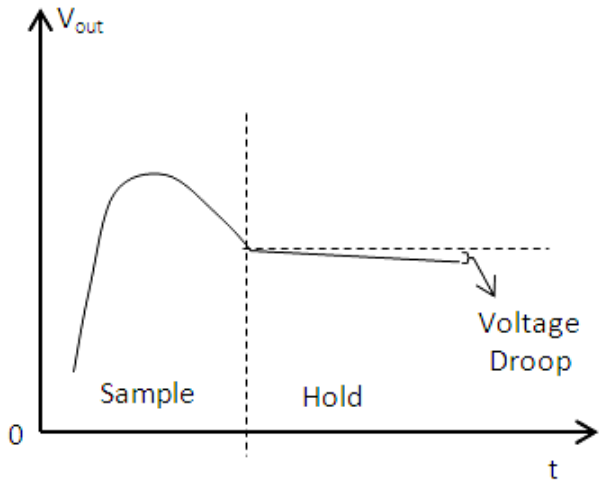


Figure 6-7 Voltage droop of switched capacitor voltage

6.3.3.2 Continuous-Time CMFB Circuit

The CMFB circuit can also be implemented using continuous-time approach as shown in Figure 6-8. Two large resistors are applied in order to obtain the output common-mode voltage. M1 and M2 form an input differential pair. The sensed common-mode voltage is connected to the gate of M1. The reference voltage is connected to the gate of M2. The current mirror load formed by M3 and M4 forces the node voltage A and B to equal when the gate voltages of M1 and M2 are equal. The output voltage at node B is fed back to tail transistors in Figure 6-3 to tune the output common-mode voltage.

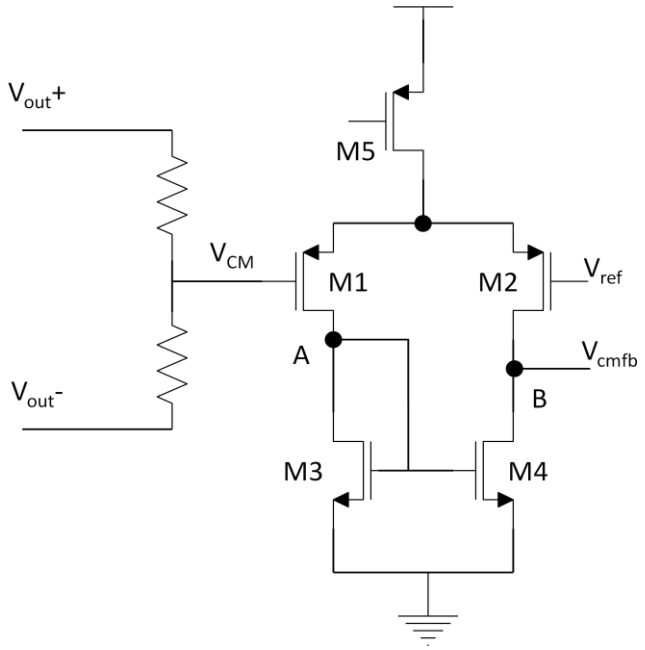


Figure 6-8 Continuous-time CMFB circuit

The drawback of the continuous-time CMFB topology is the large resistors used, which increases the area. However, the continuous-time CMFB topology does not require any clock switching. It significantly reduces the noise and switching distortions, which is crucial for high resolution modulator design.

Since SOI 1.0 μm process is used in this work, the area of the resistors which are used to sense the output common-mode voltage is no longer a serious concern. Moreover, if the switched capacitor CMFB topology is applied, a separate faster clock is necessary in order to resolve the voltage drooping issue because the sampling frequency is not high in this work. However, this introduces the synchronization problem. In addition, during the hold phase of the integrator, the switching of the CMFB circuit causes significant switching spikes as well as switching noise. This is not acceptable for high resolution requirement. Therefore, the switch capacitor CMFB method is not chosen in this work.

6.3.3.3 Single CMFB Loop vs. Double

Since the two-stage fully differential amplifier topology is adopted, there are two types of CMFB configurations, namely single-CMFB-loop configuration and double-CMFB-loop configuration. As shown in 6-9, a single-CMFB-loop configuration senses the differential output signal and feeds back the control signal to the tail of the first stage, M10. The control signal tunes the DC level of the first stage output, which is the input of the second stage. The double-CMFB-loop configuration as shown in Figure 6-10 comprises of two CMFB loops. The first CMFB loop senses the first stage differential output (A and B) signal and feeds back the CMFB control signal to the tail transistor M10. Similarly, the second CMFB loop senses the second stage differential output signal and feeds back the CMFB control signal to the tail transistors M11 and M12.

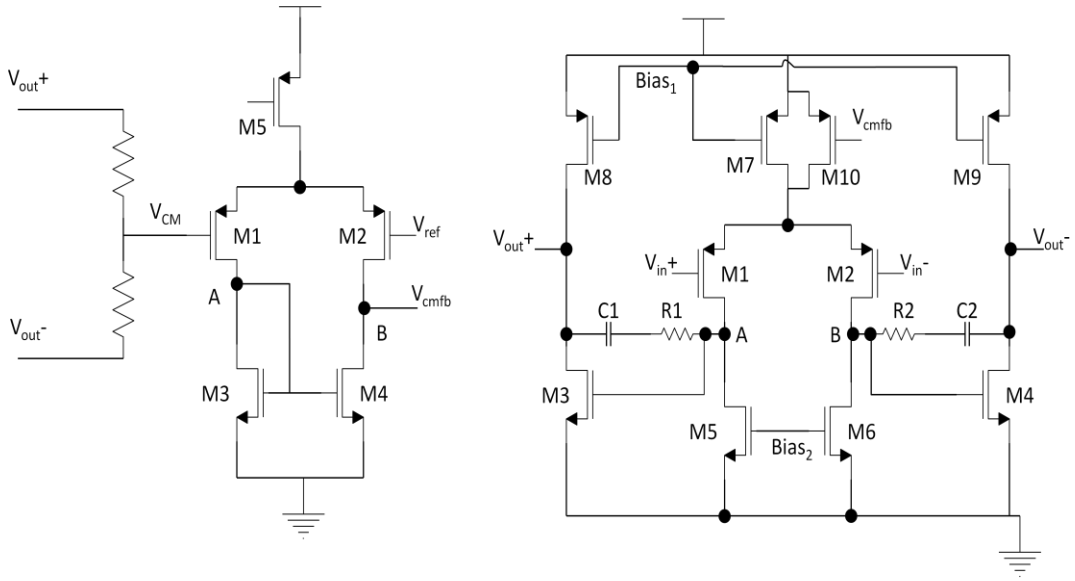


Figure 6-9 Two stage fully differential amplifier with single CMFB loop

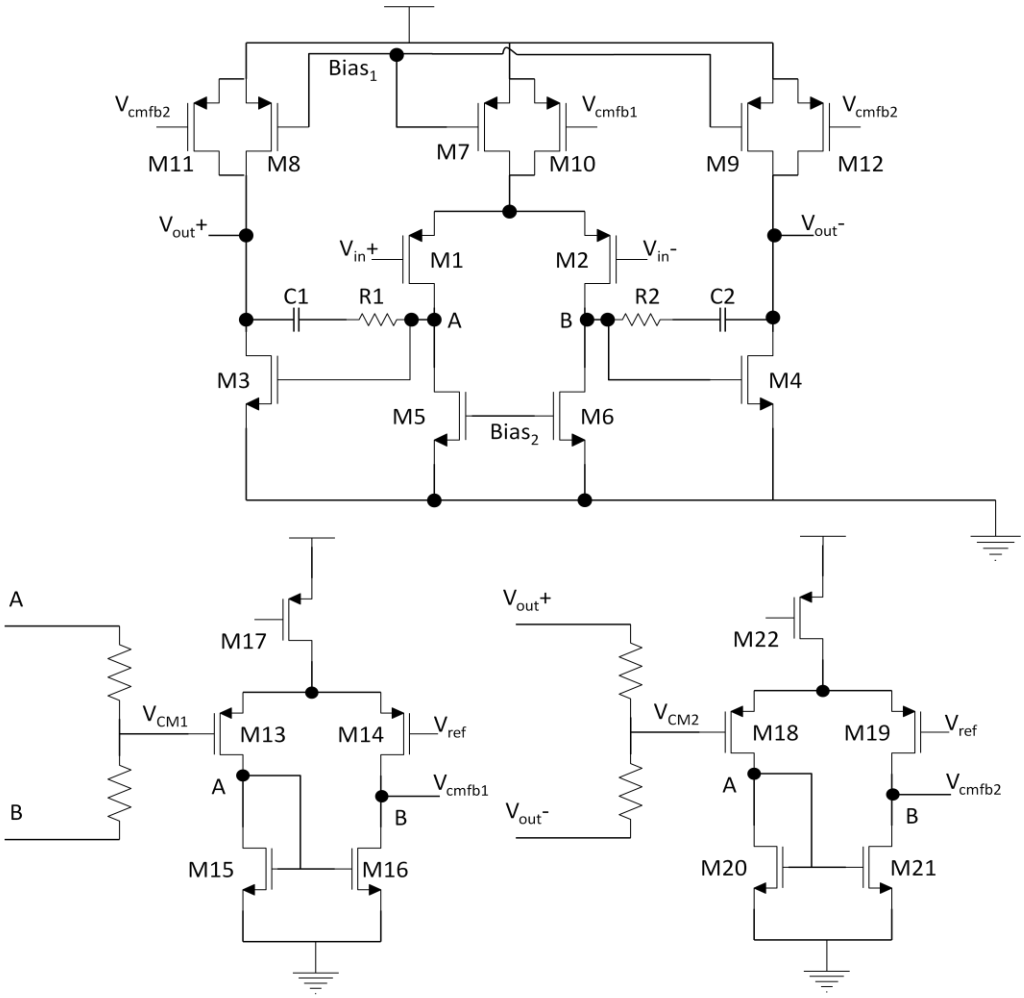


Figure 6-10 Two stage fully differential amplifier with double CMFB loops

Although the single-CMFB-loop configuration is less complex than the double-CMFB-loop configuration in terms of circuitry, it has two major drawbacks. The first drawback is the difficulty of achieving a stable loop. As shown in Figure 6-11, the CMFB loop can be viewed as a three-stage amplifier (CMFB consists of a differential pair comparator). The open loop transfer function comprises of three poles. Even though the required bandwidth for CMFB is as low as DC bandwidth, proper compensation must be done in order to achieve a stable loop. However, the compensation capacitor inserted may directly affect the amplifier's bandwidth. Another major drawback is the difficulty to achieve correct DC bias for first stage transistors within the temperature range for all process corners, since

the CMFB control transistor supplies a small current to tune the common-mode voltage. The tuning ability for transistor M10 is limited. When temperature varies, the first stage output DC voltage may not be correct. Figure 6-12 shows the temperature dependence of the first stage output signals' common mode voltage. At the temperature range from 75 ^{o}C to 225 ^{o}C, the DC level at A and B varies significantly which leads to malfunction of amplifier.

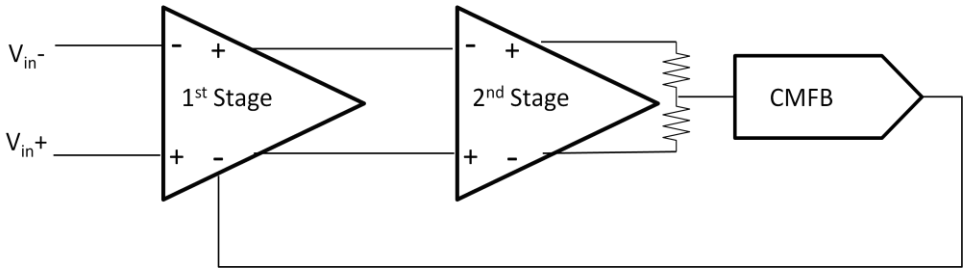


Figure 6-11 Block diagram of single loop CMFB topology

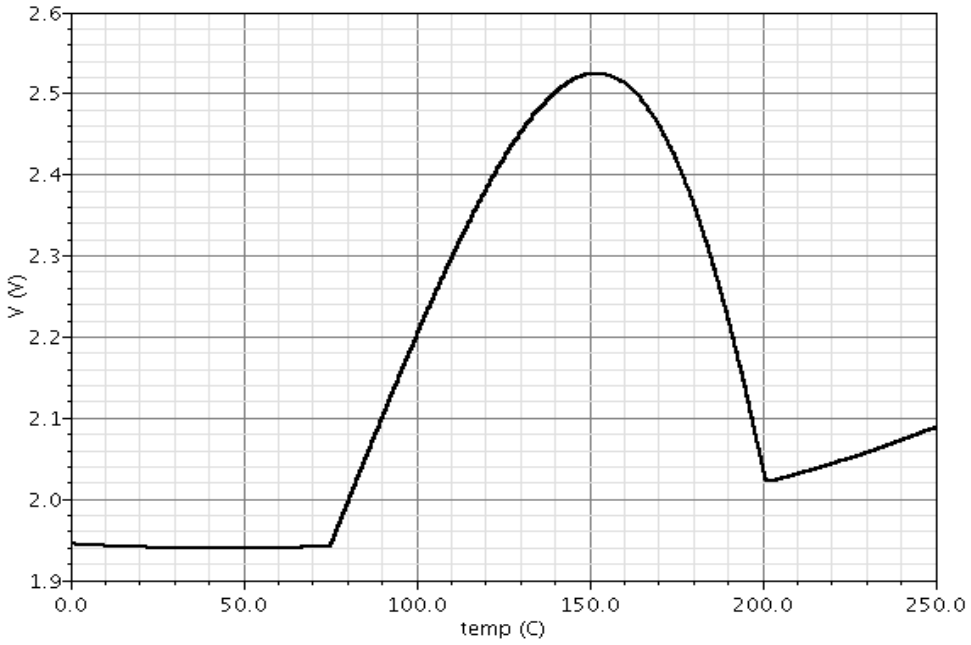


Figure 6-12 DC level of 1st stage output at different temperatures

For the double-CMFB-loop configuration, the output DC level of the first stage is controlled by the first CMFB loop. When temperature varies, the DC level of the first stage output can be fixed. This simplifies the design of the second stage. Moreover, each

CMFB loop contains two stages, which is easy to compensate. Therefore, in this work, the double-CMFB-loop configuration is chosen.

6.3.4 Biasing Circuit

The biasing circuit as shown in Figure 6-13 adopts the constant gm biasing techniques. As introduced in section 3.6.2, the transconductance gm is temperature and process invariant based on the assumption of ideal resistance of R. In order to reduce the temperature effects on the resistor. The temperature coefficients cancelling method is used. With proper sizing of the two types of resistors Rhires and Rmidres, the total resistance R shows minimum variation with temperature changes. The simulated resistance versus temperature is shown in Figure 6-14.

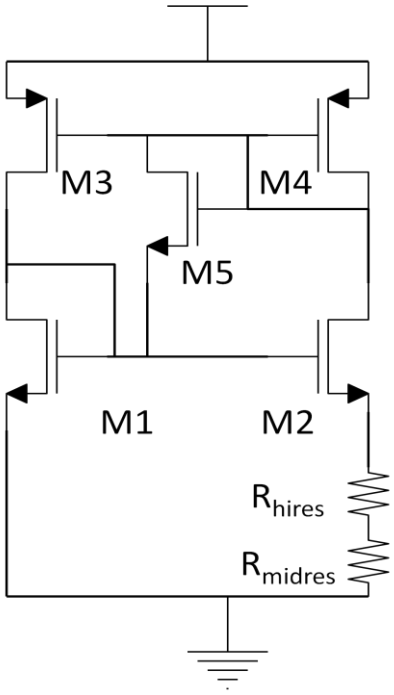


Figure 6-13 Biasing circuit

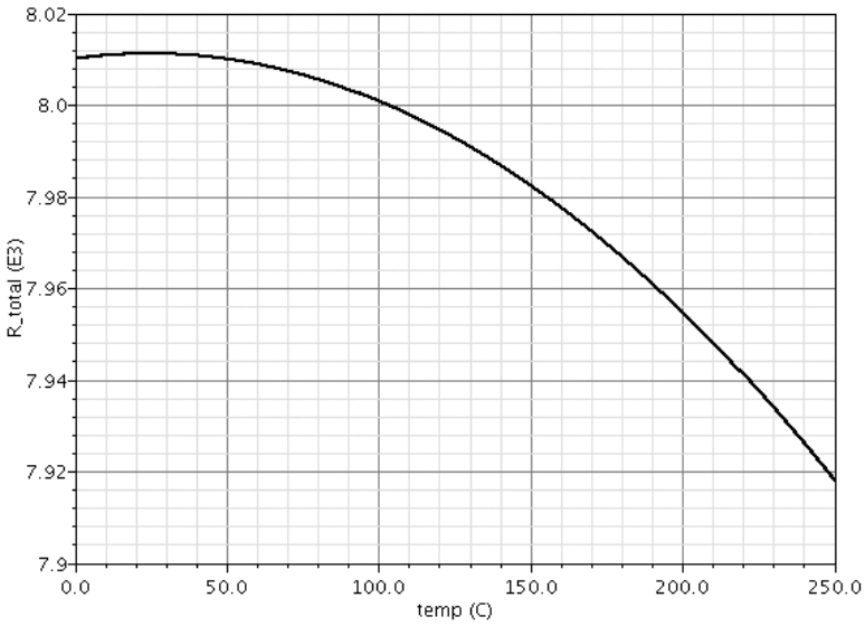


Figure 6-14 Simulated total resistance

The final amplifier schematic is shown in Figure 6-15. Capacitor $C_{1,2}$ and resistor $R_{1,2}$ are connected in series for compensation.

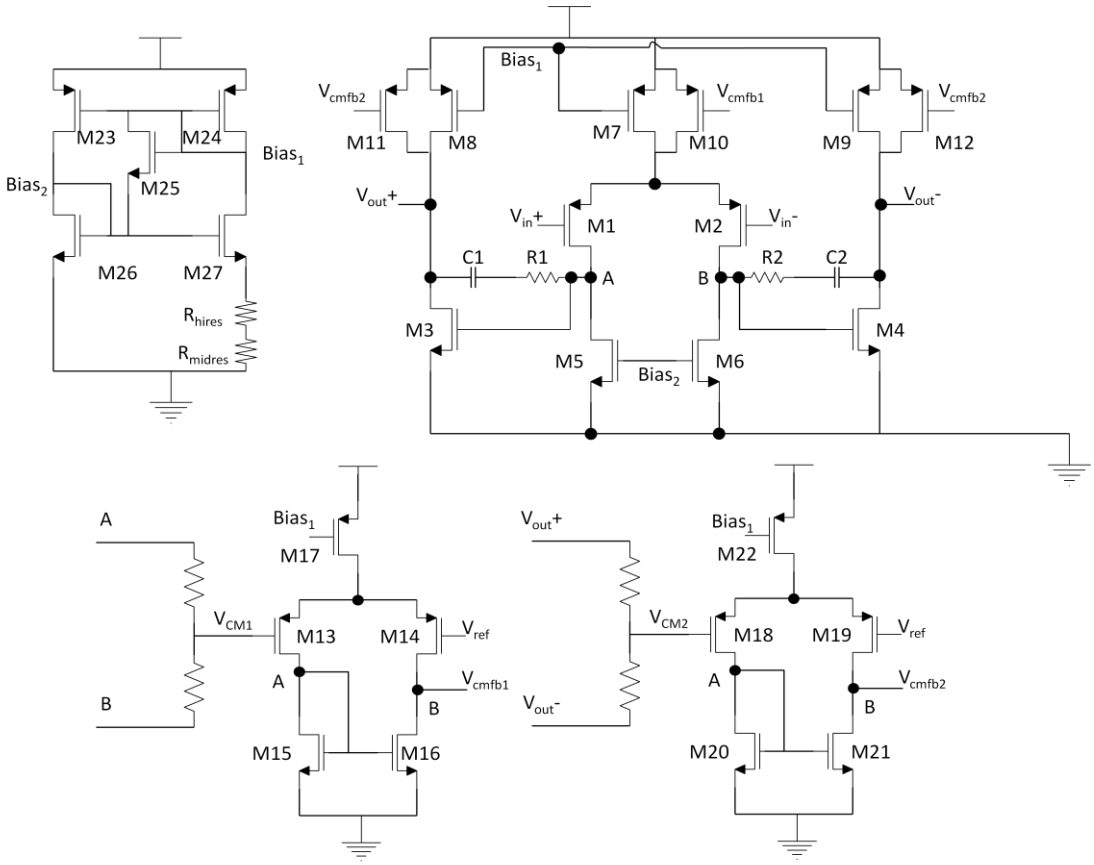


Figure 6-15 Final schematic of amplifier

6.3.5 Simulation Result of Amplifier

The simulated transient responses for temperature at 0 ^{o}C, 120 ^{o}C and 225 ^{o}C are shown in Figure 6-16. The output swing is from 1V to 4V, which meets the specification. The temperature sweep of the first stage output common-mode voltage and second stage output common-mode voltage is shown in Figure 6-17. As temperature varies from 0 ^{o}C to 225 ^{o}C, the dc voltages are stable with a small amount of variations.

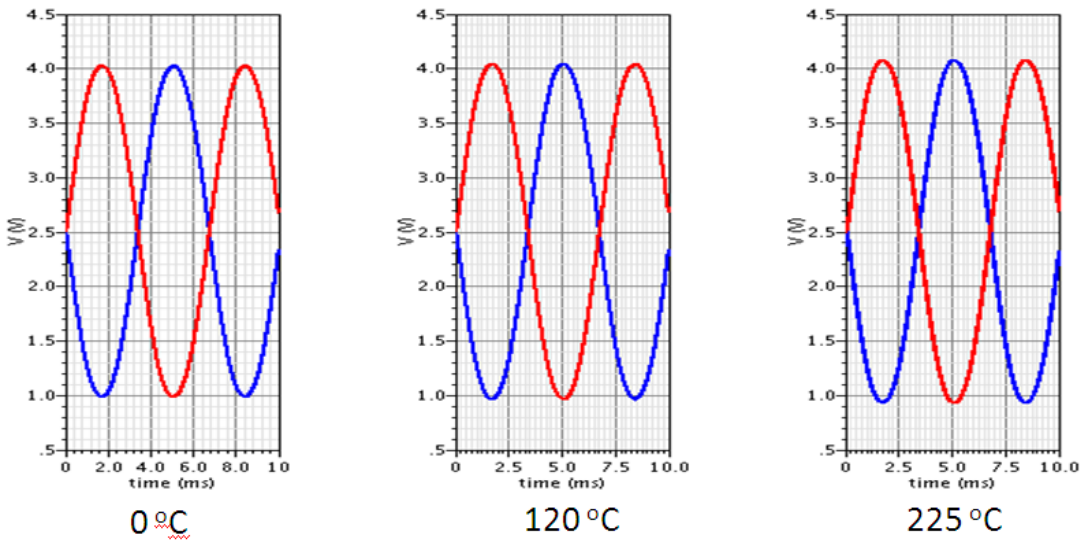


Figure 6-16 Transient plot of amplifier at different temperatures

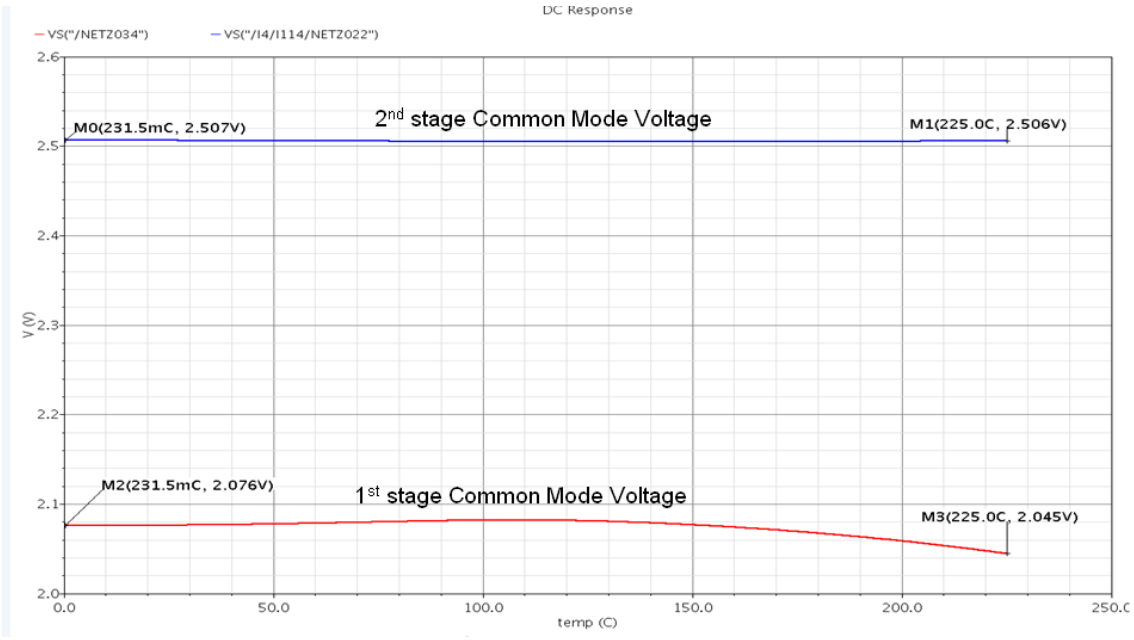


Figure 6-17 Output DC levels of 1st and 2nd stages at different temperatures

The simulated AC responses at three temperatures are shown in Figure 6-18, 6-19 and 6-20, respectively. The results are summarized in Table 6-1.

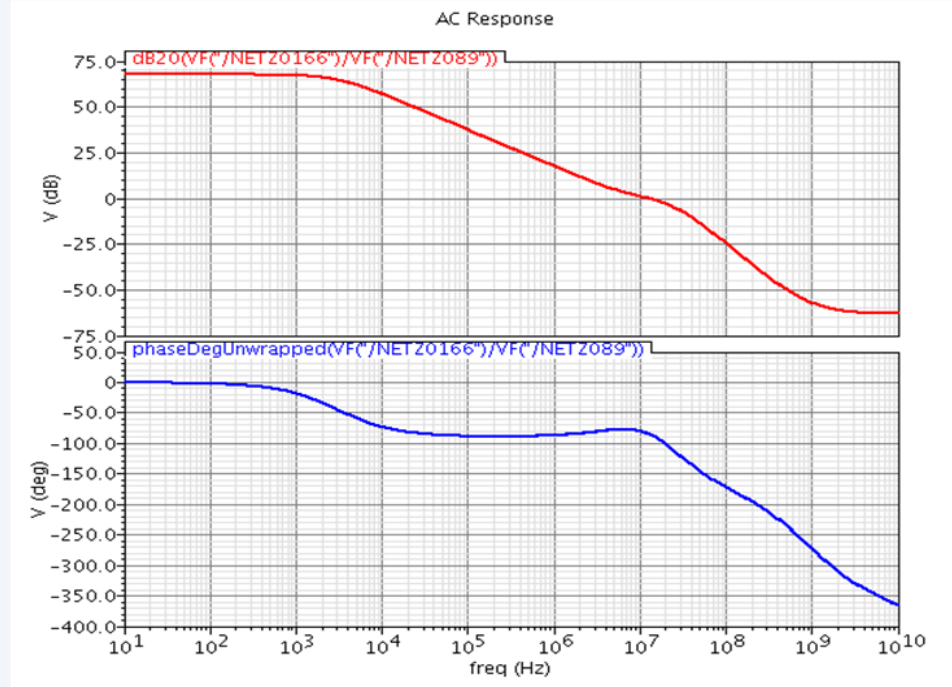


Figure 6-18 Gain and phase plot at 0 °C

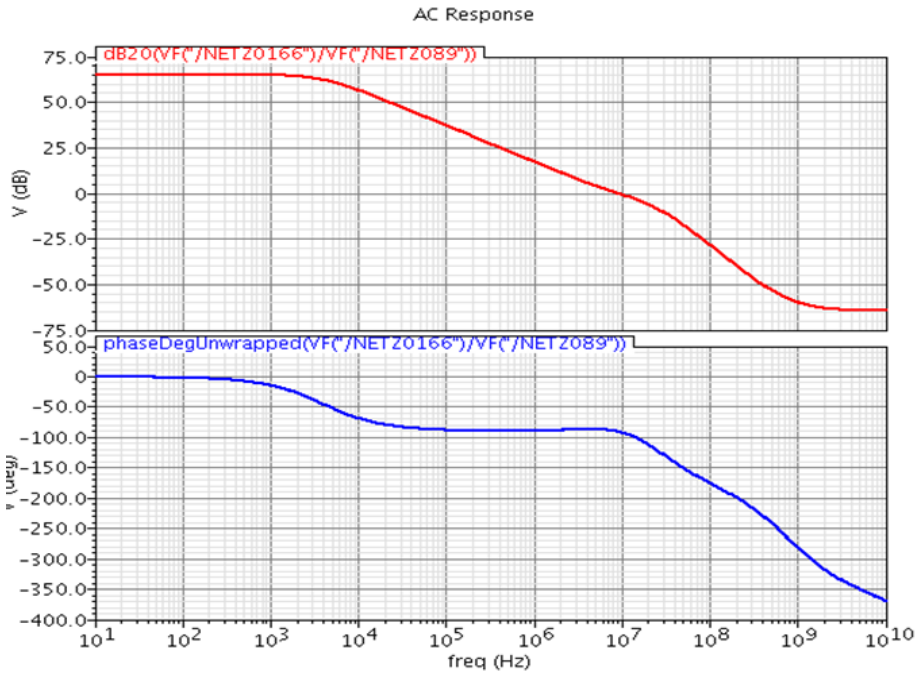


Figure 6-19 Gain and phase plot at 120 °C

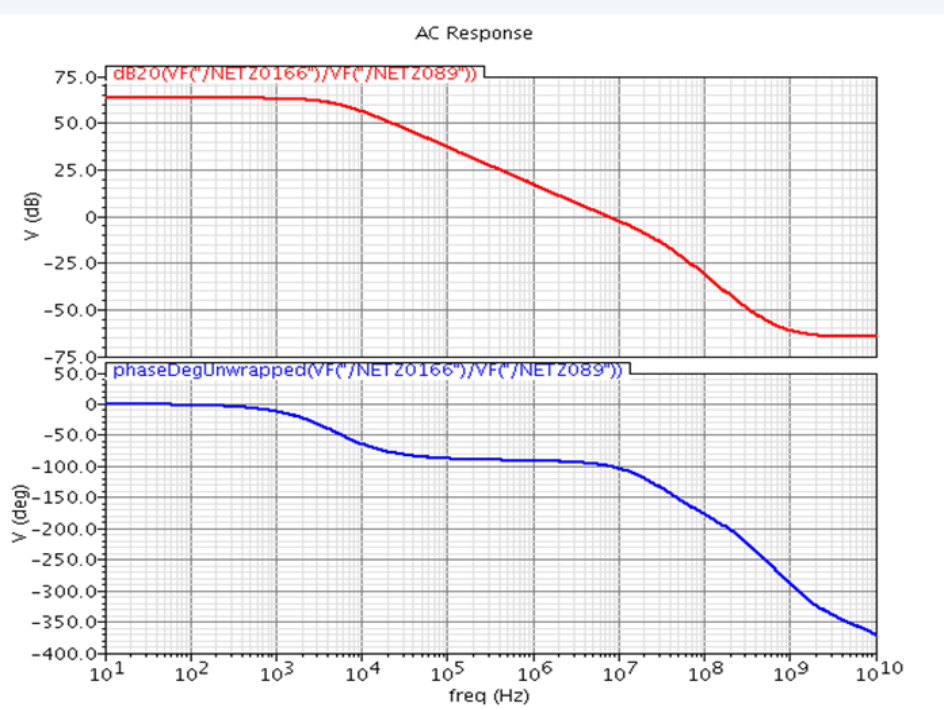


Figure 6-20 Gain and phase plot at 225 °C

Table 6-1 Amplifier AC performace

Temperature	Gain	Phase
0 °C	67.2 dB	100°
120 °C	65 dB	90°
225 °C	63 dB	80°

The power consumption of amplifier is simulated and shown in Figure 6-21.

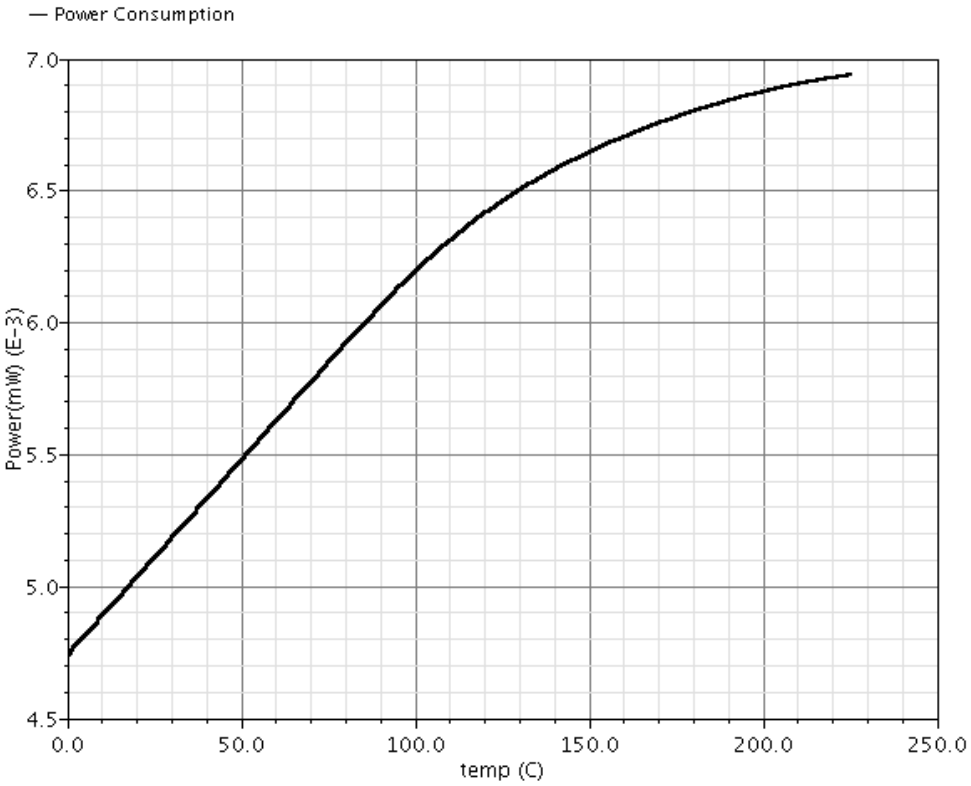


Figure 6-21 Amplifier power consumption at different temperatures

6.4 Clock generator

6.4.1 Clock Scheme

In switched capacitor integrator, one of the major concerns is the clocking scheme. As shown in Figure 6-22, when S1 and S2 are both switching simultaneously, the input and output point may be shorted during the transient. This will cause the error in charge redistribution between C_s and C_{fb}. To solve this, a non-overlapping clock scheme is applied. Figure 6-23 shows clock waveform. The non-overlapping period T_{NOV} must be guaranteed so that S1 and S2 will not be turn on at the same time.

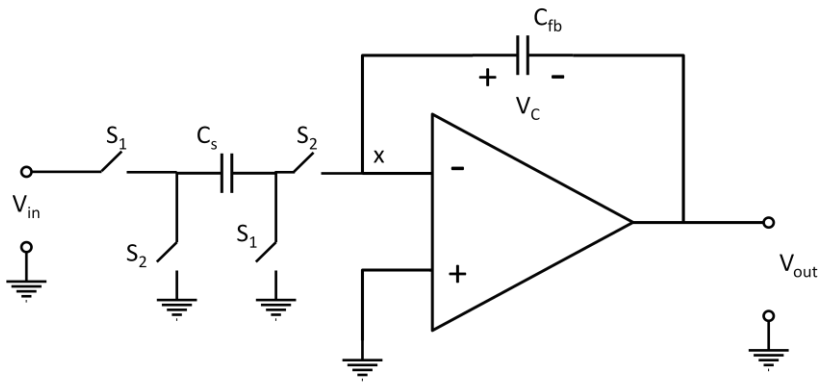


Figure 6-22 Integrator schematic

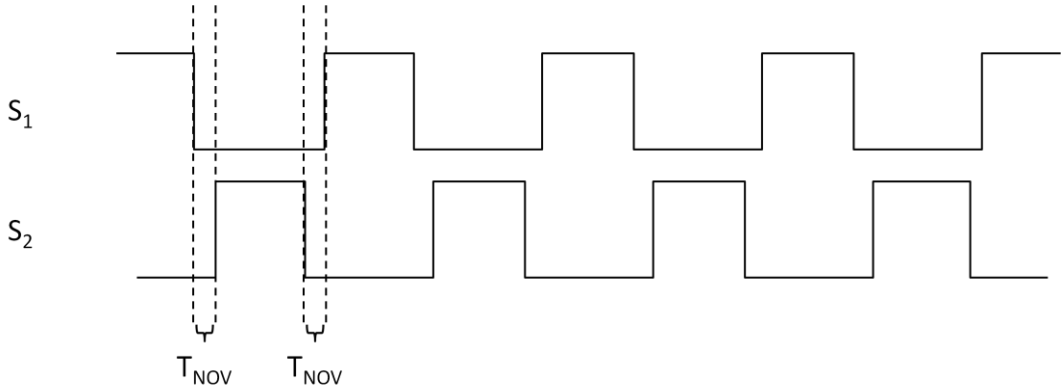


Figure 6-23 Non-overlapping clock waveform

In addition, since the bottom plate sampling technique is applied, clock S1 and S2 require delayed versions S1d and S2d. Therefore, the overall clock waveform is shown in 6-24.

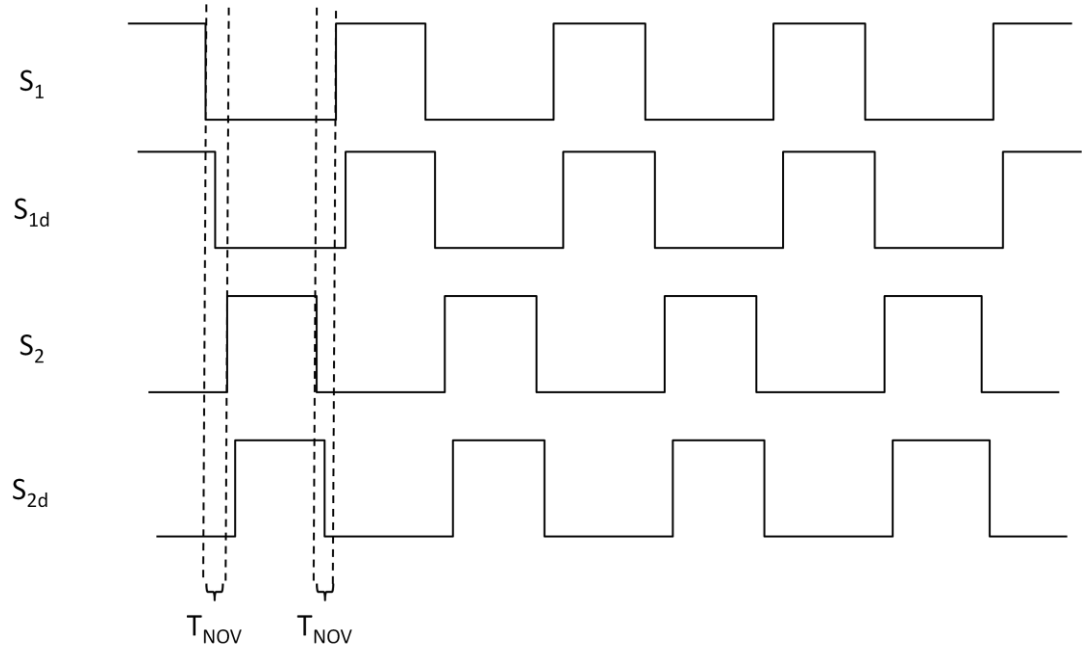


Figure 6-24 Non-overlapping with delayed clock waveform

6.4.2 Clock generator

In order to generate two phase non-overlapping clocks with delayed clocks as introduced in section 6.4.1, a clock generator is required. As shown in Figure 6-25, the clock generator circuit is built on NAND-flip flop with delay chain.

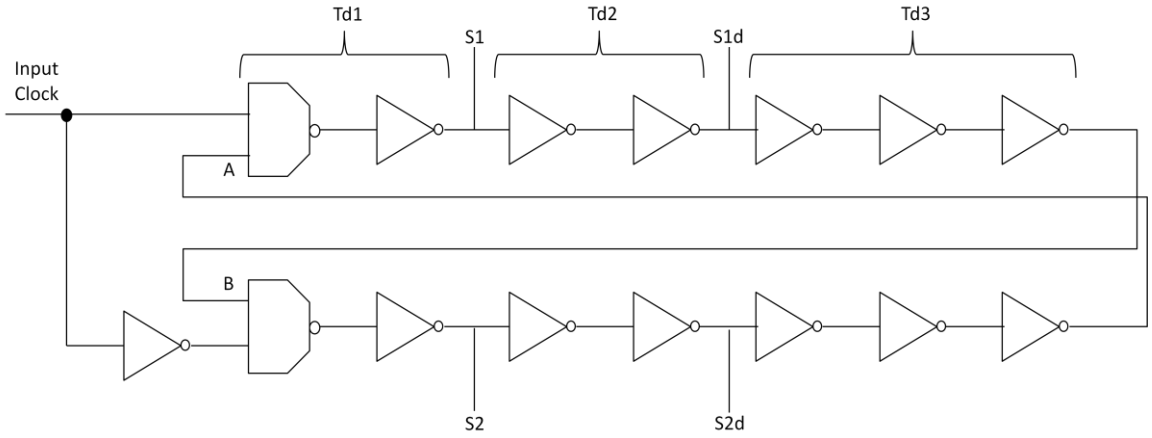


Figure 6-25 Clock generator schematic

Table 6-2 shows the signals toggles at different time points.

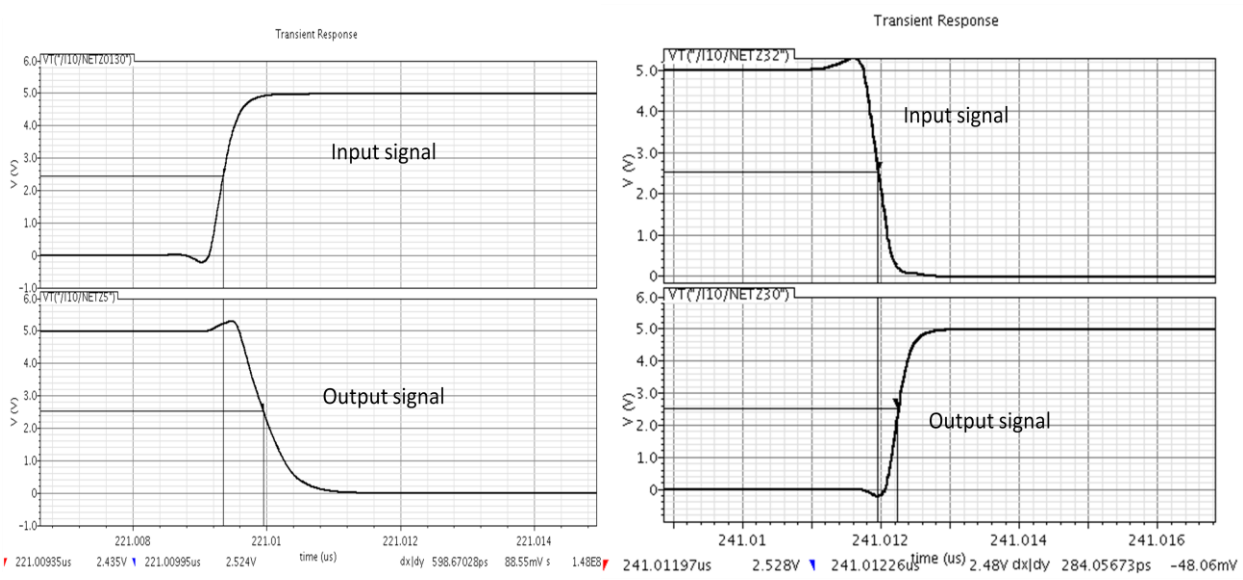
Table 6-2 Clock generator timing table

Time	clock input	S1	S1d	S2	S2d
<0	1	1	1	0	0
0	0	1	1	0	0
td1	0	0	1	0	0
td1+td2	0	0	0	0	0
2td1+td2+td3	0	0	0	1	0
2td1+2td2+td3	0	0	0	1	1
…	0	0	0	1	1
1/2T	1	0	0	1	1
1/2T+td1	1	0	0	0	1
1/2T+td1+td2	1	0	0	0	0
1/2T+2td1+td2+td3	1	1	0	0	0
1/2T+2td1+2td2+td3	1	1	1	0	0
…	1	1	1	0	0

T is the period of the input clock. Td1 is the time delay introduced by NAND gate and inverters from input clock to S1. Td2 is the time delay introduced by inverters from S1 to S1d (same as from S2 to S2d). Td3 is the time delay introduced by inverters from S1d to B (same as from S1d to A). The table shows that S1 (S1d) and S2d (S2) can never be 1 at same time. A minimum time delay of Td1+Td3 is the non-overlapping period.

6.4.3 Simulation Result of Clock generator

The simulated delay of NAND gate and inverters are shown in Figure 6-26a and Figure 6-26b. The NAND gate introduces a delay of 600 ps and the inverter introduces a delay of 284 ps. In order to achieve robust performance, a certain margin of 6 ns is chosen by inserting 20 more inverters. The overall non-overlapping period is 6.2 ns.



(a) NAND gate delay (b) Inverter delay

Figure 6-26 Delays of NAND gate (a) and inverter (b)

Figure 6-27 shows the simulation result of clock generator. The non-overlapping delay is 6.4 ns.

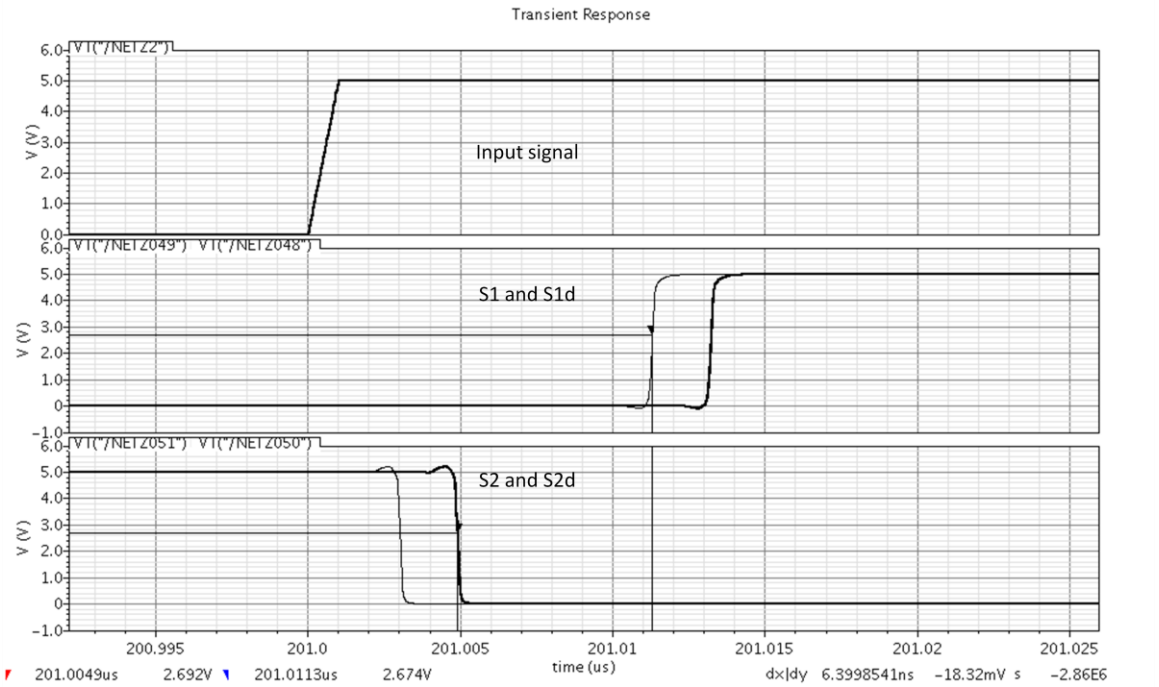


Figure 6-27 Clock generator output waveform

6.5 Comparator

6.5.1 Comparator Circuit Schematic

Since the quantization level required is one bit, a dynamic latch comparator [46] as shown in Figure 6-28 is adopted for simplicity. During operation, when clk is 0, M9 and M10 are switched on while M3 and M4 are switched off. Nodes Vout+ and Vout- are charged to VDD. Therefore, M5 and M6 are switched on. M7 and M8 are switched off. The two branches are exactly the same. In this stage, the input signals Vin+ and Vin- track the output from the previous stage. When clock toggles to 1, M9 and M10 are switched off while M3 and M4 are switched on. If Vin+ is higher than Vin-, V_B is larger than V_A. Hence, Vout- is discharging faster than Vout+. The latch structure will quickly discharge Vout- to ground while latching Vout+ at VDD. For Vin+ is lower than Vin-, A will be kept at VDD and B will be discharged to ground.

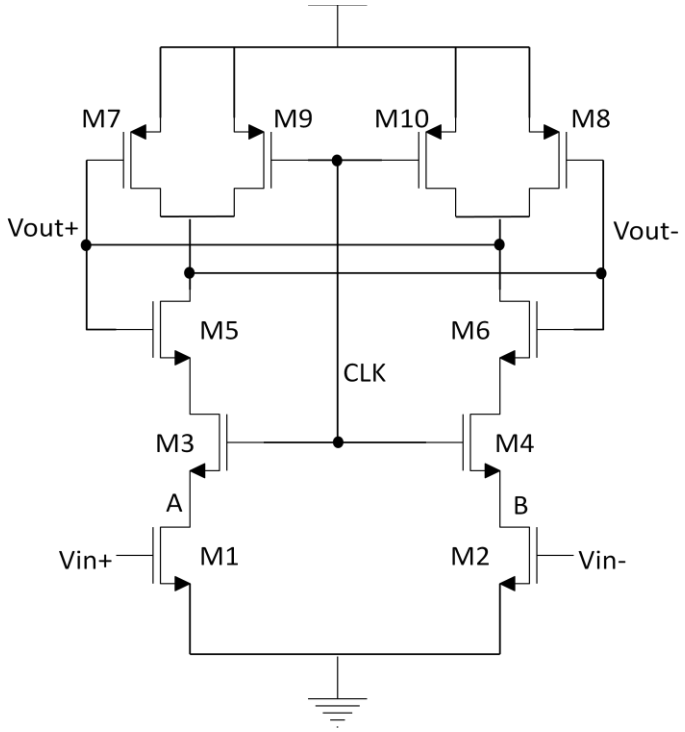


Figure 6-28 Schematic of comparator

6.5.2 Simulation Result of Comparator

Figure 6-29 shows the simulated output of comparator. The input Vin- is kept constant at 2.5V. A ramping signal from 2.48V to 2.52V is fed to input Vin+. As shown in the plot, the output Vout+ is low when Vin+ is less than 2.5V and high when Vin+ is larger than 2.5V. When Vin+ is at the region near 2.5V, fluctuation occurs and the output becomes invalid. It is observed from the plot that the minimum detectable voltage is 10mV.

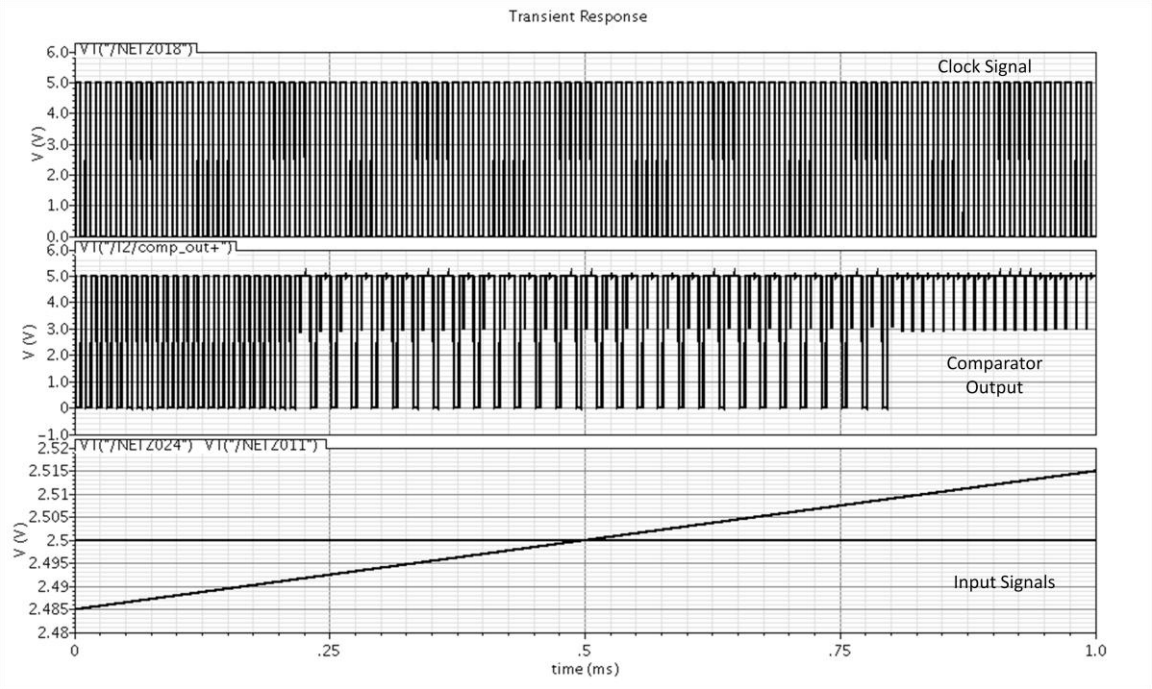


Figure 6-29 Comparator output waveform

6.5.3 Output Latch Schematic

During operation, the output of the comparator is fed to the inputs of the integrators which are controlled by different clocks. This requires the comparator's output to hold for the whole clock cycle, which is achieved by a separate latch as shown in Figure 6-30.

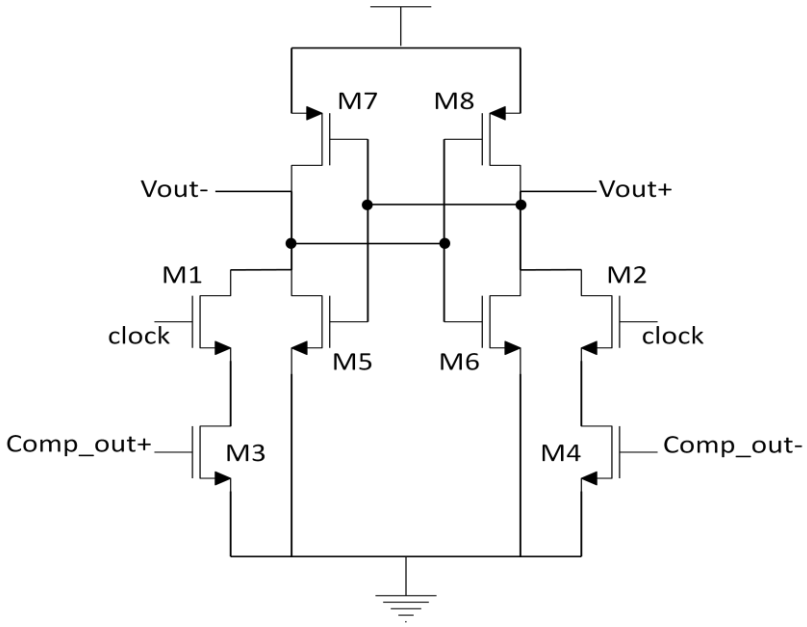


Figure 6-30 Output latch schematic

6.5.4 Simulation Results of Comparator with Output Latch

During operation, when clock is 0, M1 and M2 are switched off and the output voltage is latched with previous value. When clock toggles to 1, M1 and M2 are switched on. The gates of M3 and M4 are connected to the outputs of the comparator. If Comp_out+ is 1 and Comp_out- is 0, the voltage of Vout- is overwritten to 0. This forces Vout+ to be overwritten to 1. In this architecture, the driving ability of M3 and M4 are higher than the two inverters M5+M7 and M6+M8. This is to ensure that the values of Vout+ and Vout- can be overwritten by M3 and M4. Figure 6-31 shows the simulation result of the output latch.

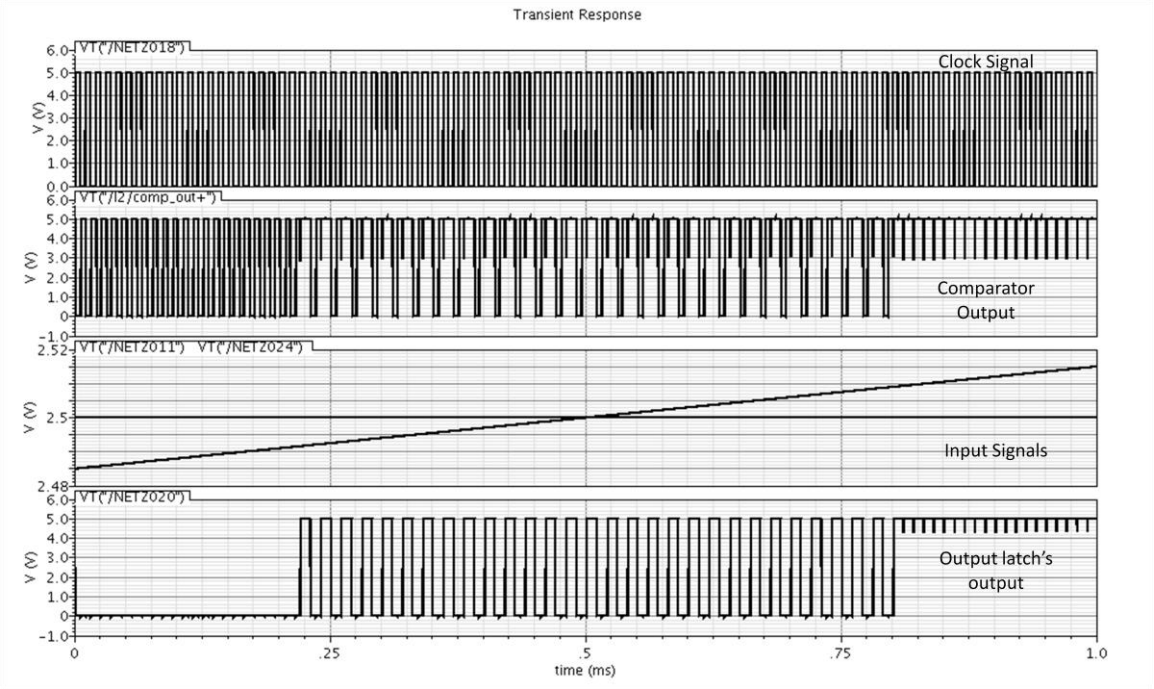


Figure 6-31 Output waveform of comparator with output latch

6.6 Post-Layout Simulation result and discussion

In this work, the layout is designed using xFab 1.0 µm SOI process [47]. The completed modulator layout is shown in Figure 6-32. In addition to the modulator, some stand alone circuit blocks are also included for testing. The whole layout occupies 2.5mmx2.5mm of space. In this process, poly-resistors with negative TC and positive TC are provided to be used to cancel the temperature effects.

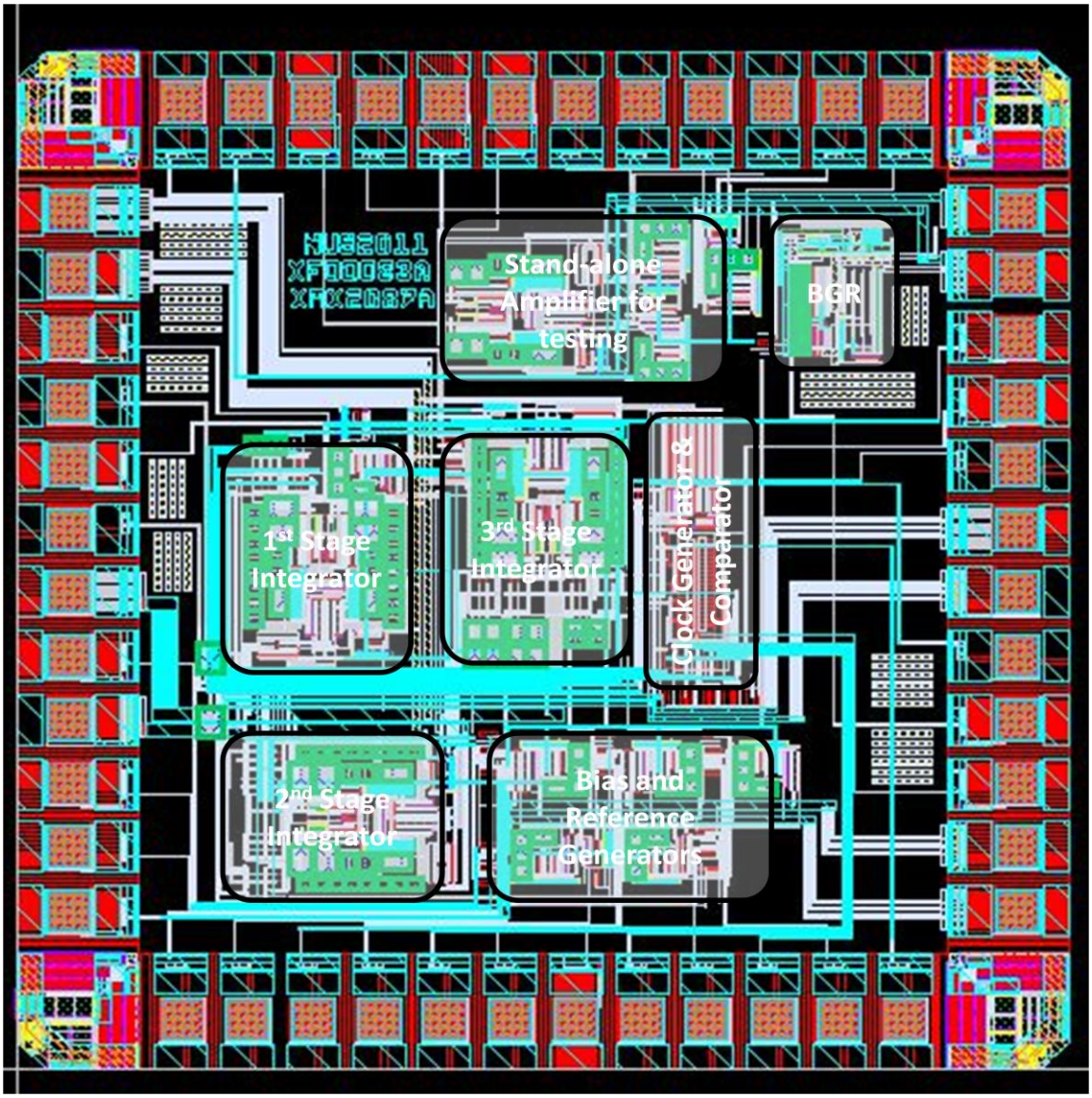


Figure 6-32 Modulator layout

The post-layout simulation is done at 27 ^{o}C, 150 ^{o}C and 225 ^{o}C due to the long simulation time. Figure 6-33 shows the PSDs of the simulated output bit streams. The noise shaping of the curves proves the functionality of modulator at different temperatures.

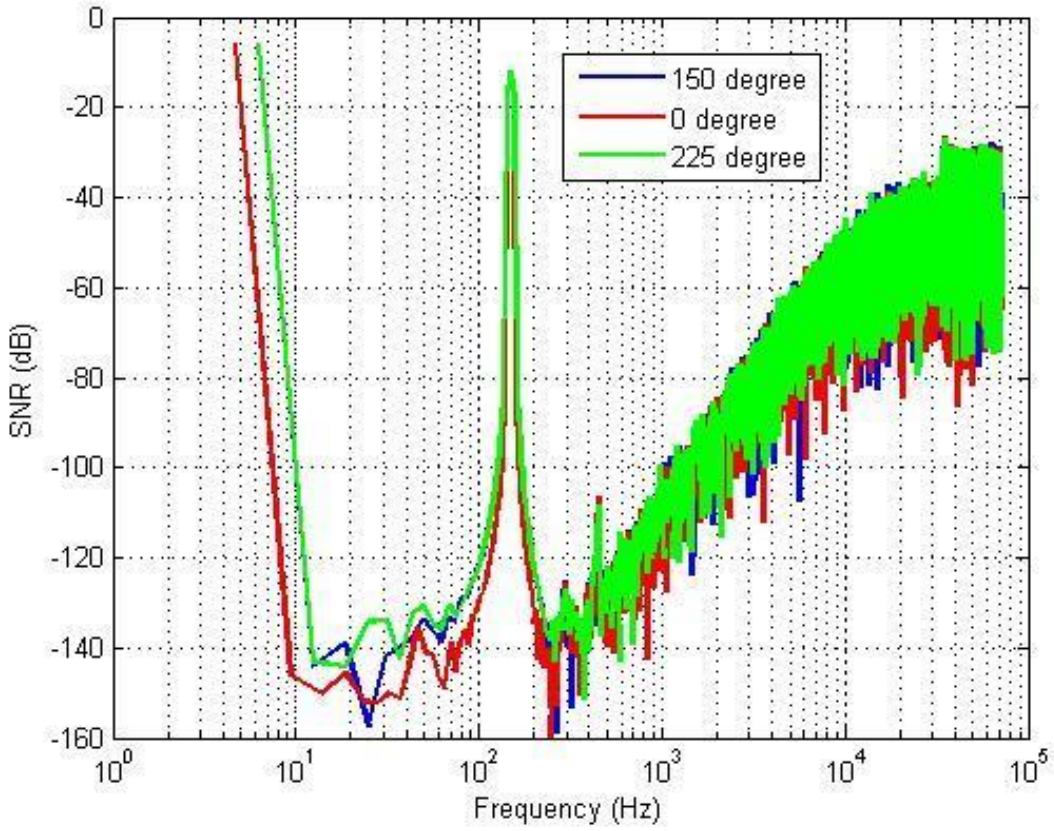


Figure 6-33 PSD of post layout simulation at different temperatures (Simulations are done with input signal amplitude of 1.5V, sampling period of 7us, band-gap reference voltage of 1.12V, supply voltage of 0-5V and reference voltages of 0-5V. Total 30682 points are collected for FFT analysis.)

Figure 6-34 shows the dynamic range of the modulator at 27 ^{o}C and 225 ^{o}C.

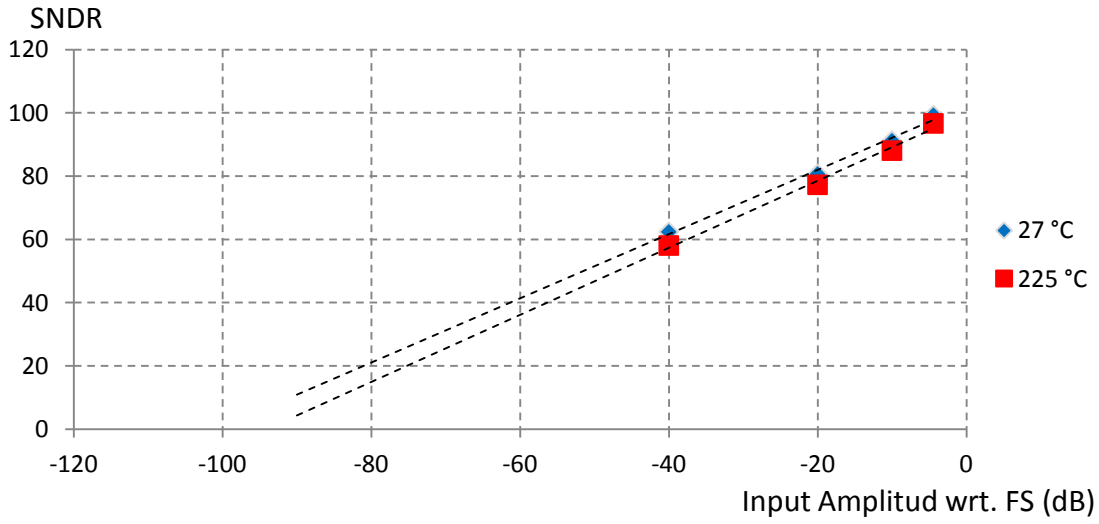


Figure 6-34 Dynamic range plot

Table 6-3 summarizes the post-layout simulation results at different temperatures.

Table 6-3 Summary of key performance parameters

ΣΔ modulator				
Target Specification		Post Layout Simulation Results		
		0 ℃	**150 ℃**	**225 ℃**
Input Bandwidth	250 Hz	250 Hz	250 Hz	250 Hz
Clock Frequency	128kHz	140kHz	140kHz	140kHz
Input Maximum Amplitude	1.5V	1.5V	1.5V	1.5V
Temperature Range	up to 225 ^{o}C	0 ℃ to 225 ℃	0 ℃ to 225 ℃	0 ℃ to 225 ℃
SNR/SNDR	102 dB	106.1 dB/99.3 dB	105.3 dB/98.7 dB	102.7 dB/98.2 dB
ENOB	17 bits	17.3 bits	17.2 bits	16.8 bits
Power Consumption	<35mW	28.5 mW	35.4 mW	40 mW
Amplifier				
Target Specification		Post Layout Simulation Results		
		0 ℃	**120 ℃**	**225 ℃**
UG Bandwidth	>2MHz	10.2 MHz	9.4 MHz	8.5 MHz
Gain	>60 dB	67.2 dB	65 dB	63 dB
Phase Margin	>60^{o}	100 °	90 °	80 °
Power Consumption	<6mW	4.7 mW	6.4 mW	6.9 mW

6.7 Measurement Results

The COB bonded chip is tested under at different temperatures. The test setup is shown in Figure 6-35. The chip is put into the oven. High temperature wires and BNC cables are used for the connection from the chip to test PCB (outside the oven).

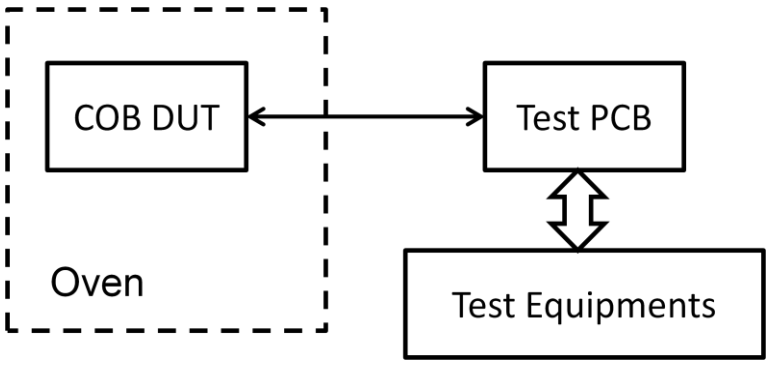


Figure 6-35 Measurement Setup Diagram

Figure 6-36 shows the measured PSDs at temperatures 30 ^{o}C, 150 ^{o}C and 296 ^{o}C. Figures 6-37, 6-38, 6-39, 6-40, 6-41 and 6-42 show the PSDs for different input amplitude at different temperatures. Figure 6-43 shows the peak SNR measured at different temperatures. Figure 6-44 shows the plots SNR against input amplitude at different temperatures. During the measurement, tuning of band-gap reference voltage is required in order to maintain normal functionality of the modulator. At temperature below 120 ^{o}C, the band-gap voltage is set at 1.14V. At temperature between 120 ^{o}C and 225 ^{o}C, the band-gap voltage is tuned to 1.17V. At temperature above 225 ^{o}C, the band-gap voltage is tuned to 1.21V.

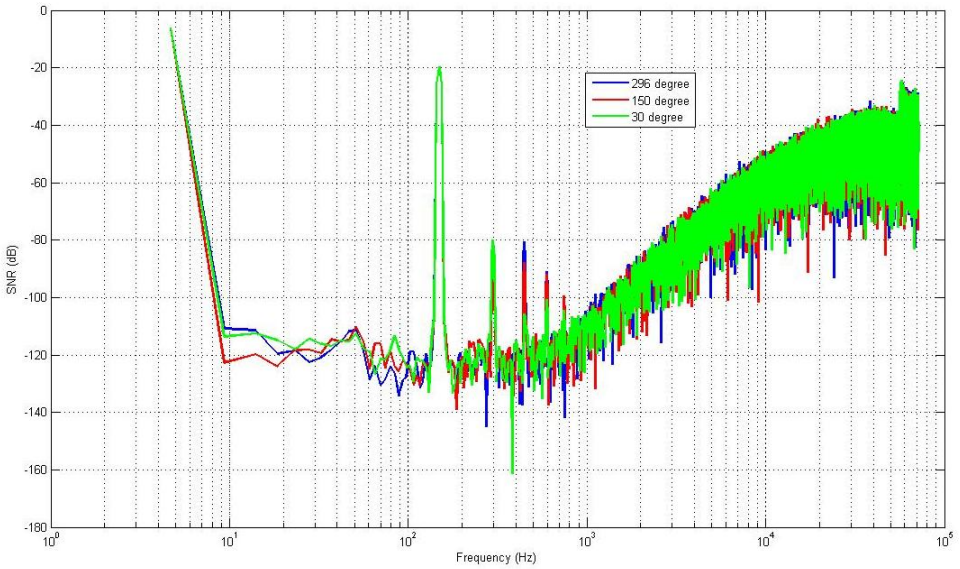


Figure 6-36 Measured PSDs at different temperatures (Measurements are done with input signal amplitude of 1.3V, sampling period of 7us, supply voltage of 0-5V and reference voltages of 0-5V. Total 30682 points are collected for FFT analysis.)

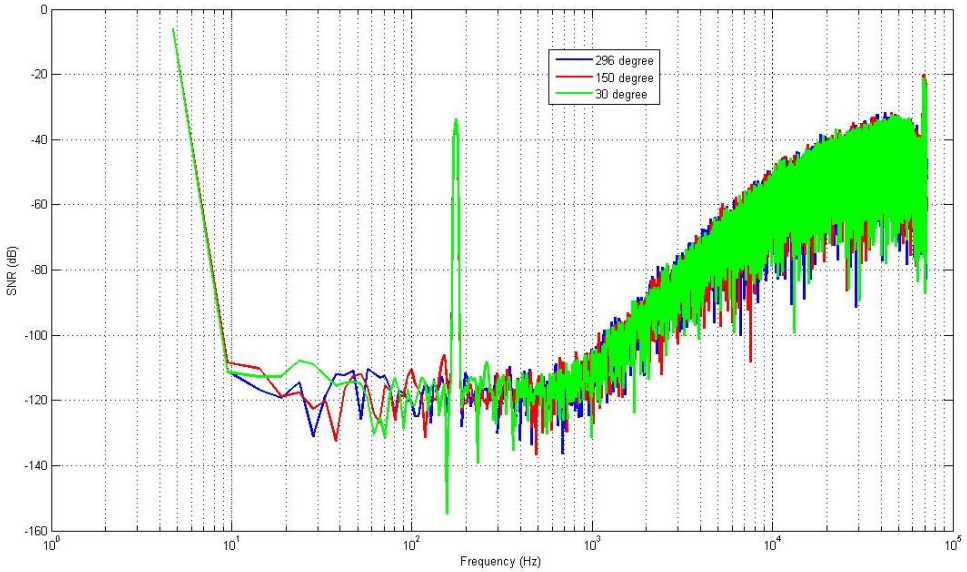


Figure 6-37 Measured PSDs at different temperatures for low input amplitude where distortions are not seen (Measurements are done with input signal amplitude of 250 mV, sampling period of 7us, supply voltage of 0-5V and reference voltages of 0-5V. Total 30682 points are collected for FFT analysis.)

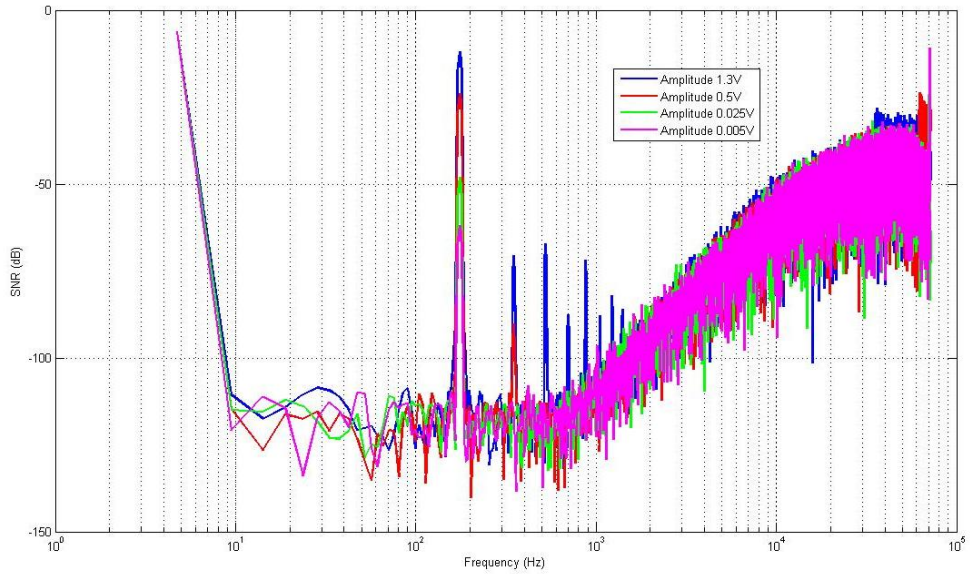


Figure 6-38 Measured PSDs for different input amplitude at 25 °C(Measurement condition same as above. Measured SNRs are 86.8dB@amplitude 1.3V, 77.4dB@amplitude 0.5V, 53.3dB@amplitude 0.025V and 39.3dB@amplitude 0.005V)

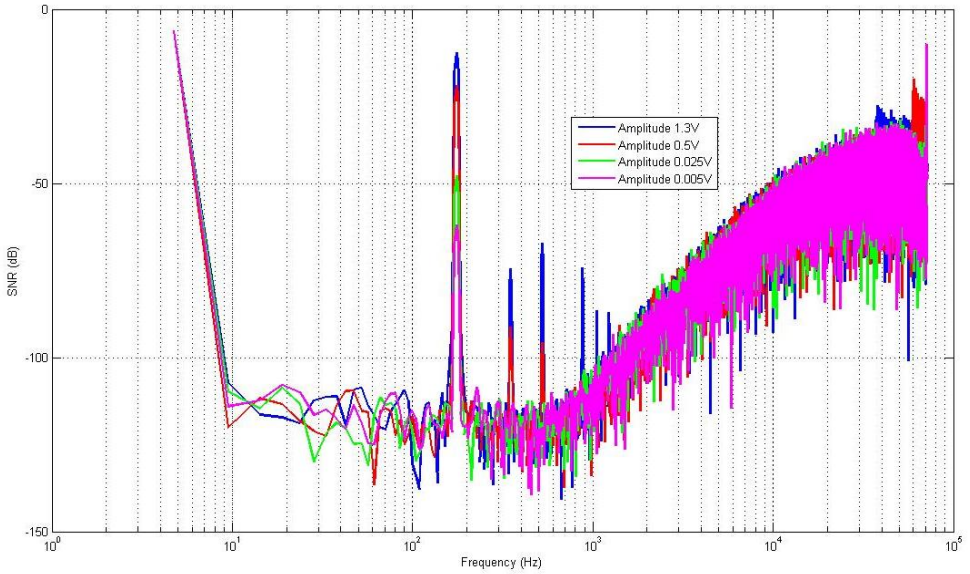


Figure 6-39 Measured PSDs for different input amplitude at 150 °C(Measurement condition same as above. Measured SNRs are 86.7dB@amplitude 1.3V, 79.2dB@amplitude 0.5V, 54.4dB@amplitude 0.025V and 39.2dB@amplitude 0.005V)

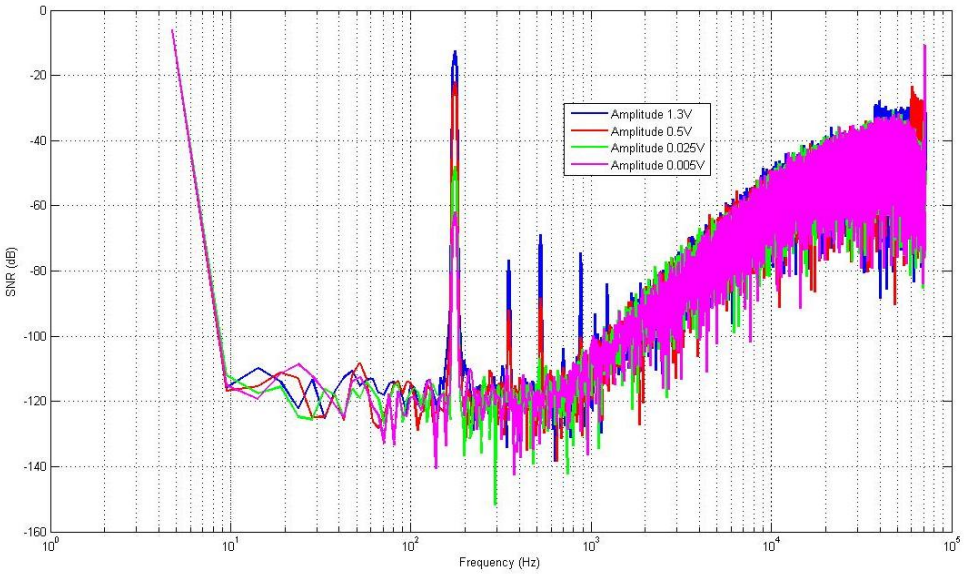


Figure 6-40 Measured PSDs for different input amplitude at 200 °C (Measurement condition same as above. Measured SNRs are 86.1dB@amplitude 1.3V, 79.8dB@amplitude 0.5V, 55.4dB@amplitude 0.025V and 40.3dB@amplitude 0.005V)

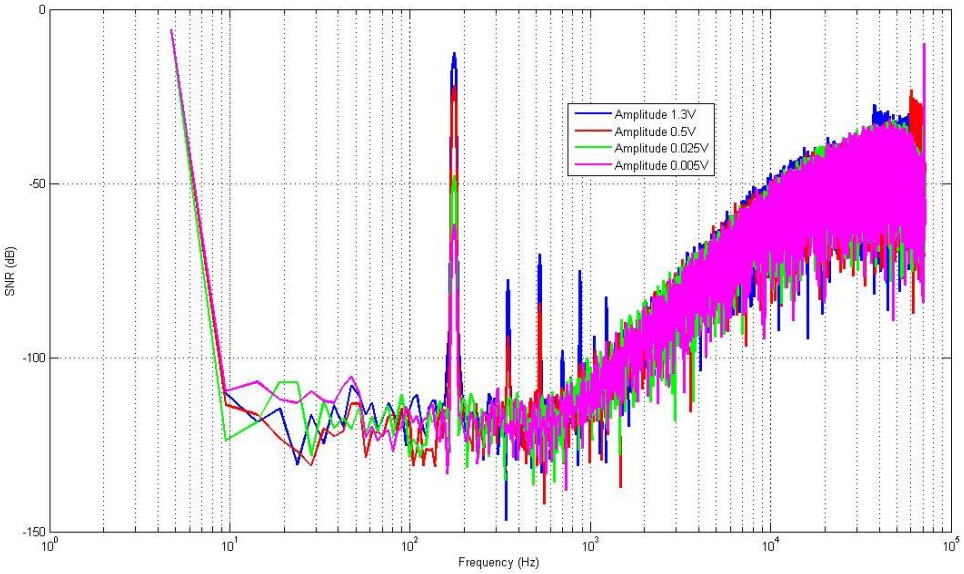


Figure 6-41 Measured PSDs for different input amplitude at 250 °C (Measurement condition same as above. Measured SNRs are 87.2dB@amplitude 1.3V, 80.4dB@amplitude 0.5V, 53.7dB@amplitude 0.025V and 39.6dB@amplitude 0.005V)

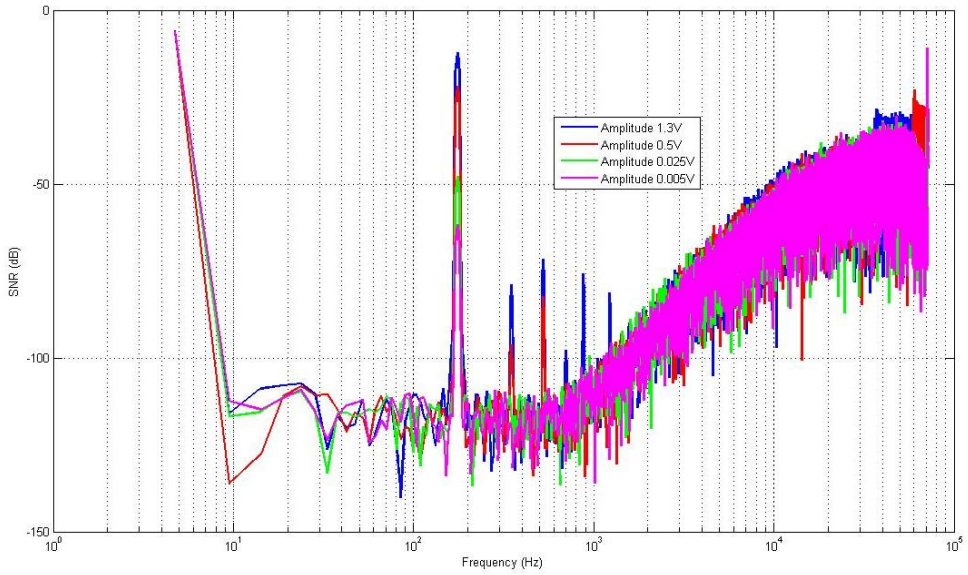


Figure 6-42 Measured PSDs for different input amplitude at 300 °C (Measurement condition same as above. Measured SNRs are 86.3dB@amplitude 1.3V, 80.0dB@amplitude 0.5V, 52.4dB@amplitude 0.025V and 39.13dB@amplitude 0.005V)

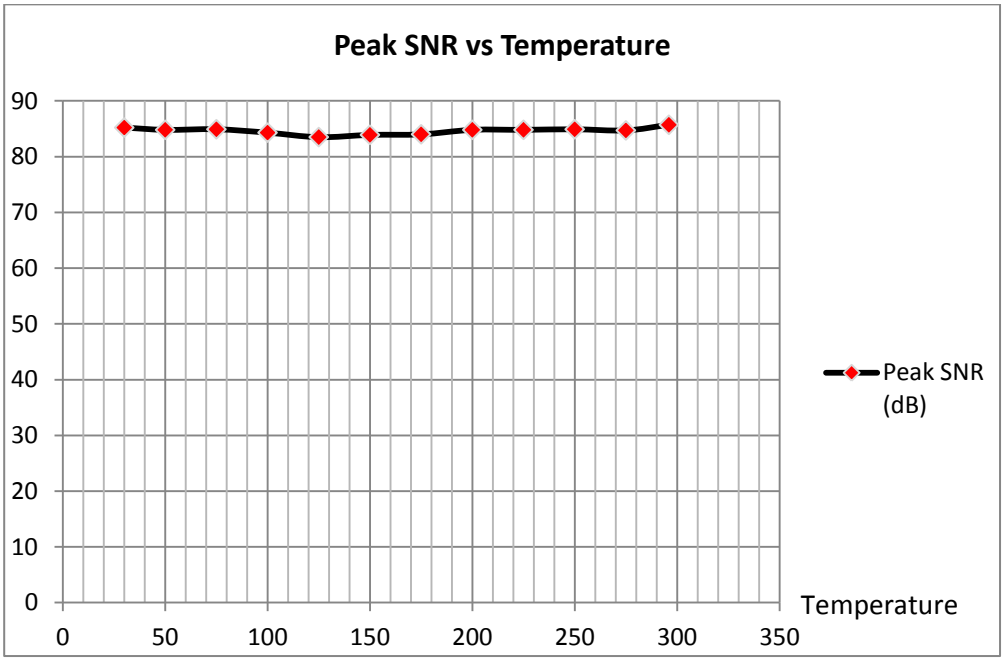


Figure 6-43 Measured peak SNR at different temperatures

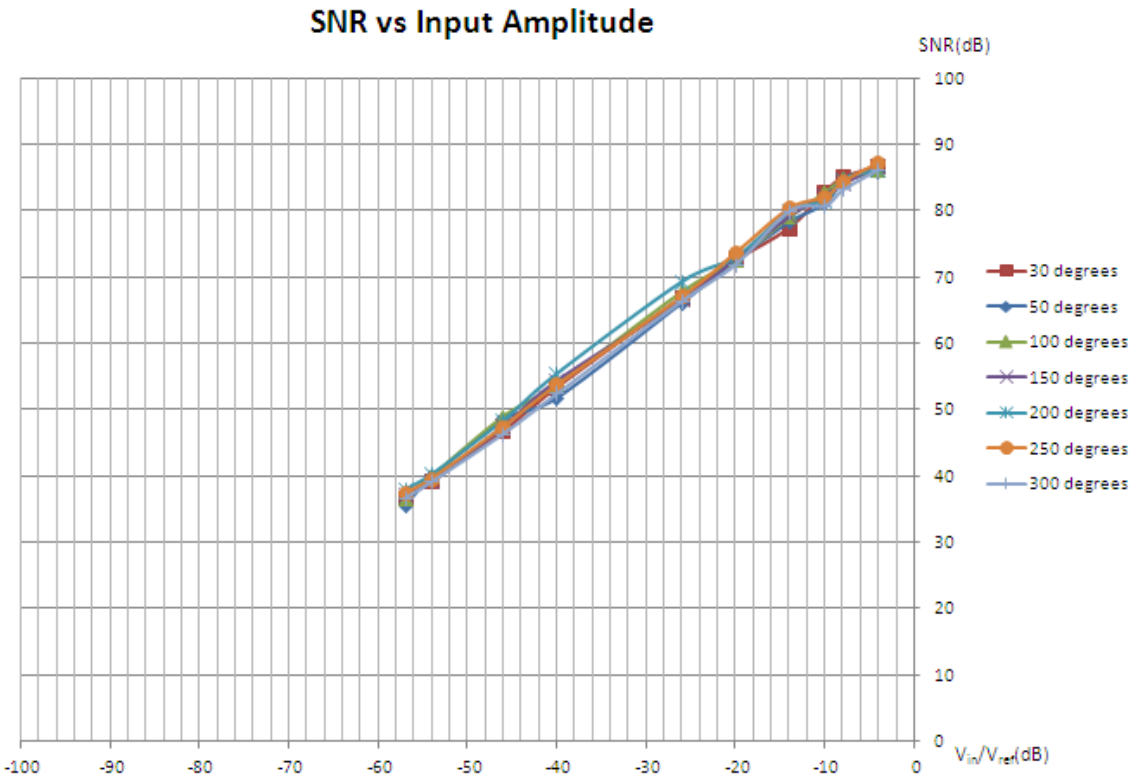


Figure 6-44 Measured SNR against input amplitude at different temperatures

As can be seen from the measurement results, the modulator shows a relatively constant SNR at different operation temperatures. The measured peak SNR is around 87 dB. The measurement results are listed in Table 6-4.

Table 6-4 Modulator Measurement Result Summary

ΣΔ modulator Measurement Results			
Items	Measurement Results		
	0 °C	**150 °C**	**300 °C**
Input Bandwidth	250 Hz	250 Hz	250 Hz
Supply Voltage	0-5V	0-5V	0-5V

Clock Frequency	140kHz	140kHz	140kHz
Input Maximum Amplitude	1.3V	1.3V	1.3V
SNR/SNDR	86.8 dB/65.2 dB	86.7 dB/65.5 dB	86.3 dB/64.8 dB
DR	90 dB	91 dB	89 dB
SFDR	69 dB	70 dB	69 dB
Power Consumption	29 mW	37 mW	42 mW
Chip Area	2.4mm x 2.4mm		
Technology	xFab 1.0μm SOI CMOS		

6.8 Result Analysis and Discussion

6.8.1 SNR drop

One of the main causes for SNR drop is due to thermal noise. It is observed from Figure 6-36, the noise level increased by 20 dB. In the circuit level design, it is assumed that capacitor is the main source of the thermal noise. However, the amplifier also injects noise into the system. As temperature increases from 27 ^{o}C (300 K) to 300 ^{o}C (600 K), the noise power doubles as temperatures almost doubles. This contributes a portion to the SNDR drop.

Another important cause for the SNR drop is due to the gain degradation of amplifier. From 0 ^{o}C to 225 ^{o}C, the amplifier's gain has dropped by 4.2 dB. As shown in section 4.4.2, this gain drop could lead to the performance degradation. This can be verified by

using behavior model of amplifier during the simulation of the modulator. As shown in Figure 6-45, if the gain is decreased by 4 dB, the SNR has dropped by 1.2 dB while other condition remains unchanged.

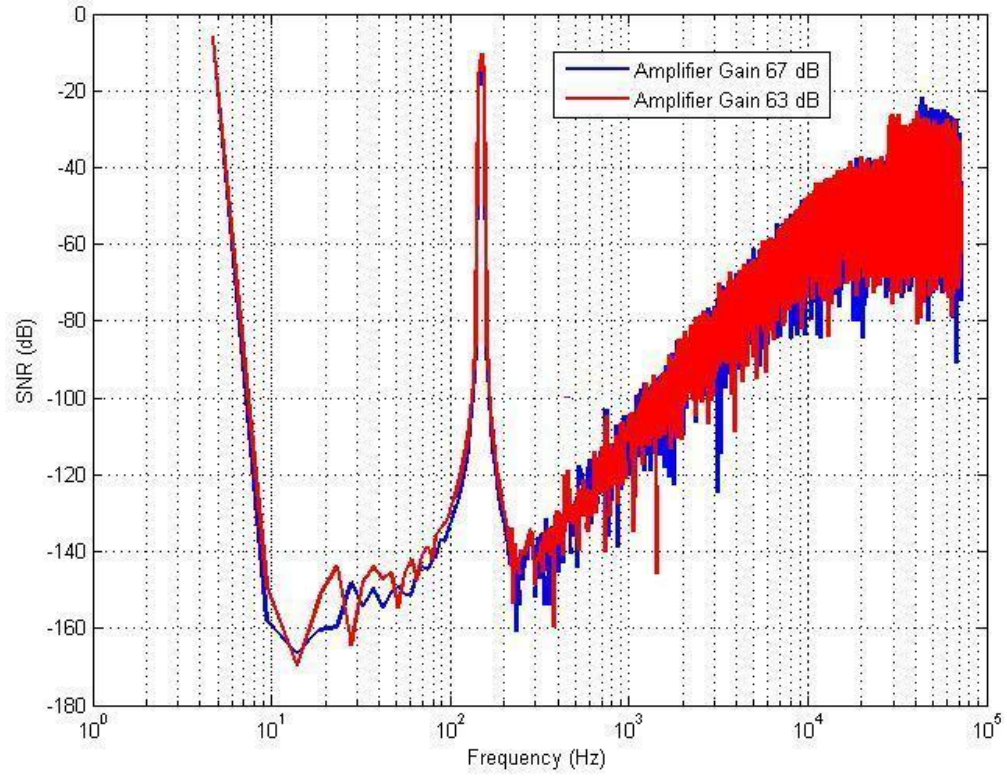


Figure 6-45 PSD simulated with behavior model of amplifier (SNR_{red} = 108.3 dB and SNR_{blue} = 109.5 dB)

6.8.2 3rd-Order Harmonics

As shown in PSD plot of Figure 6-36, a –110 dB of 3rd-order harmonic is present. As introduced in section 2.8, harmonics distortion is due to the non-linearity of the circuit blocks such as amplifiers and capacitors [48]. In this design, the switched capacitor and amplifiers are the two major sources of non-linearity.

For normal switched capacitor circuit, switch and capacitor may be the major sources that lead to non-linearity. However, as shown in the analysis in section 4.3, clock feed through introduce a constant offset to the sampled voltage. Hence it does not have much effect on linearity. Moreover, although charge injection introduces non-linearity to the system, bottom plate sampling technique and the fully differential architecture have almost eliminated charge injection. Therefore, only the capacitor affects the linearity. According to [48] [49], the capacitance of MOS capacitor is not perfectly linear. The capacitance is a function of current voltage of the capacitor as shown in equation (6.5).

$$C_s = C_{s0}\left(1 + \alpha_1 V_{out} + \alpha_2 {V_{out}}^2 + \cdots + \alpha_n {V_{out}}^n\right) \qquad (6.5)$$

By employing an ideal capacitor in the simulation, as shown in Figure 6-46, the 3rd-order harmonics has dropped by 3 dB.

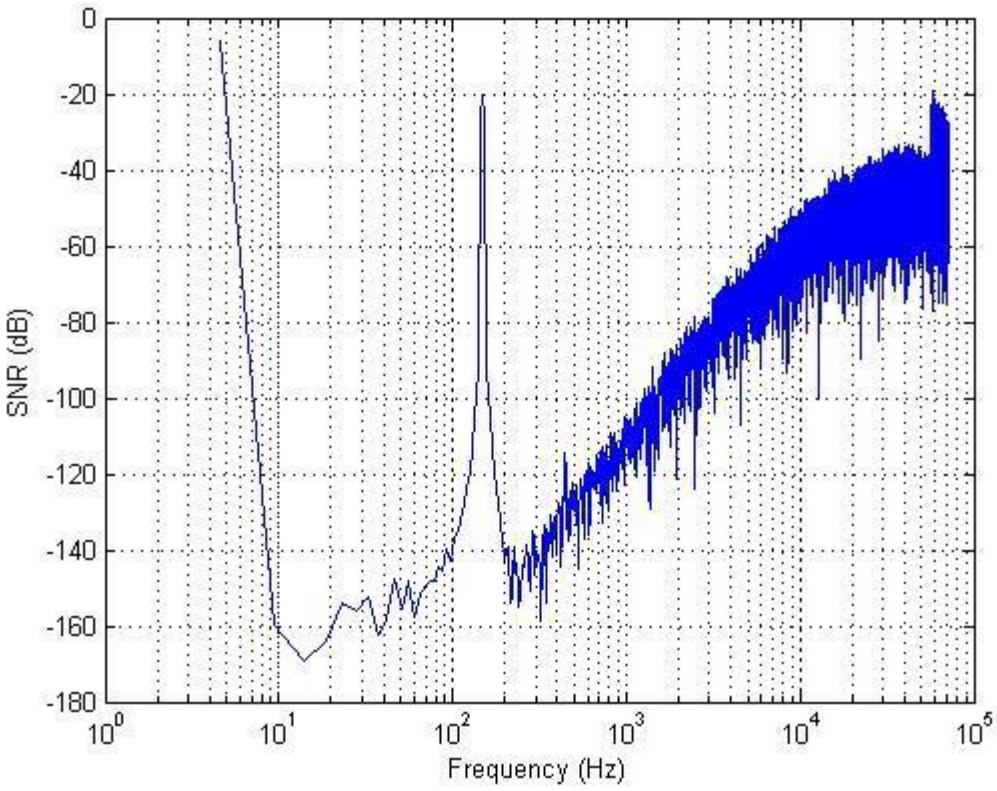


Figure 6-46 PSD simulated with ideal capacitor

Amplifier is another source that contributes to the non-linearity. According to [49], the gain of the amplifier depends on the output signal level as shown in equation (6.6). In this design, as the load capacitance of the amplifier is relatively large, the gain tends to be sensitive to the output signal level change. Moreover, compared to a folded cascode amplifier topology, a two-stage amplifier topology shows higher non-linearity.

$$A_v = A_{v0}(1 + \alpha_1 V_o + \alpha_2 V_o^2 + \cdots + \alpha_n V_o^n) \qquad (6.6)$$

As Figure 6-45 shows, when a behavior model of amplifier is used, the 3rd-order harmonic distortion has dropped to -120 dB.

6.8.3 Comparison with previously reported works

Table 6-5 shows the performance comparison between this work and the previously reported. As can be seen from the table, this work shows a relatively consistent SNR (1.5 dB of difference between maximum peak SNR and minimum peak SNR over the temperature range). Moreover, this work is measured and proved to operate at up to 300 ^{o}C.

Table 6-5 Performance Comparison between this work and reported works

	Technology	OSR	Maximum Temperature (^{o}C)	Peak SNDR @ 25 ^{o}C	Peak SNDR @ 200 ^{o}C	Peak SNDR @ 250 ^{o}C	Peak SNDR @ 300 ^{o}C	Power mW
[36]	1.5 μm 5V Standard CMOS	256	255	75 dB	88 dB	80 dB	-	-
[37]	0.5 μm 3.3V SOS CMOS	256	200	92 dB	80.6 dB	-	-	34.5
This Work	1 μm 5V SOI CMOS	256	300	65.2dB (SNR 86.8dB)	65 dB (SNR 86.1 dB)	65.9dB (SNR 87.3 dB)	65.8dB (SNR 86.3 dB)	42

Chapter 7 **Conclusion**

7.1 Conclusion

In this work, the fundamental concepts of analog-digital conversion and ΣΔ modulation are presented. Moreover, issues of high temperature circuit design have been studied. Some effective circuit design techniques have been demonstrated to resolve those high temperature issues. In addition, the basic concept of switched capacitor circuits is also presented.

A 3rd-order high temperature low pass ΣΔ modulator is proposed. It is implemented based on switched capacitor topology with fully differential circuitry. The design is based on xFab 1.0 μm SOI process. The ΣΔ modulator has an OSR of 256 and employs single bit quantization. The post layout simulation is done at different temperatures and proven to have a relatively constant performance over the temperature range. The peak SNRs are 106.1dB@0 ^{o}C, 105.3 dB@150 ^{o}C and 102.7 dB@225 ^{o}C, which corresponds to 17.3 bits, 17.2 bits and 16.8 bits respectively. The measurement is done from room temperature to 300 ^{o}C. Constant peak SNR of 87 dB is measured over the temperature range. The power dissipation is 28.5 mW@0 ^{o}C, 35.4 mW@150 ^{o}C and 40 mW@300 ^{o}C.

7.2 Future work

In order to implement a complete ΣΔ ADC, a digital filter and down-sampling block are required to be implemented in order to convert the ΣΔ modulator's output bit stream into parallel digital data.

In this design, the capacitor sizing is based on the thermal noise estimation and all three stage integrators share the same sizing. However, it is shown that the thermal noise injected into the first stage integrator has the most significant effect because of noise suppression of subsequent stages. Therefore, for second and third stage integrators, the capacitor size can be reduced. This will save both the chip area and power. In addition, after the resizing of capacitors, the slew rate requirement for the second and third stage amplifier is relaxed. As a result, the amplifiers used in second and third stage integrators can be improved to have less current in order to save the power.

As analyzed in section 6.8.2, the measured result shows a 3^{rd}-order harmonic distortion which is due to the non-linearity of capacitor and amplifier. Therefore, more work is required in the future to minimize the non-linearity. This can be improved at different stages of design. At modeling stage, the MatLab model can be further revised to suppress the internal signal swing even more for 1^{st} and 2^{nd} stages. At circuit design stage, due to the output swing requirement, the two-stage amplifier architecture is adopted in this design. However, the linearity of such a topology is poor compared to folded cascode architecture. For future improvement, folded cascode architecture can be implemented with optimized swing. It can be used in the third stage integrator which has less output swing requirement. Moreover, for the layout stage, the layout design may be further optimized to improve the matching. Custom optimized MOSFET layout can be applied instead of those imported from library.

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Appendix A MatLab Scripts for Modeling the Modulator

Code to synthesis NTF

```
%Synthesis the NTF
%Define order, OSR, quantization level and out-of-band gain
order = 3;
osr = 256;
opt = 1;
nLev = 2;
obg = 1.5;
%Function to synthesize NTF
H = synthesizeNTF(order,osr,opt,1.5,0);
% Plot the poles and zeros
figure(1); clf
set(1,'name','Poles and Zeros');
plotPZ(H,{'r','g'});
```

Code to simulate the modulator with synthesized NTF

```
%Simulate the modulator
%Define the number of samples, band width
N = 2^15;
fb = ceil(N/(2*osr))+1;
f = floor(2/3*fb);
u = (sin(2*pi*f/N*[0:N-1])).*0.6;
%Function to simulate the NTF
v = simulateDSM(u,H,nLev);
```

Code to plot the PSD

```
%Calculate the FFT and plot the PSD
f_plot = linspace(0,0.5,N/2);
spec = fft(v.*ds_hann(N))/(N*(nLev - 1)/4);
%Function to evaluate the modulator transfer function
Sqq = 4 * (evalTF(H,exp(2i*pi*f_plot))/(nLev - 1)).^2 / 3;
NBW = 1/N;
figure(2); clf
set(2,'name','Output at frequency domain');
plot(f_plot,dbv(spec(1:N/2)));
hold on;
plot(f_plot,dbp(Sqq*NBW), 'g', 'Linewidth', 2 );
grid on;
ylabel('dB');
xlabel('Normalised Frequency');

% Calculate the SNR
snr=calculateSNR(spec(90:fb),f-89);
```

Code to calculate and plot the dynamic range

```
%Calculate and plot the DR
amp = [-150:2:-20 -18:1:-1];
%Function to estimate the SNR
[snr_pred,amp]=predictSNR(H,osr,amp);
[snr,amp]=simulateSNR(H,osr,amp);
figure(3); clf;
set(3,'name','SNR vs input amplitude');
plot(amp,snr_pred,'b',amp,snr,'gs','Linewidth',2);
grid on;
figureMagic([-150 0],10,1,[0 150],10,1);
```

```
xlabel('Input Level, dB');
ylabel('SNR, dB');
title('DR curve');
```

Code to realize the modulator and perform dynamic scaling

```
%Realization
form = 'CIFB';
%Function to realize the NTF
[a,g,b,c] = realizeNTF(H,form)
b = [b(1) 0 b(3) 0]; % Use a single feed-in for the input
c = [c(1) c(2) 1]
ABCD = stuffABCD(a,g,b,c,form);
%plot the STF and NTF
[ntf stf] = calculateTF(ABCD);
f = linspace(0,0.5);
z = exp(2i*pi*f);
magntf = dbv(evalTF(ntf,z));
magstf = dbv(evalTF(stf,z));
figure(4); clf;
set(4,'name','NTF and STF graph');
plot(f,magntf,'b',f,magstf,'r','Linewidth',2);

%Dynamic Scaling
xlim = [0.9 0.3 1.5];
ymax = nLev + 2;
umax = 0.7;
%Functions to perform dynamic range scaling
[ABCD_new umax] = scaleABCD(ABCD,2,f0,xlim, ymax);
[a,g,b,c] = mapABCD(ABCD_new,form);
```

```
ABCD_new2 = stuffABCD(a,g,b,c,form);
H_new = calculateTF(ABCD_new2,1);
```

Code to calculate SNR from SimuLink Model

```
%Find the peak signal bin
BW_begin=floor(3*N/8192);
BW_end= ceil(N/(2*OSR)) +1;

%Function to perform FFT
spec = fft(out_samples.*ds_hann(N))/(N*(nLev - 1)/4);
[sigpw,PeakSigBin] = max(dbv(spec(BW_begin:BW_end)));
PeakSigBin=PeakSigBin+BW_begin-1;
%Function to calculate the SNR
snr=calculateSNR(spec(BW_begin:BW_end),PeakSigBin);
```

Appendix B Ocean Script

```
/* Define Number of Samples*/
pts = 30682

/* Define Sampling period*/
step_size = 70000e-10

/* Initial Time */
start_time = 0.0

/* End Time */
stop_time = start_time + step_size * pts + 4e-3

/*Define Output File*/
file = strcat( "./Sim/" "SDM_3nd_order" "_" pts ".txt" )
p_port = outfile( file "w" )

/*Define Simulator */
simulator( 'spectre )

/*Select Design Netlist*/
design(          "/tmp/SDM_4/spectre/schematic/netlist/netlist")
resultsDir( "/tmp/SDM_4/spectre/schematic" )

/*Select Model Files*/
modelFile(
    '("/lxap12/xfab_XI10/spectre/xi10/bsim3pd.scs" "tm")
    '("/lxap12/xfab_XI10/spectre/xi10/cap.scs" "tm")
    '("/lxap12/xfab_XI10/spectre/xi10/dio.scs" "tm")
    '("/lxap12/xfab_XI10/spectre/xi10/res.scs" "tm")
)

/* Choose Analysis*/
analysis('tran ?stop stop_time ?save "selected" ?errpreset "moderatre" )

/*Define Variables*/
desVar(          "input_amplitude" 500m    )
desVar(          "gain" 1K     )
desVar(          "cap1" 10p  )
desVar(          "cap2" 10p  )
desVar(          "cap3" 10p  )

/*Select Dual Core  for simulation*/
```

```
option(          'nthreads  "2"
         'multithread  "on"
)

/*Select Save Option*/
saveOption( ?simOutputFormat "psf with floats" )
saveOption( 'save "selected" )
save( 'v "/Vout_p" )

/*Set Initial Condition*/
converge( 'ic "/Vin_p" "2.5" )
converge( 'ic "/Vin_n" "2.5" )
converge( 'ic "/net1p" "2.5" )
converge( 'ic "/net1n" "2.5" )
converge( 'ic "/net2p" "2.5" )
converge( 'ic "/net2n" "2.5" )
converge( 'ic "/in1p" "2.5" )
converge( 'ic "/in1n" "2.5" )
converge( 'ic "/out1n" "2.5" )
converge( 'ic "/out1p" "2.5" )
converge( 'ic "/feedback1n" "0" )
converge( 'ic "/feedback1p" "0" )

/*Select Temperature
temp( 150 )

/*Run Simulation*/
run()

/*Select Output*/
selectResult( 'tran )

/*Convert Output into Bitstream
for( i 0 points
time = step_size* i + 39950e-7
vout = value( v( "/Vout_p" ) time )
if(vout > 4 vout_d=1 vout_d=0)
fprintf( p_port "%d\t\n" vout_d )
/*fprintf( p_port "%e\t%d\n" time vout_d )*/

)

/* Close File */
close( p_port )
```