DESIGN OF LOW-POWER SHORT-DISTANCE TRANSCEIVER FOR WIRELESS SENSOR NETWORKS

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SUMMARY

This thesis presents the design of a low-power 2.4-GHz BPSK/OOK transceiver for short-distance wireless sensor network applications. The transceiver is optimized for asymmetrical sensor-gateway communications where different modulation schemes and data-rates are used in the uplink and downlink paths. The transceiver is reconfigurable, and supports both the sensor and gateway modes. Circuit block reuse technique is incorporated in the design to reduce the chip area.

To improve the energy efficiency of the transmitter, a new Class-E power amplifier (PA) is proposed. The PA uses a π-shaped output matching network which provides not only harmonic rejection but also impedance transformation. Comprehensive design equations are derived to aid the PA design, characterization and optimization. The proposed design facilitates fully on-chip solution for low-power Class-E PA. Measurement results indicate that the PA can achieve power efficiency better than 50% while delivering output power around 0 dBm.

Implemented in 0.13 μm CMOS technology, the transceiver occupies a chip area of 3.3 mm^2 including bonding pads. No off-chip matching network or inductor is required. When configured in sensor mode, the transceiver is optimized for low-power consumption and high energy efficiency. The BPSK transmitter consumes only 3.66 mW at 0.2 dBm output power with a locked PLL. The achieved transmitter efficiency is close to 29%. To save power, a digitally calibrated free running oscillator is used to generate the LO signal for OOK demodulation. The OOK receiver consumes only 0.78 mW with sensitivity of -80 dBm at 100 kbps data-rate. In gateway mode, the transceiver is optimized for good performance. The BPSK receiver supports data-rate from up to 8 Mbps, and achieves sensitivity of -84.5 dBm at 5 Mbps data-rate.

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LIST OF ABBREVIATIONS

ABB	Analog Baseband
ADC	Analog to Digital Convertor
ASK	Amplitude Shift Keying
AWGN	Additive White Gaussian Noise
BB	Baseband
BER	Bit Error Rate
BOM	Bill of Materials
BP	Band Pass
DCO	Digitally Controlled Oscillator
DSP	Digital Signal Processing
ED	Envelope Detection
FSK	Frequency Shift Keying
FOM	Figure of Merit
IC	Integrated Circuits
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
LP	Low Pass
LSB	Least Significant Bit
MSB	Most Significant Bit
NF	Noise Figure
OOK	On OFF Keying
Op Amp	Operational Amplifier
PLL	Phase-Locked Loop
PPF	Poly Phase Filter

PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
RFFE	Radio Frequency Front End
RMS	Root Mean Square
SAR	Successive Approximation Register
VGA	Variable Gain Amplifier

CHAPTER 1 INTRODUCTION

1.1. General Background

Transceivers for short-distance communications have recently spurred lots of researches and developments. Various types of transceiver systems and standards have been developed for different applications, including wireless local area network (WLAN), wireless personal area network (WPAN), wireless body area network (WBAN), implantable devices, wireless sensors network (WSN), etc. Because of the different application requirements, transceivers in each category differ greatly from others in terms of data-rate, power level, and complexity. Therefore different system architectures and circuit techniques are employed to satisfy the specific application needs and optimize the performance. This thesis mainly focuses on the physical specifications and implementations of RF transceivers, which are known as the physical layer (PHY) of a network [1-5].

Based on their application fields, transceivers for short-distance communication systems can be classified into several categories as discussed below. One specific area such as WLAN applications provides high-speed wireless data transmission to eliminate the connecting cables and facilitate versatile network deployment. The transceivers for these systems are optimized for high performance, long coverage range, and better quality of service (QoS) [1, 6-11]. As AC powers are available for these systems, power consumptions of this kind of transceivers are relaxed. Portable devices, on the other hand, require the transceivers to have lower power consumptions because of the limited battery capacity. The transceivers are usually targeted at WPAN applications to provide reliable communication ranges up to 10 meters [2-5, 12-14]. There is another kind of application area targeting at communication ranges less than 1 to 2 meters known as WBAN [15-19]. These devices are usually used for medical signal monitoring, consumer electronics, etc. The power consumptions for this kind

of transceivers, especially for human implantation are critical due to the miniature sizes and long battery hour requirements. One of the widely recognized specifications for this application is the medical implant communications services (MICS) which covers frequency band of 402~405 MHz and the maximum transmission power is below -16dBm in order to constrain energy absorptions by human tissues [18, 20-22]. Finally, WSN caters for a wide variety of data rates and communication range, which gives rise to various proprietary architectures and standards [2-5, 7, 11-19, 23-30]. The transceivers targeting for various applications as discussed earlier are summarized in the following figure according to the data-rates and communication ranges.

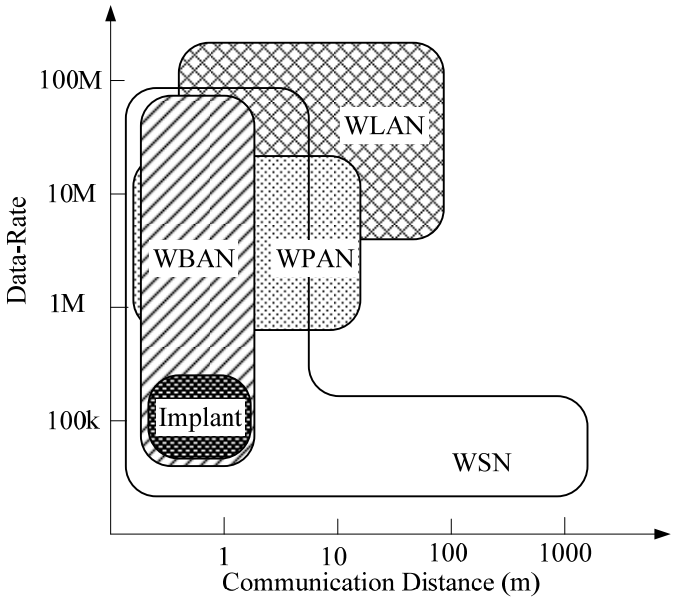


Figure 1.1 Typical data-rates and coverage ranges of different types of transceivers.

Various standards have been established for different networks discussed above. IEEE 802.11a/b/g/n standards are widely adopted in WLAN devices [1, 6-9]. IEEE 802.15.4 standard is adopted for ZigBee devices targeting at WPAN [31, 32]. Bluetooth and its subsequent modifications are also another well adopted standard targeting for low-power application [14, 33-37]. These various standards for short-distance communications are reexamined in next chapter.

Although well defined standards facilitate easy adoption of transceiver developed by different vendors, there exist also other proprietary standards with custom designed transceivers [17, 19, 24-26, 38-43]. These custom designed transceivers allow trade-off among various performance parameters to optimize for energy efficiency.

1.2. Scope of This Work

In this work, we propose a custom designed transceiver specifically optimized for energy efficiency. It targets at WSN application catering for data-rate as high as 8 Mbps and communication range about 10 meters with total power consumption less than 5 mW. An additional feature of the proposed transceiver is its reconfigurability. It can be configured as either sensor or gateway. When configured as sensor, it is optimized for the energy efficiency whereas when configured as gateway, it is optimized for sensitivity.

1.3. Research Contributions

The major contributions of this work include the system and circuit level design methodologies for the low-power transceiver. The first contribution is the proposed architecture which can be configured as sensor or gateway. The second contribution is the proposed Class-E PA with optimized efficiency at low output power. The third contribution is the circuit optimization which employs block reuse and block sharing to minimize the hardware.

The publications achieved to date are listed below.

[1] Jun Tan, Chun-Huat Heng, and Yong Lian, "Design of Efficient Class-E Power Amplifiers for Short-Distance Communications," accepted for *IEEE Transactions on Circuits and Systems I: Regular Papers*.

[2] Jun Tan and Yong Lian, "A 1-Volt, 2.5-mW, 2.4-GHz Frequency Synthesizer in 0.35μm CMOS Technology," in *2009 Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics*, Nov. 2009, Shanghai, China.

[3] Fei Zhang, Jun Tan, and Yong Lian, "An Effective Noise Reduction Technique for Wearable ECG Sensor in Body Area Network," in *2007 IEEE International Conference on Biomedical Circuits and Systems*, Nov. 2007, Montreal, Canada.

[4] Xiaodan Zou, Xiaoyuan Xu, Jun Tan, Libin Yao, and Yong Lian, "A1-V 1.1-μW Sensor Interface IC for Wearable Biomedical Devices," in 2008 IEEE International Symposium on Circuits and Systems (ISCAS), May 2008, Seattle, USA.

1.4. Organization of the Thesis

This thesis is organized as follows. In Chapter 2, various existing standards and transceivers for short-distance communications are examined. In Chapter 3, the proposed system architecture is presented. The new Class-E PA design targeting at low output power is given in Chapter 4. This is then followed by the detailed circuit design of all the key modules of the transceiver in Chapter 5. The measurement results of the transceiver are presented in Chapter 6. Finally the conclusion is given in Chapter 7.

CHAPTER 2 EXISTING TRANSCEIVER DESIGNS FOR SHORT DISTANCE COMMUNICATIONS

2.1. Transceivers Based on Established Standards

Although there are various types of standards established for short-distance communications [1-5, 33-35], not all of them are suitable for low-power applications. For example, IEEE 802.11 standards are optimized for high speed WLAN communications, and the power consumptions of these devices are normally higher than 100 mW [6, 8, 9]. We only focus on systems with low-power consumptions and coverage range up to 10 meters. The transceivers based on Bluetooth, IEEE 802.15.4 (ZigBee), and MICS standards are therefore examined here.

2.1.1. Standards for Low-Power Short-Distance Communications

Before the transceiver designs are presented, the commonly adopted standards for low-power short-distance communications including Bluetooth, IEEE 802.15.4, and MICS devices are briefly introduced first.

Bluetooth is a wireless communications standard firstly created by Ericsson in 1994. There are three power levels defined by the standard, namely Class-1, Class-2, and Class-3. Their maximum power levels are 20, 4 and 0 dBm respectively [44]. Class-1 defines high-power devices for long distance communications above 20 m. Class-2 and Class-3 are suitable for communication ranges below 10 m. In its first version (v1), Bluetooth device uses Gaussian frequency-shift keying (GFSK) modulation and the data-rate is 1 Mbps, which is called basic rate (BR). The modulation index h [45] is between 0.28 to 0.35. The channel spacing is 1 MHz and there are a total of 79 channels from 2402 to 2480 MHz [33]. In its second version

(v2.1), higher data rates are achieved by utilizing π/4-DPSK or 8DPSK modulations, which offers 2 or 3 Mbps respectively. This is called the enhanced data-rate (EDR) [33]. In the third version (v3.0), Bluetooth utilizes IEEE 802.11 standards [1] to increase the data-rate to 24 Mbps, which is defined as high speed (HS) mode [34]. Bluetooth Low-Energy (BLE) is a new feature provided by the fourth version (v4.0) [35]. The modulation scheme is 1 Mbps GFSK which is similar to the v1 standard. However the channel spacing increased to 2 MHz, and there are 40 channels from 2402 to 2482 MHz. The modulation index h is between 0.45 to 0.55, implying larger frequency deviations than Bluetooth v1 standards. When h=0.5, the phase shifting between each symbol is exactly π/2, which is equivalent to GMSK. This allows for simple circuit architecture to save power [14, 31, 32].

IEEE 802.15.4 standard is particularly popular for low data-rate and low-power applications, and its commercial name is ZigBee. Although three frequency bands are included in the standard (868, 915 MHz and the 2.4 GHz ISM bands), most designs adopt the 2.4 GHz band because it is globally available and supports more channels [46]. In the 2.4 GHz band, Offset-QPSK (O-QPSK) is used as the modulation scheme. Half-sine pulse shaping is used to improve the bandwidth efficiency and guarantees a constant output envelope. Spread spectrum techniques are incorporated to enhance the ability of interference rejection. The achieved bit-rate is 250 kbps. There are 16 channels available in the 2.4 GHz band from 2405 to 2480 MHz with 5 MHz channel spacing. The transmitter should be capable of delivering at least -3 dBm output power according to the standard.

MICS standard is for implanted devices. The frequency band is between 401 and 406 MHz. The maximum allowable channel bandwidth is only 300 kHz and the maximum transmit power is -16dBm [18, 20-22]. The relatively low frequency band ensures minimum energy absorptions from body tissues, and the low output power confines the communication range to less than 1~2 m [21, 22].

2.1.2. Transceiver Design Examples: Bluetooth, ZigBee, and MICS

In [37], a Class-2 Bluetooth v2.1 (EDR) radio SoC in 0.13 μm CMOS is presented. Because Bluetooth adopts constant envelope modulation schemes, polar transmitters are therefore used. The GFSK transmission is realized through direct frequency synthesizing from the PLL. As 8-PSK modulation is required in the Bluetooth EDR mode, phase modulation is approximated from frequency modulation, which can be realized by the frequency synthesizer as well. Due to the relatively lower symbol rate, low-IF (IF=500 kHz) architecture is used in this design, which simplify the analog baseband (ABB) filter design and alleviate the DC offset problems in the zero-IF architectures [37, 47]. The transceiver consumes 23 mW in the TX mode (excluding PA) and 36 mW in the RX mode. The efficiency of the PA is quite low (around 5%). The PA consumes about 33 mW DC power while delivering 1.6mW output power, largely degrading the overall efficiencies of the transmitter. Bluetooth 4.0 Low-Energy transceivers are commercially available like Nordic nRF8001. It achieves power consumptions of 24 mW and 28mW in the TX and RX modes respectively [36].

In [14], a multi-mode transmitter implemented in 0.18 μm CMOS is presented which supports both the Bluetooth 1.2 and ZigBee standards. GFSK and MSK modulation schemes are required for these two standards respectively, and they are realized through direct modulation of the ΔΣ PLL. The transmitter consumes about 32 mW when delivering an output power level of 2 mW. Again, the overall efficiency of the transmitter is confined by the PA with power efficiency (PE) less than 25%. In [32], a ZigBee transceiver is implemented in 0.18 μm CMOS. The transmitter is realized through direct modulating the PLL. The received signal is separated into I/Q paths through poly-phase filter (PPF). This simplifies the PLL design by avoiding the quadrature LO generation. Low-IF architecture is adopted. The power consumption is larger than 27 mW in both RX and TX modes. The efficiency of the PA is less

than 30% in this work, which confines the overall TX PE. Similar circuit architectures and power consumptions are reported in ZigBee transceiver in [13, 31, 48, 49].

The MICS standard defines maximum transmitted power of -16 dBm. Due to the small TX output level, the PE of PA or the antenna driver is not important. Major power consumptions are from the LO generation circuitry. In [21], a calibrated DCO is used to generate the RF tone, which avoids the normally used PLL and therefore achieves low power consumption below 400 μW. However, the DCO frequency is sensitive to coefficients including environment temperature and supply voltage. Therefore calibration needs to be carried out frequently, degrading the robustness of the transceiver system. In [18, 22], PLL is incorporated to guarantee frequency stability, but the power consumption is above 10 mW. Due to the limited bandwidth, MICS transceivers have relatively low data-rate. Even with 4-FSK modulation, the maximum data-rate achievable is 800 kbps [22].

In summary, the transceivers compliant to existing standards have limitations in power consumption and data-rate. The power consumptions of BLE and ZigBee transceivers are at the levels of 10 to 20 mW. The ZigBee systems can only achieve 250 kbps data-rate. The maximum data-rate for Bluetooth even with EDR is 3 Mbps. The MICS transceivers only support short-distance communications around 1~2 m and the data-rates are below 1 Mbps.

2.2. Custom Designed Transceivers using proprietary Standards

Various custom designed transceivers with proprietary standards targeting for low-power application are discussed here [17, 19, 24-26, 38-40, 50].

A low-power 2.4-GHz transceiver with 400 mV supply voltage in 0.13 μm CMOS technology is presented in [24]. Constant envelope BFSK modulation is employed which allows the use

of power efficient Class-C PA to maximize the TX efficiency. In addition, direct VCO modulation without any PLL allows further TX power optimization. On the RX side, passive receiver with lower power consumption is employed at the expense of poorer sensitivity. In addition, higher modulation index is used which trades off the spectral efficiency with power efficiency. Nevertheless, the higher NF of passive RX front-end coupled with open-loop VCO, ultimately limits the achievable sensitivity and communication range, which is not reported in the paper.

In [19], a 920 MHz FSK transceiver for body area sensor network is implemented in 0.18 μm CMOS technology. All the inductors in this work are realized off-chip. Due to the low output power (-10 to -6 dBm), the overall power consumption of the TX is constrained by LO generation circuitry instead of PA. Calibrated DCO is therefore used in the TX mode to save power. The RX is based on injection locked oscillator (ILO), which converts the FM signals into AM signals facilitating simple demodulation through envelope detection (ED). The low-power RX (420 μW) is achieved at the price of poor sensitivity (-73 dBm at 5Mbps data). The ILO based RX is also prone to jamming signals.

In [17], a 2.4-GHz ultra low-power OOK transceiver in 90 nm CMOS technology is reported. The OOK modulation scheme simplifies the circuit structure and hence the power consumptions of the whole system. Optional pulse shaping technologies can be incorporated to improve the spectral efficiency. PLL can be disabled and external control voltage is used to calibrate the frequency of the free running VCO. The RX adopts super-regenerative architecture which is inferior in selectivity, sensitivity and robustness as compared with heterodyne structures [31, 37, 51]. Low-power transceiver is achieved at the expense of additional effort of external analog tuning, which is not pragmatic in actual applications. The power consumptions with locked PLL are not reported in this paper. Although the transceiver works in half-duplex, two separate antenna ports with external matching networks are used, which increase the BOM of the whole system.

In [39], a 2.4 GHz OOK transmitter is presented with high data-rate of 136 Mbps. The DC power consumption of the TX is 3 mW when delivering an output power of -14 dBm. Due to the low energy transmitted per bit, the communication range of this work is confined within a short distance of 20 cm.

In [50] a 52 μW wake-up receiver with -72 dBm sensitivity in 90 nm CMOS is presented. The RX operates with a carrier frequency of 2GHz and 100 kbps OOK modulation. A bulk acoustic wave (BAW) resonator with high quality factor (Q) is required as the RF BP filter to select the signal and narrow down the noise bandwidth. The central frequency of the BAW filter is fixed at 2 GHz and cannot be freely tuned. The received signal is down-converted to an uncertain IF which can be anywhere between 1 to 100 MHz. Therefore DCO can be used to generate the LO signals without using PLL. ED is used to demodulate the OOK signals. The sensitivity is largely confined by the large noise bandwidth due to the uncertain IF architecture. The RX is also prone to interferences due to the large uncertain IF frequency.

In [52] a QPSK/O-QPSK 50 Mbps transmitter is designed in 0.18 μm CMOS technology. The TX is based on different phases generated by the ILO VCO. High data-rate of 50 Mbps can be achieved which optimize the FOM of energy per bit. The TX consumes 5.9 mW when delivering -3.3 dBm output power. One problem with this architecture is that the operation frequency cannot be easily adjusted as in PLL based transceivers. The relatively lower energy per bit due to the high data-rate also confines the communication range. Multi-path effect which is prominent for indoor environment complicates the RX design. The high symbol rate (25 M symbols-per-second) in this design is comparable to the coherence bandwidth [45, 53] according to indoor wireless channel measurement [7, 54]. This leads to strong inter-symbol interferences (ISI) which requires equalizers at RX.

2.3. Summary

Transceivers based on Bluetooth (v1, v2, and v4) or ZigBee standards are not suitable for ultra-low-power communication systems, because their power consumptions are larger than 10 mW [13, 14, 31, 32, 36, 37, 48, 49]. Their maximum data-rates are below 3 Mbps according to the standard definitions. The MICS transceivers have short coverage ranges below 2 m, and the maximum data-rate is below 1 Mbps.

Custom designed transceivers with proprietary standards are implemented to support higher data-rates ($\geq$ 5 Mbps) and achieve ultra low power consumptions (< 6mW) [13, 14, 31, 32, 36, 37, 48, 49]. Constant envelope modulation schemes including FSK, OOK, and PSK are adopted, which not only simplify system architecture but also allow the usage of efficient non-linear PA. Free-running VCOs with analog or digital frequency tuning are adopted to reduce power consumptions. Super-regenerative or ILO based RX architectures reduce power consumptions at the price of limited sensitivity and worse anti-jamming performance.

All the existing low-power transceivers introduced above are designed to be symmetrical where the uplink and downlink adopt the same modulation schemes and data-rates. The power consumptions are optimized for both TX and RX. The RX sensitivity is compromised to achieve lower power consumptions. They are thus suitable for peer-to-peer communications in a meshed low-power sensor network.

CHAPTER 3 SYSTEM LEVEL DESIGN OF THE ASYMMETRY TRANSCEIVER FOR LOW-POWER WSN

In this chapter, the proposed system architecture of the transceiver is presented. The design objective and targeted specifications are discussed first, followed by detailed explanation. The performance requirements of the key building blocks are derived based on theoretical analysis and system level simulation.

3.1. Background and Design Objective

In some WSN applications like wireless neural signal recording and biomedical signal monitoring [41-43], the communication is based on star-shaped network topology. The system is composed of a gateway and one or more sensor nodes. The gateway serves as a router which coordinates the communications and collects the data sent from sensor nodes. The major function of the sensor transceiver is to efficiently transmit collected data to the gateway. Obviously this communication scenario is asymmetrical in terms of data-rate and power consumptions. The transceivers in the sensor nodes should be optimized for high energy efficiency and low power consumption. The gateway transceiver has relaxed power consumption requirements because large capacity battery or AC power is available. The data-rate for uplink (sensor to gateway) should be high ($\geq$5 Mbps) in order to accommodate the large data throughput [17, 19, 55]. On the other hand, the downlink (gateway to sensor) does not require high speed transmission because only occasional handshaking or controlling is needed. Low data-rate around 100 kbps is adequate for these purposes [50, 56].

The symmetry transceivers introduced in the previous chapter are not optimized in the star-shaped WSN. These transceivers are targeted for low-power consumptions and only suitable for sensor mode operations. When the transceiver is deployed in gateway, more power can be

consumed to improve the performance, especially the RX sensitivity. But the symmetry transceivers do not provide the option to enhance the performance in gateway. The different data-rate requirements are not considered in these designs either.

The transceiver presented in this dissertation is targeted for sensor-gateway communications in a star-shaped network. The same transceiver chip is designed to be reconfigurable to support both the sensor and gateway operation modes. When used in sensor mode, the transceiver is optimized for low-power consumption and high energy efficiency. When used in gateway mode, the transceiver is optimized for good performance. The targeted coverage range of the transceiver is around 10 meters within an indoor environment, which is similar to the BLE or ZigBee transceivers. Maximum bit-rate is set to be 10 Mbps which is high enough to support most WSN applications [17, 55]. This data-rate is smaller than the coherence bandwidth in the worst cases [7, 54], facilitating simple RX architecture without equalizer. The transceiver is designed to operate in the 2.4 GHz ISM band which offers adequate bandwidth to accommodate multiple channels. The system architecture and specifications are discussed in detail below.

3.2. Overall Architecture and Specifications of the Transceiver

BPSK is chosen to be the modulation scheme for uplink communication because it offers 3 dB better BER as compared to BFSK and OOK systems [45], which helps to enhance the RX sensitivity and coverage range. The problem with the PSK modulation is the relatively complicated receiver architecture required as compared to the FSK or OOK. In the sensor-gateway communication scenario, the BPSK RX is on the gateway which can support much higher power consumptions compared to the sensor nodes. Therefore coherent demodulation scheme is adopted for the BPSK RX to enhance performance. On the other hand, OOK is used in the downlink communication for its simplicity in demodulation. This allows low-

power RX on the sensor nodes. Scalable high bit-rate of 1 to 10 Mbps is used in the uplink, whereas low speed (100 kbps) data transmission is used in the downlink. The operation principle of the dual-mode transceiver is illustrated in the following figure.

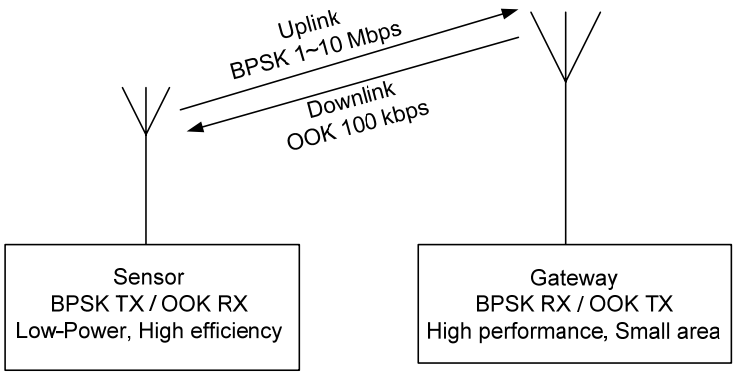


Figure 3.1. The operation principle of the dual-mode transceiver.

It should be noted that when combining the gateway and the sensor transceivers together into a single chip, there are inevitably area penalties. Some circuit blocks required in the gateway mode are not used in the sensor mode, and vice versa. Block reuse must be adopted to reduce the chip area and hence the cost. Finally, the number of the off-chip components should be minimized to allow simple implementation of the transceiver systems and to reduce the BOM costs.

The power related specs of the system are firstly defined. The power consumptions of the transceiver are estimated from the output power of the TX and the performance of the RX. In order to cover an indoor distance of around 10 m, 0 dBm or 1mW output power is a reasonable choice as in [17, 31, 32]. For state-of-the-art designs [17, 19], an overall TX efficiency of 20% to 30% can be achieved. By assuming at least 20% of efficiency, the DC power of the TX in both the sensor mode and gateway mode is therefore defined to be less than 5 mW while delivering 0 dBm output power.

The absolute power consumptions for sensor RX should be below 1 mW which is comparable to the transceivers for low-power sensors as reported in [17, 21, 24, 25]. For gateway mode RX, more power is used to achieve good sensitivity. According to [31, 32, 49], the typical RX power is 10 to 30 mW with sensitivity better than -80 dBm. The DC power of the gateway mode RX is therefore defined to be less than 15 mW with sensitivity better than -80 dBm. To summarize the analysis above, the targeted design specs of the transceiver are provided in the following table. The technology used for this design is 0.13 μm CMOS.

Table 3.1. The targeted design specs of the 2.4GHz transceiver.

TX/RX	parameters	Sensor Mode	Gateway Mode
TX	P_{DC} (mW)	< 5	< 5
	Modulation schemes	BPSK	OOK
	Data rate (Mbps)	1 to 10	0.1
	Output power (mW)	1	1
RX	P_{DC} (mW)	< 1	< 15
	Modulation schemes	OOK	BPSK
	Data rate (Mbps)	0.1	1 to 10
	Sensitivity@10^{-3} BER (dBm)	< -80	< -80

3.3. Detailed Design for the Transceiver

With the specifications provided in the above table, the detailed system design is elaborated here. The TX and RX architectures are presented. The VCO phase noise requirement is derived.

3.3.1. TX Architecture

The TX adopts simple circuitry structure to save power. It is composed of two major building blocks: the LO generation, and the PA. A frequency synthesizer serves as the LO generation circuit, which consists of a differential VCO and a PLL. The PLL locks the VCO at the desired frequency, and the differential VCO generates the 0º and 180º phases which are required by the BPSK modulation. The generated tone from the VCO is then fed into the PA. The OOK TX can be easily realized by turning on or off the PA according to the digital bits. The block diagram of the TX is shown in the following figure. In order to save power, no pulse shaping technique is incorporated, resulting in a constant envelope output signal when the PA is on. This implies highly efficient nonlinear PA can be adopted to improve the energy efficiency of the transmitter.

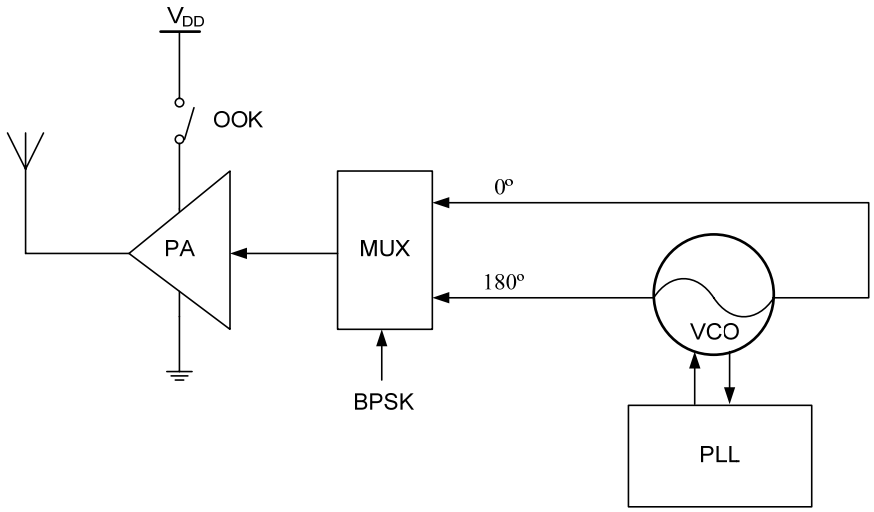


Figure 3.2. The simplified block diagram of the BPSK/OOK transmitter.

To achieve the 5 mW power budget while delivering 0 dBm output power, both the PA and PLL should be optimized for low power consumption. A fully-integrated highly-efficient Class-E PA is used for the TX, which is elaborated in the next chapter. For the PLL design, single-ended TSPC prescalers help to reduce the power consumption [47, 57]. Using 0.13 μm CMOS technology, the estimated power of the PLL excluding VCO is about 1 mW [58]. The VCO should consume less than 1 mW to meet the TX power budget.

3.3.2. RX Architecture

The system level design of the receiver is described here. The OOK RX is targeted for low-power consumption, and the BPSK RX is targeted for good sensitivity. Both the OOK RX and BPSK adopt Low-IF heterodyne architecture.

The reasons to use Low-IF architecture and comparisons with other RX structures are briefly discussed here. Zero-IF architecture suffers from strong flicker noise and DC offset issues, which result in relatively complicated circuit implementations and higher power consumptions [47]. High-IF can achieve better image rejection than Low-IF architecture [47].

However, higher IF causes the ABB to operate at a higher frequency, which results in larger power consumptions. Furthermore it also requires a wider tuning range of the VCO, complicating the circuit design. Low-IF architecture helps to reduce the circuit complexity and power consumption. Therefore it is used in this design for both OOK and BPSK RX. To save power of the ABB amplifiers, the IF should be chosen as low as possible. On the other hand, the IF should be large enough to accommodate the received signal bandwidth. In this design, larger bandwidth is required in the BPSK modulation because of the higher data-rate and rectangular pulse shaping. After down-conversion, the BPSK spectrum is a Sinc waveform centered at IF. At the maximum targeted data-rate of 10 Mbps, 70% of the total energy of the Sinc function is located within the frequency range of (IF-4.1MHz, IF+4.1MHz). The IF should be larger than 4.1 MHz in order to recover 70% of the total energy for correct demodulation, and it is therefore chosen to be 5 MHz in this design to include in some margin.

The low-power OOK RX is based on ED technique similar to the architecture used in [50]. The performance of the RX is directly related the noise bandwidth (BW_{noise}), as interpreted by the following equation [47]:

$$Senstivity(dB) = -174 + 10\log(BW_{noise}) + SNR_{\min} + NF\,, \tag{3.1}$$

where SNR_{min} is the minimum required signal-to-noise ratio at the output of the RX for certain BER (normally 10^{-3} BER is used for sensitivity definition), and NF is the noise figure of the entire RX. To improve sensitivity, the noise bandwidth should be decreased. The uncertain IF architecture in [50] results in a relatively wide noise bandwidth, which degrades the sensitivity of the RX. To improve the performance, accurate LO is needed. The VCO is digitally calibrated to provide the required LO signal. The IF is chosen to be 5 MHz, which is significantly lower than the 100 MHz IF as implemented in [50]. One problem with this architecture is the lack of image rejection. Although SSB mixer can be used for image

suppression [47], it requires quadrature LO signals which complicate the circuitry and hence increase power consumptions. To alleviate this problem, the OOK communications are located only at the two boundaries of the 2.4 GHz ISM band, as shown in the following figure. The LO frequencies are chosen such that the images signals (at 2.390 and 2.490 GHz) fall out of the 2.4 GHz ISM band, therefore minimizing the in-band interferences.

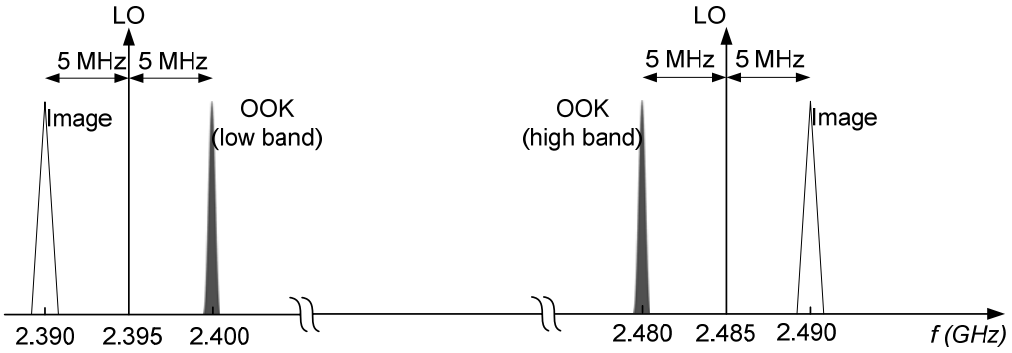


Figure 3.3. Frequency bands of the OOK communication.

The block diagram for the OOK RX is depicted in the following figure. After the ED block, the analog waveform is converted into bit streams by a comparator. Although it is possible to incorporate matched filter to improve the RX performances, it complicates the circuitry and increases power consumptions. Therefore the RX is designed to take only one sample per-bit to simplify the circuitry. In this prototype design the comparator is implemented off-chip, providing the freedom to tune the threshold voltage of the comparator (V_{th}).

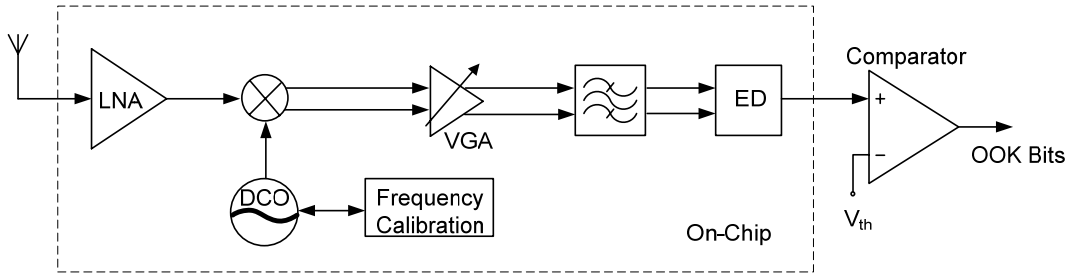


Figure 3.4. The OOK RX block diagram.

To achieve the targeted -80 dBm sensitivity, the required NF of the RX is estimated here by system level simulation. Simplified base-band (BB) model is built to simulate the BER of the OOK RX. The OOK signal is assumed to be down-converted to IF=5 MHz. The BB filter in Fig. 3.4 is assumed to be a bi-quad band pass (BP) filter centered at 5 MHz. Its transfer function is:

$$H_{BP} = \frac{s/p}{(1+s/p)^2}, \tag{3.2}$$

where $p=2\pi\cdot 5M$ rad/s. The ED block is modeled by a rectifier followed by a LP filter with cut-off frequency of 300 kHz. Only one sample is taken for each bit. The simplified RX model is shown in the following figure.

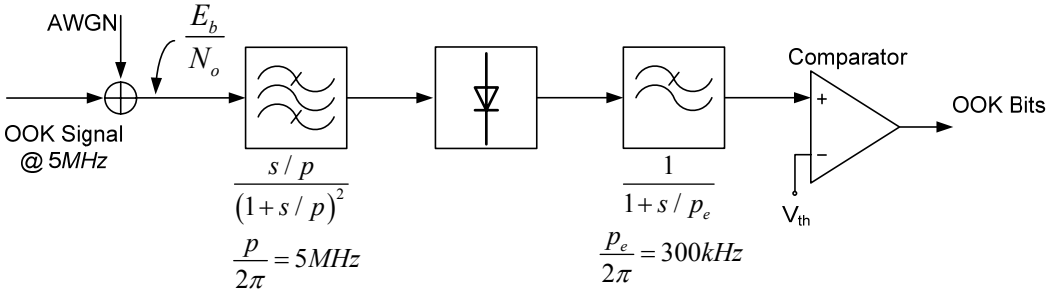


Figure 3.5. The simplified BB model to simulate OOK RX.

The above system is built in Matlab. Simulation indicates that at the signal-to-noise level of E_b/N_o=21 dB, the achieved BER is 10^{-3}. This result is about 11 dB worse than the optimized RX, where E_b/N_o=9.8 dB is needed to achieve BER of 10^{-3} [45]. To achieve -80 dBm sensitivity at 100 kbps data-rate, the required NF of the RX can be computed as follows:

$$NF_{\max} = 174 - 80 - (E_b/N_o) - 10\lg(100k) = 23dB\,. \tag{3.3}$$

This implies that the total NF for the LNA, mixer and the BB amplifiers should be better than 23 dB to achieve sensitivity of -80 dBm.

The BPSK RX adopts low-IF super-heterodyne architecture with IF=5 MHz. Quadrature signals are required for SSB mixer in order to reject the image signals. Although a quadrature VCO can generate required signals, this method requires larger on-chip area and also higher current consumptions. Another commonly used scheme is to run the VCO at twice the operation frequency followed by a frequency dividing-by-2 circuitry [47]. The operation frequency of the VCO and frequency divider is therefore doubled, increasing the power consumption. In order to save on-chip area and power, RC-CR poly-phase filter (PPF) is used in this design, which separates the received signals into I and Q paths. Simple differential VCO running at 2.4 GHz band can be used to generate the LO signal. After down-conversion, the I/Q signals are filtered and amplified by the channel selection filters and VGA. Off-chip ADC and DSP are used for final demodulation. The BPSK RX is illustrated in the following figure. It should be noted that the LNA for BPSK demodulation is different from the one for OOK. The LNA for BPSK is for high performance and hence consumes more power.

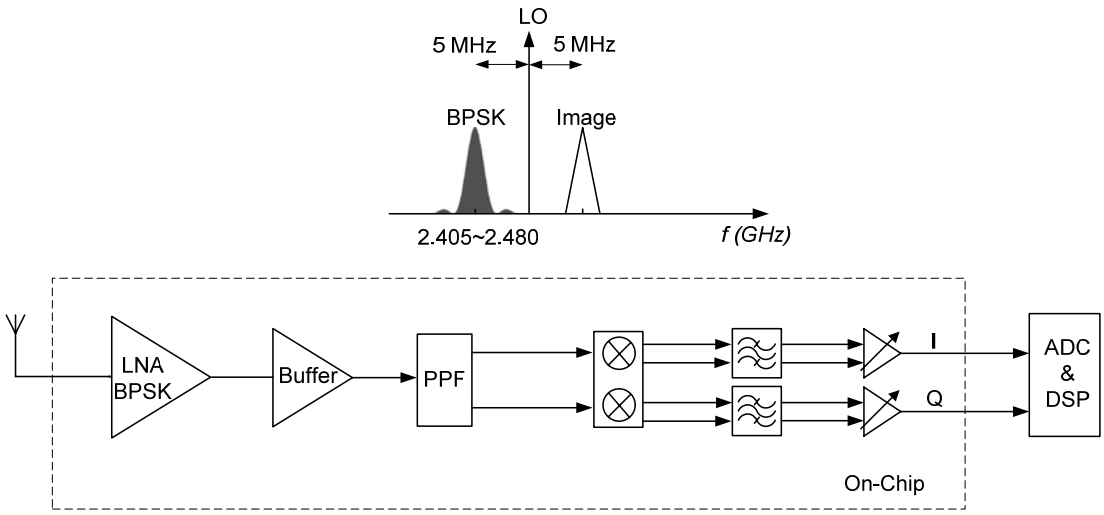


Figure 3.6. System diagram of the BPSK RX.

The required NF of the BPSK RX is estimated from the sensitivity spec. The minimum required E_b/N_o for BPSK is 6.8 dB to achieve BER of 10^{-3} in the ideal case with optimized RX [45]. From Eq. (3.1) it can be seen that the NF should be better than 17 dB to achieve -80 dBm sensitivity at 10 Mbps data-rate with BER=10^{-3}. This result is based on theoretical

analysis. In real circuits, there can be more losses from non-ideal filtering, timing error, etc. Therefore by assuming 3dB implementation loss, the required NF for the BPSK RX is 14 dB.

This NF refers to the RX architecture with quadrature (both I and Q) mixing. The quadrature mixing RX has about 2 to 3 dB better NF performance compared to the single-phase mixing (with only I or Q) RX structure. This is due to the reason of image rejection. The noise at the image band is largely suppressed through quadrature mixing, while the single phase mixing architecture does not reject noise in the image band. For ideal systems with perfect image rejection, the BB noise is 3 dB lower compared with single phase mixing RX, as shown in the following figure. In real circuit implementations, the 3 dB NF difference cannot be achieved due to the limited image rejection ratio, and the uncorrelated noise in the I/Q paths induced after the mixer stages. Normally 2 to 3 dB NF differences can be obtained as reported in [24].

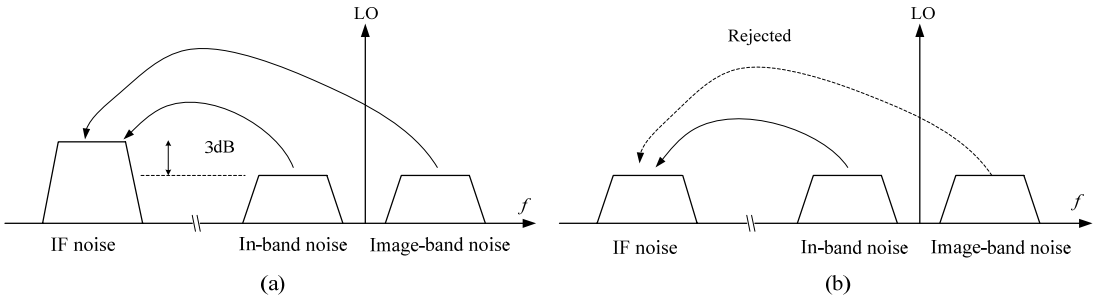


Figure 3.7. Illustration of NF differences between the single-phase and quadrature mixing. (a) Single-phase mixing. (b) Quadrature mixing.

3.3.3. VCO and PLL Specifications

The VCO and PLL specifications are derived from the phase noise requirement of the BPSK communications. The performance of BPSK communication with both AWGN and phase noise is analyzed here.

For transceiver systems with only AWGN impairment, BER is given by [45, 53]:

$$BER_{AWGN}(E_b / N_0) = Q(\sqrt{2E_b / N_o}), \tag{3.4}$$

where the Q function is defined by:

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} \exp(-0.5u^2) du \,. \tag{3.5}$$

The BER with AWGN is completely defined by the SNR (E_b/N_o) at the output of the RX. Based on this result, the BER for a certain phase noise of φ_n in an AWGN channel can be expressed by:

$$BER(\varphi_n) = Q(\sqrt{2E_b / N_o} \cdot \cos(\varphi_n)) \,. \tag{3.6}$$

This is because the distance between the BPSK symbol to the detection boundary is reduced by a ratio of $\cos(\varphi_n)$, as shown in the following figure.

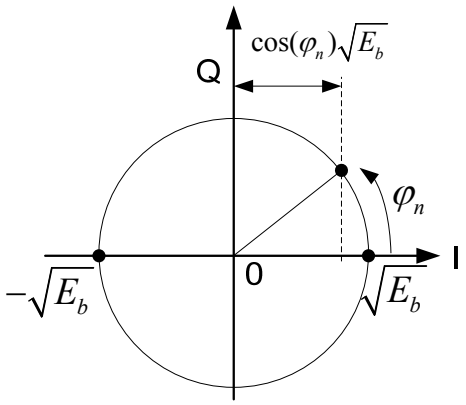


Figure 3.8. BPSK detection with phase noise of φ_n.

Suppose the phase noise φ_n follows a Gaussian distribution with zero mean and standard deviation of $\varphi_{n,rms}$. Then the final BER with both AWGN and phase noise can be approximated by averaging the BER given by Eq. (3.6) at the weight of the probability density function (pdf) of φ_n, as shown in the following equation. This approximation assumes the probability of $\varphi_n > \pi/2$ (larger than 90º) is negligible, therefore it is more valid for relatively small $\varphi_{n,rms}$ ($\leq$30º).

$$BER_{all}(E_b / N_o, \varphi_{n,rms}) = 2\int_0^{\pi/2} \frac{1}{\sqrt{2\pi\varphi^2_{n,rms}}} \exp(-\frac{\varphi^2}{2\varphi^2_{n,rms}}) Q(\sqrt{2E_b / N_o} \cdot \cos(\varphi_n)) d\varphi \quad (3.7)$$

To verify this analytical result, behavior simulations are done to estimate the BER by demodulating 5 million BPSK symbols. The results are plotted in the following figure for $\varphi_{n,rms}$ from 10º to 25º. For the comparison purpose, the BER with only AWGN is also included in the figure.

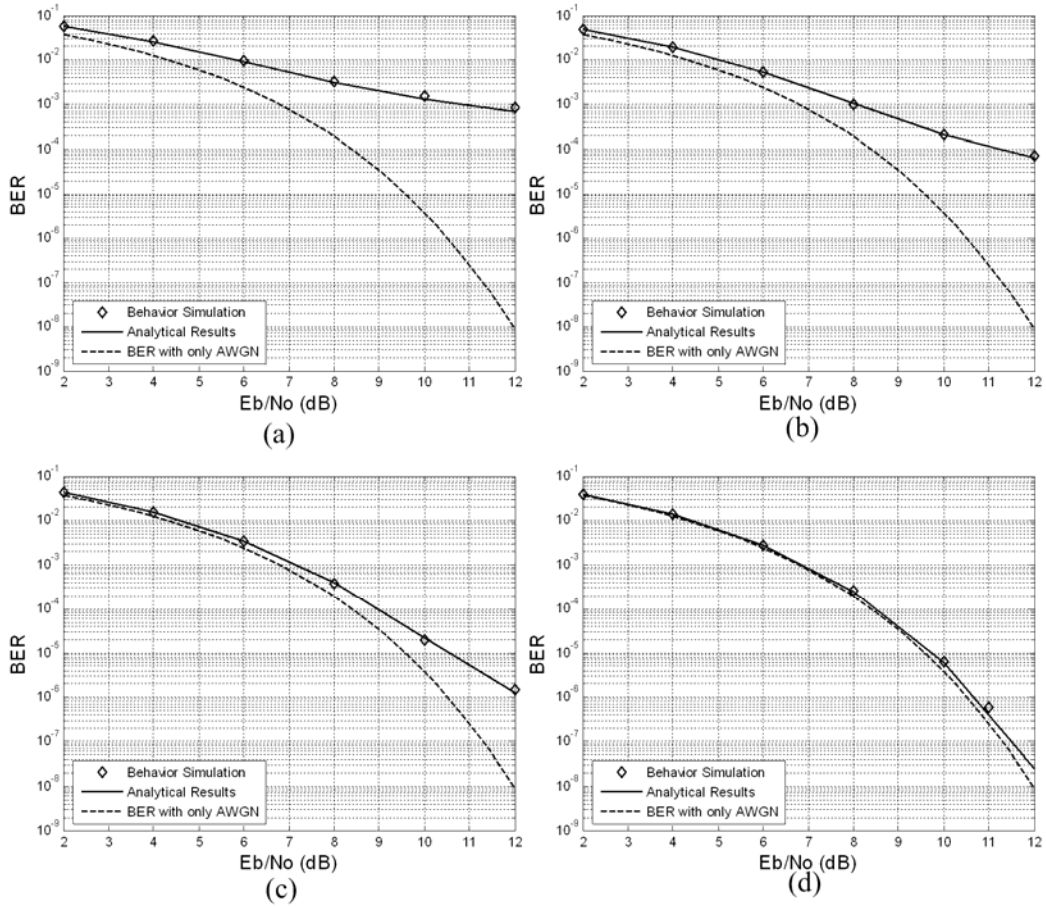


Figure 3.9. The BER of the BPSK communication system with both AWGN and phase noise. (a) $\varphi_{n,rms}$=25º, (b) $\varphi_{n,rms}$ =20º, (c) $\varphi_{n,rms}$=15º, and (d) $\varphi_{n,rms}$ =10º.

It can be seen that the results by Eq. (3.7) match the simulation well. For large phase noise levels ($\varphi_{n,rms} \geq 20º$) as shown in Fig. 3.9(a) and 3.9(b), the BER is deteriorated greatly as compared to the pure AWGN case. At the high SNR level of E_b/N_o=12 dB, the BER drops to

about 10^{-8} in the pure AWGN case, but it is limited to around 10^{-3} and 10^{-4} when $\varphi_{n,rms}$ equals to 25º and 20º respectively. For $\varphi_{n,rms}$=20º, the BER curve is worsened by more than 3.5 dB at the BER level of 10^{-4} compared to the pure AWGN case. For $\varphi_{n,rms}$=15º (in Fig. 3.9(c)), the BER is close to 10^{-6} when E_b/N_o=12 dB, which is about 2 decades better than $\varphi_{n,rms}$=20º. At this phase noise level, the BER curve is only worsened by 0.5 dB at the BER level of 10^{-4}. When $\varphi_{n,rms}$=10º (in Fig. 3.9(d)), the impact of phase noise becomes negligible. Therefore the total phase noise of the transceiver should be below 15º to achieve acceptable BER performance.

Based on the requirements on the RMS values of total phase noise ($\varphi_{n,rms}$), the phase noise spec for VCO is derived below. The typical phase noise of VCO with a locked PLL is shown in the following figure for the illustration purpose.

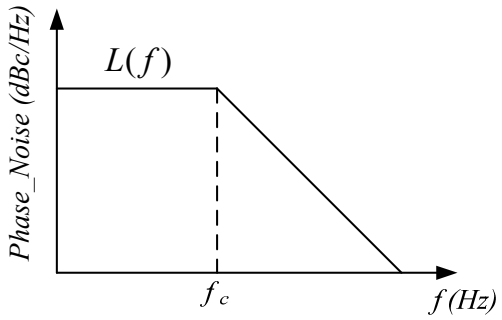


Figure 3.10. The typical phase noise of VCO locked by PLL.

Due to the PLL, the phase noise exhibits low-pass feature. The flat-band phase noise is determined by the performance of charge pump and phase detector [59]. The 3dB transition frequency f_c should be at least 10 times smaller than the reference frequency of the PLL [47]. The total phase noise can be roughly estimated by 1st order low-pass approximation. The RMS value of the single-sided phase noise can be therefore computed by:

$$\varphi_{ns,rms}(dB) = L_{flat}(dB) + 10\lg\left(\frac{\pi}{2} f_c\right), \tag{3.8}$$

where L_{flat} is the flat-band phase noise and $\frac{\pi}{2} f_c$ is the equivalent noise bandwidth of a 1st order low-pass system [60, 61]. The total power of the phase noise is twice of the single sided phase noise because the phase noise resides on both sides of the carrier, and the above equation only considers one side-band. Therefore the total RMS phase noise of the VCO can be computed by:

$$\varphi_{nd,rms}(dB) = \varphi_{ns,rms}(dB) + 3dB\,. \tag{3.9}$$

Suppose the VCO and PLL in the RX and TX have the same noise characteristics. The final phase noise at the output of the RX is determined by summing up the noise powers of two VCOs. Then the total phase noise of the system is:

$$\varphi_{n,rms} = \varphi_{nd,rms} + 3dB = L_{flat}(dB) + 10\lg\left(\frac{\pi}{2} f_c\right) + 6dB\,. \tag{3.10}$$

To simplify the system design and implementation, an Integer-*N* PLL is assumed. To accommodate multiple channels and implement the low-IF RX (with IF=5MHz), the reference frequency of the PLL is chosen to be 5 MHz. In order to increase the reference spur rejection ratio and reduce the in-band noise, the cutoff frequency of the PLL (f_c) should be much smaller than 1/10 of the reference frequency [62]. However, too small a bandwidth also results in slow settling process and difficulty to integrate the loop filter. Therefore f_c is chosen to be between 50 to 100 kHz in this design.

Assume the transition frequency f_c of the PLL is 100 kHz. From Eq. (3.10), it can be derived that the flat-band phase noise should be better than -69.6 dBc/Hz to obtain a total RMS phase noise smaller than 15º. As PLL has almost no suppression on the VCO's phase noise for frequency beyond f_c, the required VCO phase noise can be derived by extrapolating. If the phase noise is -69.6 dBc/Hz at 100 kHz offset, then the VCO's phase noise is -89.6 dBc/Hz at

1 MHz offset by assuming 20 dB per decade slope of the VCO's phase noise, as shown in the following figure.

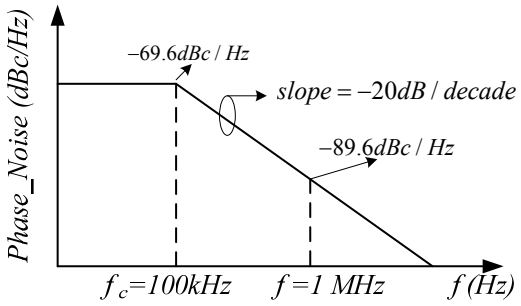


Figure 3.11. Phase noise estimation for VCO.

The above analysis for the phase noise of VCO is based on the simplified model. In real circuit implementation, there is a zero in the PLL's transfer function, which results in some peaking in the transfer function near f_c, and increases the in-band phase noise [62]. The flicker noise is omitted in the above analysis as well. The additional noise from the PLL is also neglected. Therefore the estimated phase noise of -89.6 dBc/Hz at 1 MHz offset is too optimistic. By including an additional margin of 6 dB, the minimum requirement of the VCO's phase noise is about -96dBc/Hz at 1MHz offset to guarantee $\varphi_{n,rms}$ better than 15º.

This phase noise requirement (-96dBc/Hz@1MHz-Offset) can be easily achieved by an LC-VCO with low-power consumption far below 1mW [63]. However, if a ring oscillator is used to achieve this phase noise, the expected power consumption is larger than 2mW [64-66], which is too high for this application. As a result, the VCO architecture is chosen to be LC tank based oscillator, and an integer-*N* PLL with 5MHz reference frequency is used to generate the LO signal for BPSK communication.

3.4. Summary of the System-Level Design for the Transceiver

The simplified system diagram of the transceiver is summarized in the following figure.

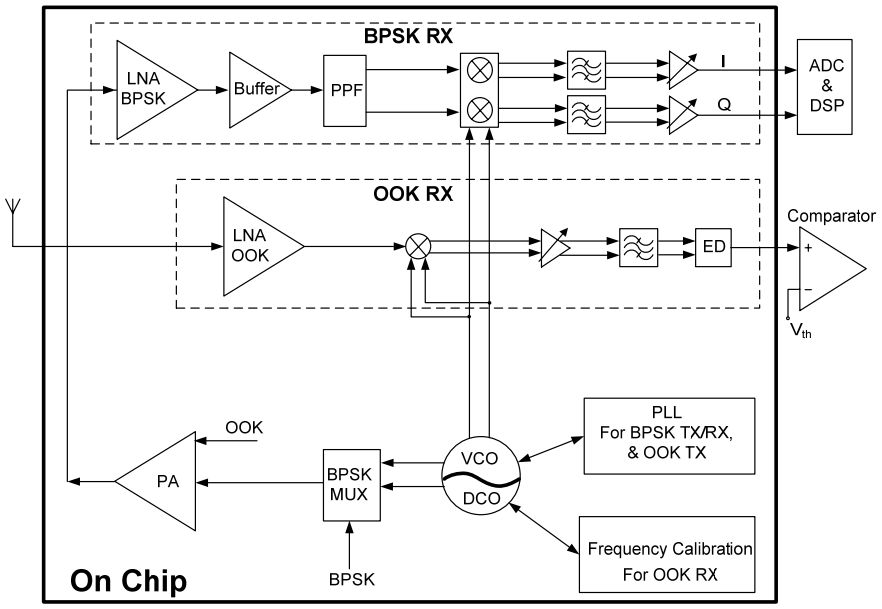


Figure 3.12. The system diagram of the proposed transceiver.

The BPSK modulation is fulfilled by switching the 0º or 180º signal phase to drive the PA. The OOK modulation is realized by turning on or off the PA. To improve the TX performance, the efficiency of the PA should be maximized. Low-IF architecture with IF=5 MHz is adopted for both the BPSK and OOK RX. The BPSK RX is used at gateway and optimized for performance. The OOK RX is deployed at sensor and targeted at low-power consumption. To achieve the specifications defined in Table 3.1, the required NFs for BPSK and OOK RX are 14 dB and 23 dB respectively. The phase noise of the VCO should be at least -96 dBc at 1 MHz offset.

CHAPTER 4 DESIGN OF EFFICIENT CLASS-E PA FOR SHORT-DISTANCE COMMUNICATIONS

4.1. Introduction

LOW power transmitter design requires optimizing the energy efficiency of PA. Class-E PA is a nonlinear switching type power amplifier which can ideally achieve 100% efficiency. This high efficiency has spurred many research interests on the design and analysis of Class-E PAs [10, 11, 44, 67-81]. A typical Class-E PA is shown in Fig. 4.1(a). The transistor serves as an on/off switch. The reactance, Z_x, can be either capacitive or inductive, depending on the desired output power level [67]. An output matching network is usually required to match the antenna's 50Ω resistance to a different value, R_{eq}. As the matching network's quality factor (Q) is normally limited, a serial resonant filter composed of L_{S0} and C_{S0} is incorporated to create a short circuit at the desired switching frequency, and block all the undesired higher harmonic components to reach the output. The Class-E PA requires the periodical steady-state (PSS) waveform of $V_D(t)$ to satisfy the following two criteria [44, 67, 70-72, 75, 78, 79]: at the instance when the switch is turned on, (1) the drain voltage of the switch equals to 0; and (2) its time derivative also equals to 0, as shown in Fig. 4.1(b).

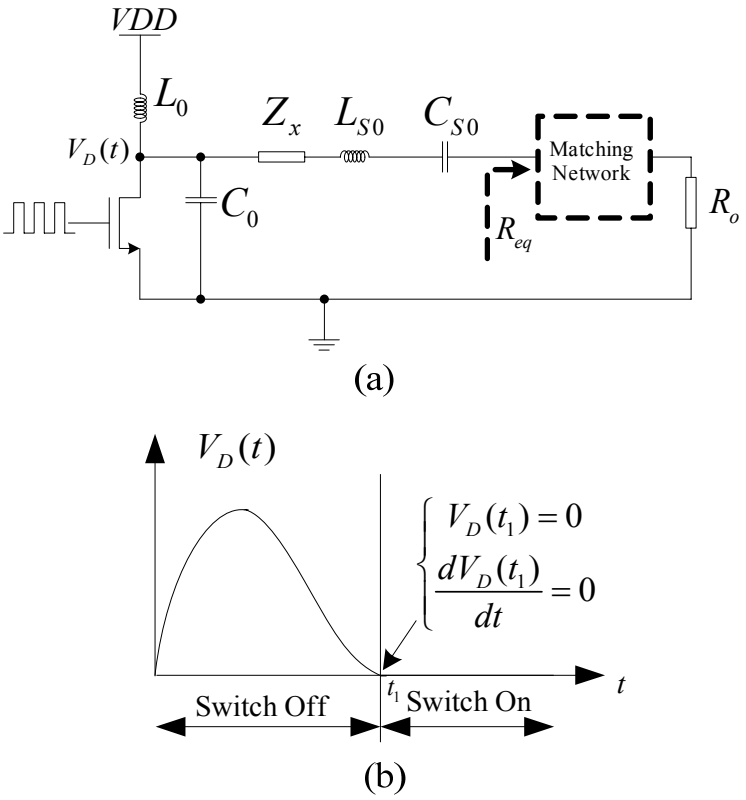


Figure 4.1 (a) Circuit diagram of the conventional Class-E PA. (b) PSS waveform of the drain voltage.

The Class-E PAs can be categorized into two types according to the inductor's function: Class-E PA with RF choke inductor or with DC feed inductor [67]. For the former case, the RF choke inductor maintains the DC biasing while behaves like an open circuit at the desired output frequency. Design equations for Class-E PA with RF choke are discussed comprehensively in [72] and [75]. For the latter case, generalized design methodologies are presented in [67, 70, 76, 78].

The existing works of Class-E PA mostly focus on designs optimized at high output level, ranging from 23 to 33 dBm [68, 69, 73, 74, 80]. If these PAs are used at lower output level, the overall efficiency significantly degrades. In [28] the PA is built based on injection-locked oscillators (ILO) which works in Class-E type. However the power added efficiency (PAE) drops from 44.5% to 30% when the output power level decreases from 11.1dBm to 6dBm.

For most short distance communication, such as Bluetooth and ZigBee, the output power ranges between 0 to 10 dBm [13, 31, 44]. Therefore, it is critical to look at the optimization of Class-E PA with high energy efficiency at low power levels.

To deliver low output power, the equivalent impedance R_{eq} in Fig. 4.1(a) is usually chosen to be comparable to or even higher than 50 Ω [25]. If L_0 functions as RF choke, its impedance should be much higher than R_{eq} to maximize the AC current delivery to the output. This usually results in too high an inductance value to be implemented practically on-chip. For example at 2.4 GHz, L_0 of 33.2nH is needed to have its reactance 10 times larger than R_{eq}= 50Ω. Therefore Class-E PA with L_0 functions as RF choke is not suitable for output power below 10 dBm. In addition, the series resonant network (L_{S0} and C_{S0}) needed for larger harmonic rejection also imposes inductance constraint, which makes the on-chip integration difficult. It should be pointed out that due to low R_{eq} for high power applications, the inductance constraint discussed above is much relaxed.

To circumvent this inductance constraint for low power applications, a new Class-E PA architecture facilitating fully integrated solution is presented in this chapter.

4.2. The Proposed Class-E PA

The inductance constraint imposed by L_0 can be relaxed if it functions as DC feed [67] instead of RF choke. To obviate the need for large inductance in series resonant network (L_{S0}, C_{S0}), different topology has to be employed. Fig. 4.2 illustrates our proposed idea which considers impedance network right after the impedance Z_x. Conventionally, only series resonant network is used to improve the harmonic rejection. For Fig. 4.2(a) with large R_{eq} (required for low output power), the rejection ratio is directly related to $R_{eq}/(R_{eq}+X_s(n\omega_o))$, where ω_o is the desired output frequency, and n is the n^{th} harmonic generated by Class-E PA ($n\geq 2$). To

improve the rejection, we have no choice but to increase X_s and thus L_{S0}. For Fig. 4.2(b), a parallel network is added. Now the rejection ratio would depend on the ratio of $X_p(n\omega_o)/(X_p(n\omega_o)+X_s(n\omega_o)+R_{eq})$ to $X_p(\omega_o)/(X_p(\omega_o)+X_s(\omega_o)+R_{eq})$ for $n\geq 2$. Better harmonic rejection would require $X_p(\omega_o)>X_p(n\omega_o)$ and $X_s(\omega_o)<X_s(n\omega_o)$, which implies a capacitive network and inductive networks respectively. Due to presence of X_p, it relaxes the requirement on X_s to achieve same harmonic rejection. This will reduce the L_{S0} and allow better integration.

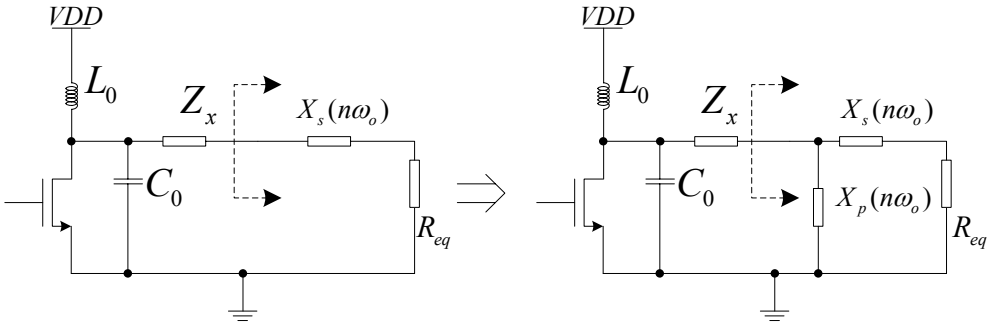


Figure 4.2. Circuit Model of the Class-E PA. (a) Conventional Structure. (b) Proposed Structure.

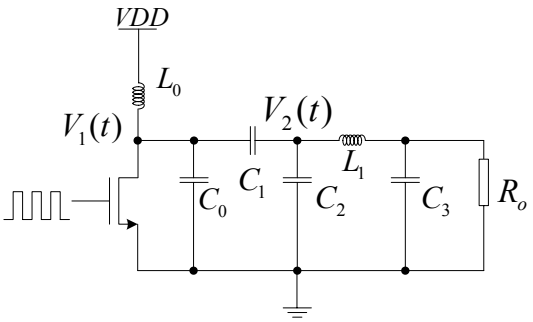


Figure 4.3. The circuitry of the proposed Class-E PA.

The proposed new circuitry of the Class-E PA is shown in Fig. 4.3. The inductor L_0 is chosen as DC feed. The capacitor C_2 functions as X_p which provides alternative current path for higher harmonics. The inductor L_1 and the capacitor C_3 form an impedance matching network which transforms the antenna resistance (R_0) to R_{eq} at the desired output frequency (ω_o). The inductor L_1 also functions as X_s which helps reducing higher harmonics current component. Unlike conventional structure, the harmonic rejection is now provided by both L_1 and C_2. This

allows smaller L_1 to be chosen for on-chip integration. It should be pointed out that the proposed architecture has merged the harmonic rejection and impedance matching into a π-network consisting of L_1, C_2 and C_3. For the proposed architecture, the drain parasitic capacitance of switching transistor can be incorporated into C_0, whereas the pad parasitic can be merged with C_3. Therefore, the circuit shown in Fig. 4.3 can be a compact representation of the actual implemented PA with all parasitic taken into considerations. As the proposed architecture is different from the existing class-E PA, a new set of design formulae needs to be derived for optimization purpose.

As there are now a total of six reactive elements (L_0, L_1, and C_0 to C_3), it offers more design freedoms in PA optimization as compared with the original architecture. The detailed component selection will be discussed next.

4.3. Analytical Design Equations for the Proposed Class-E PA.

The Class-E PA conditions are defined solely in the time domain. The PSS solutions are needed to design the PA. The following assumptions are made before we derive the design equations:

1) The resistor R_o is the only component which dissipates power. The transistor serves as an ideal switch with an 'on' resistance of 0 and 'off' resistance of infinity.
2) The current waveform of the inductor L_1 is sinusoidal (high-Q assumption).

The second assumption implies that the output network has a high harmonic rejection and thus high quality factor. This is achieved through L_1 and C_2 in our architecture. Similar simplifications have been made in [67], [70] and [75] as well to obtain explicit solutions.

With the above approximations, a simplified circuit model is shown in Fig. 4.4. The current of

the inductor L_0 is denoted by $i_L(t)$. The ideal switch is driven by an input square wave, V_{in}, with a period of T. The switch is turned off from 0 to t_1, and turned on from t_1 to T. The ratio of (T-t_1) to T is defined as the on time duty cycle (D). Let ω_o denote the angular frequency of the driving voltage of the switch, which satisfies: $\omega_o=2\pi/T$. The output current $i_{out}(t)$ represents the current of the inductor L_1 in Fig. 4.3, and is given as:

$$I_{out}(t) = I_a \cos(\omega_o t + \varphi)\,, \tag{4.1}$$

where I_a is the amplitude of the current and φ is the phase difference between the output current and the input voltage.

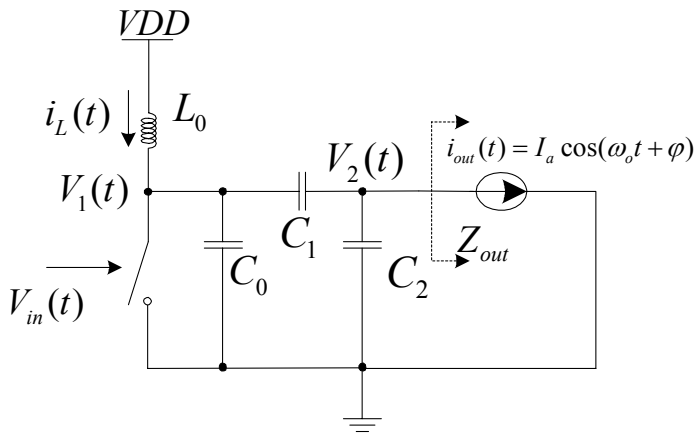


Figure 4.4. The simplified circuit model.

Suppose the supply voltage V_{DD}, the angular frequency of the driving signal ω_o, and the on time duty cycle D are known. There are totally six unknown variables in the circuitry in Fig. 4.4, namely L_0, C_0, C_1, C_2, I_a, and φ. To determine these variables, six independent equations are required. The Class-E conditions define two equations as below [44, 67, 70-73, 77-79]:

$$V_1(t_1) = 0\,, \tag{4.2}$$

$$\frac{dV_1(t_1)}{dt} = 0\,, \tag{4.3}$$

where $V_1(t)$ is the PSS waveform of the switch voltage with a period of T. Therefore four additional equations are required to solve all the six unknowns. We define four design

variables C_{eq}, α, β and q, which are depicted in Eq. (4.4) to (4.7):

$$C_{eq} = C_0 + C_1 // C_2 = C_0 + \frac{C_1 C_2}{C_1 + C_2} \ , \tag{4.4}$$

$$\alpha = C_1 /(C_1 + C_2) \ , \tag{4.5}$$

$$\beta = C_0 / C_{eq} \ , \tag{4.6}$$

$$q = \frac{1}{\omega_o \sqrt{L_0 C_{eq}}} \ , \tag{4.7}$$

where C_{eq} is the total equivalent capacitance at the switch node, α is related to the capacitance ratio of C_1 and C_2, β is the ratio of the parallel capacitance C_0 to C_{eq}, and q is the normalized frequency defined by C_{eq} and L_0. These four new variables would be the key design variables. Once determined, the actual component values of C_0–C_2 and L_0 can be determined subsequently. The remaining two unknown variables of I_a, and φ are derived next.

When the switch is off ($0 \le t \le t_1$), the state equations of the system are given by the ordinary differential equations (ODE) of Eq. (4.8), (4.9) and (4.10).

$$V_{DD} - V_1(t) = L_0 \frac{di_L(t)}{dt} \ , \tag{4.8}$$

$$i_L(t) = C_0 \frac{dV_1(t)}{dt} + C_1 \left(\frac{dV_1(t)}{dt} - \frac{dV_2(t)}{dt} \right) , \tag{4.9}$$

$$C_1 \left(\frac{dV_1(t)}{dt} - \frac{dV_2(t)}{dt} \right) = C_2 \frac{dV_2(t)}{dt} + I_a \cos(\omega_o t + \varphi) \cdot \tag{4.10}$$

When the switch is on ($t_1 \le t \le T$), the voltage V_1 is pulled to zero. The state equations become:

$$V_{DD} = L_0 \frac{di_L(t)}{dt} \ , \tag{4.11}$$

$$\left(C_1 + C_2 \right) \frac{dV_2(t)}{dt} = -I_a \cos(\omega_o t + \varphi) \ . \tag{4.12}$$

The general solutions of the ODE set of Eq. (4.8), (4.9) and (4.10) are given below when $0 \le t \le t_1$:

$$V_1(t) = A_1 V_{DD}\cos(\omega_1 t) + A_2 V_{DD}\sin(\omega_1 t) + \kappa V_{DD}\frac{1}{q^2-1}\sin(\omega_o t+\varphi) + V_{DD}, \tag{4.13}$$

$$V_2(t) = \frac{C_1}{C_1+C_2}V_1(t) - \frac{I_a}{(C_1+C_2)\omega_o}\sin(\omega_o t+\varphi) + A_3 V_{DD}, \tag{4.14}$$

$$i_L(t) = C_{eq} q\omega_o\left[A_2 V_{DD}\cos(q\omega_o t) - A_1 V_{DD}\sin(q\omega_o t)\right] + \kappa V_{DD} C_{eq}\omega_0 \frac{q^2}{q^2-1}\cos(\omega_o t+\varphi). \tag{4.15}$$

The variable κ in Eq. (4.13) and (4.15) is defined as:

$$\kappa = \frac{\alpha I_a}{C_{eq}\omega_0 V_{DD}}. \tag{4.16}$$

When $t_1 \le t \le T$, the waveforms of V_2 and i_L can be obtained from the ODE set of Eq. (4.11) and (4.12). The initial conditions of $V_2(t_1)$ and $i_L(t_1)$ are computed from Eq. (4.14) and (4.15). The solutions are given by:

$$V_2(t) = -\frac{I_a}{(C_1+C_2)\omega_o}\sin(\omega_o t+\varphi) + A_3 V_{DD}, \tag{4.17}$$

$$i_L(t) = \frac{V_{DD}}{L_0}t + i_L(t_1). \tag{4.18}$$

The three variables of A_1, A_2 and κ are determined by the boundary conditions of the voltage waveform of V_1 during $0 \le t \le t_1$. The initial condition of V_1 is given by: $V_1(t)=0$. The voltage V_1 and its derivative at $t=t_1$ are defined by the Class-E conditions in Eq. (4.2) and (4.3). As a result, by substituting $V_1(t)$ depicted by Eq. (4.13) into these three equations, A_1, A_2 and κ may be obtained by solving the linear algebraic equations (AE):

$$A_1 = \frac{q\left(\sin(a_2)-\sin(a_1)+\sin(a_3)-\sin(a_4)\right)+\sin(a_1)+\sin(a_2)}{q\sin(a_1)-q\sin(a_2)-2q\sin(\varphi)-\sin(a_2)-\sin(a_1)}, \tag{4.19}$$

$$A_2 = \frac{q\left(\cos(a_1)-\cos(a_2)+\cos(a_4)-\cos(a_3)\right)-\cos(a_1)-\cos(a_2)+2\cos(a_5)}{q\sin(a_1)-q\sin(a_2)-2q\sin(\varphi)-\sin(a_2)-\sin(a_1)}, \tag{4.20}$$

$$\kappa = \frac{-q\left(\cos(2q\pi(1-D))q^2-\cos(2q\pi(1-D))-q^2+1\right)}{k_1+k_2+k_3+k_4+k_5}. \tag{4.21}$$

The detailed expressions of the sub-functions of $a_1,\ldots,a_5$ and $k_1,\ldots,k_5$ are provided in the Appendix at the end of this thesis.

The PSS conditions require all the waveforms to be periodical with a cycle of T. This implies that V_1, V_2 and i_L satisfy the following three conditions: $V_1(0)=V_1(T)$, $V_2(0)=V_2(T)$, and $i_L(0)=i_L(T)$. From Eq. (4.13), (4.14), (4.17) and (4.19)–(4.21), it can be seen that the first two conditions are already satisfied for arbitrary φ. By substituting $i_L(0)$ given by Eq. (4.15) and $i_L(T)$ given by Eq. (4.18) into the third condition, the required phase difference φ can be derived by solving the AE. The result is given by Eq. (4.22). The detailed expressions of the sub-function $g_{n1},\ldots,g_{n4}$ and $g_{d1},\ldots,g_{d5}$ are given in the Appendix.

$$\varphi = \pi D + \pi - \tan^{-1}\left(\frac{g_{n1}+g_{n2}+g_{n3}+g_{n4}}{g_{d1}+g_{d2}+g_{d3}+g_{d4}+g_{d5}}\right). \tag{4.22}$$

The constant A_3 is related to the DC component of V_2, and it is relatively trivial in characterizing the PA. Its detailed expression is omitted here.

From the above analysis it can be seen that by choosing C_{eq}, q, α, and β as free design variables, all the six unknowns in Fig. 4.4, namely L_0, C_0, C_1, C_2, I_a, and φ can be solved explicitly from Eq. (4.4)–(4.7), (4.16), (4.21), and (4.22). The PSS waveforms of the system are also determined by Eq.(4.13)–(4.22).

The output network composed of L_1 and C_3 are determined from the output current $i_{out}(t)$ and the voltage waveform of $V_2(t)$. The current through the inductor L_1 (in Fig. 4.3) should be

equal to $i_{out}(t)$ (in Fig. 4.4). As $V_2(t)$ is a periodical function, it can be expanded into Fourier series:

$$V_2(t) = V_{2\_0} + V_{2\_1}\cos(\omega_o t + \phi_1) + V_{2\_2}\cos(2\omega_o t + \phi_2) + V_{2\_3}\cos(3\omega_o t + \phi_3) + \ldots, \tag{4.23}$$

where V_{2_i} and ϕ_i are the voltage amplitude and phase offset at the i^{th} harmonic frequency respectively. At the fundamental frequency ω_o, the equivalent output impedance seen from the left of the output current source in Fig. 4.4 is:

$$Z_{out} = \frac{V_{2\_1}}{I_a}\exp\left[(\phi_1 - \varphi)j\right] = Z_{out\_real} + j \cdot Z_{out\_imag}, \tag{4.24}$$

where Z_{out_real} and Z_{out_imag} are the real and imaginary parts of the impedance Z_{out}. The expressions to compute V_{2_1} and ϕ_1 are derived from PSS waveform of V_2. The detailed formulae are given by Eq. (4.36)–(4.39) in the Appendix.

From the circuit in Fig. 4.3, it can be seen that the equivalent output impedance Z_{out} seen from the left of the inductor L_1 at the fundamental frequency can be calculated by:

$$Z_{out} = \left(R_o // \frac{1}{C_3\omega_o j}\right) + L_1\omega_o j = \frac{R_o}{1+(R_o C_3\omega_o)^2} + \left(L_1\omega_o - \frac{R_o^2 C_3\omega_o}{1+(R_o C_3\omega_o)^2}\right)j. \tag{4.25}$$

By equating Eq. (4.24) and (4.25), the component values of L_1 and C_3 can be obtained from:

$$L_1\omega_o = Z_{out\_imag} + \frac{R_o^2 C_3\omega_o}{1+(R_o C_3\omega_o)^2}, \tag{4.26}$$

$$C_3\omega_o = \sqrt{\left(\frac{1}{Z_{out\_real}R_o} - \frac{1}{R_o^2}\right)}, \tag{4.27}$$

where Z_{out_real} and Z_{out_imag} can be calculated from Eq. (4.24) and (4.36) –(4.39).

To summarize the above analysis, the component values of the proposed PA are listed in Table 4.1. Note the normalized capacitance and inductance are defined as:

$$L_{xn} = L_x \cdot \omega_o , \tag{4.28}$$

$$C_{xn} = C_x \cdot \omega_o . \tag{4.29}$$

The output power of the PA can be computed by averaging the current through L_0 as follows:

$$P_{out} = V_{DD} \cdot \frac{1}{T}\int_0^T i_{L0}(t)dt = {V_{DD}}^2 C_{eqn} h(q, D) . \tag{4.30}$$

The function h is described by Eq. (4.40) in the Appendix.

Table 4.1. The Normalized Component Values of the Proposed PA

L_{0n}	C_{0n}	C_{1n}	C_{2n}	L_{1n}	C_{3n}
$\frac{1}{q^2 C_{eqn}}$	βC_{eqn}	$\frac{(1-\beta)C_{eqn}}{1-\alpha}$	$\frac{(1-\beta)C_{eqn}}{\alpha}$	(4.26)	(4.27)

4.4. Analysis and Design of Fully Integrated Class-E PA.

In this section, the design perspectives of the proposed Class-E PA are discussed. Relationships between the design variables and the PA's performance are briefly studied. Simplified design equations are provided to approximate the PA's output power and the values of L_1 and C_3. We also present the methodologies on the selection of the component values of the proposed PA to meet the integration criteria.

The PA's output power is given by Eq. (4.30). It scales linearly with C_{eqn} and the square of the supply voltage. The output power is also related to the design parameters of q and D. By setting the normalized equivalent capacitance C_{eqn} to be 10 mF, the relationships between the output power and the normalized frequency q under different duty cycle D are shown in Fig.

4.5. The output power decreases with larger q and smaller D. As illustrated, the desired output power level has strong dependencies on D. For the targeted moderate and low output power (≤10 dBm), D of 0.4 or 0.5 can be chosen.

The current of the DC feed inductor L_0 is also plotted in Fig. 4.6. When q approaches 0, L_0 behaves like RF choke and exhibits almost constant DC current. As q increases, L_0 functions as DC feed inductor and it exhibits higher AC current swing. The current through the switch when it is turned on can be computed by summing the currents through L_0 and C_1. Its waveform is plotted in Fig. 4.7. The duty cycle is chosen to be 0.5 and C_{eqn} equals to 10 mF. The current through the switch increases gradually from 0, which verifies the soft switching feature of the Class-E PA [44]. The switch transistor should be large enough such that the voltage drop across it is close to zero.

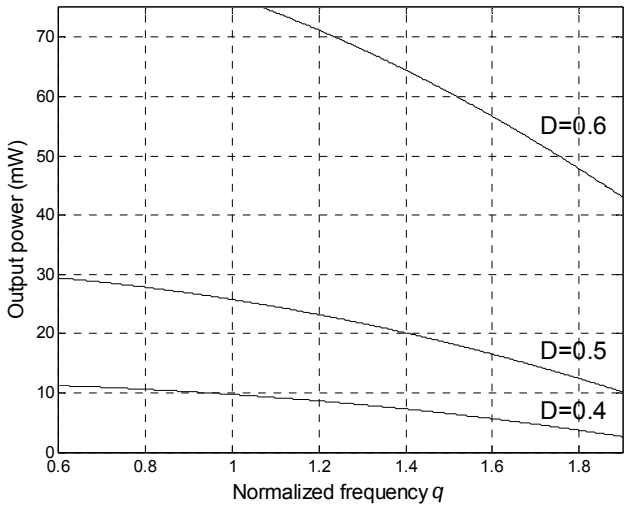


Figure 4.5. The output power of the PA vs. the normalized frequency q. The supply voltage is set to 1-Volt. The switch duty cycle changes from 0.4 to 0.6. C_{eqn}=10 mF.

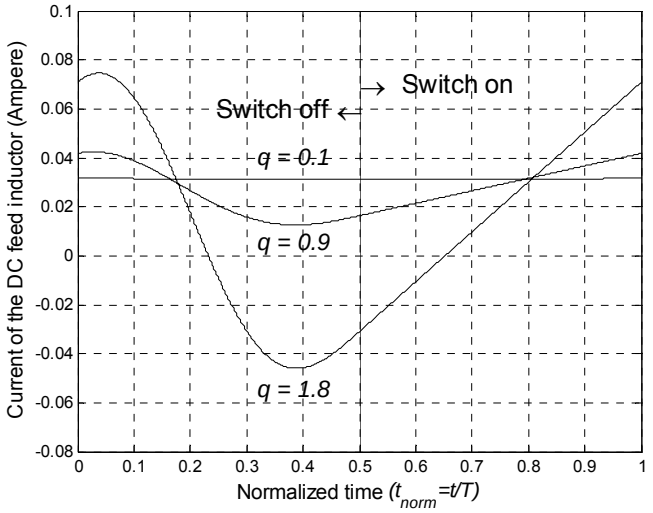


Figure 4.6. The current waveform of the inductor L0. D=0.5. C_{eqn}=10 mF.

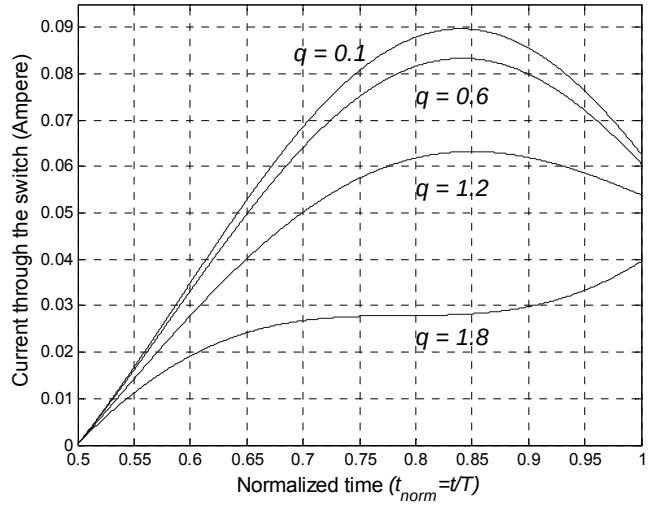


Figure 4.7. The current of the switch when it is turned on. D=0.5. C_{eq}=10 mF.

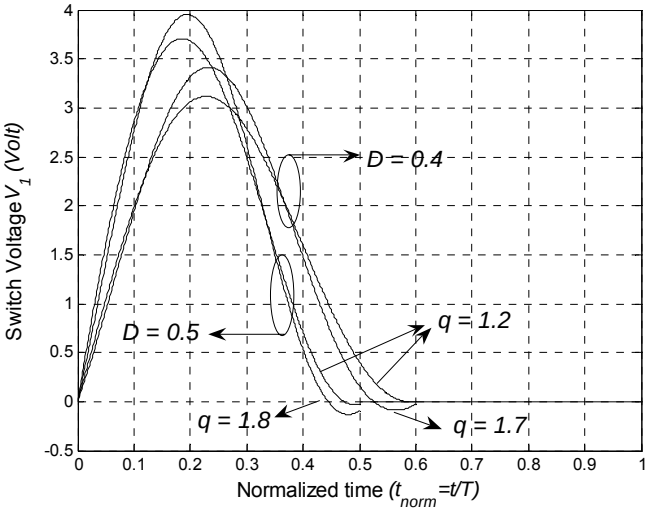


Figure 4.8. The PSS waveform of voltage $V_1(t)$ when the switch is off. α=β=0.3.

The PSS waveform of the switch voltage $V_1(t)$ is plotted in Fig. 4.8. The supply voltage is set to 1-volt. α and β are both chosen to be 0.3. The waveform deviates gradually from the Class-E requirements with larger q. This is because the error caused by the high-Q assumption is larger when q increases. A smaller α value implies larger value of C_2, which helps to divert the higher harmonic components to ground. Hence the high-Q approximation is more valid for smaller α. If α is chosen to be 0.3, simulation results indicate that it is proper to choose q<1.7 for D=0.4 and q<1.8 for D=0.5.

Although all the explicit equations have been derived in the previous section, the equations for computing the PA's output power and the component values of L_1 and C_3 are quite complicated. Simplified design equations are provided here to ease computation. Cubical polynomial approximations are used to compute these variables. Least squares fitting techniques are used to derive all the polynomial coefficients. The errors caused by these approximations are below 3%. The PA's output power can be estimated by the following equation for $q \in (0,1.7)$.

$$P_{out} \approx \left(p_{O3} q^3 + p_{O2} q^2 + p_{O1} q + p_{O0} \right) C_{eqn} {V_{DD}}^2 . \tag{4.31}$$

The polynomial coefficients of p_{Oi} (i=0,…,3) for different duty cycle D are summarized in Table 4.2.

Table 4.2. The Polynomial Fitting Coefficients to Estimate Output Power

D	p_{O3}	p_{O2}	p_{O1}	p_{O0}
0.4	-3.80E-2	-0.179	-2.04E-2	1.21
0.5	-3.03E-2	-0.526	-1.15E-2	3.14

The inductance value L_{1n} depicted by Eq. (4.26) is related to C_{eqn}, α, β, D, and q. To simplify analysis, α and β are both fixed to 0.3. The antenna resistance is assumed to be 50 Ω. The normalized inductance L_{1n} is plotted in Fig. 4.9. We approximate its value by a cubical

polynomial of q as shown in Eq. (4.32).

$$L_{1n} \approx p_{L3}q^3 + p_{L2}q^2 + p_{L1}q + p_{L0}\,. \tag{4.32}$$

The fitting parameters of p_{Li} when C_{eqn} is equal to 10, 15 and 20 mF are listed in Tables 4.3 and 4.4.

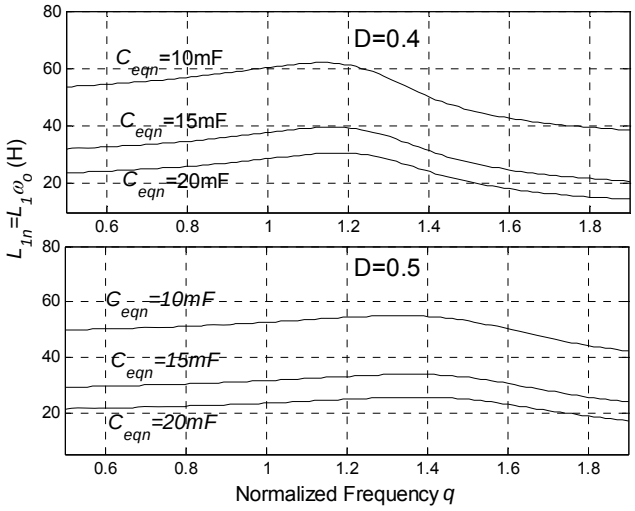


Figure 4.9. The normalized inductance value L_{1n} vs. q for different C_{eqn} values. α=β=0.3. D=0.4 and 0.5.

Table 4.3. The Fitting Parameters to Compute L_{1n} (D=0.4, α=β=0.3)

C_{eqn}	10 mF		15 mF		20 mF	
q	0 ~1.2	1.2~1.7	0~1.2	1.2~1.7	0~1.2	1.2~1.7
p_{L3}	-6.8507	116.64	-2.1298	-143.49	-0.2186	146.22
p_{L2}	21.060	-448.46	12.151	-589.33	8.1241	-612.92
p_{L1}	-7.1363	516.17	-3.8959	762.01	-2.4570	818.03
p_{L0}	44.650	-121.28	31.291	-273.73	24.433	-319.21

Table 4.4. The Fitting Parameters to Compute L_{1n} (D=0.5, α=β=0.3)

C_{eqn}	10 mF		15 mF		20 mF	
q	0 ~1.2	1.2~1.8	0~1.2	1.2~1.8	0~1.2	1.2~1.8
p_{L3}	1.0341	74.321	1.2577	47.824	1.2863	34.645
p_{L2}	2.5564	-378.74	1.5158	-254.60	1.0340	-191.47
p_{L1}	-0.1029	611.43	0.1204	424.48	0.2028	327.52
p_{L0}	40.861	271.09	28.605	-192.72	22.314	-151.27

The capacitance C_{3n} depicted by Eq. (4.27) is related to C_{eqn}, α, D, and q. Its relationships with C_{eqn} and q are plotted in Fig. 4.10. The variable α is set to be 0.3. A cubical polynomial approximation is provided to estimate this capacitance, i.e.:

$$C_{3n} \approx p_{C3}q^3 + p_{C2}q^2 + p_{C1}q + p_{C0}\,. \tag{4.33}$$

The fitting parameters of p_{Ci} are listed in Tables 4.5 and 4.6.

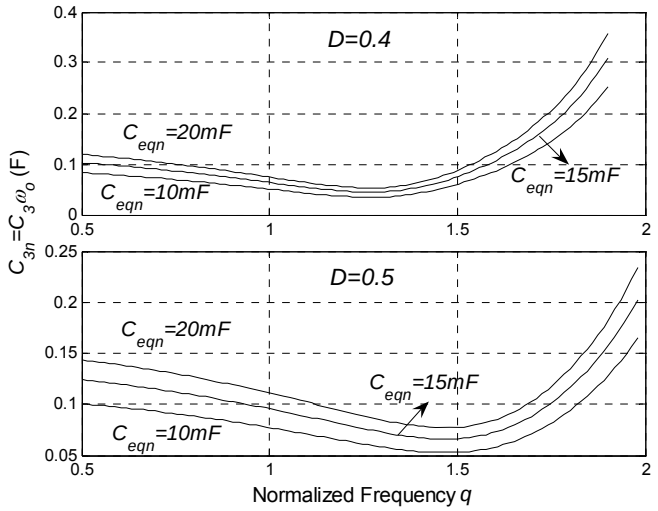


Figure 4.10. The normalized capacitance value C_{3n} vs. q for different C_{eqn} values. α=0.3. D=0.4 and 0.5.

Table 4.5. The Fitting Parameters to Compute C_{3n} (D=0.4, α=0.3)

C_{eqn}	10 mF		15 mF		20 mF	
q	0 ~1.1	1.1~1.7	0~1.1	1.1~1.7	0~1.1	1.1~1.7
p_{C3}	9.008E-2	4.888E-3	0.1413	7.237E-3	0.1793	9.018E-3
p_{C2}	6.150E-2	-5.10E-2	-6.168E-2	-6.331E-2	-0.1430	-7.356E-2
p_{C1}	-0.5798	3.775E-3	-0.5130	5.046E-3	-0.4889	6.045E-3
p_{C0}	0.4872	9.309E-2	0.5063	0.1149	0.5371	0.1331

Table 4.6. The Fitting Parameters to Compute C_{3n} (D=0.5, α=0.3)

C_{eqn}	10 mF		15 mF		20 mF	
q	0 ~1.2	1.2~1.8	0~1.2	1.2~1.8	0~1.2	1.2~1.8
p_{C3}	2.644E-3	0.3351	3.550E-3	0.4095	4.270E-3	0.4722
p_{C2}	-3.559E-2	-1.214	-4.370E-2	-1.488	-5.050E-2	-1.719
p_{C1}	2.283E-3	1.401	2.901E-3	1.725	3.407E-3	1.996
p_{C0}	0.1080	-0.4469	0.1330	-0.5539	0.1540	-0.6429

The design procedure of the PA is summarized below.

Step 1. Choose the parameters of D, C_{eq}, and q according to the required targeted power and supply voltage. Compute the inductance value L_0 accordingly.

Step 2. Choose the parameters of α and β to determine C_0, C_1 and C_2.

Step 3. Compute the output network of L_1 and C_3.

Step 4. Ensure all the component values to be within the practical range for on-chip

integration. Otherwise go back to Step 1 to adjust the design variables.

To illustrate the advantage of our proposed circuitry, we present a design example of a 433-MHz Class-E PA for on-chip integration with 3 dBm output power. Normally the low-power PAs at such low frequency range require inductance values larger than 40 nH, making it impractical to be implemented on-chip due to huge area penalty and poorer quality factor [29, 40]. Our proposed circuitry can potentially overcome such issues and provide full chip solution even for such a low operating frequency. The simplified design equations are adopted to design this PA. The on time duty cycle D is chosen to be 0.4, and the normalized frequency q is selected to be 1.55 to reduce the output power level and the required inductance values. The values of α and β are both chosen to be 0.3. The supply voltage is set to be 0.5-V. From Eq. (4.31), it can be derived that C_{eqn} should be 13.2 mF such that the output power is 3 dBm with 0.5-V supply voltage. In order to use the polynomial approximation formulae to compute L_{1n} and C_{3n}, we round C_{eqn} to 15 mF resulting in an output power of 2.28 mW. The values of L_{0n}, C_{0n}, C_{1n} and C_{2n} can be obtained from the equations depicted in Table 4.1. The values of L_{1n} and C_{3n} are obtained from Eq. (4.32) and (4.33). The unnormalized component values of the PA are summarized in Table 4.7. The simulated PSS waveform of the switch voltage is plotted in Fig. 4.11. It can be seen that the waveform satisfies the Class-E requirements well. The maximum inductance required is only about 10.2 nH facilitating a fully on-chip solution.

Table 4.7. Component Values of the PA

C_0	C_1	C_2	C_3	L_0	L_1
1.65pF	5.52pF	12.9pF	32.8pF	10.2nH	9.56nH

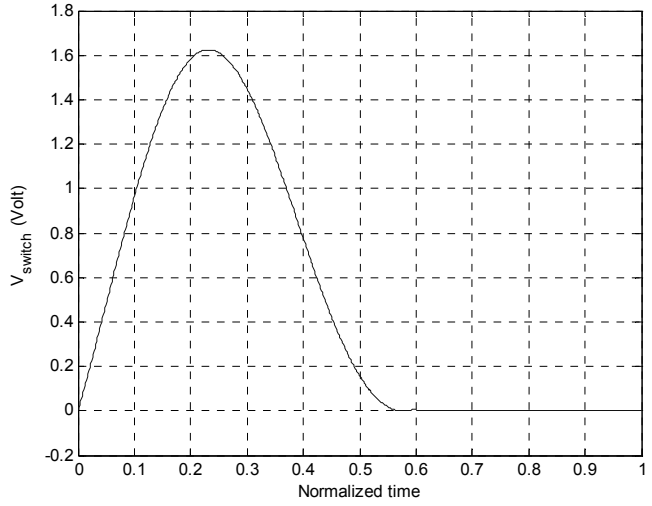


Figure 4.11. The simulated PSS voltage waveform of the switch. The time is normalized to one period.

4.5. Prototype Circuit Design and Measurement Results

In this section, the design and measurement results of a 2.4-GHz PA with output power levels around 0 dBm are presented. This PA is implemented in 0.13μm CMOS technology. The die of the PA is encapsulated in a Quad-Flat-No-leads (QFN) package.

The design parameters are chosen as: α=0.42, β=0.3, q=1.26 and C_{eqn}=12.3 mF. With this setting, the output power is about 2.5 mW with 0.5-volt supply voltage if all the components are ideal. This guarantees the output power to be close to 0 dBm by assuming an overall energy efficiency of 50% when the PA is implemented in CMOS. The circuitry of the PA and all the component values are shown in Fig. 4.12. The switching transistor M_1 is designed to have a large W/L ratio (180μm/0.12μm) to reduce the 'on' resistance. Note that the minimum transistor length is 0.12 μm in this 0.13μm CMOS process. All the parasitic capacitances at the drain terminal of M_1 are lumped into the parallel capacitance C_0. Two identical output pads are implemented at the output node. Therefore two bonding wires in parallel connect the PA's output to the package lead. This reduces the influences of the bonding wire inductance

by half. The output node of the PA is DC biased to ground potential without any need of DC block capacitor or other external components. The parasitic capacitances of the output pads are lumped into C_3. The gate capacitance of the switching transistor M_1 is large for its relatively large aspect ratio. If a CMOS inverter composed of both NFET and PFET is used as the pre-driver, the inverter itself consumes high power because of the large loading capacitance, hence degrading the overall efficiency. To reduce the power consumption, an inductively biased NFET inverter composed of M_0 and L_2 is used as the pre-driver. The inductance L_2 helps to tune out the gate capacitance of M_0. The transistor M_0 is designed to have a small aspect ratio (15μm/0.12μm) to reduce the loading capacitance of the previous stage. A small sized CMOS inverter is used to drive the gate of M_0. The RF tone is generated from an on-chip VCO locked by a PLL. The pre-driver and the PA share the same power supply with a nominal voltage of 0.5V and the CMOS inverter works with a supply voltage of 1.2V. When the gate driving voltage of M_0 is high, V_0 is pulled down to a low voltage closed to 0. Hence the transistor M_1 is turned off. When the driving voltage of M_0 is low, V_0 is determined by the transient waveform defined by L_2 and the total capacitances at the drain node of M_0.

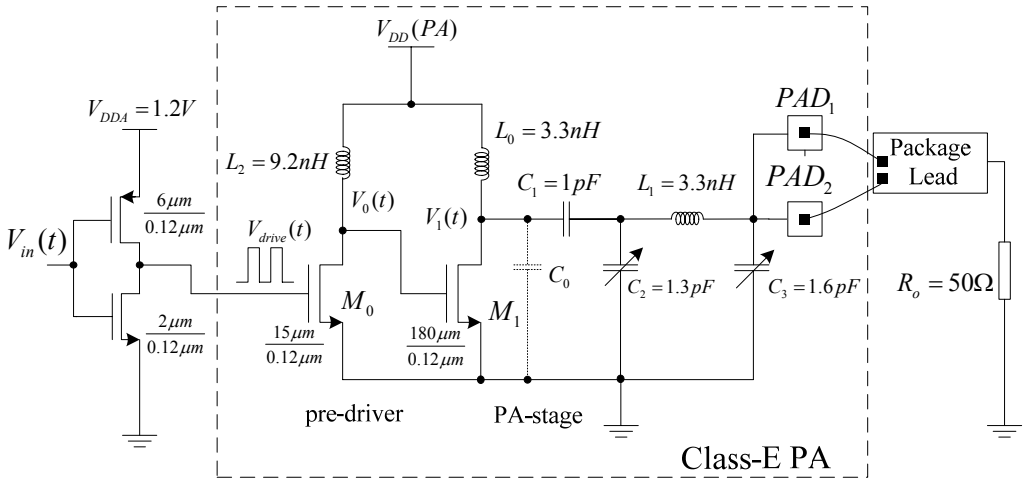


Figure 4.12. The circuitry of the proposed 2.4-GHz PA.

The analytical formulae and waveforms derived in the previous sections are based on ideal

devices. When the PA is implemented in CMOS as depicted in Fig. 4.12, simulations are needed to characterize the circuit performance with lossy elements and nonideal driving voltage of the switch. The simulated PSS waveforms of V_0, V_1 and the channel current of M_1 (i_{M1}) are plotted in Fig. 4.13(a) with a supply voltage of 0.5 V. Because M_1 has a large aspect ratio, it is approximately turned off when V_0 is below the threshold voltage V_{th}, and turned on when V_0 is larger than V_{th}. The on duty cycle is about 40%. The normalized power loss ($P_{Loss\_M1\_norm}$) and accumulated power loss ($P_{ACC\_M1\_norm}$) are defined in Eq. (4.34) and (4.35), and their waveforms are plotted in Fig. 4.13(b). It can be seen that there are two positive peaks in the waveform of $P_{Loss\_M1\_norm}$. The first peak is due to the reason that M_1 is turned on slightly before V_1 reaches zero. The second peak is because of the finite 'on' resistance of M_1. The energy loss from the switching transistor M_1 accounts for 13.6% of the total power of the entire PA (including the PA-stage and pre-driver).

$$P_{Loss\_M1\_norm}(t) = P_{Loss\_M1}(t) / P_{DC,PA}. \tag{4.34}$$

$$P_{ACC\_M1\_norm}(t) = \frac{1}{T}\int_0^t P_{Loss\_M1\_norm}(t)dt. \tag{4.35}$$

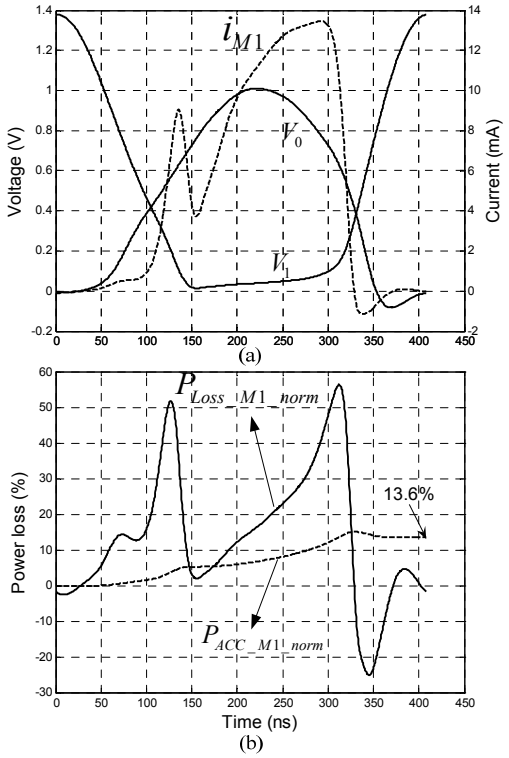


Figure 4.13. Simulated PSS waveforms in one complete cycle of (a) V_0, V_1 and i_{M1}. (b) Normalized power loss and accumulated power loss of M_1.

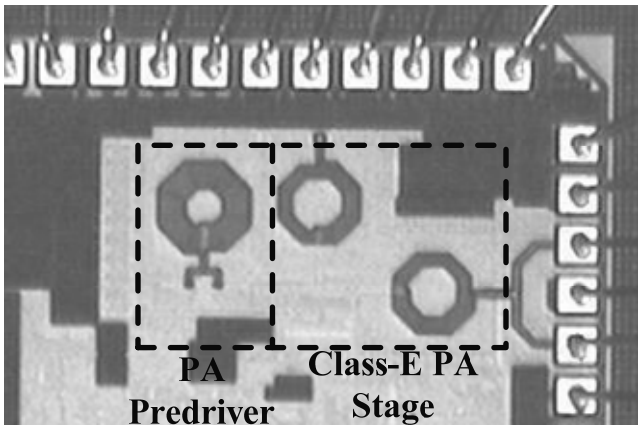


Figure 4.14. The die photo of this work.

As the pre-driver is an indispensible stage, when we refer to 'PA', both the pre-driver and PA stage are included. The microphotograph of the PA is shown in Fig. 4.14. The core area is 0.5 mm^2 and the total area with bonding PADs is 1.0 mm^2. It should be noted that the input port of the PA (composed of the PA-stage and the pre-driver) is mainly the gate capacitance of M_0 instead of being matched to 50 Ω. It is driven by a small sized CMOS inverter as shown in Fig. 4.12. The input power (P_{in}) of the PA is mainly caused by the signal feed through between the gate and drain nodes of M_0 through the C_{gd} of the transistor. Due to the small size of M_0, P_{in} is quite small. Simulation results verify that the power gain of the total PA is larger than 20 dB when V_{DD}>0.35-V, implying the differences between PE and PAE is less than 0.5%. Although PAE is a good definition for stand-alone PAs with 50Ω input impedance matching, overall PE is a better indication to characterize integrated PA from the system point of view [44]. We therefore use PE to evaluate the performance of the PA. Only the component at the fundamental frequency is taken into account when computing the output power and efficiency. The results are shown in Fig. 4.15. The input frequency is set to be 2.45 GHz. The measured power levels and efficiencies are slightly lower than the simulation prediction. This may be caused by the process variation and imperfect matching and excessive losses from the testing PCB. When the supply voltage varies from 0.45 to 0.8 V, the measured output power level ranges from 1 to 3.7 mW, and the overall PE is from 53.5% to 55%. According to simulation, the PA's pre-driver consumes about 2% to 3% of the total

power. Therefore it has no significant impact on the overall performance. Fig. 4.16 shows the simulated and measured results under different frequencies. The measurement frequency is confined to 2.1~2.5 GHz due to the limited tuning range of the on-chip VCO. According to the measurement, in the 300 MHz bandwidth from 2.2 to 2.5 GHz the PE variation is less than 2% and the output power level changes less than 5%. This implies the PA can operate in a wide frequency range. The measured 2nd and 3rd order harmonics are less than -25.5 and -41 dBc respectively. Therefore the energy losses at higher harmonics are negligible.

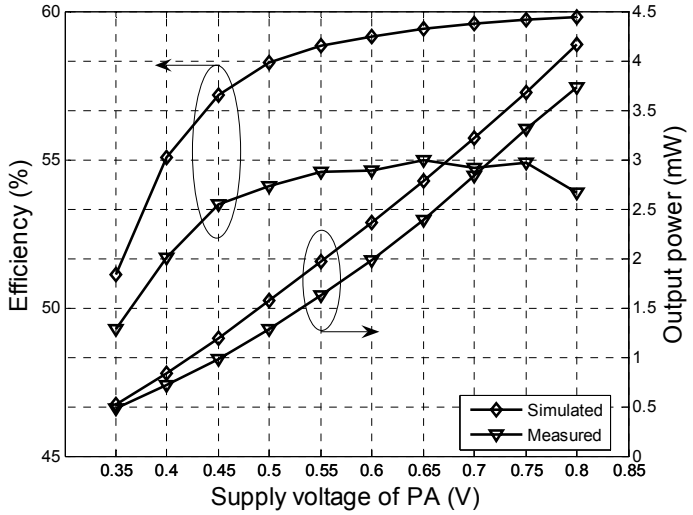


Figure 4.15. The simulated and measured results of the output power and overall efficiency of the PA (pre-driver and PA-stage) at frequency of 2.45 GHz.

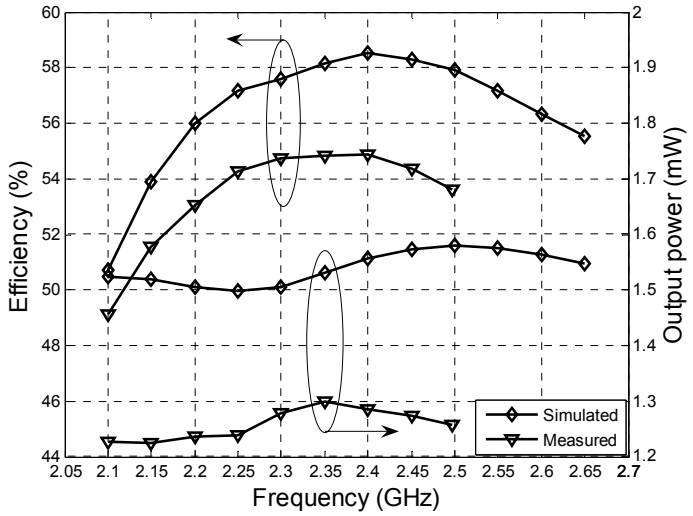


Figure 4.16. The simulated and measured results of the output power and efficiency of the PA (pre-driver and PA-stage) under different frequencies. The supply voltage is set to 0.5 V.

Comparisons are made between the proposed PA and existing low-power PA solutions. The core area of this PA is comparable with the existing integrated low-power PAs reported in [25], [82], and [27]. The Class-E PA in [82] is targeted at higher power levels (>6 dBm). Smaller inductances can therefore be used, which reduces the on-chip area. The low-power Class-C PA in [25] and the ILO PA in [27] only require one inductor, resulting in smaller area. However, their maximum PEs are worse as compared to the Class-E PAs in [10, 11, 28, 82] and this work. As pointed out earlier, most reported Class-E PAs are not optimized for low-power applications, and the measurement results are usually limited to 10 dBm and above. However, due to the characteristics of these Class-E PAs, the efficiencies are expected to deteriorate further with lower output power. As illustrated in Table 4.8, the power efficiencies for [10, 11, 28] worsen when the output power levels drop below 10 dBm. Although high PE of 52.5% is achieved in [82], only the DC feed inductor is integrated on-chip, lacking the output filter for harmonic suppression. Our structure exhibits superior efficiency at low output power levels without any need of external components. The achieved peak PE of 55% is at least 10% better than other types of low-power PAs reported in [24, 27, 38].

Table 4.8. Performance comparison with Existing PA.

PA Class	f(GHz)	P_{out} (dBm)	PE (%)	Core Area (mm^2)	Technology	Ref.
E-ILO	2.35	6/11	33/45.4	1.4	0.18 µm	[28][c]
E	2.40	10/20	34/69	----	0.18 µm	[10, 11][a,b]
E	2.40	6/10	52.5/52.5	0.45	0.18 µm	[82][c,d]
ILO	2.40	7.6	36	0.34	0.18 µm	[27] [c]
C	2.34	-5.2	45	0.45	0.13 µm	[24][c]
AB	2.40	0	33	0.07	90 nm	[38][c,e]
E	2.45	0/2/ 4/5.7	53.5/54.6/55 /53.9	0.5	0.13 µm	This Work

Unless stated, all designs are implemented in CMOS technology and use on-chip spiral inductors.
[a] SiGe technology….. [b] Bonding wire inductors….. [c] Estimated core area
[d] Only the DC feed inductor is integrated, lacking the output filter.
[e] Off-chip matching network/inductors required.

4.6. Conclusion

In this chapter, a new circuitry of Class-E PA is presented. The PA is optimized for delivering low output power level with high efficiency and allows for fully integrated solution. Explicit design equations are derived to characterize the PA. As a proof of concept, a 2.4-GHz Class-E PA is implemented in 0.13μm CMOS technology. Measurement results show the PA can deliver an output power level from -3.2 to 5.7 dBm with maximum efficiency of 55% including the auxiliary pre-drive stage.

CHAPTER 5 CIRCUIT DESIGN OF THE TRANSCEIVER

In this chapter, detailed circuit designs of the transceiver are presented. The TX of the transceiver is introduced first. The RX designs for BPSK and OOK are presented next. Finally the LO generation circuits including the VCO/DCO, PLL, and the frequency calibration modules are presented.

5.1. TX Design

As discussed in the system design part, the TX of the transceiver is composed of the PA and the BPSK modulation MUX. The VCO generates the two signal phases of 0º and 180º. The BPSK MUX selects one of the signal phases according to the input bit, and drives the PA. For OOK transmission, the input phase is fixed (either to 0º or 180º). The OOK transmission is realized by turning on or off the PA directly. The circuitry of the whole TX is shown in Fig. 5.1.

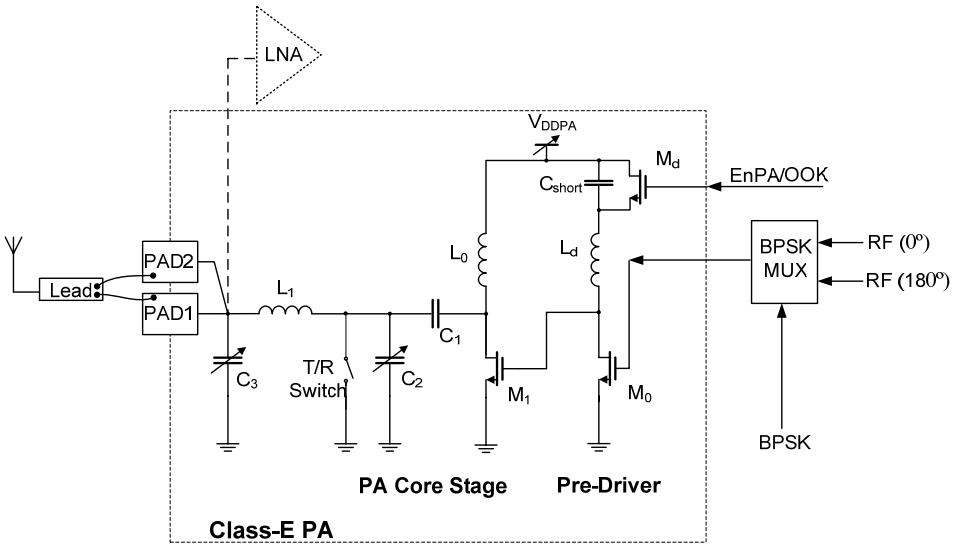


Figure 5.1. The transmitter circuitry.

The BPSK MUX is simply realized by the digital combinational logic circuits as shown in Fig. 5.2.

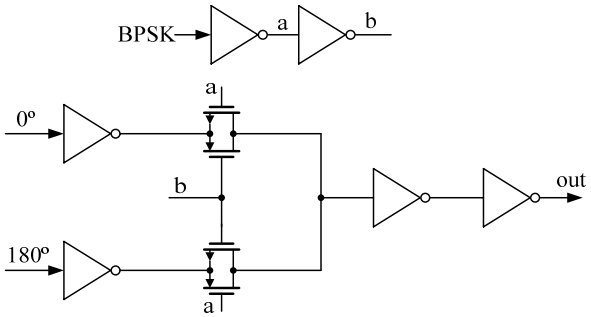
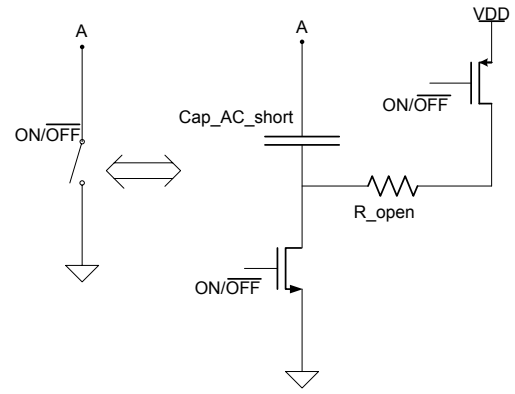


Figure 5.2. The BPSK MUX Circuitry.

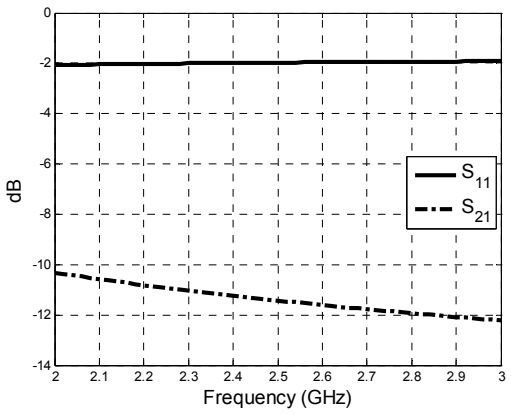
The Class-E PA circuit architecture presented in Chapter 4 is used to design the PA. As the TX and RX share the same antenna, co-design of the PA and LNA is considered. Although the LNA is turned off by setting its biasing current to 0 during the TX mode, it still induces parasitic capacitances at the input. As the Class-E PA incorporates a π-matching output network of L_1, C_2 and C_3, all the parasitic capacitances at the output node of the PA can be lumped into C_3, which includes the capacitances from the input of LNA, the output pads, and all the parasitic capacitances from interconnections. As a result, the influence of the LNA is taken into account during the PA design. Two parallel I/O pads are bonded to the same package lead in order to reduce the bonding wire inductance.

The conventional way to separate the TX and RX is to put the T/R switch directly in the RF signal path, which inevitably introduces losses and degrades the power efficiency of TX. In this design, the T/R switch is not located in the signal path. The switch is open during the TX mode, and closed in the RX mode. As one terminal of the switch is ground, it can be simply realized by an NFET with relatively large W/L ratio, which works either in deep triode region or off region. When the switch is off in the TX mode, the parasitic capacitance from the switch can be lumped into C_2. When it is on in the RX mode, the inductance L_1 can resonate with all the capacitances at the input of the LNA, which helps to improve the input matching

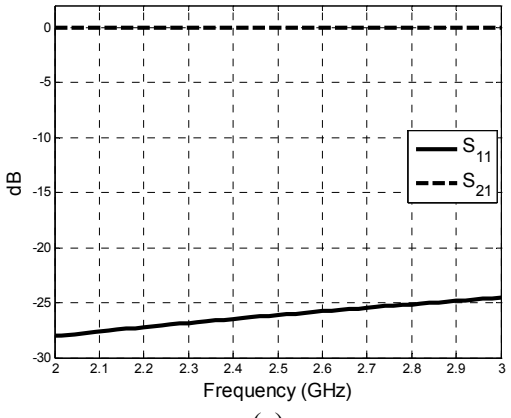
of the RX. This will be discussed in more detail in the RX design. The detailed circuit implementation and the simulated performances of the switch are shown in the following figure.



(a)



(b)



(c)

Figure 5.3. Circuit and performance of the switch. (a). Circuit implementation of the switch. (b). S_{11} and S_{21} when the switch is on. (c). S_{11} and S_{21} when the switch is off.

When the switch is on, the capacitance creates an AC short, and the NFET is turned on. When the switch is off, the drain terminal of the NFET is biased to V_{DD} to prevent leakage current. The simulated input reflection coefficient (S_{11}) and forward voltage gain (S_{21}) when the switch is turned on and off are plotted in Fig. 5.3(b) and Fig. 5.3(c) respectively. When the switch is on, the simulated S_{11} is about -2 dB within the 2.4GHz ISM band, which is close to 0 dB in the ideal case. The difference is caused by the impedance of the capacitor and the NFET. S_{21} is below -10 dB which implies most input energy is diverted to ground. When the switch is off, S_{11} is below -25 dB and S_{21} is close to 0 dB, implying a good 'off' state of the switch. The finite S_{11} is due to the leakage caused by parasitic capacitance.

The pre-driver of the PA is slightly different from the one introduced in the previous chapter as shown in Fig. 4.12. An on/off switching transistor M_d (in Fig. 5.1) is incorporated to either turn on or off the PA. When this transistor is turned on, it provides the DC current which is needed for the pre-driver. As the conductivity of the transistor degrades a lot at the RF frequency, the capacitance C_{short} (32 pF) creates approximately short circuit at the RF frequency. When M_d is turned off, the drain voltage of M_0 is pulled down to ground, hence turning off the entire PA.

The PA is expected to deliver about 0 dBm output power with a nominal supply voltage of 0.5-V. The design parameters of the PA are chosen as: α=0.48, β=0.37, q=1.24 and C_{eqn}=9.5 mF. The output power of the PA is about 2 mW with 0.5-V supply voltage if all the components are ideal. Assuming a power efficiency of 50% in real CMOS circuit implementation, the output power is about 1 mW or 0 dBm. By setting the operation frequency to 2.45 GHz, the unnormalized component values of the PA are summarized in the following table. The switch transistor M_1 is designed to have a large aspect ratio of: 180μm/0.12 μm. The inductance L_2 in the pre-driver is chosen to be 9.8 nH. The transistor M_0 has a small W/L ratio of 12 μm /0.12 μm, resulting in a small input capacitance.

Table 5.1. The component values of the Class-E PA for the transceiver.

C_1	C_2	C_3	L_0	L_1
$0.75pF$	$0.81pF$	$0.92pF$	$4.4nH$	$4.2nH$

This parameter setting is also helpful for the RX design. At 2.45 GHz, L_1 (4.2 nH) resonates with a capacitance of 1.0 pF, which is very close to C_3. By incorporating digital tuning to C_3, it can resonate with L_1 in the RX mode, and improves the input matching.

Post layout simulation indicates that the PA achieves an overall power efficiency of 59% while delivering 1.35mW under 0.5-Volt power supply.

5.2. BPSK RX Design

The overall block diagram of the BPSK RX is shown in the following figure. The RF amplifiers include the LNA and LNA buffer. The LNA helps to improve the NF of the system and provides impedance matching. The LNA buffer drives an RC-CR PPF circuit which separates the signals into I and Q paths. The mixer down-converts the RF signal to IF (5 MHz). The analog baseband (ABB) part consists of the BB-buffer, channel filter, VGA, and output buffer. The supply voltage of the RX is 1-Volt. The detailed circuit of each building block is discussed in detail below.

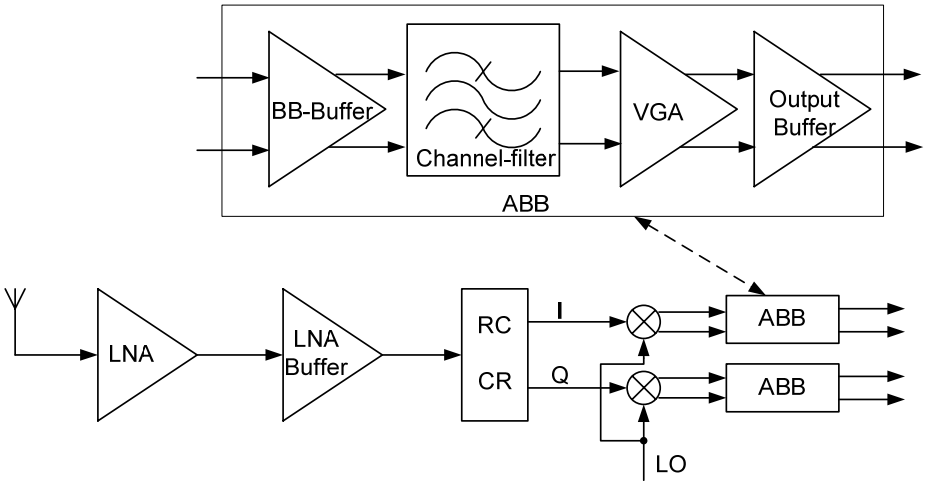


Figure 5.4. The circuit diagram of the BPSK RX.

5.2.1. LNA

The LNA for BPSK is optimized to achieve good performance. Common Gate (CG) amplifier is used to achieve 50Ω input impedance matching. The parallel resonant circuit composed of L_1 and C_3 (reused from the PA as shown in Fig. 5.1) forms a pre-filter to reject the out-of-band interferences and improves the input matching by tuning out the parasitic capacitance at the input node of the LNA. Although it is possible to use an additional inductor as the output loading of the LNA to improve the gain and NF, this would cause large area penalties due to the relatively large sizes of on-chip spirals. Resistive loading is hence chosen as the LNA's output loading to save area. Because the on-chip resistance is subject to 10 to 20% variation, the DC operating point may deviate away from the design point, which degrades the gain and NF of the LNA. To circumvent this problem, a PMOS loading is connected in parallel with the resistor, as shown in the following figure. The gate biasing of the PMOS is controlled by a feedback loop. A LP filter composed of R_o and C_o extracts out the DC potential of the output node. The Op Amp forces the DC operating point to be approximately equal to the biasing voltage of V_{DC}, which is set to 0.6 of V_{DD}. This feedback topology ensures a stable output

voltage regardless of the process variations. The DC current of the LNA is 1.9 mA. The LNA provides a gain of about 8.4 dB according to simulation.

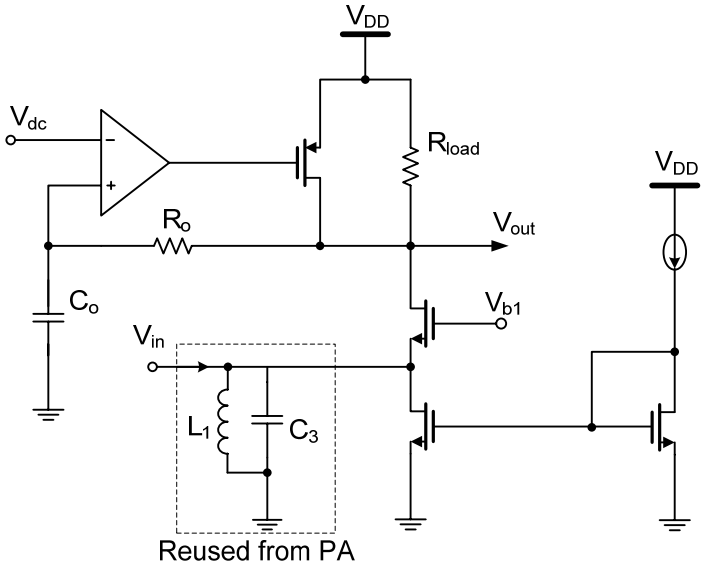


Figure 5.5. The schematic of the LNA for BPSK receiver.

5.2.2. LNA Buffer and the RC-CR PPF.

After the 1st LNA stage, the signal is amplified by the buffer stage, which drives an RC-CR PPF. The RF signal is then separated into the I and Q paths to allow quadrature mixing in the latter stage of the mixer. To save area, no inductor is used in the buffer stage either. Common source (CS) topology is used for the buffer stage. To boost up the gain, both the NFET (M_{n0}) and PFET (M_{p0}) are used as amplification transistors. Similar feedback technique is used to stabilize the DC operation point by controlling the gate bias of the PFET M_{p1}. The DC voltage of the output node is biased at half of V_{DD} to ensure all the transistors are in the saturation region. The size of M_{p0} is chosen to be three times larger than M_{p1} to increase the transconductance and hence the gain of the amplifier.

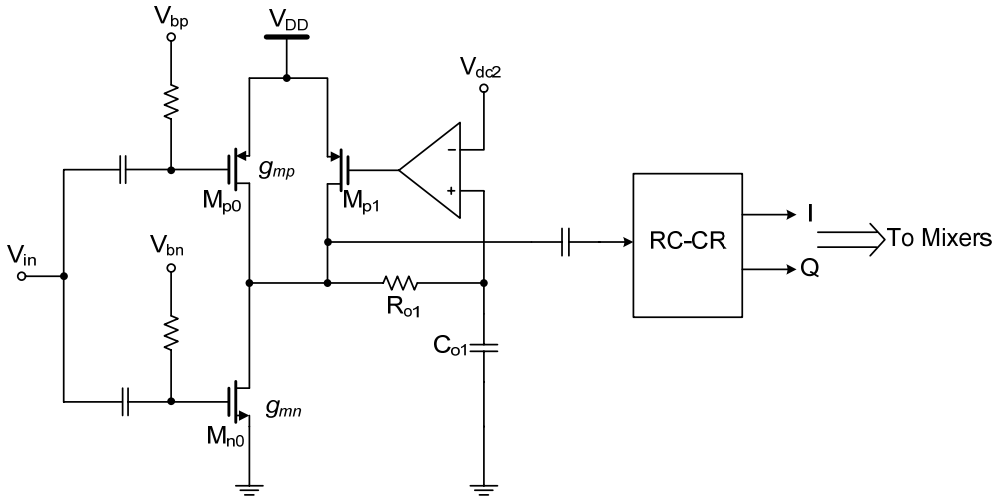


Figure 5.6. The schematic of the LNA buffer.

The RC-CR PPF circuit serves as output loading of the LNA buffer, and it splits the RF signal into the I and Q paths at the desired frequency, as shown in the following figure. The I and Q signals are fed into mixer for down conversion. The DC voltage biasing required for the mixer is included in the RC-CR filter circuitry through the large resistance R_b. With this configuration, the generated I and Q signals can be directly connected to the inputs of mixer.

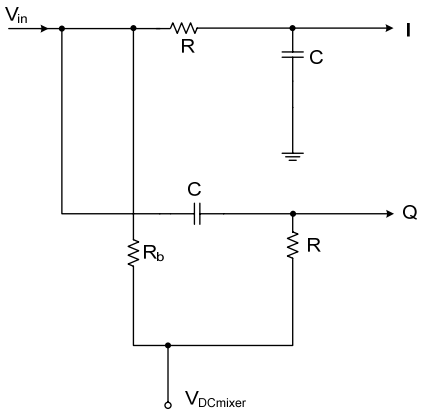


Figure 5.7. The circuitry of the RC-CR PPF.

In order to equalize the gains of the I and Q channels, the R and C value should satisfy the following equation:

$$RC = 1/\omega_o, \tag{5.1}$$

where ω_o is the angular frequency of the RF signal. The R and C values are chosen such that the gain of the buffer stage is reasonable and does not degrade the overall noise performance of the receiver. The total impedance of the RC-CR circuit is given by:

$$\left|Z_{RCCR}(\omega)\right| = \frac{1}{2}\sqrt{R^2 + \frac{1}{(C\omega)^2}}\,. \tag{5.2}$$

By combining the above two equations, it can be seen that the magnitude of the impedance becomes $\frac{\sqrt{2}}{2}R$ at the RF frequency of ω_o. The gain of the buffer stage including the RC-CR filter can be estimated by the following equation:

$$A_{buffer} \approx \frac{\sqrt{2}}{2}\left(g_{mn} + g_{mp}\right)\left|Z_{RCCR}(\omega_o)\right| = \frac{1}{2}\left(g_{mn} + g_{mp}\right)R\,. \tag{5.3}$$

In order to maximize the voltage gain, the resistance R should be chosen as large as possible. On the other hand, a larger R implies that the corresponding C value becomes small, which causes matching problems. As a result, the R and C values should be compromised to ensure sufficient gain while still maintaining good matching. In this design, the resistance R is chosen to be 352 Ω and the capacitance equals to 192 fF. The DC current biasing of the LNA buffer is chosen to be 1.2 mA. With these settings, the simulated gain of the LNA buffer is 2.2 dB. The physical dimension of the resistor is 3.4 by 4.8 μm and the capacitance size is 10.0 by 9.0 μm. With these dimensions, the corresponding 3σ matching of the resistance and capacitance is 1.8%.and 0.4% respectively. By assuming $RC\omega_o$=1, the voltage transfer functions of the RC-CR filter are expressed by the following two equations.

$$H_{RC}(\omega_o j) = \frac{j\left[1 + \frac{\Delta R_1}{R} + \frac{\Delta C_1}{C}\right]}{1 + j\left[1 + \frac{\Delta R_1}{R} + \frac{\Delta C_1}{C}\right]}, \tag{5.4}$$

$$H_{CR}(\omega_o j) = \frac{1}{1 + j\left[1 + \frac{\Delta R_2}{R} + \frac{\Delta C_2}{C}\right]}. \quad (5.5)$$

By substituting the maximum variations into the above two equations, the worst case gain error and phase error of the filter can be found to be 2.4% and 1.3º respectively. The actual matching performance should be better than this estimation by careful layout arrangement such that the matching is fine.

The tolerances of the absolute values of the resistance and capacitances should be considered as well. In IC implementations, the absolute values of the R and C components are subject to deviations from their nominal design values. According to the process documents, the 3σ tolerances of the absolute R and C values of the RC-CR filter are both about 10%. By analyzing the transfer functions of filter, it can be seen that the absolute value deviations of the R and C values only incur gain error. The 90º phase shift is still maintained. The gain error can be expressed by the follow equation:

$$e_{gain} = \left(\frac{\Delta R}{R_{norm}} + \frac{\Delta C}{C_{norm}}\right). \quad (5.6)$$

With maximum variations of 10% for both resistance and capacitance, the gain error in the worst case is 20%. Combined with the errors caused by the matching, the maximum overall gain error and phase error is about 20% and 1.3º respectively.

For gain error, it can be cancelled out by digital BB signal processing such that the I and Q channel have almost the same output power levels after calibration. The image rejection ratio (IRR) is mainly determined by the phase error. In [47], an approximation equation is given to estimate the IRR as follows:

$$IRR = 10\log\left(\frac{\left(\Delta A / A\right)^2 + \theta^2}{4}\right), \quad (5.7)$$

where $\Delta A / A$ represents relative gain error and θ is the total phase error in rad. By assuming zero gain error ($\Delta A / A$=0) and the phase error of $\theta = 1.3^{\circ}$, the estimated *IRR* by Eq. (5.7) is -39 dB. In actual circuit implementations, the gain error cannot be thoroughly compensated. Therefore the actual *IRR* should be worse than -39 dB. For example, if the residue gain error is 2%, the *IRR* degrades to -36.4 dB.

As the mixers form the loading of the RC-CR filters, the gate capacitances of the mixers should be considered. The influences of the mixers' input capacitances are analyzed here. As shown in the following figure, the input gate capacitance is denoted by C_{mx}.

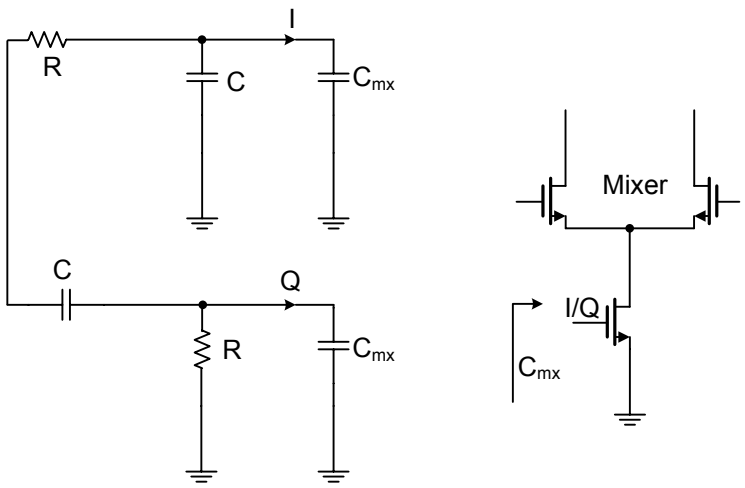


Figure 5.8. RC-CR filter with parasitic capacitance from the input of mixer.

With the parasitic capacitance taken into consideration, the transfer function of the I and Q path can be expressed by the following two equations.

$$H_I = \frac{1}{1 + R(C + C_{mx})S}. \tag{5.8}$$

$$H_Q = \frac{RCS}{1 + R(C + C_{mx})S}. \tag{5.9}$$

It can be seen that the even with the additional parasitic capacitance as the additional loading at the output of the RC-CR filter, the 90º phase shift between the I and Q channels is still maintained. The gains of the I and Q channels also equal to each other as long as Eq. (5.1) is satisfied. Therefore the additional capacitive loading caused by the mixer does not affect the performance of the RC-CR filter.

5.2.3. Mixer

As the outputs of the RC-CR PPF are single-ended, there is no need to use double balanced mixer. Single balanced active mixer is used in this design to save power. Current bleeding technique is incorporated to reduce the currents for the switching transistor pairs, thus allowing more abrupt switching of the currents. With current bleeding, the loading resistance can be increased to boost the gain of the mixer. The circuitry is shown in the following figure. The bleeding current is 3-bits adjustable to guarantee proper DC operating point with process variations. By assuming ideal switching of the differential pair, the conversion gain of the mixer can be expressed by the equation below.

$$A_{mx} = \frac{4}{\pi} g_m R_o . \tag{5.10}$$

The resistance R_o and the total capacitance C_o at the output node form a LP filter which filters out the high frequency components. The output resistance is chosen to be 6.0 kΩ, and DC biasing current is 0.65 mA. The gates of the switching transistors are directly driven by the VCO. The simulated conversion gain of the mixer is about 18 dB.

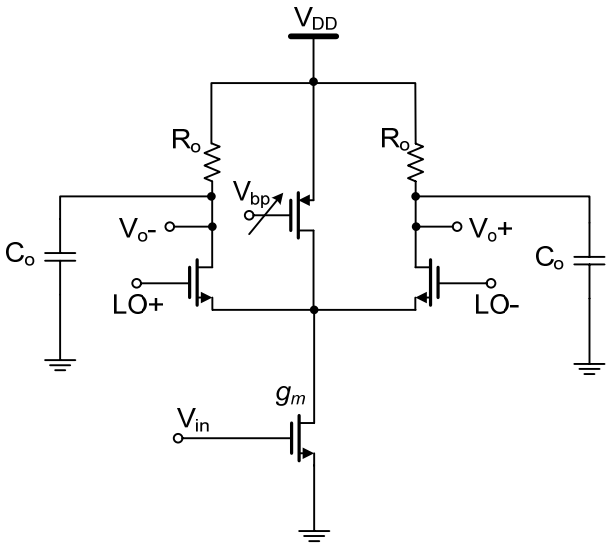


Figure 5.9. The circuit of the mixer.

Post-layout simulation is done to check the overall functionality and performance of the BPSK RF-Front-End (RFFE) including the LNA, LNA buffer, RC-CR filter, and the mixer. The conversion gain (S21), input matching (S11) and NF are plotted in the following figures. The conversion gain of the RFFE is about 28 dB and the input matching is about -26 dB. The simulated NF of the I or Q channel (by single-phase mixing) is about 14 dB at 5 MHz. As pointed out earlier, the overall NF of the receiver with both I and Q channels is about 3 dB better than the single channel result. Therefore the overall NF of the RFFE is close to 11 dB.

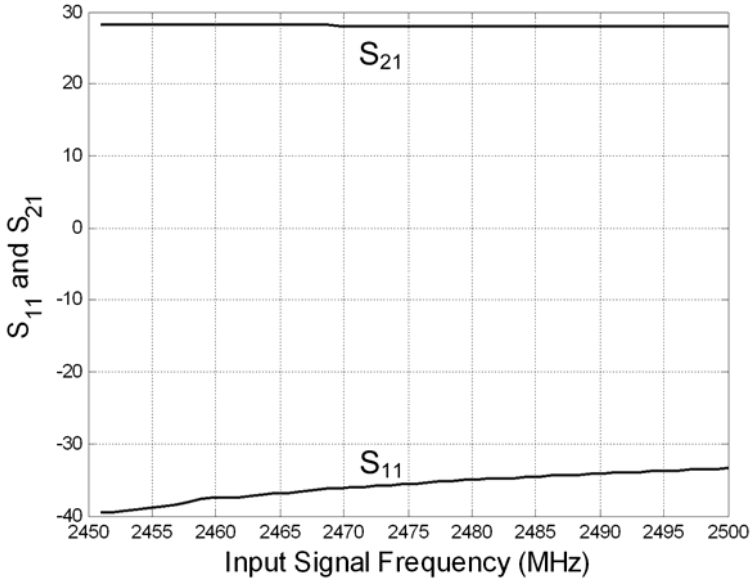


Figure 5.10. Simulated conversion gain (S_{21}) and input reflection coefficient (S_{11}) of the complete RFFE. LO is placed at 2.45GHz.

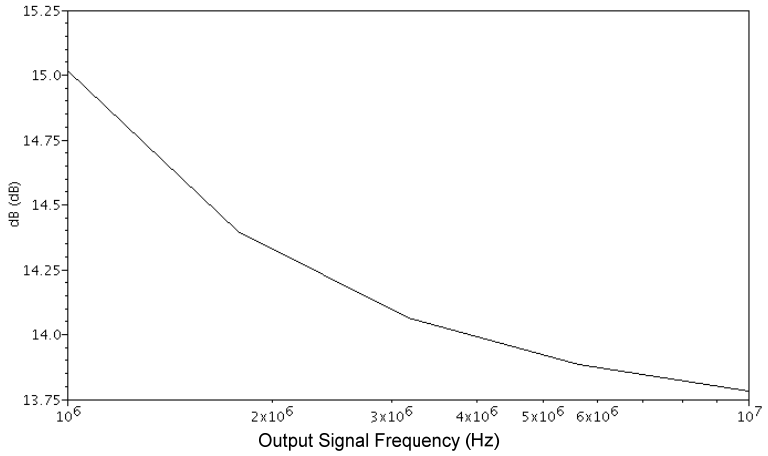


Figure 5.11. The simulated noise figure of the single I or Q channel.

5.2.4. Analog Baseband (ABB)

After the mixer stage, the frequency of the signals are down converted to IF which equals to 5 MHz. Before the signals enter the filter and VGA, they are firstly amplified by a buffer stage which provides an additional gain of about 9 dB and hence relaxes the noise requirements of the subsequent stages. The buffer amplifier is composed of an open-loop amplifier with

resistive output loading, as shown in the following figure. Source degeneration is incorporated to improve the linearity of the amplifier. The degeneration resistance (R_{dg}) and output resistance (R_o) are chosen to be 0.39 and 5.0 kΩ respectively.

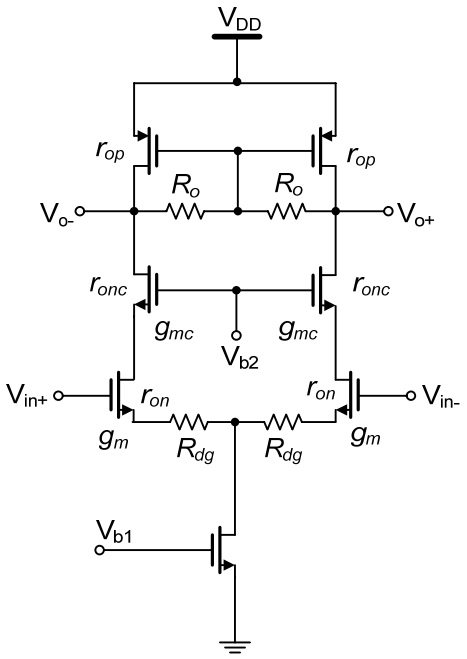


Figure 5.12. The schematic of the buffer stage.

The total gain of the amplifier can be calculated by the following equations:

$$G = \frac{R_{out}}{R_{dg} + g_m^{-1}} = \frac{R_{out} g_m}{1 + R_{dg} g_m}, \tag{5.11}$$

where g_m is the transconductance of the input transistor. R_{out} is the total impedance at the output node of the amplifier. Cascode topology is used to increase the output impedance and hence the gain. The total output impedance can be expressed by R_o in parallel with the output impedance of the transistors as shown in the following equation:

$$R_{out} = R_o // r_{op} // \left[r_{on} (1 + g_{mc} r_{onc}) \right]. \tag{5.12}$$

The tail current of the amplifier is tunable from 100 to 150 μA. With source degeneration, the input voltage amplitude (differential) can reach up to 90 mV for output THD ≤5%. The

simulated gain of the buffer is 8.7 dB. The input referred noise of the buffer is 17 $nV/\sqrt{Hz}$ at 5 MHz, which is equivalent to -142.3 dBm/Hz. This noise is then referred back to the LNA's input. With about 28 dB gain of the RFFE, the input referred noise of the buffer stage at the antenna port is -170.3 dBm/Hz, implying an NF of about 4 dB. As the NF of the RFFE is about 11 dB, therefore the receiver's noise is dominated by the RFFE. The overall noise figure of the receiver can be computed by summing the input referred noises of both the RFFE and the buffer, and is given by the following equation:

$$NF_{all} = 10\lg\left(10^{\frac{NF_{RFFE}}{10}} + 10^{\frac{NF_{buffer}}{10}}\right) \approx 12dB. \quad (5.13)$$

As a result, the overall NF of the receiver is increased by about 1 dB due to influence of the buffer. According the Friis equation for noise [47], the noises of the latter stages after the buffer are largely suppressed by the combined gain of the RFFE and the buffer stage which is about 36 dB. Their noise contributions to the system can be ignored.

5.2.5. Channel Selection Filter

The LP filter is used to pick up the desired signals while rejecting the unwanted interference signals at the neighboring channels. It also serves as the anti-aliasing filter for the ADC. As shown in the following figure, high order LP filter can better suppress the out-of-band signals than the low order (1st or 2nd order) LP filters. High order filter also helps to reduce the BB ADC sampling frequency with the same suppression ratio.

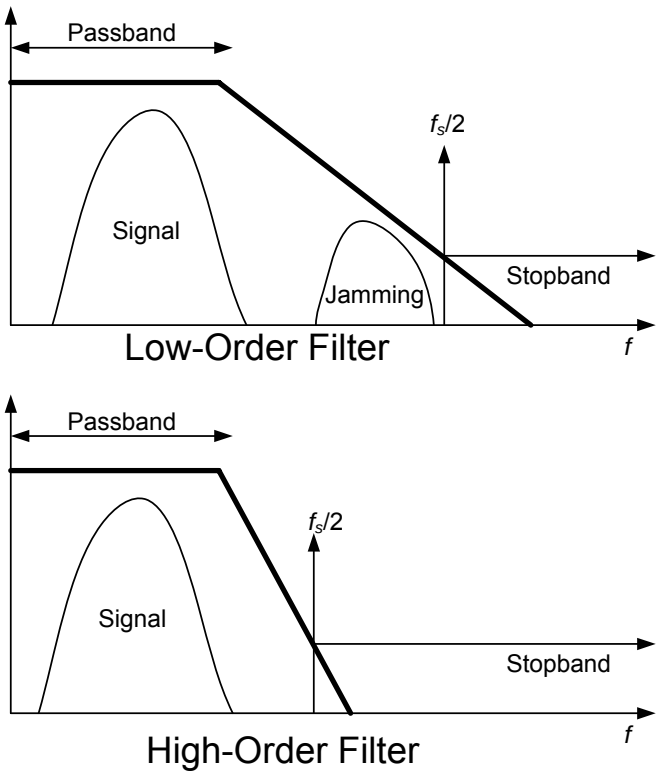


Figure 5.13. Comparison of the lower/higher order filters.

In this design, a 4th order Butterworth LP filter is employed for the channel selection filter. As the IF is chosen to be 5 MHz, the received signal is centered at this frequency. For BPSK modulations, the signal spectra are Sinc functions. The first lobe of the Sinc function occupies $\pm B$ Hz, where B is the BPSK bit rate. For the Sinc function with 1st null at B Hz, 70% of energy is located within the bandwidth of (-0.41B, +0.41B). Therefore to maintain most of BPSK energy (70%) for 10 Mbps data-rate, the filter needs to cover the frequency range of (IF-0.41B, IF+0.41B), which equals to (1MHz, 9MHz). The 3dB cutoff frequency of the LP filter should be larger than 9 MHz.

The transfer function of the 4th order Butterworth filter is expressed by the following equation:

$$H(s_n) = \frac{1}{(s_n^{\,2} + 0.7654 s_n + 1)\cdot(s_n^{\,2} + 1.848 s_n + 1)}, \tag{5.14}$$

where s_n is the normalized complex frequency and it equals to $\frac{s}{2\pi f_c}$. The filter is implemented through the state variable method [83]. The 4th LP order filter can be realized through four integrators as shown in Fig. 5.14(a). The detailed circuitry of the integrator is shown in Fig. 5.14(b).

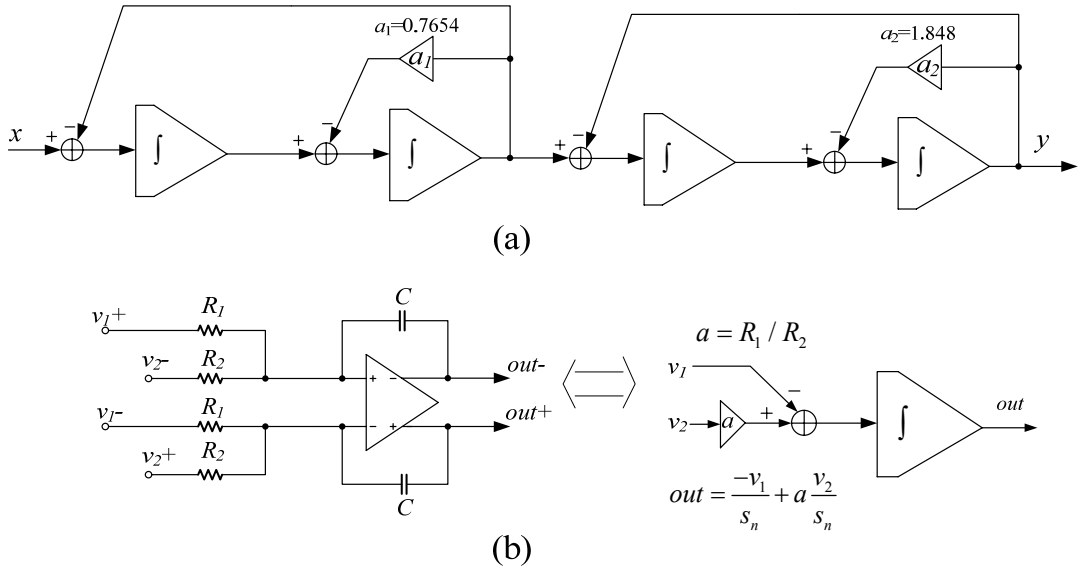


Figure 5.14. The implementation of the 4th order filter. (a). The block diagram of the filter. (b). Circuit implementation of the integrator.

In this design R_1 and C are chosen to be 42 kΩ and 400 fF respectively, resulting in a cut-off frequency of 9.5 MHz. For the two integrators with a=0.7654 and a=1.848 (in Fig. 5.14), the corresponding resistances of R_2 are chosen to be 54.7 kΩ and 22.6 kΩ respectively. It can be seen that all the components values are reasonable for on-chip realization. The smallest resistance is 22.6 kΩ which does not form a heavy loading for the previous stages.

The frequency response of the Butterworth LP filter from circuit level simulation is shown in the following figure. The simulation result shows a flat pass-band and sharp roll-off in the stop-band which verifies the design. The transfer function exhibits maximally 2.3 dB peaking effect near the transition frequency. This is due to the slightly insufficient phase margin of the

Op Amp used in the filter. As the 2.3 dB peaking is not severe, the filter can still be used for the BPSK signal filtering. The -3dB cut-off frequency is 9.3 MHz which is slightly lower than the theoretically computed frequency of 9.5 MHz. This is mainly due to the limited bandwidth of the Op Amp used for the filter, and the additional parasitic capacitance in the layout. The details of the Op Amp design will be described later.

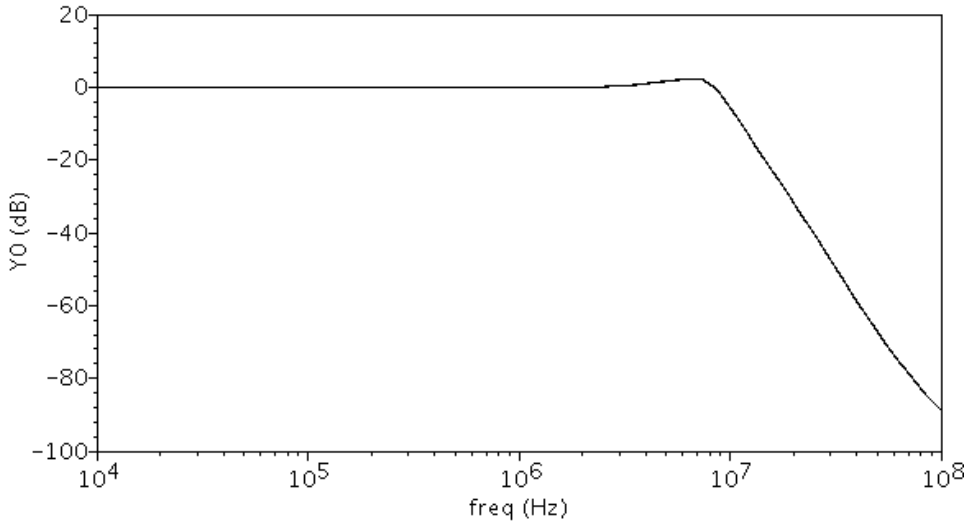


Figure 5.15. The simulated frequency response of the 4th Butterworth filter.

5.2.6. The VGA design

The VGA is composed of 4 tunable gain stages (Fig. 5.16). Each stage provides a gain of 0 or 9.5 dB. Gain tuning is realized by altering the feedback resistance through digital control. In the low-gain setting, the feedback resistance equals to R_o, resulting in a unit gain buffer. For the high-gain setting, the feedback resistance is $3R_o$, implying a gain of 3 or 9.5 dB. Relatively coarse tuning is provided by the VGA. Fine tuning step below 9 dB can be achieved in the digital domain. AC coupling is adopted for connecting the gain stages. Therefore the DC offset of the Op Amp does not propagate to the next stage. As pointed out earlier in the channel selection filter design section, the pass-band of the filter should at least cover the frequency range of (1MHz, 9MHz) to accommodate 70% energy of the 10 Mbps BPSK signal. Therefore it is reasonable choose the HP transition frequency to be below 1

MHz. In the VGA design, the input resistance R_o is chosen to be 35 kΩ, and the input capacitance is set to 6.5 pF. The HP 3dB transition point is hence 700 kHz. The simulated gains of a single sub-stage of the VGA are plotted in Fig. 5.17 which verifies the design. The bandwidth of the VGA is smaller in the high-gain mode than it is in the low-gain mode. This is due to the constant gain bandwidth product (GBW) of the Op Amp. Higher closed-loop gain implies lower bandwidth.

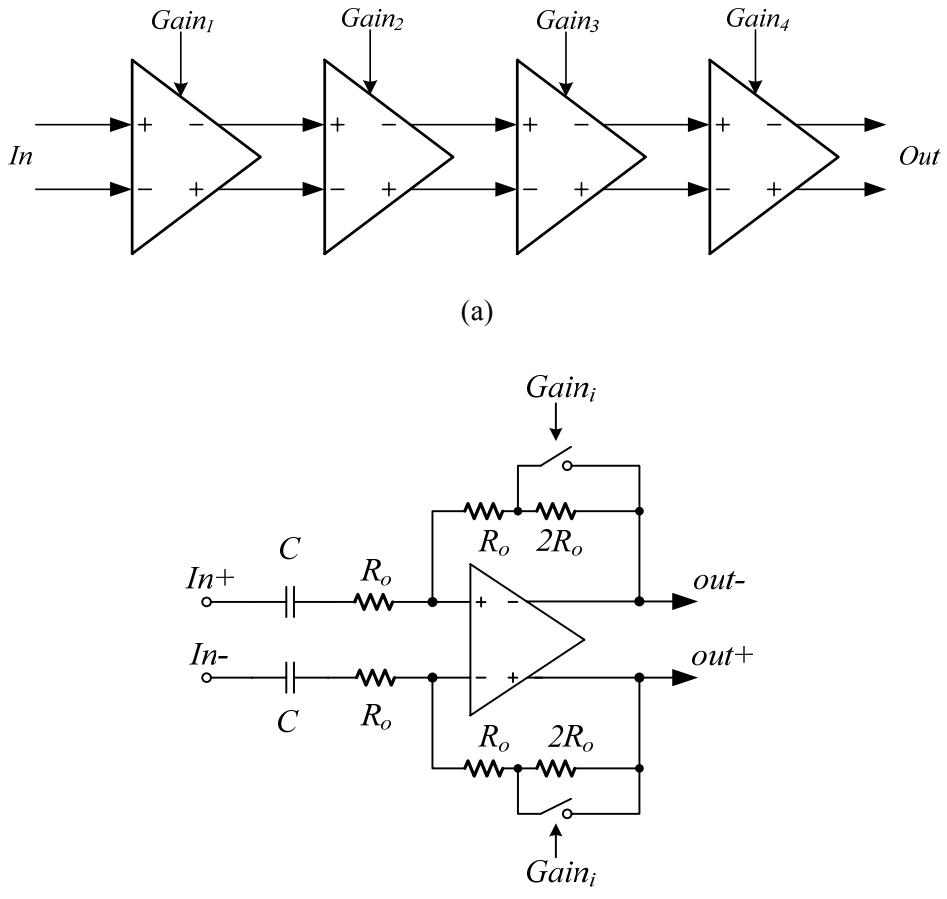


Figure 5.16. The VGA circuit implementation. (a) The VGA topology. (b) The detailed circuitry of each gain stage.

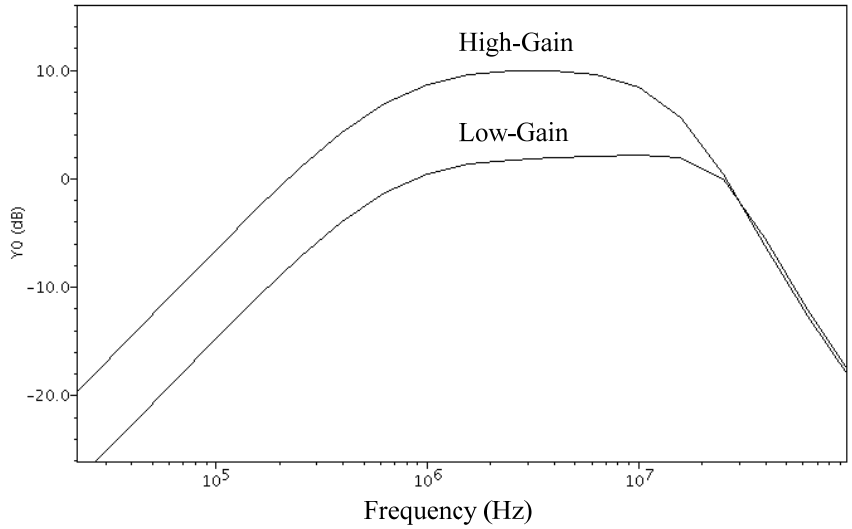


Figure 5.17. The simulated gain curves of a single variable gain stage.

5.2.7. The Op Amp Design

The design of the Op Amp used in the channel selection filter and VGA is introduced here. The amplifier is comprised of two stages (in Fig. 5.18). Miller compensation [47] is used to guarantee stability. The first stage mainly provides enough gain. The second stage is targeted at large output swing and drivability. The first stage of the Op Amp draws a current of 50 μA. The DC bias current for each output branch is 70 μA to increase the output drivability. The common mode feedback (CMFB) circuitry consumes 10 μA. The total current consumption of the Op Amp is therefore about 200 μA. The common mode voltage (V_{OCM}) of the output is sensed by two identical resistors. The CMFB circuitry controls the bias voltage of the PFETs (M_{p1} and M_{p2}) at the 1st stage of the Op Amp, such that the output common mode voltage approximately equals to common mode voltage (V_{CM}). In this design, V_{CM} is set to half of the supply voltage to maximize the output dynamic range.

As the VGA stages are AC coupled, the DC voltage level of the input pair of the Op Amp equals to the common mode voltage V_{CM} during normal operations. However, the Op Amp may suffer from a dead-lock state without the start-up circuitry. Suppose the input voltage of

the Op Amp is initially 0. The input pair (M_{n1} and M_{n2}) of the Op Amp is hence turned off. This causes the output voltages of the 1st and 2nd stages to be close to V_{DD} and 0 respectively. Although V_{CMFB} is pulled to V_{DD} hence turning off the PFETs of M_{p1} and M_{p2}, the other two PFETs of M_{p3} and M_{p4} are always on. Therefore the output voltage of the 1st stage is stuck at V_{DD}, and the output voltage of the 2nd stage is fixed at 0, causing the dead-lock state.

To solve the problem, a start-up circuit is added. A small size inverter (M_{p7} and M_{n3}) is used to sense the output voltage of the Op Amp. The NFET and PFET sizes of the inverter are chosen to be 0.6µm/2µm and 0.3µm/2µm respectively. As the NFET is 3 times wider than the PFET, and NFET has intrinsically stronger drivability, the trip voltage of the inverter is low. When the Op Amp enters the dead-lock state, the inverter (M_{p7} and M_{n3}) outputs '1' and hence turns on the two PFETs of M_{p5} and M_{p6}. These two transistors are connected to the input pair of the transistor, and pull the input voltage up, hence activating the 1st stage. After starting up, the common mode voltage of the Op Amp (V_{OCM}) is close to $V_{CM}=V_{DD}/2$. The inverter outputs zero and hence turns off the start-up circuitry.

The simulated open-loop gain and PM of the Op Amp is shown in Fig. 5.19. With 500 fF output loading capacitance at each output node, the GBW of the Op Amp is 100 MHz and the PM is 53º. To check the start-up process, the Op Amp is incorporated in the VGA circuit in Fig. 5.16(b). The initial conditions of the Op Amp's input and output voltages are all set to zero. Sinusoidal signals with amplitude of 10 mV and frequency of 5 MHz are used as the input stimuli of the VGA. In Fig. 5.20 (a), the start-up circuitry pulls the DC input voltage up, and the Op Amp enters normal operation mode. After that, the start-up circuit is deactivated. For the purpose of comparison, the start-up circuitry is omitted and the transient response is shown in 5.20 (b). The input and output voltages of the Op Amp are stuck at the dead-lock state close to 0. Therefore the start-up circuitry is essential for proper operation of the Op Amp.

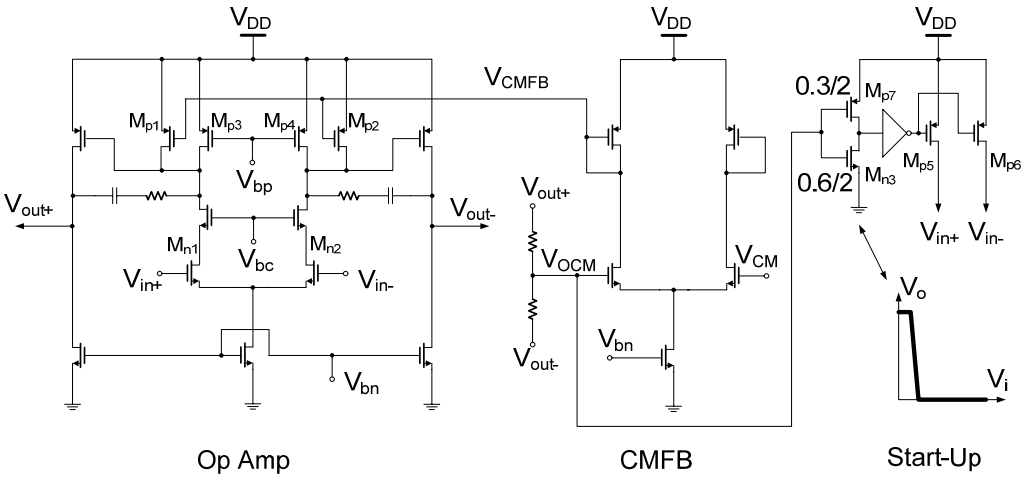


Figure 5.18. The schematic of the Op Amp.

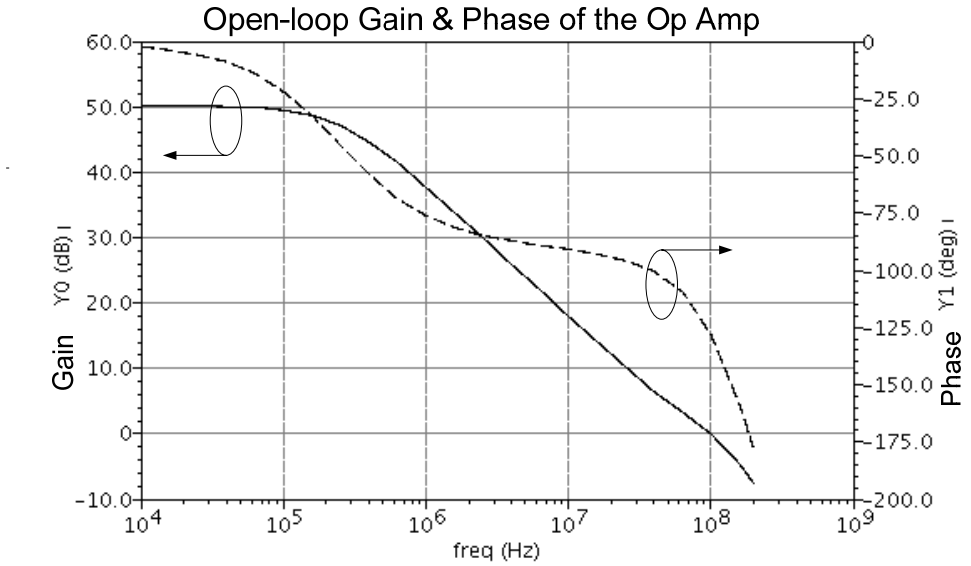


Figure 5.19. The Open-loop gain and phase of the Op Amp with 500 fF loading capacitance. The simulated GBW and PM are 100 MHz and 53º respectively.

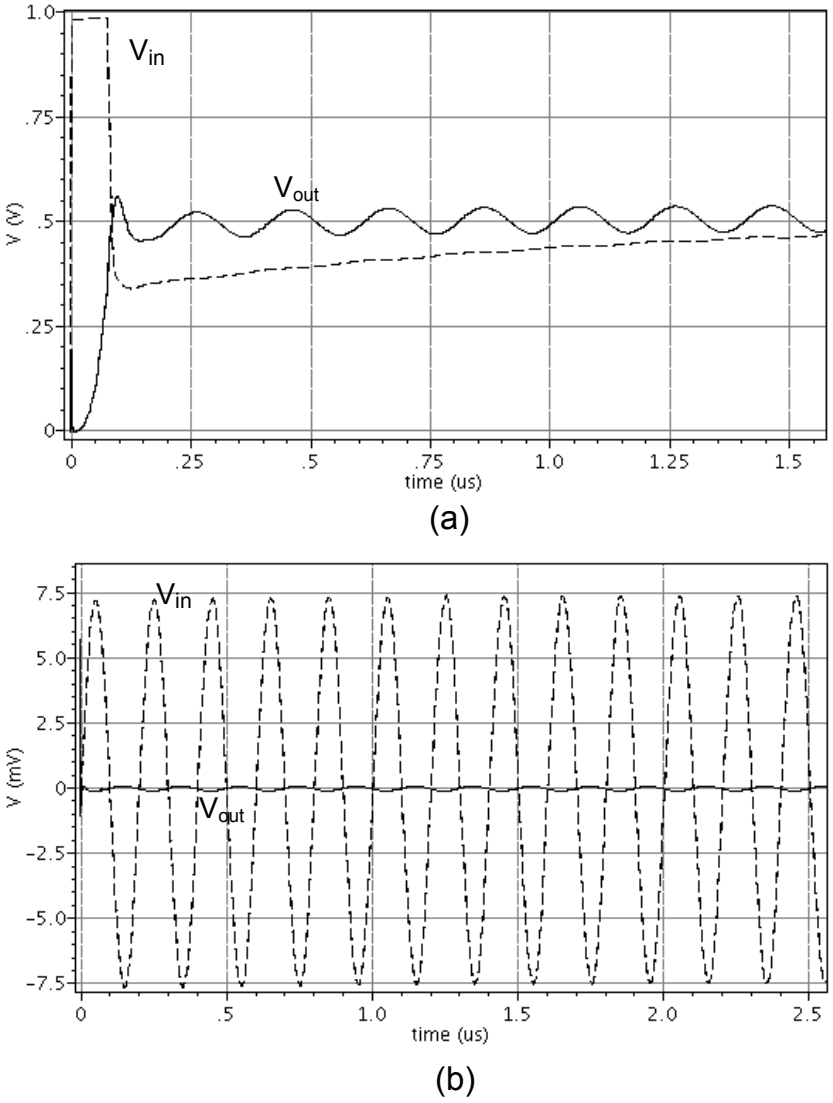


Figure 5.20. The transient response of the Op Amp connected as VGA. The initial conditions of the Op Amp are set to be:$V_{in}(0)=V_{out}(0)=0$ Volt. The Op Amp is configured (a). with start-up circuitry; (b). without start-up circuitry.

5.2.8. Output Buffer

The probes of the testing instruments usually have a loading resistance of 1 MΩ and a capacitance of about 18 pF connected in parallel [84]. For the two-stage Op Amp with Miller compensation in Fig. 5.18, the dominant pole should be located at the output node of the 1st stage. If this Op Amp is used to drive the large capacitance (18 pF) of the testing instrument

directly, the pole at the output node (2nd stage) is pushed forward to lower frequency, largely degrading the GBW and PM. The simulation indicates that the GBW and PM of the Op Amp in Fig 5.18 drop to 17 MHz and 20º respectively with 18 pF output loading capacitance. Therefore the Op Amp may become unstable if it is configured in a feedback loop. To solve this problem, an output buffer is added. It consists of a single stage Op Amp with resistive feedback (R_{11}~R_{22}), as shown in the following figure. R_{b1} and R_{b2} are two large resistors which serve as CMFB. The single stage structure guarantees stability even with large load capacitances. The closed-loop gain of the buffer is about 4 dB at the central frequency of 5 MHz with the instrument loadings of 1 MΩ resistance and 18 pF capacitance connected in parallel.

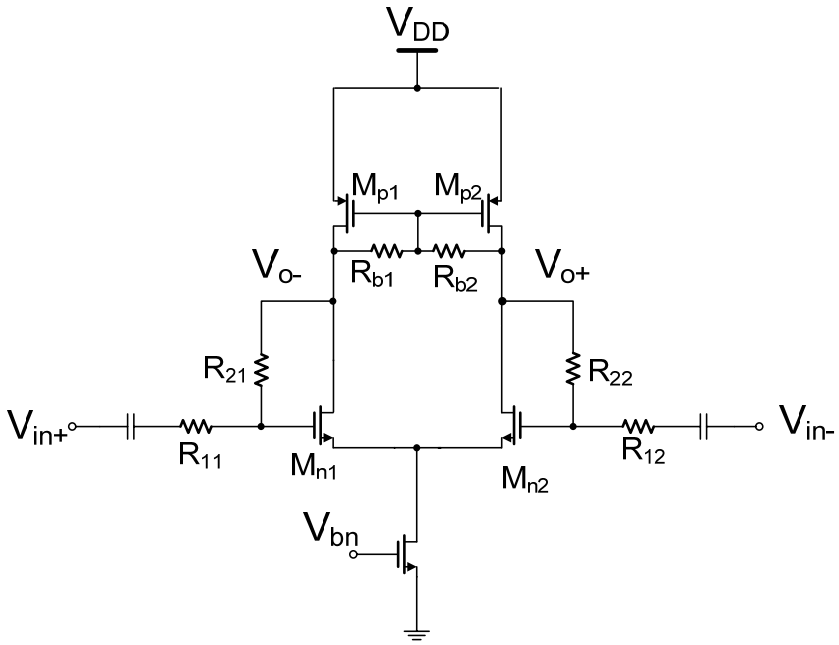


Figure 5.21. The schematic of the output buffer.

5.3. OOK RX Design

The OOK RX aims at low power consumption. The demodulation is realized through ED. The simplified block diagram of the OOK RX is shown in Fig. 5.22. A simple common

source (CS) amplifier serves as the LNA for OOK RX. It is followed by a mixer which converts the RF signal to IF (5 MHz). The VGA, signal selection filter and ED are realized in the IF domain instead of RF to save power.

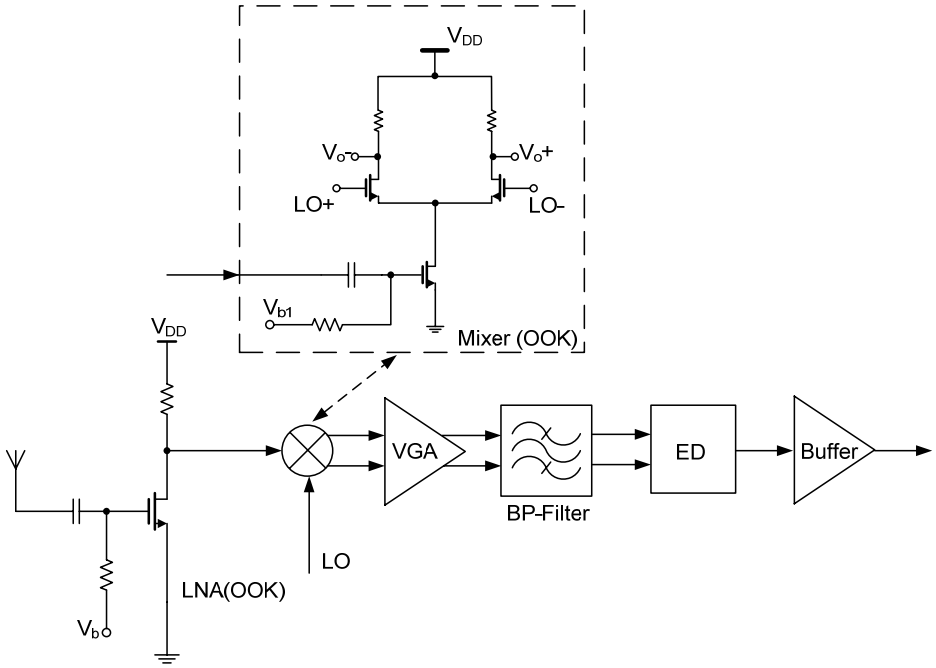


Figure 5.22. The block diagram of the OOK RX.

5.3.1. RFFE of the OOK RX

The antenna port is co-shared with the BPSK RX. The input impedance of the LNA for the OOK RX is not matched to 50 Ω. A simple CS amplifier serves as the LNA for its simplicity. Single balanced mixer with resistive loading down-converts the signal into IF. With 1-V supply voltage, the LNA and mixer consume 150 μW and 70 μW respectively. The voltage gain of the LNA is 4 dB and the conversion gain of the mixer is 18 dB, resulting in a total gain of the RFFE about 22 dB. The simulated NF of the combined LNA and mixer is 21 dB.

5.3.2. VGA for OOK RX

The VGA of the OOK RX consists of two types of gain cells as shown in the following figure.

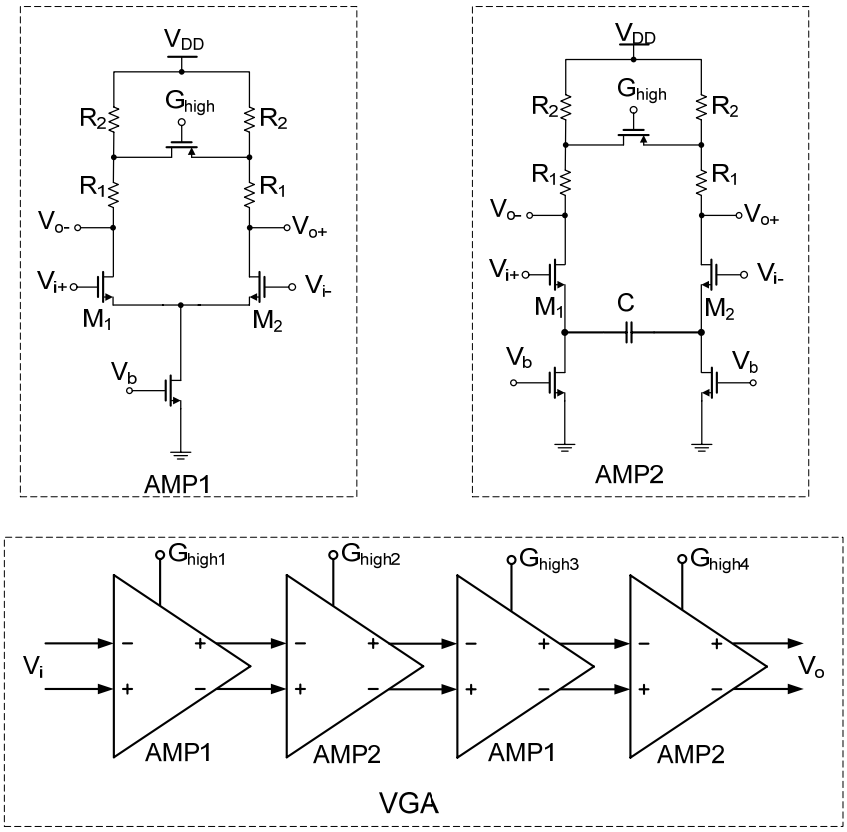


Figure 5.23. The schematic of the VGA for OOK RX.

The first type gain cell (AMP1) is simply the CS differential pair with resistive loading. The gain control is realized by the PFET. When the gain control signal 'G_{high}' is '1', the higher gain of the amplifier can be approximated by:

$$G_h \approx g_m \left(R_1 + R_2 \right), \tag{5.15}$$

where g_m is the transconductance of the input transistor. When 'G_{high}' is '0', the PFET is on and the lower gain of the amplifier is:

$$G_l \approx g_m R_1 . \tag{5.16}$$

The simulated gain tuning step is about 11 dB.

The second type gain cell (AMP2) is similar to AMP1. The tail current is evenly separated into two paths which are connected through a capacitor (C) [50, 56]. At the signal frequency (IF=5MHz), the capacitor creates a short circuit. Therefore its gain is roughly the same with AMP1 as in Eq. (5.23) and (5.24). At lower frequencies near DC, the capacitor creates an open circuit. And the amplifier becomes a source degeneration circuitry which has much lower gain. As a result, the AMP2 serves as a HP filter. The advantage of this structure is the relatively compact circuitry. Only one capacitance is required to create a differential HP filter. No additional resistors are required as in the RC based HP filter. The quantitative analysis of the AMP2 is given below.

The half circuitry of the amplifier is shown in the following figure. The resistance r_o stands for the drain resistance of the tail current transistor.

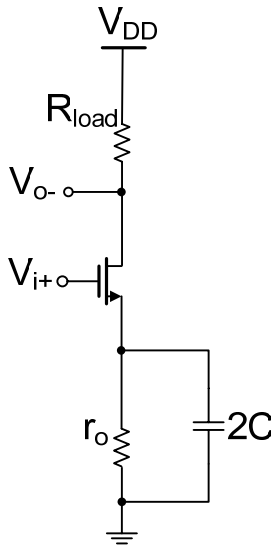


Figure 5.24. Half circuit of the AMP2.

The small signal gain of the above stage can be expressed by:

$$G = \frac{R_{load}}{1/g_m + r_o // \dfrac{1}{2Cs}} = \frac{\dfrac{R_{load}}{r_o}\left(1 + 2r_o Cs\right)}{1 + \dfrac{1}{g_m r_o} + \dfrac{2Cs}{g_m}} \tag{5.17}$$

As the term of '$g_m r_o$' is large, the gain expression in the above equation can be approximated by:

$$G \approx \frac{\frac{R_{load}}{r_o}}{1+\frac{2Cs}{g_m}} + \left(R_{load} g_m\right) \cdot \frac{2Cs / g_m}{1+2Cs / g_m}. \tag{5.18}$$

It can be seen that the gain can be expressed by the summation of two terms in the above equation. By choosing $R_{load}/r_o<<1$, the gain is then dominated by the second term, which implies a HP filter. As expected, the pass-band gain is still determined by the product of the transconductance and the output loading impedance ($R_{load}g_m$). The cut-off frequency of the HP filter is given by $g_m/(2Cs)$. The minimum gain of the stage is determined by the first term of Eq. (5.18), which equals to R_{load}/r_o. This circuitry combines the HP filter with the amplification stage, and therefore simplifies the circuit complexity. It also prevents the accumulation of offset voltages of the amplifiers. The capacitance for AMP2 is chosen to be 6 pF, and the DC current of each amplification stage is set to be around 6 μA. The simulated -3dB transition frequency of the HP filter is about 830 kHz.

It should be noted that for the circuitry of AMP1 and AMP2, a pole is created by the output resistance and the total capacitance at the output nodes. Therefore these two amplifiers are inherently LP filters. In the high gain mode, the LP cutoff frequency is approximately 10 MHz.

5.3.3. BP Filter

The BP filter in Fig. 5.22 is implemented by the same circuitry architecture as AMP2. The only difference is that an output loading capacitance is added to reduce the bandwidth of the filter as shown in the following figure, approximately creating a bi-quad BP filter. The simulated AC response of the BP filter is plotted in Fig. 5.26. The capacitance (C) is chosen

to be 1.2 pF, and the DC current of the filter is 6μA. It can be seen that the gain peaks around 5 MHz. As predicted by Eq. (5.18), the gain does not drop to minus infinity near DC. The difference between the peak and the gain near DC is about 33 dB, which provides adequate suppression for the low frequency signals.

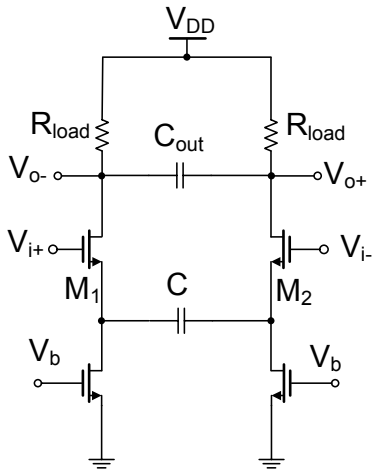


Figure 5.25. The circuitry of the BP filter.

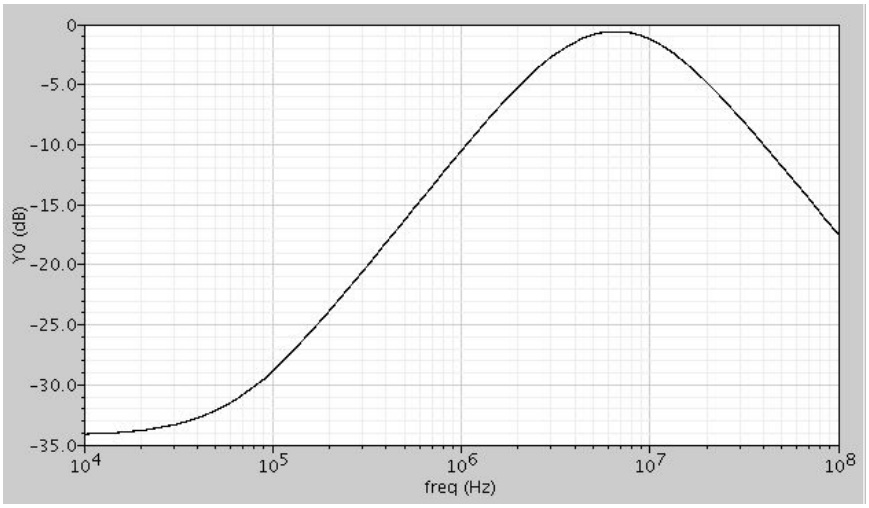


Figure 5.26. Simulated AC response of the BP filter.

5.3.4. Envelope Detector (ED)

The ED module is realized by a half-wave rectifier followed by a LP filter, as shown in the following figure. Near the equilibrium point, the currents through the PFETs of M_2 and M_3 are quite small. The output voltage is thus close to 0. When the swing of the input voltage

increases, more currents flow into M_2 and M_3. If the input voltage difference exceeds the trip point voltage of $\sqrt{\frac{2I_b}{\mu C_{ox} W / L}}$ defined by the input pair and biasing current, the input pair performs complete current switching [47]. During the half cycle when $V_{i+}>V_{i-}$, M_1 is turned off, and all the biasing current flows into M_2. M_3 mirrors the current through M_2, and drives the passive LP filter formed by R and C. The cut-off frequency of the passive RC filter is set to be close to 300 KHz, which is three times of the OOK data-rate. This guarantees the OOK waveform is not largely distorted and the IF components can be effectively suppressed. A unity gain buffer is need after the ED which drives the large capacitances from the output pad and testing instruments.

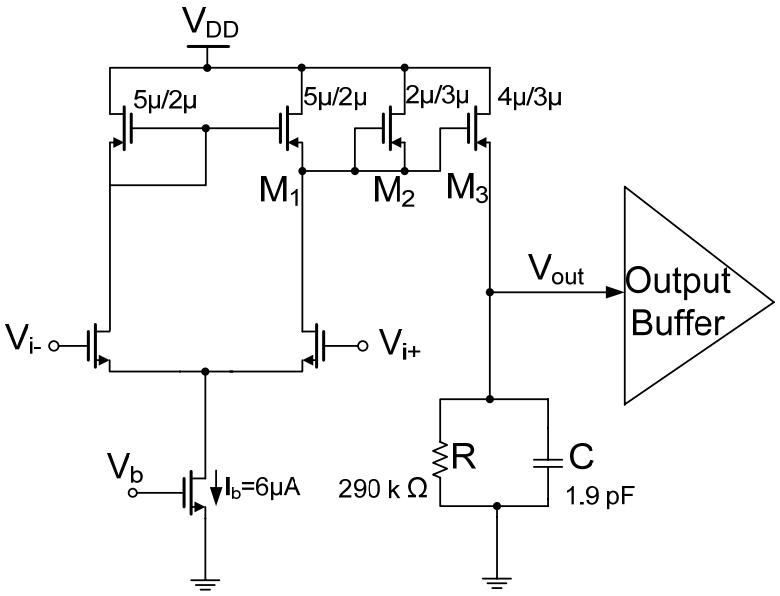


Figure 5.27. The Envelope Detector Circuitry

5.4. VCO and PLL Design

The VCO is for LO signal generation. The PLL locks the VCO and stabilize the output frequency. The PLL and the VCO form a complete frequency synthesizer. The PLL is enabled for the BPSK/OOK TX and the BPSK RX. The block diagram of the PLL based

frequency synthesizer is shown in the following figure. The integer-*N* architecture is adopted for the PLL to simplify the circuit design and to achieve low-power consumption. The reference frequency of the PLL is chosen to be 5 MHz which is generated by a crystal oscillator. The detailed circuit design for the key building blocks of the frequency synthesizer is introduced below.

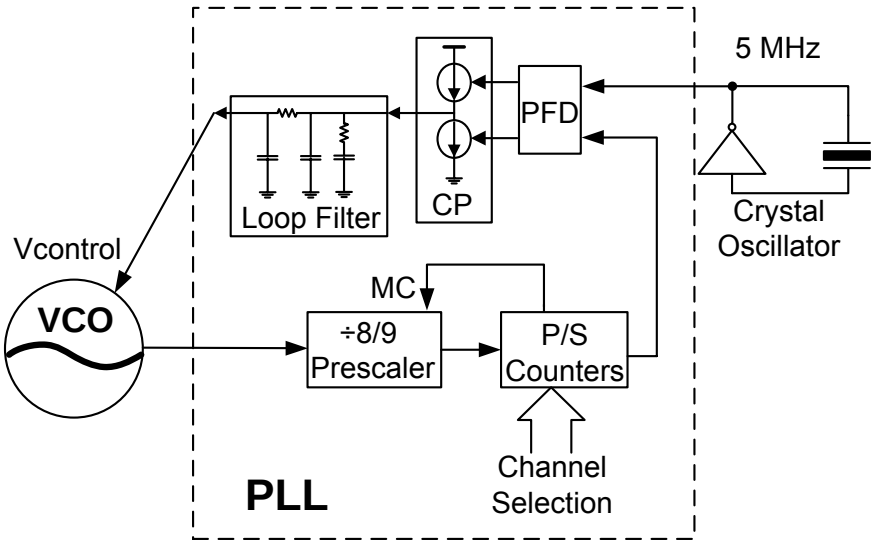
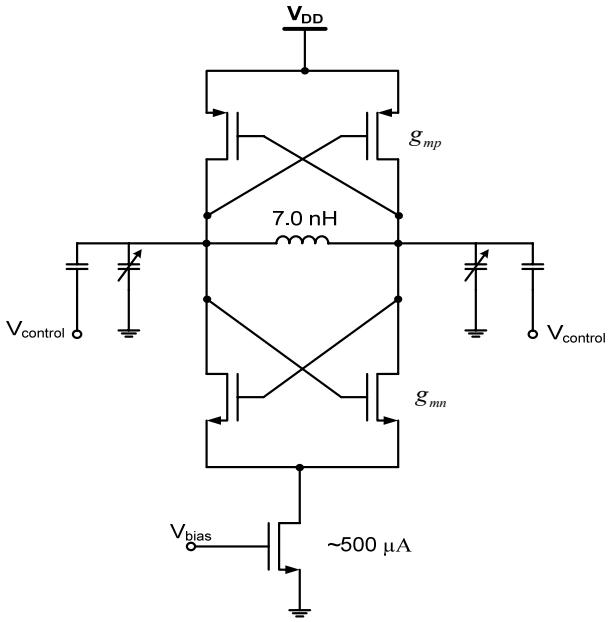


Figure 5.28. The block diagram of the PLL frequency synthesizer.

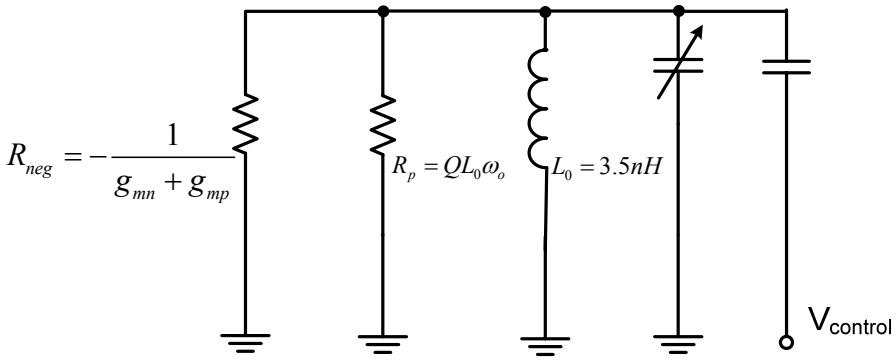
5.4.1. VCO Design

The VCO is designed to be LC negative-Gm topology incorporating both the NMOS and PMOS cross-coupled pairs, as shown in Fig. 5.29(a). The tail current (I_a) is chosen to be around 500 μA to save power. A high-Q (≥15) differential inductor is employed for the LC-resonator tank. The differential inductance is chosen to be 7 nH implying an inductance of 3.5nH for the single-ended half-circuit of the VCO (L_0), as shown in Fig. 5.29(b). The capacitance of the VCO is composed of two parts, the digitally controlled capacitance bank and the varactor. The digitally controlled capacitance bank is designed to be 11-bits tunable, including 4 coarse and 7 fine tuning bits. The 4 coarse tuning bits are for correction of the VCO frequencies due to the process variations. The coarse tuning bits provide a frequency

tuning step of 30 MHz. The 7 fine tuning bits are for frequency calibration of the DCO, which will be elaborated later. The varactor is used for continuous frequency tuning in PLL. The gain of the VCO (K_{VCO}) is designed to be about 100 MHz/V (in Fig. 5.29)



(a)



(b)

Figure 5.29. Schematic and Circuit Model of the VCO. (a) Detailed schematic of the LC negative-g_m VCO. (b) Equivalent single-ended half-circuit model of the VCO.

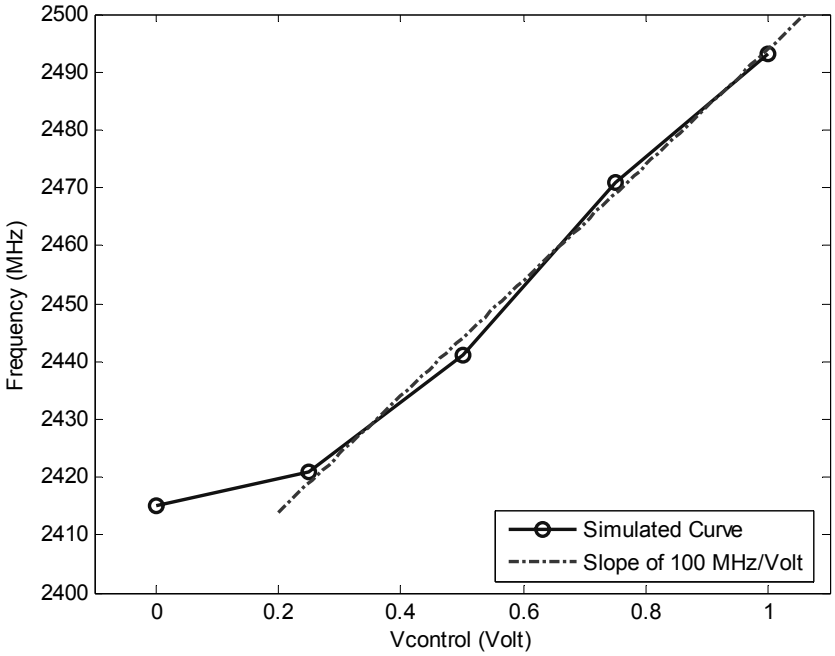


Figure 5.30. The simulated *f-v* characteristic curve of the VCO. The coarse frequency tuning bits are set to "1000".

The voltage amplitude of the VCO can be estimated by assuming abrupt switching of the cross-coupled transistor pairs. Then the currents injected into the LC-tank become square waves. The single-ended output amplitude of the VCO is therefore given by:

$$V_{Amplitude} = \frac{4}{\pi} I_a R_p , \tag{5.19}$$

where R_p is the parallel equivalent resistance of the inductor, and it is given by:

$$R_p = L_0 \omega_0 Q . \tag{5.20}$$

The variable Q in the above equation stands for the quality factor of the inductor, and ω_0 depicts the angular frequency of the oscillator. Simulation results indicate that the Q of the inductor is about 15. Then the estimated amplitude of the VCO output is about 0.5-V with a tail current of I_a=500μA. In real CMOS circuits, the transistors are not ideal switches. The currents flowing into the LC-tank are therefore not ideal square waves. Furthermore, the

parasitic serial resistances from the varactor and the gates of the transistors also degenerate the overall Q of the LC-tank. Due to these two reasons, the actual amplitude of the VCO is smaller than the ideal prediction by Eq. (5.19). Simulation results indicate about 0.35-V single-ended amplitude with I_a=500μA. This voltage swing is large enough for the proper operation of the down conversion mixer in the receiver. The simulated phase noise of the VCO is -110 dBc/Hz at 1 MHz offset, which is much better than the phase noise requirement of -96 dBc/Hz defined in the system design chapter. Therefore the influences from the phase noise are negligible for BPSK modulation and demodulation.

Although further power reduction may be possible by decreasing the bias current and increasing the inductance value (to maintain output voltage swing), this may bring with some issues. The inductance value of 7 nH in this design (equivalent to 3.5 nH in the single-ended half circuitry) resonates with about 1.2 pF capacitance in the 2.4 GHz band. This capacitance value is large enough to include all the tuning capacitances, mixer input loading and parasitic. Larger inductance values cause the corresponding resonant capacitance to decrease, which may possibly become too small to accommodate all the capacitances mentioned above. Larger inductor also has lower Q and occupies more area. Therefore the choices on inductance and biasing current in this VCO design achieve good balances between low-power consumption and adequate design margins of resonant capacitance.

5.4.2. Frequency Divider and PFD

The frequency divider of the PLL is composed of the dual-modulus prescaler and the programmable pulse-swallow counters [47].

The prescaler is the key module of the PLL frequency synthesizer. As the prescaler works at the RF frequency (2.4-GHz in this design), this module is power hungry. Although current

mode logic (CML) circuits are suitable for high frequency applications [85], they are not power efficient for the reason that constant current biasing and differential circuitries are required. In this design, the prescaler is implemented by true single-phase clocked (TSPC) logic circuits [85], which allows single-end operations and hence helps to reduce the power consumption.

The detailed circuit of the prescaler is shown in Fig. 5.31. The circuit works in asynchronous manner as proposed in [86]. The operation principle is briefly described below. The prescaler is designed to be dual-modulus with frequency divisors of 8 and 9. The three DFFs of D1, D2, and D3 form the frequency division part, and they divide the input frequency by 8 if "MC" is set to 0. If "MC" is set to 1, then the additional DFF D4 outputs 1 for the state of (Q3, Q2, Q1)=(1, 1, 1). One incoming clock pulse is thus disabled for the PFET M_{P1} is turned off. The timing diagram for dividing-by-9 operation is shown in Fig. 5.31. It can be seen that only D1 and D4 operate at the RF frequency of 2.4 GHz. D2 and D3 works at about 1.2 and 0.6 GHz respectively. The DFFs of D1 to D3 toggle their outputs for every incoming clock. D4 only toggles once for 9 incoming clocks, when "MC" is set to 1. It does not toggle when the "MC" is set to 0 for the dividing-by-8 operation. This circuit minimizes the toggle rates and hence reduces the dynamic power consumptions.

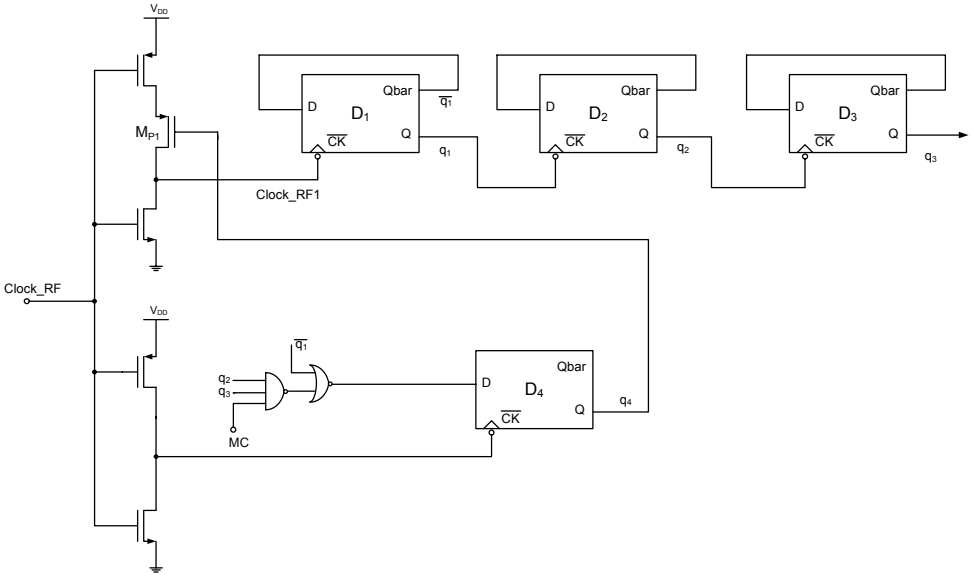


Figure 5.31. The schematic of the 8/9 prescaler. The circuit divides the input frequency by 9 when MC=1, and divides the frequency by 8 when MC=0.

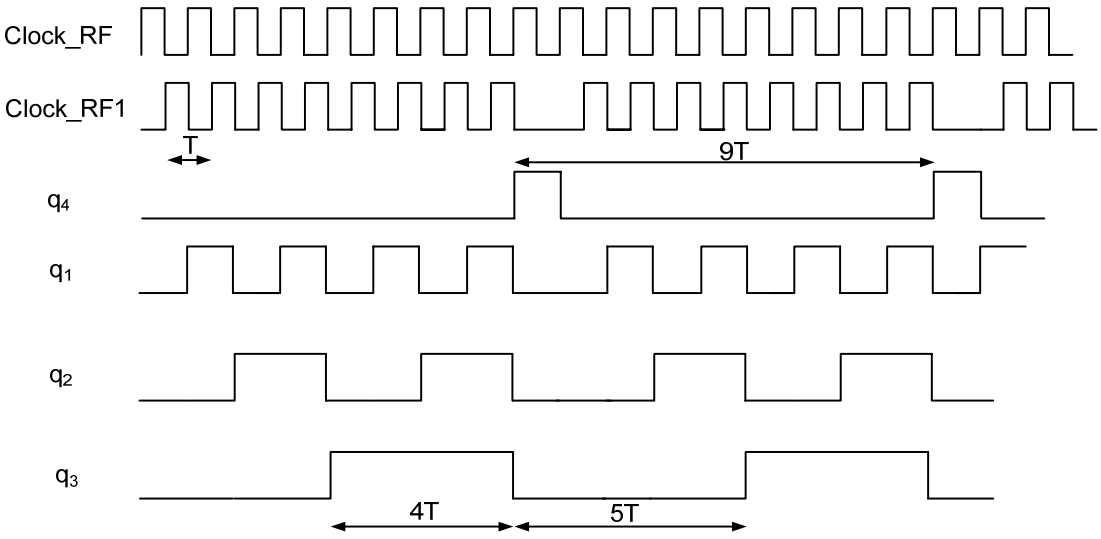


Figure 5.32. The timing diagram of the prescaler when MC=1 and the prescaler divides the input frequency by 9.

The circuitry of the TSPC DFFs is shown in Fig. 5.33 [85]. The TSPC DFF circuitry utilizes the parasitic capacitances to store binary information. The operation of this DFF is described below. When the clock (CK) is high, the input signal 'D' is inverted and stored on the node 'X', the node 'Y' is discharged to 0, and 'Qbar' maintains its original state. When the clock toggles from high to low, the previous stored binary state on node 'X' is propagated to

'Qbar'. When the clock is high, the input signal 'D' is not transparent to 'Y', and therefore cannot propagate to the output. As a result, 'Qbar' is latched to the inversed signal of 'D' at each falling edge of the clock. The DFF therefore toggles at negative edges of the input clock. The circuit of the TSPC DFF is comprised of only 5 NFETs and 6 PFETs, which is simple to implement and works efficiently at RF frequency.

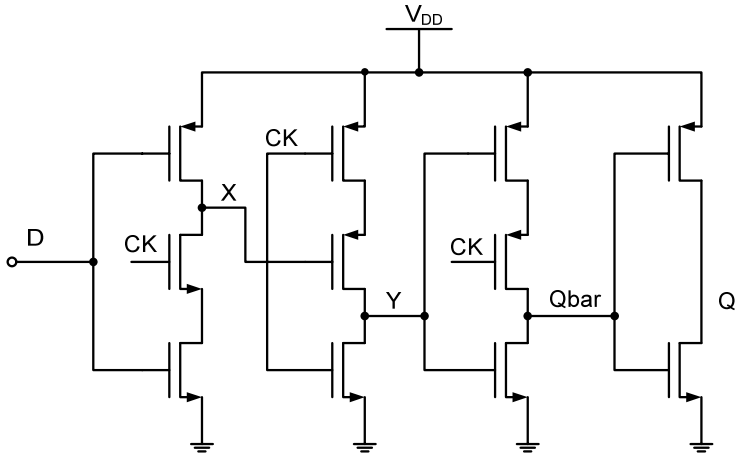
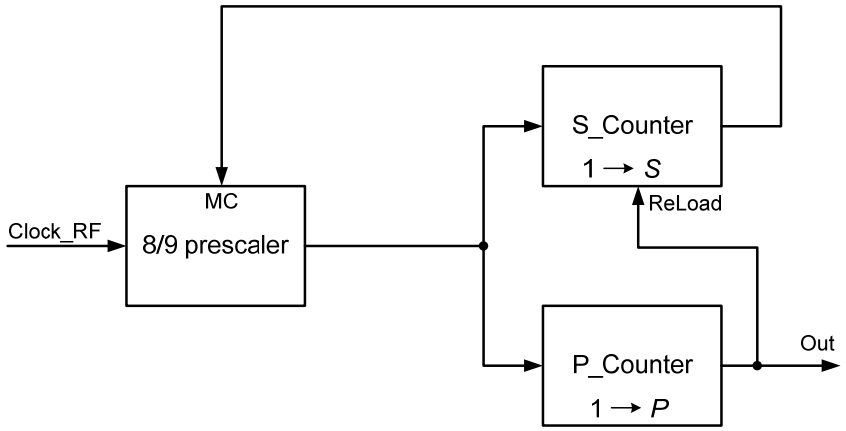


Figure 5.33. The schematic of the TSPC DFF for the prescaler.

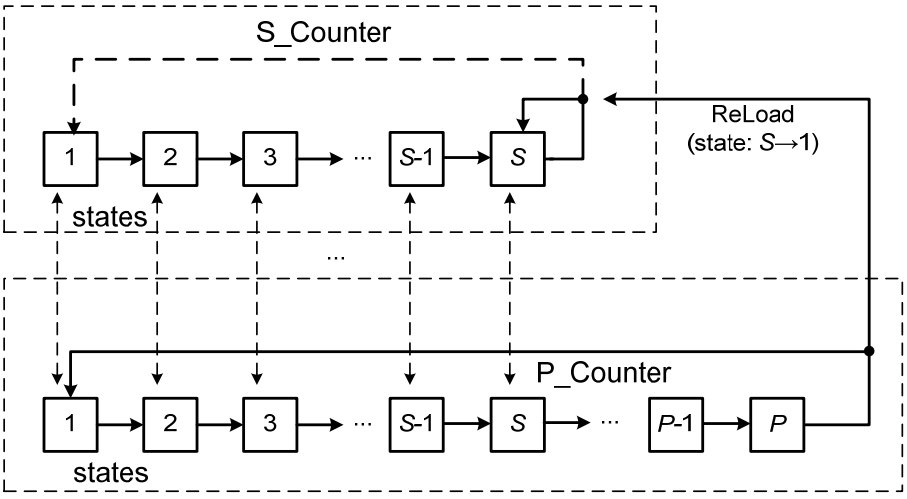
The programmable pulse-swallow counters work with the prescaler to fulfill the frequency division function [47], as shown in Fig. 5.34. The P-Counter contains *P* number of consecutive states of (1, 2, 3, …, *P*), and it is automatically reloaded to the state '1' after the state '*P*' is reached. The S-Counter contains *S* number of consecutive states of (1, 2, 3, …, *S*), where *S*<*P*. When the S-Counter reaches the final state '*S*', its state is locked to to '*S*' until it receives the 'Reload' signal from the P-Counter and reset to '1'. The output of the S-Counter controls the dual-modulus prescaler. In each complete cycle of the whole system, the counters perform 'dividing by *N*+1' for *S* times followed by 'dividing by *N*' for '*P*-*S'* times. The total dividing ratio of the counter is therefore given by:

$$Dv = (N+1)S + N(P-S) = NP + S\,. \tag{5.21}$$

By changing the division factor of the S-Counter, the total dividing factor can be changed by a step of 1. In this design, *P* is set to be 59, and *S* is 5-bits programmable from 0 to 31. Therefore the overall dividing ratio (*Dv*) is from 472 to 503. With a reference frequency of 5 MHz, the PLL synthesizer can cover 2360 to 2515 MHz which is adequate for the 2.4 GHz ISM band.



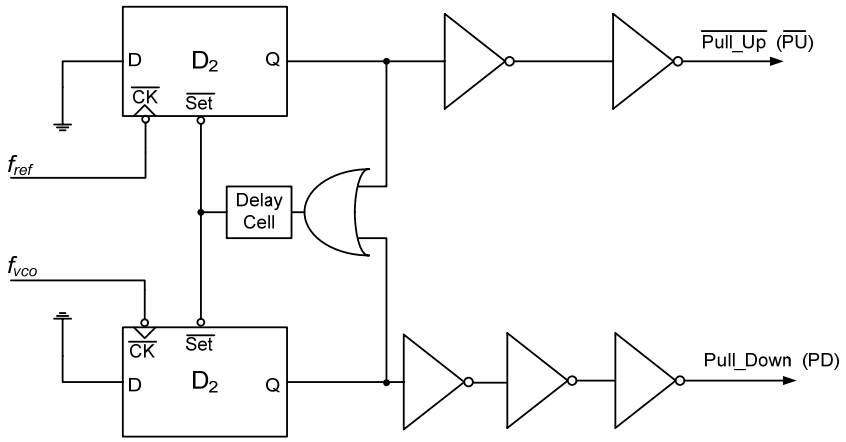
(a)



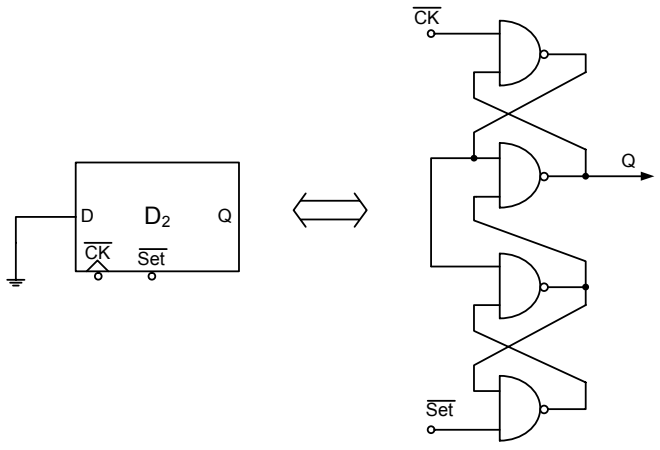
(b)

Figure 5.34. The pulse-swallow counter for the PLL. (a) The block diagram of the pulse-swallow counter. (b) The state transition diagram of the 'P' and 'S' counters.

The phase/frequency detector (PFD) circuits are shown in Fig. 5.35. The DFFs are triggered at negative edges of the incoming clocks. If the outputs of the DFF equals to '0', the 'Pull Up' or 'Pull Down' function is activated. When both DFFs output '0', they are set to '1' through the OR gate. A delay cell is added into the 'set' path to ensure enough time for activating the charge pump, and therefore eliminate the 'dead zone' effect [47, 62]. As the inputs of the DFFs for the PFD are fixed to '0', the circuitry of the DFF can be simplified. As shown in Fig. 5.35(b), the DFF can be implemented by 4 NAND gates.



(a)



(b)

Figure 5.35. The circuits of the PFD. (a) Block diagram of the PFD. (b) Circuits of the DFF for the PFD.

5.4.3. Charge-Pump Circuit

The charge-pump (CP) is the key module to determine the in-band phase noise and reference spur levels of the PLL. The CP current is selected to be 50 μA to save power. The CP circuit is shown in Fig. 5.36. Ideally the CP is composed of two current sources which are controlled by the pull-up (PU) and pull-down (PD) signals respectively, and the output impedance of the current sources is infinity. However in real circuit implementation, MOSFETs have finite output impedances due to the channel length modulation effect. As a result, the PU and PD currents may be imbalanced which degrades the reference spur performance [47, 62]. To alleviate this problem, the CP is composed of two branches: the output branch and mirror branch. An Op Amp is incorporated to balance the PU and PD currents, as shown in Fig. 5.36(b). The current sources in the mirror branch are always turned on, and the Op Amp forces the output of the mirror branch (Vmirror) to follow the output of the CP (Vout). As the output of the mirror branch is a high impedance node, therefore the PU and PD currents are exactly matched when the steady state is met. The device sizes of the mirror branch are half of the output branch in order to save power. The compensation capacitance (Cc) is added to the output of the Op Amp to ensure stability.

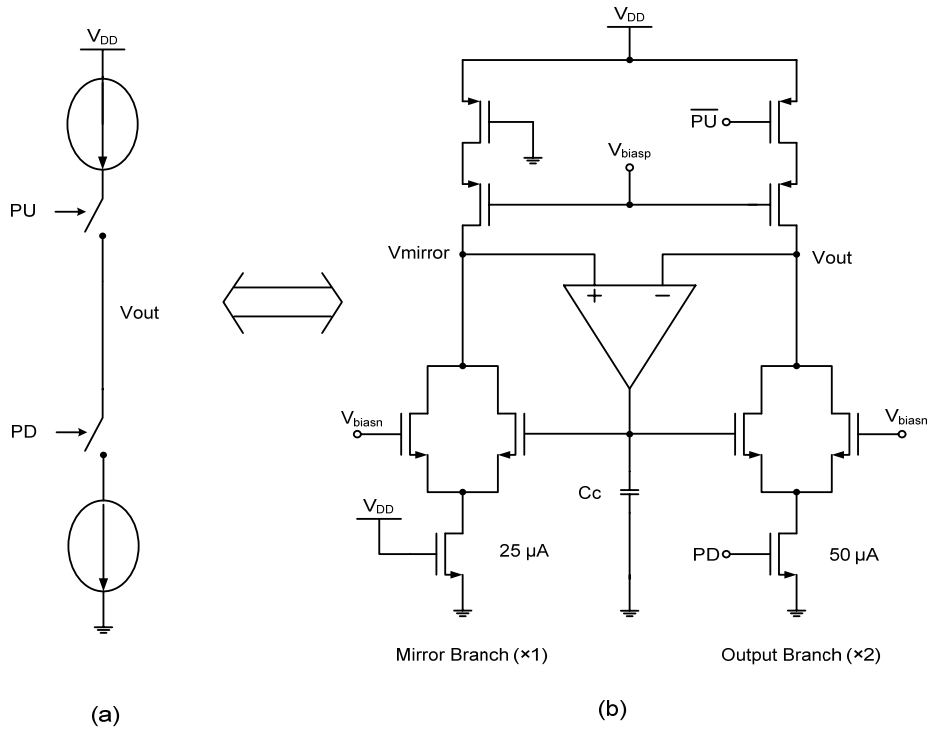


Figure 5.36. The charge-pump schematic. (a).The ideal circuit model. (b) The detailed circuitry of the charge-pump.

5.4.4. Loop filter design

The loop-filter of the PLL is designed to be 3rd order for better suppression of the reference spurs. The circuitry of the loop filter and the component values are shown in Fig. 5.37. The total capacitance of the passive loop filter is smaller than 130 pF and can be implemented fully on-chip. Double-layer metal-insulator-metal (MIM) capacitor is used to save area, and high-resistance poly-silicon resistor is adopted to achieve the relatively high resistance.

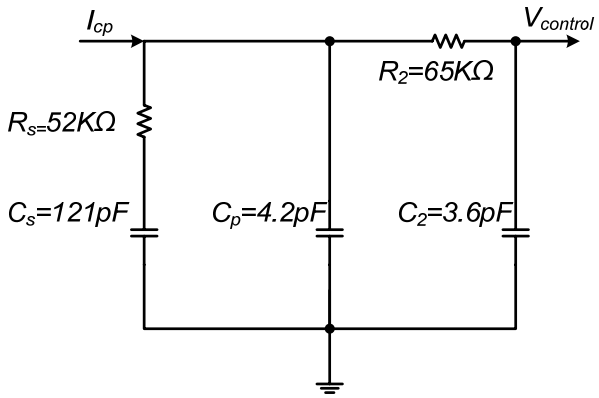


Figure 5.37. The 3rd order loop filter of the PLL.

The component values of the loop filter is determined by the closed-loop transfer function of the PLL as proposed in [87]. For the 3rd order loop as shown in the above figure, the closed-loop transfer function of the PLL becomes 4th order due to the additional pole contributed by the VCO [47]. The closed-loop transfer function (H_{pll}) of the PLL can be depicted by the following equation:

$$H_{pll}(s)=\frac{R_S C_S s+1}{\frac{C_S C_P C_2 R_S R_2}{K_{pll}}s^4+\frac{\left(R_S C_S C_P+R_S C_S C_2+R_2 C_2 C_P+R_2 C_2 C_S\right)}{K_{pll}}s^3+\frac{\left(C_S+C_P+C_2\right)}{K_{pll}}s^2+R_S C_S s+1}. \quad (5.22)$$

The variable K_{pll} is given by:

$$K_{pll}=\frac{I_{cp}K_{vco}}{2\pi N}, \quad (5.23)$$

where I_{CP} is the CP current in ampere, K_{vco} is the gain of the VCO in Rad/Second/Volt, and N stands for the total dividing factor of the PLL. In this design, I_{CP} is 50 μA, K_{vco} is about 630 M-rad/s/Volt (100 MHz/Volt), and N is from 480 to 497 depending on the channel selected. In the loop filter design, the average value of 490 is used as the division factor N. From Eq. (5.22) it can be seen that the PLL contains four poles. The closed loop transfer function is

chosen by placing the first two dominant poles at 60 kHz, and the other two poles at 170 kHz and 1700 kHz. Then the closed-loop transfer function of the PLL satisfies:

$$H_{pll}(s) = \frac{1 + s(\frac{1}{\pi\, pole_0} + \frac{1}{2\pi\, pole_1} + \frac{1}{2\pi\, pole_2})}{(1 + \frac{s}{2\pi\, pole_0})^2 (1 + \frac{s}{2\pi\, pole_1})(1 + \frac{s}{2\pi\, pole_2})}, \tag{5.24}$$

where $pole_0$, $pole_1$, $pole_2$ equals to 60, 170 and 1700 kHz respectively. By equating Eq. (5.22) and Eq. (5.24), all the component values of the loop filter can be derived by solving the AEs, and the results are shown in Fig. 5.37.

To check stability of the system, phase margin of the PLL is computed. The open-loop transfer function (H_{open}) is used to derive the phase margin. It is related to the closed-loop transfer function (H_{pll}) by the following equation.

$$H_{open} = \frac{H_{pll}}{1 - H_{pll}}. \tag{5.25}$$

Phase margin are obtained by computing the phase difference between H_{open} and 180 degree when $|H_{open}|$=1. With the loop filter defined in Fig. 5.37, the phase margin is about 55 degrees which guarantees stability of the PLL. According to the process design manual, the adopted capacitance and resistance may deviate from their nominal design values by 10% and 20% respectively in the worst case. The phase margin is still above 50 degrees under the worst case process variations, with VCO gain of 100 MHz/Volt. Therefore the loop filter can be implemented on-chip without tuning mechanism.

With all the building blocks, the transient response of the PLL control voltage is obtained by post layout simulation. The dividing factor is set to be 490, corresponding to the output frequency of 2.45 GHz. The VCO control voltage of is shown in the following figure. It can

be seen that the PLL settles in about 30 us. The reference spur is close to -60 dBc according to simulation. The simulated output spectrum of the locked PLL will be given in the next chapter to compare with the measurement results.

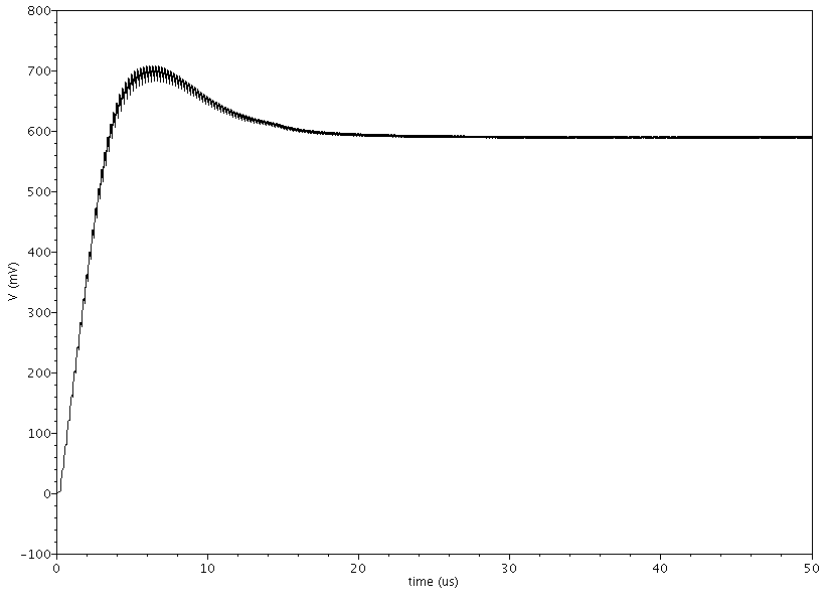


Figure 5.38. The settling transient of the VCO's control voltage by post-layout simulation.

5.5.Frequency Calibration for OOK RX

The PLL is disabled for the OOK RX in order to save power. In this mode, the VCO is reconfigured as a frequency calibrated DCO. The DCO has 4 coarse and 7 fine tuning bits. Automatic frequency calibration is implemented for the 7 fine tuning bits. The LSB frequency deviation is set to be around 700 kHz. The frequency calibration is realized through simple digital counters and SAR control logics.

The timing diagram for frequency calibration is shown in Fig 5.39. As it is difficult and power consuming to design digital counters working under RF frequency, the DCO's

frequency is firstly divided by 8. The prescaler in the PLL is reused here to divide the RF frequency, and the modulus of the prescaler is fixed to 8. The counter is firstly reset to 0. The generated signal then clocks the counter within a fixed time of '$6T$=19.2 μs'. According to the counter outputs, the SAR control logic circuit then determines each fine tuning bit (from MSB to LSB) of the DCO. It takes 25.6 μs to calibrate one bit, and the total calibration time for 7 bits is 179.2 μs seconds. The counter output can be expressed by the following equation:

$$C = floor\left[\frac{6T \cdot f_{RF}}{8}\right] \quad or \quad floor\left[\frac{6T \cdot f_{RF}}{8}\right] + 1, \tag{5.26}$$

where the function $floor(x)$ gives the nearest inter number which is smaller than x. Therefore the frequency error caused by the counter is:

$$\Delta f_{counter} \in \left(-\frac{8}{6T}, \frac{8}{6T}\right). \tag{5.27}$$

By choosing T=3.2 μs, the maximum frequency error due to the counter uncertainty is ±417 kHz. As the LSB of the DCO corresponds to frequency deviation of 700 kHz, the quantization error falls within the range of (-LSB/2, LSB/2), or (-350 kHz, 350 kHz). As a result, the worst case residue frequency error after calibration can be calculated by the following equation:

$$\left|\Delta f_{r\_MAX}\right| = \left|\Delta f_{count\_MAX}\right| + \left|LSB/2\right| = 770kHz\,. \tag{5.28}$$

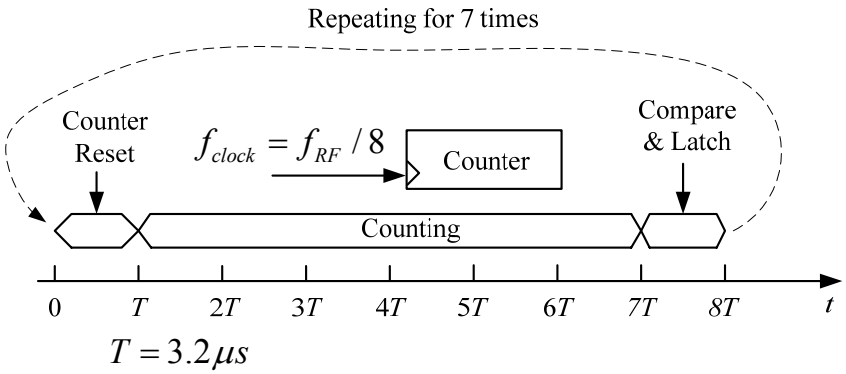


Figure 5.39. The timing diagram for DCO frequency calibration.

For OOK demodulation, the DCO frequency is tuned to either 2.395 or 2.485 GHz. After frequency calibration, the prescaler is turned off to save power. The residue frequency error of the DCO is less than 800 kHz after calibration, which is sufficiently accurate for the OOK demodulation with IF=5MHz. Compared with the locked PLL, this method provides power saving of 1 mW according to simulation.

5.6. Summary of the Transceiver Design

The detailed circuit design of the transceiver is presented in this chapter. The complete transceiver circuit block diagram is summarized in the following figure. The transceiver works in half-duplex manner where the TX and RX are not on for the same time. The same antenna is shared by the TX and RX without off-chip matching network. The Class-E PA and LNA are co-designed by sharing one inductance. The PA works with a supply voltage of 0.5-V and the other parts of the transceiver work with 1-V supply.

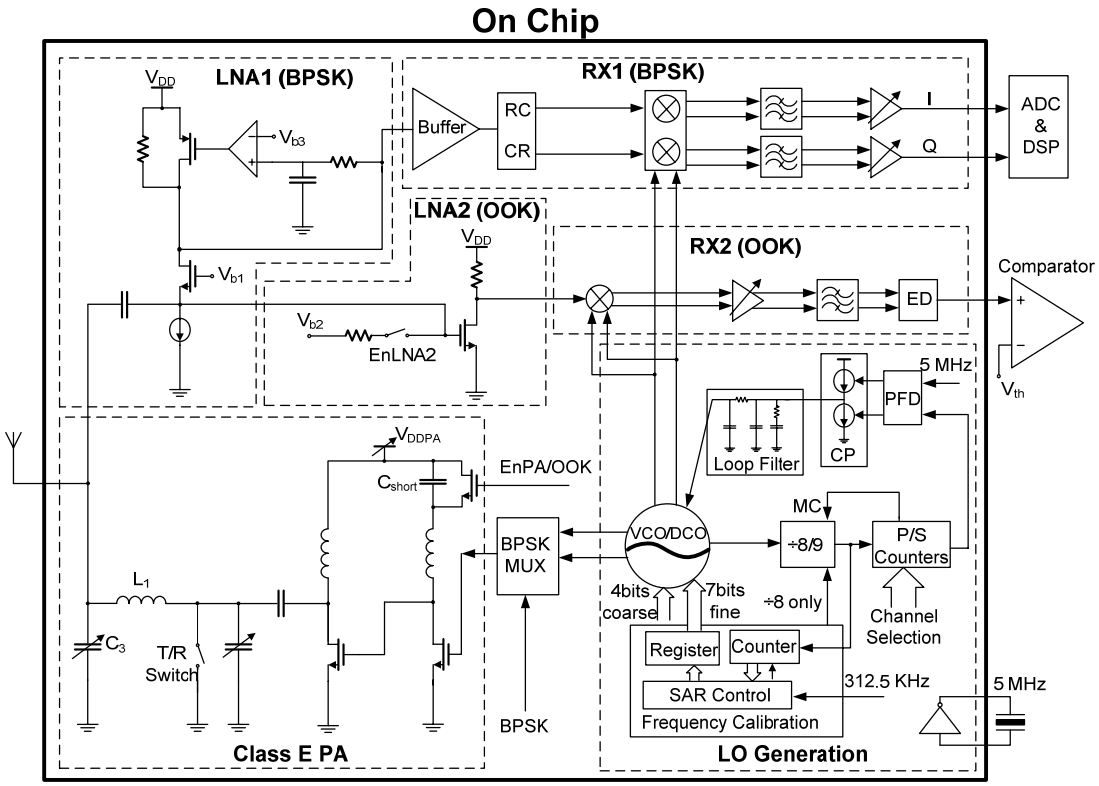


Figure 5.40. The system diagram of the transceiver.

The simulated the efficiency of the PA is 59% while delivering 1.35 mW output power. The VCO consumes minimally 500 μW. The PLL, BPSK MUX, and other auxiliary circuits consume about 1.05 mW. Therefore the total power consumption of the TX about 3.77 mW while delivering 1.35 mW output power.

The BPSK RX (gateway mode) is targeted for good performance. The data-rate of BPSK is 1~10 Mbps. The RFFE (including LNA, LNA Buffer, and mixers) consumes 4.6 mW including biasing circuits. The ABB for BPSK RX consumes 3.2 mW excluding the output buffer. The total gain of the BPSK RX is tunable from 42 to 80 dB. The total power consumption for the BPSK RX including the VCO and PLL is about 9.4 mW. The simulated NF of the BPSK RX is about 12 dB with quadrature mixing.

The OOK RX (sensor mode) is targeted at low-power consumption. The LO in this mode is generated by the calibrated free-running DCO. The total power consumption for the OOK RX mode is about 760 μW excluding the output buffer and the crystal oscillator.

The detailed simulation results of the transceiver are presented in the next chapter together with the measurement results for the purpose of comparison.

CHAPTER 6 MEASUREMENT RESULTS OF THE TRANSCEIVER

6.1.Die Photo and Chip Area

The transceiver is fabricated in 0.13μm CMOS technology. The micrograph of the transceiver is shown in the following figure. The chip size is 2.09mm×1.59mm including the pads. The transceiver supports both the sensor and gateway modes. The additional circuits for the BPSK RX (including the RFFE and ABB) only incur 14% of area penalty.

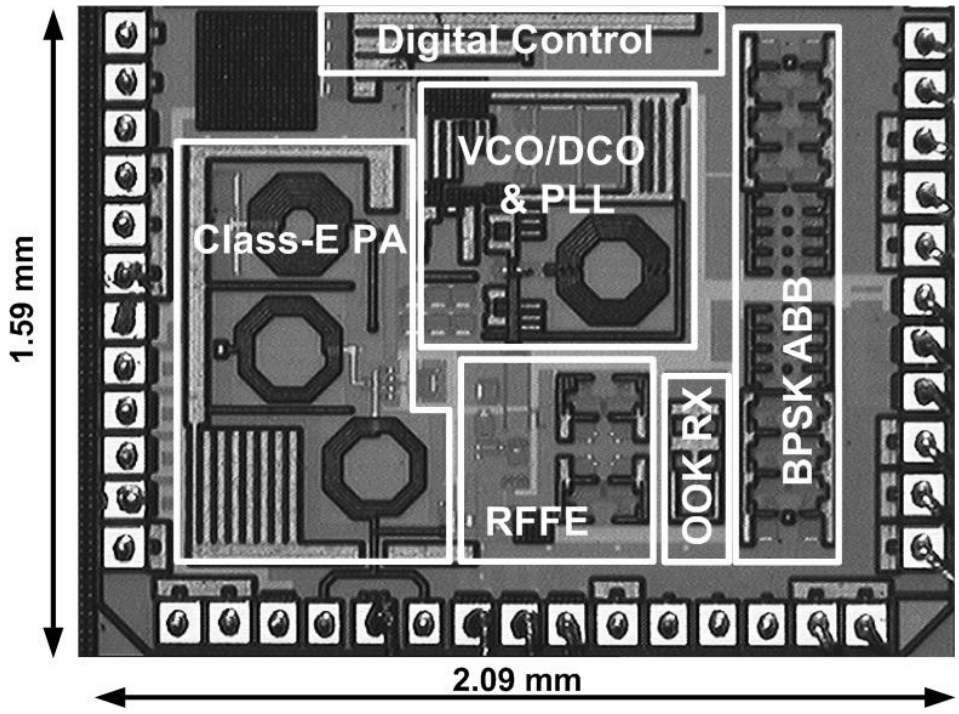


Figure 6.1. The micrograph of the transceiver.

6.2.VCO & PLL Measurement

The PLL is functional and can cover the 2.4 GHz ISM band. The VCO phase noise with locked PLL is shown in Fig. 6.2. The VCO is locked at 2.450 GHz. The measured phase noise at 1 MHz offset is 106.8 dBc/Hz. As expected, the PLL suppresses the noise within the loop filter bandwidth. The achieved phase noise is adequate for BPSK communication as discussed in the system level design. For the purpose of comparison, the simulated free-running VCO is shown in Fig. 6.3. Simulation indicates phase noise of -110 dBc/Hz at 1 MHz offset, which differs from the measurement result by about 3 dB. In simulation, a perfect ground connection is assumed. In actual implementation, the bonding wires cause additional inductance, which is insufficiently modeled during simulation. The PLL modules of change pump and loop filter also contribute additional phase noise. Therefore the measured VCO phase noise at 1 MHz offset is worse than simulation. The measured and simulated power spectra of the VCO with lock PLL are shown in in Fig. 6.4 and Fig. 6.5 respectively. The measured reference spur level is -53.2 dBc, while the simulated reference spur level is -59 dBc. This may be caused by the reference signal feed-through from the supply rails and substrate, which is not included in the simulation. However, the achieved reference spur level in measurement is adequately low for the modulation and demodulation purpose.

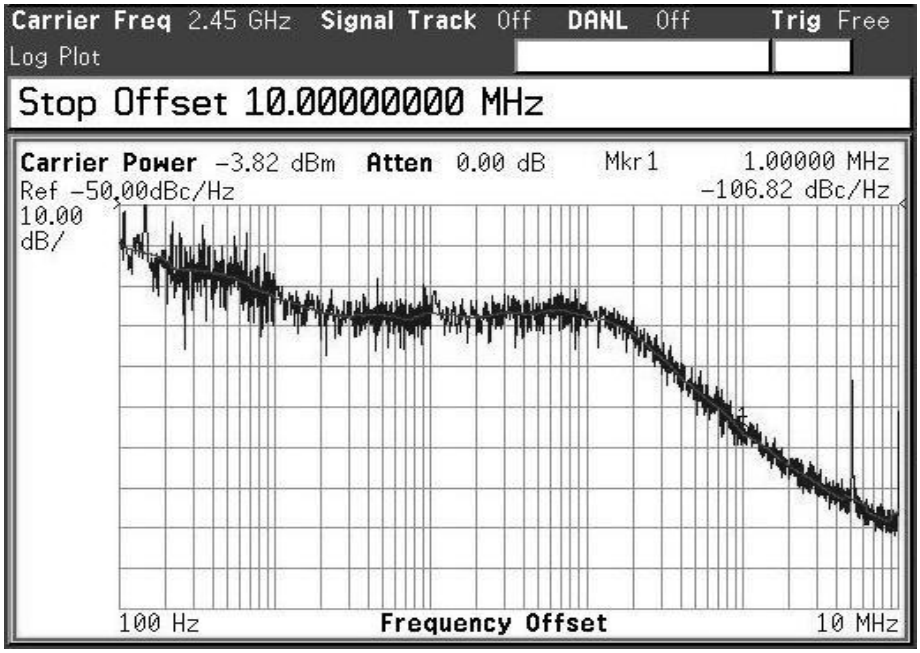


Figure 6.2. Measured phase noise of the VCO with locked PLL at 2.45 GHz.

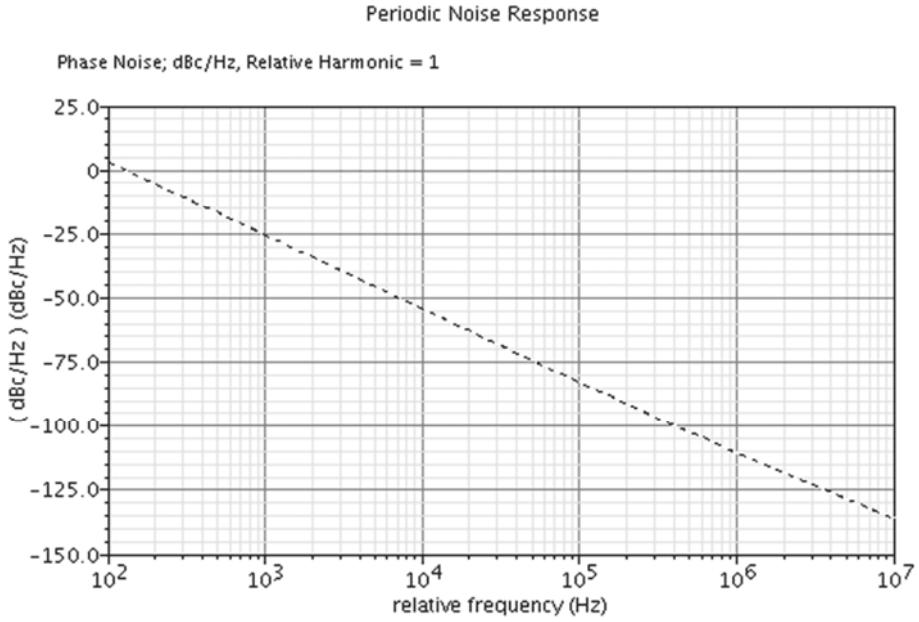


Figure 6.3. Simulated phase noise of the free-running VCO.

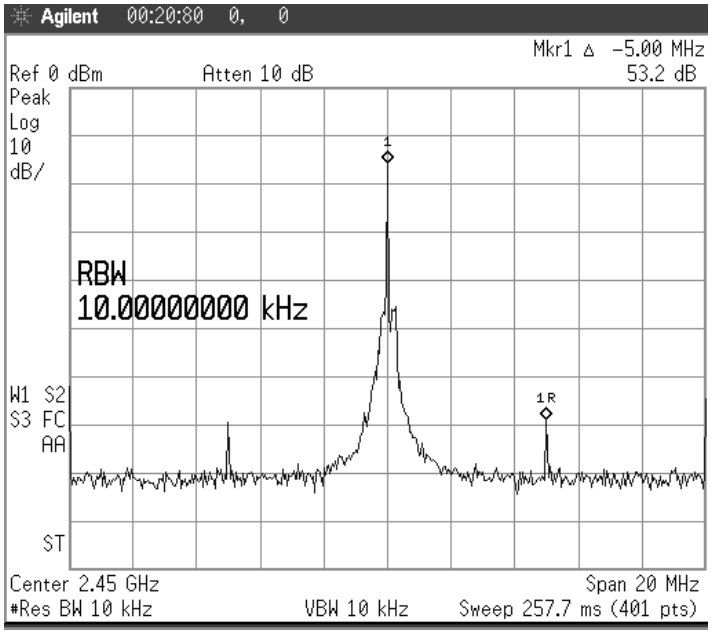


Figure 6.4. The measured power spectrum and reference spur level of the PLL.

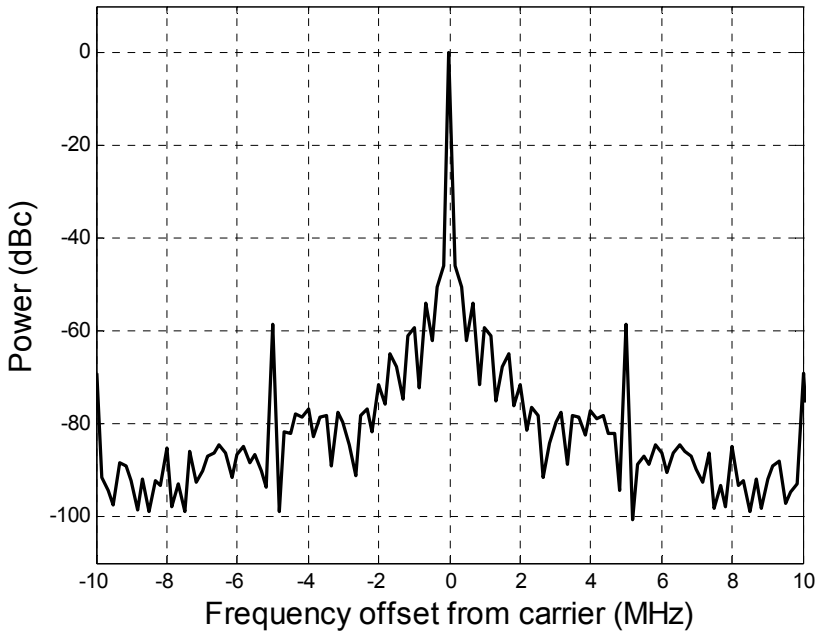


Figure 6.5. Simulated power spectrum of the PLL.

6.3. TX Measurement

The efficiencies of the PA and the BPSK TX are measured at 2.45 GHz. The output power of the PA is tunable by changing its supply voltage. The measured and simulated results are shown in Fig. 6.6. It can be seen that when the efficiency of the PA (including the pre-driver)

is larger than 50% when the supply voltage is from 0.35 to 0.7 Volt. The PA delivers 1.06 mW output power at 0.5-V V_{DD} according to measurement. Due to the insufficient modeling of the bonding wire inductance and additional losses caused by PCB, the measured PA output power and efficiency are both slightly lower than simulation results as shown in Fig. 6.6.

The power efficiency of the TX is defined by the output power divided by the DC power of the whole TX, which includes the PA, VCO, PLL, BPSK MUX and all the auxiliary circuits. At 0.2 dBm output power, the TX consumes about 3.66 mW DC power, resulting in a total TX efficiency of 29%. The efficiencies of the TX and PA at different output power levels are plotted in Fig. 6.7. Due to the high efficiency of the PA, the overall TX efficiency exceeds 30% when the output power is above 1 dBm. The measurement results match with simulation with slight losses due to the bonding wire, package and PCB implementation.

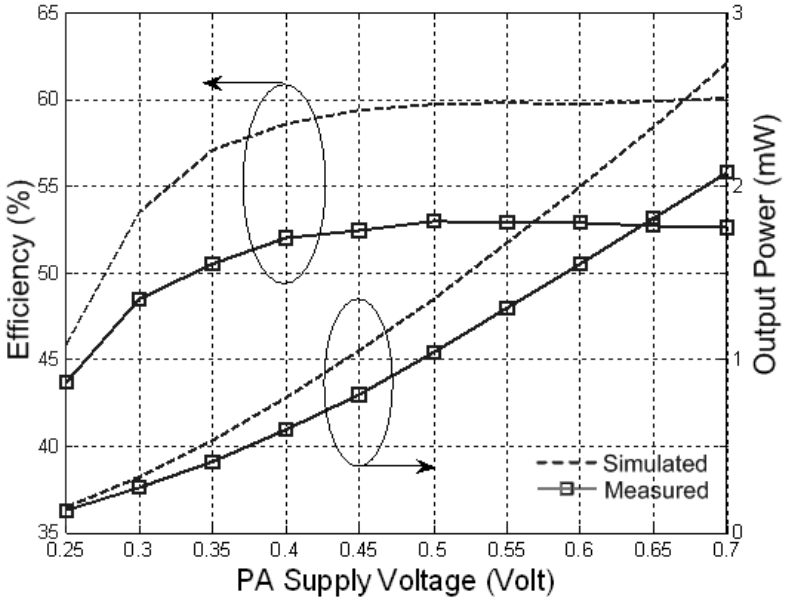


Figure 6.6. The efficiency and output power of the PA.

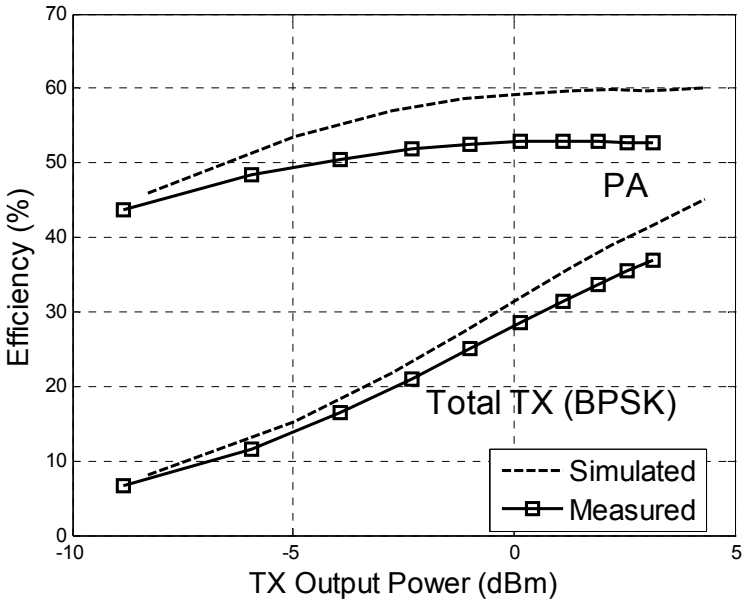
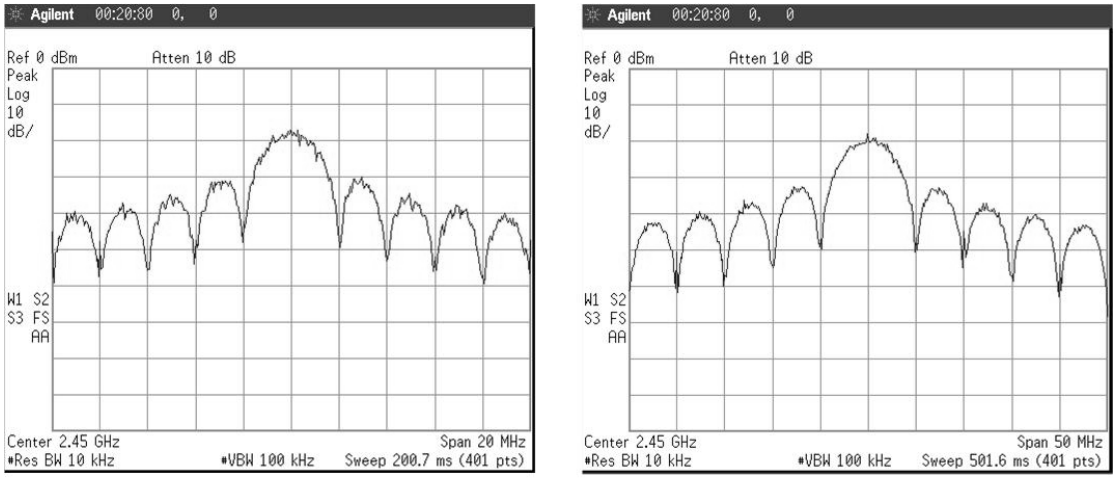


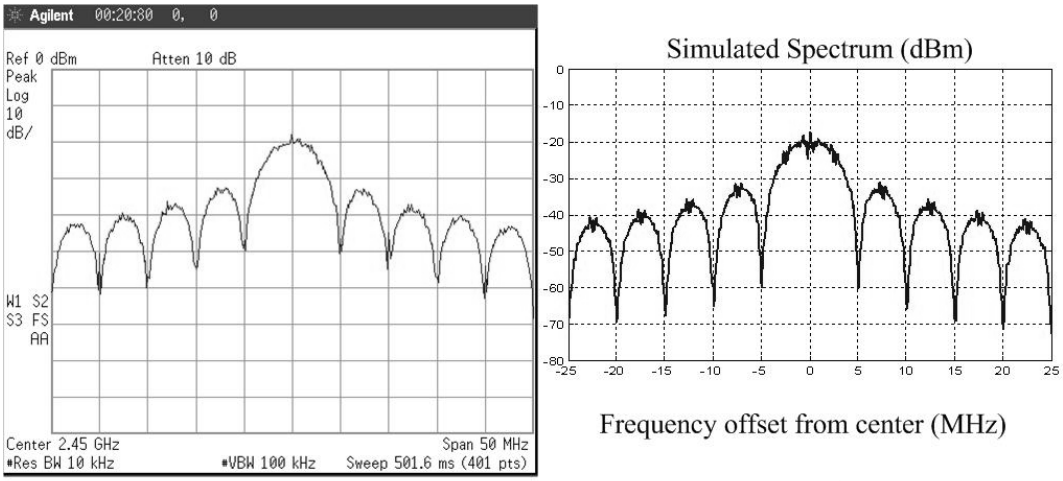
Figure 6.7. Efficiency of the PA and the whole Transmitter.

The measured BPSK spectra when sending pseudo random binary sequences (PRBS) are shown in Fig. 6.8. It can be seen that output spectra follow the Sinc function as expected. In Fig. 6.9, the measured and simulated spectra of 5 Mbps BPSK are provided. It can be seen that the measurement results match with simulation well. The data-rate of TX can exceed 10 Mbps. However, the maximum data-rate of the transceiver is limited by the RX as explained in the RX measurement part.



(a) (b)

Figure 6.8. The BPSK spectra for PRBS input for different data-rates. (a) 2 Mbps; (b) 5 Mbps.



(a) (b)

Figure 6.9. Comparison between the measured and simulated power spectrum for 5 Mbps BPSK. (a) Measured results; (b) Simulated waveform.

6.4.RX Measurement

The measured gain for the single I or Q channel is from 41.5 to 77.5 dB, with a tuning step of about 9 dB. The gain error between the I channel and Q channel is 2% (V/V). The measured phase error of I/Q signals is close to 1.0º. The measured image rejection ratio of the RX is 35 dB. As the gain of the whole RX is high, the NF of the RX is measured through the gain method [88]. The measured NF of the whole RX with I/Q quadrature mixing is 14 dB. The measured RX gain and NF is about 2 dB worse than simulation results. In simulations, all the supply rails are supposed to be ideal. In real implementation, bonding wires induce additional inductances, resulting in imperfect supply and ground. The substrate cross-talk is not modeled during simulation. The testing PCB brings with additional losses. All these effects may lead to gain and NF degradation.

To measure the performance of the BPSK RX, the input frequency is set to 2.45GHz. The demodulation is done by off-chip DSP, which incorporates matched filter and timing recovery to optimize the performance [45]. The measured eye diagram for 2 Mbps PRBS at -77 dBm input power is shown in the following figure. The time is normalized to 1 representing one bit

period. In this plot, 2000 data points are included. At this input power level with high SNR, the BER is far below 10^{-5}.

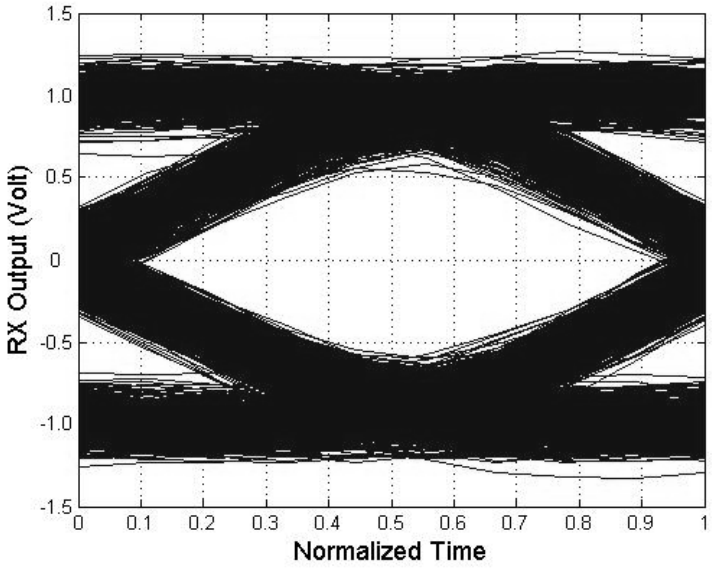


Figure 6.10. The eye diagram for 2 Mbps BPSK at -77 dBm input power. 2000 data-points are included.

When the input power is reduced to -88 dBm, the SNR degrades and the eye opening become much smaller, as shown in the following figure. With smaller eye openings, the probability for error bits becomes larger.

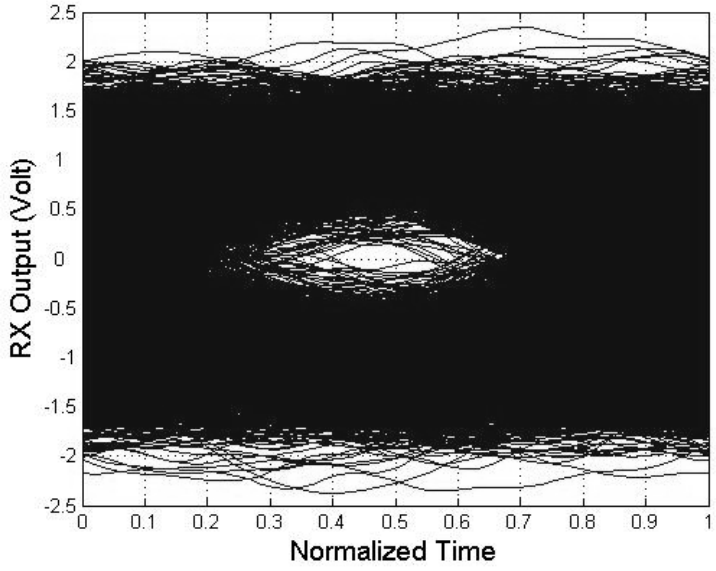


Figure 6.11. The Eye Diagram for 2 Mbps BPSK at -88 dBm input power. 2000 data-points are included.

For higher data-rate and lower input power level, the probability of error bits becomes larger due to smaller energy per bit. The measured signal constellation with 5 Mbps data-rate and -84 dBm input power is plotted in the following figure. The BPSK signals are densely distributed around two regions representing the '0' or '1' bit. At this low input power level and high data-rate, some received points may exceed the detection boundary in the middle of the figure, resulting in bit errors. As shown in the figure, 2 errors occur out of 5000 received bits.

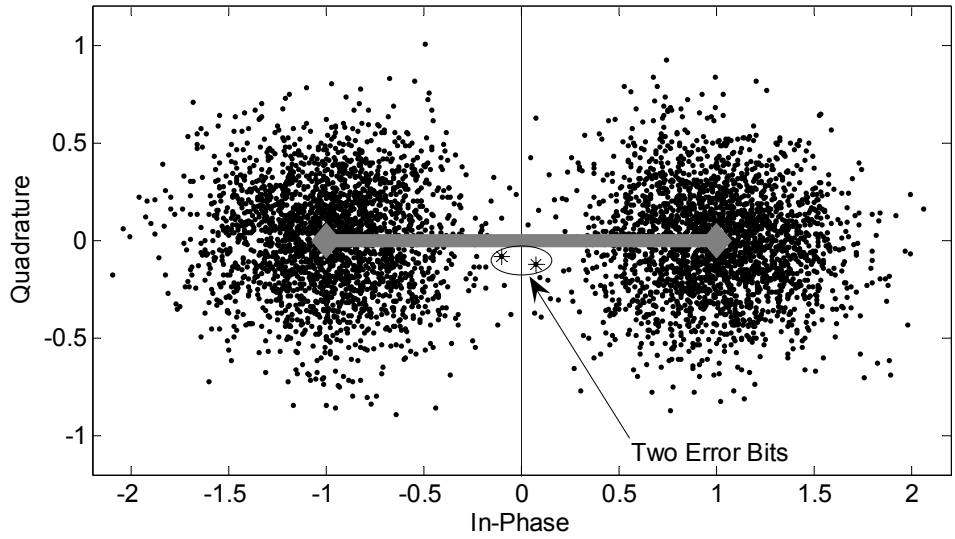


Figure 6.12. The received signal constellation of BPSK signal. The data-rate is 5 Mbps and the input power is -84 dBm. There are 2 errors in 5000 received bits.

The maximum achievable data-rate of the BPSK RX is limited to 8 Mbps. This is due to the insufficient bandwidth of the ABB. The bandwidth of the VGA is not high enough. When it is set at high gain mode, its cut-off is lower than 10 MHz. Due to process variations, the bandwidth of the amplifier in the VGA is lower than expected. The measured and simulated frequency response of the whole BPSK RX is shown in the following figure with maximum gain setting. The pass-band gain at 5 MHz is normalized to 0 dB. It can be seen that cut-off frequency of the entire BPSK RX is about 7.5 MHz, which is lower than the simulated value of 8.6 MHz. Therefore the received signal gets distorted when the signal bandwidth becomes higher. Measurement indicates that when the data-rate exceeds 5 Mbps, the RX performance

degrades a lot due to the limited bandwidth of the ABB amplifiers. The measured BER of the BPSK for different data-rates is plotted in Fig. 6.14. The sensitivities of the BPSK RX with 10^{-3} BER are -92.5, -89, -84.5, and -77 dBm for data-rates of 1, 2, 5, and 8 Mbps respectively.

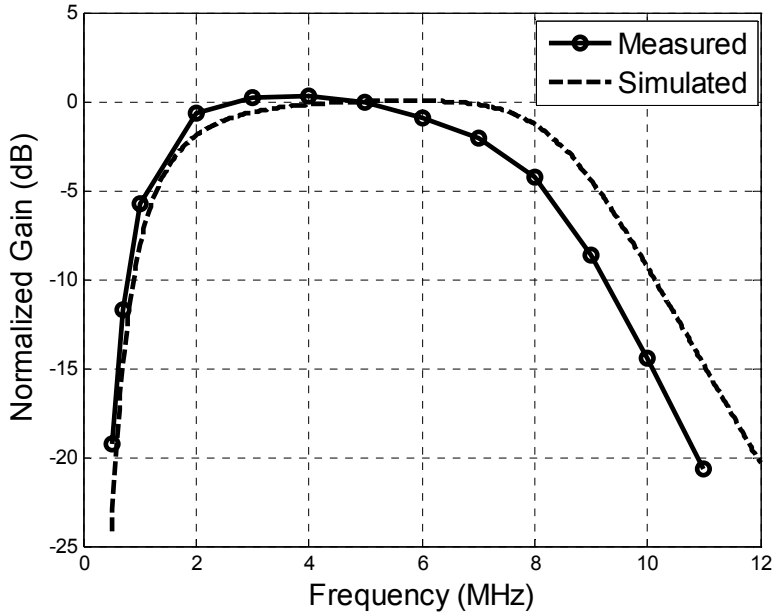


Figure 6.13. The measured frequency response of the BPSK RX.

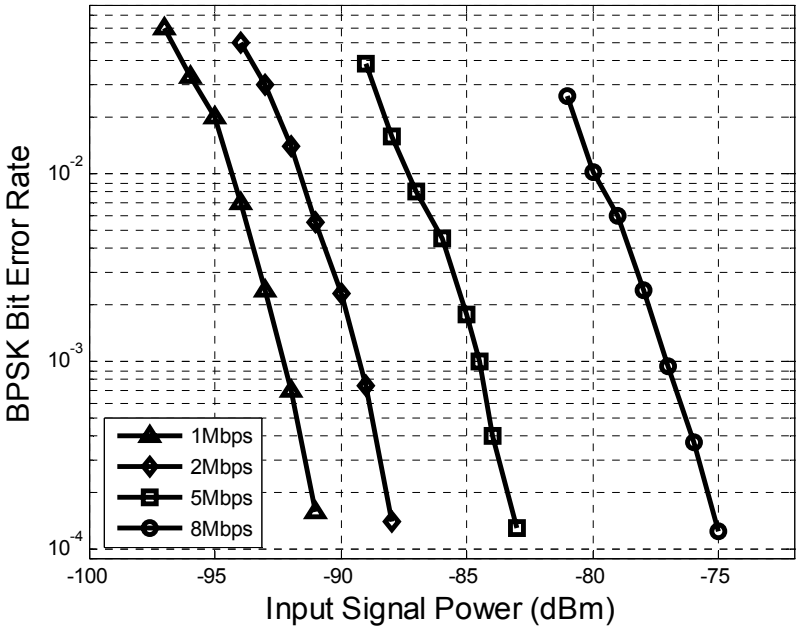


Figure 6.14. The measured BER of the BPSK RX with data-rate varying from 1 to 8 Mbps.

In the BPSK RX mode, the analog parts (including VCO, RFFE, ABB, and biasing) consume 9.05 mA with 1-Volt supply voltage. The digital parts (including PLL, BPSK MUX, and

crystal oscillator) draw 1.15 mA with 1-V supply voltage. The total power consumption of the BPSK RX is therefore 10.2 mW.

The performance of the OOK RX is measured at the input frequency of 2.40 GHz. The frequency calibration circuits automatically adjust the frequency of the DCO to generate the required LO signals. After frequency calibration, all the digital parts can be disabled to save power in the OOK RX mode. The measured power consumptions of the analog parts (including the DCO and OOK RX circuits) consume 0.78 mW with 1-Volt supply voltage. To demodulate the OOK signal, only one sample is taken for each data point. No matched filter is incorporated. The demodulation is fulfilled by an off-chip comparator. With input signal power of -79 dBm, the measured eye diagram for 5000 OOK data points is plotted in Fig. 6.15. It can be seen that the eye is open and no error bits occur. For smaller input power, the eye diagram as smaller openings resulting in higher BER. The measured BERs for different input power levels are plotted in Fig. 6.16.

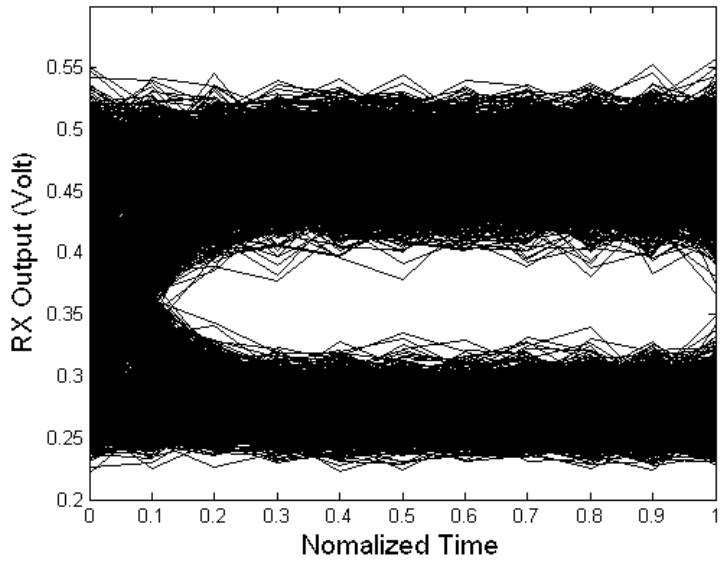


Figure 6.15. The eye diagram of the OOK RX with -79 dBm input power. The data-rate is 100 kbps and the 5000 PRBS points are included in this plot.

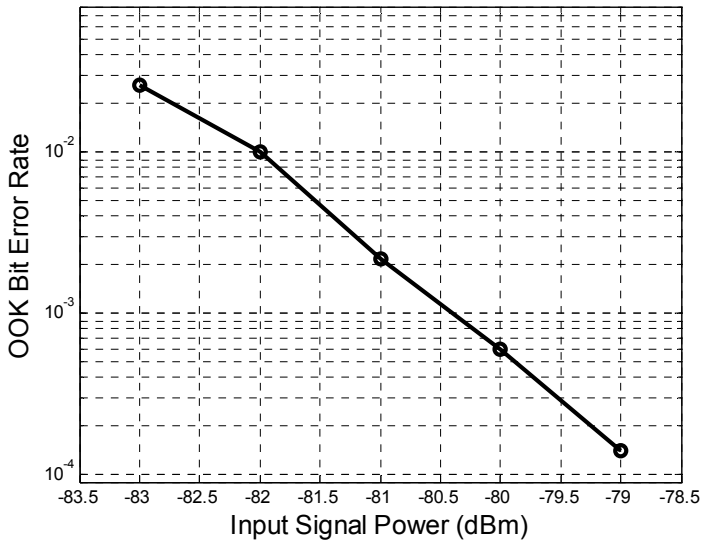


Figure 6.16. The measured BER of the OOK RX for different input power levels.

The measured and simulated input reflection coefficients (S_{11}) of the BPSK and OOK receivers are plotted in Fig. 6.17. The LNA for BPSK achieves S_{11} lower than -16 dB for the entire 2.4 GHz ISM band. The measured and simulated S_{11} waveforms both exhibit a notch in the 2.4 GHz ISM band which is due to the parallel L-C filtering effect as expected. The Measured S_{11} is worse than simulation, and the notch point position is also slightly different from the simulated results. In simulation the biasing current of the LNA is chosen such that the input impedance is matched to 50 Ω. Therefore the simulated S_{11} is well below -30dB in the entire 2.4 GHz ISM band, which is too optimistic. In actual implementations, the biasing current of the LNA cannot be finely tuned as in simulation, resulting in worse input matching than simulation. Other factors including insufficient modeling of the parasitic components in the package and PCB, and L/C value variations also cause discrepancies between measurement and simulation.

The LNA for OOK is designed for low power consumption. The input matching is not optimized. The differences between the measurement and simulation can be due to the insufficient modeling of the parasitic components and process variations.

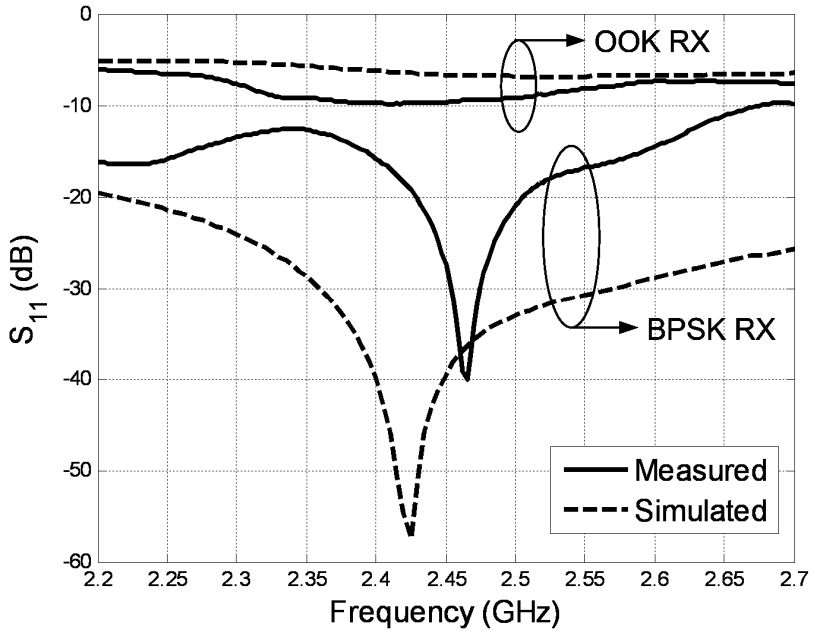


Figure 6.17. Measured and simulated input reflection coefficient (S_{11}) of the BPSK and OOK RX.

6.5. Performance Summary

The simulated and measured performances of the transceiver are summarized in the following table. The supply voltage of the transceiver is set to 1-V except for the PA. It can be seen that the measured power consumption matches well with simulation. The measured PA efficiency is about 6.5% lower than simulation which can be due to the losses from bonding wire, packaging and PCB. The measured RX performance is close to the simulation results. In the simulation, the sensitivities are estimated purely from noise figure, and are therefore too optimistic. In actual circuit, limited filter bandwidth and other implementation losses further degrade the RX performance, resulting in poorer sensitivities compared with simulation results.

Table 6.1. Performance Summary of the Transceiver

	Simulated	Measured
Power Consumption (mW)		
VCO	0.5	0.52
PLL, BPSK MUX, & Crystal Oscillator	1.0	1.15
PA & Pre-driver @ 0.5V V_{DDPA}	2.27	1.99
BPSK RFFE&ABB	8.0	8.5
OOK RFFE&ABB	0.26	0.26
BPSK TX (Total) @ 0.5V V_{DDPA}	3.77	3.66
BPSK RX (Total)	9.5	10.2
OOK RX (Total)	0.76	0.78
TX Efficiency (%)		
PA @ 0.5V V_{DDPA}	59.5	53
BPSK TX @ 0.5V V_{DDPA}	35.8	29
RX Performance		
BPSK RX Noise Figure (dB)	12	14
BPSK RX Sensitivity @ 5Mbps (dBm)	-88*	-84.5
OOK RX Sensitivity @ 100kbps (dBm)	-82*	-80.5

*Estimated from Noise Figure.

Comparisons are made also between this work and state-of-the-art designs in [17, 19]. When used as TX, this work achieves the best PA efficiencies. The PLL helps to stabilize the LO frequency and improves the robustness of the system. Even with locked PLL, this work achieves better FOM of Energy/bit/P_{out} than the reference designs [17, 19] which use free running VCO/DCO. When used as RX, this work achieves much better sensitivity in the gateway mode and consumes comparable power in the sensor mode. No additional inductors are used for the BPSK RX, and the area penalty caused by the BPSK RX is only 14%. The TX and RX share the same antenna, and no off-chip inductors or matching networks are required. The reconfigurable transceiver can support both the sensor and gateway operation modes. All the targeted design specs are met except for the maximum data-rate. The cut-off frequency of the VGA amplifiers is lower than expected. Therefore the maximum data-rate of BPSK RX is limited to 8 Mbps compared to the targeted 10 Mbps. However, this data-rate is still higher than the 5 Mbps data-rate reported in [17, 19], and therefore adequate for most WSN applications. The achieved sensitivity of -84.5 dBm at 5 Mbps data-rate is more than 9 dB better than the designs in [17, 19].

Table 6.2. Performance comparison with state-of-the-art designs.

Transceiver			
Reference	**[17] ISSCC2011**	**[19] JSSC2011**	**This Work**
Technology	90nm	0.18µm	0.13µm
Supply	1V	0.7V	1V; 0.5V for PA
Modulation	OOK	FSK	BPSK/OOK
Frequency (GHz)	2.4	0.92	2.4
Off-chip matching/inductors	Yes	Yes	No
TX			
LO generation	VCO	DCO	PLL
$P_{rad,averag}$ (dBm)	-3	-6	0.2
TX Power (mW)	2.53	0.93	3.66
PA Efficiency (%)	30	35	53
TX Efficiency (%)	24	27	29
Data-Rate (Mbps)	1/5/10	5	1/5/8
Energy/bit/$P_{rad, averag}$ (nJ/bit/mW)	5.0/1.0/0.50	0.74	3.5/0.69/0.44
RX			
Architecture	Super-regenerative	Injection-locking	Super-heterodyne
RX Power (mW)	0.53	0.42	0.78(Sensor) 10.2 (Gateway)
Sensitivity@5Mbps (dBm)	-75	-73	-84.5

CHAPTER 7 CONCLUSIONS AND FUTURE WORKS

7.1. Conclusions

Transceivers are the most power-hungry block in WSN systems. It is critical to design low-power and highly efficient transceiver for sensor nodes. Sensor-gateway communications require asymmetry data link, i.e. sensor has high data-rate TX (uplink) and low data-rate RX (downlink) whereas the gateway exactly complements the sensor. The gateway transceiver can be optimized for good performance by consuming higher power. This thesis presents several techniques to optimize the performances of the transceivers for asymmetry sensor-gateway communications.

Firstly, a reconfigurable transceiver is designed which supports both the sensor and gateway operation modes. The TX for the sensor is optimized for power efficiency. BPSK modulation is used in the uplink, which not only allows compact circuit realization of the TX but also improves the RX performance. No pulses shaping is adopted for BPSK transmission, which compromises the spectral efficiency to achieve better power efficiency. Simple OOK is adopted in the downlink, which helps to achieve low-power RX on the sensor nodes.

Secondly, a new low-power Class-E PA is proposed, which helps to increase the overall efficiencies of the TX. The PA is suitable for low-power applications where the output levels are between 0 to 10 dBm. A π-matching network is incorporated which not only suppresses the higher harmonics but also realizes impedance transform. Comprehensive equations are derived to select component values and optimize the PA design. Measurement results indicate that the fully integrated Class-E PA can achieve PE above 50% while delivering 0 dBm output power.

Thirdly, circuit block co-design and reuse techniques are adopted in the transceiver design. The inductor in the π-matching output network for the PA is reused in the input filter for the BPSK-LNA. The input matching of the BPSK-LNA is improved by this scheme. The T/R switch is not located in the RF signal path, which improves the TX efficiency. No additional inductors are used in the BPSK RX to save area. The area penalty due to the BPSK RX accounts for only 14% of the total chip area. The VCO is reused as the DCO to generate LO signals for OOK demodulation. The prescaler in the PLL is reused in the frequency calibration modules.

The reconfigurable transceiver supports both the sensor and gateway modes. When used in sensors, the BPSK TX achieves power efficiency of 29% at output power of 0.2 dBm, and the OOK RX consumes only 0.78 mW with sensitivity better than -80 dBm. The achieved TX efficiency with a locked PLL is comparable with the state-of-the-art designs with free running VCO or DCO. The BPSK RX achieves high sensitivities of -92, -89, and -84.5 dBm for data-rates of 1, 2, and 5 Mbps respectively, which are about 10 dB better compared with existing designs [17, 19].

7.2.Future Works

The transceiver presented in this thesis is implemented in 0.13 μm CMOS. It still requires two different supply voltages, where the PA uses about 0.5-Volt supply and the other parts works under 1-Volt V_{DD}. By adopting better technology nodes, it is possible to realize the whole transceiver with a single 0.5-Volt power supply voltage, which may further reduce the power consumptions of the overall system. Therefore low-voltage, low-power designs for frequency synthesizer and RF and BB amplifiers require further research. At lower supply voltage, the amplifiers suffer from reduced headroom and limited dynamic range. The gain of the amplifier is also reduced due to the difficulty in incorporating cascode structure. New

techniques are required to design low-voltage low-power amplifiers. With lower supply voltage, conventional analog PLL architecture suffers from several issues including limited VCO tuning range, poorer charge-pump performance, and loop-filter inaccuracy. All-digital PLL (ADPLL) architecture may help to solve these problems [89]. With advanced technology node and reduced supply voltage, the power consumption of digital circuits can be largely reduced. It will be valuable to look into the low-voltage and low-power design of the ADPLL, which may also help to improve the performance of the frequency synthesizer and reduce the chip area.

In this design, the output power control of the transmitter is realized by changing the supply voltage of the Class-E PA. This requires variable voltage supply source which is difficult to realize. Further research is needed to investigate schemes which change the output power levels of the PA with a constant supply voltage. The power control of the proposed Class-E PA may be realized by altering the component values in the matching network while still maintaining the Class-E conditions.

The ring oscillator based LO generation circuitry is another promising exploration direction for it has much smaller on-chip area compared with the LC-VCOs. The major problem with the ring oscillator is its poor phase noise, which strongly impacts phase modulated signals. Although injection-locking technologies may significantly improve the phase noises of ring oscillators, it cannot achieve the fine frequency tuning steps as in conventional PLLs. Therefore it is not suitable for multiple channel applications. To tackle this issue, more research is needed to improve the tunability of the injection locked oscillators. Conventional designs use single tone injection signals to lock the oscillator, which limit the output frequency to be integer multiples of the injection frequency. It may be possible to alter the injection signal frequency and incorporate $\sum$-Δ modulation so as to realize fine tuning steps.

The BPSK modulations cannot support high data-rate. QPSK, 8-PSK, or QAM transceivers can be designed to achieve better data throughput. Spectral efficiency can be improved by including pulse shaping technologies. However, pulse shaping may complicate the circuit structure and increase the power consumption. Non-constant envelope output signal also requires a linear PA which has a much lower efficiency than the nonlinear counterpart. Polar transmitter with nonlinear PA can potentially achieve both high energy efficiency and spectral efficiency. Therefore low-power polar transmitter architecture is a promising direction for further researches.

Energy harvesting and energy scavenging technologies are worthwhile to study for WSN application. It is possible to harvest energies from ambient lights, motions, radio waves, and thermal sources. Circuit related researches include low-loss rectifiers, switches, DC-DC converters, energy storages, etc.

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APPENDIX. THE DETAILED FUNCTIONS TO CHARACTERIZE THE CLASS-E PA

Appendix A. Function Expressions for Output Network and Power

The required functions for deriving the output network of L_1 and C_3 are given by Eq. (A1)–(A4). The function h which defines the output power of the PA is given by Eq. (A5). The sub-functions of $u_1,\ldots,u_4$, $v_1,\ldots,v_4$, and $h_1,\ldots,h_5$ in Eq. (A1)–(A5) are provided in Appendix B.

$$V_{2\_1} = \sqrt{V_I^{\,2} + V_Q^{\,2}}\ . \tag{A1}$$

$$\phi_1 = \tan^{-1}(V_I / V_Q)\ . \tag{A2}$$

$$V_I = \frac{\alpha\left(u_1 + u_2 + u_3 + u_4\right)}{\pi\left(q^2 - 1\right)} - \kappa\frac{\alpha(1-\alpha)}{1-\beta}\sin(\varphi)\ . \tag{A3}$$

$$V_Q = -\frac{\alpha\left(v_1 + v_2 + v_3 + v_4\right)}{\pi\left(q^2 - 1\right)} + \kappa\frac{\alpha(1-\alpha)}{1-\beta}\cos(\varphi)\ . \tag{A4}$$

$$h(q, D) = h_1 + h_2 + 0.5\left(h_3 + h_4 + h_5\right)D. \tag{A5}$$

Appendix B. Sub-Functions

$$a_1 = 2\pi(1-D)(1+q) + \varphi\ .$$

$$a_2 = 2\pi(q-1)(1-D) - \varphi\ .$$

$$a_3 = 2q\pi(1-D) + \varphi\ .$$

$$a_4 = 2q\pi(1-D) - \varphi\ .$$

$$a_5 = 2\pi(1-D)+\varphi\ .$$

$$k_1 = -q\sin(\varphi) - q\cos(2q\pi(1-D))\cos(\varphi)\sin(2\pi D)\ .$$

$$k_2 = 2q\cos(2q\pi(1-D))\sin(\varphi)\cos^2(\pi D)\ .$$

$$k_3 = -q\cos(2q\pi(1-D))\sin(\varphi)\ .$$

$$k_4 = \sin(2q\pi(1-D))\cos(\varphi)\left(-2\cos^2(\pi D)+1\right).$$

$$k_5 = -\sin(2q\pi(1-D))\sin(\varphi)\sin(2\pi D)\ .$$

$$g_{n1} = -0.5q\sin(\pi D)\sin(2q\pi(1-D))\ .$$

$$g_{n2} = -\pi q^2 D\sin(\pi D)\cos^2(q\pi(1-D))\ .$$

$$g_{n3} = -\cos(\pi D)\left(1-\cos^2(q\pi(1-D))\right)\ .$$

$$g_{n4} = -0.5Dq\pi\cos(\pi D)\sin(2q\pi(1-D))\ .$$

$$g_{d1} = \sin(\pi D)\left(\cos^2(q\pi(1-D))-1\right)\ .$$

$$g_{d2} = q^2\sin(\pi D)\left(1-\cos^2(q\pi(1-D))\right)\ .$$

$$g_{d3} = 0.5\pi qD\sin(\pi D)\sin(2q\pi(1-D))\ .$$

$$g_{d4} = -\pi q^2 D\cos(\pi D)\cos^2(q\pi(1-D))\ .$$

$$g_{d5} = -\pi q^2 D\cos(\pi D)\ .$$

$$h_1 = \frac{1}{2\pi}\left[A_2\sin(2q\pi(1-D)) - A_1\left(1-\cos(2q\pi(1-D))\right)\right].$$

$$h_2 = \frac{\kappa}{2\pi}\frac{q^2}{q^2-1}\left(\sin(-2\pi D+\varphi)-\sin(\varphi)\right).$$

$$h_3 = A_2 q + \kappa\frac{q^2}{q^2-1}\cos(\varphi)\ .$$

$$h_4 = A_2 q\cos(2q\pi(1-D)) - A_1 q\sin(2q\pi(1-D))\ .$$

$$h_5 = \kappa\frac{q^2}{q^2-1}\cos(-2\pi D+\varphi)\ .$$

$$u_1 = -\sin(2\pi D)q^2 + \sin(2\pi D) + A_2 q\ .$$

$$u_2 = \kappa\pi(1-D)\sin(\varphi) + 0.25\kappa\cos(\varphi) - 0.25\kappa\cos(-4\pi D+\varphi)\ .$$

$$u_3 = 0.5q\left(-A_2 r_1 + A_1 r_2 - A_2 r_4 + A_1 r_3\right).$$

$$u_4 = 0.5\left(A_2 r_1 - A_1 r_3 + A_1 r_2 - A_2 r_4\right).$$

$$v_1 = (q^2 - 1)\left(1 - \cos(2\pi D)\right) - A_1.$$

$$v_2 = 0.25\kappa\left(\sin(\varphi) - \sin(-4\pi D + \varphi)\right) + \kappa\pi(1 - D)\cos(\varphi).$$

$$v_3 = 0.5q\left(A_1 r_4 + A_2 r_2 - A_2 r_3 - A_1 r_1\right).$$

$$v_4 = 0.5\left(A_1 r_4 + A_2 r_3 + A_2 r_2 + A_1 r_1\right).$$

$$r_1 = \cos(2\pi(q - D - qD)).$$

$$r_2 = \sin(2\pi(q + D - qD)).$$

$$r_3 = \sin(2\pi(q - D - qD)).$$

$$r_4 = \cos(2\pi(q + D - qD)).$$