LOW-VOLTAGE LOW-POWER SWITCHED-CAPACITOR ΔΣ MODULATOR DESIGN

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SUMMARY

As most of modern signal processing systems use digital signal instead of analog one, the interface between digital and real world becomes more crucial. ADC and DAC are two fundamental building blocks at these interfaces to convert data from one format to another. With the growing demand in portable and handheld devices, low-power ADC design attracts much research effort in the past few years, especially sub-1 V Delta-Sigma (ΔΣ) modulators. In this research, we proposed several techniques for low-voltage low-power ΔΣ modulator designs.

The first fabricated chip in the study is a fourth-order audio-band ΔΣ modulator with a single-loop single-bit input-feedforward architecture which employs a finite impulse response (FIR) feedback DAC [1]. It has been implemented in a 0.13-μm CMOS process. Switch-free direct summation technique has been adopted to minimize the power consumption and reduce the supply voltage. Conventional switched-capacitor (SC) summation circuit for the feedforward paths is removed, and it is replaced by a multi-input comparator. A 2-tap FIR filter is inserted in the feedback loop to effectively attenuate the high frequency quantization noise, resulting 22% reduction in the maximum integration step of the first integrator and relaxing the slew rate requirement for the OTA to 9.5 V/μsec (diff). Clocked at 4 MHz, the modulator achieves 87.0 dB SNDR, 91.4 dB SNR, and 91.8 dB DR for a 20-kHz signal bandwidth while consuming 99.7 μW from a 0.7-V supply.

The second prototype presents a 0.5-V 1.5-bit double-sampled ΔΣ modulator for audio codec. Unlike other existing double-sampled design, the proposed double-sampled ΔΣ modulator employs input-feedforward topology, which reduces internal signal swings, hence relaxes design requirements for low-voltage amplifier and reduces distortion. Moreover, the proposed architecture with compensation loop restores noise transfer function to that of its single-sampled version and avoids performance degradation. It also employs a new fully-differential amplifier with a global common-mode feedback loop to minimize power, as well as a resistor-string-reference switch matrix based on direct summation quantizer to simplify compensation loop. The chip prototype has been fabricated in a 0.13-μm CMOS technology with a core area of 0.57 mm^2. The measured results show that operated from a 0.5-V supply voltage with a clock frequency of 1.25 MHz, the modulator achieves a peak SNDR of 81.7 dB, a peak SNR of 82.4 dB and DR of 85.0 dB while consuming 35.2 μW for a 20-kHz signal bandwidth.

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LIST OF ABBREVIATIONS

A-A	Anti-Aliasing
ADC	Analog-to-Digital Converter
ASP	Analog Signal Processing
CMRR	Common Mode Rejection Ratio
CMFB	Common-Mode Feedback
CT	Continuous-Time
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processing
DT	Discrete-Time
DR	Dynamic Range
ENOB	Effective Number of Bits
FOM	Figure-Of-Merits
LP	Low-Pass
NTF	Noise Transfer Function
OTA	Operational Transconductance Amplifier
OSR	OverSampling Ratio
PSRR	Power Supply Rejection Ratio
PCB	Printed Circuit Board
PSD	Power Spectral Density
SNR	Signal to Noise Ratio
SC	Switched-Capacitor
SNDR	Signal-to-Noise-and-Distortion Ratio
SQNR	Signal-to-Quantization Noise Ratio

SOC	System-On-Chip
STF	Signal Transfer Function
THD	Total Harmonic Distortion

CHAPTER 1

INTRODUCTION

Microelectronics technologies have changed our life by its rapidly improved products for more than four decades. The key ability of microelectronics is to reduce feature size of transistor for lowering fabrication cost. One of the most famous trends is geometrical scaling, which is usually expressed as Moore's Law. The scaling trend has guided targets for decades, and will continue in many aspects of chip manufacture.

Reduced transistor channel length and thickness of gate dielectrics have driven supply voltage to decline for reliability reasons. Since voltage difference is the most common used expression in today's mixed signal circuits, reduced supply voltage means decreasing the maximum achievable signal level. In order to keep the same dynamic range, analog circuits are likely to dissipate more power when the dynamic range is limited by thermal noise. This has a strong impact on mixed-signal product development for system-on-chip (SOC) solutions. Moreover, reduced supply voltage decreases voltage headroom of analog circuits, which limits the choices of circuit topologies. For example, the telescopic topology is seldom used in low-voltage design despite its high gain feature.

Impact of the voltage drop between drain and source upon effective channel length becomes more severe than ever as the effective channel length decreases. This results in reduced intrinsic gain of transistors. Reduced device intrinsic gain causes difficulty in building precision analog blocks. The accuracy of analog blocks is important to

system in many aspects of performances, such as harmonic distortion, offset error, differential non-linearity, etc. This trend demands a robust system with relaxed requirement on analog blocks.

1.1 Overview of Analog-to-Digital Converters

Analog-to-digital converters (ADCs) are frequently required to interface digital processors to real signals such as radio, image and speech. Since quantization of continuous amplitude of information requires analog operations, ADCs often limit the throughput of digital signal processing (DSP) based systems. In general, ADCs can be categorized into Nyquist ADCs and oversampling ADCs based on sampling rate. Usually, the minimum required sampling rate of Nyquist ADCs is twice the bandwidth of input signal, thus signal bandwidth of this sort of ADCs could achieve several tenth Giga Hertz [2-4]. However, their accuracy is directly limited by quantization error and hence its resolution is restricted to approximate 15 bits of effective number of bit (ENOB) [5, 6]. Oversampling ADCs have their sampling frequency considerably higher than the bandwidth of input signal. Oversampling avoids aliasing, improves resolution and reduces in-band noise. Resolution of this sort of ADCs could achieve 24 bits [7-9], but the maximum bandwidth of the ADCs is limited by a few hundred Mega Hertz [10]. Survey data collected advanced ADCs [11], regardless of their architecture, over past fourteen years indicates that the power efficiency of ADCs, has improved on average by a factor of two every two years while the performance has doubled every four years. It also demonstrates that speed, power efficiency and resolutions are most important trade-off in design of state-of-the-art advanced ADCs.

1.2 Motivation

Usually, quantization noise is evenly spread over the whole bandwidth of converter at the Nyquist sampling rate. If an analog signal is sampled at a rate much higher than that of the Nyquist frequency during analog to digital conversion and then digitally filtered to limit it to the signal bandwidth, the resulting signal may have the following features.

- Due to better properties of digital filters a sharper anti-aliasing filter can be realized and hence the filtered signal could have better result.
- With oversampling technique, it is possible to obtain an effective resolution larger than that provided by the converter alone.
- The improvement in SNR is 3 dB per octave of oversampling which is not sufficient for many applications. Therefore, oversampling is usually associated with noise shaping. With noise shaping, the improvement is $6L + 3$ dB per octave where L is the order of loop filter used for noise shaping. For example, a second-order loop filter provides an improvement of 15 dB per octave.

Therefore, ΔΣ ADCs, which use both oversampling and noise shaping techniques, have a unique character that is suitable for nanometer-scale technologies. First, the design requirement for a front-end anti-alias filter is quite relaxed due to oversampling reasons. The roll-off frequency response needs not be too sharp as that for Nyquist ADCs. This results in simpler architecture of the anti-alias filter as well as less power consumption. Second, since noise shaping technique improves the effective resolution while high loop gain suppresses distortions induced by analog building blocks, stringent accuracy is not required in analog building blocks in most

cases. For example, more than 100 dB DC gain is required for amplifier in first few stages of a pipeline structure which is desired to achieve 14 bit resolution if no digital calibration is used [12]. In contrast to pipeline ADCs, a single-loop high-order ΔΣ modulator needs only 40 dB DC gain for the first amplifier to reach the same accuracy level [13, 14]. Since continuing down scaling of effective channel length makes the intrinsic gain of a transistor decrease to approximate 20 dB in sub-100 nm CMOS technologies [15], ΔΣ ADCs demonstrate a great compatibility with state-of-the-art CMOS technologies which is substantially optimized for digital circuitry.

Low-voltage low-power ΔΣ ADCs have increasingly gained attentions not only because of the need for accompanying pace of down-scaling, but also due to the proliferated demand for portable or handheld applications. For past ten years, lowest supply voltage of this sort of ADCs for audio-band applications has declined from 1 V to approximate 0.25 V [16] while the power consumption has decreased from several milliwatts [17, 18] to several tenth microwatts [19, 20]. Although power consumption of this sort of ADCs has considerably decreased, the performance still remains as high as above 85 dB of dynamic range (DR), so that it is applicable in many cases such as image sensor, digital-audio codec [20-24].

1.3 Objectives and Significances

Research gaps for current study of low-voltage low-power SC ΔΣ modulators are summarized below:

- Although single-loop multi-bit ΔΣ modulators exhibit good robustness and could handle full input signal range, the quantizer suffers from mismatch

problem and hence the performance is degraded [25]. Moreover, dynamic element matching (DEM) circuit which is employed to suppress non-linearity of DAC tends to consume at least several hundred microwatts [14].

- Single-loop single-bit ΔΣ modulators tend to result in lower power consumption. However, low-order of this architecture suffers from idle tone while high-order architecture might encounter stability problem [26]. Moreover, SC implementation of this architecture usually fails to reach full referece range and hence is inferior to its multi-bit counterpart.
- Multi-stage noise shaping ΔΣ modulators (MASH) avoid stability problem while restore high-order noise shaping character. Unfortunately, this architecture suffers from mismatch problem between stages and requires high accuracy of analog building blocks. Therefore, this architecture tends to result in higher power consumption [27].

The main aim of this study is to propose a low-voltage low-power SC ΔΣ modulator. The specific objectives of this study are to:

- Develop a SC sampling network that could handle full available reference range for single-loop single-bit ΔΣ modulators.
- Analyze and compare the noise performance of the proposed sampling network with conventional sampling network.
- Develop a power-efficient amplifier or system architecture that suitable for low-voltage low-power audio-band applications.
- Reduce supply voltage to the extent that could be comparable to sum of the threshold voltage of both PMOS and NMOS.
- Minimize the power consumption while maintaining high DR as before.

1.4 List of Publications

The listed below are publications generated from this study.

Zhenglin Yang, Libin Yao, "A 1-V 190-μW Delta-Sigma Audio ADC in 0.13-μm full digital CMOS technology," *IEEE International Conference on Electron Devices and Solid-State Circuits*, pp.1-4, Dec., 2008.

Zhenglin Yang, Libin Yao, Yong Lian, "A 0.7-V 100-μW Audio Delta-Sigma Modulator with 92-dB DR in 0.13-μm CMOS," *Proc. IEEE Int. Symp. Circ. Syst. (ISCAS)*, pp. 2011-2014, May, 2011.

Zhenglin Yang, Libin Yao, Yong Lian, "A 0.5-V 35-μW 85-dB DR Double-Sampled ΔΣ Modulator for Audio Applications," *IEEE Journal of Solid-State Circuits*, pp. 722-732, Mar., 2012.

1.5 Organization of the Thesis

The thesis is organized as follows:

Chapter 2: This chapter presents a brief review of ΔΣ converter. Theoretical calculation of basic parameter is presented first, followed by an introduction of several architectures of ΔΣ modulator and their implementation.

Chapter 3: This chapter discusses design considerations for low-voltage low-power circuits. The discussion starts from low-voltage circuit design issues. Then it is followed by low-voltage circuit design techniques. Collaborated with low-voltage application, low-power design technique is presented at the end.

Chapter 4: This chapter presents a low-voltage low-power ΔΣ modulator for audio-band applications. The Architecture of this modulator is based on input-feedforward topology. The modulator employs a 2-tap FIR DAC to reduce integration step of the first stage. The feedforward path is embedded in a multi-input comparator to simplify circuit implementation. The fabricated prototype operates from a 0.7-V supply voltage while consuming 99.7 μW.

Chapter 5: This chapter presents a double-sampled 1.5-bit SC ΔΣ modulator for audio-band applications. The modulator operates from a 0.5-V supply with a three level quantization. Compensated double sampling scheme and a proposed sampling network with an improved noise performance are employed in the work. The chip prototype has been fabricated in a 0.13-μm CMOS technology with a core area of 0.57 mm^2.

Chapter 6: This chapter summarizes the study and draws conclusions. Future work of low-voltage low-power ΔΣ converter is also presented here.

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CHAPTER 2

BRIEF REVIEW OF ΔΣ CONVERTERS

When modern signal processing extensively employ digital signal other than analog signal, the interface between digital domain and real world becomes more crucial. ADCs and DACs are fundamental building blocks of theses interfaces. Low-voltage low-power circuits are increasingly demanded for portable or handheld devices while their performances still expected to be high. These low-voltage low-power ADCs are the subject of this study.

Compared to classical Nyquist ADCs such as pipeline, successive approximation and flash type, ΔΣ ADCs offer many unique advantages. First, the combination of oversampling and noise-shaping technique allows it to trade speed for accuracy. Therefore the converter is insensitive to circuit imperfections such as mismatch. Although ΔΣ ADCs require an additional digital decimation filter to remove the out-of-band quantization noise, modern CMOS technologies which substantially optimized for digital circuits make the implementation of this type of ADC easy. Second, due to inherently oversampling character of the ADCs, the complicated analog anti-aliasing filter with sharp transition is avoided. Third, one type of ΔΣ ADCs which called frequency-to-digital ΔΣ ADCs mostly implements all building blocks by digital circuits [28, 29], and hence is very compatible with state-of-the-art nano-scale technologies.

This chapter starts from Nyquist conversion, and then presents the quantization error

and the calculated signal-to-noise ratio of the converter. Next, the concepts of oversampling and noise-shaping are introduced. Finally, several architectures of ΔΣ modulators as well as circuit implementations are presented.

2.1 Nyquist-Rate ADCs

In a Nyquist conversion, the signal bandwidth f_b could reach up to $\frac{f_s}{2}$, where f_s represents the sampling frequency of the system. As illustrated in Figure. 2.1, a Nyquist-rate ADC usually consists of an anti-aliasing filter, a sampler and a quantizer. The input of the Nyquist conversion system is a continuous-time signal $X_c(t)$. A continuous time signal $X_c(t)$ is converted into discrete data $X_d(n)$ by the sampler. If the frequency of the input signal exceeds the band of interest, an anti-aliasing filter is required to remove the out-of-band signals because these parts can alias into the baseband because of sampling operation. The anti-aliasing filter has a low-pass filter character. In ideal case, the transition band is zero and hence the minimum sampling frequency without aliasing is $2f_b$. In practice however, the abrupt transition from passband to stopband cannot be implemented. Therefore, for a proper operation, the corner frequency is defined as $\frac{f_s}{2}$, which represents the sum of the signal band and the transition band. This implies that the practical Nyquist conversion is slightly oversampled. The quantizer converts the sampled data $X_d(n)$ into quantized data $X_q(n)$. Meanwhile, the quantization error is introduced into signal band. The maximum amplitude of quantization error is dependent on the levels of the quantizer. If the sampled data varies random enough, the introduced quantization error can be regarded as a white noise. In time domain, the input signal is multiplied by a periodic

Dirac pulses spaced at $\frac{1}{f_s}$. This corresponds to a convolution with a periodic pulse spaced at f_s in the frequency domain. After the convolution, aliasing appears if the highest frequency of input signal exceeds $\frac{f_s}{2}$.

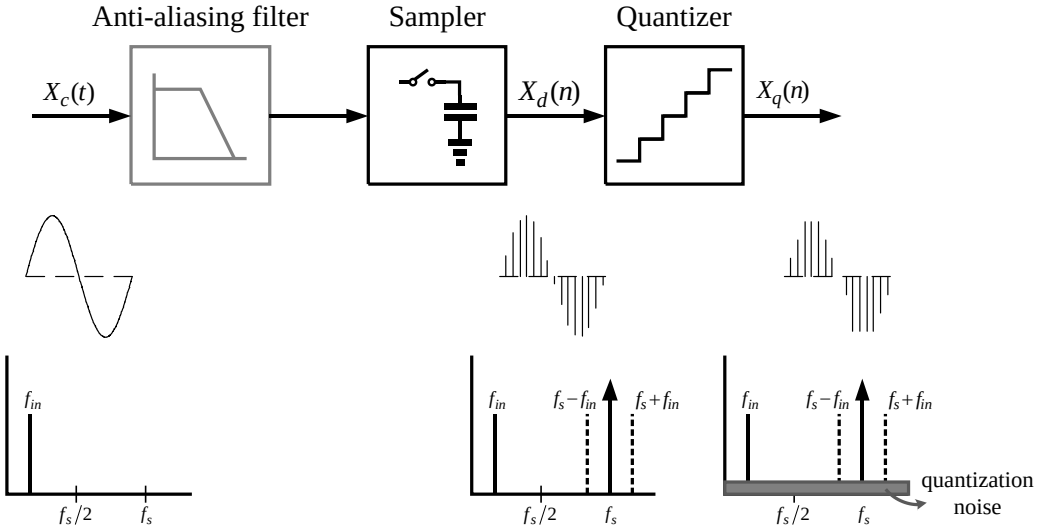


Figure 2.1 Block diagram of Nyquist-rate ADC and operation of the different blocks in time and frequency domain.

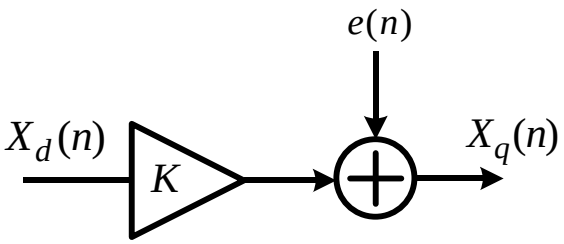


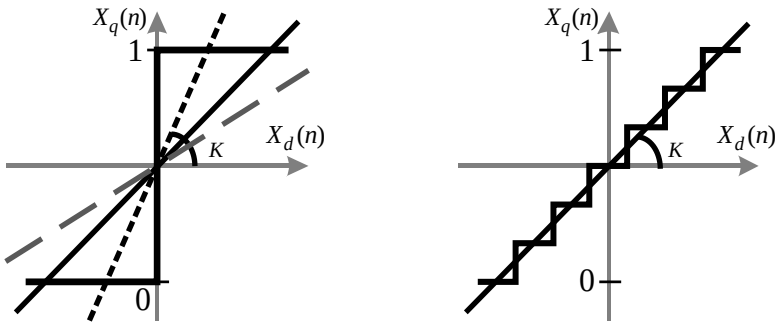
Figure 2.2 Linear model of quantizer.

Figure 2.2 shows a linear model of a quantizer, where $X_d(n)$, $X_q(n)$, $e(n)$, K represent the sampled data, the quantized data, the quantization error and the gain of the quantizer, respectively. This figure implies that even an ideal quantizer does introduce a degradation of the input signal. Since the input and output range are not necessarily equal, the quantizer can exhibit a gain different from one. Figure 2.3

shows transfer characteristics of single-bit and multi-bit quantizer, respectively. We can clearly see that the quantization gain of single-bit quantizer could vary arbitrarily while that of multi-bit quantizer might be regarded as constant. If the quantization error could be represented by a white noise source, the total quantization noise power can be calculated as [30]

$$e_q^2 = \int_{-\infty}^{\infty} e^2 de = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12}, \tag{1}$$

where Δ is defined as the step size of the quantizer.



(a) (b)

Figure 2.3 Transfer characteristics of (a) single-bit quantizer and (b) multi-bit quantizer.

In order to obtain signal-to-noise ratio (SNR) of the quantizer, the signal power also needs to be calculated. The maximum signal range of the quantizer [31] can be represented by

$$x_{max} = 2^m \frac{\Delta}{2}\frac{1}{k}, \tag{2}$$

where m represents the number of bits of the quantizer, K represents the gain of the quantizer. Thus, the signal power through the quantizer is

$$Power = \frac{(kx_{max})^2}{2} = 2^{2m-3}\Delta^2. \tag{3}$$

From the ratio of (1) and (3), the peak SNR of an ideal m-bit quantizer can be expressed as

$$SNR_p = 1.76 + 6.02\, m \;\; dB, \tag{4}$$

It should be noted that each additional bit in the quantizer results in approximate 6 dB improvement in SNR.

2.2 Oversampling ADCs

Besides classical Nyquist ADCs, an alternative type of ADCs is oversampling ADCs which have their input signal sampled at much higher frequency than the Nyquist sampling rate. And the oversampling ratio (OSR) is defined as the effective sampling frequency divided by the Nyquist rate, i.e.,

$$OSR = \frac{f_S}{f_N} = \frac{f_S}{2f_b}. \tag{5}$$

Figure 2.4 shows the operation of an oversampling ADC. Compared to Nyquist-Rate ADCs illustrated in Figure 2.1, a decimation filter is required in the post signal

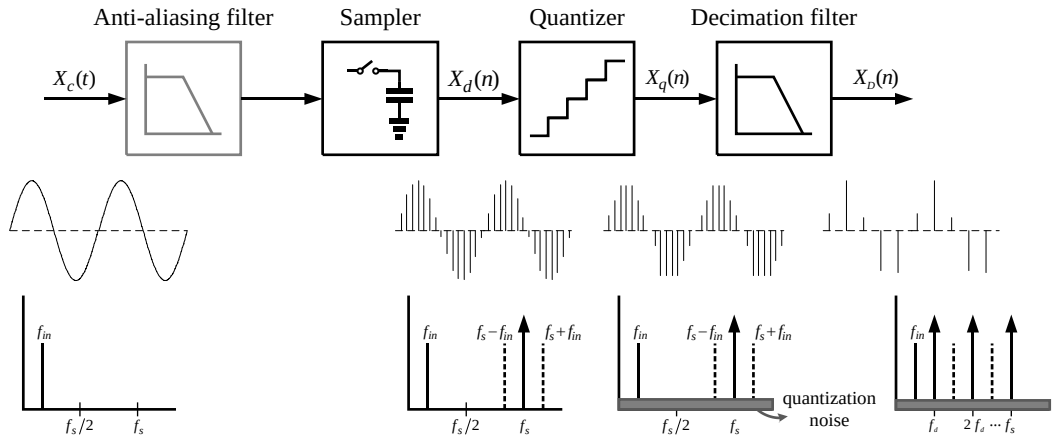


Figure 2.4 Block diagram of oversampling ADC and operation of the different blocks in time and frequency domain.

processing. The function of the decimation filter is to down-sample the quantized result at a lower rate while convert the oversampled short-bit word to long-bit one.

Oversampling ADCs have an advantage that the high sampling rate significantly alleviates the design requirement for the analog anti-aliasing filter. This is because the signal bandwidth f_b is much lower than half of the sampling rate $\frac{f_s}{2}$ and the spectrum between f_b and $\frac{f_s}{2}$ cannot alias into the signal band, therefore, the large transition space from pass band to stop band eases implementation of the anti-aliasing.

Since all quantization noise appears at the band of $-\frac{f_s}{2}$ to $\frac{f_s}{2}$, only a portion of them falls into the band of interest. Thus the total quantization noise power can be calculated as [30]

$$N_q = e_q \frac{f_b}{f_s/2} = \frac{\Delta^2}{12OSR}, \tag{6}$$

where Δ is defined as the step size of the quantizer. Compared to a Nyquist-rate converter, the noise power of the signal band is reduced by OSR.

The equation to calculate the signal power is identical as that for a Nyquist-rate converter. The peak SNR of an oversampling converter results in:

$$SNR_p = 1.76 + 6.02\, m + 10 \log(OSR)\ \ dB. \tag{7}$$

where m represents the number of bits of the quantizer.

2.3 ΔΣ Modulators

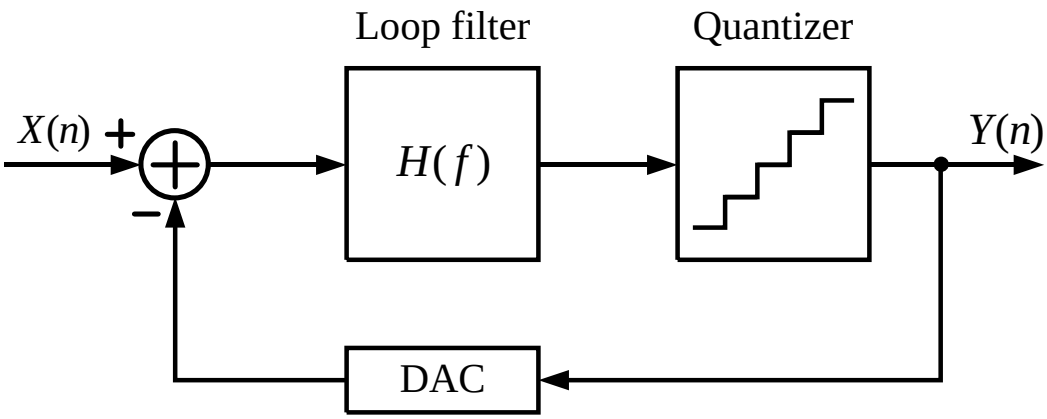


Figure 2.5 General block diagram of ΔΣ modulator.

By applying a high-gain loop filter before the quantizer and forming a negative feedback loop, as shown in Figure 2.5, the spectrum of the quantization noise can be high-pass shaped, and resulting in a noise-shaped modulator which is a most important block of ΔΣ converter. This type of modulator consists of a loop filter, an *m*-bit quantizer and an *m*-bit DAC. When noise-shaping and oversampling are combined, a significant improvement of SNR is achieved. A noised-shaped oversampled converter is called a ΔΣ converter. Figure 2.5 shows a basic structure of a ΔΣ modulator. By employing a linearized model for the quantizer and assuming the DAC is ideal, the linearized model for a first-order ΔΣ modulator is illustrated in Figure 2.6.

The linear model has two inputs: the input signal and the negative quantization result. The output thus can be represented in *Z*-domain as

$$Y(z) = H_x(z)X(z) + H_e(z)E(z), \tag{8}$$

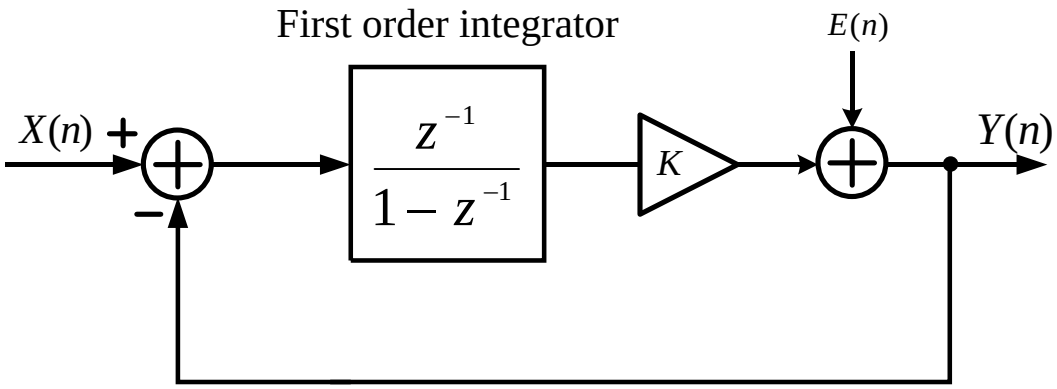


Figure 2.6 Linearized model for a first-order ΔΣ modulator.

where $Y(z)$, $X(z)$ and $E(z)$ are digital output, analog input signal and quantization error in Z-domain, respectively; $H_x(z)$ and $H_e(z)$ are the signal and noise transfer functions, respectively.

Suppose quantizer gain K is unity, the signal and noise transfer functions could be respectively represented as

$$H_x(z) = \frac{H(z)}{1+H(z)}, \tag{9}$$

$$H_e(z) = \frac{1}{1+H(z)}, \tag{10}$$

For a first-order low-pass loop filter where transfer function $H(z) = \frac{z^{-1}}{1-z^{-1}}$, the signal transfer function $H_x(z)$ and noise transfer function $H_e(z)$ can be respectively calculated as

$$H_x(z) = z^{-1}, \tag{11}$$

$$H_e(z) = 1 - z^{-1}. \tag{12}$$

This linearized model implies that the input signal directly passes through the loop filter, as the quantization error is suppressed by the loop filter and hence high-pass shaped. Figure 2.7 shows simulated loop filter, signal and noise transfer functions of a second-order canonical ΔΣ architecture, respectively.

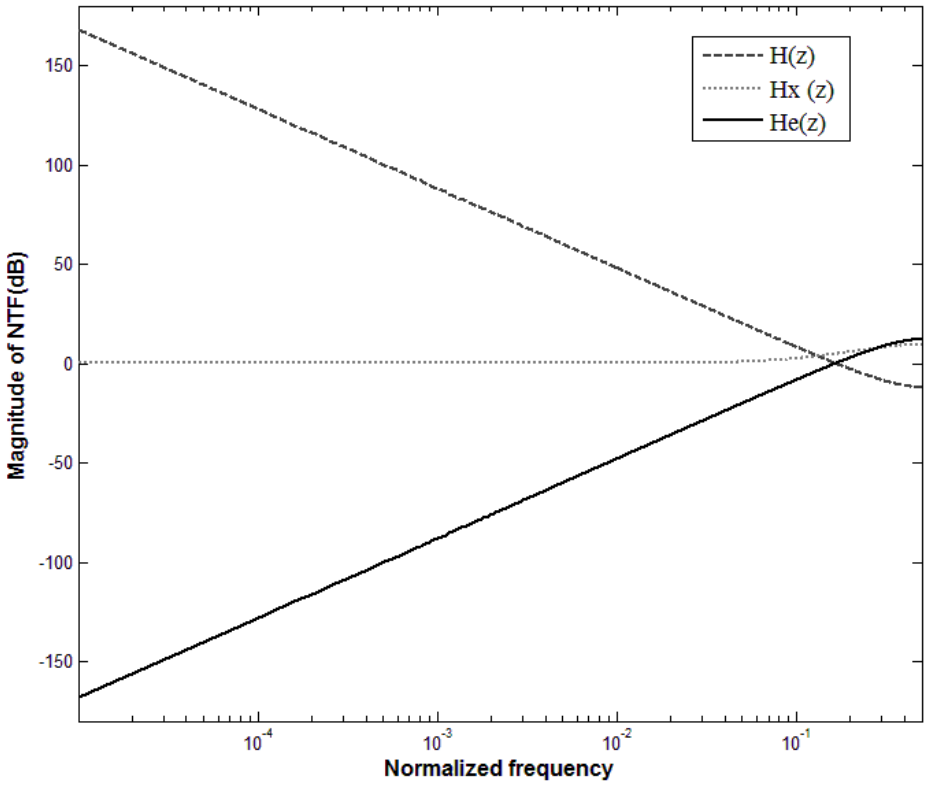


Figure 2.7 Transfer functions of a second-order canonical ΔΣ modulator.

2.4 ΔΣ ADC Topology

A number of alternative topologies exist which can perform noise shaping as discussed in the previous section. Single-loop topology reduces quantization noise by raising the order of the loop filter while cascade topology relies on the cancellation of quantization noise rather than aggressively shaping the quantization noise. This section is devoted to discuss several frequently used modulator topologies.

2.4.1 Distributed Feedback Topology

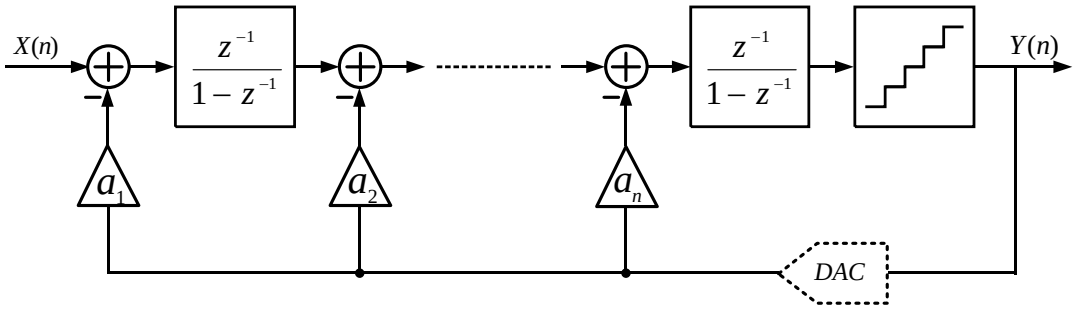


Figure 2.8 General diagram of a *N*-th order single-loop feedback topology.

Figure 2.8 shows a general block diagram of a *N*-th order single-loop ΔΣ modulator with distributed feedback. Since there is only one loop in the whole modulator, the ability of the noise shaping could be improved only by increasing the order of the loop filter. However, the stability considerations limit the maximum input signal range for high-order loops. The reason is that the higher loop-gain of the high-order loop filter causes overload of the quantizer [32]. The internal swings of each stage of this topology are dependent on amplitude of the input signal. This is because the input signal exists in each output stage. For example, the transfer function of a second-order of feedback topology is as follows

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2 E(z), \tag{13}$$

where $Y(z)$, $X(z)$ and $E(z)$ are the digital output, the input signal, and the quantization noise in *z*-domain, respectively. The linearized model shows that the outputs at each stage are

$$y_1(z) = z^{-1}(1 + z^{-1})X(z) - z^{-1}(1 - z^{-1})E(z), \tag{14}$$

$$y_2(z) = z^{-2}X(z) - z^{-1}(2 - z^{-1})E(z), \quad (15)$$

where $y_1(z)$ and $y_2(z)$ are the output signals of the first and second stages, respectively. From the above equations, we can clearly see that the output signals of two stages are the functions of the input signal $X(z)$. Signal swings at each stage exhibit large so that the implementation with low supply voltage is difficult. Moreover, the signal-dependent harmonics induced by the amplifier non-linearity reduce SNDR of the modulator.

2.4.2 Input-Feedforward Topology

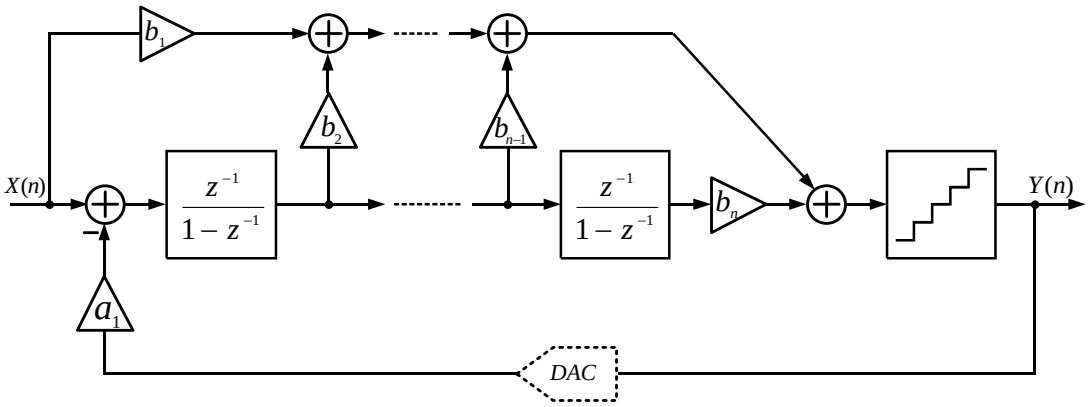


Figure 2.9 General diagram of a *N*-th order single-loop input-feedforward topology.

An alternative useful single-loop topology is input-feedforward, as illustrated in Figure 2.9. The distinguishing features of this topology are the direct feedforward path from the input to the quantizer and the single feedback path from the digital output. The transfer function of a second-order feedforward ΔΣ modulator topology can be represented as

$$Y(z) = X(z) + (1 - z^{-1})^2 E(z), \tag{16}$$

where $Y(z)$, $X(z)$ and $E(z)$ are the digital output, the input signal, and the quantization noise in *z*-domain, respectively. The output signals of each stage are as follows

$$y_1(z) = -z^{-1}(1 - z^{-1})E(z), \tag{17}$$

$$y_2(z) = -z^{-2}E(z), \tag{18}$$

where $y_1(z)$ and $y_2(z)$ are the output signals of the first and second stages, respectively. From equation (17) and (18), we can see that the $y_1(z)$ and $y_2(z)$ are free from the input signal $X(z)$, which means that the loop filter does not process the signal, thus the requirements on linearity of the amplifier might be considerably relaxed. Furthermore, with reduced signal amplitudes this topology eases implementation of analog building blocks with reduced supply.

2.4.3 Error Feedback Topology

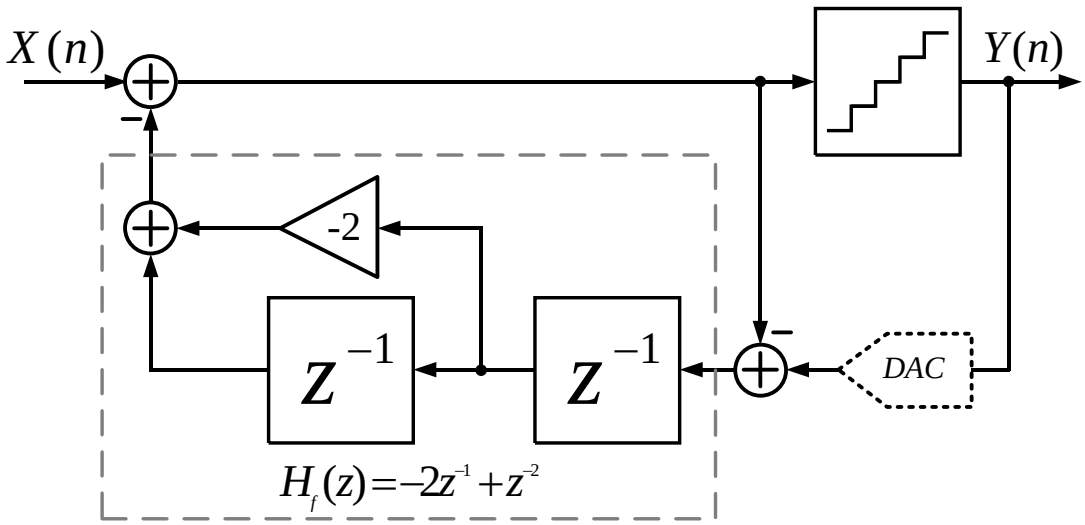


Figure 2.10 Second-order error feedback topology.

Figure 2.10 shows a second-order error feedback topology for simplicity. The key idea of the topology is to reconstruct quantization error. The topology subtracts the input of the quantizer from the output of DAC to obtain the quantization error in analog form. Then this error is fed back into a loop filter $H_f(z)$. Despite directly obtaining the quantization error, the topology is not practical for analog implementation, because it is very sensitive to variations of its parameters [33]. However, this topology can be used as the final stage combined with other topologies to enhance the noise shaping character [34].

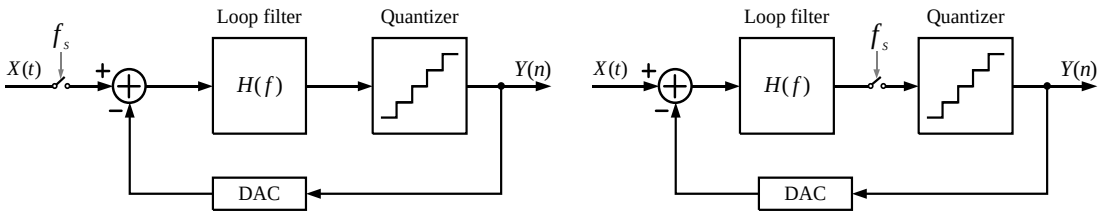
2.4.4 MASH Topology

The concept of multi-stage or MASH (Multi-stAge noise-Shaping) modulator is to extract the quantization error of the first stage for the input of the second stage, and then cancel it by employing digital filters at each stage. This topology has advantage that the stability character remains as that of low-order modulator while its shaping character exhibits like that of high-order modulator. However, the multi-stage topology suffers from match problem between stages. Therefore, it requires high accuracy for analog building block such as amplifier. For low-voltage application, this topology tends to result in higher power consumption [27, 35].

2.5 Circuit Implementation

As for circuit implementation of ΔΣ modulator, we usually employ discrete-time or continuous-time circuits. Discrete-time modulator differs from continuous-time

modulator in the place where input signal is sampled. As illustrated in Figure 2.11, in a discrete-time modulator, input signal is sampled at the input of the loop filter while it is sampled at the output of the loop filter in a continuous-time modulator. This results in significant difference in many aspects. First, continuous-time is prone to be affected by nonidealities, especially, clock jitter. Because the uncertainty of acquisition time directly affects the length of feedback signal and the uneven length of feedback signal might cause quantization noise leakage in the band of interest. Second, design method for discrete-time modulator is mature. Behavioral or analytical simulation might well predict stability as well as performance of discrete-time modulator. Third, discrete-time modulator requires much more switches than continuous-time modulator. For a low-voltage application, each individual switch may need a booster to acquire sufficient overdrive voltage and hence consume more power. Final, settling requirement for discrete-time modulator is much stringent than that of continuous-time modulator. Usually, gain bandwidth (GBW) of amplifier used for integrator in a discrete-time modulator should be at least five times of clock frequency [36]. In practice however, for a continuous-time modulator, it only needs two times of clock frequency [37].



(a) (b)

Figure 2.11 General block diagram of (a) DT and (b) CT ΔΣ modulator.

CHAPTER 3

DESIGN CONSIDERATION FOR LOW-VOLTAGE LOW-POWER CIRCUITS

Continuing down scaling of device geometry makes supply voltage declined. Reduced supply voltage with a relative higher threshold voltage has an important impact on circuits design. This chapter discusses low-voltage low-power issues related to switched-capacitor (SC) circuits and introduces low-voltage and low-power circuits design techniques.

3.1 Low-Voltage Low-Power Circuit Design Issues

3.1.1 Floating Switch Problem

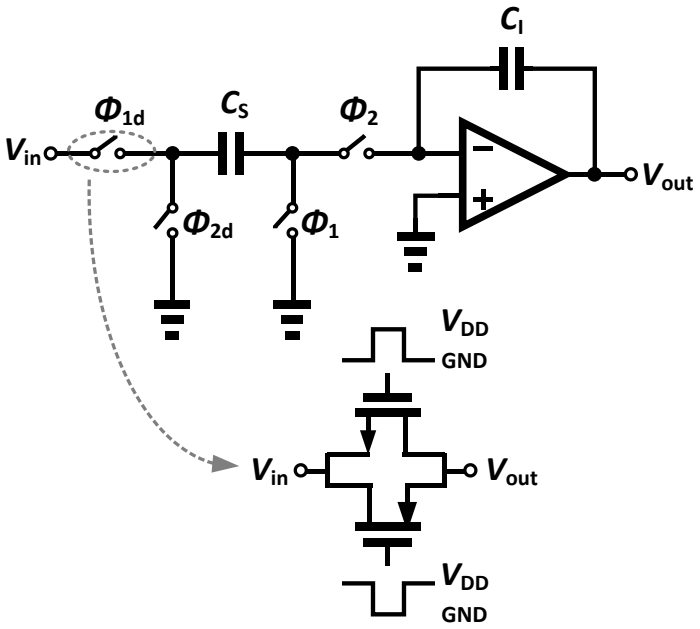


Figure 3.1 Floating switch in a typical SC integrator.

SC circuit is the most frequently used implementation for discrete-time system in CMOS technology. Figure 3.1 shows a typical SC integrator. The switch which connected between the input signal and the sampling capacitor is called floating switch. The operation of the SC integrator is as follows. During phase $\phi 1$, the input signal V_{in} is sampled into the sampling capacitor C_s through the floating switch. Ideally, the floating switch in the on-state should behave as a constant linear resistor. In practice however, the on-resistance of this switch varies with the input signal as shown in Figure 3.2. If supply voltage is large enough compared to the sum of the threshold voltages of PMOS and NMOS transistors, the on-resistance of the switch is approximately constant over the whole input signal range. However, if supply voltage approaches or less than the sum of the threshold voltages, both PMOS and NMOS transistors almost turn off in the mid-input signal range, and hence significantly increase resistance in this region. In order to have the on-resistance low enough, the gate-source voltage must be much larger than the sum of the input signal amplitude and the threshold voltage of the switch.

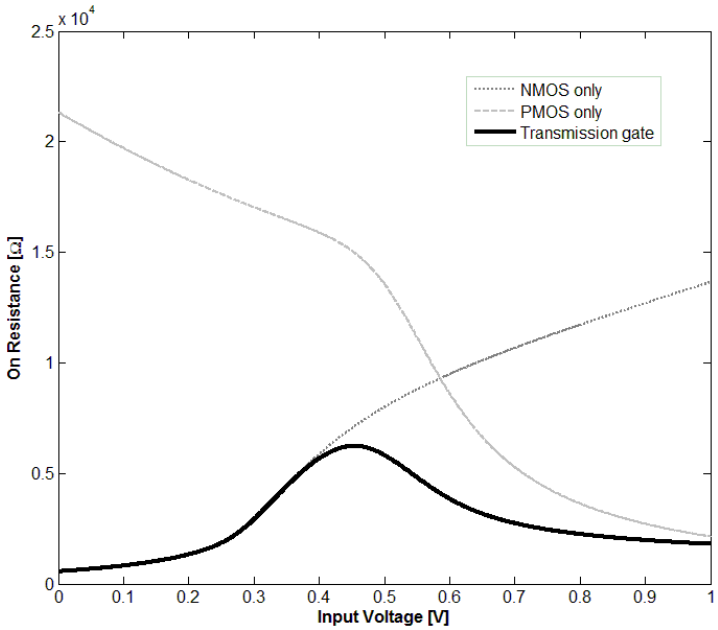


Figure 3.2 Simulated on-resistance of a transmission gate under 1-V supply voltage ($V_{th,n}$=438.2m, $V_{th,p}$=578.7m, W/L=1.2u/0.12u).

3.1.2 Intrinsic Noise

The most severe impact of reduced supply voltage is to limit input signal range, and hence reduce dynamic range. For SC circuits, in order to maintain dynamic range, we usually increase size of sampling capacitor to reduce thermal noise since the thermal noise does not related to supply voltage, i.e., KT/C . However, increased sampling capacitance dissipates more power. The trade-off between dynamic range and power consumption in a low-voltage design becomes more stringent. Besides thermal noise, for low-frequency applications such as biomedical and audio circuits, flicker noise with state-of-the-art CMOS technology becomes more important. This is because newer CMOS process employs thinner gate oxide and tends to have a higher corner frequency where flicker noise line and thermal noise line are crossed over in spectrum [38].

3.1.3 Leakage Current

In general, leakage current can be categorized into off-state drain leakage and on-state gate leakage based on biasing condition of transistor. The continuous scaling down of CMOS technology results in increase of leakage current. First, reduction of threshold voltage exponentially increases subthreshold leakage. Second, reduced gate oxide thickness increases gate edge-direct-tunneling leakage and gate-induced drain-leakage. Third, lightly doped-drain also exponentially increases bulk band-to-band-tunneling leakage [39]. Leakage current, especially off-state drain leakage, can substantially increase total power consumption. Therefore, for low-power circuits such as memory and mobile system, leakage current reduction is very important technique in circuit

design [40, 41]. To prevent from leakage, state-of-the-art technologies may implement a low-power process which features relative higher threshold voltage.

3.1.4 Intrinsic Gain

Reduced effective gate length makes the charge sharing between gate and source or drain more severe, and thus allow the voltage drop between drain and source V_{ds} control drain current apparently. The unexpected control of V_{ds} results in considerable reduction of output impedance r_o of transistor. Although transconductance g_m of each newer generation has been enhanced, the intrinsic gain of state-of-the-art transistor which equals to $g_m r_o$ declines. Reduced supply voltage even makes this worse. This is because reduced supply voltage severely squeeze V_{ds}, so that push transistor move into linear region and thus reduce r_o further.

3.2 Low-Voltage Circuit Design Techniques

3.2.1 Body-Driven Technique

Usually, body terminal is connected to source or ground to eliminate body effect which may increase threshold voltage. However, when gate input is substituted by body input, supply voltage can be substantially reduced due to the fact that the input range for body input is much larger than that for gate input. Body-driven technique demonstrates a possibility to work with very low supply voltage [42-44]. However, this technique suffers from several limitations compared to conventional gate-driven circuits. First, body input exhibits lower transconductance, DC gain, gain-bandwidth

(GBW) and larger power for same load capacitance. Second, input impedance declines while body input may draw current from signal source. This fact tends to create parasitic bipolar transistor which might result in a latch-up problem. Third, due to low transconductance body-driven circuits may suffer from larger thermal noise and hence degrade system performance. Final, this technique is process related. For most cases, only PMOS transistor is applicable for body-driven technique because P-WELL is not available.

3.2.2 Charge Pump Technique

Due to low supply voltage the overdrive voltage for transistor is often insufficient to transmit signal. Therefore, charge pump technique is frequently employed in low-voltage circuit design. Boosted clock and bootstrapped switch [45-47] are two common used implementations. The former doubles amplitude of clock signal to increase the overdrive voltage for switch while the latter provides a constant gate-source voltage V_{gs} to gain better linearity. Figure 3.3 shows a conceptual diagram of bootstrapped switch.

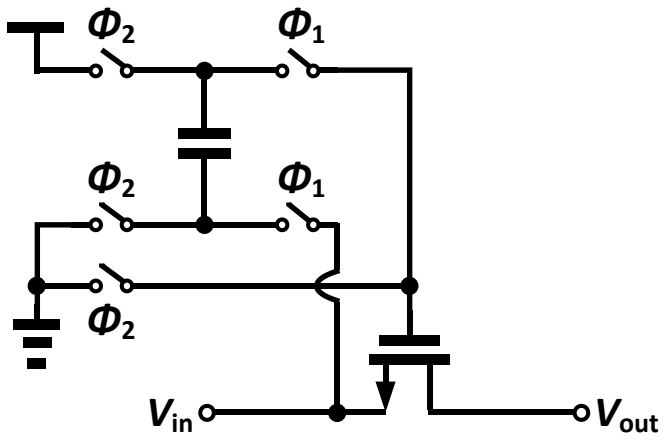


Figure 3.3 Conceptual diagram of bootstrapped switch.

3.2.3 Switched-Opamp Technique

In order to solve floating switch problem, switched-opamp [48-52] is proposed to eliminate the floating switch, as illustrated in Figure 3.4. In preceding stage, output stage and bias of the miller-compensated opamp are switchable. When these switches are on, the opamp operates like a normal two-stage opamp. When these switches are off, the opamp stop to work and the output node is floating. This technique is compatible with SC circuits and might operate with low supply voltage. When the opamp stops to work, ideally, quiescent current declines to zero and power could be saved. However, switched-opamp might need a long time to recover from an idle state, and thus may be unsuitable for high speed applications.

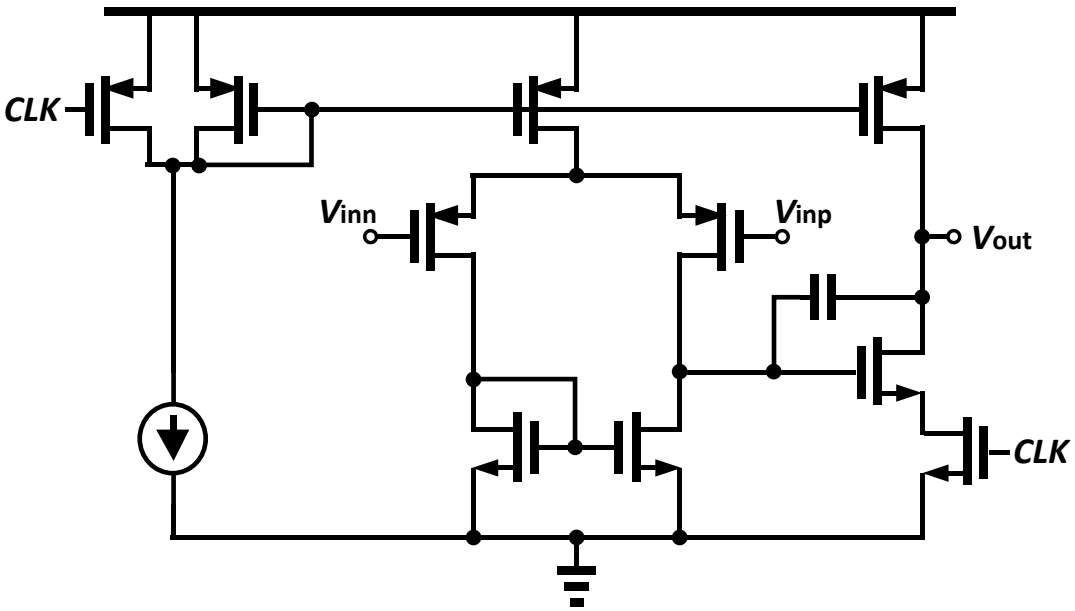


Figure 3.4 Two-stage miller-compensated switched opamp.

3.2.4 Switched-RC Technique

An alternative way to solve the floating switch problem is switched-RC technique [22, 27, 53, 54]. As shown in Figure 3.5, using a constant resistor to replace the floating switch not only improves linearity of the input sampling network, but also avoids insufficient overdrive voltage. This technique is also suitable for low supply voltage and very easy to realize. However, this constant resistor inevitably reduces output impedance of preceding stage and thus requires high DC gain for previous amplifier. Moreover, output load of the preceding stage is severely affected by the sampling state [27].

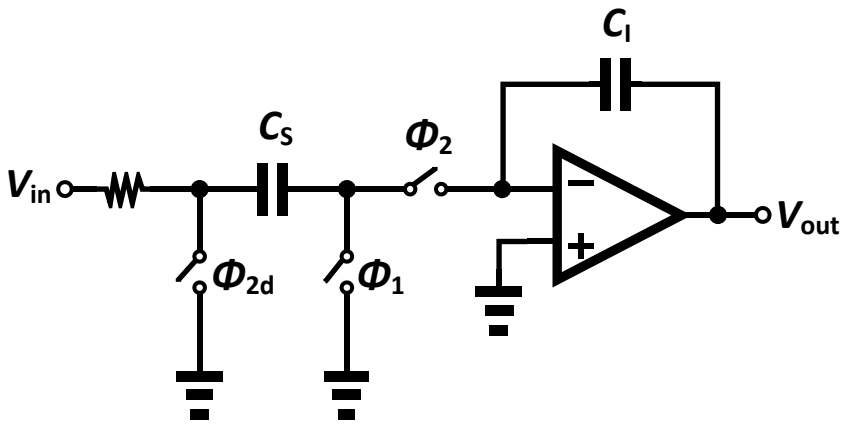


Figure 3.5 Switched-RC integrator.

3.3 Low-Power Circuit Design Techniques

3.3.1 Double Sampling Technique

As illustrated in Figure 3.6, the amplifier in the double-sampled integrator is utilized in both phases and thus the effective sampling rate is twice of that of conventional

single-sampled integrator. Double sampling technique has advantages that for a given sampling rate the clock frequency can be halved and hence power consumption of integrator is minimized [22, 55-58]. Another benefit of this technique is symmetrical equivalent load for the integrator. The same load avoids ringing in one phase. In practice however, due to mismatch between two sampling capacitor high frequency noise might easily fold down into baseband and hence increase noise floor [55].

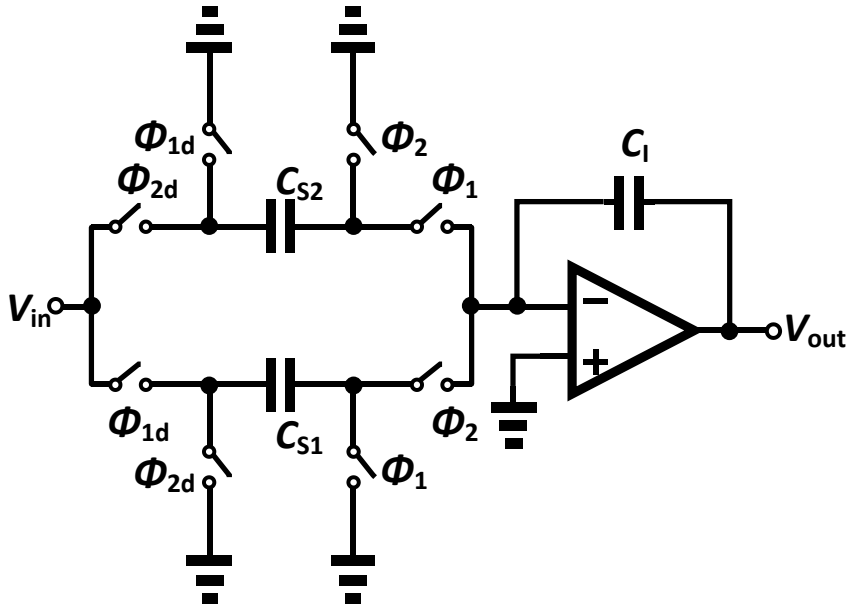


Figure 3.6 Double-sampled SC integrator.

3.3.2 Time-Sharing Technique

In order to minimize power consumption, analog building blocks such as amplifier, comparator might be shared within different clock period [14, 59-61]. The time-sharing technique reduces the number of analog building blocks and hence total chip area. Since number of analog building block is significantly reduced, mismatch problem between each cell is alleviated. For example, using one comparator instead of

multi-comparator in a multi-bit quantizer avoids performance degradation due to mismatch between each comparator [14].

However, these remaining analog building blocks operated within reduced time space may need higher gain-bandwidth, slew rate. Moreover, control logic for the time-shared circuit might become more complicated.

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CHAPTER 4

A 0.7-V 100-μW AUDIO MODULATOR WITH 92-dB DR IN 0.13-μm CMOS

This chapter demonstrates an example of low-voltage low-power ΔΣ modulators for audio-band applications. This prototype is a fourth-order single-bit input-feedforward ΔΣ modulator operated from a 0.7-V supply voltage while consuming 99.7 μW. The modulator has been fabricated in a 0.13-μm CMOS process and exhibits high figure-of-merits among audio-band sub-1 V low-power ΔΣ modulators based on measured results. The modulator utilizes a 2-tap finite-impulse-response (FIR) filter in the feedback path to reduce integration step of the first stage, resulting 22% reduction in the maximum integration step and relaxing the slew rate requirement for the first opamp to 9.5 V/μsec (diff). It also simplifies circuit implementation by embedding feedforward path in a multi-input comparator.

4.1 Introduction

The growing demands for fully integration of data converters and digital signal processing circuits make data converters migrating towards deep-submicron CMOS technologies. However, in contrast with digital circuits, which have gained higher power efficiency, higher area density and more powerful functions from smaller geometry of transistor size and lowered supply voltage, data converters are most likely to have its performance degraded due to the lowered supply voltage and worse

transistor characteristics. The first problem confronted is the lowered supply voltage. To ensure the reliability of transistor, the supply voltage is forced to decline in deep-submicron technologies. However, the dynamic range of analog circuits is restricted by signal swing, which is limited by supply voltage. Thus, the reduced signal power makes the input network to have a larger sampling capacitor to reduce the noise floor in a discrete time system for a desired signal-to-noise ratio (SNR). Increasing capacitor size is most likely to raise power consumption. In terms of power consumption, analog building blocks tend to increase with the decrease of supply voltage for a given SNR. One method of keeping high available SNR accompanied with low level of the total power consumption is to separate the power line of analog and digital circuits, as in [62]. Since the rated supply voltage of state-of-the-art process already shrinks to around 1 volt, the supply voltage difference between these two parts is not very big to effectively reduce total power consumption, and it would be at the cost of more noise coupling and electromagnetic interface [22]. Besides lowered supply voltage, the impact of scaling down of CMOS technologies on analog building blocks is not ignorable; and the most prominent problem is DC gain degradation of amplifiers. Several multistage amplifiers topologies, such as three-stage with nested g_m-C compensation [63], are employed to alleviate this degradation. However, multistage amplifiers in a low-voltage environment are difficult to design and most likely to be inferior to single-stage one in terms of power efficiency. Fortunately, the degradation of analog building blocks can be mitigated at the system level; and it will be discussed later.

A multi-bit single-loop ΔΣ topology employed in low-voltage, low-power audio-band modulator with high precision is reported in [14]. However, the main drawback of

multi-bit topology is the complicated digital circuits and its increased power dissipation. Flash ADC based quantizer doubles the number of comparators for each one bit increased of the quantizer, and appears power hungry. The more power-efficient successor, comparator-based tracking quantizer [59, 64], though save more power, but suffers from excessive loop delay [14]. Besides the multi-bit quantizer, the dynamic element matching (DEM) circuits, which used to suppress tone and nonlinearity induced by the capacitor mismatches of the feedback digital-to-analog converter, are also a power hungry part. As far as power efficiency is concerned, single-bit single-loop topology is proved to be more suitable for low-power applications.

Continuous-time ΔΣ modulators are usually applied in wideband applications. Its attractive feature is low-power consumption and relaxed requirement of unity-gain-bandwidth for amplifier compared with discrete-time counterpart. However, it is very prone to be affected by clock jitter and the jitter requirement is much stringent than that of discrete-time ΔΣ modulators [65]. For high precision reasons, switched-capacitor circuitry is more popular and suitable in low-voltage audio band applications.

This section presents a fourth-order SC audio-band ΔΣ modulator. To relax the design requirement for analog building blocks and reduce power consumption, single-loop single-bit feedforward topology with a 2-tap FIR filter is adopted in the work. A multi-input comparator is employed in the quantizer to fulfill the combined function of summation and quantization; hence the conventional feedforward capacitors can be removed.

The section is organized as follows: section 4.2 describes the system architecture of the low-voltage low-power ΔΣ modulator. The detailed circuit design of the analog building blocks is presented in sections 4.3. Section 4.4 reports the measurement results, and the conclusion is drawn in Section 4.5.

4.2 System Design

The second-order single-loop feedforward topology for broadband and low-distortion applications has been firstly presented in [66], as shown in Figure 4.1. Compared with the conventional feedback topology, the unique features make it a perfect candidate for low-voltage ΔΣ analog-to-digital converters. Firstly, the signal transfer function of this topology is unity, which is less affected by the non-idealities of the building blocks. The quantization noise transfer function remains the same as the classic topology, a single loop topology without the feedforward. Secondly, the internal signal swing can be well controlled by optimizing the loop coefficients. Besides, there is only one feedback path to the first integrator, which simplifies the feedback circuit compared to the conventional topology.

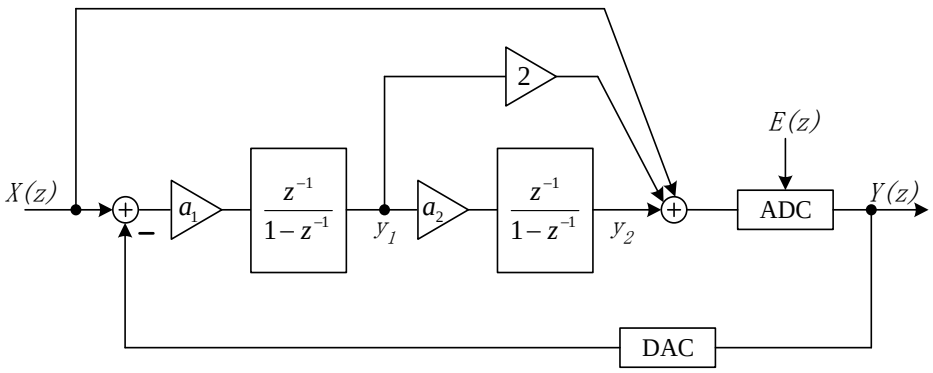


Figure 4.1 Second-order single-loop feedforward topology.

For single-loop single-bit topology realized by switched-capacitor circuitry, the power consumption is mainly determined by the size of capacitors. Thanks to the noise suppression inside the loop, all capacitors with the exception of that in the first stage can be scaled down to save power [32]. Indeed, several low-voltage low-power ΔΣ modulators show that the first stage dominates the total power dissipations [19, 22, 67]. However, the thermal noise induced by input switched-on resistance is also determined by the sampling capacitor of the first stage. Thus, there is a tradeoff between power consumption and SNR in a thermal noise dominant ΔΣ system.

High power-efficient low-voltage low-power ΔΣ modulators always exploit power-efficient amplifiers. Such amplifiers usually have class-AB output or simply consist of only a class-C inverter [20, 67, 68]. Both class-AB output and class-C inverter have similar attribute with digital circuits, which power consumption is proportionally to the switching activity. In terms of integrators, the power consumption is closely related to the integration step. From the linear model shown in the Figure 4.1, the output swing of the first stage and the integration step is derived as following:

$$y_1 = -a_1 z^{-1}(1 - z^{-1})E(z), \tag{19}$$

$$\Delta_1 = \left| y_1(z) - y_1(z)z^{-1} \right| = \left| a_1 z^{-1}(1 - z^{-1})^2 E(z) \right|. \tag{20}$$

Equation (20) shows that either integration gain of the first stage, or quantization errors, or both can be minimized to reduce integration step.

From system perspective, the selection of the coefficient or the integration gain of the first stage is important to affect the power consumption of the first stage. When the integration gain increases, not only the integration step, but also the output signal

swings would increase proportionally. This would lead to penalty in terms of slew rate and DC gain of amplifier. However, too small integration gain would be at the cost of large capacitor spread. If a desired sampling capacitor is fixed or for a given SNR, the integration capacitor would be very large with small integration gain. Although several approaches have been reported to deal with the capacitor spread problem, such as T-network scheme [69] and charge-discharge-redistribution scheme [70], they are not likely chosen to serve for the sampling network. The main reason is the extra thermal noise induced by the additional switches and the added clock noise.

The quantization error is explicitly reduced by multi-bit topology, and is reversely proportional to the number of quantization level. But this is a power-hungry choice for low-power application for the reasons described above. An alternative way to reduce the impact of the quantization error is using a FIR filter to chop off the most power of the quantization errors centered at $f_s/2$ [71, 72]. This method does not incur any non-linearity from the feedback DAC and requires no DEM circuits. Furthermore, the residual error at the input of the first stage is reduced. Thus, the integration step is reduced. Figure 4.2 illustrates a conceptual diagram of reduced residual error by a 2-tap comb FIR filter DAC. A 2-tap FIR filter raises the level of a 1-bit quantizer to that of a 1.5-bit quantizer, and minimizes the residual errors.

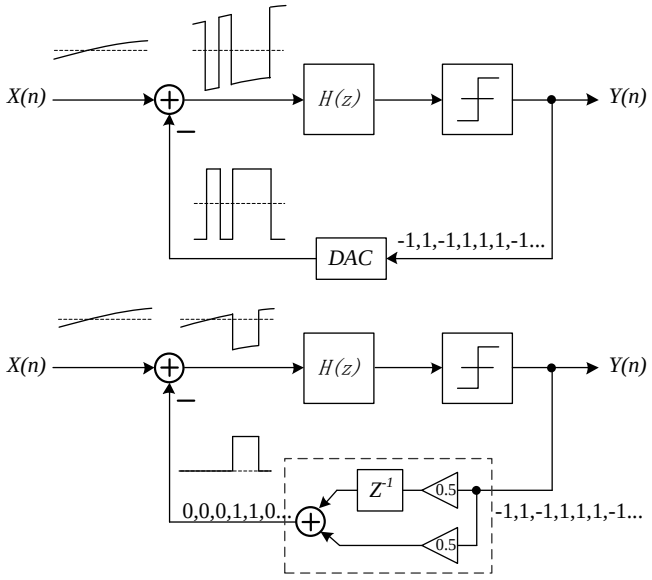


Figure 4.2 Conceptual operation of a 2-tap FIR filter.

According to the behavior simulation, the output swings of the first stage are slightly affected by FIR filters, as shown in Figure 4.3. The integration step declined dramatically with the increase of length of tap of the filter, as shown in Figure 4.4. However, the increased length of tap would be at cost of complexity of compensation network. Thus, for simplicity reasons, a fourth-order single-bit feedforward architecture with a 2-tap comb FIR filter is adopted in the work, as shown in Figure 4.5. After introducing a FIR filter in the feedback path, two extra feedback paths are needed to be added to the input of the second integrator and the input of the quantizer to avoid stability problem or performance loss for the changes at the output of the first integrator. Behavior simulation result shows that the maximum integration step is reduced by 22% and the accumulated integration step is only 58% of that without the filter.

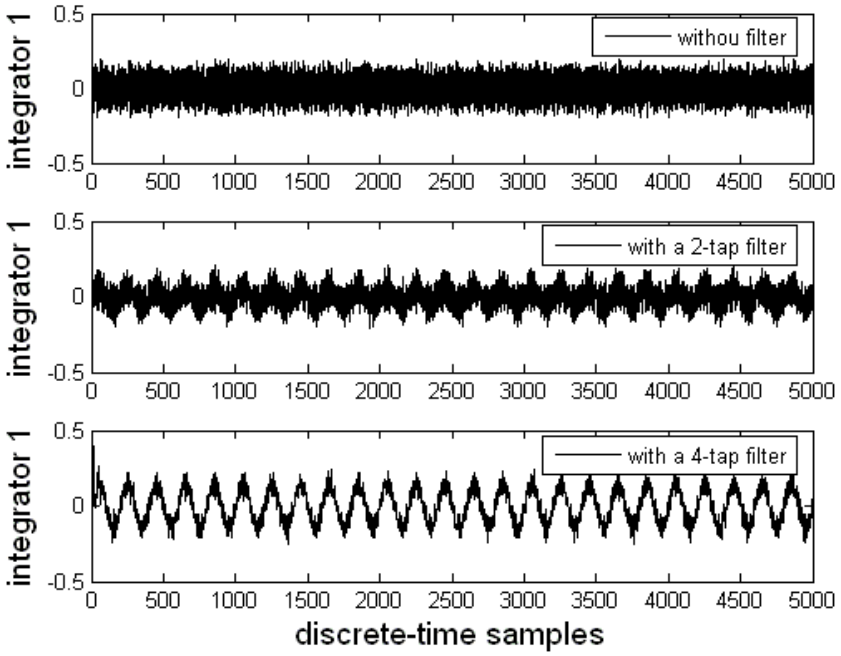


Figure 4.3 Output signal swings of the first integrator with/without a FIR filter.

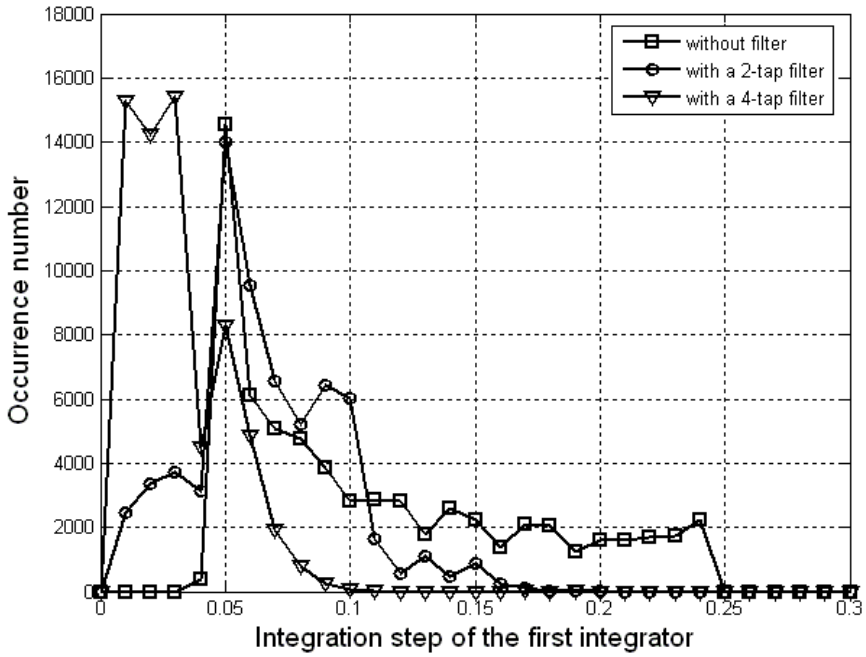


Figure 4.4 Histogram of integration step of the first integrator with/without a FIR filter.

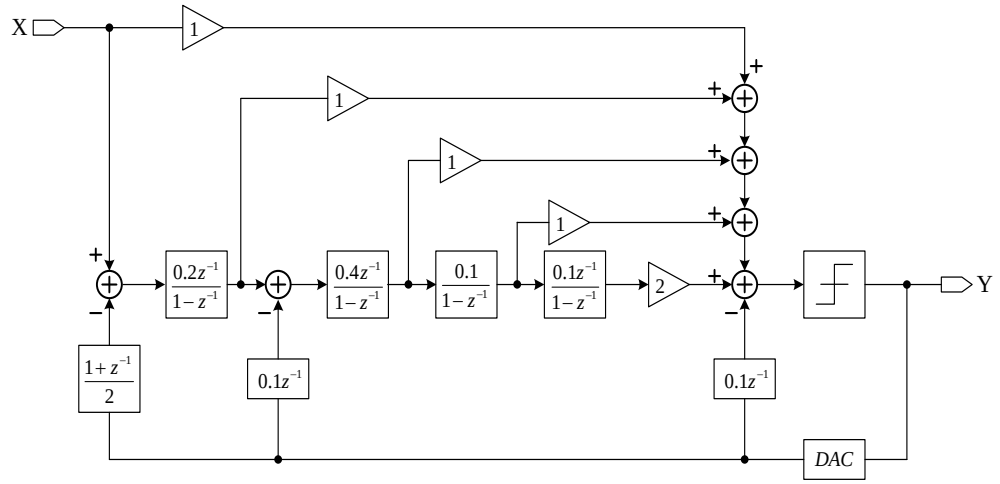


Figure 4.5 System diagram of the ΔΣ modulator.

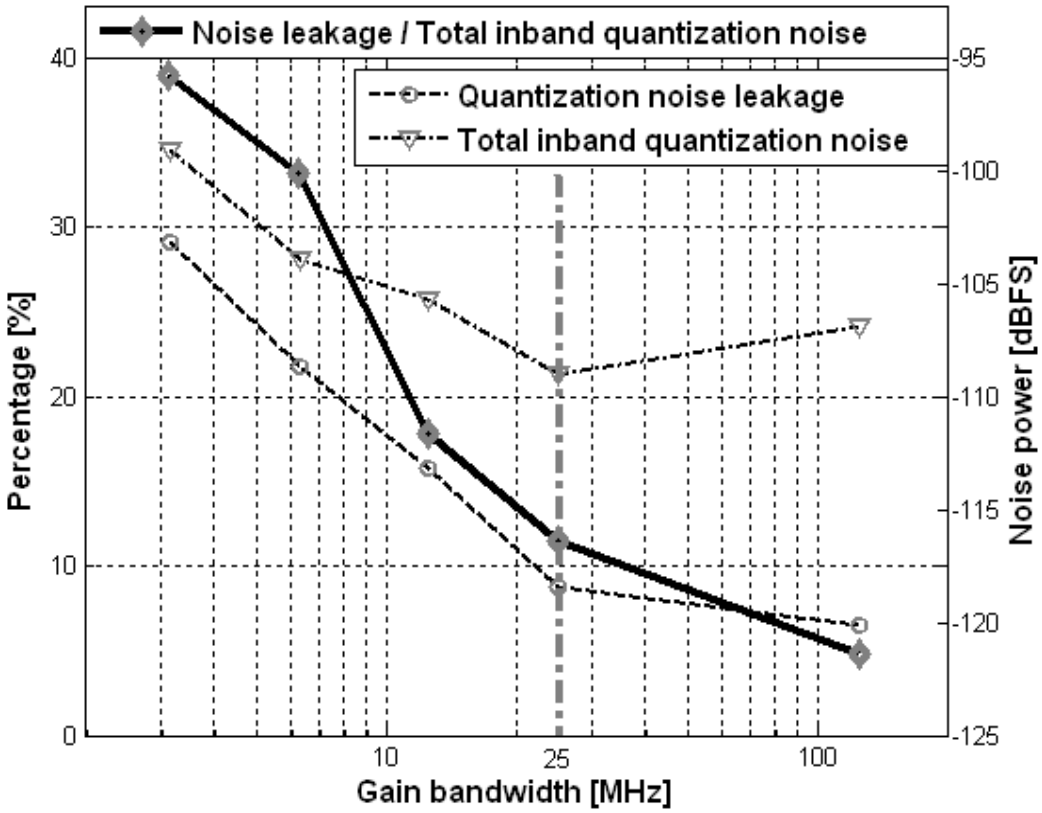


Figure 4.6 Percentage of noise leakage over total in-band quantization noise versus the first opamp's GBW.

Prediction of leakage of the quantization noise is important for achieving desired performance in low-voltage low-power ΔΣ modulator design. Existing behavioral simulation does not provide a good prediction on the noise leakage while full

transistor level simulation prolongs entire design process. To address this issue, we use a mixed-mode simulation for leakage prediction, which is flexible and less time consuming. Under the mixed-mode simulation, all building blocks are based on transistor level design, except for opamps which are modeled by small signal models. For the first stage, the opamp is modeled as a fully differential one by voltage-control-current-sources (VCCS) and resistors. For opamps in the downstream stages, they are modeled by voltage-control-voltage-sources (VCVS) to save simulation time since non-idealities of the downstream integrators have little effect on the leakage.

In order to estimate the quantization noise leakage, we separate the unshaped quantization noise from the shaped one for evaluating the leakage power. The leakage power is evaluated by accumulating the quantization noise spectrum within a half of signal band, i.e. 10 kHz, under different gain bandwidth (GBW) settings of the first stage opamp. Figure 4.6 shows the percentage of noise leakage over total in-band quantization noise versus the first opamp's GBW, where the DC gain is fixed at 35 dB. It can be seen that the noise leakage due to the opamp bandwidth contributes more than 30 % to the the total in-band quantization noise when the GBW is below 6 MHz. When the GBW is above 25 MHz the noise leakage declines slowly and occupies less than 12 % of the total. We can clearly see that the noise leakage degrades SQNR by more than 5 dB when the GBW is reduced from 25 MHz to 6 MHz. The DC gain does not have clear influence on the leakage. When the GBW is fixed at 25 MHz, the leakage is almost constant when DC gain increases from 29 dB to 41 dB. For achieving a better SNR, it is desirable to let GBW of the first opamp reasonably high so that the noise leakage can be minimized.

4.3 Circuit Implementation

Analog building block is a key element in low-voltage low-power ΔΣ modulator. All switches are implemented with bootstrapped switches to increase linearity in a low-voltage environment. Two non-overlapped signals are generated from the on-chip clock generator.

4.3.1 Two-Tap FIR DAC

Figure 4.7 shows the signal timing diagram of the feedback signal and the first stage output. The quantizer resolves a comparison at the end of ϕ_2. Within one clock period, the integration of the first stage occurs twice in both ϕ_1 and ϕ_2, respectively. According to the time domain, at the end of ϕ_1,

$$V_{o1}\left(n-\frac{1}{2}\right) = V_{o1}(n-1) + [X\left(n-\frac{1}{2}\right) - fb(n-2)] \times 0.1. \quad (21)$$

At the end of ϕ_2,

$$V_{o1}(n) = V_{o1}\left(n-\frac{1}{2}\right) + [X\left(n-\frac{1}{2}\right) - fb(n-1)] \times 0.1, \quad (22)$$

where $V_{o1}(n)$ is the output of the first stage, $X(n)$ is the input signal, $fb(n)$ is the feedback signal. Adding (4.3) to (4.4) and taking z-transfer transform on the sum, we have

$$V_{o1}(z) = V_{o1}(z)z^{-1} + X(z)z^{-0.5} - 0.2 \times fb(z)z^{-1}[\frac{1+z^{-1}}{2}]. \quad (23)$$

We can clearly see from equation (23) that the feedback signal has been filtered.

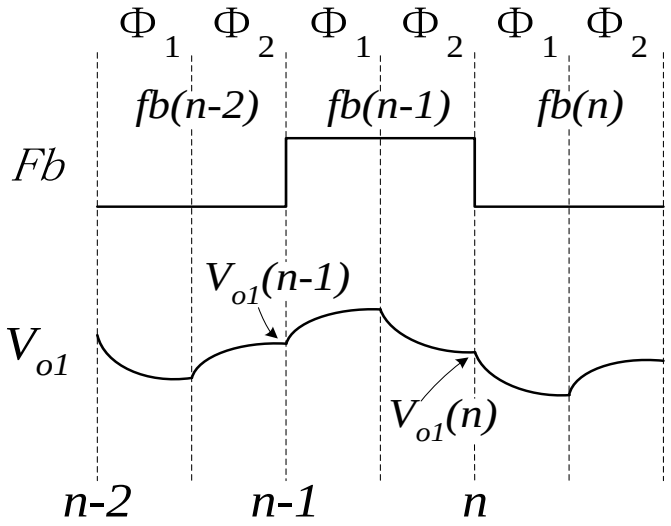


Figure 4.7 Signal timing diagram of the feedback signal and the first stage output.

4.3.2 Power-Efficient Rail-to-Rail Amplifier

As CMOS technologies are migrating towards the deep-submicron, the intrinsic gain of a transistor shrinks dramatically. With lowered supply voltage this condition becomes even worse. However, high-gain amplifier which employed in a low-voltage environment is difficulty to design, and have to exploit two or three stages cascade topology. Thanks to the oversampling feature of ΔΣ converters, the requirements of amplifier are not stringent as that of amplifiers which employed in Nyquist rate's converters, such as pipeline converters. Moreover, the reduced signal swings at the internal nodes of feedforward topology make the requirements relaxed much more. These two factors make even an inverter served as an amplifier [13]. As shown in Figure 4.8, this work exploits single-stage fully differential gain-enhanced current mirror OTA. It offers specific advantages in a low-voltage environment, such as low minimum required supply voltage, rail-to-rail output swing and high power efficiency. The process used provides the possibility of optimizing the threshold voltage of the

transistors due to the reverse short-channel effect. The minimum required supply for the OTA is restricted by the input stage, which is $3|V_{ds,sat}|+|V_{TH}|$. By optimizing the threshold voltage of the PMOS diode-connected transistor to 0.2 V and designing $|V_{ds,sat}|$ to be 0.1 V, the minimum supply voltage of the OTA is only 0.5 V. NMOS input differential pairs are used to increase the transconductance efficiency. To ensure good distortion suppression, the gain enhancement technique is adopted to increase the OTA DC gain while most parts of the current in the PMOS diode-connected transistors are shunted by a current source. The simulated DC gain and GBW for the OTA in the first integrator are 41 dB and 21 MHz with a 3-pF load capacitor, respectively. Switched-capacitor common-mode feedback circuit is used in the fully differential OTAs to set the output common-mode at the middle of the supply, while the input common-mode of the OTAs is set to 0.3 V.

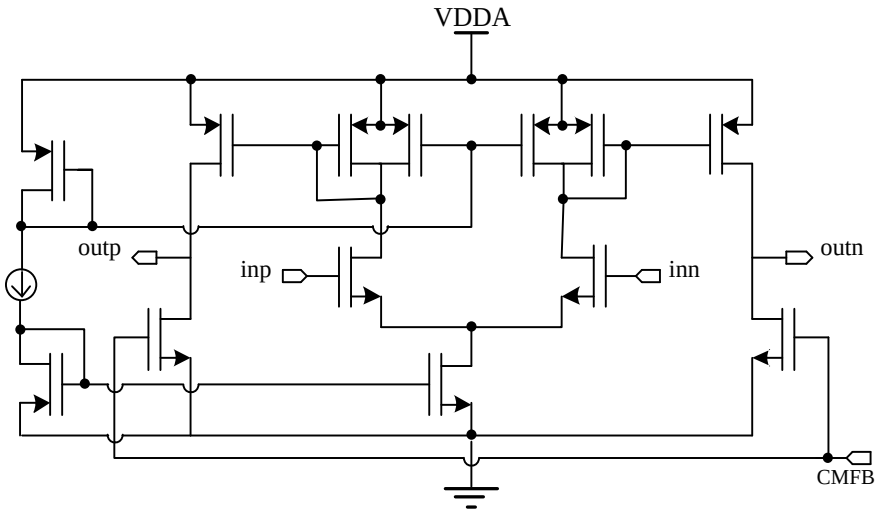


Figure 4.8 Gain-enhanced current mirror OTA.

Flicker noise is a dominant noise in low frequency region. Several approaches have been reported to deal with this problem, such as chopper stabilization technique and correlated double sampling. However, both of them suffer some limitations. Chopper

stabilization technique belongs to a modulation method; it might be at the risk to modulate shaped high-frequency quantization noise back down to the baseband, thus couples additional noise to the baseband [62]. Correlated double sampling belongs to a sampling method; it would lead a penalty of additional thermal noise and coupling clock noise induced by added switches in the sampling front-end. For simplicity reasons, we simply increase the geometric sizes of input transistors to suppress flicker noise.

4.3.3 Multi-Input Comparator

Conventionally, the summation of the feedforward paths is realized by a switched-capacitor summation circuit shown in Figure 4.9a, which requires $2 \times (N + 1)$ capacitors and extra switches for an Nth-order topology. In the proposed circuit implementation, the summation function is embedded in the quantizer [73]. The quantizer consists of a multi-input comparator and a SR latch. The feedforward paths are implemented by directly feeding the input signal and the output of each integrator to the comparator, as shown in Figure 4.9b. When CLK is low, the comparator is inactivated. The internal nodes X, Y are pulled down to GND, thus, $V_X = V_Y \approx 0$. And all input transistors are pushed into the linear region. Once $V_{GS} > V_{THN}$ is validated for all input transistors. The current at X and Y is derived as:

$$I_X = \sum_{i=0}^{4} I_i = \mu_n C_{ox} \sum_{i=0}^{4} (\frac{W}{L})_i (V_{oi+} - V_{THN} - \frac{V_X}{2})(V_X), \quad (24)$$

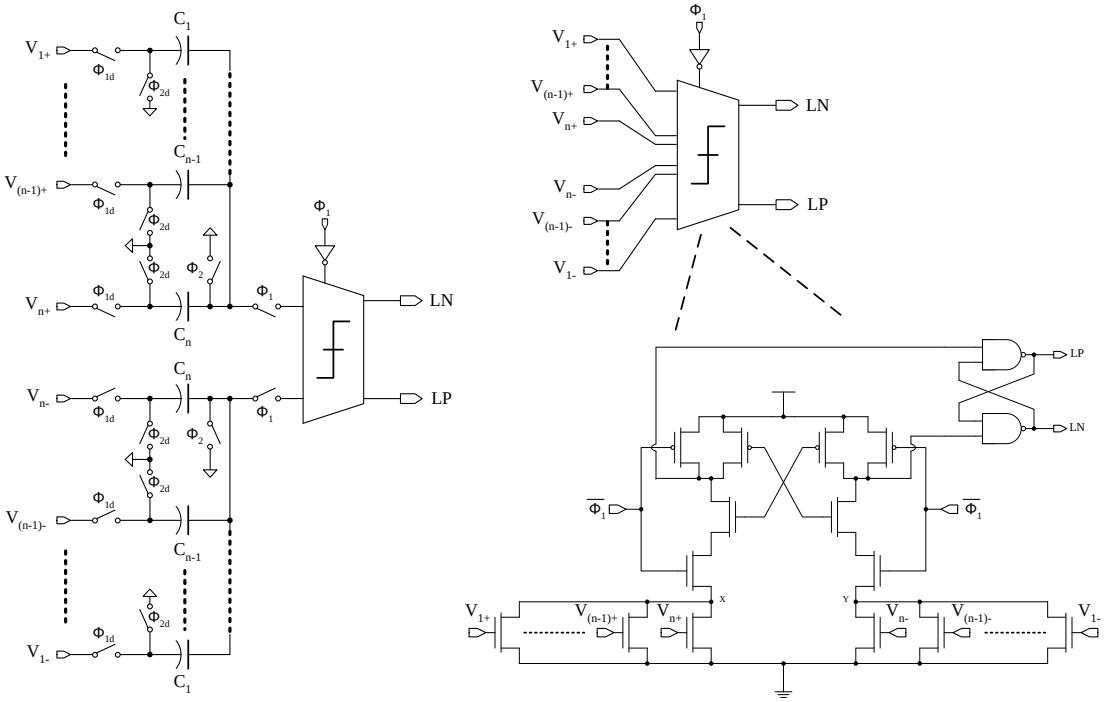
$$I_Y = \sum_{i=0}^{4} I_i = \mu_n C_{ox} \sum_{i=0}^{4} (\frac{W}{L})_i (V_{oi-} - V_{THN} - \frac{V_Y}{2})(V_Y), \quad (25)$$

where V_{THN} is the threshold voltage of all input transistors.

When CLK is high, the comparator starts to sense the difference between *IX* and *IY*. Since all input transistors are initially operated in the linear region when the comparator is activated, the difference between *IX* and *IY* is linearly proportional to the difference between the sums of the input signals of both sides. That is

$$I_X - I_Y = \mu_n C_{ox} V_X \sum_{i=0}^{4} \left(\frac{W}{L}\right)_i (V_{oi+} - V_{oi-}) \qquad (26)$$

The linear relationship between $(I_x - I_y)$ and $(V_{oi+} - V_{oi-})$ in equation (26) indicates that the ratio of $\left(\frac{W}{L}\right)_i$ can be used to realize the feedforward coefficients in Figure 4.5. This difference is then amplified by the regenerative circuit to reach the level of the final outputs.



(a) Conventional switched-capacitor summation circuit.

(b) Proposed multi-input comparator-based quantizer.

Figure 4.9 Different implementation techniques of the feedforward paths.

4.4 Measurement Results

The prototype fourth-order feedforward ΔΣ modulator is fabricated in a 1P8M 0.13-μm CMOS process with MIM capacitor. The core area is 1.27×0.55 mm^2. Figure 4.10 shows the chip micrograph. And the chip is packaged in a 28-pin QFN package.

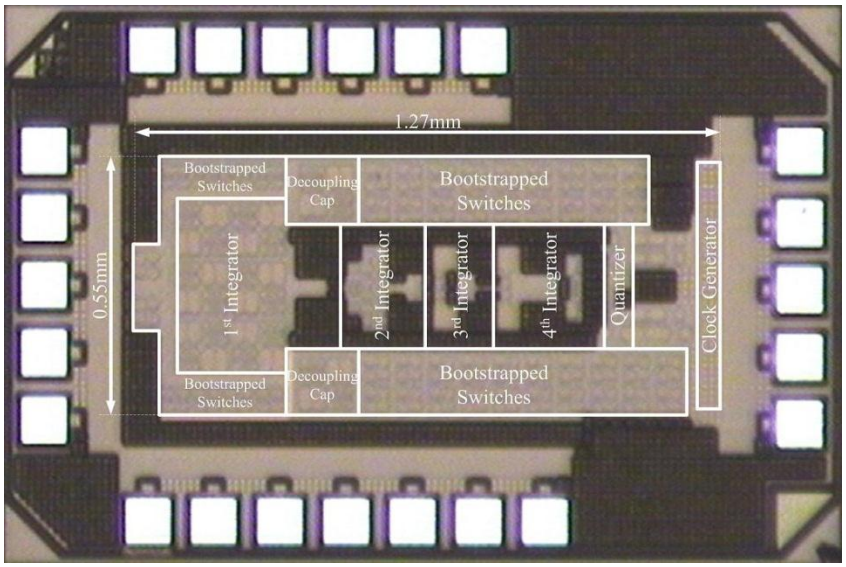


Figure 4.10 Chip micrograph.

4.4.1 Measurement Setup

Low distortion function generator SRS DS360 is served for input signal. Unfortunately, the in-band rated noise power is slightly higher, and would affect the accuracy of the SNR measurement. The specifications details that the rated maximum white noise voltage is 15 $nV/\sqrt{Hz}$ for a 1 kHz sine wave into Hi-Z load with maximum 1.26 Vpp [74]. The maximum in-band noise power is calculated by

$$P_{no,in} = BW \times (Noise\_Voltage)^2 = 20kHz \times \left(15nV/\sqrt{Hz}\right)^2 = 4.5(\mu V)^2,$$

The in-band thermal noise power by KT/C is

$$P_{no,KT/C} = \frac{KT}{C_S \times OSR} = \frac{1.38\times10^{-23}\times300}{6\times10^{-12}\times100} = 6.9(\mu V)^2.$$

Considering two sampling capacitors separately integrated in two consecutive phases, the in-band thermal noise power would be doubled. Thus, the in-band noise induced by the function generator is 32.6% of that by KT/C. Of course, the in-band KT/C noise power is not the total in-band power. But it dominates or occupies at least half in the total in-band power according to the theoretical analysis [33]. Furthermore, the white noise power induced by the function generator would increase with the increase of input signal frequency [75]. Thus, it is worth to attenuate it. A first-order low-pass RC filter is adopted in the test setup. The -3dB cutoff frequency of the filter is designed around 6.3 kHz to attenuate the most white noise power and make the passed sine wave can be clearly plotted with 64-k sample points. The resistance of the filter is the output resistance of the function generator. When it set to Hi-Z load, the output resistance is 25 Ω.

Figure 4.11 shows the printed circuit board (PCB) for testing this chip. Cares have been taken in designing the PCB to minimize the noise coupled from the supplies.

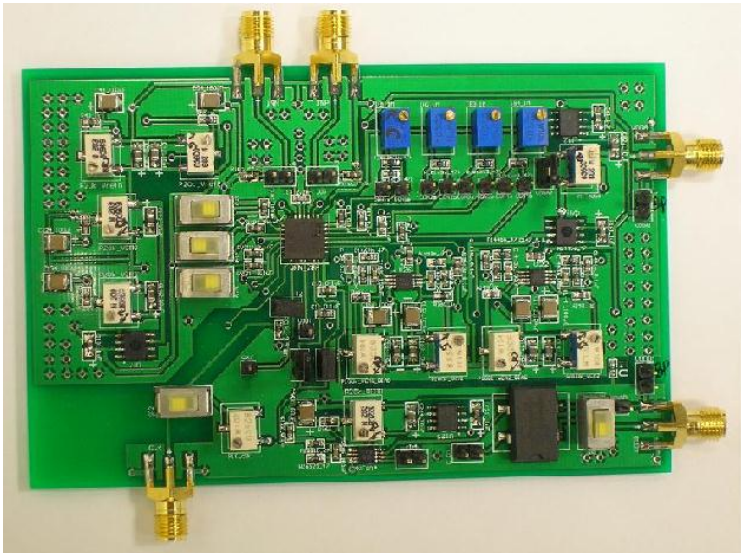


Figure 4.11 Printed circuit board for the prototype chip testing.

4.4.2 Measurement Results and Discussions

The accumulated noise in the audio bandwidth shows that the increase rate of the noise power without the low-pass RC filter is slightly higher than that with the low-pass filter, and it causes around 1-dB reduction of SNR. Although the passive low-pass RC filter can attenuate white noise, it also adds distortions. For SNDR measurement, the filter is deactivated. Figure 4.12 shows the measured 65536-point output spectrum for a 2.33-kHz sinusoidal input without the RC filter.

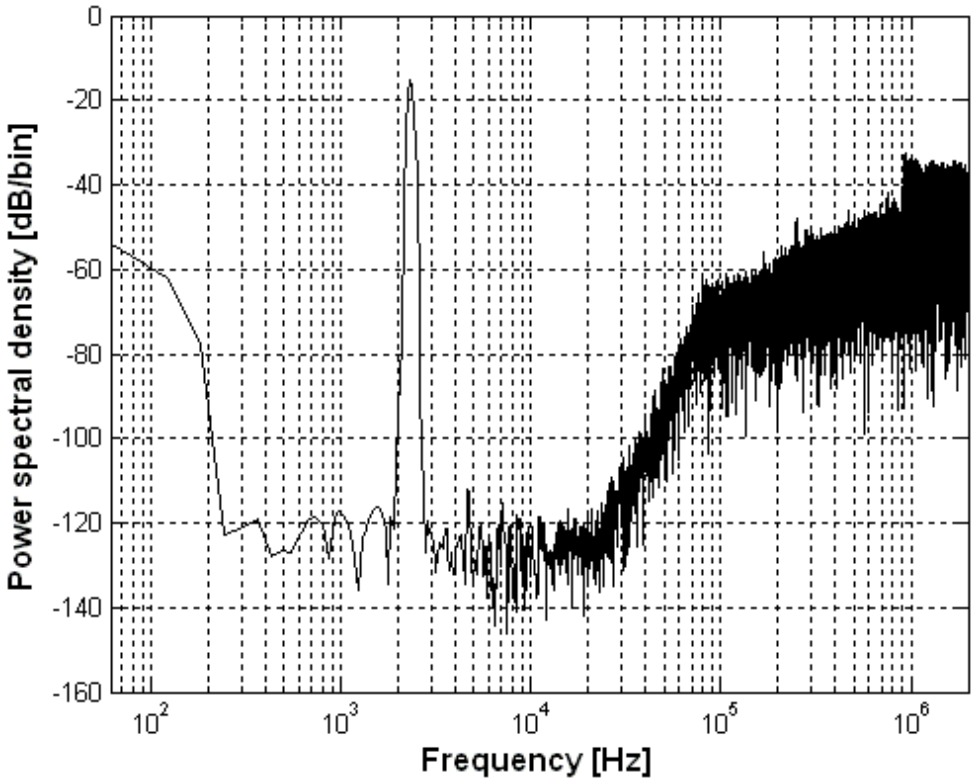


Figure 4.12 Measured output spectrum with a 2.33-kHz sinusoidal input.

The measured SNR and SNDR versus input amplitude is presented in Figure 4.13. Clocked at 4 MHz, the modulator achieves a 87 dB peak SNDR from a 0.7-V supply. Compared those modulators which does not use bootstrap technique in the sampling network [19, 68], the distortion performance is exhibited better at slight penalty of

power. This could be a possible important factor to affect the linearity of modulators. Table 4.1 summarizes the measured performance.

Table 4.1 Performance summary.

Parameter	Measured Value
Supply Voltage	0.7 V
Total Power Consumption	99.7 μW
Analog Power Consumption	68.2 μW
Digital Power Consumption	31.5 μW
Sampling Frequency	4 MHz
Signal Bandwidth	20 kHz
Over Sampling Ratio	100
Input Range	1.4 Vpp-diff
Peak SNR	91 dB
Peak SNDR	87 dB
Dynamic Range	92 dB
FOM	174.8
Core Area	1.27 mm x 0.55 mm
Technology	0.13 μm CMOS

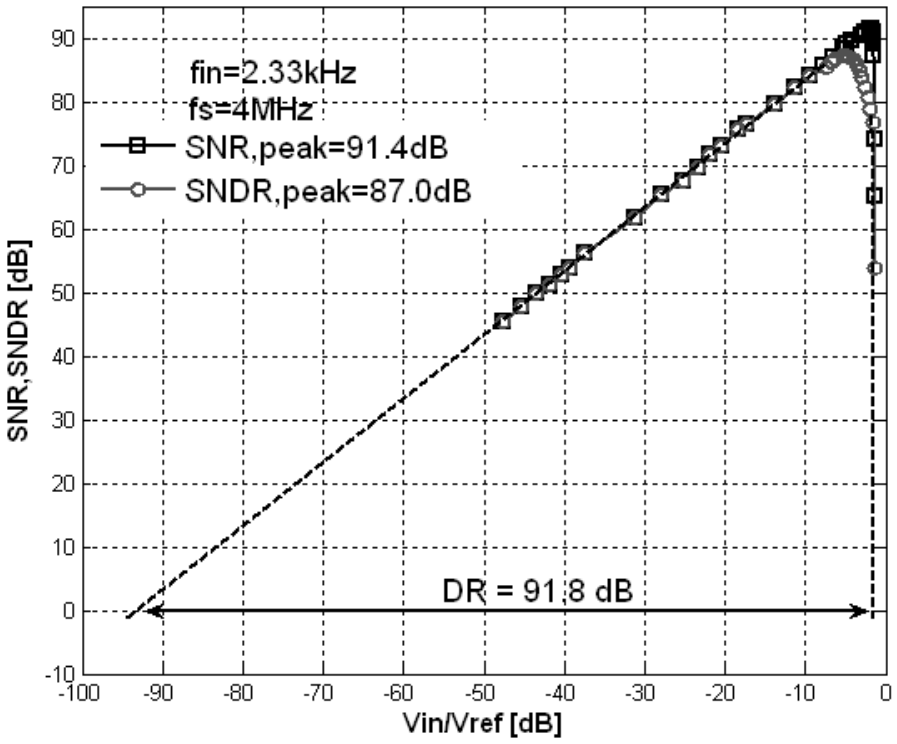


Figure 4.13 Measured SNR and SNDR versus input amplitude.

When the supply voltage varies from 1 V to 0.5 V, the modulator still remains functional. However, the performance is degraded to 81 dB SNDR and 83 dB DR for a 10-kHz signal bandwidth with a power consumption of 56.5 μW from a 0.5-V supply. The performance variation versus the supply voltage is depicted in Figure 4.14.

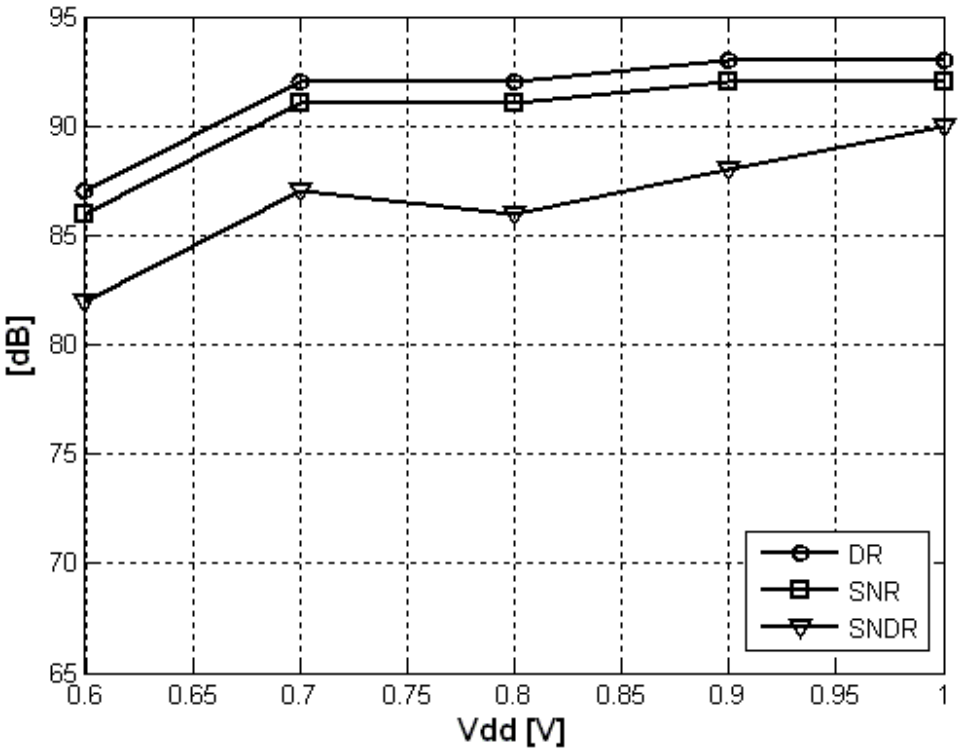


Figure 4.14 Performance versus supply voltage.

4.4.3 Performance Comparison

Table 4.2 compares the proposed ΔΣ modulator with other published sub-1V ΔΣ modulators. The modulator achieves a FOM of, where FOM is defined as $FOM = DR + 10log_{10}(BW/Power)$.

Table 4.2 Performance comparison with state-of-the-art low-power low-voltage ΔΣ audio modulators.

	V_{DD} [V]	BW [kHz]	SNDR [dB]	SNR [dB]	DR [dB]	Power [µW]	Area [mm^2]	CMOS [µm]	FOM
Yao 04 [21]	1.0	20	81	85	88	140	0.176	0.09	169.5
Kim 08 [76]	0.9	24	89	91	92	1500	1.44	0.13	153.2
Roh 08 [19]	0.9	20	73	82	83	60	0.42	0.13	168.2
Chae 08 [20]	0.7	20	81	84	85	36	0.715	0.18	172.4
Park 08 [23]	0.7	25	95	100	100	870	2.16	0.18	170.7
Roh 09 [77]	0.6	20	81	82	83	34	0.33	0.13	170.7
This work	0.7	20	87	91	92	99.7	0.698	0.13	174.8

4.5 Conclusion

This section presents a fourth-order single-bit ΔΣ modulator. It combines input feedforward architecture with a 2-tap FIR filter to reduce both internal signal output swings and integration step of the first stage. Thanks to the unique feature of the optimized low-power architecture, low-voltage power-efficient gain-enhanced current mirror OTAs are adopted in the work. The feedforward paths are implemented by directly feeding to the multi-input comparator, thus the extra power induced by the conventional switch-capacitor summation circuits is saved and compact circuitry is obtained. The measurement results show that the proposed modulator has achieved very good performance in terms of FOM among all published sub-1V audio ΔΣ modulators.

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CHAPTER 5

A 0.5-V 35-μW 85-dB DR DOUBLE-SAMPLED ΔΣ MODULATOR FOR AUDIO APPLICATIONS

This chapter presents a 0.5-V 1.5-bit double-sampled ΔΣ modulator for audio codec. Unlike other existing double-sampled design, the proposed double-sampled ΔΣ modulator employs input-feedforward topology, which reduces internal signal swings, hence relaxes design requirements for low-voltage amplifier and reduces distortion. Moreover, the proposed architecture with its compensation loop preserves noise-shaping character of its single-sampled version and avoids performance degradation. It also employs a new fully-differential amplifier with a global common-mode feedback loop to minimize power as well as a resistor-string-reference switch matrix based on direct summation quantizer to simplify compensation circuit.

5.1 Introduction

As demand for low-power circuit becomes more aggressive, two trends appear gradually. First, reduced supply voltage due to scaled CMOS technology helps reduction of power, particularly, for digital module. Second, key analog building blocks, especially amplifiers or its substitute become more power efficient. Single-stage topologies such as improved current mirror using current shunt [78] or local positive feedback structure [19] have exhibited good power efficiency. However, in switched-capacitor (SC) circuit, due to different output load in two phases, i.e.,

sampling phase and integration phase, these amplifiers easily suffer from ringing settling and thus induce distortion. Previous work used switchable compensated-capacitor opamp [79], partially [8] or fully double-sampling scheme [55] to solve this problem. Of them, double-sampling technique for SC circuit is the best solution. This is because of two reasons. First, symmetric output load of both phases benefit amplifier to keep same phase margin during operation, and hence reduce distortion [22]. Second, double-sampling technique is believed to be superior due to the doubled effective oversampling rate (OSR) without extra power consumption of amplifiers. Instead of using amplifier, inverter-based SC circuits [13] demonstrate unique character such as high power efficiency and compatibility with low supply voltage. Unfortunately, this circuit is incompatible with double-sampling technique due to the need of one phase to store the offset voltage. And it also suffers from increased input referred thermal noise due to input-injected common-mode feedback structure.

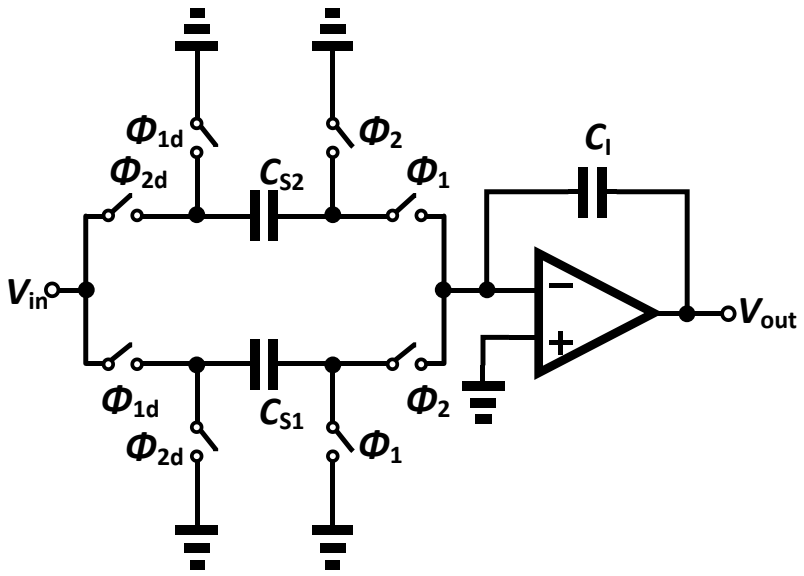
Although double-sampling technique alleviates circuits implementation, conventional double-sampled architecture that based on feedback topology suffers from large internal output swings [22, 55] which inevitably reduce reference voltage to below supply voltage, and thus it may not suitable for really low-voltage low-power applications. Moreover, these existing double-sampled architectures exhibit degradation of noise shaping character compared to its original single-sampled version [55]. This is because an additional pole induced by the fully-floating SC configuration. This work combines double-sampling technique with input-feedforward architecture to reduce internal signal swings, and thus we can make use of full supply voltage to maximize dynamic range of reference voltage. Moreover, compared to single-sampled version, transfer function of the proposed architecture is

restored by adding an extra compensation loop. Therefore, the noise-shaping performance does not degrade.

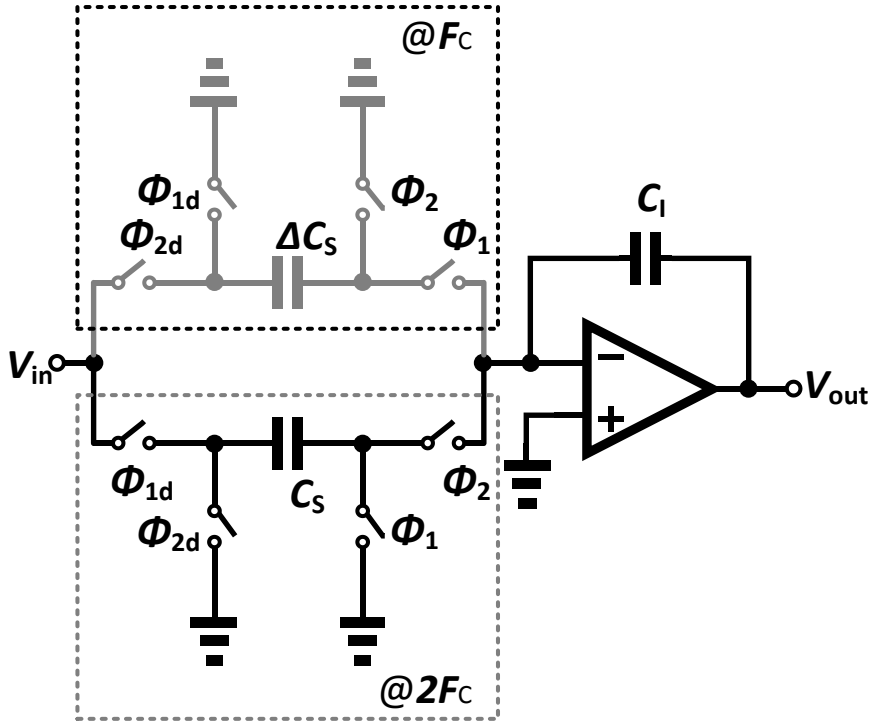
In Section 5.2, we review existing double-sampled architecture in detail. In section 5.3 we introduce the proposed double-sampled architecture. In Section 5.4, we examine existing improved current mirror amplifier for low-voltage low-power ΔΣ modulators. This is followed by the proposed power-efficient amplifier in section 5.5. We report the measurement results in section 5.6 and conclude in section 5.7, respectively.

5.2 Existing Double-Sampled Architecture

In a SC integrator circuit, the amplifier remains idling during the sampling phase. If two sampling capacitors are used operating with interleaved clock signals, full utilization of amplifier in both phases could be achieved. This double-sampled SC



(a)



(b)

Figure 5.1 (a) Double-sampled switched-capacitor integrator. (b) Simplified model of double-sampled switched-capacitor integrator.

integrator that achieves an effective sampling rate of $F_S = 2F_C$(F_C= clock frequency) is shown in Figure 5.1a. Utilizing double-sampling technique has two advantages:

- By maintaining the same clock frequency the effective sampling rate has been doubled; thus, the quantization noise in the band of interest is substantially reduced. Or, by halving the clock frequency the settling time of amplifiers has been relaxed so that minimizing power consumption.
- Since amplifiers are active in both phases, the effective load for amplifiers is completely same so that relaxing the design of amplifiers. Compared to single-sampling scheme, no special technique [79] is needed to compensate the variation of phase margin.

In practice however, due to mismatches within the pair of sampling capacitors, the simplified model of this double-sampling SC integrator is shown in Figure 5.1b, where ΔC_S is the mismatch between C_{S1} and C_{S2}. The main problem associated with this mismatch is that the input signal is also sampled at frequency of F_C due to the presence of the equivalent switched-capacitor ΔC_S. Figure 5.2 illustrates the aliasing effects due to this compound sampling process. This aliasing does not significantly degrade the performance for the input signal V_{in} because the input signal is band-limited (for example, by a continuous or a sampled-data filter running at higher sampling rates). However, it does seriously for the feedback signal due to the noise-shaping character. A fully-floating switched capacitor configuration [55] is proposed to solve the mismatch problem. As shown in Figure. 5.3, the input charge is transferred to the integration capacitor in both phases of clock. The transfer function of the fully-floating SC integrator is given by

$$\frac{V_{OUT}(z)}{V_{IN}(z)} = \left(\frac{C_s}{C_F}\right)\frac{1+z^{-1}}{1-z^{-1}}. \tag{27}$$

It is clear that the transfer function differs from that of a conventional SC integrator due to the factor $1 + z^{-1}$. This factor can be seen as a 2-tap FIR filter which minimizes high frequency noise and makes the charge transfer error randomized in time domain, hence alleviates noise folding as well as distortion.

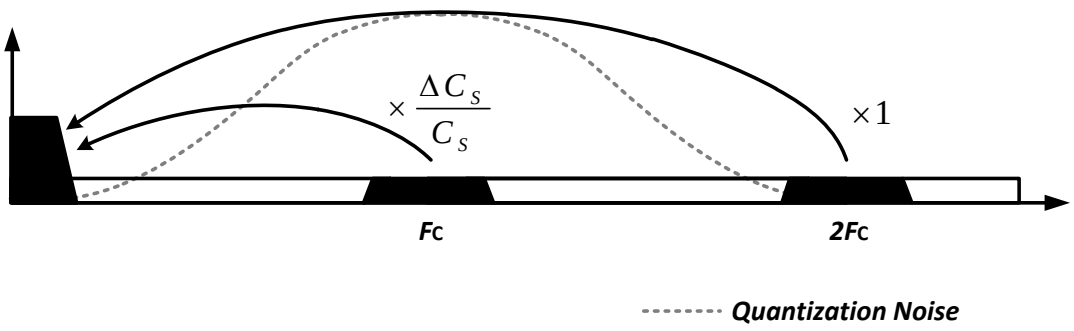


Figure 5.2 Aliasing effect due to sampling process in a double-sampled ΔΣ modulaotr.

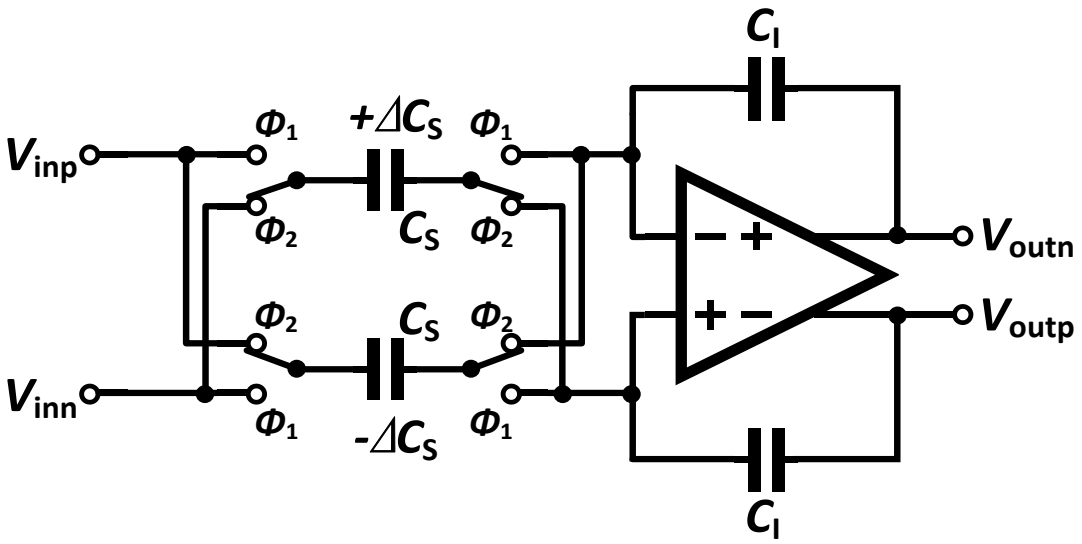
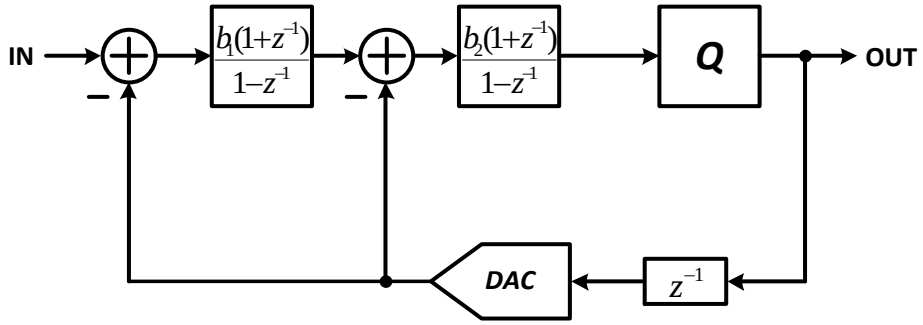
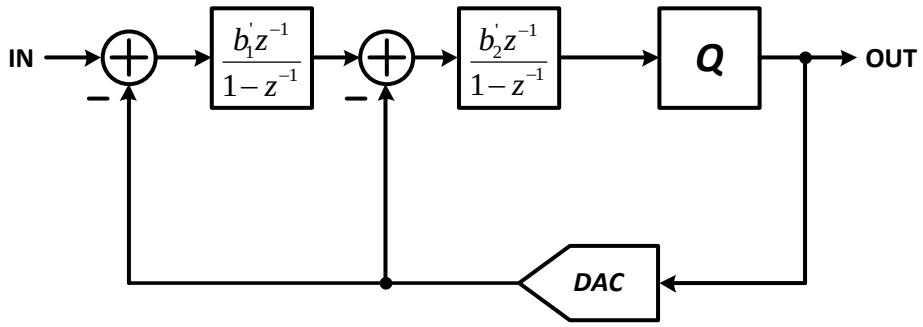


Figure 5.3 Fully-floating switched-capacitor integrator.



(a)



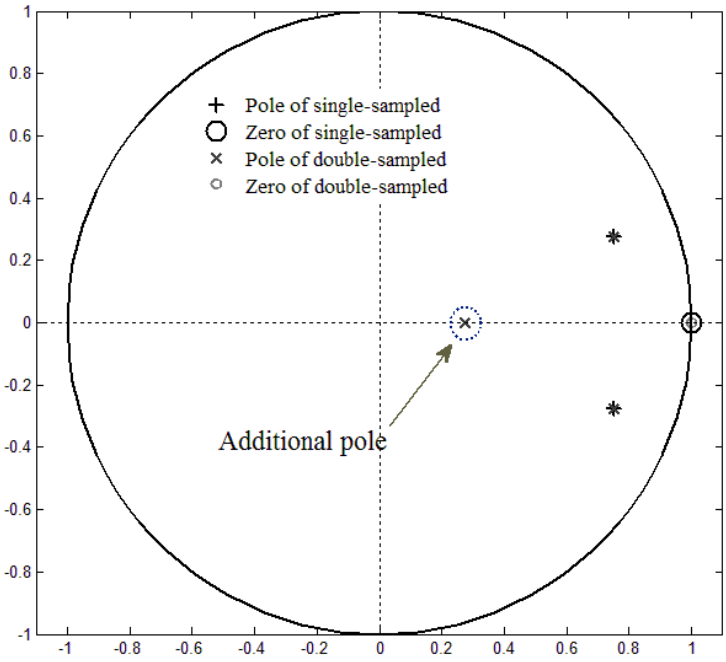
(b)

Figure 5.4 (a) Second-order double-sampled architecture based on feedback topology. (b) Second-order single-sampled architecture based on feedback topology.

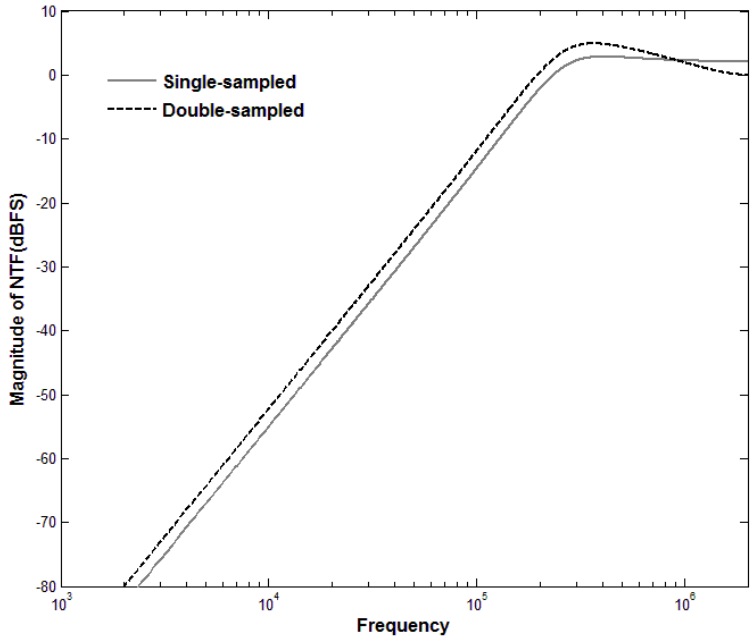
One existing double-sampled architecture which based on feedback topology [55] is shown in Figure 5.4a. Disadvantage of feedback topology is the large internal signal swings and the stringent requirements for analog building blocks. In addition, multi-feedback-loop with fully-floating SC configuration complicates the overall architecture and degrades the noise-shaping performance compared to original single-sampled version. Figure 5.4b shows a comparative single-sampled architecture. Since transfer function of the fully-floating SC integrator changes to $\frac{1+z^{-1}}{1-z^{-1}}$ from $\frac{z^{-1}}{1-z^{-1}}$, one clock delay z^{-1} is inevitably added to the feedback path to match the clocked quantizer [33]. Therefore, noise transfer function (NTF) of the double-sampled architecture changes to

$$NTF(z) = \frac{(1-z^{-1})^2}{1+(b_1b_2+b_2-2)z^{-1}+(2b_1b_2+1)z^{-2}+(b_1b_2-b_2)z^{-3}}. \quad (28)$$

Compared to NTF of Figure 5.4b which only contains a second-order delay z^{-2}, this NTF adds an extra pole, as illustrated in Figure 5.5a. Behavioral simulation shows that this additional pole moves NTF towards left side along frequency axis, as illustrated in Figure 5.5b. And thus it degrades the noise shaping. Measured result of [55] also confirmed this degradation.



(a)



(b)

Figure 5.5 (a) Pole-zero chart of single-sampled and double-sampled architecture. (b) NTF comparison between single-sampled and double-sampled architecture.

5.3 Proposed Architecture

5.3.1 Proposed double-Sampled ΔΣ Architecture

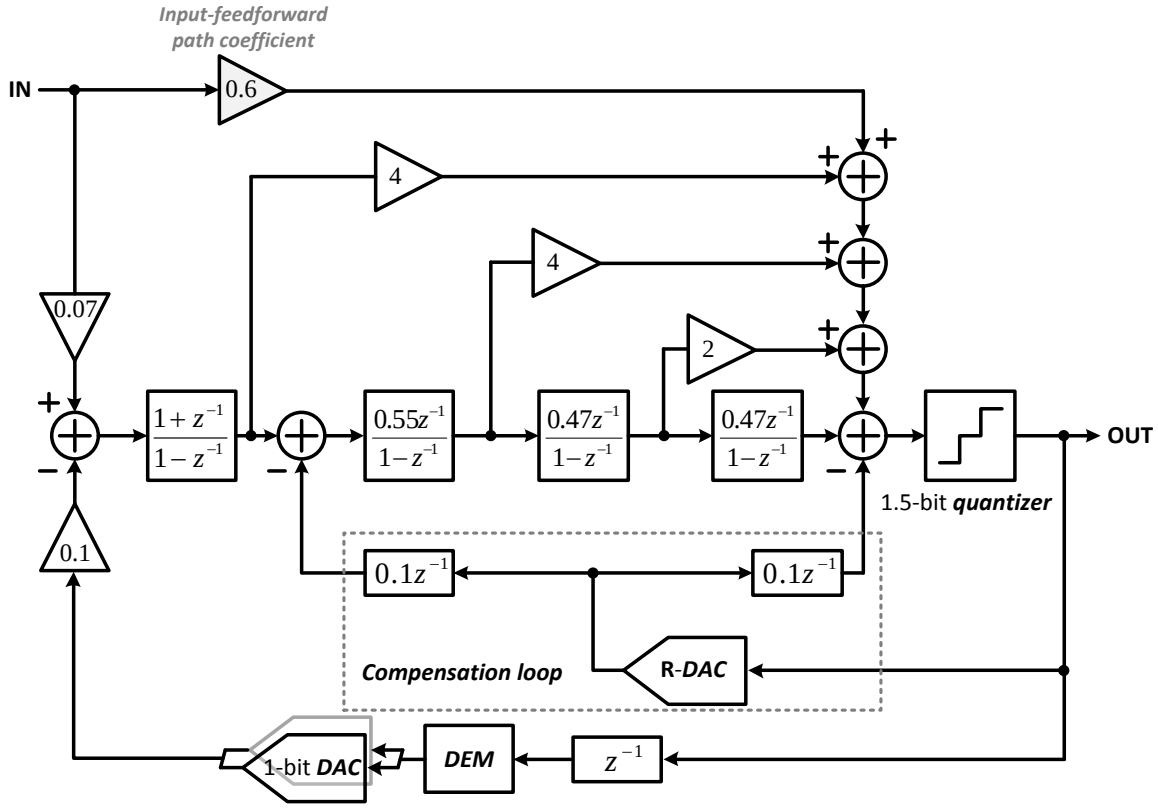


Figure 5.6 Proposed fourth-order double-sampled ΔΣ modulator based on input-feedforward topology.

In this work, a fourth-order 1.5-bit ΔΣ modulator based on input-feedforward topology is proposed as illustrated in Figure 5.6. Unlike other existing double-sampled architecture [22, 55] which employs fully-floating SC configuration for distributed feedback loop, this architecture only uses one fully-floating SC configuration to the first feedback path, which reduces sensitivity to mismatch of the feedback signal. Two extra feedback paths are added as a compensation loop to restore noise transfer function to that of original single-sampled version as well as

stability of the system. The longest delay of the main loop filter is z^{-5} which means an extra pole is added in the fourth-order system. However, the left branch of the compensation loop cancels this extra pole thus resulting in a four-pole system. This compensation can be explained at the first stage in z-domain expression.

$$\begin{aligned} H_{ds}(z)H_f(z) + H_{com}(z) &= \frac{1+z^{-1}}{1-z^{-1}}(-0.1z^{-1}) - 0.1z^{-1} \\ &= -0.2\frac{z^{-1}}{1-z^{-1}} \\ &= H_{ss}(z), \end{aligned} \tag{29}$$

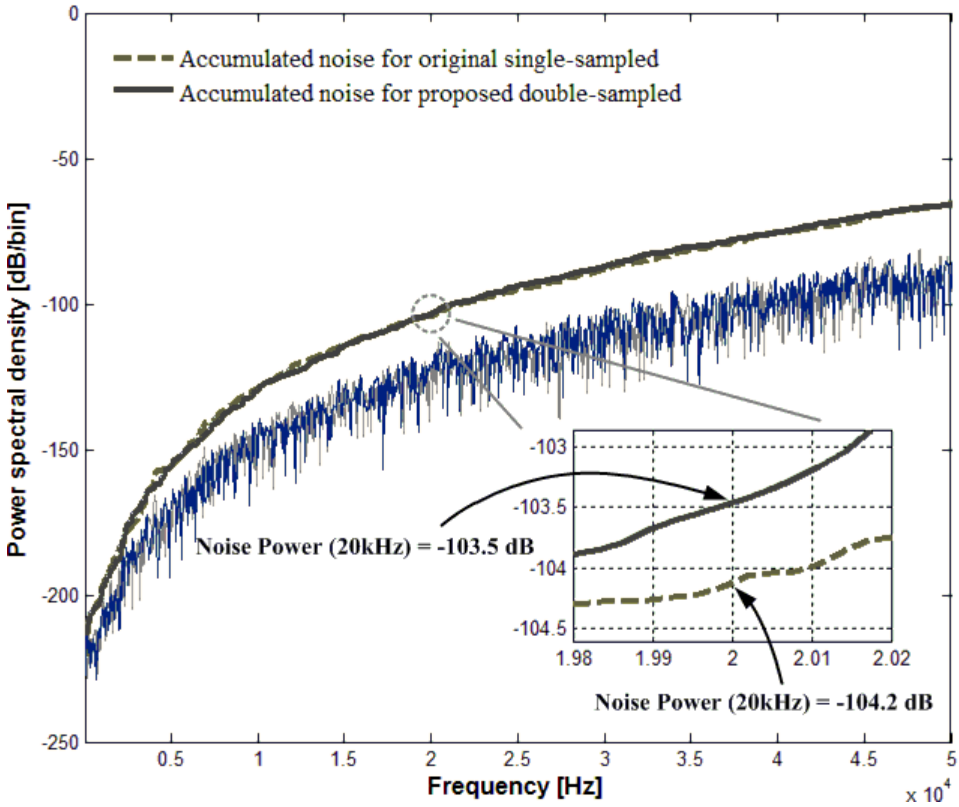
where $H_{ds}(z) = \frac{1+z^{-1}}{1-z^{-1}}$, $H_f(z) = -0.1z^{-1}$ and $H_{com}(z) = -0.1z^{-1}$ are the transfer function of the double-sampled integrator, the delayed feedback loop and the left branch of the compensation loop, respectively. As apparent from equation (29), the double-sampled architecture restores the same transfer function as that of single-sampled version. Figure 5.7 shows behavioral simulation result of the proposed double-sampled architecture and its original single-sampled version. Figure 5.7a exhibits only a degradation of 0.7 dB compared to that of 5.3 dB in a conventional double-sampled architecture, which shown in Figure 5.7b. This slightly degradation is due to the mismatch induced by nonidealities in the first integrator between the main feedback loop and the compensation loop.

For a high-order single-bit topology, the stable range that the modulator usually can handle is 0.7 of reference voltage, which means 3 dB loss from maximum available signal power. Figure 5.8a shows a sampling network with two separate sampling capacitors. One which is for entering the input signal refers to the input capacitor C_S while the other for DAC signal refers to the feedback capacitor C_F. The output of the integrator is as follows

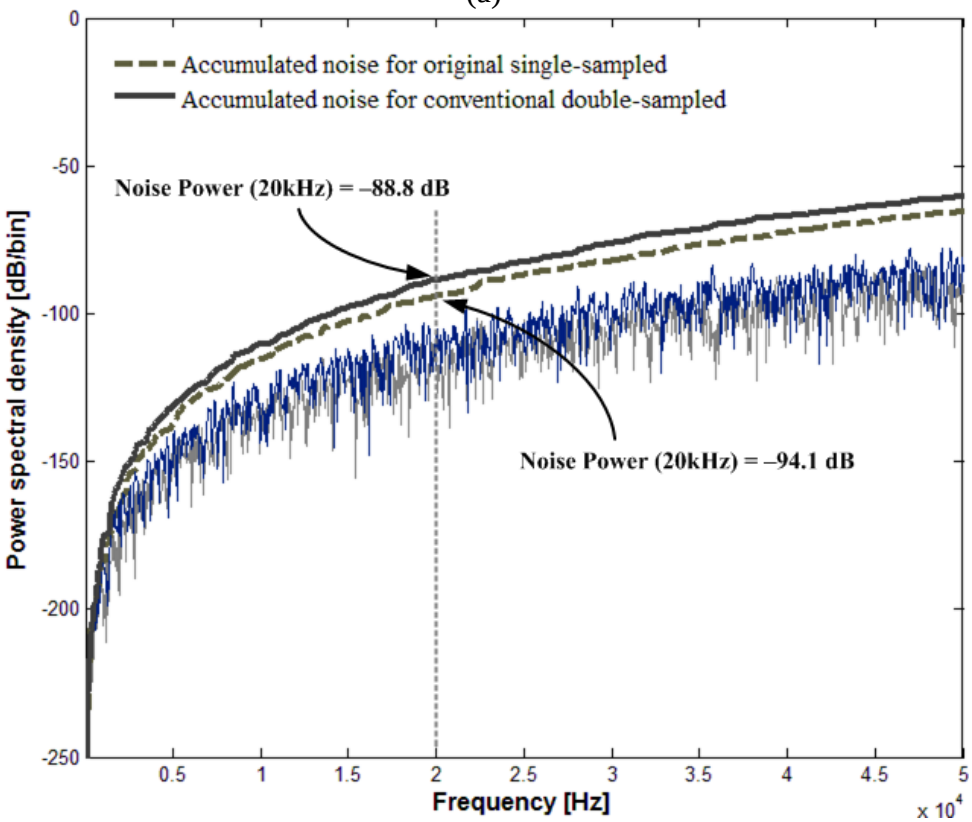
$$V_{out} = V_{in} \times \frac{C_S}{C_I} + V_{ref} \times \frac{C_F}{C_I}. \quad (30)$$

To compensate the 3 dB loss, we scale input sampling capacitor to $0.7C_s$, thus the input signal could be extended to full reference range. This benefits peak signal power by 3 dB. However, the added feedback capacitor C_F increases input-referred noise by 5.4 dB. Moreover, the feedback capacitor C_F inevitably increases the equivalent load capacitance of the integrator and hence the power consumption of the modulator. If taking power increase into consideration, the peak SNR is reduced by 4.7 dB totally.

To reduce total sampling capacitance of sampling network, Figure 5.8b reduces both the input sampling capacitor C_s and the feedback capacitor C_F to half by alternatively sampling positive and negative signal. Since the output-referred signal power remains same in Figure 5.8, if the change of input signal in a phase period is ignored (this is indeed true for most single-bit ΔΣ modulator due to the high OSR), it is instructive to compare the output-referred noise. The output-referred noise is proportional to the sum of sampling capacitance , from this point of view, this sampling network which shown in Figure 5.8b may yield higher peak SNR. Detailed calculation based on input-referred noise verifies the conclusion. It is interesting to note that by sampling input signal in two consecutive phases the equivalent input-referred signal power is quadrupled. This is because the basic sampling network only samples input signal in one phase and transfers the signal in another phase. However, the sampling network with separate capacitors allows the input capacitor to enter input signal in both phases. Since the sampled input signal in two consecutive phases is correlated, the equivalent input-referred signal voltage is doubled, thus the power is quadrupled, which means another 6 dB improvement for the peak signal power.



(a)



(b)

Figure 5.7 (a) Noise-shaping comparison between proposed double-sampled and original single-sampled architecture. (b) Noise-shaping comparison between conventional double-sampled and original single-sampled architecture.

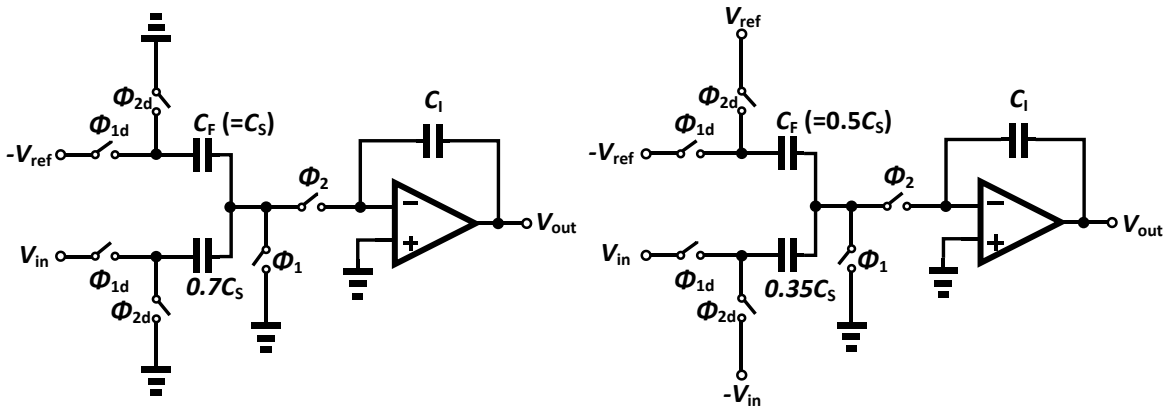


Figure 5.8 (a) Sampling network with scaled input sampling capacitors and feedback reference sampling capacitor. (b) Proposed sampling network with scaled input sampling capacitors and feedback reference sampling capacitor.

5.3.2 Integrator Output Swings

Reduced integration step benefits modulator to minimize power. As illustrated in Figure 5.9, small integration step ($< 0.15V_{ref}$) occupies 93.8% for the proposed double-sampled architecture while it only occupies 59.3% for the single-sampled version. The double-sampled architecture differs from the original single-sampled version only in the floating SC configuration and the added compensation feedback loop. This reduction is because the filter process induced by the fully-floating SC

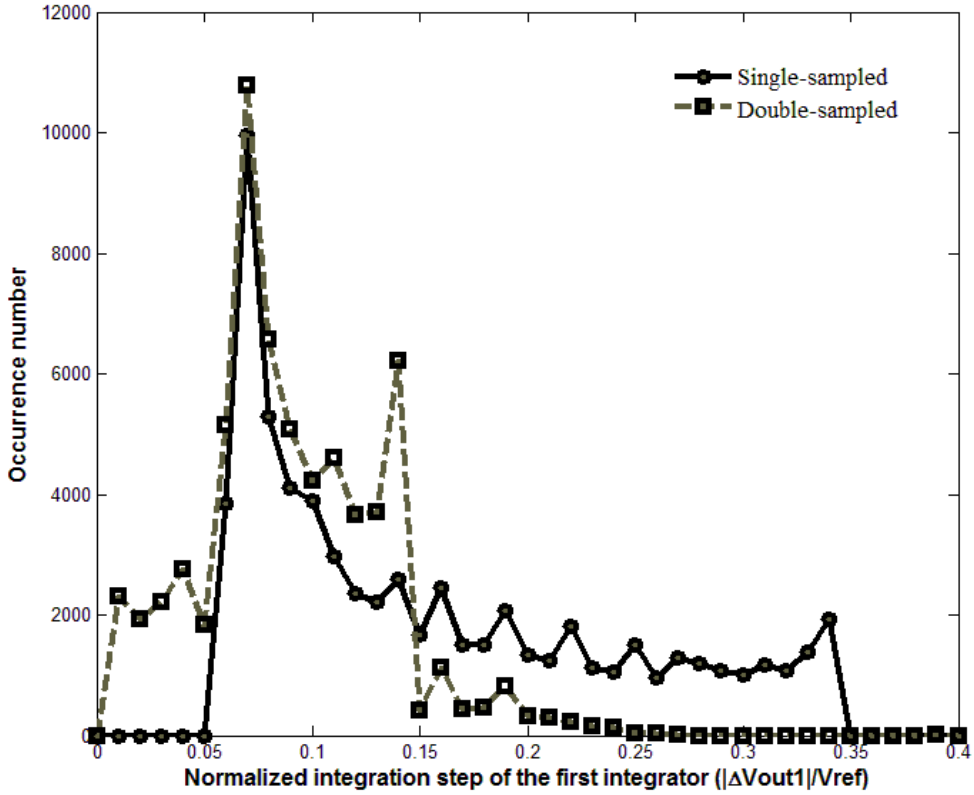


Figure 5.9 Reduced integration step of the first integrator of double-sampled architecture.

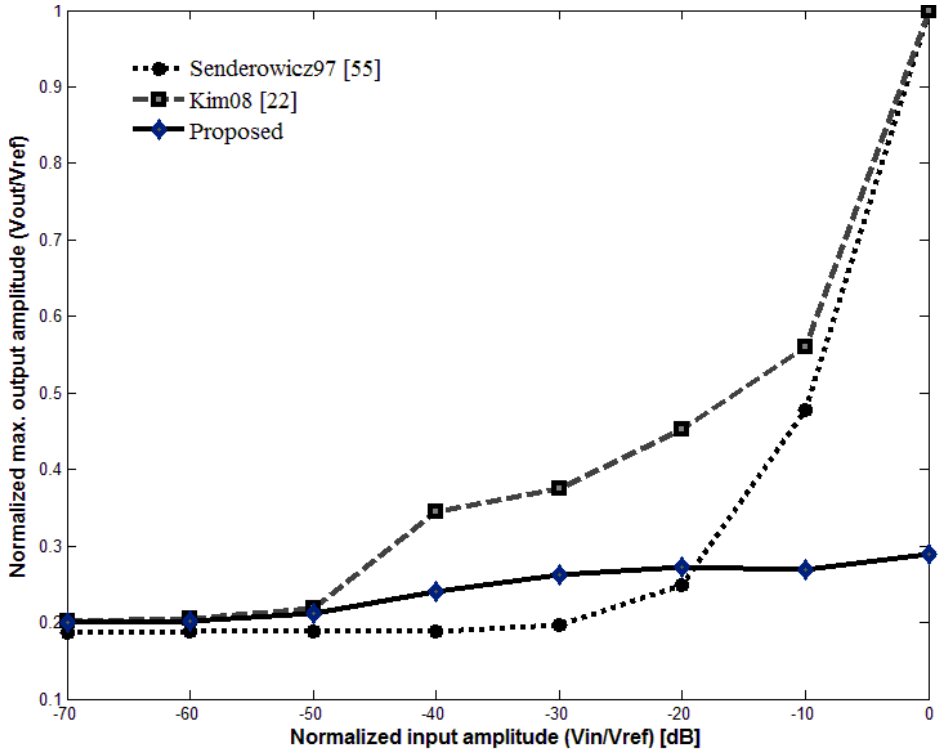
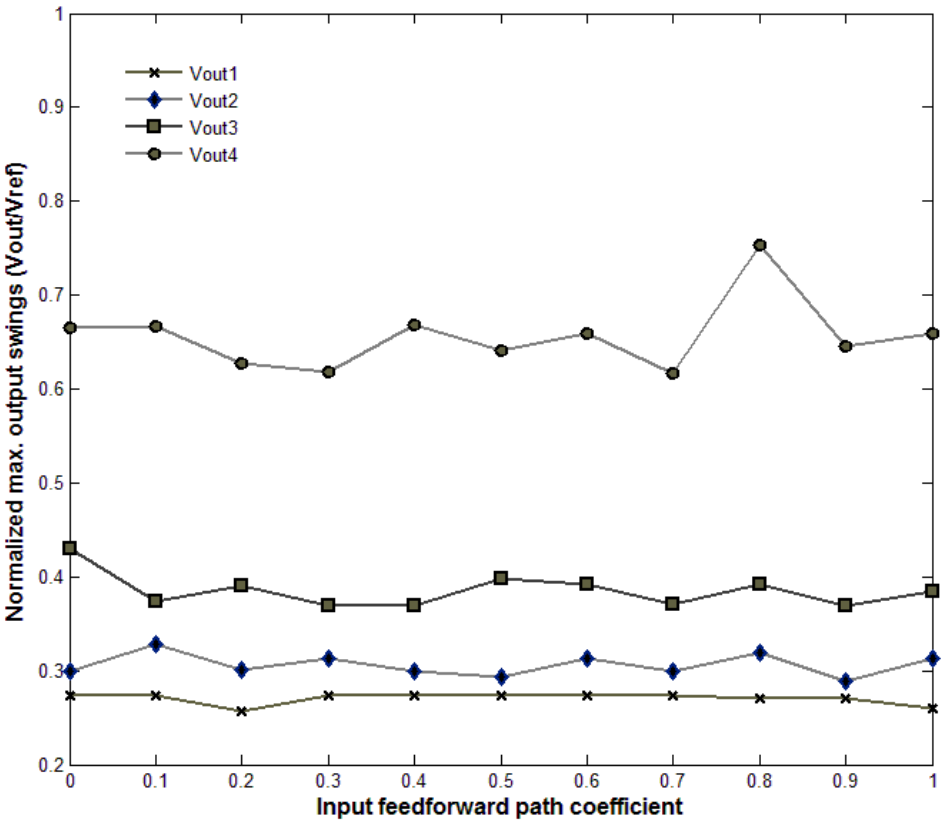


Figure 5.10 Output voltage swing of the first integrator versus increased input signal amplitude.

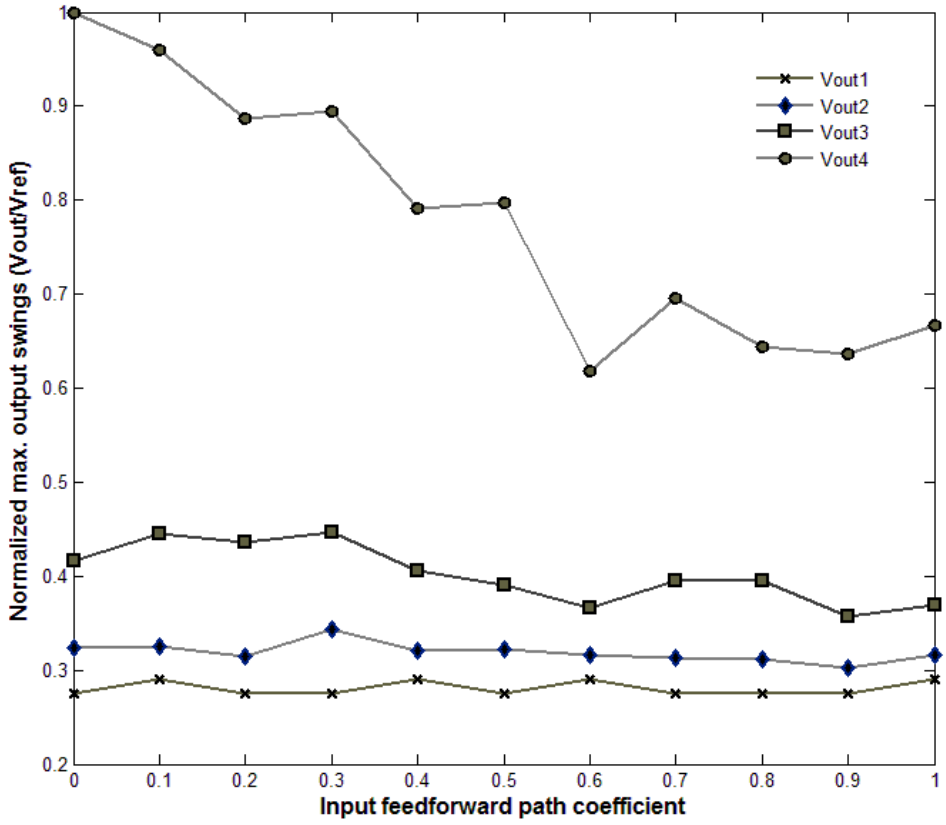
configuration. It provides a zero at $F_S/2$ which effectively reduces high frequency quantization power flow into the ΔΣ loop filter.

Figure 5.10 compares the output voltage swing of the first integrator versus increased input signal amplitude with other existing double-sampled architecture. The proposed double-sampled architecture based on input-feedforward topology demonstrates reduced and relatively input-independent swing at the first integrator output. From this figure we can clearly see that thanks to scaled input sampling capacitor the proposed architecture even can work with 0 dBFS input (normalized to reference voltage). The reduced swing at the first integrator output substantially relaxes the requirement of DC gain which is stringent in other existing double-sampled architecture to suppress DC gain nonlinearity, hence further benefit the architecture to reduce power.

Besides output swing at the first stage, output swing at the last stage which usually appears maximum in input-feedforward topology [62] should be taken into consideration to avoid signal overload. Unlike in [62] which uses additional negative input signal to suppress the output swing, we directly optimize the input feedforward path coefficient to minimize the output swing. This is because two reasons. Firstly, for single bit quantizer, the quantizer gain is less constant than that of multi-bit quantizer, thus making use of linear model does not certainly result in relaxed design requirement for analog building block. Moreover, since the input feedforward path prevents most signal energy from flowing into the ΔΣ loop filter, there may exist an optimized coefficient to minimize output swings of all integrators. Behavioral simulation finds that the input feedforward path coefficient obviously affects output



(a)



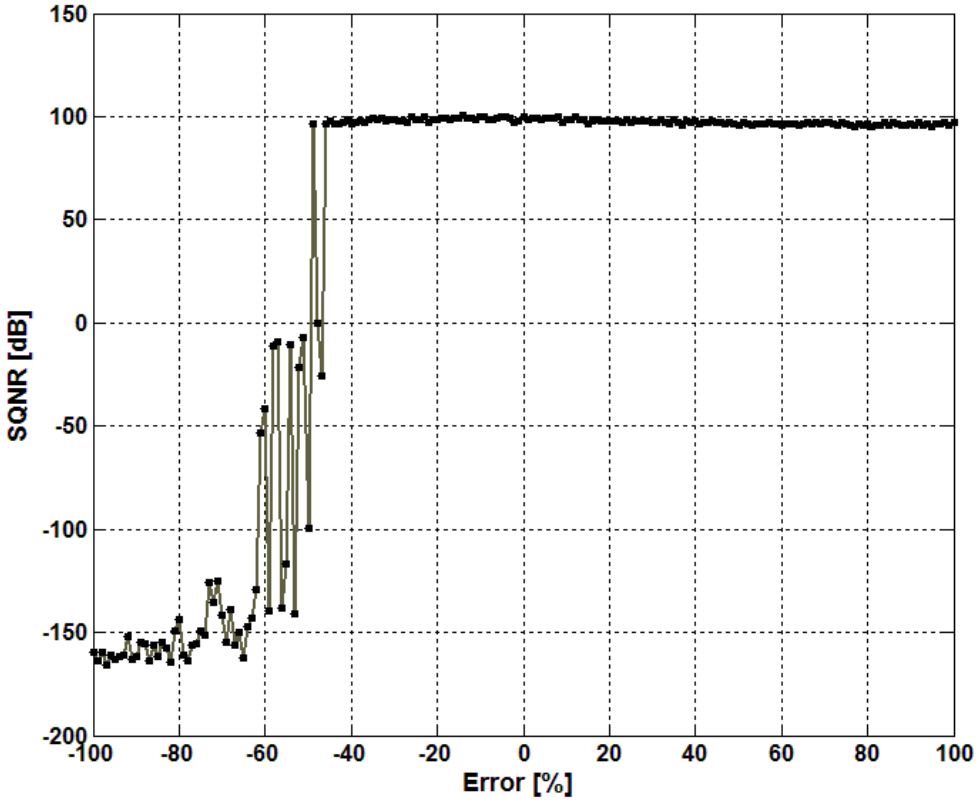
(b)

Figure 5.11 Normalized output voltage swings versus input feedforward path coefficient (a) with -20 dBFS sinusoidal input. (b) with 0 dBFS sinusoidal input.

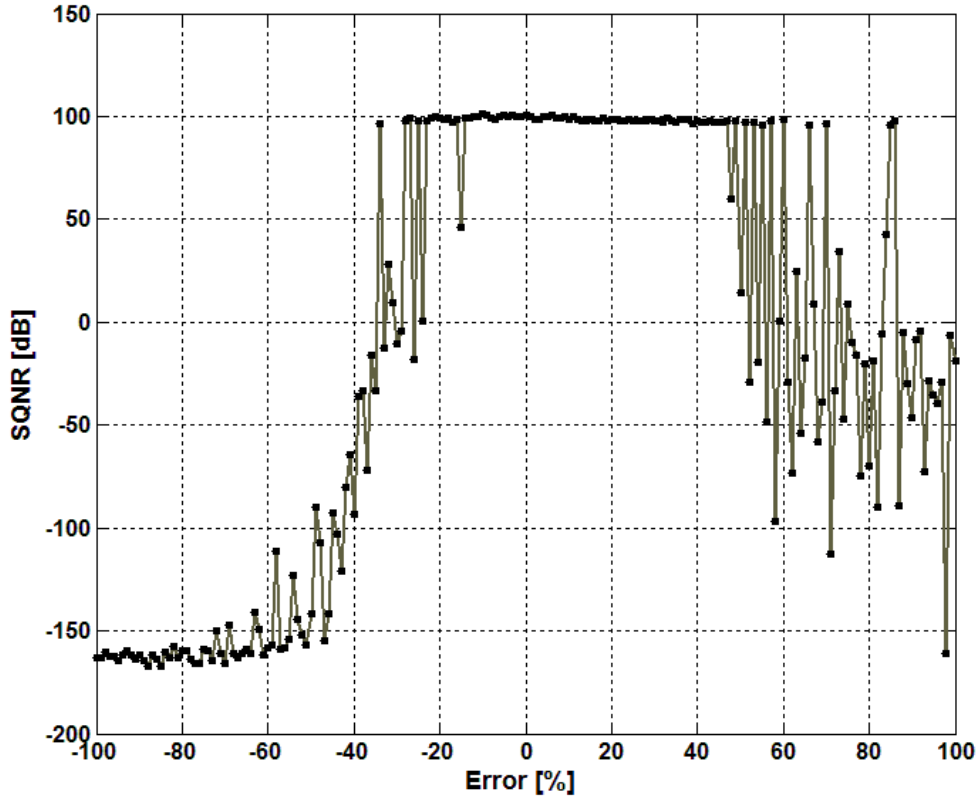
swing at the last stage, but has little of influence on output swing at rest stages. Figure 5.11 demonstrates normalized output voltage swings versus input feedforward path coefficient. We choose 0.6 as the input-feedforward path coefficient.

5.3.3 Mismatch Consideration

There are several mismatch sources may degrade performance of the modulator. The most important one is the mismatch within the pair of input sampling capacitor of the first stage, we employ fully-floating SC configuration [55] to solve the mismatch problem. Moreover, the three-level feedback signal also could produce distortions. We use a simplified data-weighted averaging (DWA) circuit [22, 80, 81] to alleviate this problem. In addition, in order to simplify circuit implementation, we choose resistor-ladder-based reference to realize compensation feedback loop. The compensation coefficients suffer from mismatch due to process variation. This mismatch should be considered carefully since resistor variation is considerably larger than capacitor variation in CMOS process. The resistor ladder only needs to produce one reference voltage which equals to $0.1V_{ref}$. Behavioral simulation shows performance of the modulator versus variation of the reference for the compensation feedback loop with large input signal feeding into the modulator. As illustrated in Figure 5.12a, when input amplitude reaches -1 dBFS and the reference error is within 46%, the system remains stable and the performance is almost kept constant. Figure 5.12b shows that as input amplitude reaches 0 dBFS the error tolerance declines to 16% while the system is stable. Such large tolerance for large input signal may suggest that using resistor ladder to produce reference voltage is applicable.



(a)



(b)

Figure 5.12 Performance versus error (a) with -1 dBFS sinusoidal input. (b) with 0 dBFS sinusoidal input.

5.4 Existing Power-Efficient Low-Voltage Low-Power Amplifier

Current mirror topology is believed to be a power-efficient choice for low-voltage low-power opamp. However, reduced DC gain due to scaling down of process makes it inapplicable for most ΔΣ architecture. Several power-efficient architectures used for a low-voltage low-power opamp have been proposed based on current mirror topology [19, 67]. [67] proposes partially to shunt the diode current while [19] employs local positive feedback loop to improve DC gain.

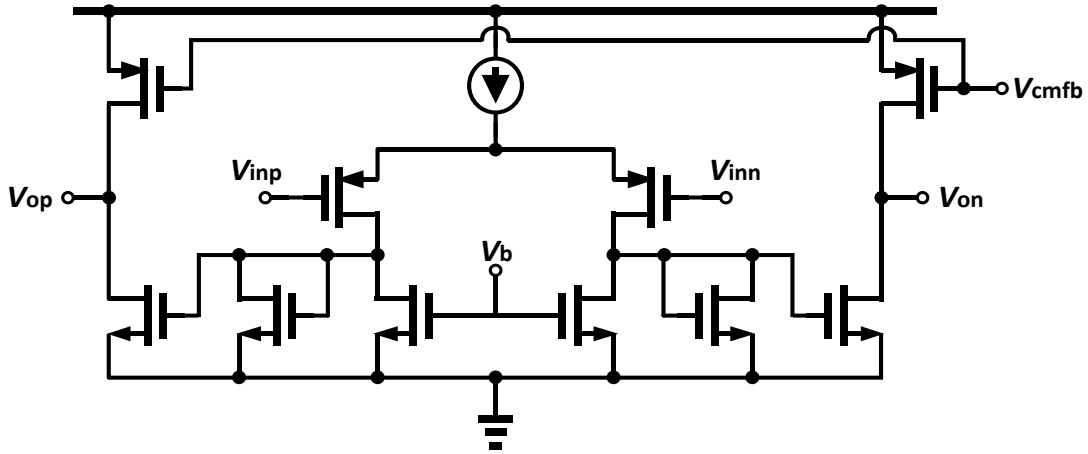
5.4.1 Current-Shunt Current Mirror Topology

As illustrated in Figure 5.13a, using a current source to shunt a portion of diode current, the current at the output stage is reduced by (*1-k*), where *k* is ratio between total shunted current and tail current at the input stage. Since the output current is decreased, the DC gain is improved at the expense of a lower slew rate.

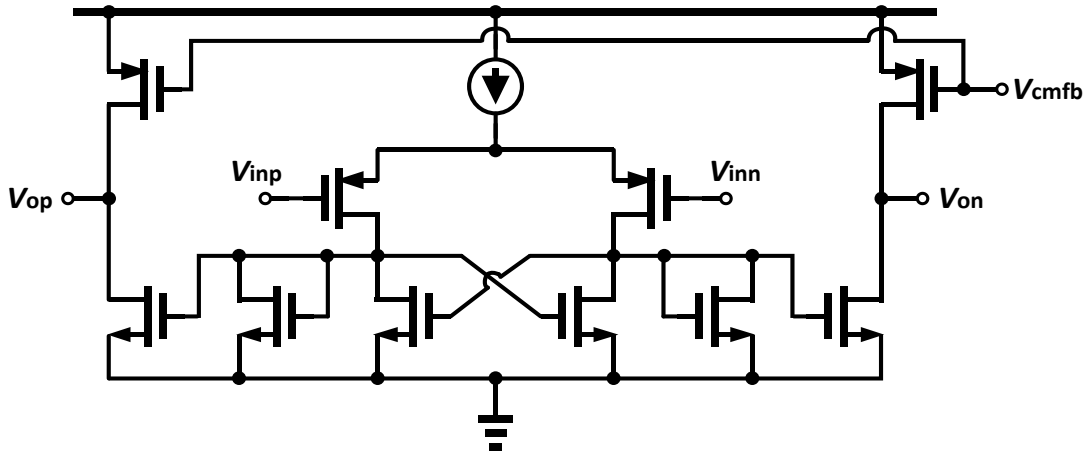
5.4.2 Local Positive Feedback Current Mirror Topology

J. Roh, et al. [19] employs a local positive feedback loop in shunt with the diode in the input stage, as shown in Figure 5.13b. The local positive feedback configuration provides a negative transconductance which partially cancels transconductance of the diode. Meanwhile, it also bypasses a portion of the diode current, thus reduce output

current and slew rate as well. The advantage of this structure is that no additional bias voltage is needed like that in [67]. However, this design is more sensitive to parameter mismatch since positive feedback is easily prone to oscillation.



(a)



(b)

Figure 5.13 (a) Current-shunt current mirror amplifier. (b) Current mirror amplifier employing a local positive feedback loop..

5.5 Circuit Implementation

5.5.1 Proposed Fully-Differential Amplifier with Inverter Output Stages

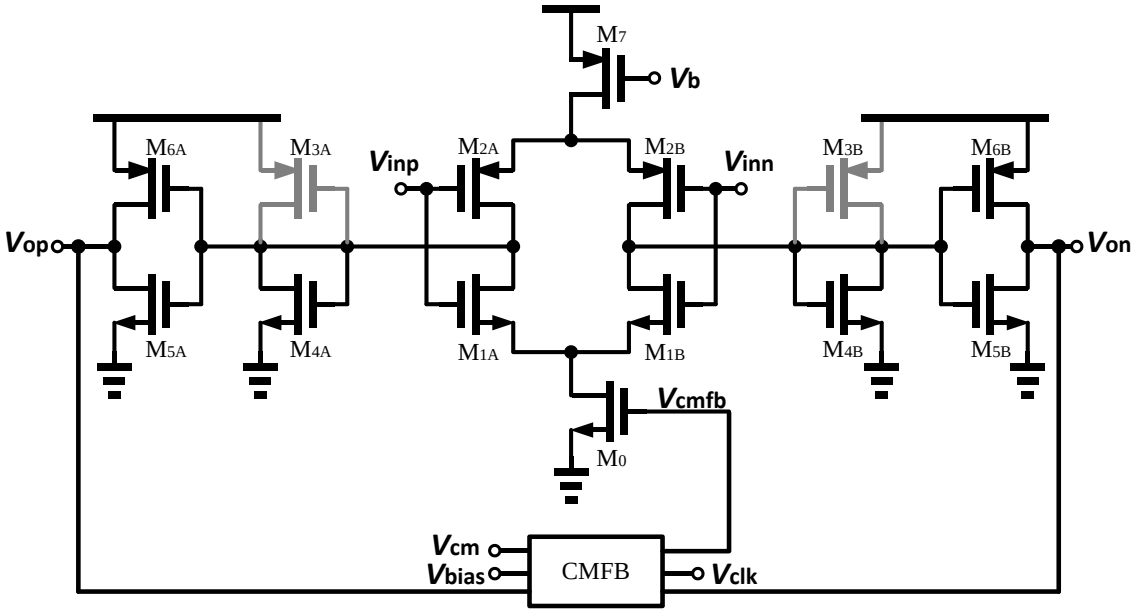


Figure 5.14 Proposed fully-deferential amplifier with inverter output stages.

Previous published fully-differential amplifiers developed from current mirror structure [19, 67] had achieved adequate DC gain, large bandwidth, high slew rate and low quiescent current for ΔΣ modulators. However, these fully-differential amplifiers are much inferior compared to their single-ended version [78, 82] in terms of power efficiency due to the large quiescent current at the output stages. The large quiescent current occurs due to the requirement for common-mode (CM) loop bandwidth. We propose an alternative way to realize the CM loop. Figure 5.14 shows the proposed fully-differential amplifier. For simplicity reasons, the bias circuit is not drawn in the Figure. The V_b in the Figure 5.14 is internally generated on-chip. Detailed comparison based on simulations is covered in section 5.5.3. In addition, in order to improve the transconductance of the input stage, a pair of NMOS and PMOS transistors is used to serve as an input pair. And also the increased size of the input pairs is beneficial to

reduce flicker noise. A pair of complimentary diode is employed to improve the settling. Details on the impact of complimentary diode are covered in section 5.5.4.

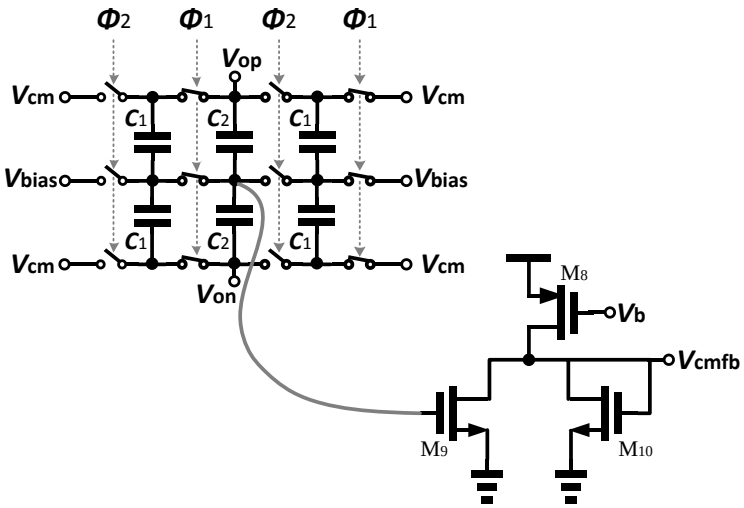


Figure 5.15 Improved SC-CMFB circuits with an inverting stage.

An improved version of SC-CMFB [83] is used in the work, as shown is Figure 5.15. An inverting stage is added in between the SC-CMFB and the fully-differential amplifier to obtain negative feedback. Switches on the left side of axis of symmetry through V_{op} and V_{on} node, operate with opposite clock phase as compared to those on the right side. Thus, during every clock phase, the total loading on the differential loop due to CM loop is $C_T = C_1 + C_2$. In this work, $C_1$is designed 5 times that of C_2 for faster DC settling, lower steady-state errors, charge injection errors and leakage errors. Thus, a better performance of the SC-CMFB can be obtained, for the symmetrical total capacitance loading of the DM loop, at the cost of additional die area.

Since the CMFB is shifted to the input stage, an inverter can be employed as the output stage to improve slewing as well as transconductance. To achieve both high gain and wide GBW, the inverter should be operated at the boundary between the

weak and strong inversion regions, which can be found by using the sum of threshold voltages of both PMOS and NMOS [13]. The threshold voltages of PMOS and NMOS are -0.27 V and 0.22 V, respectively. The supply voltage of this work is chosen to be 0.5 V. The DC-gain of the proposed amplifier is as follows.

$$A_{DM} = \frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}+g_{m3}+g_{m4}+g_{ds3}+g_{ds4}} \times \frac{g_{m5}+g_{m6}}{g_{ds5}+g_{ds6}}, \quad (31)$$

where g_m is the transconductance when input is cross between gate and source, g_{ds} is the transconductance when input is cross between drain and source.

5.5.2 Intrinsic Noise Analysis

Since supply voltage is very low, the input pair and the output stage are biased under weak inversion condition. Assuming both PMOS and NMOS of the input pair, the complimentary diode and the output stage have the same transconductance $g_{mw,in}$, $g_{m,cd}$ and $g_{mw,o}$, respectively. The input-referred thermal noise voltage of the proposed architecture is derived as follows.

$$\overline{V_{n\_t}^2} = \frac{4KT\gamma}{g_{mw,in}} + \frac{4KT\gamma \cdot g_{m,cd}}{g_{mw,in}^2} + \frac{4KT\gamma \cdot g_{m,cd}^2}{g_{mw,o} \cdot g_{mw,in}^2}, \quad (32)$$

where γ is 2/3 for a strong inversion transistor and 1/2 for a weak inversion transistor. For a given bias current, the transconductance g_{mw} of a weak inversion transistor is almost five times larger than g_m of a strong inversion transistor [13]. Thus, the weak inversion biased amplifier has much lower thermal noise compared to classical current mirror amplifier for almost same quiescent current (the current flow though the complimentary diode is quite small, and thus can be ignored). The thermal noise

comparison between classical current mirror OTA and the proposed amplifier is summarized in Table 5.1.

Table 5.1 Thermal noise comparison between classical current mirror and the proposed OTA.

	$\overline{V_{n\_t}^2}\ (V^2/Hz)$
Classical current mirror OTA	$\frac{64KT}{9g_{m,in}} + \frac{32KT}{27g_{m,o}}$ *
Proposed OTA	$\frac{32KT}{75g_{m,in}} + \frac{2KT}{1125g_{m,o}}$ **

*assuming the transconductance $g_{m,d}$ of the diode is 1/3 of $g_{m,in}$.of the input transistor.

**$g_{mw,in} = 5g_{m,in} = 3g_{m,cd}$, $g_{mw,o} = 5g_{m,o}$.

5.5.3 CMFB with Global Loop vs Local Loop

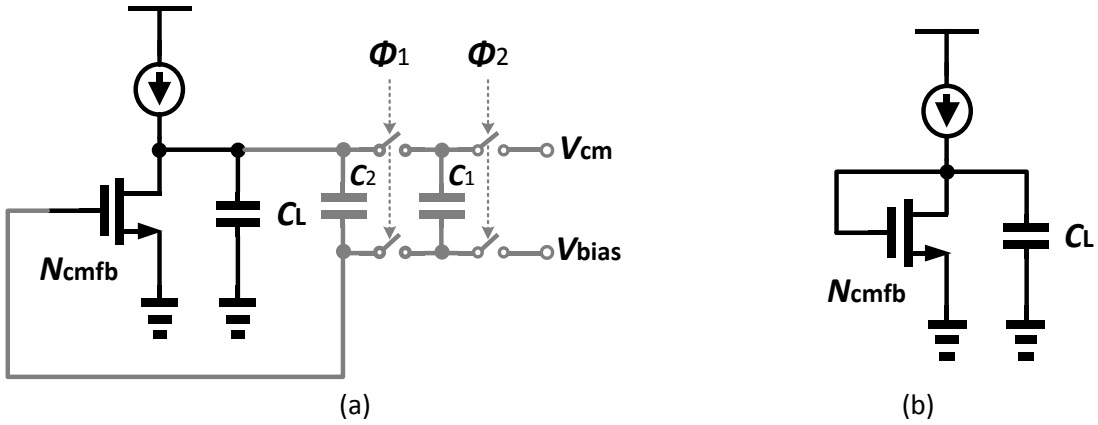


Figure 5.16 (a) CMFB loop of conventional fully-differential amplifier (b) simplified model of (a).

For SC circuit, it is better to design the CM loop bandwidth larger than its differential-mode (DM) loop bandwidth [84]. In practical design, though the CM loop bandwidth needn't larger than DM loop bandwidth, it still needs sufficient large to suppress the spurs of CM signals so that it does not disturb the differential performance [85].

Compared to continuous time circuit, the requirement for CM loop bandwidth is much stringent for SC circuit. Figure 5.16a shows a CM loop for other existing differential amplifiers. Suppose the clock frequency of SC-CMFB is much higher than that of SC circuit, the CM loop can be simplified to Figure 5.16b. It should be noted that the CM loop bandwidth is proportional to the transconductance of only one transistor, i.e.,

$$GBW_{cm} = \frac{g_{cmfb,o}}{C_L}. \tag{33}$$

Therefore, this CMFB transistor needs adequate large current to produce enough transconductance to meet the requirement for CM loop bandwidth. Moreover, the increased current of output stage also reduces the output resistance which in turn needs more current to increase the transconductance of the input stage to meet DC gain requirement.

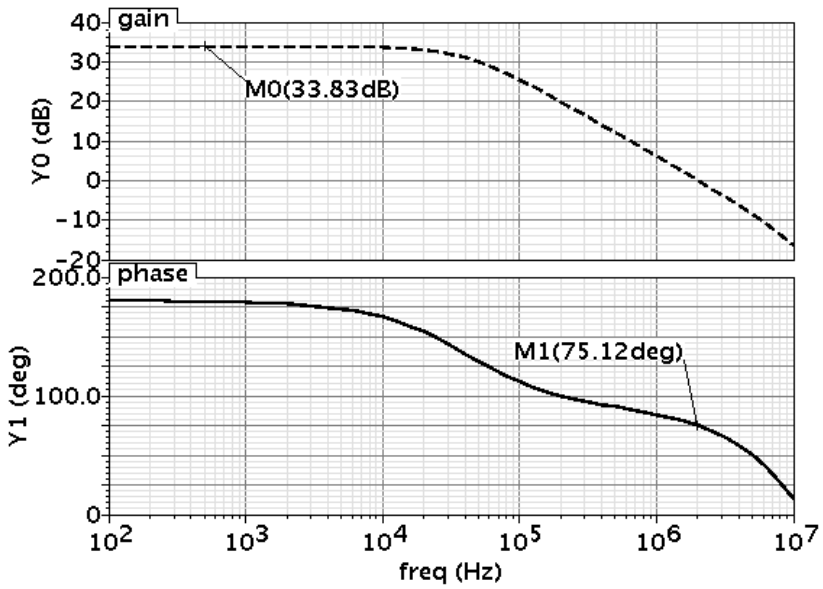


Figure 5.17 CM loop gain and bandwidth of the proposed opamp.

The proposed global CM loop mostly relies on tail current of the input stage to improve CM loop bandwidth, thus the current of the output stage needn't to be large, i.e.,

$$GBW_{CM} \approx \frac{A_{inv}(g_{m5}+g_{m6})}{2(g_{m3}+g_{m4})} \times \frac{g_{m0}}{C_{eq,L}}. \quad (34)$$

Moreover, the first item in the right site of above equation was another factor to enhance the bandwidth of the CM loop. As illustrated in Figure 5.17, transistor-level circuit simulations show that CM loop gain and bandwidth were 33.8 dB and 2 MHz with 15.6 pF for the first stage, respectively. Current of the output stage is 2.8 μA. Compared to conventional CM loop configuration, with same GBW and load capacitor, the proposed output stage saved more than 58% current. Meanwhile, the DM gain of the output stage improved by 7.4 dB. Comparison between conventional CM loop with a single NMOS transistor and the proposed CM loop is shown in Table 5.2. it can be seen that the proposed CM loop have higher gain, larger bandwidth and longer loop. The long loop of CM loop is likely to induce more poles, thus reduces phase margin of the CM loop. However, careful design of the CM loop could still leave the phase margin larger than 75°.

Table 5.2 Comparison of output stage between conventional CM loop with a single NMOS and proposed CM loop.

Output Stage	Current (μA)	CM-Gain (dB)	CM-PM (^{0})	CM-GBW (MHz)	DM-Gain (dB)	Load (pF)
Single NMOS	6.628	26.42	92.9	2	24.53	15.6
Proposed	2.796	33.83	75.1	2	31.47	15.6

5.5.4 Settling with Complimentary Diode Loading

We usually use small signal parameters to simulate an amplifier in a behavioral ΔΣ modulator model. However, in a SC integrator circuit under low-power environment, step response with large input signal could severely affect quiescent current of amplifier, thus vary dominant pole and first non-dominant pole in settling process,

and hence degrade the settling performance. This is because when input pair experiences a large excursion, output of the input stage responds quickly due to small time constant at the diode node and also experiences a relative large excursion. Not like the input pairs which have total current capped by the tail source, the relatively large excursion of the current causes the transconductance of diode to vary considerably during the transient. The slow settling behavior causes quantization noise leakage and hence significantly raises the in-band noise. In order to achieve fast settling, complementary diode is proposed to restrict the variation of total transconductance of diode pair when input pair experiences a large excursion. The total transconductance keeps less variable when the transconductance of PMOS diode increases and that of NMOS diode decreases, or vice versa. In this work, we use transistor-level simulation to investigate settling behavior of single diode structure and complementary diode structure as a low-impedance load for the proposed input pair, as well as quantization noise leakage for both structures. As illustrated in Figure 5.18, the proposed complementary diode load shows better settling performance than that with a single NMOS diode load. When the proposed amplifier settles within 0.1% error, the amplifier with a single diode load just moves into the range of 1% settling error. The settling time within 0.1% error of the proposed structure saves 33% compared to that with single diode structure. Both amplifiers in the simulation have same quiescent current, DC gain, GBW and phase margin. Figure 5.19 shows difference of the quantization noise leakage (settling noise) induced by the settling error for a –2-dBFS, 20-kHz sinusoidal input signal. The in-band noise power decreases by 95.3% for the proposed structure. This results in 94 dB of SQNR from transistor-level simulation. From another point of view, this result indicates that only

relying on small signal parameter [86, 87] may underestimate the noise power, thus degrade the performance of modulator.

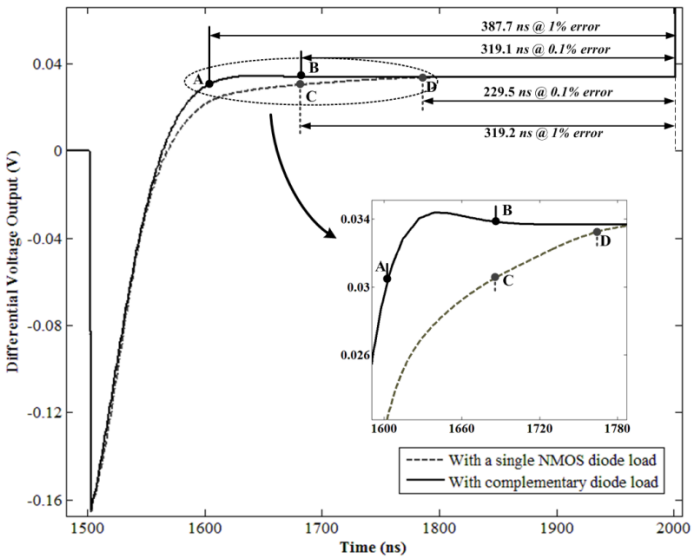


Figure 5.18 Settling behavior comparison between a single diode load and complementary diode load.

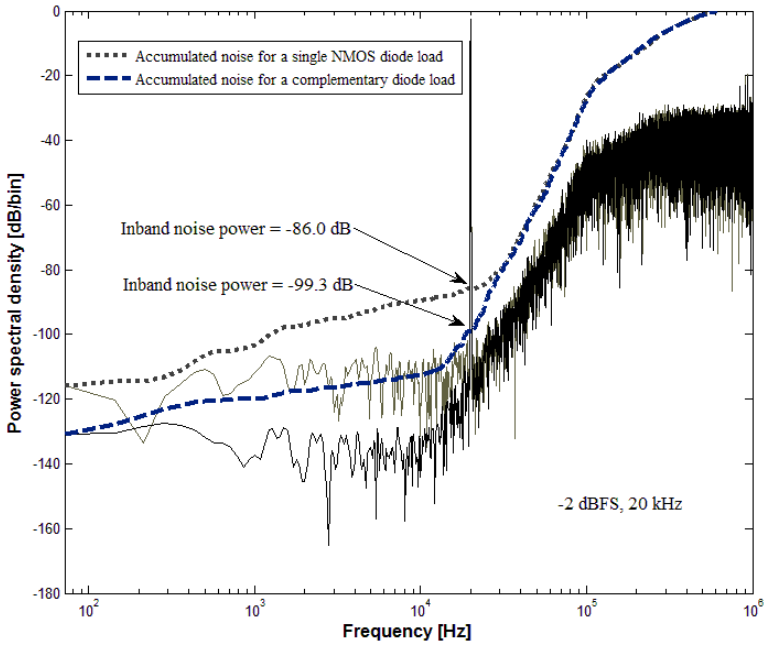


Figure 5.19 Quantization noise leakage induced by settling error.

5.5.5 Simple Reference Switch Matrix for Feedback Compensation

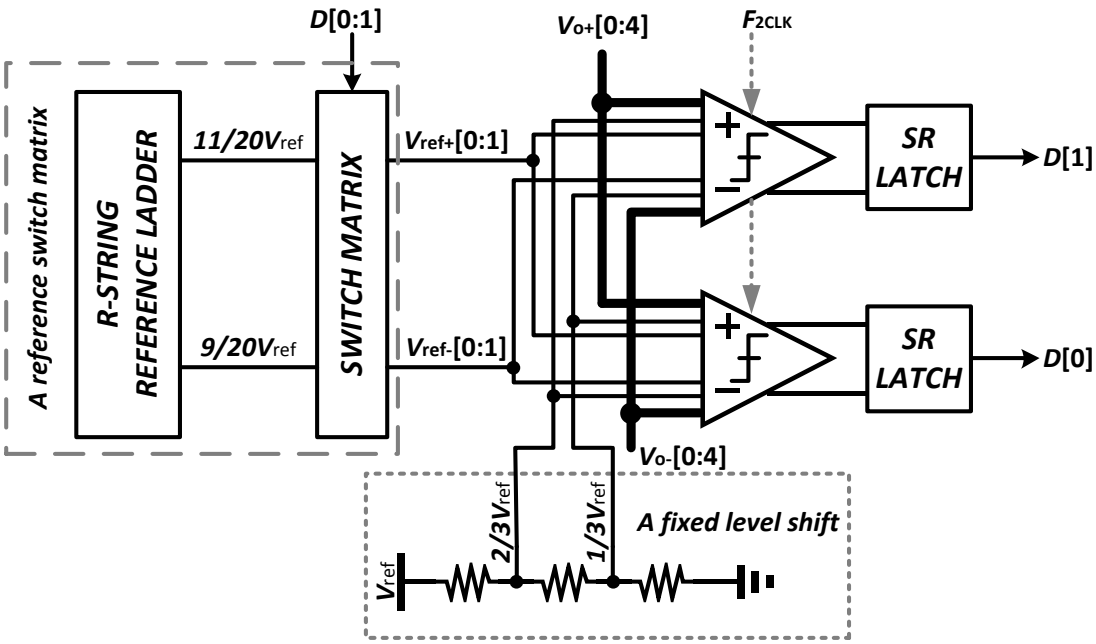


Figure 5.20 Circuits blocks of feedback compensation based on the 1.5-bit quantizer.

SC summer is frequently used in feedforward architecture for summing the outputs of each stage. However, this passive summation network suffers from attenuation by a factor of $\sum_{i=1}^{n} C_i$, where C_i is the feedforward capacitor of each stage. In a multi-bit implementation, it is necessary to use an amplifier to have gain compensation before applying to the multi-bit quantizer [65, 84]. Moreover, if double sampling scheme is employed, the area would obviously increase since the feedforward capacitors and its control switches would be doubled. This work proposes a simple reference switch matrix based on direct summation technique [73] to perform the feedback compensation for the system. Since all signals are directly fed into the multi-bit quantizer and the sum is not attenuated, the amplifier which used for gain compensation before the quantizer is removed. Figure 5.20 shows the circuit blocks of feedback compensation based on the 1.5-bit quantizer. It consists of a reference switch matrix, a fixed level shift, two multi-input comparators and two SR-latches. Bootstrapped switches are used in the switch matrix to reduce RC time constant. The

feedforward coefficients are realized by the ratio of the multi-input pair of the comparator.

5.6 Measurement Results

The prototype double-sampled fourth-order 1.5-bit input-feedforward ΔΣ modulator is fabricated in a 1P8M 0.13-μm CMOS process with MIM capacitor. The core area is 0.95×0.6 mm^2. Figure 5.21 shows the chip micrograph. The chip is packaged in a CQFP package. The feedback reference voltages which externally buffered are set to 0.5 V and 0 V.

All measurements are performed at a 2.5-MHz sampling rate. Figure 5.22 shows the measured 50k-point output spectrum for a –3.2-dBFS 3-kHz sinusoidal input. The measured SFDR is 96.0 dB. When the input amplitude reaches near the full scale, the SFDR declines to 75.8 dB at a 3-kHz. The measured SNR and SNDR versus input amplitude for a 3-kHz sinusoid is presented in Figure 5.23. Clocked at 1.25 MHz, the modulator achieves a 81.7 dB peak SNDR, 82.4 dB peak SNR and 85.0 dB DR from a 0.5-V supply. Table 5.3 summarizes the measured performance.

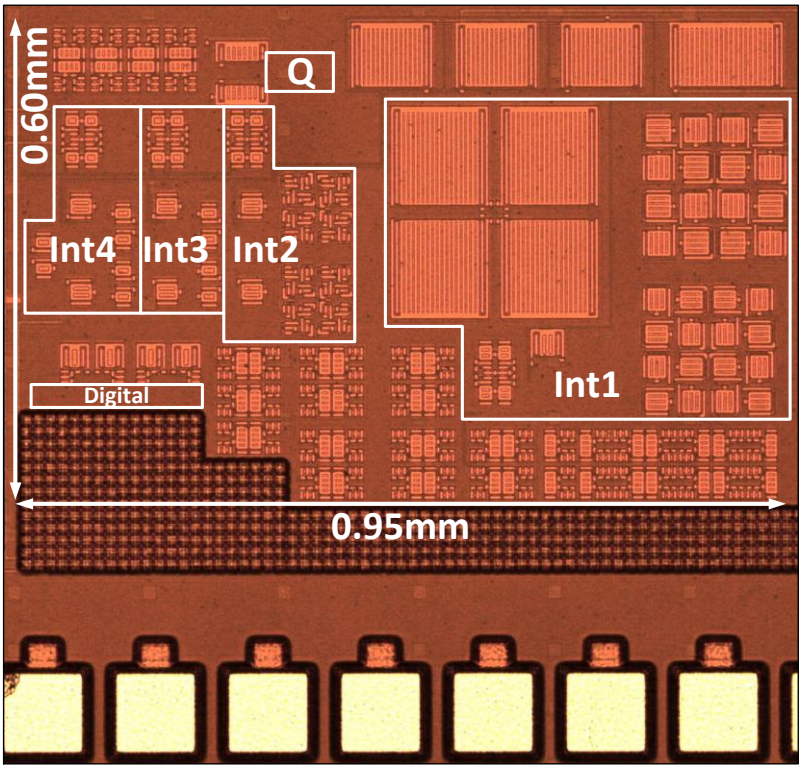


Figure 5.21 Chip photograph.

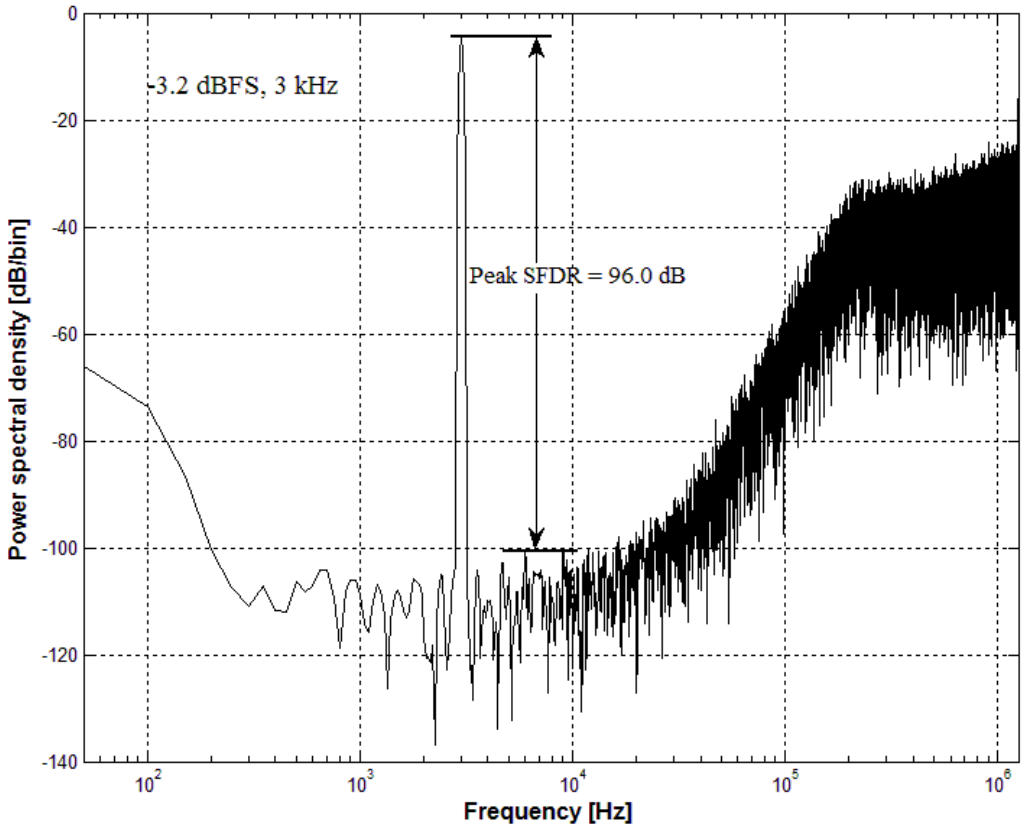


Figure 5.22 Measured output spectrum with –3.2-dBFS 3 kHz sinusoidal input.

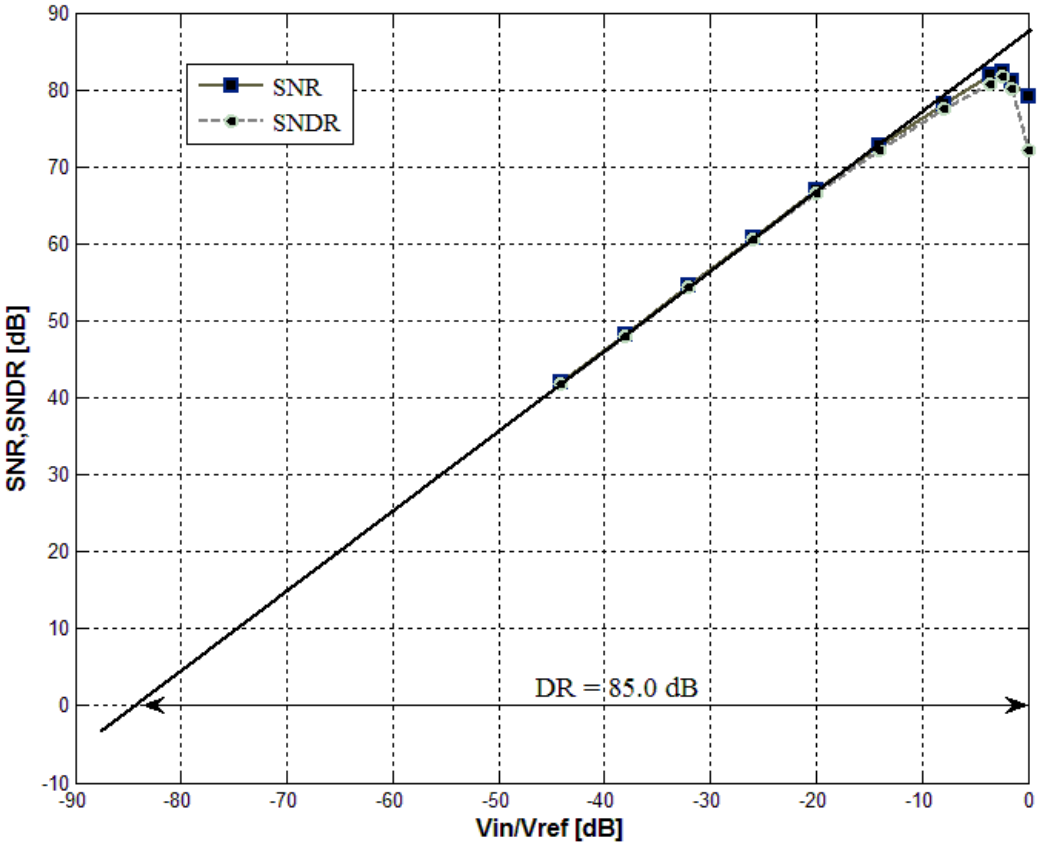


Figure 5.23 Measured SNR and SNDR versus input amplitude for a 3-kHz sinusoid.

DWA for a three level quantization may not be a critical circuit to the modulator performance. Figure 5.24 shows a performance comparison with or without DWA circuit. The result only demonstrates a slightly difference (less than 2 dB). The spectrum with or without DWA circuit for a –3.4-dBFS, 3-kHz sinusoid is presented in Figure 5.25. The result may suggest that for a small number of quantization level based on input-feedforward topology, the modulator could remove DWA circuit which is used for DAC non-linearity suppression.

Supply voltage variation does not significantly affect the modulator performance. Figure 5.26 shows peak SNDR versus supply voltage variation with reference of full supply voltage range. To order to ensure maximum input amplitude could reach full reference range and to demonstrate it at different frequency, instead of 3-kHz, a 0-

dBFS, 11-kHz sinusoidal input signal is plotted in Figure 5.27. As shown in the spectrum with large input signal, the slightly rising of noise floor may indicate the overload of input signal for the quantizer and the modulator begin to move towards unstable condition.

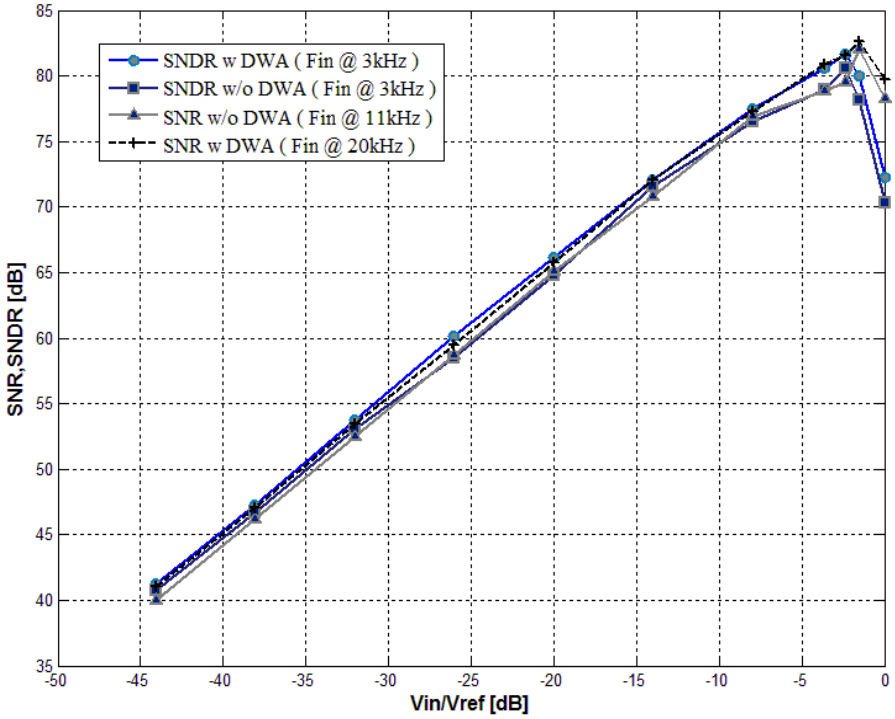
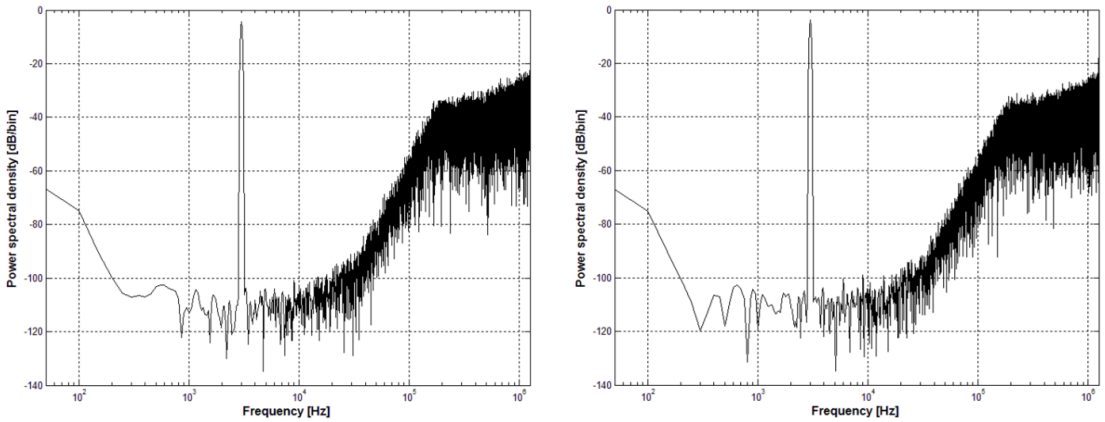


Figure 5.24 Measured SNR/SNDR versus input amplitude w/wo DWA circuit.



(a) (b)

Figure 5.25 Measured spectrum for a –3.4-dB, 3-kHz sinusoidal input signal (a) with DWA circuit, (b) without DWA circuit.

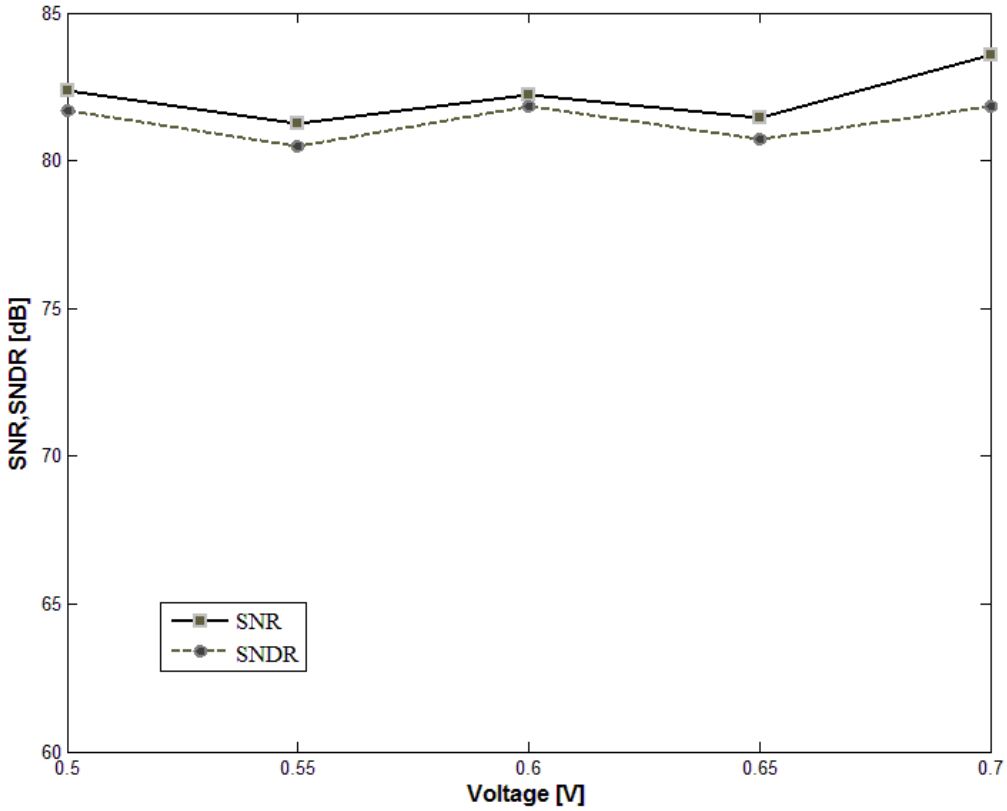


Figure 5.26 Measured SNDR versus supply voltage variation.

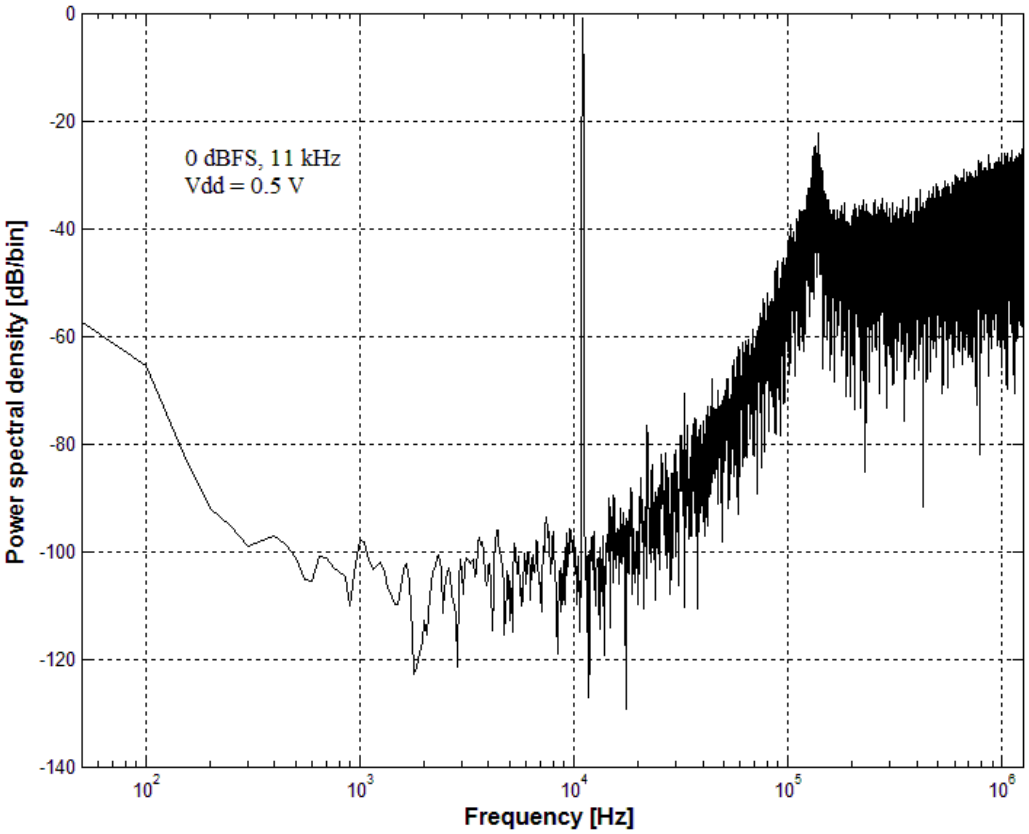


Figure 5.27 Measured spectrum for a 0-dB, 11-kHz sinusoidal input signal.

Table 5.3 Performance summary.

Parameter	Measured Value
Supply Voltage	0.5 V
Sampling Frequency	2.5 MHz
Clock Frequency	1.25 MHz
References	0 V, 0.5 V
Signal Bandwidth	20 kHz
Power Consumption	29.5(A) + 5.7(D) = 35.2 μW
Dynamic Range	85.0 dB
SFDR	96.0 dB
Peak SNR	82.4 dB
Peak SNDR	81.7 dB
Core Area	0.95 X 0.6 mm^2
Technology	0.13 μm CMOS

Table 5.4 compares the proposed modulator with other published sub-1V audio-band modulators. The improved input range makes full use of the supply range and results in high DR. a FOM, which is defined as

$$FOM = DR + 10\log(\frac{BW}{Power})$$

gives a fair comparison.

Table 5.4 Performance comparison with state-of-the-art sub-1V audio-band ΔΣ modulators.

	VDD [V]	BW [kHz]	SNDR [dB]	DR [dB]	Power [μW]	Type	CMOS [μm]	Area [mm^2]	FOM
[22]	0.9	24	89	92	1500	1.5-bit SC	0.13	1.44	164
[19]	0.9	20	73.1	83	60	1-bit SC	0.13	0.42	168
[13]	0.7	20	81	85	36	1-bit SC	0.18	0.72	172
[14]	0.7	25	95	100	870	Multi-bit SC	0.18	2.16	174
[27]	0.6	20	78	79	1000	Cascaded	0.35	2.88	152
[77]	0.6	20	81	83	34	1-bit SC	0.13	0.33	171
[88]	0.6	20	79.1	82	28.6	1-bit CT	0.13	0.11	170
[43]	0.5	25	74	76	300	1-bit CT	0.18	0.60	155
[16]	0.25	10	61	64	7.5	1-bit SC	0.13	0.34	165
This	0.5	20	81.7	85	35.2	1.5-bit SC	0.13	0.57	173

5.7 Conclusion

A double-sampled modulator based on input-feedforward topology has been successfully fabricated. Measurement result shows that the proposed sampling network with scaled input sampling capacitor enables full input range which is superior to other existing single-bit modulator. The proposed amplifier combined with global CMFB, complementary diode and inverter output stage demonstrates unique compatibility with low-voltage low-power circuit. Only consume 35.2 μW from a 0.5 V supply voltage, this modulator achieves 85.0 of DR.

CHAPTER 6

CONCLUSION AND FUTURE WORKS

6.1 Conclusion

The rapid development of portable and handheld device demands for low-voltage low-power analog-to-digital converters. This study presents two low-voltage low-power ΔΣ modulators for audio applications. Different techniques are employed in these works to minimize power consumption while maintaining SNR as high as approximate 80 dB.

First prototype chip demonstrates a 0.7-V audio-band ΔΣ modulator. It utilizes a 2-tap FIR filter to reduce the power of quantization noise, resulting substantially reduction of integration step at the first stage. The modulator also employs a double sampling input network to balance the equivalent load capacitance of the first stage. Compared to other sub-1V high-performance audio-band ΔΣ modulator [14, 22], i.e., more than 90 dB of DR, this work exhibits much lower power consumption, thanks to power-efficient analog building blocks and compact circuit implementation. Compared to other sub-1V sub-100 μW audio-band ΔΣ modulator [19, 20], this work demonstrates an improvement of at least more than 6 dB of DR from the same supply voltage. However, the power consumption of the work seems slightly higher due to overdesign of the digital circuits.

The main task in low-voltage low-power ΔΣ modulator design is to minimize power consumption, as well as maintaining high performance. In order to reduce power consumption, a new fully differential amplifier is proposed in second work. Output stage of the differential amplifier consists of an inverter. Inverter is well known for its push-pull character and free from constraints of slew rate. The simulation shows that this sort of amplifier has high slew rate and low quiescent current. Compared to conventional current mirror amplifier, it saves more than 58% of power consumption. Based on simulation, it is found that traditional current mirror amplifier with a single diode load exhibits slow settling when its input signals experience a large excursion. The slow settling behavior causes quantization noise leakage and hence considerably raises the in-band noise power. In order to obtain fast settling, complementary diode is proposed to alleviate the variation of total transconductance of diode pair when input pair experiences a large excursion. Ideally, the total transconductance remains relative constant as the transconductance of PMOS diode increases and that of NMOS diode decreases, or vice versa. The settling time (0.1% error) is reduced by 33 % and the in-band noise power is decreased by 95.3%. Low-power design consideration is also carried out on the system level. The double sampling input feedforward structure is developed based on three levels quantization. The simulation results show that 94 dB of SQNR is obtained without any local feedback loop or downstream resonator. The input range, within which the modulator is stable, only reaches 0.7 of reference for 1 or 1.5 bit quantizer. This is intrinsic inferior than that for a multi-bit quantizer, which could achieve full range of reference voltage. This indicates that multi-bit modulator has advantages over single-bit modulator for low-voltage low-power ΔΣ modulator. However, this sacrifice is remedied in double sampling scheme since the input sampling capacitor and reference feedback capacitor are intrinsically separated.

It is found that the input signal range achieves full reference if the input sampling capacitor is scaled to 0.7 of the feedback capacitor. This indicates 3 dB improvement of peak signal power of the modulator. Moreover, compared to single sampling scheme, the doubled effective OSR reduces the thermal noise power to half.

This study develops a double-sampled input-feedforward ΔΣ modulator. The measurement results show the total power consumption of the modulator is ultra-low, i.e., approximate 35 μW from a 0.5 V supply voltage, meanwhile the SNR could remain as high as approximate 80 dB. Theoretical analysis predicts that an approximate 4 dB improvement of SNR could be obtained in the work. However, there are several limitations in the analysis. Firstly, the digital power consumption is not taken into consideration. It should be noted that this is not a critical issue since the part of digital power only contribute to 5% ~ 10% of total power consumption for a power-efficient single-bit modulator. Therefore, the analysis result is basically fair. Secondly, the feedback delay in double sampling scheme might more severely affect its settling behavior than that in single sampling scheme. This limitation might be even critical since low supply voltage prolongs the delay time. This work restrains the delay time within 10% of each integration period.

6.2 Future Works

There are several interesting directions for future work:

One alternative way to achieve high performance is based on multi-bit quantization for low-voltage low-power ΔΣ modulator. This sort of modulators demonstrates robust stability of system and achieves ultra-high SNR from low supply voltage, for

example., more than 100 dB of SNR from a 0.7-V supply voltage [23]. However, with continuing reduction of supply voltage, the difference of quantization levels may be smaller than the offset voltage due to mismatch, thus the non-linearity of quantization level might significantly reduce the performance of modulator. Except for the common used voltage mode quantizer, the expression of quantization level could also be diverse. For example, a frequency mode quantizer, i.e., VCO-based quantizer, might achieve good performance as well [89, 90].

For modulators those work under ultra-low supply voltage [91, 92], suppose 0.2 V, the expression of quantization variables might be much different from those operated under higher supply voltage. They might utilize frequency [28, 93] or time difference [94-96] to replace voltage difference under such low supply voltage since frequency or time variables are unrelated to supply voltage. Frequency-based modulator prefers first-order noise shaping [97] and could be implemented in mostly digital fashion [29]. However, first-order noise shaping character makes modulator significantly rely on high OSR to improve signal bandwidth. The subsequently high frequency clock signal makes even digital circuit difficult to design.

In summary, single-loop high-order modulator with a multi-bit quantizer using an alternative variable might contribute towards the future of low-voltage low-power ΔΣ modulator.

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