HIGH-K DIELECTRICS IN METAL INSULATOR METAL (MIM) CAPACITORS FOR RF APPLICATIONS

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Abstract

The thesis provided some solutions to address the challenges faced by the metal-insulator-metal (MIM) capacitor technology for the radio frequency (RF) and analog-mixed signal (AMS) applications. The MIM capacitors for the RF and AMS applications have requirements of high capacitance densities and low quadratic voltage coefficients of capacitance (VCCs) and leakage currents. To address these conflicting requirements, MIM capacitors using stacked dielectrics of a high-k dielectric on SiO_2 were proposed.

The MIM capacitors comprising thin film SiO_2 formed by atomic layer deposition (ALD) at 200 and 400 °C were characterized for the first time. The MIM capacitor with 4 nm ALD SiO_2 deposited at 400 °C achieved a low leakage current of 2×10^{-7} A/cm^2 at 3.3 V, a high field strength of 19 MV/cm, and a high operation voltage of 3.6 V for 10-year lifetime. The leakage currents through ALD SiO_2 were shown to be at least 10 times smaller than those through SiO_2 deposited by PECVD (plasma enhanced chemical vapour deposition). Moreover, the negative quadratic VCC of SiO_2 was explained by modeling the polarization in SiO_2 as a sum of the electronic, ionic and orientation polarization in which the former 2 are relatively independent of the electric field. The orientation polarization however reduces with increasing electric field, giving rise to the negative quadratic VCC in SiO_2.

The MIM capacitors with sputtered Er_2O_3 on ALD SiO_2 stacked dielectrics were then demonstrated to have excellent performance. An optimized MIM capacitor with 8.9 nm Er_2O_3 on 3.3 nm ALD SiO_2 deposited at 400 °C had a capacitance density of 7 fF/μm^2, a quadratic VCC of -89 ppm/V^2 at 100 kHz, a leakage current of 10^{-8} A/cm^2 at 3.3 V, a dielectric field strength of 8.6 MV/cm and an operation voltage

of 5.1 V for a 10-year operation lifetime. With leakage currents of ~10^{-7} A/cm^2 at 3.3 V and ~10^{-8} A/cm^2 at 2 V, the MIM capacitors with capacitance densities of 7.5 and 8.6 fF/μm^2 and quadratic VCCs less than 100 ppm/V^2 were also demonstrated with the Er_2O_3 (7 nm)/ALD SiO_2 (3.3 nm) (deposited at 400 °C) and Er_2O_3 (8.8 nm)/ALD SiO_2 (2.3 nm) (deposited at 200 °C) stack dielectrics.

Lastly, the stack dielectrics of Er_2O_3 on ALD SiO_2 were also investigated for the high voltage (20 V) applications. Although the MIM capacitors with single layer Er_2O_3 or HfO_2 demonstrated a notable performance: capacitance density of 2.6 fF/μm^2 and low quadratic VCC (less than 20 ppm/V^2), the leakage currents were still very high, about 4×10^{-5} A/cm^2 at -20 V. Using the stack dielectric of Er_2O_3 on ALD SiO_2 deposited at 400 °C, a high capacitance density of 2.5 fF/μm^2 and a low leakage current of ~1×10^{-6} A/cm^2 at -20 V was achieved. Having low quadratic VCCs, the capacitance densities obtained in this work were much higher than 0.5-1 fF/μm^2 obtained by the Si_3N_4 MIM capacitors, indicating that the Er_2O_3/SiO_2 stacked dielectric is a potential structure to be used in the MIM capacitors for high precision, high voltage applications.

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List of abbreviations and symbols

AC	alternating current
ALD	atomic layer deposition
AMS	analog/mixed signal
CET	capacitive equivalent thickness
CMOS	complementary metal-oxide-semiconductor
DC	direct current
IC	integrated circuits
ITRS	International Technology Roadmap for Semiconductor
MIM	metal-insulator-metal
MIS	metal-insulator-silicon
PECVD	plasma enhanced chemical vapor deposition
PVD	physical vapor deposition
RF	radio frequency
VCC	voltage of coefficient of capacitance

α	quadratic voltage coefficient of capacitance
β	linear voltage coefficient of capacitance
C	capacitance density
C_0	capacitance density at zero bias
ε_r	dielectric constant of a dielectric
J	leakage current through a dielectric
E	electric field across a dielectric

Chapter 1

Introduction

1.1. Radio Frequency and Analog/Mixed-Signal Technology

In this information era, the world witnesses an explosive growth of communication devices such as mobile phones, personal computers and tablets with wireless internet capability, GPS (global positioning system) and etc. The radio frequency (RF) and analog/mixed-signal (AMS) technologies play crucial roles in those wireless devices, in which the RF signals are converted into digital data and vice versa. As the market requires smaller and thinner products, all the components including memory, micro-processing unit, RF and analog/mixed signal modules are often integrated in a system-on-a-chip (SOC). Scaling of the active components (CMOS transistors) successfully increased the density of the transistors on the chip and reduced the die size, following Moore's law. However, the RF and analog/mixed signal circuit performance depends significantly on the performance of the passive components, mainly consisting of inductors, resistors and capacitors. These passive components cannot be scaled down as fast as the active components, because of the precise resistance, capacitance, and impedance levels needed to process an analog

signal. The number of passive components increased significantly in the modern wireless systems due to more complex analog signals. The passive components occupy 60-70% of the total area of an RF and analog-mixed signal module [1]. The exact percentages of resistor, inductor and capacitor are not known, however, the worldwide consumptions of capacitor, resistor and inductor in 2006 were 67%, 23% and 10% of the total 25 billion USD, respectively [2]. This infers that the capacitors occupy about 67% of the total passive components.

1.2. **MIM capacitors in the RF and AMS circuits**

Among the passive components in the RF and AMS circuits, the capacitors are needed in the coupling and decoupling circuits, oscillator, phase shift, filter, analog to digital, digital to analog converters and etc. A charged capacitor blocks the DC (direct current) component but allows the AC (alternating current) component of a signal; as such it is used to separate the AC from the DC component (coupling). The capacitor is also used to decouple a circuit from another, such that the noise from one circuit is shunted and does not affect the rest of the circuit. Capacitors are the main elements of filters, such as low pass, band pass and high pass filters. The reactance of a capacitor is inversely proportional to the frequency, and thus the impedance of the filter at certain frequency can be adjusted, blocking or allowing the frequency to pass. The diagrams of a simple oscillator, phase shift circuit, decouple capacitors and analog to digital converters are shown in Fig. 1-1. The analog to digital converter [Fig. 1-1 (d)] uses an array of capacitors to digitalize an analog signal into different discrete digital signals [3].

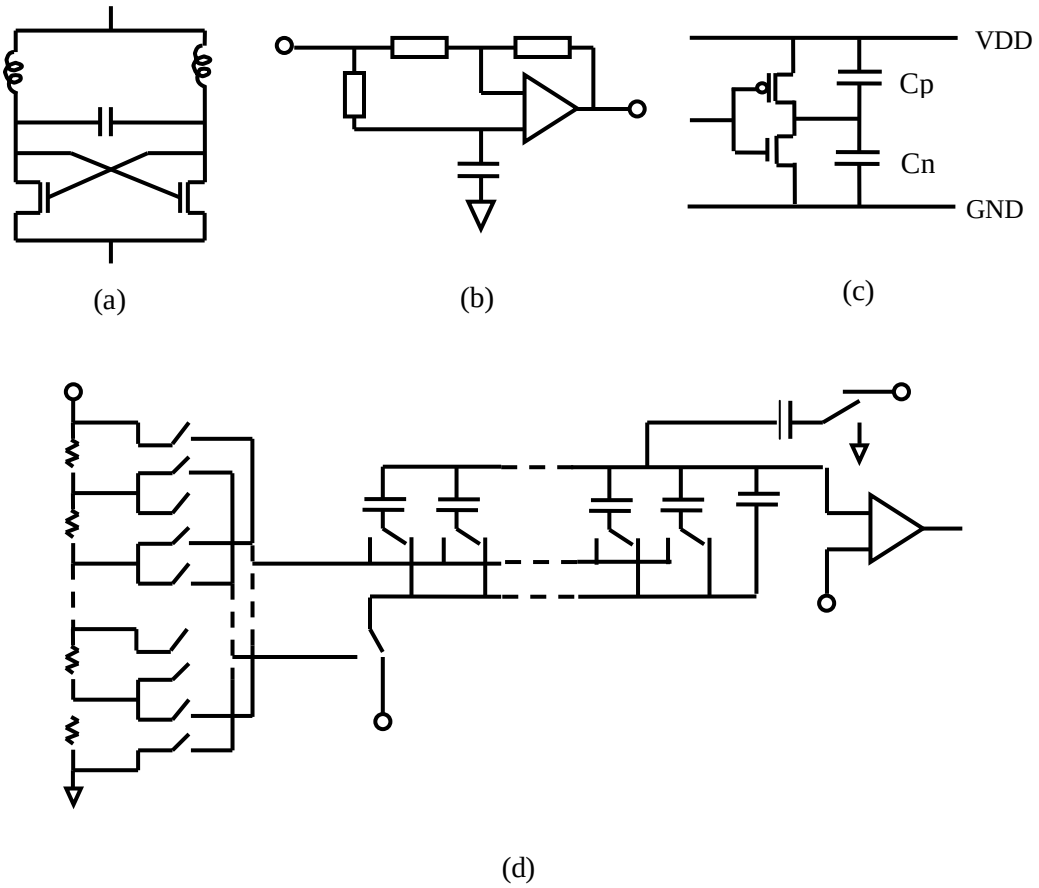

Fig. 1-1: Some applications of the MIM capacitors in the RF and AMS circuit: (a) cross coupled LC oscillator, (b) phase shift circuit, (c) decoupling capacitors, and (d) analog-digital converters.

As illustrated in Fig. 1-2, the metal (polysilicon)-insulator-silicon (MIS) capacitors were initially used in the silicon circuits [4-5]. The MIS capacitor was then replaced by the polysilicon-insulator-polysilicon capacitor because the latter has smaller voltage coefficient of capacitance (VCC) and stray capacitance [6]. Metal-insulator-polysilicon and metal-insulator-polysilicide structures were also investigated [7-8]. The traditional polysilicon-insulator-polysilicon capacitors however have several issues: depletion of polysilicon electrodes, high resistivity, and excessive capacitance loss due to the substrate [8-10]. As such, the metal-insulator-metal (MIM) capacitor became the next generation capacitor for RF and AMS integrated circuit, with depletion free, low resistivity electrodes and low capacitance loss [11-14].

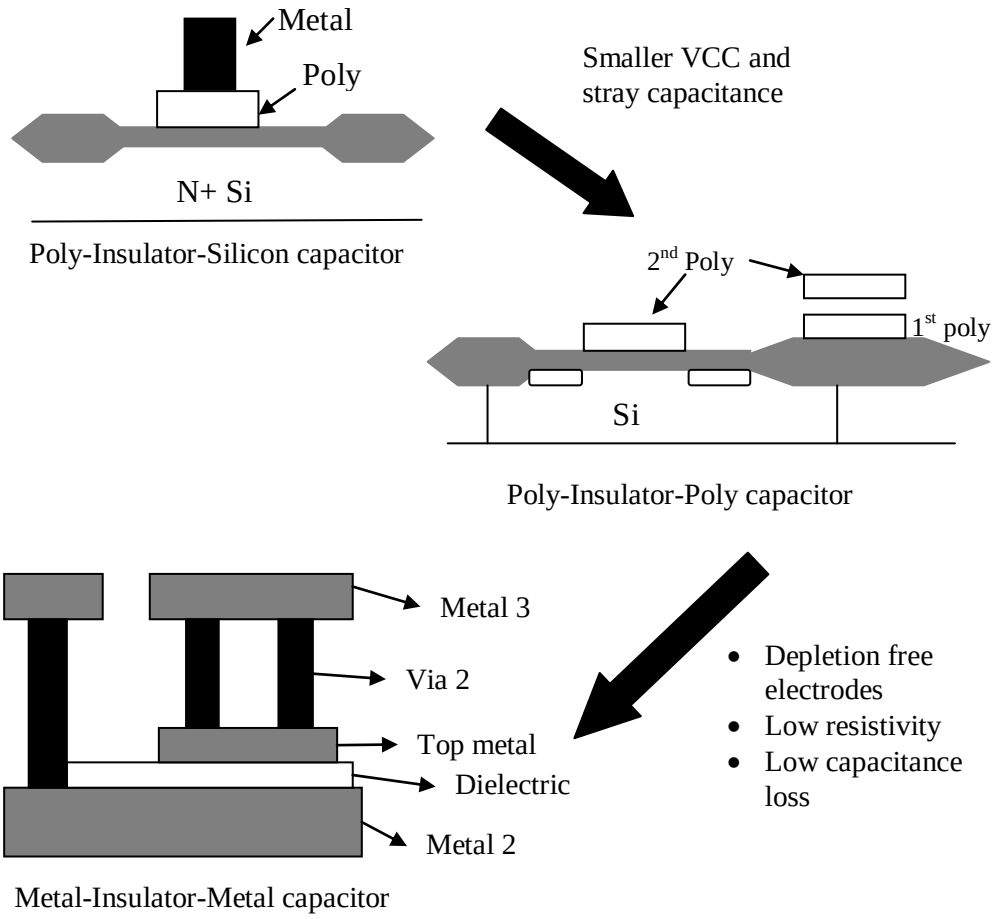

Fig. 1-2: Development of capacitors for silicon integrated circuit from poly-insulator-silicon structure [4] to poly-insulator-poly [6] and metal-insulator-metal structures.

Since the MIM capacitors are used in two major applications: RF application and DRAM (dynamic random access memory) in which the capacitor is used as the charge storage, it is important to distinguish the difference in the requirements for both applications. The capacitor for RF and AMS circuit is required to have low quadratic voltage coefficient of capacitance (VCC) of less than 100 ppm/V^2 (hence it is usually called high precision capacitor) and a density of 7 fF/μm^2 for year 2013-2015 [15]. These capacitors are fabricated after the first metal line is formed and thus to be compatible with the back-end-of-line (BEOL) process with Al and Cu metal lines, the process temperature is limited to 400 °C. The requirements for DRAM are

very different: each capacitor to have a cell size less than 0.0061 μm^2, a capacitance density of 25 fF/cell [15] and most importantly small VCC is not needed. The capacitor for DRAM application is fabricated at the front-end-of-line (FEOL) and thus high temperature process is often used to reduce the leakage current and increase the capacitance density. The requirements of a capacitor for RF and AMS application are further discussed in chapter 2.

1.3. **Motivation of the thesis**

The capacitors occupy about 67% of the passive components, thus an effective way to reduce the size of the RF and AMS circuit is to increase the capacitance densities of the capacitors. The International Technology Roadmap of Semiconductor (ITRS) suggests the capacitance density requirement for MIM capacitors for RF and AMS circuit of 7, 10 and 12 $fF/\mu m^2$ for the year 2013, 2016, and 2020, respectively [15]. Moreover, the leakage currents and quadratic VCC are required to be smaller than 10^{-8} A/cm^2 and 100 ppm/V^2, respectively. These requirements can only be achieved by implementing high-k dielectrics in the MIM capacitor. However, as reviewed in chapter 2, most of the high-k dielectrics have very high quadratic VCCs, which increase with the capacitance densities. The motivation of this thesis is to fabricate MIM capacitors having high capacitance densities, low quadratic VCCs (less than 100 ppm/V^2), and low leakage currents (less than 10^{-8} A/cm^2). The process temperature of the capacitors is limited to 400 °C to be fully compatible with the BEOL process.

1.4. **Thesis outline and contributions**

The technology and literature review of recent works on the MIM capacitors for RF and AMS integrated circuits using high-k dielectrics are presented in chapter 2.

In chapter 3, the MIM capacitors with single layer SiO_2 deposited by plasma enhanced chemical vapor deposition (PECVD) and atomic layer deposition (ALD) are investigated. The ALD SiO_2 was deposited at 200 °C and 400 °C. The findings in this chapter are used to analyze the data obtained in chapter 4 and 5. Moreover, the negative quadratic voltage of coefficients (VCC) of SiO_2 is successfully modeled for the first time.

In chapter 4, a high capacitance density, high precision MIM capacitor with Er_2O_3 on ALD SiO_2 stacked dielectrics is demonstrated to have very low quadratic VCC of less than 100 ppm/V^2 and leakage currents of less than 10^{-8} A/cm^2. This work is among the first to demonstrate the usage of ALD SiO_2 and Er_2O_3 in MIM capacitor for RF and AMS integrated circuits.

Chapter 5 expands the MIM capacitor study to high operation voltage applications. MIM capacitors with HfO_2, Er_2O_3 single layer and Er_2O_3/SiO_2 stacked dielectrics are thoroughly investigated with an operation voltage of 20 V. Different post deposition treatments are also studied.

Chapter 6 concludes the findings from the studies and suggests possible future research directions.

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Chapter 2

Literature and Technology Review

2.1. Requirements of an MIM capacitor for RF and AMS integrated circuits

The three major requirements of an MIM capacitor for RF and AMS applications are high capacitance density, low leakage current and small voltage linearity. The International Technology Roadmap for Semiconductor (ITRS) suggests the capacitance density requirements of 7 and 10 $fF/\mu m^2$ for the year 2013 and 2016 respectively (Table 2-1) [1], while the leakage currents and voltage linearity must be less than 10^{-8} A/cm^2 and 100 pm/V^2, respectively. SiO_2 and Si_3N_4 were the conventional dielectrics used in the MIM capacitors [2-5], but their capacitance densities were often less than 2 $fF/\mu m^2$. Although Si_3N_4 has a higher dielectric constants than SiO_2 (~7 as compared to 3.9), the frequency dependence of the nitride capacitor is more significant than that of the SiO_2 capacitors [3, 6]: the quadratic VCC of MIM capacitor with 30 nm Si_3N_4 can vary from 30 to 300 ppm/V^2 when the frequency is reduced from 1 MHz to 200 kHz. Reducing the thicknesses of SiO_2 and Si_3N_4 to achieve higher capacitance density is not possible because of the high

leakage current. To attain a capacitance density of 7 fF/μm^2, the thickness of the SiO_2 layer must be less than 4.93 nm. As such, it is inevitable that high-k dielectrics are needed in the MIM capacitors for RF applications.

Table 2-1: International Technology Roadmap for Semiconductor (ITRS), year 2010 [1]. Work group: RF and A/MS Technologies for Wireless Communications.

Year	2012	2013	2014	2015	2016	2017	2018
Capacitance density (fF/μm^2)	5	7	7	7	10	10	10
Voltage linearity (ppm/V^2)	<100	<100	<100	<100	<100	<100	<100
Leakage current (A/cm^2)	<1E-8	<1E-8	<1E-8	<1E-8	<1E-8	<1E-8	<1E-8
Q (5 Ghz for 1pF)	>50	>50	>50	>50	>50	>50	>50

The requirements by the ITRS present a major challenge: if the dielectric thickness is scaled down to increase the capacitance density, both the leakage current and the quadratic voltage of coefficient of capacitance (VCC) will increase. The quadratic VCC is derived from the capacitance versus voltage curve, in which the capacitance of an MIM capacitor can be fitted into a quadratic equation:

$$C = C_0(1 + \beta V + \alpha V^2), \tag{2-1}$$

where α and β are the quadratic and linear VCC, respectively. The linear VCC (β) can be eliminated by circuit designs such as cross-coupled arrangement [7]. The quadratic VCC (α) causes a bowing effect to the transfer curve in the analog-digital and digital-analog converters as shown in Fig. 2-1 [8] which affects the resolution and accuracy of the converter, and thus α needs to be less than 100 ppm/V^2. The quadratic VCCs of

the MIM capacitors often increase with their capacitance densities and in many dielectrics such as HfO_2 [9], Sm_2O_3 [10] and Al_2O_3 [11], the quadratic VCC is inversely proportional to the square of the dielectric thickness. Except for SiO_2, Si_3N_4, and Ta_2O_5, the quadratic VCC of reported high-k dielectrics are mostly positive. The quadratic VCC of SiO_2 is always negative and the quadratic VCC of Si_3N_4 can change from negative to positive after a post deposition treatment [5]. The mechanism for the voltage dependence of capacitance is not fully understood, however, several models were presented. The positive quadratic VCC of the high-k dielectric was explained by the ionic polarization model: displacements of metal cations in the dielectric from their equilibrium positions under an electric field generates field depending dipoles [11]. The origin of the positive quadratic VCC was also explained by an electrostriction model: the induced strain in the dielectric under an electric field causes the deformation of the dielectric [12], and thus the capacitance density varies with the applied electric field.

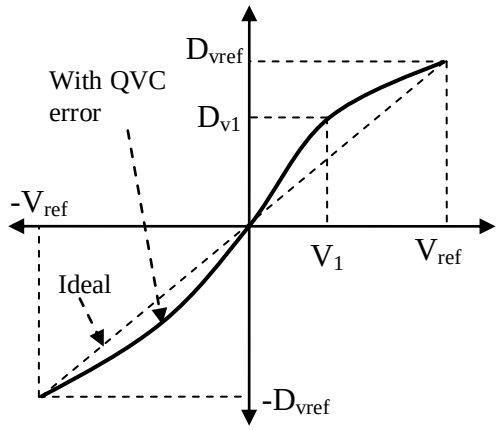

Fig. 2-1: Analog-digital converter transfer curve with and without quadratic voltage coefficient (QVC) error.

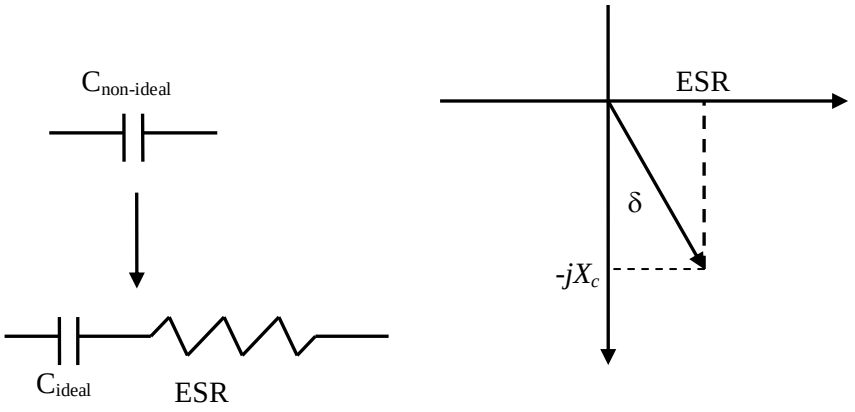

Fig. 2-2: Illustration of the dissipation factor (loss tangent δ).

Another important parameter shown in Table 2-1 is the quality factor Q, which is a reciprocal of the dissipation factor of the MIM capacitor. For each oscillation, electric power is dissipated, often in a form of heat. A non-ideal capacitor can be modeled as an ideal lossless capacitor with an equivalent series resistance (ESR). In the phasor diagram shown in Fig. 2-2, the dissipation factor ($\tan\delta$) is the tangent of the angle δ between the impedance vector and the negative y-axis, and given by the equation:

$$\tan\delta = \frac{ESR}{|X_c|}. \qquad (2\text{-}2)$$

Some other important performance parameters of the MIM capacitors for RF and AMS applications are frequency dependency, dielectric field strength and time-dependent-dielectric breakdown (TDDB) performance. When the frequency increases, the dipole in the dielectric cannot switch directions fast enough. The effective dipole moment is smaller, and that results in a smaller capacitance density. This effect is more significant in ferroelectrics (PZT, $BaTiO_3$ and BST) than in paraelectrics (SiO_2, Al_2O_3, Ta_2O_5) [13]. While no change in dielectric constant of SiO_2, Al_2O_3, and Ta_2O_5 is observed for frequency from 100 Hz to 1 MHz, fast reductions by 20 to 50% are

seen for PZT, $BaTiO_3$ and BST. The dielectric field strength and TDDB performance affect the reliability and the operation voltage of the MIM capacitors. The capacitor is often subjected to a constant voltage stress test, and the times to breakdown under different stress voltages are used to estimate the operation voltage that allows the capacitor to operate continuously for 10 years.

The MIM capacitors are fabricated at the back end of line (BEOL), above metal line 1. As such, the process temperature of these capacitors is limited to about 400 °C to prevent issues such as diffusion of dopants in Si, material expansion and contraction, softening of metal lines, metal diffusion, and compound formation. A post-deposition treatment is usually carried out to improve the quality of the high-k dielectrics after the low temperature deposition.

2.2. **High-k dielectrics**

Various high-k dielectrics have been investigated in recent years. The objectives were to optimize the capacitance density, the quadratic VCC and the leakage currents of the MIM capacitors. This section briefly reviews some of the dominant works on the high-k dielectrics in the MIM capacitors for RF applications. The insulators used in these works can be classified into two types: single layer dielectrics and stacked dielectrics. The former type can be subcategorized into binary metal oxides and ternary metal oxides (and above). The stacked dielectrics are insulators with several types of dielectrics stacking on each other, such as HfO_2 on SiO_2 [14] or $Al_2O_3/HfO_2/Al_2O_3$ stack [15].

2.2.1 **Binary metal oxide**

The simplicity of the deposition methods (some of which can be done by sputtering) makes binary metal oxides popular choices in the MIM capacitor studies. Among these binary oxides, Al_2O_3, HfO_2, and Ta_2O_5 were extensively investigated for RF applications. Recently, rare-earth high-k dielectrics such as Sm_2O_3, La_2O_3, and Y_2O_3 also received much research attention.

Al_2O_3

Al_2O_3 has several characteristics suitable for the precision MIM capacitor applications: small capacitance dependency on frequency [16], low leakage current due to its large band gap of 6.6-6.7 eV [17-18], and a medium dielectric constant of about 8 to 10 [19-20]. A 12 nm PVD (sputtered) Al_2O_3 layer was reported to achieve a leakage current of 4.3×10^{-8} A/cm^2 at 1 V, a capacitance density of 5 fF/μm^2, corresponding to a *k* value of about 6.6 [16]. The quadratic VCC however was larger than 2000 ppm/V^2. Using atomic layer deposition (ALD), the capacitance density of 13 nm Al_2O_3 was 6.05 fF/μm^2 (corresponding to dielectric constant of 8.9), with a leakage current of 4.8×10^{-8} A/cm^2 at 3V [20]. The quadratic VCC is however still very high, about 795 ppm/V^2 measured at 1 MHz. The quadratic VCC of Al_2O_3 was explained by S. Becu *et al.* using an ionic polarization model: the displacement of the metal cation from its equilibrium position under an electric field induced an ionic polarization which susceptibility had a quadratic relation with the electric field [11, 21]. Although Al_2O_3 MIM capacitors have low leakage currents and low frequency dispersion, their quadratic VCCs are much higher than the required 100 ppm/V^2.

Ta_2O_5

The dielectric constant of Ta_2O_5 is about 25 [22], which is 3 times higher than that of Al_2O_3. A dielectric constant of 90 to 110 could be achieved when Ta_2O_5 was in a defect free crystalline form, which typically required a high temperature treatment of 800 °C [23]. As such Ta_2O_5 was used in dynamic random access memory (DRAM) [24-26] and seen as one of the candidates for the MIM capacitors for RF and AMS application. Y.L. Tu *et al.* demonstrated an MIM capacitor with MOCVD Ta_2O_5 which optimized both the capacitance density (4 fF/μm^2) and the quadratic VCC (-9.9 ppm/V^2) [27]. Similar result was also obtained by Y.K. Jeong *et al.* [28]. However, the leakage through Ta_2O_5 layer was usually high, which could be 10^5 times higher than those of SiO_2 and Si_3N_4 having the same thickness [29]. Due to its small bandgap, the leakage current through Ta_2O_5 also increased significantly with temperature [30].

HfO_2

HfO_2 was extensively studied as a high-k gate dielectric to replace SiO_2 in the Si CMOS transistors due to its high dielectric constants (~25) and medium band gap (5.7 eV). It was natural that HfO_2 was also investigated as the insulator of the MIM capacitors for RF and AMS applications. With a quadratic VCC less than 100 ppm/V^2, an MIM capacitor with 50 nm PVD HfO_2 achieved a capacitance density of 3.3 fF/μm^2 with a leakage current of 9×10^{-8} A/cm^2 at 5 V [31]. By reducing the thickness of the dielectric, higher capacitance of 13 fF/μm^2 was achieved with 10 nm ALD HfO_2 [9]. Using pulsed-laser deposition (PLD) HfO_2, a 3 fF/μm^2 capacitor with quadratic VCC less than 200 ppm/V^2 and very low leakage current of 2×10^{-9} A/cm^2 at 3V was also demonstrated [32]. However, the HfO_2 capacitor with a capacitance

density of 7 fF/ μm^2 had a quadratic VCC higher than 1000 ppm/V^2 [9]. Moreover, HfO_2 is not easily etched after crystallization, which occurs at a temperature as low as 400 °C [33], a standard temperature used for post dielectric deposition anneal to improve the dielectric quality.

Rare earth metal oxides

Sm_2O_3, La_2O_3, and Y_2O_3 were recently investigated in precision MIM capacitors for RF and analog applications. A capacitance density of 7.5 fF/μm^2, and a quadratic VCC of 234 ppm/V^2 was demonstrated with PVD Sm_2O_3 MIM capacitor after the dielectric was treated in N_2 plasma [34]. High capacitance density of 9.2 and 6.9 fF/ μm^2 were achieved by MIM capacitors with 22 and 29 nm La_2O_3 dielectrics, respectively [35]. The quadratic VCCs were more than 1000 ppm/V^2 and below 100 ppm/V^2 when the frequency was in megahertz and gigahertz range, respectively. However, the leakage currents were about 10^{-4}-10^{-3} A/cm^2 for the La_2O_3 dielectrics. An MIM capacitor with low quadratic VCC of 248 ppm/V^2 was demonstrated with a 29 nm thick Y_2O_3 film, yielding a capacitance density of 2.3 fF/μm^2 [36]. When the thickness was reduced to 8 nm to achieve a 8.5 fF/μm^2 capacitance density, the quadratic VCC increased significantly to 14100 ppm/V^2 [36]. A Pr_2O_3 MIM capacitor was also reported to achieve a capacitance density of 9.1 fF/μm^2 with a leakage current of 10^{-7} A/cm^2 at 1V, and a quadratic VCC of 1310 ppm/V^2 [37].

2.2.2 **Ternary metal oxide**

A binary oxide with high dielectric constant often has smaller band gap, as shown in Fig. 2-3 after Robertson [22, 38]. As shown in the inset of Fig. 2-3, the

dielectric constant *k* is related to the band gap (E_g) as k ~ $1/E_g^{1.8}$. It is possible to adjust the dielectric constant and the band gap of an oxide by adding another element into the binary oxide to form a ternary oxide. In the MIM capacitor studies for the RF applications, majority of the ternary oxides are hafnium (Hf), tantalum (Ta) or titanium (Ti) based ternary oxides.

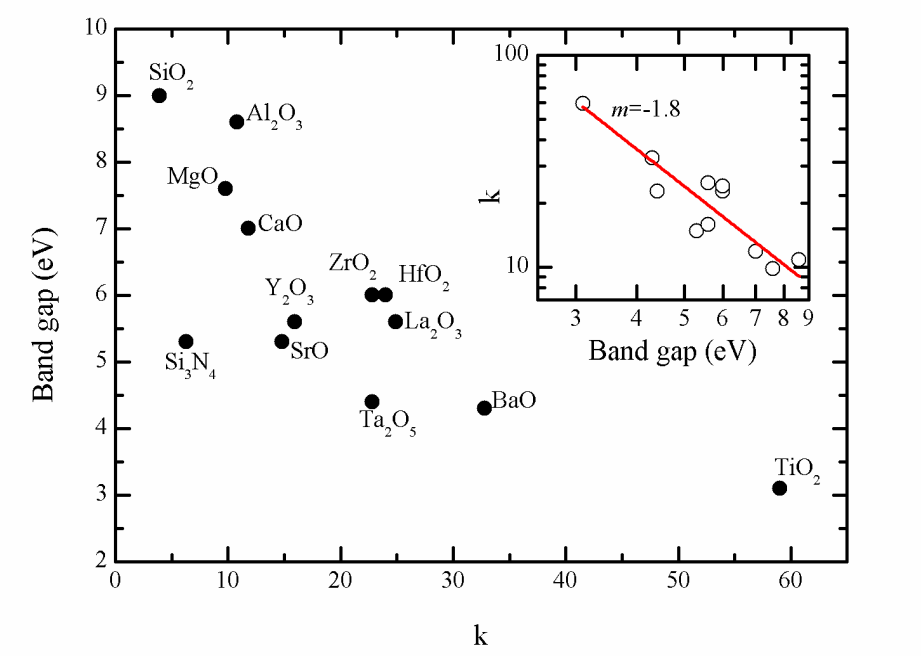

Fig. 2-3: Band gap (E_g) versus dielectric constant (*k*) of several binary oxides [22]. Inset: log(*k*) versus log(E_g) showing that k ~ $1/E_g^{1.8}$.

Hafnium (Hf) based ternary oxide

Ternary or higher oxides make use of two or more metal oxides to utilize the advantage from each individual oxide. For instance, by tuning the stoichiometric ratio, the band gap and permittivity of Hf-Al oxide can be adjusted between those of Al_2O_3 and HfO_2. MIM capacitors with sputtered $HfAlO_x$ having capacitance densities of 3.5 to 6 fF/μm^2 and respective quadratic VCCs of 143 to 583 ppm/V^2 were reported [39]. The leakage currents were however as high as 10^{-4} and 10^{-2} A/cm^2 at 3V for the 3.5 and 6 fF/μm^2 capacitors, respectively. In another work, the leakage through ALD

$(HfO)_{1-x}(Al_2O_3)_x$ reduced from 1×10^{-6} to 5×10^{-8} A/cm^2 as x increased from 0 to 1, due to the increase in the band gap of the dielectric [40], however the capacitance density and quadratic VCC also decreased and increased, respectively with increasing x. For x = 0.14, the MIM capacitor with $(HfO)_{1-x}(Al_2O_3)_x$ was optimized with a capacitance density and a quadratic VCC of 3.5 fF/µm^2 and 180 ppm/V^2, respectively [40]. An MIM capacitor with 8% La- HfLaO deposited by ALD had high dielectric constant of 38 after 500 °C anneal [41]. Having low leakage currents of about 10^{-8} A/cm^2, the capacitances of 7.5 to 16 fF/µm^2 were achieved with HfLaO thickness ranged from 45 to 15 nm. The quadratic VCCs however, were higher than 1000 ppm/V^2. An MIM capacitor with PVD HfTbO also achieved high density of 13.3 fF/µm^2 and low leakage current of 2×10^{-7} A/cm^2 at 3.3V, but with a quadratic VCC of 2667 ppm/V^2 [42].

Tantalum (Ta) based ternary oxide

Since the dielectric constant of Ta_2O_5 can be as high as 110 [23], Ta was added to many ternary oxides to achieve higher dielectric constants. An MIM capacitor with TaZrO dielectric was demonstrated to achieve a capacitance density of 12 fF/µm^2 and a leakage current of 10^{-8} A/cm^2 at 1V [43]. The quadratic VCC however was higher than 1000 ppm/V^2. MOCVD SrTaO and BiTaO were reported to have very high dielectric constant of 20 and 50, respectively [44]. With 10 fF/µm^2 capacitance density, the leakage current at 3V was in the order of 10^{-8} A/cm^2. The quadratic VCCs were 200 and 600 ppm/V^2 at 1 MHz for SrTaO and BiTaO, respectively. However, SrTaO needs a 500 °C anneal to achieve these performances. By doping Ta_2O_5 with Al_2O_3 to form $AlTaO_x$, high capacitance density of 17 fF/µm^2

was obtained, with a leakage current of 9×10^{-7} A/cm^2 at –2 V [45]. The quadratic VCC however was not mentioned in ref. [45].

Titanium (Ti) based ternary oxide

The dielectric constant of TiO_2 is as high as 170, depending on its lattice orientation [46-47]. With the addition of Ti into the ternary oxide, the dielectric constant of the high-k dielectric can be increased substantially. Several Ti based ternary oxides were studied as the dielectrics of the MIM capacitors for RF and AMS integrated circuit. The dielectrics giving excellent performance were $SrTiO_3$, TiTaO, TiCeO, and TiZrO. Among the 4 dielectrics, $SrTiO_3$ has the highest dielectric constant, up to 300 [48]. An MIM capacitor using $SrTiO_3$ achieving high capacitance density of 44 fF/μm^2 and low leakage current of 5×10^{-7} A/cm^2 (at 1V) was demonstrated [49]. The quadratic VCC changed from >3000 ppm/V^2 at 1 MHz to less than 100 ppm/V^2 at 10 GHz [49], indicating that this capacitor is suitable for the gigahertz frequency range. With a dielectric constant of 45, TiTaO MIM capacitor was demonstrated to have a density of 14.3 fF/μm^2, a quadratic VCC and leakage current at 2V of 634 ppm/V^2 and 2×10^{-7} A/cm^2, respectively [50]. In another work by Lukosius *et al.* [51], the dielectric constant of TiTaO deposited by ALD was 50, close to the value reported by Chiang *et al.* [50]. The quadratic VCC was expected to reduce below 100 ppm/V^2 when the thickness of TiTaO is higher than 40 nm (corresponding to a capacitance density of 11 fF/μm^2). The leakage current at 2V for the 40 nm TiTaO MIM capacitor however was in the order of 10^{-6} A/cm^2. Besides TiTaO, TiCeO was also reported to have large dielectric constants of 45 [52]. MIM capacitors using TiCeO with dual interface plasma treatment was reported having a capacitance density of 10.3 fF/μm^2, a leakage current at -2V of 4.7×10^{-7} A/cm^2 and a

quadratic VCC of 866 ppm/V^2 [52]. TiZrO has a dielectric constant of 28 [53], which is about half of those of TiTaO and TiCeO. Cheng *et al.* reported in ref. [53] a TiZrO MIM capacitor with a capacitance density of 5.5 fF/μm^2, a quadratic VCC of 105 ppm/V^2 and a leakage current of 4×10^{-8} A/cm^2. TiCeO is more suitable than TiZrO in capacitance effective thickness (CET) scaling and quadratic VCC optimization [52].

MIM capacitors with 15 nm TiLaAlO and TiLaYO dielectrics deposited by co-sputtering were also shown to have high capacitance densities of 24 and 16.4 fF/μm^2, respectively and the leakage currents at -2 V were in the order of 10^{-7} A/cm^2 [54]. The quadratic VCCs were however about 1900 ppm/V^2 [54]. It is worth noting that other Ti based ternary oxides such as $PrTi_xO_y$ and $AlTiO_x$ were also studied, however the performance was not as good as TiTaO, TiCeO and TiZrO reviewed above. The quadratic VCCs were more than 1000 ppm/V^2 for $PrTi_xO_y$ MIM capacitors with densities of 5 to 10 fF/μm^2 and the leakage currents were in the order of 10^{-6} A/cm^2 (at 1V) [55]. A 10 fF/μm^2 $AlTiO_x$ MIM capacitor was shown to have very high leakage current of 10 A/cm^2 at 2V and a large capacitance reduction with increasing frequency [16].

2.2.3 **Stacked dielectrics**

Stacked dielectrics of two or more dielectrics have similar benefits as the ternary oxide: to harness the strength from the individual dielectric layer, such as high dielectric constant for high capacitance density and large band gap for small leakage current. This review discusses several MIM capacitor works for RF applications using stacked dielectrics on SiO_2, Hf based oxide and Ta_2O_5.

Stacked dielectrics with SiO_2

While the quadratic VCCs of the MIM capacitors using single layer high-k dielectric are positive, SiO_2 MIM capacitor has a negative quadratic VCC. Si_3N_4 also displayed negative quadratic VCC under certain processing condition [5]. Several works exploited the negative quadratic VCC of SiO_2 to compensate the positive quadratic VCC of a high-k dielectric to achieve very small quadratic VCC. Kim *et al.* stacked 12 nm ALD HfO_2 on 4 nm PECVD SiO_2 and demonstrated an MIM capacitor with a capacitance density of 6 fF/μm^2 and a quadratic VCC of 14 ppm/V^2 [14]. Using a similar concept, Yang *et al.* [34, 56] and Chen *et al.* [10] demonstrated MIM capacitors with Sm_2O_3 stacked on SiO_2, achieving low quadratic VCC and high capacitance density of up to 7.9 fF/μm^2. Wenger et al. [57] also demonstrated an MIM capacitor with $Pr_2Ti_2O_7$ on SiO_2 stacked dielectrics having a quadratic VCC smaller than 100 ppm/V^2, however, the capacitance density was only 3.2 fF/μm^2. The quadratic VCC in the high-k dielectric/SiO_2 stack was tuned by changing the thickness ratio of the high-k dielectric and SiO_2. The advantage of this method is that the low quadratic VCC and high capacitance density can be concurrently achieved. The disadvantage of this method is the low dielectric constant of SiO_2, and thus SiO_2 is required to be very thin which leads to a high leakage current. The leakage currents of MIM capacitors with a capacitance density of 7 fF/μm^2 reported in ref. [10, 34, 56] were from 10^{-7} to 10^{-6} A/cm^2. The leakage current can be reduced by improving the quality of the high-k dielectrics and SiO_2.

Stacked dielectrics with Hf based oxide:

HfO_2 on Al_2O_3 stacked and laminated dielectrics were reported in many works on MIM capacitors for RF applications. Laminated $Al_2O_3/HfO_2/Al_2O_3$ (AHA) MIM

capacitors demonstrated low leakage currents, high capacitance density and high reliability [15, 58]. A capacitance density of 12.8 fF/μm^2 with a leakage current at 2 V of 7.45×10^{-9} A/cm^2 was demonstrated with A-H-A-H-A laminated dielectrics, where A and H are Al_2O_3 (1 nm) and HfO_2 (5 nm) respectively [58]. The quadratic VCC was still high, at 1990 ppm/V^2 [58]. Another laminated AHA MIM capacitor with a capacitance density of 3.1 fF/μm^2 demonstrated a leakage current at 3.3V as low as 10^{-9} A/cm^2, and a quadratic VCC of 100 ppm/V^2 [15]. The quadratic VCC of the MIM capacitor with $Al_2O_3/HfO_2/Al_2O_3$ dielectrics can be minimized by reducing the Al_2O_3 to HfO_2 ratio [59], however, this is traded off by a lower breakdown voltage. The lowest α reported in [59] was about 1000 ppm/V^2 for an 8 fF/μm^2 capacitor with Al_2O_3 (1 nm)/HfO_2 (15 nm)/Al_2O_3 (1 nm) stack. The MIM capacitor with $HfO_2/HfO_xC_yN_z/HfO_2$ (HNH) was also reported to have a better time dependent dielectric breakdown (TDDB) characteristic and a lower quadratic VCC than those of the MIM capacitors with laminated Al_2O_3/HfO_2 [60] because the $HfO_xC_yN_z$ layer suppressed the crystallization of HfO_2. The MIM capacitor with HNH achieved a capacitance density of 8.8 fF/μm^2, a leakage current at 3V of 1.5×10^{-8} A/cm^2 and a quadratic VCC of 700 ppm/V^2. The MIM capacitors with HfLaO/$LaAlO_3$/HfLaO (HLH) dielectric stack deposited by ALD were shown to have similar quadratic VCC scaling and better leakage currents than those of MIM capacitors with AHA laminated dielectric [41]. A 7.4 fF/μm^2 HLH capacitor had a leakage current at 3.3 V of 3×10^{-9} A/cm^2, and a quadratic VCC of 700 ppm/V^2 [41]. The HLH capacitor however has a poorer reliability than the MIM capacitor with HfLaO single layer.

Stacked dielectrics with Ta_2O_5

As reviewed earlier, Ta_2O_5 dielectric has a good quadratic VCC performance, but its leakage current was high. The dielectric stacks with Ta_2O_5 aims to harness the low quadratic VCC of Ta_2O_5 and utilize the other dielectric to reduce the leakage current. An MIM capacitor with $Ta_2O_5/HfO_2/Ta_2O_5$ (THT) laminated dielectrics was reported with good performance [28]: a quadratic VCC of 16.9 ppm/V^2, a capacitance density of 4 fF/μm^2 and a leakage current of 1×10^{-7} A/cm^2 measured at 3.3V and 125 °C. This is much better than the leakage performance of the single layer Ta_2O_5 MIM capacitor [28]. Ta_2O_5 was also reported stacking with Al_2O_3, achieving low leakage currents in the range of 10^{-7} to 10^{-8} A/cm^2 [27, 61], thanks to the barrier layer Al_2O_3. Capacitance densities of 4.4 and 9.2 fF/μm^2 with corresponding quadratic VCCs of 400 and 3580 ppm/V^2 were demonstrated by the MIM capacitors with Ta_2O_5 (40 and 16 nm, respectively) sandwiching between two 3 nm Al_2O_3 barrier layers [61].

2.3. Other parameters affecting the performance of the MIM capacitors

Besides the dielectrics used in the MIM capacitors, other parameters such as the deposition method, the post-deposition treatment and the choice of metal electrodes were shown to affect the performance of the MIM capacitors, especially on the leakage currents and quadratic VCC. A dielectric can be deposited by several methods: physical vapour deposition (PVD), plasma enhanced chemical vapor deposition (PECVD), metal organic chemical vapor deposition (MOCVD) and atomic layer deposition (ALD). PVD is among the simplest and cheapest deposition methods and it can be performed at room temperature. The dielectric can be sputtered from a

metal oxide target, or from a metal target in an oxidizing environment. PECVD uses reactive gases (SiH_4+N_2O and SiH_4+NH_3) with plasma to deposit the oxides (SiO_2 and Si_3N_4, respectively) at a deposition temperature from 250 to 400 °C. MOCVD and ALD use metal precursors to deposit the dielectric at a temperature of about 400 °C. MOCVD of Ta_2O_5 uses Tert-Butylimido-Tris(Diethylamido)Tantalum (TBTDET) with an oxidizing agent (O_2) and carrier gas (N_2) while plasma enhanced ALD of Ta_2O_5 uses Ta ethoxide $C_2H_5OTa(OC_2H_5)_4$ as precursor in oxygen plasma environment [62]. The dielectric films formed by MOCVD and ALD generally have higher quality than those by PECVD and PVD in terms of uniformity, defect density and stoichiometric ratio control. The leakage current and dielectric constant of an MIM capacitor depends on the dielectric deposition method. The leakage current through the plasma enhanced ALD Ta_2O_5 is a hundred times smaller than that through the MOCVD Ta_2O_5 [62]. ALD Al_2O_3 was also shown to have lower leakage currents and higher dielectric constants than PVD Al_2O_3 [16, 20].

Post-deposition treatments are often performed to improve the quality of the dielectric: to reduce water absorption, improve the interface, passivate the defects, enhance the dielectric constants and reduce the quadratic VCC. A high-k dielectric in crystallized form often has higher dielectric constant than in amorphous form, for instance, the dielectric constant of Ta_2O_5 after a 800 °C anneal increases from ~25 to ~110 [23], and HfLaO dielectric constant change from ~22 to ~30 and ~39 after a 420 °C and 500 °C anneal, respectively [41]. Crystallized dielectrics such as HfO_2, ZrO_2 may have larger leakage currents than the amorphous one, due to the formation of grain boundaries [63-64]. However, it is worth noting that Ta_2O_5 in polycrystalline form has a lower leakage current than in amorphous form [65]. The post dielectric deposition treatment often leads to a significant quadratic VCC reduction, while

maintaining the capacitance density of the MIM capacitor. A simple PDA at 400 °C with traced O_2 reduced the quadratic VCC of Sm_2O_3 and Sm_2O_3/SiO_2 stack by almost 2 times [10, 34, 56]. Besides annealing the dielectrics, some treatments were also performed on the metal electrodes. NH_3 and O_2 plasma treatment on the bottom TaN electrode before the deposition of TiCeO was shown to reduce the leakage current, improve the uniformity of TaN electrode and increase the capacitance density, as compared to the untreated sample [52].

The choice of metal electrodes often affects the leakage current and the capacitance density of the MIM capacitor. A high potential barrier between the metal and the high-k dielectrics often leads to a lower leakage current. A better interface between the dielectric and gate metal gives a higher capacitance density [52]. The HfO_2 capacitor with Al top electrode was shown to have lower capacitance density and leakage current than that with Cu electrode [31]. Similarly TiO_2-LaYO (TLYO) with Ir electrode had much lower leakage current than TLYO with TaN electrode [54].

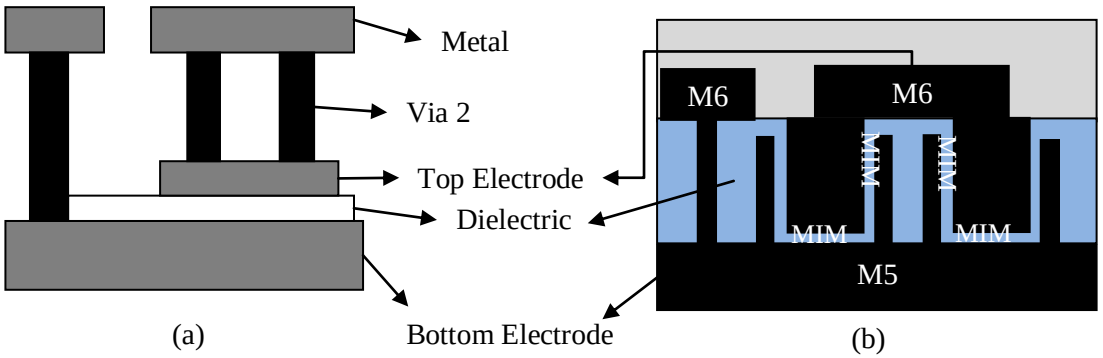

Fig. 2-4: (a) planar (2D) MIM structure and (b) 3D damascene MIM structure.

Another option to increase the capacitance density of an MIM capacitor is to use a 3D damascene MIM capacitor structure, instead of the conventional 2D planar

structure as illustrated in Fig. 2-4. The 3D structure uses the vertical dimension to increase the total surface area and the capacitance of the MIM capacitor by almost 2 times, without changing the circuit area [66].

2.4. **Summary**

The quadratic VCC versus capacitance density of the reviewed binary, ternary and stacked dielectrics are shown in Fig. 2-5. As shown in the figure, all the binary dielectrics do not satisfy both the quadratic VCC and capacitance requirement. Sm_2O_3 nearly satisfy the requirement. For ternary oxides, TiTaO has the potential to satisfy the ITRS requirement for the year 2016 (10 fF/μm^2 and 100 ppm/V^2). TiTaO however has a large leakage current, higher than 10^{-6} A/cm^2 at 2V for a 10 fF/μm^2 capacitor [51]. For the stack dielectrics, only the MIM capacitors with Sm_2O_3 on SiO_2 stack dielectrics satisfy the ITRS requirement for year 2013, however the leakage currents are higher than 10^{-7} A/cm^2 which are 10 times higher than the value required by the ITRS. This thesis adopts the stacking of a high-k dielectric on SiO_2 approach, because high capacitance density and low quadratic VCC can be achieved concurrently when the thicknesses of high-k and SiO_2 are properly matched. This work uses SiO_2 deposited by atomic layer deposition (ALD), which is believed to yield lower leakage current than PECVD SiO_2. Moreover, a new high-k material Er_2O_3 is investigated for the stacked dielectrics.

The 3D MIM structure is highly promising in delivering very high capacitance density, however the fabrication process is more complicated than that of a planar MIM capacitor. Since the foundation of the 3D MIM capacitor is still a 2D planar capacitor, this thesis only investigates 2D MIM capacitors with low quadratic VCC

and high capacitance density. The results can be applied to the 3D structures in future works.

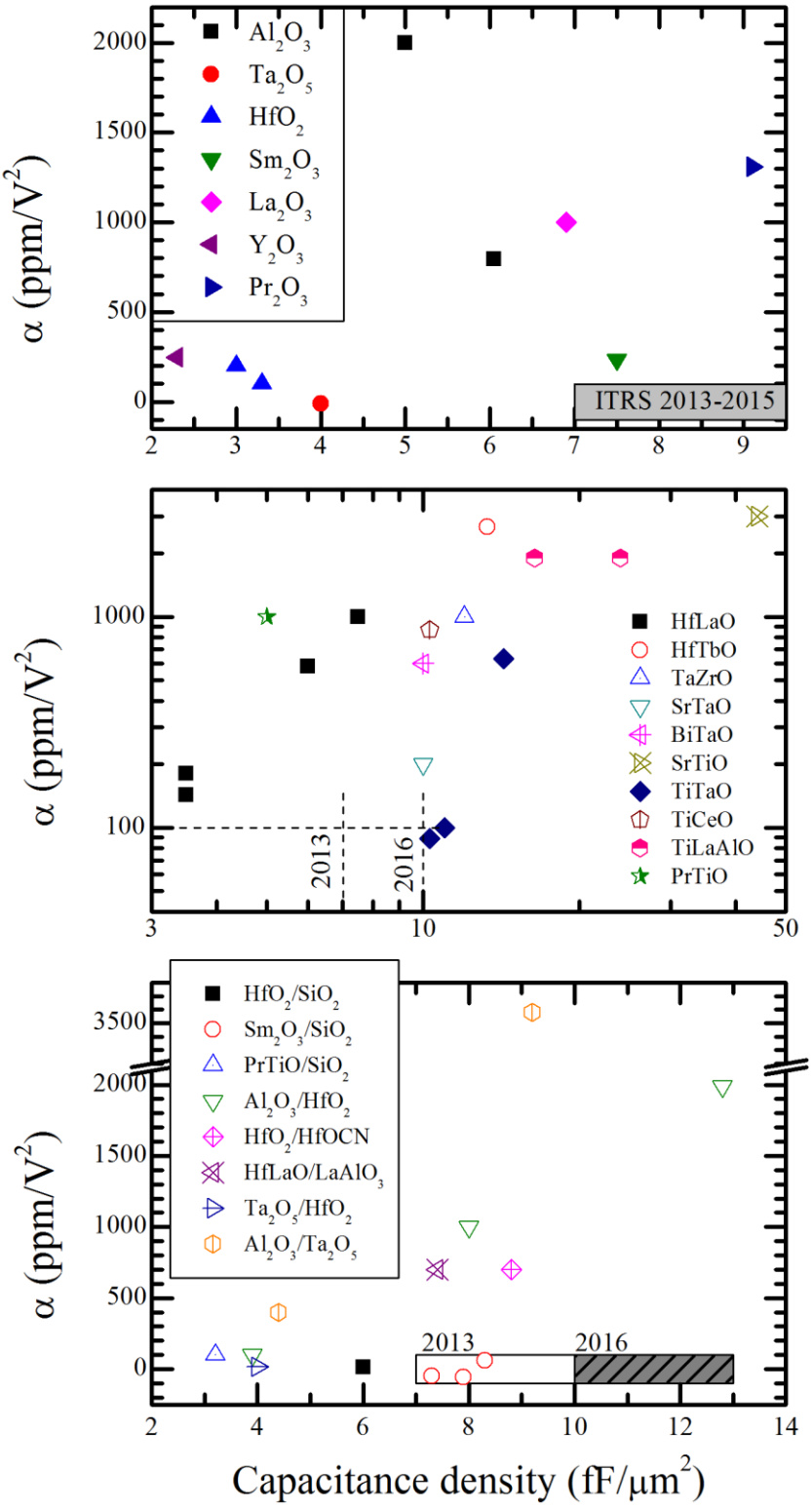

Fig. 2-5: Quadratic VCC versus capacitance density of the reviewed binary (top graph), ternary (middle graph) and stacked dielectrics (bottom graph). ITRS capacitance density requirement for 2013 and 2016 are 7 and 10 fF/μm^2, respectively.

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Chapter 3

Silicon Dioxide (SiO_2) for MIM Applications

3.1. **Introduction**

Silicon dioxide (SiO_2) has been widely used in many applications, such as complementary metal-oxide-semiconductor (CMOS) process, metal-insulator-metal (MIM) capacitors, and micro-electro-mechanical system (MEMS). Thermal oxide by dry oxidation at high temperature (800-1200 °C) was used as the gate dielectric of the CMOS transistors until it was replaced by hafnium based high-k dielectrics. In the MIM capacitor, plasma enhanced chemical vapour deposition (PECVD) SiO_2 deposited at a low temperature was used as the dielectric of the capacitors with low capacitance densities and high breakdown voltages [1-3]. PECVD SiO_2 was also stacked with HfO_2 [4] and Sm_2O_3 [5-6] to achieve high-capacitance density with low quadratic voltage coefficient of capacitance (VCC). In recent years, atomic layer deposition (ALD) of SiO_2 was extensively studied [7-11] for advanced Si CMOS technology due to its high film quality and excellent thickness controllability. An ultrathin ALD SiO_2 layer is used as an interfacial layer between the silicon substrate and the high-k gate dielectric to improve the Si-dielectric interfacial quality [12] and

to prevent interfacial reaction [13]. There is significant interest to study and evaluate ALD SiO_2 to be used in the MIM capacitors for RF and AMS integrated circuits.

The first part of this chapter studies the performance of the MIM capacitors with PECVD SiO_2 subjected to different post-deposition treatments. The second part characterizes the MIM capacitors with ALD SiO_2 deposited at low temperatures of 200 and 400 °C, denoted as SiO_2 (200C) and SiO_2 (400C), respectively. The electrical and capacitance performance including the capacitance density, quadratic voltage coefficient of capacitance (VCC), leakage current, and reliability are examined. A comparison between PECVD SiO_2 and ALD SiO_2 are made, and the advantage of ALD SiO_2 is assessed. The last part of this chapter models the negative quadratic VCC observed in SiO_2 where the existing models of the positive quadratic VCC in high-k dielectrics [14-15] fail to explain.

3.2. **MIM capacitors with PECVD SiO_2**

3.2.1 **Experiments**

On Si substrates coated with 200-nm-thick thermally-grown SiO_2, the bottom TaN electrode was formed by sputtering from a Ta target in N_2 and O_2 environment. SiO_2 layers were then deposited by PECVD to achieve thicknesses of 7 to 13 nm. Two post-deposition treatments were performed on selected samples: post-deposition anneal (PDA) at 400 °C for 2 mins in O_2 and N_2 ambient and N_2 plasma treatment at 200 °C for 5 mins. The treatment conditions and the thicknesses of the SiO_2 layers are listed in Table 3-1. The top TaN electrode was then formed by sputtering, after which lithography and etching was used to pattern the top electrodes of the MIM capacitors.

Table 3-1: The anneal conditions and the thicknesses of PECVD SiO_2 in the MIM capacitors.

Split	Specified thickness (nm)	Anneal condition (nm)
S1	7 nm	No anneal
S2	8nm	
S3	11nm	
S4	12nm	
S5	7 nm	400 °C, 2 mins, 5% O_2
S6	8nm	
S7	11nm	
S8	12nm	
S9	7 nm	N_2 plasma treatment, 5 mins 200 °C
S10	8nm	
S11	11nm	
S12	12nm	

3.2.2 **Results and Discussion**

The *C-V* measurements were performed at frequency f=100 kHz with the applied bias swept from -10 to 10 V. From the C-V plots, the values of capacitance C_0 at 0 V were extracted, and by using the equation $\Delta C / C_0 = (C - C_0) / C_0 = \alpha V^2 + \beta V$, the *C-V* plots were normalized to $\Delta C/C_0$ versus *V* plots to extract of quadratic and linear VCC (α and β values, respectively). The normalized $\Delta C/C_0$-*V* curves shown in Fig. 3-1 (a) belong to samples S1-S4, corresponding to the MIM capacitors with different SiO_2 thicknesses that were not subjected to any treatment. The normalized

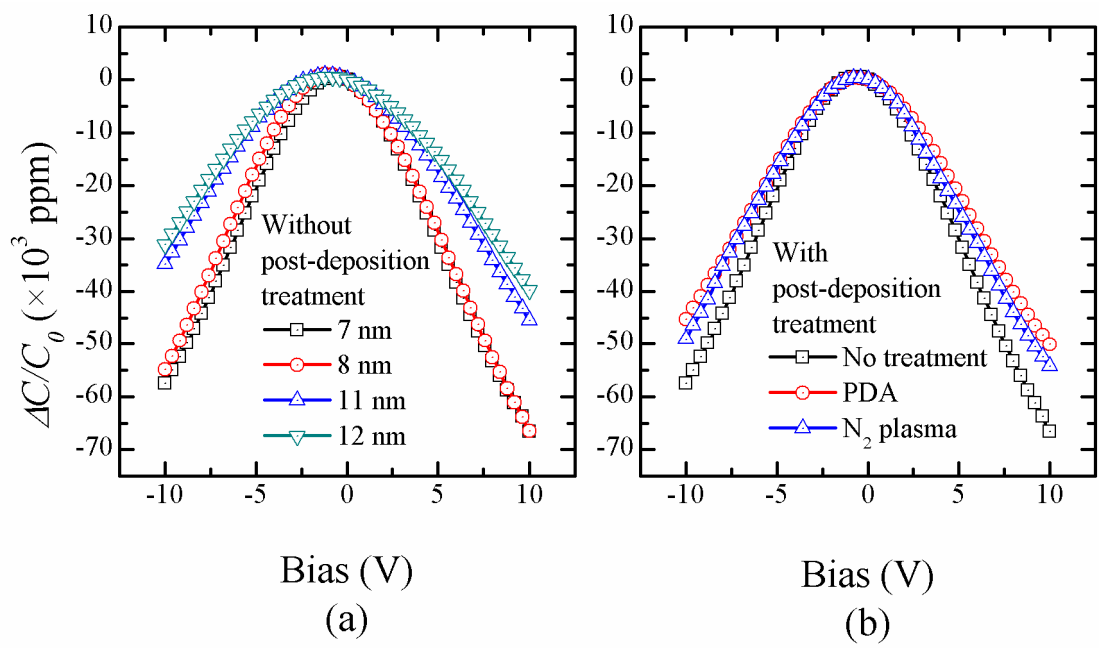

Fig. 3-1: The normalized capacitance density $\Delta C/C_0$ measured at f=100 kHz for (a) samples S1-4 with as deposited PECVD SiO_2 and (b) samples S1, S5 and S9 with 7 nm SiO_2 with varied post-deposition treatment.

$\Delta C/C_0$-V curves shown in Fig. 3-1(b) belong to the sample S1, S5 and S9, which are the MIM capacitors with 7 nm SiO_2 subjected to various post-deposition treatments. The capacitance densities C_0 and corresponding capacitive effective thicknesses (CET) of the samples with different post-deposition treatments are shown in Fig. 3-2 (a) and the extracted quadratic VCC for different C_0 and CET of SiO_2 is shown in Fig. 3-2 (b). The CET is calculated by the formula $d_{CET} = 3.9\varepsilon_0/C_0$ where ε_0 is the permittivity of free space. It is seen that the PDA and N_2 plasma treatment increase the CETs of the MIM capacitors. Comparing to the SiO_2 without any post-deposition treatment, the PDA constantly increases the CET of SiO_2 by ~0.5 nm. The O_2 flow during the PDA could have reacted with the bottom TaN and formed a thin oxide layer at the interface. On the other hand, the N_2 plasma treatment changes the CET by an amount proportional to the thickness of the as-deposited SiO_2, suggesting that the dielectric constant of SiO_2 was reduced. This reduction in the dielectric constant could

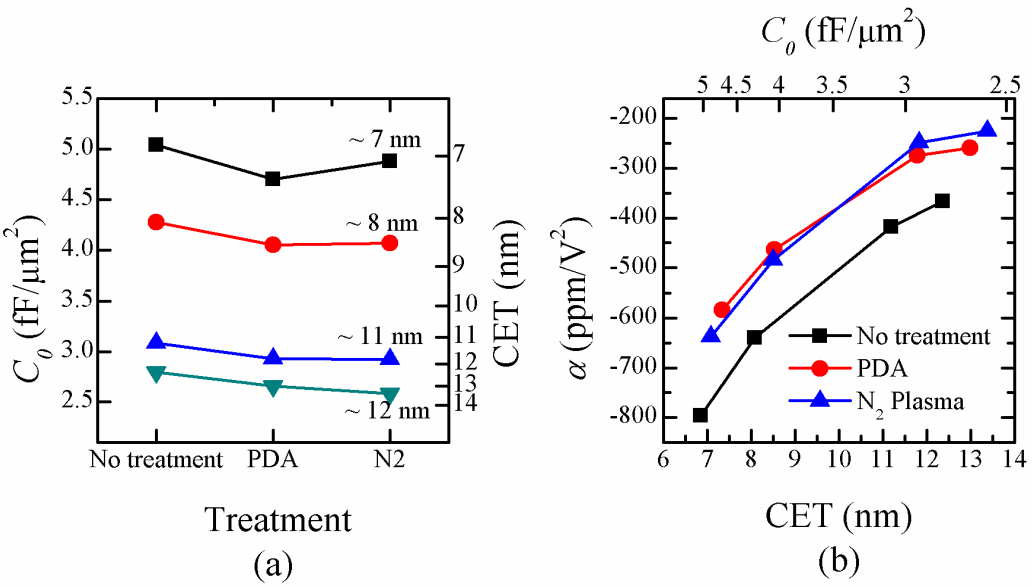

Fig. 3-2: (a) The capacitance density C_0 and EOT of MIM capacitors for different post-depostion treatment and (b) the quadratic VCC (α) versus EOT of the MIM capacitors for different post-deposition treament.

be chamber related. From Fig. 3-2 (b), it is clearly shown that the quadratic VCC of SiO_2 with PDA and N_2 plasma treatment are comparable, and are about 25% smaller than those of the as-deposited SiO_2. The capacitor with ~12 nm SiO_2 subjected to the N_2 plasma treatment demonstrates a capacitance density of 2.6 fF/μm^2 and a low quadratic VCC of -220 ppm/V^2.

To study the field strength of the PECVD SiO_2, the samples were subjected to an applied bias swept from 0 to 20 V, until breakdown occurred. A set of leakage currents at different bias voltage for samples S1, S5 and S9 are shown in Fig. 3-3, in which the corresponding breakdown voltages are 10.6, 13.7 and 11.4 V. The distributions of breakdown voltage for selected SiO_2 samples are shown in Fig. 3-4. The breakdown voltages and electric field strength against different CETs for SiO_2 layers subjected to different post-deposition treatment is shown in Fig. 3-5. The dielectric field strengths of SiO_2 layers without any treatment are 14-16.5 MV/cm, which are consistent with the reported field strength of 15-16 MV/cm for SiO_2 layer

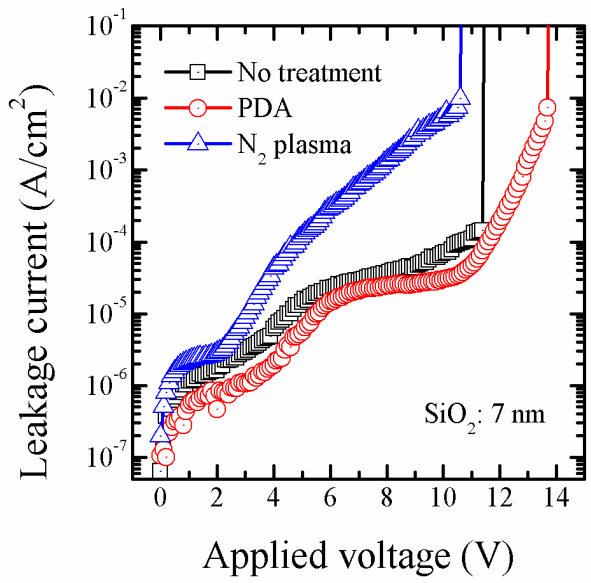

Fig. 3-3: Leakage current at different applied bias for samples S1, S5 and S9 in a breakdown stress test.

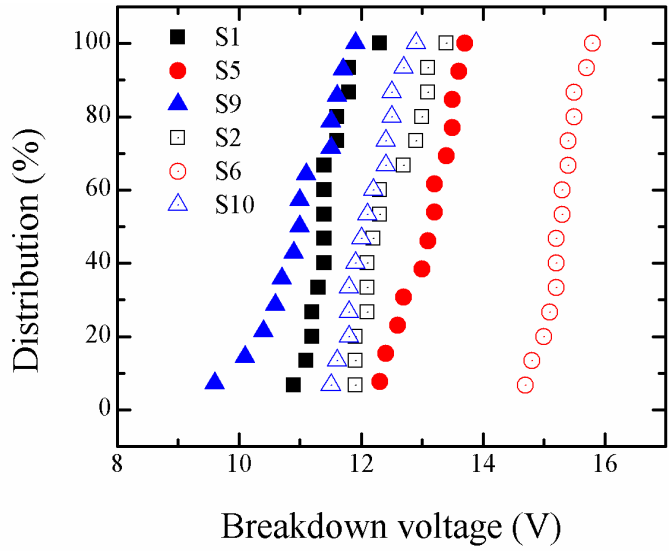

Fig. 3-4: Breakdown voltage distributions of selected MIM capacitors.

with thicknesses from 5-10 nm [16]. From Fig. 3-4 and Fig. 3-5, it is seen that the breakdown voltages of SiO_2 layers subjected to the PDA are about 15-20% and 20-25% higher than those of SiO_2 without any treatment and with N_2 plasma treatment, respectively. This could be due to two possible reasons: (1) the physical thickness of the dielectric is slightly thicker (by 0.5 nm) and (2) the dangling bonds in the SiO_2

layers are passivated by O_2 during the 400 °C anneal. The SiO_2 layers subjected to the N_2 plasma have lower breakdown voltages than those of SiO_2 without any treatment. As previously discussed, the introduction of N_2 into the SiO_2 film changes the structure of SiO_2, which possibly reduced the field strength of the dielectric.

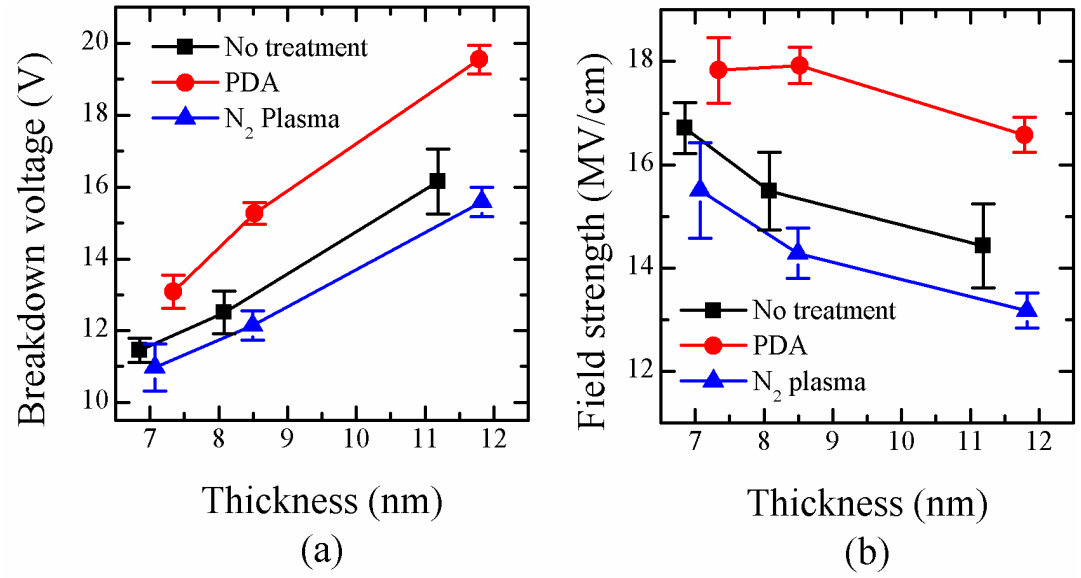

Fig. 3-5: (a) Breakdown voltage and (b) dielectric field strength versus CET of the MIM capacitors subjected to different post-deposition treatments.

3.3. MIM capacitors with ALD SiO_2

3.3.1 Experiment

The fabrication steps of the ALD SiO_2 MIM capacitors were similar to those of PECVD SiO_2 MIM capacitors. After the bottom TaN electrode was sputtered, SiO_2 layers with thickness 3-6 nm were deposited by ALD at 200 °C and 400 °C. Selected samples were annealed in at 400 °C for 2 minutes with traces of O_2, as listed in Table 3-2. The thicknesses of the samples in Table 3-2 are the specified thicknesses to an external organization that performed the ALD of SiO_2, and may not be same as the

actual thicknesses. The top TaN electrode was then deposited, followed by photolithography and dry etching to form the top electrode. The photoresist was removed by ashing, followed by a dilute HF dip to remove the ALD SiO_2 on the bottom electrode. This completed the fabrication of the MIM capacitors.

Table 3-2: The sample split for the experiment on MIM capacitors with ALD SiO_2.

Label	Specified thickness	ALD Temperature	PDA
H3	3 nm	400 °C	400 °C for 2 mins
H4	4 nm		
H6	6 nm		
L3	3 nm	200 °C	
L4	4 nm		
L6	6 nm		
H4-N	4 nm	400 °C	None
L4-N	4 nm	200 °C	

3.3.2 **Results and discussion**

The capacitance of the MIM capacitors was measured at different frequencies ranging from 1 kHz to 100 kHz with a bias swept from -4 to 4 V. The capacitance voltage characteristics of selected MIM capacitors measured at 100 kHz are shown in Fig. 3-6 (a). The normalized $\Delta C / C_0 = (C - C_0) / C_0$ curves shown in Fig. 3-6 (b) indicate that the quadratic VCC of the MIM capacitors with ALD SiO_2 are negative, and they vary with SiO_2 thickness, deposition temperature and the anneal condition.

The frequency-dependent capacitance density (C_0), quadratic VCC (α) and linear VCC (β) are shown in Fig. 3-7 (a), (b), and (c), respectively. Values of α and β

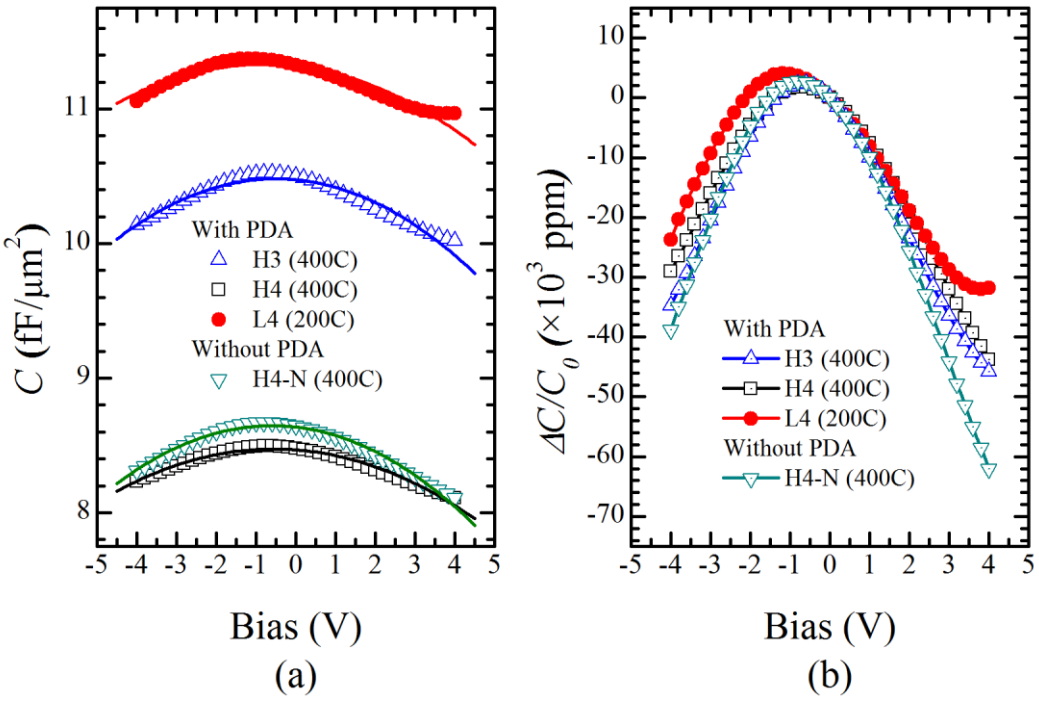

Fig. 3-6: (a) Capacitance versus applied bias and (b) the extracted normalized capacitance density versus applied bias for selected MIM capacitors with ALD SiO_2.

were extracted by fitting the equation $\Delta C / C_0 = (C - C_0) / C_0 = \beta V + \alpha V^2$ to the measured data. The quadratic VCC against capacitance density for SiO_2 having different deposition temperatures and PDA conditions are shown in Fig. 3-7 (d). The capacitance densities of ALD SiO_2 MIM capacitors are found to be relatively constant over the 1 – 100 kHz frequency range [Fig. 3-7 (a)]. The CETs of the samples are extracted using the capacitance densities at 100 kHz, and listed in the legends of Fig. 3-7. While the CETs of ALD SiO_2 (400 C) are close to the specified thicknesses, the CETs of ALD SiO_2 (200 C) are smaller than the specified thicknesses by about 25%. The PDA slightly reduces the capacitance density and increases the CET, due to the introduction O_2 into the dielectric and a possible formation of a thin high-k Ta-based oxide at the bottom TaN-SiO_2 interface. The magnitudes of α and β are higher for a thinner SiO_2. While the magnitude of α of ALD SiO_2 (400C) changes slightly with frequency, the α values of ALD SiO_2 (200C) reduces by 25% over the frequency

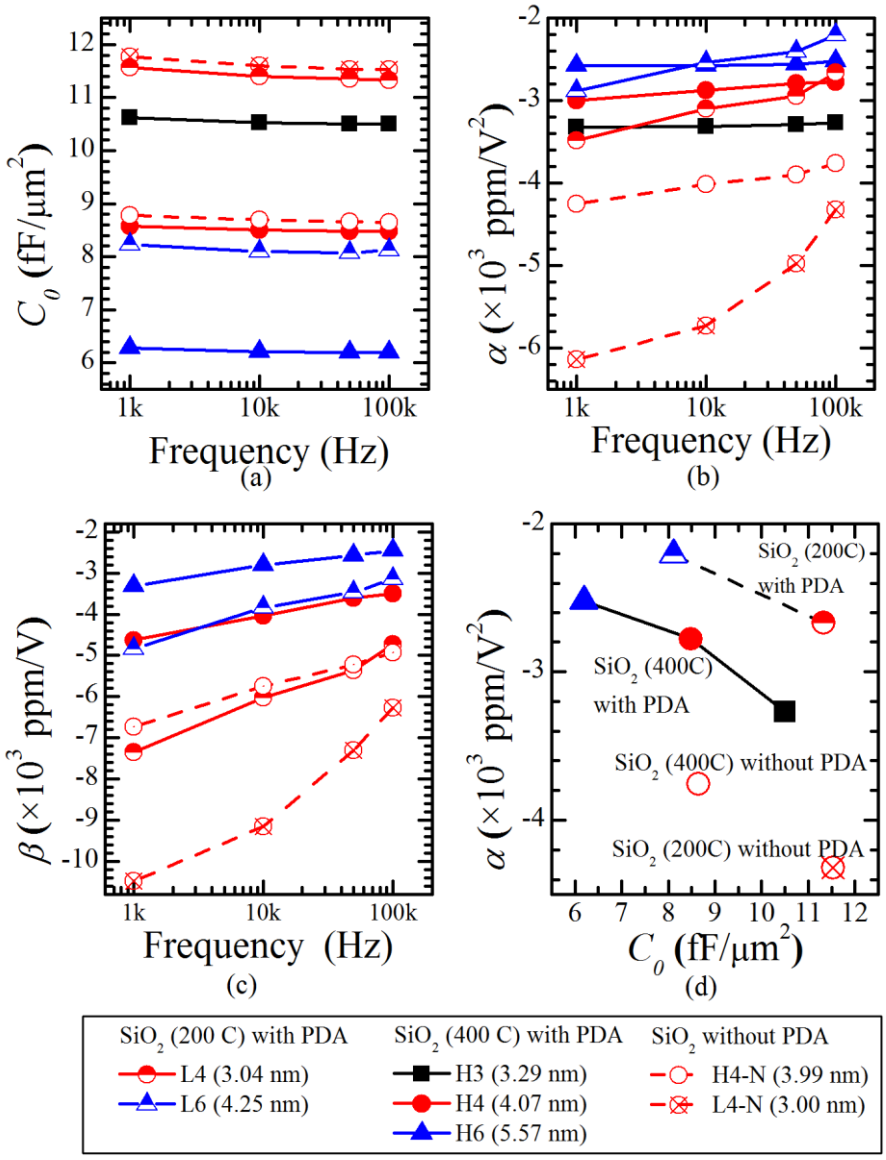

Fig. 3-7: Frequency dependent (a) capacitance density C_0 at 0 V bias, (b) quadratic and (c) linear VCC for the MIM capacitors with ALD SiO_2. (d) The quadratic VCC (α) for different capacitance density C_0 measured at frequency f = 100 kHz. The thicknesses indicated in the legends are the CETs of the samples, using the capacitance densities measured at 100 kHz.

range. The PDA reduces the magnitudes of α and β significantly, by up to 1.8 and 1.5 times, respectively. From Fig. 3-7 (d), it is observed that the magnitudes of the quadratic VCCs (α) increase with capacitance density. This trend is commonly observed in other dielectrics, such as Al_2O_3 [17], Sm_2O_3 [6], TiZrO [18] and HfLaO [19]. With the PDA applied, the quadratic VCCs of SiO_2 (200C) are smaller than those of SiO_2 (400 C) for the same C_0.

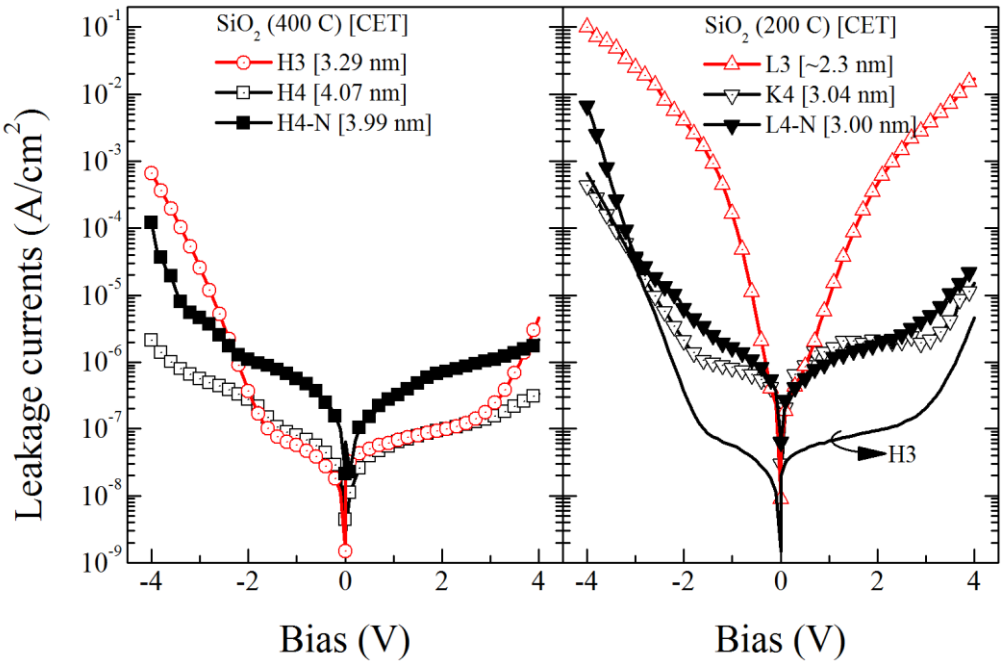

Fig. 3-8: Leakage currents of MIM capacitors with ALD SiO_2 with bias swept from -4V to 4V.

The leakage currents of the MIM capacitors with applied bias swept from -4 to 4 V for 3 and 4 nm ALD SiO_2 are shown in Fig. 3-8. The leakage currents at negative bias are generally higher than those at positive bias, suggesting that injection of electrons from the top electrode is higher than from the bottom electrode. The MIM capacitor L3 with 3 nm (specified) SiO_2 (200C) has a very high leakage current, which appears to be mainly caused by direct tunneling [20]. The CETs of ALD SiO_2 (200C) are consistently 0.76 times the CETs of ALD SiO_2 (400C) for the same specified thicknesses, and thus the CET of H3 is expected to be ~2.3 nm. A lower leakage current was achieved when a PDA with traces of O_2 is applied, as this could have passivated some of the dangling bonds in SiO_2. Samples H3 and H4 have similar leakage currents at low bias, which start to deviate at bias 2-2.5 V. The leakage currents for the 3 and 4 nm thick SiO_2 (400 C) measured at 3.3 V are about 4×10^{-7} and

2×10^{-7} A/cm^2, respectively. These are as low as the leakage currents through stacked Sm_2O_3 (7 nm) on PECVD SiO_2 (4 nm) reported in ref. [5-6]. Samples L4, L4-N and H3 have similar CETs, but the leakage currents of H3 are considerably lower than those of L4 and L4-N.

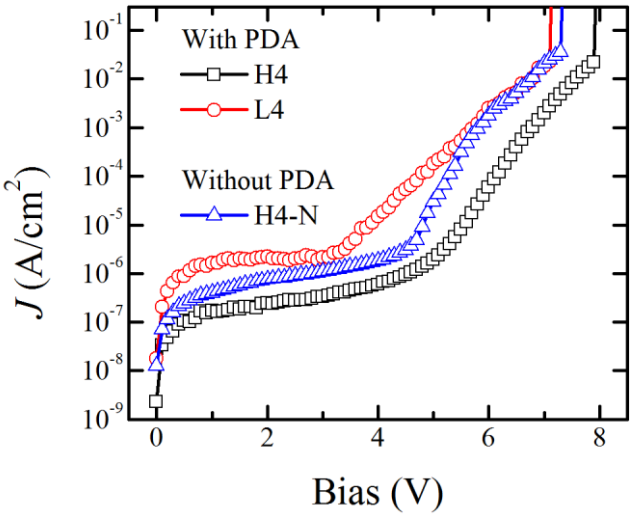

Fig. 3-9: The leakage currents through selected ALD SiO_2 layers in a breakdown stress test.

In a breakdown stress test, the applied bias was swept from 0 to 15 V until breakdown occurred. The leakage currents through the SiO_2 layers for 4 nm (specified) ALD SiO_2 are shown in Fig. 3-9. The ALD SiO_2 dielectric breaks down when the leakage current density exceeds about 10^{-2} A/cm^2, as seen in Fig. 3-9. From the leakage current (J) versus bias (Vg) plots, the terms are rearranged to study the conduction mechanism through the SiO_2 layers. Some of the conduction mechanisms through the dielectric are: volume conduction due to Ohm's law (Ohmic conduction), space charge limited (SCL) conduction, Schottky emission (SE), Poole-Frenkel (PF) emission, direct tunneling and Fowler-Nordheim (FN) tunneling. At low bias when the carrier injection into the dielectric is low, the conduction of free carriers in the dielectric follows Ohm's law ($J \sim V_G$) [21]. The SCL conduction [22-25] consists of

three mechanisms: trap-limited, trap-filled limited and trap-free limited. In all the 3 cases, the current and voltage has a power law relationship $J \sim V_G^m$ where $m = 2$ for trap-limited and trap-free limited SCL (this is also known as the Mott-Gurney law) and $m > 2$ for trap-filled limited SCL. The value of m can be obtained from the linear slope of ln(J) versus ln(V_G).

The Schottky emission is a field-assisted thermionic emission, and the current density is expressed as [26]:

$$J = A^* T^2 \exp\left[\frac{-q(\Phi_B - \sqrt{qE/4\pi\varepsilon_0\varepsilon_r})}{kT}\right] \tag{3-1}$$

where

$$A^* = \left(\frac{4\pi q m^* k^2}{h^3}\right). \tag{3-2}$$

A^*, Φ_B, ε_r, k, h and m^* are the effective Richardson constant, Schottky barrier height, dielectric constant, Boltzmann constant, Planck's constant and the effective electron mass, respectively. The dielectric constant ε_r and the Schottky barrier height Φ_B can be obtained from the linear slope and the y-intercept of the plot ln(J) versus $E^{1/2}$.

The Poole-Frenkel (PF) emission is a de-trapping of carriers from the bulk oxide into the conduction band. The current density is expressed as [26-27]:

$$J \sim E \exp\left[\frac{-q(\Phi_t - \sqrt{qE/\pi\varepsilon_0\varepsilon_r})}{kT}\right] \tag{3-3}$$

where Φ_t is the trap energy level of the oxide. The dielectric constant ε_r can be obtained from the linear slope of ln(J/E) versus $E^{1/2}$.

The FN and direct tunneling refer to the tunneling of electrons into a conduction band through the triangle and trapezoidal barrier, respectively. While the

current density for direct tunneling is not easily derived, the current density for FN tunneling can be expressed as [28-29]:

$$J = AE^2 \exp(-B/E) \tag{3-4}$$

where

$$A = q^3 m_e / (8\pi h m^* \Phi_B) \tag{3-5}$$

and

$$B = 4(2m^*)^{1/2} \Phi_B^{3/2} / (3qh/2\pi). \tag{3-6}$$

m_e and Φ_B are the electron mass in free space and the barrier height between the oxide and the gate. For the FN tunneling, the barrier height Φ_B can be extracted from the slope of the straight line from the $\ln(J/E^2)$ versus 1/E plot.

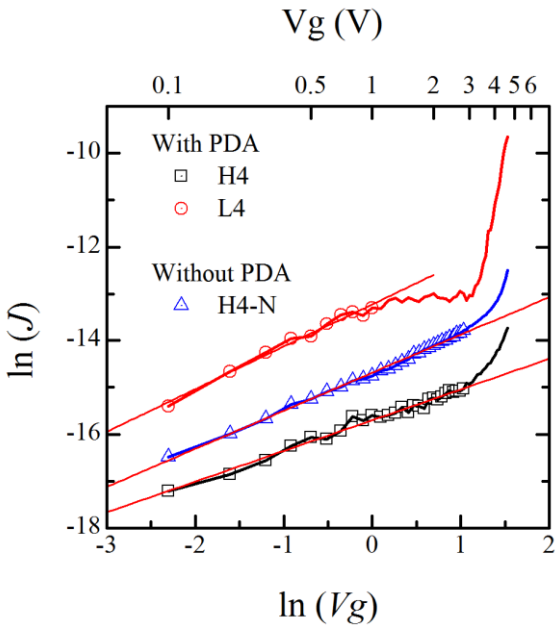

Fig. 3-10: $\ln(J)$ versus $\ln(Vg)$ for 4 nm SiO_2, showing that the conduction mechanism through the SiO_2 at low bias is space charge limited (SCL), following Ohm's Law.

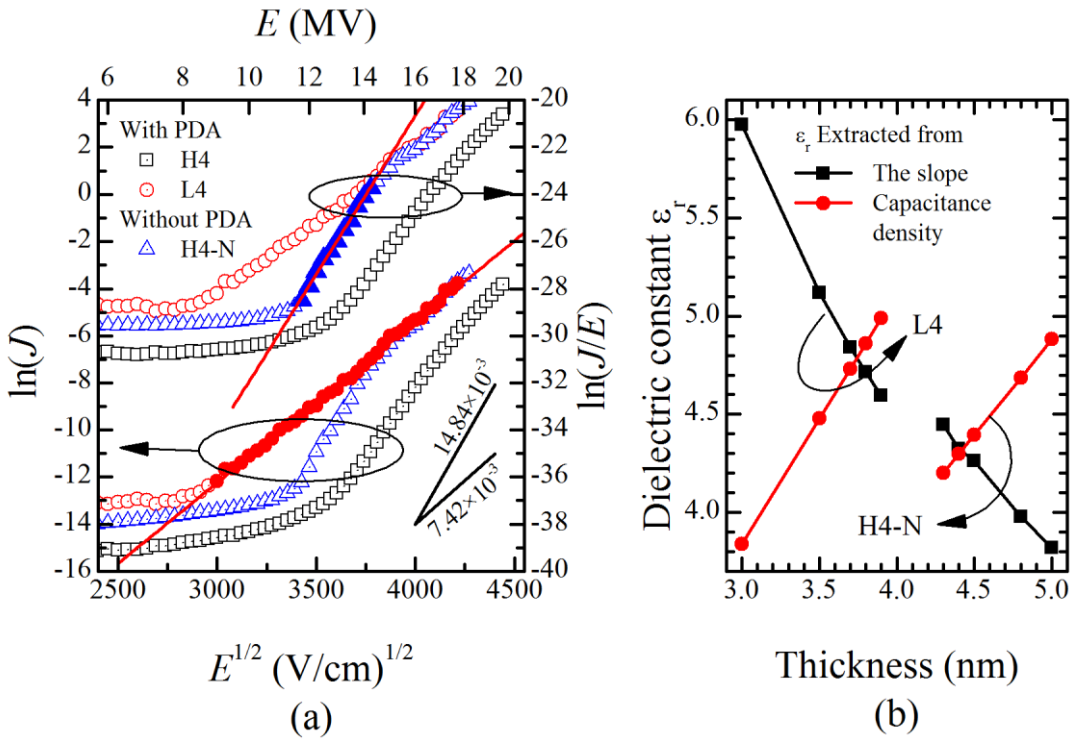

Fig. 3-11: (a) ln(J) and ln(J/E) versus $E^{1/2}$ for 4nm SiO_2 for the Schottky and PF emission. When the dielectric constant is 3.9, the slopes of ln(J) and ln(J/E) versus $E^{1/2}$ corresponding to Schottky and PF emission are 7.42×10^{-3} and 14.84×10^{-3} $(cm/V)^{1/2}$, respectively. (b) Dielectric constant for different physical oxide thickness derived from the capacitance density [8.64 and 11.3 fF/μm^2 for SiO_2 (400C) and (200C), respectively] and from the fitted slopes from (a).

The current densities in Fig. 3-9 were rearranged into ln(J) versus ln(Vg) (Fig. 3-10), ln(J) and ln(J/E) versus $E^{1/2}$ (Fig. 3-11) and ln(J/E^2) versus 1/E (Fig. 3-12) to determine the leakage mechanisms for different electric fields. The plots ln(J) versus ln(Vg) in Fig. 3-10 can be fitted with straight lines with slopes of 0.65-0.91 when the gate bias is less than 3 V for H4 and H4-N [SiO_2 (400C)] and 1 V for L4 [SiO_2 (200C)], suggesting that volume conductivity due to Ohm's law appears at this bias range. Moreover, direct tunneling which is difficult to be characterized is also expected at this low bias for SiO_2 [30].

From the ln(J) versus $E^{1/2}$ plots in Fig. 3-11, it is seen that Schottky emission is dominant when the E-field is ~9-17.7 MV/cm for L4. The extracted Schottky barrier heights are ~1.4 eV using an effective electron mass $m^*=0.5m_e$ [29, 31-33].

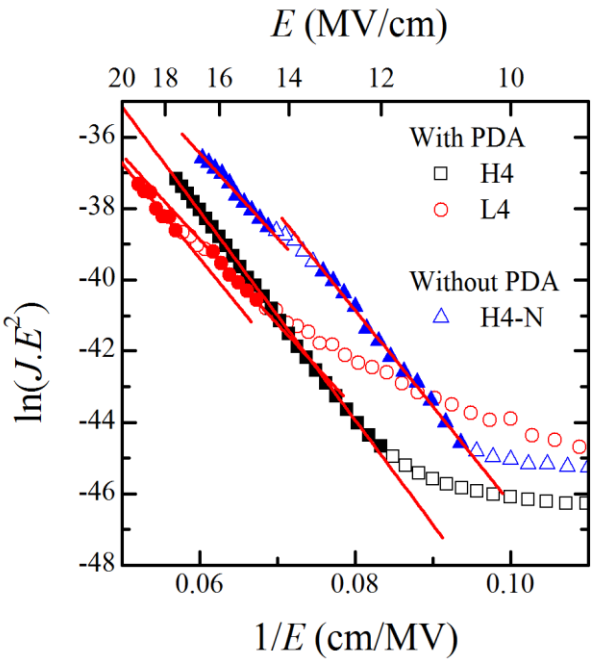

Fig. 3-12: $\ln(J/E^2)$ versus $1/E$ for 4 nm SiO_2 to determine the region corresponding to the FN tunneling.

Similarly, from the $\ln(J/E)$ versus $E^{1/2}$ plots, PF emission can be observed when the E-field is ~11.8-14 MV/cm for H4-N. Using the equation (3-1) and (3-3), the slopes of the straight lines giving a dielectric constant of 3.9 corresponding to Schottky and PF emission are 7.42×10^{-3} and 14.84×10^{-3} $(cm/V)^{1/2}$, respectively. The electric field E is expressed as $E=Vg/t_{ox}$ where t_{ox} is the physical thickness of the oxide, assumed to be 4 nm in the plot in Fig. 3-11 (a). The dielectric constant ε_r of SiO_2 can be extracted from the slopes of $\ln(J)$ and $\ln(J/E)$ versus $E^{1/2}$ plots in Fig. 3-11 (a) and the capacitance density C_0: $\varepsilon_r=C_0t_{ox}/\varepsilon_0$. The dielectric constants (ε_r) of L4 and H4-N for different physical oxide thicknesses calculated by these two methods are shown in Fig. 3-11 (b). As seen, the two extraction methods give the same physical thickness and dielectric constants when the physical thicknesses of SiO_2 in L4 and H4-N are ~3.7 and ~4.4 nm, respectively, with corresponding dielectric constants of ~4.8 and ~4.2. The two thicknesses are close to the specified 4 nm thickness.

The $\ln(J/E^2)$ versus $1/E$ for 4 nm SiO_2 plots are shown in Fig. 3-12. To calculate the electric field, the physical thicknesses of H4 and H4-N are assumed to be 4.4 nm, and of L4 is 3.7 nm. It is seen that the FN tunneling is the conduction mechanism for high electric field in SiO_2. The extracted barrier heights Φ_B are ~3.4 and 3.1 for H4 and H4-N [SiO_2 (400C)], respectively and ~2.8 eV for L4 [SiO_2 (200C)]. These barrier heights are consistent with the reported barrier heights between SiO_2 and TaN (~ 3.4-3.6 eV) [34].

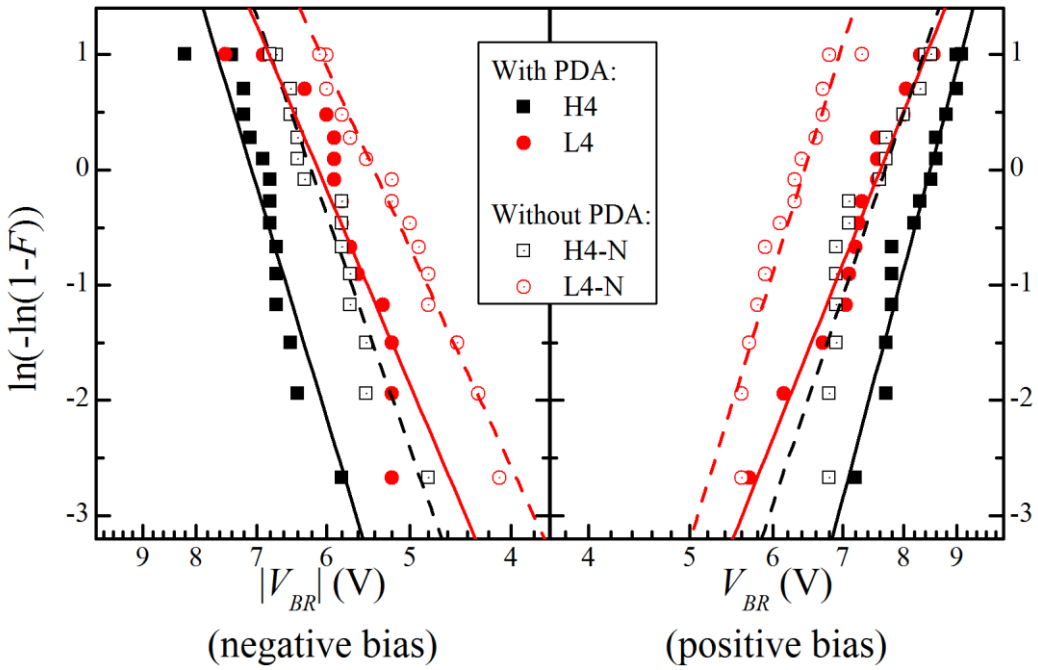

Fig. 3-13: Weibull distribution of breakdown voltage for MIM capacitors with 4 nm ALD SiO_2 with positive and negative bias.

The breakdown voltage distributions of capacitors H4, L4, H4-N and L4-N with negative and positive bias are shown in Fig. 3-13. The breakdown voltage distributions are converted into Weibull distribution:

$$\ln(-\ln(1-F)) = m \times \ln(V_0) + c \tag{3-7}$$

where F, m, and V_0 are the cumulative distribution, the Weibull shape parameter and the characteristic breakdown voltage at 63.2 % failure, respectively. It is seen that the dielectrics breakdown at a lower voltage when negative bias was applied, as compared to positive bias. This trend is consistent with higher leakage current for negative bias shown in Fig. 3-8. It is also observed from Fig. 3-13 that the PDA improves the field strength of the ALD SiO_2. The values of m, V_0 and dielectric field strength are listed in Table 3-3. The thicknesses used for SiO_2 (200C) and (400C) are 3.7 and 4.4 nm, respectively. The dielectric field strengths for SiO_2 with PDA are about 2 MV/cm stronger than those of SiO_2 without PDA. With PDA, the field strength of ~ 19-20 MV/cm was achieved.

Table 3-3: The characteristic breakdown voltage V_0 and Weibull slope parameters for MIM capacitors with 4 nm ALD SiO_2.

		Positive bias			Negative bias		
		m	V_0 (V)	E (MV/cm)	m	Vo (V)	E (MV/cm)
PDA	H4 (400C)	14.8	8.5	19.3	13	-7.1	-16.1
	L4 (200C)	9.8	7.6	20.5	9.2	-6.1	-16.5
Without PDA	H4-N (400C)	11.8	7.7	17.5	11.1	-6.2	-14.1
	L4-N (200C)	12.8	6.4	17.3	8.5	-5.4	-14.6

The capacitor H4 [4 nm SiO_2 (400C) with PDA] was stressed with constant voltages of 6.7, 7.0, and 7.3 V in a time dependent dielectric breakdown study. The stress time probability distributions for H4 are shown in Fig. 3-14. From the distributions, the time-to-breakdown TBD at 63.2% failure was obtained and plotted

against the stress electric field to extrapolate the voltage for 10-year operation (inset of Fig. 3-14). The operation voltage to achieve 10-year lifetime is extrapolated to be 3.6 V for the 4 nm thick ALD SiO_2 (400C).

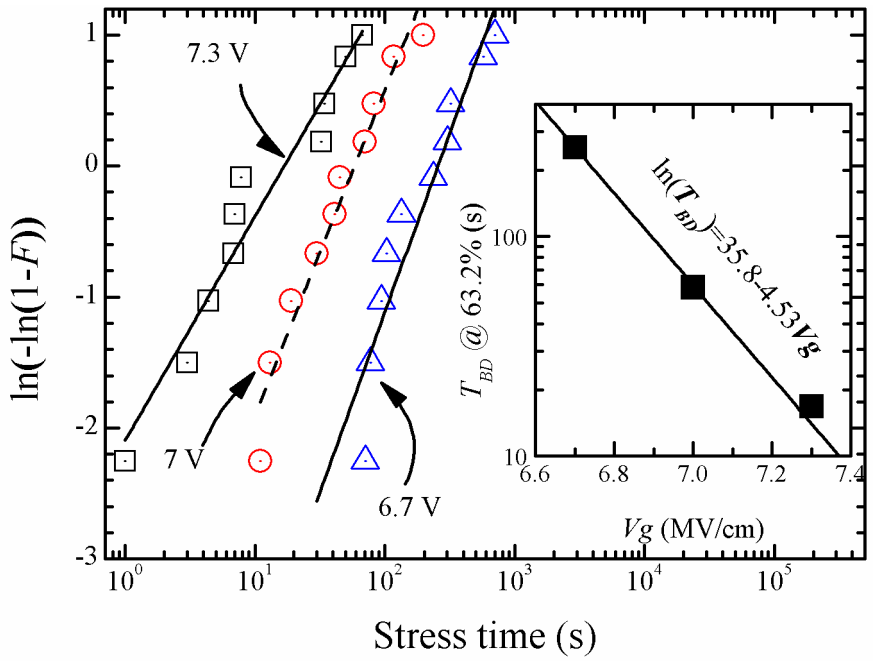

Fig. 3-14: Weibull distribution of time-to-breakdown obtained using constant voltage stress. The inset plots the time-to-breakdown at 63.2% for different stress electric field for the MIM capacitor with 4 nm ALD SiO_2 (400C).

3.3.3 **Performance comparison of ALD and PECVD SiO_2**

The performance of 7 nm PECVD SiO_2 is compared to that of 4 nm ALD SiO_2 (400C) in Fig. 3-15: the leakage currents for different bias is plotted in (a) and the breakdown voltage in (b). The PDA was applied to both layers. Despite having a thicker dielectric, the PECVD SiO_2 layer has a leakage current of about 10 times higher than that of ALD SiO_2 (400C). The dielectric field strength of ALD SiO_2 (400C) is also about 2 MV/cm higher that of PECVD SiO_2. The low leakage current and high dielectric field strength for ALD SiO_2 (400C) is due to low level of traps inside the oxide layer.

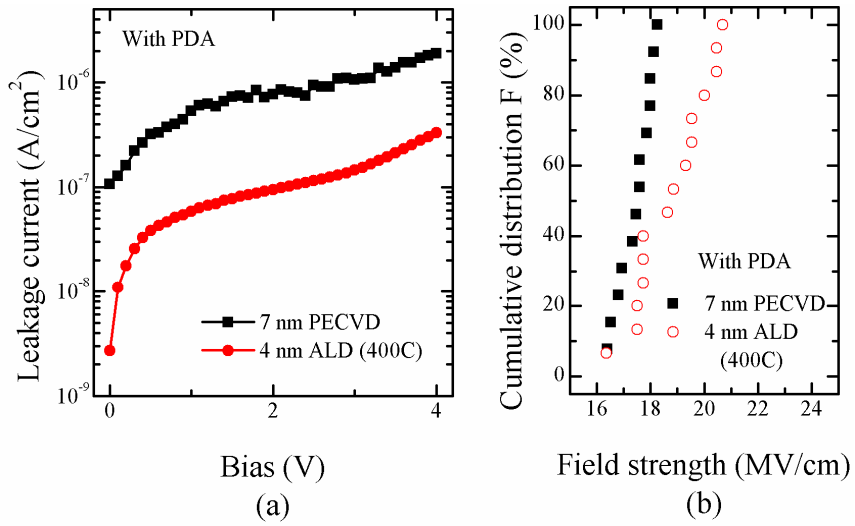

Fig. 3-15: Comparison of (a) leakage currents for different applied bias and (b) breakdown voltage distribution of 7 nm PECVD SiO_2 and 4 nm ALD SiO_2 (400C). PDA was applied to both SiO_2 layers.

3.4. **Modeling of the negative quadratic VCC of SiO_2**

Two models were proposed to explain the positive quadratic VCC of the high-k dielectrics: the ionic polarization [14] and electrostriction models [15]. The ionic polarization model suggests that the metal cation in the dielectric is displaced from its equilibrium position due to the electric field, and that generates a field dependent ionic susceptibility [14]. The electrostriction model states that the induced strain in the dielectric under an electric field causes the deformation of the dielectric and thus the capacitance varies [15]. These 2 models however cannot explain the negative quadratic VCC of SiO_2. Using the model in [14] and the total free energy of the SiO_2 molecule described by McPherson [35], the ionic susceptibility of SiO_2 is derived as:

$$\chi_i \approx 0.155 + A_i E^2, \tag{3-8}$$

where $A_i \approx 7.7\times10^{-21}$ m^2/V^2 and E is the applied electric field. The electrostriction coefficient of SiO_2 is $-0.18\pm0.07\times10^{-21}$ m^2/V^2 [36]. The magnitude of the capacitance

variation due to the ionic polarization and electrostriction effect are 30 and 200 times smaller than the experimental values in this work, respectively and thus can be ignored. Moreover, Eq. (3-8) over-estimates χ_i because it assumes that the axis of the SiO_2 molecule is either parallel or anti-parallel to the electric field.

Blonkowski [37] made the first attempt to explain the negative quadratic VCC (α) of SiO_2 which he attributed to the spatial variation in electronic charge: α is negative when the derivative $\delta = R\partial q/q\partial R$ is sufficiently negative (-250) where q and R are the ionic charge and first neighbour distance, respectively. However, from the derivation of δ by Blonkowski *et al.* [38], it is difficult for δ to reach that negative value. In this work, the quadratic VCC of SiO_2 is modeled based on the orientation polarization in SiO_2. It is shown that the capacitance densities of the SiO_2 MIM capacitors fitted very well to a derived function.

The C-V curves of the MIM capacitor with SiO_2 thicknesses from 3-13 nm presented in section 2 and 3 were used for the modeling of the negative quadratic VCC. The SiO_2 layers with 3 and 4 nm thickness were deposited by atomic layer deposition (ALD) at 400 °C and those with thicknesses from 7-13 nm were deposited by PECVD. A post-deposition anneal (PDA) at 400 °C for 2 mins was performed on selected samples.

The quadratic VCCs of the SiO_2 capacitors are negative and their magnitudes $|\alpha|$ are plotted against the corresponding SiO_2 thicknesses (d) in Fig. 3-16. From the fitted straight lines, it is found that $\alpha = A/d^2$ where A $\approx$ -3.74×10^{-20} and -5.40×10^{-20} m^2/V^2 for SiO_2 with and without PDA, respectively. When the maxima of the $\Delta C/C_0$ (= $\beta dE+\alpha d^2E^2$) versus E curves were shifted toward E = 0 to eliminate the effect of the linear VCC (β), the curves for SiO_2 with and without PDA converge into 2 curves

(inset of Fig. 3-16), further confirming that $A = \alpha d^2$ is a constant and a material property.

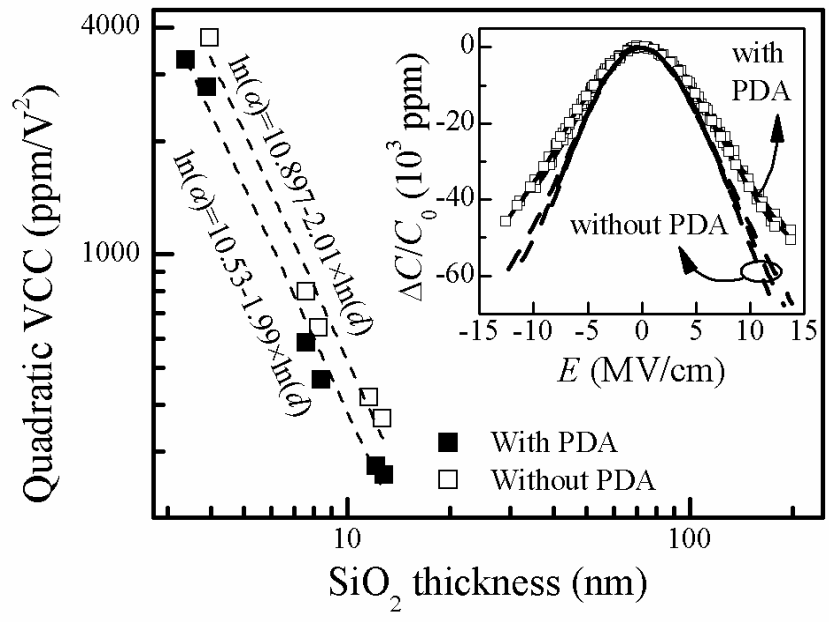

Fig. 3-16: Magnitude of quadratic VCCs $|\alpha|$ for different thicknesses of SiO_2 with and without PDA. Inset: normalized capacitance density ($\Delta C/C_0$) versus electric field E. The maxima of the normalized capacitance density curves were shifted toward zero E-field to isolate the effect of the linear VCC.

The total polarization in SiO_2 can be expressed as $P = P_i + P_e + P_o$ where P_i, P_e, and P_o are the ionic, electronic, and orientation polarization, respectively. Moreover, $P_{i,e} = \varepsilon_0 \chi_{i,e} E$ where χ_i and χ_e (= n^2) are the ionic and electronic susceptibility, respectively, n (= 1.5) is the refractive index of SiO_2 and ε_0 is the permittivity of free space. Since the Kerr coefficient n_2 of SiO_2 is 1.22×10^{-22} m^2/V^2 (1.1×10^{-13} in esu unit) [39] and the variation of χ_i with electric field is insignificant [Eq. (3-8)], χ_i and χ_e are assumed to be independent of the electric field. To calculate the orientation polarization in SiO_2, it is assumed that SiO_2 has N active dipoles in a

unit volume, each with dipole moment μ_0. The moment along the electric field due to the dipole μ_0 is:

$$\mu = \mu_o \cos\theta \tag{3-9}$$

where θ is the angle between the dipole μ_0 and the local electric field E_{loc}. The energy of moment along the electric field due to dipole μ_0 is given as:

$$W = -\mu_o E_{loc} \cos\theta \tag{3-10}$$

By Boltzmann statistics, the average value of $<\cos\theta>$ is expressed as:

$$<\cos\theta> = \frac{\int_0^{\pi} \cos\theta e^{\frac{\mu_0 E_{loc}\cos\theta}{kT}} \frac{1}{2}\sin\theta d\theta}{\int_0^{\pi} e^{\frac{\mu_0 E_{loc}\cos\theta}{kT}} \frac{1}{2}\sin\theta d\theta} = \frac{1}{a}\frac{\int_{-a}^{a} e^x x dx}{\int_{-a}^{a} e^x dx} = \tag{3-11}$$

$$= \frac{1}{a}\frac{[xe^x - e^x]_{-a}^{+a}}{[e^x]_{-a}^{+a}} = \frac{e^a + e^{-a}}{e^a - e^{-a}} - \frac{1}{a} = \coth a - \frac{1}{a} = L(a),$$

where $x = \frac{\mu_0 E_{loc}\cos\theta}{kT}$ and $a = \frac{\mu_0 E_{loc}}{kT}$.

$L(a)$ is called Langevin function [40]. The local electric field E_{loc} is related to the applied field E by a relation $E_{loc} = \lambda E$ where λ is the local field correction factor. Using the Lorentz's approach, $\lambda = (2+\varepsilon_r)/3 \cong 1.97$, while the Onsager's approach yields $\lambda = 3\varepsilon_r/(2\varepsilon_r+1) \cong 1.33$ [41], where ε_r (~ 3.9) is the dielectric constant of SiO_2. As such, $a = \lambda\mu_0 E/kT$ and when one let $\mu_b = \lambda\mu_0$ and $N_b = N/\lambda$, the total polarization along the electric field is:

$$P = \left[\varepsilon_0(\chi_i + \chi_e) + (\frac{N_b \mu_b^2}{kT})\frac{L(a)}{a} \right] E . \tag{3-12}$$

As such, the permittivity of SiO_2 is:

$$\varepsilon(E) = \varepsilon_0 + \varepsilon_0(\chi_i + \chi_e) + (\frac{N_b \mu_b^2}{kT})\frac{L(a)}{a} \tag{3-13}$$

where ε_0 is the permittivity of free air. When E=0, $L(a)/a=1/3$, and thus the static permittivity $\varepsilon(0)$ is:

$$\varepsilon(0) = \varepsilon_0 + \varepsilon_0(\chi_i + \chi_e) + \frac{N_b \mu_b^2}{3kT} \tag{3-14}$$

The permittivity $\varepsilon(E)$ is then reduced to:

$$\varepsilon(E) = \varepsilon(0) + \frac{N_b \mu_b^2}{kT}\left[\frac{L(a)}{a} - \frac{1}{3}\right] \tag{3-15}$$

and thus

$$\frac{\Delta C}{C_0} = \frac{\Delta\varepsilon(E)}{\varepsilon(0)} = \frac{\varepsilon(E) - \varepsilon(0)}{\varepsilon(0)} = \frac{N_b \mu_b^2}{\varepsilon(0) \cdot kT}\left[\frac{L(a)}{a} - \frac{1}{3}\right]. \tag{3-16}$$

where $a = \mu_b E/kT = \mu_b V C_0/\varepsilon(0)kT$.

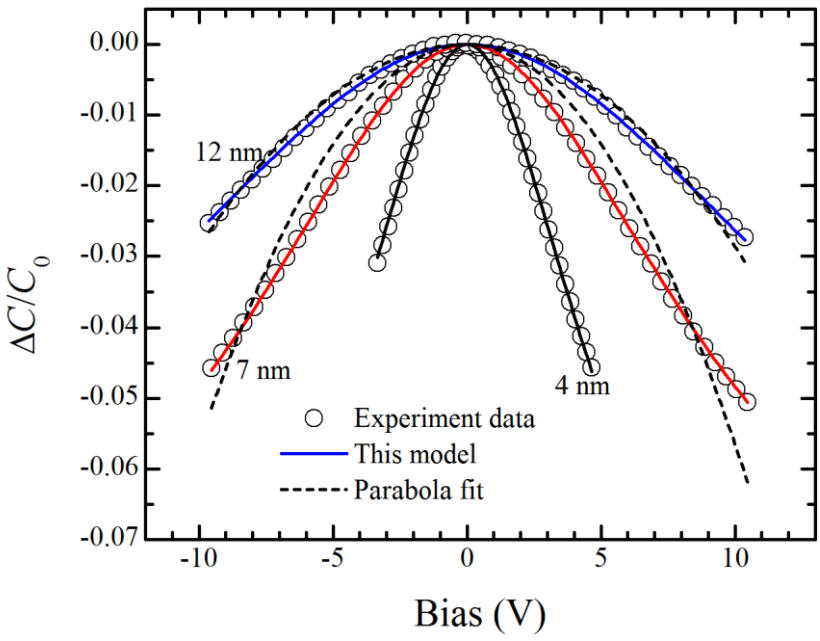

Fig. 3-17: The normalized capacitance density of SiO_2 MIM capacitors are fitted into the Eq. (3-16) and parabola fit. The Eq. (3-16) matches the experimental data (solid lines) very well and much better than the parabola fit (dotted lines).

The $\Delta C/C_0$ versus V plots of the SiO_2 MIM capacitors with their maxima shifted to V = 0 were fitted with Eq. (3-16) using the non-linear regression method. The fittings for 4, 7 and 12 nm SiO_2 with PDA are shown in Fig. 3-17. The Eq. (3-16) matches the experimental curves very well and much better than the parabola fit. The static permittivity $\varepsilon(0)$ was assumed to be $3.9\varepsilon_0$. The values of N_b and μ_b for SiO_2 with PDA obtained from the non-linear regression fitting are listed in Table 3-4. The values of μ_b (= $\lambda\mu_0$) are fairly constant, with an average of 1.065×10^{-29} Cm.

Table 3-4: Values of N_b and μ_b for different SiO_2 thicknesses d obtained from the regression fitting with the dielectric constant of SiO_2 set as 3.9.

d (nm)	3.3	4.1	7.3	8.5	11.8	13
μ_b (10^{-29} Cm)	1.118	1.091	0.995	1.074	1.046	1.068
N_b (10^{20} cm^{-3})	3.964	4.959	5.776	4.989	4.816	5.011

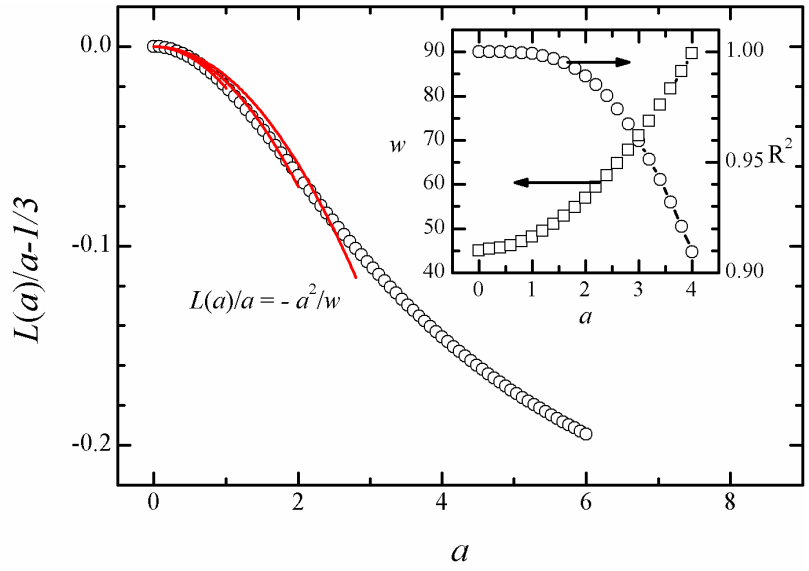

Fig. 3-18: $[L(a)/a\text{-}1/3]$ versus a plot is fitted into the quadratic equation $-a^2/w$. Excellent fit was obtained with small a, but the fitting degrades as a increases. The values of w and the coefficients of determination R^2 for different a are plotted in the inset.

The function $[L(a)/a–1/3]$ can be approximated by a parabolic function $–a^2/w$ for small a where w = 45 for a $\ll$ 1 as shown in Fig. 3-18. As a increases, the estimation is worsened, evidenced by the decreasing coefficient of determination R^2. With V = ±10 V, a = 3.4 and 2.1 for 7 and 12 nm SiO_2, respectively which explains why there are some discrepancies with the parabola fitting and why the discrepancies are larger for 7 nm SiO_2 as compared to those of 12 nm SiO_2.

In the above non-linear regression fitting, $\varepsilon(0)$ is assumed to be a constant of $3.9\varepsilon_0$. However, $\varepsilon(0)$ varies with N_b and μ_b as in Eq. (3-14). Thus N_b and $\varepsilon(0)$ are allowed to vary and the μ_b is set as a constant of 1.065×10^{-29} Cm. Excellent fittings were obtained for all SiO_2 thicknesses studied, and the coefficients of determination (R^2) were all larger than 99.6%. The values of N_b and dielectric constants ε_r [$\varepsilon_r = \varepsilon(0)/\varepsilon_0$] obtained from the nonlinear regression fitting for different SiO_2 thicknesses, with and without anneal are shown in Fig. 3-19. The average dielectric constants of SiO_2 with and without PDA are 3.94 and 4.02, respectively.

The average values of N_b (= N/λ) for SiO_2 with and without PDA are 5.05×10^{20} and 7.10×10^{20} cm^{-3}, respectively and are relatively independent of thickness. A possible explanation for the reduction of the dipole density N (= λN_b) after the PDA is that the dipoles in SiO_2 are generated due to the oxygen vacancy in the Si-O tetrahedron network, where the Si-O-Si bond is replaced by Si-Si bond [42] as illustrated in Fig. 3-19. The $Si{\equiv}O_3$ cell A and B each has a dipole moment of $p = (2e)[3(f_0^*)(r_0/3)] \cong 2.04\ e$Å, where f_0^* (= 0.6) is the bond polarity and r_0 (=1.7 Å) is the Si-O bond length [35]. To achieve a net dipole moment of $\mu_0 \cong 1.065\times10^{-29}/\lambda$ Cm, the angle ϕ between the axes of A and B are ~170.5° and ~ 165.9° for λ = 1.97 and 1.33, respectively. The PDA with O_2 flow eliminates some of these oxygen vacancies and

thus reduces the density of dipoles. Another explanation is that SiO_2 changed from a "relaxed" to "unrelaxed" state after the PDA. In the "unrelaxed" state, the Si and O atoms are fixed at their positions, while in the "relaxed" state, the atoms can move under the electric field [43]. The total dipole moment densities (per volume) determined by first principle total energy in ref. [43] for "unrelaxed" and "relaxed" states are about 0.57 and 0.75 μC/cm^2, which are comparable to the densities (calculated as $N\mu_0$) of 0.54 and 0.76 μC/cm^2 for SiO_2 with and without PDA in this work, respectively.

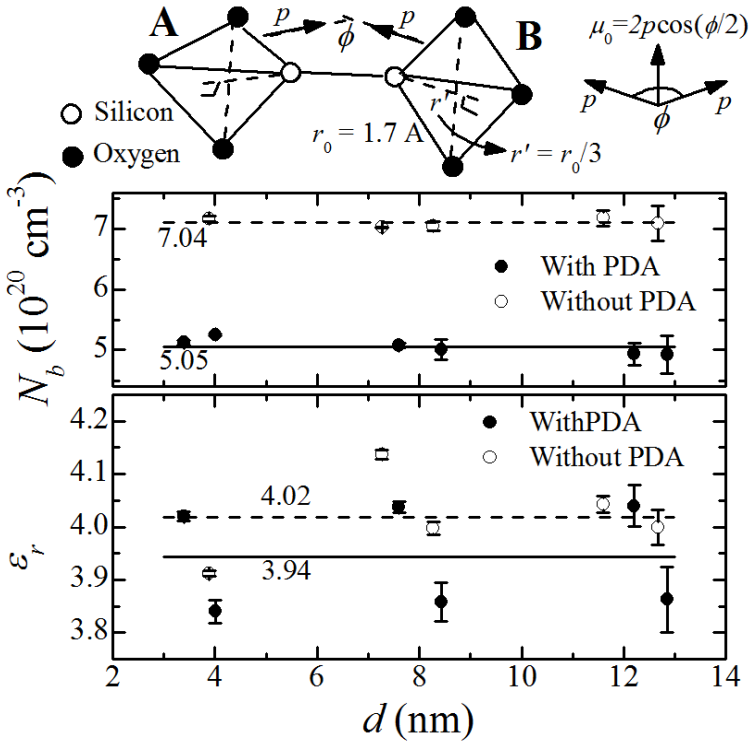

Fig. 3-19: Values of N_b and dielectric constant ε_r obtained from the nonlinear regression fitting of the $\Delta C/C_0$ versus V curves using Eq. (3-16). An illustration of $O_3{\equiv}Si{-}Si{\equiv}O_3$ structure is also shown.

3.5. **Summary**

The MIM capacitors with PECVD and ALD SiO_2 were studied in this chapter. Both types of SiO_2 exhibit negative quadratic VCC, which magnitude can be reduced substantially by a post-deposition anneal. The magnitudes of the quadratic and linear VCCs decrease with increasing measurement frequency. For a given capacitance density, ALD SiO_2 deposited at 200 °C has smaller quadratic VCC (in term of magnitude) than that of ALD SiO_2 deposited at 400 °C. The ALD SiO_2 layers were demonstrated to have low leakage currents and high breakdown field strengths. The leakage current through 4 nm ALD SiO_2 is 10 times lower and the dielectric field strength is 2 MV/cm higher than those of 7 nm PECVD SiO_2. The MIM capacitor with 4 nm ALD SiO_2 deposited at 400 °C achieved a low leakage current of 2×10^{-7} A/cm^2 at 3.3 V, a high field strength of 19.3 MV/cm, and a high operation voltage of 3.6 V for 10-year operation. With such an excellent leakage and breakdown performance, ALD SiO_2 is a very promising material for MIM capacitor applications. The ALD SiO_2 will be stacked with a high-k dielectric in the subsequent chapters.

Besides characterizing the capacitance and leakage performance of the SiO_2 MIM capacitors, the negative quadratic VCC of SiO_2 was successfully modeled in this chapter. The polarization in SiO_2 was modeled as a sum of the electronic, ionic and orientation polarization in which the former 2 are relatively independent of the electric field. The orientation polarization however reduces with increasing electric field, giving rise to the negative quadratic VCC in SiO_2. The normalized capacitance densities against voltage curves for the SiO_2 MIM capacitors fitted the derived Eq. (3-16) very well for the entire range of SiO_2 thicknesses (3-13 nm) investigated here.

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Chapter 4

High Performance MIM Capacitors with Er_2O_3 on ALD SiO_2

4.1. **Introduction**

Among the passive components in radio-frequency (RF) and analog/mixed signal (AMS) integrated circuits, the metal-insulator-metal (MIM) capacitor plays an essential role and occupies a large area in the integrated circuits. To achieve the high capacitance density suggested by the International Technology Roadmap of Semiconductor (ITRS) [1], high-k MIM dielectrics such as Ta_2O_5 [2], HfO_2 [3-4], $TaYO_x$ [5] and Sm_2O_3 [6], or stacked dielectrics such as $Al_2O_3/HfO_2/Al_2O_3$ [7-8] and $HfLaO/LaAlO_3/HfLaO$ [9] were investigated. However, these high-k dielectrics usually have large positive quadratic voltage coefficients of capacitance (VCCs) (symbol α), especially when their thicknesses are scaled down to achieve higher capacitance density. One way to concurrently achieve a low quadratic VCC and a high capacitance density is to stack a high-k dielectric on SiO_2, so that the positive α of the high-k dielectric is compensated by the negative α of SiO_2. This method was demonstrated in recent works on the MIM capacitors with stacked dielectrics of HfO_2 [10] or Sm_2O_3 [11-12] on plasma enhanced chemical vapor deposition (PECVD)

SiO_2. However due to the high capacitance density requirement, both the SiO_2 and high-k dielectric layers were relatively thin, resulting in a high leakage current through the stacked dielectrics. From chapter 3, SiO_2 deposited by atomic layer deposition (ALD) was shown to have a much lower leakage current and higher dielectric field strength than PECVD SiO_2. Thus, replacing PECVD SiO_2 with ALD SiO_2 in the stacked dielectrics is expected to reduce the leakage current of the MIM capacitors substantially.

Besides using ALD SiO_2, a new choice of high-k dielectric is studied in this chapter. Er_2O_3, a lanthanoid dielectric with large band gap of about 5.3-5.5 eV [13-16] and high dielectric constant of 13-17 [17-20], was used as the high-k dielectric of the MIM capacitor. In the first part of this chapter, MIM capacitors with single layer Er_2O_3 are characterized. Er_2O_3 which has a dielectric constant of about 20 and a band gap of 5.29 eV (as shown later) can be sputtered at room temperature with a consistently fast deposition rate. Unlike HfO_2, it can be easily etched by wet-etching method after being annealed at 400 °C. In the second part, a stack of high-k Er_2O_3 on ALD SiO_2 is demonstrated for the first time. The ALD SiO_2 is deposited at low temperatures of 200 and 400 °C, which was characterized in the previous chapter. By stacking high-k Er_2O_3 on the ALD SiO_2, MIM capacitors with high capacitance densities, low leakage currents and low quadratic VCCs are demonstrated.

4.2. **Single layer Er_2O_3 MIM capacitor**

In this experiment, a 20 nm thick Er_2O_3 layer was used as the dielectric of the MIM capacitor. After the bottom TaN electrode was formed on SiO_2 coated Si wafers by sputtering, Er_2O_3 was deposited by direct current (DC) sputtering from an Er metal

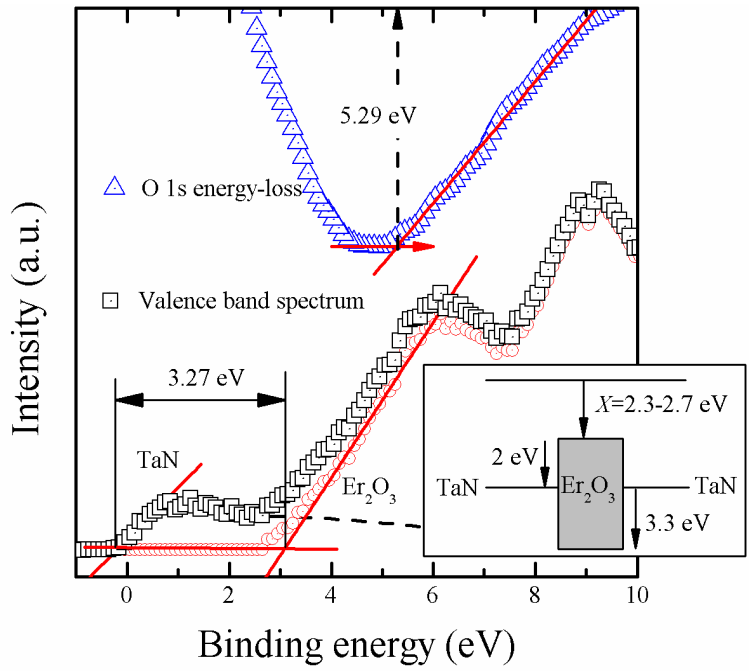

Fig. 4-1: The oxygen (O) 1s energy loss spectrum of Er_2O_3 and the valence band spectrum of a thin layer of Er_2O_3 on TaN measured by XPS. These spectra were used to calculate the band gap and valence band offset between TaN and Er_2O_3. The resulting band structures are shown in the inset.

target with 2 sccm O_2 and 27 sccm Ar gas flow at the room temperature. Spectroscopic ellipsometry determined that the thickness Er_2O_3 was about 20 nm from a control sample, in which Er_2O_3 was sputtered on a bare Si wafer. The dielectric was subjected to 4 different post-deposition treatments: no anneal, post-deposition anneal (PDA) at 400 °C with traced O_2, O_2 plasma treatment at 170 °C for 10 mins, and PDA followed by O_2 plasma treatment. The top TaN electrode was then deposited by sputtering, and patterned by lithography.

X-ray photoelectron microscopy was used to determine the band structures of Er_2O_3. The oxygen (O) 1s energy loss spectrum and the valence band spectrum of a thin Er_2O_3 layer on TaN are shown in Fig. 4-1. The oxygen (O) 1s energy loss can be used to determine the band gap of a dielectric [21-23] by linearly extrapolating the loss spectrum with maximum negative slope to the background level. As shown in

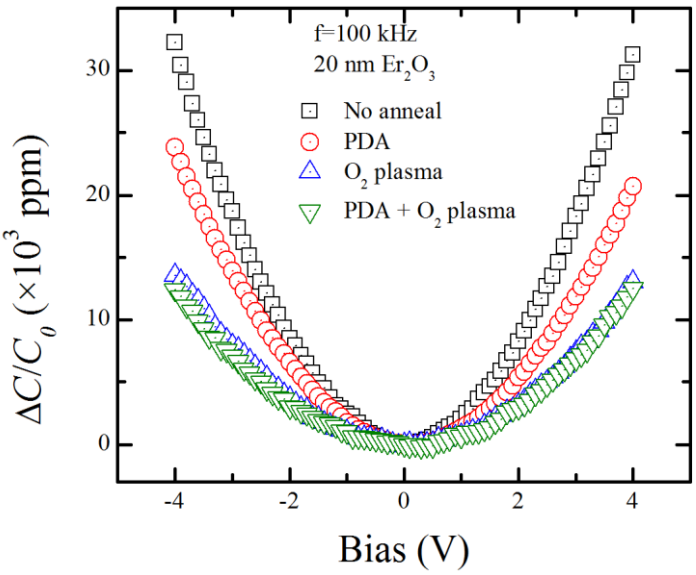

Fig. 4-2: Normalized capacitance ($\Delta C/C_0$) versus bias for MIM capacitors with 20 nm Er_2O_3, subjected to different post-deposition treatments. The measurements were performed with frequency f=100 kHz.

Fig. 4-1, the extracted band gap of Er_2O_3 is approximately 5.29 eV, which is consistent to the band gaps of 5.3-5.5 eV reported by other works [13-16]. The valence band offset between Er_2O_3 and TaN can be estimated from the XPS valence band spectrum of a thin Er_2O_3 layer on TaN, as also shown in Fig. 4-1. The spectrum is deconvoluted into the TaN and Er_2O_3 components, and the calculated valence band offset is 3.27 eV. This method was widely used to compute accurately the valence band offsets of Ta/Ta_2O_5, Si/SiO_2, Al/Al_2O_3 [24] and $Hf_{1-x}Si_xO_2/Si$ [25]. The conduction band offset between TaN and Er_2O_3 is thus ~2 eV. TaN has a work function of about 4.3-4.7 eV [26-29] and thus the electron affinity of Er_2O_3 is 2.3-2.7 eV, which is consistent with a reported value of 2.4 eV [30]. From the above calculated values, the band structures of Er_2O_3 and TaN are as shown in the inset of Fig. 4-1.

The capacitance of an MIM capacitor can be expressed as $C = C_0(1+\beta V+\alpha V^2)$, where C_0, β and α are the capacitance at 0 V bias, the linear VCC, and quadratic

VCC, respectively. The normalized capacitances $\Delta C/C_0 = (C–C_0)/C_0$ versus bias measured at 100 kHz for the Er_2O_3 MIM capacitors with different post-deposition treatments are shown in Fig. 4-2. Unlike SiO_2 presented in the previous chapter, these plots can be fitted excellently into quadratic equations, with positive quadratic VCCs. The post-deposition treatments reduce the quadratic VCC of the MIM capacitors, as seen from the graph. The sample with PDA followed by the O_2 plasma treatment shows the most reduction in the quadratic VCC.

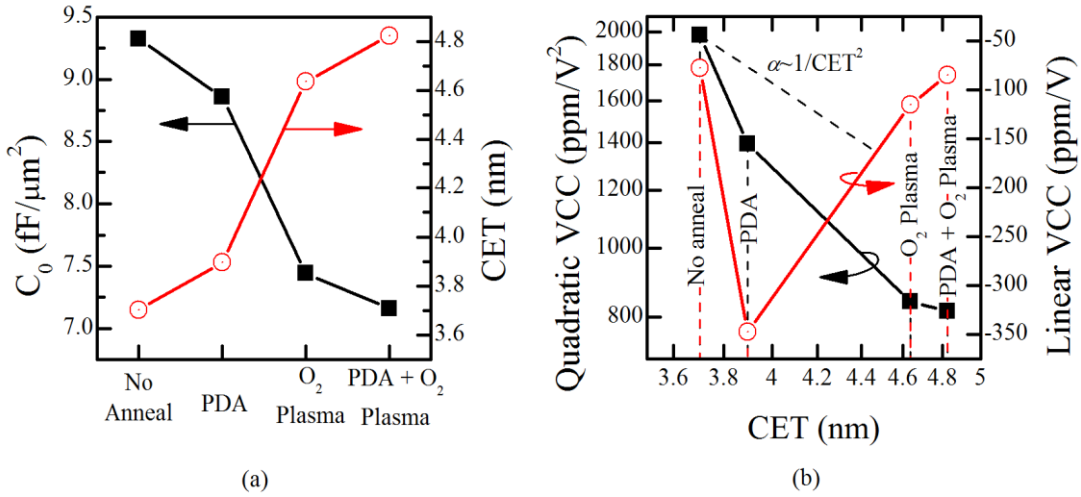

Fig. 4-3: (a) Capacitance density C_0 and corresponding CET and (b) the quadratic and linear VCC versus CET for MIM capacitors with 20 nm Er_2O_3, subjected to different post-deposition treatments.

The capacitance densities of the MIM capacitors with single layer Er_2O_3 and their corresponding capacitive effective (SiO_2) thickness (CET) are shown in Fig. 4-3 (a) and their quadratic and linear VCCs against CET are shown in Fig. 4-3 (b). As seen, high capacitance density of 9.32 fF/μm^2 was achieved with the as-deposited Er_2O_3 MIM capacitor. Thus, the dielectric constant *k* is about 21, which is slightly higher than dielectric constants of 13-17 [17-20] from other reports of Er_2O_3 on Si. However, the lower reported *k* values could be due to the poor reaction between Er_2O_3 and Si [31]. The PDA reduced the capacitance density of the Er_2O_3 capacitors

slightly, corresponding to a 0.2 nm CET increase. The capacitance density however dropped significantly when the O_2 plasma treatment was performed on Er_2O_3, with an increase in CET of about 1 nm. Due to the high amount of O_2 flow and long duration of plasma treatment, it is likely that the bottom TaN electrode was oxidized, resulting in high-k Ta based dielectric and increased the CET of the MIM capacitors. As seen in Fig. 4-3 (b), the PDA and O_2 plasma treatment were shown to reduce the quadratic VCC of the Er_2O_3 capacitors by 1.4 and 2.3 times, respectively. The quadratic VCC α of a dielectric is expected to be inversely proportional to the square of its thickness, as seen in Sm_2O_3 [32], Al_2O_3 [12] and SiO_2 (as presented in previous chapter). Although the CET (and possibly the physical thickness) of Er_2O_3 increased when the PDA and O_2 plasma treatment was applied, the drops in the values of α are much faster than the relation $\alpha \sim 1/CET^2$. The quadratic VCC is reduced because the dielectric could have been crystallized during the PDA, or the Ta based high-k dielectric formed during the O_2 plasma treatment modified the quadratic VCC of the dielectric. The linear VCCs are negative, and their magnitudes are generally much smaller than those of the quadratic VCC.

The leakage currents of the Er_2O_3 MIM capacitors against applied bias from 0 to 10 V in log-log scale are shown in Fig. 4-4. The leakage current through Er_2O_3 with PDA (1.3 μA/cm^2 at 3.3 V) is substantially smaller than that of through Er_2O_3 without PDA (3.8 μA/cm^2 at 3.3 V). Although the O_2 plasma treatment does not improve the leakage currents, it helps to increase the breakdown voltages of the devices. As seen in Fig. 4-4, the capacitors without anneal and with PDA both have a breakdown voltage of about 6.1 V, while the capacitors subjected to O_2 plasma have significantly higher breakdown voltages. Thus the dielectric field strengths of Er_2O_3 with and

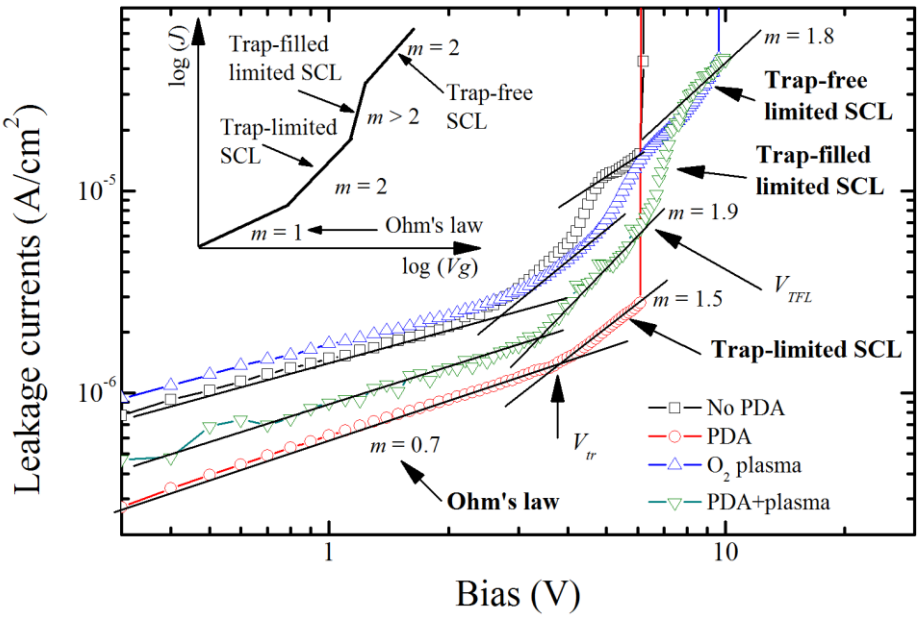

Fig. 4-4: Leakage currents of the MIM capacitors with 20 nm Er_2O_3 for bias from 0 to 10 V. The capacitors without anneal and with PDA break down at about 6.1 V, while the capacitor with O_2 plasma treatment breaks down at 9.5 V. Up to 10V, the capacitor treated with PDA followed O_2 plasma does not breakdown. The inset plots a typical leakage current versus bias in log-log scale due to space charge limited (SCL) conduction.

without PDA are about 3 MV/cm, and those of Er_2O_3 subjected to O_2 plasma are as high as 5 MV/cm.

Several linear regions can be observed from the log(J) versus log (Vg) plots in Fig. 4-4, which match the characteristic of a typical space charge limited (SCL) conduction mechanism shown in the inset [33-34]. The SCL current and voltage has a power law relationship $J \propto V^m$, where m can be extracted from the log$J$ versus log$V$ plot. At low voltage, the leakage current is a bulk conduction governed by Ohm's law where m = 1 due to the presence of thermal equilibrium carriers in the dielectric. When voltage is sufficiently large (V_{tr}), the injected carriers dominates the volume conductivity by Ohm's law, the conduction mechanism becomes trap-limited SCL (m = 2) in which the injected carriers into the dielectric fill up the traps. When sufficient traps are filled (voltage V_{TFL}) , the current rises sharply (m > 2) indicating a trap-filled limited SCL region which was also characterized as emission limited region in certain

work [35]. Beyond that, the dielectric behaves like a trap-free material, and the conduction is limited by the free carriers in the dielectrics, and the current versus voltage power law $J \propto V^2$ holds again.

In Fig. 4-4, the slopes of log$J$ versus log$V$ plots are slightly different from the ideal values because there are possibly other conduction mechanisms such as direct tunneling, thermionic emission. Nevertheless, the errors are within the experimental acceptance. The voltage V_{tr} and V_{TFL} (which mark the start of the trap-limited and trap-filled limited SCL regions, respectively) are larger for capacitors with smaller leakage currents. The values of V_{tr} for Er_2O_3 MIM capacitors with no anneal, O_2 plasma treatment, PDA and PDA followed by O_2 plasma treatment are about 2.5, 2.8, 3.9 and 3.4 V respectively and the corresponding V_{TFL} voltages are 4.1, 4.5, more than 10 V, and 6 V.

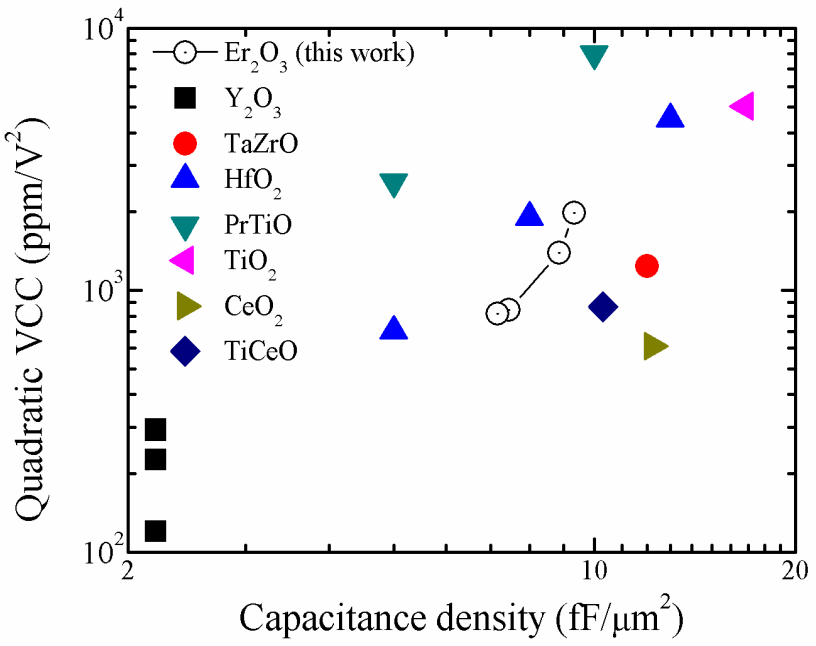

Fig. 4-5: The quadratic VCCs of Er_2O_3 in this work are compared to those of Y_2O_3 [36], TaZrO [37], HfO_2 [4], PrTiO [38], TiO_2, CeO_2 and TiCeO [39].

The quadratic VCC versus capacitance density of Er_2O_3 is compared with the values reported from other high-k dielectrics in Fig. 4-5. For the same capacitance density, Er_2O_3 has comparable quadratic VCCs with the other high-k dielectrics. High capacitance density of 9.3 fF/μm^2 can be achieved, however, the quadratic VCC was very high. The PDA and O_2 plasma treatment can reduce the quadratic VCC to about 800 ppm/V^2, which is still significantly higher than the specified 100 ppm/V^2. The leakage currents at 3.3 V bias are in the order of 10^{-6} A/cm^2, which is 100 times higher than the specified 10^{-8} A/cm^2 by the ITRS [1]. To further reduce the leakage current and quadratic VCC of the capacitor, Er_2O_3 is stacked on ALD SiO_2, as presented in the next section.

4.3. **High performance MIM capacitors with Er_2O_3 on ALD SiO_2**

As shown in the previous section, although high capacitance density was achieved, the quadratic VCC of the MIM capacitors with single layer Er_2O_3 was much higher than 100 ppm/V^2. In this section, the high-*k* Er_2O_3 is stacked on ALD SiO_2, such that the negative quadratic VCC from SiO_2 compensates the positive quadratic VCC from Er_2O_3. The device fabrication process started with the sputtering of a 150 nm thick TaN bottom electrode on SiO_2-covered Si substrates. SiO_2 layers with specified 3 nm thickness were deposited by atomic layer deposition (ALD) at 200 and 400 °C, denoted as "SiO_2 (200 °C)" and "SiO_2 (400 °C)", respectively. The CETs of 3 nm SiO_2 (200 °C) and (400 °C) are 2.3 and 3.3 nm, respectively. Er_2O_3 layers with thicknesses of 6-9 nm were subsequently sputtered. Based on the study in chapter 3 and 4.2, the Er_2O_3 thicknesses were chosen to have matching quadratic VCCs to those of SiO_2. Post-deposition anneal (PDA) at 400 °C for 2 minutes in N_2 ambient with

traces of O_2 was performed on the stacked dielectrics. Next, the top TaN electrode was sputter-deposited. Optical lithography and dry etching were used to define the top TaN electrode. The bottom TaN electrode was exposed by wet etching of Er_2O_3 and SiO_2.

A low power (12 W) radio-frequency (RF) bias is commonly applied to the wafer holder to generate substrate plasma, which improves the uniformity of the sputtered films. In a control experiment, the RF bias was applied to the substrate during the sputtering of Er_2O_3 and the top TaN electrode in selected samples. However as presented in section 3.1, the generated plasma has a detrimental effect on the performance of the MIM capacitors, especially the leakage current performance. As such, in the main experiment, RF bias was not applied to the substrate during the sputtering of Er_2O_3 and the top TaN electrode.

4.3.1 **Effect of substrate plasma on the performance of the MIM capacitors**

The control experiment was carried out on the MIM capacitors with single layer 4 nm SiO_2 (400C) and capacitors with 8.9 nm Er_2O_3 on 3.3 nm ALD SiO_2 (400C) stacked dielectrics. In some samples, the RF bias was applied to the substrate holder during the sputtering of Er_2O_3 and the top TaN electrode. The leakage currents of MIM capacitors with single layer 4 nm SiO_2 (400C) and the stacked dielectrics are shown in Fig. 4-6 (a) and (b) respectively. Compared to a control device in which no RF bias was applied, the leakage current of MIM capacitors increased by 2 times when RF bias was applied during the deposition of TaN. However, the leakage currents increased by 10 to 100 times when the RF bias was applied during the sputtering or Er_2O_3, as seen in Fig. 4-6 (b). The plasma could have caused some

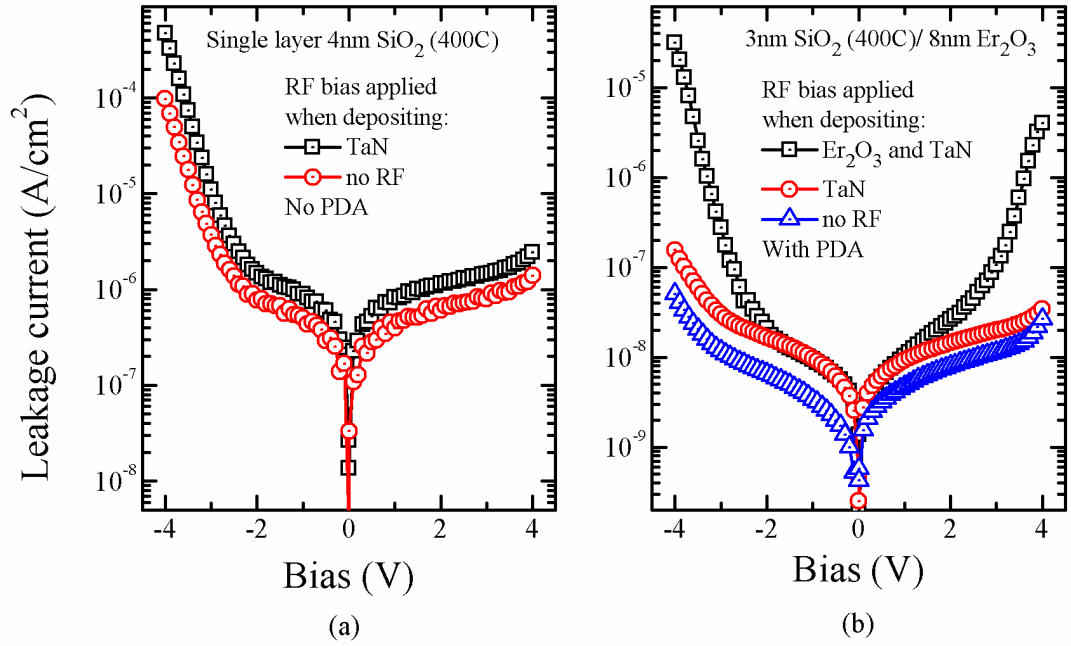

Fig. 4-6: Effect of RF bias on the leakage currents of single layer 4 nm SiO_2 (400C) and stacked 8.9 nm Er_2O_3 /3.3 nm SiO_2 (400C) capacitors.

damages on the surface of the SiO_2 and Er_2O_3 layers during the sputtering of TaN. However, after a layer of TaN was formed, the dielectrics surface could have been protected, and the degradation of the surface was stopped and as a result, the leakage currents only increased slightly. On the other hand, the quality of Er_2O_3 is significantly degraded during the deposition of Er_2O_3 when the substrate plasma was generated, because the plasma constantly etched the surface of the reactive Er_2O_3. The distributions of leakage currents at 3.3 and -3.3 V of the MIM capacitors with the stacked dielectrics are shown in Fig. 4-7. The distributions were fitted to the Weibull distributions, and the mean leakage currents at 63.2% for the samples are listed in Table 4-1. The leakage currents at 3.3 V of the MIM capacitors in which no RF bias applied are about 0.9-2×10^{-8} A/cm^2, with a mean of 1.4×10^{-8} A/cm^2. These increased to 2-4×10^{-8} and 10^{-7}-10^{-6} A/cm^2 when the RF bias was applied during the deposition of TaN and both Er_2O_3 and TaN, respectively. The leakage currents on the negative

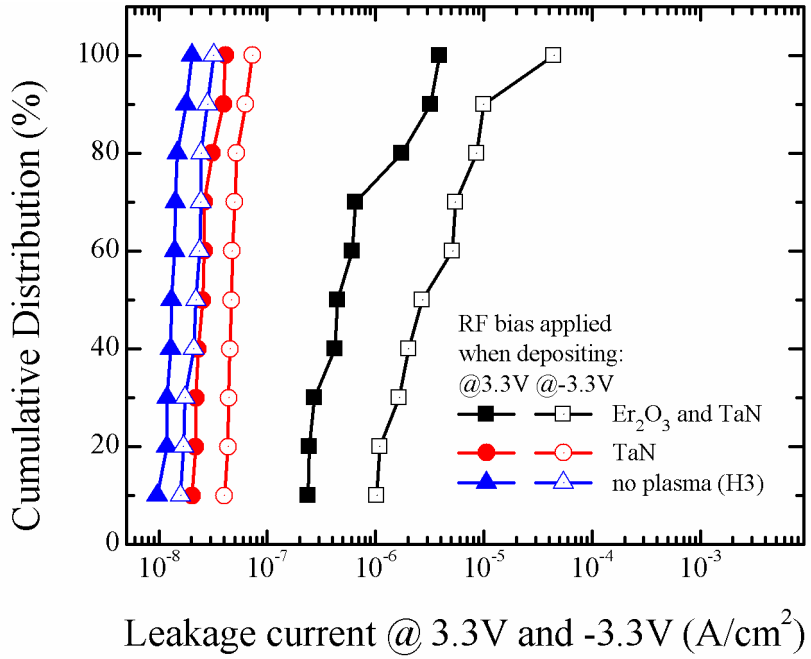

Fig. 4-7: Leakage currents at bias of 3.3 and -3.3V of MIM capacitors with 8 nm Er_2O_3 /3.3 nm SiO_2 (400C) stacked dielectrics.

bias are higher than those on the positive bias, and the difference is the largest for the MIM capacitors with plasma generated during the sputtering of both Er_2O_3 and TaN.

The substrate plasma also affected the capacitance performance of the MIM capacitors as seen in Fig. 4-8 where the normalized capacitance density $\Delta C/C_0$ measured at 100 kHz and the frequency dependent quadratic VCC of MIM capacitors with 8.9 nm Er_2O_3 on 3.3 nm SiO_2 (400C) stacked dielectrics are shown. The quadratic VCC of the control sample with no applied RF bias is generally smaller, and its variation with frequency is lesser. For the measured frequency range, the quadratic VCC varied from -73 to 89 ppm/V^2 for the control MIM capacitor and from -120 to 140, -280 to 220 ppm/V^2 for the MIM capacitors with RF bias applied to the substrate holder during the sputtering of TaN only and both TaN and Er_2O_3, respectively. Noting the detrimental effect of the substrate plasma on the leakage current and

quadratic VCC of the MIM capacitors, no RF bias was applied during the sputtering of Er_2O_3 and top TaN electrode in the subsequent experiments.

Table 4-1: Mean leakage currents measured at 3.3 and -3.3 V for the MIM capacitors with 8.9 nm Er_2O_3 on 3 nm ALD SiO_2 (400C) stack dielectrics, showing the effect of the substrate RF bias applied during the sputtering of TaN and Er_2O_3.

RF applied during the sputtering of:	*J* @ 3.3V (10^{-8} A/cm^2)	*J* @ -3.3V (10^{-8} A/cm^2)
Er_2O_3 and TaN	101	608
TaN	2.9	5.3
No Plasma	1.4	2.4

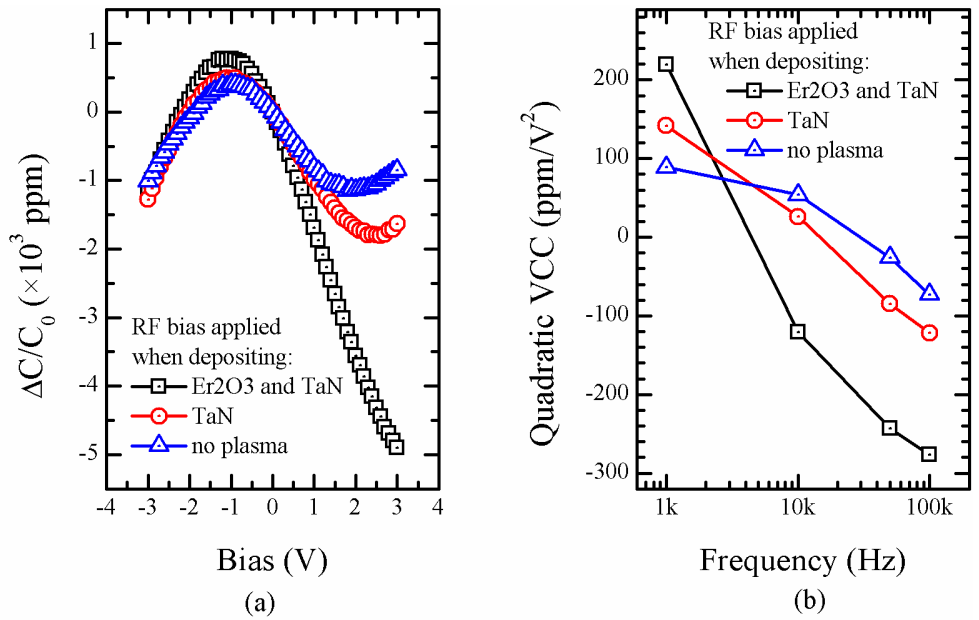

Fig. 4-8: (a) The normalized capacitance density $\Delta C/C_0$, measured at 100 kHz and (b) frequency dependent quadratic VCC of the MIM capacitors with 8.9 nm Er_2O_3 on 3.3 nm SiO_2 (400C). The RF bias was applied during the sputtering of Er_2O_3 and TaN in certain samples.

4.3.2 Er_2O_3/SiO_2 MIM capacitor

The frequency dependent capacitance densities and dissipation factors $tan\delta$ of the MIM capacitors with Er_2O_3/SiO_2 stacked dielectrics are shown in Fig. 4-9 (a) and

(b), respectively. The capacitance densities remain constant over the frequency range with the thickest dielectric stack having a capacitance density of about 7 fF/μm^2. The capacitance densities of MIM capacitors with stacked dielectrics on SiO_2 (200 °C) are higher than those on SiO_2 (400 °C), due to the smaller CET from SiO_2 (200 °C). The thicknesses of the Er_2O_3 layers in the stack dielectrics, values of which are indicated in the figures, are estimated from the capacitance densities of the stack dielectrics and single layer SiO_2 and Er_2O_3. The dissipation factors increase with frequency due to the increased capacitor reactance, and are generally smaller than 0.02, corresponding to quality factors of at least 50. The dissipation factors can be further improved by reducing the contact resistance; however that is not the main focus of this work.

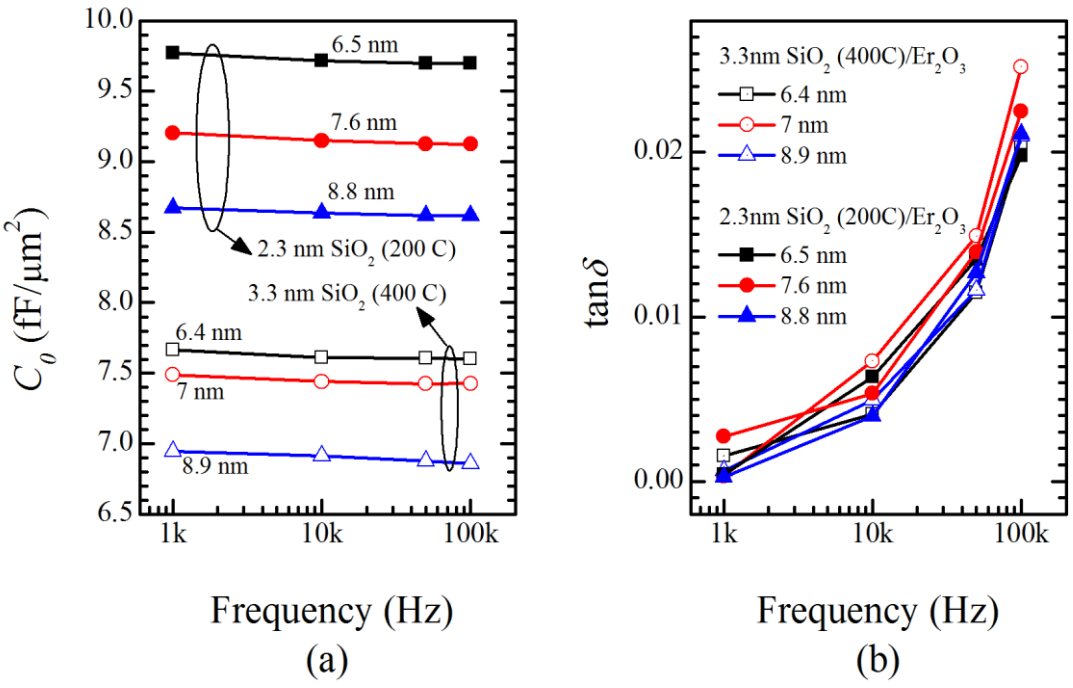

Fig. 4-9: Frequency dependent (a) capacitance densities and (b) dissipation factor tanδ of the MIM capacitors with PVD Er_2O_3 on ALD SiO_2 stacked dielectrics.

The normalized capacitances $\Delta C/C_0 = (C–C_0)/C_0$ measured at 100 kHz of the capacitors are shown in Fig. 4-10. The capacitors with Er_2O_3 stacking on 3.3 nm ALD SiO_2 (400 °C) and 2.3 nm ALD SiO_2 (200 °C) have negative and positive quadratic

VCCs, respectively. The extracted values of α as a function of frequency are shown in Fig. 4-11. The α values reduce with increasing frequency. For the capacitors with Er_2O_3 on 3.3 nm ALD SiO_2 (400 °C), the quadratic VCCs were negative, which increased towards zero with thicker Er_2O_3. The trend is, however, opposite for samples with Er_2O_3 on 2.3 nm ALD SiO_2 (200 °C). The capacitor with 8.9 nm Er_2O_3 on 3.3 nm SiO_2 (400 °C) has low α values from 89 to -73 ppm/V^2 and high capacitance densities of 6.95 to 6.86 fF/μm^2. The capacitor with 7 nm Er_2O_3 on 3.3 nm SiO_2 (400 °C) has a capacitance density of 7.5 fF/μm^2 and a quadratic VCC within ±100 ppm/V^2 range at low frequency. The capacitor with 8.9 nm Er_2O_3 on 2.3 nm SiO_2 (200 °C) has a capacitance density of 8.6 fF/μm^2 and a quadratic VCC of 154 ppm/V^2 at 100 kHz. The quadratic VCC is expected to reduce below 100 ppm/V^2 at 500 kHz.

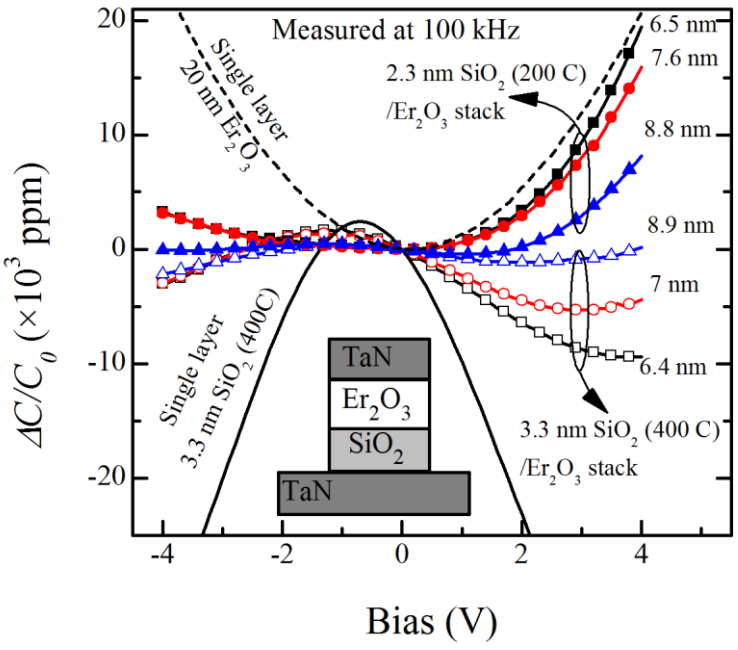

Fig. 4-10: Normalized capacitance ($\Delta C/C_0$) of the MIM capacitors with PVD Er_2O_3 on ALD SiO_2 stacked dielectrics.

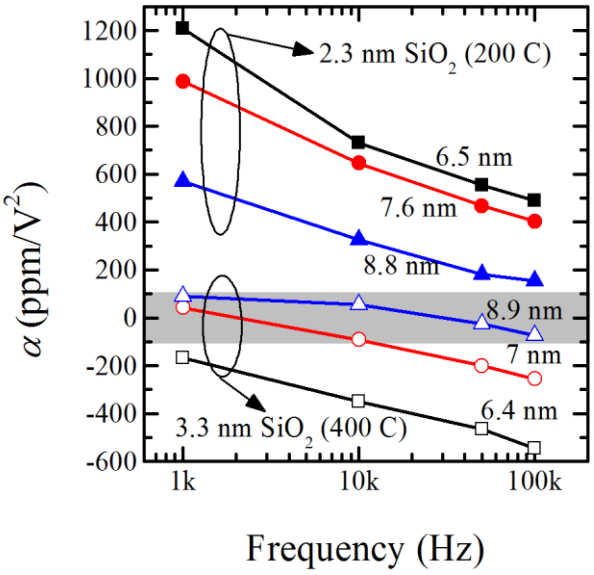

Fig. 4-11: Frequency dependent quadratic VCC of the MIM capacitors with PVD Er_2O_3 on ALD SiO_2 stacked dielectrics.

An MIM capacitor C with the stacked dielectrics can be modeled as two capacitors C_1 (SiO_2) and C_2 (Er_2O_3) in series. The capacitance density at zero bias, linear VCC and quadratic VCC of Er_2O_3/SiO_2 stack, SiO_2 and Er_2O_3 are (C_0, β, α), (C_{1o}, β_1, α_1), and (C_{2o}, β_2, α_2), respectively. The individual normalized capacitances of SiO_2 and Er_2O_3 are expressed in term of the potential V_1 and V_2 across SiO_2 and Er_2O_3:

$$\Delta C_1/C_{1o} = \alpha_1 V_1^2 + \beta_1 V_1. \quad (4\text{-}1)$$

and

$$\Delta C_2/C_{2o} = \alpha_2 V_2^2 + \beta_2 V_2. \quad (4\text{-}2)$$

The total capacitance C of the stacked dielectrics is related to C_1 and C_2 by the equation:

$$1/C = 1/C_1 + 1/C_2. \quad (4\text{-}3)$$

Taking the 1st order derivative of the above equation, one arrives at:

$$\Delta C/C_0^2 = \Delta C_1/C_{1o}^2 + \Delta C_2/C_{2o}^2, \quad (4\text{-}4)$$

$$\text{i.e. } \Delta C/C_0 = (C_0/C_{1o})\times\Delta C_1/C_{1o} + (C_0/C_{2o})\times\Delta C_2/C_{2o}. \quad (4\text{-}5)$$

Moreover,

$$C_0/C_{1o} = V_1/V \text{ and } C_0/C_{2o} = V_2/V. \quad (4\text{-}6)$$

Substituting Eq. (4-1), (4-2), and (4-6) into Eq. (4-5), one reaches:

$$\Delta C/C_0 = \alpha V^2 + \beta V \quad (4\text{-}7)$$

where

$$\beta = (C_{1o}^2\beta_2 + C_{2o}^2\beta_1)/(C_{1o} + C_{2o})^2, \quad (4\text{-}8)$$

and

$$\alpha = (C_{1o}^3\alpha_2 + C_{2o}^3\alpha_1)/(C_{1o} + C_{2o})^3. \quad (4\text{-}9)$$

The Eq. (4-9) can also be rearranged into:

$$\alpha = C_0^3 (\alpha_2/C_{2o}^3 + \alpha_1/C_{1o}^3). \quad (4\text{-}10)$$

In Fig. 4-12, the quadratic VCCs of the stacked dielectrics are plotted against the capacitance densities. The grey box indicates the region satisfying the ITRS requirement for year 2013-2015: a quadratic VCC within ±100 ppm/V^2 and a capacitance density of at least 7 fF/μm^2. The capacitors with 7 and 8.9 nm Er_2O_3 on 3.3 nm SiO_2 (400C) and 8.9 nm Er_2O_3 on 2.3 nm SiO_2 (200C) satisfy these requirements. The α value decreases with C_0 for the stack on 3.3 nm SiO_2 (400C) and increases with C_0 for the stack on 2.3 nm SiO_2 (200C). The estimated trends of α against C_0 for the MIM capacitors with Er_2O_3 (varied thicknesses) stacking on SiO_2 [fixed thicknesses of 3.3 and 2.3 nm for SiO_2 (400C) and (200C), respectively] are shown in Fig. 4-12. The maximum capacitance densities are about 10.5 and 15 fF/μm^2

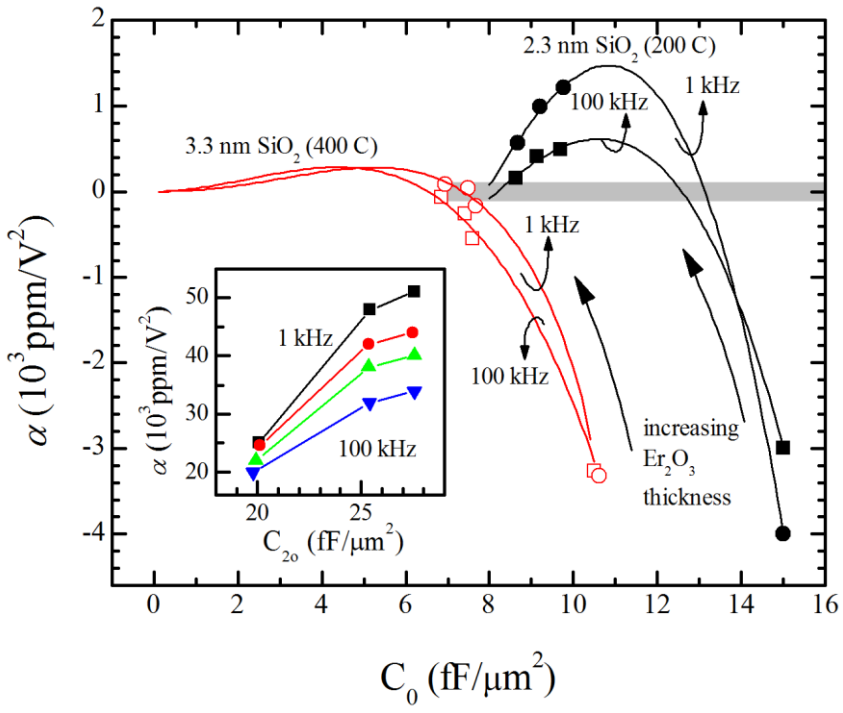

Fig. 4-12: The quadratic VCCs versus capacitance densities of the MIM capacitors with stacked dielectrics. Inset: quadratic VCCs versus capacitance densities of Er_2O_3 dielectrics.

for the stack on 3.3 nm SiO_2 (400C) and 2.3 nm (200C), respectively when the Er_2O_3 thickness is 0. The quadratic VCCs of 3.3 nm SiO_2 (400C) and 2.3 nm SiO_2 (400C) are obtained and extrapolated, respectively from chapter 3. Two regions are expected from the trends: the SiO_2-dominant region where the quadratic VCC α becomes less negative with increasing Er_2O_3 thickness, crosses the zero α point and reaches a maximum value; and the Er_2O_3-dominant region where the positive α decreases with increasing Er_2O_3 thickness. In short, α is more negative and positive with larger C_0 in the SiO_2-dominant and Er_2O_3-dominant regions, respectively. As shown in Fig. 4-12, the quadratic VCCs of the stacks on 2.3 nm SiO_2 (200C) and 3.3 nm SiO_2 (400C) fall into the Er_2O_3-dominant and SiO_2-dominant region, respectively. For the stack on 2.3 nm SiO_2 (200C), the quadratic VCC is expected to reach zero at a capacitance density higher than 9.6 fF/μm^2 (possibly as high as 13 fF/μm^2) when the Er_2O_3 layer is thinner than 6.5 nm.

Using Eq. (4-9), the quadratic VCC of 6.4, 7 and 8.9 nm Er_2O_3 are estimated from the capacitance density and quadratic VCC of the MIM capacitors with stacked dielectrics and single layer 3.3 nm SiO_2 (400 C). The frequency dependent quadratic VCC for different capacitance density of Er_2O_3 is shown in the inset of Fig. 4-12. The quadratic VCC of Er_2O_3 reduces with increasing frequency which is consistent with the trends of other high-k dielectrics [4, 12].

The leakage currents of the MIM capacitors with Er_2O_3/ALD SiO_2 stacked dielectrics are shown in Fig. 4-13. Samples with thicker Er_2O_3 layers exhibit lower leakage currents. For the samples with Er_2O_3/ALD SiO_2 (400 °C) stacked dielectrics, the currents on positive and negative bias were approximately the same, indicating similar top and bottom electron injection. For samples with Er_2O_3/ALD SiO_2 (200 °C), the bottom injection (positive bias) is higher than the top injection (negative bias). The leakage current at 3.3 V of the MIM capacitor with 8.9 nm Er_2O_3 on 3.3 nm SiO_2 (400 C) is as low as 10^{-8} A/cm^2. The leakage currents at 3.3 V of the capacitors with 7 nm Er_2O_3 on 3.3 nm SiO_2 (400 C) and 8.8 nm Er_2O_3 on 2.3 nm SiO_2 (200 C) are 1×10^{-7} and 2×10^{-7} A/cm^2 respectively. At 1V, the leakage currents of the 2 capacitors are 2 and 2.8×10^{-8} A/cm^2, and at 2 V, 4.1 and 4.5×10^{-8} A/cm^2. It is noted that the leakage current, capacitance density and the quadratic VCC of the capacitor with 8.9 nm Er_2O_3 on 3.3 nm SiO_2 (400 C) satisfy the ITRS requirements for year 2013-2015 [1]. The leakage currents of the stack on 2.3 nm SiO_2 (200C) increase gently for bias from 0 to about 2.8 V. From 3 V bias, the currents rise sharply with bias. The sharp increase is observed for the stack on 3.3 nm SiO_2 (400 C) only at a bias close to 4 V. This is because for a given bias applied across the stack dielectrics, the electric field across the 2.3 nm SiO_2 is higher than that across 3.3 nm SiO_2. As seen in Fig. 4-14 (a), the electric field across SiO_2 is about 5 times higher than that

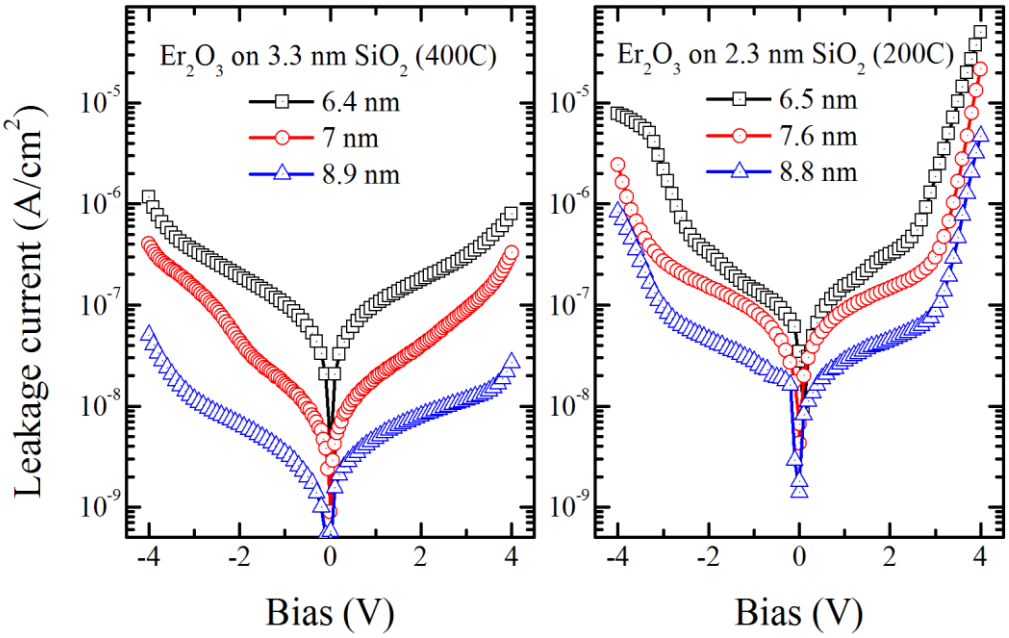

Fig. 4-13: Leakage currents of MIM capacitors with Er_2O_3 on (left) 3.3 nm ALD SiO_2 (400C and 2.3 nm ALD SiO_2 (200 C) stacked dielectrics.

across Er_2O_3. With an applied bias of 3V which triggers the sharp increase in the leakage current, the electric field across the SiO_2 layer in the stack of 6.5 nm Er_2O_3 on 2.3 nm SiO_2 is about 8.3 MV/cm. To achieve similar electric field across 3.3 nm SiO_2, the bias is about 3.8 V. The slopes of the linear regions in the log$J$ versus log$V$ plots for the MIM capacitors with 6.5 nm Er_2O_3 on 2.3 nm SiO_2 in Fig. 4-14 (b) is 0.9, suggesting that the leakage currents with the gentle slope at low voltage from 0-2.8 V are likely due the bulk conduction following Ohm's law. The direct tunneling, which is difficult to be characterized, is also expected at this bias range. The sharp increase in the leakage current occurs when the electric field across SiO_2 is higher than 8.3 MV/cm. As seen from the band diagram in Fig. 4-14 (a), FN tunneling requires a potential drop across SiO_2 of at least 3-3.5 V (corresponding to potential barrier height between TaN and SiO_2) and thus it is not likely the conduction mechanism responsible for the sharp increase in leakage current. From the log(J) versus $E_{ox}^{1/2}$ plot

where E_{ox} is the electric field across SiO_2 in Fig. 4-14 (b), 2 linear regions are observed: one at low bias with a gentle gradient and one at high bias with a large gradient. The corresponding dielectric constants calculated from the slopes using the Schottky emission equation [Eq. (3-3)] is 183 and 3.9, respectively. This indicates that the sharp rise in leakage current from 3V is due to the Schottky (thermionic) emission. It is also worth noting that in the study of single layer SiO_2 (200 C) in chapter 3, Schottky emission was also observed when the electric field across SiO_2 was higher than 8.5 MV/cm.

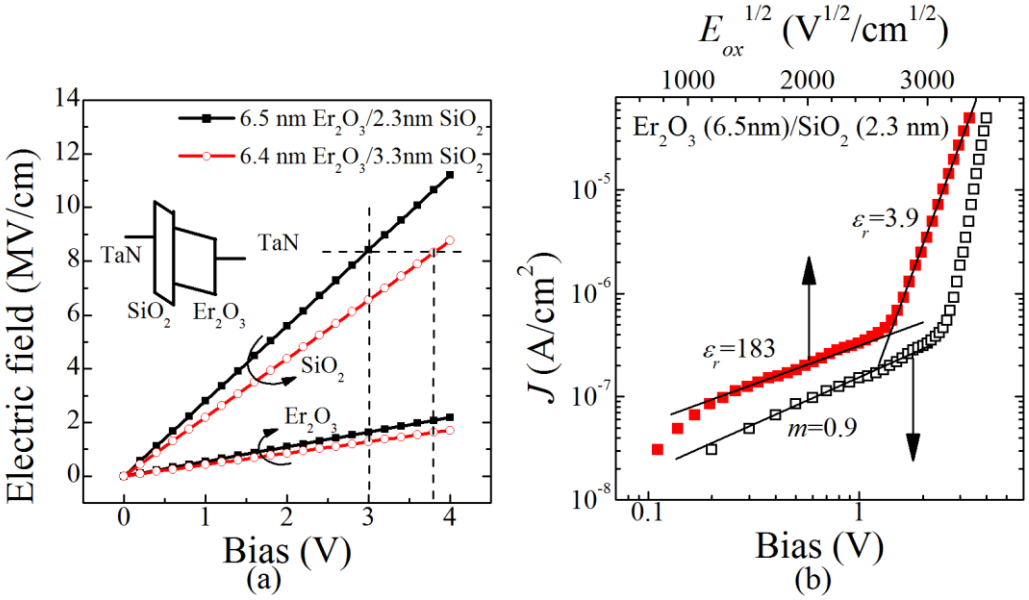

Fig. 4-14: (a) Electric field across SiO_2 and Er_2O_3 for given applied bias across the stack dielectrics. (b) log(J) versus log(V) and $E_{ox}^{1/2}$ for the MIM capacitors with 6.5 nm Er_2O_3 on 2.3 nm ALD SiO_2 (200 C) stacked dielectrics.

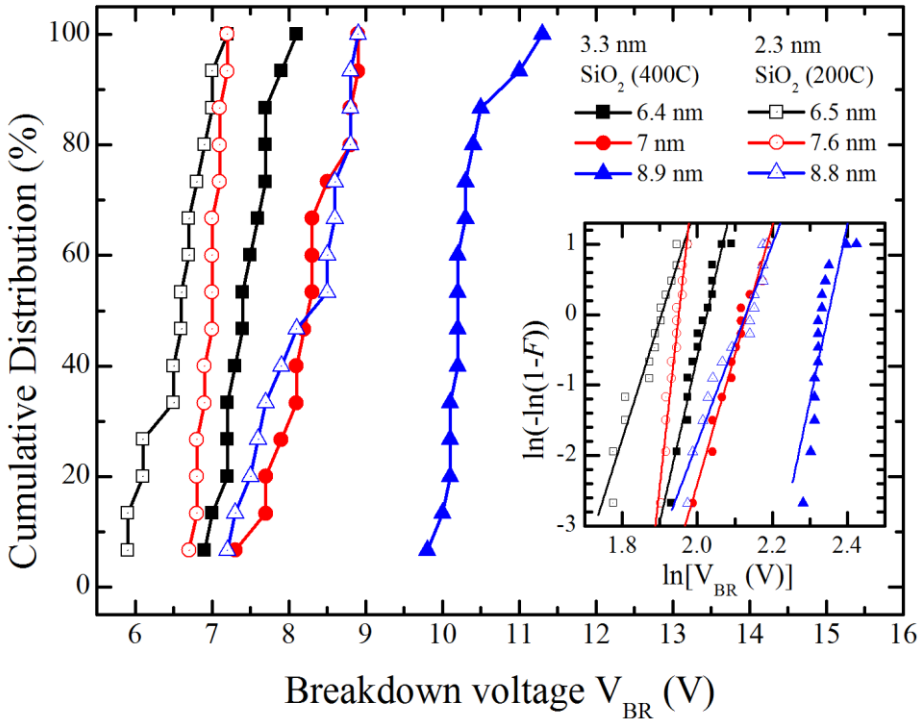

Fig. 4-15: Cumulative distributions of the breakdown voltages of the MIM capacitors with Er_2O_3 on ALD SiO_2 stacked dielectrics. Inset: Weibull plot of ln(-ln(1-*F*) versus ln(V_{BR}).

The cumulative distributions of the breakdown voltages for the MIM capacitors are shown in Fig. 4-15. The MIM capacitors with thicker dielectric stacks have higher breakdown voltages. Samples with 3.3 nm ALD SiO_2 (400 °C) have higher breakdown voltage than those with 2.3 nm ALD SiO_2 (200 °C), due to the thicker oxide. The cumulative distributions were converted to the Weibull distribution of ln(-ln(1-*F*)) versus ln(*V*) plots (*F* and *V* are cumulative probability and breakdown voltage respectively) and fitted with straight lines to obtain the characteristic breakdown voltage at 63.2% failure, as shown in the inset of Fig. 4-15. The breakdown voltages at 63.2% failure and the corresponding dielectric field strength of the MIM capacitors are listed in Table 4-2. A high breakdown field strength of 8.6 MV/cm was demonstrated.

Table 4-2: Breakdown voltages and dielectric field strengths at 63.2% for the MIM capacitors with Er_2O_3/SiO_2 stacked dielectrics.

SiO_2 (nm)	Er_2O_3 (nm)	V_0 (V)	E_0 (MV/cm)
3.3 (400 C)	6.4	7.58	7.81
	7	8.43	8.18
	8.9	10.48	8.59
2.3 (200 C)	6.5	6.72	7.63
	7.6	7.03	7.10
	8.8	8.41	7.57

Constant voltage stress test was performed on the capacitors with 7 and 8.9 nm Er_2O_3 on 3.3 nm SiO_2 (400 C) and 8.8 nm Er_2O_3 on 2.3 nm SiO_2 (200 C), each with 3 different stressing voltages. The representative stress leakage currents versus time for the capacitors with 7 and 8.9 nm Er_2O_3 on 3.3 nm SiO_2 (400 C) are shown in Fig. 4-16. In a study on the conduction mechanisms in a constant voltage stress test by Ramprasad [40], it was found that time dependent leakage current was inversely proportional to stress time, increased slowly with stress time or remained relatively constant when the conduction mechanisms through the dielectric was trap assisted tunneling, Poole-Frenkel emission or Fowler-Nordheim tunneling, respectively. As seen from Fig. 4-16, the leakage currents reduced with stress time at first, after which it increased slowly until breakdown occurred suggesting that the conduction started with trap assisted tunneling at the start of the voltage stress test and changed to Poole-Frenkel as the stress time is longer.

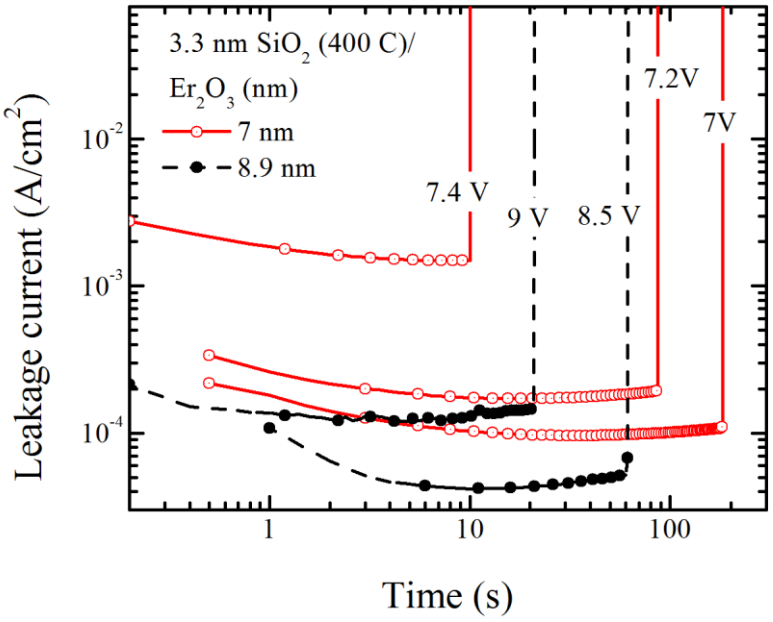

Fig. 4-16: Leakage currents under constant voltage stress for the MIM capacitors with 7 and 8.9 nm Er_2O_3 on 3.3 nm ALD SiO_2 (400C).

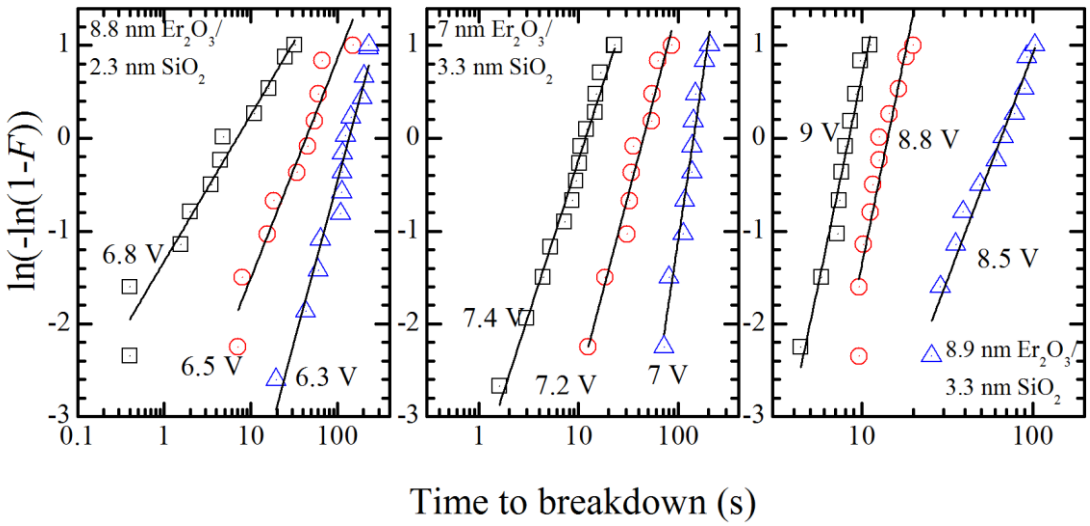

Fig. 4-17: Cumulative distributions of the time to breakdown in a constant voltage stress test of the MIM capacitors with the stacked dielectrics indicated in the plots.

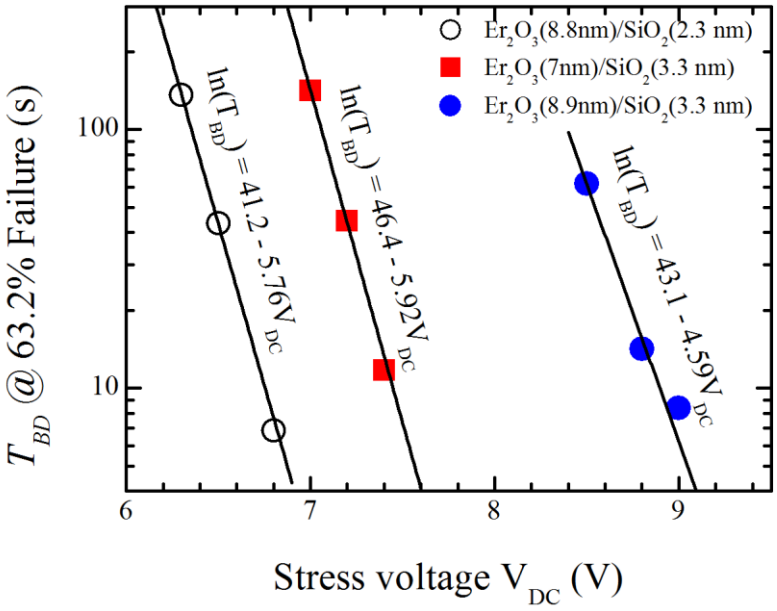

Fig. 4-18: Time to breakdown T_{BD} at 63.2% failure against stress voltage of the studied MIM capacitors.

The cumulative distributions versus time to breakdown for the MIM capacitors are shown in Fig. 4-17, from which the time to breakdown at 63.2% failure were obtained for each stress voltage by fitting the distributions with Weibull functions. The time to breakdown at 63.2% failure T_{BD} was plotted against the stress in Fig. 4-18. The fitted straight lines and their equations are shown in the graph, from which the operation voltages for 10 year lifetime were extracted to be 4.5, 5.1 and 3.7 V, respectively for the MIM capacitors with 7 and 8.9 nm Er_2O_3 on 3.3 nm SiO_2 (400 C) and 8.8 nm Er_2O_3 on 2.3 nm SiO_2 (200C), respectively.

A performance comparison between the MIM capacitor with Er_2O_3 on ALD SiO_2 presented in this work and some of the recently published works is listed in Table 4-3. Among the capacitors meeting the capacitance density and α requirements of 7 fF/μm^2 and <100 ppm/V^2, respectively, this work features the lowest leakage current and the highest field strength.

Table 4-3: Comparison of this work with recently published works which demonstrated MIM capacitors with low quadratic VCC.

Structure	C_0 (fF/μm^2)	α at 100KHz (ppm/V^2)	Leakage current @ 3.3V (A/cm^2)	Field strength (MV/cm)	Ref.
3.3nm SiO_2(400C)/8.9nm Er_2O_3	7	-73	1×10^{-8}	8.6	*
3.3nm SiO_2(400C)/ 7nm Er_2O_3	7.5	-255	1×10^{-7}	8.2	*
2.3nm SiO_2(200C)/ 8.8nm Er_2O_3	8.6	154	2×10^{-7}	7.6	*
HfO_2/SiO_2	6	14	1×10^{-8}	-	[10]
Sm_2O_3/SiO_2	7.3	-46	1×10^{-7}	6	[11]
Sm_2O_3/SiO_2	7.9	-56	2×10^{-7}	7	[12]
$TaYO_x$	5.4	120	4×10^{-3}	3.5-4.5	[5]
Sm_2O_3	7.35	234	6×10^{-8}	-	[6]
$Ta_2O_5/HfO_2/Ta_2O_5$	4	16.9	1×10^{-7}	-	[41]
$Pr_2Ti_2O_7/SiO_2$	3.2	-100	2×10^{-9} (^)	6.5	[42]
$SrTiO_3/ZrO_2$	11.5	-60	3.5×10^{-8} (#)	4	[43]
SrTaO	10	300	4×10^{-8}	6	[44]
HfO_2/Al_2O_3	4.3	207 (##)	$< 1\times10^{-8}$	6	[7]

* this work
(^) leakage current at 2 V (#) leakage current at 2 V
(##) quadratic VCC measured at 1 MHz

4.4. **Summary**

In this chapter, high-k dielectric Er_2O_3 was investigated for high capacitance density, precision MIM capacitors. With a single layer 20 nm Er_2O_3, a capacitance density of 9.3 fF/μm^2 was achieved, with leakage current of about 10^{-6} A/cm^2 (measured at 3.3 V). However, the positive quadratic VCCs of MIM capacitors with 20 nm Er_2O_3 are still relatively higher than 100 ppm/V^2. To further reduce the quadratic VCC, Er_2O_3 was stacked on ALD SiO_2, featuring excellent capacitance, leakage and reliability performance. The MIM capacitor with 8.9 nm Er_2O_3 on 3.3 nm ALD SiO_2 deposited at 400 °C stacked dielectrics was demonstrated to have high capacitance density of ~7 fF/μm^2, low quadratic VCC of less than

100 ppm/V^2, low leakage current at 3.3 V of 1×10^{-8} A/cm^2 and a high breakdown field strength of 8.6 MV/cm. The operating voltage for 10 year life time of the capacitor is as high as 5.1 V. The MIM capacitor with 8.8 nm Er2O3 on 2.3 nm SiO2 (200C) also demonstrated high capacitance density of 8.6 fF/μm^2, a low quadratic VCC which is expected to be smaller than 100 ppm/V^2 at 500 kHz, and a low leakage current of 4.5×10^{-8} A/cm^2 at 2 V. The low α value is the result of combining the negative α of SiO_2 with the positive α of Er_2O_3 while the high field strength and low leakage current are attributed to the high quality SiO_2 layer deposited by atomic layer deposition.

References

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Chapter 5

MIM Capacitors for High Voltage Applications

5.1. **Introduction**

In chapter 4, the metal-insulator-metal (MIM) capacitors with high capacitance densities, low quadratic voltage coefficients of capacitance (VCCs) and low leakage currents were demonstrated using Er_2O_3 on SiO_2 stacked dielectrics. However, these MIM capacitors have low breakdown voltages and only suitable for applications with an operating voltage less than 5 V. Higher operating voltages of 24, 28 or 30 V may be required in some applications, such as radar, cellular infrastructure, and power amplifier in which increasing the capacitance densities of the capacitors will reduce the circuit size. Moreover, the MIM capacitors may also be integrated on top of the GaN and SiC power devices. Thick Si_3N_4 film (50-100nm) deposited by plasma enhanced chemical vapour deposition (PECVD) was often used in the high voltage MIM capacitors, and capacitance densities of 0.5-1 $fF/\mu m^2$ was often achieved [1-4]. However, the dielectric constant of Si_3N_4 is about 7.5, which is about 3 times smaller than those of HfO_2 and Er_2O_3. In this chapter, the high-k dielectrics HfO_2 and Er_2O_3 are investigated for the high voltage MIM capacitor

applications. Several dielectric structures are studied: single layer Er_2O_3 and HfO_2 deposited by physical vapour deposition (PVD), stacked dielectrics of PVD Er_2O_3 on atomic layer deposition (ALD) or PECVD SiO_2. Several post-deposition treatments are also studied and optimized.

5.2. **Experiments**

On silicon wafers coated with 400 nm field SiO_2, bottom TaN electrodes (150 nm thick) were sputtered from a Ta target in an Ar and N_2 ambient. For MIM capacitors with single layer dielectric, Er_2O_3 or HfO_2 (80 nm thick) was sputtered from Er or Hf targets, respectively in an O_2 and Ar ambient. For MIM capacitors with stacked dielectrics of Er_2O_3 on SiO_2, SiO_2 was deposited by ALD at 400 °C (thickness: 5.5 nm), ALD at 200 °C (thickness: 4.3 nm), and PECVD (thickness: 8 nm), followed by the sputtering of 30 to 60 nm of Er_2O_3. The sputtering rates of TaN, Er_2O_3 and HfO_2 were approximately 12, 16, and 7 nm/min, respectively. The MIM capacitors with single layer dielectric and with stacked dielectrics of Er_2O_3 on ALD and PECVD SiO_2 were subjected to post-deposition treatments with the conditions as listed in Table 5-1, 5-2, and 5-3, respectively. The top TaN electrode (150 nm thick) was then sputtered. Lithography and dry etching of top TaN electrode was carried out to define the top electrode regions. The capacitances and leakage currents of the MIM capacitors were measured by an HP4284A precision LCR meter and an HP4155B semiconductor parameter analyzer, respectively. The maximum operation voltage of the HP4155B semiconductor parameter analyzer is ±20 V.

Table 5-1: The anneal conditions for the MIM capacitors with single layer Er_2O_3 and HfO_2 dielectric. The temperature and the amount of O_2 in the chamber were varied. The anneal time was 2 minutes.

Split	High-K	Temperature (°C)	Gas flow	Notation
H1	HfO_2 (80nm)	no anneal		
H2		300	5% O_2	300_5%
H3		350	RTO	350_RTO
H4		400	Residue O_2	400_RO_2
H5		400	5% O_2	400_5%
H6		400	RTO	400_RTO
E1	Er_2O_3 (80nm)	No anneal		
E2		400	Residue O_2	400_RO_2
E3		400	5% O_2	400_5%
E4		400	RTO	400_RTO
Residue O_2: O_2 is flown and then turn off prior to the anneal 5% O_2 :75 sccm O_2, 1500 sccm N_2 during anneal RTO: Rapid thermal oxidation, 1500 sccm O_2, no N_2				

5.3. **MIM capacitors with single layer dielectrics**

The MIM capacitors with single layer 80 nm Er_2O_3 and HfO_2 dielectrics were treated with different post-deposition anneals (PDA) as listed in Table 5-1. The temperature and amount of oxygen (O_2) flown in the chamber were varied. The normalized capacitance density $\Delta C/C_0 = (C-C_0)/C_0 = \beta V+\alpha V^2$ measured at 100 kHz for selected MIM capacitors with Er_2O_3 and HfO_2 dielectrics are shown in Fig. 5-1. The dissipation factors ($\tan\delta$) for all the measurements were less than 0.01, and thus

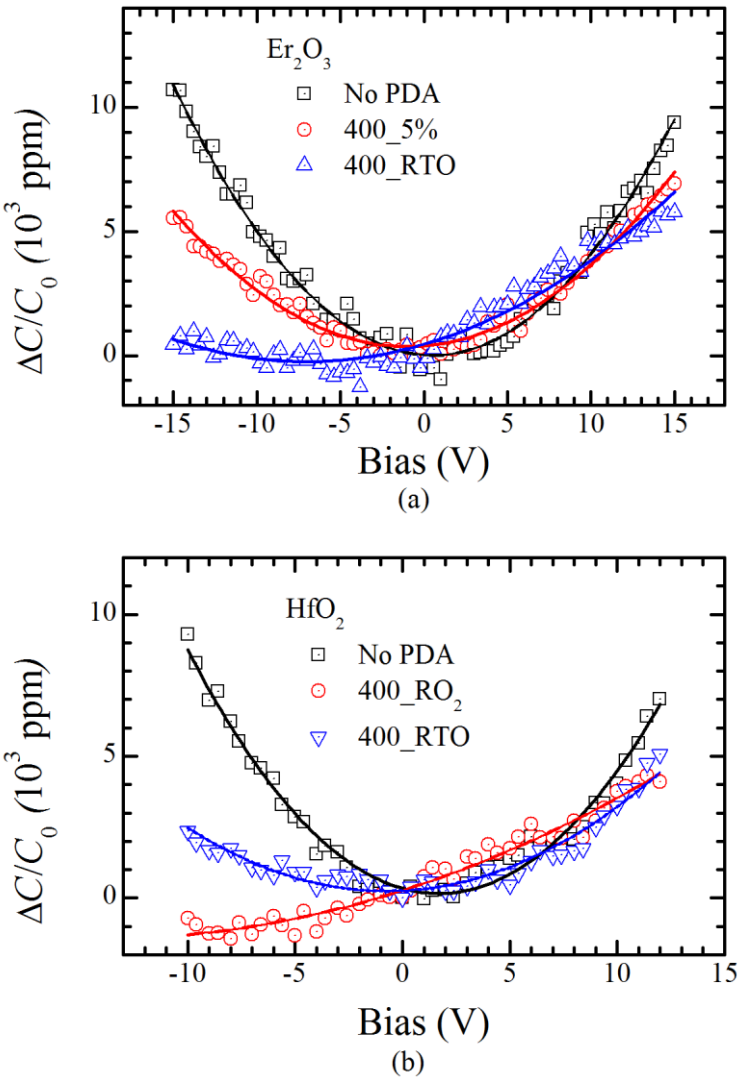

Fig. 5-1: The normalized capacitance density versus bias of (a) Er_2O_3 and (b) HfO_2 MIM capacitors are fitted with quadratic equations.

the Q (quality) factors were higher than 100. The quadratic VCCs of the samples are positive, and they varied with the post-deposition anneal conditions. The origin of the positive quadratic VCC can be explained by an ionic polarization model: displacements of metal cations in the dielectric from their equilibrium positions under an electric field generates field depending dipoles [5]; or by an electrostriction model: the induced strain in the dielectric under an electric field causes the deformation of the dielectric [6].

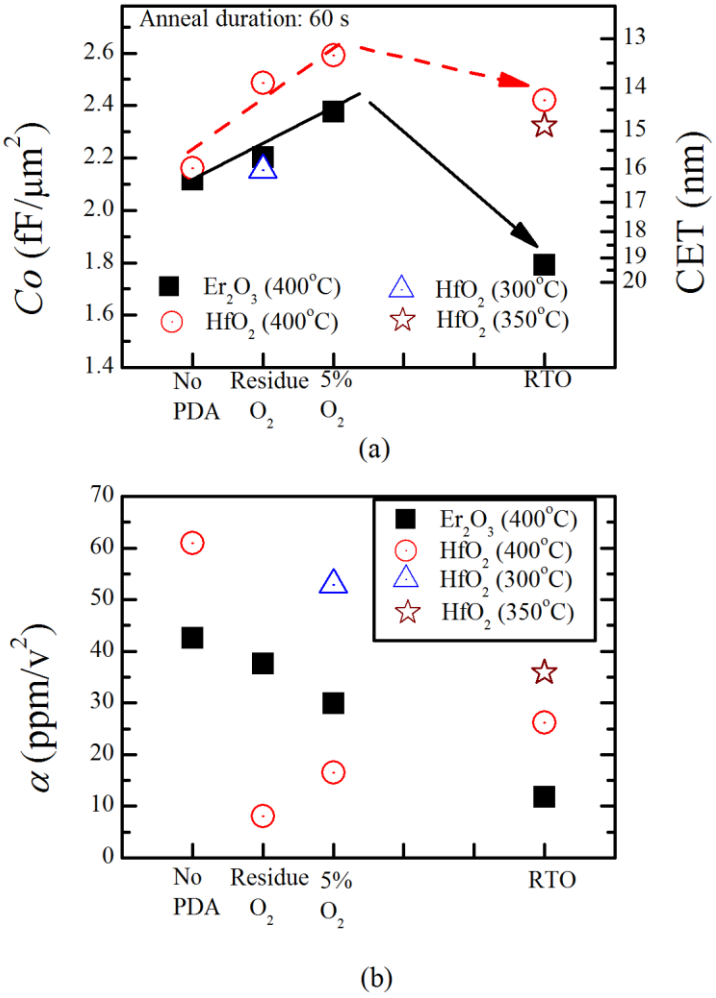

Fig. 5-2: (a) Capacitance density with corresponding CET and (b) quadratic VCC (α) of the Er_2O_3 and HfO_2 MIM capacitors treated with different anneal conditions. The x-axis shows the anneal conditions with increasing O_2 content present during the anneal.

The extracted C_0 and α values for different PDA conditions are shown in Fig. 5-2. The linear VCC (β) was not included because it can be compensated by circuit design [7]. The equivalent capacitance (silicon) oxide thickness (CET) was calculated as $3.9\varepsilon_0/C_0$, where ε_0 is the permittivity of vacuum. As shown in Fig. 5-2, by increasing the O_2 concentration during the PDA, the capacitance densities of the MIM capacitors increase to maximum values, after which they drop. The MIM capacitors with as-deposited Er_2O_3 and HfO_2 (without any PDA) have similar capacitance densities. However, when they are subjected to a PDA, the MIM capacitors with HfO_2

dielectric have higher capacitance densities and smaller CETs than the MIM capacitors with Er_2O_3. From the C_0 values, the dielectric constants of the as-deposited HfO_2 and Er_2O_3 are approximately 19.5 and 19.1, respectively. When subjected to the 400 °C_5% O_2 PDA, the dielectric constants of HfO_2 and Er_2O_3 increased to 23.4 and 21.5, respectively. The dielectric constants of HfO_2 and Er_2O_3 are consistent with previously reported values of 16-25 [8-11] and those obtained in chapter 4, respectively. The large increase in HfO_2 dielectric constant could be due the crystallization of HfO_2 after the PDA, which occur at a temperature as low as 400 °C [12]. The MIM capacitors with HfO_2 subjected to a 300_5% PDA shows no increment in the capacitance density as compared to the capacitor with the as-deposited HfO_2, suggesting that HfO_2 was still amorphous after the 300 °C PDA. Similarly, by comparing the HfO_2 MIM capacitors subjected to an RTO at 350 °C to that at 400 °C, it is seen that the capacitance density of the former is lower, due to the lower anneal temperature. The drop in the capacitance density after the RTO was believed to be due to the oxidation of TaN and thus a thin oxide layer formed at the interface between the dielectrics and the bottom TaN electrode.

Fig. 5-2 (b) shows that the PDA reduces the quadratic VCC of both HfO_2 and Er_2O_3. By the ionic polarization model [5], the PDA strengthens the bonds between the metal cations (Hf and Er) and the O atoms, and thus the displacements of Hf and Er under an electric field is smaller. Using the electrostriction model [6], the stronger bonds in the dielectrics reduce their deformation under an electric field. In certain samples, the α values are as low as 8 ppm/V^2. For the MIM capacitors with Er_2O_3 dielectric, the PDA with a higher concentration of O_2 reduces the quadratic VCC of the capacitors. The trend for HfO_2 is however not obvious.

The quadratic VCCs (α) of the MIM capacitors for different capacitance densities C_0 for Er_2O_3 and HfO_2 dielectrics are shown in Fig. 5-3, in which the α values decrease with capacitance densities due to different annealing conditions. This trend is different from those reported on other high-k dielectrics such as Al_2O_3 [5], Sm_2O_3 [13], TiZrO [14] and HfLaO [15], in which the quadratic VCC increases with capacitance density due to different film thickness. Fig. 5-3 demonstrates that by optimizing the post-deposition annealing process, it is possible to increase the capacitance density and reduce the quadratic VCC at the same time.

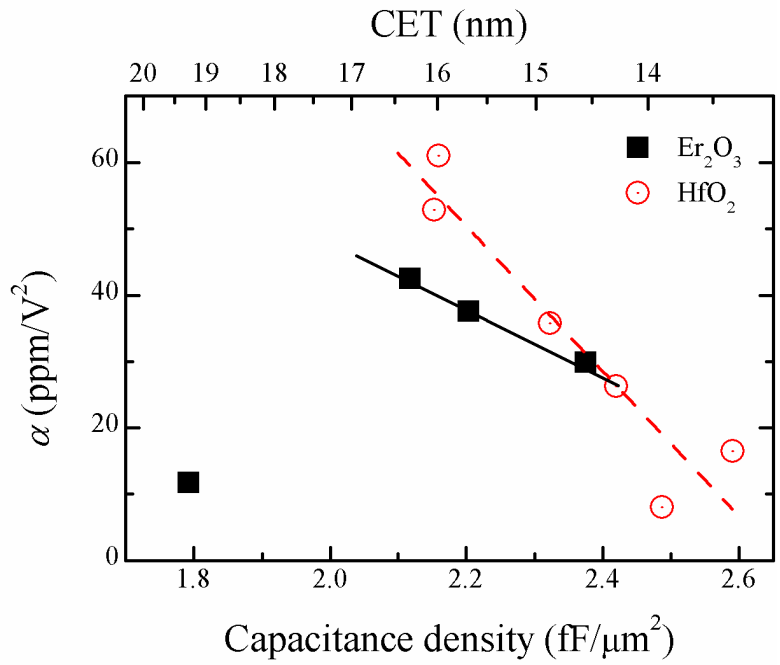

Fig. 5-3: Quadratic VCCs for different capacitance densities of Er_2O_3 and HfO_2 MIM capacitors. The α values decrease with capacitance densities due to different annealing conditions.

The leakage currents through Er_2O_3 and HfO_2 with applied bias swept from -20 to 20 V (the limit of the HP4155B semiconductor parameter analyzer) are shown in Fig. 5-4 (a) and (b), respectively. The dielectrics do not breakdown at bias ±20 V, suggesting that the field strengths of the PVD HfO_2 and Er_2O_3 are higher than 2.5

MV/cm. It is seen from Fig. 5-4 that the PDA improves the leakage performance of the MIM capacitors for both Er_2O_3 and HfO_2. The MIM capacitors subjected to the 400_5% PDA have the lowest leakage currents, and their leakage currents at ± 20 V applied bias are in the order of 10^{-5} A/cm^2. With the 400_5% PDA, the leakage currents of the Er_2O_3 MIM capacitor is lower than that of the HfO_2 MIM capacitor.

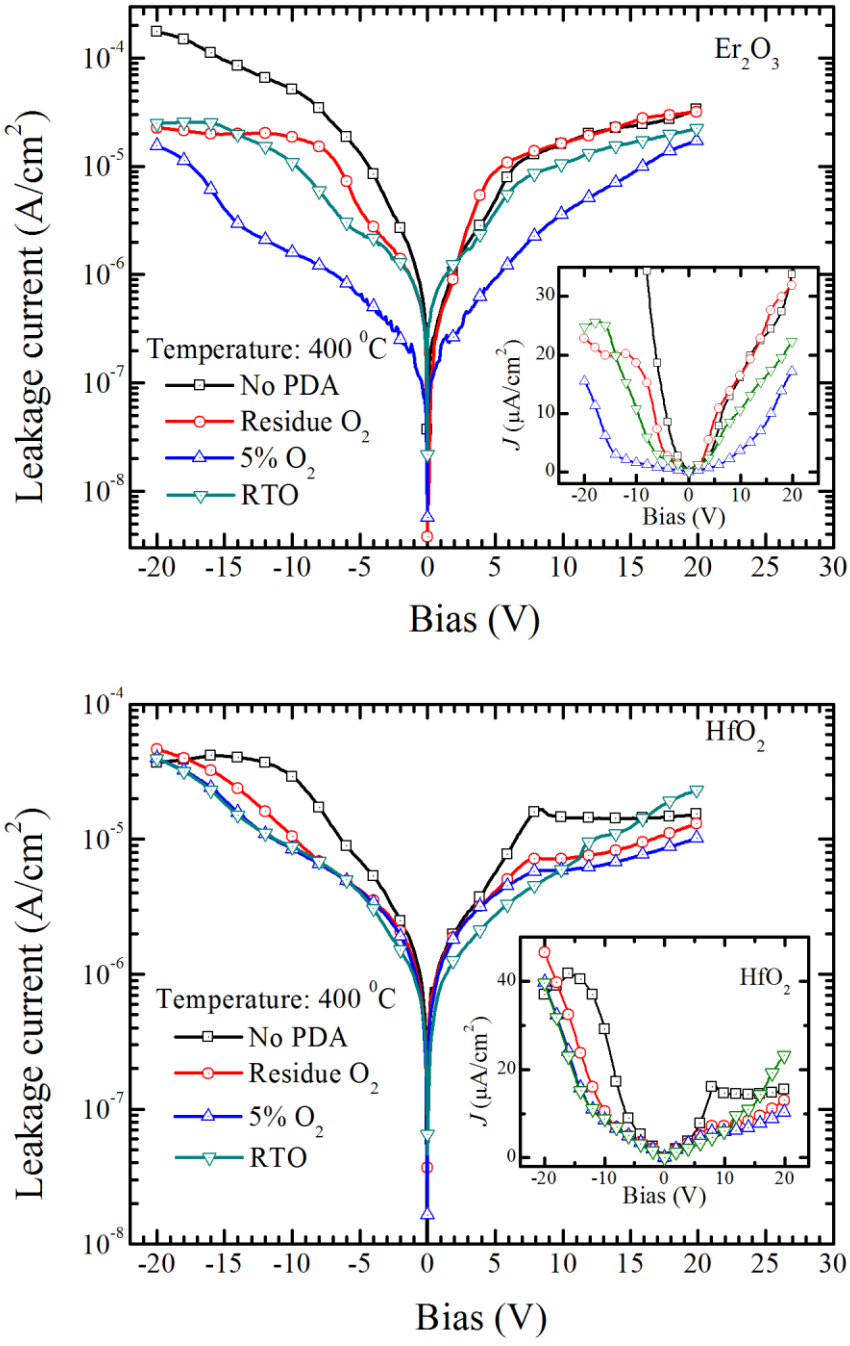

Fig. 5-4: Leakage currents through 80 nm Er_2O_3 and HfO_2 dielectrics subjected to various post-deposition anneal.

From the insets of Fig. 5-4, several negative resistance regions are observed in the leakage current against bias plots, especially in the MIM capacitor with HfO_2 dielectric. The negative resistance which was also observed in Al_2O_3 by Gomez *et. al.* [16] is due to the potential well of electron in the dielectrics, which screens the tunneling electrons and causes a reduction in the leakage current. The negative resistance starts to occur at positive bias of about 7 V for HfO_2 MIM capacitors.

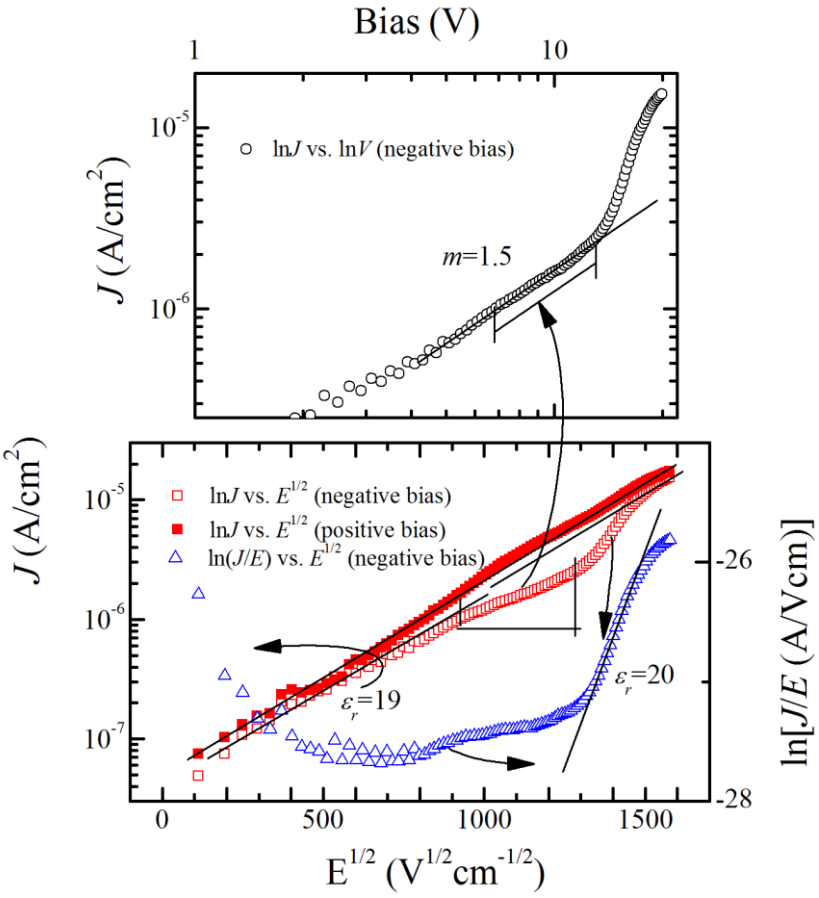

Fig. 5-5: log$J$ versus log$V$, log$J$ versus $E^{1/2}$ and ln$J$/E versus $E^{1/2}$ for the MIM capacitor with 80 nm Er_2O_3 dielectric subjected to the 60 second 400 °C 5% O_2 PDA.

The leakage current of the MIM capacitor with Er_2O_3 subjected to the 400_5% PDA is the lowest among those of the MIM capacitors with Er_2O_3 dielectrics, and is used for a conduction mechanism study. The leakage currents are converted to log$J$ versus log$V$, log$J$ versus $E^{1/2}$ and ln(J/E) versus $E^{1/2}$ as shown in Fig. 5-5 to determine

if the conduction mechanism is space-charge limited (SCL), Schottky emission or Poole-Frenkel (P-F) emission. From the plot ln$J$ versus $E^{1/2}$, it is seen that Schottky emission is the dominant conduction mechanism for positive bias from 0 to 20 V, corresponding to an electric field of 0-2.5 MV/cm. The dielectric constant extracted from the slope of the fitted straight line using the Schottky emission equation is about 19, which is close to the value derived from the measured capacitance densities. This further confirms that the conduction mechanisms for the observed linear regions were Schottky emission. For the negative bias, Schottky emission is observed at electric field 0-0.8 MV/cm, as seen by the linear region in the log$J$ versus $E^{1/2}$ plot which slope is similar to that of the positive bias. For electric field from 0.8-1.8 MV/cm, the region in ln$J$ versus $E^{1/2}$ plot may be fitted to a straight line, however the dielectric constant derived from this slope is ~40, about twice the dielectric constant of Er_2O_3. Moreover, a linear region is observed in the log$J$ versus log$V$ plot (corresponding to space charge limited conduction) for this electric field range with a slope of m = 1.5, same as the slope predicted by Child-Langmuir law (m = 1.5) [17-18] and close to the value predicted by Mott-Gurney Law (m = 2) [19] for the SCL conduction. Thus it is deduced that the space charge limited conduction is responsible for E = 0.8-1.8 MV/cm. For E = 1.8-2.3 MV/cm, when ln(J/E) is plotted against $E^{1/2}$, a linear region is observed suggesting that Poole-Frenkel emission is responsible for the sharp increase in leakage current. Furthermore, the dielectric constants obtained from the slope of the linear region using the P-F emission equation [Eq. (3-3)] is about 20, which is consistent with the dielectric constant of Er_2O_3. For E = 2.3-2.5 MV/cm, the mechanism appears to be Schottky emission again, as seen from the log$J$ versus $E^{1/2}$ plot.

The conduction mechanisms through Er_2O_3 at different negative bias are illustrated in Fig. 5-6. As the electric field increased (for negative bias), electrons were emitted by thermionic (Schottky) emission and flow through the dielectrics. Some of the electrons were trapped inside the dielectrics, building up a space charge region which limited the conduction. At higher electric field, Poole-Frenkel emission then occurred where the trapped electrons inside Er_2O_3 were emitted from the dielectric into the conduction band. After most of the electrons were de-trapped, the conduction became Schottky emission again.

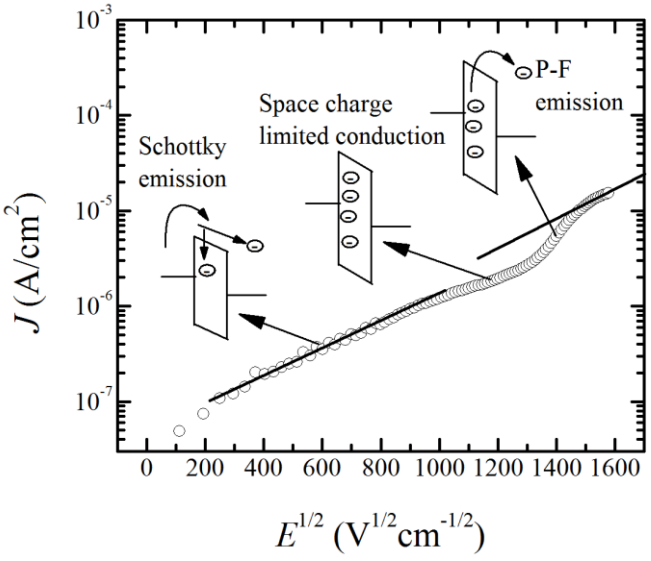

Fig. 5-6: Illustration of the conduction mechanisms through the Er_2O_3 MIM capacitor subjected to the 400 °C_5% O_2 PDA.

The leakage currents through HfO_2 with 400_5% PDA were also used for conduction mechanism analysis, as shown in Fig. 5-7. As seen from the top inset, the plots of log$J$ versus log$V$ for low positive and negative biases $0 < |V| < 4$ V can be fitted with straight lines with slopes of 0.73 and 0.8, respectively, which are closed to the slope of 1 for bulk conduction following Ohm's law. For the bias of $|V| = 4$-8 V, the conduction mechanism changed to Schottky emission, as seen by the linear region

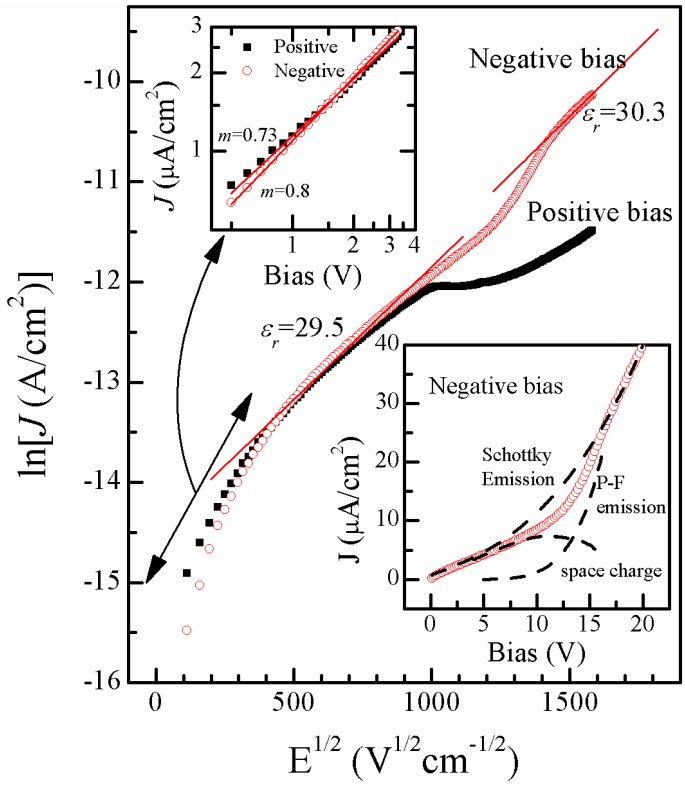

Fig. 5-7: ln$J$ versus $E^{1/2}$ for MIM capacitor with HfO_2 subjected to the 400 °C 5% O2 PDA. Top inset: J versus bias in log-log scale for low bias. The linear regions have slopes near to 1, indicating that Ohmic conduction is responsible. Bottom inset: J versus bias plot in linear scale, with illustrated conduction mechanisms at different biases.

in the ln$J$ versus $E^{1/2}$ plot. The extracted dielectric constant from the slope is about 29, close to the actual value of HfO_2. For the bias $|V| > 8$ V, the slopes of both negative and positive bias reduce, which as discussed earlier is the effect of the space charge region created by the trapped electrons in the dielectric. At higher electric field, the trapped electrons were released from the dielectric by P-F emission. The bottom inset of Fig. 5-7 illustrates the changes in the conduction mechanisms for the negative bias. The leakage current at high and low bias can be predicted by the Schottky emission curve. However, at a medium bias, the actual leakage current is smaller than the one predicted by the Schottky emission due to the formation of a space charge layer and the P-F emission.

5.4. **Stacked Er_2O_3 on SiO_2**

The MIM capacitors with single layer Er_2O_3 and HfO_2 have low quadratic VCCs and high capacitance densities for high voltage applications; however their leakage currents are still considerably high, in the order of 10^{-5}-10^{-4} A/cm^2 at 20 V. As such in this section, the Er_2O_3 layers with thicknesses from 30-60 nm were stacked on SiO_2 [8 nm PECVD SiO_2, 4.3 nm ALD SiO_2 (deposited at 200 °C), and 5.5 nm ALD SiO_2 (deposited at 400 °C)] to investigate if the leakage currents can be reduced. The thicknesses of SiO_2 were determined from the capacitance densities of the SiO_2 MIM capacitors using the relation: $d_{CET}=3.9\varepsilon_0/C$. The post-deposition treatments for the stacks with PECVD and ALD SiO_2 are listed in Table 5.2 and 5.3, respectively.

5.4.1 **Er_2O_3 on PECVD SiO_2**

In this sub-experiment, the thicknesses of the Er_2O_3 layers on 8 nm PECVD SiO_2 were varied from 30 to 60 nm, and the stacked dielectrics were subjected to several post-deposition treatments: a post-deposition anneal at 400 °C for 2 mins with 5% O_2 flow (PDA); an N_2 plasma treatment after the SiO_2 deposition following by a PDA after the Er_2O_3 deposition; dual N_2 plasma treatment after the SiO_2 and Er_2O_3 depositions following by a PDA; and lastly without any treatment (Table 5-2). The normalized capacitance densities of the MIM capacitors without any treatment are shown in Fig. 5-8 (a), showing the effect of Er_2O_3 thicknesses on the quadratic VCC. The normalized capacitance densities of the MIM capacitors with 30 nm Er_2O_3 on 8 nm SiO_2 stacked dielectrics subjected to different treatments are shown in Fig. 5-8 (b). The capacitance measurement was performed at frequency 100 kHz.

Table 5-2: Anneal conditions for the MIM capacitors with stacked dielectrics of Er_2O_3 on 8 nm PECVD SiO_2.

Split	Anneal	Er_2O_3 (nm)
1	No anneal	30
2		45
3		60
4	400C, 5% O_2, 2 mins (PDA)	30
5		45
6		60
7	N_2 plasma 5 mins after SiO_2 deposition + PDA	30
8		45
9		60
10	N_2 plasma 5 mins after SiO_2 and HfO_2 deposition + PDA	30
11		45
12		60

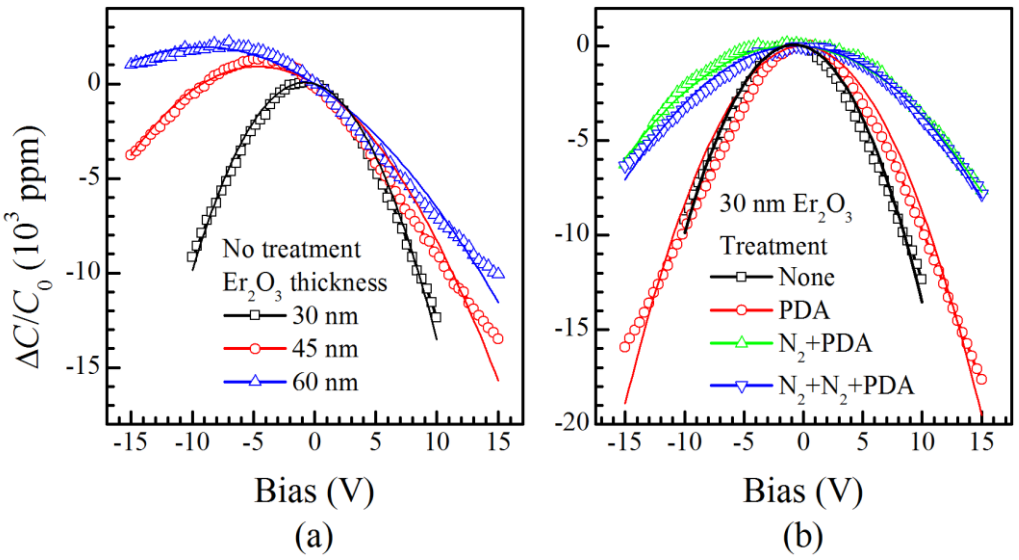

Fig. 5-8: Normalized capacitance densities of the MIM capacitors with Er_2O_3 on 8 nm PECVD SiO_2 stacked dielectrics: (a) No post-deposition treatment was applied and the thickness of Er_2O_3 layer was varied; and (b) the thickness of Er_2O_3 layer was 30 nm, and the treatment condition was varied.

The values of C_0 and α measured at 100 kHz for the MIM capacitors with different post-deposition treatments are shown in Fig. 5-9 (a) and (b), respectively. The PDA increases the capacitance densities while both of the N_2 plasma treatments (single and dual) reduce the capacitance densities of the MIM capacitors, as compared to the one without any treatment. The PDA and N_2 treatments however reduce the quadratic VCCs (absolute values) of the capacitors. The reductions are larger in the capacitors with thinner Er_2O_3 and with N_2 plasma treatment. The stacked dielectric subjected to the N_2 plasma treatment has smaller quadratic VCC change with thickness than those with PDA and without treatment.

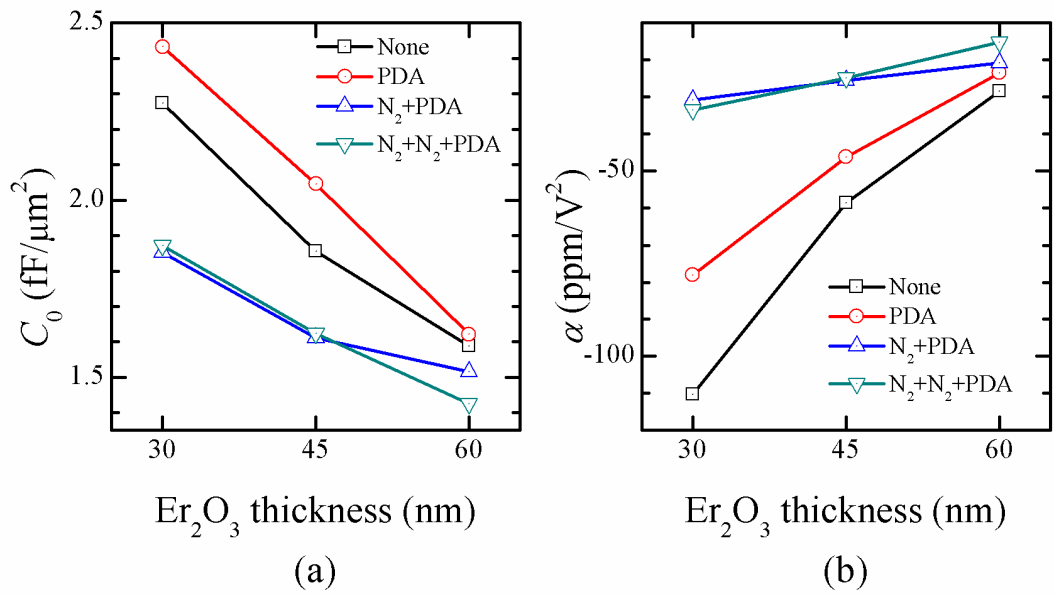

Fig. 5-9: (a) The capacitance densities and (b) quadratic VCCs of the MIM capacitors with stacked dielectrics of Er_2O_3 on 8 nm PECVD SiO_2 with different post-deposition treatments.

The leakage currents at -20 V of the MIM capacitors are shown in Fig. 5-10. There is no observed thickness dependent for the leakage currents, possibly because there is a large amount of defects in the sputtered Er_2O_3 and PECVD SiO_2 layers. The capacitors with PDA and N_2 plasma treatment have smaller leakage currents than the

one without any treatment. The leakage currents at -20 V through the stacked dielectrics are in the order of 10^{-5} to 10^{-4} A/cm^2, which are similar to the leakage currents of MIM capacitors with single layer Er_2O_3 and HfO_2.

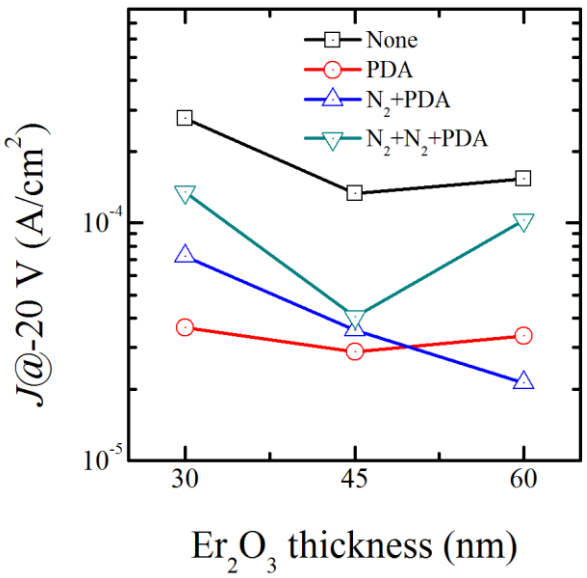

Fig. 5-10: Leakage currents at -20 V of the MIM capacitors with stacked dielectrics of Er_2O_3 on 8 nm PECVD SiO_2.

5.4.2 Er_2O_3 on low temperature (200 °C) ALD SiO_2

The capacitance performance of the MIM capacitors with the stacked dielectrics of Er_2O_3 with varied thickness on 4.3 nm SiO_2 (SiO_2 formed by ALD at 200 °C) is shown in Fig. 5-11. The capacitors were annealed at 400 °C for 2 mins with 5% O_2 flow (Table 5-3). The normalized capacitance density in Fig. 5-11 (a) shown that as the thickness of Er_2O_3 changes from 30 to 60 nm, the quadratic VCC reduced from a positive to a negative value. The capacitance densities of the MIM capacitors having Er_2O_3 thicknesses of 30 nm, 45 nm and 60 nm are 3.49, 2.63 and 2.15 fF/µm^2, respectively and they are fairly constant over the measured frequency range [Fig. 5-11 (b)]. These densities are slightly higher than the one achieved by

Table 5-3: Anneal conditions of the MIM capacitors with stacked dielectrics of Er_2O_3 on 5.5 nm SiO_2 ALD at 400 °C and 4.3 nm SiO_2 ALD at 200 °C. The anneal time and temperature was 2 minutes and 400 °C, respectively. The O_2 gas flow rates during the anneal denoted by 5% O_2 and 20% O_2 are 75 sccm and 300 sccm, respectively while the N_2 gas flow rate is a constant 1500 sccm.

Split	PDA	ALD SiO_2	Er_2O_3 (nm)
1	400 °C 5% O_2	5.5 nm (400 °C)	30
2			45
3			60
4	None		60
5	400 °C 20% O_2		60
6	400 °C 5% O_2	4.3 nm (200 °C)	30
7			45
8			60

Er_2O_3 on 8 nm PECVD SiO_2 presented earlier due to thinner SiO_2 used. The extracted dielectric constants of Er_2O_3 are in the range of 19.5-20.5, consistent with other values obtained earlier. The quadratic VCCs of the stacked dielectrics with 30 nm and 60 nm Er_2O_3 are positive and negative, respectively for the whole frequency range, however, the quadratic VCC of the stack with 45 nm Er_2O_3 changes from positive to negative as the frequency increases, with very low α values of 2.4 and -13 ppm/V^2 at frequency 50 and 100 kHz, respectively.

The leakage currents of the MIM capacitors with the stacked dielectrics with negative bias are generally smaller than those with positive bias, as shown in Fig. 5-12. The capacitor with 30 nm Er_2O_3 however breaks down at -18 V while the capacitors with 45 and 60 nm Er_2O_3 do not breakdown at ±20 V, indicating that the

dielectric field strengths of the latter 2 stacks are higher than 4 MV/cm. The leakage current at -20 V of the stack with 45 nm and 60 nm Er_2O_3 are 9.4 and 2.3 μA/cm^2, respectively.

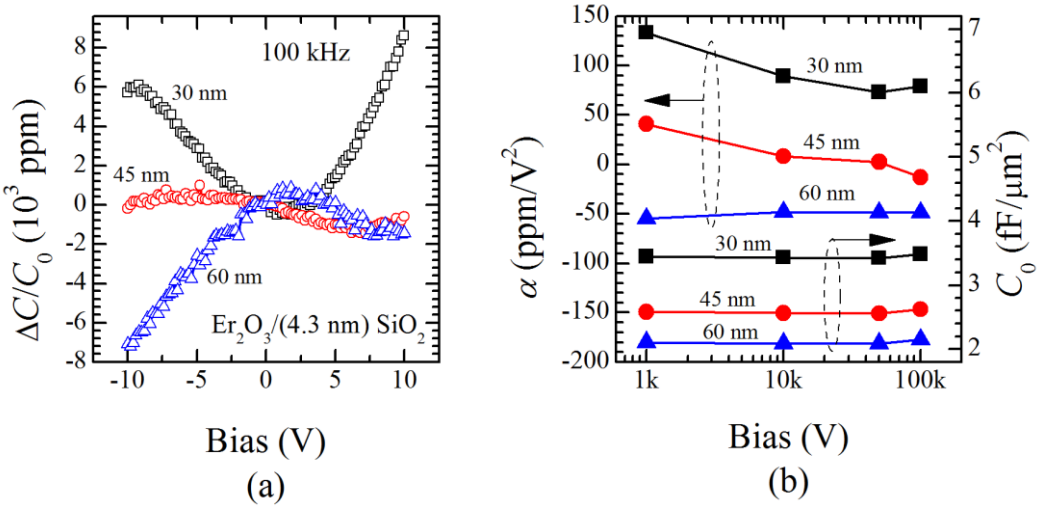

Fig. 5-11: (a) $\Delta C/C_0$ and (b) the frequency dependent quadratic VCC α and capacitance densities C_0 for MIM capacitors with the stacked dielectrics of Er_2O_3 with varied thicknesses on 4.3 nm SiO_2. SiO_2 was deposited by ALD at 200 °C.

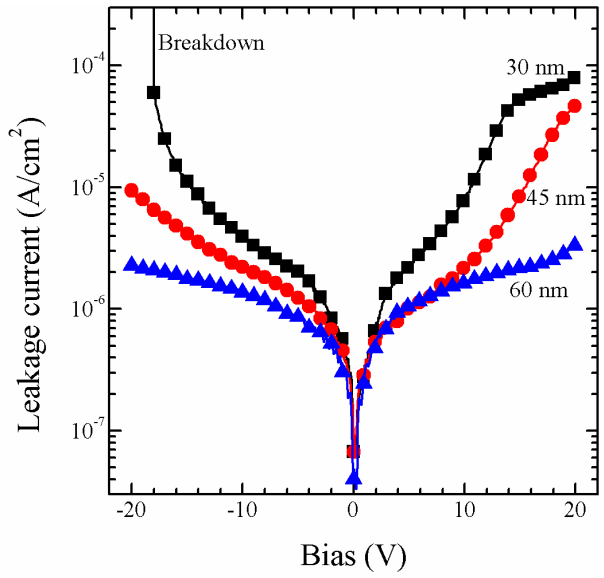

Fig. 5-12: Leakage currents of the MIM capacitors with the stacked dielectrics of Er_2O_3 with varied thicknesses on 4.3 nm SiO_2. SiO_2 was deposited by ALD at 200 °C.

5.4.3 Er_2O_3 on high temperature (400 °C) ALD SiO_2

The normalized capacitance densities of the MIM capacitors with Er_2O_3 on 5.5 nm ALD SiO_2 (400 °C) stacked dielectrics are shown in Fig. 5-13, from which the quadratic VCCs were extracted. In Fig. 5-13 (a) which the PDA condition was kept constant, the quadratic VCC becomes less negative as the thickness of Er_2O_3 increases. In Fig. 5-13 (b), the samples subjected to a PDA with 5% and 20% O_2 have similar capacitance densities and quadratic VCCs, both of which are less negative than that of the capacitor without PDA. The capacitance stays relatively constant over the frequency range, with a slight increase at 100 kHz as shown in Fig. 5-14. The dielectric constants of Er_2O_3 calculated from the capacitance densities are 19.5-21. From Fig. 5-14 (b), it is seen that the anneal conditions changed the capacitance densities by only ±0.05 fF/μm^2. The dissipation factors tanδ are smaller than 0.02 for all the samples measured, as shown in the inset of Fig. 5-14 (b), and thus the Q factors (= 1/tanδ) are all larger than 50.

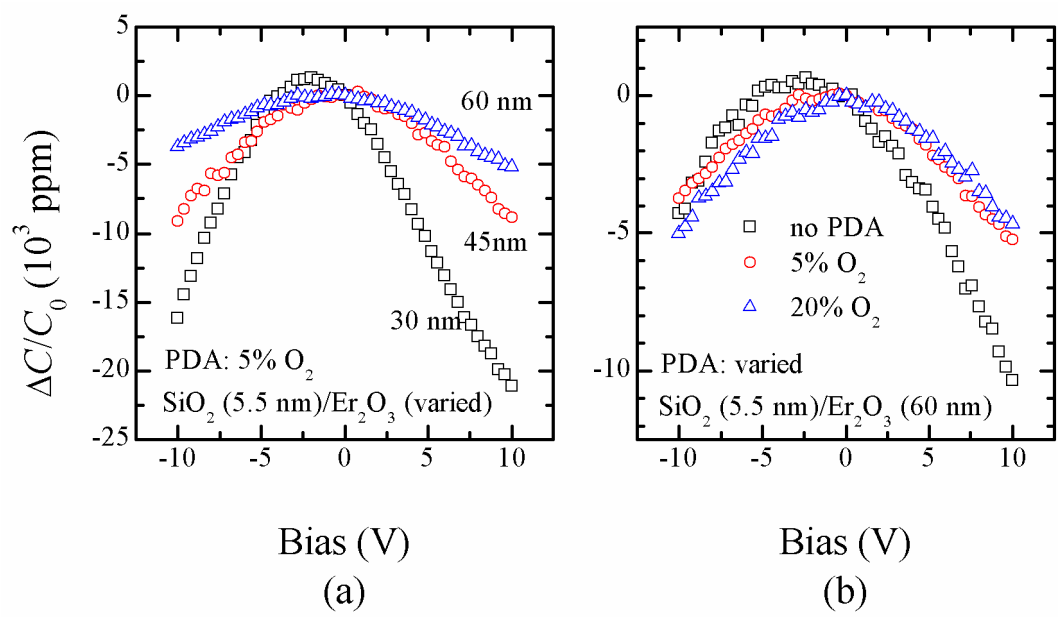

Fig. 5-13: Normalized capacitance densities of the MIM capacitors with stacked dielectrics: (a) The PDA condition was 400 °C, 2 mins, with 5% O_2 for all samples and the thickness of Er_2O_3 was varied. (b) Er_2O_3 thickness was fixed at 60 nm, and the PDA condition was varied.

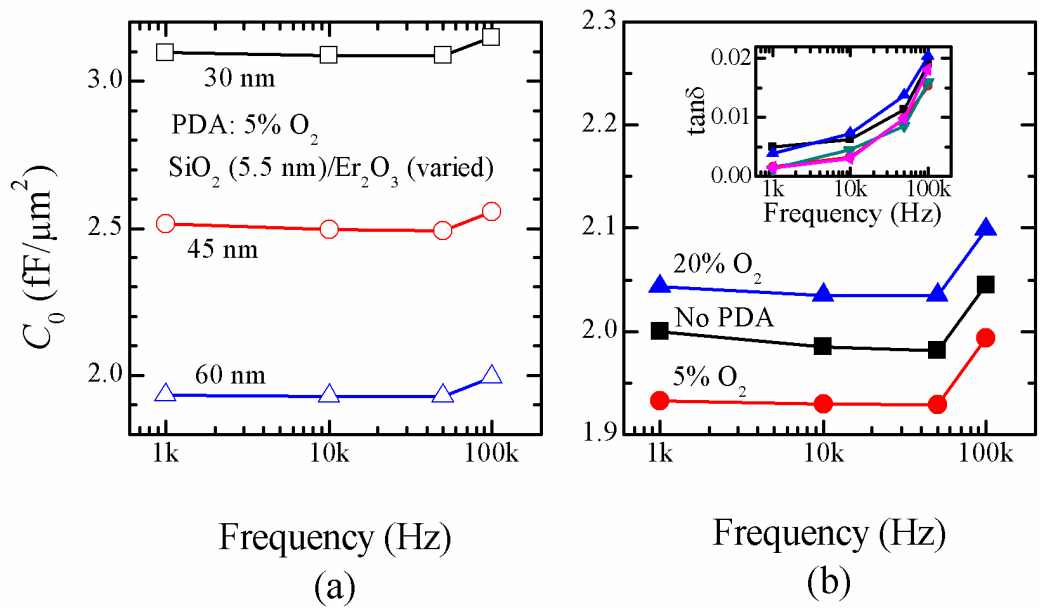

Fig. 5-14: The capacitance densities versus frequencies of the MIM capacitors with (a) varied Er_2O_3 thicknesses and (b) varied PDA conditions.

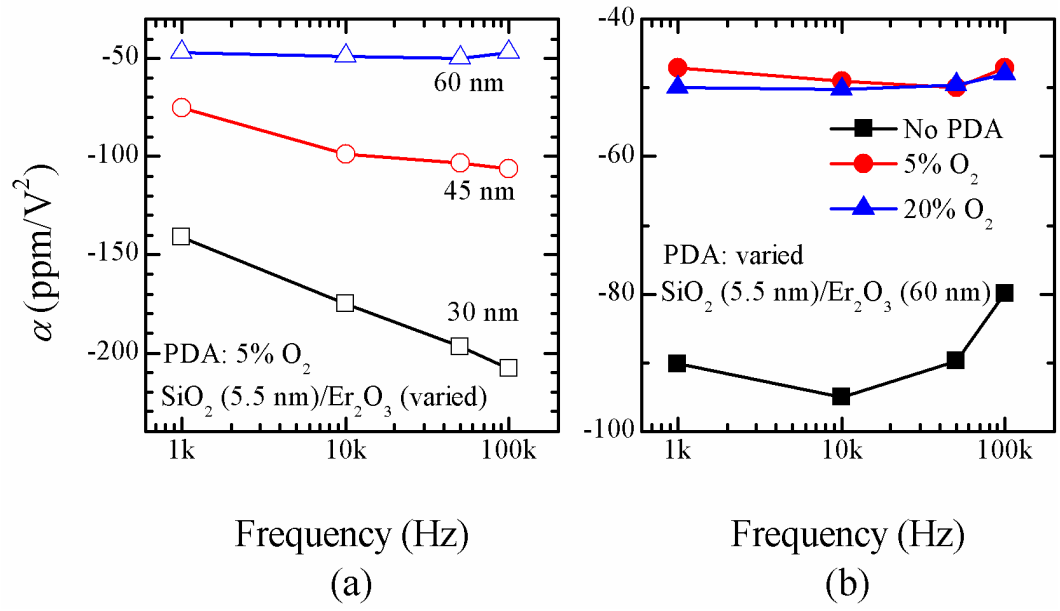

Fig. 5-15: The quadratic VCCs versus frequencies of the MIM capacitors with (a) varied Er_2O_3 thicknesses and (b) varied PDA conditions.

The frequency dependent quadratic VCC of the MIM capacitors with varied Er_2O_3 thicknesses in the stacked dielectrics and varied PDA conditions are shown in Fig. 5-15 (a) and (b), respectively. The MIM capacitor with thicker Er_2O_3 has smaller

frequency dispersion, as seen from Fig. 5-15 (a). The quadratic VCCs of SiO_2 (5.5 nm)/Er_2O_3 (60 nm) with PDA (5% O_2 and 20% O_2) stay relatively constant over the frequency range, at about -50 ppm/V^2 while the capacitor without PDA has quadratic VCC varying from -95 to -80 ppm/V^2. The negative quadratic VCCs of the stacked dielectrics indicate that the effect from the negative α of SiO_2 is stronger than that from the positive α of Er_2O_3.

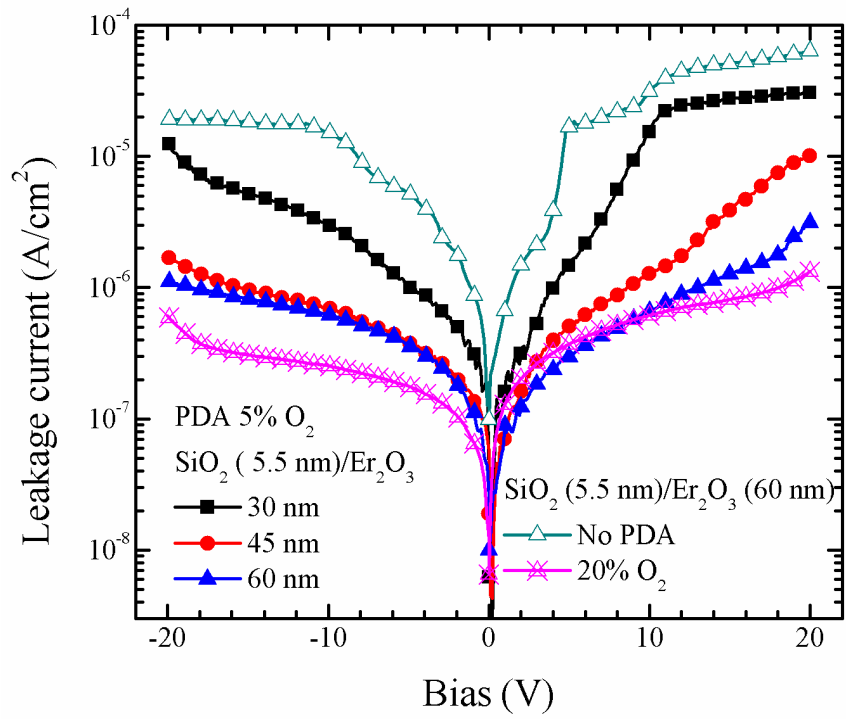

Fig. 5-16: Leakage currents of the MIM capacitors with Er_2O_3 on ALD SiO_2 stacked dielectrics having varied Er_2O_3 thicknesses and PDA conditions.

The leakage currents of the MIM capacitors with varied Er_2O_3 thicknesses and PDA conditions are shown in Fig. 5-16. The leakage currents with positive bias are higher than those with negative bias. When the same PDA condition (5% O_2) is applied, the MIM capacitor with thicker Er_2O_3 has smaller leakage currents. Among the MIM capacitors with stacked dielectrics of 60 nm Er_2O_3 on 5.5 nm SiO_2, the MIM capacitor without PDA has very high leakage current, and the slope of the I-V curve

changes abruptly, suggesting that there is large amount of defects inside the dielectrics. The MIM capacitor with 20% O_2 PDA has the lowest leakage current which the leakage current at -20 V is 6×10^{-7} A/cm^2. The PDA with 20% O_2 is more optimal than the one with 5% O_2 in passivating the defects in the dielectric.

5.5. **Summary**

The MIM capacitors with various dielectric structures were investigated for high voltage applications: single layer 80 nm Er_2O_3 and HfO_2, stacked dielectrics of Er_2O_3 (30-60 nm) on 8 nm PECVD SiO_2, 4.3 nm ALD SiO_2 (deposited at 200 °C) and 5.5 nm ALD SiO_2 (deposited at 400 °C). The summary of the quadratic VCCs and the leakage currents at -20 V against the capacitance densities of the MIM capacitors are shown in Fig. 5-17. The capacitance densities and the quadratic VCCs were greatly affected by the anneal temperature and the amount of O_2 present during the post-deposition anneal. By optimizing the anneal condition, increasing the capacitance density and reducing the quadratic VCC could be achieved concurrently in the MIM capacitors with single layer Er_2O_3 and HfO_2. Low quadratic VCC of 17 ppm/V^2 and high capacitance density of 2.6 fF/μm^2 was achieved by the capacitor with 80 nm HfO_2, however the leakage current at -20 V was still considerably high (4×10^{-5} A/cm^2 at -20 V).

For the stacked dielectrics of Er_2O_3 on SiO_2, the quadratic VCC is less negative (increases) with increasing Er_2O_3 thicknesses in the stacked on 5.5 nm ALD SiO_2 (deposited at 400 °C) and 8 nm PECVD. The trend is however opposite for the stack on 4.3 nm ALD SiO_2 (deposited at 200 °C): the quadratic VCC changes from positive to negative (reduces) when the thickness of Er_2O_3 is increased. Due to the thick SiO_2 (5.5 nm by ALD at 400 °C and 8 nm by PECVD), the stacked dielectrics

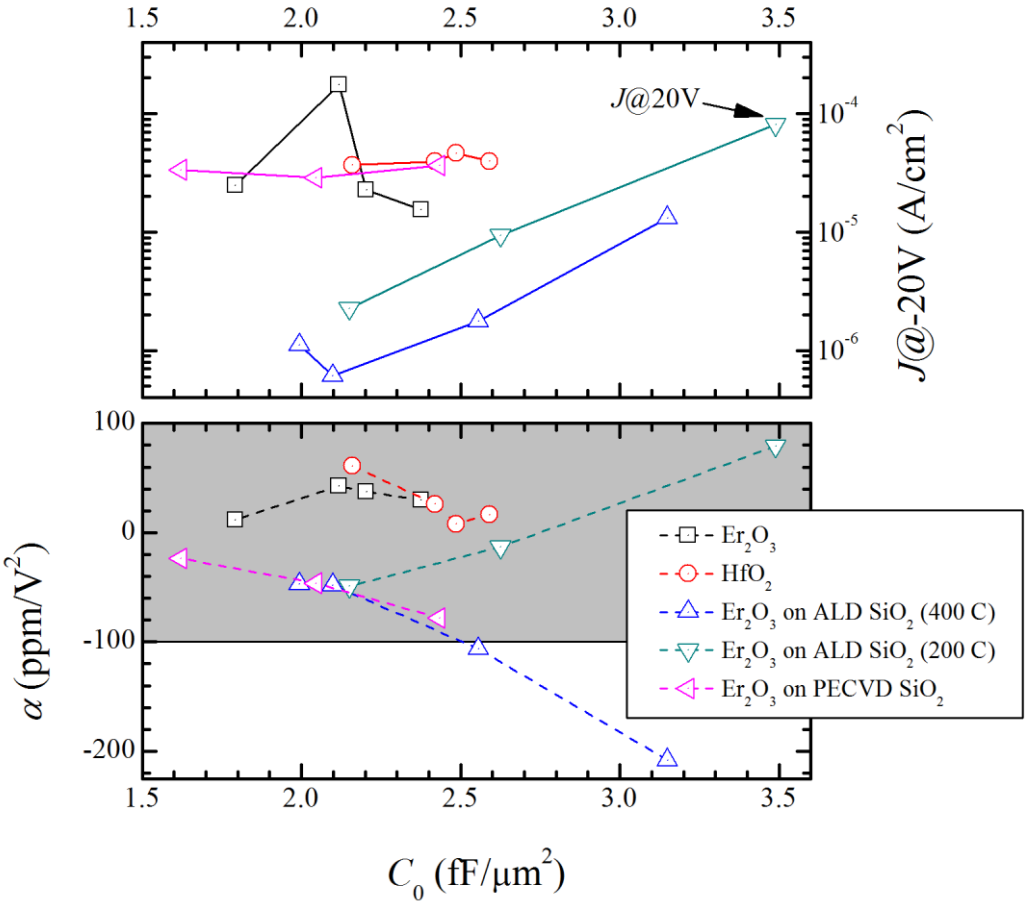

Fig. 5-17: The leakage currents and quadratic VCCs (α) against the capacitance densities (C_0) of the MIM capacitors using various dielectric structures: single layer Er_2O_3 and HfO_2, stacked dielectrics of Er_2O_3 on 5.5 nm ALD SiO_2 (deposited at 400 °C), 4.3 nm ALD SiO_2 (deposited at 200 °C) and 8 nm PECVD SiO_2.

appear to be SiO_2-like: α is more negative with larger C_0. For Er_2O_3 on 4.3 nm ALD SiO_2 (deposited at 200 °C), due to a thinner SiO_2 layer, the stacked dielectrics are Er_2O_3-like: α is more positive with larger C_0. A low quadratic VCC of -13 ppm/V^2, high capacitance density of 2.62 fF/μm^2 and a leakage current at -20 V of 9.4×10^{-6} A/cm^2 was achieved with 45 nm Er_2O_3 stacking on 4.3 nm ALD SiO_2 (deposited at 200 °C).

The leakage currents of MIM capacitors with the stacked dielectrics of Er_2O_3 on ALD SiO_2 (400 °C) are the lowest among the structures studied in this chapter. To

achieve a capacitance density of about 2.1 fF/μm^2, the leakage current at -20 V of the MIM capacitor with the stacked dielectrics of 60 nm Er_2O_3 on 5.5 nm ALD SiO_2 (400 °C) is 6×10^{-7} A/cm^2 which are about 4 and 50 times smaller than the leakage currents in the stacks of Er_2O_3 on 4.3 nm ALD SiO_2 (deposited at 200 °C) and 8 nm PECVD SiO_2, respectively. The grey box in Fig. 5-17 indicates the region where the quadratic VCC $|\alpha|$ is less than 100 ppm/V^2 required for the RF applications. The structure with optimized performance is the stacked dielectrics of Er_2O_3 (about 45 nm thick) on 5.5 nm ALD SiO_2 (400 °C), yielding a capacitance density of ~2.5 fF/μm^2, a quadratic VCC of -100 ppm/V^2 and a leakage current at -20 V of ~ 1×10^{-6} A/cm^2. With low quadratic VCCs, the demonstrated capacitance densities in this work are much higher than 0.5-1 fF/μm^2 obtained by Si_3N_4 MIM capacitors, indicating that the Er_2O_3 and HfO_2 single layer and Er_2O_3/SiO_2 stacked dielectrics are the potential materials to be used in the MIM capacitors for high capacitance density, high voltage applications.

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Chapter 6

Conclusions and Future Works

6.1. Conclusions

High capacitance density MIM capacitors for RF applications using different dielectric structures were investigated in this thesis: single layer PECVD (plasma-enhanced chemical vapor deposition) and ALD (atomic layer deposition) SiO_2, single layer Er_2O_3, stacked dielectrics of Er_2O_3 on ALD SiO_2. Moreover, high precision MIM capacitors for high voltage applications using HfO_2, Er_2O_3 single layer and Er_2O_3/SiO_2 stacked dielectrics were also studied. An MIM capacitor with a quadratic VCC less than 100 ppm/V^2, leakage current of 10^{-8} A/cm^2 at 3.3 V and capacitance density of 7 fF/μm^2 was demonstrated. The conclusions of the individual chapter are presented.

6.1.1 Silicon dioxide (SiO_2) for MIM applications

The MIM capacitors using SiO_2 dielectric deposited by PECVD and ALD method were extensive studied. The quadratic VCC of SiO_2 was negative, and was believed to be caused by the orientation polarization in SiO_2. An equation based on

the orientation polarization of dipole moments in SiO_2 and their concentration was successfully derived and it fitted the measured normalized capacitance density versus electric field across SiO_2 excellently. The ALD SiO_2 was demonstrated to have lower leakage currents and higher electric field strength than PECVD SiO_2 by more than 10 times and 2 MV/cm, respectively. The ALD SiO_2 deposited at 200 °C has a smaller quadratic VCC in term of magnitude than ALD SiO_2 deposited at 400 °C, for a given capacitance density. The MIM capacitor with 4 nm ALD SiO_2 deposited at 400 °C has a low leakage current of 2×10^{-7} A/cm^2 at 3.3V bias, a high field strength of 19.3 MV/cm and high operation voltage of 3.6V for a 10-year operation lifetime.

6.1.2 **High performance MIM capacitors with Er_2O_3 on ALD SiO_2**

The MIM capacitor with 20 nm Er_2O_3 was demonstrated to have a capacitance density of 9 fF/μm^2, leakage current of 10^{-6} A/cm^2 at 3.3V bias and a quadratic VCC of 1400 ppm/V^2. Post deposition treatments consisting of the post-deposition anneal at 400 °C and O_2 plasma treatment were shown to reduce the quadratic VCC of the MIM capacitor with 20 nm Er_2O_3 significantly.

Er_2O_3 was stacked on ALD SiO_2 to achieve low leakage current and quadratic VCC while maintaining the high capacitance density. The RF bias applied to the wafer substrate holder was found to have detrimental effect on the leakage currents of the stacked dielectrics. An optimized MIM capacitor with 8.9 nm Er_2O_3 on 3.3 nm ALD SiO_2 deposited at 400 °C was demonstrated to have excellent performance: a capacitance density of 7 fF/μm^2, a quadratic VCC of -89 ppm/V^2 at 100 kHz, a leakage current of 10^{-8} A/cm^2 at 3.3 V, a dielectric field strength of 8.6 MV/cm and an operation voltage of 5.1 V for a 10-year operation lifetime. With leakage currents of

~10^{-7} A/cm^2 at 3.3 V at ~ 10^{-8} A/cm^2 at 2V, the MIM capacitors with capacitance densities of 7.5 and 8.6 fF/μm^2 and quadratic VCCs less than 100 ppm/V^2 were also demonstrated with the (7 nm) Er_2O_3/(3.3 nm) ALD SiO_2 (deposited at 400 °C) and (8.8 nm) Er_2O_3/(2.3 nm) ALD SiO_2 (deposited at 200 °C) stack dielectrics.

6.1.3 **MIM capacitors for high voltage applications**

MIM capacitors with single layer Er_2O_3 and HfO_2 (80 nm) deposited by sputtering were investigated. The dielectric constants of as-deposited Er_2O_3 and HfO_2 were found to be similar, which were about 19.5 and 19.1, respectively. The amount of O_2 flow in the chamber during the post-deposition anneal of the dielectrics affected the capacitance densities and quadratic VCC of Er_2O_3 and HfO_2 significantly. By optimizing the anneal condition, reducing the quadratic VCC and increasing the capacitance density could be achieved concurrently. The MIM capacitors with HfO_2 (and Er_2O_3) were demonstrated to have quadratic VCCs of 17 (and 30) ppm/V^2, capacitance densities of 2.6 (and 2.4) fF/μm^2 and leakage currents of 40 (and 15) μA/cm^2 at -20V bias.

For the stacked dielectrics of Er_2O_3 on SiO_2, the quadratic VCCs were less negative (increased) with increasing Er_2O_3 thicknesses in the stack of Er_2O_3 (30-60 nm) on 5.5 nm ALD SiO_2 (deposited at 400 °C) and 8 nm PECVD. The trend was however opposite for the stack of Er_2O_3 (30-60 nm) on 4.3 nm ALD SiO_2 (deposited at 200 °C): the quadratic VCC changed from positive to negative (reduced) when the thickness of Er_2O_3 increased. Low quadratic VCC of -13 ppm/V^2 and high capacitance density of 2.62 fF/μm^2 were achieved with 45 nm Er_2O_3 on 4.3 nm ALD SiO_2 (deposited at 200 °C) stacked dielectrics. The leakage current at -20 V was

9.4×10^{-6} A/cm^2. The leakage current can be reduced to 6×10^{-7} A/cm^2 with the dielectrics stack of 60 nm Er_2O_3 on 5.5 nm ALD SiO_2 (deposited at 400 °C), however the capacitance density and quadratic VCC were also changed to 2.1 fF/μm^2 and -48 ppm/V^2, respectively.

6.2. **Suggestions for future works**

In chapter 4, an MIM capacitor using Er_2O_3/SiO_2 stacked dielectrics with a performance satisfying the ITRS requirement for year 2013-2015 was demonstrated. However, to meet the requirement for the year 2016-2019, extensive research must be carried out. As presented in chapter 4, the quadratic VCC of an MIM capacitor with a stack of a high-k dielectric on SiO_2 is given by:

$$\alpha = C_0^3 \left(\alpha_2/C_{2o}^3 + \alpha_1/C_{1o}^3\right), \tag{6-1}$$

Where (α, C_0), (α_2,C_{2o}) and (α_1,C_{1o}) are the quadratic VCC and capacitance density of the stack dielectrics, high-k dielectric and SiO_2, respectively. When the thickness of the high-k dielectric or SiO_2 is reduced to zero (their capacitances approach infinity values), the values of α_1/C_{1o}^3 or α_2/C_{2o}^3, respectively should also approach zero.

The aim of the MIM capacitor design for RF application is to increase C_0 and keep α as low as possible (α = 0). To increase the capacitance density C_0, one can increase the value C_{1o} or C_{2o} which are related to each other by Eq. (6-1) for a zero quadratic VCC (α). The illustrations of α/C^3 versus capacitance density C of the high-k dielectric and SiO_2 are shown in Fig. 6-1, showing how C_{1o} and C_{2o} can be matched to obtain α = 0. Three scenarios are presented Fig. 6-1: (a) the capacitance densities of the high-k dielectric and SiO_2 both increase, (b) the capacitance density of SiO_2 is

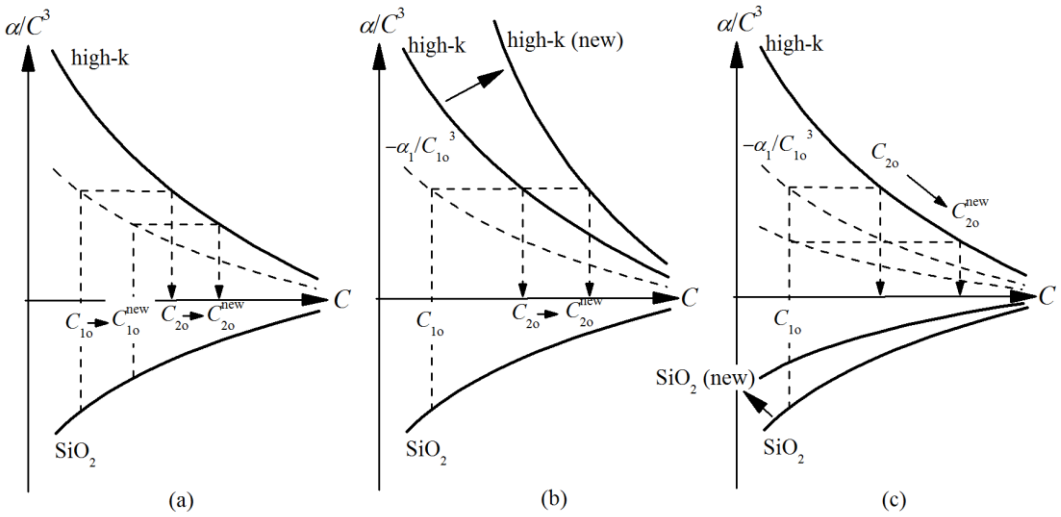

Fig. 6-1: Illustrations of α/C^3 versus capacitance density C for SiO_2 and a high-k dielectric showing how to achieve zero quadratic VCC for the stack dielectrics. (a) The capacitance densities of the high-k dielectric and SiO_2 both increase; (b) the capacitance density of SiO_2 is constant, but a new high-k dielectric is used; and (c) a new SiO_2 material is used. The interception points between α_2/C_{2o}^3 curves and the $-\alpha_1/C_{1o}^3$ lines give the matching capacitance density C_{2o} for $\alpha = 0$.

constant, but a new high-k dielectric is used and (c) a new SiO_2 material is used. As seen in Fig. 6-1 (a), when the thickness of SiO_2 is reduced and capacitance density increases from C_{1o} to C_{1o}^{new}, the capacitance density of the high-k dielectric also increase from C_{2o} to C_{2o}^{new} so that $\alpha = 0$ and as a result, the total capacitance density C_0 also increases. However, one cannot continuously scale down the thickness of SiO_2 due to the leakage current requirement. And to further increase C_0 while keeping C_{1o} constant, one should use other high-k dielectrics with larger quadratic VCC as illustrated in Fig. 6-1 (b) or reduce the quadratic VCC of SiO_2 as shown in Fig. 6-1 (c), both of which give $C_{2o}^{new} > C_{2o}$ for $\alpha = 0$. To reduce the thickness of SiO_2 and keep a good leakage current performance, atomic layer deposition is essential [option (a)]. Regarding the high-k dielectrics with high quadratic VCC at a given capacitance density, Al_2O_3 and PrTiO are two good candidates, as reviewed in chapter 2 [option

(b)]. To reduce the quadratic VCC of SiO_2, new deposition method such as low temperature ALD and optimized post-deposition treatment can be used [option (c)]. Besides SiO_2, Si_3N_4 and Ta_2O_5 which have larger dielectric constants were also reported to have negative quadratic VCC under certain conditions and should also be investigated for the stacked dielectrics.

The MIM capacitors for high voltage applications were also studied in this work. Low quadratic VCC and high capacitance densities were demonstrated; however the leakage currents are still relatively high. The quality of the high-k dielectric needs to be improved by specifically optimizing the deposition method and the post deposition anneal for thick dielectric films.

Appendix

A. List of publications

Journals and letters

[1] **T.H. Phung**, D.K. Srinivasan, P. Steinmann, R. Wise, M.B. Yu, Y.C. Yeo, and C.X. Zhu, "Investigation of PVD Er_2O_3 and ALD SiO_2 in Metal-Insulator-Metal Capacitors for RF Applications", pending submission.

[2] **T.H. Phung**, P. Steinmann, R. Wise, Y.C. Yeo, and C.X. Zhu, "Modeling the Negative Quadratic VCC of SiO_2 in MIM Capacitor", *IEEE Electron Device Letter*, v. 32, 1671, 2011.

[3] **T.H. Phung**, D.K. Srinivasan, P. Steinmann, R. Wise, M.B. Yu, Y.C. Yeo, and C.X. Zhu, "High Performance Metal-Insulator-Metal Capacitors with Er_2O_3 on ALD SiO_2 for RF Applications", *Journal of Electrochemical Society*, v. 158, H1289-H1292, 2011.

[4] **T.H. Phung**, R.L. Xie, S. Tripathy, M.B. Yu, and C.X. Zhu, "Low Temperature Metal Induced Lateral Crystallization of Ge Using Germanide Forming Metals", *Journal of Electrochemical Society*, v. 157, H208, 2010.

[5] **T.H. Phung**, R.L. Xie, S. Tripathy, M.B. Yu and C.X. Zhu, "Low Temperature Metal-Induced Lateral Crystallization of $Si_{1-x}Ge_x$ Using Silicide/Germanide-Forming-Metals", *Japanese Journal of Applied Physics*, v. 49, 04DH10, 2010.

[6] **T.H. Phung** and C.X. Zhu, "Palladium-Induced Crystallization of Germanium with Varied Palladium Thicknesses", *Journal of Electrochemical Society*, v. 157, H755, 2010.

[7] R.L. Xie, **T.H. Phung**, M.B. Yu, and C.X. Zhu, "Effective Surface Passivation by Novel SiH_4-NH_3 treatment and BTI Characteristic on Interface-Engineered High-Mobility HfO_2 – Gated Ge pMOSFETs*"*, *IEEE Transactions on Electron Devices*, v. 57, 1399, 2010.

[8] R.L. Xie, **T.H. Phung**, M.B. Yu, S.A. Oh, S. Tripathy, and C.X. Zhu, "Palladium-Induced Lateral Crystallization of Amorphous-Germanium Thin Film on Insulating Substrate", *Electrochemical Solid-State Letter*, v. 12, H266, 2009.

[9] R.L. Xie, **T.H. Phung**, W. He, M.B. Yu, C.X. Zhu, "Interface-engineered high-mobility high-κ/Ge pMOSFETs with 1-nm equivalent oxide thickness", *IEEE Transactions on Electron Devices*, v. 56, 1330, 2009.

Conferences

[10] **T.H. Phung**, M.J. Chen, H.J. Kang, C.F. Zhang, M.B. Yu, and C.X. Zhu, "Rapid-Melting-Growth of Ge on Insulator using Cobalt (Co) Induced-Crystallized Ge as the Seed for Lateral Growth", *International Conference on Solid-State and Integrated Circuit Technology*, 2010.

[11] **T.H. Phung**, R.L. Xie, S. Tripathy, M.B. Yu and C.X. Zhu, "Low Temperature (375 ^{o}C) Metal Induced Lateral Crystallization (MILC) of $Si_{1-x}Ge_x$ ($0 \leq x \leq 1$) using Silicide/Germanide Forming Metals (Ni, Pd and Co)", *2009 International Conference on Solid State Devices and Materials (SSDM2009)*, 2009.

[12] R.L. Xie, **T.H. Phung**, W. He, Z.Q. Sun, M.B. Yu, Z.Y. Cheng and C.X. Zhu, "High mobility high-k/Ge pMOSFETs with 1 nm EOT -New concept on interface engineering and interface characterization", *IEEE International Electron Devices Meeting (IEDM)*, pp.1-4, 2008.