Interface study of high-k oxide and Ge for the future Ge based MOSFET device

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Abstract

The progress of continuous scaling of metal-oxide-semiconductor field-effect transistors (MOSFET) technology is accompanied by many novel materials and advanced process technologies. High-k dielectrics materials and Germanium (Ge) are two most promising aspects for the further improvement when the international technology roadmap for semiconductors (ITRS) hits 22nm and below. High-k dielectrics gate oxide is critical to replace current SiO_2 with thickness limitation of 2nm and alternative high mobility Ge channel can dramatically improve the device performance.

This thesis examines the interface and surface properties of Ge and high-k materials $SrTiO_3$ (STO) from both the experiment and first-principles calculation. In the experiment part, Ge is grown on top of the STO (100) substrate through direct DC sputtering with atomic oxygen source treatment. From high resolution XRD results, it can be concluded that 500 ℃ substrate temperature leads to the single crystalline Ge (111) thin film while 650 ℃ substrate temperature changes the thin film to Ge (100). This single crystalline structure and clean interface are verified by HRTEM images. STEM EDX line-scan reveals the phenomenon of Ge diffusion at interface, which is much more serious at higher deposition temperature. The stable surface bonding is Ge-TiO2 terminated instead of -SrO in the Si and high-k interface. XPS analysis of the Ge thin films shows the existence of oxidation states at the interface, which is a

mix of Ge_2O (Ge^{1+}) and GeO (Ge^{2+}) components. The HRTEM and AFM images of samples with 6mins deposition time present the Nanocrystal (NC) islands for the Ge and the density is around $3.68\times10^{12}cm^{-2}$. This highly integrated NCs (~10^{12} cm^{-2}) is very useful for the application of floating – gate (FG) in the nonvolatile memory (NVM) technology.

In the first-principles calculation part, Hybrid-functionals calculations have been employed to study interfacial electronic properties of perovskite $SrTiO_3$ (001)/Ge (100). It is found that the Ge surface states of Ge p-(2×1) can be effectively removed either by one Sr or two O atoms, and the surface passivated by two oxygen atoms is more energetically favorable. Interface structure of $SrTiO_3$ with TiO_2 terminated surface is more stable despite the different surface chemical environments of Ge, and the interface structures without dangling bonds show semiconductor character. It is also noted that the relative stability of the insulating interface structures is not affected by the external electric field.

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Chapter 1

Introduction

1.1 Si based MOSFET and Scaling Technology

We have stepped into the “silicon age” for more than 60 years since the first semiconductor transistor was invented in December 1947 by John Bardeen and Walter Brattain at Bell Labs. [1] After the birth of the first generation metal oxide semiconductor field effect transistor (MOSFET) in 1960, [2] the integrated circuits (IC, also known as microchips or microcircuits), where MOSFET plays an important role for the core electronic devices, have been successfully revolutionizing the world for the past half century. (See Fig. 1.1 for a typical MOSFET)

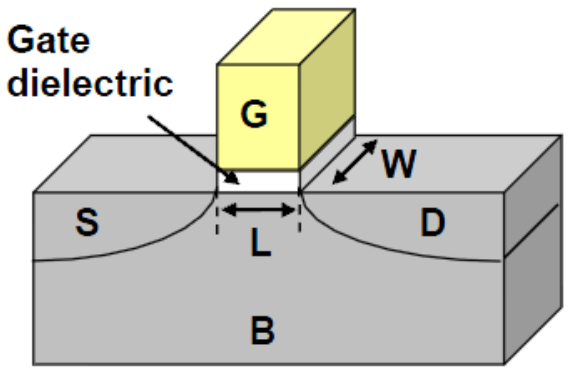

Figure 1.1. Schematic of a typical bulk MOSFET structure. Four terminals are denoted as Gate (G), Source (S), Drain (D), and Body (B). Geometry parameters are denoted as gate length (L) and gate width (w).

In order to continuously improve the speed and the functionality of the IC, scaling of MOSFET technology is a must trend for increasing both the package density and performance. This scaling behavior as the IC driving force has been vividly described and predicted by Gordon Moore at 1960: the size of the transistor will be reduced by two times and the density of devices in a chip will be double for every 18 months (Fig. 1.2). [3, 4] The Semiconductor Industry Association (SIA) has also been publishing the international technology roadmap for semiconductors (ITRS) since 1992 to reveal the semiconductor industry's future technology trends and requirements (Fig. 1.3). [6]

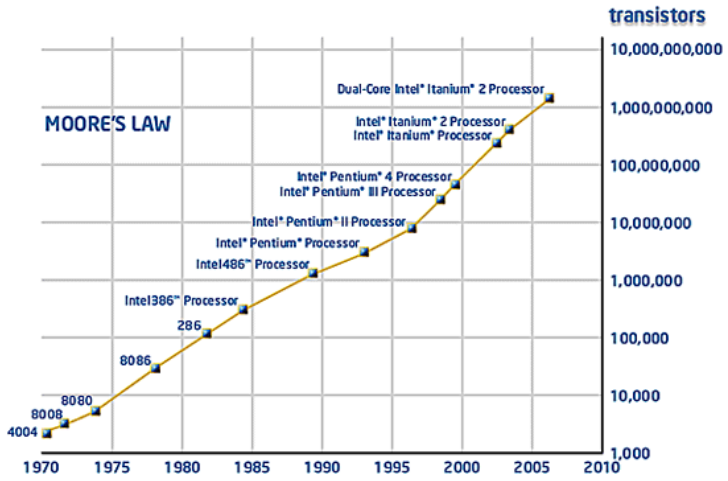

Figure 1.2. Historical trend agrees with the Moore's Law. Number of transistor in the Intel Micro Processor increases exponentially over time. [5]

Year of Production	2006	2007	2008	2009	2010	2011	2012
DRAM 1/2 Pitch (nm) (contacted)	70	65	57	50	45	40	36
MPU/ASIC Metal1 1/2 Pitch (nm) (contacted)	78	68	59	52	45	40	36
MPU Physical Gate Length (nm)	28	25	23	20	18	16	14
EOT for extended planar bulk (Å)	11	11	9	7.5	6.5	5	5
Effective NMOS $I_{d,sat}(\mu A/\mu m)$ (extended planar bulk) ($I_{d,sat}$ of PMOS is ~ 40-50%)	1130	1200	1570	1810	2050	2490	2300
Mobility Enhancement Factor for $I_{d,sat}$ (extended planar bulk)	1.09	1.08	1.09	1.10	1.10	1.12	1.11

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known

Figure 1.3. Near-term high-performance logic technology requirements in ITRS 2005. [6]

The enhancement of various electrical parameters of MOSFET (such as gate length, gate width, gate thickness and power supply voltage) is the key concept for the MOSFET scaling according to the roadmap and already proposed by Dennard in 1974. [7] In Fig. 1.1, it is a typical four-terminal bulk MOSFET and the saturated drain current is given by Equation 1.1, where C is the inversion capacitance, (V_g-V_{th}) is the gate overdrive, μ_{eff} is the effective carrier mobility.

$$I_d = \frac{w\mu_{eff}C}{2L}(V_g - V_{th})^2 \tag{1.1}$$

According to Eq. (1.1), in order to achieve a higher drive current (I_{dsat}), we can either increase gate overdrive power (V_g - V_{th}), effective carrier mobility (μ_{eff}), width (w), inversion capacitance (C) or reduce channel length (L). The increase of width is

contrary with the scaling rule and the increase of power has the reliability concerns. Besides them, the decrease of gate length can cause short channel effect and currently the gate length has already reached its fundamental limit. [8] The only parameters left behind are the effective carrier mobility (μ_{eff}) which is the channel carrier mobility and inversion capacitance(C) which is related to the gate dielectric. Many novel device technologies and new materials have been proposed to solve the ultimate scaling issues for future MOSFET by improving these two parameters, e.g. high mobility channel materials and high-k dielectric. These approaches which are also named performance boosters by ITRS can control the short channel effect (SCE) while maintain continuous performance enhancement (Fig. 1.4). [9]

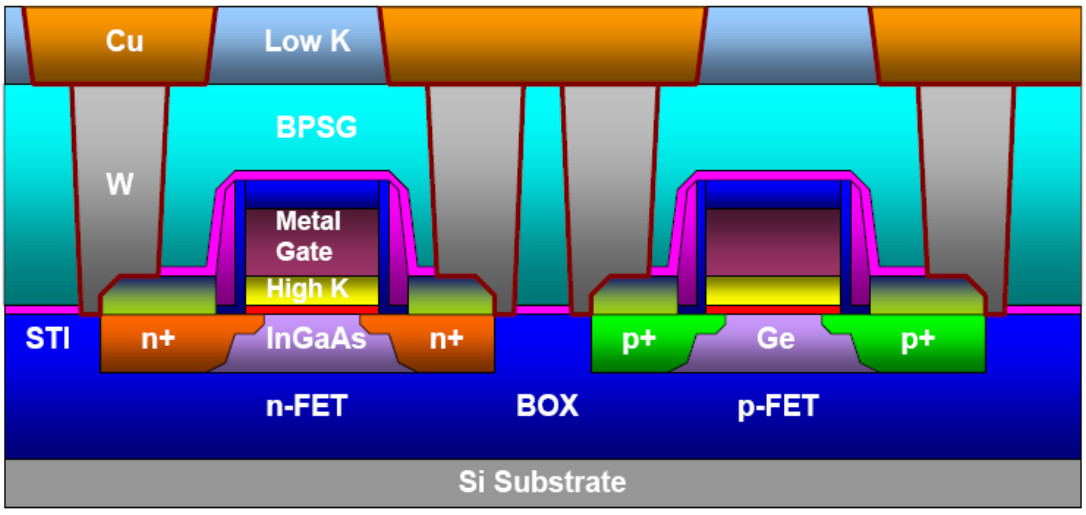

Figure 1.4. A schematic showing a possible combination of technology boosters. In the front end, device has high-k dielectric, metal gate electrode, and thin body, high mobility InGaAs for n-FET and Ge for p-FET. The back end interconnect includes low-k dielectric and low resistive metal Cu. [9]

1.2 High-k Dielectrics and Ge Channel in MOSFET

1.2.1 Introduction of High-k Dielectrics Materials

As mentioned in section 1.1, one major approach to enhance MOSFET performance is to increase the inversion capacitance(C). Currently in the industry the major material used for gate dielectric are SiO_2 (dielectric constant is 3.9) and SiON (for high performance technologies, dielectric constant is around 7). In order to meet the scaling requirement, the thickness of the gate dielectric continues to scale down till 1.5nm. [10, 11] Although this gate dielectric oxide thickness scaling can keep improving the device performance, it will reach the limit of around 2nm, below which the gate leakage current density J_g could become unacceptably high (see Fig. 1.5). Accordingly, it will also increase the static power and degrade device performance. [12, 13]

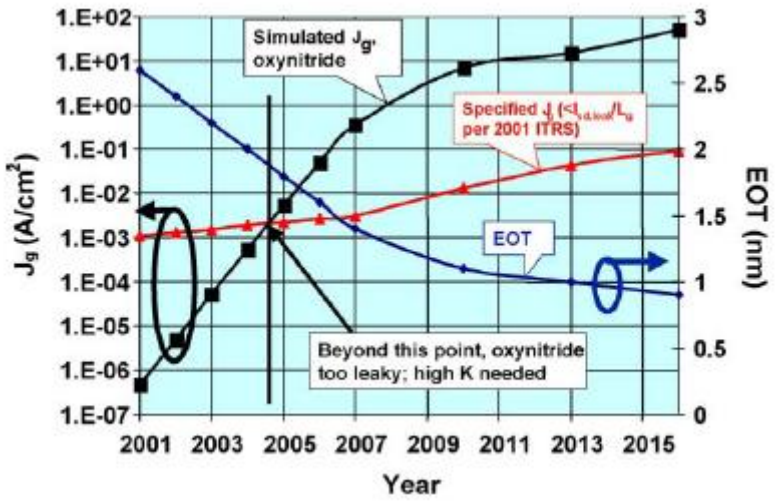

Figure 1.5. Gate leakage current, JG (SiON-based devices), and equivalent oxide thickness (EOT) of CMOS technologies, vs. the expected production year of these technologies. When the leakage current flowing through the SiON layer exceeds the ITRS requirements (here for low stand-by power technologies), an alternative gate dielectric should be used.

By introducing high-k gate dielectrics to replace the traditional SiO_2 or SiON, the physical thickness of the high-k gate dielectric can be much thicker compared to the physical thickness of the SiO_2 dielectric with the same equivalent oxide thickness (EOT can be described at equation 1.2 below).

$$t_{eq} = t_x \left(\frac{\kappa_{SiO_2}}{\kappa_x} \right) \tag{1.2}$$

where t_x is the physical thickness of the alternative oxide film and k_x is its dielectric constant, e.g. an oxide film with a dielectric constant of 7.8 can be approximately twice as thick as a SiO_2 film, while still having the same capacitance per unit area to maintain gate control over a MOSFET. [12] Therefore, the leakage current will be much smaller even for the EOT less than 1nm. That's to say, high-k materials as the gate oxide can enable the possibility of device scaling.

Some requirements for selecting the high-k materials for Si-MOSFET are summarized by M.Houssa: [13]

1. The relative dielectric constant of the high-k material should be somewhere between 10 and 30, which will give rise to fringe fields from the gate to the drain or source and these fields can degrade short channel performances.

2. The dielectric material must be an insulator with a band gap larger than 5 eV and the band offsets with silicon must be sufficient. Generally, increasing dielectric constant leads to lower conduction and valence band offset for materials in contact with silicon, and there is an inverse relationship between dielectric constant and the band gap [14]. To prevent conduction by Schottky emission of electrons or holes into their respective bands, i.e. reduce leakage current, the barrier at each band must be greater than 1 eV. As a comparison, the band gap of SiO_2 is 9 eV, and the conduction and valence band offsets with Si are 3.1 eV and 4.8 eV, respectively.

3. Interface preparation and quality are important for layer growth.

4. Low interface trap defect density, D_{it}, is typically less than 10^{11} cm^{-1} eV^{-1}.

5. Thermodynamic stability is essential for direct contact with Si. The oxides must have a large Gibbs free energy of formation to prevent reaction with Si. Oxygen diffusion coefficients must be low as they will cause uncontrolled interfacial layer (re)growth.

	K	Gap (eV)	CB offset (eV)
Si		1.1	
SiO_2	3.9	9	3.2
Si_3N_4	7	5.3	2.4
Al_2O_3	9	8.8	2.8 (not ALD)
Ta_2O_5	22	4.4	0.35
TiO_2	80	3.5	0
$SrTiO_3$	2000	3.2	0
ZrO_2	25	5.8	1.5
HfO_2	25	5.8	1.4
$HfSiO_4$	11	6.5	1.8
La_2O_3	30	6	2.3
Y_2O_3	15	6	2.3
a-$LaAlO_3$	30	5.6	1.8

Table 1.1. Static dielectric constant (K), experimental band gap and (consensus) conduction band offset on Si of the candidate gate dielectrics.

Table 1.1 shows the properties of a wide variety of high-k materials. These years, most of them have been studied and indentified as promising gate dielectrics candidates. In the semiconductor industry, Intel has been already using Hf-based high-k dielectrics (HfO_2 or nitride $HfSiO_x$) for its 45nm technology. Among these high-k materials in the list, $SrTiO_3$ has the highest dielectric constant ~2000; while this materials is rarely studied as a candidate for gate dielectrics in Si-MOSFET, due to its small band gap(~3.2 eV) and small conduction band offset(~0 eV) which could cause large leakage current. In our study, Ge with smaller band gap (~0.6 eV) is adopted instead of Si. [16] Taking the advantage of high dielectric constant and small lattice mismatch to Ge, we will focus on $SrTiO_3$ in this thesis from first-principles calculation and experimental respects.

1.2.2 Introduction of Ge Channel

One of the most important performance boosters is using the transport enhanced channel to replace the traditional Si based channel in the MOSFET. As stated in section 1.1, another parameter to increase the saturation current (I_{on}) with the device scaling is effective carrier mobility (μ_{eff}). The saturation current (I_{on}) can be represented by equation 1.3:

$$I_{on} \approx qN_s^{source} \cdot v_s \tag{1.3}$$

where q is the elemental charge, N^{source}_s is the surface carrier concentration near the source edge, and v_s is the carrier velocity near the source edge which is proportional to the mobility [17, 18]. Especially for the channel length less than 10nm, the carrier transport is dominated by full ballistic transport. The transistor speed is no longer determined by saturation velocity but by source injection velocity. Therefore, there is a must to replace the conventional silicon channel with novel materials with high mobility for the future generation nanoelectronics.

The characteristics of potential alternative channel materials like Ge, main III-V semiconductors (GaAs, InSb and InP) are listed in Table 1.2. Among these materials, it is noted that Ge is the only material that offers high mobility enhancement for both hole and electron with appropriate bandgap. In addition, its low melting point ensures

that the dopant activation temperature is as low as 400 ℃-500 ℃. [19, 20]

	Ge	Si	GaAs	InSb	InP
Bandgap, E_g (eV)	0.66	1.12	1.42	0.17	1.35
Electron affinity, χ (eV)	4.05	4.0	4.07	4.59	4.38
Hole mobility, μ_h ($cm^2V^{-1}s^{-1}$)	1900	450	400	1250	150
Electron mobility, μ_e ($cm^2V^{-1}s^{-1}$)	3900	1500	8500	80 000	4600
Effective density of states in valence band, N_V (cm^{-3})	6.0×10^{18}	1.04×10^{19}	7.0×10^{18}	7.3×10^{18}	1.1×10^{19}
Effective density of states in conduction band, N_C (cm^{-3})	1.04×10^{19}	2.8×10^{19}	4.7×10^{17}	4.2×10^{16}	5.7×10^{17}
Lattice constant, a (nm)	0.565	0.543	0.565	0.648	0.587
Dielectric constant, k	16.0	11.9	13.1	17.7	12.4
Melting point, T_m (°C)	937	1412	1240	527	1060
Clarke number (%)	6.5×10^{-4}	25.8	Ga: 1×10^{-3} As: 5×10^{-4}	In: 1×10^{-5} Sb: 5×10^{-5}	In: 1×10^{-4} P: 8×10^{-2}

Table 1.2. Material characteristics of alternative channel materials [16]

Although III-V semiconductors have higher electron mobility, Ge can provide the highest hole mobility among the main semiconductors, and it has already been demonstrated that compressively strained Ge p-MOSFETs provide ten times or higher hole mobility against Si p-MOSFETs. [21-24] The compatibility of Ge with both nMOSFET [25] and pMOSFET [26] has also been proven. It's even reported that hole mobility enhancement of as high as ten is obtained by combing both Ge channel (GOI with 93% Ge content) and compressive strain, [26] which can further indicate that Ge is one of the most important future channel materials.

Although Ge is a promising material to be the channel in the MOSFET, there are still

many issues yet to be solved: [26]

(1) Gate-insulator formation with high-quality MIS interfaces, the poor properties of germanium oxides and lack of good quality gate dielectric greatly hinder the development of Ge MOS device. For example, it is reported that the high density of interface traps of the gate stacks is one of the possible reasons for the low mobility of Ge nMOSFET [27];

(2) High-quality Ge or GOI channel layer formation; [28 - 32]

(3) Formation of low-resistivity S/D junctions;

(4) Improvement of poor performance of n-channel MOSFETs;

(5) Reduction in large leakage current;

(6) Appropriate CMOS structures and integration technologies.

In this thesis, we will focus on the point (1) and (2) to discuss about first-principles study of interface of high-k material (STO) with Ge, and experimental study of crystal growth of Ge on high-k material (STO) for future application of GOI channel formation.

1.2.3 Literature Review of Ge with High-k Dielectrics

By successfully implementing Ge as MOSFET channel materials integrated with high-k dielectrics materials, state of the art researches mainly focus on two fields: (1) Ge on top of the high-k dielectrics material, which constitutes the structure called Germanium-on-insulator (GeOI); (2) high-k material on top of the Ge, which forms the stack of high-k gate oxide and Ge active channel.

The first important application of high-k dielectrics in the Ge channel based MOSFET is the GeOI, which combines high mobility of charge carriers with the advantages of an Silicon-on-insulator (SOI) structure. It is also an attractive integration platform for the future IC technology. As the replacement for the SOI structure, a truly realization of MOSFET on a fully epitaxial structure GeOI channel must involve two material problems: a uniform epitaxial oxide is needed, and a uniform epitaxial semiconductor must be grown. [33]

Traditionally, amorphous SiO_2 is used as electrical isolation layer; while for the GeOI, this isolation layer can be any suitable oxide like SiO_2 or high-k materials with proper lattice constant which serves not only the electrical isolation function but also the buffer layer between Ge cannel and Si substrate.

Large dimension of Ge layers has been directly deposited on Si by using low growth

temperature 300–340 ℃ early at 1994. [34, 35] Due to the large lattice mismatch between Si and Ge (4.2%), the three-dimensional island nucleation is inhibited, [36 - 39] which is good to get a flat Ge layer. However, this large lattice mismatch could also induce high threading dislocation density. The post annealing at 750–890 ℃ is necessary and effective to repair this defect but could cause another problem that Si diffuses from substrate into the Ge film and reduce the purity of Ge epilayer. [40 - 43] Many reports also represent other methods to grow Ge channel on Si substrate, e.g. selective growth on patterned Si substrate [44-47] and growth on compositionally graded SiGe buffers. [48, 49] Although these approaches can provide relatively large area Ge epilayer, all of them suffer from the same problem: direct contact of Ge and Si can easily induce Si impurities at Ge epilayer. [50] Also, several micrometers SiGe buffer layer located in the interface of Ge and Si also put up a question for industry to integrate Ge into Si-based device. [51]

All these difficulties can be overcome in the GeOI fabrications. The most common methods for the GeOI fabrication are Ge condensation technique [52] and smart cut technique (or layer transfer technique). [53] Ge condensation technique or oxidation-induced Ge condensation is based on oxidation of SiGe epitaxially grown on the SOI substrate. This method can be useful for the local and thin GeOI formation. The Ge epilayer thickness is controlled by the Ge fraction and the SiGe layer thickness. The major drawback is the high thermal budget (>1000 ℃) and the oxidation induced plastic deformation. Smart cut technique nowadays is the most

widely used approach for GeOI fabrication. Usually for thick Ge film formation, bond and grinding method is used [54]; for thin Ge film growth, grind and etch-back method is applied where compositionally graded Si_xGe_y is the chosen buffer layer [55]. Only one of these two methods can be used for one single wafer which is not applicable for the wafer level GeOI fabrication. Smart cut technology can be efficient to get both benefits. The basic process flow includes oxide formation, ion implantation, hydrophilic bonding to a Si base substrate, followed by Ge film transfer and finishing steps. Wafer diameters from 100 to 200mm with the thickness range from 200 down to below 50 nm were demonstrated [56 - 58]. However, this method requires complex processing and has difficulty in obtaining very high-quality Ge crystals.

In recent years, single crystalline high-k dielectrics have been studied as potential epitaxial templates for Ge epitaxy. The first report about Epitaxial silicon and germanium on buried insulator heterostructures with single crystalline oxide dielectric buffer layer was published by N. A. Bojarczuk *et al.* in 2003. [33] By using the solid phase epitaxy, the structure of Si(111)/substrate/LaYO/Si and Si(111)/substrate/LaYO/Ge (see Fig 1.6(a)) has been grown. It's noted that the thickness of the Ge is 4nm and the solid phase epitaxial transformation temperature for Ge is 450 ℃, which is lower than that for Si (around 580 ℃). Based on this heterostructure, Ge channel MOSFET is also fabricated and the output characteristics in Fig 1.6(b) demonstrate a field effect charge inversion in the epitaxial germanium

channel by applying a field through the buried epitaxial LaYO gate dielectric.

J.W. Seo *et al.* reported the (001) oriented Si based GeOI in 2007. [59] They fabricated the GeOI on (001)-Si substrate by using Sr(Hf,Ti)O3 / Si template. Two steps growth process is applied in this experiment: Firstly, crystalline (001) oriented islands are seeded at 610 ℃; secondly, the Ge growth is continued at a lower temperature of 350 ℃, which promotes homogeneous coverage of the oxide. They concluded the crystallinity of the islands strongly depended on the temperature (below 610 ℃ can only get amorphous Ge) while the further increase of the growth temperature did not change the three-dimensional growth. This is the reason behind this high to low temperature growth process. Although the epi-Ge film quality is good, the low mobility and high density of defects still make it far from device fabrication.

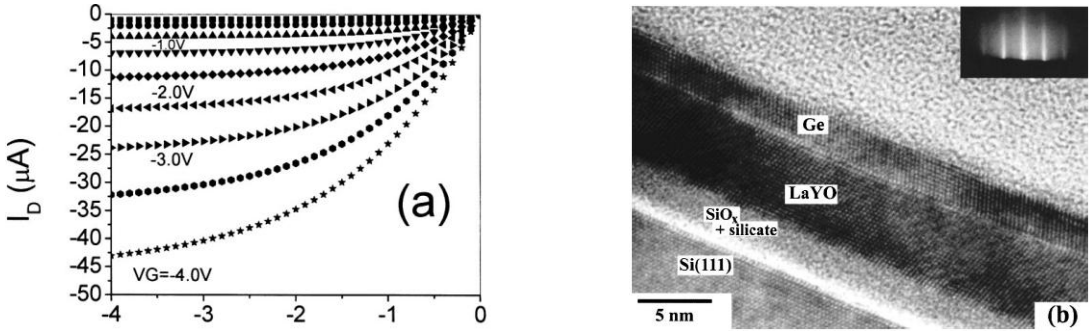

Figure 1.6. (a) the drain to source current (Id) plotted against the drain to source voltage (V_d) as a function of different gate voltages (Vg) in the GeOI-MOSFET; (b) high resolution transmission electron micrograph of an epitaxial Si(111)/LaYO/Ge structure.

Another popular high-k oxide dielectric material as buffer layer for GeOI application

is Pr_2O_3. Schroeder's group has made a lot of contributions for this study. [60 - 68] Single crystalline Ge layers were integrated on Si (111) by MBE as well as CVD via MBE grown Pr oxide heterostructures Ge(111)/Pr2O3(111)/Si(111). High-to-low temperature growth steps are also adopted by using 550 ℃ to get crystalline Ge (111) seed islands and subsequently by 300 ℃ substrate temperature to deposit large single crystalline and fully relaxed Ge (111) layers. Their findings reveal that the Pr oxide buffer systems can be used to functionally tailor some important heteroepitaxy parameters.

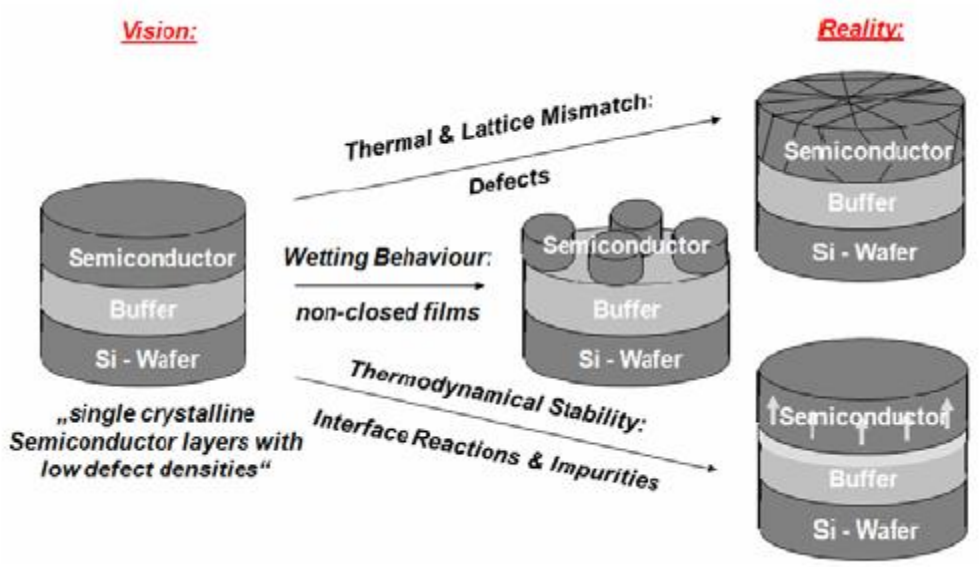

Figure 1.7. Overview of important epitaxy parameters to achieve the integration of high quality semiconductor layers via oxide heterostructures on Si.

Overall, the GeOI has three major advantages from Fig 1.7: Lattice misfit engineering, Interface reactivity engineering and Surface wetting engineering. [61] They can also be extended to all possible oxide heterostructures which can be grown single

crystalline on Si to achieve the integration of single crystalline alternative semiconductor layers on Si. In this thesis, we choose $SrTiO_3$ as the substrate to evaluate the growth behavior of Ge on the top. As $SrTiO_3$ is proven to be easily and epitaxially grown on the Si, this study can finally broaden the topic to Ge/$SrTiO_3$/Si based Ge-FET and other related devices.

The second hot topic is that the high-k material as the function of gate oxide on top of the active Ge channel. In the early development stage of Ge MOSFET, germanium oxynitride (GeON) is used as gate dielectrics instead of GeO_2. [69, 70] As the continuous downscaling of roadmap, GeON could introduce very high leakage current, especially for the EOT of gate oxide smaller than 20A. [71] Under this condition, high-k material must to be implemented as gate dielectrics for the future Ge MOSFET.

Many research groups have reported growth of high-k oxides on Si and Ge substrate, such as HfO_2 and ZrO_2. For HfO_2, which is proven to be very good high-k dielectrics replacement of SiO_2 for the Si MOSFET, it encounters the difficulty when comes to Ge. Some reports found that the formation of Germanide between HfO_2 and Ge interface would cause large leakage current in devices like GeON. [72, 73] Compared with HfO_2, ZrO_2 is a better choice for Ge instead of Si substrate. A layer of unstable silicide is formed by the reaction of ZrO_2 and Si surface which can lead to high leakage current. In contract, ZrO_2 is the first high-k material demonstrated in the Ge

MOSFET and it shows no interfacial layer at the interface of ZrO_2 and Ge channel. [74] The peak hole mobility of this ZrO_2/Ge FET is as high as 313 cm2/V s while the problem is also from high leakage current. [75] Although many high quality single crystalline high-k dielectrics materials have been epitaxially grown on Si, such as $SrTiO_3$ [76], ZrO_2 [77], and HfO_2 [78], very few are reported on Ge substrate. Kim *et al*. reported the epitaxial deposition of ZrO_2 on Ge (001) substrate by atomic layer deposition in 2003. [79] Large frequency dispersion and hysteresis from C-V test from this sample illustrate the poor interface of this epitaxial grown thin film. Therefore, we need to investigate more on the other suitable high-k materials on the Ge substrate, where the small lattice mismatch between the selected high-k oxide and the Ge is the essential for epitaxial growth. Similar to the GeOI application, we also choose $SrTiO_3$ on Ge as the study model in this thesis.

1.3 Motivation, Scope and Thesis Organization

Although plenty of works have been done on the study of interface of Ge and high-k materials both in the aspects of Ge growth on high-k buffer layer (GeOI) and high-k dielectric on Ge channel, there are many problems needed to be solved before the application for the future Ge-MOSFET, especially in the sub-22nm regime. Some major challenges are listed below:

1. Si and Ge diffusion at high temperature during the deposition growth will form undesirable inter-layer and cause high leakage current for the device. We have to look for more suitable candidates as the buffer layer to grow single crystalline Ge channel in the Ge-MOSFET.

2. Current cost of high quality GOI fabrication is expensive and the process is very complex, therefore, alternative simple deposition methods need to be investigated.

3. Despite the large amount of demands in the near future, there are limited studies on the surface passivation of Ge and approximate high-k dielectrics materials which are suitable for Ge-based electronic devices.

4. More studies about the physical properties of interface of high-k oxide and Ge

need to be carried out for the engineering desires respective to the different device electrical requirements.

The objectives of this thesis are to address these challenges mentioned above by focusing on two areas:

1. To experimentally grow high quality single crystalline Ge on $SrTiO_3$ substrate and do the physical characterizations to study its interface/surface properties and thermal stability.

2. To theoretically investigate the structural and electronic properties of the model of $SrTiO_3$ on Ge substrate through first-principles calculation with and without external electric field.

The main issues discussed in this thesis are documented within 4 chapters and organized as following:

In chapter 2, we briefly describe some typical fabrication processes and equipments for the growth of epitaxial layer, as well as some characterization techniques and tools for the subsequent material study. Besides, we also discuss some basic theories of first-principles calculation and modeling.

In chapter 3, we present results of experimental study on the growth of the crystalline Ge layer on top of the $SrTiO_3$ (100) substrate. We found that the orientation of Ge strongly depended on the substrate temperature during the process. Higher temperature around 650 ℃ leads to Ge (001); while at 500 ℃ Ge (111) with good crystalline quality is formed. TEM, XRD, XPS and STEM EDX line-scan results show the clear evidence on these findings.

In chapter 4, we focus on Hybrid-functionals based first-principles study of the models for $SrTiO_3$ (100) on top of the Ge (100) substrate. We found that the Ge surface can be effectively passivated either by Sr or O atoms, and the O atom passivation is more energetically favorable. Interface structure of $SrTiO_3$ with TiO_2 termination on Ge surface is more stable despite the different surface chemical environments of Ge, and the relative stability of this stable structure is not affected by the external electric field.

Finally, we summarize this thesis with conclusions and make some recommendations for the future work.

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Chapter 2

Methodology

Many techniques can be used to study the physical properties of this Ge/High-k dielectrics material system from both the experimental and theoretical aspects. For the thin film growth, mainly three categories of deposition methods are suitable: (1) physical vapor deposition (PVC), e.g., evaporation method, reactive PVD and Sputtering; (2) chemical vapor deposition (CVD), e.g., low pressure CVD, plasma enhanced CVD and metal organic CVD; (3) and other depositions such as reactive deposition and molecular beam epitaxy (MBE). In this chapter, we will only focus on the details of sputtering with the atomic oxygen source, which is the method adopted for the Ge thin film growth for this thesis.

Besides the deposition, many different characterization methods are available for those important properties of thin films. Some most common measurement techniques are listed here. Spectrophotometer and ellipsometer can be taken to measure the thickness and the optical properties of thin film. For the crystal structure, transmission electron microscopy (TEM) and X-ray diffraction (XRD) are the best choice. Some more, we can use scanning electron microscope (SEM) and atomic force microscopy (AFM) to study the surface microstructure. AES, XPS, EDAX and SIMS are the four common methods for the chemical and elemental Composition. As varying from

application to application, we can combine some of these methods for the thin film study. In this chapter and also this thesis, we will introduce four characterization techniques: TEM, XRD, XPS and AFM.

The theoretical techniques for the selected model study include empirical (or semi-empirical) and first-principles methods. In the last part of this chapter, first-principles calculation with VASP and CASTEP codes will be briefly discussed which are used as theoretical method for this thesis.

2.1 Thin Film Deposition Methods - Sputtering

Sputtering and sputter deposition are widely used techniques for the erosion of surfaces and the deposition of films. Sputtering is also called sputter etch, where atoms are ejected from a solid target material due to bombardment of the target by energetic particles. Sputter deposition is a well known physical vapor deposition (PVD) method of depositing thin films on semiconductor.

Generally, sputtering occurs whenever an energetic particle strikes a surface with enough energy to dislodge an atom from the surface. The incident particle can be any species, e.g. atoms, ions, electrons, photons, and neutrons as well as molecules and molecular ions. But for practical case, sputtering almost always utilizes ion bombardment, either with inert gas ions such as Ar+ and Kr+, or small molecular ions such as N2+ and O2+. As the Incident particle energies are required to be in the range of hundreds of eV, ions are the better choice compared to the neutral atoms. Therefore, an acceleration voltage of a few hundred volts within a vacuum chamber is configured as the plasma system, which can serve to generate and accelerate the ions. Based on the different source for producing plasma, there are three major classes of systems for sputtering application.

(a) DC diode system, which is just consisted of an anode and a cathode inside a vacuum system. Under some proper conditions with adequate voltage

across the electrodes and the appropriate gas pressure, the gas will breakdown into plasma. Near the cathode is a dark space or sheath in which there is a very large electric field. Therefore the negatively biased target plate (cathode) is bombarded by argon ions at about 10 mTorr pressure. (Fig. 2.1(a)) In the Chapter 3, the experiment is conducted under DC diode sputter system and the details of conditions will be discussed later.

(b) RF diode system, compared to the DC diode system, the only difference is the power supply is not a DC and running at a high frequency (normally it is 13.56MHZ), see Fig. 2.1(b). The RF diode operates in a slightly different way than the DC diode: for a small part of the RF cycle, the cathode and anode are electrically reversed. This eliminates charge buildup on an insulating surface by providing an equal number of ions and electrons. This allows insulators and metals to be sputtered in reactive environments which is not possible with DC system due to charge. Secondary, the electrons oscillating in the RF field is more efficient within plasma, and for the same power level RF sputtering can have higher deposition rate. The limitation for the RF diode is that a high voltage (>2000 V) is required during the process.

(c) Magnetrons system, where a static magnetic field configured is used at the cathode plate, and the magnetic field is located parallel to the cathode surface, see Fig. 2.2. As the magnet behind the target creates a field to confines the

electron movement, the ionization is more efficient compared to the diode system and therefore can dramatically increase the deposition rate at a low power (only 5 to 20 kW). The working voltage for magnetrons system is around 500 V and working pressure is about 0.1 to 10 mTorr.

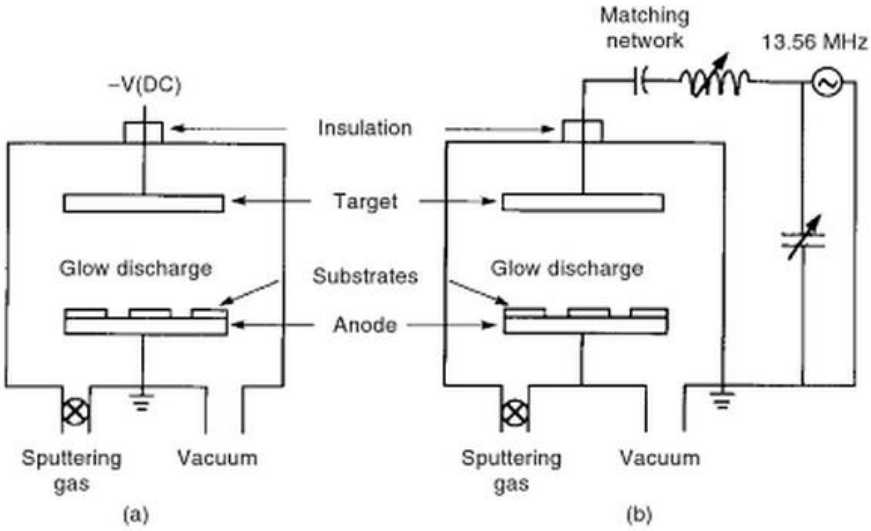

Figure 2.1. Schematic sputtering systems (a) DC and (b) RF [1]

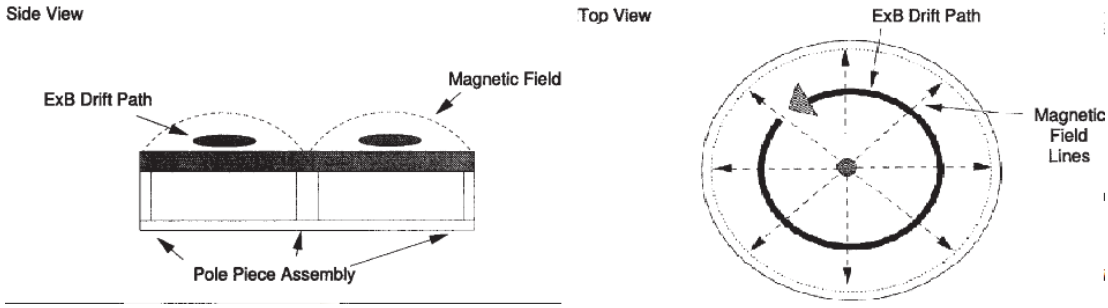

Figure 2.2. The magnetic field configuration for a circular planar magnetron cathode. [2]

2.2 Materials Characterization Techniques

2.2.1 Transmission Electron Microscopy

Transmission electron microscopy (TEM) is a microscopy technique where electron beams are transmitted through an ultra thin specimen, interacting with the specimen as it passes through. By focusing the electron beam, diffraction patterns can be measured from the microscopic region and often a single microcrystal is selected for this diffraction measurement. The images of the electron intensity emerging from the sample can be finally generated at the optics of electron microscopes. The configuration of TEM is very similar to a transmission light microscope, which including: light source, condenser lens, specimen stage, objective lens and projector lens. The only difference is the electromagnetic lens is employed for the electron beam instead of glass lenses for the visible light. (See Fig. 2.3)

The basic function of TEM is to take the images such as interfaces, dislocations and second phase particles. This is due to the diffraction contrast where the variations in the intensity of electron intensity emerging from the sample. More-ever, the images of columns of atoms can be achieved by using high resolution transmission electron microscopy (HRTEM), where the phase of the diffracted electron wave can be preserved and interferes constructively or destructively with the phase of the transmitted wave. High-angle annular dark field imaging method, which by increasing the scattering angles to minimize electron interference behavior, can

greatly enhance the quality of high resolution images of columns of atoms. In this thesis, we get some clear pictures of the interface of Ge (100) and STO (100) through HRTEM.

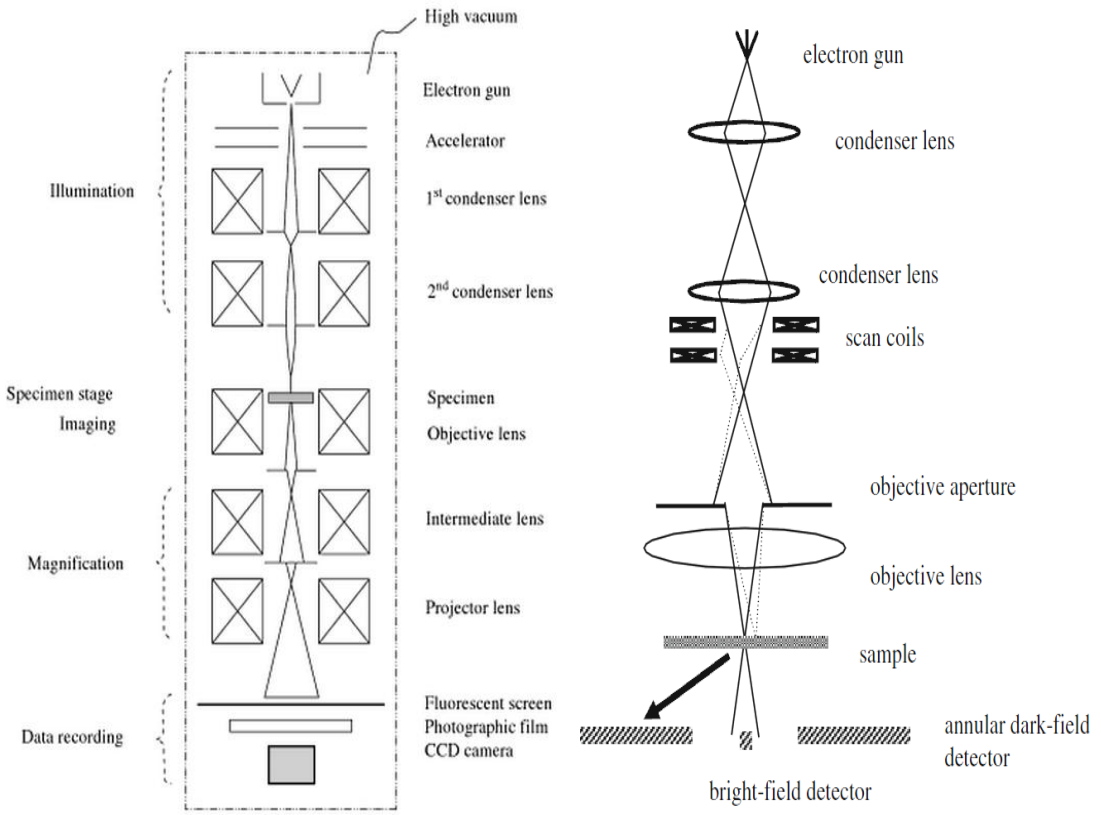

Figure 2.3. Schematic of TEM (left) and STEM (right) [3]

Besides the basic function of TEM, many modes are available for utilizing various measurements. Below are these techniques: [4]

- Conventional imaging (bright-field and dark-field TEM)
- Electron diffraction (selected area electron diffraction, SAD)
- Convergent-beam electron diffraction (CBED)
- Phase-contrast imaging (high-resolution TEM, HRTEM)
- Z-contrast imaging

- Energy-dispersive x-ray spectroscopy (EDS)
- Electron energy-loss spectroscopy

Most of these techniques are useful in the mode of scanning transmission electron microscopy (STEM), where a 1 to 10 Å focused beam of electrons moves in a television style raster pattern across the target thin sample and the emitted data such as x-rays, secondary electrons and backscattered electrons can be acquired as the basic information provided for above mentioned techniques. (See Fig. 2.3) The transmitted electrons in the STEM can also be detected with a moving detector to serve the conventional TEM imaging. For instance, an image of the distribution of Fe in a thin sample can be measured in synchronization with the raster pattern. Besides this, either the emission of Fe Kα x-rays can be observed by EDS spectrometer or the numbers of transmitted electrons that undergo energy losses greater than that of the Fe L-edge can be detected from EELS spectrometer. In the STEM, Z-contrast is by using an annular dark-field detector for high angle annular dark-field imaging (HAADF) and HAADF is using incoherent elastic scattering of electrons to form images of atom columns. With the help of HAADF-STEM with EDX line-scan, we not only get the images of atom columns for the Ge (100) and STO (100) but also see the profiling of the different elements in Chapter 3.

2.2.2 X-ray Diffraction

X-ray diffraction (XRD) is versatile, non-destructive technique which reveals information about the crystallographic structure, chemical composition, and physical properties of materials and thin films. Fundamental principles of XRD comes from Bragg's law (see Fig. 2.4), which states general relationship between the wavelength of the incident X-rays, angle of incidence and spacing between the crystal lattice planes of atoms in equation: $n \lambda = 2d \sin\Theta$. This theory determines the scattering angles at which the peaks of strong scattered intensity may occur and can be the direct evidence for the periodic atomic structure of crystals postulated for several centuries.

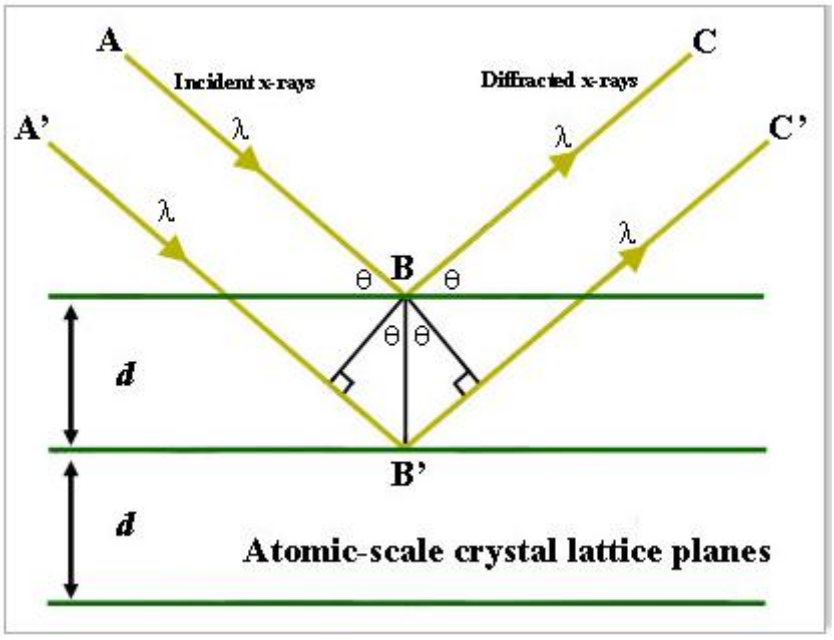

Figure 2.4. Bragg's Law reflection. The diffracted X-rays exhibit constructive interference when the distance between paths ABC and A'B'C' differs by an integer number of wavelengths (λ)

The basic structure of an X-ray diffractometer consists of three elements: an X-ray

tube, a sample holder, and an X-ray detector. Figure 2.5 is the schematic of a simple XRD. X-ray is generated at X-ray tube through the collision between high-speed electrons and a metal target (Cu, Al, Mg or Mo). Generated monochromatic X-rays collimate and direct go onto the sample material at holder. The holder and the detector keep rotating to record the intensity of the reflected X-rays from different location of sample. Diffraction occurs only when Bragg's Law is the satisfied condition for constructive interference. Therefore, only the geometry of the incident X-rays reflects the sample under this condition, constructive interference occurs and a peak in intensity occurs. After the data collection, X-ray signals are converted to the count rate which is then output to a device such as a printer or computer monitor.

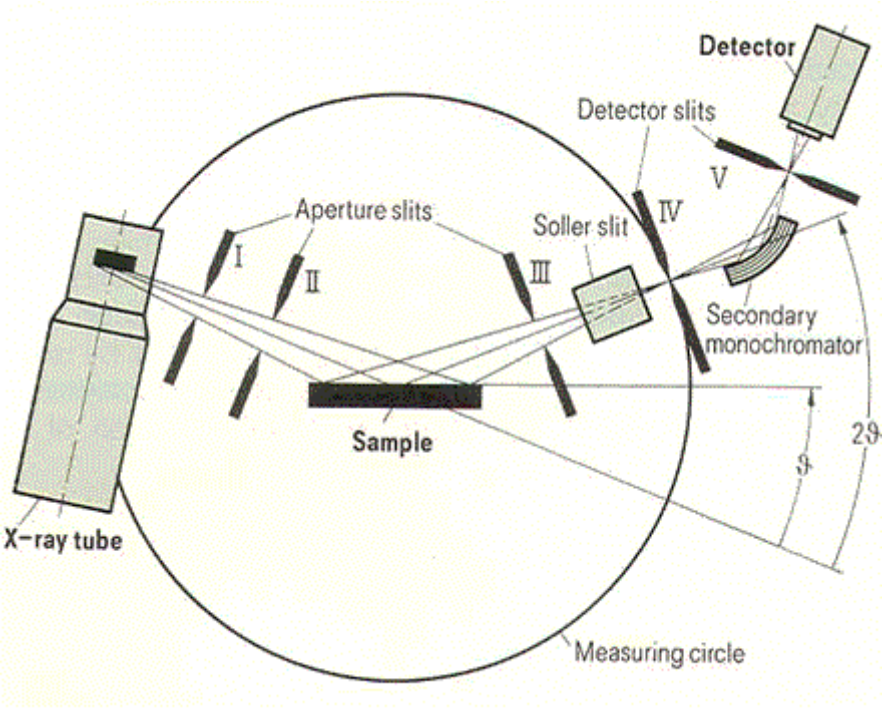

Figure 2.5. Schematic of a Powder X-ray diffracto=meters

One of the most important applications of XRD is to measure the thin film parameters in semiconductor manufacturing even with the thickness less than 2nm. For example,

the proportion of crystallinity in films that is nominally amorphous, the composition of the crystalline components of the material, the grain size of a crystalline material, the stress in a crystalline material and the distribution of crystallite orientations within a polycrystalline material. [5] In this thesis, the thin film sample morphology is characterized by high resolution x-ray diffraction (XRD, PANalytical X'Pert PRO MRD XL)

2.2.3 X-ray Photoemission Spectroscopy

X-Ray Photoelectron Spectroscopy (XPS), also called Electron Spectroscopy for Chemical Analysis (ESCA), is a high-energy version of the photoelectric effect based spectroscopic technique. [6, 7] It is primarily designed for identifying the chemical elements at the sample surface except hydrogen and helium. Because the diameters of these orbitals are too small, reducing the catch probability to almost zero. Current XPS technique give the allowance to measure many properties of materials, e.g. elemental composition of the surface (top 1–10 nm usually), empirical formula of pure materials, elements that contaminate a surface, chemical or electronic state of each element near the surface, uniformity of elemental composition across the top surface (or line profiling or mapping) and uniformity of elemental composition as a function of ion beam etching (or depth profiling).

The working principle can be illustrated at below Fig. 2.6. Incident X-rays with 1000 – 2000 eV energy hit the sample and eject photoelectrons from it. According to one-electron model and the conservation of energy, the measured energy of the ejected photoelectrons at the spectrometer, $E_{kinetic}$, can be related to the binding energy of the electron $E_{binding}$ and X-ray photons energy E_{photon} in the equation 2.1.[8]

$$E_{photon} = E_{photon} - E_{binding} - \varphi + \psi \quad (2.1)$$

where φ is the work function of the analyzer, and ψ is the energy shift due to net surface charges of the sample. Fine tuned calibration will make – φ + ψ equal to zero. Electron binding energy is affected by its chemical surroundings which make XPS suitable to determine the chemical states in addition to the elemental identification. Also, XPS is less destructive and more surface-sensitive compared to other similar techniques.

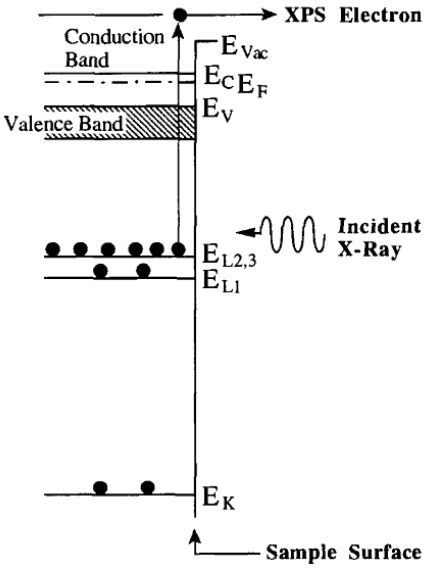

Figure 2.6. Electronic processes in X-ray photoelectron spectroscopy [9]

In this thesis, VG ESCA LAB-220i XL is the specified XPS to study the interface elemental states and chemical states between Ge (111) thin film and STO (111) substrate. We can see this XPS system in Fig. 2.7, which includes an X-ray gun in the UHV main chamber, a monochromator, an ion sputtering gun, a flood electron gun and an energy analyzer. The best energy resolution of this XPS system is about 0.45 eV, and the accuracy of the observed binding energy is within 0.02 to 0.03 eV.

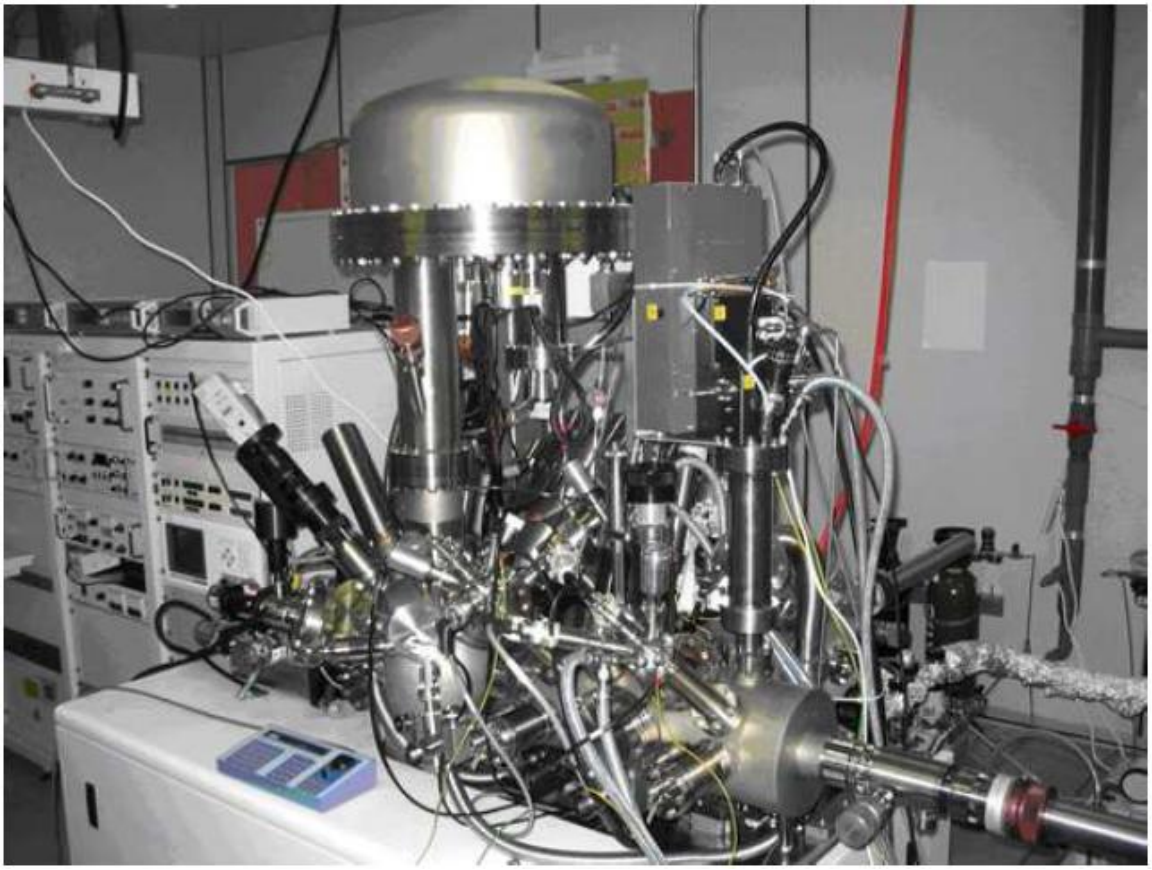

Figure 2.7. Overview of the VG ESCALAB 220i-XL XPS system.

2.2.4 Atomic Force Microscopy

Atomic force microscopy (AFM) is a scanning probe microscopy (SPM) technique based surface analytical method to generate very high-resolution images of a surface and provide some topographic, chemical, mechanical and electrical information about the sample surface. The AFM can examine any sufficiently rigid surface in air, liquid or even vacuum.

Fig. 2.8 is the basic schematic of a scanning AFM, where 1 is Laser diode; 2 is cantilever; 3 is mirror; 4 is position-sensitive photodetector; 5 is electronics; and 6 is scanner with sample. In the case of scanned probe, it is the tip that is scanned instead of the sample. By repeating the processes of measuring the forces acting on the sharp tip at cantilever (made from silicon or silicon nitride) through photodetector, the sample surface image can be drawn with very high resolution from 2D or 3D view. The forces available for the deflection of cantilever in AFM consist of mechanical contact force, van der Waals forces, capillary forces, chemical bonding, electrostatic forces and magnetic forces depending on the situations.

Many modes can be employed to suit for different applications in AFM, such as contact mode, lateral force microscopy, noncontact mode, dynamic force / intermittent-contact / “tapping mode” AFM, force modulation and phase imaging. In this thesis, normal contact mode is chosen to analysis surface roughness and

topographic of the grown Ge (111) thin film.

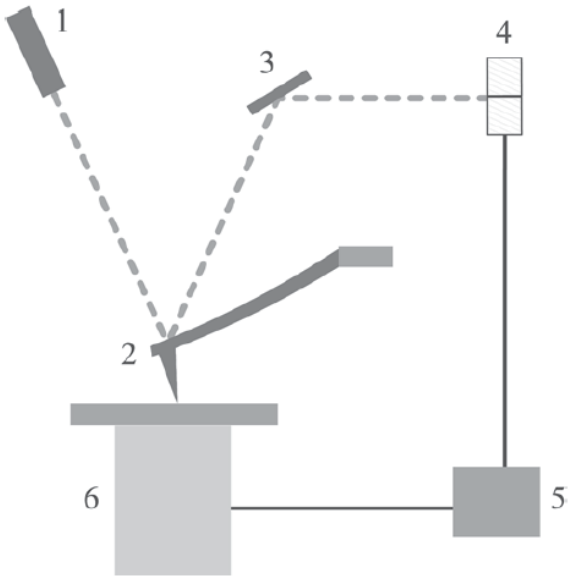

Figure 2.8. Schematic diagram of a scanned-sample AFM [10]

2.3 First-principles Calculations

First-principles calculation, or *ab initio* calculations, are the calculation methods to predict the atomic and molecular structure directly from the first-principles of quantum mechanics, without using quantities derived from input parameters.

The history of *ab initio* calculation begins with the basic fundamental of quantum mechanics, time-dependent Schrodinger equation of the many body system. [11]

$$\hat{H}\Psi = E\Psi, \tag{2.2}$$

where Ψ is the many body wavefunctions for the N electronic eigenstates, an anti-symmetric function of the electronic coordinates $\{\mathbf{r}_i : i = 1 \ldots N\}$, and E is the total energy. The Hamiltonian $\hat{H}$ is given by

$$\hat{H} = \sum_i -\frac{\hbar^2}{2m_e} \nabla^2_{\mathbf{r}_i} + V_{ext}(\{\mathbf{R}_I\}) + V_{e-e}(\{\mathbf{r}_i\}), \tag{2.3}$$

where V_{ext} is the external potential imposed by the nuclear configuration $\{\mathbf{R}_I\}$ and V_{e-e} is the electron - electron interaction given by the Hartree term $\sum_{j>i} \frac{e^2}{|\mathbf{r}_i - \mathbf{r}_j|}$.

Later in 1960s, Kohn proposed the famous density functional theory (DFT) which

makes an important process after the many body system. [12, 13] DFT theory basically includes two theorems for electron function ρ(r):

(1) If the number of electrons in the system is conserved, the external potential V (r) uniquely determines the ground state density $\rho_0(r)$.

(2) There exist a universal functional of ρ, E[ρ], which is minimized by the ground state density ρ_0 (r).

Within DFT, the many body problem of interacting electrons is presented to a reduced system of single-particle Schrodinger equations (Kohn–Sham equations). [13]

$$\{-\frac{1}{2}\nabla^2 + \int \frac{\rho(\mathbf{r})'}{|\mathbf{r}-\mathbf{r}'|}d^3\mathbf{r}' + \frac{\delta E_{xc}[\rho(\mathbf{r})]}{\delta\rho(\mathbf{r})} + V(\mathbf{r})\}\psi_i(\mathbf{r}) = \varepsilon_i\psi_i(\mathbf{r}), \tag{2.4}$$

where the first term in the Kohn-Sham equation is the kinetic energy, and the following terms are the Coulomb (or Hartree, or Electron to electron interactions), the exchange-correlation (xc) and the external (e.g. the ionic) potentials, respectively. Comparing with time-dependent Schrodinger equation of the many body system, this single-particle Schrodinger equations is much easier for the practical model and must be solved self-consistently (SCF, for self-consistent field) and iteratively.

Among all terms in Eq. (2.4), only exchange-correlation (xc) is an unknown function to solve this Kohn-Sham equation. To apply this DFT equation into real system, many

approximate formulas have been proposed for the exchange-correlation function. By considering data reliability and computational cost, local density approximation (LDA) is the most suitable assumption. [13,14-18] In the LDA, xc functional is reduced to a function of the local charge density that has been calculated accurately and interpolated using parameterized forms in Eq. 2.5.

$$\varepsilon_{xc}[\rho(\mathbf{r})] = \int \epsilon_{xc}(\mathbf{r})\rho(\mathbf{r})d^3\mathbf{r}, \tag{2.5}$$

where ε_{xc} is the exchange-correlation energy per electron.

In order to get a more accurate approximations, generalized gradient approximation (GGA) is proposed, which takes into account the gradient of the electron density (Eq. 2.6) comparing to the LDA with a homogeneous electron density in small region r. [19,20]

$$\varepsilon_{xc}[\rho(\mathbf{r})] = \int f(\rho, \nabla\rho)d^3\mathbf{r}, \tag{2.6}$$

For the system containing large amount of particles (around 10^{23} for solid), Bloch's theory and suppercell approximation are introduced. Bloch's theory is adopted in the system with electron moving in periodic potential. Suppercell approximation is useful for the system without periodic symmetry in all the three dimensions. For example, in the interface system in chapter 4, we build the model by constructing the periodically

separated supercells of GE/STO plus separated vacuum layers with thickness thicker than 10 Å. Typically, the supercells are chosen in such a way that they contain two interfaces that are equivalent in terms of stoichoimetry and geometry, to avoid electric fields due to unbalanced charges.

As this thesis is focus on the interface of semiconductor, pseudopotential approximation is an efficient approach, at which only the valence electrons responsible for the formation of the chemical bonds and determine the relevant low-energy physical properties of the system are thought to make the contribution to the system. The pseudopotential derived from solved self-consistently calculations for the isolated atom with an all-electron technique describes the effects of the nucleus and of the core electrons on the valence electronic states [21-25]. For periodic solids, a plane-wave basis set up to a certain kinetic energy cutoff is generally used to expand the single-particle electronic orbitals. Therefore, this pseudopotential approximation allows the expansion of electronic wavefunctions with much smaller number of plane-wave basis sets.

In this thesis, we use VASP (Vienna ab initio simulation package) [25, 26] and CASTEP (Cambridge serial total energy package) [27] as the first-principles calculations codes. Both the codes belong to DFT scope and applying the ultrasoft pseudopotentials or the PAW method and a plane wave basis set.

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Chapter 3

Experimental Study of Ge Thin Films Growth on $SrTiO_3$

3.1 Introduction

The integration of Ge channel to the Si substrate is of the current research and development (R & D) interest for a number of future silicon technologies. As mentioned from previous chapter, the conventional method of direct Ge deposition on Si substrate through heteroepitaxial growth will cause the diffusion of Si into the Ge layer at high temperature and the formation of an undesirable thick SiGe layer during the annealing process. To avoid such critical problem, we can use a single crystalline oxide as a buffer layer between Ge and Si (GeOI fabrication). Up-to-date GeOI process approaches have been reviewed in chapter 1, and the drawbacks of them are high associated cost and the complex process. Therefore, we need to find a cost-effective way to build GeOI structure by choosing some more suitable candidate high-k material and deposition method.

Among various high-K oxide materials, $SrTiO_3$ (STO) is known for its excellent insulating properties, such as large band gap, high dielectric constant, good mechanical properties, and high thermal stability. In particular, the lattice constant

mismatch between STO (100) and Ge (110) is very small, about 2.3%. This indicates that in principle it is possible to epitaxially grow high quality Ge thin films on STO (100) substrate or buffer layer. The growth of epitaxial layer of STO on the top of Si substrate with TiO_2-SrO-Si structure has been widely reported [1], which makes the integration of Ge on Si wafer through STO buffer layer feasible. However, there have been limited studies on epitaxial growth of Ge on STO.

In this chapter, we report results of epitaxial growth of Ge on STO (100) substrate by using ultra-high vacuum sputtering. We found that the orientation of the deposited crystalline Ge can be controlled by varying growth parameters such as substrate temperature, which provides us a simple way to control the desired orientation of the grown Ge surface on STO substrate.

3.2 Experiment Details

Commercially available $SrTiO_3$ with (100) orientation was used in this experiment. The model of DC sputtering tool used was TORUS UHV SOURCE TM3U and the detail parameters can refer to the details as below. Single crystal Ge was used as target and the RF atom source from Oxford Applied Research (OAR) was employed as atomic oxygen source. The sample morphology was characterized by *ex situ* high resolution x-ray diffraction (XRD, PANalytical X'Pert PRO MRD XL) and *ex situ* High resolution transmission electron microscopy (HRTEM). The chemical composition was analyzed by *in situ* x-ray photoemission spectroscopy (XPS, VG ESCA LAB-220i XL).

STO (100) substrate (10×10×0.3 mm) was pre-cleaned using acetone and ethanol in an ultrasonic cleaner before the deposition. Then the sample was transferred into an ultra high vacuum (7.0×10^{-10} mbar) chamber and was thermally annealed at 600 ℃ for 20 mins to remove Carbon based contaminations. To minimize the undesirable oxygen vacancies of STO, the STO substrates were treated by using atomic oxygen source (Oxford Applied Research) with an oxygen partial pressure of 3×10^{-5} mbar at 300 ℃ for 30 mins. After the surface treatment, the STO substrates were *in situ* transferred into a DC sputtering system, of which single crystal Ge was used as the target to deposit Ge on STO with fixed argon partial pressure of 1.1×10^{-3} mbar and DC power of 100 W, respectively. The orientation and quality of the deposited Ge

were controlled by varying growth conditions such as sputtering time and substrate temperature in the range of 400 - 700 ℃. The post deposition annealing (PDA) was conducted for all samples at the temperature of 500 ℃ to reduce the threading dislocation density.

The samples with a deposition time of 6 mins were used to study interface properties by using high resolution x-ray photoemission spectroscopy (XPS), and the samples with a deposition time of 60 mins were used to study the epitaxial growth of Ge/STO heterostructure using high resolution x-ray diffraction (XRD) and transmission electron microscopy (HRTEM). Both the samples with deposition times of 6 mins and 60 mins are used to study the surface prosperities of grown Ge on STO substrate through Atomic force microscopy (AFM).

3.3 Results and Discussions

Ge thin films were deposited on STO (100) substrate at temperatures varying from 400 to 700 ℃ with fixed optimized argon partial pressure, and the crystalline structures of the grown Ge thin films were characterized by using high resolution x-ray diffraction. Fig. 3.1(a) shows the XRD θ-2θ scan results for the sample grown at the sputtering temperature of 500 ℃ for 60 mins. It clearly shows that the dominant peak is from Ge (111) plane besides sharp peaks of crystalline STO (100) substrate, indicating that the epitaxial relationship is Ge (111) || STO (100) for the grown Ge thin films on STO (100) substrate at 500 ℃. The inset in Fig. 3.1(a) is the Ge (111) omega peak, and the full width at half maximum (FWHM) of this peak is only 0.336 deg. This shows a good quality of the grown crystalline Ge (111) thin films. The in-plane rotation of these two sample are identified by the Phi (Φ) scan with in-plane directions of Ge [100] and STO [111], indicating that the rotation angle is 45 ° for all four peaks as shown in Fig. 3.2.

The XRD pattern shown in Fig. 3.1(a) is for the sample grown under higher substrate temperature (650 ℃) for 60 mins. Together with strong peaks from STO (100) substrate, Ge (400) peak is observed. This Ge (400) peak indicates the formation of Ge thin film with (100) orientation. Thus, at the substrate temperature of 650 ℃, the epitaxial orientation between Ge thin films and STO turns into Ge (100) || STO (001). The Ge (400) omega peak is presented in the inset of Fig. 3.1(b), the FWHM of which

is 0.420 deg, indicating the high quality of the grown Ge (100) thin films on STO (100) by using this sputtering process.

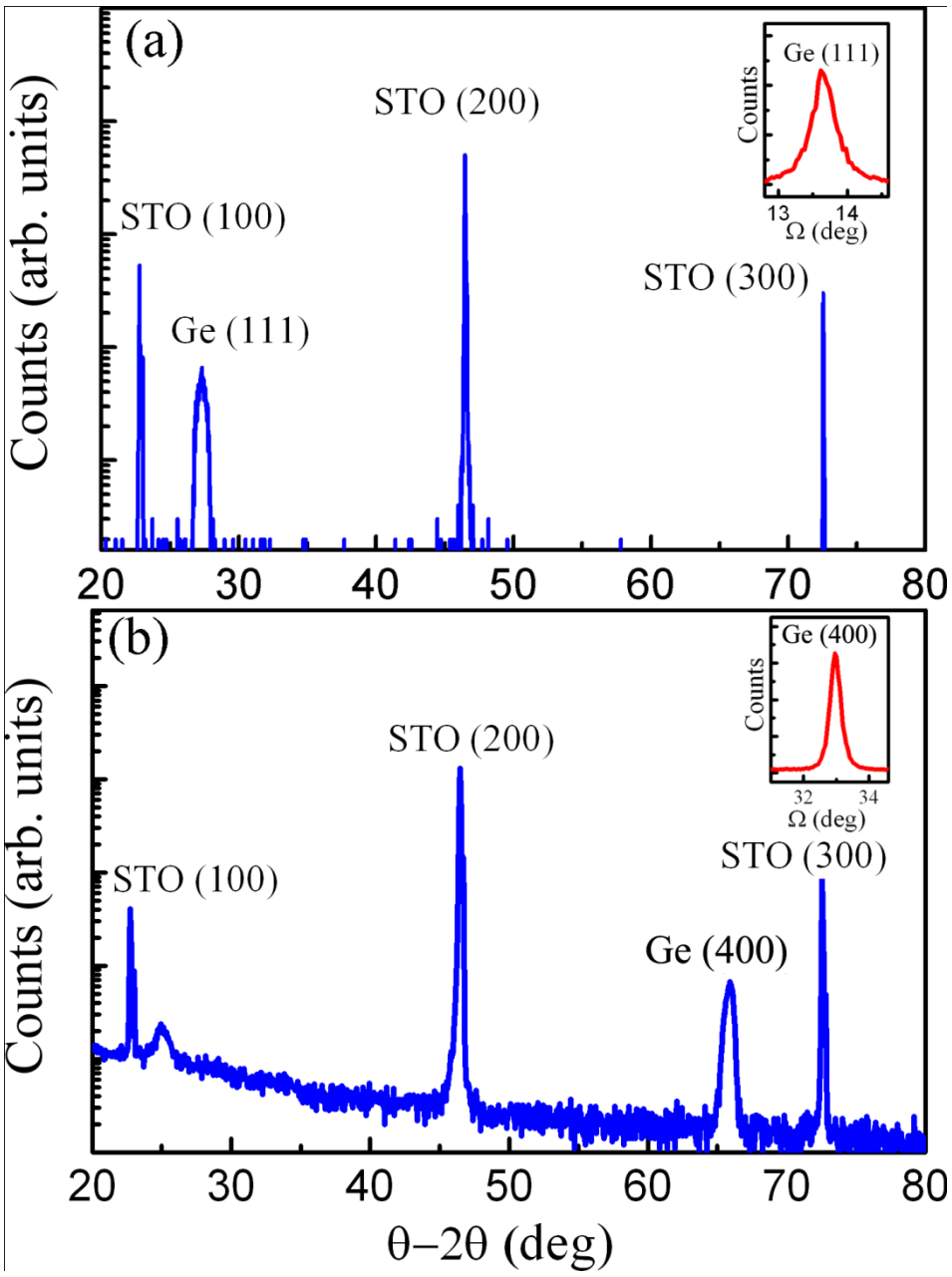

Figure 3.1. XRD θ-2θ scan of Ge films deposited on STO (100) at temperatures of (a) 500 ℃ and (b) 650 ℃, respectively. The insets show the ω peaks of (b) Ge (111) and Ge (400) peaks, respectively.

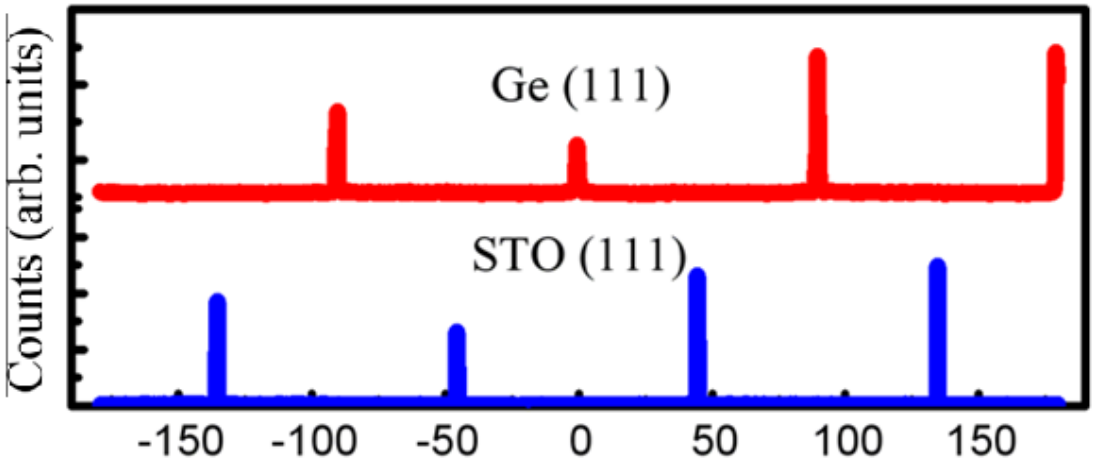

Figure 3.2. XRD phi (Φ) scans of Ge (111) plane and STO (111) plane for Ge sputtered on STO (100) at 500 ℃

These results are consistent with previous experimental results. For instance, Seo *et al.* [2] found the formation of Ge (111) thin films on La_2O_3 substrate at 400 ℃, while Bojarczuk *et al.* [3] reported epitaxial growth of Ge (100) on $(La_xY_{1-x})_2O_3$ at 650 ℃ by using molecular beam epitaxy. This change of preferred crystalline orientation from Ge (111) at 500 ℃ to Ge (100) at 650 ℃ results from the change of surface energy of Ge layers and interface energy between Ge layers and STO substrate at the initial growth stage at the different growth temperatures. For Ge, the most energetically favorable surface is (111) surface and (100) is the next most stable surface [4, 5]. At the lower substrate temperature, surface energy is dominant for the formation of surface orientation, thus at 500 ℃ Ge (111) is formed on STO substrate. At higher substrate temperature, the interface energy increases due to enhanced interaction between Ge and the substrate. Competition between the interface energy and the surface energy affects the orientation of the grown Ge thin films. When the interface energy dominates over the surface energy, it is possible for other surface

orientations such as Ge (100) to be formed on STO substrate. [6] Therefore, our results show that by carefully controlling the substrate temperature, we can manipulate the growth of the preferable surface orientation of crystalline Ge thin films on STO substrate by using sputtering.

To further study the epitaxial relationship between Ge and STO, high resolution transmission electron microscopy (HRTEM) images of the samples grown at 500 ℃ and 650 ℃ were taken and are shown in Fig. 3.3. It is clear in Fig. 3.3(a) that the well-defined Ge layers with good quality of crystallinity are formed on STO substrate, in good agreement with the XRD results. Besides, the interface of this heterostructure is very sharp, and transition from STO to Ge without any disoriented layers can be clearly seen. The line-scan of elements from scanning transmission electron microscopy (STEM) shown in Fig. 3.4(a) further confirms the high quality interface.

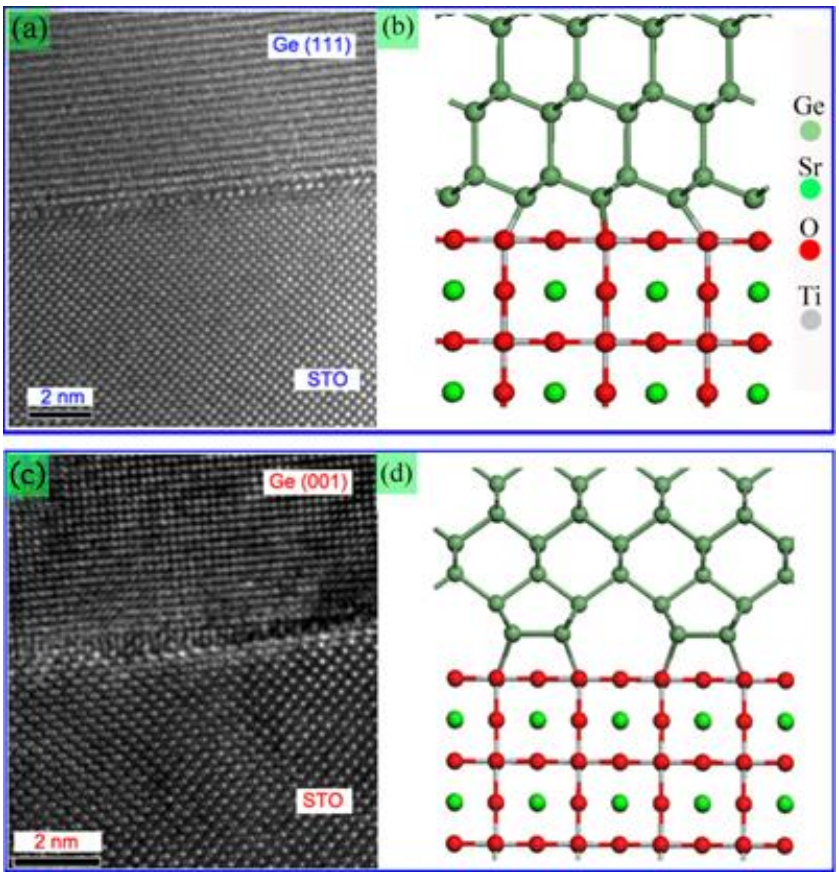

Figure 3.3. Cross section HRTEM images of the Ge films deposited on STO (100): (a) the formation of crystalline Ge (111) on STO (100) at the substrate temperature of 500 ℃, (b) a schematic interfacial atomic structure for Ge (111)/STO (100), (c) the formation of crystalline Ge (001) on STO (100) at the substrate temperature of 650 ℃, and (d) a schematic interfacial atomic structure for Ge (001)/STO (100).

To better understand the crystalline interface of Ge (111) / STO (100), we propose a model for the atomic interface structure based on the orientation relationship between Ge (111) and STO (100), as shown in Fig. 3.3(b), in which $(2\sqrt{3}\times 3)$ Ge (111) surface was stretched by 9.4% and 2.3% respectively to match (3×3) STO (100) in surface symmetry and lattice constant. Figure 3.3(c) and (d) show the TEM images and proposed atomic interface structure for Ge (001)/STO (100), respectively. It is seen clearly from Fig. 3.3(c) that the epitaxial Ge thin films were grown on STO (100) substrate with good crystalline quality and sharp interface. A slightly disoriented layer

is found at the interface. This may attribute to mutual diffusion of interfacial atoms at high growth temperature. The orientation relationship in interfacial model of Fig. 3.3(d) is similar to that for STO (100)/Si (100). As mentioned above, the Ge (100) surface matches well with STO (100) both in surface lattice symmetry and constant (only 2.3% lattice mismatch). We believe that this small surface strain may facilitate the formation of Ge (100) on STO (100).

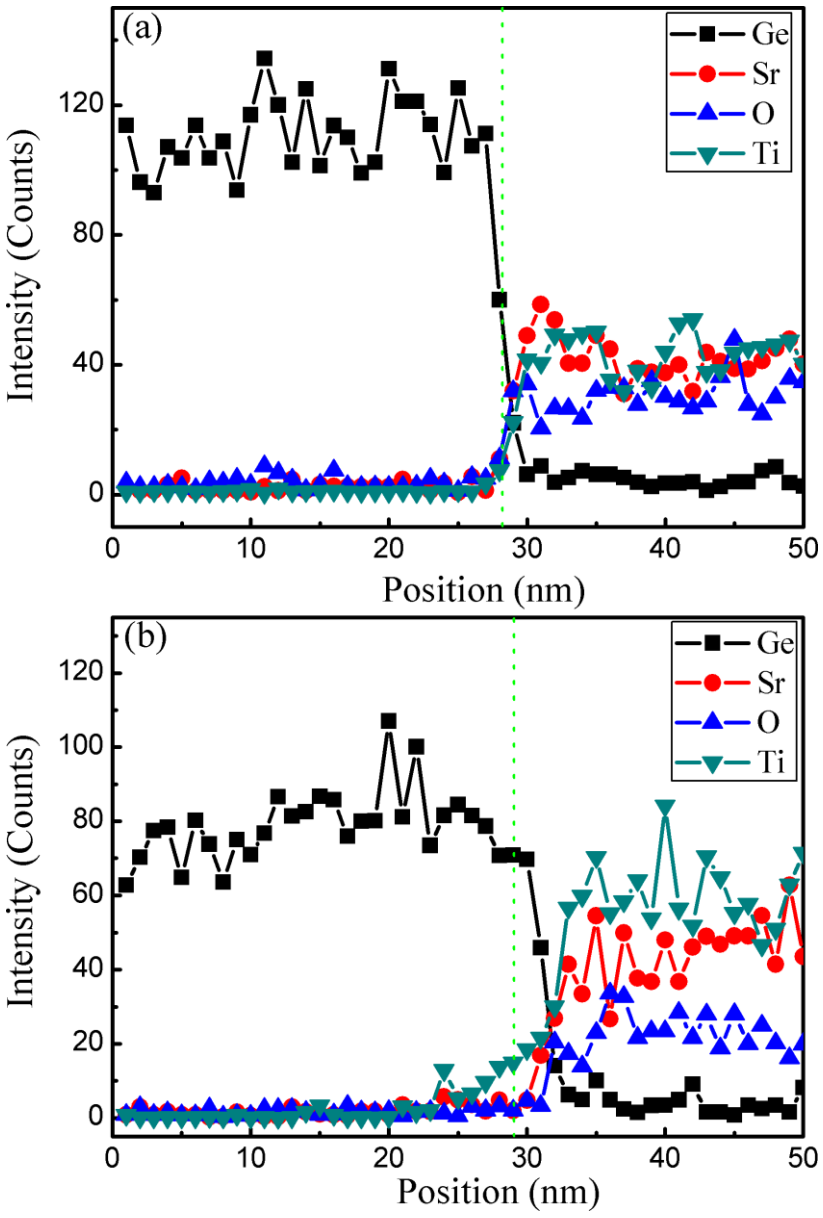

Figure 3.4. STEM EDX line-scan of interfacial chemical compositions for the Ge films on STO (100) at temperature of: (a) 500 ℃ and (b) 650 ℃. The vertical line indicates the position of the Ge/STO interface.

The interfacial chemical compositions of these samples have been studied also by using STEM with EDX line-scan, as shown in Fig. 3.4. At the temperature 500 ℃ (Fig. 3.4(a)), a small amount of Ge diffused into the STO. The phenomenon of Ge diffusion into high-K oxide layers has been well studied recently [7-9], and Ge oxide layers are often found at the interface. When the temperature increased to 650 ℃, more Ge would diffuse into STO substrate (see Fig. 3.4(b). At this high substrate temperature the STO (001) surface is Ti-rich, which indicates that the interfacial bonding of this sample is Ge-TiO_2. It is quite different from the interface of epitaxially grown STO on Si substrate. For the interface of STO (001)/Si (100), the STO (001) is also rotated 45 °in-plane to match Si (100) substrate, but it is found that SrO terminated interfacial bonding structures are more energetically favorable [10, 11]. This difference indicates different interface stabilities between Si/high-K and Ge/high-K oxide stacks due to different chemical reactivities of Ge and Si. As discussed above, Ge diffused easily into substrate even at the low processing temperature, which causes the decrease of electrical properties significantly. Thus, oxide layers such as STO are highly desired to serve as a buffer layer between Ge and Si to be effective barrier against Ge and other impurity diffusion.

In addition, Hall measurement was conducted for these samples to study the carrier type and mobility. The carrier in the sample at 500 ℃ is p-type with a measured

mobility of 36 cm2/V.s, while it becomes n-type with a mobility of 22 cm2/V.s for the sample at 650 ℃. Both n and p-type carrier concentrations are around ~10^{19} cm-3, which lead to the low mobility in both of samples. For the n-type Ge, it might be attributed to the lattice dislocation or Ge vacancy defect [2], and the diffused metal atom into Ge thin films might cause the detected p-type carrier.

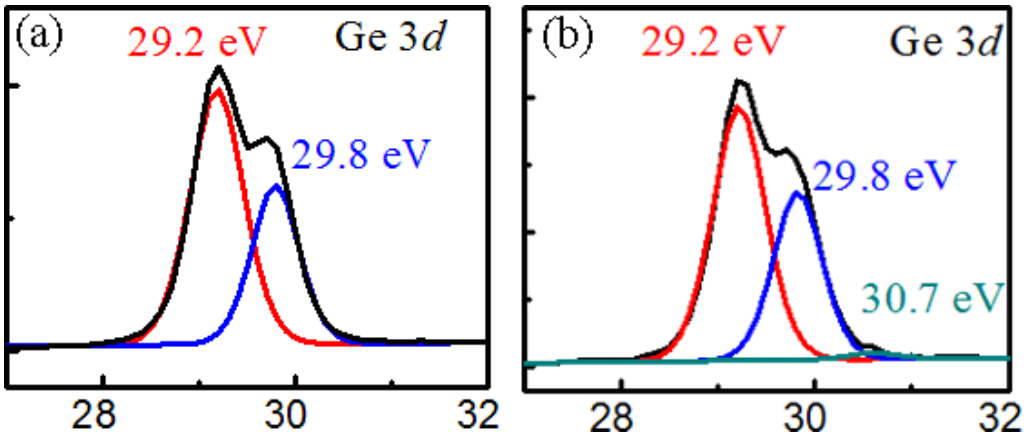

Figure 3.5. The XPS core-level spectra of Ge 3d for the Ge thin films grown on STO (100) with the deposition time of 6 mins and the substrate temperature of (a) 500 ℃ and (b) 650 ℃.

In order to have a profound understanding of chemical composition of Ge and STO at interface, high resolution *in situ* x-ray photoemission spectroscopy (XPS) study was performed. Figure 3.5 shows Ge *3d* core level peaks for the samples grown at 500 ℃ and 650 ℃, respectively. The charging effect induced by the photoemission was corrected using the C 1s as reference (284.50 eV). Fitting of the Ge *3d* core level to the Gaussian curves reveals two and three peak components for the sample with the substrate temperature 500 ℃ and the sample with the substrate temperature 650 ℃, respectively. The peaks at 29.20 eV and 29.80 eV in Fig. 3.5(a) come from the

elemental Ge doublets, which indicates the high resolution of our XPS system. No other Ge peaks were found. We can, therefore, conclude that there is no Ge sub-oxidation states formed at the interface of this sample prepared at the low temperature.

From Fig. 3.5(b), two peaks of elemental Ge doublets are also extracted from the data. In addition, an extra peak is found at 30.70 eV. The reported chemical shift of Ge^{1+} peak and Ge^{2+} peaks to the Ge 3d peak are 0.70±0.05 eV and 1.70±0.10 eV, respectively [12,13]. This extra peak at 30.70 eV indicates that there are Ge oxidation states at the interface, which are a mix of Ge_2O (Ge^{1+}) and GeO (Ge^{2+}) components. This result agrees well with the TEM images and STEM EDX line-scan for the interfaces. Therefore, the diffusion of Ge at high substrate temperature into the STO leads to the formation of Ge oxide layers at the interface.

It is well known that the growth of Ge on the epitaxial oxide is indeed of three-dimensional Volmer-Weber-type. According to the assumption from L. Largeaua and Patriarche *et al.* [13] that Ge NC present large contact angles (sometimes higher than 90°) and round profiles can indicate a large interfacial energy. Therefore, at the very early stages of Ge growth, Ge adatoms first nucleate and form localized platelets on the STO surface, due to large interface energy, three-dimensional mutually isolated Ge nanocrystals (NC) instead of continuous flat layer are formed at the surface of STO. It can also be proven from the HRTEM picture in Fig. 3.6. Ge NC`s contact

angles are not fixed by the stabilization of facets, but by the interface energy and the surface energies of the STO of the Ge platelets. The dimension of the NCs is about 20nm which also matches the report from Largeaua *et al.* [14], where the average lateral size is 25.2+/-11.6.

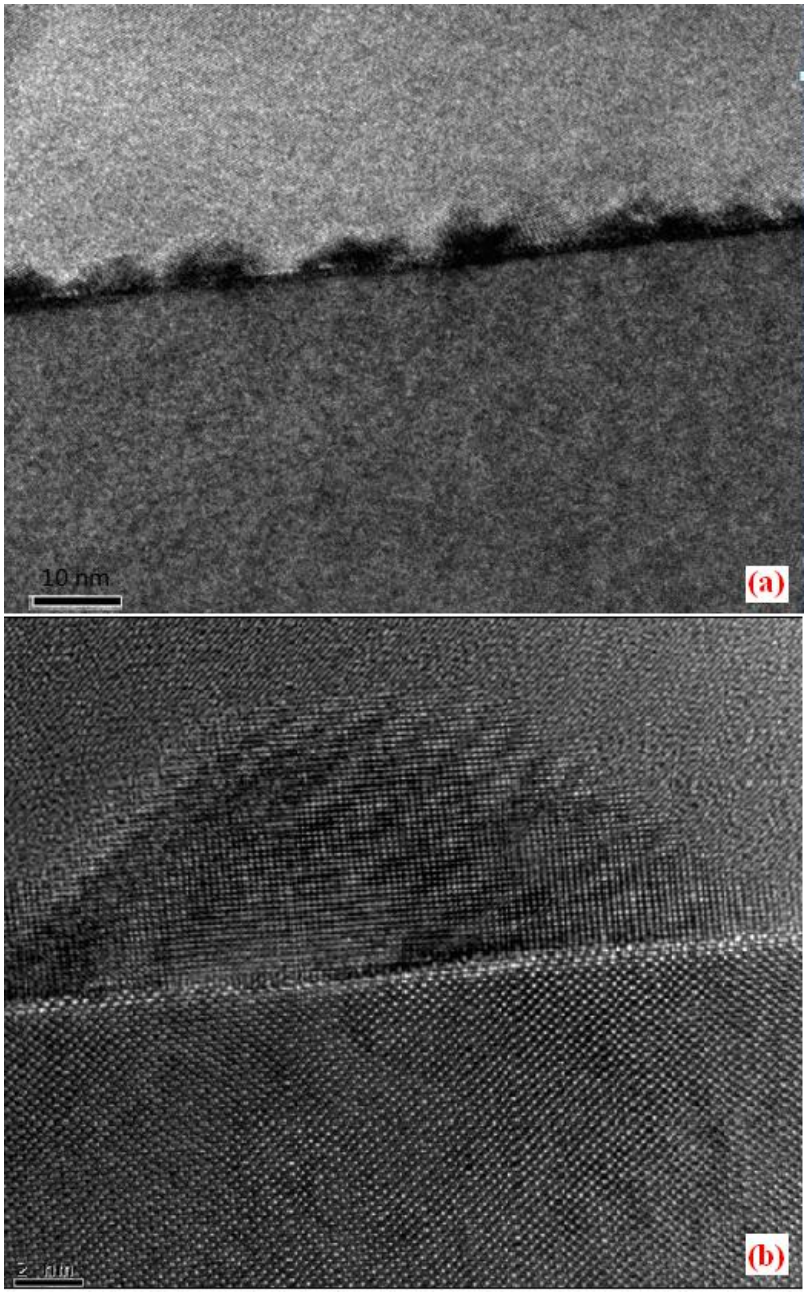

Figure 3.6. Cross section HRTEM images of the Ge films deposited on STO (100) at the substrate temperature of 650 ℃ for 6 mins: (a) 10nm scale, (b) 2nm scale

The surface properties of Ge grown at the surface of STO are also investigated through AFM. In Fig. 3.7(b), after 6mins deposition of Ge at the temperature of 500 ℃, we can see many round shaped NCs formed at the surface. The surface roughness is 5.471nm the density of NCs is around $3.68 \times 10^{12} cm^{-2}$. This high density and highly integrated NCs can be very useful for the application of floating-gate (FG) flash memory cells or so-called nonvolatile memory (NVM) technology, in which the use of discrete, mutually isolated NC's instead of continuous FG layers attracted more attention. Hence, uniformly distributed NC's with a sharp size distribution and a high density of 10^{12} cm^{-2} are generally targeted to guarantee manufacturability with sufficient storage capacity and high reliability. [15] Some reports have reveals the possible self-assembled Ge NCs system by Choi *et al.* [16-18]. From the result of high density up to 10^{12} cm^{-2} in this thesis, we can provide the alternative way to get the Ge NCs through simple direct sputtering.

In Fig. 3.7(a), we can see the round shape Ge NCs disappear after 60mins deposition. Some large Ge clusters are formed at the surface with the dimension up to several um but the roughness is as high as 47.094nm. The roughness is directly correlated with the coalescence of islands formed during the film growth. Thus, in order to obtain a flat Ge, the three-dimensional growth has to be suppressed and lateral growth needs to be promoted. Some reports have suggested taking a two temperature deposition method which uses high temperature to get single crystal Ge island followed by low temperature to laterally grow the Ge. [2, 19]

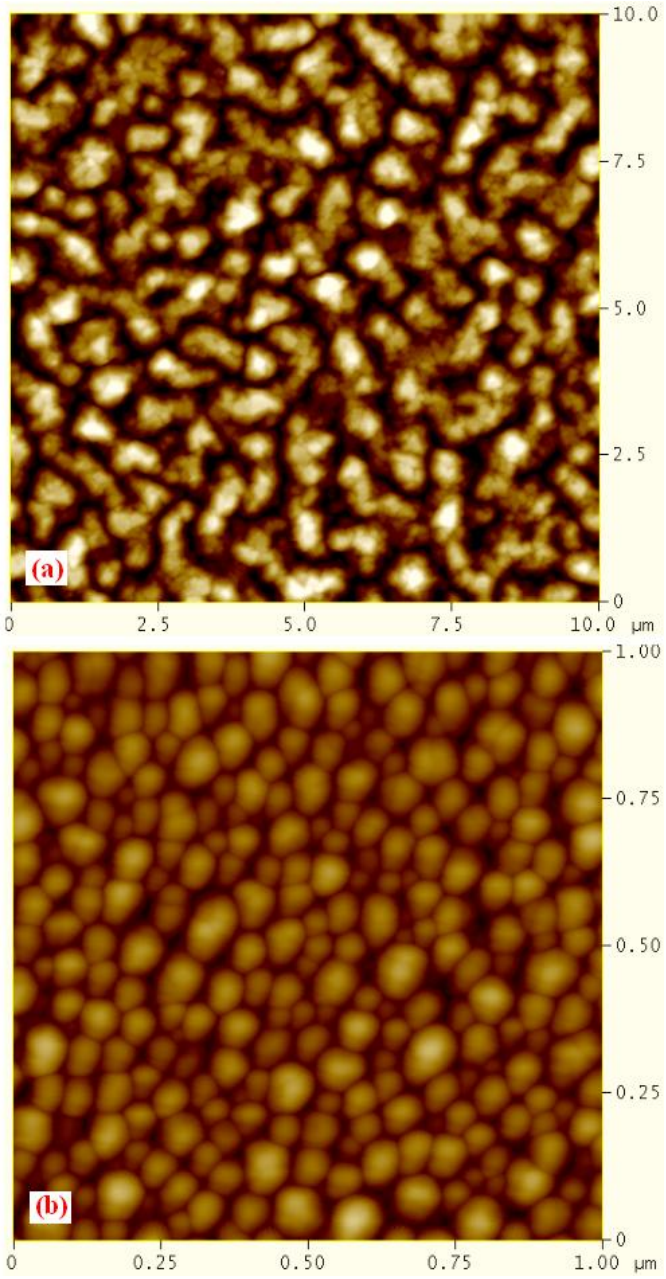

Figure 3.7. AFM images of the Ge films deposited on STO (100) at the substrate temperature of 500 ℃ for: (a) 60mins, (b) 6mins

3.4 Conclusions

In conclusion, high quality (100) and (111) oriented single crystalline Ge have been successfully grown on the top of $SrTiO_3$ (100) surface by using sputtering. We have shown that by varying the substrate temperature, two types of orientations of Ge can be selectively grown. At high temperature, the out-diffusion of Ge will cause the disoriented interface and the formation of Ge oxide layer. Our works demonstrate that $SrTiO_3$ has the potential in the application of the germanium on buried insulator field effect transistors. To better understand the interface between Ge and STO, in next Chapter, first-principles calculations will be carried out to study the interface satiability, and the related electronic properties.

3.5 Reference

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Chapter 4

First-principles Calculation Study of Interface Properties of $SrTiO_3$ and Ge

4.1 Introduction

In chapter 3, the crystalline Ge thin films with (100) or (111) surface orientation on $SrTiO_3$ substrate have been grown by sputtering and investigated experimentally. Besides this application of GeOI, high-k dielectrics material is very useful to be gate oxide for the Ge-MOSFET. In both cases, the interfacial structures between Ge and high-k oxides are of great importance for the determination of related electronic and electrical properties, and need to be theoretically studied.

Extensive studies have been carried out on the interface between STO and Si both experimentally and theoretically. [1, 3 – 6] For instance, STO can be epitaxially grown on Si with high quality and without the formation of silicon oxide transition layers. [1] The interfacial properties of $SrTiO_3$/Si have been studied by density functional theory calculations also, of which it was reported that the band offsets at $SrTiO_3$ and Si interface can be tuned to some extent by controlling interfacial chemical environment. [3, 6] But conduction band offset of $SrTiO_3$/Si is still too small, resulting in large tunneling current in MOS devices. [6, 7] The band gap of Ge is much smaller than that of Si, and thus the valence band offset between $SrTiO_3$ and Ge

may be increased. In addition, the lattice constant mismatch between Ge (110) and perovskite $SrTiO_3$ is small, about 2.3%, which is favorable for epitaxial growth of $SrTiO_3$ on Ge substrate. However, the understanding of the interfacial properties at $SrTiO_3$ and Ge is still limited, which is crucial to develop $SrTiO_3$ and Ge based electronic applications, as it has been pointed out that the different interfacial chemical bonding can dramatically affect electronic properties of the interface. [2, 8]

In this chapter, via first-principles hybrid functional calculations, we report results of interfacial properties of SrTiO3 on Ge substrate, of which the insulating Ge surface can be achieved by the passivation of either one Sr atom or two O atoms on per Ge unit cell with 2×1 reconstruction, and these different surface chemical environments do not have significant effects on the interfacial stability of $SrTiO_3$/Ge, but alter the related band offsets much. Besides, it is also found that the stability of the insulating $SrTiO_3$/Ge is insensitive to the applied external electric field.

4.2 Computational Details

All calculations were carried out by using Vienna *ab*-initio simulation package (VASP) [9, 10] based on density functional theory (DFT) with projector augmented-wave (PAW) method [11], in which the hybrid functional induced by Heyd, Scuseria, and Ernzerhof [12] was used for the exchange-correlation energy. A cutoff energy of 400 eV was used for plane wave expansion of electron wave function. For Ge primitive cell, the first Brillouin zone was sampled by a 10×10×10 k-point mesh within the Monkhorst-Pack scheme, and an 8×8×8 k-point mesh was used for bulk STO. For the interface structures, there are 6 layers of STO on (2×1) Ge (001) surface with 11 layers, in which dangling bonds at Ge bottom surface are saturated by H atoms and a 4×8×1 k-point mesh was applied. A 12 Å vacuum layer along (001) direction of the interface structures was applied to minimize surface interaction, and all structures were fully relaxed until the force acting on each atom was smaller than 0.02 eV/Å. In section 4.3.4, the electric field was applied along z direction by the planar dipole layer method integrated in VASP to study the electric field effects on interfacial properties. [13]

4.3 Results and Discussions

4.3.1 Ge and STO Bulks

The conventional approximations for exchange-correlation energy in DFT such as local density approximation (LDA) or generalized gradient approximations (GGA) often underestimate band gap of semiconductor or insulator. For instance, Ge, a well-known semiconductor with a bang gap about 0.67 eV, while in standard DFT calculation with LDA or GGA, it is gapless, which is a challenging issue as many related important electronic properties cannot be predicted well. An alternative approach is to mix a fraction of the non-local exact exchange to a semi-local exchange expression, which can produce an improved band gap in most cases. Here, we adopted HSE06 format hybrid function, which is based on PBEsol functionals calculation for the semi-local exchange and correlation part. [12] The calculated band gap using the hybrid functional is about 0.68 eV, in contrast with the zero band gap by LDA or GGA functional. The comparison for the GGA and hybrid functional calculated structural and band gap of Ge is summarized in Table 4.1, which clearly shows that the HF gives a better description of the structure and band gap for Ge.

	HF	GGA	Eexpriment
Lattice constant (Å)	$a = 5.672$	$a = 5.68$	$a = 5.67$
E_g (eV)	0.68	0	0.74

Table 4.1. Structural and electronic properties of bulk Ge.

The calculated lattice constant of cubic perovskite structure of STO is 3.91 ℃A, which is in good agreement with experimental results and previous calculations. [15, 16] The in-plane surface lattice constant mismatch between STO (001) and Ge (100) is only about 2.7%, resulting in a small interfacial strain to facilitate the crystalline growth. STO can be used for Ge-based electronics in two ways. One is to serve as a high-k dielectric, of which the first several STO layers are strained to match Ge lattice constant during the epitaxial growth process. The other is to be the substrate to grow Ge (GeOI), and in this case Ge is stressed. In this study, we focus on the epitaxial growth of STO on Ge (100) surface, in which the c-STO is in-plane strained with $a_{\parallel}=a_{Ge/\sqrt{2}}$=4.009 ℃A, and lattice constant c is contracted to 3.862 ℃A accordingly. This tensile strain on STO does not change its pm3m symmetry, but causes the reduction of band gap, as shown in Fig. 4.1(a). The HF calculated band for perovskite STO without strain is about 3.08 eV [20], close to experimental value (3.20 eV) [15], and this value is much improved compared with conventional GGA calculated band gap (1.97 eV). With the 2.7% tensile strain, the band gap is reduced to 2.74 eV, and the PDOS shows that this reduction is mainly from the down shift of Ti 3d orbital at the conduction band edge (Fig. 4.1(b)). It is noted that the strain induced band gap reduction has been found also in other systems such as ZrO_2/Si. [17]

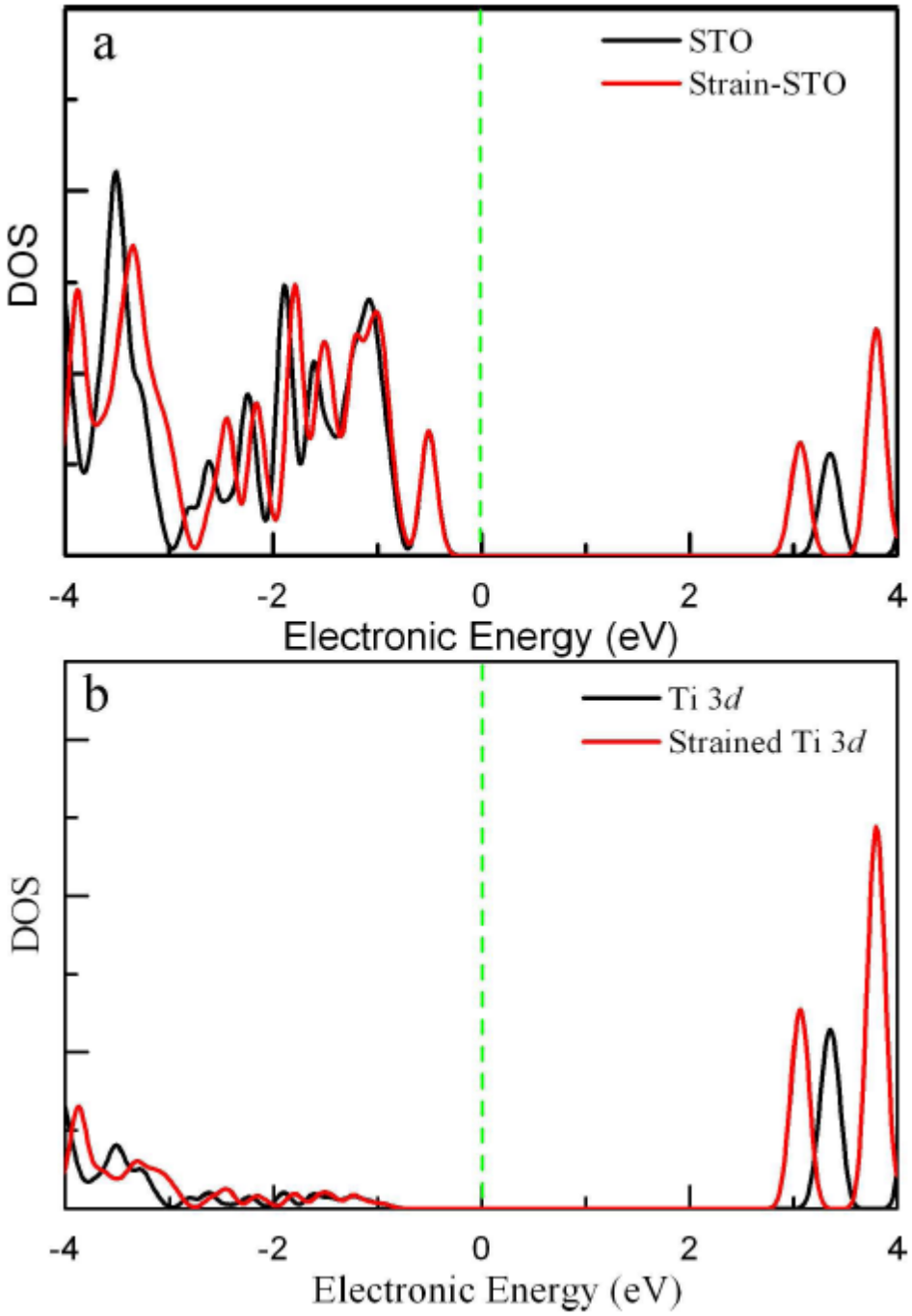

Figure 4.1. (a) Total DOS of STO with/without tensile strain. (b) Projected Ti 3d DOS of STO with and without strain.

4.3.2 Endogenous Passivation of Ge Surface

For Ge (1×1) (001) surface, there are two dangling bonds per atom at the surface originating from the discontinuity of periodic lattices. To minimize total energy, surface reconstruction is preferable. At room temperature, Ge (001) surface has a p-(2×1) reconstructed structure, in which the neighboring surface atoms form dimmers, resulting in decreased dangling bonds at the surface.

From the charge-neutrality view, the two dangling bonds at Ge p-(2×1) surface can be passivated by one Sr or O atom endogenously during the growth of STO, as shown in the inset of Fig. 4.2(a) and (b) shows, respectively. For Sr passivated Ge surface, electrons transferred from Sr to the Ge atom, making the Ge atom negatively charged, while for O passivated Ge surface, Ge is positively charged due to the stronger electronegativity of O atom, similar to the ZrO_2/Si interface. [17, 18] Fig. 4.2(a) is the calculated DOS of Ge surface passivated by a Sr atom, and as expected the surface states are fully removed with a gap about 0.28 eV. In contrast, when Ge surface is passivated by an O atom, the DOS (Fig. 4.2(b)) is cross over Fermi level, indicating a metallic surface. The relaxed surface structure shows that the Ge p-(2×1) surface structure was destroyed by the strong electronegative O atom, leading to two dangling bonds that induce surface states in mid gap. These two dangling bonds can be further passivated by one more O atom. The relaxed surface and the corresponding electronic structures are shown in Fig. 4.2(c), from which we can see that the Ge surface is well

passivated and recovers semiconductor character with a gap about 0.22 eV. In principles, these two more dangling bonds can also be passivated by the introduction of one more Sr atom (Fig. 4.2(d)), but the calculated DOS is metallic, which is attributable to strong repulsive interaction between Ge and large Sr atoms. Thus, to endogenously passivate Ge (001) surface effectively during the growth of STO, the introduction of one Sr or two O atoms per unit on Ge (001) surface is feasible.

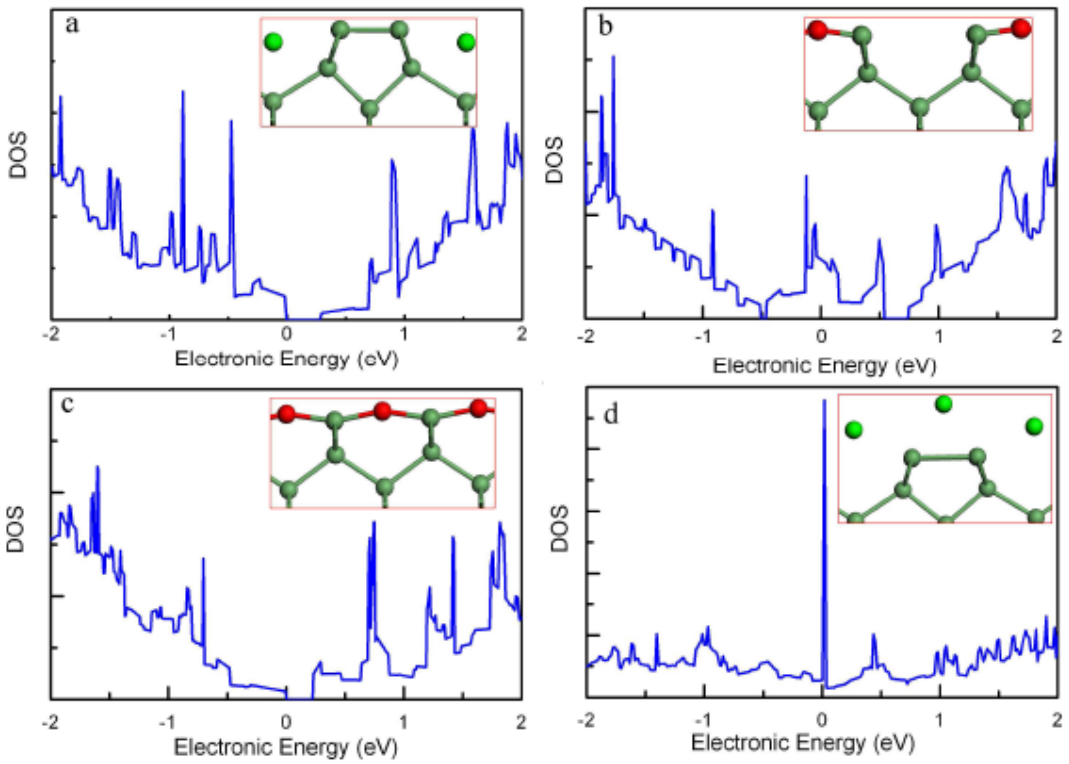

Figure 4.2. Total DOS of Ge surface passvitated by a Sr atom (a), a O atom (b), two O atoms (c), and two Sr atoms (d) (the insets are the corresponding atomic structures).

The relative stability of adatoms at Ge surface is given by the adsorption energy, and lower adsorption energy is related to a more stable adsorption configuration. The calculated adsorption energy for a Sr atom and two O atoms on Ge p-(2×1) surface is

about -1.18 and -12.79 eV, respectively. The lower adsorption energy means that the O passivated Ge surface is more stable. But, this low adsorption energy also suggests the favorable formation of Ge oxide on Ge, which is consistent with previous experimental results that Ge oxide layers are found to be easily formed between high-k dielectric and Ge due to the diffusion of O atom into Ge substrate or improper oxygen partial pressure. [19–21] Thus, during the passivation process, the oxygen chemical potential should be carefully controlled to avoid the formation of a thick Ge oxide layer, as it is well known that Ge oxide is not a good dielectric, which may decrease electrical properties of electronic devices severely.

4.3.3 Interfacial Structures and Stability of STO/Ge

For epitaxial growth of STO on Ge, there are many possibilities for the interfacial structures, even for direct stacking. Based on the interface of ZrO_2/Si, Robertson et al. proposed an interfacial bonding rule for insulator/semiconductor interface, which is a useful guidance to build possible interface structures. [18] For the possible interfacial structures of STO on a Sr or two O atoms passivated Ge (001) surface, due to transformation symmetry constrain, Ge, Sr or O atoms in the surface are within an irreducible triangle, which is consisted of Sr and O atoms for SrO terminated STO surface or Ti and O atoms for TiO2 terminated STO surface. Thus, for two O atoms passivated Ge (001) surface, we proposed 8 possible interfacial structures in term with different surface terminations (SrO or TiO2) of STO at the interface, and similarly, there are also 8 possible interface structures for STO with SrO or TiO2 termination on 1 Sr atom passivated Ge surface. All the interface structures are shown in Fig. 4.3 and Fig. 4.4, from which it is noted that there is no dangling bond in all interface structures. After relaxation, although each layer in STO and Ge surface are neutral, significant bonding relaxation is observed at the interfacial layers, due to the discontinuity of chemical environment and strong interactions between Ge and STO layers. At the middle layers the atomic bondings recover their bulk character.

For an interface structure, the stability is determined by its interface formation energy. Smaller interface formation energy is related to a more stable interface structure.

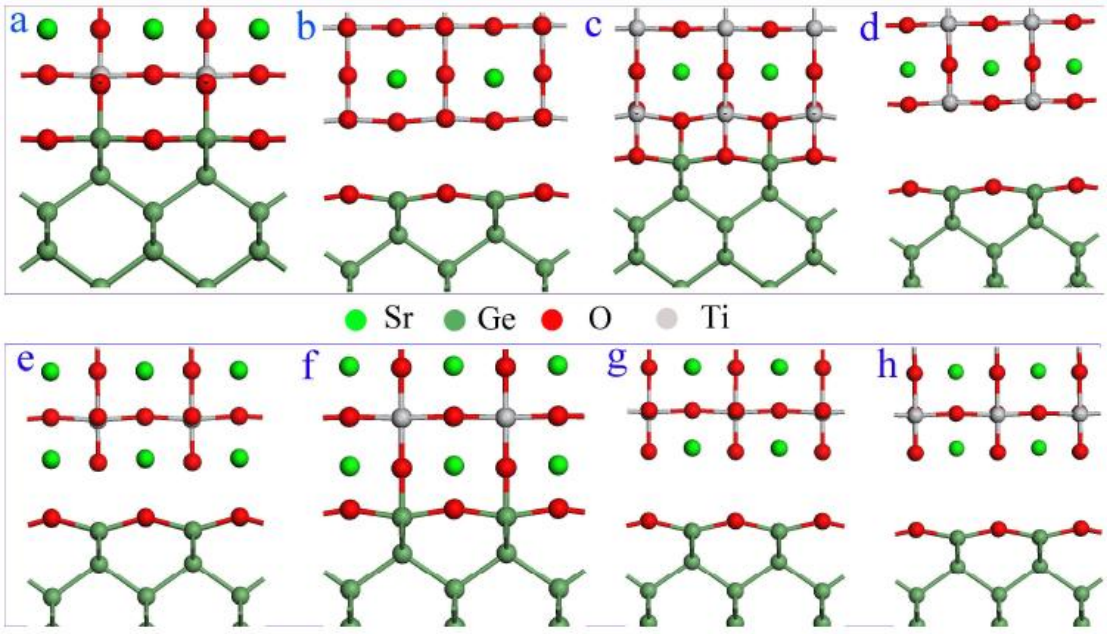

Figure 4.3. Interface structures for STO on Ge passivated by two O atoms

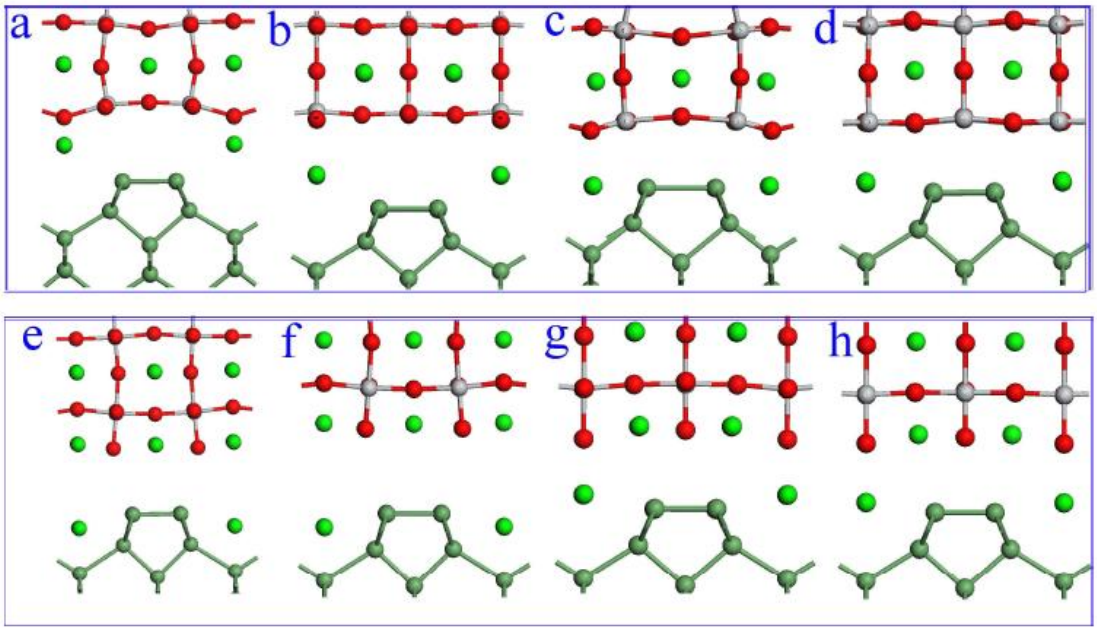

Figure 4.4. Interface structures for STO on Ge passivated by a Sr atom

For STO on Sr or O atoms passivated Ge surface, the related interface formation energy can be simplified as:

$$E_{form} = \frac{E_{total} - (E_{STO} + E_{Ge-passivated} + E_{others})}{A}, \tag{4.1}$$

Where E_{total} is the total energy of the interface slab, E_{STO} is the total energy of STO top layers, and $E_{Ge-passivated}$ is the total energy of passivated Ge surface, respectively. E_{others} includes the upper surface energy of STO and the energy related to the H atoms, and A is the basal area of the interface supercell. The calculated interface formation energies for all proposed interface structures are summarized in Table 4.2 and Table 4.3. For two O passivated Ge surface, the most stable interface structure among the structures we proposed is structure 3c, which is TiO_2 terminated STO on Ge (100) surface and is 0.24 eV lower than the next stable interface structure (3-e), as shown in the Table II. For Sr passivated Ge surface, the most energetically favorable interface is structure 4-a. It is also TiO_2 terminated STO surface on Ge, and has at least 0.47 eV energy over other interface structures. These results indicate that STO is preferable to form TiO2 terminated surface on Ge substrate, despite the different Ge surface chemical environments. In contrast, for interface structures of STO / Si, the most studied interface structure is SrO terminated STO on Sr passivated Si surface [3, 22], partially due to that the formation of metallic interface of Silicide is undesirable in real electronic applications, because when STO with TiO_2 terminated surface on Si, the metallic interface may be formed due to the diffusion of Ti atoms into Si substrate during the thermal annealing process. It is also reported the formation of Ti-Germanide in between metal and Ge by thermal annealing, but this Germanide does not decrease the electrical properties much. [8, 23]

	3-a	3-b	3-c	3-d	3-e	3-f	3-g	3-h
E (eV)	2.04	1.90	0.00	2.24	1.18	0.24	2.10	2.14

Table 4.2. Relative interface formation energy of STO on O passivated Ge (100).

	4-a	4-b	4-c	4-d	4-e	4-f	4-g	4-h
E (eV)	0.00	1.92	1.91	0.47	1.67	1.77	1.00	0.76

Table 4.3. Relative interface formation energy of STO on Sr passivated Ge (100).

4.3.4 Electronic Properties at STO/Ge Interface

The electronic structure of an interface structure is of great importance for applications. An interface structure with metallic character is undesired because this may result in large tunneling current. Moreover, the band offset between high-k oxide and semiconductor should be larger than 1 eV at least in order to minimize the standby leakage current. In addition, to reduce interfacial charge trapping density, the interfacial dangling bonds induced gap states should be minimized also.

Since the interface structure 3-c and 4-a is the most energetically favorable for Sr or O passivated Ge, respectively, the corresponding relaxed interface slabs were used to calculate electronic properties such as DOS and projected DOS (PDOS) on each atom. Figure 4.5 shows the calculated total DOS and PDOS of interface slab 3-c, of which the total DOS clearly shows semiconductor character of this interface structure. From the PDOS, it is noted that the PDOS of Sr, Ti, O, and Ge atoms at the middle layer of

the interface slab is similar to that in respective bulks, and the oscillation is mainly at the layers near interfacial region, consistent with the structural relaxation results. Similarly, there is no gap state of the DOS and PDOS for interface slab 4-a (Fig. 4.6), due to perfect interfacial bonding.

Band offsets at dielectric/semiconductor interface is an important quantity because they determine the tunneling chance for interfacial carriers. Lower band offsets are related to higher tunneling possibility, and thus larger leakage current. Since the valence band edge of STO is mainly from O 1s, the valence band offset (VBO) at the interface such as STO/Ge can be roughly estimated from the rigid shift of DOS of middle Ge 3d and O 1s atoms with their bulk counterparts. [24] The calculated rigid shift of DOS for the interface structure 3-c and 4-a is shown in Fig. 4.7 and Fig. 4.8, which clearly show that due to different interfacial net dipoles, the rigid shit of the core levels such as O 1s and Ge 3d between the interface structure and the bulk varies much. The VBO for the interface 3-c and 4-a is estimated to be 1.35 and 2.25 eV, respectively. It is noted that the different interface structures lead to the variation of the VBO, indicating the possibility of band offset tailoring by controlling the interfacial bonding, which is in agreement with previous studies. [3, 17] The band offsets at STO/Ge interface have been estimated to be 0.37 (CBO) and 2.0 eV (VBO) by Robertson et al. [25] by using charge neutrality level (CNL) method. The band offsets are slightly different with those we obtained, which may be attributable to the interfacial bonding effects including in our estimations.

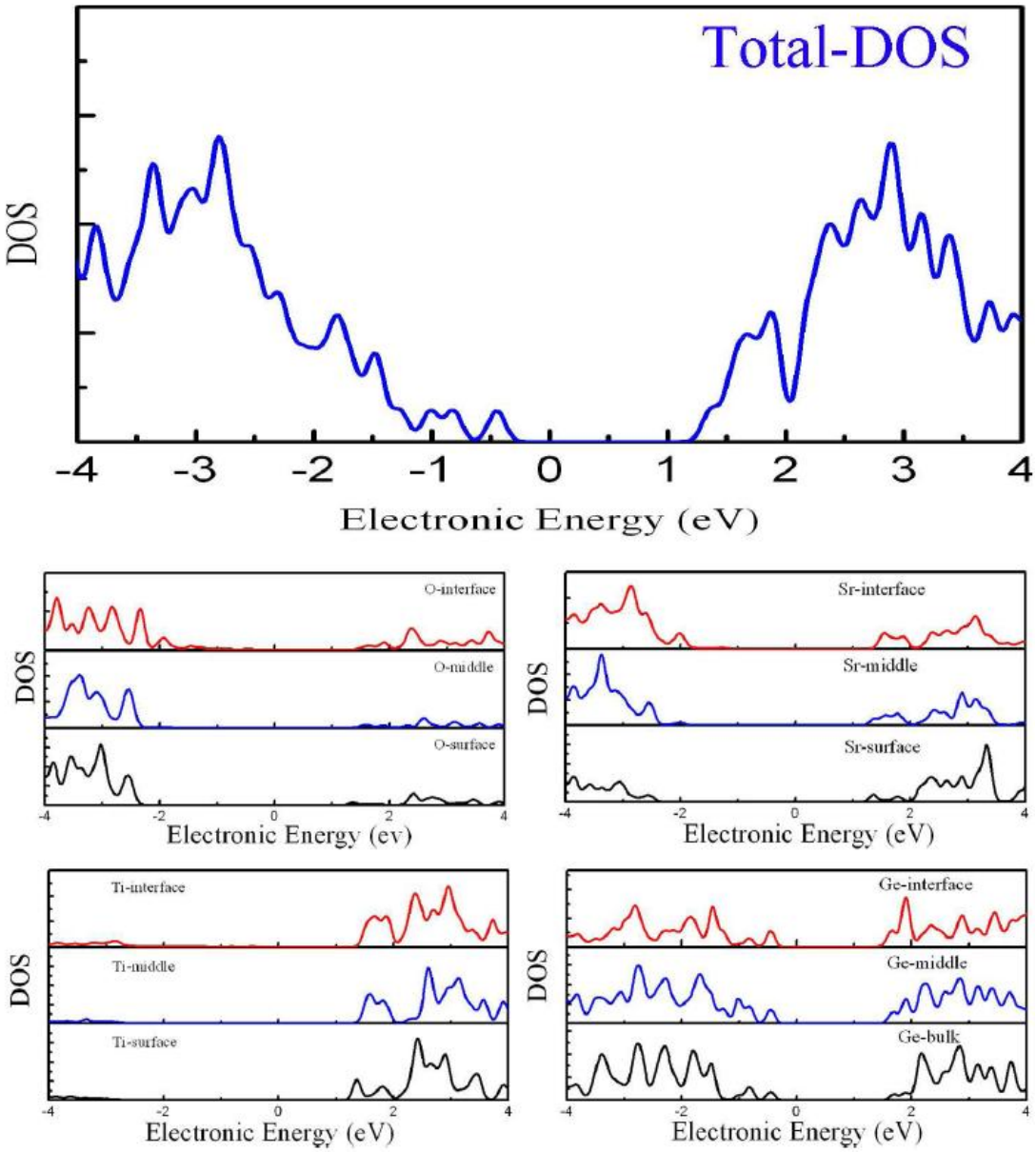

Figure 4.5. The total and projected DOS for the interface structure 3-c

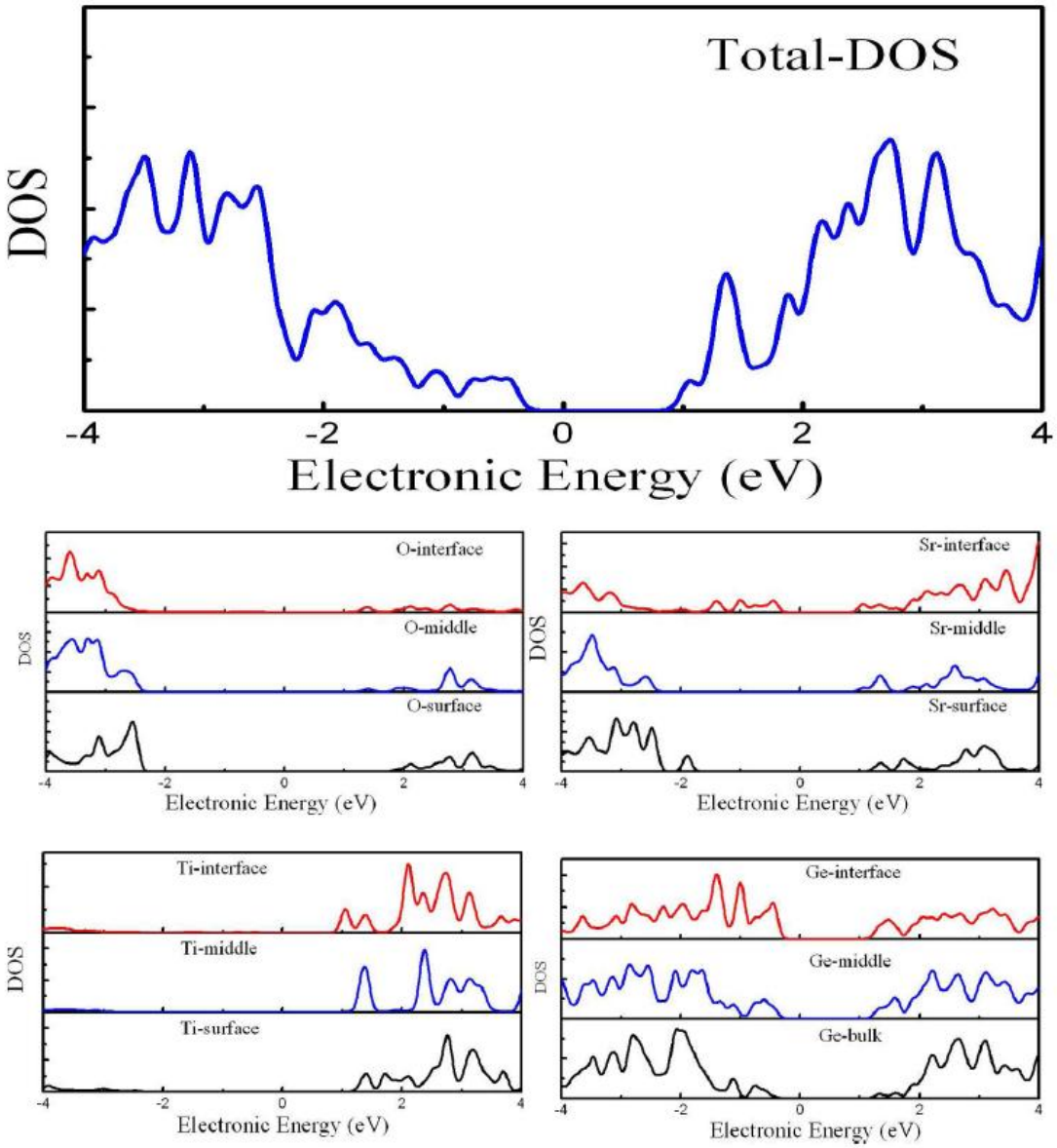

Figure 4.6. The total and projected DOS for the interface structure 4-a

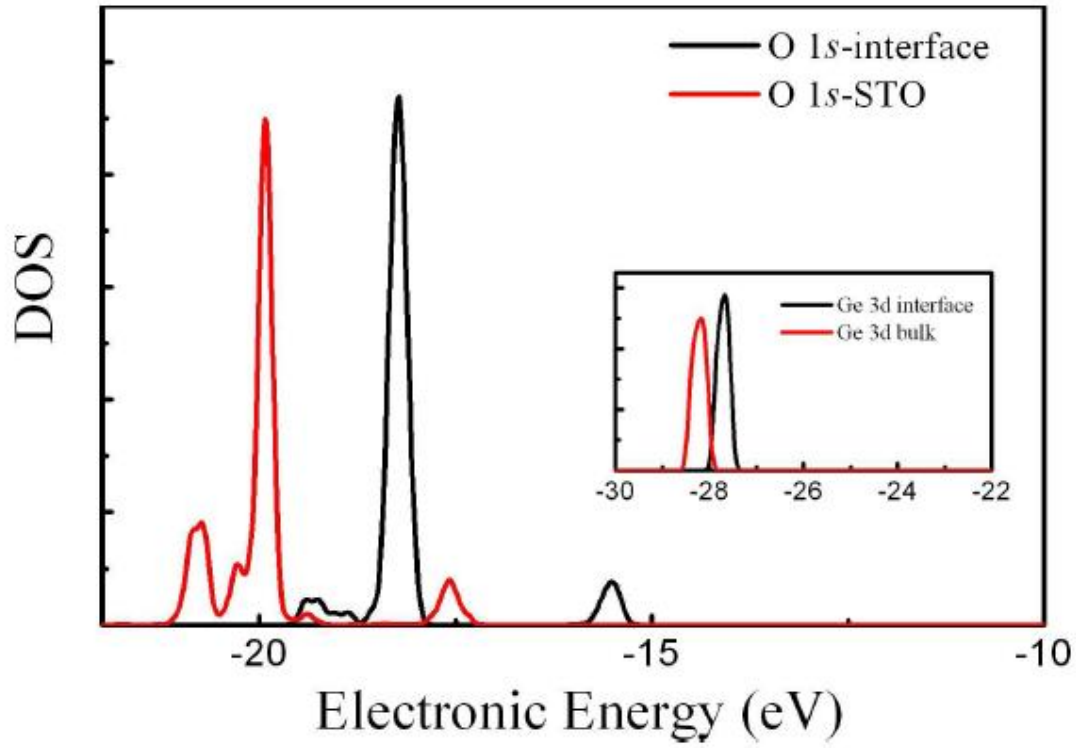

Figure 4.7. The rigid shift of O 1s and Ge 3d (inset) DOS between interface structure 3-c and the related bulk

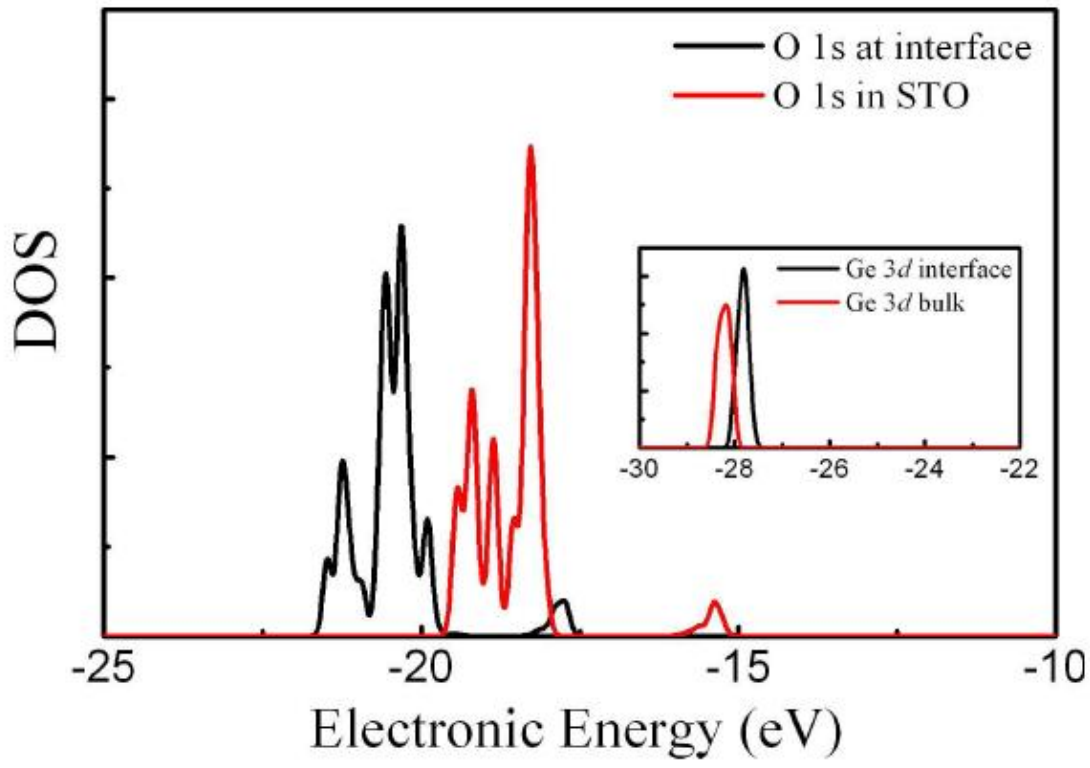

Figure 4.8. The rigid shift of O 1s and Ge 3d (inset) DOS between interface structure 4-a and the related bulk

4.3.5 Electric Field Effects on Interfacial Properties

Electric field has great effects on physical and chemical properties of materials at nano scale. For instance, the introduction of electric field can alter the absorption of molecules or clusters on oxide substrates, and it is also reported that electric field may change the magnetic properties of magnetic tunneling junctions. [26, 27] In this study, we applied external electric filed on the interface structures to examine the change interface stability. The calculated dependence of interfacial formation energy for the interface structures 3-c, 3-f, 4-a, and 4-d on the electric field is shown in Fig. 4.9(a) and (b), respectively. It is clearly seen that with the increase of electric field, all the four interface structures become more stable as their formation energy decreases, and the introduction of electric field does not change the relative stability of the interface structures. For example, TiO-3 is the most stable structure for STO on O passivated Ge (001) without electric field, and with 0.5 V/Å electric field, it is still the most stable. These results indicate that the insulating interface structure is robust against external influence.

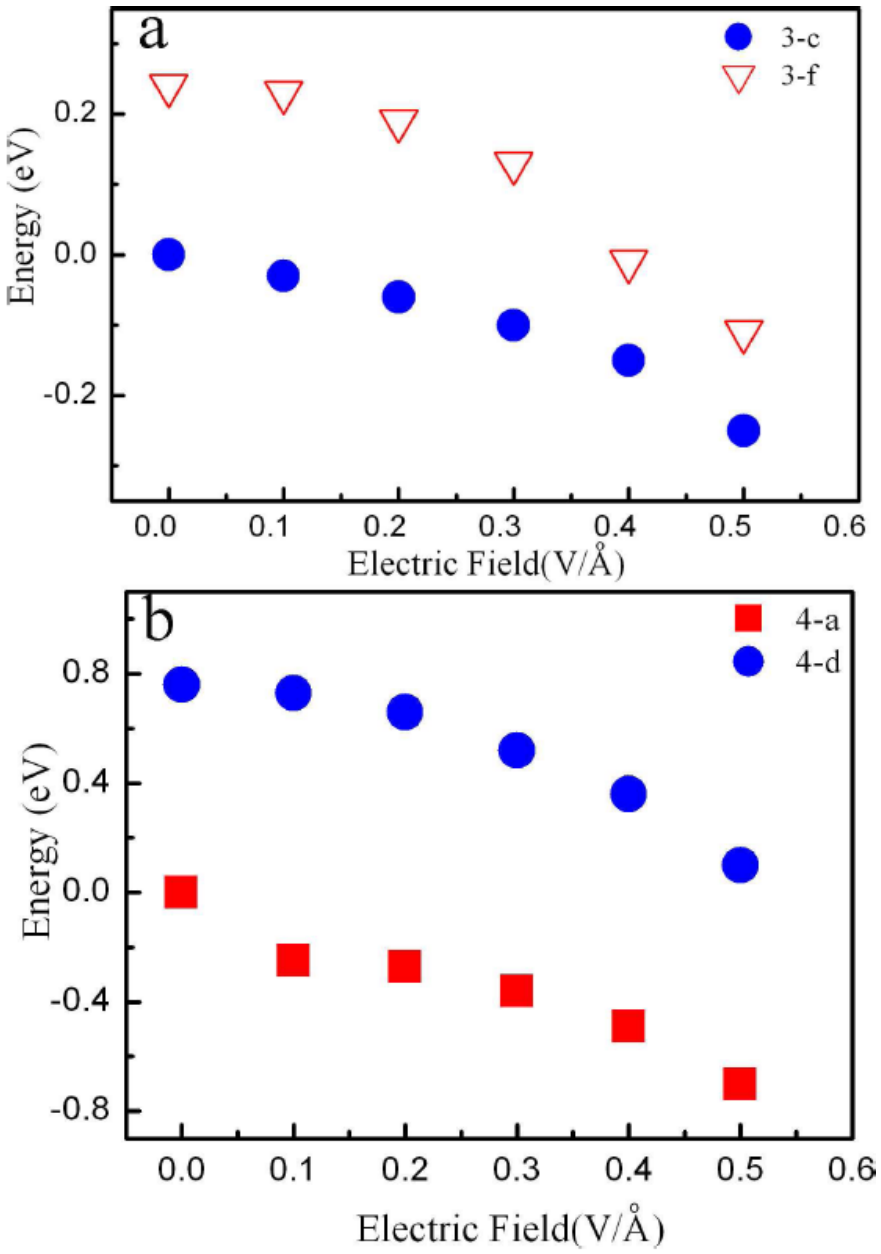

Figure 4.9. The dependence of interface stability on the external electric field: (a) interface structure 3-c and (b) interface structure 4-a.

4.4 Conclusions

In conclusion, we have used first-principles calculations to investigate structural and electronic properties of perovskite STO on Ge (001) substrate with the effects of different surface chemical treatments and external electric fields. It is found that the dangling bonds at Ge (001) (2×1) surface can be effectively passivated either by one Sr or two O atoms, and O passivated Ge surface is more stable, indicating high possibility of forming Ge oxide layers between Ge and STO. The calculated interface formation energy shows that STO terminated with TiO_2 is more preferably formed on Ge surface, and perfect interfacial bonding excludes the mid gap states, resulting in semiconductor like electronic properties. In addition, the relative stability among the insulating interface structures is insensitively with the applied electric field.

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Chapter 5

Conclusions and Future Works

5.1 Conclusions

The interaction of high mobility Germanium (Ge) layers with high-k oxides enables the possibility for the further scaling down of the MOSFET technology in the near future. This thesis mainly studies the interface properties of the high-k oxide materials ($SrTiO_3$) and the Ge through first-principles calculations and the experimental characterizations.

From the introduction and literature review chapter, many reports point out that the applications of high-k materials and high mobility Ge channel are two of the key elements to push the further downscaling of the MOSFET technology and IC industry. Integration of single crystaline Ge channel on top of the Si substrate encounters the difficulties to achieve both the high-quality Ge layer with defect free interface of Ge/Si by direct growth of Ge thin film on Si. Some researches have proven the GeOI fabrication through condensation technique and smart cut technique for both the chip and wafer level, but the cost is quite expensive. Single crystalline high-k dielectrics as the buffer layer has attracted bunches of interests recently. Within these high-k materials, LaYO and Sr(Hf,Ti)O3 have been widely reported. Before the application

of high-k in the GeOI for industry, more studies need to be carried on those potential materials and the deposition techniques. High-k material as the gate dielectric layer together with Ge-channel is the other very hot topic. For the Ge MOSFET in the sub-22 nm regime, both GeO_2 and GeON gate dielectric could introduce high leakage curren. Some groups have reported some high-k oxide on Ge substrate such as $SrTiO_3$, ZrO_2 and HfO_2 to replace the traditional gate dielectrics. These findings are still limited by the poor interface and the high leakage current due to the low quality high-k thin films. Therefore, further investigations are needed to find the other suitable high-k materials on Ge and their physical behaviours.

In the first half of the thesis, we focus on the experiment aspect of material growth and characterizations. A layer of single crystalline Ge (111) is successfully deposited on top of $SrTiO_3$ (111) at the sputtering temperature of 500 ℃. By ramping the substrate temperature to 650 ℃, single crystalline Ge (100) thin film show up at the same $SrTiO_3$ (111) substrate. The sharp Ge (100) and Ge (111) peak from XRD θ-2θ scan from both samples prove the good quality of the grown crystalline Ge. This phenomenon can be explains by the balance of surface energy of Ge layers and interface energy between Ge layers and STO substrate at the initial growth stage at the different growth temperatures. From the HRTEM pictures, sharp and defect free interface of Ge/Si can be clearly observed. Ge diffusion problem is caught by STEM with EDX line-scan, where higher temperature can lead to more Ge diffuse into the STO substrate. The other interesting finding from this STEM is that the interfacial

bonding of the Ge/STO interface is Ge-TiO_2, which is quite different from the Si-SrO interface boinding for Si/STO. XPS analysis also illustrate the existing of Ge_2O (Ge^{1+}) and GeO (Ge^{2+}) components caused by the Ge diffusion. Although the measured mobility is not very high for these samples, we expect further optimization of the experiment can achieve better results.

In the second half of the thesis, first-principles calculation is carried out to study the interfacial electrical structures of $SrTiO_3$ (100) and Ge (100). By employing the HSE06 format hybrid functional, we can get more accurate band gap of Ge (0.68eV) with 5.672Å lattice constant. The tensile strain is introduced in order to epitaxially grow STO on Ge (100) substrate, which can reduce the band gap of STO from 3.08eV to 2.74eV. One Sr or two O atom can be used to passivate the Ge p-(2×1) surface, and the O passivation is more favorable from the results of adsorption energy. Eight possible interfacial structures each in term with different surface terminations (SrO or TiO_2) of STO at the interface of one Sr atom or two O atom passivated Ge surface are proposed in this study. According to the formation energy definition, interface structure of $SrTiO_3$ with TiO_2 termination on Ge surface is more stable, which is consistent with the experiment results in chapter 3. The valance band offset estimated for these two TiO_2 terminated structure are 1.35 eV and 2.25 eV, respectively, which is based on the rigid shift of DOS of middle Ge 3d and O 1s atoms with their bulk counterparts. After we add in the external electric field, the formation energies decrease for all the possible structures, which can conclude that the relative stability

of the insulating interface structures is not affected by external influences.

5.2 Future Works

From the experimental aspect of fabrication of single crystaline Ge thin film on top of high-k material STO, there are two areas can be further improved and studied. Firstly, we can utilize double temperature steps Ge growth process to achieve both high quality and smooth Ge film on STO. This method is reported recently by some research groups for Ge/PrO2 and Ge/SHO. [1, 2] At the initial stage, high temperature can result high crystallinity Ge seed islands due to the three dimensional growth mode. Following by reducing the temperature, e.g. 300 ℃, the Ge growth rate can be lowered to about 0.01 nm/s, which is the two-dimensional growth mode. By combining and tuning these two growth stages, it is expected to get a atomically smooth and single crystalline Ge (100) or Ge (111) thin film.

Secondly, we can further fabricate Ge on insulater/high-k(STO) field effect transistor. After optimizing the Ge deposition on STO, we can easily build Ge/STO/Si stack as the technique of STO growth on Si substrate is well known. By simply doping the Ge film with boron and Si substrate with n-type dose, this GeOI heterostructure can be treated as the MOSFET, [3] where heavily doped Si is the bottom gate electrode and STO is the oxide (thickness can be controlled). Nearly all the characterizations of the

typical MOSFET can be carried on this similar Ge MOSFET and which can be very helpful for the future application in the foundry industry.

Both experimental and computational studies can be also carried out on effects of intrinsic and extrinsic defects in STO and Ge on electronic and electrical properties of Ge and STO based electronic devices. It has been reported that the defects in high-k oxides affects the electrical properties of Si based MOS devices significantly, which may induce large leakage current or cause Fermi Level pinning. The related study in high-k oxide and Ge is still needed in order to develop high performance Ge based electronic devices.

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