DESIGN OF A BROAD-BAND DISTRIBUTED AMPLIFIER AND DESIGN OF CMOS PASSIVE AND ACTIVE FILTERS

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2011

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Beng (Hons), NUS

A THESIS SUBMITTED

FOR THE DEGREE OF MASTER OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2011

ACKNOWLEDGEMENTS

The work described in this thesis could not have been accomplished without the help and support of many individuals.

First of all I would like to give my deepest gratitude to my supervisor, Assistant Professor Koen Mouthaan, for his guidance and encouragement throughout the two years. He helped me to overcome difficult problems whenever I got stuck during this period of time. Other than the academic progress he also helped me in my personal growth during the past two years.

I would also like to thank Mdm Lee Siew Choo, Mdm Guo Lin and Mr Sing for their help in the fabrication and the measurement of the microwave circuits during the past two years. Also I would like to thank Mdm Zheng for her technical support.

I am also thankful to all the friends in the MMIC lab who helped me during the last two years. I am truly grateful to Li Yong Fu, Hu Zijie, Azadeh Taslimi and Hu Feng for their help and technical support at various stages of the project. Also I would like to thank my brother Sandun Dalpatadu for providing support during the thesis writing.

Last but not the least I wish to thank my parents for bringing me up and for their forever love. I have always been learning to be more kind-hearted, patient, and optimistic from them.

TABLE OF CONTENTS

CHAPTER 1: Introduction 1

1.1 Broad-Band Amplifiers for RF Communication Systems 1

1.2 Broadband Amplification Techniques 3

1.2.1 Reactively matched circuit 3

1.2.2 Feedback Amplifier Configuration 4

1.2.3 Lossy Matched Amplifier Circuit 5

1.2.4 Distributed Amplifier Circuit 5

1.3 CMOS Technology for RF and Microwave Applications 7

1.4 Motivation, Scope and Thesis Organization 9

CHAPTER 2: Distributed Amplification Technique 11

2.1 Introduction 11

2.2 Gain Bandwidth Product of an Amplifier 12

2.3 Principle of Distributed Amplification 13

2.3.1 Power Performance of a Distributed Amplifier 17

2.3.2 Noise Performance of Distributed Amplifiers 18

2.3.3 Stability of Distributed Amplifiers 18

2.4 Theoretical Analysis on Distributed Amplifiers 19

2.4.1 Amplifier with periodically loaded transmission lines 19

2.4.2 Analysis of a distributed amplifier with discrete inductors 25

2.4.3 Cascaded four-ports formulation 27

2.5 Effect of FET Parasitics on Distributed Amplifier Performances 31

2.5.1 Effect of Gate-to-Source Capacitance 32

2.5.2 Effect of Series Resistance R_i when C_{gs} = 100 fF 33

2.5.3 Effect of Series Resistance R_i when C_{gs} = 200 fF 34

2.5.4 Effect of gate-to-drain capacitance when C_{gs} = 10 fF 35

2.5.5 Effect of Drain-to-Source Capacitance when C_{gs} = 10 fF and C_{gd} = 1.5 fF 36

2.6 Conclusions and Recommendations 37

CHAPTER 3: TRL Calibration and Measurement 38

3.1 Introduction....38

3.2 S – Parameter measurement....39

3.2.1 Vector Network Analyzer....39

3.2.2 TRL (**T**HRU – **R**FLECT – **L**INE) Calibration....40

3.3 Measurement of Active and Passive devices....47

3.3.1 Measurement of the transistor....47

3.3.2 Measurement of the passive devices....48

3.4 Conclusions and Recommendations....52

CHAPTER 4: Design of a Distributed Amplifier....53

4.1 Introduction....53

4.2 Circuit Realization....54

4.2.1 Bends, Meander Lines and T-Junctions....54

4.2.2 Stability Analysis....54

4.2.3 Schematic Design and Simulation....56

4.2.4 Electromagnetic Simulation Results....60

4.3 Measurement and Discussion....62

4.3.1 DC Measurement and Check for Oscillations....62

4.3.2 S – Parameter Measurement Results....63

4.3.3 Input 1-dB Compression point of the amplifier....69

4.4 Conclusions and Recommendations....69

CHAPTER 5: CMOS Active Filter Design....71

5.1 Introduction....71

5.2 Microwave transversal Filtering....72

5.3 Design of a CMOS lumped and transversal element filter 75
5.3.1 Filter Schematic Design 75
5.3.2 Schematic Simulation Results 77
5.3.3 Gain Compression of the Filter 79
5.3.4 Monte-Carlo Simulation Results 80
5.4 Layout Design and Post Layout Simulation Results 80
5.4.1 Standard 0.13 μm CMOS process 80
5.4.2 Layout Design 83
5.4.3 Post Layout Simulation 84
5.5 Measurement Results 85
5.6 Conclusions 89
CHAPTER 6: Microwave CMOS Passive Filter Design 90
6.1 Introduction 90
6.2 CMOS Lumped Element Filter Design 91
6.3 Filter Design 92
6.3.1 Calculation of Filter Element Values 92
6.3.2 CMOS MIM Capacitor Design 96
6.3.3 Filter Layout Design 97
6.4 Conclusions 102
CHAPTER 7: Conclusions and Recommendations 103
7.1 Distributed Amplifier Design 103
7.2 CMOS Active and Passive Filter Design 104
Appendix A 111
Appendix B 115

Summary

Broadband amplifiers are an important component in multiband radio systems and in optical receiver systems. Out of many existing topologies, the distributed amplification technique is an ingenious way of obtaining high bandwidths even greater than 100 GHz with good gain and return loss. Out of the two parts of this thesis, the first part addresses the design and implementation of a distributed amplifier on PCB. The concept of distributed amplification was deeply investigated and some of the limitations which degraded the performance of such amplifiers have been presented. The designed amplifier has a bandwidth of more than 3.0 GHz with a return loss better than 15 dB and a gain of 15 dB. Several issues encountered during design and measurement have also been addressed.

The second part of this thesis is mainly concerned with the design of CMOS passive and active filters. Due to the lossy nature of the silicon substrate the design of filters with a good return loss and a good pass band rejection is a challenge. The first design of the second project is related to the design of an active filter in 2-4 GHz. The proposed topology is based on lumped and transversal element filter topology, in which transversal elements are used to compensate the losses due to the substrate. In addition, these transversal elements are also used to improve the pass band rejection of the filter.

The second design addresses the design of a microwave passive filter at a centre frequency of 27.5 GHz. The proposed topology is based on the inverse Chebyshev filter prototype elements, in which inductors are designed using simple transmission lines. MIM capacitors are used to obtain the necessary capacitance values and, due to the inaccuracies of foundry provided models, capacitors were simulated in Sonnet EM simulator. The designed filter has a bandwidth of 7% at a centre frequency 27.5 GHz and a return loss of 8 dB.

LIST OF TABLES

Table 3.1: Calculated length of the TRL calibration kit..44
Table 4.1: Amplifier Design Specifications...56
Table 4.2: Optimized lengths and widths of gate and drain lines of the amplifier 57
Table 5.1: Active filter specifications 75
Table 5.2: 8th Order Chebyshev filter element values...75
Table 5.3: Low pass and high pass element values..76
Table 6.1: Passive filter design specifications..92
Table 6.2: Element values for the band pass filter structure 94
Table 6.3: Series parallel section element values...95

LIST OF FIGURES

Fig. 1.1 Multi-band and software defined radio systems. 2
Fig. 1.2 Fibre optic receiver system. 3
Fig. 1.3 Reactively matched amplifier. 3
Fig. 1.4 Feedback amplifier...4
Fig. 1.5 Lossy matched amplifier circuit...5
Fig. 1.6 Schematic diagram of a distributed amplifier circuit.................................6
Fig. 1.7 Microwave transversal filter circuit. 8
Fig. 2.1 Simple band pass amplifier structure. 12
Fig. 2.2 Schematic representation of a FET distributed amplifier. 13
Fig. 2.3 Small signal equivalent circuit of a FET. 14
Fig. 2.4 Equivalent circuit of a distributed amplifier. 14
Fig. 2.5 Schematic diagram of a traveling wave amplifier. 17
Fig. 2.6 Equivalent circuit of (a) gate line; (b) single unit cell of the gate line. 20
Fig. 2.7 Equivalent circuit of (a) drain line; (b) single unit cell of the drain line. 20
Fig. 2.8 Equivalent circuit of a DA with discrete components (a) gate line; (b) drain line. . 25
Fig. 2.9 A cross section of the distributed amplifier circuit 28
Fig. 2.10 Internal components of the four ports 28
Fig. 2.11 Individual components of the four port section (a) Transmission lines; (b) Y parameters of the FET; (c) transmission lines 29
Fig. 2.12 Small signal equivalent circuit of a FET. 31
Fig. 2.13 Effect of gate-to-source capacitance (a) $|S_{21}|$ (dB); (b) $|S_{11}|$ (dB); (c) $|S_{22}|$ (dB)....32
Fig. 2.14 Effect of Series Resistance R_i when C_{gs} = 100 fF (a) $|S_{21}|$ (dB); (b) $|S_{11}|$(dB); (c) $|S_{22}|$ (dB)..33
Fig. 2.15 Effect of Series Resistance R_i when C_{gs} = 200 fF (a) $|S_{21}|$ (dB); (b) $|S_{11}|$ (dB); (c) $|S_{22}|$ (dB)..34
Fig. 2.16 Effect of gate-to-drain capacitance when C_{gs} = 10 fF (a) $|S_{21}|$ (dB); (b) $|S_{12}|$ (dB); (c) $|S_{11}|$ (dB); $|S_{22}|$ (dB)..35
Fig. 2.17 Effect of Drain-to-Source Capacitance when C_{gs} = 10 fF and C_{gd} = 1.5 fF (a) $|S_{21}|$ (dB); (b) $|S_{12}|$ (dB); (c) $|S_{11}|$ (dB); (d) $|S_{22}|$ (dB) 36
Fig. 3.1 Block diagram of a N-port vector network analyzer [59]. 39
Fig. 3.2 Microstrip test fixture structure...41
Fig. 3.3 THRU standard. 41

Fig. 3.4 REFLECT standard. 42
Fig. 3.5 LINE standard. 42
Fig. 3.6 Substrate definition 43
Fig. 3.7 Fabricated TRL calibration kit. 45
Fig. 3.8 S-parameters of the THRU standard (a)$|S_{21}|$ (dB); $|S_{12}|$ (dB); (c) $|S_{11}|$ (dB);
(d) $|S_{22}|$ (dB). 46
Fig. 3.9 S-parameters of the THRU line with bias tees (a) $|S_{21}|$ (dB); (b) $|S_{12}|$ (dB);
(c) $S_{11}|$ (dB); (d) $|S_{22}|$ (dB). 47
Fig. 3.10 Measured S-parameters of the ATF-36077 transistor (a) $|S_{21}|$ (dB); (b) $|S_{12}|$ (dB);
(c) $|S_{11}|$ (dB); (d) $|S_{22}|$ (dB) 48
Fig. 3.11 Measured S-parameters of a 100 nH Inductor (a) $|S_{21}|$(dB); (b) $|S_{12}|$ (dB);
(c) $|S_{11}|$ (dB); (d) $|S_{22}|$ (dB); (e) $|S_{11}|$ Smith chart. 49
Fig. 3.12 Measured S-parameters of a 100 pF Capacitor (a) $|S_{21}|$ (dB); (b) $|S_{12}|$ (dB);
(c) $|S_{11}|$ (dB); (d) $|S_{22}|$ (dB); (e) $|S_{11}|$ Smith chart. 50
Fig. 3.13 S-parameter measurement of a 50 Ohm resistor (a) $|S_{11}|$ (dB); (b) $|S_{22}|$ (dB);
(c) $|S_{11}|$ Smith Chart; (d) $|S_{22}|$ Smith Chart. 51
Fig. 4.1 Microstrip discontinuities (a) Bend; (b) T - junction; (c) Meander line. 54
Fig. 4.2 Schematic Diagram of the amplifier 58
Fig. 4.3 Schematic simulation results of the amplifier. 59
Fig. 4.4 Layout of the distributed amplifier. 60
Fig. 4.5 Comparison between schematic simulation and EM simulation. 61
Fig. 4.6 Fabricated amplifier 62
Fig. 4.7 Measured and simulated S –parameters. 63
Fig. 4.8 Comparison between measured S-parameters of the transistor using
Agilent VNA and R&S VNA 64
Fig. 4.9 Comparison between measurement and schematic simulations using transistor
measured in HP VNA. 65
Fig. 4.10 S-parameter measurement results for different input power levels. 67
Fig. 4.11 Fabricated TRL calibration kit with CPW. 68
Fig. 4.12 S-parameter comparison between the measured amplifier and the simulations
conducted using the transistor measured with the CPW calibration kit. 68
Fig. 4.13 Measured input 1dB compression point (a) 1 GHz; (b) 2 GHz. 69
Fig. 5.1 Digital transversal filtering. 72
Fig. 5.2 Typical microwave transversal filter structure. 73

Fig. 5.3 Microwave lumped and transversal element filter topology....74
Fig. 5.4 (a) Low pass filter; (b) High pass filter....76
Fig. 5.5 Schematic diagram of the designed filter....78
Fig. 5.6 Simulation results (a) $|S_{21}|$ (dB); (b) $|S_{12}|$ (dB); (c) $|S_{11}|$ (dB); (d) $|S_{22}|$ (dB);
(e) Stability factor K; (f) Delta factor....79
Fig. 5.7 (a) Gain VS input power; (b) Output power VS Input power....79
Fig. 5.8 Monte Carlo simulation (a) $|S_{21}|$ (dB); (b) $|S_{11}|$ (dB)....80
Fig. 5.9 CMOS 0.13-um layer configuration....81
Fig. 5.10 Effect of ground plane on (a) Inductance; (b) Q factor....82
Fig. 5.11 Pad de-embedding (a) Short; (b) Open....82
Fig. 5.12 Layout of the designed filter....83
Fig. 5.13 Schematic simulation VS post layout simulation (a) $|S_{21}|$ (dB); (b) $|S_{12}|$ (dB); (c) $|S_{11}|$ (dB); (d) $|S_{22}|$ (dB)....84
Fig. 5.14 Fabricated filter....85
Fig. 5.15 Measured first IC (a) $|S_{11}|$ (dB) (b) $|S_{12}|$ (dB) (c) $|S_{11}|$ (dB) (d) $|S_{22}|$ (dB)....86
Fig. 5.16 Measured second IC....87
Fig. 5.17 Measured input 1 dB compression point....88
Fig. 6.1 Low pass inverse Chebyshev filter structure....92
Fig. 6.2 Low pass to band pass conversion....93
Fig. 6.3 Band pass filter structure....94
Fig. 6.4 Conversion of parallel section in to two series parallel sections....95
Fig. 6.5 Final inverse Chebyshev band pass filter structure....95
Fig. 6.6 Cross section view of an MIM capacitor structure....96
Fig. 6.7 Comparison between MIM capacitor foundry model with Sonnet simulation....97
Fig. 6.8 Sonnet simulation results (a) $|S_{21}|$ (dB); (b) $|S_{11}|$ (dB)....98
Fig. 6.9 Sonnet simulation for different dielectric thickness
(a) $|S_{21}|$ (dB); (b) $|S_{11}|$ (dB)....98
Fig. 6.10 S-parameter simulation results with frequency shift
(a) $|S_{21}|$ (dB); (b) $|S_{11}|$ (dB)....99
Fig. 6.11 S-parameter simulation results of different substrate conductivities
(a) $|S_{21}|$ (dB); (b) $|S_{11}|$ (dB)....99
Fig. 6.12 3D view of the designed filter....100
Fig. 6.13 Layout of the lumped element filter....101

CHAPTER 1

Introduction

1.1 Broad-Band Amplifiers for RF Communication Systems

Broadband amplifiers are one of the main building blocks in modern communication systems. Some of the applications that employ broadband amplifiers include electronic warfare, radar and high-data-rate fibre optic communication systems. The interest for this type of devices has grown rapidly due to the availability of various mobile communication standards and increasing demand for high data rate communication systems.

As various mobile communication standards are available, it is important to develop mobile terminals that can be used as multi-mode transceivers. One main solution for realizing multi-mode mobile communication standards is the "software defined radio architecture" [1].

Fig 1.1 shows a comparison between the conventional multi-band radio systems and software defined radio systems. In the conventional multi-band radio architecture of Fig 1.1 (a), each standard consists of one receiver chain. Each receiver chain selects the channel according to the required carrier frequency. The analog section consists of fixed analog filters which select corresponding the carrier frequency and bandwidth. In software defined radio systems the received signal is first fed into a broadband amplifier. Next, the channels

are converted to the digital domain using a high speed A/D converter. The desired channel is next selected with the software defined channel selection filters in the digital domain. Hence, broadband amplifiers play a key role in software defined radio architectures.

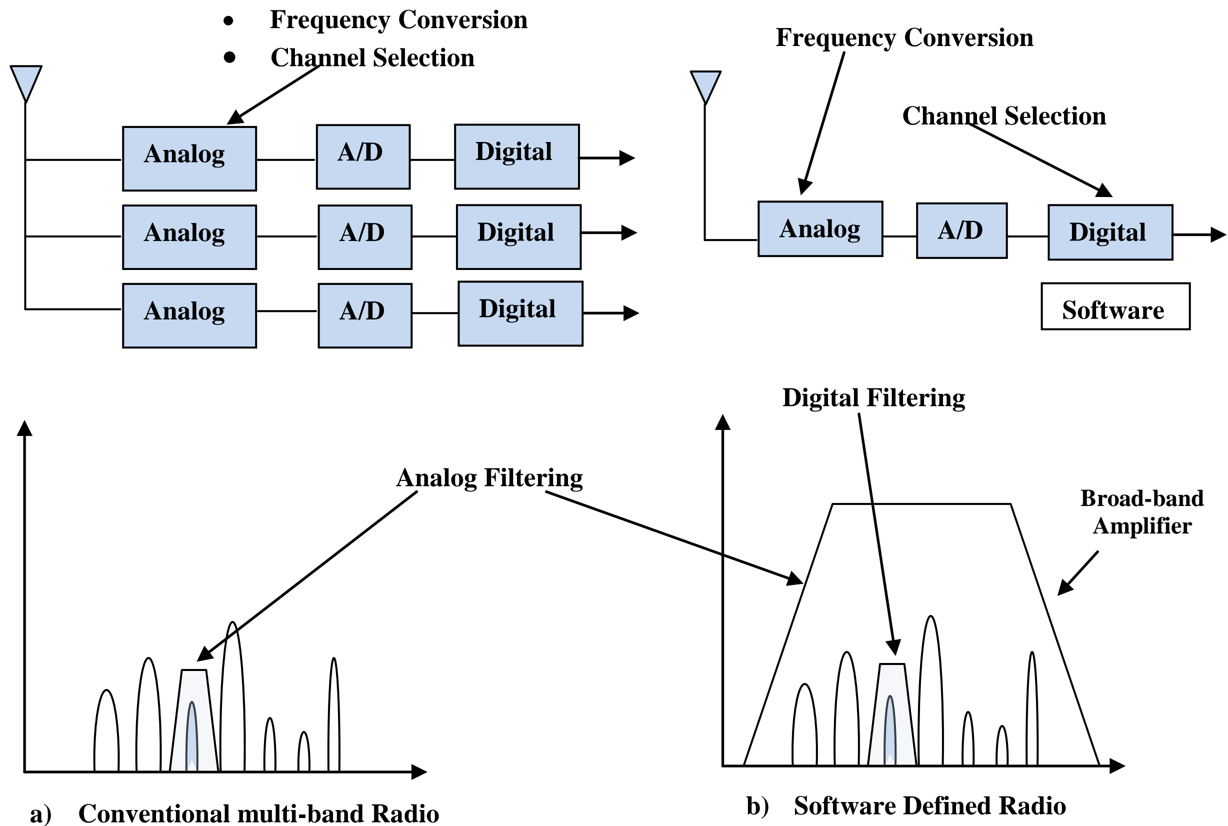


Fig. 1.1 Multi-band and software defined radio systems.

In optical communication systems the carrier frequency is around 200 THz, with high speeds of data transfer. Fig 1.2 shows a fiber optic receiver system. In such a system, optical signals are converted to electrical signals by using a photodetector. Converted signals are amplified by a TIA (Trans-Impedance Amplifier), which is a broadband amplifier.

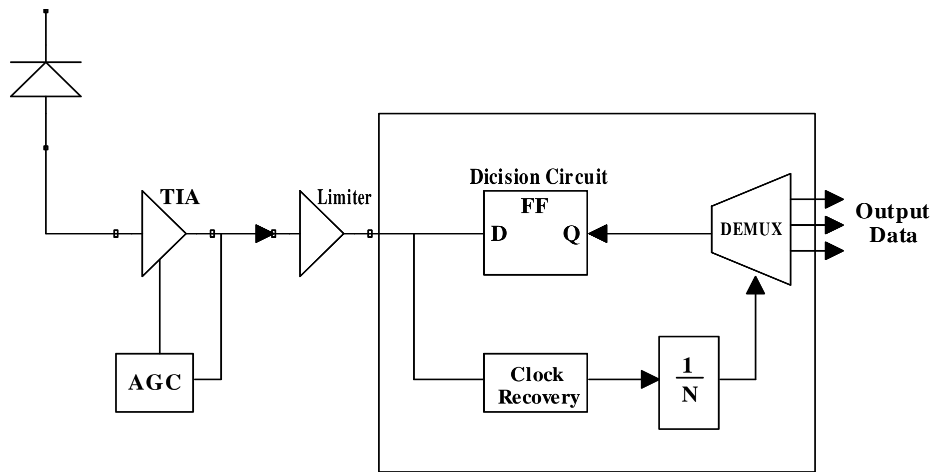


Fig. 1.2 Fibre optic receiver system.

1.2 Broadband Amplification Techniques

To realize a broad bandwidth amplifier, conventional narrowband matching techniques are not suitable. Hence, special techniques need to be incorporated in order to achieve wide bandwidths. Some of the well-established techniques are:

- Reactively matched circuit;
- Feedback circuit;
- Lossy matched circuit;
- Distributed amplifier circuit;

1.2.1 Reactively matched circuit

This is also known as the lossless matched amplifier due to the reactively matched input and output circuit. Fig 1.3 shows a block diagram of a conventional reactively matched amplifier [2].

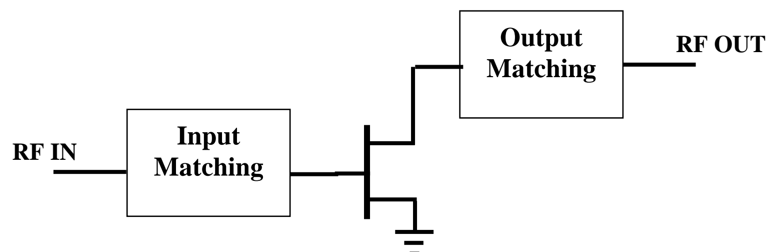


Fig. 1.3 Reactively matched amplifier.

The matching circuit in this topology uses gain compensation by creating reflections between the matching circuits and the FET. In this topology the poor impedance matching is a disadvantage. The first reactively matched circuit was reported in 1981 by Tserng, et al. [3]. He was able to achieve a bandwidth of 16 GHz from 2 – 18 GHz with a gain of 5 dB. However, the return loss is less than 10 dB throughout the bandwidth.

1.2.2 Feedback Amplifier Configuration

Figure 1.4 shows the circuit diagram of a feedback amplifier. In this circuit, a shunt feedback is incorporated between gate and the drain in-order to obtain a broader bandwidth. This feedback contains three elements. The value of the resistor R_{fb} controls the gain of the amplifier. Gate inductance L_g, drain inductance L_d, and feedback inductance L_{fb} controls the bandwidth of the amplifier [4]. The capacitance C_{fb} acts as a DC block from the drain biasing.

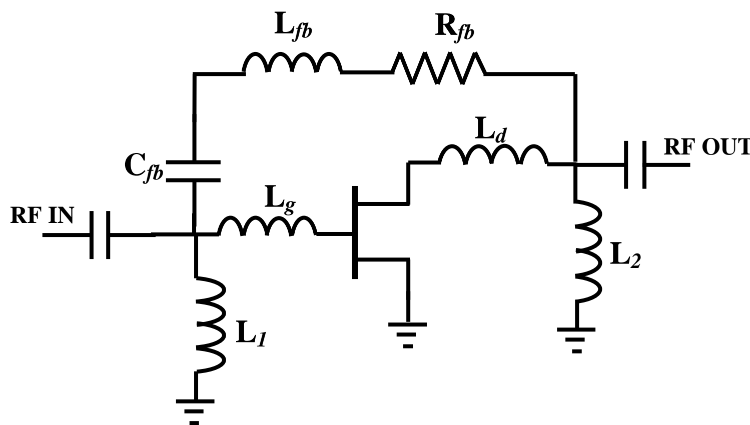


Fig. 1.4 Feedback amplifier

Some of the advantages of this topology include: less complexity, ability to provide higher power added efficiency, flat gain and better stability. The main disadvantage of this configuration is the poor noise figure due to the feedback resistance used. Also, it is very sensitive to frequency in hybrid circuits due to the parasitic and hence more suitable for MMIC design. Niclas, et al. first proposed the concept of the feedback amplifier in 1980 [4].

The concept of negative feedback was available before Niclas publication. However, in his design he incorporated both negative and positive feedback to obtain a broader bandwidth. He was able to obtain a gain of 4 dB from 350 MHz to 14 GHz with an output power of 13 dBm.

1.2.3 Lossy Matched Amplifier Circuit

In this topology, two resistors R_1 and R_2 are employed for the input and output matching respectively as illustrated in Fig 1.5. These resistors are used to obtain flat gain by maintaining an input and output match throughout the desired bandwidth. It has a broader bandwidth at the expense of low power added efficiency. Moreover, due to the resistor R_1 and R_2, it consists of a poor noise figure. This was first reported in the paper published by K. Honjo [5]. He was able to obtain a bandwidth of 13.5 octaves and 8.6 dB of gain using GaAs FETs.

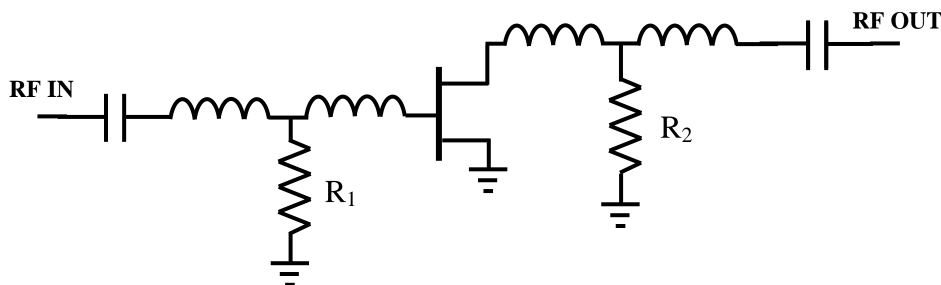


Fig. 1.5 Lossy matched amplifier circuit.

1.2.4 Distributed Amplifier Circuit

This is a well-known technique used in microwave amplifier design. This concept can be used to realize microwave amplifiers with multi octave bandwidths. In a conventional distributed amplifier topology, several numbers of transistors are connected between the input and output lines as shown in Fig 1.6.

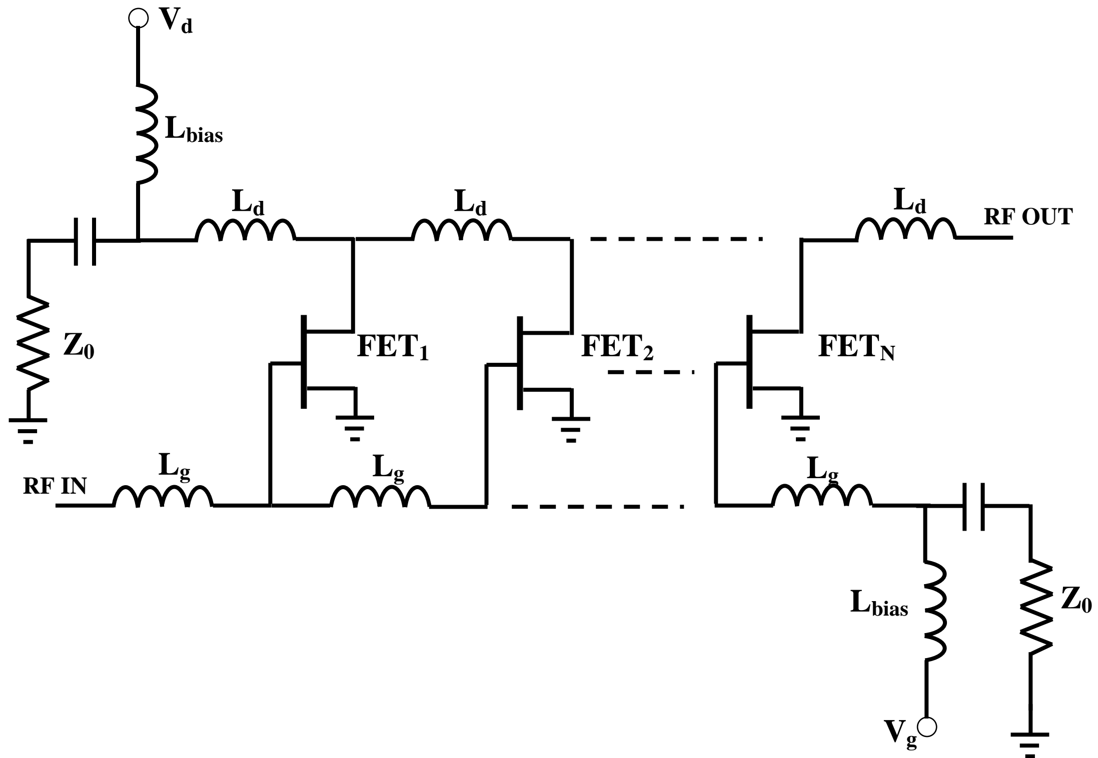


Fig. 1.6 Schematic diagram of a distributed amplifier circuit.

The gate and drain impedance of the FETs are absorbed in these lossy artificial transmission lines. These lines are referred to as gate and drain transmission lines and they are coupled by the transconducatnce of the FETs. The principle of distributed amplification was first proposed by W. S. Percival in 1937 [6]. However, his work was not widely known until after E. L. Ginzton et al. reported the analysis of distributed amplifiers using valves in 1948 [7].

The first part of this thesis concentrates on the designing of such a distributed amplifier in PCB. A detailed discussion of this particular topology is provided in later chapters.

1.3 CMOS Technology for RF and Microwave Applications

Conventionally, RF and microwave ICs were very often realized in III-V technologies. Such as GaAs and InP. MESFETs and HFETs, which are available in these technologies, are able to operate at high frequencies and are superior in their performance. However, these technologies are not suitable for consumer products due to the high cost.

Silicon based technologies, such as CMOS, SiGe and BiCMOS are more suitable for consumer products, due to their high yield and low cost. Out of these technologies CMOS is relatively cheaper and more suitable for integrating digital circuits and data storage devices on the same chip.

However, designing RFICs in CMOS is challenging due to the lossy substrate. In a typical CMOS substrate, the Silicon conductivity is ~ 10 S/m, which is very lossy. Hence, realizing inductors with a high quality factor is challenging in this technology, especially at microwave frequencies due to the ohmic losses in the metal traces and substrate resistance and eddy currents. There are techniques used in CMOS RFIC in order to improve the quality factor of these inductors. Some of the techniques include; increasing the number of metal layers so that the inductor can be realized on the top most layer by increasing the distance between the lossy substrate and the microstrip lines, use lowest metal layer as a ground to provide an excellent isolation, choose thickened metal for the top most layer signal lines to reduce metal loses [8]. On the other hand, research interest on using active inductors and active filters has increased in recent years.

CMOS Active and Passive Filters

Traditionally, CMOS active filters were realized using transconductance amplifiers [9]. However, this type of filters is most suitable for low frequency range applications only [10]. Nowadays, research is conducted to implement inductors using active components [11]-[14]. Such active inductors are suitable for CMOS, because of reduced size and high quality factor. However, these circuits exhibit poor linearity and high noise figure due to the active components.

Various methods have been researched in the past to implement active filters in MMIC. Some of the research works consider active gyrators [15]. The transversal and recursive principle is another concept used in GaAs to implement active filters [16]. This was a concept used in discrete time filtering and adopted in the microwave frequency range later by Rauscher [16]. Later Schindler et al. modified this concept to reduce the circuit size and they proposed lumped and transversal element filters to realize an active filter [17] as shown in Fig 1.7. The concept of transversal filtering is somewhat similar to the distributed amplifier concept. The fundamental difference between the two types of filtering is that, in the case of the distributed amplifier, the signals are combined together in phase. And in the case of filtering, the filtering is done by combining different amplitudes and frequency dependent phase delays.

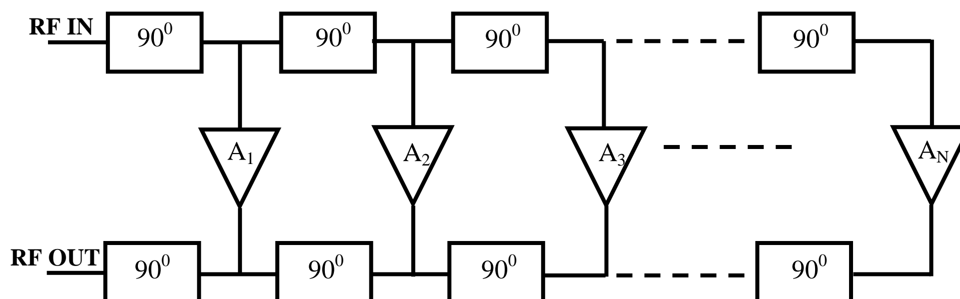


Fig. 1.7 Microwave transversal filter circuit.

The interest in the design of microwave and millimeter wave passive filters has recently increased. This is mainly because at higher operating frequencies the wavelengths are comparable with on-chip component dimensions. Therefore distributed elements can be used to design filters at higher frequencies such as millimeter wave. Using lumped elements in CMOS, microwave filter design is a challenging task due to the low quality factor of inductors and capacitors.

1.4 Motivation, Scope and Thesis Organization

The main objective of this thesis is the design of a broadband amplifier in 0.1-3.0 GHz and active and passive filters for RF and microwave front end systems. Frequency range in 0.1-3.0 GHz is chosen as it covers most of the commercial application bands such as UHF, VHF, ZigBee, GSM, Bluetooth and wireless LAN etc. This project has been divided into two subprojects. In the first project, a detailed description of the distributed amplification technique has been discussed. Some of the characteristics of this type of amplifiers have been simulated and verified. Next, a detailed explanation of the design and fabrication of a distributed amplifier from 0.1-3.0 GHz in PCB is reported.

The second project consisted of two designs. The first design is a lumped and transversal element band pass filter and the second is a passive lumped element filter using the Global Foundries CMOS 0.13-μm process. The simulation results have been verified by measuring the fabricated device. The organizations of the thesis is as follows:

Chapter 2: In this chapter the theory of distributed amplification is presented. Also, the effect of FET parasitics on distributed amplifier performance is discussed and verified through simulation.

Chapter 3: Measurement of active and passive components using TRL calibration technique is reported.

Chapter 4: A design of a distributed amplifier on PCB is presented. Schematic simulation results and comparison between electromagnetic and measurement results are provided.

Chapter 5: This chapter presents the second project which is the design of a lumped and transversal element filter in a 0.13-μm CMOS process. Simulation results of the designed filter are presented. Next, on wafer measurement results of the filter are compared with simulations.

Chapter 6: The design of a passive filter in 0.13-μm CMOS process at Ka band is presented.

Chapter 7: The work presented in this thesis is summarized and recommendations are provided.

CHAPTER 2

Distributed Amplification Technique

2.1 Introduction

Microwave amplifiers always have benefited from new developments in device technology. Out of many characteristics of an amplifier, gain, frequency are the most important. After the invention of the triode, it was found that the gain bandwidth product of an amplifier is highly affected by the shunt capacitance. Hence, realizing a wide bandwidth amplifier was a challenging task. Distributed amplification is a well-known technique to overcome this challenge.

In this chapter we discuss the concept of distributed amplification. First, the gain bandwidth product of an amplifier is introduced. Next the principle of distributed amplification is discussed, followed by the explanation of several theoretical analysis methods. Finally, simulation verification of the effect of the FET intrinsic parasitics on a distributed amplifier is reported.

2.2 Gain Bandwidth Product of an Amplifier

It has been shown by Wheeler [18] that the gain and bandwidth of an amplifier cannot be increased simultaneously beyond a certain limit. This limit is determined by a factor which is proportional to the ratio of tube transconductance g_m to the square root of the product of input and output plate capacitance. Hence, the gain bandwidth product cannot be increased indefinitely by connecting tubes in parallel because an increase in gain due to g_m is compensated by the total of input and output plate capacitance. Therefore, these two quantities are trade-offs when designing an amplifier. The concept illustrated by Wheeler [18] for tubes also applies to modern FET transistors as well. Thomas Wong [19] illustrated this concept by considering a simple transistor combined with coupling circuit as shown in figure 2.1.

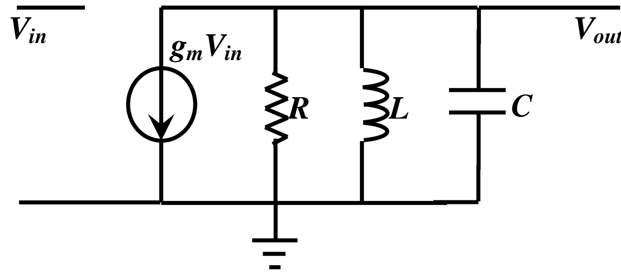


Fig. 2.1 Simple band pass amplifier structure.

The transfer function of the above circuit can be obtained as:

$$A_v(\omega) = \frac{-g_m}{1 + jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)} \tag{2.1}$$

Where $\omega_0 = \frac{1}{\sqrt{LC}}$ and $Q = \omega_0 RC$

The maximum gain occurs at midband and is given by$g_m R$. The -3 dB bandwidth B is given by $1/_{2\pi RC}$. Hence the gain-bandwidth product is

$$A_{vo}B = \frac{g_m}{2\pi C} \tag{2.2}$$

From equation 2.2 it can be seen that, if we are interested in obtaining the maximum gain-bandwidth product from a given active device, then we should keep *C* close to the intrinsic contribution from the input and output capacitance of the active device.

2.3 Principle of Distributed Amplification

To overcome the difficulty of increasing the gain-bandwidth product of an amplifier, an arrangement should be made so that we can connect transistors in parallel without increasing up the input and output parasitic capacitances. The distributed amplification technique enables us to increase the gain-bandwidth product without adding shunt capacitance. This concept was first proposed by W. S. Percival's patent in 1937 [6]. In his design, he made the electrodes of the tubes in a helical coil form, which combined with the inter electrode capacitors to form an artificial transmission line. Percival's invention did not gain widespread attention until Ginzton et al. [7] published a paper on distributed amplification in 1948. Figure 2.2 shows a schematic representation of a FET distributed amplifier.

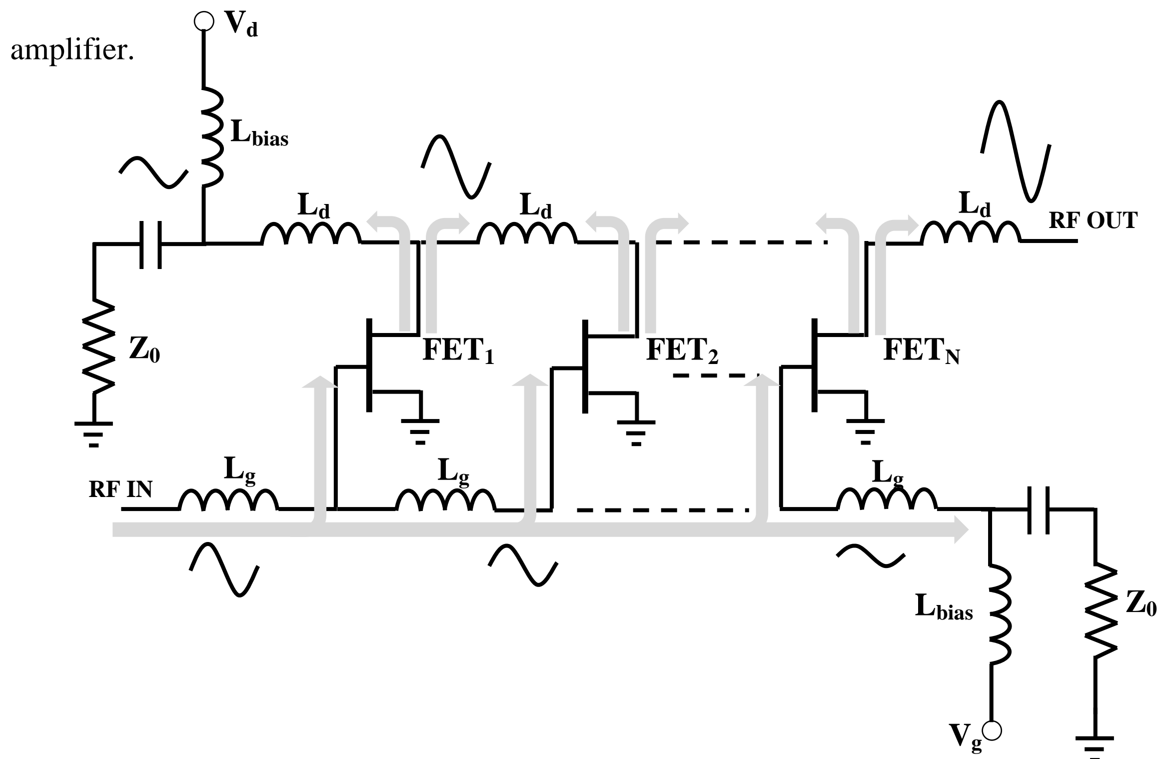


Fig. 2.2 Schematic representation of a FET distributed amplifier.

As shown in Fig. 2.2, the gates of the FETs are connected to a series of inductors L_g which is known as gate-line inductors. Similarly, drains of the FETs are connected to a series of inductors L_d which is known as the drain-line. Fig. 2.3 shows the small signal equivalent circuit of a FET. C_{gs} and C_{ds} are the input and output capacitance of the FET respectively. C_{gd} is the capacitance between gate and drain. In this case, we assume the unilateral case. Hence, C_{gd} is neglected. These input and output capacitors are absorbed into the gate line inductors and drain line inductors to form a constant k LC low-pass ladder filter structure as shown in Fig 2.4. One end of both lines has been terminated with the appropriate characteristic impedance Z_g and Z_d.

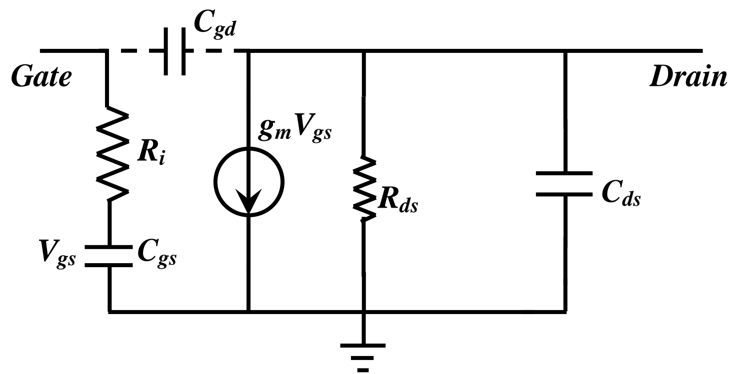


Fig. 2.3 Small signal equivalent circuit of a FET.

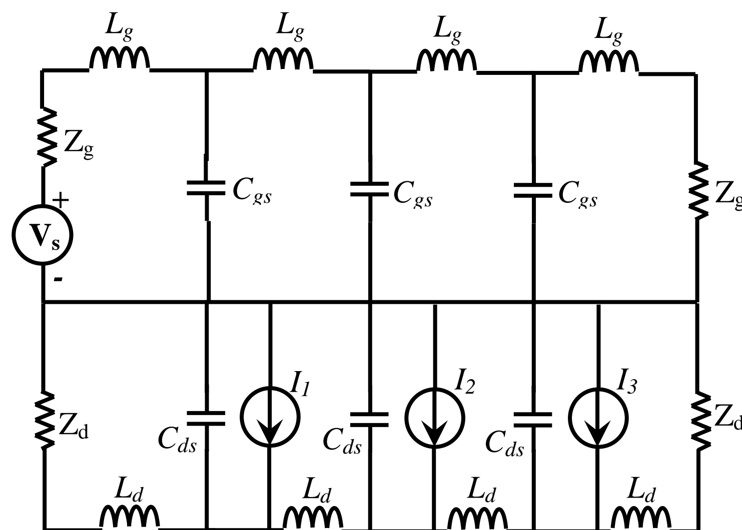


Fig. 2.4 Equivalent circuit of a distributed amplifier.

When an RF signal is applied at the input of the gate line, the signal travels down the gate line and will be absorbed at the termination end. As the signal travels down the gate line, the transistors are excited by the traveling voltages and will be coupled into the drain line through the transconductance of each transistor. At each node in the drain line the signal will travel away in opposite directions. Signals traveling to the left will be absorbed by the network termination impedance. Only the signals that travel to the right will appear as useful output. To produce sufficient gain, it is important that the drain currents add in phase as the signal propagates along the drain line. This is achieved by making the phase shift per section of the gate line equal to the phase shift per section of the drain line. This is possible under the assumption that all the transistors are identical.

For a typical FET, C_{gs} is larger than C_{ds}. Hence, in order to equalize the phase shift per section in both lines, an additional capacitance has to be added as shown in Fig. 2.4.

Hence,

$$C_{gs} = C_{ds} + C_{add} \quad (2.3)$$

Next we choose

$$L_g = L_d = L \quad (2.4)$$

There for cut-off frequency of the line is given by:

$$\omega_c = \frac{2}{\sqrt{LC_{gs}}} = \frac{2}{\sqrt{L\big(C_{ds} + (C_{add})\big)}} \quad (2.5)$$

The characteristics impedance of the lines is given by:

$$Z_0 = \sqrt{\frac{L}{C_{gs}}} = \sqrt{\frac{L}{C_{ds} + C_{add}}} \quad (2.6)$$

From the equivalent circuit of the distributed amplifier, it can be seen that inductors and capacitors form a distributed low pass filter structure, whose bandwidth is determined by

the amount of inductance and capacitance in one period. Hence, it is possible to increase the gain by introducing more transistors without compromising the bandwidth. However, this is possible only if the transistors and transmission networks are not dissipative. In a practical system, increasing the number of sections will not increase the gain per section beyond a certain limit and it might even become negative.

Ginzton addressed some of the techniques to improve the flatness of gain and delay by incorporating m-derived networks with *m* greater than unity. He also suggested that by connecting together the adjacent anodes or grids in pairs, a constant gain can be obtained throughout the pass-band. Soon after Ginzton's publication in 1948, Horton et al. published a paper in 1950 addressing some of the practical considerations in distributed amplifiers [20]. In their paper, they considered effects not considered in the first order theory such as, coil losses, grid losses, grid and plate inductors and coil winding capacitance. He also suggested corrective methods to counteract the limitations. In 1954 Bassett reported a way to improve the gain fluctuation at the cut-off frequency of a distributed amplifier by incorporating resistors into the m-derived low pass filter structure [21].

The research in distributed amplifiers using vacuum tubes continued [20]-[24] until the first solid-state GaAs MESFET distributed amplifier investigated by Moser in 1967 [25] and Jutzi in 1969 [26]. The first monolithic GaAs distributed amplifier was successfully built and tested by Ayasli et al. in 1981 [27] and 1982 [28], which was a vital point in the evolution of the distributed amplifiers. Ayasli et. al. used a new approach to obtain a wideband performance using distributed amplifiers. In their approach they used GaAs FETs as the active elements and instead of using inductors, gate and drain lines were implemented with transmission lines, which are truly distributed. Fig 2.5 shows a schematic diagram of such amplifier. Since the gate and drain lines are implemented using transmission lines, it is also known as "*Traveling-Wave amplifier*". With this approach it is possible to avoid many

difficulties occurring in the conventional approach such as capacitive and inductive coupling, loading due to grid and coil losses, parasitic inductance and capacitance in coil windings.

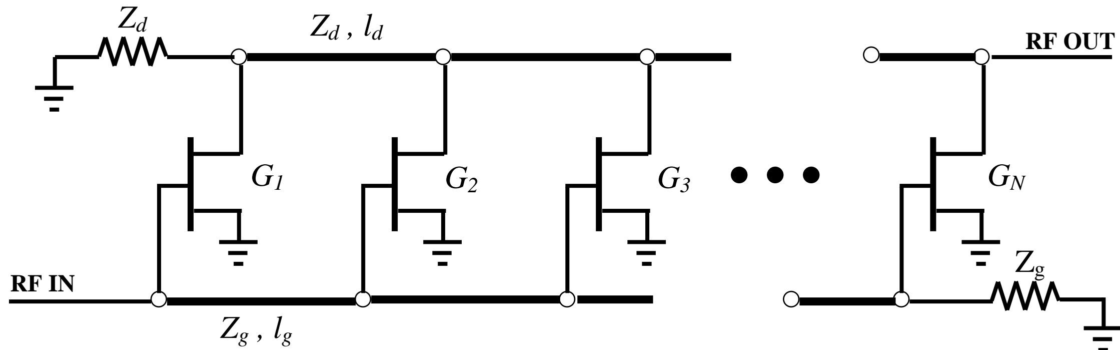


Fig. 2.5 Schematic diagram of a traveling wave amplifier.

Ayasli et al. also showed a theoretical analysis for the traveling-wave amplifier constructed with periodically loaded transmission lines, which will be discussed later in this chapter.

As described earlier, the bandwidth of a distributed amplifier depends on the cut-off frequency of the artificial transmission line. Engineers were able to obtain several hundreds of GHz bandwidth using this technique [29]-[33]. A special technique used to improve the bandwidth of the distributed amplifier is capacitive division [33]-[36]. In this technique a capacitor is connected in series with the FET gate-source capacitor which acts as a voltage divider. The reduction in gain was recovered by increasing the number of stages in the amplifier. Introducing such capacitive division helps in increasing the amplifier bandwidth equal to f_{max} of the FET [33]. On-the-other hand, it also helps to increase the total device periphery per gain stage and this helps to bring the optimum as load line of the FET closer to the output drain line impedance.

2.3.1 Power Performance of a Distributed Amplifier

Since the invention of the transistor, the distributed amplifier was a main research area in the RF and microwave field. Much research has been conducted to improve the

performance of this topology. Improving the power performance of a distributed amplifier was a main research area [37]-[46]. A conventional distributed amplifier's power performance is limited due to several reasons such as breakdown voltage of the transistor; unequal contributions from the transistors to the output power, and none-optimum load impedance seen by the transistors [43]. Capacitive drain coupling is one proposed technique to increase the power capabilities of a distributed amplifier [38]. In this case, an additional capacitor is added between the drain line and the drain of the last FET to reduce the drain line loading and increase the impedance seen by the FET. Schindler et al. was able to obtain an output power of 20 dBm up to 33 GHz. Using GaN devices also can help to improve power handling capabilities of distributed amplifiers due to its superior thermal and breakdown voltage properties [44]. By using GaN devices, they were able to obtain an output power of 37 dBm and a power added efficiency of 27 % in the frequency range 0.002 – 3.0 GHz.

2.3.2 Noise Performance of Distributed Amplifiers

In terms of noise, distributed amplifiers have a medium noise figure. It typically varies from 4 – 8 dB [47-54]. Formulas for the intrinsic noise figure of a distributed amplifier was first formulated by Niclas [47] in 1983. Based on his formulation, the minimum noise figure of a distributed amplifier can be reduced by increasing the number of sections.

2.3.3 Stability of Distributed Amplifiers

The analysis on oscillation conditions in distributed amplifiers has been done by Gamand et al. in 1989 [55]. Based on their analysis, the instability for a given transistor with width W, increases with g_m, C_{gd} and the parasitic resistances r_{ds} and R_i tend to moderate the oscillations. In addition, he found that oscillations occur at high frequencies and they are

mainly due to the internal loops formed by the transconductance and the feedback capacitance C_{gd} of the transistor combined with the transmission lines.

2.4 Theoretical Analysis on Distributed Amplifiers

In this section three types of analysis methods available in the literature are presented. The first two types are based on the unilateral ($C_{gd} = 0$) version of the FET and will analyze an amplifier with loaded gate and drain transmission lines and an amplifier with inductors as gate and drain lines. The third analysis considers the effect of gate to drain capacitor (C_{gd}).

2.4.1 Amplifier with periodically loaded transmission lines

This analysis was first proposed by Ayasli et al. in 1982 [28]. Fig. 2.5 shows a distributed amplifier with periodically loaded transmission lines. By considering the unilateral figure of the FET, the above circuit can be separated into two sections each, for gate and drain lines, as shown in Figures 2.6 and 2.7 [56]. Hence, the circuit can be analyzed separately. The gate and drain lines are connected via the coupling through the current source $I_{dn} = g_m V_{cn}$. Fig. 2.6 (b) and 2.7 (b) shows a single unit cell of gate and drain lines respectively.

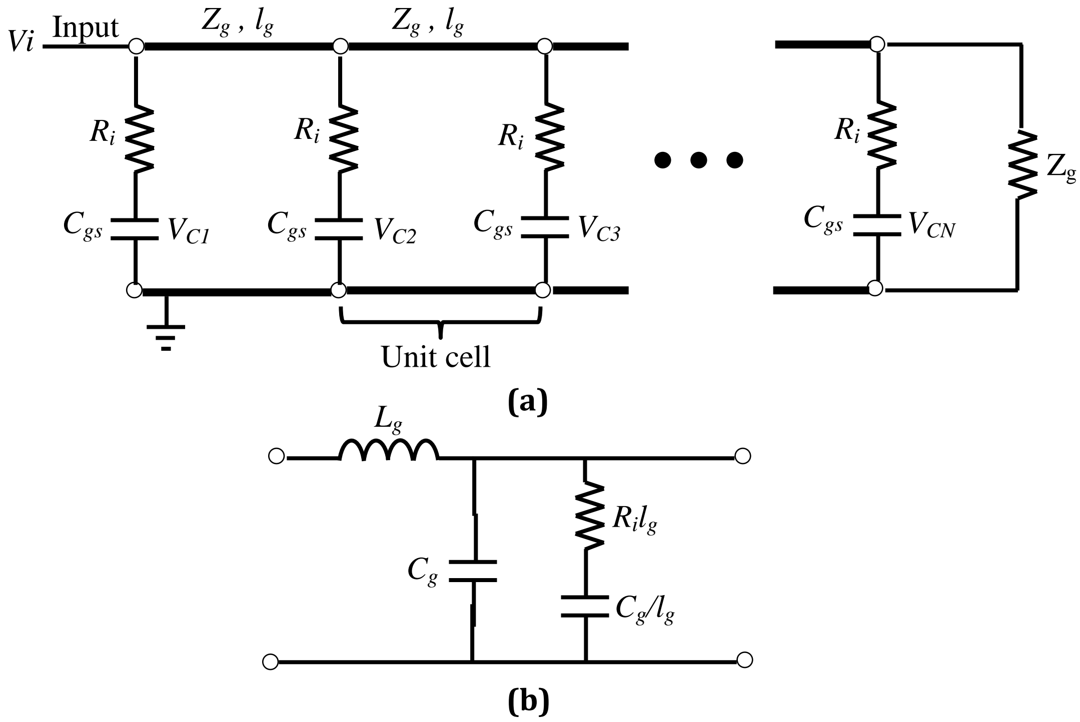


Fig. 2.6 Equivalent circuit of (a) gate line; (b) single unit cell of the gate line.

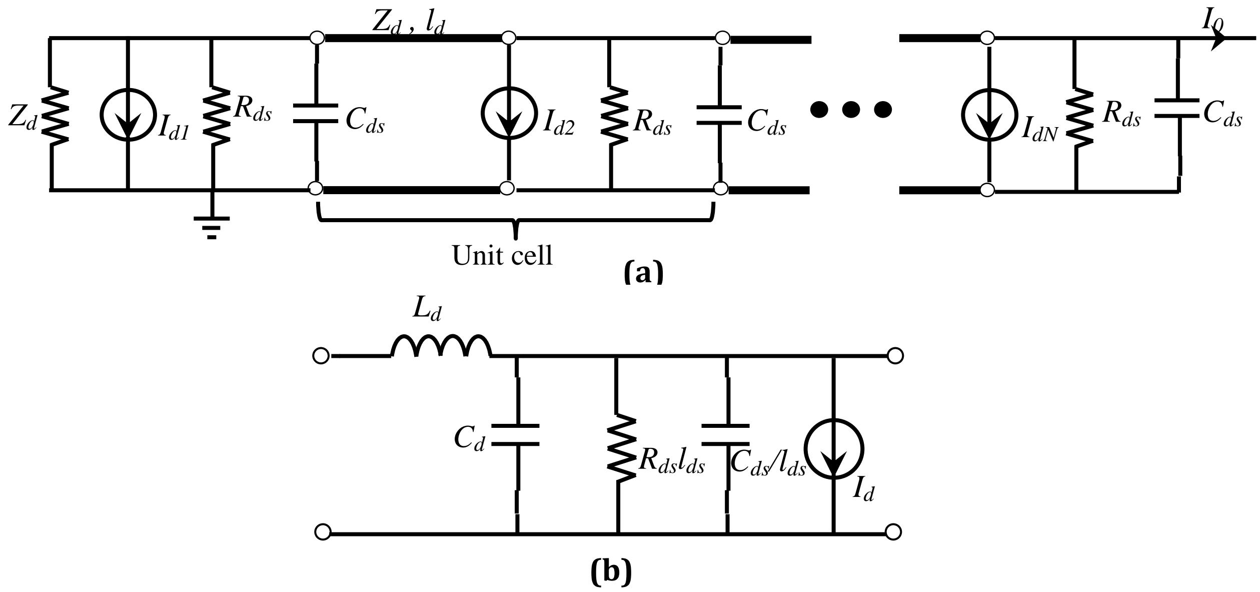


Fig. 2.7 Equivalent circuit of (a) drain line; (b) single unit cell of the drain line.

L_g and C_g are the per unit inductance and capacitance of the gate transmission lines. $R_i l_g$ and C_{gs}/l_g are the per unit length loading due to the FET input resistance R_i and gate to source capacitance C_{gs}. Similarly, L_d and C_d are the inductance and capacitance per unit length of

the drain line and $R_{ds}l_d$ and C_{ds}/l_d are the per unit length loading due to the FET output resistance R_{ds} and drain to source capacitance C_{ds}.

Since the transmission line properties change due to the FET input and output capacitances, we need to obtain the characteristic impedance of the modified lines. For the gate line, the series and parallel admittance per unit length are given by

$$Z = j\omega L_g \tag{2.7}$$

$$Y = j\omega C_g + \left[R_i l_g + \frac{1}{j\omega C_{gs}/l_g} \right]$$

$$\Rightarrow Y = j\omega C_g + \frac{j\omega C_{gs}/l_g}{1 + j\omega C_{gs} R_i} \tag{2.8}$$

Where Z is the series impedance and Y is the shunt admittance. Next, using transmission line theory, characteristic impedance of the gate line is obtained as

$$Z_g = \sqrt{\frac{Z}{Y}} = \sqrt{j\omega L_g \left\{ j\omega C_g + \frac{j\omega C_{gs}/l_g}{1 + j\omega C_{gs} R_i} \right\}^{-1}}$$

$$Z_g = \sqrt{\frac{L_g}{C_g + C_{gs}/l_g}}, \qquad R_i \approx 0 \tag{2.9}$$

In the above calculation, we have assumed that the loss due to the resistance R_i is negligible. By definition, the propagation constant of the transmission line is given by

$$\gamma_g = \alpha_g + j\beta_g = \sqrt{ZY} \tag{2.10}$$

Where, α_g is the gate line attenuation constant and β_g is the phase shift per section of the gate line.

Assuming small loss, such that $\omega R_i C_{gs} \ll 1$, $\omega^2 C_{gs}^2 R_i^2 \approx 0$, the gate-line propagation constant is calculated as:

$$\gamma_g = \frac{\omega^2 R_i C_{gs}^2 / l_g}{2} Z_g + j\omega \sqrt{L_g \left(C_g + C_{gs}/l_g\right)} \tag{2.11}$$

A similar analysis is used to obtain the characteristic impedance and propagation constant of the drain line. Hence, the series impedance *Z* and shunt admittance *Y* of the drain line are found as:

$$Z = j\omega L_d \tag{2.12}$$

$$Y = \frac{1}{R_{ds} l_d} + j\omega(C_d + C_{ds}/l_d) \tag{2.13}$$

Next, the characteristic impedance of the drain line is found as:

$$Z_d = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_d}{C_d + C_{ds}/l_d}} \tag{2.14}$$

And by using the small loss approximation, the propagation constant can be calculated as:

$$\gamma_d = \alpha_d + j\beta_d = \sqrt{ZY} \tag{2.15}$$

$$\gamma_d = \sqrt{j\omega L_d \left[\frac{1}{R_{ds} l_d} + j\omega(C_d + C_{ds}/l_d)\right]} \tag{2.16}$$

$$\cong \frac{Z_d}{2 R_{ds} l_d} + j\omega \sqrt{L_d (C_d + C_{ds}/l_d)} \tag{2.17}$$

The amplifier gain can be calculated by considering an incident input voltage of V_i. Hence, the voltage across the gate-to-source capacitance of the nth FET can be written as:

$$V_{cn} = V_i e^{-(n-1)\gamma_g l_g} \left\{ \frac{1/j\omega C_{gs}}{R_i + 1/j\omega C_{gs}} \right\}$$

$$\Rightarrow V_{cn} = V_i e^{-(n-1)\gamma_g l_g} \left\{ \frac{1}{1 + j\omega C_{gs} R_i} \right\} \quad (2.18)$$

For a typical FET we assume that, $\omega R_i C_{gs} \ll 1$. Hence, the factor $\frac{1}{1+j\omega C_{gs} R_i}$ can be approximated as unity throughout the bandwidth.

Each current generator in the drain line contributes waves in the form of $-\frac{1}{2} I_{dn} e^{\pm\gamma_d Z}$ in each direction. Also I_{dn} is given by

$$I_{dn} = g_m V_{cn} \quad (2.19)$$

Therefore, the total output current I_0 at the Nth terminal of the drain line is

$$I_0 = -\frac{1}{2} \sum_{n=1}^{N} I_{dn} e^{-(N-n)\gamma_d l_d} = -\frac{g_m V_i}{2} e^{-N\gamma_d l_d} e^{\gamma_g l_g} \sum_{n=1}^{N} e^{-n(\gamma_g l_g - \gamma_d l_d)} \quad (2.20)$$

Equation (2.20) can be simplified by using the identity

$$\sum_{n=1}^{N} x^n = \frac{x^{N+1} - x}{x - 1} \quad (2.21)$$

Thus, the total output current can be calculated as:

$$I_0 = \frac{-g_m}{2} V_i e^{-N\gamma_d l_d} e^{\gamma_g l_g} \left[\frac{\left\{ e^{-(\gamma_g l_g - \gamma_d l_d)} \right\}^{N+1} - e^{-(\gamma_g l_g - \gamma_d l_d)}}{e^{-(\gamma_g l_g - \gamma_d l_d)} - 1} \right]$$

$$I_0 = \frac{-g_m}{2} V_i \left[\frac{e^{-N\gamma_g l_g} - e^{-N\gamma_d l_d}}{e^{-\gamma_g l_g} - e^{-\gamma_d l_d}} \right] \quad (2.22)$$

Next the amplifier gain is calculated as:

$$G = \frac{P_{out}}{P_{in}} = \frac{\frac{1}{2}I_0^2 Z_d}{\frac{1}{2}|V_i|^2/Z_g} = \frac{g_m^2 Z_d Z_g}{4}\left|\frac{e^{-N\gamma_g l_g} - e^{-N\gamma_d l_d}}{e^{-\gamma_g l_g} - e^{-\gamma_d l_d}}\right|^2 \quad (2.23)$$

As explained in section 2.3, to obtain useful gain, waves contributed by each generator in the drain line must be added in phase. To ensure phase addition, $\beta_g l_g = \beta_d l_d$.

Hence, the gain in (2.23) can be simplified to

$$G = \frac{g_m^2 Z_g Z_d}{4}\frac{\left(e^{-N\gamma_g l_g} - e^{-N\gamma_d l_d}\right)^2}{\left(e^{-\alpha_g l_g} - e^{-\alpha_d l_d}\right)^2} \quad (2.24)$$

If we assume losses to be negligible, the term $e^{-\alpha_g l_g} - e^{-\alpha_d l_d}$ can be approximated as: $\alpha_g l_g = \alpha_d l_d$

Hence, for the ideal lossless case, the expression of the gain is found as

$$G = \frac{g_m^2 Z_g Z_d N^2}{4} \quad (2.25)$$

From equation (2.25), it can be seen that for an ideal distributed amplifier, the gain increases as N^2. However, in a conventional cascaded stage, gain increases with $(G_0)^N$ [56]. If we include losses, equation (2.24) explains that when $N \rightarrow \infty$ the gain of the distributed amplifier approaches zero. This is because that, the wave traveling along the lossy gate line decays exponentially. Hence, the FET at the end of the amplifier receives less input signal. On the other hand, amplified signals at the beginning of the drain line decay exponentially. However, an increase in the number of sections N is not enough to compensate for an exponential decay of signals. Therefore, we cannot increase the number of sections in a distributed amplifier indefinitely for a real lossy case. Which implies that there is an

optimum number for N for a given FET. To obtain the optimum N, which gives maximum gain, we need to differentiate equation (2.24) with respect to N. Hence N_{opt} is given as:

$$N_{opt} = \frac{\ln(\alpha_g l_g / \alpha_d l_d)}{\alpha_g l_g - \alpha_d l_d} \tag{2.26}$$

2.4.2 Analysis of a distributed amplifier with discrete inductors

In 1984 Bayer et al. [57] presented the analysis and reported a systematic graphical approach to design a distributed amplifier. For simplicity they used the unilateral model of the FET.

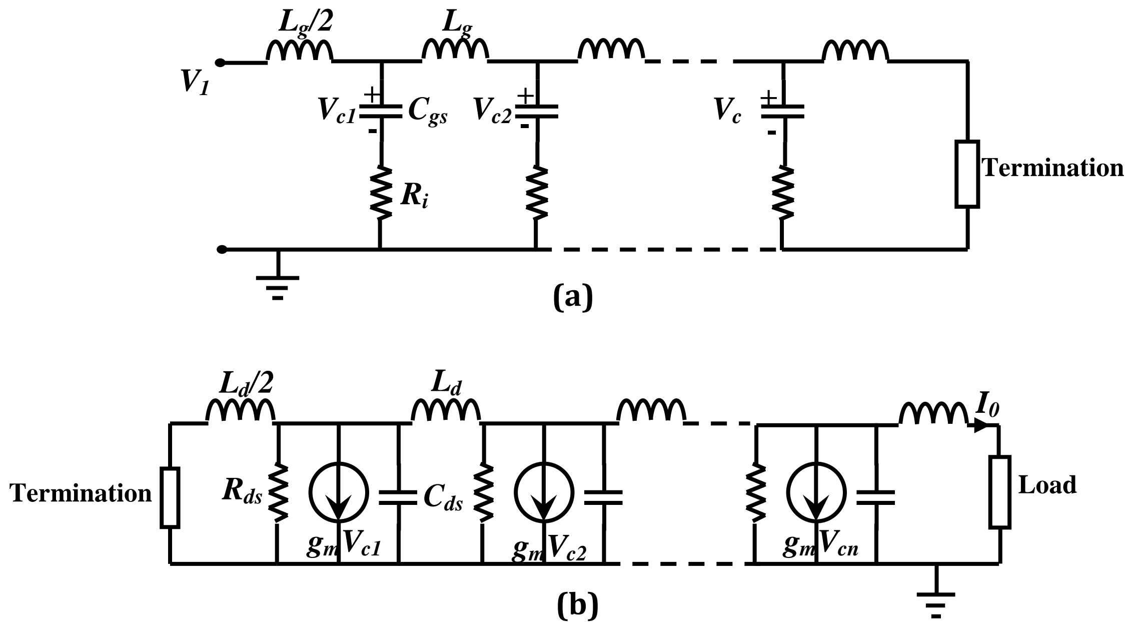


Fig. 2.8 Equivalent circuit of a DA with discrete components (a) gate line; (b) drain line.

Figure 2.8 shows the equivalent circuit for the gate and drain lines of the distributed amplifier. These lines are considered as constant-k lines and resistances R_i and R_{ds} introduce losses. In the analysis, they assumed that the lines are terminated with the image impedance. Hence, current delivered to the load of the amplifier is given by

$$I_0 = \frac{1}{2} g_m e^{-\theta_d/2} \left[\sum_{k=1}^{n} V_{ck} e^{-(n-k)\theta_d} \right] \tag{2.27}$$

Where, V_{ck} is the voltage across the gate-to-source capacitance of the kth FET,

$\theta_d = A_d + j\phi_d$ is the propagation constant of the drain line,

A_d and ϕ_d are the attenuation and the phase shift per section of the drain line respectively,

n is the number of FETS in the amplifier.

Next V_{ck} is expressed in terms of the voltage at the gate terminal of the kth FET and is given by:

$$V_{ck} = \frac{V_i e^{-(2k-1)\theta_g/2 - j\tan^{-1}(\omega/\omega_g)}}{\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]^{1/2}\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]^{1/2}} \tag{2.28}$$

Where,

V_i is the input voltage of the amplifier,

$\theta_g = A_g + j\phi_g$ is the propagation function of the gate line,

A_g and ϕ_g are the attenuation and the phase shift per section of the gate line respectively,

$\omega_g = 1/R_t C_{gs}$ is the radian gate line cut-off frequency and

$\omega_c = 2\pi f_c$ is the radian cut-off frequency of the lines.

As before, in order to obtain a useful gain, the phase velocities of both lines must be the same. Therefore, $\phi_g \cong \phi_d = \phi$, and by using equations (2.27) and (2.28), I_o can be re-written as

$$I_0 = \frac{g_m V_i \sinh\left[\frac{n}{2}\left(A_d - A_g\right)\right] e^{-n(A_d+A_g)/2} e^{-jn\phi - j\tan^{-1}(\omega/\omega_g)}}{2\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]^{1/2}\left[1+\left(\frac{\omega}{\omega_c}\right)^2\right]\sinh\left[\frac{1}{2}\left(A_d - A_g\right)\right]} \tag{2.29}$$

Power delivered to the load is given by:

$$P_0 = \frac{1}{2}|I_0|^2 Re[Z_{ID}] \cong \frac{1}{2}|I_0|^2\sqrt{L_d/C_d[1-(\omega/\omega_c)^2]} \tag{2.30}$$

Input power of the amplifier is given by:

$$P_i = \frac{|V_i|^2}{2|Z_{IG}|^2} Re[Z_{IG}] \cong \frac{1}{2}|V_i|^2 \Big/ \sqrt{L_g/C_g[1-(\omega/\omega_c)^2]} \tag{2.31}$$

Where Z_{IG} and Z_{ID} are the image impedance of the gate and drain lines respectively. The power gain of the amplifier is given by:

$$G = \frac{g_m^2 R_{01} R_{02} \sinh^2\left[\frac{n}{2}\left(A_d - A_g\right)\right] e^{-n\left(A_d + A_g\right)}}{4\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right][1-(\omega/\omega_c)^2]\sinh^2\left[\frac{1}{2}\left(A_d - A_g\right)\right]} \tag{2.32}$$

$R_{01} = \sqrt{L_g/C_g}$ and $R_{02} = \sqrt{L_d/C_d}$ are the characteristic impedance of gate and drain lines respectively. The voltage gain of the amplifier is given by

$$A = \frac{g_m (R_{01} R_{02})^{1/2} \sinh\left[\frac{n}{2}\left(A_d - A_g\right)\right] e^{-n\left(A_d + A_g\right)/2}}{2\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]^{1/2}\left[1+\left(\frac{\omega}{\omega_c}\right)^2\right]^{1/2}\sinh\left[\frac{1}{2}\left(A_d - A_g\right)\right]} \tag{2.33}$$

The optimum number of stages of the amplifier can be obtained using equation (2.33) and is given by:

$$N_{opt} = \frac{\ln\left(A_d/A_g\right)}{A_d - A_g} \tag{2.34}$$

2.4.3 Cascaded four-ports formulation

In the previous two analyses, the unilateral case for the FET is assumed for simplicity. However, this ignores the finite isolation of the FET. To describe these effects we need to account for the gate-to-drain capacitance of the FET. Such analysis will lead to more complicated formulations and may not give any closed form results. Hence, we need to employ numerical methods in order to solve these equations.

Cascaded four port formulation is a well-known method which includes the effect of gate-to-drain capacitor [58]. In this formulation, a cross section of the amplifier is considered with four ports as shown in Fig. 2.9.

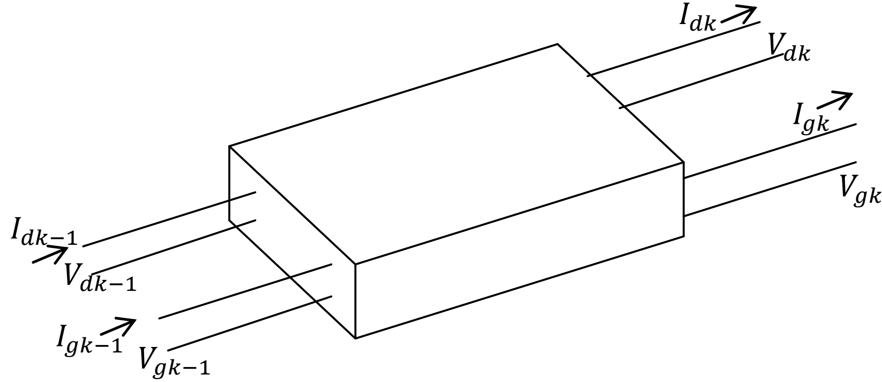


Fig. 2.9 A cross section of the distributed amplifier circuit

By considering Fig.2.9, a chain matrix for a four port can be defined in parallel with the ABCD matrix for a two port. Such a chain matrix can be written as

$$\begin{bmatrix} V_{dk-1} \\ I_{dk-1} \\ V_{gk-1} \\ I_{gk-1} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{13} & A_{14} \\ A_{21} & A_{22} & A_{23} & A_{24} \\ A_{31} & A_{32} & A_{33} & A_{34} \\ A_{41} & A_{42} & A_{43} & A_{44} \end{bmatrix} \begin{bmatrix} V_{dk} \\ I_{dk} \\ V_{gk} \\ I_{gk} \end{bmatrix} \quad (2.35)$$

Fig. 2.10 shows the internal components of the four ports. The active device is represented by a two port with admittance matrix $[Y]$.

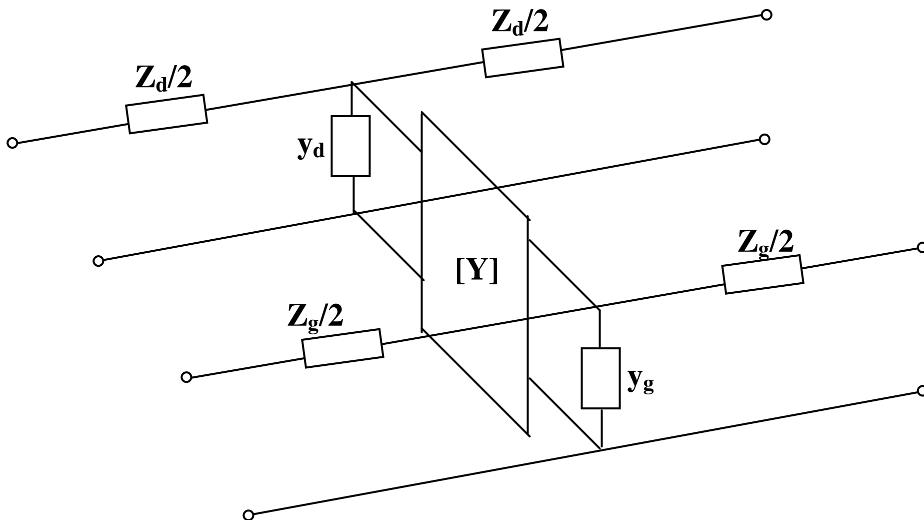


Fig. 2.10 Internal components of the four ports

To obtain a chain matrix for this section, we first separate the above circuit into several sections consisting of an active device, shunt elements and transmission lines. The chain matrix of the series elements is obtained by augmenting the ABCD matrices of the two ports and is given by

$$A_l = \begin{bmatrix} 1 & Z_d & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & Z_g \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{2.36}$$

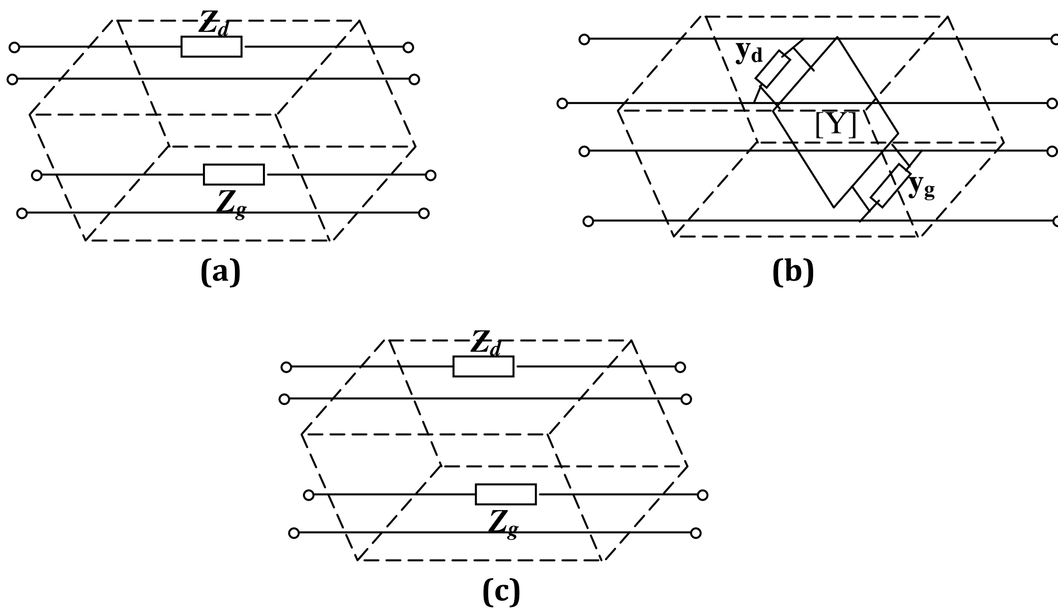


Fig. 2.11 Individual components of the four port section (a) Transmission lines; (b) Y parameters of the FET; (c) transmission lines

The chain matrix of the middle subsection is obtained by applying Kirchhoff's current law (a detailed derivation is provided in Appendix A) and is given by:

$$A_t = \begin{bmatrix} 1 & 0 & 0 & 0 \\ y_{22} + y_d & 1 & y_{21} & 0 \\ 0 & 0 & 1 & 0 \\ y_{12} & 0 & y_{11} + y_g & 1 \end{bmatrix} \tag{2.37}$$

If we use transmission lines instead of lumped elements equation (2.36) can be written as

$$A_l = \begin{bmatrix} \cosh\theta_d & Z_{0d}\sinh\theta_d & 0 & 0 \\ Z_{od}^{-1}\sinh\theta_d & \cosh\theta_d & 0 & 0 \\ 0 & 0 & \cosh\theta_g & Z_{0g}\sinh\theta_g \\ 0 & 0 & Z_{og}^{-1}\sinh\theta_g & \cosh\theta_g \end{bmatrix} \quad (2.38)$$

And equation (2.37) can be written as:

$$A_t = \begin{bmatrix} 1 & 0 & 0 & 0 \\ y_{22} & 1 & y_{21} & 0 \\ 0 & 0 & 1 & 0 \\ y_{12} & 0 & y_{11} & 1 \end{bmatrix} \quad (2.39)$$

The final chain matrix for this section, assuming that the network is symmetrical, is written as:

$$A_k = A_l A_t A_l \quad (2.40)$$

For a distributed amplifier with N sections, the overall chain matrix can be written as:

$$B = \prod_{k=1}^{N} A_k = \begin{bmatrix} \beta_{11} & | & \beta_{12} \\ -- & - & -- \\ \beta_{21} & | & \beta_{22} \end{bmatrix} \quad (2.41)$$

Where, β_{jj} represents a 2 x 2 sub-matrix. Hence, the input and output relation of the amplifier can be written as:

$$\begin{bmatrix} V_{do} \\ -V_{od}/Z_L^d \\ V_{go} \\ I_{go} \end{bmatrix} = B \begin{bmatrix} V_{dN} \\ V_{dN}/Z_L^d \\ V_{gN} \\ V_{gn}/Z_L^g \end{bmatrix} \quad (2.42)$$

Equation (2.42) can be used to obtain closed form formulas for S_{11}. However, the analytical results are cumbersome. Niclas et al. showed some of their numerical simulation results for the above formulations and some optimization methods for distributed amplifiers [58].

2.5 Effect of FET Parasitics on Distributed Amplifier Performances

The theoretical analysis performed in the previous section is based on a simple FET model and this type of analysis does not provide any insight into how the individual parasitics affect the distributed amplifier performance. In this section we explore how these parasitics affect the gain $|S_{21}|$, input return loss $|S_{11}|$, output return loss $|S_{22}|$ and isolation $|S_{12}|$ of a distributed amplifier.

To investigate the effect of parasitics, commercially available circuit simulator Agilent's Advanced Designed System (ADS) was used. Equivalent circuit model shown in Fig. 2.12 was used for the transistor model. Next, a three stage distributed (traveling-wave) amplifier incorporating ideal 50 Ohm transmission lines is designed. Gate and drain lines are terminated with a 50 Ohm resistor.

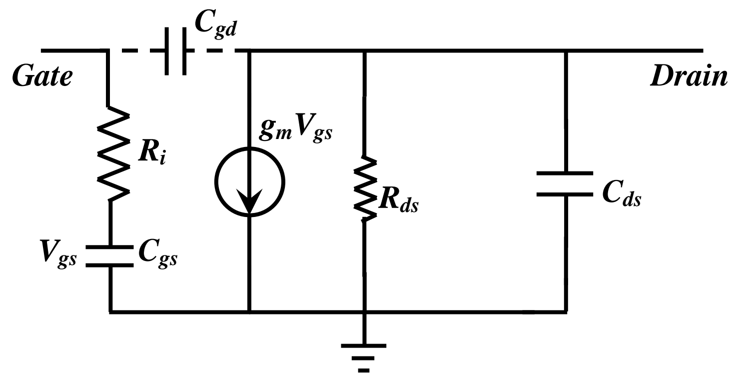


Fig. 2.12 Small signal equivalent circuit of a FET.

Several simulations are performed in order to investigate the effect of the parasitics. First we explore the effects of the gate-to-source capacitance (C_{gs}) by considering other parasitics negligible. Values of 0.1 fF, 1.0 fF, 10 fF, 100 fF and 200 fF were considered. Next, we explore the effect on series gate resistance R_i on the performance of a distributed amplifier. In this simulation R_i was varied for two different values of gate-to-source capacitance. Finally we explore the effect of gate-to-drain capacitance (C_{gd}) of a distributed amplifier when C_{gs} = 10 fF. The simulated results are shown in the subsection below.

2.5.1 Effect of Gate-to-Source Capacitance

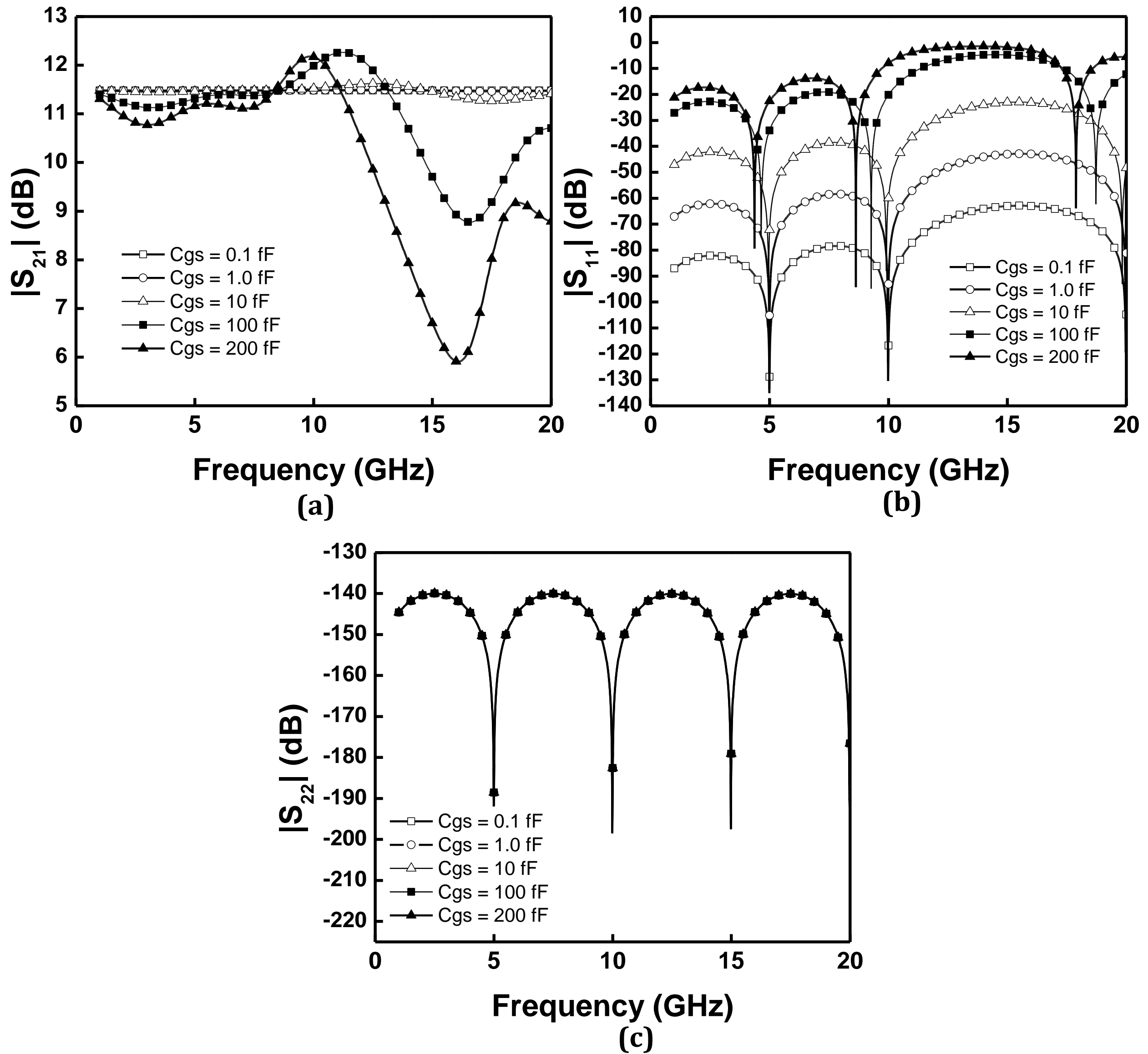


Fig. 2.13 Effect of gate-to-source capacitance (a) $|S_{21}|$ (dB); (b) $|S_{11}|$ (dB); (c) $|S_{22}|$ (dB)

Based on the simulated results it is seen that the value of C_{gs} can affect the return loss significantly. For a distributed amplifier with loaded transmission lines, increasing C_{gs} changes the characteristic impedance of the artificial transmission line. If the value of C_{gs} is very small, the characteristic impedance of the transmission line will be close to 50 Ohm and, hence, good input matching is achieved.

From the above graphs, it can also be seen that increasing C_{gs} reduces the cut-off frequency of the amplifier and it increases the ripples in the gain. However, an increase in C_{gs} does not affect the output return loss of the amplifier. This is because in this simulation we have assumed C_{gd} to be negligible.

2.5.2 Effect of Series Resistance R_i when C_{gs} = 100 fF

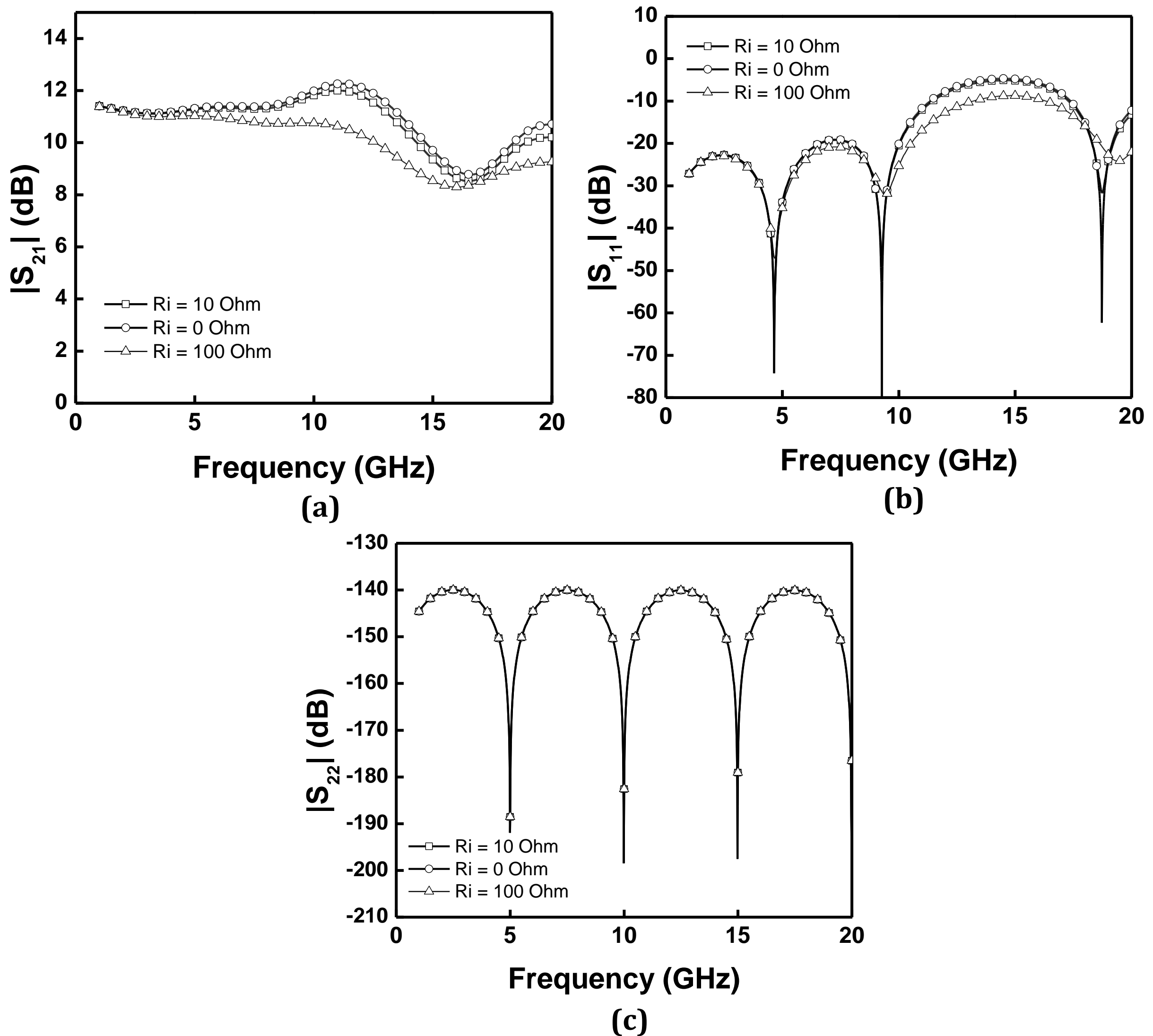


Fig. 2.14 Effect of Series Resistance R_i when C_{gs} = 100 fF (a) $|S_{21}|$ (dB); (b) $|S_{11}|$(dB); (c) $|S_{22}|$ (dB)

2.5.3 Effect of Series Resistance R_i when C_{gs} = 200 fF

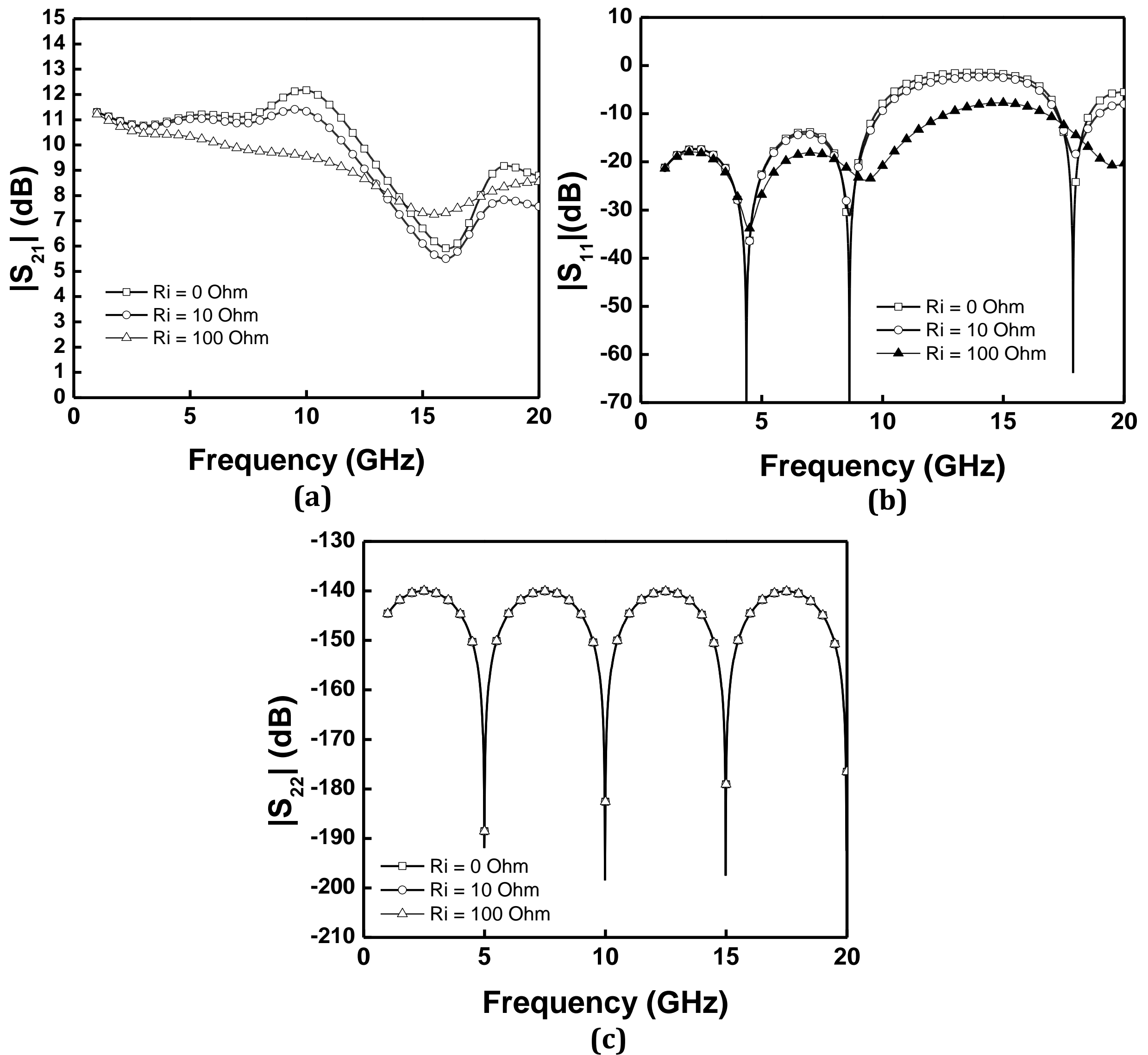


Fig. 2.15 Effect of Series Resistance R_i when C_{gs} = 200 fF (a) $|S_{21}|$ (dB); (b) $|S_{11}|$ (dB); (c) $|S_{22}|$ (dB)

Based on the above simulations, it can be seen that increasing R_i significantly affects the gain of the amplifier. This is due to the losses introduced by the resistance. On the other hand, it is also clear that this impact is more pronounced when C_{gs} is increased from 100 fF to 200 fF.

2.5.4 Effect of gate-to-drain capacitance when C_{gs} = 10 fF

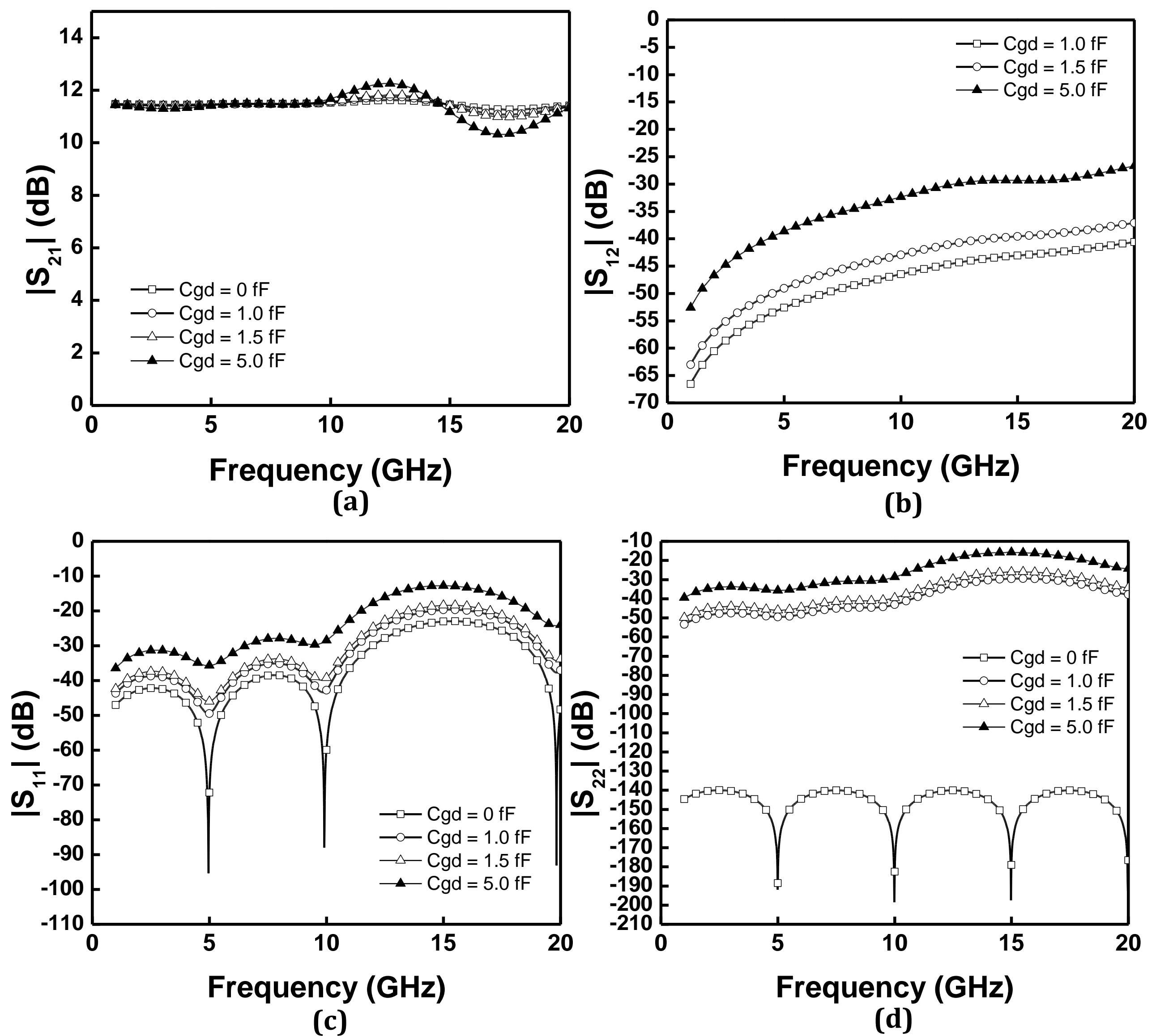


Fig. 2.16 Effect of gate-to-drain capacitance when C_{gs} = 10 fF (a) $|S_{21}|$ (dB); (b) $|S_{12}|$ (dB); (c) $|S_{11}|$ (dB); $|S_{22}|$ (dB)

For a typical discrete transistor, C_{gd} is around one tenth of C_{gs}. Hence, we have chosen values from 1.0 fF – 5.0 fF for C_{gd}. From the above graphs it is clear that C_{gd} affects the return loss, gain and output return loss.

2.5.5 Effect of Drain-to-Source Capacitance when C_{gs} = 10 fF and C_{gd} = 1.5 fF

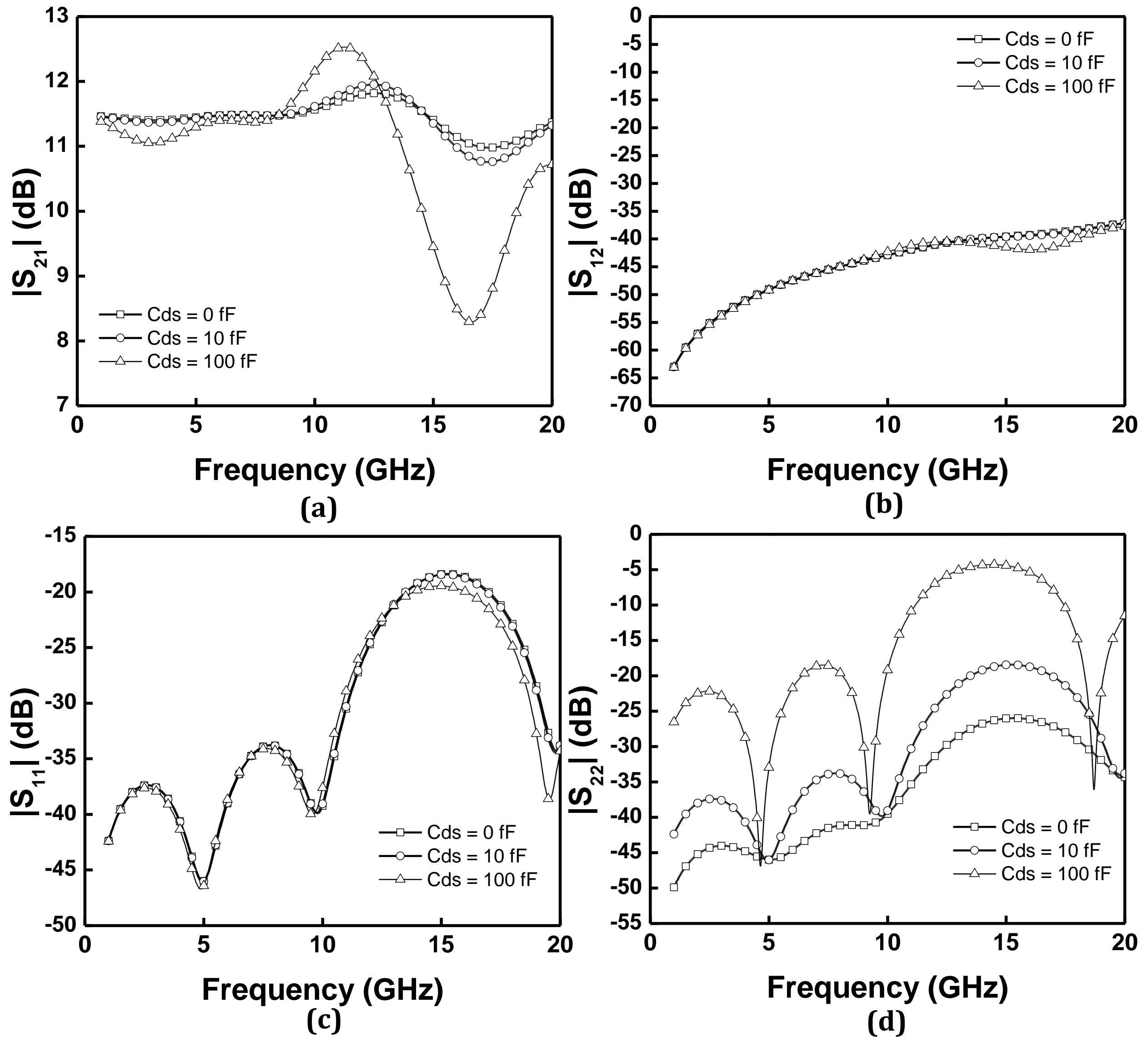


Fig. 2.17 Effect of Drain-to-Source Capacitance when C_{gs} = 10 fF and C_{gd} = 1.5 fF (a) $|S_{21}|$ (dB); (b) $|S_{12}|$ (dB); (c) $|S_{11}|$ (dB); (d) $|S_{22}|$ (dB)

Based on the simulations, output return loss is mostly affected by the value of C_{ds}. Because, when C_{ds} is present, the characteristics impedance of the drain-line is not equal to 50 Ohms. From the above simulations it is clear that parasitics introduced by the transistor tend to degrade the performance of distributed amplifiers. These parasitics are only contributions from the intrinsic part of a transistor. However, transistors with packages consist of many other parasitics due to the package itself. Therefore, designer needs to take account these contributions in order to design a working distributed amplifier.

2.6 Conclusions and Recommendations

In this chapter, the principle of distributed amplification is presented. Some of the performances such as power, noise and stability, are discussed and theoretical expressions are formulated based on previous research work. Agilent's ADS simulator is used to obtain insight into how the transistor intrinsic parasitics effect the distributed amplifier performance. Based on the simulation results, it is concluded that the amplifier return loss is mostly affected by the transistor gate-to-source capacitance (C_{gs}). Increasing C_{gs} also caused an increase in the ripples in the gain of the amplifier. An increase in the gate-to-drain capacitance (C_{gd}) also degrades the performance of the amplifier. The presence of C_{gd} also causes unnecessary oscillations due to the internal loops formed. To design a successful working amplifier it is recommended to include all the parasitic effects of the amplifier as well as the package parasitics.

CHAPTER 3

TRL Calibration and Measurement

3.1 Introduction

As described in the previous chapter, package parasitics degrade the performance of distributed amplifiers. In order to design a distributed amplifier by considering these effects, we measured the S-parameters of the transistors and used these results in our design. Passive components, such as inductors and capacitors, may not have a very high self-resonant frequency. Hence, we had to consider the behavior at higher frequencies of these components to design a broadband amplifier as well.

In this work, the TRL calibration technique for accurate measurement of active and passive components is discussed. Measurement results of measured components are presented, which were used in the design of a distributed amplifier.

3.2 S – Parameter measurement

3.2.1 Vector Network Analyzer

The vector network analyzer (VNA) is one of the most important instruments used to measure S-parameters of active and passive components. It generates a sinusoidal test signal that is applied to the DUT as a stimulus. Considering the DUT to be linear, the analyzer measures the response of the DUT, which is also sinusoidal. Fig 3.1 shows a block diagram of an N-port vector network analyzer which is based on a heterodyne principle [59].

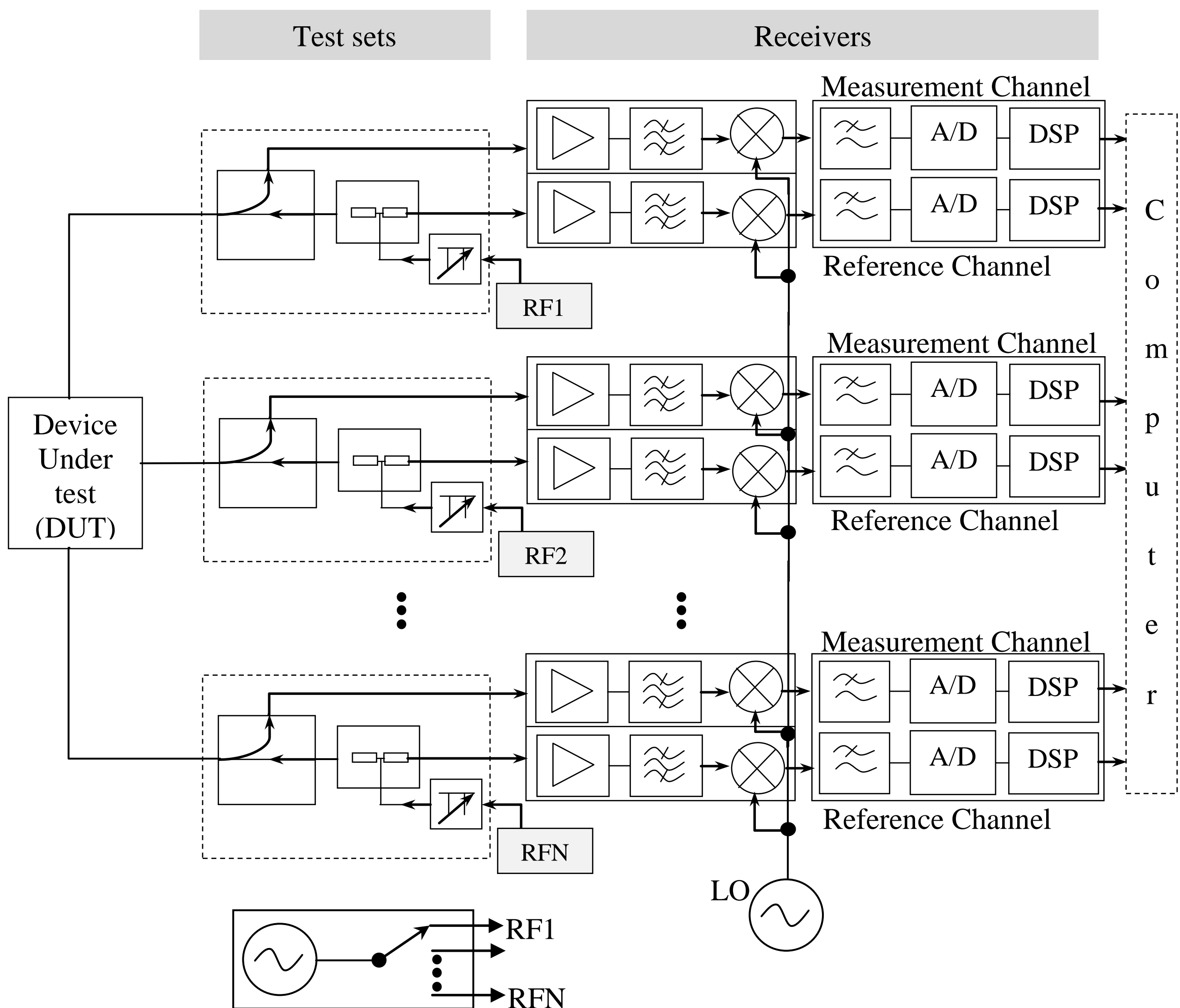


Fig. 3.1 Block diagram of a N-port vector network analyzer [59].

The test set separates incident and reflected waves by using directional couplers. The generator provides the RF signal which referred to as the stimulus.

Each test set combines with two separate receivers for the measurement channel and reference channel. They consist of a RF section, which down converts to IF signals, and a digital signal processing unit.

The computer is used to do the system error correction and displaying measurement data.

A VNA can perform full system error correction to compensate the systematic measurement error of the test instrument.

Before processing with measurement of components, we need to account for the systematic errors in the instrument and losses in the cables, and we also shifted the reference plane of the measurement. This was done by using the calibration process in which a network analyzer measures precisely known calibration standards and stores the vector differences between the measured and the actual values. Some of the calibration standards mostly used are short (S), open (O), load (L), match (M), through (T), reflect (R) and line (L).

The required calibration standard depend on the method of calibration used. There are many calibration methods available. Some of the techniques are TOM, TRM, TRL, TNA, SOLT and UOSM [60]-[62]. In this work we concentrate on the TRL calibration technique in order to measure the active and passive devices.

3.2.2 TRL (**T**HRU – **R**FLECT – **L**INE) Calibration

One of the major issues faced when making network analyzer measurements is the need to separate the effects of the transmission medium in which the device is embedded and testing [63]. Also in a microstrip test fixture there is a discontinuity at the coaxial to microstrip transition and also signal can be attenuated along the microstrip line, Fig 3.2. These effects can significantly change the measured data.

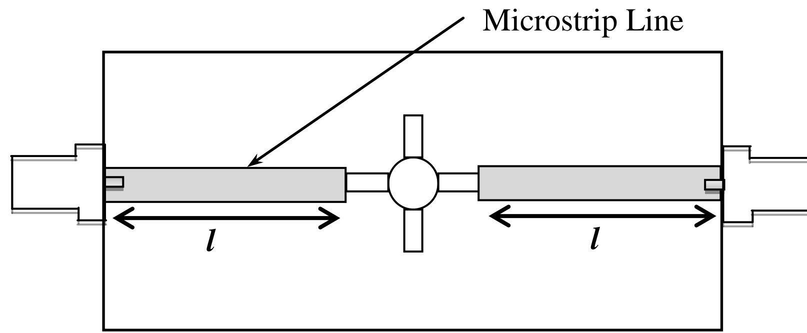


Fig. 3.2 Microstrip test fixture structure.

TRL calibration is a commonly used approach in which the calibration can be done until a specified reference plane. It is a THRU – RFLECT – LINE approach which is a 2 – port calibration that relies on transmission lines.

THRU – This refers to the connection of port 1 and port 2 directly or with a microstrip line. If a non-zero line is used, the mid-section of the microstrip line will be considered as the reference plane. The characteristic impedance Z_0 of the THRU line should be the same as the line standard. For a test structure similar to Fig 3.2, the THRU line is fabricated by connecting line l_1 and l_2 together as shown in Fig 3.3.

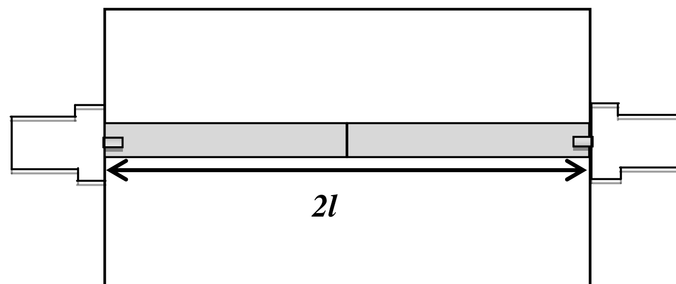


Fig. 3.3 THRU standard.

REFLECT – This one port standard exhibits a reflection coefficient $|\Gamma| > 0$, optimally 1.0. The exact reflection value is not requred to know, however, it must be identical at both test ports. The diagram of a REFLECT line is shown in Fig 3.4.

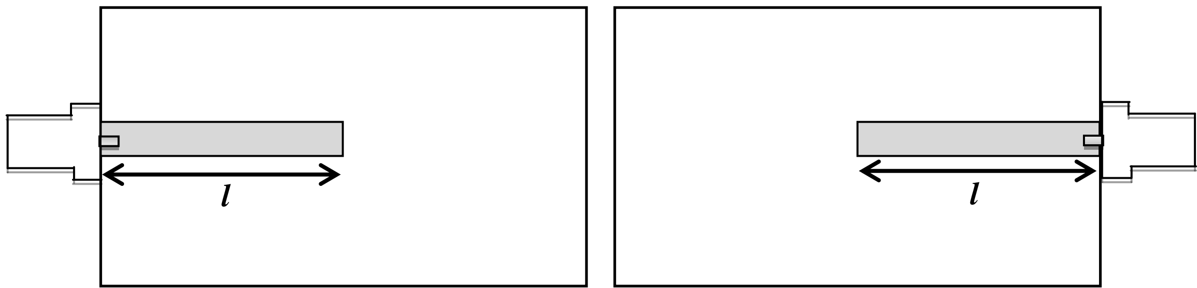


Fig. 3.4 REFLECT standard.

LINE – This is a two port standard in which the characteristic impedance of the line needs to be matched precisely possible to the reference impedance. In this standard a line is inserted between the fixture halves as illustrated in Fig 3.5.

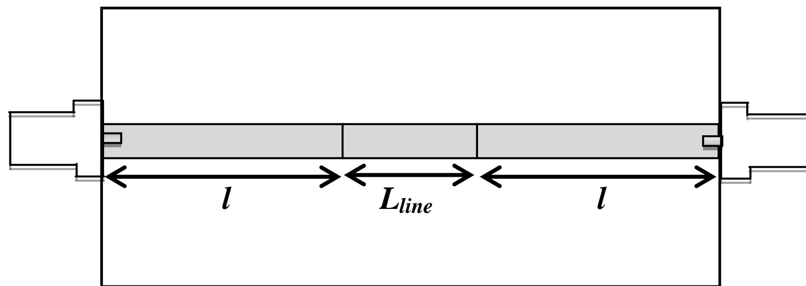


Fig. 3.5 LINE standard.

The electrical length of the L_{line} must be different than the length of the THRU standard used and also the length difference of these lines should not be equal to an integral multiple of half wavelengths since it will increase the measurement uncertainty significantly. Therefore, the frequency range for the calibration standard is restricted, because the phase difference between the two lines must be sufficiently different from 0° and 180° (e.g. it must be between 20° and 180° or the ratio of the stop and start frequencies must have a maximum ratio of 8:1). However, the frequency range of the calibration can be further increased by using multiple line standards.

Design of the calibration kit

In this work we designed a calibration kit for a frequency range 0.1 – 25 GHz. The length of the THRU line was 5.0 *cm*. Hence, the length of a reflect line was 2.5 *cm*. The substrate definition is shown in Fig 3.6, which is the same substrate used to measure the passive and active elements.

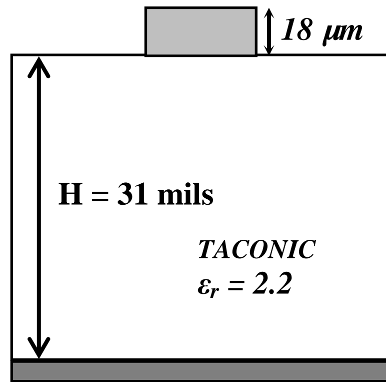


Fig. 3.6 Substrate definition

First, equation (3.1) was used to calculate a LINE with ¼ wavelength at centre frequency and is given by:

$$l = \frac{c}{4f\sqrt{\epsilon_{eff}}} \quad (3.1)$$

Where, c is the speed of light at free space, ϵ_{eff} is the effective dielectric constant of the substrate, f is the frequency.

At the centre frequency f = 12.55 GHz, the effective dielectric constant is ϵ_{eff} = 1.915.

Hence ¼ wavelength is calculated as $l_{\lambda/4}$ = 4.32 *mm*.

It is necessary to check whether the LINE meets the acceptable insertion phase requirement. The insertion phase of each line is given by

$$\frac{360 \times f \times l}{c} \quad (3.2)$$

Therefore at 0.1 GHz the insertion phase was = 5.1°. And at 25 GHz the insertion phase was = 129.6°

From the above calculation it can be seen that a 4.32 *mm* line does not meet the required insertion phase which is between 20° and 160°. This can also be verified by taking the ratio of 0.1 GHz to 25 GHz which is greater than 8. Therefore, the desired frequency span must be divided in to several sections.

Three frequency ranges were selected such that each span has a ratio less than 8. The selected frequency ranges are 0.1 GHz – 0.7 GHz, 0.7 GHz – 4.9 GHz and 4.9 GHz – 25 GHz. Hence, for this calibration kit we have used three lines. The total length of each line was obtained by adding the length of the THRU standard.

For LINE 1, the quarter wavelength at the centre frequency 0.4 GHz was calculated using (3.1) and it is equal to 13.682 *cm*. Therefore, the total length of LINE 1 is 5 *cm* + 13.682 *cm* = 18.682 *cm*.

Similar method is used to calculate the lengths of the other two lines. Table 3.1 below shows a summary of each of the lines calculated.

Calibration Standard	**Frequency Range (GHz)**	**Length (*cm*)**	**Delay (ps)**
THRU	0.1 - 25	5	230.6
REFLECT	0.1 - 25	2.5	
LINE 1	0.1 – 0.7	18.682	624.5
LINE 2	0.7 – 4.9	6.953	89.67
LINE 3	4.9 - 25	5.361	16.7

Table 3.1: Calculated length of the TRL calibration kit

Fig 3.7 shows the fabricated calibration standards.

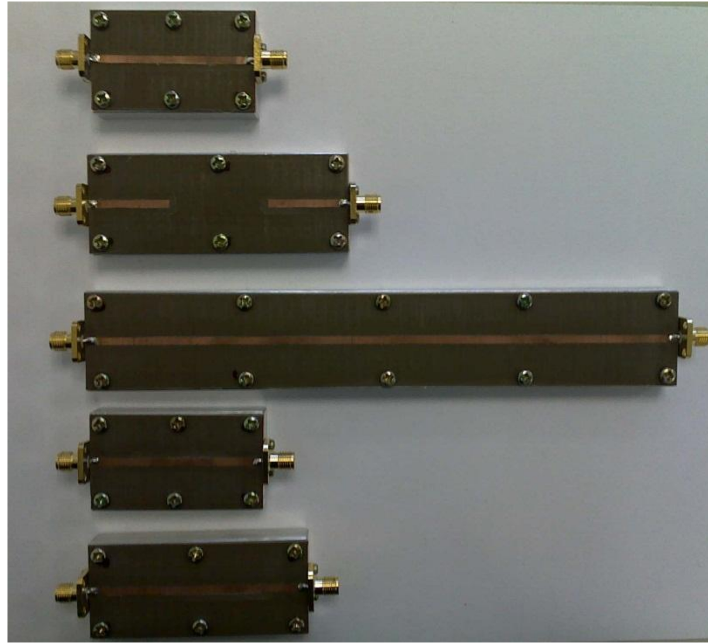


Fig. 3.7 Fabricated TRL calibration kit.

In order to measure the transistor we need to bias it using bias tees. Therefore, calibration was done by adding bias tees in between the test fixture and the coaxial cable. To verify that the calibration was done accurately, we measured the S-parameters of the THRU standard. Fig 3.8 and Fig 3.9 show the measured S-parameters for the THRU standard with and without bias tees respectively. The calibration was conducted using the Rohde & Schwarz ZVA 50 vector network analyzer.

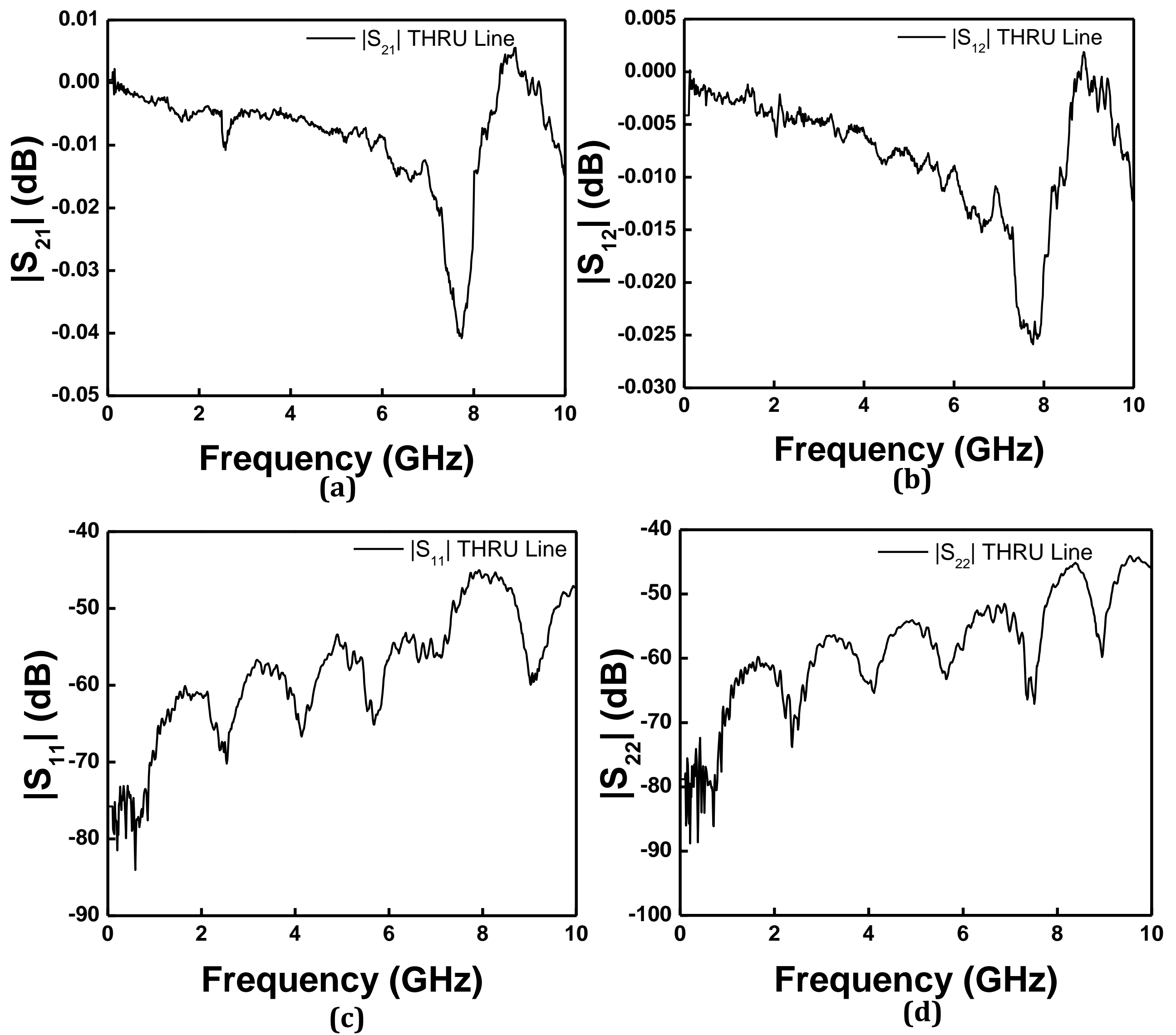


Fig. 3.8 S-parameters of the THRU standard (a)$|S_{21}|$ (dB); $|S_{12}|$ (dB); (c) $|S_{11}|$ (dB); (d) $|S_{22}|$ (dB).

Theoretically $|S_{21}|$ and $|S_{12}|$ of the THRU line should be 0 dB since the effects of the transmission lines are removed after calibration. From the above figure it can be seen that $|S_{21}|$ and $|S_{12}|$ of the THRU standard are close to 0 dB between 0.1 GHz and 10 GHz. Furthermore, the input and output reflection coefficients should be as small as possible. In this calibration, the return loss of the THRU standard is better than 45 dB, which is a good input match. Similar results were obtained for the calibration with bias tees.

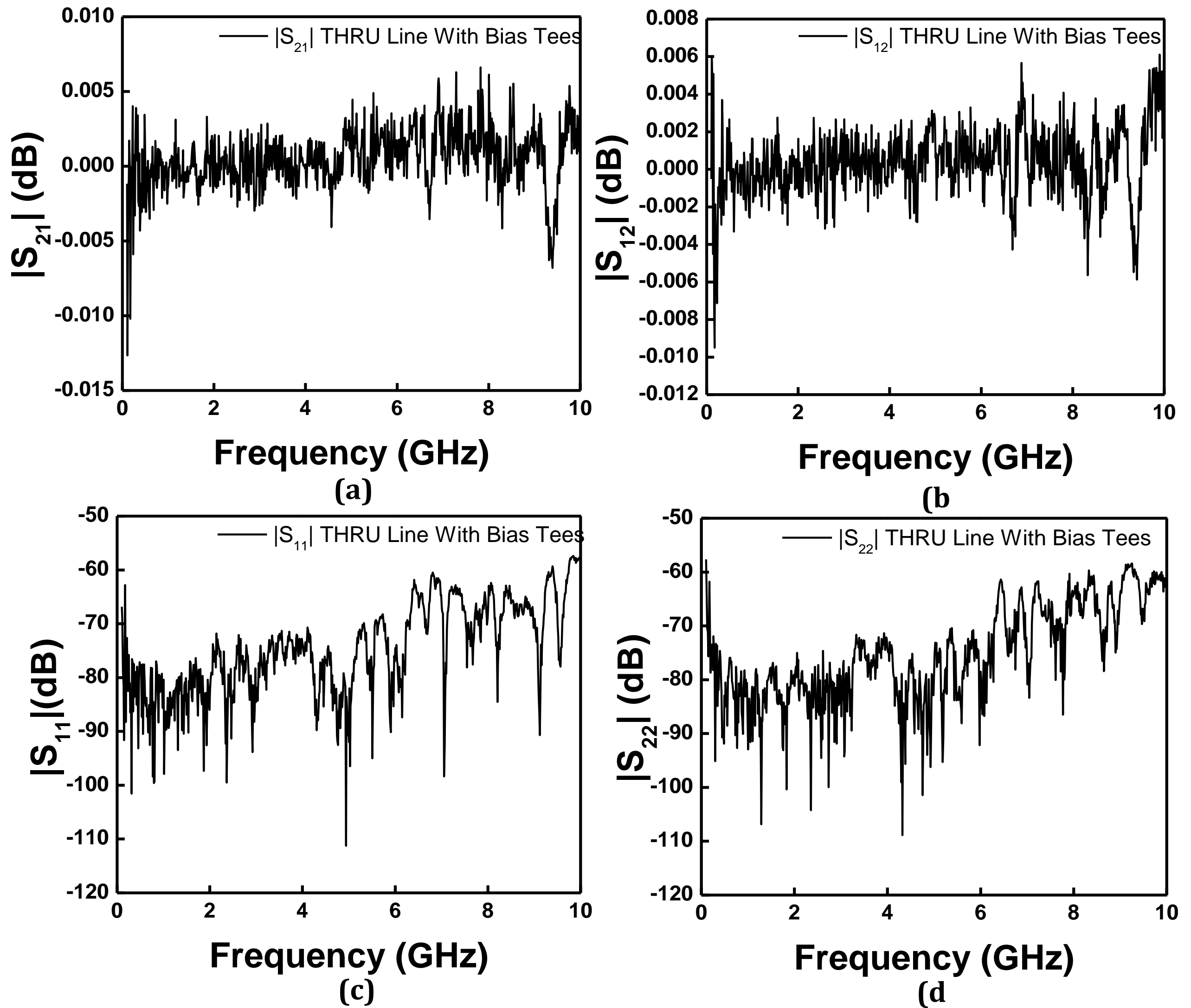


Fig. 3.9 S-parameters of the THRU line with bias tees (a) $|S_{21}|$ (dB); (b) $|S_{12}|$ (dB); (c) $S_{11}|$ (dB); (d) $|S_{22}|$ (dB).

3.3 Measurement of Active and Passive devices

3.3.1 Measurement of the transistor

In this work we concentrate on designing a low noise distributed amplifier. The Avago ATF-36077 pHEMT transistor was chosen as the transistor which has a very low noise figure of 0.5 dB even at 12 GHz and it has an operating frequency of up to 18 GHz. The transistor was measured at V_d = 1.5 V and V_g = -0.1 V. Fig 3.10 shows the S–parameter measurement results at V_d = 1.5 V and Vg = -0.1 V.

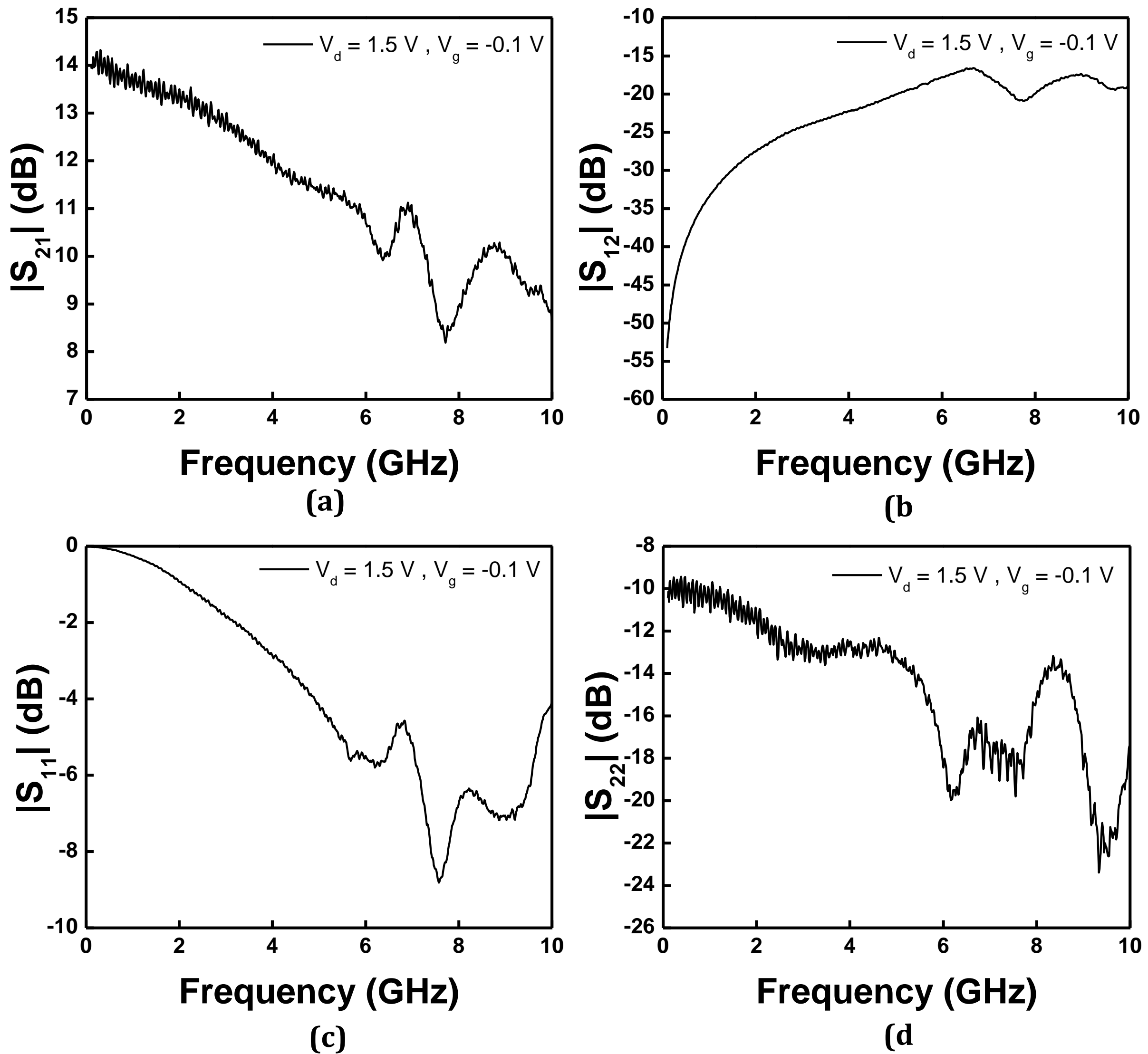


Fig. 3.10 Measured S-parameters of the ATF-36077 transistor (a) $|S_{21}|$ (dB); (b) $|S_{12}|$ (dB); (c) $|S_{11}|$ (dB); (d) $|S_{22}|$ (dB)

3.3.2 Measurement of the passive devices

For designing the amplifier we need several passive devices, such as the 50 Ohm terminating resistor, resistors for gate biasing, DC block capacitors and RF de-coupling and inductors for RF chokes. For DC block and RF de-coupling we chose SMD components of a capacitor of 100 pF and for the RF choke we chose an inductor of 100 nH. Figures below show the measurement results for each of the surface mounted component types. The measurement results have also been compared with an ideal element to get an insight into how these components works at high frequencies.

Measurement Comparison of a 100 nH Inductor

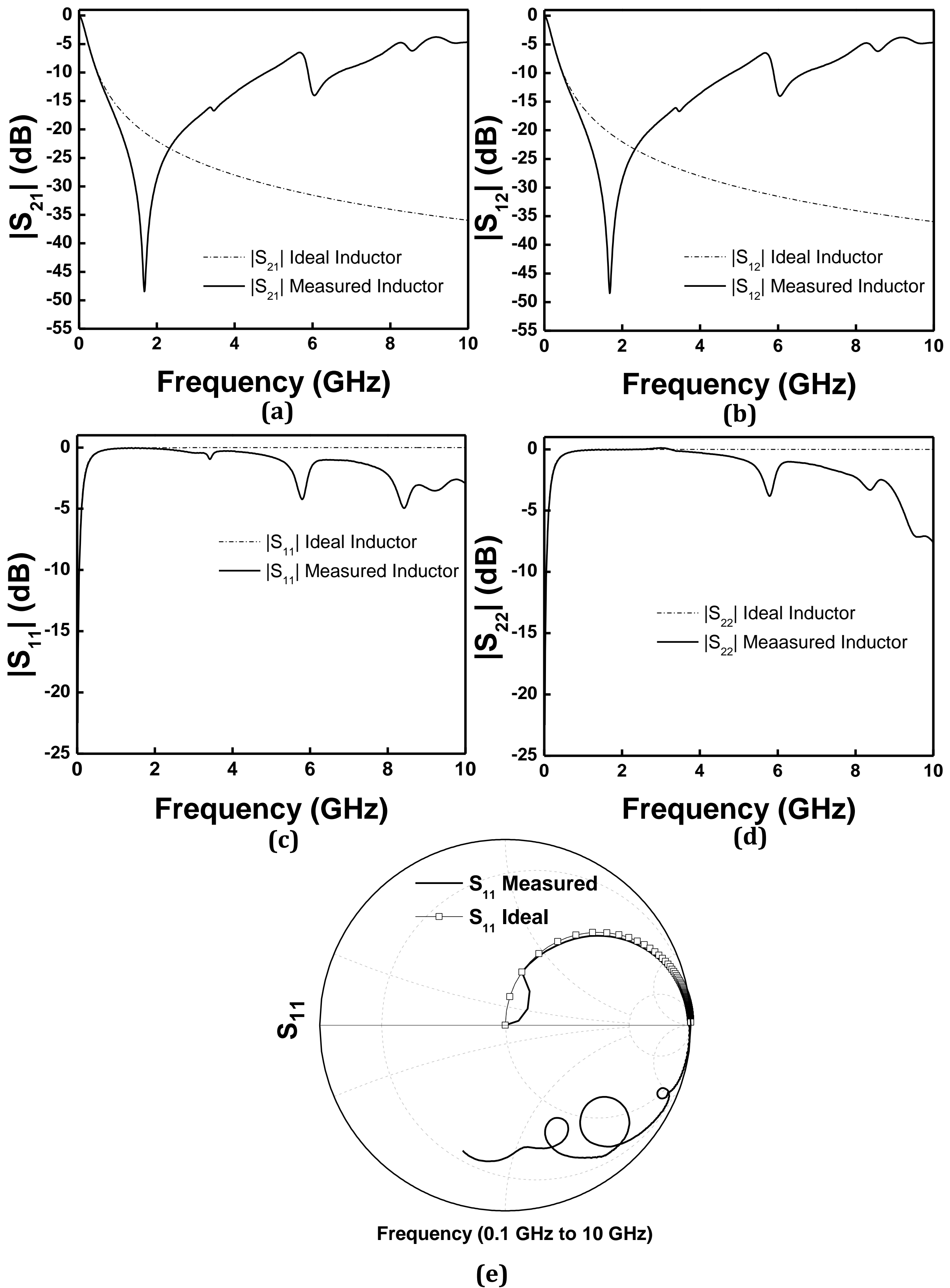


Fig. 3.11 Measured S-parameters of a 100 nH Inductor (a) $|S_{21}|$(dB); (b) $|S_{12}|$ (dB); (c) $|S_{11}|$ (dB); (d) $|S_{22}|$ (dB); (e) $|S_{11}|$ Smith chart.

Measurement Comparison of a 100 pF Capacitor

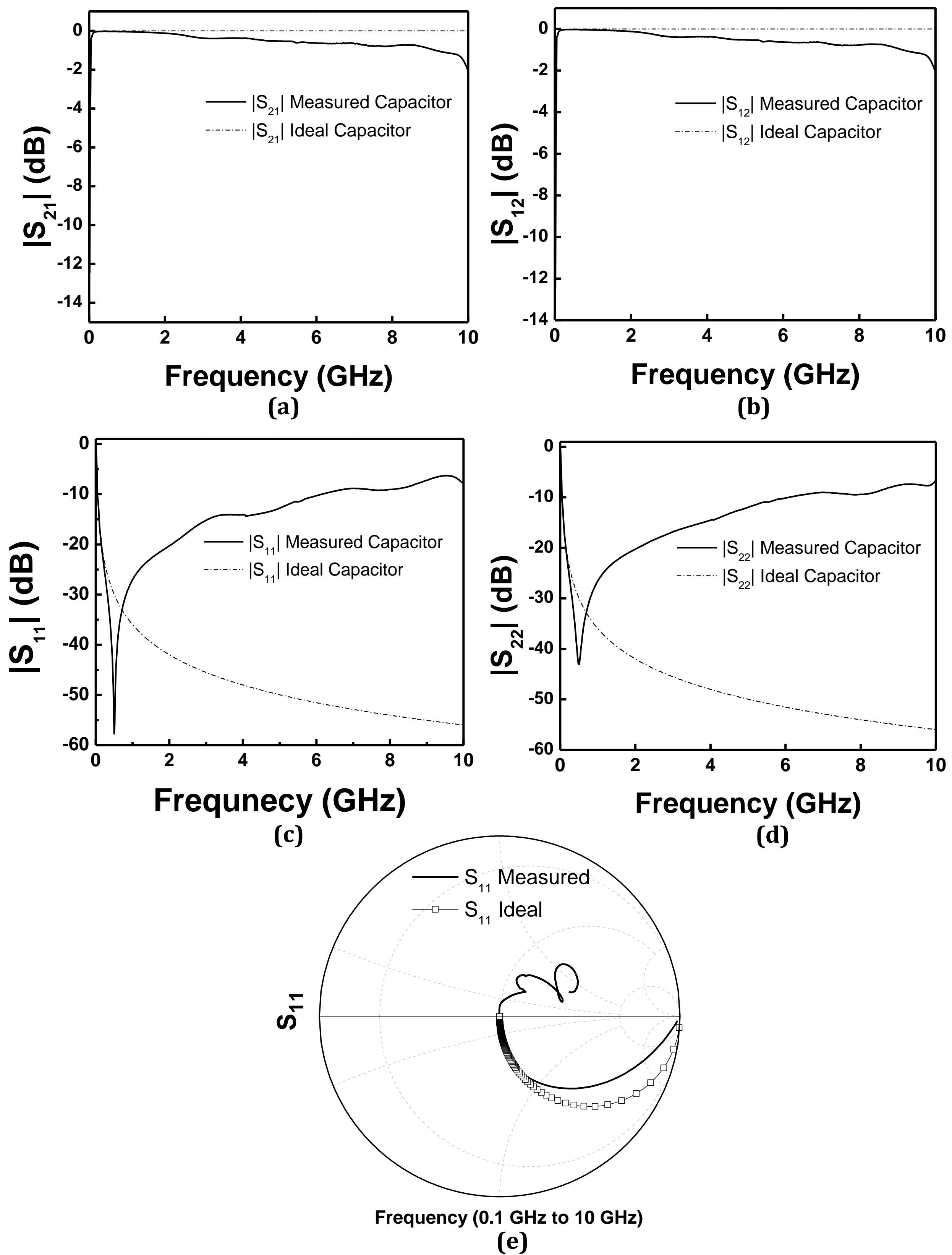


Fig. 3.12 Measured S-parameters of a 100 pF Capacitor (a) $|S_{21}|$ (dB); (b) $|S_{12}|$ (dB); (c) $|S_{11}|$ (dB); (d) $|S_{22}|$ (dB); (e) $|S_{11}|$ Smith chart.

Measurement Comparison of a 50 Ohm Resistor

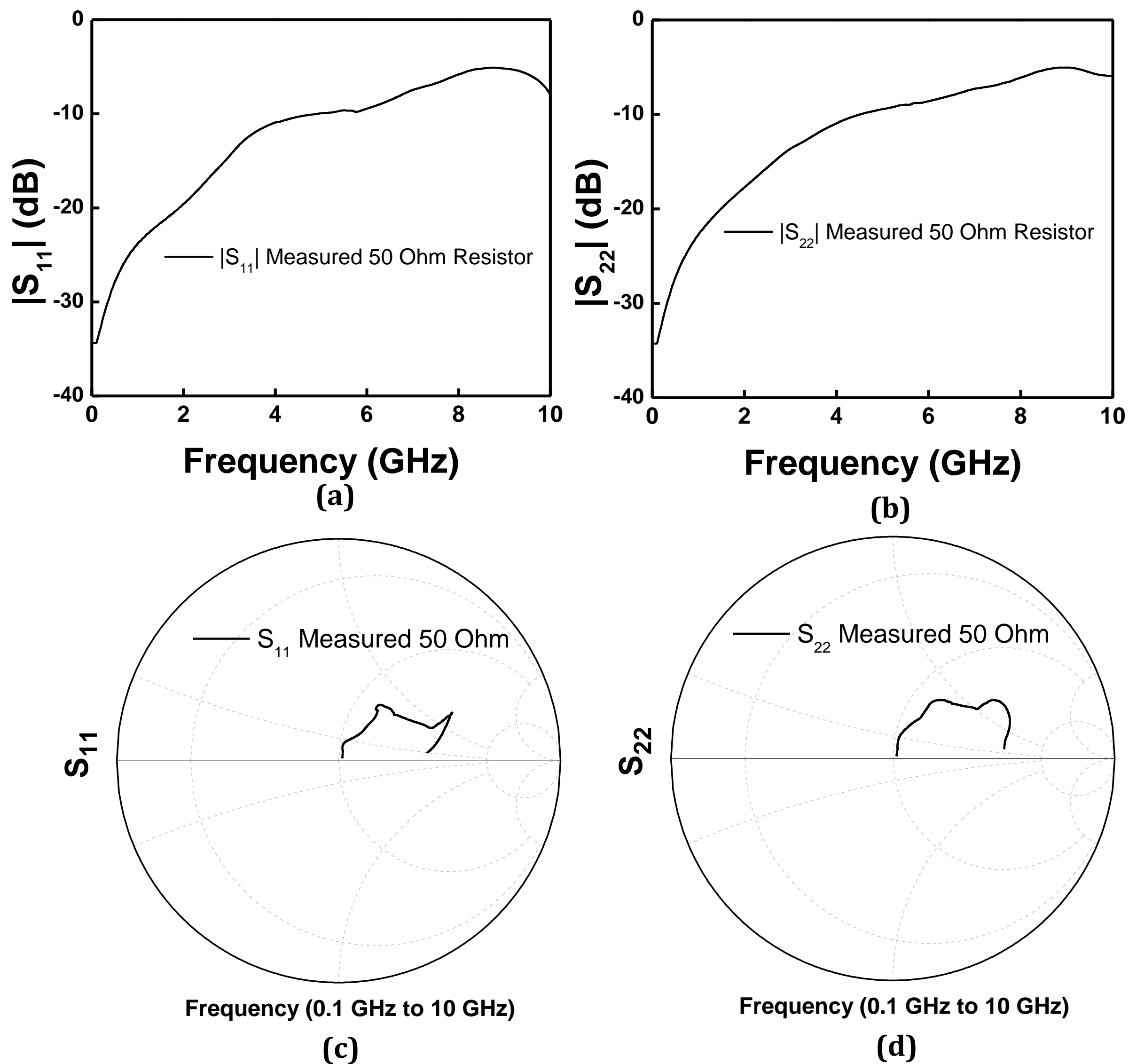


Fig. 3.13 S-parameter measurement of a 50 Ohm resistor (a) $|S_{11}|$ (dB); (b) $|S_{22}|$ (dB); (c) $|S_{11}|$ Smith Chart; (d) $|S_{22}|$ Smith Chart.

An ideal inductor which is terminated by a 50 Ohm resistor is matched at 0 GHz and moves towards the infinity point in the smith chart as shown in Fig 3.11. However, based on the measurement it is apparent that at high frequencies it behaves as a capacitor. This is due to the fact that the measured inductor has a low self-resonant frequency. Based on the measurement, the inductor behaves properly up to 900 MHz. Fig 3.12 shows similar measurement conducted for the 100 pF capacitor. An ideal capacitor starts from infinity and

moves towards the centre of the Smith chart at high frequencies. However, based on the measurement, the self-resonant frequency of the capacitor is around 500 MHz. Fig 3.13 shows a comparison of a 50 Ohm resistor where port two is grounded. An ideal response should have a infinite return loss and it should be in the centre of the Smith chart. However, measured resistor behaves differently than expected. This might be due to the package parasitics of the surface mounted resistor.

Based on the above comparison, it is apparent that it is necessary to include the high frequency behavior of these surface mounted devices when designing a broad band amplifier up to several GHz.

3.4 Conclusions and Recommendations

Accurate measurements of active and passive devices are important when designing a broadband amplifier for several Gigahertz. Calibrating and de-embedding is a crucial step in microwave measurement. In this chapter, the method of TRL calibration was introduced for accurate calibration and de-embedding purposes.

It is found that the measured passive components, such as inductors and capacitors, have a very low resonant frequency below 900 MHz. Also, the working frequency of a 50 Ohm resistor was in the range of several Megahertz. Including these high frequency effects was necessary in the design in order to obtain a wide bandwidth and also to avoid any unnecessary oscillations due to high frequency parasitics.

CHAPTER 4

Design of a Distributed Amplifier

4.1 Introduction

The measured active and passive components in the previous chapter are incorporated in the design of the distributed amplifier. This chapter mostly concentrates on designing a distributed amplifier using these measured active and passive components. Distributed amplifier described in this chapter uses the topology of the traveling-wave amplifier which contains microstrip transmission lines instead of lumped inductors. The substrate used is the same substrate used to calibrate and measure the active and passive components.

In this chapter the design flow used to design the amplifier is presented. The design was conducted to obtain the maximum possible bandwidth using the measured S-parameter of the components. Also some of the important parameters which were needed to consider such as stability and electromagnetic coupling are considered. EM simulations using Sonnet, EM ADS Momentum and AWR Axiem are compared with the schematic simulation results. The final measurement results of the fabricated amplifier is compared with the simulated performance. Also some of the issues met during the measurement are presented.

4.2 Circuit Realization

4.2.1 Bends, Meander Lines and T-Junctions

In all of the analysis presented in chapter 2, the transmission lines were assumed to be straight lines and lossless. However, in reality the layout included a large number of discontinuities such as bends, T- junctions and meander lines as shown in Fig 4.1. These discontinuities may introduce undesirable results for the final amplifier design. In order to predict the accurate results, it is necessary to consider the effects of such microstrip discontinuities.

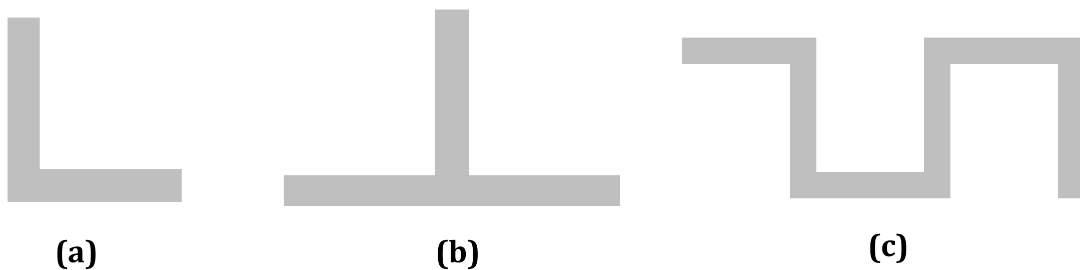


Fig. 4.1 Microstrip discontinuities (a) Bend; (b) T - junction; (c) Meander line.

4.2.2 Stability Analysis

Stability analysis is an important criterion to check in any amplifier design. As depicted in chapter 2, the oscillations in distributed amplifiers mostly occur at high frequencies and it is mainly due to the internal loops formed by the transconductance and the feedback capacitance C_{gd} of the transistor combined with the transmission lines. Some of the standard methods to analyze the unconditional stability is to perform K - Δ test or to check the μ factor.

The K - Δ test or the *Rollet's condition* is defined as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \ > \ 1, \qquad (4.1)$$

and

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \ < \ 1, \qquad (4.2)$$

Testing μ factor is a newly proposed method which contains only single parameter μ and it is defined as:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \qquad (4.3)$$

However, the above tests may not be sufficient for the stability analysis of a distributed amplifier [55]. This is because even if the above test indicates that the overall amplifier is stable, it is still possible that the distributed amplifier is unstable due to the inter-stage loops formed. These loops exist due to the parasitic C_{gd} in the FET. Another method to check stability is to use S-probes developed by Campbell and Brown [64]. An S-probe can be inserted at any place of a circuit without any loading. The function of an S-probe is to obtain the input Z_1 and output Z_2 impedance at either side of the inserted element. Hence, we can obtain the input Γ_1 and output Γ_2 reflection coefficients at either side of the element. The condition for unconditional stability is:

$$Re(\Gamma_1\Gamma_2) < 1 \qquad (4.4)$$

If the above relation is fulfilled then the condition for oscillation will never be satisfied.

4.2.3 Schematic Design and Simulation

Table 4.1 summarizes the design specifications of the amplifier.

Supply Voltage	1.5 V
Bandwidth	> 3.0 GHz
Gain	> 10 dB
Input Return Loss	> 10 dB
Output Return Loss	> 10 dB
Isolation	> 10 dB

Table 4.1: Amplifier Design Specifications

In order to begin the design, values were estimated for the unknown transmission line lengths and widths of the gate and drain lines. Next these values were optimized using the simulator optimization tool. To obtain flat gain, broad bandwidth and good return loss, we first optimized the lengths of the transmission lines by maintaining the initial estimated widths. Next the same procedure was repeated by introducing T-junctions, at each gate and drains of the FET which connects to the gate and drain lines respectively. Next, we optimized the widths of the gate and drain transmission lines to obtain the desired input and output return loss. While performing the optimization it was also necessary to make sure that the amplifier is stable throughout the desired bandwidth. To ascertain that the amplifier is stable, $K - \Delta$ test and μ factor were simulated. Since these tests may not be sufficient for stability analysis of distributed amplifiers, S-probes were also used at each input and output node of the transistor.

It is also necessary to include tapering whenever there is a microstrip step is involved. For example, in this design tapering was used whenever there was a passive component such as a capacitor, since the pad width of the capacitor is different from the gate and drain transmission lines. These effects were included as well.

Eventhough we had the S-parameter files for the transistors, it was still necessary to investigate the effect of DC biasing on the designed circuit. For the gate biasing we used a 1 kΩ resistor, 100 pF RF decoupling capacitor and a 100 nH RF choke. For the drain biasing

a 100 nH RF choke and a 100 pF RF decoupling capacitor are used. The T-junctions connecting to these biasing sections also affected the performance of the amplifier.

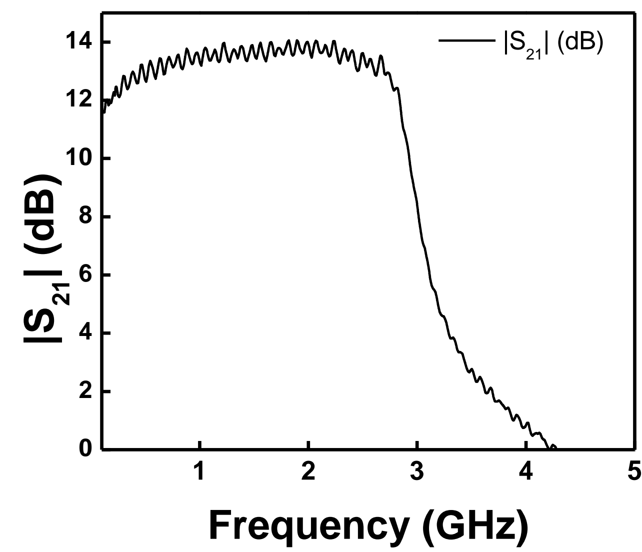
Table 4.1 shows the optimized lengths and widths of gate and drain lines. From this table it can be seen that the length of a drain line section is longer than the length of the gate line section. This may be due to the differences between FET's gate-to-source capacitance and FET's drain-to-source capacitance. For a typical FET the drain-to-source capacitance is smaller than gate-to-source capacitance. As described in Chapter 2, to obtain a useful gain, the phase shift per gate and drain lines has to be equal. Therefore, to equalize the phase the length of drain line is usually made longer than the length of gate line.

Unknown Parameters	Optimized Value (mm)
L_g	17.6
W_g	1.4
L_d	19.2
W_d	1.0
L_g_In	10
W_g_In	2.3
L_d_In	10
W_d_In	2.7

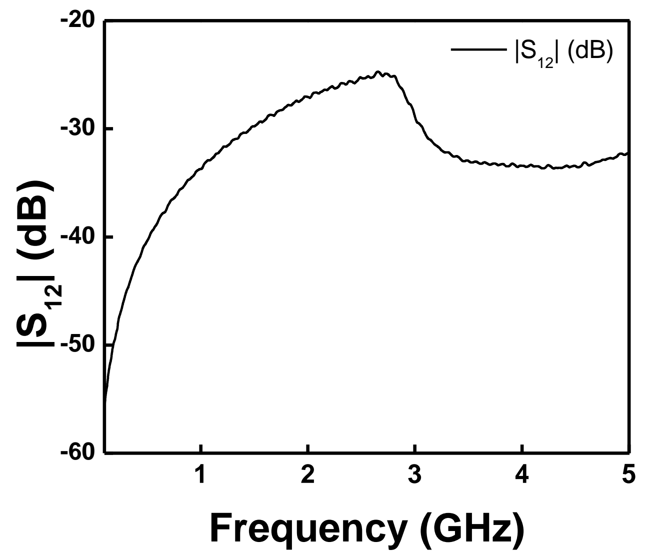
Table 4.2: Optimized lengths and widths of gate and drain lines of the amplifier

Meander lines were used to design the gate and drain lines of the amplifier. The final circuit was optimized to obtain a bandwidth from 0.1 – 3.0 GHz. The input return loss of the amplifier is better than 20 dB throughout the bandwidth. Fig 4.2 shows the schematic diagram and Fig 4.3 shows the simulation results.

Fig. 4.2 Schematic Diagram of the amplifier



(a)



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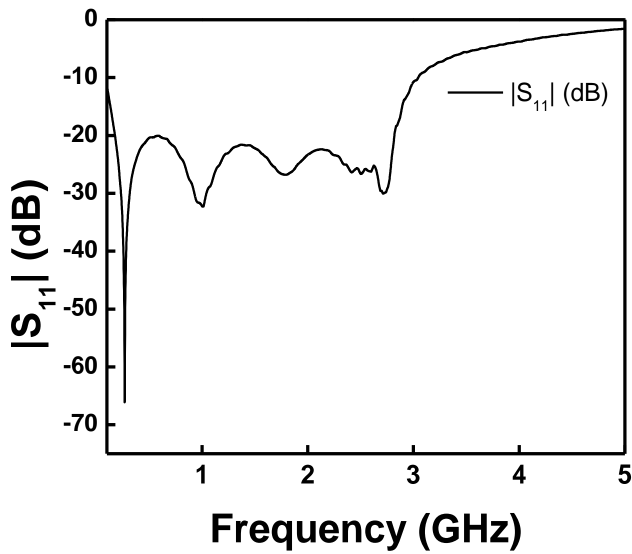

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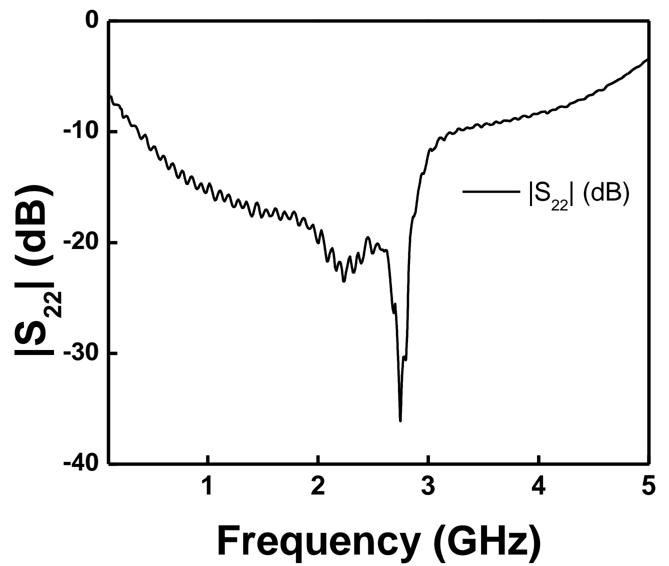

(d)

Fig. 4.3 Schematic simulation results of the amplifier.

4.2.4 Electromagnetic Simulation Results

Fig 4.3 shows the layout of the designed circuit. The schematic simulation result shown before does not account for any coupling between the transmission lines. For example, the inductive coupling between the meandered lines could influence the performance of the amplifier. Also, it is necessary to check whether there is significant coupling between the gates and drain lines which may cause oscillation. The layout was simulated using Sonnet EM simulator, ADS momentum and AWR Microwave Office Axiem. Fig 4.5 shows the final simulation results.

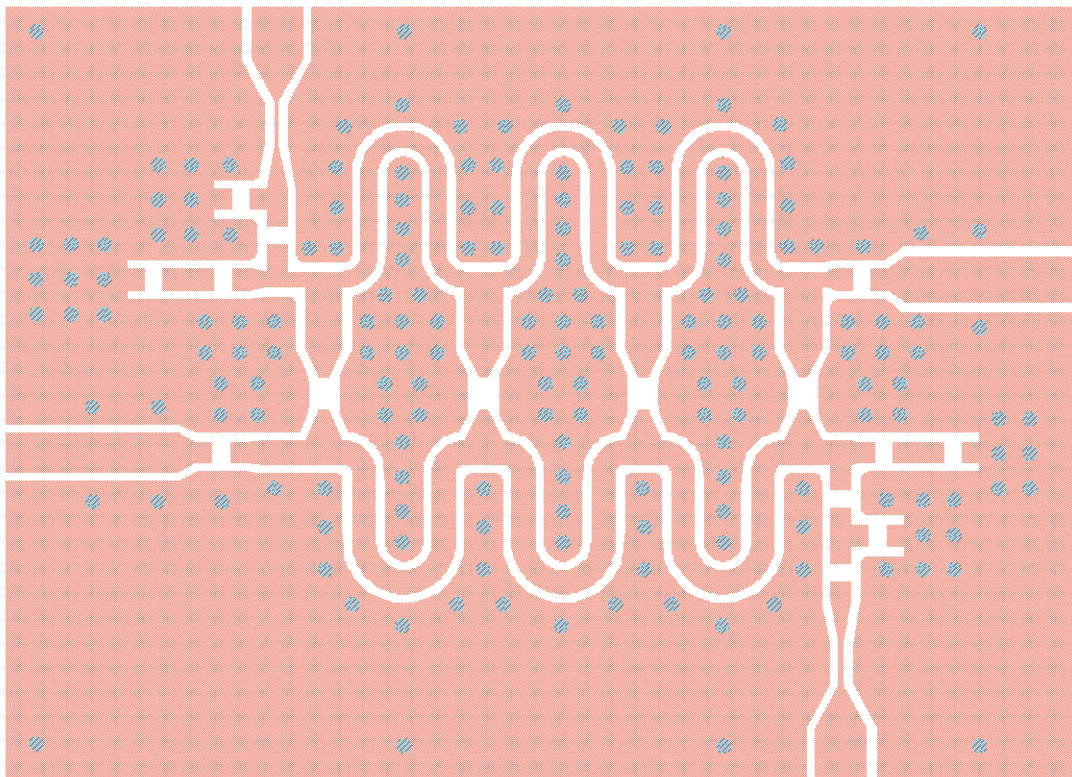

Fig. 4.4 Layout of the distributed amplifier.

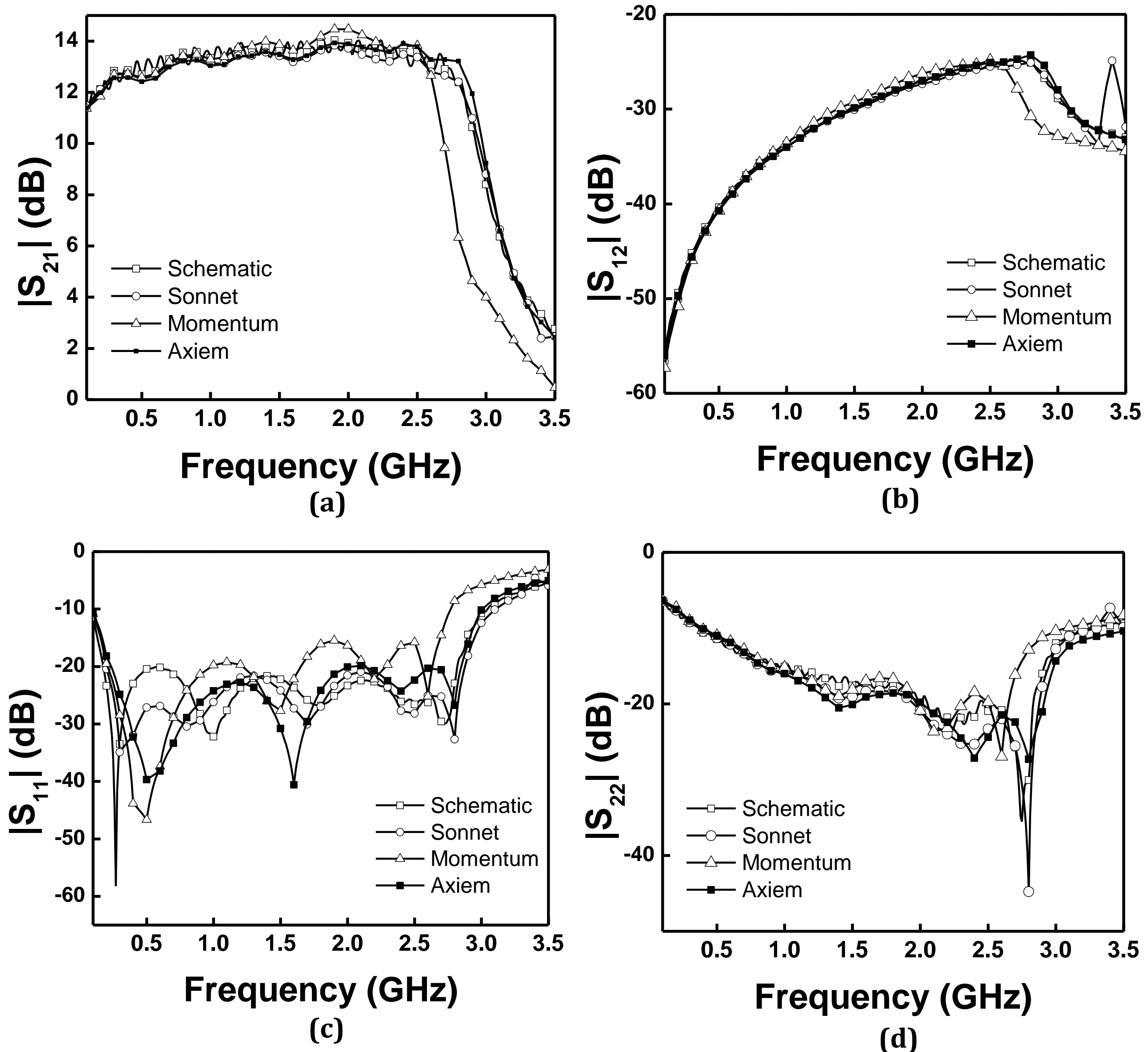

Fig. 4.5 Comparison between schematic simulation and EM simulation.

The final circuit designed was fabricated using the TACONIC substrate with dielectric constant 2.2. Fig 4.6 shows an image of the actual fabricated circuit design.

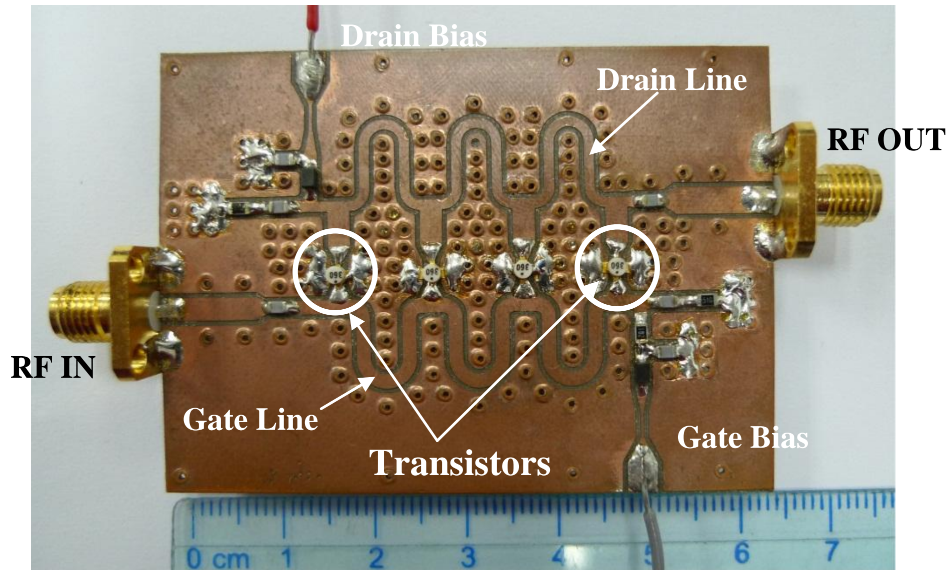

Fig. 4.6 Fabricated amplifier

4.3 Measurement and Discussion

4.3.1 DC Measurement and Check for Oscillations

Before measuring the S-parameters, it was necessary to check whether the circuit draws the expected DC current and whether there are any oscillations. The transistor used in this device is a GaAs PHEMT device which requires a negative gate voltage and a positive drain voltage to operate at a specific quiescent operating point. Details of this device are provided in Appendix B. The proper biasing sequence for a GaAs device is to pinch off the device with a higher negative voltage, followed by the drain voltage [65]. Next, a higher positive voltage is applied to the gate up to the desired operating point. This is because applying the drain voltage before the gate voltage could damage the device. The total DC current of the final amplifier was 105 mA at a drain voltage of 1.5 V and gate voltage of -0.1 V.

The next step is to ensure that the amplifier is not oscillating at the DC biasing point. This is a necessary step in amplifier measurement since oscillations could damage the VNA during the S-parameter measurements. A spectrum analyzer was used to ensure that there are no oscillations in the amplifier. Oscillations in the amplifier can be detected then from the spectrum analyzer.

4.3.2 S – Parameter Measurement Results

An HP 8510C vector network analyzer is used to measure the amplifier's S-parameters. Before starting the measurement a normal calibration was performed to eliminate the VNA errors. Fig 4.7 shows a comparison between the measured and the simulated results. Based on the results, it is evident that the discrepancy in the gain between measurement and simulation is significant. The return loss of the measured device is better than 15 dB.

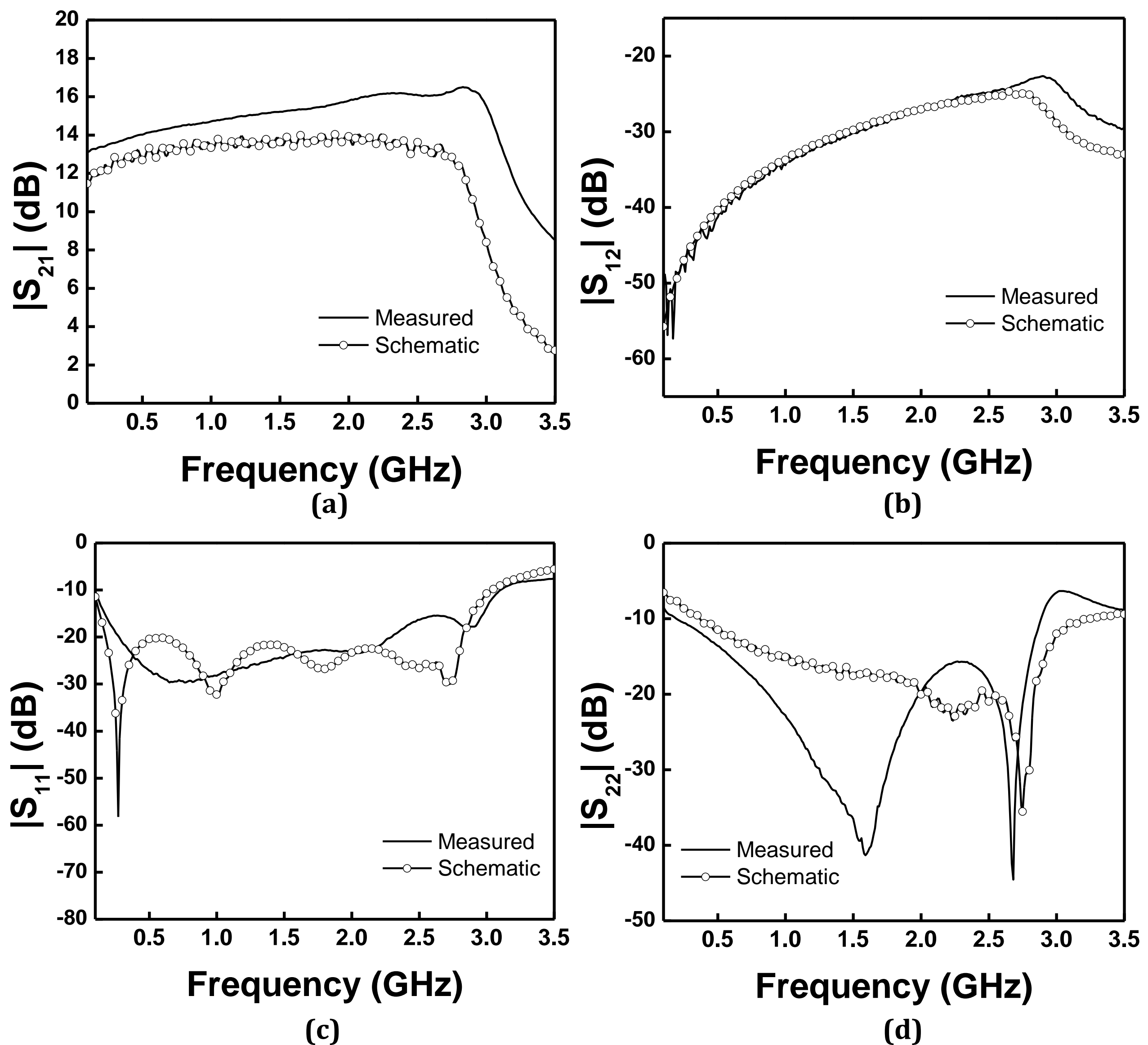

Fig. 4.7 Measured and simulated S –parameters.

To investigate the discrepancies, the transistor was re-measured using the VNA. HP8510C VNA was used to conduct the TRL calibration and measurement. It was found that the measured S-parameters of the transistor were different from the previously completed measurements in Rohde & Schwarz ZVA 50 VNA. Fig 4.8 shows a comparison between the two measurement results.

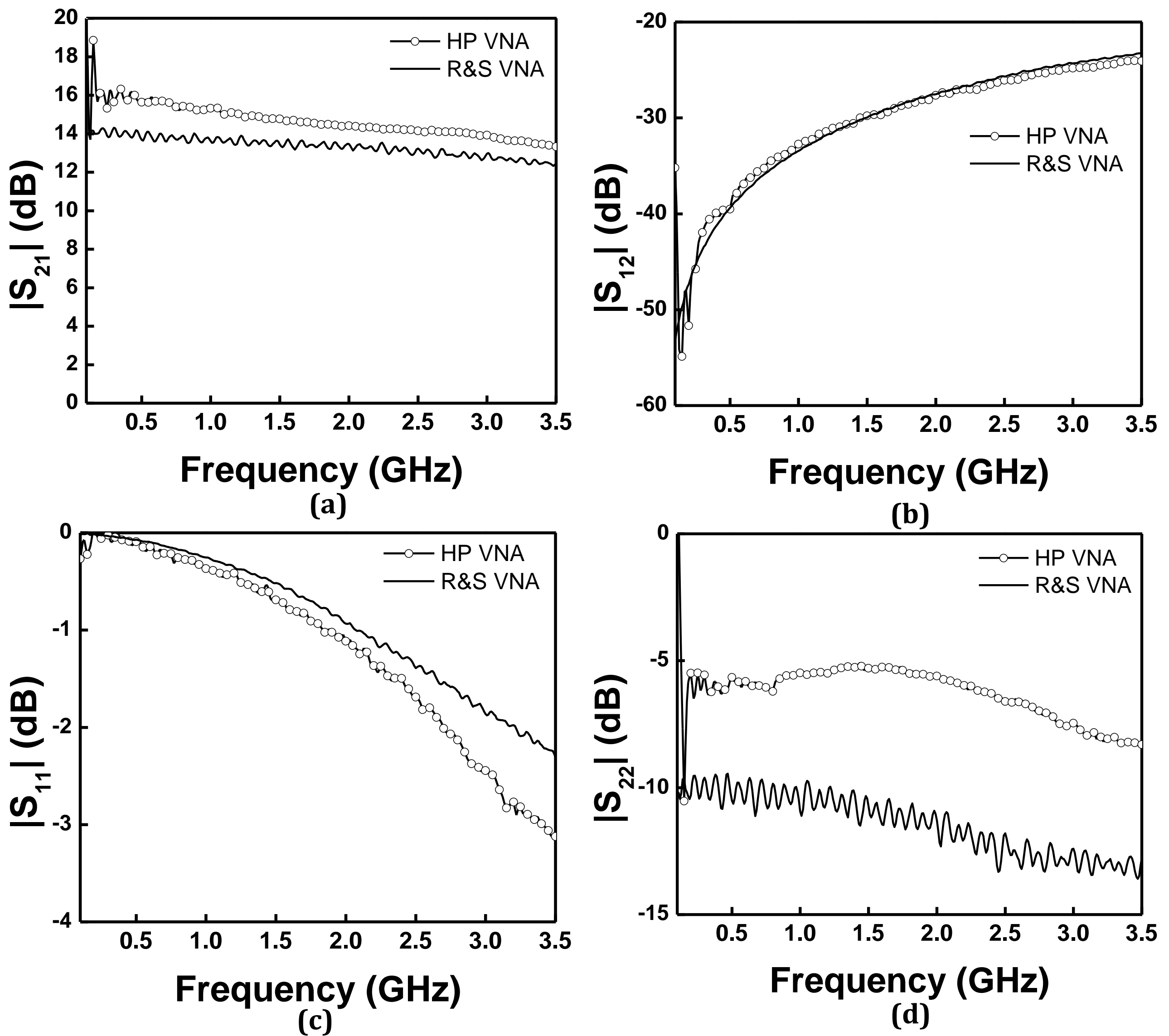

Fig. 4.8 Comparison between measured S-parameters of the transistor using Agilent VNA and R&S VNA

Next, the newly measured transistor S – parameters were used in the simulation. Fig 4.9 shows the comparison between the measured and the simulated S-parameters of the amplifier. It can be seen that the measured and simulated results are much closer than the previous comparison. However, there is still a slight discrepancy between the measured and simulated results. Further investigations were conducted to understand the reasons for the discrepancies.

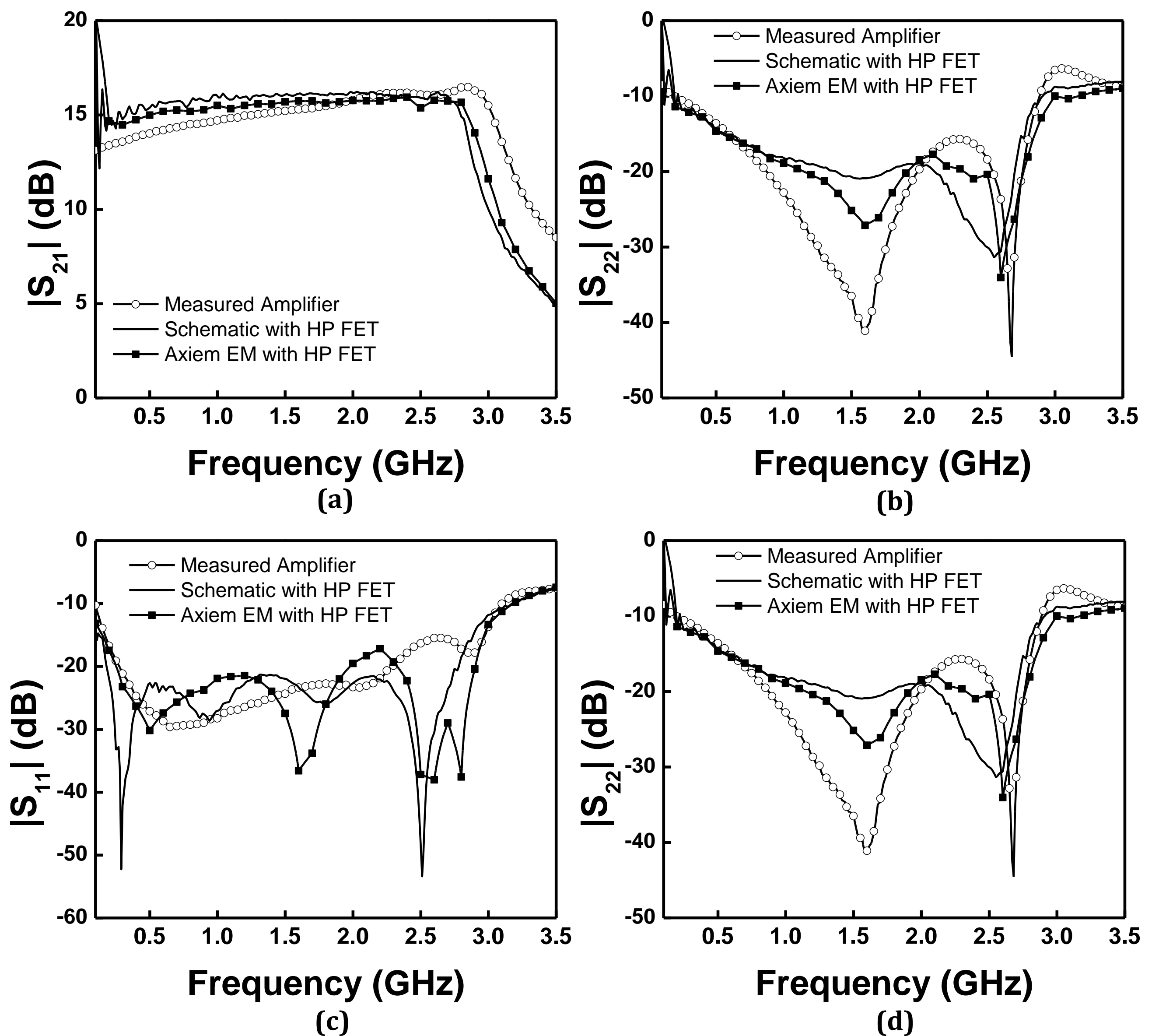

Fig. 4.9 Comparison between measurement and schematic simulations using transistor measured in HP VNA.

The minimum input power of the HP8510C VNA is about -10 dBm. This input power level may be high enough to change the transistor's small signal performance. Therefore, the circuit was measured again with -20 dBm and -30 dBm input power levels. Attenuators were used to provide an input power level of -20 dBm and -30 dBm. To obtain accurate results, first 10 dB and 20 dB attenuators were measured using the VNA. Next, the amplifier was measured by connecting the attenuators at the input of the amplifier. The S – parameters of the amplifier are obtained by using ABCD parameters as shown below.

$$[ABCD]_{At}[ABCD]_{A0} = [ABCD]_{Al} \quad (4.5)$$

Where,

At is the ABCD parameters of the measured attenuators

A0 is the ABCD parameters of the Amplifier

A1 is the total ABCD parameters of the measured amplifier with the attenuators

Therefore, by using cascade theory of ABCD parameters

$$A_t A_0 = A_1 \quad (4.6)$$

Hence,

$$A_0 = A_t^{-1} A_1 \quad (4.7)$$

Where, A_t^{-1} is the inverse matrix of A_t

A comparison between the different input power level is shown in Fig 4.10. Based on the these results, it can be seen that applying input power levels lower than -10 dBm does not provide a significant impact on the amplifier's small signal performances. This may be because at -10 dBm input power, transistor still behaves as a linear device.

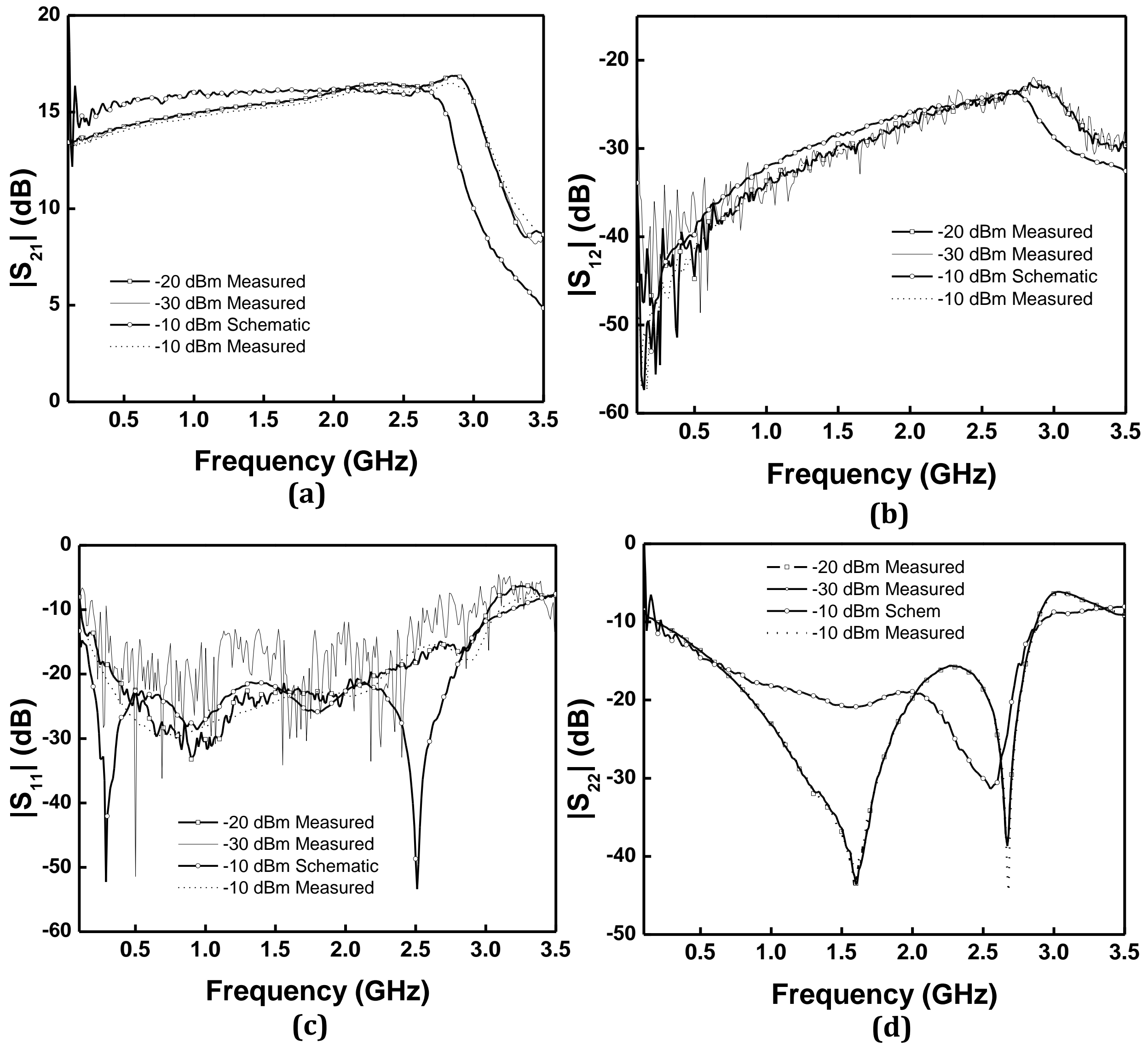

Fig. 4.10 S-parameter measurement results for different input power levels.

To further investigate the discrepancies, a new set of TRL calibration standards was fabricated with CPW grounding effect. This is because the fabricated amplifier contains grounding surrounding the transistors. The transistor was re-measured with a similar environment. Fig 4.11 shows the image of the newly fabricated TRL calibration kit. Fig 4.12 shows a comparison between the measured amplifier and the simulation results with the new transistor measurement data. It can be seen that at low frequencies the measured results are much closer to the schematic simulation with the new transistor S-parameters. However, discrepancies on input and output return loss is still needed to be investigated.

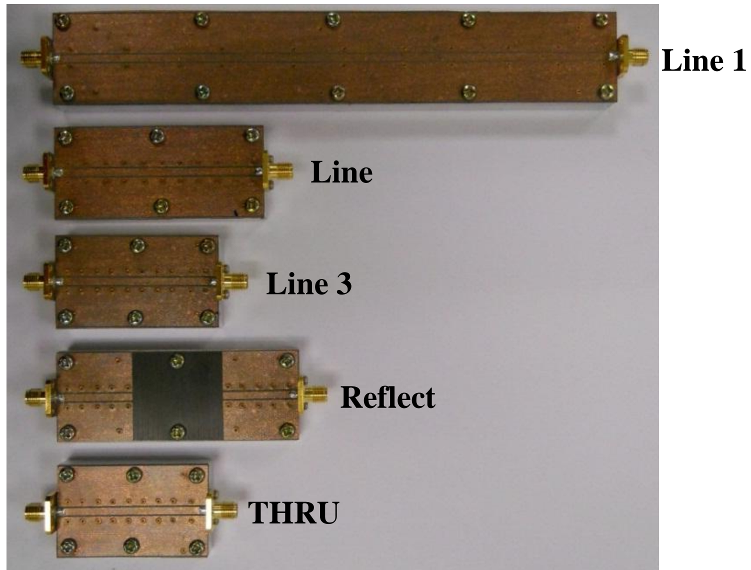

Fig. 4.11 Fabricated TRL calibration kit with CPW.

$|S_{21}|$ (dB)
20
15
10
5
0
0.5 1.0 1.5 2.0 2.5 3.0 3.5
Frequency (GHz)
Schematic with CPW FET
Measured Amplifier
AWR Axiem simulation with CPW FET
(a)

$|S_{12}|$ (dB)
-20
-30
-40
-50
-60
0.5 1.0 1.5 2.0 2.5 3.0 3.5
Frequency (GHz)
Schematic with CPW FET
Measured Amplifier
AWR Axiem simulation with CPW FET
(b

$|S_{11}|$ (dB)
0
-20
-40
-60
0.5 1.0 1.5 2.0 2.5 3.0 3.5
Frequency (GHz)
Schematic with CPW FET
Measured Amplifier
AWR Axiem simulation with CPW FET
(c)

$|S_{22}|$ (dB)
0
-10
-20
-30
-40
-50
-60
0.5 1.0 1.5 2.0 2.5 3.0 3.5
Frequency (GHz)
Schematic with CPW FET
Measured Amplifier
AWR Axiem simulation with CPW FET
(d

Fig. 4.12 S-parameter comparison between the measured amplifier and the simulations conducted using the transistor measured with the CPW calibration kit.

4.3.3 Input 1-dB Compression point of the amplifier

It was also necessary to check the input 1-dB compression point of the amplifier. As shown in Fig 4.13 the input 1-dB compression point is around -6 dBm at 2 GHz. This is mainly due to the fact that selected transistor is mostly designed for low noise amplifiers and not for power amplifiers.

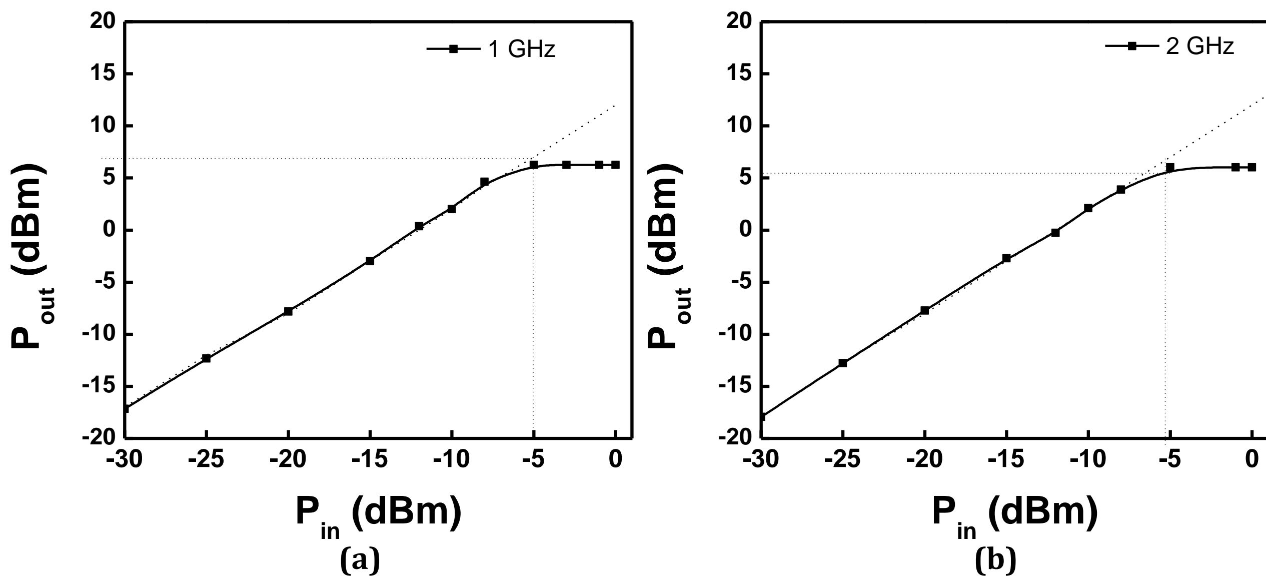

Fig. 4.13 Measured input 1dB compression point (a) 1 GHz; (b) 2 GHz.

4.4 Conclusions and Recommendations

Designing a broadband distributed amplifier is a challenging task due to the parasitics involved in the package of passive and active components. In this chapter we designed, fabricated and tested a distributed amplifier on PCB. A step by step design procedure and optimization of the amplifier is discussed. The design is based on the measurement of active and passive components done in the previous chapter. Electromagnetic simulations were done in order to check for coupling between transmission lines. The final design was fabricated and measured using an HP8510C vector network analyzer. The measured results were compared with the simulated. It was found that the first calibration done was not accurate enough and as a result discrepancies were observed between measured and

simulated results. Several investigations were performed to understand the reasons for the inconsistencies. It is found that calibration and measurement of the transistor with CPW effects included provides much closer results for the measured amplifier. However, further investigations are needed to understand the reasons for the inconsistencies between measured and simulated input and output return losses.

The first part of this thesis mainly focuses on distributed amplifiers. The principle of distributed amplifier is discussed and some of the works conducted in literature are presented. Also the influence of transistor parasitics on the distributed amplifier was discussed. TRL calibration was done to measure the active and passive components and these measured components were used to design and fabricate a distributed amplifier with a bandwidth of 3.0 GHz.

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CHAPTER 5

CMOS Active Filter Design

5.1 Introduction

The interest in developing highly integrated low cost CMOS RF transceivers has increased due to the rapid growth of wireless communications. However, designing high quality RF filters with high selectivity is crucial in RF CMOS due to the low quality factors of passive components. An alternative approach is to use active components where the gain of the active components can compensate for the losses of the passive components.

Several filter topologies have been published in the literature employing active components. One such approach is to use transistors as active inductors [11]-[14] which helps to obtain high Q inductors and to reduce the overall chip area.

In [12], an active inductor with a self-resonance frequency of 5.7 GHz is presented. A measured quality factor of 665 is achieved and a high Q band-pass filter using this inductor was also presented. In [13] a 6th order RF band-pass filter from 2.05-2.45 GHz was presented using high Q CMOS active inductors. However, band-pass filters realized using active elements suffer from high noise figure and poor linearity [14].

Using active-g_m-RC circuits in filter design is also a well-researched area and several papers have been published recently [66-69]. However, the bandwidth of these types of topologies is limited to several MegaHertz and, therefore, are not suitable for microwave frequencies.

In [16], Rauscher proposed an ingenious method to realize broadband active filters using transversal and recursive filtering concepts. This topology was first implemented in a GaAs MMIC and it has rarely been reported for a CMOS process. In this chapter we focuses on designing a lumped and transversal filter using Global Foundries standard 0.13-µm CMOS process. The pass-band of the designed filter was from 2.0 – 4.0 GHz.

5.2 Microwave transversal Filtering

Transversal filtering has been commonly used in discrete time applications [16] and it consists of tapped delay lines with constant delay increments as well as amplitude weighting elements as illustrated in Fig 5.1.

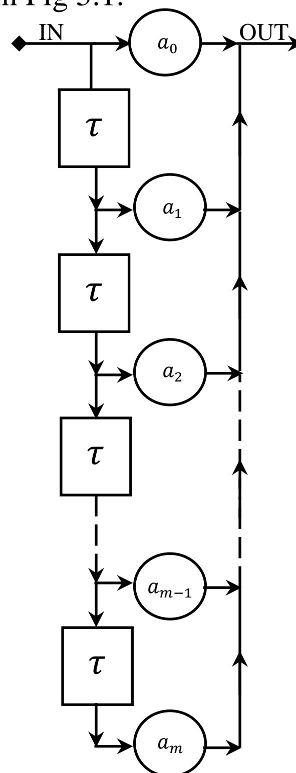

Fig. 5.1 Digital transversal filtering.

The coefficients α_m represent the amplitude weighting factors and τ represents constant time delay intervals.

When realizing it physically in the microwave domain, uniform transmission elements can be used to provide the necessary constant time delays and active devices can be used to provide the necessary gain. Fig 5.2 illustrates a typical microwave transversal filter diagram. In this figure $A_1 - A_N$ represent the amplitude elements which provide necessary gain and which are combined 180° out of phase. 90° degree lines provide the necessary phase delay.

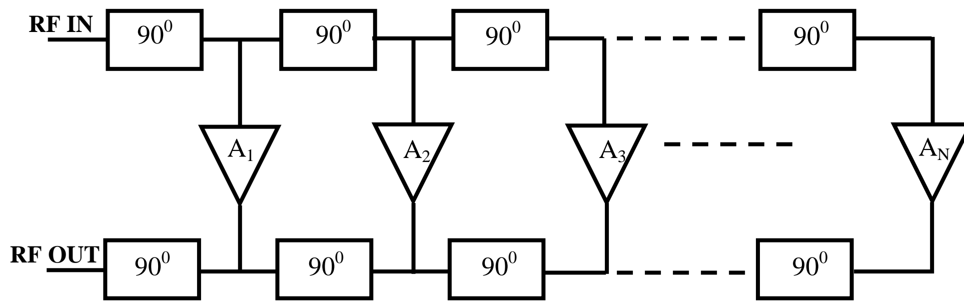

Fig. 5.2 Typical microwave transversal filter structure.

Depending on the frequency, the output signal of the transversal elements is added constructively or destructively. Schindler et al. [17] proposed another method where they utilized lumped elements to obtain band pass characteristics and transversal elements to obtain the necessary gain as illustrated in Fig 5.3. In this approach, conventional low pass filters were used at the input followed by a gain element and a high pass filter structure.

Schindler et al. also showed that a low pass single section has a phase delay which is given by

$$\theta_{lp} = \sin^{-1}\left(\omega\sqrt{LC}\right) \quad (5.1)$$

And for a highpass single section phase delay is given by

$$\theta_{hp} = -\sin^{-1}\left(\frac{1}{\omega\sqrt{LC}}\right) \quad (5.2)$$

Where, L and C are the inductor and capacitor values for a low pass section or for a high pass section. Based on these formulations it has been shown that a low pass section has a 90^0 phase delay whereas a high pass section has a 90^0 phase advance.

The filtering process of this circuit is done by combining the phase delays of both the high pass and low pass sections.

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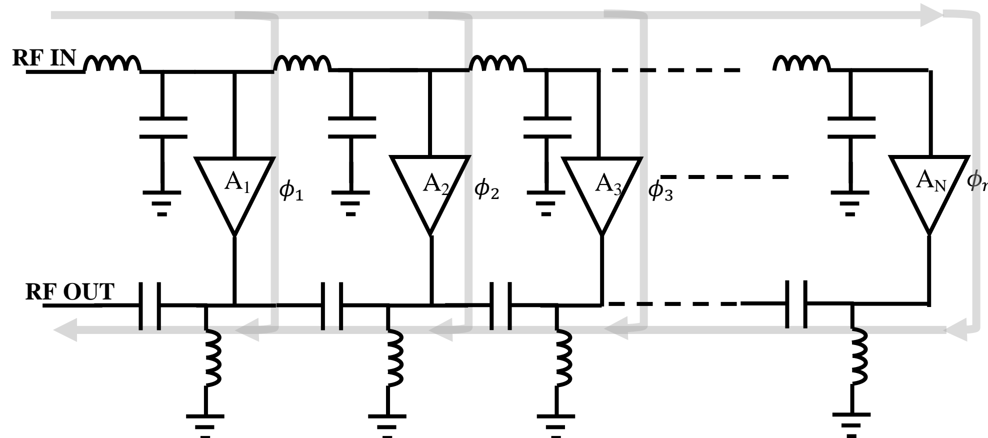


Fig. 5.3 Microwave lumped and transversal element filter topology.

As illustrated in Fig 5.3 the main signal path travels through the last gain element A_N. Each gain element has an insertion phase of ϕ_x and when there is a difference of 180^0 between ϕ_x and ϕ_n an amplitude reduction is possible and this happens mainly when it approaches the cutoff. The low pass and high pass filters are terminated by 50 Ohms resistors to ensure they are properly matched.

The first GaAs MMIC implementation was published by Schindler et al. where they obtained a passband of 9.8 – 11.1 GHz with 2 dB loss. A rejection of 30 dB was achieved at 1.1 GHz. Another GaAs circuit was published by Tam et .al [70], where they incorporated tuned amplifiers as transversal elements. The tuning is accomplished by inserting a resonant circuit at the final stage of the filter. In [71], an L band filter was designed in a 0.8 µm BiCMOS process. A 3 dB bandwidth of 6% at a centre frequency of 1.7 GHz is achieved with a side band rejection of 24 dB at 1.4 GHz and 2.0 GHz.

5.3 Design of a CMOS lumped and transversal element filter

5.3.1 Filter Schematic Design

Design specifications:

Supply Voltage	1.2 V
Filter Centre Frequency (f_c)	3.0 GHz
3-dB bandwidth	2.0 GHz
Insertion Loss	< 3 dB
Ripple within BW (-3dB)	0.5 dB
-55 dB frequency (below f_c)	1.5 GHz
-60 dB frequency (above f_c)	5.0 GHz
Input Return Loss	> 20 dB
Output Return Loss	> 10 dB
Isolation	30 dB
Size	< 4 mm^2

Table 5.1: Active filter specifications

To design a lumped and transversal element filter, first a low pass filter and a high pass filter is designed to obtain a pass band of 2.0 – 4.0 GHz. The low pass filter is designed at a cutoff frequency of 4.0 GHz and the high pass filter is designed at a cutoff frequency of 2.0 GHz. For an 8th order Chebyshev filter with a 0.5 dB ripple and cutoff frequency 1, the prototype low pass element values are given by [72]:

g_1	g_2	g_3	g_4	g_5	g_6	g_7	g_8	g_9
1.7451	1.2647	2.6564	1.3590	2.6564	1.3389	2.5093	0.8796	1.9841

Table 5.2: 8th Order Chebyshev filter element values

The low pass inductor L and capacitor C values are calculated using [73]:

$$L_{lp} = \left(\frac{\Omega_c}{\omega_c}\right)\gamma_0 g \tag{5.3}$$

And

$$C_{lp} = \left(\frac{\Omega_c}{\omega_c}\right)\frac{g}{\gamma_0} \tag{5.4}$$

The *L* and *C* values of the high pass filter are obtained by using the high pass transformation and are given by

$$C_{hp} = \left(\frac{1}{\omega_c \Omega_c}\right) \frac{1}{\gamma_0 g} \tag{5.5}$$

And

$$L_{hp} = \left(\frac{1}{\omega_c \Omega_c}\right) \frac{\gamma_0}{g} \tag{5.6}$$

Where,

Ω_c = 1.0 rad/s

ω_c = Cutoff frequency

γ_0 = Impedance scaling factor 50 Ω

Fig 5.4 shows the low pass and high pass filter circuits and Table 5.1 shows the calculated capacitor and inductor values.

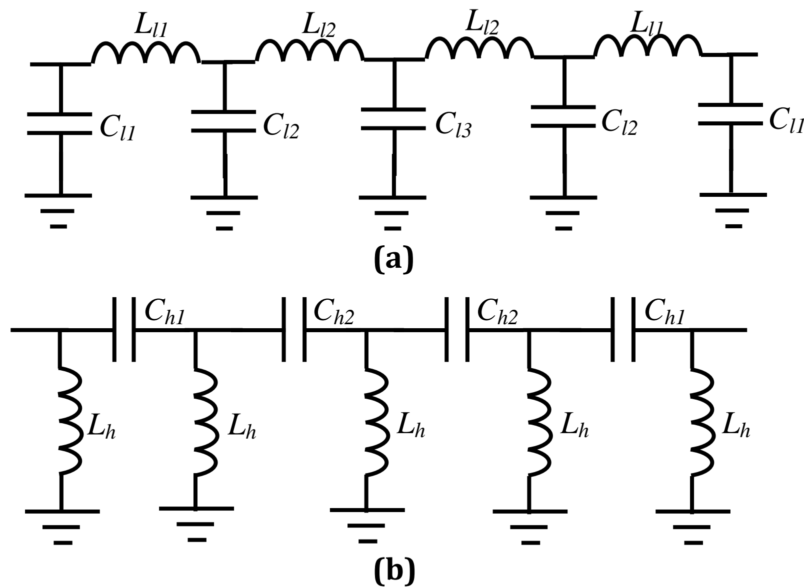


Fig. 5.4 (a) Low pass filter; (b) High pass filter

Low pass	L_{l1} = 2.52 nH	L_{l2} = 2.72 nH	C_{l1} = 1.39 pF	C_{l2} = 2.12 pF	C_{l3} = 2.16 pF
High pass	C_{h1} = 1.25 pF	C_{h2} = 1.16 pF	L_{h1} = 2.27 nH	L_{h2} = 1.46 nH	L_{h3} = 1.49 nH

Table 5.3: Low pass and high pass element values

The next step is to combine the two filter sections and include the transistors. The design is done in Cadence. Three transistors are used to obtain the necessary gain. A better rejection is achieved when the transistor at the last section is removed and the low pass section is directly connected to the high pass section. Since the foundry only provides a limited number of inductors, the calculated values were optimized for the available inductor values. The transistor dimensions were carefully selected to maintain the desired bandwidth and at the same time to obtain good return loss and good rejection. Since the inductors for the RF choke occupies a significant amount of chip area the drain biasing were implemented through the shunt inductors of the high pass filter and the shunt inductors were grounded through 10 pF capacitors. The drains were individually biased because during measurement each biasing was controlled individually. The gates were biased through 5 kOhm resistors connected to the low pass filter. It is also possible to control the gain of the filter through the gate biasing during the measurements.

5.3.2 Schematic Simulation Results

The simulated S-parameters of the filter are shown in Fig 5.5. The results are illustrated for different gate biasing values. As shown in the simulated results, the filter has a pass band from 2.0 – 4.0 GHz with a gain of 8 dB and a good rejection of -50 dB and -60 dB at 1.5 GHz and 5.2 GHz when it is biased at V_g = 1.0 V and V_d = 1.0 V. The K - Δ test was performed to check the stability of the filter and it is shown in Fig 5.5 (e-f). It can be seen that within the frequency range 0-10 GHz the filter is unconditionally stable.

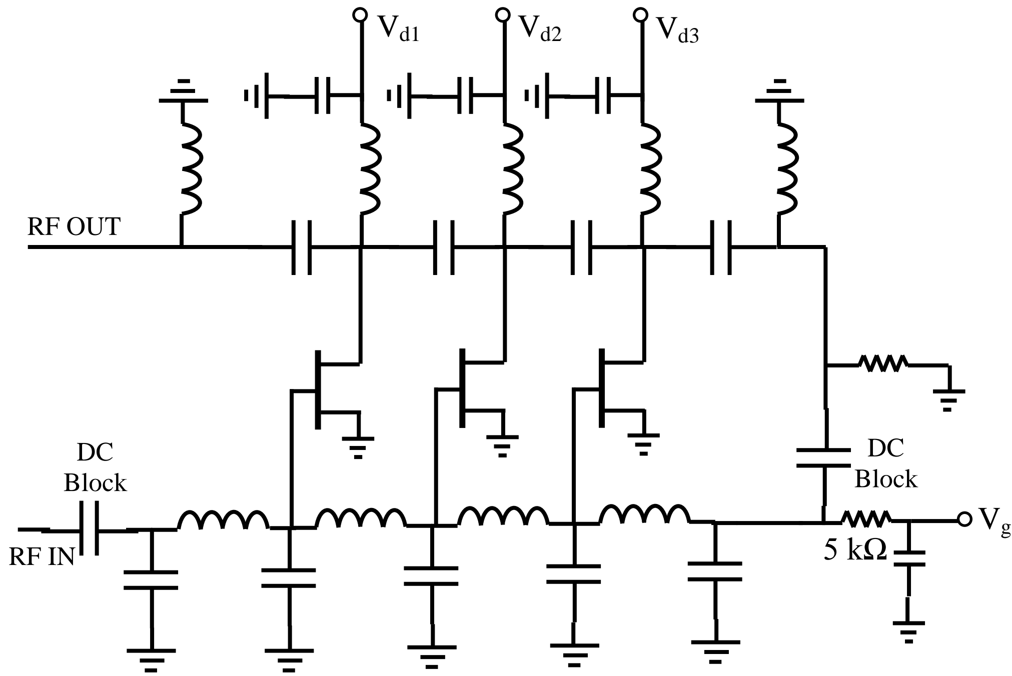
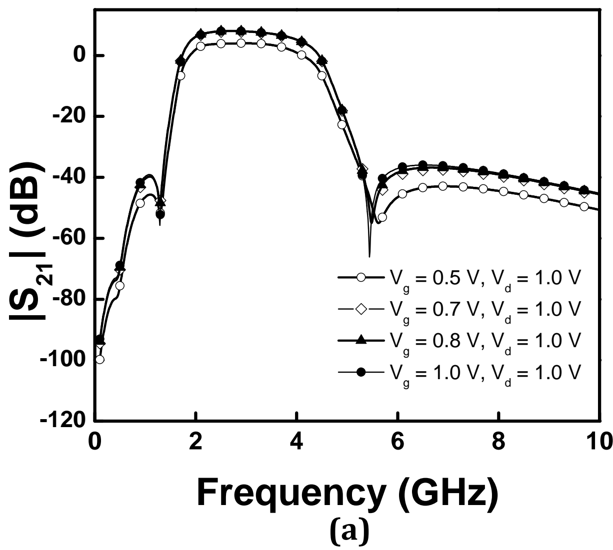
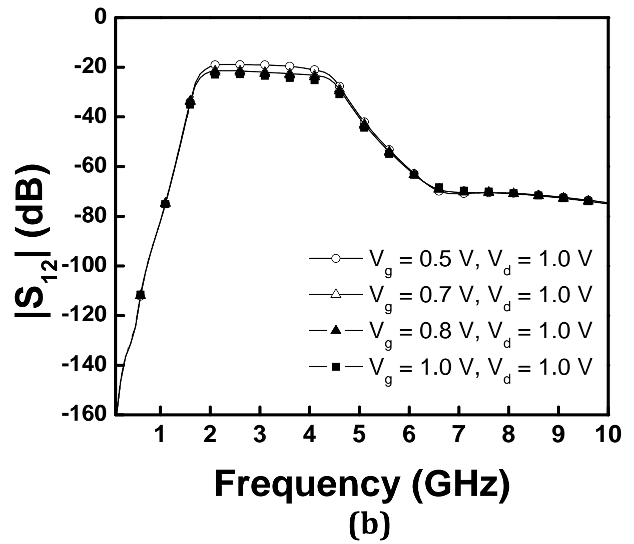


Fig. 5.5 Schematic diagram of the designed filter.



(a)



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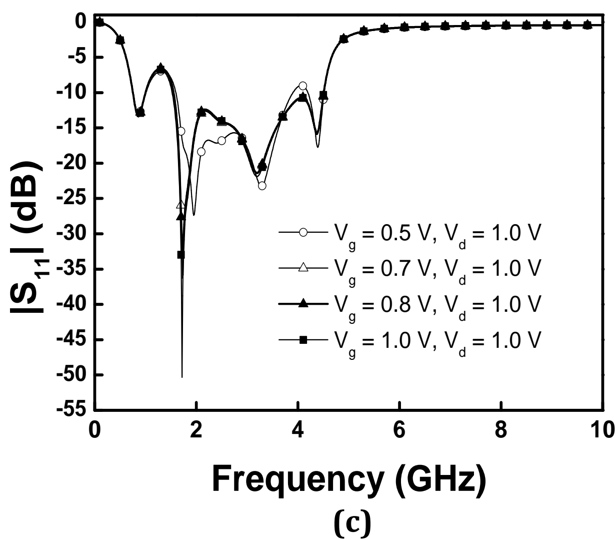

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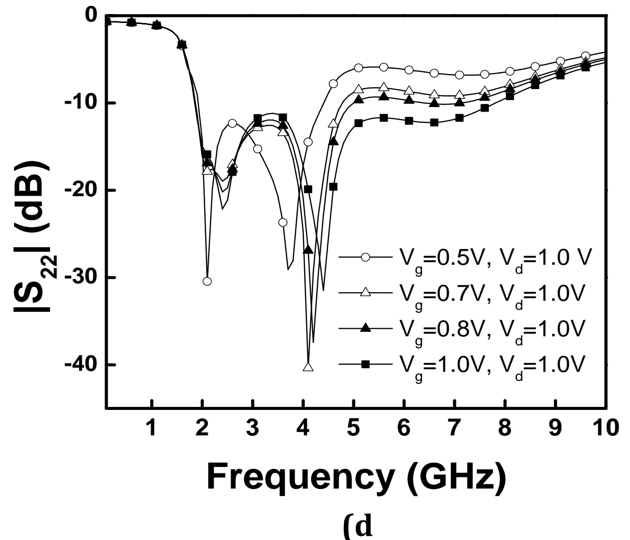

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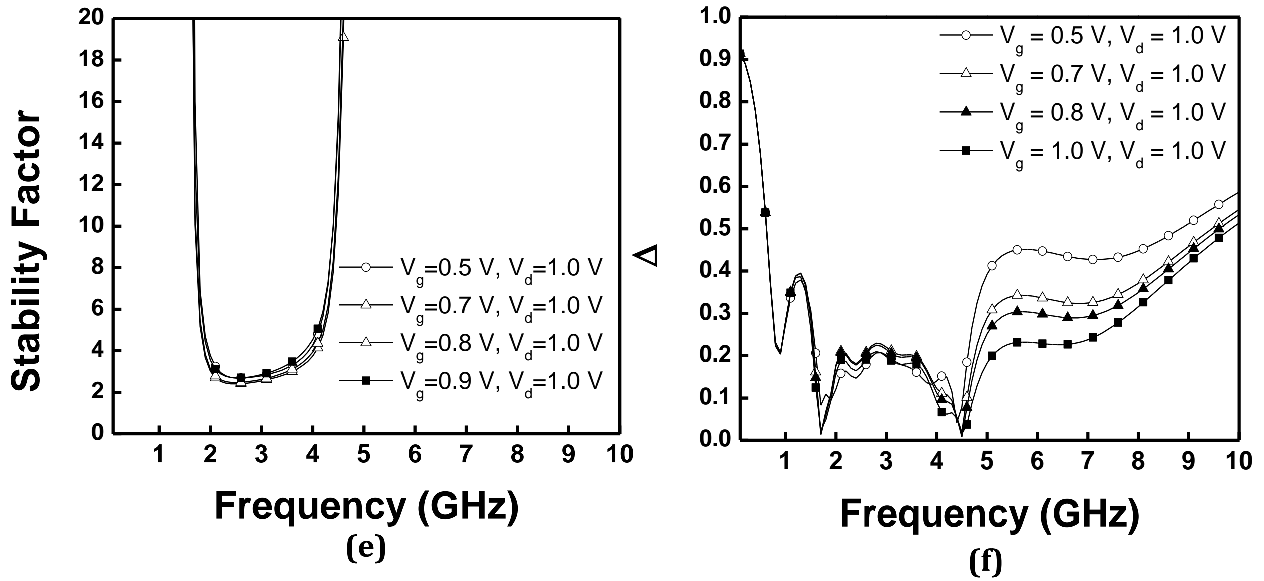


Fig. 5.6 Simulation results (a) $|S_{21}|$ (dB); (b) $|S_{12}|$ (dB); (c) $|S_{11}|$ (dB); (d) $|S_{22}|$ (dB); (e) Stability factor K; (f) Delta factor.

5.3.3 Gain Compression of the Filter

Since active elements are incorporated in the design, it is necessary to simulate the gain compression of the filter. Fig 5.7 illustrates the simulated gain compression and the input P1dB of the filter at 3.0 GHz. Based on the simulation, the input P1dB comes to around 1.7 dBm.

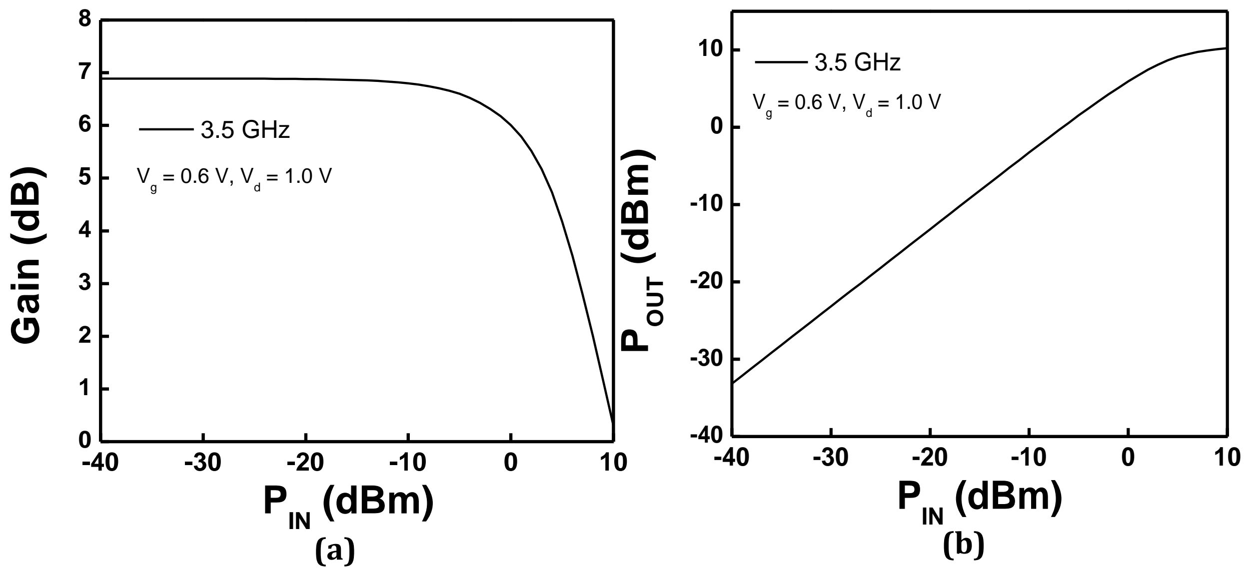


Fig. 5.7 (a) Gain VS input power; (b) Output power VS Input power.

5.3.4 Monte-Carlo Simulation Results

It is important to consider the manufacturing process variations during the design. For example, it is possible for transistor parameters to vary from die to die [74]. Such variations may produce faulty chips, which reduce the yield of the device. Monte-Carlo simulations are capable of predicting IC yield due to manufacturing process variations. Fig 5.8 shows the simulated S-parameters obtained using Monte-Carlo simulation.

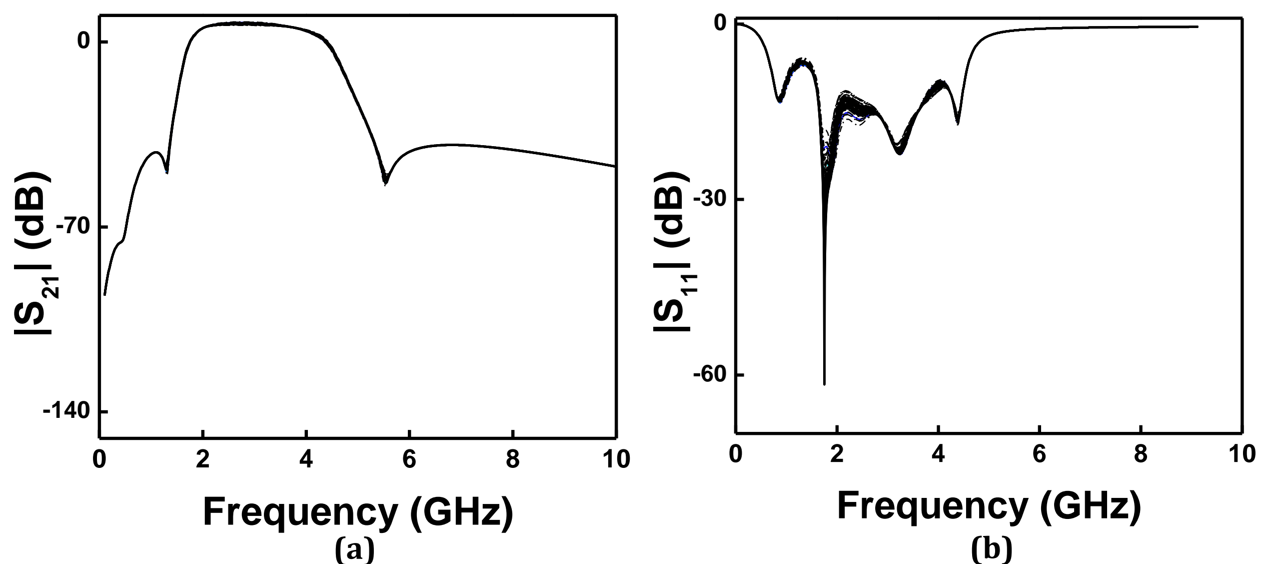


Fig. 5.8 Monte Carlo simulation (a) $|S_{21}|$ (dB); (b) $|S_{11}|$ (dB).

5.4 Layout Design and Post Layout Simulation Results

5.4.1 Standard 0.13 μm CMOS process

The filter design was based on the Global Foundries 0.13 μm CMOS process. Fig 5.9 shows the layer stack of the process with eight metallizations. Top metal (MT) has a thickness of 3.0 μm. Metal layers from M2 – M7 has a thickness of 0.42 μm while the bottom most layer has a thickness of 0.31 μm. The distance between MT and M7 is 0.6 μm and the distance between adjacent metallization from M1 – M7 is 0.42 μm. Total thickness of SiO_2 is 8.95 μm and the thickness of silicon substrate is about 480 μm.

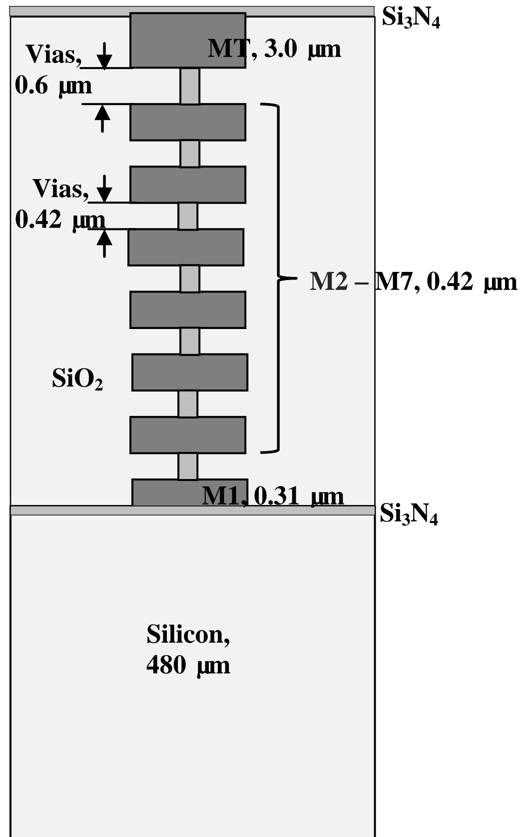


Fig. 5.9 CMOS 0.13-um layer configuration

In order to verify the inductor models given by the foundry, the Sonnet EM electromagnetic simulator was used to simulate and compare with foundry model provided. Based on the simulations it can be seen that by placing a ground plane directly below the inductors causes a reduction of Q-factor of the inductor and it also changes the actual inductance value. Hence, grounding was not used below the inductor in the actual filter layout design. This was also verified by fabricating and measuring several inductor test structures. Fig 5.10 shows a comparison between measured and simulated inductor test structures. Open and short structures were used to de-embed the pads of the inductors [75] as illustrated in Fig 5.11.

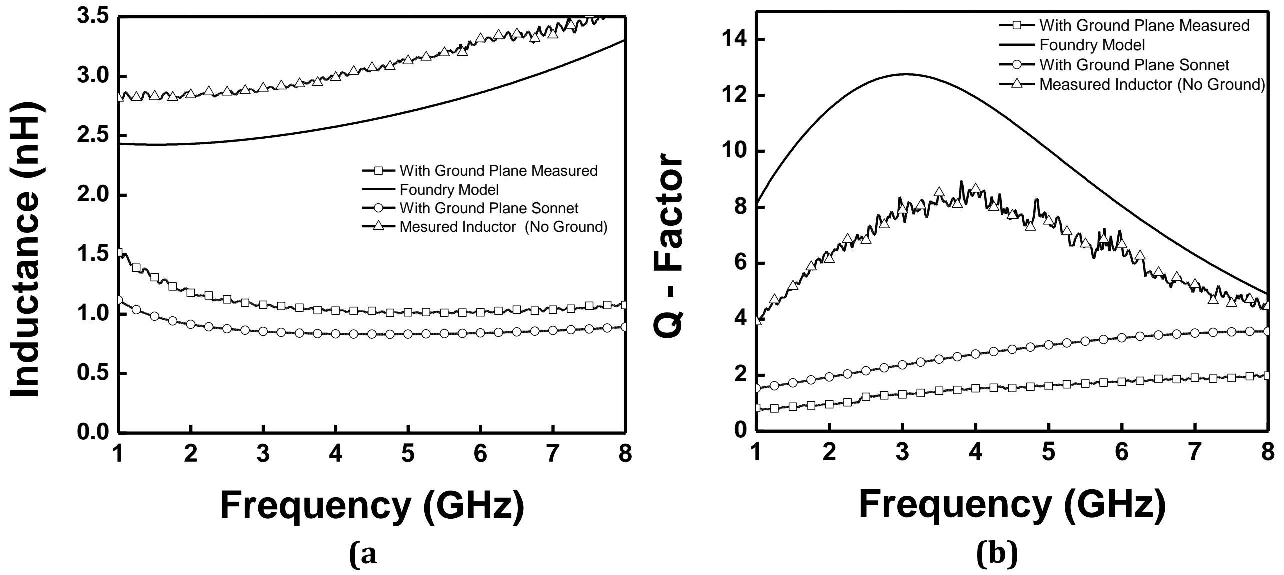


Fig. 5.10 Effect of ground plane on (a) Inductance; (b) Q factor.

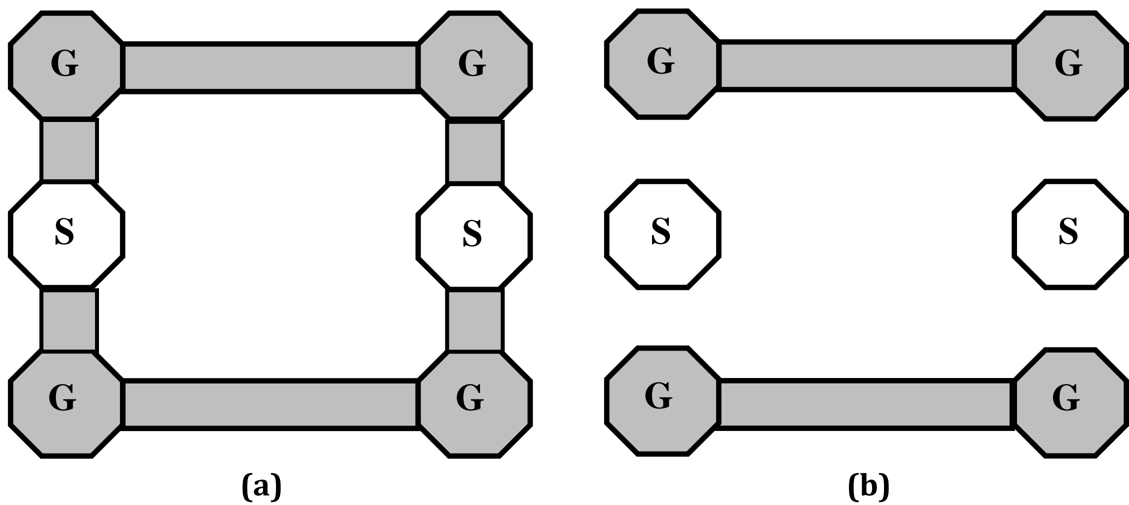


Fig. 5.11 Pad de-embedding (a) Short; (b) Open.

As illustrated in Fig 5.10 it can be concluded that using a ground plane below the inductor reduces the Q factor of the inductor.

Based on the foundry design rules it is also recommended to not use line widths larger than 12 μm. This is to prevent dishing during the manufacturing process which reduces the planarity of the metal lines. Therefore, slots have to be used if widths greater than 12 μm are required. Since the ground plane occupies a larger area slotting was done to prevent dishing. Also diodes were used to avoid any Antenna violation rules.

5.4.2 Layout Design

Fig 5.12 shows the layout view of the designed active filter. The entire chip with pads occupies an area of 1x2 mm^2.

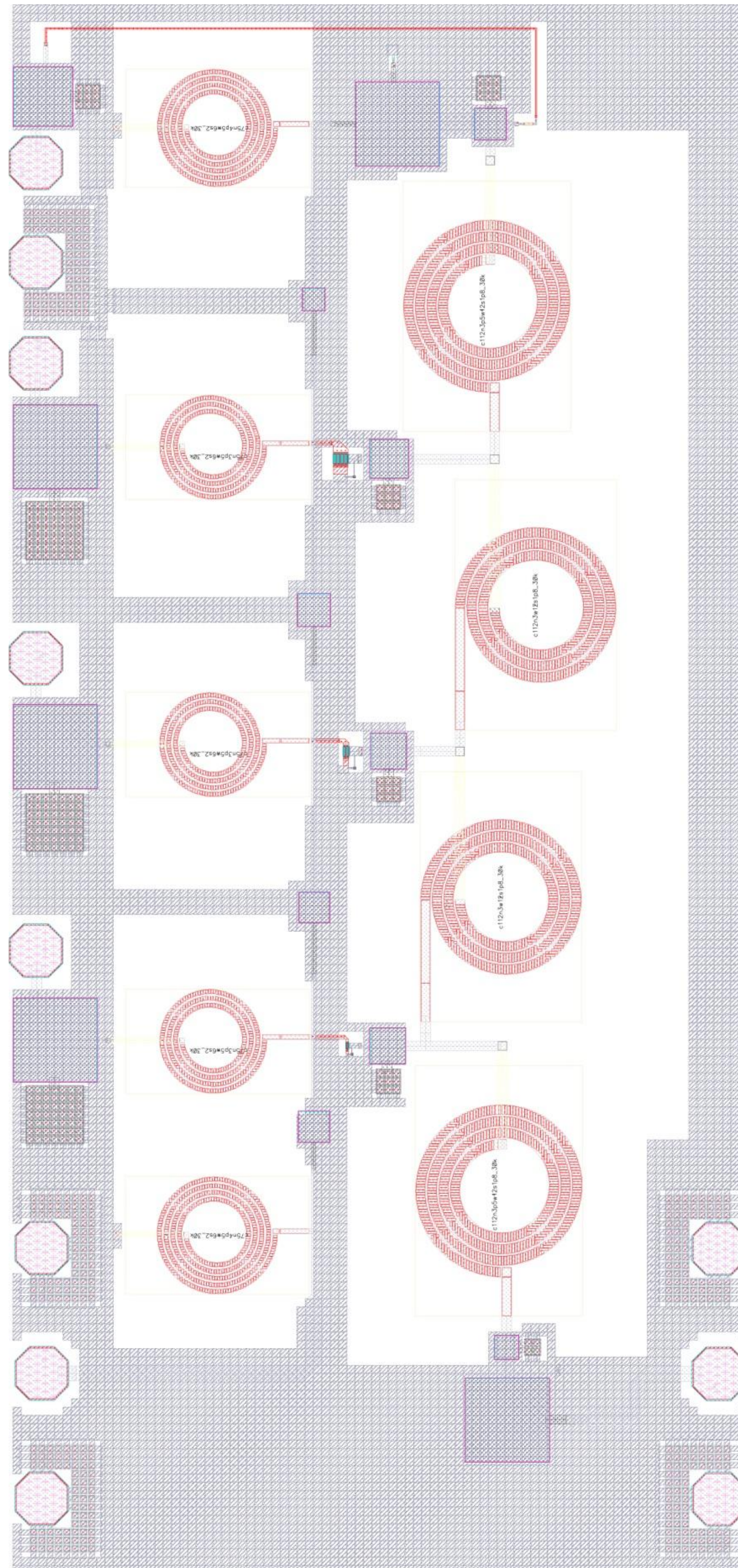


Fig. 5.12 Layout of the designed filter

5.4.3 Post Layout Simulation

Post layout simulation is performed using Cadence calibre parasitic extraction simulator. Fig 5.13 illustrates a comparison between schematic and post layout simulation. It can be seen that there is a slight reduction in insertion loss.

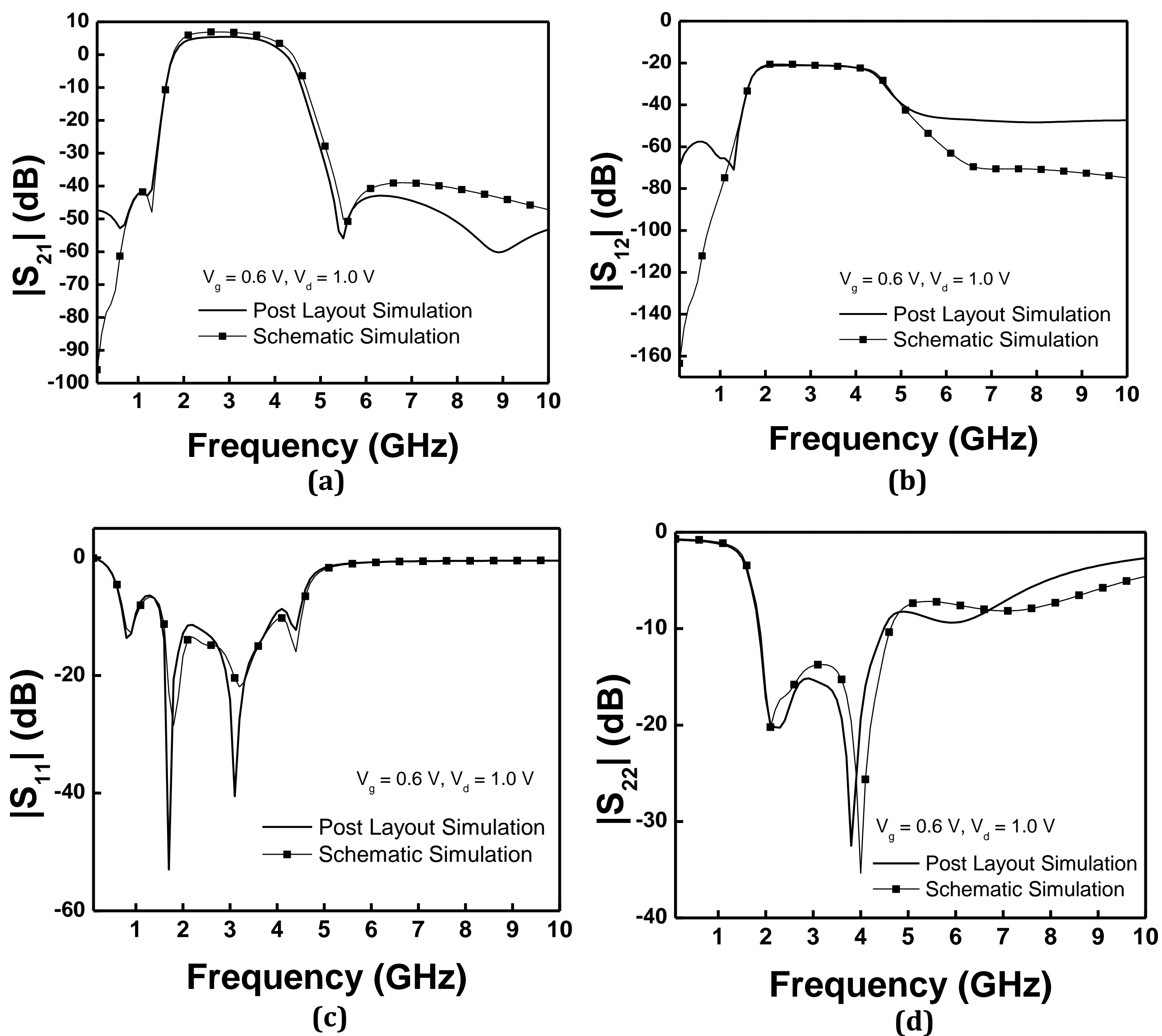


Fig. 5.13 Schematic simulation VS post layout simulation (a) $|S_{21}|$ (dB); (b) $|S_{12}|$ (dB); (c) $|S_{11}|$ (dB); (d) $|S_{22}|$ (dB).

5.5 Measurement Results

The designed chip is manufactured using Global Foundries 0.13-µm CMOS process as shown in Fig. 5.14.

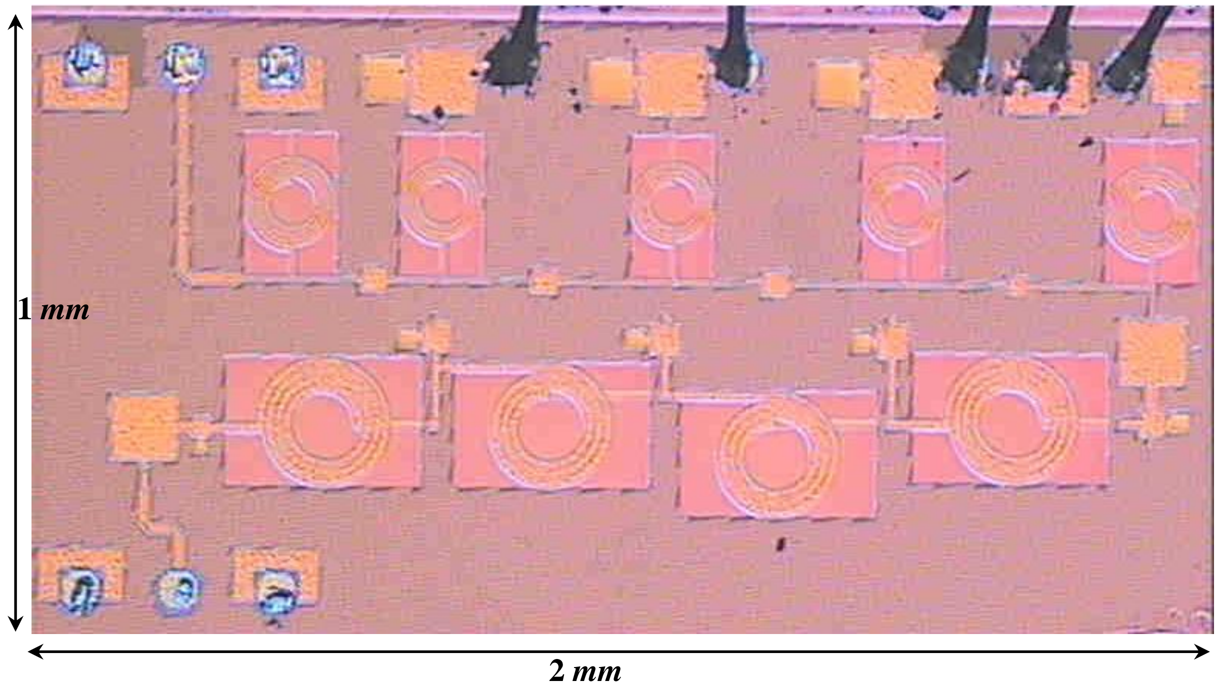
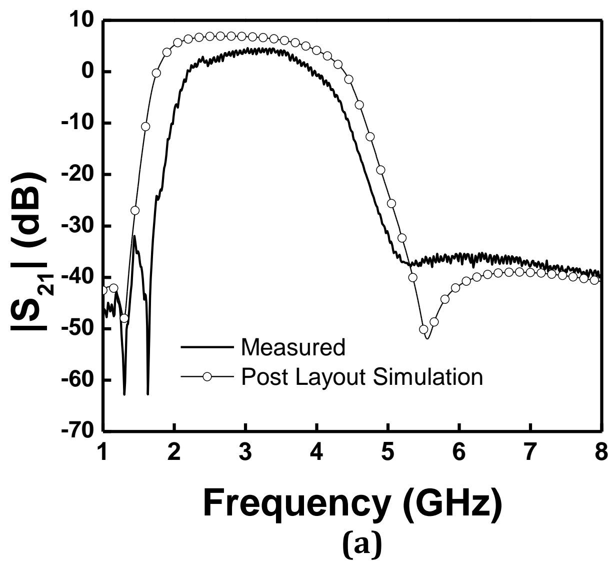
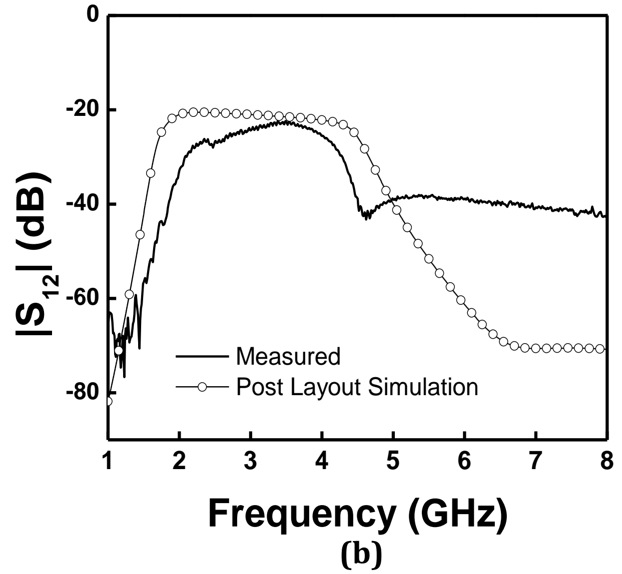


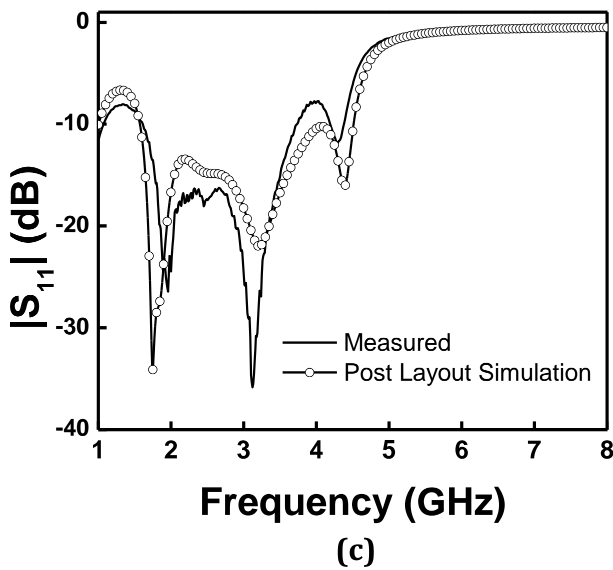
Fig. 5.14 Fabricated filter.

Gold bonding is used to provide DC biasing and the measurements are performed using Agilent HP 8510C VNA and the Cascade Microtech GSG probes. Measured filter S-parameter results are shown in following figures.

Measured First IC







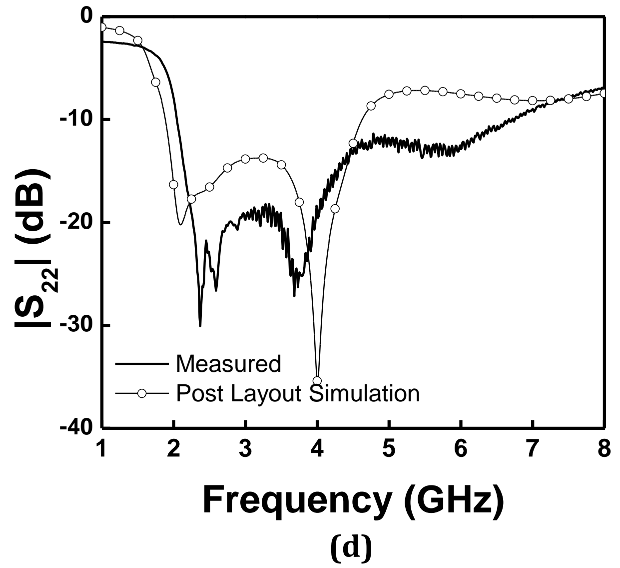


Fig. 5.15 Measured first IC (a) $|S_{11}|$ (dB) (b) $|S_{12}|$ (dB) (c) $|S_{11}|$ (dB) (d) $|S_{22}|$ (dB).

Measured Second IC

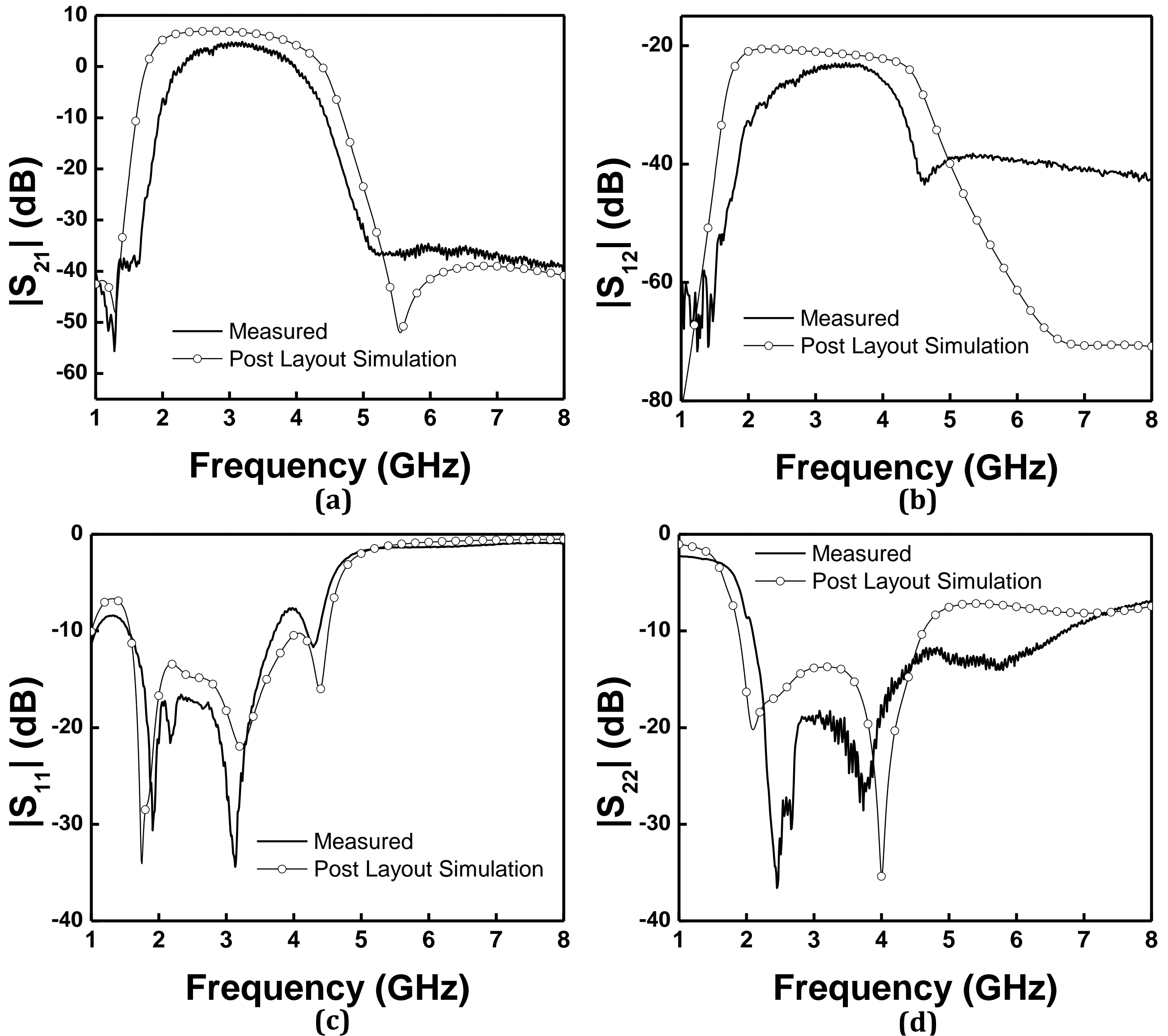


Fig. 5.16 Measured second IC.

Based on the above measurement results it can be seen that input return loss, output return loss and isolation results are comparable with the simulated results. However, there is a discrepancy between measured and simulated in the insertion loss of the filter. As can be seen from the graphs, there is a reduction in gain in about 2 dB. This may be due to the inaccuracies of the models provided by the foundry. The low rejection near the cut off at 5 GHz is may be due to the additional parasitic inductances introduced by the connections in the circuit. Such parasitics were not included in the post layout simulation. Also it can be seen that there is a reduction in the bandwidth in the measured. This may be due to the

additional inductance introduced by the bond wires. As explained before, the drain biasing for the transistors were done through the inductance of the high pass filter structure which was connected to the ground through a bypass capacitor. In this circuit, a bypass capacitance of 10 pF was used. However, this capacitance may not be enough and hence the additional inductance introduced by the bond wires may have altered the passband characteristics. To improve the performances it is necessary to include these bonding effects in the simulations. Also increasing the bypass capacitance value also can help to improve the performances.

Measured Large Signal Performance

Following figure shows the 1 dB compression point of the measured filter.

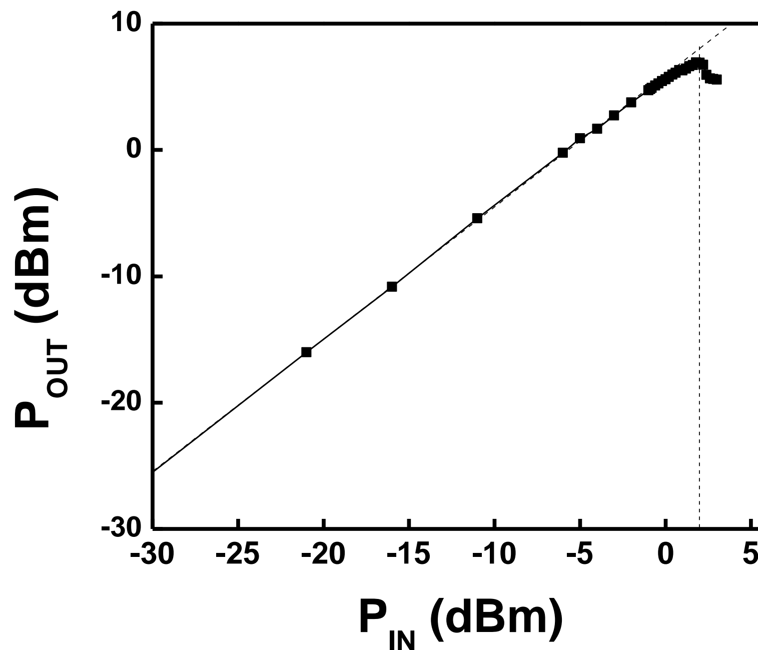


Fig. 5.17 Measured input 1 dB compression point.

Based on the above graph it can be seen that the input 1 dB compression is closed to the simulated and it is around 1.8 dBm.

5.6 Conclusions

This chapter introduced the concept of transversal filtering and demonstrated designing of a lumped and transversal element filter. The filter was successfully fabricated and measured in CMOS 0.13 μm process. Measurement results are comparable with the simulated and some discrepancies are observed due to the additional parasitic inductances introduced by the bonding wires. To overcome such discrepancies it is necessary to include such bonding effects in the simulation as well. Based on the measured results it is evident that the input 1 dB compression is around 1.8 dBm. Hence further research needs to be done in order to improve the large signal performance of the amplifier. This type of topology can be used in millimeter wave filter design as well. Hence, research can be further extend to design active filters at millimeter wave frequency range.

CHAPTER 6

Microwave CMOS Passive Filter Design

6.1 Introduction

Some of the general trends in the short range communication systems in microwave and millimeter wave regions, such as 24 – 29 GHz and 60 – 77 GHz, bands are increasing data rates of 100 Mbit/s to 1 Gbit/s, and low power consumptions [76]. In a millimeter wave transceiver system, passive filters are mostly used for interference rejection. At millimeter wave frequencies such as 60 – 77 GHz, it is more desirable to use distributed elements rather than LC lumped elements to design filters. Usually lumped element filters are small in size. However, elements such as inductors and capacitors have low Q-factors and hence are not preferred to be used at higher frequencies. In contrast, using distributed elements such as transmission lines are much preferred due to the accurate models available, straight forward designs and easy layout [77]. However, filters based on both lumped and distributed elements are available in literature.

6.2 CMOS Lumped Element Filter Design

Several papers have been published related to CMOS lumped element filter design [78]-[81]. In [78], Chiang et al. presented a Ku band pass filter in 0.18 μm CMOS process. The filter structure was based on a π network coupling structure to construct the desired coupling. They were able to achieve a 3 dB bandwidth of 15 % at a centre frequency of 17 GHz with an insertion loss of 3.2 dB. Another lumped element filter was reported in SiGe technology for automotive radar systems at 77 GHz by Dehlink et al. [79]. The filter prototype is based on Butterworth characteristics and achieves a 3 dB bandwidth of 15.5% with a minimum insertion loss 6.4 dB. It occupies a small chip area of 110x60 μm^2. Recently a K – band bandpass filter was reported in IBM 90 nm CMOS process [81]. The design is based on Chebyshev characteristics and has an insertion loss of 5 dB at 20 GHz and a 3 dB bandwidth of 20 %. The total size of the filter was 700x450 μm^2.

This chapter has addresses the design of a LC lumped passive filter at centre frequency 27.5 GHz. Since models for the transistors are not available at this frequency range a passive filter topology is chosen. Element values were based on inverse Chebyshev prototype characteristics. Its properties are inverse of a Chebyshev filter and it has a better pass band over the equal-ripple approximation [82]. It was also possible to obtain smaller values for the inductors and capacitors using this method which is presented later in this chapter. This is an advantage in high frequency design since a better Q factor can be obtained using smaller inductors and capacitors.

The designed filter has a bandwidth of 2.0 GHz at a centre frequency of 27.5 GHz with a good out of band rejection and a 3 dB bandwidth of 7 %. The design specs are shown below. Simple transmission lines were used to design inductors and MIM capacitors were modeled in Sonnet Electromagnetic simulator to obtain the desired capacitance values.

Design specifications:

Requirement	Value
Input Return Loss	15 dB
Output Return Loss	15 dB
Pass band Frequency	27-28 GHz
Pass Band Loss	< 3 dB
Pass Band Ripple	< 2 dB
Low side at 25.75 GHz	> 35 dB
High Side at 29.25 GHz	> 35 dB

Table 6.1: Passive filter design specifications

6.3 Filter Design

6.3.1 Calculation of Filter Element Values

The prototype element values were obtained using the tables provided in [82] for inverse-Chebyshev low-pass realizations. For a 3rd order filter with attenuation 20 dB, low-pass element values were given by: C_1 = 1.17172, L_2 = 2.34344, C_2 = 0.32004, C_3 = 1.17172. Network configuration for this topology is shown in Fig 6.1.

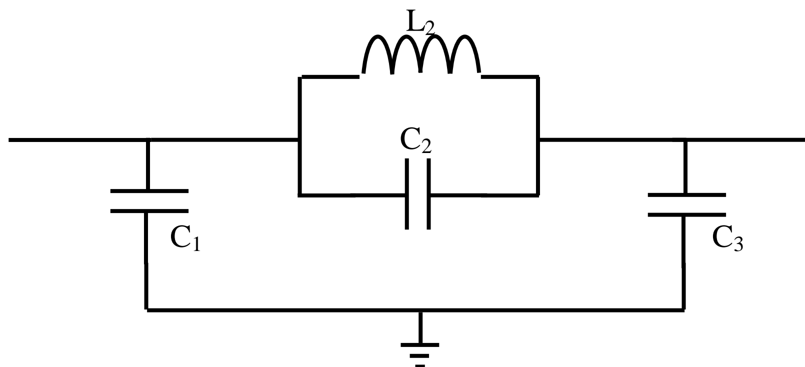


Fig. 6.1 Low pass inverse Chebyshev filter structure.

The next step was to transform the low-pass filter structure into a band-pass filter structure. Based on transformation theory, an inductor can be transformed in to a series LC and a capacitor can be transformed in to a parallel LC as illustrated in Fig 6.2.

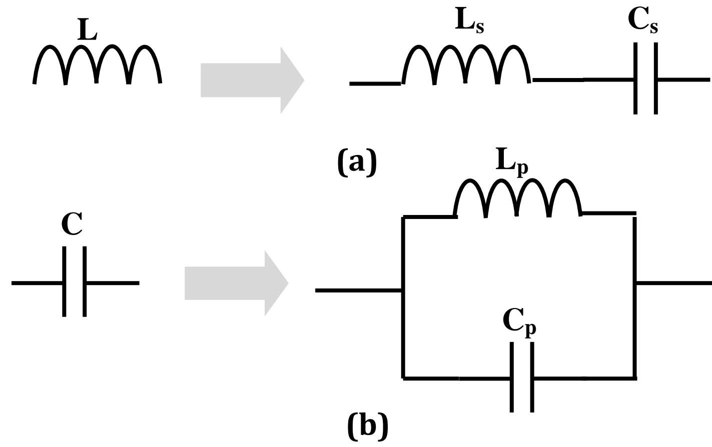


Fig. 6.2 Low pass to band pass conversion.

For g representing an inductance element values can be calculated as:

$$L_s = \left(\frac{\Omega_c}{FBW\omega_0}\right)\gamma_0 g \tag{6.1}$$

$$C_s = \left(\frac{FBW}{\omega_0\Omega_c}\right)\frac{1}{\gamma_0 g} \tag{6.2}$$

For g representing capacitance element values can be calculated as:

$$C_p = \left(\frac{\Omega_c}{FBW\omega_0}\right)\frac{g}{\gamma_0} \tag{6.3}$$

$$L_p = \left(\frac{FBW}{\omega_0\Omega_c}\right)\frac{\gamma_0}{g} \tag{6.4}$$

Where, FBW is the fractional bandwidth which is given by:

$$FBW = \frac{\omega_2 - \omega_1}{\omega_0} \tag{6.5}$$

$$\omega_0 = \sqrt{\omega_1\omega_2} \tag{6.6}$$

$\Omega_c = 1.0$ rad/s

γ_0 = Impedance scaling factor 50 Ω

Based on the above equations, element values for the band pass filter for the network configuration shown in Fig 6.3 are given by:

L'_0	C'_0	L'_1	C'_1	C'_2	L'_2
38.19 pH	877.67 fF	4.39 nH	7.63 fF	239.72 fF	139.82 pH

Table 6.2: Element values for the band pass filter structure

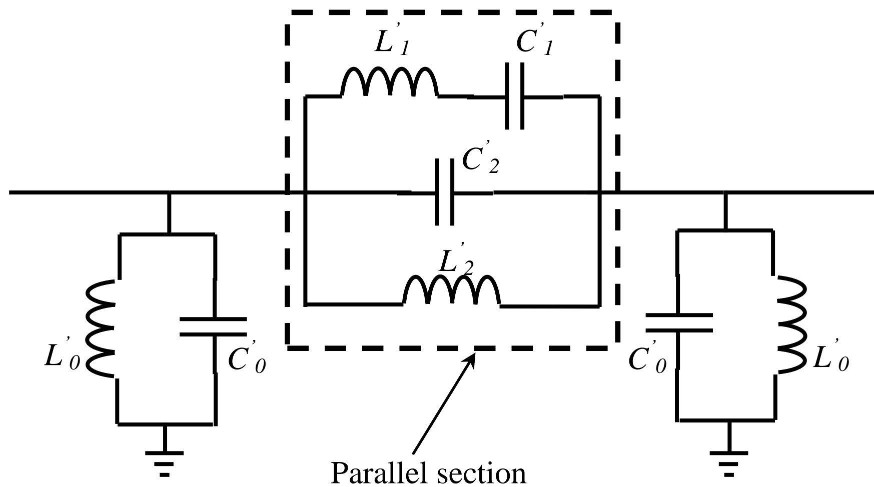


Fig. 6.3 Band pass filter structure.

The inductance of 4.39 nH is difficult to implement with a good Q factor at microwave frequencies. In addition, models provided by the foundry for the capacitance are not accurate enough for smaller capacitance values of about 7 fF due to the fringing capacitance. The network configuration illustrated in Fig 6.3 was further simplified by simplifying the parallel section into two series parallel sections as illustrated in Fig 6.4.

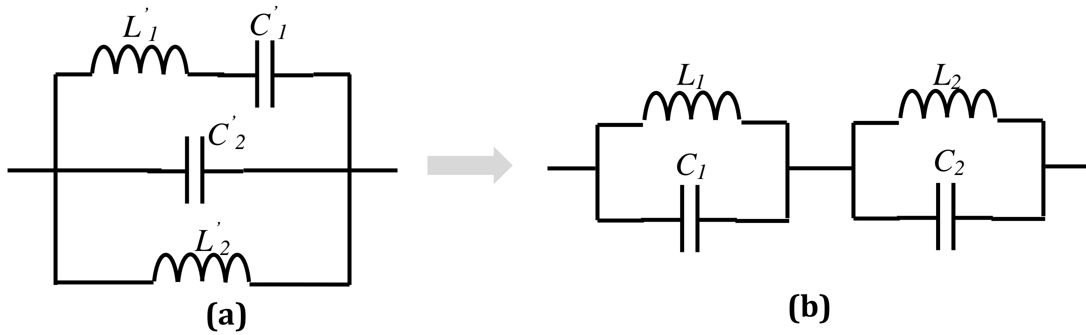


Fig. 6.4 Conversion of parallel section in to two series parallel sections.

For the parallel section shown in Fig 6.4 (a), the total impedance can be calculated as:

$$Z_1 = \frac{j\omega L_2'\{1-\omega^2 L_1' C_1'\}}{(1-\omega^2 L_1' C_1')(1-\omega^2 L_2' C_2') - \omega^2 L_2' C_1'} \tag{6.7}$$

And for the configuration shown in Fig 6.4 (b), the total impedance can be calculated as:

$$Z_2 = \frac{j\omega\{L_1(1-\omega^2 L_2 C_2) + L_2(1-\omega^2 L_1 C_1)\}}{(1-\omega^2 L_1 C_1)(1-\omega^2 L_2 C_2)} \tag{6.8}$$

Since the LC values in (6.7) are known, (6.8) and (6.7) equated to obtain the LC values of the new network configuration. Final calculated values are tabulated in Table 6.2.:

L_1	C_1	L_2	C_2
76.03 pH	526.52 fF	63.53 pH	441.57 fF

Table 6.3: Series parallel section element values

And the final lumped element filter structure is shown in Fig 6.5.

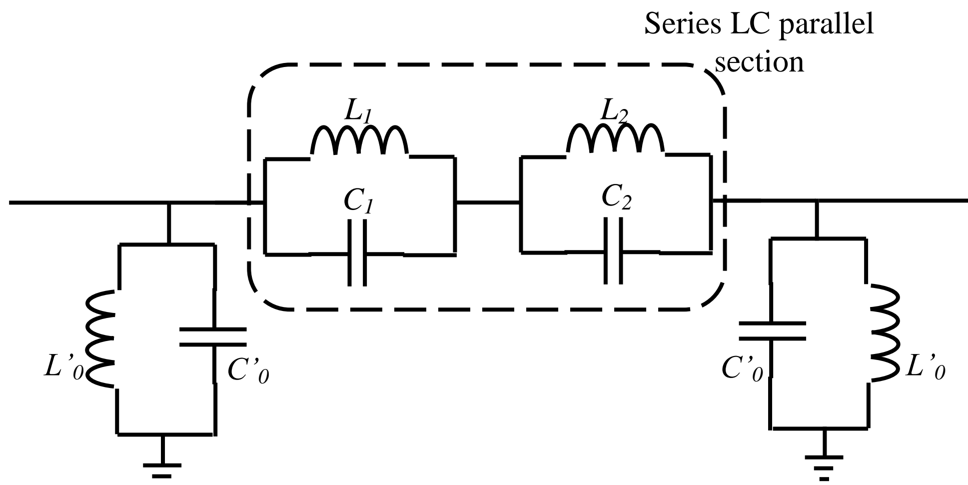


Fig. 6.5 Final inverse Chebyshev band pass filter structure.

Based on the calculated values, simple transmission lines can be used to construct the inductors. Capacitances can be obtained from foundry provided MIM capacitors.

6.3.2 CMOS MIM Capacitor Design

The same technology used in the active filter design was used and the layer configuration is the same as Fig 5.10. Models given by the foundry for the MIM capacitor may not be valid at high frequencies such as at 27.5 GHz. Therefore, the Sonnet EM electromagnetic simulator is used to model the foundry capacitors. Fig 6.6 illustrates a cross sectional view of a MIM capacitor based on Global Foundries 0.13 μm CMOS process.

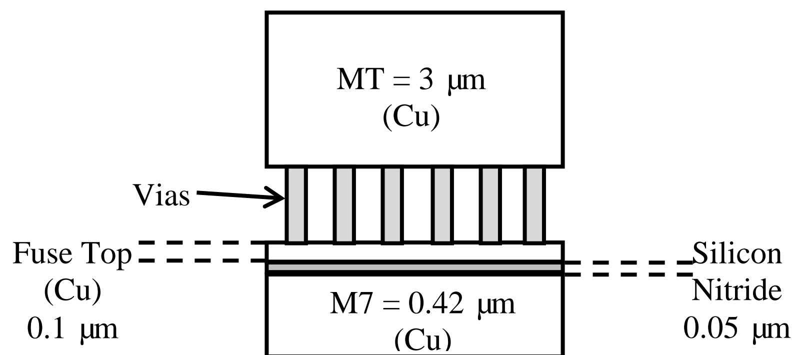


Fig. 6.6 Cross section view of an MIM capacitor structure

The thickness of the Silicon Nitride layer, which acts as the dielectric is around 0.05 μm. However, this value may vary with the process variations. For a typical case, this value is around 0.05 μm and for a best case scenario this value is around 0.0575 μm. Based on the above structure, a 50 fF MIM capacitor was simulated and compared with the foundry provided model.

A comparison between the simulated Sonnet structure and the foundry model is shown in Fig 6.7.

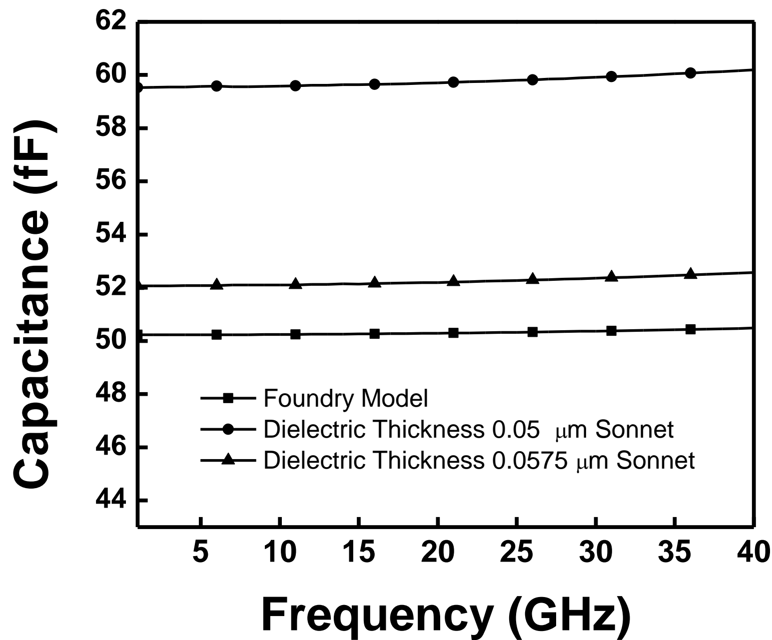


Fig. 6.7 Comparison between MIM capacitor foundry model with Sonnet simulation.

It can be seen that the Sonnet simulation results differ from the model provided by the foundry. This may be because the model provided by the foundry may not be valid at higher frequencies. It is also apparent that the thickness of the dielectric layer influences the value of the capacitance. Choosing the dielectric thickness as 0.0575 μm provides a value much closer the foundry model.

6.3.3 Filter Layout Design

The layout is first optimized with the series LC parallel sections. Then the simulated S-parameters are combined with the schematic lumped components to optimize the shunt LC section in schematic level. Next, shunt LC sections are designed in Sonnet and combined with the optimized series LC parallel sections. Finally the circuit was once more optimized with the input feed lines and the pads.

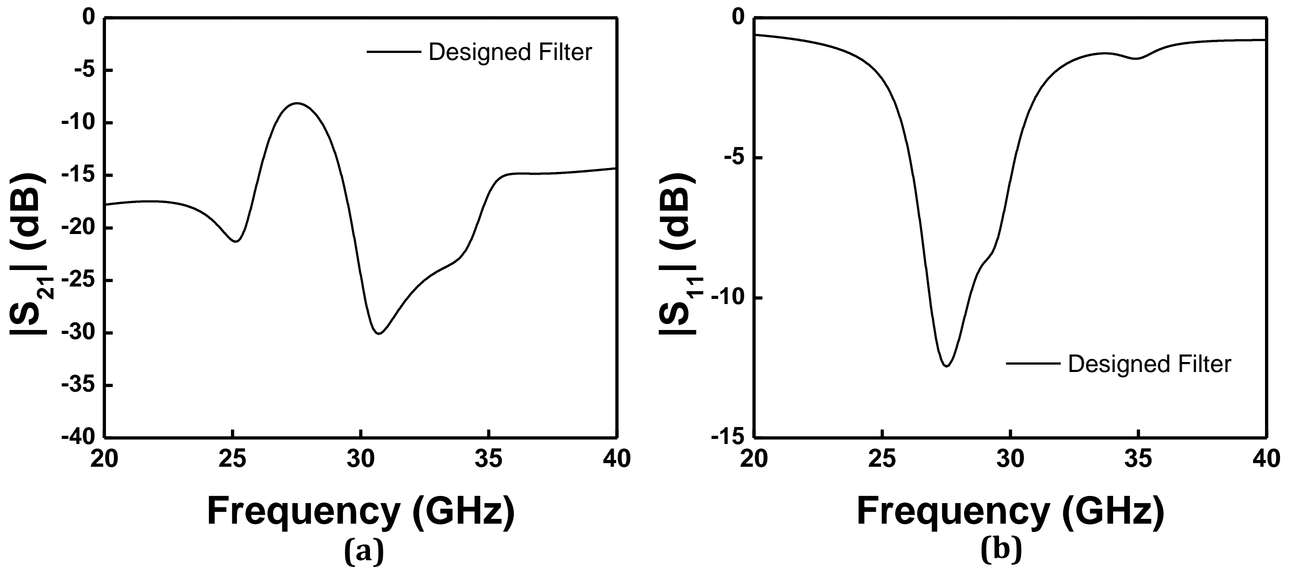


Fig. 6.8 Sonnet simulation results (a) $|S_{21}|$ (dB); (b) $|S_{11}|$ (dB).

Fig 6.8 shows the simulated S-parameters of the designed filter. The simulated, filter has an insertion loss of about 8 dB with a return loss better than 10 dB and a 3 dB bandwidth of 7%. The designed filter is based on a Silicon Nitride thickness equal to 0.0575 μm. Fig 6.9 shows a comparison of the filter S-parameters for different dielectric thicknesses.

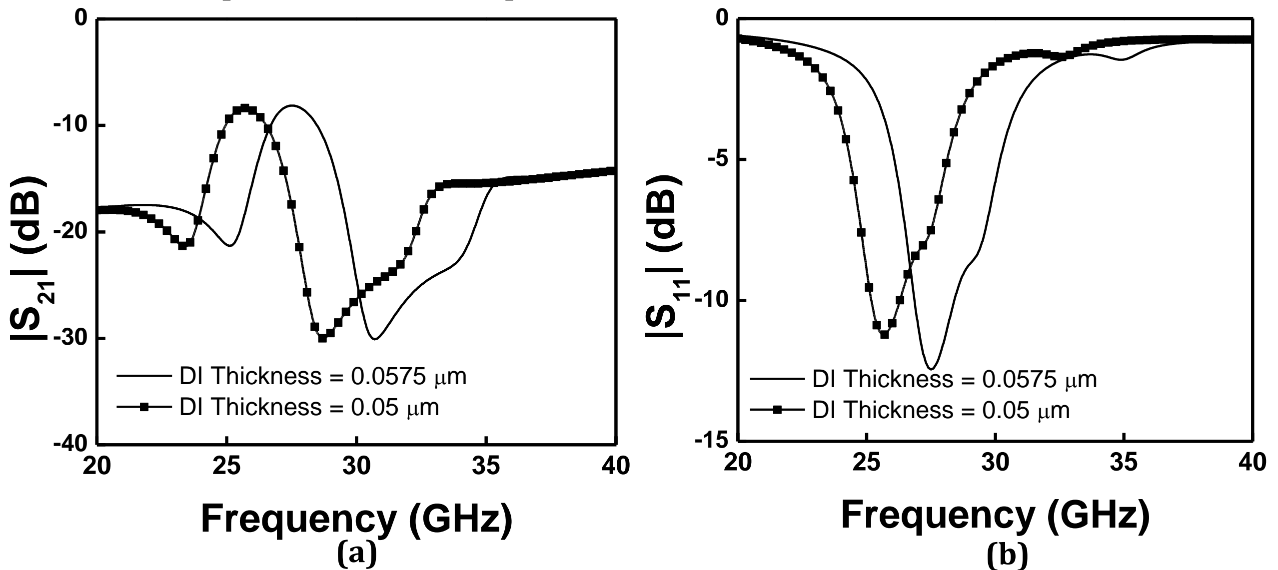


Fig. 6.9 Sonnet simulation for different dielectric thickness
(a) $|S_{21}|$ (dB); (b) $|S_{11}|$ (dB).

When the thickness is equal to 0.05 μm the graph shifts to the left of the initial designed filter. Therefore, several circuits were designed with different centre frequencies. This can

be done by increasing or decreasing the capacitor sizes. Increase the capacitor size causes a shift to the right and decreasing the size causes a shift to the left. Fig 6.10 shows the S-parameter results for the designed filter at different centre frequencies.

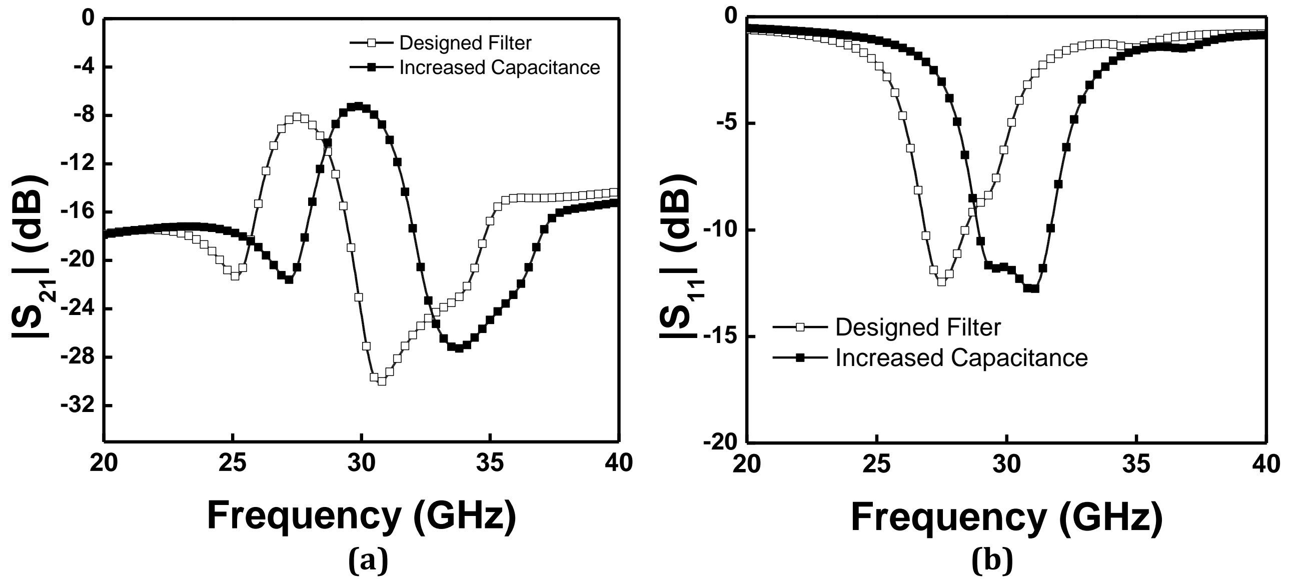


Fig. 6.10 S-parameter simulation results with frequency shift
(a) $|S_{21}|$ (dB); (b) $|S_{11}|$ (dB).

The performance of the filter may vary with the variations in the silicon conductivity. Therefore, several simulations were done with several conductivities and results are illustrated in Fig 6.11. Based on the simulation, variations in the conductivity does not affect the filter performance significantly.

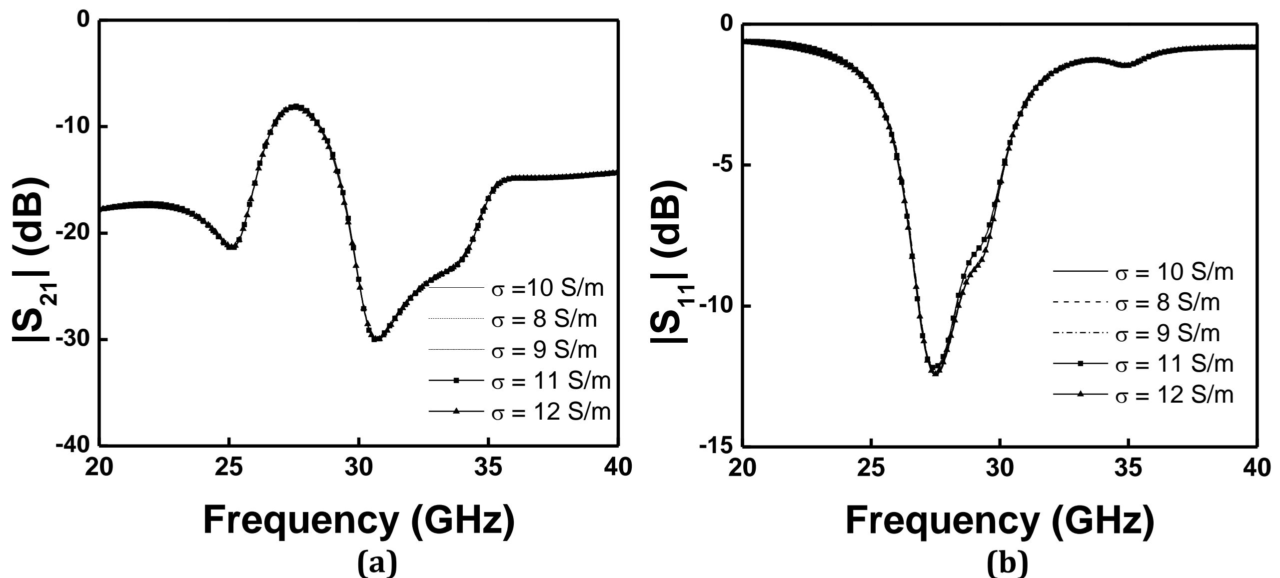


Fig. 6.11 S-parameter simulation results of different substrate conductivities
(a) $|S_{21}|$ (dB); (b) $|S_{11}|$ (dB).

Fig 6.12 shows the final 3D view of the designed filter. The final layout, which was sent for fabrication, is shown in Fig 6.13. As described in the previous chapter metal slotting was used to avoid dishing. Since the simulations were done without dummy metals, dummy metals were not used in the actual design as well. The total filter occupies an area of 580x410 μm^2.

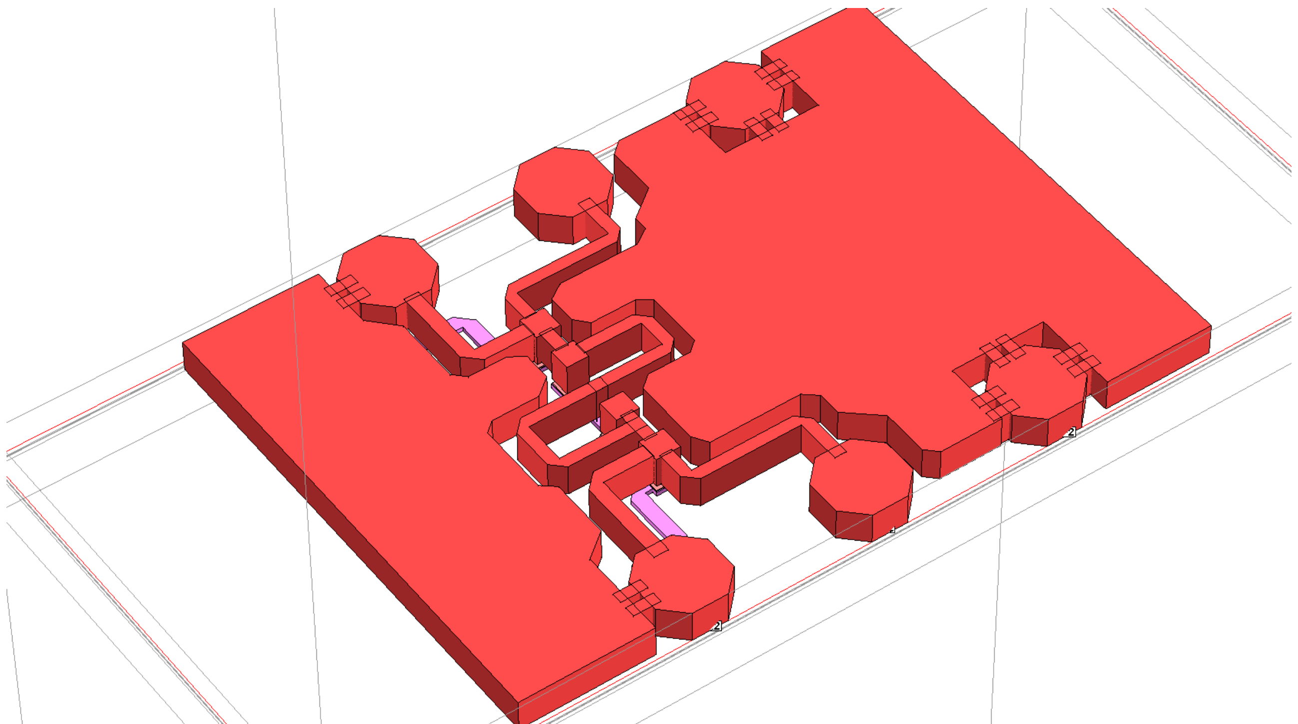


Fig. 6.12 3D view of the designed filter.

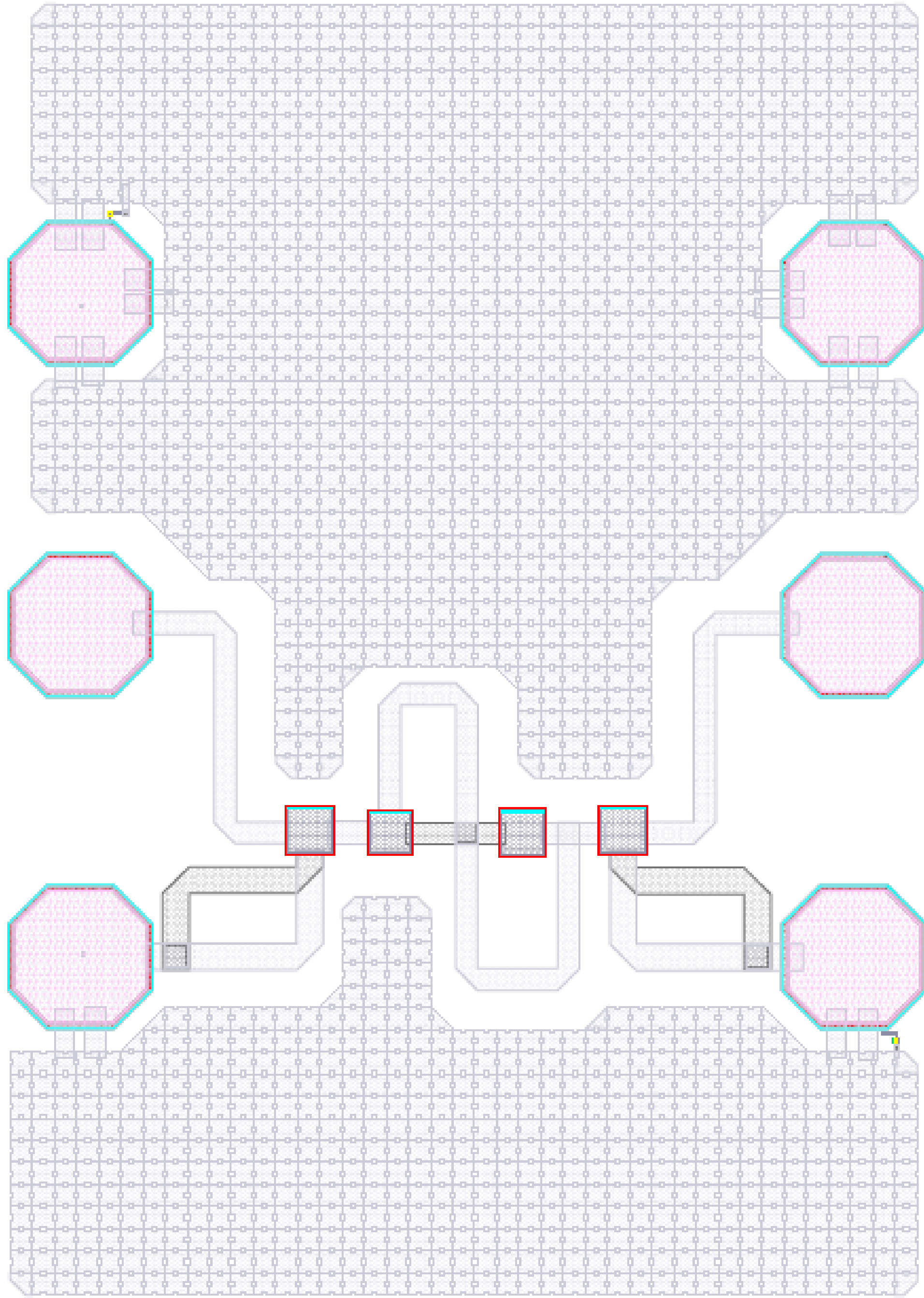


Fig. 6.13 Layout of the lumped element filter.

6.4 Conclusions

This work demonstrates the implementation of a narrow band passive filter at 27.5 GHz. The design is based on inverse Chebyshev characteristic lumped element filter. The designed filter had a 3 dB bandwidth of 7% with an insertion loss 8 dB. Based on the simulations, process variations may change the values of the MIM capacitance, which causes a shift in the centre frequency. Therefore several designs were done by changing the capacitance value of the design. The final filter was sent for fabrication.

CHAPTER 7

Conclusions and Recommendations

This thesis consists of two subprojects. The first project reports the implementation of a broadband distributed amplifier on PCB. The second project consists of two designs. The first design demonstrates the design and implementation of a CMOS active filter. And the second design demonstrates the design of a CMOS passive filter. In this chapter main results are summarized and recommendations are presented.

7.1 Distributed Amplifier Design

Due to the rapid grow of various mobile communication standards, the interest in multi-mode transceivers has increased substantially. The software-defined architecture is a concept suitable for multimode transceiver systems where broadband amplifiers play an important role. The distributed amplifier is an ingenious topology which can be used to obtain a broad bandwidth with a good gain and a good return loss. In this work we have designed and fabricated a distributed amplifier on PCB. The fabricated amplifier has a gain of 15 dB and a return loss better than 15 dB, throughout the bandwidth of 3 GHz. Simulations using the measured S parameters of the transistor with CPW calibration kit

provide results closer to the measurement results at low frequencies. Listed below are some of the suggestions for further improvements:

- It was found that the lack of accurate calibration caused larger discrepancies between the measured and simulated results. Therefore, calibration has to be performed carefully to obtain accurate S-parameter measurements for the transistors.
- The measured behaviour of the input and output return losses differ from the simulated losses. Therefore further investigations are needed to identify the reasons for the discrepancies.
- The input P1dB of the designed amplifier is around – 5 dBm. Hence, the amplifier is not suitable to work as a power amplifier. This is mainly due to the fact that the transistors used are not optimized for high power applications. However, new techniques have to be investigated on improving the large signal performance of a distributed amplifier.

7.2 CMOS Active and Passive Filter Design

Due to the lossy nature of the silicon substrate, interests, for using active components in filter design has increased greatly. Transversal filtering is a known technique commonly used in digital domain. In a microwave transversal topology, active components are used to compensate the losses of the passive components. These active components also help to provide good out of band rejection. Such a topology has been rarely reported for CMOS processes and in this work we have designed and measured such a filter in CMOS process. The designed filter has a bandwidth of 2 GHz from 2.0 – 4.0 GHz and a return loss better than – 10 dB. Pass band rejections at 1.5 GHz and 5.5 GHz were better than – 40 dB.

Based on simulations and measurements, it was found that placing a ground plane below the inductor reduces the inductance and the Q factor of the inductor. Secondly a microwave

passive filter at Ka band is designed. Due to the unavailability of transistor models at high frequencies, a passive filter circuit is chosen. The designed filter is based on inverse Chebyshev response. Since the models provided by the foundry were not suitable at high frequencies, Sonnet's EM electromagnetic simulator is used to model the capacitors at high frequencies. Recommendations for further research in CMOS passive filter design are as follows:

- Based on the EM simulations, the designed filter has a bandwidth of 7% at a centre frequency of 27.5 GHz and a return loss of around 8.0 dB. To improve the insertion loss of such filters it is recommended to use active elements to compensate for the losses. Hence, accurate transistor models at those frequencies are needed.
- In this study, MIM capacitors were used to design the band pass filter structure. However, Q factor of such capacitors is not high enough at microwave frequencies. Therefore, new capacitor structures need to be investigated to achieve good Q factors.

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Appendix A

Consider the chain matrix obtained in terms of the parameters of the two-port network inside the four-port shown in Fig A.1.

$$\begin{bmatrix} V_{dk-1} \\ I_{dk-1} \\ V_{gk-1} \\ I_{gk-1} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{13} & A_{14} \\ A_{21} & A_{22} & A_{23} & A_{24} \\ A_{31} & A_{32} & A_{33} & A_{34} \\ A_{41} & A_{42} & A_{43} & A_{44} \end{bmatrix} \begin{bmatrix} V_{dk} \\ I_{dk} \\ V_{gk} \\ I_{gk} \end{bmatrix} \quad \text{(A.1)}$$

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad \text{(A.2)}$$

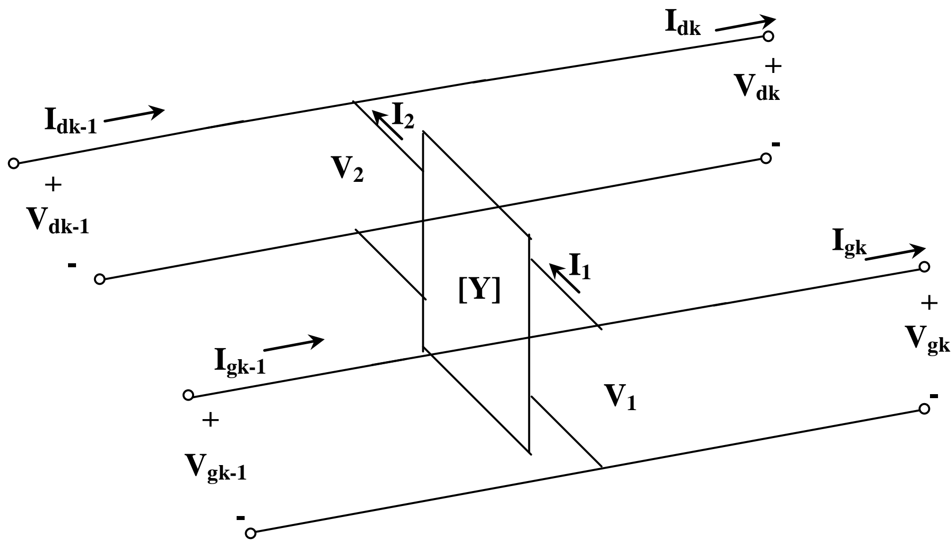


Fig A.1: Four port network

$$V_{dk-1} = V_{dk} \quad \text{(A.3)}$$

$$I_{dk-1} = I_{dk} - I_2 \quad \text{(A.4)}$$

$$V_{gk-1} = V_{gk} \quad \text{(A.5)}$$

$$I_{gk-1} = I_{gk} + I_1 \quad \text{(A.6)}$$

From equation (A.3)

$$A_{11} = 1 \tag{A.7}$$

$$A_{12} = \left.\frac{V_{dk-1}}{I_{dk}}\right|_{V_{dk},V_{gk},I_{gk}} = 0 \tag{A.8}$$

$$A_{13} = \left.\frac{V_{dk-1}}{V_{gk}}\right|_{V_{dk},I_{dk},I_{gk}} = 0 \tag{A.9}$$

$$A_{14} = \left.\frac{V_{dk-1}}{I_{gk}}\right|_{V_{dk},I_{dk},V_{gk}} = 0 \tag{A.10}$$

The second row of the chain matrix is obtained as:

$$A_{21} = \left.\frac{\mathrm{I}_{dk-1}}{V_{dk}}\right|_{I_{dk},V_{gk},I_{gk}} = -\left.\frac{I_2}{V_2}\right|_{V_1} = \frac{A}{B} = Y_{22} \tag{A.11}$$

$$A_{22} = \left.\frac{I_{dk-1}}{I_{dk}}\right|_{V_{dk},V_{gk},I_{gk}} = 1 \quad (I_{dk-1} = I_{dk}\ when\ I_2 = 0, V_2 = V_1 = 0) \tag{A.12}$$

$$A_{23} = \left.\frac{I_{dk-1}}{V_{gk}}\right|_{V_{dk},I_{dk},I_{gk}} \tag{A.13}$$

$$= -\frac{I_2}{V_1} = -\frac{1}{B} = y_{21} \quad (I_{dk-1} = -I_2,\ I_{dk} = 0)$$

$$A_{24} = \left.\frac{I_{dk-1}}{I_{gk}}\right|_{V_{dk},I_{dk},V_{gk}} = 0 \quad (I_2 = 0, \qquad V_2 = V_1 = 0) \tag{A.14}$$

Similarly we find for the third and fourth rows

$$A_{31} = \left.\frac{V_{gk-1}}{V_{dk}}\right|_{I_{dk},V_{gk},I_{gk}} = 0 \tag{A.15}$$

$$A_{32} = \left.\frac{V_{gk-1}}{I_{dk}}\right|_{V_{dk},V_{gk},I_{gk}} = 0 \tag{A.16}$$

$$A_{33} = \left.\frac{V_{gk-1}}{V_{gk}}\right|_{V_{dk},I_{dk},I_{gk}} = 1 \tag{A.17}$$

$$A_{34} = \left.\frac{V_{gk-1}}{I_{gk}}\right|_{V_{dk},I_{dk},V_{gk}} = 0 \tag{A.18}$$

$$A_{41} = \left.\frac{\mathrm{I}_{gk-1}}{V_{dk}}\right|_{I_{dk},V_{gk},I_{gk}} = -\left.\frac{I_1}{V_2}\right|_{V_1} = y_{12} \tag{A.19}$$

$$A_{42} = \left.\frac{I_{gk-1}}{I_{dk}}\right|_{V_{dk},V_{gk},I_{gk}} = \left.\frac{I_1}{I_{dk}}\right|_{V_1,V_2} = 0 \tag{A.20}$$

$$A_{43} = \left.\frac{I_{gk-1}}{V_{gk}}\right|_{V_{dk},I_{dk},I_{gk}} = \left.\frac{I_1}{V_1}\right|_{V_2} = y_{11} = \frac{D}{B} \tag{A.21}$$

$$A_{44} = \left.\frac{I_{gk-1}}{I_{gk}}\right|_{V_{dk},I_{dk},V_{gk}} = \left.\frac{I_{gk-1}}{I_{gk}}\right|_{I_1} = 1 \tag{A.22}$$

Hence, the chain matrix is obtained as:

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ y_{22} & 1 & y_{21} & 0 \\ 0 & 0 & 1 & 0 \\ y_{12} & 0 & y_{11} & 1 \end{bmatrix} \tag{A.23}$$

When the shunt arms of the artificial line section are included, y_{11} is replaced by $y_{11}+y_g$ and y_{22} is replaced by $y_{22}+y_d$.

$$A_t = \begin{bmatrix} 1 & 0 & 0 & 0 \\ y_{22} + y_d & 1 & y_{21} & 0 \\ 0 & 0 & 1 & 0 \\ y_{12} & 0 & y_{11} + y_g & 1 \end{bmatrix} \tag{A.24}$$

Appendix B

ATF-36077

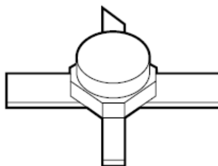
2–18 GHz Ultra Low Noise Pseudomorphic HEMT

Data Sheet

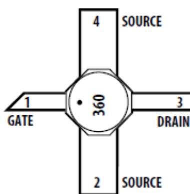
Description

Avago Technologies' ATF-36077 is an ultra-low-noise Pseudomorphic High Electron Mobility Transistor (PHEMT), packaged in a low parasitic, surface-mountable ceramic package. Properly matched, this transistor will provide typical 12 GHz noise figures of 0.5 dB, or typical 4 GHz noise figures of 0.3 dB. Additionally, the ATF-36077 has very low noise resistance, reducing the sensitivity of noise performance to variations in input impedance match, making the design of broadband low noise amplifiers much easier. The premium sensitivity of the ATF-36077 makes this device the ideal choice for use in the first stage of extremely low noise cascades. The repeatable performance and consistency make it appropriate for use in Ku-band Direct Broad-cast Satellite (DBS) Television systems, C-band Television Receive Only (TVRO) LNAs, or other low noise amplifiers operating in the 2-18 GHz frequency range.

77 Package



Pin Configuration



Features

- **PHEMT Technology**
- **Ultra-Low Noise Figure:**
  0.5 dB Typical at 12 GHz
  0.3 dB Typical at 4 GHz
- **High Associated Gain:**
  12 dB Typical at 12 GHz
  17 dB Typical at 4 GHz
- **Low Parasitic Ceramic Microstrip Package**
- **Tape-and-Reel Packing Option Available**

Applications

- **12 GHz DBS LNB (Low Noise Block)**
- **4 GHz TVRO LNB (Low Noise Block)**
- **Ultra-Sensitive Low Noise Amplifiers**

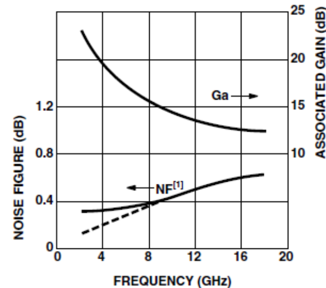


Figure 1. ATF-36077 Optimum Noise Figure and Associated Gain vs. Frequency for V_{DS} = 1.5 V, I_D = 10 mA.

This GaAs PHEMT device has a nominal 0.2 micron gate length with a total gate periphery (width) of 200 microns. Proven gold based metalization systems and nitride passivation assure rugged, reliable devices.

Note: 1. See Noise Parameter Table.

ATF-36077 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain – Source Voltage	V	+3
V_{GS}	Gate – Source Voltage	V	-3
V_{GD}	Gate-Drain Voltage	V	-3.5
I_D	Drain Current	mA	I_{dss}
P_T	Total Power Dissipation[3]	mW	180
$P_{in\ max}$	RF Input Power	dBm	+10
T_{ch}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2,3]: θ_{ch-c} = 60°C/W

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Measured at P_{diss} = 15 mW and T_{ch} = 100°C.
3. Derate at 16.7 mW/°C for T_C > 139°C.

ATF-36077 Electrical Specifications,

T_C = 25°C, Z_O = 50 Ω, V_{ds} = 1.5 V, I_{ds} = 10 mA, (unless otherwise noted).

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF	Noise Figure[1]	f = 12.0 GHz	dB		0.5	0.6
G_A	Gain at NF[1]	f = 12.0 GHz	dB	11.0	12.0	
g_m	Transconductance	V_{DS} = 1.5 V, V_{GS} = 0 V	mS	50	55	
I_{dss}	Saturated Drain Current	V_{DS} = 1.5 V, V_{GS} = 0 V	mA	15	25	45
$V_{p\ 10\%}$	Pinch-off Voltage	V_{DS} = 1.5 V, I_{DS} = 10% of I_{dss}	V	-1.0	-0.35	-0.15

Note:

1. Measured in a fixed tuned environment with Γ source = 0.54 at 156°; Γ load = 0.48 at 167°.

ATF-36077 Characterization Information,

T_C = 25°C, Z_O = 50 Ω, V_{ds} = 1.5 V, I_{ds} = 10 mA, (unless otherwise noted).

Symbol	Parameters and Test Conditions		Units	Typ.
NF	Noise Figure (Tuned Circuit)	f = 4 GHz	dB	0.3[2]
		f = 12 GHz	dB	0.5
G_A	Gain at Noise Figure (Tuned Circuit)	f = 4 GHz	dB	17
		f = 12 GHz	dB	12
$S_{12\ off}$	Reverse Isolation	f = 12 GHz, V_{DS} = 1.5 V, V_{GS} = -2 V	dB	14
P_{1dB}	Output Power at 1 dB Gain Compression	f = 4 GHz	dBm	5
		f = 12 GHz	dBm	5
$V_{GS\ 10\ mA}$	Gate to Source Voltage for I_{DS} = 10 mA	V_{DS} = 1.5 V	V	-0.2

Note:

2. See noise parameter table.

ATF-36077 Typical Scattering Parameters,
Common Source, $Z_O = 50\ \Omega$, $V_{DS} = 1.5$ V, $I_D = 10$ mA

Freq. GHz	S_{11} Mag.	S_{11} Ang.	S_{21} dB	S_{21} Mag.	S_{21} Ang.	S_{12} dB	S_{12} Mag.	S_{12} Ang.	S_{22} Mag.	S_{22} Ang.
1.0	0.99	-17	14.00	5.010	163	-36.08	0.016	78	0.60	-14
2.0	0.97	-33	13.81	4.904	147	-30.33	0.030	66	0.59	-28
3.0	0.94	-49	13.53	4.745	132	-27.25	0.043	54	0.57	-41
4.0	0.90	-65	13.17	4.556	116	-25.32	0.054	43	0.55	-54
5.0	0.86	-79	12.78	4.357	102	-24.04	0.063	33	0.53	-66
6.0	0.82	-93	12.39	4.162	88	-23.17	0.069	24	0.50	-78
7.0	0.78	-107	12.00	3.981	75	-22.58	0.074	16	0.48	-89
8.0	0.75	-120	11.64	3.820	62	-22.17	0.078	8	0.46	-99
9.0	0.72	-133	11.32	3.682	49	-21.90	0.080	1	0.44	-109
10.0	0.69	-146	11.04	3.566	37	-21.71	0.082	-6	0.42	-119
11.0	0.66	-159	10.81	3.473	25	-21.57	0.083	-13	0.40	-129
12.0	0.63	-172	10.63	3.401	13	-21.44	0.085	-19	0.38	-139
13.0	0.61	175	10.50	3.349	1	-21.32	0.086	-25	0.37	-149
14.0	0.60	161	10.41	3.315	-12	-21.19	0.087	-32	0.35	-160
15.0	0.58	147	10.36	3.296	-24	-21.04	0.089	-39	0.33	-171
16.0	0.57	131	10.34	3.289	-37	-20.87	0.091	-47	0.31	177
17.0	0.56	114	10.34	3.289	-50	-20.69	0.092	-55	0.29	164
18.0	0.57	97	10.35	3.291	-64	-20.53	0.094	-65	0.26	148

ATF-36077 Typical "Off" Scattering Parameters,
Common Source, $Z_O = 50\ \Omega$, $V_{DS} = 1.5$ V, $I_D = 0$ mA, $V_{GS} = -2$ V

Freq. GHz	S_{11} Mag.	S_{11} Ang.	S_{21} dB	S_{21} Mag.	S_{21} Ang.	S_{21} dB	S_{21} Mag.	S_{21} Ang.	S_{22} Mag.	S_{22} Ang.
11.0	0.96	-139	-14.2	0.19	-43	-14.2	0.19	-43	0.97	-125
12.0	0.95	-152	-14.0	0.20	-56	-14.0	0.20	-56	0.97	-137
13.0	0.94	-166	-13.8	0.20	-69	-13.8	0.20	-68	0.96	-149

ATF-36077 Typical Noise Parameters,

Common Source, $Z_O = 50\ \Omega$, $V_{DS} = 1.5$ V, $I_D = 10$ mA

Freq. GHz	F_{min}[1] dB	Γ_{opt} Mag.	Ang.	R_n/Z_o -
1	0.30	0.95	12	0.40
2	0.30	0.90	25	0.20
4	0.30	0.81	51	0.17
6	0.30	0.73	76	0.13
8	0.37	0.66	102	0.09
10	0.44	0.60	129	0.05
12	0.50	0.54	156	0.03
14	0.56	0.48	-174	0.02
16	0.61	0.43	-139	0.05
18	0.65	0.39	-100	0.09

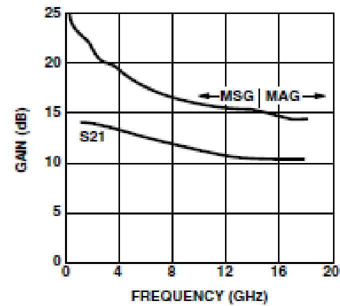
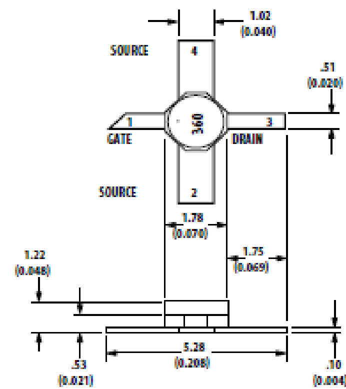


Figure 2. Maximum Available Gain, Maximum Stable Gain and Insertion Power Gain vs. Frequency. $V_{DS} = 1.5$ V, $I_D = 10$ mA.

Note:

1. The F_{min} values at 2, 4, and 6 GHz have been adjusted to reflect expected circuit losses that will be encountered when matching to the optimum reflection coefficient (Γ_{opt}) at these frequencies. The theoretical F_{min} values for these frequencies are: 0.10 dB at 2 GHz, 0.20 dB at 4 GHz, and 0.29 dB at 6 GHz. Noise parameters are derived from associated s parameters, packaged device measurements at 12 GHz, and die level measurements from 6 to 18 GHz.

77 Package Dimensions



TYPICAL DIMENSIONS ARE IN MILLIMETERS (INCHES).

Part Number Ordering Information

Part Number	No. of Devices	Container
ATF-36077-TR1[2]	1000	7" Reel
ATF-36077-STR	100	strip

Note:

2. For more information, see "Tape and Reel Packaging for Semiconductor Devices," in "Communications Components" Designer's Catalog.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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AV02-1222EN - April 29, 2008

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