DYNAMIC CONTROL IN ENERGY STORAGE AUGMENTED RENEWABLE ENERGY SYSTEM

ZHOU HAIHUA

NATIONAL UNIVERSITY OF SINGAPORE

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ZHOU HAIHUA

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Contents

Summary

Renewable energy is a way to solve the energy crisis problem. However, its slow dynamic response or/and intermittent characteristics prohibit its wide applications.

Energy storage system is thus needed to satisfy the differences between source and load. To actively control power flow and to meet voltage differences between energy storage and load, power electronic converter is essential.

The objective of this thesis are

- To design and control a bi-directional converter in a wide operating range for energy storage
- To design and control an energy storage augmented renewable source system to maximally use the renewable power and to satisfy load requirements

Energy storage and load requirements specify the bi-directional converter design and control. Energy storage provides low and varying output voltage while

load voltage can be high. Phase shifted Dual Active Bridge (DAB) converter provides high voltage boost ratio and nature isolation. Therefore DAB is chosen here. Since the terminal voltage of energy storage and the load power always vary, it is desirable that DAB operates in a wide operating range. In the thesis, a hybrid modulation scheme is proposed and implemented to widen the power transfer capability in DAB. Feedback liberalization controller is designed to regulate the voltage in a linear form.

In energy storage augmented renewable energy system, a power electronic converter is also needed to actively control power flow between the renewable energy source and the DC bus. Similar to energy storage, its terminal voltage can be also low and varying while DC voltage can be high. Boost type converter is usually preferred. Control of boost type converter naturally faces difficulties in designing a stable wide bandwidth controller. This is due to its non-minimum phase shift relationship between output voltage and control variable. A passivity based controller (PBC) is investigated. Results show the non-minimum phase shift relationship still exists in the boost converter but by proper injecting the damping in the current trajectory, PBC controller can achieve a stable voltage regulation in a wide range as well as maintain a good dynamic performance.

The design objectives of the energy storage augmented renewable source system are to use renewable power as much as possible and to regulate the bus voltage. Energy management scheme then is designed to coordinate power flow between renewable source and energy storage. Current regulation is implemented for renewable source while voltage regulation is achieved by energy storage. Simulation and experimental results show the effectiveness of source current regulation and

fast load dynamic response. An accurate model to reflect the relationship between load current and source current is also built.

Further, the bi-directional DAB converter system can be extended in microgrid application. The size of energy storage for microgrid application range from hundred kW to few MW. Thus power rating of the bi-directional converter is high. In addition, energy storages can have different functions in a microgrid. For instance, it can function as energy buffer to shift power between two time zones or it can function as power source to support load peak power demands. Modular design achieves high flexibility hence it is used. The proposed modular structure can be scaled up to any power and energy. By properly connecting the modules in series or in parallel, various combinations are possible to meet different source and load requirements. Interleaved scheme is also implemented in modules to reduce input and output ripple. Therefore input and output filter size are reduced. Simulation results confirm that the proposed interleaved modular DAB converter achieves the desired performances.

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Acronyms

ICFFB	Interleaved Current Fed Full Bridge
CFFB	Current Fed Full Bridge
DAB	Dual Active Bridge
SOC	State Of Charge
TZM	Trapezoidal Modulation
TRM	Triangular Modulation

PSM	Phase Shift Modulation
PTRM	Proposed Triangular Modulation
MPF	Mixed Potential Function
BM	Brayton Moser
PBC	Passivity Based Control
IPOS	Input Parallel Output Seires
IPOP	Input Parallel Output Parallel
ISOP	Input Series Output Parallel
ISOS	Input Series Output Series
ZVS	Zero Voltage Switching
FPGA	Field Programmable Gate Array
PWM	Pulse Width Modulation

Chapter 1

Introduction

In modern societies, power generation is mainly dependant on the burning of fossil fuels. However, natural resources such as petroleum, coal, and natural gas are limited in supply, while our energy demand keeps on increasing. According to [1], if our energy demand increases by 2.4% per year, our total fossil fuel will be depleted after 75 years. The situation becomes even worse if the energy demand increases by a rate of 5%, then there is only 50 years of supply left. To continuously meet our energy demand, we have to use energy efficiently as well as to utilize more renewable energy such as Photovoltaics (PV) and wind etc [2].

Renewable energy, which harnesses the natural resources such as sun and wind,is intermittent in nature, see PV power output in Fig. 1.1(b). On the other hand, load demand can be continuous and varying, see residential load demand as

Fig. 1.1(a). To use renewable energy as the primary source, energy storage system should compensate the differences between renewable source and load, its power profile is shown as Fig. 1.1(c).

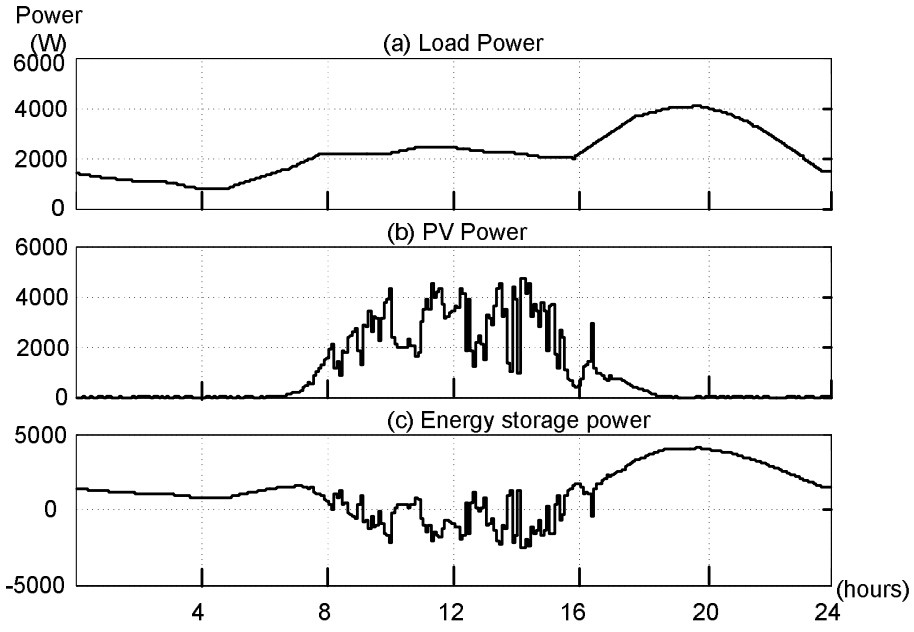


Figure 1.1: Typical 24 hours power profile

(a)Residential load (b)PV source (c) Energy storage

Other than mitigating the intermittency, energy storage system has many applications such as power quality improvement, load shaving, peak power shaving and frequency regulation for grid connected wind power etc [3]. Some structures to connect energy storage with the load are shown in Fig. 1.2. In Fig. 1.2(a)(b), DC type energy storages such as batteries are connected to grid via a Voltage Source Converter (VSC) while super-conducting coil and flywheels, shown as Fig. 1.2(c)(d), are connected via DC-DC and DC-AC converters to the power system [4]. Therefore, power electronics converters are indispensable in energy storage system.

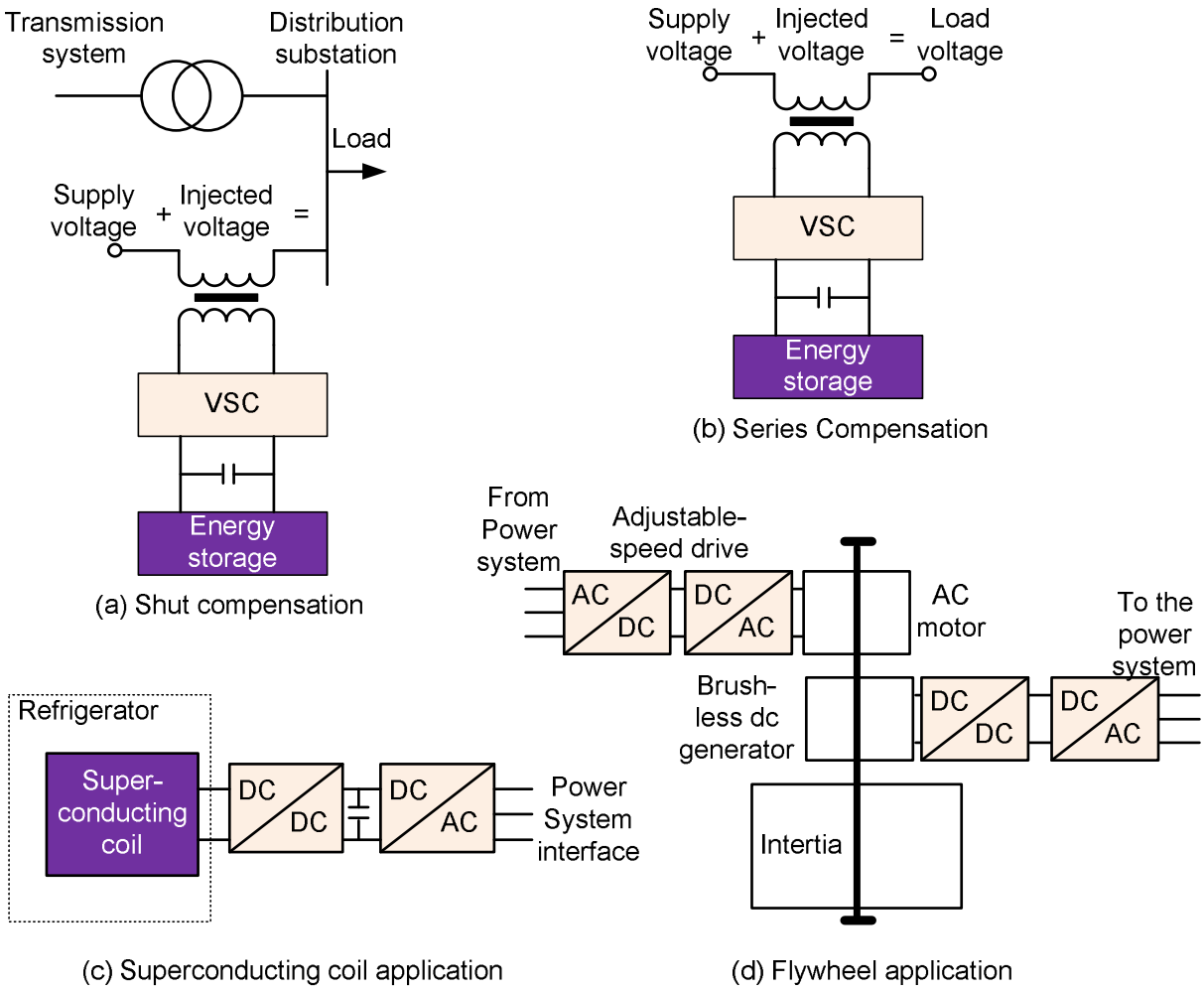


Figure 1.2: Block diagram in using energy storage for various applications

Fig. 1.3 shows the block diagram to connect DC type of renewable energy and energy storage via power converter with different types of load [5].

From Fig. 1.3, we can see that the energy storage is connected to DC bus via a bi-directional converter, see shaded block in the figure. This bi-directional converter plays a very important role. It boosts/bucks source voltage to another DC bus voltage and regulates the DC bus.

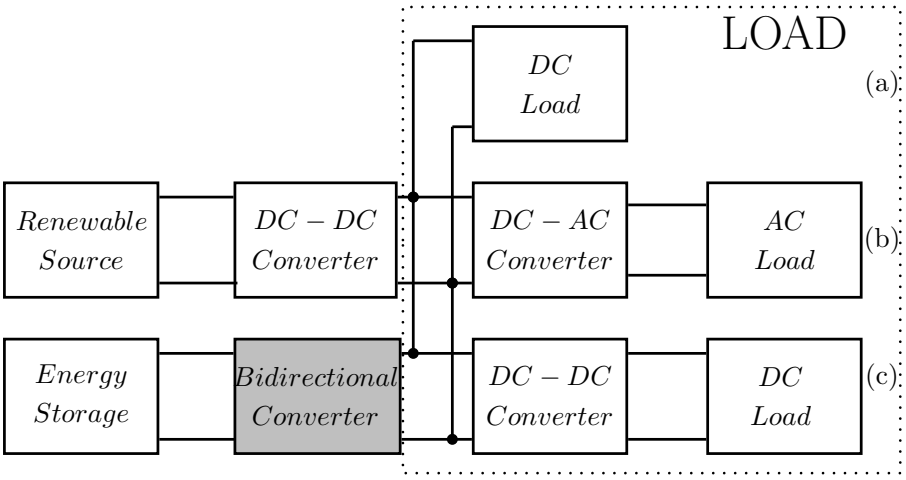


Figure 1.3: Block diagram of augmented system with DC-DC front-end converter

The other possible system block diagram to connect renewable source and energy storage to different loads is shown in Fig. 1.4. In this approach, energy storage is directly connected to AC bus via a bi-directional converter. If energy storage voltage is low and a high AC bus voltage is required, a high boosting capability transformer is needed. However, this 50 Hz transformer can be significantly bulky and costly. At the same time, AC-AC converter using DC link as intermediate is inefficient due to the fact that one more power conversion stage is involved. In addition, terminal voltage of the energy storage, as Table. 1.1 shows, varies a lot. This poses difficulties in DC-AC converter modulation if energy storage is directly connect to DC-AC converter.

As a result, system structure shown as Fig. 1.3 is preferably used in this thesis to connect DC type of energy storage with other DC type renewable energy. Therefore, the focus of this thesis is to explore how to design and control a bi-directional converter for energy storage and how to control energy storage

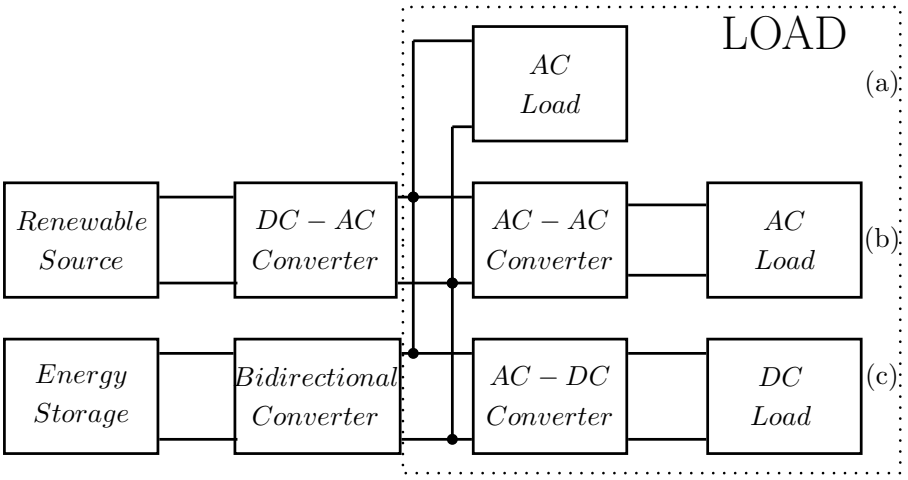


Figure 1.4: Block diagram of augmented system with DC-AC front-end converter augmented renewable energy system.

1.1 Problem Definitions

- **Issue 1: Design of a bi-directional converter with wide power transfer capability**

  Fig. 1.1(c) shows a energy storage power profile for supplying the power differences between a PV source and residential load. From Fig. 1.1(c), the power profile changes over a wide range. Hence a bi-directional converter with wide operating power range, which is shown in Fig. 1.3, is desired to interface energy storage. Literature show that Dual Active Bridge (DAB) converter, which has advantages such as high boost ratio, high power transfer capability and natural isolation, are one of the best converter candidates. However, its conventional phase shift modulation limits its power transfer

capability to low power ranges. Therefore, the challenge is, how to design a DAB converter with a wide power transfer capability.

- **Issue 2: Control of DAB converter with nonlinear characteristics**

  In order to actively control power flow from the energy storage and regulate the DC bus voltage, a proper controller is required. Furthermore, (1) the source voltage and load power vary in a wide range and (2) the relationship between the control variable and the control objective is nonlinear. Therefore, design of a simple controller to regulate the output voltage in a wide range becomes another challenge.

- **Issue 3: Control a boost type converter for stable operation in a wide range**

  Boost type converter is used to interface current-fed renewable energy and high voltage dc bus. However, boost type converter has non-minimum phase characteristics. Thus it poses difficulties in designing a stable wide bandwidth controller. The challenge becomes to control boost type converter stably in a wide range.

- **Issue 4: Case study: Dynamic power distribution between renewable source and energy storage system**

  Energy storage can be designed to achieve different roles in the system shown in Fig. 1.3. No matter what kind of renewable source is used, load always demands a fast dynamic response in case of any load variation. However, renewable source can be intermittent or slow in responding. Hence, the chal-

lenge are how to regulate the DC bus voltage and how to control the power distribution between the renewable source and energy storage.

1.2 Contributions of the thesis

- **Hybrid modulation for achieving a wide power transfer capability in Dual Active Bridge Converter**

  A hybrid modulation methodology that uses triangular modulation in low power region and conventional phase shift modulation in high power region is proposed to achieve a wider range of power transfer in DAB.

- **Feedback linearization control to regulate DAB voltage in a linear approach**

  A feedback linearization algorithm is used to overcome difficulties in handling the nonlinear relationship between output current and control variable, and thus voltage regulation can be achieved over a wide operating range.

- **Passivity Based Control for Interleaved Current Fed Full Bridge (ICFFB) achieves stable voltage regulation in a wide operating range**

  An energy-based approach using a Brayton-Moser modeled passivity-based controller along with an augmented integrator is proposed for boost type front-end converter for renewable energy. It achieves voltage regulation under wide operating range.

- **Dynamic power distribution controller is designed for energy storage augmented renewable energy system**

  A controller is proposed to achieve (1) fast voltage regulation by using ultracapacitor to compensate dynamic load power and (2) maximum power utilization in renewable energy.

1.3 Organization of the thesis

Based on above descriptions, this thesis is organized as

- **Chapter 2** investigates various topologies for bi-directional converters. Dual Active Bridge is chosen and its operating principles are reviewed. Limitation of power transfer in low power range is discussed and a hybrid modulation scheme is proposed to achieve wide power transfer range.

- **Chapter 3** discusses the nonlinear relationship between the control objective and control variables. Various controller are reviewed and a feedback linearization controller is designed. Experiments are conducted to verify the effectiveness of the controller.

- **Chapter 4** discusses the non-minimum phase relationship in the boost type converter for renewable energy application. Non-minimum phase relationship poses difficulties in designing a stable wide bandwidth controller. Brayton-

Moser Form based Passivity-Based Controller is explored. Finally, evaluation of PBC controller with respect to PI controller is provided.

- **Chapter 5** provides a case study for quick regulation of the output voltage and to dynamically distribute the power between energy storage and renewable energy. Small signal models for the two converters are developed and controllers are designed. Experimental results validate the functionality of the controller.

- **Chapter 6** proposes an interleaved DAB converter for interfacing high power energy storage in micro-grid application. Modular approach enables the flexible configuration and high power transfer capability when multiple modules are connected.

- **Chapter 7** concludes the main issues studied in the thesis. Future work is also discussed.

Table 1.1: Voltage swing in different energy storages

[6]

Storage type	Nominal Voltage v_N (V)	Final voltage v_f (V)	Charging voltage v_{chg}(V)	Voltage Swing $(v_{chg}/v_f - 1)\%$
ZEBRA	2.58	1.72	2.85	65
NaS	2.08	1.82	2.3	26
Ni-Cd	1.2	1.0	1.5	50
Lead-Acid	1.94	1.79	2.3	28
Li-Ion	3.6	2.7	4.0	48
Ultracapacitor	2,7	1.25	2.5	50

Chapter 2

Hybrid modulation to widen power transfer capability

2.1 Introduction

As mentioned in the introduction, a bi-directional converter is the key to interface the energy storage to the DC bus. By controlling the power in bi-directional converter, the power transfer between the energy storage and the load can be actively controlled.

The design of bi-directional converter should satisfy both energy storage and load requirements. The selection of the energy storage is dependent on its role in

the system. For instance, it can be used for peak power shaving or it can be used for load shifting etc.

Ragone chart [7], as shown in Fig. 2.1, describes the relation between specific energy (in Wh/kg) and specific power (in W/kg) for different energy storage technologies. From the figure, it is shown that the ultracapacitor has high power density and low energy density. Therefore it is suitable to be used where fast power delivery is needed. On the other hand, lead-acid has high energy density. Hence, it is preferred when high energy capacity is required. In this thesis, ultracapacitor is selected as the energy storage to compensate fast dynamic requirement. If continuous energy is needed for long term, then battery is a better choice. In either form, same methodology on bi-directional converter and controller design can be applied.

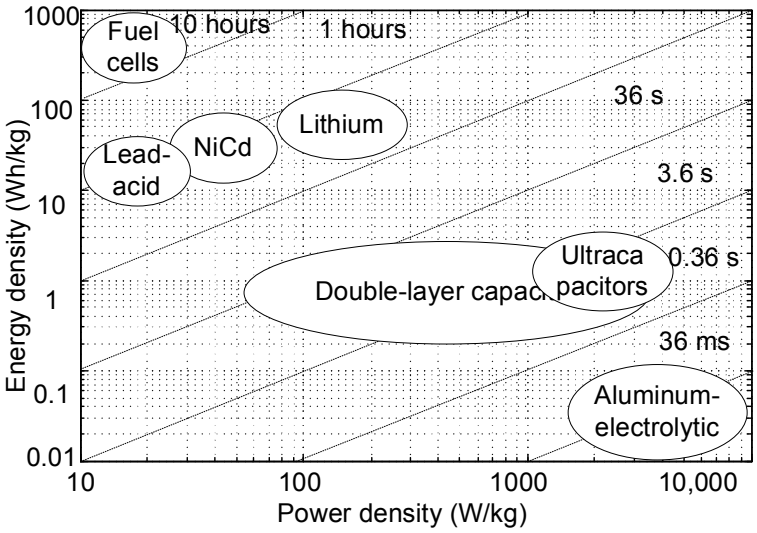


Figure 2.1: Ragone chart for alternative sources

Ultracapacitor, as many other energy storages, has low output voltage. Rated voltage for a single cell ultracapacitor is approximately 2.7V while ultracapacitor module voltage is in several tens of volts. On the other hand, DC bus voltage usually is high. Therefore, a high voltage boost ratio bi-directional converter is required to connect ultracapacitor and DC bus. In addition, ultracapacitor voltage varies under charging and discharging process. Power profile for energy storage also changes over a wide range. Hence, bi-directional converter should be able to transfer a wide range power under large voltage variation.

Furthermore, to meet safety specifications such as UL 1459, isolation is needed between ultracapacitor and load. Therefore, bi-directional converter should have isolation capability.

A Dual Active Bridge (DAB) converter, which has high boost ratio and galvanic isolation capability, is chosen as ultracapacitor's front-end converter. However, its conventional Phase Shift Modulation (PSM) has limited low power transfer capability.

In past, modulation methods such as Trapezoidal Modulation (TZM) and Triangular Modulation (TRM) have been investigated in [8] and [9] to improve the system efficiency as well as to increase the range of input and output voltage that allows bi-directional power transfer. In TZM, in addition to vary the phase shift ϕ, the duty ratio D can also be changed to enable lower power transfer than PSM. However, using two variables poses challenges such as selection of a suitable control

combination for ϕ and D. Though, the phase shift and duty ratio are chosen as minimum, TZM still cannot meet the desired low power transfer requirements. TRM proposed in [8] is able to transfer lower power compared to both PSM and TZM. However it works under the condition when input voltage V_1 and output voltage refer to transformer primary side V_2/n are different. However, in the DAB design, transformer turns ratio n is usually selected as $n = V_2/V_1$, which means V_1 can equal to V_2/n. This arrangement minimizes the peak current rating for devices. To overcome above limitations, a hybrid modulation algorithm is proposed to widen the power transfer range.

This chapter is organized as follows: Section. 2.2 reviews the current bi-directional converters. Section. 2.3 describes the DAB operating principles and its parameters selection. Section. 2.4 investigates the limitations in conventional modulations. Section. 2.5 proposes a hybrid modulation scheme to widen the power transfer capability. Section. 2.6 documents and investigates the results. Finally, Section. 2.7 constitutes a summary of this chapter.

2.2 Literature review of bi-directional converter

Previously, buck-boost converter shown in Fig. 2.2 has been implemented [10, 11, 12, 13].

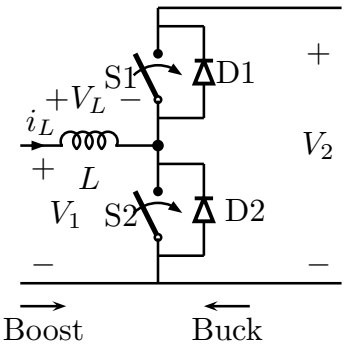


Figure 2.2: Buck boost Converter

Its key waveforms are shown in Fig. 2.3. In boost mode, when power is transferred from energy storage V_1 to the DC link V_2, lower switch S_2 is modulated (Fig. 2.3 (a)). On the other hand, when power is transferred from the DC link to energy storage, upper switch S_1 is modulated (Fig. 2.3 (b)).

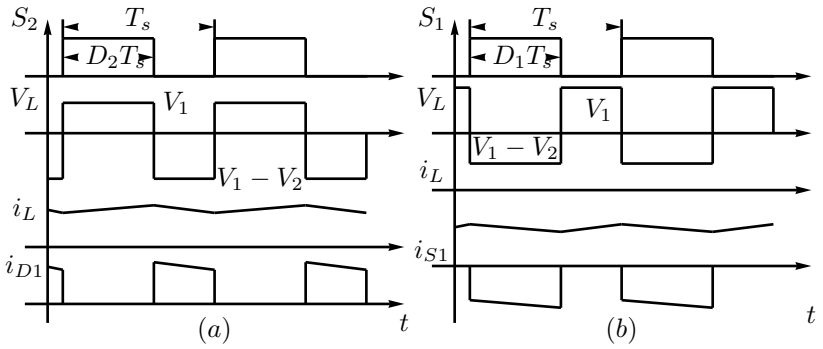


Figure 2.3: Key waveforms in buck boost converter

(a) Boost Mode (b) Buck mode

The relationship between V_1 and V_2 during buck and boost mode are expressed

in Eqn. (2.1) and Eqn. (2.2) respectively.

$$Buck : V_1 = D_1 \cdot V_2 \tag{2.1}$$

$$Boost : V_2 = \frac{1}{1 - D_2} \cdot V_1 \tag{2.2}$$

Buck boost converter is simple and efficient, the current i_L can flow from the high voltage DC link V_2 to the energy storage V_1 and vice-versa. In Eqn. (2.2), the output voltage V_2 is determined by the input voltage V_1 and the duty ratio D_2. However, in practice, there are parasitic resistances in the inductor. If equivalent series resistor R_L is taken into consideration and the load resistor is denoted as R. The relationship between the output voltage V_2 and input voltage V_1 becomes:

$$V_2 = \frac{1}{\frac{R_L}{R(1-D_2)} + 1 - D_2} \cdot V_1 \tag{2.3}$$

From this, the higher the ratio between the R_L and R, the lower the output voltage can be. In practice, voltage boost capability is limited up to 5 times of the input voltage under this case. As a result, buck boost converter has difficulties to achieve high voltage boost ratio.

For high voltage ratio applications, transformer coupled bi-directional converters have been proposed. Peng et.al. [14] [15] [16] [17] have proposed a half bridge dual active converter as Fig. 2.4.

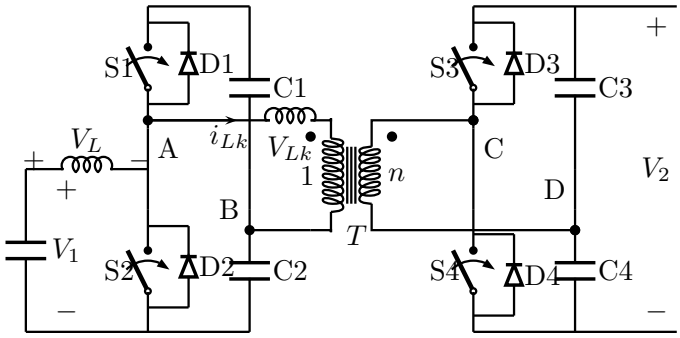


Figure 2.4: Half Bridge Dual Active Converter

Its key waveforms during the boost and buck mode are shown in Fig. 2.5.

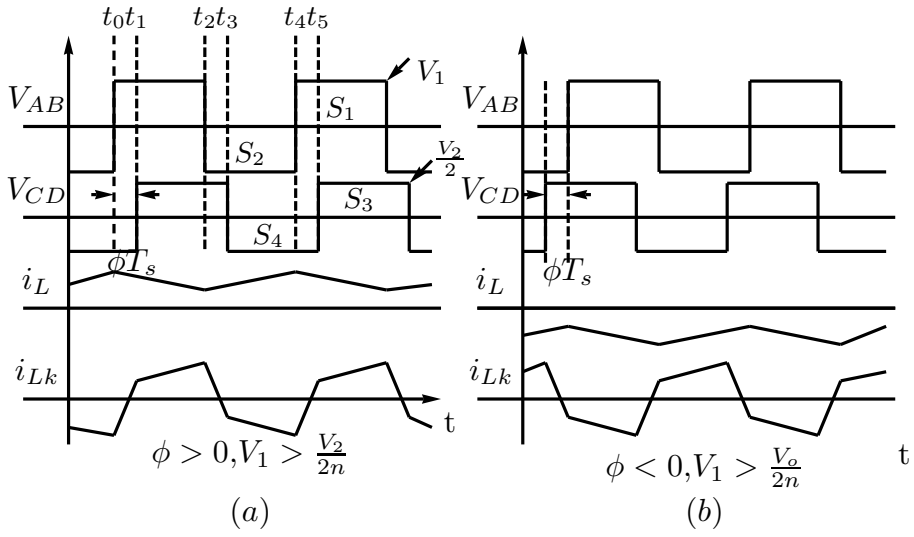


Figure 2.5: Waveforms of half bridge dual active converter

The output power varies by changing the relative phase shift between the primary side voltage V_{AB} and the secondary side voltage V_{CD}. However, the circuit requires higher numbers of passive component such as high frequency capacitors. These capacitors are required to ensure an equal voltage distribution across the

upper and lower switches of the half bridge. Besides that, higher current rating devices are needed for lower side switches on the low voltage side of the transformer.

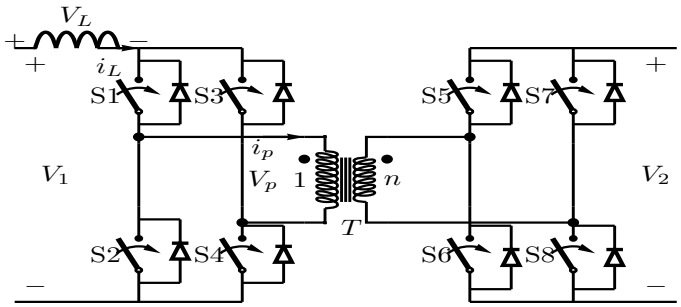


Figure 2.6: Current Fed Full Bridge Converter

Current-fed full bridge converter, shown in Fig. 2.6, has also been proposed in past [18] [19].

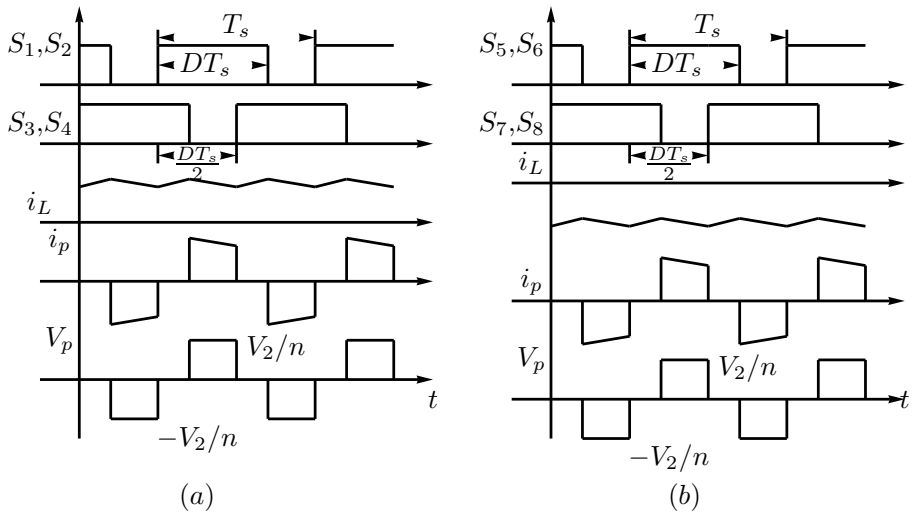


Figure 2.7: Key waveforms in the current-fed full bridge

Its key waveforms in boost and buck mode are shown as Fig. 2.7 (a),(b) respectively. The boost operation is achieved via modulating four switches in the

primary side while using secondary side switches as diode rectifier. Similarly, a buck mode is achieved when secondary side switches are modulated while primary side switches are used as diode rectifier. However, current-fed converter has severe performance limitations such as high transient voltage in switches. In addition, external circuit is needed to support its soft-start [19].

Dual Active Bridge Converter (DAB), as Fig. 2.8 shows, has high boost voltage ratio, easy bi-directional power flow control and galvanic isolation nature. Its full bridge topology allows DAB to be extended in high power application while transformer can boost input voltage more than 10 times. Thus it has attracted attention of many researchers[8][20][21][22][23]. In this thesis, DAB is chosen as a bi-directional converter for interfacing the energy storage and load.

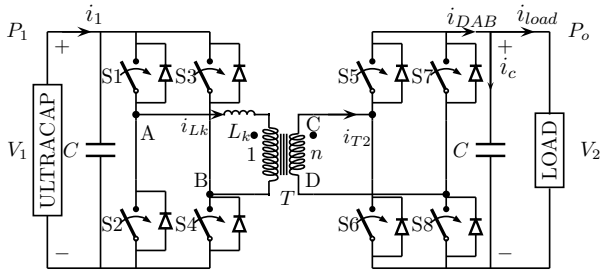


Figure 2.8: Topology of DAB converter

2.3 Conventional modulation in DAB

2.3.1 Operating principle of DAB

As Fig. 2.8 shows, DAB contains two full bridges and one transformer.

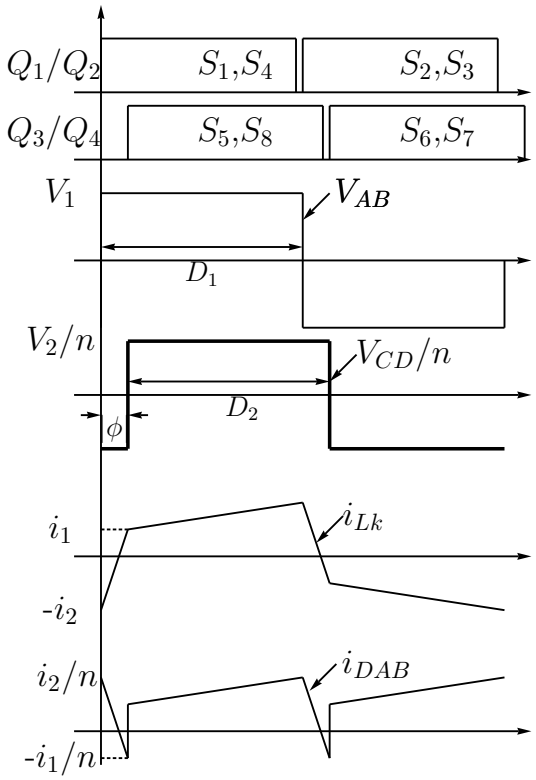


Figure 2.9: Waveforms of PSM under positive power transfer

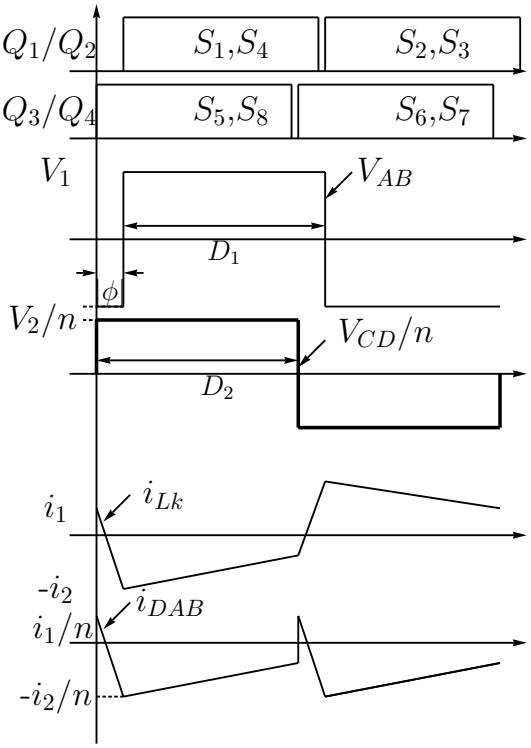


Figure 2.10: Waveforms of PSM under negative power transfer

Conventional Phase Shift Modulation (PSM), which is proposed in [24], is shown as Fig. 2.9. By changing the phase between the transformer primary side voltage V_{AB} and secondary side voltage V_{CD}, the power flow can be controlled. When power is transferred from ultracapacitor side V_1 to load side V_2 (Fig. 2.8),

we call it positive power transfer. On the contrary, negative power transfer is defined when power flows from V_2 to V_1 side. Here, Fig. 2.9 and Fig. 2.10 show key waveforms under positive power and negative power transfer respectively. In Fig. 2.9 and 2.10, the thick lines represent the secondary voltage V_{CD} referred to the primary side. D_1 and D_2 are duty ratios that represent the duration for which V_1 and V_2 are applied to transformer primary and secondary respectively. For PSM, $D_1 = D_2 = 0.5$. This modulation method is simple to be implemented and has higher power transfer capability.

2.3.2 Average output current in DAB

In this section, the relationship between the output current and its phase shift under PSM modulation is investigated. The derivation is based on Fig. 2.11 when phase shift is positive. The voltage across the leakage inductance within one switching period are shown in Fig. 2.12.

According to Fig. 2.11 and Fig. 2.12, current flow in the leakage inductance i_{Lk} at any time instant t can be written as:

$$\begin{aligned}
Interval[t_0, t_1] : i_{Lk}(t) &= -I_2 + \frac{1}{L_k}(V_1 + V_2/n)(t - t_0) \\
Interval[t_1, t_2] : i_{Lk}(t) &= I_1 + \frac{1}{L_k}(V_1 - V_2/n)(t - t_1) \\
Interval[t_2, t_3] : i_{Lk}(t) &= I_2 - \frac{1}{L_k}(V_1 + V_2/n)(t - t_2) \\
Interval[t_3, t_4] : i_{Lk}(t) &= -I_1 - \frac{1}{L_k}(V_1 - V_2/n)(t - t_3)
\end{aligned} \tag{2.4}$$

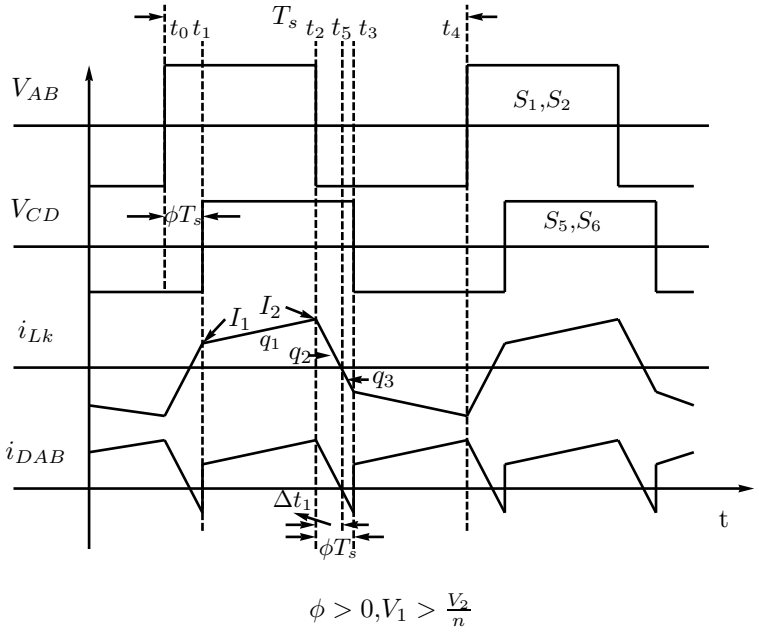


Figure 2.11: Key waveforms in Dual Active Bridge Converter

where L_k is leakage inductance and n is transformer turns ratio. I_1 and I_2 are currents at $t = t_1$ and $t = t_2$ respectively as shown in Fig. 2.11.

If $\tilde{I}_{13}$ is assigned as average current flowing in primary leakage inductance during the period t_1 to t_3, then the average output current from DAB $\tilde{I}_{DAB}$ can be represented as $\tilde{I}_{DAB} = \frac{\tilde{I}_{13}}{n}$. Hence, $\tilde{I}_{13}$ has to be calculated first.

The average current flowing in leakage inductance between t_1 to t_3 can be calculated as:

$$\tilde{I}_{13} = \frac{(q_1 + q_2 + q_3)}{0.5T_s} \tag{2.5}$$

where q_1,q_2 and q_3 are charges with respect to time within interval $[t_1, t_2]$, $[t_2, t_5]$

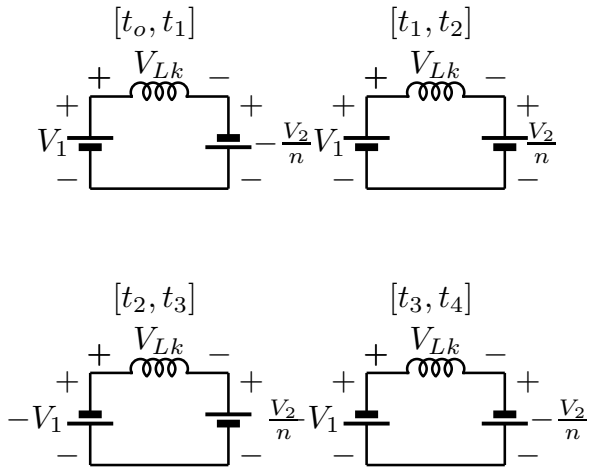


Figure 2.12: Equivalent circuit during interval [t_0,t_4]

and $[t_5, t_3]$, and can be expressed as:

$$\begin{aligned} q_1 &= \frac{1}{2}(I_1 + I_2)(0.5 - \phi)T_s \\ q_2 &= \frac{1}{2}(0 + I_2)\Delta t_1 \\ q_3 &= -\frac{1}{2}(0 + I_1)(\phi T_s - \Delta t_1) \end{aligned} \tag{2.6}$$

where Δt_1 could be calculated as: at time instant t_5

$$\begin{aligned} \because 0 &= I_2 - \frac{1}{L_k}(V_1 + V_2/n)\Delta t_1 \\ \therefore \Delta t_1 &= \frac{I_2 L_k}{(V_1 + V_2/n)} \end{aligned} \tag{2.7}$$

by knowing this, at time instant t_2

$$I_2 = I_1 + \frac{1}{L_k}(V_1 - V_2/n)(0.5 - \phi)T_s \tag{2.8}$$

and at time instant t_3

$$-I_1 = I_2 - \frac{1}{L_k}(V_1 + V_2/n)\phi T_s \tag{2.9}$$

based on equation(2.8) and (2.9), I_1 and I_2 can be represented as,

$$\begin{aligned} I_1 &= \frac{V_1 T_s}{2L_k}(2\phi - 0.5) + \frac{V_2}{4nL_k}T_s \\ I_2 &= \frac{V_1 T_s}{4L_k} + \frac{V_2 T_s}{nL_k}(\phi - 1/4) \end{aligned} \tag{2.10}$$

from (2.5) to (2.10), $\tilde{I}_{13}$ could be expressed as:

$$\tilde{I}_{13} = \frac{(1-2\phi)\phi V_1 T_s}{L_k} \tag{2.11}$$

Therefore, according to $\tilde{I}_{DAB} = \frac{\tilde{I}_{13}}{n}$, average output current $\tilde{I}_{DAB}$ is shown as:

$$\tilde{I}_{DAB} = \frac{(1-2\phi)\phi V_1 T_s}{nL_k} \tag{2.12}$$

Applying $f_s = \frac{1}{T_s}$ and rearranging Eqn. (2.12), average current of the DAB can be represented as

$$\tilde{I}_{DAB} = \frac{V_1}{2L_k f_s n} 2\phi(1-2\phi) \tag{2.13}$$

Till now, the average output current from DAB when phase shift is positive is derived. The same derivation steps could be applied to get the average output from

DAB when phase shift is negative. Eqn. 2.14 represents the relationship between output current and phase shift under both positive and negative power transfer

$$\tilde{I}_{DAB} = \frac{V_1}{2L_k f_s n} 2\phi(1 - 2|\phi|) \tag{2.14}$$

When output voltage is V_2, the output power transfer can be represented by Eqn. (2.15),

$$P_o^{PSM} = V_1 \frac{V_2 2\phi(1 - 2|\phi|)}{2L_k f_s n} \tag{2.15}$$

2.3.3 Parameters selection for DAB design

In order to transfer desired power under constraints from input/output voltage and phase shift range, converter parameters such as transformer turns ratio n, leakage inductance L_k and switching frequency f_s should be properly chosen. In following paragraphs, parameters' selection guidelines are discussed.

First, the input and output requirements are specified in the following paragraphs. In the lab, Maxwell 48V/110F ultracapacitor is used. Its terminal voltage is designed to vary between 28V to 45V such that 65% of energy which is stored in ultracapacitor can be utilized. Under this arrangement, ultracapacitor can continuously supply 1.5 kW power for 45 seconds when its voltage drops from 45V to 28V. Converter power rating is selected as 1500W and DC bus voltage is selected to be 400V. This DC bus can power up 3 phase 120V DC-AC converter.

Second, the practical phase shift is discussed here. As described in Ref. [21], the relationship between the Power Factor(PF) and phase shift is shown as Eqn.(2.16), where phase shift ϕ is in p.u. and 360^o is 1 p.u.

$$PF = 1 - 0.5\phi\sqrt{\frac{3}{3-\phi}} \tag{2.16}$$

The relationship can be represented as Fig. 2.13. From the figure, the larger the phase shift, the lower the power factor. Therefore, high phase shift is not desirable. It will cause low power factor which introduces large reactive power transfer in transformer. It further causes extra losses within circuit.

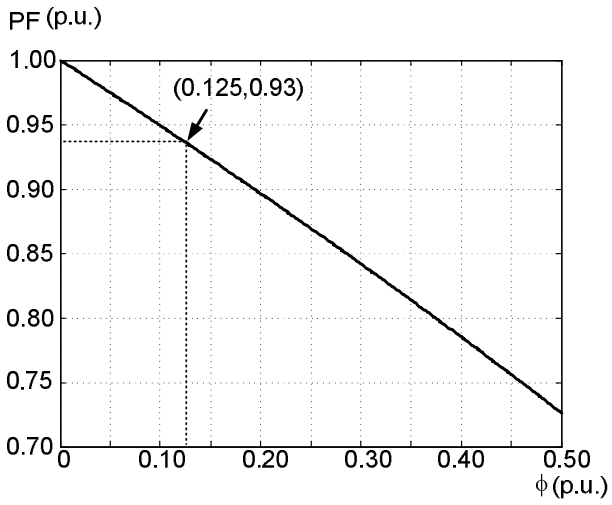


Figure 2.13: Relationship between the power factor and phase shift

Based on Eqn.(2.15), Fig. 2.14 shows relationship between output power and phase shift under various leakage inductance. Similarly, as Fig. 2.14 shows, to get

the same output power, high phase shift requires large leakage inductance which again introduces large reactive power within transformer.

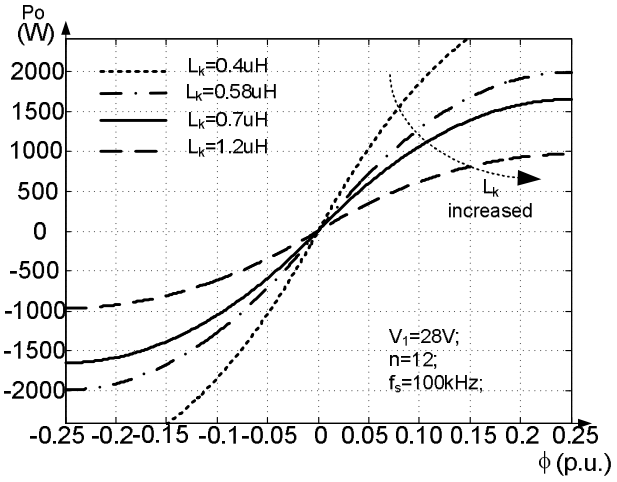


Figure 2.14: Relationship between power and phase shift under various leakage inductance

On the other hand, the low phase shift needs low leakage inductance to transfer the same amount of power. However the size of the leakage inductance, though can be minimized, is still limited by physical winding of the transformer. Based on above descriptions, the selection of the phase shift is a trade off process. In the thesis, maximum phase shift is selected to be 0.125 p.u. such that PF can always be above 0.93 as well as the leakage inductance can be designed properly.

At the same time, minimum phase shift is selected as 0.03 p.u. This value arises from finite switching times and the finite rate of change of transformer voltage. A phase shift smaller than this can cause substantial overlap periods, whereby the transformer voltage V_{AB} and secondary voltage V_{CD} may be rising/falling. During this period, the exact amount of energy transfer cannot be easily determined.

Such practical conditions determine the minimum phase shift.

At the same time, the minimum phase shift is limited by finite switching time of switches. The finite switching time of switches causes finite rate of change of transformer voltage. In ideal case, primary and secondary voltages across the transformer are shown in Fig. 2.14 (a)

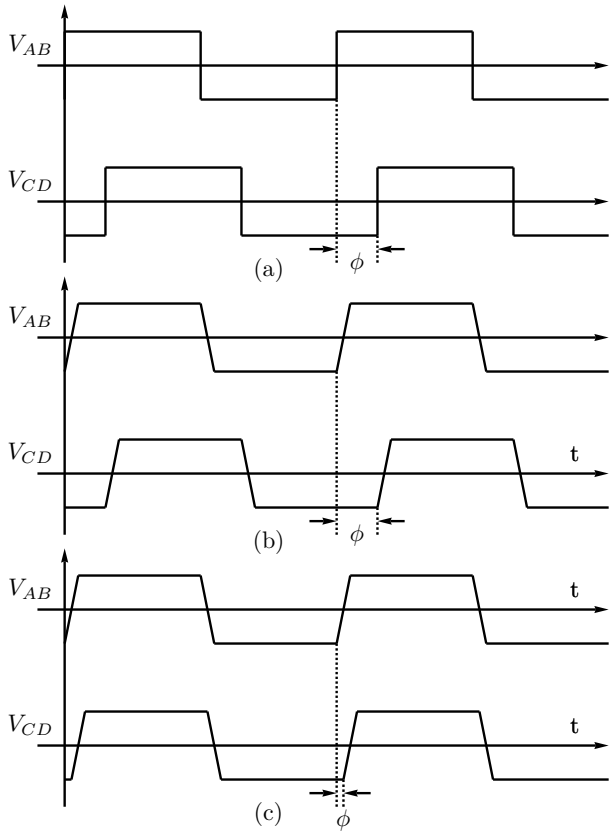


Figure 2.15: Voltage across transformer under (a)Ideal case (b) Practical case with large ϕ (c) Practical case with small ϕ

In practice, due to finite rise time, primary and secondary voltages across the transformer are shown in Fig. 2.14 (b).

When phase shift is large enough, effect of rise time in transformer voltage

on power transfer can be neglected. However, when phase shift reduces to the value comparable to transformer voltage rise time (as shown in Fig. 2.14 (c)), the relationship between phase shift and power output in Eqn. 2.15 is no longer valid. In addition, the output power is sensitive to phase shift variation. For instance, when V_1=45V, ϕ=0.03 p.u results 729W output power variation. In this thesis, minimum phase shift is chosen as 0.03 p.u based on the rise time of the transformer voltage.

Till now, all the input and output requirements and practical phase shift range are discussed. Now, let us have a look on DAB converter parameters selection.

The turns ratio of transformer should be selected such that V_1 and V_2/n can be as close as possible. The reason to choose V_1 and V_2/n as close as possible is that the large differences in $(V_1 - V_2/n)$ causes large Δi in interval 2 as shown in Fig. 2.16. For instance, Δi_2 in Fig. 2.16 (b) is larger compared to Δi_1 in Fig. 2.16 (a). As a result, higher peak current appears in devices which in turn increases device current rating.

Regarding the switching frequency, for high switching frequency, magnetic and capacitor size can be reduced but it increases high switching loss. Here, 100kHz is chosen for this lab demo setup.

Further, the leakage inductance is determined when minimum input voltage

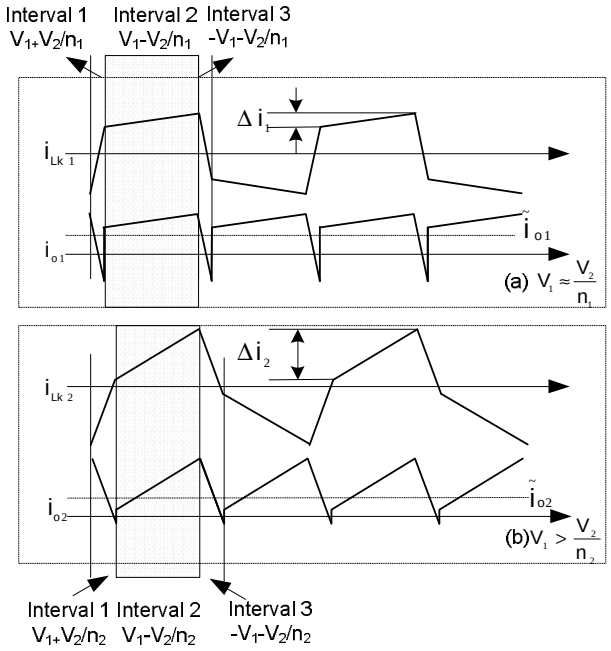


Figure 2.16: Peak current under different turns ratio

is chosen as 28V and maximum phase shift as maximum 0.125 p.u. ,that is

$$L_k = V_{1min}\frac{V_2 2\phi_{max}(1-2|\phi_{max}|)}{2P_{omax}f_s n} \tag{2.17}$$

Based on above equation and inserting V_{1min}=28V, V_2=400V, ϕ_{max}=0.125 p.u., P_o=1500W, f_s=100kHz and n=12, the L_k is calculated as 0.58μH.

2.4 Limitations of conventional modulations

As explained in the introduction, DAB is introduced to interface the energy storage to support renewable energy intermittency. Fig. 2.17 shows the simple block diagram of energy storage augmented renewable energy system while Fig. 2.18

shows one of the desired power profile for renewable energy, load and ultracapacitor respectively. In both Fig. 2.17 and Fig. 2.18, P_{RES}, P_{CAP} and P_{LOA} represent power from renewable source, power from ultracapacitor and power flow in the load respectively. From shaded area in Fig. 2.18, it shows that a wide range of power is needed from ultracapacitor which equivalently requires that the bi-directional converter can transfer the power in a wide range under varying voltage.

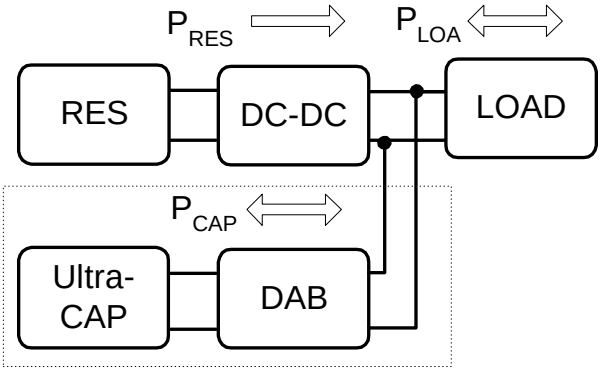


Figure 2.17: Block diagram of energy storage augmented renewable source system

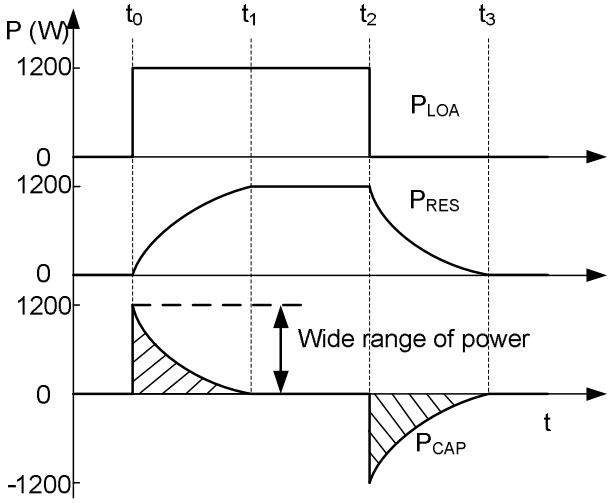


Figure 2.18: Desired power range of energy storage system

In the design, a low minimum power such as 200W is chosen so that it enables the ultracapacitor system to compensate the power differences between the main

source and load faster to achieve better performances. However, too low minimum power will cause the converter to always operate in the low efficiency range and will cause the converter to connect and disconnect from main system frequently. In addition, as small variation in phase shift results in large variation in power transfer around the zero power region, it is hard to control the power transfer accurately in extremely low power area. Therefore, the target power transfer range is limited between 200W - 1200W. Based on above descriptions, the desired power range is shown as rectangular in Fig. 2.19.

Under conventional phase shift modulation (PSM) and above described parameters, the power transfer capability of DAB converter is shown as shaded area in Fig. 2.19.

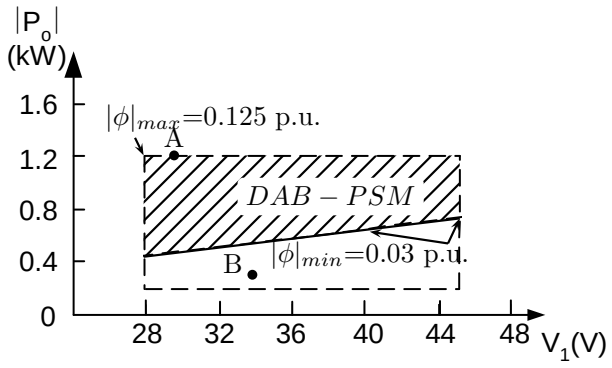


Figure 2.19: Desirable output power P_o vs input voltage V_1

From Fig. 2.19, at maximum input voltage of 45V the least power that can be transferred is only 58.33% of $P_{max} = 1200W$. The limitation of minimum power transfer capability also poses a voltage regulation problem. This can be explained

using Fig. 2.20, here the load current demand changes from 3A to 1A at time instant of 30ms, the voltage V_2 is no longer regulated.

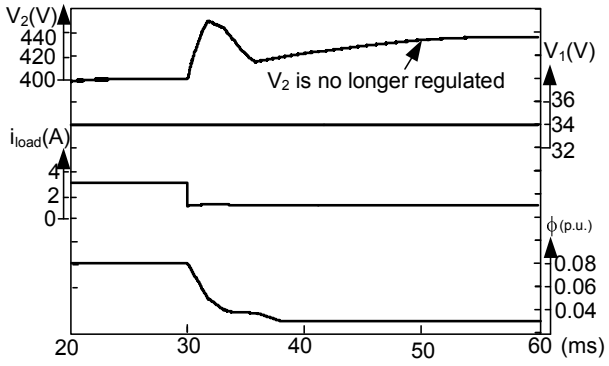


Figure 2.20: Simulation when positive power transfer operate under phase shift alone

This is because the desired operating point, point B shown in Fig. 2.19, cannot be achieved if phase shift modulation is used. Therefore the converter is operating under minimum power transfer condition along the lower boundary of the shaded quadrilateral shown in Fig. 2.19. At the same time, controller output is limited in the minimum phase shift. This means that controller is no longer effective. As a result, V_2 can no longer be regulated. This simulation shows that DAB converter is not able to achieve regulated transfer of lower power under PSM alone. Hence this will increase the power level threshold at which the ultracapacitor is operational in the energy transfer, restricting its operational range for energy transfer.

To extend DAB power transfer capability in low power range, several existing modulation schemes are investigated.

2.4.1 Trapezoidal modulation (TZM)

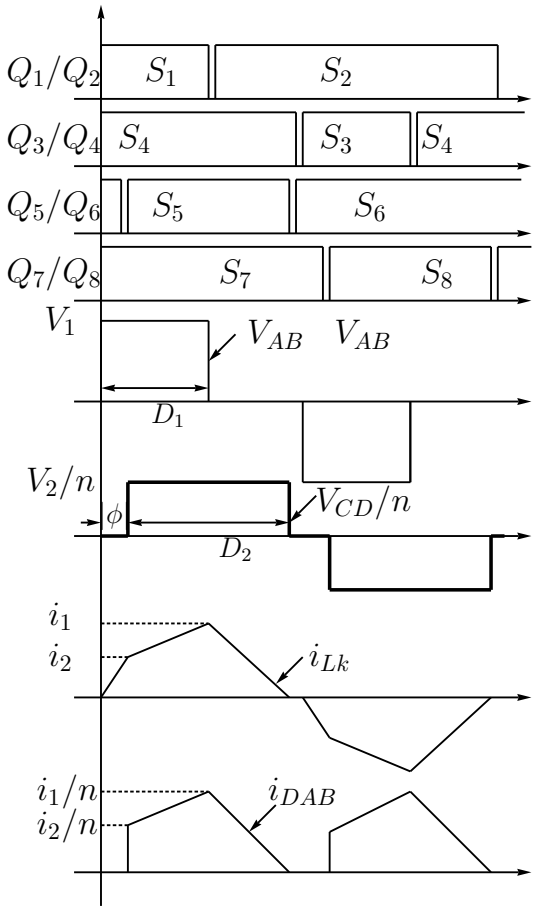


Figure 2.21: TZM under positive power transfer

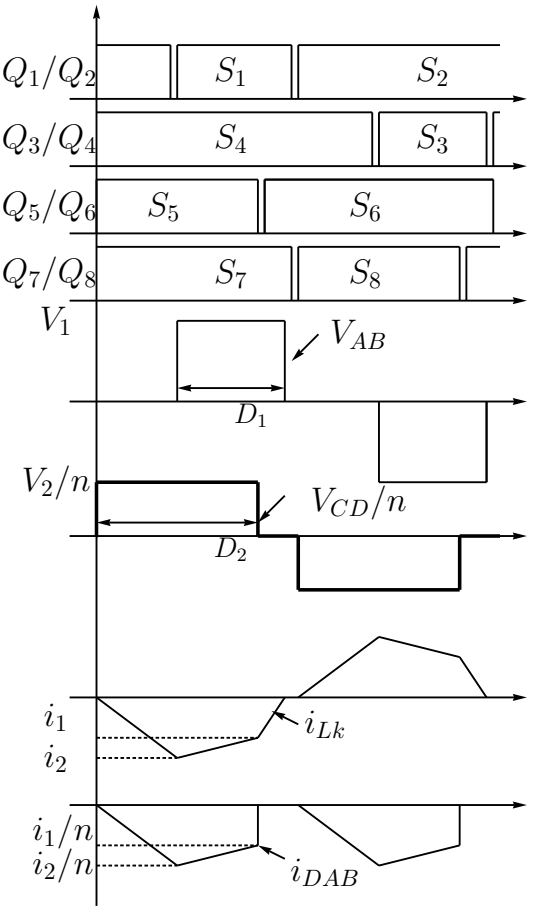


Figure 2.22: TZM under negative power transfer

Modulation methods such as trapezoidal modulation (TZM) and triangular modulation (TRM) are investigated in [8] and [25] respectively. The key waveform of TZM is shown as Fig. 2.21 and Fig. 2.22. Unlike fixed duty ratio $D_1 = D_2 = 0.5$ in PSM (Fig. 2.9), D_1 and D_2 in TZM (Fig. 2.21) can be different and less than 0.5. In Fig. 2.21 and Fig. 2.22, Q_1 to Q_8 are gating signals for switches S_1 to S_8 respectively. Gating signals for switches in the same leg, for instance, S_1 and S_2

are generated complementary with a dead time. Input voltage V_1 is connected to the primary side transformer for time D_1T_s while output voltage V_2 is connected to secondary side transformer for time D_2T_s. Based on this condition, power transfer equation under TZM can be described as

$$P_o^{TZM} = \frac{V_1}{L_k f_s}(D_1^2 V_1 - (D_1 - \phi)^2 V_2/n) \tag{2.18a}$$

$$D_2 = \frac{V_1}{V_2/n} D_1 \tag{2.18b}$$

2.4.2 Triangular modulation (TRM)

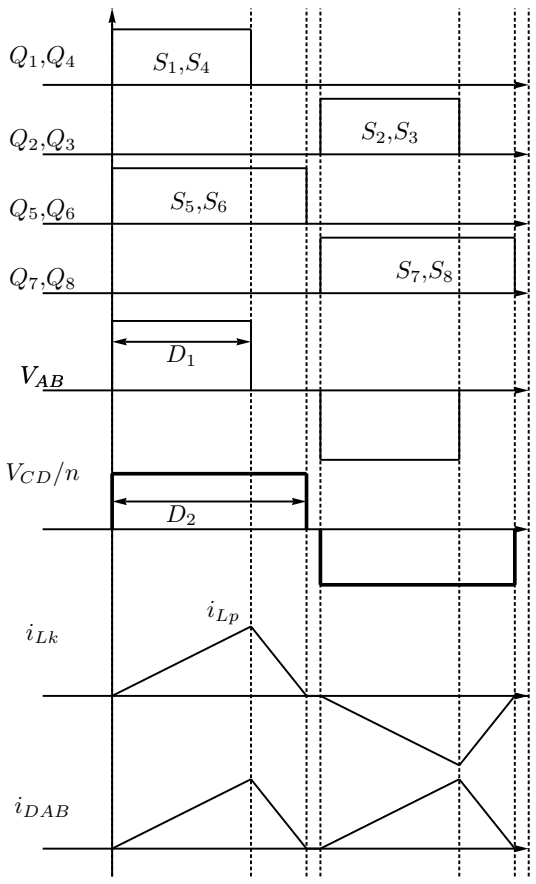


Figure 2.23: TRM under positive power transfer

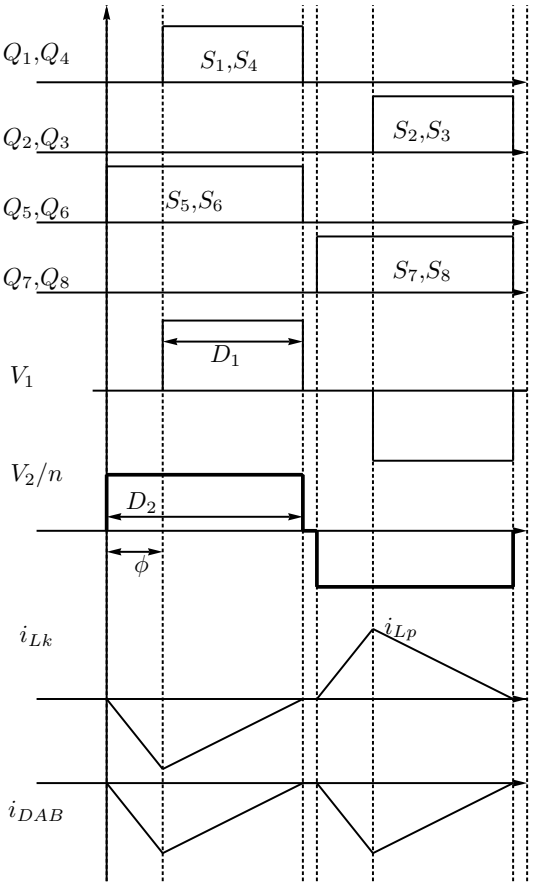


Figure 2.24: TRM under negative power transfer

TRM described in [25] is also explained through Fig. 2.23 and Fig. 2.24. With respect to TZM, TRM can be considered as a special case of TZM when $\phi = 0$. The power transfer equation under TRM is given as

$$P_o^{TRM} = \frac{V_1}{L_k f_s}(D_1^2 V_1 - (D_1)^2 V_2/n) \tag{2.19a}$$

$$D_2 = \frac{V_1}{V_2/n} D_1 \tag{2.19b}$$

By inserting the maximum phase shift $\phi_{max} = 0.125 p.u.$ for PSM in Eqn. (2.15) and duty ratio $D_1^{max} = 0.21 p.u.$ for TZM and TRM in Eqn. (2.18a) and (2.19a), the maximum power transfer capabilities under three modulations have following relationship $P_{max}^{TRM} < P_{max}^{TZM} < P_{max}^{PSM}$.

Though TZM is able to transfer lower power than PSM, its minimum power transfer capability is still limited. Fig. 2.25 shows the relationship between output power and duty ratio when minimum phase shift is chosen as 0.03 p.u. From Fig. 2.25, when 45V voltage is applied, TZM minimum power is limited at 21% which is still higher than our design requirements 16.67%, which is 200W out of 1200W.

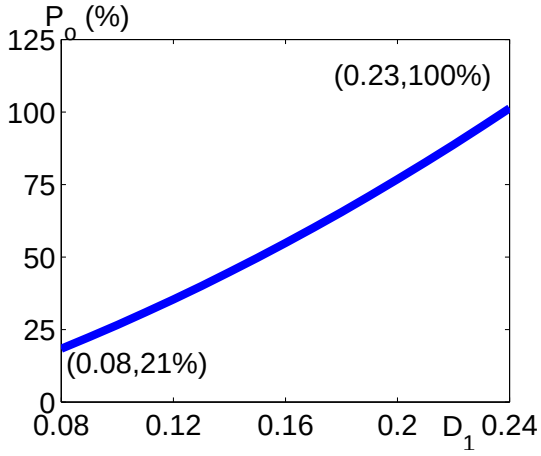


Figure 2.25: Limitation of the TZM modulation

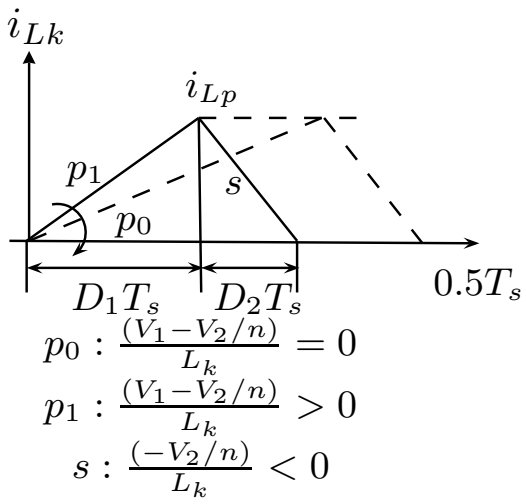
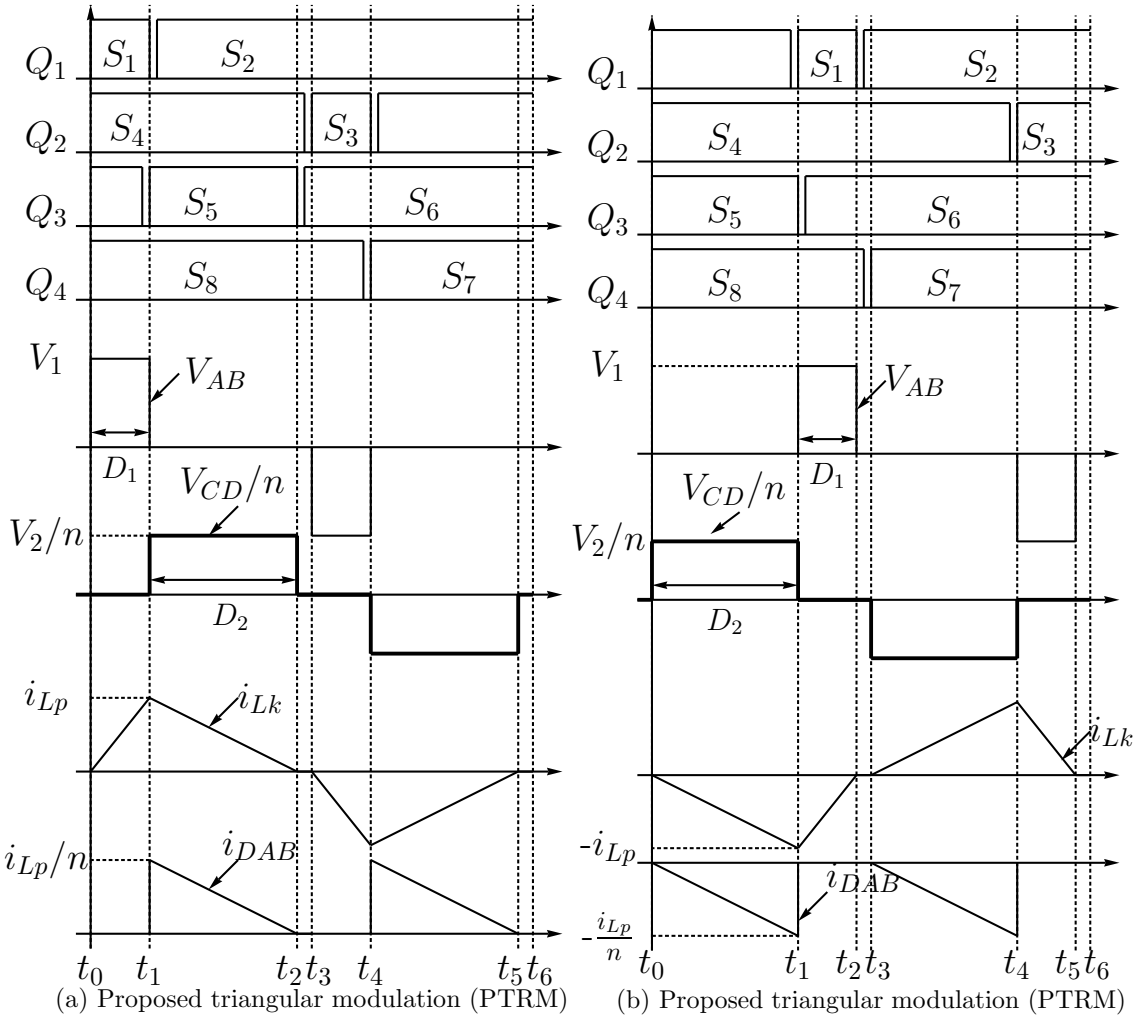


Figure 2.26: Limitation of the TRM modulation

TRM [25] cannot work when $V_1 = V_2/n$. Due to the waveform symmetry, only leakage inductance current within the first half cycle is shown in Fig. 2.26. According to Fig. 2.26, within D_1T_s interval, the voltage across the leakage inductance is $(V_1 - V_2/n)$, this means i_{Lk} increases with a slope of $(V_1 - V_2/n)/L_k$. On the other hand, during D_2T_s interval, i_{Lk} decreases with a slope of $-V_2/L_k$. If $(V_1 - V_2/n)$

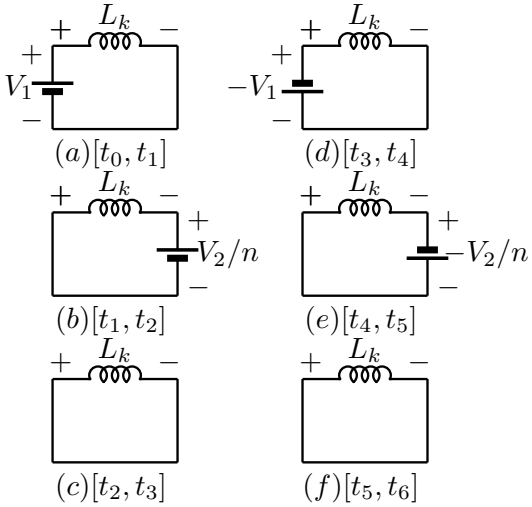
reduces to zero, the positive rate of change of current is equal to zero and hence there would be no increase in i_{Lk} during D_1T_s. In practise, transformer turns ratio n is designed as close as V_2/V_1 to ensure lowest peak current as described before. Based on this, TRM cannot be used to extend the power transfer range in practical DAB.

2.5 Hybrid modulation widen power transfer



(a) Proposed triangular modulation (PTRM) under positive power transfer

(b) Proposed triangular modulation (PTRM) under negative power transfer



(c) Equivalent circuit of PTRM under positive power transfer

Figure 2.27: Key waveforms of proposed triangular modulation (PTRM)

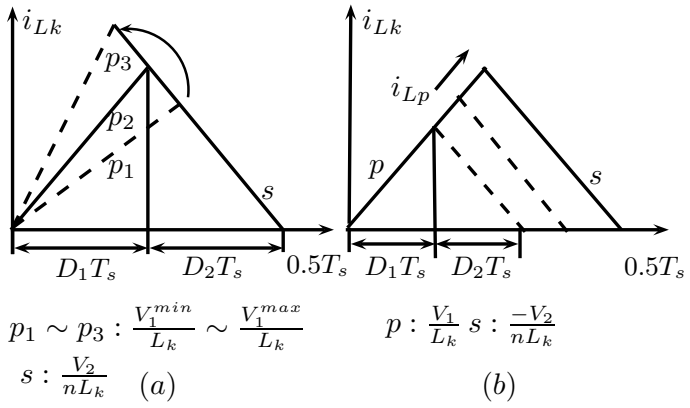


Figure 2.28: Waveforms of proposed triangular modulation

In order to achieve lower power transfer in DAB, another novel triangular modulation shown in Fig. 2.27 is proposed in this chapter. Fig. 2.27 (a),(b) are transformer waveforms when positive and negative power transfer occur under Proposed Triangular Modulation (PRTM) respectively.

As defined earlier, positive power occurs when power is transferred from V_1 to V_2 side and the thick line represents V_{CD}/n. The corresponding equivalent circuit for positive power transfer is shown in Fig. 2.27 (c). Unlike TRM mentioned before, this proposed triangular modulation is suitable when magnitude V_1 and V_2/n are close. In the proposed method, the voltage across leakage inductance is either V_1 or V_2/n. Fig. 2.28 (a) shows the leakage current waveform within half cycle. When input voltage changes from V_1^{min} to V_1^{max}, the leakage inductance current waveform changes from p_1 to p_3, refer Fig. 2.28 (a). The necessary value of D_1 is achievable within this range. Under this modulation, the output power can be controlled by

varying D_1. Fig. 2.28 (b) shows, under the same input voltage, the peak current i_{Lp} increases as D_1 increases. The peak current flow in the primary leakage inductance can be derived based on Ldi/dt

$$L_k \frac{i_{Lp} - 0}{D_1 T_s} = V_1 \ldots \text{for } D_1 T_s \tag{2.20a}$$

$$L_k \frac{0 - i_{Lp}}{D_2 T_s} = -V_2/n \ldots \text{for } D_2 T_s \tag{2.20b}$$

Based on above equations, the relationship between the amount of the power to be transferred and the duty ratio D_1 can be derived as

$$P_o^{PTRM} = V_1^2 \frac{D_1^2}{L_k f_s} \tag{2.21}$$

From Eqn. (2.21), minimum output power is achieved when D_1 is minimum. Similar as minimum phase shift limitation, D_1 is also limited by finite rise and fall time in the switch. Therefore D_1 is chosen as 0.03p.u x2 =0.06 p.u.. Inserting D_1=0.06 p.u. and V_1=45V in Eqn. (2.21), the minimum power is less than 200W. Compared to PSM modulation, PTRM is able to transfer desired low power.

As $D_1 + D_2 < 0.5$, the maximum power that can be transferred under PTRM is

$$P_{omax}^{PTRM} = \frac{V_1^2 (V_2/n)^2}{4 L_k f_s (V_1 + V_2/n)^2} \tag{2.22}$$

Fig. 2.29 demonstrate the relationship between output power P_o and duty ratio D_1 under various V_1 by using PTRM scheme.

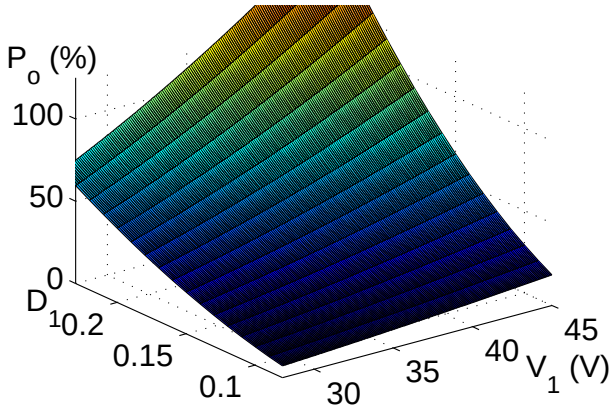


Figure 2.29: Relationship between P_o and V_1 under PTRM

Determining the maximum power transfer capability of PTRM, it is found that PTRM is also able to operate at high power transfer range that is achieved using PSM. However, compared with PSM, when the same output power is transferred, the triangular shape of current in PTRM introduces higher peak current both in transformer and the switches. This will increase the copper losses in transformer and the conduction losses in switches. Hence PTRM is not suitable for high power transfer. In this chapter, the proposed PTRM is used solely for lower power transfer. Based on above discussion, a combination of phase shift and novel triangular modulation is able to transfer desired power under wide range.

Fig. 2.30 shows the phase shift modulation works in higher power range while proposed triangular modulation functions in lower power range.

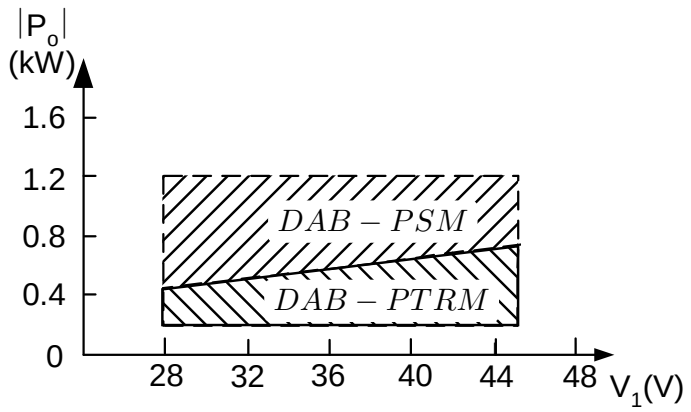


Figure 2.30: Hybrid modulation to achieve the desirable output power

2.6 Experimental results

The controller is implemented in dSPACE 1104 platform and the gating signals are generated by Opal Kelly XEM3010 FPGA board. The block diagram for controller platform is shown in Fig. 2.31.

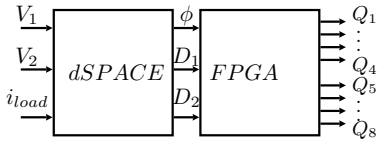


Figure 2.31: Schematic of hardware implementation

As shown in Fig. 2.31, the control variables ϕ, D_1 and D_2 are generated by dSPACE. The gating signal Q_1 to Q_8 are generated by FPGA. In the implementation, there are 8 bits allocated for ϕ and within those 8 bits, 1 bit is reserved

for the sign of phase shift. In addition, the full scale range ($7F(Hex)$)for phase shift is chosen as 90^o. Hence the phase resolution is 0.7^o(1bit). For duty ratio D_1 and D_2, the full scale range is chosen to be $0.5(=3F(Hex))$ as 6 bits are utilized to represent it. This gives a resolution of $0.0008(=1\text{bit})$. Table. 2.1 lists numerical parameters for DAB.

Table 2.1: Numerical parameters

Switching frequency	Sampling frequency	Filter cutoff frequency	Proportional gain K_c	Integral time T_i
100kHz	10kHz	3.3kHz	0.0176	0.0022

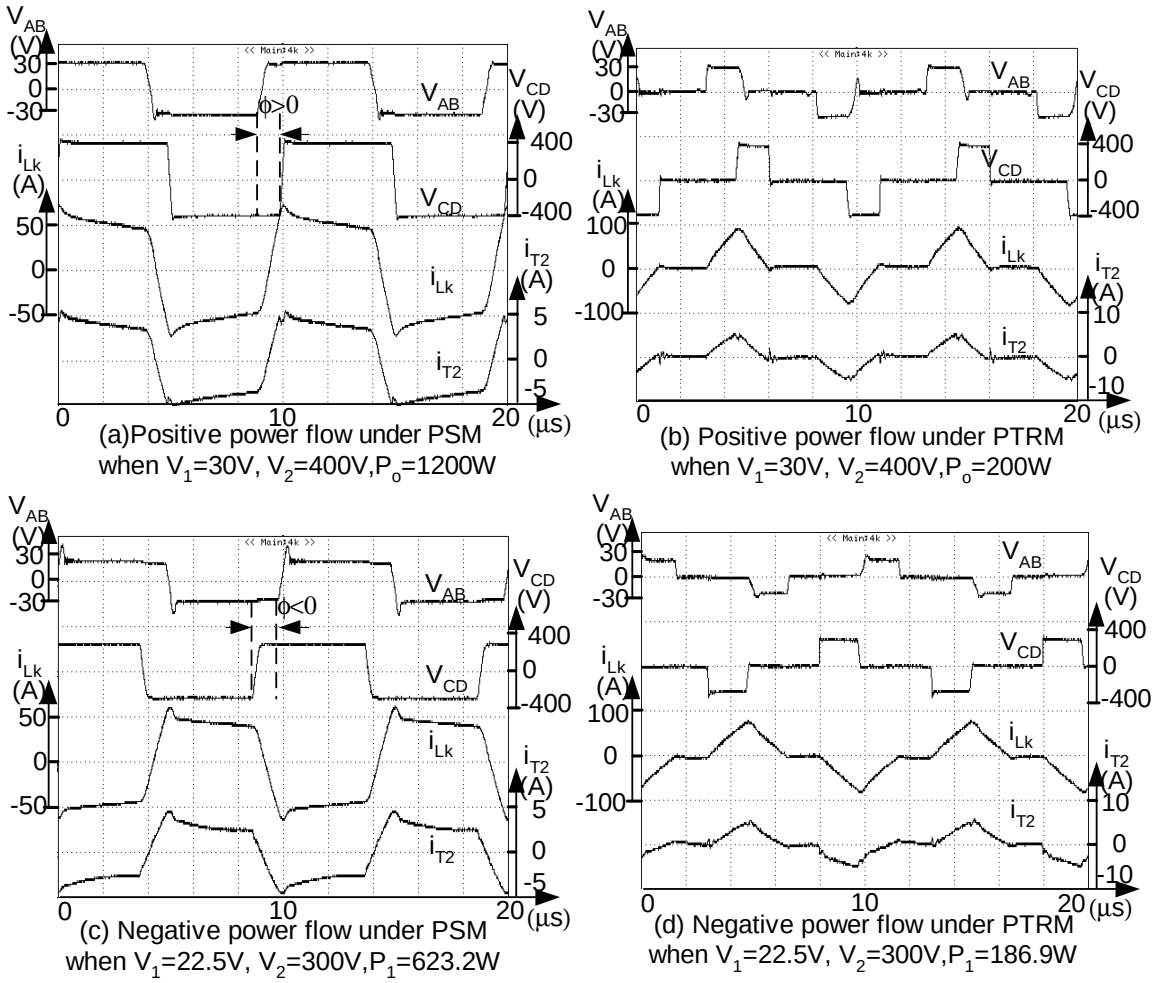


Figure 2.32: Transformer waveforms

Fig. 2.32 shows transformer current and voltage waveforms under phase shift modulation. Fig. 2.32 (a)(c) shows the phase shift modulation under positive power transfer and negative power transfer respectively. As described previously, when V_{AB} is leading the V_{CD}, a positive power transferred from V_1 side to V_2 side.

Fig. 2.32(b),(d) are the proposed triangular modulation waveforms under positive and negative power transfer. Above figures verify the two modulation

schemes used in this thesis.

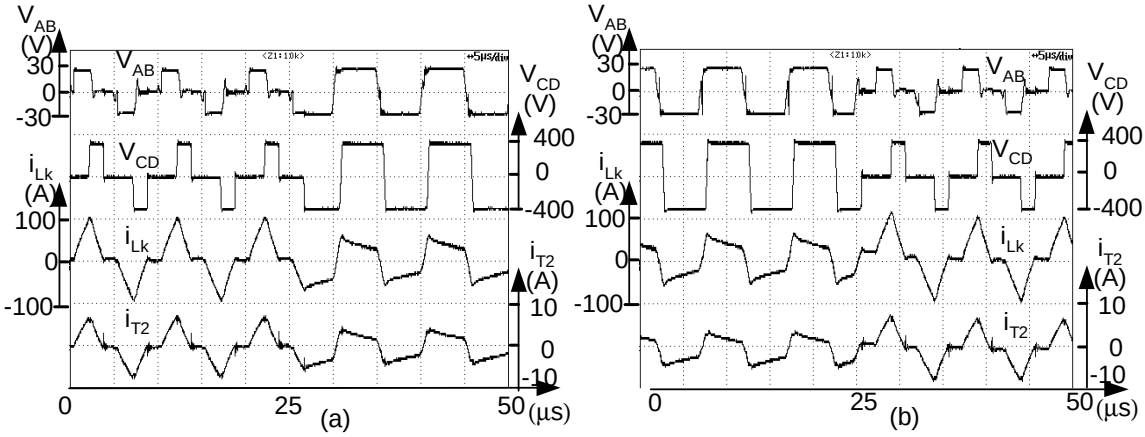


Figure 2.33: Transformer waveforms when power changes between 300W and 900W

Fig. 2.33 records the transformer waveforms for transition between two modes of control viz. PSM and PTRM. This further confirms the proposed controller with the hybrid modulation functions well during transition.

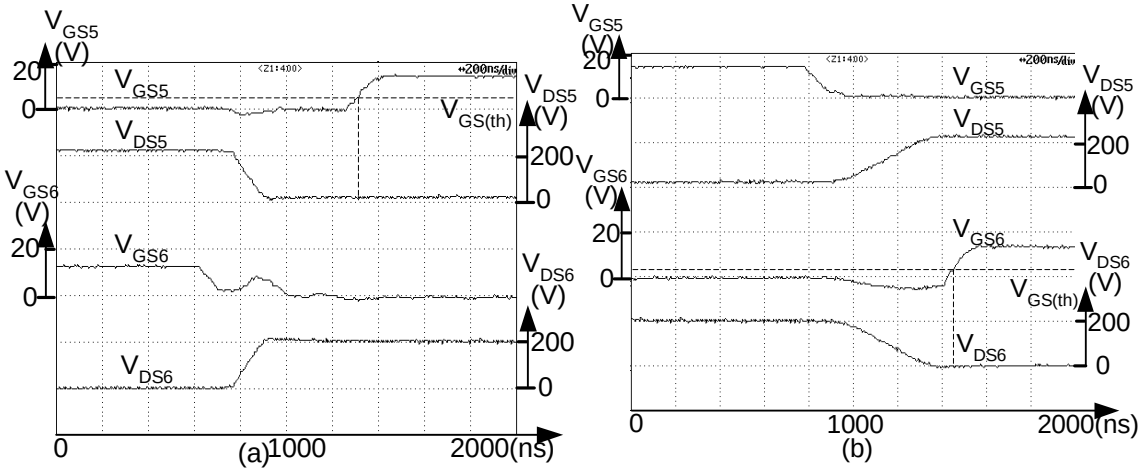


Figure 2.34: Zero voltage switching (a) S5 ZVS turn on (b) S6 ZVS turn on

In addition, soft switching technique such as zero voltage switching (ZVS) is implemented to achieve higher efficiency [26]. Fig. 2.34 (a)(b) show S_5 and S_6 are

turned on at ZVS when load is 900W respectively. It is also applicable for S_7 and S_8 due to the symmetry of the circuit.

2.7 Conclusions

Dual Active Bridge (DAB) converter appears very attractive in the application as interface converter for ultracapacitor in high power range. It is capable of achieving bi-directional power flow as well as high voltage boost capability and isolation between energy storage and load side. However, conventional phase shift modulation has limitation that it cannot transfer power at a lower range. A proposed triangular modulation scheme is implemented to extend the power range down to 200W. This hybrid modulation scheme enables an increase in the operational power range from 100% to 16.67% instead of 100% to 58.33%, almost a 100% increase in power transfer range.

Chapter 3

Feedback linearization for DAB

3.1 Introduction

In previous chapter, a hybrid modulation scheme is proposed to widen the power transfer range in DAB. Since the DAB output voltage has to be regulated in case of load and source variation, in this chapter, a proper controller is proposed.

As discussed before, source voltage and load power both have wide variation. Controller has to function well under wide operating range. In addition, nonlinear relationship between control variable and output poses extra difficulties in controller design.

In [27], a PI controller is designed based on linearized model of the half bridge dual active converter. The same approach can be adopted for DAB. This controller can achieve voltage regulation at designed operating point. However, if the operating point changes, the performance of converter can be sluggish and the system may be unstable.

In [28], an innovative average model is derived and a cascaded controller is designed for linearized model. However, the use of half cycle leakage inductance current as state variable needs extra processing block and the measurement of the leakage inductance current also requires an extra high bandwidth current sensor.

In [25], a controller including a predictive phase shift block is used. Hence a fast dynamic response is expected. However, it has the same limitation that only one operating point is considered.

For the DAB converter to work with wide range operating points, a suitable controller is required that is not just optimized for a linearized system at a fixed operating point. In this chapter, a feedback linearization approach with a linear controller that can work with different modulation methods over wide input voltage and output power range is proposed.

This chapter is organized as follows: Section. 3.2 reviews the nonlinearity in the control objective and variable. Section. 3.3 proposes using feedback linearization to achieve the voltage regulation. In Section. 3.4 documents and investigates

the results. Finally, Section. 3.5 concludes the chapter.

3.2 Nonlinearity in hybrid modulation

The relationship between i_{DAB} and phase shift ϕ under PSM modulation is defined before in Eqn. (2.13), it is rewritten here for reading convenience

$$i_{DAB} = F_I(u) = \frac{V_1 2\phi(1-2\phi)}{2nL_k f_s} \tag{3.1}$$

Under Proposed Triangular Modulation (PTRM), the relationship between output current i_{DAB} and duty ratio D_1 can be derived based on Eqn. (2.21),

$$i_{DAB} = F_{II}(u) = \frac{V_1^2 D_1^2}{V_2 L_k f_s} \tag{3.2}$$

From Eqn. (3.1), i_{DAB} is a nonlinear function of ϕ. Similarly under proposed triangular modulation, the relationship between i_{DAB} and duty ratio is also in nonlinear relationship as Eqn. (3.2).

Fig. 3.1 and Fig. 3.2 show the relationship between output current i_{DAB} and control variable under two modulation modes. Nonlinearities can also be observed from the figures.

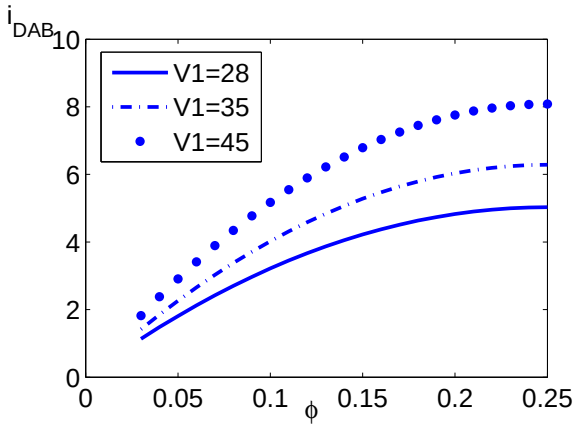


Figure 3.1: Relationship between i_{DAB} and ϕ under PSM

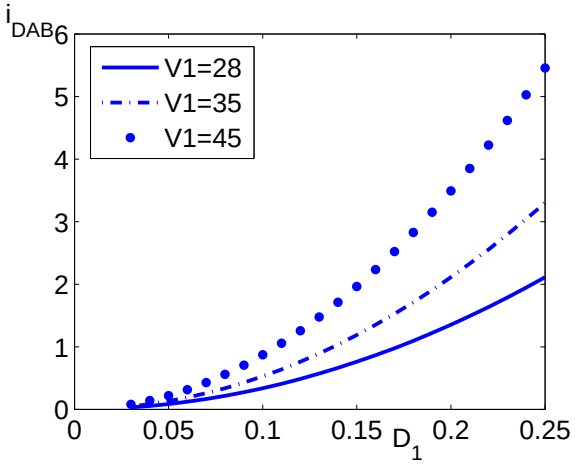


Figure 3.2: Relationship between i_{DAB} and D under PTRM

Nonlinearity between the control variable and output current causes the difficulties to design a linear controller that is suitable for a wide operating range. To simplify the controller design, a feedback linearization is used to compensate for the nonlinearities, so that the closed loop controller can be designed in a linear form [29].

3.3 Feedback linearization controller design

The control objective is to regulate V_2 and satisfy load variation between 200W to 1200W which corresponds to 16.67% to 100 % of the maximum power to be transferred. As mentioned in previous chapter, this range cannot be achieved if only phase shift modulation is used. Thus the system operates under two possible modulation modes. These modulation modes are incorporated in the controller design.

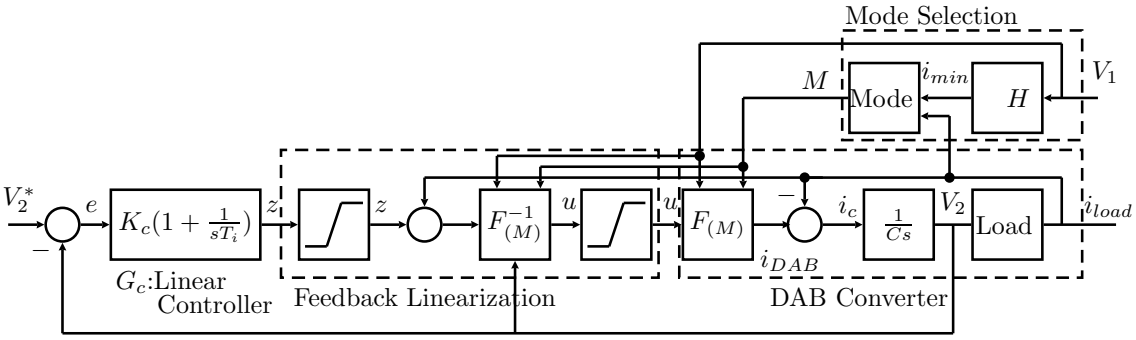


Figure 3.3: Control diagram by using feedback linearization

3.3.1 Feedback linearization controller

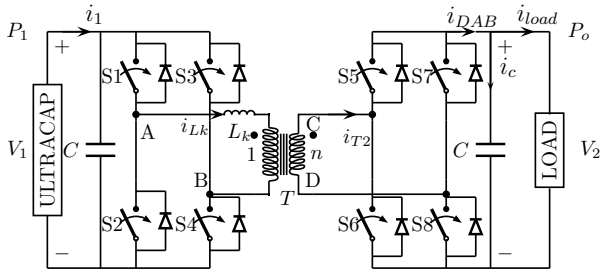


Figure 3.4: Topology of DAB converter

The control diagram is shown as Fig. 3.3 and detailed controller design procedures are given below. To illustrate the design of controller, proposed triangular modulation is used as an example. According to Fig. 3.4, the system dynamics can be written as

$$\begin{aligned} C\frac{dV_2}{dt} &= i_{DAB} - i_{load} \\ &= F_M(u) - i_{load} \end{aligned} \tag{3.3}$$

Here M denotes the selected mode. For example, when phase shift modulation is used, Mode I will be enabled, otherwise Mode II will be enabled with the proposed triangular modulation. $u[D_1, D_2, \phi]$ is a set of control variables. The relationship between i_{DAB} and u when proposed triangular modulation used is described in Eqn.(3.2) and rewritten here

$$i_{DAB} = F_{II}(u) = \frac{V_1^2 D_1^2}{V_2 L_k f_s}$$

If u is chosen such that

$$u = F_{II}^{-1}(z + i_{load}) \tag{3.4}$$

with z being "equivalent input" to be specified, the resulting dynamics becomes linear

$$C\frac{dV_2}{dt} = z \tag{3.5}$$

Choosing z as

$$\dot{z} = K_c\dot{e} + \frac{K_c}{T_i}e \tag{3.6}$$

where the $e = V_2^* - V_2$. Inserting Eqn. (3.6) in Eqn. (3.5), the closed loop system dynamic can be represented as

$$\ddot{V}_2 + \frac{K_c}{C}\dot{V}_2 + \frac{K_c}{T_i C}V_2 = \frac{K_c}{CT_i}V_2^* \tag{3.7}$$

Using Eqn. (3.6), we choose the natural frequency $\omega_n = 628$rad/s and the damping ratio as $\xi = 1$ in the characteristic polynomial $p^2 + 2\xi\omega_n p + \omega_n^2$ such that the roots of the polynomial are so placed that it results in a stable system dynamics. The function of $F_M^{-1}(i_{DAB})$ block changes according to the modes tabulated in Table. 3.1.

Table 3.1: Inverse function of phase shift and proposed triangular modulations

Mode	F_M^{-1}	ϕ	D_1	D_2
Mode I	F_I^{-1}	$sgn(i_{DAB})\frac{1}{4}[1 - \sqrt{1 - \frac{8\lvert i_{DAB}\rvert nL_k f_s}{V_1}}]$	0.43	0.43
Mode II	F_{II}^{-1}	$sgn(i_{DAB})D_1$	$\frac{1}{V_1}\sqrt{L_k f_s V_2 \lvert i_{DAB}\rvert}$	$V_1/(V_2/n)D_1$

In the proposed scheme, V_1 and i_{load} are measured. It is necessary to measure V_1 in real time to monitor the ultracapacitor terminal voltage. Using this information, the energy level in the ultracapacitor can be estimated and over-voltage and under-voltage can be avoided. The load sensor can also be used to monitor the over-current. It allows us to shut down the converter as well as disconnect the

converter from ultracapacitor if need arises. By measuring the V_1, the controller is able to handle the input voltage disturbance as well. Using a model to generate the relationship between the i_{DAB} and duty ratio D_1, the feedback load current together with feedback linearization block will generate the desired control variable in time. The PI controller will react only when there is steady state error. Therefore the system dynamic will be significantly improved.

An accurate model is needed, the differences between the ideal and practical model is shown in Fig. 3.5. However, in practice, the existence of losses and the dead time causes the above mentioned inverse model to be inaccurate. Fig. 3.5 shows the relationship between the phase shift and the output current when V_1=28.5V and the power varies from 650W to 1200W. In Fig. 3.5, the practical curve requires more phase shift than the ideal case. Also, the converter does not have the same efficiency under different power loading.

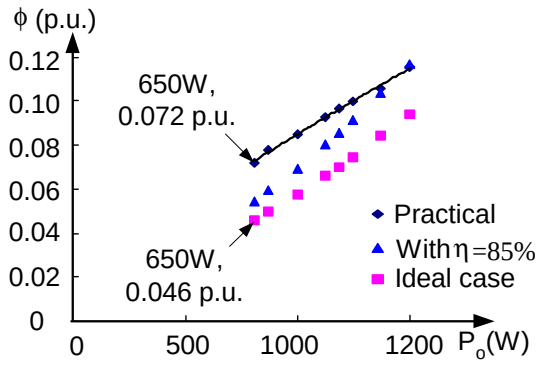


Figure 3.5: Comparison between the ideal and practical inverse model

This difference is big especially at low power load. For example, 0.046 p.u.

is needed to transfer 650W as calculated according to the inverse model listed in Table. 3.1. However, in practice, 0.072 p.u. is needed. This causes the PI controller to not only cancel the minor steady state error, but also contribute about 36% of final steady state value of total phase shift. In order to avoid this, a more accurate model is used.

3.3.2 Mode selection

To switch between two modes smoothly, a hysteresis mode selection is described here. As mentioned above, since hybrid modulation is applied a mode selection block *Mode* shown in Fig. 3.3 is introduced. Block H in Fig. 3.3 is used to generate i_{min} under different input voltages, the function is described as

$$i_{min} = \frac{V_1 2\phi_{min}(1 - 2\phi_{min})}{2L_k f_s n} \tag{3.8}$$

by using minimum phase shift $\phi_{min} = 0.03$ p.u. To avoid the chattering between two different modes, a hysteresis comparator shown in Fig. 3.6 is utilized. This hysteresis comparator enables Mode I when the absolute load current is higher than the minimum phase shift modulation capability i_{min} by 0.15A. Mode II will be enabled when the absolute load current is lower than the i_{min}. After mode selection, the reference i_{DAB} is available, the related phase shift and duty ratios for each mode can be generated according to inverse model measured based on experiments.

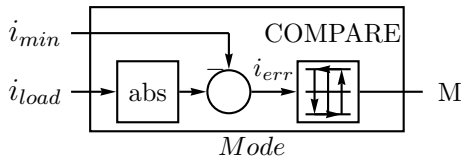


Figure 3.6: Hysteresis comparison block

3.4 Experimental results

Same dSPACE 1104 experimental platform, which is described in Chapter. 2, is used to implement the feedback linearization controller.

Fig. 3.7 to Fig. 3.9 show the close loop step response under different input and various load condition. The control objective is to regulate output voltage V_2 at 400V. The practical model with the feedback linearization controller using proposed hybrid modulation is adopted here.

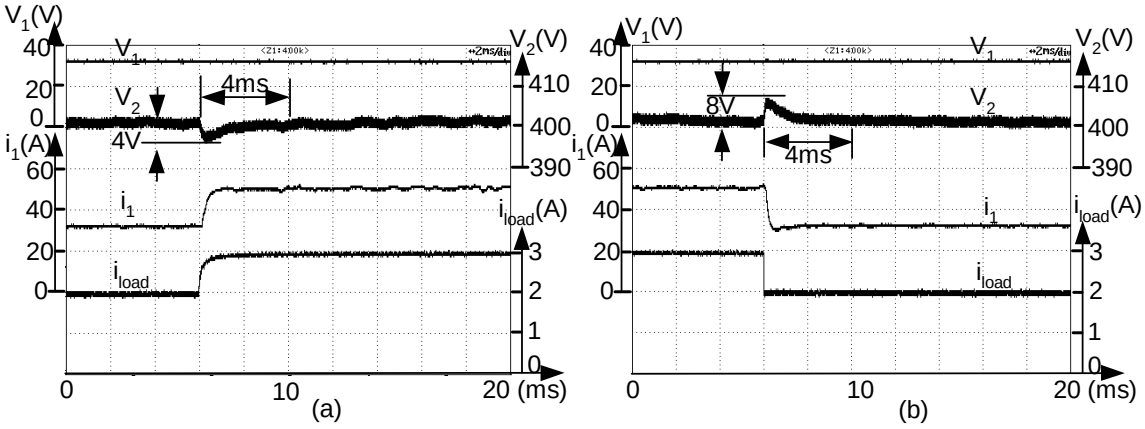


Figure 3.7: Response when power changes between 800W and 1200W when (V_1=30V)

Fig. 3.7 shows the step response when input voltage is 30V and load power changes from 800W and 1200W. From Fig. 3.7, the undershoot and the overshoot during the step up and step down are only 4V and 8V respectively and the recovery time is 4ms.

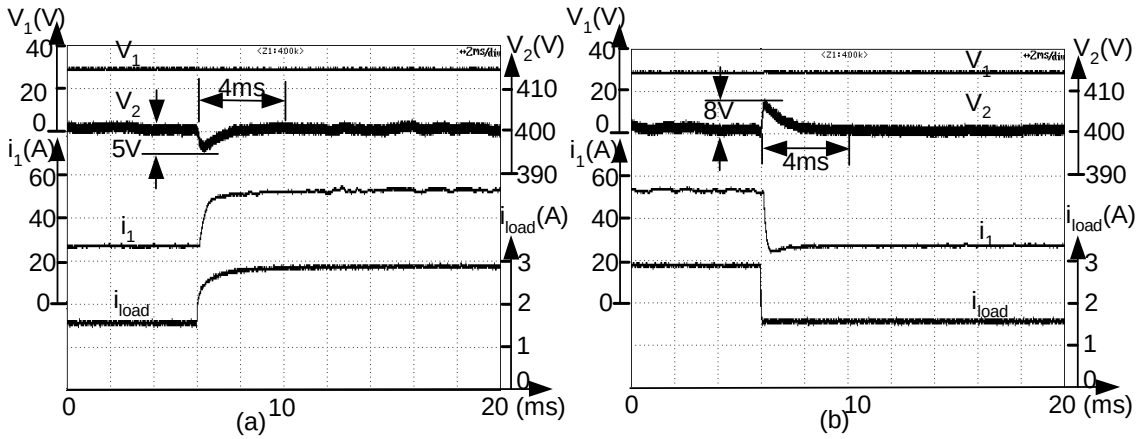


Figure 3.8: Response when power changes between 650W to 1200W

Fig. 3.8 is recorded when input voltage is 28.5V and the power changes from 650W to 1200W. From Fig. 3.8, the output voltage is well regulated and dynamic responses is good.

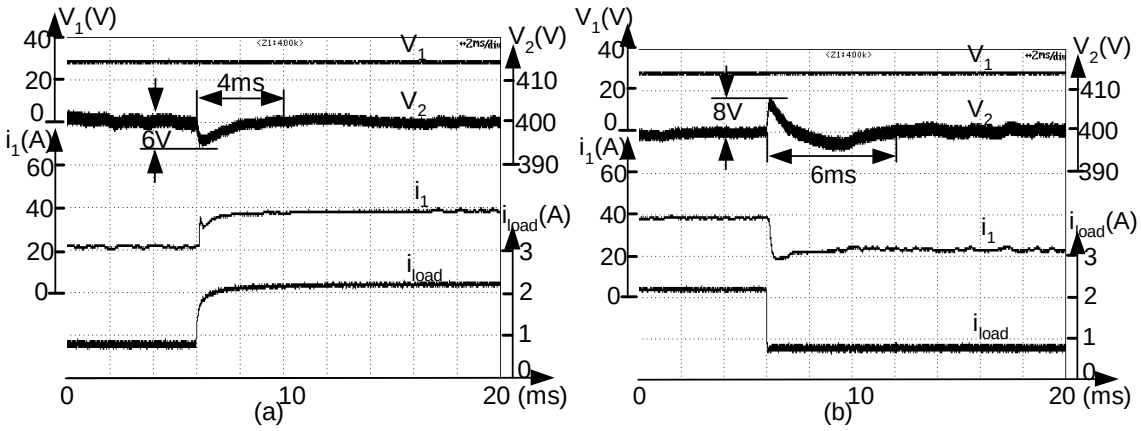


Figure 3.9: Response when power changes between 300W and 900W

The close loop step response when two modulation all involved is shown in Fig. 3.9. From power calculation, the minimum power of phase shift modulation is 443W when $V_1 = 28.5V$. In other words, the proposed triangular modulation will be used between 200W to 443W under this condition. When load changes between 300W and 900W, see Fig. 3.9, the output voltage is well regulated and the recovery time for step up and step down are 4ms and 6ms respectively.

3.5 Summary

In this chapter, a feedback linearization controller has been implemented to achieve voltage regulation in a wide range. The experimental results show the proposed controller with hybrid modulation is able to achieve good dynamic response as well as regulation.

Chapter 4

Passivity based control for ICFFB converter

4.1 Introduction

Just as energy storage needs bi-directional converter, a front-end converter is also needed to interface the renewable source and DC bus. Generally, the renewable energy has low and varying output voltage while DC bus voltage is always high. Therefore, boost type converter is usually connected between the renewable energy and load. Besides that, ripple current caused from front-end converter should be minimized so that more output power can be used [30]. In this chapter, Interleaved Current Fed Full Bridge (ICFFB) converter [31] is studied due to its low input

ripple, high boost ratio and isolated capability .

However, as most boost type converter, voltage regulation for ICFFB has non-minimum phase characteristics. This poses difficulties in high bandwidth voltage regulation, especially under conditions where the operating points vary a lot. In this chapter, we will investigate the controller design for this boost type converter.

The conventional methods of controller design used for the boost type converter can be broadly divided into two types: linear and nonlinear controller.

Design of linear controllers is based on either frequency domain methods or root locus method that either compensates or cancels the unwanted poles of the existing system. For PI type linear controller design, the controller is designed for the converter transfer function which is linearized at an operating point. On the other hand, renewable energy source voltage is not controlled and will vary based on current changes. Thus, the operating point also changes. Hence a linear controller designed for a specific operating point will not be effective.

In [32, 33] nonlinear controllers are also proposed to solve the regulation problem. They allow a design over wide operating range. Methods such as sliding mode control and Lyapnouv's direct control methods have been used to achieve this.

Passivity based control [34] achieves control objective through energy reshap-

ing. The stability is naturally achieved in the whole operating range. It is interesting to investigate PBC controller in this chapter.

This chapter is organized as follows: Section. 4.2 investigates the limitation of non-minimum phase system. Section. 4.3 describes the background of passivity based control. Section. 4.4 models CFFB converter using Mixed Potential Function (MPF). Section. 4.5 implements PBC controller. Stability and tuning parameters are investigated. Section. 4.6 discusses the experimental results. Section. 4.7 compares the controller performance. Finally, conclusions and discussions are listed in Section. 4.8.

4.2 Non-minimum phase characteristics in boost converter

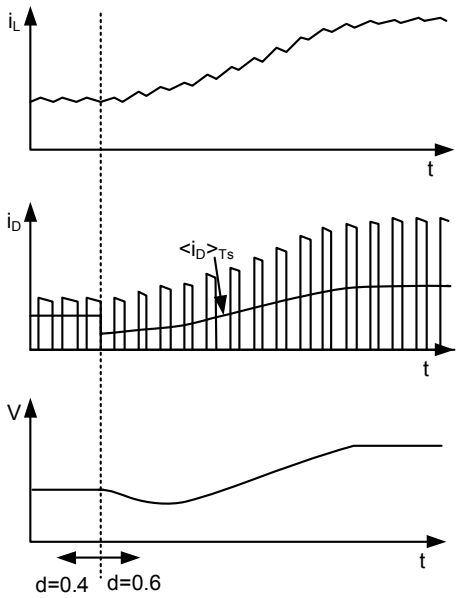


Figure 4.1: Dynamic response when duty ratio step changes from 0.4 to 0.6

Boost converter has non-minimum phase relationship between its control variable duty ratio and its output voltage. Fig. 4.1 shows typical non-minimum phase system dynamic response. At $t = t_0$, duty ratio steps from 0.4 to 0.6. The output voltage V reduces initially then increases in the later stage. This wrong direction change in the dynamic tends to destabilize wide-bandwidth feedback loops.

To understand non-minimum phase nature of ICFFB converter which is shown as Fig. 4.2, the transfer function between the duty ratio and the output voltage is investigated. From [31], small signal modeling of the converter can be

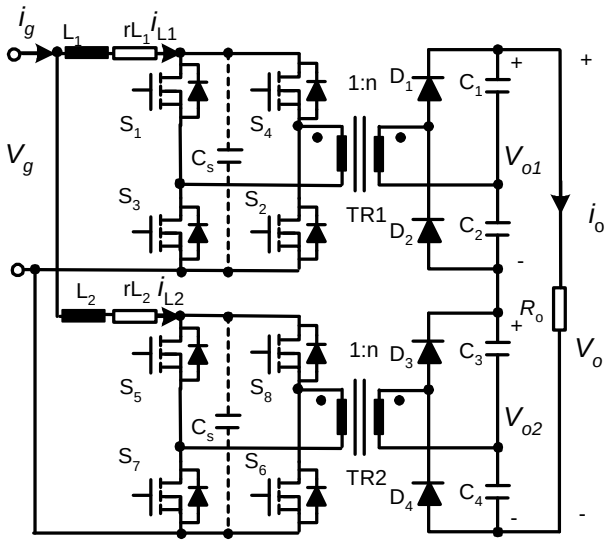


Figure 4.2: Interleaved Current Fed Full Bridge Converter(ICFFB)

rewritten as

$$L_1 \frac{d\langle i_1(t)\rangle_{T_s}}{dt} = (v_g(t) - r_1 i) - \frac{v_o(t)}{2n} D', \tag{4.1}$$

$$L_2 \frac{d\langle i_2(t)\rangle_{T_s}}{dt} = (v_g(t) - r_2 i) - \frac{v_o(t)}{2n} D', \tag{4.2}$$

$$C_1 \frac{d\langle v_{c1}(t)\rangle_{T_s}}{dt} = C_2 \frac{d\langle v_{c2}(t)\rangle_{T_s}}{dt} = \frac{i_1(t)}{n} D' - \frac{v_o(t)}{R}, \tag{4.3}$$

$$C_3 \frac{d\langle v_{c3}(t)\rangle_{T_s}}{dt} = C_4 \frac{d\langle v_{c4}(t)\rangle_{T_s}}{dt} = \frac{i_2(t)}{n} D' - \frac{v_o(t)}{R}. \tag{4.4}$$

In order to simplify the calculations, it is reasonable to assume that $C_1 \sim C_4 = C$. Linearizing Eqn. (4.1) $\sim$ Eqn. (4.4) at steady-state, and applying Laplace

transformation, the control to output small signal transfer functions is obtained:

$$\begin{aligned} G_{i1d}(s) &= \frac{\hat{i_1}}{\hat{d}} \\ &= \frac{n(r_2 + L_2 s)(8 + CRs)V_o}{2(D'^2 R * a + n^2(r_1 + L_1 s)(r_2 + L_2 s)(4 + CRs))}, \end{aligned} \tag{4.5}$$

$$\begin{aligned} G_{i2d}(s) &= \frac{\hat{i_2}}{\hat{d}} \\ &= \frac{n(r_1 + L_1 s)(8 + CRs)V_o}{2(D'^2 R * a + n^2(r_1 + L_1 s)(r_2 + L_2 s)(4 + CRs))}, \end{aligned} \tag{4.6}$$

$$\begin{aligned} G_{vig}(s) &= \frac{\hat{v_o}}{\hat{i_g}} \\ &= \frac{-8n(r_1 + L_1 s)(r_2 + L_2 s) + 2D'^2 R * a/n}{D'(8 + CRs) * a}. \end{aligned} \tag{4.7}$$

Where

$$\begin{cases} a = r_1 + r_2 + (L_1 + L_2)s, \\ \hat{i}_g = \hat{i}_1 + \hat{i}_2. \end{cases} \tag{4.8}$$

$G_{i1d}(s)$ and $G_{i2d}(s)$ are small signal transfer functions from duty ratio to individual inductor current, while $G_{vig}(s)$ is the small signal transfer function from input current to output voltage.

Here, it is obvious that there is a Right Half Zero (RHZ) in transfer function Eqn. (4.7). Whenever open-loop system has a right-half plane zero, the step response spends part of its time going in the wrong direction as Fig. 4.1. Since zeros of the open-loop forward transfer function $G_{vig}(s)$ appear as closed-loop zeros, then the system's step response will exhibit undershoot, taking on negative values.

4.3 Background of Passivity Based Control

Since the power converter is used to transfer the energy from the source to the load, an energy based controller can be investigated for boost type converter in this chapter. The merits of passivity based control (PBC) are

- Design controllers without linearization of the system.
- Physical and intuitive representation of the control problem
- Global stability is ensured by passivity properties

Before using PBC controller, questions such as how to represent a system in energy form; What are the potential function and dissipative function should be investigated. Basic terms such as dissipative and passive system are defined here [34].

Dissipative System: During interval $\triangle t$, for a system if change in energy supplied to system is larger than the increase of stored energy. We call this system as dissipative.

Passive System: If the system is dissipative, and we denote $u \in R^m$ and $y \in R^m$ are the input and output of the dissipative system respectively, and for which the supply rate function as $u^T y$, then the system $\sum : u \rightarrow y$ is passive system [34].

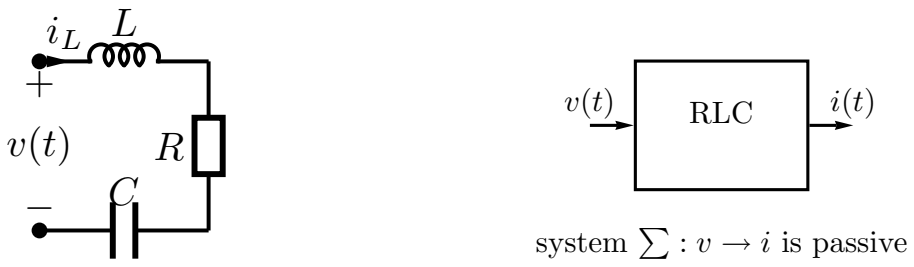


Figure 4.3: Basic RLC circuit

For instance, for RLC circuit shown in Fig. 4.3, voltage is the input of the system while current is the output of system. First, due to loss in resistor R, energy supplied from voltage source is larger than the increase of stored energy in L and C. Therefore system is dissipative. At the same time, the supply rate function can be represented by Vi. Therefore, the system $v \longrightarrow i$ is passive.

After we understand the dissipative and passive system definition. Now, let us have a look on how to model system in terms of Euler Lagrange (EL) format for a conservative system,

$$\frac{\partial \mathcal{L}}{\partial q_i} - \frac{d}{dt}(\frac{\partial \mathcal{L}}{\partial \dot{q}_i}) = 0, i = 1, ..., N; \tag{4.9}$$

where $\mathcal{L}(q, \dot{q}, t)$ is Lagrange function defined as the difference between the kinetic and potential energy:

$$\mathcal{L}(q, \dot{q}, t) = \underbrace{\mathcal{T}(q, \dot{q}, t)}_{kinetic} - \underbrace{\mathcal{V}(q, t)}_{potential} \tag{4.10}$$

q and $\dot{q}$ are *displacements* and *velocities* in mechanical system.

Here the conservative system is the system whose total energy is always constant,

that is

$$\sum energy = \mathcal{T}(q, \dot{q}, t) + \mathcal{V}(q, t) = Constant \tag{4.11}$$

According to Hamilton's principle, the actual dynamic path of a system described by Lagrange function $\mathcal{L}(q, \dot{q}, t)$ from time t_1 to t_2 is such that the line integral

$$I = \int_{t1}^{t2} \mathcal{L}(q, \dot{q}, t) \tag{4.12}$$

is an extremum for this path. Therefore

$$\delta I = \delta \int_{t1}^{t2} \mathcal{L}(q, \dot{q}, t) = 0 \tag{4.13}$$

That means system always finds minimum action way to reach the next point though there exists many possible ways.

In practice, system always faces external forces and disturbances. Therefore a non-conservative system can be described as

$$\frac{d}{dt}(\frac{\partial \mathcal{L}_{\mathcal{NC}}}{\partial \dot{q}_i}) - \frac{\partial \mathcal{L}_{\mathcal{NC}}}{\partial q_i} = \underbrace{u + Q_\varsigma - \frac{\partial \mathcal{F}}{\partial \dot{q}_i}}_{dissipative function} \tag{4.14}$$

where u is the control and Q_ς is the external disturbances

$$\mathcal{L}_{\mathcal{NC}}(q, \dot{q}, t) = \mathcal{T}(q, \dot{q}) + \int_0^t \mathcal{F}(\dot{q})dt - \underbrace{(\mathcal{V}(q) + \mathcal{V}_{NC}(q, t))}_{potential function} \tag{4.15}$$

Here

$\int_0^t \mathcal{F}(\dot{q})dt$ is the Rayleigh dissipation function. For.e.g. friction loss

$\mathcal{V}_{NC}(q,t)$ is the non-conservative forces. For.e.g. external energy

From above descriptions, we can see that a change in the potential function will change the equilibrium point of the system while modification of the dissipative function will change the trajectory of the system. Therefore, to control the trajectory of a system, a controller can be implemented to modify its dissipative function. This is the basis of the PBC controller.

4.4 Dynamic model of CFFB using Mixed Potential Function (MPF)

However Euler-Lagrange form model and controller design is more suitable in representation of the mechanical system. For systems that are represented as electrical circuits, energy content can be represented by a single scalar function: the mixed potential function, proposed by Brayton and Moser [35], [36]. Thus the controller could be expressed directly in physically measurable quantities like current and voltages instead of the charges or fluxes required in the Euler-Lagrangian formulation. In addition to general benefits of PBC controller listed in the previous, another salient feature of BM based PBC is it enables the controller design on measurable variables such as voltage and current in electrical circuit.

In this section, a Mixed Potential Function (MPF) will be constructed for

CFFB converter. In order to understand the detailed formulation and physical meaning of mixed potential function P, here the derivation of mixed potential function P for a simple boost converter is given first as example

4.4.1 Formulating Mixed Potential Function (MPF) for boost converter

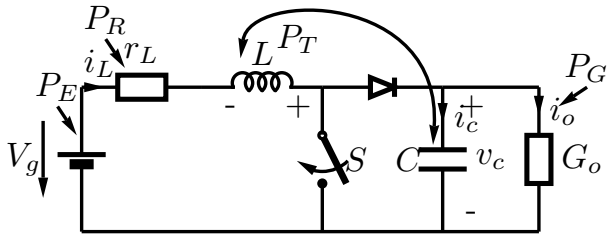


Figure 4.4: Topology of boost converter

The mixed potential of the boost converter shown in Fig. 4.4 is defined as

$$\begin{aligned} P(i_L, v_c) &= P_{i_L}^{tot} - P_{v_c}^{tot} + P_T \\ P(i_L, v_c) &= P_T + \underbrace{P_R - P_G}_{P_D} + \underbrace{P_E - P_J}_{P_F} \end{aligned} \tag{4.16}$$

where

$P_{i_L}^{tot}$: total current potential

$P_{v_c}^{tot}$: total voltage potential

P_T : internal power circulating across the dynamic elements

P_R : dissipative current potential

P_G : dissipative voltage potential

P_E : total supplied power by current controlled voltage source

P_J : total supplied power by voltage controlled current source

Thus, the mixed potential represents the total power in the system and has the units of power. Here, $P_D = P_R - P_G$ is the defined as the total dissipative potential and $P_F = P_E - P_J$ is a measure of the total power supplied to the system. The positive sign of P_E represents energy generated or supplied to the system while the positive sign for dissipative power P_R represents the energy is out from the system.

In the boost converter, for the current state variable i_L, current potentials can be written as

$$P_E = -\int^{i_L} V_g di_L = -V_g i_L \tag{4.17}$$

$$P_R = \int^{i_L} r_L i_L di_L = \frac{1}{2} r_L i_L^2 \tag{4.18}$$

Similarly, potentials can be expressed using the voltage state variable v_c as

$$P_J = 0 \tag{4.19}$$

$$P_G = \int^{v_c} G_o v_c dv_c = \frac{1}{2} G_o v_c^2 \tag{4.20}$$

P_J, the potential that represents the total power supplied by the current source, is zero as there are no current sources in the circuit. P_G is dissipative power across

the load G_o.

The internal power P_T circulating across the dynamic elements between inductor and the capacitor at any instant is

$$P_T = \int^{v_c} i_L(1-u)dv_c = i_L(1-u)v_c \tag{4.21}$$

Here, u represents the switching function. When $u = 0$, the switch S in circuit Fig. 4.4 is open, inductor stored power P_T is transferred to the capacitor. While $u = 1$, there is no power transfer from inductor to capacitor. Therefore, the MPF for the boost converter shown in (4.16) can be formulated as:

$$\begin{aligned} P(i_L, v_c) &= \underbrace{(\frac{1}{2}r_L i_L^2 - V_g i_L)}_{P_{i_L}^{tot}} - \underbrace{(\frac{1}{2}G_o v_c^2 + 0)}_{P_{v_c}^{tot}} + \underbrace{i_L(1-u)v_c}_{P_T} \\ &= \underbrace{(\frac{1}{2}r_L i_L^2 - \frac{1}{2}G_o v_c^2)}_{P_D} + \underbrace{(-V_g i_L - 0)}_{P_F} + \underbrace{i_L(1-u)v_c}_{P_T} \end{aligned} \tag{4.22}$$

4.4.2 Dynamic model of CFFB using Mixed Potential Function (MPF)

One ICFFB converter, Fig. 4.5, contains two identical Current Fed Full Bridge (CFFB) converters. For simplicity, only the model of the upper CFFB shown in Fig. 4.6 is being considered. As depicted in Fig. 4.6, the CFFB system has one inductor and two capacitors. Assuming that the transformer is ideal, the state variables $i_{L1}(t)$, $v_{C1}(t)$, $v_{C2}(t)$ can be used to represent the system. Here $i_{L1}(t)$ is the current flowing through inductor, $v_{C1}(t)$, $v_{C2}(t)$ are the voltages across the capacitor C_1 and C_2 respectively.

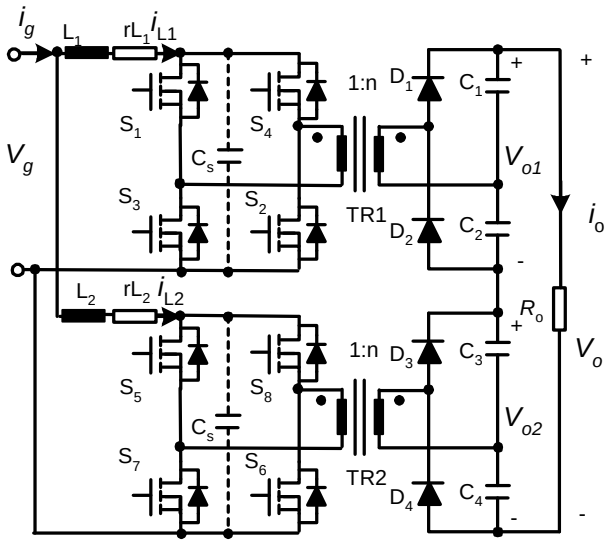


Figure 4.5: Interleaved Current Fed Full Bridge Converter(ICFFB)

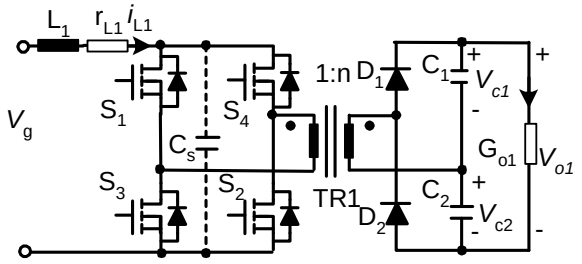


Figure 4.6: Single Current Fed Full Bridge Converter (CFFB)

The dynamic behavior of the converter system in the BM form could be described as

$$-L_1 \frac{di_{L1}(t)}{dt} = \frac{\partial P}{\partial i_{L1}}(i_{L1}, v_{C1}, v_{C2}) \tag{4.23a}$$

$$C_1 \frac{dv_{C1}(t)}{dt} = \frac{\partial P}{\partial v_{C1}}(i_{L1}, v_{C1}, v_{C2}) \tag{4.23b}$$

$$C_2 \frac{dv_{C2}(t)}{dt} = \frac{\partial P}{\partial v_{C2}}(i_{L1}, v_{C1}, v_{C2}) \tag{4.23c}$$

Similarly as formulated for boost converter, for CFFB converter, the mixed-

potential function P that captures the interconnection potential P_T, dissipation potential P_D and potential due to external energy sources P_F is given as

$$\begin{aligned} P(i_{L1}, v_{C1}, v_{C2}) &= P_T + P_D + P_F \\ &= (i_{L1}\frac{1-u_1}{n}v_{C1} + i_{L1}\frac{1-u_2}{n}v_{C2}) \\ &\quad +(\frac{1}{2}i_{L1}^2 r_{L1} - G_{o1}\frac{(v_{C1}+v_{C2})^2}{2}) \\ &\quad +(-V_g \cdot i_{L_1} - 0) \end{aligned} \tag{4.24}$$

Here u_1 and u_2 are switching functions for controlling S_1, S_2 and S_3, S_4 in CFFB converter (Fig. 4.6) respectively. r_{L1}, n and G_{o1} are the equivalent series resistor of inductor L_1, transformer turns ratio and the load conductance.

Inserting Eqn. (4.24) into Eqn. (4.23), the equations describing the dynamic behavior of the CFFB converter are given as

$$L_1\frac{di_{L1}}{dt} = \frac{v_{C1}(1-u_1)}{n} + \frac{v_{C2}(1-u_2)}{n} \tag{4.25a}$$

$$+ i_{L1}r_{L1} - V_g$$

$$C_1\frac{dv_{C1}}{dt} = \frac{i_{L1}(1-u_1)}{n} - G_{o1}(v_{C1}+v_{C2}) \tag{4.25b}$$

$$C_2\frac{dv_{C2}}{dt} = \frac{i_{L1}(1-u_2)}{n} - G_{o1}(v_{C1}+v_{C2}) \tag{4.25c}$$

For converters operating at constant switching frequency of a sufficiently high value, the system could be described using average value of state variables. This average value is calculated within one switching period. In so doing, the duty ratio D can be used as the control variable, instead of a switching function u. For CFFB converter, the duty ratio of S_3, S_4 and S_1, S_2 are the same, see Fig. 4.7, hence

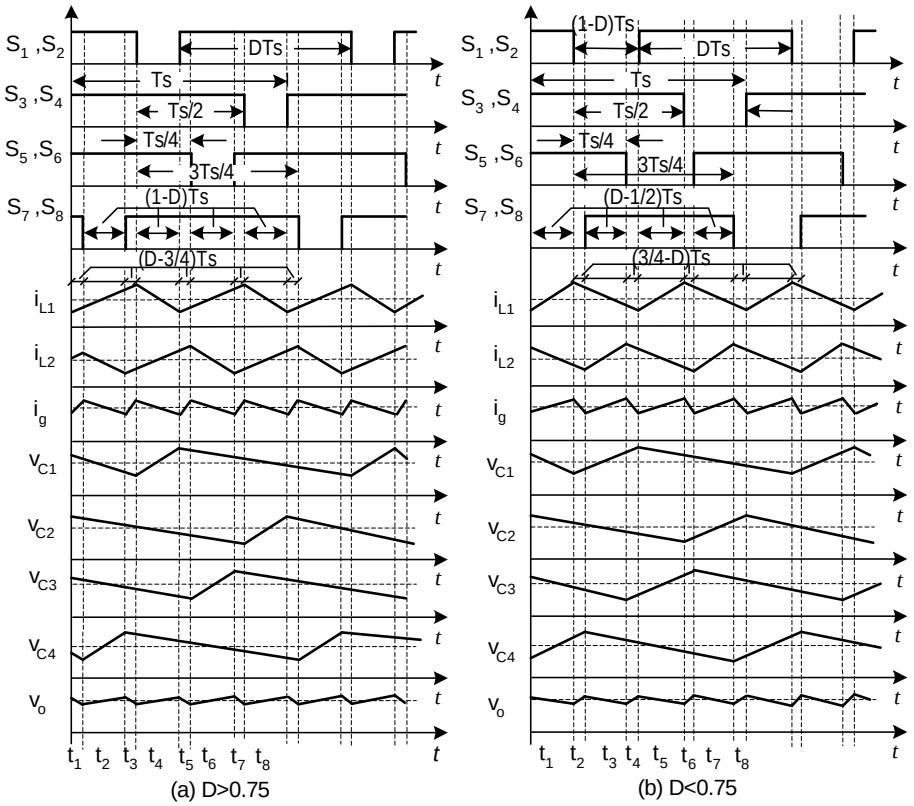


Figure 4.7: Key waveforms in ICFFB

$D_1 = D_2 = D$. The instantaneous state variables i_{L1}, v_{C1}, v_{C2} in (4.25) can be replaced by their average state variables $\langle i_{L1}(t)\rangle$, $\langle v_{C1}(t)\rangle$ and $\langle v_{C2}(t)\rangle$. Since the output voltage V_{o1} is being measured and controlled, an augmented state variable can be defined as $\langle v_{o1}(t)\rangle = \langle v_{C1}(t)\rangle + \langle v_{C2}(t)\rangle$. Let $C_1 = C_2 = 2C$, $L_1 = L$ in Eqn. (4.25). Then the simplified mixed potential function using average state variables $\langle i_{L1}(t)\rangle$ and $\langle v_{o1}(t)\rangle$ is

$$\begin{aligned} P(\langle i_{L1}\rangle, \langle v_{o1}\rangle) &= P_T(\langle i_{L1}\rangle, \langle v_{o1}\rangle) + P_D(\langle i_{L1}\rangle, \langle v_{o1}\rangle) + P_F(\langle i_{L1}\rangle, \langle v_{o1}\rangle) \\ &= (\langle i_{L1}\rangle \frac{1-D}{n} \langle v_{o1}\rangle) \\ &\quad +(\frac{1}{2}\langle i_{L1}\rangle^2 r_{L1} - G_{o1}\frac{\langle v_{o1}\rangle^2}{2}) \\ &\quad +(-V_g \cdot \langle i_{L1}\rangle - 0) \end{aligned} \tag{4.26}$$

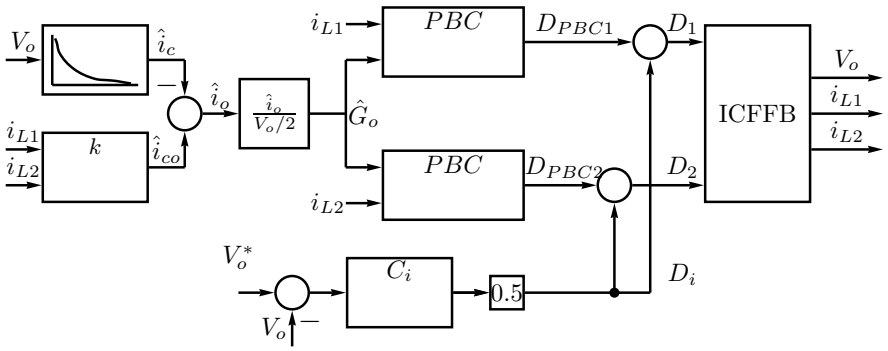


Figure 4.8: Control block for proposed PBC with augmented integrator and load estimator

Therefore the dynamic behavior of CFFB can be obtained by partial differentiation of the MPF Eqn. (4.26) with respect to each state variable

$$-L\frac{d\langle i_{L1}(t)\rangle}{dt} = \frac{\langle v_{o1}(t)\rangle(1-D)}{n} + \langle i_{L1}(t)\rangle r_{L1} - V_g \tag{4.27a}$$

$$C\frac{d\langle v_{o1}(t)\rangle}{dt} = \frac{\langle i_{L1}(t)\rangle(1-D)}{n} - G_{o1}\langle v_{o1}(t)\rangle \tag{4.27b}$$

4.5 Passivity Based Controller (PBC) Design

The controller is designed to control the inductor current directly and shape its trajectory to achieve the desired output voltage. This can be achieved by injecting series damping in the inductor path. The advantages of using the series damping are 1) there is simple relationship between inductor current and output voltage under specific load 2) current has a minimum phase behavior with the duty ratio 3) the steady state characteristic of the average value of inductor current is monotonically increasing as a function of the duty ratio [37], [38]. However for the series damping injection approach, the exact circuit parameters should be known.

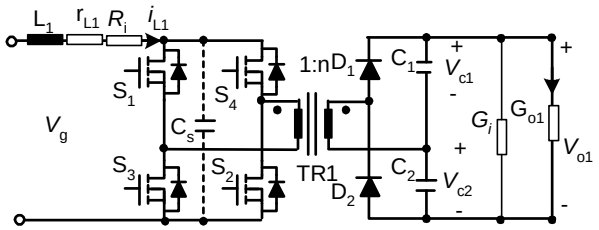


Figure 4.9: Possible damping injection in CFFB

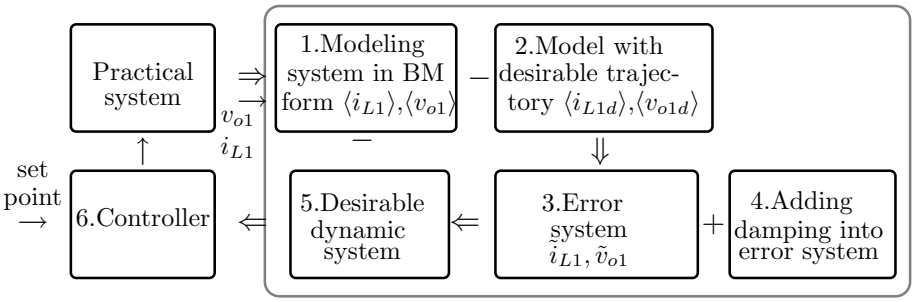


Figure 4.10: Procedures to design the BM based PBC controller

In passivity based control, damping is injected into the system through the control function. To shape the error dynamics of the system, damping resistor R_i is injected in series with the inductor and damping conductance G_i is injected in parallel with the capacitor as shown in Fig. 4.9. However, as CFFB converter has a non-minimum phase relationship between the output voltage and duty ratio, the direct control of the output voltage leads to system instability [34, 39].

The process of passivity based control is described in Fig. 4.10. As in block 1, Fig. 4.10, the dynamic behavior of the system can be described using the mixed

potential function as

$$-L\frac{d\langle i_{L1}\rangle}{dt} = \frac{\partial(P_T + P_D + P_F)}{\partial\langle i_{L1}\rangle}(\langle i_{L1}\rangle, \langle v_{o1}\rangle) \tag{4.28a}$$

$$C\frac{d\langle v_{o1}\rangle}{dt} = \frac{\partial(P_T + P_D + P_F)}{\partial\langle v_{o1}\rangle}(\langle i_{L1}, v_{o1}\rangle) \tag{4.28b}$$

On the other hand, in block 2, Fig. 4.10, the desired trajectory of the state variables can be expressed in terms of a mixed potential function of an auxiliary system as

$$-L\frac{d\langle i_{L1d}\rangle}{dt} = \frac{\partial(P_T + P_D + P_F)}{\partial\langle i_{L1d}\rangle}(\langle i_{L1d}\rangle, \langle v_{o1d}\rangle) \tag{4.29a}$$

$$C\frac{d\langle v_{o1d}\rangle}{dt} = \frac{\partial(P_T + P_D + P_F)}{\partial\langle v_{o1d}\rangle}(\langle i_{L1d}\rangle, \langle v_{o1d}\rangle) \tag{4.29b}$$

Here $\langle i_{L1d}\rangle$ and $\langle v_{o1d}\rangle$ are the desired trajectories for the average inductor current and average output voltage for one CFFB converter.

The difference between the state variables of the systems defined in block 1 and 2 in Fig. 4.10 and given by (Eqn. 4.28) and (Eqn. 4.29) would define the error trajectory of the state variables as $\tilde{i}_{L1} = \langle i_{L1}\rangle - \langle i_{L1d}\rangle$ and $\tilde{v}_{o1} = \langle v_{o1}\rangle - \langle v_{o1d}\rangle$.

The error dynamics are described as

$$-L\frac{d\tilde{i}_{L1}}{dt} = \frac{\partial(P_T + P_D + P_F)}{\partial\langle i_{L1}\rangle}(\langle i_{L1}\rangle, \langle v_{o1}\rangle) - \frac{\partial(P_T + P_D + P_F)}{\partial\langle i_{L1d}\rangle}(\langle i_{L1d}\rangle, \langle v_{o1d}\rangle) \tag{4.30a}$$

$$C\frac{d\tilde{v}_{o1}}{dt} = \frac{\partial(P_T + P_D + P_F)}{\partial\langle v_{o1}\rangle}(\langle i_{L1}, v_{o1}\rangle) - \frac{\partial(P_T + P_D + P_F)}{\partial\langle v_{o1d}\rangle}(\langle i_{L1d}\rangle, \langle v_{o1d}\rangle) \tag{4.30b}$$

It is assumed that the first two derivatives $P_T(\langle i_{L1}\rangle, \langle v_{o1}\rangle)$, $P_D(\langle i_{L1}\rangle, \langle v_{o1}\rangle)$ are linear functions of $\langle i_{L1}\rangle$, $\langle v_{o1}\rangle$. Similarly, $P_T(\langle i_{L1d}\rangle, \langle v_{o1d}\rangle)$, $P_D(\langle i_{L1d}\rangle, \langle v_{o1d}\rangle)$ are linear functions of $\langle i_{L1d}\rangle$ and $\langle v_{o1d}\rangle$ respectively. The derivative of P_F is constant. Then the error dynamics can be written as

$$\begin{aligned} -L\frac{d\tilde{i}_{L1}}{dt} &= \tfrac{\partial(P_T+P_D)}{\partial\tilde{i}_{L1}}(\tilde{i}_{L1}, \tilde{v}_{o1}) \\ C\frac{d\tilde{v}_{o1}}{dt} &= \tfrac{\partial(P_T+P_D)}{\partial\tilde{v}_{o1}}(\tilde{i}_{L1}, \tilde{v}_{o1}) \end{aligned} \tag{4.31}$$

In order to modify the error dynamics, damping is added to the error dynamics, shown by block 4 in Fig. 4.10 as

$$-L\frac{d\tilde{i}_{L1}}{dt} = \frac{\partial(P_T + P_D + P_{Ri}^m)}{\partial\tilde{i}_{L1}}(\tilde{i}_{L1}, \tilde{v}_{o1}) \tag{4.32a}$$

$$C\frac{d\tilde{v}_{o1}}{dt} = \frac{\partial(P_T + P_D)}{\partial\tilde{v}_{o1}}(\tilde{i}_{L1}, \tilde{v}_{o1}) \tag{4.32b}$$

where $P_{Ri}^m(\tilde{i}_{L1}) = \frac{1}{2}R_i\tilde{i}_{L1}^2$ is injected dissipation and R_i is virtual injected series damping in the inductor current trajectory.

Subtracting Eqn. (4.32) from Eqn. (4.28), the closed loop dynamic could be written as

$$-L\frac{\langle i_{L1d}\rangle}{dt} = \frac{\partial(P_T + P_D + P_F)}{\partial\langle i_{L1d}\rangle}(\langle i_{L1d}\rangle, \langle v_{o1d}\rangle) - \frac{\partial P_{Ri}^m(\tilde{i}_{L1})}{\partial\tilde{i}_{L1}} \tag{4.33a}$$

$$C\frac{d\langle v_{o1d}\rangle}{dt} = \frac{\partial(P_T + P_D + P_F)}{\partial\langle v_{o1d}\rangle}(\langle i_{L1d}\rangle, \langle v_{o1d}\rangle) \tag{4.33b}$$

Replacing $\langle i_{L1}\rangle$, $\langle v_{o1}\rangle$ with $\langle i_{L1d}\rangle$, $\langle v_{o1d}\rangle$ in Eqn. (4.26), the mixed potential function

to describe desired trajectory is derived as

$$\begin{aligned} P(\langle i_{L1d}\rangle, \langle v_{o1d}\rangle) &= P_T(\langle i_{L1d}\rangle, \langle v_{o1d}\rangle) + P_D(\langle i_{L1d}\rangle, \langle v_{o1d}\rangle) + P_F(\langle i_{L1d}\rangle, \langle v_{o1d}\rangle) \\ &= (\langle i_{L1d}\rangle \frac{1-D}{n} \langle v_{o1d}\rangle) \\ &\quad + (\frac{1}{2}\langle i_{L1d}\rangle^2 r_{L1} - G_{o1d}\frac{\langle v_{o1}\rangle^2}{2}) \\ &\quad + (-V_g \cdot \langle i_{L1d}\rangle - 0) \end{aligned} \tag{4.34}$$

Inserting Eqn. (4.34) into Eqn. (4.33), the closed loop system dynamic response will be

$$-L\frac{\langle i_{L1d}\rangle}{dt} = \frac{\langle v_{o1d}\rangle(1-D)}{n} + \langle i_{L1d}\rangle r_{L1} - V_g - R_i\tilde{i}_{L1} \tag{4.35a}$$

$$C\frac{d\langle v_{o1d}\rangle}{dt} = \frac{\langle i_{L1d}\rangle(1-D)}{n} - G_{o1}\langle v_{o1d}\rangle \tag{4.35b}$$

By subtracting Eqn. (4.35) from Eqn. (4.27), the error dynamic can be described as

$$-L\frac{d\tilde{i}_{L1}}{dt} = \tilde{v}_{o1}\frac{1-D}{n} + r_{L1}\tilde{i}_{L1} + R_i\tilde{i}_{L1} \tag{4.36a}$$

$$C\frac{d\tilde{v}_{o1}}{dt} = \tilde{i}_{L1}\frac{1-D}{n} - G_{o1}\tilde{v}_{o1} \tag{4.36b}$$

By shaping the energy of the auxiliary system to achieve a desired trajectory, the control function for the actual system can be derived.

4.5.1 Determining control variable for PBC with series injection

In applications where a constant DC voltage source is needed, the ideal desired trajectory of the output voltage should remain constant under all conditions. Hence to obtain this control objective, let $\frac{d\langle i_{L1d}\rangle}{dt}$ in Eqn. (4.35) equal to zero and the desirable voltage $\langle v_{o1d}\rangle$ equal to the fixed reference V_{o1}^* in Eqn. (4.35), then

$$V_{o1}^*\frac{(1-D)}{n} + \langle i_{L1d}\rangle r_{L1} - V_g - R_i\tilde{i}_{L1} = 0 \tag{4.37a}$$

$$\langle i_{L1d}\rangle\frac{(1-D)}{n} - G_{o1}V_{o1}^* = 0 \tag{4.37b}$$

Solving equation in Eqn. (4.37b), the desired inductor current $\langle i_{L1d}\rangle$ is

$$\langle i_{L1d}\rangle = \frac{nG_{o1}V_{o1}^*}{(1-D)} \tag{4.38}$$

Replacing $\tilde{i}_{L1} = \langle i_{L1}\rangle - \langle i_{L1d}\rangle$ in equation Eqn. (4.37a), it becomes

$$\frac{V_{o1}^*(1-D)}{n} + (r_{L1}+R_i)\langle i_{L1d}\rangle - V_g - R_i\langle i_{L1}\rangle = 0 \tag{4.39}$$

Inserting Eqn. (4.38) in Eqn. (4.39),

$$V_{o1}^*\frac{(1-D)^2}{n^2} - (V_g + R_i\langle i_{L1}\rangle)\frac{1-D}{n} + (r_{L1}+R_i)G_{o1}V_{o1}^* = 0 \tag{4.40}$$

Solving Eqn. (4.40) for duty ratio,

$$D_{PBC} = 1 - n\left[\frac{(V_g + R_i\langle i_{L1}\rangle)}{2V_{o1}^*} \pm \sqrt{\frac{(V_g + R_i\langle i_{L1}\rangle)^2}{4V_{o1}^{*2}} - (R_i + r_{L1})G_{o1}}\right] \tag{4.41}$$

The realizable expression for duty ratio is obtained as

$$D_{PBC} = 1 - n\left[\frac{(V_g + R_i\langle i_{L1}\rangle)}{2V_{o1}^*} + \sqrt{\frac{(V_g + R_i\langle i_{L1}\rangle)^2}{4V_{o1}^{*2}} - (R_i + r_{L1})G_{o1}}\right] \quad (4.42)$$

4.5.2 Stability of PBC controller

To this end a positive definite function PD is constructed as

$$PD = \frac{1}{2}L\tilde{i}_{L1}^2 + \frac{1}{2}C\tilde{v}_{o1}^2 \quad (4.43)$$

From above, $PD = 0$ only when $\tilde{i}_{L1} = 0$ and $\tilde{v}_{o1} = 0$, or else $PD > 0$. The derivative of PD is

$$\dot{PD} = L\dot{\tilde{i}}_{L1} * \tilde{i}_{L1} + C\dot{\tilde{v}}_{o1} * \tilde{v}_{o1} \quad (4.44)$$

From error dynamic equation Eqn. (4.36), $L\dot{\tilde{i}}_{L1}$ and $C\dot{\tilde{v}}_{o1}$ can be represented as

$$L\dot{\tilde{i}}_{L1} = -\tilde{v}_{o1}\frac{1-D}{n} - (r_{L1} + R_i)\tilde{i}_{L1} \quad (4.45a)$$

$$C\dot{\tilde{v}}_{o1} = \tilde{i}_{L1}\frac{1-D}{n} - G_{o1}\tilde{v}_{o1} \quad (4.45b)$$

Then inserting Eqn. (4.45) to Eqn. (4.44), the derivative of PD is

$$\dot{PD} = -(r_{L1} + R_i)\tilde{i}_{L1}^2 - G_{o1}\tilde{v}_{o1}^2 < 0 \quad (4.46)$$

In practical circuit, $r_{L1} > 0$, $G_{o1} > 0$ and damping injection R_i is also greater than zero. Then from Eqn. (4.46), the $\dot{PD}$ is always negative unless $\tilde{i}_{L1} = 0$ and $\tilde{v}_{o1} = 0$. Eqn. (4.43) and Eqn. (4.46) show the system is always stable when PBC controller is implemented. This is one of the advantages of using PBC controller.

4.5.3 Tuning the PBC controller

The duty ratio is a nonlinear function of various state variables. In this section the influence of the series injected damping on the duty ratio is studied.

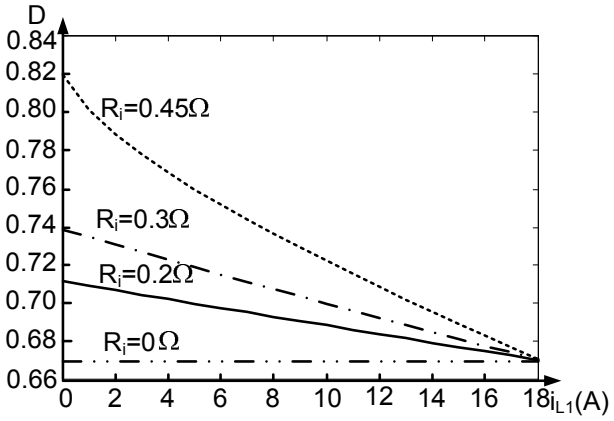


Figure 4.11: D vs i_{L1} under various R_i

The selection of R_i will influence the variation of duty ratio. Based on Eqn (4.42), Fig. 4.11 shows relationship between the control variable D and inductor current i_{L1} under various R_i when V_g=33V, V_{o1}^*=200V, G_{o1}=0.015G, $r_{L1} = 0\Omega$ and n=2. From Fig. 4.11, the higher the R_i, the larger the variation in duty ratio for the current.

The maximum R_i is limited to a value that ensures that the expression under the square root in Eqn. (4.42) is positive and hence produces a real value of duty ratio. Therefore, for any input inductor current i_{L1}, R_i has to satisfy the condition

$$R_i < \frac{V_g^2}{4V_{o1}^{*2}G_{o1}} - r_{L1} \tag{4.47}$$

To ensure R_i is satisfies the condition Eqn. (4.47) under all the load conditions, we need to ensure that condition Eqn. (4.47) is true under maximum load G_{o1}^{max}.

Replacing $P_{o1}^{max} = V_{o1}^{*2} G_{o1}^{max}$ in Eqn. (4.47). The maximum R_i is determined as

$$R_i^{max} = \frac{V_g^2}{4P_{o1}^{max}} - r_{L1} \tag{4.48}$$

From reference [40], the minimum R_i to ensure a reasonable response in overshoot and settling-time, has to be

$$\begin{aligned} R_i^{min} &= \frac{1-D}{n}\sqrt{\frac{L_1}{C_1}} \\ &= \frac{V_g}{V_{o1}^*}\sqrt{\frac{L_1}{C_1}} \end{aligned} \tag{4.49}$$

Here $(1-D)/n$ is the ratio between input and output voltage for one CFFB converter.

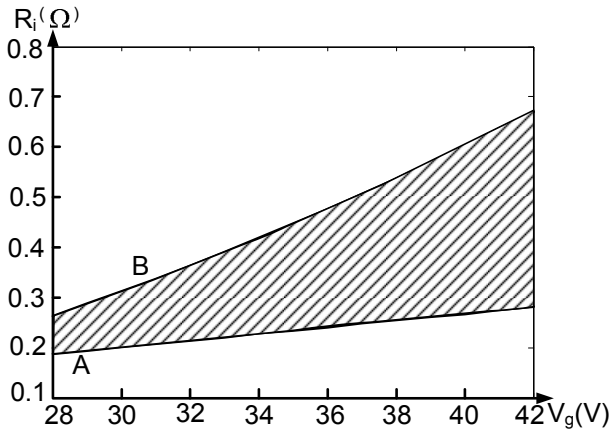


Figure 4.12: Selection of R_i when V_g ranges from 28V to 42V

Fig. 4.12 curve A shows the lower boundary R_i as Eqn. (4.49) when input voltage changes from 28V to 42V. While curve B represents the upper boundary of R_i as given by Eqn. (4.48) when $r_{L1} = 64m\Omega$ and $P_{o1}^{max} = 600W$ under the same input voltage variation. The relation given here is in terms of single CFFB. From Fig. 4.12, higher damping injection, R_i, is required for higher values of input voltage, V_g .

From Eqn. (4.42), the duty ratio is a function of load conductance G_{o1} and it will change with load current. Hence, it is necessary to measure the load current to determine the change in G_{o1}. As the system model does not include all the parasitic elements, the duty ratio generated by Eqn. (4.42) is not sufficient to produce accurate current trajectory. Hence, the output voltage will have a steady state error after a change in load. Hence, in case of parameter variation, PBC with the series damping alone is not able to regulate the output voltage accurately.

4.5.4 Augmented integral action for zero steady state error

Control diagram with augmented integrator and load estimator is shown in Fig. 4.13.

To achieve zero steady state error when circuit parameters are not known accurately, an integral action is added. The proposed control schematic is shown as Fig. 4.13, there are two CFFB converters in one ICFFB system. Therefore two

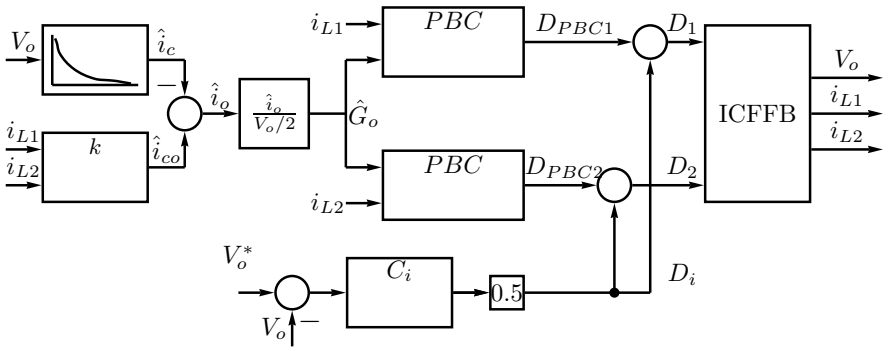


Figure 4.13: Control block for proposed PBC with augmented integrator and load estimator

PBC controllers are shown in Fig. 4.13. Each CFFB converter supplies half the output voltage V_o. To overcome the steady state error, an augmented integrator block C_i is designed as

$$D_i = (1/2) \int K_i (V_o^* - V_o) dt \tag{4.50}$$

Since the function of this integrator is to compensate the steady state error, the K_i has to be kept to a small value such that its contribution to the total duty ratio is always within 10% of its steady state value.

As mentioned in previous section, the PBC controller requires load information. By measuring the load current i_o and output voltage V_o, the equivalent load conductance for each CFFB converter is

$$G_{o1}(t) = \frac{i_o}{V_o/2} \tag{4.51}$$

To this end, external load measurement [41] or a parameter adaption scheme [39] can be used.

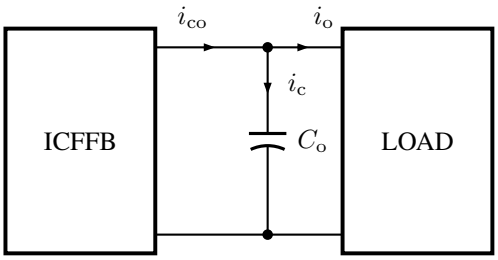


Figure 4.14: Dynamic load equivalent circuit

If load measurement is not available, it can be estimated using the system in Fig. 4.14. From Fig. 4.14, the load current i_o is represented as

$$i_o(t) = i_{co}(t) - i_c(t) \tag{4.52}$$

where the i_{co} is the current output of the converter and i_c is capacitor current. The estimated current output of the converter i_{co} is calculated by multiplying the input current i_g with the steady state current ratio k.

From [31], the voltage ratio of the ICFFB converter is

$$\frac{V_o}{V_g} = \frac{2n}{1-D} \tag{4.53}$$

In the ICFFB case, $n = 2$. Assuming a negligible loss within converter, the steady state current ratio k is

$$k = \frac{i_g}{i_o} = \frac{1-D}{2n} \tag{4.54}$$

Therefore the estimated current from the converter is

$$\hat{i}_{co} = (i_{L1} + i_{L2}) \times k \tag{4.55}$$

In addition, the capacitor current i_c is calculated by differentiating the output voltage. However, the differentiation will introduce noise. Therefore, a low pass filter is introduced to attenuate the undesirable noise. The filter transfer function between the estimated capacitor current and the capacitor voltage is:

$$O(s) = \frac{k_d s}{1 + T_i s} \tag{4.56}$$

where the $T_i = 1/2\pi f_c$ and $k_d = C$ and f_c is the cutoff frequency of the low pass filter. The high value of f_c will help to capture the fast change in capacitor current, but it will also allow higher value of noise to go through. Based on the estimated load current $\hat{i}_o(t)$ and the measurable output voltage V_o, the estimated load becomes

$$\hat{G}_{o1}(t) = \frac{\hat{i}_o(t)}{V_o/2} \tag{4.57}$$

4.6 Experimental results and discussion

A 1.2 kW ICFFB converter with switching frequency 10kHz has been built. The detailed design of the converter is described in our earlier work [31]. The control system shown in Fig. 4.13 has been implemented on the dSPACE 1104 platform, where the PBC control is computed at each switching period.

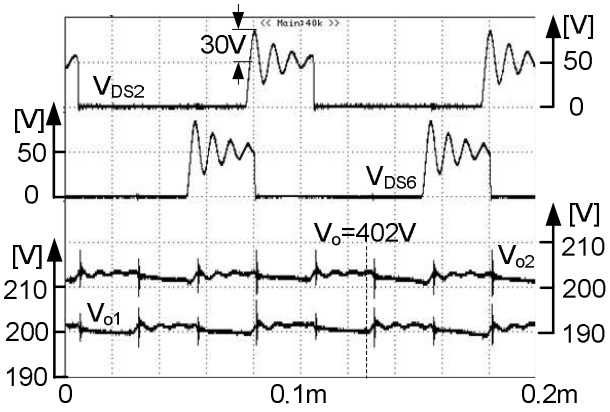


Figure 4.15: Voltage waveforms measured in the ICFFB system

Fig. 4.15 shows voltage waveforms measured in the ICFFB converter. The upper traces show V_{DS} across the two MOSFETS and lower traces show the output voltage of each CFFB V_{o1} and V_{o2}. The waveforms shows the maximum 2V difference between V_{o1} and V_{o2} when output voltage V_o=402V.

Since the current through the transformer is interrupted, the energy stored in the stray inductance of the transformer will produce over-voltage. Due to the snubber capacitance C_s connected across the DC bus, refer to Fig. 4.5, the voltage across the switch is limited and is shown in upper two traces of Fig. 4.15. The upper traces show the overshoot in the switches S_2 and S_6 when $V_g = 30V$, $V_o = 402V$, P_o=600W and D_1=D_2=0.7.

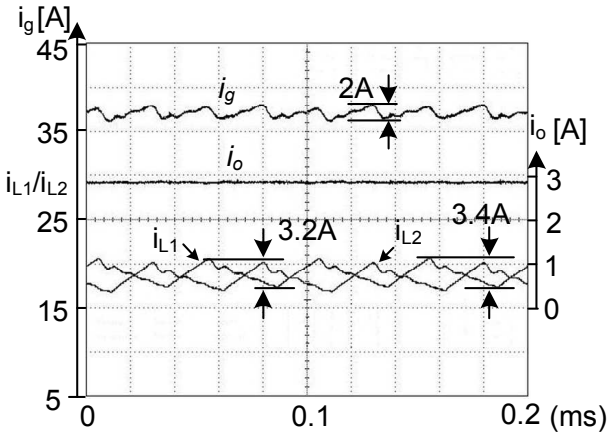


Figure 4.16: Steady state current waveforms of the ICFFB converter

Fig. 4.16 displays the individual CFFB inductor current ripples in i_{L1} and i_{L2} to be about 20% of their rated inductor current. On the other hand, due to interleaving, the ripple in the input current i_g is reduced to 5% of the rated input current. This results verify that the interleaved modulation minimizes current ripples. Moreover, the paralleling at the input reduces the current rating of input devices.

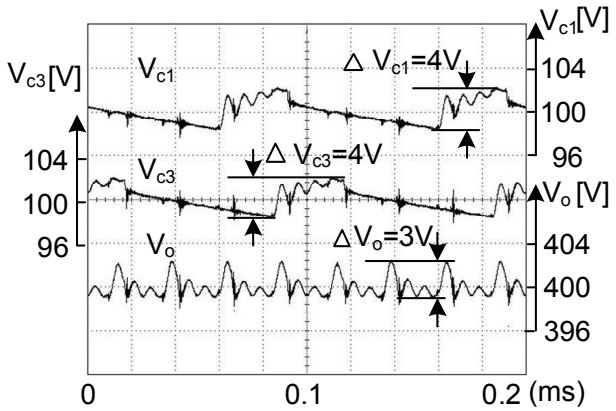


Figure 4.17: Steady state voltage waveforms of the ICFFB converter

Fig. 4.17 shows the ripple in the output voltage. The upper traces are capacitor voltages V_{c1} and V_{c3} and the trace at the bottom is the total output voltage V_o. The ripple in individual capacitor is 4V, which is 4%. In contrast, the voltage ripple in total output voltage has the amplitude about 3V, which is just 0.75% of the rated voltage.

To understand the contribution of PBC controller and voltage integrator, the ICFFB system is tested at input voltage 24V while the output voltage is regulated at 300V. However, to demonstrate the effectiveness of PBC controller, the input voltage is changed from 18V to 30V while the output voltage is regulated at 300V. The resulting duty ratio changes from 0.6 to 0.72. Under these conditions, the variation range is sufficient to verify the controller's effectiveness in wide operation. Hence the proposed converter and controller can be used in applications where a variable DC source voltage, such as in Fuel Cell stack and PV, has to be boosted an regulated at a high value of DC voltage.

Fig. 4.18 to Fig. 4.20 plot the input current i_g, output current i_o, input voltage V_g and output voltage V_o when load power changes between 360W and 720W.

Fig. 4.18 are the results when series damping PBC is applied. Damping injection $R_i = 0.4$ is used during experiment. There is 18V steady state error in the output voltage due to the inaccurate modeling.

Fig. 4.19 show the steady state error in the output voltage is canceled when

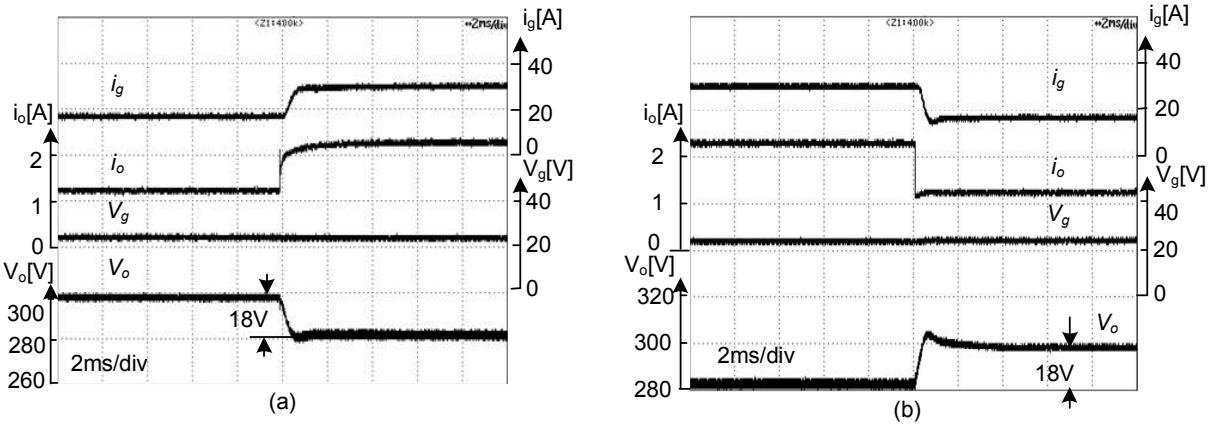


Figure 4.18: Step responses under series damping PBC alone

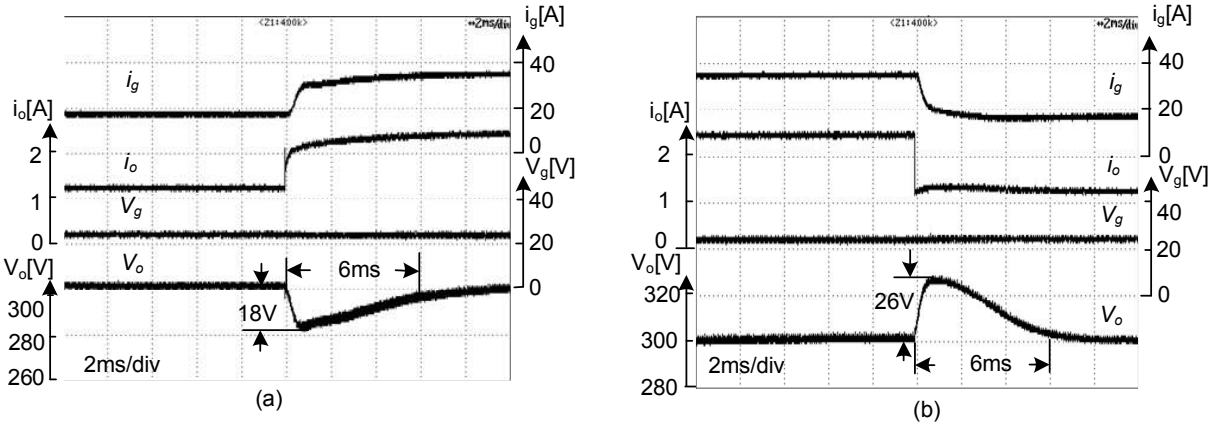


Figure 4.19: Step responses under integrator augmented PBC with measured load voltage integrator with K_i=0.5 is used.

Fig. 4.20 are achieved when proposed integrator augmented PBC controller with load estimated scheme is used. The regulation is poorer as the bandwidth of load estimation is limited due to the low pass filter. In this chapter, the implementation of PBC to ICFFB system is explored. The load estimator is not the main focus of this chapter.

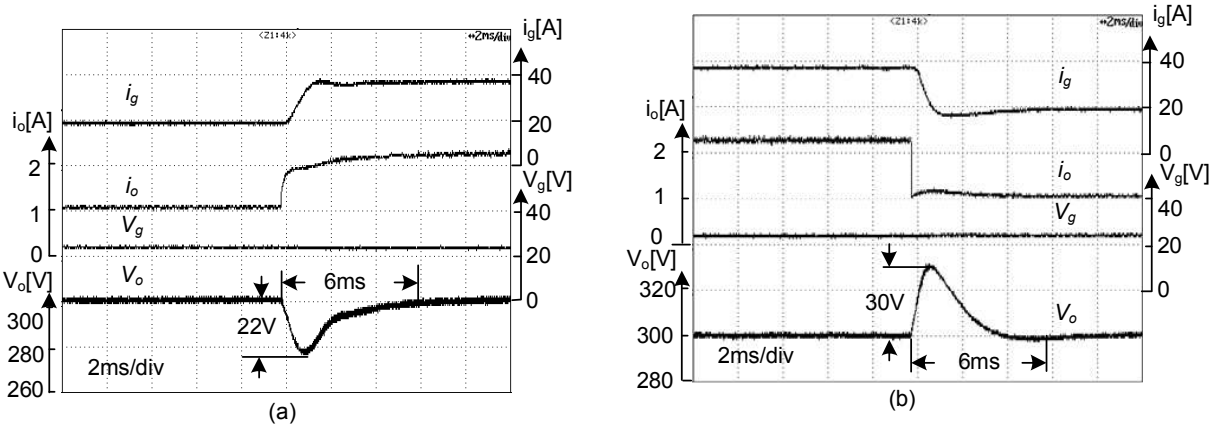


Figure 4.20: Step responses under integrator augmented PBC with estimated load

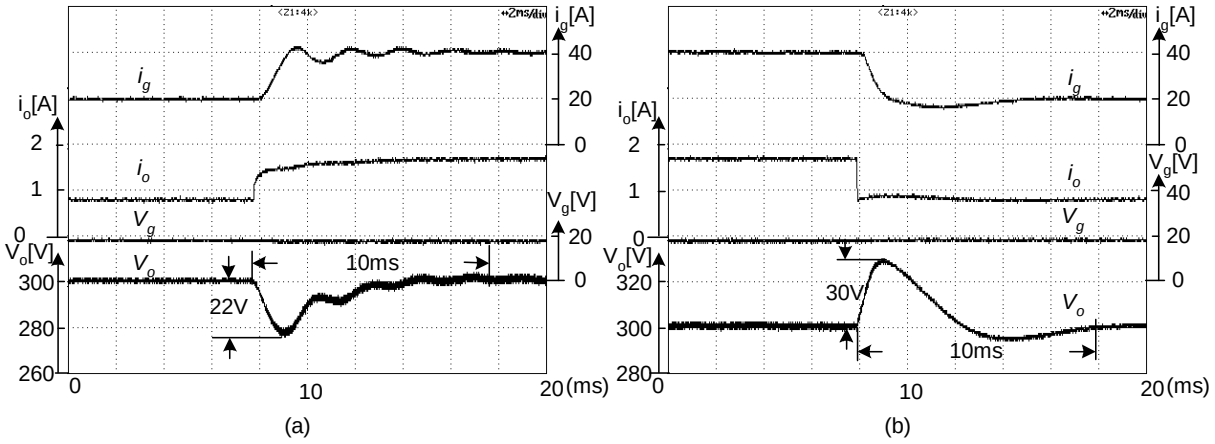


Figure 4.21: Waveforms when V_g=18V and P_o=270W to 540W

In order to verify that the proposed controller is able to function well under wide variations of voltage and output power for application requirements, Fig. 4.21 to Fig. 4.23 illustrate the system step response when the input voltage changes from 18V to 30V and the load power varying from 270W to 900W.

Table. 4.1 records the parameters used for the experimental testing.

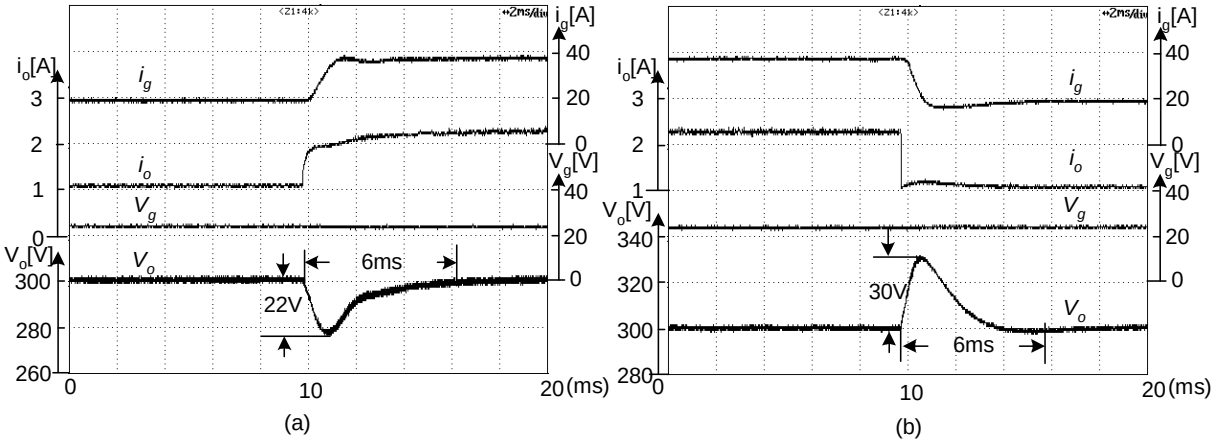


Figure 4.22: Waveforms when V_g=24V and P_o=360W to 720W

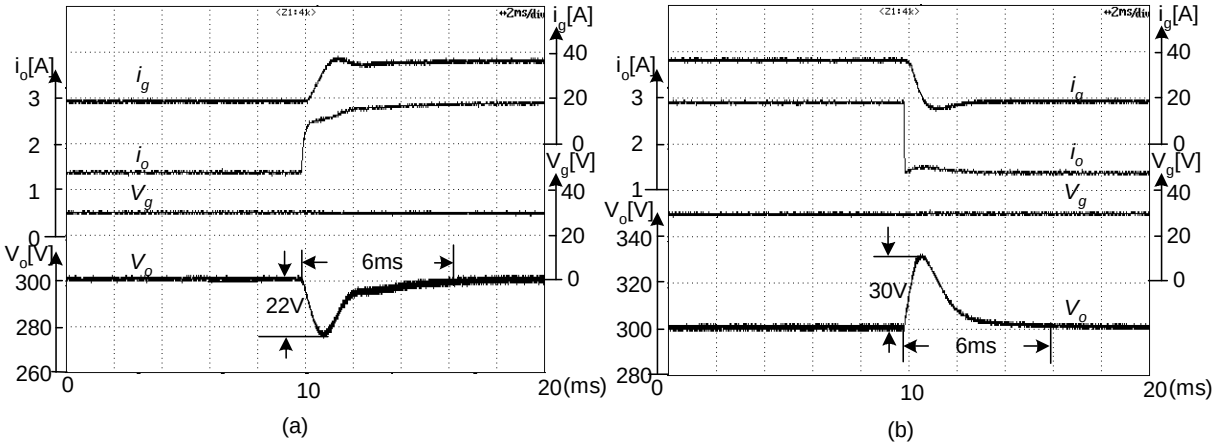


Figure 4.23: Waveforms when V_g=30V and P_o=450W to 900W

Table 4.1: Parameters of controller implementation

f_c	Estimator cutoff frequency	2 kHz
f_s	Sampling frequency	10 kHz
K_i	Integrator gain	0.5

4.7 Controller performance discussion

Though proposed augmented PBC is able to achieve stability under wide operating range. However, it is still interesting to compare its performances with conventional PI controllers. Two controller are investigated here: direct voltage mode control and cascaded current mode control. The controller would be derived according to the following three basic guidelines: 1) phase margin at least 60 degree 2) gain margin at least 10dB and 3) as fast dynamic response as possible [26][42]. Since, the transfer function is derived by linearizing one operating point, the dynamic performance is only evaluated under one operating point, which is V_g=33V, V_o=400V, D=0.67 and R=133.3Ω, L=178.8μH, C=100μF and r_L=64 $m\Omega$.

4.7.1 Direct voltage control

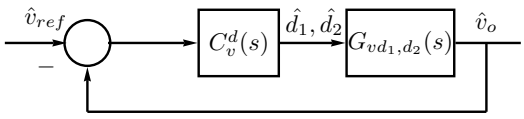


Figure 4.24: Control diagram of direct voltage control

The control diagram for direct voltage control is shown in Fig. 4.24. The transfer function between the output voltage and the control variable duty ratio is

$$G_{vd_1,d_2} = \frac{-2n^2V_o(r_L + Ls) + V_o(1-D)^2R_o}{[2(1-D)^2R_o + n^2(r_L + Ls)(4 + CR_os)](1-D)} \tag{4.58}$$

The PI controller in form as

$$C_v^d = k_p^d + k_i^d \frac{1}{s} \tag{4.59}$$

is designed. This controller has crossover frequency 10Hz, phase margin 80^o and gain margin 12dB. The bode diagram of compensated system is shown in Fig. 4.25 (a).

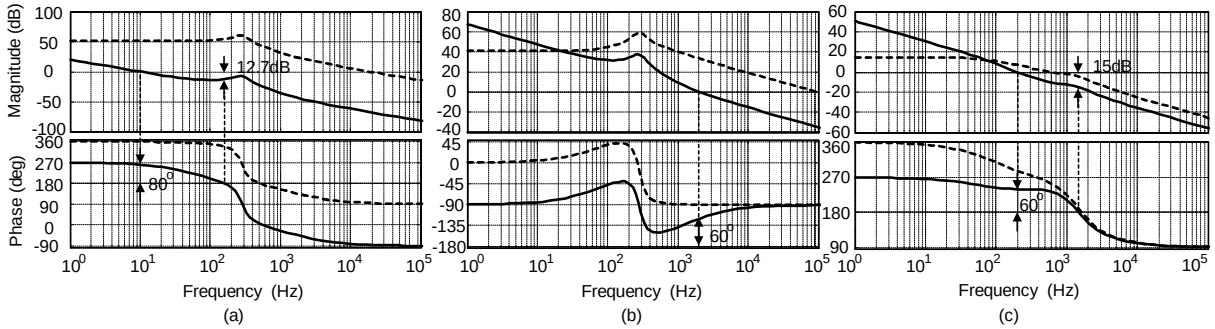


Figure 4.25: Bode diagram (a) Direct voltage control

Cascaded current control: (b)inner current loop (c)outer voltage current loop

Here solid line and dashed line in Fig. 4.25 represent open loop and closed loop transfer function respectively.

4.7.2 Cascaded current control

The control diagram of cascaded current control implemented in [31] is shown in Fig. 4.26. The inner loop transfer function between inductor current and the duty ratio is

$$G_{id_{1,2}} = \frac{n(8 + CR_o s)V_o}{2(2(1-D)^2 R_o + n^2(r_L + Ls)(4 + CR_o s))} \tag{4.60}$$

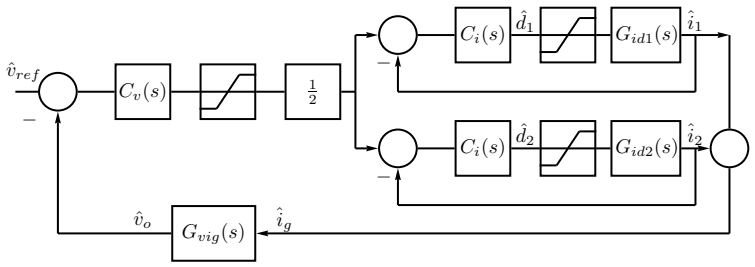


Figure 4.26: Control diagram of cascaded current control

While the transfer function between the output voltage and the input current is

$$G_{vig} = \frac{-4n(r_L + Ls) + 2(1-D)^2 R_o/n}{(1-D)(8 + CR_o s)} \tag{4.61}$$

The PI controller in the same form as Eqn. (4.59) for both inner current loop and outer voltage loop are derived. The bode diagram of the compensated system is shown in Fig 4.25 (b)(c). For inner current loop, the open loop G_{id1} has crossover frequency 100kHz while infinite gain margin and 90 degree phase margin. To sufficiently filter out the switching ripple which is 10kHz, crossover frequency of the compensated system is selected as 2kHz (Fig. 4.25 (b)). For the outer voltage loop, crossover frequency is selected as 200Hz. Above this frequency, the gain margin would be lower than 10dB. Low gain margin would cause system easily become unstable while system parameters varied.

4.7.3 Performance comparison and discussion

The simulations are carried out in SIMPLORER. The step responses under three different control schemes are shown in Fig. 4.27. To be consistent, the input

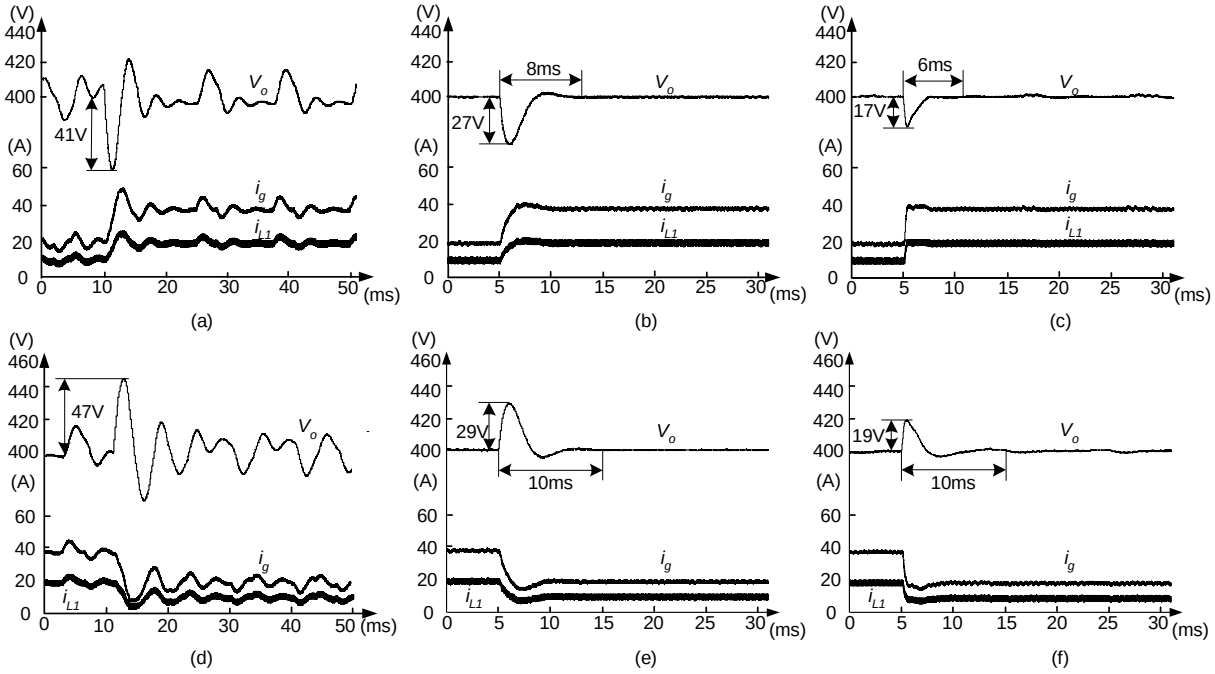


Figure 4.27: Comparison of step response between 600W and 1200W

(a)(d) Direct voltage (b)(e) Cascaded current (c)(f) PBC with integrator

voltage is maintained at 33V and load is varied between 600W to 1200W through out the testing. The control objective is to regulate the output voltage at 400V. From Fig. 4.27 (a)(d), the direct voltage control has the poorest dynamic response. There are 41V undershoot during step up operation while 47V overshoot under step down. It contains large variations during steady state both in input inductor and output voltage. The cascaded current control (Fig. 4.27 (b)(e)) and the proposed augmented PBC control (Fig. 4.27 (c)(f)) have similar settling time. The cascaded current control and PBC perform well. The differences are proposed augmented PBC scheme has lower overshoot and undershoot during transient. This is due to the current responses are faster in the proposed scheme.

Based on single point performance comparison, following conclusions are made (1) Non-minimum phase relationship between the control variable and output voltage still exists (2)Using series damping can bypass the non-minimum phase relationship (3) Nevertheless, PBC achieves stable operating under wide range.

4.8 Discussion and conclusion

In this chapter, the implementation of passivity based controller for Interleaved Current Fed Full Bridge (ICFFB) converter has been investigated. In the proposed implementation of the passivity based control, a series damping injection is used to control the inductor current trajectory. This series damping injection is like adding an additional resistance R_i in series with r_L. Thus such series injection influences the dynamics of the current to duty ratio transfer function given in Eqn. (4.7). By not using parallel damping injection, the non-minimum phase loop is bypassed. The current reference is now generated using the load measurement and converter current transfer ratio and hence the rate at which the inductor current reference is built up is not dependent on the response of the voltage controller as is the case in cascaded control. Thus the rate at which the charge in output capacitor is compensated now is determined by the response of the current loop. However, this comes at the expense of load measurement. Moreover, a similar structure could also be proposed with a current control loop that uses PI controller. However, the PI controllers parameters will have to be scheduled for different operating points

for a wide range of operation.

On the other hand, passivity based control offers an energy shaping based approach that allows us to design a controller for a wide range of operation. The effect of series injection and its limits are discussed in this chapter and it provides a framework for design of controller for a wide range of operation.

Chapter 5

Dynamic power distribution in storage augmented renewable energy system

5.1 Introduction

In previous chapters, front-end converters are designed for energy storage and renewable source respectively. In this chapter, a controller to regulate the output voltage as well as to distribute the power between ultracapacitor and renewable energy is investigated.

It is known that source has to respond quickly when load varies to maintain a stable operation. Otherwise it causes downstream electronic controller to wrongly enter shutdown mode or poses difficulties for modulation in downstream DC-AC converters, as a result, system becomes instable. For commercial DC voltage sources, a maximum up to 5% voltage deviation for every 10% to 50% load step should be expected [43].

On the other hand, renewable energy has slow or intermittent nature. It may not be able to respond to load dynamic requirements. Therefore, energy storage system, when its size is properly designed, is introduced to respond fast and to supply sufficient energy so that load requirements are satisfied.

In this chapter, a fast voltage regulation controller which distributes the power between the ultracapacitor and renewable energy source is designed. In the controller design, reference signals for controllable renewable energy system , such as Fuel cell, are generated based on load information. Therefore, an accurate model describing the relationship between input and output current is also designed. For the uncontrollable renewable energy such as PV, maximum power tracking scheme is applied to generate the current reference signals. Simulation and experimental results verify that the augmented system dynamic response and voltage deviation are reduced, compared with the situation when renewable source is used alone.

This chapter is organized as follows: Section. 5.2 constructs the small signal model of ICFFB and DAB systems. Section. 5.3 proposes a control scheme

to achieve fast dynamic response in the system. Section. 5.4 discusses a system identification approach to extract the accurate model between input and output current in ICFFB converter. Simulation and experimental results are provided in Section. 5.5. Finally, Section. 5.6 concludes this chapter.

5.2 Small Signals Modeling of ICFFB and DAB converters

As mentioned in previous chapter, Interleaved Current Fed Full Bridge Converter (ICFFB) [31] has low input ripple, high voltage boost ratio and isolated nature. Thus it is a favorable front-end converter for renewable sources. Though, current-fed converter has large inrush current during startup, researchers have developed a simple way to overcome this limitation [44]. Therefore, in this chapter, ICFFB converter are investigated as front-end converter for renewable source. Here, ICFFB is redrawn at the top of Fig. 5.1.

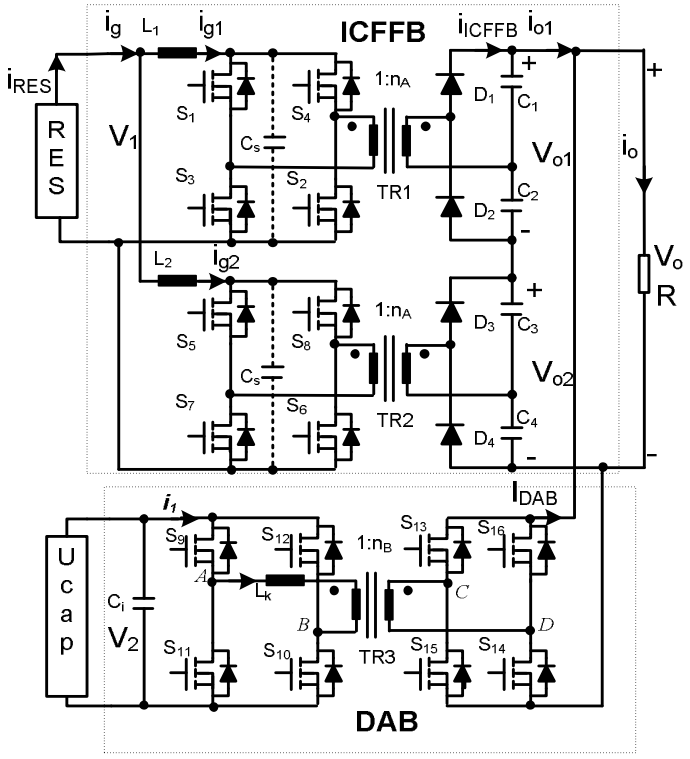


Figure 5.1: Topology of augmented system using ICFFB and DAB

In order to study the dynamic behavior of augmented system, transfer functions of the two converters using small signal analysis are developed. Applying circuit analysis and state variable averaging over switching period T_s, the dynamics of ICFFB converter can be expressed as

$$L_1 \frac{d\langle i_{g1}(t)\rangle_{T_s}}{dt} = (v_g(t) - r_1 i_{g1}) - \frac{v_o(t)}{2n_A} D' \tag{5.1}$$

$$L_2 \frac{d\langle i_{g2}(t)\rangle_{T_s}}{dt} = (v_g(t) - r_2 i_{g2}) - \frac{v_o(t)}{2n_A} D' \tag{5.2}$$

$$C_1 \frac{d\langle v_{c1}(t)\rangle_{T_s}}{dt} = C_2 \frac{d\langle v_{c2}(t)\rangle_{T_s}}{dt} = \frac{i_{g1}(t)}{n_A} D' - i_{o1} \tag{5.3}$$

$$C_3 \frac{d\langle v_{c3}(t)\rangle_{T_s}}{dt} = C_4 \frac{d\langle v_{c4}(t)\rangle_{T_s}}{dt} = \frac{i_{g2}(t)}{n_A} D' - i_{o1} \tag{5.4}$$

where L_i and r_i are input inductor and inductor series resistor respectively. V_g, V_1 and V_o are input voltage for ICFFB, input voltage for DAB and output voltage for the augmented system. n_A is ICFFB transformer turns ratio, $D' = 1 - D$ where D is the steady state duty ratio in ICFFB. To simplify the calculations, we assume that the two interleaved circuits are identical. That means $C_1 \sim C_4 = C$, $L_1 = L_2 = L$ and $r_1 = r_2 = r$. Linearizing (5.1)-(5.4) in steady state, we can get the controller to inductor current transfer function of the ICFFB converters as

$$\begin{aligned} G_{id1}(s) &= G_{id2}(s) = \frac{\hat{I}_g}{\hat{d}} \\ &= \frac{n_A(r+Ls)(8+CR_os)V_o}{2(D'R_o * a + n_A^2(r+Ls)^2(4+CR_os))} \end{aligned} \tag{5.5}$$

where $a = 2(r + Ls)$. At $V_o = 400$V, and $n_A = 2$ we obtain the transfer function of the individual CFFB converter as

$$G_{id}(s) = \frac{0.001899s^2 + 1.822s + 409.6}{3.38 \times 10^{-9}s^3 + 3.444 \times 10^{-6}s^2 + 0.0115s + 3.848} \tag{5.6}$$

The DAB average current output can be changed without any dynamic delay by changing the phase shift between the two active bridges. Hence we can write the small signal transfer function for this converter as

$$G_{iDAB} = \frac{\hat{I}_{DAB}}{\hat{\phi}} = \frac{V_1}{2L_k f_s n_B}[2 - 8\phi] \tag{5.7}$$

where ϕ is phase shift at the steady state operating point, here n_B is the transformer turns ratio in DAB.

5.3 Controller Design

In this section, a controller, which seeks to achieve fast dynamic response while distributing the power between the ultracapacitor and renewable source to maximally utilize the renewable energy, is presented. Controller stability is also investigated.

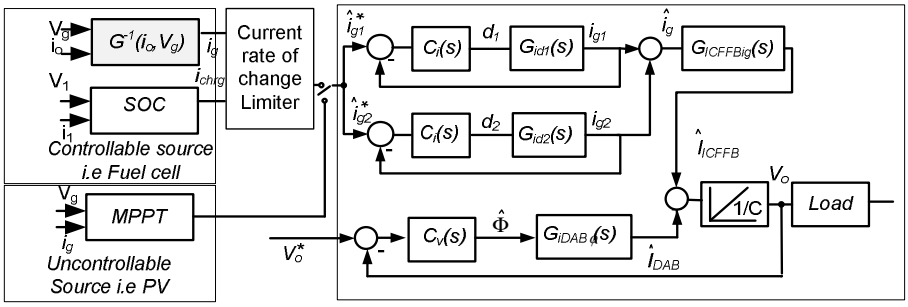


Figure 5.2: DC link voltage control scheme of the augmented system

Fig. 5.2 shows the control block diagram for the system. The control structure of the augmented system is formed as follows. The output voltage at the DC link is compared with the reference voltage and the error is fed to a PI-controller. The output of the PI-controller is the desired phase shift, $\hat{\phi}$, for the DAB converter. The output current of the DAB converter $\hat{I}_{DAB}$ adds to the output current of the ICFFB, $\hat{I}_{ICFFB}$, to charge the output capacitor.

The main objective of ICFFB controller is to use renewable energy as much as possible. There are two kinds of renewable energy source. One is controllable renewable source such as fuel cell and the other one is the uncontrolled renewable

source such as PV.

For controllable renewable source, the average output current is mostly supplied by the ICFFB converter. Hence, we use load current to generate a reference current for the ICFFB converter, as shaded block in Fig. 5.2. Since, the renewable source dynamic response can be relatively slow, a current rate of change limiter that represents how fast the source responds is included in the controller design. For instance, to avoid fuel starvation so that the membrane in fuel cell is protected, a current rate of change limiter is always used [45] [46] [47]. The rate of change can be defined during the initialization based on the specific renewable source dynamic response capability. Therefore, the reference current for the ICFFB can be designed as

$$i_g^* = Q + i_{chrg} \tag{5.8}$$

where Q is the current to match load requirements

$$Q = \begin{cases} G^{-1}(i_o(k), V_g(k)) & \frac{G^{-1}(i_o(k),V_g(k))-i_g(k-1)}{t(k)-t(k-1)} < R \\ i_g(k-1) + \frac{R}{t(k)-t(k-1)} & \frac{G^{-1}(i_o(k),V_g(k))-i_g(k-1)}{t(k)-t(k-1)} > R \end{cases}$$

R is source current rate of change limit.i_{chrg} is current to charge the ultracapacitor

and SOC is the State Of Charge to measure the availabe capacity of energy storage.

$$i_{chrg} = \begin{cases} 0 & SOC > SOC_{min} \\ min\{20, (i_g^{max} - G^{-1}(i_o, V_g))\} & SOC < SOC_{min} \end{cases}$$

Here SOC_{min} is selected as 33% of rated capacity to ensure 67% capacity can be used when the 110F, 48V ultracapacitor output voltage varies between 58% to its full rated voltage. The charge current is chosen as 20A when there are sufficient power in renewable source. Otherwise, the ultracapacitor will be charged by the difference between the maximum renewable source and load power.

For uncontrollable renewable source, the reference current for ICFFB equals maximum power that can generated by renewable source. Therefore, a maximum power point tracking (MPPT) block is included in Fig. 5.2. A flow chart to get the reference current is shown in Fig. 5.3. The initial reference current can be chosen as the half of the rated current and the step change current is set as 2% of the rated value.

The ICFFB converter then is operated in average current mode control. A PI-controller $C_i(s)$ is used to control the inductor current $\hat{I}_{g1} = \hat{I}_{g2}$. The output current of the two converters charge the output capacitor as shown in the circuit

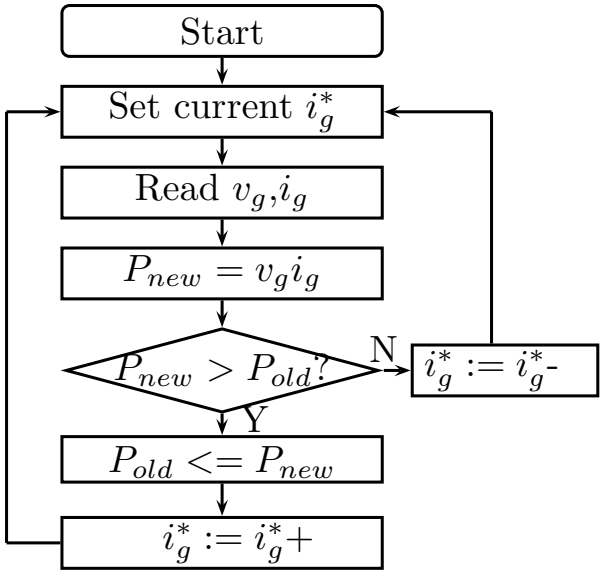


Figure 5.3: Reference current generating using maximum power point tracking technique

schematic in Fig. 5.1. This can be represented in control block diagram as

$$\hat{I}_{ICFFB} = G_{ICFFBig}\hat{I}_g = \frac{1-D}{2n_A}\hat{I}_g$$

We will first design the current controller for the ICFFB converter. The ICFFB operates at $f_s = 10$ kHz switching frequency, hence we choose the controller cut-off frequency as $f_s/10$. To design the parameters for the PI-controller we choose a phase margin of 60 degrees. This phase margin brings a 12% overshoot. Using these conditions we get the controller as

$$C_i(s) = \frac{0.008821s + 33.4}{s} \tag{5.9}$$

Once the ICFFB current controller design is available, we can write the closed

loop transfer function of the current loop as

$$G_{cig} = \frac{\hat{I}_g}{\hat{I}_g^*} = \frac{C_i G_{id}}{1 + C_i G_{id}} \tag{5.10}$$

Further we can write the relation between the input and output current of the ICFFB as

$$\begin{aligned} \hat{I}_{ICFFB} &= G_{ICFFBig}\hat{I}_g \\ &= \frac{C_i G_{id}}{R_o(1 + C_i G_{id})}\hat{V}_o \end{aligned} \tag{5.11}$$

Similarly for the DAB converter, we get

$$\hat{I}_{DAB} = G_{iDAB}C_v(\hat{V}_o^* - \hat{V}_o) \tag{5.12}$$

Using (5.11) and(5.12) we can derive the voltage output as

$$\hat{V}_o = G_{LOAD}(s)(\hat{I}_{DAB} + \hat{I}_{ICFFB}) \tag{5.13}$$

$$\begin{aligned} &= G_{LOAD}(s)G_{iDAB}C_v(s)(\hat{V}_o^* - \hat{V}_o) \\ &\quad + G_{LOAD}\frac{C_i G_{id}}{R_o(1 + C_i G_{id})}\hat{V}_o \end{aligned} \tag{5.14}$$

Hence the closed loop transfer function of the augmented system is given as

$$\frac{\hat{V}_o}{\hat{V}_o^*} = \frac{G_{LOAD}G_{iDAB}C_v(s)}{1 + G_{LOAD}G_{iDAB}C_v - \frac{G_{LOAD}C_i G_{id}}{R_o(1+C_i G_{id})}} \tag{5.15}$$

In order to design the PI-controller $C_v(s)$ to achieve the output voltage control, we reform the closed loop transfer function as shown in Fig. 5.4.

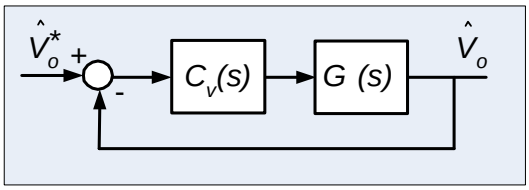


Figure 5.4: Simplified block diagram of the closed loop augmented system

We need to determine the parameters of the controller C_v as given by

$$C_v(s) = K_v \frac{1 + T_{iv}s}{T_{iv}s} \tag{5.16}$$

In order to achieve a fast response, let us restrict the range of the integral time constant to $T_{iv} = 10ms$. For the set point ($V_o = 400V$) of operation, the open loop transfer function is given as $C_v(s) \times G(s)$, where $G(s)$ is given by (5.17).

$$G(s) = \frac{9.282 \times 10^{-6}s^4 + 0.009459s^3 + 31.59s^2 + 1.057 \times 10^4 s}{4.505 \times 10^{-11}s^5 + 4.929 \times 10^{-8}s^4 + 0.00014s^3 - 0.01669s^2 - 60.62s - 1.368 \times 10^4} \tag{5.17}$$

We can verify that all the poles of G(s) lie in left-half of the s plane. To check the stability of the closed loop augmented system for different values of K_v, let us take two possible test conditions: $1/T_{iv} = 1/10^4$ and $1/T_{iv} = 1/100$. Fig. 5.5 shows the Nyquist plot of the open loop transfer function $C_v(s)G(s)$. We note that the system is stable for $K_v \epsilon [10^{-4}, 100]$. As the gain reduces, the frequency plot approaches the negative real axis reducing the phase margin.

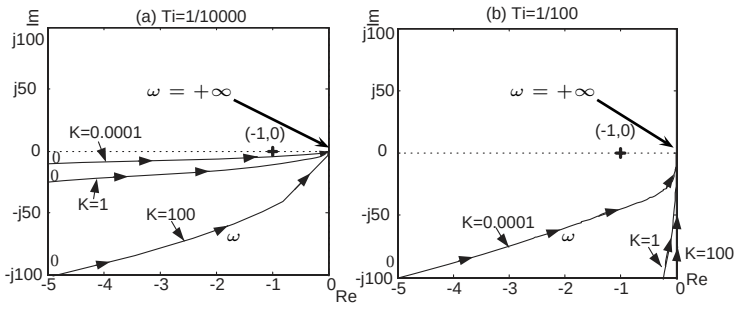


Figure 5.5: Nyquist plot of $C_v(s) \times G(s)$ for variation in control gain (K_v)

The cutoff frequency of the voltage controller $C_v(s)$ is selected to be 3 kHz and phase margin is 70 degrees. The selection of the cutoff frequency is limited by sampling period of 100μs used in the system. Therefore $C_v(s)$ is obtained as

$$C_v(s) = 0.08998 \frac{2.9309 \times 10^{-4} s + 1}{2.9309 \times 10^{-4} s} \tag{5.18}$$

The Nyquist plot of the open loop $C_v \times G(s)$ for controller designed in (5.18), Fig. 5.6, shows the system is stable.

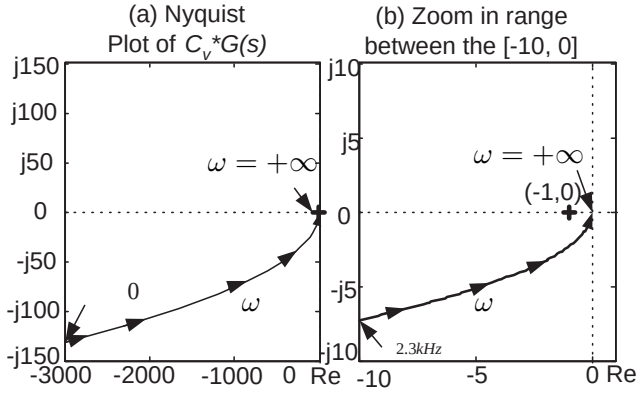


Figure 5.6: Nyquist plot for $C_v(s) \times G(s)$ using the controller $C_v(s)$

To evaluate the effectiveness of the controller, simulation is carried out in Matlab Simulink. For the uncontrollable renewable source, both input current reference step change and load step change are introduced. The simulation results is shown in Fig. 5.7 (a), the voltage V_o is well regulated when source current step changes from 50% to 100% (1.2kW is 100%) at time instant $t = 50$ms . Fig. 5.7 (b) shows detail waveform during this dynamic response. Initially, i_g increases fast while V_o reduces. This is due to the non-minimum phase relationship between control variable and output voltage. The voltage regulator senses the voltage variation so current i_{uc} is pumped out from ultracapacitor. After 20ms, both desired current for ICFFB and dc bus voltage are regulated. At $t = 100ms$, load steps from 1.5A to 3A. During this dynamic, as Fig. 5.7 (c) shows, the ultracapacitor current i_{uc} increases to meet load demand. The current from renewable source i_g remains the same because there is no change in reference current. This simulation shows the designed controller can meet source requirements as well as regulate the DC bus voltage. In addition, the MPPT block is designed to update the current reference every 20ms. Within 20ms, the current regulation is fast enough to track the current variation as shown in Fig. 5.7.

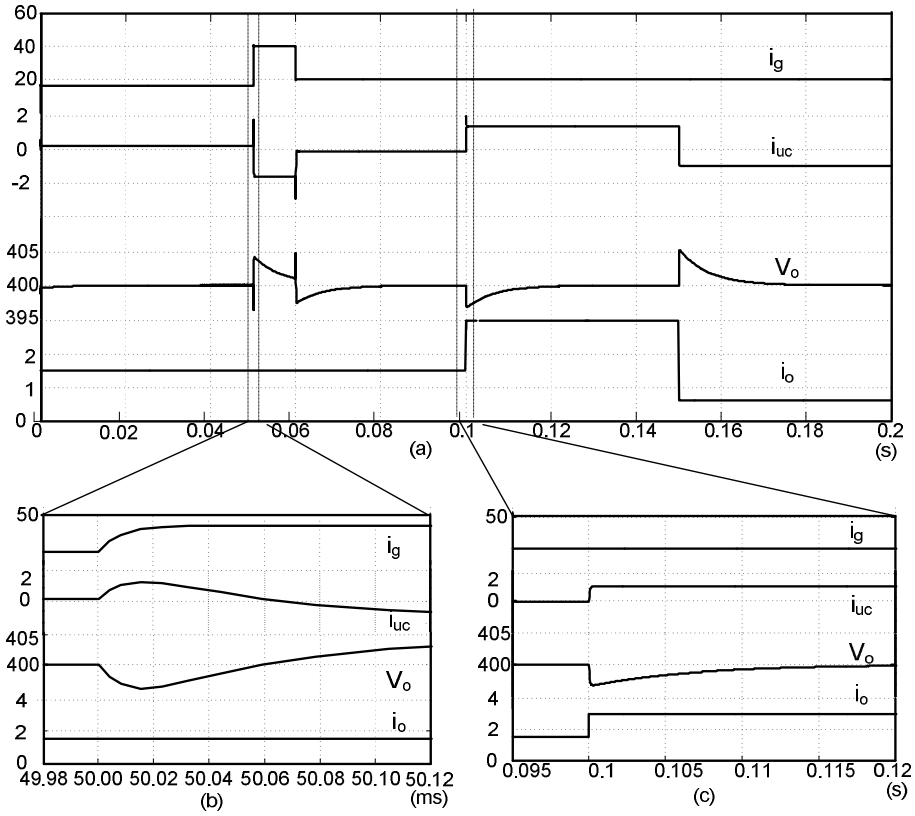


Figure 5.7: Dynamic response when when controllable source is used

5.4 Accurate Model of ICFFB converter

In our previous controller design, assuming power conservation within converter, for controllable renewable source, the reference for input current i_g can be calculated based on total output power divided by input voltage, where the total power is generated based on load information. However, this is not accurate.

This inaccurate current reference causes the power generated from the renew-

able source to fall short of the load requirements. Hence the ultracapacitor system continuously generates the mismatch power between the load and the renewable source. For instance, when load demand is 1200W and source voltage is constant, due to inaccurate current reference generating, only 85% of full load requirements 1200W is generated by renewable source. In order to match load power requirements, the rest 15% power will be supplied by the ultracapacitor system. Under this condition, the bi-directional converter connecting with ultracapacitor operates at light load. The converter has low efficiency about 30%-40%. Hence, power from ultracapacitor can be as high as 600W to output only 180W power. In conclusion, the inaccuracy of reference generating causes (1) Low efficiency in ultracapacitor system under low power operation (2) Increased charge and discharge cycles and (3) Reduced effective energy stored in the ultracapacitor to support the high power dynamic demand. To avoid this, an accurate current reference is needed.

Prior research had mainly focused on the small signal identification of the frequency domain information such that controller can be designed accordingly [48][49][50]. Some methods involve the use of equivalent circuit to model the static behavior of the converter [51][52][53]. Parasitics are modeled as equivalent series resistances (ESR) associated with the circuit components. This solution becomes complicated when large number of energy storage is used.

In this chapter, a simple accurate model is constructed and the nonlinear least square approach is utilized to obtain the correct model parameters. Compared

with other empirical modeling approaches, the nonlinear least square modeling can provide a good approximation with minimal experimental data points and is able to cover a wide range of operation [54][55].

The proposed model reduces the error from 22% to 2% compared with the ideal model. Model validation is carried out to further confirm the accurateness of proposed model. The proposed static model extraction approach is also applicable to other converters for loss analysis and relationship investigation.

5.4.1 Model identification

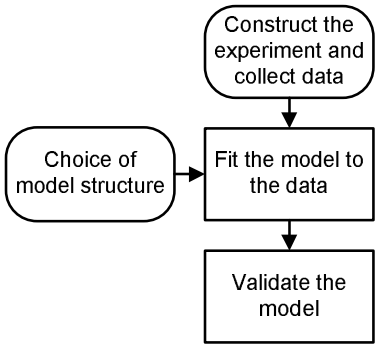


Figure 5.8: Procedures to achieve the data fitting

Fig. 5.8 shows a general procedures to extract the model [56]. The ovals blocks are the designer's main responsibility while the rectangles blocks are the computer's main responsibility. Therefore data acquisition and model selection are the two most important parts in the model identification. In the following sections we will mainly describe these four blocks, namely, data acquisition, model selection,

data fitting and model evaluation.

5.4.2 Data acquisition

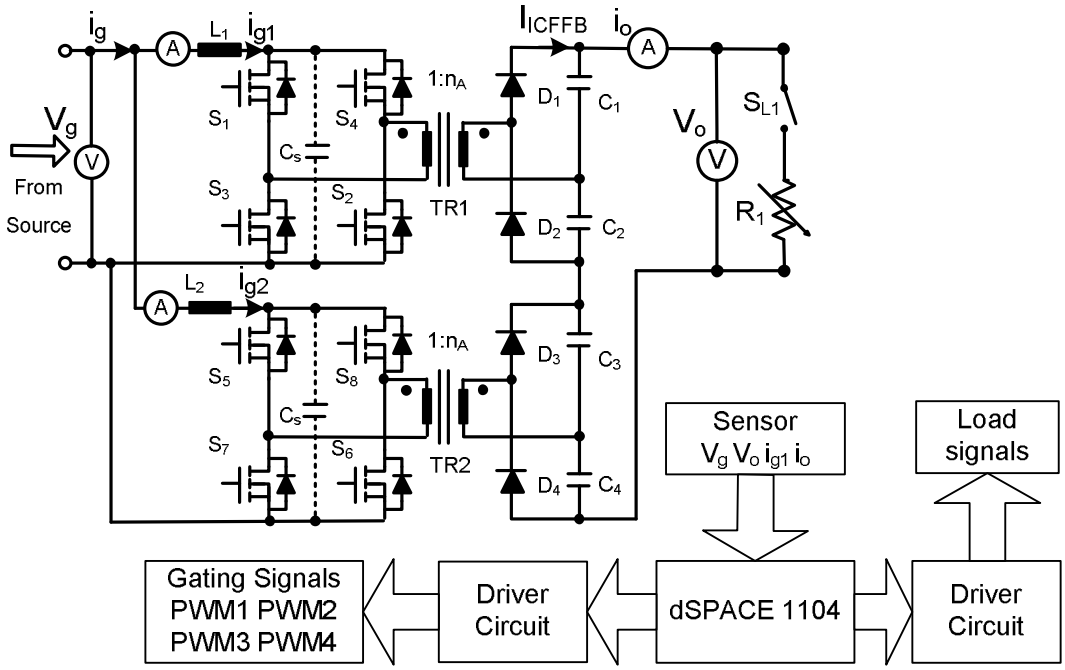


Figure 5.9: Setup for data acquisition

The objective of data acquisition is to record the experimental data (i_o, V_g, i_{g1}) at the desired output voltage 400V. These data will be used for model fitting in the next section. The experimental setup for data acquisition is shown in Fig. 5.9. In practise, data acquisition can be carried out together with quality test of converter under various loading conditions.

The flow chart of the data acquisition process is shown in Fig. 5.10. The program is implemented in dSPACE 1104. As shown in Fig. 5.10, the initial duty

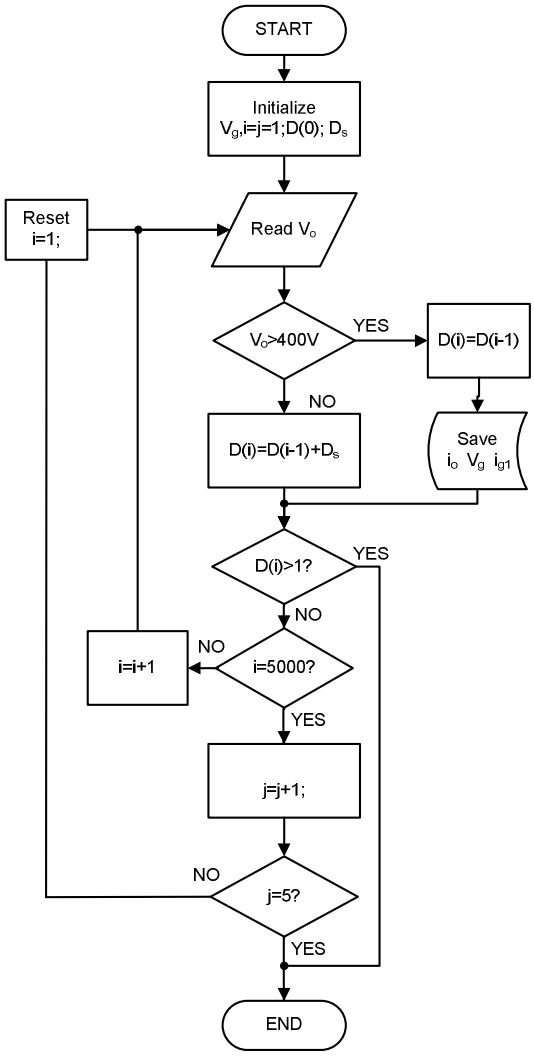


Figure 5.10: Flow chart for the data acquisition process

ratio $D(0)$ and duty step D_s are set as 0.66 and 0.001 respectively. The selection of initial duty ratio is based on the relationship between the output voltage and the maximum input voltage while the duty step is limited by the PWM resolution. The output voltage V_o is measured and fed back to the dSPACE. Every 50ms the duty ratio will be updated once. If the output voltage is higher than 400V, the duty ratio will remain unchanged. At the same time, the corresponding variable set (i_o, V_g, i_{g1}) are recorded. Otherwise, the duty ratio will increase by 0.001.

The 50ms is set to ensure that the circuit reaches steady state at each duty ratio. Because output current i_o and input voltage V_g can have different values, various data profiles are needed. In the data acquisition, load is programmed to change between 200W to 1200W. Every 5 seconds, the load will increase by 200W. The input voltage V_g is also arranged to change every 30 seconds from 27.5V to 30V with 0.5V step. The appeal of the data acquisition is its simplicity because there is no close loop used to record data. The open loop data acquisition ensures the stable system and stable operation with minimal design effort. In addition, since model extraction is carried out before controller implementation, it is better to use the open loop data acquisition approach here.

5.4.3 Model selection

In order to reach the accurate model $i_{g1} = G^{-1}(i_o, V_g)$, an appropriate model structure has to be first selected. Here model structure is chosen according to the power balance within the circuit. In the steady state, we can write

$$P_i = P_o + P_{loss} \tag{5.19}$$

Where P_i, P_o and P_{loss} are input power, output power and power loss within the converter.

Power loss can be generally divided into (1) loss proportional to the i_o^2 (i.e. conduction loss in MOSFET and copper loss in transformer); (2) loss proportional

to the i_o (i.e. diode conduction loss due to the forward voltage drop); (3) loss proportional to the $V_g i_o$ (i.e. switching loss in the MOSFET) and (4) constant power loss (i.e. core loss in the transformer etc);

Therefore the power balance equation (5.19) can be written as

$$\underbrace{V_g i_{g1}}_{P_i} = \underbrace{V_{o1} i_o}_{P_o} + \underbrace{k_1 i_o^2 + k_2 i_o + k_3 + k_4 i_o V_g}_{P_{loss}} \tag{5.20}$$

Accordingly, the inverse model $i_{g1} = G^{-1}(i_o, V_g)$ can be

$$i_{g1} = \frac{1}{V_g}(V_{o1} i_o + k_1 i_o^2 + k_2 i_o + k_3) + k_4 i_o \tag{5.21}$$

Here K=[k_1, k_2, k_3 ,k_4] are the parameters to be estimated. All these parameters have physical significance as described above. Therefore, Eqn. (5.21) can truly reflect the relationship between the input current i_{g1} and (i_o, V_g).

5.4.4 Model fitting

The model fitting objective is to find coefficients $K = [k_1, k_2, k_3, k_4]$ for model $i_{g1} = G^{-1}(i_o, V_g)$ that best fit the measured data. The problem can be represented as to find K that minimize function $F(K)$ which is

$$F(K) = \frac{1}{2} \sum_{j=1}^{n} [i_{g1}^{(j)} - G^{-1}(i_o^{(j)}, V_g^{(j)})]^2 \tag{5.22}$$

Here $i_{g1}^{(j)}$, $i_o^{(j)}$ and $V_g^{(j)}$ are the jth measured data.

To achieve the minimization problem, conventionally Newton's method and line search approach are used. However, Newton's method can only guarantee the

local convergence. In addition, the line search approach is not sufficient for n-dimensional quadratic model. On the other hand, trust region method can achieve global convergence for n-dimensional quadratic model [57]. Therefore, we use the trust region method to solve minimization problem as Eqn.(5.22).

In trust region method, a region around the current iterate is first defined based on [57].

$$\Omega_j = \{K_j : \|K - K_j\| \leq \Delta_j\} \tag{5.23}$$

where Δ_j is the radius of Ω_j, in which the model is trusted to be adequate to the objective function. And then we choose a step h_j on the general sphere where K_j is center

$$\{K_j + h \leq \Delta_j\} \tag{5.24}$$

such that the minimum of

$$L(h) = F(K_j) + h^T c_j + \frac{1}{2} h^T B_j h \tag{5.25}$$

is achieved on point of $K_j + h_j$ Here $c \in R^4$ and the $B \in R^{4\times4}$ is symmetric. Typically, the model is a second order Taylor expansion of F around K_j and $L(h)$ is an approximation to this expansion. It is generally true that such a model is good only when h is sufficiently small.

The algorithm of trust region can be summarized as Fig. 5.11.

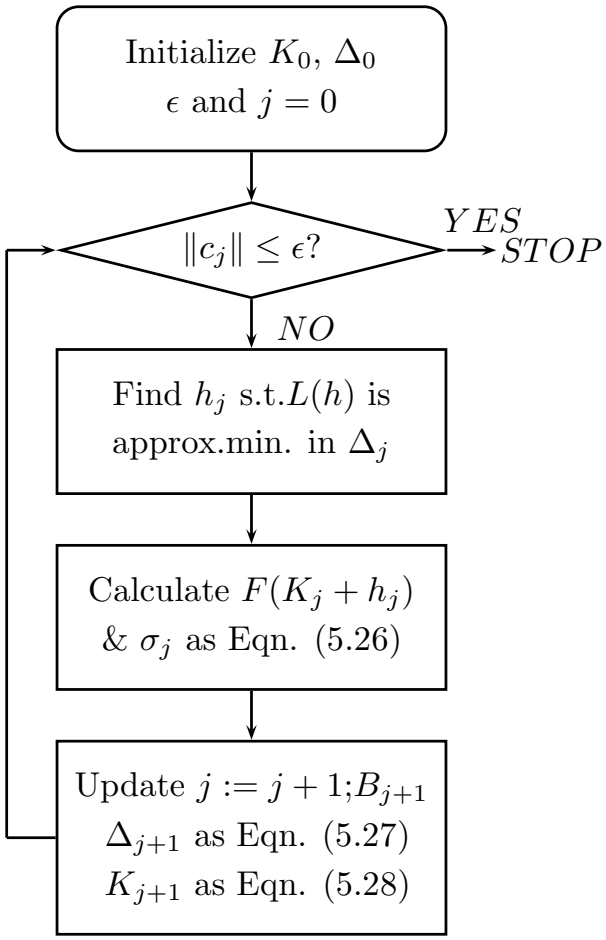


Figure 5.11: Algorithm of the trust region approach

To update Δ_j, ratio σ_j is introduced as

$$\sigma_j = \frac{F(K_j) - F(K_j + h_j)}{L(0) - L(h_j)} \tag{5.26}$$

The ratio σ plays important role in selecting new iterate K_j and updating the trust-region radius Δ_j. If σ_j is close to one, it means there is a good agreement between the approximate and the real function then the trust region can be expanded for next generation. If it is close to zero or negative, then the trust region is reduced.

Therefore, Δ_j is updated as

$$\begin{aligned} \sigma_j < 0.25 &\Rightarrow \Delta_{j+1} = \Delta_j/2 \\ 0.25 < \sigma_j < 0.75 &\Rightarrow \Delta_{j+1} = 3\Delta_j/4 \\ \sigma_j > 0.75 &\Rightarrow \Delta_{j+1} = max\{\Delta_j, 3* \parallel h_j \parallel\} \end{aligned} \tag{5.27}$$

and K_j is updated as

$$\begin{aligned} K_{j+1} &= K_j + h_j \quad if\ \sigma > 0.25 \\ K_{j+1} &= K_j \qquad otherwise \end{aligned} \tag{5.28}$$

Parameters 0.25 and 0.75 can be chosen by other values less than one. Here, these values are chosen based on [57].

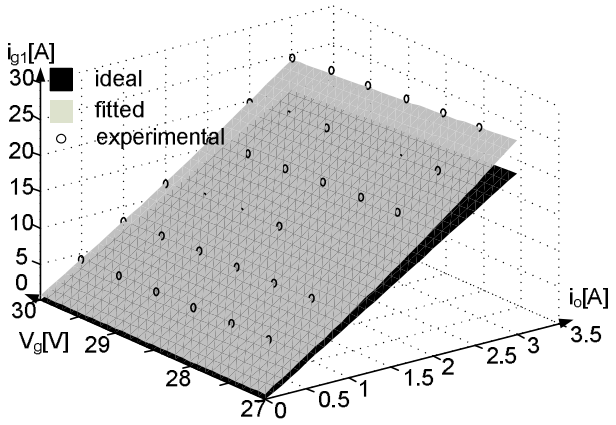


Figure 5.12: Comparison between ideal, fitted and experimental results (V_g=27 to 30V)

Based on the above mentioned algorithm, the fitted model K=[8.1694 9.2341 19.7684 0.0406] is derived. Fig. 5.12 shows the fitted model surface $G^{-1}(i_o, V_g)$ and the experimental data. The experimental data are well located on the fitted model surface. Fig. 5.13 shows the relationship between i_{g1} and i_o when input voltage is fixed under V_g=28V. Compared with the ideal model, when loss are not included,

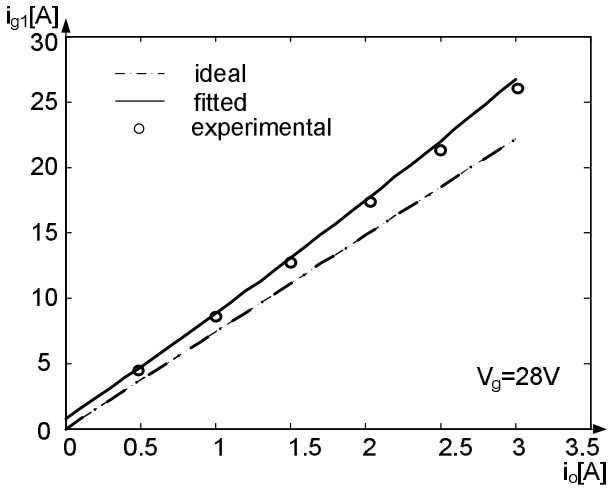


Figure 5.13: Comparison between ideal, fitted and experimental results (V_g=28V)

the fitting model is more accurate. In addition, error between the ideal model and fitted model with experimental data when V_g=28V is recorded in Table. 5.1. The calculation for error between fitted model and experimental data is based on

$$error\% = \frac{|G^{-1}(i_o^j, v_g^j) - i_g^j|}{i_g^j} \times 100\% \tag{5.29}$$

Table 5.1: Error comparison between the ideal and fitted model under V_g=28V

	200W	400W	600W	800W	1000W	1200W
ideal(%)	21.44	15.10	13.55	15.02	15.71	17.73
fitted(%)	0.13	1.20	1.96	0.59	0.64	0.62

Table. 5.1 verifies that the fitted model can represent the system accurately. The error is reduced from 21.44% to 1.96% when the fitted model is used.

5.4.5 Model evaluation

To further verify the model accuracy, more data is recorded. The load changes from power 500W to 1100W with 200W step and the input voltage changes from 27.5V to 30V with 0.5V step. By comparing the model results with the measured data via equation (5.29), the maximum 1.98% error is found in Table. 5.2. The results show that the model is able to represents the system within maximum 2% error. This 2% reference error only causes 1% DC bus voltage deviates from its rated 400V when maximum power 1200W are applied. Hence, this error is allowed without cause extra power from ultracapacitor system.

5.5 Experimental results

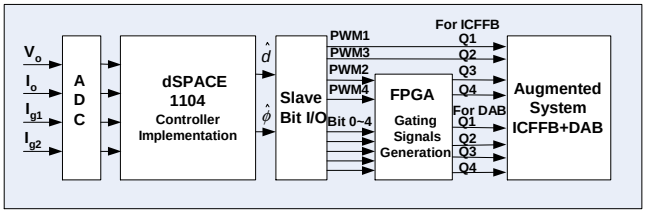


Figure 5.14: Block diagram: dSPACE implementation of the controller

The closed loop control system is implemented in the dSPACE 1104. The hardware implementation diagram is shown in Fig. 5.14. As Fig. 5.14 shows, there are four feedback signals: the output voltage V_o, the output current I_o and the two inductor current in the ICFFB; there are also two control variables: duty cycle $\hat{d}$ for

Table 5.2: Error between model and experimental results

	500W	700W	900W	1100W
Vg=27.5V	0.88%	1.70%	1.82%	1.89%
Vg=28V	0.31%	1.18%	0.64%	1.33%
Vg=28.5V	0.12%	0.06%	1.10%	1.21%
Vg=29V	0.65%	0.37%	0.41%	1.25%
Vg=29.5V	0.46%	0.37%	0.41%	1.11%
Vg=30V	1.98%	1.01%	0.26%	0.70%

ICFFB and phase shift $\hat{\phi}$ for DAB. In addition, in order to drive the MOSFETs of the DAB converter, phase shifted gating signals have to be generated. For ICFFB converter, phase shift of 90 degrees has to be added between the gating signals of the individual CFFB converter. In the ICFFB converter, variable duty ratio gating signals are used for current control. Because the dSPACE can only produce variable duty ratio PWM gating signals, a FPGA board is introduced to generate the phase shifted gating signals for both ICFFB and DAB. The ICFFB needs 90 degrees

phase shifted gating signals to drive the two converters in interleaved mode. Two channels in the PWM block are directly connected to one of the driver boards for CFFB, the other two channels are sent to the FPGA. The FPGA shifts the gating signals by 90 degrees and then sends them to the second CFFB driver board. As opposed to ICFFB's variable duty cycle control, DAB operation needs variable phase shift gating signals. A voltage controller for the DAB is implemented in the dSPACE where the control variable $\hat{\phi}$ is generated with a 5 bit resolution. Together with 2 PWM channels for the ICFFB, these 7 bits are then fed into the FPGA via a buffer. The fixed frequency gating signals for the DAB converter is preprogrammed in the FPGA. The phase shift information received from the dSPACE is used to modify the phase shift between the gating signals for the two DAB bridges.

Experimental verification are carried out using ICFFB converter and a DAB converter with parameter given in Chapter. 7. The load changes between 600W and 1200W. The rate of change in input current for ICFFB is ramped at 0.5A/ms.

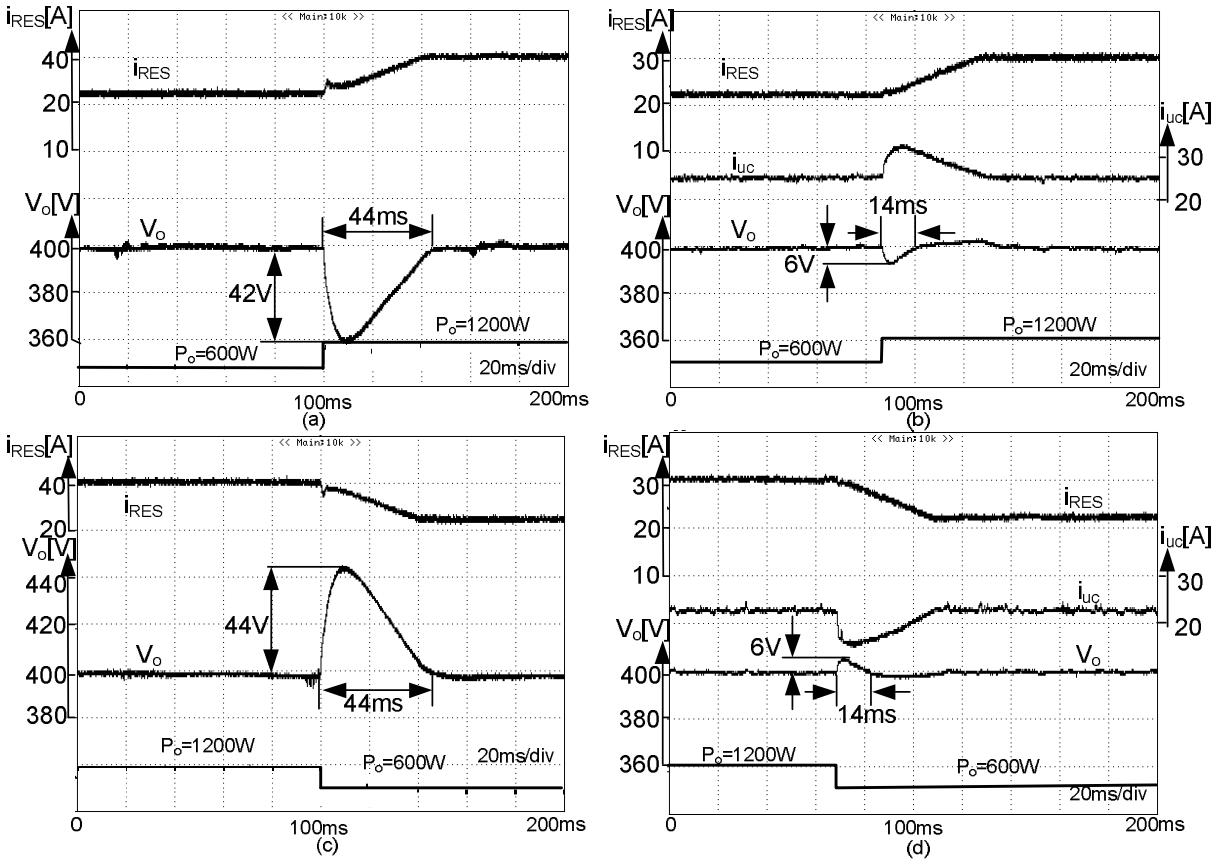


Figure 5.15: Dynamic response comparison between ICFFB alone and hybrid converter

Fig. 5.15 (a)(c) shows dynamic response of the ICFFB converter alone when load power steps between 600W and 1200W while Fig. 5.15 (b)(d) shows dynamic response of the augmented system when load power steps between 600W and 1200W.

Due to the slow response of the ICFFB converter alone, there is a big undershoots and overshoots in output voltage V_o from Fig. 5.15 (a)(c). On the contrary, when ultracapacitor is introduced, as Fig. 5.15(b)(d), the ultracapacitor current compensates the differences between load and renewable source. Hence, V_o has

very small deviation from regulated point.

5.6 Summary

In this chapter, a fast dynamic response controller, which uses ultracapacitor regulating the DC voltage and utilizes maximum power from renewable source, is implemented. To generate the accurate reference for the current loop for ICFFB, an approach to get the accurate model is proposed. The proposed model managed to reduce the error from 22% to 2% compared with the ideal model. The closed loop results show the proposed controller has improved the voltage deviation from 44% to 14% when step load is applied.

Chapter 6

Interleaved DAB Converter in Micro-Grid application

6.1 Introduction

In previous chapters, Dual Active Bridge Converter is implemented to interface ultracapacitor with load. As renewable energy are always implemented at power rating of hundred kW to MW for utilities or microgrid application, it is necessary to explore the bidirectional converter for this high power application.

As PV output is intermittent and the load can change fast, both high power and high energy density energy storages are required. Different energy storage and

their roles in the system have diverse requirements on bi-directional converters. In addition, high power switching causes large ripple at input and output side thus needs large filter to minimize the ripples.

In order to achieve high flexibility and minimum filter size, in this chapter, an interleaved modular design is used [58] [59] [60]. By properly connecting the modules in series or in parallel, various combinations are possible to meet different source and load requirements. The structure is modular so that power and energy rating of the converter can be scaled up to any level. The interleaved modulation scheme is applied to minimize the input and output ripple due to switching. Thus, it significantly reduces the size of input and output filters.

Furthermore, cascaded voltage controller is implemented to regulate the output voltage and to maintain balanced power distribution between converters.

In summary, the salient features of the proposed interleaved modular converters are

- Higher power handling capability
- Smaller filter size
- Flexible combination

This chapter is outlined as following: Section. 6.2 lists the possible com-

binations of DAB converter for different applications. Section. 6.3 describes the operating scheme of interleaved DAB converter. Section. 6.4 explains the controller design to achieve voltage regulation as well as active power sharing within each module. Section. 6.5 presents the simulation results for verification. Finally the conclusion is included in Section. 6.6.

6.2 Flexible combinations of converters

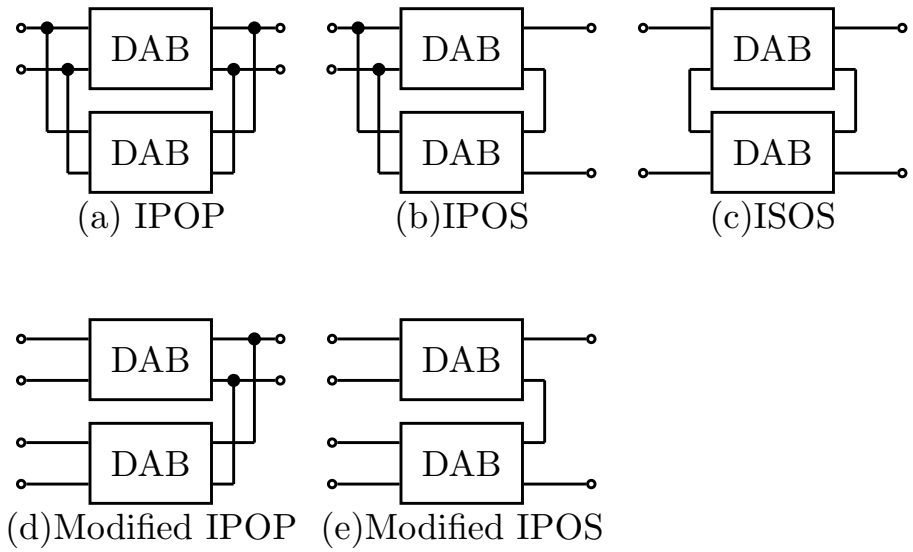


Figure 6.1: Possible configurations of module based converters

As mentioned earlier, module based design is the best approach to satisfy all the requirements of energy storage and load. The configurations of module based converter are shown in Fig. 6.1. Fig. 6.1(a) to Fig. 6.1(c) are demonstrated as possible configurations for interfacing single energy storage while Fig. 6.1(d) and

Fig. 6.1(e) are derived for connecting multiple energy storages.

Input Parallel Output Parallel (IPOP) configuration as shown in Fig. 6.1(a) shares the input and output current in modules. Therefore, it is suitable for applications where currents are relatively high both in input and output. By controlling the input current in each of the converter, the power flow in each can be controlled [61]. Fig. 6.1(d) is derived from Fig. 6.1(a) to interface multiple sources. Similar to IPOP, by controlling input current of individual converter, power flow control in energy storages is achieved. This is also a common topology in connecting multiple sources [62].

Input Parallel Output Series (IPOS) topology presented in Fig. 6.1(b) shares the current in the parallel side while achieves high voltage in series side. Therefore, it is suitable for applications where energy storage and load have large voltage difference. To equally share the power flow among the modules, voltage controller is needed for individual modules. Fig. 6.1(e) is derived from Fig. 6.1(b). Many identical energy storages can be connected through DC-DC converters and their outputs are connected in series to achieve high output voltage.

Input Series Output Series (ISOS) configuration of Fig. 6.1 (c) shares voltage both in input and output side. It is favorable for high input and output voltage application. This connection is especially useful when power increases to MW level since higher voltage can help to reduce the magnitude of current to achieve lower loss [63], [20]. However, it is necessary to implement both input and output voltage

sharing control scheme which increases the control complexity.

In all the above mentioned schemes, the basic power converter module used is the DAB. The module based converter design approach not only can match the different source and load requirements, but also share the power in each module and thus help to release the switch stress. Table. 6.1 lists the comparison of switch stress and transformer turns ratio in IPOP, IPOS and ISOS with single DAB converter respectively. Base values are chosen according to single DAB rating when same power and same input/output voltage are used. From Table. 6.1, we can clearly see the advantages of different topologies in switch rating selection. For example, the current rating for primary side switches and voltage rating for the secondary side switches are reduced to 1/n p.u. (as shaded rows) when n modules are connected under IPOS structure. As mentioned before, IPOS structure is suitable for applications where energy storage and load have large voltage differences. In other words, lower current rating in low voltage side and lower voltage rating in high voltage side is achievable using IPOS structure.

This modular design approach is followed in realizing the power converter structure in the proposed CESS system.

6.3 Operating principles of Interleaved IPOS DAB converter

To illustrate the operating principle, interleaved modulation scheme and control strategy are adopted for converter modules. Topology IPOS is investigated. This topology is suitable when source voltage is low while DC bus voltage is quite high. Here, four DABs are used for illustration. Its topology is shown as Fig. 6.2. The key waveform is displayed at Fig. 6.3.

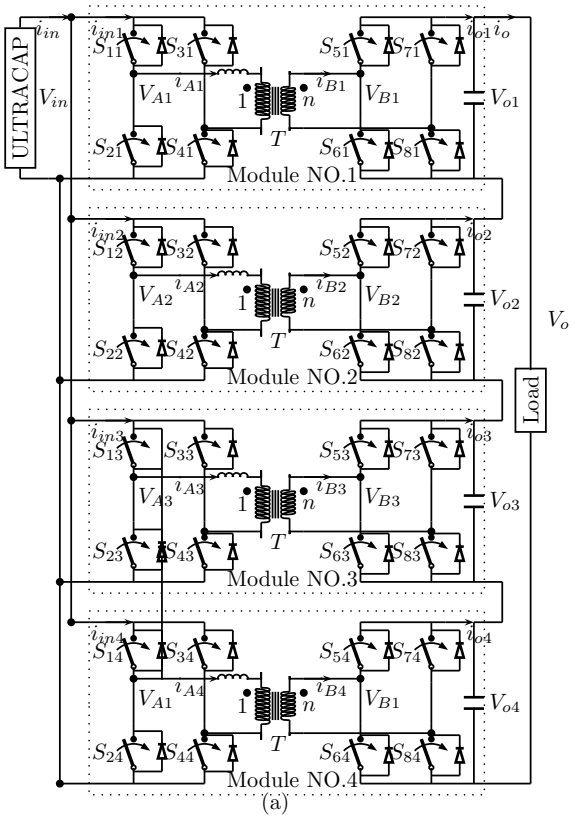


Figure 6.2: Topology of IPOS interleaved DAB

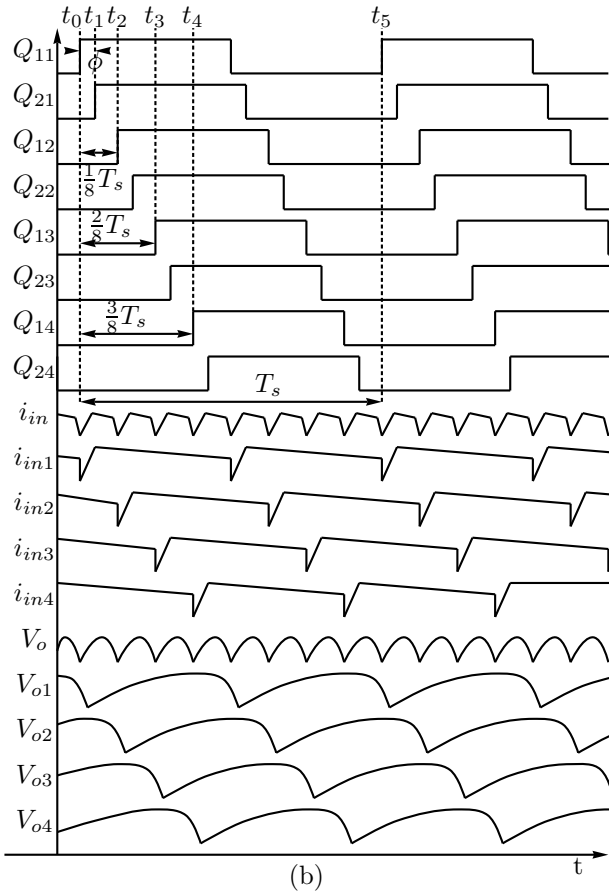


Figure 6.3: Typical waveforms in IPOS interleaved DAB

Here four DABs are connected and interleaved to achieve high power as well as low input and output ripple. Fig. 6.3 shows the gating signals and key waveforms in IPOS converter (Fig. 6.2). Here Q_{1j} is the control signal in primary side to switch S_{1j} and S_{4j} for Module NO.j while S_{2j} and S_{3j} are turned on complementarily. Q_{2j} are the gating signals for controlling switches S_{5j} and S_{8j} in secondary side while S_{6j} and S_{7j} are turned on complementarily. In order to achieve the interleaving, Q_{12}, which controls the primary switches in Module No. 2, is phase shifted by 45^o ($\frac{T_s}{8}$) to Q_{11}, which controls the primary switches in Module No.1. Similarly,

Q_{13} and Q_{14} are phase shifted by 90^o and 135^o respectively referred to Q_{11}. As described before, the ripple frequency in the input current i_{in} is 4 times as the one from single module such as i_{in1}. The ripple magnitude is less than $\frac{1}{4}$ compared to i_{in1}. Same observations can be found in output capacitor voltage V_o from Fig. 6.3.

6.4 Controller design for interleaved IPOS DAB converter

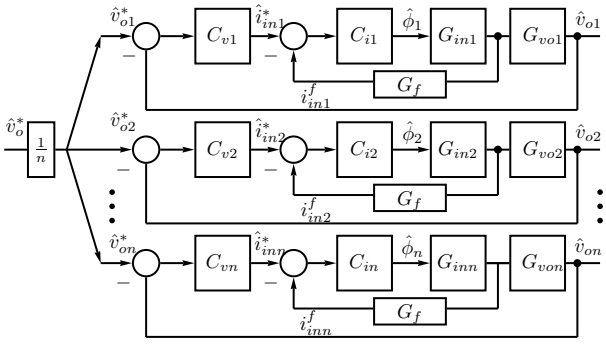


Figure 6.4: Control block diagram for the IPOS interleaved DAB converter

The objectives of controller design are (1) to regulate the output voltage at its desired value and (2) to actively share the power between each module.

In order to achieve above objectives, for IPOS converter, individual voltage controller is implemented. The reference voltage for each module is set to be $\hat{v}^*_{oj}$. For example, $\hat{v}^*_o$ is supposed to be regulated as 800V in our application. There are four converters connected together. Each module voltage reference $\hat{v}^*_{oj}$ will be 200V. By implementing this controller, active power sharing is naturally achieved. As

discussed in [61], the input currents i_{in} drawn from the source by different parallel branches also become equal. Therefore, second objective is also achieved. The block diagram of cascaded controller for IPOS connected interleaved DAB converter is shown in Fig. 6.4. The controller diagram consists of voltage controller C_v and current controller C_i as shown in Eqn.(6.1). To filter out the large switching ripple in the feedback input current i_{in}, a low pass filter G_f in Eqn.(6.2) is implemented.

$$\begin{aligned} C_v &= K_{cv}(1 + \frac{1}{sT_{iv}}) \\ C_i &= K_{ci}(1 + \frac{1}{sT_{ii}}) \end{aligned} \tag{6.1}$$

$$G_f = \frac{2\pi f_{cf}}{s + 2\pi f_{cf}} \tag{6.2}$$

Where f_{cf} is the low pass filter cut off frequency.

6.5 Simulation Results

Simulation is carried out in SIMPLORER software. Table. 6.3 lists all the simulation parameters.

Table 6.2: Simulation parameters (1)

Ultracapacitor voltage (V)	V_{UC}	25-48
Output Voltage (V)	V_{o1}	200
Transformer turns ratio	n	6.67
Switching frequency (kHz)	f_s	20
Output Power (kW)	P_{o1}	1.2
Leakage Inductance of DAB_1^I (uH)	L_{k1}	1.20(0%)
Leakage Inductance of DAB_2^I (uH)	L_{k2}	1.26(5%)
Leakage Inductance of DAB_3^I (uH)	L_{k3}	1.44(20%)
Leakage Inductance of DAB_4^I (uH)	L_{k4}	1.32(10%)

Table 6.3: Simulation parameters (2)

Gain in voltage controller	K_{cv}	3
Time constant in voltage controller	T_{iv}	0.00125
Gain in current controller	K_{ci}	0.001
Time constant in current controller	T_{ii}	0.5
Cut-off frequency for feedback (kHz)	f_{cf}	1
Capacitance of output voltage V_{o1} (uF)	C_{o1}	100(0%)
Capacitance of output voltage V_{o2} (uF)	C_{o1}	105(5%)
Capacitance of output voltage V_{o3} (uF)	C_{o1}	120(20%)
Capacitance of output voltage V_{o4} (uF)	C_{o1}	110(10%)

Fig. 6.5 shows transformer waveforms for interleaved DAB converters. To achieve the interleaved scheme, the transformer primary side voltage in Module

No. 1 (Fig. 6.5 (a)) leads the one in Module No.2 (Fig. 6.5 (c)) by $\frac{T_s}{8}$ time period. Similarly, Module No. 3 (Fig. 6.5 (b)) leads by $\frac{T_s}{8}$ referred to the one in Module No.4 (Fig. 6.5 (d)).

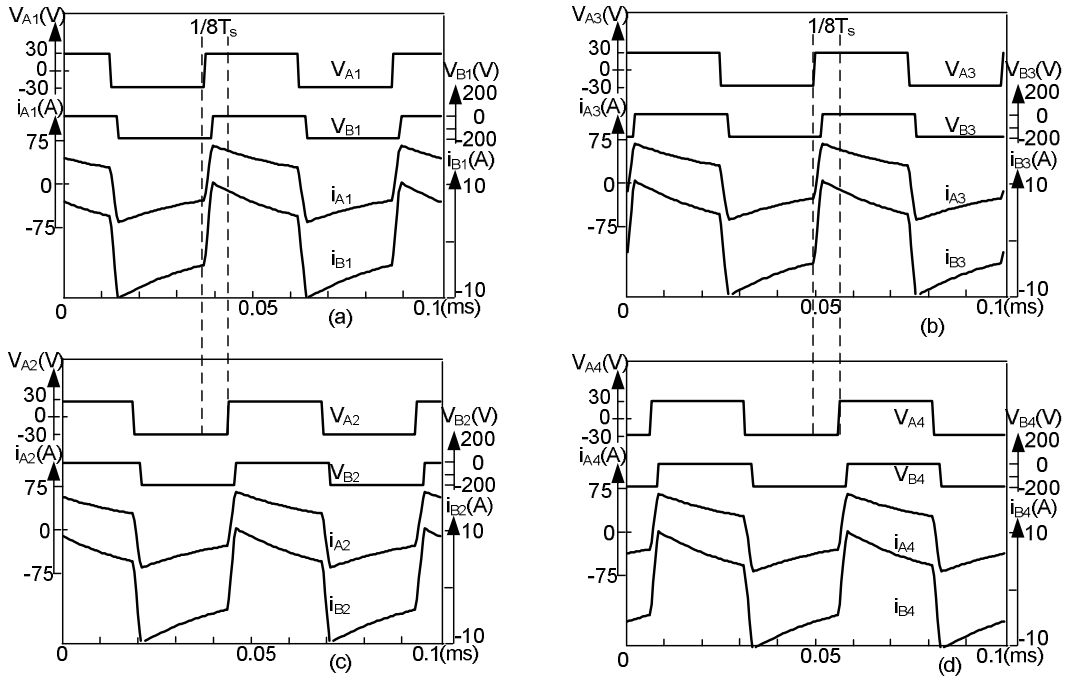


Figure 6.5: Waveforms of voltage and current in transformer

(a)-(d) are for module 1 to module 4

Fig. 6.6 (a) illustrates that the input current i_{in} has peak to peak ripple of 46.8% (base current is 160A) while the one in i_{in1} has 222.5% (base current is 40A). Similarly in Fig. 6.6 (b) the output voltage V_o has ripple of 0.08% (base voltage is 800V) while V_{o1} has 0.67% (base voltage is 200V). The results show that the interleaved scheme helps to reduce the input/output ripple at least 4 times compared to the single module. The same ripple reduction results can be found in Fig. 6.6 (c) and (d) when negative power is transferred. From Fig. 6.6 (a) to (d),

input current i_{in1} to i_{in4} and output voltage v_{o1} to v_{o4} in each module are nearly the same even though the inductor and capacitor values have up to 20% differences in each module shown in Table. 6.3. This shows, the designed controller can achieve the active power sharing in each module.

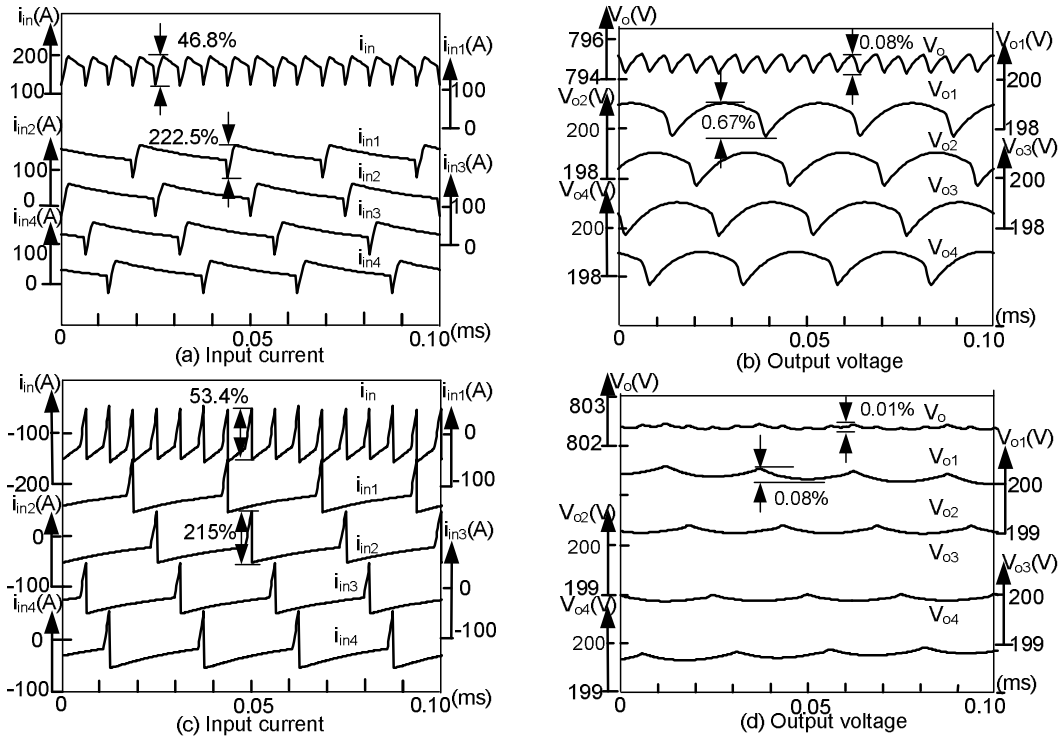


Figure 6.6: Waveforms of input current

(a-b) positive power transfer (c-d) negative power transfer

Fig. 6.7 (a) shows the step response when load changes from 50% to 100% (4.8kW is rated value) for an input voltage of 28V. The overshoot and undershoot are within 3.75% of rated 800V. Similarly, when input voltage is 45V and same load steps are applied, the proposed voltage controller can restore the voltage within

20ms. The overshoot and undershoot are below 2.5% under this case. Fig. 6.7 (c) and (d) are achieved when the negative power is transferred under the similar load step changes. All the above simulation verified that the controller is able to regulate the output voltage under a wide operating range. This feature is important for ultracapacitor application where the terminal voltage varies during charging and discharging. The transferred power can also be changed in a wide range.

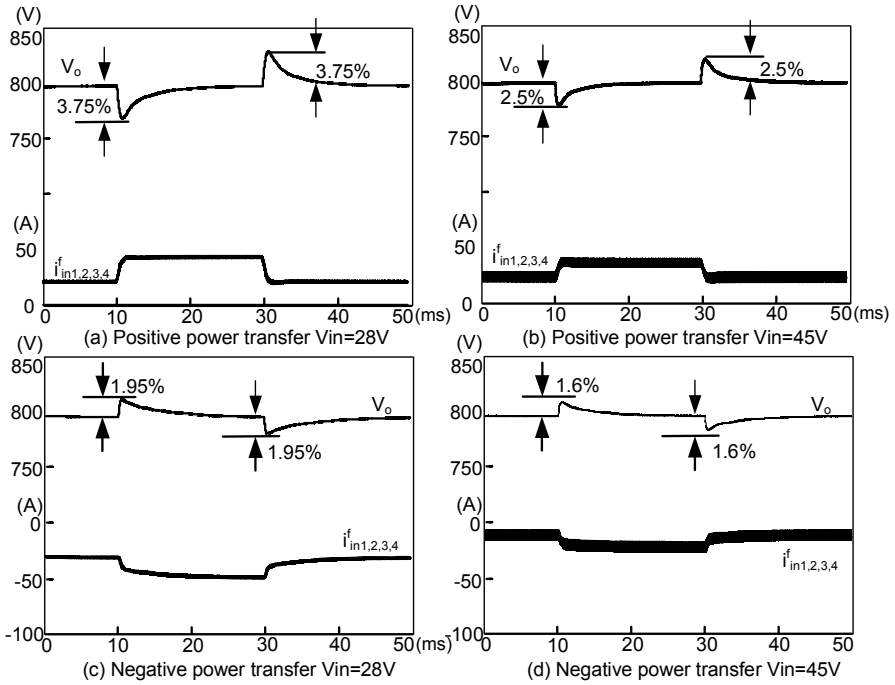


Figure 6.7: Output voltage waveform when load steps between 2.4kW and 4.8kW

6.6 Summary

In this chapter, a modular design is proposed to connect DAB converter for high power application. An interleaved Input Parallel Output Series Dual Active

Bridge DC-DC converter topology is investigated for interfacing ultracapacitor with the micro-grid. The proposed topology achieves high power density and high boost ratio. A cascaded controller is also proposed. The simulation results show that the proposed controller is able to regulate the output voltage in a wide operating range. The power sharing objective is also achieved even at the presence of 20% variation in parameters among individual converters.

Table 6.1: Comparison of devices stress under same output power

	IPOP (p.u.)	IPOS (p.u.)	ISOS (p.u.)
Primary			
Switch Current Rating	$1/n$	$1/n$	1
Switch Voltage Rating	1	1	$1/n$
Secondary			
Switch Current Rating	$1/n$	1	1
Switch Voltage Rating	1	$1/n$	$1/n$
Turns ratio	1	$1/n$	1

Chapter 7

Conclusion and future work

7.1 Conclusion

The objective of this thesis is to design and control suitable power electronic converters for interfacing energy storage and load. In this thesis, energy storage is used to dynamically support the renewable source.

In Chapter 2, a Dual Active Bridge converter was selected to interface the ultracapacitor and load. A novel hybrid modulation scheme was proposed to widen its power transfer range. By using the proposed hybrid modulation scheme, the power transfer capability ranges from 100% to 16.67% instead of 100% to 58.33% in conventional phase shift case, which was almost 100% increase in effective power

transfer range.

In Chapter 3, a feedback linearization controller was implemented to regulate the DAB voltage under a wide range. The advantage of using this controller was that the nonlinear relationship can be taken care of by the controller, thus, a simple linear PI controller could be designed.

In Chapter 4, a Passivity based controller (PBC), which achieves energy shaping by injecting damping in the controller, had been investigated in boost type ICFFB converter. Stable operation was achieved under a wide range. Performance comparison with PI controller was carried out. The results showed that the PBC using series damping injection had similar performance as PI controller using current loop.

In Chapter 5, in order to achieve fast dynamic response in the system, a controller was designed to regulate the DC bus voltage as well as to dynamically distribute the power between the renewable source and ultracapacitor is implemented. The experimental results verified the effectiveness of the controller.

In Chapter 6, an Interleaved Modular DAB converter for Micro-grid application was proposed. Its high power transfer and flexible reconfiguration capabilities showed great potential in high power application. The input and output ripple was minimized due the proper interleaving modulation. A cascaded controller was also proposed for voltage regulation and the simulation results were given to validate

the effectiveness of the converter design.

In conclusion, this thesis had investigated the design and control of power electronic converter for energy storage interfacing. The analysis, simulation and experimental results have demonstrated the feasibility of the design.

7.2 Future work

In this thesis, controllers are implemented to the energy storage augmented renewable energy system. A framework to use intermittent renewable energy is proposed. In order to efficient share the energy among the renewable source and the energy storage, an optimized energy management scheme can be designed. It should be able to take care of the following issues

(1) Predict the load profile

In current approach, energy storage is designed to take care of any shortage between the renewable energy and load. If load prediction can be incorporated in the energy management scheme, the sizing of the energy storage can be much more accurate instead of over sizing. In order to do so, historical profiles for renewable energy sources and the load are needed. Then a proper prediction algorithm should be developed to generate the load profile.

(2) Schedule the power distribution

To schedule the power distribution as well as maintain a good reserve in energy storage system, energy storage characteristics should be modeled into energy management. The energy storage model, which reflects the relationship between the depth of discharge and life cycle, efficiency and thermal characteristics, needs to be developed. Based on that, the energy utilization can be improved as well as load demand can be met continuously.

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Appendix A

Description of hardware

1.1 Overview of the implementation scheme

The experimental set-up for implementing the proposed controller and hybrid modulation for the DAB are built up, using dSPACE DS1104 processor board and rapid-prototyping software tools, as shown in the block diagram of Fig. A.1. The experimental set-up comprises of the following units:

- A pentium III PC for rapid-prototyping and real-time control.
- A DSP-ds1104 controller board for running control programs, generating control signals, sampling feedback signals and communicating with the computer.
- An interface board for voltage shifting and buffering.

- A Field-Programmable Gate Array (FPGA) SPARTAN-3 for high frequency PWM generation
- A driver board to drive the power switch
- A Dual Active Bridge Converter
- An Interleaved Current Fed Full Bridge Converter
- Sensing devices including current sensors and voltage sensors.
- A controllable resistive load bank.

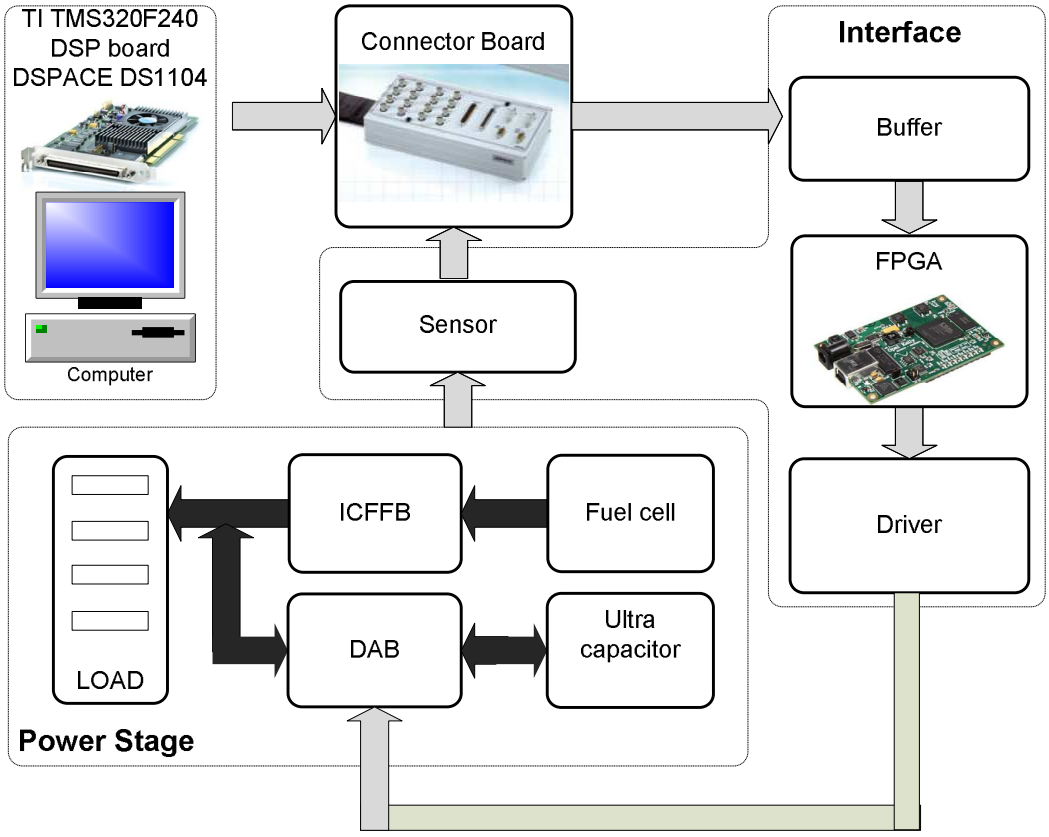

Figure A.1: Block diagram of hardware implementation

1.2 dSPACE DS1104

The control development platform is dSPACE DS1104, which uses a floating point processor MPC8240 as the main processor, and a TMS320F240 Slave DSP. The PC interface of the DSP controller provides an easy development environment. The DS1104 system has four 16-bit A/D, four 12-bit A/D channels, 4 single phase PWM and total 24 digital I/Os.

1.3 Generating high frequency phase shifted PWM signals

To minimize the size of the passive components, the DAB converter was designed to operate at 100kHz switching frequency. As described in previous section, the power transfer in DAB is achieved by phase shifting the gating signals between primary and secondary sides of H-bridges.

However, dSPACE is not able to provide PWM signals higher than 20kHz. In addition, no phase shifting function is available in dSAPCE. Since FPGA has a high clock frequency and therefore it is able to generate high frequency switching signals.

The high frequency phase shifted switching signals are generated as follows,

- FPGA generates 100kHz switching frequency with 600ns dead-time

  As we know, 100kHz corresponds to 10μs switching period. 100MHz clock frequency means 10ns/clock. Therefore, in FPGA, one switching period equals to 1000 clocks. Taking dead time into consideration, the total turn on period is 440 clocks while turn off period occupies 560 clocks.

- FPGA generates phase shifted PWM signals

  Firstly, FPGA receives phase shift signal from dSPACE. For example, 0.1 p.u. phase shift equals to 0.1 p.u.x 1000 clocks=100 clocks. The phase shifted signal Q_3 is generated after delaying 100 clocks refereed to Q_1. The resolution of phase shift is 10ns or 0.36 degree. Since 7 bits phase shift is used, when full range is selected as 0.125 p.u., the phase shift resolution can be calculated as $\frac{0.125p.u.}{125}10us$ =10ns.

Fig. A.2 shows the block diagram of interfacing board. Detailed I/O mapping between the dSPACE and FPGA is shown in Appendix. B.

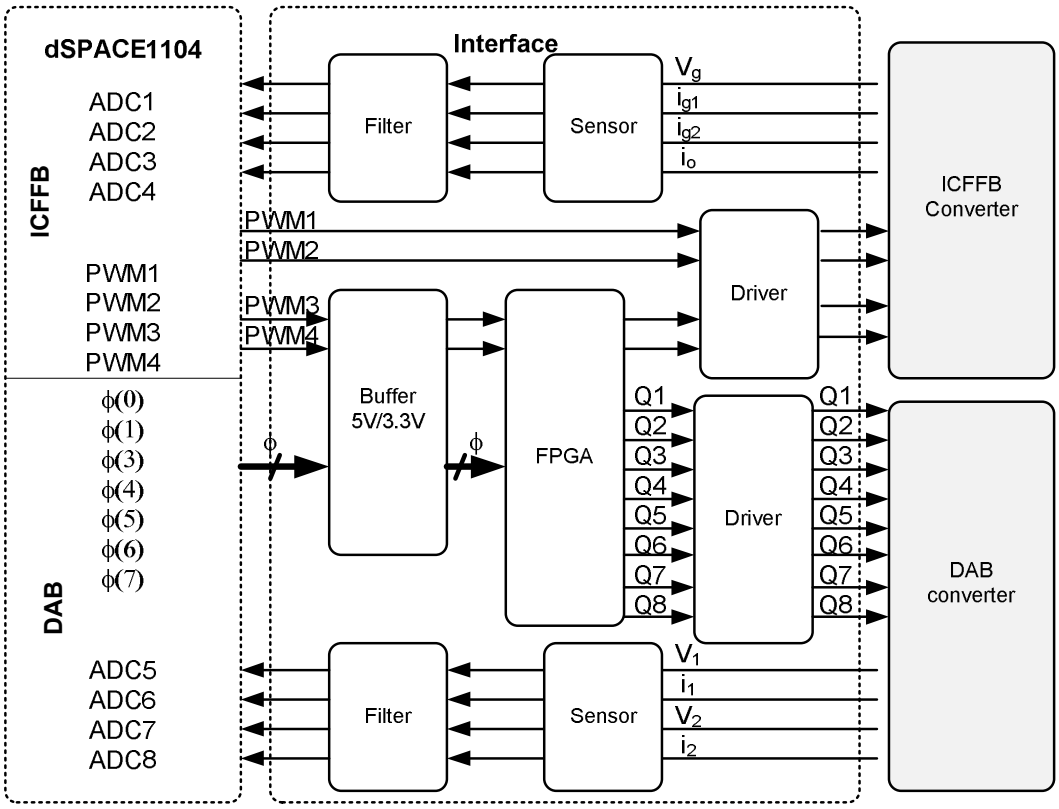

Figure A.2: Block diagram of the controller interfacing board

1.4 Specifications of power converters

A 2kW DAB and a ICFFB converter have been implemented. Their specifications are listed in Table. A.1 and Table. A.3.

Table A.1: ICFFB converter specification (a)

Switching frequency	$f_s = 10kHz$
Maximal output power	$1200W$
Switches	IXFK90N20 MOSFETs $R_{DS(ON)} = 40m\Omega(100^oC)$
Diodes	4×Ultra fast MUR860 $8A/600V$
Output capacitors	$100\mu F$,$200V$ Electrolytic $+0.027\mu F$ polyester
Snubber capacitors	$0.44\mu F$ polyester

Table A.2: ICFFB converter specification (b)

Input inductors	$E305-26$, Iron powder core L_1: $178.8\mu H$, $r_1 = 64m\Omega$ L_2: $177\mu H$, $r_2 = 68.6m\Omega$
Transformers	$EC70$, Ferrite core$-3C90$ $n_1/n_2 = 1:2$, $L_m = 931.7\mu H$ leakage inductance $L_k = 4.9\mu H$

Table A.3: DAB converter specification

Low voltage side	8xIXTH200N10T MOSFET Electrolytic capacitor 2x10mF Film capacitor 20x15μF
High voltage side	4xSPA17N80C3 MOSFET Snubber capacitor 4x1nF MKP 338 4 X2 2x10μ F Capacitor X2 15x0.22μF
Transformer	PM 114/93 Ferrocube 1:n= 5:60 Lk=0.58 μH,Lm=70 μH

Appendix B

Experiments

In this Appendix, physical I/O address mapping between FPGA and dSPACE are listed in Table. B.1. Fig. B.1 and Fig. B.2 show the FPGA I/O assignment and FPGA program generating phase shifted PWM signals respectively. Fig. B.3 to Fig. B.6 are PCB drawings for DAB power stage implementation.

Table B.1: Physical IO address mapping between FPGA and dSPACE

phase	FPGA	dSPACE	DAB gate	FPGA	dspace
phase(0)	XBUS-0	CP17 2	Q1	XBUS-46	N/A
phase(1)	XBUS-2	CP17 3	Q2	XBUS-44	N/A
phase(2)	XBUS-4	CP17 5	Q3	XBUS-42	N/A
phase(3)	XBUS-6	CP17 6	Q4	XBUS-40	N/A
phase(4)	XBUS-8	CP17 8	Q5	XBUS-41	N/A
phase(5)	XBUS-10	CP17 9	Q6	XBUS-43	N/A
phase(6)	XBUS-12	CP17 11	Q7	XBUS-45	N/A
phase(7)	XBUS-14	CP17 12	Q8	XBUS-47	N/A
duty1	FPGA	dSPACE	duty2	FPGA	dSPACE
duty1(0)	XBUS-15	CP17 27	duty2(0)	XBUS-17	CP17 14
duty1(1)	XBUS-11	CP17 24	duty2(1)	XBUS-21	CP17 33

```
#PACE: Start of PACE I/O Pin Assignments
#Updated 11-03-2008; ZHOU HAIHUA
NET "CLOCK"  LOC = "N9"  ;#definition of clock frequency
#definition of phase I/O port
NET "phase<0>"  LOC = "U18"  ;
NET "phase<1>"  LOC = "T18"  ;
NET "phase<2>"  LOC = "R17"  ;
NET "phase<3>"  LOC = "R18"  ;
NET "phase<4>"  LOC = "P17"  ;
NET "phase<5>"  LOC = "P18"  ;
NET "phase<6>"  LOC = "N17"  ;
NET "phase<7>"  LOC = "M18"  ; #bit for sign

NET "duty1<0>"  LOC = "M16"  ;#definition of D1 I/O port
NET "duty1<1>"  LOC = "M15"  ;
NET "duty1<2>"  LOC = "N15"  ;
NET "duty1<3>"  LOC = "P16"  ;
NET "duty1<4>"  LOC = "P15"  ;
NET "duty1<5>"  LOC = "R16"  ;

NET "duty2<0>"  LOC = "K18"  ;#definition of D2 I/O port
NET "duty2<1>"  LOC = "K17"  ;
NET "duty2<2>"  LOC = "M14"  ;
NET "duty2<3>"  LOC = "N14"  ;
NET "duty2<4>"  LOC = "L16"  ;
NET "duty2<5>"  LOC = "L15"  ;

NET "Q8"  LOC = "E18"  ;#definition gate signal output for DAB
NET "Q7"  LOC = "F17"  ;
NET "Q6"  LOC = "G18" ;
NET "Q5"  LOC = "H17"  ;
NET "Q4"  LOC = "F15"  ;
NET "Q3"  LOC ="G15"  ;
NET "Q2"  LOC = "G16" ;
NET "Q1"  LOC = "H15"  ;

#definition of enable I/O port
NET "EN1"  LOC = "L17"  ; #Mode I
NET "EN2"  LOC = "L18"  ; #Mode II
NET "EN3"  LOC = "J15"  ; #Mode III

#definition shifted phase for ICFFB converter
NET "PH_A"  LOC = "T17"  ; #JP1-31 #PWM2 In
NET "PH_B"  LOC = "T16"  ; #JP1-33 #PWM1 In
NET "ph_a_out_90"  LOC = "H13" ;#"J18"  ; #JP2-61 #PWM2 Out
NET "ph_b_out_90"  LOC = "H14" ;#"J17"  ; #JP2-63 #PWM1 Out

NET "LED7"  LOC = "V14"  ;  #definition LED address
NET "LED6"  LOC = "U14"  ;
NET "LED5"  LOC = "T14"  ;
NET "LED4"  LOC = "V15"  ;
NET "LED3"  LOC = "U15"  ;
NET "LED2"  LOC = "V16"  ;
NET "LED1"  LOC = "V17"  ;
NET "LED0"  LOC = "U16"  ;
```

Figure B.1: I/O definition in FPGA program

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer: ZHOU HAIHUA
-- Dependencies:
-- Additional Comments:
--Modified on 05/29/2008
--Designed for the DAB converter operated at 100kHz
--Hybrid Modulation Purpose
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity phase is
   Port ( CLOCK : in  STD_LOGIC;
          --ICFFB
               PH_A : in std_logic;
        PH_B : in std_logic;
                                  ph_a_out_90 : out std_logic := '0';
                             ph_b_out_90 : out std_logic := '0';
          --DAB
               EN1: in std_logic;
               EN2: in std_logic;
               EN3: in std_logic;
              phase : IN STD_LOGIC_VECTOR(7 DOWNTO 0):= (OTHERS => '0');--bit 7=SIG
               duty1 : in std_logic_vector(5 downto 0);
               duty2 : in std_logic_vector(5 downto 0);
                                  LED0 : out  STD_LOGIC;
                                  LED1 : out  STD_LOGIC;
                                  LED2 : out  STD_LOGIC;
                                  LED3 : out  STD_LOGIC;
                                  LED4 : out  STD_LOGIC;
                                  LED5 : out  STD_LOGIC;
                                  LED6 : out  STD_LOGIC;
                                  LED7 : out  STD_LOGIC;

        Q1 : out  STD_LOGIC;
        Q2 : out  STD_LOGIC;
        Q3 : out  STD_LOGIC;
        Q4 : out  STD_LOGIC;
        Q5 : out  STD_LOGIC;
        Q6 : out  STD_LOGIC;
        Q7 : out  STD_LOGIC;
        Q8 : out  STD_LOGIC);
end phase;

architecture Behavioral of phase is

Begin

PROCESS(CLOCK)
--90 degree phase shift for ICFFB converter; FPGA clock is 100MHz (10ns per cycle)
-- if a delay of 180 deg is needed then 5000 cycles are needed;
--if the delay of 90 deg is needed then 2500 cycles are needed;
-- these value are inputted for data_size
```

```
constant data_size_a : integer := 2500;
constant data_size_b : integer := 2500;
variable data_a : bit_vector(data_size_a downto 0);
variable data_b : bit_vector(data_size_b downto 0);

VARIABLE COUNTER  : INTEGER RANGE 0 TO 1023 := 0;
VARIABLE phase_temp :      INTEGER RANGE 0 TO 1023 := 0;
VARIABLE  neg :STD_LOGIC_VECTOR(6 DOWNTO 0):= "0000000";
VARIABLE  sign : STD_LOGIC;
VARIABLE duty1_temp :      INTEGER RANGE 0 TO 511 := 0;
VARIABLE duty2_temp :      INTEGER RANGE 0 TO 511 := 0;
Constant WidthAB: std_logic_vector (11 downto 0):=x"1B8";           -- (440=500-60 clk )
Constant WidthCD: std_logic_vector (11 downto 0):=x"1B8";           -- (440=500-60 clk )
Constant thresh: std_logic_vector (11 downto 0):=x"03C"; --( 60 clk ) for mode phase  shift
Constant thresh1: std_logic_vector (11 downto 0):=x"03C"; --(60 clk )for mode triangular
Constant Duty: std_logic_vector (11 downto 0):=x"1F4";   -- (500 clk )

begin
IF (CLOCK 'EVENT AND CLOCK = '1') THEN
--ICFFB
            if ph_a = '1' then
              data_a(0) := '1';--computing phase a
              data_a := data_a rol 1;
  else
              data_a(0) := '0';
              data_a := data_a rol 1;
  end if;

  if data_a(0) = '1' then
              ph_a_out_90 <= '1';
  else
              ph_a_out_90 <= '0';
  end if;
            if ph_b = '1' then
              data_b(0) := '1';   --computing phase b
              data_b := data_b rol 1;
   else
              data_b(0) := '0';
              data_b := data_b rol 1;
  end if;

  if data_b(0) = '1' then
              ph_b_out_90 <= '1';
  else
              ph_b_out_90 <= '0';
  end if;
             -- end of computing phase b

 --DAB---
            duty1_temp := 8*conv_integer(duty1);--80ns as resolution for duty ratio
            duty2_temp := 8*conv_integer(duty2);

            IF (COUNTER >= 999) THEN -- MOD  1000 Counter
                        COUNTER := 0;
            ELSE
                        COUNTER := COUNTER + 1;
            END IF;
```

```
IF (COUNTER=0) THEN
                        LED0<=phase(0);
                        LED1<=phase(1);
                        LED2<=phase(2);
                        LED3<=phase(3);
                        LED4<=phase(4);
                        LED5<=phase(5);
                        LED6<=phase(6);
                        LED7<=EN3;
                        sign:=phase(7); -- sign
    if (sign = '0') then
                        phase_temp := 1*conv_integer(phase);--resolution for phase shift is 10ns
                        else
                        neg(0):=phase(0);
                        neg(1):=phase(1);
                        neg(2):=phase(2);
                        neg(3):=phase(3);
                        neg(4):=phase(4);
                        neg(5):=phase(5);
                        neg(6):=phase(6);
                        phase_temp :=1*conv_integer(neg);---246
                        end if;
             END IF;
IF (EN3='1') THEN --dSPACE default IO is high, EN3=1,all the switches are off for DAB
            Q1<= '0';
            Q2<= '0';
            Q3<= '0';
            Q4<= '0';
            Q5<= '0';
            Q6<= '0';
            Q7<= '0';
            Q8<= '0';
ELSE
IF (EN2='1') THEN
  IF (EN1 = '0') THEN--Triangular Positive Power Transfer
            IF (COUNTER<duty1_temp) THEN
                                    Q1<= '1';
                        ELSE
                                    Q1 <= '0';
                        END IF;

            IF ((COUNTER>duty1_temp+thresh1) AND (COUNTER<Duty-thresh1+Duty)) THEN
                                    Q2<= '1';
                        ELSE
                                    Q2 <= '0';
                    END IF;

            IF ((COUNTER>Duty) AND (COUNTER<duty1_temp+Duty)) THEN
                                    Q3<= '1';
                        ELSE
                                    Q3 <= '0';
                        END IF;

            IF ((COUNTER<Duty-thresh1) OR (COUNTER>Duty+duty1_temp+thresh1)) THEN
                                    Q4<= '1';
                        ELSE
                                    Q4 <= '0';
                        END IF;
```

```
        IF ((COUNTER>duty1_temp+thresh1) AND (COUNTER<duty1_temp+duty2_temp-thresh1))
THEN
                                Q5<= '1';--S5 stop here
                        ELSE
                                Q5 <= '0';
                        END IF;

        IF ((COUNTER<duty1_temp) OR (COUNTER>duty1_temp+duty2_temp)) THEN
                                Q6<= '1';---S5 start here
                        ELSE
                                Q6 <= '0';
                        END IF;

THEN
        IF ((COUNTER>duty1_temp+thresh1+Duty) AND (COUNTER<duty1_temp+duty2_temp-
thresh1+Duty)) THEN
                                Q7<= '1';
                        ELSE
                                Q7 <= '0';
                        END IF;

        IF ((COUNTER<duty1_temp+Duty) OR(COUNTER>Duty+duty1_temp+duty2_temp)) THEN
                                Q8<= '1';
                        ELSE
                                Q8 <= '0';
                        END IF;
        ELSE --Triangular Negative power transfer
       IF (COUNTER<duty1_temp) THEN
                                Q5<= '1';
                        ELSE
                                Q5 <= '0';
                        END IF;
        IF ((COUNTER>duty1_temp+thresh1) AND (COUNTER<Duty-thresh1+Duty)) THEN
                                Q6<= '1';
                        ELSE
                                Q6 <= '0';
                        END IF;
        IF ((COUNTER>Duty) AND (COUNTER<duty1_temp+Duty)) THEN
                                Q7<= '1';
                        ELSE
                                Q7 <= '0';
                        END IF;
        IF ((COUNTER<Duty-thresh1) OR (COUNTER>Duty+duty1_temp+thresh1)) THEN
                                Q8<= '1';
                        ELSE
                                Q8<= '0';
                        END IF;

        IF ((COUNTER>duty1_temp) AND (COUNTER<duty1_temp-thresh1+duty2_temp-thresh1))
THEN
                                Q1<= '1';
                        ELSE
                                Q1 <= '0';
                        END IF;
```

```
IF ((COUNTER<duty1_temp-thresh1) OR (COUNTER>duty1_temp+duty2_temp-thresh1)) THEN
                                        Q2<= '1';
                                ELSE
                                        Q2 <= '0';
                                END IF;
        IF ((COUNTER>duty1_temp+Duty) AND (COUNTER<duty1_temp+duty2_temp-thresh1+Duty-
thresh1)) THEN
                                        Q3<= '1';
                                ELSE
                                        Q3 <= '0';
                                END IF;

        IF ((COUNTER<duty1_temp+Duty-thresh1) OR(COUNTER>Duty+duty1_temp+duty2_temp-
thresh1)) THEN
                                        Q4<= '1';
                                ELSE
                                        Q4 <= '0';
                                END IF;
    END IF;
 ELSE
   IF (sign = '0') THEN  --For the positive phase shift
        IF (COUNTER<WidthAB) THEN
                                        Q1<= '1';
                                        Q4<= '1';
                                ELSE
                                        Q1 <= '0';
                                        Q4 <= '0';
                                END IF;
        IF ((COUNTER>Duty) AND (COUNTER<WidthAB+Duty)) THEN
                                        Q2 <= '1';
                                        Q3 <= '1';
                                ELSE
                                        Q2 <= '0';
                                        Q3 <= '0';
                                END IF;
        IF ((COUNTER>phase_temp) AND (COUNTER<phase_temp+WidthCD)) THEN
                                        Q5 <= '1';
                                        Q8 <= '1';
                                ELSE
                                        Q5 <= '0';
                                        Q8 <= '0';
                                END IF;
    IF (phase_temp>=thresh1) THEN
       IF ((COUNTER<=phase_temp+WidthCD-Duty) OR (COUNTER>phase_temp+Duty)) THEN
                                        Q6 <= '1';
                                        Q7<= '1';
                                ELSE
                                        Q6 <= '0';
                                        Q7 <= '0';
                                END IF;
    ELSIF ((COUNTER > phase_temp+Duty ) AND (COUNTER <(phase_temp+Duty+WidthCD)))THEN
                                        Q6 <= '1';
                                        Q7<= '1';
                                ELSE
                                        Q6 <= '0';
                                        Q7 <= '0';
                                END IF;
```

```
  ELSE
                        IF (COUNTER<WidthCD) THEN        --For the negative phase shift
                                Q5<= '1';
                                Q8<= '1';
                        ELSE
                                Q5<= '0';
                                Q8<= '0';
                        END IF;
                        IF ((COUNTER>Duty) AND (COUNTER<WidthCD+Duty)) THEN
                                Q6<= '1';
                                Q7<= '1';
                        ELSE
                                Q6<= '0';
                                Q7<= '0';
                        END IF;
IF ((COUNTER>phase_temp) AND (COUNTER<phase_temp+WidthAB)) THEN
                                Q1 <= '1';
                                Q4 <= '1';
                        ELSE
                                Q1 <= '0';
                                Q4 <= '0';
                        END IF;
IF (phase_temp>=thresh) THEN
   IF ((COUNTER<=phase_temp+WidthAB-Duty) OR (COUNTER>phase_temp+Duty)) THEN
                                Q2 <= '1';
                                Q3 <= '1';
                          ELSE
                                Q2 <= '0';
                                Q3 <= '0';
                          END IF;
ELSIF ((COUNTER > phase_temp+Duty ) AND (COUNTER < (phase_temp+Duty+WidthAB)))THEN
                                Q2 <= '1';
                                Q3 <= '1';
                          ELSE
                                Q2 <= '0';
                                Q3 <= '0';
            END IF;
          END IF;
END IF;
END IF;
END IF;
END PROCESS;
end Behavioral;
```

Figure B.2: FPGA program for phase shifted PWM signals

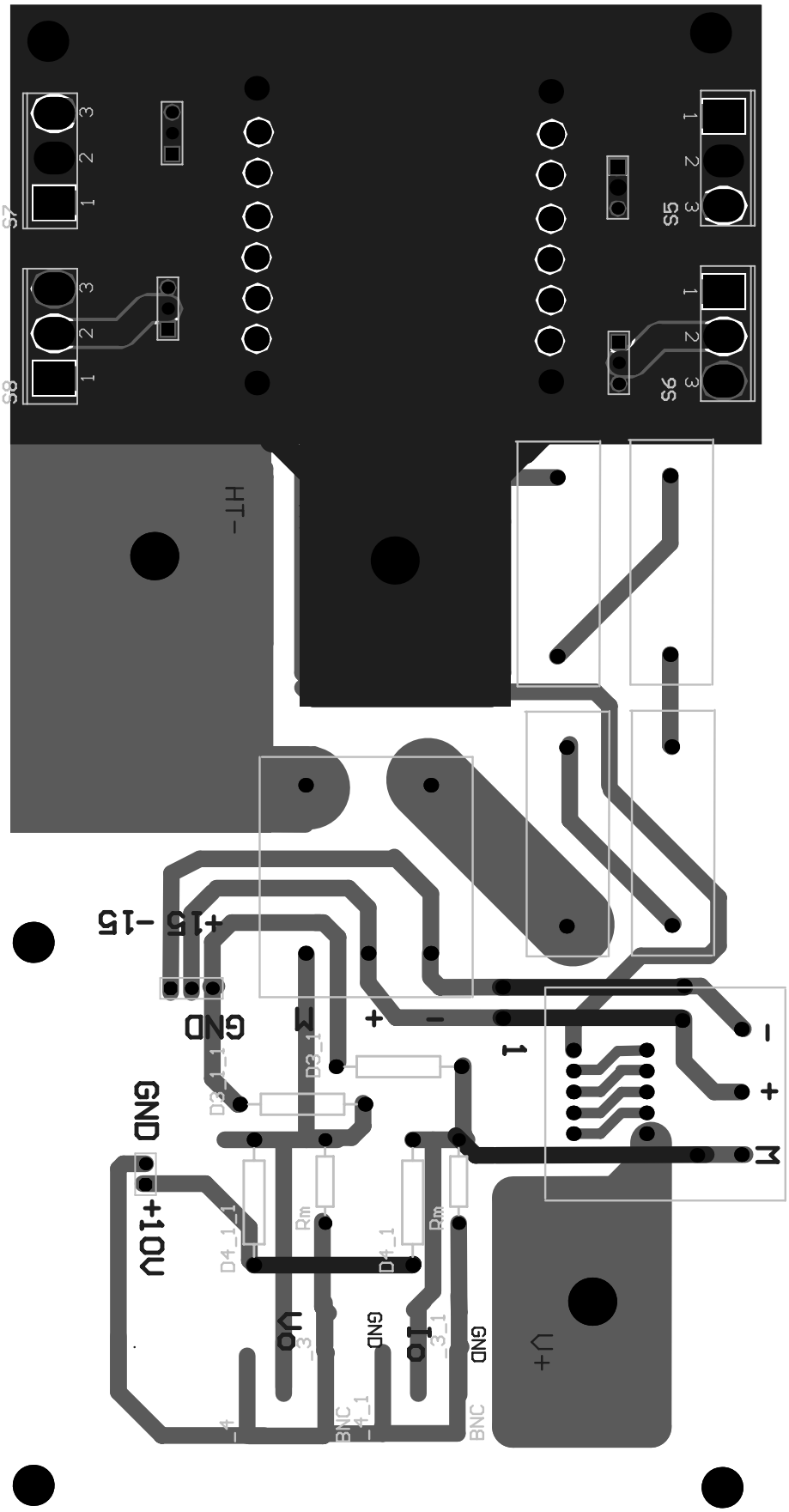

Figure B.3: DAB secondary side power stage

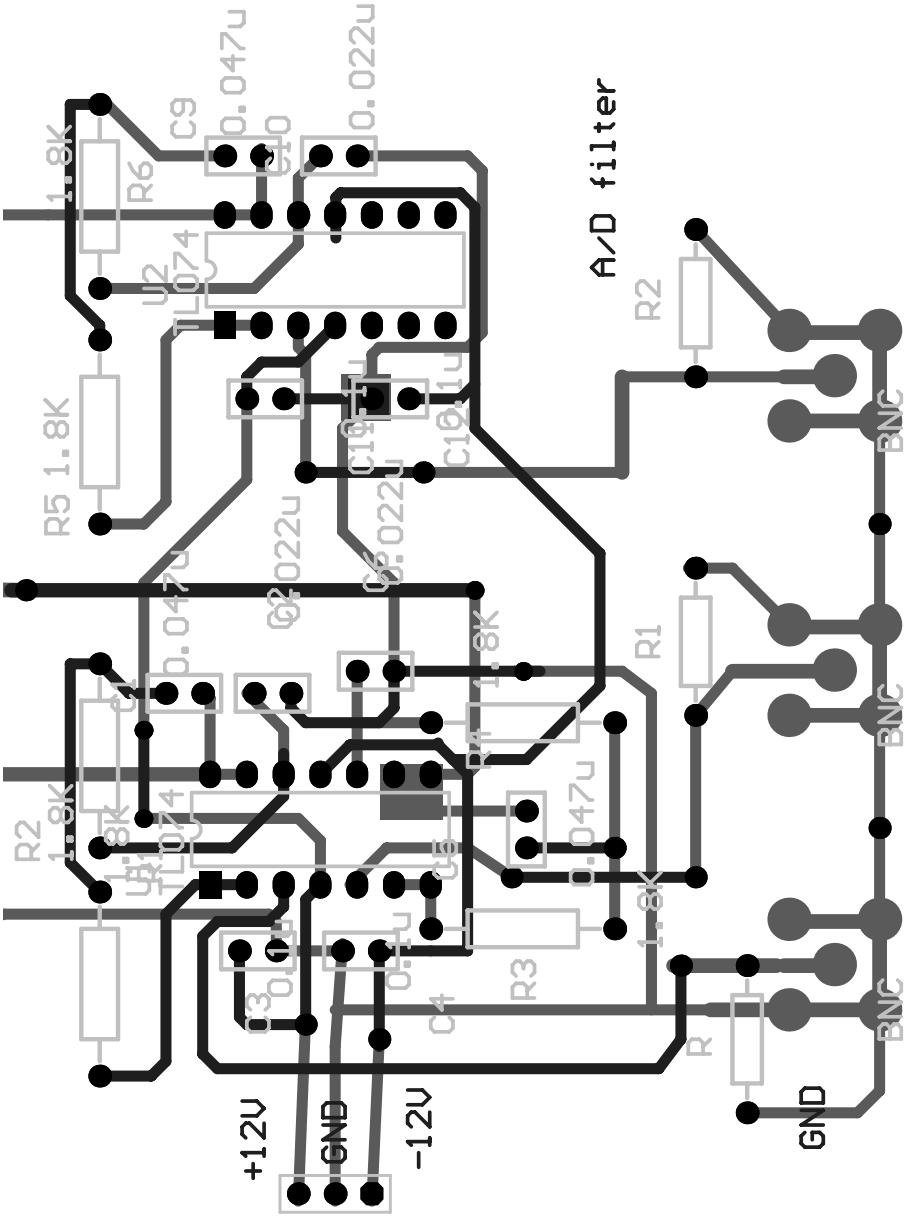

Figure B.4: Filter design layout

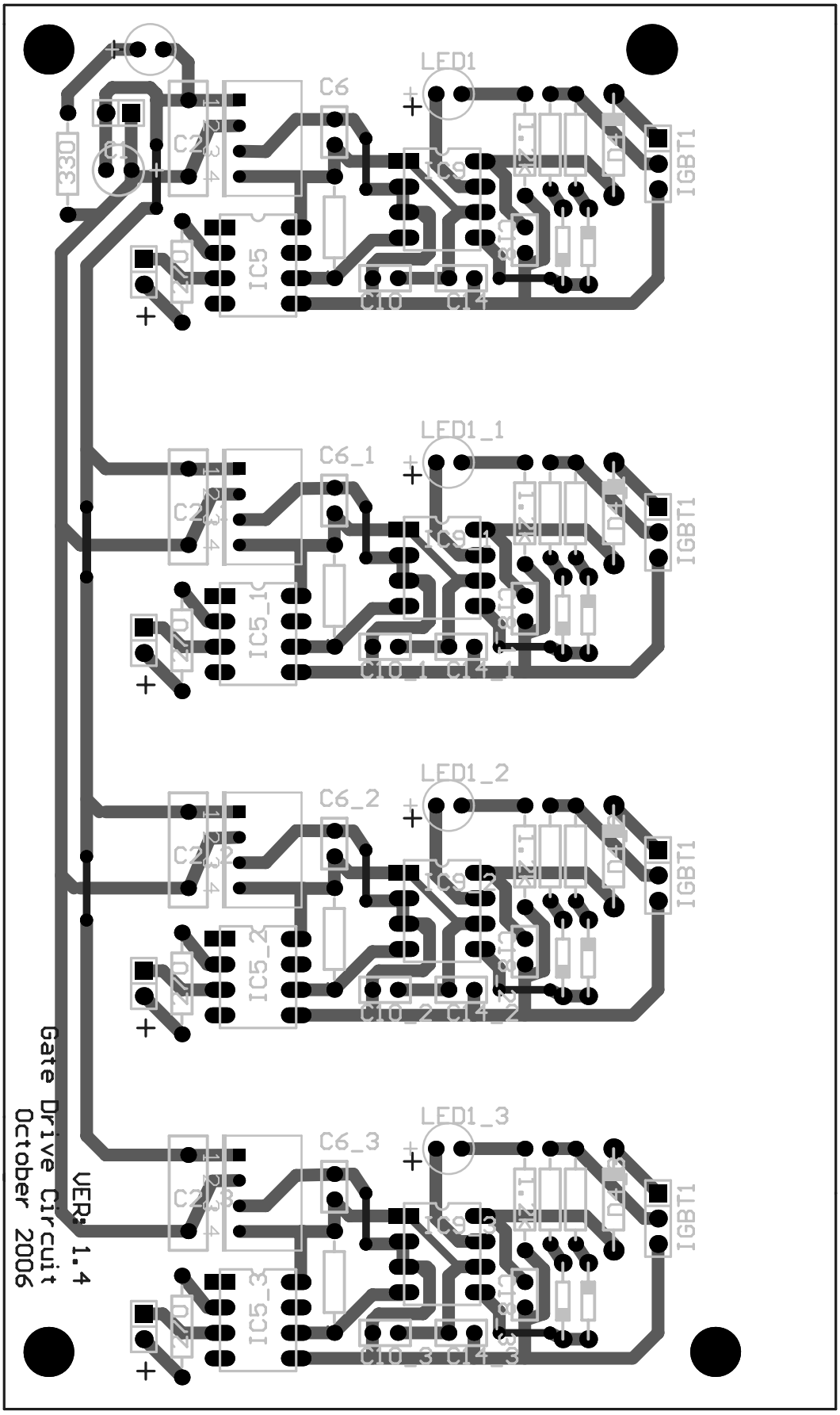

Figure B.5: Driver circuit layout

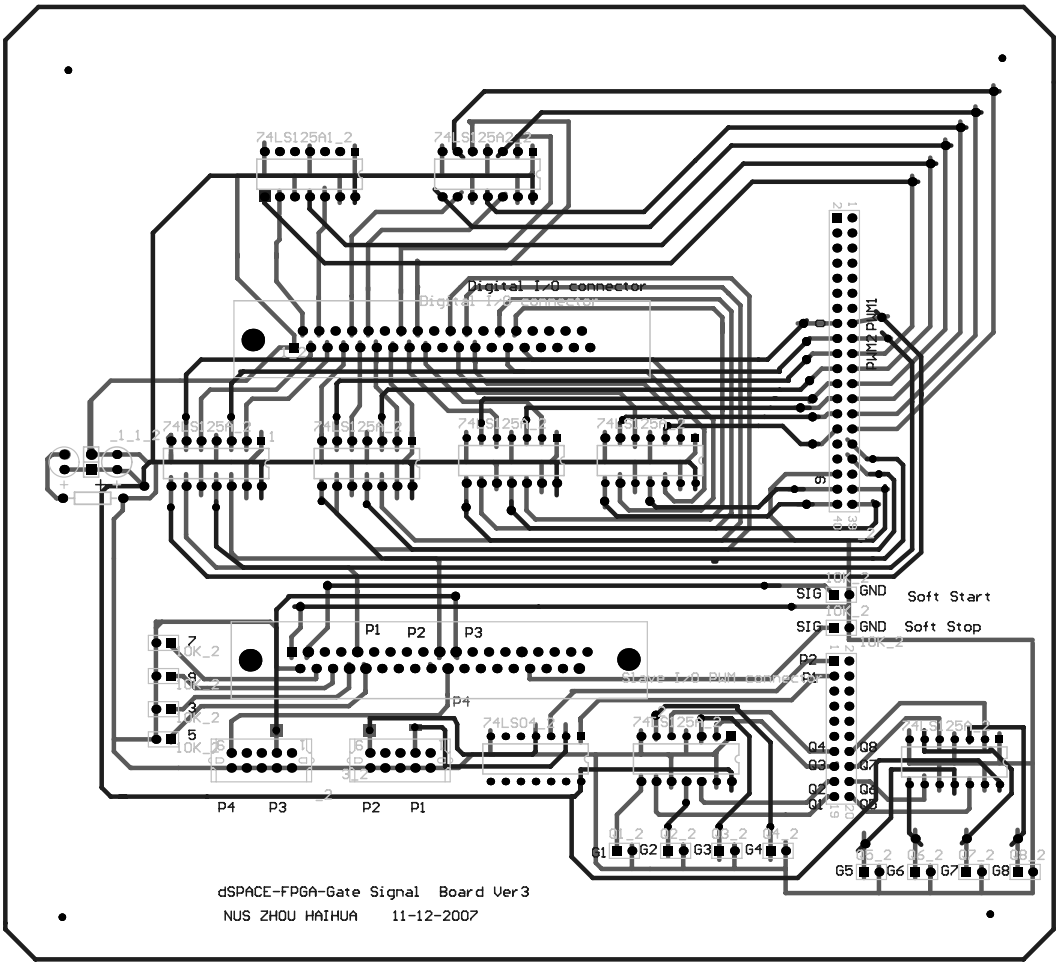

Figure B.6: Interface board between FPGA and dSPACE

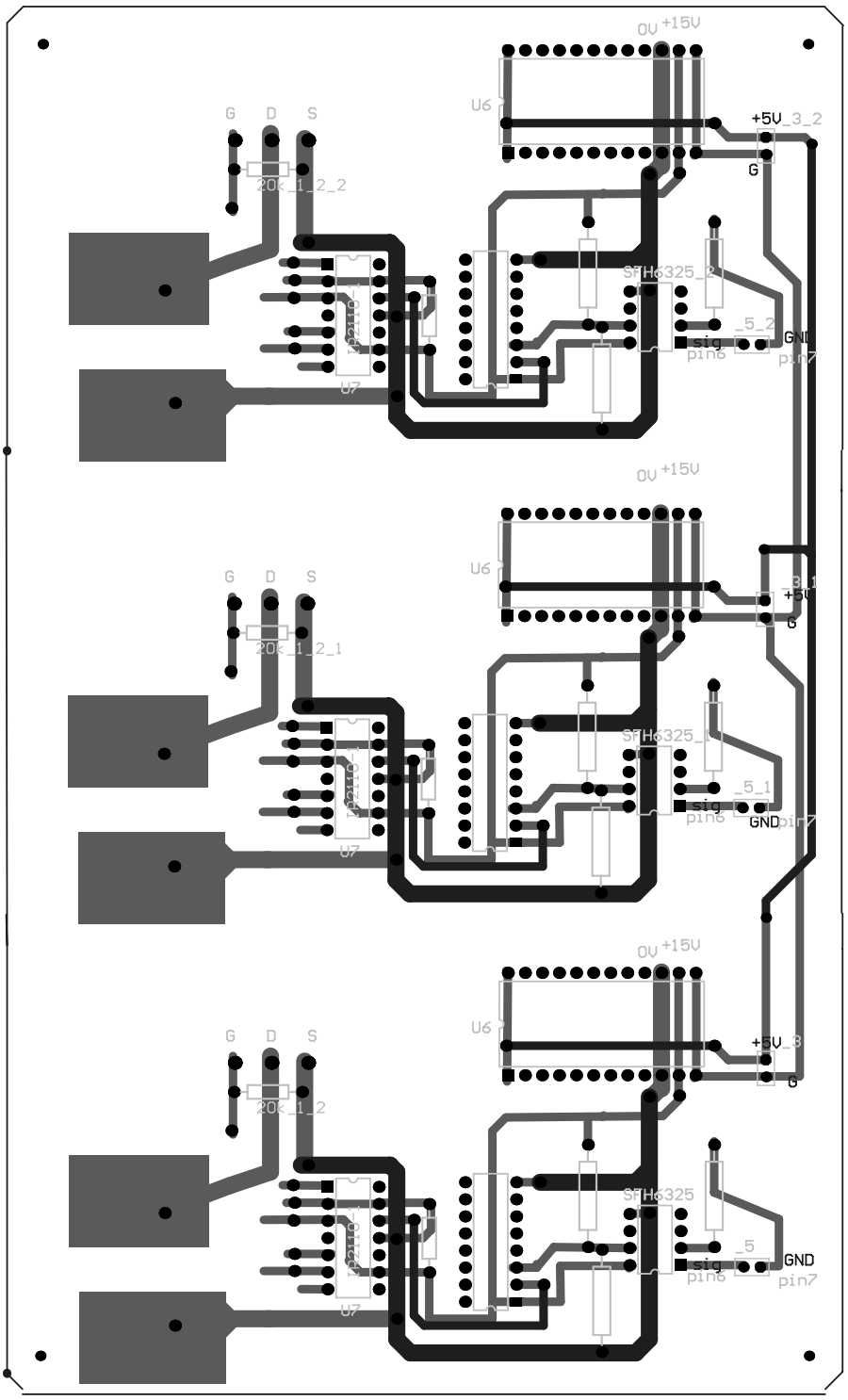

Figure B.7: Load switches board

List of Publications

Journal Publications

1. **Haihua Zhou** and Khambadkone, A.M. (2009), "Hybrid Modulation for Dual Active Bridge Bi-Directional Converter With Extended Power Range For Ultracapacitor Application," Industry Applications, IEEE Transactions on 45(4): 1434-1442.

2. **Haihua Zhou**, Khambadkone, A.M. and Xin Kong (2009), "Passivity Based Control for an Interleaved Current Fed Full Bridge converter With a Wide Operating Range using the Brayton Moser Form," Power Electronics, IEEE Transactions on 24(9): 2047-2056.

3. **Haihua Zhou**, Tanmoy Bhattacharya, Duong Tran, Terence Siew and Khambadkone, A.M, "Composite Energy Storage System Involving Battery and Ultracapacitor with Dynamic Energy Management in Microgrid Application," Accepted by IEEE Transaction of Power Electronics special issue "Power

Electronics for Microgrid", 2010

Conference Publications

1. **Haihua Zhou**, Tanmoy Bhattacharya, Duong Tran, Terence Siew and Khambadkone, A.M., "Composite Energy Storage System Using Dynamic Energy Management in Microgrid Applications," 2010 International Power Electronics Conference (IPEC), pp.1163 - 1168 , June 2010

2. **Haihua Zhou**, Tanmoy Bhattacharya, Duong Tran, Terence Siew and Khambadkone, A.M., "Composite Energy Storage System with Flexible Energy Management Capability for Micro-grid Applications," IEEE Energy Conversion Congress and Expo (ECCE) , pp.2558 - 2563 Sep.2010

3. **Haihua Zhou**, Tran Duong, Terence Siew, Khambadkone, A.M., "Interleaved Bi-directional Dual Active Bridge DC-DC Converter for Interfacing Ultracapacitor In Micro-Grid Application," 2010 IEEE International Symposium on Industrial Electronics (ISIE), pp.2229 - 2234, July 2010

4. Tran Duong, **Haihua Zhou** and Khambadkone, A.M., " A simple design of DC power system with multiple source-side converters to operate stably under constant power load," 2010 2nd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), , pp. 520-525, June 2010

5. **Haihua Zhou** and Khambadkone, A.M., "Hybrid Modulation for Dual Active Bridge Bi-Directional Converter With Extended Power Range For Ultracapacitor Application," IEEE 43nd Industry Applications Conference, IAS08, pp.1-8, Oct 2008

6. **Haihua Zhou**, Khambadkone, A.M. and Xin Kong, "A Passivity Based Control with Augmented Integration for an Interleaved Current Fed Full Bridge Converter as a Front End for Fuel Cell Source," IEEE 42nd Industry Applications Conference, IAS07, pp.643-649, Sep 2007

7. **Haihua Zhou**, Khambadkone, A.M. and Xin Kong, " Fast Dynamic Response in a Fuel Cell based Converter using Augmented Energy Storage," IEEE 38th Power Electronics Specialists Conference, PESC07, pp.1255-1260, Jun 2007