# STRAINED MULTIPLE-GATE TRANSISTORS WITH SI/SIC AND SI/SIGE HETEROJUNCTIONS

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# STRAINED MULTIPLE-GATE TRANSISTORS WITH SI/SIC AND SI/SIGE HETEROJUNCTIONS

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# Summary

High performance multiple-gate transistors such as FinFETs are likely to be required beyond the 32 nm technology node. Process-induced strain techniques can significantly enhance the carrier mobility in the channels of such transistors. In this dissertation work, complementary lattice mismatched source and drain stressors are studied for both n and p-channel multiple-gate transistors. $Si_{1-y}C_y$ (or SiC), which has a lattice constant smaller than that of Si, is employed to induce uniaxial tensile strain in the channel regions of n-channel devices. $Si_{1-x}Ge_x$ (or SiGe), which has a lattice constant larger than that of Si, is employed to induce uniaxial compressive strain in the channel regions of p-channel devices.

For n-channel devices, various integration challenges pertaining to SiC S/D stressors were identified and addressed. Evaluation of the electrical performance of such strained devices was also performed, showing that significant drive current enhancement can indeed be achieved. Backscattering characterization was also performed to clarify the carrier transport behaviour of strained FinFETs with SiC S/D stressors. The compatibility of the SiC stressor with high stress tensile SiN capping layer was also shown.

Further enhancement of devices with SiC S/D stressors was also investigated. A novel technique involving spacer removal prior to backend passivation layer (or contact etch-stop layer) deposition was proposed and experimentally shown to increase the influence of the S/D stressor on the channel regions, allowing greater performance benefits to be obtained at very low cost. It was also shown that the contact silicide (NiSi:C) can be tuned for higher intrinsic tensile stress, so as to induce

further tensile strain in the channel. This will be of great importance in achieving low parasitic series resistances as well as high channel stress.

For further scalability of SiC S/D stressor technology, in-situ doped SiC films were explored as an alternative to implantation doped SiC films. In-situ doping makes a high temperature S/D activation anneal unnecessary. This has the effect of suppressing the loss of carbon substitutionality, preserving it in its as-grown state. This makes it easier to control the final substitutional carbon percentage in the film as it is now solely controlled by the epitaxial growth process conditions.

For p-channel devices, enhancements to the conventional embedded SiGe S/D stressors were sought. The Ge condensation technique was investigated for vertically standing fins. The results show that up to 90% Ge content can be obtained using the condensation technique. It was also observed that substrate compliance suppresses dislocation formation. Applying this technique to the SiGe S/D regions of p-channel devices resulted in simultaneous Ge enrichment and embedding of the S/D stressors. The enrichment of Ge content as well as the increased proximity of the stressors to the channel resulted in further performance enhancement.

Ge S/D stressors were evaluated with ultra-thin body SOI planar and nanowire FETs. Enhanced substrate compliance in ultra-thin SOI and narrow structures resulted in dramatic performance enhancement from the Ge S/D stressors. A Ge melting technique for enhanced dopant diffusion and activation in the S/D stressors was also introduced. This technique resulted in further strain enhancement as a result of the simultaneous embedding effect.

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# Chapter 1

# 1. Introduction

## 1.1 Current Issues and Motivation

Since 1965, Moore's law [1.1],[1.2] has been the underlying principle which drives increasing performance in microprocessors. Historically, MOSFET scaling governed by Dennard's scaling criteria has resulted in performance improvements at each process generation. In particular, the gate delay ($C_{gate}V_D/I_{Dsat}$), which is one of the key determinants of switching speed, improves with conventional scaling. At each technology generation, the improvement in gate delay is about 30-40% [1.3]. However, conventional scaling is becoming increasingly challenging in nanoscale devices. In this regard, it is vital that new technological solutions are found.

Off-state leakage, which detrimentally impacts power consumption, will ultimately limit the smallest practical gate and channel lengths. Gate oxide scaling with $SiO_2$ is also limited at approximately 1.2 nm [1.4], beyond which high-κ dielectrics must be adopted. Although viable alternative dielectric candidates have been identified, numerous challenges still exist. As such, the multiple-gate device architecture becomes increasingly attractive, since it offers enhanced electrostatic control over the channel, which can relax the dielectric scaling requirements as the gate lengths are scaled down. In particular, FinFETs [1.5]-[1.10] or tri-gate FETs [1.11],[1.12] emerge as potentially manufacturable multiple-gate transistor designs.

At the same time, channel carrier mobility engineering using process-induced strain offers an alternative approach towards improving $I_{Dsat}$ performance, allowing performance targets to be attained with less aggressive scaling. The channel strain requirements for n and p-channel transistors are different, necessitating the utilization of different process-induced strain techniques. For future technology generations which may adopt the multiple-gate device architecture, it becomes clear that process-induced strain techniques for multiple-gate transistors must also be developed. In this thesis, strain engineering techniques using lattice-mismatched source and drain stressors for both n and p-channel multiple-gate transistors are explored.

## 1.2 Background

### 1.2.1 Multiple-Gate Transistors

Multiple-gate FETs provide better electrostatic control than single-gate FETs [1.13]. An example of the multiple-gate transistor is the double-gate (DG) FET. A schematic representation of the DG FinFET, a type of manufacturable DG FET which uses the two sidewalls of a vertically standing fin to form the device's channels, is shown in Figure 1-1. In the DG FET, the gate shields the channel from both sides and suppresses penetration of the field from the drain. This reduces short channel effects [1.14]. For single-gated FETs the substrate plays the part of the bottom shield. This results in a tradeoff between the degree of shielding and the reduction of the subthreshold slope [1.15]. In the DG FET this tradeoff does not exist. Furthermore both gates are strongly coupled to the channel, which increases the transconductance of the device. For the DG FET, the relative scaling advantage is about two times [1.14]. In symmetrical DG FETs such as DG FinFETs, the performance is further enhanced by higher channel mobility compared to a bulk FET. This is because the average electric field in the channel is lower, which reduces interface roughness scattering according to the universal mobility model [1.16],[1.17]. Using the DG FET as an example of multiple-gate FETs, it is not difficult to see the performance benefits of multiple-gate FETs over single-gate FETs.

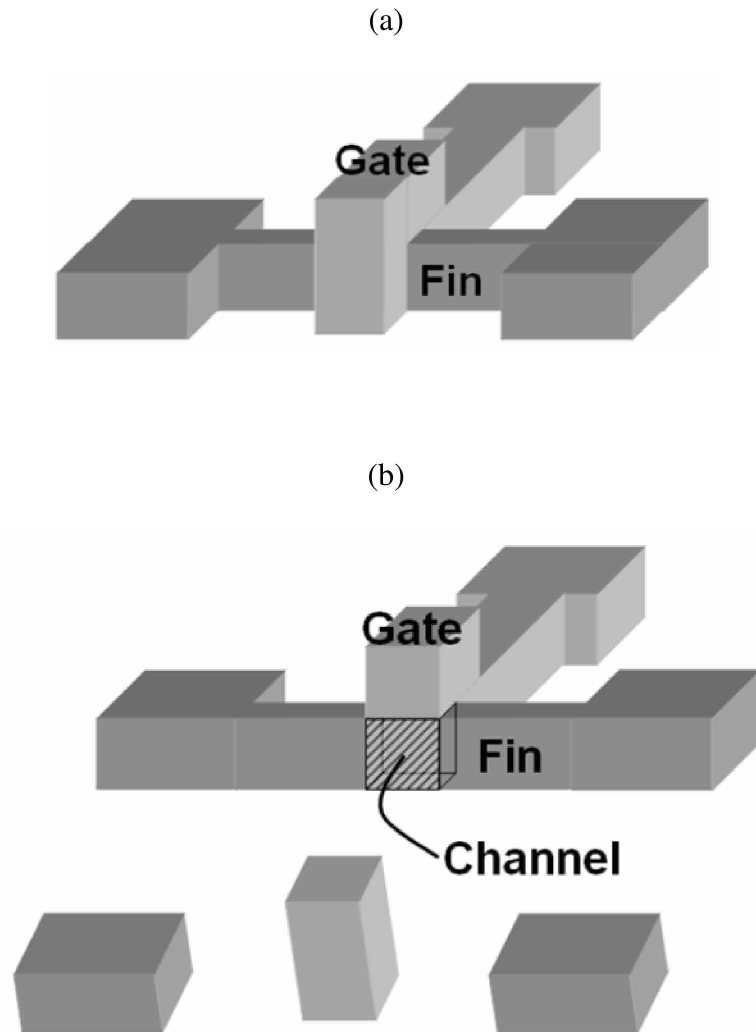


Figure 1-1 (a) Schematic illustrating the structure of a double-gate FinFET. (b) Schematic of the same structure which has been sliced vertically to reveal one of the two side channels of the device, which would otherwise be obscured by the gate which runs over the fin. (For the double-gate FinFET, the top of the fin is covered with a thick dielectric hardmask which prevents inversion of the top surface. In the tri-gate FinFET, this top hardmask is removed prior to gatestack formation, resulting in a total of 3 channel surfaces.)

## 1.2.2 Strained-Silicon

### *1.2.2.1 Strain Techniques*

Strained silicon techniques can be broadly classified into global and local strain techniques. In global strain techniques, the entire top layer of Si is strained. This is typically achieved by having a lattice-mismatched material underneath the strained-Si layer [1.18],[1.19]. For the case of biaxial tensile silicon, the layer underneath the strained-Si layer comprises relaxed SiGe. Recently, there have also been increasing reports on devices fabricated using strained-Silicon on Insulator (sSOI) substrates [1.20], [1.21]. These globally strained substrates are fabricated by the transfer of a strained-Si layer from one wafer to another wafer with an oxide layer on top, using wafer bonding and splitting techniques [1.22], [1.23]. However, global strain also implies that all devices on the wafer will be affected by the same strain. This can sometimes cause degradation of performance for one type of devices while enhancing the performance of another type of devices, due to the difference in strain requirements for n and p-channel FETs.

Local strain techniques involve the use of process-induced strain. One of the early reports on this involved high stress capping layers deposited on MOSFETs [1.24], [1.25]. This was studied as a method of inducing strain in the channel regions. Another method stemmed from the introduction of embedded SiGe in the source and drain regions of the transistor for higher boron activation and reduced external resistance [1.26]. This led to Intel's evaluation of this technology, which later led to conclusions that uniaxial compressive channel stress was a key contributor to the performance enhancement achieved. The evaluation of global versus local process-

induced uniaxial strain techniques eventually led to the industry's preference of local strain techniques. This was because uniaxial stress provides much larger hole mobility enhancement at low strain and high vertical electric field, as compared to biaxial stress. Another reason was that uniaxial stress techniques provide larger drive current enhancement for nanoscale devices with short gate lengths.

The clear advantages offered by process-induced uniaxial strain techniques resulted in their adoption at the 90-nm technology node [1.27]. Two process flows have been utilized to independently obtain the desired strain magnitude and polarity for n and p-channel FETs. One involved embedded and raised SiGe in the source and drain regions of p-channel devices and a high stress tensile SiN capping layer on the n-channel devices. The other utilizes capping layers of dual stress polarities. Compressive and tensile SiN liners are used for p and n-channel devices, respectively. Both process flows provide low cost yet effective performance benefits. Process-induced strain is hence present in nearly all high-performance logic technologies at 90, 65 and 45-nm technology nodes [1.28]-[1.36].

Besides lattice mismatched SiGe S/D stressors and high stress capping layers, other methods of channel strain engineering have also been reported. The techniques used are summarized in Figure 1-2. The alternative techniques of strain engineering include using shallow-trench isolation (STI) induced stress [1.37]-[1.39], silicide stressors [1.40]-[1.41], gate stressors [1.42]-[1.46] or beneath-the-channel lattice-mismatched stressors [1.47]-[1.48]. These techniques can be used separately or combined for further stress effects. However, entirely additive strain effects may not be obtained.

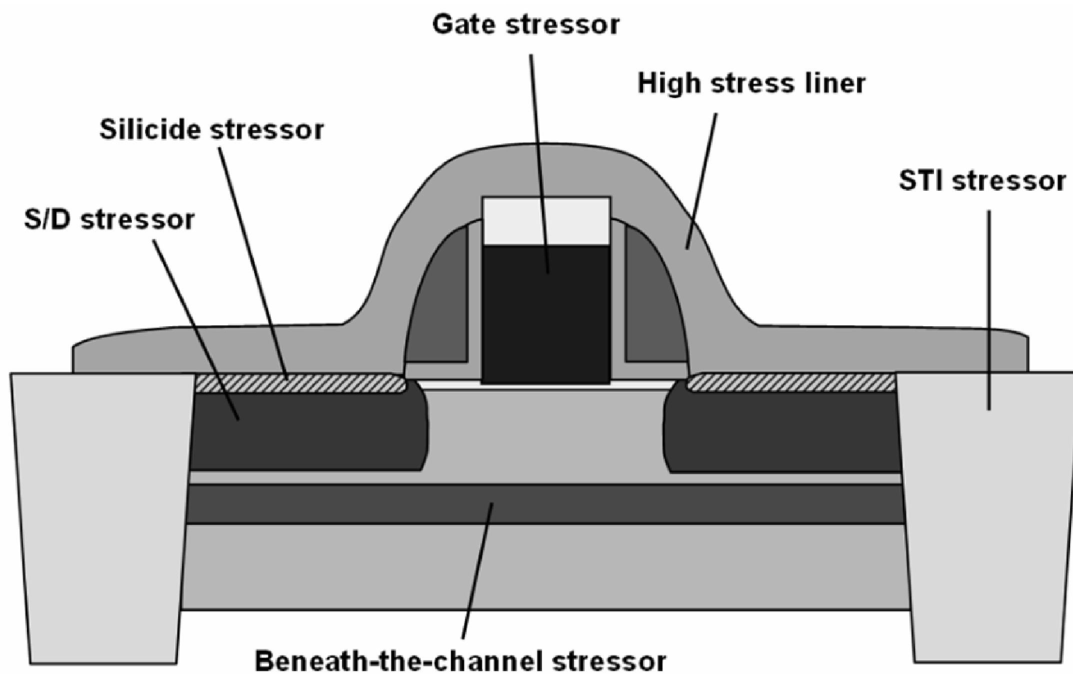


Figure 1-2 Schematic illustrating the various process-induced strain techniques for introducing stress in the channel.

There have been limited reports on strain engineering techniques for multiple-gate transistors. Reported techniques involve the use of SiGe S/D stressors [1.49],[1.50], high stress capping layers [1.51],[1.52] and sSOI [1.53]. However, the reported performance enhancement values from experimental device characterization have been relatively limited compared to single-gate planar devices. For anisotropically relaxed sSOI, there is also the problem of uniaxial tensile stress being present in the channels of both n and p-channel devices. While this enhances n-channel devices, the performance of p-channel devices is degraded, requiring an additional compressive liner to restore the performance [1.53].

#### *1.2.2.2 Physics of Strained-Si*

Strain alters the electronic band structure of Si and changes the carrier transport properties and carrier mobility. This section is meant only to be a brief introduction of the physics of strained-Si. In-depth discussions can be found in [1.54]-[1.55]. Strain causes energy-level splitting, inversion-layer quantum confinement energy-level shifts, average mass change due to carrier repopulation and band warping, two-dimensional (2-D) density of states, and interband scattering changes as a result of band splitting. The concepts are similar for holes and electrons, so it is simpler to look at the effect of strain on electron mobility. The electron mobility in strained bulk-Si is determined by electron occupation and scattering in the $\Delta_2$ and $\Delta_4$ valleys. This can be expressed by the following qualitative expression [1.54]:

$$\mu_{eff} = q\frac{\left(\tau_{\Delta_2}\frac{n_{\Delta_2}}{m_i^*}+\tau_{\Delta_4}\frac{n_{\Delta_4}}{m_i^*}\right)}{\left(n_{\Delta_2}+n_{\Delta_4}\right)} \qquad \text{(Equation 1-1)}$$

where $q$, $n$, $\tau$, $m$ are the electron charge, concentration, relaxation time, and conductivity mass in the FET channel direction, respectively. Strain increases the electron concentration in the $\Delta_2$ valley. The effective mass in the transport direction is smaller for the electrons in the $\Delta_2$ valley compared to the $\Delta_2$ valley. The electron repopulation improves the average in-plane conductivity mass. Strain also causes splitting between the $\Delta_2$ and $\Delta_4$. This reduces intervalley scattering and is also partially responsible for the enhancement when the energy split becomes comparable or larger than the optical phonon energy. The effect of strain on hole transport is more complicated since strain significantly warps the valence band. This alters both the in-plane and out-of-plane mass and 2-D density-of-states. The mass also changes with

stress and is not constant in *k* space. Nevertheless, the general concepts are similar. More details can be found in [1.54].

## 1.3 Objectives of Research

The objective of this dissertation work is to address important challenges of carrier mobility engineering in nanoscale multiple-gate transistors. An emphasis is placed on developing effective and potentially viable source and drain process-induced strain techniques for future high performance multiple-gate transistors.

## 1.4 Thesis Organization

Chapter 1 provides a brief introduction of the current technological status and explains the need for developing process-induced strain techniques for multiple-gate transistors. It also provides some background information regarding multiple-gate transistor architecture and strained silicon. Fundamental physics of strained silicon is also briefly introduced.

The core of this thesis can be primarily organized into 2 major parts. The first part (Chapters 2 and 3) describes the SiC source and drain (S/D) stressor induced strain for n-channel multiple-gate transistors, while the second part (Chapters 4, 5 and 6) focuses on SiGe or Ge S/D technologies for p-channel multiple-gate transistors.

Chapter 7 concludes the thesis and gives suggestions for future work.

### 1.4.1 SiC S/D Technologies for N-Channel Multiple-Gate Transistors

In Chapter 2, the integration of SiC S/D stressors with n-channel FinFETs is explored. Its compatibility with high stress SiN ESL layers is also experimentally proven. Backscattering characterization was used to provide insights in the carrier

transport properties of such strained transistors. The approach of performing simple geometric scaling of key structural parameters and its effect on channel strain is also shown.

In Chapter 3, novel techniques for further enhancing strained multiple-gate transistors with SiC S/D stressors were proposed and experimentally validated. A spacer removal technique which increases the influence of the S/D stressors on the channel without physically moving the stressors closer to the channel regions is described. A high-stress contact silicide was also developed for FinFETs with SiC S/D stressors, providing additional silicide-induced strain for further performance enhancement. It is further shown that in-situ doped SiC films removes limitations on carbon substitutionality typically experienced with conventional implantation-doped SiC films.

### 1.4.2 SiGe S/D Technologies for P-Channel Multiple-Gate Transistors

In Chapter 4, the enriching effect of Ge condensation on Ge concentration in three-dimensional structures (resembling fins) is investigated and described. The effect of substrate compliance on the strain relaxation mechanism in such vertical structures is also investigated.

Chapter 5 describes the results obtained with applying Ge condensation to FinFETs with SiGe S/D regions, which simultaneously allows Ge enrichment and embedding of the SiGe S/D stressors.

In Chapter 6, the integration of pure Ge S/D stressors with multiple-gate transistors is described. The effect of substrate compliance in ultra-thin SOI substrates,

as well as narrow quasi-nanowire structures, on the stressor's effectiveness is reported. A method for uniformly doping the Ge S/D regions is also presented.

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# Chapter 2

# 2. Silicon Carbon ($Si_{1-y}C_y$) Source and Drain Technology for N-Channel Multiple-Gate FETs

## 2.1 Introduction

In Chapter 1, it has been explained that uniaxial tensile strain in the channel can lead to electron mobility enhancement. $Si_{1-y}C_y$ alloys have smaller lattice constants than Si. The incorporation of SiC in the source and drain (S/D) regions of a transistor can induce uniaxial tensile strain in the channel. In this section, the feasibility of integrating SiC S/D stressors with n-channel multiple-gate transistors (FinFETs) is experimentally evaluated for the first time.

## 2.2 Lattice Strain Effects with Silicon Carbon Source and Drain Stressors

### 2.2.1 Device Fabrication

FinFET devices with two channel orientations were fabricated, characterized and analyzed. The key difference between the Si S/D control devices and the strained SiC S/D devices is the material comprising the raised S/D regions, as shown in Figure 2-1.

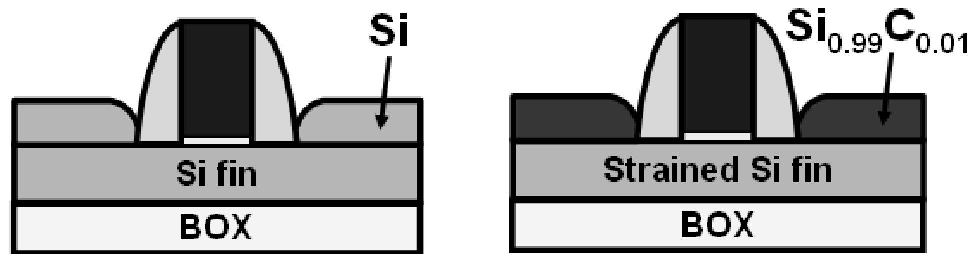



Figure 2-1 Schematic showing the difference between Si S/D control and the SiC S/D strained devices. SiC S/D strained devices have $Si_{0.99}C_{0.01}$ films grown in the S/D regions. The lattice mismatched SiC S/D stressors induce uniaxial tensile strain in the transistor's channel regions.

In the experiment, tri-gate FinFET devices were fabricated on SOI wafers with a 140 nm thick buried oxide and a 50 nm thick Si. A process flow schematic showing the key steps in the device fabrication flow is shown in Figure 2-2. The device fabrication process flow is summarized as follows: P-well and $V_t$ adjust implants were performed and activated. Fins were patterned using 248 nm lithography. After photoresist trimming and etching, fin widths down to 30 nm were obtained. $SiO_2$ of 20Å was used as a gate dielectric. Poly-Si gate material was then deposited. Gate implant was performed and activated. A $SiO_2$ hardmask was then deposited. After gate patterning, photoresist trimming and etching, gate lengths down to 25 nm were obtained. The formation of spacers involved further in-situ etching after normal over-etching to remove nitride stringers which would otherwise surround the Si mesas. This exposes the sidewall of the fins, enabling epitaxial growth of the lattice-mismatched SiC on both the top surface and sidewalls of the fins to maximize strain effects. This will be discussed in greater detail later. The control FinFETs have ~40 nm raised Si S/D for effective reduction of series resistance. This allows for a fairer comparison between strained devices and control Si S/D devices.

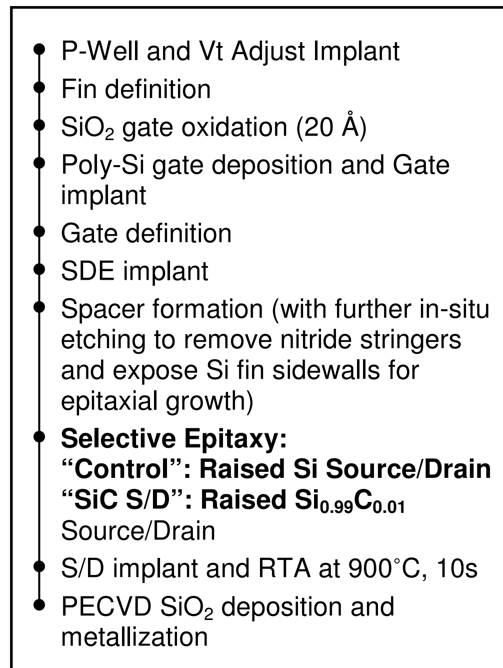



Figure 2-2 Process flow schematic showing the key steps in the fabrication of FinFETs with SiC S/D stressors and control devices.

All device splits were then implanted with $P^+$ and $As^+$ ions. The $As^+$ implants were targeted at the surface of the raised S/D regions, while the $P^+$ implants were targeted at the middle of the raised S/D regions. Following S/D dopant activation using RTA at 900°C for 10s, the devices went through standard $SiO_2$ passivation, contact formation and metallization steps. The metallization involves Al interconnects with a TaN barrier layer between the Al and Si. This metallization scheme is used throughout for all the devices with metallization fabricated for this dissertation work.

## 2.2.2 Selective Epitaxial Growth of $Si_{1-y}C_y$

### *2.2.2.1 Cyclic Growth/Etch Process Details*

A brief in-situ baking at high vacuum was performed to remove native oxide on the Si fin surface prior to the selective epitaxial growth of $Si_{1-y}C_y$ in an Ultra-high Vacuum Chemical Vapor Deposition (UHVCVD) epitaxy reactor (Canon Anelva I-

2100SRE). To achieve selective epitaxial growth of $Si_{1-y}C_y$, the epitaxy reactor uses a cyclic process, with each cycle comprising a growth and an etch step. For the growth step, methylsilane and disilane were used as the growth precursor gases for the epitaxy growth. The concentration of carbon incorporation was tuned by adjusting the partial pressures of methylsilane to disilane. This was determined by high resolution XRD, which is capable of resolving the substitutional carbon content. The XRD also confirms the high crystalline quality of the $Si_{1-y}C_y$. The growth of $Si_{1-y}C_y$ has intrinsic selectivity to dielectrics such as $SiO_2$ and SiN for a brief period of time known as the incubation period. However, this incubation period is often far too short for sufficient thicknesses of $Si_{1-y}C_y$ to be grown in the S/D regions of the transistor. For the etch step, undiluted chlorine is introduced as the etchant. During the etch step, any small $Si_{1-y}C_y$ islands which have grown on the dielectrics are etched away. The cyclic process essentially takes advantage of the growth rate differences between the Si S/D regions and the dielectric regions such as isolation $SiO_2$ and SiN gate spacers to achieve completely selective growth on the S/D regions only. Figure 2-3 shows the SEM images of FinFET S/D regions after selective epitaxial growth of $Si_{0.99}C_{0.01}$

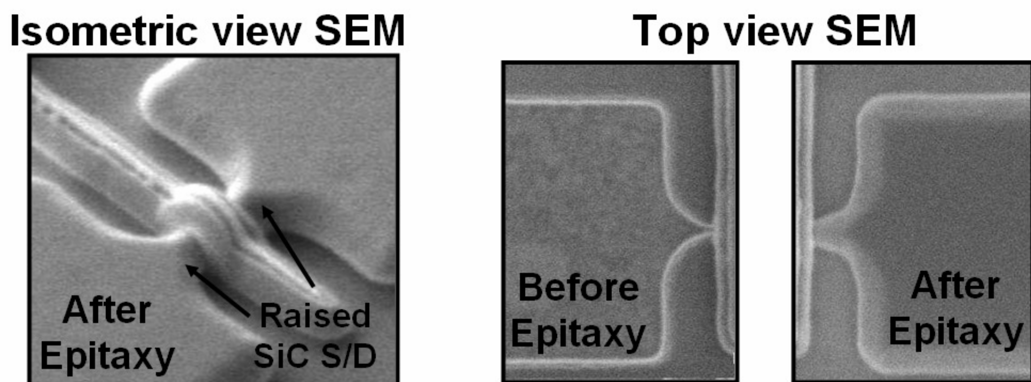



Figure 2-3 SEM images showing the successful growth of $Si_{0.99}C_{0.01}$ in the S/D regions of FinFET transistors. Excellent selectivity to the SiN gate spacers and isolation $SiO_2$ was achieved.

#### *2.2.2.2 Si migration and SOI agglomeration during Pre-epitaxy UHV Anneal*

Prior to epitaxial growth of $Si_{1-y}C_y$ in the epitaxy reactor, a brief in-situ anneal in ultra-high vacuum (UHV) is usually performed to volatilize and remove any native oxide that has grown after the pre-epitaxy wet clean. For bulk substrates, temperatures between 750 to 800 deg C are typically used. For thin-body SOI planar FETs and FinFETs, integration problems are encountered as shown in Figure 2-4. It has been reported that SOI films can undergo agglomeration during annealing in UHV [2.1], due to the surface-energy-driven dewetting tendency of SOI [2.2]. This problem is even worse near pattern edges [2.3], [2.4]. This explains the agglomeration effects observed in Figure 2-4.

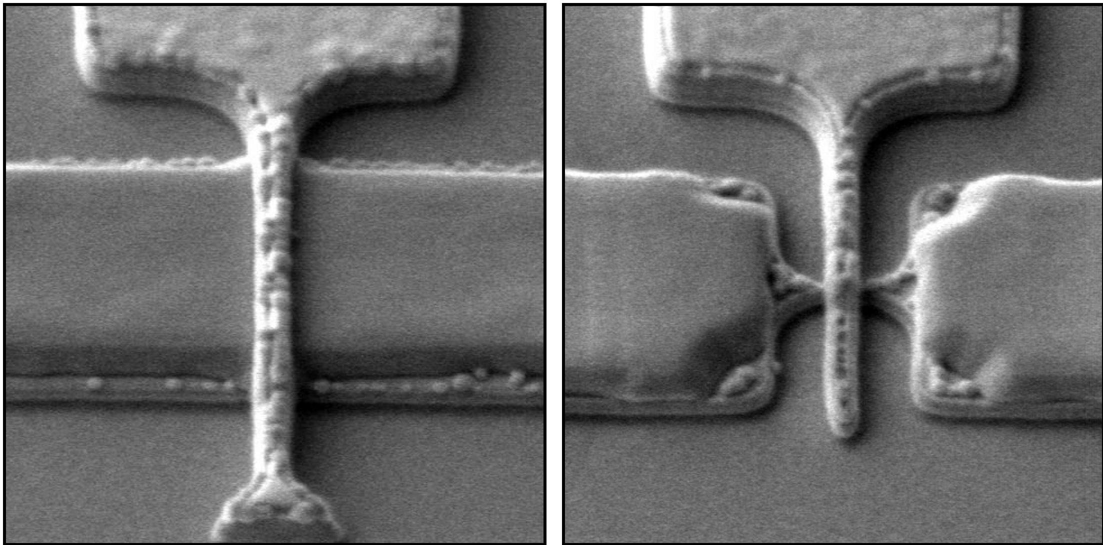


Figure 2-4 SEM images showing (a) agglomeration at edges of the S/D area in SOI planar FETs and (b) agglomeration at the fin extensions between the gate and the S/D regions.

To obtain agglomeration-free epitaxial growth of $Si_{1-y}C_y$, the UHV anneal temperature was reduced to ~680°C. This enabled the successful epitaxial growth as shown earlier in Figure 2-3. For even thinner substrates or narrower fins, the tendency to agglomerate may be increased, which requires even further lowering of the anneal temperature. However, an anneal temperature that is too low may result in incomplete removal of native oxide. This can affect the film quality. In order to tackle this issue in manufacturing, it is proposed that future epitaxy tools for FinFET or ultra-thin body SOI planar devices should include an in-situ wet chemical oxide removal chamber. This allows the native oxide to be removed in-situ at low temperatures.

#### *2.2.2.3 Epitaxial growth on FinFET devices with different channel orientations*

The fins were formed with two orientations: $\theta = 0^{\circ}$ and $\theta = 45^{\circ}$. These are the commonly used device orientations in CMOS layouts. The surface orientations of the top and side channels of these differently-oriented devices are shown in Figure 2-5. Selective epitaxial growth formed ~35 nm of $Si_{0.99}C_{0.01}$ in the S/D regions of the strained FinFETs. The SiC growth on 0° and 45°-oriented devices was observed to be very similar (Figure 2-6). This allows comparison between 0° and 45°-oriented devices at approximately the same $Si_{1-y}C_y$ stressor thicknesses. From the difference in piezoresistance coefficients for (110)/<110> and (100)/<100> [2.5], [2.6], we can deduce that strain sensitivities for these two channel orientations will be different. Hence, it is expected that the strain effects for differently oriented FinFETs with SiC S/D stressors will be different. The electrical results corresponding to devices of different orientations will be discussed in detail later.

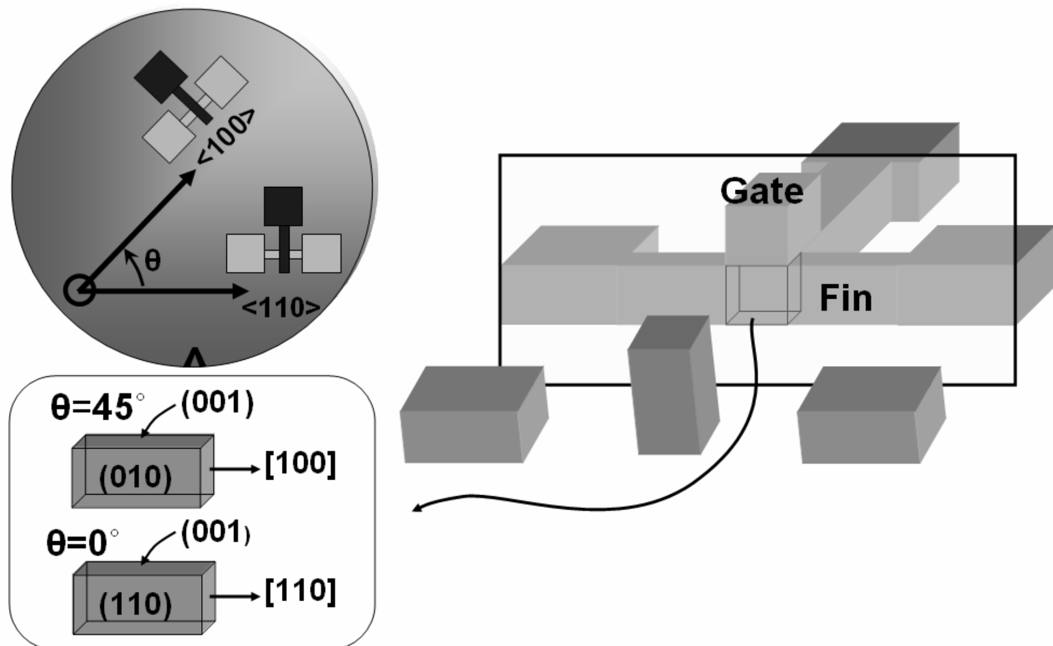



Figure 2-5 Schematic showing the channel direction and surface orientations of 0 and 45 degree oriented devices. The effect of strain on different channel surface orientations and directions are different, as can be inferred from piezoresistivity coefficients.

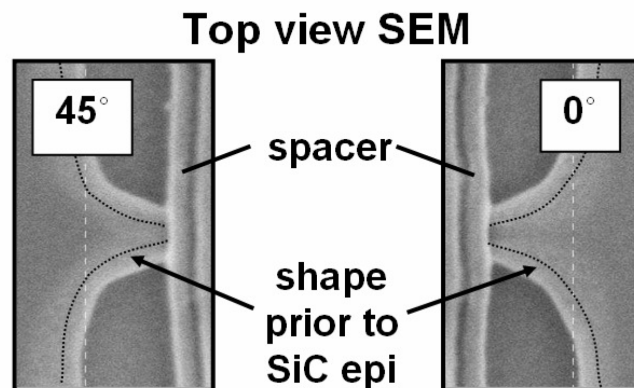



Figure 2-6 Top view SEM images showing the epitaxial growth of $Si_{0.99}C_{0.01}$ in the S/D regions of 0 and 45 degree oriented devices. The thicknesses of the epitaxial films grown in the S/D regions are quite comparable.

#### 2.2.2.4 *Stress effect of Π-shaped stressors compared to embedded stressors*

The spacer formation process allows the $Si_{1-y}C_y$ stressors to be grown on the top surface as well as the side surfaces of the FinFET's S/D regions, forming Π-shaped stressors. A schematic which describes this spacer formation process is shown in Figure 2-7. An extra in-situ over-etch during the spacer formation step removes the nitride spacer stringers from the S/D regions. Due to the height differences between the gate and the FinFET S/D regions, it is possible to remove the nitride stringers from around the S/D regions while preserving an adequately tall nitride gate spacer. A thicker $SiO_2$ gate hardmask can also be used to accentuate the height differences and to protect the gate from being exposed during epitaxial growth.

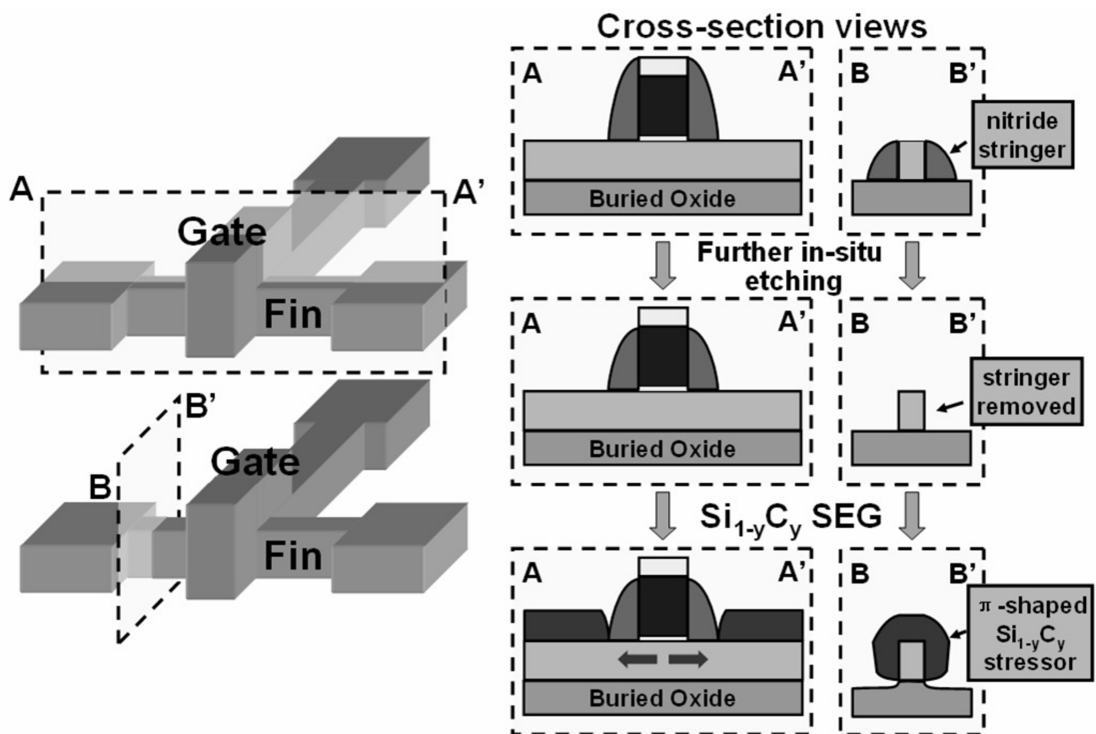



Figure 2-7 Process flow schematic showing how Π-shaped SiC S/D stressors can be integrated with multiple-gate FinFETs. An extra in-situ over-etch during the spacer formation step removes the nitride spacer stringers from around the S/D regions, allowing the epitaxial growth of $Si_{1-y}C_y$ on the top surface as well as the side surfaces of the S/D regions.

TCAD stress simulations were performed to compare the channel stress profiles of 2 transistors, one with the Π-shaped stressors, and the other with more conventional 50% embedded stressors. It is clear from Figure 2-8 that Π-shaped stressors enable much higher longitudinal stress values to be achieved in the FinFET channel as a result of increased lattice-strain coupling from the stressors to the channel. This increase in longitudinal stress will greatly boost the effectiveness of the $Si_{1-y}C_y$ stressors on increasing the electron mobility in the channel.

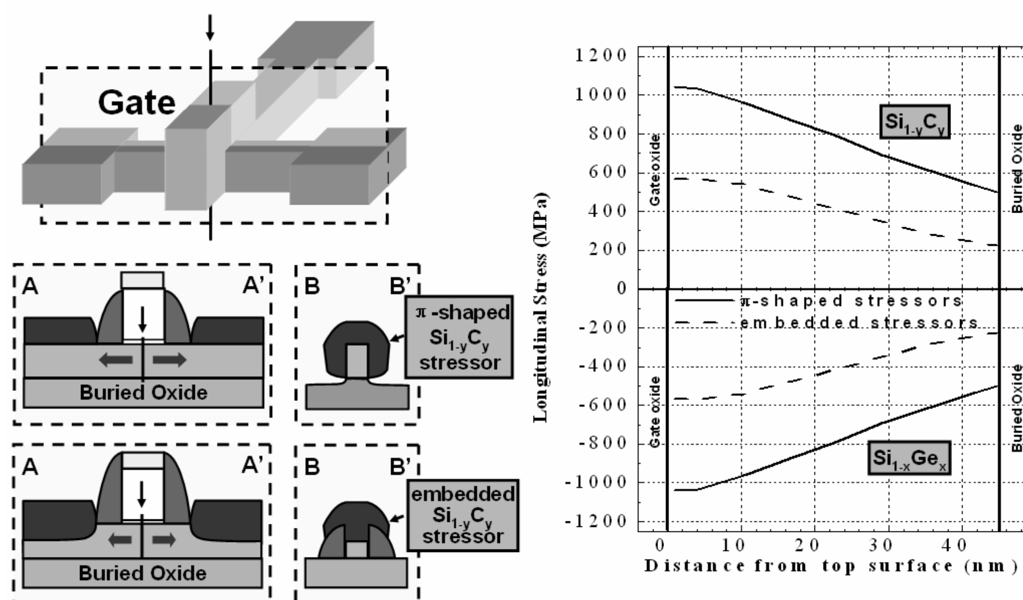



Figure 2-8 TCAD stress simulation provides a rough gauge of the enhancement in channel stress in FinFET devices with the proposed pi-shaped S/D stressors as compared to a device with 50% S/D embedding of the S/D stressors. The cut-line along which the stress is plotted is shown in the schematic.

## 2.2.3 Device Characterization

### *2.2.3.1 <100>-oriented devices (45°)*

First, the 45° oriented FinFET devices were examined. These devices have (100) sidewall channel surface orientations with a carrier transport direction of <100>.

Figure 2-9 shows the $I_{OFF}$-$I_{ON}$ plot for the SiC S/D strained FinFETs and the control FinFETs, highlighting the 20% $I_{Dsat}$ improvement at an $I_{OFF}$ of $10^{-7}$ A/µm. The $I_{Off}$-$I_{On}$ plot shows statistical information of the enhancement in performance, and is important for evaluating strain-induced $I_{Dsat}$ enhancement in our fabricated devices.

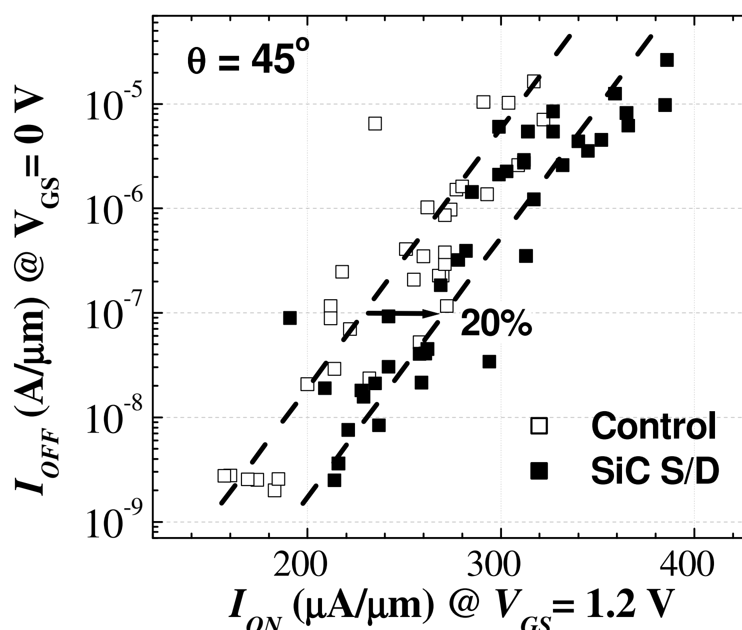



Figure 2-9 $I_{OFF}$-$I_{ON}$ plot comparing SiC S/D devices and raised Si S/D control devices (θ = 45˚ for all devices), showing 20% improvement at $I_{OFF}$ = $10^{-7}$ A/µm.

To examine the device performance more closely, IV-characteristics for a pair of closely matched devices are examined in greater detail. Figure 2-10 shows the $I_{DS}$-$V_{GS}$ characteristics of two closely matched 45˚-oriented FinFETs with $L_G$ = 25 nm, fin width $W_{fin}$ = 35 nm, and similar $I_{OFF}$, subthreshold swing (100 mV/dec.), and DIBL (0.17V/V). Due to the process-induced spread in the device parameters, comparing devices with matched short channel effects (similar gate length) helps to provide greater fairness in obtaining the $I_{Dsat}$ enhancement. The strained FinFET with SiC S/D

shows 20% higher $I_{Dsat}$ than the control device (Figure 2-11). The $I_{Dsat}$ enhancement is attributed to uniaxial tensile strain induced in the channel by the $Si_{0.99}C_{0.01}$ S/D [2.7],[2.8]. Extraction of S/D series resistances (Figure 2-12) in these devices shows that the series resistances are closely matched to within 5%. This is expected because the control devices have raised Si S/D regions as well for reduced series resistances. Hence, we can attribute the drive current enhancement to strain.

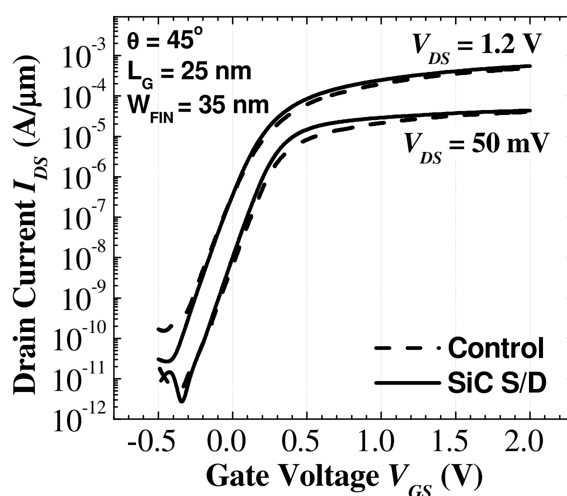



Figure 2-10 $I_D$-$V_G$ characteristics of SiC S/D device and raised Si S/D control device with the same off-state current, comparable DIBL and subthreshold swing (θ = 45° for both devices).

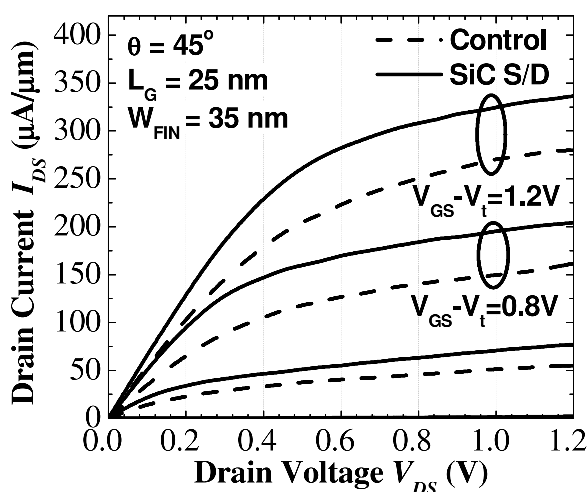



Figure 2-11 $I_D$-$V_D$ showing 20% saturation drive current enhancement of SiC S/D device over the raised Si S/D control device (θ = 45° for both devices).

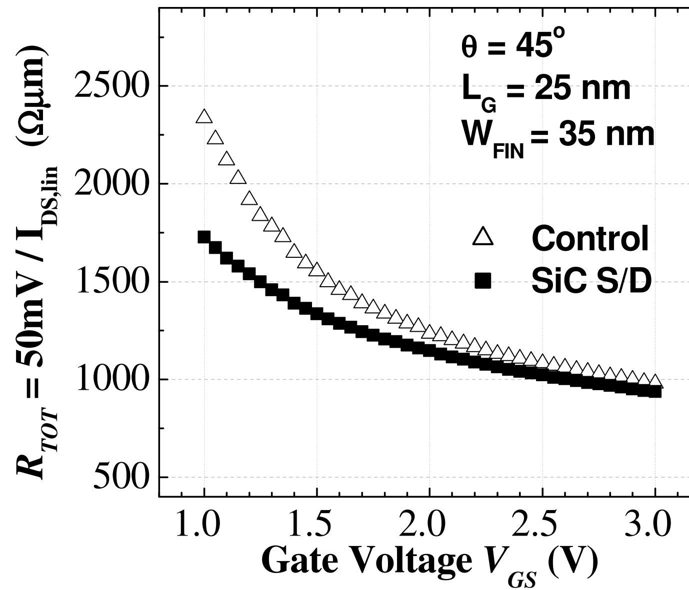



Figure 2-12 Estimation of series resistance by examining the value of total resistance, given the asymptotic behavior of total resistance at large gate bias. The series resistances for both SiC S/D and raised Si S/D control devices are closely matched to within 5% (θ=45˚ for both devices).

#### *2.2.3.2 <110>-oriented devices (0°)*

Next, the performance enhancement of <110>-oriented devices is examined. These devices have (110) sidewall channel surface orientations with a carrier transport direction of <110>. The top surface orientation (100) is the same as that of the <100>-oriented devices. However, it should be noted that the carrier transport direction is <110> instead of <100>. While this difference in carrier transport direction is not significant for unstrained devices, it does make a difference for strained devices due to the anisotropic strain sensitivities of the (100) channel surface to strain applied in the <100> and <110> directions. Figure 2-13 shows the $I_{Off}$-$I_{On}$ plot for <110> oriented devices. The enhancement in $I_{Dsat}$ performance is far less pronounced than that obtained with <100> oriented devices. This is attributed to the reduced strain sensitivity of the (110) surface to tensile strain in the <110> direction

as compared to that of the (100) surface in the <100> direction [2.5], [2.6]. At the same time, it also gives indirect evidence that the $I_{Dsat}$ enhancement is indeed strain induced electron mobility enhancement.

The increased spread in the $I_{Off}$-$I_{On}$ data points can be attributed to process uniformity issues of the fabricated devices. Furthermore, doped channel FinFETs tend to suffer from random dopant fluctuation effect, which causes threshold voltage fluctuation. To evaluate the $I_{Dsat}$ enhancement more closely, IV characteristics of matched pairs of devices were examined. Figure 2-14 shows the $I_{DS}$-$V_{GS}$ transfer characteristics of a pair of matched <110>-oriented devices. It can be seen that the DIBL and subthreshold swing values are comparable, which indicates that these two devices have comparable effective channel lengths. Figure 2-15 shows the $I_D$-$V_D$ family of curves, which shows the enhancement in $I_{Dsat}$ of about 7%. Figure 2-16 compares the S/D series resistances of the same devices. A simplified linear region drain current equation that includes a source/drain series resistance parameter was used to generate curves which fit each set of measured data points. The series resistances were estimated to be 594, and 614 Ωμm for “Si S/D” and “SiC S/D” respectively. The comparable series resistance values help to confirm that the drive current enhancement is indeed due to electron mobility enhancement as a result of longitudinal tensile strain.

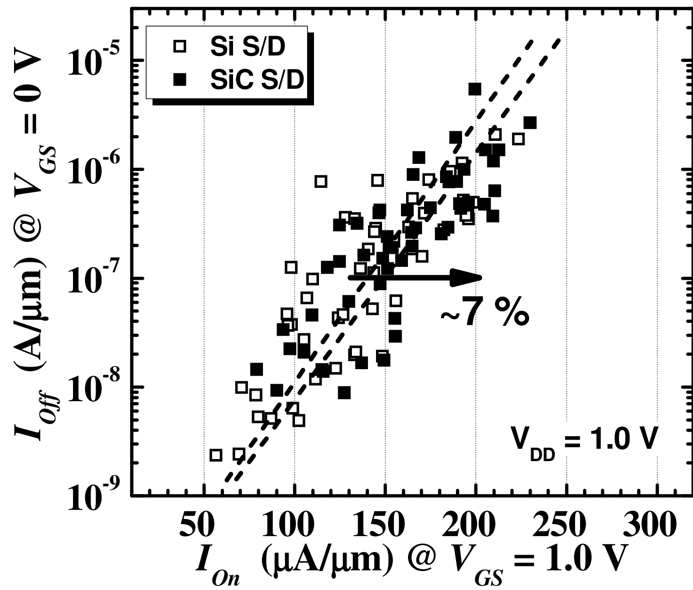



Figure 2-13 $I_{OFF}$-$I_{ON}$ plot comparing SiC S/D devices and raised Si S/D control devices (θ = 0° for all devices), showing 7% improvement at $I_{OFF}$ = $10^{-7}$ A/μm.

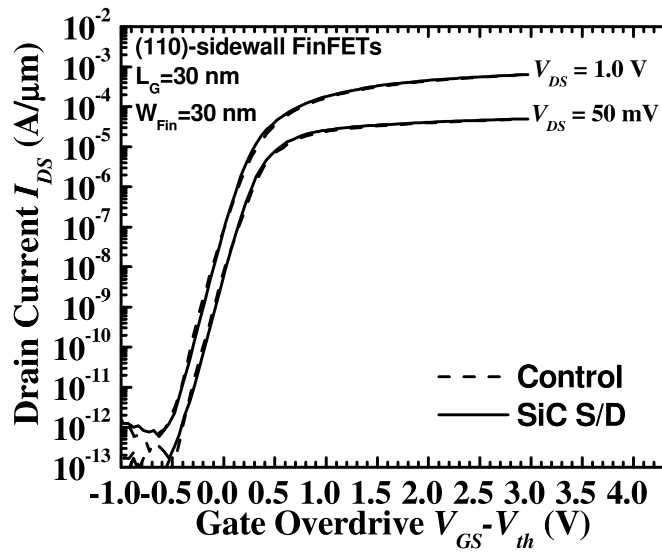



Figure 2-14 $I_D$-$V_G$ transfer characteristics of SiC S/D device and raised Si S/D control device with the same off-state current, comparable DIBL and subthreshold swing (θ = 0° for both devices).

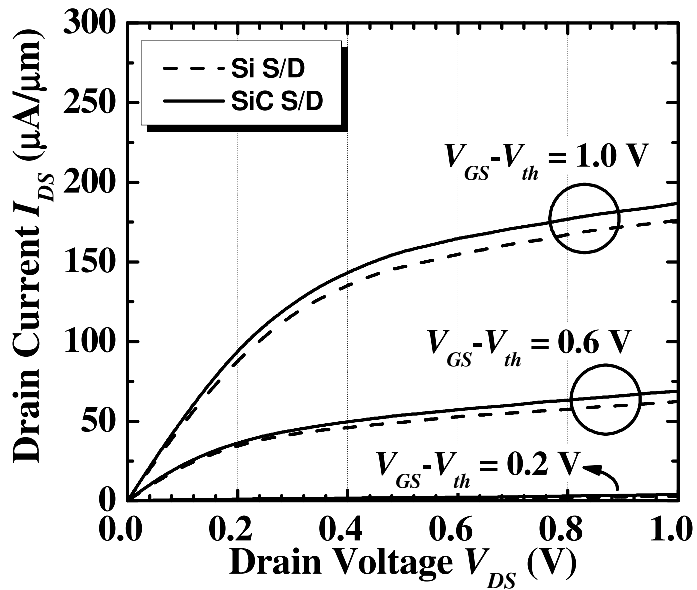



Figure 2-15 $I_D$-$V_D$ showing 7% saturation drive current enhancement of SiC S/D device over the raised Si S/D control device (θ = 0˚ for both devices).

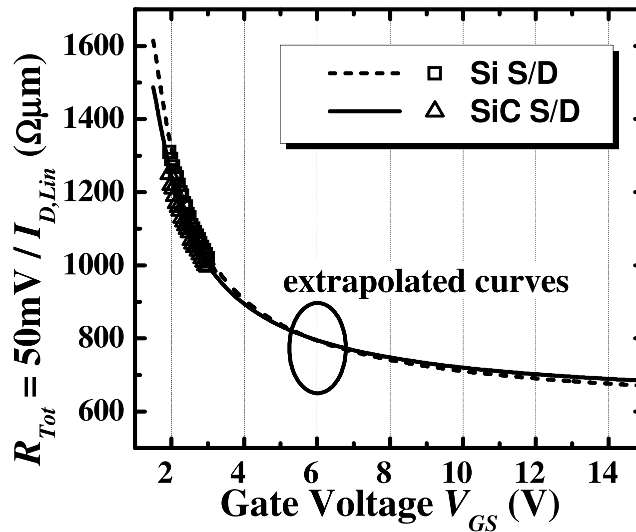



Figure 2-16 Extraction of series resistance by examining the asymptotic behavior of total resistance at large gate bias. (θ=0˚ for both devices). A simplified linear region drain current equation that includes a source/drain series resistance parameter was used to generate curves which fit each set of measured data points. The series resistances were estimated to be comparable, 594 and 614 Ωμm for "Si S/D" and "SiC S/D" respectively.

#### 2.2.3.3 Comparison between <100> and <110> oriented SiC S/D FinFETs

The longitudinal piezoresistance coefficients $|\Pi_l|$ for the channel surfaces of <100> and <110> oriented devices are plotted in Figure 2-17, alongside with $I_{Dsat}$ enhancement obtained for devices of each channel orientation. The results show that the $I_{Dsat}$ enhancement is almost directly proportional to the piezoresistance coefficients. Hence, the $I_{Dsat}$ enhancement values are consistent with theoretical predictions using piezoresistive theory for the channel surfaces being examined. This provides further evidence that the enhancement is due to strain, and not due to other parasitic effects such as series resistance or EOT differences.

Thus, it has been established that for FinFETs with SiC S/D stressors, the <100>-oriented devices have higher absolute performance, as well as higher strain-induced enhancement. It becomes obvious that <100>-oriented devices should be employed in CMOS layouts. This essentially means that in order to maximize both n and p-channel FinFET drive currents, fins with (100) and (110) sidewalls, respectively, should ideally be used (Note: Hole mobility is highest for the (110) surface orientation). However, this also incurs an area penalty which is undesirable in density-critical applications such as SRAM [2.9]. This area penalty can be avoided by using fins with (110) sidewalls for both n and p-channel FinFETs, which then compromises the performance of n-channel FinFETs due to drastically lower electron mobility on (110) surfaces. Thus, it seems that while significant 20% $I_{Dsat}$ enhancement can be obtained in <100>-oriented SiC S/D FinFET devices, <110>-oriented FinFET devices may not be sufficient to meet aggressive mobility enhancement targets set in the ITRS as the enhancement is only about 7%. In the next section, the co-integration of SiC S/D

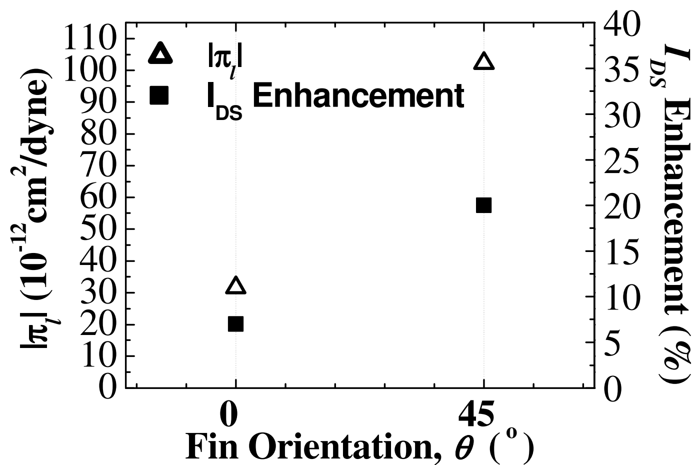



Figure 2-17 $I_{DSat}$ enhancement of SiC S/D over Control for the 45˚-oriented FinFETs is larger compared to the 0˚-oriented FinFETs. This is expected due to the larger magnitude of longitudinal piezoresistance coefficient, $|\Pi_l|$ for the channels in the 45˚-oriented FinFETs.

stressors with high stress nitride etch-stop layer stressors [2.10],[2.11] is examined to see if performance can be improved further.

## 2.3 Co-integration with High-stress Etch Stop Layer Stressors

### 2.3.1 Introduction

High stress SiN liners, which also act as contact etch-stop layers (CESL), can induce longitudinal tensile stress in the channel regions of transistors, improving the performance of n-channel transistors [2.10], [2.11]. In this section, the compatibility and performance benefits of SiN liner stress technology with $Si_{1-y}C_y$ S/D stressor technology is evaluated experimentally.

### 2.3.2 Device Fabrication

The device fabrication flow is similar to that described in section 2.2.1. The key difference is highlighted in the process flow schematic shown in Figure 2-18 while Figure 2-19 illustrates the difference between the SiC S/D+ESL split and the SiC S/D split. The high stress liner comprises 40 nm of SiN, which is deposited in a Low Pressure Chemical Vapor Deposition (LPCVD) furnace. Wafer curvature measurements on blanket wafers confirm the intrinsic stress values in the SiN to be +1.1 GPa (tensile). A cross-section TEM image of a device, as shown in Figure 2-20, illustrates the transistor structure of SiC S/D+ESL devices.

- P-Well and Vt Adjust Implant
- Fin definition
- $SiO_2$ gate oxidation (20 Å)
- Poly-Si gate deposition and Gate implant
- Gate definition
- SDE implant
- Spacer formation (with further in-situ etching to remove nitride stringers and expose Si fin sidewalls for epitaxial growth)
- **Selective Epitaxy:**<br>**"Control": Raised Si Source/Drain**<br>**"SiC S/D", "SiC S/D+ESL": Raised $Si_{0.99}C_{0.01}$ Source/Drain**
- S/D implant and RTA at 900°C, 10s
- **"SiC S/D+ESL": LPCVD ESL SiN (intrinsic stress: +1.1GPa)**
- PECVD $SiO_2$ deposition and metallization

Figure 2-18 Process flow schematic showing the key steps in the fabrication of FinFETs with SiC S/D stressors and control devices.

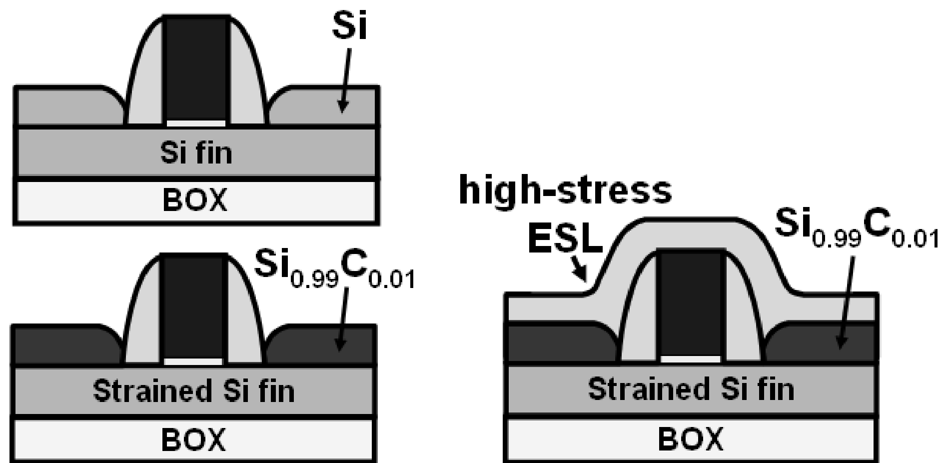



Figure 2-19 Schematic showing difference between Si S/D+ESL devices from the Si S/D control and the SiC S/D strained devices. SiC S/D+ESL devices are similar to SiC S/D devices, with the sole exception that a high-stress SiN capping layer (+1.1 GPa) was added as a contact etch-stop layer. This high-stress liner induces further stress in the device channel.

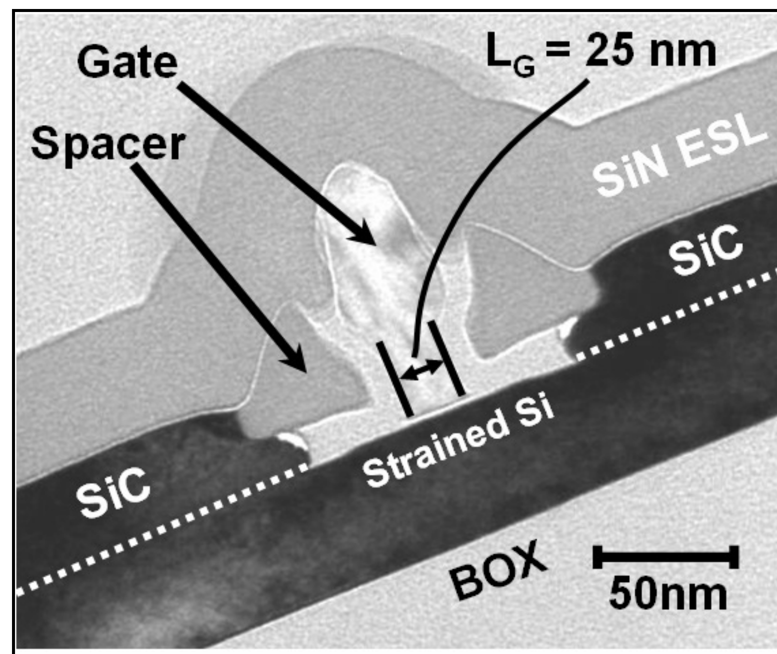



Figure 2-20 Cross-section TEM image showing the transistor structure of SiC S/D+ESL devices. Like SiC S/D devices, $Si_{0.99}C_{0.01}$ is grown in the S/D regions. After S/D implantation and activation, the high stress SiN ESL is deposited as a second stressor.

### 2.3.3 Device Characterization

#### *2.3.3.1 <100>-oriented devices (45°)*

The performance benefits of co-integrating SiC S/D stressors with a high-stress SiN ESL liner is first examined with <100>-oriented devices. From the $I_D$-$V_G$ transfer characteristics shown in Figure 2-21, it is clear that the SiC S/D+ESL device does not show any sign of short channel degradation as a result of the added thermal budget experienced during the LPCVD SiN liner deposition, as can be seen from the comparable DIBL and subthreshold swing values. The $I_D$-$V_D$ curves for the same devices show 20% $I_{Dsat}$ enhancement of the SiC S/D device over the control. A 30% further enhancement in $I_{Dsat}$ is observed for the SiC S/D+ESL device over the SiC S/D device. This brings the total enhancement of the SiC S/D+ESL device over the control to 56%. The $I_{Off}$-$I_{On}$ plot shown in Figure 2-22 shows statistical data of the $I_{Dsat}$ enhancement, and confirms the enhancement figure that was obtained by examining single pairs of matched devices. The enhancement obtained with combining both stressors is larger than that reported in previous work on FinFETs employing SiN stressors alone [2.12]. This observation points towards the effectiveness of combining SiC S/D stressors with a high stress SiN ESL for synergistic performance enhancement. Besides acting as S/D stressors, raised SiC S/D regions also serve to reduce the parasitic S/D resistances of SOI FinFET devices, not unlike raised Si S/D regions, as reported in [2.13]. Ref [2.13] reported the reduction in the series resistances and the drive currents of FinFET devices when Si was epitaxially grown in the S/D regions. The epitaxially grown Si effectively "raises" the S/D regions and results in a larger cross-sectional area for current conduction. Hence, a similar effect is expected for the raised SiC S/D regions.

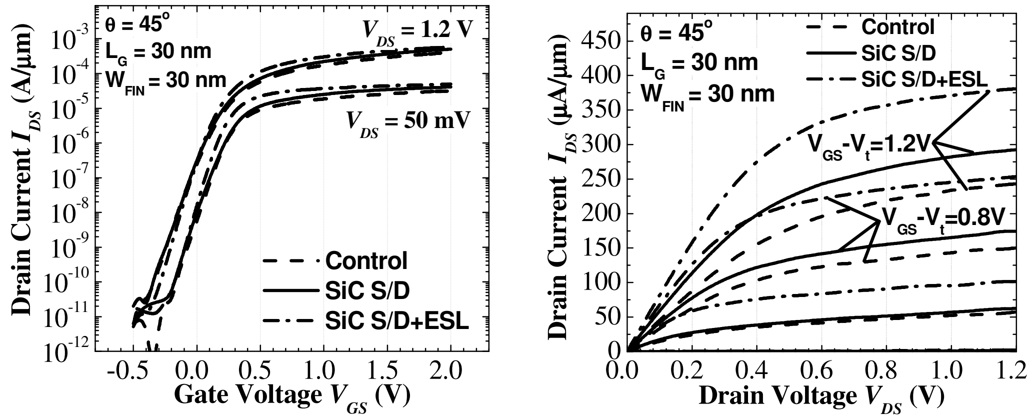



Figure 2-21 From the $I_D$-$V_G$ transfer characteristics, it is clear that the SiC S/D+ESL device does not show any sign of short channel degradation as a result of the added thermal budget experienced during the LPCVD SiN liner deposition. The $I_D$-$V_D$ curves for the same devices show 20% enhancement of the SiC S/D device over the control. A 30% further enhancement in $I_{Dsat}$ is observed for the SiC S/D+ESL device over the SiC S/D device.

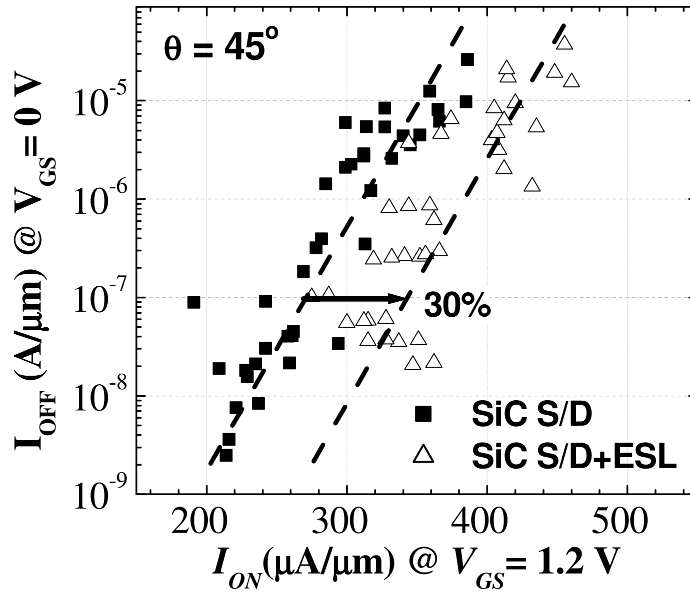



Figure 2-22 $I_{On}$-$I_{Off}$ plot statistically confirms the additional 30% enhancement in $I_{Dsat}$ that was gained by co-integrating a high-stress SiN ESL with SiC S/D devices.

#### *2.3.3.2 <110>-oriented devices (0°)*

In section 2.2.3.3, it was shown that SiC S/D stressors only result in about 7% $I_{Dsat}$ enhancement when integrated with <110>-oriented devices. This was attributed to the reduced sensitivity of the (110)-sidewall channels to longitudinal tensile strain in the <110> direction. In this section, the effects of combining SiC S/D stressors with a high-stress SiN ESL stressor are evaluated. The $I_{Off}$-$I_{On}$ plot shown in Figure 2-23 indicates that a significant 50% $I_{Dsat}$ enhancement can be obtained by co-integrating SiC S/D stressors with a high stress SiN ESL. Figure 2-24 shows the subthreshold characteristics of FinFETs with Si S/D, SiC S/D, and SiC S/D and ESL, showing similar values of DIBL and subthreshold slope. The fin sidewall surface is a (110) surface. $I_{DS}$ is plotted against $V_{GS}$ - $V_{th}$ for clearer illustration, where $V_{th}$ = $V_{GS}$ @ $I_{DS}$ = 100 nA/μm, when $V_{DS}$ = 1.0 V. The values of $V_{th}$ are 84, 40 and 2 mV for "Si S/D", "SiC S/D" and "SiC S/D + ESL" respectively. The threshold voltage lowering in "SiC S/D" and "SiC S/D + ESL" is attributed to strain-induced conduction band lowering**.** The inset shows total resistance ($R_{Tot}$ = 50 mV / $I_{D,lin}$) plotted against gate voltage. A simplified linear region drain current equation that includes a source/drain series resistance parameter was used to generate curves which fit each set of measured data points. The series resistances were estimated to be 594, 614 and 595 Ωμm for "Si S/D", "SiC S/D" and "SiC S/D + ESL" respectively. The comparable series resistances ensure a fair comparison between the three devices. Figure 2-25 shows that a further 29 % enhancement in $I_{Dsat}$ was obtained by adding a tensile SiN ESL for this particular device.

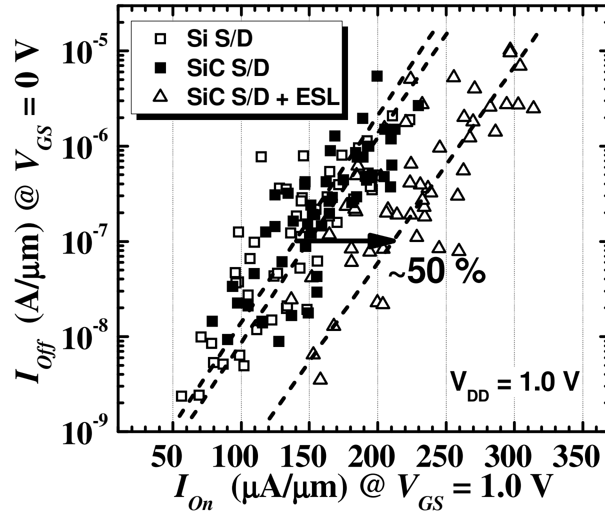



Figure 2-23 $I_{Off}$-$I_{On}$ characteristics of FinFETs with Si S/D, SiC S/D, and SiC S/D and ESL. For <110>-oriented (110)-sidewall FinFETs, incorporating $Si_{1-y}C_y$ S/D stressors alone results in modest performance enhancement. However, further addition of a tensile SiN ESL results in significant performance enhancement of about 50%.

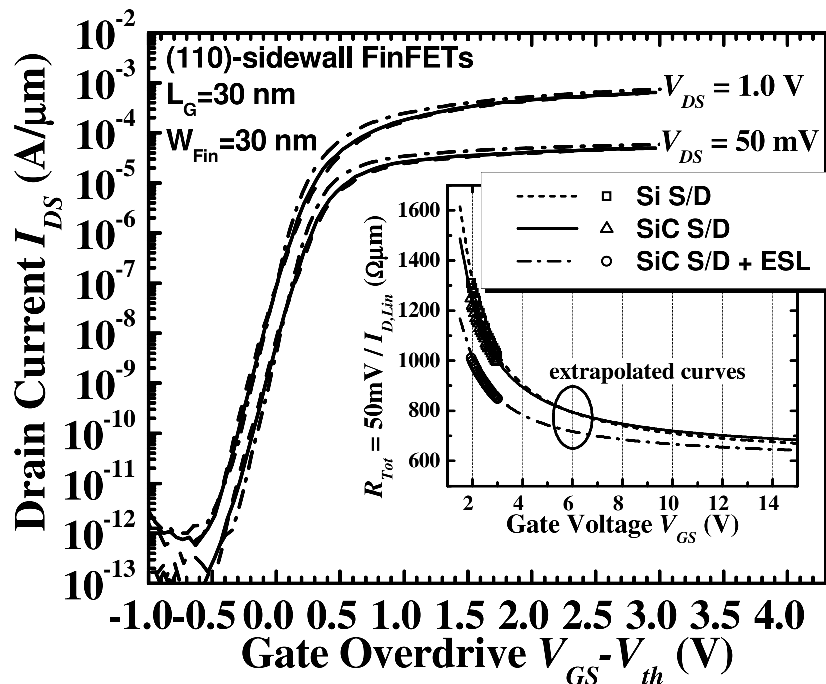



Figure 2-24 Subthreshold characteristics of FinFETs with Si S/D, SiC S/D, and SiC S/D and ESL, showing similar values of DIBL and subthreshold slope. The inset shows total resistance ($R_{Tot}$ = 50 mV / $I_{D,lin}$) plotted against gate voltage. A simplified linear region drain current equation that includes a source/drain series resistance parameter was used to generate curves which fit each set of measured data points.

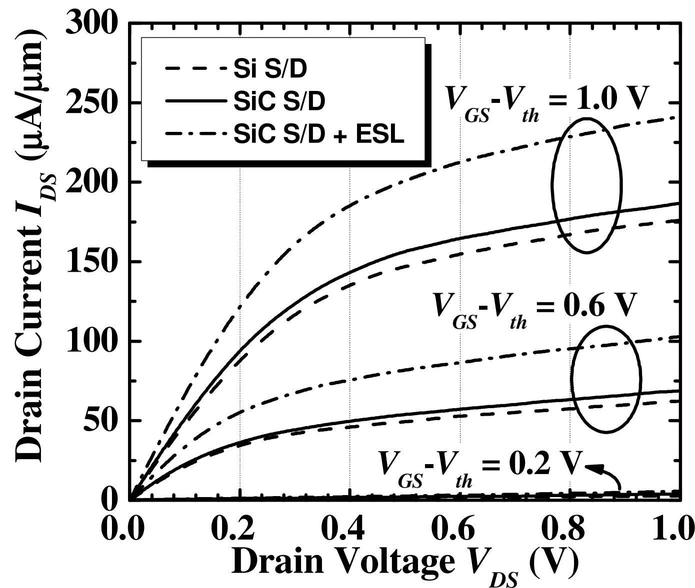



Figure 2-25 $I_{DS}$-$V_{DS}$ characteristics of the FinFETs at various gate over-drives, $V_{GS}$-$V_{th}$. $I_{Dsat}$ enhancement of about 6 % was obtained by incorporating $Si_{1-y}C_y$ S/D stressors alone, while a further 29 % enhancement can be obtained by adding a tensile SiN ESL, bringing the total enhancement to ~37%. $V_{th}$ is defined as $V_{GS}$ when $I_{DS}$ = 100 nA/µm and $V_{DS}$ = 1.0V.

The large enhancement in $I_{Dsat}$ with the addition of a SiN ESL stressor is best explained with the help of Figure 2-26. The differences in the splits are elucidated. A 3-D schematic of the fin is also shown for the "SiC S/D + ESL" split, in which the stress components acting on the (110) sidewall channel surface are also indicated. Since the <110>-oriented FinFETs are not sensitive to longitudinal strain, as shown earlier in section 2.2.3.3, it is unlikely that the added longitudinal stress from the SiN ESL stressor would have this much of an impact on the drive current performance. For the (110)/<110> sidewall channel surfaces, it has been reported that both longitudinal tensile stress and vertical compressive stress result in electron mobility enhancement, with vertical compressive stress having a greater effect in the lower stress regime [2.14]. As such, it is reasonable to believe that vertical compressive

stress plays a major role in the mobility enhancement of the (110)/<110> sidewall channel surfaces.

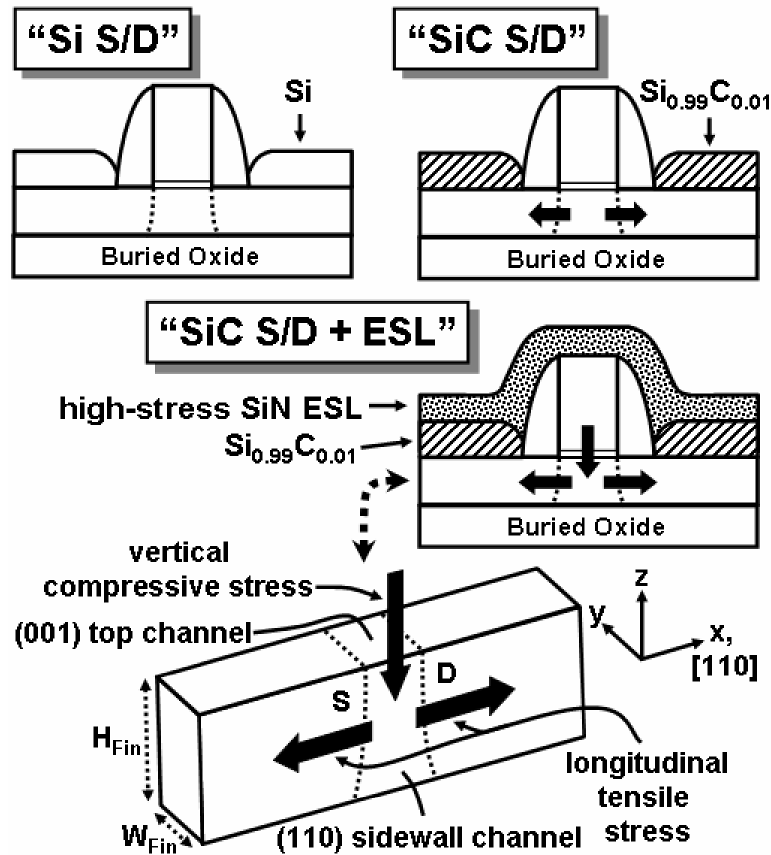



Figure 2-26 Schematic showing the three experiment splits or device structures comprising "Si S/D", "SiC S/D" and "SiC S/D + ESL". In the "Si S/D" control split, the devices have raised Si S/D regions. In both the "SiC S/D" and "SiC S/D + ESL" splits, the devices have raised $Si_{1-y}C_y$ S/D regions. In the "SiC S/D + ESL" split, an additional tensile SiN ESL was deposited. A 3-D schematic of the fin is also shown for the "SiC S/D + ESL" split, in which the stress components acting on the (110) sidewall channel surface are also indicated.

### *2.3.3.3 Summary*

Table 2-1 Effect of SiC S/D and SiC S/D+ESL stressors on FinFET Performance

| | **(100)-sidewall FinFETs** | | | **(110)-sidewall FinFETs** | | |
|---|---|---|---|---|---|---|
| **Device Structure** | ***Si S/D*** | ***SiC S/D*** | ***SiC S/D +ESL*** | ***Si S/D*** | ***SiC S/D*** | ***SiC S/D +ESL*** |
| **$I_{On}$ @ $I_{off}$ = 1 x $10^{-7}$ A, $V_{DD}$ = 1.0 V (µA/µm)** | **167** | **200** | **261** | **140** | **149** | **211** |
| **$\Delta I_{On} / I_{On,\ Si\ S/D}$ (%)** | **0** | **20** | **56** | **0** | **6** | **51** |

The performance benefits of SiC S/D and SiC S/D co-integrated with ESL stressors is summarized in Table 2-1. It is clear that (100)-sidewall FinFETs with combined SiC S/D and ESL stressors exhibit the best overall $I_{on}$ performance. For (110)-sidewall FinFETs, integration with combined SiC S/D and ESL stressors leads to 51 % $I_{On}$ enhancement, which makes their absolute $I_{on}$ performance superior to that of unstrained Si S/D as well as strained SiC S/D (100)-sidewall counterparts. SiC S/D and ESL stressors can thus be an extremely attractive option for enhancing <110>-oriented FinFETs, which may be preferred in density-critical applications.

## 2.4 Carrier Backscattering Characterization

### 2.4.1 Backscattering Theory

In nanoscale transistors, carrier scattering theory has been proposed [2.15]. As illustrated in Figure 2-27, a fraction of the injected carriers near the source end of the channel regions are backscattered from the channel region back into the source. This is assumed to occur within a $k_BT$ layer, which has a potential drop of $k_BT/q$. The thickness of this layer is defined as $l_0$. Hence, the drive current in the transistor is essentially determined by the carrier backscattering ratio $r_{sat}$ and the injection velocity $v_{inj}$ at the top of the source-channel barrier.

Using a temperature dependent carrier backscattering model [2.16],[2.17], it is possible to extract the values of $v_{inj}$ and $r_{sat}$ in nanoscale transistors. This can help us to understand the carrier transport properties in strained-channel transistors, such as FinFETs with SiC S/D regions.

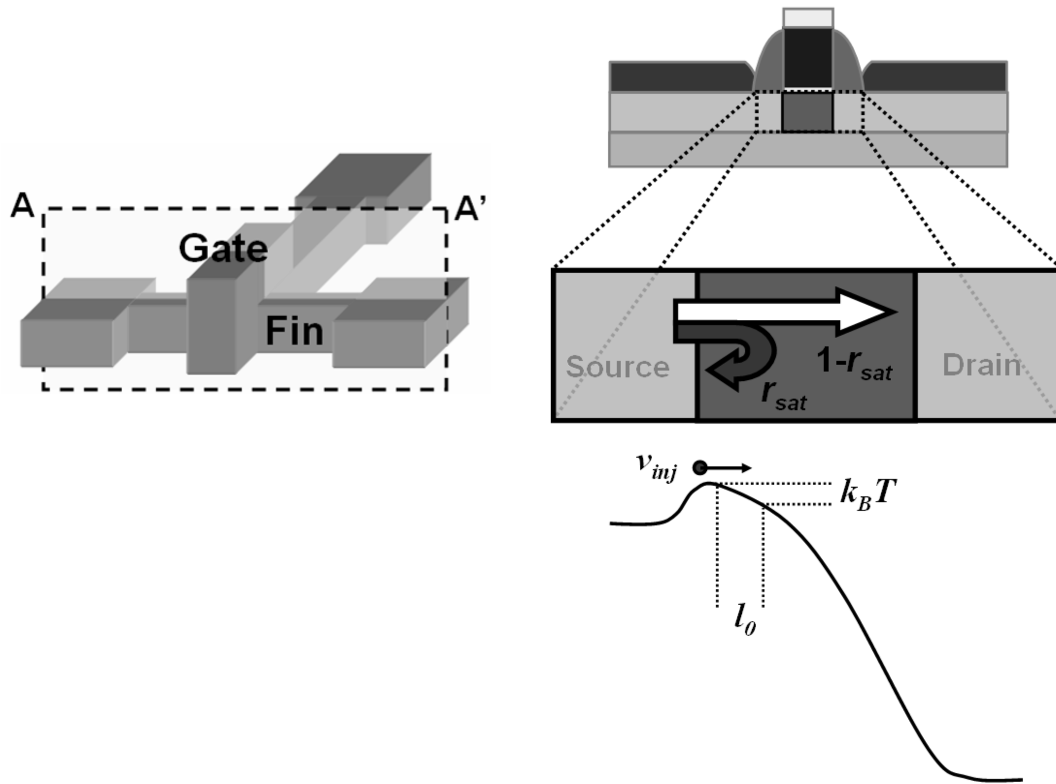



Figure 2-27 Schematic representation of an n-channel transistor showing the conduction band profile across the channel from source to drain. $r_{sat}$ represents the fraction of electrons that are backscattered from the channel to the source size. The electrons are injected in the channel with an injection velocity $v_{inj}$.

The drive current in the saturation regime $I_{Dsat}$ can be expressed as follows:

$$I_{Dsat} = W\upsilon_{inj}\left(\frac{1-r_{sat}}{1+r_{sat}}\right)C_{eff}\left(V_G - V_{th,\,sat}\right) \qquad \text{(Equation 2-1)}$$

To extract the value of $r_{sat}$ in nanoscale transistors, the following analytic expressions can be used:

$$\begin{aligned}\frac{dI_{Dsat}}{dT} &= I_{Dsat}\left[\frac{1}{\upsilon_{inj}}\frac{d\upsilon_{inj}}{dT} + \frac{1+r_{sat}}{1-r_{sat}}\frac{d}{dT}\left(\frac{1-r_{sat}}{1+r_{sat}}\right) + \frac{1}{V_G - V_{th,\,sat}}\frac{d\left(V_G - V_{th,\,sat}\right)}{dT}\right] \\ &= I_{Dsat}\left[\frac{1}{2T} - \left(\frac{1}{1+r_{sat}} + \frac{1}{1-r_{sat}}\right)\frac{dr_{sat}}{dT} - \frac{\eta}{V_G - V_{th,\,sat}}\right] \\ &= I_{Dsat}\alpha \qquad \text{(Equation 2-2)}\end{aligned}$$

where $\alpha = \frac{I_{Dsat1} - I_{Dsat2}}{I_{Dsat2}(T_1 - T_2)}$ and $\eta = \frac{V_{th,sat1} - V_{th,sat2}}{T_1 - T_2}$ are the temperature coefficients of $I_{Dsat}$ and $V_{th,sat}$ respectively.

This allows α to be expressed as follows, which allows $\frac{\lambda_0}{l_0}$ to be extracted:

$$\alpha = \frac{1}{T}\left(\frac{1}{2} - \frac{4}{2 + \frac{\lambda_0}{l_0}}\right) - \frac{\eta}{V_G - V_{th,sat}} \qquad \text{(Equation 2-3)}$$

Finally, we can obtain the values of the backscattering ratio $r_{sat}$ and ballistic efficiency $B_{sat}$ using the following expressions:

$$r_{sat} = \frac{1}{1 + \frac{\lambda_0}{l_0}} \qquad \text{(Equation 2-4)}$$

$$B_{sat} = \frac{1 - r_{sat}}{1 + r_{sat}} \qquad \text{(Equation 2-5)}$$

### 2.4.2 Device Backscattering Characterization

Both <100> and <110> oriented FinFET devices with SiC S/D stressors, together with their respective Si S/D control devices were characterized by making IV measurements throughout a range of temperatures, similar to that performed in [2.16]. Backscattering parameters were then extracted using the analytic expressions described in Section 2.4.1. Figure 2-28 shows the values of $r_{sat}$ that were extracted. The incorporation of SiC S/D regions to apply uniaxial tensile strain to the channel resulted in the reduction of $r_{sat}$ for both device channel orientations. <100>-oriented devices had a slightly larger reduction in $r_{sat}$ compared to <110>-oriented devices, which is consistent with the increased sensitivity of the (100)/<100> sidewall channel surface to longitudinal tensile strain. However, the slight differences in $r_{sat}$ reduction

cannot account completely for the large differences observed in the $I_{Dsat}$ enhancement of the respective devices. Figure 2-29 shows the ballistic efficiency of the devices. It is observed that with SiC S/D stressors, <100>-oriented FinFETs have reached a ballistic efficiency of >52%. Figure 2-30 shows the enhancement in injection velocity $v_{inj}$ for the devices. The enhancement in $v_{inj}$ for <100>-oriented devices is ~26% while that for <110>-oriented devices is about ~13%. It is hence possible that the large discrepancy in $I_{Dsat}$ enhancement for <100> and <110>-oriented devices is related to the difference in $v_{inj}$ enhancement. This also agrees well with reported results on uniaxially strained n-channel planar devices in [2.17]-[2.20]. Figure 2-31 plots the extracted mobility enhancement against $I_{Dsat}$ enhancement for <100> and <110> FinFET devices. It confirms our understanding of the observed effects of strain on carrier mobility and $I_{Dsat}$ enhancement in differently oriented FinFET devices. Significant $I_{Dsat}$ enhancement observed in strained n-channel FinFETs is attributed to the large gain in electron mobility, which is approximately 2 times the $I_{Dsat}$ enhancement. $I_{Dsat}$ enhancement for [010]-oriented FinFETs is higher than that for [110]-oriented FinFETs, as can be expected by examining the piezoresistance coefficients of the channel surfaces [2.5],[2.6].

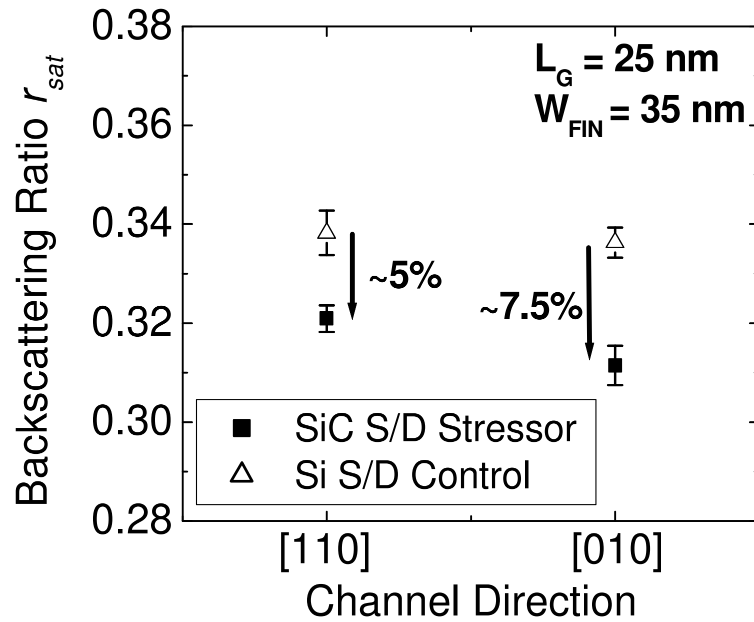



Figure 2-28 SiC S/D FinFETs show improvement (reduction) in backscattering ratio $r_{sat}$ over control Si S/D FinFETs. This could possibly be due to a reduced critical length for backscattering $\ell_o$ as a result of conduction band barrier modulation.

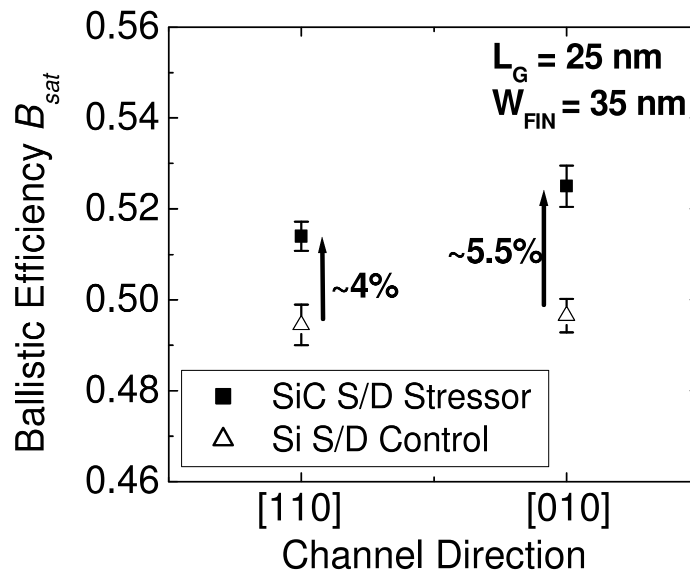



Figure 2-29 SiC S/D FinFETs show improvement (increase) in ballistic efficency $B_{sat}$ over control Si S/D FinFETs. It is observed that the dependence of $\Delta B_{sat}$ on channel direction is not very prominent.

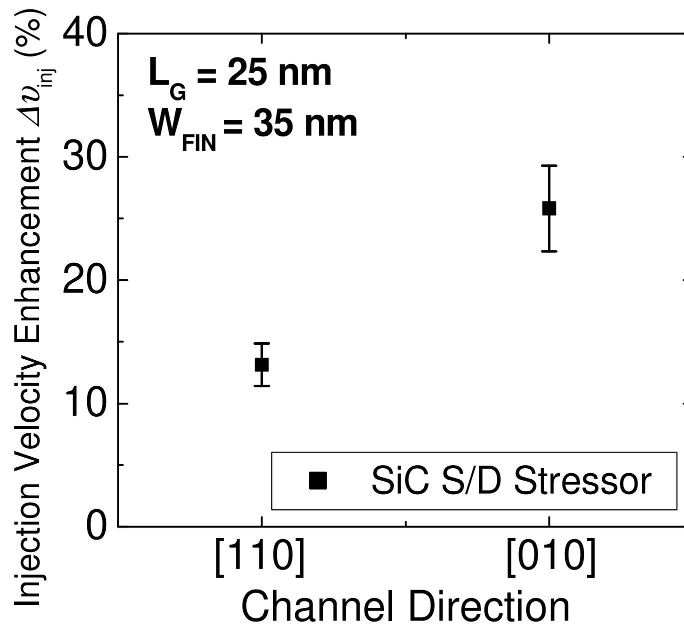



Figure 2-30 Injection velocity $v_{inj}$ enhancement in the strained SiC S/D FinFETs is higher for [010] channel direction than for the [110] channel direction.

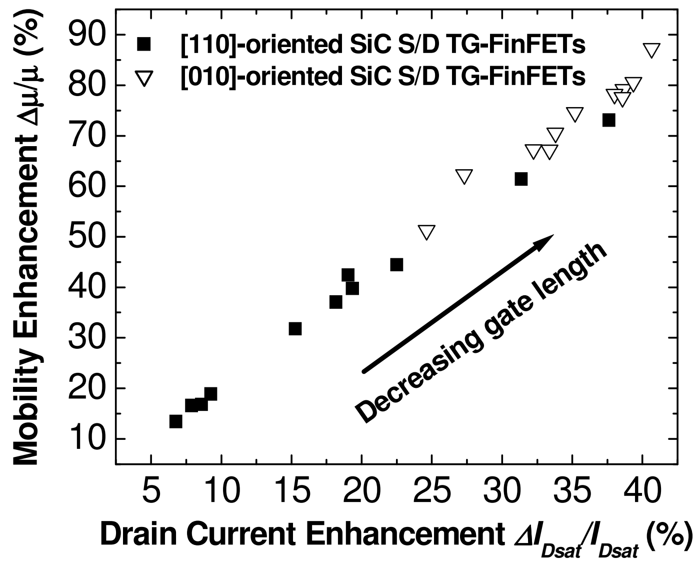



Figure 2-31 Significant $I_{Dsat}$ enhancement observed in strained n-channel FinFETs is attributed to the large gain in electron mobility. The mobility enhancement is approximately 2 times the $I_{Dsat}$ enhancement. $I_{Dsat}$ enhancement for [010]-oriented FinFETs is higher than that for [110]-oriented FinFETs, as can be expected by examining the piezoresistance coefficients of the channel surfaces.

## 2.5 Geometrical Approaches to Further Stress Enhancement

### 2.5.1 Introduction

In this section, the effect of geometric parameters such as the SiC S/D stressor thicknesses and the effect of increasing the stressor-to-channel proximity (by reducing spacer width) are briefly evaluated. The experiments confirm that higher strain induced enhancement can be obtained with such geometric changes.

### 2.5.2 Effect of Increasing Stressor Thickness

When SiC S/D stressors are grown in the S/D regions of FinFETs, it is expected that SiC S/D stressors will attempt to compressively strain the underlying Si S/D regions, which will in turn apply longitudinal tensile strain to the channel due to shape-anisotropic contraction. However, it should be noted that the SiC film itself will come under tensile strain. This enlarges its lattice constant and reduces the amount of strain that is transferred. The amount of strain energy in a S/D stressor film depends on thickness. Hence, it is believed that scaling up the thickness of the SiC S/D stressor will result in greater channel strain for higher performance enhancement.

To evaluate, two SiC stressor thicknesses were grown on different device splits. Devices denoted as "Thin" and "Thick" have SiC S/D stressor thicknesses of 30 nm and 45 nm respectively. These are tri-gate devices with <100>-oriented channels for maximum sensitivity to longitudinal strain from the SiC S/D stressors. Figure 2-32 shows a SEM image of a FinFET device with thick SiC S/D stressors of 45 nm. Excellent selectivity to the surrounding isolation $SiO_2$ and the SiN gate spacers was

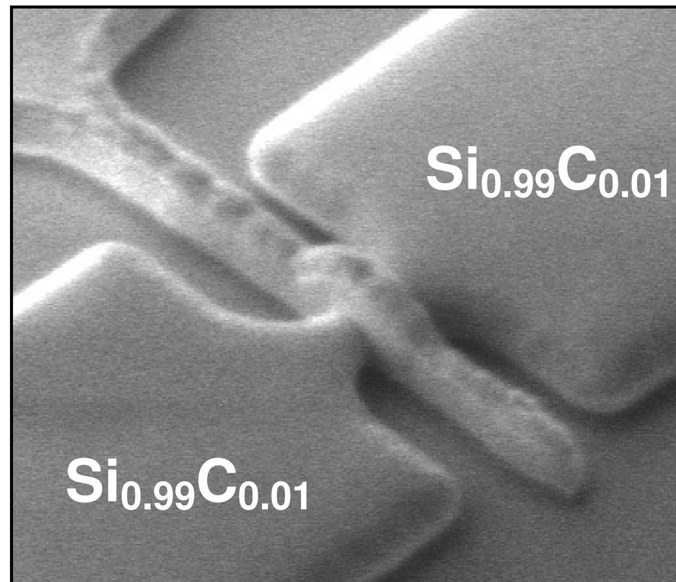



Figure 2-32 SEM image showing thick $Si_{0.99}C_{0.01}$ S/D stressors of 45 nm grown selectively in the S/D regions of a FinFET device.

still achieved. It should be noted that selectivity can be lost if the SiC film thickness is too large. In dense layouts, excessive S/D overgrowth can also result in shorts to neighbouring active regions.

Due to the spread in $I_{Off}$-$I_{On}$ data points, it is difficult to extract small enhancement figures. Instead, devices with closely matched gate lengths and subthreshold characteristics are examined. Figure 2-33 shows the $I_D$-$V_G$ characteristics of a pair of devices, one with a 30 nm thick SiC S/D stressor, and the other with a 45 nm thick SiC S/D stressor. The process flow used to fabricate these devices is identical to that used to fabricate devices in section 2.2.3. It can be observed that both devices have comparable subthreshold swing and DIBL. The S/D series resistances were also estimated to be quite similar, which suggests that a raised SiC S/D of 30 nm is already sufficient to reduce the sheet resistance component to an acceptable value,

such that other resistance components such as extension resistance and spreading resistance dominate. Figure 2-34 shows the $I_D$-$V_D$ characteristics for the same pair of devices. A further 9% enhancement in $I_{Dsat}$ was obtained by scaling up the SiC thickness from 30 nm to 45 nm.

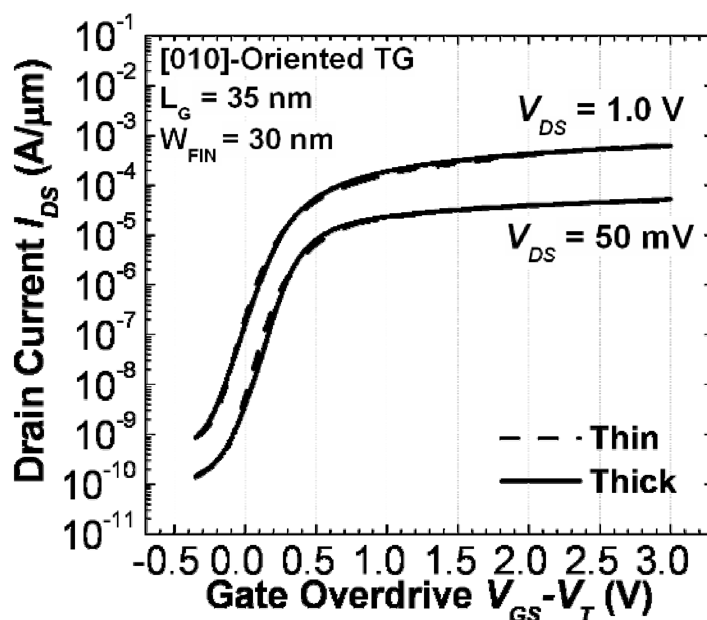



Figure 2-33 Subthreshold characteristics of a matched pair of TG FinFETs of 2 SiC S/D stressor thicknesses having similar DIBL and subthreshold swing. The estimated series resistances are also very similar.

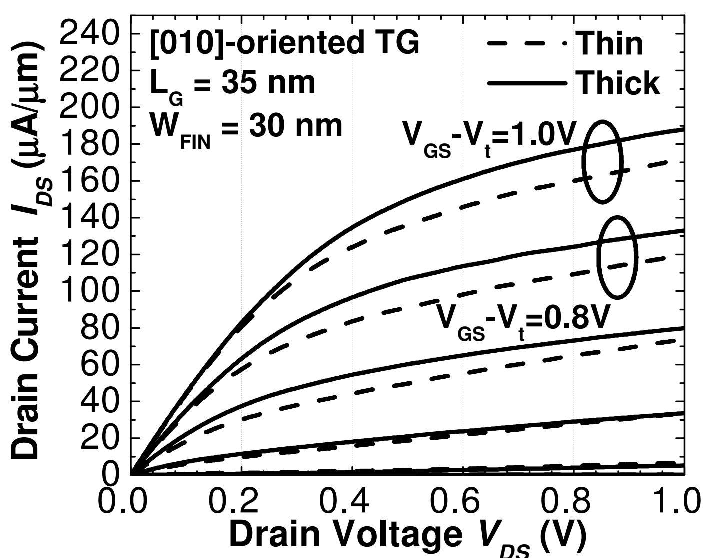



Figure 2-34 $I_{DS}$-$V_{DS}$ characteristics of the same matched pair of devices show ~9% $I_{Dsat}$ enhancement of "Thick" SiC S/D FinFETs over "Thin" SiC S/D FinFETs.

### 2.5.3 Effect of Increasing Stressor-to-channel Proximity

Increasing the proximity of the SiC S/D stressor to the channel regions can help to increase the channel strain. This can be accomplished by scaling down the spacer widths. In this set of experiments, the spacer width was scaled down from 40 nm to 25 nm in double-gate FinFETs. “Spacer 1” devices have spacer widths of 40 nm while “Spacer 2” devices have spacer widths of 25nm. As these are double-gate devices, the additional difference between these devices and the tri-gate devices in Sections 2.2.1 and 2.5.2 are that a 10 nm $SiO_2$ fin hardmask was left on top of the fin prior to gate oxide formation. This resulted in the formation of double-gate devices, which aids in the analysis of strain effects due to the pronounced strain sensitivity differences between the (110)/<110> and (100)/<100> channel surfaces.

Figure 2-35 shows the cross-section TEM image of a device with 25 nm spacers and $Si_{0.99}C_{0.01}$ stressor thickness of 45 nm. Figure 2-36(a) shows the subthreshold characteristics for a pair of [010]-oriented DG FinFETs with 2 spacer widths and similarly thick stressors. DIBL and subthreshold swing in these devices are comparable. Figure 2-36 (b) shows an $I_{Dsat}$ enhancement of ~20%, of which part of it must be attributed to reduction in source/drain series resistance.

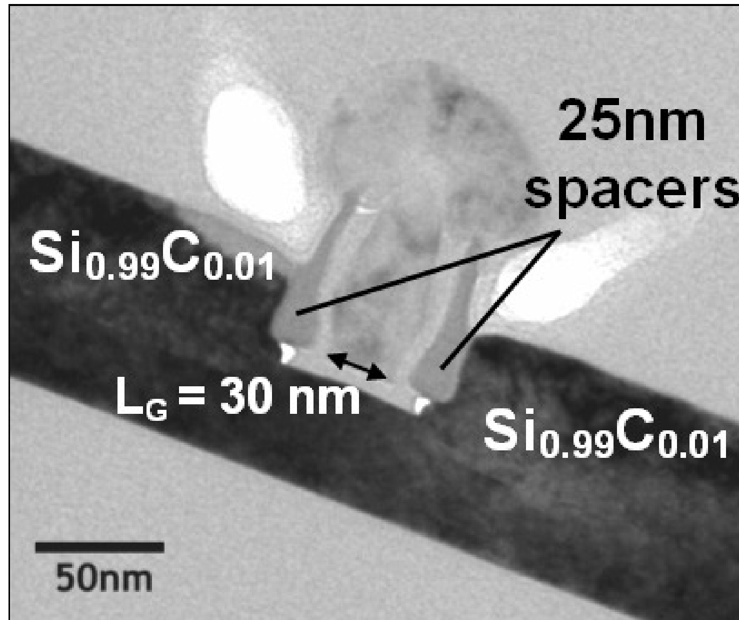
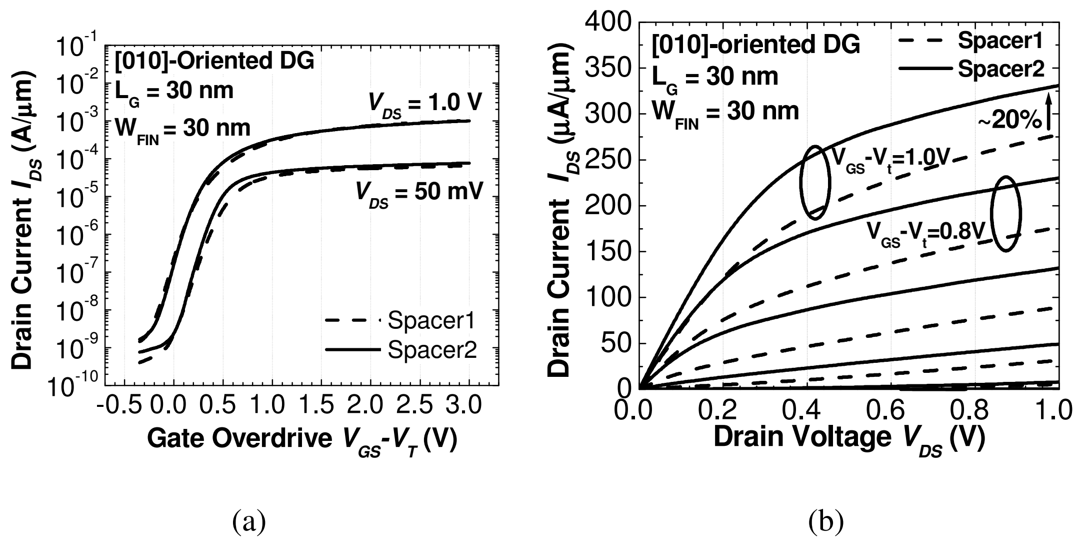



Figure 2-35 Cross-section TEM of a "Spacer-2" device with 30 nm gate length, 25 nm spacer width and 45 nm $Si_{0.99}C_{0.01}$ stressors. "Spacer-1" device (not shown here) has a 40 nm spacer. The narrower spacer width in a "Spacer-2" device allows closer proximity between the $Si_{0.99}C_{0.01}$ S/D stressors and the channel. An oxide hardmask of ~10 nm $SiO_2$ on top of the fin allows the devices to function as DG FinFETs.




(a) (b)

Figure 2-36 (a) Subthreshold characteristics of a pair of DG FinFETs with similar DIBL and subthreshold swing. "Spacer1" and "Spacer2" have spacer widths of ~40 nm and ~25 nm respectively. (b) $I_{DS}$-$V_{DS}$ characteristics of the same pair of devices show ~20% $I_{Dsat}$ enhancement of "Spacer-2" SiC S/D FinFETs over "Spacer-1" SiC S/D FinFETs. A small fraction of this enhancement is attributed to series resistance reduction.

Since the reduction in spacer width also reduces the S/D extension resistance, the degree of the contribution of S/D series resistance enhancement to $I_{Dsat}$ enhancement must be ascertained. Figure 2-37 shows the plot of total resistance $R_{Tot}$ against gate over drive. Due to the asymptotic behavior of the curve, $R_{Tot}$ approximates the value of S/D series resistance at high gate overdrive voltages. It is therefore estimated that reduction in spacer width results in a 14% series resistance enhancement.

To decouple the strain effects from the series resistance effects, $I_{Dsat}$ and series resistance values of devices with 2 channel directions (<110> and <100> directions) are examined, as shown in Figure 2-38. The reduction in series resistance for devices of both channel directions is comparable, which implies approximately similar contributions to $I_{Dsat}$ enhancement from series resistance reduction for both channel directions. Average $I_{Dsat}$ enhancement is much higher for [010]-oriented devices than for [110]-oriented devices. The ratio of $I_{Dsat}$ enhancements obtained for the two differently oriented devices agrees well with the ratio of their piezoresistance coefficients [2.5], [2.6]. Hence, increased strain effects from closer proximity between the $Si_{0.99}C_{0.01}$ S/D stressors and the channel account for a large fraction of the $I_{Dsat}$ enhancement.

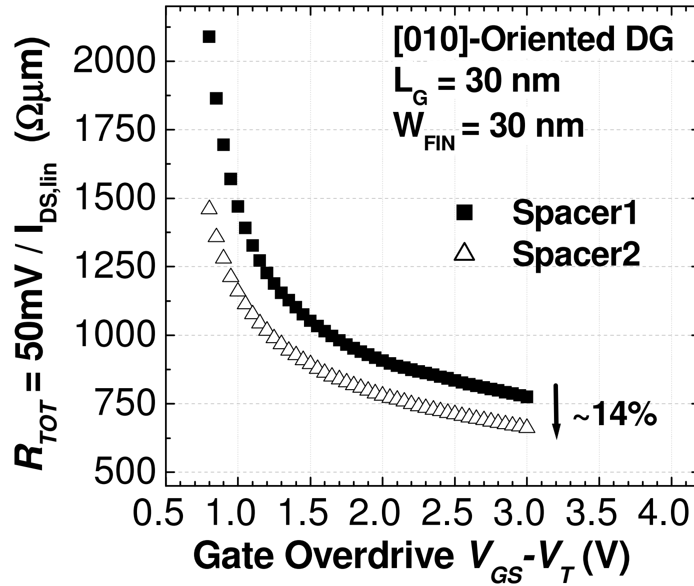



Figure 2-37 Series resistance extraction by examining the asymptotic behaviour of total resistance at large gate bias estimates 14% reduction in series resistance for this pair of devices.

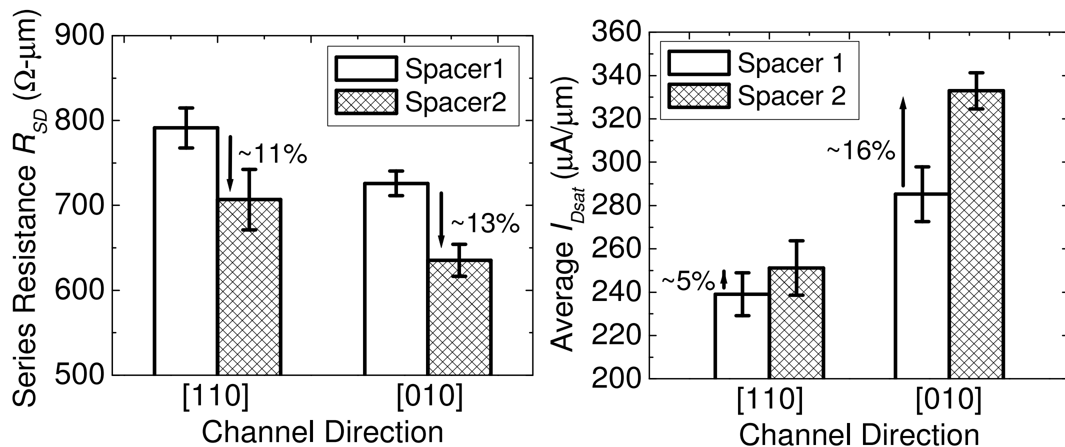



Figure 2-38 (a) Average estimated series resistances are shown for the 2 channel directions. The reduction in series resistances for both channel directions is comparable. This suggests similar contributions to $I_{Dsat}$ enhancement from series resistance reduction for both channel directions. (b) Average $I_{Dsat}$ enhancement is much higher for [010]-oriented devices than for [110]-oriented devices. Hence, increased strain effects from closer proximity between the $Si_{0.99}C_{0.01}$ S/D stressors and the channel accounts for a large fraction of the $I_{Dsat}$ enhancement.

The matched pairs of devices were further characterized using measurements performed at various temperatures to extract the carrier backscattering parameters

using the temperature dependent carrier backscattering model as described in Section 2.4.1. Both $B_{sat}$ and $r_{sat}$ are degraded when spacer width is scaled down from 40 nm to 25 nm. This can possibly be related to carbon diffusion to the channel regions, which results in an increase in impurity scattering. This implies that device designers should exercise caution with the scaling down of spacer widths for SiC S/D devices. There may be an optimum point, beyond which there may be compromises. However, $v_{inj}$ is simultaneously enhanced by almost 40%. Coupled with the earlier observation of only 14% reduction in series resistance, it is thus concluded that the overall $I_{Dsat}$ enhancement of the "Spacer-2" device over the "Spacer-1" device is likely to come primarily from enhancement in injection velocity, as a result of the increase in longitudinal tensile strain in the channel.

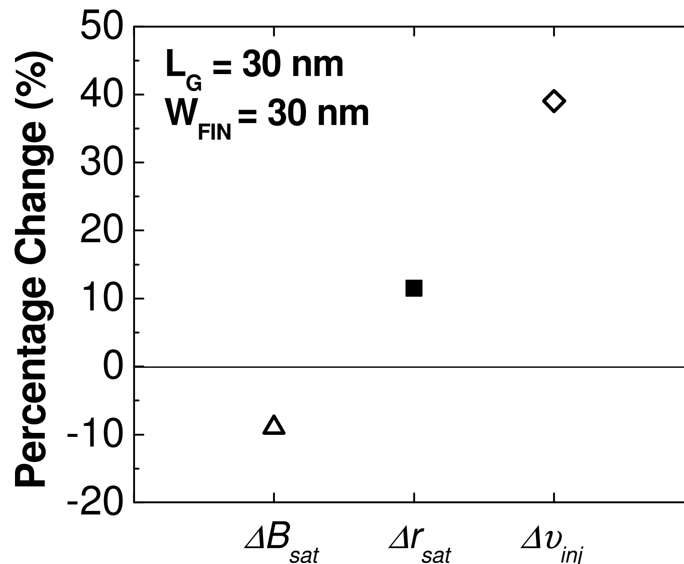



Figure 2-39 Both $B_{sat}$ and $r_{sat}$ of the "Spacer-2" device are degraded over that of "Spacer-1". However, $v_{inj}$ is significantly enhanced by almost 40%. Hence, the $I_{Dsat}$ enhancement of the "Spacer-2" device over the "Spacer-1" device is likely to come primarily from the injection velocity enhancement.

### 2.5.4 Summary

It has been shown that tuning geometrical parameters such as stressor thicknesses and spacer widths can lead to enhanced strain effects in FinFETs with SiC S/D stressors. Hence, it should be noted that device structural parameters become especially important in strained multiple-gate transistors. With closer proximity from the S/D stressors to the channel, the variation in process control will result in greater device performance fluctuation, resulting in a tighter process margin. It can be inferred that good control of variability in structural parameters will reduce the variability in channel stress and hence, device drive current performance.

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# Chapter 3

# 3. Novel Techniques for Further Improving N-Channel Multiple-Gate FETs with Silicon Carbon ($Si_{1-y}C_y$) Source and Drain Technology

## 3.1 Introduction

In this chapter, techniques for further improving the performance of n-channel multiple-gate transistors with SiC S/D stressors are proposed and experimentally investigated. Section 3.2 describes a spacer removal technique for extending the influence of the S/D stressors without physically bringing them closer to the channel. Section 3.3 describes a high-stress contact silicide which can have synergistic stress contributions with the SiC S/D stressors. Section 3.4 describes how carbon substitutionality in SiC S/D stressors can be further scaled with in-situ doped epitaxial films.

## 3.2 Spacer Removal Technique for Further Strain Enhancement

### 3.2.1 Introduction

Employing selectively grown lattice-mismatched source and drain (S/D) stressors such as $Si_{1-y}C_y$ S/D stressors shows great feasibility due to the ease of integration and large performance enhancement. It is also important to note that the effectiveness of such local strain technology will be adversely affected when active area dimensions are scaled down in subsequent technology generations [3.1], one reason being the imposition of severe mechanical constraints or physical boundary conditions. To maximize strain-induced performance enhancement, it would be desirable to maximize the stress coupling between the S/D stressor and the channel region. In this section, a novel technique which improves this stress coupling efficiency in strained n-channel tri-gate FinFETs with Silicon-Carbon (SiC or $Si_{1-y}C_y$) S/D stressors by relaxing mechanical boundary constraints via gate spacer removal will be discussed. A schematic representation of the concept of Gate-Spacer-Removed SiC (GSR-SiC) FinFETs is shown in Figure 3-1. This low-cost technique involves the removal of the gate spacers prior to ILD deposition.

It should be emphasized that this concept is different from that of stressor proximity, which involve scaling down or removing the spacers, and subsequently physically placing the stressors closer to the channel [3.2], [3.3]. Moreover, this technique can be applied in conjunction with that described in [3.3] for combined stress effects. In this section, the effectiveness of this simple and low-cost technique is

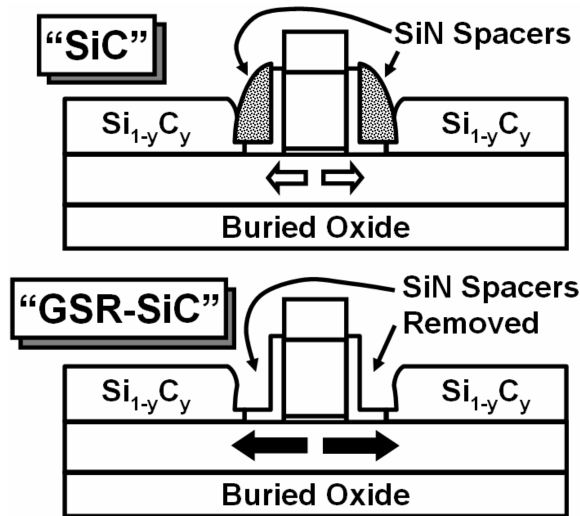



Figure 3-1 Schematic illustrating that the device structure for both "SiC" and "GSR-SiC" FinFETs are exactly the same, except for the removal of the gate spacers in "GSR-SiC" devices just prior to ILD deposition.

demonstrated experimentally, obtaining significant further $I_{Dsat}$ enhancement over already strained n-channel FinFETs with SiC S/D stressors.

### 3.2.2 Device Fabrication

N-channel tri-gate (TG) FinFET devices of various nanoscale gate lengths ($L_G$) and fin widths ($W_{Fin}$) were fabricated on (001) SOI wafers with a Si thickness of ~40 nm. The device fabrication scheme shown in Figure 3-2 is very similar to that described in Section 2.2.1. As described earlier, the spacer formation process involved intentionally removing fin sidewall spacers, while retaining gate spacers, enabling the selective epitaxial growth of Π-shaped SiC S/D stressors that wrap around the top and sidewall fin surfaces for maximum lattice strain coupling.

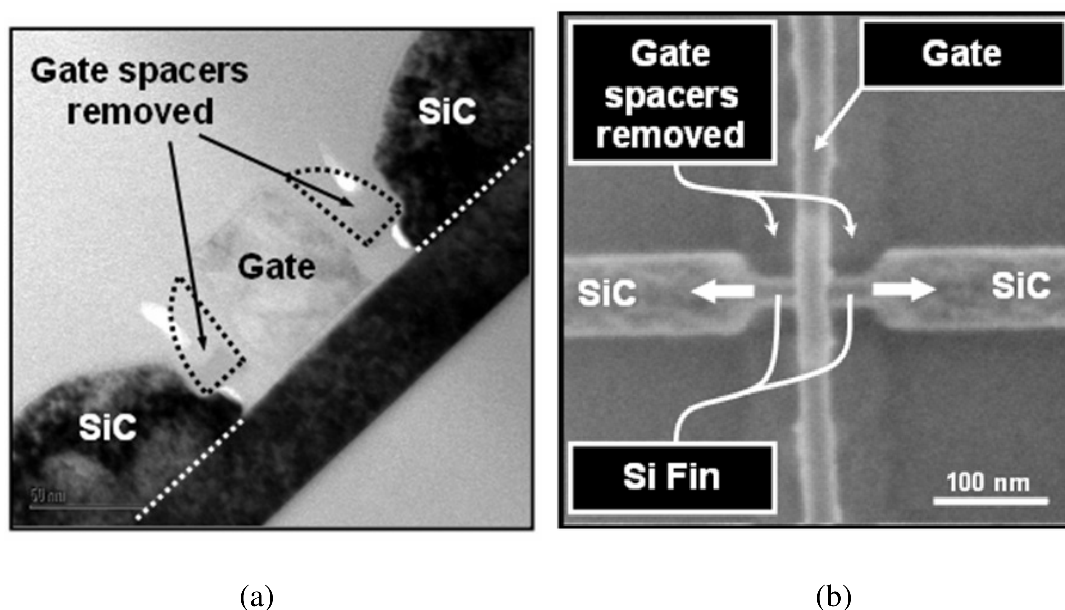
After S/D implant and RTA activation, the redundant SiN gate spacers were removed by selective wet etching for devices on one wafer, so as to improve stress

- Channel implant
- Fin definition
- $SiO_2$ gate oxidation (25 Å)
- Poly-Si gate deposition and Gate implant
- Gate definition
- SDE implant
- Spacer formation (35nm) with stringer removal
- **Selective Epitaxy of $Si_{0.99}C_{0.01}$ for *BOTH* "SiC" and "GSR-SiC" devices**
- S/D implant and RTA activation
- **Gate Spacer Removal for "GSR-SiC" devices**
- PECVD ILD ($SiO_2$) deposition and metallization

Figure 3-2 Process sequence showing key steps employed in FinFET device fabrication. For Gate-Spacer-Removed-SiC or "GSR-SiC" devices, the SiN gate spacers were removed by selective wet etching after S/D implant activation.

transfer from the SiC S/D stressors to the channel. Although salicidation was not performed on these devices, others have successfully demonstrated selective removal of SiN spacers post-salicidation [3.3]. Hence, this technique is also compatible with salicided devices.

A TEM image in Figure 3-3(a) shows the cross-section of a spacerless device after the selective removal of the gate spacers. A top-view SEM image of a spacerless FinFET just after gate spacer removal is shown in Figure 3-3(b). The S/D extension regions that were previously covered by the gate spacers can clearly be seen after the spacer removal process. The impact of spacer removal on the channel stress is that it will cause an imbalance in forces within the strained FinFET device structure, which is essentially a perturbation to its mechanical equilibrium. This necessitates stress changes in various regions of the device structure in order to restore mechanical force equilibrium. By removing the gate spacers, rigid boundary conditions at the SiC S/D stressor edges are removed. As a result of the stress changes to restore mechanical




(a) (b)

Figure 3-3 (a) Cross-section TEM image showing a spacerless device with raised SiC S/D regions. The gate spacers have been selectively etched away after S/D activation. (b) Top-view SEM image of a spacerless FinFET with raised SiC S/D regions. Removing the gate spacers enhances the stress coupling to the channel, resulting in an increase in longitudinal tensile channel stress.

equilibrium, longitudinal tensile stress in the S/D extension regions and the channel increases. This effectively improves the stress coupling efficiency of the S/D stressors to the channel. Longitudinal tensile channel stress is particularly beneficial for enhancing the electron mobility of (100) channel surfaces with a <100> channel direction, based on piezoresistance coefficients [3.4],[3.5]. Hence, an increase in longitudinal tensile channel stress, as a result of the spacer removal process, should improve the performance of n-channel (100)-sidewall tri-gate FinFETs significantly.

### 3.2.3 Device Characterization

The n-channel FinFETs characterized in this section have (100) channel surfaces and <100> channel directions for maximum sensitivity to any channel strain changes induced by the spacer removal process. Due to the fact that both “SiC” and “GSR-SiC” FinFETs are strained devices, it is necessary to maintain similar SiC S/D stressor thicknesses for a fair comparison. With this in mind, FinFET test devices

characterized in this work were designed not to have contact mesas next to the fin, and have a large contact-to-spacer distance of ~0.16 μm [See Figure 3-4]. To minimize variations in SiC S/D stressor thickness consumption, salicidation was deliberately not performed. As expected, the long unsilicided portions of the SiC S/D regions between the contact and the SDE drastically increases parasitic source/drain series resistance $R_{SD}$, which then becomes a reflection of S/D stressor thickness. Hence, devices with matched $R_{SD}$ also have comparable S/D stressor thicknesses.

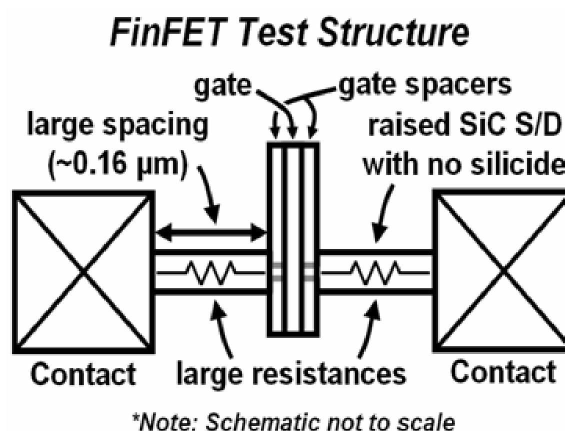



Figure 3-4 Schematic of the FinFET test structure.

The $I_{Off}$-$I_{On}$ plot indicates an enhancement in $I_{On}$ at a given $I_{Off}$, with an increasing $I_{On}$ enhancement at larger values of $I_{Off}$ [See Figure 3-5]. The standard deviations of $I_{On}$ for the devices plotted in the $I_{Off}$-$I_{On}$ plot are 30.6 μA and 30.9 μA, respectively, for SiC and GSR-SiC devices. This indicates that spacer removal does not significantly degrade variability. Figure 3-6 plots $I_{On}$ against *DIBL* for the same sets of devices. Lines are generated by linearly fitting each set of data points using a method of least squares. *DIBL* is correlated with effective channel length, which is related to the physical gate length. DIBL is a short channel effect which worsens

(increases in value) as the effective gate length is scaled down. As such, the plot is a reflection of the $I_{On}$ trend with decreasing gate lengths. The $I_{On}$ enhancement increases with increasing values of *DIBL*. This implies that the extra performance benefit gained from the spacer removal process will become even more significant as physical gate lengths are scaled down.

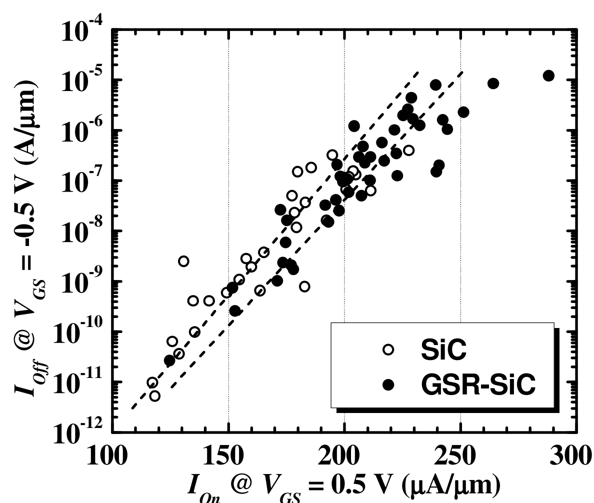



Figure 3-5 $I_{Off}$-$I_{On}$ plot showing enhancement in $I_{On}$ of GSR-SiC devices over conventional SiC devices at a given $I_{Off}$

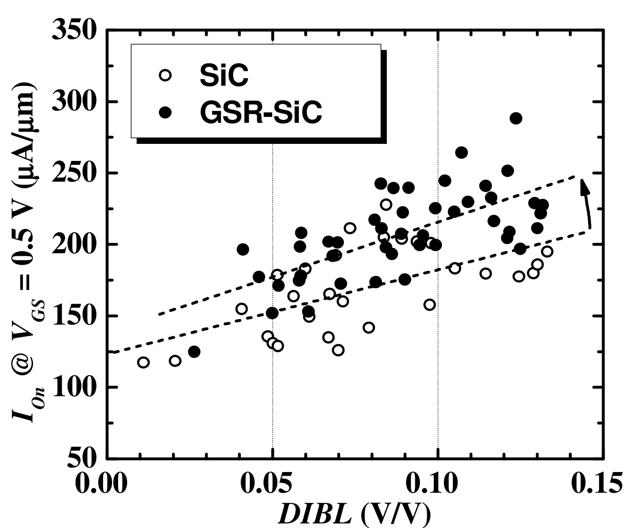



Figure 3-6 $I_{On}$-*DIBL* plot showing improvement in $I_{On}$ at a given value of *DIBL*. It is observed that the enhancement in $I_{On}$ increases with *DIBL*.

Figure 3-7 shows the cumulative probability plots of *DIBL*, *SS* and $V_{t,lin}$, respectively, for the same set of FinFETs shown in the $I_{Off}$-$I_{On}$ plot. Both sets of "SiC" and "GSR-SiC" devices show very comparable *DIBL* and *SS*. Both "SiC" and "GSR-SiC" devices have lower-than-expected threshold voltages due to the use of $n^+$-polysilicon gates. "GSR-SiC" devices have a reduced average $V_{t,lin}$ of about 60 mV compared to "SiC" devices. This threshold voltage lowering can be attributed to greater conduction band lowering in "GSR-SiC" devices as a result of the higher channel strain. Gate spacer removal is a wet chemical process which does not involve any significant thermal budget that can cause any dopant diffusion. The lowering of the conduction band (Δ2 valleys are lowered[3.6]) is due to the increase in conduction band splitting as a result of the enhanced channel strain. Hence, the onset of inversion is reached at a lower voltage since the surface conduction band-bending in the channel arrives at the inversion threshold sooner with applied gate bias.

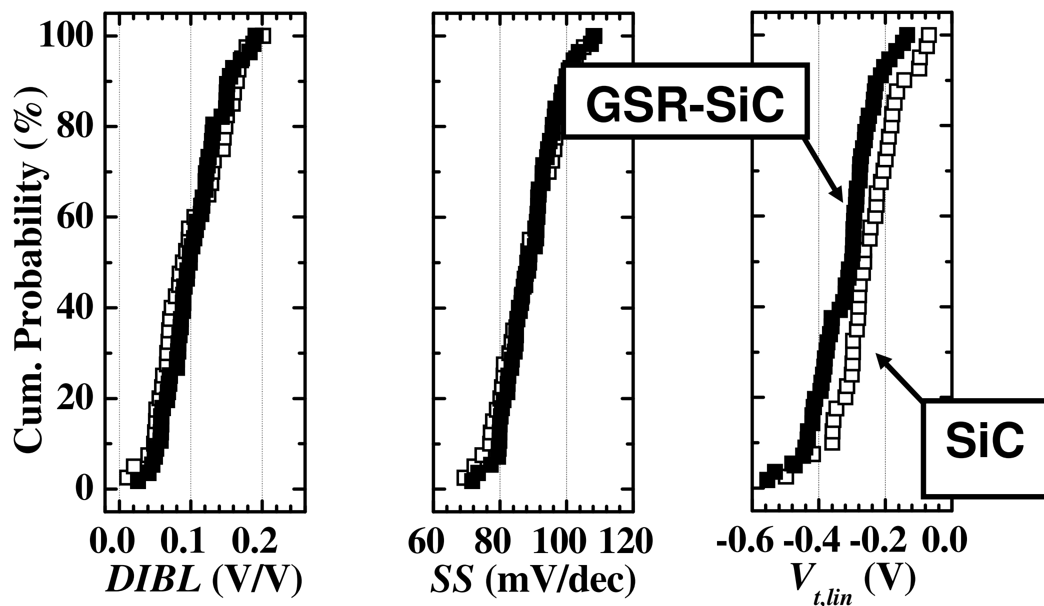
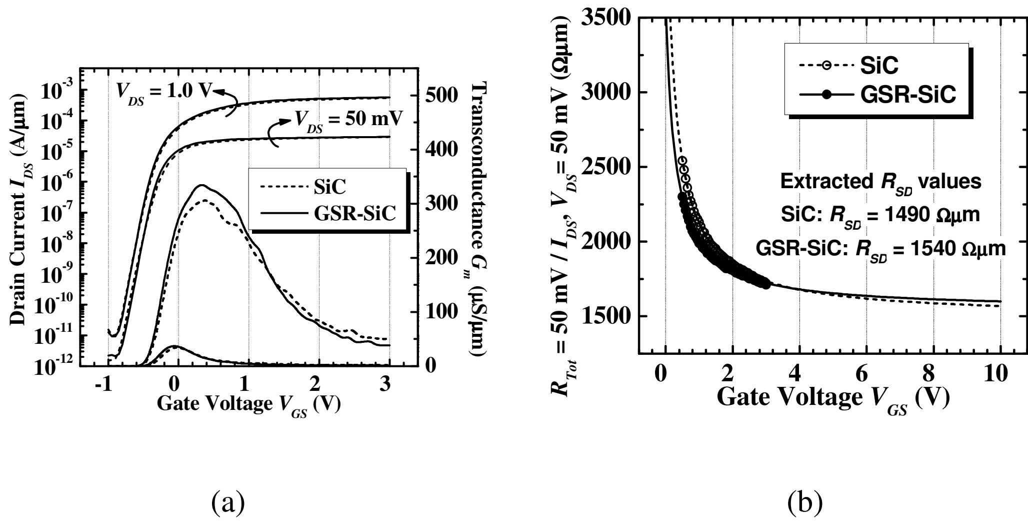



Figure 3-7 Cumulative probability plots of *DIBL*, *SS* and $V_{t,lin}$

Next, matched devices with similar subthreshold characteristics and series resistances were examined in greater detail. The electrical results also indicate performance enhancement in devices which underwent the spacer removal process. The $I_{DS}$-$V_{GS}$ and $G_m$-$V_{GS}$ characteristics for a pair of SiC and GSR-SiC devices are shown in Figure 3-8(a). These devices have comparable values of subthreshold swing and *DIBL*, which indicates similar effective channel lengths. Enhancement of both linear and saturation transconductances is observed. Figure 3-8(b) plots the total resistance $R_{Tot}$ against $V_{GS}$ for the same pair of devices. S/D Series resistances $R_{SD}$ were extracted by fitting the data points with curves generated using a simplified linear region drain current equation which includes an $R_{SD}$ parameter. $R_{SD}$ was estimated to be 1490 Ωµm and 1540 Ωµm for the SiC and GSR-SiC devices respectively. Since silicidation was deliberately not performed (for a fair comparison as explained later), the high values of $R_{SD}$ in these devices are expected. Due to the fact that strain depends on the thickness of the SiC S/D stressors, a fair comparison can only be made if both devices have the same growth thickness. By not performing silicidation in this FinFET test structure, there is a long unsilicided portion (~0.16 µm long) of the fin between the S/D extension regions and the contact via. The series resistance component of this portion, which is highly dependent on the SiC growth thickness, contributes substantially to the total $R_{SD}$. Hence, having such comparable values of $R_{SD}$ also implies similar SiC growth thicknesses, and ensures a fair comparison between these two devices. A 10% enhancement in drive current $I_{Dsat}$ was obtained in the GSR-SiC device over the conventional SiC device [Figure 3-9(a)]. This is significant, considering that the conventional SiC control device is also a

strained device. The enhancement factor is likely to be even higher in state-of-the-art devices with silicided S/D regions, where S/D series resistances are very much lower compared to the channel resistance. Since $R_{SD}$ of the GSR-SiC device is slightly higher than that of the conventional SiC device, the enhancement factor will be even larger if $R_{SD}$ values are exactly matched. The extra drive current enhancement most likely stems from the enhancement in longitudinal tensile channel strain as a result of the spacer removal process.

The backscattering parameters were extracted using the temperature dependent carrier backscattering model described in Section 2.4.1. Figure 3-9(b) shows that improvement in backscattering ratio $r_{sat}$, ballistic efficiency $B_{sat}$, and injection velocity $v_{inj}$ was obtained. Unlike the reduction of spacer width, which physically moves the SiC S/D stressors closer to the channel, the spacer removal technique allows strain in the channel to be increased without physically moving the stressors. This has the added advantage of relatively less carbon diffusion into the channel regions. It can be observed that $r_{sat}$ is not degraded in the case of spacer removal, in contrast with that observed for spacer width reduction.




(a) (b)

Figure 3-8 Electrical results for a pair of SiC and GSR-SiC FinFETs ($W_{Fin}$ = 40 nm, $L_G$ = 70 nm). (a) $I_{DS}$-$V_{GS}$ and $G_m$-$V_{GS}$ characteristics. Values of DIBL and subthreshold swing in this pair of devices are closely matched. Improved transconductance is observed in the GSR-SiC FinFET. (b) $R_{Tot}$-$V_{GS}$ characteristics. S/D series resistances were estimated to be quite similar, which allows for a fair comparison.

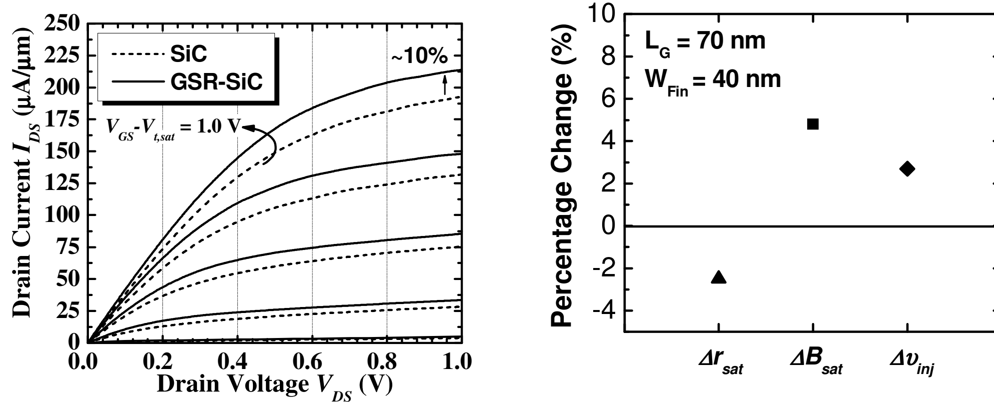



Figure 3-9 (a) $I_{DS}$-$V_{DS}$ family of curves ($V_{GS}$-$V_{t,sat}$ = 0 to 1.0 V in steps of 0.2 V). At $V_{GS}$-$V_{t,sat}$=1.0 V, $I_{Dsat}$ of the GSR-SiC FinFET was enhanced by 10% over that of the SiC FinFET. (b) Extraction of backscattering parameters shows improvement in backscattering ratio $r_{sat}$, ballistic efficiency $B_{sat}$, and injection velocity $v_{inj}$.

### 3.2.4 Summary

A simple and low-cost technique for improving the stress coupling efficiency of the lattice-mismatched S/D stressors has been demonstrated for strained n-channel FinFETs with SiC S/D stressor technology. An additional $I_{Dsat}$ enhancement of 10% was obtained as a result of the spacer removal process when a pair of closely matched devices was compared. The electrical results further indicate that even greater performance benefits can be reaped when physical gate lengths are scaled down. It is believed that performance benefits can also be derived by applying the spacer removal technique to strained p-channel FinFETs with SiGe S/D stressor technology as similar favorable mechanical equilibrium adjustment is also expected.

## 3.3 Contact Silicide-Induced Strain

### 3.3.1 Introduction

While stress developed in silicide films can be harnessed for mobility enhancement [3.7]-[3.9], silicide formation also consumes part of the lattice-mismatched silicon-germanium $Si_{1-x}Ge_x$ or silicon-carbon $Si_{1-y}C_y$ source and drain (S/D) stressor material. For maximum drive current performance in strained FinFETs, contact silicide technologies should not only achieve low series resistance but also minimize loss or negation of stress contributed by other S/D stressors. This is especially important for the ultra-thin-body or multiple-gate device architecture where the extent of lattice-mismatched S/D stressor embedding is limited by the semiconductor-on-insulator thickness and the volume of S/D stressor is small. The silicide and the lattice-mismatched S/D stressors should have complementary stress effects that work together in synergy to achieve optimum performance. However, compatibility or integration of $Si_{1-y}C_y$ S/D stressors and silicide stress effects has never been investigated before. Moreover, contact technology on $Si_{1-y}C_y$ S/D stressors is not well explored.

In this section, results on a new high-stress nickel silicide-carbon (NiSi:C) contact technology is reported. The first investigation of the compatibility of high-stress contact silicide films and lattice-mismatched silicon-carbon S/D stressors, and integration in multiple-gate transistors, is performed. Stress-induced drive current and transconductance enhancement in FinFETs with high stress NiSi:C and $Si_{1-y}C_y$ S/D stressors will be reported.

### 3.3.2 High stress Nickel-Silicide Carbon (NiSi:C)

For process development, 8-inch Si wafers as well as wafers with 40 nm $Si_{0.99}C_{0.01}$ epitaxially grown on Si were used. Ni with a thickness of ~ 30 nm was deposited. In order to study silicide stress and sheet resistance evolution with annealing, a two-step Ni silicidation was carried out in a single wafer rapid thermal furnace (SRTF). The first and second anneal steps were performed in $N_2$ ambient at 320˚C for 10 min. and 400˚C for 10 min., respectively. For process development efforts, formation of the NiSi:C layer fully consumed the $Si_{0.99}C_{0.01}$ film. After silicide formation, these wafers were subjected to cumulative isochronal annealing (10 min.) in a SRTF at temperatures ranging from 400˚C to 800˚C. After each anneal, sheet resistance and wafer curvature measurements were performed to monitor the evolution of sheet resistance and film stress in the NiSi and NiSi:C films.

Figure 3-10 shows the resistance of NiSi:C films to agglomeration when subjected to annealing at high temperatures. This behaviour is unlike NiSi, which agglomerates easily. The evolution of sheet resistance and stress of both NiSi and NiSi:C films with post-silicidation annealing is summarized in Figure 3-11(a) and (b), respectively. Figure 3-11(a) shows that NiSi:C films exhibit improved thermal stability compared to NiSi films. This is in agreement with results reported in [3.10]-[3.12]. It is observed that the sheet resistance of NiSi degrades at temperatures above ~550˚C, while NiSi:C films are stable up to about 800˚C. Uniformity in NiSi:C sheet resistance also improves with higher temperature annealing. Figure 3-11(b) shows the evolution of silicide film stress with post-silicidation annealing at various temperatures. NiSi:C starts off with a lower intrinsic film stress (+0.6 GPa) than NiSi at 400˚C. When annealed at higher temperatures (>450˚C), the tensile stress in NiSi:C

films is significantly increased, reaching +1 GPa for annealing temperatures above 575˚C. There is little increase in stress beyond 600˚C. This gives a large process window for the stress-enhancing post-silicidation annealing process. As phase transformation is completed at 450˚C even for RTA anneal [3.10], the phase transformation is likely to be completed at even lower temperatures for the soak anneals used in this experiment. The stress increase could be due to grain growth during the post-silicidation annealing. NiSi:C with tensile stress can induce tensile channel stress in n-channel transistors for electron mobility enhancement. The new NiSi:C films with +1.0 GPa tensile stress will be exploited for transistor strain engineering. Higher NiSi:C film stress will result in higher tensile strain in the transistor channel.

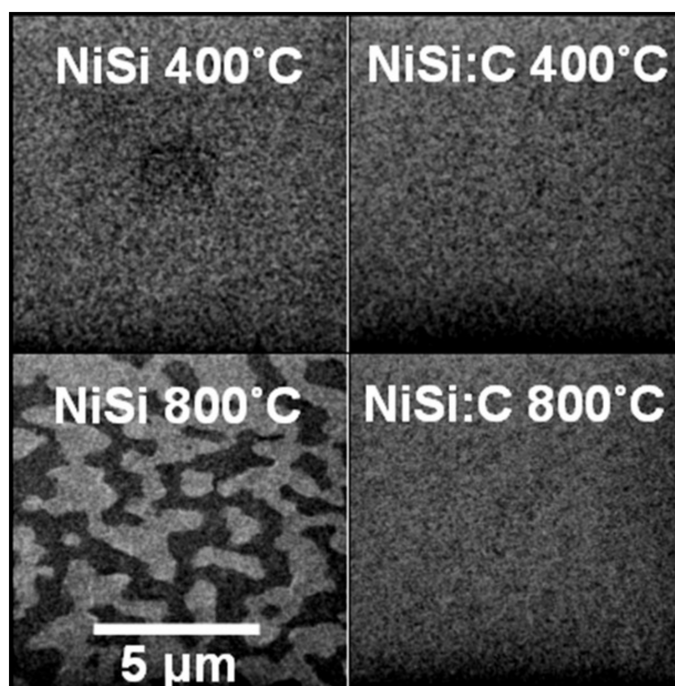
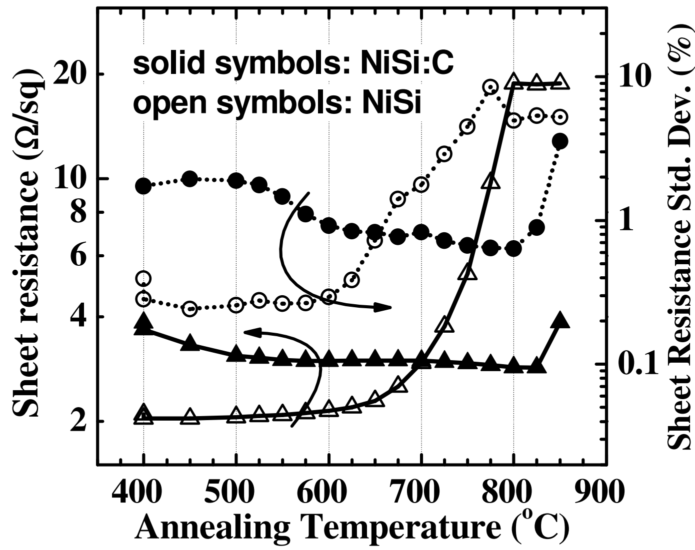
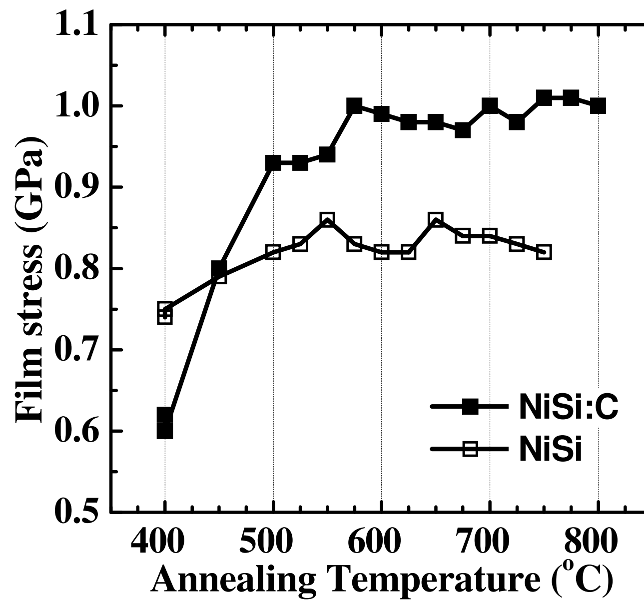



Figure 3-10 SEM images showing good thermal stability of NiSi:C compared to NiSi.




**(a)**




**(b)**

Figure 3-11 Evolution of (a) sheet resistance and its uniformity across a 200 mm wafer in NiSi and NiSi:C films and (b) stress evolution in NiSi and NiSi:C films, with cumulative isochronal anneals at increasing temperatures. In NiSi:C, stress increases from ~0.6 GPa to ~1 GPa with annealing at temperatures up to about 575°C, after which the stress levels appear to saturate.

### 3.3.3 Device Fabrication

High stress (+1.0 GPa, 600˚C post-silicidation anneal) and low stress (+0.6 GPa, 400˚C post-silicidation anneal) NiSi:C contacts were then integrated with <100>-oriented (100)-sidewall double-gate FinFETs (~30 nm-wide fins) incorporating ~40 nm of raised $Si_{0.99}C_{0.01}$ S/D regions, resulting in two device splits, "HS NiSi:C" and "LS NiSi:C", respectively. The NiSi:C contacts were formed using 20 nm of Ni. Figure 3-12 shows a schematic for the device fabrication process flow. The device fabrication flow is essentially similar to that detailed in Section 2.2.1, with a key difference being the presence of a thermal oxide hardmask on top of the fin so as to form double-gate FinFETs. Figure 3-13 illustrates the experiment splits that were fabricated.

- Channel implant
- Fin definition
- $SiO_2$ gate oxidation (18 Å)
- Poly-Si gate deposition and Gate implant
- Gate definition
- SDE implant
- Spacer formation (35nm) with stringer removal
- **Selective Epitaxial Growth of $Si_{0.99}C_{0.01}$**
- S/D implant and RTA activation
- Two-step Ni silicidation (20 nm Ni deposition, RTA 320˚C, excess Ni wet etch, and RTA 400˚C)
- **Stress-enhancing RTA anneal (600˚C) for: "HS NiSi:C"**
- PECVD ILD ($SiO_2$) deposition and metallization

Figure 3-12 FinFET fabrication process flow. A post-silicidation anneal enhances silicide stress.

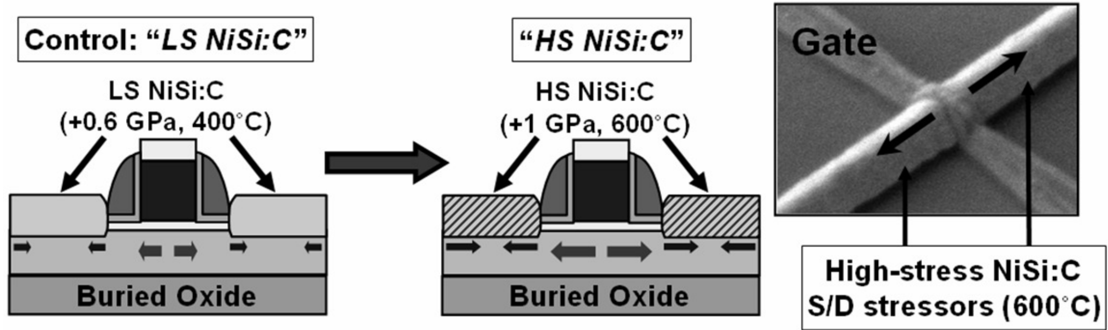
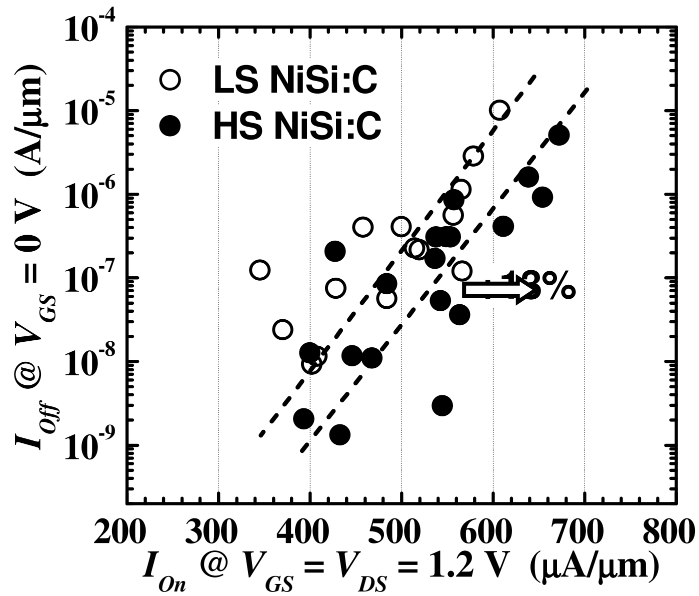


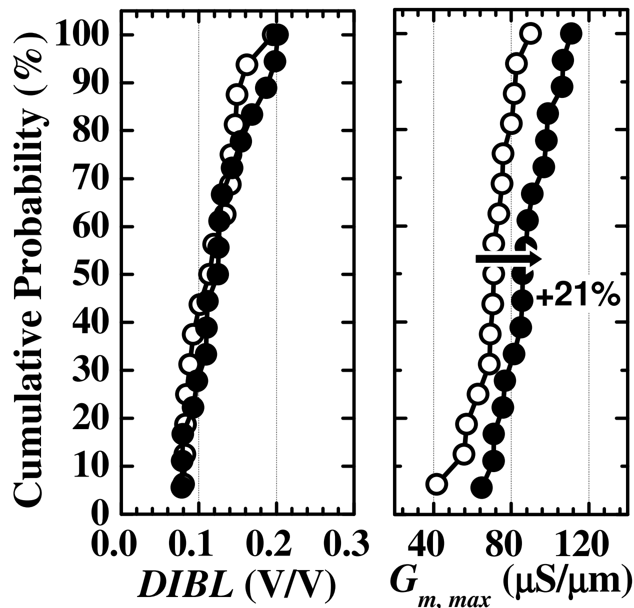

Figure 3-13 Schematic showing the experiment splits. In "HS NiSi:C" split, a post-silicidation stress enhancing anneal was performed.

### 3.3.4 Device Characterization

For (100) Si surfaces with a <100> carrier transport direction, which are the channel surfaces in these double-gate FinFET devices, uniaxial tensile strain can enhance electron mobility significantly. The $I_{Off}$-$I_{On}$ plot in Figure 3-14(a) indicates a ~13% $I_{On}$ enhancement in HS NiSi:C devices over LS NiSi:C devices at a fixed $I_{Off}$ of $10^{-7}$ A/µm. The spread in $I_{Off}$-$I_{On}$ data points is due to threshold voltage variation in doped-channel FinFETs. Cumulative distributions of *DIBL* and peak linear transconductance $G_{m,max}$ of the same set of devices in Figure 3-14(a) are plotted in Figure 3-14(b). It is clear from the comparable *DIBL* that the additional 600˚C anneal employed in the HS NiSi:C devices did not degrade short channel performance. The median enhancement in $G_{m,max}$ is about 21%, and is a further indication of electron mobility enhancement in HS NiSi:C devices.




(a)




(b)

Figure 3-14 (a) $I_{Off}$-$I_{On}$ characteristics showing ~13% $I_{On}$ enhancement at a given $I_{Off}$ of $10^{-7}$ A/μm. (b) Cumulative distribution for *DIBL* and peak linear $G_m$ for the same set of devices. Open circles are for low-stress NiSi:C contacts (LS NiSi:C) and closed circles are for high-stress NiSi:C contacts (HS NiSi:C). *DIBL* values are comparable for this set of devices. Devices with HS NiSi:C show a median peak $G_m$ enhancement of about 21% over devices with LS NiSi:C.

The S/D series resistances $R_{SD}$ of these devices are also examined. A matched pair of devices with comparable subthreshold swing and *DIBL* is selected for comparison [See Figure 3-15(a)]. Figure 3-15(b) plots the total resistance $R_{Tot}$ of each device against gate overdrive ($V_{GS}$-$V_{t,lin}$) at a $V_{DS}$ of 50 mV. Curves generated using a simplified linear region drain current equation, which includes an $R_{SD}$ parameter, were fitted to the measured data points using a method of least squares. It can be seen that $R_{SD}$ for both devices are comparable, despite the fact that the HS NiSiC film annealed at 600˚C has ~19% lower sheet resistance than the LS NiSi:C film. This suggests that the sheet resistance of the silicide contact only accounts for a small part of the total $R_{SD}$ in these devices. The $I_{DS}$-$V_{DS}$ characteristics for the same pair of devices are shown in Figure 3-16. At a gate overdrive of 1.2 V, 14 % enhancement in $I_{Dsat}$ was obtained. The peak transconductance was also enhanced by 24 %.

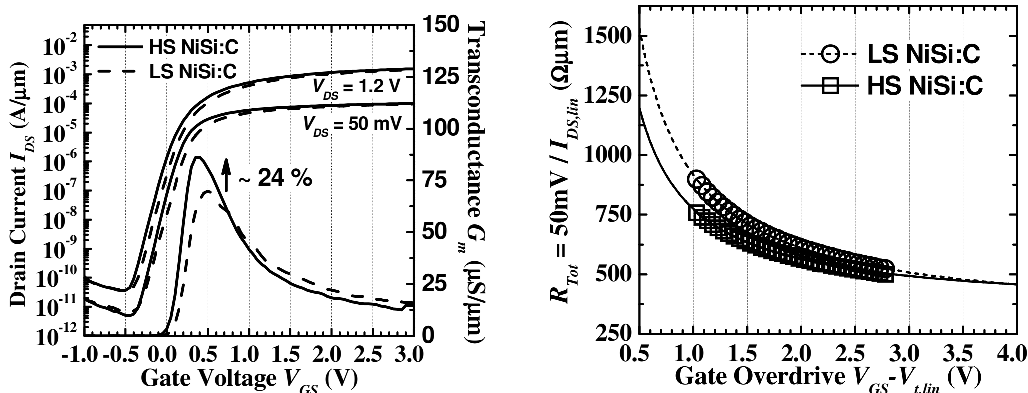



Figure 3-15 (a) $I_{DS}$-$V_{GS}$ and $G_m$-$V_{GS}$ characteristics of a pair of "LS NiSi:C" and "HS NiSi:C" devices. (b) $R_{Tot}$ is plotted against gate overdrive $V_{GS}$-$V_{t,lin}$ for the same pair of matched devices. The gate length is ~40 nm. S/D series resistances are estimated to be comparable in both devices.

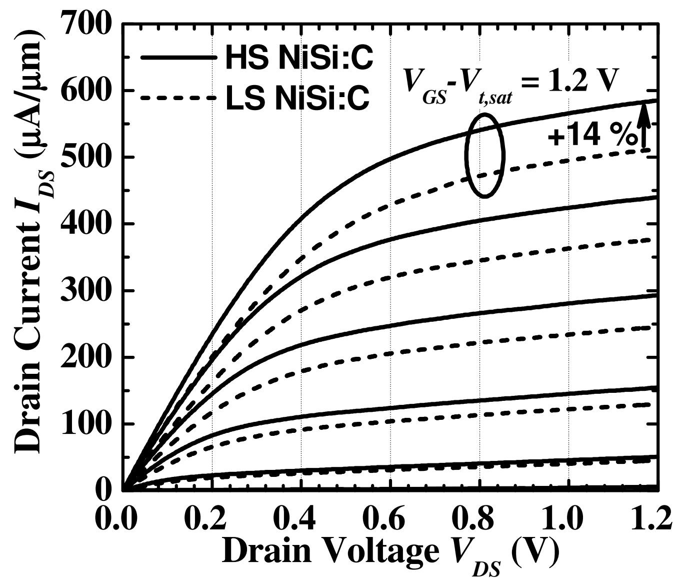



Figure 3-16 $I_{DS}$-$V_{DS}$ family of curves ($V_{GS}$-$V_{t,sat}$ = 0 to 1.2 V in steps of 0.2 V, $V_{t,sat}$ = $V_{GS}$ where $I_{DS}$ = $10^{-7}$ A/μm when $V_{DS}$ = 1.2 V). A ~14% $I_{Dsat}$ or $I_{On}$ enhancement due to increased silicide-induced stress effects is observed.

## 3.3.5 Compatibility with FUSI Metal-gate

### *3.3.5.1 Introduction*

In this section, the compatibility of high-stress NiSi:C with FUSI (fully silicided) metal gates is established. High performance gains of peak transconductance and drive current was obtained. Improved gate control of short channel effects was naturally obtained due to the increase in gate capacitance as poly-depletion is eliminated.

### *3.3.5.2 Device Fabrication*

As the polysilicon gate thickness was deliberately made very thin (~30 nm), simply removing the gate hardmask of the devices prior to the silicidation step results in the simultaneous silicidation of the gate together with the S/D regions. Figure 3-17

shows the process flow for the fabrication of “HS NiSi:C + FUSI Gate” devices. Figure 3-18(a) and (b) shows the isometric-view SEM images of a poly-Si gate FinFET with HS NiSi:C contacts (poly-Si gate is capped by a gate hardmask), and a FUSI gate FinFET with HS NiSi:C contacts respectively. Figure 3-18(c) shows the TEM image of a device as shown in Figure 3-18(b). One of the FUSI side-gates is captured within the FIB sample.

- Channel implant
- Fin definition
- $SiO_2$ gate oxidation (18 Å)
- Poly-Si gate deposition and Gate implant
- Gate definition
- SDE implant
- Spacer formation (35nm) with stringer removal
- Selective Epitaxial Growth of $Si_{0.99}C_{0.01}$
- S/D implant and RTA activation
- **Gate hardmask removal for:<br>“HS NiSi:C + FUSI Gate” split**
- Two-step Ni silicidation (20 nm Ni deposition, RTA 320˚C, excess Ni wet etch, and RTA 400˚C)
- **Stress-enhancing RTA anneal (600˚C) for:<br>“HS NiSi:C” and “HS NiSi:C + FUSI Gate”**
- PECVD ILD ($SiO_2$) deposition and metallization

Figure 3-17 FinFET fabrication process flow showing a single additional step of gate hardmask removal for the “HS NiSi:C + FUSI Gate” split. A post-silicidation anneal enhances silicide stress for both “HS NiSi:C” and “HS NiSi:C + FUSI Gate” splits.

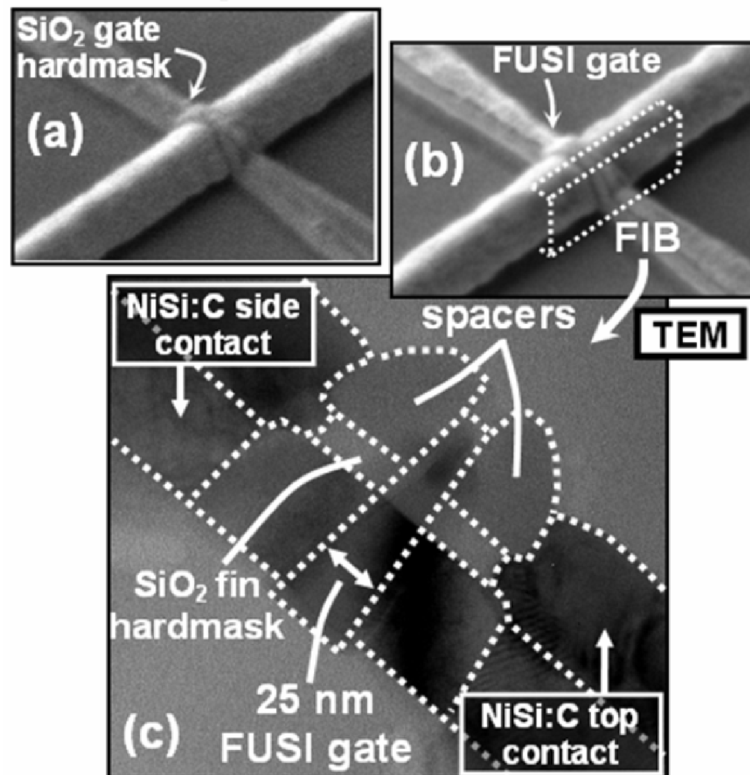



Figure 3-18 Isometric-view SEM images showing (a) a poly-Si gate FinFET with HS NiSi:C contacts (poly-Si gate is capped by a gate hardmask), and (b) a FUSI gate FinFET with HS NiSi:C contacts. (c) TEM image of a device as shown in (b). One of the FUSI side-gates is captured within the FIB sample.

#### *3.3.5.3 Device Characterization*

Figure 3-19 shows the $I_{Off}$-$I_{On}$ plot of the devices. A significant 40% enhancement in $I_{Dsat}$ was obtained by integrating HS NiSi:C with FUSI metal gate. The good performance obtained with the FUSI gate devices is testament to the compatibility between FUSI metal gate and high stress NiSi:C. Figure 3-20 shows the cumulative distributions of SS and $G_m$ of the same sets of devices used for the $I_{Off}$-$I_{On}$ plot. A clear improvement in SS is obtained for FUSI devices due to improved gate control as a result of eliminating the poly-depletion effect. $G_m$ enhancement is due to stress effects in "HS NiSi:C" devices. In "HS NiSi:C+FUSI Gate" devices, the enhancement

is due to the elimination of the poly-depletion effect, and the corresponding increase in gate capacitance, as well as gate-induced channel stress effects [3.14].

$I_{DS}$-$V_{GS}$ and $G_m$-$V_{GS}$ characteristics of a pair of "HS NiSi:C" and "HS NiSi:C + FUSI gate" devices is shown in Figure 3-21(a). With FUSI, gate stress effects and increase in $C_{ox}$ results in significant peak $G_m$ enhancement of 64%. As shown in Figure 3-21(b) Integration with a high-stress FUSI metal gate results in a further 32 % $I_{Dsat}$ enhancement.

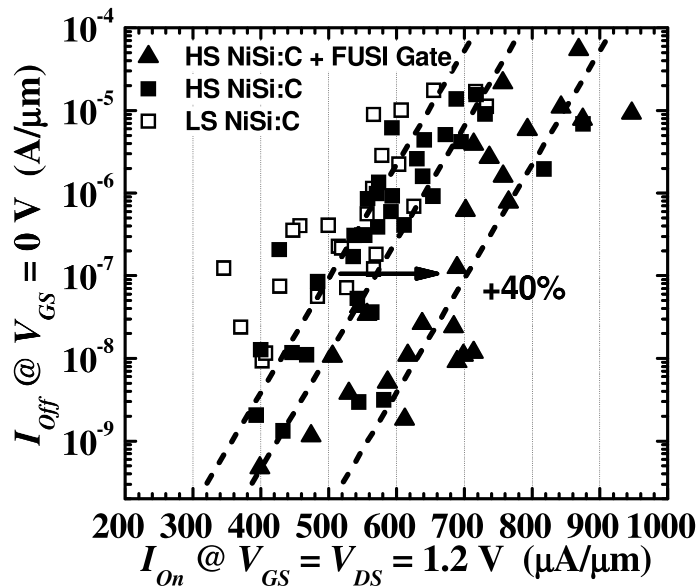



Figure 3-19 Integrating HS NiSi:C contacts with FUSI metal gate gives a combined enhancement of ~40 %.

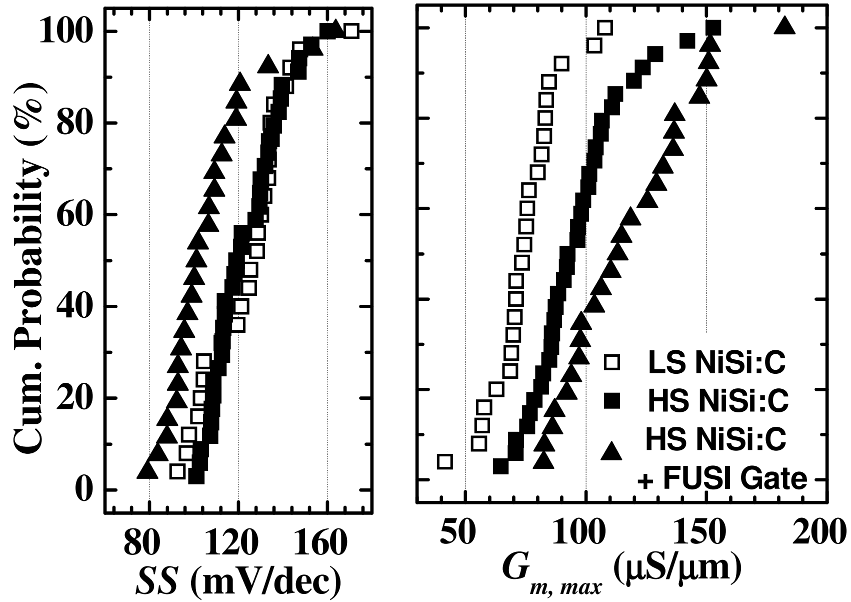
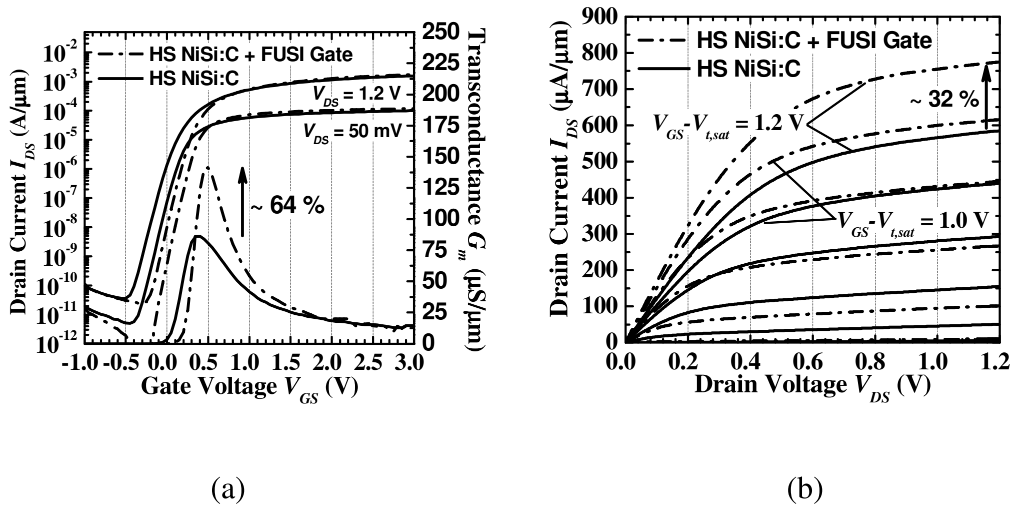



Figure 3-20 Cumulative distributions of SS and $G_m$ of the same sets of devices used for the $I_{Off}$-$I_{On}$ plot. A clear improvement in SS is obtained for FUSI devices due to improved gate control. $G_m$ enhancement is due to stress effects in "HS NiSi:C" devices. In "HS NiSi:C+FUSI Gate" devices, the enhancement is due to the elimination of the poly-depletion effect, as well as gate-induced channel stress effects.




(a) (b)

Figure 3-21 (a) $I_{DS}$-$V_{GS}$ and $G_m$-$V_{GS}$ characteristics of a pair of "HS NiSi:C" and "HS NiSi:C + FUSI gate" devices. With FUSI, gate stress effects and increase in $C_{ox}$ results in significant peak $G_m$ enhancement. (b) Integration with a high-stress FUSI metal gate results in a further 32 % $I_{Dsat}$ enhancement at $V_{GS}$-$V_{t,sat}$ = 1.2 V, where $V_{t,sat}$ = $V_{GS}$ at which $I_{DS}$ = 1 x $10^{-7}$ A/µm when $V_{DS}$ = 1.2 V.

### 3.3.6 Summary

NiSi:C is a thermally stable contact silicide that can be adopted in FinFETs with silicon-carbon S/D stressors. Higher silicide-induced tensile channel stress can be obtained by applying a stress-enhancing post-silicidation anneal at moderate temperatures with a large process window. Significant transconductance and drive current enhancement (+13%) was obtained as a result of increased silicide-induced strain, without compromising short channel control. This implies that high stress NiSi:C contacts, when optimally integrated with embedded silicon-carbon S/D stressors, can potentially result in synergistic S/D-induced channel stress effects as well as reduced series resistances in FinFETs.

Successful integration of devices with HS NiSi:C contacts and FUSI metal gate proves its compatibility. At a given $I_{Off}$ of 1 x $10^{-7}$ A/µm, the combination of these two techniques can provide up to 50 % $I_{Dsat}$ enhancement.

# 3.4 Scaling up Carbon Substitutionality with In-situ doped Si:CP S/D Stressors

## 3.4.1 Introduction

In several published reports, $Si_{1-y}C_y$ films with up to 1% substitutional carbon have been exploited in source/drain (S/D) stressor-induced strained-silicon technology for both planar transistors [3.15]-[3.19] as well as multiple-gate transistors such as FinFETs [3.19]-[3.22], resulting in significant $I_{Dsat}$ enhancement. In Chapter 2, fabrication and characterization of multiple-gate transistors (FinFETs) with SiC S/D regions of 1% substitutional carbon have been discussed. The performance enhancement has been attributed to an increase in electron mobility as a result of the tensile stress induced in the channel [3.23]. However, it is important to note that the solid solubility of carbon in silicon is extremely low [3.24]. While it is possible to substitutionally incorporate carbon above the solid solubility limit in silicon carbon films using non-equilibrium epitaxial growth processes, subsequent thermal processes such as S/D dopant activation anneals can cause the loss of carbon substitutionality in these metastable films via the formation of silicon-carbide precipitates [3.26], [3.27]. Naturally, the loss of carbon subsitutionality will cause a decrease in tensile channel strain. As such, the thermal instability places a limit on the performance enhancement of devices with implantation-doped $Si_{1-y}C_y$ S/D stressors. Besides scaling up the $Si_{1-y}C_y$ S/D stressor thickness and increasing the proximity between the stressor and the channel regions [3.22], or mechanically increasing the lattice strain coupling from the S/D stressors to the channel [3.28], it is highly desirable to find alternative ways of easily scaling up the channel stress induced in such transistors. *In-situ* doped $Si_{1-y}C_y$

S/D stressors have the potential of achieving high channel stress, but there are very few reports of the electrical characteristics of transistors with *in-situ* doped $Si_{1-y}C_y$ S/D stressors.

In this section, we show that Si:CP films with high substitutional carbon concentration (1.7 atomic % and 2.1 atomic %) can be employed to induce even larger strain in the channel regions of FinFETs than was previously possible using an implantation-doped epitaxial S/D stressor [3.20]. The reason is that the S/D stressors being *in-situ* doped renders further S/D dopant activation anneals unnecessary. Unlike prior work where $Si_{1-y}C_y$ stressors were implanted and annealed to form the S/D [3.15],[3.16],[3.18], *in-situ* doped $Si_{1-y}C_y$ S/D stressors do not need to experience high temperature S/D activation anneals that could reduce carbon substitutionality. This allows the preservation of the high substitutional carbon concentration of the stressor film in its as-grown state, in which the carbon percentage is determined by the epitaxial growth process conditions. The incorporation of exceedingly high carbon content for maximum lattice mismatch induced strain is therefore possible. This paper provides an extensive documentation of the electrical characteristics of FinFETs with $Si_{1-y}C_y$ S/D stressors *in-situ* doped with phosphorus, i.e. Si:CP, and the performance enhancement that can be achieved with such S/D stressors.

### 3.4.2 In-situ Phosphorus Doped Silicon-Carbon (Si:CP) Films

Phosphorous doped $Si_{1-y}C_y$ layers (Si:CP) described in this section were grown in an Epsilon® reduced pressure (RP) CVD epitaxial deposition tool manufactured by ASM. The growth precursors comprised Silcore® (ASM trademarked version $Si_3H_8$), (Mono-) methylsilane (20% MMS in $H_2$) and $PH_3$ (1% in $H_2$), respectively. Silcore,

being a precursor with efficient decomposition at low temperatures, is ideally suited for the incorporation of large amounts of substitutional carbon concentration $C_{sub}$ (> 2%). Increasing the substitutional carbon concentration in Si:CP films increases its lattice-mismatch with Si, therefore leading to higher Si:CP film stress.

Films with various percentages of substitutional carbon were grown and characterized using high-resolution X-ray diffraction (HRXRD). The HRXRD rocking curves reveal high carbon substitutionality in the Si:CP films of up to 2.3% (Figure 3-22). The clearly observable fringe patterns also suggest that these films possess excellent crystallinity. In lattice-mismatched SiGe films grown on Si, it is well established that the critical thickness, beyond which strain relaxation via a dislocation-mediated mechanism would occur, reduces with higher Ge concentration (higher lattice mismatch) [3.29],[3.30]. Increasing the C concentration in Si:CP films could also result in a similar behavior due to the increasing lattice mismatch and strain energy. It is expected that such dislocation-mediated strain relaxation would be undesirable for both silicon-germanium and silicon-carbon S/D stressor films in strained transistors, as strain levels in the channel will decrease. To investigate the possibility of dislocation-mediated strain relaxation of high C content Si:CP S/D films in typical CMOS strain engineering applications, 50 nm-thick Si:CP blanket films with various carbon percentages were grown on bulk Si wafers. Film stress measurements reveal a linear relationship between Si:CP film stress and substitutional carbon percentage, as shown in Figure 3-23. Since the measured stress value is linearly related to the lattice strain in the Si:CP film, the existence of a linear relationship between film stress and substitutional carbon percentage indicates that the no plastic relaxation has occurred. This implies that the metastable critical thickness

has yet to be reached for the Si:CP films at the growth temperatures, and seems to be the case even for the Si:CP film with 2.3% substitutional carbon. As long as this linear relationship between stress and carbon percentage is maintained, stress levels in the transistor's channel can be easily tuned or scaled by adjusting the carbon percentage in the Si:CP film.

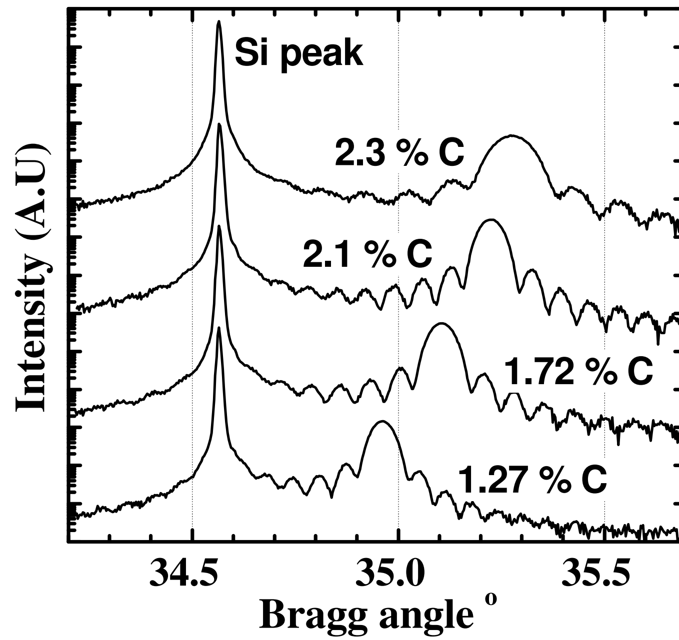



Figure 3-22 HRXRD rocking curve of Si:CP films with various substitutional carbon percentages showing excellent crystallinity in the films despite the high carbon content.

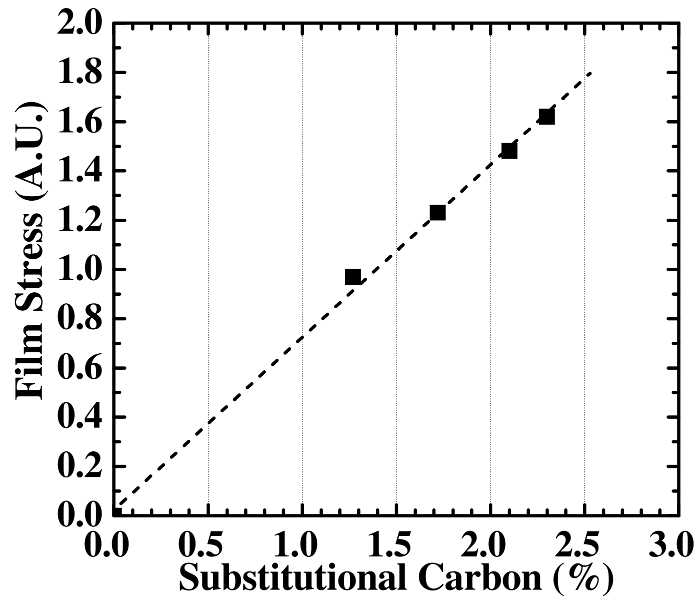



Figure 3-23 Wafer curvature measurements indicate a linear relationship between film stress and substitutional carbon percentage in the Si:CP films. This implies that higher stress can be obtained in the FinFET channel regions by incorporating Si:CP S/D stressors of higher substitutional carbon percentages.

### 3.4.3 Device Fabrication

The Si:CP process was optimized to selectively grow Si:CP films on the FinFET S/D regions. In Figure 3-24(a), an isometric-view SEM image shows the selective growth of Si:CP with 1.7 atomic percent of substitutional carbon concentration (also denoted as "Si:CP 1.7%" in this work) in the S/D regions of a FinFET test structure. The corresponding TEM is shown in Figure 3-24(b). Details of the process used to achieve the selective Si:CP films can be found in [3.31]. The formation of gate spacers involved an extra *in-situ* etch to remove the fin spacers, exposing the side surfaces of the fin for epitaxial growth, resulting in the formation of extended Π-shaped Si:CP S/D stressors, where the Si:CP epi-layer fully covers the top and sidewall surfaces of the fin. The wrapping of the S/D stressor around the Si fin ensures maximum lattice interaction for efficient lattice strain coupling from the S/D

stressors to the channel. Since the Si:CP S/D stressors are *in-situ* doped with phosphorus to a concentration of $3\times10^{20}$ cm$^{-3}$, parasitic S/D series resistances are also effectively reduced. With *in-situ* doping, an additional high temperature spike anneal for dopant activation becomes unnecessary and is eliminated in the device fabrication process. This is not only beneficial for preventing loss of carbon substitutionality, but will also be helpful in preventing EOT increases in transistors with ultra-thin oxides or high-κ gate dielectrics.

For the experiment detailed in this section, double-gate (DG) (110)-sidewall FinFETs were fabricated on SOI wafers using a FinFET process flow that is essentially similar to that described in Section 2.2.1. Figure 3-25 shows the key steps in the process flow. The gate stack comprises 20Å of thermally grown $SiO_2$ gate oxide, and phosphorus-doped poly-silicon gate. After source/drain extension (SDE) implant and activation, *in-situ* doped Si:CP raised S/D stressors were grown. This simultaneously forms the highly doped S/D regions. Three splits employing different S/D epitaxial films were fabricated in this work. A schematic depicting the device splits is shown in Figure 3-26. All device splits underwent the same process steps up to the selective epitaxial growth of the raised S/D regions. Phosphorus-doped Si, $Si_{0.983}C_{0.017}$ and $Si_{0.979}C_{0.021}$ films were grown selectively in the S/D regions, and are denoted as "Si:P", "Si:CP 1.7%" and "Si:CP 2.1%", respectively. Silicidation of the S/D regions was not performed in these experiments to maintain process simplicity.

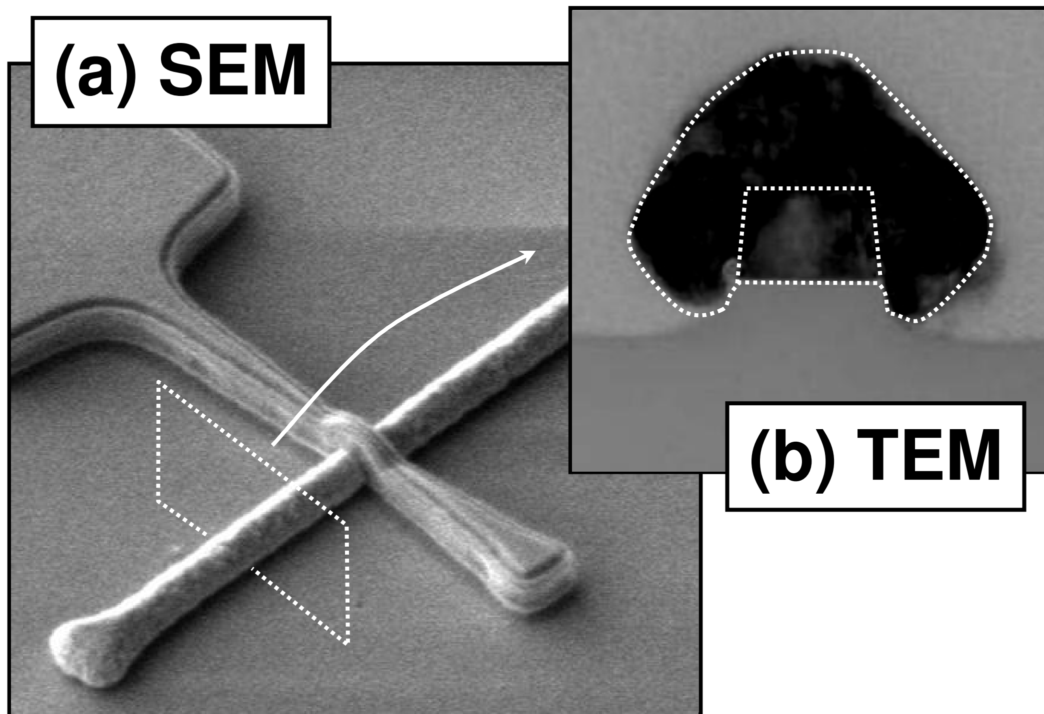



Figure 3-24 (a) Isometric-view SEM image showing selective epitaxial growth of Si:CP with 1.7 atomic percent of substitutional carbon concentration (also denoted as "Si:CP 1.7%" in subsequent figures) in the S/D regions of the FinFET test structure. (b) Cross-section TEM of the indicated S/D regions shows Si:CP growth on both the top and side surfaces of the fin, forming an extended Π-shaped S/D stressor that wraps around the Si fin for maximum lattice interaction.

- Channel Implant
- Fin definition
- Poly-Si/$SiO_2$ (20Å) gate-stack formation
- Gate definition
- Source/drain extension (SDE) implant
- Spacer formation with stringer removal
- SDE RTA implant activation
- **Spacer liner oxide undercut (wet etching)**
- **Selective Epitaxy Splits:**
  **Si:P: P-doped Si (Control)**
  **Si:CP 1.7%: P-doped $Si_{0.983}C_{0.017}$**
  **Si:CP 2.1%: P-doped $Si_{0.979}C_{0.021}$**

Figure 3-25 Process sequence showing key steps employed in FinFET device fabrication. Double-gate (DG) FinFETs were fabricated. The gate spacer formation scheme involves an extra in-situ etch to remove fin spacers, allowing the formation of extended Π-shaped S/D stressors.

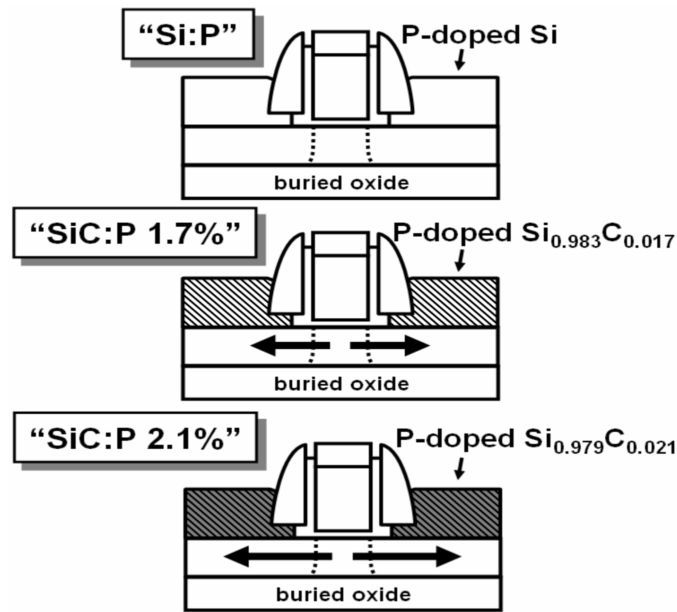



Figure 3-26 Schematic showing the three splits fabricated. They are structurally similar except for the selectively-grown S/D epitaxial film. Si:CP with substitutional carbon percentages of 1.7% and 2.1% were grown in the S/D regions of the strained FinFETs. Si:P was grown in the S/D regions of the control FinFETs.

Undercutting of the spacer liner oxide was performed using wet etching with HF prior to selective epitaxial growth of the S/D stressors. Figure 3-27 illustrates how this simple process is done. Prior to epitaxial growth, a wet clean using dilute hydrofluoric acid (HF) is typically performed to remove native oxide from the Si surface. By extending the duration of this HF clean step, it is possible to undercut the liner oxide underneath the nitride spacers. The degree of liner oxide undercut can be controlled by adjusting the duration of the HF cleaning step. This enables epitaxial growth not just on the exposed S/D regions outside of the gate nitride spacers, but underneath the gate nitride spacers as well. This effectively forms laterally encroached SiC:P S/D stressors for higher stress-coupling efficiency in the strained

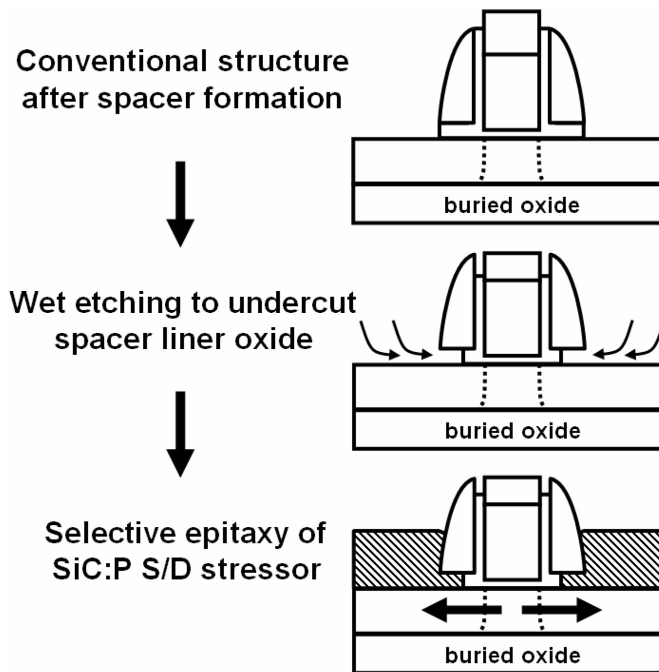



Figure 3-27 Schematic showing the key steps for forming the Si:CP S/D stressors for strained devices or Si:P S/D for control devices. Wet etching with HF is performed to undercut the $SiO_2$ liner oxide underneath the SiN spacer. This enables the epitaxial growth of Si:CP or Si:P in the S/D extension regions. Extension resistance is also reduced since the films are *in-situ* doped. For FinFETs with Si:CP S/D, closer proximity of S/D stressors to the channel leads to enhanced stress coupling for larger stress benefits.

FinFETs. Furthermore, this also reduces the S/D extension resistances since the epitaxial films are in-situ doped to a high doping concentration of $3 \times 10^{20}$ $cm^{-3}$ and have low sheet resistivity. In FinFETs or thin-body SOI FETs, where the S/D extension regions are very thin, S/D extension resistances can be a large fraction of the total parasitic series resistance. As such, reducing S/D extension resistances using laterally encroached in-situ doped films can be especially beneficial in such devices. It should, however, be noted that evaluation of the performance benefits of lateral stressor encroachment is not the focus.

### 3.4.4 Device Characterization

<110>-oriented (110)-sidewall p-channel FinFETs tend to have good performance due to the high hole mobility of (110) surfaces. While <100>-oriented (100)-sidewall n-channel FinFETs tend to show better performance, <110>-oriented (110)-sidewall n-channel FinFETs can be more densely laid out beside similarly oriented p-channel counterparts, making them of particular importance in density critical applications such as SRAM. All the devices discussed in this section are <110>-oriented (110)-sidewall n-channel DG FinFETs. The devices have gate lengths down to about 40 nm and fin widths of about 35 nm. Figure 3-28 and Figure 3-29 show the $I_{Off}$-$I_{On}$ plots for FinFETs having Si:CP S/D with $C_{sub}$ of 1.7% and 2.1%, respectively, compared to control FinFETs with *in-situ* doped Si S/D (denoted as Si:P). At a fixed $I_{Off}$ of $1\times10^{-7}$ A/μm, Si:P, Si:CP 1.7% and Si:CP 2.1% devices have an average $I_{On}$ of 569, 642, 681 μA/μm, respectively. FinFETs having Si:CP S/D stressors with $C_{sub}$ = 1.7% show ~13% $I_{On}$ enhancement at a fixed $I_{Off}$ of $1\times10^{-7}$ A/μm compared to the control. An excellent $I_{On}$ enhancement of ~20% over control was achieved for strained FinFETs with $C_{sub}$ = 2.1 %. This is a significant enhancement, considering that only 7% enhancement could be obtained in (110)-sidewall FinFETs with non-in-situ doped $Si_{0.99}C_{0.01}$ S/D stressors. The performance enhancement is further confirmed by the $I_{On}$ versus drain-induced barrier lowing (*DIBL*) plot in Figure 3-30, which shows approximately ~15% and ~20% enhancement for strained FinFETs with Si:CP S/D stressors having $C_{sub}$ of 1.7% and 2.1% FinFETs, respectively, over the control FinFET with Si:P S/D at a DIBL of about 100 mV/V. As *DIBL* is related to

the effective channel length, comparing $I_{On}$ enhancement at the same values of *DIBL* illustrates the enhancement at the same effective channel length.

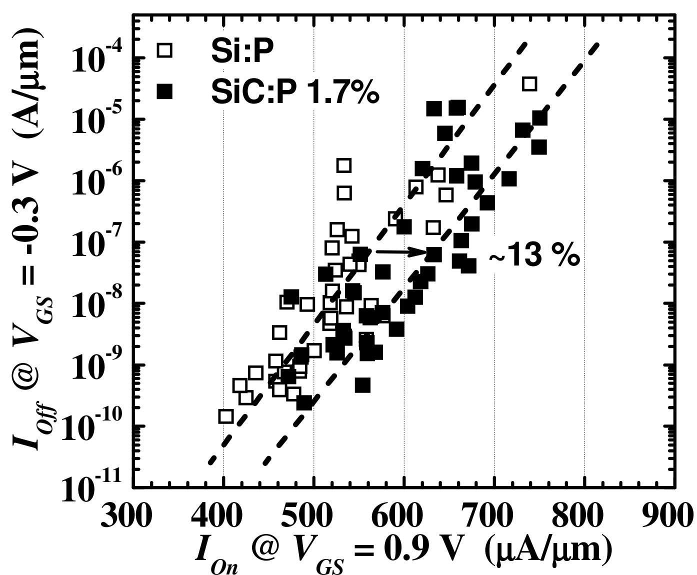



Figure 3-28 $I_{Off}$-$I_{On}$ plot shows ~13% enhancement in $I_{On}$ at a fixed $I_{Off}$ of $1 \times 10^{-7}$ A/μm due to the incorporation of Si:CP S/D stressors with 1.7% substitutional carbon.

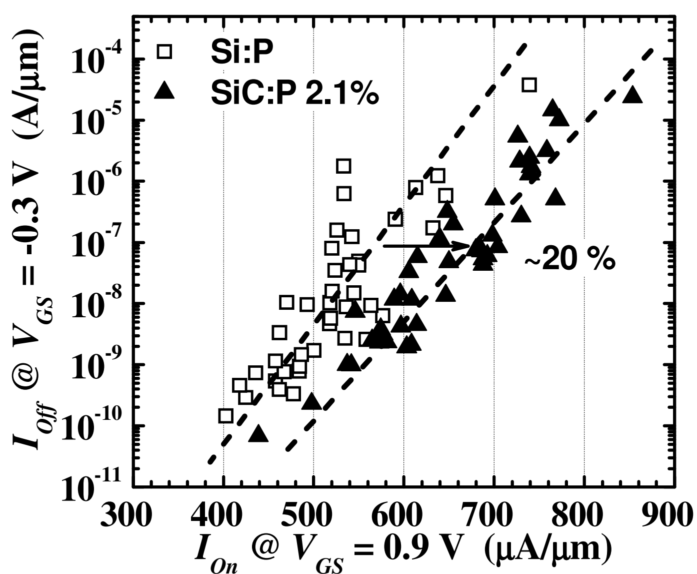



Figure 3-29 $I_{Off}$-$I_{On}$ plot shows ~20% enhancement in $I_{On}$ at a fixed $I_{Off}$ of $1 \times 10^{-7}$ A/μm due to the incorporation of Si:CP S/D stressors with 2.1% substitutional carbon.

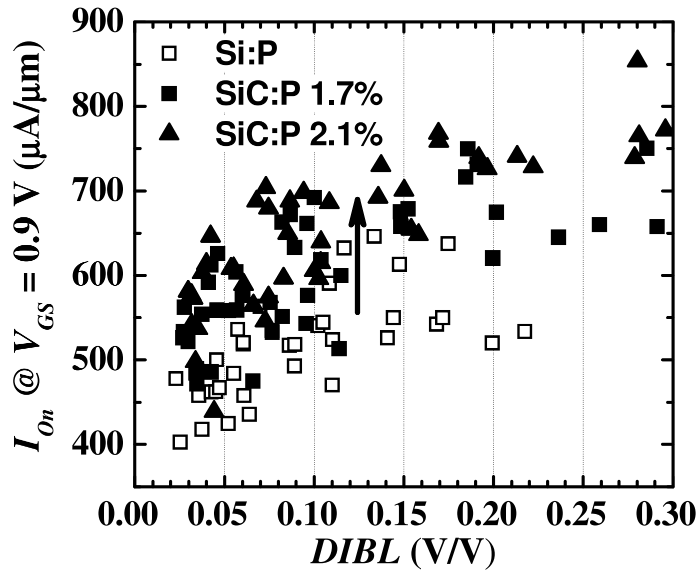



Figure 3-30 Up to ~20% enhancement in $I_{On}$ can be obtained by incorporating Si:CP S/D stressors with 2.1% substitutional carbon at a fixed value of drain-induced barrier lowering (DIBL). For the split with Si:CP 1.7%, an enhancement of ~15% can be obtained.

For S/D series resistance estimation, total resistance ($R_{Tot}$) at high gate overdrive was plotted against *DIBL* (Figure 3-31), where $R_{Tot}$ = 50 mV / $I_{DS}$ at ($V_{GS}$ - $V_{t,lin}$) = 2.7 V and $V_{DS}$ = 50 mV. At high values of gate overdrive, the value of total resistance tends asymptotically towards the value of the S/D series resistance. This is because the channel resistance decreases with increasing gate overdrive (and decreasing effective channel length) while the S/D series resistance stays relatively constant, approximating an asymptotic behavior in which $R_{Tot}$ tends towards the value to S/D series resistance at high gate overdrive. This allows for a qualitative estimation of the S/D series resistances using $R_{Tot}$. It is clearly observed that the FinFETs with Si:P S/D have lower S/D series resistances than the FinFETs with Si:CP S/D stressors. This can be attributed to the greater S/D series resistance

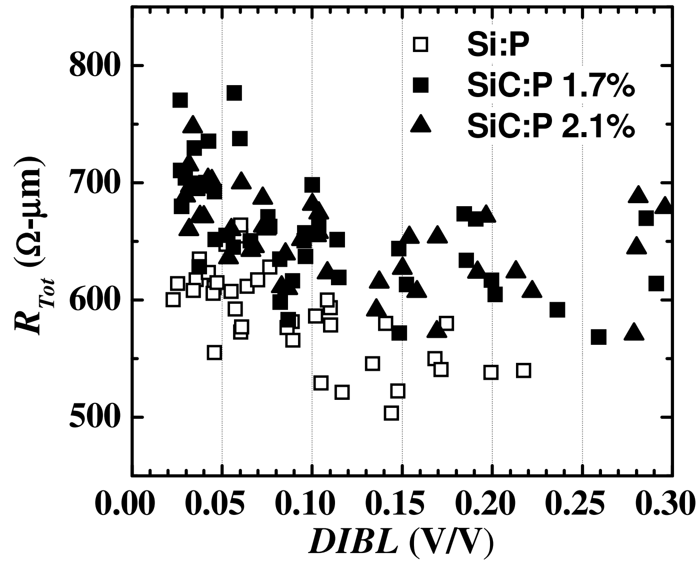



Figure 3-31 $R_{Tot}$ at high gate overdrive is indicative of the S/D series resistances of the various types of devices ($R_{Tot}$ = 50 mV / $I_{DS}$ @ $V_{GS}$-$V_{t,lin}$ = 2.7 V, $V_{DS}$ = 50 mV). It was found that Si:P devices have generally lower series resistances.

reduction in FinFETs with Si:P S/D compared to the FinFETs with Si:CP S/D stressors. This is due to the lower resistivity in the Si:P films compared to the Si:CP films. Sheet resistance measurements confirm this, as sheet resistances of 75, 128 and 160 Ω/square were obtained for Si:P, Si:CP 1.7% and Si:CP 2.1%, respectively. This implies that the actual strained-induced enhancement could possibly be larger, but is somewhat suppressed by the influence of larger S/D parasitic resistances in the devices with Si:CP S/D.

Next, we evaluate the short channel matching of Si:CP S/D FinFETs compared with Si:P S/D FinFETs. Figure 3-32 plots $I_{Off}$ against $V_{t,\mathrm{sat}}$ for devices from all three splits. The comparable $I_{Off}$ at various values of $V_{t,\mathrm{sat}}$ indicates excellent matching in short channel control. This confirms that the epitaxial processes for Si:CP did not degrade the short channel effects of the devices. This is expected since the epitaxial processes employed a very low thermal budget. Instead, high growth rates at

low epitaxial growth temperatures were ensured by adopting appropriate growth precursors. Figure 3-33(a) and (b) plots the cumulative distributions of *SS* and *DIBL* of devices shown in the $I_{Off}$-$I_{On}$ plots. The relatively large spread in the data points is due to the fact that the devices which comprise the $I_{Off}$-$I_{On}$ plots have a variety of gate lengths. Nevertheless, all three splits show comparable *SS* and *DIBL*, which once again points towards excellent short channel matching between Si:P and Si:CP devices. Figure 3-33(c) shows the cumulative distribution of $V_{t,sat}$. The slight decrease in threshold voltage can be attributed to channel strain-induced conduction band lowering. Figure 3-33(d) shows a clear enhancement in the peak transconductance $G_{m,max}$ of Si:CP devices over that of Si:P devices. $G_{m,max}$ enhancement is often attributed to mobility enhancement in strained transistors due to its reduced dependence on S/D series resistance effects. Hence, the enhancement in $G_{m,max}$ gives further evidence for the strain-induced mobility enhancement.

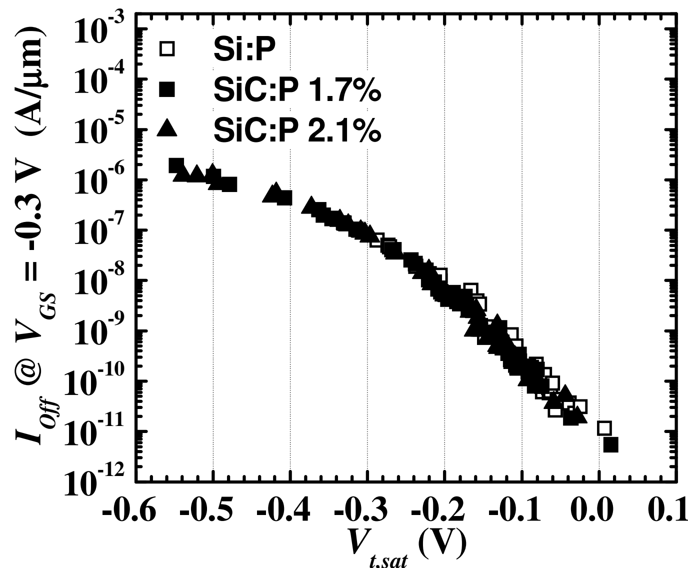



Figure 3-32 Excellent match in control of short channel effects for both Si:P and Si:CP devices is evident from the comparable $I_{Off}$ for devices with different values $V_{t,sat}$. Threshold voltage is lower than usual due to the use of $n^+$ poly-Si gate with a relatively low channel doping concentration.

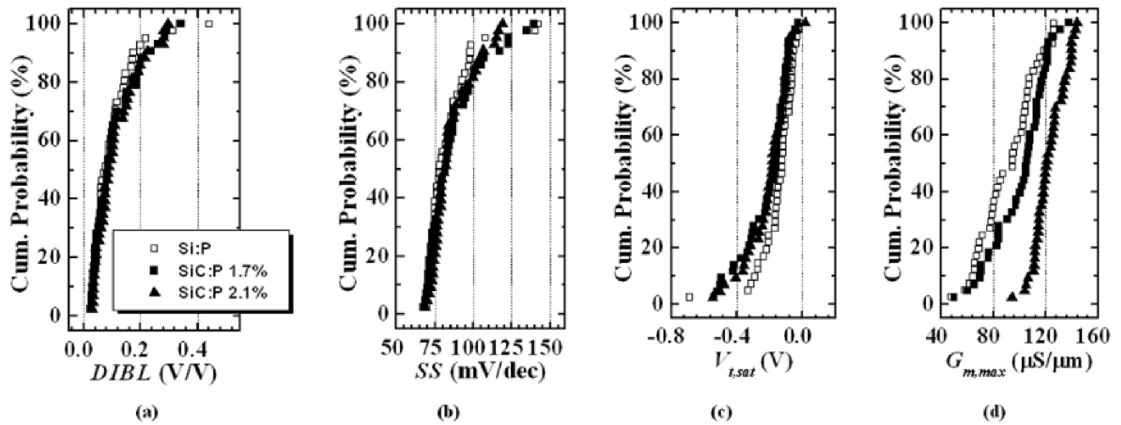



Figure 3-33 Cumulative distributions of (a) *DIBL*, (b) *SS*, (c) $V_{t,sat}$ ($V_{t,sat}$ = $V_{GS}$ @ $I_{DS}$ = 1μA/ μm, $V_{DS}$ = 1.2 V) and (d) $G_{m,max}$ of all the FinFET devices employed in the $I_{Off}$-$I_{On}$ plots. All three splits have comparable *SS* and *DIBL*, suggesting similar short channel control in devices from all three splits. $V_{t,sat}$ is lower for the strained devices than for the control, possibly due to conduction band lowering (See page 70). $G_{m,max}$ of both Si:CP splits show enhancement over the Si:P control.

A matched pair of Si:CP 2.1% and Si:P FinFETs were examined more closely. Figure 3-34 shows the $I_D$-$V_G$ transfer characteristics of the matched pair. Both these devices have a *DIBL* value of ~85 mV/V and a *SS* of ~80 mV/decade, indicating that they have approximately the same effective channel length. To further ensure a fair comparison, the S/D series resistances of the devices were estimated and compared. $R_{Tot}$ is plotted against gate overdrive in Figure 3-35. A first-order exponential decay fit of the data points was performed to extract the $R_{SD}$ values of the devices [3.32]. While this method of $R_{SD}$ extraction may not possess the best absolute accuracy, it provides for a good qualitative comparison for single devices in nanoscale multiple-gate FETs where device-to-device fluctuation can be larger that that of planar counterparts. The series resistance of the Si:P device (~490 Ωμm) was extracted to be slightly lower than that of the strained Si:CP 2.1% device (~560 Ωμm). This difference in the series resistance is attributed to the difference in resistivity of the laterally encroached regions of Si:P and Si:CP. Figure 3-36 plots the $I_D$-$V_D$ family of

curves for the same devices. It shows that incorporating Si:CP S/D stressors with $C_{sub}$ = 2.1% gives a ~23% enhancement for this particular device over the Si:P control, despite the fact that the series resistance difference is in favor of the Si:P device.

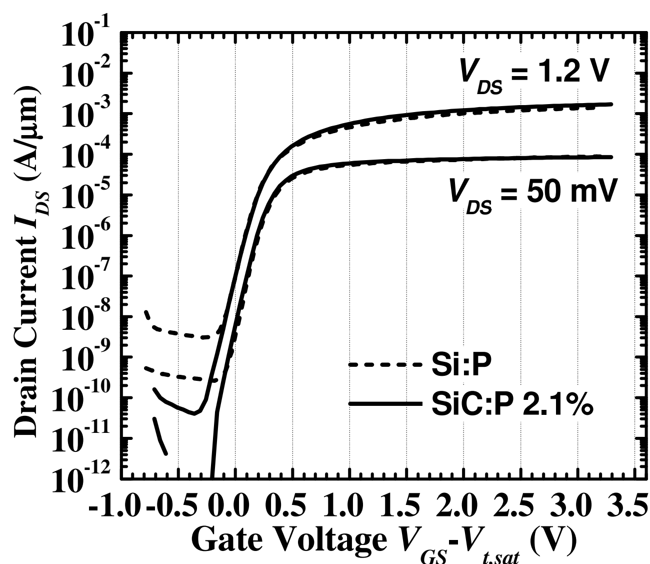



Figure 3-34 Transfer characteristics of a pair of matched FinFET devices showing comparable *DIBL* and *SS*. The *DIBL* is 85 mV/V and the *SS* is 80 mV/decade ($V_{t,sat} = V_{GS}$ @ $I_{DS}$ = 100 nA/ μm, $V_{DS}$ = 1.2 V).

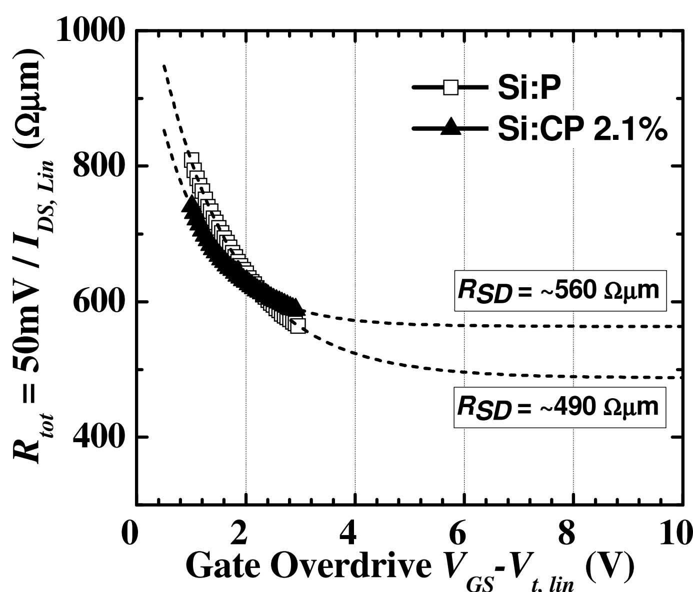



Figure 3-35 S/D series resistances of the matched devices were estimated by extrapolating $R_{Tot}$ to high gate overdrive voltages using a first-order exponential decay fit. The Si:P device has a slightly lower series resistance then the Si:CP 2.1% device.

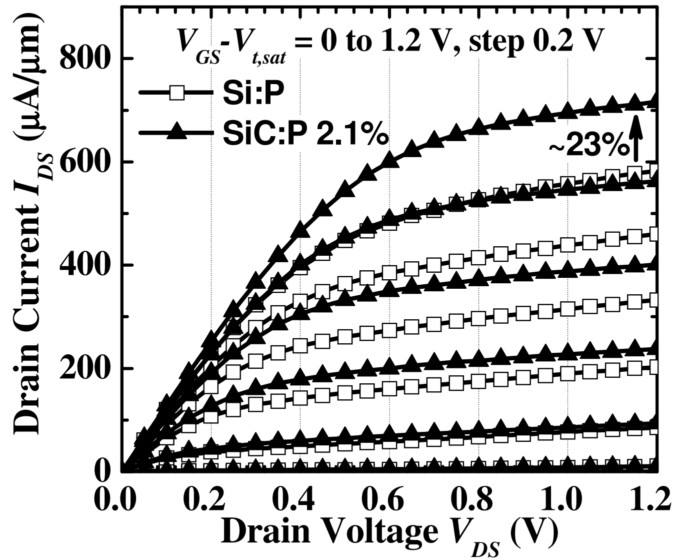



Figure 3-36 $I_{DS}$-$V_{DS}$ curves showing 23% $I_{Dsat}$ enhancement for this pair of matched devices ($V_{t,sat}$ = $V_{GS}$ @ $I_{DS}$ = 100 nA/ μm, $V_{DS}$ = 1.2 V). This enhancement is mainly attributed to strain effects.

### 3.4.5 Summary

The effectiveness of in-situ doped high substitutional carbon Si:CP S/D stressors in enhancing $I_{Dsat}$ for <110>-oriented (110)-sidewall DG FinFETs has been explored. It was found that a significant 20% strain-induced enhancement was obtained in Si:CP S/D FinFETs incorporating a substitutional carbon concentration of 2.1%. This culminated in an $I_{Dsat}$ value of 716 μA/μm, which is quite high, especially when considering that the S/D regions were not silicided.

## 3.5 Summary

Techniques for extending the performance of multiple-gate transistors with $Si_{1-y}C_y$ S/D regions have been proposed and experimentally proven. The spacer removal technique can be applied for a low cost yet effective way to increase the influence of the S/D stressors, regardless of the technology generation. Contact silicides to SiC S/D FinFETs have also been investigated. It was further shown that stress in the silicide film can be exploited and harnessed to induce further strain in the channel. This silicide stress-enhancing technique was also shown to be fully compatible with FUSI metal gate technology, resulting in high performance benefits (>+40% $I_{Dsat}$). In-situ doping removes the limitations of carbon substitutionality associated with implantation doped $Si_{1-y}C_y$ stressors, since a high temperature S/D activation anneal can be omitted.

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# Chapter 4

# 4. Germanium Condensation on SiGe Fin Structures: Ge enrichment and Substrate Compliance Effects

## 4.1 Introduction

Under the right conditions during thermal oxidation of SiGe, a phenomenon in which Si is selectively incorporated into the thermal oxide occurs, causing a pile-up of Ge at the oxidation front. This process is known as Ge condensation. During Ge condensation of crystalline SiGe, the condensed Ge-rich layer, being lattice mismatched with the substrate, develops high stress. This typically culminates in the formation of dislocations [4.1]. A schematic illustrating Ge condensation of bulk SiGe substrates is shown in Figure 4-1. Most Ge condensation experiments have been carried out on planar substrates with (001) surface orientations. Although work on (110) substrates has been reported [4.2], there was no detailed defect and lattice strain analysis. A significant dislocation density in strained Germanium-on-insulator (GOI) substrates, fabricated by Ge condensation of epitaxially-grown SiGe on Silicon-on-insulator (SOI) substrates, was reported [4.3]. This may be attributed to the low effective compliance of conventional SOI substrates below oxide viscous flow temperatures [4.4]-[4.6]. To this end, there have also been some efforts to improve SOI substrate compliance at relatively lower temperatures by incorporation of Boron

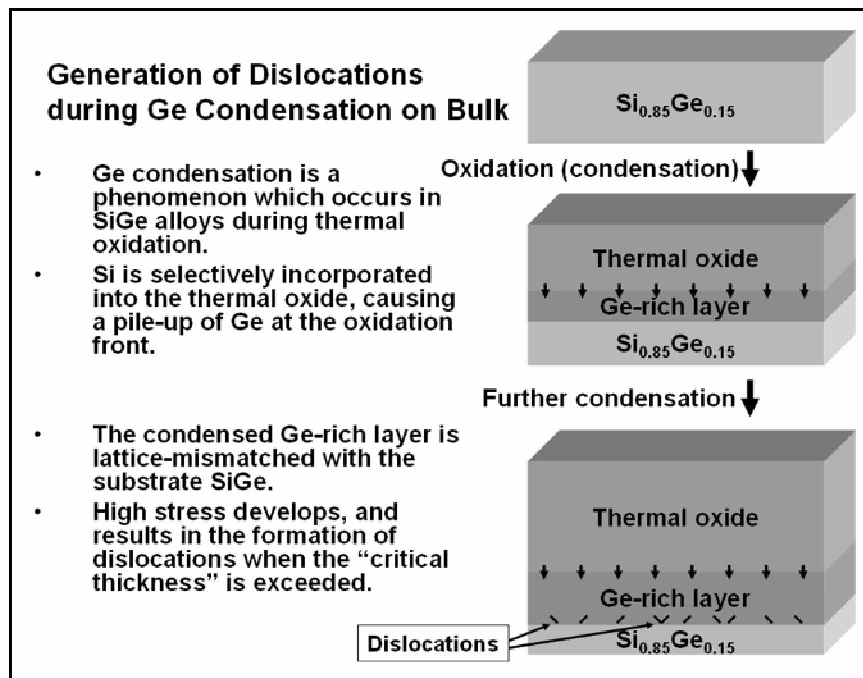



Figure 4-1 Schematic illustrating the phenomenon of Ge condensation of SiGe (eg. $Si_{0.85}Ge_{0.15}$) bulk substrates. Ge enrichment in the Ge-rich layer results in a large lattice mismatch with the $Si_{0.85}Ge_{0.15}$ substrate. This results in dislocation-mediated strain relaxation.

into the buried oxide layer, so as to reduce oxide reflow temperatures [4.7],[4.8]. Nevertheless, the use of SOI with either conventional oxide or Boron-doped oxide imposes limitations on the substrate quality for carrier-depleted GOI device fabrication. A free-standing planar thin film is another approach to realize substrate compliance, but its viability may be limited by fabrication difficulties, structural fragility and strained-induced film warping [4.9],[4.10].

Conversely, a vertical free-standing thin film, such as the Si fin body in a Fin Field-Effect-Transistor (FinFET), can be a practically feasible compliant substrate. The formation of fins is free from the earlier-mentioned limitations, since it has been shown to be compatible with Complementary Metal-Oxide-Semiconductor (CMOS) processes. Such vertical structures will also be resistant to strain-induced warping due to their structural symmetry. In this section, the results of applying Ge condensation

was to SiGe fins of various fin widths are reported. The Ge concentration, dislocation density and lattice strain in these vertical structures were investigated. Their relationship with fin widths in the context of substrate compliance is discussed.

## 4.2 Experiment

SiGe wafers with (001) surface orientation were used in this experiment. Each wafer comprised an epitaxially-grown strain-relaxed $Si_{0.85}Ge_{0.15}$ layer (thickness of ~0.5 μm) on a graded SiGe buffer layer (thickness of 2 μm) on Si substrate. Fin patterns of various widths (80 nm – 650 nm) were formed using 248 nm-lithography, photoresist trimming and Reactive Ion Etch (RIE) of SiGe. The fin height is typically about 480 nm. The patterned SiGe wafers were subjected to dry thermal oxidation at 875˚C for different durations. The oxidation temperature was chosen to be below the melting point of pure Germanium yet sufficiently high to ensure that no Germanium was incorporated into the thermal oxide. Applying Ge condensation to enhance Ge concentration in 3-dimensional SiGe structures is illustrated in Figure 4-2.

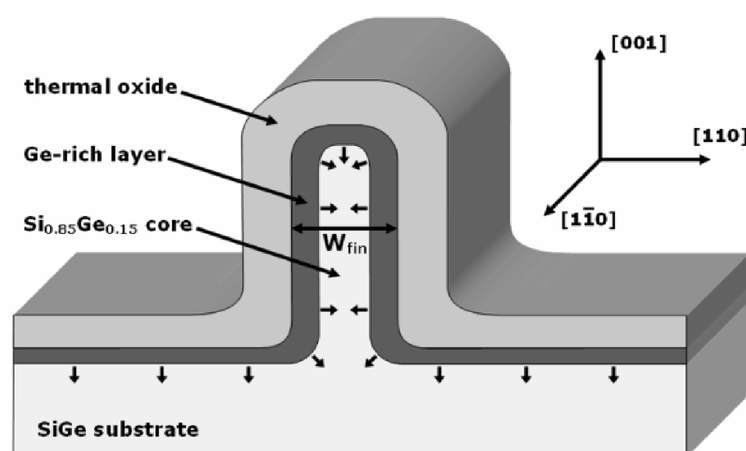
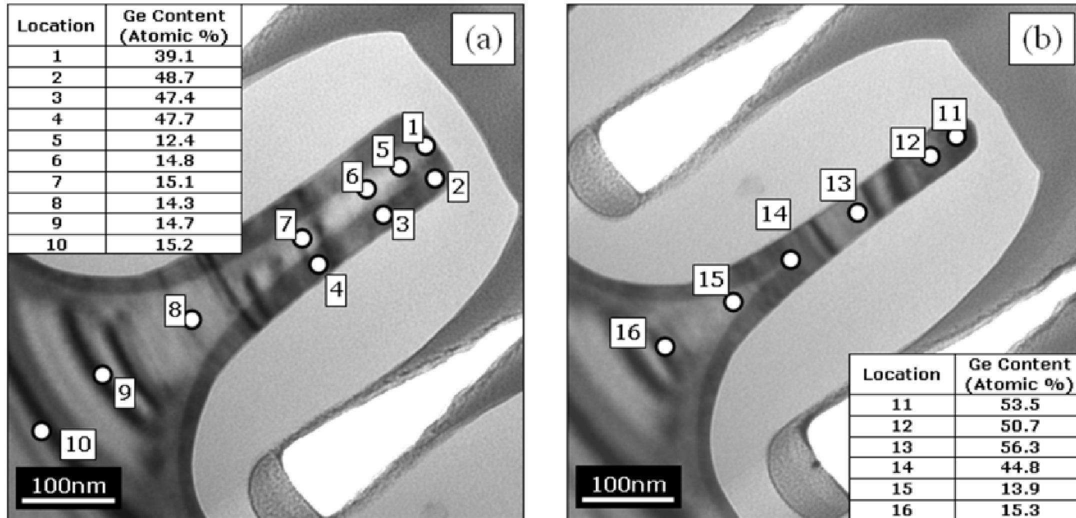



Figure 4-2 Cross-sectional schematic of a SiGe fin heterostructure during Ge condensation. The piling up of Ge at the oxidation front to form a Ge-rich layer is shown. As oxidation proceeds, the Ge-rich layer increases in thickness and the fin width ($W_{fin}$) decreases. This also results in decreasing $Si_{0.85}Ge_{0.15}$ core thickness ($T_{core}$).

## 4.3 Results and Discussion

Cross-sectional TEM micrographs of 2 fins with different fin-widths ($W_{fin}$) are shown in Figure 4-3. These fins had been subjected to 12 hours of dry oxidation at 875°C. It is observed that Ge condensation occurs for both (001) and (110) surfaces. Due to rejection of Ge from the oxide, the local Ge condensation rates are directly related to the local oxidation rates. The local oxidation rates are in turn dependent on surface orientation and presence of local stress. Oxidation rates are typically higher on the (110) surface as compared to the (001) surface. Low temperature oxidation below oxide viscous flow temperatures (~950˚C) also generates stress, which tends to build up in the corners of the structures and reduces the local oxidation rates [4.11]. Energy Dispersive Spectrometry (EDS) was used to estimate the atomic Ge concentration in different regions. The condensed Ge-rich regions, with Ge concentration in the range 40 – 55%, are visually distinguishable from uncondensed regions with Ge concentration of about 15%. Figure 4-3(a) shows a medium-width SiGe fin ($W_{fin}$=100 nm). The Ge concentration values at several locations are shown. The Ge concentration values ranges from 39.1% to 48.7% in the Ge-rich layer and remains at around 15% in uncondensed SiGe regions. Figure 4-3(b) shows a narrower fin ($W_{fin}$=45 nm). Due to the smaller fin width, the Ge-rich layers from opposite sides of the fin have merged homogeneously at the top portion of the fin. The Ge concentration in the merged portion is also observed to be higher – ranging from 50.7% to 56.3%. With further Ge condensation, the Ge concentration can be increased further.




| Location | Ge Content (Atomic %) |
|---|---|
| 1 | 39.1 |
| 2 | 48.7 |
| 3 | 47.4 |
| 4 | 47.7 |
| 5 | 12.4 |
| 6 | 14.8 |
| 7 | 15.1 |
| 8 | 14.3 |
| 9 | 14.7 |
| 10 | 15.2 |

| Location | Ge Content (Atomic %) |
|---|---|
| 11 | 53.5 |
| 12 | 50.7 |
| 13 | 56.3 |
| 14 | 44.8 |
| 15 | 13.9 |
| 16 | 15.3 |

Figure 4-3 Cross-sectional TEM images of 2 SiGe fins after 12 hours of Ge condensation. The oxidation temperature of 875°C is below the viscous flow temperature of thermal oxide of about 950°C, resulting in the unique geometry of the thermal oxide encapsulating the fin. The vertical sidewall surfaces of the SiGe fins also appear to be very smooth, making them suitable for FinFET applications where sidewall surface roughness would degrade carrier mobility dramatically at high electric field. The Ge atomic concentration values obtained by EDS at several locations in each fin are shown. (a) A wider fin ($W_{fin}$=100 nm) showing the Ge-rich layer and the sandwiched $Si_{0.85}Ge_{0.15}$ core. (b) A narrower fin ($W_{fin}$=45 nm) in which the Ge-rich layers have merged from opposite sides of the fin.

Figure 4-4 shows the EDS-derived Ge concentration profile across a 70nm-wide fin after 18 hours of Ge condensation. The Ge concentration within the Ge-rich layer is quite uniform (~50%). The Ge concentration profile is abrupt at the interface (heterojunction) between the Ge-rich layer and the $Si_{0.85}Ge_{0.15}$ core. The concentration profile is a result of competing dynamics of the processes such as oxidation of SiGe, Ge segregation out of the oxide region and Ge diffusion in SiGe with varying Ge concentration. The abrupt concentration profile at the heterojunction is consistent with the fact that Ge self-diffusion is five orders of magnitude faster than Ge diffusion in pure Si [4.12]. Considering the Ge-rich layer to be of a uniform concentration of 50%, the lattice mismatch between the Ge-rich layer and the $Si_{0.85}Ge_{0.15}$ core will be ~1.5%, according to Vegard's law. This mismatch will result in high strain in either or both the layers, depending on relative layer thicknesses. However, it is reasonable to

expect that the strain will be relaxed via the formation of dislocations when layer thicknesses exceed a certain critical thickness. The dislocation density was investigated using TEM. Figure 4-5 shows the cross-sectional TEM micrographs of 3 fins of different fin widths after 18 hours of Ge condensation. Figure 4-5(a) shows a wide fin ($W_{fin}$=480nm). It is observed that a large number of dislocations are present at the heterojunction between the Ge-rich layer and the $Si_{0.85}Ge_{0.15}$ core of the fin. A larger number of dislocations are found in the fin corners, possibly due to higher localized strain. The dislocation density at the (110) heterojunction is estimated to be about ~40 $\mu m^{-1}$. Figure 4-5(b) shows a medium-width fin ($W_{fin}$=70nm) in which much fewer dislocations (~8 $\mu m^{-1}$) are found at the (110) heterojunction as compared to the wide fin. No dislocations are observed at the heterojunction even in the fin corners. Since the lateral thicknesses of the Ge-rich layer ($T_{(Ge\text{-}rich\ layer)}$) in both fins are almost identical, the difference between these 2 fins lies in the lateral thickness of the sandwiched $Si_{0.85}Ge_{0.15}$ core ($T_{core} = W_{fin} - 2 \times T_{(Ge\text{-}rich\ layer)}$). We can thus hypothesize that the thin $Si_{0.85}Ge_{0.15}$ core ($T_{core}$ < 15 nm) in the medium-width fin exhibits compliance and complies easily with the lattice constant of the Ge-rich layer. If this is the case, the core will be highly-strained and few dislocations will be formed. This is consistent with reported results regarding epitaxial growth of a thick SiGe layer on thin Si membranes [4.13]. Figure 4-4(c) shows a narrow fin ($W_{fin}$=20nm). The Ge-rich layers from opposite sides of the fin have merged to form a homogeneous Ge-rich fin in which no dislocations are observed. During Ge condensation, core compliance played a dominant role in strain relaxation, resulting in a very low dislocation density (< 1 $\mu m^{-1}$). The Ge concentration in this fin is found to be ~90%.

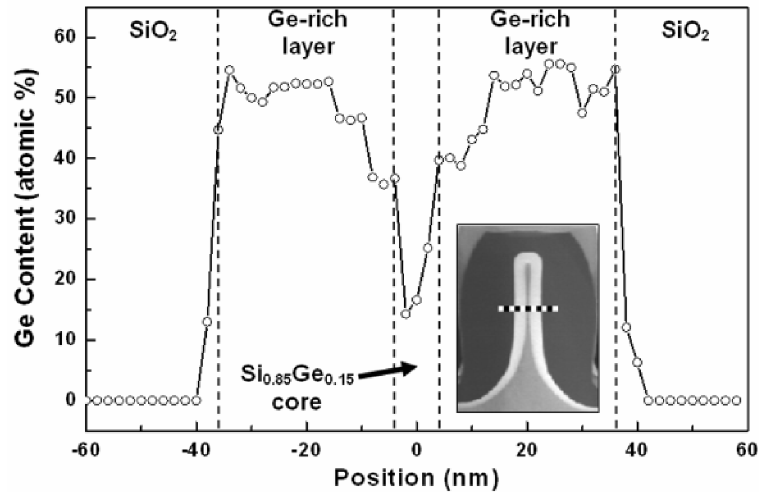



Figure 4-4 Ge concentration profile across a medium-width SiGe fin ($W_{fin}$=70nm, see inset) that has undergone 18 hours of Ge condensation. The Ge concentration within the Ge-rich layer is quite uniform. The Ge concentration profile is observed to be rather abrupt at the interface between the Ge-rich layer and the $Si_{0.85}Ge_{0.15}$ substrate.

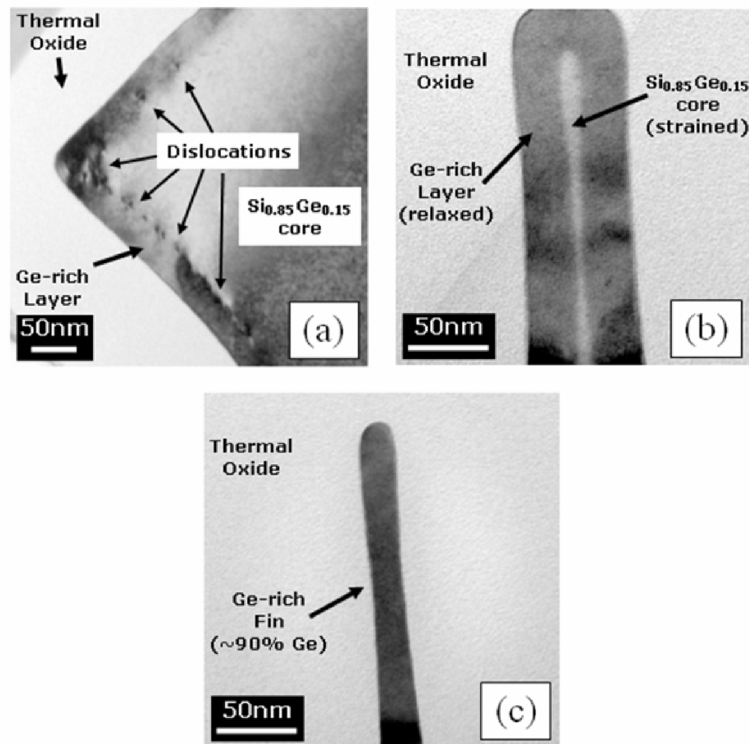



Figure 4-5 Cross-sectional TEM images highlighting dislocations in 3 SiGe fins of different fin widths ($W_{fin}$) after 18 hours of Ge condensation. (a) A wide fin ($W_{fin}$=480nm) with a high dislocation density at the interface between the Ge-rich layer and the $Si_{0.85}Ge_{0.15}$ core. (b) A medium-width ($W_{fin}$=70nm) fin with a much lower dislocation density. (c) A narrow homogenous Ge-rich fin ($W_{fin}$=20nm, ~90% Ge concentration) showing no observable dislocations.

To further examine the compliant nature of the sandwiched $Si_{0.85}Ge_{0.15}$ core, a combination of High-Resolution Transmission Electron Microscopy (HRTEM) and Fast Fourier Transform (FFT) diffractogram [4.14] was used to derive the lattice mismatch between the Ge-rich layer and the $Si_{0.85}Ge_{0.15}$ core for each of the 2 wider fins ($W_{fin}$=70nm, 480nm). In short, this technique requires analysis using high-resolution lattice images of the heterojunctions. A schematic explaining this technique is shown in Figure 4-6. With the help of FFT diffractograms, the relative lattice constants of the heterolayers were extracted and used to derive the lattice mismatch. If the heterolayers are both relaxed, the lattice mismatch will be ~1.5%, according to Vegard's law. For the wide fin ($W_{fin}$=480nm), the lattice mismatch was derived from the analysis to be 1.3±0.3%, which is close to the value of 1.5%. This clearly points to dislocation-mediated strain relaxation in these heterolayers, which is expected of a non-compliant substrate. For the medium-width fin ($W_{fin}$=70nm), the lattice mismatch was derived to be only 0.5±0.3%, suggesting the existence of a large amount of strain (~1±0.3%). For a face-centered cubic (FCC) lattice, the ratio $a_{[110]}/a_{[001]}$ (where $a_{[110]}$ is the atomic spacing in the [110] direction and $a_{[001]}$ is the atomic spacing in the [001] direction) has a value of $\sqrt{2}$. Strain causes distortion of the cubic lattice and the deviation of this ratio from $\sqrt{2}$. For the medium-width fin ($W_{fin}$=70 nm), the ratio $a_{[110]}/a_{[001]}$ of the Ge-rich layer was calculated to be within 0.15% of $\sqrt{2}$. This indicates that the Ge-rich layer is almost strain-free and the majority of the strain is present in the $Si_{0.85}Ge_{0.15}$ core, thus confirming the compliant nature of the core. In the case of the narrow homogeneous fin ($W_{fin}$=20nm) with 90% Ge concentration, the ratio was also within 0.15% of $\sqrt{2}$, indicating its strain-relaxed nature.

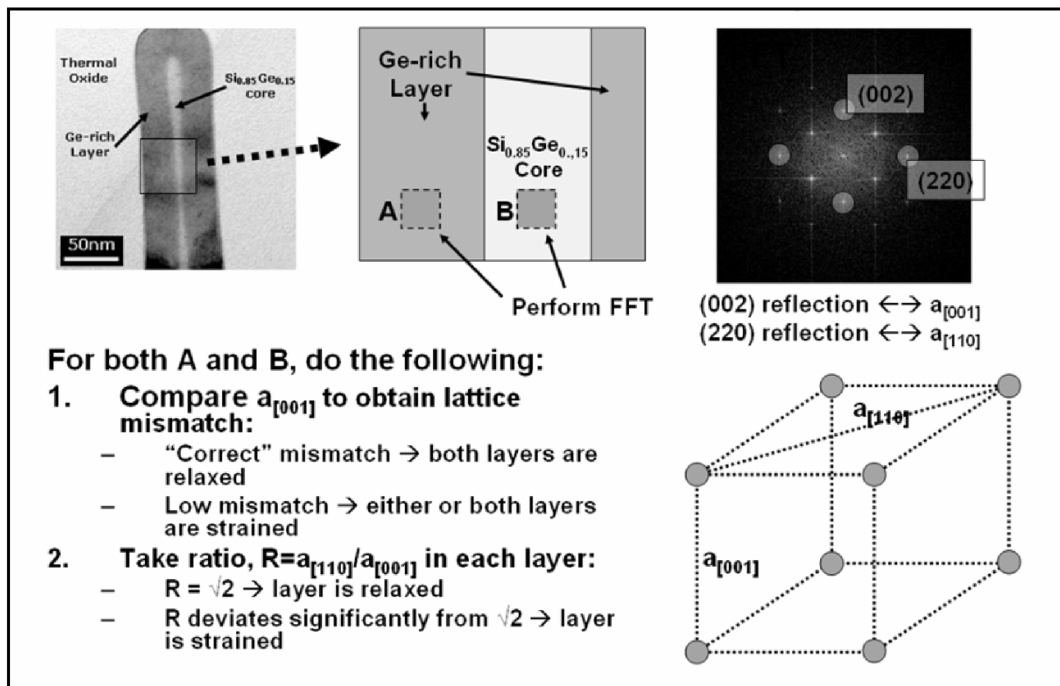



Figure 4-6 A schematic explaining how the estimation of strain using HRTEM FFT diffractogram analysis is performed.

## 4.4 Summary

In conclusion, narrow SiGe fins demonstrated substrate compliance during Ge condensation. The effect of substrate compliance allowed the condensed Ge-rich layer on opposite sides of a SiGe fin to relax with greatly reduced dislocation formation. This was further evidenced by the formation of dislocation-free Ge-rich fins with ~90% Ge content. These results can be useful for engineering FinFETs or Nanowire-FETs employing high mobility channel material such as strained Si, SiGe and or Ge, as CMOS technology scales beyond the 32 nm technology generation. In Chapter 5, the Ge condensation technique is applied to p-channel FinFETs with SiGe S/D stressors. In Chapter 6, the effect of enhanced substrate compliance in narrow S/D regions is utilized to increase channel stress in nanowire-FETs with Ge S/D stressors.

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# Chapter 5

# 5. P-Channel FinFETs with Embedded SiGe stressors Fabricated using Ge condensation

## 5.1 Introduction

For p-channel transistors, SiGe source and drain (S/D) stressor is commonly used to induce strain in the device channel. By making use of the lattice mismatch between Si and SiGe, compressive strain can be induced in the channel to enhance hole mobility. For enhanced strain effect, a S/D recess etch can be performed on the S/D region prior to the SiGe epitaxial growth to realize embedded SiGe S/D stressors [5.1],[5.2].

The fabrication of p-channel FinFETs with embedded SiGe S/D has been demonstrated by Verheyen *et al.* [5.3], achieving an $I_{Dsat}$ enhancement of 25% over control FinFETs. Their integration scheme involved performing an anisotropic S/D recess etch prior to SiGe epitaxy on the top surface. However, since the conduction channel for the FinFET lies on the fin sidewalls as well, an isotropic etch should ideally be performed on the S/D regions and the SiGe epitaxial layer should also be grown on the sidewalls [5.4],[5.5] to maximize the strain effects. This will be very challenging especially when the fin width is scaled down drastically to less than 10 nm for better SCE control. Local Ge condensation in the S/D regions can be an alternative technique of fabricating embedded SiGe S/D stressors, which eliminates the need for a recess etch [5.6]. In this section, sub-30 nm tri-gate FinFETs with

embedded SiGe S/D stressors were formed using a novel condensation process on the SiGe fin S/D regions [5.7] and characterized. Compressive stress is exerted on the channel from the SiGe S/D regions on both the top and sidewalls.

## 5.2 Device Fabrication

Figure 5-1 shows a schematic of the devices fabricated in this work. Comparisons were made between two structures having a different SiGe profile at the fin S/D region. Silicon-on-insulator (SOI) substrates with 35 nm thick Si were used. Threshold voltage $V_t$ adjust implant was performed. Fin patterning employed 248 nm lithography, resist trimming, and reactive ion etching (RIE) to achieve fin widths $W_{fin}$ down to 30 nm. Sacrificial oxidation was performed to repair the fin sidewall damage due to the RIE. $SiO_2$ gate dielectric (~3 nm) was thermally grown, followed by polycrystalline-silicon gate deposition and etch. Sub-30 nm gate lengths were achieved as shown in Figure 5-2. During the silicon nitride (SiN) spacer formation process, an excess over-etch was performed for the removal of SiN stringer at the fin sidewall as shown in Figure 5-2(a), therefore enabling the exposure of fin sidewall surfaces for selective SiGe growth to maximize the strain effects.

Selective epitaxial growth of $Si_{0.75}Ge_{0.25}$ was performed on all wafers. Figure 5-2(b) shows a SEM image of a FinFET with the S/D region of the fin and contact covered by the SiGe epi-layer. The existence of epitaxial SiGe on the fin sidewall and top surfaces in the S/D regions was clearly observed. On one device structure with SiGe S/D, Ge condensation, which is essentially a thermal oxidation process, was performed at 950°C for 5 min. For the control wafer, the Ge condensation process step was skipped. When Ge condensation or oxidation was performed on a SiGe-

covered Si fin, Si atoms from the SiGe are oxidized to form an oxide while Ge atoms are driven into the S/D regions of the fin. S/D implant and anneal were performed after the removal of gate hardmask to complete the fabrication process. Direct probing was done to obtain the electrical characteristics of the device. As the absolute channel resistance of the FinFET device is much larger than the parasitic probe contact resistance and diffusion resistances, direct probing showed good repeatability with probing a single device in different regions of the probe pad. This allows reasonably good accuracy in the measurements. Series resistance was also extracted by applying a high gate bias and assuming that the channel resistance is very small as compared to the S/D resistance at this condition [5.8].

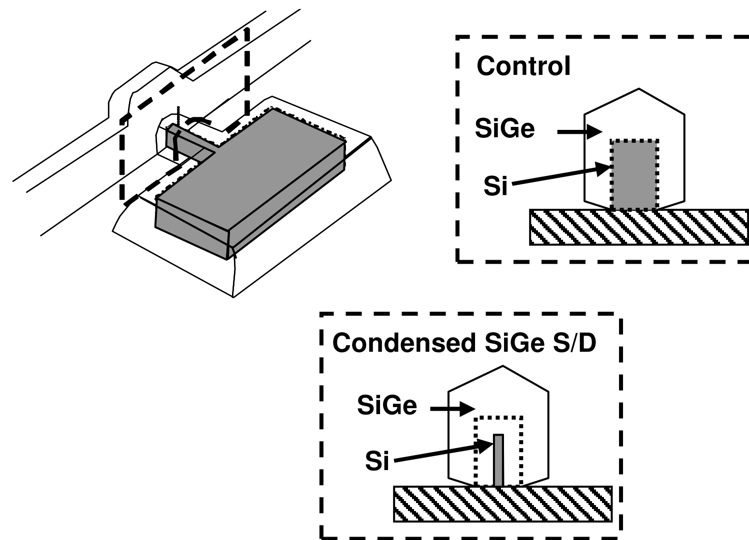


Figure 5-1 Schematic of device structures fabricated in this work showing the selectively grown SiGe on the S/D regions. The schematic also shows the difference in the Ge distribution in the fin at the S/D region for a control FinFET and a FinFET with condensed SiGe S/D. Si region is shown in grey and SiGe region is shown in white.

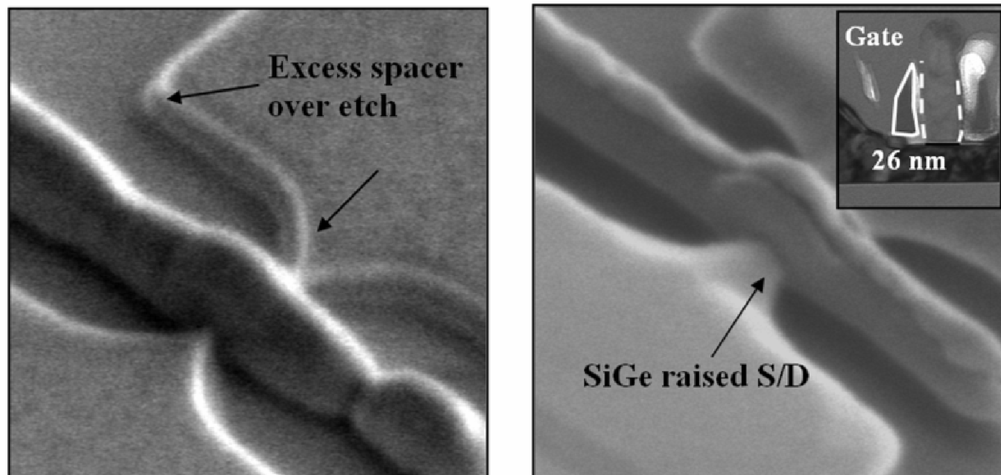


Figure 5-2 (a) SEM images of the FinFET structure after SiN spacer etch. An excessive over-etch step was used for the removal of spacer stringers (b) SEM image of FinFET with SiGe S/D after Ge condensation and oxide removal. The inset shows the TEM image of the gate stack, having a gate length of 26 nm.

The effect of Ge condensation on fin structures was also studied by first growing $Si_{0.75}Ge_{0.25}$ on the fin test structures. Figure 5-3(a) shows the TEM image of the fin after the epitaxy process. The inset of Figure 5-3(a) shows the diffractogram image taken at the SiGe layer, showing the good crystalline quality. From Figure 5-3(a), it can be observed that the thickness of SiGe is larger at the top when compared to the sidewalls indicating a higher growth rate for the (100) surface orientation as compared to the (110) surface. Similar findings were also reported by Sugiyama *et al* [5.9]. A longer growth time will therefore be needed to grow the SiGe at the sidewall for the FinFET structure for a targeted thickness as compare to a planar device. Ge condensation was performed on this structure at 950°C for 20 min and Figure 5-3(b) shows the TEM image of the fin after the condensation process. In Figure 5-3(b), it is observed that the Ge has diffused into the Si fin from all the three sides, creating a SiGe profile that is similar to an epi-grown SiGe layer on an isotropically recess-

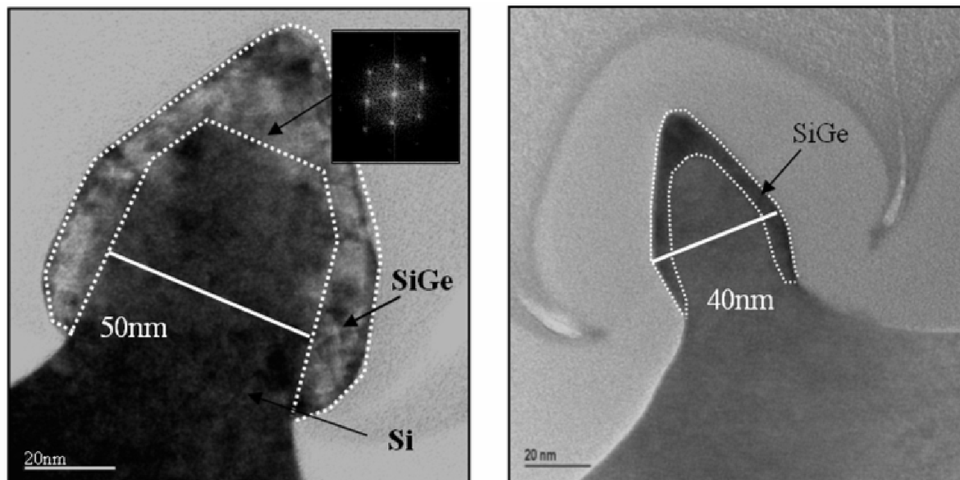


Figure 5-3 (a) TEM image of a fin structure with SiGe grown on the top (100) and the sidewall (110) surfaces. (b) Ge diffuses into the fin after condensation at $950^0$C for 20 min in an oxygen ambient as indicated by the reduction of Si fin width.

etched fin. An embedded SiGe at the S/D region of the fin is thus created, eliminating the need for a recess etch that will become increasingly challenging as the fin width becomes smaller. Even if the isotropic recess etch can be achieved, Si migration may also become a problem for such thin Si fins during the SiGe epitaxy process [5.10], [5.11]. The oxidation of SiGe in the (110) surface orientation is also observed to be faster when compared to the (100) surface orientation. By optimizing the process and the dimensions of the fin, it is also possible to achieve a higher Ge concentration at the S/D regions due to the piling up of Ge atoms [5.4], [5.12], thereby enhancing the effect of strain further.

Three-dimensional stress simulation was performed using Taurus Process simulator. The simulation results are summarized in Figure 5-4. Comparison was made between a FinFET with SiGe S/D structure having a 5 nm recessed profile on both the sides and top of the fin to a FinFET with epitaxial SiGe grown on un-

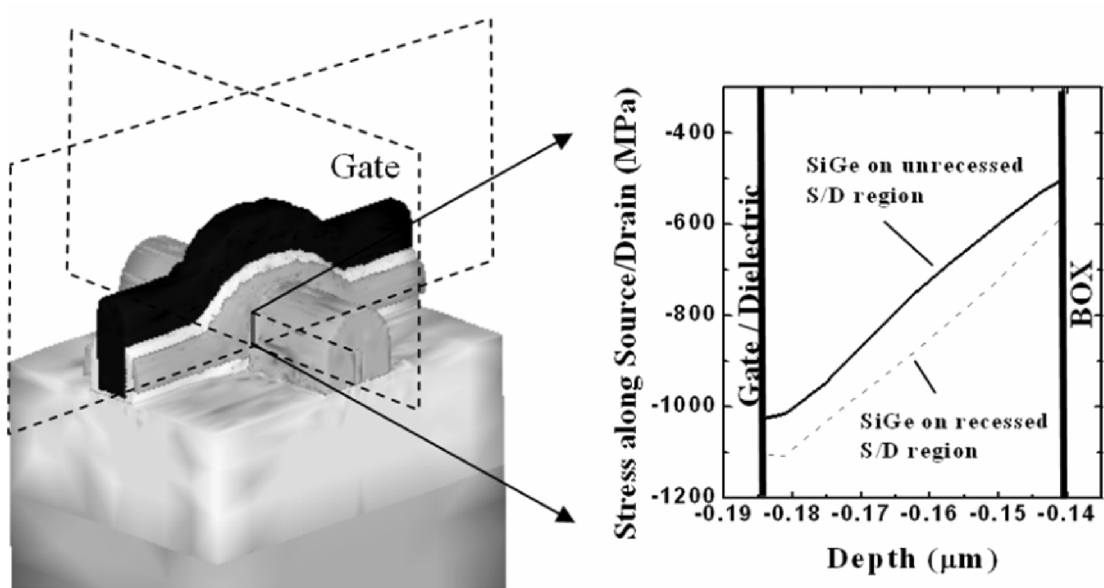


Figure 5-4 Stress simulation for FinFET (fin width = 20 nm) with recessed profile shows a larger compressive strain.

recessed S/D regions. The former structure simulates the stress effect for the FinFET device that undergoes an additional Ge condensation step (FinFET with embedded SiGe S/D) while the latter simulates the control device (FinFET with non-embedded SiGe S/D). The compressive stress along the S/D direction at the center of the channel is found to be larger for the FinFET having an embedded SiGe S/D. For both types of FinFET structures, the magnitude of compressive stress decreases from the top to bottom of the fin. The average stress of the FinFET with embedded SiGe S/D is consistently larger than that of the control. Hence, higher performance can be expected for the FinFET with embedded SiGe S/D.

## 5.3 Device Characterization

Figure 5-5(a) shows the $I_D$- $V_G$ characteristics of a FinFET with a condensed SiGe S/D and the control device. The FinFET with condensed SiGe S/D ($L_G$ = 26 nm) shows a subthreshold swing of ~100 mV/decade and drain induced barrier lowering

(DIBL) of 0.13 V/V. It can also be observed that the additional condensation step does not degrade the performance of the FinFET. The difference in DIBL between the control and the FinFET with condensed SiGe S/D maybe attributed to the control device having a smaller effective length due to process differences. The $I_D$-$V_D$ characteristics of the devices are plotted in Figure 5-5(b) at various gate overdrives. At ($V_G$ - $V_t$) of -1.2 V, the FinFET with condensed SiGe S/D shows a 28% higher $I_{Dsat}$ than the control device. This is possibly attributed to a recessed Ge profile and an increased Ge concentration for larger strain effects.

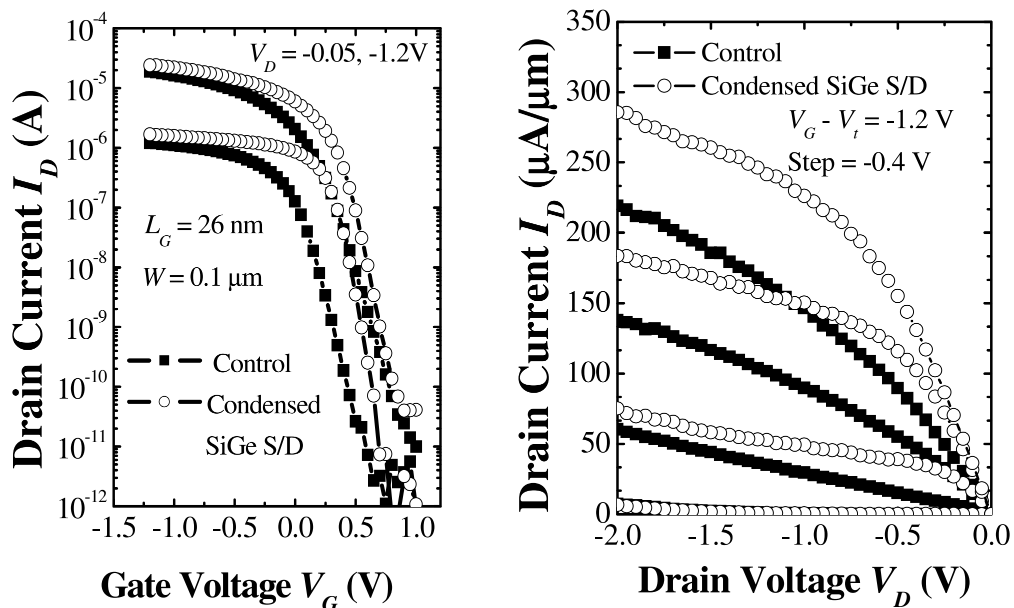


Figure 5-5 (a) $I_D$-$V_G$ characteristics of FinFET devices having an $L_G$ of 26nm. (b) $I_D$-$V_D$ characteristics of FinFET devices at various gate overdrives ($V_G$-$V_t$). FinFET with condensed SiGe S/D shows a higher drive current.

FinFET with condensed SiGe S/D also shows a larger peak tranconductance than the control device as shown in Figure 5-6, indicating a higher hole mobility which can be attributed to the enhanced strain effect. As shown in Figure 5-7, the two devices have comparable source/drain series resistances. This can be deduced from the plot of the total channel resistance $R_{tot}$ as a function of gate voltage. At large $|V_G|$, it is assumed that the channel resistance is much smaller than the series resistance. This is evident from the asymptotic behavior of the curve, which tends towards the source/drain series resistance at large $|V_G|$.

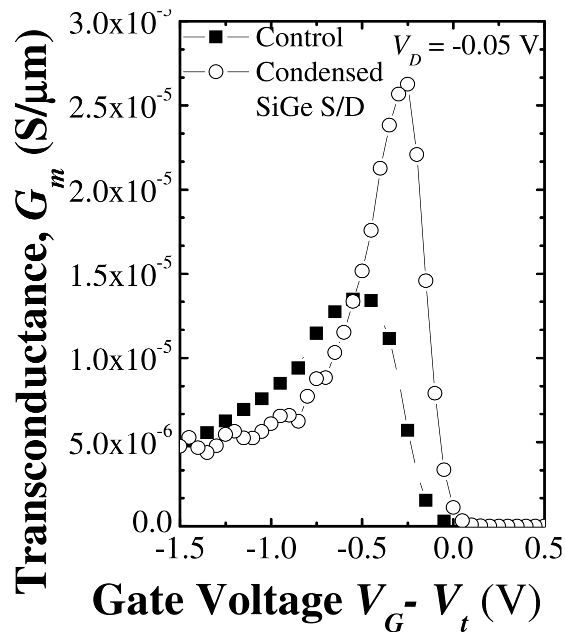


Figure 5-6 Comparison of transconductance $G_m$ at the same gate overdrive, illustrating an enhancement of 91% for the FinFET with condensed SiGe S/D over the control device.

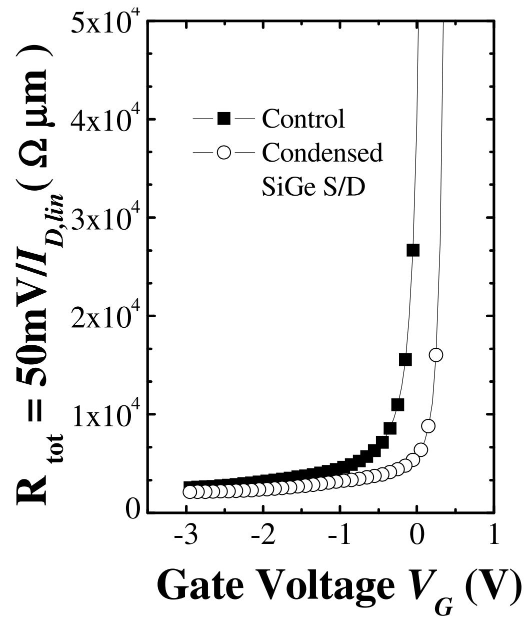


Figure 5-7 Extraction of series resistance by examining the the total resistance, which asymptotically approaches the value of the S/D series resistance at large gate bias.

## 5.4 Summary

P-channel FinFETs with condensed SiGe S/D regions were demonstrated for the first time, with gate lengths down to 26 nm. 28% drive current enhancement was observed in comparison with a FinFET with an uncondensed SiGe S/D. The Ge condensation process leads to a more recessed Ge profile in the S/D regions and possibly higher Ge concentration, both of which give rise to higher uniaxially compressive channel strain for hole mobility enhancement. A FinFET with embedded SiGe S/D stressor can therefore be fabricated without the use of an isotropic recess etch process that becomes increasingly challenging as fin dimensions scale down.

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# Chapter 6

# 6. Multiple-gate UTB and Nanowire-FETs with Ge S/D stressors

## 6.1 Introduction

In strain-engineered p-channel transistors, SiGe S/D stressors have been exploited to induce uniaxial compressive channel stress, improve hole mobility, and enhance $I_{Dsat}$ performance. There have been several reports on integrating embedded SiGe stressors (with low Ge %) in multiple-gate transistors [6.1]- [6.4]. In Chapter 5, the fabrication and characterization of FinFETs with a novel condensed SiGe S/D stressor were described. However, in the most advanced devices with extremely thin EOT, the relatively high thermal budget required for Ge condensation makes it less attractive.

Integrating embedded SiGe stressors with UTB SOI planar or even nanowire FETs is extremely challenging, since there is very limited margin for S/D recess etch prior to SiGe epitaxy. To further exacerbate the problem, as body thickness is reduced, lattice strain coupling from the S/D stressors is also expected to decrease [6.2]. A viable way of boosting the channel strain is to increase the Ge concentration of the SiGe S/D stressors. Although this approach is somewhat intuitive, actual successful implementation is not easy due to epitaxial growth and defect control issues [6.5]. In this section, we demonstrate the scaling up of Ge concentration to the limit, by employing epitaxially grown pure germanium S/D stressors in UTB-FETs

and nanowire FETs. No successful attempt has ever been reported on forming Ge S/D stressors in nanowire-FETs or UTB-FETs.

Additionally, it has been reported that in thin silicon structures, large amounts of strain energy can be elastically accommodated due to the effect of substrate compliance [6.6],[6.7]. Since the lattice mismatch between Ge and Si is large (4.2%), dislocation-mediated strain relaxation will occur even with thin Ge stressor films. We show that the substrate compliance effect can be exploited to suppress dislocation-mediated strain relaxation, thus maximizing the lattice strain induced in the channel regions. As a result, even higher performance enhancement can be obtained with Ge S/D stressors.

## 6.2 Device Fabrication

P-channel multiple-gate UTB-FETs were fabricated on 10 nm SOI with (100) surface orientation. Figure 6-1a process flow schematic which summarizes the key fabrication steps. A gate stack comprising 30Å of $SiO_2$ and p+ polysilicon was used. Gate lengths down to less than 10 nm were defined by an optimized gate etch process which results in bottom-tapered gates, making the gate length at the bottom of the gate the smallest. The UTB-FETs have device widths ranging between 30 nm to 80 nm. The smaller width devices are effectively quasi-nanowire FETs. Both the UTB and nanowire channels were formed by trimming of the patterned photoresist mask, hard mask before Si etch. No oxidation was performed to further shrink the dimensions. The nanowires are 30 nm wide and 8 nm tall. Following extension implants and spacer formation, selective epitaxial growth of either Si or Ge was performed in an ultra-high vacuum chemical vapor deposition (UHVCVD) epitaxy

reactor. Following Si epitaxial growth, nickel silicidation (~6nm) was performed to reduce series resistances for the control device (“Si S/D”). For the strained devices, pure Ge was grown selectively in the S/D regions to form the lattice-mismatched S/D stressors. Ge growth on Si follows the Stranski-Krastanov growth mode, in which a two-dimensional growth transitions to three-dimensional growth beyond a certain critical thickness. The growth passes through an intermediate hut cluster phase, which subsequently leads to the formation of macroscopic Ge islands [6.8]. Obviously, Ge films with such surface morphology are unsuitable for CMOS applications. By growing Ge at sufficiently low temperatures in the epitaxy reactor, three-dimensional growth was suppressed, allowing Ge S/D stressors of good morphology to be grown [Figure 6-2(a) and 1(b)]. This can possibly be attributed to the un-desorbed hydrogen acting as a surfactant, similar to that reported in [6.9], and to reduced atomic surface migration lengths at low temperatures [6.10]. Two stressor thicknesses of 33 and 66 nm were grown on two wafers, forming the splits of “Thin Ge S/D stressors” and “Thick Ge S/D stressors” respectively. Germanidation of the strained Ge S/D devices was skipped for process simplicity and to maintain the as-grown Ge stressor thicknesses. All splits then received $BF_2^+$ and $B^+$ S/D implants which were targeted to distribute the dopants throughout the raised S/D regions. After depositing a $SiO_2$ capping layer, dopants were activated using rapid thermal annealing (RTA) at 900°C for 10s. This was followed by $SiO_2$ passivation, contact formation and metallization.

- Active-patterning (10nm SOI)
- Gate stack formation:
  p+ Poly-Si / $SiO_2$ (30Å)
- SDE implant
- SiN Spacer formation
- Selective Epi for Raised-SD
  1. Ge S/D (thick or thin)
  2. Si S/D (control)
- HDD implant
- $SiO_2$ capping
- RTA activation
- Ni silicidation for Si control
- Contact and metallization

Figure 6-1 Process flow schematic which summarizes key steps in the device fabrication process.

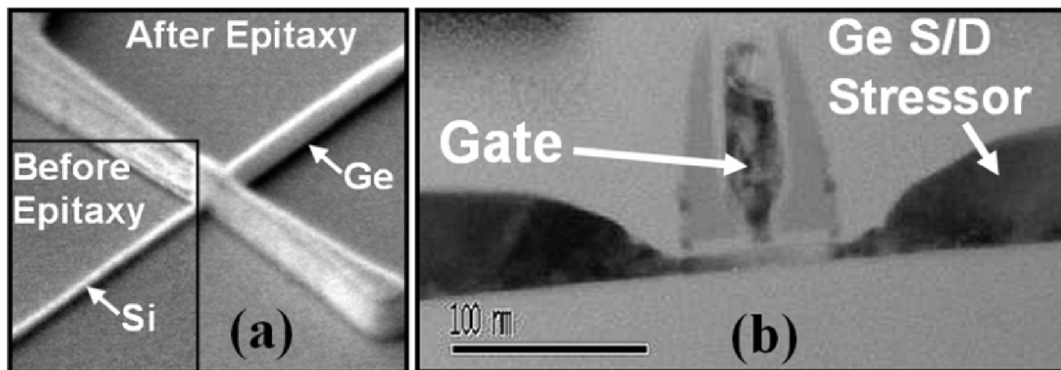


Figure 6-2 (a) SEM images taken at a 45° tilt, showing the S/D regions of a nanowire-FET before and after Ge epitaxial growth. Excellent selectivity is achieved (b) TEM image showing a cross-section of the gate structure and Ge S/D stressors.

## 6.3 Device Characterization

To investigate the effect of substrate compliance in narrow width SOI structures, TEM analysis of Ge stressor films grown on structures with different line widths was performed. It is observed that the dislocation density in the wide structure shown in Figure 6-3(a) is much higher compared to that in the narrow structure shown in Figure 6-3(b). This concurs with the observations reported in [6.6]. Additionally, there also seems to be a small degree of buckling/bending in the ultra-thin SOI. Similar

buckling/bending behavior has been reported in [6.11], which has been attributed to the reduced viscosity of the underlying buried $SiO_2$ under large amounts of shear stress. In [6.11], it is particularly interesting that the strain relaxation in the Ge "nano-stressor" is completely elastic. This suggests that, under the right conditions, Ge stressors grown on ultra-thin SOI can possibly relax, straining the underlying silicon highly, without the formation of dislocations. It is postulated from these observations, firstly, that ultra-thin SOI substrates can have enhanced compliance effects when subjected to large amounts of stress from Ge stressors, and secondly, that narrow patterns show further enhanced width-dependent compliance. One can thus expect a large strain to develop in the channel regions of UTB-FETs with Ge S/D stressors, since the SOI in the S/D regions are easily strained by the Ge stressors. One can further expect narrow width (nanowire) devices to exhibit even greater levels of channel strain as a result of increased width-dependent compliance.

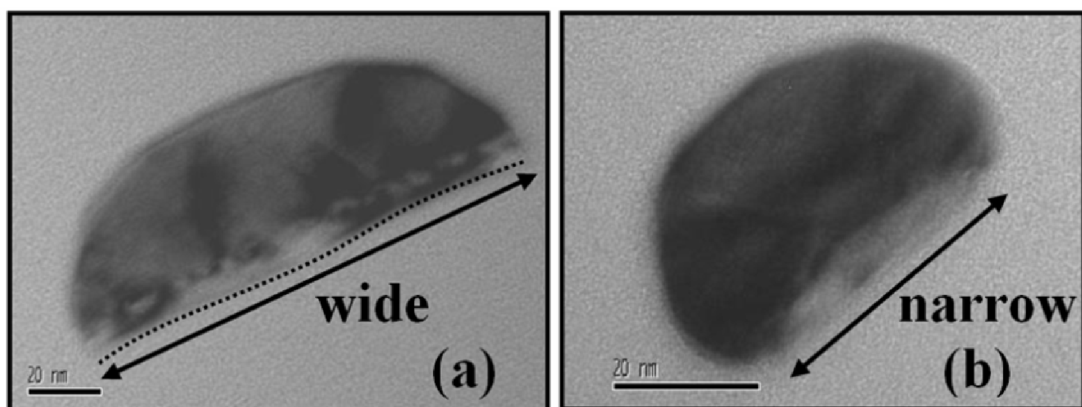


Figure 6-3 TEM images of Ge grown on ultra-thin SOI showing (a) a wide active region with multiple dislocations at the Ge-Si interface, and (b) a narrow active region with a greatly reduced dislocation density.

Figure 6-4 shows the $I_{Off}$-$I_{On}$ plot for devices with Thin and Thick Ge S/D stressors, compared to the Si S/D control devices. These are quasi-planar UTB devices with a device width of 80 nm. At a fixed $I_{Off}$ of $1\times10^{-7}$A/μm, 39% and 80% $I_{Dsat}$ enhancement was obtained for devices with Thin and Thick Ge S/D stressors, respectively. Such pronounced $I_{Dsat}$ enhancement can be linked to the large compressive stress that Ge S/D stressors exert on the channel, which results in significant hole mobility enhancement. This hole mobility enhancement has typically been attributed to a reduced conductivity hole effective mass, which comes as a result of uniaxial compressive strain lifting degeneracy in the valence band, as well as sub-band shape deformation and shifting [6.12], [6.13]. Figure 6-5 plots the peak of the transconductance $G_m$ against DIBL. $G_m$ is enhancement is closely related to mobility enhancement, and is also less sensitive to series resistance differences. Since DIBL is related to the effective channel length, which is itself related to the physical gate length, this plot essentially shows the dependence of $G_m$ against physical gate length. It is observed that $G_m$ enhancement increases with increasing values of DIBL. This means that as gate lengths are scaled down, the strain induced mobility enhancement increases due to the local nature of the S/D stressors, and is consistent with that reported in [6.14] for embedded SiGe S/D devices.

Figure 6-6 summarizes the $I_{Dsat}$ enhancement obtained for different device widths, for devices with both Thin and Thick Ge S/D stressors. It is clear that $I_{Dsat}$ enhancement increases with decreasing device width. This is consistent with the TEM observations made earlier of increased substrate compliance effects in narrow ultra-thin SOI patterns. An interesting point to note is that for 30 nm wide devices (quasi-nanowire FETs), employing Thin Ge S/D stressors is already sufficient to achieve

77% $I_{Dsat}$ enhancement, which is close to that obtained with Thick Ge S/D stressors (96%). This is very significant, considering that the thin stressor is only half the thickness of the thick stressor. These results imply that extremely scaled nanowire-FETs may only require very thin Ge stressor films to obtain large gains in performance.

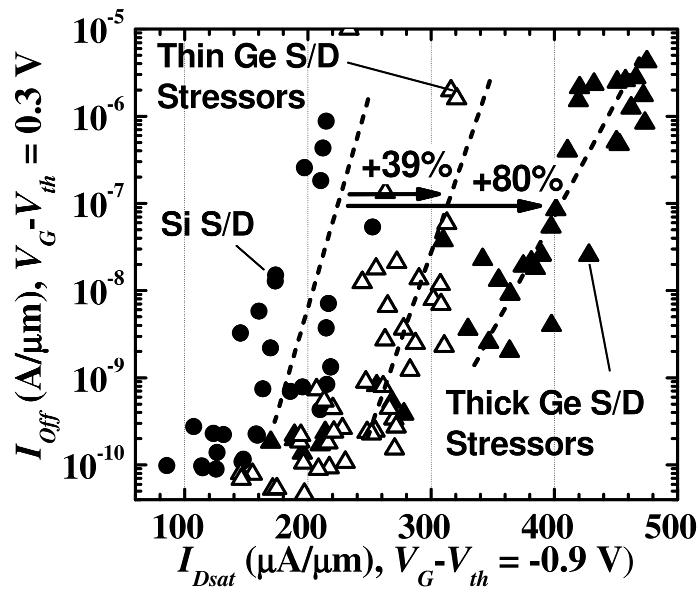


Figure 6-4 Thin and Thick Ge S/D stressors result in 39% and 80% $I_{Dsat}$ enhancement, respectively, at a fixed $I_{Off}$ of $1\times10^{-7}$ A/µm. ($W$ = 80 nm)

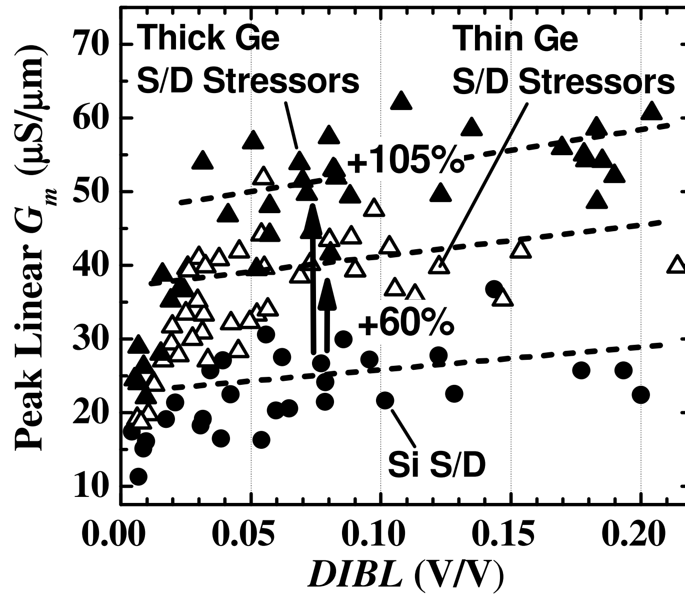


Figure 6-5 Hole mobility is very significantly enhanced by large compressive stress due to Ge S/D stressors. Peak transconductance is increased by 60% and 105%, respectively, at a DIBL of 75 mV/V.

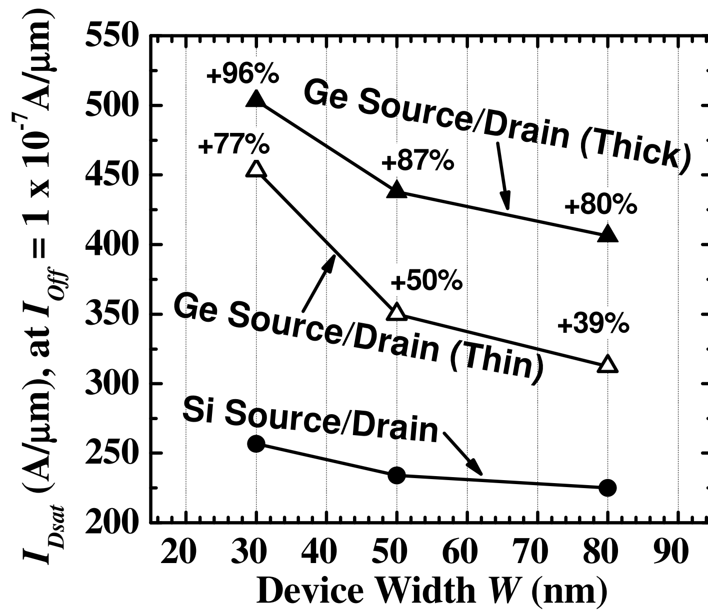


Figure 6-6 $I_{Dsat}$ enhancement (indicated in %) for 2 different Ge S/D stressor thicknesses, compared to a control with raised Si S/D. UTB-FETs with small width $W$ have larger enhancement. For $W$ of 30 nm, $I_{Dsat}$ enhancement due to Thin Ge S/D stressor approaches that of Thick Ge S/D stressor.

## 6.4 Melt-enhanced Dopant Diffusion and Activation Technique for Ge S/D Stressors

### 6.4.1 Introduction

For multiple-gate devices with raised S/D regions, it is desirable to uniformly dope the epitaxially grown S/D regions. This ensures low resistivity paths from the contact silicide to the S/D extension regions. The topology of multiple-gate devices with raised S/D regions can also make it challenging to dope the raised S/D regions using ion implantation. One method of accomplishing this is to employ in-situ doping of the film during the epitaxial growth process. This was experimentally done and described in Section 3.4, where Phosphorus in-situ doped $Si_{1-y}C_y$ films were integrated with FinFETs. In this section, an alternative technique of uniformly doping of the raised Ge S/D regions in devices with Ge S/D stressors (which were described earlier in Section 6.2) is proposed and experimentally demonstrated. The technique involves doping the surface of the Ge S/D regions heavily using low energy ion implantation, and then selectively melting the Ge to uniformly distribute and activate the dopants in the Ge S/D regions. This technique is named Melt-Enhanced Dopant (MeltED) diffusion and activation technique. The technique also has the further advantage of simultaneously embedding the Ge S/D regions for enhanced lattice strain coupling from the stressors to the channel [6.3].

### 6.4.2 Devices with MeltED Ge S/D Stressors

Key steps for forming MeltED or embedded Ge S/D stressors are shown in Figure 6-7. When Ge is melted at temperatures exceeding 938˚C, extremely fast liquid-state diffusion of dopants allow for rapid and uniform distribution of dopants throughout

the Ge S/D stressor. During this process, Si and Ge inter-diffusion also occurs at the heterointerface, resulting in "embedding" of the Ge stressor for improved channel stress coupling effects. Figure 6-8 shows the sheet resistance values of films with 2 different Ge thicknesses. The films were doped near the surface with low energy 5keV $BF_2^+$ implantation of identical dose. After capping and undergoing the MeltED anneal, the sheet resistances were measured and plotted with calculated resistivity values in Figure 6-8. The identical resistivity values clearly indicate uniform distribution and incorporation of B in Ge. Hence, the results prove that this technique can facilitate uniform dopant diffusion and incorporation regardless of Ge thickness or S/D geometries.

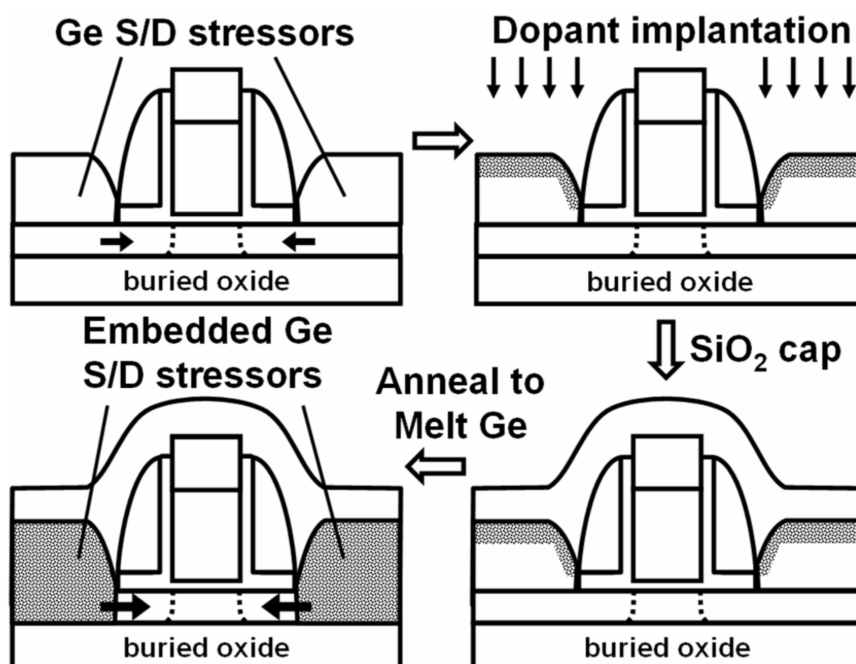


Figure 6-7 New Melt-Enhanced Dopant (MeltED) diffusion and activation process. After shallow S/D implant and $SiO_2$ capping, a 950°C spike anneal melts the Ge-rich region, and achieves these key objectives: Interface inter-diffusion *embeds* the Ge stressor; Dopant diffuses, redistributes uniformly, and is substitutionally incorporated as Ge recrystallizes.

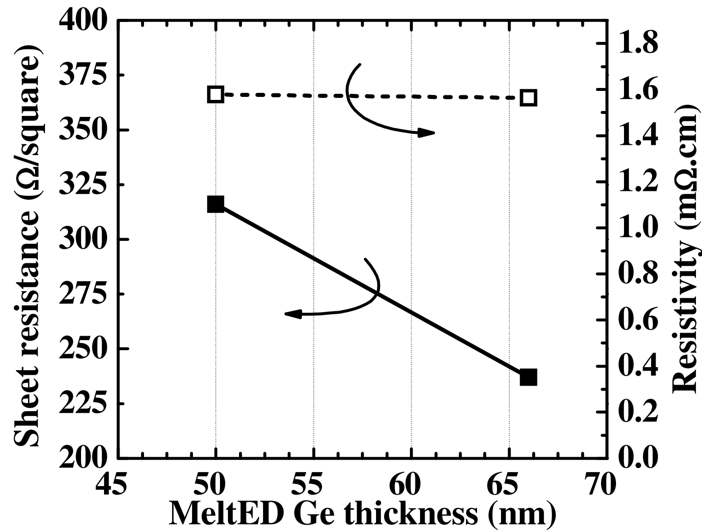


Figure 6-8 Sheet resistance (4 point probe measurements) of MeltED Ge with 2 thicknesses. Both received surface $BF_2^+$ implants only. Both films have near identical resistivity values, which confirms that Boron is uniformly diffused in the liquid Ge and is substitutionally incorporated as Ge re-crystallizes.

### 6.4.3 Device Characterization of MeltED Ge S/D devices

Compared to Ge S/D devices without Ge melting, devices with MeltED or embedded Ge S/D exhibit a further 10% $I_{Dsat}$ enhancement (Figure 6-9) as well as a further 15% peak $G_m$ improvement (Figure 6-11). Since MeltED Ge S/D devices employ a slightly higher activation thermal budget, one might question if the enhancement is simply due to a decrease in effective channel lengths or S/D series resistances. Figure 6-11 plots the cumulative distributions of SS, $R_{tot}$, and $G_{m,max}$ for 2 sets of devices with similar mask gate lengths. It is quite clear that non-melted Ge and MeltED Ge devices have comparable short channel control and S/D series resistances (estimated from $R_{tot}$ at high gate overdrive). $I_D$-$V_G$ characteristics in Figure 6-12 show comparable SS and DIBL between a MeltED Ge S/D and a Si S/D control device. $G_m$ is clearly enhanced by ~22%. The MeltED Ge S/D device shows a dramatic 120% $I_{Dsat}$ enhancement over the Si S/D control device (Figure 6-13). On average, the $I_{Dsat}$

enhancement at an $I_{Off}$ of $1 \times 10^{-7}$ A/µm obtained with the MeltED Ge technique is close to 100%.

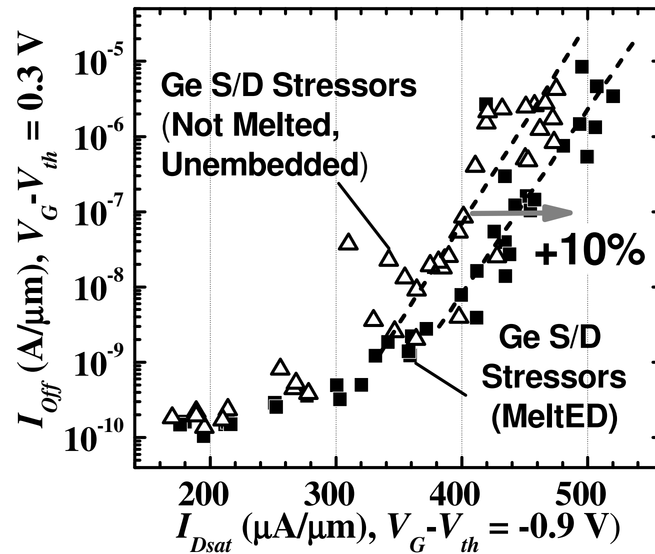


Figure 6-9 MeltED Ge S/D stressors are embedded, and gives a further 10% $I_{Dsat}$ enhancement at $I_{Off}$ of $1 \times 10^{-7}$A/µm, as compared to the unembedded Ge S/D stressors (also plotted in Fig. 4). Greater strain effects come with S/D stressor embedding.

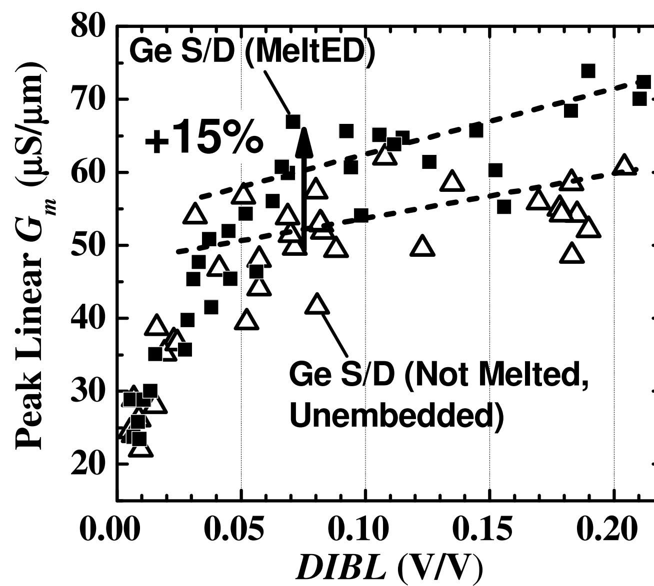


Figure 6-10 An additional 15% enhancement in peak transconductance was obtained at a DIBL of 75 mV/V as a result of increased channel strain.

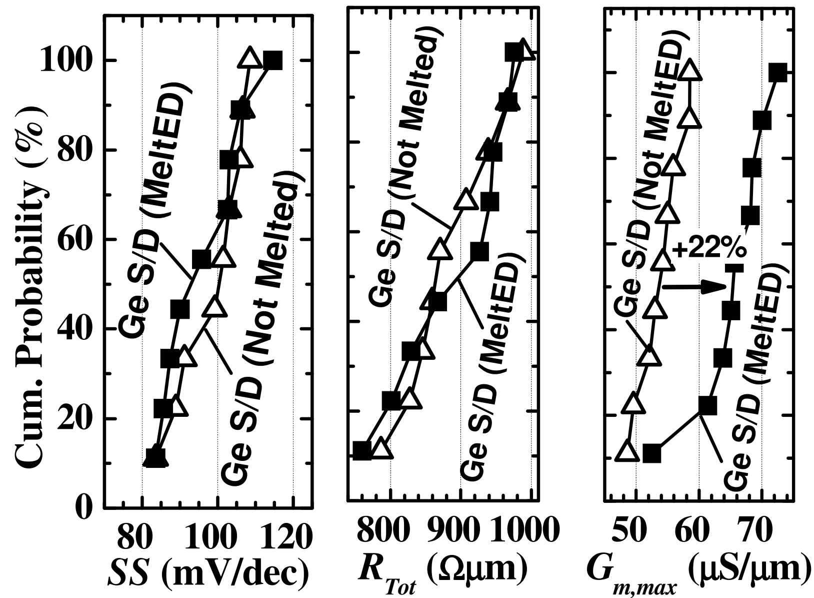


Figure 6-11 P-FETs with MeltED/Embedded Ge S/D have 22% higher $G_{m,max}$ than those with unembedded Ge S/D (not melted). All p-FETs have the same short channel control and $L_G$ (35nm). $R_{Tot}$ at high gate overdrive ($V_G$-$V_{th}$ = 2.5V) estimates $R_{SD}$ to be comparable.

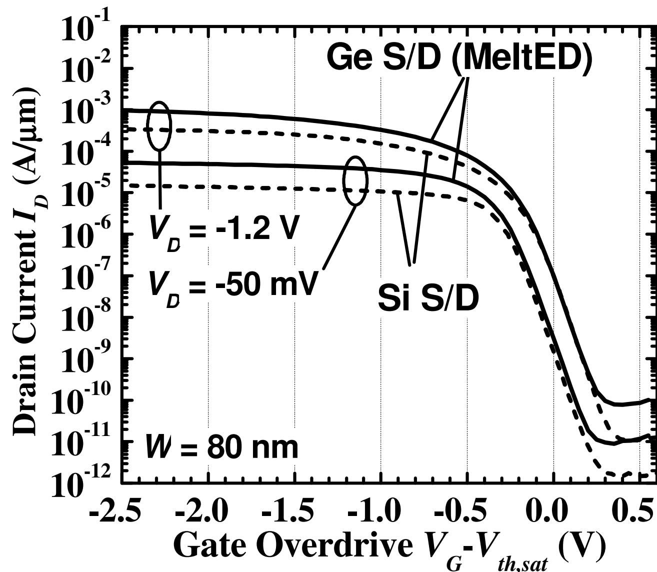


Figure 6-12 $I_D$-$V_G$ plot showing comparable DIBL and SS for a p-FET with Raised Si Control and a p-FET with Embedded Ge S/D (MeltED).

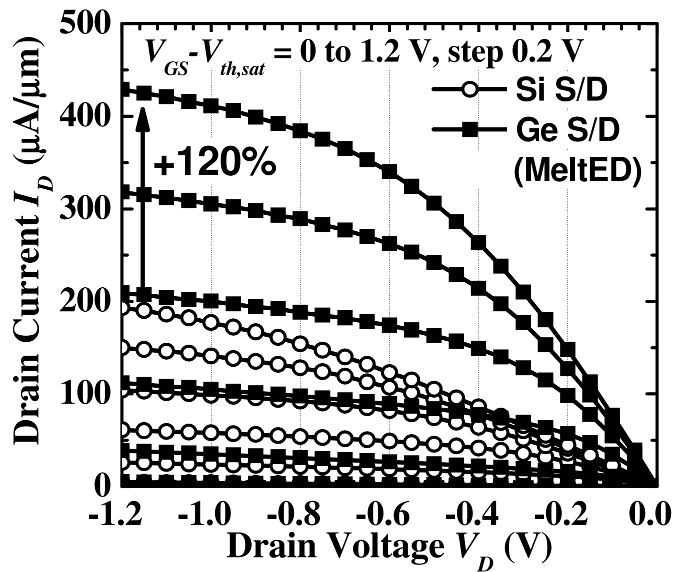


Figure 6-13 $I_D$-$V_D$ plot of same pair of devices in Fig. 14. Embedded Ge S/D (MeltED) gives a 120% $I_{Dsat}$ enhancement over a p-FET with Si S/D.

Since the lattice mismatch between Ge and Si is 4.2%, the substrate compliance effect of narrow and thin SOI lines may not be able to completely suppress the formation of dislocations. It is important that such defects are formed outside the S/D depletion regions during transistor operation. Figure 6-14 compares the junction leakage currents of Si Control, non-melted Ge S/D and MeltED Ge S/D devices. It is found that the leakage currents are quite comparable and are of a low magnitude.

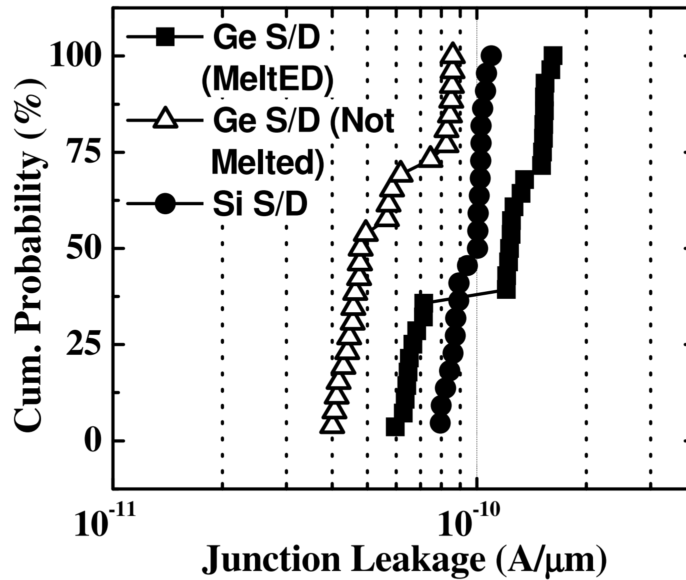


Figure 6-14 Ge S/D stressors does not significantly impact junction leakage, indicating that defects are well-confined outside the extension regions. The abrupt change observed in the junction leakage distribution of Ge S/D (MeltED) devices at about 40% could be coincidental due to the small sample size. A larger sample size should yield a more gradual distribution.

Energy dispersive spectrometry (EDS) of a MeltED Ge S/D nanowire's S/D reveals uniform ~85% Ge concentration as shown in Figure 6-15. It is postulated that as Ge melts, Si also dissolves in the molten Ge. In a Si/Ge core/shell nanowire S/D region, the small volume of Si can completely dissolve in the relatively much larger surrounding volume of molten Ge, leading to the formation of a uniform SiGe alloy upon re-crystallization. In this case, the seed for re-crystallization is located underneath the gate spacers. As a result, fully embedded Ge-rich SiGe stressors are formed in the S/D regions of nanowire devices. $I_D$-$V_G$ transfer characteristics in Figure 6-16 show comparable SS and DIBL for MeltED Ge and non-melted Ge S/D nanowire devices. Such embedded stressors result in a further 16% $I_{Dsat}$ enhancement in the MeltED Ge S/D nanowire device, improving its drive current to 609 μA/μm

(Figure 6-17). Note that such performance levels were achieved without S/D metallization.

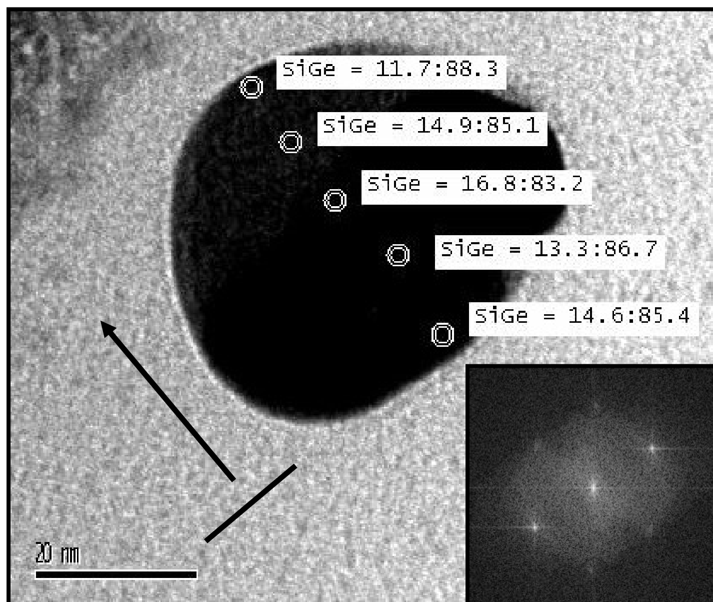


Figure 6-15 EDS analysis of MeltED Ge nanowire S/D shows uniform ~85% Ge concentration from top to bottom. Reciprocal space diffractogram (inset) shows single crystallinity.

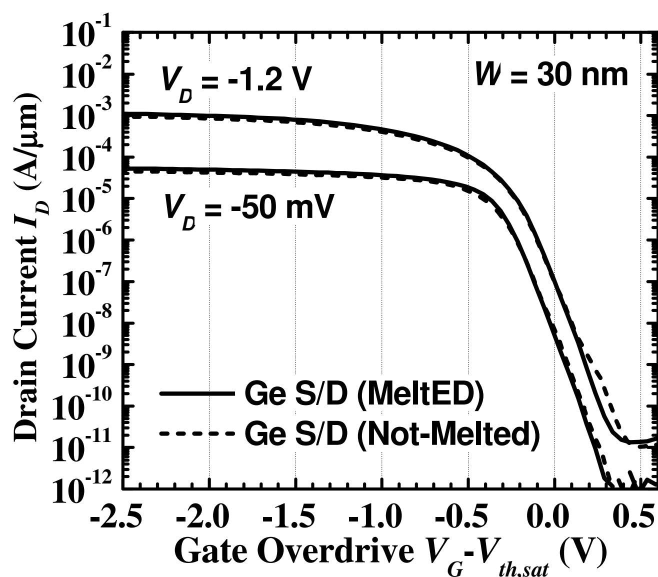


Figure 6-16 $I_D$-$V_G$ transfer characteristics showing a pair of nanowire p-FETs with Ge S/D with comparable DIBL and SS.

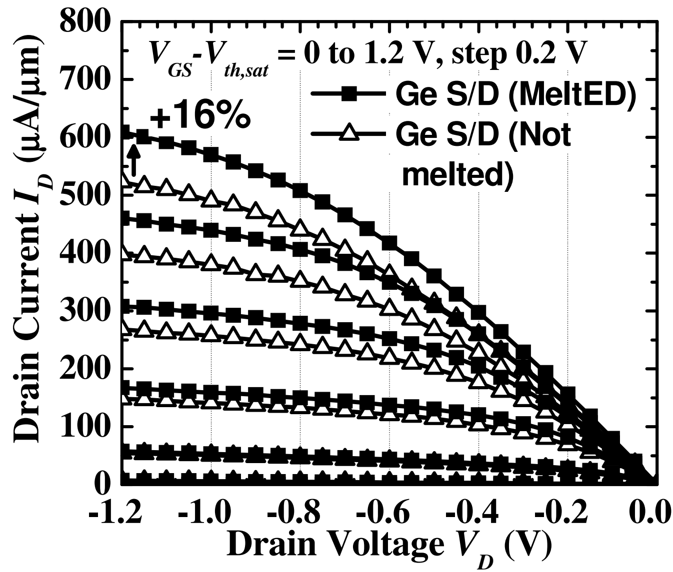


Figure 6-17 $I_D$-$V_D$ plot of same pair of Nanowire p-FETs in Fig. 18. Embedded Ge S/D (MeltED) shows a further 16% $I_{Dsat}$ enhancement over unembedded Ge S/D.

## 6.5 Summary

Large $I_{Dsat}$ performance enhancement has been obtained in p-channel UTB-FETs and nanowire-FETs by incorporating Ge S/D stressors in the S/D regions as stressors. Width-dependent substrate compliance effects in ultra-thin SOI result in increasing effectiveness of Ge S/D stressors in straining the channel. By employing a Ge melting technique, dopant activation and stressor embedding was accomplished in a single process step, achieving $I_{Dsat}$ enhancement of ~100% and ~125% for planar UTB-FETs and nanowire-FETs respectively. Strain technology incorporating Ge S/D stressors are expected to become important building blocks for realizing extremely scaled high performance p-channel SOI FETs.

## 6.6 References


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two-step recessed SiGe-S/D and stress liner technology," in *VLSI Tech. Dig.*, 2007, pp. 48-49.

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# Chapter 7

# 7. Conclusions and Future Work

## 7.1 Conclusions

Process-induced strain techniques revolving around lattice-mismatched S/D stressors have been proposed and experimentally explored for nanoscale multiple-gate transistors. Techniques involving SiC and SiGe S/D stressors have been studied for n and p-channel transistors, respectively.

### 7.1.1 Silicon Carbon ($Si_{1-y}C_y$) Source and Drain Technology for N-Channel Multiple-Gate FETs

SiC S/D stressors have proven to be effective for inducing uniaxial tensile strain and enhancing the performance of n-channel multiple-gate transistors significantly. For n-channel multiple-gate transistors, it has been shown that up to 20% enhancement in $I_{Dsat}$ can be obtained with (100)-sidewall FinFETs using implantation doped SiC S/D stressors. (110)-sidewall FinFETs proved to be less sensitive to the longitudinal tensile channel strain, achieving 7% $I_{Dsat}$ enhancement. By adding a high stress SiN liner, the additional vertical compressive stress exerted on the (110)-sidewall channels boosts the electron mobility significantly. As a result, the $I_{Dsat}$ enhancement of both (100)-sidewall and (110)-sidewall FinFETs with combined SiC S/D and liner stressors exceed 50%, clearly showing the compatibility of SiC S/D stressors with the high stress SiN liner stressor.

It was also shown that enhancement in $I_{Dsat}$ performance can also be obtained by scaling geometrical parameters such as SiC stressor thickness and spacer widths in the strained devices. Naturally, it is desirable that simple geometrical scaling can provide an additional avenue for increasing channel stress. However, it should also be noted that variability in the control of geometric parameters such as spacer widths, stressors thicknesses or fin widths could result in increased variability in channel electron mobility. This could in turn adversely affect $I_{Dsat}$ variability. As such, more stringent process uniformity control requirements may be needed for key processes in such strained devices.

### 7.1.2 Novel Techniques for Further Improving N-Channel Multiple-Gate FETs with Silicon Carbon ($Si_{1-y}C_y$) Source and Drain Technology

Focusing on extending the performance of strained multiple-gate transistors with SiC S/D stressors, it was found that the strain induced in the channel can be further increased using several techniques as described in Chapter 3. In particular, a spacer removal technique increases the influence of the SiC S/D stressors, effectively improving the lattice-strain coupling from the S/D stressors to the channel. A further 10% enhancement in $I_{Dsat}$ can be obtained with this spacer removal technique. It was also established that the enhancement is likely to increase as gate lengths are scaled down. This technique is very attractive due to its simplicity, low cost and its applicability at future technology generations.

A high-stress contact silicide (+1 GPa) was also developed for the SiC S/D regions of multiple-gate transistors. The results indicate that silicide-induced strain can be harnessed for synergistic strain effects in conjunction with SiC S/D stressors. It

was further shown that even higher performance can be obtained with FUSI metal gates in these devices.

It has also been shown that in-situ doped SiC films with even higher carbon substitutionality can be integrated with multiple-gate transistors. The carbon substitutionality is preserved in its as-grown state since a S/D dopant activation anneal is no longer required. This allows straightforward control of the desired amount of substitutional carbon by tuning the epitaxial process conditions, enabling scalability for future technology generations.

### 7.1.3 Germanium Condensation on SiGe Fin Structures: Ge enrichment and Substrate Compliance Effects

Germanium condensation enables the enrichment of Ge concentration not only in planar SiGe substrates, but also three-dimensional structures such as vertical fins. It has been shown that the Ge concentration in SiGe fins can be enriched up to ~90%. Theoretically, a Ge concentration approaching 100% can be achieved with an optimized process.

Substrate compliance effects reduce the dislocation density in narrow SiGe fin heterostructures formed using this method. This has the added benefit of reducing dislocation-mediated strain relaxation, which will especially be of benefit when such a technique is used to form Ge-rich channel or S/D regions. Ge condensation can be especially useful for embedding the SiGe stressors in the S/D regions of SOI ultra-thin body planar or multiple-gate transistors. This overcomes the limitations of the recess etch process, which would otherwise be necessary to embed the SiGe stressors in a conventional integration scheme. This technique was later applied to multiple-

gate transistors with SiGe S/D stressors in Chapter 5, successfully obtaining further performance enhancement in such devices.

### 7.1.4 P-Channel FinFETs with Embedded SiGe stressors Fabricated using Ge condensation

Ge condensation was used to simultaneously embed and enrich the Ge concentration in the S/D regions of p-channel FinFETs. The increased lattice-mismatch and proximity of the SiGe stressors to the channel gave rise to an increase in longitudinal compressive channel strain. This resulted in 28% $I_{Dsat}$ enhancement over the control without S/D Ge condensation.

### 7.1.5 Multiple-gate UTB and Nanowire-FETs with Ge S/D stressors

The successful integration of Ge S/D stressors with multiple-gate transistors have been demonstrated, exploiting the substrate compliance effects of ultra-thin SOI and narrow structures. By incorporating Ge S/D stressors in the S/D regions as stressors, very significant $I_{Dsat}$ performance enhancement has been obtained in p-channel UTB-FETs and nanowire-FETs, due to compressive channel strain. It was found that width-dependent substrate compliance, similar to that described earlier in Chapter 4, allowed greater channel strain to be developed in devices with narrower widths.

A novel Ge melting technique was proposed and experimentally shown to achieve dopant activation and stressor embedding in a single process step. Integration with devices with Ge S/D stressors resulted in $I_{Dsat}$ enhancement of ~100% and ~125% for planar UTB-FETs and nanowire-FETs respectively. This makes Ge S/D

stressor technology extremely attractive for extremely scaled multiple-gate devices in subsequent technology generations.

## 7.2 Future Work

It is desirable if the S/D stressors technologies identified and studied in this dissertation work can be integrated easily with other process-induced strain technologies for combined effects.

For n-channel multiple-gate transistors with SiC S/D stressors, it has been shown that further performance benefits can be obtained with additional stressors such as a high stress SiN liner, or a high-stress contact silicide. A possible area for future work is the integration of SiC S/D stressors with the Stress Memorization Technique (SMT), which is an important and manufacturable process-induced strain technique. Since a S/D amorphization implant is performed for SMT, carbon substitutionality may be adversely affected. Studies should thus be carried out to ascertain whether these two technologies can have synergistic effects. A possible approach can be the implantation of carbon, preferably into pre-amorphized S/D regions, putting down the SMT high stress layer, and then using non-equilibrium nanosecond-type anneals to re-crystallize the S/D regions.

With strain engineering and continued scaling, the S/D series resistances are becoming a very significant part of the total on-state resistance. It has been shown that the formation of high stress NiSi:C contacts significantly reduces the S/D series resistances. Nevertheless, the contact resistivity of NiSi:C to n+ $Si_{1-y}C_y$ is still quite

high due to the high electron barrier height (comparable to NiSi to n+ Si). With decreasing contact area in extremely scaled devices, it may be worthwhile to explore low barrier height silicide contacts to $Si_{1-y}C_y$. This can be in the form of rare-earth silicides or silicides formed from co-sputtered metals with Ni. Naturally, it would also be highly desirable if the new silicide film's instrinsic stress is also highly tensile.

For p-channel multiple-gate devices incorporating condensed SiGe S/D stressors, further work can be done to reduce the thermal budget needed for condensing the S/D regions. Ge condensation at lower temperatures using wet oxidation can be an option, since wet oxidation offers much faster oxidation rates than dry oxidation at a given temperature. However, this also requires optimization since too low an oxidation temperature would result in the non-selective oxidation of SiGe, thereby losing the condensation property.

For the p-channel multiple-gate devices incorporating Ge S/D stressors described in Chapter 6, further work can be done in the area of germanidation. Like in the case for n-channel devices, low contact resistivity necessitates a low (hole) barrier height between the germanide and p+ Ge. It would also be beneficial if the intrinsic stress in the germanide film is of a highly compressive nature.

Further work can also be done for the *MeltED* diffusion and activation technique to incorporate dopants in Ge S/D stressors. Although it has been proven that besides embedding the stressors, this technique enables uniform distribution and activation of B in the Ge S/D stressors, the resultant activation level of B in Ge is still not very high. As such, the resistivity of the Ge S/D stressor film can still be improved. Exploratory work can be performed using other p-type dopant such as Al and Ga. It is speculated that Al will yield better resistivity results than B, based on their relative

solid solubilities in Ge. In the case of incorporating Ga, the larger atomic radius of Ga can possibly result in an enlarged lattice constant for the resulting Ge:Ga alloy as compared to Ge:B. This could translate to even larger stress effects if Ga can be incorporated as a dopant in Ge.

Like in the case of n-channel devices, where a tensile SiN liner can help in inducing tensile channel strain, a compressive liner (SiN or other novel materials such as diamond-like carbon (DLC)) can also help in inducing compressive channel strain. Hence, it would also be of great benefit if compressive liners can be fully compatible with the Ge S/D stressors and have synergistic stressing properties. This area is also well-worth further efforts.

# Appendix A: Publication List

## Journal Publications

[1.] **T.-Y. Liow**, K.-M. Tan, Y.-C. Yeo, A. Agarwal, A. Du, C.-H. Tung, N. Balasubramanian, "Investigation of silicon-germanium fins fabricated using germanium condensation on vertical compliant structures," *Applied Physics Letters*, vol. 87, no. 26, 262104, Dec. 2005.

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[8.] **T.-Y. Liow**, K.-M. Tan, D. Weeks, R. T. P. Lee, M. Zhu, K.-M. Hoe, C.-H. Tung, M. Bauer, J. Spear, S. G. Thomas, G. S. Samudra, N. Balasubramanian, and Y.-C. Yeo, " Strained n-Channel FinFETs Featuring In-situ Doped Silicon-Carbon ($Si_{1-y}C_y$) Source and Drain Stressors with High Carbon Content," *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2475-2483, Sep. 2008.

[9.] **T.-Y. Liow**, K.-M. Tan, R. T. P. Lee, M. Zhu, B. L.-H. Tan, N. Balasubramanian, and Y.-C. Yeo, "Germanium source and drain stressors for ultra-thin-body and nanowire field-effect transistors," *IEEE Electron Device Letters*, vol. 29, no. 7, pp. 808-810, Jul. 2008.

[10.] **T.-Y. Liow**, K.-M. Tan, R. T. P. Lee, M. Zhu, B. L.-H. Tan, N. Balasubramanian, and Y.-C. Yeo, "Strained-silicon nanowire transistors with germanium source and drain stressors," *IEEE Trans. Electron Devices*, vol. 55, no. 11, 2008.

## Conference Publications

[11.] R. T. P. Lee, **T.-Y. Liow**, K.-M. Tan, K.-W. Ang, K.-J. Chui, G.-Q. Lo, D.-Z. Chi, and Y.-C. Yeo, "Process-Induced Strained P-MOSFET Featuring Nickel-Platinum Silicided Source/Drain," *Materials Research Society Symposium Proceedings*, San Francisco, CA, Apr. 17-21, 2006.

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[16.] R. T. P. Lee, **T.-Y. Liow**, K.-M. Tan, A. E.-J. Lim, C.-S. Ho, K.-M. Hoe, T. Osipowicz, G.-Q. Lo, G. Samudra, D.-Z. Chi, and Y.-C. Yeo, "Novel epitaxial nickel aluminide-silicide with low Schottky-barrier and series resistance for enhanced performance of dopant-segregated source/drain MuGFETs," *Symposium on VLSI Technology 2007*, Kyoto, Japan, Jun. 12-14, 2007, pp. 108-109.

[17.] K.-M. Tan, **T.-Y. Liow**, R.-T.-P. Lee, N. Balasubramanian, G. S. Samudra, and Y.-C. Yeo, "Plasma etching of gate electrode and gate-stringer for the fabrication of nanoscale multiple-gate transistors," *4th International Conference on Materials for Advanced Technologies* (*ICMAT*), Symposium E: Nanodevices and Nanofabrication, Singapore, Jul. 1-6, 2007.

[18.] **T.-Y. Liow**, K.-M. Tan, R. T. P. Lee, M. Zhu, K.-M. Hoe, G. S. Samudra, N. Balasubramanian, and Y.-C. Yeo, "Strain enhancement in spacerless n-channel FinFETs with silicon-carbon source and drain stressors," *37th European Solid-State Device Research Conference* (*ESSDERC*), Munich, Germany, Sep. 11-13, 2007.

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