COMPLIANT CHIP-TO-PACKAGE INTERCONNECTS FOR WAFER LEVEL PACKAGING

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Compliant Chip-to-Package Interconnects for Wafer Level Packaging

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Abstract

Explosive development of integrated circuit (IC) technologies has imposed continuous challenges on chip-to-package interconnections including I/O density, electrical performance, thermomechanical reliability and cost of fabrication and assembly. In this thesis, two novel compliant chip-to-package interconnect schemes, *Multi-Copper-Column (MCC)* and *Planar Microspring* interconnects, are developed particularly to address the thermomechanical reliability concern by enhanced 3-D compliances, while the other challenges are also investigated. A simplified analytical model for MCC interconnects reveals the favorable influence of lateral compliance on the thermomechanical reliability. Numerical analysis indicates that, in comparison with conventional Single-Copper-Column (SCC) and pure solder interconnects, Triple-Copper-Column (TCC) interconnect demonstrated 55% and 73% higher vertical and lateral compliances, with 34% higher electrical resistance and close inductance and capacitance. For *Planar Microspring* interconnects, various spring designs are evaluated and compared by simulation, and a *J*_shape design is chosen for further studies because of its high compliances (~35mm/N and ~170mm/N in horizontal and vertical directions, respectively), good electrical characteristics and manufacturability. Using micro-fabrication techniques compatible with CMOS back-end-of-line (BEOL) processes, high-aspect-ratio (~6) MCC and free-hanging *Planar Microspring* interconnects are successfully prototyped in wafer form, which facilitates on-wafer testing and burn-in to identify known good dies (KGDs) and hence enables cost-effective wafer-level packaging. High I/O density and bandwidth are provided as results of reduced interconnect pitches of 40μm and 100μm for *MCC* and *Planar Microspring* interconnects, respectively. The mechanical robustness, electrical functionality under low- and high-frequency conditions for both interconnects are

verified respectively by nano-indentation technique, electrical test on daisy chain of interconnections and scattering parameter (*S*-parameter) measurement using a customized set-up. For TCC interconnects, an electrical resistance of 21.1mΩ, inductance of 15.8nH and capacitance of 0.4pF were measured plus half of the on-chip and on-board metallization traces, while an insertion loss of ~3dB was achieved at 2GHz using a customized high-frequency measurement set-up. Since high-quality fine-pitch (100μm) organic test board is not available, numerical analysis techniques are utilized to investigate the thermomechanical reliability of *MCC* interconnect under temperature cycling. For *MCC* interconnects, a systematic method has been developed to model the distinctive profile of solder joints using the software *Surface Evolver*, and then to export the solder model into ANSYS for reliability analysis. A series of numerical analyses is conducted to establish the dependence of solder bridging and thermomechanical fatigue damage on material properties, interconnect geometry and orientation with respect to package etc. For composite interconnects such as *MCC*, a quantitative model is established to relate the compliance and deformation to thermomechanical damage, which explains the complex influence of the compliances of the non-solder component upon solder joint reliability and hence provides guidance for design of any similar composite interconnects. High electrical performance (insertion loss of <0.05dB at 10GHz) under various package scenarios are illustrated for both compliant interconnects by simulation with High Frequency Structure Simulator (HFSS). Equivalent lumped circuit model parameters are extracted for MCC interconnects and verified by good agreement between direct HFSS simulation of the interconnect and calculation of the equivalent circuit. In short, the 3-D compliances, low electrical parasitics, low power loss up to giga-scale frequency range, and good wafer-level manufacturability with reasonable cost make both *MCC*

and *Planar Microspring* promising candidates for next-generation high-density, compliant chip-to-package interconnections.

Chapter 1 Introduction

1.1 Introduction to Microelectronics Packaging

The past several decades have witnessed an explosive development in the microelectronic industry that brings about huge impact upon various aspects of human society. Starting from bulky discrete components, microelectronic devices have evolved into an era of ultra-large-scale integrated circuits that consist of millions of transistor in a single silicon chip. As the real functional blocks, transistors constitute the "*brain*" of integrated circuits (IC). However, any IC device cannot work without proper packaging. Briefly speaking, the function of IC packaging can be categorized as follows:

- To provide electrical paths for off-chip communication with high efficiency and signal fidelity;
- To facilitate thermal dissipation for proper operation of transistors and interconnections;
- To provide mechanical support to IC dies for easy handling and transportation;
- To protect functional ICs from external contamination and harsh environment;

It can be noted from the descriptions above that microelectronics packaging necessitates solid understanding of multiple scientific fields and hybrid technologies. As a result, concurrent engineering must be implemented during the whole development cycle of a certain package, i.e., from the initial design to final testing, to guarantee that the product meets all of the performance and cost targets.

Conventional IC packaging can be divided into different hierarchies in terms of its integration level as shown in Fig. 1-1. On the first level, a piece of IC die is generally

attached to a chip carrier, wire-bonded to a lead frame, and then encapsulated. On the second level, packaged chips are bonded to a printed circuit board (PCB) by either through-hole or surface mount technology. Conductor traces on PCB work as communication paths between different IC chips. On the third level, many PCBs are mounted onto a motherboard through sockets or connectors. Finally, motherboards are connected with each other to make the whole system.

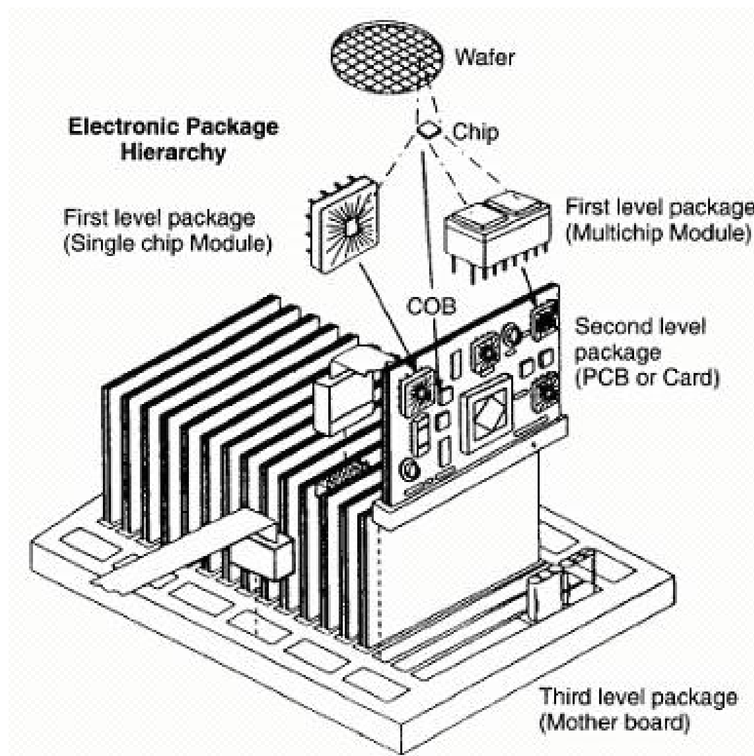


Fig. 1-1 Hierarchy of Microelectronic Packaging [1]

1.1.1 Historical Development of Microelectronics Packaging Technology

A great number of packaging schemes have been commercially available in the market and used for various applications. As shown in Fig. 1-2, packages have been evolving into smaller sizes and higher pin counts in order to match the ever increasing I/O density and miniaturization of ICs. Among the early packages, dual-in-line packages (DIP) gain most popularity in the 1970's and 1980's. DIP packages have an

upper limit of 64 pins, hence they have been gradually given way to pin grid array (PGA) packages that consist of more pins distributed in an area array. Through-hole packages are inherently limited in some applications by their big size or inefficient use of the PCB estate, and the solution comes with the emergence of surface mount packages in 1980's. Surface mount packages occupy only one side of the PCB estate and thus significantly increase the second level packaging density compared with through-hole packages. Elimination of drilling holes for through-hole packages also means that smaller pins with smaller pitches can be realized. Typical surface mount technologies include plastic leaded chip carrier (PLCC), small outline packages (SOP), quad flat packages (QFP), ball grid array (BGA) packages, tape automated bonding (TAB) and flip chip packaging [2]. It should be noted that some of them, for instance flip chip packaging, are different from others in terms of the connection manner between IC chips and carriers or PCB. As the name reveals, in flip chip technology the chip is flipped over with the active side connected to the carriers or PCB by solder bumps, which is in sharp contrast with DIP devices where the active side of die faces up and is wire-bonded to the carrier. Flip chip devices are electrically superior to conventional dual-in-line package (DIP) and pin grid array (PGA) packages since electrical parasitics associated with long bonding wires and lead frame pins are effectively eliminated. Although reliability concerns and cost issues are still to be solved before flip chip technology completely replaces wire bonding technology [3], it is accepted that flip chip technology is the right direction especially for high pin count devices. Both solder and gold bumping is used in flip chip technology, and correct choice is application dependent [4,5]. Furthermore, by properly applying underfill material between chip and carrier, reliability of flip chip packages can be enhanced by a factor of ten [6].

The industry may finally move to direct chip attach (DCA) technology that eliminates the first level package and thus further reduce cost, but the current infrastructure is still more suitable to other advanced schemes like chip scale packages (CSP), which is defined as package with a dimension size less than 1.2 times die size. Generally, CSP devices have solder ball interconnects with a diameter of 0.3mm and a pitch of 0.5mm. A CSP package may come as small as 5×5 mm^2 and 1 mm thick. Compared to DCA technology, CSP devices are easier to handle, assemble, test at speed and rework. Various CSP manufacturing methodologies have been developed by major semiconductor companies such as National Semiconductor, Motorola and Fujitsu etc. Typical CSPs can be divided into lead frame, rigid and flex substrate types and they still follow the conventional packaging process sequence, i.e., die singulation before packaging. On the other hand, wafer level packaging (WLP) technology has attracted more and more interest from industry because of its substantial cost advantage. Details on WLP technology will be given in Section 1.2.

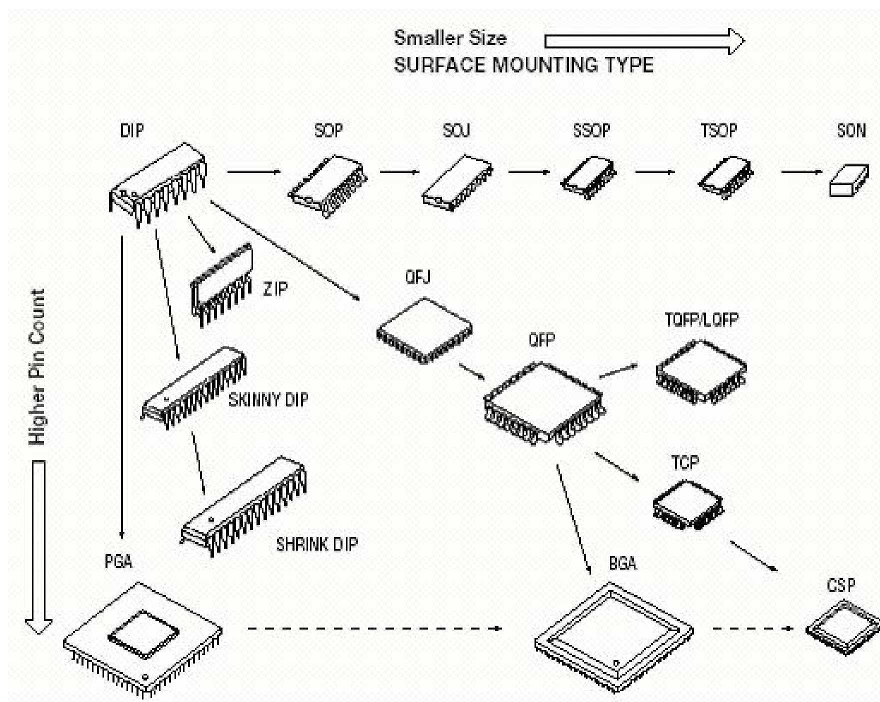


Fig. 1-2 Schematic of microelectronic packaging trend [2]

It can be noted that, in all packaging technologies described so far, the signal is always transmitted between dies or chips through interconnections made of electrical conductors. With the ever decreasing feature size of ICs and increasing working frequency in demand, the RC delay and crosstalk effects associated with the meal interconnections may develop to such a high level that the signal integrity cannot be maintained with any packaging technology mentioned above. Three-dimensional (3-D) packaging technology [7,8] suggests that dies or chips can be stacked in the vertical direction to shorten interconnections and to reduce the form factor of the final package as well. Another advantage is that the current infrastructure for packaging may still be used. To ultimately eliminate the bottleneck of signal transmission due to metal conductors, optics or wireless devices [9,10] may be utilized instead for signal communication within microelectronic packages.

1.1.2 Challenges in Microelectronics Packaging

The microelectronic packaging community will always continue to face technical challenges as long as people seek for more portable products with higher performance. As a guide for research in the packaging field, the International Technology Roadmap for Semiconductors (ITRS) clearly indicates the technical challenges that can be roughly categorized as PCB-related, material-related, and design and simulation challenges [11].

With the increasing complexity and integration of semiconductor technology, PCB fabrication has become a bottleneck for IC development. On-chip I/O count increases with transistors according to Rent's rule while chip size keeps falling, as a result more stringent requirements are imposed on the corresponding metal pads on PCBs in terms of their size and pitch. To realize the finer-pitch board-level

interconnects, microvia and soldering technologies need to be further improved to fabricate reliable multilayer PCBs. Owing to the cost consideration, organic substrates have been and will continue to be the focus of PCB research. Advanced organic substrates must have higher glass transition temperature (T_g) to accommodate the high temperature processing of Pb-free solders, and the planarity must be controlled at an acceptable level. Electrically, the substrates must have improved impedance control and lower dielectric loss to support high frequency applications.

Major material challenges are placed on underfill, Cu/low *k* dielectrics and Pb-free solders. Underfill is a liquid polymer-based composite that is dispensed and flow between the flipped chip and underneath PCB to relieve the high strain in the chip-to-next-level interconnects. The current underfill materials must be improved in terms of their manufacturability and reliability by enhancing their adhesion, lowering moisture absorption and broadening the operating temperature range. Advanced underfill materials under development include pre-dispensed underfills, reworkable underfills [9] and snap-cure underfills. Copper metallization and low-*k* dielectrics are introduced into electronic packaging for the sake of lower signal delay and thus higher signal integrity required by next generation IC products. However, mechanical concerns results from higher mismatch in coefficient of temperature expansion (CTE) and poor interfacial strength between low-*k* dielectric and metallization traces. Common low-k dielectrics include BCB and *SiLK* from Dow Chemical Co., Coral from Novellus Systems Inc., and Black Diamond from Applied Materials Inc., which are applied by either spin-on or chemical vapor deposition (CVD) technology [12,13]. Finally, Pb-free solders are mandated not only to relieve the environmental concerns but also to reduce radiation-induced soft errors. The most significant emissions of alpha particles come from decay of ^{210}Pb, an unstable isotope of lead in the solder [14]. Tin-based

alloys are the most promising lead-free solder candidates, including Sn-3.5Ag, CuSbAgSn and Sn-3.4Ag-4.8Bi etc.

The need of more powerful design and simulation tools represent another big challenge to the packaging community. As mentioned earlier, various materials and academic disciplines are involved in development of packages, which makes it impossible to analyze the complete performance of packages without powerful simulators. On the other hand, reliability and manufacturability must be taken into account at the early design stage to reduce cost and product development cycles. All of these considerations necessitate system-level design tools and simulators.

1.2 Wafer Level Packaging Technology

Wafer level packaging (WLP) refers to a revolutionary packaging technology in which bumping, assembly, packaging, test and burn-in are all handled at the wafer level while the singulation only happens before the final product is shipped to customers. Compared with conventional packaging technologies where silicon wafers with devices are first singulated into dies and then each die sequentially go through assembly, packaging and test and burn-in steps, all processes of WLP are directly fabricated on IC dies when they are still in the wafer form, and thus WLP is inherently a true chip-scale package. WLP technology is advantageous over conventional packaging schemes particularly in terms of the size miniaturization and cost per die [15].

Wafer-level packages usually use area-array solder balls as chip-to-next-level interconnection. According to the technology by which area-array distribution of solder balls is realized, WLPs can be categorized as redistribution WLP, encapsulated WLP and Flex/tape WLP. Many commercial WLPs have been successfully

introduced into the market and are reviewed in Table 1-1 with respect to their process features [16].

Redistribution WLP generally involves deposition of dielectric layer (such as BCB or polyimide) and metallization (Cu or Al) so that the peripheral chip pads are rerouted into an area-array fashion. Solder balls are generally formed by screen printing and reflowing. The under bump metallization (UBM) is very important since it enhances interfacial adhesion while blocking diffusion of Sn from solder into the redistribution layer. Some examples of redistribution WLPs are IZM-Berlin's S^3-Diepack, FCT's Ultra CSP and Fujitsu's *Super*CSP etc.

Table 1-1 List of commercialized wafer-level packages [16]

Company	**Technology**	**Feature**	**UBM**	**Dielectric**	**Solder ball diameter/pitch (mm)**
Amkor	wsCSP™	WB connection Cu/PI film	N/A	PI film	0.3-0.5/0.5-0.8
FCT	Ultra CSP™	Redistribution	Al/NiV/Cu	BCB	0.35-0.5/0.5-0.8
FormFactor	MOST™	WB "spring"	N/A	N/A	N/A
Fujitsu	Super CSP™	Encapsulated 0.1 mm Cu posts	Ti/Ni/Cu	PI	0.35-0.5/0.5-0.8
IZM Berlin	S^3-diepack	Cu redistribution	TiW/Cu/Ni/Au	BCB	0.3
Intarsia	MicroSMT™	Epoxy Si/glass encapsulation	Ti/Cu/Ni/Au	Proprietary	0.3
Oki	-	CMP encapsulated Cu posts	-	PI	-
Shellcase	Shell BGA™	Glass encapsulation	Ni/Au	BCB epoxy	0.3
Tessera	WAVE™	Cu/PI film, low modulus encapsulant		PI film	
Unitive	-	Redistribution	Al/Ti/Cr-Cu	BCB	Plated bumps 0.125-0.25

Encapsulated WLPs involve encapsulation of wafers, which contain the active devices, by bonding them with another Si or glass wafer. Commercial products include Shellcase's Shell CSP and Intarsia's MicroSMT. Hereby the Shell CSP is taken as an example to show the technology. As shown in Fig. 1-3, two glass plates are used to encapsulate the silicon wafer containing active components. The first step is to extend the chip pads into the dicing street that defines the final package size in X-Y plane. The backside of silicon wafer is then polished to 100 μm and the wafer is encapsulated between two glass wafers. The stacked wafers are sawn at the dicing street till the extended chip pads are exposed. Finally, metallization and UBM layer are respectively deposited and patterned, and solder bumps are attached.

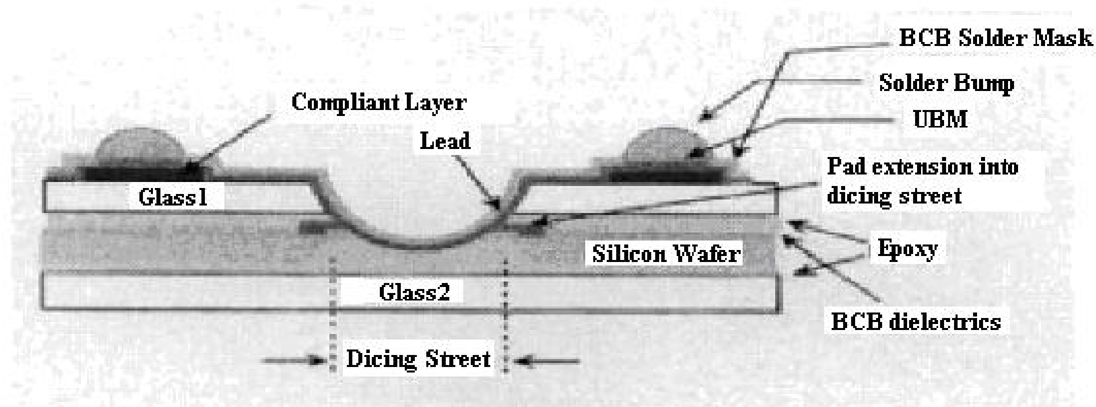


Fig. 1-3 Side view of Shellcase's wafer-level CSP [17]

Flex tape WLPs include Amkor-Anam's wsCSP^{TM}, Tessera's μBGA and Form Factor's MOST^{TM} technology. The latter two technologies produce compliant chip-to-next-level interconnects and thus are left to later sections. The wsCSP^{TM}, as shown in Fig. 1-4, starts with defining the redistribution layer on a Cu/polyimide flex tape. The flex tape is then attached to the silicon wafer and wire bonding is used to connect from peripheral IC pads to the tape. Liquid encapsulant is used to protect the wire bonds and eutectic solder bumps are finally attached.

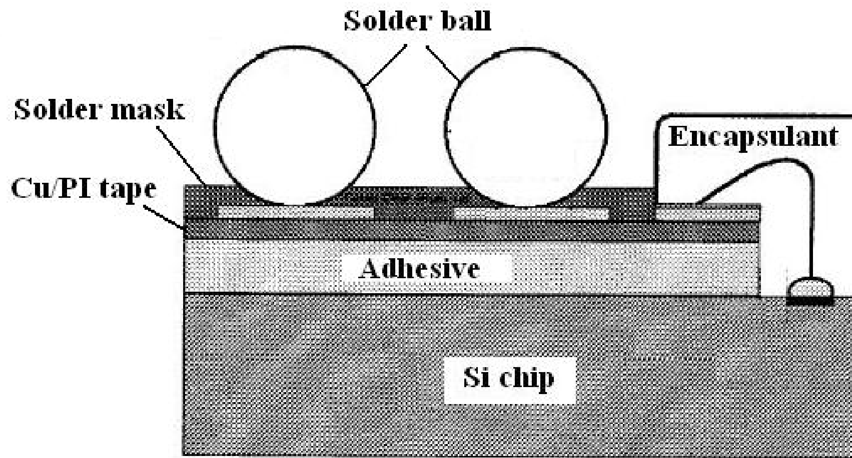


Fig. 1-4 Schematic of wsCSP^{TM} by Amkor-Anam [18]

Despite numerous advantages over conventional packaging schemes, wide acceptance of WLP technology is still challenged in terms of device reliability, test and burn-in methodologies and available PCB technologies. For solder jointed devices, the mechanical reliability depends on solder bump distance from neutral point (DNP) of the package, bump standoff and the number of bumps. Current WLPs demonstrate good reliability for dies with size of 10×10 mm^2, but the reliability for large chips are still in doubt. Secondly, since ICs are packaged during wafer fabrication, efficient wafer-level test and burn-in are required to identify known good dies (KGD) and known good packages (KGP) so that the whole yield can be enhanced to a reasonable level. Finally, with silicon processes evolving into higher technology nodes, WLP technology enables chips to end up with off-chip interconnects with extremely small size and pitch that was impossible before with conventional packaging technology. This correspondingly imposes much higher requirements than before on pad size and pitch on the PCB side. Current PCBs generally have pad pitches of ~500 μm, but IC technology and device functionality require PCB pads with a pitch of 100 μm or less. To make it worse, the PCB cost still has to be maintained at a low level to justify themselves in industrial applications.

1.3 Compliant Off-Chip Interconnects for Wafer Level Packaging

It was mentioned earlier that flipped chips are bonded with PCBs through either solder or gold bumping. One of the key advantages of solder over gold is that solder interconnects have self-aligning property when they go through reflow process. This feature results in a broader process window allowed for PCB planarity and bumping height uniformity. However, when the package is subjected to temperature cycling, the large CTE mismatch between Si (~2.3 ppm/°C) and organic PCB substrate (10-15 ppm/°C) induces high cyclic strains in solder joints, and thus fatigue and creep reliability remains a big concern for the solder interconnection. In the case of eutectic 63Sn/37Pb solder, which is preferred due to the low melting point of 183°C, creep deformation can happen even at room temperature. In fact, solder joints are the most frequently observed failure sites in flip chip devices. The current standard solution to the solder joint reliability problem depends on application of underfill materials. The pre-dispensed liquid underfill flows into the gap between flipped chip and PCB substrate and is then cured. Consequently, the thermal deformation is evenly distributed through the underfill material and solder joints, and thus the solder joint reliability is substantially improved. This reliability improvement, however, is obtained at the expense of cost increase and electrical performance degradation [19] associated with the underfill materials. Moreover, the underfill materials may also suffer from cracking or interfacial delamination during thermal cycling. Based on these considerations, compliant off-chip interconnects with both vertical and lateral compliances appear to be a better solution especially for wafer level packaging, in which the vertical compliance facilitates wafer-level test and burn-in, and the lateral compliance helps reduce strain accumulated in solder joints. Some compliant off-chip

interconnects for wafer-level packaging, which is either available on market or under development in laboratory, are reviewed as follow.

1.3.1 Tessera's μBGA and WAVE^{TM} technology

Tessera's μBGA may be one of the earliest and also the most popular package scheme using compliant interconnects. It was originally developed in the early 1990's for a unique multiple chip module (MCM) at Tessera, with vertical compliances that facilitate reliable contact during electrical testing. However, μBGA CSPs have been so matured that they are extensively used in flash memory devices and Rambus RDRAM [16].

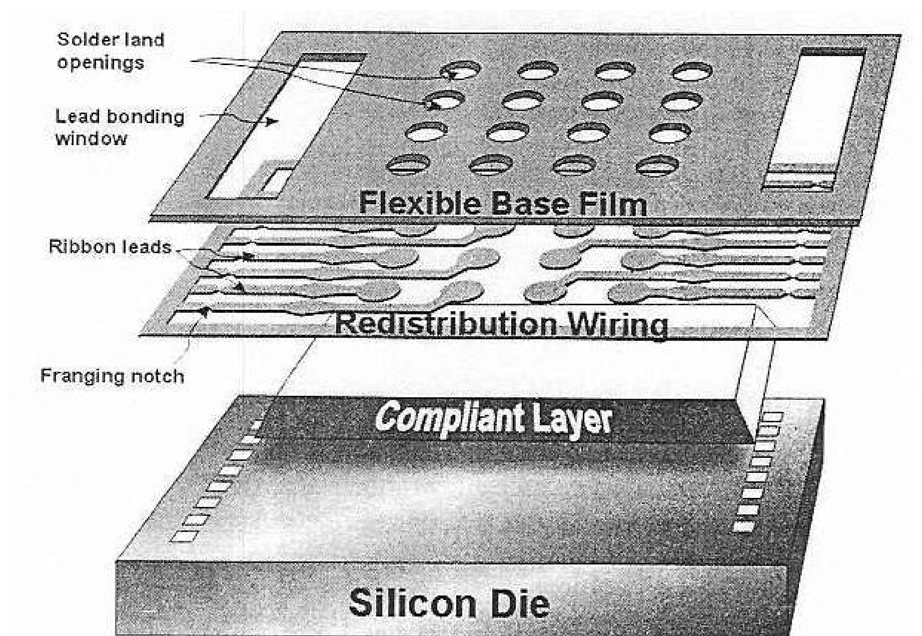


Fig. 1-5 Fundamental components of μBGA package by Terresa [20]

Although some licensees of the μBGA technology (such as Amkor and Hitachi etc.) have developed many modifications, the fundamental elements are still the same as shown in Fig. 1-5. The compliant or buffer layer plays the most critical role in providing the required compliances. It is generally made of low-modulus silicone

elastomer with a thickness of 75~150μm. Since the compliant layer is in direct contact with the active side of IC, it must be free of alpha-particle. The redistribution layer provides flexible links between IC pads and the chip-to-next-level interconnections such as solder balls. Another feature is that the notched leads remain attached to the carrier film until the moment of bonding. The parasitic resistance, inductance and capacitance (R, L and C) for a 3.2 mm long lead are measured to be 0.59Ω, 3.1nH and 0.502pF at DC condition. The board-level reliability of μBGA is excellent, with a life of over 2876 cycles under temperature cycling between -60~150 °C [20].

Followers of μBGA include Zinger^{TM} and Wide Area Vertical Expansion (WAVE^{TM}) technologies, and the latter is briefly reviewed here. In short, WAVE^{TM} upgrades μBGA^{TM} by integrating more flexible interconnections and bonding all pads to the substrate simultaneously instead of individually [21-22]. As shown in Fig. 1-6, the WAVE packages integrate the silicon die with a stress decouple layer made of low-modulus encapsulant and a copper intrachip wiring layer made of two metal/polyimide substrates. The assembly process, which plays the most important role in providing compliances, starts from formation of the peelable copper bonding leads. By injection of encapsulant, the gap between flex substrates and die is filled and expanded to a height of 100~150μm. The peelable copper leads transform to flexible links during this injection process. The thermal stress due to CTE mismatch is minimized since the stress decoupler layer and flexible link allow relative movement of die and flex substrates in X, Y and Z directions. Board-level reliability testing demonstrated a life of over 1500 cycles under thermal cycling in the range of -40~125 ºC for package samples with a gap distance of 150 μm between flex substrate and Si die. Numerical analysis indicates the reliability can be further improved with optimization of lead type, lead orientation and gap distance [22] etc. Key electrical

parameters such as signal trace inductance and capacitance are measured to be 4.5nH and 0.74pF, respectively.

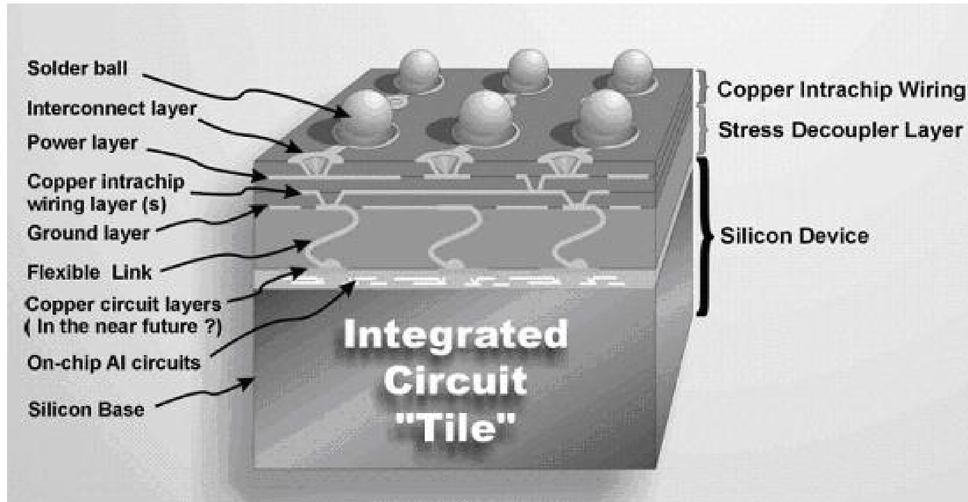


Fig. 1-6 Schematic of Wide Area Vertical Expansion (WAVE^{TM}) package [21]

1.3.2 Sea-of-Lead (SoL) Interconnects

Sea of leads (SoL) [23-26] is an ultra-high-density interconnection technology developed at the Georgia Institute of Technology (GIT) to meet high-performance requirement of I/Os (e.g., gigascale off-chip communication) anticipated by ITRS. Important features of SoL interconnects include high I/O density of more than 10^4 leads per cm^2, 3-D compliances, low electrical parasitics and high bandwidth etc.

SoL is a wafer-level packaging technology since it extends the back-end IC technology to include the fabrication of chip-to-next-level interconnects. The basic process sequence starts from exposure of chip pads and evolves as follows: 1) apply and pattern polymer; 2) deposit seed layer for later electroplating of Cu leads that then work as electrical and mechanical interconnection between the chip pads and off-chip solder bumps; 3) remove seed layer, cover the Cu leads with a second polymer layer and pattern it for later solder electroplating; 4) deposit another seed layer, electroplate solder, and finally remove the seed layer. The key to SoL packaging technology lies

in the integration of thick (25μm) polymer layer, Ultradel 1414, which is a mixture of polyimide and siloxane. The low Young's modulus and dielectric constant of Ultradel 1414 enable interconnects with high out-of-plane and in-plane compliances, low electrical parasitics and crosstalk. Fig. 1-7 is a SEM photograph of SoL interconnect array.

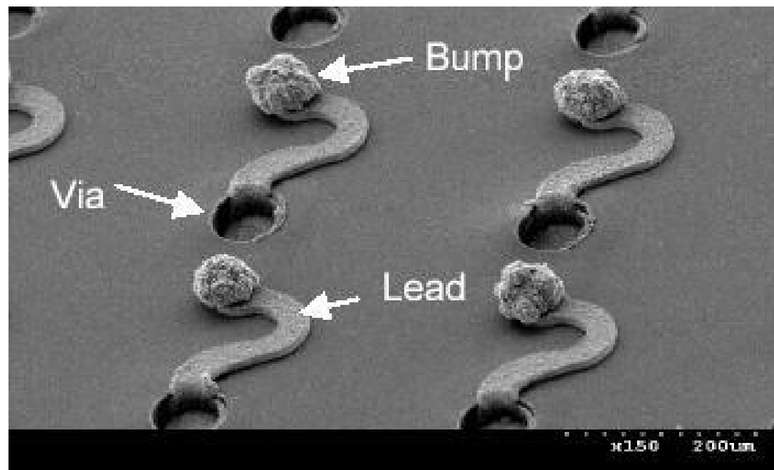


Fig. 1-7 SEM photograph of SoL interconnects [25]

Continuous improvements have been made to enhance the SoL packaging technology described as above. Embedded air-gaps under the Cu leads were made by processing a polynorbornene (PNB) sacrificial (Unity™ 400) layer. Obviously, air-gaps help to increase mechanical compliances and electrical performance as well because of the low permittivity of air. Furthermore, optical waveguides are proposed to be incorporated within the next-generation SoL packages, in which the embedded air-gaps are used as the upper cladding for optical waveguides. Potential advantages of next-generation SoL packages include enhanced predictability of global clock signals, higher heat removal and power supply capabilities that is especially important to packaging of hybrid electrical/optical systems.

1.3.3 Helix-type Interconnects

Another compliant chip-to-next-level interconnects, namely helix-type interconnects [27], have been developed at Georgia Institute of Technology based on conventional IC technology. Starting from completion of die pads, a thick photoresist layer is first applied and patterned, and the bottom post is electroplated with seed layer. After sputtering a new seed layer, a thinner photoresist layer is applied and patterned for the following electroplating of an arc beam. By alternatively applying photoresist and electroplating, a five-layer helix-type interconnect was fabricated as shown in Fig. 1-8. One can see that the processes of helix-type interconnects can be easily integrated into standard IC fabrication technologies.

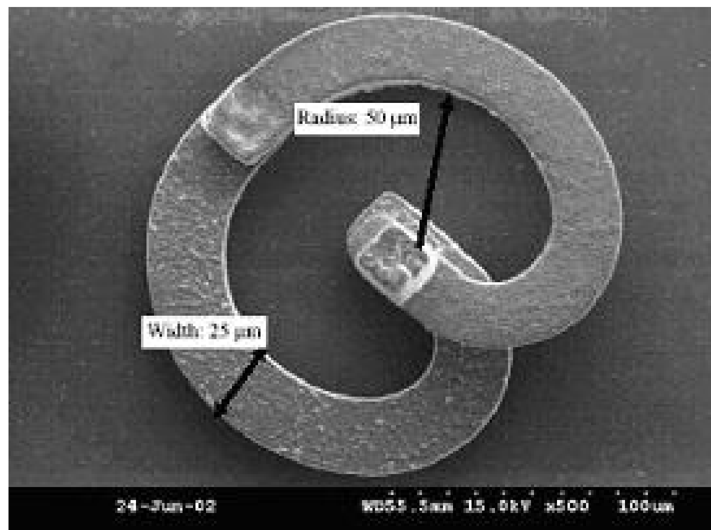


Fig. 1-8 Helix-type compliant interconnects [27]

To reduce the involved mask number and thus cost, a G-helix interconnect is designed and fabricated using alternating thick photoresist lithography and Cu electroplating process [28]. Compared to the five masks used in beta-fly helix, only three masks are involved in G-helix, which however still achieves the target compliances. Following the similar fabrication sequence of thick photoresist and Cu electroplating, another new compliant interconnect, FlexConnects [29], is recently

proposed to further reduce the fabrication to 2-mask process, and also to address the high-inductance issue that was observed in G-helix. Both single-path and parallel-path designs are investigated. It is found that, since parallel-path design provides two electrical path compared to the one path in single-path design, the compliance of parallel-path design is 4 times that of single-path design while the electrical resistance is kept the same.

1.3.4 MOST^{TM} Interconnects

In 1998, FormFactor introduced Microspring^{TM} technology, the industry's first wafer-level packaging technology that can be integrated with silicon back-end processes. Other than wafer-level contactors used for burn-in or test, it also enables fabrication of chip-to-next-level interconnects, which is called Microspring^{TM} contact on Silicon Technology (MOST^{TM}) [30,31]. The core of MOST^{TM} is fabrication of the microspring as shown in Fig. 1-9 based on wire bonding technology. Three assembly methods have been developed by FormFactor and its licensees to make the connection between MOST^{TM} contacts and PCB: conventional solder attach, self-socketing die, and attach using conductive epoxies.

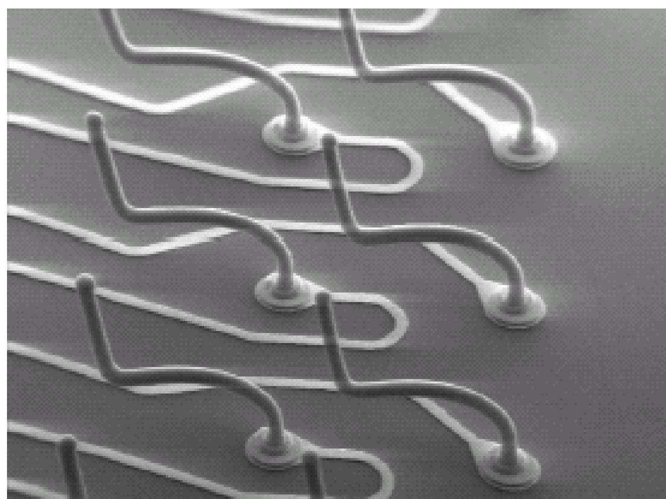


Fig. 1-9 MOST^{TM} interconnect array by FormFactor [31]

In addition to low cost advantage due to utilization of conventional materials and equipments, MOST^{TM} interconnects also eliminate usage of underfill because of its controlled shape and inherent spring characteristics. Moreover, soft errors caused by Pb-containing solder can be significantly reduced or even totally removed in the case of self-socketing die assembly where solder is not used for connection. Reliability test shows a life of over 1000 cycles under temperature cycling in the range of -55~125ºC. Compared to many solder-ball based interconnects, MOST^{TM} interconnects demonstrates low inductance and low stray capacitance. Finally, an obvious disadvantage is that the MOST^{TM} interconnects are fabricated by wire-bonding, which is an sequential process and thus the cost per interconnect is relatively high.

1.3.5 Cantilevered Nanospring Interconnects

Nanospring interconnects [32-34] have been introduced by Georgia Institute of Technology, Xerox Palo Alto Research Center and Nanonexus Inc. to address the compliant ultra-fine-pitch interconnects requirement for next-generation packaging. It is based on metal sputtering technology in which residual stress in metal films lead to deformation after the film is released from the substrate. By controlling the stress gradient across the film thickness, a free-standing cantilever may bend up or down to an expected extent. In nanospring technology, Mo(80)/Cr(20) alloy is chosen to make the cantilever-type interconnects because its residual stress can be adjusted from compressive to tensile with various sputtering conditions. The cantilever structure is then coated with a highly conductive metal layer such as Au to improve its electrical conductivity. Finally, the adhesive layer under the cantilever structure is etched and the cantilever bend upward to form the spring interconnects. A completed spring interconnect array is shown in Fig. 1-10.

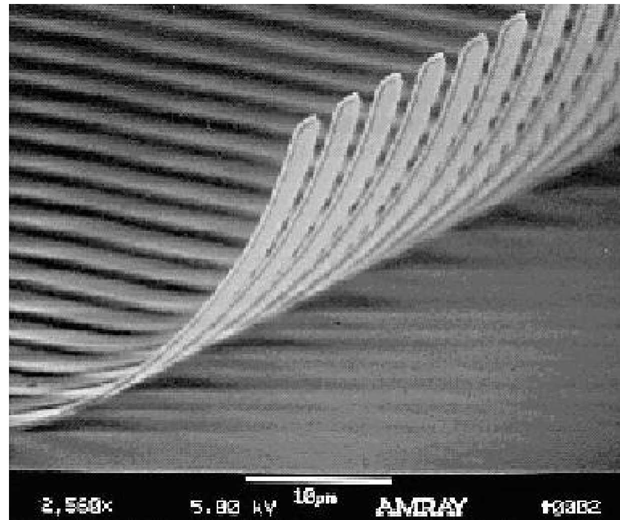


Fig. 1-10 Ultra-fine-pitch nanospring interconnects [33]

The most remarkable advantage of this interconnect technology is that it enables fabrication of interconnects with ultra-fine pitch as small as 6μm. Compared to other compliant interconnects, spring interconnects possess very high compliances, i.e., tens of millimeters per Newton in X and Y directions, and over 10,000 mm/N in Z direction. Low cost is also an advantage of this technology since it involves few process steps and can be easily integrated with standard IC technologies. The obvious drawback is that only some specific metals can be used to fabricate the nanospring with this method.

1.4 Proposal of Novel Compliant Interconnects

As can be seen in the previous section, the compliant interconnects developed so far are still more or less plagued by either process or material issues. For wafer level packaging, it is a fundamental requirement that the interconnect process is fully compatible with the standard IC back-end-of-line (BEOL) process. High throughput is always desired as well. The interconnect should be made of common materials with high electrical conductivity, but they should not be limited to specific materials. In

this thesis, two novel off-chip interconnect schemes are proposed and studied, namely *Multi-Copper-Column (MCC)* and *Planar Microspring* interconnects.

Fig. 1-11 shows a schematic view of MCC interconnects that are actually a modification of conventional Cu post interconnects [35-37]. The column array in MCC interconnects can be formed by replacing the conventional short and bulky Cu post with multiple slender Cu columns. Hence, the fabrication will be focused on how to achieve the Cu columns with high aspect ratio and minimum spacing. The most significant advantage MCC over other compliant interconnects is that it can be fabricated with the lowest number of process steps. From the performance point of view, the high-aspect-ratio Cu columns provide high flexibility in the lateral direction. The multiple column design is superior to conventional bulky post in terms of electrical performance or function at least in two aspects: First, the ratio of surface area over volume is enhanced which is in favor of electrical conduction particularly within the high frequency range; Secondly, a longer life of service or functionality may be expected for MCC interconnect because of the redundant column design within a single interconnect. Even if electrical interconnection failure occurs at the interface between an individual Cu column and the solder joint, the remaining columns are still able to support the chip functionality. In fact, at this moment the MCC interconnect obtained even higher lateral flexibility.

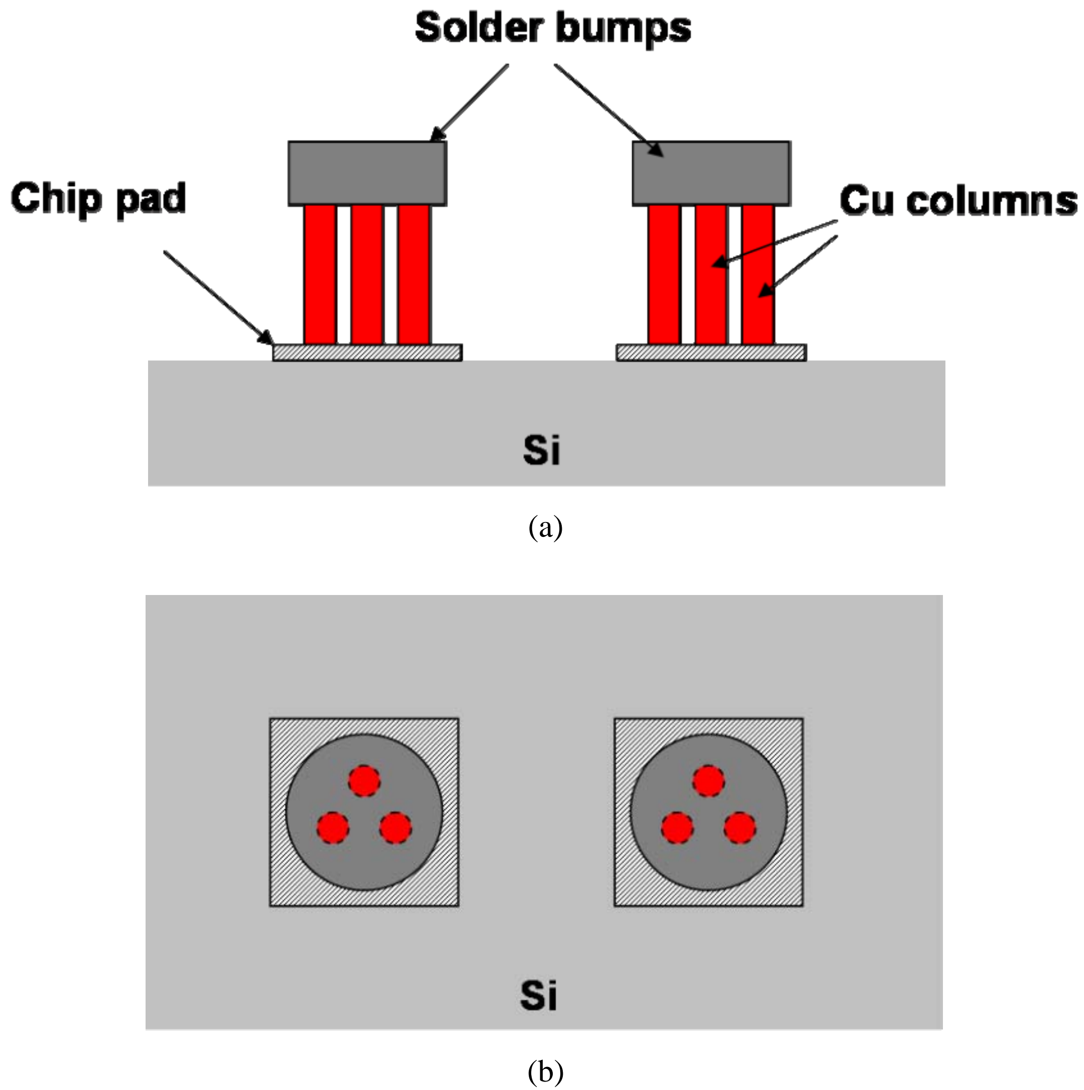


Fig. 1-11 Schematic of *Multi-Copper-Column (MCC)* interconnects (a) side view; (b) top view

Fig. 1-12 shows a schematic view of the so-called *Planar Microspring* interconnect. The name results from the fact that the springs as shown in Fig. 1-12(b) are planar structures, which makes it distinctive from the 3-D Nanospring interconnect [33]. The major component of this interconnect is the meander springs which are suspended over a cavity and electrically connected to the chip pads through the vias. Surface micromachining techniques will be used to realize the cavity in the sacrificial layer and hence release the springs. Solder bumps are applied on the central pad of spring structures and finally connect to the pads on the PCB side.

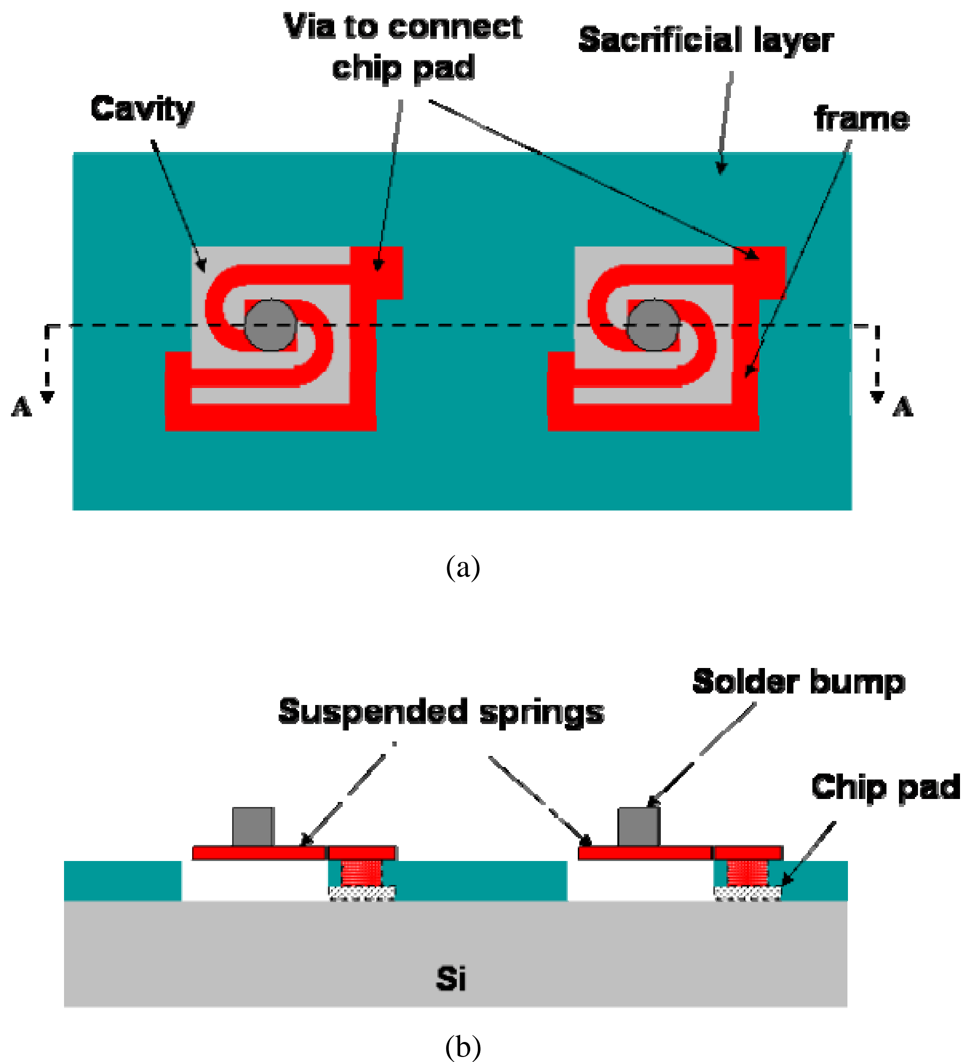


Fig. 1-12 Schematic of *Planar Microspring* interconnects (a) plan view; (b) A-A cross section view

Because of the meander shape and separation from the underneath substrate, the spring beams enable the interconnects of high compliances in both vertical and lateral directions. Fig. 1-12 shows a J_shape springs that will be thoroughly studied in the following chapters. In fact, the spring profile can be optimized to meet the mechanical and electrical requirements for various applications.

The subsequent chapters will respectively describe the initial design, fabrication, characterization, advanced numerical analysis of thermomechanical reliability and high-frequency electrical performance for both interconnect schemes.

Chapter 2 Design Considerations for Compliant Interconnects

A typical compliant interconnect design is composed of a solder joint and a flexible structure, which significantly enhance the 3-D compliances of the whole interconnect. This flexibility may significantly facilitate wafer-level test and burn-in, and more importantly, is expected to improve the solder joint reliability under thermal cycling. On the other hand, one should note that the electrical parasitics associated with the compliant interconnects are usually higher than the conventional solder interconnects. The increased parasitics manifest themselves as a longer *RC* delay or a substantial simultaneous switching noise in the power plane.

Because of these opposite effects, a compliant interconnect must be carefully designed to achieve a good balance between the compliances and electrical parasitics. This can only be done on the basis of a clear understanding of the geometry dependence of the compliances and electrical parasitics, which may be much more complicated for compliant interconnects compared to the conventional ones. For example, in the earlier column-based interconnects such as *Super*CSP and Oki's interconnect schemes [35-37], the column's contribution to the compliances and parasitics is small and straightforward because of its short height, bulky diameter and the single column design. For MCC interconnects in this thesis, however, the slender columns are expected to result in higher compliances and electrical resistance compared to the bulky counterparts. Hence, the column design determines to a large extent the mechanical and electrical performance of the whole interconnect. Furthermore, owing to the multiple column design, the geometry dependence of the

compliances and electrical parasitics is more complicated for MCC than for the conventional counterparts.

In this chapter, analytical or numerical analysis is conducted on MCC and Planar Microspring interconnects to understand their compliances and electrical parasitics behavior. It has been instinctively believed for a long time that, for off-chip interconnects between Si die and package substrate or printed circuit board, an enhanced compliance will lead to higher thermomechanical reliability, but unfortunately no quantitative correlation has been established. In the first part of this chapter, for the first time, a simplified analytical model is constructed in terms of MCC interconnects to give the quantitative correlation between lateral compliance and strain damage, and finally the fatigue life under thermal cycling. The result can be used to roughly but quickly evaluate the interconnect reliability as a function of geometric dimension and material properties. In the second part, numerical analysis is used to reveal the advantages of MCC over conventional Single-Copper-Column (SCC) and pure solder interconnects. Various designs of planar microsprings are evaluated in terms of three-dimensional compliances and electrical parasitics up to 10GHz. Finally, for both MCC and Planar Microspring interconnects, parametric studies are conducted to explore the geometric effects on compliance and electrical parasitics (R, L & C), which can be used as design guidelines for various applications.

2.1 Quantitative Correlation between Compliance and Fatigue Reliability

2.1.1 Analytical Model and Analysis

A simple two-dimensional model as shown in Fig. 2-1 was established to deduce the quantitative correlation between the lateral compliance and the fatigue life of the solder joint within an MCC interconnect. Assuming a stress-free state at room

temperature, Fig. 2-1(a) shows the deformation of the critical MCC interconnects at a temperature increase of ΔT, since the packaging substrate expanded more than the Si chip. Here the critical interconnect refers to the interconnect fartherest from the neutral point of the assembly. Fig. 2-1(b) and (c) show the exploded view of a single copper column and solder joint under deformation, where the solder joint is simplified with a quadrilateral model. It should be noted that, although only three columns are drawn, the model and analysis are also applicable to MCC interconnects consisting of any number of columns.

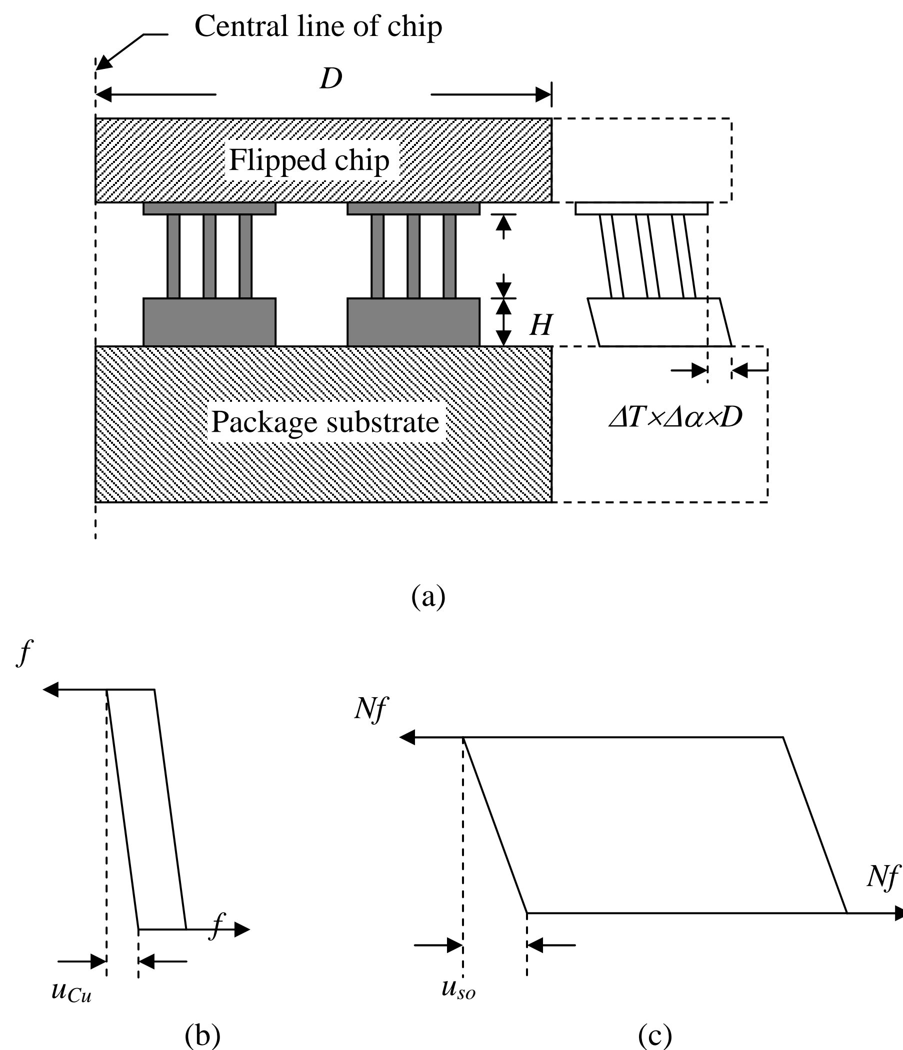


Fig. 2-1 Schematic of MCC interconnects under lateral deformation

Assuming that the Si chip and the PCB substrate are rigid in comparison with the interconnects, the total relative shear deformation (u_{to}) on the critical interconnect was obtained as equation (2-1), where ΔT is the temperature cycling range, α_{sub} and α_{chip} are thermal expansion coefficients of substrate and chip, respectively, and D is half of the diagonal length of the chip:

$$u_{to}=\Delta T\times\Delta\alpha\times D=\Delta T\times(\alpha_{sub}-\alpha_{chip})\times D \quad \ldots\ldots \quad (2\text{-}1)$$

For a single Cu column in the critical MCC interconnect (which is the farthest from the central line of chip) as shown in Fig. 2-1(b), by assuming f as the shear force at the column ends, the relative lateral displacement of the Cu column (u_{Cu}) can be obtained [37] as:

$$u_{Cu}=\frac{fh^3}{6E_{Cu}\pi r^4}\text{, (if }\frac{h}{2r}\geq 8\text{)} \quad \ldots\ldots \quad (2\text{-}2)$$

where h is column height, r is column radius and E_{Cu} is the elasticity modulus of Cu. For the copper columns made by electroplating process, the height/diameter ratio (i.e., the aspect ratio) is usually not quite high (<8) and the deflection due to transverse shear is not negligible. Hence a more accurate solution for the lateral deflection of a column with low aspect ratio [37] should be:

$$u_{Cu}=\frac{fh^3}{6E_{Cu}\pi r^4}+\frac{10fh}{9G_{Cu}\pi r^2}\text{, (if }\frac{h}{2r}<8\text{)} \quad \ldots\ldots \quad (2\text{-}3)$$

where G_{Cu} is shear modulus of Cu with other symbols same as above. Correspondingly, for an MCC interconnect that consists of N copper columns, the solder joint is subjected to a lateral force $N\times f$ that is equal in magnitude but opposite in direction on the top and bottom surface, as shown in Fig. 2-1(c). It can be seen from Fig. 2-1(a), however, that the distribution area of the shear force is different for the top and bottom surfaces of the solder joint. Therefore, an effective area A_{so}, which

is the average of the shear force distribution area on the top and bottom solder joint surface respectively, is taken for analytic calculation of the solder deformation. By assuming only elastic deformation, the relative lateral displacement of the solder joint (u_{so}) can be simply expressed as:

$$u_{so} = \frac{Nf}{A_{so}G_{so}} \times H \quad \ldots\ldots \quad (2\text{-}4)$$

where H is the solder joint standoff and G_{so} is the shear modulus of solder. Therefore, in an alternative form, the lateral load f can be expressed as:

$$f = \frac{u_{so}A_{so}G_{so}}{NH} \quad \ldots\ldots \quad (2\text{-}5)$$

On the other hand, the total shear deformation (u_{to}) of the interconnect should be the sum of the shear displacement of the copper column (u_{Cu}) and the shear displacement of solder (u_{so}):

$$u_{to} = u_{Cu} + u_{so} \quad \ldots\ldots \quad (2\text{-}6)$$

By substituting equations (2-1), (2-3) and (2-5) into the equation (2.6), the relative shear displacement of solder can be obtained as:

$$u_{so} = \frac{\Delta T \Delta \alpha \cdot D}{1 + \frac{A_{so}G_{so}}{NH}\left(\frac{h^3}{6E_{Cu}\pi r^4} + \frac{10h}{9G_{Cu}\pi r^2}\right)} \quad \ldots\ldots \ (2\text{-}7)$$

The shear strain range ($\Delta\gamma$) of the solder joint within on thermal cycle thus can be obtained as:

$$\Delta\gamma = \frac{u_{so}}{H} = \frac{\Delta T \Delta \alpha \cdot D}{H\left[1 + \frac{A_{so}G_{so}}{NH}\left(\frac{h^3}{6E_{Cu}\pi r^4} + \frac{10h}{9G_{Cu}\pi r^2}\right)\right]} \quad \ldots\ldots \ (2\text{-}8)$$

It can be seen from the equation (2-8) that the shear strain range of the solder joints of the MCC interconnects is lower than that of pure solder interconnects

without copper columns, which can be expressed as $\frac{\Delta T \Delta \alpha \cdot D}{H}$. For example, for a triple-copper-column (TCC) interconnect with r=2.5μm, h=5μm, H=18μm, R=12.5μm, E_{Cu}=127.4GPa, G_{Cu}=46.84GPa, G_{so}=12GPa and A_{so}=147.65μm^2 as defined above, the equation (2-8) predicts that the effective shear strain range is reduced by 19% in comparison with the pure solder interconnect without copper columns. Finally, the shear strain range can be related to thermal fatigue life by Engelmaier's equation [38]:

$$N_f = 0.5\left(\frac{\Delta\gamma}{0.65}\right)^{\frac{1}{c}} \quad \ldots\ldots \text{(2-9)}$$

where N_f is the cycles to failure and c is the fatigue ductility exponent. Correspondingly, if the fatigue ductility exponent takes a value of -0.4, an increase of 69% in the fatigue life is predicted by the equation (2-9).

2.1.2 Discussion

In the previous section, a formula has been deduced so that, for MCC interconnects with any number of columns, the improvement of solder joint fatigue life compared to pure solder interconnects can be roughly projected. However, some assumptions were taken implicitly or explicitly during the deduction and thus the consequent limitation should be addressed.

1) It was assumed that the total lateral deformation of the critical interconnect was only dependent on the package and chip dimension, temperature variation range and the CTE mismatch between package and chip, as indicated by the equation (2-1). The "*restraining*" effect of interconnects on the thermal expansion or contraction of package and chip is therefore neglected. For very high density interconnect array,

however, the thermal deformation of chip and package substrate is restricted to some extent, and thus the lateral deformation of the critical interconnect is no longer a constant as calculated by equation (2-1), but a function of the interconnect count and layout pattern. In particular, the shear strain range calculated by equation (2-8) will be higher than the actual value. The "*restraining*" effect is clearly revealed in Chapter 5.

2) It was assumed that the solder joint and copper columns were subjected to elastic deformation only, and the material properties were constant within the temperature variation range. These two assumptions are not true particularly for solder since, for example, the working temperature can easily go up beyond 0.6 of the melting point of eutectic 63Sn37Pb solder (183°C), and therefore the majority of solder deformation is plastic. Consequently, the shear deformation and shear strain range of the solder joint as shown by equation (2-7) and (2-8) are actually under-estimated. Similarly, the solder properties are highly dependent upon temperature. To compensate for this effect, a temperature-averaged solder property may be applied in the calculations.

3) Referring to Fig. 2-1(c), the top and bottom surfaces of the solder joint are subjected to shear forces equal in magnitude but opposite in direction. However, the effective acting area of the shear forces is different between the top and bottom surfaces. In equation (2-4), an effective surface area is taken by averaging top and bottom surface area and then is arbitrarily used to correlate the shear force and shear deformation. It is anticipated that the solder deformation would be affected by the copper column pattern. For example, the solder must deform in a different way if four copper columns transform from a square pattern to a rectangular pattern. However, this effect was not reflected in the formulae above. Finally, the shape of the solder

joint and Cu columns were not taken into account in the analysis and thus the accuracy of strain analysis is limited.

2.2 Calculation of Compliance and Electrical Parasitics

2.2.1 Simulation Models

2.2.1.1 ANSYS Model for Compliance Calculation

The previous section gave an approximate analytical estimation on how the MCC geometry affect the interconnect compliance and hence fatigue life. The accuracy of the analytical solution is limited by many assumptions as described above. Furthermore, the analytical method is not possible for complex structures such as Planar Microspring interconnects. Therefore, in this section, numerical analysis with ANSYS 6.1 is conducted to calculate the compliances of MCC and Planar Microspring interconnects as functions of their geometric parameters.

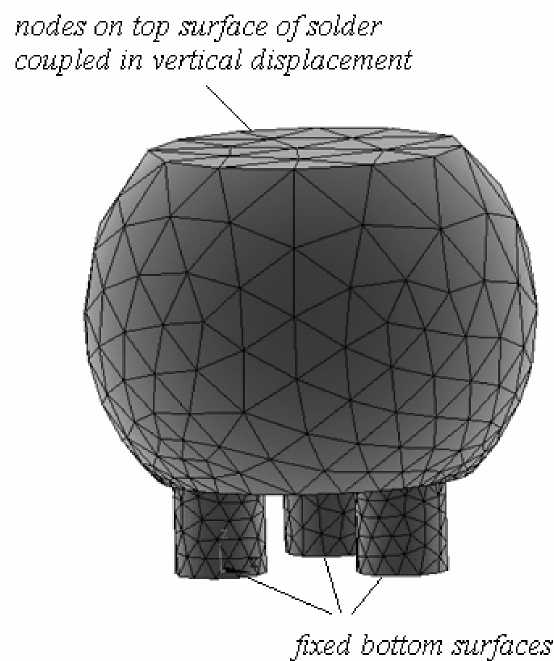


Fig. 2-2 TCC interconnect model for compliance calculation

Fig. 2-2 shows the ANSYS model for compliance calculation of a triple-copper-column (TCC) interconnect. The solder is modeled as a double truncated ball on top of three copper columns, which are arranged in an equilateral triangular manner. It will be shown in Chapter 5 that the solder actually wicks up along the copper column surface and thus the columns are partially embedded in the solder. This distinctive interface may have significant influence on the solder strain deformation, but not the compliances. Therefore, the double truncated model is used here for the sake of simplicity. The boundary conditions are as follows: the copper column ends connecting to the chip are fully fixed in all degrees of freedom (DOF), and the nodes on the solder top surface are coupled in vertical movement. It is understood that, in a real application scenario, the solder joint top surface may slightly tilt due to warpage of the package substrate during temperature variation. Because of the small size of MCC interconnect, this tilt translates into very small difference in vertical movement of the nodes associated with the solder top surface. Moreover, the tilt magnitude is dependent upon the solder joint position with respect to the neutral point of package substrate, which makes it very difficult to include this effect in simulation of an individual interconnect. As a result, all the nodes on solder top surface are assumed to be coupled in vertical movement as shown in Fig. 2-2. Vertical or lateral force is applied to the solder top surface, and the resulting average vertical or lateral displacement of relevant nodes is taken to calculate the compliances.

Similarly, the Planar Microspring interconnect model was constructed as Fig. 2-3, consisting of microspring beams, central pad and a solder joint. The ends of microsprings are assumed to be fixed as boundary conditions. The solder joint is still simulated with a double truncated model, with the top surface modeled as a rigid plane like the case of MCC interconnects. First a vertical force and later a lateral force

is applied to the solder top surface, and the resulting displacements were taken to calculate the vertical and lateral compliances, respectively.

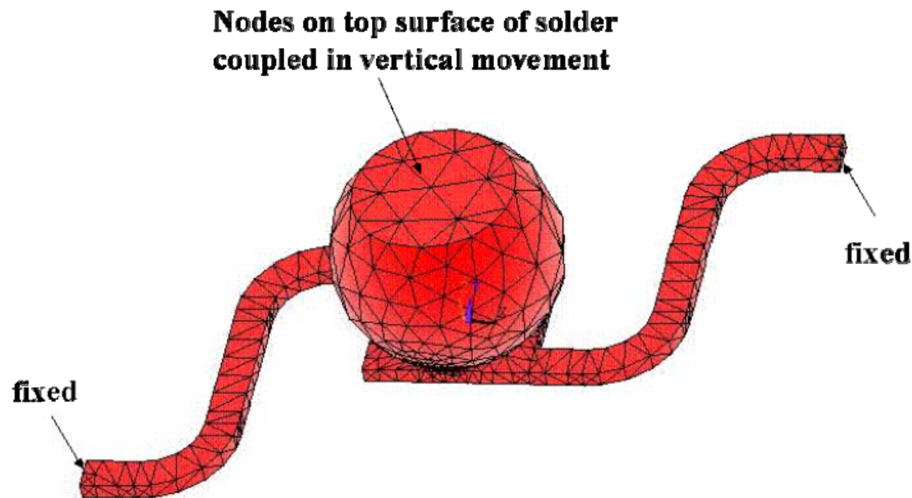


Fig. 2-3 Planar Microspring interconnect model for compliance calculation

For these two compliant interconnect schemes, the columns in MCC and the microspring beams are made of electroplated Cu, while the solder joint were always made of electroplated eutectic 63Sn-37Pb alloy. Although these two materials both demonstrate remarkable capability for plastic deformation, the compliances are evaluated in the linear elastic domain for the ease of comparison. SOLID92 element is used for finite element modeling in ANSYS. The mechanical properties of electroplated Cu and 63Sn-37Pb are shown in Table 2-1.

2.2.1.2 Ansoft's Q3D Model

The DC and low-frequency (100MHz) electrical parasitics (*R, L & C*) associated with the compliant interconnects are calculated with Ansoft's Q3D simulator [39]. As shown in Fig. 2-4, the model consists of not only the interconnect itself, which in the case of MCC includes Cu columns and solder joint, but also the Al pad on the chip

and Cu pad on the substrate. This arrangement is made in order to be consistent with the high-frequency simulation model in Chapter 6, in which the pads cannot be excluded because of the de-embedding limitations. Similarly, referring to Fig. 1-11, the Ansoft's Q3D model for planar microspring interconnects is composed of microspring beams, central pad, solder joint, metal frame, Cu plug in the via, and pads on both chip and package substrates. It is also shown in Fig. 2-4 that the electrical current flow through the interconnect structure, starting from the bottom surface of the chip pad and finishing at the top surface of the pad on the substrate. The electrical crosstalk effect of neighboring interconnects is neglected in this thesis, thus all the electrical values refer to self parasitics with respect to a single interconnect. The material properties used in the simulation are shown in Table 2-1.

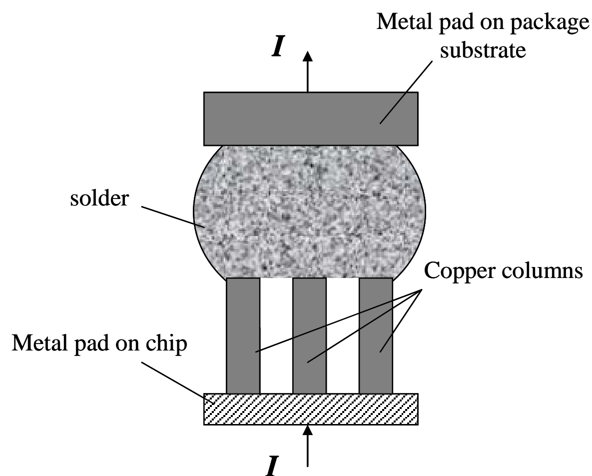


Fig. 2-4 Ansoft's Q3D model for electrical parasitics calculation

Table 2-1 Material properties for ANSYS and Ansoft's Q3D simulation

	Elastic modulus, GPa	Poisson's ratio	Electrical conductivity, S/m
Electroplated Cu [40]	127.4	0.36	5.88E+7
63Sn-37Pb [41]	33.58	0.4	7E+6
Al	-	-	3.8E+7

2.2.1.3 Ansoft's HFSS model

Ansoft's High Frequency Structure Simulation (HFSS) v8.5 is used for optimization of the planar microspring shape designs in terms of associated electrical parasitics. As shown in Fig. 2-5, microstrip transmission lines are employed to transmit the signal through the interconnect. Silicon dioxide (SiO_2) and FR-4 were

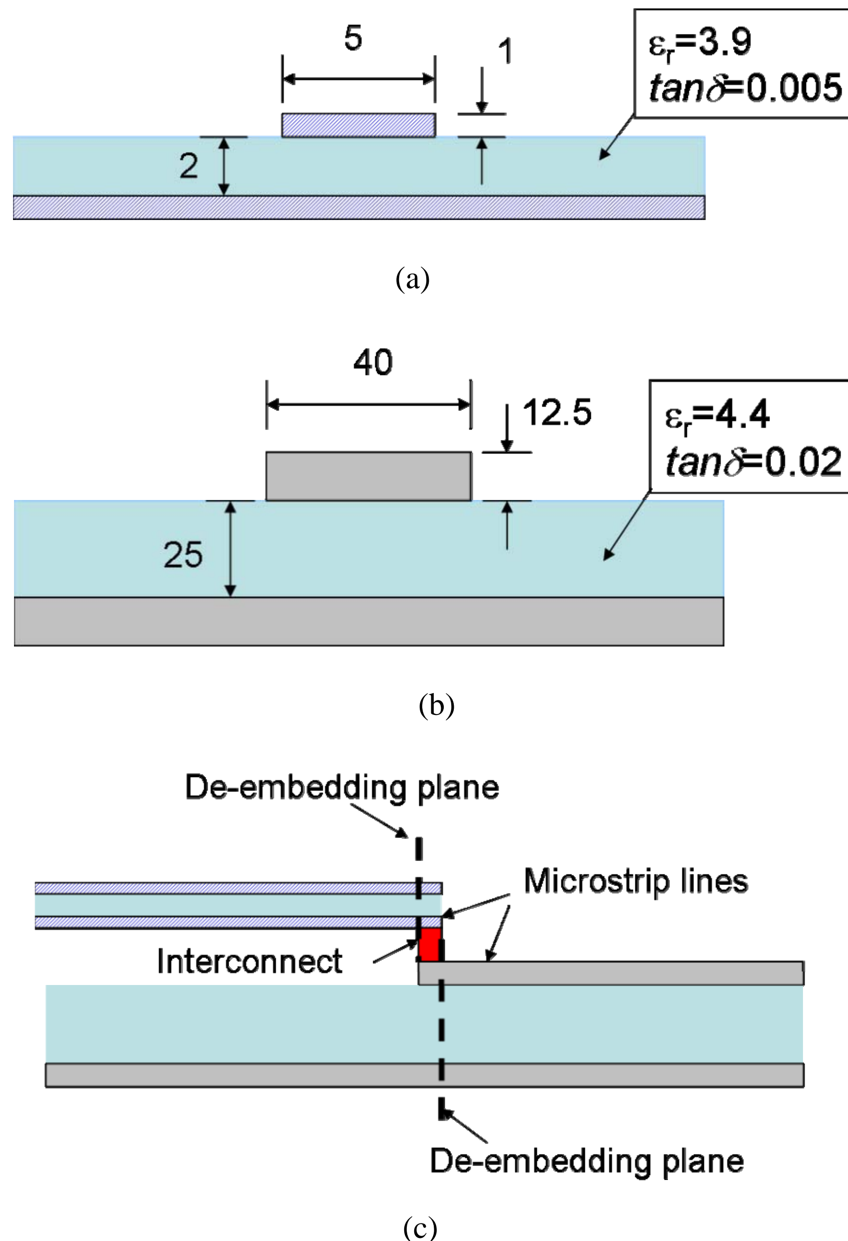


Fig. 2-5 Schematic of Ansoft's HFSS model for Planar Microspring Optimization (a) cross section view of microstrip line on chip; (b) cross section view of microstrip line on package substrate; (c) side view of simulation model (unit: µm)

assumed between the signal and ground plane on chip- and package-side, respectively. The conductors on chip- and package-side are assumed as Al and Cu, respectively, with the material properties same as shown in Table 2-1. Fig. 2-5(a) & (b) shows the dimensions of transmission lines, which were designed to give a characteristic impedence (Z_0) of ~50Ω at 5GHz. Finally, Fig. 2-5(c) shows the side view of the whole simulation model. De-embedding was conducted to extract the scattering parameters (*S*-parameters) associated with the Planar Microspring interconnects. It should be noted that, for the sake of simplicity, the Cu plug and the cavity in sacrificial layer (referring to Fig. 1-11) are not included in the model.

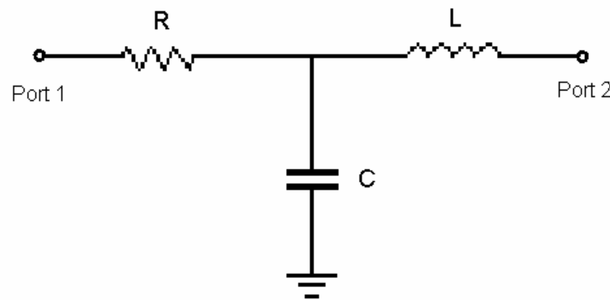


Fig. 2-6 Equivalent lumped circuit model for parasitic extraction

The *S*-parameters from HFSS simulation can then be converted into impedance parameters (*Z*-parameters) or admittance parameters (*Y*-parameters) using Hewlett-Packard's Advanced Design System (ADS). The interconnects considered here have stand-off heights (<20μm) much shorter than the signal wavelength (~3cm at 10GHz), therefore the transmission line effects can be neglected and an equivalent lumped circuit model such as Fig. 2-6 can be employed to represent the interconnect. According to *Y*, *Z*-parameter definition and 2-port network analysis, equations can be easily deduced as below to calculate the associated electrical parasitics (*R, L* & *C*):

$$R = -real\left[\frac{1}{Y(2,1)}\right] \quad \ldots\ldots \text{(2-10)}$$

$$L = -\frac{imag\left[\frac{1}{Y(2,1)}\right]}{2\pi f} \quad \ldots\ldots \text{(2-11)}$$

$$C = -\frac{1}{2\pi f \times imag[Z(2,1)]} \quad \ldots\ldots \text{(2-12)}$$

where f is the excitation frequency, "*real*" and "*imag*" refer to the real and imaginary part of complex numbers, respectively.

2.2.2 Superior Performance of MCC over SCC and C4 Interconnects

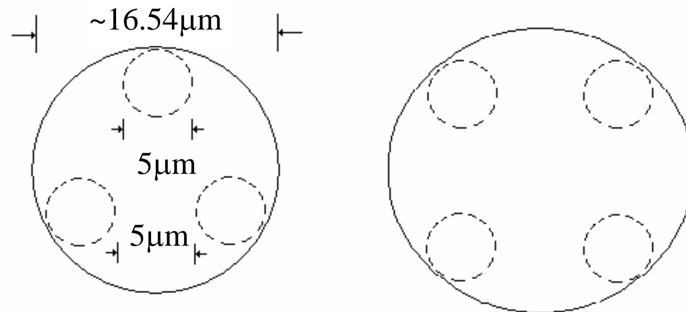


Fig. 2-7 Top view of SCC vs. TCC (left) and SCC vs. QCC (right)
(solid line:SCC; dashed line: TCC & QCC)

Since pure solder (i.e., controlled collapse chip connect or C4) and single copper column (SCC) interconnects have been available in the market, it is very important to justify the MCC interconnect concept by demonstrating its superior performance. For a fair comparison, the same wafer estate occupancy is assumed for MCC and SCC interconnects. In other words, an MCC interconnect can be imaged to be formed by removing portions of the Cu column in a SCC interconnect. As shown in Fig. 2-7, for instance, if the copper columns in a Triple-Copper-Column (TCC) interconnect are arranged in an equilateral triangular pattern with column radius of 2.5μm and centre-to-centre column spacing of 10μm, an SCC interconnect with copper column radius of

~8.27μm is employed for comparison. The same applies to Quadruple-Copper-Column (QCC) interconnects. The solder geometry remains the same for MCC, SCC and pure solder interconnects. The details of model geometry are shown in Table 2-2, where *H* and *R* represent the solder ball height and radius, *h*, *r* and *l* represent the copper column height, radius and centre-to-centre spacing, respectively. The compliances and electrical parasitics are calculated with the procedure as described in section 2.2.1.1 and 2.2.1.2, respectively.

Table 2-2 Interconnect geometry for performance comparison between MCC and SCC interconnects (unit: μm)

	TCC vs. SCC		QCC vs. SCC	
	TCC	SCC	QCC	SCC
Copper column	h=5, r=2.5,	h=5, r=8.27	h=5, r=2.5,	h=5, r=9.57
Solder ball	H=18, R=12.5		H=21, R=14.5	
Al pad on chip	25×25×0.5		25×25×0.5	
Cu pad on package	25×25×5		25×25×5	

Table 2-3 shows simulation results of TCC and QCC interconnects in comparison with their corresponding SCC counterparts. Note that the AC resistance and inductance are calculated at 100 MHz. Compared to SCC interconnects, the vertical and lateral compliances increase by 55% and 73%, respectively, for TCC interconnects, but the ratios fall to 41% and 59%, respectively, for QCC interconnects. On the other hand, most of the electrical parasitics of MCC interconnects are more or less increased when compared to SCC interconnects. For TCC interconnects, the DC resistance increases by 39% accompanied with a smaller increase of 34% in AC resistance. The differences reduce to 31% and 28%, respectively, for the QCC interconnect over its SCC counterpart.

Table 2-3. Performance comparison between MCC, SCC and pure solder joint interconnects

	TCC vs. SCC			QCC vs. SCC		
	TCC	SCC	SOLDER	QCC	SCC	SOLDER
Vertical compliance, μm/N	3.03	1.95	1.5	2.39	1.7	1.3
Lateral compliance, μm/N	16.4	9.48	7.24	12.7	7.99	6.33
Capacitance, fF	3.21	3.33	3.4	3.47	3.19	3.35
DC resistance, mΩ	11.37	8.17	7.74	9.31	7.08	6.64
DC inductance, pH	7.18	7.03	4.93	7.66	7.59	5.57
AC resistance, mΩ	14.25	10.63	9.88	11.82	9.27	8.54
AC inductance, pH	4.88	4.66	3.03	4.93	4.72	3.12

Considering the skin effect that leads to current concentration in the near-surface region of conductors, resistance at high frequencies becomes more dependent on surface area rather than volume. Therefore, it may be reasonably expected that, at higher frequencies, the electrical resistance of QCC interconnects may become comparable or even less than that of SCC interconnects. On the other hand, one can also see from Table 2-3 that inductance and capacitance of TCC and QCC interconnects are very close to their SCC counterparts. Based on these observations, it can be concluded that, without much loss in electrical performance, the interconnect compliances can be significantly improved by replacing SCC with MCC structures. Conventional pure solder ball interconnects without copper columns are also included in Table 2-3 for comparison. It can be observed that, even though the copper columns have a low aspect ratio of 1, the compliances are double that of the values for

conventional pure solder interconnects. In contrast, the increase of electrical parasitics is much less.

Table 2-4. Performance comparison between TCC and other compliant interconnects

	Lateral compliance, mm/N	Vertical compliance, mm/N	R, mΩ	L, nH	C, fF
Sea of Lead [25]	-	-	20	0.1	5.31
β-fly Helix [27]	11.2	14.6	52	0.069	-
G-helix [28]	9.068	10.149	43.63	0.08989	-
FlexConnects [29]	4.82	-	40.94	0.0365	-
TCC	0.016	0.003	11.37	0.007	3.21

Table 2-4 shows a performance comparison between TCC interconnects and two other compliant interconnects such as Sea-of-Lead and β–fly helix interconnects. The results of TCC interconnect are taken from Table 2-3, and all of the electrical parasitic data refer to the DC condition. It should be noted that the compliances of β–fly helix interconnect is evaluated without the presence of solder, while in this work the solder joint is included in the model for compliance calculations. The compliances of the β–fly helix are much higher than those of TCC interconnects, but this higher compliance is achieved at the expense of process complexity and much higher cost. On the other hand, the electrical parasitics of TCC interconnects are much lower than the other two interconnects.

2.2.3 Shape Optimization of Planar Microsprings

In this section, the simulation procedure as described in section 2.2.1.1 and 2.2.1.3 is employed to optimize the planar microspring shape in terms of compliance and

electrical parasitics. All the interconnect structures analyzed here are composed of 2 or 4 beams and the whole structure demonstrates 180° rotational symmetry. It is understood that a 1-beam structure, like cantilevers, shows higher compliances. However, this kind of structures is not employed here considering that: 1) cantilever-type structures intrinsically have higher electrical resistance than those with multiple beams that are electrically connected in parallel; 2) During wafer-level test, the cantilever-like interconnects may deform laterally when subjected to loading of the test probe. This will result in loose contact between the interconnects and test probe, and hence high contact resistance and compromise of the accuracy in testing. This drawback can be overcome by multiple beam design as illustrated in Fig. 2-8.

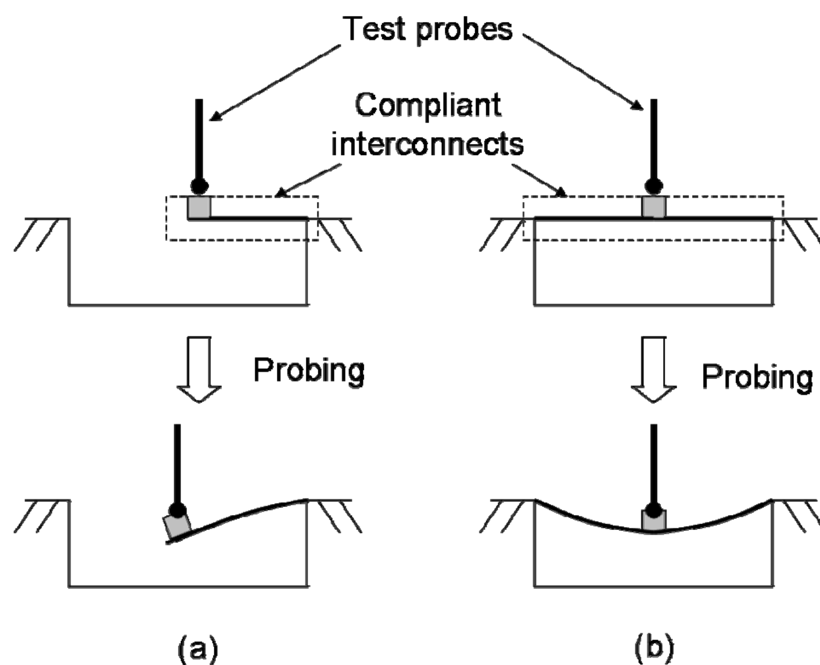


Fig. 2-8 Schematics of cantilever-like and multiple-beam Planar Microspring interconnects under probing

Fig. 2-9 shows six spring structure designs under evaluation. It is understood that there can be other microspring shape designs. For example, the straight segment of J-shape (as shown in Fig. 2-9 (f)) can be replaced by zigzag-shape beams to further

improve the compliance. However, this will clearly sacrifice electrical performance in terms of resistance. The general trend is that, the more complicated the structure

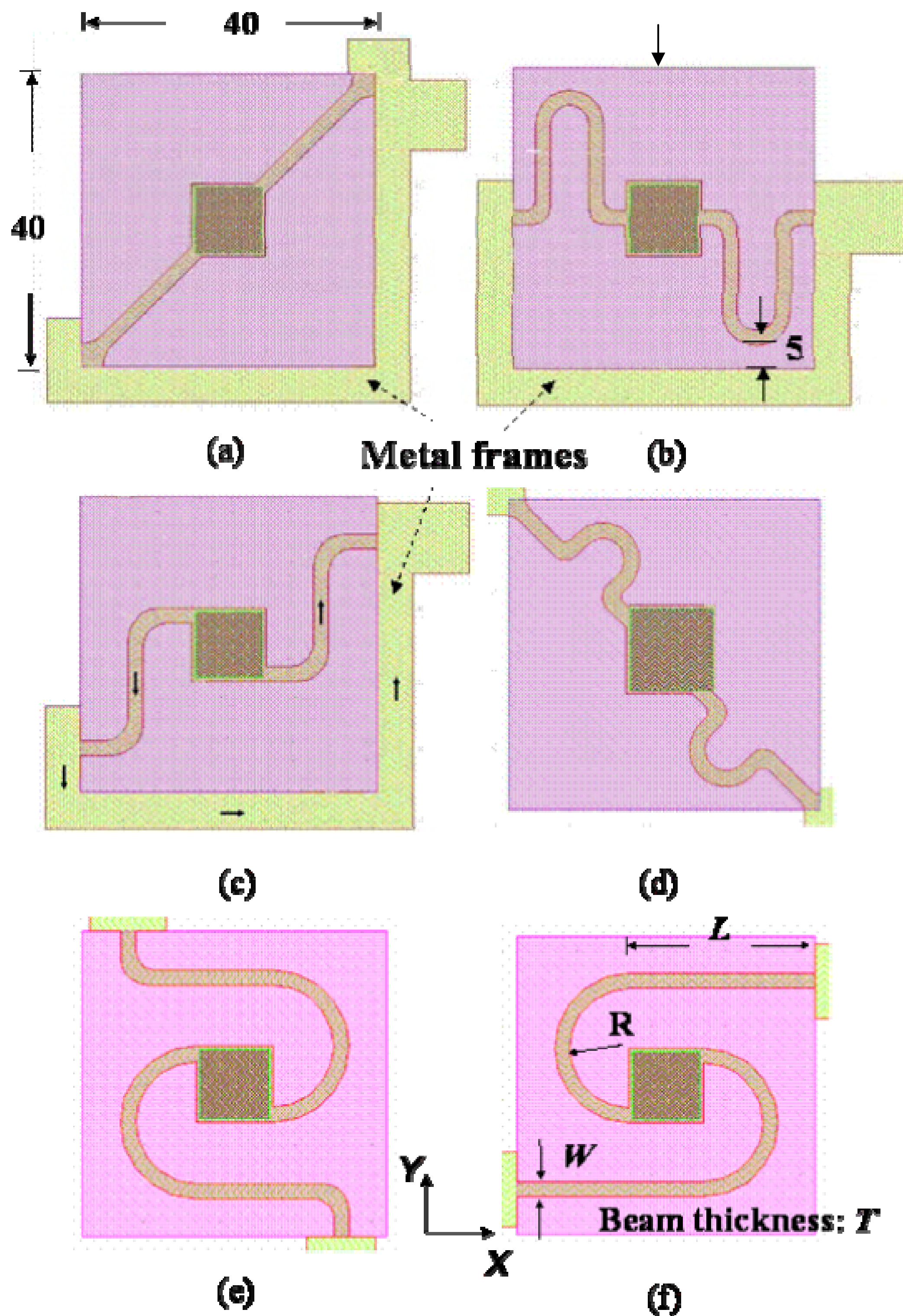
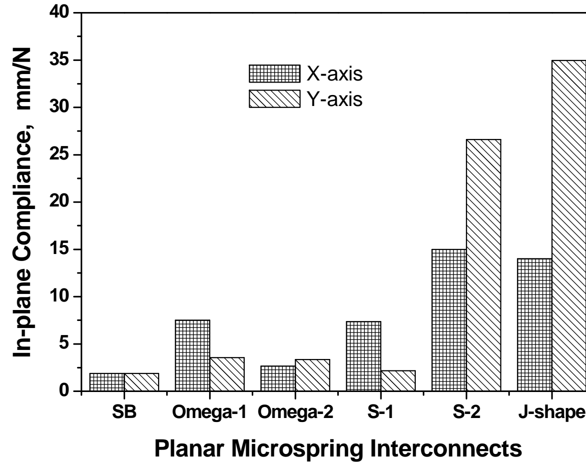


Fig. 2-9 Schematic of six planar microspring structures (a) simple beam (SB); (b) omega_1; (c) omega_2; (d) *S*_1; (e) *S*_2; and (f) *J*_shape (Not in scale, unit: µm)

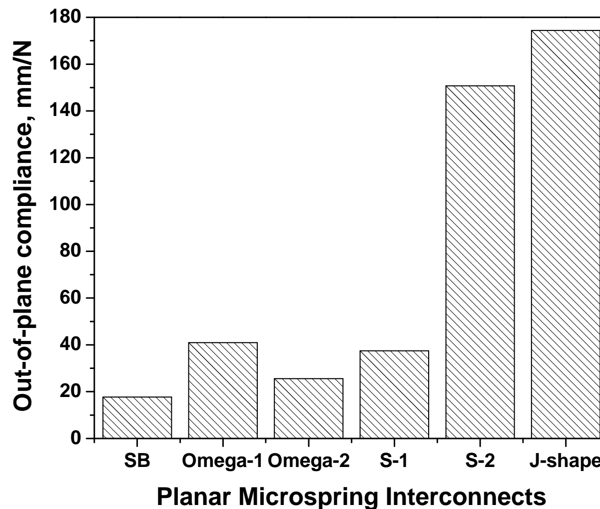
geometry, the higher mechanical compliance and as well the electrical parasitics. Therefore, in this thesis, only a few representative structures with similar geometry complicacy are taken for consideration. As shown in Fig. 2-9, all the spring structures are suspended over a 40×40μm^2 cavity, with a central pad of 10×10μm^2 and spring beams with both width and thickness of 2μm. For each shape, the springs are designed to achieve the maximum effective spring length within the design rule limits. For example, it was required by the fabrication process that there must be a ≥5μm spacing between the microspring beams and the cavity edge as illustrated in Fig. 2-9(b). In addition, the metal frames as shown in Fig. 2-9(a), (b) & (c) for example, are included in the electrical simulation models. The metal frames are arranged around the periphery of the cavity and electrically connect the microspring beams in parallel. The metal frames are made of electroplated Cu of 2μm thick, and their length is only dependent upon the count of microspring beams. Specifically, the metal frame was 80μm or 160μm long, respectively, in the case of 2- or 4-beamdesign. A double truncated solder joint with a height of 10μm and diameter of ~14.1μm is included for both compliances and electrical parasitics calculation.

Fig. 2-10 indicates that, for all designs with two beams, the J_shape design has the highest compliances in both horizontal and vertical directions, which is consistent with its highest effective length. On the other hand, electrical resistance demonstrated opposite dependence upon the structure length. As shown in Fig. 2-11(a), the J-shape and S_2 designs demonstrate the maximum electrical resistance. For inductance, the spacing between spring beams and that between beams and metal frames also contributed to the total inductance in the form of mutual inductance. Hence, the inductance was not only determined by the effective beam length, and the S-2 and omega-1 designs demonstrated highest inductance as shown in Fig. 2-11(b). One

should note that it was always preferred to avoid high inductance since it easily induces remarkable noise in the power plane and erraneous on/off operation of the digital IC. Finally, Fig. 2-11(c) showed that the SB, J_shape and S-2 designs have higher capacitance values than other designs.



(a)



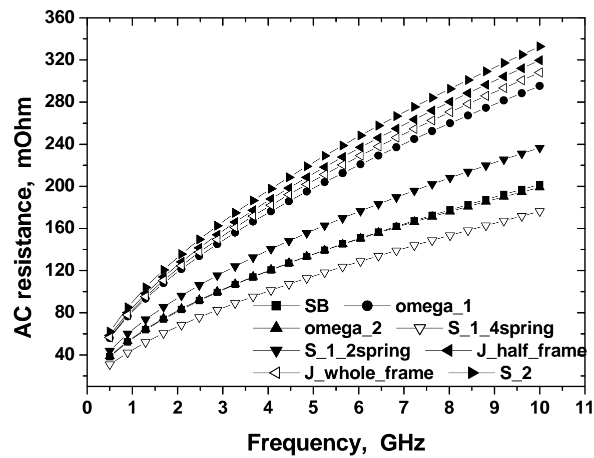
(b)

Fig. 2-10 Compliance comparison of various microspring structures (a) in-plane compliance; (b) out-of-plane compliance

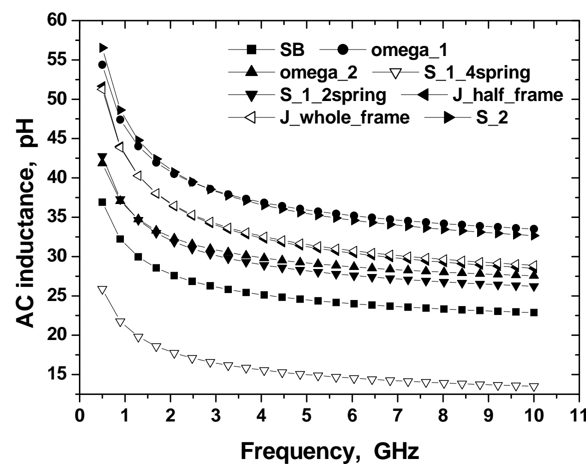
More design considerations have been taken for the metal frame and the spring count. For those interconnects including two springs, either a full or a half metal frame can be used without influence on the compliances. However, it can be seen

from Fig. 2-11(c) that for the J-shape structure, a whole metal frame introduces 17% more capacitance but negligibly less resistance compared to the half metal frame option. For some designs such as S_1, four springs can be used instead of two to reduce the electrical resistance and inductance at the expense of capacitance and mechanical compliance. In the design of these planar spring structures, a trade-off between mechanical compliance and electrical performance will have to be made. Furthermore, since all of these structures are not axis-symmetrical, caution must be taken while designing their orientation layout with reference to the chip in order to take the most advantage of the high compliances.

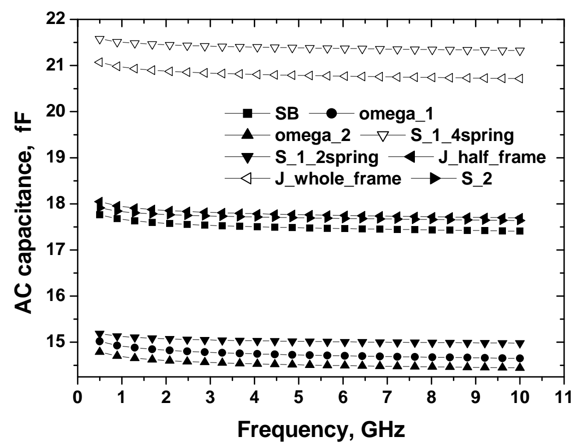
For interconnects such as planar microspring consisting of multiple parallel electrical paths, the different signal delay along multiple paths may potentially affect the signal fidelity. The wavelength of a single-frequency signal traveling in a medium with dielectric constant ε_r and relative permittivity μ_r is given by $\lambda = \left(2.998\times10^{8}\right)/\left\{f\sqrt{\varepsilon_r\mu_r}\right\}$, where f is the frequency in Hertz and λ is the wavelength in meters. Assuming the conductors are surrounded by air, the equation is simplified to $\lambda = \left(2.998\times10^{8}\right)/f$. It can be seen from this equation that the signal wavelength is inversely proportional to the frequency, and the signal wavelength is ~30mm when the frequency is as high as 10GHz. For both MCC and Planar Microspring interconnects, the length difference of parallel electrical path is quite small. Referring to Fig. 2-9, the maximum difference is 80μm for Planar Microspring since the cavity is 40×40μm^2 in dimension. This can be translated to a negligible phase shift of 0.96°. However, it should be noted that this phase shift can really affect the signal integrity when the frequency further increases. For example, if the signal frequency increases to 100GHz, the phase shift can be calculated as 9.6°, which may no longer be neglected.



(a)



(b)



(c)

Fig. 2-11 Electrical parasitics of various spring designs as a function of frequency (a) resistance; (b) inductance; and (c) capacitance

2.2.4 Parametric studies of compliant interconnects

2.2.4.1 MCC Interconnects

For an optimum MCC design, it is important to understand how the geometric parameters affect its mechanical and electrical behavior. Key geometric parameters specific to MCC interconnects are identified as column radius *(r)*, column height *(h)* and centre-to-centre column spacing *(l)*. The effects of these parameters on compliances and electrical parasitics are described below in terms of TCC interconnects. The simulation model as shown in Figs. 2-2 and 2-4 are taken for compliance and electrical parasitic calculation, respectively. For both cases, a double-truncated spherical solder ball has a radius of 22μm and a height of 31μm is adopted. Particularly, for electrical simulation, the Al pad on the chip side and the Cu pad on the package side have dimensions of $33\times33\times0.5\mu m^3$ and $33\times33\times5\mu m^3$, respectively. The simulation procedure described in section 2.2.1.1 is employed.

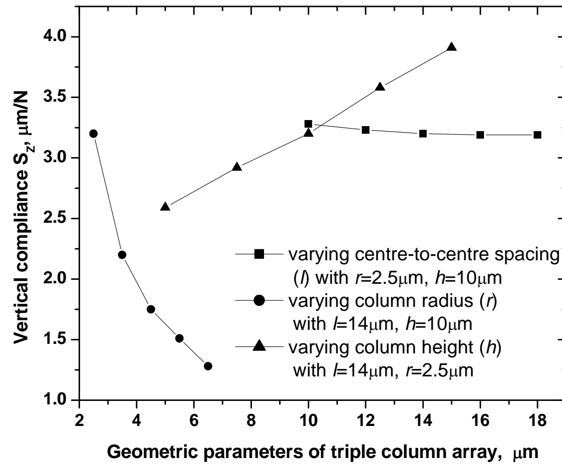
a) Geometric effects on compliances

As shown in Fig. 2-12, geometric parameters have different influences on compliances. Both vertical and lateral compliances can be enhanced by reducing column radius and increasing column height. The figure also illustrates that both vertical and lateral compliances are insensitive to centre-to-centre column spacing. Fitting the points in Fig. 2-12 with power law gives the lateral compliance ($S_{X\text{-}Y}$) of the TCC interconnects as a function of column radius (r) and column height (h):

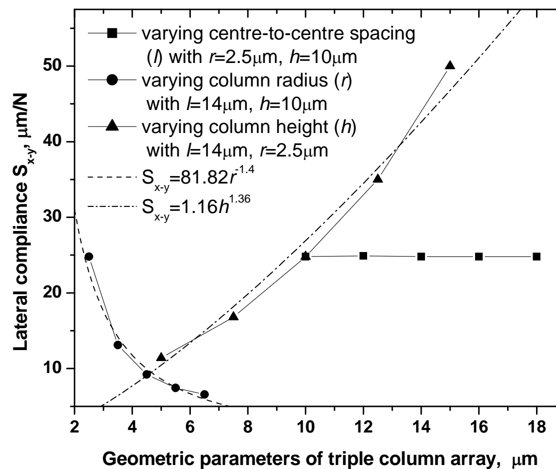
$$S_{X-Y} \propto Ar^{-1.4}h^{1.36} \quad \ldots\ldots \text{ (2-13)}$$

where A is a factor depending on the geometry of solder joint supported by the copper column array. It can be concluded from this equation that, for TCC interconnects, increasing the column radius is almost equal to decreasing the column height in terms of the lateral compliance. In comparison, the equation (2-3) shows that, for a single column, the radius has a stronger effect than the height upon the lateral compliance.

This discrepancy mainly arises from the fact that the coupling between the copper columns and solder joint is simplified in the analytical model.



(a)



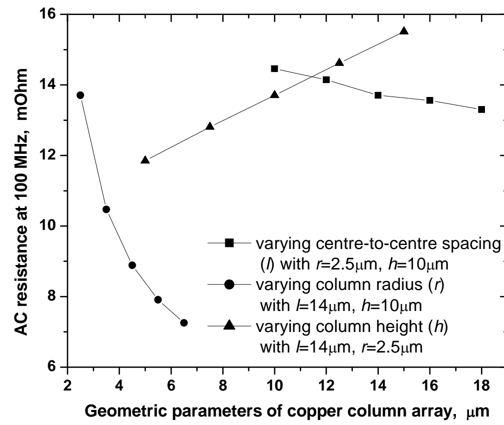
(b)

Fig. 2-12 Geometric effects of TCC interconnects on (a) vertical compliance; (b) lateral compliance

b) Geometric effects on electrical parasitics

As mentioned above, compliances of TCC interconnects can be enhanced by adjusting the geometric parameters, mainly decreasing column radius and increasing column height. From the electrical point of view, however, these adjustments may lead to inferior electrical performance. To make a reasonable trade-off between mechanical

and electrical performance, an understanding of the dependence of the electrical parasitics on geometry is required.



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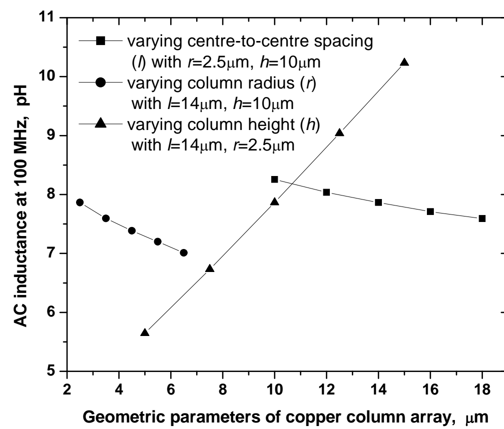

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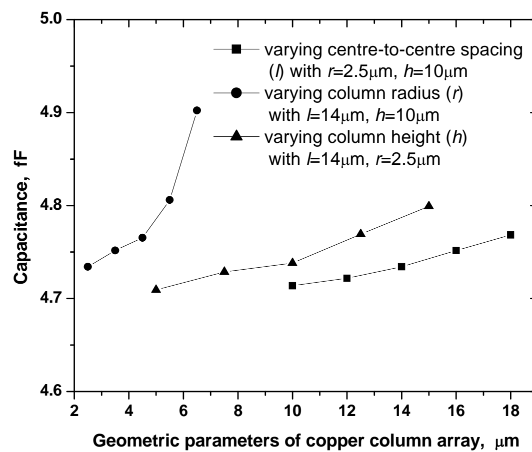


(c)

Fig. 2-13 Geometric effects of TCC interconnects on (a) AC resistance; (b) AC inductance and (c) capacitance

Fig. 2-13(a) shows the dependence of AC resistance on the geometric parameters. As expected, resistance increases with increase of column height or decrease of column radius. Interestingly, the resistance increases with decrease of centre-to-centre column spacing, which may be attributed to the proximity effect [43]. Since the current flows along the copper columns in the same direction, the magnetic fields induced by every column exert a repelling force upon each other, leading to less current density within the cross-section of the columns. Given the same column radius, the proximity effect abates with increase of column spacing, resulting in a larger effective cross-section for current and thus lower resistance. However, there should be a minimum resistance that corresponds to a critical column spacing where the proximity effect can be neglected. Recalling that the compliance of TCC interconnects are insensitive to column spacing, the column spacing can be adjusted to reduce the resistance without any reduction in the compliance.

Similar relationships can be observed in Fig. 2-13(b) with respect to the dependence of the AC inductance on geometry, while the DC inductance demonstrates similar geometry dependence and thus is not shown here. The total inductance of the triple copper column array consists of self-inductance of individual columns and mutual inductance between each other. Self-inductance is not affected by the column spacing, but mutual inductance decreases with the increase of column spacing. The net effect is that the interconnect inductance can be decreased by increasing the column spacing. The trend of inductance varying with the column array geometry is in accord with the analytical formula [44] for three conductors joined in parallel and symmetrical arrangement, which indicates that the inductance of such a conductor array at DC and low frequency condition can be calculated as:

$$L = 0.002h\left[\ln\left(2hr^{-\frac{1}{3}}l^{-\frac{2}{3}}\right) - \frac{11}{12}\right] \quad \ldots\ldots \text{ (2-14)}$$

The capacitance of the TCC interconnect is mainly dependent on its effective surface area where the current is distributed. As such, the capacitance increases rapidly with column radius but almost linearly with column height, as shown in Fig. 2-13(c). It is noted that the capacitance increases with the column spacing. According to the proximity effect as explained above, the effective surface area for current distribution increases with the column spacing, resulting in the increase of capacitance. Similar to the case of resistance, there should be a maximum capacitance that corresponds to a critical column spacing where the proximity effect can be neglected.

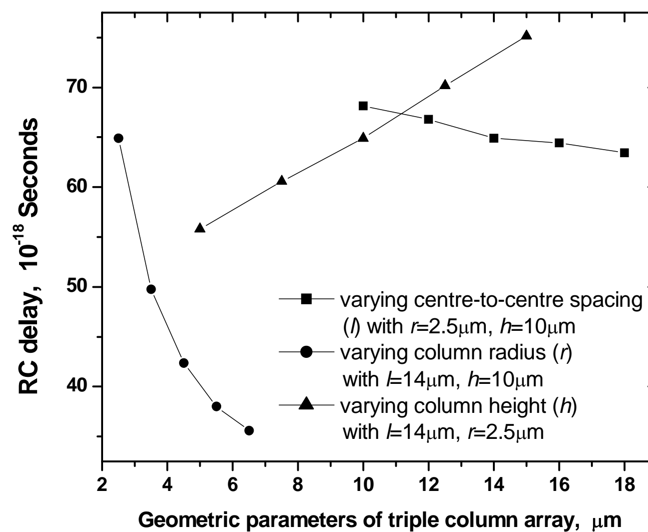


Fig. 2-14 *RC* delay of TCC interconnects varying with geometric parameters

At low frequencies, the inductive reactance of the TCC interconnect is negligible compared to resistance. Therefore, the signal delay associated with the interconnect can be approximately characterized with a series *RC* model, with the voltage across the capacitor as the input to the following transmission line or receiver. The time constant as shown in Fig. 2-14, which is expressed as resistance multiplied by

capacitance, reflects the rate at which the voltage across the capacitor increases to the steady value. Clearly, this *RC* delay can be reduced by increasing the column spacing, since the resistance decreases at a higher rate than the capacitance increases with the increase of column spacing. The delay also decreases with increase of column radius. On the other hand, the delay increases almost linearly with column height, in contrast with a greater-than-1 power dependence of lateral compliance on the column height as indicated by equation (2-13). This suggests that, with the column height increasing, the benefits in terms of the lateral compliance become more and more significant compared to the electrical degradation in terms of time delay.

Based on the above observations, it can be concluded that the centre-to-centre column spacing may be maximized to achieve better electrical performance without adverse effects on compliances, but a trade-off is generally needed between mechanical and electrical performance while designing copper column radius and height since they showed opposite effects on the compliance and electrical parasitics.

2.2.4.2 J_shape Planar Microspring Interconnects

a) Geometric effects on compliances

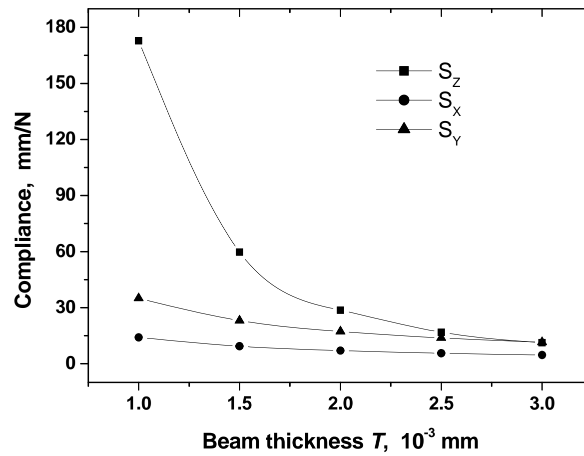
The three-dimensional mechanical compliance has been studied as a function of the spring geometry parameters in terms of J_shape microspring interconnects (inclusive of the solder joint) as shown in Fig. 2-9(f). Typical dependence of compliance on these parameters is presented in Fig. 2-15. It can be observed that the compliances decrease with increase of spring element thickness *T* and width *W*, particularly in the lower range of dimensions. In constrast, the influence of the other two parameters (*R* and *L*) is much less. Based on the simulation results, the 3-D compliances can be correlated to the geometric parameters by fitting with power law:

$$S_Z \propto W^{0.889} T^{-2.497} exp(0.152R+0.06L) \;\ldots\ldots\; (2\text{-}15)$$

$$S_X \propto W^{-2.436} T^{-1.004} exp(0.299R+0.011L) \;\ldots\ldots\; (2\text{-}16)$$

$$S_Y \propto W^{-2.816} T^{-1.013} exp(0.104R+0.083L) \;\ldots\ldots\; (2\text{-}17)$$

Hence, from the above equations it can be concluded that reduction of the spring thickness is most effective in enhancing the out-of-plane compliance, and narrowing the spring beams results in rapid increase of the in-plane compliance. It should be noted that, from the process point of view, thinning is much easier than narrowing of the spring beams.



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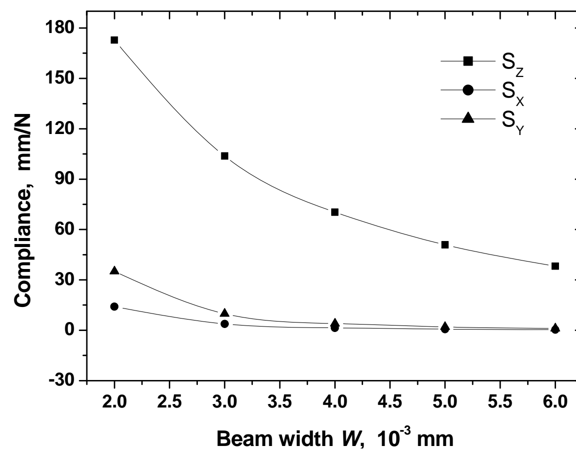

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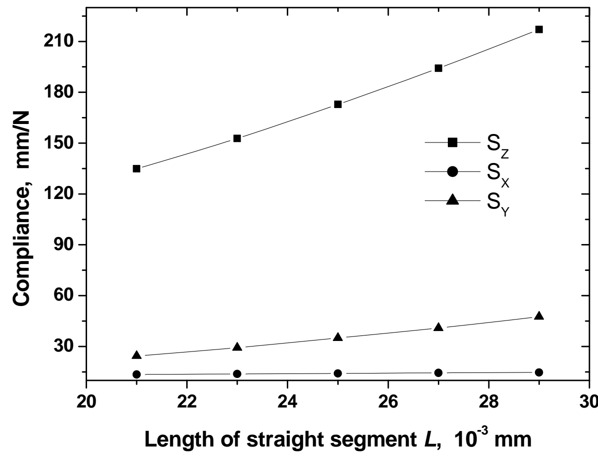

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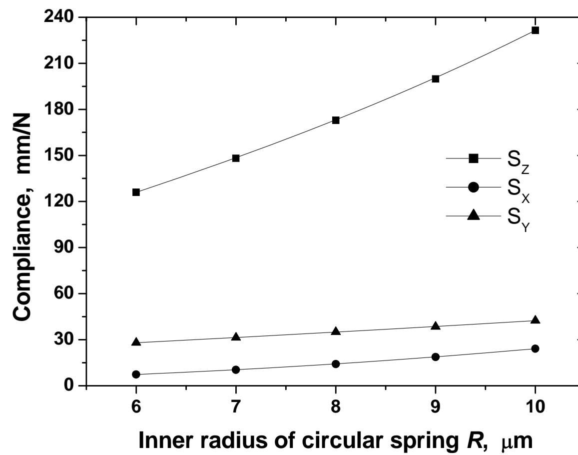
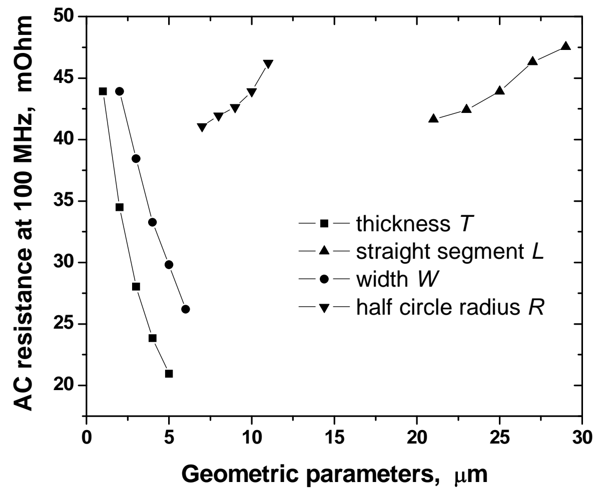


(d)

Fig. 2-15 Geometric dependence of *J*_shape interconnect compliances (a) spring thickness; (b) beam width; (c) length of straight segment; (d) inner radius of circular segment

b) Geometric effects on electrical parasitics

Effects of geometric parameters on electrical parasitics have been studied with Ansoft's Q3D for J-shape interconnects as shown in Fig. 2-16. As expected, the beam thickness *T* and width *W* show more significant influence on the resistance than the other parameters. The inductance shows inverse dependence on the beam thickness and width, which may be attributed to a combination of skin effect, proximity effect and the electrical current loop geometry. Finally, it can be seen that the beam width show much less effect upon the capacitance than the other geometric parameters.



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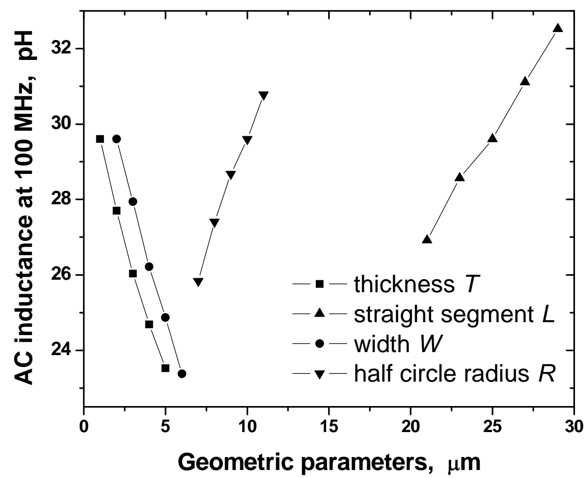

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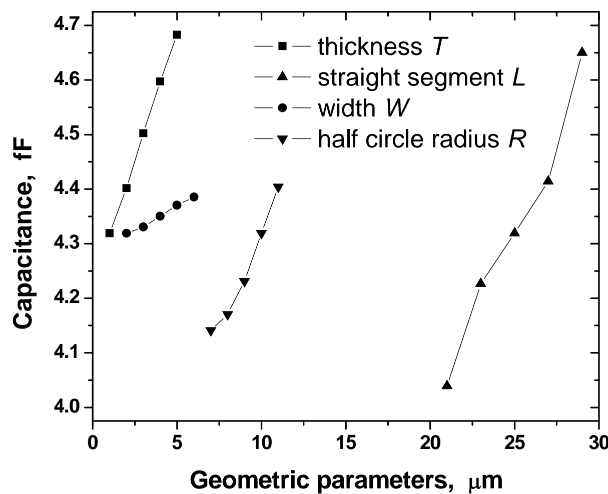


(c)

Fig. 2-16 Electrical parasitics of J_shape interconnect as function of geometric parameters (a) resistance; (b) inductance and (c) capacitance

Chapter 3 Wafer-level Fabrication of Compliant Interconnects

Fabrication processes and prototyping of compliant interconnects are presented in this chapter. First, we discuss about selection of appropriate materials and relevant process, which to a large extent decides the interconnect performance and cost-effectiveness of the fabrication process. In the second section, detailed process information will be provided for both MCC and Planar Microspring interconnect, respectively.

3.1 General considerations: Materials and Processes

The compliant interconnects developed in this thesis target at high I/O density application for wafer-level packaging, which imposes demanding requirements on material properties and process integration. On one hand, the interconnect size must be scaled down to meet the high I/O density requirement, which however may result in increase of electrical resistance. Therefore, the compliant interconnects should be preferably made of materials with excellent electrical conductivity. From the mechanical point of view, the non-solder part of the compliant interconnects must have good flexibility in order to reduce the strain deformation on the solder joint. This can be achieved by choosing low-modulus materials or optimization of the structure geometry as shown in Chapter 2. On the other hand, wafer-level fabrication requirement further limits material selection to those that can be applied and patterned by standard Si processing technologies. Both materials and relevant processes are preferably compatible with CMOS back-end-of-line (BEOL) processes. In the

following sections, discussion of materials and process will be made on columns of MCC interconnects, cavity formation for Planar Microspring interconnects, and solder joints for both interconnects, respectively.

3.1.1 Column-related Considerations for MCC Interconnects

The columns of MCC interconnects can be made of pure metal or composites with non-metal core and metallic coating [45]. The composite column concept is quite attractive for compliant interconnect application, since the flexibility of interconnects can be significantly improved if the core is made of soft polymeric materials. Furthermore, the electrical performance in high frequency range is not degraded, because the electrical current is concentrated to the interconnect surface (i.e., skin effect) and hence the metallic coating is able to complete the same function as the pure solid metallic column. It could be projected that, however, the electrical resistance of composite interconnect at low to middle frequency range is still much higher than the pure metallic one. More concerns come with respect to the reliability. In one aspect, the composite interconnect consists of materials with different thermal expansion coefficient, which under thermal cycling and/or power cycling will induce thermal stress and strain at the material interface. Therefore, the metallic coating may finally delaminate from the non-metallic core and finally results in open circuit. In another aspect, at low and middle frequency range, because the electrical cross section area is small, the electrical current density is high for composite interconnects and then results in serious electromigration. Both mechanisms may lead to shorter service life of composite interconnects compared to conventional pure metal interconnects.

While the composite interconnects are still in quite early research stage, pure metallic columns have been used in practice for several interconnects like Wire

Interconnect Technology (WIT) [46,47] and *Super*CSP [35]. Copper is mostly used for the columns (and any other structures for compliant interconnects) because of the following advantages: 1) copper has higher electrical conductivity than any other metals commonly used in IC industry; 2) copper demonstrates good thermal conductivity; 3) copper demonstrates good plasticity that means a large amount of deformation energy of the interconnect can be absorbed by the columns; 4) copper can be easily deposited by electroplating which is a low-cost and high-throughput batch process; 5) copper has been conventionally used as Under Ball Metallization (UBM) layer and its reaction with Sn-based solder has been well understood.

With a target of less than 100μm pitch for MCC interconnect, the biggest challenge is how to fabricate high-aspect-ratio Cu columns with narrow spacing. The best solution lies in the combination of high-resolution patterning technique and electroplating, of which the former results in high-aspect-ratio vias and the latter results in void-free metal filling of the vias. For via fabrication, a reasonable depth is desired to enable formation of slender Cu column, and also to effectively reduce solder-related soft error. Small via diameter and spacing are required to achieve fine pitches for interconnects. For metal filling of vias, both damascene and bottom-up electroplating can be applied. However, damascene electroplating is usually conducted on inorganic dielectrics such as SiO_2, which in this case means that a very thick layer of SiO_2 has to be deposited. The resultant disadvantages in process integration include high stresses associated with thick SiO_2, expensive Chemical Mechanical Polishing (CMP) process to remove extra Cu, and time-consuming removal of thick SiO_2. In contrast, bottom-up electroplating can be easily applied to fill vias in polymeric materials. No CMP is required and even thick polymer usually

can be quickly removed using a solvent. The comparison of these two schemes is illustrated in Fig. 3-1.

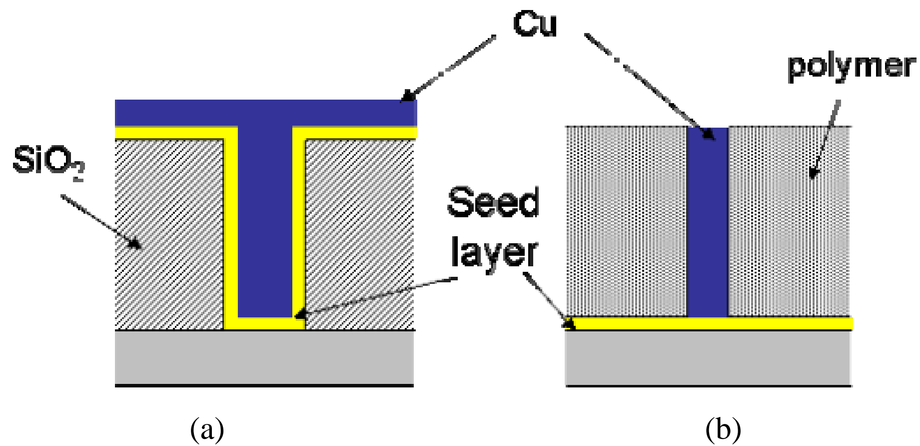


Fig. 3-1 Schematics of (a) damascene and (b) bottom-up electroplating for via filling

Photolithography can be applied to photo-imagible polymers to directly realize holes for electroplating. In this way, vias with aspect ratio of up to 2 can be formed in some thick photoresist or dry films, but the application of these materials is plagued by issues such as removal difficulty. For example, a negative tone photoresist, namely SU8, has been widely used for molding and MEMS application. It has been reported [48] that high-aspect-ratio (10~20) microstructures can be directly defined by photolithography, but the material can hardly be fully removed once exposed to Ultra Violet (UV) light. In another way, dry etching methods such as Deep Reactive Ion Etch (DRIE) can also be used for via formation in polymers. This method usually enables vias of higher aspect ratio than photolithography. For example, very-high-aspect-ratio vias have been realized in Si-containing polymer Benzocyclobutene (BCB) by using plasma mixing O_2 and fluorine gas [49]. The disadvantages of this method include low throughput, high cost associated with additional mask and the deep etching process itself.

The difficulty of solid via filling increases with the aspect ratio. First, for high-aspect-ratio vias, because of the surface tension and hydrophobic nature, it is hard for the electroplating chemical to go down to the bottom of the vias, which manifests itself as partially plated or even non-plated vias. Secondly, even if the chemical goes down to the via bottom, it cannot be fully replenished because of the great depth of the vias. This may manifest itself more clearly as a uniformity issue across the wafer. For example, the flow rate of the electroplating bath may be faster at the wafer edge than the center region, and thus the vias at the edge often see a fresher bath than the center, which ultimately translates into over-plated edge region while the center region is still under-plated.

3.1.2 Cavity-related Issues for Planar Microspring Interconnects

For Planar Microspring interconnects, the most critical process lies in the formation of the cavity, which finally enables the microspring beams with high 3-D compliances. The cavity is formed by etching off the sacrificial materials under the microspring beams. From the interconnect compliance point of view, a thicker sacrificial layer is preferred, since this thickness determines the maximum allowable displacement of the interconnect in vertical direction. On the other hand, the electrical crosstalk between neighboring Planar Microspring interconnects, and also that between Planar Microspring interconnect and the final on-chip global interconnections increase with the dielectric constant of sacrificial material, therefore a low-κ material is preferred. It is noted that many polymer materials can be easily spin-coated with thickness of up to tens of micrometers, and also their dielectric constants are lower than those of many inorganic materials.

To release the microspring beams, the underneath sacrificial materials have to be removed by isotropic etching. The undercutting feature of wet etching can be utilized for in-organic materials like SiO_2. In contrast, isotropic patterning of polymeric materials is usually achieved by dry etching, in which the plasma conditions like pressure, gas flow rate and power must be carefully manipulated.

3.1.3 Solder-related Issues

For both MCC and Planar Microspring interconnects, a solder joint on top of the flexible structure is preferred because of its self-aligning property. This property means that, in a molten state, the solder at the package and chip sides tends to attract each other due to the surface tension. Therefore, a larger misalignment during assembly can be accommodated. Solder materials can be categorized according to their composition: lead-containing and lead-free. Table 3-1 shows common solder materials used in IC packaging. The lead-free solders are gradually replacing the lead-containing counterparts due to environmental concerns. However, the melting points of lead-free solders are usually higher than Pb-Sn solders, which thus introduces higher thermal shock to the IC device during assembly process and, in extreme cases, may even exceed the glass transition temperature (T_g) of some polymeric substrates. In this work, eutectic 37Pb-63Sn solder was used considering its low cost, ease of assembly and manufacturing.

Solder is usually applied by either electroplating or screen printing. In the former case, an alloy with the targeted composition is employed as the anode. For eutectic 37Pb-63Sn electroplating, the advantage is that the process window of current density is much broader than other metals such as Cu. For screen printing, a screen with though-hole patterns of a certain size must be pre-formed. Solder paste is placed at

one end of the screen aligned to the wafer. Then, the solder paste is spread from one end to the other end by a squeegee, and thus solder is squeezed through the holes and deposited on the wafer. The process is highly dependent on the through-hole design and pushing speed. The screen printing process is low-cost and high through-put. However, it is usually applicable to solder joints of relatively large sizes and pitch of over 200μm. In this work, electroplating is the only available choice since the solder joint size is targeted at 10~20μm.

Table 3-1 Property and cost comparison of eutectic Sn-Pb solder and some popular lead-free solders [50]

Property	Sn-37Pb	Sn-3.5Ag	Sn-3.5Ag-0.7Cu	Sn-3.8Ag-0.7Cu	Sn-0.7Cu
Density, g/cm^3	8.4	7.5		7.5	7.3
Melting point, °C	183	221		217	227-240 [51]
Electrical resistivity, μΩ·cm	14.5		12.3		13
Young's modulus at 20°C, MPa	30.2	56GPa [52]			
Tensile strength at 20°C, N/mm^2	40	58	48	48	
Joint shear strength at 0.1mm/min, 20°C, N/mm^2	23	27		27	20-23
Cost, US$/cm^3	0.046	0.142			0.056

At the initial stage of this work, customized simple set-up as shown in Fig. 3-2 has been established for 63Sn-37Pb solder electroplating. Both electrolyte solution and 63Sn-37Pb anode come from *Schloetter Plating Technology, Germany*. A specific

grain refiner ingredient is present in the electrolyte solution and is responsible for growth of fine-grain solder. Constant-current power supply is employed for electroplating since the plating rate is dependent on current density magnitude. Separation distance between anode and cathode is maintained at ~10 cm. Electroplating is conducted at room temperature and no stirring is applied.

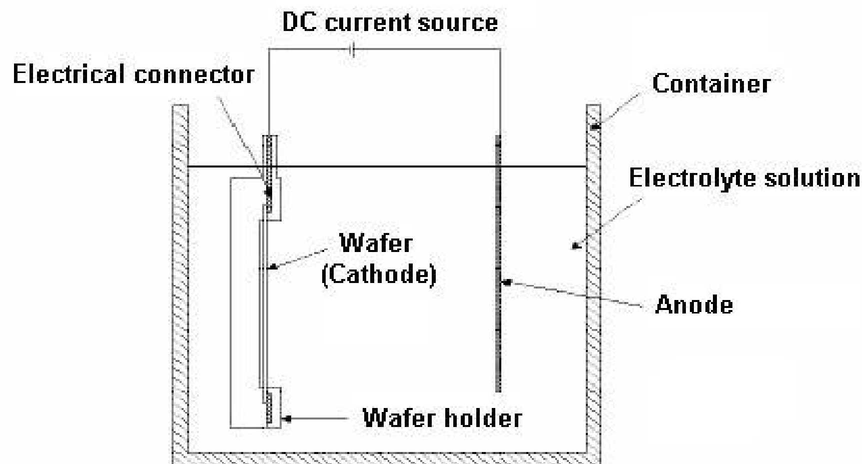


Fig. 3-2 Schematic of solder electroplating set-up

Calibration is conducted to find the plating rate as a function of the current density. According to Faraday's law [53], the amount of deposited material is a function of the current passing through the electrode interface and proportional to the chemical equivalent weight of the material, which can be represented in mathematical form as:

$$M = \frac{\alpha I t A_w}{nF} \tag{3-1}$$

where M is the mass of the deposited material, α is current efficiency at the cathode, I is the current, t is the duration of electroplating, A_w is the atomic weight of the deposit, n is the number of electrons transferred per atom in reduction reaction, F is Faraday's constant and equals to 9.65×10^4 C/mole.

By rearranging the above equation, the plating rate can be related to current density as:

$$r = \frac{\alpha A_w}{nF\rho} \times j \qquad (3\text{-}2)$$

where r is plating rate, ρ is density of the deposit and j is current density. The meanings of other symbols are the same as above. It can be observed that the plating speed is proportional to current density for a specific plating system. Fig. 3-3 shows that the measured plating rate linearly increase with current density ranging between 1~2 A/dm^2. A current density of ~1.5 A/dm^2 was finally selected for solder electroplating.

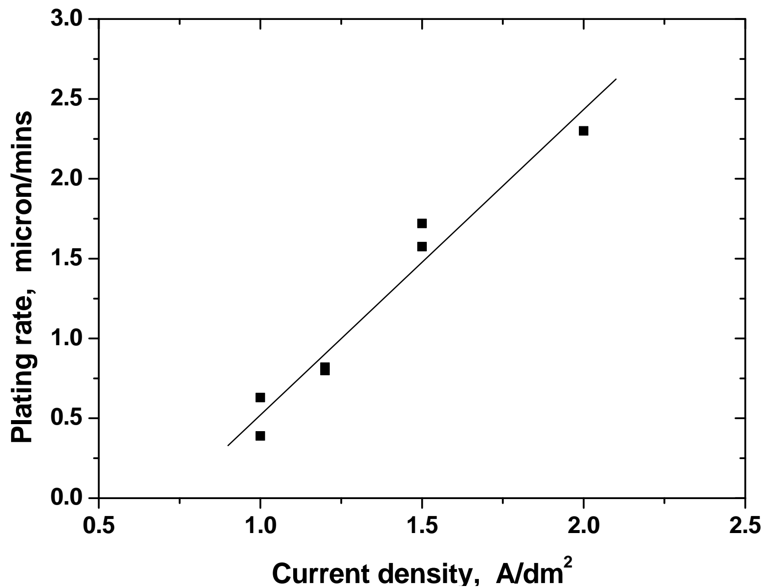
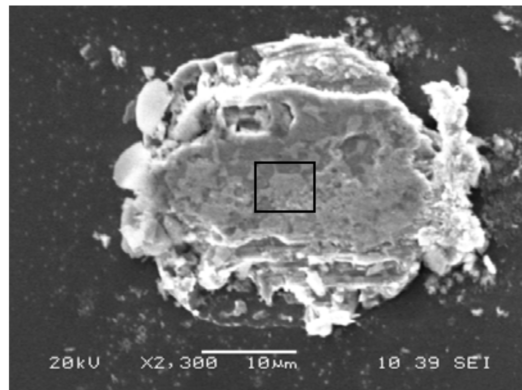


Fig. 3-3 Relationship of solder electroplating rate vs. current density

For both MCC and Planar Microspring interconnects, solder joints are directly grown on top of structures made of Cu. To evaluate the solder-Cu interface strength, eutectic 63Sn-37Pb solder bumps of 36×36×15μm^3 were prepared on Ti/Cu seed layer by electroplating with a plating current density of 1.5 A/dm^2. The solder-Cu interface

strength was characterized on a DAGE BT24 Shear Tester. During testing, a shear probe pushes the solder ball with a pre-defined speed (5 μm/s) until failure of solder ball joints occurs. The maximum loading force is recorded as the shear force. Several solder ball failure modes may be identified such as ball shear, pad lift and ball lift etc. Ball shear is the desired failure mode since it implies strong adhesion between solder ball and the under ball metallization (UBM) layer. Testing of 40 solder balls distributed across a 6” wafer revealed an average shear force of about 35.3mN with a standard variation of 0.07. A topological observation of the shear failure site as shown in Fig. 3-4(a) revealed that ball shear was the dominant failure mode, which was further confirmed by energy diffraction X-ray (EDX) analysis as shown in Fig. 3-4(b) where only Pb and Sn elements were detected.



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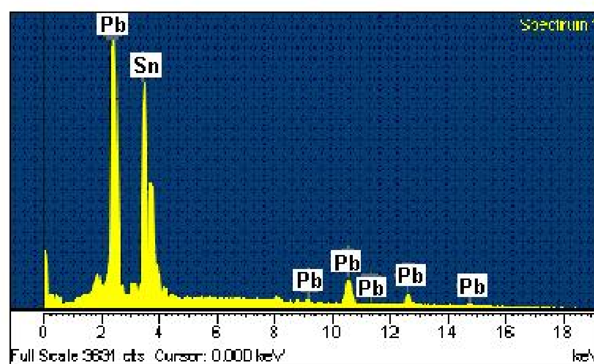


(b)

Fig. 3-4 (a) SEM photo of solder ball failure site, and (b) EDX analysis result

3.2 Wafer-level Fabrication of Compliant Interconnects

3.2.1 MCC Interconnects

3.2.1.1 Process Flow

Fig. 3-5 illustrates the process flow for MCC interconnects, which starts from a Si wafer with passivation layer (e.g., SiO_2) and exposed contact pads (Al or Cu). The wafer as shown in Fig. 3-5(a) mimics a real device wafer with final passivation and

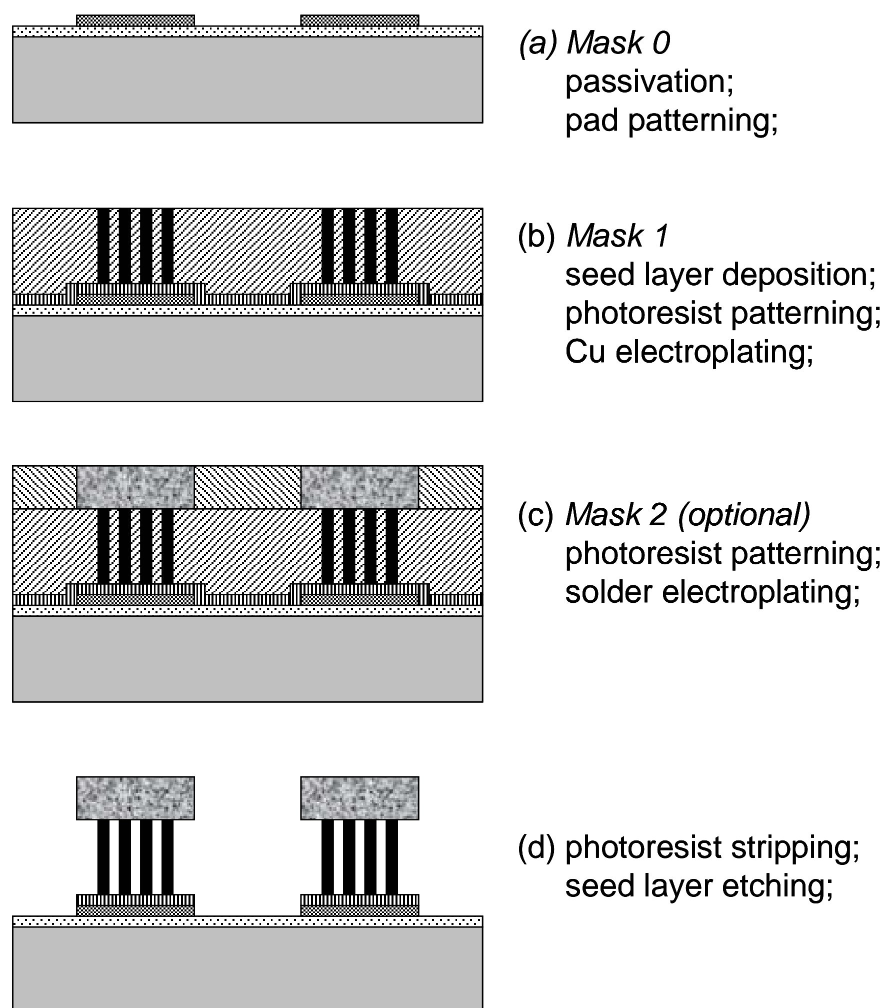


Fig. 3-5 Process flow of MCC interconnects

exposed metal pad. Fig. 3-5(b) shows that a conductive layer is then deposited on the wafer, which acts as the seed layer for the following electroplating process. The seed

layer usually consists of double metallic layers: adhesion/diffusion barrier layer on the bottom, and a more conductive layer on the top. In IC fabrication, Ti is widely used for adhesion improvement, while Ta and TaN are used for the same purpose but also as a barrier layer for Cu diffusion. In this work, Ti is used as adhesion layer because of ease of processing. For Cu electroplating, sputtered Cu or Au is commonly used as the top seed layer. Cu has the obvious advantage of lower cost and compatibility with CMOS back-end-of-line (BEOL) process. However, for MCC interconnects, the thickness of Cu seed layer has a narrow allowable range, because a too thin Cu layer is easily etched away in the SO_4^{2-}-based Cu electroplating bath, while a too thick Cu seed layer is difficult to be removed in the following process without attacking the slender Cu columns. In contrast, a thin Au layer is a better choice because of its good electrical conductivity and chemical resistance.

As shown in Fig. 3-5(b), a photoresist layer is then spin-coated on the wafer and patterned to realize the vias for electroplating. The thickness of this photoresist layer defines the height of copper columns, while the via size and spacing define the diameter and spacing of the copper columns. In the bottom-up electroplating process, copper columns are grown up from the exposed seed layer region till they are flush with the photoresist surface, which is controlled by the plating time. Fig. 3-5(c) shows that, without stripping the first photoresist layer, a second photoresist layer can be applied to define the solder electroplating window, which determines the solder bump area, height and thus the volume. In the case that the spacing between neighboring MCC interconnect is large or the required solder volume is small, the second masking process may be skipped.

It should be noted that, if two photoresist layers are used to define overlapping patterns, caution must be taken to select photoresists with appropriate polarity. Fig. 3-

6 shows four different scenarios. Shown in Fig. 3-6(a) is the worst case, where positive photoresist is used for both layers. It could be projected that, the patterns of bottom positive photoresist may be more or less damaged by the UV exposure and developing process of the top positive photoresist layer, therefore the following electroplated solder profile is affected. In the case of negative photoresist is used for both layers as shown in Fig. 3-6(b), the pattern region of bottom photoresist is only subjected to additional developing process, which however still probably damages the bottom photoresist. These problems can be avoided if photoresists with complementary nature are used. In Fig. 3-6(c), the bottom positive photoresist in the pattern region is able to survive the developing process of the top photoresist, because of its original polymerized chemical structure. In Fig. 3-6(d), the bottom negative photoresist in the pattern regions is even further polymerized during the UV exposure of top photoresist, and hence its survival chance through the lithography of top photoresist is improved. Other than the polarity consideration, selection of photoresist also depends on availability of resists with required thickness and resolution.

After solder is deposited by electroplating, the single or double photoresist layers can be removed by photoresist stripper or acetone. Occasionally, the first photoresist layer may not be fully removed since the column spacing is too small and the surface tension of the liquid chemical prevents itself from penetrating into the gaps between columns. In this case, dry etch method like O_2 plasma can be used. It should be applied in a short time (~1 minute), however, so that the copper column is not severely oxidized. Finally, the seed layer is etched to complete the whole process.

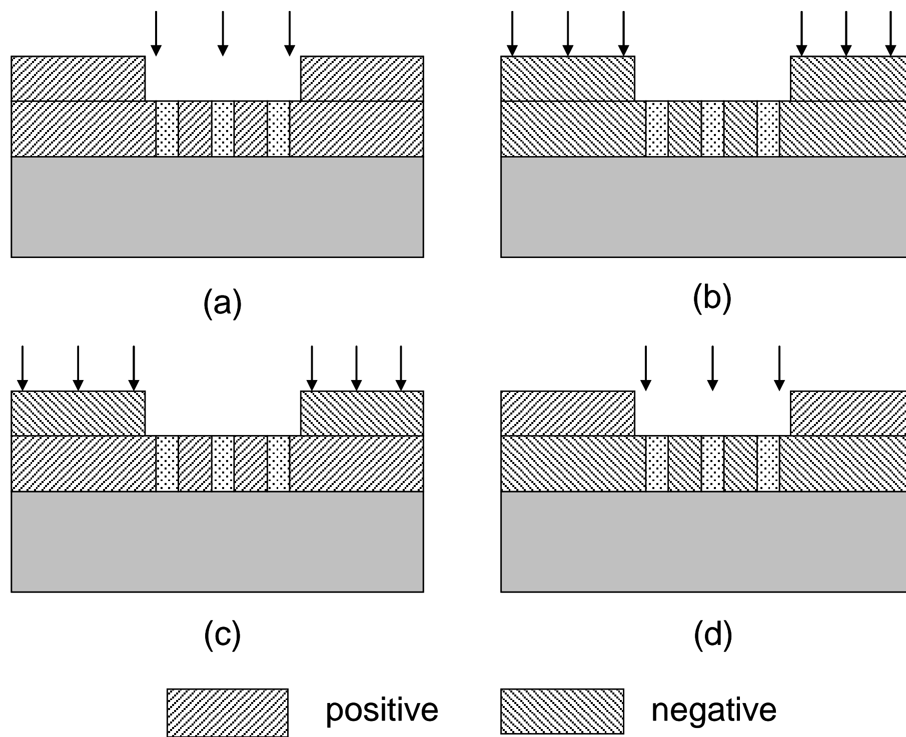


Fig. 3-6 Four scenarios of sequential photolithography process (a) positive resists for both layers; (b) negative resists for both layers; (c) positive resist for bottom layer and negative resist for top layer; (d) negative resist for bottom layer and positive resist for top layer

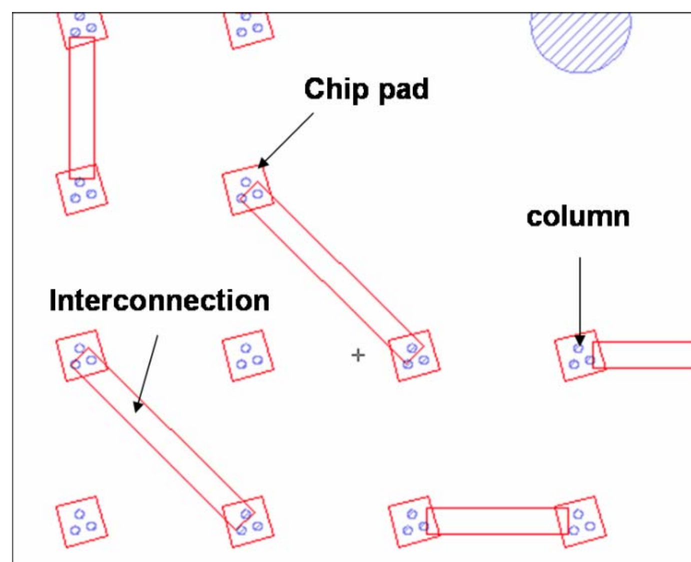


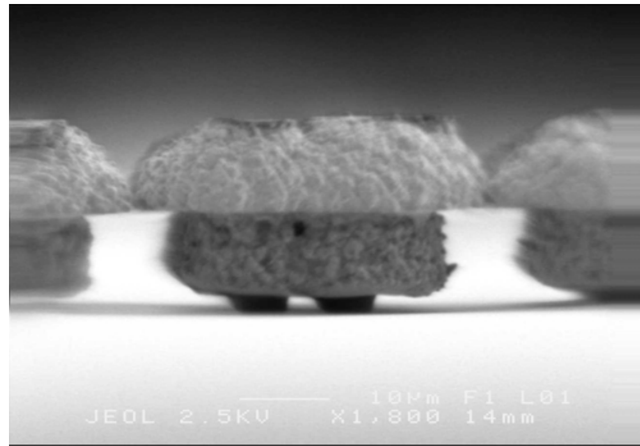
Fig. 3-7 Layout of test masks for MCC interconnects

Fig. 3-6 shows that only two or three photomasks are involved in the MCC interconnect process. However, the chip pad mask *(Mask 0)* is used for defining the on-chip metal pad, which is usually completed in the IC fabrication process. As explained previously, the solder mask *(Mask 2)* can be optionally skipped in certain cases that strict control of solder profile and volume is not needed. Therefore, the whole process for this wafer-level MCC interconnects may require only one additional mask. Fig. 3-7 shows a drawing of two masks for chip pad and Cu columns.

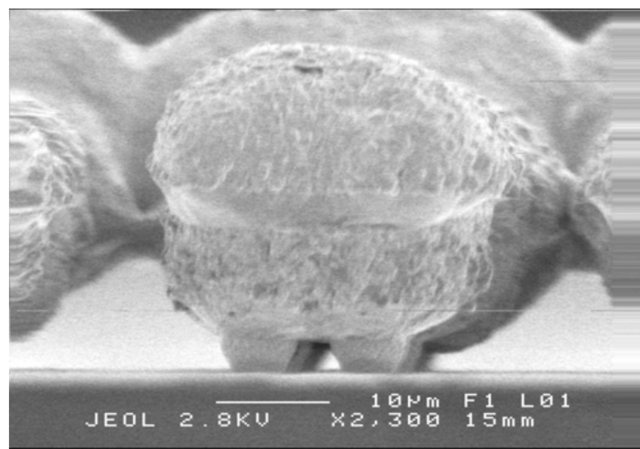
3.2.1.2 Phase I: Low-aspect-ratio MCC Interconnects Prototyping

Starting with patterned dielectric layer (SiO_2) and metal (Cu) pad, low-aspect-ratio (~1) MCC interconnects are first fabricated. A seed layer of 200Å Ti and 500Å Au is sequentially deposited by sputtering. A PFI-27C9 positive photoresist layer of 5μm thick is then spin-coated and via patterns are made through the photoresist with *MASK 1* by contact photolithography. Copper column arrays are grown in the holes by electroplating with the copper column in level with the photoresist layer.

Without stripping the first positive photoresist layer, another negative MA-N490 photoresist layer of 6μm thick is spin-coated and patterned with *MASK 2*. This step defines the window for solder plating. Finally, both photoresist layers are stripped away in PRS3000 photoresist stripper. Two wet etching recipes have been used to etch the Au layer. One chemical is made by dissolving 2.5g KCN and 2.5g Entreat 100 salt powder [54] in 1 liter DI wafer that is pre-heated to 50°C. There are also non-cyanide Au etchants such as Transene's TFA [55], which is an aqueous solution of 3% iodine and 42% potassium iodide. Etching with both etchants is conducted at room temperature. However, the selectivity of both etchants over Cu is not high enough and as a result the delicate Cu columns are partially or totally etched away.



(a)



(b)

Fig. 3-8 Quadruple-copper-column (QCC) interconnects (a) as-plated; (b) after solder reflow

Sputtering etch by N_2 plasma is finally selected for this purpose. Clean removal of Au is achieved without loss of Cu column, but accompanied with the penalty of low throughput. One hour is needed to remove 500Å Au at 100mTorr, 300W and total N_2 flow rate of 46sccm. The 200Å Ti layer can be either stripped away in wet etchant (Ethyleneglycol:HF=3:1) in 1 minute or in a 30%CF_4+70%O_2 plasma at the condition of 100mTorr, 300W and total flow rate of 20sccm.

Fig. 3-8(a) shows a SEM photograph of as-fabricated quadruple-copper-column (QCC) interconnects. The as-plated solder shows a mushroom shape because of over-plating. After reflowing at peak temperature of 235 °C as shown in Fig. 3-9, the solder

bump transforms into ball shape and the spacing between neighboring interconnects can be clearly observed as shown in Fig. 3-4(b). The sloped profile of copper columns arose from imperfect patterning of the photoresist PFI-27C9. It should be noted that the center-to-center interconnect pitch is 40μm, with a nominal diameter of 5μm for a single column and spacing of 5μm between columns within the same interconnect.

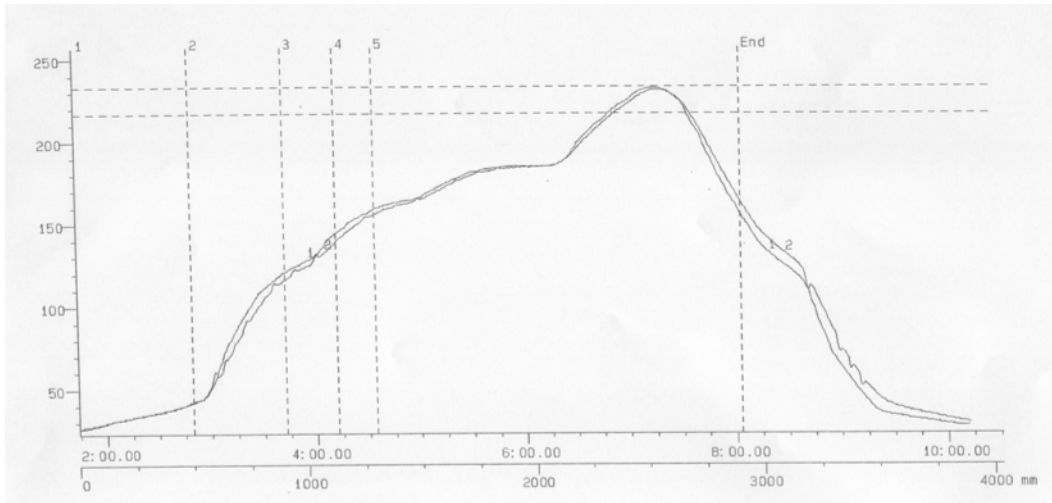


Fig. 3-9 Temperature profile of eutectic 63Sn-37Pb solder reflow

3.2.1.3 Phase II: High-aspect-ratio MCC Interconnect Prototyping

In the *Phase I* fabrication, the aspect ratio of copper columns is only ~1. Both analytic and numerical analysis in Chapter 2 suggested that, with the increase of copper column height and the decrease of copper column radius, the interconnect compliance increases at an exponential rate. Consequently, copper columns with higher aspect ratio are desired in order to achieve excellent thermomechanical reliability for the solder joints of MCC interconnects.

In *Phase II* fabrication, a high-resolution photoresist AZ9260 [56] is used to form the micro-mould for the following copper electroplating process. Although its maximum thickness for a single spin coating is only 20μm, multilayer coating is

allowed to achieve a thickness as high as over 100μm [57]. Furthermore, because of its positive-tone characteristic, removal of this photoresist after plating is not an issue like the cases of some negative thick photoresists such as SU-8 [58]. For our purpose of high-aspect-ratio plating mould, a two-layer coating process is developed to achieve a final thickness of ~32 μm. After the first layer is spin-coated, a soft bake is performed on hot plate at 80°C for 90 seconds. After the coating of the second layer, an oven soft bake is conducted at 90°C for 1 hour to remove the solvent. The wafer is then kept in a cleanroom environment for 12 hours for re-hydration [57]. After a single proximity UV exposure with energy intensity of 1200mJ/cm^2, the micro-mould was realized by immersion of the wafer into AZ300MIF developing solution for 25 minutes. Fig. 3-10 shows the cross section view of the micro-mould, in which the vias have a diameter of 3μm and 10μm at the bottom and top, respectively.

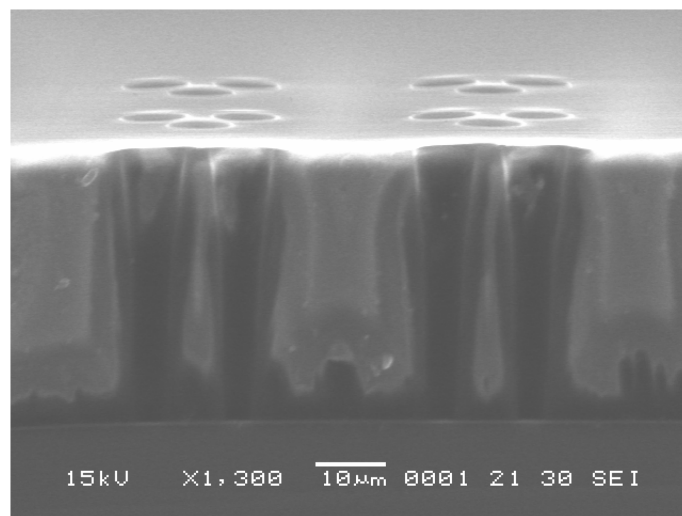


Fig. 3-10 Cross-section view of deep vias in AZ9260

Both Cu and solder are electroplated with the conditions as shown in Table 3-2. A negative photoresist JSR's THB110N is tentatively used to define the window for solder electroplating. Fig. 3-11 shows the plan view of TCC interconnects after a

10μm THB110N layer is patterned with an exposure energy of 400mJ/cm^2. It can be observed that window is well defined to expose the copper columns. Photoresist stripping and seed layer etching are completed using the same methods in *Phase I*. Figs. 3-12 & 3-13 show MCC prototypes fabricated with different pitch and design.

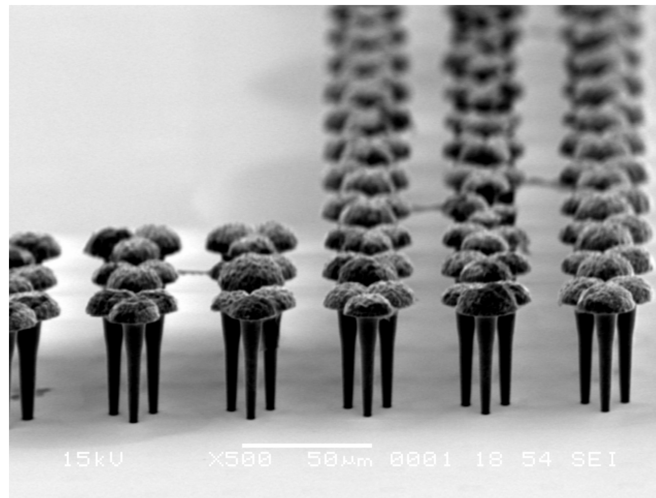
Table 3-2 Electroplating conditions for Cu and eutectic 63Sn-37solder

	Plating bath	Current density, A/dm^2	Temp., °C
Cu	Spherolyte Cu200	~1	24
Solder		~3	23

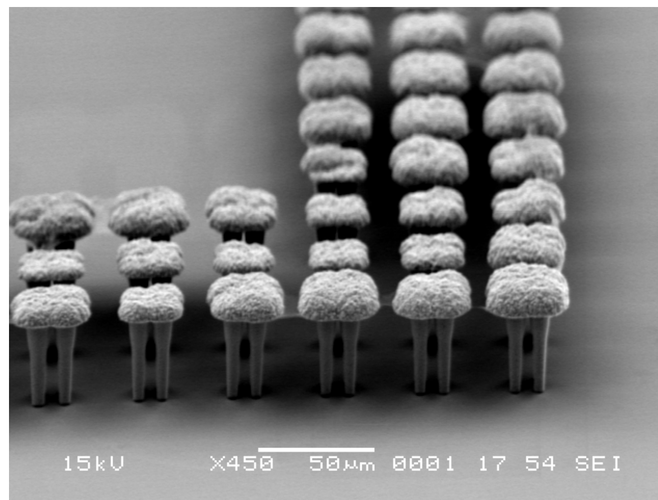
Fig. 3-11 Top view of solder plating window defined with THB110N

It is noted that copper-column-based interconnects have been employed in some commercial applications such as Fujitsu's *Super*CSP. In such applications, however, the copper posts possess low compliances due to their low aspect ratio (~1), and therefore an underfill layer with a coefficient of thermal expansion close to that of the substrate is needed to relieve the strain occurred in the solder joints. By replacing the single post with multiple slimmer columns with higher aspect ratio, it is anticipated

that the MCC interconnects may demonstrate higher compliance and hence thermomechanical reliability while the strain buffer layer may be finally eliminated. Moreover, the ultra-fine pitch of MCC interconnects is able to match the needs of higher I/O density for future packages.



(a)



(b)

Fig. 3-12 Prototypes of 3-row peripheral MCC interconnects with pitch of 40µm (a) TCC; (b) QCC

3.2.2 Planar Microspring Interconnects

3.2.2.1 Process Flow

Fig. 3-14 shows the wafer-level process flow of Planar Microspring interconnects. Starting from the chip pad (Cu) and passivation layer (SiO_2), a sacrificial layer is first deposited on the wafer. As discussed in section 3.1.2, organic polymeric materials with low permittivity are preferred as this sacrificial layer. In this work, Dow's Benzocyclotubene (BCB) with a thickness of ~7.4μm was employed as the sacrificial layer during prototyping.

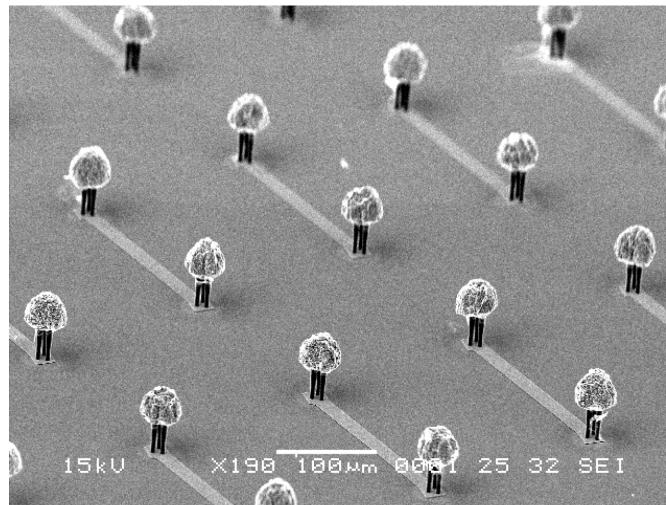


Fig. 3-13 Prototypes of fully populated TCC interconnects with pitch of 200μm

After the BCB is spin-coated and hard cured at 250°C for 1 hour, via patterns are fabricated to expose the chip pads as shown in Fig. 3-14(b). In our efforts to develop the ultra-fine pitch interconnects, the targetted via size is so small ($15\times15\mu m^2$) that photolithography technique can not be utilized to directly form the via in BCB. As a result, a fluorine-based dry etch process was developed to realize the pattern.

Subsequently, a seed layer is sputtered, followed by photoresist coating, patterning, and bottom-up Cu electroplating. As shown in Fig. 3-14(c), this electroplating process is expected to fill in the BCB via and also to form the planar microsprings as well as the metal frame around the microspring beams. Then, the

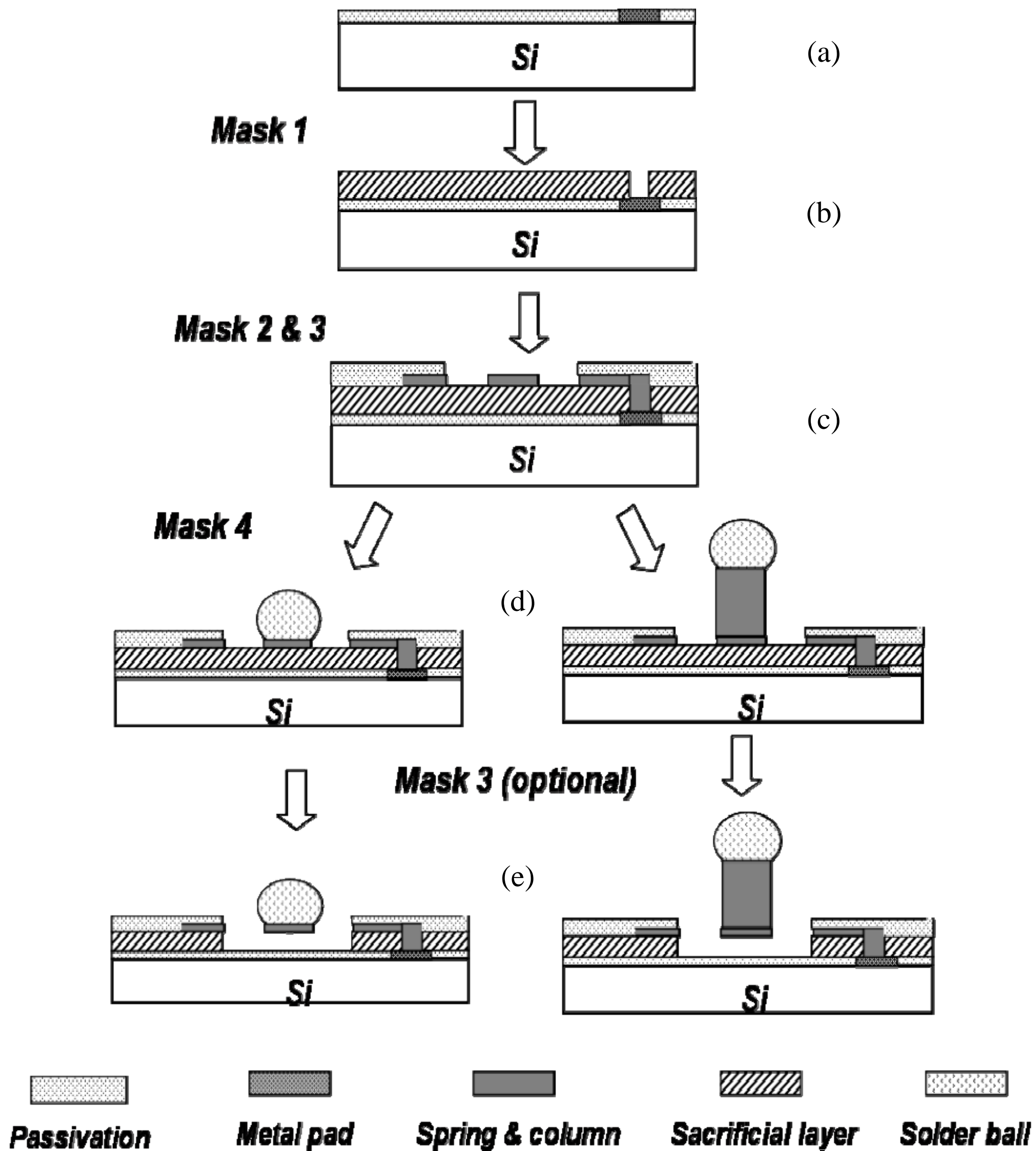


Fig. 3-14 Process flow of *Planar Microspring* interconnects (seed layer not shown)

photoresist is stripped and the exposed seed layer is removed. As shown in Fig. 3-14(c), a passivation layer (e.g., SiO_2) is then deposited and patterned to form the etching window for subsequent microspring releasing process. This layer also functions as a mechanical anchor to the metal frame around the springs. Another seed layer is sputtered, and a thick photoresist (~15μm) layer is patterned to expose the central pad of the Planar Microspring structure. At this point, either solder or additional Cu column plus solder can be grown as revealed in Fig. 3-14(d). The

presence of additional Cu column increases the interconnect standoff, thus further improving the compliances and also facilitating the chip-to-package assembly process. Finally, the photoresist is stripped and the exposed seed layer is removed. The exposed BCB is isotropically etched to release the microspring structure. It should be noted that, an anisotropic and isotropic BCB etching process are required in the process step of Fig. 3-14(b) and (e), respectively. Both processes are developed as described in the following section.

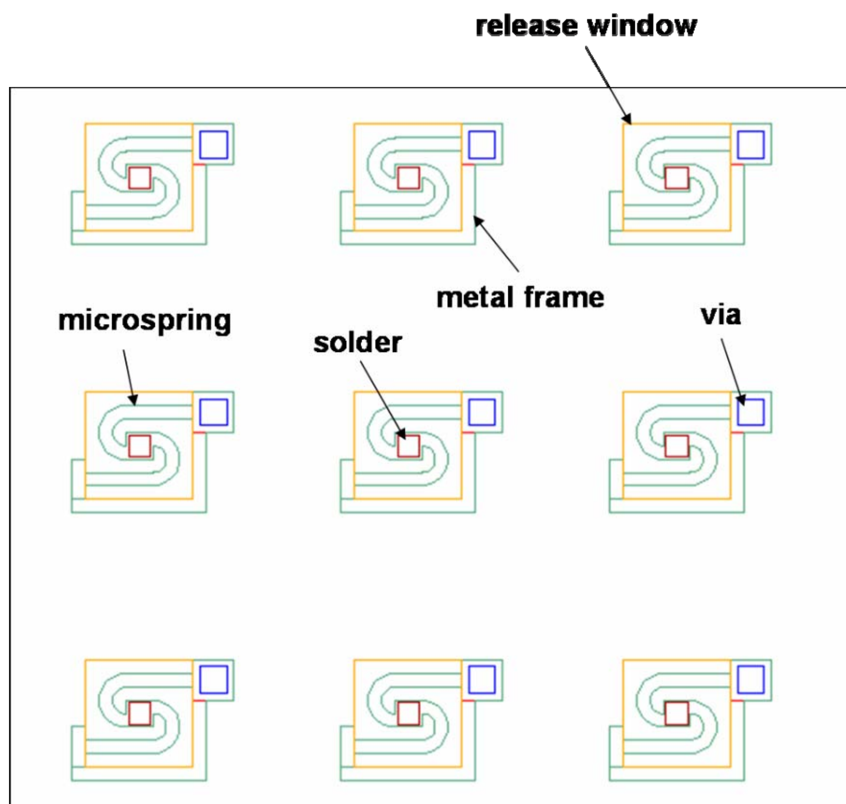


Fig. 3-15 Layout of test masks for Planar Microspring interconnects

3.2.2.2 BCB Patterning by Plasma Etch

For plasma etching of BCB, polymers such as AZ4620 [59,60], AZ9245 [61], Shipley 1813 [62] and Shipley SPR220 [63] have been reported in literatures as soft masking materials. On the other hand, inorganic materials including SiO_2 [64], SiN_x

[65], and metal films such as Cu, Al, Ni [66] and NiCr [49] have been used as hard etch masks. Usually, hard masking materials have higher etching selectivity and better control on the etching profile than soft masks. However, the application of soft masking materials simplifies the process as the consequence of its capability of direct patterning by photolithography. Moreover, thick polymers can be easily applied to compensate its low etching selectivity.

In this section, experimental results are reported on the plasma etching behavior of BCB with thick photoresist AZ9260 or sputtered Ti film as etch masks. The photoresist AZ9260 is chosen as the soft mask material because it enables thick coating and high-aspect-ratio patterning due to its high-transparency attribute. On the other hand, Ti is selected as hard mask material since it is commonly used as the adhesion layer in a typical CMOS process. Compared to other metallic etch mask materials such as Cu or Al, Ti provides more freedom for process integration.

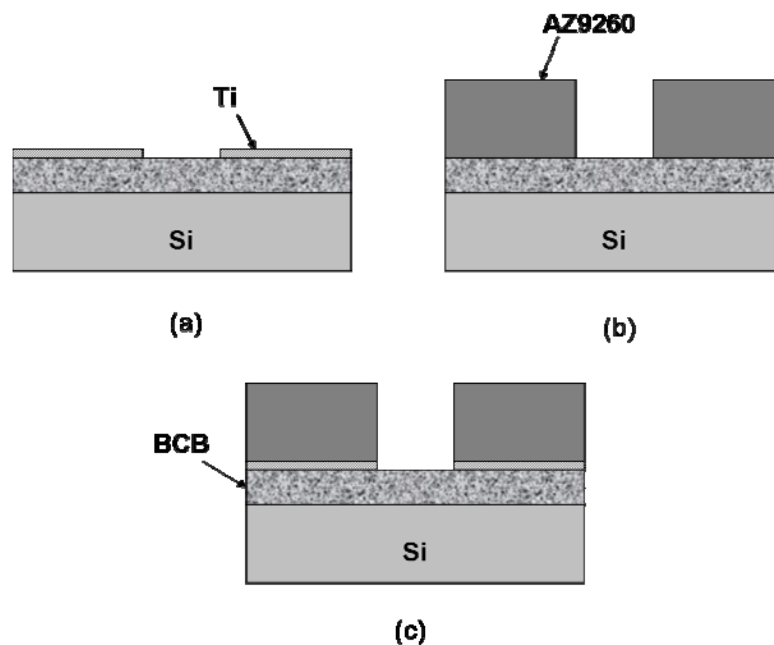


Fig. 3-16 Samples for BCB etching experiments (a) Ti/BCB selectivity; (b) AZ9260/BCB selectivity; (c) BCB etching profile control

Three kinds of samples of 25×25 mm^2 as shown in Fig. 3-16 were prepared for BCB etching experiments. A 10μm BCB film was spin-coated and cured in N_2 atmosphere at 250°C for 1 hour to achieve more than 95% of polymerization [67]. As shown in Fig. 3-16(a), a 0.5μm Ti film was sputtered on some samples and patterned in a wet etchant (Ethyleneglycol:HF=3:1) for 1min at room temperature. These samples were used for measurement of BCB etching selectivity over Ti. Similarly, a 15μm thick AZ9260 photoresist was coated and patterned on some samples, as shown in Fig. 3-16(b), for measurement of BCB etching selectivity over AZ9260. By combining Ti and AZ9260, some samples were also prepared as shown in Fig. 3-16(c) for study of BCB etching profile control.

Etching experiments were conducted in Plasma-Therm 790 series Dry Etcher using CF_4/O_2 plasma. DEKTAK 8000 Surface Profiler was used to measure the film thickness before and after etching, and hence the etching rate and selectivity were calculated. Scanning Electron Microscopy (SEM) was used to determine the etching profile. The correlation between the etch rates, selectivity and the fluorine concentration was first studied with a fixed RF power and chamber pressure. A three-level design of experiments technique was then used to explore the effects of the RF power (100W → 200W → 300W) and chamber pressure (50mTorr → 150mTorr → 250mTorr) on various BCB etching characteristics. For all the experiments, the total flow rate of gases was fixed at 20sccm.

Fig. 3-17 shows the etching rates of AZ9260, BCB and sputtered Ti film in different etching gases with a constant power of 300W and a total pressure of 50mTorr. The etching rates were obtained by linearly fitting the etching depths at different time. A maximum BCB etching rates of 0.7μm/min was achieved at 30% CF_4 percentage condition. The BCB etching rate rapidly decreases as the fluorine

concentration deviates from the optimum concentration. This was due to the fact that BCB includes both hydrocarbon and Si in its molecular chain. In pure O_2 plasma, oxygen reacts with hydrogen in BCB to produce radical type active center on the BCB surface, which can be attacked again by atomic oxygen till the final formation of SiO_2 film. Since the bond energy of F-H is higher than that of O-H by 35kcal/mol [66], even a small addition of CF_4 can result in significant increase of the BCB etch rate as shown in Fig. 3-17. With the continuous increase of fluorinated gas concentration, however, fluorocarbon polymer may be produced on the BCB surface by direct deposition from the CF_4 plasma. The fluorocarbon layer functions as a diffusion barrier for the reactive species, therefore the BCB etch rate starts to decrease as the fluorinated gas concentration increases beyond a critical value. Similar trend of BCB etch rate has been reported previously [64,65].

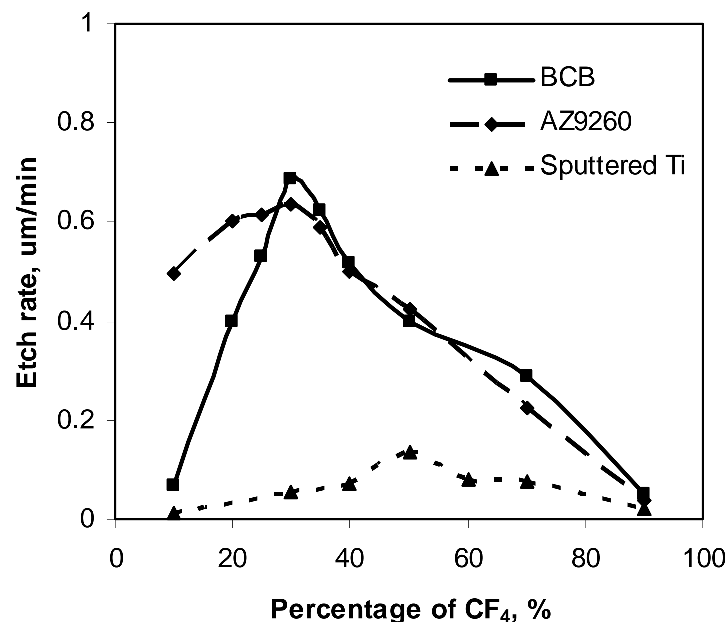


Fig. 3-17 Etch rates of BCB, AZ9260 and sputtered Ti

Fig. 3-17 also shows the etching rate of AZ9260 and sputtered Ti varying with fluorine concentration. Interestingly, the photoresist etch rate also demonstrates a

maximum at 30% CF_4. At this composition, an etching selectivity ~1.1 of BCB over the photoresist was achieved. In comparison, the sputtered Ti film shows much slower etch rate and hence higher selectivity over BCB. In CF_4/O_2 plasma, the maximum Ti etch rate was ~0.14μm with 50% CF_4 concentration. The maximum selectivity of BCB over sputtered Ti was achieved as ~13 with a 30% CF_4 concentration. It was noted that for CF_4/O_2 plasma, the maximum selectivity over Ti roughly coincides with the maximum BCB etching rate.

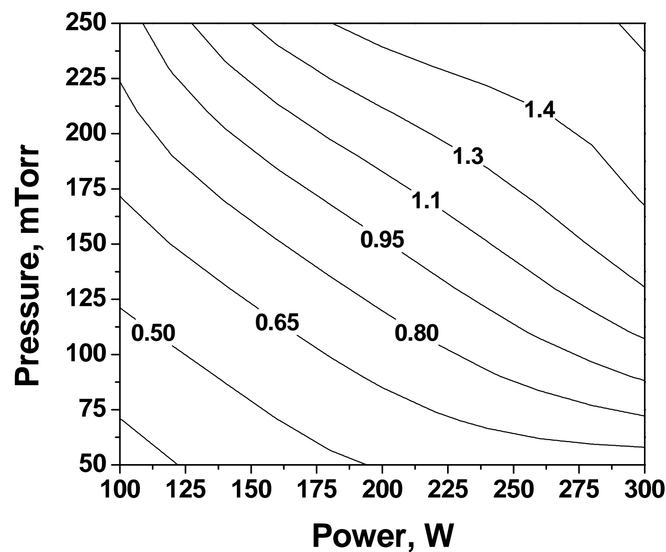


Fig. 3-18 Contour plot of BCB etch rate as a function of power and pressure for 30%CF_4/70%O_2 plasma

Fig. 3-18 illustrates the BCB etch rates varying with the power and pressure in 30%CF_4/70%O_2 plasma. Fig. 3-19 shows the dc bias developed at the electrode as a function of chamber pressure and RF power. It was understood that reactive ion etching occurs as a consequence of combined ion-etching and spontaneous chemical reaction. A comparison between Fig. 3-18 and Fig. 3-19 shows that the power effect on etch rate was demonstrated by increased dc bias and hence an enhanced ion-etching effect. This observation is applicable at any pressure level.

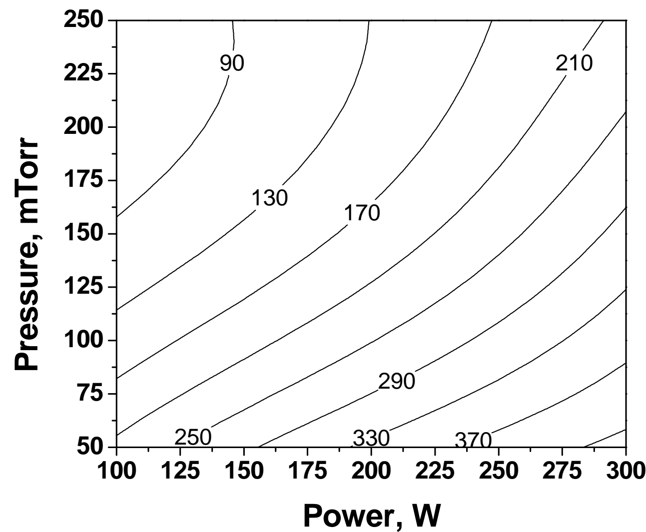


Fig. 3-19 Contour plot of DC bias as a function of power and pressure in $30\%CF_4/70\%O_2$ plasma

For $30\%CF_4/70\%O_2$ plasma, an increase in pressure resulted in decrease of dc bias as shown in Fig. 3-19 but increase of BCB etch rate as shown in Fig. 3-18. It was well-known that the pressure effect on etch rate is manifested in two opposing aspects: 1) the mean free path of electrons and charged particles in the plasma increases with the decrease of pressure, and thus higher dc bias voltage develops at the electrode, resulting in stronger ion-etching effects on the target and hence higher etch rate; 2) lower pressure means lower density of etching agent and therefore lower etch rate, which obviously depends on the mass transportation in the local region for the etching reaction. Therefore, it can be inferred from the above observation that for the $30\%CF_4/70\%O_2$ plasma system, the F-radicals was more and more depleted by the decrease of pressure, and as a result the BCB etch rate decreased even though the ion-etching effect became stronger.

For $30\%CF_4/70\%O_2$ plasma, the etch rate of AZ9260 slightly varies with power and pressure. The selectivity almost always decreases with higher power as shown in Fig. 3-20, implying that the AZ9260 etching rate increases more rapidly with the power than BCB, which is consistent with previous report for SF_6/O_2 plasma [60].

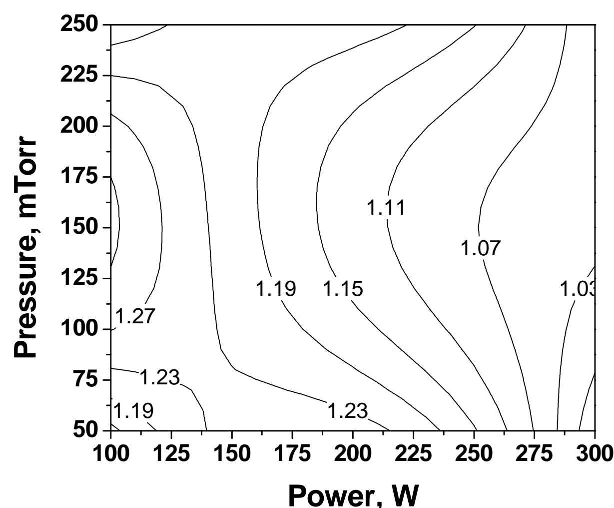


Fig. 3-20 Contour plot of BCB/AZ9260 selectivity as a function of power and pressure in 30%CF_4/70%O_2 plasma

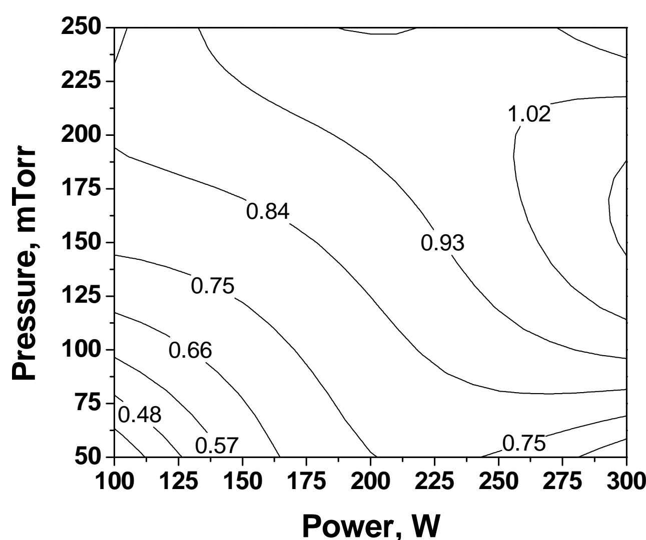


Fig. 3-21 Contour plot of lateral/vertical etch ratio varying with power and pressure (CF_4: 6sccm; O_2: 14sccm)

Based on the above experimental results, a double layer combining 500nm sputtered Ti and ~10μm photoresist AZ9260 is patterned as BCB etching mask as shown in Fig. 3-16(c). During BCB etching, the Ti mask is less eroded than photoresist because of its higher selectivity, while its thickness deficiency may be compensated by the thick photoresist. Power and pressure conditions of CF_4/O_2 plasma are optimized to achieve anisotropic BCB etching as required in Fig. 3-14(b)

and isotropic BCB etching as required in Fig. 3-14(e). In this work, a lateral etching distance was defined as half of the difference between the top width of the etched via and the bottom width of the opening in the etch mask. Vertical etching depth represents the magnitude of directional BCB etching. Hence, a lower lateral/vertical etching ratio is preferred for BCB via etching, and a high lateral/vertical etching ratio is desired for microspring releasing. Fig. 3-21 shows that in the 30%CF_4/70%O_2 plasma, the lateral/vertical etching ratio can be reduced to less than 0.4 with lower power and pressure, but increases to ~1 with higher power and pressure.

3.2.2.3 Prototyping of Planar Microspring Interconnects

Starting with patterned dielectric layer (SiO_2) and metal (Cu) pad, Dow's BCB4024-40 was spin-coated and hard cured at 250°C for 1 hour to achieve a final thickness of ~7.4μm. A 0.5μm sputtered Ti and ~10μm AZ9260 photoresist was sequentially deposited and patterned with *Mask 1* (blue layer in Fig. 3-15) for the following BCB dry etching to expose the on-chip metal pad. Based on the BCB etching experiments as described in the previous section, 30%CF_4/70%O_2 plasma with conditions of 100W and 50mTorr was selected to form the BCB via. After stripping the photoresist, a seed layer of 200**Å** Ti and 500**Å** Au was sequentially deposited by sputtering. A 5μm AZ9260 photoresist was again spin-coated and patterned with *Mask 2* (cyan layer in Fig. 3-15), followed by Cu electroplating to form the Planar Microspring which was connected to the on-chip metal pads. Fig. 3-22 shows daisy chain of *J*_shape Planar Microspring array with a pitch of ~100μm after removing the Ti/Au seed layer using the same process as described in section 3.2.1.2. The daisy chain was designed for the purpose of electrical characterization that will be presented in Chapter 4.

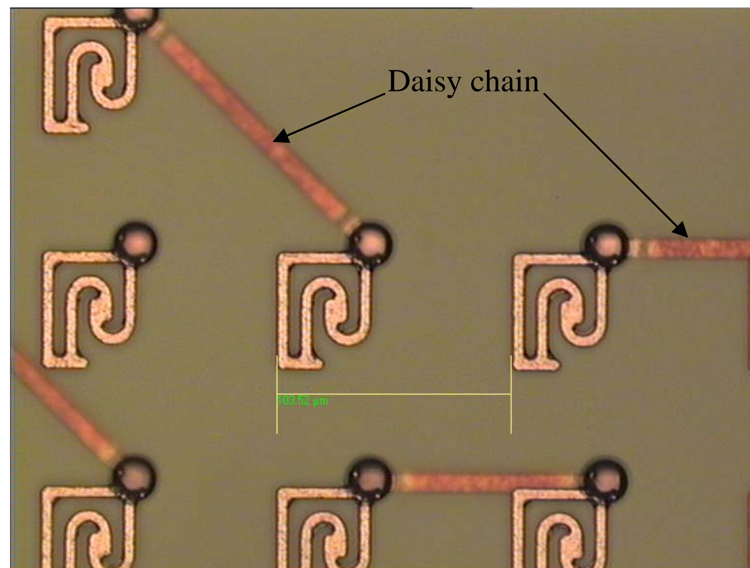
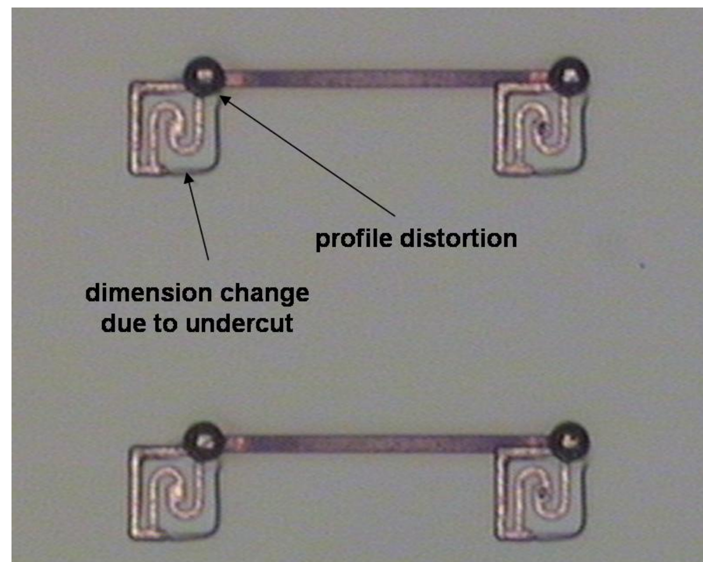


Fig. 3-22 Daisy chain of *J*_shape Planar Microspring prototype

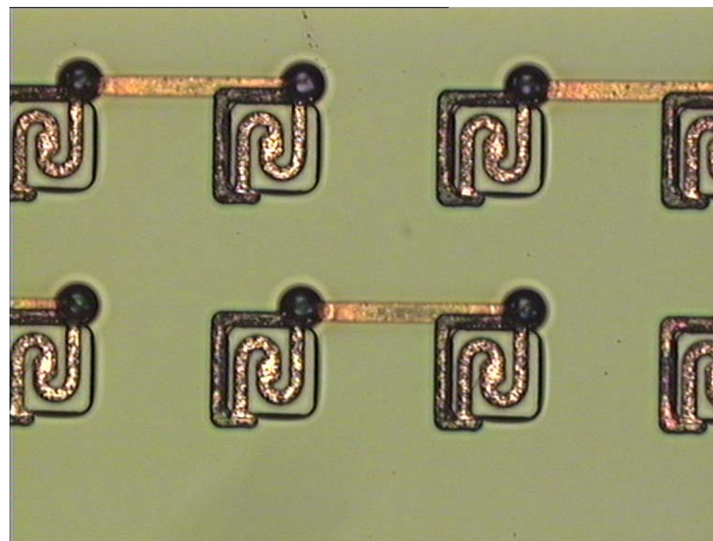
A 0.5μm PECVD-SiO_2 was then deposited, followed by ~10μm SPR220 photoresist coating and patterning with *Mask 3* (yellow layer in Fig. 3-15). The exposed SiO_2 on top of the Planar Microsprings was etched while the metal frame around the microsprings was still covered by the remaining SiO_2. At this point, plasma etch of SiO_2 is preferred over wet etching by buffered oxide etchant (BOE) since the latter induce significant SiO_2 undercut as shown in Fig. 3-23(a). In contrast, a plasma etch using 90%CHF_3 10%O_2 at conditions of 300W, 80mTorr and total flow rate of 50sccm led to much better control of the etching profile as shown in Fig. 3-23(b).

A seed layer of 200Å Ti and 500Å Au was again sequentially deposited by sputtering, followed by ~15μm AZ9260 photoresist coating and patterning with *Mask 4* (brown layer in Fig. 3-15). At this point, only the central pad of the Planar Microspring structure was exposed. Either eutectic 63Sn-37Pb solder or Cu column plus solder was electroplated with the same conditions as shown in Table 3-2. After electroplating, the photoresist and Ti/Au seed layer was removed using the same

process as described in section 3.2.1.2. Finally, a ~15μm AZ9260 photoresist was again spin-coated but patterned with *Mask 3* to define the BCB etch window for microspring releasing. This step can be skipped if the previously defined SiO_2 window is thick enough to survive the following BCB isotropic etching. Based on the BCB etching experiments as described in the previous



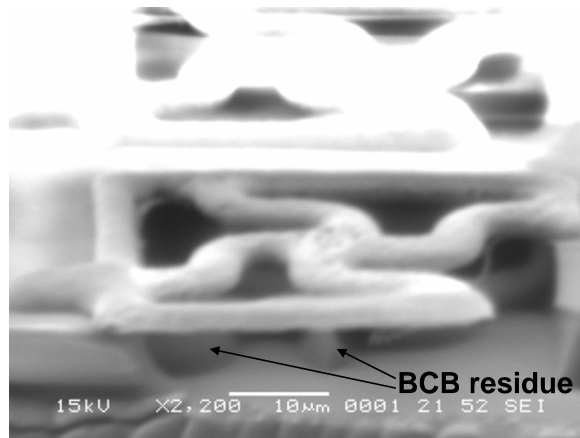
(a)



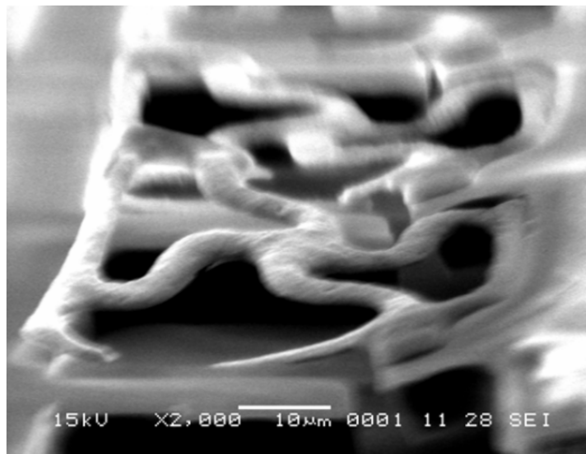
(b)

Fig. 3-23 Comparison of SiO_2 etching profile by (a) wet etchant BOE; (b) CHF_3+O_2 plasma etch

section, 30%CF_4/70%O_2 plasma with conditions of 300W and 200mTorr was selected for isotropic etching of BCB to release the microspring beams. Fig. 3-24(b) clearly shows improved isotropic etching of BCB under microspring beams as compared to incomplete BCB etching in Fig. 3-24(a).



(a)

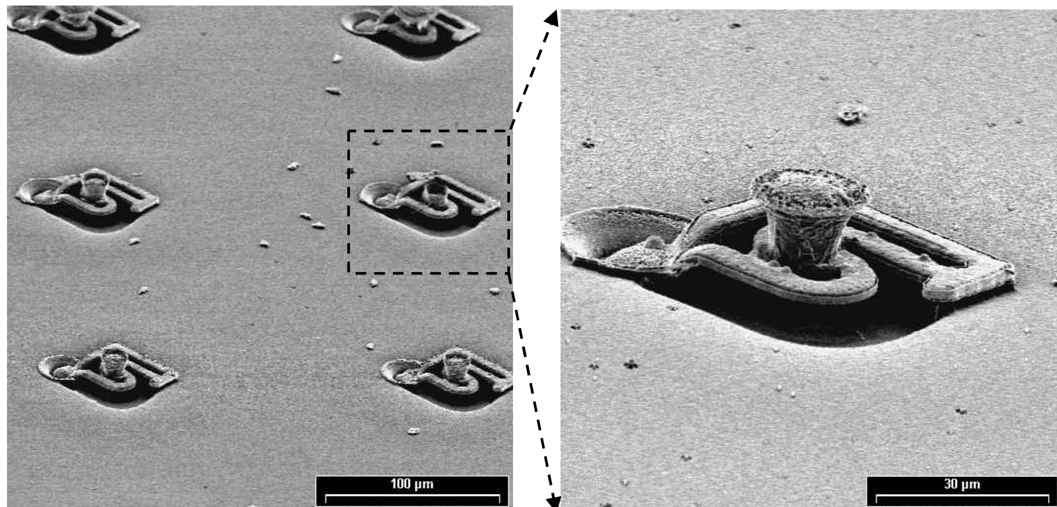


(b)

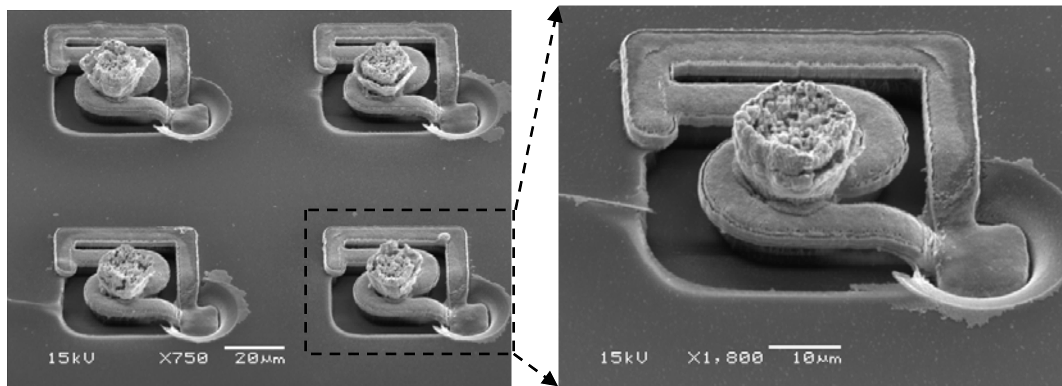
Fig. 3-24 Isotropic etching of BCB by 30%CF_4/70%O_2 to release microspring beams (a) 300W and 50Torr; (b) 300W and 200mTorr (etching time: 8.5mins)

Fig. 3-25(a)~(d) shows prototypes of *J*_shape interconnect array with pitches of 200μm or 100μm. The nominal width and thickness of microspring are 5μm and 2μm,

respectively. Fig. 3-25(a) & (b) shows interconnect prototypes with ~8μm high Cu column between microsprings and solder. Solder bumps can also be directly electroplated onto microsprings, as shown in Fig. 3-25(c) & (d).



(a) (b)



(c) (d)

Fig. 3-25 SEM image of *J*-shape *Planar Microspring* interconnects (a) interconnects with additional Cu column, 200μm pitch; (b) close-up view of single interconnect with additional Cu column; (c) interconnects without additional Cu column, 100μm pitch; (d) close-up view of single interconnect without additional Cu column

Chapter 4 Characterization of Compliant Interconnects

In this Chapter, both mechanical and electrical testing results are reported for compliant interconnects. First, a nano-indentator is utilized to quantitatively evaluate the stiffness of both MCC and Planar Microspring interconnects. In the following, dummy chips with MCC interconnects are flip-chip bonded to Si test boards for extraction of electrical parasitics (R, L & C). Finally, dummy chips are assembled to customized testing set-up and effective signal transmission through MCC interconnects is verified up to 5GHz.

4.1 Mechanical Testing of Compliant Interconnect Using a Nano-Indentator

4.1.1 Testing Method

For extremely miniaturized and particularly composite structures like MCC interconnects, the structure integrity under external loading is always a big concern. For conventional solder interconnects, the Sn content in Pb-Sn solder material reacts with Cu or Au in the Under-Ball-Metallization (UBM) layer to form intermetallics. The intermetallics have high elastic modulus, resulting in a strong and reliable interface between solder and pads on chip or packaging substrates. For compliant interconnects in this thesis, the solder is expected to form strong joints with pads on the packaging substrate, just like the pure solder interconnects. However, the addition of copper-based flexible structures introduces two new interfaces between different material layers. For MCC interconnects, new interfaces are formed between the on-chip Cu pad and the electroplated Cu columns, and between the electroplated Cu

columns and solder as well. For Planar Microspring interconnects, new interfaces are formed between the solder and electroplated Cu beams, and also between the Cu beams and the underneath sacrificial layer (e.g., BCB). Good adhesion is required for these interfaces to survive external loading or deformation due to thermal mismatch. In this section, the structural stiffnesses of both compliant interconnects are quantitatively evaluated using a nano-indentator.

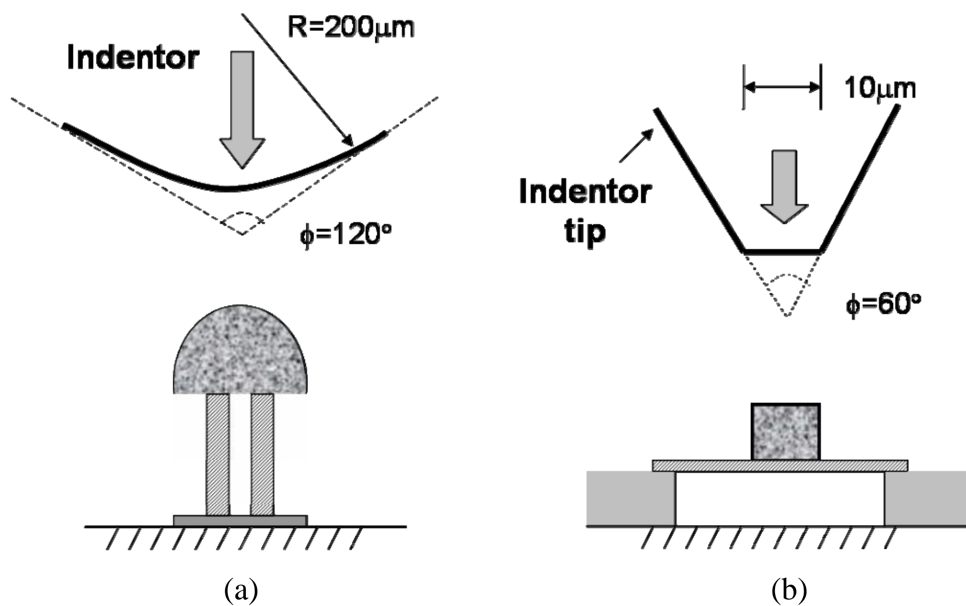


Fig. 4-1 Schematic of nano-indentation testing on (a) MCC; (b) Planar Microspring Interconnects

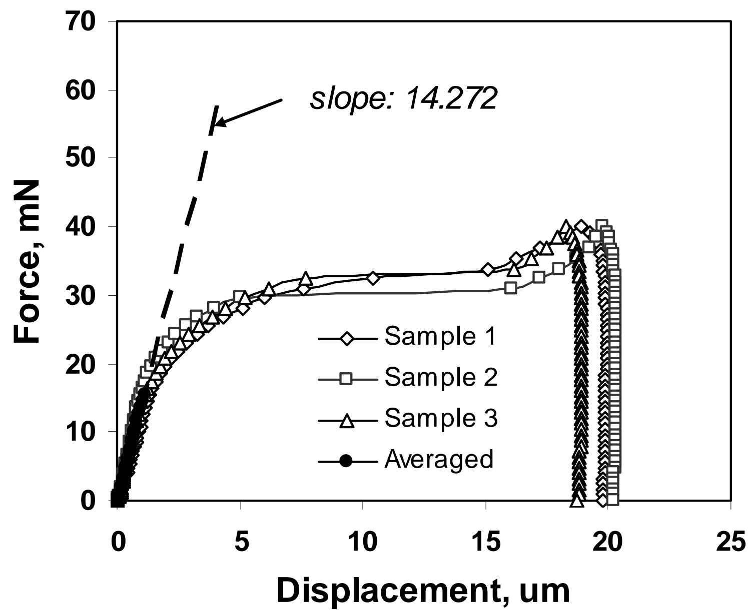
As shown in Fig. 4-1, different nano-indentors were used to apply vertical force loading on MCC and Planar Microspring interconnects, respectively, and the resultant vertical displacement of the indentor was recorded as response. Triple-Copper-Column (TCC) interconnect prototypes with column heights of either 15μm or 30μm were tested. Taking into account the solder thickness, the total height of TCC interconnects is ~35μm or ~50μm. An indentor with round tip as shown in Fig. 4-1(a) is used for testing of MCC interconnects. The advantage of this indentor in this application is that a maximum contact area between the indentor and the solder joint

can be achieved. This guarantees that vertical loading is applied to the whole interconnect instead of a local solder region.

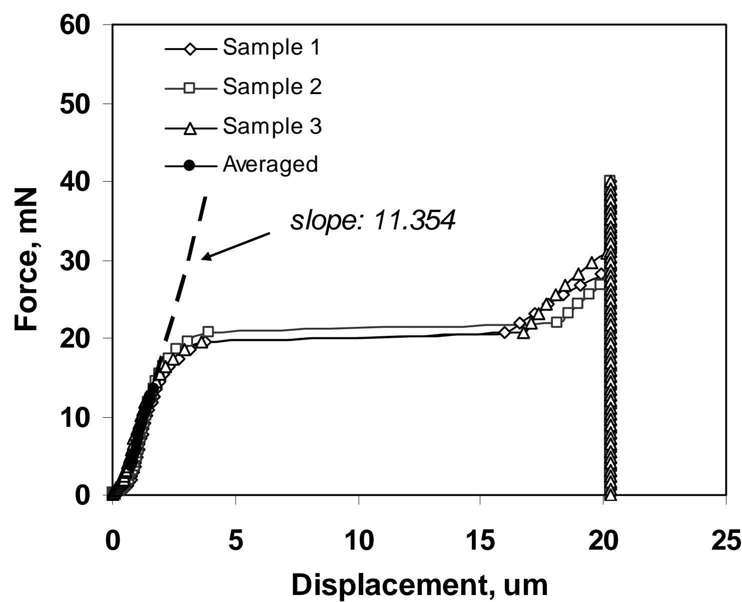
Planar Microspring interconnects without additional Cu columns have a low standoff height of ~10μm, and the solder bump size is only ~10×10μm^2. For this interconnect, a punch-type indentor with flat tip was used for testing as shown in Fig. 4-1(b). The tip size is 10×10μm^2 and exactly matches the size of solder bump. Therefore, the vertical loading can be effectively transferred to the beams of the microspring.

4.1.2 Results and Discussion

Fig. 4-2 shows the force-displacement curve for TCC interconnects with column height of 15μm or 30μm. Three samples were tested for each column height, and good process uniformity was evidenced by the very similar curves obtained for each sample. For those samples with 15μm high Cu columns, a drastic increase of displacement was observed at force of ~30mN. In comparison, a similar trend was observed at ~20mN for samples with 30μm high Cu columns. The abrupt increase of displacement can be attributed to buckling of copper columns. For columns of fixed cross section area, the structure stability under axial loading decreases with increase of height, and hence the critical force for buckling to take place is lower.



(a)



(b)

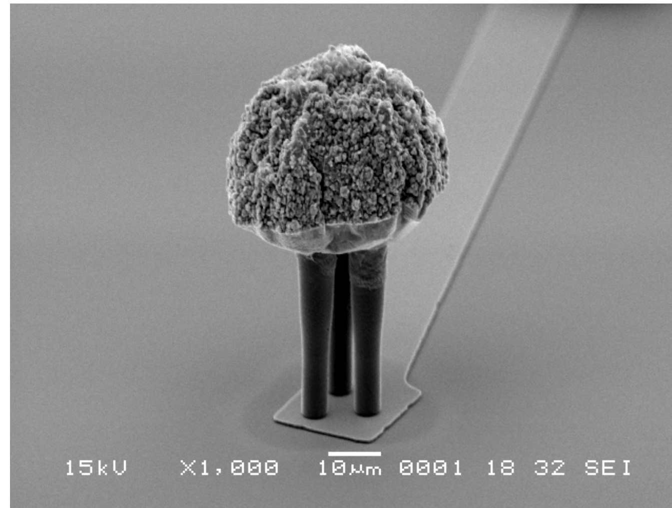
Fig. 4-2 Force-displacement Curve for TCC interconnects with Cu column of (a) 15μm; (b) 30μm

At the initial stage of loading, Fig. 4-2 shows that the displacement increases monotonically with the force. A linear fitting of the averaged data gives a slope of 14.272mN/μm and 11.354mN/μm, respectively, for TCC interconnects with column height of 15μm and 30μm. The slopes translate to nominal vertical compliances of

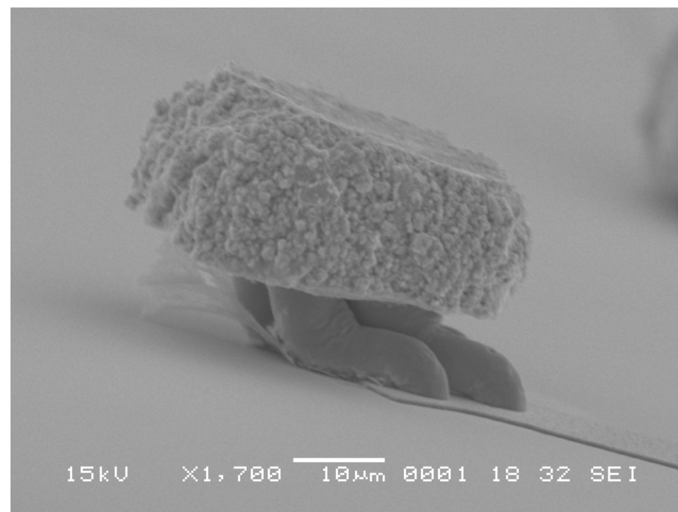
0.07mm/N and 0.088mm/N, respectively. Recall that in Chapter 2, a vertical compliance of 0.003mm/N for TCC interconnect with column height of 5μm was obtained from numerical simulation using ANSYS. In addition to the difference in column height, the major causes leading to the discrepancy between simulation and experiment may be attributed to the following: 1) In the numerical simulation, both solder and Cu columns are arranged in a symmetric manner with respect to the axis of the interconnects. The force is uniformly applied to the solder top surface, therefore the resultant force is perfectly axial. In this way, the interconnect is more resistant to buckling and hence demonstrates lower compliance. In the experiment, however, the force was easily applied off-axis because of the small size of the interconnect. As a result, column buckling takes place at lower loading and higher compliance is obtained. 2) In the numerical simulation, a flat top surface was assumed for solder which is real for interconnects assembled to the package board. However, the sample used in the experiment had a solder of dome shape. During loading, the spherical tip of the indentator as shown in Fig. 4-1(a) easily developed a sliding movement along the solder surface resulting in a higher compliance being measured.

Fig. 4-3 shows SEM photos of a typical TCC interconnect prototype before and after vertical loading. It could be seen that structural integrity is preserved, despite a high loading as evidenced by the flattened top surface of the solder and the bent copper columns. No crack could be observed at the interface between the electroplated copper column and the sputtered Cu pad, indicating a strong bond resulting from the Cu electroplating process. The interface between the copper column and solder is invisible in Fig. 4-3(b). However, the interface was assumed as not degraded since the solder bump remained parallel to the chip surface after loading.

It also can be inferred from Fig. 4-3(b) that the buckling occurred initially at the center and then the bottom of the Cu columns.



(a)



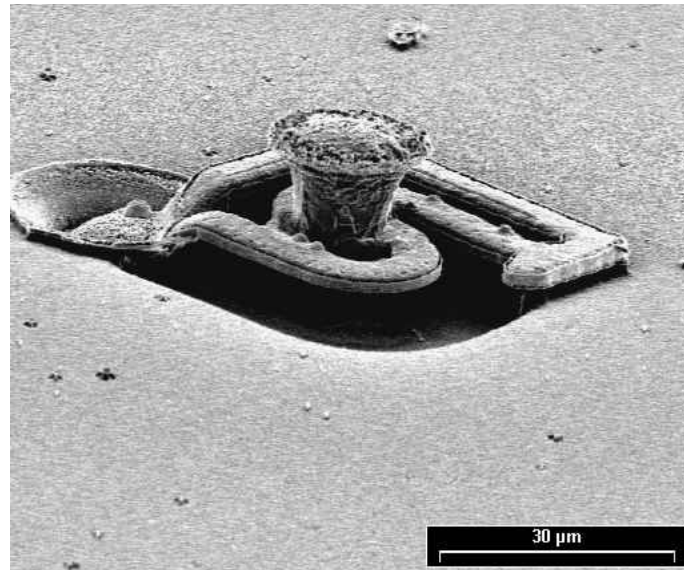
(b)

Fig. 4-3 Nano-indentation testing on MCC interconnects (a) TCC prototype; (b) deformed TCC

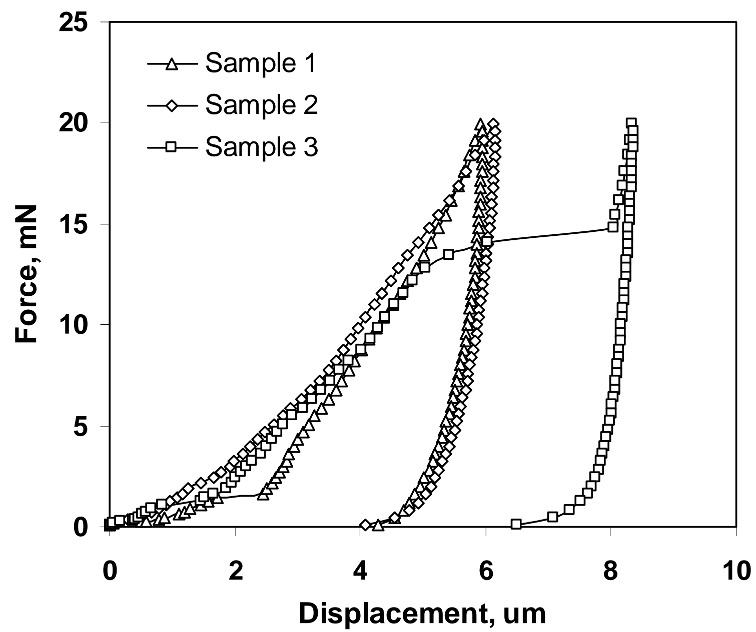
Fig. 4-4 and Fig. 4-5 show SEM photos of Planar Microspring interconnect prototypes for Nano-indentation test and the resulting Force-Displacement curves. Both *J*_shape and *S_1* with four beams designs were evaluated. The microspring beams were 2μm thick and 5μm wide. An additional Cu column of ~8μm high was

grown on the central pad of microsprings, followed by eutectic 63Sn-37Pb solder of ~2μm thick. Vertical force loading was applied onto the solder by a punch-tip indentator as shown in Fig. 4-1(b).

Benefiting from optimized design and less beam count, the *J*_shape interconnect shows higher flexibility than the *S_1* design. For example, the *J*_shape interconnect demonstrated vertical displacement of ~6μm at a loading force of 20mN, while in comparison the *S_1* was pressed down by only 3.7~4.2μm for the same loading force. The repeatability of structure flexibility is good as evidenced by the similar trend for all the three samples in Fig. 4-4(b) and Fig. 4-5(b). For *J*_shape interconnects, sample 3 showed an abnormal increase of displacement at a loading force of ~13mN, which may be attributed to the breaking of microspring beams. The other two samples maintained structural integrity after a vertical loading of 20mN, at which a maximum displacement of ~5.9μm was recorded. However, owing to plastic deformation of the Cu microsprings and solder, the interconnects were left with a residual displacement of 4μm after force unloading. In comparison, Fig. 4-5(b) shows that the *S_1* interconnects with four microsprings gave a displacement of 3.7~4.3μm at 20mN and a residual displacement of 2.7~3.2μm. It also can be inferred from the force-displacement curve that all the *S_1* interconnect samples maintained structural integrity throughout the testing.

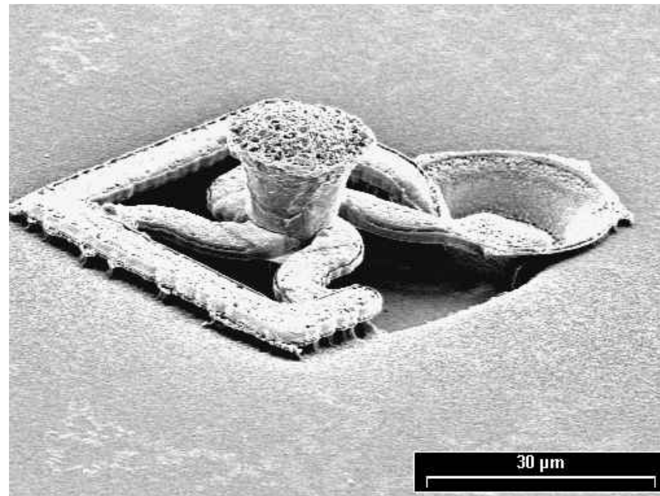


(a)

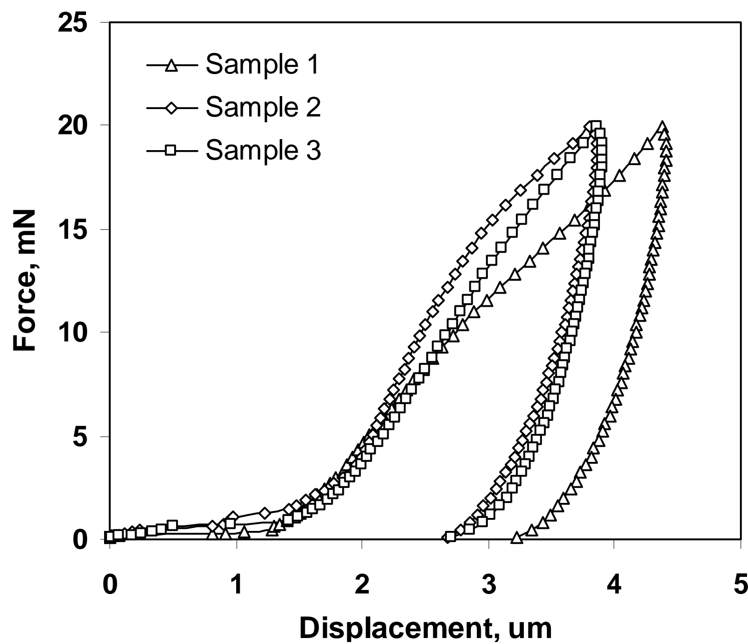


(b)

Fig. 4-4 *J*-shape *Planar Microspring* Interconnect with ~8µm Cu column (a) SEM photo; (b) Force-Displacement curve from Nano-indentation



(a)



(b)

Fig. 4-5 *S_1* Planar Microspring Interconnect (4 beams) with ~8μm Cu column (a) SEM photo; (b) Force-Displacement curve from Nano-indentation

For flip-chip compliant interconnects of small size such as MCC or Planar Microspring, it is of great interest to know whether the self weight of the chip, which is flipped and joined to the packaging substrate through the compliant interconnects, will significantly deform the interconnect. Considering a Si chip with a size of $20\times20\times0.74mm^3$ and density of $2330kg/m^3$, the self weight of chip is calculated as

0.69g. If the chip is populated with 3 by 3 peripheral rows of compliant interconnects with a pitch of 100μm, and total amount of interconnects is more than 2300 and a vertical loading of less than 0.003mN is applied to a single interconnect. Hence, it can be concluded from Fig. 4-2, 4-4 and 4-5 that the self weight of chip will not induce any perceivable deformation on the MCC and *Planar Microspring* interconnects.

4.2 Low-frequency Electrical Measurement of MCC Interconnects

4.2.1 Test Chip & Board: Design, Fabrication and Assembly

Because of the extremely small size, it is impractical to directly probe the MCC interconnects to measure their electrical parasitics. In this thesis, interconnection chains on test chip and board are designed in such a way that, when the chip is flipped over and mounted onto the board, the on-chip and on-board chains are connected through the MCC interconnects to form a long electrical path. Big metal pads are fabricated at both ends of the electrical path for probing. The test board is made of Si and fabricated using standard IC technology. The parasitics (R, L & C) measured from the electrical loop is then divided by the number of interconnects to give parasitics per interconnect, which actually include contributions from both on-chip and on-board interconnections. Although accurate quantitative measurement is not possible with this method, it enables us to verify the functionality of MCC interconnects and also gives a rough estimation of the parasitics.

Fig. 4-6 shows the layout of the test chip, which has a size of $10\times10mm^2$ and consists of fully area array of MCC interconnects with 100μm pitch. Within the Triple-Copper-Column (TCC) interconnects, the copper columns with diameter of 5μm and height of ~30μm are arranged in an equilateral triangular pattern with spacing of 5μm. The test chip was fabricated according to the procedure described in

Section 3.2.1.3, Chapter 3, except that the on-chip interconnections were made of 5μm electroplated copper to reduce the electrical resistance.

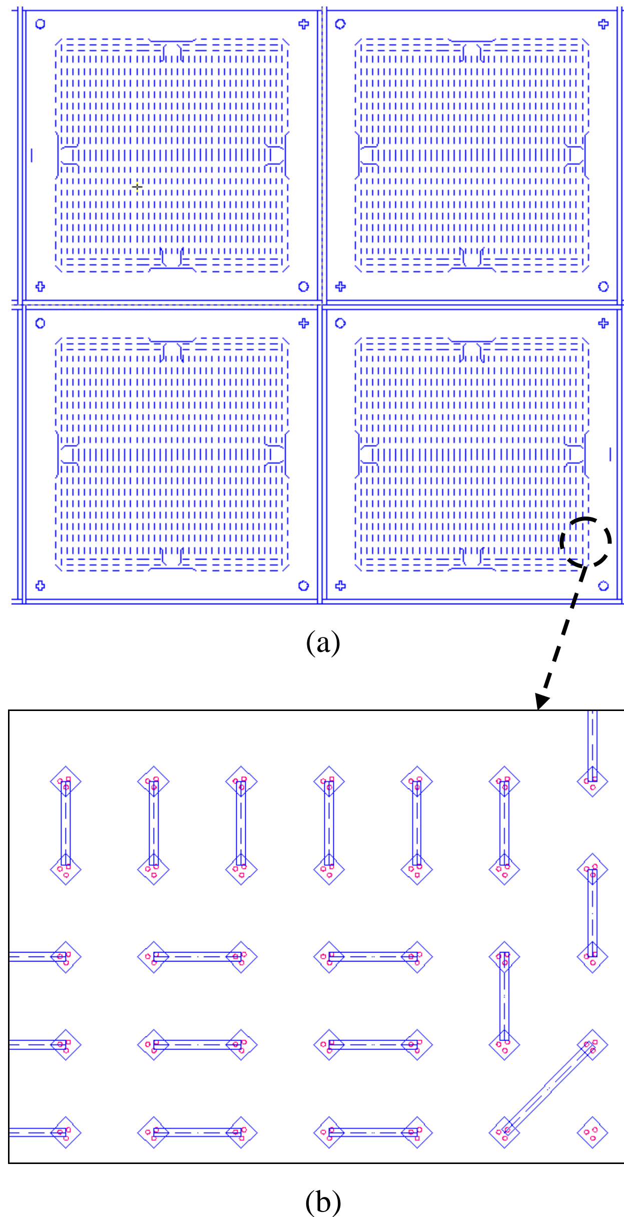
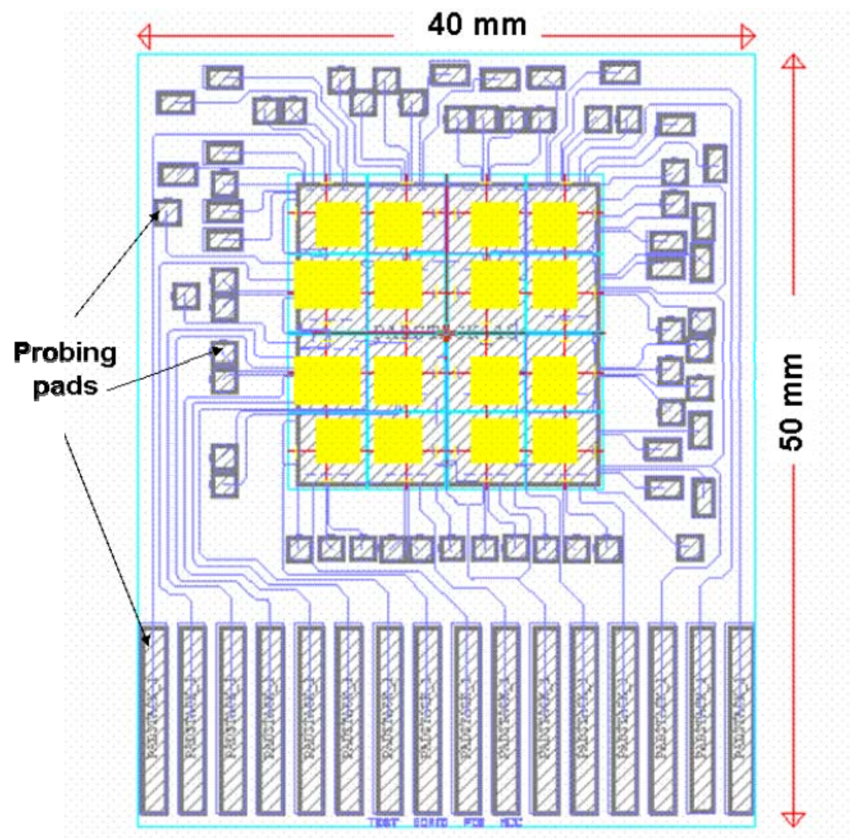


Fig. 4-6 Mask layout of test chip with size of 10×10mm^2 and pitch of 100μm; (a) whole view; (b) close view.

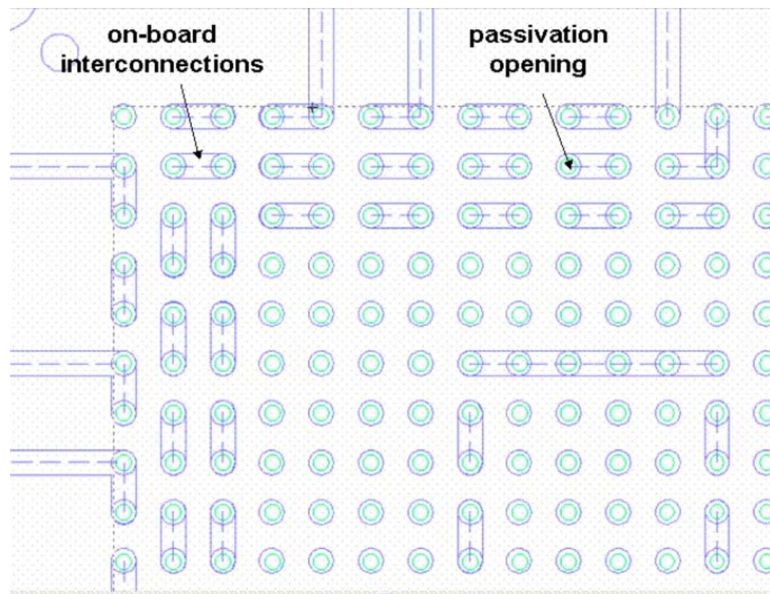
Fig. 4-7(a) shows the layout of Si test board with a size of 40×50mm^2. It should be noted that this test board was initially designed for measurement of 20×20mm^2 test chips, but each quarter of the chip area includes independent daisy chain designs. Hence, the test chip as described above can be assembled to any quarter area for

electrical testing. Fig. 4-7(a) also shows metal pads for probing. Fig. 4-7(b) shows a close view of the layout design. Two masks were involved, one for on-board interconnections and metal pads, and another one for opening of the passivation.

Fig. 4-8 shows process flow for the Si test board. First, a Si wafer was passivated with 500nm-thick SiO_2 by plasma enhanced chemical vapor deposition (PECVD) technique. A seed layer of 25nm Ta and 150nm Cu was then deposited by sputtering, followed by electroplating of 500nm-thick Cu. This thick Cu layer will be used as ground plane for measurement of inductance and capacitance. A double passivation layer was then deposited, including 100nm SiN and 500nm SiO_2. Ammonia treatment was applied before SiN deposition to remove the thin layer of copper oxide on the blanket Cu surface. In the following, a seed layer of 50nm Ti and 500nm Cu was deposited and followed by selective electroplating of 5μm Cu to form the daisy chain of on-board interconnections. After etching back the seed layer, a double passivation layer of 100nm SiN and 200nm SiO_2 was then deposited and patterned by plasma etch to form passivation openings.



(a)



(b)

Fig. 4-7 Layout of 10×10mm^2 Si test board with 100μm pitch; (a) whole view; (b) close view

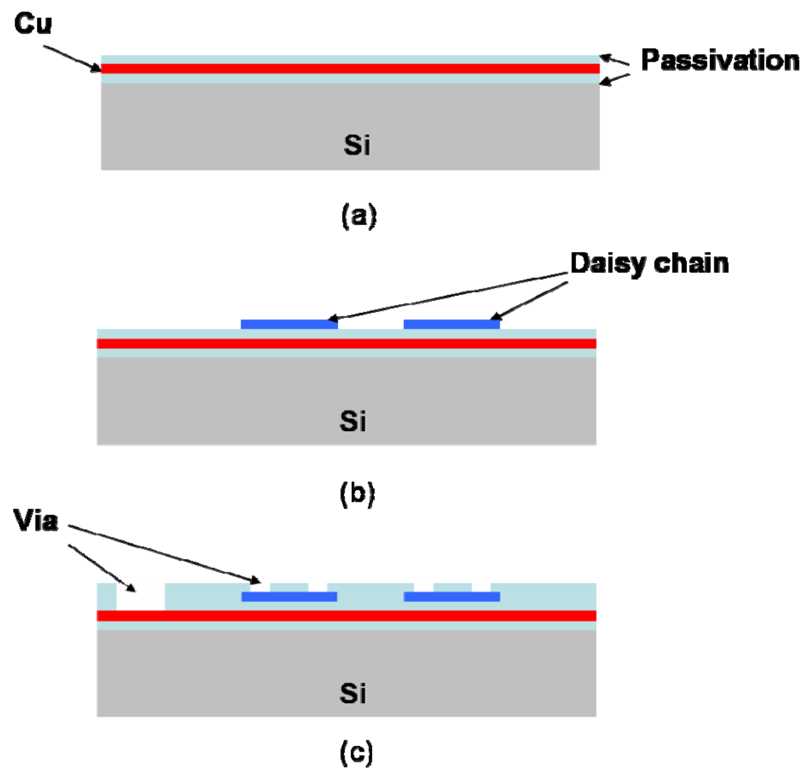
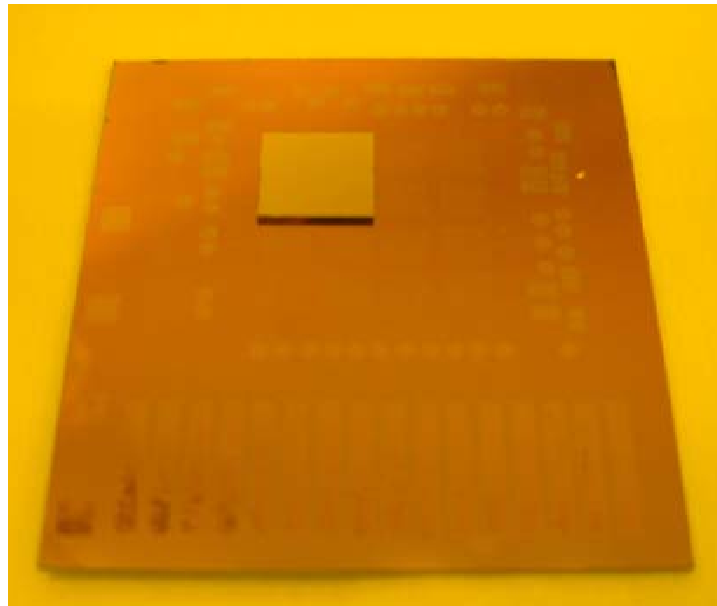
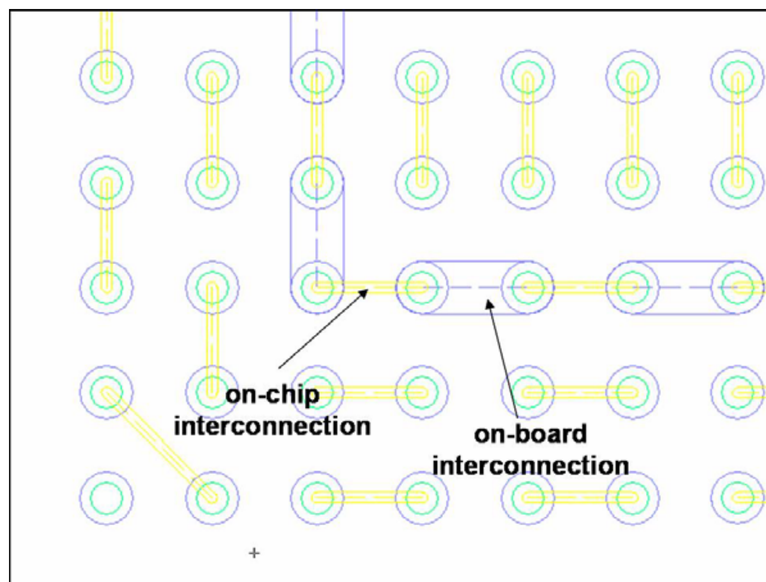


Fig. 4-8 Process flow for Si test board

Since Cu is easily oxidized in air environment, the fabricated test board was immersed in concentrated acetic acid at 30°C for 10 minutes immediately before the assembly process. Furthermore, flux was applied to the test board in order to facilitate the solder bonding when the MCC interconnects were brought into contact with the test board. The flipped test chip was assembled to the test board using Flip-Chip Bonder FC150 by SUSS Microtec. A pressing force of ~2N was applied on the chip to compensate for the standoff height uniformity of MCC interconnects. Considering that there are totally 6724 interconnects distributed on a 10×10mm^2 test chip, it can be easily inferred from previous nano-indentation testing that this pressing force would not bring about any perceivable deformation on the interconnects. The assembled test chip and board were then sent through a 5-zone BTU Model SSA 70 reflow oven. Peak temperature was set as 245°C.



(a)



(b)

Fig. 4-9 Test chip flipped and bonded to Si test board (a) assembled sample; (b) schematic of daisy chain of interconnections

Fig. 4-9(a) shows a 10×10mm^2 flipped test chip assembled onto the left upper quarter of the 20×20mm^2 active area on the test board. Correct alignment of chip to board was verified using X-ray microscopy. As shown in Fig. 4-9(b), electrical path forms in such a way that the signal repetitively goes through on-board

interconnections, MCC interconnects, on-chip interconnections and again MCC interconnects.

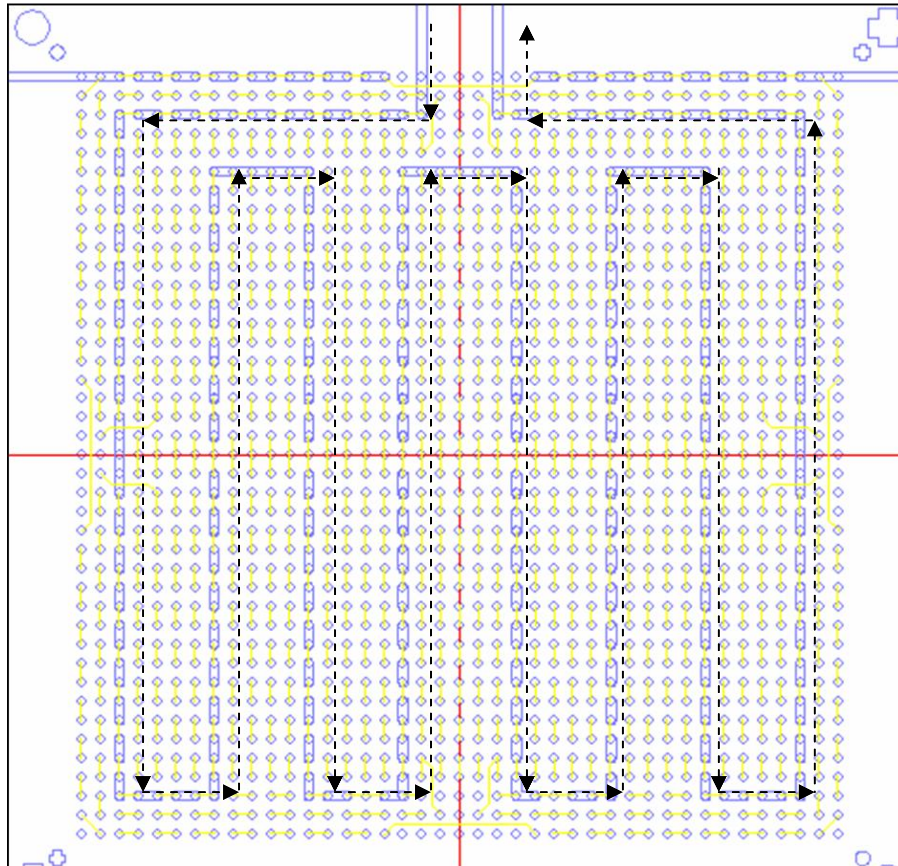
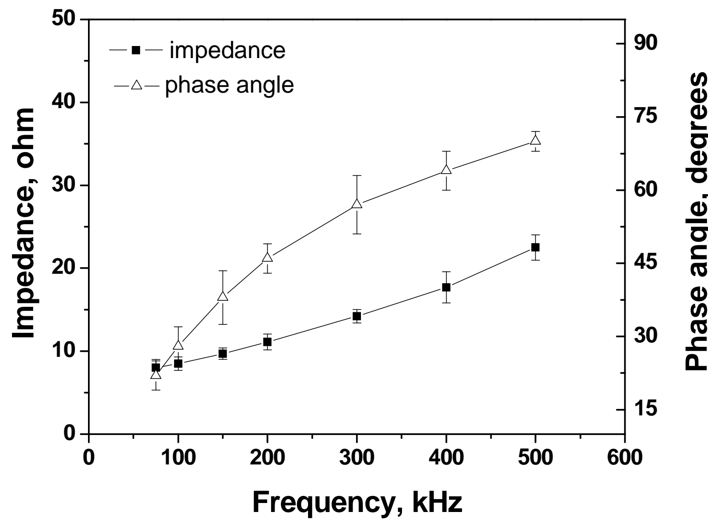


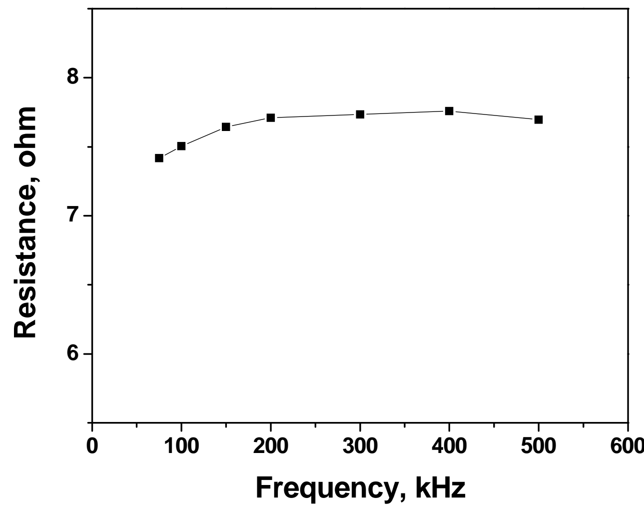
Fig. 4-10 Schematic of daisy chain chosen for electrical measurement

4.2.2 Measurement Results and Discussion

A daisy chain consisting of 374 interconnects and corresponding on-chip and on-board interconnections was chosen for electrical test using Hewlett Packard's precision LCR meter 4285A. Three similar daisy chains were chosen for measurement within a frequency range of 75kHz~500kHz.



(a)



(b)

Fig. 4-11 Electrical measurement of chosen daisy chain (a) impedance & phase angle; (b) resistance extracted from (a)

By probing on the pads at the two ends of chosen daisy chain, the impedance and phase angle were illustrated in Fig. 4-11(a) as a function of frequency. Correspondingly, the resistance R was calculated from the averaged impedance and phase angle as:

$$R=Z\times Cos(\theta) \qquad (4\text{-}1)$$

where Z is the impedance and θ represents the phase angle. Within the frequency range under evaluation, impedance increases almost linearly while the phase angle gradually approaches 90° as a result of increasing inductive reactance. The extracted resistance slightly increases with frequency till 200kHz, but then remains almost constant up to 500kHz.

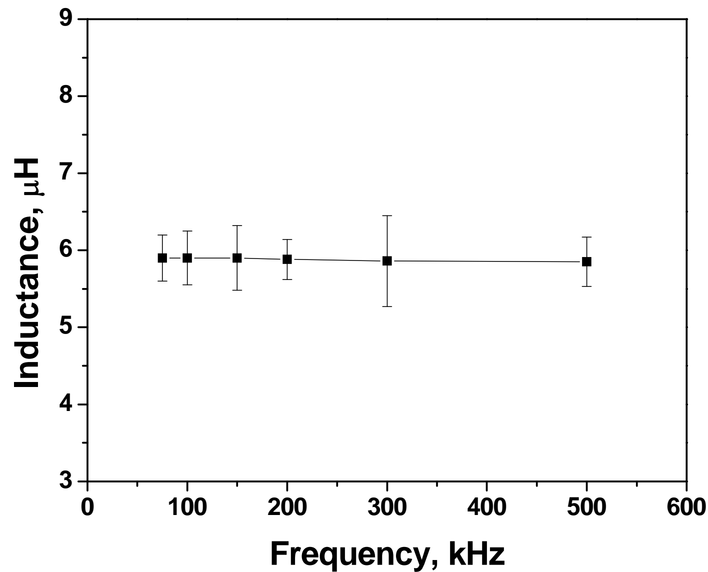


Fig. 4-12 Measured inductance for chosen daisy chain as function of frequency

With one probe contacting the pad at one end of the daisy chain and another probe contacting the ground plane, the inductance and capacitance were measured as functions of frequency as shown in Fig. 4-12 and 13. In this way, the measured inductance qualitatively represents the noise magnitude on a nearby power plane induced by the daisy chain of interconnections. Both inductance and capacitance mildly varies with frequency. Finally, Table 4-1 shows the averaged *R, L* and *C* values, which consist of contributions from one single MCC interconnects, one half of a single on-chip interconnection and one half of a single on-board interconnection.

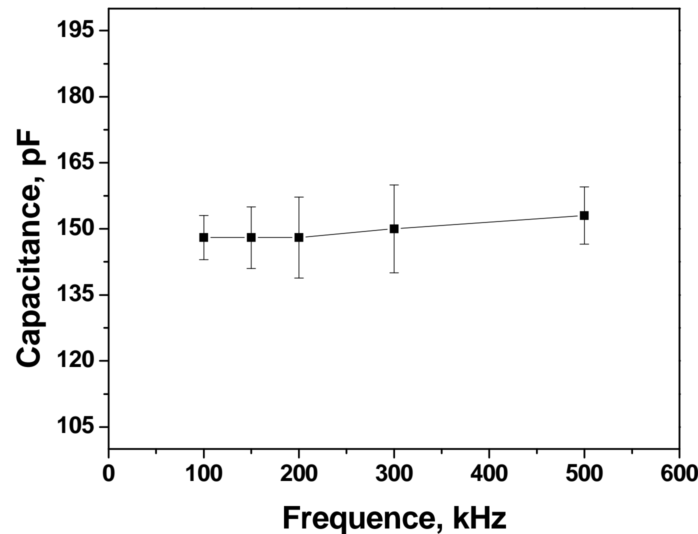


Fig. 4-13 Measured capacitance for chosen daisy chain as function of frequency

Table 4-1 Averaged *R, L* & *C* values at 100kHz

Frequency, kHz	Resistance, mΩ	Inductance, nH	Capacitance, pF
100	21.1	15.8	0.4

4.3 High-frequency Electrical Testing of MCC Interconnects

For very small wafer-level interconnects such as MCC, high-frequency electrical testing faces serious challenges in two aspects. First, the non-planarity of interconnect standoff must be accommodated in the test board design. This can be easily achieved for conventional solder joints because of its low modulus and excellent structural stability. For MCC, however, the non-planarity may be worsen by additional process steps, and also more caution must be taken to control the probing force so that the integrity of the delicate structure can be maintained after testing. Secondly, contact resistance at various electrical interfaces may play a very important role in the test because of the extremely small dimensions of the interconnects, and this contact resistance must be minimized by test board design. A few innovative testing schemes

[68-70] have been proposed to solve the above issues, but they are limited by process complicacy, relatively high cost and also low service life. In this section, a customized set-up based on a trampoline elastomer probe [71] was used to characterize the electrical performance of MCC interconnects up to 20GHz.

4.3.1 Measurement Set-up

Fig. 4-14 shows the schematic of the high-frequency electrical testing set-up used for MCC interconnects. The device under test (DUT, a chip with MCC interconnects in this work) was flipped over with MCC down and located in the slot of the device guide (6). A vertical force is applied onto the DUT by the pressure adjust (1) and spring (4). Because the trampoline contactor (7) underneath DUT consists of Ground-Signal-Ground (GSG) metallization on the basis of highly compliant elastomer as shown in Fig. 4-15, a good electrical contact can be achieved between the MCC interconnects and trampoline probe. The electrical path is further extended to the bismaleimide triazine (BT) printed circuit board (8) and SMA RF connector (5), where a vector network analyzer (VNA) is connected for signal input and output measurement. Fig. 4-16 shows a prototype of customized measurement set-up.

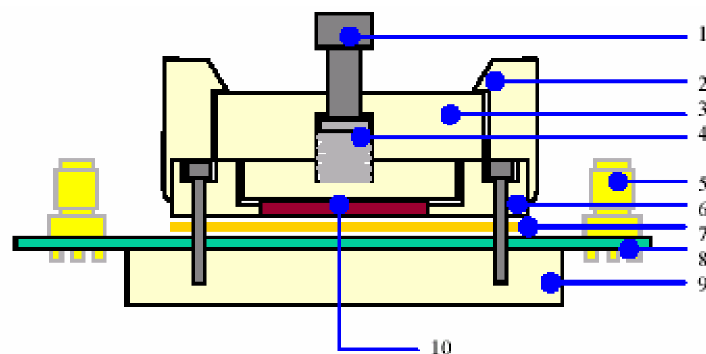


Fig. 4-14 Prototype test socket [71] (1: Pressure Adjust; 2: Screw Clamp lever; 3: Device press plate; 4: DUT press spring; 5: SMA RF connector; 6: Device Guide; 7: Trampoline Contactor; 8: BT PCB; 9: Base Plate; 10: DUT)

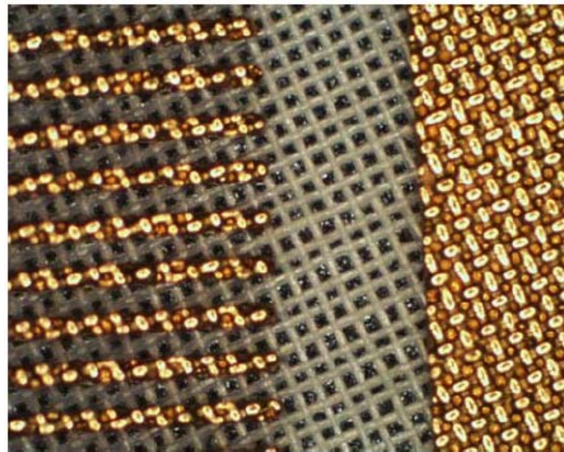


Fig. 4-15 Trampoline elastomer sample with metallization pattern [71]

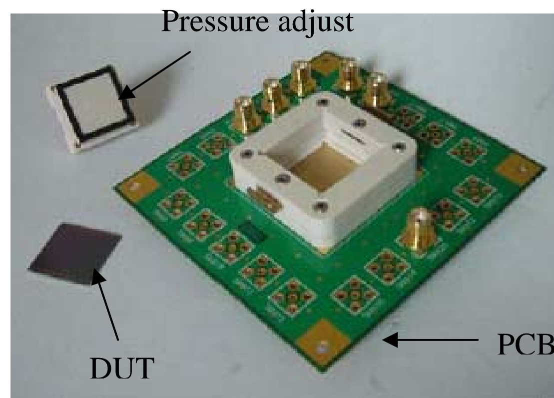


Fig. 4-16 Components of test socket [71]

4.3.2 Results and Discussion

A depopulated 20×20mm^2 test chip with three peripheral rows of MCC interconnects was designed and fabricated for high-frequency electrical characterization using the customized set-up described above. As shown in Fig. 4-17, a coplanar waveguide (CPW) transmission line structure was designed on-chip. When mounted and pressed on the trampoline probe, the on-chip CPW structure was connected to the metallization on the trampoline via the MCC interconnects, and finally to the SMA connector via the metal layers on PCB. Fig. 4-17 shows a close view of the on-chip CPW and MCC interconnect array with 100μm-pitch on a test

chip prototype. In each MCC interconnect, the Cu columns are 30μm high, 5μm in diameter and separated by 5μm.

Fig. 4-18 shows the transmission coefficient magnitude of the system-level measurement results, which consists of contributions from trampoline probe, MCC interconnects, PCB and SMA connectors. It can be observed that the MCC interconnects transmit electrical signal well up to 2GHz where the system demonstrated an insertion loss of ~3dB. To specifically find out the transmission characteristics associated with MCC interconnects, the contribution from other components including PCB and SMA connectors must be deducted. For this purpose, the customized measurement set-up must be further optimized by using low-loss PCB material (e.g., Roger4000 series substrates) or end-launch SMA connector in place of vertically mounted connectors [71].

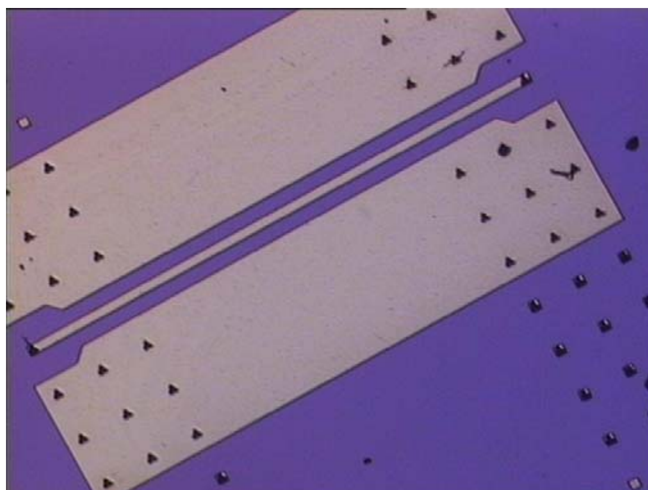


Fig. 4-17 Test chip with GSG structure for electrical characterization

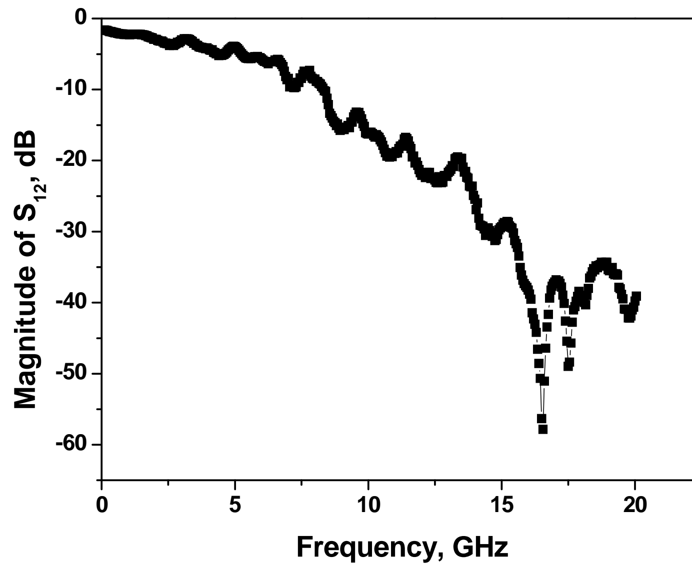


Fig. 4-18 System-level measurement of transmission characteristics

Chapter 5 Thermomechanical Reliability of Compliant Interconnects

For fine-pitch compliant interconnects, it is very challenging to evaluate the thermomechanical damage due to thermal mismatch between the chip and next-level package. In an experimental evaluation of thermomechanical reliability, an assembly process is first implemented, in which the chip with interconnects is flipped over, aligned and joined to a test board through a solder reflow process. For flip-chip solder interconnects available in the market with a typical pitch of ~500μm, the solder joint size is at a level of hundreds of micrometers. Hence, the non-uniformity of the solder height can be easily overcome by the big volume of molten solder and pressing force allowed during the assembly process. For fine-pitch interconnects such as MCC and Planar Microspring, however, the solder size is drastically reduced to less than 50μm, and hence the uniformity issue of the interconnects is much less compensated by the molten solder volume. Furthermore, the presence of delicate structure under solder also limits the pressing force magnitude during the assembly process. Experimental investigation of thermomechanical reliability is further hindered by the shortage of high-quality fine-pitch test boards. Owing to the limitation of processes on printed circuit board (PCB), it is very difficult to achieve the width and spacing of metal traces, and also uniform control of small solder joints required by the fine-pitch (100μm or less) chip-to-package interconnects. As an example, Fig. 5-1 shows a bismaleimide triazine (BT) test board on which daisy chain of 100μm-pitch pad with eutectic 63Sn-37Pb solder finish was fabricated. One can see that at some locations neighboring solder is bridged while in other places solder is not deposited at all.

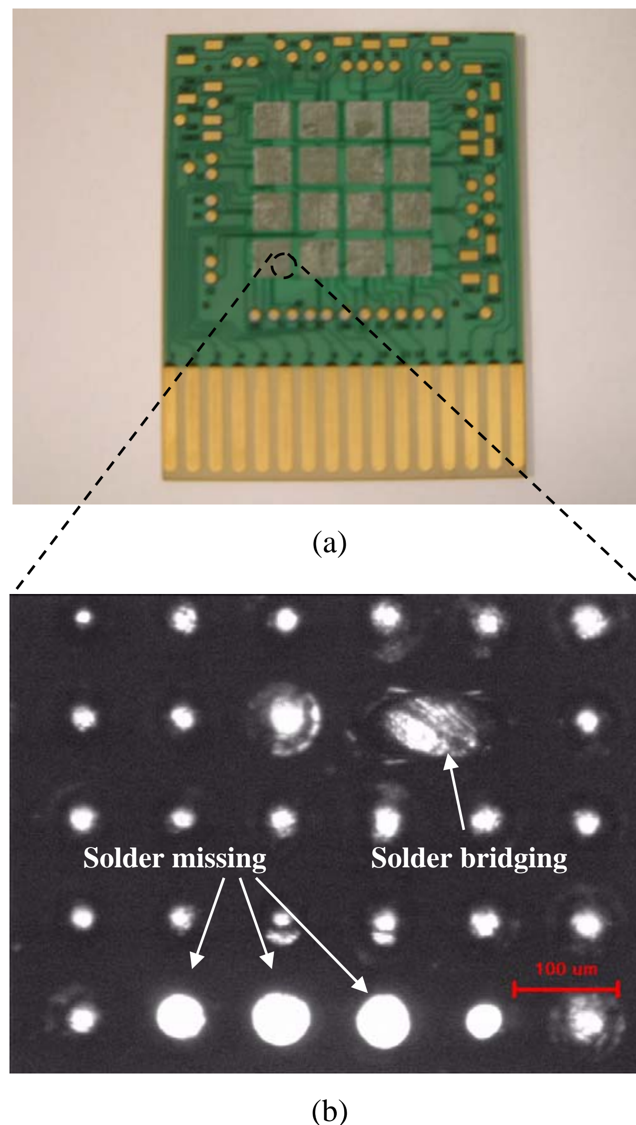


Fig. 5-1 Photograph of 100μm-pitch BT test board with solder finish (a) full view; (b) defects of solder finish

Numerical analysis of thermomechanical reliability can also be a formidable job for fine-pitch compliant interconnects. First, the interconnect count number drastically increases with decrease of pitch for a fixed chip size. For example, if the interconnect pitch is reduced by n times, the interconnect count number increases by n or n^2 times for depopulated layout with peripheral interconnect array or full area interconnect array, respectively. As a result, a huge memory resource capacity may be required for board-level thermomechanical modeling in which both the chip, interconnects and package board have to be included. Secondly, those methods that have been

commonly used to reduce the model size for solder interconnects may not be suitable for compliant interconnects that are composed of solder joint and non-solder flexible structure. For instance, because of the axisymmetric feature of solder joints, board-level modeling of pure solder interconnects can be represented by slice model in which only a strip of the package along the diagonal direction is taken for simulation to reduce the model size. For compliant interconnects like MCC and Planar Microspring, both structures are not axisymmetric and therefore cannot be simplified by a slice model.

Considering the unavailability of high-quality fine-pitch PCB test boards, advanced numerical analysis technique is still utilized to understand the thermomechanical reliability characteristics of MCC interconnects. A solder joint shape modeling software, namely Surface Evolver (SE) 2.23 [72], is first utilized to extract accurate solder joint profiles which is especially important for MCC interconnects. A systematic method is developed to realize seamless integration of solder profile and thermomechanical reliability modeling. Both chip- and board-level analyses are conducted to understand the effects of interconnect geometry upon the thermomechanical reliability performance. Finally, a qualitative correlation between compliance, deformation and reliability performance is established in terms of full area array of single copper column (SCC) interconnects, which provides valuable guidance for design and layout of any compliant interconnects composed of solder joints and non-solder flexible structures.

5.1 Solder Joint Shape Modeling Using Surface Evolver (SE)

5.1.1 Overview of Solder Joint Modeling Techniques

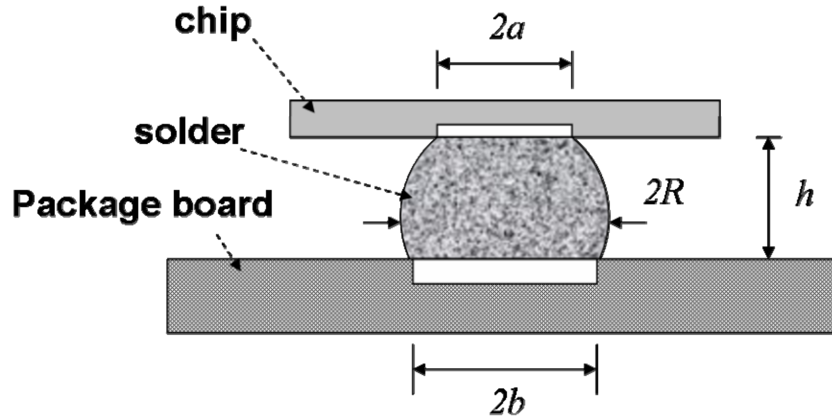


Fig. 5-2 Schematic of double truncated model (DTM) for solder joint

In a typical Ball Grid Array (BGA) package, the geometry of solder joint has significant influence upon its thermomechanical reliability. Numerous researches [73-77] have been conducted to study how the solder joint geometry is affected by design and processes at different fabrication and assembly stages, and also in turn how the solder joint geometry such as solder joint shape and standoff affect the reliability of the interconnects. Solder joint shape prediction is usually implemented using the truncated sphere model [78], force-based analytical method [79,80] or a public simulation tool Surface Evolver [72]. Each of them has its advantages and disadvantages. For a typical flip-chip solder joint after the reflow process, a double truncated model (DTM) as shown in Fig. 5-2 is capable of predicting the solder geometry using the following equations:

$$V = \frac{\pi}{3}\left[\sqrt{R^2 - b^2}\left(2R^2 + b^2\right) + \sqrt{R^2 - a^2}\left(2R^2 + a^2\right)\right] \qquad (5\text{-}1)$$

$$h = \sqrt{R^2 - a^2} + \sqrt{R^2 - b^2} \qquad (5\text{-}2)$$

where V is the solder volume, R is the solder radius, h is the solder joint height, a and b are the chip and substrate pad radius, respectively. Given the solder pad radius and the solder volume, these two equations can be used to predict the solder joint height

and radius, or inversely, with a given desired solder joint geometry, the required solder volume can be calculated and then deposited by an electroplating or a screen printing process. The truncated model is easy to use and able to give the results quickly, but its accuracy is compromised by the fact that all the non-geometry factors affecting the solder shape evolution during solidification are neglected.

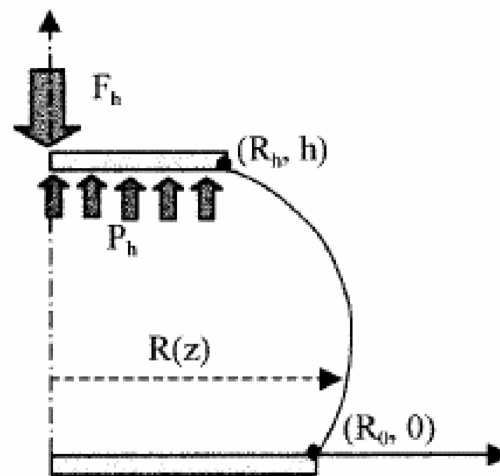


Fig. 5-3 Analytical modeling of solder joint based on force balance [81]

The limitation of DTM can be partially overcome by including the external loading and surface tension force of the molten solder into the analytical model [79-81]. As shown in Fig. 5-3, the molten solder may achieve the final profile under the balance between the external loading F_h (which may be the chip weight), the solder joint internal pressure and the surface tension. However, similar to the DTM, this force-based analytical model is still only applicable to axisymmetric solder joints.

An even more accurate modeling technique utilized minimum energy theory to calculate the solder joint geometry [72,81]. The total energy of a solder joint in molten status consists of three major energy portions: the surface tension energy, the gravitational energy, and the energy due to external forces during solder solidification. The solder profile finally stabilizes when the total energy reaches a minimum value.

Combining with finite element analysis, this solder joint modeling technique can be easily implemented with software tools such as *Surface Evolver* [72] developed by K. A. Brakke, which is no longer limited to axisymmetric solder joints. Another advantage is that the effects of pad wettability on solder joint shape evolution can be investigated.

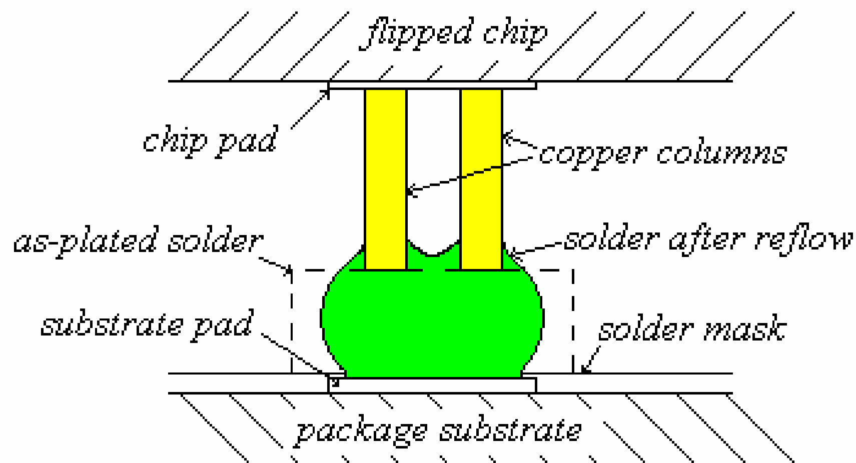


Fig. 5-4 Schematic of special solder joint profile within multi-copper-column (MCC) interconnects

In comparison with conventional pure solder interconnects, the solder joint in MCC interconnects may develop into a distinctive geometry that needs to be taken into account in the thermomechanical reliability study. As shown in Fig. 5-4, when the chip with MCC interconnects is flipped and joined to the package board by a solder reflow process, the molten solder may "*wick*" up along the copper columns as a result of good wettability of Sn-Pb solder on Cu, and thus the copper columns are partially embedded in the solder joint. This specific solder-copper interface may significantly affect the solder joint strain deformation and thus the fatigue life estimation. Since the solder joint of MCC interconnects is no longer axisymmetric as

with typical pure solder joints, *Surface Evolver (SE) 2.23* is utilized throughout this chapter to predict the shape of solder joints.

5.1.2 Solder Joint Modeling for MCC Interconnects

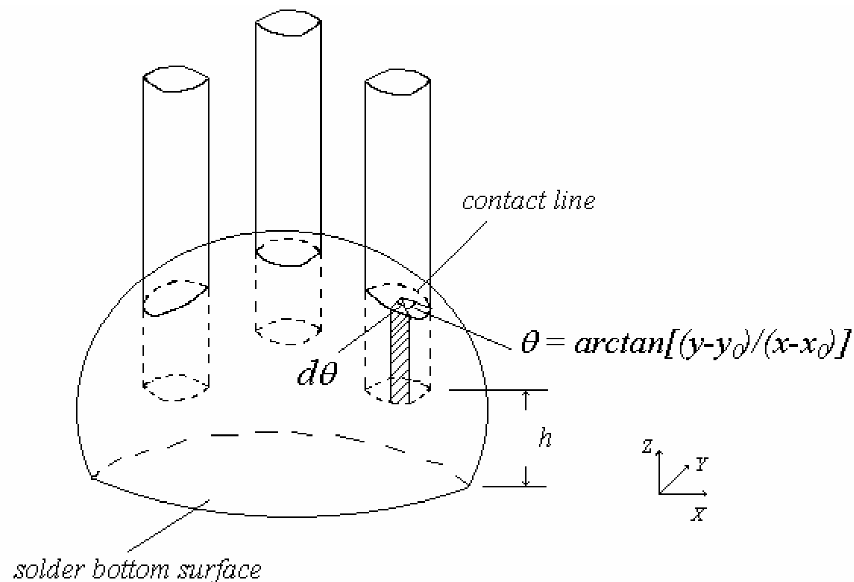


Fig. 5-5 Energy calculation for solder joints of MCC interconnects

For solder joints in MCC interconnects, the equilibrium in a molten state is obtained when a minimum is reached for the sum of three energy components: surface tension energy of the molten solder surface, gravitational energy, and the energy associated with the partial cylindrical surfaces of copper columns that are embedded in the solder. The external energy applied by the self-weight of the chip is neglected. While the calculation of the first two components is straightforward and hidden in the *SE* simulator, the last energy component needs user inputs and can be calculated as follows. As shown in Fig. 5-5, by dividing the embedded cylindrical surface into vertical stripes, the energy *dE* associated with the shaded strip can be expressed as:

$$dE = \gamma \cdot (z - h) \cdot r_c \cdot d\theta \qquad (5\text{-}3)$$

where γ is the surface tension force of solder along the solder-copper interface, z is the vertical coordinate of the solder-copper contact line, h is the standoff height between the copper column and substrate pad, r_c is the copper column radius, and $d\theta$ is the radial angle corresponding to the shaded strip, which can be further calculated as:

$$d\theta = d\arctan\left(\frac{y-y_0}{x-x_0}\right) = \frac{(x-x_0)\cdot dy - (y-y_0)\cdot dx}{r_c^{\,2}} \qquad (5\text{-}4)$$

with (x, y) and (x_0, y_0) being the coordinate values of the contact line and axis of the copper column projected on the horizontal plane, respectively. Hence, the energy associated with the embedded copper column surface can be calculated by combining the above two equations:

$$E = \iint_S dE = \oint_L \gamma\cdot(z-h)\cdot\frac{(x-x_0)\cdot dy - (y-y_0)\cdot dx}{r_c} \qquad (5\text{-}5)$$

where S is the embedded cylindrical surface and L is the contact line. It can be observed from this equation that the energy integral on the area is simplified to an integral on a closed circle. In this work, the standoff height value h is always assumed to be equal to the as-plated solder bump thickness, but one should note that this value may vary during the assembly process due to chip weight or fixture movement of the flip chip bonder.

The MCC interconnect modeling process is illustrated in Fig. 5-6. As shown in Fig. 5-6(a), a hexagonal prism model is first constructed within *SE* simulator to represent the as-plated solder bump. The copper columns need not be included in the solder shape prediction model, because some "*constraint*" conditions are applied to stipulate that: (a) the key points on the solder-copper column contact line remain at the cylindrical surface of copper columns; (b) all of the "*edges*" and "*facets*" on the top surface of the hexagonal prism cannot "*flow*" into the cylindrical holes that

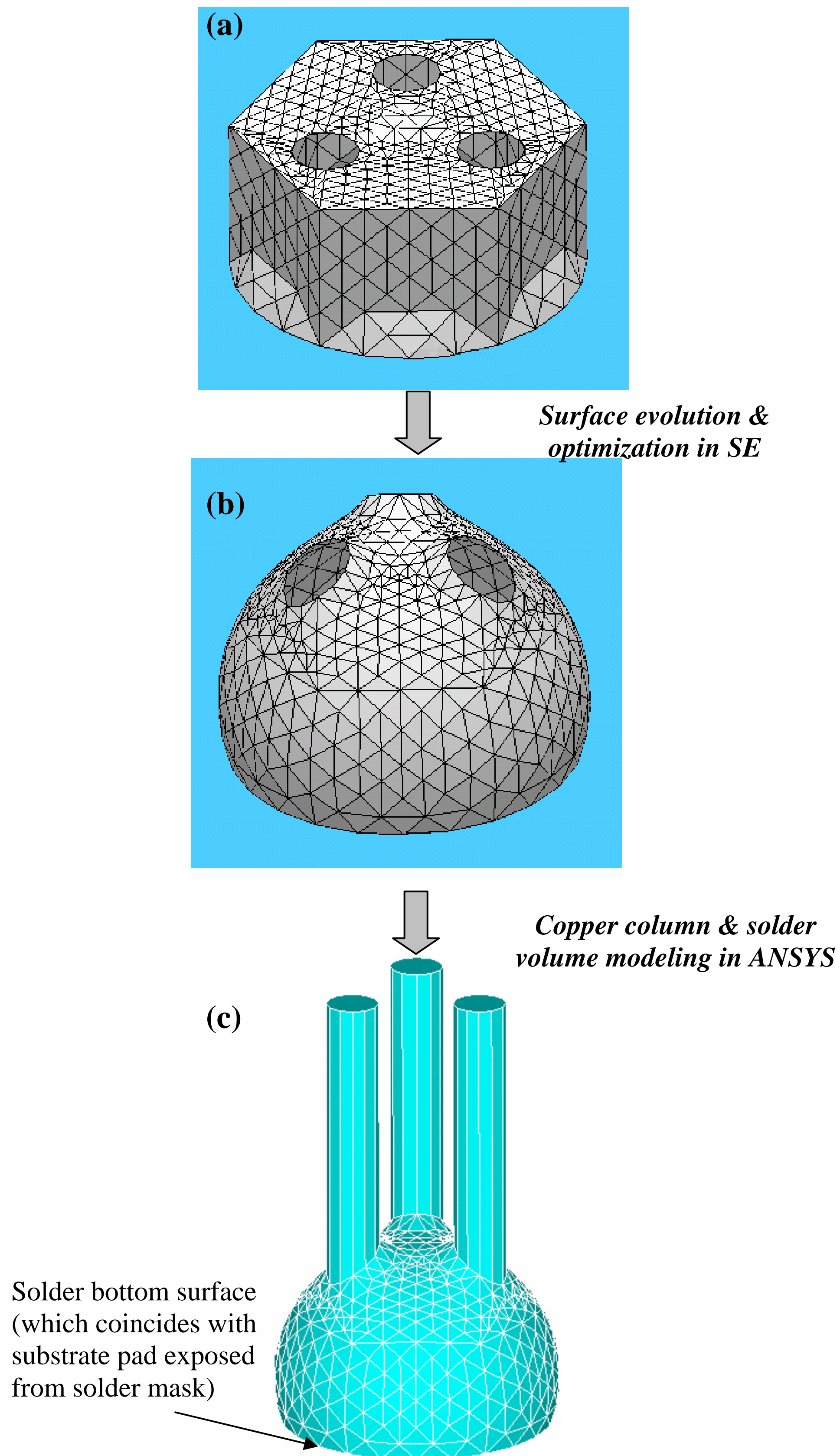


Fig. 5-6 Sequence of solder joint and MCC interconnect modeling (a) original hexagonal prism; (b) evolved solder joint surface; (c) complete interconnect model

represent the copper columns. The solder joint surface evolution continues till the variation of total energy between two consecutive iterations is less than 1%. After getting the initial evolution results, some actions such as "*equiangulation*" and "*tiny edge elimination*" must be taken to optimize the solder surface as shown in Fig. 5-6(b). This is to avoid poorly-shaped facets that would otherwise lead to difficulties or even failure during the volume meshing process in ANSYS that is used for mechanical analysis of solder joints. The coordinates of optimized key points from SE are then exported into ANSYS, where the facets of solder surface are re-formed by connecting the corresponding key points. Finally, copper columns are added to complete the MCC interconnect model for thermomechanical analysis, which is shown as Fig. 5-6(c). Since triangular facets are exported from *SE* simulator into ANSYS, the solder joint is modeled with tetrahedral elements, and quadratic element SOLID92 is used to enhance the calculation accuracy in ANSYS [82]. An example of simulation code for MCC solder joint shape modeling is included in ***Appendix I***.

5.1.3 Solder Joint Bridging Study for Fine-pitch MCC Interconnects

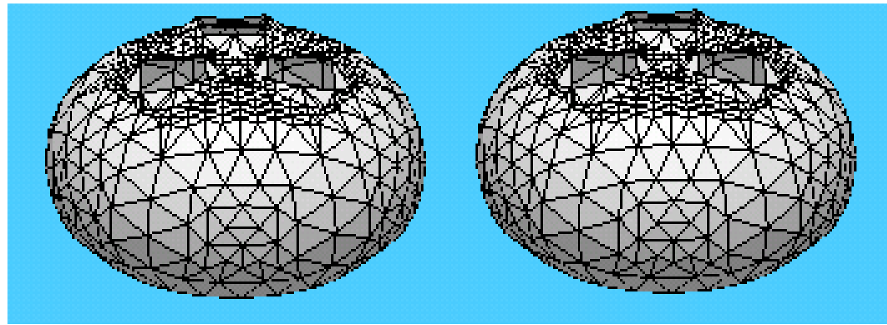
5.1.3.1 Modeling Methodology

For surface mount and flip chip devices that employs solder-based interconnection technology, the solder bridging may not be a marginal issue when the pin or solder interconnect pitch becomes smaller than 200μm. MCC interconnect is meant for high I/O density application, therefore its wafer-level fabrication and assembly process must be carefully controlled to prevent the solder bridging. For conventional solder joints, for a given pitch value, one can directly use Equations (5-1) & (5-2) to predict the required solder volume according to the designed pad dimensions and solder standoff, and thus the solder bridging risk can be easily eliminated. For MCC

interconnects, however, the critical solder volume cannot be worked out in this way because of solder wicking along the copper columns. Instead, *Surface Evolver* is still utilized to solve this problem.

Similar to the procedure as described in Section 5.1.2, two hexagonal prism models are constructed to represent the original solder bumps. An example of simulation code for solder bridging modeling is shown in ***Appendix II***. With the aid of some of the latest features in *SE* such as "*merge*" algorithm, the neighboring solder joints merge into one as soon as overlapping occurs on the surface of two individual joints. It is noted that in an indirect method described in [83], the neighboring solder joints are initially assumed bridged, and then the critical solder volume for bridging is calculated as the volume with which bridged solder joints breaks into individual ones. In comparison, the method used in this thesis simulates the real process of solder shape evolution during solder reflow and thus predicts a more accurate critical solder volume for bridging.

The critical solder volume can be deduced by observing the solder shape evolution while continuously adjusting the solder volume. As an example, for a given set of geometry parameter values, Fig. 5-7 shows the shape evolution of two neighboring solder joints with increase of solder volume. The distance between neighboring solder balls decreases with the increase of solder volume, and finally a stable channel forms between the solder joints after a critical solder volume of 1.488×10^4 μm^3 is reached. As soon as the critical solder volume is exceeded, the extra solder tends to concentrate at the bridging area, rather than wicking up the copper columns. This also led to the observation that the shape evolution of bridging solder joints converges faster than that of individual solder joints.



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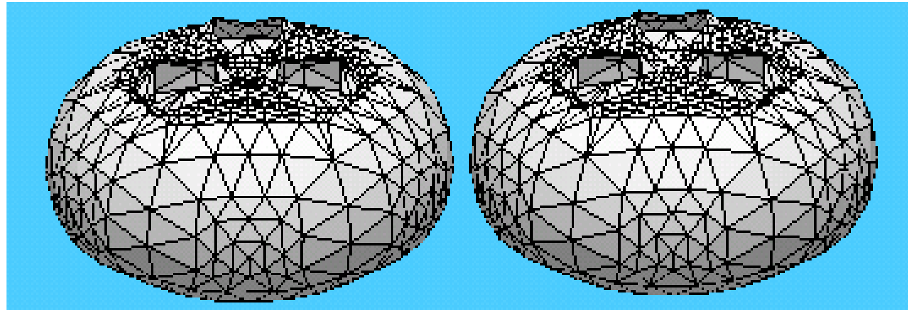

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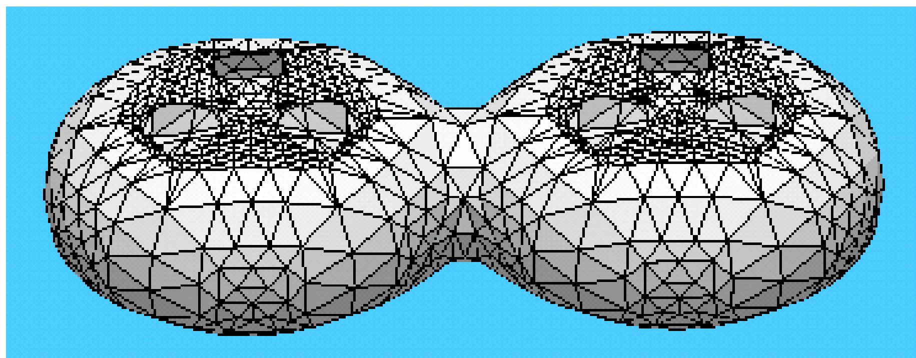

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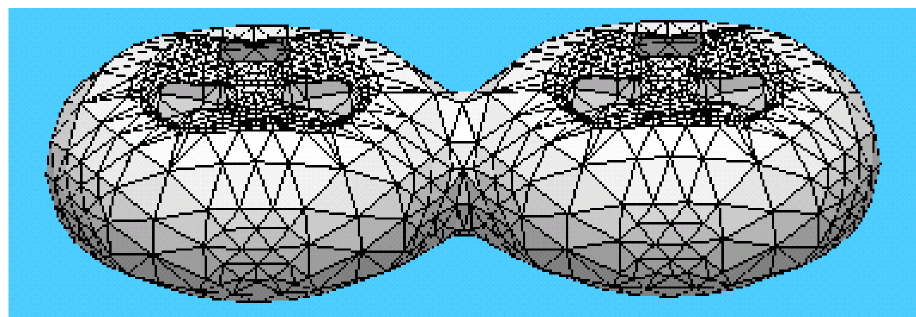


(d)

Fig. 5-7 Solder joint bridging evolution with varying solder volume (a) $V=1.2\times10^4$ μm^3, (b) $V=1.487\times10^4$ μm^3, (c) $V=1.488\times10^4$ μm^3, (d) $V=1.6\times10^4$ μm^3 (substrate pad radius=13μm, as-plated solder thickness=15μm, copper column radius=3.5μm, column spacing=5μm)

5.1.3.2 DoE Analysis of Critical Volume for Solder Bridging

To systematically investigate the solder bridging risk as a function of various geometric parameters of MCC interconnects, a three-level quadratic designed experiment $L_9(3^4)$ [84] is used to study the critical solder volume varying with four variables: as-plated solder bump thickness (10→15→20μm); substrate pad radius (10→13→16μm); copper column radius (1.5→2.5→3.5μm) and column spacing (5→7.5→10μm), which have been shown in Fig. 5-4.

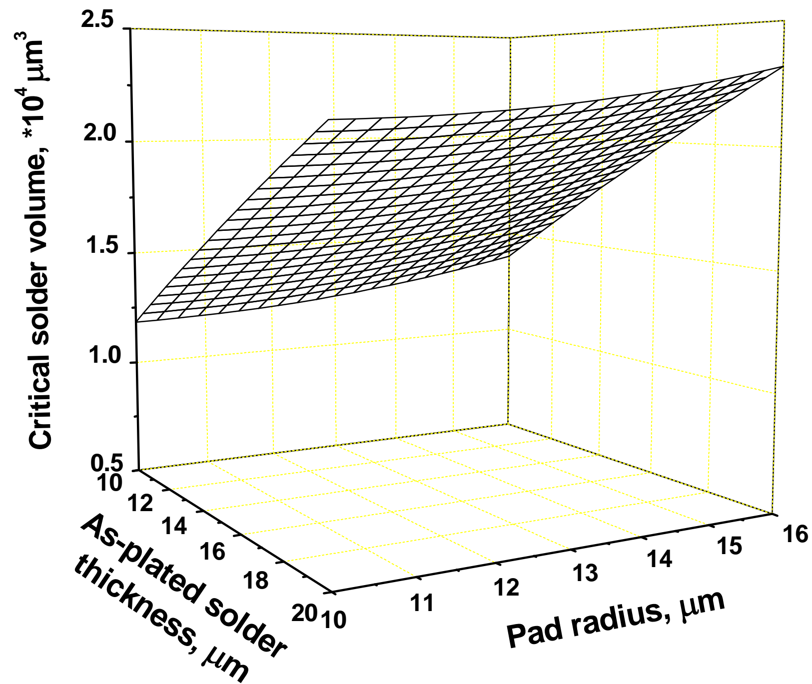
Table 5-1 Geometric parameters for DoE simulation for solder bridging

Run #	As-plated solder bump thickness, μm	Substrate pad radius, μm	Copper column radius, μm	Copper column spacing, μm
1	10	10	1.5	5
2	10	13	2.5	7.5
3	10	16	3.5	10
4	15	10	2.5	10
5	15	13	3.5	5
6	15	16	1.5	7.5
7	20	10	3.5	7.5
8	20	13	1.5	10
9	20	16	2.5	5

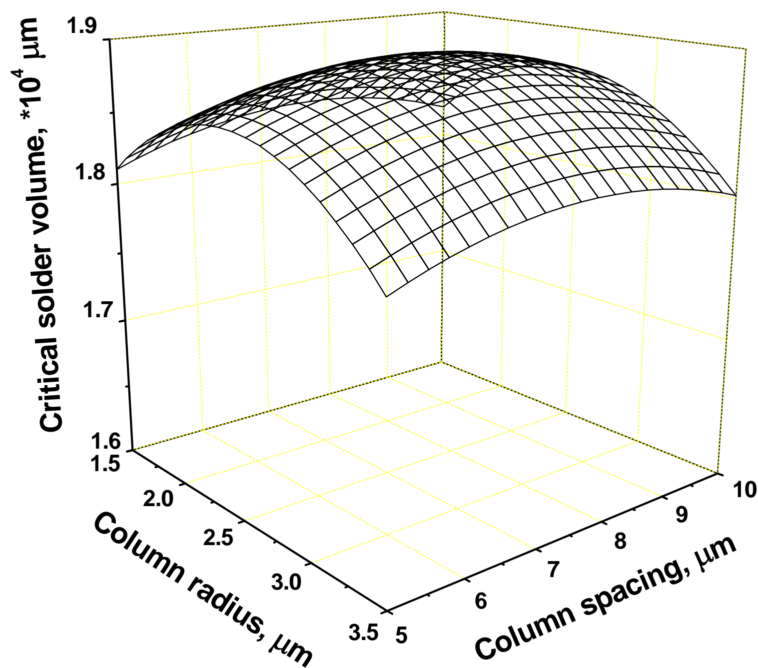
The correlation between the critical solder volume (V_{cr}) and the above geometric parameters can be formulated as:

$$V_{cr} = C_1+C_2X_1+C_3X_1^2+C_4X_2+C_5X_2^2+C_6X_3+C_7X_3^2+C_8X_4+C_9X_4^2 \qquad (5\text{-}6)$$

where X_1~X_4 represent various geometric parameters while C_1~C_9 are coefficients depending on interconnect geometry and material properties as well. Hence, all the coefficients can be extracted by fitting results of 9 simulation runs to the above

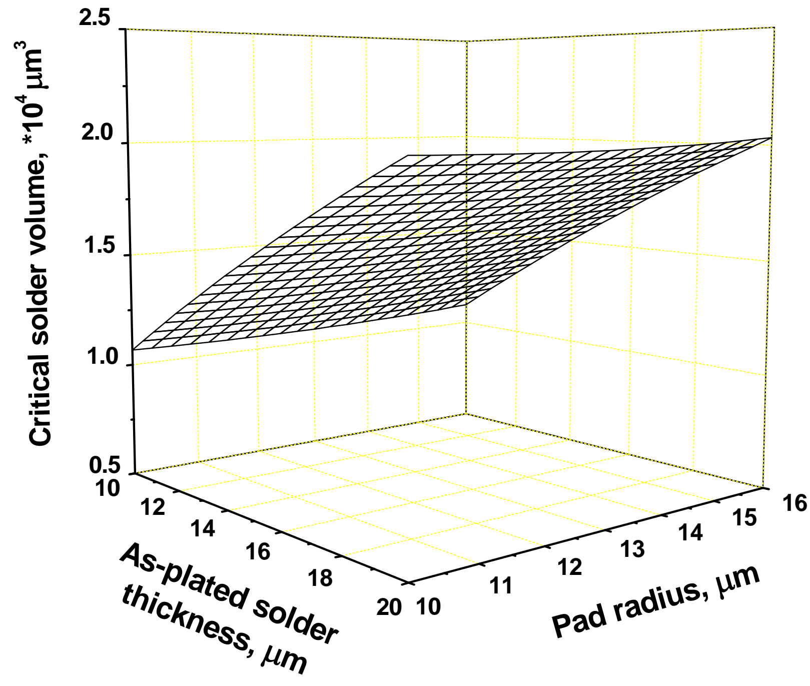


(a)

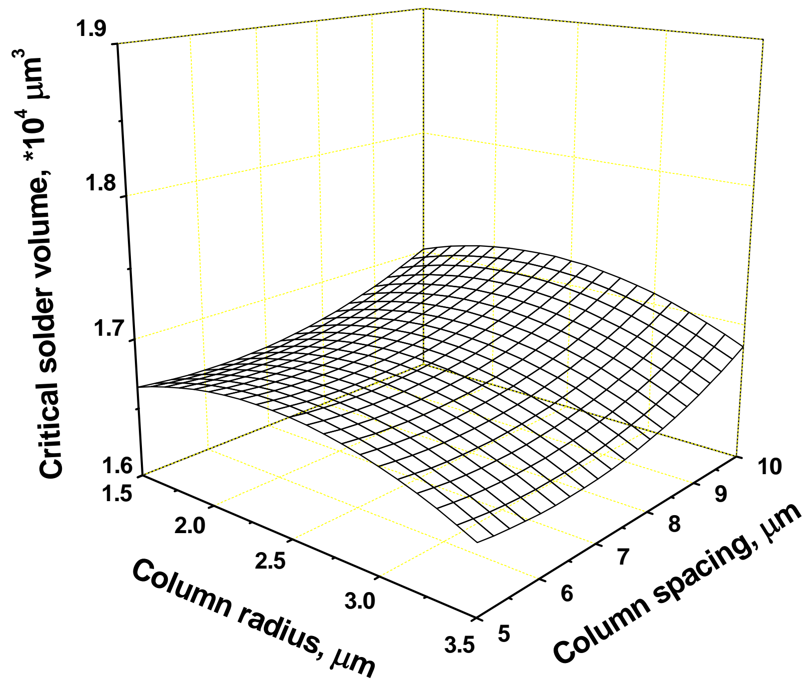


(b)

Fig. 5-8 Response of critical solder volume for TCC solder joint to (a) as-plated solder thickness & substrate pad radius with column radius 2.5μm and column spacing 5μm; (b) copper column radius & spacing with substrate pad radius 13μm and as-plated solder thickness 15μm



(a)



(b)

Fig. 5-9 Response of critical solder volume for QCC solder joint to (a) as-plated solder thickness & substrate pad radius with column radius 2.5μm and column spacing 5μm; (b) copper column radius & spacing with substrate pad radius 13μm and as-plated solder thickness 15μm

formula. It should be pointed out that in the solder bridging study, the interconnect pitch is set to 40μm, which is the minimum pitch that has been achieved in fabrication. The geometric values in each simulation run are shown in Table 5-1. Solder properties used in the simulation include the density [79,81] of 9.28×10^{-12} g/μm^3, surface tension 4.63×10^{-7} N/μm [79,81] and wetting angle 20° on Cu.

Figs. 5-8 & 5-9 show the response surface of critical solder volume for Triple-Copper-Column (TCC) and Quadruple-Copper-Column (QCC) interconnects, respectively. It can be observed that the substrate pad radius, column radius and spacing have quite a weak influence on the critical solder volume. Interestingly, the critical solder volume increases almost linearly with the as-plated solder bump height. This is in contrast to the pure solder interconnect, in which the critical solder volume for bridging should be a constant given a fixed pad radius and pitch. A higher as-plated solder thickness in MCC interconnects means that the copper columns are located at a higher distance from the substrate pad. Owing to the surface tension and solder wetting on the Cu column, the molten solder "*wicks*" up along the column to a certain distance. In other words, the copper columns may exert a "*lifting-up*" force on the molten solder that counteracts the downward gravitational effects of solder. Hence, with a higher as-plated solder thickness or a higher distance between copper columns and substrate pad, the molten solder during reflow process is "*pulled*" up to an increased height and as a result, a higher solder volume can be accommodated without bridging. It should be noted, however, that the molten solder may no longer absorb onto the copper columns if the distance between copper columns and substrate pad exceeds a limit. Based on above results, the solder volume can be maximized by adjusting the solder plating dimension while bridging risks can be eliminated. A higher solder volume is preferred for both assembly and reliability performance.

5.2 Thermomechanical Reliability of Individual MCC Interconnects

In this section, an individual MCC interconnect is taken to study the effects of various geometric and material factors on its resistance to thermomechanical failure. In addition, the influence of multiple copper column orientation upon the solder joint fatigue damage is also investigated. Finally, in combination of solder joint modeling using *Surface Evolver 2.23*, thermomechanical failure characteristics as well as their dependence upon the interconnect geometry is calculated with ANSYS 6.1.

5.2.1 Modeling Methodology

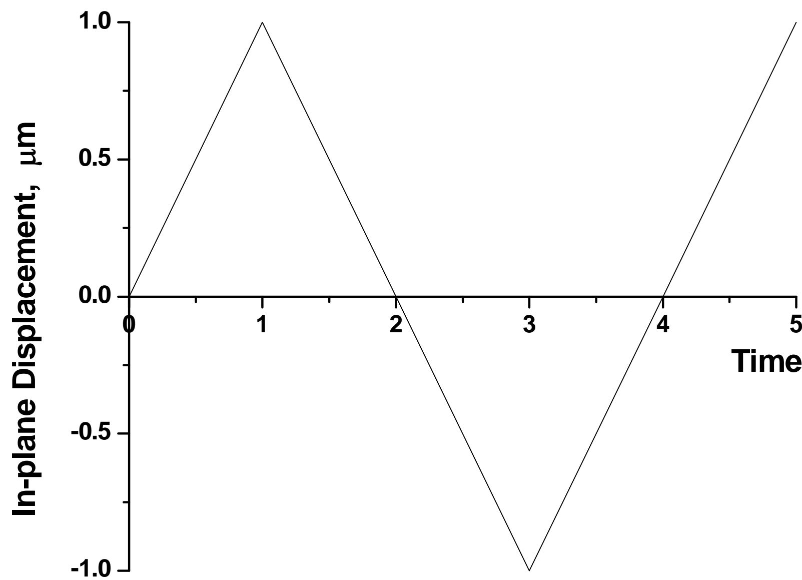


Fig. 5-10 Cyclic shear displacement loading applied to solder joint

For a given MCC interconnect, the solder joint shape is first extracted from SE simulator based on solder volume, as-plated height, substrate pad radius, copper column geometry and arrangement. Details of solder joint shape modeling within SE and its integration with ANSYS 6.1 were described in Section 5.1.2. The solder density and surface tension are assumed to be 9.28×10^{-12} g/μm^3 and 4.63×10^{-7} N/μm, respectively. While a fixed boundary condition is applied to the copper column ends

away from the solder joint, a cyclic shear displacement loading as shown in Fig. 5-10 is applied to the solder joint bottom surface (refer to Fig. 5-6(c)), mimicking the shear deformation of interconnects due to thermal mismatch of chip and package substrate that were subjected to temperature cycling. It should be noted that the horizontal coordinate of Fig. 5-10 does not mean a real "*time*" but it is only used to represent the loading history. Actually, the time-dependent creep behavior of solder is not considered in this thesis. Table 5-2 shows the mechanical properties of electroplated Cu and 63Sn37Pb solder used in ANSYS simulation. Finally, the solder element with maximum equivalent plastic strain range [85] during the pseudo time period of 1~5 is identified as the failure site. The corresponding equivalent plastic strain range values are taken for comparison of fatigue damage in various scenarios.

Table 5-2 Mechanical properties of electroplated copper and 63Sn37Pb solder

	Electroplated Copper	63Sn37Pb Solder
Elastic modulus, GPa	127.4	33.58
Poisson's ratio	0.36	0.4
Yield strength, MPa	262.4	30.2
Hardening coefficient, MPa	315	33.9
Hardening exponent	0.54	0.033

5.2.2 Effects of Solder Joint Modeling Techniques: SE vs. DTM

To justify the application of SE simulator, the geometry of a solder joint of the same volume is modeled by Double Truncated Model (DTM) and Surface Evolver (SE) 2.23, respectively, and the strain damage within a loading cycle is subsequently calculated and compared. The geometrical parameters used in this modeling are given in Table 5-3. For DTM solder modeling, with a given solder volume, substrate pad

radius and solder ball height, the solder ball geometry can be fully determined using equations (5-1) and (5-2). For the purpose of SE modeling, however, other material property inputs such as the wetting angle of solder on Cu, solder density and surface tension force are required. Depending on whether the solder is treated in flux, the wetting angle of eutectic PbSn solder on Cu surface ranges from 11° to over 40° [86,87]. In this section, an intermediate wetting angle of 20° is used in the SE modeling of the solder joint shape.

Table 5-3 Geometry of MCC interconnect for Surface Evolver & DTM modeling

	DTM	TCC	QCC
Solder volume, μm^3	7213	7213	7213
Solder height, μm	12.1	-	-
Substrate pad radius, μm	13	13	13
Copper column radius, μm	2.5	2.5	2.5
Copper column spacing, μm	5	5	5
Copper column height, μm	30	30	30

For DTM solder model, the solder joint and copper column models can be directly established in ANSYS. For the SE solder model, the solder joint shape is obtained by the method described in Section 5.1.2 and then exported into ANSYS to construct the interconnect model with addition of copper columns as shown in Fig. 5-6(c). Because of the non-axisymmetric feature of the MCC interconnects, however, it is anticipated that the deformation particularly the strain damage behavior of the solder joint may significantly depend upon the shear loading direction with respect to the copper column pattern orientation. Fig. 5-11 illustrates a schematic of MCC interconnect viewed with solder bottom surface up, where the solid and dashed circle represent the solder and copper columns respectively. A loading direction parameter, α, is defined

as the acute angle between the shear loading direction and the Y-axis. From a careful analysis of the symmetry of the interconnect structure, it is concluded that an α value of 0°~30° and 0°~45° could be taken to represent all possible shear loading directions for TCC and QCC interconnects, respectively. A cyclic shear displacement loading as shown in Fig. 5-10 is applied to the bottom surface of the solder joint (see Fig. 5-6(c)).

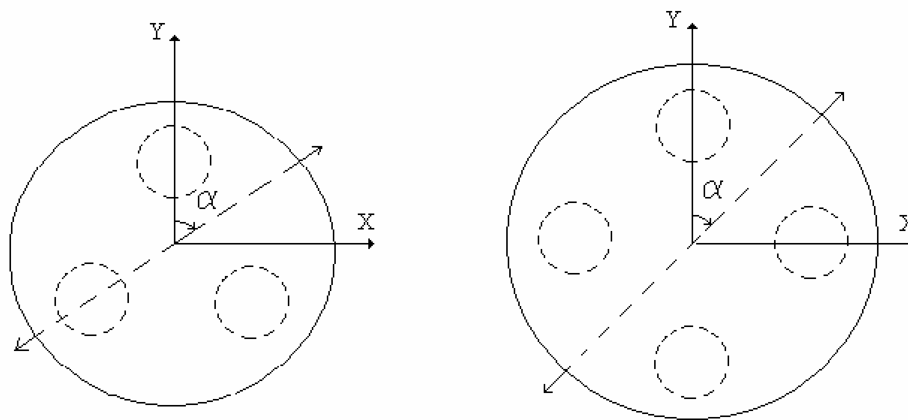


Fig. 5-11 Shear loading orientation for TCC and QCC interconnects

The variation of the plastic strain range of solder joints of TCC and QCC interconnects with loading angle α obtained using both SE simulator and DTM is shown in Fig. 5-12. Several conclusions can be made. First, a remarkable difference in strain damage is found between the plastic strain ranges of SE and DTM models. The SE model predicts a plastic strain range more than 50% lower than that the DTM model for both TCC and QCC interconnects. This clearly demonstrates the importance of accurate solder joint shape prediction. Secondly, the SE and DTM solder models predict different preferential loading angles, along which a minimum plastic strain range occurs within the solder joints. This difference can be related to the different solder-copper interface geometry obtained using SE and DTM models.

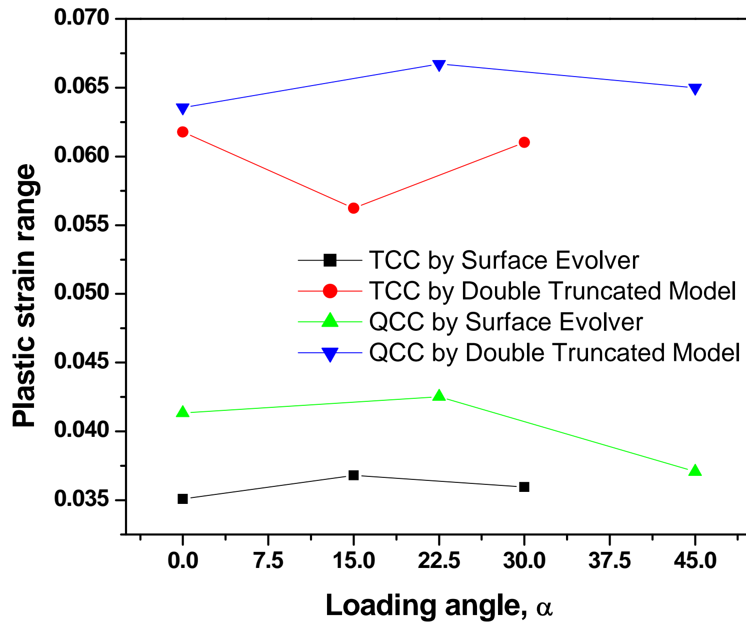
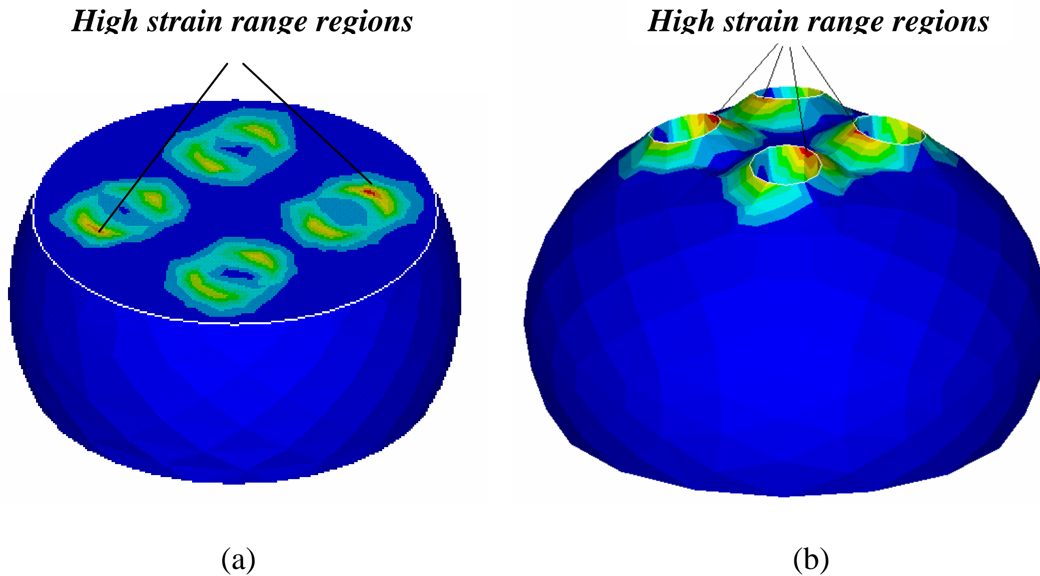


Fig. 5-12 Comparison of plastic strain range based on SE & DTM solder modeling

Thirdly, it has been mentioned that the upward movement of the solder along the copper column surface results in solder fillets around the copper columns. In fact, the solder fillets are not symmetric about the vertical axis of the corresponding copper columns. A close observation of the solder fillet around a single copper column reveals that the fillet is higher at the side facing the centre of the solder joint, but lower at the opposite side, as shown in Fig. 5-13(b). Clearly, this leads to a more complex loading direction dependence of the fatigue behavior for solder joints obtained by the SE simulator. Fig. 5-13 also illustrates the preferential failure sites for solder joints predicted using DTM and SE, respectively. For DTM, the location of maximum plastic strain range is found at the junction between copper columns and the solder joint while with SE, it occurs in the solder fillets adjacent to the copper columns.



(a) (b)

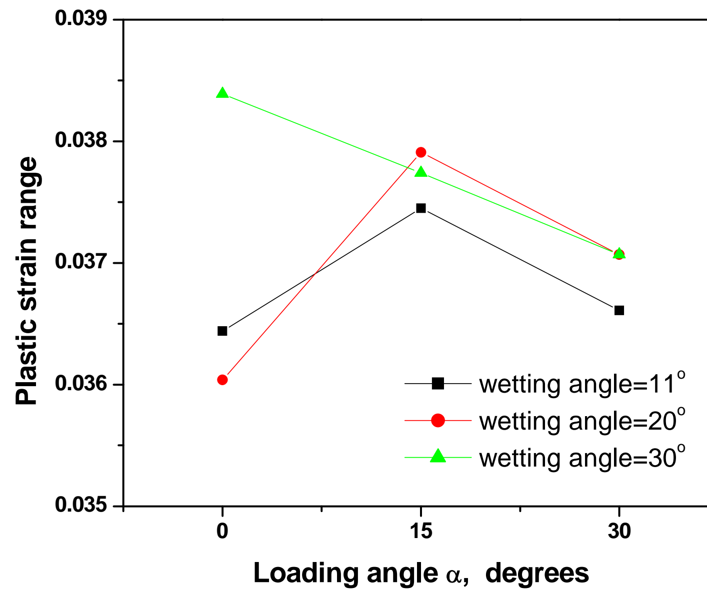
Fig. 5-13 High strain regions in solder joints obtained by (a) DTM; (b) SE

5.2.3 Effects of Loading Direction and Solder-Copper Wetting Angle

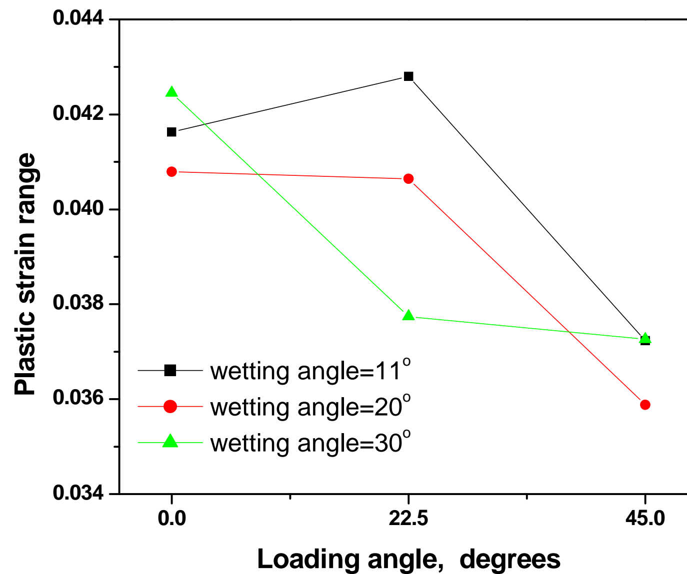
In this section, more simulations are conducted to study the influence of loading direction, solder-copper wetting angle and their interaction upon the fatigue damage of solder joints. Most of the model geometry and materials properties are still the same as that in the previous section, except that the solder volume is taken to be 7450μm^3 for QCC interconnects.

Fig. 5-14 shows the plastic strain range variation with different wetting angles and loading directions. For TCC interconnects, the loading orientation that results in the minimum plastic strain range is dependent on the solder-copper wetting angle as shown in Fig. 5-14(a). With a wetting angle of 11° or 20°, a minimum plastic strain range is obtained when the loading angle is zero. As the wetting angle increases to 30°, however, a maximum plastic strain range is obtained instead when loaded along the 0° direction while a minimum plastic strain range occurs when loaded along the 30° direction. In practice, as long as the flux is properly applied during the assembly process, the solder-copper wetting angle can be easily controlled below 20°. Therefore,

less fatigue damage and hence longer service life can be achieved for TCC interconnects on the condition that the major shear loading direction is maintained parallel to the Y-axis as shown in Fig. 5-11(a).



(a)



(b)

Fig. 5-14 Effects of loading angle and wetting angle on plastic strain range (a) TCC; (b) QCC interconnects

For QCC interconnect, Fig. 5-14(b) shows that a minimum plastic strain range is always obtained when the interconnect is loaded along the 45° direction, regardless of the solder-copper wetting angle. It is noted that in an area-array package, the solder joints along the diagonal direction of the package is subjected to the highest deformation among all the joints. Therefore, the above simulation results indicate that the TCC (or QCC) interconnects should be arranged in such a manner that the α=0° (or α=45°) direction should be along the diagonal direction of the chip or packages. On the other hand, no monotonic dependence of fatigue damage on the wetting angle can be determined from Fig. 5-14. It can be inferred, however, that an interaction between the wetting angle and loading direction may exist in terms of their influence on fatigue damage.

5.2.4 DoE Analysis of Individual Interconnect Reliability

In the previous section, the importance of accurate solder shape modeling using *Surface Evolver* has been shown by revealing the remarkable difference in fatigue damage obtained between SE and conventional DTM modeling. It has also been shown that the solder wetting angle and the interconnect orientation play a role in the solder joint reliability due to the unique solder-Cu interface and the non-axisymetric feature of interconnect geometry. In the following, the interconnect geometry such as the copper column height and diameter, will be investigated in a systematic manner to understand their effects on the interconnect reliability.

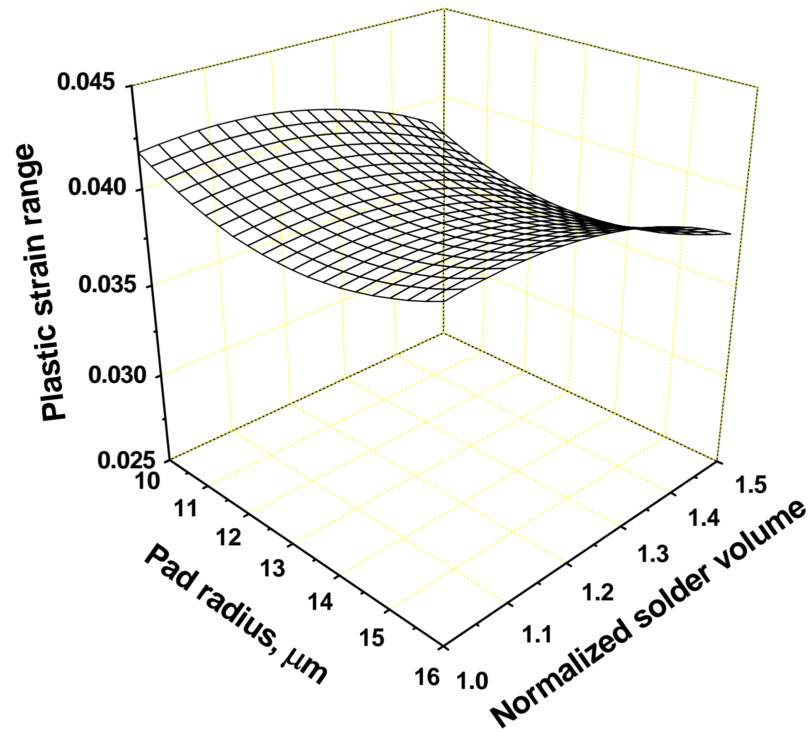
The cyclic shear displacement loading as shown in Fig. 5-10 is still applied to the solder bottom surface as shown in Fig. 5-6(c). A loading angle of zero and solder wetting angle of 20° are employed while the other material properties are maintained the same as before. By using the DoE technique, four geometric parameters are

studied in terms of their effects on solder joint reliability: substrate pad radius (10→13→16μm), solder volume (9000→11500→14000μm^3), copper column radius (1.5→2.5→3.5μm) and column spacing (5→7.5→10μm). The Taguchi's thee-level orthogonal array [84], $L_9(3^4)$, is utilized to study the effects of these four geometric parameters on fatigue deformation of the Triple-Copper-Column (TCC) interconnects. The geometric parameters for each simulation run are summarized in Table 5-4.

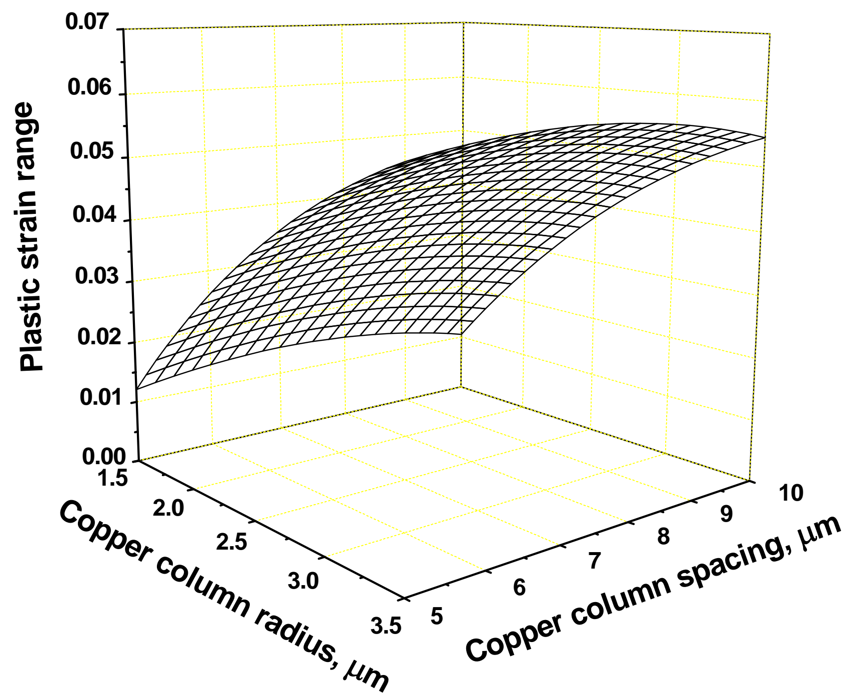
Table 5-4 Geometric parameters for DoE simulation for interconnect geometry effects on solder joint reliability

Run #	Solder volume, μm^3	Substrate pad radius, μm	Copper column radius, μm	Copper column spacing, μm
1	9000	10	1.5	5
2	9000	13	2.5	7.5
3	9000	16	3.5	10
4	11500	10	2.5	10
5	11500	13	3.5	5
6	11500	16	1.5	7.5
7	14000	10	3.5	7.5
8	14000	13	1.5	10
9	14000	16	2.5	5

Using the same procedure described in Section 5.1.3.2, the response surface of plastic strain range as a function of the geometric parameters in Table 5.4 can be obtained by regression analysis. The highest plastic strain range is always observed at the solder fillets around the copper column with Fig. 5-13(b) as an example. As shown in Fig. 5-15, a larger solder volume leads to reduced plastic strain range response, because the additional solder "*wicks*" up further along the copper column and the solder fillets are less deformed as a result of the larger distance from the



(a)



(b)

Fig. 5-15 Response of plastic strain range in TCC solder joint to (a) substrate pad radius & solder volume normalized to $9000\mu m^3$ with column radius=2.5μm and spacing=5μm; (b) copper column radius & spacing with substrate pad radius=13μm and solder volume=$9000\mu m^3$

solder bottom surface where the shear displacement is applied. The substrate pad radius may have opposite effects on solder deformation. On one hand, increasing substrate pad radius results in short and bulky solder profile that reduces effective shear displacement transferred to the solder fillets at the solder-copper column interface. On the other hand, with a given solder volume, the "*wicking*" distance of solder decreases with increase of substrate pad radius, therefore the deformation of those critical solder elements is less restrained by the copper columns. It could be observed from Fig. 5-15 that for the MCC interconnects with the current dimensions, these two effects nearly cancel each other and as a result the substrate pad radius demonstrates only a weak influence on the solder joint reliability. Finally, a significantly reduced plastic strain range is observed with decreasing copper column radius as expected, since slimmer copper columns are able to absorb more shear deformation. However, it should be stressed again that the current analysis is conducted on a single interconnect, of which the shear displacement is assumed to be unaffected by other interconnects and hence the results only reflect the intrinsic fatigue resistance of interconnects with various geometric parameters. In practice, however, for high I/O density packages with uniform area array of miniaturized compliant interconnects, all the interconnects have a synergistic effect on the deformation of the critical interconnect. In other words, the shear deformation of the critical interconnect is not only determined by package dimension, temperature variation and thermal mismatch, but also significantly dependent upon the geometry of each interconnect geometry. In such case, board-level simulation has to be conducted to investigate the deformation behavior of these compliant interconnects as to be shown in the following section.

5.3 Board-level Thermomechanical Reliability of MCC Interconnects

5.3.1 Overview of Thermomechanical Reliability Modeling Techniques

For modern electronic packages such Ball Grid Array (BGA), there have been a few board-level modeling techniques commonly accepted for evaluation of fatigue damage on interconnects due to thermal mismatch between the package and the motherboard. According to the modeling level and material properties used in the calculations, these techniques can be categorized as [88]: 1) nonlinear slice model; 2) nonlinear global model; 3) nonlinear global model with linear super elements; 4) linear global model with nonlinear sub-model; 5) nonlinear global model with a nonlinear sub-model.

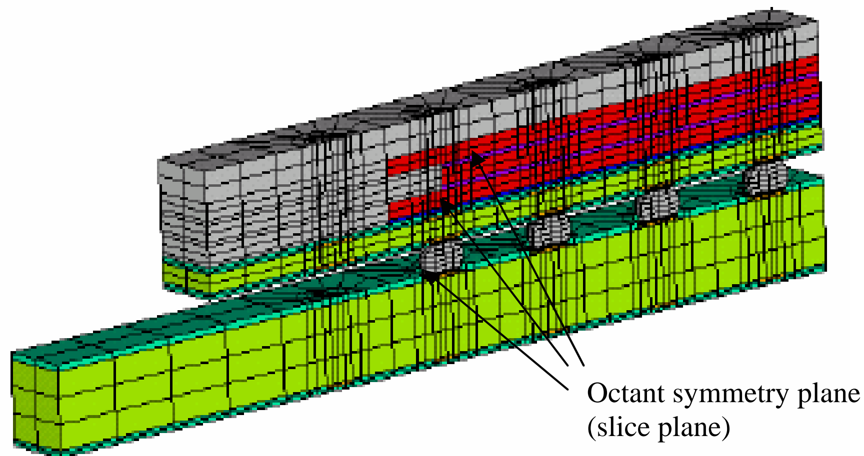


Fig. 5-16 Slice model for solder joint reliability prediction[89]

As shown in Fig. 5-16, the slice modeling technique takes advantage of the octant symmetry feature of a package to simplify the model and thus the computation time is highly reduced. Non-linear material models have to be applied to solder since its strain damage is directly calculated in this slice model. The slice plane coincides with the octant symmetry plane and thus the symmetrical boundary conditions are applied. The back surface opposite to the octant symmetry plane is assumed parallel to the

slice plane, which implies that the package is infinitely long in the direction perpendicular to the slice plane. As a result, the shear strain damage of the solder joint during temperature cycling is over-estimated and thus the fatigue life is under-estimated. As can be seen from Fig. 5-16, both chip, interconnects and package board are included in the model, and fine meshes have to be applied in the solder interconnects to obtain accurate strain values. The required computation resources may become formidable if tens of solder joints have to be considered in the model, which is actually the case for ultra-fine-pitch interconnects such as MCC. The non-axisymmetric geometry of MCC interconnects also limits the application of the slice model.

To eliminate the limitations due to the assumption of symmetrical boundary conditions, global modeling has to be conducted with penalty of huge computational resources. To solve this problem, all the components including the package, PCB and non-critical interconnects can be modeled with coarse meshes while the critical interconnect is modeled with fine meshes, which has been implemented in the "*nonlinear global model*" technique. Alternatively, the global model calculation can be simplified by modeling the package and PCB as super-elements. For both techniques, it is time-consuming to generate fine meshes for the critical interconnects to match the coarse meshes of the other components. Furthermore, although the non-critical interconnects and other components are modeled with coarse meshes, the amount of resultant elements for fine-pitch packages is still too large for practical analysis.

In finite element analysis, the node displacement is not sensitive to the mesh density while the stress/strain calculation is highly dependent on the mesh size. Therefore, two-stage modeling techniques have been developed to simultaneously

address the computational resource limitations and calculation accuracy. First, a global model with coarse meshes is subjected to temperature cycling to extract the node displacements of the critical interconnect. At this stage, either linear or nonlinear material model has been applied for package, PCB and interconnects, depending on the model and accuracy requirement. In the second step, a sub-model of the critical interconnect is constructed with fine meshes and the displacement results from the global modeling are applied as boundary conditions. A non-linear material model is always applied to solder joints for accurate stress/strain analysis.

5.3.2 Modeling Methodology

In this section, the board-level thermomechanical reliability of the fine-pitch MCC interconnects is analyzed by nonlinear global model with a nonlinear sub-model. Note that for a 40μm-pitch fully area array of MCC interconnects that were fabricated on a 10×10mm^2 chip, the total number of interconnects is over 60,000. For such a package, a typical nonlinear global modeling still results in impractical model size even though the only a quarter of the package model is simulated because of symmetry. Hence, a so-called micro-macro numerical technique [90-94] is employed to reduce the size of board-level MCC interconnect modeling. The validity of this method in terms of fatigue prediction of large BGA type packages has been verified by comparison with full-scaled 3-D modeling [92-95] or experimental observation [96]. Taking J. S. Corbin's work on second-level Solder Ball Connect (SBC) structures [96] as an example, the simulation procedure is briefly described as below:

a) At micro level, a 3D model was developed for a single solder joint to study its deformation behavior. Two deformation modes were investigated, including pure shear mode and pure axial compression mode. This micro-model

simulation produced the reaction force results corresponding to the respective displacement modes;

b) An equivalent beam model was constructed, which ideally possesses the same displacement-reaction force curve as the above 3D interconnect model;

c) In macro-level modeling, both the package substrate and the motherboard were modeled with shell elements, which, together with the equivalent beam model obtained earlier, produced deformation results (i.e. net shear and axial displacement values) of any solder joint through temperature cycling;

d) The displacement results obtained in the previous step were input back to the 3D micro-model as boundary conditions, and the plastic strain range of a solder joint within one temperature cycle was obtained for estimation of the thermal fatigue life;

The simulation procedure for MCC interconnects principally follows Corbin's procedure except that:

a) In Corbin's study, the interconnect structure was a pure solder ball that can be well represented by a double truncated model (DTM). In this paper, because of the wetting of solder on copper column surface, the software tool Surface Evolver (SE) has been used to predict the solder joint profile. The solder geometry calculated in SE was imported into ANSYS for thermomechanical analysis. Details of this method were described in Section 5.1.2;

b) In Corbin's study, the micro-model does not only consist of the SBC structure, but also extend to the mid-plane of the package substrate and motherboard. In this work, however, the micro-model was only composed of the interconnect structure. Compensation is correspondingly made in macro-modeling by offsetting the midplanes of chip and package substrate, respectively;

c) In Corbin's study, axial compression deformation was used to obtain the equivalent beam. In this study, axial tension is used instead to avoid beam buckling;

d) In Corbin's study, while the results obtained in the macro-modeling step were input back to the 3D micro-model as boundary conditions, the local CTE mismatch within the micro-model was also taken into account. In this work, the local CTE mismatch effects were neglected;

5.3.3 Case Studies

The details of the solder joint modeling within Surface Evolver 2.23 and macro-micro-modeling within ANSYS 6.1 for this board-level thermomechanical simulation are revealed in the following case study.

Table 5-5 Material properties of copper and solder for micro-modeling

Material Properties	Copper	Eutectic Sn/Pb	
		-40°C	125°C
Elastic modulus, GPa	127.4	40.554	15.474
Poisson's ratio	0.36	0.4	
Yield strength, MPa	262.4	38	8.7
Stress at ε_p=0.002, MPa	273	46.4	9.2
Stress at ε_p=0.005, MPa	280	50.2	9.5
Stress at ε_p=0.01, MPa	288.2	53	9.8
Stress at ε_p=0.02, MPa	300.1	56.5	10.1
Stress at ε_p=0.05, MPa	324.5	60.3	10.4
Stress at ε_p=0.1, MPa	352.8	63.4	10.7
Stress at ε_p=0.2, MPa	394.1	66.8	10.9
Stress at ε_p=0.5, MPa	478.7	71.9	11.1

5.3.3.1 Solder Joint Shape Modeling Using SE

The interconnect geometry used for SE simulation is same as the 4th run in Table 5-7. Fig. 5-17 illustrates the solder model developed from SE simulations, in which the used material properties include solder wetting angle on Cu of 20°, solder density 9.28×10^{-12}g/μm^3, and solder surface tension 4.63×10^{-7} N/μm. It could be seen from Fig. 5-17 that the solder wicks up along the copper columns to form the wedge-shaped fillet around the column surface.

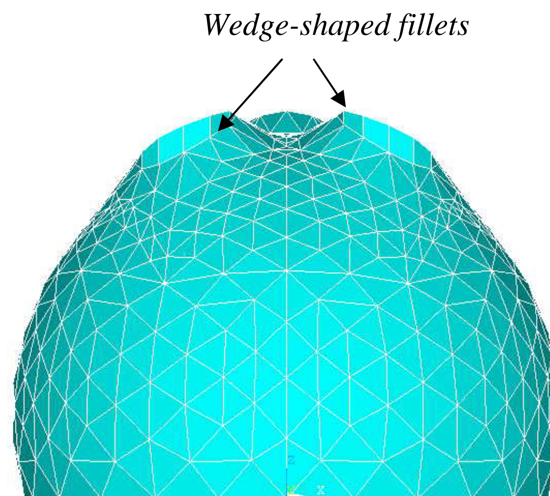


Fig. 5-17 Solder shape developed from SE modeling

5.3.3.2 Micro Deformation Analysis and Equivalent Beam Extraction

A 3-D micro-model is constructed by addition of the copper columns into the above solder model as shown in Fig. 5-17. Fig. 5-18 shows the displacement-reaction force results for pure shear and tension deformation modes at the two extreme temperatures of temperature cycling: -40°C and 125°C. Table 5-5 show the material properties used for micro-modeling analysis. The equivalent beam geometry and material properties are defined by the following procedure.

According to the elastic beam theory, for a beam with one end fixed and the other end moving laterally only, the shear reaction shear force F_y can be related to the shear displacement U_y by:

$$F_y = \frac{12EIU_y}{L^3} = \frac{3EU_y\pi r^4}{L^3} \qquad (5\text{-}7)$$

where I is the second area moment of inertia of the beam with a cross section radius of r, L is the beam length. On the other hand, for a beam in purely axial deformation mode, the reaction axial force F_z can be related to the axial displacement U_z as:

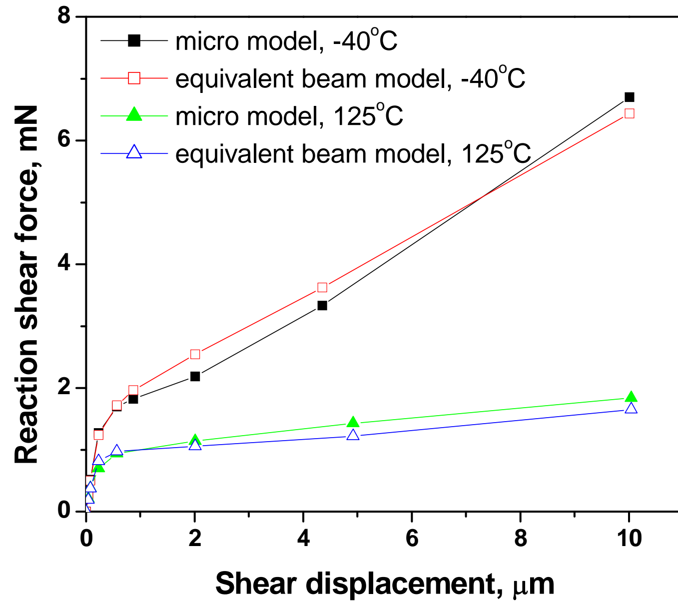
$$U_z = \frac{F_z L}{\pi r^2 E} \qquad (5\text{-}8)$$

By combining equations (5-7) and (5-8), the following equation can be obtained:

$$U_z \times F_y = \frac{3F_z U_y r^2}{L^2} \qquad (5\text{-}9)$$

The equivalent beam length L is always assumed to be the same as the whole interconnect standoff height, which is 42.1μm in this case. By inputting the elastic displacement and reaction force data of the micro deformation analysis as shown in Fig. 5-18 and the L value into the equation (5-9), the cross-section radius of the equivalent beam is obtained, and finally the elastic modulus of the equivalent beam is calculated through either equation (5-7) or (5-8). The Poisson's ratio of equivalent beam is assumed as 0.4. The plastic properties of the equivalent beam were optimized by iteratively adjusting the hardening coefficient and hardening exponent so that the maximum approximation in terms of the deformation behavior is achieved between the 3D interconnect structure and the equivalent beam. Fig. 5-18 showed that the equivalent beam well matched the 3-D interconnect model in the shear deformation, but obvious discrepancy exists in the axial deformation. Because of the significant difference of material properties between Cu and solder that constitute the composite

interconnect structure, it is difficult to obtain a perfect equivalent beam that represents the composite structure simultaneously well in both deformation modes. Since the shear displacement is usually one order higher than the axial displacement, priority is given to the match of shear deformation.



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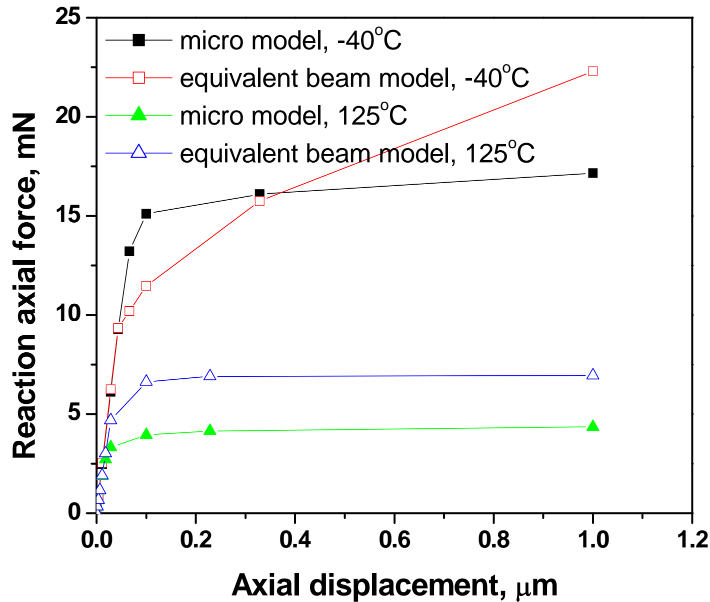


(b)

Fig. 5-18 Force-displacement correlation for MCC & the corresponding equivalent beam (a) shear deformation; (b) axial deformation

5.3.3.3 Macro modeling

The material properties used for macro modeling is shown in Table 5-6. The MCC interconnects are arranged in a fully populated manner with a pitch of 40μm only. The package size is 10×10mm^2, but only a quarter of the package (i.e., 5×5mm^2) as shown in Fig. 5-19(a) was modeled for simulation because of symmetry. The distance

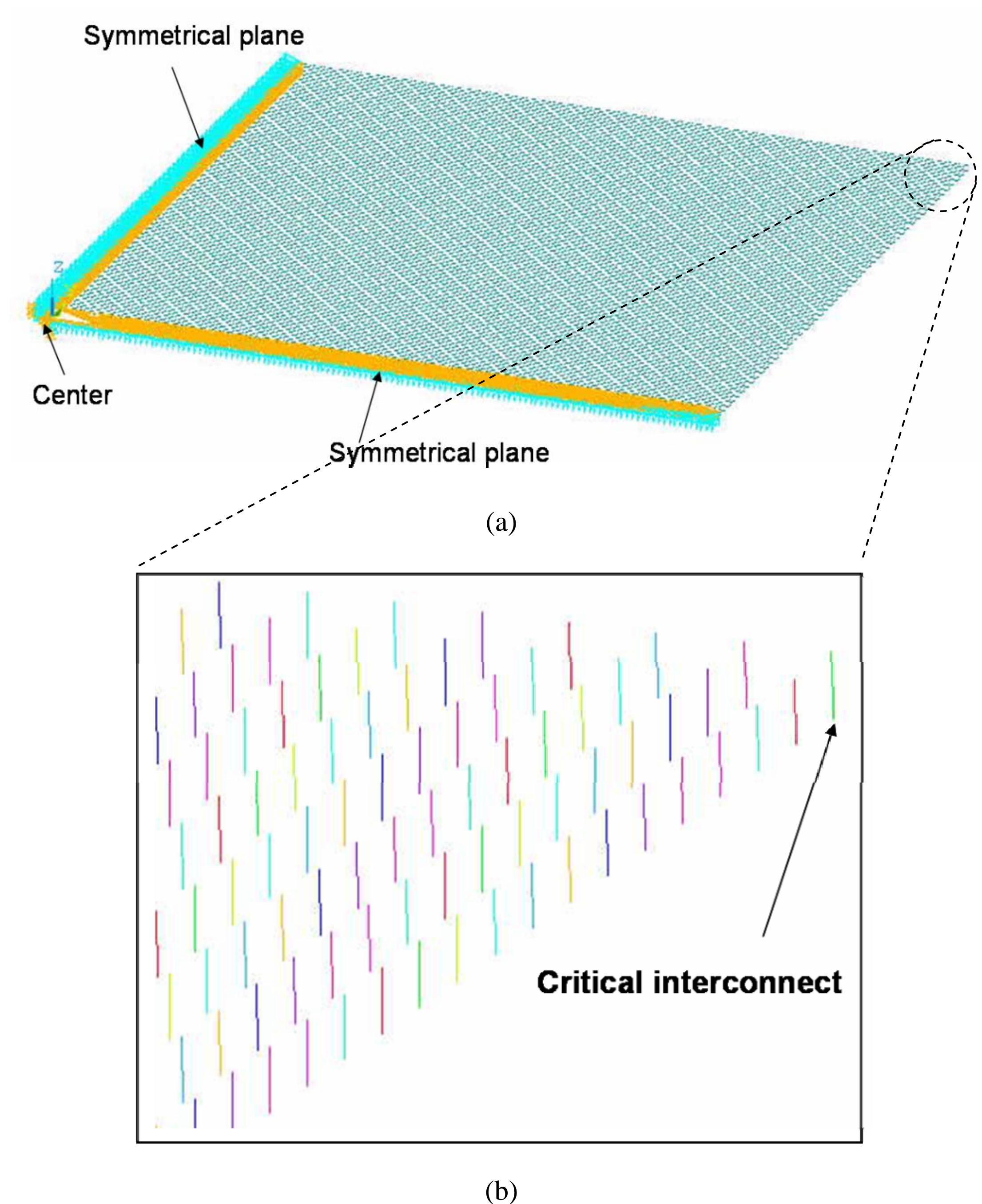


Fig. 5-19 Model for Macro-level analysis

Table 5-6 Material properties of Si and FR-4 substrates for macro modeling

	Si	FR-4
Elastic modulus, GPa	131	22
Poisson's ratio	0.23	0.28
CTE, ppm/K	2.8	10

from the farthest interconnect (i.e., the *critical interconnect*) to the neutral point of the package is ~6335μm. The Si chip and the FR-4 PCB substrate thickness are 640μm and 800μm, respectively. As shown in Fig. 5-19(b), each MCC interconnect in macro modeling is represented by one quadratic beam element with geometry and nonlinear material properties extracted in the previous micro-modeling. Correspondingly, both chip and package substrate are modelled with shell elements. In this way, the whole model is composed of ~15,000 beam elements and ~30,000 shell elements that can be calculated in a typical workstation. The temperature cycling range is -40~125°C with an intial temperature of 125°C. Five termperature cycles are simulated, outputing the net displacement results of the critical interconnect as shown in Fig. 5-20. It can be observed that the shear displacement is much higher than the axial one, which justfies the priority on shear deformation during the above equivalent beam extraction.

5.3.3.4 Micro-modeling for Strain Analysis

The cyclic displacement results of the critical interconnect obtained in the previous step are applied to the 3D micro-model of a single MCC interconnect as boundary conditions to calculate the plastic strain range in the solder joint. Fig. 5-21 shows the finite element model where the solder meshes around the boundary between copper column and solder surface were refined to get accurate strain results. The element with maximum equivalent plastic strain is identified. The equivalent

plastic strain of this particular solder element and all the other immediate neighboring solder elements are averaged to obtain a more practical result. The averaged equivalent plastic strain evolution with pseudo time is shown in Fig. 5-22. The equivalent plastic strain range in the last (i.e. 5th) cycle was recorded as the strain damage indicator for fatigue life prediction.

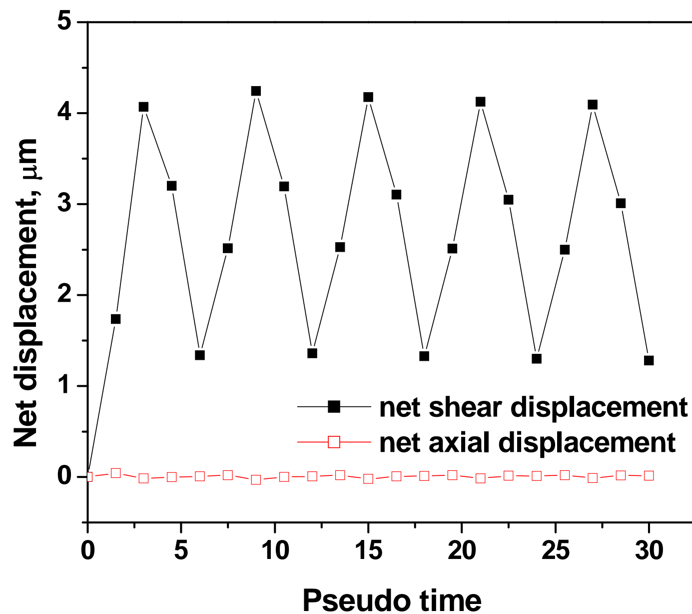


Fig. 5-20 Net deformation result of the critical interconnect with a distance of ~6335μm from the neutral point of package

5.3.4 Analyzing dependence of board-level reliability on geometry using DoE

By combining the macro micro modeling technique as described in the above section and the Design of Experiment (DoE) technique, four geometric parameters of MCC interconnects as listed in Table 5-7 are studied in terms of their influence on the thermal fatigue damage of the solder joints. The Taguchi's thee-level orthogonal array [84], $L_9(3^4)$, is utilized to implement the parametric study. All the other geometric and material properties are the same as the previous section. Following the sequence described in Section 5.3.3, the net displacement and plastic shear strain range on the critical interconnects in different scenarios as shown in Table 5-7 are listed in Table

5-8. The fatigue life cycle, which is projected according to Solomon's equation [97] $\Delta\gamma_P N_f^{0.51} = 1.14$, is also included in the table.

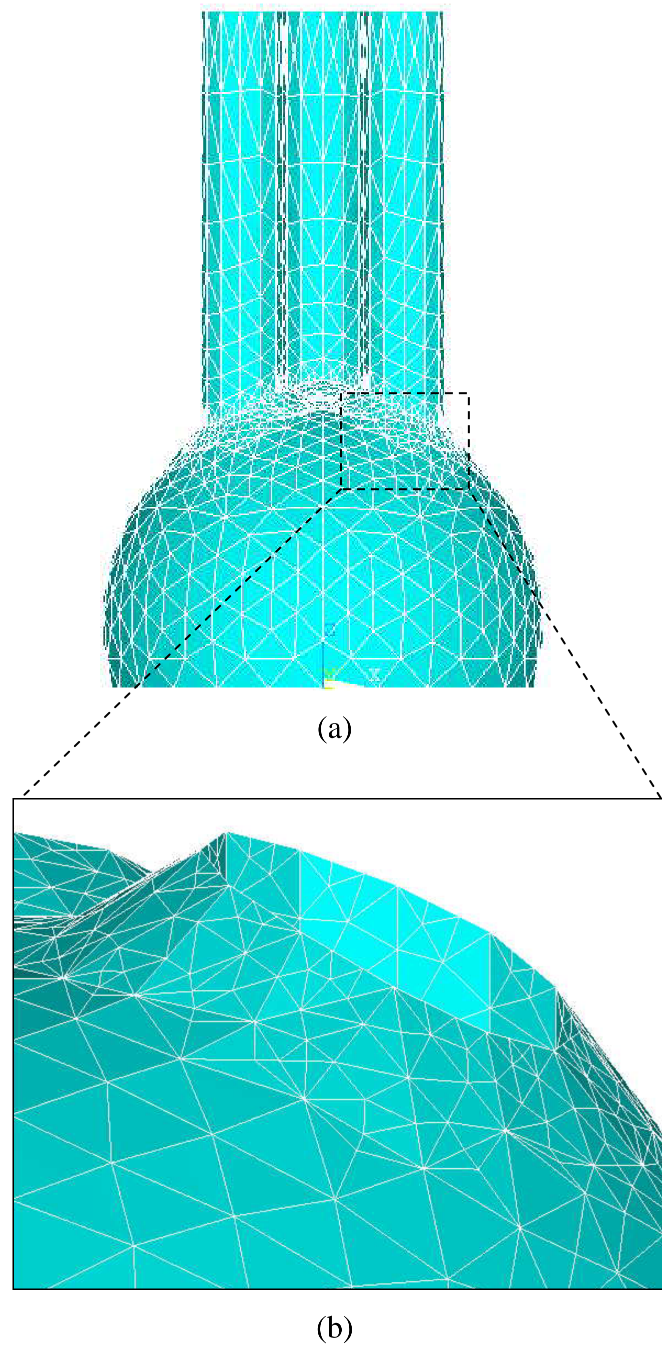


Fig. 5-21 3D micro-model for strain analysis (a) full model; (b) mesh refinement around the column periphery

The solder shape evolution is affected by the solder volume, the substrate pad size and the copper column radius. Fig. 5-23 shows the solder models for runs 1 and 7, which results in distinct shapes even though the volume is the same. Compared to the 1st run, the solder model of the 7th run has a larger bottom area because of the larger pad on package substrate, and the solder also wicks up a longer path since the copper columns also provide a larger wetting surface.

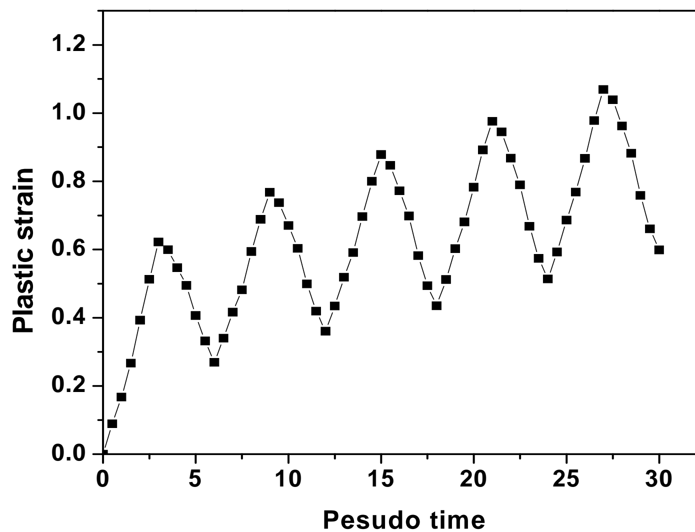


Fig. 5-22 Equivalent plastic strain evolution with pseudo time

Table 5-7 MCC interconnect geometry for DoE simulations

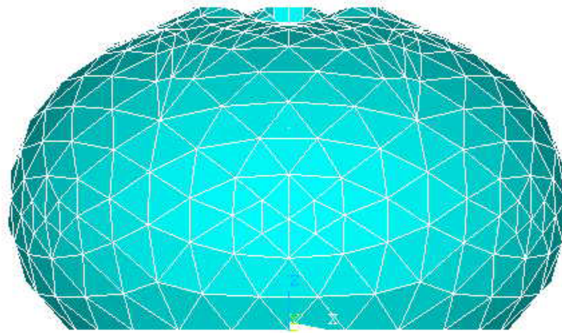
Run #	Substrate pad radius, μm	Solder volume, μm^3	Copper column radius, μm	Copper column height, μm
1	10	7500	1.5	15
2	10	10000	2.5	22.5
3	10	12500	3.5	30
4	13	7500	2.5	30
5	13	10000	3.5	15
6	13	12500	1.5	22.5
7	16	7500	3.5	22.5
8	16	10000	1.5	30
9	16	12500	2.5	15

Table 5-8 Calculated displacement, strain and fatigue life of critical interconnects

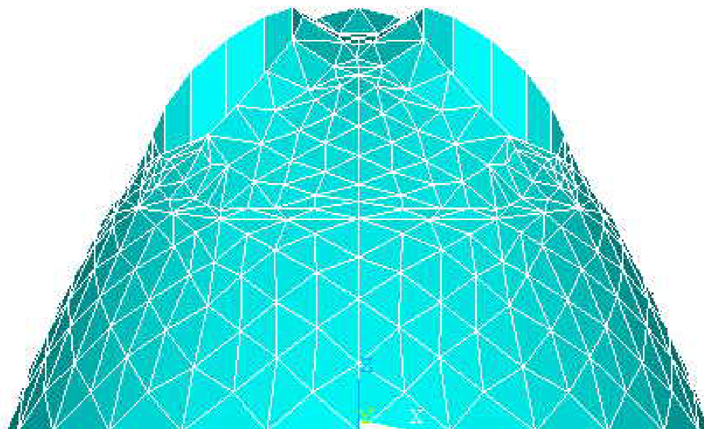
Run #	Net axial displacement, μm	Net shear displacement, μm	Plastic shear strain range	Fatigue life cycle *
1	-0.105	4.547	0.84	2
2	0.108	2.988	0.54	4
3	0.132	2.339	0.30	13
4	-0.011	4.095	0.56	4
5	0.176	1.006	0.12	83
6	-0.182	5.274	0.92	2
7	0.136	2.364	0.22	26
8	-0.321	6.277	1.51	N.A.
9	0.184	1.934	0.52	5

* Fatigue life cycle is calculated according to Solomon's equation $\Delta\gamma_p N_f^{0.51} = 1.14$ [97]

For the critical interconnect farthest from the neutral point, Fig. 5-24 shows the net shear displacement results obtained from the macro analysis, and Fig. 5-25 shows the plastic strain range results from the 3D micro strain analysis. In the case of a larger solder volume or a smaller substrate pad, the extra solder must "*wick*" up along the copper column and hence practically strengthen the interconnect. However, because of the large difference in elastic modulus between copper and solder, this strengthening effect is quite small in comparison with the influence of column radius and height. The column radius shows the most remarkable effect, which is consistent with equation (5-7).



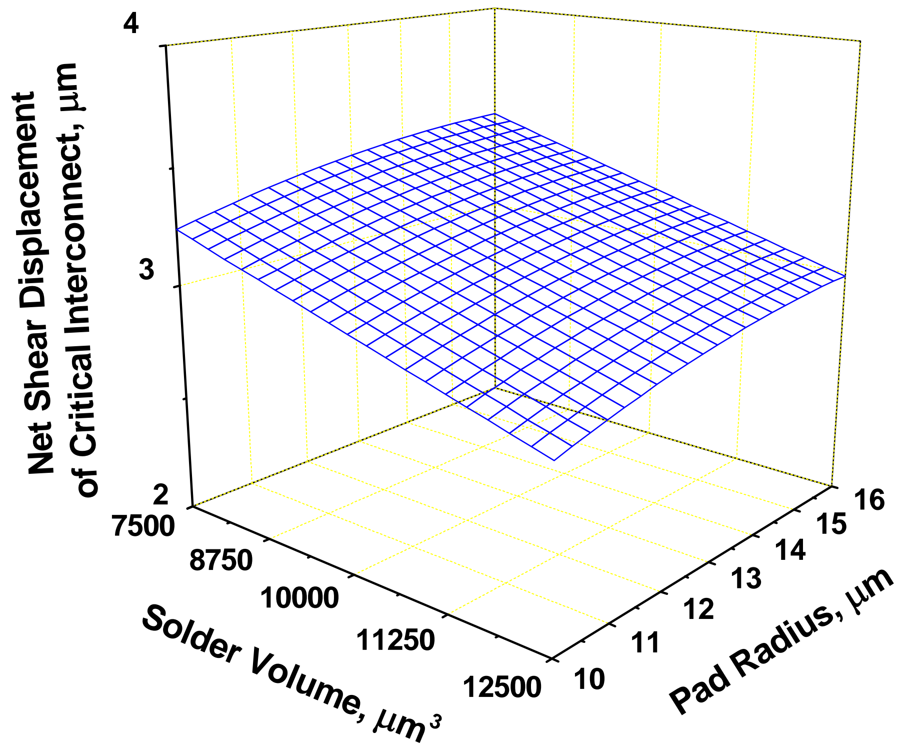
(a)



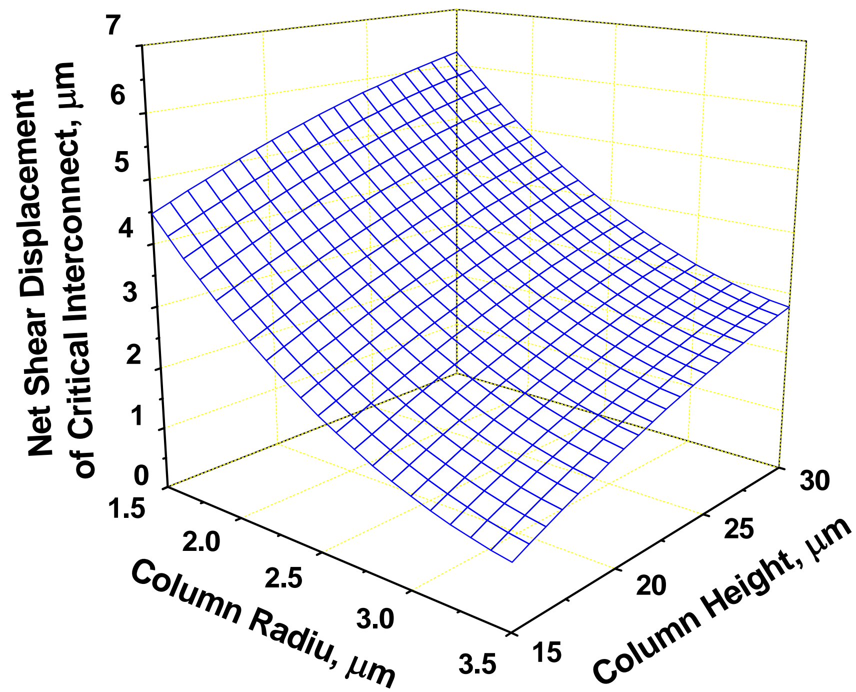
(b)

Fig. 5-23 Solder shape predicted for (a) run 1 and (b) run 7

As shown in Fig. 25(a), a stronger effect on the plastic strain range than on net displacement can be observed for the solder volume and substrate pad dimension. Fig. 25(b) shows that a higher plastic strain range is induced for MCC interconnects with higher aspect-of-ratio columns. The resemblance of Fig. 24(b) and Fig. 25(b) suggests that this increased strain damage mainly originates from the increased displacement.

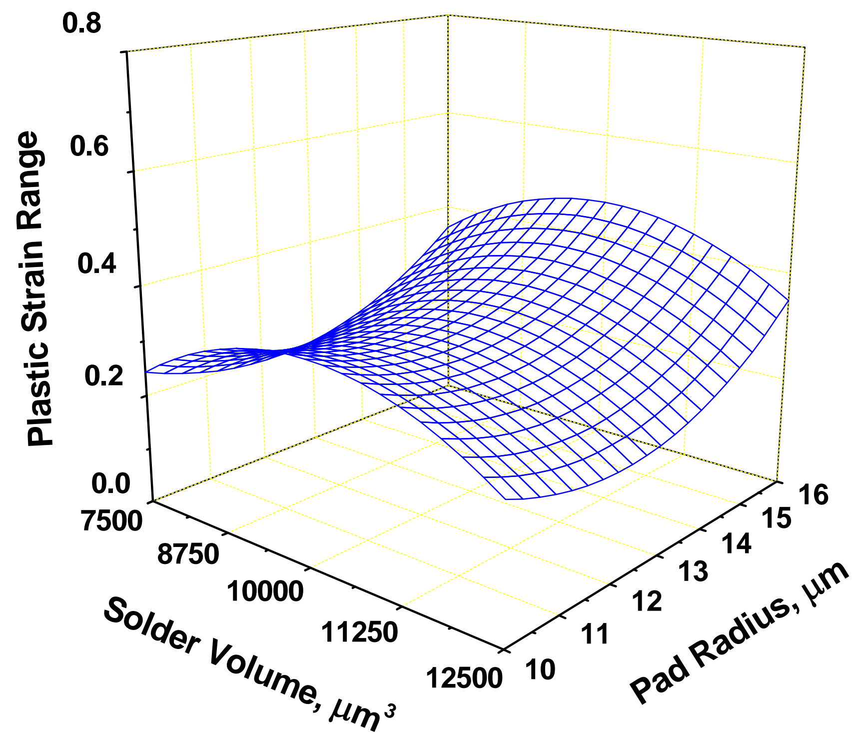


(a)

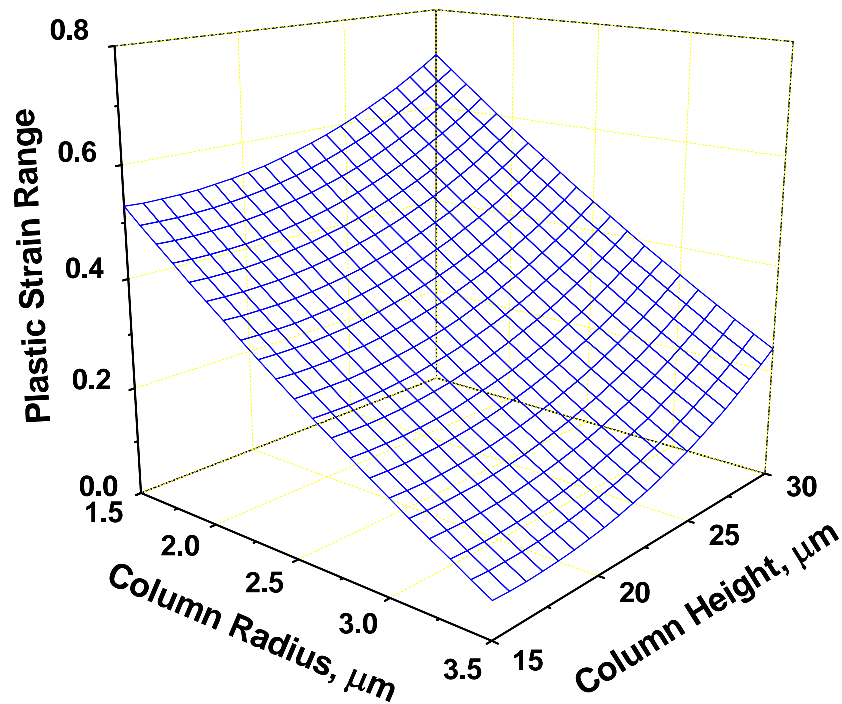


(b)

Fig. 5-24 Net shear displacement of the critical interconnect as a function of (a) solder volume & pad radius (r=2.5μm, h=22.5μm); (b) column radius & height ($V=10^4 \mu m^3$, R=13μm)



(a)



(b)

Fig. 5-25 Plastic strain range of the critical interconnect as a function of (a) solder volume & pad radius (r=2.5μm, h=22.5μm); (b) column radius & height ($V=10^4\mu m^3$, R=13μm)

It has been observed in a previous study on a similar composite interconnect structure that the solder reliability may be impaired when the aspect-of-ratio of the copper column is nearly doubled [98]. This degradation was attributed to the shift of deformation mode, i.e., when the column becomes shorter, shear becomes the dominant deformation mode in place of bending, and the most stressed site within the solder joint shifted toward the thicker region and hence the strain energy can be absorbed by a larger solder volume. In our study, however, thermomechanical failure seems to always occur at the solder fillets around the boundary between solder surface and copper columns. Instead, the increase of fatigue damage seems to be consistent with the increase of shear displacement introduced by the change in geometry of the interconnects. In short, the previous simulation demonstrates that, for fine-pitch compliant interconnects such as MCC, the flexibility of the non-solder structure has two opposite effects on the solder joint reliability: 1) it induces higher displacement loading and hence adverse effects on the solder joint reliability; 2) it is able to absorb more strain energy so as to enhance the solder joint reliability. The net effect of these two competing mechanisms determines whether the compliance enhancement will improve or impair the solder joint reliability. Hence, one way to enhance interconnect reliability is to improve the flexibility of the non-solder structure while the shear deformation on the corresponding interconnect is maintained. To achieve this, the critical interconnect or a small group of interconnects nearby the critical one can be replaced by different MCC design with higher-aspect-ratio columns and thus higher compliances. Because these interconnects may only take a small fraction of the whole interconnect array, this change in their geometry will not induce perceivable variation on the shear deformation applied on themselves. Therefore, the thermomechanical reliability of these interconnect can be improved as a result of higher compliances as

shown in Section 5.2.4. The same concept has been practised in another compliant interconnect scheme Sea of Lead [99]. The disadvantage of this concept is that different interconnect designs have to be introduced into the same chip, and the percentage of each design needs to be optimized. On the other hand, it is still possible to achieve higher thermomechanical reliability only by improving compliances of the non-solder structure, which will be shown in the following section.

5.3.5 Correlation between compliance, deformation and thermomechanical reliability

It was demonstrated in the last section that, within the same package scenario and temperature cycling range, a higher aspect-of-ratio of copper columns actually leads to higher strain damage in the solder, which can be explained by a higher shear displacement exerted on the interconnect. To clearly show the complicated effects of non-solder structure flexibility on solder joint reliability, and also the possibility of achieving higher solder joint reliability without increasing complexity of interconnect design, a board-level reliability analysis of interconnects with different compliances is conducted as follows.

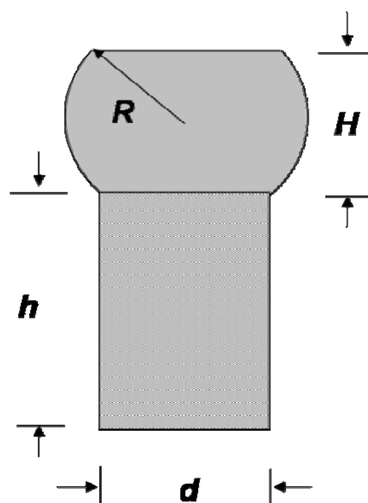


Fig. 5-26 Schematic of single copper column interconnect

A 10×10mm^2 package model consisting of 800μm thick FR-4 PCB, 640μm thick Si chip and fully populated interconnect array with pitch of 100μm is constructed for temperature cycling (-40~125°C) simulation. To simplify the simulation process, the interconnect consists of only one copper column and solder joint, the latter of which is represented by a double truncated model with a radius 5μm and height 8μm. The copper column has a fixed diameter of 3μm, but different heights are used to simulate the effect of column compliances. The compliance, net shear displacement, and also the equivalent plastic strain range of the critical interconnect (which is at a distance of ~6859μm away from the package center) is calculated using the same procedure as described in Section 5.3.3.

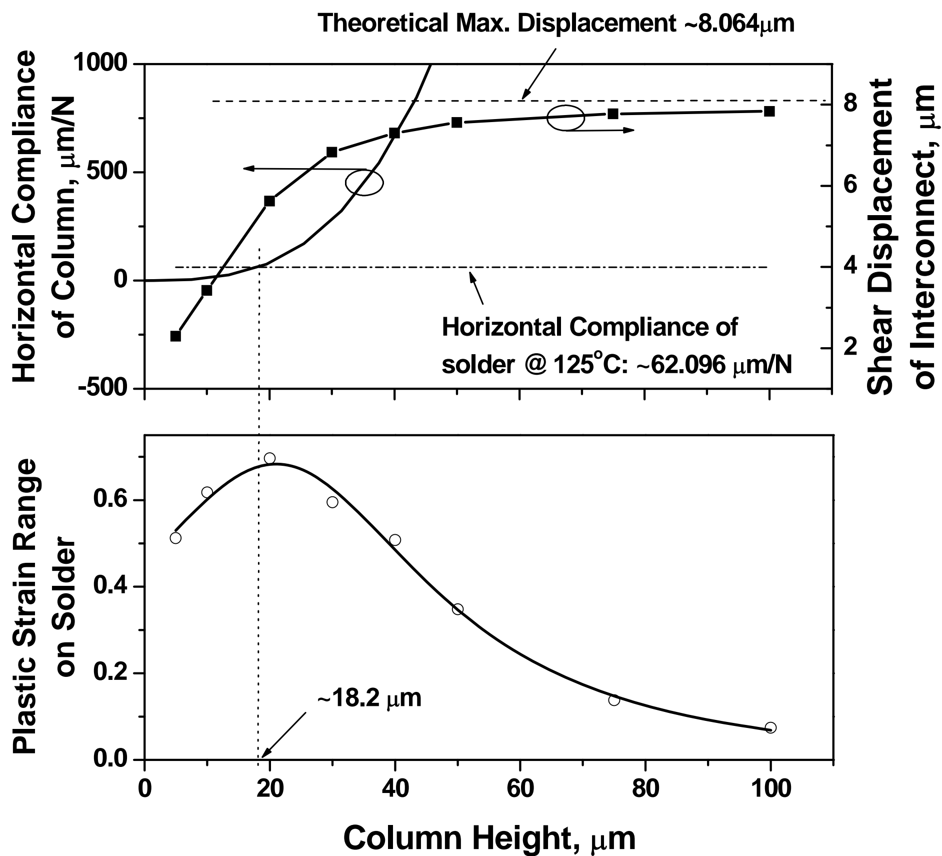


Fig. 5-27 Variation of column compliance, net shear displacement and plastic strain range of critical interconnect as function of column height

From the upper part of Fig. 5-27, it could be seen that the horizontal compliance of copper column increases with the column height by a power law. The solder ball compliance is ~62.096μm/N at 125°C. The copper column compliance exceeds the solder compliance when the column height increase beyond ~18.2μm. On the other hand, the net shear displacement of the critical interconnect increases with the column height and finally approximates the theoretical maximum displacement, which is determined by the CTE mismatch between Si chip and package substrate, temperature cycling range and the distance from the critical interconnect to the neutral point of the package. The bottom part of Fig. 5-27 shows that the enhancement of column compliance is initially unfavorable but then beneficial to solder reliability. The cross-over point occurs at a critical height of ~20μm, which is quite close to the point where the compliance of the copper column is about the same as that of the solder. In short, Fig. 5-27 suggests that whether an increase of column compliance improves the solder joint reliability or not will depend on whether the copper column height is less than or greater than 20μm. This dependance can be interpreted as follows. An increase of the column height (compliance) always leads to reduction of the "*restraining*" effect of the interconnections, i.e. copper column and solder joint, between the neutral point and the outermost interconnect on the relative movement of chip and package substrate, and thus a higher shear displacement of the outermost critical interconnect. Whether this higher shear displacement leads to an increase or decrease in the strain at the critical solder joint of the outermost interconnection depends on the magnitude of the compliance of the interconnection. Thus, when the column compliance of the interconnection, is very low in the region corresponding to a copper column height of less than 20μm (Fig. 5-27), the restraining effect of the interconnections between the neutral point and the outermost interconnect is so effective that the strain experienced

by the critical solder joint of the outermost interconnection is very low. On increasing the compliance of the interconnections, the restraining effect of the interconnections is reduced, causing the relative shear displacement at the outermost interconnection to increase. As the column compliance is small, this increase in relative shear displacement leads to an increased strain experienced by the critical solder joint (Fig. 5-27), resulting in decreased reliability. However, in the region corresponding to a copper column height greater than 20μm (Fig. 5-27), due to the high column compliance, this increase in relative shear displacement leads to a decrease in strain experienced by the critical solder joint, resulting in increased reliability.

The above analysis provides importance implications and guidance to design of compliant interconnect across the die. Given a composite interconnect in which the compliance of non-solder component is higher than that of the solder joint, the reliability of solder joint can be improved by uniformly increasing the compliance of the non-solder component across the whole die. On the other hand, if the compliance of non-solder component is lower than that of the solder joint, and the process does not allow the compliance of non-solder part to go beyond the critical point (e.g., ~62.096μm/N in Fig. 5-27), uniform increase of the compliance of non-solder component will actually lead to higher thermomechanical damage to the solder joints. In this case, from the reliability point of view, the central region of the die is preferentially occupied with low-compliance interconnect, while the high-compliance interconnects can be distributed around the corner region of the die. A similar method has been implemented in the Sea of Lead technology [24] where the interconnect compliance is designed according to its location on the die. It is noticed that an integrative solution has been recently proposed to achieve optimum mechanical and electrical performance [100] in terms of the whole interconnect array. In this method,

simple copper columns are distributed at the center of die as ground-power interconnects to carry higher current and also as a restrainer for the shear deformation on the high-compliance interconnects, which is located close to the corner of the die. Low-compliance (which is still higher than that of the copper columns at die center) interconnects are distributed in the middle. Simulation results show that this heterogeneous design of interconnect array with varying compliance produces superior reliability than identical high-compliance interconnect distribution.

Chapter 6 High-Frequency Electrical Simulation of Compliant Interconnects

The continuous increase of system clock speed and improvement of on-chip interconnection technology have imposed stringent challenges on packaging technologies. In particular, as a bridge between the on-chip global interconnections and the package, the chip-to-package interconnects are expected to transmit the signals with minimum loss of fidelity. Conventionally, bonding wires [101] have been the dominant approach to electrically connect chip to package. However, a number of studies concerning the electrical performance of bonding wires in microstrip [102] and coplanar [103,104] configurations demonstrate that the associated power loss drastically increases with excitation frequency. The reason behind those observations is that, with frequency increasing, the length of wires becomes comparable to the signal wavelength, and hence the wires exhibit transmission line behavior. Therefore, wire bonding as a chip-to-package interconnection technology is limited to applications of up to 15~20 GHz. In comparison, flip-chip technology using solder interconnects that was initially developed by IBM [105,106] significantly extends the working frequency because the interconnect length is remarkably reduced.

In *Chapter 4*, the high-frequency functionality of Multi-Copper-Column (MCC) interconnects has been verified using a customized measurement set-up. However, the electrical performance associated with the interconnects themselves was not verified because of the huge noise introduced by the components used in the measurement set-up. Considering the miniaturized size and pitch of MCC interconnects, it is currently impractical to experimentally isolate and extract their high-frequency electrical

performance. In the following, the electrical characteristics of MCC and Planar Microspring interconnect will be extracted using High Frequency Structure Simulator (HFSS) 8.5. The effects of various package factors including interconnect pitch, chip and substrate materials will be presented. Finally, an equivalent lumped circuit model is successfully constructed to represent the MCC interconnects up to ~30GHz.

6.1 High-frequency Simulation Model

In the previous electrical modeling of MCC interconnects within the low frequency range (≤100MHz), the signal input and output were assumed exactly at the two ends of the interconnect as shown in Fig. 2.4. For high-frequency (>GHz) simulation, however, because of the non-uniform cross-section of the interconnect, this arrangement results in transmission and reflection of multiple higher-order electromagnetic field modes along the interconnect. Simulation of all the modes may take too much computation resource, while missing of any mode may result in erroneous results. Hence, a uniform transmission line with enough length (>10λ, where λ is signal wavelength of interest [107] is designed on both chip and package substrate, so that the higher modes die off before reaching the MCC interconnects. In this way, only the dominant propagation mode is simulated.

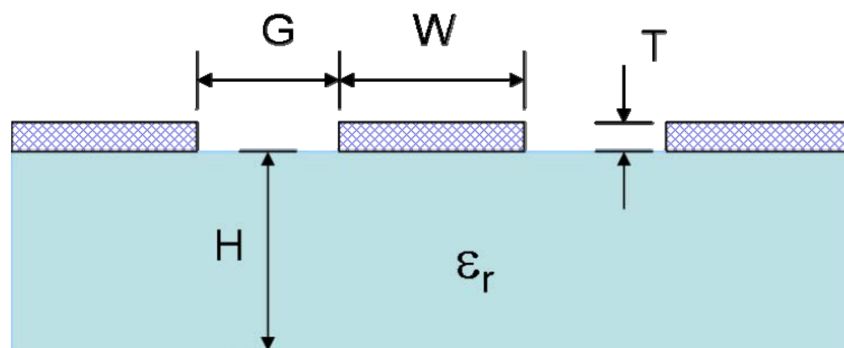
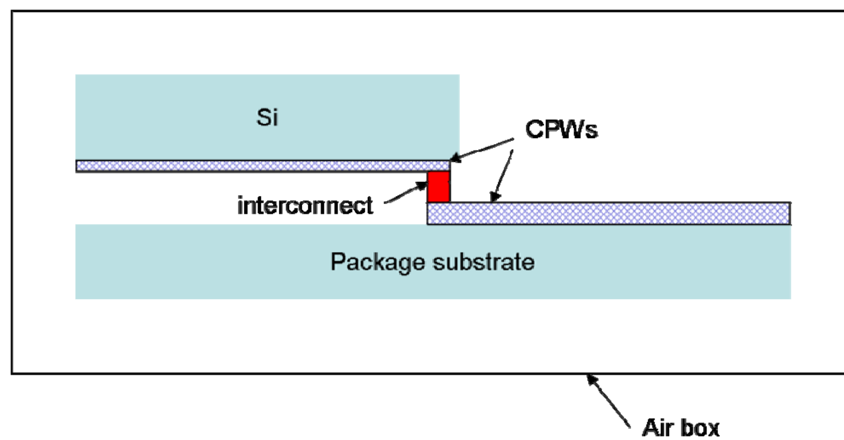
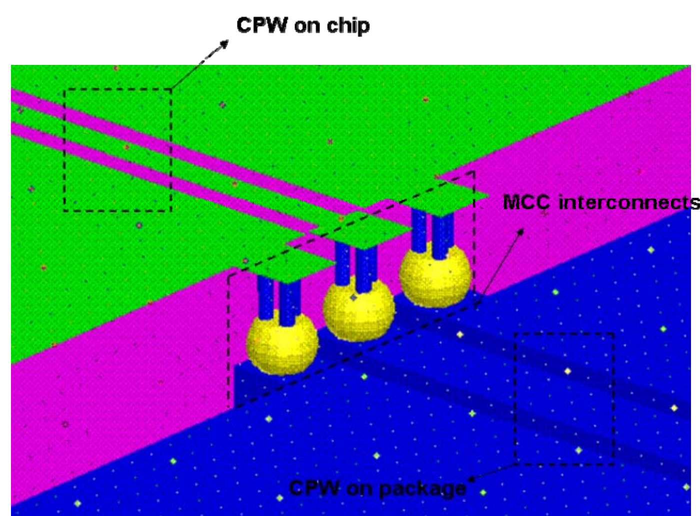


Fig. 6-1 Cross section view of Co-Planar Waveguide (CPW) transmission line

There are different transmission lines that can be used to extract the electrical performance of flip-chip interconnects, including microstrip lines, striplines and co-planar waveguide (CPW). It was reported [108] that, owing to the orientation of the electric field in the CPW, the flip chip transition between two CPW's shows the best electrical performance up to 40GHz and possibly 100GHz. Furthermore, the process to fabricate CPW is practically much easier since it is fabricated on only one side of the chip or package substrate. Therefore, the CPW transmission line is included in the high-frequency simulation model as described below.



(a)



(b)

Fig. 6-2 HFSS simulation model of compliant interconnects (a) side view; (b) close-up view of MCC interconnects in a CPW scenario

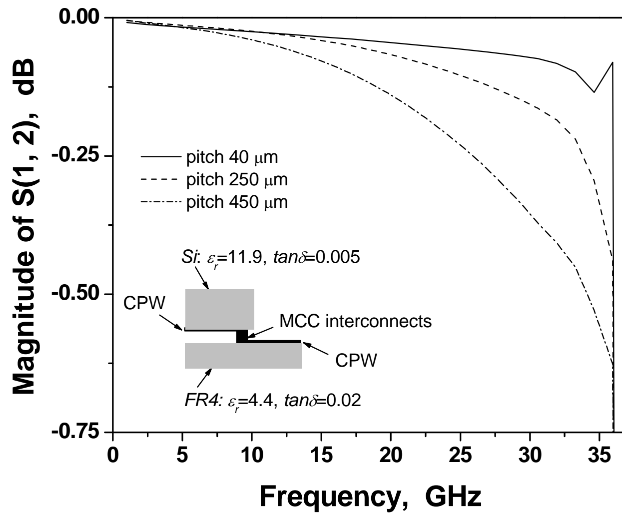
Fig. 6-1 shows the schematic of a CPW transmission line sitting on a substrate with a thickness of *H* and a dielectric constant of ε_r. The CPW is made of Cu with an electrical conductivity of 5.88×10^7 S/m. The dimensional parameters of CPW include the thickness *T*, the signal plane width *W*, and the spacing *G* between the signal plane and the ground plane. Fig. 6-2(a) shows a schematic side view of the HFSS simulation model including chip and package substrate, interconnects and CPW transmission lines. Radiation boundary condition is applied to the air box, of which the dimension in the direction normal to the chip or package substrate surfaces is 20 times that of the chip-interconnect-package model. The *S*-parameter within the frequency range of 1~40GHz is obtained first, and then the contribution from the transmission line is deducted through de-embedding procedure so that the insertion loss (S_{12}) associated with the compliant interconnect only is extracted.

6.2 Effects of Package Scenario on Power Loss of Interconnects

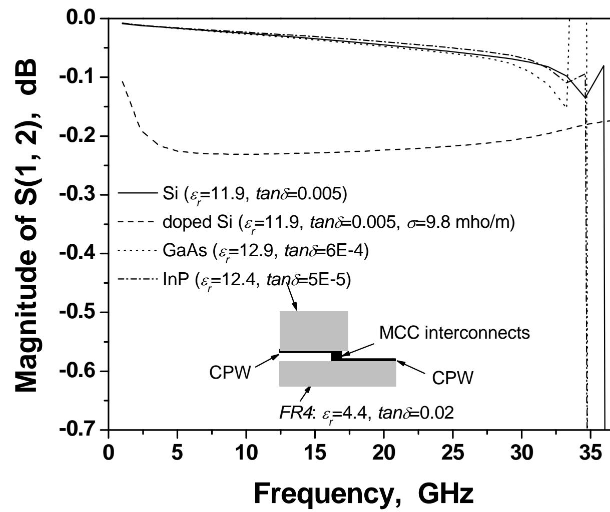
6.2.1 Multi-Copper-Column (MCC) Interconnects

TCC interconnect with column height, spacing and radius of 20μm, 5μm and 2.5μm is used in this study. The double-truncated spherical solder joint has a height of 18μm and a radius of 12.5μm. The Al and Cu pad dimensions are 25×25×0.5μm^3 and 25×25×17.5μm^3 on chip and package substrate, respectively.

Fig. 6-3 shows the transmission characteristics of TCC interconnects within scenarios with various pitch, chip and package substrates. It is observed from Fig. 6-3(a) that, within a Si-FR4 scenario, the power loss decreases with the interconnect pitch. At a pitch of 40μm, the power loss is less than 0.1dB till the frequency of 33GHz. Irrespective of the interconnect pitch, a sharp increase of loss is observed always at a frequency of ~36GHz because of self resonance. The resonance frequency



(a)



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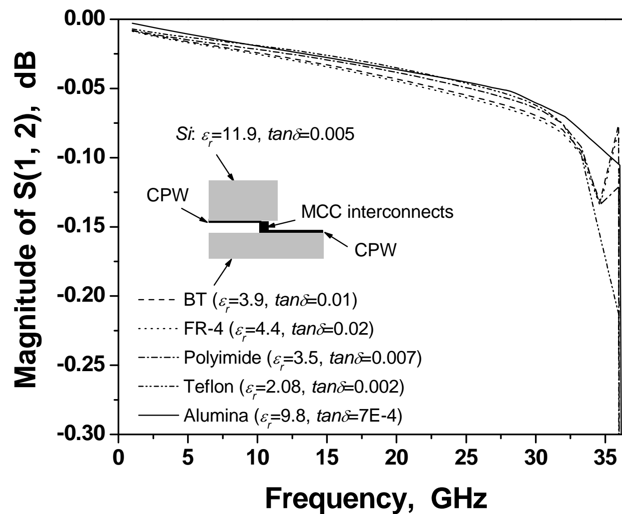


(c)

Fig. 6-3 Insertion loss *S(1,2)* of MCC interconnect depending on (a) interconnect pitch; (b) chip substrate; and (c) package substrate

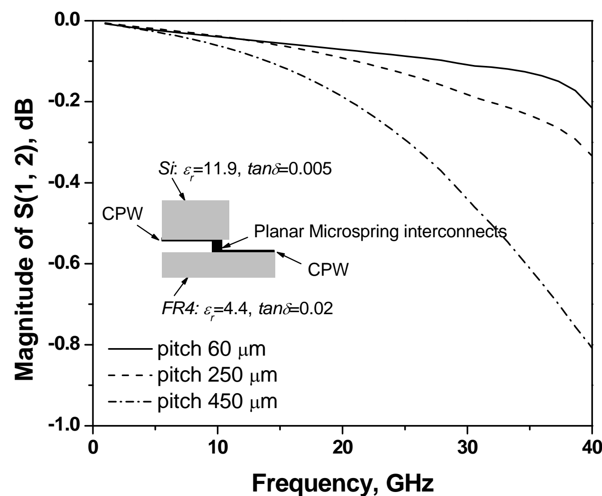
shifts toward the lower end with increase of dielectric constant of the chip substrate, as shown in Fig. 6-3(b). A Si substrate with a conductivity of 9.8 S/m, which corresponds to a typical doping concentration of $1\times10^{15}cm^{-3}$ in *p*-type Si, is also included in Fig. 6-3(b) for reference. The power loss within a conductive Si scenario is much higher as expected, but resonance is not observed within the frequency range of simulation. The effects of common package substrates on the insertion loss of MCC interconnect are shown in Fig. 6-3(c), with a pitch of 40μm and Si chip substrate applied. A minimum loss is obtained with Alumina and Teflon package substrates that have higher dielectric constant and lower loss tangent.

It can be observed from Fig. 6-3 that a rapid power loss occurs around 35~36GHz within all scenarios. One may easily conclude that this is caused by TM_0 surface wave propagation [109,110] that can be supported by a grounded dielectric slab, but the unusual rebound of the insertion loss before the final drastic loss suggests a more complex situation. To the best of the author's knowledge, a surface-wave-like (SWL) propagation mode proposed by Mikio Tsuji et al. [111,112] may cause this unusual power loss rebound. The SWL mode has a field distribution similar to that of the TM_0 mode, but its coupling with dominant transmission mode of CPW occurs at a lower frequency than the TM_0 mode. Since the SWL and dominant CPW modes have opposite electric fields at the ground regions of the CPW structure, a so-called "*cancellation effect*" exists within a narrow spectral window and hence a power loss minima can be observed. A detailed field distribution around the critical spectral region is still needed to verify the existence of the "*cancellation effect*" within our scenarios. The final sharp power loss may be alleviated or suppressed by careful selection of substrate thickness and flip-chip transition height, etc [113].

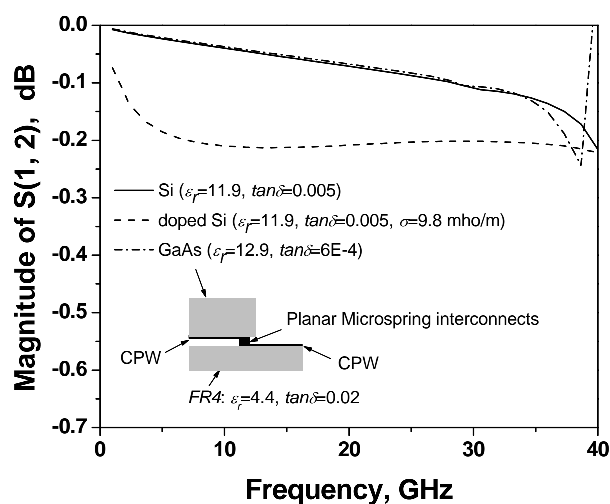
6.2.2 Planar Microspring Interconnects

Similar simulations have been conducted to demonstrate the high-frequency electrical performance of Planar Microspring interconnects in various package scenarios. Referring to Fig. 2-9(f), a J_shape planar microspring interconnect with R=7.5μm, L=25μm, W=5μm and T=2μm is used as an example. A double truncated solder joint with a height of 10μm and diameter of ~14.1μm, and a 5μm-wide Cu frame surrounding half of the periphery are included in the modeling.

Fig. 6-4(a)~(c) illustrates the power loss associated with the planar microspring interconnect as a function of pitch, chip and substrate material properties. No self resonance can be observed till 40GHz. With decrease of interconnect pitch, the electromagnetic field is confined in a smaller region and thus less power is dissipated in the forms of dielectric loss or others. On the other hand, less power loss associated with the interconnects was observed for chip and package substrates with higher dielectric constant and lower loss tangent. All of these simulation results were obtained with ~7μm-thick BCB sacrificial layer. When BCB is replaced by amorphous Si which has a higher dielectric constant, however, the power loss associated with planar microspring interconnects is increased as shown in Fig. 6-5, which is opposite to the chip and package substrate effects. This can be explained by the electromagnetic field orientation and package configuration. In a CPW scenario, the electric field starts from the signal line and points toward the ground line, while the magnetic field exists in the CPW cross section plane but is perpendicular to the electric field. For planar microspring interconnects, the sacrificial material underneath the planar microsprings is removed to form the suspended spring, but there is still sacrificial materials between neighboring interconnects. Hence, the sacrificial material effect is related to the electric field distribution, and the lower power loss for BCB



(a)



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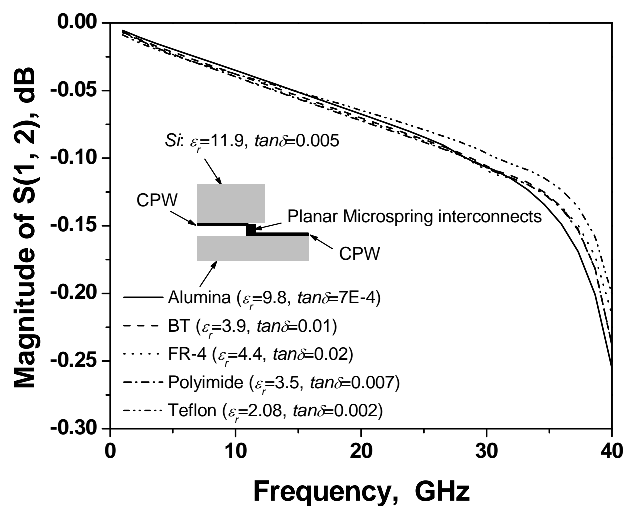


(c)

Fig. 6-4 Insertion loss *S(1,2)* of J_shape Planar Microspring interconnect depending on (a) interconnect pitch; (b) chip substrate; and (c) package substrate

arises from its lower dielectric constant, loss tangent and hence lower dielectric loss [114]. Polyimide of the same thickness demonstrated a similar loss behavior, despite its higher loss tangent (0.007) compared to that of BCB (0.0008). Increase of BCB thickness from 2μm to 10μm did not bring about remarkable improvement in the interconnect performance. On the other hand, the substrate effect is related to the magnetic field, and thus the lower power loss for high-dielectric-constant substrates can be attributed to lower eddy currents induced.

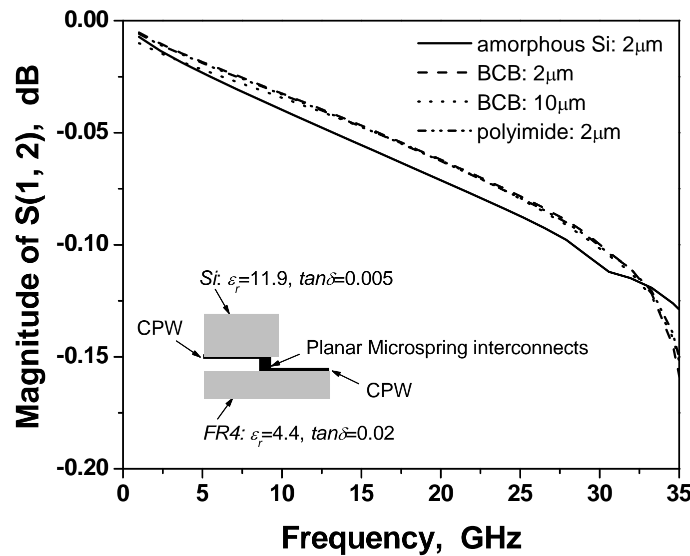


Fig. 6-5 Insertion loss *S(1,2)* of J_shape interconnect varying with sacrificial materials

6.3 Equivalent Lumped Circuit Modeling

A lumped circuit model for TCC interconnects is developed and shown in Fig. 6-6. To simplify the calculation, a symmetrical π-model is hereby used, where R represents the interconnect resistance, L represents the interconnect inductance, G represents the sum of dielectric losses associated with the chip and package substrate, and C represents the sum of capacitances associated with the interconnect. With this model, the transfer impedance *Z(1,2)* and admittance *Y(1,2)* parameter can be obtained as:

$$Y(1,2) = -\frac{1}{R + j\omega L} \qquad (6\text{-}1)$$

$$Z(1,2) = \frac{1}{\left[G + \frac{1}{4}\left(RG^2 - R\omega^2 C^2 - 2\omega^2 LCG\right)\right] + j\omega\left[C + \frac{1}{4}\left(2GCR + LG^2 - \omega^2 LC^2\right)\right]} \qquad (6\text{-}2)$$

With the assumptions:

$$G >> \frac{1}{4}(RG^2 - R\omega^2 C^2 - 2\omega^2 LCG) \qquad (6\text{-}3)$$

and

$$C >> \frac{1}{4}(2GCR + LG^2 - \omega^2 LC^2) \qquad (6\text{-}4)$$

Equation (6-2) can be simplified as:

$$Z(1,2) = \frac{1}{G + j\omega C} \qquad (6\text{-}5)$$

Therefore, the lumped circuit parameters can be obtained by simple manipulation of these two transfer parameters. Polynomial functions are obtained to approximate the frequency dependence of the circuit parameters, which are then used for verification of the equivalent circuit model. Considering the abnormal electrical behavior of the MCC interconnects at the higher spectral end as shown in Fig. 6-3, the equivalent lumped circuit parameters are extracted within frequency range of 1~33GHz.

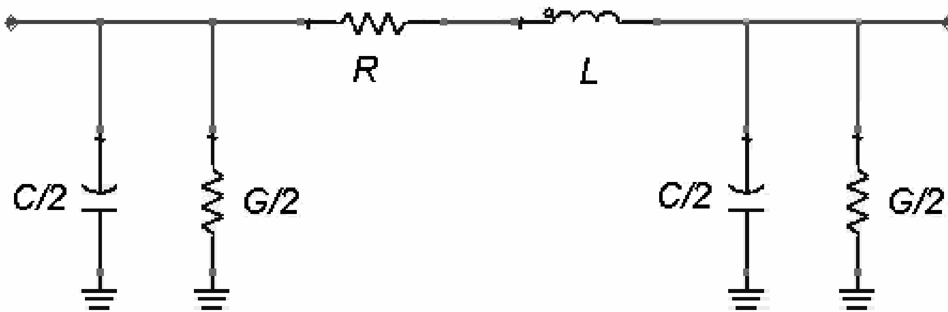
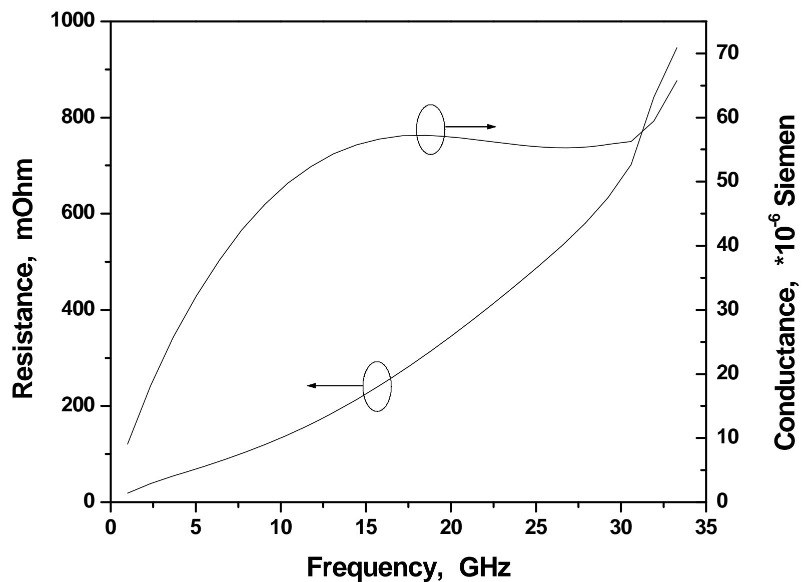
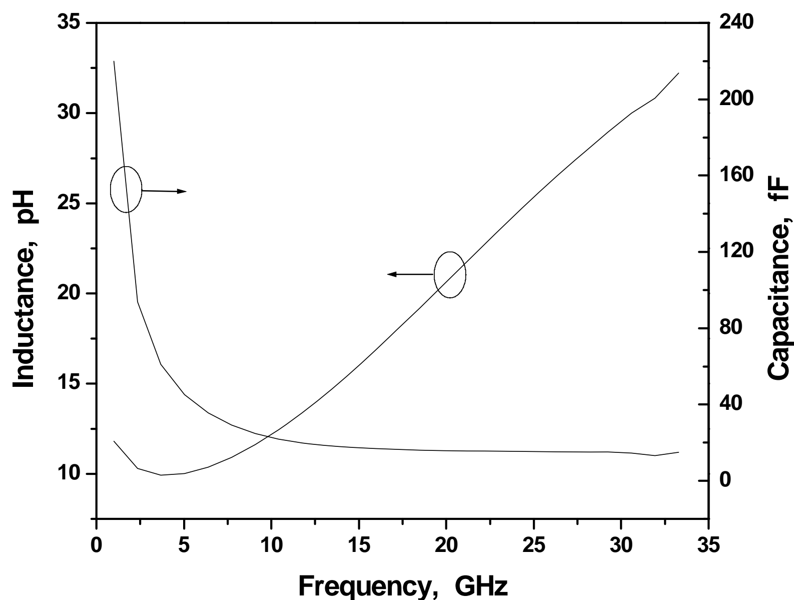


Fig. 6-6 Equivalent lumped circuit model for MCC interconnects



(a)

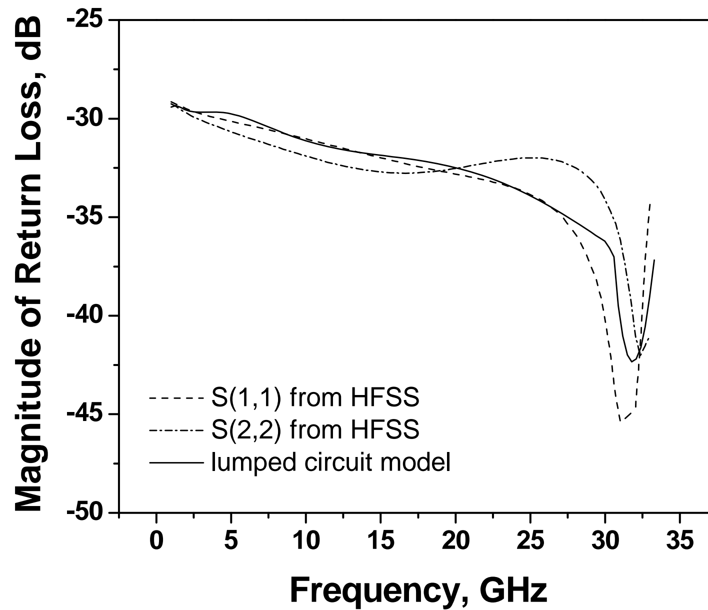


(b)

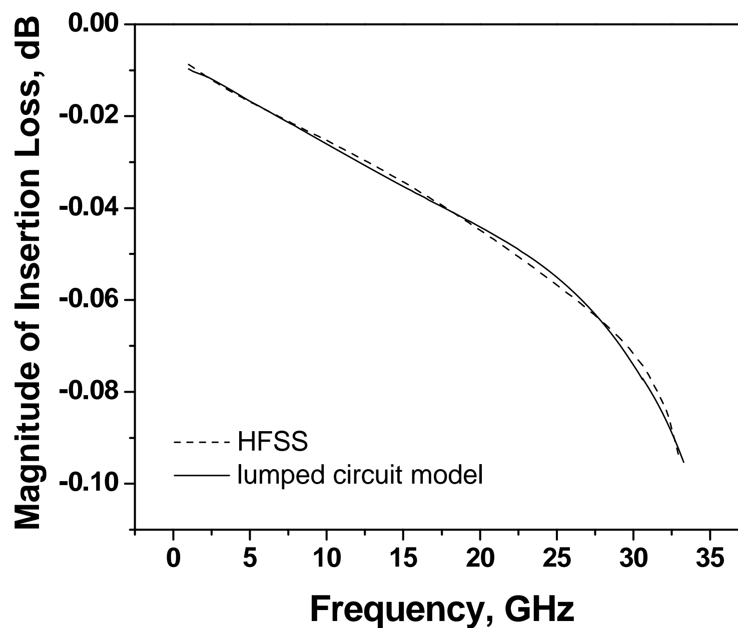
Fig. 6-7 Frequency dependence of lumped circuit parameters (a) resistance and conductance; (b) inductance and capacitance

Fig. 6-7 shows the frequency dependence of lumped circuit parameters, which confirmed the validity of equations (6-3) and (6-4) within the frequency range of interest. The resistance continuously increases with frequency and demonstrate highest frequency dependence. Fig. 6-8 shows *S*-parameter comparison of lumped

circuit model and HFSS simulation. This lumped circuit model gives good agreement with the HFSS simulation, particularly in terms of the insertion loss.



(a)



(b)

Fig. 6-8 *S*-parameter comparison between lumped circuit model and HFSS simulation (a) return loss; (b) insertion loss

Chapter 7 Conclusion and Future Work

7.1 Summary and Conclusions

The following is a brief summary of the main achievements and conclusions of this research:

1) Wafer-level fabrication has been successfully implemented for prototyping of Multi-Copper-Column (MCC) and Planar Microspring interconnects. Based on the capability of available facility, high-aspect-ratio (~6) copper columns have been achieved for MCC interconnect with ultra-fin-pitch of 40μm. Planar Microspring interconnect array with 100μm pitch is fabricated. Both fabrication procedures make use of low-cost high-throughput electroplating process to form compliant structures. All processes are fully compatible with standard CMOS back-end-of-line (BEOL) processes.
2) An analytical model based on elasticity theory was established for MCC interconnects, which relates the geometric parameters of copper columns to the solder joint reliability. This model gives a rough but quick estimation of solder joint reliability improvement due to presence of copper columns.
3) In comparison with conventional Single-Copper-Column (SCC) and pure solder interconnects, Triple-Copper-Column (TCC) interconnect demonstrated 55% and 73% higher vertical and lateral compliances, with 34% higher electrical resistance and close inductance and capacitance.
4) A *J*_shape planar microspring beam produces the best balanced performance and manufacturability among various microspring designs. For *J*_shape design, a half metal frame leads to 17% less capacitance but almost same electrical resistance and inductance as compared to full metal frame design.

5) Parametric studies have been conducted to relate the geometric parameters of both compliant interconnects to their compliances and electrical parasitics (*R*, *L* & *C*). For TCC interconnects, increasing the column radius is almost equal to decreasing the column height in terms of the effects on lateral compliance. For *J*_shape microspring interconnect, reduction of the spring thickness is most effective in enhancing the vertical compliance, and narrowing the spring beams results in rapid increase of the horizontal compliance.
6) Both compliant interconnects demonstrated good mechanical robustness as evidenced by structural integrity remaining after an external vertical loading of 20mN. The self weight of chip will not exert any perceivable deformation of both interconnects.
7) An electrical resistance of 21.1mΩ, inductance of 15.8nH and capacitance of 0.4pF were measured for TCC interconnect plus half of the on-chip and on-board metallization traces. An insertion loss of ~3dB was achieved at 2GHz using a customized high-frequency measurement set-up.
8) A systematic method has been developed to model the distinctive profile of solder joint in MCC interconnects using Surface Evolver, and then to realize seamless integration of solder joint shape modeling and stress/strain analysis in ANSYS. Using this method, the critical solder volume for solder joint bridging has been investigated as a function of various geometric parameters. Modeling of solder joint shapes using Surface Evolver produces lower fatigue damage than the conventional double truncated model (DTM).
9) The thermomechanical reliability of the solder joints in MCC interconnects is dependent on the arrangement of copper columns with respect to the chip orientation. An optimum loading angle as defined in Fig. 5-11 was obtained as

0° for TCC and 45° for Quadruple-Copper-Column (QCC) interconnects. These optimum loading angles should be followed during interconnect layout design in order to achieve maximum solder joint reliability.

10) With fixed shear displacement loading, the solder joint reliability of *MCC* interconnect increases with aspect-ratio of copper columns. However, board-level reliability analysis showed that for a given solder joint geometry, a critical aspect-ratio or compliance of interconnections exists. For an interconnection compliance below this critical value, increasing the aspect-ratio (compliance) of copper column interconnects actually leads to lower solder joint reliability. Beyond this critical value, increasing the aspect-ratio (compliance) of copper column interconnects leads to higher solder joint reliability.
11) Low power loss up to 30GHz has been found for both compliant interconnects in a coplanar waveguide (CPW) scenario. A chip or package substrate with higher dielectric constant or reduced interconnect pitch gives rise to lower power loss. For *Planar Microspring* interconnects, a sacrificial layer with lower dielectric constant and loss tangent helps reduce power loss.

In short, the 3D compliances, low electrical parasitics, low power loss up to millimeter wave range, and good wafer-level manufacturability with reasonable cost make both *MCC* and *Planar Microspring* promising candidates for next-generation high-density chip-to-package interconnections.

7.2 Future Work

The research on both compliant interconnects may be extended to include the following aspects:

1) **Further increase of I/O density and process improvement**. With the current available facility, the pitch of Planar Microspring interconnect can be further reduced from 100μm to 60μm, which implies a significant increase of I/O number from ~10,000 to ~25,000 for a fully populated $1\times1cm^2$ chip. For both interconnects, the employment of bottom-up Cu electroplating leaves seed layer behind that is hard to strip without damaging the miniaturized compliant structure. Hence, for Planar Microspring interconnect, damascene Cu electroplating may be utilized to form the microspring beams, followed by chemical-mechanical polishing to remove the seed layer. Another advantage of this scheme is that the microspring beams are flush with surrounding material, hence the risk of external damage such as scratch is reduced.

2) **Integration of embedded passives**. The wafer-level fabrication process, utilization of metallization and low-κ dielectrics such as BCB for Planar Microspring interconnects makes it easy for further integration of embedded passives (resistor, capacitor, inductor, transformer, antenna, transmission lines and so on). This enables wafer-level testing of passive components or functional blocks, and helps improve the surface estate efficiency of package substrate and reduce the system-level form factor.

3) **Reliability improvement by layout optimization using interconnects with varying compliances**. For MCC interconnects, very-high-aspect-ratio copper columns are confronted with both fabrication and handling difficulty. A practical solution to improve the solder joint reliability is to distribute interconnects with higher compliance at the peripheral region of the chip and

those with lower compliance in the central region. The stiffer interconnects in the central region help to reduce the shear displacement loading on the peripheral interconnects, while the latter has higher flexibility to relieve the strain accumulated in the solder joints. The number of interconnects with variable compliance and their positional arrangement on the chip can be optimized through board-level reliability analysis.

List of Publications and Patent:

1. ***E. B. Liao***, A. A. O. Tay, S. S. Ang, H. H. Feng, R. Nagarajan, V. Kripesh, R. Kumar and G. Q. Lo. "*Planar Microspring* — A Novel Compliant Chip-to-Package Interconnect for Wafer-level Packaging", submitted to IEEE Transactions on Advanced Packaging.
2. ***E. B. Liao***, A. A. O. Tay, S. S. T. Ang, H. H. Feng, R. Nagarajan, V. Kripesh. "Fatigue and Bridging Study of High-aspect-ratio Multi-copper-column Flip-chip Interconnects through Solder Joint Shape Modeling". IEEE Transactions on Components and Packaging Technology, Vol. 29, No. 3, September 2006, pp.560-569.
3. ***E. B. Liao***, A. A. O. Tay, S. S. Ang, H. H. Feng, R. Nagarajan, V. Kripesh. "Numerical Analysis on Compliance and Electrical Behavior of Multi-Copper-Column Flip-Chip Interconnects for Wafer-level Packaging", IEEE Transactions on Advanced Packaging, Vol. 29, No. 2, May 2006, pp.343-353.
4. ***E. B. Liao***, W. H. Teh, K. W. Teoh, A. A. O. Tay, H. H. Feng and R. Kumar. "Etching Control of Benzocyclobutene in CF_4/O_2 and SF_6/O_2 Plasmas with Thick Photoresist and Titanium Masks", Thin Solid Films, Vol. 504, No. 1-2 , 10 May 2006, pp.252-256.
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Appendix I: Simulation Code for Solder Joint Profile in Triple-Copper-Column (TCC) Interconnects

```
// tcc.fe
// three upper pads. one lower pad. bottom solder surface fixed with lower pad with
same area.
// consider contact angle at upper pads. upper pads can move vertically.
// Circular, parallel, coaxial wetted pads. With gravity.
// Both pads represented with constraints.
// Liquid entirely bounded by facets.

evolver_version "2.11c"  // needed for zforce.cdm

// interior angle between plane and surface, degrees
PARAMETER angle = 20

// virtual tension of facet on plane
#define WALLT  (-S_TENSION*cos(angle*pi/180))

// physical constants, in um-g-s units
// one dynes is 1e-5 Newton
parameter S_TENSION = 0.0463    // liquid solder surface tension, dynes/um
parameter SOLDER_DENSITY = 9.28e-12 // grams/um^3
gravity_constant 9.8e6     // um/sec^2

// configuration parameters, in unit of um
parameter height = 12.1    // height of upper pad
parameter radius_lower_pad = 16 // radius of lower pad
parameter columnr = 3.5  // radius of column
parameter spacing = 10 // center to center column spacing
parameter shift1x = spacing/2 // x value of center of 1st column
parameter shift1y = -spacing*tan(pi/6)/2 // y value of center of 1st column
parameter shift2x = 0 // x value of center of 2nd column
parameter shift2y = spacing/(2*cos(pi/6)) // y value of center of 2nd column
parameter shift3x = -spacing/2 // x value of center of 3rd column
parameter shift3y = -spacing*tan(pi/6)/2 // y value of center of 3rd column


// the edges of solder bottom surface
constraint 1
formula: z = 0

// rim of lower pad
constraint 2
formula: x^2 + y^2 = radius_lower_pad^2

// for vertices and edges confined to surface of 1st column
```

```
// with integral for blob area on 1st column
constraint 3
formula: (x-shift1x)^2 + (y-shift1y)^2 = columnr^2
energy:
e1:  -WALLT*(z-height)*(y-shift1y)/columnr
e2:  WALLT*(z-height)*(x-shift1x)/columnr
e3:   0

// for vertices and edges confined to surface of 2nd column
// with integral for blob area on 2nd column
constraint 4
formula: (x-shift2x)^2 + (y-shift2y)^2 = columnr^2
energy:
e1:  -WALLT*(z-height)*(y-shift2y)/columnr
e2:  WALLT*(z-height)*(x-shift2x)/columnr
e3:   0

// for vertices and edges confined to surface of 3rd column
// with integral for blob area on 3rd column
constraint 5
formula: (x-shift3x)^2 + (y-shift3y)^2 = columnr^2
energy:
e1:  -WALLT*(z-height)*(y-shift3y)/columnr
e2:  WALLT*(z-height)*(x-shift3x)/columnr
e3:   0

// column surface as one-sided constraint, to keep liquid from caving in
// Can be added to vertices, edges, facets that try to cave in
constraint 6 nonnegative
formula: (x-shift1x)^2 + (y-shift1y)^2 = columnr^2

// column surface as one-sided constraint, to keep liquid from caving in
// Can be added to vertices, edges, facets that try to cave in
constraint 7 nonnegative
formula: (x-shift2x)^2 + (y-shift2y)^2 = columnr^2

// column surface as one-sided constraint, to keep liquid from caving in
// Can be added to vertices, edges, facets that try to cave in
constraint 8 nonnegative
formula: (x-shift3x)^2 + (y-shift3y)^2 = columnr^2

vertices
// lower pad
1  radius_lower_pad*cos(0*pi/3) radius_lower_pad*sin(0*pi/3) 0   constraint 1,2
2  radius_lower_pad*cos(1*pi/3) radius_lower_pad*sin(1*pi/3) 0   constraint 1,2
3  radius_lower_pad*cos(2*pi/3) radius_lower_pad*sin(2*pi/3) 0   constraint 1,2
4  radius_lower_pad*cos(3*pi/3) radius_lower_pad*sin(3*pi/3) 0   constraint 1,2
5  radius_lower_pad*cos(4*pi/3) radius_lower_pad*sin(4*pi/3) 0   constraint 1,2
6  radius_lower_pad*cos(5*pi/3) radius_lower_pad*sin(5*pi/3) 0   constraint 1,2
// vertices at outer rim of upper solder surface
```

```
7  radius_lower_pad*cos(0*pi/3) radius_lower_pad*sin(0*pi/3) height
8  radius_lower_pad*cos(1*pi/3) radius_lower_pad*sin(1*pi/3) height
9  radius_lower_pad*cos(2*pi/3) radius_lower_pad*sin(2*pi/3) height
10 radius_lower_pad*cos(3*pi/3) radius_lower_pad*sin(3*pi/3) height
11 radius_lower_pad*cos(4*pi/3) radius_lower_pad*sin(4*pi/3) height
12 radius_lower_pad*cos(5*pi/3) radius_lower_pad*sin(5*pi/3) height
// upper pad
13 shift1x-columnr*cos(pi/6) shift1y+columnr*sin(pi/6) height   constraint 3
14 0 shift2y-columnr height   constraint 4
15 shift3x+columnr*cos(pi/6) shift3y+columnr*sin(pi/6) height   constraint 5
16 shift1x shift1y-columnr height   constraint 3
17 shift1x+columnr*cos(pi/6) shift1y+columnr*sin(pi/6) height   constraint 3
18 columnr*cos(pi/6) shift2y+columnr*sin(pi/6) height   constraint 4
19 -columnr*cos(pi/6) shift2y+columnr*sin(pi/6) height   constraint 4
20 shift3x-columnr*cos(pi/6) shift3y+columnr*sin(pi/6) height   constraint 5
21 shift3x shift3y-columnr height   constraint 5

edges  // defined by endpoints
// lower pad edges
1    1  2  constraint 1,2 fixed
2    2  3  constraint 1,2 fixed
3    3  4  constraint 1,2 fixed
4    4  5  constraint 1,2 fixed
5    5  6  constraint 1,2 fixed
6    6  1  constraint 1,2 fixed
// edges at the outer rim of upper solder surface
7    7  8
8    8  9
9    9  10
10   10 11
11   11 12
12   12 7
// vertical edges
13   1  7
14   2  8
15   3  9
16   4  10
17   5  11
18   6  12
// upper pad edges
19   16  17  constraints 3
20   17  13  constraints 3
21   13  16  constraints 3
22   18  19  constraints 4
23   19  14  constraints 4
24   14  18  constraints 4
25   20  21  constraints 5
26   21  15  constraints 5
27   15  20  constraints 5
// edges inside of the solder top surface
```

```
28   13  14  constraints 6,7,8 /* inner three edges anticlockwise order */
29   14  15  constraints 6,7,8
30   15  13  constraints 6,7,8
31   17  18  constraints 6,7,8 /* middle three edges anticlockwise order */
32   19  20  constraints 6,7,8
33   21  16  constraints 6,7,8
34   18  8  constraints 6,7,8 /* outer six edges anticlockwise order */
35   19  9  constraints 6,7,8
36   20  10  constraints 6,7,8
37   21  11  constraints 6,7,8
38   16  12  constraints 6,7,8
39   17  7  constraints 6,7,8

faces // defined by oriented edge loops to have outward normal
// lateral solder faces
1   1 14  -7 -13 tension S_TENSION
2   2 15  -8 -14 tension S_TENSION
3   3 16  -9 -15 tension S_TENSION
4   4 17 -10 -16 tension S_TENSION
5   5 18 -11 -17 tension S_TENSION
6   6 13 -12 -18 tension S_TENSION
// lower pad
7   -6 -5 -4 -3 -2 -1 fixed no_refine color red tension 0
// top solder faces. from inner to outer.
9   28 29 30  constraints 6,7,8 tension S_TENSION /* most inner triangle */
10   31 -24 -28 -20   constraints 6,7,8 tension S_TENSION /* middle four
quadrulateral */
11   -23 32 -27 -29   constraints 6,7,8 tension S_TENSION
12   -26 33 -21 -30   constraints 6,7,8 tension S_TENSION
13   39 7 -34 -31   constraints 6,7,8 tension S_TENSION /* outer six tradrulateral */
14   34 8 -35 -22   constraints 6,7,8 tension S_TENSION
15   35 9 -36 -32   constraints 6,7,8 tension S_TENSION
16   36 10 -37 -25   constraints 6,7,8 tension S_TENSION
17   37 11 -38 -33   constraints 6,7,8 tension S_TENSION
18   38 12 -39 -19   constraints 6,7,8 tension S_TENSION

bodies // defined by oriented face list
1   1 2 3 4 5 6 7 9 10 11 12 13 14 15 16 17 18   volume 6103 density
SOLDER_DENSITY // pi*radius_lower_pad^2*height

read

hessian_normal
```

Appendix II: Simulation Code for Solder Bridging Study of Triple-Copper-Column (TCC) Interconnects

```
// tcc_bridging.fe
// three upper pads. one lower pad. solder bottom surface fixed with lower pad with
same area.
// consider contact angle at upper pads. upper pads can move vertically.
// used for bridging study of two TCC interconnects.
// Circular, parallel, coaxial wetted pads. Gravity considered.
// all pads represented with constraints.
// liquid entirely bounded by facets.

evolver_version "2.11c"  // needed for zforce.cdm

// interior angle between plane and surface, degrees
PARAMETER angle = 20 // contact angle of solder on Cu surface

// virtual tension of facet on plane
#define WALLT  (-S_TENSION*cos(angle*pi/180))

// physical constants, in um-g-s units
// one dynes is 1e-5 Newton
parameter S_TENSION = 0.0463    // liquid solder surface tension, dynes/um
parameter SOLDER_DENSITY = 9.28e-12 // grams/um^3
gravity_constant 9.8e6     // um/sec^2

// configuration parameters for both TCCs, in unit of um
parameter height = 15   // height of upper pad
parameter radius_lower_pad = 13    // radius of lower pad
parameter columnr = 3.5  // radius of column
parameter spacing = 12 // center to center column spacing
parameter pitch = 40 // center to center interconnect spacing

// configuration parameters for 1st TCC, in unit of um. Line 41
parameter shift1x_1 = spacing/2-pitch/2 // x value of center of 1st column
parameter shift1y_1 = -spacing*tan(pi/6)/2 // y value of center of 1st column
parameter shift2x_1 = 0-pitch/2 // x value of center of 2nd column
parameter shift2y_1 = spacing/(2*cos(pi/6)) // y value of center of 2nd column
parameter shift3x_1 = -spacing/2-pitch/2 // x value of center of 3rd column
parameter shift3y_1 = -spacing*tan(pi/6)/2 // y value of center of 3rd column

// configuration parameters for the 2nd TCC, in unit of um
parameter shift1x_2 = spacing/2+pitch/2 // x value of center of 1st column
parameter shift1y_2 = -spacing*tan(pi/6)/2 // y value of center of 1st column
parameter shift2x_2 = 0+pitch/2 // x value of center of 2nd column
parameter shift2y_2 = spacing/(2*cos(pi/6)) // y value of center of 2nd column
parameter shift3x_2 = -spacing/2+pitch/2 // x value of center of 3rd column
parameter shift3y_2 = -spacing*tan(pi/6)/2 // y value of center of 3rd column
```

```
// the edges of solder bottom surface
constraint 1
formula: z = 0

// rim of lower pad
constraint 2
formula: (x+pitch/2)^2 + y^2 = radius_lower_pad^2

// rim of lower pad
constraint 3
formula: (x-pitch/2)^2 + y^2 = radius_lower_pad^2

// for vertices and edges confined to surface of 1st column of 1st TCC
// with integral for blob area on 1st column of 1st TCC
constraint 4
formula: (x-shift1x_1)^2 + (y-shift1y_1)^2 = columnr^2
energy:
e1:  -WALLT*(z-height)*(y-shift1y_1)/columnr
e2:  WALLT*(z-height)*(x-shift1x_1)/columnr
e3:   0

// for vertices and edges confined to surface of 2nd column of 1st TCC
// with integral for blob area on 2nd column of 1st TCC
constraint 5
formula: (x-shift2x_1)^2 + (y-shift2y_1)^2 = columnr^2
energy:
e1:  -WALLT*(z-height)*(y-shift2y_1)/columnr
e2:  WALLT*(z-height)*(x-shift2x_1)/columnr
e3:   0

// for vertices and edges confined to surface of 3rd column of 1st TCC
// with integral for blob area on 3rd column of 1st TCC
constraint 6
formula: (x-shift3x_1)^2 + (y-shift3y_1)^2 = columnr^2
energy:
e1:  -WALLT*(z-height)*(y-shift3y_1)/columnr
e2:  WALLT*(z-height)*(x-shift3x_1)/columnr
e3:   0

// for vertices and edges confined to surface of 1st column of 2nd TCC
// with integral for blob area on 1st column of 2nd TCC
constraint 7
formula: (x-shift1x_2)^2 + (y-shift1y_2)^2 = columnr^2
energy:
e1:  -WALLT*(z-height)*(y-shift1y_2)/columnr
e2:  WALLT*(z-height)*(x-shift1x_2)/columnr
e3:   0

// for vertices and edges confined to surface of 2nd column of 2nd TCC
```

```
// with integral for blob area on 2nd column of 2nd TCC
constraint 8
formula: (x-shift2x_2)^2 + (y-shift2y_2)^2 = columnr^2
energy:
e1:  -WALLT*(z-height)*(y-shift2y_2)/columnr
e2:  WALLT*(z-height)*(x-shift2x_2)/columnr
e3:   0

// for vertices and edges confined to surface of 3rd column of 2nd TCC
// with integral for blob area on 3rd column of 2nd TCC
constraint 9
formula: (x-shift3x_2)^2 + (y-shift3y_2)^2 = columnr^2
energy:
e1:  -WALLT*(z-height)*(y-shift3y_2)/columnr
e2:  WALLT*(z-height)*(x-shift3x_2)/columnr
e3:   0

// column surface as one-sided constraint, to keep liquid from caving in. Line 119
// Can be added to vertices, edges, facets that try to cave in
constraint 10 nonnegative
formula: (x-shift1x_1)^2 + (y-shift1y_1)^2 = columnr^2

// column surface as one-sided constraint, to keep liquid from caving in
// Can be added to vertices, edges, facets that try to cave in
constraint 11 nonnegative
formula: (x-shift2x_1)^2 + (y-shift2y_1)^2 = columnr^2

// column surface as one-sided constraint, to keep liquid from caving in
// Can be added to vertices, edges, facets that try to cave in
constraint 12 nonnegative
formula: (x-shift3x_1)^2 + (y-shift3y_1)^2 = columnr^2

// column surface as one-sided constraint, to keep liquid from caving in
// Can be added to vertices, edges, facets that try to cave in
constraint 13 nonnegative
formula: (x-shift1x_2)^2 + (y-shift1y_2)^2 = columnr^2

// column surface as one-sided constraint, to keep liquid from caving in
// Can be added to vertices, edges, facets that try to cave in
constraint 14 nonnegative
formula: (x-shift2x_2)^2 + (y-shift2y_2)^2 = columnr^2

// column surface as one-sided constraint, to keep liquid from caving in
// Can be added to vertices, edges, facets that try to cave in
constraint 15 nonnegative
formula: (x-shift3x_2)^2 + (y-shift3y_2)^2 = columnr^2

vertices
// lower pad vertices of 1st TCC. Line 150
```

```
1  radius_lower_pad*cos(0*pi/3)-pitch/2 radius_lower_pad*sin(0*pi/3) 0   constraint
1,2
2  radius_lower_pad*cos(1*pi/3)-pitch/2 radius_lower_pad*sin(1*pi/3) 0   constraint
1,2
3  radius_lower_pad*cos(2*pi/3)-pitch/2 radius_lower_pad*sin(2*pi/3) 0   constraint
1,2
4  radius_lower_pad*cos(3*pi/3)-pitch/2 radius_lower_pad*sin(3*pi/3) 0   constraint
1,2
5  radius_lower_pad*cos(4*pi/3)-pitch/2 radius_lower_pad*sin(4*pi/3) 0   constraint
1,2
6  radius_lower_pad*cos(5*pi/3)-pitch/2 radius_lower_pad*sin(5*pi/3) 0   constraint
1,2
// vertices at outer rim of upper solder surface of 1st TCC
7  radius_lower_pad*cos(0*pi/3)-pitch/2 radius_lower_pad*sin(0*pi/3) height
8  radius_lower_pad*cos(1*pi/3)-pitch/2 radius_lower_pad*sin(1*pi/3) height
9  radius_lower_pad*cos(2*pi/3)-pitch/2 radius_lower_pad*sin(2*pi/3) height
10 radius_lower_pad*cos(3*pi/3)-pitch/2 radius_lower_pad*sin(3*pi/3) height
11 radius_lower_pad*cos(4*pi/3)-pitch/2 radius_lower_pad*sin(4*pi/3) height
12 radius_lower_pad*cos(5*pi/3)-pitch/2 radius_lower_pad*sin(5*pi/3) height
// upper pad vertices of 1st TCC
13 shift1x_1-columnr*cos(pi/6) shift1y_1+columnr*sin(pi/6) height   constraint 4
14 0-pitch/2 shift2y_1-columnr height   constraint 5
15 shift3x_1+columnr*cos(pi/6) shift3y_1+columnr*sin(pi/6) height   constraint 6
16 shift1x_1 shift1y_1-columnr height   constraint 4
17 shift1x_1+columnr*cos(pi/6) shift1y_1+columnr*sin(pi/6) height   constraint 4
18 columnr*cos(pi/6)-pitch/2 shift2y_1+columnr*sin(pi/6) height   constraint 5
19 -columnr*cos(pi/6)-pitch/2 shift2y_1+columnr*sin(pi/6) height   constraint 5
20 shift3x_1-columnr*cos(pi/6) shift3y_1+columnr*sin(pi/6) height   constraint 6
21 shift3x_1 shift3y_1-columnr height   constraint 6

// lower pad vertices of 2nd TCC. Line 179
22  radius_lower_pad*cos(0*pi/3)+pitch/2 radius_lower_pad*sin(0*pi/3) 0
constraint 1,3
23  radius_lower_pad*cos(1*pi/3)+pitch/2 radius_lower_pad*sin(1*pi/3) 0
constraint 1,3
24  radius_lower_pad*cos(2*pi/3)+pitch/2 radius_lower_pad*sin(2*pi/3) 0
constraint 1,3
25  radius_lower_pad*cos(3*pi/3)+pitch/2 radius_lower_pad*sin(3*pi/3) 0
constraint 1,3
26  radius_lower_pad*cos(4*pi/3)+pitch/2 radius_lower_pad*sin(4*pi/3) 0
constraint 1,3
27  radius_lower_pad*cos(5*pi/3)+pitch/2 radius_lower_pad*sin(5*pi/3) 0
constraint 1,3
// vertices at outer rim of upper solder surface of 2nd TCC
28  radius_lower_pad*cos(0*pi/3)+pitch/2 radius_lower_pad*sin(0*pi/3) height
29  radius_lower_pad*cos(1*pi/3)+pitch/2 radius_lower_pad*sin(1*pi/3) height
30  radius_lower_pad*cos(2*pi/3)+pitch/2 radius_lower_pad*sin(2*pi/3) height
31 radius_lower_pad*cos(3*pi/3)+pitch/2 radius_lower_pad*sin(3*pi/3) height
32 radius_lower_pad*cos(4*pi/3)+pitch/2 radius_lower_pad*sin(4*pi/3) height
33 radius_lower_pad*cos(5*pi/3)+pitch/2 radius_lower_pad*sin(5*pi/3) height
```

```
// upper pad vertices of 2nd TCC
34 shift1x_2-columnr*cos(pi/6) shift1y_2+columnr*sin(pi/6) height   constraint 7
35 0+pitch/2 shift2y_2-columnr height   constraint 8
36 shift3x_2+columnr*cos(pi/6) shift3y_2+columnr*sin(pi/6) height   constraint 9
37 shift1x_2 shift1y_2-columnr height   constraint 7
38 shift1x_2+columnr*cos(pi/6) shift1y_2+columnr*sin(pi/6) height   constraint 7
39 columnr*cos(pi/6)+pitch/2 shift2y_2+columnr*sin(pi/6) height   constraint 8
40 -columnr*cos(pi/6)+pitch/2 shift2y_2+columnr*sin(pi/6) height   constraint 8
41 shift3x_2-columnr*cos(pi/6) shift3y_2+columnr*sin(pi/6) height   constraint 9
42 shift3x_2 shift3y_2-columnr height   constraint 9

edges  // defined by endpoints. Line 200
// lower pad edges of 1st TCC
1    1  2  constraint 1,2 fixed
2    2  3  constraint 1,2 fixed
3    3  4  constraint 1,2 fixed
4    4  5  constraint 1,2 fixed
5    5  6  constraint 1,2 fixed
6    6  1  constraint 1,2 fixed
// edges at the outer rim of upper solder surface of 1st TCC
7    7  8
8    8  9
9    9  10
10   10 11
11   11 12
12   12 7
// vertical edges of 1st TCC
13   1  7
14   2  8
15   3  9
16   4  10
17   5  11
18   6  12
// upper pad edges of 1st TCC
19   16  17  constraints 4
20   17  13  constraints 4
21   13  16  constraints 4
22   18  19  constraints 5
23   19  14  constraints 5
24   14  18  constraints 5
25   20  21  constraints 6
26   21  15  constraints 6
27   15  20  constraints 6
// edges inside of the solder top surface of 1st TCC
28   13  14  constraints 10,11,12,13,14,15 /* inner three edges anticlockwise order */
29   14  15  constraints 10,11,12,13,14,15
30   15  13  constraints 10,11,12,13,14,15
31   17  18  constraints 10,11,12,13,14,15 /* middle three edges anticlockwise order */
32   19  20  constraints 10,11,12,13,14,15
33   21  16  constraints 10,11,12,13,14,15
```

34 18 8 constraints 10,11,12,13,14,15 /* outer six edges anticlockwise order */
35 19 9 constraints 10,11,12,13,14,15
36 20 10 constraints 10,11,12,13,14,15
37 21 11 constraints 10,11,12,13,14,15
38 16 12 constraints 10,11,12,13,14,15
39 17 7 constraints 10,11,12,13,14,15

// lower pad edges of 2nd TCC
40 22 23 constraint 1,3 fixed
41 23 24 constraint 1,3 fixed
42 24 25 constraint 1,3 fixed
43 25 26 constraint 1,3 fixed
44 26 27 constraint 1,3 fixed
45 27 22 constraint 1,3 fixed
// edges at the outer rim of upper solder surface of 2nd TCC
46 28 29
47 29 30
48 30 31
49 31 32
50 32 33
51 33 28
// vertical edges of 2nd TCC
52 22 28
53 23 29
54 24 30
55 25 31
56 26 32
57 27 33
// upper pad edges of 2nd TCC
58 37 38 constraints 7
59 38 34 constraints 7
60 34 37 constraints 7
61 39 40 constraints 8
62 40 35 constraints 8
63 35 39 constraints 8
64 41 42 constraints 9
65 42 36 constraints 9
66 36 41 constraints 9
// edges inside of the solder top surface of 2nd TCC
67 34 35 constraints 10,11,12,13,14,15 /* inner three edges anticlockwise order */
68 35 36 constraints 10,11,12,13,14,15
69 36 34 constraints 10,11,12,13,14,15
70 38 39 constraints 10,11,12,13,14,15 /* middle three edges anticlockwise order */
71 40 41 constraints 10,11,12,13,14,15
72 42 37 constraints 10,11,12,13,14,15
73 39 29 constraints 10,11,12,13,14,15 /* outer six edges anticlockwise order */
74 40 30 constraints 10,11,12,13,14,15
75 41 31 constraints 10,11,12,13,14,15
76 42 32 constraints 10,11,12,13,14,15
77 37 33 constraints 10,11,12,13,14,15

78 38 28 constraints 10,11,12,13,14,15

faces // defined by oriented edge loops to have outward normal. Line 291
// lateral solder faces of 1st TCC
1 1 14 -7 -13 tension S_TENSION
2 2 15 -8 -14 tension S_TENSION
3 3 16 -9 -15 tension S_TENSION
4 4 17 -10 -16 tension S_TENSION
5 5 18 -11 -17 tension S_TENSION
6 6 13 -12 -18 tension S_TENSION
// lower pad of 1st TCC
7 -6 -5 -4 -3 -2 -1 fixed no_refine tension 0
// top solder faces of 1st TCC. from inner to outer.
8 28 29 30 constraints 10,11,12,13,14,15 tension S_TENSION /* most inner triangle */
9 31 -24 -28 -20 constraints 10,11,12,13,14,15 tension S_TENSION /* middle four quadrulateral */
10 -23 32 -27 -29 constraints 10,11,12,13,14,15 tension S_TENSION
11 -26 33 -21 -30 constraints 10,11,12,13,14,15 tension S_TENSION
12 39 7 -34 -31 constraints 10,11,12,13,14,15 tension S_TENSION /* outer six tradrulateral */
13 34 8 -35 -22 constraints 10,11,12,13,14,15 tension S_TENSION
14 35 9 -36 -32 constraints 10,11,12,13,14,15 tension S_TENSION
15 36 10 -37 -25 constraints 10,11,12,13,14,15 tension S_TENSION
16 37 11 -38 -33 constraints 10,11,12,13,14,15 tension S_TENSION
17 38 12 -39 -19 constraints 10,11,12,13,14,15 tension S_TENSION

// lateral solder faces of 2nd TCC
18 40 53 -46 -52 tension S_TENSION
19 41 54 -47 -53 tension S_TENSION
20 42 55 -48 -54 tension S_TENSION
21 43 56 -49 -55 tension S_TENSION
22 44 57 -50 -56 tension S_TENSION
23 45 52 -51 -57 tension S_TENSION
// lower pad of 2nd TCC
24 -45 -44 -43 -42 -41 -40 fixed no_refine tension 0
// top solder faces of 2nd TCC. from inner to outer.
25 67 68 69 constraints 10,11,12,13,14,15 tension S_TENSION /* most inner triangle */
26 70 -63 -67 -59 constraints 10,11,12,13,14,15 tension S_TENSION /* middle four quadrulateral */
27 -62 71 -66 -68 constraints 10,11,12,13,14,15 tension S_TENSION
28 -65 72 -60 -69 constraints 10,11,12,13,14,15 tension S_TENSION
29 78 46 -73 -70 constraints 10,11,12,13,14,15 tension S_TENSION /* outer six tradrulateral */
30 73 47 -74 -61 constraints 10,11,12,13,14,15 tension S_TENSION
31 74 48 -75 -71 constraints 10,11,12,13,14,15 tension S_TENSION
32 75 49 -76 -64 constraints 10,11,12,13,14,15 tension S_TENSION
33 76 50 -77 -72 constraints 10,11,12,13,14,15 tension S_TENSION
34 77 51 -78 -58 constraints 10,11,12,13,14,15 tension S_TENSION

```
bodies // defined by oriented face list. Line 334.
1   1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17   volume 14880 density
SOLDER_DENSITY
2   18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 volume 14880 density
SOLDER_DENSITY// pi* radius_lower_pad^2*height
// volume 10500 density SOLDER_DENSITY // pi*radius_lower_pad^2*height

read

// Command to merge via vertices that should be the closest ones.
// Do after evolving.
do_merge := {
   // find rightmost vertex on body 1
   highx := max(body[1].facet ff,max(ff.vertex,x));
   foreach body[1].facet ff do
    foreach ff.vertex vv do
    { if vv.x > highx - 0.00001 then
      { vertex1 := vv.id;
        break 2;
      }
    };
   // find leftmost vertex on body 2
   lowx := min(body[2].facet ff,min(ff.vertex,x));
   foreach body[2].facet ff do
    foreach ff.vertex vv do
    { if vv.x < lowx + 0.00001 then
      { vertex2 := vv.id;
        break 2;
      }
    };

   // merge the vertices, with vertex1 being kept.
   if vertex[vertex1].x >= vertex[vertex2].x then {

   vertex_merge(vertex1,vertex2);

   // transfer facets on body 2 to body 1
   set body[2].facet frontbody 1;
   body[1].target += body[2].target;
   unset body[2] target;

   // Create tunnel between the two bubbles.  The two surfaces fairly close
   // together and fairly parallel but not interpenetrating while doing this pop.
     pop vertex[vertex1];

  }
}

gogo := {  g 5; do_merge; }
```