APPLICATION OF PEEC MODELING FOR THE DEVELOPMENT OF A NOVEL MULTI-GIGAHERTZ TEST INTERFACE WITH FINE PITCH WAFER LEVEL PACKAGE

JAYASANKER JAYABALAN

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2005

APPLICATION OF PEEC MODELING FOR THE DEVELOPMENT OF A NOVEL MULTI-GIGAHERTZ TEST INTERFACE WITH FINE PITCH WAFER LEVEL PACKAGE

BY

JAYASANKER JAYABALAN

M.Sc.(Engg), National University of Singapore

A THESIS SUBMITTED FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2005

ACKNOWLEDGMENTS

TABLE OF CONTENTS

ABSTRACT

This thesis derives efficient partial element equivalent circuit (PEEC) models in homogeneous media, dielectric mesh media, inhomogeneous media with multilayered composites and applies the models for the development of a novel test interface for wafer level packages (WLP) operating at multi-gigahertz frequencies given the tight geometrical constraints of fine pitch (of the order of 100 micron) off-chip interconnects and large device pin counts (of the order of thousands).

PEEC scaling technique incorporating Baker-Campbell-Hausdorff-Dynkin series for the analysis of fine pitch geometries has been proposed. An improved PEEC model is derived for homogeneous media through the scaling of circuit elements. The model is verified with a stripline geometry. Relatively good agreements between the Method of Moments simulation data and the results generated from the scaled circuit model are obtained. PEEC modeling is then extended to lossy silicon substrates using the theory of complex images. The model is verified with a measurement based lumped circuit model. The model is found to agree with measured data over a wide frequency range for coplanar waveguides fabricated on a high resistivity silicon substrate.

For wafer level package test application, there is a need for using elastomer mesh probes due to vertical and lateral compliance requirements. A novel circuit model is developed for treating the dielectric-metal composite mixture that the probe is built with. The local interaction between the dielectric and metal is factored into the Electric Field Integral equation for accurate representation of the circuit element. The model is verified with measurements.

PEEC model of multilayer dielectric geometry is next developed to address the signal redistribution in WLP test hardware. To do this, the concept of mutual interactions between circuit elements is extended to an interface function. Isolation of the self and mutual components lends itself to separate treatment of the interface from the bulk substrate. This formulation was first tested in a quasi-static capacitance problem in a micro-strip. The per unit length capacitance was evaluated for different geometries and material properties. Then, transmission characteristics of a multilayered coupled micro-strip filter were analyzed. The treatment of the dielectric interface in terms of the convolution of the interface function and source function in pulse basis is found to give satisfactory results compared to other independent studies.

This thesis combines the modeling techniques derived above for developing a prototype test interface comprising of a compliant elastomer mesh for probing fine pitch wafer level packaged devices. The prototype has been built to handle multi-gigahertz signal propagation using 100 micron pitch GSG mesh-coplanar probes. The components of the prototype namely multilayer PCB with connectors, elastomer mesh probe, WLP interconnect and coplanar transmission lines have all been modeled. A complete system level model has been developed. The validity of the modeling as well as the efficacy of the prototype system for WLP test is demonstrated with model simulation and measurement results.

LIST OF FIGURES

LIST OF TABLES

xiv

LIST OF SYMBOLS

A	Magnetic vector potential
B	Magnetic displacement vector
D	Electric displacement vector
E	Electric field vector
G(**r,r'**)	Green's function for the field at **r** due to source at **r'**
H	Magnetic field vector
J	Electric current density
ρ	Electric charge density
i	Electric current
q	Electric Charge
V_j	Voltage across the jth circuit element
I_j	Current along the jth circuit element
L_P	Partial inductance
C_P	Partial capacitance
P_P	Partial coefficient of potential
R_P	Partial resistance
ε_0	Permittivity of free space
ε	Permittivity of a medium

Φ	Electrostatic potential
μ_0	Permeability of free space
λ_0	Wavelength in free space
k	Wave number
f	Linear frequency
ω	Angular frequency
σ	Conductivity
t_d	Retardation time
$\nabla_{\mathbf{v}} R(\mathbf{v})$	Vector of the first partial derivative of a scalar function R with respect to vector $\mathbf{v}$
$\nabla_{\mathbf{v}}^2 R(\mathbf{v})$	Matrix of the second partial derivatives of a scalar function R with respect to vector $\mathbf{v}$

CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

In conventional integrated circuit (IC) packaging, test and burn-in are done after the IC is packaged using package formats such as Quad Flat Package (QFP), Ball Grid Array (BGA), or Chip Scale Package (CSP). But this singulated device test and burn-in at the packaged IC level is very expensive.

Wafer Level Packaging (WLP) is a new paradigm in microelectronic packaging which provides solution, to arrest cost escalation, through miniaturization [1]. WLP offers batch processing capability at the wafer level. Since test and burn-in can be performed in one go with many devices in parallel, test productivity is multiplied while test cost is significantly reduced. But the need to make electrical contacts to the large number of I/O pins with fine pitches of the order of 100 microns presents new problems to the conventional wafer level test system. Furthermore, the bandwidth requirements present difficulties in the selection of materials as well as integration and fabrication methods necessitating efficient modeling of test system interface to avoid costs of multiple prototyping cycles.

Fine pitch WLPs with large number of input / output pins pose tremendous test challenges at multi-gigahertz frequencies for several reasons. The test probes need to be packed with high I/O density. They need to be mechanically compliant in the vertical direction to accommodate thickness variations in the wafer and interconnects. They also

need to be compliant in the lateral direction to accommodate thermal expansion and contraction. At the same time, they should offer good electrical contact for efficient signal transmission and integrity over several gigahertz frequency ranges.

There are many test probes available currently that meets some but not all of the test needs of WLP semiconductor devices. Coaxial probes and air-coplanar probes, for instance, provide high frequency operation but they are too bulky and so they are suited for low pin count device testing only. The cantilever beam probes have been used traditionally in the industry for testing chips with pin counts of the order of hundreds but they are very bad for high frequency testing due to huge inductance of long lead length. There are Cobra probes, membrane and DoD (die-on-die) probes from various sources but their problem is that they are not providing reliable contacts and are not scalable to very high pin counts (beyond a thousand or two). Thus the motivation behind this thesis is to provide a new solution to testing WLPs using a novel elastomer mesh material based probe geometry with a fine pitch of 100 micron and a multilayer PCB for multi-gigahertz signal distribution. The partial element equivalent circuit (PEEC) method [2] is used for modeling and physical realization of such a test interface. The content of this thesis is, therefore, (a) the derivation of efficient PEEC model in homogeneous media from the Green's function [3] and from the scattering parameter measurements, (b) derivation of efficient PEEC model in inhomogeneous media with dielectric mesh [4], (c) derivation of efficient PEEC model in inhomogeneous media with multilayered composites and (d) application of the PEEC models for the development and analysis of test interface for wafer level package operation at multi-gigahertz frequencies (about 2.5 to 5 GHz) given the tight geometrical constraints of fine pitch (of the order of 100 micron) and large

2

device pin counts (of the order of thousands). In the following section, a review of the literature on PEEC method which has been developed over the past decades for modeling multi-conductor systems in homogeneous dielectric media is given.

1.2 Partial Element Equivalent Circuit Modeling

In typical device applications, we are not interested in knowing the field values at every point in the domain of the problem. We are only interested in the terminal or nodal voltages and currents. There is the possibility to condense the field information into the circuit information that is good enough for most VLSI applications. PEEC modeling suits the purpose due to the popularity and efficiency of circuit solvers like SPICE among VLSI design community for many decades. The challenges are not only the complexity of the 3D structures, but also an ever growing number of interconnects that must be modeled accurately. PEEC provides an efficient option to handle the VLSI circuit complexity through its ability to reduce the problem order by condensing the field information at innumerable points into circuit element information over a more manageable number of area and volume elements. PEEC method is similar to the moment method with pulse function used for weight as well as basis. The interaction between capacitive displacement currents and the inductive conductor currents are to be considered for getting accurate results.

The PEEC method is applicable in both time and frequency domain [5]-[6]. Fast implementations of the method have been shown using fast multipoles and wavelets [7]-[9]. Non-orthogonal versions of the method have been proposed to handle arbitrary geometries [10]-[12]. Ruehli and Garrett [13]-[16] have made accuracy and stability

3

improvements. Model order reduction has been addressed by Antonini, Cullum and Cangellaris [17]-[24]. Numerous applications of PEEC has been demonstrated for the case of interconnects, vias, power-ground planes, LTCC circuits, spiral inductors, accurate treatment of crosstalk, skin effect and dielectric loss [19]-[55].

The availability of better CAD tools for the extraction of inductances and capacitances makes the PEEC models attractive. PEECs are equivalent to Maxwell's equations in the limit of an infinite lattice of partial elements and when retardation field is neglected. PEECs can be combined with other models, like transistors, for a circuit simulator like SPICE.

Unlike differential equation RLC lump model, PEEC includes cross-coupling terms. The mutual components are represented by delayed interaction. The circuit equation thus obtained, which is actually a delay differential circuit equation (DDE), is solved by an implicit time stepping algorithm [56]. The time domain solution of DDEs by time stepping algorithms is discussed in the next section. The method for frequency domain solution of DDE system in circuit solver is detailed in section 1.4.

1.3 Solving Delay Differential Equation (DDE) Systems

1.3.1 DDE Example with Two Nodes
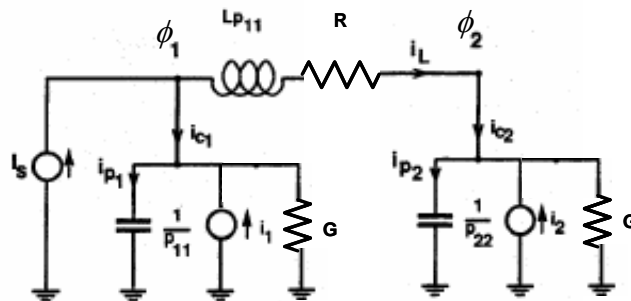
Fig. 1.1: DDE network with two nodes.

Let ϕ_1 and ϕ_2 be the potentials of a network shown in Fig. 1.1, with two nodes, which is typical of the PEEC topology. The nodes are separated by the partial inductance L_{p11} and partial resistance R. The excitation and the load currents are I_S and I_L respectively. The partial coefficients of potentials (reciprocal capacitances) corresponding to the two nodes are p_{11} and p_{22} with the conductance component G. Let τ be the interaction time delay between the two capacitances. Then, the MNA (modified nodal analysis) equations of the equivalent circuit can be written as

$$\frac{1}{p_{11}}\frac{\partial\phi_1}{\partial t} + G\phi_1 + I_L - \frac{p_{12}}{p_{11}}I_L(t-\tau) = I_S , \qquad (1.1)$$

$$\frac{1}{p_{22}}\frac{\partial\phi_2}{\partial t} + G\phi_2 - I_L + \frac{p_{12}}{p_{22}}I_L(t-\tau) = \frac{p_{12}}{p_{22}}I_S(t-\tau) , \qquad (1.2)$$

$$(\phi_2 - \phi_1) + L_{p11}\frac{\partial I_L}{\partial t} + I_L R = 0 . \qquad (1.3)$$

The time factor t is implicit for all the state variables and is suppressed for brevity except where delays are involved. In matrix operator form, the MNA equations are,

$$\begin{pmatrix} \dfrac{1}{p_{11}}\dfrac{\partial}{\partial t}+G & 0 & 1-\dfrac{p_{12}{}'}{p_{11}} \\[2mm] 0 & \dfrac{1}{p_{22}}\dfrac{\partial}{\partial t}+G & -1+\dfrac{p_{12}{}'}{p_{22}} \\[2mm] -1 & +1 & L_{p11}\dfrac{\partial}{\partial t}+R \end{pmatrix} \begin{pmatrix} \phi_1 \\ \phi_2 \\ I_L \end{pmatrix} = \begin{pmatrix} I_S \\ \dfrac{p_{12}}{p_{22}}I_S{}' \\ 0 \end{pmatrix} , \qquad (1.4)$$

where the ' is used to symbolize time delays. Upon re-arranging equation (1.4), we obtain

$$
\begin{pmatrix} \dfrac{\partial}{\partial t}\phi_1 \\[2mm] \dfrac{\partial}{\partial t}\phi_2 \\[2mm] \dfrac{\partial}{\partial t}I_L \end{pmatrix} = \begin{pmatrix} p_{11} & 0 & 0 \\ 0 & p_{22} & 0 \\ 0 & 0 & \dfrac{1}{L_{p11}} \end{pmatrix} \begin{pmatrix} G & 0 & +1 \\ 0 & G & -1 \\ -1 & +1 & R \end{pmatrix} \begin{pmatrix} \phi_1 \\ \phi_2 \\ I_L \end{pmatrix}
$$

$$
-\begin{pmatrix} p_{11} & 0 & 0 \\ 0 & p_{22} & 0 \\ 0 & 0 & \dfrac{1}{L_{p11}} \end{pmatrix} \begin{pmatrix} 0 & 0 & \dfrac{p_{12}}{p_{11}} \\[2mm] 0 & 0 & \dfrac{p_{12}}{p_{22}} \\[2mm] 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} \phi_1(t-\tau) \\ \phi_2(t-\tau) \\ I_L(t-\tau) \end{pmatrix}. \qquad (1.5)
$$

Now expression (1.5) is in a form suitable for performing the time stepping with backward Euler since the delay differential equation can be written as a delay difference equation. This example is a simple case where the matrix inversion is trivial due to the diagonal nature of the system matrix. In the most general case, however, an LU decomposition would be performed for solving the system. The solution of an example of the DDE system is illustrated with Matlab codes in Appendix A.

1.3.2 Time Stepping Algorithm for Solving Delay Differential Equation Systems

Both explicit [57] and implicit [58] schemes are available in the literature to solve the delay differential equations. Since implicit scheme is known to be stable, we use backward Euler method for the time domain solution [56].

Let **A** be the system matrix, and **x'** be the state variables and **w** the input stimuli. Then the system is represented as

$$
\mathbf{x'} = \mathbf{Ax} + \mathbf{w}. \qquad (1.6)
$$

In backward Euler method, we have

$$\mathbf{x}_{n+1} = \mathbf{x}_n + h\mathbf{x}'_{n+1}, \tag{1.7}$$

where h is the time step. Using equation (1.6) in equation (1.7), we have

$$\mathbf{x}_{n+1} = \mathbf{x}_n + h(\mathbf{A}\mathbf{x}_{n+1} + \mathbf{w}_{n+1}). \tag{1.8}$$

Rewriting equation (1.8), we get

$$(\mathbf{I} - h\mathbf{A})\mathbf{x}_{n+1} = \mathbf{x}_n + h\mathbf{w}_{n+1}. \tag{1.9}$$

If the step size is not changed during the simulation, then the matrix $(\mathbf{I} - h\mathbf{A})$ remains constant. So we need to do LU factorization only once for the matrix inversion. This makes the process very efficient.

Time domain solutions have sometimes been found to diverge after a sufficient number of time steps, because of the accumulation of numerical noise. The source of the noise could be numerical round-off errors or from the analytical and numerical approximations made in developing the circuit model. The approximation errors are said to introduce low-amplitude, right-half-plane, nonphysical poles into the model. Many techniques for solving late-time instabilities have been reported [59]. Tijhuis [60] investigated using an improved time-interpolation scheme to increase the accuracy of time derivatives. Rao *et al.* [61] used a conjugate gradient technique to control error accumulation over time. Smith [62] describes a procedure that considers the fact that late-time instabilities, generally being of a high-frequency nature relative to the correct response, can be filtered from the solution by averaging techniques.

1.4 Scattering Parameter Analysis of Circuits

First each port is represented by a resistor in series with a voltage source. The value of resistance is set to the reference resistance of the port, typically 50 Ohms. The magnitude of the source voltage is initially set to zero at all the ports.
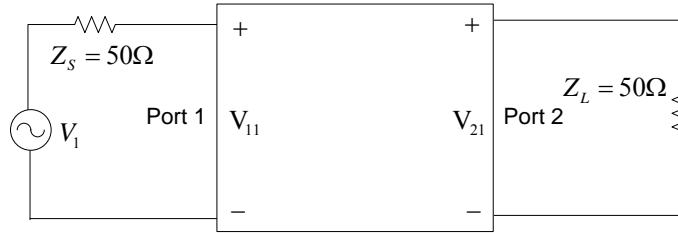
Fig. 1.2: Simulation setup for S_{11} and S_{21}.
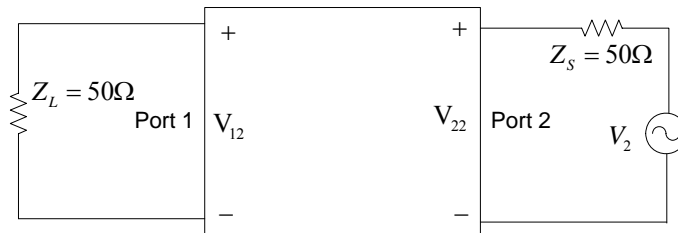
Fig. 1.3: Simulation setup for S_{12} and S_{22}.

The scattering parameters are related by

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+,$$
(1.10)

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+,$$
(1.11)

where V_1^-, V_2^- are the reflected waves and V_1^+, V_2^+ are the transmitted waves at the ports

1 and 2 respectively. Also, in Fig. 1.1 V_{11} is the sum of the transmitted and reflected

waves at port 1 and V_{21} is the sum of the transmitted and reflected waves at port 2. Thus,

$$V_{11} = V_1^+ + V_1^-, \tag{1.12a}$$

$$V_{21} = V_2^+ + V_2^-, \tag{1.12b}$$

and

$$V_1 = V_1^+ - V_1^- + V_{11}. \tag{1.13}$$

Using equation (1.12a), equation (1.13) becomes

$$V_1 = 2V_1^+. \tag{1.14}$$

Using equations (1.10), (1.12a) and (1.14), S_{11} is given by

$$S_{11} = \left. \frac{V_1^-}{V_1^+} \right|_{V_2^+ \to 0} = \frac{V_{11} - V_1^+}{V_1^+} = V_{11} - 1, \tag{1.15}$$

since the input source V_1 is excited with an amplitude of 2 volts. Using equations (1.11),

(1.12b) and (1.14), S_{21} is given by

$$S_{21} = \left. \frac{V_2^-}{V_1^+} \right|_{V_2^+ \to 0} = \left. \frac{V_{21} - V_2^+}{V_1^+} \right|_{V_2^+ \to 0} = V_{21}. \tag{1.16}$$

Fig. 1.2 shows the circuit arrangement for the computations. For computing S_{11} and S_{21}, the magnitude of the voltage source on the first port is set to 2Volts and the alternating current (AC) analysis [63] is run over the frequency range of interest. For automatically performing subtraction, a 1Volt source is installed to obtain S_{11}.

Similarly, as shown in Fig. 1.3, S_{22} and S_{12} are obtained from

$$S_{22} = V_{22} - 1, \tag{1.17}$$

$$S_{12} = V_{12}. \tag{1.18}$$

For convenience, the model simulation results are presented in the thesis in the form of scattering parameter (S parameter) data since it is easier to compare with the results of full-wave EM solvers without having to do FFT. Example SPICE codes for S parameter analysis are given in Appendix E.

1.5 Scope and Organization of this Thesis

This thesis presents the derivation and application of PEEC modeling for the development of a multi-gigahertz test interface for fine pitch wafer level packages. First, efficient PEEC models for homogeneous media are derived from a new scaling technique based on Baker-Campbell-Hausdorff-Dynkin series [64]. This technique leads to an order of improvement in relative accuracy for predicting small quantities such as return loss. Secondly, the PEEC models are extended to lossy silicon substrates and compared with lumped circuit model derived, by mapping the physical geometry to circuit elements and by applying symmetry properties of ABCD matrix elements, from scattering parameter measurements. The lump circuit approach has practical value when it is harder to derive Green's function integral terms due to singularity problem in small geometry scales and

due to material inhomogeneity and geometric discontinuity. Thirdly, PEEC models for inhomogeneous media with dielectric mesh are derived. The dielectric mesh substrate with metallization suits the need for test probes for wafer level packages. Fourthly, PEEC model for multi-layer geometry is developed by considering additional interaction terms arising from multilayer interfaces. Current generation of high speed devices and the hardware used for testing such devices are built with multi-layer substrates and boards to redistribute power and signal lines. Hence, multilayer PEEC has practical significance in the design and test of devices operating at RF and microwave frequencies. Finally, PEEC models derived above are combined and applied towards development of a complete test interface for fine pitch wafer level package for multi-gigahertz operation at probe pitch of the order of 100 micron.

Chapter 2 derives a novel PEEC model based on a perturbation technique for scaling of circuit elements in homogeneous media. Baker-Campbell-Hausdorff-Dynkin series [64] is used to scale the circuit derived from the geometry. Circuit scaling is shown to provide an order of magnitude of accuracy improvement in the prediction of return loss from PEEC models. A strip line geometry is taken as a test case. The results of the circuit model simulation are compared with that from Method of Moments (MoM). Relatively good agreements between the scaled circuit model simulation data and the MoM are obtained.

PEEC modeling derived in Chapter 2 is extended to lossy substrates using the theory of images. The extended model is compared with a measurement based lumped circuit model. The lumped circuit model is optimized in a least squares sense using the measured data. Congruent property of the geometry and the resultant symmetry of the

ABCD matrix structure are used to derive the optimization algorithm. A sample device having coplanar waveguide structure fabricated on high resistivity silicon substrate (2 kilo-ohm cm) is used as a test case. The models and measurements are well matched over 100 MHz to 20 GHz range.

For wafer level package test applications, there is a need to use elastomer mesh substrate based probes due to vertical and lateral compliance requirements. A novel PEEC model is developed in Chapter 4 for treating the dielectric-metal composite mixture that the probe is built with. The local interaction between the dielectric and metal is factored into the electric field integral equation for accurate representation of the circuit elements. The model is verified with measurements in a coplanar GSG (Ground Signal Ground) probe structure.

In Chapter 5, PEEC method for multilayer dielectric geometry is presented. To do this, the concept of mutual interactions between circuit elements is extended to an interface function. Isolation of the self and mutual components lends itself to separate treatment of the interface from the bulk substrate. This formulation is first tested in a quasi-static capacitance problem in a micro-strip. The per unit length capacitance is evaluated for different geometries and material properties. Then transmission characteristics of a multilayered coupled micro-strip filter are analyzed. The treatment of the dielectric interface in terms of the convolution of the interface function with source function in pulse basis in the time domain is found to give satisfactory results compared to other studies based on the method of moments.

Application of PEEC modeling for WLP test interface prototype development is discussed in Chapter 6. The details of modeling a prototype test hardware comprising of a

compliant elastomer mesh, a multilayer printed circuit board substrate with coplanar transmission lines and coaxial connectors are presented. The test hardware is built to handle multi-gigahertz signal propagation using 100 micron pitch GSG mesh-coplanar probes. The components of the test hardware such as the SMA connectors, coplanar transmission lines on the PCB, off-chip and on-chip interconnect of the WLP and elastomer mesh probe have all been modeled. Two cases of system level model containing the above sub-systems, one based on PEEC and the other from full-wave solver, has been developed and compared. The numerical results of scattering parameters from both modeling and the measurements on the prototype are found to be in good agreement over the frequency range from DC to 5 GHz.

1.6 Original Contributions

As a result of this research, the following contains the original contributions made by the author of this thesis:

A new perturbation technique based on Baker-Campbell-Hausdorff-Dynkin [64] series for PEEC scaling is presented. This technique effectively reduces the stiffness of the differential equation system. Consequently, an order of improvement in the prediction accuracy of small quantities such as return loss is achieved.

PEEC model is extended to lossy substrates and verified with a measurement based lumped circuit modeling methodology. The lumped circuit modeling method is valuable where Green's function approach fares poorly due to its singular behaviour and due to the material inhomogeneity and geometric discontinuity in the small region. The congruent

symmetry of the model and the consequent simplicity of the ABCD matrices are used to develop this method.

PEEC method for modeling dielectric mesh medium including metallization is derived. The mesh has novel electrical and mechanical properties that make it attractive for applications such as wafer level package test.

Interface function coefficients based on the method of images is derived. This method takes into account the effect of multiple stacks of dielectrics, which are common in current CMOS, LTCC and other integrated circuit and package fabrication technologies. Multilayer PEEC modeling method is derived using the interface function. This method makes it possible to represent multilayer objects in terms of circuit elements without the need to rely on full-wave field solvers.

A test methodology is demonstrated for fine pitch (of the order of 100 micron), high pin count (of the order of thousands) wafer level packages at high frequencies (of the order of gigahertz) using elastomer mesh probes.

The contributions made in this research are reported in the following publications:

1.6.1 Journals

1. J. Jayabalan, B.L. Ooi, M.S. Leong and M.K. Iyer, "A scaling technique for partial element equivalent circuit analysis using SPICE," *Microwave and Wireless Components Letters, IEEE* ,Vol. 14 , Issue: 5 , pp. 216 – 218, March 2004.

2. J. Jayabalan, W. Bin, D. X. Xu, B.L. Ooi, M. S. Leong and M. K. Iyer, "A methodology for accurate modeling of pad structure from S-Parameter

14

measurements," *Microwave and Optical Technology Letters,* Vol.45, Issue 2, pp. 115-118, Wiley Interscience, April 2005.

3. J. Jayabalan, B.L. Ooi, M.K. Iyer and M.S. Leong, "Modeling and application of elastomer mesh for microwave probing," *IEE proceedings on Microwaves, Antennas and Propagation*, Vol.153, No. 1, pp.83-88, Feb 2006.

4. J. Jayabalan, R. Jayaganthan, A.A.O. Andrew Tay and B.L. Ooi., "Energetics of Copper Nanowires," *International Journal of NanoScience*, World Scientific, Singapore, Vol. 4, No. 4, pp 717-724, Aug. 2005.

5. J. Jayabalan, B.L. Ooi, M.S. Leong and M.K. Iyer, "Novel Circuit Model for Three-Dimensional Geometries with Multilayer Dielectrics," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 54, Issue 4, Part 1, pp. 1331 – 1339, Jun 2006.

1.6.2 Journal Submissions under Review

6. J. Jayabalan, M.K.Iyer, M.D. Rotaru, V.S. Rao. V. Kripesh, B.L. Ooi and M.S. Leong, "A novel test strategy for fine pitch wafer level packaged devices," to appear in *IEEE CPMT Transactions on Advanced Packaging*.

1.6.3 Conferences

1. J. Jayabalan, M.D. Rotaru, D. Chun, H.H. Feng, M.K. Iyer, B.L. Ooi, M.S. Leong, S. Ang, A.A.O. Tay, D. Keezer and T. Rao, "Test strategies for fine pitch wafer level packaged devices;" *Electronics Packaging Technology Conference Proceedings,* pp. 397 – 400, 10-12 Dec. 2003.

2. J. Jayabalan, C.K. Goh, B.L. Ooi, M.S. Leong, M.K. Iyer and A.A.O. Tay, "PLL based high speed functional testing, "*IEEE Proceedings Asian Test Symposium*, pp. 116 – 119, ATS 2003.

3. J. Jayabalan, W. Bin, D. X. Xu, B.L. Ooi, M. S. Leong and M. K. Iyer," Pad modeling from S-Parameter measurements," in *Progress in electromagnetic research symposium proceedings, Nanjing, China, PIERS,* Aug. 2004.

4. J.Jayabalan, M.D.Rotaru, Jimmy PH Tan, M.K.Iyer, B.L.Ooi and M.S. Leong, "Test Bench modeling and characterization for fine pitch wafer level packaged devices, *IEEE Electronics Packaging Technology Conference Proceedings,* pp. 502 – 505, Dec. 2004.

5. J. Jayabalan, B.L. Ooi, and M. S. Leong, "PEEC Model for Multiconductor Systems Including Dielectric Mesh," *Asia Pacific Microwave Conference proceedings,Suzhou, China,* Vol. 2, Dec. 2005.

6. J. Jayabalan and M.D. Rotaru, "High Frequency Characterizaion of 100 micron pitch wafer level package interconnects," to appear in *IEEE Electronics Packaging Technology Conference Proceedings*, Vol. 1, pp 171-174, Dec. 2005.

1.6.4 Patents

1. J. Jayabalan, M.D. Rotaru, M.K. Iyer, and A.A.O. Tay, "Compliant Probes and Test Methodology for Fine Pitch Wafer Level Devices and Interconnects," filed in US Patents and Trademarks Office, No. 11/207336, August, 2005.

CHAPTER 2

MODELING OF HOMOGENEOUS LOSSLESS MEDIA BY PEEC METHOD

2.1 Introduction

A scaling technique for Partial Element Equivalent Circuit analysis using SPICE is presented in this Chapter. The conventional PEEC model in homogeneous medium is first reviewed. The Baker-Campbell-Hausdorff-Dynkin (BCHD) series [64] for exponential matrices is then derived. Then BCHD series approximation based matrix transformation and scaling is applied to the component values extracted by the standard PEEC method to get up to an order of magnitude improvement in relative accuracy of scattering parameters with SPICE simulation. The effectiveness of the technique is verified by using the numerical example of a stripline structure and comparing the results with that of the Method of Moments (IE3D).

In PEEC modeling of micron size multi-conductor geometries, the resistance values are quite small, while the reactance values are relatively large at GHz frequencies. This huge spread in the network component values leads to poor results or ill-conditioned matrices in circuit simulation using SPICE. For example, in a microstrip structure, the transmission parameter values (S_{21}) from circuit simulation are accurate to within 5% of the expected reference value from the full-wave solution while the errors in reflection parameter values (S_{11}) are as high as 50%. Conventional linear techniques like impedance scaling and frequency scaling [56] are not enough to handle this problem

17

since this does not improve the matrix condition. A scaling technique based on the approximation of BCHD series [65]-[66] is applied to alleviate this problem.

2.2 Deriving the PEEC Model in Homogeneous Media

The PEEC model in Fig. 2.1 comes from mapping the field problem into a circuit problem. The Maxwell equations are represented in the form of an Electric Field Integral Equation (EFIE) in terms of scalar and vector potentials.
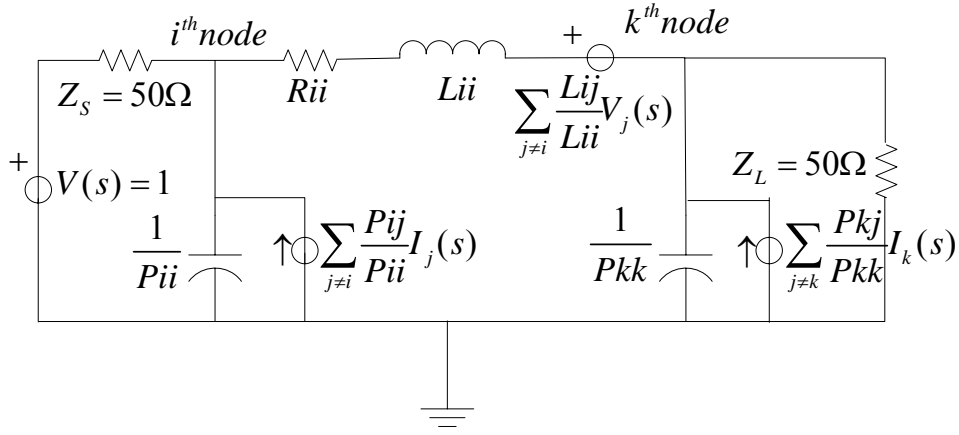
Fig. 2.1: PEEC model

Starting with the Maxwell equation,

$$\nabla \cdot \mathbf{B} = 0 , \qquad\qquad (2.1)$$

which means that **B** could be considered as a curl of some term **A** called vector potential, we have,

$$\mathbf{B} = \nabla \times \mathbf{A} . \qquad\qquad (2.2)$$

Again , from Faraday's Law

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} , \qquad\qquad (2.3)$$

18

$$\nabla \times \mathbf{E} = -\frac{\partial}{\partial t}(\nabla \times \mathbf{A}),\tag{2.4}$$

$$\nabla \times \left(\mathbf{E} + \frac{\partial \mathbf{A}}{\partial t}\right) = 0.\tag{2.5}$$

$\mathbf{E} + \dfrac{\partial \mathbf{A}}{\partial t}$ is a vector whose curl is zero. This means that the vector is equivalent to the

gradient of a scalar called the scalar potential. That is

$$\mathbf{E} + \frac{\partial \mathbf{A}}{\partial t} = -\nabla \phi,\tag{2.6}$$

$$\mathbf{E} = -\frac{\partial \mathbf{A}}{\partial t} - \nabla \phi.\tag{2.7}$$

If the loss term due to conductivity were added, equation (2.7) would become

$$\mathbf{E} = -\frac{\partial \mathbf{A}}{\partial t} - \nabla \phi - \frac{\mathbf{J}}{\sigma}.\tag{2.8}$$

where $\mathbf{E}$ is the incident field. In general, $\mathbf{E} = \mathbf{E}^i + \mathbf{E}_s$ contains both incident ($\mathbf{E}^i$) and

scattered ($\mathbf{E}_s$) components. For representing the scattered term, $\mathbf{E}=\mathbf{0}$ for a conservative

system gives

$$\mathbf{E}_s(\mathbf{r},t) = \frac{\partial \mathbf{A}(\mathbf{r},t)}{\partial t} + \nabla \phi(\mathbf{r},t) + \frac{\mathbf{J}(\mathbf{r},t)}{\sigma}.\tag{2.9}$$

Here, $\mathbf{r}$ is the distance vector between source and field points, and t is time.

Integrating the above equation over the volume, we arrive at the macroscopic Kirchoff's

voltage equation. Since the voltage around the closed loop is zero, we have

$$\frac{\mathbf{J}(\mathbf{r},t)}{\sigma} + \frac{\mu}{4\pi}\int_{v'} G(\mathbf{r},\mathbf{r}')\frac{\partial \mathbf{J}(\mathbf{r}',t_d)}{\partial t}dv' + \frac{\nabla}{4\pi\varepsilon_0}\int_{v'} G(\mathbf{r},\mathbf{r}')q(\mathbf{r}',t_d)dv' = 0,\tag{2.10}$$

where $G(\mathbf{r},\mathbf{r}')$ and t_d are the kernel function and time retardation respectively, given by

$$G(\mathbf{r},\mathbf{r}') = \frac{1}{|\mathbf{r}-\mathbf{r}'|}, \tag{2.11}$$

$$t_d = t - \frac{|\mathbf{r}-\mathbf{r}'|}{c}. \tag{2.12}$$

For the inclusion of stratified dielectric region, we note that

$$\nabla \times \mathbf{H} = \mathbf{J} + \varepsilon_0(\varepsilon_r - 1)\frac{\partial \mathbf{E}}{\partial t} + \varepsilon_0 \frac{\partial \mathbf{E}}{\partial t}. \tag{2.13}$$

Here, we consider the total current as

$$\mathbf{J}_{tot} = \mathbf{J}(\mathbf{r},t) + \varepsilon_0(\varepsilon_r - 1)\frac{\partial \mathbf{E}}{\partial t}, \tag{2.14}$$

which is a combination of conduction current and displacement current, to formulate the integral equation. The integral equation for a conductor cell then becomes,

$$\frac{\mathbf{J}(\mathbf{r},t)}{\sigma} + \frac{\mu}{4\pi}\int_{v'} G(\mathbf{r},\mathbf{r}')\left[\frac{\partial \mathbf{J}(\mathbf{r}',t_d)}{\partial t} + \varepsilon_0(\varepsilon_r - 1)\frac{\partial^2 \mathbf{E}(\mathbf{r}',t_d)}{\partial t^2}\right]dv' + \frac{\nabla}{4\pi\varepsilon_0}\int_{v'} G(\mathbf{r},\mathbf{r}')q(\mathbf{r}',t_d)dv' = 0.$$

$$\tag{2.15}$$

In the above equation, the first term is the resistance term, the second term is the inductance term and the third term is the capacitance term respectively.

When the source and the field are spread in different volume regions, we can generalize the above equation by converting the single volume integral into double integrals where the interaction terms are respectively called mutual partial inductance and mutual partial capacitance. We need to extract the lumped circuit parameters (partial inductance L, coefficient of potential P and patch resistance R) from the kernel function representation of scalar and vector potentials.

The partitioning of geometry is done such that the Inductance patches (current elements) and the capacitance patches (charge elements) are orthogonal and are placed

half a cell away from each other. This partitioning is clearly depicted in Figs. 2.2-2.3 for

the case of two dimensional object such as a thin conducting microstrip.
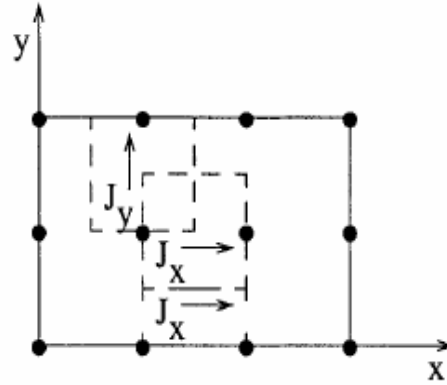
Fig. 2.2: Sectioning the object geometry into inductance partitions.
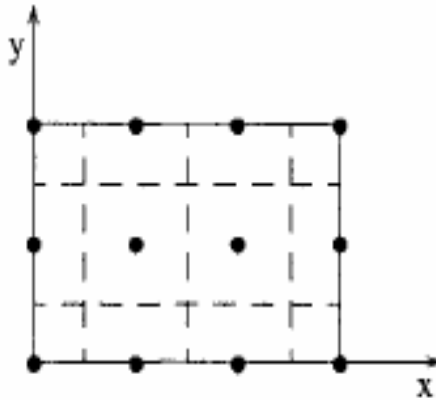
Fig. 2.3. Sectioning the object geometry into capacitive partitions.

The integral of quasi-static free space Green's function kernel which represents the

circuit components is evaluated by numerical quadrature or using approximate analytical

and closed form expressions [19], [67]-[69] for quick evaluation of component values.

The evaluation of the Green's function kernel leads to the PEEC model with self- and

partial- inductance and capacitance terms. The calculations of Green's function integral

kernels are detailed in Appendix B.

2.3 Baker-Campbell-Hausdorff-Dynkin Series Expression

Given two $n \times n$ matrices namely x and y, the objective is to find a power series $z = C(x, y)$ such that the equation

$$e^x e^y = e^z, \quad e^x = \sum_{n=0}^{\infty} \frac{x^n}{n!}, \tag{2.16}$$

holds. The solution of the matrix problem could be obtained by treating x and y as variable elements that obey certain non-commutative algebra rules. It is assumed that the matrices x and y are close to zero matrices to ensure the convergence of the series.

To proceed with the derivation, a Hausdorff derivative operator is defined as

$$u \frac{\partial}{\partial x} (x^k y x^m) = u x^{k-1} y x^m + x u x^{k-2} y x^m + x^2 u x^{k-3} y x^m + \cdots$$

$$+ x^{k-1} u y x^m + x^k y u x^{m-1} + \cdots + x^k y x^{m-1} u . \tag{2.17}$$

For the case of e^x, the relation

$$u \frac{\partial}{\partial x} e^x = u + \frac{1}{2!}(ux + xu) + \frac{1}{3!}(ux^2 + xux + x^2 u) + \cdots \tag{2.18}$$

is obtained. This results in the expression for $e^{x+\alpha u}$ as

$$e^{x+\alpha u} = e^x + \alpha u \frac{\partial}{\partial x} e^x + \alpha^2 (.) + \cdots, \tag{2.19}$$

where α is a real or complex parameter. To derive the coefficients of the series $C(x,y)$ explicitly, a deformation of x and y in terms of a special series with variables u and v gives

$$e^x e^y = e^x \left[1 + \alpha \varphi(u, x) + \cdots \right] \left[1 - \alpha \psi(v, y) + \cdots \right] e^y . \tag{2.20}$$

The vanishing of the term corresponding to α implies that

$$\varphi(u, x) = \psi(v, y), \tag{2.21}$$

22

and

$$u_{\uparrow x} \frac{\partial}{\partial x} z = v_{\uparrow \omega(x,y)} \frac{\partial}{\partial y} z \,, \qquad (2.22)$$

where the symbol $\uparrow$ is used to mean that the substitutions of $u = x$ (as a convenient choice) and $v = \omega(x, y)$ are made.

In order to calculate $\omega(x, y)$, an alternating series of the type

$$x = v \frac{1 - e^{-y}}{y} = v - \frac{1}{2!} vy + \frac{1}{3!} vy^2 - \cdots + \frac{(-1)^n}{(n+1)!} vy^n + \cdots, \qquad (2.23)$$

is considered. Using the standard expansion form of $\dfrac{y}{1 - e^{-y}}$, the $v = \omega(x, y)$ series is found to be

$$v = x \frac{y}{1 - e^{-y}} = x + \frac{1}{2} xy + \frac{B_1}{2!} xy^2 - \frac{B_2}{4!} xy^4 + \cdots + (-1)^{n-1} \frac{B_n}{(2n)!} xy^{2n} + \cdots, \qquad (2.24)$$

where B_1, B_2, $\dots$ B_n are the Bernoulli numbers defined by

$$B_n = \frac{2(2n)!}{(2\pi)^{2n}} \sum_{k=1}^{\infty} \frac{1}{k^{2n}}. \qquad (2.25)$$

Expansion on both sides of equation (2.22) leads to

$$u_{\uparrow x} \frac{\partial}{\partial x} C(x, y) = C_1(\cdot) + 2C_2(\cdot) + 3C_3(\cdot) + \cdots = v_{\uparrow \omega(x,y)} \frac{\partial}{\partial y} \big[C_0(\cdot) + C_1(\cdot) + C_2(\cdot) + \cdots \big], \qquad (2.26)$$

where $C_n = C_n(x, y)$ is the term of the nth order.

Equating the coefficients on both sides of equation (2.26) gives $C_0(x, y) = y$ (by virtue of (2.16)) and

$$C_1(x, y) = v_{\uparrow \omega(x,y)} \frac{\partial}{\partial y} C_0(x, y), \qquad (2.27)$$

23

$$2C_2(x, y) = v_{\uparrow \omega(x,y)} \frac{\partial}{\partial y} C_1(x, y).$$ (2.28)

$$3C_3(x, y) = v_{\uparrow \omega(x,y)} \frac{\partial}{\partial y} C_2(x, y),$$ (2.29)

and similarly for the following coefficient terms. Thus, the desired series $C(x, y)$ up to $(2n+1)^{th}$ order is constructed by recursion of terms in equations (2.27), (2.28) up to the C_{n-1}^{th} term.

In particular, the series expansion up to five orders is

$$C(x, y) = x + y + \frac{1}{2}{}^{\wedge}[xy] + \frac{1}{12}{}^{\wedge}[yx^2] + \frac{1}{12}{}^{\wedge}[xy^2] + \frac{1}{24}{}^{\wedge}[yx^2y] - \frac{1}{720}{}^{\wedge}[xy^4] - \frac{1}{720}{}^{\wedge}[yx^4]$$

$$+ \frac{1}{360}{}^{\wedge}[xy^3x] + \frac{1}{360}{}^{\wedge}[yx^3y] - \frac{1}{120}{}^{\wedge}[xy^2xy] - \frac{1}{120}{}^{\wedge}[yx^2yx] + \cdots, \quad (2.30a)$$

where the symbol $^{\wedge}$ is defined such that $^{\wedge}[xy] := [x, y] = xy - yx$ and $^{\wedge}[abc \cdots xyz] := [^{\wedge}[abc \cdots xy], z]$. The series is known to be convergent around the zero point. This property is of significance in applications such as the circuit solution for reflection coefficients (return loss) which are typically two orders of magnitude smaller than transmission coefficients (insertion loss).

A dual formula to the BCHD series, due to Zassenhaus [70], exists and is given by

$$e^{t(x+y)} = e^{tx} e^{ty} e^{t^2 \frac{1}{2}[y,x]} \cdots.$$ (2.30b)

2.4 Scaling the System Matrix

Let **A** be the system matrix, consisting of memory-less elements **G**, memory elements **C** and complex frequency $s = j2\pi f$, given as

$$A = G + sC .$$ (2.31)

Let **G'** be the perturbation matrix of resistive elements. Then the resulting exponent can be written as

$$e^{A}e^{G'} = e^{A+G'+\frac{1}{2}[A,G']+\frac{1}{12}[A,[A,G']]+\frac{1}{12}[G',[A,G']]+\frac{1}{24}[[A,[A,G'],G']+\cdots} .$$ (2.32)

This is the Baker-Campbell-Hausdorff-Dynkin series in which

$$[A,G'] = AG' - G'A ,$$ (2.33)

is the Jacobi bracket of matrix commutation. Approximation of the convergent series by removing the higher order terms

$$[A,[A,G']] = [G',[A,G']] = 0 ,$$ (2.34)

which are negligible, results in

$$e^{A}e^{G'} \approx e^{A+G'+\frac{1}{2}[A,G']} .$$ (2.35)

A compensation matrix **C'** defined as

$$e^{sC'} \approx e^{-G'-\frac{1}{2}[A,G']} ,$$ (2.36)

is now introduced so that the product

$$e^{A}e^{G'}e^{sC'} \approx e^{A+G'+\frac{1}{2}[A,G']-G'-\frac{1}{2}[A,G']} \approx e^{A} ,$$ (2.37)

is equivalent to the actual system matrix. The rate of change of energy and hence the perturbation of the system states is proportional to the frequency and the size of the memory elements. Thus the commutator can be represented as

$$[A,G'] \approx sC .$$ (2.38)

Substitution of equation (2.38) in equation (2.36) gives,

$$C' \approx -\frac{1}{2}C - \frac{1}{s}G' \tag{2.39}$$

The matrix **C'** is the memory element compensation necessary, due to the perturbation of memory-less element matrix G', to preserve the system   The choice of **G'** is governed by the circuit element spread.

System matrix scaling through the perturbation described above has the effect of improving its condition number which is quantified as follows [71]:

Let the system matrix **A** be scaled as **A+E** due to small perturbation **E=G'+sC'**. Let **x** be the solution of the linear system

$$\mathbf{Ax} = \mathbf{b}. \tag{2.40}$$

Let **x*** be the solution of the perturbed system such that

$$(\mathbf{A} + \mathbf{E})(\mathbf{x} + \boldsymbol{\delta}) = \mathbf{b}, \tag{2.41}$$

where $\boldsymbol{\delta} = \mathbf{x}* - \mathbf{x}$. Subtracting equation (2.40) from equation (2,41), we get

$$(\mathbf{A} + \mathbf{E})\boldsymbol{\delta} = -\mathbf{Ex}, \tag{2.42}$$

which implies that

$$\boldsymbol{\delta} = -\mathbf{A}^{-1}\mathbf{E}(\mathbf{x} + \boldsymbol{\delta}). \tag{2.43}$$

Therefore

$$\|\boldsymbol{\delta}\| \leq \|\mathbf{A}^{-1}\| \cdot \|\mathbf{E}\| (\|\mathbf{x}\| + \|\boldsymbol{\delta}\|) = \frac{Cond(\mathbf{A})}{\|\mathbf{A}\|} \|\mathbf{E}\| (\|\mathbf{x}\| + \|\boldsymbol{\delta}\|), \tag{2.44}$$

where *Cond*(**A**) refers to the condition number of **A** and the matrix norm $\|\mathbf{A}\|$ is given by

$$\|\mathbf{A}\| = \max_{\mathbf{x} \neq 0} \frac{\|\mathbf{Ax}\|}{\|\mathbf{x}\|}. \tag{2.45}$$

Solving the inequality (2.44) for $\|\boldsymbol{\delta}\|$, we get

$$\|\boldsymbol{\delta}\| \leq \frac{Cond(\mathbf{A})\dfrac{\|\mathbf{E}\|}{\|\mathbf{A}\|}\|\mathbf{x}\|}{1 - Cond(\mathbf{A})\dfrac{\|\mathbf{E}\|}{\|\mathbf{A}\|}}, \tag{2.46}$$

where the assumption that

$$Cond(\mathbf{A})\frac{\|\mathbf{E}\|}{\|\mathbf{A}\|} = \|\mathbf{A}^{-1}\| \cdot \|\mathbf{E}\| < 1 \tag{2.47}$$

has been made. From the inequality (2.46), we conclude that

$$\frac{\|\boldsymbol{\delta}\|}{\|\mathbf{x}\|} \leq \frac{Cond(\mathbf{A})\dfrac{\|\mathbf{E}\|}{\|\mathbf{A}\|}}{1 - Cond(\mathbf{A})\dfrac{\|\mathbf{E}\|}{\|\mathbf{A}\|}}. \tag{2.48}$$

The inequality (2.48) shows that small $Cond(\mathbf{A})$ indicates a small relative change in the solution. When $Cond(\mathbf{A})$ is large, introduction of small perturbation in $\|\mathbf{E}\|$ helps to reduce the error in the solution.

2.5 Numerical Example

A symmetric stripline geometry with the size of length $=500\,\mu m$, width $=25\,\mu m$ and thickness $= 0.5\,\mu m$ of copper with dielectric permittivity $= 1$ and ground plane spacing of $20\,\mu m$ as shown in Fig. 2.4, is chosen as a test example. The conductor loss is governed by the finite conductivity of copper which is taken as 5.8×10^7 Siemens/m. The dielectric loss is absent since free space is taken as a dielectric medium. The geometry is specifically chosen to obtain a characteristic impedance of 50 ohms. This helps to

simplify the treatment of PEEC boundary with the source and load terminal nodes to be 50 ohms each.
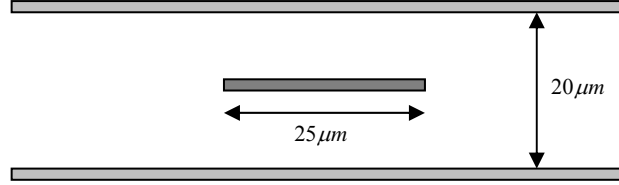
Fig. 2.4: Cross-section of stripline transmission line

The thin geometry allows for 2-dimensional basis functions to be used in the PEEC model. The pulse functions are used as the basis and weights. By sub-sectioning the geometry, it ($<\lambda/10$) results in 9+8=17 inductors, 17 resistors and 12 capacitors. The ground planes are replaced by the image elements. The partial inductance, partial potential coefficient (reciprocal of capacitance) and resistance values are obtained through

$$L_P = \frac{\mu}{4\pi l l'} \iint_{s\ s'} K(r,r')\,ds\,ds',\tag{2.49}$$

$$P_P = \frac{1}{C_P} = \frac{1}{4\pi\varepsilon a} \int_{s'} K(r,r')\,ds',\tag{2.50}$$

$$R_P = \frac{L}{\sigma W t},\tag{2.51}$$

where *K(r,r')* is the inverse distance kernel with *r* and *r'* representing distances, *ds* and *ds'* area segments and *l* and *l'* length segments (perpendicular to the direction of current flow) of the observation and source cells respectively; *a* is the surface area of the

28

capacitive partition segment and *L, W , t* and σ are the segment length (along the direction of current flow), width, thickness and conductivity respectively. We have used the surface integrals instead of the volume integrals for inductance calculations, which significantly reduce the computational overhead while keeping the required accuracy. Only the self-inductances and self-capacitances and resistances are scaled. The mutual inductance and mutual capacitance ratios need not be scaled. The scaling factor of the *Lp* and *Pp* are determined by equation (2.39). i.e. the new circuit element values are scaled as

$$Rii = R_P \rightarrow R_P + \varepsilon R_P , \qquad (2.52)$$

$$Lii = L_P \rightarrow \left[\frac{L_P}{2} - \frac{\varepsilon R_P}{s} \right], \qquad (2.53)$$

$$Cii = C_P \rightarrow \left[\frac{C_P}{2} - \frac{\varepsilon R_P}{s} \right]. \qquad (2.54)$$

where ε is the scaling coefficient determined from the system matrix condition. The equivalent circuit with the scaled circuit elements is given in Fig. 2.1 where mutual ($i \neq j$) inductance couplings are represented by voltage sources V_J and capacitive couplings by current sources I_K .

2.6 Results and Discussions

The unscaled and scaled PEEC models were simulated in SPICE and compared with the full-wave solver IE3D [72] results in terms of scattering parameter magnitude and phase.

IE3D is chosen for its accuracy and efficiency in handling rectangular geometries. Also, simulation of the structure with Ansoft HFSS shows agreement with IE3D results within 1% relative magnitude and 3 degrees phase difference. The S_{21} results of the unscaled model are in good agreement within 2% of relative magnitude error and 3 degrees of relative phase error at frequency range of 1 to 10 GHz as shown in Figs. 2.5, 2.6 and 2.7. But S_{11} results of unscaled model have errors as high as 34% in magnitude and 46 degrees in phase as shown in Fig. 2.8, and Tables 2.1 and 2.2. S_{11} results of the scaled model are in good agreement at high frequencies over 5 GHz as shown in Figs. 2.9 and 2.10.
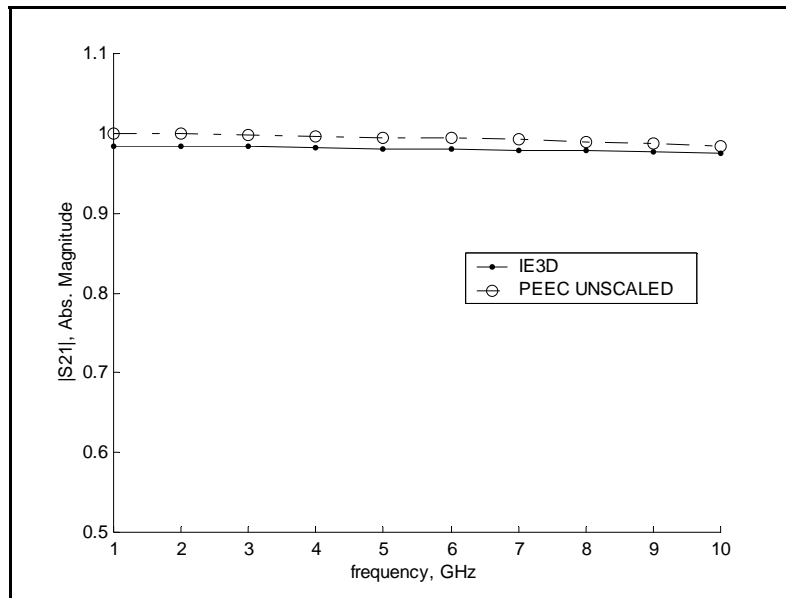
Fig. 2.5: S_{21} magnitude (linear) versus frequency.

30
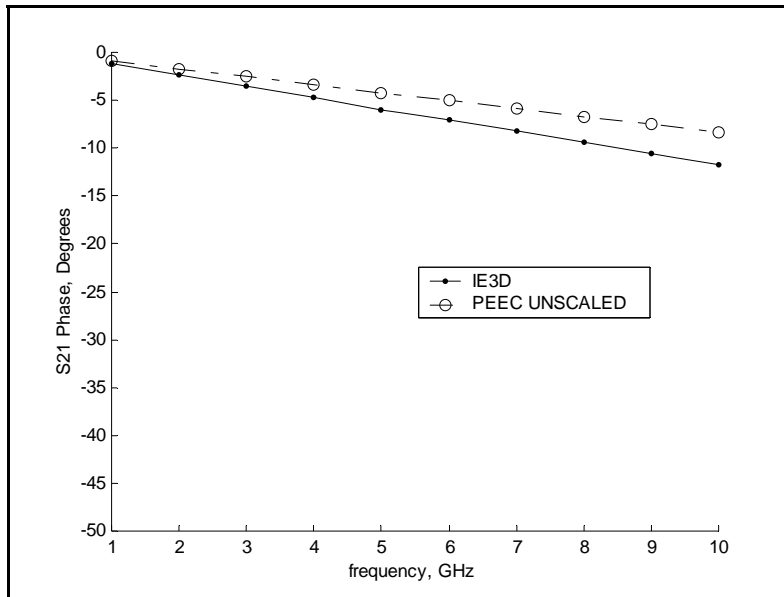
Fig. 2.6: S_{21} phase versus frequency.
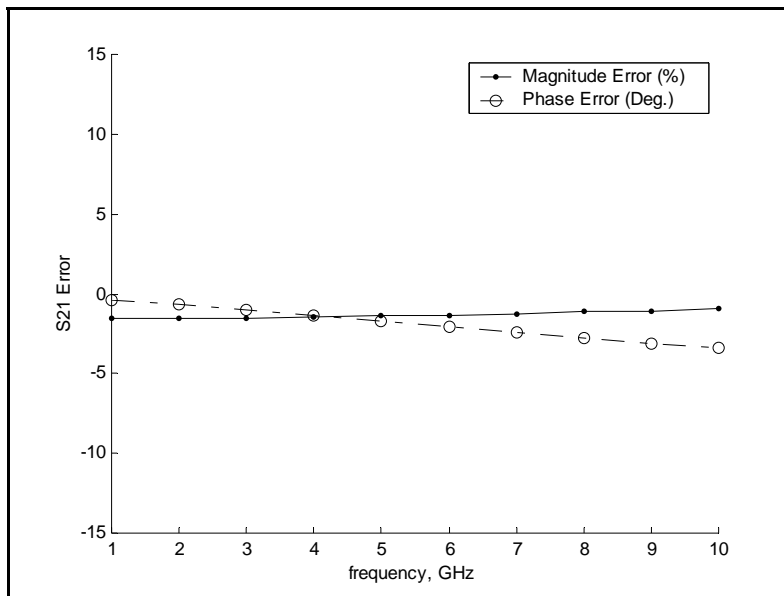
Fig. 2.7: S_{21} magnitude and phase error versus frequency

31
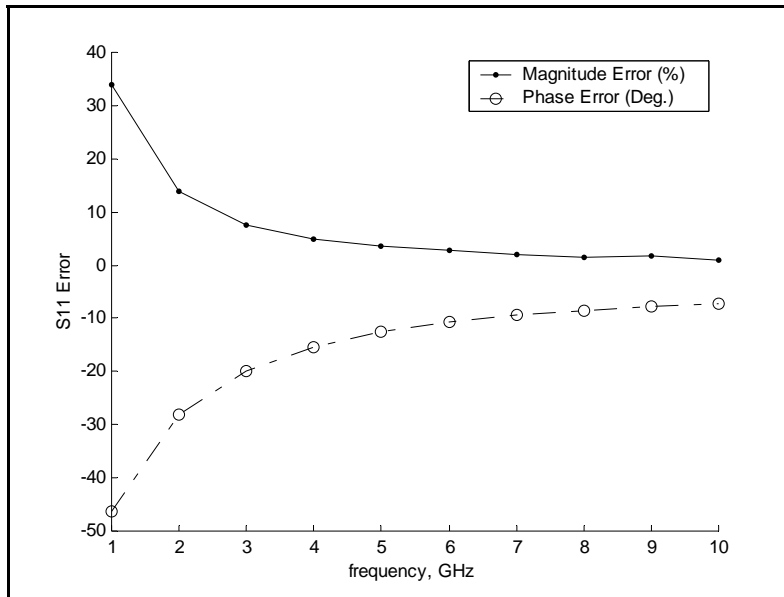
Fig. 2.8: S_{11} magnitude and phase error versus frequency

Table 2.1: S_{11} magnitude error (percentage) and Phase error (degrees).

Frequency GHz	IE3D Abs. mag	PEEC Abs. mag	IE3D Angle Degrees	PEEC Angle Degrees	Mag. Error Rel. (%)	Phase Error Degrees
1.00E+00	2.17E-02	1.44E-02	4.13E+01	8.76E+01	3.38E+01	-4.63E+01
2.00E+00	3.34E-02	2.88E-02	5.90E+01	8.72E+01	1.38E+01	-2.82E+01
3.00E+00	4.67E-02	4.32E-02	6.64E+01	8.63E+01	7.55E+00	-1.99E+01
4.00E+00	6.05E-02	5.75E-02	7.00E+01	8.54E+01	5.00E+00	-1.54E+01
5.00E+00	7.45E-02	7.18E-02	7.18E+01	8.44E+01	3.57E+00	-1.26E+01
6.00E+00	8.84E-02	8.59E-02	7.26E+01	8.34E+01	2.79E+00	-1.08E+01
7.00E+00	1.02E-01	1.00E-01	7.29E+01	8.24E+01	2.11E+00	-9.48E+00
8.00E+00	1.16E-01	1.14E-01	7.29E+01	8.14E+01	1.53E+00	-8.51E+00
9.00E+00	1.29E-01	1.27E-01	7.26E+01	8.04E+01	1.69E+00	-7.78E+00
1.00E+01	1.42E-01	1.41E-01	7.22E+01	7.94E+01	9.40E-01	-7.21E+00

Table 2.2: S_{21} magnitude error (percentage) and Phase error (degrees).

Frequency GHz	IE3D Abs. mag	PEEC Abs. mag	IE3D Angle Degrees	PEEC Angle Degrees	Mag.Error Rel. (%)	Phase Error Degrees
1.00E+00	9.84E-01	9.99E-01	-1.19E+00	-8.40E-01	-1.54E+00	-3.53E-01
2.00E+00	9.84E-01	9.99E-01	-2.39E+00	-1.69E+00	-1.57E+00	-6.96E-01
3.00E+00	9.83E-01	9.98E-01	-3.57E+00	-2.53E+00	-1.52E+00	-1.04E+00
4.00E+00	9.82E-01	9.97E-01	-4.76E+00	-3.37E+00	-1.49E+00	-1.39E+00
5.00E+00	9.81E-01	9.95E-01	-5.94E+00	-4.21E+00	-1.38E+00	-1.73E+00
6.00E+00	9.80E-01	9.94E-01	-7.11E+00	-5.04E+00	-1.38E+00	-2.07E+00
7.00E+00	9.79E-01	9.92E-01	-8.27E+00	-5.86E+00	-1.31E+00	-2.41E+00
8.00E+00	9.78E-01	9.89E-01	-9.43E+00	-6.68E+00	-1.14E+00	-2.75E+00
9.00E+00	9.76E-01	9.87E-01	-1.06E+01	-7.49E+00	-1.10E+00	-3.08E+00
1.00E+01	9.75E-01	9.84E-01	-1.17E+01	-8.30E+00	-9.64E-01	-3.40E+00
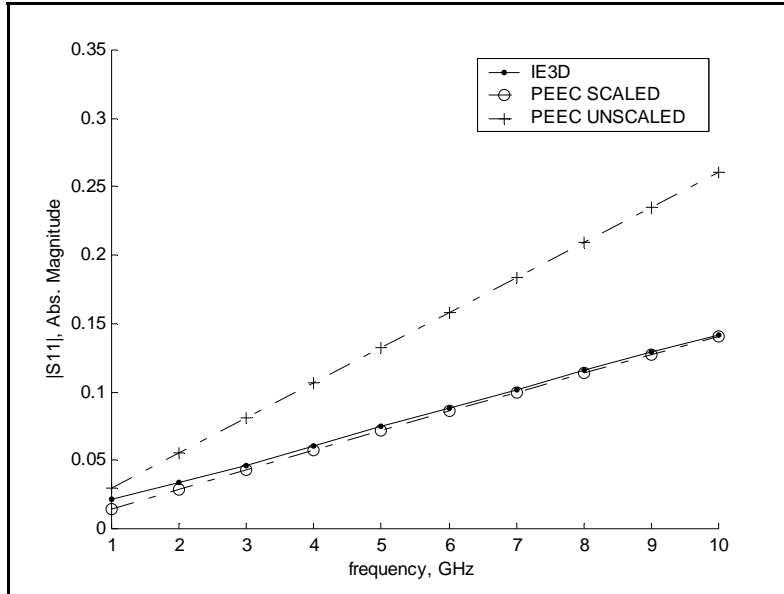
Fig. 2.9: S_{11} magnitude (linear) versus frequency
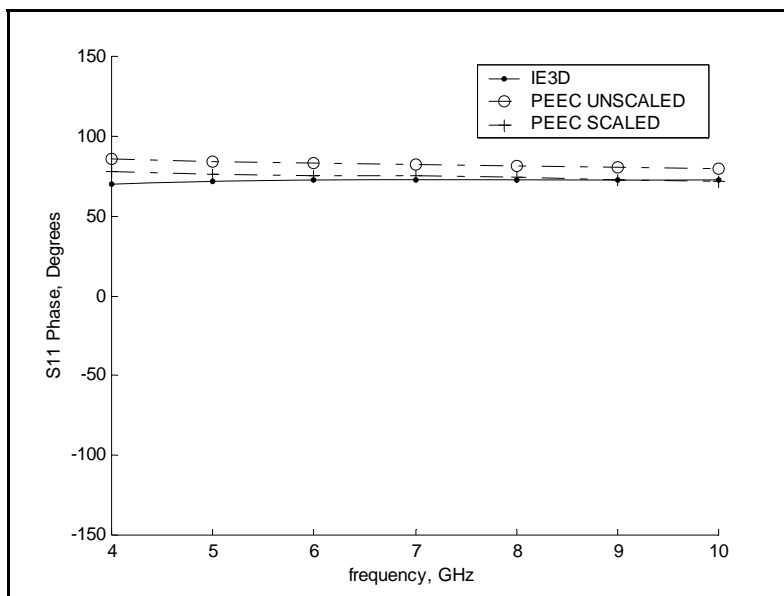
Fig. 2.10: S_{11} phase (degree) versus frequency.

The magnitude errors were less than 4% for S_{11}. Phase errors were better than 10 degrees

for S_{11} in the frequency range of 5 to 10 GHz. Without scaling the PEEC model, the

magnitude errors were higher by one order or more for S_{11} (Fig. 2.5). This is due to the

effect of small eigenvalues getting masked out by the large ones. Matrix scaling projects

all the eigenvalues onto a circle [73]. This improves the condition of the system matrix.

The solution error given by equation (2.48) is plotted against scaling coefficient ε for

different matrix conditions in Fig. 2.11. It is seen from the plot that appropriate choice of

scaling significantly reduces error for the system with large matrix condition. The matrix

condition determines the choice of coefficient ε for the given solution error.
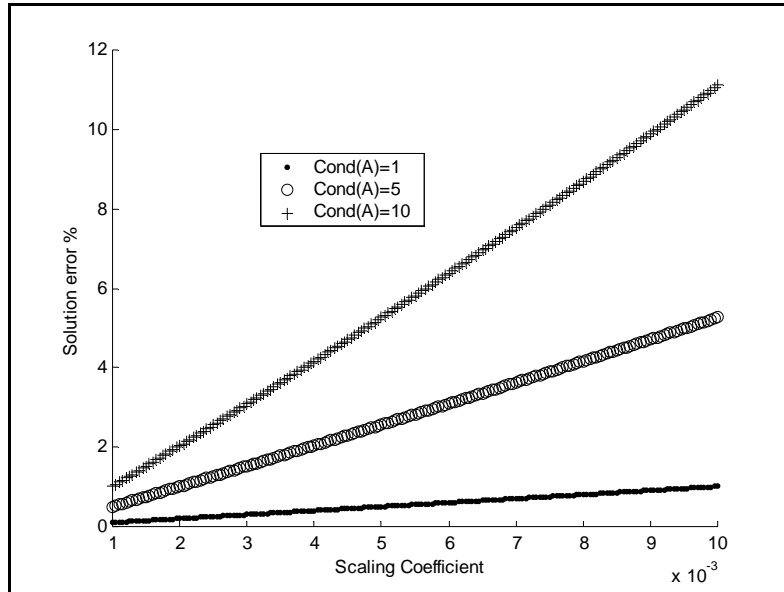
Fig. 2.11: Scaling coefficient versus solution error.

The sensitivity S_ε of the solution to the coefficient ε that forms matrix $\mathbf{E}$ is obtained by differentiation of equation (2.48) as

$$S_\varepsilon = \sum_{n=1}^{\infty} n \left[Cond(\mathbf{A}) \right]^n \left[\frac{\|\mathbf{E}\|}{\|\mathbf{A}\|} \right]^{n-1}. \tag{2.55}$$

It is to be noted that the above series (2.55) is convergent only if equation (2.47) is satisfied. The sensitivity is plotted against the scaling coefficient for various values of matrix condition in Fig. 2.12. It may be noted that there is greater sensitivity for systems with larger matrix condition $Cond(\mathbf{A})$.
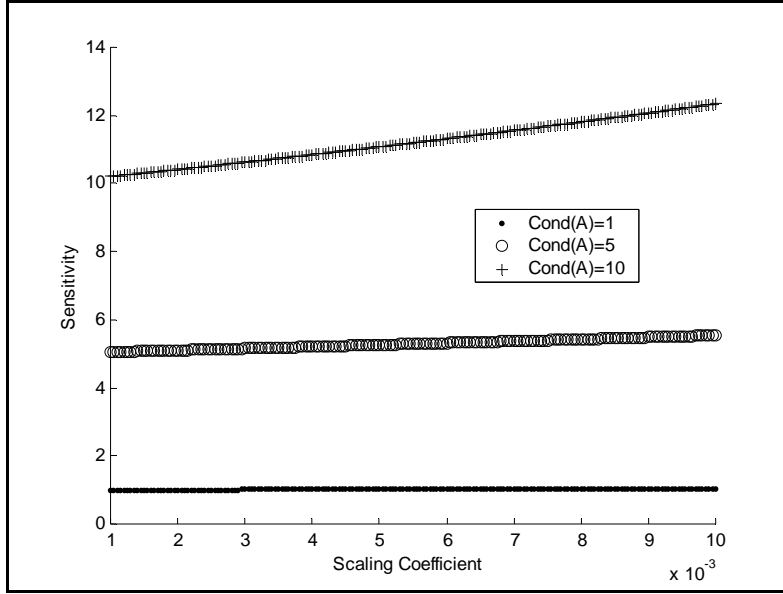
Fig. 2.12: Scaling coefficient versus sensitivity.

The usefulness of the present technique is demonstrated by the improved accuracy in the prediction of scattering parameters at high frequencies through SPICE simulation of the PEEC model of the stripline structure. Inclusion of higher order perturbation terms is expected to further enhance the accuracy of asymptotic convergence.

Table 2.3: Number of terms versus convergence error of BCHD series

Number of successive terms	Convergence Error % (large signal approximation)	Convergence Error % (small signal approximation)
1	63.212	86.466
2	26.424	45.866
3	8.030	15.415
4	1.899	3.762
5	0.366	0.731

The matrix exponential product series given by equation (2.32) is approximated with equation (2.35). The convergence of the series is tested by comparing the results obtained from the addition of an increasing number of terms. As shown in the Table 2.3, the use of 5 terms results in convergence error to be better than 1%, for both large signal and small signal approximations. Less than 5 terms lead to deviation in convergence error between the large and small signal cases. Our approximation as per equation (2.35) uses 3 terms only and is responsible for the observed phase error deviation in small signals at low frequencies. The phase error could be reduced by the inclusion of higher order terms and more accurate 3D extraction of component values.

CHAPTER 3

PEEC AND LUMPED CIRCUIT MODELING OF HOMOGENEOUS LOSSY MEDIA

3.1 Introduction

While PEEC modeling in homogeneous lossless substrates was the focus of Chapter 2, this Chapter extends the PEEC model to lossy silicon substrates. The loss due to eddy currents in the silicon substrate is taken into account by applying the theory of complex images [74]. The PEEC model is verified with an accurate lumped circuit model which is extracted from S parameter measurements. The measurement based modeling approach is useful especially when we encounter material inhomogeneity and geometric discontinuity in the fine pitch structures which are difficult to model.

3.2 PEEC Model Extension to Lossy Substrates

The lossy substrate is approximately represented in terms of an image plane located at a complex distance h_{eff} as shown in Fig. 3.1. The resulting [75] complex effective height is given by

$$h_{eff} = h_{ox} + \frac{1-j}{2}\delta \tanh\left[\frac{(1+j)h_{si}}{\delta}\right] \tag{3.1}$$

where h_{ox} is the oxide thickness, h_{si} is the thickness of bulk silicon and $\delta = 1/\sqrt{\pi f \mu_0 \sigma}$ is the skin depth of bulk silicon. The image ground plane at the effective height is used for extracting the partial mutual inductances and capacitances as explained in Chapter 2.
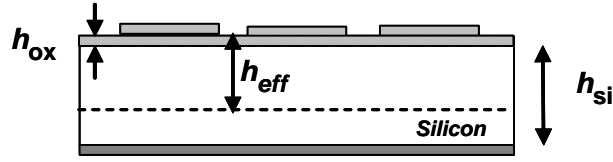
Fig. 3.1: Image ground plane for a coplanar transmission line on a lossy silicon substrate

The shunt conductance *Gxx* in the silicon substrate is determined using the relaxation time constant as [75]

$$Gxx = \frac{\sigma_{si}}{\varepsilon_{si}} Cxx \qquad (3.2)$$

where σ_{si}, ε_{si} and *Cxx* are silicon conductivity, permittivity and capacitance respectively. The oxide formation on the test samples is considered negligible in the PEEC model. PEEC representation for conductors on lossy substrates through the use of shunt conductance is a contribution made in this thesis and is shown in Fig. 3.2. The index *xx* in *Gxx* and $Cxx = 1/Pxx$ equals *ii* and *kk* for the ith node and k^{th} node in the Fig. 3.2 respectively. Transmission line on lossy substrate is represented by lossless substrate with virtual ground plane at effective height given by (3.1). Only real inductors and capacitors are used. Shunt admittance is implemented with equivalent *R* and *C* elements where

$$R = \frac{Gxx}{Gxx^2 + B^2}, \qquad (3.2a)$$

$$C = \frac{\omega B}{Gxx^2 + B^2} \qquad (3.2b)$$

and $B = \omega Cxx$.
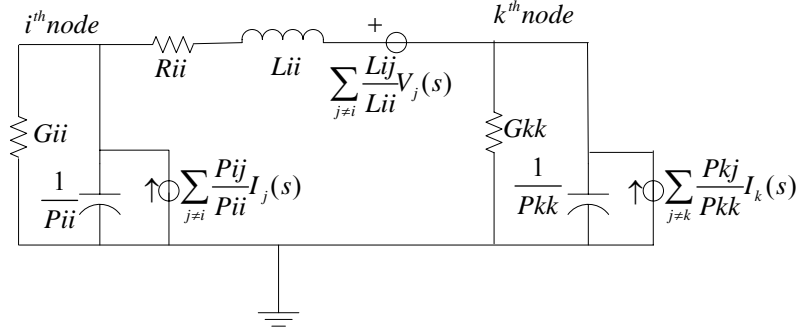
Fig. 3.2: PEEC model of transmission line on lossy substrate

3.3 Lumped Circuit Model in Lossy Substrates

The measurement based lumped circuit models are quite efficient in representing the parasitics in small geometries. A lot of work [76]-[77] has been done in the equivalent circuit representation of regular pad structures. An alternative method is described in this section to derive an equivalent circuit model that represents the pad over a wide operating frequency range of 1GHz to 20GHz. We apply the method to a square pad structure, built with 50 ohm transmission line on high resistivity silicon. Two port ABCD matrices of two transmission lines of different lengths are used to derive the model. The model is optimized and validated using circuit simulation by comparing the simulated results with measurements.

Reference [77] uses the stray capacitances alone to model pad parasitics and so it becomes easier to use simple shunt admittances for modeling end effects. But when we include the inductance and the discontinuities, the pi model of the circuit becomes too complex in the sense that the admittance matrix parameters of the pad geometry cannot be extracted. As a workaround, we propose to use two port ABCD matrices which have properties similar to that of wave cascade matrices (WCM) described in [78]. The analytical equations are simplified by making use of two transmission lines that differ in

40

lengths by a factor of 2. This makes cascading and inversion of the resultant matrix simpler. The discontinuity and lead length effects are combined into a single inductor as shown in Fig. 3.2. The inclusion of the inductor along with stray capacitances represents the high frequency effects accurately in the modeling of complex pad geometries. We demonstrate the method using square pad structures that are connected by transmission lines to arrive at an equivalent circuit that represents the pad geometry over the frequency range of 1 GHz to 20 GHz. The methodology of using congruent symmetric circuit representation for pads along with two transmission lines that differ in length by a factor of 2, is a contribution of this thesis. This results in simplification of ABCD matrix representation and hence reduced computation effort.

3.3.1 Equivalent Circuit Description

The layout and equivalent circuit of a pad test structure are shown in Fig. 3.3a. Two square pads of size $75\mu m \times 75\mu m$ are connected by a transmission line. There are two transmission line structures of same shape but with different lengths. One of the transmission lines has a length of about 700um and the other has twice the length. Each structure can be characterized as a coplanar waveguide [79], [80] with two-port frequency domain measurements. The inductance effect of the pad is also taken into account in order to allow for lumped element modeling up to 20GHz. In Fig. 3.3a, transmission line (TX) is connected to pads which are represented by C_P, the oxide capacitance coupling, C_S the substrate induced capacitance coupling and R_S the resistive losses due to substrate and L_d is the discontinuity and pad inductance combined. The

presence of L_d helps to account for the magnetically coupled losses more accurately. The

transmission line is represented by the standard RLCG network.

3.3.2 Modeling Methodology

The modeling approach adopted for this work is shown in the flowchart of Fig. 3.3b.
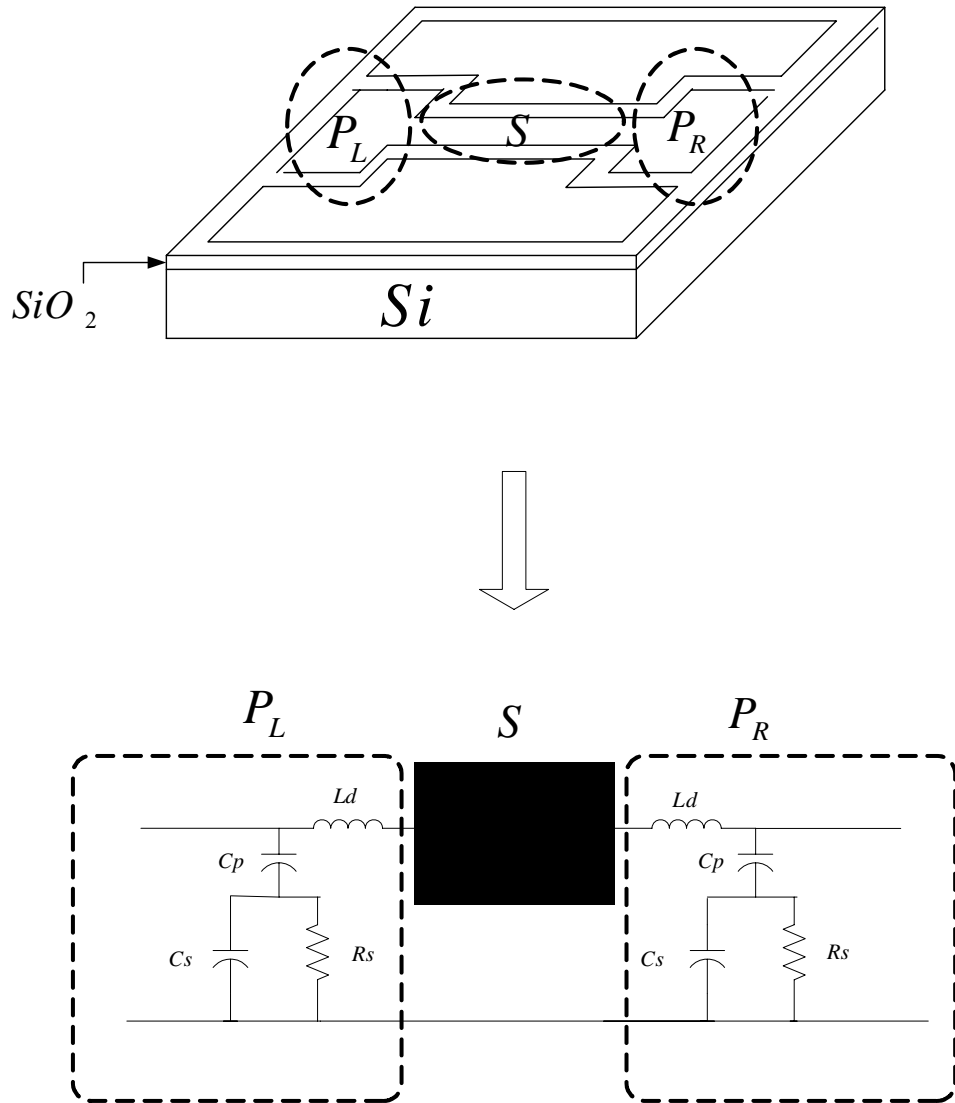
(a)
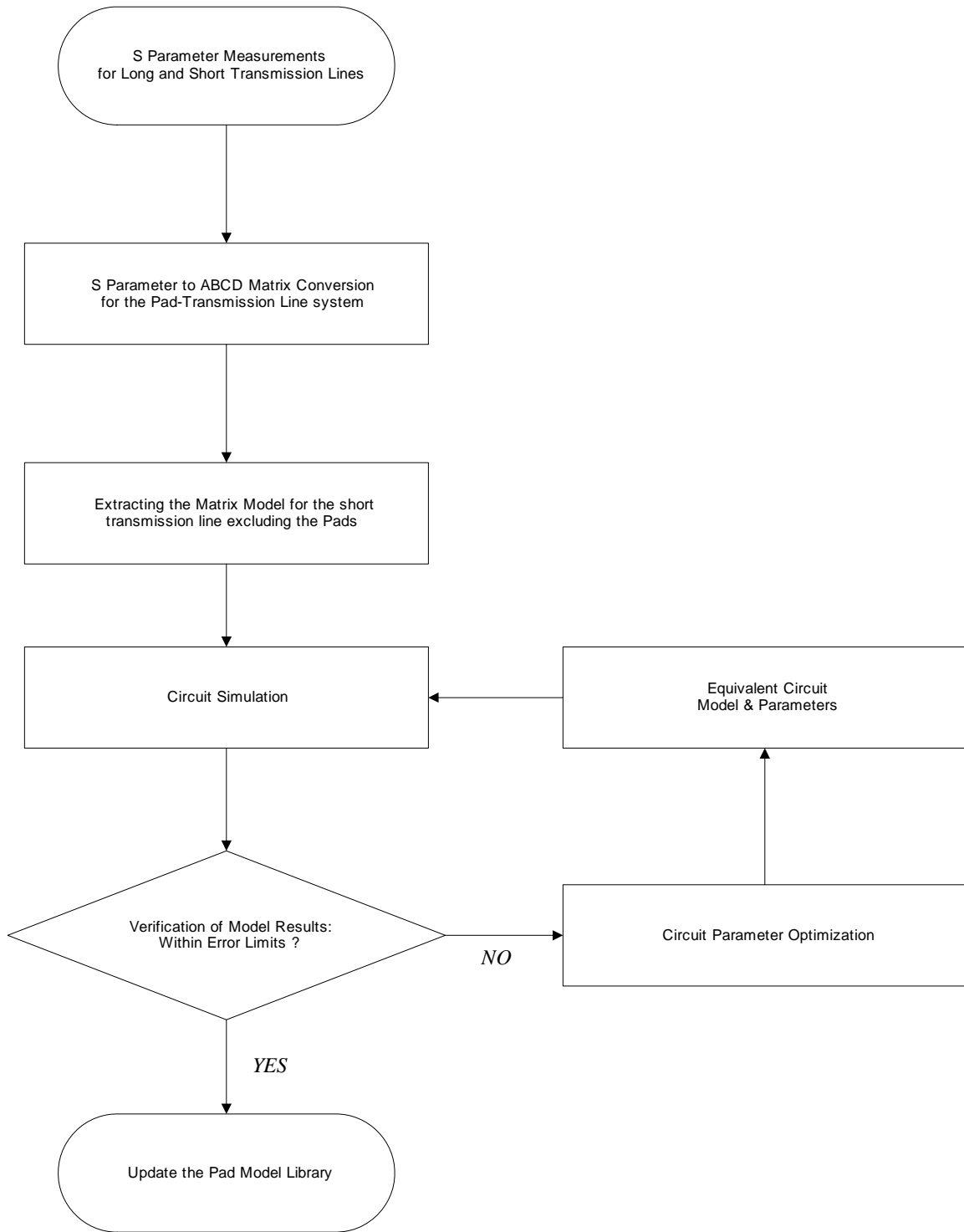
(b)

Fig. 3.3: (a) Equivalent circuit and (b) flowchart showing the lump model approach

The two port matrices for the long transmission line (A_L) and short transmission line (A_S) are

$$A_L = P_L L P_R, \tag{3.3}$$

$$A_S = P_L S P_R, \tag{3.4}$$

where P_L, P_R, L and S are the ABCD matrices [81]-[82] of the left pad, right pad, long transmission line and short transmission line respectively. It is assumed that P_L and P_R is congruent to each other due to the reflection symmetry between them.

The matrix division of long line over short line, from equations (3.3) and (3.4) is

$$A_L A_S^{-1} = P_L L P_R P_R^{-1} S^{-1} P_L^{-1} = P_L L S^{-1} P_L^{-1}. \tag{3.5}$$

Since the long line has twice the length of the short line, we have $L = S \times S$ which simplifies the short line simulation model matrix and hence equation (3.5) to

$$A_L A_S^{-1} = P_L S P_L^{-1}. \tag{3.6}$$

Since $tr(P_L S P_L^{-1}) = tr(S)$ where tr is the trace of the matrix and $P_L S P_L^{-1}$ and S are similar. So we could use $P_L S P_L^{-1}$ to represent the short transmission line (excluding pads) for optimization of pad circuit elements.

3.3.3 Minimizing the Residual Trace Function

Circuit parameter optimization is performed by minimizing the function R of the residual trace as

$$R = \sum_{k=1}^{N} \left| 1 - \frac{\text{Re}\{tr(P_L A_L A_S^{-1} P_R)_k\}}{\text{Re}\{tr(A_S)_k\}} \right|^2 + \sum_{k=1}^{N} \left| 1 - \frac{\text{Im}\{tr(P_L A_L A_S^{-1} P_R)_k\}}{\text{Im}\{tr(A_S)_k\}} \right|^2. \tag{3.7}$$

where $\operatorname{Re}\{tr(.)_k\}$ and $\operatorname{Im}\{tr(.)_k\}$ are the real and imaginary parts of $tr(.)_k$. In expression (3.7), the right pad matrix is, by symmetry, represented in terms of left pad matrix elements. i.e.,

$$P_R = \begin{pmatrix} P_L(2,2) & P_L(1,2) \\ P_L(2,1) & P_L(1,1) \end{pmatrix},$$
(3.8)

and N is the number of frequency points.

The derivation of optimization minimum and its convergence and noise sensitivity properties are found in [83] and Appendix F.

3.4 Results and Discussions

The S-parameter measurements are performed twice with two different transmission line lengths. Coplanar probes of pitch 150 micrometer from Cascade Microtech were used for the S parameter measurements. SOLT (short-open-load-through) calibration [84] of the probes is performed prior to actual measurements. 201 test points were selected over a frequency range of 1 to 20 Gigahertz. Continuous wave RF power level of -15 dBm was used. The measurement setup used is shown in Fig. 3.4.

Both the PEEC model and the lumped circuit model are compared with the measured results as shown in Figs. 3.5 - 3.8. For the lumped model, we used the search range of 0.001 to 1000 units for capacitance (in pF), inductances (in pH) and resistance (in ohms). The typical parameters obtained, with error tolerance of 5% in S_{12} and S_{21}, for the 75 X 75   pad geometry were Ld= 170pH, Cs=1.23pF, Rs=187 ohm and Cp=75pF. Evidently, the equivalent circuit model derived represents the pad geometry better over a wide operating frequency range of up to 20GHz within the tolerance of 5% of the

measured S_{21} values. PEEC model results are within 7% relative error from the measurements.
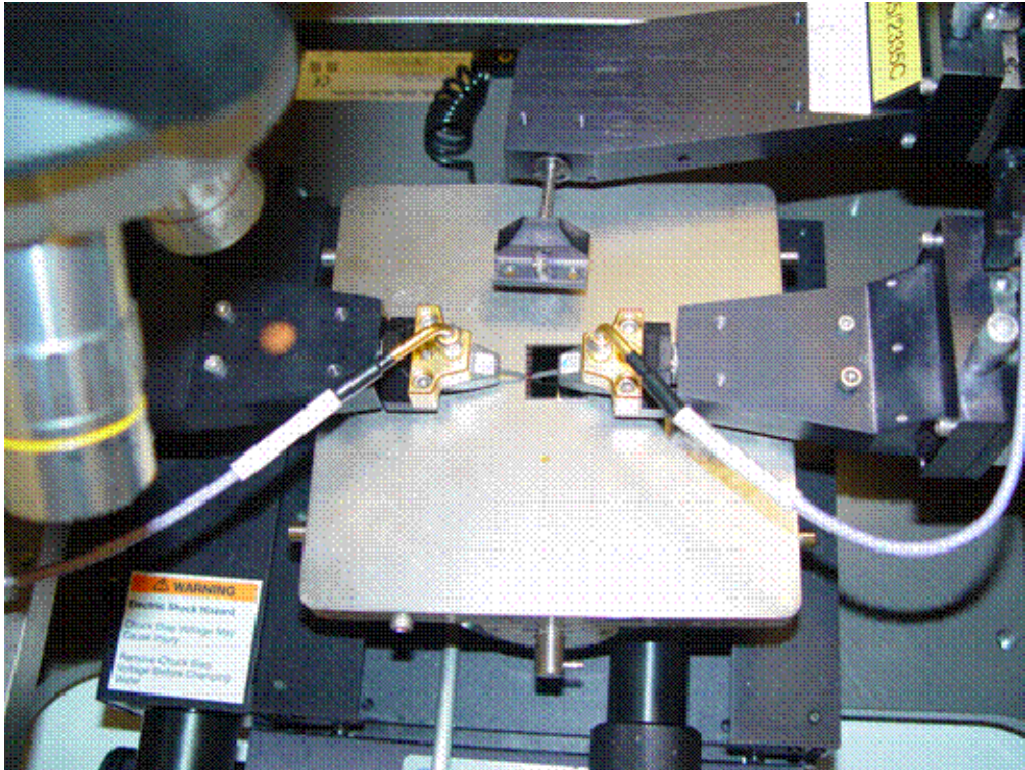
Fig. 3.4: Measurement setup
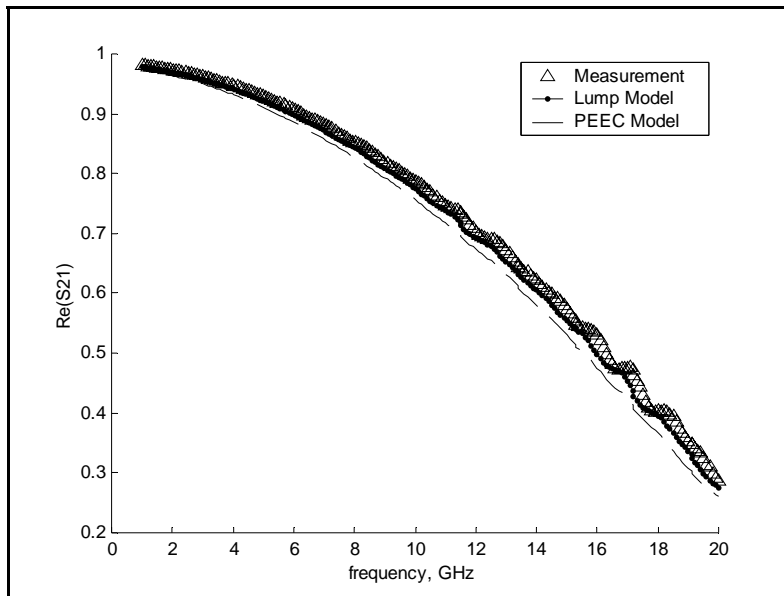
Fig. 3.5: Re(S_{21}) measurement versus simulation.
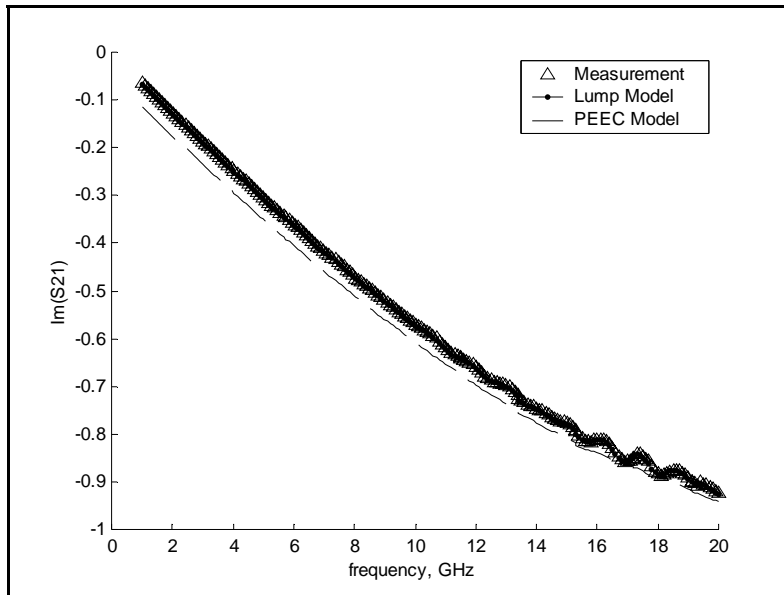
Fig. 3.6: Im(S$_{21}$) measurement versus simulation.
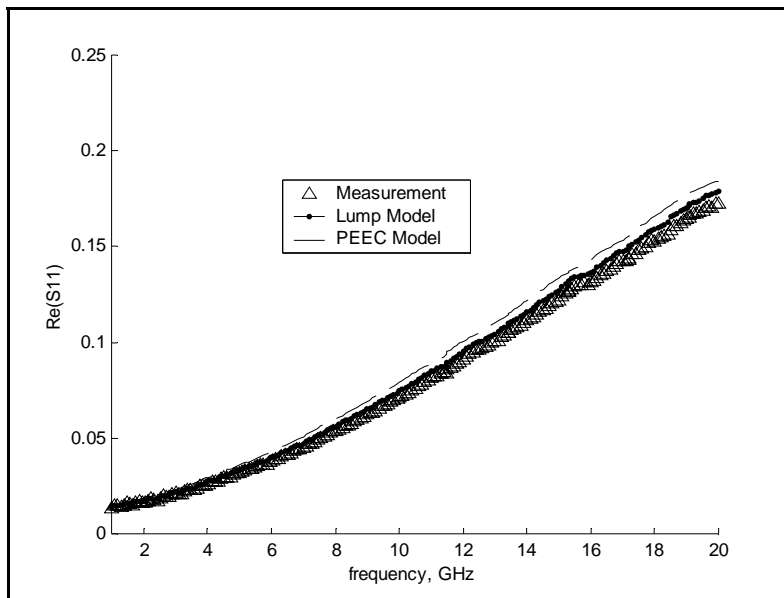
Fig. 3.7: Re(S$_{11}$) measurement versus simulation.

47
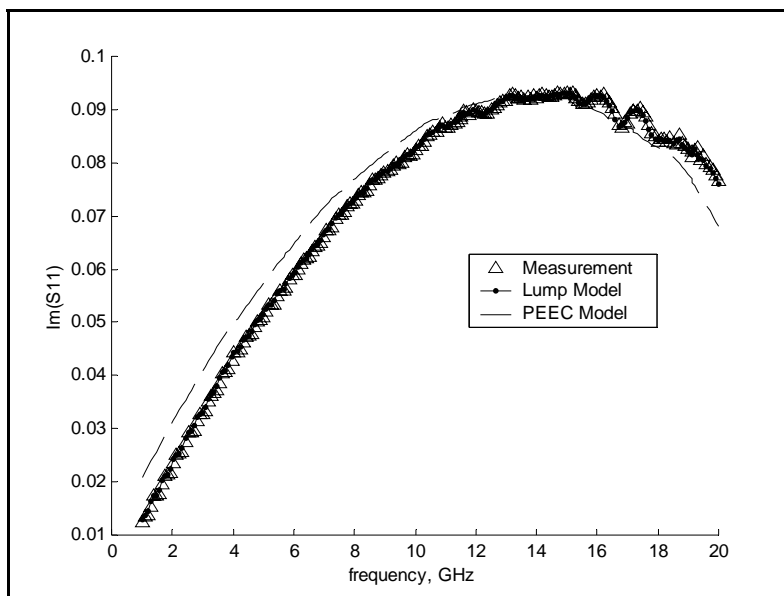
Fig. 3.8: Im(S_{11}) measurement versus simulation.

To summarize, PEEC model has been extended to lossy substrates and a measurement based method for lumped circuit modeling of pad geometries has been described in this Chapter. Theory of complex images is used to derive PEEC model. Two port ABCD matrices of two transmission lines of different lengths are used to derive the lump model. The models were applied to a coplanar structure with square pads and the equivalent circuit models derived represents the pad geometry on a silicon substrate over a wide operating frequency range of up to 20GHz. Both PEEC and measurement based lumped circuit models have been found to work well in representation of lossy silicon substrates. Measurement based lumped model is an alternative approach when handling objects, with material inhomogeneity and geometric complexity, that are difficult to model with PEEC. One limitation of the lumped model approach is that the initial values, though physical knowledge of material and layout sizes does help to make good initial guess, are the main key to fast convergence.

48

CHAPTER 4

PEEC MODELING OF MULTICONDUCTOR SYSTEM WITH DIELECTRIC MESH

4.1 Introduction

Equivalent circuit modeling of homogeneous medium geometries employing the Green's function and scattering parameter measurements have been derived in the Chapters 2 and 3 respectively. The objective of this Chapter is to describe PEEC model in a dielectric mesh medium with metallization. Dielectric meshes are specifically considered for modeling due to their importance as probes in WLP test. Naturally occurring homogeneous dielectric materials may not be suitable for the test application because of a compliance limitation. But, synthesis of materials with unique geometry such as mesh or composite / artificial dielectrics lead to systems that respond to electromagnetic excitation in the same way as the desired material but without specific limitation.

As an early example of the synthetic approach to solving material limitations in electromagnetics, Kock [85, pp. 3-5] suggested to make a dielectric lens lighter in weight by replacing the refractive material by a mixture of metal spheres in a matrix. Thus, the first light weight lenses were built by spraying conducting paint on polystyrene foam and cellophane sheets. The large polarizability effect of the metal inclusions adds to the electrical response of the neutral matrix to result in an increase in effective permittivity. Another example involves polar liquid mixtures where the calculation of local field that excites a given inclusion by Clausius-Mosotti formulation [85, p. 9] and its subsequent

refinement by Lars Onsager [85, pp. 9-11]. The refinement comes about by adding a reaction field which is a self-interaction of dipole moment of the inclusion itself through the surrounding polarization. The singularity of the reaction field is avoided by considering that the field is parallel to the source dipole moment. So, the reaction field does not affect its source but only the surrounding polarization.

This Chapter is organized as follows. Section 2 describes the probing considerations in testing high density I/O wafer level packages that necessitate the use of dielectric mesh type material as probe substrates. It deals with the process, geometrical and material aspects involved in the construction of prototype test probe for optimum electromagnetic performance. PEEC modeling of the elastomer probe made of metal-dielectric mixture is discussed in section 3. A coplanar probe is used as a test prototype for the PEEC modeling, simulation and for measurement in section 4. The numerical results are first compared and found to give good agreement in terms of insertion loss and return loss.

4.2 Probing Considerations for WLP Test : Relevance of Dielectric Mesh

Contact problems are a major concern in wafer level testing especially at high frequencies. Good electrical contact and low probe parasitics are much sought after objectives to keep test quality and yield high. While the electrical constraints need to be met, the proliferation of I/O density in the current generation of application specific integrated circuits (ASIC) requires the probes to be vertically compliant, much smaller and placed at closer pitch as well.

Cantilever probes have been traditionally used for wafer testing. They are only useful for low frequency applications of about 100MHz due to long lead inductances Coaxial probes are available with multi-GHz performance for pitches as small as 120 micron and have been used for probing devices with solder bumps. The limit on scaling down to finer pitch makes the coaxial cable not usable as a test probe for high I/O density packages. Compliant probes for SoL (sea of leads) technology[86], while scaling down to lower pitches, are yet to be proven robust against problems of high contact resistance. MEMS probe [87] holds some promise but for the challenges in fabrication.

Though the above solutions are good for low pin count device measurements, there is an obvious need for compliant, finer pitch, densely packed probes for testing area array, high I/O density packages. This need has been addressed in this study by metallization of coplanar structures on an elastomer base material. Elastic property of the substrate provides the required compliance to take up thickness variations on the wafer and also maintains good electrical contact.

Coplanar line is chosen as a test structure since it is known to be the most commonly used configuration for a probe [79], [88]-[89], for efficient transition of high frequency signals onto and off a wafer or chip. It helps to transform the transverse electric or transverse magnetic (TE or TM) modes of a waveguide or coaxial cable into TEM mode of microstrip or CPW lines commonly encountered in the wafer while also matching the characteristic impedances between the two transmission media. The conventional circuit theory deals only with the impedance matching issues, whereas the PEEC based model provides scope for addressing impedance matching as well as mode matching (accounted by the inductive and capacitive coupling interactions).

The elastomer probe is made of metal particle suspension on an elastomer base. The metallization lines are screen printed on the trampoline (Figs. 4.1 - 4.2). The ability to fabricate small features with the approaches that are used for silicon processing helps to deposit metal lines with the resolution of 40 micron line width and 100 micron pitch. The metal particles are absorbed throughout the thickness of the elastomer. This makes the mesh layer look like a double sided PCB without vias. The absence of vias makes this probe ideal for high frequency signal transmission.
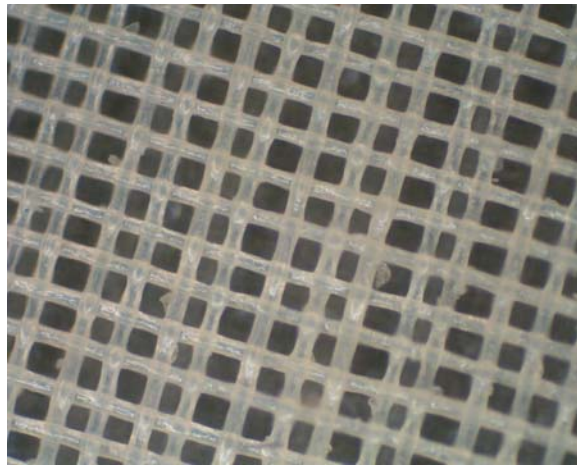
Fig. 4.1: Elastomer dielectric mesh without metallization
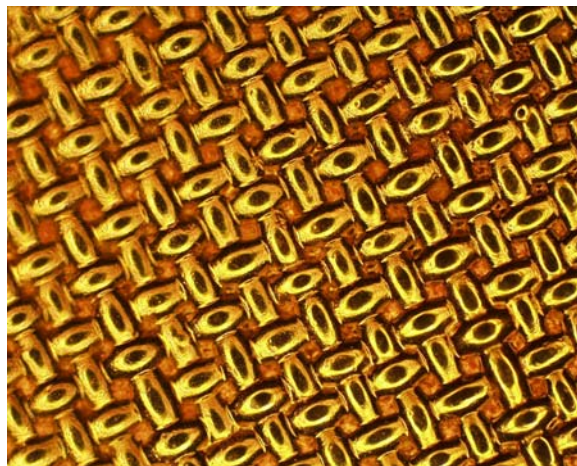
Fig. 4.2: Elastomer dielectric mesh with metallization

4.3 PEEC Modeling for Elastomer Dielectric Mesh

Usually free space homogeneous Green's function kernel is used for extraction of partial inductances and coefficient of potentials. But in the case of elastomer dielectric mesh, it is necessary to adapt the homogeneous Green's function based EFIE to account for the mixture of metallic particles and polymer material. The equivalent circuit for the mixture is constructed by considering the conduction current and displacement current through separate partial inductors. Otherwise the capacitances and resistances are treated as in standard PEEC model. The mixture of metal particles and the dielectric material means that the additional polarization effect on charges and currents inside the metallic inclusion due to dielectric mesh must be included to the homogeneous EFIE in order to compute the fields. This amounts to perturbation of the local electric field in the metal by the polarization vector by an amount that depends on the material permittivity and composition of the mixture. Considering the metal particle to be surrounded by dielectric in a spherical (or cubic) symmetry, the effective local field could be represented, for isotropic material, as

$$\mathbf{E} = \mathbf{E}_0 + \mathbf{E}_P = \mathbf{E}_0 + \frac{\mathbf{P}}{3\varepsilon_0} \,. \tag{4.1}$$

The factor $\dfrac{1}{3\varepsilon_0}$ in the second term of equation (4.1) comes from the electric field due to polarization [90] of the neighboring dielectrics. The amplitude of the external average field is thus increased by an additional contribution from the surrounding polarization [85].

53
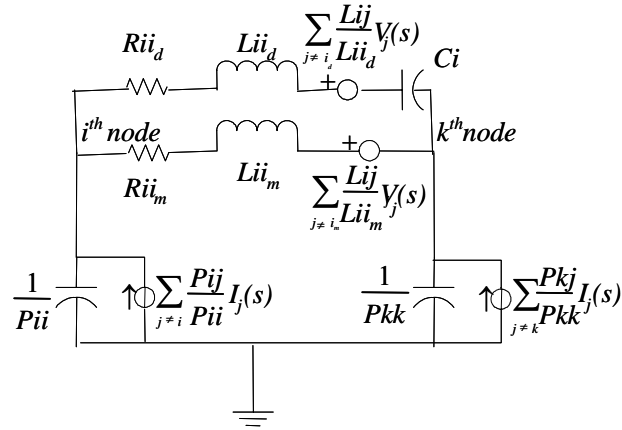
Fig. 4.3: PEEC model of a dielectric mesh cell with metallic inclusion

The static approximation (4.1) is valid for oscillatory cases when the wavelength is much longer than the spacing between metallic inclusions. Thus the equation (4.1) accounts for the fields produced by the dielectric medium with the metallic particle inclusions.

The PEEC model for the case of homogeneous dielectrics [91] is treated by adding and subtracting the displacement current from the Maxwell's equation as represented by (2.13) so that the polarization current due to the dielectrics is combined with conductor current to represent inductive elements.

It is noted from the Maxwell's equation applied to dielectrics that

$$\nabla \cdot \left(\varepsilon_0 \mathbf{E} + \mathbf{P} \right) = 0 , \tag{4.2}$$

where the polarization vector is included into the free space divergence term such that

$$\mathbf{P} = \varepsilon_0 (\varepsilon_r - 1)\mathbf{E} . \tag{4.3}$$

In view of equation (4.1), the total electric field is split into two parts. Accordingly the equation (4.3) evolves into equation (4.4) with two terms, the first term being the contribution from the bulk dielectric and the second term from the metal inclusion.

$$\mathbf{P} = \varepsilon_0(\varepsilon_r - 1)\mathbf{E}_0 + \varepsilon_0(\varepsilon_e - 1)\mathbf{E}_P, \tag{4.4}$$

where ε_r is the relative permittivity of the bulk dielectric and ε_e is the effective permittivity of dielectric with metal inclusion.

The Maxwell equation (2.13) is then modified to

$$\nabla \times \mathbf{H} = \mathbf{J}_C + \varepsilon_0(\varepsilon_r - 1)\frac{\partial \mathbf{E}_0}{\partial t} + \varepsilon_0(\varepsilon_e - 1)\frac{\partial \mathbf{E}_P}{\partial t} + \varepsilon_0 \frac{\partial \mathbf{E}}{\partial t}. \tag{4.5}$$

With this correction, the total current in the metal-dielectric mixture is given by

$$\mathbf{J}(\mathbf{r},t) = \mathbf{J}_C(\mathbf{r},t) + \varepsilon_0(\varepsilon_r - 1)\frac{\partial \mathbf{E}_0}{\partial t} + \varepsilon_0(\varepsilon_e - 1)\frac{\partial \mathbf{E}_P}{\partial t}, \tag{4.6}$$

where the approximation $\varepsilon_e = \dfrac{\varepsilon_r + 1}{2}$ is used. Equation (2.15) is then modified as

$$\frac{\mathbf{J}_C(\mathbf{r},t)}{\sigma} + \frac{\mu}{4\pi}\int_{v'} \mathbf{G}(\mathbf{r},\mathbf{r'})\left[\frac{\partial \mathbf{J}_C(\mathbf{r'},t_d)}{\partial t} + \varepsilon_0(\varepsilon_r - 1)\frac{\partial^2 \mathbf{E}_0(\mathbf{r'},t_d)}{\partial t^2} + \varepsilon_0(\varepsilon_e - 1)\frac{\partial^2 \mathbf{E}_P(\mathbf{r'},t_d)}{\partial t^2}\right]dv'$$

$$+\frac{\nabla}{4\pi\varepsilon_0}\int_{s'} \mathbf{G}(\mathbf{r},\mathbf{r'})q^T(\mathbf{r'},t_d)ds' = 0. \tag{4.7}$$

The integral equation (4.7) forms the basis of the PEEC model for metal-dielectric mixtures. The equation (4.7) which has an additional polarization term due to the metal-dielectric mesh is a main contribution of this thesis. The current derivative of the second term forms one inductor for metal object while the field derivatives form another inductor in series with capacitor between adjacent nodes for metal-dielectric mixture. When the operating frequency is of the order of relaxation time of the polarizing medium, the field derivatives need to be treated as separate inductors interacting with the corresponding time delay. The current through the second inductance path in series with capacitor becomes significant as the operating frequency increases.

Fig. 4.3 shows the equivalent circuit representation of metal and dielectric mixtures where the interaction is governed by the mutual inductances as well as capacitances. The resistance element is obtained by integrating the first term in equation (4.7) as

$$\int_{v'} \frac{\mathbf{J}_C(\mathbf{r},t)}{\sigma_{ii}} dv' = R_{ii} = \frac{l_{ii}}{\sigma a_{ii}} \ , \tag{4.8}$$

where l_{ii} and a_{ii} are the cell length along the direction of current flow and cell cross sectional area perpendicular to the direction of current flow respectively.

For the metal cells, the inductance is calculated by integrating the second term of equation (4.7) as

$$L_{ijm} = \frac{\mu}{4\pi a_i a_j} \int_{v_j} \int_{v_i'} \mathbf{G}(\mathbf{r}_j,\mathbf{r}_i') dv_i' dv_j \ , \tag{4.9}$$

where a_i and a_j are the cross sectional area of the volume cell perpendicular to the direction of current flow. $i = j$ corresponds to the partial self inductance and $i \neq j$ corresponds to the partial mutual inductance. A laminar, uniform current flow through each volume cell is assumed in applying equations (4.7), (4.8) and (4.9). The inductive couplings are represented by the voltage controlled voltage source summation term

$$V_L = \sum_{j \neq i} L_{ij} \frac{\partial i_{Lj}(t-t_{dij})}{\partial t} = \sum_{j \neq i} \frac{L_{ij}}{L_{ii}} \varphi_{Lj}(t-t_{dij}) \ , \tag{4.10}$$

where φ_{Lj} is the potential across the jth inductance cell and t_{dij} is the time delay according to (2.12) between interaction among ith and jth cell. For dielectric cells, the inductance terms L_{ijd} are similar with the addition of the factor $\varepsilon_0(\varepsilon_r - 1)$. If the dielectric involves the metal inclusion, there is an additional inductance term with factor $\varepsilon_0(\varepsilon_e - 1)$.

For capacitance calculation of the surface cells, the integral expression of the last term in equation (4.7) is approximated to give partial coefficient of potential as

$$\frac{1}{4\pi\varepsilon_0}\iint\limits_{s_j\,s_i}\frac{\partial}{\partial x}\mathbf{G}(\mathbf{r}_j,\mathbf{r}_i')q^T ds_i' ds_j = \frac{1}{4\pi\varepsilon_0 a_j}\int\limits_{s_i}\left[\mathbf{G}(\mathbf{r}_{jx}+\frac{\Delta\mathbf{r}_{jx}}{2},\mathbf{r}')-\mathbf{G}(\mathbf{r}_{jx}-\frac{\Delta\mathbf{r}_{jx}}{2},\mathbf{r}')\right]Q^T ds_i'$$

$$= Q^T(P_{ij}^+ - P_{ij}^-), \tag{4.11}$$

where $\Delta\mathbf{r}_{jx}$ is the cell width in the x direction of partition and $Q^T = a_j q^T$ is the total charge of the jth cell. In general, the coefficient of potential is represented as

$$P_{ij} = \frac{1}{4\pi\varepsilon_0 a_i a_j}\iint\limits_{s_j\,s_i}\mathbf{G}(\mathbf{r}_j,\mathbf{r}_i')ds_i' ds_j, \tag{4.12}$$

The capacitive couplings are represented by the current controlled current source summation term

$$I_C = \sum_{j\neq i}\frac{P_{ij}}{P_{ii}}i_{Cj}(t-t_{dij}), \tag{4.13}$$

where i_{Cj} is the current through the jth capacitive cell. A series resistance Rii_d is added to represent a lossy dielectric. Series capacitance is obtained from

$$C_i = \frac{\varepsilon_0(\varepsilon_i-1)a_i}{l_i}, \tag{4.14}$$

where l_i and a_i are the interior dielectric cell length along current direction and cross sectional area respectively.

4.4 Numerical Example and Discussions

The schematic of an elastomer dielectric mesh structure investigated is shown in Fig. 4.4 and the physical sample is shown in Fig. 4.5. It consists of three metal lines of 60 micron

width with the spacing of 90 micron imprinted on the elastomer mesh. This coplanar transmission line is measured on HP8510C test system using GSG air coplanar probe of 150 micron pitch. The test system is calibrated by SOLT (Short, Open, Load and Through) method. Length of the transmission line is 3000 micron. Copper metallization is used for the signal as well as ground traces. The thickness of the elastomer mesh is 50 microns. The elastomer chosen has the dielectric constant and loss tangent values of 2.86 and 0.002 respectively.
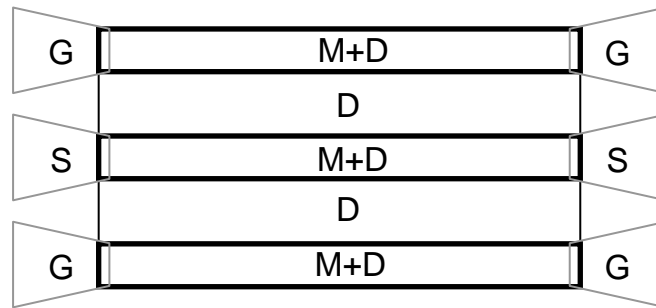
Fig. 4.4: Elastomer coplanar probe layout. M+D represents the mixture of metal and polymer mesh material. D represents the polymer mesh alone. GSG represents air coplanar probe used for VNA measurements.

The partitioning of the coplanar structure leads to partial element circuit in the form of Fig. 4.6. Only the self partial inductances are shown for clarity though couplings between inductors in same direction and between nodal capacitances are implied. Time delayed interacting current sources are represented as rectangle blocks and voltage sources are represented by circle and square blocks. The circles represent interaction among the vertical components and the squares represent interactions among the horizontal components. There are no interactions between vertical and horizontal elements since

they are orthogonal to each other. The partition cell size is chosen to be less than one tenth of the smallest wavelength in the model range.
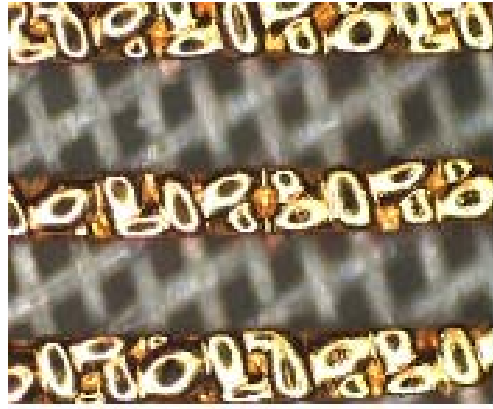
(a)

(b)

Fig. 4.5: Physical test sample of Elastomer probe (a) Top view (b) Cross-section
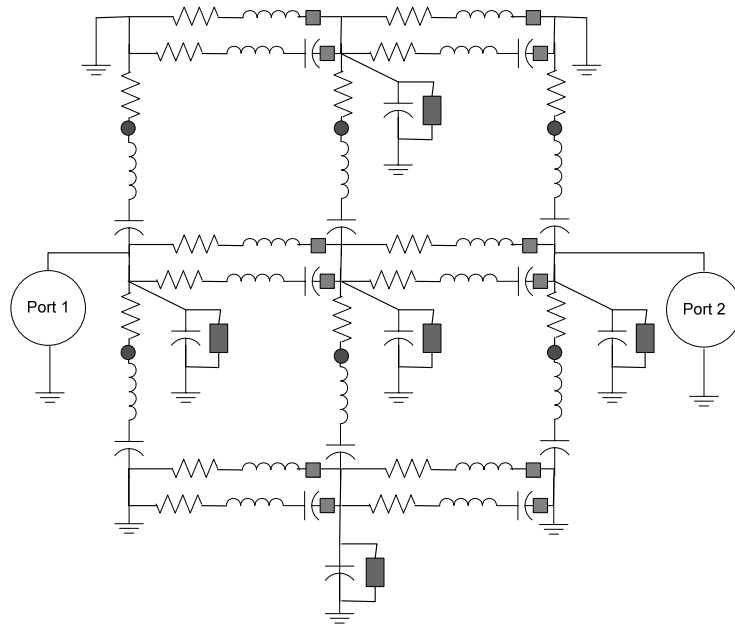
Fig. 4.6: PEEC for Elastomer mesh coplanar line

This circuit model Fig. 4.6 of the coplanar mesh sample is simulated in circuit solver SPICE and compared with the measurement results in terms of scattering parameter magnitudes S_{21} and S_{11}.
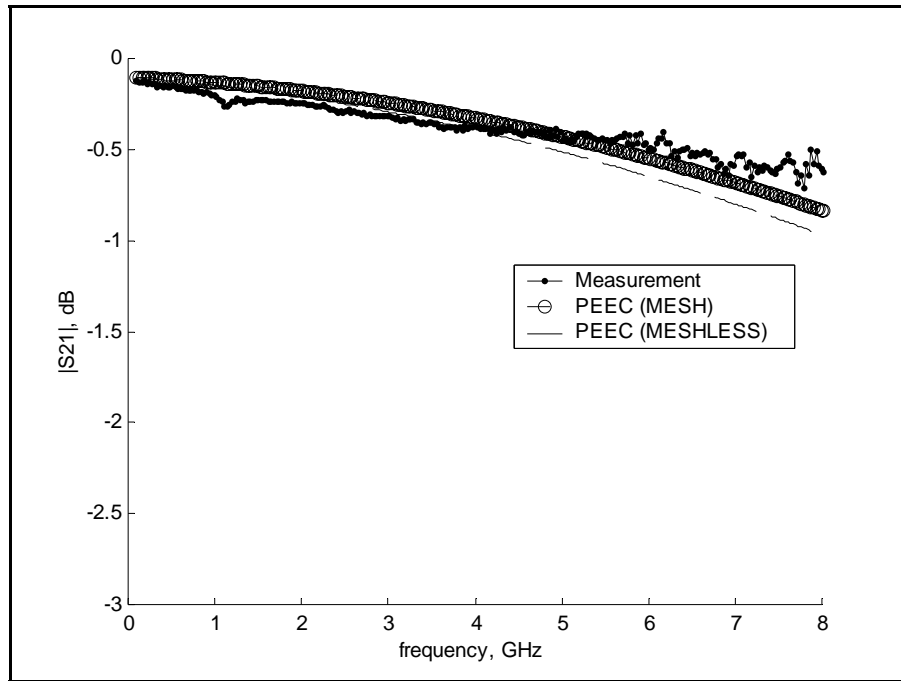
Fig. 4.7: Insertion loss (S_{21}) measurement versus PEEC model

Two variations of the PEEC model, mesh and meshless, are plotted in Figs. 4.7 and 4.8. The meshless case refers to a plain conductor assumption without elastomer meshing. In this case, the second term in equation (4.4) is ignored. This term is included in the PEEC with mesh. As seen in the Figs. 4.7 and 4.8, the included term does not have much effect at low frequency range, but at the higher frequency range, there is a discernable contribution which gives relatively more accurate results when compared to measurements.

The low frequency response, in Fig. 4.7, has an insertion loss of 0.1dB due to contact resistance between the measuring probes and the test sample. PEEC model used 0.5 ohm at the input and output ports to simulate this condition. Resonance is observed at about 1GHz in the measured data which could be attributed to the interaction between the probe and tested sample. This interaction was not included in modeling and is responsible for the 0.1dB magnitude error in the low frequency regime of up to 5GHz. The measured data shows, in the high frequency regime beyond 5GHz, better performance than the model prediction by about 0.2dB. This could be attributed to the surface wave mode propagation effect, due to the presence of grounded wafer chuck beneath the sample, which is not captured in the model.
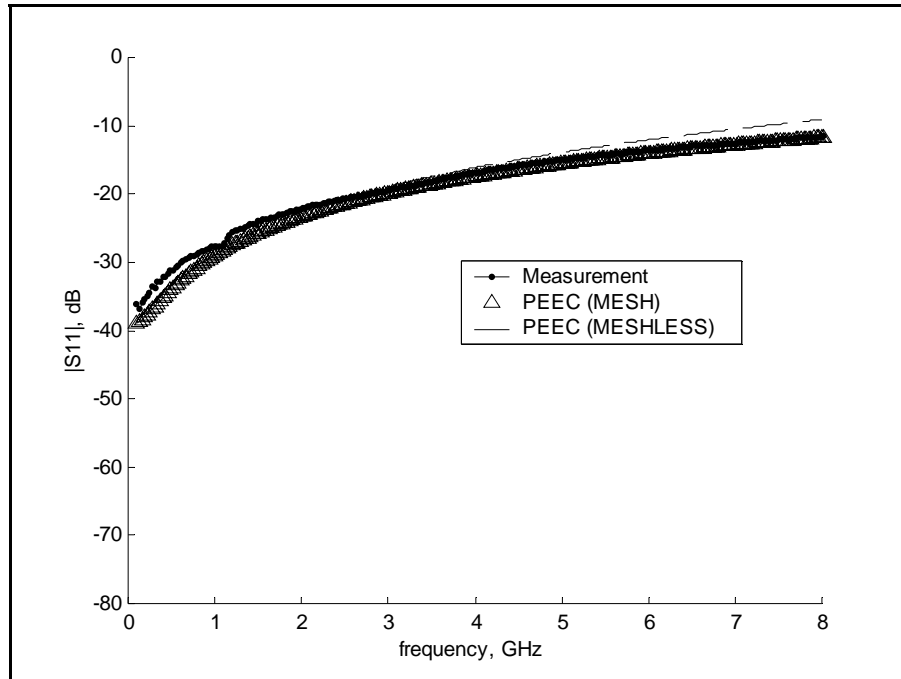
Fig. 4.8: Return loss (S_{11}) measurement versus PEEC model simulation

61

The S_{11} measurement in Fig. 4.8 shows close agreement with model at high frequencies and the low frequency deviations may have their origin in contact impedance induced phase errors. Tables 4.1 and 4.2 depict the comparison of measurements and simulation of insertion loss and return loss respectively. Insertion loss errors were less than 2% throughout the frequency range of interest. Return loss errors were below 10% beyond 2.5 GHz and below 30% at the low end below 2.5GHz.

Table. 4.1: Insertion loss model versus measurement relative error

Frequency, GHz	|S21| Measurement	|S21| Simulated	Error %
1.0	0.986	0.987	-0.25
1.5	0.981	0.986	-0.59
2.0	0.971	0.984	-1.37
2.5	0.973	0.981	-0.87
3.0	0.970	0.977	-0.84
3.5	0.964	0.973	-1.05
4.0	0.961	0.969	-0.88
4.5	0.958	0.964	-0.60
5.0	0.955	0.958	-0.35
5.5	0.955	0.951	+0.29
6.0	0.950	0.945	+0.48
6.5	0.944	0.938	+0.59
7.0	0.941	0.930	+1.14
7.5	0.936	0.921	+1.54
8.0	0.931	0.913	+1.87

Table. 4.2: Return loss model versus measurement relative error

Frequency, GHz	|S11| Measurement	|S11| Simulated	Error %
1.0	0.015	0.011	27.6
1.5	0.032	0.024	25.0
2.0	0.050	0.041	17.9
2.5	0.070	0.059	15.1
3.0	0.086	0.077	10.0
3.5	0.100	0.095	4.9
4.0	0.117	0.113	3.8
4.5	0.138	0.130	5.7
5.0	0.159	0.148	6.3
5.5	0.176	0.166	5.9
6.0	0.194	0.183	5.6
6.5	0.209	0.199	6.5
7.0	0.225	0.216	3.8
7.5	0.239	0.233	2.7
8.0	0.254	0.249	1.8

To summarize this Chapter, the dielectric mesh has been modeled by PEEC method considering the heterogeneous metal-dielectric mix of the substrate material. Good agreement is found between the model and measured results. The mesh material is chosen for fabrication of test probes to provide good vertical compliance, low contact resistance and efficient geometry for high frequency signal transmission.

Contact resistance was maintained at 0.35 ohms throughout the measurement routine as evidenced by the DC measurement values obtained prior to and after VNA measurements. This shows that there is no significant contact degradation at least within the measurement time span of 30 minutes. However, there is found to be a slight degradation over a period of 48 hours to 0.5 ohms. But this value is still acceptable for most practical applications such as burn-in test. The variation of contact resistance with number of contacts up to 20,000 cycles are within 0.5 ohms on a larger prototype meant for automated use, but using the same probe material.

A comparison between the new probing methodology using dielectric mesh substrate and the existing or commercially available probes are given in Table 4.3. Both in terms of high frequency operation and I/O pin density, the elastomer substrate based probe offers superior performance. Due to ease of manufacturability and robustness of contacts over 20000 cycles, it is cost-effective.

Table 4.3: Comparison of different probing technologies

Probe Technology Type	Pitch Micron	Frequency GHz	Pin count Number
Cantilever probe	Above 80	Less than 0.5	Less than 500
Coaxial Probe	Above 100	Less than 3	Less than 500
Membrane Probe	Above 100	Less than 3	Less than 2000
Mesh probe	Above 80	0 – 10	0-10000

CHAPTER 5

PEEC MODELING OF MULTILAYERED MEDIA

5.1 Introduction

PEEC models are becoming good approximations for handling complex challenges posed by large scale MMIC devices through the use of zero dimensional objects such as inductors, capacitors and resistors. Numerous applications of PEEC have been demonstrated for the case of interconnects, vias, power-ground planes, LTCC circuits, spiral inductors, treatment of crosstalk, skin effect and dielectric losses [20]-[26].

Ordinary differential equation based lumped circuit models are made of non-interacting components and are working well at low frequencies since the interaction terms are negligible. As the frequencies approach the microwave range, the interactions among circuit model components cannot be ignored. Delay differential equation based PEEC models are then needed which contain mutual inductive and capacitive two-body couplings. Usually the interactions are considered weak enough that only combination of two-body interactions and the second virial coefficients [92], are sufficient for practical needs.

The purpose of this Chapter is to extend the PEEC model to the case of multilayer dielectrics by treating the dielectric interfaces in terms of an interface function analog of two-body interaction. The boundary between two different dielectrics is treated as a new region to develop the interface function. The interface function is subsequently used to calculate the capacitances and inductances of interface surface cells. The method is first

verified, using a microstrip to evaluate the quasi-static capacitance, with the method of Wheeler. It is then extended to the PEEC formulation and applied to coupled microstrip line filter with multi-layered dielectrics. The results are compared with that of the method of moments. Good agreement is found in the prediction of resonant frequencies and S-parameters.

Section 5.2 introduces the formulation of a function at the interface to separate out the interaction term using boundary conditions. Familiar examples from the literature are represented here. Section 5.3 applies the concept to the quasi-static case of a micro-strip, calculates effective per unit length capacitance and verifies the calculations with the results of Wheeler's method. Section 5.4 extends the retarded-PEEC model of Ruehli and Heeb [91] to the geometries with multilayer dielectrics. Section 5.5 deals with the application of the extended PEEC to quasi-dynamic case of coupled micro-strip filter and the results of transmission and reflection characteristics of the filter are compared against that obtained from the method of moments.

5.2 Interface Function

A multilayer with a half space filled with dielectric of permittivity ε_r is considered first in Fig. 5.1. The Maxwell equation for the dielectric-free space boundary is

$$\nabla \cdot \mathbf{E} = -\frac{\nabla \cdot \mathbf{P}}{\varepsilon_0},$$
(5.1)

where $\mathbf{E}$ and $\mathbf{P}$ are the electric field and polarization vector respectively. At the interface, a third region of infinitesimally small thickness between the dielectric and free space is introduced where the polarization magnitude changes continuously in region 3. The equation (5.1) is satisfied in all the three regions.
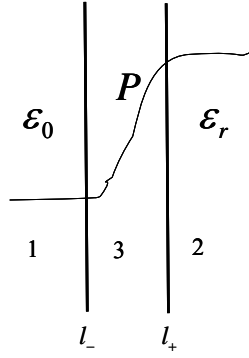
Fig. 5. 1: Interface between two dielectrics.

When the thickness is negligibly small in region 3, the effective permittivity ε_e can be represented as

$$\varepsilon_e = \frac{1}{l_+ - l_-} \int_{l_-}^{l_+} \varepsilon(l)dl \, , \tag{5.2}$$

where l_+ and l_- are locations to the right and left of the interface and $\varepsilon(l)$ is the permittivity distribution function.

When the source charges are at the boundary, we define an effective scalar function λ such that

$$\lambda = \lambda_e G = \frac{G}{\varepsilon_e} \, , \tag{5.3}$$

where G is the quasi-static free space Green's function acting at a distance $\left| \mathbf{r} - \mathbf{r'} \right|$ between the source and field. Typically G is given as

$$G = \frac{\left| \mathbf{G} \right|}{4\pi\varepsilon_0} = \frac{1}{4\pi\varepsilon_0 \left| \mathbf{r} - \mathbf{r'} \right|} \tag{5.4}$$

for three dimensional domain and

$$G = \frac{\left| \mathbf{G} \right|}{2\pi\varepsilon_0} = \frac{1}{2\pi\varepsilon_0} \ln\left| \mathbf{r} - \mathbf{r'} \right| , \tag{5.5}$$

for two dimensional domain.

For region 1, a solution of the equation

$$\nabla^2 G_{e1}(r, r') = -\delta(r - r') \tag{5.6}$$

is sought where $\delta(r - r')$ is the delta function indicating impulse excitation. The solution is obtained by applying the method of scattering superposition [93] using a combination of unbounded (or self interaction) function G_{o1} and scattering (or mutual interaction) function G_m which are represented in terms of Eqs. (5.4) or (5.5). Thus we have

$$G_{e1}(r, r') = G_{o1}(r, r') + G_m(r, r') \tag{5.7}$$

For region 2, we have a similar solution of the form

$$G_{e2}(r, r') = G_{o2}(r, r') + G_m(r, r') \tag{5.8}$$

Correspondingly, the electric fields E_{e1} and E_{e2} in the regions 1 and 2 may also be defined as a combination of unbounded and mutual parts as

$$E = G_e \cdot K, \tag{5.9}$$

where

$$E = \begin{bmatrix} E_{e1}(r, r') \\ E_{e2}(r, r') \end{bmatrix} = \begin{bmatrix} E_{o1}(r, r') + E_{m12}(r, r') \\ E_{o2}(r, r') + E_{m21}(r, r') \end{bmatrix} \tag{5.10}$$

$$G_e \cdot K = \begin{bmatrix} G_{o1}(r, r') & G_m(r, r') \\ G_m(r, r') & G_{o2}(r, r') \end{bmatrix} \cdot \begin{bmatrix} K_1(r') \\ K_2(r') \end{bmatrix} \tag{5.11}$$

K_1 and K_2 are source excitations in region 1 and 2 respectively. While Eq. (5.7) satisfies the equation (5.6) in general, it is uniquely defined only when the coefficients obtained fulfill the boundary conditions.

The 2x2 matrix G_e in (5.11) is formed such that the diagonal components of the matrix form the homogeneous unbounded quasi-static Green's function in the two regions and the counter diagonal terms form the interface component which is the result of interaction between the two regions. That is

$$G_e = \begin{pmatrix} G_{o1} & G_m \\ G_m & G_{o2} \end{pmatrix}.$$

(5.12)

with

$$G_{o1} = \frac{|\mathbf{G}|}{4\pi\varepsilon_0\varepsilon_{r1}} \text{ and } G_{o2} = \frac{|\mathbf{G}|}{4\pi\varepsilon_0\varepsilon_{r2}} \ .$$

The coefficient of G_m is obtained by setting up an eigenvalue problem with characteristic value λ_e. The equation,

$$\mathbf{G}_e\mathbf{X} = \lambda\mathbf{X}$$

(5.13)

is solved subject to the limit when the thickness of region 3 approaches zero. This entails using unit basis vector $\mathbf{X}' = [1,1]$.

The value of counter diagonal term is obtained from the solution of $|\mathbf{G}_e - \lambda\mathbf{I}| = 0$ as

$$G_m = \left(\sqrt{\lambda_e^2 - \lambda_e\left(\frac{\varepsilon_{r1}+\varepsilon_{r2}}{\varepsilon_{r1}\varepsilon_{r2}}\right) + \frac{1}{\varepsilon_{r1}\varepsilon_{r2}}} \right)G \ .$$

(5.14)

For infinitesimally thin half filled dielectric interface in Fig. 5.1, the approximation of $\varepsilon_e = \frac{1+\varepsilon_r}{2}$ leads to

$$G_m = \frac{G}{\sqrt{\varepsilon_r}}\left(\frac{1-\varepsilon_r}{1+\varepsilon_r}\right)$$

.

(5.15)

This interaction term (5.15) along with the self term is responsible for the effective response. It may be noted that the interface function has the form of Silvester's [94] reflection coefficient term divided by the geometric mean of the permittivities of the two regions. Large denominator in (15) results in faster convergence of the partial image sum series in a confined structure. For the case of an interface between two dielectric materials, the interaction term is

$$G_m = \frac{G}{\sqrt{\varepsilon_{r1}\varepsilon_{r2}}} \left(\frac{\varepsilon_{r1} - \varepsilon_{r2}}{\varepsilon_{r1} + \varepsilon_{r2}} \right) . \tag{5.16}$$

The relation (5.16) can be deduced by another reasoning. The interface zone is physically influenced by the permittivity of the neighboring dielectrics. The problem of two different permittivities with uniform charges may be treated as equivalent to the problem of two different charges with uniform permittivity considered by Maxwell [95]. To this effect, the charge terms are replaced by the permittivity terms. The distance between charges are replaced by the elliptic transformation [96]

$$\frac{2}{\varepsilon_{r1} + \varepsilon_{r2}} z = w + w^{-1} , \tag{5.17}$$

of the circle ,

$$|w| = \sqrt{\frac{\varepsilon_{r1}}{\varepsilon_{r2}}} . \tag{5.18}$$

The resulting term which is the mean radius r_m of the extremal surface is given by

$$r_m = \frac{\varepsilon_{r1}\varepsilon_{r2}}{\varepsilon_{r1}^2 - \varepsilon_{r2}^2} \left((\varepsilon_{r1} + \varepsilon_{r2}) \left(\sqrt{\frac{\varepsilon_{r1}}{\varepsilon_{r2}}} + \sqrt{\frac{\varepsilon_{r2}}{\varepsilon_{r1}}} \right) \right) . \tag{5.19}$$

This also leads to the coefficient in (5.16).
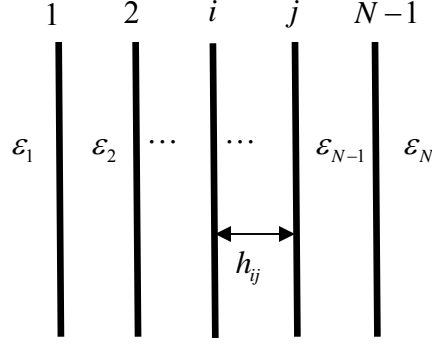
Fig. 5.2: Interfaces within multilayer dielectrics.

For generalizing the interaction term for the multilayer case, all the interfaces need to be included. Let r_{mi} and r_{mj} be the mean radii of interfaces i and j respectively at distances h_i and h_j from the reference plane. Following Maxwell's approach [95], the interaction between the interfaces turns out to be the partial image sum

$$Gm_{ij} = \frac{G}{k_{ij}\sum_{n=0}^{\infty}\left(\frac{1}{\sin h(n\omega - \alpha)}\right)} , \qquad (5.20)$$

where

$$k_{ij} = \frac{\sqrt{r_{mi}^{4} + r_{mj}^{4} + r_{ij}^{4} - 2r_{mi}^{2}r_{mj}^{2} - 2r_{mi}^{2}r_{ij}^{2} - 2r_{mj}^{2}r_{ij}^{2}}}{2r_{ij}} , \qquad (5.21a)$$

$$\alpha = \sinh^{-1}\left(-\frac{k_{ij}}{r_{mi}}\right), \qquad (5.21b)$$

$$\beta = \sinh^{-1}\left(\frac{k_{ij}}{r_{mj}}\right), \qquad (5.21c)$$

$$r_{ij} = \frac{r_{mi}h_i - r_{mj}h_j}{h_{ij}} , \qquad (5.21d)$$

$$r_{mi} = \frac{\varepsilon_i \varepsilon_{i+1}}{\varepsilon_i - \varepsilon_{i+1}} \left(\sqrt{\frac{\varepsilon_i}{\varepsilon_{i+1}}} + \sqrt{\frac{\varepsilon_{i+1}}{\varepsilon_i}} \right) \qquad (5.21e)$$

$$r_{mj} = \frac{\varepsilon_j \varepsilon_{j+1}}{\varepsilon_j - \varepsilon_{j+1}} \left(\sqrt{\frac{\varepsilon_j}{\varepsilon_{j+1}}} + \sqrt{\frac{\varepsilon_{j+1}}{\varepsilon_j}} \right) \qquad (5.21f)$$

and $\omega = \alpha + \beta$.

The interaction of ith interface with all the other interfaces from 1 to $N-1$ results in

$$Gm_i = \left(\sum_{j=1}^{N-1} \frac{1}{k_{ij} \left(\sum_{n=0}^{\infty} \frac{1}{\sin h(n\omega - \alpha)} \right)} \right) G \ . \qquad (5.22)$$

The basis for the application of the image method in multilayer structure is explained in Appendix C.1 and C.2. A comparison of the performance of Interface function with that of Silvester's [94] is given using a dielectric slab example in Appendix C.3.

5.2.1 Example A : Inductive Open Wire Loop
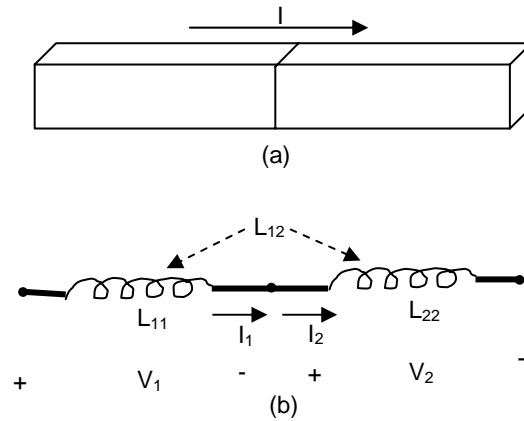
Fig. 5.3: Open wire loop of two conducting bars in series.

An inductive open wire loop example [97] of Fig. 5.3 is provided as a simple macroscopic analogue of interface function matrix. The loop may be considered as a connection of two conducting bars in series. The voltages and currents in the system are related through

$$\begin{pmatrix} V_1(s) \\ V_2(s) \end{pmatrix} = s \begin{pmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{pmatrix} \begin{pmatrix} I_1(s) \\ I_2(s) \end{pmatrix} .$$

(5.23)

Assuming that same current flows through the bars and that the bars form a tightly coupled lossless system, the mutual inductance becomes

$$L_{12} = L_{21} \approx \sqrt{L_{11}L_{22}} .$$

(5.24)

The relation (5.24) may be obtained from (5.14) by duality as a volume integration of the interface function kernel when $\lambda_e = 0$. So the net inductance of the serial conducting bar system becomes

$$L \approx L_{11} + L_{22} + 2\sqrt{L_{11}L_{22}} .$$

(5.25)

The mutual inductance in this case is an outcome of the two body interaction of two self inductance terms.

5.2.2 Example B: Insulated Capacitive Spheres
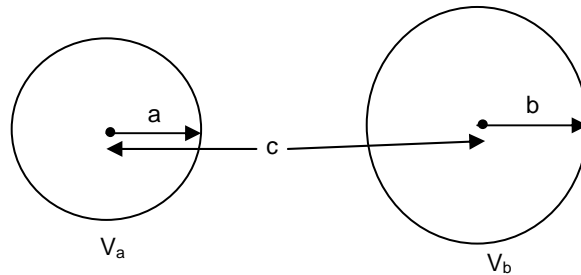
Fig. 5.4: System of two insulated spheres

Another example [98] of Fig. 5.4 is the capacitance coefficient of the system of two insulated spheres of radii a and b the centers of which are separated by distance c. When the spheres are maintained at potentials V_a and V_b, with charges Q_a and Q_b, the system is represented by

$$\begin{pmatrix} Q_a \\ Q_b \end{pmatrix} = \begin{pmatrix} C_{aa} & C_{ab} \\ C_{ab} & C_{bb} \end{pmatrix} \begin{pmatrix} V_a \\ V_b \end{pmatrix}, \tag{5.26}$$

where

$$C_{aa} = k \sum_{n=1}^{\infty} \operatorname{cosec} h(n\omega - \beta), \tag{5.27a}$$

$$C_{bb} = k \sum_{n=1}^{\infty} \operatorname{cosec} h(n\omega - \alpha), \tag{5.27b}$$

$$k = \frac{\sqrt{a^4 + b^4 + c^4 - 2a^2b^2 - 2b^2c^2 - 2c^2a^2}}{2c}, \tag{5.27c}$$

$$a = k \operatorname{cosec} h\alpha, \tag{5.27d}$$

$$b = k \operatorname{cosec} h\beta, \tag{5.27e}$$

$$c = k(\cot h\alpha + \cot h\beta) \tag{5.27f}$$

and $\alpha + \beta = \omega$. The capacitance coupling between two equal spheres is obtained as

$$C_{ab} = -\sqrt{C_{aa}C_{bb}} = -k \sum_{n=1}^{\infty} \operatorname{cosec} h(n\omega) \tag{5.28}$$

The self-terms in the form of partial image sum series of insulated spheres leads to an interaction term which is also a partial sum.

Examples A and B give the proof that the multilayer case reduces to the non-layer case as evidenced by $\lambda_e \to 0$ in equation (5.14).

5.3 Two Layer System: Microstrip Capacitance

In the microstrip quasi-static case of Fig. 5.5, the solution of potential ϕ is sought for the Laplace equation, namely,

$$\frac{\partial^2 \phi}{\partial x^2} + \frac{\partial^2 \phi}{\partial y^2} = 0 \quad , \tag{5.29}$$

with the boundary conditions

$$\phi = const \quad , \tag{5.30}$$

at the conductor boundary and

$$\varepsilon_{r1} \frac{\partial \phi_1}{\partial y} = \varepsilon_{r2} \frac{\partial \phi_2}{\partial y} \quad , \tag{5.31}$$

at the boundary between two dielectrics due to the continuity of the normal components of electric displacement.

The potential at any point in the plane of the problem is given by the logarithmic kernel as [99]-[100]

$$\phi(\mathbf{r}) = \frac{1}{2\pi\varepsilon_0} \sum_k \int_{R_k} \sigma(\mathbf{r}')\mathbf{G}(\mathbf{r},\mathbf{r}')dR \quad , \tag{5.32}$$

where $\mathbf{r}'$ and $\mathbf{r}$ are the source and field distances, $\sigma(\mathbf{r}')$ is the corresponding charge respectively over k interfaces of contour R_k .

Expanding the charges in pulse basis, P_n , leads to

$$\sigma(r) = \sum_n \sigma_n P_n(r) \quad . \tag{5.33}$$

Using the applied potential V_k at the conducting surfaces, the moment method formulation [100] of the microstrip problem with point matching becomes

$$\sum_n S_{mn}\sigma_n = V_k \ , \tag{5.34}$$

where S_{mn} is given by

$$S_{mn} = \frac{1}{2\pi\varepsilon_0} \int_{R_k} \mathbf{G}(\mathbf{r},\mathbf{r'}) dR , \tag{5.35}$$

for the PEC boundary and

$$S_{mn} = \frac{1}{2\pi\varepsilon_0} \int_{R_k} \hat{\mathbf{r}} \cdot \nabla \mathbf{G}_m(\mathbf{r},\mathbf{r'}) dR \ . \tag{5.36}$$

for the dielectric boundary. For numerical implementation, the transverse width of the dielectric layer is taken to be finite laterally.
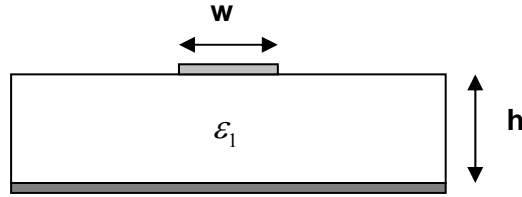
Fig. 5.5: Microstrip geometry
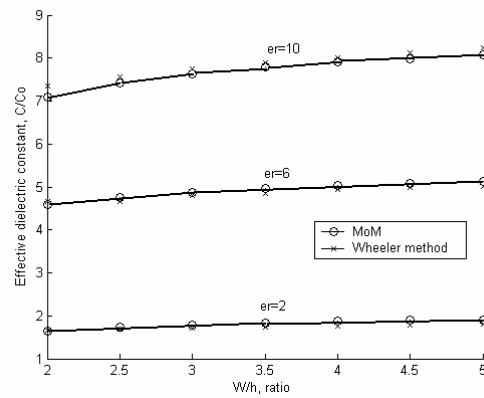
.   **Fig. 5.6:** Effective permittivity versus w/h

For the microstrip geometry, the effective capacitance is calculated as a function of the ratio of strip width and height. The dielectric layer width is taken to be about five times that of the conductor width. The results are plotted in Fig. 5.6 along with the results obtained from the Wheeler method [101] for comparison. Close agreement of the order of 1% is obtained using the interface function for the geometry variations and for different dielectric permittivity values.

5.4 Extension to PEEC Model

The PEEC model for the case of homogeneous dielectrics [91] is treated by adding and subtracting the displacement current from the Maxwell's equation as

$$\nabla \times \mathbf{H} = \mathbf{J}_C + \varepsilon_0 (\varepsilon_r - 1) \frac{\partial \mathbf{E}}{\partial t} + \varepsilon_0 \frac{\partial \mathbf{E}}{\partial t}, \qquad (5.37)$$

so that the polarization current due to the dielectrics is combined with conductor current to represent inductive elements.
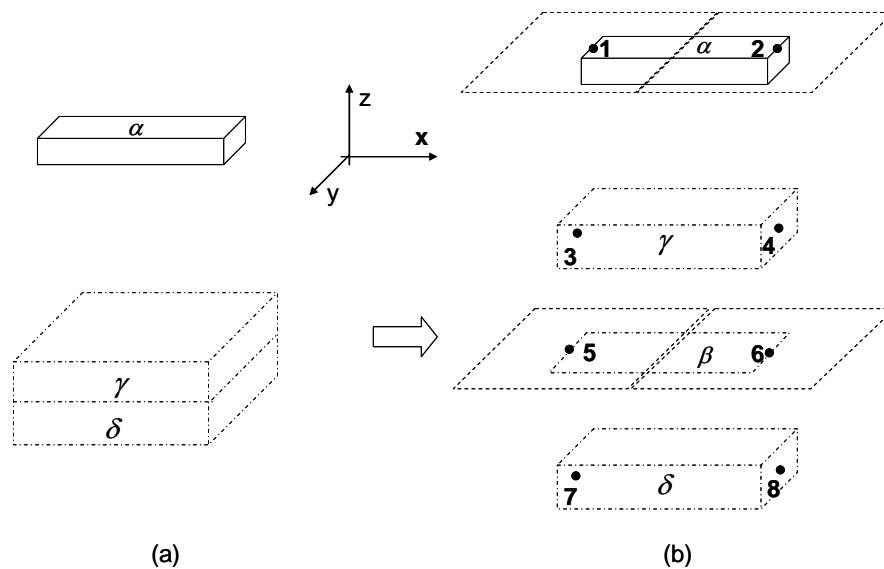
Fig. 5.7: Cell structure for finite conductor including (a) multilayer dielectrics with (b) multilayer split into two bulk layers and an interface layer

By including dielectric interfaces, it is noted from (5.1) that

$$\nabla \cdot \left(\varepsilon_0 \mathbf{E} + \mathbf{P} \right) = 0 , \tag{5.38}$$

where the polarization vector is included into the free space divergence term such that

$$\mathbf{P} = \varepsilon_0 (\varepsilon_r - 1) \mathbf{E} . \tag{5.39}$$

In view of (5.10), the polarization field is split into unbounded and interaction parts. Accordingly the equation (5.39) evolves into (5.40) with two terms, the first term being the contribution from the bulk dielectric and the second term from the interface.

$$\mathbf{P} = \varepsilon_0 (\varepsilon_r - 1) \mathbf{E}_0 + \varepsilon_0 (\varepsilon_e - 1) \mathbf{E}_m . \tag{5.40}$$

The field equation (5.37) is then modified to,

$$\nabla \times \mathbf{H} = \mathbf{J}_C + \varepsilon_0 (\varepsilon_r - 1) \frac{\partial \mathbf{E}_0}{\partial t} + \varepsilon_0 (\varepsilon_e - 1) \frac{\partial \mathbf{E}_m}{\partial t} + \varepsilon_0 \frac{\partial \mathbf{E}}{\partial t} . \tag{5.41}$$

The polarization term $\varepsilon_0 (\varepsilon_e - 1) \mathbf{E}_m$ is responsible for the interaction $\mathbf{G}_m$ in the interface function.

For the case of a multilayer dielectric system in Fig. 5.7 consisting of a conductor cell α and multi-dielectric cell $\gamma - \delta$, the PEEC model takes the form of additional sets of inductance and capacitance elements due to the interface layer nodes. Following the notations from [91], the PEEC equation for dielectric interfaces – a contribution of this thesis, for components in x- direction, applied to conductor cell α in Fig. 5.7 is

$$\frac{\mathbf{J}_x^C(\mathbf{r},t)}{\sigma_\alpha} + \frac{\mu}{4\pi} \int_{v_\alpha'} \mathbf{G}(\mathbf{r},\mathbf{r}') \frac{\partial \mathbf{J}_x^C(\mathbf{r}',t_d)}{\partial t} dv' \qquad + \frac{\mu}{4\pi} \varepsilon_0 (\varepsilon_\beta - 1) \int_{s_\beta'} \mathbf{G}_m(\mathbf{r},\mathbf{r}') \frac{\partial^2 \mathbf{E}_{mx}(\mathbf{r}',t_d)}{\partial t^2} ds'$$

$$+ \frac{\mu}{4\pi} \varepsilon_0 (\varepsilon_\gamma - 1) \int_{v_\gamma'} \mathbf{G}(\mathbf{r},\mathbf{r}') \frac{\partial^2 \mathbf{E}_{0x}(\mathbf{r}',t_d)}{\partial t^2} dv' + \frac{\mu}{4\pi} \varepsilon_0 (\varepsilon_\delta - 1) \int_{v_\delta'} \mathbf{G}(\mathbf{r},\mathbf{r}') \frac{\partial^2 \mathbf{E}_{0x}(\mathbf{r}',t_d)}{\partial t^2} dv'$$

$$+\frac{1}{4\pi\varepsilon_0}\int_{s_\alpha'}\frac{\partial}{\partial x}\mathbf{G}(\mathbf{r},\mathbf{r}')q^T(\mathbf{r}',t_d)ds'+\frac{1}{4\pi\varepsilon_0}\int_{s_\beta'}\frac{\partial}{\partial x}\mathbf{G}_m(\mathbf{r},\mathbf{r}')q^T(\mathbf{r}',t_d)ds'=0,\qquad(5.42)$$

where $\mathbf{J}_C$ and q^T are the source currents and charges. t_d is the retardation time between circuit elements given by

$$t_d=t-\frac{|\mathbf{r}-\mathbf{r}'|}{c}\sqrt{\mu_f\varepsilon_f}\ ,\qquad(5.43)$$

where c is the velocity of light in free space and μ_f, ε_f are the relative permeability and permittivity of the field regions. The representation of dielectric interfaces, through equation (5.42), using interface function $\mathbf{G}_m$ is a contribution of this thesis. This leads to the treatment of multilayer dielectrics in a PEEC framework. The integral equation expression [2, 5, 91] for the PEEC model is given by equation (2.15) where the inverse distance kernel function $G(\mathbf{r},\mathbf{r}')=\dfrac{1}{|\mathbf{r}-\mathbf{r}'|}$ which is part of the quasi-static free space Green's function, is used for extraction of circuit components. For circuit solver operation in the time domain the factor $e^{-jk|\mathbf{r}-\mathbf{r}'|}$ is replaced by the time delay $t_d=t-\dfrac{|\mathbf{r}-\mathbf{r}'|}{c}$ where c is the velocity of light and $|\mathbf{r}-\mathbf{r}'|$ is the source to field distance. Delay factor included through t_d in the expressions for current derivative and charge variables, $\dfrac{\partial\mathbf{J}(\mathbf{r}',t_d)}{\partial t}$ and $q(\mathbf{r}',t_d)$, accounts for time harmonic effects through the convolution of $\mathbf{G}(\mathbf{r},\ \mathbf{r}')$ and current source $\dfrac{\partial\mathbf{J}(\mathbf{r}',t_d)}{\partial t}$ for inductive couplings and through the convolution of $\mathbf{G}(\mathbf{r},\ \mathbf{r}')$ and charge source $q(\mathbf{r}',t_d)$ for capacitive couplings.

For multilayer dielectrics, similarly, the static form $\mathbf{G(r,r')}$ is modified by images $\mathbf{G_m(r,r')}$ for interface cells but retaining the retardation time t_d. The PEEC equation in time domain is given by equation (5.42). The same approach as [2, 5, 91] has been followed using retarded action between mutual couplings among inductances and among capacitances to produce time harmonic effects with the only modification of the static inverse distance kernel $\mathbf{G(r,r')}$ with its image equivalent $\mathbf{G_m(r,r')}$ for the multilayer dielectrics.

Upon integration, the first term of equation (5.42) leads to the potential term due to the resistance element with conductivity of σ, the second term gives the potential due to inductance of electric conductor, the third term gives the potential due to the inductance of dielectric interface, the fourth and fifth terms lead to the potential due to the inductances of dielectric interiors respectively. The last two terms correspond to the potentials due to capacitance elements of conducting surfaces with free charges and dielectric interfaces with bound charges respectively.
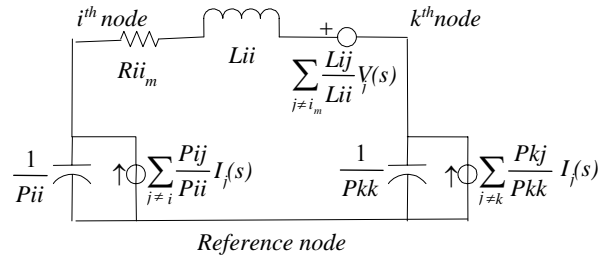
Fig. 5.8: PEEC model at metal and dielectric interface

Fig. 5.8 shows the equivalent circuit representation of metal and dielectric interfaces where the interaction is governed by the mutual inductances as well as capacitances. The resistance element is obtained by integrating the first term in (5.42) as

$$\int_{v'} \frac{\mathbf{J}_x^C(\mathbf{r},t)}{\sigma_{ii}} dv' = R_{ii} = \frac{l_{ii}}{\sigma a_{ii}} \quad , \tag{5.44}$$

where l_{ii} and a_{ii} are the cell length along the direction of current flow and cell cross sectional area perpendicular to the direction of current flow respectively.

For the metal cells, the inductance is calculated by integrating the second term of (5.42) as

$$L_{ijm} = \frac{\mu}{4\pi a_i a_j} \int_{v_j} \int_{v_i} \mathbf{G}(\mathbf{r}_j, \mathbf{r}_i') dv_i' dv_j \quad , \tag{5.45}$$

where a_i and a_j are the cross sectional area of the volume cell perpendicular to the direction of current flow. $i = j$ corresponds to the partial self inductance and $i \neq j$ corresponds to the partial mutual inductance. The inductive couplings are represented by the voltage controlled voltage source summation term

$$V_L = \sum_{j \neq i} L_{ij} \frac{\partial i_{Lj}(t - t_{dij})}{\partial t} = \sum_{j \neq i} \frac{L_{ij}}{L_{ii}} \varphi_{Lj}(t - t_{dij}) , \tag{5.46}$$

where φ_{Lj} is the potential across the jth inductance cell and t_{dij} is the time delay according to (5.43) between interaction among ith and jth cell.

For dielectric interfaces volume integrals are to be replaced by surface integrals such that the interaction becomes

$$L_{ijd} = \frac{\mu \varepsilon_0 (\varepsilon_j - 1)}{4\pi a_i l_j} \int_{v_j} \int_{v_i} \mathbf{G}_m(\mathbf{r}_j, \mathbf{r}_i') dv_i' ds_j , \tag{5.47}$$

where ε_j and l_j are the effective permittivity and cross sectional length perpendicular to current flow in the dielectric interface respectively.

For capacitance calculation of metal cells, the integral expression of the sixth term in (5.42) is approximated to give partial coefficient of potential as

81

$$\frac{1}{4\pi\varepsilon_0}\iint_{s_j\,s_i}\frac{\partial}{\partial x}\mathbf{G}(\mathbf{r}_j,\mathbf{r}_i')q^T ds_i' ds_j = \frac{1}{4\pi\varepsilon_0 a_j}\int_{s_i'}\left[\mathbf{G}(\mathbf{r}_{jx}+\frac{\Delta\mathbf{r}_{jx}}{2},\mathbf{r}')-\mathbf{G}(\mathbf{r}_{jx}-\frac{\Delta\mathbf{r}_{jx}}{2},\mathbf{r}')\right]Q^T ds_i'$$

$$= Q^T(P_{ij}^+ - P_{ij}^-)\,, \tag{5.48}$$

where $\Delta\mathbf{r}_{jx}$ is the cell width in the x direction and $Q^T = a_j q^T$, is the total charge of the jth

cell. In general, the coefficient of the potential is represented as

$$P_{ijm} = \frac{1}{4\pi\varepsilon_0 a_i a_j}\iint_{s_j\,s_i'}\mathbf{G}(\mathbf{r}_j,\mathbf{r}_i')ds_i' ds_j\,, \tag{5.49}$$

Similarly, for the capacitance calculation of dielectric interfaces, the coefficient of
potential used is

$$P_{ijd} = \frac{1}{4\pi\varepsilon_0 a_i a_j}\iint_{s_j\,s_i'}\mathbf{G}_m(\mathbf{r}_j,\mathbf{r}_i')ds_i' ds_j\,. \tag{5.50}$$

The capacitive couplings are represented by the current controlled current source
summation term

$$I_C = \sum_{j\neq i}\frac{P_{ij}}{P_{ii}}i_{Cj}(t-t_{dij})\,, \tag{5.51}$$

where i_{Cj} is the current through the jth capacitive cell.
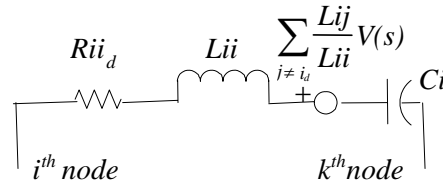
Fig. 5.9: PEEC model at dielectric interior

Fig. 5.9 shows the equivalent circuit for dielectric interior [91] where the interaction is due to the mutual inductance components alone. The inductance formulation for the dielectric interior is similar as (5.45) with the exception of the weight $\varepsilon_0(\varepsilon_r - 1)$. A series resistance is added to represent a lossy dielectric. Series capacitance is obtained from

$$C_i = \frac{\varepsilon_0(\varepsilon_i - 1)a_i}{l_i} \ ,$$
(5.52)

where l_i and a_i are the interior dielectric cell length along current direction and cross sectional area respectively.

5.5 Multilayer PEEC Example: Coupled Microstrip Line Filter

The coupled microstrip line filter is chosen as a specific numerical test of the proposed PEEC model. The dynamic properties of the circuit such as the transmission characteristics and resonant frequency for three layer and four layer geometries are investigated.

5.5.1 Three Layer Geometry

The substrate in Fig. 5.10 is made of two dielectric layers with permittivity of 3.78 and 2.31 for the bottom and top layer respectively. Thickness of both the layers is 31.5 mils. The top metal layer has three coupled micro-strip lines with length of 870 mils, width of 90 mils and spacing of 50 mils in the exterior lines and 35 mils in the interior lines. The exterior transmission lines are extended by 435 mils. The intermediate metal layer has two conducting patches of size 435mil x 230 mil. These patches are introduced to

enhance the coupling effects. Copper metal of thickness 1.2 mils is used. All the dielectrics are assumed to have a loss tangent of 0.0009.

n1 to n7 in Fig. 5.10 are the geometrical locations corresponding to the circuit nodes indicated in Fig. 5.11. For clarity of presentation, only portions of the complete equivalent circuit are shown in Figs. 5.9 and 5.10. Interactions between circuit elements are shown in solid objects. The squares and circles represent inductance couplings of the form of (5.46) in the x and y direction respectively. The vertical rectangles in Fig. 5.11 and horizontal rectangles in Fig. 5.12 represent the capacitive couplings in the form of Eq. (5.51) due to the metal and dielectric interfaces respectively.
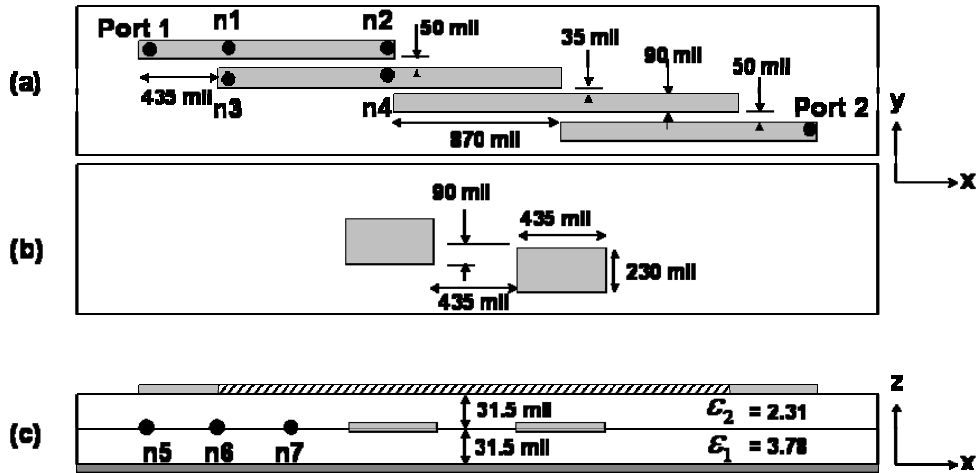
Fig. 5.10: Coupled microstrip filter geometry. (a) Top metal layer, (b) Intermediate metal layer and (c) Multilayer cross section backed by ground plane (hashed segment represents coupled line; solid segments represent single transmission line / metal patch)

The geometry was simulated in moment method based on a full-wave solver from called Momentum [102]. The results are compared with that obtained from PEEC simulation. Circuit implementation treats the lateral extent of the substrate to be finite, of about five times the size of the coupled strip, to keep the computational effort reasonably low while

maintaining required accuracy. The circuit element cells have been segmented in the order of $\lambda/10$ for 3 GHz operation. Details of the implementation are similar to that described in [91], [2, 25] but with inclusion of additional circuit nodes of Fig. 5.12 due to multilayer interfaces. Fig. 5.13 shows the close agreement between the two simulations. The resonant frequencies are found to be 2.14 GHz and 2.45 GHz with insertion loss (S_{21}) of 1.5dB and 2.3dB respectively.
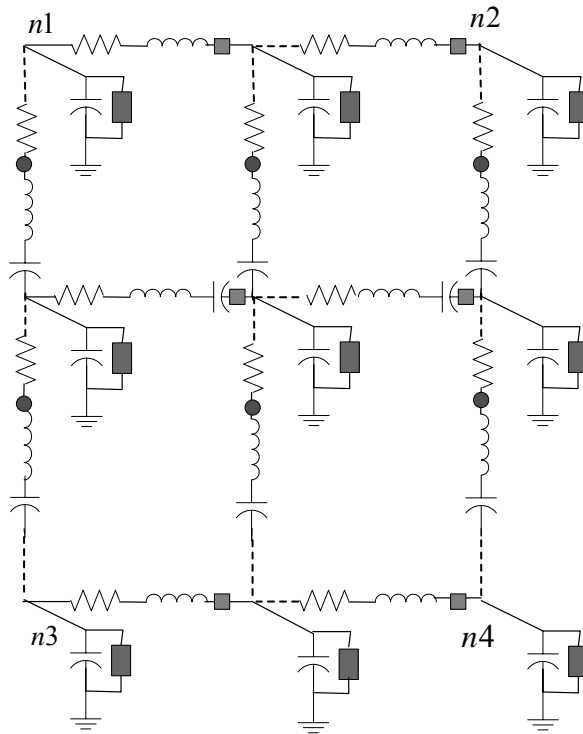
Fig. 5.11: Equivalent circuit for a coupled micro-strip
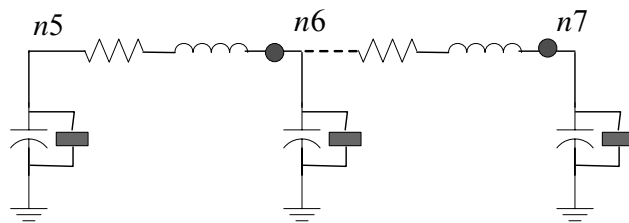
Fig. 5.12: Equivalent circuit at the interface layer nodes
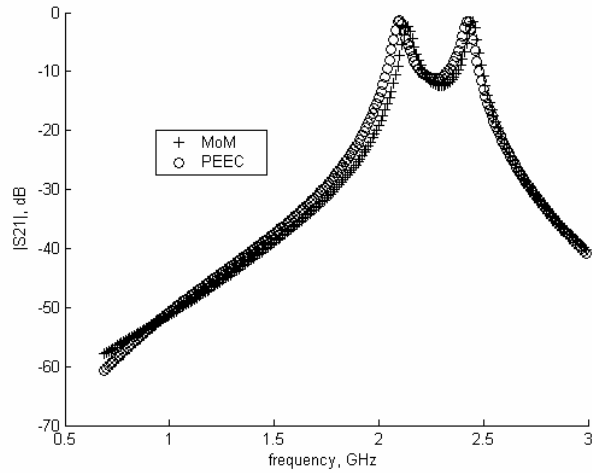
Fig. 5.13: S_{21} magnitude response of three layer coupled line filter

5.5.2 Four Layer Geometry

The substrate in Fig. 5.14 is modeled with three dielectric layers and the free space as the top layer. The geometry is same as the earlier test case except that the bottom layer with the permittivity of 4.82 and thickness 31.5 mils has been added. A square shaped metallic patch of side 355 mil and thickness 1.2 mil is included between the bottom and its adjacent layer. The PEEC implementation is same as the previous case.

S11 in Fig. 5.15 shows that the lower resonant frequency has drifted noticeably due to the couplings from the additional dielectric and metal layer. The resonant frequencies were found to be 2.03GHz and 2.45GHz in the method of moment solver which compares closely to 2.01 GHz and 2.41GHz calculated through PEEC.
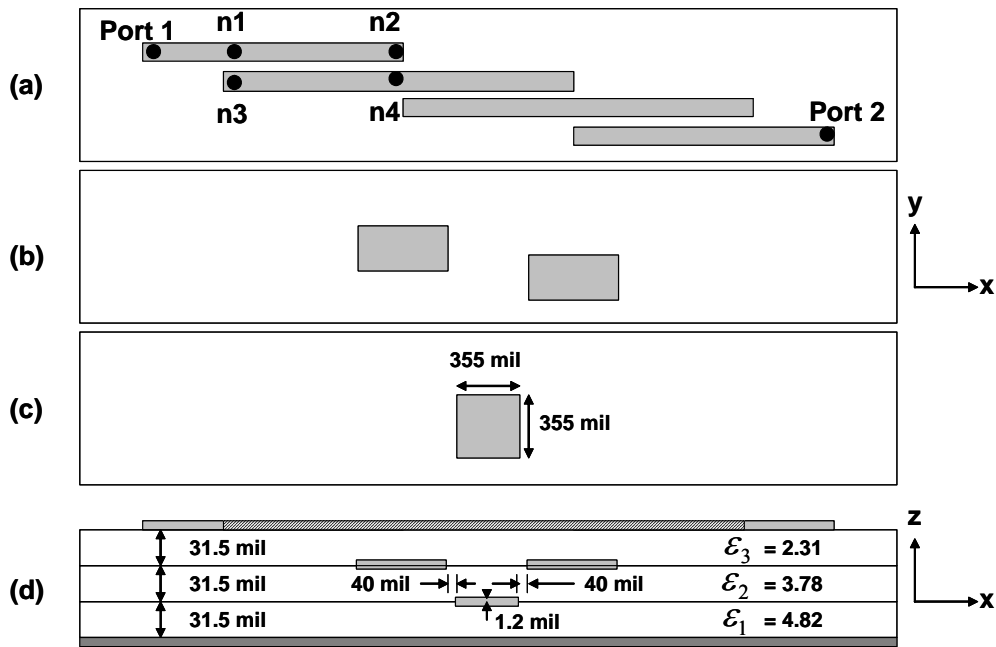
Fig.5.14: Four layer coupled microstrip filter geometry. (a) Top metal layer, (b) Second metal layer, (c) Third metal layer and (d) Multilayer cross section backed by ground plane (hashed segment represents coupled line; solid segments represent single transmission line / metal patch)
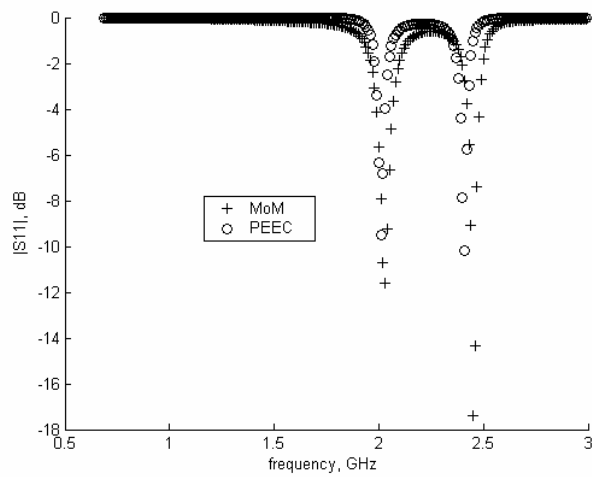
Fig. 5.15: S_{11} magnitude response of four layer coupled line filter

5.6 Discussion

PEEC method has been applied to multilayer dielectric geometry in this Chapter. To do this, the concept of mutual interactions between circuit elements is extended to interface function. Isolation of the self and mutual components lends itself to separate treatment of the interface from the bulk substrate. This formulation was first tested in a quasi-static capacitance problem in a micro-strip. The per unit length capacitance was evaluated for different geometries and material properties. Then transmission characteristics of a multilayered coupled micro-strip filter were analyzed. The treatment of the dielectric interface in terms of the convolution of the interface function and the source function with pulse basis in the time domain is found to give satisfactory results compared to other independent studies. This formulation will be useful in analyzing complex multilayer chips and packaged systems at microwave/RF frequencies by incorporating it into existing circuit solvers.

Existing multilayer models, for example, dyadic Green's function, while being rigorous are relatively computation intensive. The image based model described in this Chapter is more economical in computational terms due to the faster convergence of the partial image sum series. This economy would translate to a more practical and compact circuit representation of large multilayer VLSI systems where we typically look for accuracy of the order of a few percent in circuit solvers. We could gain the flexibility to handle large complex systems with acceptable accuracy.

CHAPTER 6

DEVELOPMENT OF A NOVEL MULTI-GIGAHERTZ TEST INTERFACE FOR FINE PITCH WAFER LEVEL PACKAGES : AN APPLICATION OF PEEC MODELING

6.1 Introduction

PEEC modeling of transmission lines in homogeneous lossless and lossy media, dielectric mesh and multilayer have been addressed in the earlier Chapters. The objective of this Chapter is bringing together all the above components into a system, modeling the system towards the physical realization of a prototype hardware and demonstration of high frequency signal transmission with 100 micron pitch wafer level packages.

The test concepts with specific reference to fine pitch wafer level packages are presented in the rest of this section. Section 6.2 gives the details of the prototype structure and fabrication to facilitate the discussion of the modeling which is the subject of section 6.3. Model and measurement results are discussed in section 6.4. Section 6.5 provides the practical implementation aspects for functional and structural testing of WLPs along with measured results.

6.1.1 Significance of Wafer Level Packaging

Miniaturization of portable and hand-held electronic devices has stimulated the need for packages of even smaller size than conventional BGA and CSP packages. A wafer level package is a chip size package, and the area that it occupies when mounted onto a system

level board is as small as the size of the IC itself. This is what makes it different from all other package types. Since the size of the package and the area it occupies on the printed wiring board are equal to the size of the IC, WLP can be considered as the ultimate IC packaging option. WLPs offer minimum size and weight for a given die, but cost is also expected to be lower than for traditional IC packaging.[1]

Conventionally semiconductor device wafers are sawn into dies and then made into packages by using plastic molding compounds. The packaging process degrades the electrical performance of the devices because the plastic acts like a capacitance attached to every node of the circuit. So it slows down the device speed. That is one reason, from electrical performance point of view, why a big effort is going on to use bare dies with fine pitch interconnects directly onto the PCB boards. The mismatch in the coefficient of thermal expansion (CTE) between silicon and organic substrates makes the components to expand (CTE mismatch by a factor of 10 for silicon and FR4) at different rates while heating up and this lead to cracks and other reliability problems. So a wafer level off-chip interconnect is needed to cushion this difference. Testing WLP with its off-chip interconnects is critical to make sure that the device meets electrical performance specifications before using it in the final product.

6.1.2 WLP Test Concept

WLP testing involves three major considerations. Firstly, the electronic circuits that create and detect signals at high frequency with which the device operates. The signal generation point should be as close to the device as possible to minimize parasitic effects that usually corrupt the signal integrity. The multi-gigahertz signal can be produced from

low frequency signals either by multiplexing them using programmable gate arrays[103] or by multiplying with phase locked loops[104]. Signal detection is done by demultiplexing or sampling the high frequency signals. For the current prototype, a vector network analyzer is used for forcing and measuring signals via SMA connectors soldered on multilayer PCB board.

Secondly the interface which links the test signal hardware to the device under test, referred to as interposer, should provide enough vertical compliance to accommodate thickness variations on the wafer while maintaining good electrical contact without breaking either the probe or the interconnect. Lateral compliance is also needed for thermal tests at hot and cold ambient to accommodate the contraction and expansion of the device. The present prototype employs the novel elastomer mesh as an interposer between the WLP and the PCB substrate.

Thirdly we need a manual or an automated mechanism to align the leads of the WLP device under test and the test interposer. We have used manual alignment socket with corner guide pins for our prototype. For mass production test, the alignment part can be done in an automated wafer prober with pattern recognition facility in the equipment. The CCD sensor on the prober captures the device pad / interconnect features and the interposer probe as two images which are then merged for establishing alignment through the feedback mechanism that drive wafer chuck with a stepper motor .

6.1.3 Limitation of Conventional Test Approaches for WLPs

Currently available test probes do not meet the pitch and frequency requirements of WLP devices at the same time. While the coaxial probes and air-coplanar probes, for instance,

91

provide high frequency operation, they do not scale down to small sizes and so are not suited for fine pitch device characterization.

The cantilever beam probes have been used at pitch sizes of the order of 80 microns in the industry for testing chips with peripheral pin counts on the order of hundreds but the long leads make them unsuited for high frequency area array testing. There are Cobra probes, membrane and DoD (die-on-die) probes from various sources but their problem is that they do not provide reliable contacts and are not scalable to very high pin counts (beyond a thousand or two).

It is desired to provide very high pin count (on the order of 1000's of pins per square centimeter), vertically compliant, high frequency and high temperature test probes to meet the demands of wafer scale probing of semiconductors as against the testing of individual chips.

6.1.4 Test Solution
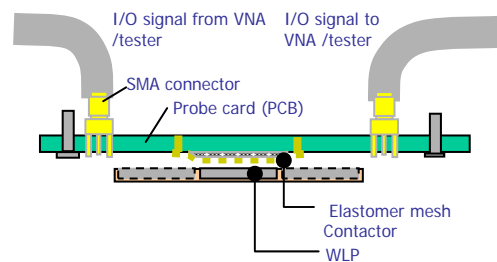
Fig. 6.1: Test hardware for WLP device under test.

Fig. 6.1 shows the proposed test bed connection of the elastomer mesh interposer sheet between WLP device under test and PCB with SMA connectors. The interposer sheet is made of metal particle suspension on a dielectric mesh. This heterogeneous mixture contributes towards the necessary vertical and lateral compliance while maintaining good conductivity and low contact resistance. The multilayer PCB is used for signal distribution between WLP and the test equipment.

6.2 Structure of Prototype and Fabrication

6.2.1 Test Fixture

The schematic of the test fixture is shown in Fig. 6.2 with its associated components described in Table 6.1. The test fixture design consists of two parts, first, an elastomer mesh that provides electrical and mechanical interface to the WLP and secondly a multilayer PCB substrate made of BT resin material which houses 3.5mm SMA connectors. The connectors are connected through coaxial cables with the vector network analyzer for S parameter measurements.

The multilayer PCB has four metal layers, two of which form signal trace layers on either side of the board and the other two are buried layers used as ground planes. The PCB serves as a space transformer between the fine pitch WLP (at the 100 micron level) and the instrumentation connector (at the millimeter level). The layout of the PCB signal traces are depicted in Figs. 6.3 and 6.4.
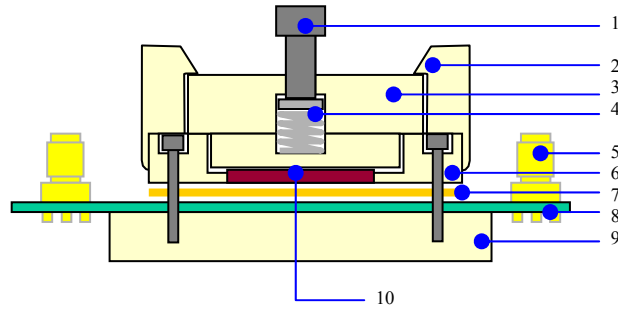
Fig. 6.2: Prototype test fixture

Table. 6.1:: Test fixture part details

No.	Parts name	Material
1	Pressure Adjust	Techtoron PPS
2	Screw Clamp lever	Techtoron PPS
3	Device press plate	Techtoron PPS
4	DUT press spring	Customized
5	RF connector	SMA 3.5mm
6	Device Guide	Techtoron PPS
7	Elastomer Mesh Contactor	Forming
8	PCB	BT Resin
9	Base Plate	Techtoron PPS
10	DUT	Wafer Level Package
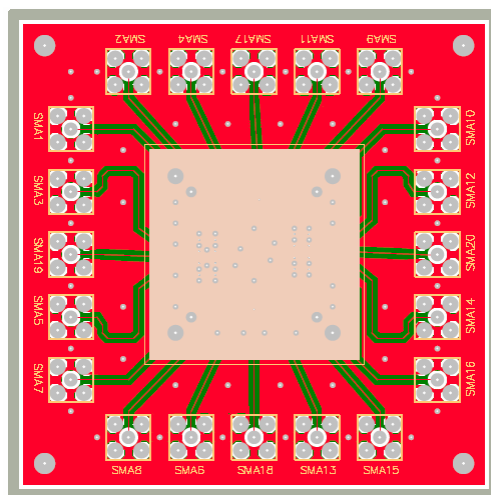
Fig. 6.3: PCB Top layer with SMA connector footprints. Elastomer mesh is the square sheet in the centre
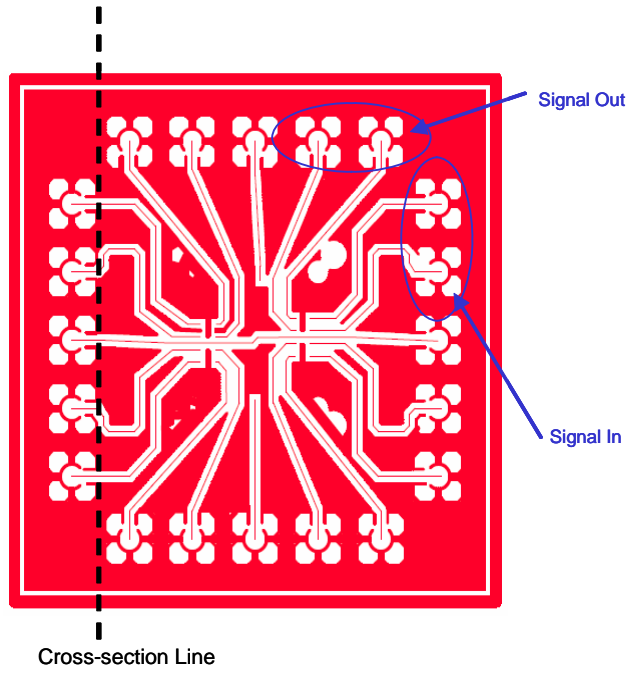
(a)
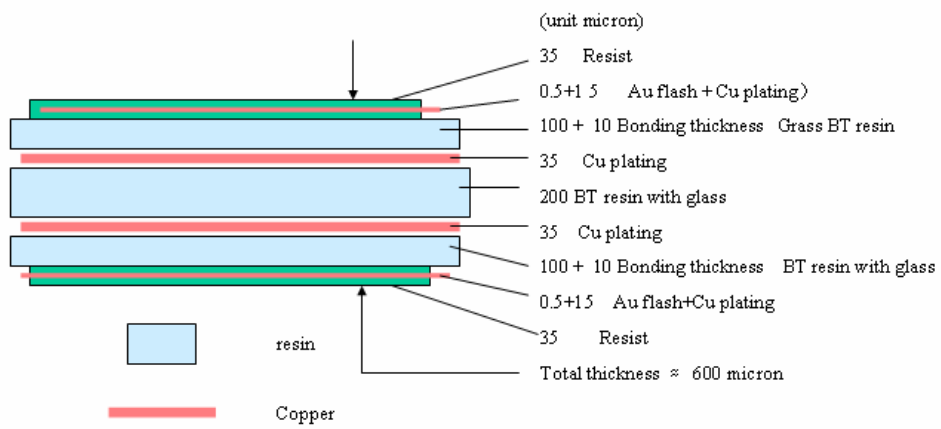
(b)

Fig. 6.4: PCB. (a) Signal layer and (b) Cross-Section

95

(a)

(b)
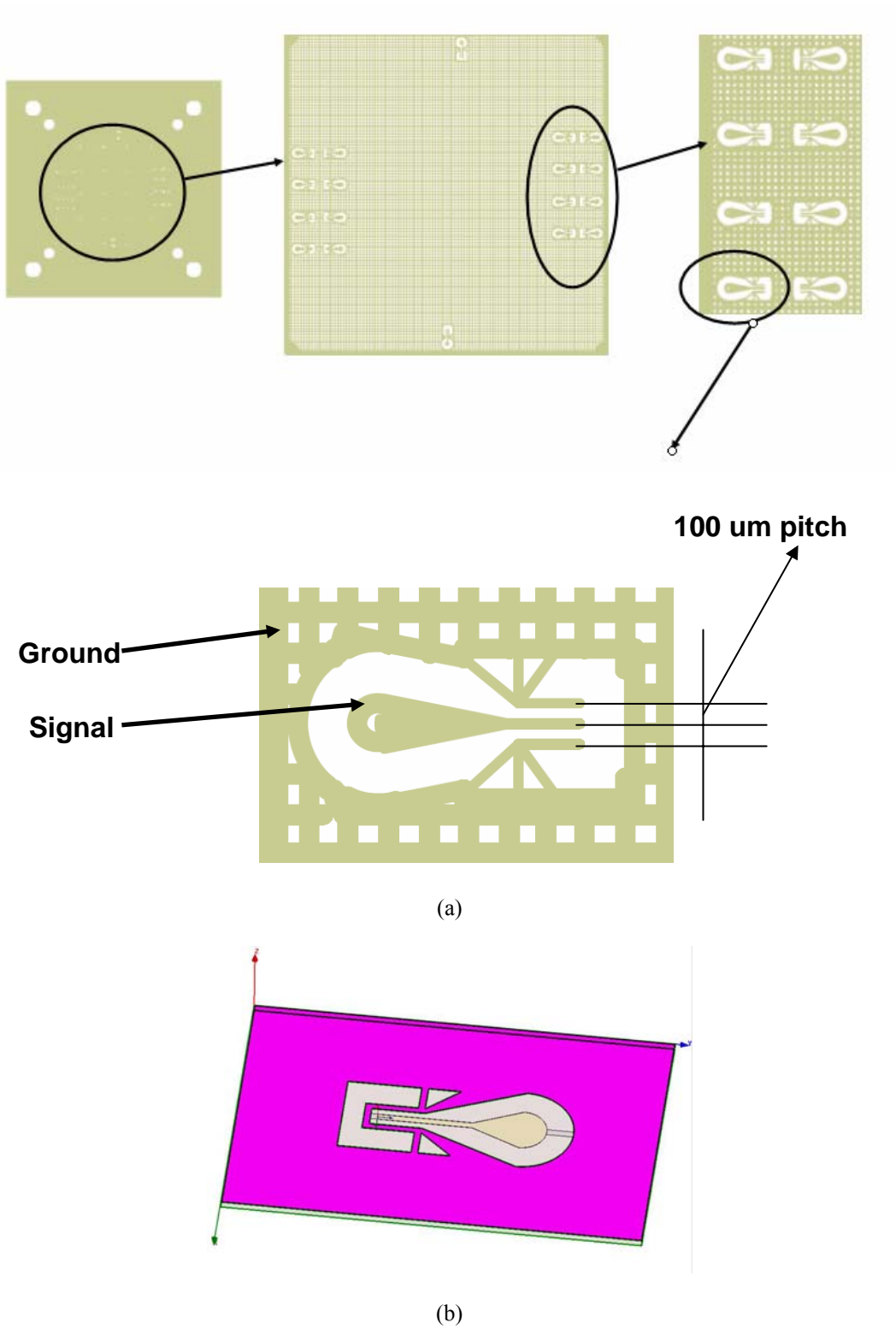
Fig. 6.5: Elastomer mesh shown with a magnified probe. (a) Physical structure and (b) Full-wave model
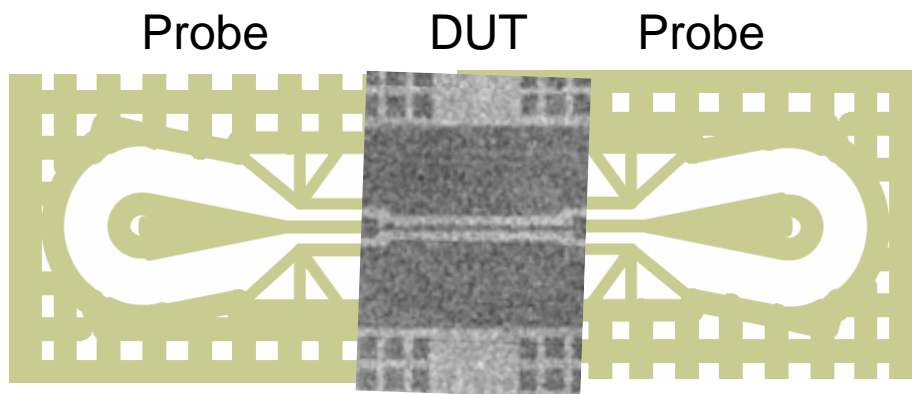
Fig. 6.6: Elastomer mesh with device under test
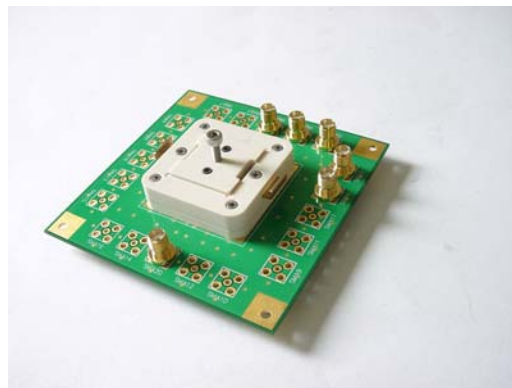
Fig. 6.7: Fabricated prototype test fixture
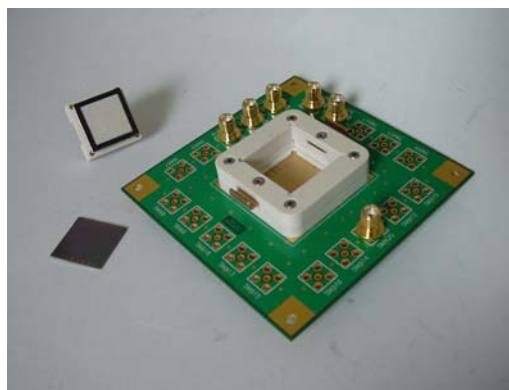
Fig. 6.8: Prototype test fixture components (mesh exposed)

The contact probes are made by screen printing the metallization lines on the mesh substrate as shown in Figs. 6.5 and 6.6. The metallization could be in the form of a plane to act as ground or power grid or in the form of mesh-coplanar probes that float in the sparse elastomer matrix. They could be densely populated to test fine pitch, high I/O density WLP devices. The elastomer mesh material has spaces into which metallization seeps in. This arrangement contributes towards the necessary compliance while maintaining low contact resistance over a large area. VNA based frequency domain measurements could be performed via sub-miniature version A (SMA) connectors installed on the multilayer PCB substrate. On the other hand, time domain functional test could be implemented by having test circuits [105] directly on top of the PCB in the vicinity of the probe.

The multilayer PCB substrate is designed with 50 ohm transmission lines leading from the device under test (DUT) to SMA connectors for signal in/outs. The PCB is made of BT resin material that is usable up to 6 Gigahertz. Figs. 6.7 and 6.8 shows an illustration of the prototype test hardware. Elastomer mesh provides a compliant interface

between the chip (or wafer or WLP) and the multi-layer substrate. A diced WLP is placed inside the socket on the test hardware. Connectors surrounding the WLP are to be connected to measurement instruments. The SMA connector has a good electrical performance up to 18 Gigahertz. The coplanar transmission line on the substrate printed circuit board and the probe on the mesh offer efficient high frequency transmission.

6.2.2 Device Under Test

The WLP test sample is fabricated as a coplanar transmission line on a high resistivity silicon (2Kohm-cm). The layout of the test structure with a transmission line and square pads is shown in Fig. 6.9. The two pads are of size 75um X 75um.
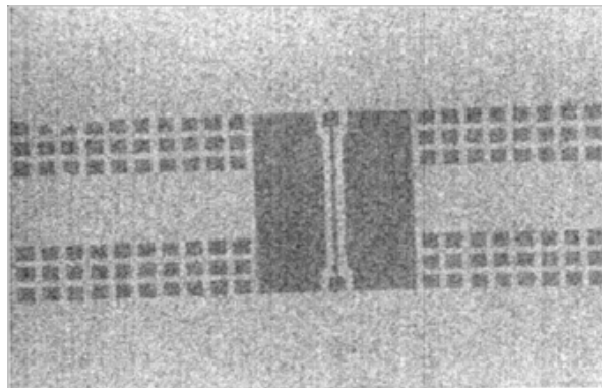
Fig. 6.9: X-Ray image of the DUT coplanar structure (top view)

On the WLP pad, the fabrication of the wafer-level Bed of Nail (BoN) copper column interconnect of Fig. 6.10 is grown as follows: On a given clean WLP pad, Ti/Ni/Au metal layer is first sputter deposited. The photo-resist is then applied and patterned for metal pads with daisy chains which are used for electrical testing, by using Ti/Ni/Au etching one by one and resist removal. Secondly, BCB dielectric polyimide is spun to passivate the daisy chains and pattern the dielectric layer using UV lithography to open the pads. Ti/Cu or Ti/Au seed layer is then sputtered. The bottom Ti layer is applied

99

to improve the adhesion between dielectric and Cu or Au. Then a thick photo-resist is spun, soft backed, UV patterned, and developed.
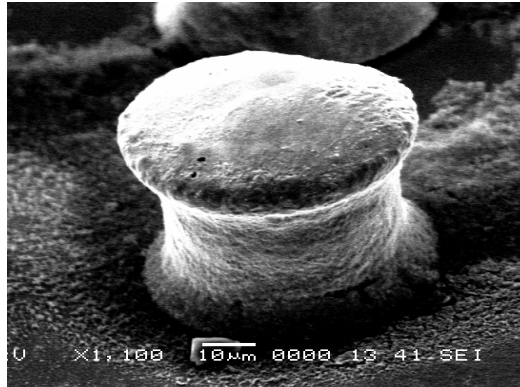
Fig. 6.10: SEM image of a fabricated copper column interconnect

The copper post is electroplated. The solder is then electroplated at the tip of the copper post for bump formation. Thick photo-resist is then removed and Ti/Cu or Ti/Au seed layer is etched away to complete the interconnect structure. Finally, solder is reflowed in N2 atmosphere . This fabrication process is based on photolithography and electroplating process which is compatible to the conventional integrated circuit (IC) fabrication and the fabrication is integrated into wafer-level processing as batch process. Additional masks are not needed as UBM mask can be used to pattern the photo resist for copper column deposition. After fabrication of BoN interconnects on the silicon wafer, the wafer is diced into individual dies and the die is flipped and assembled onto the test fixture for measurements.

6.3 Model of Prototype Components

6.3.1 WLP

The device under test (DUT) is independently measured with the standard air-coplanar probe (cascade microtech) and its S parameter results are used to derive the circuit model as discussed in Chapter 3. Due to fact that the electrical length of the tested geometry (about 900 microns) is much smaller than the operating wavelength (about 5000 microns), the lumped model suffices for this component. The equivalent circuit of the WLP transmission and the pads is depicted in Fig. 6.11.
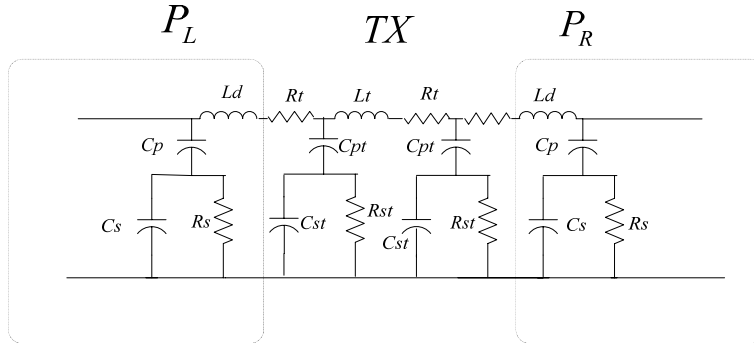
Fig. 6.11: Equivalent circuit of the WLP transmission and pads

6.3.2 WLP off-chip interconnect

The off-chip WLP interconnect used is a bed of nail copper column [106]. This interconnect is grown on the top of WLP pads. The physical geometry and the corresponding equivalent circuit of this interconnect are shown in Figs. 6.12 and 6.13 respectively. The equivalent circuit is again obtained from S parameter data from a bare WLP device and WLP with interconnect. Again, the small electrical length allows the use of a lump circuit representation of the interconnect.

101

The cylinders are modeled as a transmission line since the current flow through the cylindrical copper column is similar to that of a transmission line. The per-unit-length capacitance between two cylinders is calculated as [107]

$$C = \frac{\pi \varepsilon}{\cosh^{-1}\left(\dfrac{d}{2a}\right)}, \tag{6.1}$$

in Farads/meter where a is the radius of the cylinder, d is the center-to-center distance between two adjacent cylinders and ε is the permittivity of the material surrounding the cylinders.

The total capacitance of the cylinders is $2C$. Then the per-unit-length inductance is determined as

$$L = \frac{\varepsilon_r}{2C \times c_0^2}, \tag{6.2}$$

in Henries/meter where c_0 is the free-space light velocity and ε_r is the relative dielectric constant. The foregoing assumptions have been verified from 3D simulations with HFSS [108] and so we have used the same approach in our modeling of Fig. 6.13. In the T-network of Fig. 6.13, the component values are given by

$$L1 = L2 = \frac{L}{2}l \tag{6.3}$$

$$C1 = 2Cl \tag{6.4}$$

$$R1 = R2 = \frac{R}{2}l \tag{6.5}$$

where l is the length of the cylindrical column and R is the static resistance of the column.
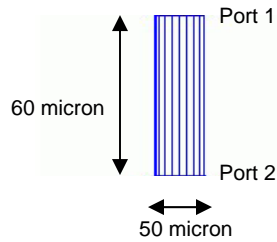
Fig. 6.12: Copper column interconnect geometry
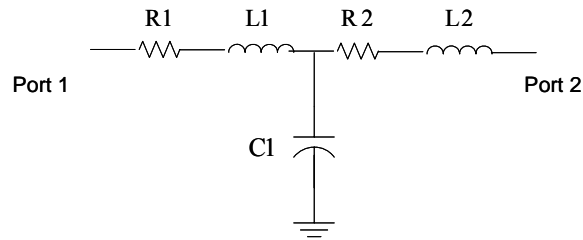
Fig. 6.13: Equivalent circuit of WLP interconnect copper column

6.3.3 Elastomer Mesh

The Model of elastomer mesh follows the presentation of Chapter 4. The material used has a permittivity of 2.86 and tangent loss of 0.002. Each probe location consists of three fingers that correspond to ground-signal-ground placed at a pitch of 100 microns. Gold metallization is used for the contacts as well as ground. The metallization lines are screen printed on the elastomer in the form of tapered GSG probes. The ability to fabricate small features with the same approaches that are used for silicon processing helps to deposit metal lines with the resolution of 40 micron line width and 100 micron pitch required in

the application. The thickness of the mesh is 50 microns. Thin mesh allows a two dimensional representation of the equivalent circuit. The equivalent circuit of the mesh without and with metallization and the probe tips are presented in Figs. 6.14, 6.15 and 6.16 respectively.
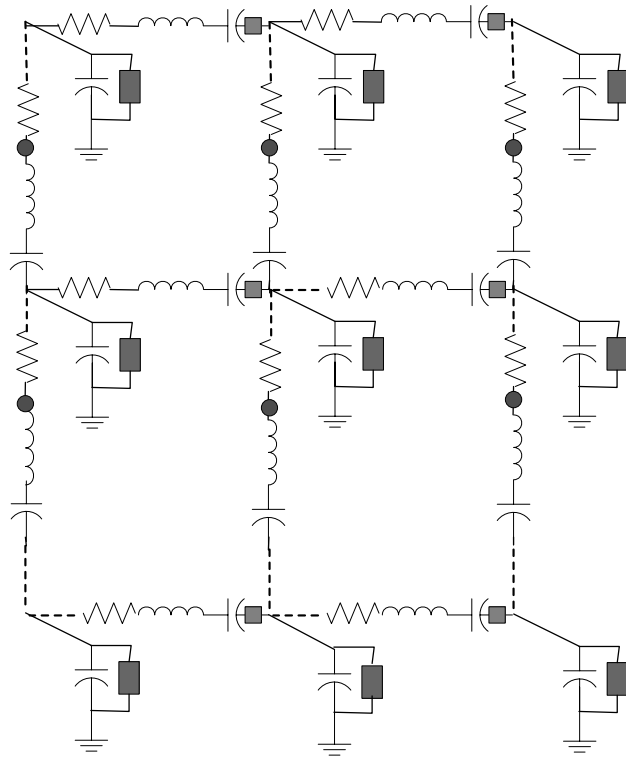
Fig. 6.14: Equivalent circuit model of Elastomer mesh plane
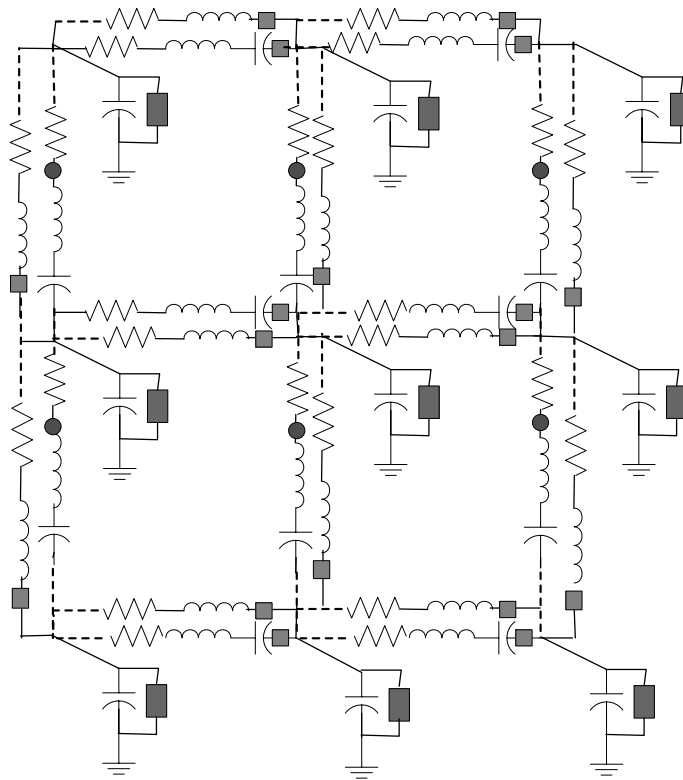
Fig. 6.15: Equivalent circuit for Elastomer mesh plane with metallization
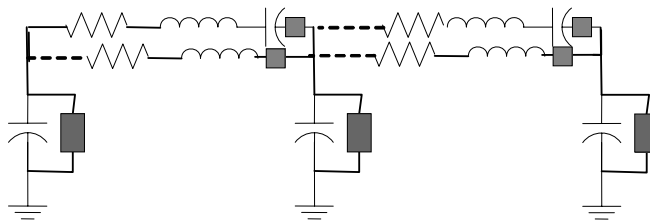
Fig. 6.16: Equivalent circuit for the mesh probe

6.3.4 Multilayer Substrate

The model for the multilayered geometry follows the formulation in Chapter 5. The dielectric material used is BT glass resin with permittivity of 4.4. Transmission line with 50 ohm impedance is laid on one side of the PCB. The line width is 200 microns. It connects SMA connector on exterior end with 40 micron diameter via in the other interior

end. The through via connects to the mesh probe on the other side of PCB. The mesh probe has a pitch of 100 micron and width of 50 micron. The hardware components modeled are shown in Fig. 6.17. The equivalent circuit of the ground plane, the multilayer interface and the vias are given in Figs. 6.18, 6.19 and 6.20 respectively.

Coplanar Line (200 micron)

Copper metal (15 micron)

BT Glass Resin (100 micron)

Copper metal (35 micron)

BT Glass Resin (200 micron)

Via (40 micron)

Copper metal (35 micron)

BT Glass Resin (100 micron)

Copper metal (15 micron)

Coplanar Line (50 micron)
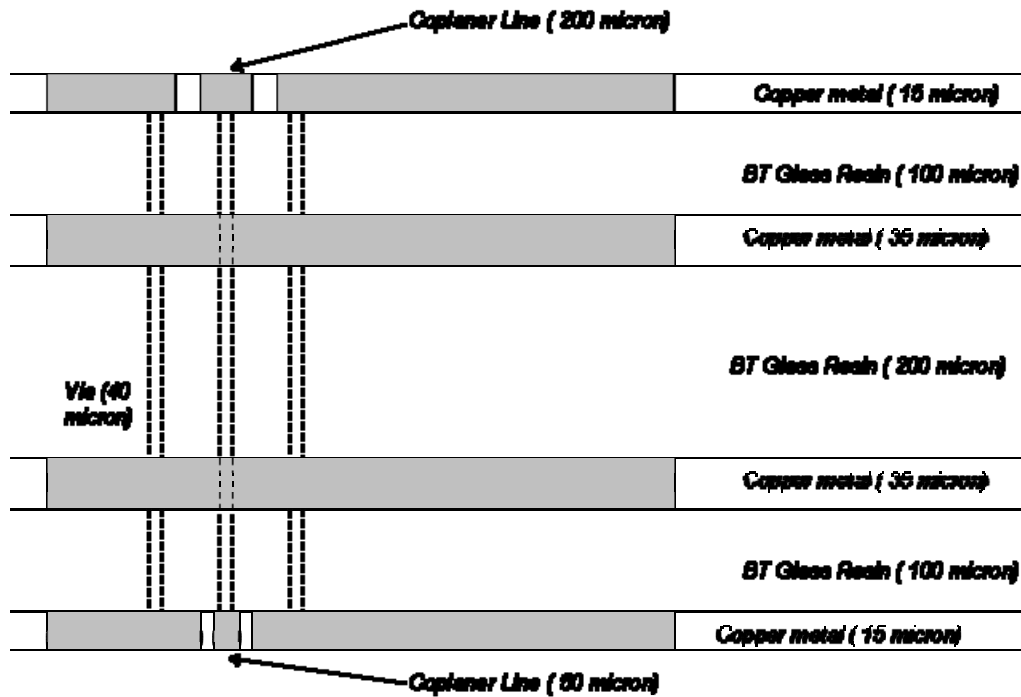
(a)
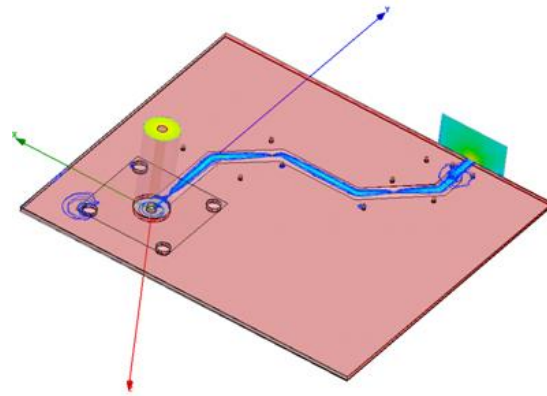
(b)

Fig. 6.17: Multilayer substrate geometry. (a) Cross-section and (b) Full-wave model
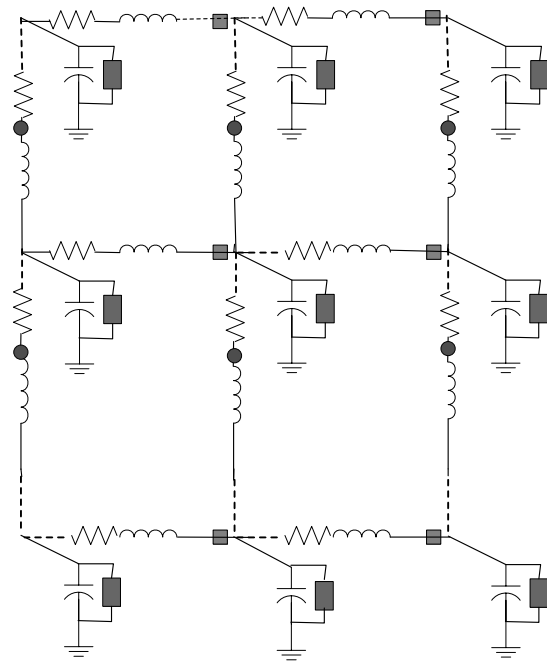
Fig. 6.18: Equivalent circuit for the PCB ground plane
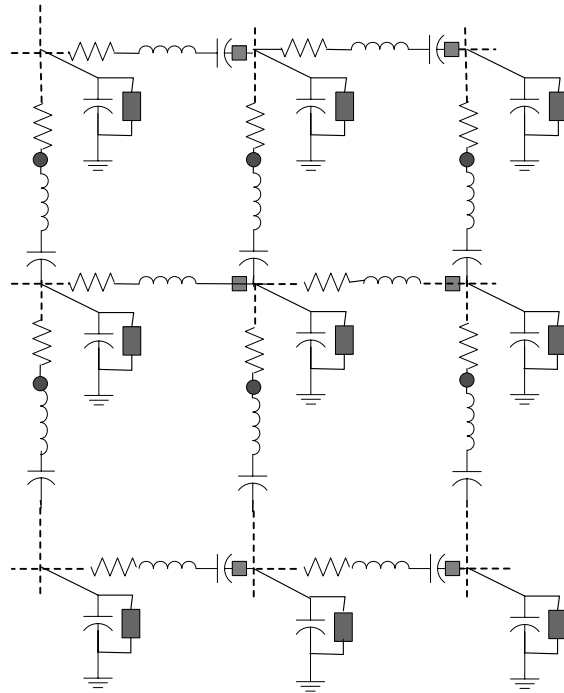
Fig. 6.19: Equivalent circuit at the multilayer interface
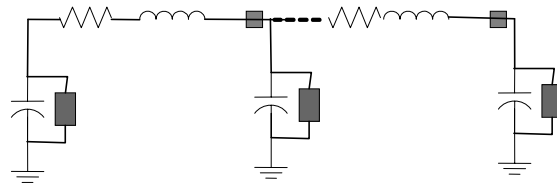
Fig. 6.20: Equivalent circuit for the PCB and coaxial via

6.3.5 System Level Model

Two forms of modeling, PEEC as well as full wave, are implemented at the system level.

In full-wave model, due to the presence of very small features of the interconnect which

is of the order of 50 microns and very large features of the PCB which is of the order of

20 centimeter, the problem size is found to be too big on the full-wave solver [108]

equipped with a computing resource of 2 GB of on-board memory and 2.8 GHz

processor speed. This constraint is alleviated by partitioning the hardware into smaller,

more manageable components such as the transmission line on multilayer PCB, SMA

108

connectors, elastomer mesh, WLP and interconnect. Each component is separately modeled. The signal path components consisting of the SMA signal-in connector, multilayer transmission line, via, elastomer mesh probe , WLP off-chip interconnect, WLP and then back to WLP off-chip interconnect, elastomer mesh probe, multilayer via, transmission line and SMA signal-out connector are combined into a system model.

In PEEC system model, the interactions are included when the component geometry is comparable to one-tenth of the operating wavelength of interest, that is 6000 microns for 5 GHz. Thus the WLP transmission and the interconnect are treated as lumped elements. The multilayer substrate and elastomer mesh interactions are treated as PEEC elements with inductive and capacitive couplings between them. Since the couplings are resolved in the three directions, only components in the same direction are coupled. For computing return loss, circuit scaling, as described in Chapter 2, was applied.

The PEEC and full-wave system level model is represented in Figs. 6.21a and 6.21b respectively. The PCB and the SMA connectors are seen to have a major influence on the electrical performance of the hardware. The elastomer probe tips, WLP and interconnect contribute less towards signal degradation due to their small dimension and low loss.

(a)

110
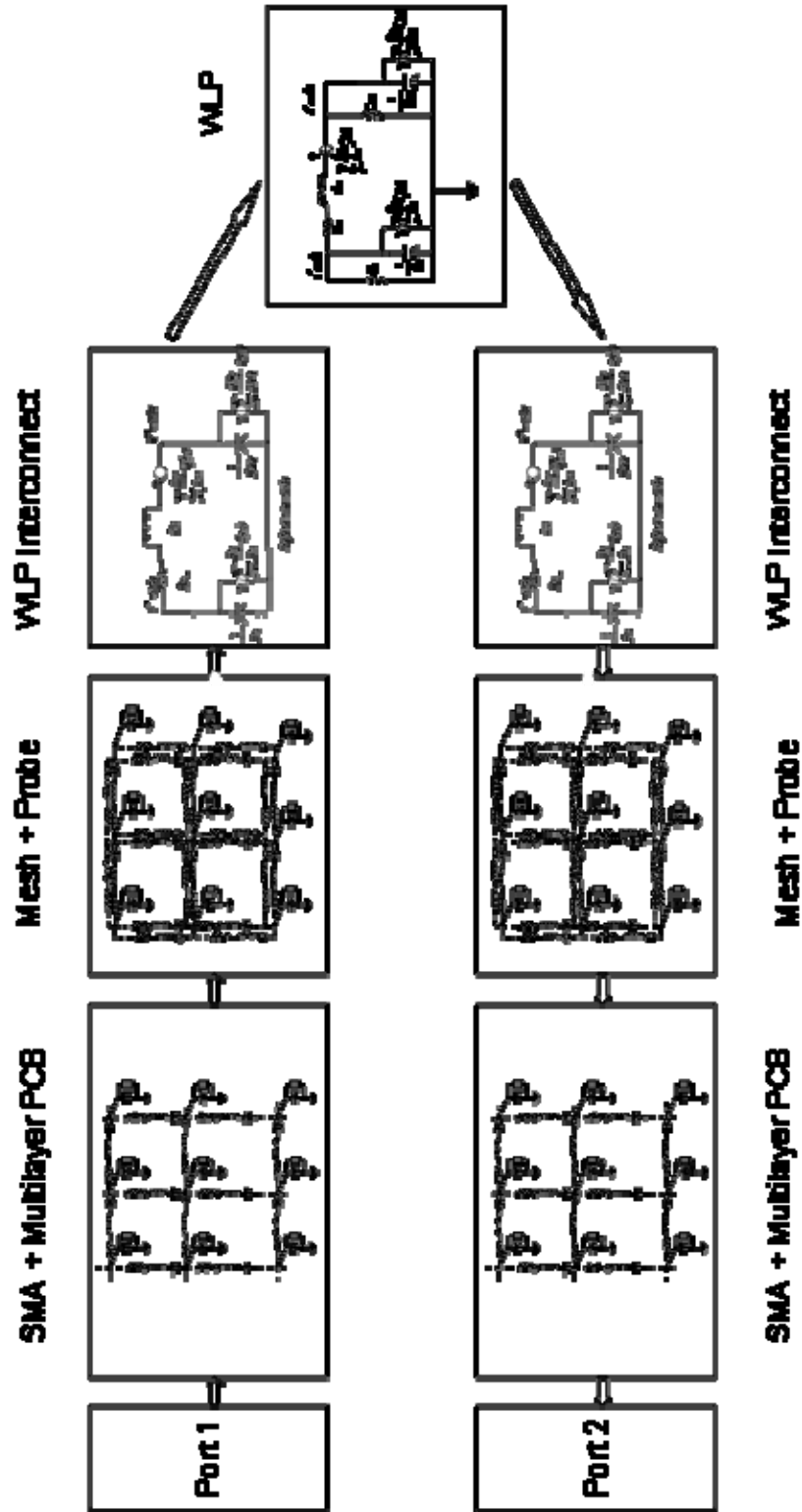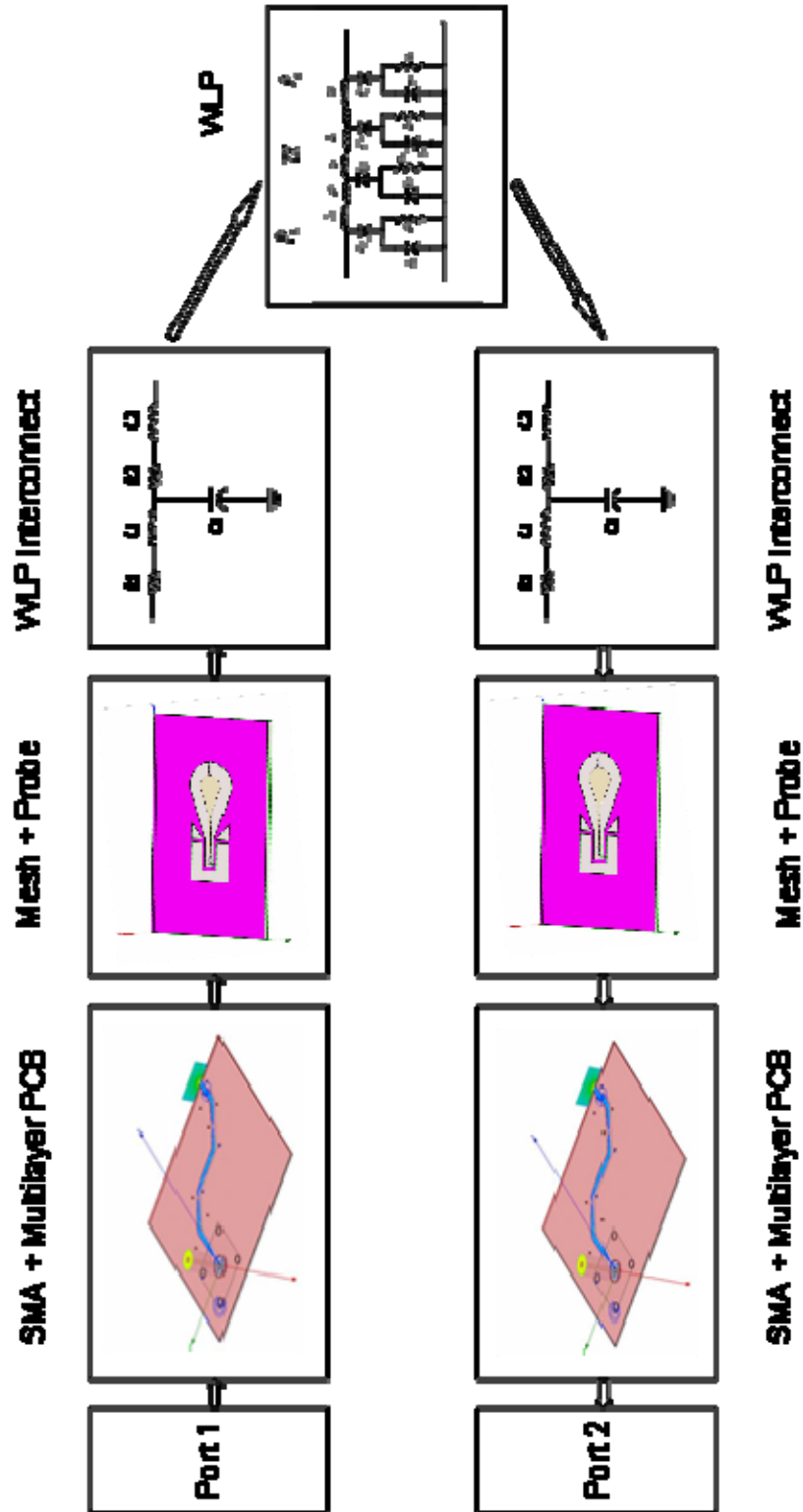
(b)

Fig. 6.21: System level (a) PEEC model and (b) Full-wave model

6.4 Test Results

The system level measurement and model simulation results for the prototype and WLP with copper column interconnect are shown in Figs. 6.22 and 6.23. The complete system consisting of two SMA connectors, coplanar transmission lines on the PCB, elastomer mesh and the WLP with interconnects as a whole performs up to 2 GHz with an insertion loss less than 1.5 dB. For 5 GHz performance, the insertion loss is about 3dB. The transitions at the vias, SMA connectors and the mesh significantly contribute to the loss.

Figs. 6.22 and 6.23 contain the simulated results of PEEC and full-wave model of the prototype along with measurements. There is a fair agreement between the two models up to 2.5 GHz but above 2.5 GHz, the PEEC model is closer to the measurement than the full-wave model. This deviation is attributed to the partitioning of the prototype into blocks in the full-wave model where the significant interaction between input and output blocks is ignored.

A relatively good agreement of insertion loss and return loss between PEEC model and measurement is found. At the lower frequency range up to 3 GHz, the insertion loss error is less than 4%. The error is within 8% in the frequency range up to 5 GHz as seen form the Table 6.2. Return loss is found to be better than 10 dB up to 2 GHz and 8dB up to 5 GHz.

With optimization of the geometry and material selection through the model, further performance improvement could be obtained. Particularly, the transitions have to designed carefully to minimize the reflections and to optimize the matching of the impedance and the modes.
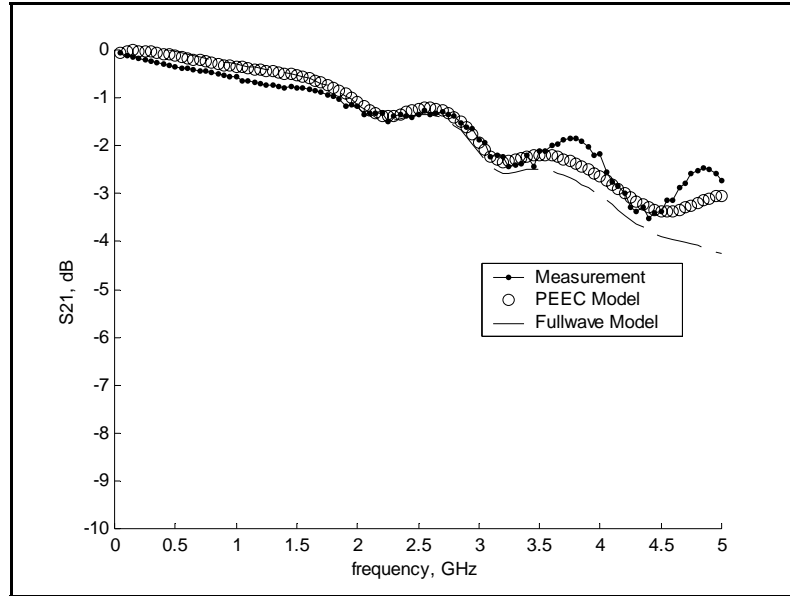
Fig. 6.22: Insertion loss measurement of WLP with single copper column
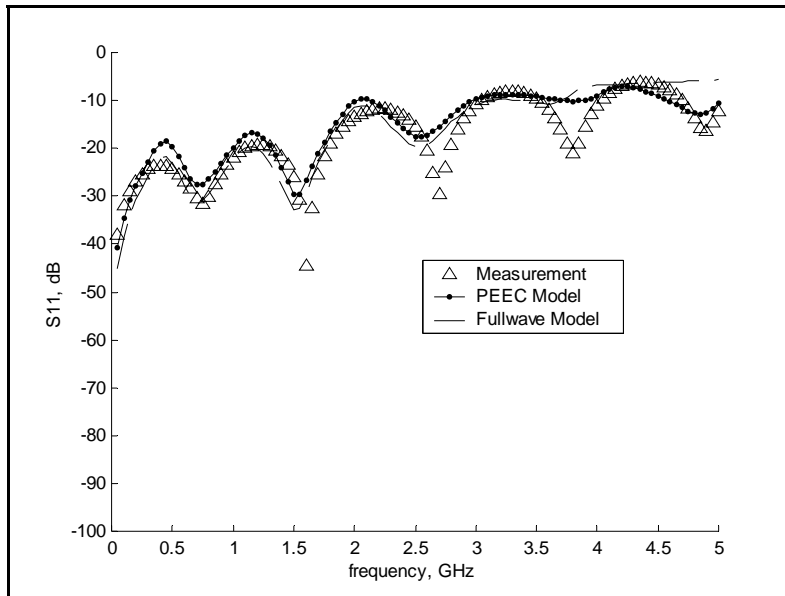
Fig. 6.23: Return loss measurement of WLP with single copper column

Table 6.2: S_{21} measurement and model data

Frequency, GHz	|S21| Measurement	|S21| Simulation	Error %
0.25	0.976	0.997	-2.06
0.50	0.960	0.986	-2.64
0.75	0.949	0.973	-2.42
1.00	0.936	0.961	-2.55
1.25	0.919	0.952	-3.54
1.50	0.911	0.940	-3.14
1.75	0.898	0.920	-2.39
2.00	0.873	0.883	-1.01
2.25	0.842	0.852	-1.13
2.50	0.855	0.869	-1.46
2.75	0.857	0.859	-0.20
3.00	0.805	0.801	+0.51
3.25	0.755	0.765	-1.30
3.50	0.784	0.777	+0.96
3.75	0.807	0.766	+5.22
4.00	0.778	0.738	+5.25
4.25	0.684	0.702	-2.51
4.50	0.678	0.677	+0.04
4.75	0.742	0.688	+7.28
5.00	0.730	0.705	+3.51

WLP devices with different WLP off-chip interconnects have been measured. Figs. 6.24 and 6.25 show the insertion loss and return loss the prototype with multiple copper column[109]. Figs. 6.26 and 6.27 show the insertion loss and return loss the prototype with solder bumps. In both these interconnects, the contact between the mesh probe and the interconnect are poorly formed. This is likely due to the much larger curvature of the interconnect tips as compared to single copper column interconnect. The larger curvature of the bump reduces the contact area of the test probe. So a signal degradation with insertion loss of 1 dB is observed even at 100 MHz. Nevertheless an insertion loss performance of about 3 dB up to 3 GHz is seen in both cases.
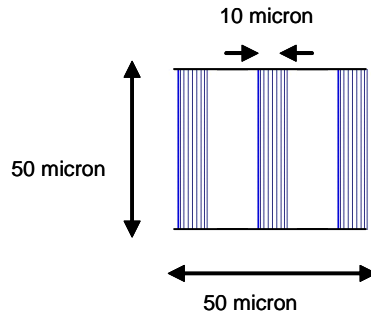
Fig. 6.24: Multiple copper column schematic
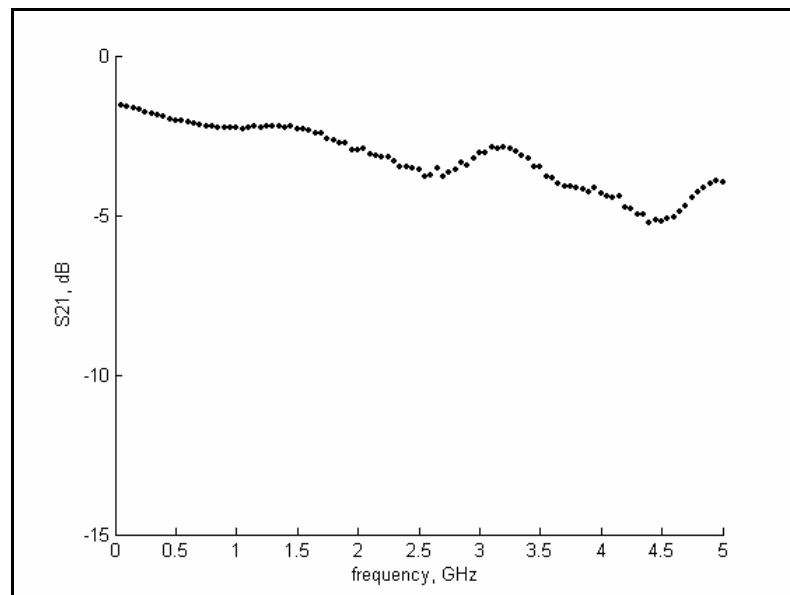
(a)
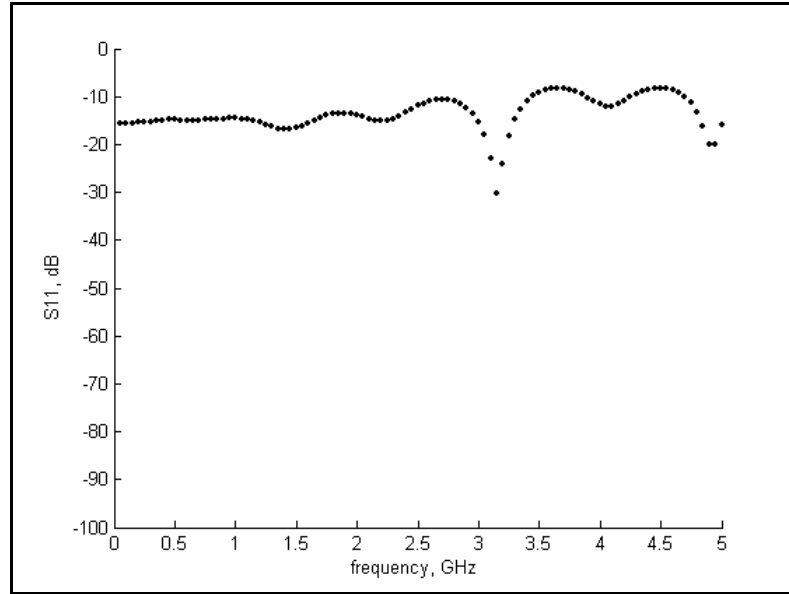
(b)

Fig. 6.25: (a)Insertion loss and (b) Return loss measurement of WLP with multiple copper column

50 micron

50 micron
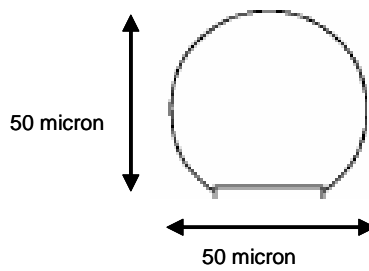
Fig. 6.26: Solder bump schematic
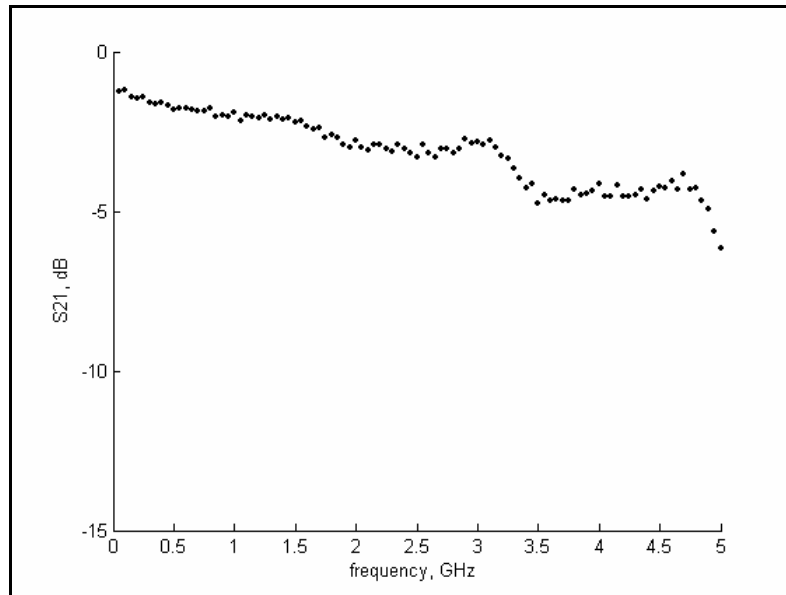
(a)
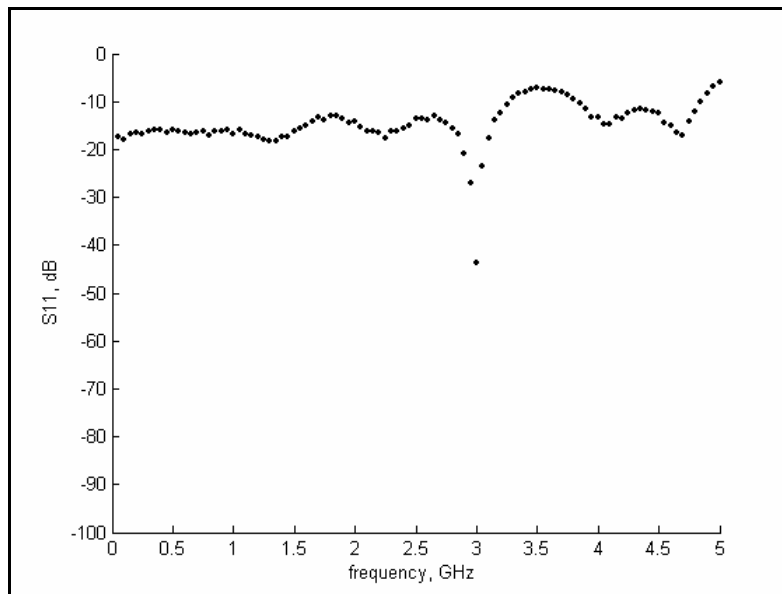
(b)

Fig. 6.27: (a) Insertion loss and (b) Return loss measurement of WLP with solder bump
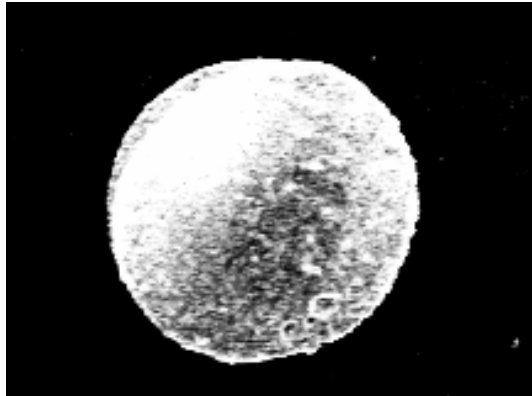
Fig. 6.28: SEM image of copper column interconnect: Before probing

Probe Mark
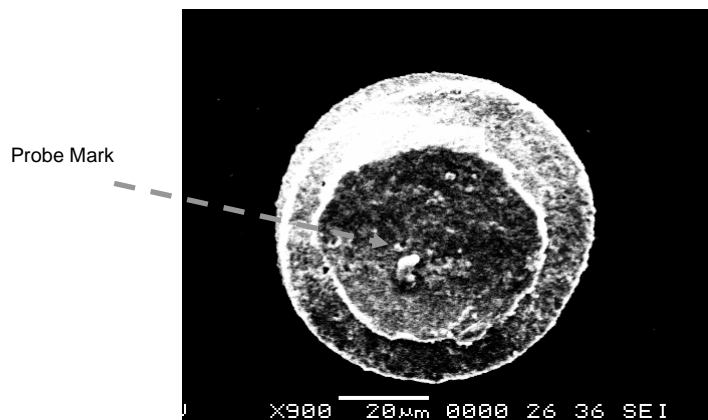
Fig. 6.29: SEM image of copper column interconnect: After probing

Figs. 6.28 and 6.29 show the top view of the single copper column interconnect before and after probing respectively. The top of the copper column has been coated with solder with thickness of 10 micron. The probe mark on the soft solder is visible in Fig. 6.29.

6.5 Adaptation of Hardware for Functional and Structural Test

6.5.1 Functional versus Structural Test

The normal approach to electrical testing of WLPs is to exercise the circuit in such a way that all possible functions are performed under all test conditions such as different frequencies and different loads. If the correct output is obtained every time, then the circuit is fault-free. This approach is called functional testing, because it actually verifies that the circuit performs the intended functions. The circuit is exhaustively tested by exercising all possible combinations of input stimuli. The drawback of this approach is that the high degree of complexity of present day VLSI devices makes exhaustive functional testing impractical. The test time would simply grow exponentially. Alternative test methods such as structural testing are sought to alleviate the test time complexity.

Structural testing directly confirms that the circuit is fabricated correctly according to design. When coupled with accurate and complete modeling and simulation, structural testing can be an efficient way to assure that the intended functions will also be performed. Structural testing can be more efficient than functional testing because the circuit can be partitioned into simpler sub-circuits that are checked independently from the other sub-circuits. This technique allows very complex circuits to be tested piece-by-piece. However, it does not directly demonstrate the circuit's functionality. Effects such as corruption of signals by noise can be missed with purely structural tests, because structural tests are usually performed at low frequencies. Therefore, structural tests are complemented by non-exhaustive (partial) functional tests performed at full operating speed.

6.5.2 High Speed Signal Generation and Detection for Functional Test of Fine Pitch and High Pin Count WLP Devices

For proof of elastomer mesh-coplanar probe concept, the prototype used SMA connectors on the prototype to apply excitation signals for VNA measurements as shown in Fig. 6.30. However for functional testing of devices at wafer level [110], the high frequency signal can be generated by multiplexing a low frequency clock from an external RF source in a Field Programmable Gate Array (FPGA) chip or a voltage controlled oscillator (PLL test). The signal integrity is maintained by keeping the high frequency signal source very close to the probe test point as shown in Fig. 6.31 and 6.32. Since many signal sources can be placed very close together, it is possible to concurrently perform high speed, fine pitch probing over large pin counts and silicon area. The low frequency signal such as a reference clock, test control signal, power line can be placed away from the test site. The clock distribution, timing generation, data multiplexing, and driver/receiver buffering that are handled in the support logic chips can be placed surrounding the signal generation circuits.
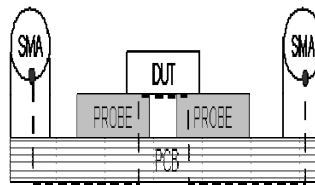
Fig. 6.30: Test hardware for VNA measurement (dashed lines indicating signal path)
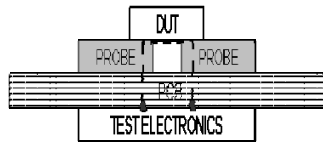
Fig. 6.31: Functional test hardware (with dashed lines indicating signal path)
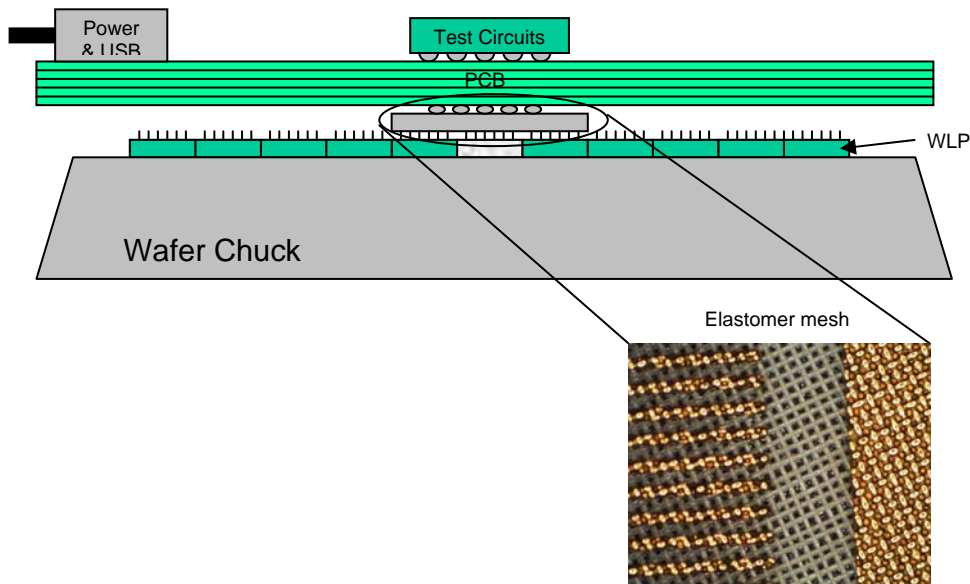
Fig.6.32: Wafer probe setup with functional test hardware

Contact resistance is frequency dependant and it can degrade signal quality severely especially at high frequencies. So even a good interconnect may not get the signal across the device. It is then desirable to have the test signal generation and detection to be built into the DUT chip itself (Built-In Self Test) to minimize the problem due to contact resistance and also transmission line effects. It is thus possible to test the on chip circuitry at speed while the interface only operates at low speed. On the other hand, closeness of the wire traces makes the circuits vulnerable to strong coupling of the

noise in the high speed clock lines. So jitter tolerance must also be built-in such designs [105].

Functional test electronics circuits could be packed on one side of the multi-layer substrate while on the other side could be connected the compliant mesh interposer sheet to connect between low pitch wafer dies and high pitch PCB circuits that have pin electronics. This arrangement helps to pack about 1000s of test probes per square centimeter. The test probe density could be increased to 10,000 per square centimeter by forming metal dots on the interposer sheet and implementing the space transformation (tapering the probe) in the multi-layer substrate. When the number of signal points in the WLP device grows very huge, that is, of the order of 10,000 pins per square centimeter, there is no room on the compliant sheet itself to do space transformation. This has to be done in the multi-layer substrate.

6.5.3 Eye Diagrams

The prototype system has been tested with pseudo-random binary bit stream at 2.5 Gbps (gigabit-per-second), 5 Gbps and 8 Gbps as a further verification of its functional performance and very good results have been obtained. In the Figs. 6.33 - 6.35, the lower eye diagram is the output of the source signal, and the upper eye is the same signal after passing through the test prototype socket. The signals look very good below 5 Gbps and still show (small) eye openings at 8 Gbps. In each case there is a degradation of the signal in edge-rate and signal swing, but this is to be expected especially at the higher speeds.
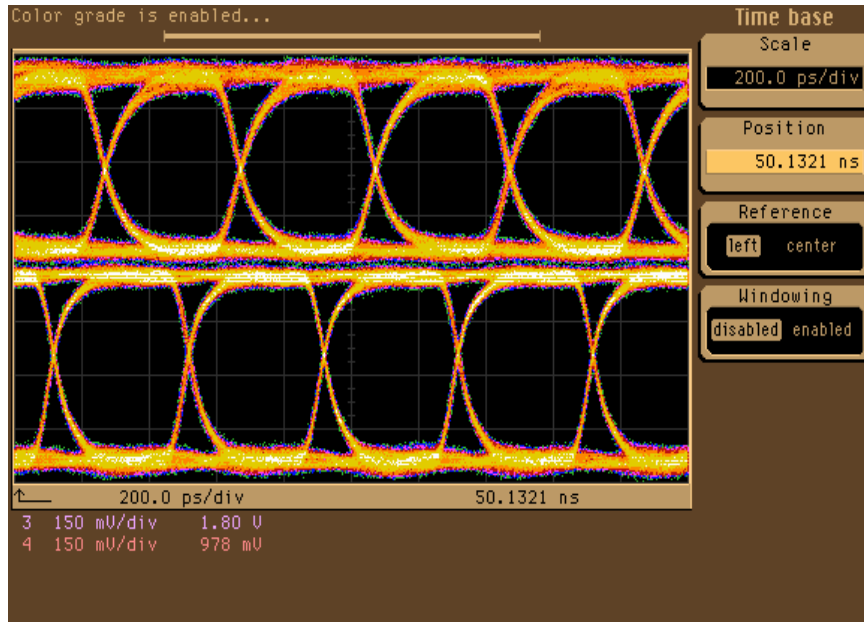
Fig.6.33: Eye diagram at 2.5 Gbps
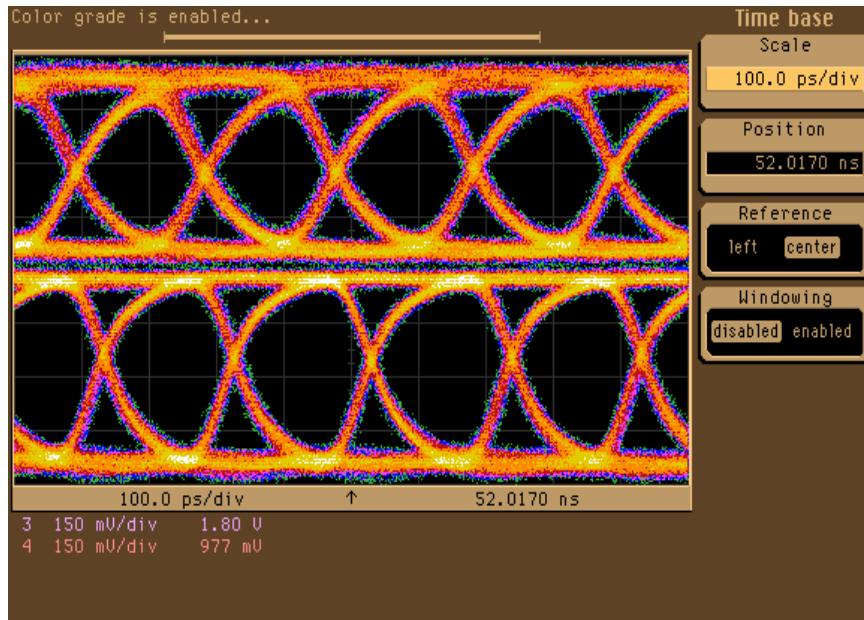
Fig.6.34: Eye diagram at 5 Gbps
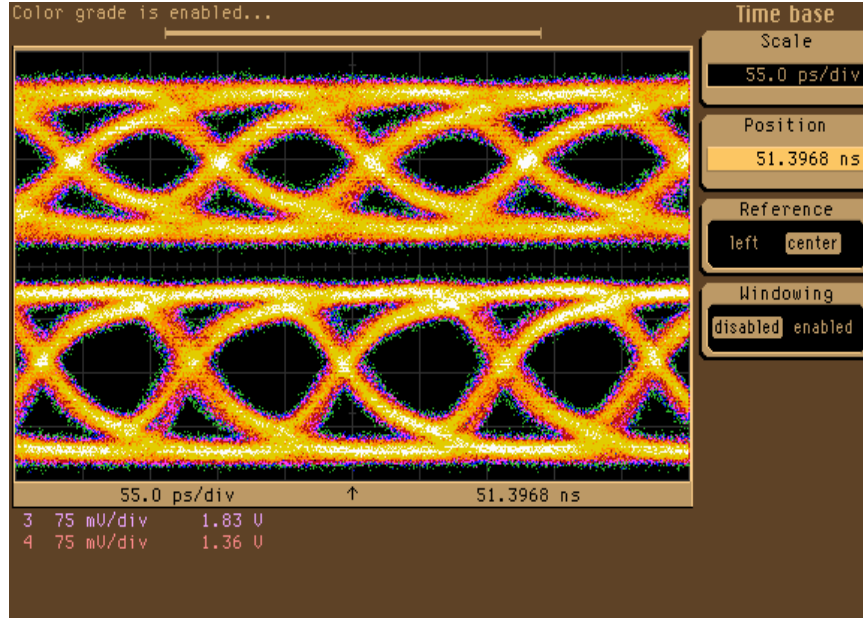
Fig.6.35: Eye diagram at 8 Gbps

6.6 Discussions

PEEC modeling has been applied for implementation of the new microwave probing concept using elastomer mesh which demonstrates the possibility of testing high I/O density wafer level packages at multi-gigahertz frequencies. A prototype test interface was designed and developed to verify the concept by using high resistivity silicon samples containing coplanar transmission lines with WLP interconnects. Modeling, simulation and measurements were performed and found to be in good agreement up to 5GHz. The operating frequency range is extendable beyond 5 GHz by using microwave laminate materials, coaxial vias in place of normal vias on PCB and using end-launch SMA connectors in place of vertically mounted connectors. Eliminating

124

connectors with programmable gate arrays placed close to the probes could improve the test performance further.

The mesh material is amenable to fabrication over a large area of 8 or 12 inch wafers with pitch resolution of 40 microns besides excellent compliance properties. So this probing concept is applicable to full-wafer parallel test which can provide phenomenal throughput in functional testing of fine pitch, high pin-count wafer level devices.

The new compliant elastomer mesh probe and test methodology described in this Chapter has the following advantages over the related conventional wafer test approaches:

1. The new designs are demonstrated for test applications of both the fine pitch, high pin count flip chip type of packages and for complete wafer testing, up to 5 GHz range and beyond.

2. There are no level transitions in the interposer elastomer mesh sheet structure. This reduces high frequency signal reflections significantly.

3. The stress due to CTE of the PCB and the wafer is absorbed by the elasticity of the interposer sheet. Unlike the spring contacts for compliance, the sheet itself provides the required compliance. Since the interposer sheet is so thin (between about 30 and 300 microns), it has a near 2D structure, thus providing much better contact stability.

4. By provision of mesh formation in the interposer sheet, the local relaxation during heating releases the thermal stresses and thereby helps to achieve wafer level test and burn-in together.

CHAPTER 7

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORKS

7.1 Concluding Remarks

In this thesis, the efficient PEEC models for lossless and lossy homogeneous media, the efficient PEEC model for conducting media with dielectric mesh and the efficient PEEC model for conductors with multilayers are derived. These models are successfully applied for the development and realization of a microwave probing hardware for wafer level package test at multi-gigahertz frequencies, under the tight geometrical constraints of fine pitch (of the order of 100 micron) and large device pin counts (of the order of thousands).

The PEEC method is chosen for its advantages such as the efficiency to solve large scale problems, the flexibility to model some components of the system in greater detail while modeling other component crudely with certain tolerance, the facility to solve problems which have an electromagnetic and circuit parts, and the applicability in the frequency domain as well as time domain.

The PEEC modeling in a homogeneous lossless medium is first investigated. In micron size multi-conductor geometries, the resistance values are quite small, while the reactance values are relatively large at GHz frequencies. This huge spread in the network component values leads to poor results from circuit simulation using SPICE with errors in return loss values (S_{11}) as high as 50%. Conventional linear techniques like impedance scaling and frequency scaling [56] are not enough to handle this problem since this does

not improve the matrix condition. We have applied a scaling technique based on the approximation of BCHD series [65]-[66] to counter this problem. The improvement of the matrix condition comes about through the reduction in the stiffness of the differential equation system. The usefulness of technique has been demonstrated by improved accuracy in the prediction of scattering parameters at high frequencies through SPICE simulation of the PEEC model of the stripline structure. The magnitude errors are less than 4% for S_{11}. The phase errors are better than 10 degrees for S_{11} in the frequency range of 6 to 10 GHz.

Modeling of lossy substrates is studied in Chapter 3. Two approaches, namely one based on PEEC modeling of lossy silicon substrate using the theory of complex images while another lumped model based on measurements, are implemented. Due to the fine pitch (100 micron) nature of the geometry, relatively small number of circuit elements is required for lump model. Both the PEEC and measurement based lumped circuit models have been found to agree well in the representation of lossy silicon substrates. The models are verified using a square pad structure, built with 50 ohm transmission line on high resistivity silicon over a wide operating frequency range of 1GHz to 20GHz.

The PEEC model in a dielectric mesh medium with metallization is then derived. Dielectric meshes are specifically considered for modeling due to their importance as probes in WLP test. The mesh material is chosen for fabrication of test probes to provide good vertical compliance, low contact resistance and efficient geometry for high frequency signal transmission. The equivalent circuit for the mesh is constructed by considering the conduction current and the displacement current through separate partial inductors. The mixture of metal particles and the dielectric material gives additional

polarization effect on charges inside the metallic inclusion. It amounts to perturbation of the local electric field in the metal by the polarization vector. This term is included to the homogeneous EFIE in order to compute the fields. A coplanar mesh transmission line has been chosen as a test case. The model and the measurement of the insertion loss and return loss are found to be in close agreement.

Since the development of the test interface is aimed at handling I/O (input/output pins) density of thousands in an area of one square centimeter, it is essential to introduce multiple layers for the redistribution of large number of signal lines. Typically, thrice the number of signal pins is required for the total WLP because about two-third of the pins are meant for power and ground. Hence, the Chapter 5 has addressed a method to extend the PEEC model to the case of multilayer dielectrics by treating the dielectric interfaces in terms of an interface function analog of two-body interaction. The boundary between two different dielectrics is treated as a new region to develop the interface function. The interface function is subsequently used to calculate the capacitances and inductances of interface surface cells. The method is first verified, using a microstrip to evaluate the quasi-static capacitance, with the method of Wheeler. It is then extended to the PEEC formulation and applied to coupled microstrip line filter with multi-layered dielectrics through the convolution of the interface function and the source function with pulse basis in the time domain. The results are compared with that of the method of moments. Good agreement is found in the prediction of resonant frequencies and S-parameters.

The PEEC models of the different subsystems of the multi-gigahertz test interface are combined towards the physical realization of the prototype. The prototype test interface incorporates a novel concept where a combination of a multi-layer substrate and

compliant dielectric mesh interposer sheet are used in designing a coplanar wave-guide transmission structure. The combination of multi-layer substrate and compliant interposer sheet results in an effective fine pitch, high density I/O test methodology that can test future high pin count, fine pitch wafer dies and VLSI chip scale packages at microwave and RF frequencies with less reflection and less insertion loss. The built-in compliance of the interposer provides for the thickness variation of the DUT thereby maintaining reliable electrical contacts over a wide area of square centimeters. Two dimensional array of compliant probes provides for mechanical stability while also making good electrical contact without breaking the device under test or the probe.

The complete system consisting of two SMA connectors, coplanar transmission lines on the PCB, elastomer mesh and the device under test as a whole is verified through both prototype measurement, and the PEEC and the full-wave model simulations. A close agreement of the insertion loss and return loss data over the frequency range of 1 to 5 GHz demonstrates the validity of PEEC modeling approach as well as the efficacy of the prototype for multi-gigahertz test applications.

7.2 Suggestions for Future Works

As noted in the beginning of this thesis, there are many areas which are currently being explored in the study of PEEC modeling method and its applications. The focus of this thesis has been on the derivation of PEEC method for cases of homogeneous and inhomogeneous media and geometries that are of importance for the development of a high frequency test interface for fine pitch wafer level packages. This final section discusses a number of other topics in PEEC modeling for test interface development

which are of interest for much higher frequencies and smaller sizes than that considered in this thesis.

7.2.1 Modeling Intermediate and Far Field Effects

Current PEEC models mostly work by discretizing the given geometry into sub sections and deriving the circuit elements of the individual sections. They ignore the surrounding spatial medium. While this is acceptable for near field problems in the low gigahertz frequency range, it may not suffice at the higher end of the microwave spectrum. To improve the model accuracy at higher frequencies, the intermediate and the far field effects need to be accounted for.

An obvious option to solve the problem above is to discretize the space as well, and include it into the existing PEEC models with the result that the problem size gets rather large. The problem size could be handled by truncating the infinite lattice to the required accuracy. Because of the symmetry and uniformity of space, the models could exhibit faster asymptotic convergence.

For instance, in the case of a three dimensional cubic lattice of impedances (with each arm having unit value), the near neighborhood impedance value can be given by the lattice Green's function [104, 105] as

$$Z_{\ell,m,n} = \int_0^\pi \int_0^\pi \int_0^\pi \frac{dxdydz}{\pi^3} \left[(1 - \cos(\ell x)\cos(my)\cos(nz))/(3 - \cos(x) - \cos(y) - \cos(z)) \right]$$

In the special case of the simple cubic lattice, the limiting value for $Z_{\ell,m,n}$ as $|\ell^2 + m^2 + n^2| \to \infty$ is exactly calculable. The asymptotic value is

$$Z_\infty = \frac{4}{\pi^2} (18 + 12\sqrt{2} - 10\sqrt{3} - 7\sqrt{6}) \times \left(K((2 - \sqrt{3})(\sqrt{3} - \sqrt{2})) \right)^2$$

where *K(k)* refers to a complete elliptic integral of the first kind of modulus *k*. Evaluating the numerical value for this expression gives $Z_\infty \approx 0.50546$. The nearest neighbors have an equivalent impedance of 1/3 and an infinite distance has an equivalent impedance of about 0.5055. All intermediate distances must have an equivalent impedance between these two values since the equivalent impedance function rises monotonically with radial distance.

Depending on the accuracy needed, an equivalent near neighbor impedance value can be used as a termination impedance in the radiative PEEC models. Due to the close proximity, the near neighbor interaction could be considered without delays.

7.2.2 Modeling Nano-Scale Size Effects

Quantum manifestations of classical systems are expected when the circuit dimensions reach the nano and sub-nano scales [113]. For instance, in sufficiently flat microwave resonators, Maxwell's equations reduce to the Schroedinger equation for a free particle. The classical electromagnetic cavity is characterized by the stationary Helmholtz equation

$$\nabla^2 \mathbf{E} = -k^2 \mathbf{E} \tag{7.1}$$

where $k = \dfrac{2\pi f}{c}$, f is the frequency in Hz and c is the velocity of light in meters per second. The electric field **E** vanishes due to the Dirichlet boundary condition. On the other hand, the quantum oscillator cavity is governed by the stationary Schroedinger equation

$$\nabla^2 \mathbf{\Psi} = -k^2 \mathbf{\Psi} \tag{7.2}$$

where $k = \sqrt{\dfrac{2mE}{h^2}}$, m and E denote the mass and energy of the particle respectively.

The wave function Ψ also vanishes at the boundary due to the infinite potential well. In the case of a sufficiently flat cavity, equation (7.1) and (7.2) become identical and have identical eigenvalues k^2 and eigenfunctions $\mathbf{E}$ and Ψ respectively.

In the case of one-dimensional system such as copper nanowire, the quantum effect begins to manifest when the wire size reduces to below 50 Bohr radii. (One Bohr radius = 0.529 Angstroms). Since the macroscopic properties of the circuits such as conductivity, capacitance and inductance depend on the Fermi energy, an accurate evaluation of the circuit elements can be possible only when the quantum effects on the changes in Fermi energy are taken into account. This is an area with a lot of scope in the emerging nano and bio-electronic circuits and systems. Appendix D derives the size effects on Fermi energy for one dimensional copper nanowire system.

REFERENCES

[1] R. Tummala, *Fundamentals of microsystems packaging*, NewYork, McGraw-Hill, 2001.

[2] A.E. Ruehli, "Equivalent Circuit Models for Three-Dimensional Multiconductor Systems," *IEEE Transactions on Microwave Theory and Techniques,* Volume: 22, Issue: 3, pp. 216 -221, March 1974.

[3] J. Jayabalan, B.L. Ooi, M.S. Leong and M.K. Iyer, "A scaling technique for partial element equivalent circuit analysis using SPICE," *Microwave and Wireless Components Letters, IEEE*, Volume: 14, Issue: 5, pp. 216 – 218, March 2004.

[4] J. Jayabalan, B.L. Ooi, M.S. Leong and M.K. Iyer, "Modeling and application of elastomer mesh for microwave probing," to appear in *IEE Proceedings Microwaves, Antennas and Propagation,* 2006.

[5] A. Ruehli, "Partial element equivalent circuit (PEEC) method and its application in the frequency and time domain;" *Electromagnetic Compatibility Symposium,* pp. 128 – 133, 19-23 August 1996.

[6] W. Pinello and A. Ruehli, "Time domain solutions for coupled problems using PEEC models with waveform relaxation," *Antennas and Propagation Society International Symposium*, AP-S. Digest , Volume: 3 , pp. 2118 – 2121, July 1996.

[7]G. Antonini, "The fast multipole method for PEEC circuit analysis," *Electromagnetic Compatibility Symposium Proceedings*, Volume: 1, pp. 446 – 451, 19-23 August 2002.

[8] G. Antonini and A. Orlandi, "A wavelet-based time-domain solution for PEEC circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Volume: 47, Issue: 11, pp. 1634 – 1639, November 2000.

[9] G. Antonini, A. Orlandi and A.E. Ruehli, "Speed-up of PEEC method by using wavelet transform," *Electromagnetic Compatibility Symposium proceedings*, Volume: 1, pp. 95 - 100, 21-25 August 2000.

[10] A.E. Ruehli, G. Antonini, J. Esch, J. Ekman, A. Mayo and A. Orlandi, "Nonorthogonal PEEC formulation for time- and frequency-domain EM and circuit modeling," *IEEE Transactions on Electromagnetic Compatibility*, Volume: 45, Issue: 2, pp. 167 – 176, May 2003.

[11] G. Antonini, A.E. Ruehli and J. Esch, "Nonorthogonal PEEC formulation for time and frequency domain modeling," *Electromagnetic Compatibility Symposium Proceedings*, Volume: 1, pp. 452 – 456, 19-23 August 2002.

[12] G. Antonini, A. Orlandi and A.E. Ruehli, "Analytical integration of quasi-static potential integrals on nonorthogonal coplanar quadrilaterals for the PEEC method," *IEEE Transactions on Electromagnetic Compatibility*, Volume: 44, Issue: 2, pp. 399 – 403, May 2002.

[13] J.E. Garrett, A.E. Ruehli and C.R. Paul, "Accuracy and stability improvements of integral equation models using the partial element equivalent circuit (PEEC) approach," *IEEE Transactions on Antennas and Propagation,* Volume: 46, Issue: 12, pp. 1824 - 1832, December 1998.

[14] A.E. Ruehli and G. Antonini, "On modeling accuracy of EMI problems using PEEC," *Electromagnetic Compatibility Symposium Proceedings*, Volume: 1, pp. 341 – 346, August 2003.

[15] J. Garrett, A.E. Ruehli and C. Paul, "Recent improvements in PEEC modeling accuracy," *Electromagnetic Compatibility Symposium Proceedings*, pp. 347 – 352, August 1997.

[16] A. Ruehli, U. Miekkala, A. Bellen and H. Heeb, "Stable time domain solutions for EMC problems using PEEC circuit models," *Electromagnetic Compatibility Symposium Proceedings*, pp. 371 – 376, August 1994.

[17] J. Cullum, A.E. Ruehli and T. Zhang, "Model reduction for PEEC models including retardation," *Proceedings of the Electrical Performance of Electronic Packaging topical Meeting*, pp. 287 – 290, October 1998.

[18] G. Antonini, A. Orlandi and A.E. Ruehli, "Harten's scheme for PEEC method," *Electromagnetic Compatibility Symposium Proceedings,* Volume: 1 , pp. 340 – 344, August 2001.

[19] S.A. Teo, B.L. Ooi; S.T. Chew and M.S. Leong, "A fast PEEC technique for full-wave parameters extraction of distributed elements," *Microwave and Wireless Components Letters*, Volume: 11, Issue: 5, pp. 226 – 228, May 2001.

[20] P.J. Restle, A.E. Ruehli, S.G. Walker and G. Papadopoulos, "Full-wave PEEC time-domain method for the modeling of on-chip interconnects," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* , Volume: 20, Issue: 7, pp. 877 – 886, July 2001.

[21] Y. Cao, Z. F. Li, J. F. Mao and J.F. Mao, "A PEEC with a new capacitance model for circuit simulation of interconnects and packaging structures," *IEEE Transactions on Microwave Theory and Techniques,* Volume: 48, Issue: 2, pp.281 – 287, February 2000.

[22] J. Cullum, A. Ruehli and T. Zhang, "A method for reduced-order modeling and simulation of large interconnect circuits and its application to PEEC models with

retardation," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Volume: 47, Issue: 4, pp. 261 – 273, April 2000.

[23] K.L. Wu, L.K.Yeung and Y. Ding, "An efficient PEEC algorithm for modeling of LTCC RF circuits with finite metal strip thickness," *Microwave and Wireless Components Letters, IEEE*, Volume: 13, Issue: 9, pp. 390 – 392, September 2003.

[24] K.M. Coperich, A.E. Ruehli and A. Cangellaris, "Enhanced skin effect for partial-element equivalent-circuit (PEEC) models," *IEEE Transactions on Microwave Theory and Techniques*, Volume: 48, Issue: 9, pp. 1435 – 1442, September 2000.

[25] C. Wollenberg and A. Gurisch, "Analysis of 3-D interconnect structures with PEEC using SPICE," *IEEE Transactions on Electromagnetic Compatibility*, Volume: 41, Issue: 4, pp. 412 – 417, November 1999.

[26] G. Antonini, S. Cristina and A. Orlandi, "PEEC modeling of lightning protection systems and coupling to coaxial cables," *IEEE Transactions on Electromagnetic Compatibility,* Volume: 40, Issue: 4, pp. 481 – 491, November 1998.

[27] R. Araneo and L. Shaofeng, "Investigation of potential resonances in CEMPIE-PEEC simulations of multilayered PCBs," *Electromagnetic Compatibility Symposium Proceedings*, Volume: 2, pp. 642 – 647, August 2003.

[28] J. Ekman, G. Antonini and A. Orlandi, "3D PEEC capacitance calculations," *Electromagnetic Compatibility Symposium Proceedings*, Volume: 2, pp. 630 – 635, August 2003.

[29] H. Sanchez and J. Carpio, "Evaluation of current distribution on wires with a simple model based on PEEC method," *Electromagnetic Compatibility Symposium Proceedings*, Volume: 1, pp. 434 – 436, August 2003.

[30] B. Archambeault, "Analyzing power/ground plane decoupling performance using the partial element equivalent circuit (PEEC) simulation technique," *Electromagnetic Compatibility Symposium Proceedings*, Volume: 2 , pp. 779 – 784, August 2000.

[31] W. Pinello, A. Ruehli and A. Cangellaris, " Analysis of interconnect and package structures using PEEC models with radiated emissions," *Electromagnetic Compatibility Symposium Proceedings*, pp. 353 – 358, August 1997.

[32] M. Kamon, N. Marques, L.M. Silveira and J. White, "Generating reduced order models via PEEC for capturing skin and proximity effects," *Electrical Performance of Electronic Packaging Topical Meeting Proceedings*, pp. 259 – 262, October 1997.

[33] A. E. Ruehli, W.P. Pinello and A.C. Cangellaris, "Comparison of differential and common mode response for short transmission line using PEEC models," *Electrical Performance of Electronic Packaging Topical Meeting*, pp. 169 – 171, October, 1996.

[34] P. Leduc, A. Schellmanns, D. Magnon and F. Guitton, "Modeling of integrated inductors with a coplanar ground plane using the PEEC method," *European Microwave Conference Proceedings*, Volume: 1 , pp. 447 – 450, October, 2003.

[35] A. Rong, A.C. Cangellaris and L. Dong, "Comprehensive broadband electromagnetic modeling of on-chip interconnects with a surface discretization-based generalized PEEC model," *Electrical Performance of Electronic Packaging Topical Meeting Proceedings*, pp. 367 – 370, October 2003.

[36] G. Antonini, A.E. Ruehli and A. Haridass, "Including dispersive dielectrics in PEEC models," *Electrical Performance of Electronic Packaging Topical Meeting Proceedings*, pp. 349 – 352, October 2003.

[37] H. Yu and L. He, "Vector potential equivalent circuit based on PEEC inversion," *Design Automation Conference Proceedings*, pp. 718 – 723, June 2003.

[38] H. Long, Z. Feng, H. Feng, A. Wang and R. Tianling, "MagPEEC: extended PEEC modeling for 3D arbitrary electro-magnetic devices with application for m-cored inductors," *Radio Frequency Integrated Circuits (RFIC) Symposium Proceedings*, pp. 251 – 254, June 2003.

[39] K.Y. Su and J.T. Kuo, "Analytical evaluation of inductance of spiral inductors using partial element equivalent circuit (PEEC) technique," *Antennas and Propagation Society International Symposium Proceedings*, Volume: 1, pp. 364 – 367, June 2002.

[40] L. Guo-Lin and Z.H. Feng, "Consider the losses of dielectric in PEEC," *Microwave and Millimeter Wave Technology Conference Proceedings*, pp. 793 – 796, August 2002.

[41] H. Hu and S. S. Sapatnekar, "Efficient PEEC-based inductance extraction using circuit-aware techniques," *Computer Design: VLSI in Computers and Processors, Conference Proceedings,* pp. 434 – 439, September 2002.

[42] M. Besacier, M. Coyaud, J.L. Schanen, J. Roudet and B. Rivet, "Hybrid Si-SiC fast switching cell modelling and characterisation including parasitic environment description by PEEC method," *Power Electronics Specialists Conference Proceedings,* Volume: 4, pp. 1753 – 1757, June 2002.

[43] G. Antonini, "Full wave analysis of power electronic systems through a PEEC state variables method," *Proceedings of the IEEE International Symposium on Industrial Electronics*, Volume: 4, pp. 1386 – 1391, July 2002.

[44] G. Antonini and S. Cristina, "EMI design of power drive system cages using the PEEC method and genetic optimization techniques," *Electromagnetic Compatibility Symposium Proceedings*, Volume: 1, pp. 156 – 160, August 2001.

[45] J. Ekman, "Experimental verification of PEEC based electric field simulations," *Electromagnetic Compatibility Symposium Proceedings*, Volume: 1, pp. 351 − 355, August 2001.

[46] N. Matsui, S. Shintani, R. Raghuram and N.Orhanovic, "Return path analyzer based on PEEC and sectioning methods," *Electromagnetic Compatibility Symposium Proceedings*, Volume: 1, pp. 345 − 350, August 2001.

[47] H. Wang, B. Archambeault and T.H. Hubing, "Challenge problem update: PEEC and MOM analysis of a PC board with long wires attached," *Electromagnetic Compatibility Symposium Proceedings*, Volume: 2 , pp. 811 − 814, August 2001.

[48] B. Archambeault, A. Roden and O. Ramahi, "Using PEEC and FDTD to solve the challenge delay line problem," *Electromagnetic Compatibility Symposium Proceedings*, Volume: 2, pp. 827 − 832, August 2001.

[49] A. Rong and A.C. Cangellaris, "Generalized PEEC models for three-dimensional interconnect structures and integrated passives of arbitrary shapes," *Electrical Performance of Electronic Packaging Topical Meeting Proceedings*, pp. 225 − 228, October 2001.

[50] G. Wollenberg and A. Gorisch, "Coupling of PEEC models with transmission line models for simulation of wiring structures," *Electromagnetic Compatibility Symposium Proceedings*, Volume: 2 , pp. 848 − 853, August 1999.

[51] A.E. Ruehli and G. Papadopoulos, "Solution of a complex via-pin connector problem using the partial element equivalent circuit (PEEC) method," *Electromagnetic Compatibility Symposium Proceedings*, Volume: 2, pp. 673 − 678, August 1999.

[52] K.M. Coperich, A.E. Ruehli and A.C. Cangellaris, "Enhanced skin effect for partial element equivalent circuit (PEEC) models," *Electrical Performance of Electronic Packaging Topical Meeting Proceedings*, pp. 189 − 192, October 1999.

[53] A. E. Ruehli and A.C. Cangellaris, "An application of the partial element equivalent circuit (PEEC) method to realistic printed circuit board problem," *Electromagnetic Compatibility Symposium Proceedings*, Volume: 1, pp. 182 − 187, August 1998.

[54] N. Piette, Y. Marechal and E. Clavel, "Calculation of electrodynamic efforts on busbar technology: comparison between partial equivalent element circuit method (PEEC) and finite element method (FEM)," *Industry applications Conference Proceedings*, *IEEE*, Volume: 2, pp. 921 − 924, October 1998.

[55] A. Ruehli and E. Chiprout, "The importance of retardation in PEEC models for electrical interconnect and package (EIP) applications," *Electrical Performance of Electronic Packaging Topical Meeting Proceedings*, pp. 232 − 234, October 1995.

[56] J.Vlach and K.Singhal, *Computer Methods for circuit analysis and Design*, NewYork, Van Nostrand-Reinhold, 1983.

[57] E. V. Solodovnik, G. J. Cokkinides and A. P. Sakis Meliopouls, "Comparison of implicit and explicit integration techniques on the non-ideal transformer example," *Proceedings of the Thirtieth Southeastern Symposium on System Theory*, pp. 32 - 37, March 1998.

[58] P.F. Cox, R. G. Burch, P. Yang and D. E. Hocevar, "New implicit integration method for efficient latency exploitation in circuit simulation," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Volume: 8, Issue 10, pp. 1051 – 1064, October 1989.

[59] R.P. Rynne and P.D. Smith, "Stability of time marching algorithms for the electric field integral equation," *Journal of Electromagnetic Waves and Applications,* Volume: 4, pp. 1181-1205, 1990.

[60] A.G. Tijhuis, "Toward a stable marching-on-in time method for two dimensional transient electromagnetic scattering problems," *Radio Science,* Volume: 19, pp. 1311-1317, 1984.

[61] P.D. Smith, "Instabilities in time marching methods for scattering: Cause and Rectification," *Electromagnetics*, Volume: 10, pp. 439-451, 1990.

[62] S.M. Rao, T.K. Sarkar and S.A. Dianat, "A novel technique to the solution of transient electromagnetic scattering from thin wires," *IEEE Transactions on Antennas and Propagation,* Volume: 34, pp. 630-634, 1986.

[63] K.S.Kundert, *The Designer's guide to SPICE and SPECTRE*, Kluwer Academic, 1995.

[64] L. Duleba, "On the use of Campbell-Baker-Hausdorff-Dynkin formulas in nonholonomic motion planning," *Proceedings of the First Workshop on Robot Motion and Control*, pp. 177 -182, June 1999.

[65] R. Bellman, *Introduction to Matrix Analysis*, 2nd Edition, McGraw-Hill, pp 180-181, 1970.

[66] H. Kawaguchi, "Evaluation of the Lorentz group Lie algebra map using the Baker-Cambell-Hausdorff formula," *IEEE Transactions on Magnetics*, Volume: 35, Issue: 3, pp. 1490 -1493, May 1999.

[67] F. W. Grover, *Inductance Calculations,* New York, NY: Van Nostrand, 1962.

[68] A.E. Ruehli and P.A. Brennan, " Efficient Capacitance Calculations for Three-Dimensional Multiconductor Systems," *IEEE Transactions on Microwave Theory and Techniques,* Volume:21, Issue: 2, pp. 76-82, February 1973.

[69] S. Chakraborty and V. Jandhyala, "Evaluation of Green's function integrals in conducting media" *Antennas and Propagation Society International Symposium Proceedings*, Volume: 3, pp. 320 – 323, June 2003.

[70] J. Czyz, *Paradoxes of measures and dimensions originating in Felix Hausdorff's ideas*, World Scientific, Singapore, pp. 415 – 510, 1994.

[71] F. Szidarovszky and S. Molnar, *Introduction to Matrix Theory*, World Scientific, Singapore, pp. 476 – 479, 2002.

[72] Zeland Software Inc., *IE3D 9.0 User's Manual*, 2003.

[73] C. Lanczos, *Applied Analysis*, Sir Issac Pitman & Sons Ltd., London, pp. 180 - 188, 1957.

[74] P. R. Bannister, *Applications of complex image theory*, Radio Science, Volume: 21, No.:4, pp. 603 – 616, 1986.

[75] A. Weisshaar, H. Lan and A. Luoh, "Accurate closed-form expression for the frequency dependent line parameters of on-chip interconnects on lossy silicon substrte,: *IEEE Transactions on Advanced Packaging*, Volume: 25, pp. 288 – 296, 2002.

[76] A.Rinaldo, "An innovative modelisation of loss mechanism in Silicon Integrated Circuits," *IEEE transactions on Circuits and Systems II*, December 1999.

[77] P.Heymann, H. Prinzler and F. Schnieder, "De-embedding of MMIC transmission-line measurements," *IEEE MTT-S International Microwave Symposium Digest*, Volume: 2, pp. 1045 – 1048, May 1994.

[78] J.A. Reynoso Hernandez *et al*., "An improved method for the wave propagation constant estimation in broadband uniform millimeter-wave transmission line," *Microwave and Optical Technology Letters*, Volume: 22, Issue: 4, August 1999.

[79] S.A. Wartenberg, "Selected topics in RF coplanar probing," *IEEE Transactions on Microwave Theory and Techniques,* Volume: 51, Issue: 4 , pp. 1413 – 1421, April 2003.

[80] T. E. Kolding, "Shield based Microwave On-Wafer Device Measurements," *IEEE Transactions on Microwave Theory and Techniques*, Volume: 49, Issue: 6, April 2001.

[81] D.M.Pozar, *Microwave Engineering*, John Wiley & Sons, 1998.

[82] J. F. White, *High Frequency Techniques*, IEEE Press, Wiley Interscience, 2004.

[83] J.R. Magnus and H.Neudecker, *Matrix Differential Calculus with Applications in Statistics and Economics*, John Wiley & Sons, 1988.

[84] S. Padmanabhan, P. Kirby, J. Daniel and L. Dunleavy, "Accurate broadband on-wafer SOLT calibrations with complex load and thru models," *ARFTG Conference Digest*, pp. 5-10, June 2003.

[85] A. Sihvola, *Electromagnetic Mixing Formulas and Applications*, The Institution of Electrical Engineers, London, 1999.

[86] H.D. Thacker, M.S. Bakir, D.C. Keezer, K.P. Martin, K.P, and J.D. Meindl, "Compliant probe substrates for testing high pin-count chip scale packages," *Electronic Components and Technology Conference Proceedings*, pp. 1188 – 1193, May 2002.

[87] C. Deng, S. Ang, H. H. Feng, A. A. O. Tay, M. Rotaru and D. Keezer, "A MEMS Based Interposer for Nano-Wafer Level Packaging Test," *Electronics Packaging Technology Conference Proceedings*, pp. 405-409, December 2003.

[88] J.L. Carbonero, G. Morin and B. Cabon, "Comparison between beryllium-copper and tungsten high frequency air coplanar probes," *IEEE Transactions on Microwave Theory and Techniques*, Volume: 43, Issue: 12, pp. 2786 – 2793, December 1995.

[89] N. Muthukrishnan, S.M. Riad and A. Elshabini-Riad, "A thick-film coplanar probe for time domain measurements," *IEEE Transactions on Microwave Theory and Techniques*, Volume: 12, Issue: 2, pp. 297 –302, June 1989.

[90] R.F. Harrington, *Field Computation by Moment Methods*, pp. 38-41, The Macmillan Co., New York, 1968.

[91] A.E. Ruehli and H. Heeb, "Circuit models for three-dimensional geometries including dielectrics," *IEEE Transactions on Microwave Theory and Techniques*, Volume: 40, Issue: 7, pp. 1507 -1516, July 1992.

[92] D. TerHarr, *Introduction to the Physics of Many-Body Systems*, Interscience publishers, pp. 1-8, 1958.

[93] C.T. Tai, *Dyadic Green Functions in Electromagnetic Theory*, 2nd Edition, Chapter 2, IEEE Press, pp. 21-37, 1993.

[94] P. Silvester, "TEM wave properties of microstrip transmission line," *Proceedings of the Institute of Electrical Engineers*, Volume: 115, pp. 43-38, 1968.

[95] J.C. Maxwell, *A Treatise on Electricity and Magnetism*, Dover, pp. 244-271, 1954.

[96] G. Szego, "Conformal mapping of the interior of an ellipse onto a circle," *The American mathematical monthly,* Volume: 57, Issue: 7, pp. 474-478, 1950.

[97] A.E. Ruehli, Ed., *Circuit Analysis, Simulation and Design, Advances in CAD for VLSI*, Volume 3, Chapter 11, pp 235-249, Elsevier, 1986.

[98] A.G. Greenhill, *The Application of Elliptic Functions*, New York, Macmillan, pp. 287-288, 1892.

[99] C. Wei, R.F. Harrington, J.R. Mautz and T.K. Sarkar,"Multiconductor transmission lines in multilayered dielectric media," *IEEE transactions on Microwave Theory and Techniques*, Volume: 32, Issue: 4, pp. 439-450, 1984.

[100] Y. Naiheng and R.F. Harrington,"Characteristic impedance of transmission lines with arbitrary dielectrics under the TEM approximation," *IEEE transactions on Microwave Theory and Techniques*, Volume: 34, Issue: 4, pp. 439-450, 1986.

[101] A. Bhattacharyya, *Electromagnetic Fields in Multilayered Structures: Theory and Applications*, Chapter 6, pp. 123-130, Artech House, 1994.

[102] Agilent Technologies, *Advanced Design System - Momentum*, Users' manual, 2003.

[103] D.C. Keezer, Q. Zhou, C. Bair, J. Kuan and B. Poole, "Terabit-per-second automated digital testing," *Proceedings of IEEE International Test Conference*, pp. 1143 -1151, 2001.

[104] J. Jayabalan, C.K. Goh, B.L. Ooi, M.S. Leong, M.K. Iyer and A.A.O. Tay, "PLL based high speed functional testing, "*IEEE Asian Test Symposium Proceedings*, pp. 116 – 119, 2003.

[105] J. Jayabalan, M.D. Rotaru, J.P.H. Tan, M.K.Iyer, B.L.Ooi and M.S. Leong, "Test Bench modeling and characterization for fine pitch wafer level packaged devices, *IEEE Electronics Packaging Technology Conference Proceedings*, pp. 502 – 505, December 2004.

[106] V.S. Rao, A.A.O. Tay, V. Kripesh, C.T. Lim and S.W. Yoon "Bed of nails -100 microns pitch wafer level interconnections process," *IEEE Electronics Packaging Technology Conference Proceedings*, pp. 444 – 449, 2004.

[107] L.C. Shen and J.A. Kong, *Applied Electromagnetics*, Third Edition, PWS Publishing Co., Boston, 1995.

[108] W. Kim and R. Madhavan, "Electrical design of package on board for gigabit data transmission," *IEEE proceedings of the Electronics Packaging Technology Conference*, pp. 150-159, December 2003.

[109] E.B. Liao, S.S. Ang, A.A.O. Tay, H.H. Feng, R. Nagarajan and V. Kripesh, "Fabrication and parametric study of wafer-level multiple-copper-column interconnect,"

IEEE Electronic Components and Technology ECTC '04. Proceedings, Volume 2, pp. 1251–1255, June 2004.

[110] J. Jayabalan, M.D. Rotaru, D. Chun, H.H. Feng, M.K. Iyer, B.L. Ooi, M.S. Leong, S. Ang, A.A.O. Tay, D. Keezer and R. Tummala, "Test strategies for fine pitch wafer level packaged devices;" *Electronics Packaging Technology Conference Proceedings,* pp. 397 – 400, December 2003.

[111] F. Spitzer, *Principles of Random Walk*, Van Nostrand, 1964.

[112] D. Bowman, *Private Communication*, Georgetown College, Phys-L Archives, http://lists.nau.edu, 1999.

[113] D.A. Hejhal, J. Friedman, M.C. Gutzwiller and A.M. Odlyzko, *Emerging Applciations of Number Theory*, Springer, pp. 479-482, 1999.

[114] D.M. Etter, D. C. Kuncicky and Doug Hull, *Introduction to MATLAB 6*, Pearson Education, 2004.

[115] K.E. Lonngren, *Electromagnetics with Matlab*, Cambridge International Science Publishers, 1997.

[116] S. Chandrasekhar, *Newton's Principia for the Common Reader*, Oxford University Press, New York, 1995.

[117] J.P. Rogers, P.H. Cutler, T.E. Feuchtwang, N. Miskovsky and A.A. Lucas, "Influence of the boundary conditions on the fermi energy and density of states in a free-electron solid of sub-micron dimensions," *Surface Science*, Volume: 141, Issue: 1, pp. 61-81, 1984.

[118] V.V. Pogosov, D. P. Kotlyarov, A. Kiejna and K. F. Wojciechowski, "Energetics of finite metallic nanowires," *Surface Science*, Volume: 472, Issue: 3, pp. 172-178, 2001.

[119] J. P. Rogers III, P.H.Cutler and T.E. Feuchtwang, "Quantum size effects in the fermi energy and electronic density of states in a finite square well thin film model," *Surface Science,* Volume: 436, Issue: 3, p. 181, 1987.

[120] M. Seidl and M. Brack, "Liquid Drop Model for Charged Spherical Metal Clusters," *Annals of Physics*, Volume: 245, Issue: 2, pp. 275 – 310, 1996.

[121] M. Seidl, J.P. Perdew, M. Brajczewska and C. Fiolhais, "Ionization energy and electron affinity of a metal cluster in the stabilized jellium model: Size effect and charging limit," *Journal of Chemical Physics,* Volume: 108, Issue: 19, pp. 8182 - 8189, 1998.
[122] V.V. Pogosov, "Sum-rules and energy characteristics of small metal particle," *Solid State Communications,* Volume: 75, Issue: 5, pp. 469 – 472, 1990.

[123] A. Kiejnia and V.V. Pogosov, "On the temperature dependence of the ionization potential of self-compressed solid- and liquid-metallic clusters," *Journal of Physics: Condensed Matter*, Volume: 8, Issue: 23, pp. 4245 – 4258, 1996.

[124] I. Brodie, "Uncertainty, topography, and work function," *Physical Review B*, Volume: 51, Issue: 19, pp. 13660 – 13668, 1995.

[125] K.F. Wojciechowski, "Quantum size effect in the work function of jellium slabs confined by a finite well of thickness-dependent depth ," *Physical Review B*, Volume: 60, Issue: 13, pp. 9202 - 9203, 1999.

[126] S. Halas and T. Durakiewicz, "Work functions of elements expressed in terms of the Fermi energy and the density of free electrons," *Journal of Physics: Condensed Matter*, Volume: 10, Issue: 48, pp. 10815 - 10826, 1998.

[127] L. D. Landau and E. M. Lifshitz, *Electrodynamics of Continuous Media*, Pergamon Press, New York, 1960.

[128] D.C. Barker, *MINNIE and HSpice for Analogue Circuit Simulation*. Chapman & Hall, 1991.

APPENDIX A

DELAY DIFFERENTIAL EQUATION CODING EXAMPLE FOR PEEC WITH 2 NODES

For the DDE system discussed in Section 1.4 with 2 node PEEC topology, an example loss less network is excited with a Gaussian mono-pulse current and the response output terminal voltage is captured by time stepping scheme. The code written in Matlab follows. For explanations of the code instruction set used, please refer to Matlab reference literature [114]

```
%----------code starts here------------------
tic;
hold on;
%  Time step used
h0=1/100000e9;
% Declaration of partial potential coefficients
p11=1/1e-12;
p22=2/1.33e-12;
p12=1/1e-15;



% Partial Inductance
l11=2.51e-9;
```

```
% Initialize system matrix

A1=zeros(3);

% Fill the diagonal PEEC values into system matrix

pl=[p11 p22 1/l11];

for ii=1:3

    A1(ii,ii)=pl(ii);

end

% Manipulation of off-diagonal elements

A2=zeros(3);

A2(1,3)= 1-(p12/p11);

A2(2,3)=-1+(p12/p22);

A2(3,1)=-1;

A2(3,2)=1;

% Resistance Value

A2(3,3)=0;

% State Variable Declaration

A=-A1*A2;

X=(zeros(1,3))';

X2=(zeros(1,3))';

Y=(zeros(1,3))';

Z=(zeros(1,3))';

W0=zeros(3,10000);

for mm=1:10000
```

```matlab
W0(:,mm)=[0 0 0]';

end

% % Source Excitation: Frequency of 2GHz gaussian pulse sampled at 500GHz

fc = 2E9;  fs=500E9;

tc = gmonopuls('cutoff', fc);

t  = 0 : 1/fs : 10*tc;

y2 = gmonopuls(t,fc); %plot(t,y2)

for mm=1:150

W0(1,mm)=y2(mm);

end

mm=1:800;

W=A1*W0;

B=(eye(3)-h0*A);

% LU matrix decomposition

[L,U,P] = lu(B);

sizeL=size(L);

xsizeL=sizeL(1);

L2=zeros(xsizeL, xsizeL-1);

L2(2,1)= -L(2,1);

L2(3,1)= -L(3,1);

L2(3,2)= -L(3,2);

U2=zeros(xsizeL, xsizeL-1);

U2(2,2)= -U(2,3);
```

```
U2(3,1)= -U(1,2);

U2(3,2)= -U(1,3);

UI=size(xsizeL,1);

for ui=1:xsizeL

UI(ui)=U(ui,ui);

end

% Time stepping

for jj=1:400

for iter=1:xsizeL

Y=[(X+h0*A1*W0(:,jj)) L2 ]*[1 Y(1) Y(2)]';

end

X=Y;

for iter2=1:xsizeL

Z = [[Y(3) Y(2) Y(1)]' U2]*[1 Z(2) Z(1)]';

end

X2= Z./[UI(3) UI(2) UI(1)]';

plot(jj,W0(1,jj),'k+:');

plot(jj,(X2(3)),'k.:');

xlabel('time, ps ');

ylabel(' Excitation, Ampere / Response, Volts ');

legend('Excitation Current','Voltage Response');

end

toc;
```

%----------code ends here--------------------------
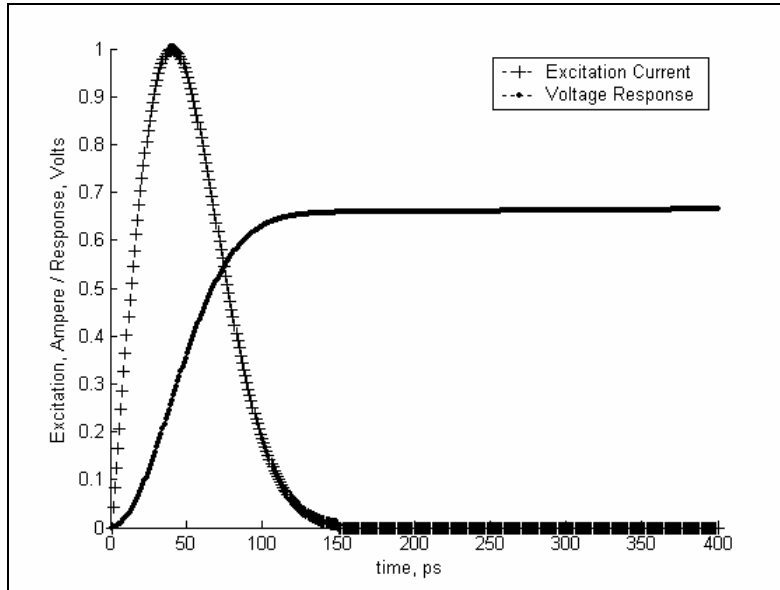
Fig. A.1: Response of a two node DDE system to a Gaussian excitation

APPENDIX B

COMPUTATION OF GREEN'S FUNCTION INTEGRALS

B.1 Numerical Evaluation
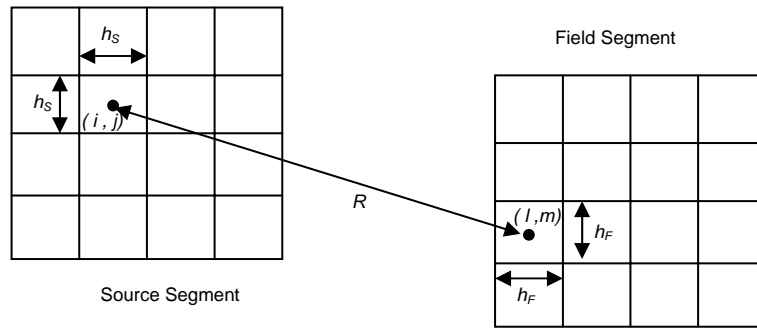
Fig. B.1: Segmentation of source and field surface elements

To illustrate the evaluation of multiple integrals, the potential at a surface segment centered at (x,y) due to sources (could be charge or current depending on whether the scalar or vector potential is calculated) at the surface segment centered at (x',y'), as represented in Fig. B.1, is considered as

$$V_\Phi(x, y) = \int_{\Delta x} \int_{\Delta y} \int_{\Delta x'} \int_{\Delta y'} \frac{\rho_s(x', y')}{4\pi\varepsilon_0 R} dy' dx' dy dx \qquad (B.1)$$

where ρ_v is the charge density assumed to be distributed uniformly throughout the segment surface and R is the distance between the centers of source and field sub-segment given by

$$R = \sqrt{(x - x')^2 + (y - y')^2} \qquad (B.2)$$

149

Let the source surface be sub-segmented into smaller areas of size $h_S \times h_S$ and let the field surface be sub-segmented into smaller areas of size $h_F \times h_F$. Let the centre of the ij^{th} source segment be given by $\left(ih_S - \dfrac{h_S}{2}, jh_S - \dfrac{h_S}{2} \right)$ and let the centre of the lm^{th} field segment be given by. $\left(lh_F - \dfrac{h_F}{2}, mh_F - \dfrac{h_F}{2} \right)$

The potential (B.1) is then given by

$$V_\Phi = \frac{1}{4\pi\varepsilon_0} \sum_i \sum_j \sum_l \sum_m \frac{\rho_s h_S^2}{\sqrt{X^2 + Y^2}} \tag{B.3}$$

where

$$X = \left(\left(ih_S - \frac{h_S}{2} \right) - \left(lh_F - \frac{h_F}{2} \right) \right) \tag{B.4}$$

$$Y = \left(\left(jh_S - \frac{h_S}{2} \right) - \left(mh_F - \frac{h_F}{2} \right) \right) \tag{B.5}$$

Likewise the potential at a volume segment centered at (x,y,z) due to sources at the volume segment centered at (x',y',z') is considered as

$$V_A(x, y, z) = \int_{\Delta x} \int_{\Delta y} \int_{\Delta z} \int_{\Delta x'} \int_{\Delta y'} \int_{\Delta z'} \frac{\mu_0 \rho_v(x', y', z')}{4\pi R} dz' dy' dx' dz dy dx \tag{B.6}$$

where ρ_v is the current density assumed to be distributed uniformly throughout the segment cross section and R is the distance between the centers of source and field sub-segment given by

$$R = \sqrt{(x-x')^2 + (y-y')^2 + (z-z')^2} \qquad \text{(B.7)}$$

Let the source volume be sub-segmented into smaller volumes of size $h_S \times h_S \times h_S$ and let the source volume be sub-segmented into smaller volumes of size $h_F \times h_F \times h_F$. Let the centre of the ijk^{th} source segment be given by $\left(ih_S - \dfrac{h_S}{2}, jh_S - \dfrac{h_S}{2}, kh_S - \dfrac{h_S}{2} \right)$ and let the centre of the lmn^{th} field segment be given by $\left(lh_F - \dfrac{h_F}{2}, mh_F - \dfrac{h_F}{2}, nh_F - \dfrac{h_F}{2} \right)$.

The potential (B.6) is then given by

$$V_A = \frac{\mu_0}{4\pi} \sum_i \sum_j \sum_k \sum_l \sum_m \sum_n \frac{\rho_v h_S^2}{\sqrt{X^2 + Y^2 + Z^2}} \qquad \text{(B.8)}$$

where X, Y and Z are given by (B.4), (B.5) and

$$Z = \left(\left(kh_S - \frac{h_S}{2} \right) - \left(nh_F - \frac{h_F}{2} \right) \right) \qquad \text{(B.9)}$$

respectively. For the evaluation of multiple integral terms (self terms) when source and field regions coincide, the step sizes for the grids can be chosen differently by disconnecting their centre points with an irrational number (such as square root of 2) or a transcendental number (π, e) to avoid singularity without compromising desired accuracy.

B.2 Analytical Evaluation

While numerical evaluation is more accurate and flexible to use for a variety of arbitrary geometries, the analytical forms serve as a quick and intuitive first order cross check, of numerical algorithms, using regular / symmetrical geometries.

B.2.1 Approximate Forms for Removing Singularity
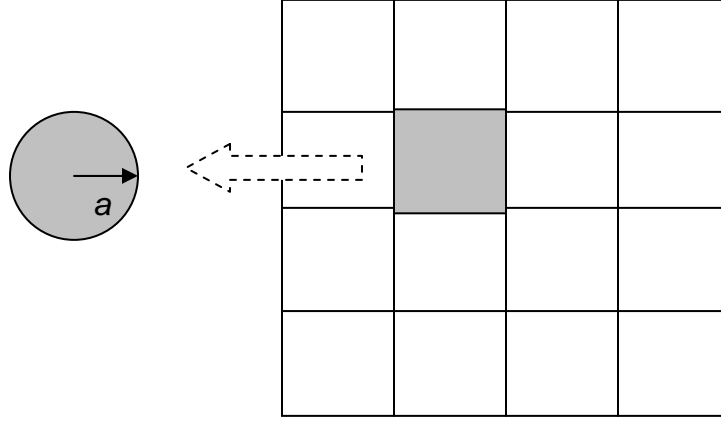
Fig. B.2: Circular approximation of a square patch for self term evaluation

To evaluate the self potential term for a square (or rectangular) surface Δs_{ii}, an equivalent circular area may be used to replace the original surface. It is assumed that the charge is distributed within the perimeter of the circle. The potential is then computed at the perimeter. The potential at the center is set equal to this value and is given by

$$V_{ii} = \frac{1}{4\pi\varepsilon_0} \int_0^{2\pi}\int_0^a \frac{\rho_s r \, dr \, d\varphi}{r} = \frac{\rho_s}{4\pi\varepsilon_0} 2\pi a = \frac{\rho_s}{2\varepsilon_0} a = \frac{\rho_s}{2\varepsilon_0}\sqrt{\frac{\Delta s_{ii}}{\pi}} \qquad (\text{B.10})$$

where radius a of the circle is written in terms of the area of grid element.

Likewise the self terms of a line charge element, volume charge element can be evaluated by approximating them with a cylindrical surface and spherical surface respectively. To explore further on these lines, please refer [115].

B.2.2 Approximate Evaluation of Self Terms From Variational Considerations

In the work by Ruehli [68], a self capacitance calculation scenario for an infinitely thin square plate by different methods including that of Maxwell is outlined. Maxwell's procedure involving symmetry considerations yields 40.13pF while the best of Galerkin method with as many as 30 cells per side gives about 41 pF.

Here is our approach that aims to get results quickly from purely energy and charge variational considerations: We consider an infinitely thin square shaped charge sheet with length a. For simplicity we initially assume that the charge is uniformly distributed with density σ. Then the charge at a distance r from the centre of the sheet is

$$Q_r = \sigma a^2 = 4\sigma r_{max}{}^2 \tag{B.11}$$

$$dQ = 4\sigma \times 2r dr \tag{B.12}$$

The potential energy of the system is given by

$$dU = \frac{Q dQ}{4\pi\varepsilon_0 r} = \frac{32\sigma^2 r^2 dr}{4\pi\varepsilon_0} \tag{B.13}$$

$$U = \frac{32\sigma^2 r^3}{4\pi\varepsilon_0 \times 3} = \frac{2}{3} \times \frac{(4\sigma r^2)^2}{4\pi\varepsilon_0 r} = \frac{4}{3} \times \frac{Q^2}{4\pi\varepsilon_0 a} \tag{B.14}$$

153

The above result shows that the average inverse distance for the pairs of source and field points of the system comes out to be

$$\sum \frac{1}{r} = \frac{4}{3a}$$
(B.15)

Since capacitance is given by

$$C = \frac{4\pi\varepsilon_0}{\sum \frac{1}{r}} \quad ,$$
(B.16)

for 1 square meter plate, if we include the equipotential correction factor 2 for the non uniform charge distribution (corresponding to minimum energy) , we get the capacitance to be 41.7pF which is within 1% of the expected value from the Ruehli's plot [68]. Applying similar approach to a charge cube but with a charge correction factor of 4 due to the three dimensional geometry, the capacitance is 69.5pF which is within 5% of the expected value as per Ruehli's plot. This analysis shows that for standard geometries we can quickly extract the self terms for circuit parameters by generating a look up table of 2D and 3D shapes with their correction terms. An extension of this approach for mutual term computations could be done using geometric mean distances [67]. Subsection B.2.2 for approximate evaluation of self-terms from variational considerations is a contribution of this thesis. Other sections are developed based on the basic principles from the references.

APPENDIX C

THE METHOD OF IMAGES IN MULTILAYERS

C.1 On the Use of Image Method in Representing Multilayers
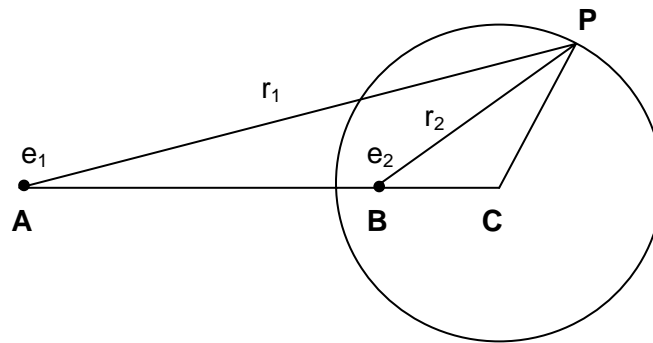
Fig. C.1: Equipotential spherical surface P due to point charges at A and B

Maxwell describes in his *Treatise* [92, Vol.I, pp. 244-248], an equipotential surface given by

$$\frac{e_1}{r_1} + \frac{e_2}{r_2} = 0 \tag{C.1}$$

when there are two charges e_1 and e_2 located at A and B distant r_1 and r_2 from any point P on the surface. The charges are said to be images of each other and the locations A and B are said to be inverse of each other because the electrified (imaginary) points are equivalent to the imaginary (electrified) surface. They can be exchanged without changing the neighboring fields. The following simple relations hold.

$$AC \cdot BC = a^2 \tag{C.2}$$

$$AC : BC = e_1{}^2 : e_2{}^2 \qquad\qquad (C.3)$$

$$a = AB \frac{e_1 e_2}{e_1{}^2 - e_2{}^2} \qquad\qquad (C.4)$$

where a is the radius of the surface. Eq. (A.4) is derived in a homogeneous dielectric medium.

The possibility that the problem of two different permittivities with uniform charges may be treated as equivalent to the problem of two different charges with uniform permittivity is first assumed. (C.4) can then be recast by transforming charge variables into permittivity terms and distance variable into elliptic transformation of permittivity ratio circle $|w| = \sqrt{\dfrac{\varepsilon_{r1}}{\varepsilon_{r2}}}$ to give Eq. (5.19) which can be reordered to

$$r_m = \frac{\varepsilon_{r1}\varepsilon_{r2}}{\varepsilon_{r1}{}^2 - \varepsilon_{r2}{}^2} \left(\frac{\varepsilon_{r1} + \varepsilon_{r2}}{\sqrt{\varepsilon_{r1}\varepsilon_{r2}}} \right) (\varepsilon_{r1} + \varepsilon_{r2}) = \frac{(\varepsilon_{r1} + \varepsilon_{r2})\sqrt{\varepsilon_{r1}\varepsilon_{r2}}}{(\varepsilon_{r1} - \varepsilon_{r2})}. \qquad (C.5)$$

(C.5), a contribution of this thesis, is exactly the coefficient of Eq. (5.16) obtained from the solution of the eigenvalue problem $\mathbf{G}_e \mathbf{X} = \lambda \mathbf{X}$. The resemblance of the result from two different stand points makes the earlier assumption more credible and admits the use of image method in the representation of multilayers.

C.2 Multilayer Problem as a Multi-body Problem

The mathematical equivalence of the terms corresponding to coulomb potential and force and that of gravitation imply an exact solution of the multilayer problem. To illustrate, first the equivalence of the two forms of forces is considered. Secondly, the uniqueness of the solution to multi-layers is shown to follow from the dual laws of coupling forces.

156

As noted by Chandrasekhar [116, pp. 293-298], the method of images has been first discovered and is mentioned in the gravitational context in Proposition LXXXII of Newton's *Principia*. This is interesting due to the fact (known to date) that there are no negative mass (charge) and no zero potential in gravitation in the same sense as in electrostatics. Still, when two interacting electric charges are of opposing sign, the attractive force coupling does lead to similar equi-potential surfaces as in gravitation. Thus the ease with which both forms of forces are amenable to the image method is a consequence of the mathematical equivalence of the electrostatic and gravitational potential.

Again, the laws of both the force forms exhibit coupling strength that varies with inverse square distance as

$$F_e = \frac{e_1 e_2}{4\pi\varepsilon_0 r^2} \tag{C.6}$$

and

$$F_g = G\frac{m_1 m_2}{r^2} \tag{C.7}$$

The relationship of the inverse distance law with the elliptic motion signifies that the focus of the ellipse in inverse square distance is dual to the centre of the ellipse in linear distance [116, pp. 114-126]. Also the case of multi-body problem is exactly solvable when the mutual force coupling varies as linear distance [116, pp. 215-217]. This thesis thus recognizes that the multilayer problem formulation resembles the multi-body couplings and hence unique solution of the form of (5.22) is admissible.

C.3 Silvester's Image Model of Spatial Green's Function

The dyadic Green's function in the space domain is generally not known in a closed form. A static equivalent, however, has been derived by Silvester [94] from a model of charge images.
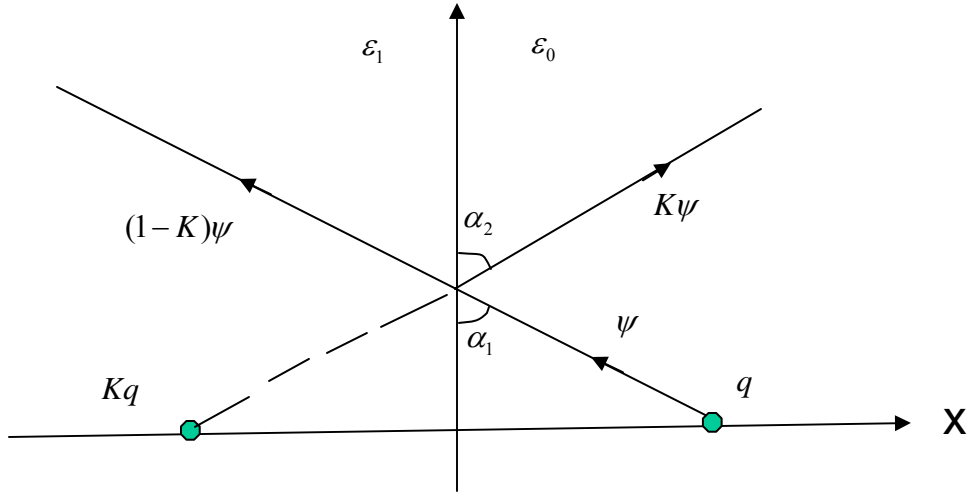
Fig. C.2: Flux lines associated with a line charge near a semi-infinite dielectric half-space.

The simple case of a half-space, $x<0$, filled with a homogeneous dielectric of permittivity ε_1 is considered in Fig. C.2. Two-dimensional symmetry is assumed and a line charge q coulombs per meter is supposed lying at a distance a from the surface $x=0$. This charge results in electric flux radiating uniformly from its length. Considering a tube of flux ψ emanating from the charge source, some fraction of the flux $K\psi$ will fail to penetrate while the remainder $(1-K)\psi$ will continue into the dielectric material. The normal component of flux density and the tangential component of electric field should be continuous across the interface. The normal flux density requirement gives

$$(1-K)\psi \sin\alpha_1 = \psi \sin\alpha_1 - K\psi \sin\alpha_2 . \tag{C.8}$$

It follows that $\alpha_1 = \alpha_2$ since the angles subtended by incident and reflected flux are equal.

The continuity of the tangential electric field component means that

$$\frac{1}{\varepsilon_1}(1-K)\psi \cos\alpha_1 = \frac{1}{\varepsilon_0}\psi \cos\alpha_1 + \frac{1}{\varepsilon_0}K\psi \cos\alpha_2. \tag{C.9}$$

This leads to the value of K i.e.,

$$K = \frac{\varepsilon_0 - \varepsilon_1}{\varepsilon_0 + \varepsilon_1}. \tag{C.10}$$

This analysis shows that the geometrical relationships governing the behaviour of flux lines near a dielectric interface are analogous to those of optics and that the image coefficient K plays a role corresponding to the optical reflection coefficient. The equality of angles found leads to an apparent existence of images. Thus the flux lines on the right-hand side of the interface appear to be due to two different line sources, the original source q and an image source Kq located in the dielectric region at a distance a behind he interface. Considering the region $x<0$, any measurement performed in the dielectric region would indicate a single source of strength $(1-K)q$ located in the right half-space. Thus, for the simple half-space dielectric slab, the potential of the line source is, $x>0$,

$$V(x,y) = -\frac{q}{4\pi\varepsilon_0}[\ln\{(x-a)^2 + y^2\} + K\ln\{(x+a)^2 + y^2\}] \tag{C.11}$$

$x<0$,

$$V(x,y) = -\frac{q}{4\pi\varepsilon_1}(1-K)\ln\{(x-a)^2 + y^2\} \tag{C.12}$$

For a slab dielectric of finite thickness, multiple images arise as shown in Fig. C.3 and the potential function is given by

$$V(r) = -\sum_{i=1}^{\infty} \frac{q_i}{2\pi\varepsilon} \ln |\mathbf{r} - \mathbf{r}_i'| \qquad (C.13)$$
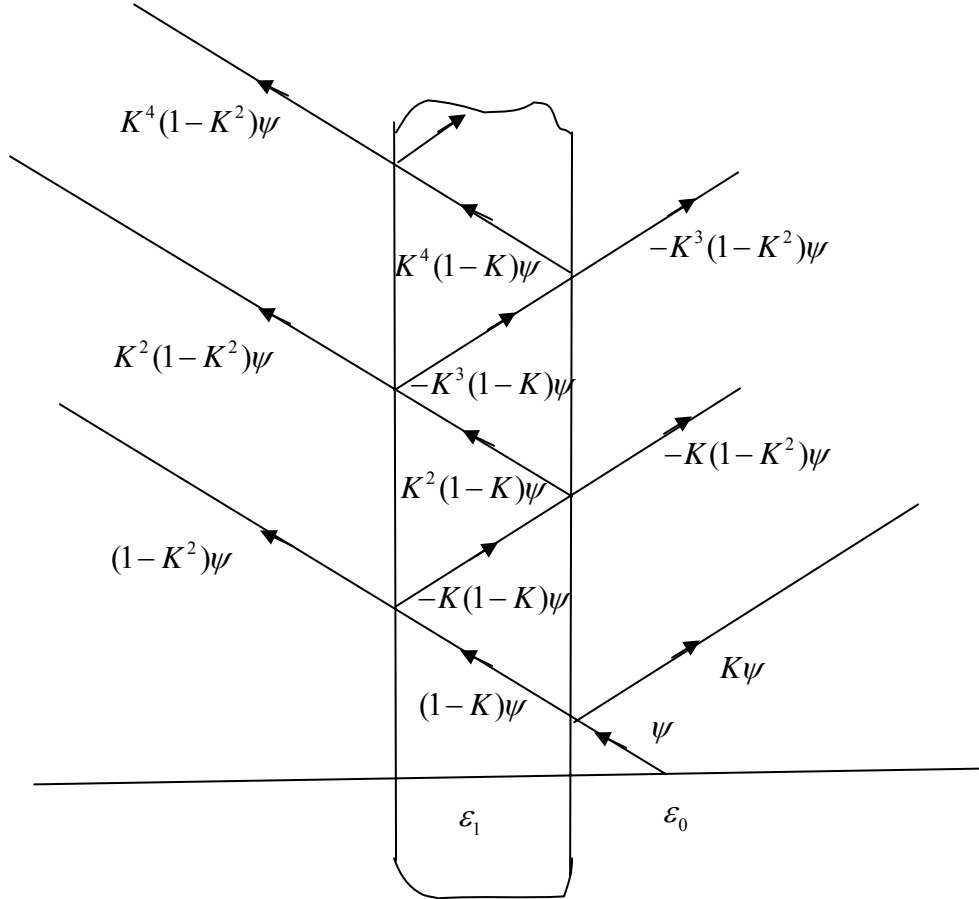
Fig. C.3: Flux lines due to a line charge near a dielectric slab.

A comparison of Silvester's Green's function term based on equation (C.13) and the Interface function term based on equation (5.20) for a dielectric slab situated at a distance from an electrically charged source is shown in Figs. C.4 – C.7. The relative error is within 2% in the wide range of slab width and source distance shown in C.5 and C.7 respectively.
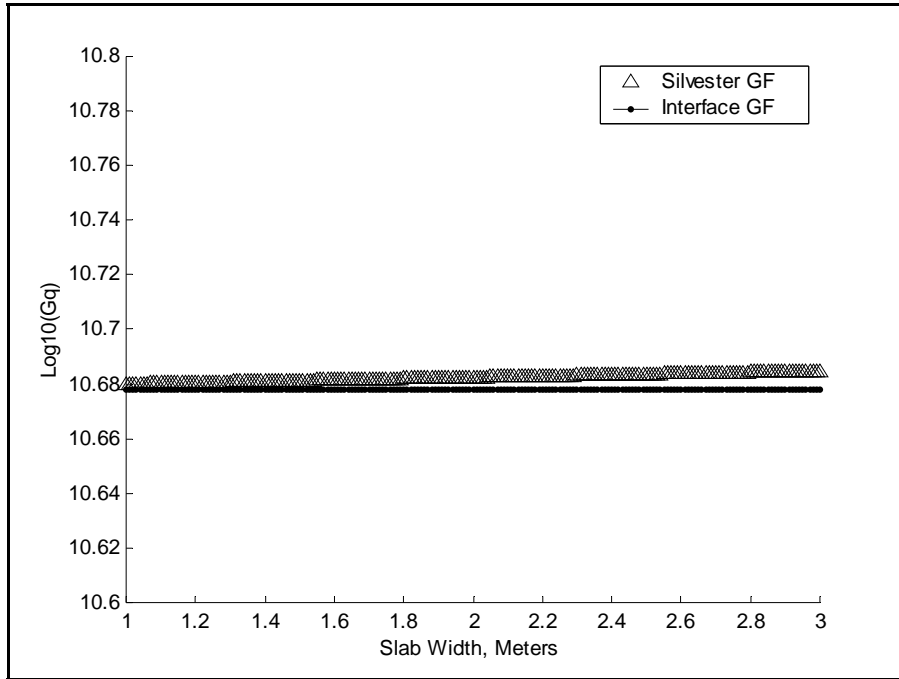
Fig. C.4: Green's function for the dielectric slab at the field distance of x=5 m, y= 7m and source distance
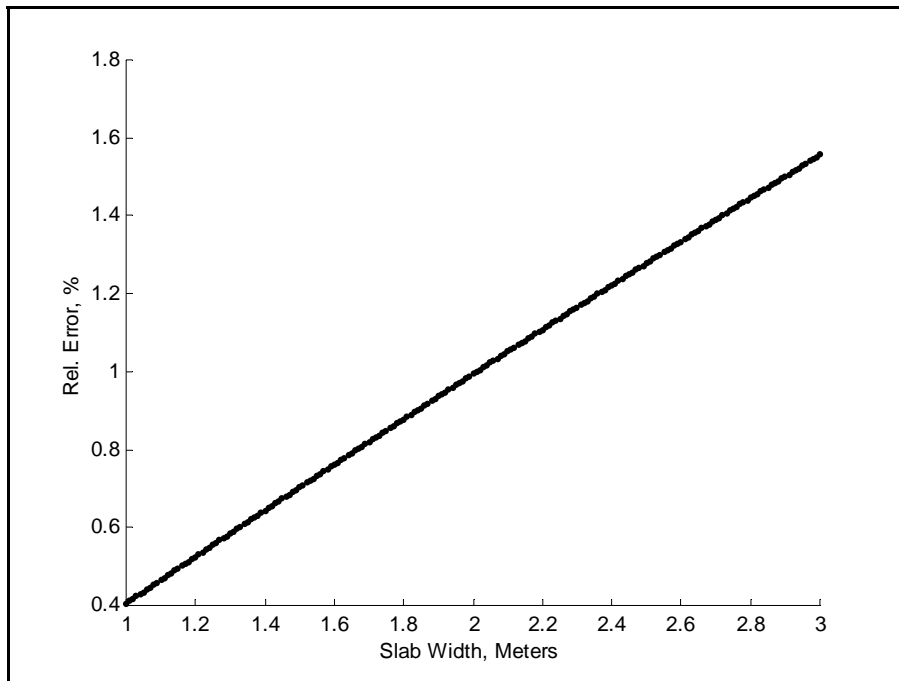
of x'=75m, y'=0m. .

Fig. C.5: Relative difference in Green's function for the dielectric slab at the field distance of x=5 m, y=

7m and source distance of x'=75m, y'=0m..
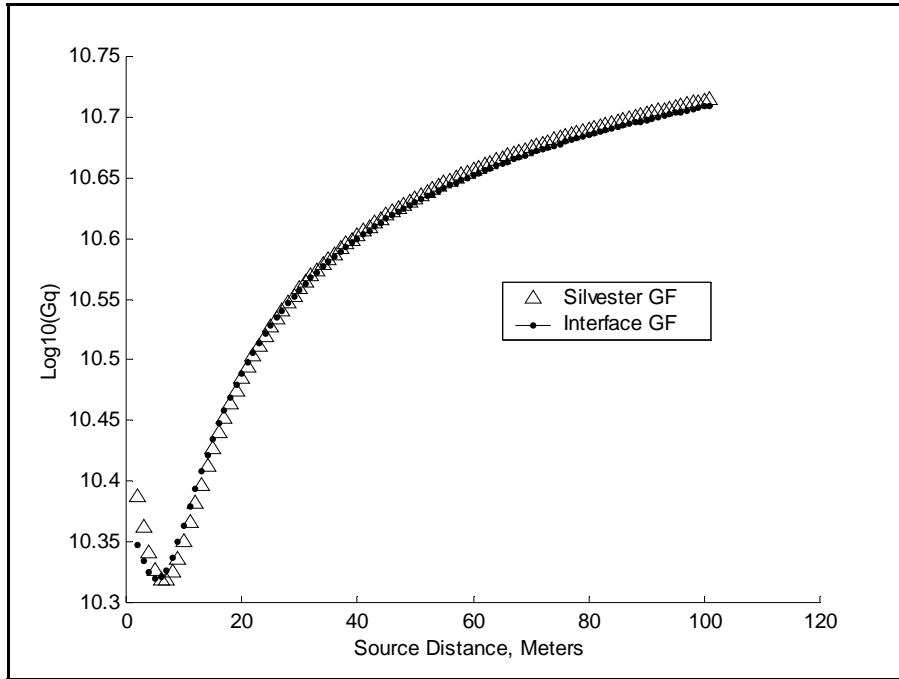
Fig. C.6: Green's function for the dielectric slab at the field distance of x=5 m, y= 7m, source distance of

y'=0m and slab width of 2m..
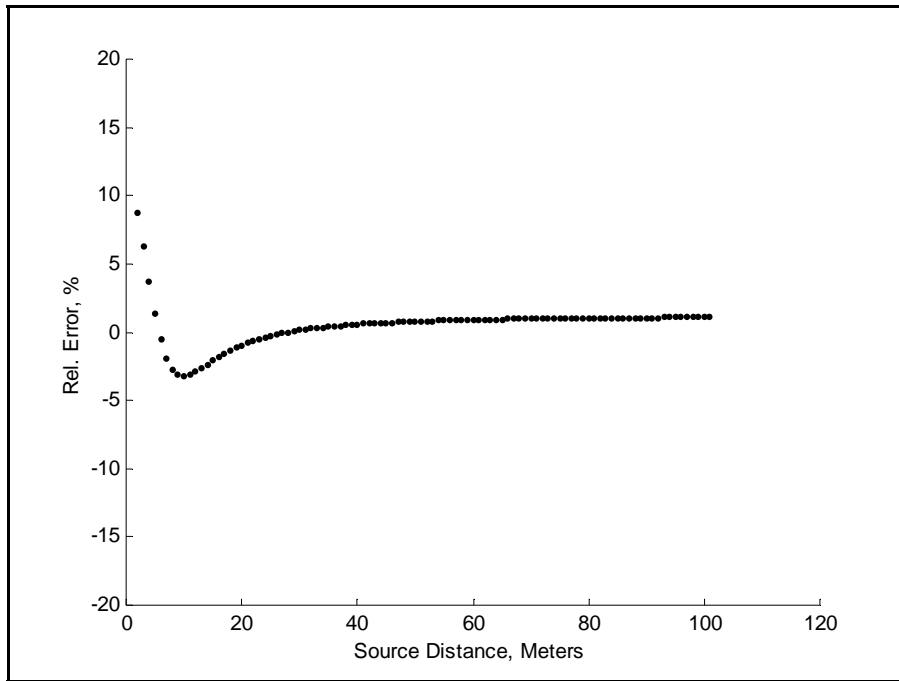
Fig. C.7: Relative difference in Green's function for the dielectric slab at the field distance of x=5 m, y=

7m, source distance of y'=0m and slab width of 2m..

162

Elliptic transformation of the permittivity circle leading to image equation of the form (C.5) is contributed by this thesis. This leads to the treatment of dielectric multilayer through images. Recognition of the analogy between the multilayer and multi-body problem is another contribution from the thesis. Comparison of silvester function with interface function with dielectric slab example is also a contribution of this thesis.

APPENDIX D

MODEL CONSIDERATONS AS CIRCUIT SIZES APPROACH NANO-SCALE

This appendix illustrates the size dependent behavior of Fermi energy, work function and the ionization potential of finite conducting copper nanowire by using a free electron model. A uniform conductor of finite length and a square cross section is assumed to model the copper nanowires. The energy spectrum of the wire is determined by solving the one-electron Schrödinger equation with the potential described by a square well potential. Calculation on size dependent behavior of copper nano-wire is a contribution of this thesis. Others have done similar work for metallic nano-wires in general and for other materials but our study are specific to copper.

D.1 Introduction

The properties of condensed systems with nanometer dimensions have been studied actively in the recent past. The continued miniaturization of electronic devices and nanoscale measurement systems has stimulated an interest in nanometer-scale materials such as nanowires and point contacts. Interconnect delays are dominating transistor switch delays in the current sub-micron devices. Nanowires represent the smallest dimension for efficient transport of electrons and excitons, and thus could be used as interconnects and critical devices in nanoelectronics and nano-optoelectronics. The

application of nanowires as interconnects in integrated circuit chips requires the detailed study of electronic structure as it affects electrical and transport properties.

The surface energy and work function of metallic nanowires changes with decrease in size. The electrical properties of nanowires are strongly influenced by size and interface effects. One of the main issues in low dimensional materials is the determination of size dependence of surface free energy and work function. The work function of the metals shows oscillations around the monotonic average dependence as function of decreasing particle size. The size dependence of the physical quantities can be decomposed into the monotonic component and the oscillating one. The analytical expression of density of states and the Fermi energy of a free electron metal of sub-micron dimensions are discussed in detail [117]-[119] with an infinite potential barrier model. The size dependent behavior of finite copper nanowire is discussed based on the well developed theory of spherical cluster [120]. An important quantity used in the analysis is the chemical potential, μ, of N-electron liquid of density, $\bar{n} = 3/(4\pi r_s^3)$, in a neutral sample confined by a spherical surface of the radius R = $r_s N^{1/3}$, where r_s is the electron density parameter. The μ is expressed as

$$\mu = \mu_o + \frac{\mu_1}{R} + O(R^{-2})$$

(D.1)

The common value of $\mu 1 = 0.12$ a.u is assumed for the simple metals following the calculations of [121]-[122], and self compressed [123] clusters.

The work function for a flat metal surface is defined as,

$$W_0 = -\mu_0$$

(D.2)

165

where the electrostatic potential, far away from the sample, is put equal to zero. We can define the quantity, work function of neutral sample as

$$W = -\mu \tag{D.3}$$

Using Eq. (D.1), we can rewrite Eq. (D.3) in the following form

$$W = W_o - \mu 1/R < W_o \tag{D.4}$$

Ionization potential is defined as the work needed to remove an electron from a neutral metallic cluster. For a large radius R, the ionization potential can be expressed as

$$IP = W + \frac{e^2}{2\varepsilon_0 R} = W + \frac{e^2}{2C} \tag{D.5}$$

where C is the capacitance of the conductor sphere. This equation can be interpreted as the effect of charging on the curvature dependence of the "work function" of the neutral finite sample. They correspond to a different origin of the size corrections, $\mu 1/R$, and $\frac{e^2}{2\varepsilon_0 R}$.

The above difference will be useful for the analysis of energetics of copper nanowire. A wire of infinite length has an infinite capacitance and therefore IP $\rightarrow$ W. Eq. (D.4) is used to test the criterion for the size dependence of the work function of a nanowire. The energy spectrum of the wire is determined by solving the one-electron Schrödinger equation with the potential described by a square well potential.

D.2 Modeling

A uniform conductor of finite length and a square cross section is assumed to model the copper nanowires. The finite wire has a length L $\equiv$ L, and a cross section of the

dimensions Ly = Lz ≡ a << L, and the constant volume Ω in the cuboidal enclosure has been considered by neglecting the temperature effects in the present work. The energy spectrum of the wire is determined by solving the one-electron Schrödinger equation with the potential V(r) described by a square well potential of depth Vo< 0, inside a wire and zero outside. The electron wave equations of the form Ψ(r) = Ψ(x) Ψ(y) Ψ(z), allow to separate the wave equation with respect to x, y, and z coordinates. The Length L is assumed to be large for a spectra corresponding to the momentum component Px, to form a quasi continuum. The strong quantization is considered in the transverse, y and z, directions, kT << Δ, where Δ is the distance between occupied levels, max{ny,nz}<< {nx}. The electron energy is given as

$$E = \frac{P_x^2}{2m} + E_{nyz} \tag{D.6}$$

with Enyz = Eny + Enz, where nyz is the number of the sub-band. For an infinitely deep potential well, the above equation reduces to

$$E_{nyz} = \frac{\hbar^2 \pi^2}{2ma^2} n_{yz}^2 , \tag{D.7}$$

where $n_{yz}^2 = n_y^2 + n_z^2$.

Vo and *Enz* are expressed as $-V_o = \frac{\hbar^2 \chi^2}{2m}$ and

$$E_{nz} = \frac{\hbar^2 k_{nz}^2}{2m} \tag{D.8}$$

Using the matching conditions for the one electron wave function at the lateral faces of the wire one gets two relations, of identical form, to determine k_{ny} and k_{nz} :

$$tan(k_{nz}a/2) = \pm\left(\frac{\chi^2}{k_{nz}^2} - 1\right)^{\pm 1/2} \tag{D.9}$$

where (+) and (-) signs correspond to even and odd stationary states, respectively. The size oscillations have been neglected for determining the depth of the potential energy well and the following formula has been assumed to be applicable.

$$-V_o = W_o - E_F^0 \tag{D.10}$$

where $E_F^0 = \left(\frac{\hbar^2}{2m}\right)(3\pi^2 \bar{n})^{2/3}$ is the Fermi energy of a uniform electron system. Eq. (D.10) is analyzed for the following three different approximations for Vo.

i) $$V(E_F) = W(E_F) - E_F \tag{D.11}$$

The functional dependencies for $W(E_F)$ based on the Brodie concept [124] of the work function was used in the present work.

ii) To calculate the quantum size effects in the work function of jellium slabs [125] using the expression,

$$W(E_F) = AE_F^{1/4} \tag{D.12}$$

iii) The expression for $W(E_F)$ derived [126] by using the length of spontaneous polarization of the electron gas at the Fermi level and the image force action, to give

$$W(E_F) = \frac{B}{r_s^{3/2}E_F^{1/2}} \tag{D.13}$$

The coefficients A and B are calculated for Cu. Equation (D.12) is derived from equation (D.13) using the relations between r_s and E_F, and they both give the same results for the extended system. For a low dimensional system, the different functional dependence of W on the Fermi energy leads to different variations of the work function with the wire

width.　At low temperatures, $k_B T \to 0$, the electron distribution function can be represented by the step function, $f(E) = \Theta(E - E_F)$, and we obtain

$$N = 2L\sqrt{\frac{2m}{\pi^2 \hbar^2}} \sum_{ny,nz}^{+} (E_F - E_{nyz})^{1/2}$$

(D.14)

The number of electrons N in the wire is fixed. Thus, by solving simultaneously the set of Equations (D.9) and (D.14) using equations (D.10-D.14), we can calculate the Fermi energy and then W(E_F). The capacitance C is represented by that of a "needle" in the shape of a prolate spheroid [127] so that

$$C \approx \varepsilon_0 x_0 (\ln 2\zeta)^{-1}$$

(D.15)

where x_o and y_o are the half axes of a spheroid , and the parameter $\zeta = x_o/y_o \gg 1$.

D.3 Results and Discussion
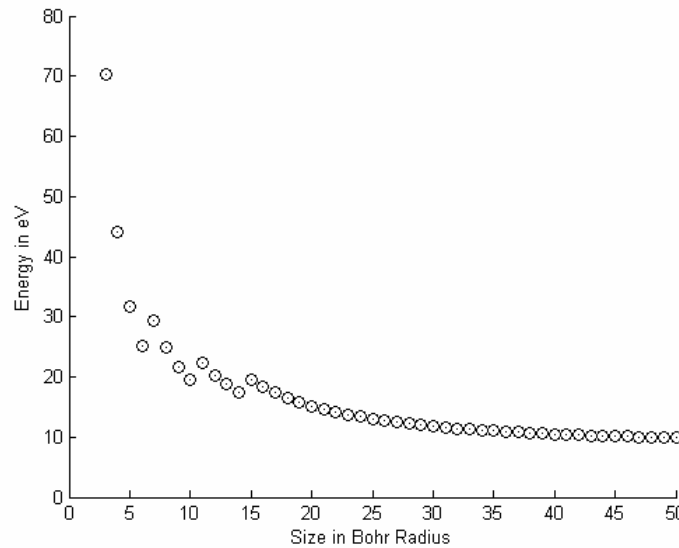
Fig. D.1:　The plot of Fermi energy versus width of Copper Nanowire.

Fig. D.1 shows the plot of Fermi energy versus width of a copper nanowire, calculated using the approximations (equation D.9).　The size dependence of   the electronic

properties of nanowire is calculated by simultaneous solution of the equations (D.10) and (D.14). From the Fig. D.1, it is evident that the Fermi energy of wire increases with decrease in wire width. The size dependence of work function and ionization potential of Cu nanowire is shown in Fig. D.2 and D.3 respectively. The size dependence is very sensitive to the applied potential form. The work function show reverse character for the model i) and iii) compared to model (ii). There is a qualitative agreement with the curvature dependence of W(R) for spherical clusters.

Using the calculations for the variant (iii), it is observed that the bottom of the potential well and the Fermi level show oscillations of the amplitude less than 1 eV. The ionization potential of the copper nanowire is estimated from the equation (D.5) and the capacitance from equation (D.15).
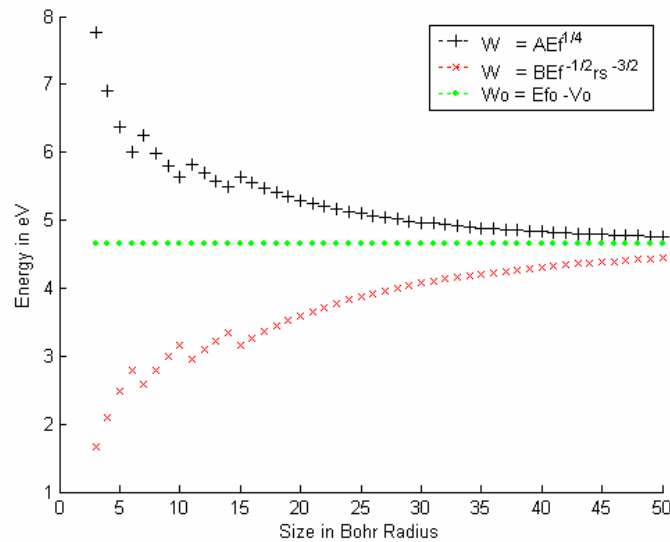
Fig. D.2: The plot of work function versus versus size of Copper Nanowire.
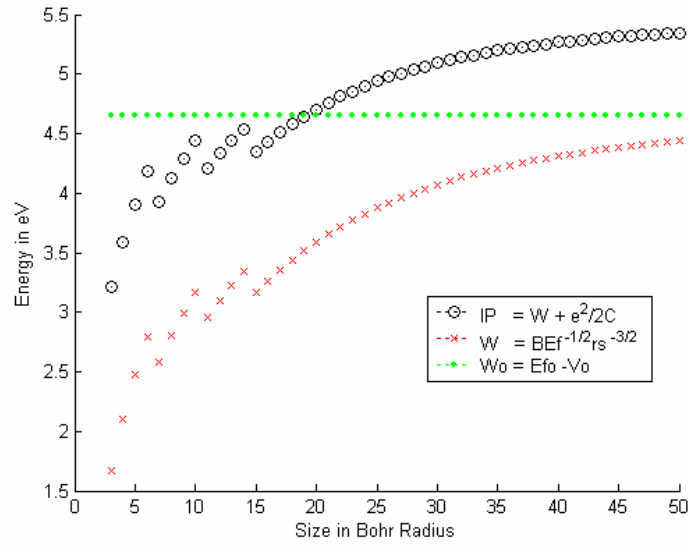
Fig. D.3: The plot of ionization potential versus size of Copper Nanowire.

The ionization potential values are increasing with increase in wired width as shown in Fig. D.3. For a large width, (a > 7 a.u), the ionization potential exhibits an oscillatory curve. It may be mentioned that the ionization potential depends only on the geometry of the wire and is independent of the direction of electron emission.

The size dependent behavior of Fermi energy, work function and the ionization potential of finite copper nanowire by using a free electron model have been calculated in the present appendix. The Fermi energy of copper nanowires increases with the reduction in the wire width. Ionization potential increases with increase in wire width of copper nanowire.

APPENDIX E

SPICE EXAMPLE CODE FOR PEEC IMPLEMENTATION

A thin two dimensional single conductor of length 500micron and width 25 micron is taken as an example to illustrate the Spice code implementation of PEEC. Inductive partitioning of the geometry is chosen such that there are 9 inductors in the x direction and 8 inductors in the y direction. The surface is segmented into 12 capacitor nodes. For details of the Spice instructions set, please refer [128].

```
.OPTIONS LIST NODE POST OPTS
..AC LIN 10 1G 10G
.PRINT AC V(1001101) V(1003401) S21(DB) S21(M) S21(P) S11(M) S11(DB) S11(R)
S11(I)
V1 1001101 0 DC 0 AC 1


.NET V(1003401,0) V1 ROUT=50 RIN=50
.PLOT AC S21(DB) (-50,10) S21(M) (-50,10)


Cx11  0 1001100 2.159F
Rx11  1001101 1001102 0.6951N
Lx11  1001102 1001103 0.0557N
Ry11  1001101 2001102 0.6951N
Ly11  2001102 2001103 0.4385P


Ex1101  1001103 1001104 VCVS DELAY 1001202 1001203 SCALE=0.1995 TD=0.6ps
Ex1102  1001104 1001105 VCVS DELAY 1001302 1001303 SCALE=0.0627 TD=1.1ps
Ex1103   1001105  1001106  VCVS  DELAY  1002102  1002103  SCALE=0.6133
TD=0.04ps
Ex1104  1001106 1001107 VCVS DELAY 1002202 1002203 SCALE=0.1841 TD=0.6ps
Ex1105  1001107 1001108 VCVS DELAY 1002302 1002303 SCALE=0.0626 TD=1.1ps
Ex1106   1001108  1001109  VCVS  DELAY  1003102  1003103  SCALE=0.4451
TD=0.08ps
Ex1107  1001109 1001110 VCVS DELAY 1003202 1003203 SCALE=0.1715 TD=0.6ps
```

Ex1108 1001110 1001201 VCVS DELAY 1003302 1003303 SCALE=0.0625 TD=1.1ps

Ey1101 2001103 2001104 VCVS DELAY 2001202 2001203 SCALE=0.1783 TD=0.6ps
Ey1102 2001104 2001105 VCVS DELAY 2001302 2001303 SCALE=0.0494 TD=1.1ps
Ey1103 2001105 2001106 VCVS DELAY 2001402 2001403 SCALE=0.0332 TD=1.8ps
Ey1104   2001106 2001107 VCVS DELAY 2002102 2002103 SCALE=0.5890 TD=0.04ps
Ey1105 2001107 2001108 VCVS DELAY 2002202 2002203 SCALE=0.1628 TD=0.6ps
Ey1106 2001108 2001109 VCVS DELAY 2002302 2002303 SCALE=0.0493 TD=1.1ps
Ey1107 2001109 1002101 VCVS DELAY 2002402 2002403 SCALE=0.0332 TD=1.8ps

VSENS11 1001100 1001101 DC 0 AC 0
VSENS12 1001200 1001201 DC 0 AC 0
VSENS13 1001300 1001301 DC 0 AC 0
VSENS14 1001400 1001401 DC 0 AC 0
VSENS21 1002100 1002101 DC 0 AC 0
VSENS22 1002200 1002201 DC 0 AC 0
VSENS23 1002300 1002301 DC 0 AC 0
VSENS24 1002400 1002401 DC 0 AC 0
VSENS31 1003100 1003101 DC 0 AC 0
VSENS32 1003200 1003201 DC 0 AC 0
VSENS33 1003300 1003301 DC 0 AC 0
VSENS34 1003400 1003401 DC 0 AC 0

F1101 1001100 0 CCCS DELAY VSENS12 SCALE=0.1278 TD=0.6ps
F1102 1001100 0 CCCS DELAY VSENS13 SCALE=0.0595 TD=1.1ps
F1103 1001100 0 CCCS DELAY VSENS14 SCALE=0.0424 TD=1.8ps
F1104 1001100 0 CCCS DELAY VSENS21 SCALE=0.6150 TD=0.04ps
F1105 1001100 0 CCCS DELAY VSENS22 SCALE=0.1273 TD=0.6ps
F1106 1001100 0 CCCS DELAY VSENS23 SCALE=0.0594 TD=1.1ps
F1107 1001100 0 CCCS DELAY VSENS24 SCALE=0.0424 TD=1.8ps
F1108 1001100 0 CCCS DELAY VSENS31 SCALE=0.4775 TD=0.08ps
F1109 1001100 0 CCCS DELAY VSENS32 SCALE=0.1261 TD=0.6ps
F1110 1001100 0 CCCS DELAY VSENS33 SCALE=0.0593 TD=1.1ps
F1111 1001100 0 CCCS DELAY VSENS34 SCALE=0.0424 TD=1.8ps

Cx12 0 1001200 2.161F
Rx12 1001201 1001202 0.6951N
Lx12 1001202 1001203 0.0557N
Ry12 1001201 2001202 1.2902N
Ly12 2001202 2001203 0.2658P

Ex1201 1001203 1001204 VCVS DELAY 1001102 1001103 SCALE=0.1237 TD=0.6ps
Ex1202 1001204 1001205 VCVS DELAY 1001302 1001303 SCALE=0.1995 TD=0.6ps
Ex1203 1001205 1001206 VCVS DELAY 1002102 1002103 SCALE=0.1230 TD=0.6ps
Ex1204   1001206 1001207 VCVS DELAY 1002202 1002203 SCALE=0.6133
TD=0.04ps
Ex1205 1001207 1001208 VCVS DELAY 1002302 1002303 SCALE=0.1841 TD=0.6ps
Ex1206 1001208 1001209 VCVS DELAY 1003102 1003103 SCALE=0.1213 TD=0.6ps
Ex1207   1001209 1001210 VCVS DELAY 1003202 1003203 SCALE=0.4451
TD=0.08ps
Ex1208 1001210 1001301 VCVS DELAY 1003302 1003303 SCALE=0.1715 TD=0.6ps

Ey1201 2001203 2001204 VCVS DELAY 2001102 2001103 SCALE=0.1876 TD=0.6ps
Ey1202 2001204 2001205 VCVS DELAY 2001302 2001303 SCALE=0.2289 TD=0.6ps
Ey1203 2001205 2001206 VCVS DELAY 2001402 2001403 SCALE=0.0842 TD=1.1ps
Ey1204 2001206 2001207 VCVS DELAY 2002102 2002103 SCALE=0.1853 TD=0.6ps
Ey1205   2001207 2001208 VCVS DELAY 2002202 2002203 SCALE=0.6490
TD=0.04ps
Ey1206 2001208 2001209 VCVS DELAY 2002302 2002303 SCALE=0.2119 TD=0.6ps
Ey1207 2001209 1002201 VCVS DELAY 2002402 2002403 SCALE=0.0841 TD=1.1ps

F1201 1001200 0 CCCS DELAY VSENS11 SCALE=0.1614 TD=0.6ps
F1202 1001200 0 CCCS DELAY VSENS13 SCALE=0.1280 TD=0.6ps
F1203 1001200 0 CCCS DELAY VSENS13 SCALE=0.0670 TD=1.1ps
F1204 1001200 0 CCCS DELAY VSENS21 SCALE=0.1605 TD=0.6ps
F1205 1001200 0 CCCS DELAY VSENS22 SCALE=0.6155 TD=0.04ps
F1206 1001200 0 CCCS DELAY VSENS23 SCALE=0.1274 TD=0.6ps
F1207 1001200 0 CCCS DELAY VSENS24 SCALE=0.0670 TD=1.1ps
F1208 1001200 0 CCCS DELAY VSENS31 SCALE=0.1586 TD=0.6ps
F1209 1001200 0 CCCS DELAY VSENS32 SCALE=0.4779 TD=0.08ps
F1210 1001200 0 CCCS DELAY VSENS33 SCALE=0.1263 TD=0.6ps
F1211 1001200 0 CCCS DELAY VSENS34 SCALE=0.0668 TD=1.1ps

Cx13 0 1001300 2.161F
Rx13 1001301 1001302 0.6951N
Lx13 1001302 1001303 0.0557N
Ry13 1001301 2001302 1.2902N
Ly13 2001302 2001303 0.2658P

Ex1301 1001303 1001304 VCVS DELAY 1001202 1001203 SCALE=0.1237 TD=0.6ps
Ex1302 1001304 1001305 VCVS DELAY 1001102 1001103 SCALE=0.0555 TD=1.1ps
Ex1303 1001305 1001306 VCVS DELAY 1002102 1002103 SCALE=0.0555 TD=1.1ps
Ex1304 1001306 1001307 VCVS DELAY 1002202 1002203 SCALE=0.1230 TD=0.6ps

Ex1305   1001307   1001308   VCVS   DELAY   1002302   1002303   SCALE=0.6133 TD=0.04ps
Ex1306 1001308 1001309 VCVS DELAY 1003102 1003103 SCALE=0.0554 TD=1.1ps
Ex1307 1001309 1001310 VCVS DELAY 1003202 1003203 SCALE=0.1213 TD=0.6ps
Ex1308   1001310   1001401   VCVS   DELAY   1003302   1003303   SCALE=0.4451 TD=0.08ps

Ey1301 2001303 2001304 VCVS DELAY 2001202 2001203 SCALE=0.1457 TD=0.6ps
Ey1302 2001304 2001305 VCVS DELAY 2001102 2001103 SCALE=0.0736 TD=1.1ps
Ey1303 2001305 2001306 VCVS DELAY 2001402 2001403 SCALE=0.3310 TD=0.6ps
Ey1304 2001306 2001307 VCVS DELAY 2002102 2002103 SCALE=0.0735 TD=1.1ps
Ey1305 2001307 2001308 VCVS DELAY 2002202 2002203 SCALE=0.1444 TD=0.6ps
Ey1306   2001308   2001309   VCVS   DELAY   2002302   2002303   SCALE=0.6490 TD=0.04ps
Ey1307 2001309 1002301 VCVS DELAY 2002402 2002403 SCALE=0.2975 TD=0.6ps

F1301 1001300 0 CCCS DELAY VSENS12 SCALE=0.1280 TD=0.6ps
F1302 1001300 0 CCCS DELAY VSENS11 SCALE=0.0670 TD=1.1ps
F1303 1001300 0 CCCS DELAY VSENS14 SCALE=0.1614 TD=0.6ps
F1304 1001300 0 CCCS DELAY VSENS21 SCALE=0.0670 TD=1.1ps
F1305 1001300 0 CCCS DELAY VSENS22 SCALE=0.1274 TD=0.6ps
F1306 1001300 0 CCCS DELAY VSENS23 SCALE=0.6155 TD=0.6ps
F1307 1001300 0 CCCS DELAY VSENS24 SCALE=0.1605 TD=0.6ps
F1308 1001300 0 CCCS DELAY VSENS31 SCALE=0.0668 TD=1.1ps
F1309 1001300 0 CCCS DELAY VSENS32 SCALE=0.1263 TD=0.6ps
F1310 1001300 0 CCCS DELAY VSENS33 SCALE=0.4779 TD=0.6ps
F1311 1001300 0 CCCS DELAY VSENS34 SCALE=0.1586 TD=0.6ps

Cx14 0 1001400 2.163F
Ry14 1001401 2001402 0.6951N
Ly14 2001402 2001403 0.4385P

Ey1401 2001403 2001404 VCVS DELAY 2001202 2001203 SCALE=0.0461 TD=1.1ps
Ey1402 2001404 2001405 VCVS DELAY 2001302 2001303 SCALE=0.1275 TD=0.6ps
Ey1403 2001405 2001406 VCVS DELAY 2001102 2001103 SCALE=0.0317 TD=1.8ps
Ey1404 2001406 2001407 VCVS DELAY 2002102 2002103 SCALE=0.0317 TD=1.8ps
Ey1405 2001407 2001408 VCVS DELAY 2002202 2002203 SCALE=0.0461 TD=1.1ps
Ey1406 2001408 2001409 VCVS DELAY 2002302 2002303 SCALE=0.1249 TD=0.6ps
Ey1407   2001409   1002401   VCVS   DELAY   2002402   2002403   SCALE=0.5890 TD=0.04ps

F1401 1001400 0 CCCS DELAY VSENS12 SCALE=0.0596 TD=1.1ps
F1402 1001400 0 CCCS DELAY VSENS13 SCALE=0.1281 TD=0.6ps
F1403 1001400 0 CCCS DELAY VSENS11 SCALE=0.0425 TD=1.8ps
F1404 1001400 0 CCCS DELAY VSENS21 SCALE=0.0425 TD=1.8ps
F1405 1001400 0 CCCS DELAY VSENS22 SCALE=0.0595 TD=1.1ps
F1406 1001400 0 CCCS DELAY VSENS23 SCALE=0.1275 TD=0.6ps
F1407 1001400 0 CCCS DELAY VSENS24 SCALE=0.6161 TD=0.04ps
F1408 1001400 0 CCCS DELAY VSENS31 SCALE=0.0425 TD=1.8ps
F1409 1001400 0 CCCS DELAY VSENS32 SCALE=0.0594 TD=1.1ps
F1410 1001400 0 CCCS DELAY VSENS33 SCALE=0.1264 TD=0.6ps
F1411 1001400 0 CCCS DELAY VSENS34 SCALE=0.4784 TD=0.08ps

Cx21 0 1002100 2.160F
Rx21 1002101 1002102 1.2902N
Lx21 1002102 1002103 0.04725N
Ry21 1002101 2002102 0.6951N
Ly21 2002102 2002103 0.4385P

Ex2101 1002103 1002104 VCVS DELAY 1001202 1001203 SCALE=0.2170 TD=0.6ps
Ex2102 1002104 1002105 VCVS DELAY 1001302 1001303 SCALE=0.0738 TD=1.1ps
Ex2103 1002105 1002106 VCVS DELAY 1001102 1001103 SCALE=0.7232 TD=0.04ps
Ex2104 1002106 1002107 VCVS DELAY 1002202 1002203 SCALE=0.2289 TD=0.6ps
Ex2105 1002107 1002108 VCVS DELAY 1002302 1002303 SCALE=0.0739 TD=1.1ps
Ex2106 1002108 1002109 VCVS DELAY 1003102 1003103 SCALE=0.7232 TD=0.04ps
Ex2107 1002109 1002110 VCVS DELAY 1003202 1003203 SCALE=0.2170 TD=0.6ps
Ex2108 1002110 1002201 VCVS DELAY 1003302 1003303 SCALE=0.0738 TD=1.1ps

Ey2101 2002103 2002104 VCVS DELAY 2001202 2001203 SCALE=0.1628 TD=0.6ps
Ey2102 2002104 2002105 VCVS DELAY 2001302 2001303 SCALE=0.0493 TD=1.1ps
Ey2103 2002105 2002106 VCVS DELAY 2001402 2001403 SCALE=0.0332 TD=1.8ps
Ey2104 2002106 2002107 VCVS DELAY 2001102 2001103 SCALE=0.5890 TD=0.04ps
Ey2105 2002107 2002108 VCVS DELAY 2002202 2002203 SCALE=0.1783 TD=0.6ps
Ey2106 2002108 2002109 VCVS DELAY 2002302 2002303 SCALE=0.0494 TD=1.1ps
Ey2107 2002109 1003101 VCVS DELAY 2002402 2002403 SCALE=0.0332 TD=1.8ps

F2101 1002100 0 CCCS DELAY VSENS12 SCALE=0.1276 TD=0.6ps
F2102 1002100 0 CCCS DELAY VSENS13 SCALE=0.0595 TD=1.1ps
F2103 1002100 0 CCCS DELAY VSENS14 SCALE=0.0425 TD=1.8ps
F2104 1002100 0 CCCS DELAY VSENS11 SCALE=0.6757 TD=0.04ps

F2105 1002100 0 CCCS DELAY VSENS22 SCALE=0.1279 TD=0.6ps
F2106 1002100 0 CCCS DELAY VSENS23 SCALE=0.0595 TD=1.1ps
F2107 1002100 0 CCCS DELAY VSENS24 SCALE=0.0425 TD=1.8ps
F2108 1002100 0 CCCS DELAY VSENS31 SCALE=0.6757 TD=0.04ps
F2109 1002100 0 CCCS DELAY VSENS32 SCALE=0.1276 TD=0.6ps
F2110 1002100 0 CCCS DELAY VSENS33 SCALE=0.0595 TD=1.1ps
F2111 1002100 0 CCCS DELAY VSENS34 SCALE=0.0425 TD=1.8ps

Cx22 0 1002200 2.163F
Rx22 1002201 1002202 1.2902N
Lx22 1002202 1002203 0.04725N
Ry22 1002201 2002202 1.2902N
Ly22 2002202 2002203 0.2658P

Ex2201   1002203 1002204 VCVS DELAY 1001202 1001203 SCALE=0.7232 TD=0.04ps
Ex2202 1002204 1002205 VCVS DELAY 1001302 1001303 SCALE=0.2170 TD=0.6ps
Ex2203 1002205 1002206 VCVS DELAY 1002102 1002103 SCALE=0.1457 TD=0.6ps
Ex2204 1002206 1002207 VCVS DELAY 1001102 1001103 SCALE=0.1450 TD=0.6ps
Ex2205 1002207 1002208 VCVS DELAY 1002302 1002303 SCALE=0.2289 TD=0.6ps
Ex2206 1002208 1002209 VCVS DELAY 1003102 1003103 SCALE=0.1450 TD=0.6ps
Ex2207   1002209 1002210 VCVS DELAY 1003202 1003203 SCALE=0.7232 TD=0.04ps
Ex2208 1002210 1002301 VCVS DELAY 1003302 1003303 SCALE=0.2170 TD=0.6ps

Ey2201   2002203 2002204 VCVS DELAY 2001202 2001203 SCALE=0.6490 TD=0.04ps
Ey2202 2002204 2002205 VCVS DELAY 2001302 2001303 SCALE=0.2119 TD=0.6ps
Ey2203 2002205 2002206 VCVS DELAY 2001402 2001403 SCALE=0.0841 TD=1.1ps
Ey2204 2002206 2002207 VCVS DELAY 2002102 2002103 SCALE=0.1876 TD=0.6ps
Ey2205 2002207 2002208 VCVS DELAY 2001102 2001103 SCALE=0.1853 TD=0.6ps
Ey2206 2002208 2002209 VCVS DELAY 2002302 2002303 SCALE=0.2289 TD=0.6ps
Ey2207 2002209 1003201 VCVS DELAY 2002402 2002403 SCALE=0.0842 TD=1.1ps

F2201 1002200 0 CCCS DELAY VSENS12 SCALE=0.6765 TD=0.04ps
F2202 1002200 0 CCCS DELAY VSENS13 SCALE=0.1278 TD=0.6ps
F2203 1002200 0 CCCS DELAY VSENS14 SCALE=0.0671 TD=1.1ps
F2204 1002200 0 CCCS DELAY VSENS21 SCALE=0.1616 TD=0.6ps
F2205 1002200 0 CCCS DELAY VSENS11 SCALE=0.1611 TD=0.6ps
F2206 1002200 0 CCCS DELAY VSENS23 SCALE=0.1281 TD=0.6ps
F2207 1002200 0 CCCS DELAY VSENS24 SCALE=0.0671 TD=1.1ps
F2208 1002200 0 CCCS DELAY VSENS31 SCALE=0.1611 TD=0.6ps

F2209 1002200 0 CCCS DELAY VSENS32 SCALE=0.6765 TD=0.04ps
F2210 1002200 0 CCCS DELAY VSENS33 SCALE=0.1278 TD=0.6ps
F2211 1002200 0 CCCS DELAY VSENS34 SCALE=0.0671 TD=1.1ps

Cx23 0 1002300 2.163F
Rx23 1002301 1002302 1.2902N
Lx23 1002302 1002303 0.04725N
Ry23 1002301 2002302 1.2902N
Ly23 2002302 2002303 0.2658P

Ex2301 1002303 1002304 VCVS DELAY 1001202 1001203 SCALE=0.1450 TD=0.6ps
Ex2302   1002304 1002305 VCVS DELAY 1001302 1001303 SCALE=0.7232
TD=0.04ps
Ex2303 1002305 1002306 VCVS DELAY 1002102 1002103 SCALE=0.0654 TD=1.1ps
Ex2304 1002306 1002307 VCVS DELAY 1002202 1002203 SCALE=0.1457 TD=0.6ps
Ex2305 1002307 1002308 VCVS DELAY 1001102 1001103 SCALE=0.0654 TD=1.1ps
Ex2306 1002308 1002309 VCVS DELAY 1003102 1003103 SCALE=0.0654 TD=1.1ps
Ex2307 1002309 1002310 VCVS DELAY 1003202 1003203 SCALE=0.1450 TD=0.6ps
Ex2308   1002310 1002401 VCVS DELAY 1003302 1003303 SCALE=0.7232
TD=0.04ps

Ey2301 2002303 2002304 VCVS DELAY 2001202 2001203 SCALE=0.1444 TD=0.6ps
Ey2302   2002304 2002305 VCVS DELAY 2001302 2001303 SCALE=0.6490
TD=0.04ps
Ey2303 2002305 2002306 VCVS DELAY 2001402 2001403 SCALE=0.2975 TD=0.6ps
Ey2304 2002306 2002307 VCVS DELAY 2002102 2002103 SCALE=0.0736 TD=1.1ps
Ey2305 2002307 2002308 VCVS DELAY 2002202 2002203 SCALE=0.1457 TD=0.6ps
Ey2306 2002308 2002309 VCVS DELAY 2001102 2001103 SCALE=0.0735 TD=1.1ps
Ey2307 2002309 1003301 VCVS DELAY 2002402 2002403 SCALE=0.3310 TD=0.6ps

F2301 1002300 0 CCCS DELAY VSENS12 SCALE=0.1278 TD=0.6ps
F2302 1002300 0 CCCS DELAY VSENS13 SCALE=0.6765 TD=0.04ps
F2303 1002300 0 CCCS DELAY VSENS14 SCALE=0.1611 TD=0.6ps
F2304 1002300 0 CCCS DELAY VSENS21 SCALE=0.0671 TD=1.1ps
F2305 1002300 0 CCCS DELAY VSENS22 SCALE=0.1281 TD=0.6ps
F2306 1002300 0 CCCS DELAY VSENS11 SCALE=0.0671 TD=1.1ps
F2307 1002300 0 CCCS DELAY VSENS24 SCALE=0.1616 TD=0.6ps
F2308 1002300 0 CCCS DELAY VSENS31 SCALE=0.0671 TD=1.1ps
F2309 1002300 0 CCCS DELAY VSENS32 SCALE=0.1278 TD=0.6ps
F2310 1002300 0 CCCS DELAY VSENS33 SCALE=0.6765 TD=0.04ps
F2311 1002300 0 CCCS DELAY VSENS34 SCALE=0.1611 TD=0.6ps

Cx24 0 1002400 2.164F
Ry24 1002401 2002402 0.6951N
Ly24 2002402 2002403 0.4385P

Ey2401 2002403 2002404 VCVS DELAY 2001202 2001203 SCALE=0.0461 TD=1.1ps
Ey2402 2002404 2002405 VCVS DELAY 2001302 2001303 SCALE=0.1249 TD=0.6ps
Ey2403   2002405 2002406 VCVS DELAY 2001402 2001403 SCALE=0.5890 TD=0.04ps
Ey2404 2002406 2002407 VCVS DELAY 2002102 2002103 SCALE=0.0317 TD=1.8ps
Ey2405 2002407 2002408 VCVS DELAY 2002202 2002203 SCALE=0.0461 TD=1.1ps
Ey2406 2002408 2002409 VCVS DELAY 2002302 2002303 SCALE=0.1275 TD=0.6ps
Ey2407 2002409 1003401 VCVS DELAY 2001102 2001103 SCALE=0.0317 TD=1.8ps

F2401 1002400 0 CCCS DELAY VSENS12 SCALE=0.0596 TD=1.1ps
F2402 1002400 0 CCCS DELAY VSENS13 SCALE=0.1278 TD=0.6ps
F2403 1002400 0 CCCS DELAY VSENS14 SCALE=0.6768 TD=0.04ps
F2404 1002400 0 CCCS DELAY VSENS21 SCALE=0.0425 TD=1.8ps
F2405 1002400 0 CCCS DELAY VSENS22 SCALE=0.0596 TD=1.1ps
F2406 1002400 0 CCCS DELAY VSENS23 SCALE=0.1281 TD=0.6ps
F2407 1002400 0 CCCS DELAY VSENS11 SCALE=0.0425 TD=1.8ps
F2408 1002400 0 CCCS DELAY VSENS31 SCALE=0.0425 TD=1.8ps
F2409 1002400 0 CCCS DELAY VSENS32 SCALE=0.0596 TD=1.1ps
F2410 1002400 0 CCCS DELAY VSENS33 SCALE=0.1278 TD=0.6ps
F2411 1002400 0 CCCS DELAY VSENS34 SCALE=0.6768 TD=0.04ps

Cx31 0 1003100 2.160F
Rx31 1003101 1003102 0.6951N
Lx31 1003102 1003103 0.0557N

Ex3101 1003103 1003104 VCVS DELAY 1001202 1001203 SCALE=0.1715 TD=0.6ps
Ex3102 1003104 1003105 VCVS DELAY 1001302 1001303 SCALE=0.0625 TD=1.1ps
Ex3103   1003105 1003106 VCVS DELAY 1002102 1002103 SCALE=0.6133 TD=0.04ps
Ex3104 1003106 1003107 VCVS DELAY 1002202 1002203 SCALE=0.1841 TD=0.6ps
Ex3105 1003107 1003108 VCVS DELAY 1002302 1002303 SCALE=0.0626 TD=1.1ps
Ex3106   1003108 1003109 VCVS DELAY 1001102 1001103 SCALE=0.4451 TD=0.08ps
Ex3107 1003109 1003110 VCVS DELAY 1003202 1003203 SCALE=0.1995 TD=0.6ps
Ex3108 1003110 1003201 VCVS DELAY 1003302 1003303 SCALE=0.0627 TD=1.1ps

F3101 1003100 0 CCCS DELAY VSENS12 SCALE=0.1262 TD=0.6ps
F3102 1003100 0 CCCS DELAY VSENS13 SCALE=0.0594 TD=1.1ps
F3103 1003100 0 CCCS DELAY VSENS14 SCALE=0.0424 TD=1.8ps
F3104 1003100 0 CCCS DELAY VSENS21 SCALE=0.6153 TD=0.04ps
F3105 1003100 0 CCCS DELAY VSENS22 SCALE=0.1273 TD=0.6ps
F3106 1003100 0 CCCS DELAY VSENS23 SCALE=0.0594 TD=1.1ps
F3107 1003100 0 CCCS DELAY VSENS24 SCALE=0.0425 TD=1.8ps
F3108 1003100 0 CCCS DELAY VSENS11 SCALE=0.4777 TD=0.08ps
F3109 1003100 0 CCCS DELAY VSENS32 SCALE=0.1279 TD=0.6ps
F3110 1003100 0 CCCS DELAY VSENS33 SCALE=0.0595 TD=1.1ps
F3111 1003100 0 CCCS DELAY VSENS34 SCALE=0.0425 TD=1.8ps

Cx32 0 1003200 2.162F
Rx32 1003201 1003202 0.6951N
Lx32 1003202 1003203 0.0557N
Ex3201   1003203 1003204 VCVS DELAY 1001202 1001203 SCALE=0.4451 TD=0.08ps
Ex3202 1003204 1003205 VCVS DELAY 1001302 1001303 SCALE=0.1715 TD=0.6ps
Ex3203 1003205 1003206 VCVS DELAY 1002102 1002103 SCALE=0.1230 TD=0.6ps
Ex3204   1003206 1003207 VCVS DELAY 1002202 1002203 SCALE=0.6133 TD=0.04ps
Ex3205 1003207 1003208 VCVS DELAY 1002302 1002303 SCALE=0.1841 TD=0.6ps
Ex3206 1003208 1003209 VCVS DELAY 1003102 1003103 SCALE=0.1237 TD=0.6ps
Ex3207 1003209 1003210 VCVS DELAY 1001102 1001103 SCALE=0.1213 TD=0.6ps
Ex3208 1003210 1003301 VCVS DELAY 1003302 1003303 SCALE=0.1995 TD=0.6ps

F3201 1003200 0 CCCS DELAY VSENS12 SCALE=0.4783 TD=0.08ps
F3202 1003200 0 CCCS DELAY VSENS13 SCALE=0.1264 TD=0.6ps
F3203 1003200 0 CCCS DELAY VSENS14 SCALE=0.0669 TD=1.1ps
F3204 1003200 0 CCCS DELAY VSENS21 SCALE=0.1606 TD=0.6ps
F3205 1003200 0 CCCS DELAY VSENS22 SCALE=0.6161 TD=0.04ps
F3206 1003200 0 CCCS DELAY VSENS23 SCALE=0.1275 TD=0.6ps
F3207 1003200 0 CCCS DELAY VSENS24 SCALE=0.0670 TD=1.1ps
F3208 1003200 0 CCCS DELAY VSENS31 SCALE=0.1616 TD=0.6ps
F3209 1003200 0 CCCS DELAY VSENS11 SCALE=0.1587 TD=0.6ps
F3210 1003200 0 CCCS DELAY VSENS33 SCALE=0.1281 TD=0.6ps
F3211 1003200 0 CCCS DELAY VSENS34 SCALE=0.0671 TD=1.1ps

Cx33 0 1003300 2.162F
Rx33 1003301 1003302 0.6951N
Lx33 1003302 1003303 0.0557N

Ex3301 1003303 1003304 VCVS DELAY 1001202 1001203 SCALE=0.1213 TD=0.6ps
Ex3302   1003304 1003305 VCVS DELAY 1001302 1001303 SCALE=0.4451
TD=0.08ps
Ex3303 1003305 1003306 VCVS DELAY 1002102 1002103 SCALE=0.0555 TD=1.1ps
Ex3304 1003306 1003307 VCVS DELAY 1002202 1002203 SCALE=0.1230 TD=0.6ps
Ex3305   1003307 1003308 VCVS DELAY 1002302 1002303 SCALE=0.6133
TD=0.04ps
Ex3306 1003308 1003309 VCVS DELAY 1003102 1003103 SCALE=0.0555 TD=1.1ps
Ex3307 1003309 1003310 VCVS DELAY 1003202 1003203 SCALE=0.1237 TD=0.6ps
Ex3308 1003310 1003401 VCVS DELAY 1001102 1001103 SCALE=0.0554 TD=1.1ps

F3301 1003300 0 CCCS DELAY VSENS12 SCALE=0.1264 TD=0.6ps
F3302 1003300 0 CCCS DELAY VSENS13 SCALE=0.4783 TD=0.08ps
F3303 1003300 0 CCCS DELAY VSENS14 SCALE=0.1587 TD=0.6ps
F3304 1003300 0 CCCS DELAY VSENS21 SCALE=0.0670 TD=1.1ps
F3305 1003300 0 CCCS DELAY VSENS22 SCALE=0.1275 TD=0.6ps
F3306 1003300 0 CCCS DELAY VSENS23 SCALE=0.6161 TD=0.04ps
F3307 1003300 0 CCCS DELAY VSENS24 SCALE=0.1606 TD=0.6ps
F3308 1003300 0 CCCS DELAY VSENS31 SCALE=0.0671 TD=1.1ps
F3309 1003300 0 CCCS DELAY VSENS32 SCALE=0.1281 TD=0.6ps
F3310 1003300 0 CCCS DELAY VSENS11 SCALE=0.0669 TD=1.1ps
F3311 1003300 0 CCCS DELAY VSENS34 SCALE=0.1616 TD=0.6ps

Cx34 0 1003400 2.163F

F3401 1003400 0 CCCS DELAY VSENS12 SCALE=0.0594 TD=1.1ps
F3402 1003400 0 CCCS DELAY VSENS13 SCALE=0.1264 TD=0.6ps
F3403 1003400 0 CCCS DELAY VSENS14 SCALE=0.4784 TD=0.08ps
F3404 1003400 0 CCCS DELAY VSENS21 SCALE=0.0425 TD=1.8ps
F3405 1003400 0 CCCS DELAY VSENS22 SCALE=0.0595 TD=1.1ps
F3406 1003400 0 CCCS DELAY VSENS23 SCALE=0.1275 TD=0.6ps
F3407 1003400 0 CCCS DELAY VSENS24 SCALE=0.6161 TD=0.04ps
F3408 1003400 0 CCCS DELAY VSENS31 SCALE=0.0425 TD=1.8ps
F3409 1003400 0 CCCS DELAY VSENS32 SCALE=0.0596 TD=1.1ps
F3410 1003400 0 CCCS DELAY VSENS33 SCALE=0.1281 TD=0.6ps
F3411 1003400 0 CCCS DELAY VSENS11 SCALE=0.0425 TD=1.8ps
.END

APPENDIX F

OPTIMIZATION: MINIMUM, CONVERGENCE AND NOISE SENSITIVITY

To find the minimum of a function $R(\mathbf{v})$, an $n \times 1$ vector $\mathbf{e}$ is first defined such that $|\mathbf{e}| \leq \varepsilon$, for a real positive constant radius ε. For a region $\Re$ that contains a minimum $\mathbf{v}_{min}$ such that for all $\mathbf{e}$ in the hyperspace of radius ε and center at origin, $\{\mathbf{v}_{min} \pm \mathbf{e}\} \in \Re$, the relation

$$R(\mathbf{v}_{min}) < R(\mathbf{v}_{min} \pm \mathbf{e}), \forall \{\mathbf{v}_{min} \pm \mathbf{e}\} \in \Re, \qquad (F.1)$$

is satisfied. A Taylor series expansion of $R(\mathbf{v}_{min} + \mathbf{e})$ leads to

$$R(\mathbf{v}_{min} \pm \mathbf{e}) = R(\mathbf{v}_{min}) \pm \{\nabla_{\mathbf{v}} R(\mathbf{v}_{min})\}^T \mathbf{e} + \frac{1}{2} \mathbf{e}^T \{\nabla_{\mathbf{v}}^2 R(\mathbf{v}_{min})\} \mathbf{e} \pm \cdots. \qquad (F.2)$$

From equations (F.1) and (F.2), $R(\mathbf{v}_{min}) < R(\mathbf{v}_{min} \pm \mathbf{e})$ implies that $\pm \{\nabla_{\mathbf{v}} R(\mathbf{v}_{min})\}^T \mathbf{e} > \mathbf{0}$ can be satisfied for non-trivial values of $\mathbf{e}$ only if $\nabla_{\mathbf{v}} R(\mathbf{v}_{min}) = \mathbf{0}$ where $\mathbf{0}$ denotes the n x 1 null vector.

The equation (F.2) is simplified by $\nabla_{\mathbf{v}} R(\mathbf{v}_{min}) = \mathbf{0}$ yielding

$$R(\mathbf{v}_{min} \pm \mathbf{e}) = R(\mathbf{v}_{min}) + \frac{1}{2} \mathbf{e}^T \{\nabla_{\mathbf{v}}^2 R(\mathbf{v}_{min})\} \mathbf{e} \pm \cdots. \qquad (F.3)$$

Again, $\mathbf{e}^T \{\nabla_{\mathbf{v}}^2 R(\mathbf{v}_{min})\} \mathbf{e} \geq 0$ is implied from $R(\mathbf{v}_{min}) < R(\mathbf{v}_{min} \pm \mathbf{e})$. That is, $\nabla_{\mathbf{v}}^2 R(\mathbf{v}_{min})$ is positive semi-definite such that $\det \nabla_{\mathbf{v}}^2 R(\mathbf{v}_{min}) \geq 0$. Thus the problem of finding the

minimum of $R(\mathbf{v})$ amounts to that of finding $\mathbf{v}$ which solves $\nabla_{\mathbf{v}} R(\mathbf{v}_{min}) = \mathbf{0}$, subject to

$\det \nabla_{\mathbf{v}}^2 R(\mathbf{v}_{min}) \geq 0$. A Newton-Raphson method is then used to derive the solution [83].

Convergence rate of the method is derived as follows: Let $v = r$ be a solution point of the function $R(v)$ which is assumed, without loss of generality, to depend on single variable v. Expanding $R(v)$ around the solution point up to the quadratic term gives

$$R(v) = R(r) + (v-r)R'(r) + \frac{1}{2}(v-r)^2 R''(r). \qquad (F.4)$$

Differentiating equation (F.4) leads to

$$R'(v) = R'(r) + (v-r)R''(r). \qquad (F.5)$$

The two successive $(k+1)^{th}$ and k^{th} terms of the Newton-Raphson algorithm are related by

$$v_{k+1} = v_k - \frac{R(v_k)}{R'(v_k)}. \qquad (F.6)$$

Let E_{k+1} be the error made at the $(k+1)^{th}$ step. Then,

$$E_{k+1} = v_{k+1} - r. \qquad (F.7)$$

Substitution of equations (F.4) and (F.5) in equation (F.7) and further simplification gives

$$E_{k+1} = E_k \left[1 - \frac{1 + \left(\dfrac{E_k}{2}\right)\left(\dfrac{R''(r)}{R'(r)}\right)}{1 + E_k\left(\dfrac{R''(r)}{R'(r)}\right)} \right]. \qquad (F.8)$$

E_{k+1} is, thus, approximately given as

$$E_{k+1} \square\, E_k \left(\frac{E_k}{2}\right)\frac{R''(r)}{R'(r)}. \qquad (F.9)$$

Equation (F.9) shows that the error at $(k+1)^{th}$ step is approximately proportional to the square of the error at the kth step. Thus the algorithm is quadratically convergent.

To derive an expression for sensitivity of the solution to noise, let **x** be the solution of the linear system

$$\mathbf{A}\mathbf{x} = \mathbf{b} .$$ (F.10)

Let **x*** be the solution of the perturbed system with measurement noise **n** such that

$$\mathbf{A}(\mathbf{x} + \boldsymbol{\delta}) = \mathbf{b} + \mathbf{n} ,$$ (F.11)

where $\boldsymbol{\delta} = \mathbf{x}^* - \mathbf{x}$. Subtracting equation (F.10) from equation (F.11), we get

$$\mathbf{A}\boldsymbol{\delta} = \mathbf{n} .$$ (F.12)

Equation (F.12) can be represented by an inequality using vector and matrix norms as

$$\left\| \boldsymbol{\delta} \right\| \le \left\| \mathbf{A}^{-1} \right\| \cdot \left\| \mathbf{n} \right\| .$$ (F.13)

Also, equation (F.10) is represented by inequality of norms as

$$\left\| \mathbf{b} \right\| = \left\| \mathbf{A}\mathbf{x} \right\| \le \left\| \mathbf{A} \right\| \cdot \left\| \mathbf{x} \right\| .$$ (F.14)

Combining the inequalities (F.13) and (F.14), we get

$$\frac{\left\| \boldsymbol{\delta} \right\|}{\left\| \mathbf{x} \right\|} \le \left\| \mathbf{A} \right\| \cdot \left\| \mathbf{A}^{-1} \right\| \cdot \frac{\left\| \mathbf{n} \right\|}{\left\| \mathbf{b} \right\|} ,$$ (F.15)

where $\left\| \mathbf{A} \right\| \cdot \left\| \mathbf{A}^{-1} \right\|$ refers to the condition number of matrix **A**. Equation (F.15) shows that the relative change in the solution is linearly bounded by the condition number times the measurement uncertainty due to noise.