Simulation and Fabrication of an Interposer for Electrical Testing of Fine-Pitch Wafer Level Packages

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Summary

This thesis describes the design, fabrication and characterization of a new MEMS-based interposer which serves as the electro-mechanical interface between the device chip under test and the test processor. The interposer has vertical through wafer interconnection and capable of probing area array pins. It is designed to meet the requirement of fanning out the 100um pitch chip-to-substrate interconnections to about 750um pitch which is compatible with current printed circuit board processing technology. It has three build-up metal layers on top of a silicon substrate, in turn named power plane, ground plane and compliant structure. It is fabricated on a silicon substrate by semiconductor and micro-machining processes. Through-wafer vias are formed by potassium hydroxide anisotropic etching. Conductive materials are filled in the vias to form an interconnection. The compliant structures which give vertical compliance to the probe pads are released by XeF2. The high frequency electrical characteristics were evaluated using software HFSS. As the substrate is made of silicon, there is no thermal mismatch between chip and substrate and hence no thermal stress induced during wafer level burn-in testing. This is an important advantage of using a silicon interposer.

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CHARPTER 1: Introduction

1.1 Project Background

An electronic package has four main functions: to protect, power, cool the microelectronic chip or component, and to provide electrical and mechanical connection between the chip and the outside world.

As microelectronic components have evolved from a single transistor to highly complex integrated circuits (ICs), packaging technology has also advanced from a simple metal can to complex multi-layer ceramic and plastic structures to provide packaging solutions to the growing microelectronics industry. There are mainly two categories of packaging according to their input/output (I/O) layout. One is peripheral packaging whose I/Os are only located at the periphery of the chips and the other is area array whose I/Os are populated all over the area of the chips. Peripheral packages include DIPs (Dual In Line Packages), SOPs (Small Outline Packages), QFPs (Quad Flat Packages). Area array packages refer to Flip Chips, BGAs (Ball Grid Arrays) and CSPs (Chip Scale Packages). Though there are so many kinds of packages, each of them has its own application and limitations. The DIP was the first package invented by Bryant Rogers of Fairchild in the early 1960s. It has a large lead pitch, which is a limitation when space is a critical design constraint. The SOP is well suited for 24 to 48 pin memory packaging in space-constrained applications. The QFP is another member of the family of peripherally-leaded packages, but its leadframe runs around on all four sides of the package enabling higher pin counts, up to 304 pins, although most common usage is in the 48 to 128 range. When resistance to high temperature and humidity becomes an important design parameter, a ceramic QFP is a good choice. BGA was the first high volume pin grid array package and had remained the primary

package solution for microprocessor units since its successful implementation in 1982 for 286 microprocessors. However its higher price prevents it from taking a bigger share of the market. It is only cost effective for device with greater than 250 I/Os.

The emergence of chip scaled packages (CSPs) has dramatically changed the landscape for array packages. In recent years, it has become one of the most important package types due to the unprecedented demand for portable and handheld devices, such as cell phones, digital cameras, etc. One of the unique features of most CSPs is that it uses a substrate or metal layer to redistribute the fine-pitch (as small as 75μm) peripheral (or staggered) pads on the chip to a much larger pitch (1mm, 0.8mm, 0.75mm and 0.5mm) area array pads on the PCB, or FPC, or glass. The CSP has advantages over direct chip attach (DCA). With the substrate the CSP is easier to test-at–speed and burn-in for known good die (KGD), to handle, to assemble, to rework, to standardize, to protect the die, to deal with die shrink and expand, and it is subjected to less infrastructure constraints. It becomes the choice of packaging engineers. From 1993 to 2000, 52 types of CSPs have been introduced in the market that differs in structures, materials, and interconnecting systems. It follows the traditional IC packaging fabrication steps. At the completion of wafer fabrication, the wafer is diced into individual chips. The functional chips are placed in a temporary testing socket to test for functionality and reliability under various conditions. The chips that survive this “burn-in” stage are then placed into permanent package and re-tested before they are made available for system assembly on the printed wiring board (PWB).The steps associated with this process flow involve a single chip at a time (i.e. chips are individually tested, packaged, and assembled on the PWB). This approach is expensive and inefficient. A novel packaging technology is needed to address the requirements of modern and future microelectronic systems, which have higher levels of integration,

higher performance and increasing functionality.

According to The International Technology Roadmap for Semiconductors (ITRS, 2002), the existing packaging technologies are incapable of addressing the cost, performance, functional, heat removal and size requirements of future generations of semiconductor ICs. Wafer-Level Packaging (WLP) appears to have all the fundamental advantages of cost, size, electrical performance and reliability as compared to other conventional packages. Wafer-level package is IC packaging formed at wafer level on the wafer in the wafer foundry. It is a novel concept of packaging that the entire wafer is packaged at the same time instead of packaging one chip at a time. In this process, the front-end IC fabrication and back-end IC assembly are performed at the wafer foundry. The process flow for wafer level packages is dramatically different from conventional technologies including chip scale packages as can be seen from Fig. 1.1. (Vasquez & Lindsey, 1994)

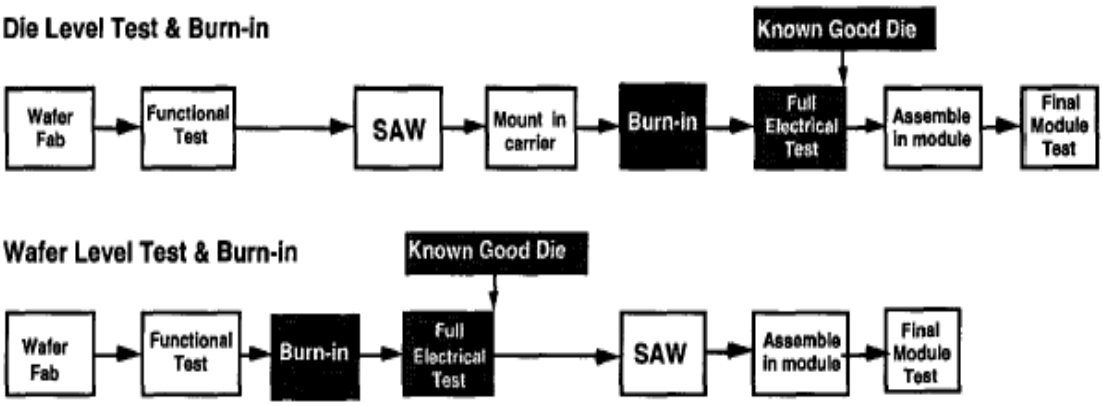


Fig. 1. 1 Comparison of WLP and conventional Packaging Process Flow
(Vasquez & Lindsey, 1994)

Immediately after the completion of wafer fabrication and before test, IC connections are formed with a few more steps on the wafer, then encapsulating, testing and singulating into individually functional packaged chips. These packaged parts are then

assembled onto the system board. As a result of the new process flow, the WLP significantly lowers manufacturing cost of the package. Wafer-level packaging is expected to provide a number of benefits that include (Tummala, 2001):

- Smallest IC package size as it is a truly chip-size package (CSP);
- Lowest cost per I/O because the interconnections are all done at the wafer level in one set of parallel steps;
- Lowest cost of electrical testing as this is done at the wafer level;
- Lowest burn-in cost as burn-in is done at the wafer level;
- Eliminates underfill because of compliancy of leads or other ways to achieve reliability
- Enhances electrical performance because of the short interconnections.

Among these, size and cost are the most important two factors driving the WLP development.

Nano wafer level packaging (NWLP) is an advanced version of WLP by employing Nano materials and structures to realize WLP for future ICs with fine pitches and greater number of I/Os. It will bring about unprecedented advances in electrical, mechanical, and thermal properties in the chip-to-package interconnections. It has finer pitches and higher I/O densities as the industry would develop to have. At present, the work in this novel packaging technology is still in its early stage.

1.2 Motivation for the Work

As traditional packaging technology cannot fulfill the requirement of greatly reducing cost, nano-wafer level packaging (NWLP) is steadily becoming the future choice and research on this new packaging technology is currently being intensely pursued. The project "Nano-wafer Level Packaging" is an international research and education collaboration between the National University of Singapore, the Institute of Microelectronics, Singapore and Georgia Institute of Technology Packaging Research Center, USA. It is an effort to advance the research towards fine pitch packaging. The team is presently investigating the materials, processes, electrical and mechanical properties and test and burn-in methods relating to this new packaging technology.

The work described in this thesis is only a part of the entire NWLP project. It is to develop and fabricate an interposer which implements the test task for the WLP at 100μm pitch. Our approach will make use of the existing silicon processing technology to fabricate the interposer. The challenges are materials selection and process integration in the fabrication of the fine pitch interposer with the limitation of the equipment. This work is focused on the process development and integration.

Simulation is a powerful tool which allows us to examine the process effect on device structure as well as device performance. Software HFSS and HPADS have been used to simulate the interposer structure. It gives us a hint on the future design.

1.3 Objectives of the Work

The interposer was fabricated at the Institute of Microelectronics, Singapore. The test signal processor was designed and fabricated at Georgia Tech Packaging Research Center, USA. After both are fabricated, the test processor will be integrated onto the interposer to form the TSP interposer which will undertake the task of test and burn-in for 100um pitch wafer.

The main objective of the work is to prove the concept of the interposer, to work out the process which can be utilized in the fabrication of the interposer for the NWLP test. Once the process is proved workable, future optimized design of the same feature sizes can be implemented.

The first phase of the research is to design and fabricate the test structures. The layout design of test structures is realized through Cadence^{TM}. Several variations are employed in the design to fully explore the effects of those parameters on the final performance and process feasibilities in IME. These parameters include line width, layout of test structures as well as alternative processes flows and methods. In the meanwhile, design parameter optimization is investigated by simulation. A lot of attention has been paid on the fabrication process, because the control of process parameters affects the final device availability and performance. Visual inspection is performed using Scanning Electron Microscope (SEM). Analyses are performed based on the SEM images.

1.4 Organization of the Thesis

This thesis is divided into five chapters.

Chapter 1 provides a brief introduction to the evolution of packaging, and why we need nano wafer level packaging. Motivation and objectives of the work are introduced.

Chapter 2 is a review of the literature related to this work. Background of the known good die technology is given and major probe cards are introduced.

The concept of the interposer and the design strategies are discussed in Chapter 3. The interposer structures are presented. The layout design and fabrication process flow are involved and in-depth details of these procedures are given in this chapter.

In Chapter 4, nano-indentation test method is described. Mechanical and electrical simulations are also described.

Chapter 5 concludes the work finished within this project. A few suggestions for future research work are given.

CHAPTER 2: Literature Review

2.1 Background of Probe Card Technologies

Wafer level packaging has distinct advantages compared to traditional ones, but it is incomplete without guaranteeing known-good-dies (KGDs). A lot of people published papers and books to address the importance of KGD technology and the related problems (Agahdel et al., 1993; Vasquez et al., 1993a,b; Prokopchak et al., 1994; Lau, 1995a,b,c; Arnold et al., 1998; Atwood et al., 1998; Hodges et al., 1998). Packaging costs are increasing with the complexity of IC's. In order to minimize the costs, complete ac, dc and functional testing at wafer level is becoming increasingly important. By rejecting the defective component at the early stage unnecessary packaging costs are avoided. The probe cards, which act as interfacial communication between the tester and the device under test, are the critical performance element. As devices become more intricate, sophisticated test probe cards which have faster speed, smaller pitches, parallel testing chip capability and which can be automatically loaded, positioned and aligned to the wafer are needed (Barsotti et al., 1988).

Various approaches have been brought up in the past several years (Bates et al., 1997; Beiley et al., 1992a,b, 1995a,b), but none of them has satisfactorily solved the problems in producing KGD on the wafer level. In order to test the die, satisfactory contact force must be produced by the probe to ensure the good electrical performance. Many people have been dedicated to solve this problem. Different kinds of probes and different contact methods have been produced. A membrane probe with pyramidal tips was reported by Kasukabe et al.(1998). Kataoka introduced a low contact force probe utilizing fritting contacts (2002). Other methods such as thermally actuated probe cards

and electrostatically actuated probe card were also reported. (Zhang et al., 1997; Shingo et al., 2003). Cho et al. developed a probe with knife-edged tips in 2003. All these efforts were made on producing a good contact force. For the full wafer contact, it is even more difficult. There are some papers introducing the technology of full wafer test (Zhang et al., 1997; Pandey et al. 1998; Soejima et al., 1999), but the problems are not fully solved. It hinders the development of test and burn-in technology. This indicates that test and burn-in technology has become bottleneck in driving the packaging cost further down. A cheap and novel test and burn-in method is desperately needed. In the past, wafer burn-in did not use a test carrier (Singh, 1994), but it required that power, ground and clock connections to each die be fabricated on the wafer so that circuit could be powered up and clocked using a few probe connects on the wafer. These extra connections complicate die design and occupy effective die area. Furthermore, any failure in these test connections can disable the testing of large part of the wafer. Thus, this method is not practical or at least needs further optimization. Presently, most of the research is focused on the device-level burn-in (DLBI) using a temporary carrier. The carrier technologies thus became the hinge in successful burn-in process. To produce an effective burn-in carrier, the biggest challenge lies in how to make a compliant contact between the die pads and the test probes evenly without damaging the pads while providing reliable electrical contact. There have been many efforts to address this question in the past 20 years. A lot of probe cards have been reported. Some probe cards are based on material properties to absorb the contact force, for example, deformable solder bumps, and membrane probes; while others are designed into special test structures to get compliant contact, i. e., FormFactor MicroSpring. Each has its unique properties, but none of them has met all the requirements needed in the fast developing IC industry.

2.2 Typical Probe Cards

2.2.1 Epoxy Ring Probe Card

The epoxy ring probe card is one of the earliest probe cards. It consists of a controlled impedance signal on a PCB substrate to which variable lengths of cantilevered wires of uncontrolled impedance are attached. The wire materials are tungsten, palladium or beryllium-copper. It is a kind of cantilever beam probe. Its main advantages are relatively low cost, reparability and it stands for the industry standard. But this kind of probe card has fundamental limitations for measuring high frequency signals, due mostly to the large parasitic associated with the probe tips. The cards are incapable of probing high I/O chips because of its big probe tips.

2.2.2 Membrane Probe

The membrane probe was first proposed in 1986. Since then, the idea has received a lot of attention (Leung et al., 1993, 1995). Barsotti reported a vey high density (VHD) probe card (Barsotti et al., 1988). Hewlett-Packard's Circuit Technology R&D Laboratories also developed a proprietary technology for the design and fabrication of such probes (Leslie and Matta, 1988, 1989). The concept is illustrated in Fig. 2.1. A flexible dielectric membrane supports a set of microstrip transmission lines that connect the test electronics to the device under test (DUT). Each transmission line is formed by a conductor trace patterned on the side of dielectric membrane and a thin metal film on the opposite side, which acts as a common ground plane. The width of the trace is chosen to obtain the desired line impedance to match a particular device technology. Contact to the DUT is made by an array of micro-contacts which are formed at the end of the transmission line through via holes in the membrane.

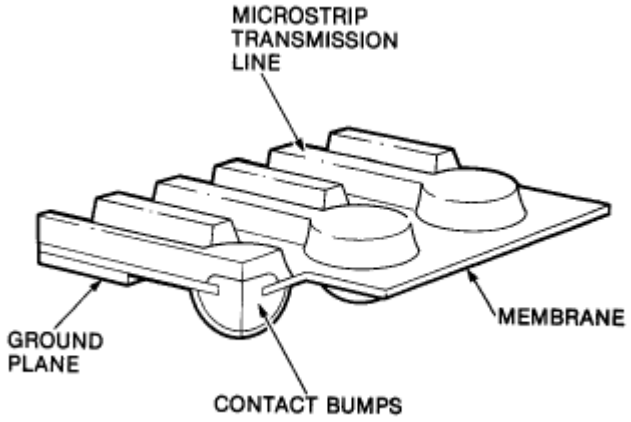


Fig. 2. 1 Basic Concept of Membrane Probe (Leslie and Matta, 1988)

The membrane probe card has many advantages over the epoxy needle probe card such as lower parasitic inductance, controlled impedance tips and improved mechanical reliability. Because of its merits, a lot of scientific groups developed many kinds of probe cards based on the membrane concept and each has its own unique properties.

In 1994, You Kondoh and Toshiaki Ueno proposed a new type of probe (Kondoh and Ueno, 1994). They called it “Universal Membrane Probe” (UMP), which consists of tape automated bond (TAB) tap mounted with an array of micro-bumps, instead of the conventional needles. Fig. 2.2 shows the UMP structure. An elastic material such as rubber is chosen to reduce the pressure difference due to the uneven die surface. This UMP can be applied to a variety of die sizes and pad configurations as can be shown in Fig. 2.3. The UMP has radial wiring line patterns on which the pitch of bumps equal to typical I/O pads, as a result only one of the bumps connected to a particular wire will come into contact with a pad. This makes it applicable to many

die designs. After test, it is found that the bump contact is not as good as scrubbing probe which can break through the local oxide film of aluminum to obtain good electrical conduction. The bump shape and size need to be optimized to improve the situation.

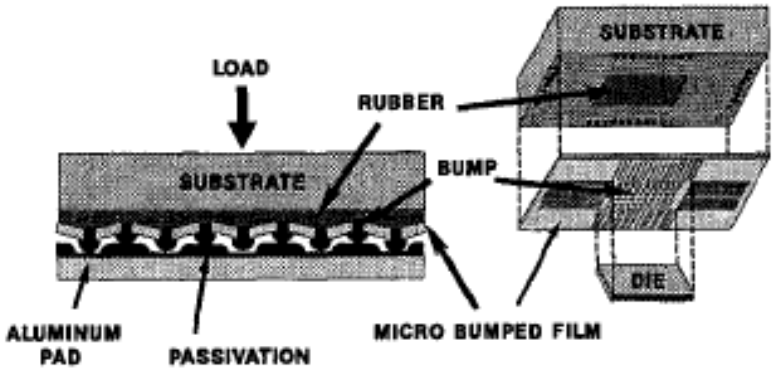


Fig. 2. 2 UMP Structure (Kondoh and Ueno, 1994)

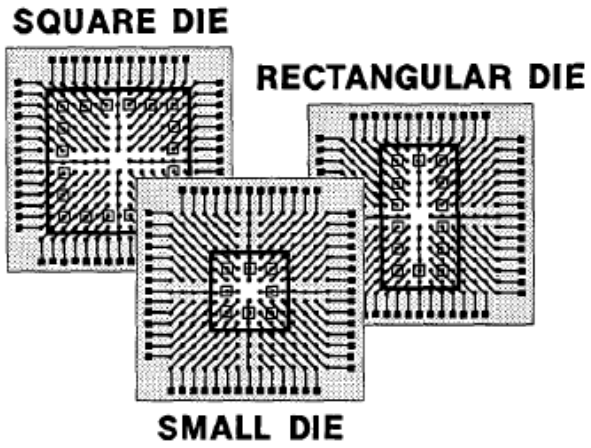


Fig. 2. 3 UMP Pattern and Different Die Sizes (Kondoh and Ueno, 1994)

Another approach based on TAB technology was proposed by Salatino and Nolan [Salatino et al., 1994]. In this method, the contact finger is bent up to an angle that would produce a lateral scrubbing motion as the chip is pushed down against them. This makes a good contact. Under the slope of the fingers a backfill of silicone material was added to provide compliancy. Fig. 2.4 shows the bent leads with silicone

underfill.

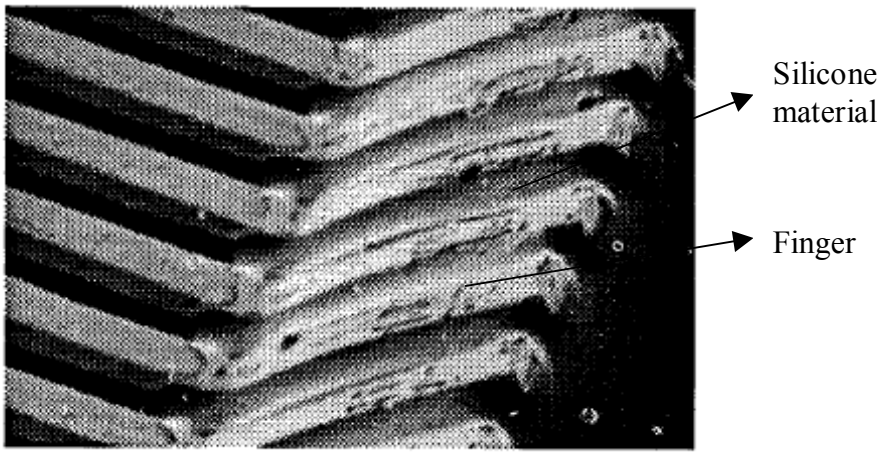


Fig. 2. 4 The Bent Leads with Backfilled Silicone Material (Salatino et al., 1994)

All these membrane probe technologies have to deal with the thermal mismatch between the membrane and the silicon chip. The membrane probe cards may have a thermal expansion coefficient above 40ppm/℃ (vs. 3ppm/℃ for silicon), from room temperature 25℃ to burn-in temperature of 150℃. This implies a differential dimensional change about 1mm over a 200mm wafer. This is almost two orders of magnitude higher than what is acceptable. A technology using the contactor controlled thermal expansion is reported by a Japanese corporation (Nakata et al., 1997). In their report, a polyimide membrane with nickel bumps is used. The membrane is fixed on a ring of ceramic which has a thermal expansion coefficient similar to the silicon substrate. In order to hold the contactor onto the wafer, a method of parallel pressing utilizing atmosphere pressure between the contactor and the wafer tray by decompressing the internal space has been developed. Localized pressure-sensitive conductive rubber is used to establish interconnect between the bumps on the polyimide membrane and the wiring substrate. It also serves to absorb the deviations of bump heights and wafer warpage. This method leads to a reliable wafer-level burn-in

(WLBI), but it involves specific tools design and vacuum equipment and so on, which results in cost increase. Fig. 2.5 and Fig. 2.6 schematically show the contactor structure and the wafer tray.

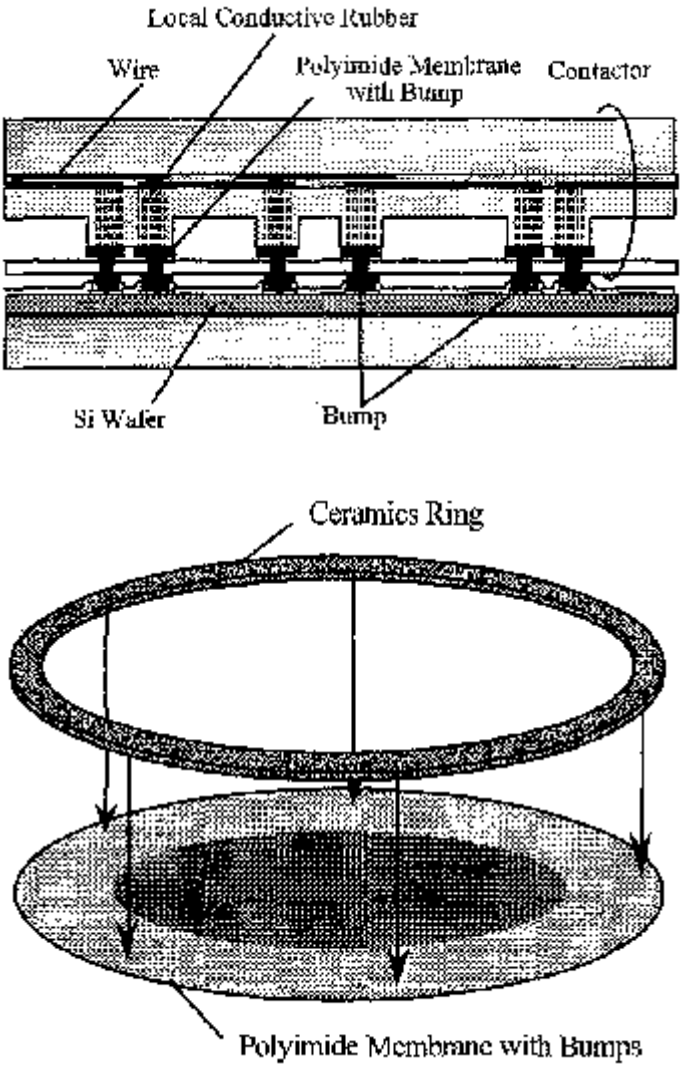


Fig. 2. 5 **Contactor Structure** (Nakata et al., 1997)

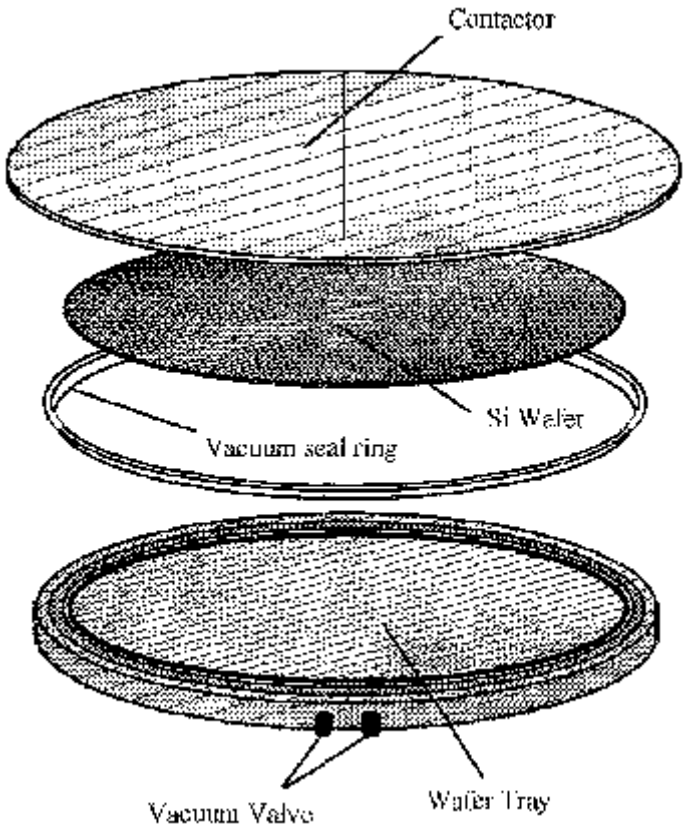


Fig. 2. 6 **Wafer Tray** (Nakata et al., 1997)

As discussed above, membrane probes have many advantages over epoxy ring probes, but they also have drawbacks. They do not produce scrubbing action required for low resistance and need additional force delivery mechanism or air pressure to provide the force needed for giving sufficient and uniform contacts. The contacts are not independently compliant. Because the membrane is so thin and flexible, it would be very difficult to make wafer-sized probes. The problem of thermal mismatch also cannot be neglected when using membrane probes for burn-in (Hirano et al., 1994). For this reason, other materials are proposed to be incorporated in the test carrier, such as ceramic material and silicon itself.

2.2.3 Silicon Based Probe Card

In parallel with membrane cards, there are also some other probe cards, which do not use those materials which have high thermal expansion coefficients, such as polyimide and rubber. The best material to avoid thermal mismatch is the same material as the die, so naturally silicon has been chosen to be incorporated into the probe cards. In 1994, David B. Tuckerman, Bruce Jarvis, Chang-Ming Lin, Pradip Patel and Michael Hunt from nCHIP, Inc. brought up a wafer-level burn-in probe card which employ this strategy, the probe card is shown in Fig. 2.7. (Tuckerman et al., 1994).

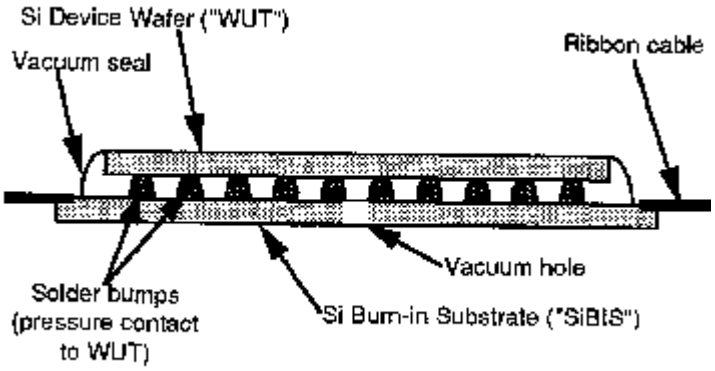


Fig. 2. 7 WLBI Concept (Tuckerman et al., 1994)

The Silicon Burn-in Substrate (SiBIS) is fabricated using nCHIP SiO_2-based multilayer thin-film MCM-D technology, augmented with an internal layer of integral thin-film resistors and a top layer of solder bumps. The SiBIS face is designed with the solder bumps laid out in an exact mirror image pattern to the bond pads on the wafer under test (WUT). The silicon-to-silicon wafer contact is established through a face-to-face pressure based on deformable solder bumps which are functional in a high temperature burn-in environment. The SiBIS is immune to the thermal expansion

mismatch problem which is one of the major risks of wafer level probing. The probe card is reusable and does not damage or contaminate bond pads. The method is suitable for high-volume production and can reduce test and burn-in costs. In this technology, bump uniformity is a key parameter for reducing the contact force which might damage the die when the force applied is too big. Another disadvantage is that the solder bumps need reflow after each burn-in, and the reflow methods need specialized equipment at the site of the burn-in operation. It is a perceived cost disadvantage.

In 1995, IBM Research, Tokyo Research Laboratory also produced another Silicon Microprobing Array for test and burn-in. It is made by micromachining method on a silicon substrate, as shown in Fig.2.8. The contact is made by metal bump. The polyimide layer is used to give z-compliancy. The thickness decides the compliancy. This method is low temperature processing (for polyimide baking at 350° C). It is very important for integration with electrical circuits, which could be damaged by high temperature. This method potentially can be used to wafer level burn-in, but the interconnect is still planar, which restricts the contact I/O counts.

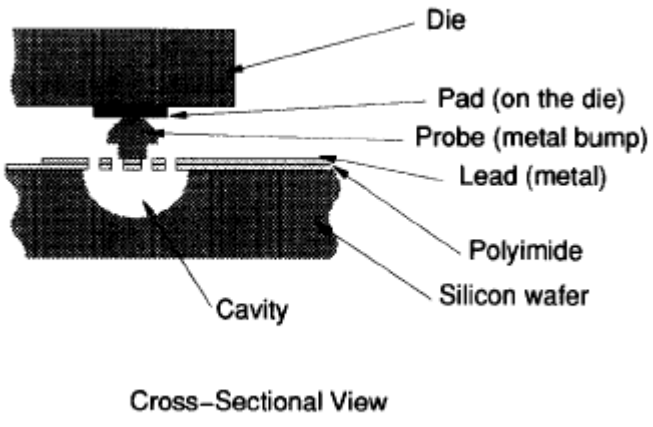


Fig. 2. 8 Silicon Microprobing Array (IBM, 1995)

Some other research groups also reported several silicon based probe cards (Zimmermann, 1995; Matsuo et al., 2000; Kim et al., 2002) which more or less solved some of the associated problems.

2.2.4 MicroSpring Contacts

Various cantilevered beam structures have been reported since 1989 (Hong et al., 1989,1991; Tada et al., 1990), but the impedance of the long cantilevered wires is high and this always provides unacceptably low bandwidth. It has difficulties keeping up with new trends in the chip industry. In 1997, FormFactor introduced the industry's first integrated wafer-level back-end process. They produced a WOW (Wafer on Wafer) process for the wafer-level burn-in test. The concept is the same as the above mentioned temporary carrier technology, but the outstanding feature is their MicroSpring Contact Technology, which involves fabricating MicroSpring^{TM} contacts directly on the wafer. The MicroSpring contacts are the compliant interface to the wafer-level contactors used in burn-in or test. They also serve as the first level interconnection, either soldering or socketing the die to other substrates. The MicroSpring contacts are true springs (Fig.2.9), providing the benefits of linear force versus compression and maintenance of true shape and position over a known range of compression. The MicroSpring can fulfill 100% pin contact on the wafer level. The finest pitch FormFactor has achieved to date is 175μm.

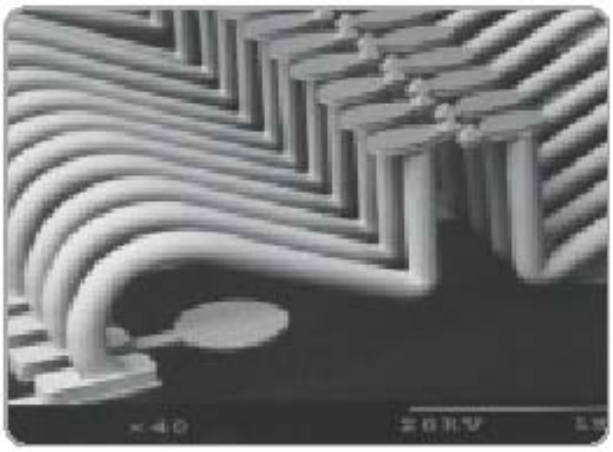


Fig. 2. 9 FormFactor's MicroSpring Contacts

CHAPTER 3: Interposer Design and Fabrication

3.1 The Interposer Concept

Test at wafer-level is still in its infant stage. The lag of development of the test and burn-in methods compared to the highly developed packaging technology has become a bottle-neck for the packaging industry. A novel test system has been proposed to provide the test and burn-in for nano wafer level packaging (NWLP) in this project. As can be seen in Fig. 3.1. (Keezer et al., 2002), the system comprises two parts. One part is the test support processor (TSP), which will be developed at Georgia Tech; the other part is the interposer, which is the subject of this thesis.

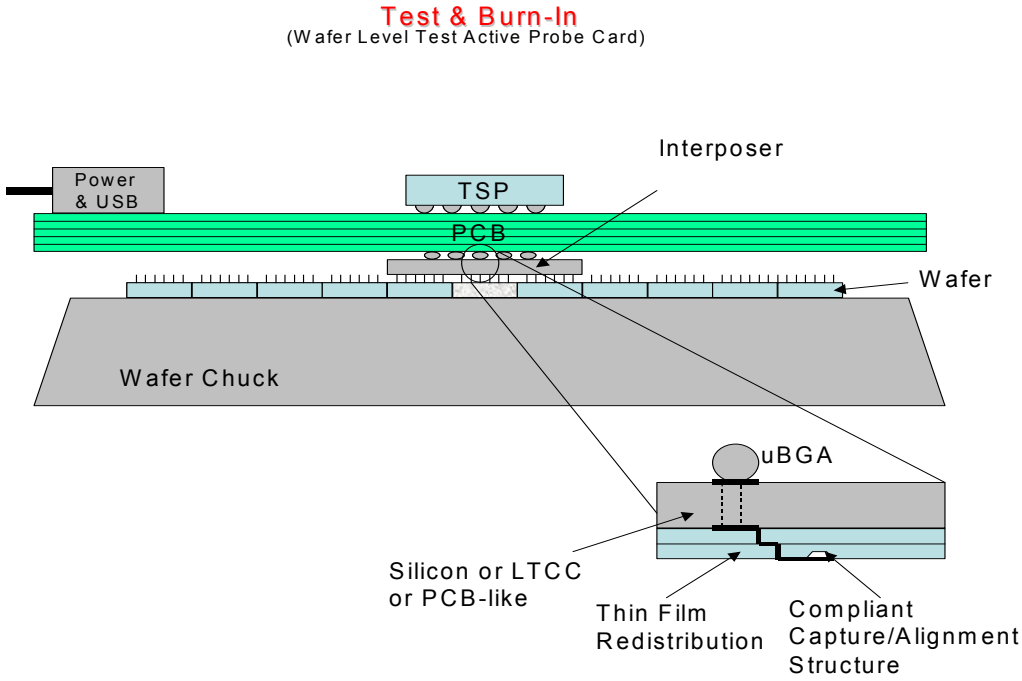


Fig. 3. 1 Active Probe Card for Nano Wafer-Level Package Device

The test support processor (TSP) board consisting of a field-programmable array device, memory devices, sample-and hold devices, clocks, multiplexers, and

others, will be integrated onto the top layer of the interposer using the flip chip attachment method. The TSP will act as the tester with the required test stimuli and memory to capture the tested data.

The interposer is similar to a conventional probe, but with vertically connected signal traces. With self-aligned, z-axis compliant and good electrical contact features, it serves as the electrical and mechanical interface between the NWLP wafer and the tester. One side of the interposer will have large pitch metal bump pads to connect the tester while another side will have fine pitch compliant structures to capture the pins on the NWLP wafers. When connecting, the interposer will be mechanically aligned to the pads of the NWLP wafers and to provide a temporary pressure contact for each electrical signal, including power and ground pins. Within the interposer, the signals are distributed and fanned-out to a large area array on the scale of a micro BGA. Due to the large number of inputs/outputs on this NWLP wafers (in the order of 10,000 to 200,000 I/Os per cm^2), it is anticipated that this interposer will need to have many layers of metal to fulfill the redistribution task. The interposer is CTE (coefficient of thermal expansion) matched to that of the silicon wafer and is mounted onto a conventional multilayer PCB, which further distributes the signals to pins or connectors that mate the TSP. With the repeat of the TSP on a two-dimensional array, a parallel of the test tasks can be simultaneously conducted. It dramatically increases the test throughput and reduces the test cost.

3.2 Layout Design

3.2.1 Design Consideration and Material Choices

To produce an effective methodology of wafer level burn-in test (WLBI), the following factors must be taken into account: alignment, contact area, normal force,

differential expansion, coplanarity, oxidation, solid-state diffusion, etc. (Lau, 1995). The challenges lie in managing mechanical, electrical and thermal problems with a much larger number of contacts and much greater heat flux.

The interposer layout design basically is to design masks for the interposer fabrication using Cadence^{TM}. When designing these masks, we must bear in mind how the process flow would be, which type of materials we will use, how to align different layers, the mask will be dark field or bright field, and what functions every pattern has, and so on. There are some trade-offs in the design consideration. In order to optimize the design, simulation or some trial and error methods must be performed.

Material choices also play a very important role in the design and fabrication because materials properties determine the device performance and the process integration method. In our interposer fabrication, there are not many choices because of the fabrication capability restriction in IME. As we have discussed earlier in this thesis, silicon-to-silicon connection is the best approach for solving the thermal mismatch problem. Other materials such as polyimide, silicone, rubber etc. all have comparatively larger thermal expansion coefficients which will bring about misalignment when used in test and burn-in. Our interposer will be based on silicon wafer. The other advantage for using silicon wafer as our beginning material is the process compatibility with CMOS technology. The interposer can be fabricated easily by mature silicon processing technology with low cost. In our experiment, the silicon-based interposer is designed to meet the requirement of fan out the 100μm pitch I/Os to about 750μm pitch which is compatible with the traditional PCB processing technology. In order to fulfill the task of routing out the large I/Os and obtain controlled impedance transmission line from tester to chip, this silicon-based interposer is designed to have three build-up metal layers on top of a silicon substrate,

in turn named power plane, ground plane and compliant structure. For the power and ground layer, we use aluminum; which has mature CMOS processing technology. It is commonly deposited by evaporation or sputtering. The power plane and the ground plane are two global metal layers on which via holes are made to let the signal traces pass by. A schematic drawing of the cross-section of the silicon-based interposer is shown in Fig. 3.2.

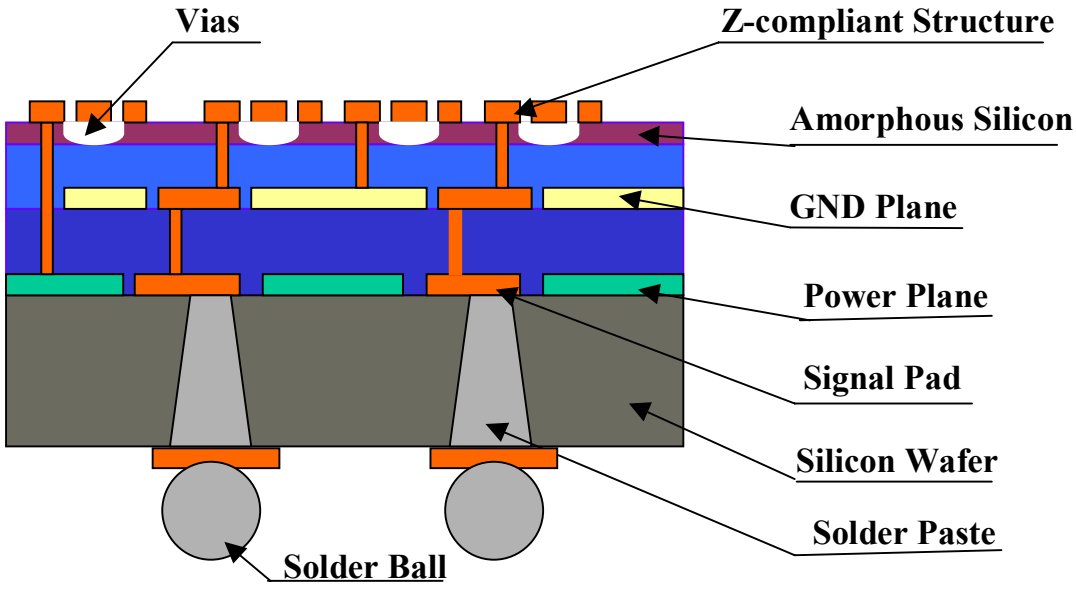


Fig. 3. 2 Interposer Cross-Section

The compliant structure is essential in this interposer fabrication. It has small feature size, as it will match the 100um pitch chips. It is also desired to have X, Y, and Z-axis compliance to facilitate its connections to the I/Os of the NWLP chips. In this way the stress induced by the interconnects would be reduced dramatically. In order to meet the fine pitch requirement within the process capability, several different structures were tried. The compliant structures do not give the contact scrubbing action, so a large force will be needed to obtain low contact resistance. In order to obtain a better contact and avoid copper oxidation, gold was chosen for the contact pad and

routine traces in the experiment. Gold also has good mechanical properties. It can give a larger compliance than copper.

As for inter metallic dielectric layers, conventional CMOS materials such as SiO_2 and SiN_3 were chosen. They also serve as etching masks or stop layers when needed during the fabrication.

A lot of other chemicals also have been used during the interposer fabrication for their unique properties. Potassium iodide (KI) was used to etch the gold seed layer. This solution has large etch selectivity between gold and copper. Aqua Regia, which is a mixture of HCl, HNO_3, and H_2O (200:600:800 by volume), can also be used to etch gold. The silicon dioxide can be etched by buffered oxide etch (BOE).

3.2.2 Layout of the Silicon Interposer

Due to process compatibility at IME, in this study, we are not able to fabricate an interposer with 2256 or more I/Os, which future ICs may require. Instead, we designed a test vehicle with only 120 I/Os to demonstrate the process feasibility and the interposer concept. Cadence was used for drawing the photomasks required for the fabrication of the interposer. The whole design is shown in Fig. 3.3.

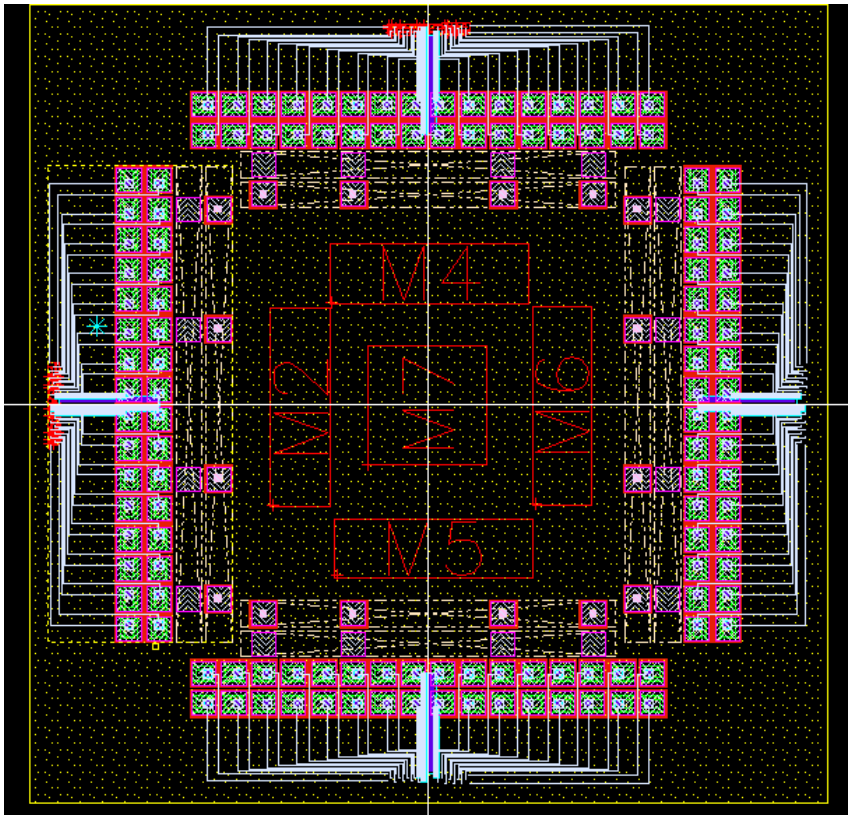


Fig. 3. 3 The Interposer Mask Design

The first metal layer photomask (just on top of the silicon wafer) for the interposer is shown in Fig. 3.4. It has 32 I/Os with 100μm pitches on each side, which will be fanned out through three metal layers to 750μm pitch I/O pads on the backside. It consists of a metal plane (power plane) on which some isolated metal pads are produced by etching away their peripheral area. The black part is metal while the red squares will be etched away. Inside these squares are the signal pads, which connect the other side signal pads through wafer vias. The second metal layer is shown in Fig. 3.5. It is similar to the first layer except that it is designated as a ground plane. The third metal layer is shown in Fig. 3.6 and is the most complicated layer. It includes the fan out traces and the compliant structure. The compliant structure has several different configurations as will be shown later in Chapter 4. Fig. 3.7 shows some different enlarged views of the compliant structures. The compliant structure normally includes

a fixed frame and one or more cantilever beams which support a small capture pad. When the pad contacts the pins of the tested wafer, the cantilever beams will give it z-axis compliance, which is most important in establishing contact over the full wafer.

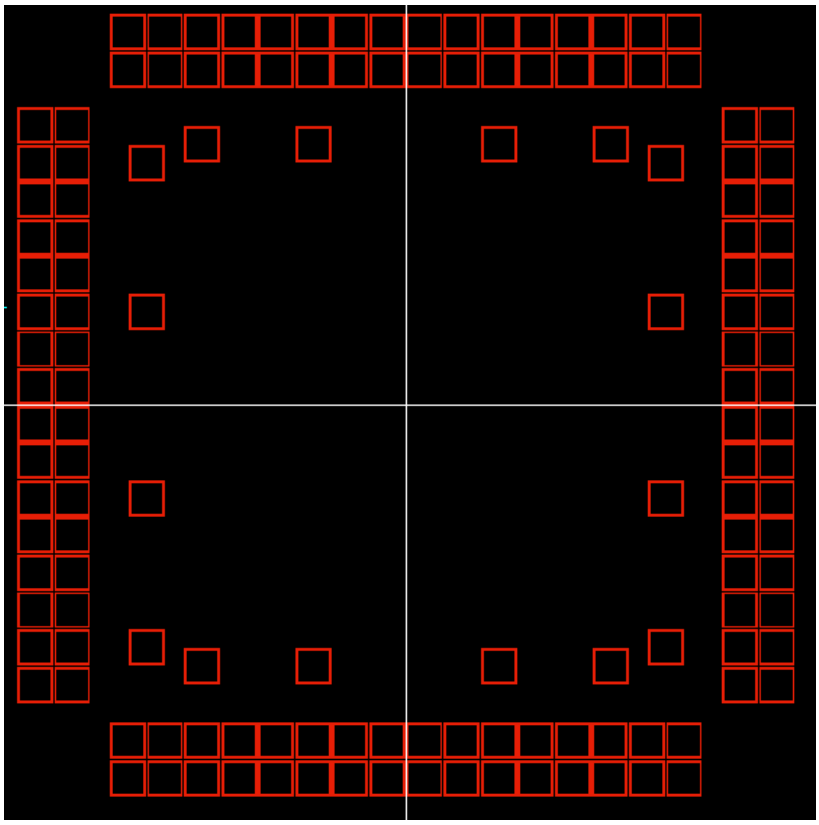


Fig. 3. 4 First Metal layer (Power Plane)

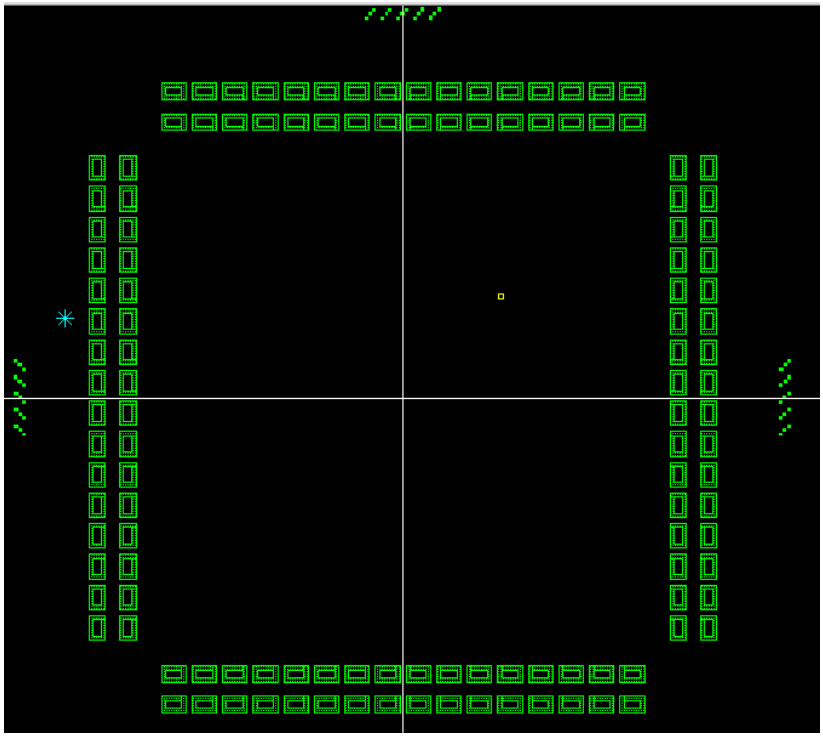


Fig. 3. 5 Second Metal layer (Ground Plane)

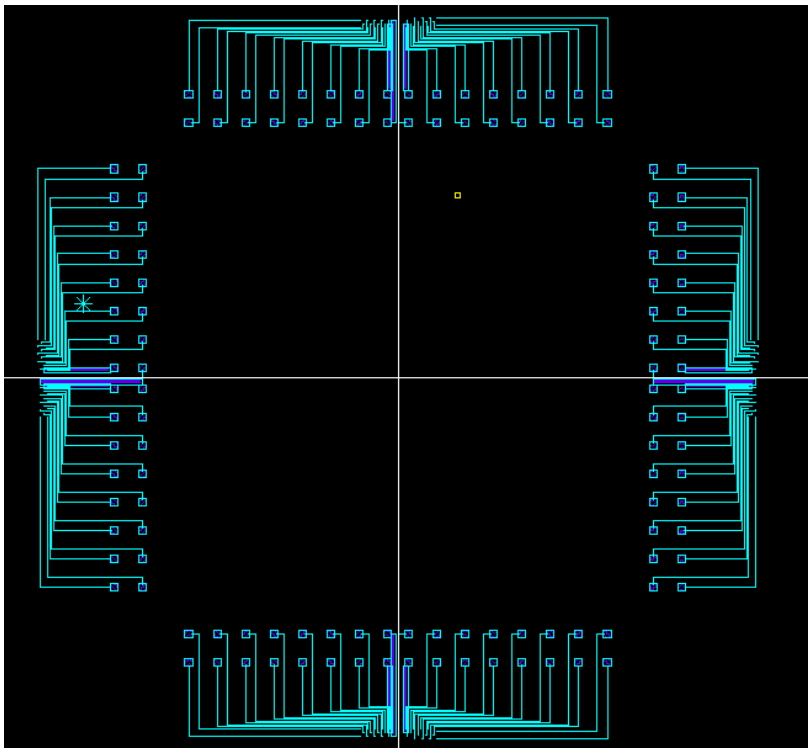


Fig. 3. 6 Third Metal layer (Compliant Capturing Pads and Traces)

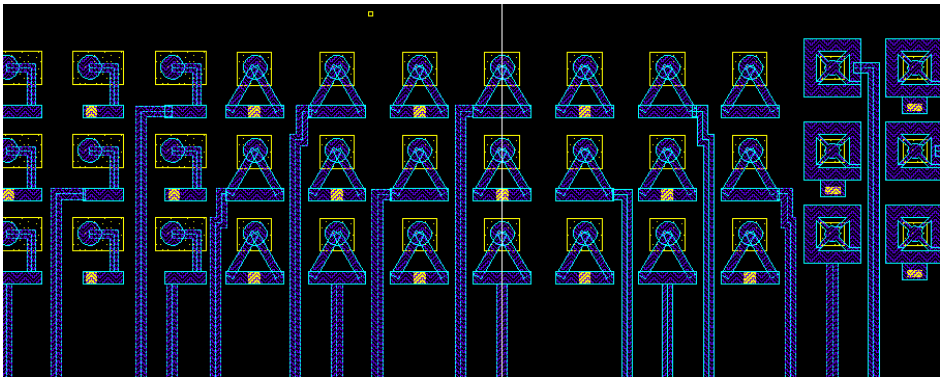


Fig. 3. 7 Enlarged Compliant Structure and Below Layers

3.2.3 Potential Problems

Because of the fine pitch of the pins, there are some potential problems in the design. Due to the close proximity of the interconnects, there could be a potential parasitic crosstalk that may impede high frequency applications. As for the compliant structures, over etching or incomplete etching will affect its performance. This will cause the final device to fail with an insufficient z-compliance. The z-compliance is highly dependent on the thickness of the sacrificial layer thickness and the pitch of the pads. In our process, the sacrificial layer was chosen to be amorphous silicon, but the thickness of the amorphous silicon layer that can be grown was only two microns. As such the vertical compliance was restricted to be less than this thickness. If we are going to try some other materials such as polyimide or BCB, we will have to use a chemical-mechanical-polishing (CMP) machine to complete the process. Even though this process is workable in theory, we could not try it out completely since a CMP machine is not available, we only experimented some individual steps.

3.3 Interposer Fabrication

After the masks fabrication, we began to fabricate the interposer on prime silicon wafers using a micromachining method, which includes lithography, via

formation, PECVD, electroplating and so on. The process parameters can be optimized based on the simulation and the summary of the finished processes.

3.3.1 Process Flow

The substrate fabrication began with a standard 6-inch wafer. Silicon was selected for its low cost, low thermal expansion coefficient, high thermal conductivity, and compatibility with IC manufacturing equipment. We had also thought of using PCB as substrate, but its thermal expansion coefficient is too high, at a burn-in temperature of 150^{o} C, the mismatch between the PCB and the silicon chip will be so large that the pins may not properly contact the pads.

Based on the process compatibility at IME and the functional requirements of the interposer, several different processes were developed; each has its own advantages and limitations.

The first process flow:

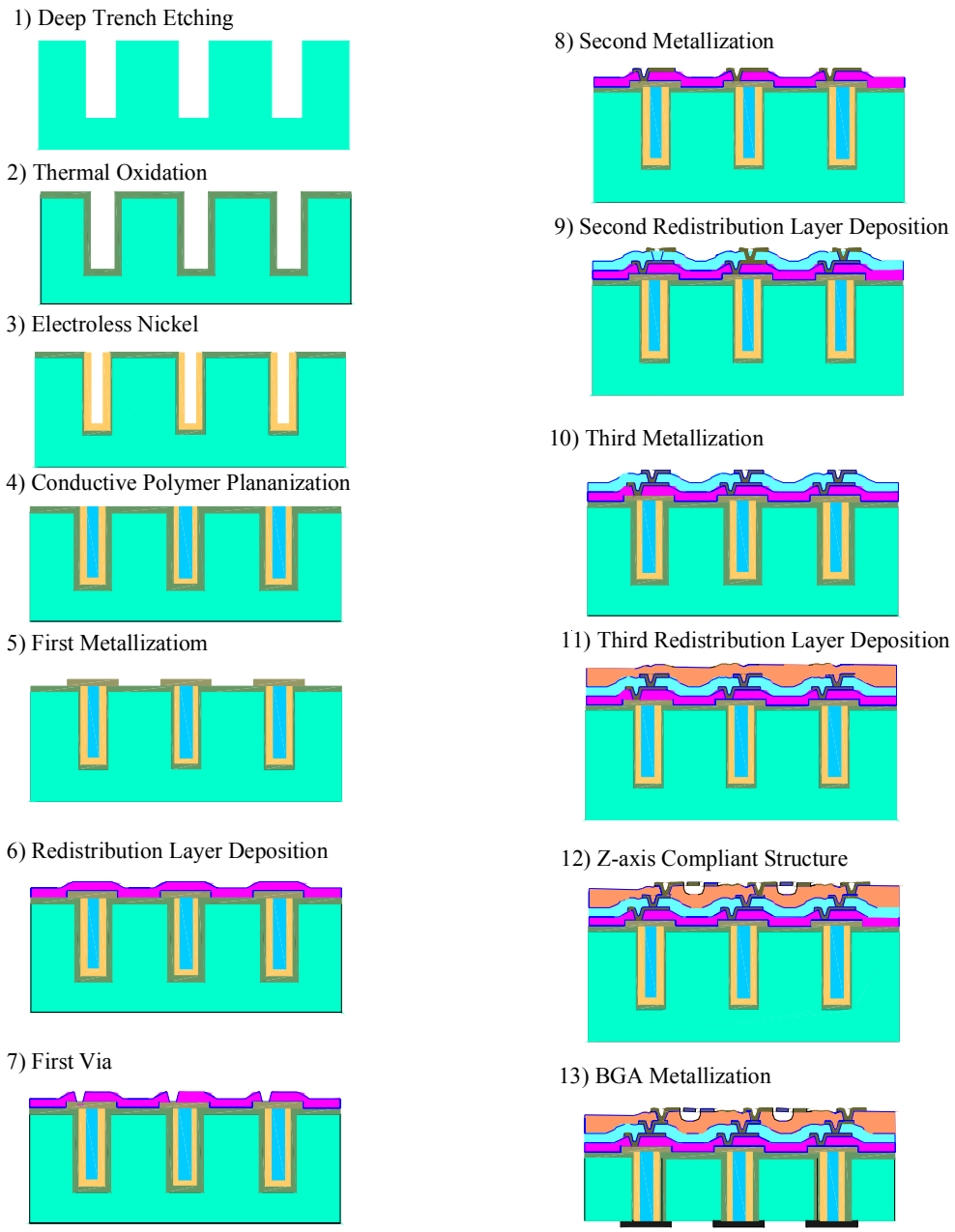


Fig. 3. 8 Interposer Process Flow (1)

The main feature of the process shown in Fig. 3.8 is the through-wafer via for the front-to-back interconnection. The difficulties of this process are as follows:

1. Planarization problems:
    a. The wafer needs to be thinned on the back side using CMP technology. Due to the lack of this facility at IME, no wafer was thinned.
    b. When the layers on top of the wafer are built up, there was a severe planarization problem. Because of the uneven surface, the upper layers cannot be processed properly.
2. Vias metallization problems:
    a. Because of the high aspect ratio of the STS etched vias, it is difficult to sputter seed layer metals (Ti and Au) on the trench wall.
    b. Before the backside CMP, the vias are blind vias. When we tried to fill in metal or conductive materials inside the vias, there is vacuum formed inside the vias. This makes the metal filling process difficult. In reality, we may not completely fill in the vias. There may be voids inside the vias, even though a vacuum chamber was used.
3. Handling Problems

    Since the vias formation step is before the other build-up processes, wafer handling becomes a big problem. The tiny pitch holes are populated on the entire wafer, which makes the wafer extremely fragile and easily broken. A very small stress will damage the wafer and all the efforts made before will become futile. In order to minimize this problem, we move the via formation step to a little later in other processes described later.

The second process flow:

Since the first process has some unresolved problems, we revised the process flow and tried another more applicable method as shown in Fig. 3.9. In this process, the vias formation process is performed after completing the front side processes. Though the wafers are not as fragile, this approach gave rise to other problems in handling the wafers. However, when we do the backside processes, we will have to protect the tiny compliant structures on the front side. We should be very careful but it is difficult to avoid damaging those structures. In order to protect our compliant structures, we release the compliant structures at the end of the third process flow.

In this second process, we obtained the through-wafer vias using a potassium hydroxide (KOH) etch. This process gave us sloped wall vias in a (100) silicon wafer, as can be seen in Fig. 3.10. The slope of the wall is 54.74^{o}, which is crystallographic angle between the {111} plane to the {100} plane of the silicon. The {111} plane has the highest atoms density and the silicon atoms are oriented such that three bonds are below the plane, the plane separation is smallest (3.135A). As such, the {1 1 1} plane is etched much slower than {1 0 0} plane. This characteristic of the {1 1 1} plane is utilized to create the V-shaped groove. The slope is beneficial for our later metal seed layer sputtering and conductive materials filling-in processes.

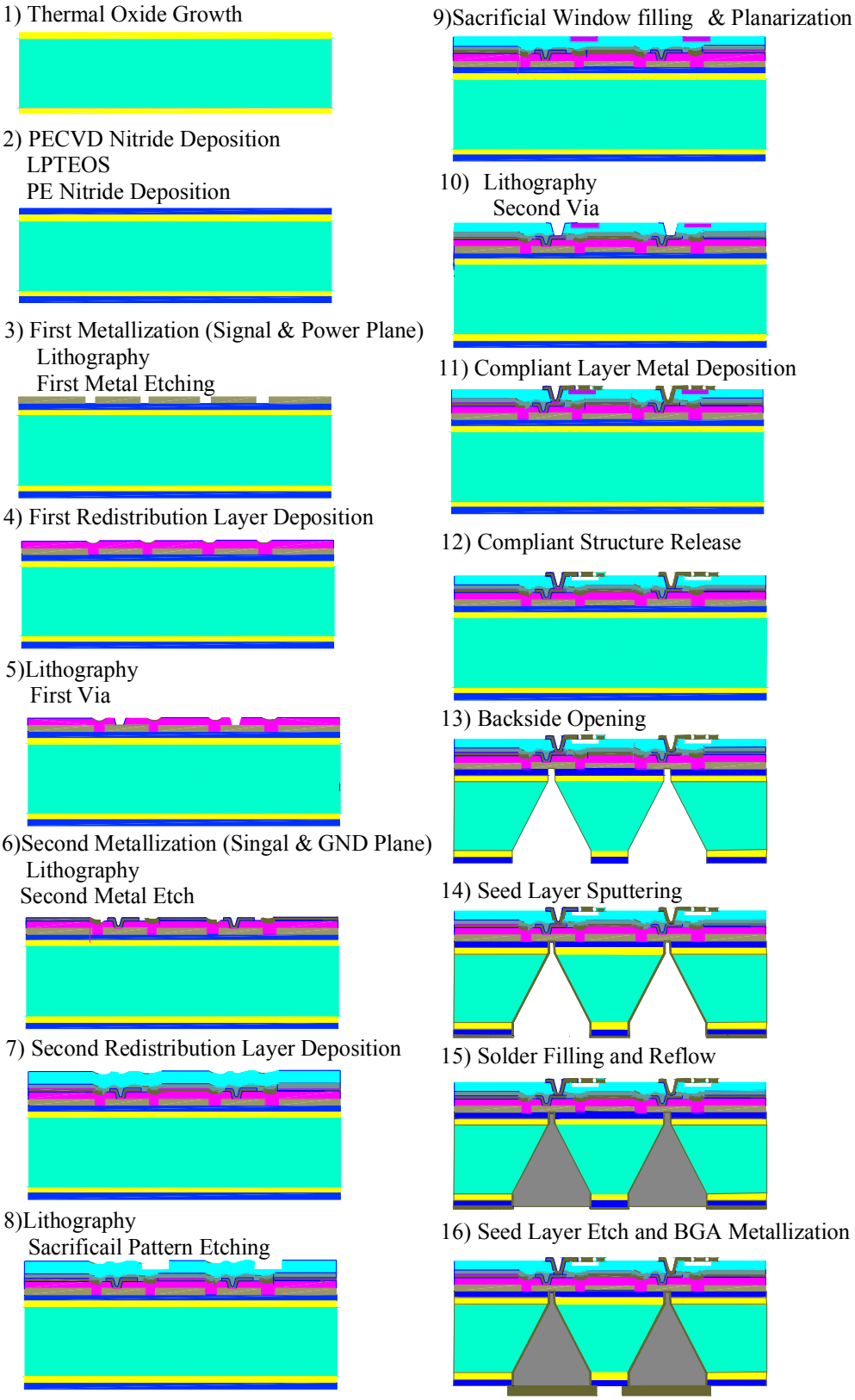


Fig. 3. 9 Interposer Process Flow (2)

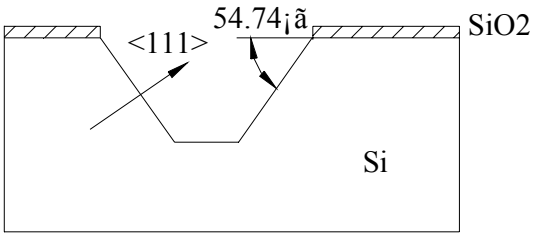


Fig. 3. 10 KOH Etched Profile

The third process flow:

The third process flow was based on the availability of processing tools and facilities at IME. The detail process steps are described in the following table and the process flow is summarized in Fig. 3.11.

Step	Process Description	Remarks
1.	Lot Start	
2.	Wafer Marking	
3.	Thermal Oxide Growth_300 A	
4.	Nitride Deposition_1500 A	
5.	Oxide TEOS LPCVD_2500 A	
6.	PECVD Nitride Deposition (BACKSIDE!!) 1KNIT	
7.	PVD Metal (Power Plane)	8000A Al with Ti/TiN underneath.
8.	Mask-1 Power Metal	
9.	Metal (8000A Al/TiN/Ti) etch and PRS	
10.	IMD deposition	
11.	Mask-2 Viak	
12.	Via etch stop on Al	
13.	PVD Metal	

14.	Mask-3 Ground Metal	
15.	Metal (8000A Al/TiN/Ti) etch and PRS-metal	
16.	PECVD TEOS Deposition (1um)	
17.	a-Si deposition, 2um deposition	
18.	Mask 4 – Via mask	
19.	Via etch (2um-a-Si and 1um PETEOS etch)	Stop on Al
20.	YES striper to strip Photo resist	
21.	Resist Strip	
22.	PVD Ti/Au seed layer deposition KDF	Ti: 500A Au: 300A
23.	Mask 5 – For electroplating of signal traces and compliant structures	
24.	Descum 1 min	
25.	Au or Cu plating (2-3um)	
26.	Resist Strip	
27.	Seed layer etch Au (Wet or dry etch)	
28.	Seed layer etch Ti	
29.	PECVD, sensor P5000, TEOS deposition Thickness 5000A	Protection
	Back Side	
30.	PETEOS deposition Thickness: 2um	
31.	Mask 6 – Backside Opening	
32.	Etch 2um PETEOS + 1000A PENit +2500A Oxide + 1500A Nit	
33.	Photoresist Strip	
34.	TMAH Etch (By time) 400um – 450um	
35.	STS etch	
36.	Backside Nitride/Oxide stack Etch	
37.	PVD Ti/Au Deposition KDF (seed layer)	
38.	Photoresist coating for plating (Paper mask)	

39.	Au or Cu Plating 2-3um	
40.	Resist Strip	
41.	Mask 7 – Metal Strip (BF)	
42.	Wet Gold seed layer Etch Aqua Regia	
43.	Wet Cr etch and Resist strip	
44.	Resist Strip on backside	
45.	Backside Via Filling (use solder ball)	
	Front side	
46.	Mask 8 – release opening	
47.	Etch 5000A PETEOS	
48.	Resist Strip	
49.	Front-side a-Si release etch Sensor STS, XeF2 release etch	

First, a thermal oxide layer thickness of 300 angstrom was grown on top of the silicon substrate to act as an insulation layer; then 1500 angstrom of silicon nitride layer was deposited on top of this silicon dioxide layer. This silicon nitride layer acts as a stop layer for the etching through-wafer vias. In order to protect this stop layer from scratches damage during wafer handling, a 2500-angstrom layer of LPCVD TEOS was deposited on top of the silicon nitride layer. On the backside of the substrate, a layer of silicon nitride was grown using PECVD. After these steps, the first metal layer was deposited and etched. This gave us the power plane and the isolated metal pads. On top of this metal layer, we deposited an interlayer dielectric with exposed vias to connect the metal pads. Then, the second metal layer for the ground plane was deposited. Isolated pads that allow signal traces to be connected to the upper compliant structure were etched. On top of this layer, another layer of interlayer dielectric was deposited on which we etched the second vias to expose the metal pads

of the ground plane. Then we went on depositing the seed layer of the compliant structure metal, and another layer of PECVD TEOS. This oxide layer acts as the stop layer for compliant structure to be released later. On this oxide layer, a 2μm amorphous silicon layer that served as the released-layer for the compliant structures was deposited. After this, through-wafer vias that connect to the front side isolated metal pads of the power plane were etched. After completing the through-wafer vias etch, a layer of oxide was grown and etched away the parts that contact the front metal pads. In this way, the walls of the through- wafer vias were insulated to reduce leakage current. These through-wafer vias were filled with conductive materials to connect them to the signal pads of the test processor. Several different conductive materials were used to fill the vias, but no satisfactory results were achieved. After this step, a layer of metal was deposited and etched and the peripheral parts were etched away to obtain the metal pads covering over the vias. These metal pads would be connected to a printed circuit board-based interposer with solder balls or other interconnects methods such as bed of nails.

This process tuned out to be successful. If we have CMP machine, we can improve it a lot, as we can change the support layer to be BCB, and also we can do CMP after the backside via filling. and so on.

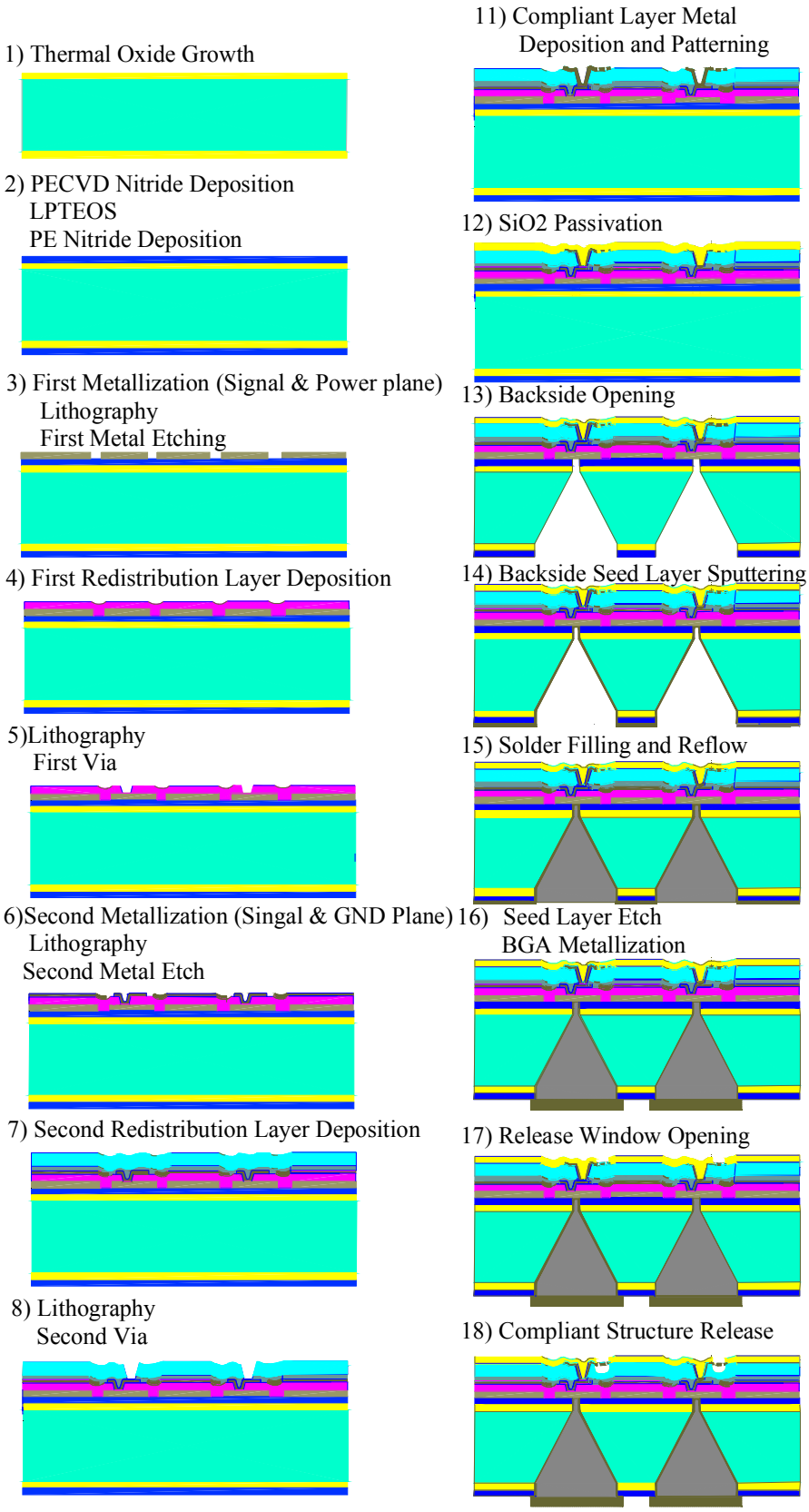


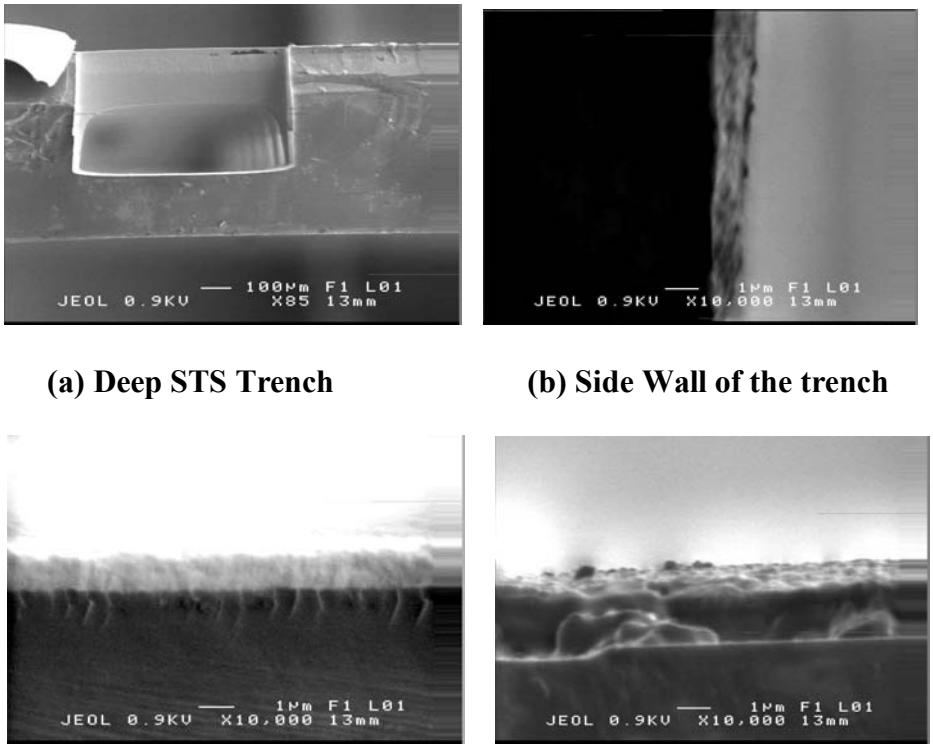
Fig. 3. 11 Interposer Process Flow (3)

3.3.2 Key Processes

3.3.2.1 Through Via Formation:

Aerial array packaging yields the highest number of I/Os on a chip. To connect the aerial I/Os, through-wafer vias are needed for our interposer. These through-wafer vias are used to connect both sides of the metal pads on the silicon substrate. As such, the formation of these through-wafer vias is an important process in the processing of our interposers. Both dry etch and wet etch techniques were explored in this project.

Dry etch makes use of highly energetic particles are generated in the plasma to strike the silicon substrate at high speed. The unprotected or unmasked parts on the silicon wafers will be etched away while the protected parts will remain there. Since the incident particles are accelerated by the electric field, their path is directional, nearly vertical to the substrate. As such, the etched profile is anisotropic and the etched vias will have nearly straight walls, as can be seen in Fig. 3.12. It shows images taken for a deep trench which was etched in an STS trench etcher. A seed layer of Ti and Au was then deposited, followed by gold evaporation.



(a) Deep STS Trench **(b) Side Wall of the trench**

(c) Bottom of the trench **(d) Top of the Trench**

Fig. 3. 12 SEM Photos for STS Etched Deep Trench

The wet etch process is a special type of chemical reaction. The selectivity is high between mask material (mainly the photoresist, silicon oxide and silicon nitride) and the etched material (silicon substrate, dielectric), but the etched profile is isotropic. The chemical will etch both laterally and vertically. The etch speed depends on the crystal structure and orientation. Our KOH etched vias have a slope wall which is 57.4 degree to the surface. Fig. 3.13 shows a KOH etched deep trench. Fig. 3.14 shows the same trench filled with solder from the reflow of the solder ball. This trench has a dimension of 700μm by 700μm. The depth of the trench is 400μm. So at the bottom of the trench, the size of the square is about 135μm by 135μm. The trench wall has a slope of 54.74^{o}, which will facilitate the filling of solder paste and other conductive materials.

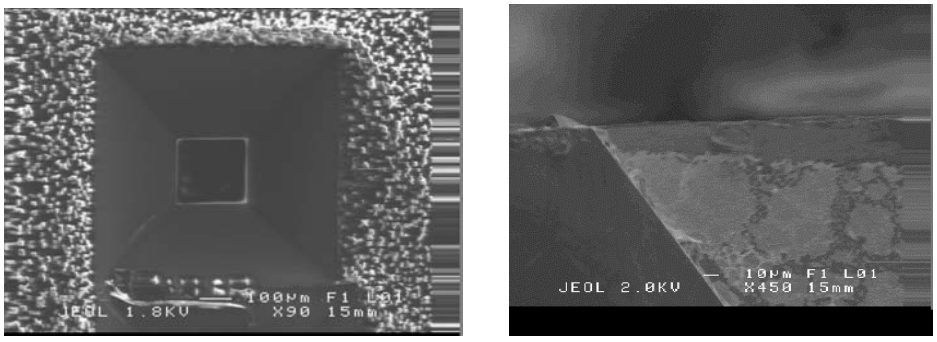


Fig. 3. 13 SEM Photos for KOH Etched Deep Trench

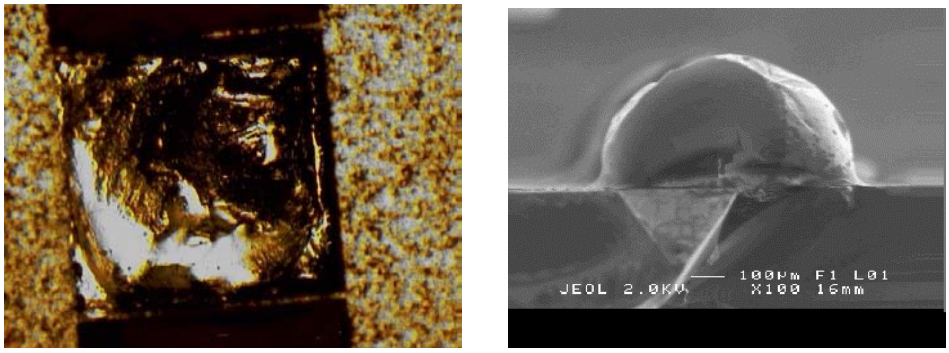


Fig. 3. 14 KOH Etched Deep Trench with Solder Ball Reflow

3.3.2.2 Thin Film Metallization

Thin film metallization techniques are widely used in microelectronic packaging to form interconnection metallization or metal pads and under bump metallization (UBM) for ball-grid array (BGA) packages. Some of these techniques are evaporation, sputtering, electro-plating and electroless plating, among which, plating is the most frequently used technique.

Electroless Plating

Electroless plating is used when there is a need for depositing metals on a nonconductive material. We tried to plate nickel and copper on silicon and silicon oxide surfaces. The procedures of electroplating of nickel are as below:

First, preparation of the plating solution:

a. Prepare a container, mixing 0.02 g $PdCl_2$, 0.20ml 37% HCl and 20 ml H_2O

b. Another container, 0.05 g $SnCl_2$ 0.50ml 37% HCl and 20 ml H_2O

c. Concoct 1% Silane solution in another container

Second, wafer pre-cleaning step: rinse the silicon wafer surface with water, then treat it in ultrasonic bath to get rid of the dirt on the surface; take it out, clean the silicon wafer surface with ethanol, rinse in water, then soak in the condensed sulfuric acid and H_2O_2 mixture for more than one hour.

Plating:

a. Take the wafer out of the sulfuric acid, rinse with ethanol, and put it into the silane solution for one hour.

b. Take the wafer out of the silane solution then put it into an oven, set the temperature to be 120°C, for one hour.

c. Take the wafer out of the oven, soak in the $SnCl_2$ solution for 2 minutes, wash it, and then soak in $PdCl_2$ solution for 10 minutes.

d. Finally put the wafer into the nickel solution, temperature kept at 88°C. Keep churning the solution to ensure the plated film's uniformity.

After 4 to 5 minutes, we take the wafer out to inspect. The film is evenly plated and the adhesion of the film is quite good with no peeling.

For our application, the interconnects should be copper for its low conductivity. The thickness of the copper is determined by the desired electrical performance as well

as its processibility. In our design, the desired copper thickness is 2 microns in order to yield a low-enough resistance for signal transmission in the RF regime. Due to the poor adhesion of copper on silicon, nickel is first electroless plated. The nickel-plated wafer was then etched in HCl solution for 10 seconds before immersed into the copper plating solution. For 3 minutes, only a 0.8μm film was observed. However, the plated film peeled off when the plating time was increased to 4 minutes. A reliable, high quality copper was not obtained after many trials. As such, we adopted the electroplating technique.

Electroplating

Electroplating can be used to deposit high quality conductor films. The weight of electrodeposited materials at the electrode is a function of the current passing through the electrolytes as well as the duration.

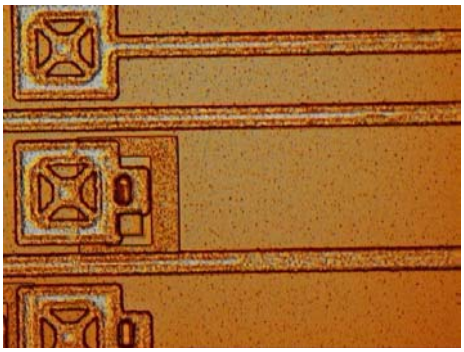
During the fabrication of the interposer, we tried to plate gold and copper under different current and duration to obtain different thickness of the metal traces. Thirteen microns wide traces and twenty by twenty micron pads were electroplated. For different dimensions the electroplating rates are slightly different, this is probably due to the loading-effect.

Table below summarizes the electroplating conditions and results we obtained from the electroplating experiments.

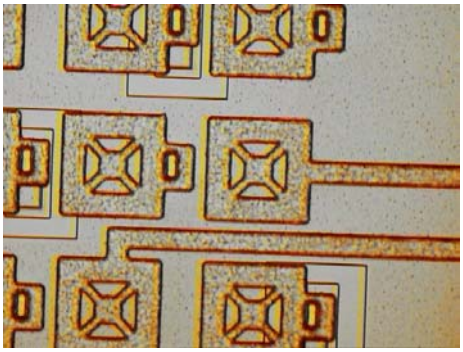
Plated material	Gold	Gold	Copper	Copper
Current (mA)	25	15	80	80
Temperature (^{o}C)	65	65	25	25
Seed layer	Ti: 500A Au: 300A	Ti: 500A Au: 300A	Ti: 500A Au: 300A	Ti: 500A Au: 300A
Duration (min)	12	6	3	2
Thickness (μm)	~3.4 -3.5	~1.5	~4	~2

The results show that gold plating can be performed in 12 minutes using 25mA of current. For copper plating, it requires 3 minutes using a current of 80mA to obtain a 4μm thick trace. These two electroplating processes have moderate speed and good profiles. The uniformity of the plated films is good. A proper control of the plating time allows us to obtain the desired metal thicknesses.

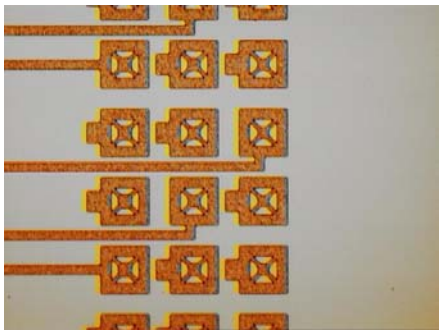
For copper plating, a plating time of less than 2 minutes will not give continuous films, as can be seen in Fig. 3.15 (a). The first picture shows the middle parts of the traces were not fully plated when the plating was performed for 2 minutes. However, a continuous plated copper film was observed as shown in Fig. 3.15 (b) after copper plating for 3 minutes.



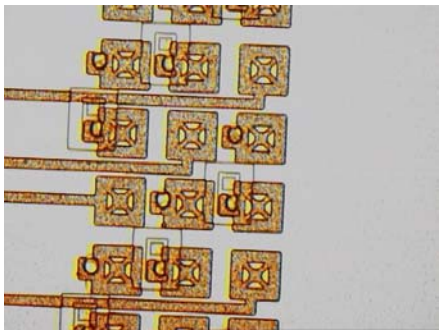
(a) 2 minutes copper plating



(b) 3 minutes copper plating



(c) Plating on Dummy Wafer



(d) Plating on Patterned Wafer

Fig. 3. 15 Plating Copper on Dummy Wafer and Patterned Wafer

Fig. 3.15 (c) shows the plated copper on a smooth surface. However, when there are some steps under the plated area, especially when the feature size is very small, the continuity is not so good, as can be seen in Fig. 3.15 (d). There are some broken parts for the plated film. This is a big problem when the metal pad is used in high-frequency signal transmission. Fig. 3.16 shows enlarged broken parts of the plated areas above a step. When we reduce the step height by reducing the thickness of the underneath metal layers, a much better plated copper film is obtained as can be seen in Fig. 3.17a.

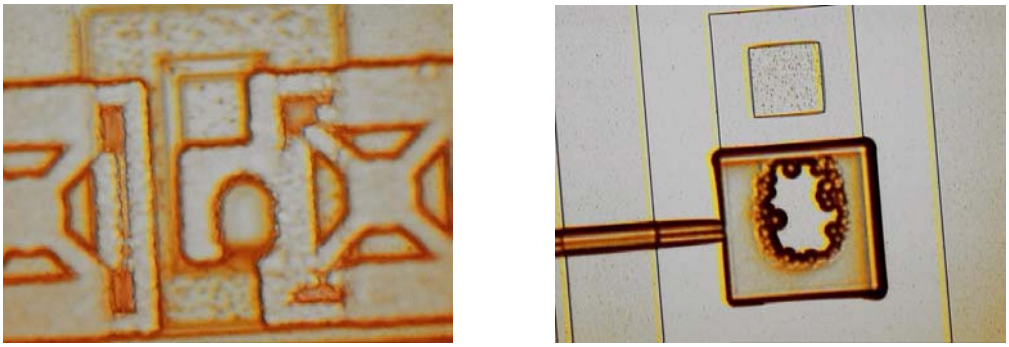
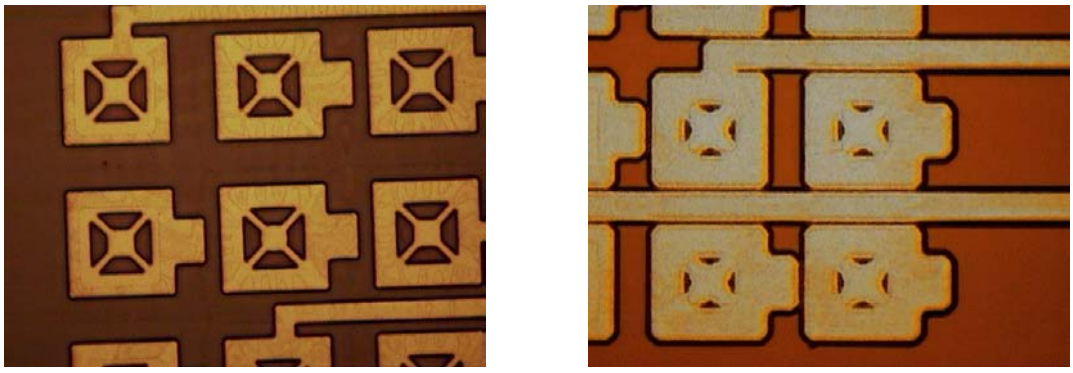


Fig. 3. 16 Plating Discontinuity Caused by Poor Step Coverage and/or Seed Layer Discontinuity

Different photoresist exposure durations have a great effect on defining the small feature sizes of the patterns. As can be seen in Fig. 3.17, photoresist exposure times can result in its inability to resolve the smaller feature size. The photoresist used is 3μm in thickness. Because the compliant structure has an extremely small feature size, for a normal exposure time of 30 seconds, its feature cannot be resolved as shown in Fig. 3.18. Thus, the exposure time of the photoresist must be reduced. After several trials, it was found that 8 seconds exposure time was good enough to define the features in the compliant structures. The traces are well defined as shown in Fig. 3.17 (a).



(a) 8s Exposure Duration (b) 30s Exposure Duration

Fig. 3. 17 Exposure 8 seconds and 30seconds for the PR Patterning

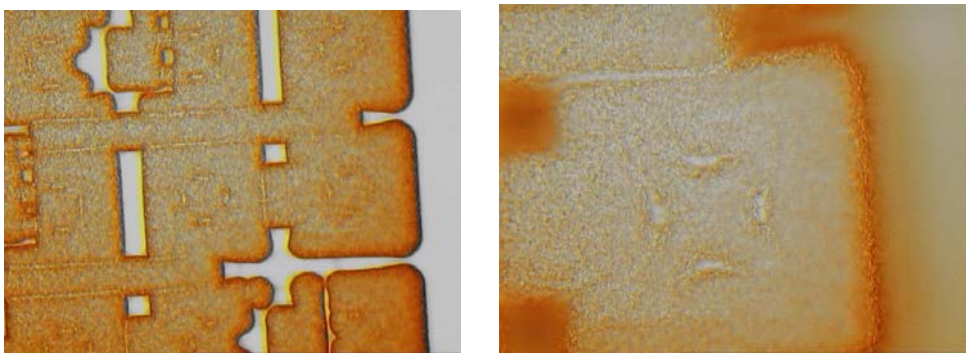


Fig. 3. 18 Enlarged Photos for Exposure 30seconds for the PR Patterning

3.3.2.3 Compliant Structure Release Processes:

Several approaches to release the compliant structure were experimented. Each has its own shortcomings as illustrated below.

The first approach:

Fig. 3.19 shows the process flow for this specific method.

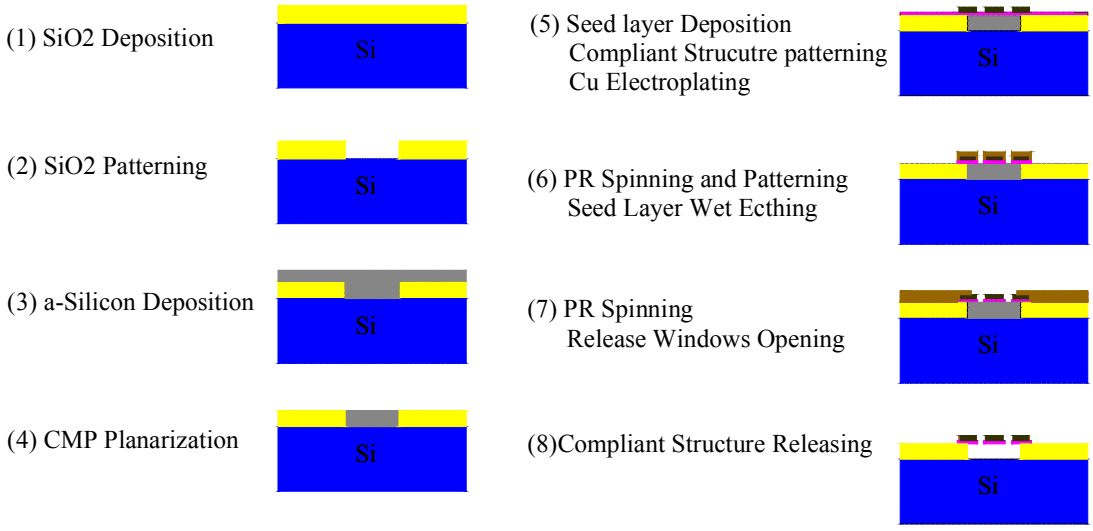


Fig. 3. 19 Compliant Structure Release Process (1)

First a layer of silicon dioxide was grown to serve as the supporting structure. On this layer, some holes were opened at the location where the compliant structure was to be released. A layer of amorphous silicon was deposited on top of this silicon dioxide layer. This serves as the sacrificial layer for the compliant structure. Because of the non-uniformity, we have to polish the surface layer to get rid of the amorphous silicon that covers the oxide layer while keeping the amorphous silicon that is inside the holes. This step is critical in this approach because if a good planarity were not attained, the subsequent processes would have problem in resolving the tiny features in this interposer. Unfortunately a CMP machines was not available for our processing.

As such, we could not polish the top layer to obtain a smooth profile we needed for subsequent processing. Though this approach is sound in theory, we were not able to use it for our interposer fabrication at IME. Another approach has to be proposed.

The second approach:

Fig. 3.20 shows the process flow for the second approach.

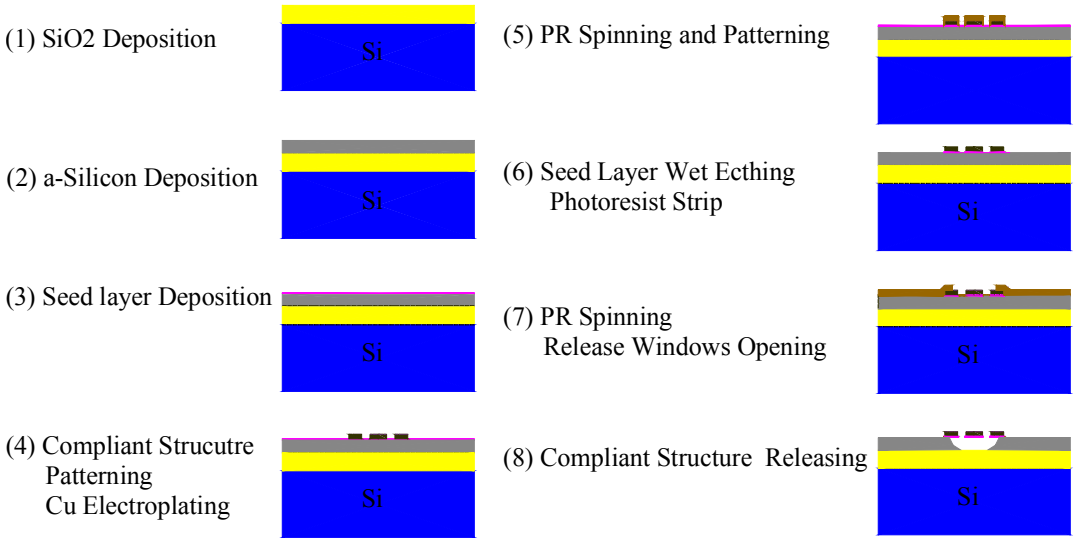


Fig. 3. 20 Compliant Structure Release Process (2)

In this approach, the silicon dioxide does not directly support the compliant structures, but it only serves as a stop layer for the release of the compliant structure. Instead, an amorphous silicon layer on top of the silicon dioxide layer is serving as the direct supporting layer. This amorphous silicon layer also serves as a sacrificial layer under the compliant structure.

First, a layer of silicon dioxide was grown to serve as a stop layer for the release of the compliant structure. Then, a layer of amorphous silicon was deposited, followed by the deposition of the metal layer. After metal deposition, the compliant structure trace was patterned. Then, we deposit photoresist and pattern it to obtain the release windows. Finally, a XeF_2 etch was used to etch the amorphous silicon that was

exposed through the release windows while keeping the copper trace intact. XeF_2 etch was chosen because of its high etching selectivity between amorphous silicon, silicon dioxide, and copper. The etching time should be controlled precisely to assure the full etching of the z direction and proper lateral etching. In this case, the amorphous silicon underneath the compliant structure frame should not be etched away since it supports the frame. In the mean time, the vertical etching should stop at the silicon dioxide layer underneath the amorphous silicon layer. Here the dimension of the compliant structure and the opening mask play important roles in obtaining successful etching profile. In order to obtain a better etching profile, complaint structures and opening masks with different dimensions were experimented.

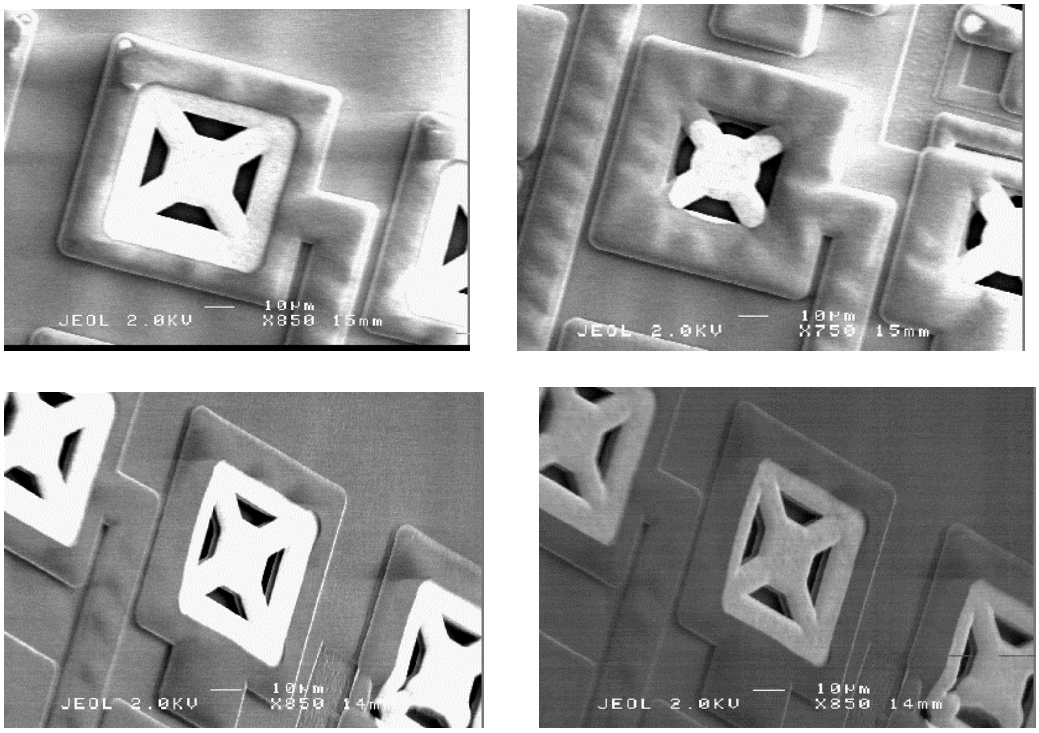


Fig. 3. 21 Amorphous Silicon Released by XeF_2

The released window (the white features) can be clearly seen in Fig. 3.21. The release time is 300 seconds. The amorphous silicon underneath was released as evident

by the hanging of the pad. From these SEM photos, we can also see the topography of the plated trace. These plated metal traces have very large steps. If this step occurs in the previous build-up processes, it will bring problems in later process, especially in fine feature devices fabrication.

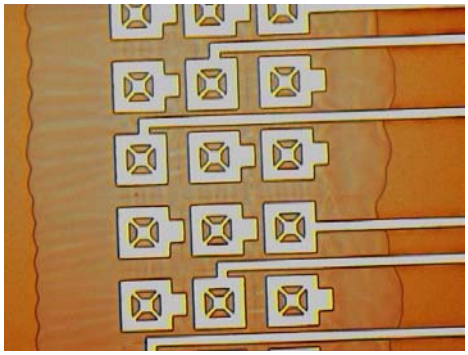


Fig. 3. 22 Released Compliant Structures

Fig. 3.22 shows several released compliant structure. The release time was 350 seconds. We can see the entire compliant structure has been peeled off due to prolonged releasing time. If there is no silicon dioxide layer on top of the surface, the entire structure may totally be peeled off. From this experience, we draw a conclusion that proper control of the release time is the most important in releasing the fine feature-size structures. Optimum parameters need to be found in future research.

For the above mentioned two approaches, the supporting layer thicknesses are limited by the process. For the first approach, the silicon dioxide thickness cannot be deposited thicker than 5μm. For the second approach, the amorphous silicon can only be deposited thinner than 2μm. In both cases, the compliant structure will only have vertical compliance less than the thickness of the underneath layers. As such, this small vertical compliance will become a major limitation for the interposer, which is supposed to take up the vertical non-planarization of I/O pins on the entire N-WLP wafer. Thus, other materials which can be fabricated at a much larger thickness while

at the same time serve as a dielectric layer must be found or developed. A good candidate is the benzocyclobutene (BCB). In order to explore the possibilities of using BCB in our devices, we successfully developed our own process recipe for more than 10μm thick BCB film. The patterns turned out to be very good.

The process is as follows:

First, an adhesion promoter (AP3000) was spun onto the wafer, and then BCB was spun onto the wafer at a speed of 2000rpm. This is a critical parameter for controlling the thickness of the BCB film. The wafer was then placed on a hot plate at 100^{o}C for 90 seconds. After baking, a lithography step followed by a patterning step was performed. The exposure time was 65 seconds. The exposed areas on the wafer formed crosslink and would not be able to be developed away, while the unexposed areas would be developed away. After lithography, the wafers were baked for another 90 seconds at 100^{o}C. After baking, the wafers were now to be developed. The developer used was DS2100. After developing, the wafers were baked one more time to stabilize the structures. The BCB patterns on the wafer were still relatively soft. A thermal cure step is required to make these patterned structures become stable.

The use of BCB to replace SiO_2 in the first approach enables a larger vertical compliance of the structure that is not limited by the supporting layer thickness. These complaint structures are limited by the cantilever beam length as shown by our simulations.

There are many alternatives by changing one or two of the procedures mentioned above. For example, a dry etch can be used which will give us better profiles but it will take a longer etch time.

We tried two different methods to etch the plating seed layer both dry etch and wet etch. In order to reduce the step difference, the seed layers of our interposer are

500 Angstroms of titanium and 300 Angstroms of gold. They are sputtered onto the dielectric layers. For the wet etch method, we found that it is only applicable to plate gold on top of the gold seed layer. If copper was plated, some reactions could take place that resulted in the formation of intermetallic compounds. It was found that small patterns cannot keep their original shape and some metallic traces would just merge together. Fig. 3.23 shows some well-defined gold plated traces etched in Ague regia for 90 seconds.

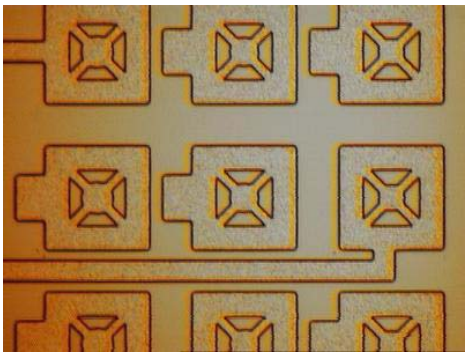


Fig. 3. 23 Wet Etch in Agua Regia for 90 Seconds (Gold Plated Traces)

Dry etch can be used to etch both plated copper and gold. The dry etching parameters were: power = 300Watts, pressure = 50mTorr, N2 gas flow rate = 46sccm. Using these process parameters, the etching rate was more than 20A/min. For over etching purpose, we etched the 300 Angstroms of gold for 40 minutes and the titanium layer for 6 minutes, respectively. The process parameters for titanium etch were: power = 280Watts, pressure = 55mTorr, temperature =25^{o}C, O_2 gas flow rate = 16sccm, CF_4 gas flow = 20sccm. Under these conditions, the etching rate for titanium was 216A/min. Fig. 3.24 shows a copper plated structure which underwent a 40 minutes gold seed layer sputtering and 6 minutes titanium seed layer sputtering. As can be seen, the etch profile is good. We checked the conduction resistance on the wafer resistance

surface; it did not give any electrical conduction. As such, the seed layers had been completely etched away.

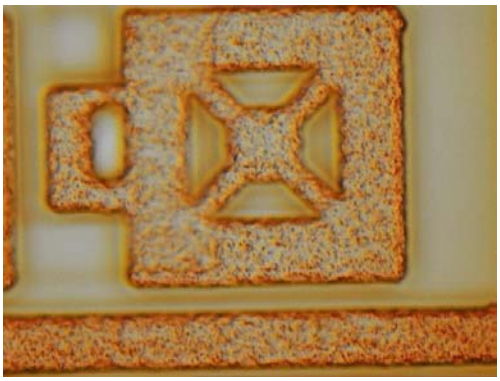


Fig. 3. 24 Gold and Titanium Seed layers Sputtered

Another problem observed during the process was that after the copper plating step, a layer of gold was required to protect the copper as the copper is easily oxidized. We can see from Fig. 3.25 that the entire wafer became greenish in colour because of the copper oxidization during the subsequent TEOS deposition and photoresist strip process steps. This will severely affect the electrical performance of the device. Since copper has lower electrical resistance than gold, and is cheaper than gold, to use copper as the metal layer is the trend. The penalty is that the fabrication process becomes more complicated.

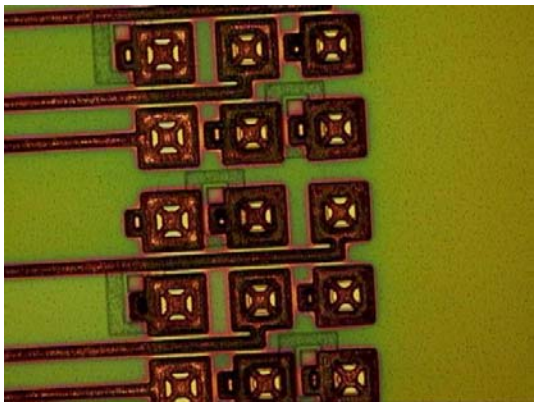


Fig. 3. 25 Plated Copper Oxidized

CHAPTER 4: Mechanical and Electrical Simulation

Simulation is an important tool in semiconductor development from the design/experiments as well as economic perspective. The results can guide us in the design and actual fabrication. Thus, ANSYS and Ansoft's HFSS, HPADS were employed to simulate the mechanical and electrical properties of the interposer.

4.1 Mechanical Properties

The z-axis compliance of an electrical tester is one of the important parameters that need to be characterized. A high compliance is desirable as this will enable the testing of chips with poor coplanarity of interconnections without inducing high contact forces. A nano-indenter was used to measure the z-axis compliance of the fabricated interposer and ANSYS was used to simulate it.

Nano-indentation Test

The nano-indenter machine deflects the pad while recording the force applied as a function of vertical displacement. From the force-deflection characteristics, the z-compliance of the interposer pad can be determined very accurately. (Hong et al.,1989, 1991). The schematic drawing is shown in Fig. 4.1.

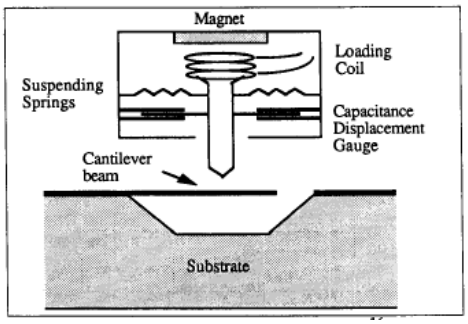


Fig. 4. 1 Nano-indenter in Beam Deflection Configuration
(Hong et al., 1989, 1991)

The applied force was to be loaded in 10 seconds and also unloaded in 10 seconds on the square shaped pads. The force-deflection curves obtained from two tests are shown in Fig. 4.2 and Fig. 4.3. From Fig. 4.2 we can see that the force varies fairly linearly with deflection. However, there appears to be a drift of 3 nm around the middle. Correcting for this drift, the compliance of the pad structure may be calculated to be (35-3)/95 = 0.337mm/N. From the results of the second test shown in Fig. 4.3, it can be seen that the force-deflection characteristic is not as linear as for the first test. We also observed that there was zero force corresponding to the first 16nm travel of the indenter tip. This was probably due to the fact that the indenter tip had not touched the pad surface when the displacement data began to record. So the maximum effective deflection of the pad corresponding to 140μN of applied force should be 68-16 = 52nm. This corresponded to a compliance of 52/140 = 0.371mm/N. So actually the two tests gave quite close values for the compliance of the square structure, i.e. average compliance = 0.354mm/N.

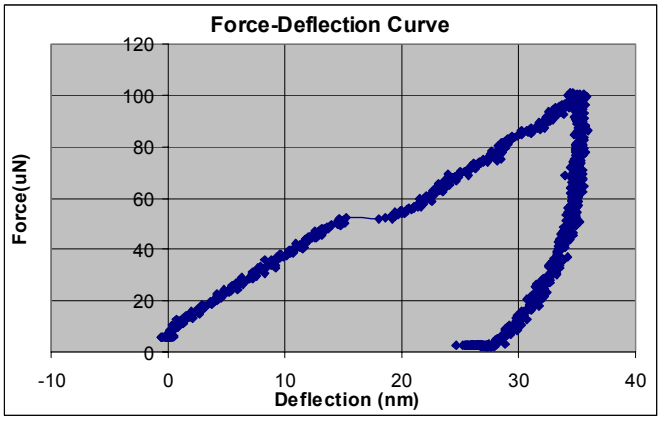


Fig. 4. 2 Force-deflection Curve for 100uN Load

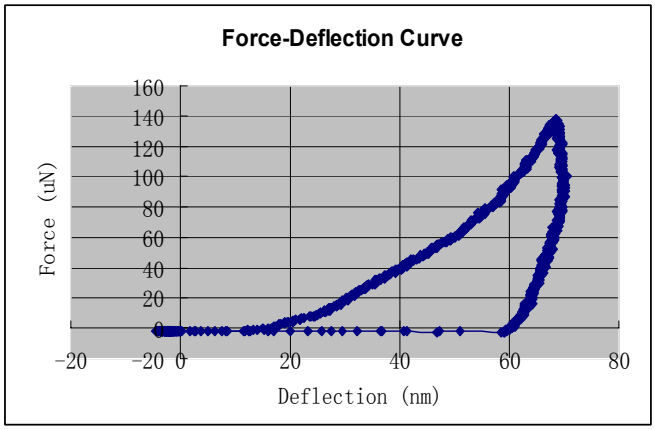
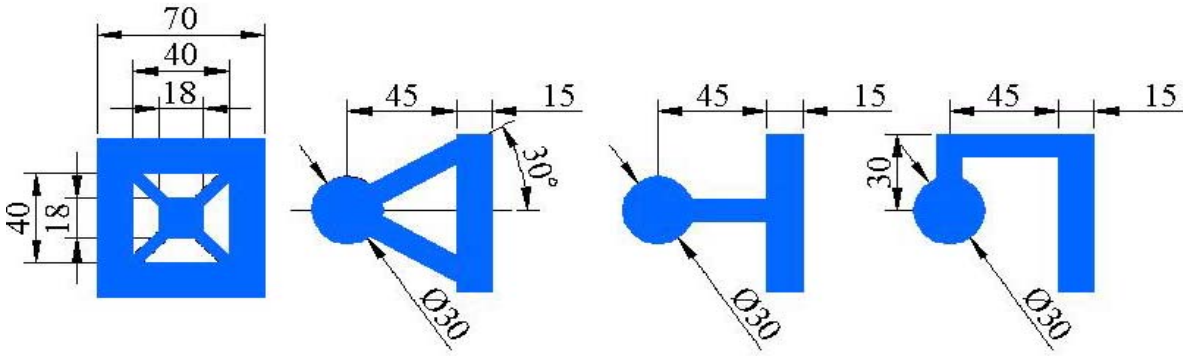


Fig. 4. 3 Force-deflection Curve for 150uN Load

4.1.1 Finite Element Simulation

Finite element simulations of the z-compliance of our compliant interposer structures were accomplished through ANSYS. Fig. 4.4 shows the compliant structures that have been simulated. There are several different configurations of the structures, all constrained by the limited space available in a 100μm pitch. The beams that connect the pad are all 10μm in width except for the first structure which is 5μm in width. For the simulation of all the structures the outer ends of the beams supporting the pads are assumed to be fixed. This can be seen from Figs. 4.5-4.7. It should be noted that the space under the pad and the beams is hollow, as the sacrificial layer previously underneath had been etched away. Thus the pads can move downward when subjected to mechanical loading. In the simulations, we assume the material is linear elastic and isotropic. Its Young's modulus is taken to be 124GPa, and the Poisson's ratio 0.345. The Ansys finite element type is selected to be SOLID92, which is a 3D element. A pressure loading of 10 standard atmosphere pressures is applied on the surface of the pads.



Square **triangle** **Straight** **L-shaped**

Fig. 4. 4 Layout of the Simulated Structures

(Note: All dimensions are in micrometers.)

4.1.2 Simulation Results

The simulation results are summarized in the table below. Figs. 4.5 to 4.7 show contour plots of vertical deflections for the last three structures.

Pattern	Square frame	Triangle support	Straight beam	L-shaped beam
Vertical deflection (μm)	0.130287	20.528	37.414	74.872
Compliance (mm/N)	0.397	28.7	52.3	104.6

From the table above, it can be seen that the value of 0.397 mm/N for the compliance of the square structure obtained from the simulation agrees well with the average experimental value of 0.354mm/N. The relative error is about 11%, which is within the range of experimental error.

From the result we also noticed that the last pattern gave the greatest compliance. We can conclude that this kind of structure is the best one which fully utilizes the space available and can provide the highest compliance under the same

load conditions. In order to get more compliance for a given space, we will need to make the cantilever structure trace longer. The greater the compliance, the greater the ability of the interposer to cater for non-planarity of the interconnections., We had put all the four types of structures on our test wafers so as to determine whether the process can be applied to all the patterns. It turned out that the process is successful in all of the patterns. So we will fabricate the L-shaped beam as our compliant test structure in the future. Due to the constraints in project time and the limitations in facilities at IME, our optimised test structures could not be fabricated. However, the results obtained in this section can be used as a reference for future development of compliant test structures.

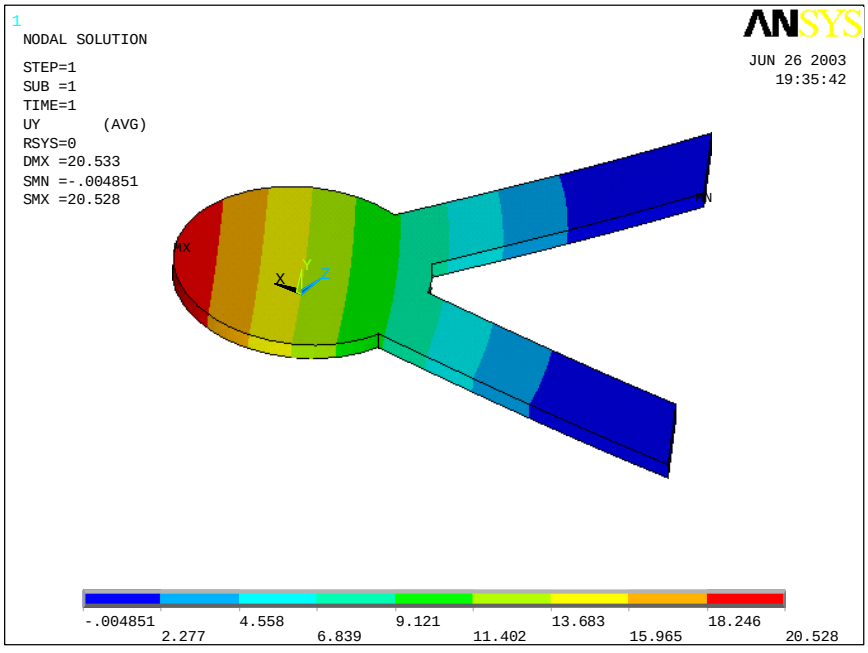


Fig. 4. 5 Distribution of Vertical Deflections for the Triangular Structure

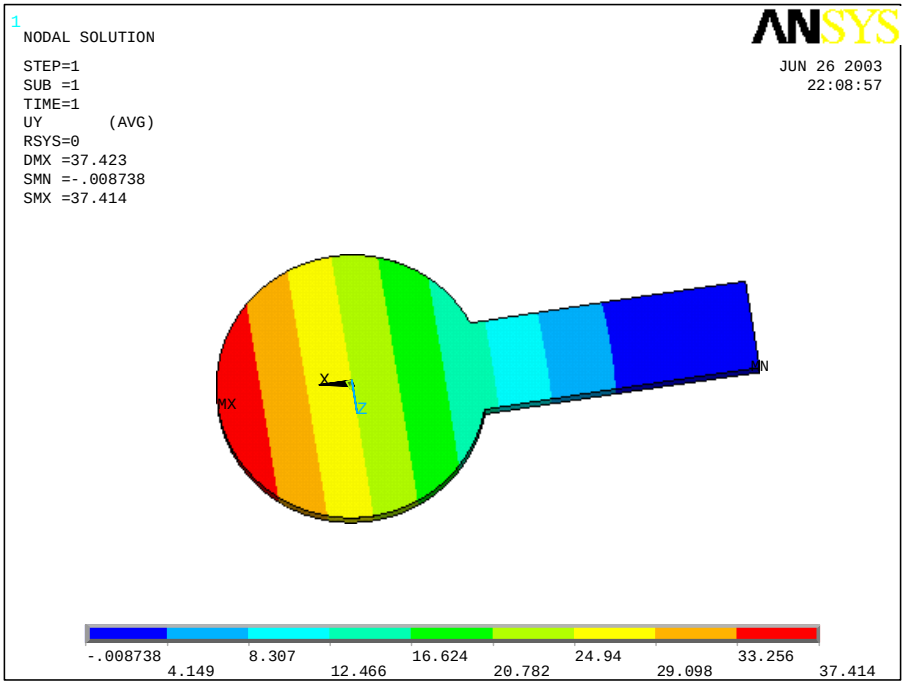


Fig. 4. 6 Distribution of Vertical Deflections for the Straight Beam

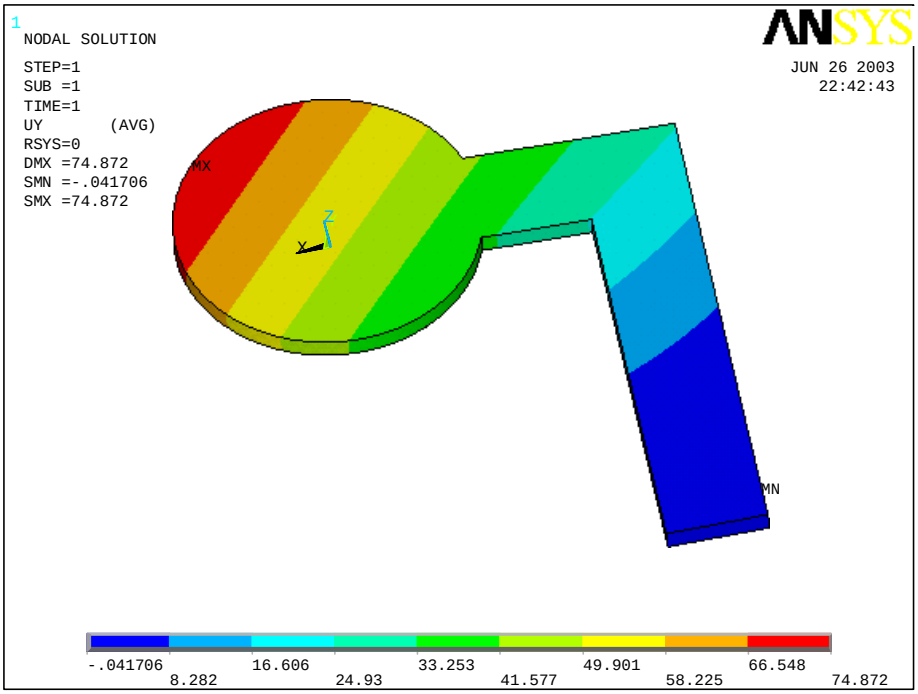


Fig. 4. 7 Distribution of Vertical Deflections for the L-shaped Beam

4.2 High Frequency Electrical Simulation

4.2.1 Simulation Approaches

The electrical response at high frequency of the interposer structure has been studied through modelling. A 3D full model of the structure has been built and solved within the Ansoft's HFSS full wave solver environment.

In order to understand the dynamics of the interposer losses and find the main parameters which influence the signal loss, we separate the interposer structure full model into three parts. The first part is considering the signal transmission through the silicon substrate, the second part is the one including the transmission structures (vias, pads, etc) through the upper build-up layers and the third part contains the long transmission lines and the compliant pad structures. Three-dimensional models for these parts have been built and solved followed by results analysis. 10GHz electrical signal was set to be the monitored signal. The signal loss (-db) versus frequency (GHz) diagrams were generated and analyzed. We also simulated the same structure with different materials so as to understand what kind of materials is more suitable for the high frequencies application.

4.2.2 Simulation Results and Analyses

Full model:

The full model includes the part that the signal transmits from the solder ball through interposer to the probe pad which connects the chip pad, which is shown in Fig. 4.8. In this model, the main materials are selected as follows: the substrate is silicon, the dielectric material is silicon dioxide and the metal traces are copper.

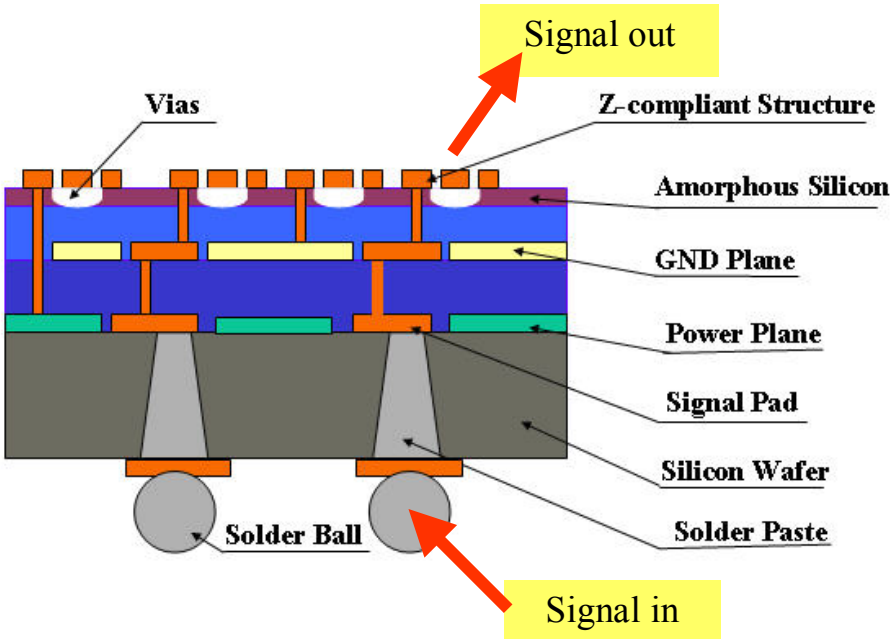


Fig. 4. 8 Schematic Drawing for the Full Model of the Interposer

The full model simulation results show a heavy loss response of the structure in the 0.1 to 10GHz bandwidth. The magnitude of the insertion loss is presented in Fig. 4.9. It can be noticed that the signal is completely attenuated by the interposer structure.

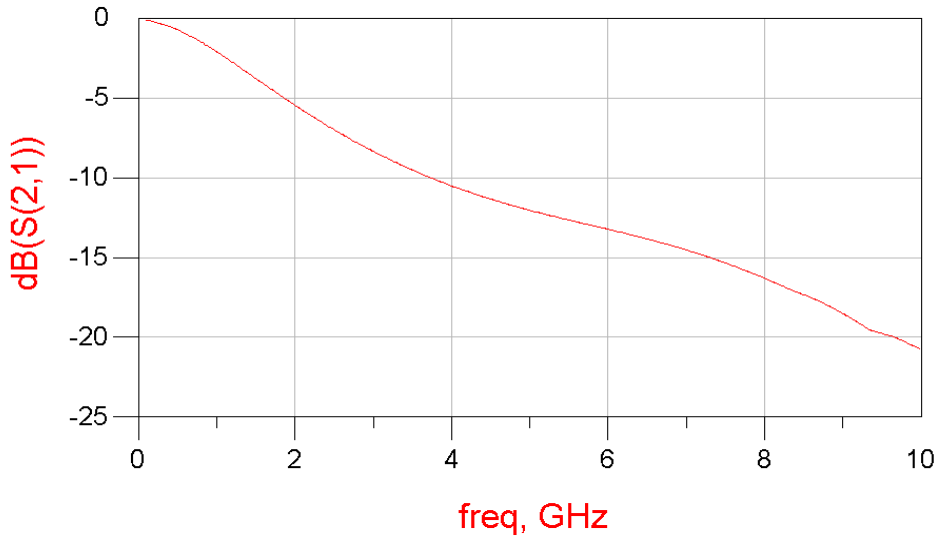


Fig. 4. 9 Magnitude of the Insertion Loss for the Interposer

Separate parts of the model:

As mentioned above, we separate the model into three parts. The first part is the signal going from the solder ball to the first metal pad-signal pad. The second part is the signal going from the signal pad through the build-up layer to the top metal pad, and the third part is the remaining structure which includes the top long trace and the compliant probe pad. The schematic drawing of the first and second parts models are shown in Fig. 4.10 and Fig. 4.11.

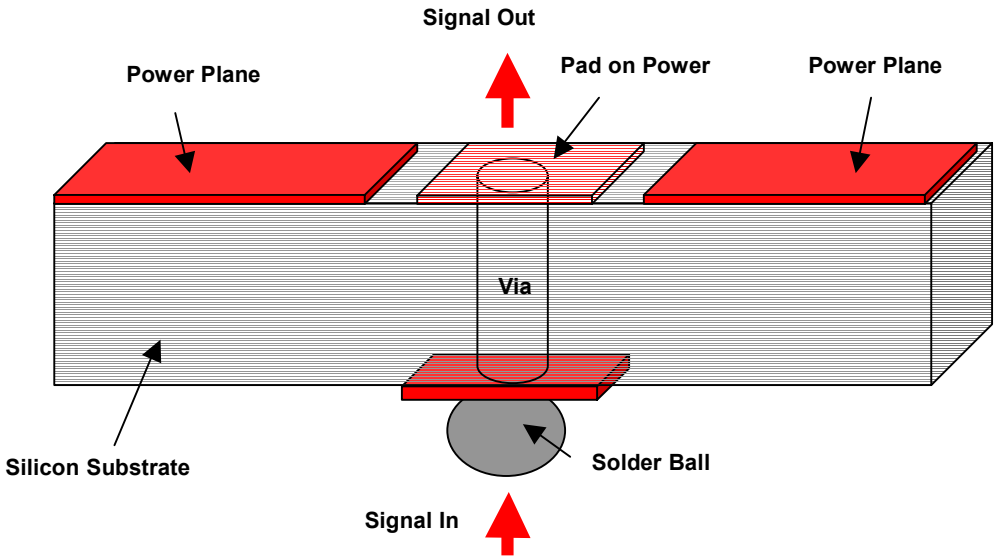


Fig. 4. 10 First Part of the Model

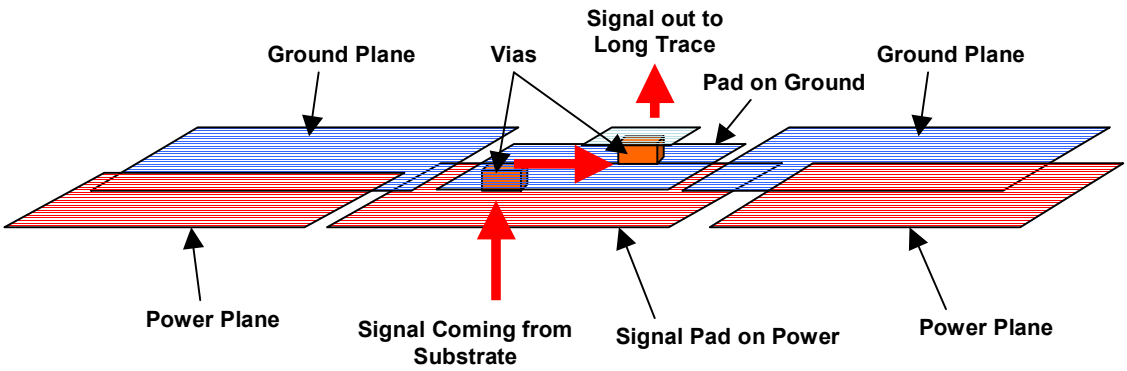


Fig. 4. 11 Second Part of the Model

From the simulation results of the three parts model which are shown in Fig. 4.12 to Fig. 4.14, we can see that the signal going through the second part has the heaviest electrical signal loss. As for the other parts, the loss is acceptable, below minus 3db or less.

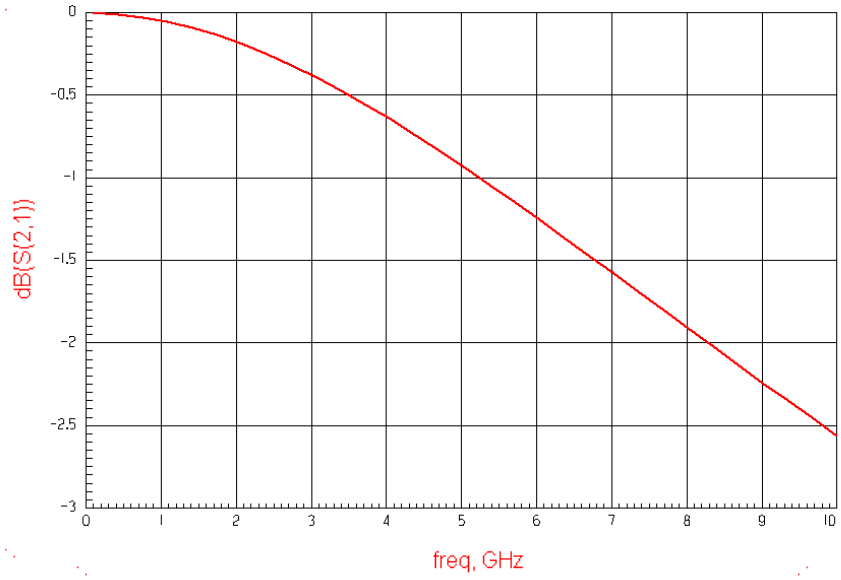


Fig. 4. 12 Insertion Loss for the 1st Part of the Model

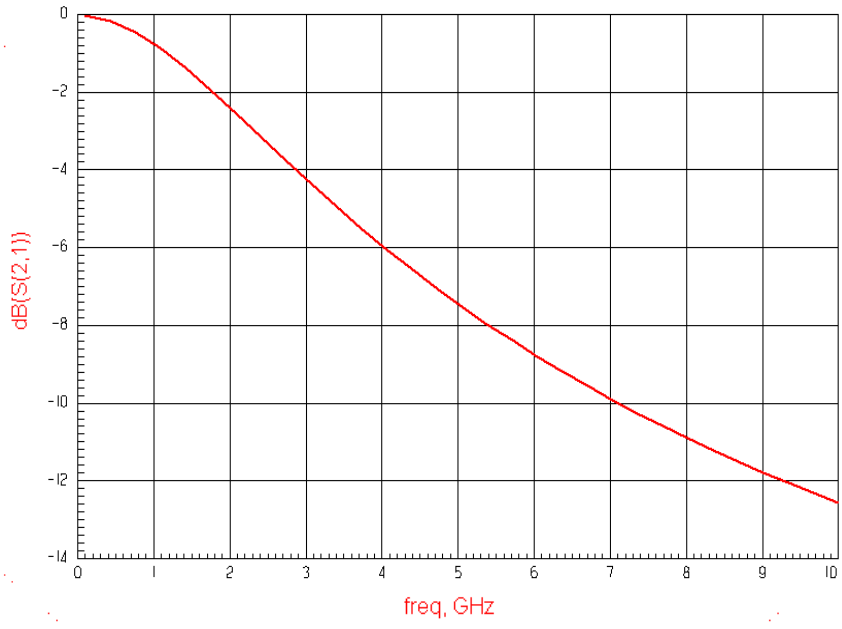


Fig. 4. 13 Insertion Loss for the 2nd Part of the Model

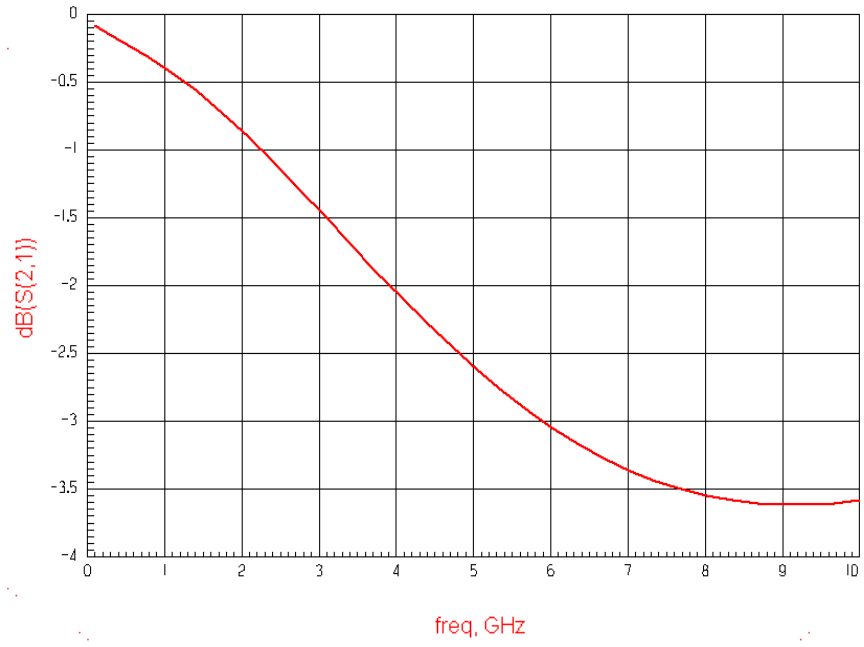


Fig. 4. 14 Insertion Loss for the 3rd Part of the Model

In order to find out the real reasons for the signal loss, several other models are built based on the second part model. These simulations include alternative material choices, dielectric layer thickness variables and the structure geometry etc.

First, material effects are investigated. Based on the second part model, we simulated two different materials (BCB and SiO_2) which are commonly used in the semiconductor industry. Comparing BCB (K =2.6) with SiO_2 (K=4), we found that in different frequencies, the electrical performances are different, as can be seen from Fig. 4.15 and Fig. 4.16. But we also notice that the situation is only slightly improved when using low K material BCB. So the material is not the main reason for the electrical loss in the interposer.

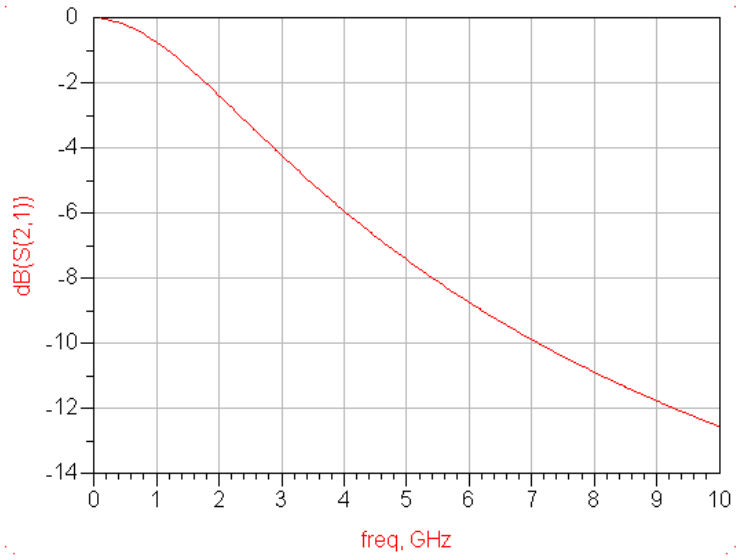


Fig. 4. 15 Insertion Loss for the 2nd Part of the Model
(BCB as Dielectric, K =2.6, thickness 2μm)

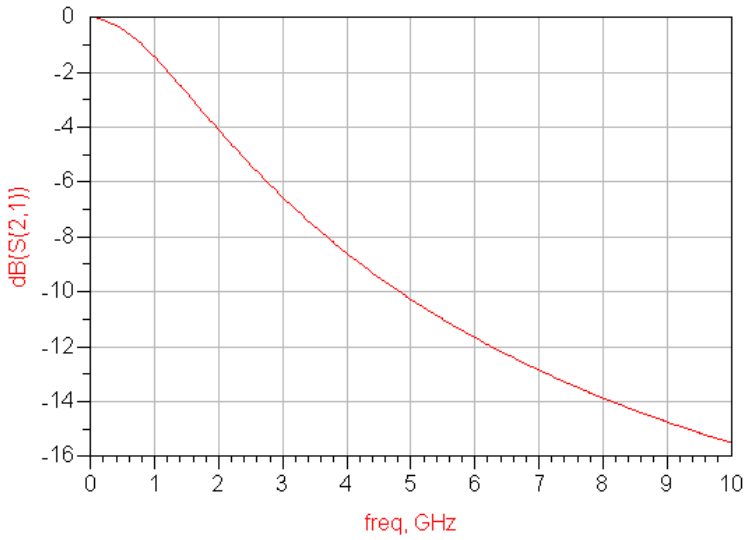


Fig. 4. 16 Insertion Loss for the 2nd Part of the Model
(SiO_2 as Dielectric, K =4, thickness 2μm)

The second exploration is to investigate the geometry effect on the electrical performance. In the original model, the signal pad on the power plane is very big; the ground plane covers part of the signal pad. The signal comes from the big pad through little via up to the ground plane pad, then passing the second via to the top pad which

connects the long trace to the compliant structure. Big capacitance effects and reflection appear at the different interfaces.

A model is built. In this model, part of the ground plane that is above the signal pad is cut off. (Fig. 4.17)

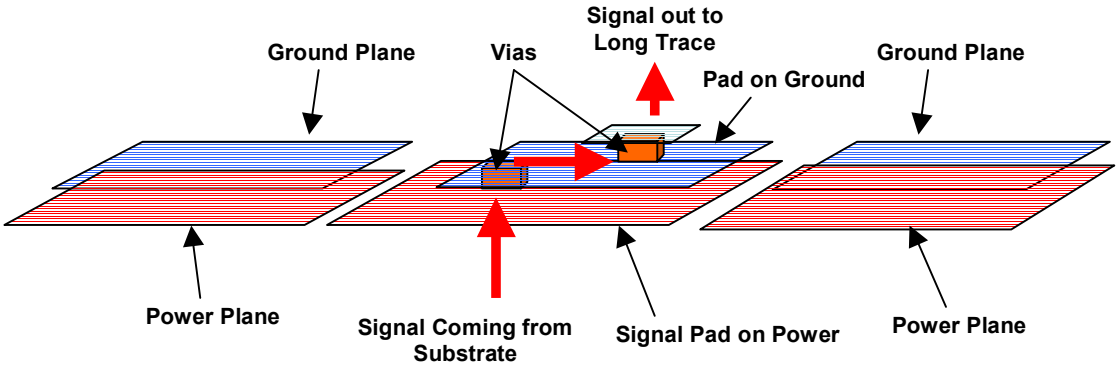


Fig. 4. 17 Partially Cut-off Ground Plane Model

In this model, by reducing the parasitic capacitance that appears between the signal pad and the metal ground plane above, the insertion loss of the second part of the interposer is reduced drastically (Fig. 4.18).

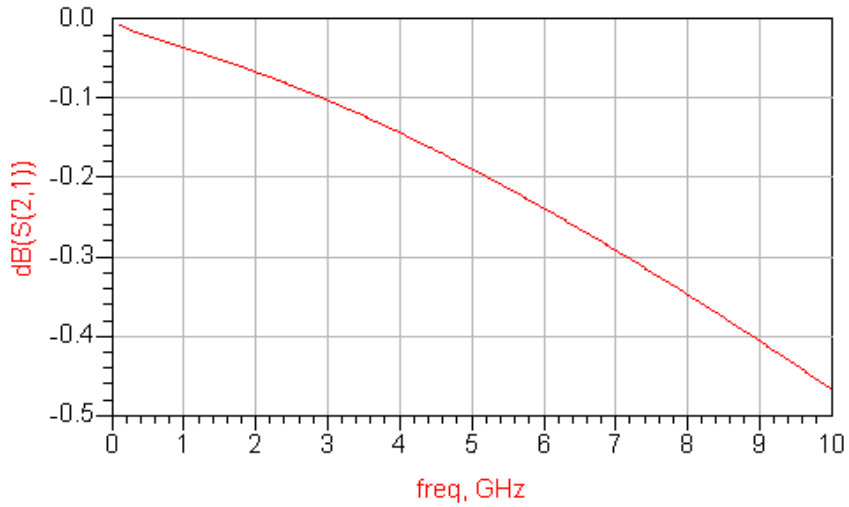


Fig. 4. 18 Insertion Loss for Partially Cut-off Ground Plane Model
(BCB as Dielectric, thickness 2μm)

In another model, the ground plane is deleted completely. It shows a result similar to the one which has partially cut-off ground plane, because there is no capacitive effect from the ground plane. However, in the model where the power plane is deleted completely, we cannot get a similar result, while we get the same result as the original model, which has big electrical loss.

Based on the Partially Cut-off Ground Plane Model shown above, the effect of dielectric thickness on the transmission has been explored. As shown in Fig. 4.19, when the thickness of the dielectric material increases, the signal transmission improves (the parasitic capacitance is further reduced).

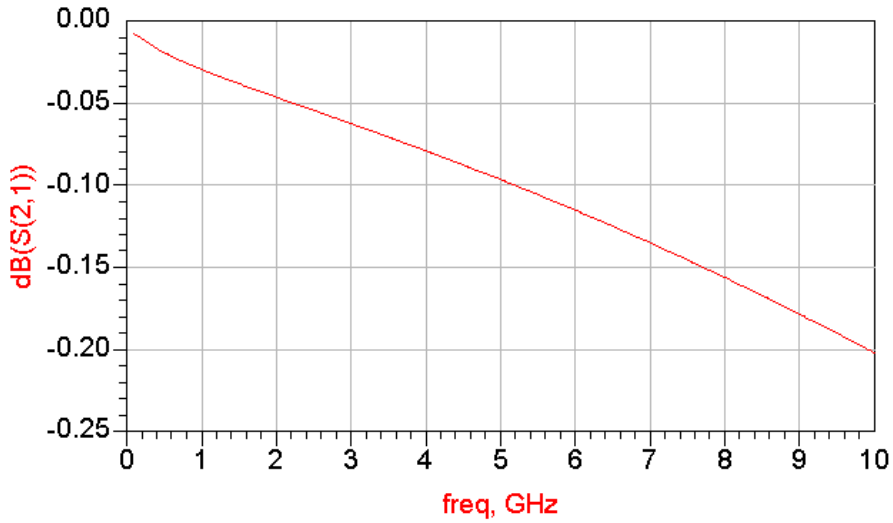


Fig. 4. 19 Insertion Loss for Partially Cut-off Ground Plane Model
(BCB as Dielectric, thickness 5μm)

4.2.3 Conclusion

From the above analyses of the electrical simulations at high frequencies, it can be concluded that the most important parameters which determine the behaviour of the electrical performance are the geometry of the structure and the components' relative positions. For the interposer, the main reason for the electrical loss came from the

parasitic capacitance which was created between the signal pad and ground plane. In the future design, we should avoid this parasitic capacitance. At the same time, the transition between layers should be smooth, and the thickness of the traces should be proper. But from the process point of view this is very difficult to realize. In the interposer design, there are some places which have sudden change of the aspect ratio. These features are undesirable, because the sudden change in the aspect ratio actually amplifies the reflections at these interfaces, which hampers the electrical transmission. But sometimes we cannot avoid this sudden change of aspect ratio just because of the process feasibility. For example, we cannot fabricate the second metal pad just on top of the first metal pad, which has little change of the aspect ratio. Instead, we have to move the second pad to avoid big step at the same location. The big step will cause process problem in the upper layer. So the design of the interposer should be a trade-off. Comprehensive consideration of the interposer structures becomes very important for fabricating an interposer which has both good mechanical and electrical performance.

CHAPTER 5: Conclusion

In this project, a new-type of interposer for electrical testing of fine-pitch wafer level packages has been designed and fabricated. Several process approaches have been successfully developed to fabricate the new-type of interposer. Although the fabricated interposers to date still have a lot of aspects that could be improved and researched, the basic concepts of fabricating the proposed interposers have been proven. We believe that as more advanced facilities become available in the future and more efforts are put into the development, we will be able to realize these interposers for actual test and burn-in for the nano wafer-level packaged devices.

Based on our simulation results, proper materials, optimized device structures and better process facilities are essential to fabricate the proposed interposer which can meet the requirements for the electrical test and burn in of fine-pitch wafer level packages.

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