

**FABRICATION OF ULTRA-SHALLOW JUNCTIONS AND  
ADVANCED GATE STACKS FOR ULSI TECHNOLOGIES  
USING LASER THERMAL PROCESSING**

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**NATIONAL UNIVERSITY OF SINGAPORE**

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## SUMMARY

With the continual scaling of the channel length and the gate dielectric thickness of conventional metal oxide semiconductor (MOS) transistors, it has become increasingly difficult or complex to form highly activated ultra-shallow junctions and near depletion-free polycrystalline silicon (poly-Si) gates that meet the stringent requirements of the international technology roadmap for semiconductors. This is in spite of extensive development work in the ion implantation and dopant activation technologies. In this project, a novel technique known as laser thermal processing (LTP) was employed to fabricate ultra-shallow  $p^+/n$  junctions and advanced poly-Si gate stacks for ultra-large scale integration technologies. LTP of ultra-shallow junctions typically involves the pre-amorphization of the silicon surface, followed by the melting of the amorphized regions (and the substrate) using a pulsed excimer laser. The extent of dopant diffusion is controlled by the melt depth and an extremely high degree of dopant activation is achieved upon recrystallization. To study the impact of LTP on the depletion of carriers at the poly-Si gate/gate oxide interface (poly-depletion), single or dual-layer capacitors with ultra-thin gate dielectrics were fabricated by subjecting as-deposited amorphous silicon gates to laser irradiation.

In this work, the dopant profiles were analyzed by secondary ion mass spectrometry (SIMS). Microstructural information was provided using transmission electron microscopy (TEM) and crystal defects were studied by Rutherford backscattering spectrometry (RBS). Capacitance-voltage (C-V) measurements and time-dependent dielectric breakdown (TDDB) studies were conducted to investigate the degree of gate-depletion and gate oxide reliability after LTP. The results show that LTP can form highly activated ultra-shallow  $p^+/n$  junctions with step-like dopant profiles. These characteristics are in sharp contrast

compared to the junctions formed by spike rapid thermal annealing (RTA). In addition, as evident from RBS and TEM results, LTP can virtually anneal all the crystal damage that is created by the pre-amorphization implant. It is further demonstrated that transient enhanced diffusion of boron occurs during a post-LTP anneal due to a supersaturation of excess interstitials in the end-of-range region. This enhanced diffusion can be significantly suppressed when the melt depth is extended beyond the amorphous layer.

The electrical data indicate that LTP, when combined with a post-LTP anneal, increases the carrier concentration (up to ~63% for arsenic-doped gates) at the poly-Si gate/gate oxide interface. Thus, the LTP + RTA process readily reduces the poly-depletion effect. SIMS depth profiles clearly show an increase in dopant concentration near the gate/gate oxide interface for samples that were subjected to LTP prior to the gate activation anneal. For  $p^+$ -gated capacitors, a reduction in poly-depletion is achieved without observable boron penetration. TDDB studies show an improvement in gate oxide reliability after LTP at high fluences. It is thus concluded that LTP, with a near-zero thermal budget, is a promising technique to fabricate ultra-shallow junctions as well as to process advanced poly-Si gate stacks for future generations of semiconductor devices.

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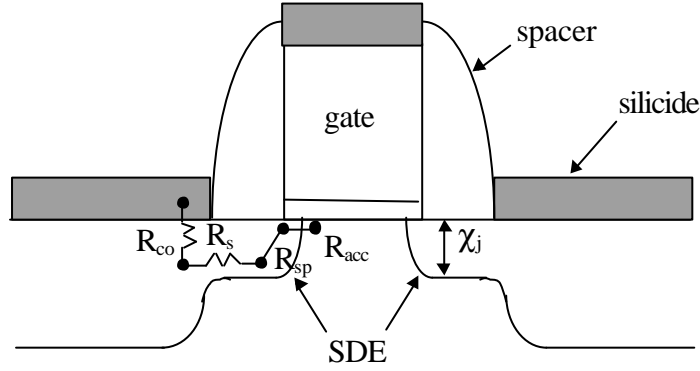
# CHAPTER 1

## INTRODUCTION

### 1.1 Background

The 2001 international technology roadmap for semiconductors (ITRS) projects source/drain extension (SDE) junctions to be 22-36 nm, with sheet resistance,  $R_s$  of less than 460  $\Omega/\square$  for advanced ( $< 75$  nm printed gate length) complementary metal oxide semiconductor field effect transistors (MOSFETs) [1]. Reducing the channel length of a MOSFET is the most appropriate way to increase the drive current and circuit density. However, this is often accompanied by a reduction in threshold voltage and an increase in the sub-threshold leakage current [2]. Hence, in order to minimize short channel effects and to confine the electric field profile in the channel region, the vertical junction depth ( $\chi_j$ ) should be scaled down appropriately [2]. The main challenge in the formation of ultra-shallow SDE junctions is the optimization of  $\chi_j$  to achieve low series resistance with good transistor turn-off performance [2, 3]. Referring to Fig. 1.1, the total series resistance,  $R_{tot}$  comprises the contact resistance due to the silicide ( $R_{co}$ ), sheet resistance of the doped layer ( $R_s$ ), spreading resistance where the carrier path turns toward the channel ( $R_{sp}$ ) and the voltage dependent accumulation resistance where the gate overlaps the junction,  $R_{acc}$  [see Eqn. (1.1)]. These parameters are in turn dependent on the doping profile, degree of dopant activation and  $\chi_j$  [2]. A reduction in  $R_{tot}$  will lead to an increase in the drive current.

$$R_{tot} = R_{co} + R_s + R_{sp} + R_{acc} \quad (1.1)$$



**Figure 1.1** Schematic showing the components of the total series resistance.

However, it has become increasingly difficult and complex for the conventional ion implantation and dopant activation technologies to fabricate junctions with the desired characteristics due to the well-known tradeoff between  $\chi_j$  and  $R_s$  [2-4]. This tradeoff is a direct consequence of the physical limits imposed by the diffusion and solid solubility of the dopant atoms in silicon. Furthermore, these technologies do not produce junctions with the ideal “box-shaped” profiles that meet the requirements of ITRS [1]. Such constraints have led a recent study [5] to conclude that continual junction scaling of  $\chi_j$  to less than 40 nm would result in little to no performance gain. This is because any improvement in short channel effects due to reduced charge sharing is offset by a large increase in external resistance. Compared to  $n^+/p$  junctions, ultra-shallow  $p^+/n$  junctions using boron ion implantation are more difficult to form due to channeling of boron ions and transient enhanced diffusion (TED) of boron during post-implantation annealing [2-4, 6, 7]. TED is mainly caused by the interaction of boron atoms with the excess interstitials generated during ion implantation. It has been demonstrated that TED is significantly suppressed by reducing the implantation energy to sub-keV energies [6-8]. Besides reducing the energy of the ion implantation, TED can also be minimized by performing an optimized sub-amorphizing

implant and by reducing the thermal budget of the post-implantation anneal [3, 6, 9]. The function of the sub-amorphizing implant is to reduce channeling of the dopant ion (such as  $B^+$ ), and to create a vacancy-rich region for the provision of vacancies to recombine with the interstitials produced by the dopant ion implantation, thereby resulting in less excess interstitials that can contribute to TED [9].

Previous studies have shown that when the ion implantation energy is low enough for TED to be almost negligible, a diffusivity enhancement factor of approximately four still exists [10]. In this case, boron enhanced diffusion (BED) is believed to be responsible for the diffusion enhancement. Agarwal *et al.* [10] have shown that BED is driven by the interstitials produced in the boron-containing silicon layer during the annealing process when the boron concentration exceeds a threshold of a few atomic percent. The importance of the control of annealing ambient is emphasized by the observation of oxygen enhanced diffusion (OED). The presence of oxygen during annealing will lead to oxide growth on the silicon substrate. During oxide growth, interstitial defects are injected into Si, resulting in increased boron diffusion into bulk silicon [11]. The need for ultra-shallow junction fabrication has led to the development of new processes such as ultra-low energy ion implantation, spike rapid thermal annealing (RTA), gas immersion laser doping (GILD) and laser thermal processing (LTP) [2, 12-14]. Among these, LTP is the most promising technique because it produces abrupt, highly activated and ultra-shallow junctions.

The advantages of LTP are (i) “near-zero” thermal budget (since laser pulses last only for tens of nanoseconds), (ii) extent of dopant diffusion is controlled by the melt depth (with negligible diffusion in the adjacent solid substrate), and (iii) rapid quench rate (metastable process). This allows active dopant concentrations to exceed the solid solubility limit [13,

14]. The disadvantages associated with LTP are (i) low throughput, (ii) differential absorption of laser light across patterned structures, and (iii) deactivation/diffusion of the dopants during post-LTP anneal steps.

Another critical aspect of MOSFET scaling is the depletion of carriers at the polycrystalline silicon (poly-Si) gate/gate oxide interface [15-18]. After doping the poly-Si gate, a RTA is usually performed to activate the gate dopants. However, the anneal may be insufficient to drive the implanted impurities down the entire depth of the gate. Consequently, a portion of the poly-Si gate nearest to the gate oxide will be depleted of carriers (poly-depletion), which degrades the device performance [16]. With reference to p-MOSFETs, although the temperature and/or time of the gate activation anneal can be increased to reduce the poly-depletion effect (PDE), extensive diffusion of boron may occur such that boron diffuses through the thin gate oxide into the channel. This phenomenon is known as boron penetration. It is well known that boron penetration causes threshold voltage instabilities and deteriorates gate oxide reliability [16-18].

## **1.2 Scope of the Project**

This project involves the fabrication (using LTP) and characterization of ultra-shallow p<sup>+</sup>/n junctions and advanced poly-Si gate stacks for ultra-large scale integration technologies. For the formation of ultra-shallow junctions, silicon substrates were first pre-amorphized by Si<sup>+</sup> or Ge<sup>+</sup>. Boron ions were then implanted using ultra-low energy ion implantation. Comparisons were made between the dopant profiles of laser-processed and spike rapid thermal annealed samples. Further work was done to investigate the crystal quality after LTP, and how residual defects affect the enhanced boron diffusion during a

post-LTP anneal. The ultra-shallow junctions were mainly characterized using secondary ion mass spectrometry (SIMS), transmission electron microscopy (TEM) and Rutherford backscattering spectrometry (RBS). To study the impact of laser irradiation on PDE, MOS capacitors with ultra-thin gate oxides were fabricated using LTP. Single or dual-layer poly-Si gated capacitors were processed after the as-deposited amorphous silicon (a-Si) gates were exposed to laser irradiation. Detailed characterizations of the gate stacks/capacitors were carried out using capacitance-voltage (C-V) measurements, SIMS, TEM and time-resolved reflectance (TRR) measurements. The mechanism of the improvement in PDE after LTP (for both  $n^+$  and  $p^+$ -gated capacitors) is elucidated based on the results.

### **1.3 Objectives**

1. To determine the effect of ramp-up rates of spike RTA on dopant redistribution and compare the dopant profiles with those obtained after conventional RTA.
2. To investigate the effect of different laser fluence on junction depth after LTP and compare the dopant profiles with those obtained after spike RTA.
3. To examine the crystal quality or residual defects after LTP and check the effect of these defects on the boron diffusivity enhancement during a post-LTP anneal.
4. To investigate the effect of a metal capping layer on the melt characteristics of a gate stack during LTP.
5. To study the effect of LTP on dopant activation at the poly-Si gate/gate oxide interface, with and without an additional rapid thermal anneal.

## **1.4 Organization of the Thesis**

The organization of the thesis and a brief synopsis of the various chapters of this thesis are provided as follows:

- **Chapter 1: Introduction**

This chapter covers some introductory information pertaining to the subject matter of this study. It also describes the scope and objectives of this project.

- **Chapter 2: Literature Review**

This chapter provides the background and relevant theories of ultra-shallow junction formation, laser interaction with materials and the poly-depletion effect. It also gives a detailed review on the subject matters of this study based on earlier works.

- **Chapter 3: Experimental**

This chapter describes the experimental setup and the sample preparation methods. It also includes the test methodologies and the simulation procedures used in this work.

- **Chapter 4: Simulation of Laser Irradiation on Silicon**

This chapter shows the results from the simulation of the laser interaction with silicon using the SLIM software. These results (e.g. melt depth vs. time, heating and cooling rates) provide some basic understanding of the LTP and the melt phenomenon.

- **Chapter 5: Formation of Ultra-shallow Junctions Using Laser Thermal Processing**

This chapter describes and compares the two most promising techniques that can be

employed to form ultra-shallow  $p^+/n$  junctions. For each technique, the discussion will include the analyses of the junction depth, the abruptness of the junction, and the sheet resistance of the boron-doped layer.

- **Chapter 6: Annealing of Crystal Defects by Laser Thermal Processing**

This chapter discusses the effect of LTP on the annealing of crystal defects. The role of the excess interstitials in the EOR region in the enhanced diffusion of boron during a post-LTP RTA is also reported.

- **Chapter 7: Phase Transformations During LTP of Gate Stacks**

This chapter presents the results and relevant discussions pertaining to the phase transformations during LTP of gate stacks. It begins with the determination of the effect of a TiN/Ti cap layer on the melt characteristics of poly-Si. The second part of the chapter discusses in detail the data obtained from TRR measurements.

- **Chapter 8: Reduction of Poly-depletion Using Laser Thermal Processing**

This chapter reports the electrical results obtained from single or dual-layer poly-Si gated capacitors. The effect of LTP on reducing poly-depletion is interpreted from C-V data and SIMS profiles. In addition, the effect of LTP on the gate oxide reliability is presented.

- **Chapter 9: Conclusions**

This chapter summarizes the major results and findings, and provides conclusions based on these findings in the light of the objectives of this project. Recommendations for further experimental work are also given.



## **CHAPTER 2**

### **LITERATURE REVIEW**

#### **2.1 Introduction**

This chapter begins with an overview on the formation of ultra-shallow junctions and transient enhanced diffusion, and proceeds to cover the relevant theories on laser interaction with materials. It also covers the poly-depletion effect and ways to prevent boron penetration. In general, the chapter gives a detailed review on the subject matter of this study based on earlier works.

#### **2.2 Ion Implantation**

For more than 15 years, ion implantation has been the method of choice for doping semiconductor devices [2, 7]. One of the complications that can arise during ion implantation is channeling, and this occurs when the ion velocity vector is parallel to a major crystal orientation [7, 19]. In this situation, some ions may travel considerable distances with little energy loss since nuclear stopping is not very effective, and the electron density in a channel is low. Once in a channel, the ion will continue in that direction, making many internal collisions that are nearly elastic until it comes to rest or de-channels.

Channeling is more pronounced when implanting light atoms on axis into a heavy matrix and can produce a significant tail on the dopant distributions [6, 7]. Thus, off-axis implantation with a typical tilt angle of  $7^\circ$  is performed to avoid this tail. However, the effect of tilt angle is found to be almost negligible for ultra-low energy ion implantation [6]. In fact, Foad *et al.* [6] have demonstrated that channeling of  $B^+$  still occurs when the implantation

energy decreases to as low as 1 keV.

Owing to the larger molecular weight of  $\text{BF}_2$  as compared to boron,  $\text{BF}_2^+$  may also be used for ion implantation to form shallow junctions. This method decreases the depth to which the B atoms are implanted because the fluorine atoms damage the surface and reduce boron channeling. Moreover, since the  $\text{B}^+$  ion only acquires  $11/49$  (ratio of the mass of  $^{11}\text{B}$  over  $^{11}\text{B}^{19}\text{F}_2$ ) of the energy of  $\text{BF}_2^+$ , it does not penetrate deeply into the silicon substrate [7, 19]. However, this technique has several disadvantages. For instance, it was found that the fluorine atoms retard boron activation and also reduce the rate of recrystallization of the amorphous region [20, 21]. Furthermore, the use of  $\text{BF}_2^+$  for the SDE implantation would imply that  $\text{BF}_2^+$  is also implanted into the gate. It follows that the presence of fluorine in the gate would enhance boron penetration into the channel as compared to pure boron implants. This was explained by the increase in boron diffusivity through the poly-Si gate and gate oxide [18, 22]. Another method to minimize channeling is to disorder the crystal lattice prior to implantation. This is achieved by pre-amorphizing the Si surface with ions such as  $\text{Si}^+$  or  $\text{Ge}^+$  [21, 23]. One major drawback of this technique is that the amorphous region must be recrystallized, and residual defects such as end-of-range (EOR) loops may remain after annealing [23, 24]. In order to remove these defects completely, it is necessary to anneal at a higher temperature; this however will cause undesirable dopant diffusion into the silicon substrate [25].

Germanium is normally preferred over silicon for the pre-amorphizing implant (PAI) because a lower dose is required for  $\text{Ge}^+$  implantation to form a continuous amorphous layer. In addition,  $\text{Ge}^+$  implantation is known to produce a sharper amorphous/crystalline (a/c) interface. This helps to inhibit the nucleation of hairpin dislocations during annealing and

thus results in less extended defects and less leakage [21, 24]. Recent studies have shown that the degree of boron activation is greater for  $\text{Ge}^+$  PAI as compared to  $\text{Si}^+$  PAI [26, 27]. This is largely due to the strain compensation provided by the larger Ge atoms in the silicon matrix. Hence, more boron atoms (which are smaller than Si) are able to move into substitutional sites during annealing [26] and become activated. The conditions for ideal shallow junction formation are that the implanted boron profile should be confined within the amorphous region, and that the final junction should completely contain the defects formed at the previous a/c interface [25, 28].

The junction depth can also be reduced by implanting the dopants through a thin ( $\sim 20$  nm) screen layer such as silicon dioxide [7, 19]. It has been proposed that this sacrificial layer randomizes or reduces the ion velocities before entering the crystal, thus minimizing channeling effects. Another reason for using a screen oxide layer is that the implanted dopant profile can be moved closer to the Si surface [7]. The problems associated with this method are: (i) oxygen may be “knocked on” into the substrate and (ii) some dopants will be trapped in the oxide film resulting in dose loss [23]. Alternatively, ultra-shallow junctions can be obtained by using polyatomic (such as decaborane,  $\text{B}_{10}\text{H}_{14}$ ) cluster ion implantation [29, 30]. This technique produces ions with low equivalent energies because the kinetic energy of the cluster is shared between the constituent atoms. The concept used in  $\text{B}_{10}\text{H}_{14}$  cluster ion implantation is similar to that of the  $\text{BF}_2$  ion implantation except that it does not include the fluorine molecule that is deleterious to the gate oxide.

## 2.3 Rapid Thermal Annealing

Rapid thermal annealing (RTA) is often employed to anneal the primary crystalline damage caused by ion implantation as well as to activate the implanted dopants, i.e., to move the dopants to substitutional lattice sites [2]. If the Si substrate was pre-amorphized, RTA is also used to recrystallize the amorphous layer that normally extends up to the surface [7]. This recrystallization process initiates from the underlying substrate and regrowth proceeds toward the surface via solid phase epitaxy (SPE). Dopant activation is obtained by the conventional “soak” or the “spike” anneal method. A typical soak anneal profile involves ramping up to a target temperature of 1000 °C, with a soak time of about 10 s, then ramping down at a rate of ~75 °C/s [2, 6]. On the other hand, spike RTA utilizes much higher ramp-up rates (as high as ~400 °C/s) and reduces the soak time to  $\ll 1$  s [12, 14]. In this way, higher temperatures can be reached while maintaining a low thermal budget. Earlier works have shown that spike anneals produce shallower junctions with superior dopant activation efficiency [3, 31] as compared to soak RTA. It has been reported that shallow junctions with extremely low leakage currents can be formed by a two-step anneal process [2]. Firstly, a low temperature (~500-600 °C) furnace anneal is used to anneal the implantation-induced defects. This is followed by a high temperature RTA to activate the dopants [32].

Previously, “thermal budget” was represented by the product of time,  $t$  and the temperature,  $T$ . More precisely, in present non-isothermal systems, the thermal budget should denote the area under the  $t$ - $T$  curve [33]. Although several thermal budgets can be used to describe the same time-at-temperature to produce shallow junctions, ideally we should anneal at the highest temperature possible for the shortest duration [25].

### 2.3.1 Transient enhanced diffusion

In recent years, significant progress has been made in quantifying the physical processes involved in transient enhanced diffusion (TED) [4, 34-38]. During TED, the diffusivity of boron may be thousands of times greater than the intrinsic value for a short period of time [36]. The following gives a brief account on TED: when a dopant is introduced into the silicon substrate via ion implantation, the process will inevitably result in implantation-induced damage (Frenkel pairs consisting of vacancies and interstitials) in the silicon substrate. During the initial phase of annealing, as the implanted dopant atoms begin to occupy substitutional sites, most of the vacancies and interstitials recombine, leaving behind a net excess of interstitials with a dose approximately equal to that of the implant [4, 35, 39]. These excess interstitials (EI) quickly coalesce into metastable clusters/extended defects. This is the well-known “+1” model of Giles [39] and has been shown to be an useful approximation for modeling dopant diffusion. Upon further annealing, the extended defects dissolve and release excess interstitials that cause the enhanced diffusivity of dopant atoms (such as B and P) which diffuse either principally or in part by an interstitial(cy) mechanism in silicon [40]. Since the enhanced diffusion is driven by excess interstitials, it is therefore a “transient” process that lasts until the defects dissolve or are annihilated at a defect-sink such as the surface [2].

Based on theoretical calculations, the activation energy of the increase in junction depth is found to be negative when boron diffusion is dominated by the dissolution of interstitial-type defects [34, 35]. This implies that if TED is allowed to run to completion (i.e. complete dissolution of extended defects) at 750 °C, the resulting junction will be deeper than if it was formed at 1000 °C [3, 34]. This is the primary reason why high-temperature

spike anneals with fast ramp-up rates are being adopted for ultra-shallow junction formation.

For the range of implantation dose and energies required to fabricate SDE, Agarwal *et al.* [3] have illustrated that a point of diminishing return is quickly reached as ramp-up rate increases. This means that when the ramp-up rate is increased to above a certain value, further reduction in junction depth is insignificant. This is due to the limited practical ramp-down rate ( $\sim 70\text{-}90$  °C/s) of the anneal. Also, for spike anneals with ultra-fast ramp-up rates, the implant damage may not be annealed out during the ramp-up portion, hence TED is delayed from the ramp-up to the ramp-down portion of the thermal cycle [3]. After short, or low-temperature anneals (e.g. 750 °C at 15 s) following implantation of doses greater than  $10^{12}/\text{cm}^2$  but less than the amorphization threshold, extended defects are observed to be primarily of the  $\{311\}$  type. These consist of interstitial agglomerates located on the  $\{311\}$  habit plane and elongated in the  $\langle 110 \rangle$  direction [4]. This indicates that the source of interstitials for TED is the dissolution of the  $\{311\}$  defects that were formed during the initial stage of annealing. However, it was found that boron TED can also occur in the absence of  $\{311\}$  defects, suggesting that there may be more than one source of interstitials [37]. For high-dose boron ion implantation, it is believed that boron-interstitial clusters (BIC) are the source of interstitials for the enhanced diffusion [38].

In the case where Si was pre-amorphized, a different kind of defect evolution occurs [36, 40]. It is well established that after PAI, there exists a highly damaged region in the crystalline material just beyond the a/c interface [4]. This EOR damaged region contains a supersaturation of interstitial point defects generated during implantation. During the early stage of annealing, EOR loops (with a small fraction of  $\{311\}$  defects) are formed and they continue to grow at the expense of the  $\{311\}$  defects. Upon further annealing (at sufficiently

high temperatures), these EOR loops dissolve and release excess interstitials that induce boron TED [2, 41]. An excellent review on the mechanism of transient enhanced diffusion has been treated in details by Stolk *et al.* [4].

## **2.4 Laser Thermal Processing**

### **2.4.1 Excimer lasers**

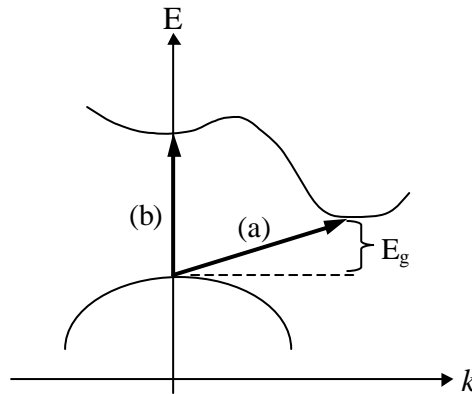
Excimer lasers are a family of lasers in which light is emitted by a short-lived molecule that consists of one rare gas atom (e.g. Argon, Krypton or Xenon) and one halogen atom (e.g. fluorine or chlorine). In practice, excimer lasers are excited by passing a short, intense electrical pulse through a mixture of gases containing the desired elements. Normally, more than 90 % of the mixture is a buffer gas (e.g. neon) that does not take part in the reaction [42]. Electrons in the discharge transfer energy to the gases, breaking up halogen molecules and results in the formation of electronically excited molecules. These molecules remain excited for a few nanoseconds and drop to the ground state, emitting a photon in the process. The most developed class of excimer lasers is the rare gas-halide lasers such as ArF, KrF and XeCl with wavelengths of 193, 248 and 308 nm, respectively [42].

### **2.4.2 Light absorption mechanism and optical properties of silicon**

There are a few mechanisms whereby light can be absorbed by semiconductors [43-45]. The absorption (and the heating) mechanism of the lattice depends greatly on the energy of the photon ( $h\nu$ ) and the band gap energy ( $E_g$ ) of the semiconductor (e.g. Si). In general, photons with energies larger than the band gap are readily absorbed into the surface regions of the semiconductor. The energy of these photons is transferred to the electronic

system of the substrate, which in turn is transferred to the lattice in a time much shorter than the pulse duration [43]. The resultant energy is then utilized to heat (or even melt) the surface layer such that the temperature of the underlying material is not significantly raised. Since the lasers (XeCl and KrF laser) used in this work produce photons with energies ( $h\nu \sim 4$  eV and  $\sim 5$  eV, respectively) larger than the band gap energy of Si ( $E_g \sim 1.12$  eV), we will only consider the absorption mechanism in the case when  $h\nu > E_g$ .

For silicon, the edge of the valence and conduction band is located at different points in momentum,  $k$  space. An electronic transition (by optical excitation) between them usually requires the assistance of a phonon to supply the additional momentum. Such a process is known as indirect transition and may occur in two ways [46]: (a) An electron in the valence band absorbs a photon and make a transition to an intermediate state in the conduction band of essentially the same wave vector [45]. Subsequently, a phonon from the lattice is absorbed and the electron transits to the conduction band (refer to Fig. 2.1). (b) The photon may excite an electron from a valence band state directly below the conduction band minimum, with the hole being transferred to the valence band maximum by phonon absorption. The final state is the same in both cases [46].



**Figure 2.1** Schematic band diagram of an indirect band gap material. The heavy arrows symbolize (a) indirect and (b) direct transition [45].



Upon relaxation from a higher energy state in the conduction band, an electron transits back to the valence band and causes a multi-phonon cascade to be emitted in the process [46]. According to the thermal model, the phonon emission process results in the transfer of energy to the lattice and raises its temperature [43, 44]. It should be noted that direct transitions are also possible in indirect band gap materials [45], provided that the photon energy is sufficiently high [47].

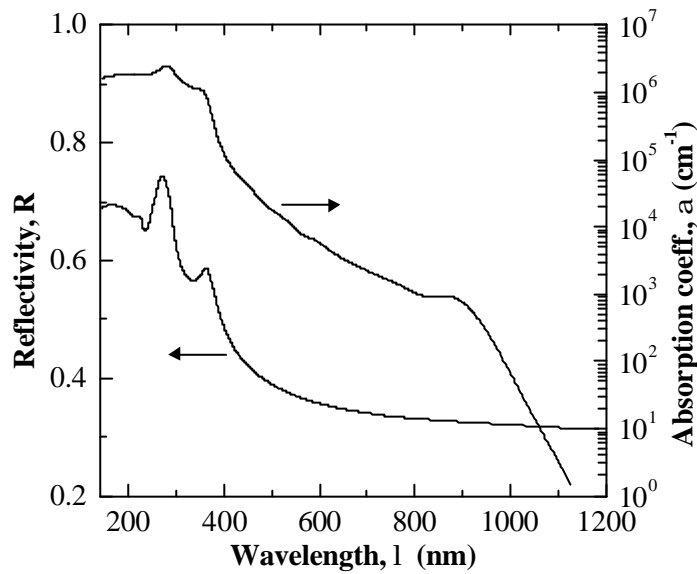
In general, since optical wavelengths,  $\lambda$  are considered large compared to atomic distances, the response of a homogenous material to the light wave can be described in terms of averaged macroscopic quantities such as the complex refractive index,  $m = n + ik$  [44, 45]. The real part  $n$  (refractive index) gives the ratio of the phase velocities in vacuum and in the material, and the imaginary part  $k$  (also known as the extinction coefficient) describes the damping of the light wave. A useful measure of the thickness required for the occurrence of significant attenuation of the incident radiation is the optical absorption length,  $\alpha^{-1}$  where  $\alpha$  is the absorption coefficient of the material. For normal beam incidence, the reflectivity,  $R$  and  $\alpha$  are related to  $n$  and  $k$  by [44, 45]:

$$R = \frac{(n-1)^2 + k^2}{(n+1)^2 + k^2} \quad (2.1)$$

$$a = \frac{4pk}{l} \quad (2.2)$$

Figure 2.2 shows the room temperature reflectivity and absorption coefficient of crystalline silicon (c-Si) as a function of wavelength. These are computed from the  $n$  and  $k$  values at various photon energies from the literature [48, 49]. It can be seen that for  $\lambda <$

360 nm,  $\alpha$  is in the order of  $10^6 \text{ cm}^{-1}$ , which is several orders of magnitude greater than that at  $\lambda > 540 \text{ nm}$ . Hence, it is desirable to use lasers with  $\lambda < 360 \text{ nm}$  for efficient heating of the substrate by optical absorption such that the laser energy density (fluence) needed to melt the Si surface is not extremely high and can be easily achieved in practice.



**Figure 2.2** Reflectivity and absorption coefficient of c-Si at room temperature.

### 2.4.3 Heat flow calculations

The transformation of electronic excitation into heat energy has been well established for the laser irradiation on metals and semiconductors. It is generally accepted that the absorbed light is instantaneously converted into heat that diffuses according to the conventional heat diffusion equation [43, 50]. For simplicity, it is assumed that the laser beam travels along the z-axis and the target composition is homogenous in this plane. After adding a source term that depends on space and time,  $t$  to the conventional heat equation, the one-dimensional heat transfer equation becomes:

$$\rho(T)C(T)\frac{\partial T(z,t)}{\partial t} = \frac{\partial}{\partial z}\left[K(T)\frac{\partial T(z,t)}{\partial z}\right] + \alpha(1-R)I_0(t)\exp(-\alpha z) \quad (2.3)$$

where  $T$  = temperature,  $\rho(T)$  = density,  $C(T)$  = specific heat capacity,  $K(T)$  = thermal conductivity,  $R$  = reflectivity of the substrate,  $\alpha$  = absorption coefficient of the substrate material, and  $I_0(t)$  = laser intensity upon reaching the substrate surface.

As shown in Eqn. (2.3), the interaction of lasers with materials is a complex phenomenon and can be affected by a variety of parameters. A lot of effort has been made to obtain numerical solutions to Eqn. (2.3) to determine the temperature distribution profiles and the melt kinetics during laser processing [43, 45]. The surface thermal field induced by pulsed laser irradiation of Si is not due to heat diffusion alone, but also depends on the penetration depth of the laser light [45, 51]. The laser heating process is affected by the absorption length,  $\alpha^{-1}$  and the heat diffusion length,  $L_T = \sqrt{2D_h t_p}$  where  $t_p$  is the laser pulse duration and  $D_h = \frac{K(T)}{\rho(T)C(T)}$  is the thermal diffusivity. There are two limiting cases, depending on whether  $L_T > \alpha^{-1}$  or  $L_T < \alpha^{-1}$ . For  $L_T > \alpha^{-1}$ , the laser pulse behaves like a surface source such that the average increase in the surface temperature as a function of time is given by [51]:

$$\Delta T(t) \approx \frac{(1-R)I_0(t)}{K} \sqrt{\frac{D_h t_p}{2}} \quad (2.4)$$

When  $L_T < \alpha^{-1}$ ,

$$\Delta T(t) \approx \frac{(1-R)I_0(t)a \exp(-az)t_p}{rC} \quad (2.5)$$

For a 248 nm laser irradiation on c-Si with  $t_p = 23$  ns at  $T = 300$  K,  $L_T \sim 2$   $\mu\text{m}$  and  $\alpha^{-1} \sim 5.6 \times 10^{-3}$   $\mu\text{m}$ . This indicates that the conduction of heat into the substrate after surface absorption plays an important role during LTP. The optical (at  $\lambda = 248$  nm) and thermophysical properties of c-Si and amorphous silicon (a-Si) are shown in Tables 2.1 and 2.2, respectively. These are obtained either directly from the literature or through a best-fit procedure of literature experimental data [48-57]. In order to simplify the heat-flow calculations, the solid-state reflectivity and absorption coefficient are typically assumed to be constant with temperature. The simplification for  $\alpha$  is justified because the absorption coefficient of Si at a wavelength of 248 nm is so high ( $\alpha > 10^6$   $\text{cm}^{-1}$ ) that it is believed that any changes in  $\alpha$  with temperature is insignificant [50]. It is noted that the absorption coefficient of silicon at  $\lambda = 308$  nm is within the same magnitude to that at  $\lambda = 248$  nm.

**Table 2.1** Optical (at  $\lambda = 248$  nm) and thermophysical properties of c-Si.

Properties	c-Si	Comments
Melting point, $T_c$ (K)	1683	From [48, 51, 52]
Boiling point (K)	3538	From [48]
Thermal conductivity, $K_c$ (W/cm K)	$1585/T^{1.229}$ (for $T < 1371$ K) $0.221$ ( $1371 < T < 1683$ K) $1.4$ ( $T > 1683$ K)	From [53, 54] and derived from [48, 55] From [53]
Volume heat capacity (J/cm <sup>3</sup> K)	$1.99 + 2.54 \times 10^{-4}T - 3.68 \times 10^{-4}/T^2$ (for $T < 1683$ K) $2.49$ ( $T > 1683$ K)	From [54] and derived from [48] Calculated from [56]
Reflectivity, R	$0.67$ ( $T < 1683$ K) $0.70$ ( $T > 1683$ K)	From [48, 54] and calculated from [49] From [45, 57]
Absorption coefficient, $\alpha$ (cm <sup>-1</sup> )	$1.81 \times 10^6$ ( $T < 1683$ K) $1.93 \times 10^6$ ( $T > 1683$ K)	From [54] and calculated from [48, 49] Calculated from [57]
Latent heat of melting, $L_c$ (J/cm <sup>3</sup> )	4192	From [53] and derived from [51, 52]

**Table 2.2** Optical (at  $\lambda = 248$  nm) and thermophysical properties of a-Si.

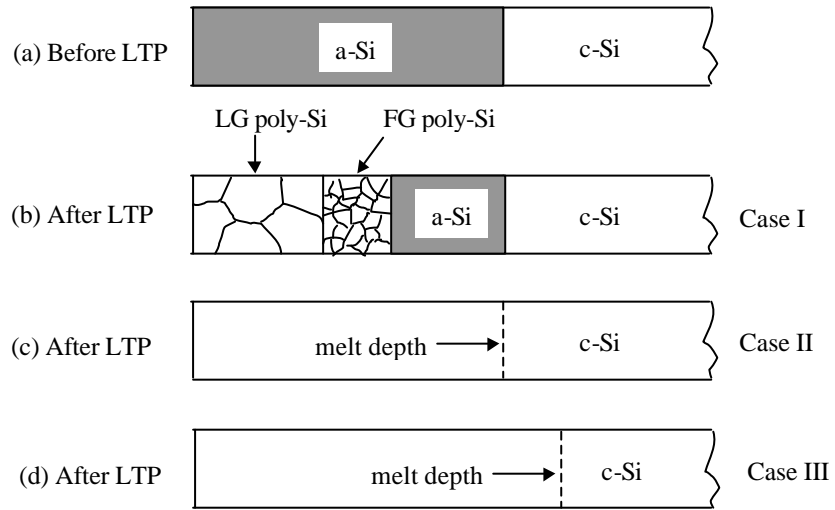
Properties	a-Si	Comments
Melting point, $T_a$ (K)	1420	From [52, 58, 59]. A range of values can be found.
Thermal conductivity, $K_a$ (W/cm K)	0.018 ( $T < 1420$ K)  1.4 ( $T > 1420$ K)	Average value from room temperature to melting point [51, 52].  From [53]
Volume heat capacity (J/cm <sup>3</sup> K)	$2.06 + 2.64 \times 10^{-4}T - 3.82 \times 10^4/T^2$ (for $T < 1420$ K)  2.49 ( $T > 1420$ K)	Assuming C and $\rho$ of a-Si is 10% greater and 6% less than c-Si respectively [51, 60].  Calculated from [56]
Reflectivity, R	0.55 ( $T < 1420$ K)  0.70 ( $T > 1420$ K)	Calculated from [49]  From [45, 57]
Absorption coefficient, $\alpha$ (cm <sup>-1</sup> )	$1.40 \times 10^6$ ( $T < 1420$ K)  $1.93 \times 10^6$ ( $T > 1420$ K)	Calculated from [49]  Calculated from [57]
Latent heat of melting, $L_a$ (J/cm <sup>3</sup> )	3076	Derived from [51, 52]

One important property of a-Si is that it exists as a unique phase and melts at a discrete temperature that is  $225 \pm 50$  °C lower than the melting point of crystalline Si [58, 59, 61]. This is due to the fact that a-Si is in a higher free energy state compared to c-Si and that the transformation from the amorphous to liquid state is a first-order phase transition [58, 62]. It was further suggested that this transition is possible because it involves a change in bonding from the covalent, amorphous phase with four-fold coordination to the metallic

liquid phase with (11 to 12)- fold coordination [58]. It should be recognized that this kind of phase transition will only occur during very rapid heating conditions, otherwise the amorphous phase will recrystallize directly in the solid phase [50]. Another important property of a-Si is that its thermal conductivity ( $K_a$ ) in the solid state is very low, with an average value (from room temperature to melting point,  $T_a$ ) of 0.018 W/cm K. This value is between one and two orders of magnitude smaller than the temperature dependent ( $K_c$ ) of c-Si for temperatures below 1420 K [51, 52].

#### **2.4.4 Laser irradiation of an a-Si overlayer on c-Si**

Important insight into the kinetics and thermodynamics of the phase transformations involved in LTP has been obtained from earlier investigations on laser irradiation of a-Si [43, 59, 61-64]. In general, the structural changes induced by laser irradiation of an a-Si layer on c-Si can be characterized by three cases. Case I: the laser fluence,  $E_l$  is only slightly greater than the threshold fluence,  $E_{th}$  for melting a-Si. In this case, the primary melt (molten layer produced directly by laser irradiation) does not penetrate through the entire a-Si layer. Typically, large-grained (LG) poly-Si will be formed at the near surface region followed by fine-grained (FG) poly-Si in the underlying region [Fig. 2.3 (b)]. The fraction of the LG region will increase at the expense of FG region with increasing fluence - a result of explosive crystallization [50, 59]. Explosive crystallization is a complex solidification process whereby the decay of the amorphous phase is accelerated by the feedback of the latent heat that is released during crystallization. At low energy densities where the laser does not melt the entire amorphous layer, the liquid Si (l-Si) will solidify as poly-Si and releases latent heat in the process [50, 59].



**Figure 2.3** Illustration of the structural changes induced by laser irradiation of an a-Si overlayer on c-Si.

Under this condition, previously unmelted a-Si that is adjacent to the newly crystallized phase gets heated to a temperature greater than  $T_a$  and begins to melt. This new liquid, however, is severely undercooled and will recrystallize almost immediately, releasing more latent heat that drives the melt even deeper into the a-Si layer. Thus, a propagating buried liquid layer (secondary melt) is formed and the process becomes self-sustaining [63, 64]. The secondary melt is finally quenched by either conduction of heat away from the melt interface or by reaching the a/c interface [61]. During the establishment of the secondary melt, the primary melt continues to solidify (as LG poly-Si) toward the surface. Thompson *et al.* [59] have observed that the depth at which poly-Si is formed is significantly greater than the maximum penetration depth of the primary melt, confirming the presence of a secondary melt.

Case II:  $E_l$  is just sufficient for the primary melt front to reach the a/c interface without melting the underlying c-Si substrate [Fig. 2.3 (c)]. Single-crystalline silicon is thus formed



via liquid phase epitaxy (LPE), using the underlying substrate as a template [43]. In theory, this regrowth process should produce crystals with reasonably good quality [50]; however it has been reported that residual defects such as microtwins and stacking faults exist in the crystallized layer [65]. Case III: at even higher energy densities, the primary melt front penetrates beyond the a/c interface [Fig. 2.3 (d)]. In this case, single-crystalline silicon is also formed upon solidification [43, 66]. The melting of a part of the crystalline substrate adjacent to the amorphous layer ensures the epitaxial growth of a nearly defect-free crystal with minimum “quenched-in” interstitials [67]. Such a crystallization process is possible since Si, unlike metals that usually slip when quenched at high cooling rates, has a high yield strength [62].

There exist a special case where a-Si can be formed directly following laser-induced melts (even on crystalline substrates) [68, 69]. This normally requires laser pulses of both short in duration (a few nanoseconds or less) and low fluence such that the cooling rates are extremely high and that the solidification velocities exceed a critical value [64, 69]. Amorphization occurs when the atoms at the liquid/solid interface do not have sufficient time to undergo the structural rearrangements necessary for epitaxial growth [43, 45].

#### **2.4.5 Dopant incorporation during rapid solidification**

The main advantage of LTP is that it offers the feasibility to form abrupt, highly activated and ultra-shallow junctions due to its extremely rapid heating and cooling rates in the nanosecond regime [13, 14, 70-73]. Thus, the thermal budget is minimized (near-zero) while providing proper dopant activation for the implanted species. Since the process does not reach thermal equilibrium, the concentration of electrically active dopants can actually

exceed the solid solubility limit [14, 71]. If the Si substrate is melted to a depth greater than the range of the implanted ion, the dopants will be incorporated substitutionally into the regrown epitaxial Si lattice. As a result, the sheet resistance decreases significantly [66, 73]. Several theories have been developed to explain the non-equilibrium diffusion and segregation of the dopant species at high solidification velocities. The most successful theory incorporates the idea of “solute trapping” to explain the increase in electrical activation [43]. Dopant incorporation into the lattice at high concentrations is proven to be a direct result of solute trapping during solidification [43, 74]. This means that if the time that is required to regrow one or more monolayer of atoms during solidification is significantly shorter than the residence time of the impurity at the interface, the dopant has a high probability of being incorporated into the growing solid [43].

Another factor that contributes to the high degree of dopant activation upon laser-melting is the near-unity interface segregation coefficient,  $k_i$  of the common dopants (e.g. B, P and As) during LTP [45, 71]. In the theory of crystal growth,  $k_i$  is defined as the ratio of the solute concentration in the growing solid to that in the liquid at the liquid/solid interface. If  $k_i = 1$ , the solute is entirely incorporated into the bulk solid and no segregation to the surface occurs. When  $k_i$  deviates from unity, segregation effects begin to manifest themselves by an accumulation of impurities in front of the advancing liquid/solid interface [43, 44]. Earlier studies on laser annealing have shown that for the common dopants, only a value of  $k_i \approx 1$  gives satisfactory fits of simulated dopant profiles with profiles obtained experimentally [43]. Since the equilibrium  $k_i$  values of these common dopants are lower than 1 (equilibrium  $k_i$  of B, P and As is 0.8, 0.35 and 0.3 respectively [43]), these observations provide evidence of the highly non-equilibrium crystallization process of LTP.

## 2.5 Alternative Approaches to Form Ultra-shallow Junctions

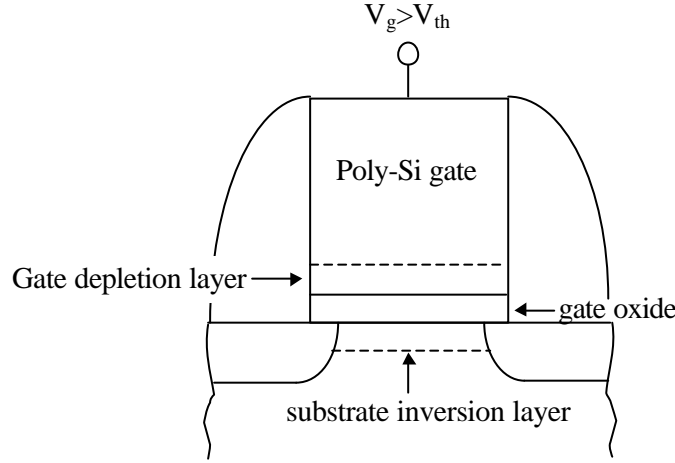
Researchers have suggested that ion implantation into an already formed silicide layer is a viable route for ultra-shallow formation since virtually all the ions stop within the silicide layer and do not penetrate into the Si. The junctions are formed by the out-diffusion of the implanted species into the Si substrate [19]. Thus, no implant damage is created and the leakage current in the junction is eliminated. This technique is also known as silicide as diffusion source (SADS) [75, 76]. Based on the literature, shallow junctions can also be fabricated using rapid thermal diffusion (RTD) of dopants. Usami *et al.* [77] have reported that such junctions have excellent electrical characteristics and are nearly defect-free. P-doped or B-doped films are first deposited onto the wafer by spin coating, followed by the thermal diffusion of the dopants in a furnace. After the diffusion of P or B, the spin-on films are removed by etching.

Plasma immersion ion implantation (PIII) is another technique to form ultra-shallow junctions [2]. This process is different from the conventional ion implantation because the implanter accelerating column, mass analyzing magnets and ion beam optics are all not used [2, 78]. The wafer is simply placed in a process chamber adjacent to the plasma ion source with a negative bias applied to it. The advantage of PIII includes the capability to implant high doses at very low energies with high throughput [78]. Gas immersion laser doping (GILD) is one alternative for shallow junction fabrication [79, 80]. The sample is usually immersed in a dopant gas ambient and doping occurs upon melting of the Si surface by a laser beam. Adsorbed dopant gas species pyrolyze and diffuse into the molten Si layer, and dopants are incorporated into electrically active sites upon epitaxial regrowth [80]. Recently, a “sub-melt” laser annealing process has been suggested for the formation of heavily doped

ultra-shallow junctions in boron-implanted silicon [81]. This technique uses laser irradiation to activate the boron atoms *without* melting the substrate, followed by a low temperature RTA to anneal the implantation-induced damages. In this way, boron diffusion is minimized and a reasonably low sheet resistance is attained.

## **2.6 Carrier Depletion in Polycrystalline Silicon Gates**

Modern CMOS processes generally use poly-Si as the gate material. One of the main reasons for this is that poly-Si allows the integration of “dual-doped” gates: p- and n-type poly-Si gate for p-MOSFET and n-MOSFET, respectively. This is important because both the p- and n-MOSFET can be maintained in the surface channel operation mode, which helps to improve short-channel immunity [16, 82, 83]. The dual-gate process also enables the fabrication of CMOS transistors with low and symmetric threshold voltages, which is required for low-power applications. One major challenge in advanced gate engineering is to have adequate dopant activation across the gate to minimize carrier depletion at the gate/gate oxide interface, while preventing the gate dopants (especially boron) from diffusing through the thin gate oxide into the channel during the subsequent gate or source/drain activation anneal [15-19]. The poly-depletion effect (PDE) for the dual-gate CMOS devices is ascribed to the fact that when the gate bias is applied to turn the transistor on, the electric field across the gate oxide not only inverts the substrate but also depletes the poly-Si at the gate/gate oxide interface (see Fig. 2.4).



**Figure 2.4** Schematic showing the components of the total gate capacitance.

The depletion layer capacitance effectively increases the electrical thickness of the gate dielectric by reducing the overall capacitance of the gate stack and results in drive current degradation [84, 85]. This is represented in Eqn. (2.6), considering that the total gate capacitance,  $C_{total}$  consists of the oxide capacitance,  $C_{ox}$  in series with the substrate capacitance,  $C_{sub}$ , and the gate electrode capacitance,  $C_{gate}$  [84]:

$$\frac{1}{C_{total}} = \frac{1}{C_{ox}} + \frac{1}{C_{sub}} + \frac{1}{C_{gate}} \quad (2.6)$$

The poly-depletion problem is exacerbated when the depletion thickness becomes a significant fraction of the gate oxide thickness, e. g., for sub-0.1  $\mu\text{m}$  devices with gate dielectric thickness less than 2 nm [16, 82]. For process simplicity, the gates are usually doped by the same ion implantation step that forms the source and drain regions. When combined with the typical low thermal budget S/D activation process, this doping method

does not yield very high active dopant concentrations at the critical gate/gate oxide interface, further leading to gate depletion problems. In order to reduce PDE, higher gate implant dosage or annealing temperature/duration is required, and boron penetration through the thin gate oxide is inevitably enhanced. Boron penetration will introduce negative fixed charges in the gate dielectric and results in an increase in the charge trapping rate in the gate oxide and an increase in the interface state generation, thus degrading the gate oxide reliability [16, 85-87]. Boron diffusion through the gate dielectric can also cause threshold voltage ( $V_{th}$ ) shifts and  $V_{th}$  mismatch [87-89]. These will result in scattered transistor parameters and make the fabrication process less controllable.

Various techniques have been proposed to suppress boron penetration. Nitridation of the gate oxide (using different thermal cycles and/or annealing ambient) and the reduction of fluorine incorporation during gate doping are effective in reducing boron diffusion through the gate oxide [17, 18, 90, 91]. Implanting nitrogen into the gate and using crystallized a-Si gates are also effective in retarding boron penetration [92-94]. However, excessive dosage of  $N_2^+$  will increase PDE instead because nitrogen combines with boron to form a B-N complex and reduces the concentration of boron reaching the gate/gate oxide interface [92]. It was reported that larger poly-Si grains can be obtained using amorphous Si gates, thus decreasing the number of grain boundaries available for excessive boron diffusion [93, 94]. Fiory *et al.* [95] have demonstrated that spike annealing with an optimized thermal budget can be utilized for poly-Si gate activation with minimum boron penetration.

Recently, attention has also been focussed on the use of polycrystalline silicon-germanium (poly-SiGe) gates for high-performance CMOS devices [96-98]. Besides having good compatibility with standard CMOS processing and enhanced mobility by the

tuning of the gate work function, the main advantages of using poly-SiGe as a gate material are the low diffusivity and enhanced activation of boron atoms in poly-SiGe, thereby reducing boron penetration and improving carrier depletion in p-MOSFET. However, it is more difficult to activate arsenic atoms in poly-SiGe films and PDE for n-MOSFET increases. As a result, the performance of n-MOS devices is degraded with increasing germanium content in the poly-SiGe gates [97, 98]. Although metals are now being explored as new gate materials, issues on integration and transistor design still remain [99]. Therefore, novel technologies for gate activation are needed in conjunction with the fabrication of ultra-shallow junctions for sub-0.1  $\mu\text{m}$  CMOS technologies.

## **2.7 Summary**

In retrospect, the main challenge in ultra-shallow junction formation is to develop dopant activation technologies that can minimize the transient enhanced diffusion of boron during thermal annealing, without compromising the electrical activation. Another concern is the annealing of the implantation-induced crystal defects. It has also been shown that the carrier depletion at the critical poly-Si gate/gate oxide interface plays an important role in the transistor's performance. The above issues will be addressed in detail in the subsequent chapters.

## **CHAPTER 3**

### **EXPERIMENTAL**

#### **3.1 Introduction**

This chapter gives a description of the entire experimental setup and the sample preparation methods used in this project. In addition, the test methodologies and the simulation procedures employed in this work are included.

#### **3.2 Simulation Studies**

To model the experimental results, we use the simulation of laser interaction with materials (SLIM) program [100] to simulate the thermal effects of 248 nm laser beam interactions with silicon. Simulation of laser irradiation on c-Si was performed using single-layer SLIM, and for a-Si on c-Si, the two-layer SLIM algorithm was employed. The substrate was set at room temperature initially, and the energy distribution profile (with respect to time) of the laser beam was assumed to follow a Gaussian function with a full-width at half-maximum (FWHM) pulse duration of 23 ns. The parameters used for the simulations have been shown in Tables 2.1 and 2.2. Simulations of detailed implantation cascades were performed with the Monte Carlo simulator, transport of ions in matter (TRIM) [101] and the binary collision code implant simulator (IMSIL) [102]. Other simulation programs that were used will be discussed along with the text in the subsequent chapters.



### 3.3 Formation of Ultra-shallow Junctions

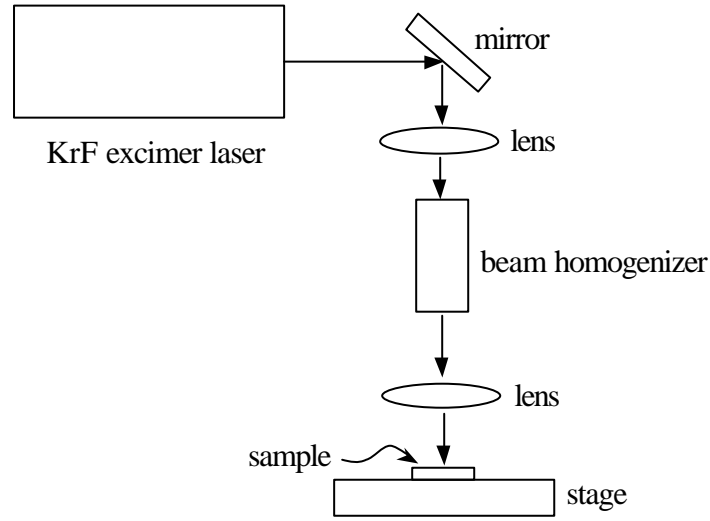
#### 3.3.1 Ion Implantation

The substrates used were 200 mm Czochralski-grown n-type (100) silicon wafers. Prior to B<sup>+</sup> implantation, some of the wafers were pre-amorphized using Ge<sup>+</sup> or Si<sup>+</sup> implantation. For the Ge<sup>+</sup> pre-amorphizing implantation (PAI) scheme, Ge<sup>+</sup> was implanted at 5 keV to a dose of 1x10<sup>15</sup>/cm<sup>2</sup>. For the Si<sup>+</sup> PAI scheme, Si<sup>+</sup> was implanted at 10 keV to a dose of 2x10<sup>15</sup>/cm<sup>2</sup> or 3x10<sup>15</sup>/cm<sup>2</sup>. Ultra-low energy <sup>11</sup>B<sup>+</sup> implantation was then performed at 0.6 or 1 keV to a dose of 1x10<sup>15</sup>/cm<sup>2</sup>. In most cases, B<sup>+</sup> implantation at 1 keV was employed.

#### 3.3.2 Dopant Activation

After the ion implantation of the dopant, the wafers were subjected to soak annealing, spike annealing, or by LTP. Soak anneals were performed with conventional RTA systems at various temperatures and times in N<sub>2</sub> ambient. The spike RTA (with soak times < 1 s) was carried out at a target temperature of 1050 °C with ramp-up rates of 75 or 300 °C/s. Laser thermal processing was performed with a 248 nm KrF excimer laser (Lambda Physik LEXtra 50) in a controlled environment. The native oxide was not deliberately etched since silicon dioxide (SiO<sub>2</sub>) is virtually transparent to 248 nm light [48], and it can also act as a protective capping layer during irradiation. The pulse duration and the repetition rate of the laser were approximately 23 ns and 1 Hz, respectively. After passing through an aperture, the laser beam was directed by a mirror/lens system until it was focussed by a quartz lens that was placed in parallel to the substrate. A schematic diagram of the apparatus setup for LTP is shown in Fig. 3.1. The degree of dopant activation was determined by measuring the

sheet resistance of the samples using the four-point probe method.



**Figure 3.1** A schematic diagram of the apparatus setup for laser thermal processing.

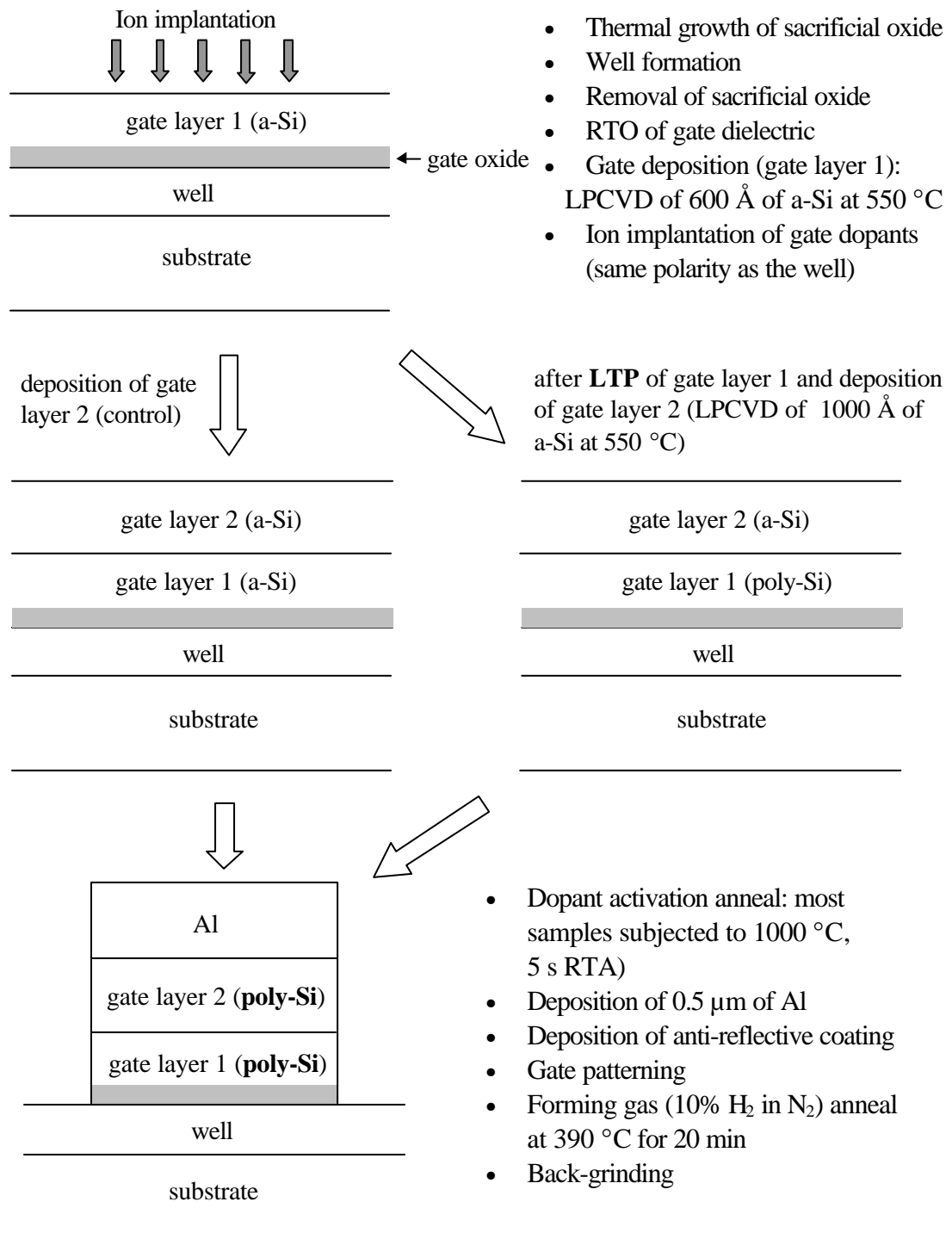
### 3.4 Gate Stacks With a TiN/Ti Capping Layer

The samples, which comprise TiN/Ti/poly-Si/SiO<sub>2</sub>/Si, were prepared using a conventional 0.25  $\mu\text{m}$  process flow. Firstly, 60 Å of SiO<sub>2</sub> was thermally grown on p-type (100) silicon substrates, followed by low pressure chemical vapor deposition (LPCVD) of a layer of 2550 Å poly-Si at 620 °C. BF<sub>2</sub><sup>+</sup> ions were then implanted at 30 keV to a dose of  $3 \times 10^{15}/\text{cm}^2$ . Some of the samples were subjected to RTA at 925 °C for 30 s to anneal the implantation-induced damage. On these samples, a metal capping layer consisting of 400 Å of titanium (Ti) and 250 Å of titanium nitride (TiN) were sputter deposited following a dilute hydrofluoric acid etch to remove any native oxide on the poly-Si. All samples were irradiated with a 248 nm KrF laser (single pulse). After laser irradiation, the samples capped with the TiN/Ti films were etched in a solution containing 1:1:5 NH<sub>4</sub>OH:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O at 60 °C to remove any unreacted metal.

### 3.5 Advanced Gate Stacks/Capacitor Structures

MOS capacitor structures with single or dual-layer poly-Si gates were fabricated on p/p<sup>+</sup> or n/n<sup>+</sup> epitaxial (100) Si wafers. The schematic of the cross-sections of the gate stacks and the associated process flow are shown in Fig. 3.2. A standard multi-step boron or phosphorous ion implantation (with a specific range of energies and dose) was performed through a sacrificial oxide for p-well and n-well formation, respectively. Immediately after the removal of the sacrificial oxide, 18 or 26 Å (measured by ellipsometry) of silicon oxynitride was grown at 1000 °C in a rapid thermal oxidation (RTO) chamber. The ambient used for the RTO was a NO-O<sub>2</sub> gas mixture. Following this, 600 Å of undoped a-Si (gate layer 1) was deposited at 550 °C by LPCVD. As the melting point of a-Si is ~250 °C lower than that of c-Si, a fluence window can be created such that the a-Si gate can be melted without melting the Si substrate underlying the gate oxide. Another purpose of using a-Si gates is to prevent uncontrolled dopant (especially boron) channeling in the gate (or even through the gate oxide) during ion implantation [103].

After the deposition of gate layer 1, B<sup>+</sup> (at 3 keV, 7° tilt, dose of 3.5x10<sup>15</sup>/cm<sup>2</sup>) or As<sup>+</sup> (at 15 keV, 7° tilt, dose of 6x10<sup>15</sup>/cm<sup>2</sup>) ion implantation was performed to form p<sup>+</sup> or n<sup>+</sup>-gated capacitors, respectively (polarity of the gate is the same as that of the well). The wafers were separated into two groups: some wafers remained as-implanted, and some were irradiated using a XeCl excimer laser ( $\lambda = 308$  nm) with a pulse duration of ~24 ns. Single-pulsed LTP was performed on the first gate layer in a cleanroom environment with the laser beam homogenized over a 5x5 mm<sup>2</sup> spot and fluences calibrated against the melt threshold fluence of c-Si. These samples will later be referred to as the “single-layer” capacitors.



**Figure 3.2** Schematic diagrams of the cross-sections of the gate stacks and the associated process flow.

On some of the laser-processed wafers and on the as-implanted wafers, a layer of 1000 Å undoped a-Si (gate layer 2) was deposited at 550 °C by LPCVD after a standard cleaning procedure to remove any native oxide. These samples will later be referred to as the “dual -layer” poly-Si gated capacitors.

It should be noted that the second gate layer was not implanted in this work. The purpose of the additional a-Si deposition (gate layer 2) is to simulate a conventional CMOS process flow to ensure that the gate stack is thick enough to block the dopants during the subsequent deep S/D ion implantation. Another purpose is to reduce the extent of dopant diffusion to neighboring devices (via connected gates) that have gates of a different polarity [104]. Subsequently, RTA was carried out (for single-layer samples that did not receive the LTP and all the dual-layer samples) at various temperatures and times in N<sub>2</sub> ambient to activate the gate dopants or for further activation (for the laser-processed samples). Most of the samples (including the control samples) were rapid thermal annealed at 1000 °C for 5 s. Following the deposition of 0.5 µm of Al on poly-Si, the gate electrodes were patterned and etched. The wafers were then annealed in forming gas (10% H<sub>2</sub> in N<sub>2</sub>) at 390 °C for 20 min to minimize interface traps. Finally, all wafers were sent for back-grinding to facilitate electrical measurements.

Another set of blanket wafers was irradiated with the 308 nm XeCl excimer laser as well. During LTP, *in-situ* time-resolved reflectance (TRR) measurements were conducted to record the evolution of the surface reflectance of the irradiated surface using a 790 nm probe laser with sub-ns resolution. The transient surface reflectance (measured in V) is analogous to the reflectivity of the film stack at a particular instant. The probe laser was focused at an incident angle of ~27° (with respect to the surface normal) to a spot size <

100  $\mu\text{m}$  in diameter onto the center of the irradiated spot. The small probe size ensures that the reflectance is measured over a homogeneously irradiated region. The duration of laser-induced melts can be determined from the reflectance traces obtained [105].

### **3.6 Materials Characterization**

#### **3.6.1 Secondary ion mass spectrometry**

All dopant profiles in this work were analyzed by secondary ion mass spectrometry (SIMS) using a Cameca IMS 6f instrument with a high-resolution magnetic sector mass spectrometer. For positive SIMS analyses (positive secondary ion detection),  $\text{O}_2^+$  was used as the primary ion source. The primary beam current used was between 20 to 50 nA at a net impact energy of 1 to 5 keV (depending on samples). For negative SIMS analyses (negative secondary ion detection),  $\text{Cs}^+$  was used as the primary ion source. The primary beam current used was 12 nA at a net impact energy of 3 keV. The primary ions impinged upon the surface at an incident angle of  $\sim 56^\circ$  and  $\sim 24^\circ$  (with respect to the surface normal) for  $\text{O}_2^+$  and  $\text{Cs}^+$  source, respectively. The typical raster area is  $200 \times 200 \mu\text{m}^2$  or  $250 \times 250 \mu\text{m}^2$ . Secondary ions were collected from the central region (30  $\mu\text{m}$  in diameter) of the sputtered crater. A post-acceleration system is used to improve the yield of low-energy secondary ions. All sputtered crater depths were measured using a Tencor Alpha-Step 500 stylus profilometer.

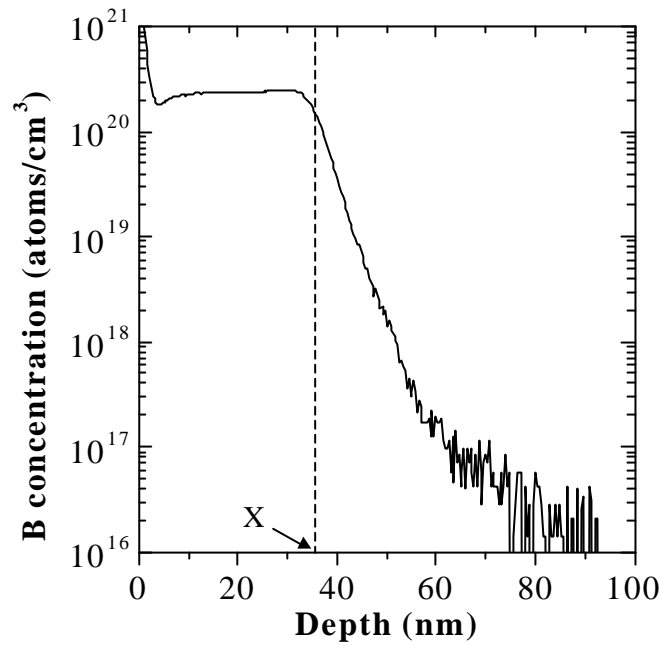
##### **3.6.1.1 Determination of junction depth (from SIMS) after LTP**

In general, when analyzing junctions that are formed by LTP (where the surface was melted by the laser), the junction depth is typically regarded as the maximum melt depth.

Ideally, since the impurity atoms can diffuse uniformly to the maximum melt depth during laser irradiation, it is expected that the samples would exhibit abrupt dopant profiles after laser melting. However, in reality, the dopant profiles that are obtained by SIMS usually have sloping tails and are not as abrupt as expected. This deviation from abrupt junction behavior can be attributed to 3 factors: (i) limited depth resolution of the SIMS instrument, (ii) spatial inhomogeneity of the laser beam, and (iii) non-abrupt amorphous/crystalline (a/c) interfaces for samples that were subjected to a pre-amorphizing implantation.

Depth resolution is often limited by ion-beam mixing and/or surface roughening during SIMS analysis [106]. When the primary ion species ( $O_2^+$  or  $Cs^+$ ) bombard the target surface, some of these ions are implanted into the target while others may be scattered back. Such collisions not only cause the target atoms to be sputtered out but can also push them deeper into the target. This effect, together with surface roughening can cause the profile to broaden, which can lead to inaccurate representation of the actual depth profiles. As for samples with PAI, the a/c interfaces will not be atomically sharp due to ion mixing, especially for  $Si^+$  PAI. Therefore, we believe that in general, the junctions formed by laser melting are still considered to be abrupt (unless otherwise stated). Now, we shall illustrate how  $\chi_j$  (after laser melting) is determined from the measured dopant profiles. Figure 3.3 is a typical SIMS profile that is obtained from a boron-implanted sample (with a n-type substrate) after laser melting. Assuming that the  $p^+/n$  junction has a rather abrupt interface, the location of this interface (i.e. the maximum melt depth) is approximated to be the position where the dopant concentration decreases by ~50% from its fairly constant value. This criterion is widely accepted in the SIMS community to define the interface between two films. Hence, the metallurgical junction depth of this sample is best represented by point X, which is ~36 nm

from the surface.



**Figure 3.3** Determination of the metallurgical junction depth (from SIMS) after laser melting.

### 3.6.2 Transmission electron microscopy

Conventional transmission electron microscopy (TEM) was employed to provide microstructural information and high-resolution transmission electron microscopy (HRTEM) was used to observe lattice images. Both plan-view and cross-sectional TEM (XTEM) specimens were thinned to electron transparency using standard grinding and polishing procedures, followed by low-energy ion milling. The samples were then examined under a Philips Tecnai F20 transmission electron microscope that was operating at an accelerating voltage of 200 kV.



### **3.6.3 Rutherford backscattering spectrometry**

Rutherford backscattering spectrometry (RBS) was performed using 2 MeV  $\text{He}^+$  ions generated from a van de Graaff accelerator. All measurements were done at normal incidence. The detector (for detecting the backscattered particles) was equipped with an Oxford microbeam data acquisition system and was located at a scattering angle of  $160^\circ$  (or an angle of approximately  $70^\circ$ ) with the sample surface. Channeling RBS was conducted by aligning the incident beam with the  $\langle 100 \rangle$  axis of virgin silicon.

### **3.6.4 Atomic force microscopy**

The morphologies of the as-implanted and annealed samples were analyzed by atomic force microscopy (AFM). Measurements were carried out in normal ambient, using the AFM (by Digital Instruments) in tapping mode in combination with tapping mode etched silicon (TESP) tips. The cantilever was oscillated near its resonant frequency as it scanned over the sample surface. With this method, high-resolution images can be obtained without inducing destructive frictional forces. Topographic images were acquired by scanning over an area of  $1 \times 1 \mu\text{m}^2$  with a resolution of  $512 \times 512$  data points. No further processing of the images was performed, except for the “flattening” procedure, which helps to eliminate artifacts that could be caused by the curvature of the piezo movements. The surfaces were characterized by measuring the dimensions of the surface features and calculating the average roughness ( $R_a$ ) and the root-mean-square roughness ( $R_{\text{rms}}$ ).

### 3.7 Electrical Characterization

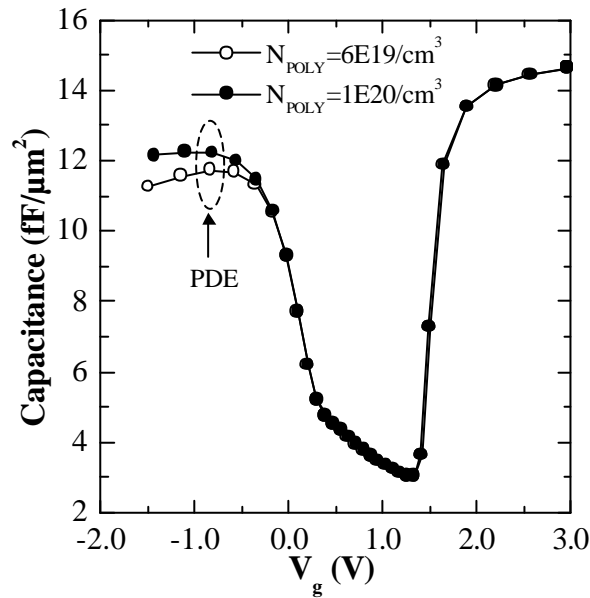
The capacitance-voltage (C-V) and current-voltage (I-V) characteristics were measured using a HP-4284A LCR meter at 1 MHz and a HP-4156B semiconductor parameter analyzer. Capacitance values were recorded as the gate bias was swept from substrate inversion to accumulation. Gate leakage currents were measured when the substrate was under accumulation. Constant voltage time-dependent dielectric breakdown (TDDB) studies were conducted at room temperature to examine the gate oxide reliability.

#### 3.7.1 Characterization of poly-depletion

In conventional MOS devices, the gate polarity is different to that of the substrate (or the well if there is a well implant). For instance, a p-MOS device typically has a  $p^+$ -poly-Si gate over a n-well. As mentioned in Chapter 2, the gate depletion effect occurs when the substrate is in inversion. Therefore, a MOSFET structure should be required to observe the gate-depletion effect from C-V plots. However, the fabrication of MOSFETs is a very tedious, time-consuming and costly process.

In this project, we employ an effective testing method using two-terminal capacitor structures with poly-Si gates that have the same polarity as the well/substrate. That is, a  $p^+$ -gated capacitor (PCAP) will have a  $p^+$ -poly-Si gate on a p-type well/substrate. When a positive gate bias is applied to the PCAP, the substrate is under depletion and the poly-Si gate is in accumulation. When the gate bias sweeps to a negative value, the substrate is in accumulation and the poly-Si gate is under depletion [108]. Therefore, the “accumulation” capacitance,  $C_{acc}$  is a measure of the degree of gate-depletion in PCAPs [109]. Similarly, the PDE in  $n^+$ -gated capacitors (on n-substrates) can be measured from  $C_{acc}$  values under

positive gate bias. These can be obtained easily using high frequency (HF) C-V measurements. In this case, it is not necessary to conduct low frequency or quasi-static C-V measurements to measure the gate-depletion effect (normally PDE is observed from the response of the minority carriers at low frequencies [108]). Figure 3.4 shows the simulated C-V plots of PCAP with different carrier concentrations at the poly-Si gate/gate oxide interface ( $N_{\text{POLY}}$ ), for the same gate oxide thickness [110]. PDE can be clearly observed in Fig. 3.4 when the substrate is under accumulation (higher  $N_{\text{POLY}}$  gives rise to less depletion and hence higher  $C_{\text{acc}}$ ).



**Figure 3.4** Simulated C-V plots of PCAP of different gate doping concentrations,  $N_{\text{POLY}}$  for the same gate oxide thickness.

## CHAPTER 4

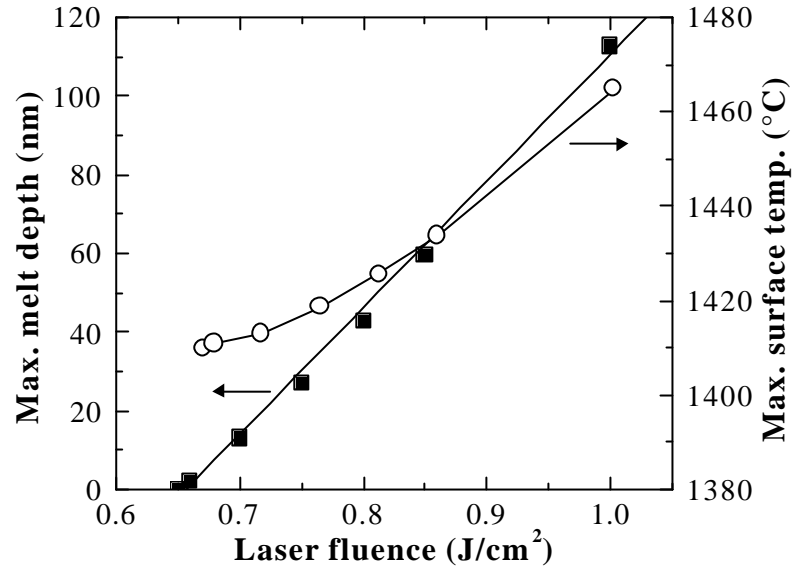
### SIMULATION OF LASER IRRADIATION ON SILICON

#### 4.1 Introduction

This chapter shows the results from the simulation of the laser interaction with silicon using the SLIM software. The results (e.g. melt depth vs. time, heating and cooling rates) provide some basic understanding of the LTP and the melt phenomenon. Further insights to the laser thermal process are provided when we use the two-layer SLIM program to simulate the melt characteristics of an a-Si overlayer on c-Si.

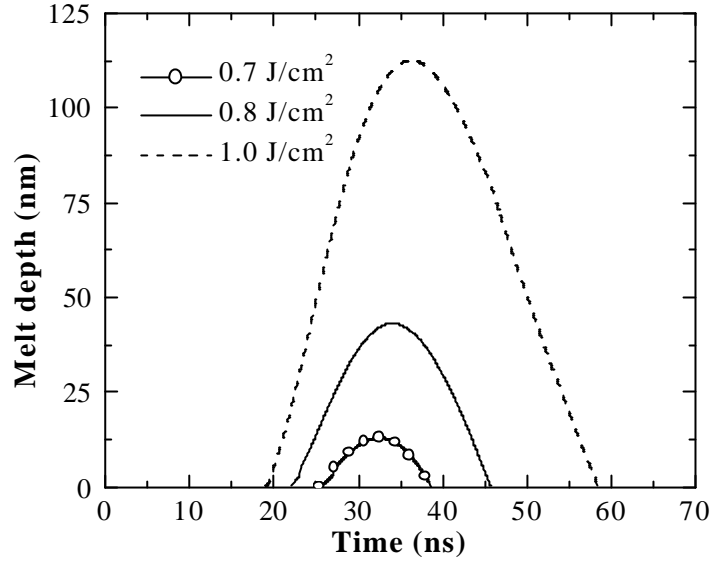
#### 4.2 Interaction of Laser with Crystalline Silicon

The correlation between laser fluence,  $E_f$ , maximum melt depth and maximum surface temperature for c-Si (obtained from SLIM) is plotted in Fig. 4.1. It is clear that the maximum melt depth varies almost linearly with fluence, which is in good agreement with the observations of Narayan *et al.* [53] in spite of the difference in laser wavelength used. The increase in the maximum melt depth with fluence is a direct consequence of an increase in thermal energy generated in the substrate by the input light wave. From Fig. 4.1, it can be seen that Si barely melts at  $0.66 \text{ J/cm}^2$ , with a maximum surface temperature of  $1411 \text{ }^\circ\text{C}$  (slightly higher than  $T_c$ ). This indicates that the threshold fluence for melting c-Si,  $E_{th}(\text{c-Si})$  is  $\sim 0.66 \text{ J/cm}^2$  for 248 nm laser irradiation.



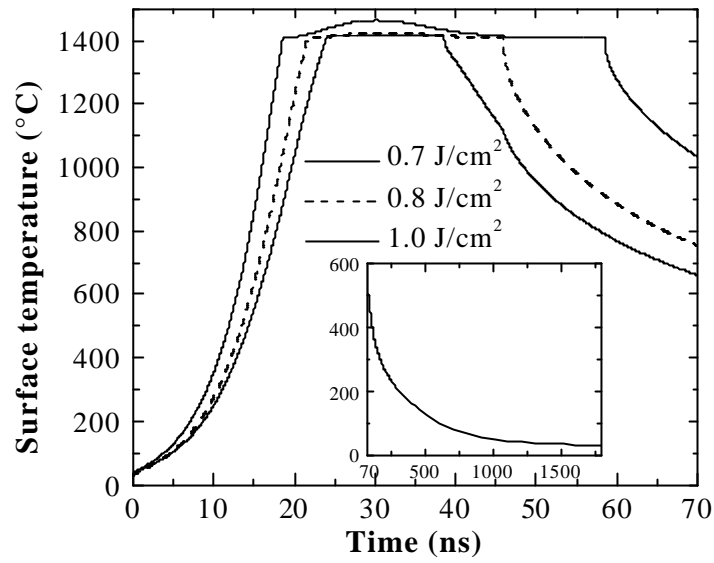
**Figure 4.1** Correlation between laser fluence, maximum melt depth and maximum surface temperature for c-Si (obtained from SLIM).

The simulated melt front profiles for c-Si during laser irradiation with various fluences are shown in Fig. 4.2. It can be observed that the melt depth increases with time for laser fluence greater than  $E_{\text{th}}(\text{c-Si})$ . After the maximum melt depth is attained, the melt front changes direction and the melt depth starts to decrease due to a reduction in local temperature with time. It is known that the instantaneous interface solidification velocity can be determined from the derivative of melt depth versus time plots similar to the plots shown in Fig. 4.2 [61]. For example, at 40 ns, the derivative of the curve representing  $E \sim 0.8 \text{ J}/\text{cm}^2$  is  $\sim 3.98 \text{ m/s}$ , indicating an extremely high solidification/regrowth velocity upon cooling.



**Figure 4.2** Simulated melt front profiles for c-Si during laser irradiation with various fluences.

From Fig. 4.3, it can be seen that initially, the surface temperature of Si increases as the duration of laser irradiation increases and remains relatively unchanged (for  $E_f \leq 0.8$  J/cm<sup>2</sup>). The surface temperature then declines continuously until the laser pulse is completed. These plots complement the melt depth against time plots in Fig. 4.2. For example, the surface temperature of Si (for a fluence of 0.8 J/cm<sup>2</sup>) is above  $T_c$  from 22 to 45 ns. These correspond to the times where the surface is molten in the initial and final stage of the melting (see Fig. 4.2). For  $E_f \sim 0.7$  J/cm<sup>2</sup>, the heating rate can be estimated by calculating the slope of the near-linear region from 14 to 20 ns. This approximates to be  $9.2 \times 10^{10}$  °C/s for a single laser pulse. It is important to note that such a heating rate can never be achieved by conventional RTA techniques. It can also be inferred from Fig. 4.3 that the heating rate increases with fluence, but the average cooling rate decreases with fluence; that is, the surface region remains heated for a longer duration at a higher fluence.



**Figure 4.3** Effect of laser fluence on the surface temperature of c-Si during irradiation. Inset figure shows that the surface temperature of Si (for a fluence of  $0.7 \text{ J/cm}^2$ ) falls to room temperature after  $\sim 1800 \text{ ns}$ .

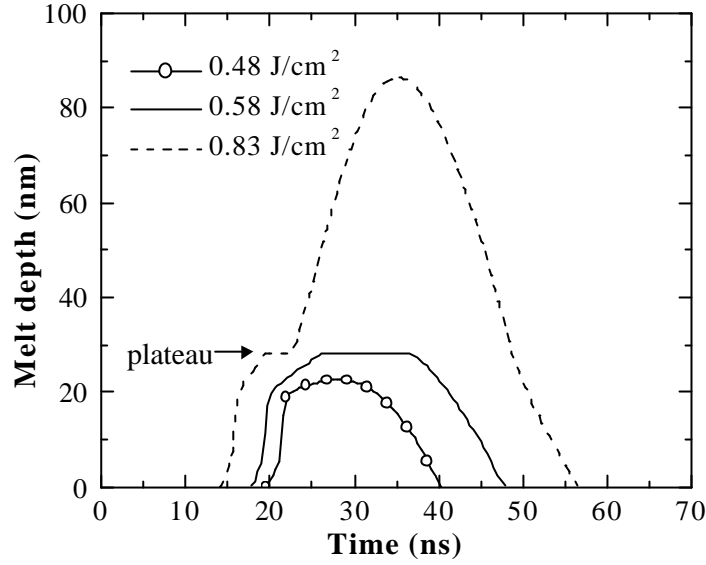
The inset of Fig. 4.3 also shows that for a laser fluence of  $0.7 \text{ J/cm}^2$ , the surface temperature of the Si sample falls to room temperature after  $\sim 1800 \text{ ns}$ , which is typical of a thermal cycle of a pulsed excimer laser. In practice, the highest frequency attainable for most excimer lasers is in the range of ten to a few hundred Hertz [41], indicating that the minimum time interval between 2 pulses is around  $1 \text{ ms}$ , which is much larger in magnitude than the time taken for a complete laser-induced thermal cycle. This suggests that for multiple laser pulses, the substrate will be cooled to room temperature after every pulse and hence there should not be any “memory” effects. That is to say, the pulse frequency/repetition rate of the laser beam has negligible effect on the thermal cycle or the heating rate. This is true unless there is a change in material property of the substrate.

### 4.3 Interaction of Laser with an a-Si Overlayer on c-Si

In this section, we perform simulation of laser interaction with an a-Si layer on c-Si using the two-layer SLIM program. This is based on a simplified heating model which presumes that the melt front only advances in *one* direction during melting or solidification. In addition, it does not take into account the complex effects of explosive crystallization (see Chapter 2 for details). In these simulations, the thickness of the amorphous layer was set to be 280 Å. Figure 4.4 shows the simulated melt front profiles of a sample with 280 Å of a-Si overlying c-Si during laser irradiation at various fluences. As expected, the maximum melt depth increases with fluence. It is also noticed that at a substantially high fluence of 0.83 J/cm<sup>2</sup>, the melt front completely penetrates through the amorphous layer into the crystalline substrate.

However, a plateau can be observed just before the melt front advances into c-Si. This agrees reasonably well with the experimental findings of Thompson *et al.* [59] where plateaus are also shown in their melt depth vs. time plots (derived from transient conductance measurements). The presence of the plateau can be interpreted as follows: during laser irradiation, melting begins at the a-Si surface when the temperature exceeds  $T_a$ . The melt front continues to propagate into the uniform a-Si layer at this reduced temperature until it encounters the a-Si/c-Si interface. Since the temperature of the melt is below  $T_c$ , the melt front must pause at this interface until sufficient energy is absorbed from the laser to increase the liquid temperature to  $T_c$  [61]. Once the temperature at the l-Si/c-Si interface exceeds  $T_c$  and the melt gains enough energy to overcome the latent heat of melting crystalline Si, the melt front advances into the underlying c-Si.





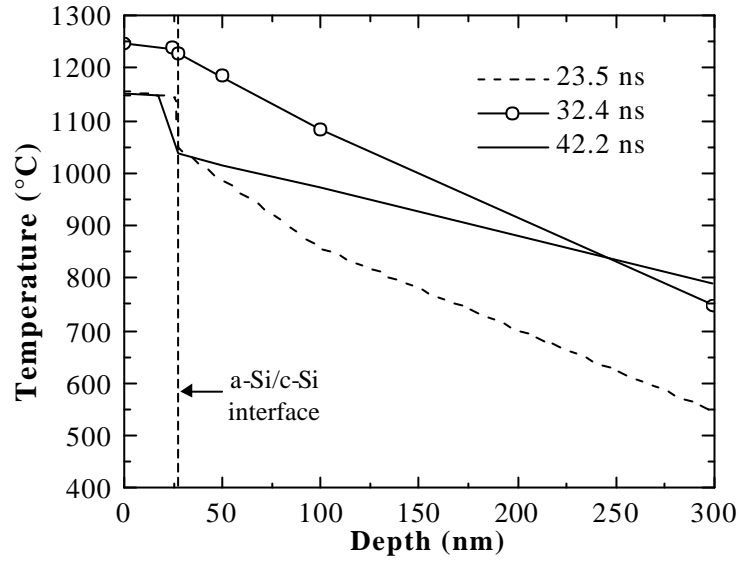
**Figure 4.4** Simulated melt front profiles for a 280 Å a-Si overlayer on c-Si during laser irradiation at various fluences.

On the other hand, at  $E_t \sim 0.58 \text{ J/cm}^2$ , the maximum melt depth is maintained at 280 Å (between 26.7 and 36.9 ns) during the laser irradiation. This shows that *theoretically*, it is possible to melt the entire a-Si layer without melting the underlying substrate (in this case the substrate is c-Si). This can be achieved by choosing a laser fluence such that the temperature of the amorphous layer is raised above its melting point but below the melting point of the underlying crystalline substrate. In this way, a process margin is created since there is a fluence window in which the melt depth does not increase with a further increase in laser fluence. Thus, it has been proposed that for the fabrication of ultra-shallow junctions using LTP, the final junction depth could be defined by the thickness of the amorphous layer (or the pre-amorphization depth). This is because the melt depth can be precisely controlled by the pre-amorphization depth [71].

It should be noted that the actual a-Si/c-Si samples used in this work are prepared by implanting c-Si with heavy ions such as  $\text{Si}^+$  or  $\text{Ge}^+$  to amorphize the surface. These pre-

amorphized samples have a lot of crystal defects near the range of the implanted ions and are structurally different from the ideal a-Si/c-Si samples where the a/c interface is clearly defined. Hence, there are some concerns on the formation of extended defects after laser-induced melting and recrystallization [65, 67]. These will be discussed in detail in Chapter 6. The above data also show that by having an amorphous silicon layer overlying c-Si, the threshold fluence needed to melt the Si substrate is reduced. Previously, a fluence of at least  $0.66 \text{ J/cm}^2$  is required to melt c-Si (Fig. 4.1), but now, a fluence of  $0.58 \text{ J/cm}^2$  is able to melt a layer of  $280 \text{ \AA}$  a-Si.

Figure 4.5 shows the simulated temperature distribution profiles in the a-Si/c-Si sample at different times during irradiation with a fluence of  $0.58 \text{ J/cm}^2$ . It can be seen that at  $23.52 \text{ ns}$ , the temperature within the amorphous layer is less than  $1147 \text{ }^\circ\text{C}$  ( $T_a$ ), indicating that the a-Si layer is not fully melted yet. Melting occurs progressively until the maximum melt depth (corresponding to the amorphous layer thickness of  $280 \text{ \AA}$ ) is reached, after which the resultant melt depth is governed by the temperature in the substrate. As can be seen from Fig. 4.5, the temperature at a depth of  $280 \text{ \AA}$  after  $32.4 \text{ ns}$  of the irradiation is  $\sim 1227 \text{ }^\circ\text{C}$ , which is greater than  $T_a$  but less than  $T_c$ . After  $42.2 \text{ ns}$  of the irradiation, the temperature profile is relatively lower than before (for depths  $< 2400 \text{ \AA}$ ), with less than  $180 \text{ \AA}$  of the substrate having a temperature greater than  $T_a$ . This results in a significant decrease in the melt depth.



**Figure 4.5** Simulated temperature distribution profiles in the a-Si/c-Si sample at different times during irradiation with a fluence of  $0.58 \text{ J/cm}^2$ .

#### 4.4 Summary

In this study, we have simulated the melt front and temperature distribution profiles for both crystalline and pre-amorphized Si during laser irradiation at 248 nm. It has been shown that the heating rate ( $>1 \times 10^{10} \text{ }^\circ\text{C/s}$ ) can never be achieved by conventional RTA techniques. The SLIM data show that theoretically, it is possible to melt the entire amorphous layer without melting the underlying crystalline substrate. This concept can be applied to the annealing of ultra-shallow  $p^+/n$  junctions where the final junction depth is controlled by the melt depth.

# CHAPTER 5

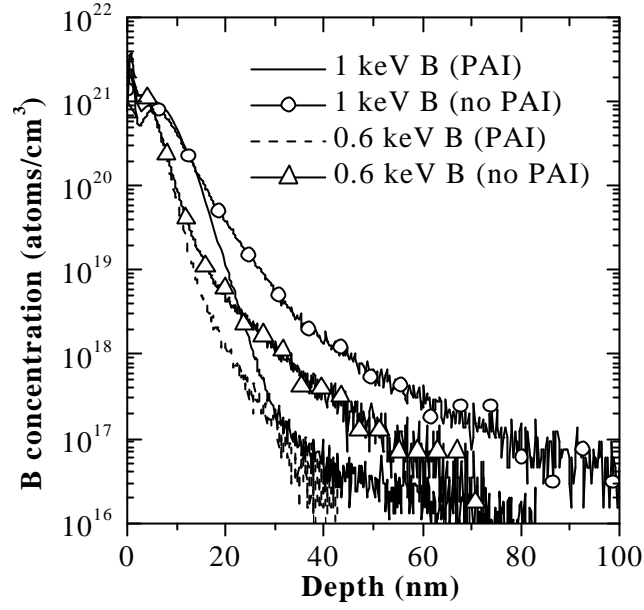
## FORMATION OF ULTRA-SHALLOW JUNCTIONS USING LASER THERMAL PROCESSING

### 5.1 Introduction

This chapter describes and compares the two most promising techniques that can be employed to form ultra-shallow  $p^+/n$  junctions. The techniques are spike rapid thermal annealing and laser thermal processing. For each technique, the discussion will include the analyses of the junction depth, the abruptness of the junction, and the sheet resistance of the boron-doped layer. The last part of this chapter shows the effect of laser irradiation on the modification of the surface morphology of boron-doped pre-amorphized silicon.

### 5.2 Effect of Surface Treatment on Channeling

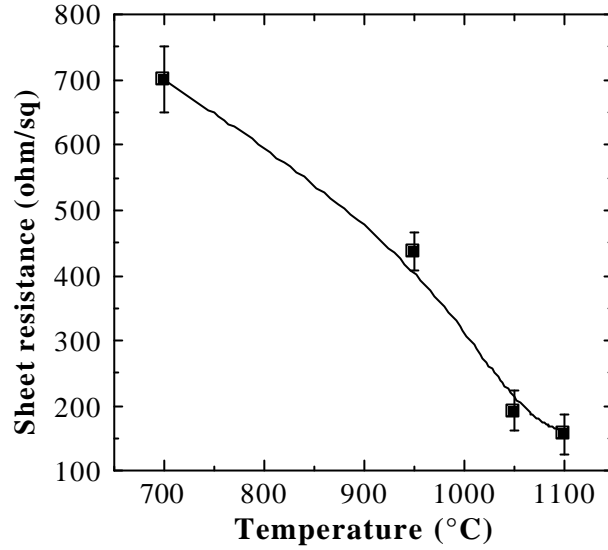
Figure 5.1 compares the as-implanted boron SIMS profiles in pre-amorphized (10 keV,  $2 \times 10^{15}/\text{cm}^2$   $\text{Si}^+$  PAI) and c-Si samples.  $\text{B}^+$  was implanted to a dose of  $1 \times 10^{15}/\text{cm}^2$  at 0.6 and 1 keV respectively. For both implant energies, it is observed that the junction depth (at a concentration of  $1 \times 10^{18} \text{ atoms}/\text{cm}^3$ ) of the pre-amorphized samples is less than that of the crystalline samples, indicating that channeling of the boron ions is largely ameliorated by the PAI. In addition, the junctions of the pre-amorphized samples are more abrupt as compared to the crystalline samples. This implies that the junctions formed after RTA of pre-amorphized samples will have steeper lateral abruptness, thus reducing short channel effects [2]. The above suggests that a PAI surface treatment is necessary for the formation of ultra-shallow  $p^+/n$  junctions (for  $\text{B}^+$  energies  $> 0.6 \text{ keV}$ ).



**Figure 5.1** Comparison of as-implanted boron SIMS profiles in pre-amorphized and c-Si samples.

### 5.3 Effect of RTA Temperature on Sheet Resistance

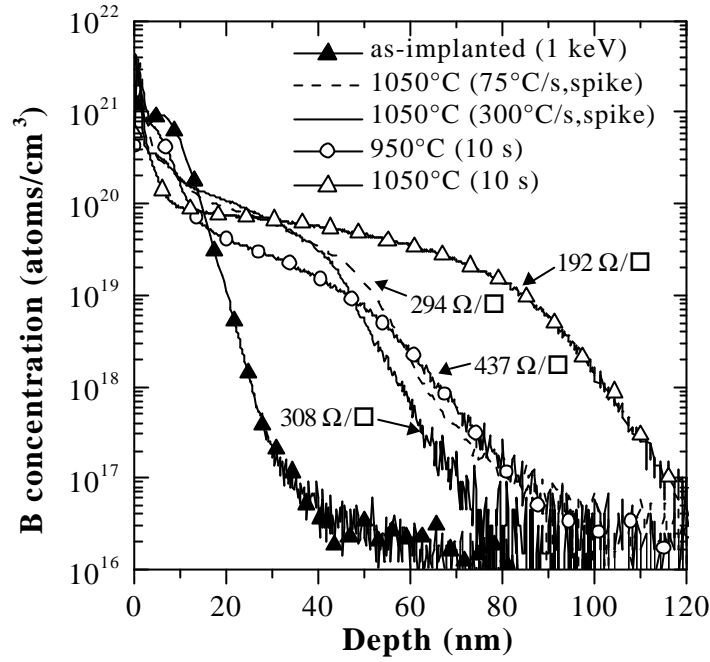
The effect of RTA temperature (at a soak time of 10 s) on the sheet resistance,  $R_s$  is shown in Fig. 5.2. The samples (pre-amorphized with 10 keV,  $2 \times 10^{15}/\text{cm}^2$   $\text{Si}^+$  PAI) were implanted with 1 keV boron to a dose of  $1 \times 10^{15}/\text{cm}^2$ . It can be seen from Fig. 5.2 that the sheet resistance decreases as the annealing temperature increases. This is attributed to 2 factors: (i) a greater degree of dopant activation and (ii) an increase in junction depth,  $x_j$  with an increase in annealing temperature. From Fig. 5.2, it can be inferred that in order to achieve a reasonably high degree of dopant activation (i.e. low  $R_s$ ), RTA should be performed at temperatures in the range of 1000 °C to 1100 °C.



**Figure 5.2** Effect of annealing temperature (at a soak time of 10 s) on sheet resistance. Samples were pre-amorphized with 10 keV,  $2 \times 10^{15}/\text{cm}^2$   $\text{Si}^+$  PAI.

#### 5.4 Comparison of Spike Anneal with Soak RTA

The boron SIMS profiles of the pre-amorphized samples (10 keV,  $2 \times 10^{15}/\text{cm}^2$   $\text{Si}^+$  PAI) before and after rapid thermal annealing under various conditions are depicted in Fig. 5.3. It is noticed that  $\chi_j$  of the conventional soak annealed sample (at 950 °C for 10 s) is comparable to that of the spike annealed sample with a ramp-up rate of 75 °C/s. However, the  $R_s$  of the spike annealed sample is considerably lower than that of the soak annealed sample (294  $\Omega/\square$  vs. 437  $\Omega/\square$ ). This is also true for the spike annealed sample with a ramp-up rate of 300 °C/s. The higher degree of dopant activation in the spike annealed samples is primarily due to the higher annealing temperature reached, despite having shallower junctions. Although a low sheet resistance was obtained for the sample that was soak annealed at 1050 °C for 10 s, the junction depth is substantially greater than that of the spike annealed samples. These suggest that conventional soak RTA is unsuitable for the formation of ultra-shallow junctions for advanced CMOS processing.



**Figure 5.3** Boron SIMS profiles of the pre-amorphized samples before and after RTA under various conditions.

For the spike annealed samples, it can be seen from Fig. 5.3 that there is a reduction in junction depth from  $\sim 630$  to  $\sim 580$  Å as the ramp-up rate increases from  $75$  °C/s to  $300$  °C/s. This reduction in  $\chi_j$  is attributed to a lower thermal budget (for the sample with a higher ramp-up rate) which reduces the total integrated time spent by the wafer at the high temperature ( $\sim 950$  °C to  $1050$  °C) regime [6]. Consequently, the intrinsic and enhanced diffusion of the boron atoms is decreased, and a shallower junction is thus formed. However, as shown in Fig. 5.3, the  $R_s$  of the spike annealed sample with a  $300$  °C/s ramp-up rate is slightly higher than that of the sample annealed with a ramp-up rate of  $75$  °C/s. This could be due to the reduced residence time at the high temperature regime associated with the higher ramp-up rate, resulting in a slightly lower degree of activation. The above results clearly demonstrate the advantages of using a high ramp-up rate spike RTA over

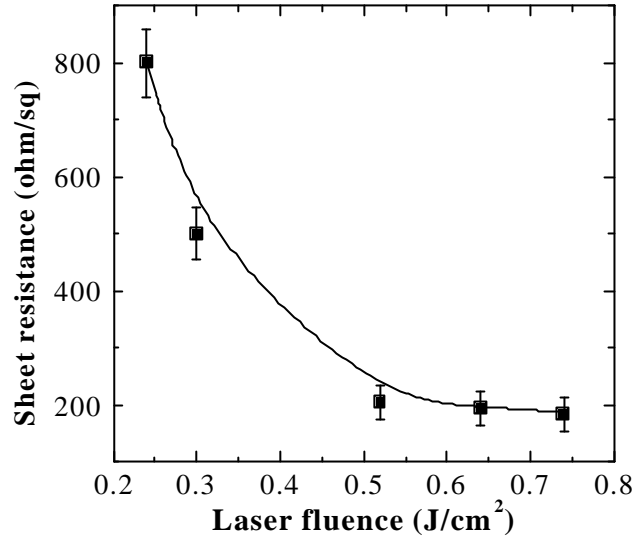
conventional soak anneal, i.e. spike RTA allows the use of higher annealing temperatures while maintaining a low thermal budget. There seems to be a compromise of the fraction of the activated dopants when the effective annealing time is decreased simply by increasing the ramp-up rate.

## 5.5 Ultra-shallow P<sup>+</sup>/n Junctions Formed By LTP

### 5.5.1 Effect of different fluence conditions

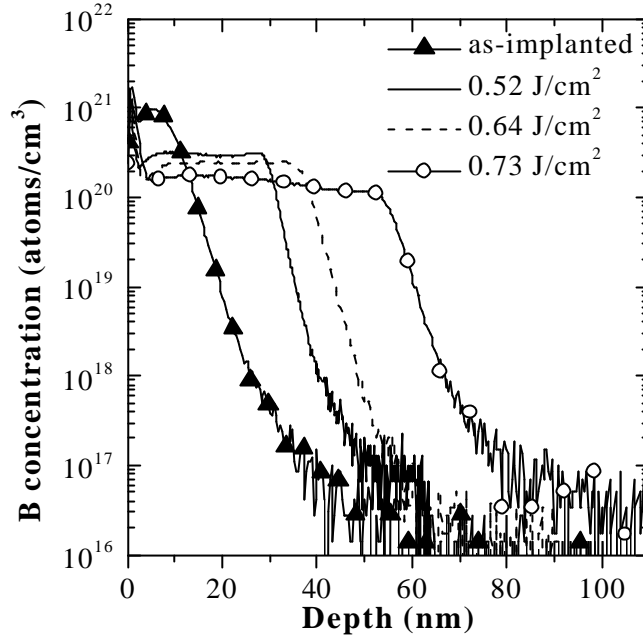
Figure 5.4 shows the sheet resistance of a 1 keV boron-implanted sample (pre-amorphized with 5 keV,  $1 \times 10^{15}/\text{cm}^2$  Ge<sup>+</sup>) as a function of laser fluence. The samples were subjected to a single-pulse irradiation from a 248 nm KrF laser. From Fig. 5.4, it is observed that the sheet resistance decreases as fluence increases, indicating an increase in dopant activation (as well as an increase in  $\chi_j$ ) with increasing fluence. However, the  $R_s$  remains virtually unchanged (at  $\sim 200 \, \Omega/\square$ ) when the fluence is increased to a value above  $0.52 \, \text{J}/\text{cm}^2$ . This implies that the dopants are almost fully activated at such high fluence levels. The high degree of dopant activation is attributed to the extremely high heating ( $>1 \times 10^{10} \, ^\circ\text{C}/\text{s}$ ) and quenching rates of the laser process. As a consequence, the dopants are engulfed in the substitutional sites during crystallization (solute trapping), with dopant concentrations that can exceed the equilibrium solid solubility limit in silicon.





**Figure 5.4** Sheet resistance of a 1 keV boron-implanted sample as a function of laser fluence.

The effect of single-pulsed laser irradiation on the redistribution of boron atoms is illustrated in Fig. 5.5. The most prominent feature in Fig. 5.5 is the presence of step-like dopant profiles following laser annealing. These profiles are in sharp contrast to those obtained after spike RTA, where the samples after spike RTA exhibit graded concentration profiles. Thus, the junctions after spike anneals do not meet the specifications of ITRS, which requires the lateral abruptness of the junctions to be at least 5 nm/decade for sub-0.1  $\mu\text{m}$  CMOS devices [1]. However, the  $\sim 4$  nm/decade lateral abruptness of the 0.52 J/cm<sup>2</sup> laser-annealed sample can satisfy the ITRS requirement. For advanced CMOS technologies, a nearly flat and abrupt profile is desired for the source/drain extension junctions to confine the electric field in the channel region under the gate and to reduce the sub-threshold leakage current. In order to achieve a reasonably high degree of dopant activation for the laser-annealed samples, the melt depth should be large enough to encompass the boron profile at  $1 \times 10^{18}$  atoms/cm<sup>3</sup>.



**Figure 5.5** SIMS depth profiles showing the effect of single-pulsed 248 nm laser irradiation on the redistribution of boron atoms.

The formation of the abrupt junction can be explained as follows: During laser irradiation, the heat generated by the laser pulse causes a thin layer of the Si surface to melt. Since the diffusivity of boron in the liquid phase ( $\sim 10^{-4} \text{ cm}^2/\text{s}$ ) is about eight orders of magnitude higher than that in the solid state ( $\sim 10^{-12} \text{ cm}^2/\text{s}$  at  $1000^\circ\text{C}$ ) [111], the boron atoms start to diffuse instantaneously and become nearly uniformly distributed within the molten Si. Diffusion stops exactly upon reaching the liquid/solid interface, thus forming an abrupt junction [14, 71]. Since the melt duration during LTP is typically in the tens of nanosecond regime, it is believed that diffusion of boron in the solid adjacent to the liquid/solid interface is negligible.

As shown in Fig. 5.5, the junction for the sample after laser annealing at  $0.52 \text{ J/cm}^2$  ( $\chi_j \sim 300 \text{ \AA}$ ) is shallower than that of the spike annealed samples (refer to Fig. 5.2) by at least  $280 \text{ \AA}$ . The determination of  $\chi_j$  after laser-induced melting has been discussed in Chapter 3.

Furthermore, the boron concentration (see the flat portion of the SIMS profile) in this sample is as high as  $3.4 \times 10^{20}$  atoms/cm<sup>3</sup>, a value that is greater than the equilibrium boron solid solubility ( $\sim 1.9 \times 10^{20}$  atoms/cm<sup>3</sup> at 1100 °C) in silicon [112]. This is manifested as an appreciable decrease in sheet resistance after LTP. For example, the  $R_s$  of the 0.52 J/cm<sup>2</sup> laser annealed sample ( $\sim 200 \text{ } \Omega/\square$ ) is considerably lower than that of the spike annealed samples ( $R_s \sim 294\text{-}308 \text{ } \Omega/\square$ ), despite a junction depth difference of at least 280 Å. The above results strongly indicate that due to the near-zero thermal budget of the laser thermal process, **single-pulsed** laser irradiation can produce abrupt, highly activated and ultra-shallow p<sup>+</sup>/n junctions for sub-0.1 μm CMOS technologies.

### 5.5.2 Lattice Strain

Previous work has suggested that the silicon lattice contracts when only boron is substitutionally incorporated into the lattice sites after pulsed laser annealing [43, 45]. This is due to the fact that the covalent radius of boron that replaces Si atoms in the lattice is substantially smaller than that of the silicon atom. This contraction will give rise to lattice strain with a magnitude that is proportional to the local boron concentration [45]. Hence, in order to minimize the strain induced by the boron atoms (especially after LTP), it is necessary to incorporate atoms that have a larger covalent radius than silicon along with boron to offset the strain (a good candidate would be Ge). Strain compensation can be explained in a quantitative way by using a “hard sphere” model [113]. Since each atom in the silicon lattice is situated within a tetrahedron comprising four neighbors, the distance between two neighboring atoms is referred to as the tetrahedral radius. The degree of strain,  $\epsilon$  (also known as the misfit factor) caused by the presence of an impurity atom in the lattice is thus

dependent on its tetrahedral radius,  $r_1$  and the tetrahedral radius of the silicon host atom,  $r_0$ . Therefore,  $\epsilon$  also gives an indication of the amount of dopants that can be incorporated into the substitutional sites [113] and is defined by:

$$\mathbf{e} = \frac{\Delta r_1}{r_0} = \left| \frac{r_1 - r_0}{r_0} \right| \quad (5.1)$$

When more than one type of dopant is present, it is proposed that we define another term called the effective strain,  $\epsilon_{\text{eff}}$ , which takes into account the strain induced by the individual dopant species.

$$\begin{aligned} \mathbf{e}_{\text{eff}} &= \frac{\Delta r_1}{r_0} + \frac{\Delta r_2}{r_0} + \dots \\ &= \left| \frac{1}{r_0} (\Delta r_1 + \Delta r_2 + \dots) \right| \end{aligned} \quad (5.2)$$

The tetrahedral radius and corresponding misfit factors [calculated using Eqn. (5.2)] of various atoms in silicon are compiled in Table 5.1. It can be seen that the misfit factor of a B-doped Si lattice is reduced from 0.254 to 0.22 by the addition of Ge atoms. In this case, since we have implanted the same dose ( $1 \times 10^{15}/\text{cm}^2$ ) of germanium and boron ions into silicon, it is reasonable to assume that there are sufficient Ge atoms to offset the strain induced by the boron atoms. The strain compensation effect that is provided by the larger Ge atoms is probably one of the factors that causes the enhanced dopant activation after laser annealing. It is noted that this is only an empirical concept that describes the physical

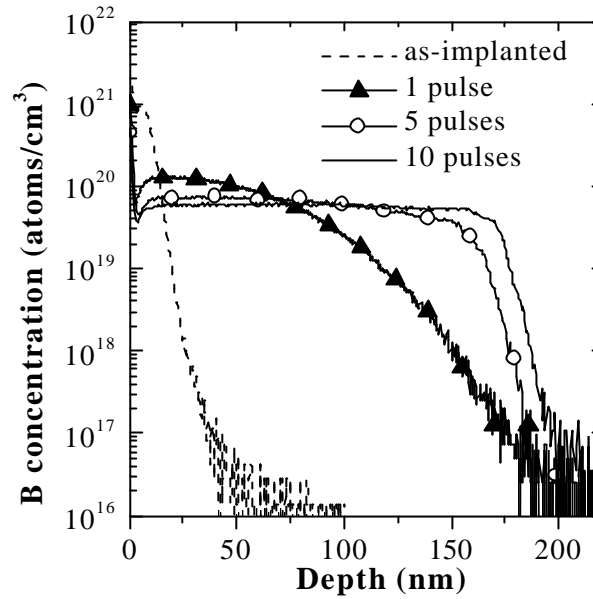
arrangement of impurity atoms in silicon and should not be taken as the sole factor in determining the electrical activity of the dopants [113].

**Table 5.1** Tetrahedral radius and misfit factors of various atoms in Si.

Atoms	Si	Ge	B	Ge + B
Tetrahedral radius (Å)	1.18	1.22	0.88	-
$\epsilon_{\text{eff}}$	0	0.034	0.254	0.22

### 5.5.3 Effect of multiple laser pulses at a high fluence

Figure 5.6 compares the boron concentration profiles after laser irradiation with successive pulses at a relatively high fluence of  $1.1 \text{ J/cm}^2$  for the 1 keV boron-implanted sample (pre-amorphized with 5 keV  $\text{Ge}^+$ ). The laser fluence employed ( $1.1 \text{ J/cm}^2$ ) is much higher than what is required to melt the pre-amorphized layer (which is  $\sim 116 \text{ Å}$  from TEM observations), rendering a substantial portion of the underlying Si substrate to be melted as well [100]. From Fig. 5.6, it can be seen that the boron SIMS profile after the first laser pulse does not resemble the typical “step-like” profile obtained following laser annealing. This result, coupled with the observation that the boron depth profile advances further into the Si substrate upon successive pulses, suggest that the boron atoms did not diffuse uniformly to the maximum attainable melt depth after the first pulse.

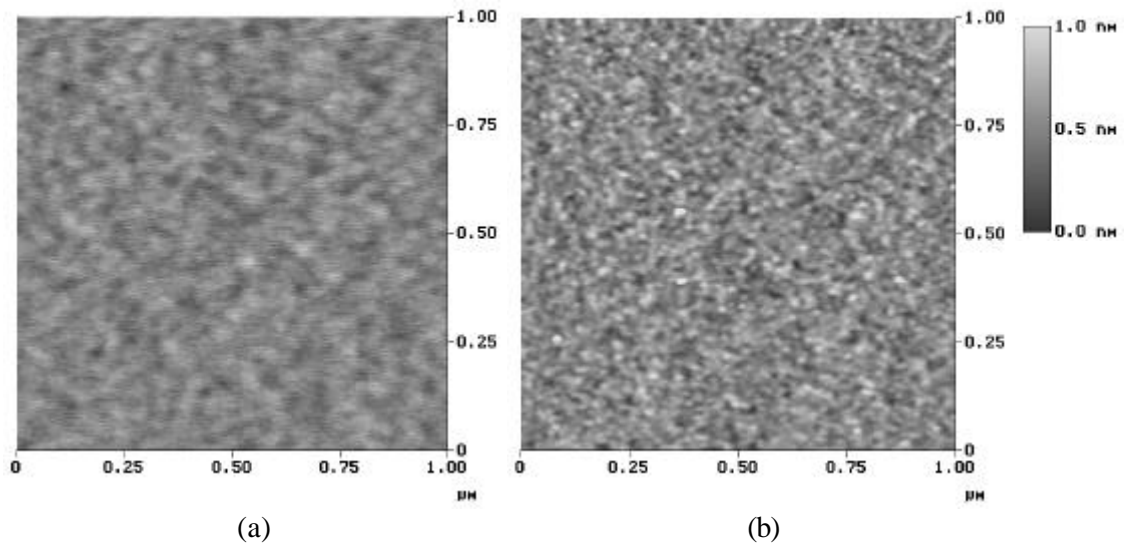


**Figure 5.6** Comparison of boron concentration profiles after LTP with successive pulses at  $1.1 \text{ J/cm}^2$ .

As can be seen from Fig. 5.6, the maximum melt depth is estimated to be  $\sim 1750 \text{ \AA}$  since the laser irradiation seems to have less effect on the dopant profile beyond 5 pulses. It is postulated that the boron atoms do not have sufficient time to diffuse up to this maximum melt depth when the first laser pulse was applied. This is probably due to two factors: Firstly, the melt front is propagating into the solid at a velocity that is much greater than the diffusive velocity of the dopant (even in molten Si). Secondly, when the primary melt front reaches the maximum melt depth, the solidification front is moving in the opposite direction at a rather high velocity, thus “preventing” the B atoms to diffuse further. However, the boron profile is able to advance into the silicon substrate as the number of pulse increases. This is attributed to the piling up of boron at the liquid/solid interface after each preceding pulse. From Fig. 5.6, it is noticed that after 10 laser pulses, the “true” maximum melt depth has been reached, and the boron atoms would have diffused uniformly up to this depth.

## 5.6 Modification of Surface Morphology by LTP

Figures 5.7(a) and (b) show the top-view AFM images of an as-implanted boron sample (pre-amorphized with 5 keV  $\text{Ge}^+$ ) and a sample after a 1050 °C, 10 s soak RTA, respectively. For the as-implanted sample, it is noticed that the surface is almost featureless, despite using a vertical scale of 1 nm (note that Figs. 5.7(a) and (b) share the same scale bar). This shows that the  $\text{Ge}^+$  PAI has negligible effects on the surface morphology of crystalline (100) silicon. From Fig. 5.7(b), it can be seen that the surface features become more defined after rapid thermal annealing at 1050 °C.



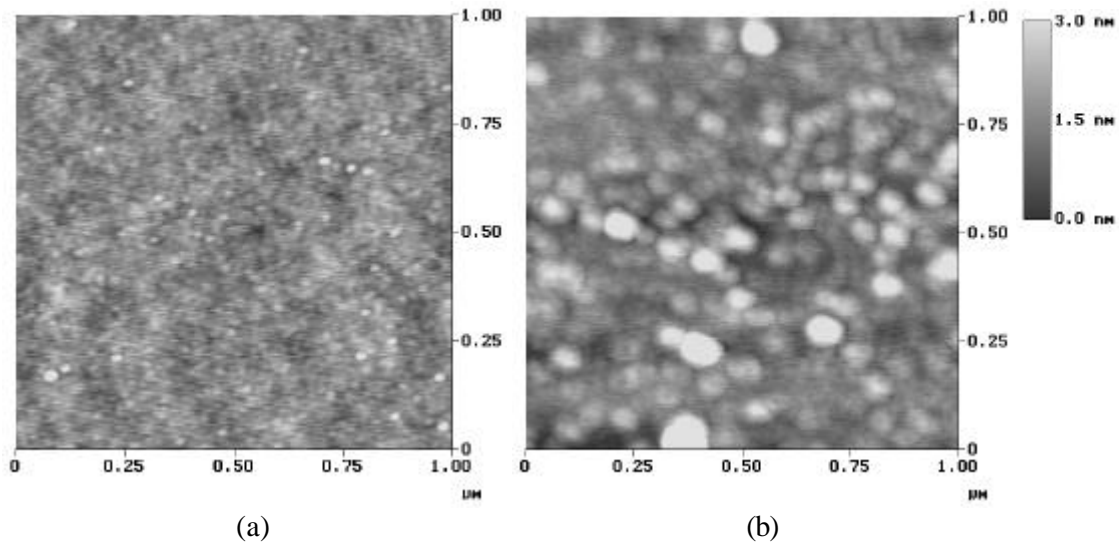
**Figure 5.7** Top-view AFM images of a (a) as-implanted sample (pre-amorphized silicon) and (b) sample after RTA.

Similar observations have been made by Mohadjeri *et al.* [114], although the roughening of their samples after annealing (at 1100 °C) is more drastic. These features may be attributed to the formation of silicon monoxide and silicon dioxide during annealing (assuming that there is residual oxygen remaining in the chamber). According to Mohadjeri *et al.* [114], at the initial stage of the annealing, small isolated islands of  $\text{SiO}_2$  are formed on

the silicon surface. As the partial pressure of oxygen decreases with annealing time, parts of the Si surface that are not covered by the SiO<sub>2</sub> clusters are etched by O<sub>2</sub> through the desorption of volatile SiO species from the surface. As a consequence, the silicon surface will experience localized etching, leading to the formation of the surface asperities observed. In order to reduce surface roughness caused by localized etching, it has been proposed that the oxygen partial pressure in the annealing ambient should be increased to above a certain value such that the continual lateral growth of a protective layer of SiO<sub>2</sub> is sustained [114]. The detailed mechanism of the competing effects of O<sub>2</sub> adsorption and SiO desorption under various oxygen partial pressures is beyond the scope of this work and will not be discussed further.

The effect of laser irradiation on surface morphology is shown in Fig. 5.8. The scale bar that is displayed is for Fig. 5.8(b). It is noted that the scale bar for Fig. 5.8(a) is the same as that for Fig. 5.7 and is not shown. For the sample after laser irradiation at 0.52 J/cm<sup>2</sup>, it is apparent that the general surface microstructure does not vary significantly from that of the rapid thermal annealed sample [Fig. 5.7(b)]. This clearly demonstrates that the laser anneal at 0.52 J/cm<sup>2</sup> does not cause any severe physical degradation of the silicon surface even though the melting of the pre-amorphized silicon during LTP causes some rearrangement of Si atoms at the surface. As can be seen from Fig. 5.8(b), when the sample was exposed to a higher laser fluence of 0.74 J/cm<sup>2</sup>, the resulting morphology is entirely different to that of the rapid thermal annealed sample and the 0.52 J/cm<sup>2</sup> laser-processed sample. An increase in laser fluence is analogous to a rise in surface temperature, thus resulting in more surface asperities.





**Figure 5.8** Effect of laser irradiation on surface morphology. AFM image of a sample (a) after LTP at  $0.52 \text{ J/cm}^2$  and (b) after LTP at  $0.74 \text{ J/cm}^2$ .

The surface roughness measurements of the as-implanted sample and the samples annealed under different conditions are computed in Table 5.2. It can be seen that the root-mean-square roughness,  $R_{\text{rms}}$  of the as-implanted sample has increased by  $\sim 49\%$  after RTA at  $1050^\circ\text{C}$ . The roughening phenomenon during RTA has been addressed above. This result is also in good agreement with the data of Edrei *et al.* [115], where it was found that the surface roughness of doped amorphous silicon increased after RTA at various temperatures.

Table 5.2 also shows that the surface roughness increases as the laser fluence increases, consistent with expectations. It is important to note that the  $R_{\text{rms}}$  of the laser-annealed sample at  $0.52 \text{ J/cm}^2$  ( $0.143 \text{ nm}$ ) is comparable to that of the sample after RTA ( $0.146 \text{ nm}$ ), confirming the similarity in the surface morphologies between these two samples. In terms of the surface morphology, it can be deduced that the optimized fluence for LTP is about  $0.52 \text{ J/cm}^2$ . Although an increase in the laser fluence can lead to a decrease

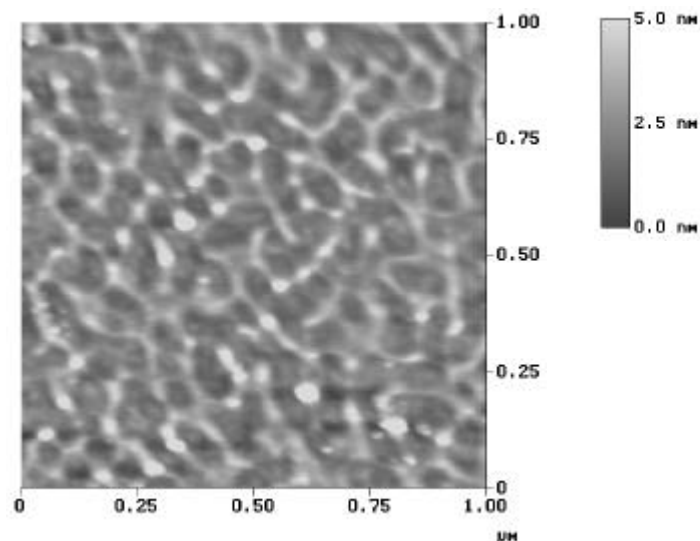
in sheet resistance (Fig. 5.4), it should be noted that this decrease in  $R_s$  is accompanied by an increase in junction depth and surface roughness, which is undesirable from the device's point of view.

**Table 5.2** Roughness measurements of the as-implanted sample and the samples annealed under different conditions.

Samples	$R_a$ (nm)	$R_{rms}$ (nm)
as-implanted (with $Ge^+$ PAI)	0.080	0.098
RTA (1050 °C, 10 s)	0.116	0.146
laser annealed (0.52 J/cm <sup>2</sup> )	0.113	0.143
laser annealed (0.62 J/cm <sup>2</sup> )	0.119	0.155
laser annealed (0.74 J/cm <sup>2</sup> )	0.462	0.687
laser annealed (1.1 J/cm <sup>2</sup> )	0.732	0.965

Figure 5.9 shows a top-view AFM image obtained from a sample after laser annealing at a high fluence of 1.1 J/cm<sup>2</sup>. It is noted that the vertical scale used in Fig. 5.9 is different from that used in Figs. 5.7 and 5.8, whereby a lighter shade represents a greater height in Fig. 5.9 as compared to Figs. 5.7 and 5.8. It appears from Fig. 5.9 that some “ridges” are formed about 55 nm apart with a pattern reminiscent of percolation theory. The formation of the ridges causes the surface roughness to increase by nearly one order of magnitude, with respect to the as-implanted sample (refer to Table 5.2).

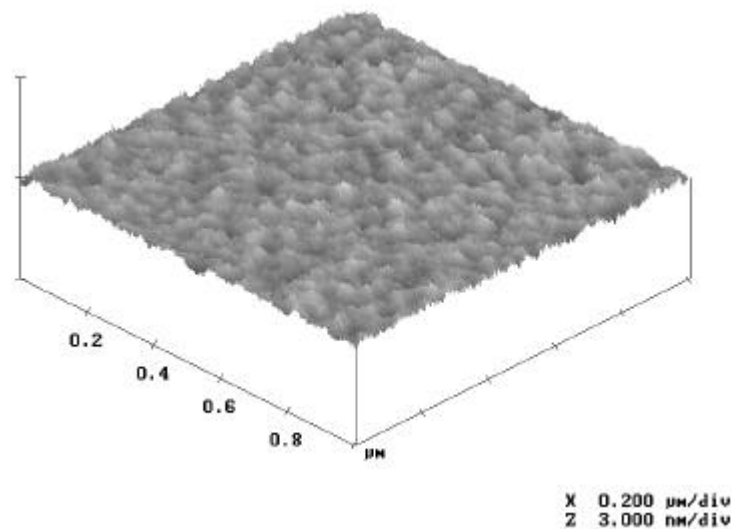
It can be proposed that when the silicon surface was exposed to laser irradiation at such a high fluence, the melting was so extensive that apparently there was not enough time to completely redistribute the material at the surface upon solidification. This results in a rough nanotexture that cannot be compromised in the fabrication of ultra-shallow junctions. The drastic increase in surface roughness after laser annealing at high fluences will have adverse effects on the electrical characteristics of semiconductor devices. For example, a significantly rough surface would result in a reduction of the effective junction depth in certain regions, giving rise to high leakage currents. Therefore, a low laser fluence should be used whenever possible in the annealing of silicon samples to avoid significant surface roughening.



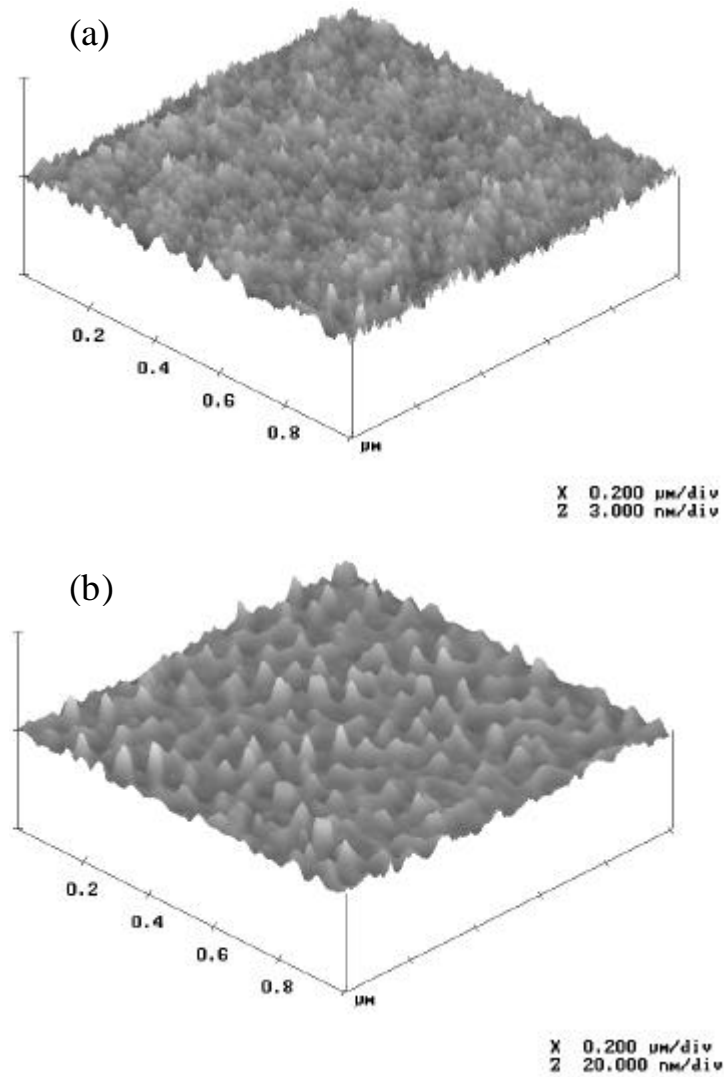
**Figure 5.9** Top-view AFM image obtained from a sample after laser annealing at a high fluence of  $1.1 \text{ J/cm}^2$ .

The three-dimensional AFM topographic plot of the as-implanted sample is depicted in Fig. 5.10. As mentioned above, the surface is almost featureless, with insignificant

undulations. Similarly, the three-dimensional AFM topographic plots of the samples after LTP at  $0.52 \text{ J/cm}^2$  and  $1.1 \text{ J/cm}^2$  are shown in Fig. 5.11. The evolution of the surface morphology of pre-amorphized silicon under different laser anneal conditions is clearly seen by comparing Fig. 5.10 and Fig. 5.11 (see Table 5.2 for corresponding roughness values). As can be seen from Fig. 5.11(b), the arrangement of the surface structures seems to follow a certain periodic order after laser annealing at a high fluence. During laser annealing, surface waves are generated on the silicon substrate beneath the native oxide. Due to the freezing of the surface waves in the silicon melt, ripple-like periodic structures are formed on the surface [116]. It has been postulated that the periodicity of the surface waves is governed by an empirical wave function [117].



**Figure 5.10** Three-dimensional AFM topographic plots of the as-implanted sample.



**Figure 5.11** Three-dimensional AFM topographic plots of (a) sample after LTP at 0.52 J/cm<sup>2</sup> and (b) sample after LTP at 1.1 J/cm<sup>2</sup>.

## 5.7 Summary

In this Chapter, we have shown that although spike RTA with high ramp-up rates can be used to form shallow junctions, the dopant activation is limited by the solid solubility and the resulting dopant profiles are usually graded. In contrast, single-pulsed LTP can produce abrupt, highly activated and ultra-shallow p<sup>+</sup>/n junctions. This is due to the near-zero thermal budget of the laser process. A low-fluence LTP should be used whenever possible in the annealing of silicon samples to avoid significant surface roughening.

# CHAPTER 6

## ANNEALING OF CRYSTAL DEFECTS BY LASER THERMAL PROCESSING

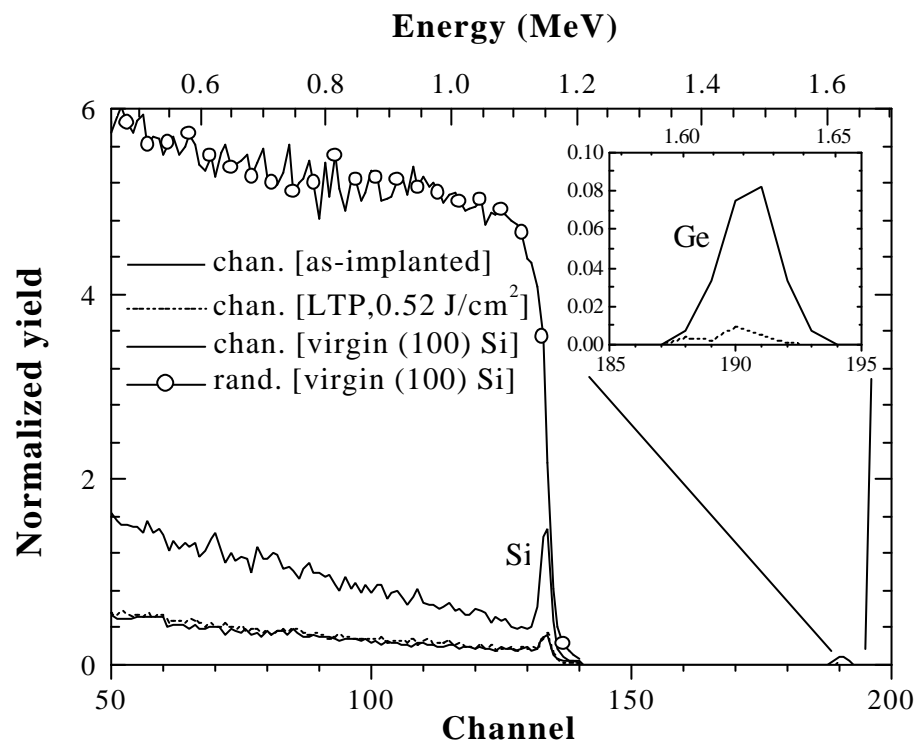
### 6.1 Introduction

As we have pointed out in Chapter 4, the LTP process typically involves the pre-amorphization of the silicon surface by implanting  $\text{Ge}^+$  or  $\text{Si}^+$ , followed by the melting of the amorphized regions without melting the underlying substrate. However, there are some concerns on the formation of extended defects after laser melting and recrystallization. In this chapter, we shall discuss the effect of LTP on the annealing of crystal defects. We also report the role of the excess interstitials in the EOR region in the transient enhanced diffusion of boron during a post-LTP RTA. A method based on melting beyond the amorphous layer during the initial LTP step was found to be effective in controlling boron TED during the post-LTP anneal.

### 6.2 RBS Studies of Si Samples With Ge PAI

Figure 6.1 displays the channeled RBS spectra of the 1 keV boron-implanted sample (pre-amorphized with 5 keV,  $1 \times 10^{15}/\text{cm}^2$   $\text{Ge}^+$ ) before and after laser annealing at 0.52 J/cm<sup>2</sup>. The random and channeled RBS spectra of a perfectly crystalline virgin (100) silicon substrate (reference sample) are also shown for reference. The x-axis is the channel number (with corresponding backscattered energy) and the y-axis is the normalized yield of the backscattered He ions. The random spectra of the  $\text{Ge}^+$  pre-amorphized sample before and after laser annealing are not shown because the backscattering yield of the silicon substrate

is virtually the same as that of the reference sample. Referring to Fig. 6.1, the intensity of the Si surface peak for the as-implanted sample is distinctively greater than that of the reference sample, indicating severe lattice disorder in the surface region of the as-implanted sample. It is believed that this damaged surface layer is completely amorphous, and is attributed to the  $\text{Ge}^+$  pre-amorphizing implantation. It can be further observed from Fig. 6.1 that the backscattering yield of the as-implanted sample is much higher than that of the virgin (100) silicon sample at depths below the damaged layer. This is because the passage of the incident beam through the amorphous surface layer greatly enhances the dechanneling rate of the  $\text{He}^+$  (relative to the case where there is no pre-amorphization), resulting in a rise in the backscattering yield.



**Figure 6.1** RBS spectra of a virgin (100) silicon substrate and the  $\text{Ge}^+$  pre-amorphized sample before and after laser annealing at  $0.52 \text{ J/cm}^2$ .

The thickness of the amorphous layer can be estimated by the following method. First of all, the ratio of  $\rho_v$  to  $R_m$  is determined, where  $\rho_v$  is the thermal vibrational amplitude and  $R_m$  is the shadow cone radius that represents scattering parameters. This ratio is calculated to be 1.61 using known parameters from the literature. From the “universal” curve obtained by Feldman *et al.* [118], a  $\rho_v/R_m$  value of 1.61 gives the number of silicon atoms/row that contributes to the silicon surface peak for the virgin silicon sample as approximately four. Since the intensity of the silicon peak for the as-implanted sample is  $\sim 4.74$  times higher than that of the virgin (100) silicon (Fig. 6.1), the surface peak for the as-implanted sample would correspond to  $\sim 4 \times 4.74 \approx 19$  silicon atoms/row. This value is then multiplied by the atomic spacing ( $5.43 \text{ \AA}$ ) of silicon along the  $\langle 100 \rangle$  rows. Therefore, the thickness of the amorphous layer is estimated to be  $\sim 18 \times 5.43 \approx 98 \text{ \AA}$  (see TEM results later).

It is evident from Fig. 6.1 that the intensity of the Si surface peak for the as-implanted sample is significantly reduced after laser annealing at  $0.52 \text{ J/cm}^2$ . In fact, the channeled RBS spectrum for this sample coincides with the spectrum for the virgin (100) silicon sample. There is striking evidence that the pre-amorphized layer has recrystallized to a single crystal with the same crystal orientation as (100) silicon after a single-pulsed LTP at  $0.52 \text{ J/cm}^2$ . Since solid-phase regrowth kinetics is too slow to explain this phenomenon [44], it is believed that regrowth of silicon has occurred via liquid phase epitaxy (LPE) using the underlying silicon substrate as a template [66]. Such an oriented crystallization mechanism can occur within the nanosecond regime of the laser irradiation because the velocity of the crystallization front is considerably high (in the order of a few m/s) [45]. During LPE, the dopants are also incorporated into the lattice sites of the regrown Si and become electrically active.



The extent of crystallization to a single crystal is normally measured by the minimum yield,  $\chi_{\min}$ , which is the ratio of the integral of the channeled spectrum to the integral of the random spectrum just after the trailing edge of the Si surface peak [45, 118]. In this study, the area under evaluation is between channel 120 and 130 and the calculated  $\chi_{\min}$  values are tabulated in Table 6.1.

**Table 6.1** Calculated  $\chi_{\min}$  values of the reference sample and the  $\text{Ge}^+$  pre-amorphized sample before and after LTP at  $0.52 \text{ J/cm}^2$ .

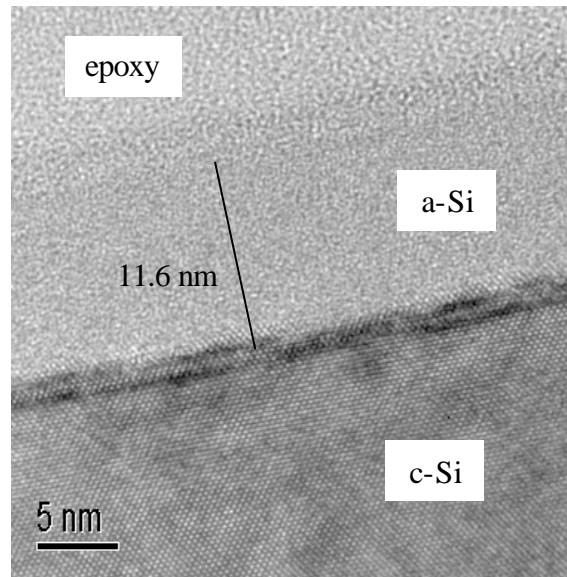
Samples	$C_{\min} (\%)$
as-implanted (with $\text{Ge}^+$ PAI)	9.22
after LTP at $0.52 \text{ J/cm}^2$	3.62
virgin (100) Si	3.52

From Table 6.1, it can be seen that the  $\chi_{\min}$  of the  $0.52 \text{ J/cm}^2$  laser annealed sample is comparable to that of virgin (100) silicon (within experimental errors), confirming that the amorphous layer has recrystallized to a single crystal with a structure similar to that of (100) silicon. An important feature to notice in Fig. 6.1 is the presence of a peak at a backscattering energy of  $\sim 1.62 \text{ MeV}$ . This peak is attributed to the backscattering of  $\text{He}^+$  from the heavier germanium atoms that were introduced into the sample during the PAI. The backscattering yield is low because the quantity of Ge atoms in the silicon matrix is rather small. An amplified view of the Ge surface peak is displayed in the inset of Fig. 6.1. It is observed that the intensity of this peak decreases drastically after LTP at  $0.52 \text{ J/cm}^2$ . The near-complete absence of the Ge surface peak provides further evidence that the LTP has

indeed completely removed the disorder in the crystal lattice, and practically all the implanted germanium atoms are located at substitutional positions in the Si lattice after epitaxial regrowth.

### **6.3 TEM Studies of Si Samples With Ge PAI**

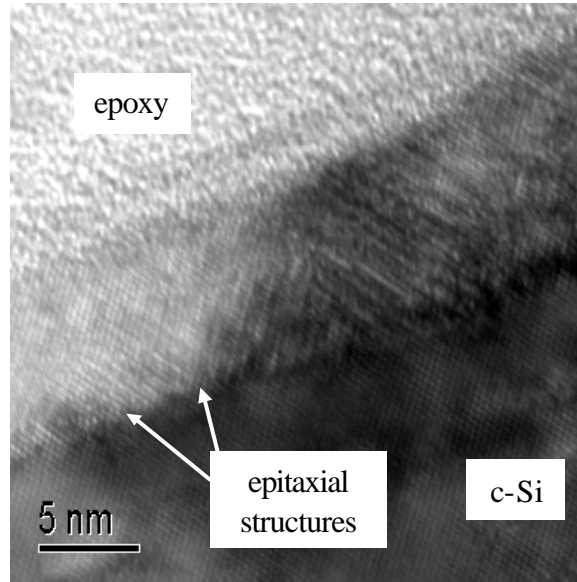
Figure 6.2 shows a cross-sectional transmission electron micrograph of the as-implanted sample (pre-amorphized with 5 keV Ge<sup>+</sup>). The surface has been bonded to an epoxy layer for TEM sample preparation purposes. Below this epoxy layer, an amorphous silicon layer of thickness  $\sim 116$  Å is distinguishable, although some residual crystalline structure is just resolved at the a/c interface. The dark band at the a/c interface may be associated with the crystal damage/strain field induced by the Ge<sup>+</sup> PAI. From Fig. 6.2, it is apparent that the amorphous layer is continuous, and it extends all the way to the surface. These results are in reasonable agreement with the channeled RBS data presented in Fig. 6.1, despite a slight discrepancy in the thickness of the pre-amorphization depth. This is because for RBS, the thickness of the amorphous layer was deduced from the intensity of the channeled surface peak. The accuracy of the result is therefore limited by several factors; mainly the unknown accuracy of the reference data used and the effects from the implanted Ge atoms that were neglected in the analysis.



**Figure 6.2** Cross-sectional transmission electron micrograph of the B<sup>+</sup> as-implanted sample, pre-amorphized with Ge<sup>+</sup> implantation.

Figure 6.3 shows a high-resolution transmission electron microscopy (HRTEM) image of a cross-section of the pre-amorphized sample that was irradiated at a laser fluence of 0.3 J/cm<sup>2</sup>. The presence of epitaxial structures that have grown from the crystalline substrate is clearly observed, indicating that the laser irradiation has transformed the amorphous surface layer into a single crystalline layer. However, this regrown layer contains a high density of microtwins and stacking faults, and the original a/c interface is still vaguely visible. The dark patches in the transmission electron micrograph could be attributed to the mass-thickness contrast during TEM analysis. Although Jones *et al.* [65] have observed similar residual defects in their laser-crystallized sample, they did not delineate the defects using HRTEM (probably because the PAI layer in their sample is much thicker-27 nm). The result strongly suggests that the pre-amorphized layer (and the crystal damage caused by the boron ion implantation) is not completely annealed by the low-fluence laser thermal process. Such junctions typically have high junction leakage current and are not acceptable for the

fabrication of advanced semiconductor devices [23].

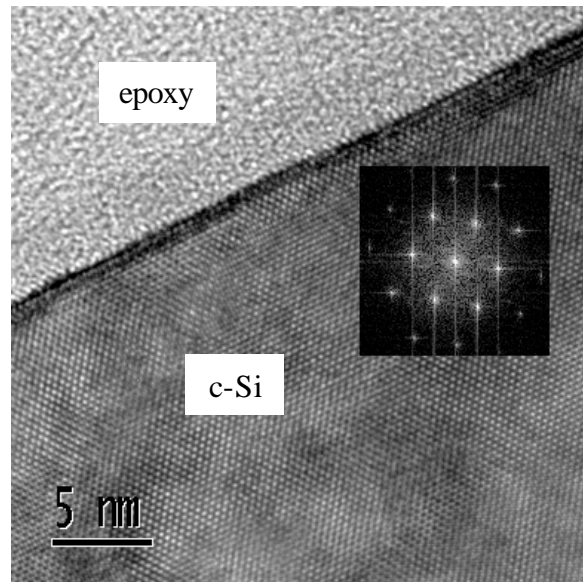


**Figure 6.3** High-resolution XTEM image of a sample that was not completely annealed by the  $0.3 \text{ J/cm}^2$  laser irradiation. It is observed that some epitaxial structures have grown from the crystalline substrate.

Based on previous studies [119, 120], it is found that the regrowth rate of silicon via laser-induced solid phase epitaxy (at temperatures close to  $T_a$ ) is  $\sim 8.7 \times 10^5 \text{ nm/s}$ . Hence, the minimum time required to grow a  $\sim 12 \text{ nm}$  epitaxial layer using SPE would be  $\sim 13.8 \times 10^{-6} \text{ s} \approx 14 \text{ } \mu\text{s}$ . This time scale is about three orders of magnitude greater than that of the laser thermal process (which is in tens of nanoseconds), indicating that the time available during the LTP is not sufficient to cause epitaxial growth of such considerable extent in the solid state. Therefore, the epitaxial growth must have involved mass transport in a liquid medium (in this case, the medium is liquid Si). We can thus envisage the scenario whereby the  $0.3 \text{ J/cm}^2$  laser irradiation melts the entire amorphous layer such that the primary melt reaches, but does not exceed the original a/c interface. Upon cooling, LPE occurs and results in the

growth of the epitaxial structures as shown in Fig. 6.3. The residual defects/disorder shown in Fig. 6.3 could be caused by the extremely high solidification velocity (but below the amorphization velocity), which is typical of a low fluence laser thermal process.

The lattice image of the as-implanted sample after laser annealing at  $0.52 \text{ J/cm}^2$  is depicted in Fig. 6.4. The TEM image illustrates essentially perfect recrystallization throughout the region of the originally pre-amorphized layer. There is virtually no secondary defect observed in the vicinity of the regrown crystal. These observations are in accordance with the laser-induced liquid phase epitaxial process, as reported earlier. It is believed that part of the underlying substrate contiguous to the amorphous layer was also melted (melt depth is  $\sim 300 \text{ \AA}$  from Fig. 5.5) in order to result in the virtually defect-free crystal.



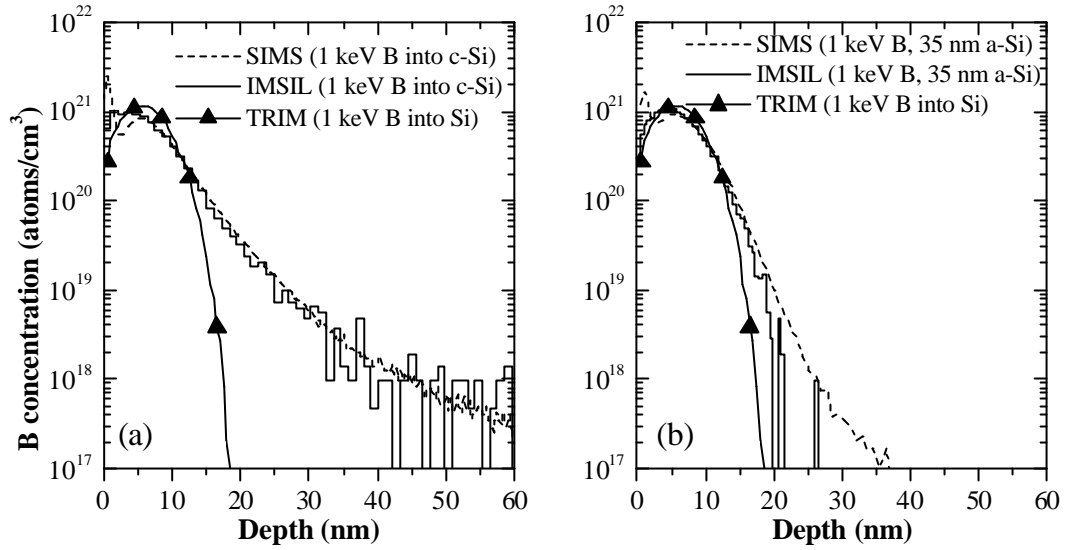
**Figure 6.4** Lattice image of the pre-amorphized sample after laser annealing at  $0.52 \text{ J/cm}^2$ . Recrystallization has occurred throughout the region of the originally amorphous layer.

Further processing of the TEM image was done using the fast Fourier transform (FFT) function to simulate the electron diffraction pattern as would be obtained from the recrystallized region after LTP (shown in the inset of Fig. 6.4). The diffraction pattern consists of distinct spots with each spot representing diffraction from a plane of a single crystal. This confirms that the amorphous layer has been recrystallized to a single-crystalline structure.

## **6.4 TED of Boron During Post-LTP Anneal**

### **6.4.1 Validation of the implant simulator, IMSIL**

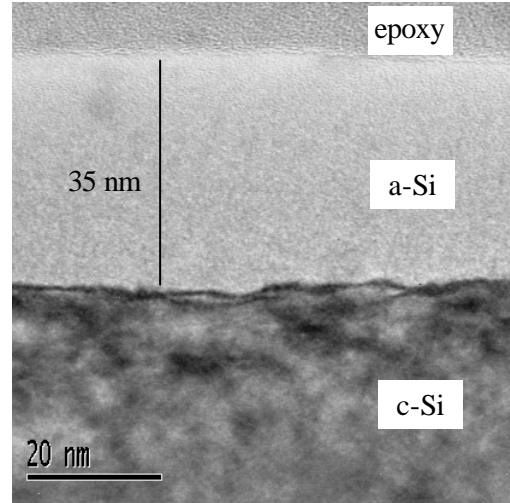
It is well known that the end-of-range (EOR) region contains a supersaturation of interstitial defects that were generated during PAI. During subsequent thermal annealing, these defects may release excess interstitials (EI) that cause the enhanced diffusivity of certain dopants (e.g. boron). Hence, it is important to understand the role of these excess interstitials in the transient enhanced diffusion of boron during a post-LTP anneal. This was done using the binary collision code implant simulator (IMSIL) [102]. In order to check the validity of IMSIL, we compare the as-implanted boron profiles in (100) crystalline silicon and amorphous silicon that were obtained from SIMS with simulated profiles from IMSIL and TRIM. These profiles are shown in Fig. 6.5. In all cases, the tilt angle and the dose of the boron ion implantation is  $0^\circ$  and  $1 \times 10^{15}/\text{cm}^2$ , respectively.



**Figure 6.5** Comparison of as-implanted 1 keV B profiles obtained from SIMS with simulated profiles from IMSIL and TRIM. (a) in c-Si and (b) in a-Si.

All ISMIL simulations were performed with 20000 ions while a total of 80000 ions were run using TRIM. For the IMSIL simulation of 1 keV B<sup>+</sup> implant into a-Si on c-Si, the thickness of the a-Si layer was assigned to be 350 Å. This corresponds approximately to the thickness of the amorphous layer created by a 3×10<sup>15</sup>/cm<sup>2</sup>, 10 keV Si<sup>+</sup> PAI (see Fig. 6.6). The TRIM profiles in Figs. 6.5(a) and 6.5(b) are the same since there is no option to specify the crystallinity of the substrate in TRIM. A 17 Å thick native oxide layer was included for the simulation of 1 keV B<sup>+</sup> implantation into (100) c-Si to have a better fit of the IMSIL results with the actual SIMS profile. From Fig. 6.5, it is clear that the shapes of the IMSIL “profiles” (histograms) resemble closely that of the experimental SIMS profiles for both c-Si and a-Si substrates. On the other hand, the TRIM profile drops off sharply at a depth of ~2.2R<sub>p</sub>, probably due to the fact that the simulation code for TRIM is applicable only to amorphous targets or random directions of a crystalline target [121]. The excellent

agreement between the simulated and measured profiles for the 1 keV B<sup>+</sup> implant validates the use of IMSIL for the simulation of collision cascades during ion implantation into silicon.

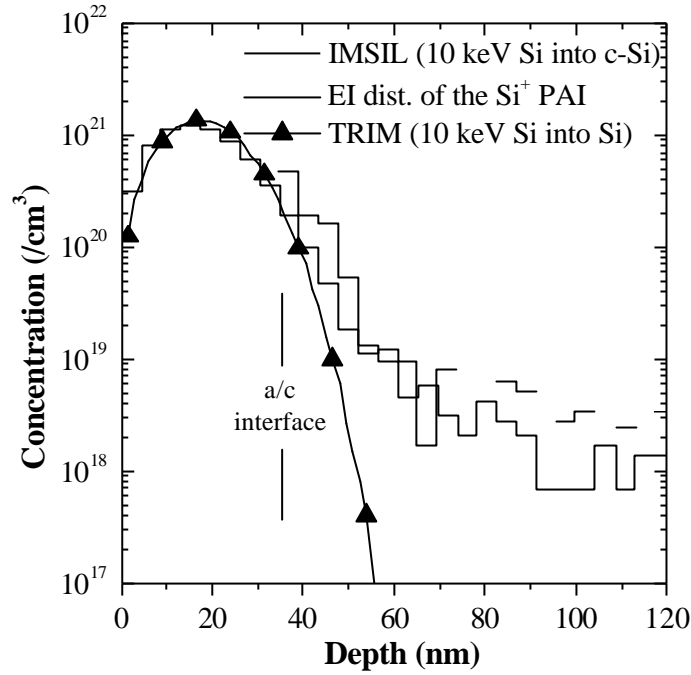


**Figure 6.6** Cross-sectional transmission electron micrograph of a sample that was pre-amorphized with  $3 \times 10^{15}/\text{cm}^2$ , 10 keV Si<sup>+</sup>.

#### 6.4.2 Simulations of implantation cascades

In the light of the previous section, we used IMSIL to simulate the detailed implantation cascades of the  $3 \times 10^{15}/\text{cm}^2$ , 10 keV Si<sup>+</sup> PAI into c-Si, and the results are shown in Fig. 6.7. The net profile of the excess interstitials (EI) is obtained by subtracting the total number of vacancies from the total number of interstitials that were generated during implantation. It can be seen that the distribution of excess interstitials somewhat mimics the simulated as-implanted Si profile. As a comparison, the Si ion distribution profile obtained from TRIM is also included in Fig. 6.7. As expected, there is a discrepancy between the IMSIL and TRIM profiles, especially near the tail of the implant (i.e. beyond a depth of  $\sim 2.2R_p$ ).

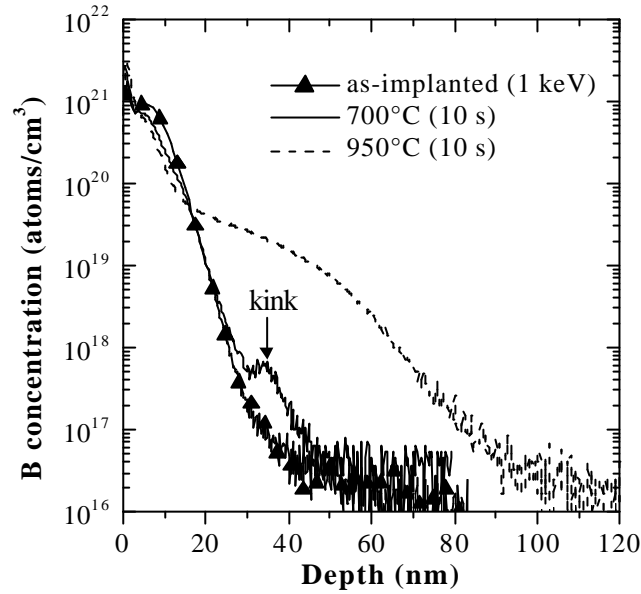




**Figure 6.7** Simulated profiles of the distribution of ions and excess interstitials for the  $3 \times 10^{15}/\text{cm}^2$ , 10 keV  $\text{Si}^+$  PAI (as obtained from IMSIL and TRIM).

Since the PAI layer encompasses the entire boron profile, it is generally accepted that the “interstitials” that were generated by the 1 keV  $\text{B}^+$  implant do not contribute to boron TED. However, the distribution of excess interstitials induced by the boron ion implantation can still be extracted from IMSIL, and it is found that these excess interstitials are indeed confined within the pre-amorphized layer. Hence, for this sample, the excess interstitials in the EOR region that will directly affect enhanced diffusion of boron during the post-LTP RTA is solely contributed by the  $\text{Si}^+$  implantation. One simple way to determine the presence of EOR defects is to subject the as-implanted sample (pre-amorphized with  $3 \times 10^{15}/\text{cm}^2$ , 10 keV  $\text{Si}^+$ ) to a low temperature RTA. As shown in Fig. 6.8, the presence of a kink at a depth of  $\sim 36$  nm is clearly observed for a sample that was annealed at 700 °C for 10 s. The kink represents segregation of boron atoms near the original a/c interface,

where there is a supersaturation of point defects. It appears that the annealing condition is not adequate to dissolve the boron clusters formed during ion implantation or during the initial stage of the thermal annealing process.



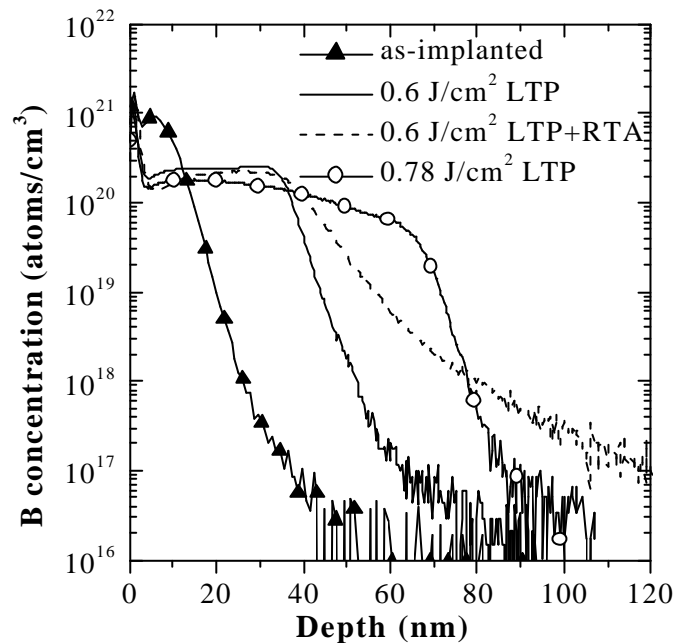
**Figure 6.8** SIMS profiles of 1 keV boron implanted into silicon (pre-amorphized with 10 keV Si<sup>+</sup>). The presence of a kink at a depth of ~36 nm is clearly observed for a sample that was annealed at 700 °C for 10 s.

#### 6.4.3 Enhanced diffusion of boron during post-LTP RTA

Figure 6.9 depicts the SIMS depth profiles of boron after LTP at different fluences and after a post- LTP (0.6 J/cm<sup>2</sup>) rapid thermal anneal at 825 °C for 30 s. This RTA condition (thermal budget) was chosen based on the assumption that the subsequent thermal cycle that the sample would experience in conventional MOSFET fabrication is the silicidation process. The abrupt junctions that are typically formed by LTP can be observed from Fig. 6.9. For the sample annealed by 0.6 J/cm<sup>2</sup> LTP, the melt depth is estimated to be

356 Å. This corresponds well to the thickness of the amorphous layer created by the 10 keV Si<sup>+</sup> PAI (see Fig. 6.6).

The result gives a clear indication that during LTP, the primary melt front has propagated through the entire amorphous layer, stopping at the original a/c interface. Based on the fact that a-Si has a lower melting point than c-Si [58, 59], the pre-amorphized layer can be melted without melting the underlying crystalline substrate. As pointed out by Talwar *et al.* [71], the pre-amorphization depth can thus be used to define the final junction depth (just like in the case of the 0.6 J/cm<sup>2</sup> LTP sample). However, as will be seen later, the damage in the EOR region is not adequately annealed by the LTP alone.



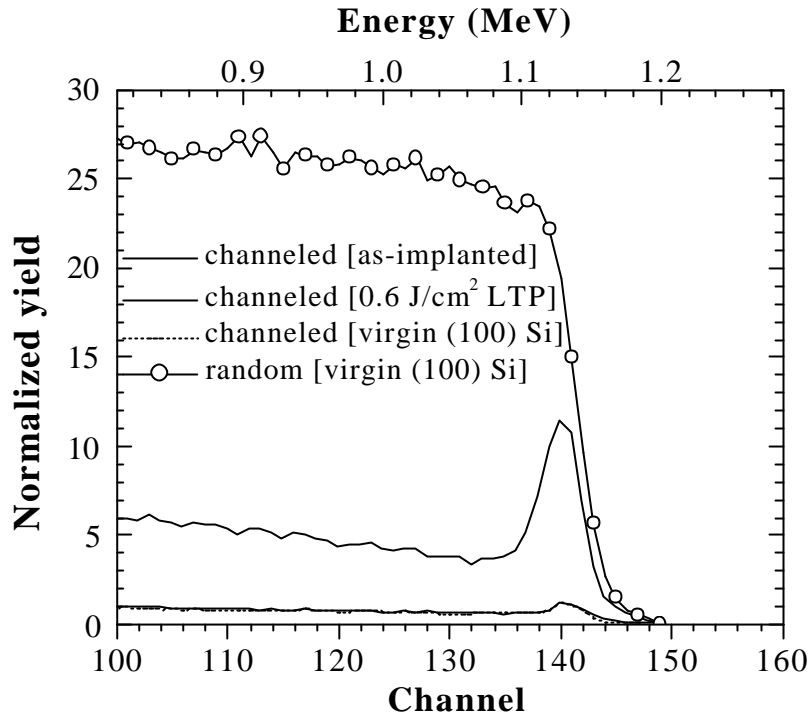
**Figure 6.9** SIMS depth profiles of boron after LTP at different fluence and after a post-LTP (at 0.6 J/cm<sup>2</sup>) anneal. The PAI condition was  $3 \times 10^{15}/\text{cm}^2$ , 10 keV Si<sup>+</sup>.

When the 0.6 J/cm<sup>2</sup> LTP sample is subjected to a post-LTP anneal at 825 °C for 30 s, there is an appreciable shift in the boron profile (Fig. 6.9). For example, at a concentration of  $1 \times 10^{18}/\text{cm}^3$ , the junction depth has shifted inward by  $\sim 260$  Å after RTA.

This corresponds to a diffusion length ( $\sqrt{2Dt}$ ) that is much greater than the equilibrium diffusion length of  $\sim 8 \text{ \AA}$  predicted using Fair's value for the intrinsic diffusivity of boron [122]. The source of this anomalous diffusion is the supersaturation of interstitials in the EOR region. By integrating the EI profile in Fig. 6.7 (for the region  $\sim 200 \text{ \AA}$  beyond the pre-amorphization depth), the dose of interstitials in the EOR region is calculated to be  $\sim 3.9 \times 10^{14} / \text{cm}^2$ . At this dose, according to the "phase diagram" for {311} behavior by Stolk *et al.* [4], {311} defects and EOR loops are expected to be formed during the initial (ramp-up) stage of the annealing process. Upon further annealing, the unstable {311} defects dissolve while the EOR loops grow into more stable structures. When the {311} defects dissolve, they release excess interstitials for TED. However, TED of boron has been observed to occur in the absence of {311} defects [37], indicating that there may be more than one source of interstitials for boron TED. At this moment, a detailed understanding of the evolution of defects during a post-LTP anneal is still lacking.

#### 6.4.4 Recrystallization of the pre-amorphized layer

The channeled backscattering spectra of the  $\text{Si}^+$  pre-amorphized sample before and after LTP are shown in Fig. 6.10. The random and channeled backscattering spectra of a virgin (100) silicon sample are also displayed for reference. The random spectra of the pre-amorphized and laser annealed samples are almost identical to that of the virgin sample and are not shown. From Fig. 6.10, it can be seen that the intensity of the silicon surface peak for the pre-amorphized sample is greater than that of virgin (100) Si, indicating the presence of damage near the surface of the pre-amorphized sample.



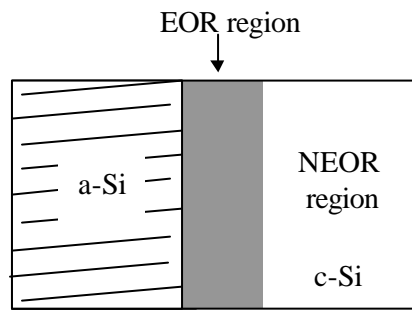
**Figure 6.10** Random and channeled backscattering spectra of a virgin (100) silicon sample and the  $\text{Si}^+$  pre-amorphized sample before and after LTP at  $0.6 \text{ J/cm}^2$ .

However, there is a significant reduction in the intensity of the Si surface peak after a LTP at  $0.6 \text{ J/cm}^2$ . It is observed that the channeled RBS spectrum for the  $0.6 \text{ J/cm}^2$  laser-annealed sample virtually coincides with the spectrum for the virgin sample, indicating that the pre-amorphized layer has been completely annealed with a single-pulse laser anneal at  $0.6 \text{ J/cm}^2$ . It should be mentioned that this laser-regrown layer may contain residual defects such as microtwins and stacking faults [65] that are not detected by RBS. Similarly, EOR defects cannot be easily detected using this technique. Hence, although RBS shows that the pre-amorphized layer has been completely annealed, the EOR damage is not sufficiently annealed by the nanosecond laser irradiation (as indicated by the boron TED during the post-LTP anneal).

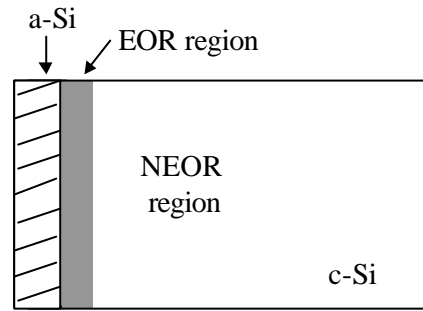
#### 6.4.5 Control of boron TED during post-LTP anneal

In order to suppress boron TED during the post-LTP annealing, it may be necessary to extend the melt depth to beyond the amorphous layer (over-melting) such that the interstitial dose in the region adjacent to the laser-melted layer is minimized. A new term is proposed for this region; it is referred as the “next to end-of-range” (*NEOR*) region. A model based on melting beyond the amorphous layer during the initial LTP step is shown in Fig. 6.11. Preferably, the dose of the excess interstitials in the NEOR region (defined as  $\sim 200 \text{ \AA}$  beyond the melt depth) should be less than the threshold dose for  $\{311\}$  formation, which is  $\sim 5 \times 10^{12} / \text{cm}^2$  [123]. From the process margin standpoint, over-melting into the substrate is rather undesirable but this is one alternative to minimize TED after LTP. This is because EOR damage cannot be avoided if a PAI is performed. It should be realized that the melt depth can still be controlled primarily by the fluence.

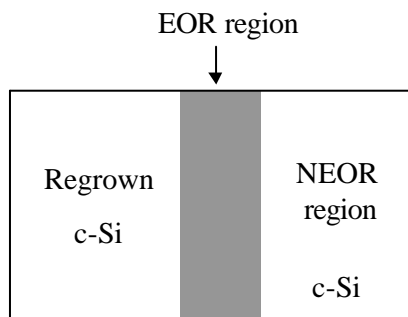
Figure 6.12 is a plot of the simulated interstitial dose in the NEOR region (for the 10 keV  $\text{Si}^+$  PAI sample) as a function of melt depth. It is assumed that the laser-melted Si recrystallizes into a good-quality crystal such that the excess interstitials (if any) trapped in the regrown crystal do not have a significant influence on the boron TED during subsequent anneal.



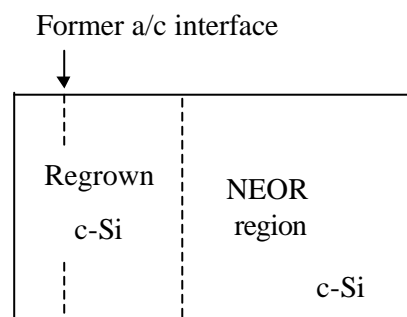
Deep PAI layer.



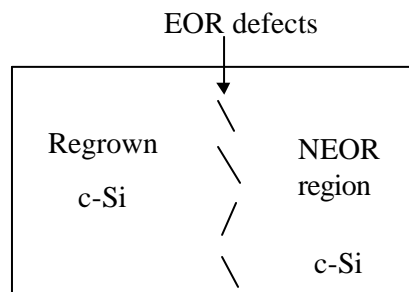
Shallow PAI layer.



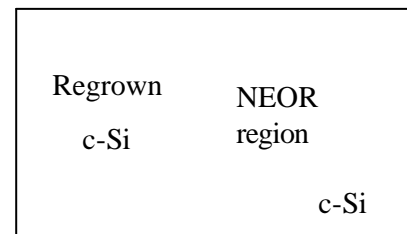
After LTP. Melt front stops at former a/c interface.



After LTP. Melt front penetrates into NEOR region with a melt depth that is comparable to that of the deep PAI case.



After post-LTP anneal. Dissolution of EOR defects gives rise to TED.

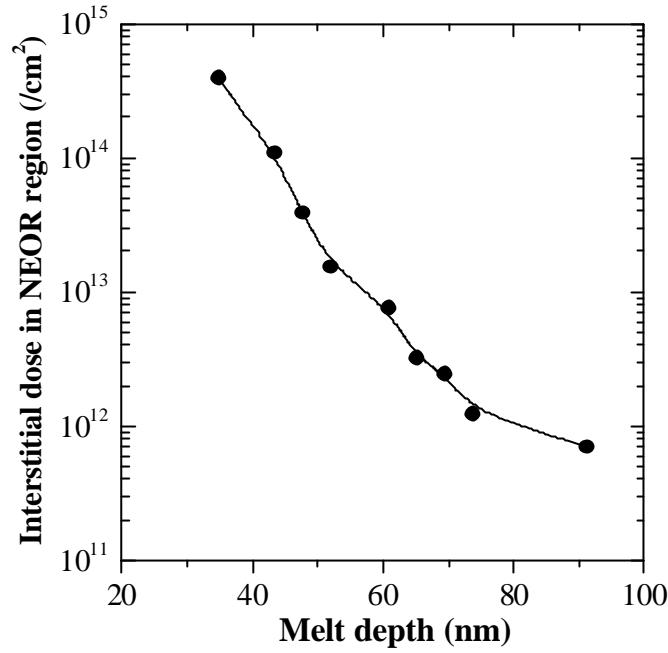


After post-LTP anneal. Absence of EOR defects nearly eliminates TED.

(a)

(b)

**Figure 6.11** Schematics showing the effect of melt front position on TED caused by EOR defects. (a) Melt front stops at former a/c interface. (b) Melt front penetrates into the NEOR region.



**Figure 6.12** Plot of the simulated interstitial dose in the NEOR region (for the 10 keV Si<sup>+</sup> PAI sample) as a function of melt depth.

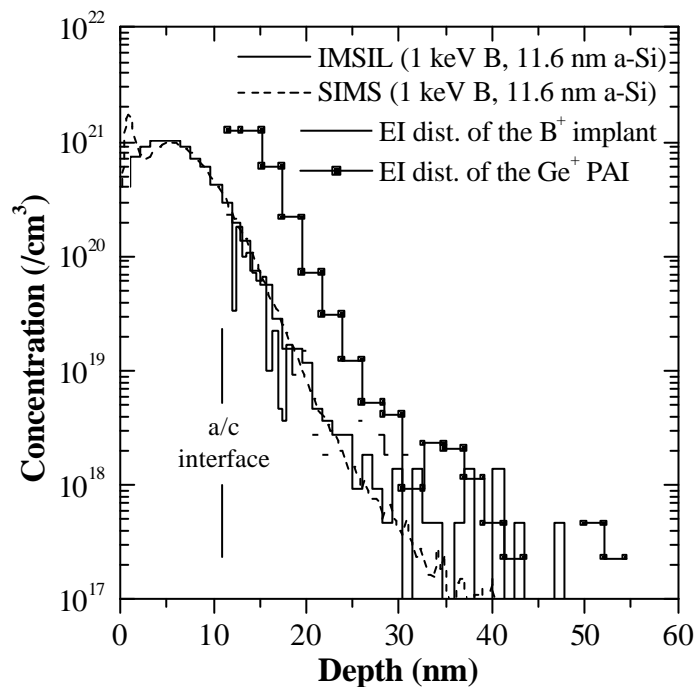
From Fig. 6.12, it can be deduced that the laser needs to melt at least 630 Å of Si to achieve an EI dose less than  $5 \times 10^{12}/\text{cm}^2$  in the NEOR region. This would result in a concentration profile similar to that of the  $0.78 \text{ J}/\text{cm}^2$  laser-processed sample as shown in Fig. 6.9. Unfortunately, such a deep junction may have adverse effects on the performance of short-channel devices. Moreover, it can be seen from Fig. 6.9 that after LTP, there is a slight decrease in boron concentration at the maximum melt depth. The result suggests that the melt duration is not sufficient to uniformly distribute the boron atoms within the melted layer.

Therefore, it can be proposed to use a pre-amorphizing implant of a lower dose and/or implantation energy to produce a shallower amorphous layer to control TED without compromising the final junction depth. Pre-amorphization of silicon is still necessary in order to prevent channeling (as shown in Fig. 6.5) and to lower the threshold laser fluence



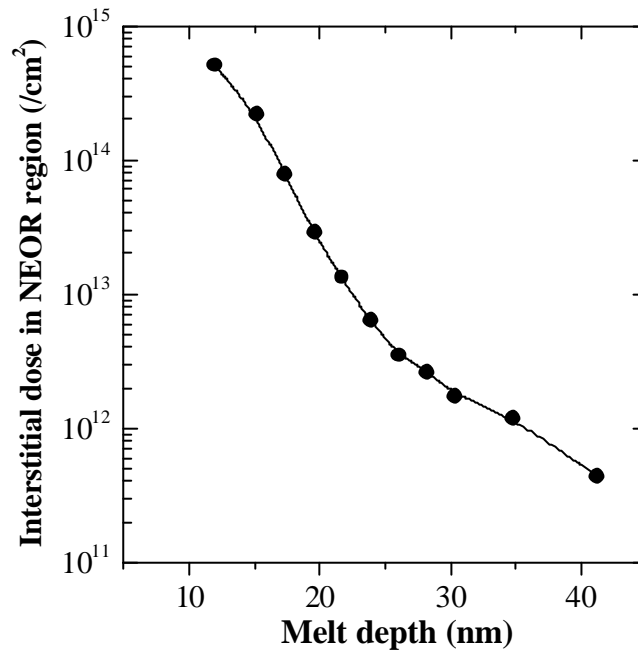
required to melt the Si substrate [67]. The second point has also been addressed in Chapter 4. From the XTEM micrograph shown in Fig. 6.2, it can be observed that the 5 keV Ge<sup>+</sup> PAI had created an amorphous layer of approximately 116 Å thick.

Figure 6.13 shows the simulated profiles of the implantation cascades of a  $1 \times 10^{15}/\text{cm}^2$ , 5 keV Ge<sup>+</sup> PAI into c-Si, followed by the implantation of 1 keV B<sup>+</sup> with a dose of  $1 \times 10^{15}/\text{cm}^2$ . It is noticed that the boron profiles (both IMSIL and SIMS) of this sample are similar to that of the 10 keV Si<sup>+</sup> PAI sample (shown in Fig. 6.5), indicating that this shallow (~116 Å) amorphous layer is adequate to prevent most of the channeling. Apparently, this boron profile is not completely contained within the amorphous layer created by the 5 keV Ge<sup>+</sup> PAI. Thus, in this case the excess interstitials generated by the 1 keV B<sup>+</sup> implant (beyond the 116 Å PAI layer) may also affect TED during subsequent thermal annealing.



**Figure 6.13** SIMS profile of boron and simulated profiles of boron ions and excess interstitials that were generated by a 1 keV B<sup>+</sup> implant and a 5 keV Ge<sup>+</sup> PAI.

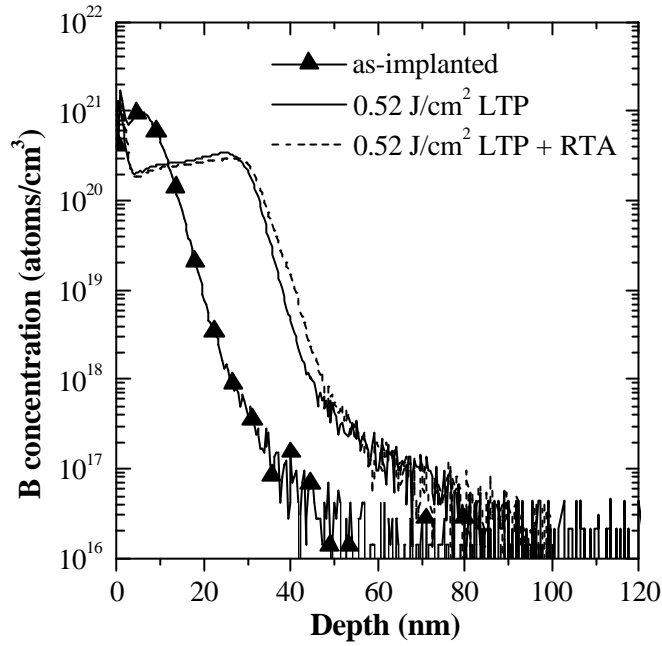
Figure 6.14 shows the simulated interstitial dose in the NEOR region (for the 5 keV  $\text{Ge}^+$  PAI sample) as a function of melt depth, taking into account the excess interstitials that were generated by the 1 keV  $\text{B}^+$  implant. It can be observed that for melt depths greater than 245 Å, the interstitial dose in the NEOR region would be less than  $5 \times 10^{12}/\text{cm}^2$ . Therefore, it is expected that the transient enhanced diffusion of boron (especially enhanced diffusion arising from the dissolution of {311} defects) be minimized for such melt depths.



**Figure 6.14** Plot of the simulated interstitial dose in the NEOR region (for the 5 keV  $\text{Ge}^+$  PAI sample) as a function of melt depth.

The boron SIMS profiles (in the  $\text{Ge}^+$  PAI sample) after LTP at  $0.52 \text{ J/cm}^2$  and after a post- $0.52 \text{ J/cm}^2$  LTP anneal (at  $825^\circ\text{C}$  for 30 s) are shown in Fig. 6.15. The laser-induced melt depth is estimated to be 290 Å, corresponding to an interstitial dose of  $\sim 2.7 \times 10^{12}/\text{cm}^2$  in the NEOR region (extracted from Fig. 6.14). Furthermore, it is observed that at a concentration of  $1 \times 10^{18}/\text{cm}^3$ , the junction has shifted only by  $\sim 30 \text{ Å}$  during the post-LTP

anneal. As this extent of boron diffusion is rather insignificant, the junction maintains its abruptness after the post-LTP anneal. This indicates that TED can indeed be suppressed by over-melting into the substrate, consistent with our hypothesis.



**Figure 6.15** Boron SIMS profiles (in the  $\text{Ge}^+$  PAI sample) after LTP at  $0.52 \text{ J/cm}^2$  and after a post- $0.52 \text{ J/cm}^2$  LTP RTA. Over-melting into the substrate nearly eliminate boron TED.

The near-complete absence of TED further suggests that the amount of “quenched-in” interstitials [124] in the recrystallized silicon (which can act as a source of interstitials) is negligible. This is probably due to the near-perfect liquid phase epitaxial regrowth of the melted layer. The proposed mechanism on the control of boron TED during a post-LTP anneal is illustrated in Fig. 6.11(b). It shows that for a shallower PAI layer, the melt front can easily penetrate into the NEOR region with a melt depth that is comparable to that of the deep PAI case. This reduces the dose of interstitials that can contribute to TED during

further annealing. The high resolution XTEM lattice image of the 5 keV  $\text{Ge}^+$  pre-amorphized sample after LTP at  $0.52 \text{ J/cm}^2$  was shown earlier (Fig. 6.4). It can be observed that the laser-regrown layer is virtually defect-free and does not contain any microtwins or stacking faults, as opposed to what might be expected in the absence of over-melting.

## 6.5 Summary

In summary, we have shown that although the amorphous layer in pre-amorphized silicon can be completely annealed by the nanosecond laser irradiation, the EOR damage is not sufficiently annealed. These EOR defects in turn can cause boron TED to occur during a post-LTP anneal. Since the EOR damage cannot be avoided if a PAI is performed, the melt depth should be extended to beyond the amorphous layer to minimize the dose of excess interstitials in the NEOR region. We have demonstrated that by using a shallower PAI layer (where channeling is still prevented), the melt front can easily penetrate into the NEOR region with a melt depth that is comparable to that of the deep PAI case. In this way, even if the initial boron profile is not completely contained within the amorphous layer, enhanced diffusion of boron can be significantly suppressed and the junction maintains its abruptness after the post-LTP anneal.

# **CHAPTER 7**

## **PHASE TRANSFORMATIONS**

### **DURING LTP OF GATE STACKS**

#### **7.1 Introduction**

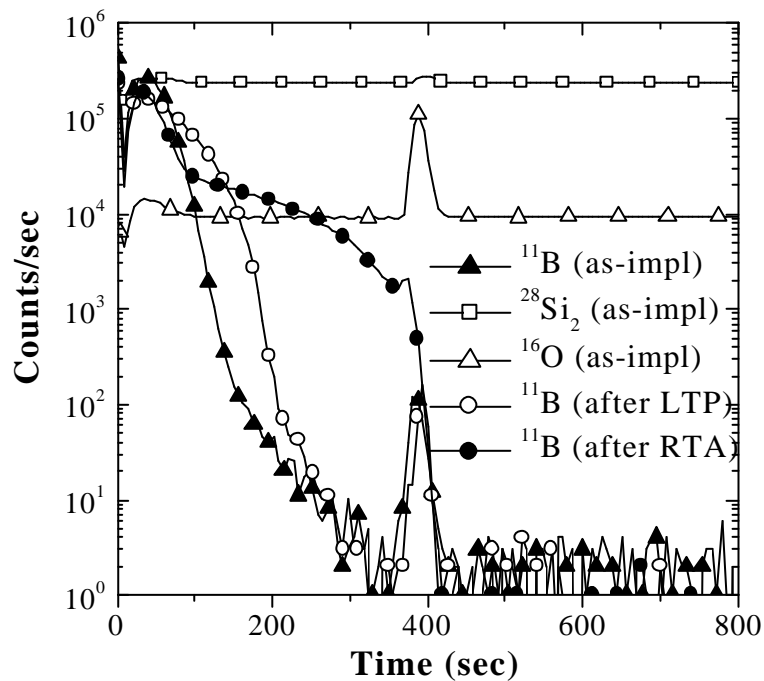
This chapter presents the results and relevant discussions pertaining to the phase transformations during LTP of gate stacks (which consist of either a poly-Si/SiO<sub>2</sub>/Si structure or an a-Si/SiO<sub>2</sub>/Si structure). It begins with the determination of the effect of a TiN/Ti cap layer on the melt characteristics of poly-Si. The second part of the chapter discusses the time-resolved reflectance (TRR) data obtained during the laser processing of as-deposited amorphous silicon gates overlying an ultra-thin gate dielectric. Based on the results, possible mechanisms for the occurrence of these phase transformations are proposed.

#### **7.2 Effect of a TiN/Ti Cap Layer on the Melt Characteristics of Poly-Si**

In a recent study, Verma *et al.* [125] have simulated the temperature profiles in the gate and source/drain extension (SDE) regions during the LTP of conventional transistor structures and found that the degree of melting in the gate is greater than that in the SDE. As a result, the channel begins to melt before the SDE. They attributed this to the difference in heat absorption and conduction between the gate structure and the SDE regions. The reason is that the energy absorbed in the gate (which is greater than that in the SDE) cannot be conducted away due to the presence of the hot SDE under it (which is adjacent to the channel). Hence, the channel region melts before the SDE and dopant activation cannot be

achieved without electrically shorting the source and the drain extension. To circumvent this problem, Verma *et al.* [125] proposed to deposit a thermally conductive absorber layer over the entire device to *thermally* “short” the gate and the SDE during LTP. In this way, the energy absorbed in the gate can diffuse away to other parts of the device/substrate efficiently and a process window whereby the SDE melts before the channel is created [71].

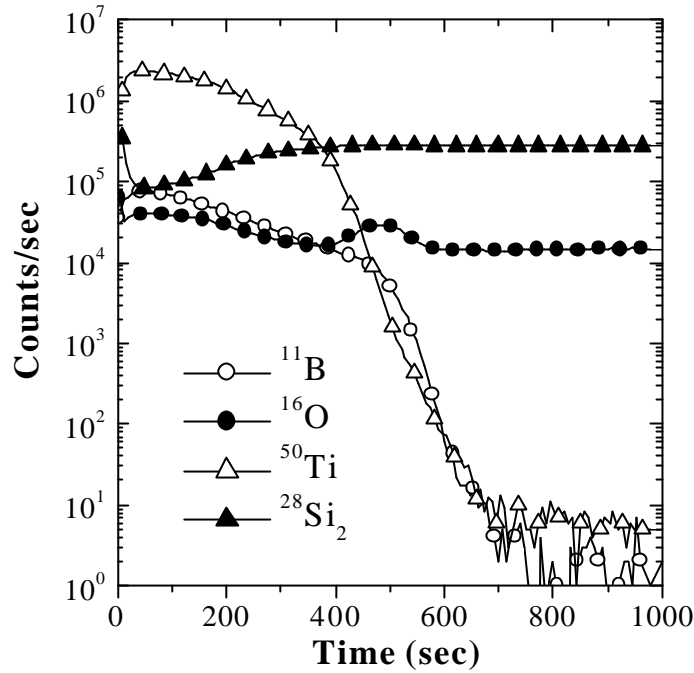
In this work, the laser irradiation of gate stacks (prepared using a conventional 0.25  $\mu\text{m}$  process flow) was performed to study the effect of a metal capping layer on the melt characteristics of 255 nm poly-Si overlying a 6 nm gate oxide layer. The results of the laser irradiation on uncapped poly-Si films are shown in Fig. 7.1. This figure compares the SIMS depth profiles of an as-implanted sample, a sample after LTP at  $0.68 \text{ J/cm}^2$ , and a sample after RTA at  $925^\circ\text{C}$  for 30 s.



**Figure 7.1** Comparison of SIMS depth profiles of an as-implanted sample, a sample after LTP at  $0.68 \text{ J/cm}^2$  and a sample after RTA at  $925^\circ\text{C}$  for 30 s (all without metal capping layers).

The location of the gate oxide layer can be identified from the  $^{16}\text{O}^+$  peak, or from the sudden increase in  $^{11}\text{B}^+$  counts at a sputtering time of  $\sim 390$  s. This yield enhancement of boron secondary ions (of nearly two orders of magnitude) is an artifact caused by the well-known matrix effect [106]. Under the  $0.68 \text{ J/cm}^2$  laser irradiation, the boron atoms have diffused to a depth corresponding to approximately one half of the total poly-Si thickness; this marks the extent of the laser-induced melt. The high diffusivity of boron in liquid silicon ensures diffusion only through the melt with minimal redistribution in the solid phase. In contrast, the sample after RTA shows boron diffusion throughout the poly-Si layer. This shows that the extent of boron diffusion in the laser-irradiated sample is not as substantial as that in the rapid thermal annealed sample. It should be recognized that there exists a boron peak in the sample even after RTA, suggesting that the 30 s,  $925^\circ\text{C}$  RTA is not sufficient to “dissolve” the boron clusters trapped at the peak location.

The effect of irradiating the sample with a TiN/Ti capping layer is illustrated in Fig. 7.2. This sample received both the rapid thermal anneal (prior to metal deposition) and the subsequent  $0.68 \text{ J/cm}^2$  LTP. Unreacted TiN and Ti (if any) were etched prior to SIMS analysis. Both Ti and B are observed to have diffused through the entire poly-Si layer, stopping at the  $\text{SiO}_2$  layer. Since such significant diffusion can only occur in the liquid phase [43], this result indicates the complete or near-complete melting of the poly-Si layer. Furthermore, the boron profile in Fig. 7.2 shows substantial flattening near the original poly-Si/ $\text{SiO}_2$  interface, reaching a level  $\sim 5$  times greater at the interface than following RTA alone.

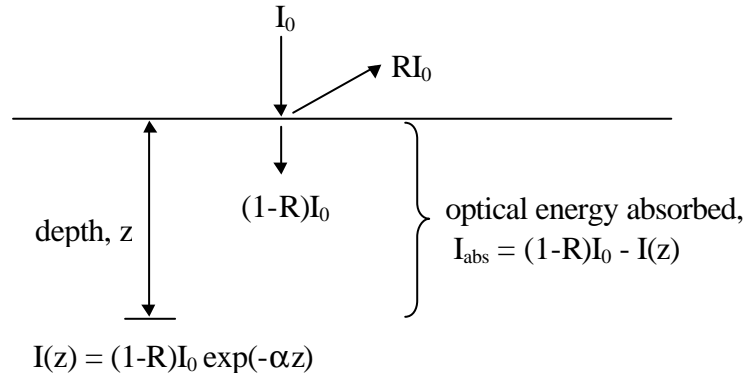


**Figure 7.2** Effect of using a TiN/Ti capping layer on the distribution of boron and titanium atoms in silicon after laser irradiation at  $0.68 \text{ J/cm}^2$ . Extensive diffusion of B and Ti had occurred.

However, as can be seen from Fig. 7.2, the Ti and B concentrations near the surface region remain much higher than that near the Si/SiO<sub>2</sub> interface, indicating that the melt duration is too short to achieve a completely uniform titanium and boron concentration profile. The non-abrupt Ti and B profiles near the silicon/oxide interface are probably due to ion-mixing effects during SIMS profiling [107]. As shown in Fig. 7.2, the peak of the  $^{16}\text{O}^+$  profile has also broadened following laser irradiation. The broadening is attributed to the roughening of the Si/SiO<sub>2</sub> interface during SIMS profiling. This roughening is known to be enhanced by the presence of a metallic layer [106]; in this case the roughening is enhanced by the TiSi<sub>2</sub> surface layer that is formed during laser irradiation.



The significant increase in the melt depth for the capped versus uncapped samples can be explained by taking into account the effect of the enhanced optical coupling of the TiN/Ti/poly-Si stack, thus increasing the net optical energy absorbed. Consider that the laser light, upon impinging a homogeneous surface, follows the optical path as shown in Fig. 7.3.



**Figure 7.3** Schematic of the optical path of the laser light upon impinging a homogeneous surface.

The correlation between the incident energy,  $I_0$  and the net optical energy absorbed in the material,  $I_{\text{abs}}$  can be expressed as:

$$\begin{aligned}
 I_{\text{abs}} &= (1-R)I_0 - I(z) \\
 &= (1-R)I_0 - (1-R)I_0 \exp(-\alpha z) \\
 &= (1-R)I_0 [1 - \exp(-\alpha z)]
 \end{aligned} \tag{7.1}$$

In a multiple-layered structure such as the TiN/Ti/poly-Si/SiO<sub>2</sub>/Si film stack, the optical path of the laser light upon impinging the surface is rather complex (due to multiple

constructive and destructive interference of light at the various interfaces). Therefore, we need to employ a simulation program, the thin film optical calculator (TFOC) [126] to determine the effective reflectivity,  $R_{\text{eff}}$  of the gate stack. The results from TFOC are compiled in Table 7.1. It can be seen that at  $\lambda = 248$  nm, the effective reflectivity of the TiN capped gate stack is approximately half that of the uncapped gate stack.

**Table 7.1** Comparison of the optical properties and net energy absorbed in TiN and Si.

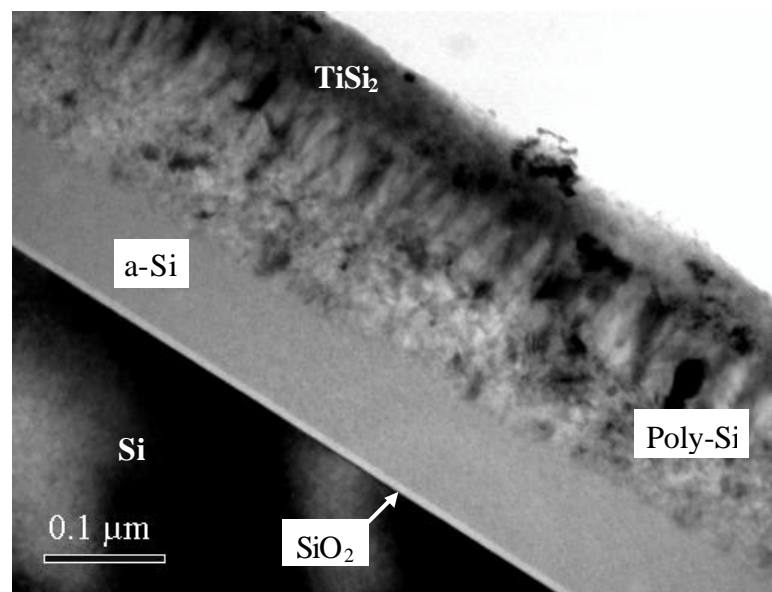
Properties	TiN/Ti capped	Uncapped
Effective reflectivity, $R_{\text{eff}}$ of gate stack	0.31	0.67
Absorption coefficient, $\alpha$ ( $\text{cm}^{-1}$ ) of the top 25 nm of material	$0.82 \times 10^6$	$1.81 \times 10^6$
$I_{\text{abs}}$ (in the top 25 nm of material) $= (1 - R_{\text{eff}})I_0 [1 - \exp(-\alpha z)]$	$\sim 0.60I_0$	$\sim 0.33I_0$

We then proceed to calculate the optical energy that is absorbed in the gate stacks. For simplicity, we compare the  $I_{\text{abs}}$  in the top 25 nm of material of the capped versus the uncapped (bare poly-Si) gate stack. Note that the thickness of the TiN capping layer is 25 nm. The absorption coefficient,  $\alpha$  of TiN and c-Si can be determined from Ref. [49, 127]. Using Eqn. (7.1), the  $I_{\text{abs}}$  in the gate stacks is computed and the results are summarized in Table 7.1.

From Table 7.1, it is evident that the net optical energy absorbed (in the top 25 nm of the material) in the TiN capped sample is nearly twice that of the uncapped sample, which is in accordance with expectations. It becomes clear that during irradiation, the TiN layer

absorbs a large fraction of the incident laser energy, which is efficiently transferred to the underlying layers due to the high thermal conductivity of TiN. As a consequence, the temperature of the film stack is raised to a temperature above the melting point of Ti and c-Si, but below that of TiN (3290 °C) and SiO<sub>2</sub> (1713 °C) [48]. Hence, the Ti and poly-Si underlayers are simultaneously melted, with the TiN and SiO<sub>2</sub> layers remaining intact. Sufficient fluence is absorbed to melt the entire poly-Si layer with the use of the TiN/Ti capping layer.

Figure 7.4 is a cross-sectional transmission electron micrograph obtained from a TiN/Ti capped sample after irradiation at 0.68 J/cm<sup>2</sup>. Energy dispersive X-ray (EDX) analyses (not shown) were performed to identify the various layers. The most prominent feature in Fig. 7.4 is the presence of a fairly uniform a-Si layer (~900 Å thick) that is adjacent to the SiO<sub>2</sub> layer. There is virtually no sign of physical degradation of the oxide layer, showing that it continued to provide a good barrier against epitaxial growth.



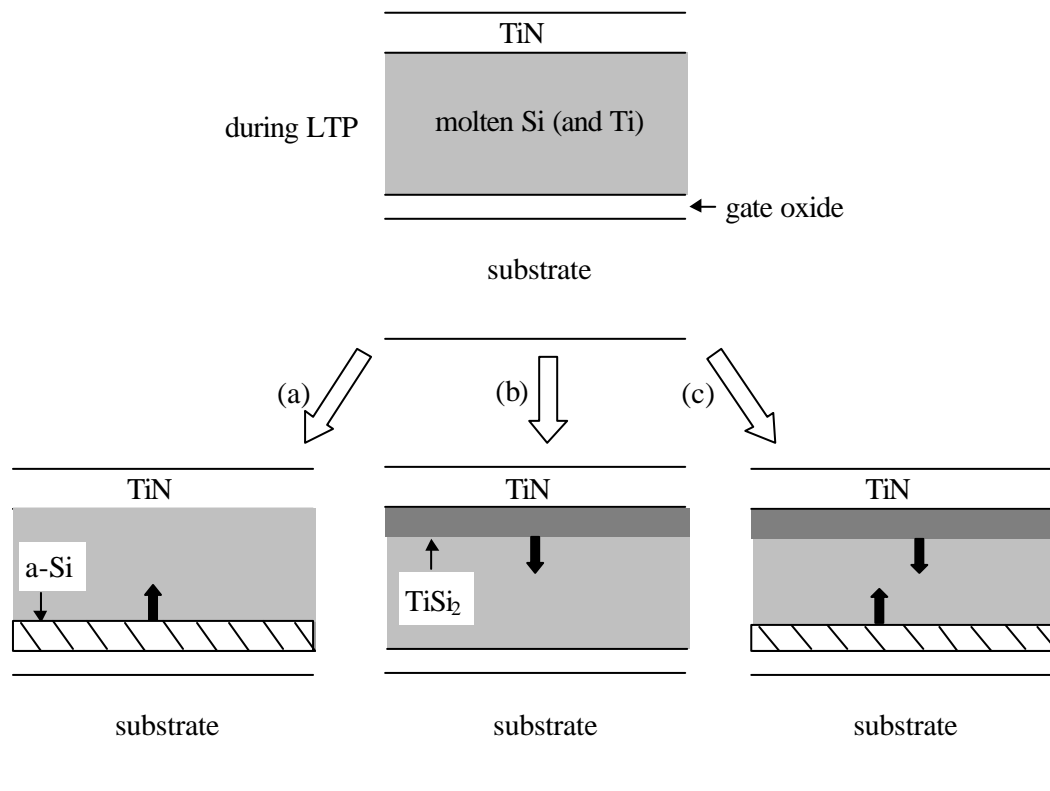
**Figure 7.4** Cross-sectional transmission electron micrograph obtained from a TiN/Ti capped sample after irradiating at 0.68 J/cm<sup>2</sup>.

The stability of the oxide layer is due to the (i) high melting point of  $\text{SiO}_2$  and (ii) negligible absorption of optical energy at 248 nm [48, 49]. The conversion of poly-Si to a-Si at the Si/oxide interface, coupled with the intact  $\text{SiO}_2$  layer supports the interpretation of a melt reaching, but not exceeding the original poly-Si/ $\text{SiO}_2$  interface. Contrary to the expectation that only poly-Si should form following a complete melt to the silicon/oxide interface, distinct regions of poly-Si and a-Si are observed instead (Fig. 7.4).

The formation of a-Si reveals that the temperature of the supercooled molten Si had fallen below the melting temperature of amorphous silicon and/or the solidification velocity had exceeded a certain value [50, 64, 69]. Either condition requires a high heat transfer rate to the substrate. This is possible since the  $\text{SiO}_2$  layer, despite its poor thermal conductivity, is only 6 nm thick. It is well established that in undoped Si, the critical velocity for amorphization is ~15 m/s or ~12 m/s for (100) or (111) surfaces, respectively [64, 69]. We believe that in our samples, the solidification temperature and the growth dynamics are substantially modified by the presence of titanium atoms such that the critical amorphization velocity is considerably reduced from the ~12-15 m/s criterion. An earlier study done by Baeri and Reitano [128] has shown that this amorphization criterion can be reduced in Si-As systems supersaturated with arsenic atoms.

Three possible mechanisms are proposed for the formation of the microstructures shown in Fig. 7.4. In a conventional growth mode, solidification starts at the oxide boundary as the lowest temperature in the system. Due to the Ti impurities and supercooling, nucleation of the amorphous phase dominates and solidification of a-Si proceeds toward the surface. Segregation of Ti, and possibly boron, occurs at the moving l-Si/a-Si interface at a high interface velocity. As solidification proceeds, the thickness of the a-Si layer increases.

This decreases the rate of heat transfer from the l-Si to the substrate (due to the low thermal conductivity of a-Si) and thus decreases the interface velocity. When the interface velocity or the concentration of the impurities reaches a critical level, nucleation and growth of poly-Si occurs, initially as fine grains and refining into large columnar-like grains. Explosive crystallization of the early-formed a-Si is suppressed by the Ti impurities. Finally, the remaining molten Si and Ti react to form  $\text{TiSi}_2$ .



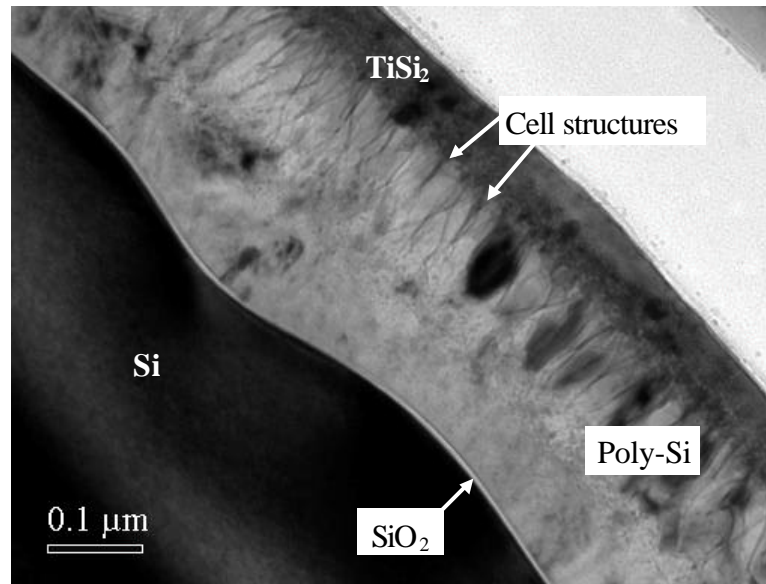
**Figure 7.5** Schematics illustrating the three possible scenarios for solidification. (a) conventional growth mode. (b) reverse growth mode. (c) combination of both modes. Dark arrows indicate the direction of solidification.

The schematic diagrams of the possible scenarios occurring during solidification upon LTP of a TiN/Ti capped gate stack are illustrated in Fig. 7.5. The second potential scenario

proposes a “reverse” growth mode, where poly-Si grows from the surface toward the silicon/oxide interface. EDX analysis shows that  $\text{TiSi}_2$  is formed only at the surface (Fig. 7.4) despite the fact that Ti atoms had diffused to a much greater depth (Fig. 7.2). In the bulk of the poly-Si layer, the concentration of Ti is not high enough to form critical stable nuclei. Since the melting points of  $\text{TiSi}_2$  and several other phases of  $\text{Ti}_x\text{Si}_y$  are higher than c-Si [48, 129], the  $\text{TiSi}_2$  layer probably forms first in the early cooling process, nucleating at the TiN layer (which remains unmelted during irradiation). In turn, the  $\text{TiSi}_2$  layer serves as an interface for poly-Si nucleation, with solidification then proceeding from the surface inward. The poly-Si grows into the supercooled liquid and ultimately quenches into a-Si near the silicon/oxide interface.

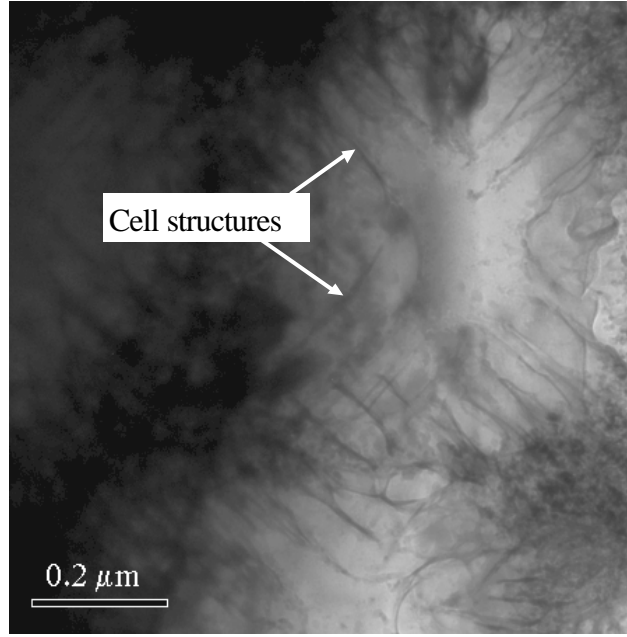
An intriguing alternative is a combination of both scenarios. The structure shown in Fig. 7.4 may be a result of two moving interfaces – one is a poly-Si layer nucleated and propagating from the surface, and the other an amorphous layer that nucleated at the Si/SiO<sub>2</sub> interface and moved toward the surface. The position where the two propagating interfaces finally meet is the demarcation in Fig. 7.4 between the a-Si layer and the fine-grained poly-Si. This complex scenario is possible since the diffused Ti can have very different influence on the melting temperatures of the polycrystalline and amorphous phases [130, 131].

Figure 7.6 shows an XTEM image of a TiN/Ti capped sample irradiated at a significantly higher fluence, 0.92 J/cm<sup>2</sup>. In contrast to Fig. 7.4, the oxide layer is severely deformed and the microstructure near the original poly-Si/SiO<sub>2</sub> interface is poly-Si instead of a-Si. The deformation of the oxide suggests that the melt extended well into the substrate, during which the thin oxide expanded and buckled under its own compressive stress.



**Figure 7.6** XTEM image of a TiN/Ti capped sample after laser irradiation at  $0.92 \text{ J/cm}^2$ . The TEM micrograph shows that the oxide layer is severely deformed.

At weak spots in the oxide, fractures occur and seeded growth from the substrate may occur. Even in the absence of the oxide failure, the cooling rate is reduced (due to the higher fluence) and may be insufficient to nucleate the amorphous phase. In addition, Fig. 7.6 shows the presence of well-defined cell structures near the surface region. These structures are formed due to liquid/solid interfacial instabilities arising from the titanium segregation during rapid solidification. Similar observations have also been made for In-Si and Ga-Si systems after high-dose implantation of  $\text{In}^+$  or  $\text{Ga}^+$ , followed by laser annealing [45]. The plan-view TEM image of the TiN/Ti capped sample after LTP at  $0.92 \text{ J/cm}^2$  is shown in Fig. 7.7. The presence of cell structures that have resulted from a highly non-equilibrium solidification process is evident from Fig. 7.7. The interior of each cell should be lowly-doped Si, and surrounding each column is a thin cell wall containing large concentrations of the rejected titanium atoms.



**Figure 7.7** Plan-view TEM image of the TiN/Ti capped sample after laser irradiation at  $0.92 \text{ J/cm}^2$ .

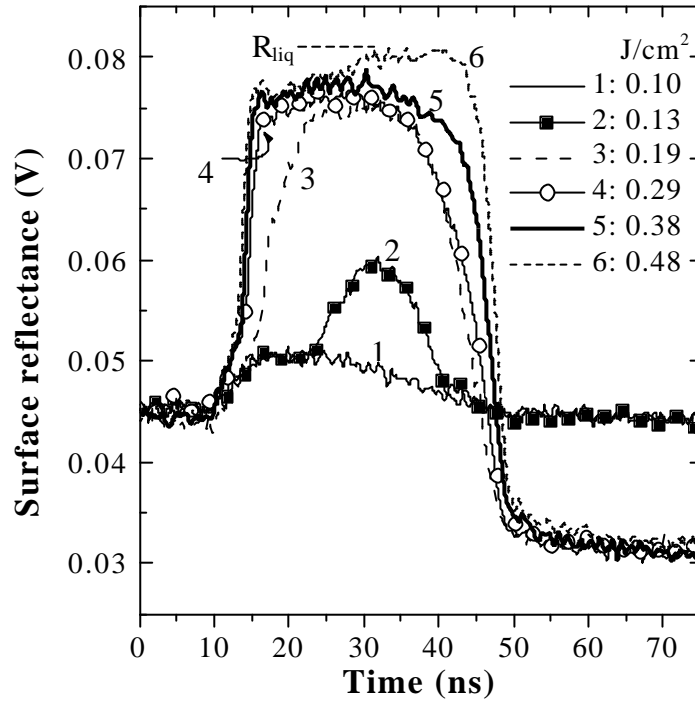
### 7.3 Results From TRR Measurements

In this section, single-pulsed LTP ( $\lambda = 308 \text{ nm}$ ) was performed on  $600 \text{ \AA}$  of as-deposited amorphous silicon (gate layer 1) overlying  $18 \text{ \AA}$  of silicon oxynitride. The gate layer 1 was implanted with  $\text{B}^+$  or  $\text{As}^+$  prior to laser irradiation. These samples will later be referred to as the “single-layer” capacitors. During LTP, *in-situ* time-resolved reflectance (TRR) measurements were conducted to record the evolution of the surface reflectance of the irradiated surface. The transient surface reflectance (measured in V) is analogous to the reflectivity of the film stack at a particular instant. The melt duration (time difference between the onset of melting and complete solidification) can also be determined from the TRR traces.



### 7.3.1 Arsenic-doped single-layer a-Si gates

The typical time-resolved reflectance traces obtained during the laser irradiation of arsenic-implanted a-Si gates at different energy densities are shown in Fig. 7.8. The numbers beside the traces represent the respective laser fluences,  $E_l$  and the smallest number denotes the lowest fluence.

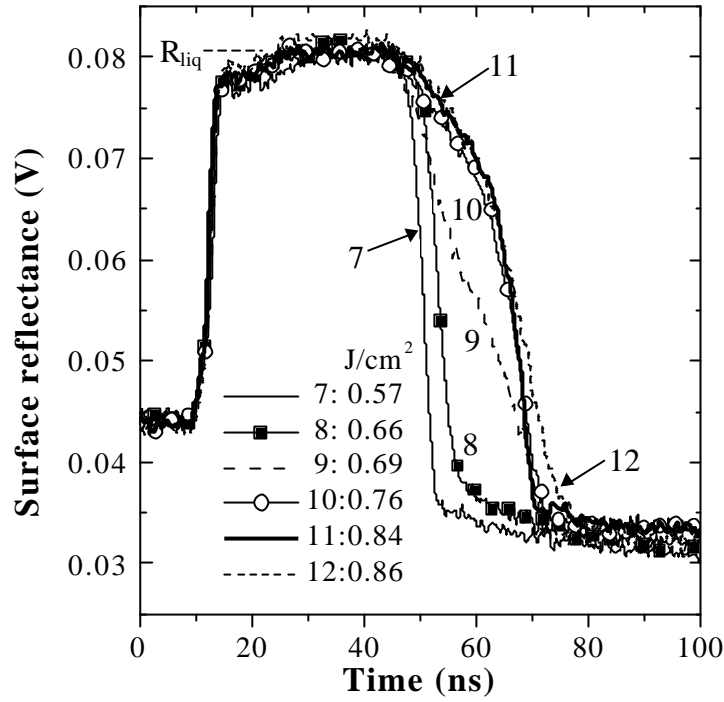


**Figure 7.8** Typical TRR traces obtained during LTP of arsenic-implanted a-Si at various fluences ( $0.10 \text{ J/cm}^2 \leq E_l \leq 0.48 \text{ J/cm}^2$ ).

For  $E_l \leq 0.10 \text{ J/cm}^2$ , melting does not occur since the increase ( $<12\%$ ) in reflectance is not significant enough to indicate the presence of a liquid layer. The increase in reflectance is ascribed to the laser-induced heating of the samples. For the  $0.13 \text{ J/cm}^2$  laser-processed sample, there is an  $\sim 32\%$  increase in reflectance for times between 23 and 42 ns. Based on the literature [64, 132], such an increase in reflectance cannot be achieved by heating in the solid state alone. Therefore, we attribute this increase to the nucleation of a liquid phase

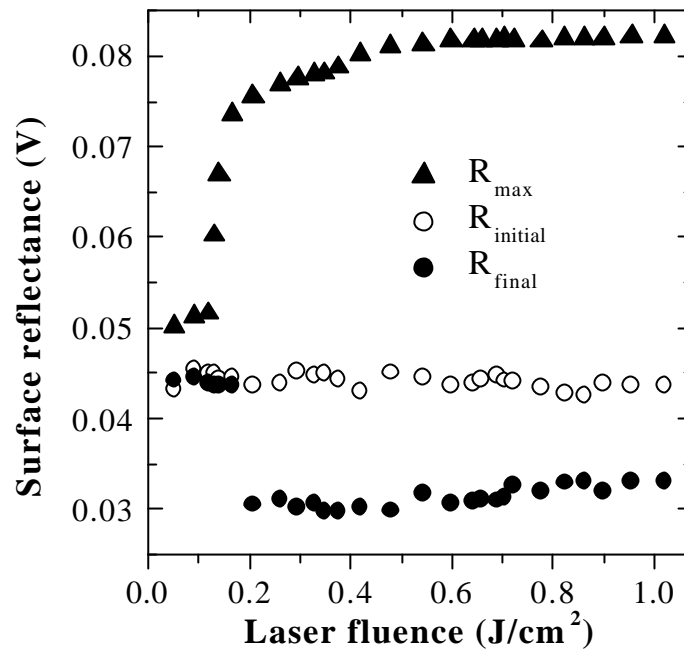
(onset of melting). From trace 2 in Fig. 7.8, it can be seen that the final value of the reflectance,  $R_f$  of the sample upon  $0.13 \text{ J/cm}^2$  LTP is the same as the value before irradiation,  $R_i$ , indicating that crystallization did not take place. This implies that the primary melt has solidified into a-Si (due to the steep temperature gradient at the low fluence), with explosive crystallization completely suppressed. Similar observations were made by Peercy *et al.* [133] for a-Si samples formed by  $\text{In}^+$  implantation. In contrast, when the fluence is increased to  $0.19 \text{ J/cm}^2$  and above, it is noticed from Fig. 7.8 that the value of  $R_f$  is lower than  $R_i$ . This is characteristic of an amorphous to crystalline phase transformation, suggesting that bulk of the sample has solidified into poly-Si (via explosive crystallization) upon LTP at  $E_l \geq 0.19 \text{ J/cm}^2$ .

As the laser fluence increases progressively, the maximum reflectance value,  $R_{\max}$  of the samples also increases, until it reaches the value that corresponds to the expected reflectance of liquid silicon,  $R_{\text{liq}}$ . The intensity of the reflected probe beam does not reach  $R_{\text{liq}}$  at  $E_l < 0.48 \text{ J/cm}^2$  because the liquid layer created at the surface is thinner than  $\sim 3.5$  skin depths of l-Si. Note that the skin depth of l-Si at the probe laser wavelength is  $\sim 9 \text{ nm}$  [57, 64]. It should be realized that the TRR traces at  $E_l \geq 0.57 \text{ J/cm}^2$  (Fig. 7.9) show the typical “top hat” feature whereby melt initiates at the irradiated surface and the surface remains molten throughout the melting process. It follows that the primary melt front propagates to the maximum melt depth after which the motion of the liquid/solid interface reverses direction and the melt returns to the surface, resulting in a decrease in surface reflectance. Signals (if any) that are reflected from the solidification front arising from explosive crystallization inside the sample are masked by the considerably thick, highly reflective molten Si layer at the surface.

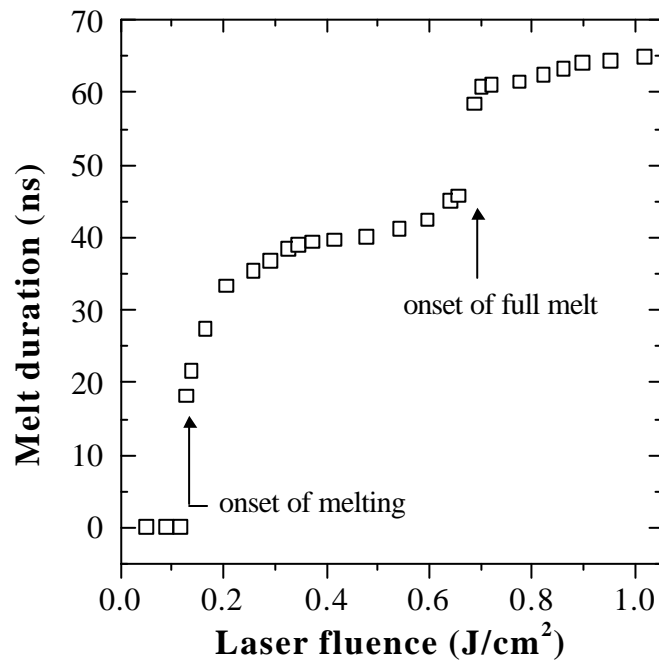


**Figure 7.9** Plots of the transient surface reflectance obtained during LTP of arsenic-implanted a-Si at various energy densities.

The sudden increase in the melt duration upon LTP at  $\sim 0.69 J/cm^2$  indicates the transition from a partial to a complete melt of the a-Si layer. It is known that upon complete melting of the a-Si film (especially on oxide, i.e. without c-Si seed layer), significant supercooling of the liquid is usually required before the onset of solidification [134]. Hence, the molten Si has to stay in liquid form for a longer period of time for solid nucleation to occur. This would result in an abrupt increase in the melt duration. The results of the TRR measurements are summarized in Figs. 7.10 and 7.11. These plots are derived from the transient reflectance traces. From Fig. 7.10, it can be seen that as the laser fluence increases, the maximum reflectance value of the samples increases gradually until it saturates at  $\sim 0.083 V$ . The onset of melting and the onset of full melt are also clearly seen from Fig. 7.11.



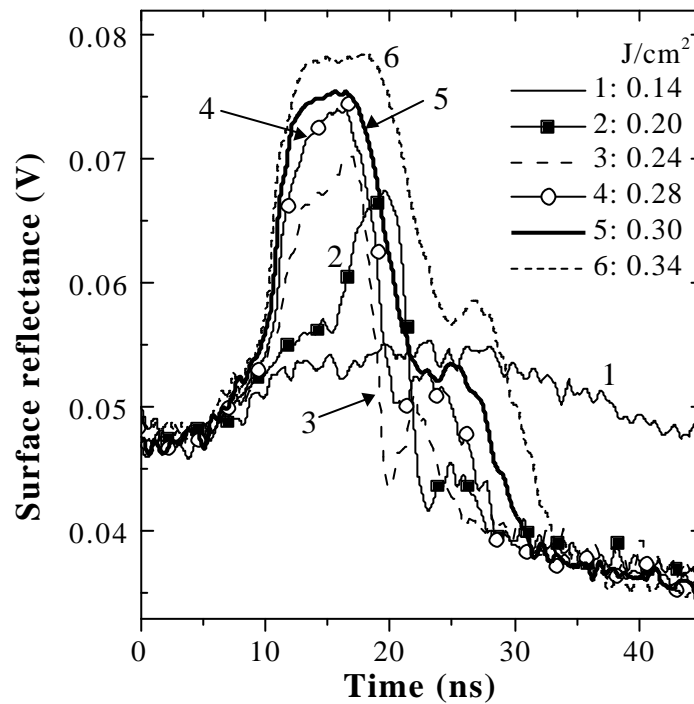
**Figure 7.10** Plot of the characteristic reflectance values as a function of laser fluence for arsenic-implanted a-Si.



**Figure 7.11** Plot of the melt duration as a function of laser fluence for an arsenic-implanted a-Si film.

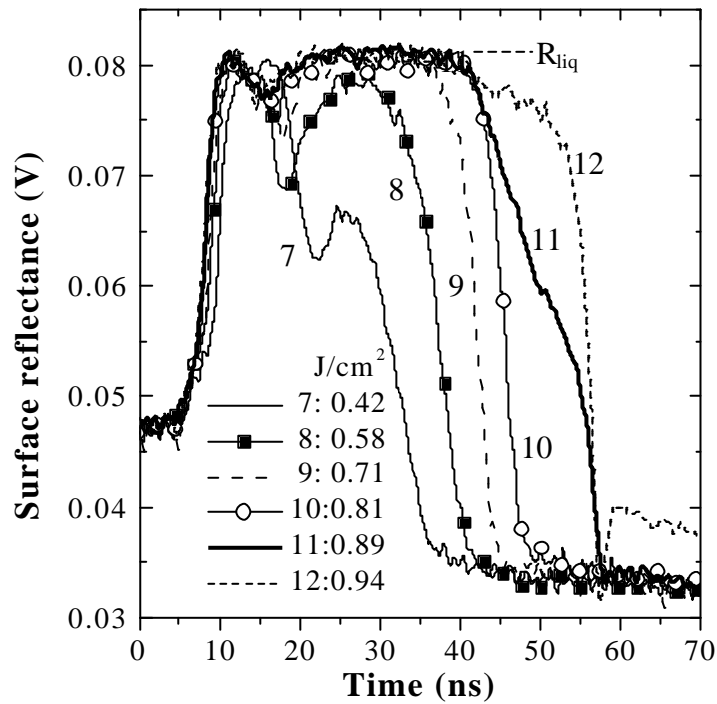
### 7.3.2 Boron-doped single-layer a-Si gates

In this section, the anomalous melt behavior during laser irradiation of boron-implanted a-Si is reported. The typical transient reflectance traces obtained during laser irradiation of B-doped amorphous silicon at various fluences ( $E_l$  is in the range of 0.14 to 0.34 J/cm<sup>2</sup>) are shown in Fig. 7.12. Similar to the case of the arsenic-implanted a-Si samples, it can be seen from Fig. 7.12 that the value of  $R_f$  becomes lower than  $R_i$  at  $E_l \geq 0.20$  J/cm<sup>2</sup>, showing that bulk of the sample has solidified into poly-Si after laser irradiation. An interesting feature to note in Fig. 7.12 is the presence of “double humps” in the TRR traces starting from  $E_l \sim 0.24$  J/cm<sup>2</sup>. The intensity of the second hump/peak seems to increase with an increase in laser fluence.



**Figure 7.12** Typical TRR traces obtained during LTP of boron-implanted a-Si at low energy densities ( $0.14 \leq E_l \leq 0.34$  J/cm<sup>2</sup>).

Figure 7.13 shows the temporal evolution of the reflectance of boron-implanted a-Si under laser irradiation at various fluences ( $0.42 \leq E_l \leq 0.94 \text{ J/cm}^2$ ). At a rather high fluence of  $0.81 \text{ J/cm}^2$  (trace 10), it is evident that appreciable melting has occurred. The melt depth should be greater than 32 nm considering the substantial melt duration. Although the TRR trace appears to exhibit the normal melt behavior, closer examination of the data reveals that the double-hump feature is still present in the TRR trace. This implies that there is no continuous layer of molten Si of  $\sim 32 \text{ nm}$  (3.5 skin depths) thick at the surface during the early stages of the laser irradiation.

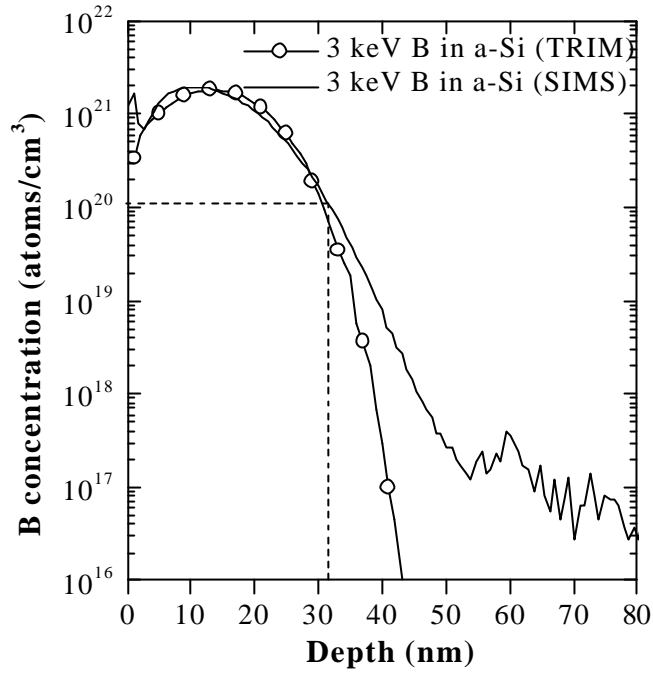


**Figure 7.13** Temporal evolution of the reflectance of boron-implanted a-Si under laser irradiation at various fluences ( $0.42 \leq E_l \leq 0.94 \text{ J/cm}^2$ ).

The presence of double humps in the TRR traces of Figs. 7.12 and 7.13 indicates some anomalies in the melt behavior of boron-implanted a-Si during laser irradiation (presence of a buried melt [135]). Since the occurrence of a buried melt is not observed in the arsenic-implanted samples (Section 7.3.1), we strongly believe that the double-hump features observed in the boron-implanted samples are associated with the implantation-induced damage in the a-Si layer.

It is known that microclusters of crystalline silicon may exist in the a-Si film even though it was deposited in the “amorphous” state [134, 136], suggesting that the a-Si film may not be completely amorphous prior to gate ion implantation. Furthermore, Roorda *et al.* [137] have shown that point defects analogous to vacancies and interstitials in c-Si also exist in a-Si. In the case of the As-doped samples, the dose of the arsenic implant ( $6 \times 10^{15}/\text{cm}^2$ ) is high enough to further amorphize the as-deposited a-Si film. On the other hand, since the dose of the boron implant is below the amorphization threshold dose, the boron implant only introduces damage to the a-Si film but not causing amorphization [138, 139]. This may explain the marked difference in the melt behavior of boron and arsenic-implanted a-Si samples.

Using the TRIM program [101], we have simulated the ion profile of the 3 keV boron implant and the result is shown in Fig. 7.14. The as-implanted boron SIMS profile is also overlaid in Fig. 7.14. As discussed by Peercy *et al.* [133], the nucleation of a liquid phase is likely to be caused by compositional inhomogeneities. It is thus believed that above a certain boron concentration (in this case  $\sim 1 \times 10^{20}$  atoms/cm<sup>3</sup> at  $\sim 3.5$  skin depths), the melting point of a-Si is significantly depressed such that melting occurs at a lower fluence compared to the regions with relatively low B concentration.



**Figure 7.14** Comparison of an as-implanted 3 keV B profile obtained from SIMS with a simulated profile from TRIM.

The data presented in Figs. 7.12 and 7.13 can be explained as follows. Melting initiates at the surface and the melt front quickly move towards the region where the melting temperature of a-Si is reduced (in the presence of high boron concentration) [61], giving rise to the first reflectance peak. The decrease in reflectance after the first maximum is reached indicates that surface solidification has occurred (probably due to residual impurities [64, 135]). The enthalpy released upon heterogeneous nucleation of the solid phase, coupled with the additional energy supplied from the laser source cause the primary melt to propagate deeper into the a-Si film and the reflectance increases. As a consequence, a second peak is formed and the time to reach complete solidification is prolonged.

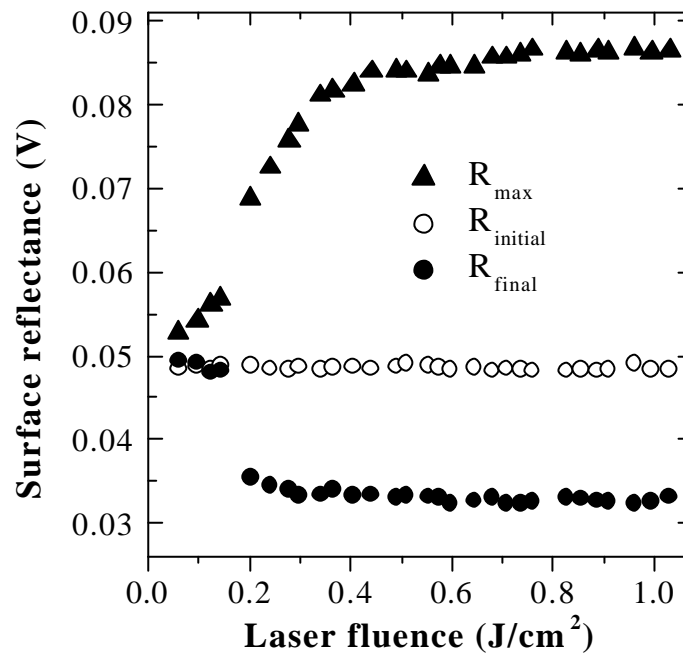


As the fluence increases, the surface nucleation of melt becomes more pronounced and the initial melt extends deeper into the a-Si film, leading to an increase in the initial maximum reflectance value. For  $E_f \geq 0.58 \text{ J/cm}^2$ , the primary melt first propagates to a depth of  $\sim 32 \text{ nm}$ , and the first reflectance peak is attained at  $R_{liq}$ . However, this initial melt front pauses at this depth before it gains enough energy to penetrate further into the a-Si layer (where the melting point is not significantly decreased). When the primary melt finally solidifies, it triggers a series of explosive crystallization process, producing secondary melts that transport boron atoms along with it.

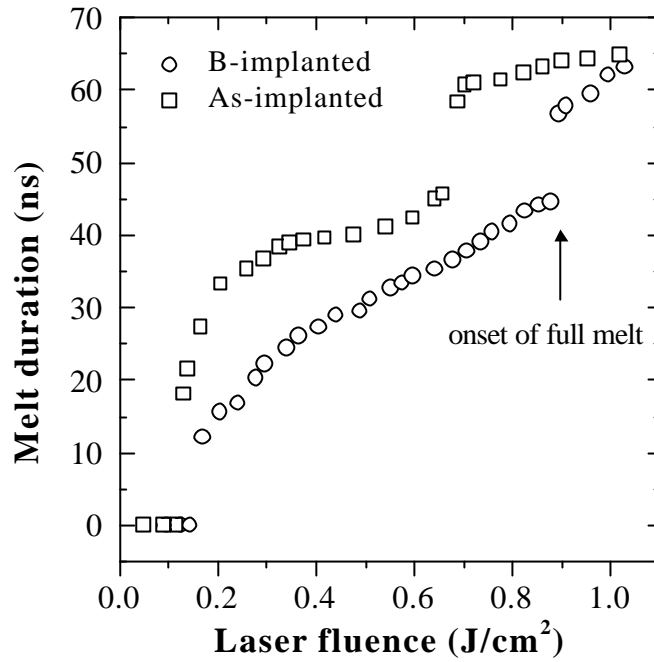
At sufficiently high fluences ( $E_f \geq 0.71 \text{ J/cm}^2$ ), it is clear from Fig. 7.13 that the intensity of the second peak exceeds that of the first peak, and the reflectance level eventually increases to  $R_{liq}$  again. This indicates that the newly formed solid phase has remelted during the later stage of LTP, suggesting that the surface l-Si solidifies into an amorphous layer.

Another salient feature in Fig. 7.13 is the abrupt increase in the melt duration upon LTP at  $0.89 \text{ J/cm}^2$  (trace 11); this marks the transition from a partial to a complete melt of the a-Si layer. It should be recognized that this transition to full melt occurs at a much higher fluence as compared to the case of the As-implanted samples. This is attributed to the amorphization of the as-deposited a-Si film as well as the large depression of the melting temperature of a-Si in the presence of high concentration of As atoms. This observation has important implications when we use LTP to form single-layer poly-Si gated capacitors with different types of gate dopants.

Figures 7.15 and 7.16 summarize the results of the TRR measurements done on B-doped samples. From Fig. 7.15, it can be seen that  $R_i$  remains relatively unchanged with fluence, whereas  $R_f$  decreases to a value lower than  $R_i$  starting from  $E_l \sim 0.20 \text{ J/cm}^2$ . Fig. 7.16 shows that the melt duration of the As-doped sample is consistently greater than that of the B-doped sample. As explained earlier, the longer melt duration is related to the greater degree of implantation-induced damage in the a-Si layer during the arsenic implant.



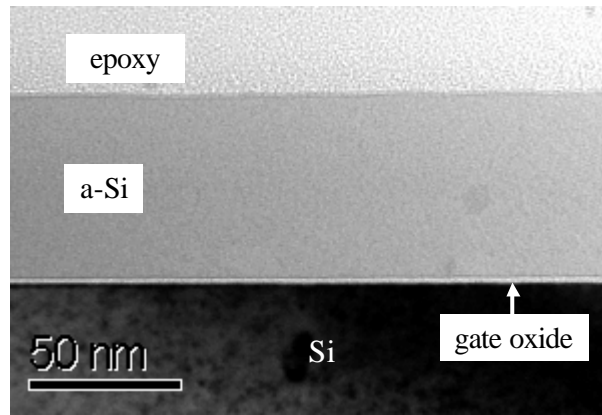
**Figure 7.15** Plot of the characteristic reflectance values as a function of laser fluence for a boron-implanted a-Si film.



**Figure 7.16** Plot of the melt duration as a function of laser fluence for a boron-implanted a-Si film. The plot for the As-doped sample is overlaid as a comparison.

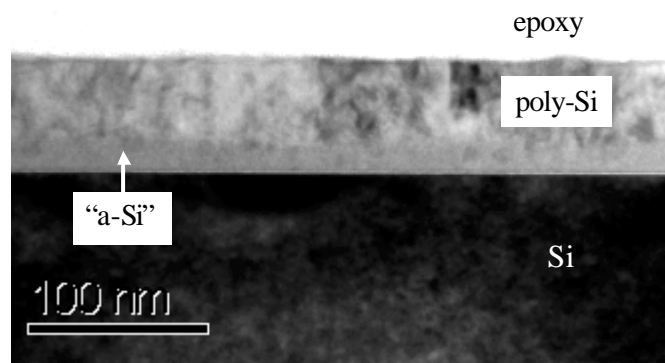
#### 7.4 TEM Studies of B-doped Single-layer a-Si Gates

Figure 7.17 is a cross-sectional transmission electron micrograph of the boron-implanted a-Si sample before laser irradiation. The surface is bonded to an epoxy layer for TEM sample preparation purposes. As can be seen, the gate oxide is virtually a thick line separating the a-Si gate and the crystalline substrate, and the a-Si gate appears to be featureless, consistent with expectations.



**Figure 7.17** Cross-sectional transmission electron micrograph of a boron-implanted a-Si sample prior to LTP.

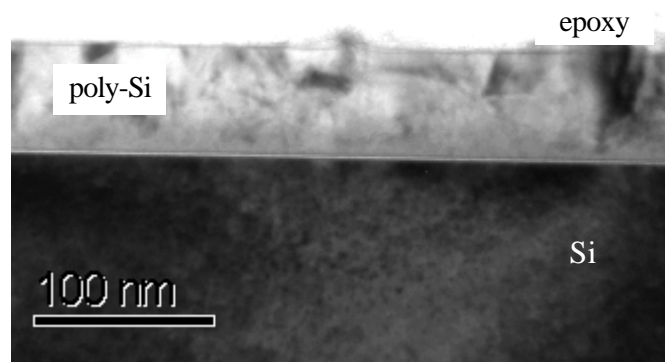
Figure 7.18 shows a bright-field TEM image of a cross-section of the boron-doped sample that was irradiated at a fluence of  $0.45 \text{ J/cm}^2$ . It is clear that for the bulk of the sample, poly-Si is formed upon solidification. However, it can be observed that near the gate/gate oxide interface, there exists a layer which is almost featureless.



**Figure 7.18** Bright-field TEM image of a cross-section of the boron-doped sample that was irradiated at a fluence of  $0.45 \text{ J/cm}^2$ .

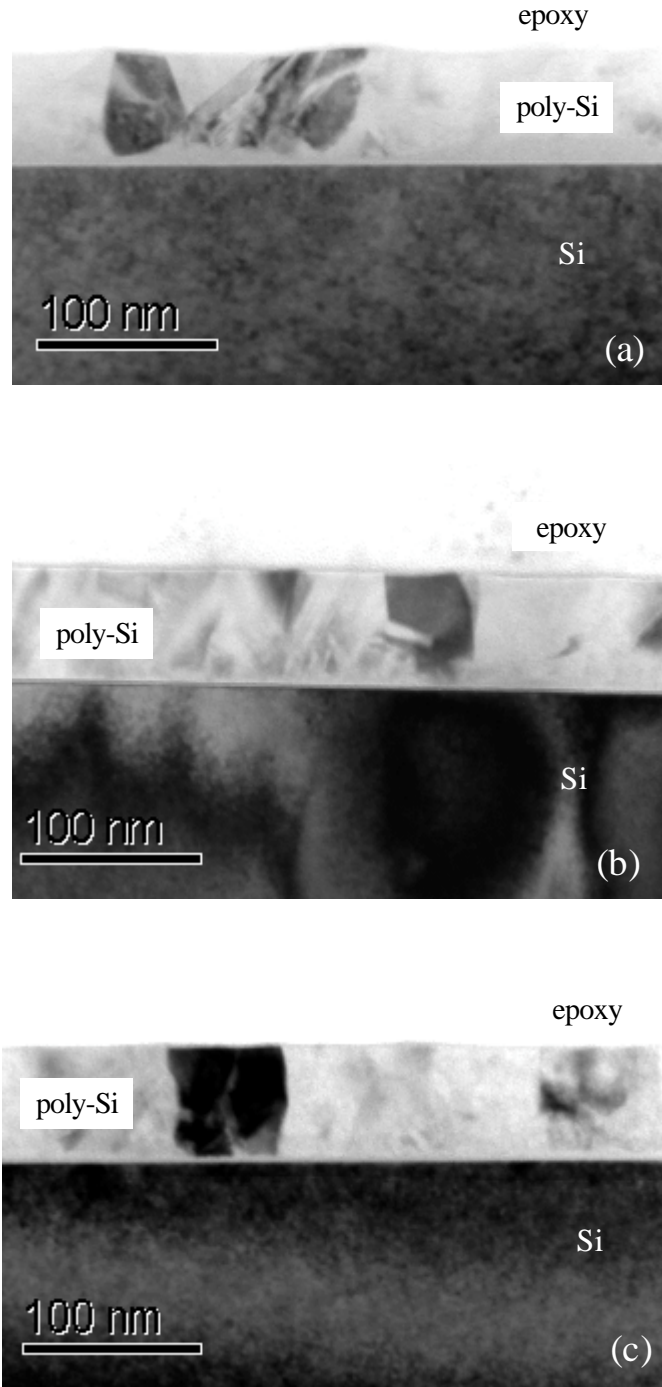
This featureless layer is not likely to be the original a-Si material that is not melted because the TRR results in Section 7.3.2 show that explosive crystallization has occurred after laser irradiation at  $E_l \sim 0.45 \text{ J/cm}^2$ , and that bulk of the sample has solidified into poly-

Si. Therefore, the featureless layer could be very fine-grained crystalline structures that are formed upon explosive crystallization at a high quench rate. It may even be a reformed a-Si layer since it is known that the termination stage of the explosive crystallization process is extremely fast. In addition, the possibility of the formation of a mixture of fine-grained poly-Si and a-Si cannot be dismissed. Similar observations are made for a sample that was irradiated at a slightly higher fluence of  $0.55 \text{ J/cm}^2$  (Fig. 7.19), except that the remnant “a-Si” layer is thinner and less obvious, indicating that the cooling rate is not as high compared to the sample after LTP at  $0.45 \text{ J/cm}^2$ .



**Figure 7.19** Bright-field TEM image of a cross-section of the boron-doped sample that was irradiated at a fluence of  $0.55 \text{ J/cm}^2$ .

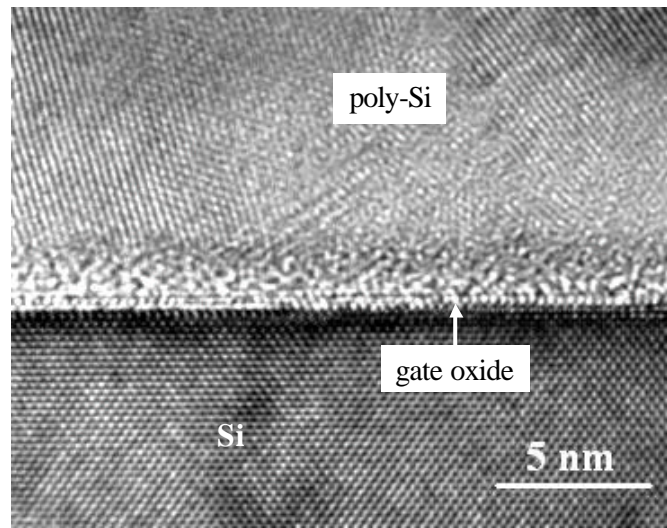
The XTEM images of a sample after LTP at  $0.75 \text{ J/cm}^2$ ,  $0.85 \text{ J/cm}^2$  and  $0.94 \text{ J/cm}^2$  are shown in Figs. 7.20(a), (b) and (c), respectively. For the sample exposed to LTP at  $0.75 \text{ J/cm}^2$ , the secondary melt has propagated to the gate/gate oxide interface, suggesting that appreciable melting has occurred. For samples after LTP at  $0.85 \text{ J/cm}^2$  and  $0.94 \text{ J/cm}^2$ , It is observed that the poly-Si grains are more well defined (columnar in nature) and the grains extend from the surface to the gate oxide. These results are in excellent agreement with our earlier interpretation of the TRR data.



**Figure 7.20** XTEM image of a cross-section of the boron-doped sample after LTP at (a)  $0.75 \text{ J/cm}^2$ , (b)  $0.85 \text{ J/cm}^2$  and (c)  $0.94 \text{ J/cm}^2$ .

Figure 7.21 depicts a HRTEM image of a cross-section of the boron-implanted a-Si sample upon LTP at  $0.94 \text{ J/cm}^2$ . It shows clear evidence of polycrystalline structures at the gate/gate oxide interface. These structures resulted from the full melt process, whereby poly-

Si is formed upon solidification.



**Figure 7.21** HRTEM image of a cross-section of the boron-implanted a-Si sample upon LTP at  $0.94 \text{ J/cm}^2$ .

## 7.5 Summary

We have demonstrated that a TiN/Ti capping layer can remarkably enhance the melt depth of poly-Si by virtue of the enhanced optical coupling. Our results clearly show that a thick a-Si layer can be formed upon LTP in the presence of Ti. In addition, we report the direct observation of the presence of buried melts during LTP of boron-implanted a-Si. The phase transformation mechanisms are elucidated using *in-situ* time-resolved reflectance measurements. The marked difference in the melt behavior of boron and arsenic-implanted a-Si samples are associated with the implantation-induced damage during gate ion implantation. It is found that the melt duration increases substantially when the a-Si film is completely melted. These observations provide important insights into the phase transformation mechanisms upon LTP of gate stacks.

# CHAPTER 8

## REDUCTION OF POLY-DEPLETION USING LASER THERMAL PROCESSING

### 8.1 Introduction

It is now well established that one major challenge in advanced CMOS gate engineering is to have adequate dopant activation at the gate/gate oxide interface to prevent poly-depletion, while preventing boron from penetrating through the gate oxide. In this chapter, electrical results that are obtained from C-V and I-V measurements of single or dual-layer gates are presented and discussed. In addition, the effects of LTP on the distribution of gate dopant atoms are investigated.

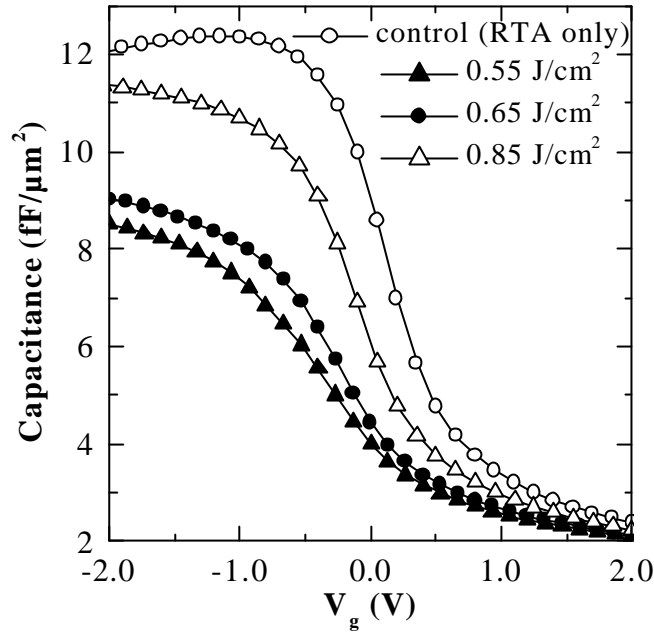
### 8.2 Results From P<sup>+</sup>-gated Capacitors (PCAP)

#### 8.2.1 LTP of single-layer PCAP

Figure 8.1 compares the high frequency (HF) C-V plots of the single-layer PCAP (with 18 Å gate dielectric) after RTA and after LTP alone. Since the polarities of the gate and the substrate are the same, the accumulation capacitance,  $C_{acc}$  is used to measure the degree of gate depletion (see Chapter 3 for details). From Fig. 8.1, it can be seen that the carrier concentration at the gate/gate oxide interface,  $N_{POLY}$ , increases (as evidenced by an increase in  $C_{acc}$ ) as fluence increases. This is due to an increase in melt depth and a corresponding increase in the gate activation with fluence. However, the  $N_{POLY}$  for the laser-processed samples (under the present fluence range) is not as high as that of the control sample, which was subjected to a RTA process at 1000 °C for 5 s. Similar observations

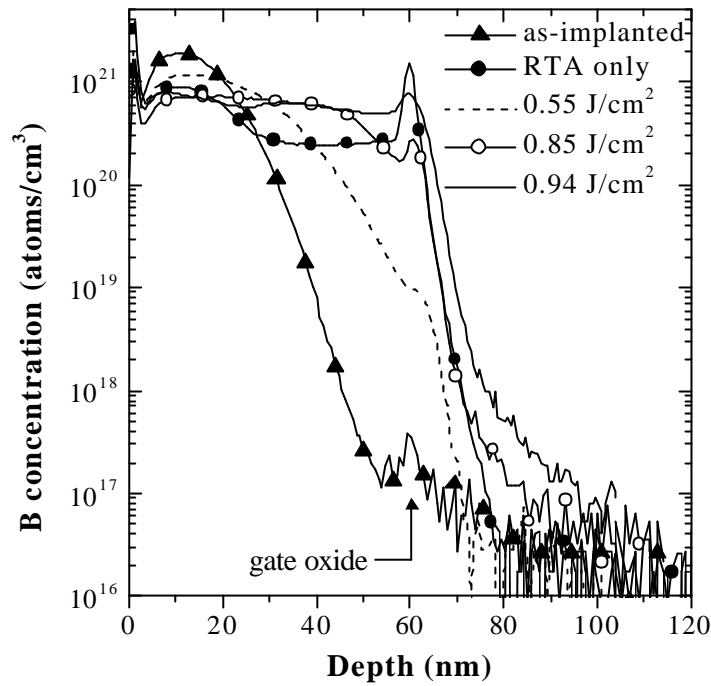


are made for single-layer PCAP with 26 Å gate oxide and thus the results are not shown.



**Figure 8.1** Comparison of high frequency C-V plots of single-layer PCAP after RTA (control sample) and after LTP alone.

The boron SIMS profiles of single-layer PCAP after laser irradiation at different fluences are shown in Fig. 8.2. It is observed that for fluences less than 0.94 J/cm<sup>2</sup>, boron is present near the gate/gate oxide interface even though the primary melt does not reach the gate oxide layer at such fluences (from the TRR data in Chapter 7). These profiles show that explosive crystallization has occurred ensuing the solidification of the primary melt, and boron is transported along with the secondary melt created. Since the duration of the secondary melt is directly proportional to fluence, the concentration of boron atoms near the Si/SiO<sub>2</sub> interface increases with fluence (Fig. 8.2). The near-uniform boron concentration profile across the poly-Si layer for the sample after 0.94 J/cm<sup>2</sup> LTP is evident that the entire a-Si film has melted (i.e. complete melt is reached).

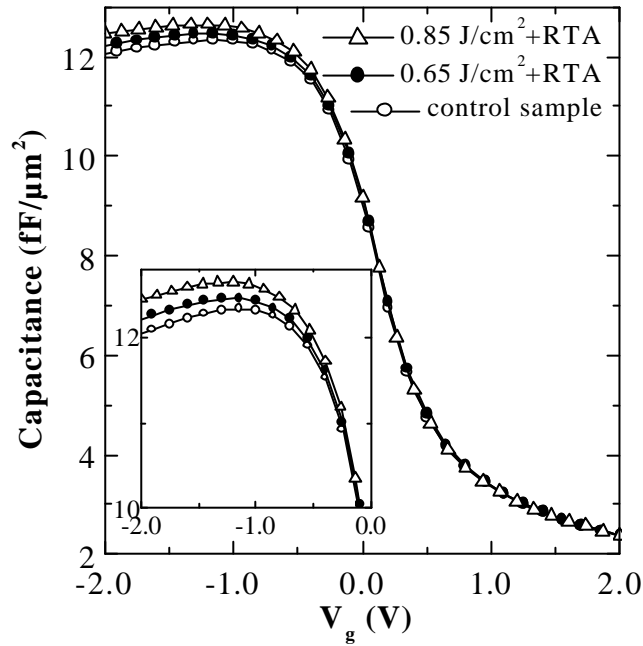


**Figure 8.2** SIMS depth profiles of boron in single-layer PCAP after LTP at different fluences.

From Fig. 8.2, it can also be seen that the boron concentration at the gate/gate oxide interface of the laser-processed samples (for  $E_l < 0.94 \text{ J/cm}^2$ ) is lower than that of the control sample. This corroborates the C-V data shown in Fig. 8.1. Furthermore, since the explosive crystallization process typically results in highly defective poly-Si, the boron atoms near the gate/gate oxide interface may not be adequately activated. This could be the reason why  $N_{\text{POLY}}$  of the single-layer PCAP after LTP alone is lower than that of the control sample. It should be noted that SIMS is not the most appropriate analytical method to observe the “boron penetration” phenomenon since there are ion-mixing effects during SIMS profiling. In addition, the ion-mixing effects are enhanced due to the considerably high concentration of boron atoms at the surface and at the near-surface regions.

### 8.2.2 Reduction of PDE in dual-layer PCAP

Figure 8.3 depicts the high frequency C-V plots of the dual-layer PCAP (with 18 Å gate dielectric) after the standard rapid thermal anneal or after a post-LTP RTA. The reduction of poly-depletion after a post-LTP anneal is clearly observed in the inset of Fig. 8.3, with the laser-processed samples having higher  $C_{acc}$  values than the control sample.



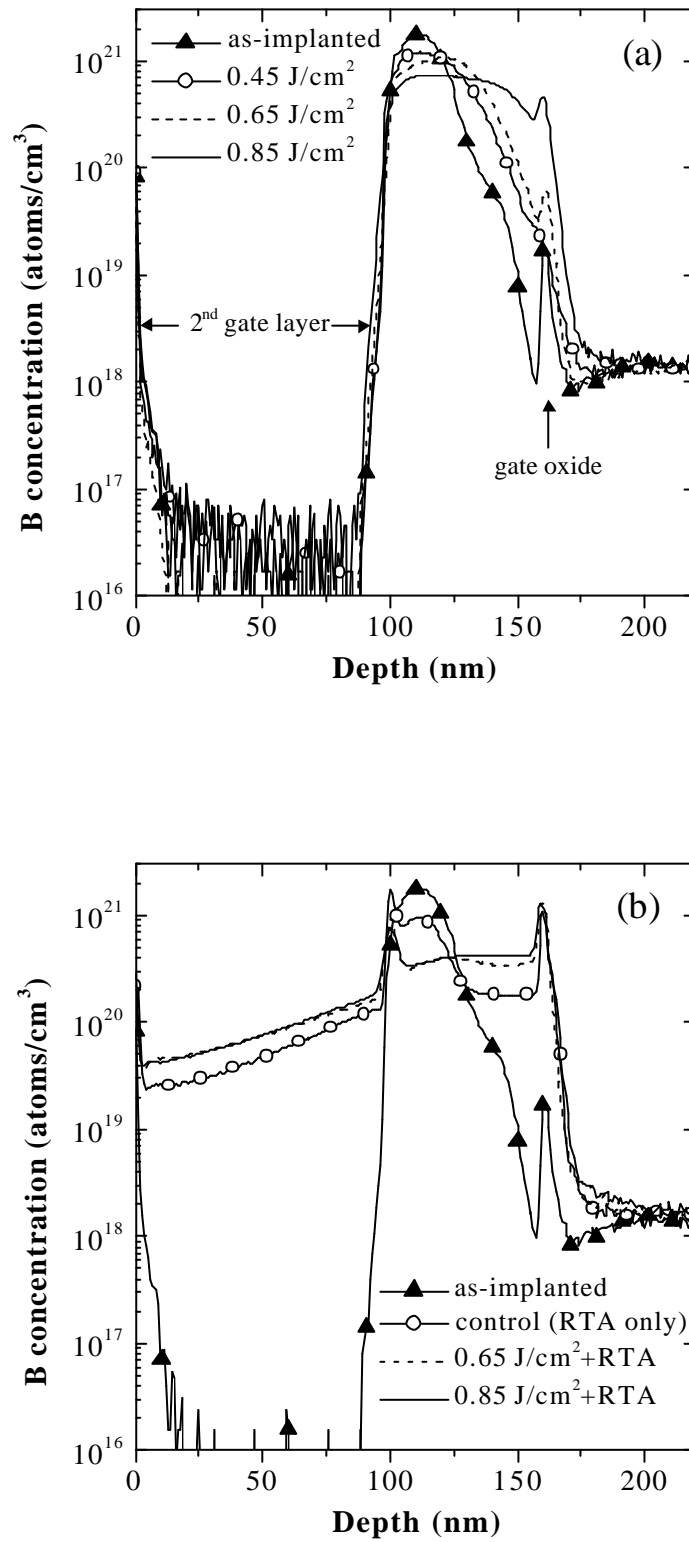
**Figure 8.3** HF C-V plots of the dual-layer PCAP after the standard RTA or after a post-LTP RTA. Inset is the enlarged view showing a reduction in PDE for the laser-processed samples.

The reduction of PDE (or an increase in  $N_{POLY}$ ) can be explained by considering the melt behavior of the samples. Upon LTP of single-layer a-Si gates, boron diffuses toward the gate oxide via explosive crystallization. However, these boron atoms may not be fully activated; this is particularly true for boron near the gate/gate oxide interface. To form the dual-layer PCAP, an additional layer of a-Si (1000 Å thick) was deposited onto the first

gate layer. When this dual-layer PCAP sample is subjected to the post-LTP anneal, the RTA further distributes (and activates) the boron atoms in both the first and second gate layers and also activates the boron atoms near the gate/gate oxide interface that were previously not activated by LTP alone. As a result, there is a substantial increase in  $N_{\text{POLY}}$  for the samples that were exposed to LTP prior to the gate activation anneal.

The effect of the standard RTA on the distribution of boron atoms in the dual-layer gates is shown in Fig. 8.4. In order to ease the comparison of the dopant distributions before and after RTA, the SIMS profiles of the dual-layer PCAP *before* it was subjected to the standard anneal (i.e. after LTP and deposition of the second gate layer) are also shown in Fig. 8.4 (a). From Fig. 8.4, it can be seen that the concentration of boron at the gate/gate oxide interface is consistently greater for samples that were subjected to LTP prior to the gate activation anneal. This shows that there are more dopants available for activation in the laser-processed samples compared to samples after RTA alone.

For the dual-layer PCAP control sample, the presence of a boron peak is observed after the standard anneal [Fig. 8.4(b)]. This immobile peak may be attributed to the formation of boron-interstitial clusters during the initial stage of RTA (analogous to the boron-point defect clustering in c-Si), revealing that the RTA is not able to “dissolve” the boron-interstitial clusters. In contrast, no such peak is detected for the samples after LTP +RTA, suggesting that the implantation-induced interstitials are annihilated in the laser-induced melt. Thus, there are no excess interstitials in the first gate layer to form boron clusters during the standard anneal. This allows more dopants to reach the gate/gate oxide interface during the post-LTP RTA.



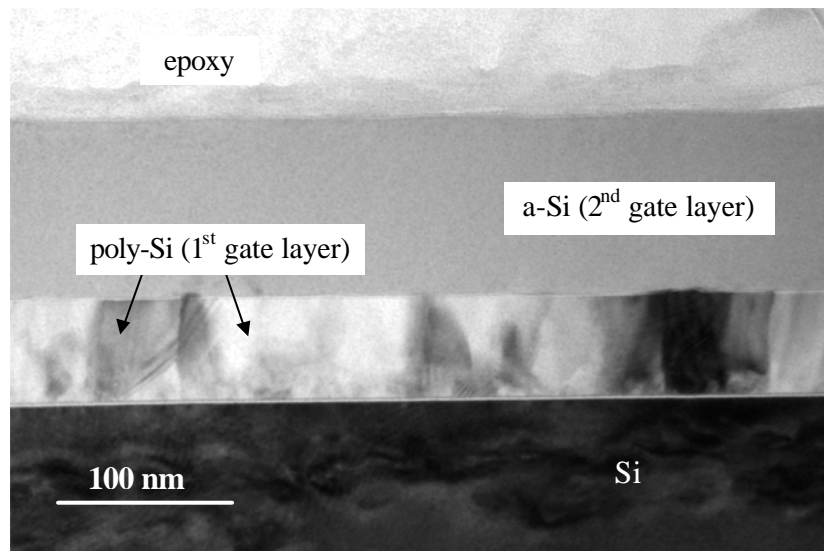
**Figure 8.4** Boron SIMS profiles in the dual-layer PCAP (a) after LTP of the first gate layer and (b) after RTA alone or LTP + RTA.

It is evident from Fig. 8.4 (b) that a substantial amount of boron atoms from the first gate layer diffuse to the second gate layer during the standard anneal, thus doping the second gate layer and making it electrically conductive. There is preferential upward diffusion of dopant atoms (i.e. toward the surface) than downward diffusion (i.e. toward the gate oxide) due to a large concentration gradient between the first and the second gate layer, which is essentially *undoped* a-Si.

The enhancement of boron counts/yield at a depth of ~100 nm indicates the presence of an interfacial oxide between the first and second gate layer. This is ascribed to the incomplete removal of the native oxide on the first gate layer prior to the deposition of the second gate layer. Since the interfacial oxide is very thin and is not continuous (see below for TEM analysis), it should not affect the electrical characteristics of the gate stack. Moreover, the substantial amount of boron atoms that penetrates through the interfacial oxide during the standard anneal should cause significant damage to the interfacial oxide such that it no longer serves as a perfect electrical insulator.

### **8.2.3 TEM studies of dual-layer PCAP**

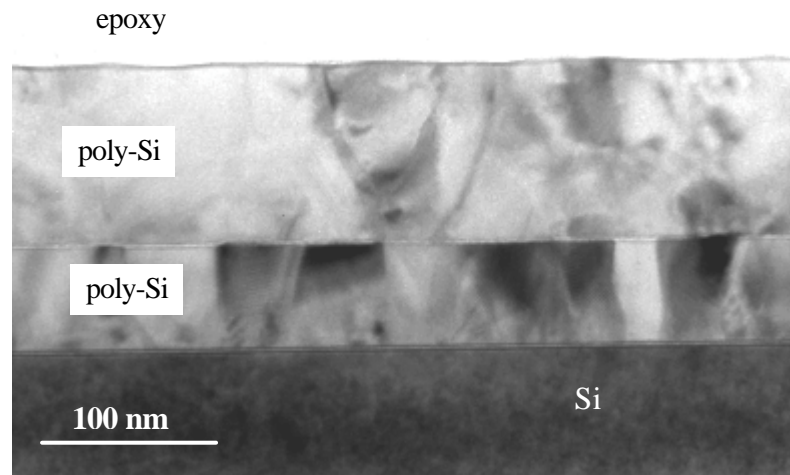
The bright-field TEM image of a cross-section of the dual-layer PCAP before it was subjected to the standard anneal is shown in Fig. 8.5. The first gate layer was exposed to LTP at  $0.85 \text{ J/cm}^2$  before the deposition of the second gate layer (refer to Fig. 8.4 (a) for the SIMS profile). The two gate layers are clearly delineated in Fig. 8.5, where it can be seen that the first gate layer is polycrystalline silicon and the as-deposited second gate layer is amorphous in nature.



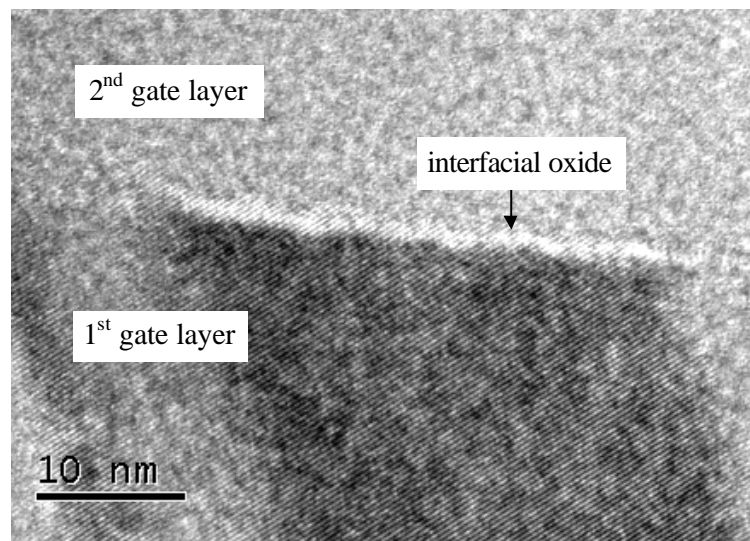
**Figure 8.5** Bright-field TEM image of a cross-section of the dual-layer PCAP before it was subjected to RTA. The first gate layer was exposed to LTP at  $0.85 \text{ J/cm}^2$  prior to the deposition of the second gate layer.

Subsequently, this dual-layer p+ poly-Si gate stack was subjected to a  $1000^\circ\text{C}$ , 5 s rapid thermal anneal. As shown in Fig. 8.6, there is no noticeable change in the microstructure of the first gate layer after the standard RTA. On the other hand, the second gate layer has fully crystallized into a poly-Si film. It is observed that the second gate layer comprises a mixture of fine and large-grained poly-Si, with large-grained poly-Si more predominant. The SIMS profile of this sample was depicted in Fig. 8.4 (b).

Figure 8.7 shows a HRTEM image of a cross-section of the dual-layer PCAP after  $0.85 \text{ J/cm}^2$  LTP + RTA, focussing on the interface between the first and the second gate layer. It is clear that an interfacial oxide exists between the first and the second gate layer, and this interfacial oxide is very thin and is not continuous. The second gate layer does not appear to be “crystalline” under high-resolution TEM because the grain orientation of the poly-Si is not aligned with the electron beam direction.



**Figure 8.6** XTEM image of the dual-layer p+ poly-Si gate stack after  $0.85 \text{ J/cm}^2$  LTP + RTA.

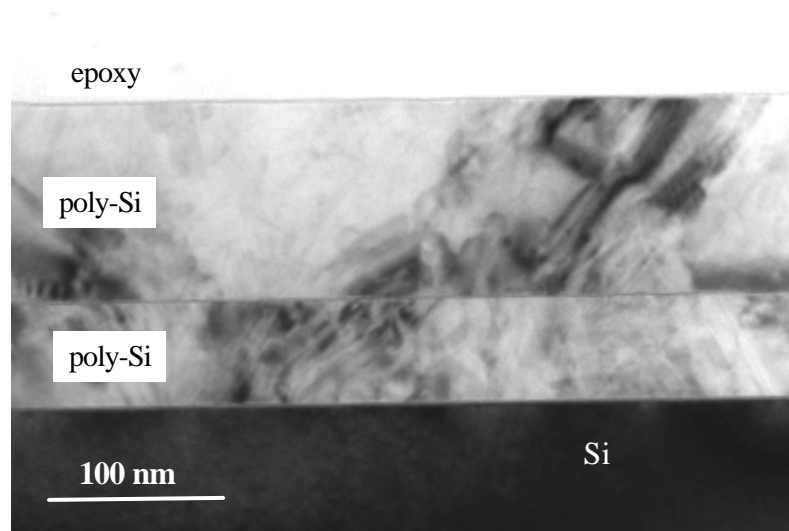


**Figure 8.7** HRTEM image of a cross-section of the dual-layer PCAP after  $0.85 \text{ J/cm}^2$  LTP+RTA, focussing on the interface between the first and the second gate layer.

Figure 8.8 is a cross-sectional transmission electron micrograph of the dual-layer PCAP after RTA alone (control sample). From Fig. 8.8, it can be observed that the control sample does not have a well-defined grain structure, but a rather non-uniform grain size distribution throughout the first and the second gate layers. This is largely attributed to the



random nucleation of c-Si during crystallization. Comparison of the gate microstructure of the dual-layer PCAP processed under different conditions shows that the gate microstructure plays an important role in the distribution of boron atoms. As can be seen from Fig. 8.6, the laser-processed sample has a regular columnar structure in the first gate layer as a result of laser-induced melt and crystallization. Such a gate microstructure promotes the diffusion of dopants toward the gate/gate oxide interface via grain boundary diffusion, leading to a further reduction in poly-depletion.

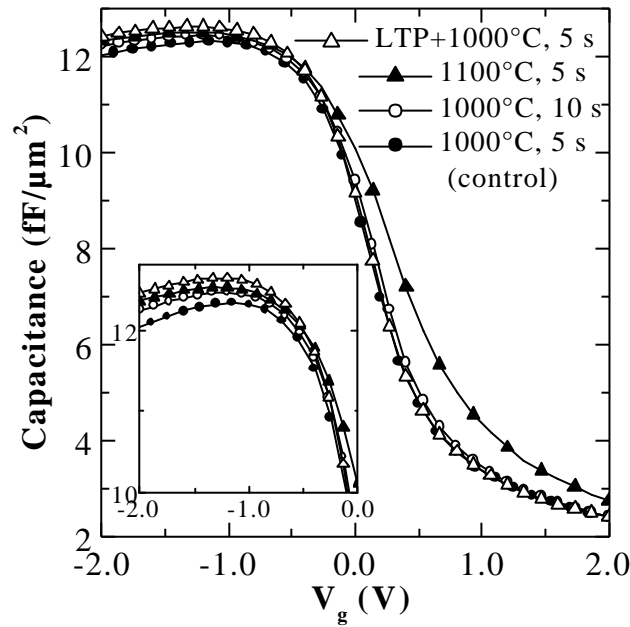


**Figure 8.8** Cross-sectional transmission electron micrograph of the dual-layer PCAP after RTA alone (control sample).

#### 8.2.4 Boron penetration in dual-layer PCAP

In order to investigate the effects of LTP and/or a high-temperature anneal on boron penetration, the dual-layer PCAP (without LTP) were subjected to various annealing conditions. The conditions were: RTA at 1000 °C for 10 s (twice the annealing duration of the control sample at the same temperature) and RTA at 1100 °C for 5 s (same duration as the control sample but at a higher temperature). The results are shown in Fig. 8.9. It is

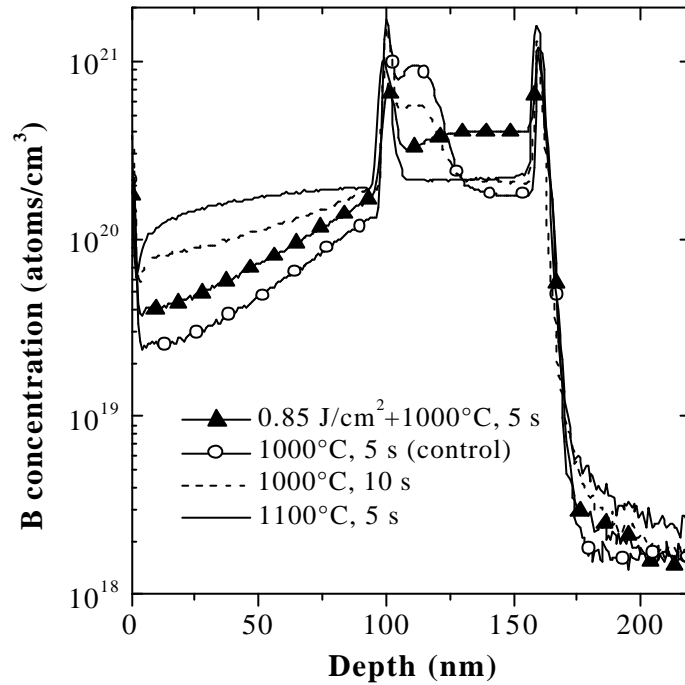
apparent that the flat band voltage,  $V_{FB}$  of the  $0.85 \text{ J/cm}^2$  LTP + RTA dual-layer PCAP is identical to that of the control sample, whereas a slight  $V_{FB}$  shift is observed for the sample annealed at  $1000^\circ\text{C}$  for 10 s. In contrast, a rapid thermal anneal at  $1100^\circ\text{C}$ , 5 s causes a large positive  $V_{FB}$  shift ( $\sim 130 \text{ mV}$ ), indicating severe boron penetration. The absence of observable  $V_{FB}$  shift gives a clear indication that boron penetration is negligible even after  $0.85 \text{ J/cm}^2$  LTP + RTA.



**Figure 8.9** C-V plots of dual-layer PCAP annealed under different conditions. RTA at  $1100^\circ\text{C}$ , 5 s causes a large positive  $V_{FB}$  shift, indicating severe boron penetration.

From the inset of Fig. 8.9, it can also be seen that for RTA alone,  $C_{acc}$  increases as the annealing duration/temperature increases, with an accompanying increase in  $N_{POLY}$ . This is reflected in the SIMS profiles illustrated in Fig. 8.10, where it is observed that the concentration of boron atoms near the gate/gate oxide interface increases with increasing annealing duration/temperature. For the sample after RTA at  $1000^\circ\text{C}$  for 10 s, a boron

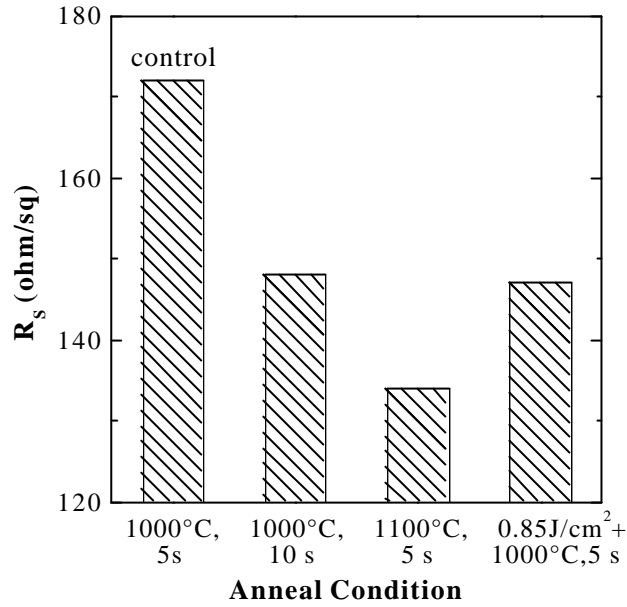
peak can still be detected (with a lower peak concentration than the control sample), indicating that the boron-interstitial clusters still exist. These clusters are fully dissolved by the 1100 °C, 5 s anneal. However, a large proportion of the boron atoms that are released upon dissolution diffuses to the second gate layer. Fig. 8.10 also shows that the boron concentration near the gate/gate oxide interface is highest in the 0.85 J/cm<sup>2</sup> LTP + RTA sample, in accordance with expectations.



**Figure 8.10** Boron SIMS profiles of the dual-layer PCAP after various annealing conditions.

Figure 8.11 compares the sheet resistance of the dual-layer p<sup>+</sup>-poly-Si gates annealed under different conditions. Although the  $R_s$  of the sample after 0.85 J/cm<sup>2</sup> LTP + RTA is comparable to that of the sample after the 1000 °C, 10 s RTA and is higher than that of the sample after the 1100 °C, 5 s anneal, it is considerably lower than that of the control

sample. This is due to the high degree of dopant activation in the first gate layer of the PCAP by the laser process.



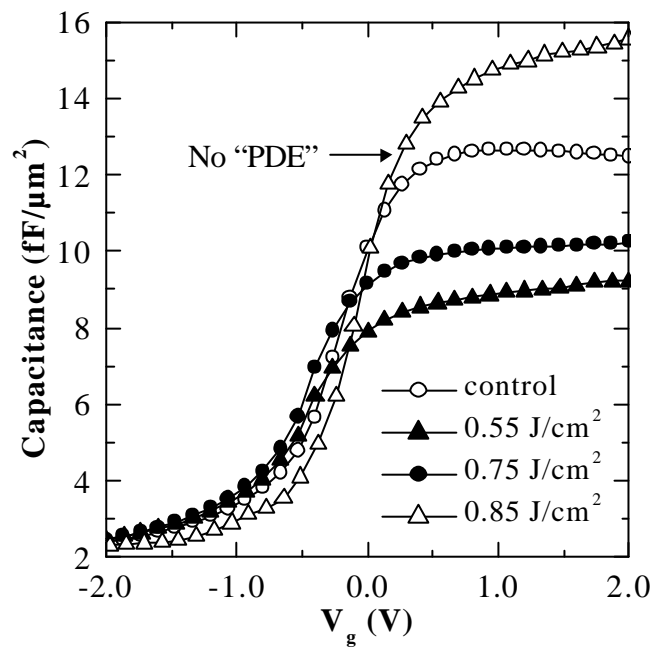
**Figure 8.11** Sheet resistance of the dual-layer PCAP annealed under different conditions.

### 8.3 Results From $N^+$ -gated Capacitors (NCAP)

#### 8.3.1 LTP of single-layer NCAP

The high frequency C-V curves of the NCAP (with 18 Å gate dielectric) after RTA (control sample) and after LTP at various fluences are shown in Fig. 8.12. It can be observed that  $C_{acc}$  of the laser-processed samples increases with an increase in the laser fluence,  $E_t$ . It is clear that for  $E_t < 0.85 \text{ J/cm}^2$ , the samples after LTP have lower  $N_{POLY}$  than the control sample, which received the 1000 °C, 5 s standard anneal. More importantly, the  $C_{acc}$  value of the NCAP upon LTP at  $0.85 \text{ J/cm}^2$  is substantially higher than that of the control sample, indicating a significant increase in the degree of the gate activation and  $N_{POLY}$  in this sample. By fitting the measured C-V curve of this NCAP to simulated curves

generated by a quantum mechanical C-V simulator [110], a good fit can only be obtained when the simulation does not consider the poly-depletion effect in the gate, with an equivalent oxide thickness (EOT) of  $\sim 1.9$  nm. This provides strong evidence that a near “depletion-free” n-type poly-Si gate has been formed upon a single-pulse LTP at  $0.85 \text{ J/cm}^2$ .



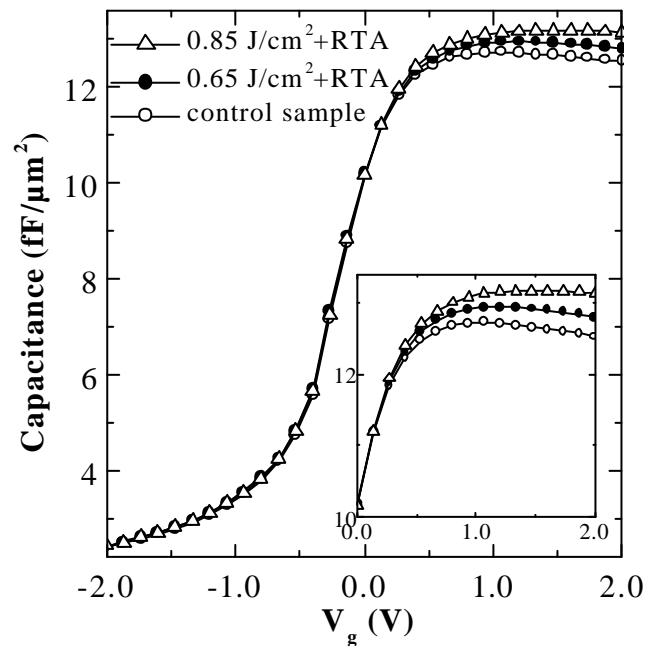
**Figure 8.12** HF C-V plots of the single-layer NCAP after LTP at different fluences.

The C-V plots in Fig. 8.12 can be interpreted as follows: for  $E_f < 0.85 \text{ J/cm}^2$ , the concentration of As atoms reaching the gate/gate oxide interface is insufficient to yield a  $N_{\text{POLY}}$  value greater than the control sample. This also applies to the case for the single-layer NCAP after LTP at  $0.75 \text{ J/cm}^2$ , where complete melting is expected to occur for an As-doped sample (from the TRR data in Chapter 7). Apparently, although a full melt is reached upon laser irradiation at this fluence, the melt duration may be insufficient to result in

extensive dopant activation. In contrast, at a fluence of  $0.85 \text{ J/cm}^2$ , the primary melt is able to penetrate easily through the entire a-Si gate layer. Under this condition, the melt duration is prolonged and the As atoms are evenly distributed throughout the primary melt (up to the gate/gate oxide interface). These As atoms become electrically active upon crystallization, with concentrations that are above solid solubility. As a result, a “depletion-free” NCAP is formed.

### 8.3.2 Reduction of PDE in dual-layer NCAP

The HF C-V plots of the dual-layer NCAP after processing at different conditions are depicted in Fig. 8.13. Similar to the case of dual-layer PCAP, it is evident from Fig. 8.13 that the PDE is reduced for samples that were exposed to LTP prior to the gate activation anneal.

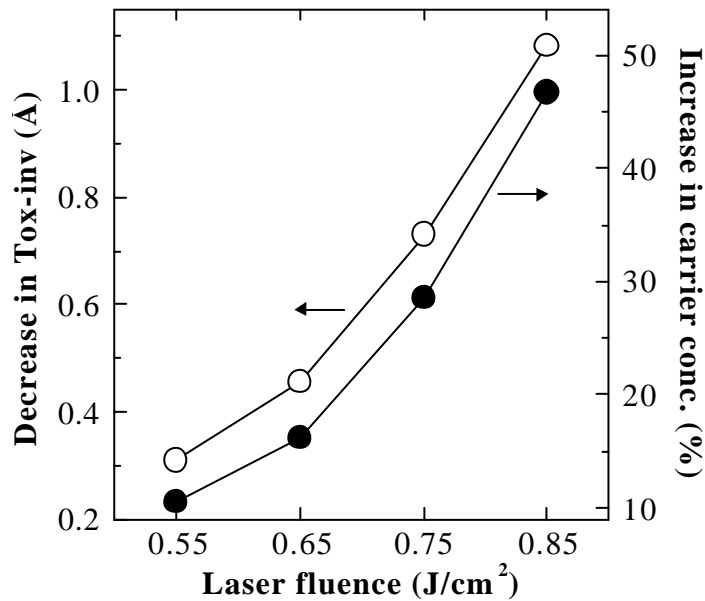


**Figure 8.13** C-V plots of the dual-layer NCAP after RTA or after a post-LTP anneal. Inset is the enlarged view showing a reduction in PDE for the laser-processed samples.

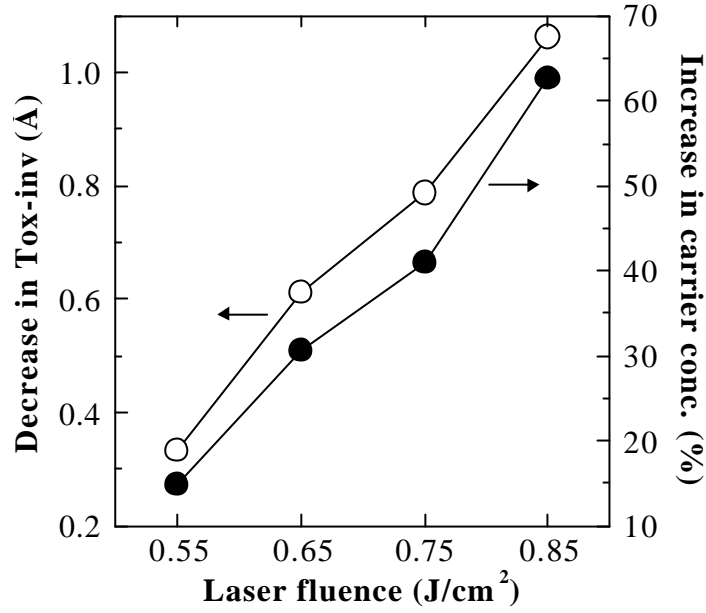
It should be realized that the  $C_{acc}$  for the NCAP that was processed at  $E_l \sim 0.85 \text{ J/cm}^2$  is reduced after the post-LTP RTA, indicating some deactivation of the arsenic atoms. However, the  $C_{acc}$  value is still higher than that of the control sample (as shown in Fig. 8.13) despite the As deactivation, suggesting that such a fluence level can still be used for the LTP of the dual-layer NCAP.

#### 8.4 Effect of LTP on Electrical Oxide Thickness

After extracting the  $N_{POLY}$  from the C-V data of both the dual-layer PCAP and NCAP, the corresponding electrical oxide thickness for a p-MOSFET or n-MOSFET in inversion region ( $T_{ox-inv}$ ) can be determined [84], and the results are shown in Figs. 8.14 and 8.15, respectively.



**Figure 8.14** Effect of a pre-RTA LTP on  $T_{ox-inv}$  and  $N_{POLY}$  for a p-MOSFET.



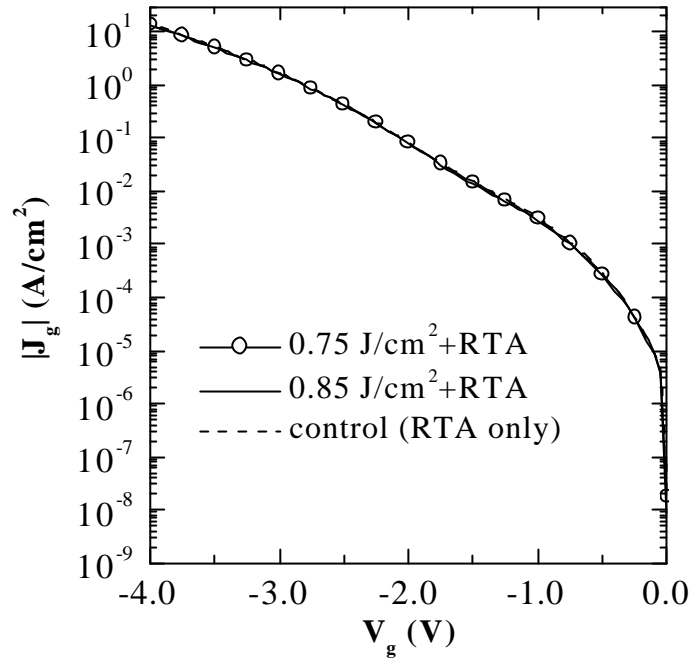
**Figure 8.15** Effect of a pre-RTA LTP on  $T_{\text{ox-inv}}$  and  $N_{\text{POLY}}$  for a n-MOSFET.

It is found that for the p-MOSFET, the  $0.85 \text{ J/cm}^2$  LTP + RTA process increases  $N_{\text{POLY}}$  by  $\sim 47\%$  and reduces  $T_{\text{ox-inv}}$  by  $\sim 1.1 \text{ \AA}$ , both with reference to the control sample. As for the n-MOSFET, the  $N_{\text{POLY}}$  increases by as high as nearly  $63\%$ . Such reductions in PDE will increase the drive current substantially.

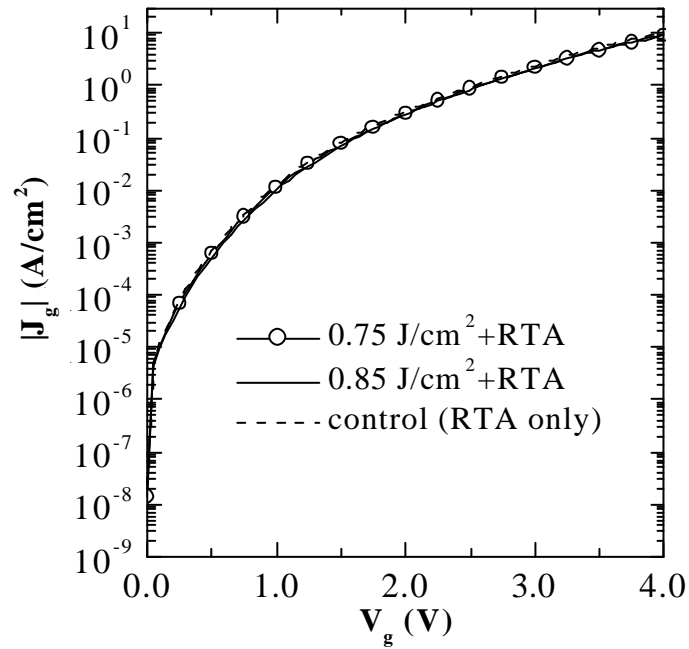
### 8.5 Effect of LTP on Gate Oxide Integrity

As there will be some concerns regarding the gate oxide integrity after LTP (especially if a complete melt is reached), we have conducted I-V measurements and time-dependent dielectric breakdown (TDDB) studies under constant voltage stressing for both the dual-layer PCAP and NCAP. Figures 8.16 and 8.17 show the gate leakage current density,  $J_g$  versus voltage plots of the dual-layer PCAP and NCAP, respectively (control and the LTP + RTA samples).





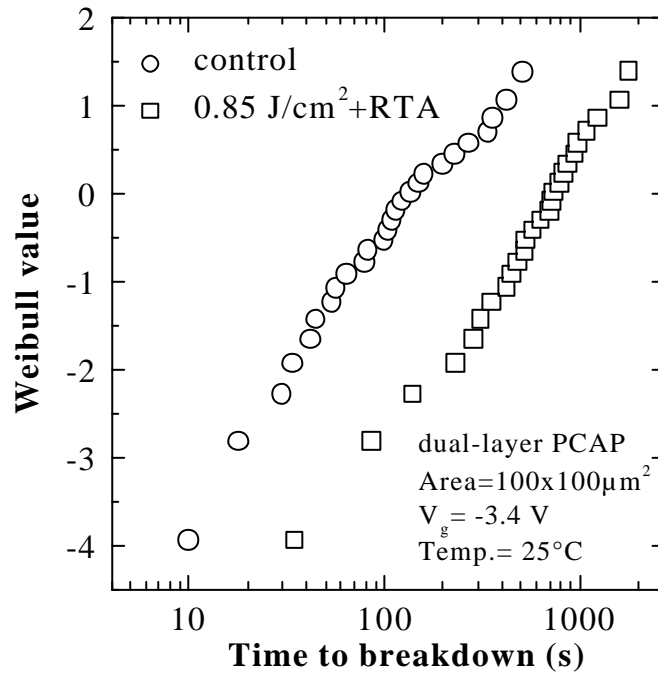
**Figure 8.16** Comparison of  $J_g$ - $V$  plots of dual-layer PCAP processed under different conditions.



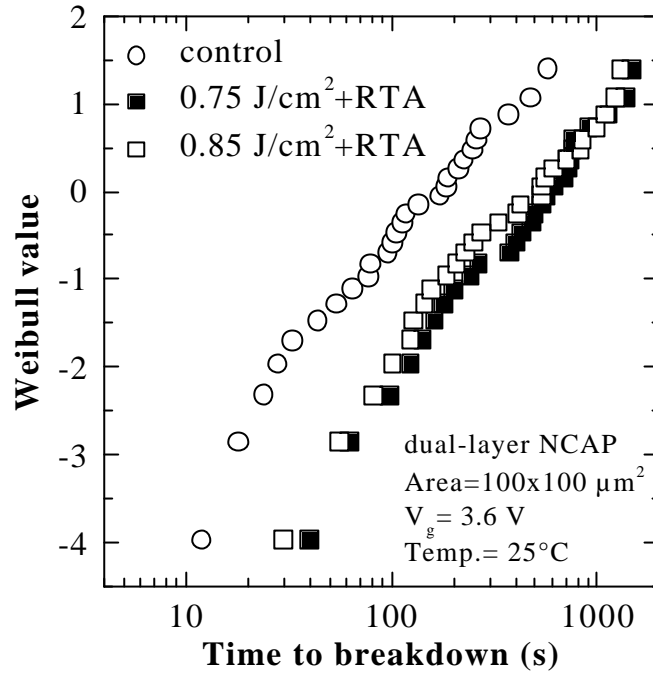
**Figure 8.17** Comparison of  $J_g$ - $V$  plots of dual-layer NCAP processed under different conditions.

From Figs. 8.16 and 8.17, it can be seen that the gate leakage characteristics of the dual-layer capacitors after LTP + RTA are similar to that of their respective control samples, indicating that the gate oxide quality is not degraded after LTP.

Figures 8.18 and 8.19 show the Weibull plots of TDDB data for the control and the LTP + RTA samples (dual-layer capacitors). As evident from these plots, the gate oxide reliability is not compromised even after LTP at such high fluences. This is also true for the  $0.85 \text{ J/cm}^2$  LTP + RTA dual-layer NCAP where a full melt is reached. In fact, it can be observed that the samples that have been subjected to a pre-RTA LTP require a longer time to reach breakdown, indicating an improvement in the gate oxide reliability. The mechanism for this improvement is not well understood at this point in time. It is possible that for the laser-processed samples, the interface roughness of the poly-Si/SiO<sub>2</sub> interface is reduced, thus enhancing the gate oxide reliability.



**Figure 8.18** Weibull plots of TDDB data for the control sample and the sample after  $0.85 \text{ J/cm}^2$  LTP + RTA (dual-layer PCAP).



**Figure 8.19** Comparison of Weibull plots of TDDB data for the control and LTP + RTA samples (dual-layer NCAP).

## 8.6 Summary

In summary, we have shown that LTP can be employed for the fabrication of highly-doped poly-Si gated MOS devices. We have successfully demonstrated that PDE in dual-layer PCAP and NCAP with ultra-thin gate dielectrics can be reduced considerably by subjecting the wafers to LTP prior to the gate activation anneal. For PCAP, this is achieved without observable boron penetration. The proposed mechanism for the increase in  $N_{\text{POLY}}$  is the diffusion of dopants toward the gate oxide via explosive crystallization. For single-layer NCAP, a “depletion-free” n-type poly-Si gate electrode has been formed when the laser fluence is high enough to cause complete melting. Constant voltage TDDB studies show that the gate oxide reliability is not degraded even after LTP at high fluences.

# CHAPTER 9

## CONCLUSIONS

### 9.1 Introduction

This chapter summarizes the major results and findings, and provides conclusions based on these findings in light of the objectives of this project. The important observations in this work are primarily categorized into two sections, namely, the formation of ultra-shallow junctions and laser thermal processing of gate stacks. Recommendations for further experimental work are also given in the last section of the chapter.

### 9.2 Formation of Ultra-shallow Junctions

The fabrication of ultra-shallow junctions for advanced CMOS devices proves to be a great challenge for the wafer fabrication industry. This is especially true when boron is used as a p-type dopant. Although significant channeling can be reduced when the ion implantation energy is reduced to the sub-keV regime, the silicon substrate should preferably be pre-amorphized to minimize channeling. Spike annealing with high ramp-up rates has been proposed to meet the stringent requirements for ultra-shallow junction formation due to its lower thermal budget as compared to conventional soak RTA. However, junctions produced by spike RTA are usually graded and are not suitable for the fabrication of source/drain extensions due to potential short channel effects.

On the other hand, laser thermal processing has shown great potential to be a good candidate in fabricating abrupt, highly activated and ultra-shallow  $p^+/n$  junctions. The superiority of LTP over spike RTA has been illustrated in Chapter 5. It is shown that the sheet resistance of the laser-annealed sample is considerably lower than that of the spike annealed sample, despite a junction depth difference of at least 200 Å. This is ascribed to the near-zero thermal budget of the laser process.

As shown in Chapters 4 and 6, although it is possible to melt the entire amorphous layer in the pre-amorphized silicon without melting the underlying substrate, a high density of residual defects remains in the recrystallized region. Furthermore, the EOR damage is not sufficiently annealed. These EOR defects can cause boron TED to occur during a post-LTP anneal. Since the EOR damage cannot be avoided if a PAI is performed, the melt depth should be extended to beyond the amorphous layer to minimize the dose of the excess interstitials in the NEOR region. We have demonstrated that by using a shallower PAI layer (where channeling is still prevented), the melt front can easily penetrate into the NEOR region to reduce the excess interstitials in the NEOR region. In this way, enhanced diffusion of boron can be significantly suppressed and the junction maintains its abruptness after the post-LTP anneal. As evident from the RBS and TEM results, LTP can virtually anneal all the crystal damages created by the PAI by over-melting into the substrate. The pre-amorphized layer recrystallizes to a single-crystalline structure via liquid phase epitaxy.

### 9.3 Laser Thermal Processing of Gate Stacks

In this study, it is found that a TiN/Ti capping layer can remarkably enhance the melt depth of poly-Si by virtue of the enhanced optical coupling. The results show that the solidification temperature and the growth dynamics are substantially modified by the presence of Ti atoms. As a consequence, a rather thick a-Si layer is formed upon LTP. Also, we report the direct observations of internal nucleation of melt during LTP of B-implanted a-Si. The phase transformation mechanisms are elucidated using *in-situ* time-resolved reflectance measurements. It has been shown that B-implanted a-Si has very different melting behavior compared to As-implanted a-Si. This is because the a-Si film may not be completely amorphous initially and the B implant only introduces damage in the a-Si film but does not cause amorphization.

In addition, we have demonstrated that LTP can be used for the formation of highly-activated poly-Si gated MOS devices. It is shown that the poly-depletion effect in dual-layer PCAP and NCAP with ultra-thin gate dielectrics can be reduced considerably by subjecting the wafers to LTP prior to the gate activation anneal. For PCAP, this is achieved without observable boron penetration. The proposed mechanism for the increase in  $N_{\text{POLY}}$  is the diffusion of dopants toward the gate oxide via explosive crystallization. This proposal is substantiated by the significant increase in the concentration of dopant atoms near the gate/gate oxide interface after the post-LTP anneal. For single-layer NCAP, a “depletion-free” poly-Si gate electrode has been formed when the laser fluence is sufficient to cause complete melting. Constant voltage TDDB studies show that the gate oxide reliability is not compromised even after LTP at high fluences.

## 9.4 Future Work

The investigations that were conducted in this project have opened up new avenues for future research work. They include:

- (i) Further optimization of the laser annealing technique by varying the substrate temperature. Since the cooling rate of the LTP is controlled by the temperature difference between the surface and the substrate, a higher substrate temperature would result in a lower cooling rate. This reduces the thermal stress induced in the substrate, especially near the corners of the shallow trench isolation (STI) regions. Another advantage of a lower cooling rate is to increase the melt duration to obtain concentration profiles with better uniformity. However, the substrate temperature should be maintained at below  $\sim 500$  °C to avoid unnecessary solid phase epitaxial growth.
- (ii) The study of laser annealing of ultra-shallow  $n^+/p$  junctions doped with  $As^+$  - to evaluate the feasibility of completing the fabrication of different polarity (i.e. arsenic and boron-doped) MOS devices on the same wafer. Hence, in future, the annealing of the S/D extensions of p-MOSFET and n-MOSFET will be carried out at the same processing stage.
- (iii) Delineation of junctions using advanced techniques such as scanning capacitance microscopy (SCM). The lateral distribution of dopants in semiconductor devices has an increasing effect on the device characteristics as the critical dimension decreases. It is thus necessary to acquire the two-dimensional (2-D) dopant profiles of actual devices. Current SIMS technique can only provide one-dimensional (1-D) profiling. A few experimental techniques have been explored to obtain 2-D information.

Differential etching of XTEM samples have yielded data in the mid  $10^{17}$  to  $10^{20}$  atoms/cm<sup>3</sup> range. However, this technique is very time consuming and difficult to control. Hence, SCM has been developed to give a more accurate analysis on 2-D dopant distribution.

- (iv) Performing LTP on CMOS transistors and compare the electrical characteristics of the laser-annealed devices with transistors that are annealed by spike RTA. Indicators of merits of LTP include the saturation current, sub-threshold leakage current and the extent of  $V_{th}$  roll-off.
- (v) Laser thermal processing of poly-SiGe gates. It is known that poly-SiGe can be used to tune the work function of the gate electrode. However, it is more difficult to activate arsenic atoms in poly-SiGe compared to boron-doped poly-SiGe films. Hence the PDE for n-MOSFET increases with increasing germanium content. It would be interesting to be able to obtain high dopant activation in boron-doped poly-SiGe. It would be even more challenging to activate arsenic-doped poly-SiGe gates using LTP. The conditions of the LTP can be optimized to form both the p-type and n-type poly-SiGe gates at the same processing stage. It is also possible to use complex schemes such as multiple laser pulses with varying fluences.



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## PUBLICATIONS AND PATENTS

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