HIGH MOBILITY

III-V COMPOUND SEMICONDUCTORS

FOR ADVANCED TRANSISTOR APPLICATIONS

CHIN HOCK CHUN

NATIONAL UNIVERSITY OF SINGAPORE

2010

HIGH MOBILITY

III-V COMPOUND SEMICONDUCTORS

FOR ADVANCED TRANSISTOR APPLICATIONS

CHIN HOCK CHUN

(B. ENG. (HONS.)), NATIONAL UNIVERSITY OF

SINGAPORE

A THESIS SUBMITTED

FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

DEPARTMENT OF

ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2010

Acknowledgements

First and foremost, I would like to express my earnest gratitude and appreciation to my research advisor, Dr. Yeo Yee Chia, for his guidance throughout my Ph.D. candidature at NUS. His knowledge and innovation in the field of semiconductor devices and nanotechnology has been truly inspirational. He has always been there to give insights into my research work and I have greatly benefited from his guidance.

I would also like to thank Associate Professor Ganesh S. Samudra for his advice and suggestions throughout the course of my research. Special thanks also go to Dr. Lee Hock Koon for his guidance and support while I was performing my experiments at Data Storage Institute. I have benefited greatly from his vast experience in semiconductor technology and process.

In addition, I am grateful to Professor Yoon Soon Fatt, Dr. Ng Tien Khee, Dr. Loke Wan Khai, and Dr. Satrio Wicaksono from Nanyang Technological University for their help and valuable discussion in the III-V epitaxy process.

I would also like to acknowledge the efforts of the technical staffs in Silicon Nano Device Laboratory (SNDL) specifically Mr Yong Yu Fu, Mr O Yan Wai Linn, Patrick Tang, Lau Boon Teck, and Sun Zhiqiang in providing technical and administrative support for my research work. Appreciation also goes out to Institute of Materials Research, and Engineering (IMRE) and Institute of Microelectronics (IME) for the use of their equipments for materials characterization.

I am also grateful for the guidance and discussions from the many outstanding researchers and graduate students of SNDL. Special thanks to Dr.

Zhu Ming for mentoring me during the initial phase of my research for the fabrication of III-V devices. Special thanks also go to Gong Xiao for his tireless support in device fabrication and measurements during the crucial conference deadlines. I would also like to thank Lina Fang, Shao Ming, Kian Ming, Rinus, Andy Lim, Alvin Koh, Fangyue, Hoong Shing, Manu, Shen Chen, Lanxiang, Ivana, Sujith, Xingui, Huaxin, Zhu Zhu, Xinke, and many others for their useful discussions, assistance and friendships throughout my candidature.

I would like to extend my greatest gratitude to my family who has always encouraged my academic endeavors. Last but not least, I am also very grateful for the support, care and encouragement of my wife, Hui Qi, throughout all these years. The sacrifices that you have made in the support of my academic pursuits will never be forgotten. Thank you for your love and devotion.

High Mobility III-V Compound Semiconductors

For Advanced Transistor Applications

Acknowledgements i

Table of Contents iii

Abstract vi

List of Figures viii

List of Symbols xix

Chapter 1. Introduction

1.1 Background 1
1.2 Emerging Channel Materials for Extending CMOS 2
1.2.1 Carbon Nanotube 2
1.2.2 Graphene 3
1.2.3 Nanowire 4
1.2.4 Germanium 5
1.3 Why III-V Compound Semiconductors? 5
1.4 Challenges of III-V MOSFET Technology 8
1.4.1 Formation of High-Quality Gate Stack 9
1.4.2 Material Integration on Si Substrate 11
1.4.3 Channel Material and Engineering 12
1.4.4 Device Structure 13
1.4.5 Formation of Low Resistance Source/Drain Regions 14
1.5 Objective of Research 15
1.6 Thesis Organization 16
1.7 References 18

Chapter 2. *In-situ* Surface Passivation and Metal-Gate/High-*k* Dielectric Stack Formation for III-V MOSFETs

2.1 Introduction 29
2.2 III-V Channel N-MOSFETs with *In-situ* SiH_4 Passivation 32
2.2.1 GaAs N-MOSFET with *In-situ* SiH_4 Passivation 33
2.2.2 $In_{0.18}Ga_{0.82}As$ N-MOSFET with *In-situ* SiH_4 Passivation 48
2.3 III-V Channel N-MOSFETs with *In-situ* SiH_4 + NH_3 Passivation 57
2.3.1 GaAs N-MOSFET with *In-situ* SiH_4 + NH_3 Passivation 57
2.3.2 InGaAs N-MOSFET with *In-situ* SiH_4 + NH_3 Passivation 65
2.4 InGaAs N-MOSFETs with *In-situ* SiH_4 + NH_3 Passivation and Tetrafluoromethane (CF_4) Plasma Treatment 74

2.4.1 Experiment 75
2.4.2 Results and Discussion 75
2.4.3 Summary 81
2.5 Summary 81
2.6 References 82

Chapter 3. Lattice Mismatched $In_{0.4}Ga_{0.6}As$ Source/Drain Stressors with *In-situ* Doping for Strained $In_{0.53}Ga_{0.47}As$ Channel N-MOSFETs

3.1 Introduction 91
3.2 Device Concepts and Fabrication 93
3.2.1 Channel Strain Engineering By Lattice-Mismatched Source/Drain Stressors 93
3.2.2 Process Development of Selective InGaAs Epitaxy with *In-situ* Doping 99
3.2.3 Device Fabrication 103
3.3 Device Characterization and Analysis 105
3.4 Summary 111
3.5 References 113

Chapter 4. III-V Multiple-Gate Field-Effect-Transistors (MuGFETs) with High Mobility $In_{0.7}Ga_{0.3}As$ Channel and Epi-Controlled Retrograde-Doped Fin

4.1 Introduction 117
4.2 Device Concepts 119
4.3 Device Fabrication 124
4.4 Device Characterization and Analysis 128
4.5 Summary 133
4.6 References 134

Chapter 5. Nanoheteroepitaxy of Gallium Arsenide on Strain-Compliant Silicon-Germanium Nanowires

5.1 Introduction 137
5.2 Experiment 138
5.3 Device Characterization and Analysis 145
5.3.1 Compliance in Nanostructures and Simulation 145
5.3.2 Growth of Gallium Arsenide on $Si_{0.35}Ge_{0.65}$ Islands or Nanowires 152
5.4 Summary 158
5.5 References 160

Chapter 6. Conclusion and Future Work

6.1 Conclusion 164
6.2 Contributions of This Thesis 165
6.2.1 *In-situ* Interfacial Engineering for High Quality MOS Stack Formation 165
6.2.2 Source/Drain Doping and Channel Strain Engineering for Performance Enhancement 166

6.2.3 Multiple-Gate Transistor Structure with Retrograde-Channel Doping for Reduced Short Channel Effects 166
6.2.4 Nanoheteroepitaxy of Gallium Arsenide on Strain-Compliant Silicon-Germanium Nanowires for Material Integration 167
6.3 Future Directions 167
6.3.1 Passivation Studies on Other High Mobility III-V Materials 168
6.3.2 Source/Drain and Channel Strain Engineering 168
6.3.3 Hetero-integration of Other High Mobility III-V Materials on Si Substrates 169
6.3.4 III-V P-Channel Devices 169
6.4 References 167

Appendix
A. List of Publications 173

Abstract

High Mobility III-V Compound Semiconductors

For Advanced Transistor Applications

by

CHIN Hock Chun

Doctor of Philosophy – Electrical and Computer Engineering

National University of Singapore

The continual geometrical scaling of Si MOSFET into nanoscale regime for improved device performance and density is rapidly approaching its fundamental limitations. Fundamental changes to the materials and device structures are deemed to hold great promises for the evolution of future CMOS technologies. High mobility III-V compound semiconductors have received renewed interest as alternative materials to replace conventional Si or strained Si channels and to be heterogeneously integrated on Si or silicon-on-insulator (SOI) substrates for advanced CMOS technology beyond the 22 nm technology node.

To take full advantage of the III-V, a gate dielectric process technology that provides good interfacial properties is required. In this thesis, effective and highly manufacturable passivation technology based on a multiple chamber MOCVD system was demonstrated. The key characteristics of these new *in-situ* passivation technologies using silane (SiH_4), silane and ammonia (SiH_4+NH_3), and post-gate dielectric deposition treatment in tetrafluoromethane (CF_4) plasma were determined and identified. Technology demonstrations in various III-V MOSFETs exhibit good transistor

characteristics. This affirms the effectiveness of the designed concept for interface engineering for native oxide reduction.

Further enhancement of III-V MOSFETs by the integration of *in-situ* doped lattice-mismatched S/D stressors for source/drain (S/D) doping and channel strain engineering is also investigated. This work explores novel $In_{0.53}Ga_{0.47}As$ N-channel MOSFET with *in-situ* doped $In_{0.4}Ga_{0.6}As$ S/D regions. The high S/D doping concentration, achieved by the *in situ* doping process, further reduces S/D series resistance (R_{SD}) for additional performance improvement. In addition, the lattice mismatch between $In_{0.4}Ga_{0.6}As$ S/D and $In_{0.53}Ga_{0.47}As$ channel is exploited to induce tensile strain in the channel for mobility enhancement.

For achieving better electrostatic control than planar FETs, novel InGaAs multiple-gate FET (MuGFET) or FinFET for enhanced carrier mobility, and an epi-controlled retrograde-doped fin to suppress short channel effects is explored. Transistor output characteristics with high saturation drain current and transconductance were obtained. In addition, significant improvement in the short channel effects, such as drain-induced barrier lowering (DIBL), as compared to planar MOSFETs was achieved.

In addition, a new method of forming GaAs on a Si-based substrate through selective migration-enhanced epitaxy (MEE) of GaAs on strain-compliant SiGe nanowire structures was reported. Good material property and growth selectivity were realized. This new III-V integration scheme may be promising for integrating high speed transistors and optoelectronic devices with advanced electronic circuits on Si platform.

List of Figures

Fig. 1.1 Mobility versus composition *x* for $In_xGa_{1-x}As$ compound semiconductors. The mobility increases with higher Indium composition. ---------- 7

Fig. 1.2 Effective mass m^* versus composition *x* for $In_xGa_{1-x}As$ compound semiconductors. The effective mass decreases with higher Indium composition, leading to higher mobility in Fig. 1.1. ---------- 7

Fig. 1.3 Bandgap E_G versus composition *x* for $In_xGa_{1-x}As$ compound semiconductors. InGaAs offers wide range of bandgap from 0.36 eV to 1.42 eV. ---------- 8

Fig. 1.4 Schematic illustration of the key technical challenges faced in the realization and integration of high mobility III-V channel MOSFET on Si substrates for future logic applications. ---------- 9

Fig. 2.1 Schematic illustration of the key process steps in the *in-situ* passivation technology based on a multiple chamber MOCVD gate cluster system. The high vacuum transfer module serves to minimize native oxide formation during wafer transfer. After pre-gate cleaning, the III-V wafers were quickly loaded into the gate cluster system for native oxide decomposition, surface treatment, and MOCVD high-*k* dielectric deposition at three different chambers. ---------- 31

Fig. 2.2 Summary of various in-situ surface passivation schemes and the III-V compound semiconductors investigated in each scheme. ---------- 32

Fig. 2.3 Process sequence employed in transistor fabrication. The *in-situ* vacuum anneal and SiH_4 interface passivation steps are performed before MOCVD high-*k* dielectric deposition. ---------- 34

Fig. 2.4 Schematic illustration of the two-mask transistor structure with gate and contact layers. The transistor width *W* is 100 µm. ---------- 35

Fig. 2.5 *C-V* characteristics of GaAs MOS capacitors formed using various process conditions. In (i), PDA of 500 °C was used, but no *in-situ* passivation was performed. In other samples, PDA temperatures of (ii) 500 °C, (iii) 550 °C, and (iv) 600 °C, were used together with *in-situ* vacuum anneal and SiH_4 passivation. ---------- 38

Fig. 2.6 Frequency dispersion of *C-V* characteristics as a function of PDA temperature for GaAs MOS capacitors. D_{it} attained at various PDA temperatures is depicted in the inset. ---------- 38

Fig. 2.7 C-V forward- and reverse sweeps for capacitors with and without *in-situ* surface passivation and at various PDA temperatures. *In-situ* surface passivation is important for minimizing hysteresis. --- 39

Fig. 2.8 A summary of hysteresis and frequency dispersion for a variety of FGA conditions for GaAs MOS capacitors. --------- 40

Fig. 2.9 D_{it} of the capacitors processed at different FGA conditions was extracted using the conductance method. About 30 % reduction in D_{it} can be achieved by using FGA at 400 °C for 10 min..--- 40

Fig. 2.10 Co-implantation of Si^+ with P^+ can boost the activation of Si as N-type dopants in GaAs. 35 % reduction in sheet resistance can be achieved. The sheet resistance was evaluated by using TLM test structures.-------------------------- 42

Fig. 2.11 PdGe contacts exhibit excellent ohmic I-V characteristics at different contact spacings (50, 100, 200, 300, and 400 μm) after contact formation at 400 °C for 10 s. ----------------------- 42

Fig. 2.12 Specific contact resistivity ρ_C at various formation temperatures was extracted using TLM test structures. The measured total resistance R_T versus contact spacing d is plotted in the inset. --- 43

Fig. 2.13 Schematic and TEM pictures showing the key features of the GaAs N-MOSFET fabricated in this experiment: TaN/HfAlO gate stack formed with *in-situ* surface passivation process as well as a PdGe ohmic contact technology. An oxidized Si interfacial layer (~ 1 nm) was formed between HfAlO dielectric and GaAs. EDX analysis of the contact region reveals the composition of PdGe ohmic contact. A Ge layer was epitaxially grown on the GaAs surface by solid phase regrowth during contact formation. --- 44

Fig. 2.14 (a) I_{DS}-V_{GS} curves of a surface channel GaAs MOS transistor with self-aligned S/D and L_G of 3 μm, showing good output characteristics. Inset plots the transconductance characteristics of the GaAs device. (b) I_{DS}–V_{DS} characteristics of the GaAs N-MOSFET at various gate overdrives. -- 45

Fig. 2.15 Gate-to-bulk capacitance C_{GB} versus V_G and gate-to-channel capacitance C_{GC} versus V_G characteristics of a GaAs transistor.--- 46

Fig. 2.16 Plot of effective carrier mobility μ_{eff} as a function of inversion charge density N_{inv} for a surface channel GaAs N-MOSFET. -- 47

Fig. 2.17 High resolution XRD rocking curve of the (004) reflection on the $In_{0.18}Ga_{0.82}As/GaAs$ structure. The clear interference pattern in the rocking curve reveals the high interface quality of the InGaAs structure. --- 49

Fig. 2.18 AFM images of (a) GaAs before InGaAs growth, showing RMS surface roughness of 1.1 Å. (b) After the growth of $In_{0.18}Ga_{0.82}As$, the RMS surface roughness is 1.3 Å. ----------- 50

Fig. 2.19 As 3*d* XPS spectra show the significant reduction in As-O bond signal after vacuum anneal and SiH_4 treatment.---------- 52

Fig. 2.20 Si 2*p* spectra verify the existence of Si-O bond at the interface in the samples with vacuum anneal and SiH_4 passivation, indicating that the thin Si interfacial layer was oxidized. -- 52

Fig. 2.21 HRTEM micrographs showing the cross-section of a completed TaN/HfAlO/InGaAs stack: (a) without, and (b) with vacuum anneal and SiH_4 passivation. In the samples with vacuum anneal and SiH_4 treatment, an oxidized silicon layer was observed. Diffractogram in the inset reveals excellent crystalline quality of the strained $In_{0.18}Ga_{0.82}As$ layer. --- 53

Fig. 2.22 *C-V* characteristics of TaN/HfAlO/InGaAs MOS capacitors characterized at frequencies of 10 kHz, 100 kHz and 1 MHz. Significant reduction in frequency dispersion was achieved with SiH_4 passivation.--- 54

Fig. 2.23 Hysteresis versus SiH_4 treatment temperature ranging from 300 ˚C to 500 ˚C. -- 54

Fig. 2.24 D_{it} at various SiH_4 treatment temperatures. D_{it} as low as 3.5 × 10^{11} to 5.0 × 10^{11} $cm^{-2}eV^{-1}$ can be achieved with additional SiH_4 treatment. -- 55

Fig. 2.25 The gate leakage current density J_G obtained at $V_G = V_{FB}$ - 1 V as a function of EOT. -- 56

Fig. 2.26 *C-V* characteristics of GaAs MOS capacitors with and without SiH_4 + NH_3 passivation and before an implant anneal to simulate dopant activation process. *C-V* characteristics of a Si capacitor without implant anneal are also plotted for comparison. The SiH_4 + NH_3-passivated GaAs capacitor reveals electrical behavior comparable to Si capacitor. -- 59

Fig. 2.27 *C-V* characteristics of SiH_4 + NH_3-passivated GaAs MOS capacitors before and after anneal. D_{it} of GaAs MOS

capacitors with and without SiH_4 + NH_3 passivation at various implant anneal conditions was summarized in inset. - 60

Fig. 2.28 High-resolution XPS spectra reveal the bonding structure at the HfAlO/GaAs. (a) As 3*d* spectra show the suppression of As-O bond after passivation, contributing to the improved interfacial quality. (b) Si 2*p* spectra show that SiO_xN_y interlayer was formed with the SiH_4 + NH_3 passivation, while SiO_x was formed with the SiH_4-only passivation.------- 61

Fig. 2.29 (a), (b) TEM micrographs of a GaAs MOSFET with L_G of 160 nm and gold-free PdGe contact. (c) Top SEM image of the GaAs transistor.-- 62

Fig. 2.30 I_D-V_G characteristics of SiH_4 + NH_3-passivated GaAs N-MOSFETs with L_G of 250 nm, showing good output characteristics. Inset plots the I_{DS}–V_{DS} curves of the GaAs device at various gate overdrives. --------------------------------- 63

Fig. 2.31 I_D-V_G characteristics of SiH_4 + NH_3-passivated GaAs N-MOSFETs with L_G of 2 μm, showing good output characteristics. Inset plots the I_{DS}–V_{DS} curves of the GaAs device at various gate overdrives. The GaAs transistor demonstrates excellent saturation and pinch-off characteristics.-- 63

Fig. 2.32 Plot of μ_{eff} versus E_{eff} for a GaAs N-MOSFET. After correction for presence of interface trap charges, the peak electron mobility is ~1920 cm^2/Vs. The inset shows the simulated and measured inversion *C-V* characteristics of the GaAs N-MOSFET. -- 64

Fig. 2.33 AFM images of InGaAs surfaces (a) before vacuum annealing, and after vacuum anneal at (b) 520 °C for 60 s, and (c) 600 °C for 60 s. The AFM scan area is 2.5 μm by 2.5 μm. Severe degradation of surface roughness was observed after vacuum anneal at 600 °C for 60 s, and is attributed to the evaporation of indium. -------------------------- 66

Fig. 2.34 Cross-sectional TEM images of the TaN/HfAlO/InGaAs stacks: (a) without and (b) with vacuum anneal and SiH_4 + NH_3 passivation. Inset reveals the existence of thin SiO_xN_y interfacial layer between HfAlO and InGaAs in the sample with vacuum anneal and SiH_4 + NH_3 passivation.-------------- 67

Fig. 2.35 (a) As 3*d* XPS spectra show the elimination of As-O bond after SiH_4 + NH_3 passivation. (b) With additional vacuum baking and SiH_4 + NH_3 passivation, In-O bond at the interface was suppressed, as illustrated by the deconvoluted components of the In 3*d* XPS spectra. (c) Si 2*p* spectrum of the SiH_4 + NH_3-passivated sample verifies the existence of

Si-O and Si-N bonds, indicating the formation of a thin SiO_xN_y interfacial layer. -- 68

Fig. 2.36 I_{CP}/f versus V_{base} for $In_{0.53}Ga_{0.47}As$ N-MOSFETs with and without SiH_4 + NH_3 passivation for rise and fall time of gate pulses ranging from 100 ns to 1000 ns. Constant-amplitude trapezoidal gate pulse train was swept from accumulation to inversion level for interface characterization. Higher I_{CP} in the control devices indicates the presence of more interface states available for trapping-detrapping. ------------------------ 70

Fig. 2.37 A gentler slope in I_{CP}/f as a function of $\ln[(t_r \cdot t_f)]$ indicates a lower D_{it} level as seen from equation (2-5). The mean D_{it} of the $In_{0.53}Ga_{0.47}As$ N-MOSFETs with and without SiH_4 + NH_3 passivation were extracted to be 6.5×10^{11} cm^{-2}eV^{-1} and 4.2×10^{12} cm^{-2}eV^{-1}, respectively. --------------------------- 70

Fig. 2.38 (a) I_D–V_G curves reveal that SiH_4 + NH_3 passivation leads to significant improvement in the subthreshold characteristics of InGaAs N-MOSFETs. (b) I_D-V_D output characteristics of the same pair of transistors showing excellent saturation and pinch-off characteristics.-- 72

Fig. 2.39 Cumulative distribution of the SS of InGaAs N-MOSFETs with and without SiH_4 + NH_3 passivation. The SiH_4 + NH_3 passivation technology reduces SS by more than 300 mV/decade. -- 72

Fig. 2.40 Plot of I_{off} versus I_{Dlin} showing significant reduction in I_{off} for $In_{0.53}Ga_{0.47}As$ MOSFET with SiH_4 + NH_3 passivation. The reduction in I_{off} is attributed to the improvement in SS due to D_{it} reduction. -- 73

Fig. 2.41 I_{off} versus I_{Dsat} showing of InGaAs N-MOSFETs with and without SiH_4 + NH_3 passivation. Similar reduction in I_{off} was also achieved in $In_{0.53}Ga_{0.47}As$ MOSFET with SiH_4 + NH_3 passivation. --- 73

Fig. 2.42 (a) Cross-sectional TEM micrograph showing a F-treated MOCVD HfAlO gate dielectric formed on a SiH_4 + NH_3-passivated surface in a $In_{0.53}Ga_{0.47}As$ MOSFET. A thin SiO_xN_y interfacial layer between HfAlO and InGaAs was observed. (b) Diffractogram reveals excellent crystalline quality of the $In_{0.53}Ga_{0.47}As$ epilayer. (c) Strong peak in the F 1*s* spectrum reveals the incorporation of fluorine in the HfAlO film after ICP CF_4 plasma treatment. This peak is absent in the control sample. -------------------------------------- 76

Fig. 2.43 SIMS profile reveals the elemental distribution of the TaN/HfAlO/InGaAs stack with SiH_4 + NH_3 passivation and

F treatment. F tends to pile up at the $HfAlO/SiO_xN_y$ interface after PDA. ---------- 77

Fig. 2.44 (a) I_D–V_G and (b) I_D–V_D output characteristics of $In_{0.53}Ga_{0.47}As$ N-MOSFETs with and without F treatment. The F-passivated transistor demonstrates improvement in subthreshold characteristics and drive current. ---------- 78

Fig. 2.45 Cumulative distribution of (a) SS, and (b) hysteresis of InGaAs N-MOSFETs with and without ICP CF_4 plasma treatment. Fluorine passivation leads to smaller SS, indicating reduced interface states in the MOS stack, and improved hysteresis, indicating the reduced number of bulk oxide traps. ---------- 78

Fig. 2.46 Electron mobility μ_e as a function of inversion charge density N_{inv}. Improvement of carrier mobility at high field could be attributed to reduced number of interface traps. Inversion *C-V* characteristics indicate that the InGaAs MOSFETs have identical EOT of 3.2 nm. ---------- 80

Fig. 2.47 Plot of off-state leakage I_{off} versus on-state saturation drain current I_{Dsat} showing significant reduction in I_{off} for $In_{0.53}Ga_{0.47}As$ MOSFET with additional F passivation. The reduction in I_{off} is attributed to the improvement in subthreshold swing due to improved gate stack quality. ---------- 80

Fig. 3.1 Schematic illustration of the channel resistance (R_{Ch}) and the source/drain resistance (R_{SD}) of a transistor. The total resistance (R_{Total}) of the transistor is the summation of these resistance components. R_{Total} of the transistor is drastically reduced by high mobility InGaAs channel and additional channel strain engineering for R_{Ch} reduction and *in-situ* doping in the S/D regions for R_{SD} reduction. ---------- 92

Fig. 3.2 Lattice constants of GaAs, $In_xGa_{1-x}As$, and InAs. The lattice constant of $In_xGa_{1-x}As$ can be tuned by varying the composition of indium. ---------- 95

Fig. 3.3 Schematic illustration of a strained N-channel $In_{0.53}Ga_{0.47}As$ transistor with lattice-mismatched $In_{0.4}Ga_{0.6}As$ S/D stressors. The $In_{0.4}Ga_{0.6}As$ stressor stretches the $In_{0.53}Ga_{0.47}As$ lattice at both the horizontal and vertical heterojunctions, as shown in the inset. ---------- 95

Fig. 3.4 Finite element simulation obtained the distribution of (a) lateral strain ε_x and (b) vertical strain ε_y in the strained $In_{0.53}Ga_{0.47}As$ channel. The S/D recess depth is 15 nm, and the separation between the $In_{0.4}Ga_{0.6}As$ source and drain regions is 200 nm. ---------- 97

Fig. 3.5 Average lateral strain ε_x and vertical strain ε_y in the transistor channel within top 5 nm from the gate dielectric-$In_{0.53}Ga_{0.47}As$ interface at various gate lengths. Both strain components increase in magnitude with smaller gate length, and can be exploited for performance scaling. ------------------ 98

Fig. 3.6 (a) Indium composition and temperature are key factors affecting the growth. SEM images showing film quality and growth selectivity under different epitaxy conditions. (b) Huge lattice mismatch leads to three-dimensional growth of InGaAs dots. (c) Two-dimensional growth of InGaAs layer was achieved with smaller lattice mismatch. (d) Higher temperature enables the desorption of nucleated seeds on the gate lines to achieve selective growth. -------------------------- 100

Fig. 3.7 The well-defined InGaAs peak in the high resolution XRD indicates high crystalline quality of the InGaAs epilayer. The composition of indium in the InGaAs epilayer was determined to be ~40 %.--- 101

Fig. 3.8 Cross-sectional TEM micrographs showing (a) an $In_{0.53}Ga_{0.47}As$ transistor structure with SiON dummy gate and selective grown $In_{0.4}Ga_{0.6}As$ structures on the S/D regions, and (b) a zoomed-in view of a region in (a) which shows raised $In_{0.4}Ga_{0.6}As$ S/D structure and SiON dummy gate. The recess depth is about 20 nm and the thickness of $In_{0.4}Ga_{0.6}As$ stressor is 70 nm. (c) A high resolution zoomed-in view of a region showing the heterojunction highlighted in (a). Pseudomorphic epitaxy of $In_{0.4}Ga_{0.6}As$ on $In_{0.53}Ga_{0.47}As$ was achieved in this MOCVD process. ----- 102

Fig. 3.9 Comparison of sheet resistance of N-type InGaAs layer formed by *in-situ* SiH_4 doping process and by Si^+ implantation and dopant activation. The sheet resistance is extracted using TLM test structure. *In-situ* SiH_4 doping process leads to significant reduction in R_{SD} for enhanced transistor performance.-- 103

Fig. 3.10 Process sequence employed in transistor fabrication. The $In_{0.53}Ga_{0.47}As$ recess etch and $In_{0.4}Ga_{0.6}As$ selective epitaxy steps are introduced to replace S/D implant step in the fabrication process.-- 104

Fig. 3.11 (a) I_D–V_D, and (b) I_D–V_G characteristics showing current enhancement in the $In_{0.53}Ga_{0.47}As$ N-MOSFET with *in-situ* doped $In_{0.4}Ga_{0.6}As$ S/D regions over a control $In_{0.53}Ga_{0.47}As$ N-MOSFET. Both devices have a gate length of 200 nm. The control N-MOSFET has $In_{0.53}Ga_{0.47}As$ S/D regions.------ 106

Fig. 3.12 R_{Total} as a function of V_G for strained $In_{0.53}Ga_{0.47}As$ N-MOSFET with *in-situ* doped $In_{0.4}Ga_{0.6}As$ S/D regions and

control $In_{0.53}Ga_{0.47}As$ N-MOSFET. L_G is 200 nm and V_D is 0.1 V. Higher S/D doping level in N-MOSFET with *in-situ* doped $In_{0.4}Ga_{0.6}As$ S/D regions gives a reduced series resistance. Inset shows the extracted R_{SD} at V_G of 3 V. -------- 107

Fig. 3.13 Linear $G_{m,ext}$ versus V_G of strained and control devices at V_D of 0.1 V. The inset plots the extracted peak linear $G_{m,int}$ of both strained and control devices. The 28 % improvement in peak $G_{m,int}$ is due to improvement in carrier mobility. ------ 108

Fig. 3.14 (a) Schematic illustrating the extraction of $G^S_{m,int}$, $G^C_{m,int}$, $G^T_{m,ext}$ to analyze the contributions from carrier mobility and R_{SD} to total $G_{m,ext}$ enhancement, using equations 3-3, and 3-4. (b) By comparing among $G^S_{m,ext}$, $G^C_{m,ext}$, and $G^T_{m,ext}$, the contribution from carrier mobility and R_{SD} can be separated. - 110

Fig. 3.15 Plot of off-state leakage I_{OFF} versus on-state saturation drain current I_{Dsat} showing significant enhancement in I_{Dsat} for $In_{0.53}Ga_{0.47}As$ MOSFET with *in-situ* doped $In_{0.4}Ga_{0.6}As$ S/D over control MOSFET. --- 111

Fig. 4.1 Three-dimensional schematic of N-channel InGaAs MuGFET, comprising high mobility InGaAs channel with indium composition of 70 %, and precise epi-controlled retrograde-doped fin structure. ------------------------------------ 118

Fig. 4.2 Three-dimensional mesh grid of the InGaAs MuGFET structure used in the device simulation. In the channel region of the transistor, a mesh with tight grid spacing of 1 nm near the oxide-III-V interface is used as the carrier distribution gradient in the inversion layer is steep. The grid spacing is relaxed gradually towards the bulk. ------------------ 120

Fig. 4.3 Band diagram of conduction band (E_C) along the MuGFET at y = 2 nm and 20 nm from the top surface and at the center of the fin with W_{fin} = 220 nm, as illustrated in the top schematic. --- 121

Fig. 4.4 Distribution of electrostatic potential in the fin region of InGaAs with V_G of 1.2 V applied to (a) $G_T + G_{S1} + G_{S2}$, (b) G_T only. V_D of 1.2 V was applied to both cases. Inset shows the position along A-A' of the fin for the analysis. -------------- 122

Fig. 4.5 Distribution of current density in the fin region of InGaAs with V_G = 1.2 V and V_D = 1.2 V applied to (a) G_T, G_{S1} and G_{S2}, and (b) G_T only. I_{Top} and $I_{Side1} + I_{Side3}$ were obtained by integrating the current densities over the regions, as illustrated in (a). Inset shows the position along A-A' of the fin for the analysis. -- 123

Fig. 4.6 Process sequence employed in transistor fabrication. A gate last fabrication approach was used in this device demonstration.-- 125

Fig. 4.7 Schematic illustration of the key process steps in the MuGFET fabrication. (a) Dummy photo resist (PR) gate pattern was used to define the S/D regions during Si^+ implantation. (b) Fin lithography was then performed before a Cl_2-based plasma etch to define the InGaAs fins with a H_{Fin} of 100 nm. This also removed the N^+ regions surrounding the fins. (c) After surface passivation and high-k dielectric deposition, TaN metal gate was reactively sputtered and patterned.-- 126

Fig. 4.8 HRXRD shows well-defined $In_{0.7}Ga_{0.3}As$ and $In_{0.55}Ga_{0.45}As$ peaks, indicating high crystalline quality of the epilayers. ---- 127

Fig. 4.9 SIMS profile reveals the elemental distribution of Be in the $In_{0.7}Ga_{0.3}As/In_{0.55}Ga_{0.45}As$ stack. The high Be concentration at the surface is an artefact. -- 127

Fig. 4.10 (a) SEM image shows the top view of a fabricated MuGFET with TaN gate electrode, $In_{0.7}Ga_{0.3}As$ channel and PdGe ohmic contacts. (b) TEM micrograph showing the cross-sectional view of the InGaAs MOSFET along B-B', as indicated in the SEM image in (a). (c) TEM micrograph showing the cross-sectional view of the InGaAs fin structure along A-A', as indicated in (a). The InGaAs fin structure has a W_{Fin} of 220 nm and H_{Fin} of 100 nm. ---------------------------- 129

Fig. 4.11 I_D–V_G transfer characteristics of $In_{0.7}Ga_{0.3}As$ N-MuGFET with retrograde p-type $In_{0.55}Ga_{0.45}As$ fin. ------------------------ 130

Fig. 4.12 I_D–V_D output characteristics of the InGaAs N-MuGFET in Fig. 4.11. -- 131

Fig. 4.13 DIBL versus channel width of the InGaAs transistors with retrograde channel doping. DIBL decreases with the reduction of channel width, indicating improved electrostatic control of the channel. --- 132

Fig. 4.14 DIBL of $In_{0.7}Ga_{0.3}As$ N-MuGFETs with retrograde doping as a function of L_{CH}.--- 132

Fig. 5.1 Schematic illustrating the process flow for the fabrication of SGOI substrate using two-steps Ge condensation process at 1050 °C and 900 °C. Cyclical oxidation and annealing performed at 900 °C serve to improve the distribution of the Ge in the SiGe layer. -- 140

Fig. 5.2 SEM top view of the SiGe layer formed by Ge condenstation process (a) without, (b) with second stage of cyclical oxidation and annealing at 900 °C. The cyclical step significantly improves the surface morphology.----------- 141

Fig. 5.3 The well-defined SiGe peak in the high resolution XRD indicates high crystalline quality of the SiGe layer. The composition of Ge in the SiGe layer was determined to be ~65 %.--- 142

Fig. 5.4 AFM surface scanning of a completed SGOI substrate after oxide removal. The SGOI substrate exhibits low RMS roughness of ~0.44 nm.-- 142

Fig. 5.5 TEM images showing film quality and growth selectivity under different epitaxy temperatures at (a) 525 °C, (b) 580 °C, and (c) 625 °C. Higher temperature enables the desorption of nucleated seeds on the SiO_2 to achieve selective growth. Diffractogram in the inset of (a) reveals that the GaAs grown on SiO_2 is polycrystalline.---------------- 144

Fig. 5.6 (a) When a GaAs layer is grown on a planar SiGe layer or a large SiGe island with limited or no compliance, the GaAs epilayer is deformed or strained, whereas the SiGe layer is relaxed. In this case, as shown in (b), a high level of strain energy is stored in the GaAs epilayer as lateral compression and vertical tension. (c) The substrate compliance effect in SiGe nanowire structure enables both the nanowire and the epilayer to be deformed. The mismatched strain energy is thus distributed between the epilayer and nanowire, as shown in (d). The reduced strain energy accumulated in the epilayer suppresses the formation of defects.-------------------- 146

Fig. 5.7 Finite element simulation obtained the distribution of (a) lateral strain ε_x and (b) vertical strain ε_y in the GaAs/$Si_{0.35}Ge_{0.65}$ heterostructure with *W* of 100 nm. The magnitude of ε_x and ε_y is the highest at the heterojunction and decreases away from the heterojunction.-------------------- 149

Fig. 5.8 Finite element simulation obtained the distribution of (a) lateral strain ε_x and (b) vertical strain ε_y in the GaAs/$Si_{0.35}Ge_{0.65}$ heterostructure with *W* of 1 µm. Both ε_x and ε_y are larger than the structure with *W* of 100 nm, as shown in Fig. 5.7. Inset shows the location of the GaAs/$Si_{0.35}Ge_{0.65}$ heterostructure for this analysis. ------------- 150

Fig. 5.9 Finite element simulation of (a) lateral strain ε_x and (b) vertical strain ε_y as a function of depth from the GaAs surface *y* in a GaAs/$Si_{0.35}Ge_{0.65}$ heterostructure formed on SiO_2. The thicknesses of the GaAs and SiGe layers are 20 nm and 100 nm. The width *W* of GaAs/SiGe nanostructure

is varied (100 nm, 200 nm, 500 nm, and 2 μm). The strain in GaAs is significantly reduced for narrower structures. ----- 151

Fig. 5.10 (a) SEM image showing the top view of a layer of GaAs grown on planar SiGe-on-insulator structure. Island formation for stress relief results in a rough GaAs surface. The cross-sectional TEM image in (b) is a zoomed-in view of a region in (c) which shows nucleation of GaAs islands on the SiGe surface. Defects such as stacking faults and dislocations are clearly observed in these GaAs islands and at the interface between GaAs and SiGe. These defects relieve the stress due to lattice mismatch at the GaAs/SiGe heterojunction. -- 153

Fig. 5.11 (a) SEM image showing the top view of a $Si_{0.35}Ge_{0.65}$ nanowire with a width of 75 nm and a GaAs layer grown on it. Cross-sectional TEM micrographs in (b) and (c) show that the GaAs layer is pseudomorphically grown on SiGe. The GaAs lattice is well-aligned to the $Si_{0.35}Ge_{0.65}$ lattice and with no observable defects such as APDs or stacking faults. - 154

Fig. 5.12 Room temperature photoluminescence spectrum of GaAs on SiGe nanowire. Interference fringes can be observed, and are attributed to multiple reflections within the multi-layer structure, indicating abrupt and flat interface.------------------- 155

Fig. 5.13 Micro-Raman spectra of GaAs grown on planar SiGe-on-insulator structure and SiGe nanowire structure. The red shift in the Si-Si, Si-Ge, and Ge-Ge mode phonons in the nanowire structure, as compared to planar structure, indicates that the SiGe nanowire is under tensile strain.------- 156

Fig. 5.14 (a) Direct, and (b) differential AES spectra at five locations as shown in SEM micrograph in the inset. Both Ga-LMM and As-LMM were detected in the nanowire regions (locations 1, 2 and 3), confirming the existence of GaAs on the nanowire. Neither Ga nor As was detected in the SiO_2 regions (locations 4 and 5), indicating the high selectivity of the migration-enhanced epitaxy method.------------------------- 158

List of Symbols

Symbol	Description	Unit
a_{GaAs}	Lattice constant of GaAs	Å
a_{InAs}	Lattice constant of InAs	Å
a_{InGaAs}	Lattice constant of InGaAs	Å
A	Capacitor area	cm^2
A_G	Area of the transistor gate	cm^2
b	Strain-shift coefficient of Si-Si mode phonons	cm^{-1}
C	Capacitance	F
C_{ox}	Oxide capacitance	F
C_{GB}	Gate-to-body capacitance	F
C_{GC}	Gate-to-channel capacitance	F
d	Thickness	m
D	Diffusion coefficient	cm^2/s
D_{it}	Interface state density	$cm^{-2}\ eV^{-1}$
DIBL	Drain-induced barrier lowering	V/V
θ	Bragg angle	°
σ	Poisson coefficient	none
σ_n	Capture cross sections of electrons	cm^2
σ_p	Capture cross sections of holes	cm^2
ε_x	Strain component in x-direction	none
ε_y	Strain component in y-direction	none
E_{eff}	Effective vertical field	V/cm
EOT	Equivalent oxide thickness	nm
FGA	Forming gas anneal	

f	Frequency	Hz
G	Conductance	S
G_D	Drain conductance	S
G_{max}	Maximum conductance	S
$G_{m,ext}$	Extrinsic transconductance	S
$G_{m,int}$	Intrinsic transconductance	S
H_{Fin}	Fin height	m
I	Current	A
I_{CP}	Charge pumping current	A
I_{DS} or I_D	Drain current (per unit width)	A/μm
I_{Dlin}	Linear drain current (per unit width)	A/μm
I_{Dsat}	Saturation drain current (per unit width)	A/μm
I_{on}	On state current (per unit width)	A/μm
I_{off}	Off state current (per unit width)	A/μm
J_G	Gate leakage current density	A/cm^2
k	Boltzmann constant	$m^2\ kg\ s^{-2}\ K^{-1}$
L_G	Gate length	m
L_{CH}	Channel length	m
l_{Ge}	Thermal Diffusion length of Ge	m
N_A	P-type doping concentration	cm^{-3}
N_{inv}	Inversion charge density	cm^{-2}
n_s	Surface concentration of minority carriers	cm^{-3}
PDA	Post-gate dielectric deposition anneal	
q	Electronic charge	C
λ	Wavelength	m

R_{Ch}	Channel Resistance	Ω-µm
R_D	Drain resistance	Ω-µm
R_S	Source resistance	Ω-µm
R_{SD}	Source/drain series resistance	Ω-µm
R_{Total}	Total Resistance	Ω-µm
ρ_C	Specific contact resistivity	Ω-cm^2
SS	Subthreshold swing	V/decade
t	Time	s
T	Temperature	K
t_r	Rise time of trapezoidal pulse	s
t_f	Fall time of trapezoidal pulse	s
μ_{eff}	Effective mobility	cm^2/V s
V	Voltage	V
V_{base}	Base voltage of trapezoidal pulse	V
V_{DS} or V_D	Drain voltage	V
V_{FB}	Flatband voltage	V
V_{GS} or V_G	Gate voltage	V
V_T	Threshold voltage	V
v_{th}	Thermal velocity of the carrier	m/s
W_{Fin}	Fin Width	m
ω	Angular frequency	s^{-1}
$\Delta\omega_{Si\text{-}Si}$	Shift in the Raman frequency of the Si-Si phonons	cm^{-1}

Chapter 1

Introduction

1.1 Background

The number of transistors on integrated circuit (IC) chips has increased exponentially for more than four decades [1.1]. Through the years, sustaining the Moore's law requires the continued downscaling of the transistor dimensions. Enabled by tremendous advancement in lithography, the minimum feature size of transistors has been reduced by a factor of ~0.7 times in successive complementary metal-oxide-semiconductor (CMOS) technology nodes. Continuous device scaling has enabled higher packing density per unit chip area and improvement in circuit speed performance, leading to improved performance-to-cost ratio for IC products. However, aggressive geometrical scaling of silicon (Si)-based transistors would eventually reach the fundamental limits imposed by the properties of Si. High leakage currents from aggressively-scaled transistors can reduce or offset the performance gains due to excessive power consumption. Hence, the advancement of future CMOS technology will rely increasingly on the innovative deployment of materials, processes, and device architectures. It is therefore important to devote research efforts to address problems relating to the physical scaling limits of conventional Si-based CMOS.

1.2 Emerging Channel Materials for Extending CMOS

The International Technology Roadmap for Semiconductors (ITRS) identifies critical technology requirements and imminent challenges encountered by the semiconductor industry [1.2]. In addition to III-V compound semiconductors, several other emerging channel materials, such as carbon nanotubes, graphene, semiconductor nanowires, and germanium (Ge), have also been identified as promising candidates to replace the conventional Si or strained-Si channels [1.2]. New materials, such as Ge and III-V, offer the possibility of reduced power consumption and enhanced speed performance to meet the key logic technology requirements in the future. These benefits come from the superior field effect mobility of these semiconductors. With enhanced carrier-transport in these new channel materials, higher on-current, I_{on}, and therefore lower gate capacitance at constant I_{on} are expected. This combination can result in higher performance MOSFET with reduced power consumption. In the following sections, the opportunities and challenges of these emerging channel materials are introduced and discussed in detail.

1.2.1 Carbon Nanotube

Carbon nanotubes are allotropes of carbon with a cylindrical nanostructure. The primary advantages of carbon nanotubes are the high carrier mobility [1.3] and the potential to minimize short channel effects by surround gate geometry. However, many difficult challenges must be solved for this material to be viable for high performance FET applications, including: 1) the ability to control bandgap, 2) control of charge carrier type

and concentration, 3) growth of the nanotubes in required locations and directions, 4) deposition of a gate dielectric, and 5) formation of a low resistance electrical contact.

Remarkable progress has been demonstrated recently. For instance, carbon nanotube FET with a measured cut-off frequency of 4 GHz was reported [1.4]. However, little progress has been made in controlling the carrier type and concentration as it is still achieved by attaching molecules to the surface of the carbon nanotube [1.5]. More research efforts are needed to develop technologies that enable carbon nanotubes as a viable alternate channel material for use in beyond CMOS applications.

1.2.2 Graphene

Graphene is another potential candidate of new channel materials [1.6]-[1.7] that offers extremely high carrier mobilities and without the need to control chirality as in carbon nanotubes. For instance, mobilities of 10,000–15,000 $cm^2\ V^{-1}s^{-1}$ are routinely reported for exfoliated graphene on SiO_2-covered Si wafers at room temperature [1.8]. Since the breakthrough results of graphene MOS device reported by K. S. Novoselov *et. al.* [1.6], significant progress was made in the development of graphene transistors, including the demonstrations of a graphene MOSFET with a high cut-off frequency of 100 GHz [1.9], and the superior switching behavior of nanoribbon MOSFETs [1.10]. However, this progress has been accompanied by the appearance of several issues, such as processes capable of growing graphene on CMOS-compatible substrate, graphene film deposition with excellent uniformity, pattern and etch with low edge defect, development of fabrication techniques

such as doping, contact formation, and integration with CMOS-compatible processes. In addition, for device applications, non-zero bandgap of graphene must be realized and controlled independently through either shape modification or applied electric fields.

1.2.3 Nanowire

Nanowire field-effect transistors are based on novel FET architecture that replaces the channel region of a planar MOSFET with a semiconducting nanowire. The nanowires may be composed of a wide range of materials, including Si, Ge, III-V and II-VI compound semiconductors, and semiconducting oxides, such as In_2O_3, ZnO, and TiO_2. Nanowires with diameters as small as 0.5 nm were demonstrated [1.11]. With small diameters, these nanowires exhibit quantum confinement behavior due to one-dimensional transport of carriers, leading to modified charge carrier scattering and suppressed short channel effects.

There are two main approaches to form the nanowires, including: 1) top down lithography [1.12]; 2) bottom up catalyzed chemical vapor deposition [1.13]-[1.14]. Vertical nanowire FETs with good electrical characteristics based on Si [1.15], InAs [1.16], and ZnO [1.17] were demonstrated. Several major challenges must be surmounted for high density IC applications, including identification of CMOS-compatible catalyst materials, control of the placement, the direction, and the doping of nanowires. In addition, processing of dense arrays of laterally placed nanowires with surround gates and low resistance contacts may be challenging.

1.2.4 Germanium

With excellent electron and hole mobilities, Ge has received renewed interest as an alternative channel material candidate. In particular, the strained Ge P-MOSFETs show significant enhancement in hole mobility than Si P-FETs [1.18]-[1.19]. However, Ge has a small bandgap of 0.66 eV at 300 K [1.20]. This results in large band-to-band tunneling (BTBT) leakage or gate-induced drain leakage (GIDL). Ultrathin Ge film maybe necessary to control the leakage [1.21]. In addition, formation of high quality gate stack is another difficult challenge. Several interface passivation schemes were proposed and demonstrated, such as Si capping layer for improving the interfacial properties [1.22]. High quality GeO_2/Ge interfaces were also demonstrated by several research groups [1.22]-[1.24]. In addition, high-*k* gate dielectrics, such as HfO_2, $LaYO_3$ [1.24], and $SrGe_x$ [1.25], have also been investigated.

However, electron mobility in Ge N-MOSFETs is unable to out perform strained-Si N-MOSFETs despite the high electron mobility in bulk Ge. In addition, formation of low resistance S/D is also very challenging for Ge N-channel devices. The performance of the Ge N-MOSFET needs substantial improvement for it to be attractive.

1.3 Why III-V Compound Semiconductors?

Most emerging materials that are formed by “bottom-up” chemical synthesis, suffer from the fundamental placement problem as there is no practical and reliable way to precisely align and position them for high density IC applications. Conversely, III-V materials can be defined precisely into desirable device structures using conventional “top-down” lithographic and

etch approaches. In this regard, III-V compound semiconductors are considered far more practical.

III-V compound semiconductors are attractive for improving the mobility of N-MOSFETs, due to their high electron mobility. A higher electron mobility leads to improved speed performance for a given supply voltage as well as reduced dynamic power consumption for a fixed performance level. These advantages can bring tremendous benefits in terms of circuit and system performance due to the improved trade-off between power and performance. Fig. 1.1 shows the carrier mobility of various InGaAs compound semiconductors with different Indium composition, x [1.26]. In general, the carrier mobility increases with higher x due to reduction in effective mass m^* [1.27], as shown in Fig. 1.2. The occurrence of a mobility minimum in the region of x ~ 0.1 to 0.2 is due to alloy scattering [1.26].

In addition, III-V compound semiconductors also have the benefit of a lattice-matched heterostructure material system with a wide selection of band gaps and materials. Compared to Si-based heterostructures such as Si/SiGe, III-V heterostructures allow much greater flexibility in band structure engineering and thereby device design for both high performance and low power applications. For instance, InGaAs compound semiconductors offer wide range of bandgap from 0.36 eV (InAs with x = 1) to 1.42 eV (GaAs with x = 0) (Fig. 1.3) [1.28].

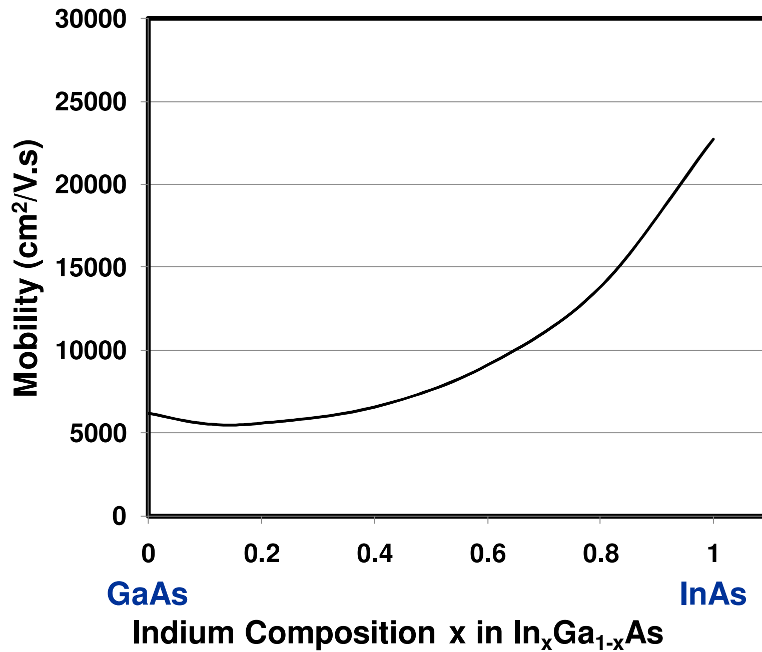


Fig. 1.1 Mobility versus composition x for $In_xGa_{1-x}As$ compound semiconductors. The mobility increases with higher Indium composition.

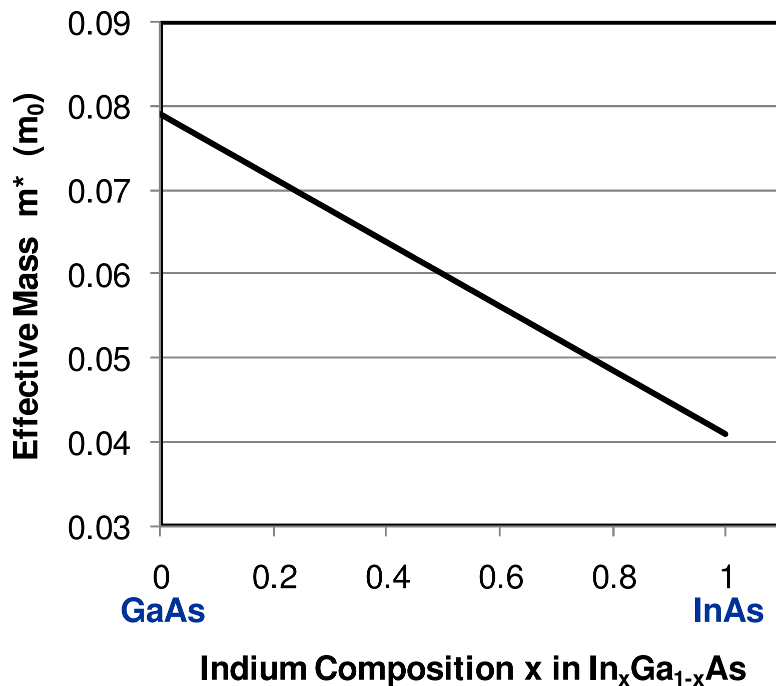


Fig. 1.2 Effective mass m^* versus composition x for $In_xGa_{1-x}As$ compound semiconductors. The effective mass decreases with higher Indium composition, leading to higher mobility in Fig. 1.1.

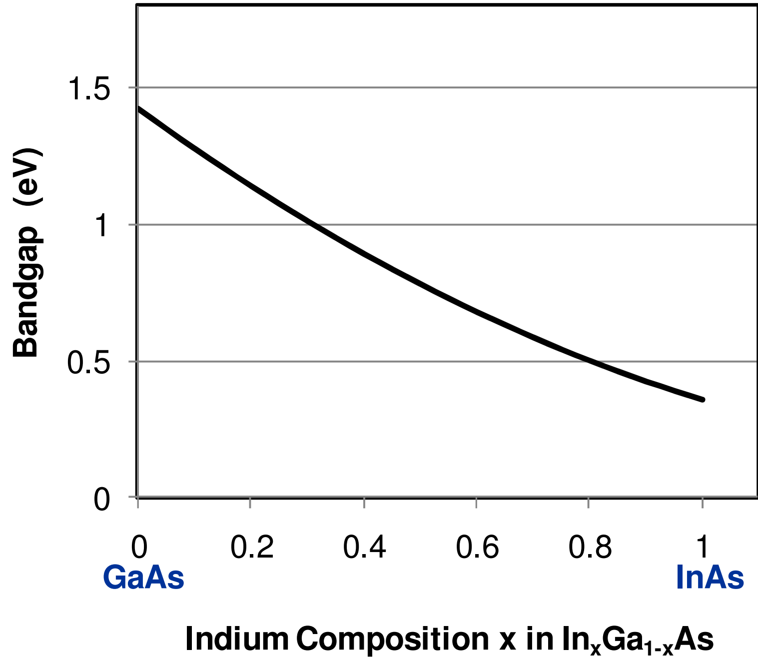


Fig. 1.3 Bandgap E_G versus composition x for $In_xGa_{1-x}As$ compound semiconductors. InGaAs offers wide range of bandgap from 0.36 eV to 1.42 eV.

1.4 Challenges of III-V MOSFET Technology

However, there are several key front-end issues that impede the progress of III-V MOSFET device technology, including high-quality gate stack formation, material integration on Si substrates, channel material and device structure selection, and low resistance S/D formation, as illustrated in Fig. 1.4. These technical challenges are discussed and summarized in the following sections.

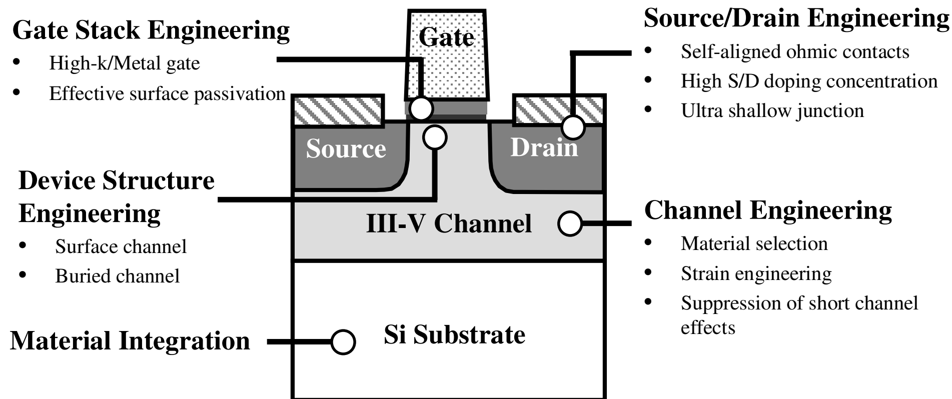


Fig. 1.4 Schematic illustration of the key technical challenges faced in the realization and integration of high mobility III-V channel MOSFET on Si substrates for future logic applications.

1.4.1 Formation of High-Quality Gate Stack

Unlike Si, native oxides of III-V have very poor electrical properties. The issues and challenges for dielectrics on III-V channels are due to the problem of chemical and electronic control of the interface between dielectric and III-V materials. Exposure of III-V to air or low vacuum results in the rapid formation of low quality native oxide on the surface, leading to Fermi level pinning and high interface state density [1.29]-[1.31]. Fermi level pinning on III-V compound semiconductors upon oxygen chemisorptions has been attributed to the formation of both donor and acceptor sites within the bandgap [1.32]. When two neighboring arsenic atoms from two different arsenic dimers are replaced by two oxygen atoms, the charge of atom of the central gallium atom deviates from its bulk value by about half an electron. Such a significant charge deviation gives rise to state formation. In addition, excess interfacial arsenic atoms occupying gallium sites create gap states as well [1.32]-[1.33].

III-V surface passivations and interface layers have been developed to manage the interface properties. Passivations such as *in-situ* molecular beam epitaxy (MBE) growth of Ga_2O_3, Gd_2O_3, and Ga_2O_3 (Gd_2O_3) [1.34]-[1.36], atomic layer deposition (ALD) of Al_2O_3 [1.37]-[1.39], HfO_2 [1.40], ZrO_2 [1.41], and $ZrO_2/LaAlO_x$ [1.42], jet vapor deposition of Si_3N_4 [1.43], wet thermal oxidation of InAlP [1.44], composite high-*k* gate stack of $TaSiO_x$/InP [1.45], as well as surface passivation technology employing Si [1.46], aluminum oxynitride (AlON) [1.47], phosphorus [1.48], phosphorus nitride P_xN_y [1.49] have been demonstrated in controlling surface oxidation effects on III-V to achieve lower interface state density D_{it} and unpinned interfaces. However, different high-*k* dielectrics may be needed for different semiconductor surfaces to prevent Fermi-level pinning in specific materials systems due to different surface reconstruction among the various III-V semiconductor surfaces [1.50]. Nevertheless, important factors such as manufacturability, performance advantages, and implementation cost should also be considered for the evaluation of the various surface passivation options. Schemes that provide simple and cost-effective integration with current manufacturing processes, and that give superior performance enhancement are highly desirable.

In the silicon CMOS industry, hafnium (Hf)-based high-*k* gate dielectric materials are deposited using techniques such as ALD and metal-organic chemical vapor deposition (MOCVD) in a manufacturable process. A missing link between the well-established gate dielectric process technology and III-V based device technology is a surface passivation technique for III-V compound semiconductors. Effective III-V surface passivation technologies

that can be easily integrated with these front-end processing tools will be preferred.

1.4.2 Material Integration on Si Substrate

III-V substrates are costly, brittle, and difficult to make in large sizes. In addition, from an economic point of view, the success of any future CMOS technology will depend on its compatibility with the existing Si manufacturing infrastructure. Therefore, methods need to be developed to integrate III-V materials on Si substrates. However, there are many issues and challenges to integrate III-V materials on Si-based substrates with controllable strain levels, acceptable defects and mobilities. Tremendous research effort has been made to overcome various technical challenges, including differences in lattice and thermal expansion parameters, and formation of antiphase domains (APDs), which typically appear during the growth of polar materials on non-polar materials.

D. Zubia *et. al.* reported direct nanoheteroepitaxial of GaAs on Si islands [1.51]. This approach relies on substrate compliance effect to accommodate the mismatch strain energy and to extend the critical thickness of the epilayer. However, the material integration is eventually limited by the large lattice mismatch of 4.1% between GaAs and Si. To reduce the lattice mismatch, SiGe graded buffer layer can be introduced between GaAs and Si [1.52]-[1.53]. However, surface dislocation density [1.54] and low throughput or high cost associated with a thick graded buffer layer remains as issues. Aspect ratio trapping (ART) method is another approach to significantly reduce the defect density by selective growth in high aspect ratio trenches and

subsequent lateral overgrowth [1.55]. Direct bonding of III-V crystalline layers through layer transfer is an alternative approach to epitaxial growth [1.56]-[1.58]. Using this approach, materials with huge lattice mismatch and desirable crystalline orientations can be integrated. However, large and expensive III-V wafers for layer transfer are needed for this technique.

Although progress has been made in integrating III-V on Si, further reduction in defect density and improvement in crystal quality is needed. Simple fabrication processes are highly desirable to reduce the process complexity and production cost. In addition, heterogeneous integration of III-V compound semiconductors on Si substrates would enable the fabrication of high-speed transistors and optoelectronic devices on a single Si-based platform and the realization of enhanced functionalities in integrated electronics.

1.4.3 Channel Material and Engineering

There is a trade-off between mobility and bandgap in general. For instance, InAs has a higher mobility but a narrower bandgap, as compared to GaAs. A lower bandgap leads to higher junction leakage current. In addition to the narrow bandgap, the energy difference between the lowest and the second lowest conduction bands tends to be small. The population of electrons in the second lowest conduction band is increased and the overall carrier mobility is degraded [1.59]. Therefore, ternary compound semiconductors, such as InGaAs, have received much attention due to their moderate bandgap and the acceptable energy difference between the lowest and the second lowest conduction band minima.

Although many III-V compound semiconductors offer very attractive electron mobility, some III-V materials, such as GaSb and InGaSb, offer high hole mobility for P-FET applications. On the other hand, channel strain engineering is another promising approach to further enhance the carrier transport of III-V semiconductors, such as GaAs and InGaAs [1.60]-[1.62].

1.4.4 Device Structure

There are primarily two III-V MOSFET architectures being investigated for logic applications: surface-channel and buried-channel MOSFETs. Buried-channel MOSFET typically has a quantum well structure to separate the gate and channel by a wide band-gap material. The buried-channel III-V high electron mobility transistors (HEMTs) demonstrates promising device performance [1.63]-[1.64]. However, the Schottky metal gate of these devices results in a large vertical Schottky gate leakage, which in turn causes high transistor off-state leakage. A gate dielectric stack which is compatible with III-V materials will need to be incorporated in the III-V buried-channel device to reduce off-state leakage, improve gate control and subthreshold slope, and therefore, enhance device scalability. While surface-channel devices are more desirable to achieve better capacitive coupling effects, they require the formation of a high-quality MOS stack with low D_{it}. For this reason, a buried-channel MOSFET design may be preferable to relax the requirements for low D_{it} and improve the carrier mobility. However, the capacitance penalty due to buried channel design will offset some of the advantages provided by the high mobility, and it is important to investigate the performance trade-off between these two device designs.

In addition, device architectures, such as FinFETs or multiple-gate FETs (MuGFETs), are attractive device architectures for III-V MOSFETs. With a better electrostatic control over the channel, several benefits can be derived from such a shift in architecture, such as improved control of short channel effects, enhanced volume inversion in the channel region, lower leakage currents, and reduced device variability arising from random dopant fluctuations.

1.4.5 Formation of Low Resistance Source/Drain Regions

S/D regions of conventional Si MOSFETs were formed by ion implantation, followed by dopant activation anneal. High doping concentration in the S/D reduces series resistance for achieving high drain current. In III-V materials, such as GaAs and InGaAs, Si is the preferred impurity to obtain N-type doping due to moderately low dopant activation temperature and thermally stable with low diffusivity. For instance, diffusivity of Si in GaAs is ~10^{-14} cm^2/s at 900 °C [1.65]. However, the maximum N-type carrier concentration in GaAs with Si as dopants is limited to ~1×10^{19} cm^{-3}, irrespective of the dose [1.66]. High fluence implant amorphizes the III-V compound material, results in the formation of high density of dislocation loops which cannot be eliminated even after high temperature annealing [1.67]. Such a low doping level leads to high S/D series resistance and further limits the S/D junction scaling for better control of short channel effects. Co-implantation of elements from Group V, such as phosphorus (P) or arsenic (As), was reported to further increase the Si activation in GaAs through the suppression of gallium on arsenic site (Ga_{As}) acceptors as well as silicon on

arsenic site (Si_{As}) acceptors [1.68]. Other innovative solutions are necessary to boost the S/D doping level to address the S/D series resistance issues.

In Si CMOS technology, S/D ohmic contacts, such as nickel silicide, are integrated based on self-aligned technology. These self-aligned S/D ohmic contacts, which are adjacent to the MOSFET's spacer, generate high conductivity paths for local wiring and therefore drastically reduce the S/D series resistance. Therefore, it is vital to develop a self-aligned S/D ohmic contact technology for III-V channel devices. In addition, gold-based contact technologies that are commonly integrated in III-V devices should be avoided as gold is a contaminant in CMOS technology.

1.5 Objective of Research

When advancing into the 22 nm technology generations and beyond, key changes to the fundamental material, process, and device structure are mandatory to sustain the need for ever increasing speed improvement. The objective of this thesis work is to address some of the most challenging front-end issues that impede the progress of current III-V device technology. Areas specific to novel interface passivation techniques for high quality MOS stack formation on III-V materials will be investigated. A comprehensive evaluation of various advanced device architectures, such as *in-situ* S/D doping, channel strain engineering and multiple-gate transistor structure, based on experimental results is furnished in this work. Another aspect of this project is on developing effective and potentially viable III-V material integration solution on Si substrate for future high volume semiconductor manufacturing.

The results of this research will help in the assessment of III-V channel MOSFET for applications in future technology generations.

1.6 Thesis Organization

The main issues discussed in this thesis are documented in 4 chapters.

Chapter 2 reports the concept and demonstration of novel surface passivation techniques to realize high quality metal gate/high-*k* dielectric stacks on a range of III-V compound semiconductors. This novel *in-situ* surface passivation technique that comprises vacuum anneal for native oxide desorption, followed by surface treatment, is compatible and can be easily integrated with a matured MOCVD gate cluster tool. A successful integration of these technologies in various III-V channel MOSFETs is demonstrated. Extensive electrical and material analysis was conducted to ascertain the attractiveness of this passivation technique.

Chapter 3 explores the integration of *in-situ* doped lattice-mismatched S/D stressors with InGaAs N-channel MOSFETs for S/D junction and channel strain engineering. Device design and concepts are explained with numerical simulations using the finite element method. Process integration and device fabrication of InGaAs channel transistors with *in-situ* doped lattice-mismatched S/D stressors are described. Material and electrical characterization results are discussed in detail to affirm the effectiveness of these advanced technologies.

Chapter 4 investigates advanced multiple-gate structure with epi-controlled retrograde channel doping to suppress short channel effects. Three-dimensional device simulations are performed to evaluate the device design

and concepts. Impact of this new device architecture on device characteristics is also presented.

Chapter 5 describes a new method of integrating GaAs on a Si-based substrate through selective migration-enhanced epitaxy (MEE) of GaAs on strain-compliant SiGe nanowire structures. The compliance effect for strain relaxation in such nanowire structures is shown. In addition, the quality of the GaAs epilayer is verified by extensive material characterization.

An overall conclusion and possibilities for future work are furnished in Chapter 6.

1.7 References

[1.1] G. E. Moore, “Progress in digital integrated electronics,” in *IEDM Tech. Dig.*, 1975, pp. 11–13.

[1.2] *International Technology Roadmap for Semiconductor*, Semiconductor Industry Association, 2009.

[1.3] T. Dürkop, S.A. Getty, E. Cobas, and M.S. Fuhrer. “Extraordinary mobility in semiconducting carbon nanotubes,” *Nano Lett.*, vol. 4, pp. 35–39, 2004.

[1.4] A. L. Louarn, F. Kapche, J.-M. Bethoux, H. Happy, G. Dambrine V. Derycke, P. Chenevier, N. Izard, M. F. Goffman, and J.-P. Bourgoin, “Intrinsic current gain cutoff frequency of 30 GHz with carbon nanotube transistors,” *Appl. Phys. Lett.*, vol. 90, no. 23, p. 233108, 2007.

[1.5] W. J. Yu, S. Y. Jeong, K. K. Kim, B. R. Kang, D. J. Bae, M. Lee, S. Hong, S. P. Gaunkar, D. Pribat, D. Perello, M. Yun, J.-Y. Choi, and Y. H. Lee, “Bias-induced doping engineering with ionic adsorbates on single-walled carbon nanotube thin film transistors,” *New J. Phys.*, vol. 10, no. 11, p. 113013, 2008.

[1.6] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, “Electric field effect in atomically thin carbon films,” *Science*, vol. 306, no. 5696, pp. 666–669, 2004.

[1.7] F. Schwierz, “Graphene transistors,” *Nat. Nanotech.*, vol. 5, no. 7, pp. 487–496, 2010.

[1.8] J.-H. Chen, C. Jang, S. Xiao, M. Ishigami, and M. S. Fuhrer., "Intrinsic and extrinsic performance limits of graphene devices on SiO_2," *Nat. Nanotech.*, vol. 3, no. 4, pp. 206–209, 2008.

[1.9] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and P. Avouris, "100-GHz transistors from wafer-scale epitaxial graphene," *Science*, vol. 327, no. 5966, p. 662, 2010.

[1.10] X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, "Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors," *Phys. Rev. Lett.*, vol. 100, no. 20, p. 206803, 2008.

[1.11] D. D. D. Ma, C. S. Lee, F. C. K. Au, S. Y. Tong, and S. T. Lee, "Small-diameter silicon nanowire surfaces," *Science*, vol. 299, no. 5614, pp. 1874–1877, 2003.

[1.12] N. Singh, F. Y. Lim, W. W. Fang, S. C. Rustagi, L. K. Bera, A. Agarwal, C. H. Tung, K. M. Hoe, S. R. Omampuliyur, D. Tripathi, A. O. Adeyeye, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "Ultra-narrow silicon nanowire gate-all-around CMOS devices: Impact of diameter, channel-orientation and low temperature on device performance", in *IEDM Tech. Dig.*, 2006, pp. 548–551.

[1.13] Cui, L. J. Lauhon, M. S. Gudiksen, J. Wang, and C. M. Lieber, "Diameter-controlled synthesis of single-crystal silicon nanowires," *Appl. Phys. Lett.*, vol. 78, no. 15, pp. 2214–2216, 2001.

[1.14] Y. Wu, and P. Yang, "Germanium nanowire growth via simple vapor transport," *Chem. Mater.*, vol. 12, no. 3, pp. 605–607, 2000.

[1.15] B. Yang, K. D. Buddharaju, S. H. G. Teo, N. Singh, G. Q. Lo, and D. L. Kwong, "Vertical silicon-nanowire formation and gate-all-around MOSFET," *IEEE Elect. Dev. Lett.*, vol. 29, no. 7, pp. 791–794, 2008.

[1.16] C. Thelander, L. E. Froberg, C. Rehstedt, L. Samuelson, and L.-E. Wenersson, "Vertical enhancement-mode InAs nanowire field-effect transistor with 50-nm wrap gate," *IEEE Elect. Dev. Lett.*, vol. 29, no. 3, pp. 206–208, 2008.

[1.17] H. T. Ng, J. Han, T. Yamada, P. Nguyen, Y. P. Chen, and M. Meyyappan, "Single crystal nanowire vertical surround-gate field-effect transistor," *Nano Letters*, vol. 4, no. 7, pp. 1247–1252, 2004.

[1.18] T. Irisawa, S. Tokumitsu, T. Hattori, K. Nakagawa, S. Koh, and Y. Shiraki, "Ultrahigh room-temperature hole Hall and effective mobility in $Si_{0.3}Ge_{0.7}/Ge/Si_{0.3}Ge_{0.7}$ heterostructure," *Appl. Phys. Lett.*, vol. 81, no. 5, pp. 847–849, 2002.

[1.19] T. Krishnamohan, Z. Krivokapic, K. Uchida, and Y. Nishi, "High-mobility ultrathin strained Ge MOSFETs on bulk and SOI with low band-to-band tunneling leakage: experiments," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 990–999, 2006.

[1.20] C. Kittel, *Introduction to Solid State Physics*, 6th Ed., New York:John Wiley, 1986, p. 185.

[1.21] J. Mitard, C. Shea, B. DeJaeger, A. Pristera, G. Wang, M. Houssa, G. Eneman, G. Hellings, W-E. Wang, J. C. Lin, F. E. Leys, R. Loo, G. Winderickx, E. Vrancken, A. Stesmans, K. DeMeyer, M. Caymax, L. Pantisano, M. Meuris, and M. Heyns, "Impact of EOT scaling down to

0.85nm on 70nm Ge-pFETs technology with STI," in *VLSI Symp. Tech. Dig.*, 2009, pp. 82–83.

[1.22] T. Takahashi, T. Nishimura, L. Chen, S. Sakata, K. Kita, and A. Toriumi, "Proof of Ge-interfacing concepts for metal/high-*k*/Ge CMOS - Ge-intimate material selection and interface conscious process flow," in *IEDM Tech. Dig.*, 2007, pp. 697–700.

[1.23] Y. Nakakita, R. Nakane, T. Sasada, H. Matsubara, M. Takenaka, and S. Takagi, "Interface-controlled self-align source/drain Ge P-MOSFETs using thermally-oxidized GeO_2 interfacial layers," in *IEDM Tech. Dig.*, 2008, pp. 877–879.

[1.24] M. Kobayashi, T. Irisawa, B. M. Kope, Y. Sun, K. Saraswat, H.-S. P. Wong, P. Panetta, and Y. Nishi, "High quality GeO_2/Ge interface formed by SPA radical oxidation and uniaxial stress engineering for high performance Ge NMOSFETs," in *VLSI Symp. Tech. Dig.*, 2009, pp. 76–77.

[1.25] Y. Kamata, A. Takashima, Y. Kamimuta, and T. Tezuka, "New approach to form EOT-scalable gate stack with Strontium Germanide interlayer for high-*k*/Ge MISFETs," in *VLSI Symp. Tech. Dig.*, 2009, pp. 78–79.

[1.26] D. Chattopadhyay, S. K. Sutradhar, and B. R. Nag, "Electron transport in direct-gap III-V ternary alloys," *J. Phys. C: Solid State Phys.*, vol. 14, pp. 891–908, 1981.

[1.27] P. Bhattachary, Ed., "Properties of Lattice-Matched and Strained Indium Gallium Arsenide," No. 8 in *EMIS Datareviews Series*, IEE INSPEC, 1993.

[1.28] R. E. Nahory, M. A. Pollack, W. D. Johnston, and R. L. Barns, “Band gap versus composition and demonstration of Vegard’s law for $In_{1-x}Ga_xAs_yP_{1-y}$ lattice matched to InP,” *Appl. Phys. Lett.*, vol. 33, no. 7, pp. 659–661, 1978.

[1.29] G. G. Fountain, R. A. Rudder, S. V. Hattangady, R. J. Markunas, and J. A. Hutchby, “Demonstration of an n-channel inversion mode GaAs MISFET,” in *IEDM Tech. Dig.*, 1989, pp. 887–889.

[1.30] C. C. Surdu-Bob, S. O. Saied, and J. L. Sullivan, “An X-ray photoelectron spectroscopy study of the oxides of GaAs,” *Appl. Surf. Sci.*, vol. 183, no. 1–2, pp. 126–136, 2001.

[1.31] M. Passlack, M. Hong, J. P. Mannaerts, S. N. G. Chu, R. L. Opila, and N. Moriya, “*In-situ* Ga_2O_3 process for GaAs inversion/accumulation device and surface passivation applications,” in *IEDM Tech. Dig.*, 1995, pp. 383–386.

[1.32] M. J. Hale, S. I. Yi, J. Z. Sexton, A. C. Kummel, and M. Passlack, “Scanning tunneling microscopy and spectroscopy of gallium oxide deposition and oxidation on GaAs(001)-c(2x8)/(2x4),” *J. Chem. Phys.*, vol. 119, no. 13, pp. 6719–6728, 2003.

[1.33] W. E. Spicer, Z. Liliental-Weber, E. Weber, N. Newman, T. Kendelewicz, R. Cao, C. McCants, P. Mahowald, K. Miyano, and I. Lindau, “The advanced unified defect model for Schottky barrier formation,” *J. Vac. Sci. Technol. B*, vol. 6, no. 4, pp. 1245–1251, 1988.

[1.34] M. Hong, J. Kwo, A. R. Mannaerts, and A. M. Sergent, “Epitaxial cubic gadolinium oxide as a dielectric for gallium arsenide passivation,” *Science*, vol. 283, no. 5409, pp. 1897–1900, 1999.

[1.35] J. Kwo, D. W. Murphy, M. Hong, R. L. Opila, J. P. Mannaerts, A. M. Sergent, and R. L. Masaitis, "Passivation of GaAs using $(Ga_2O_3)_{1-x}(Gd_2O_3)_x$, $0 \leq x \leq 1.0$ films," *Appl. Phys. Lett.*, vol. 75, no. 8, pp. 1116–1118, 1999.

[1.36] K. Rajagopalan, R. Droopad, J. Abrokwah, P. Zurcher, P. Fejes, and M. Passlack, "1-μm enhancement mode GaAs n-channel MOSFETs with transconductance exceeding 250 mS/mm," *IEEE Electron Device Lett.*, vol. 28, no. 2, pp. 100–102, 2007.

[1.37] Y. Xuan, T. Shen, M. Xu, Y.Q. Wu, and P. D. Ye, "High-performance surface channel In-rich $In_{0.75}Ga_{0.25}As$ MOSFETs with ALD high-*k* as gate dielectric," in *IEDM Tech. Dig.*, 2008, pp. 371–374.

[1.38] D. Lin, G. Brammertz, S. Sioncke, C. Fleischmann, A. Delabie, K. Martens, H. Bender, T. Conard, W. H. Tseng, J. C. Lin, W. E. Wang, K. Temst, A, Vatomme, J. Mitard, M. Caymax, M. Meuris, M. Heyns, and T. Hoffmann, "Enabling the high-performance InGaAs/Ge CMOS: a common gate stack solution," in *IEDM Tech. Dig.*, 2009, pp. 327–330.

[1.39] Y. Q. Wu, M. Xu, R.S. Wang, O. Koybasi, and P. D. Ye, "High performance deep-submicron inversion-mode InGaAs MOSFETs with maximum G_m exceeding 1.1 mS/μm: New HBr pretreatment and channel engineering," in *IEDM Tech. Dig.*, 2009, pp. 323–326.

[1.40] M. M. Frank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Muller, "HfO_2 and Al_2O_3 gate dielectrics on GaAs grown by atomic layer deposition," *Appl. Phys. Lett.*, vol. 86, no. 15, pp. 152904–152906, 2005.

[1.41] N. Goel, D. Heh, S. Koveshnikov, I. Ok, S. Oktyabrsky, V. Tokranov, R. Kambhampatic, M. Yakimov, Y. Sun, P. Pianetta, C.K. Gaspe, M.B. Santos, J. Lee, S. Datta, P. Majhi, and W. Tsai, “Addressing the gate stack challenge for high mobility $In_xGa_{1-x}As$ channels for NFETs,” in *IEDM Tech. Dig.*, 2008, pp. 363–366.

[1.42] J. Huang, N. Goel, H. Zhao, C. Y. Kang, K.S. Min, G. Bersuker, S. Oktyabrsky, C.K. Gaspe, M.B. Santos, P. Majhi, P. D. Kirsch, H.-H. Tseng, J.C. Lee, and R. Jammy, “InGaAs MOSFET performance and reliability improvement by simultaneous reduction of oxide and interface charge in ALD (La)AlO_x/ZrO_2 gate stack,” in *IEDM Tech. Dig.*, 2009, pp. 335–338.

[1.43] W. P. Li, X. W. Wang, Y. X. Liu, S. I. Shim, and T. P. Ma, “Demonstration of unpinned GaAs surface and surface inversion with gate dielectric made of Si_3N_4,” *Appl. Phys. Lett.*, vol. 90, no. 19, p. 193503, 2007.

[1.44] Y. Cao, X. Li, J. Zhang, P. Fay, T. H. Kosel, and D. C. Hall, “Microwave performance of GaAs MOSFET with wet thermally oxidized InAlP Gate Dielectric,” *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 317–319, 2006.

[1.45] M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and R. Chau, “Advanced high-*k* gate dielectric for high-performance short-channel $In_{0.7}Ga_{0.3}As$ quantum well field effect transistors on silicon substrate

for low power logic applications," in *IEDM Tech. Dig.*, 2009, pp. 319–322.

[1.46] I. Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, L. Yu, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and J. C. Lee, "Self-aligned n- and p-channel GaAs MOSFETs on undoped and p-type substrates using HfO_2 and silicon interface passivation layer," in *IEDM Tech. Dig.*, 2006, pp. 829–832.

[1.47] M. Zhu, C.-H. Tung, and Y.-C. Yeo, "Aluminum oxynitride interfacial passivation layer for high-permittivity gate dielectric stack on gallium arsenide," *Appl. Phys. Lett.*, vol. 89, no. 20, p. 202 903, 2006.

[1.48] J. Lin, S. Lee, H.-J. Oh, W. Yang, G. Q. Lo, D. L. Kwong, and D. Z. Chi, "Plasma PH_3-passivated high mobility inversion InGaAs MOSFET fabricated with self-aligned gate-first process and HfO_2/TaN gate stack," in *IEDM Tech. Dig.*, 2008, pp. 401–404.

[1.49] H. J. Oh, J. Q. Lin, S. A. B. Suleiman, G. Q. Lo, D. L. Kwong, D. Z. Chi, and S. J. Lee, "Thermally robust phosphorous nitride interface passivation for InGaAs self-aligned gate-first N-MOSFET integrated with high-*k* dielectric," in *IEDM Tech. Dig.*, 2009, pp. 339–342.

[1.50] D. L. Winn, M. J. Hale, T. J. Grassman, A. C. Kummel, R. Droopad, and M. Passlack, "Direct and indirect causes of Fermi level pinning at the SiO/GaAs interface," *J. Chem. Phys.*, vol. 126, no. 8, p. 084703, 2007.

[1.51] D. Zubia, S. Zhang, R. Bommena, X. Sun, S. R. J. Brueck, and S. D. Hersee, "Initial nanoheteroepitaxial growth of GaAs on Si(100) by OMVPE," *J. Electron. Mater.*, vol. 30, no. 7, pp. 812–816, 2001.

[1.52] R. M. Sieg, J. A. Carlin, J. J. Boeckl, S. A. Ringel, M. T. Currie, S. M. Ting, T. A. Langdo, G. Taraschi, E. A. Fitzgerald, and B. M. Keyes, "High minority-carrier lifetimes in GaAs grown on low-defect-density Ge/GeSi/Si substrates," *Appl. Phys. Lett.*, vol. 73, no. 21, pp. 3111–3113, 1998.

[1.53] E. A. Fitzgerald, Y.-H. Xie, M. L. Green, D. Brasen, A.R. Kortan, J. Michel, Y.-J. Mii, and B. E. Weir, "Totally relaxed Ge_xSi_{1-x} Layers with low threading dislocation densities grown on Si substrates," *Appl. Phys. Lett.*, vol. 59, no. 7, pp. 811–813, 1991.

[1.54] C. W. Leitz, M. T. Currie, A. Y. Kim, J. Lai, E. Robbins, E. A. Fitzgerald, and M. T. Bulsara, "Dislocation glide and blocking kinetics in compositionally graded SiGe/Si," *J. Appl. Phys.*, vol. 90, no. 6, pp. 2730–2736, 2001.

[1.55] J. Z. Li, J. Bai, J.-S. Park, B. Adekore, K. Fox, M. Carroll, A. Lochtefeld, and Z. Shellenbarger, "Defect reduction of GaAs epitaxy on Si (001) using selective aspect ratio trapping," *Appl. Phys. Lett.*, vol. 91, no. 2, p. 021114, 2007.

[1.56] K. Hjort, "Transfer of InP epilayers by wafer bonding," *J. Cryst. Growth*, vol. 268, no. 3–4, pp. 346–358, 2004.

[1.57] P. Chen, Y. Jing, S. S. Lau, D. Xu, L. Mawst, T. L. Alford, C. Paulson, and T. F. Kuech, "High crystalline-quality III-V layer transfer onto Si substrate," *Appl. Phys. Lett.*, vol. 92, no. 9, p. 092107, 2008.

[1.58] M. Yokohama, T. Yasuda, H. Takagi, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka, and S. Takagi, "High mobility metal S/D III-V-on-insulator MOSFETs on a Si substrate

using direct wafer bonding," in *VLSI Symp. Tech. Dig.*, 2009, pp. 242–243.

[1.59] K. C. Saraswat, C. O. Chui, D. Kim, T. Krishnamohan, and A. Pethe, "High mobility materials and novel device structures for high performance nanoscale MOSFETs," in *IEDM Tech. Dig.*, 2006, pp. 659–662.

[1.60] G. E. Pikus, and G. L. Bir, *Symmetry and Strained-Induced Effects in Semiconductors*, New York, J. Wiley, 1974.

[1.61] C. Kopf, H. Kosina, and S. Selberherr, "Physical models for strained and relaxed GaInAs alloys: Band structure and low-field transport," *Sol.-State Elec.*, vol. 41, no. 8, pp. 1139–1152, 1997.

[1.62] S. Suthram, Y. Sun, P. Majhi, I. Ok, H. Kim, H. R. Harris, N. Goel, S. Parthasarathy, A. Koehler, T. Acosta, T. Nishida, H.-H. Tseng, W. Tsai, J. Lee, R. Jammy, and S. E. Thompson, "Strain additivity in III-V channels for CMOSFETs beyond 22 nm technology node," in *VLSI Symp. Tech. Dig.*, 2008, pp. 182–183.

[1.63] D.-H. Kim and J. A. del Alamo, "Logic-performance of 40nm InAs HEMTs," in *IEDM Tech. Dig.*, 2007, pp. 629–631.

[1.64] N. Waldron, D.-H. Kim, and J. A. del Alamo, "90nm Self-aligned Enhancement-mode InGaAs HEMT for logic applications," in *IEDM Tech. Dig.*, 2007, pp. 633–635.

[1.65] M. V. Rao, "Ion implantation in III-V compound semiconductors," *Nucl. Inst. And Meth. In Phys. Res.*, vol. B79, no. 1-4, pp. 645–647, 1993.

[1.66] J. P. de Souza, and D. K. Sadana, "Ion implantation in gallium arsenide

MESFET technology," *IEEE Trans. Electron Devices*, vol. 39, no. 1, pp. 166–175, 1992.

[1.67] C. W. Farley, and B. G. Streetman, "The role of defects in the diffusion and activation of impurities in ion implanted semiconductors," *J. Electron. Mater.*, vol. 13, no. 2, pp. 401–436, 1984.

[1.68] F. Hyuga, H. Yamazaki, K. Watanabe, and J. Osaka, "Activation efficiency improvement in Si-implanted GaAs by P co-implantation," *Appl. Phys. Lett.*, vol. 50, no. 22, pp. 1592–1594, 1987.

Chapter 2

In-situ Surface Passivation and Metal-Gate/High-*k* Dielectric Stack Formation for III-V MOSFETs

2.1 Introduction

High mobility III-V compound semiconductors have received interest as potential channel materials to replace conventional Si or strained Si channels and to be heterogeneously integrated onto a silicon platform. High quality and thermodynamically stable metal-oxide-semiconductor (MOS) stack on III-V is vital for exploiting the full advantages of high mobility channel materials. However, exposure of III-V surface to air or low vacuum results in the rapid formation of a low quality native oxide on the surface, leading to Fermi level pinning and high interface state density D_{it} [2.1]-[2.5].

Recently, III-V MOSFET research has been directed at developing advanced gate dielectric technology, including *in-situ* molecular beam epitaxy (MBE) growth of Ga_2O_3, Gd_2O_3, and Ga_2O_3 (Gd_2O_3) [2.6]-[2.8], atomic layer deposition (ALD) of Al_2O_3 [2.9]-[2.11], HfO_2 [2.12], ZrO_2 [2.13], and ZrO_2/$LaAlO_x$ [2.14], jet vapor deposition of Si_3N_4 [2.15], wet thermal oxidation of InAlP [2.16], composite high-*k* gate stack of $TaSiO_x$/InP [2.17], as well as surface passivation technology employing Si [2.18]-[2.19], aluminum

oxynitride (AlON) [2.20], phosphorus [2.21], phosphorus nitride P_xN_y [2.22] for reduction of D_{it}. Nevertheless, important considerations such as manufacturability, implementation cost, and performance benefits are crucial factors in the assessment of the various surface passivation options. Schemes that allow simple and cost-effective integration with current manufacturing processes, and that give superior performance improvements are preferred.

In the Si CMOS industry, hafnium (Hf)-based high-*k* gate dielectric materials are commonly deposited using processes such as ALD and metal-organic chemical vapor deposition (MOCVD). A missing link between the well-established gate dielectric process technology and III-V based device technology is an effective surface passivation technique. Effective III-V surface passivation technologies that can be easily integrated with gate dielectric deposition tools would be desirable.

In this chapter, novel surface passivation schemes on various III-V compound semiconductors are explored to realize high quality metal gate/high-*k* dielectric stack. The *in-situ* surface technique comprises a vacuum anneal for native oxide desorption, followed by a surface treatment process that is compatible and that can be easily integrated with a matured MOCVD gate cluster tool as shown in Fig. 2.1. This MOCVD gate cluster system consists of three process chambers for native oxide desorption, surface passivation, and MOCVD high-*k* dielectric deposition. It is also equipped with a high vacuum transfer module with base pressure of 1×10^{-7} Torr to prevent native oxide formation during wafer transfer. The low vacuum level was achieved by the two-stage dry pumps and high speed turbo pump. The

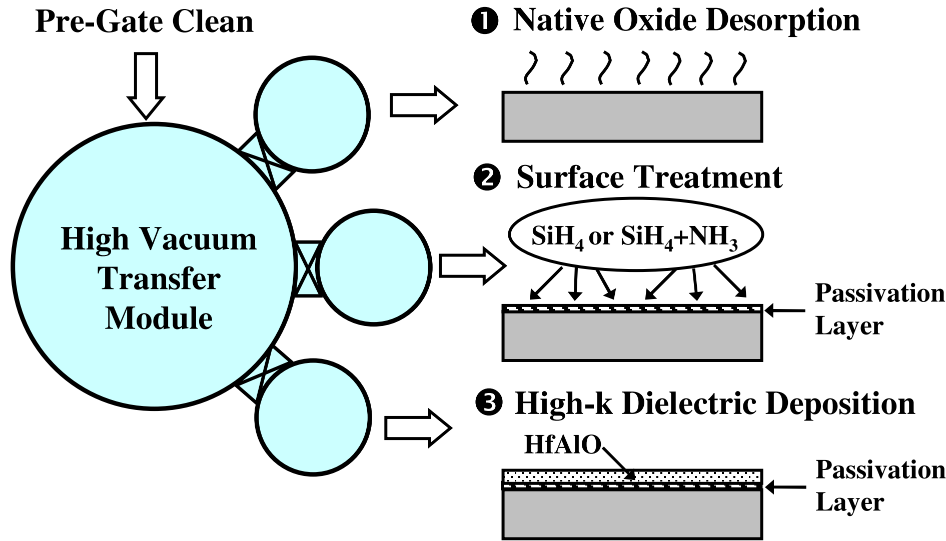


Fig. 2.1 Schematic illustration of the key process steps in the *in-situ* passivation technology based on a multiple chamber MOCVD gate cluster system. The high vacuum transfer module serves to minimize native oxide formation during wafer transfer. After pre-gate cleaning, the III-V wafers were quickly loaded into the gate cluster system for native oxide decomposition, surface treatment, and MOCVD high-*k* dielectric deposition at three different chambers.

system has a robot arm that can handle two 8 inch wafers. The small III-V wafers are placed on these 8 inch handling wafers for processing in the tool.

Various *in-situ* surface passivation schemes explored in this thesis are summarized in Fig. 2.2. In addition, Fig. 2.2 also shows the III-V compound semiconductors investigated in each scheme. In Section 2.2, GaAs, with high carrier mobility, was first used in *in-situ* surface passivation, featuring vacuum anneal and silane (SiH_4) treatment. After high-quality MOS stack formation on GaAs, SiH_4 passivation study was extended to $In_{0.18}Ga_{0.82}As$ to explore the impacts to gate stack with additional Indium. In Section 2.3, surface treatment using silane and ammonia (SiH_4 + NH_3) gas mixture is also employed on GaAs, and $In_{0.53}Ga_{0.47}As$. $In_{0.53}Ga_{0.47}As$ was investiged due to its high

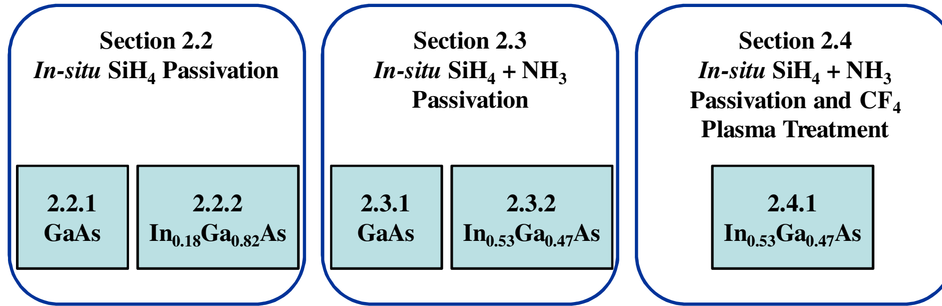


Fig. 2.2 Summary of various *in-situ* surface passivation schemes and the III-V compound semiconductors investigated in each scheme.

mobility [Fig. 1.1] and lattice constant that matches well with InP substrate. Section 2.4 explores the integration of multiple passivation methods with *in-situ* SiH_4 + NH_3 surface passivation and post-gate dielectric deposition treatment in tetrafluoromethane (CF_4) plasma for further performance enhancement. Section 2.5 summarizes the key achievements attained.

2.2 III-V Channel N-MOSFETs with *In-situ* SiH_4 Passivation

In this section, novel III-V channel N-MOSFETs with *in-situ* surface passivation, comprising vacuum anneal and SiH_4 treatment, are investigated for enhancing gate stack quality. Vacuum annealing eliminated poor quality native oxide on III-V surface, while a thin silicon interfacial layer was formed by SiH_4 treatment, therefore effectively preventing the III-V surface from exposure to an oxidizing ambient during MOCVD high-*k* dielectric deposition.

In this section, self-aligned surface channel III-V N-MOSFET with *in-situ* SiH_4 surface passivation was realized. Section 2.2.1 demonstrates high quality gate stack formation on GaAs using *in-situ* SiH_4 passivation technology. Section 2.2.2 explores the integration of *in-situ* SiH_4 passivation

on InGaAs with indium composition of 20 %, showing improved device performance.

2.2.1 GaAs N-MOSFET with *In-situ* SiH_4 Passivation

In this section, GaAs N-MOSFET with *in-situ* vacuum anneal and SiH_4 passivation is reported. The impact of post-gate-dielectric deposition anneal (PDA) and forming gas anneal (FGA) conditions on the electrical performance and integrity of GaAs N-MOSFETs is investigated. This self-aligned N-channel GaAs MOSFET is also incorporated with Si^+ + P^+ deep S/D regions [2.23]-[2.24] and gold-free low resistance PdGe ohmic contacts.

2.2.1.1 Experiment

P-type Zn-doped GaAs (100) substrates with a N_A of $1 - 5 \times 10^{16}$ cm^{-3} were used for device fabrication. The process flow is depicted in Fig. 2.3. The pre-gate cleaning process comprises degreasing using acetone and isopropanol, removal of native oxide and excess elemental As using hydrochloric acid (HCl) and ammonium hydroxide solution (NH_4OH), and *ex-situ* surface passivation using ammonium sulphide solution [$(NH_4)_2S$]. The native oxide on epi-ready GaAs surface is 2 to 3 nm [2.25]. With HCl cleaning, native oxide and elemental gallium were rapidly removed [2.26]. As elemental arsenic has low solubility in acid, the following NH_4OH treatment is useful for excess elemental arsenic removal [2.27]. A dip in $(NH_4)_2S$ solution was finally performed for *ex-situ* surface passivation [2.28].

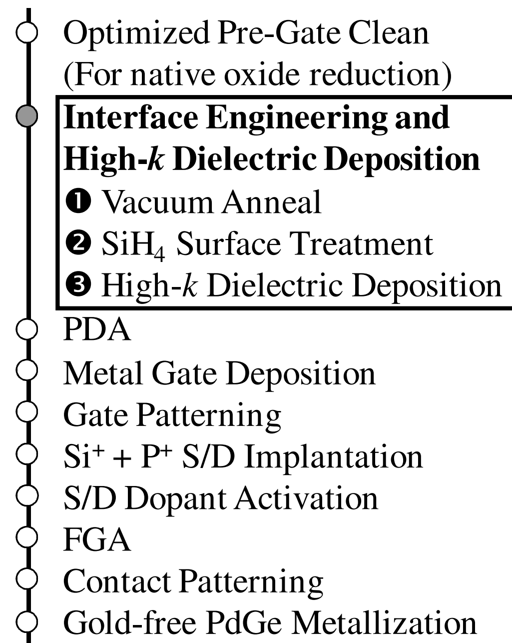


Fig. 2.3 Process sequence employed in transistor fabrication. The *in-situ* vacuum anneal and SiH_4 interface passivation steps are performed before MOCVD high-*k* dielectric deposition.

After the pre-gate clean, the wafers were quickly loaded into a multiple-chamber MOCVD gate cluster. In the first chamber of the gate cluster system, the wafers were annealed at 600 °C for 60 s at process pressure of ~ 1×10^{-6} Torr for native oxide decomposition. The RMS surface roughness of the GaAs before and after vacuum anneal is 1.2 Å and 1.3 Å, respectively. The wafers were then transferred to a second chamber through the transfer module for SiH_4 treatment at 400 °C for 60 s at pressure of 5 Torr (the flow rates of SiH_4 and N_2 are 60 and 250 sccm, respectively) [2.29]. Without breaking vacuum, the wafers were transferred to a third chamber for HfAlO high-*k* dielectric deposition. The MOCVD process employed a single cocktail source, $HfAl(MMP)_2(OiPr)_5$, as precursor and Ar as the carrier gas at temperature of 450 °C and pressure of 400 mTorr [2.30]. As the precursor is

in liquid state with low vapor pressure of ~ 6.4 × 10^{-5} Torr at room temperature, the precursor was first delivered to a vaporizer using liquid delivery system at a liquid flow rate of 40 mg/minute. The vaporized precursor was subsequently delivered to the process chamber using Ar as the carrier gas at flow rate of 170 sccm. On a control wafer, HfAlO was deposited directly on GaAs without *in-situ* vacuum anneal and SiH_4 passivation.

After high-*k* dielectric deposition, PDA at various temperatures ranging from 500 to 600 °C was performed in a rapid thermal process chamber for 60 s in N_2 ambient [2.29]-[2.30]. TaN metal gate was reactively sputtered. Fig. 2.4 shows the two-mask transistor structure. Gate patterning was then carried out using contact printing in a mask aligner. After spin-coating of photoresist, pre-bake at 95 °C was used to drive off excess solvent prior exposure in 365 nm ultraviolet light. Post-exposure bake at 115 °C for 60 s was then performed to improve adhesion and to improve side wall profile caused by standing wave phenomena. After development, hard bake at 115 °C for 60 s was used to solidify the remaining photoresist. Gate etching in Cl_2 based plasma was then performed. The Cl_2 dry etching was stopped at high-*k* dielectric to protect the S/D regions. The remaining high-k dielectric was

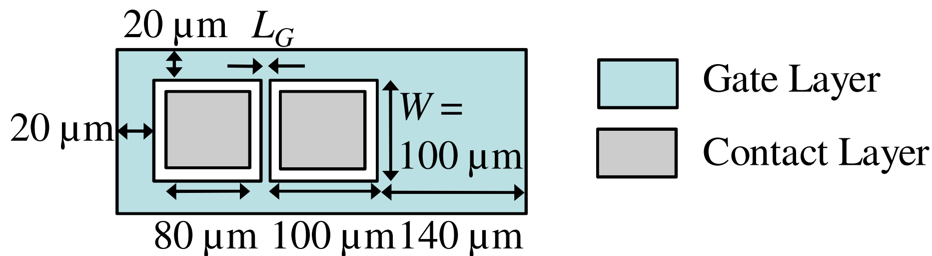


Fig. 2.4 Schematic illustration of the two-mask transistor structure with gate and contact layers. The transistor width *W* is 100 μm.

removed by another wet cleaning in dilute HF solution. Self-aligned deep S/D regions formation were formed by Si^+ and P^+ implantation at dose of 1×10^{14} cm^{-2} (25 keV and 80 keV) and 5×10^{13} cm^{-2} (25 keV and 80 keV), respectively, and dopant activation at 850 °C in N_2 ambient. Due to the lack of ion implanter in NUS, all the ion implantation processes in this thesis were not conducted by me. The shallow implant at 25 keV serves to increase the doping level near the surface for contact resistance reduction. The deep implant at 80 keV is used to increase the junction depth for source/drain series resistance reduction. Si^+ ions were introduced as n-type dopants whereas the P^+ ions serve to reduce the formation of Si on As site acceptors [2.23]-[2.24]. After that, some devices underwent FGA at various temperatures between 300 ^oC to 500 ^oC for 10 min. to 30 min. at process pressure of 400 Torr (the flow rates of H_2 and N_2 are 300 sccm and 2000 sccm, respectively). S/D ohmic contact regions were defined by a second optical lithography before the deposition of 40 nm of Pd, followed by 90 nm of Ge, using electron beam evaporation. Lift-off process and contact formation at various temperatures between 300 to 450 °C for 10 s were subsequently carried out to complete the device fabrication.

2.2.1.2 Results and Discussion

The effect of PDA temperature is first investigated. Fig. 2.5 depicts the *C-V* characteristics of GaAs capacitors formed with various process conditions: (i) without *in-situ* passivation, but PDA of 500 °C was performed; with *in-situ* surface passivation and PDA at temperatures of (ii) 500 °C, (iii) 550 °C, and (iv) 600 °C. In all cases, the duration of the PDA is 60 s. The

square shape GaAs capacitors are 100 μm by 100 μm in dimensions. Electrical measurement was performed by using the TaN gate as metal contact. FGA was included. As transistor can be fabricated by gate-last approach, implantation anneal was skipped here to evaluate the best achievable performance by this technique. A separate investigation on the impact of implant anneal can be found in Fig. 2.26. The control GaAs capacitors exhibit severe frequency dispersion due to the presence of a large number of interface traps (Fig. 2.6). The frequency dispersion is evaluated as the percentage difference in accumulation capacitance values measured at 10 kHz and 1 MHz without correction for series resistance. Frequency dispersion reveals difference time response of the interface states.

C-V characteristics in forward and reverse sweeps are plotted in Fig. 2.7. Substantial reduction in hysteresis was observed in GaAs capacitors with additional *in-situ* surface passivation (inset of Fig. 2.7). Hysteresis is defined as the difference in flatband voltage of *C-V* curves obtained from forward and reverse gate voltage V_G sweeps. Dalapati *et al.* reported significant degradation in electrical properties of gate dielectric at PDA temperatures above 500 °C, due to elemental Ga and As out-diffusion [2.31]. The weak PDA temperature dependence of frequency dispersion and hysteresis suggests that the *in-situ* surface passivation technique is quite effective. SiH_4 treatment allows the eventual formation of an interfacial layer comprising SiO_2 that improves the thermal stability of gate stack. The out-diffusion of Ga and As into the high-*k* dielectric during high temperature processing steps is also suppressed.

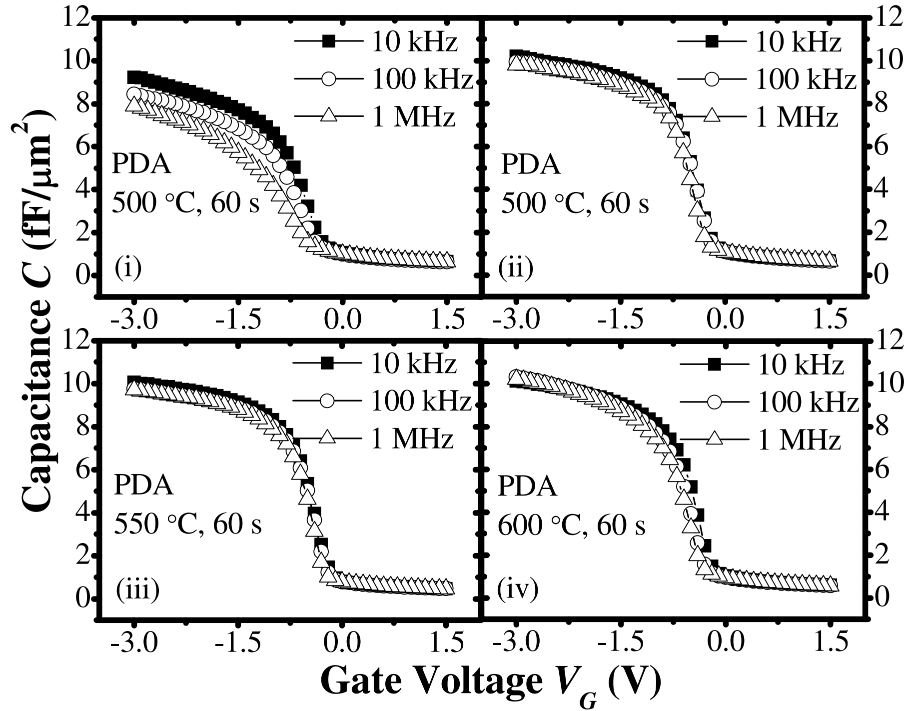


Fig. 2.5 *C-V* characteristics of GaAs MOS capacitors formed using various process conditions. In (i), PDA of 500 °C was used, but no *in-situ* passivation was performed. In other samples, PDA temperatures of (ii) 500 °C, (iii) 550 °C, and (iv) 600 °C, were used together with *in-situ* vacuum anneal and SiH_4 passivation.

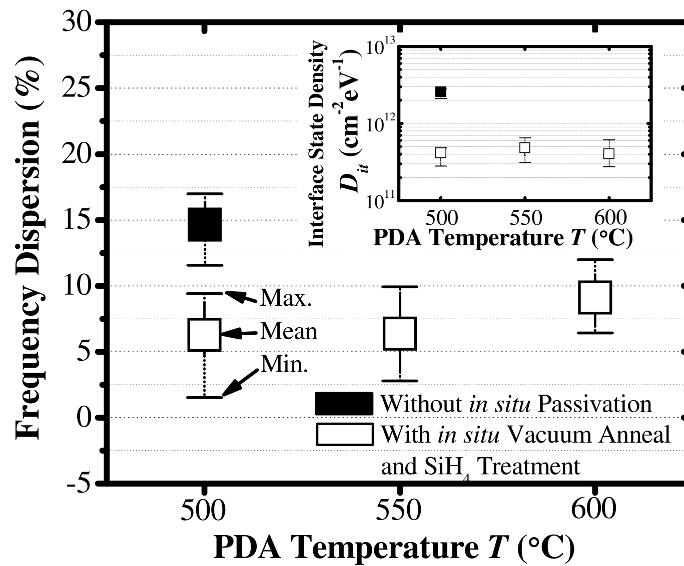


Fig. 2.6 Frequency dispersion of *C-V* characteristics as a function of PDA temperature for GaAs MOS capacitors. D_{it} attained at various PDA temperatures is depicted in the inset.

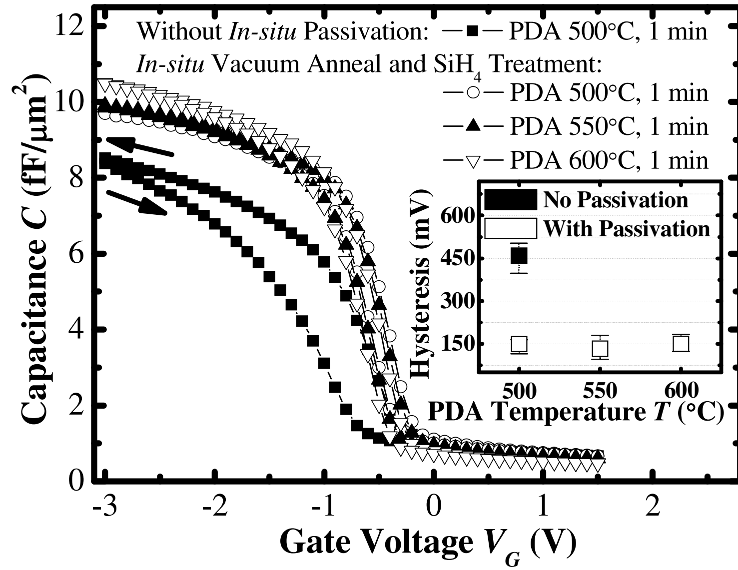


Fig. 2.7 *C-V* forward- and reverse sweeps for capacitors with and without *in-situ* surface passivation and at various PDA temperatures. *In-situ* surface passivation is important for minimizing hysteresis.

FGA in gas mixtures of hydrogen and nitrogen ($H_2 + N_2$) is effective in passivating dangling bonds and in reducing D_{it} at the SiO_2–Si interface [2.32]. Similar advantages were also found for GaAs capacitors. In general, hysteresis, frequency dispersion, and D_{it} were improved after FGA (Fig. 2.8 and Fig. 2.9). The single frequency conduction method used for calculating D_{it} can be expressed as

$$D_{it} = \frac{(2A/q)(G_{\max}/\omega)}{[(G_{\max}/\omega C_{ox})^2 + (1 - C_m/C_{ox})^2]}, \tag{2-1}$$

where A is the capacitor area, q is the electronic charge, ω is the angular frequency, C_{ox} is the oxide capacitance, G_{max} is the maximum conductance in the conductance-voltage (*G-V*) plot and its corresponding capacitance C_m [2.33]. The frequency f for the D_{it} analysis is 100 kHz. By using an optimum FGA condition (400 °C for 10 min.), hysteresis, frequency dispersion, and D_{it} can be further reduced by ~ 23 %, ~ 60 % and ~ 30 %, respectively, as

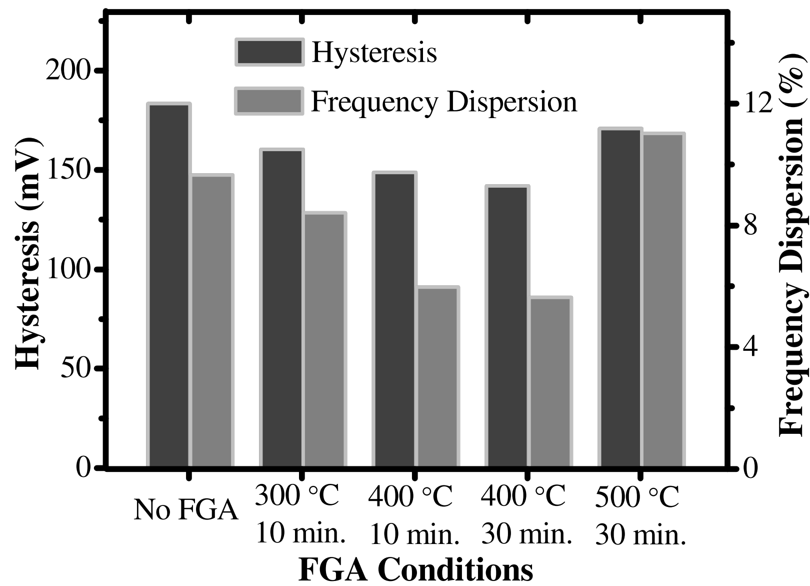


Fig. 2.8 A summary of hysteresis and frequency dispersion for a variety of FGA conditions for GaAs MOS capacitors.

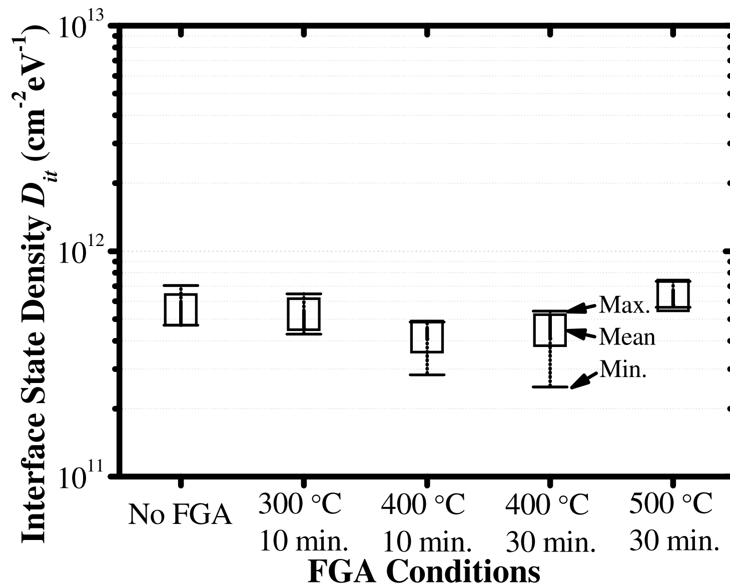


Fig. 2.9 D_{it} of the capacitors processed at different FGA conditions was extracted using the conductance method. About 30 % reduction in D_{it} can be achieved by using FGA at 400 °C for 10 min..

compared to a sample without FGA. There are two main considerations for an effective FGA. First, the annealing temperature needs to be sufficiently high for hydrogen to permeate into the gate stack for effective passivation, *i.e.* more than 300 °C. Second, excessive thermal budget, such as more than 500 °C for 30 minutes, may leads to interfacial reaction between high-*k* dielectric and GaAs, giving high D_{it}.

High S/D doping concentration reduces R_{SD} for higher I_{Dsat}. Next, the effect of additional P^+ co-implantation for increasing the N-type doping concentration is investigated. Fig. 2.10 compares the sheet resistance of N-type GaAs regions formed by Si^+ + P^+ co-implantation and by Si^+ implantation only at various dopant activation conditions. The sheet resistance of the N-type doped layer is determined from the slope of total resistance R_T versus contact spacing in transfer length method (TLM) test structures. Reduction in sheet resistance with increasing annealing temperature is observed, indicating better electrical activation of the implanted dopants. In all activation conditions, lower sheet resistance was achieved in the N-type regions with additional P^+ co-implantation. This is due to a reduced concentration of Si on As site acceptors (Si_{As}), whose formation is inhibited by additional P atoms [2.23]-[2.24]. P co-implant reduced the sheet resistance by ~35 % for the case here the activation anneal conditions was 850 °C for 10 s.

The next process module component to be developed for a GaAs device technology is the contact technology. PdGe ohmic contacts integrated on heavily N-type Si^+ + P^+ co-implanted regions demonstrate excellent ohmic behavior over a wide range of contact spacings (Fig. 2.11). To achieve ohmic behavior, the ratio of Ge over Pd should be greater than two so that excess Ge

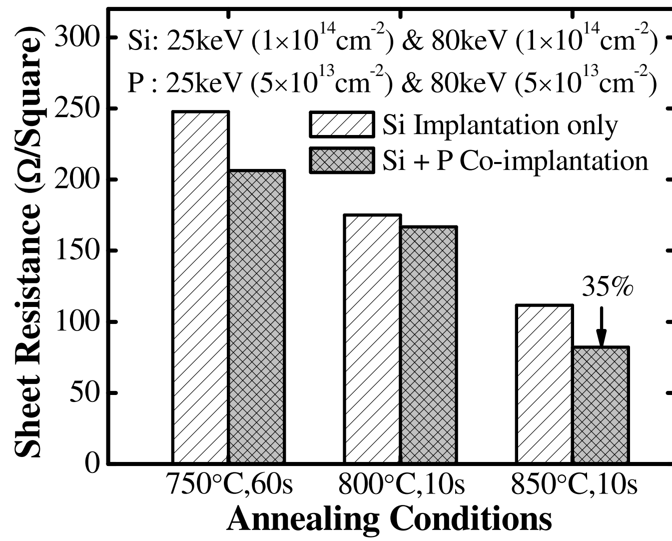


Fig. 2.10 Co-implantation of Si^+ with P^+ can boost the activation of Si as N-type dopants in GaAs. 35 % reduction in sheet resistance can be achieved. The sheet resistance was evaluated by using TLM test structures.

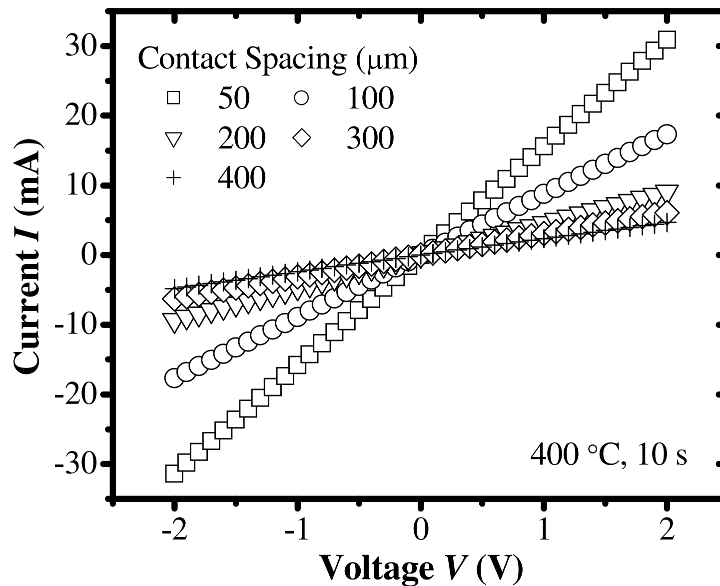


Fig. 2.11 PdGe contacts exhibit excellent ohmic *I-V* characteristics at different contact spacings (50, 100, 200, 300, and 400 μm) after contact formation at 400 °C for 10 s.

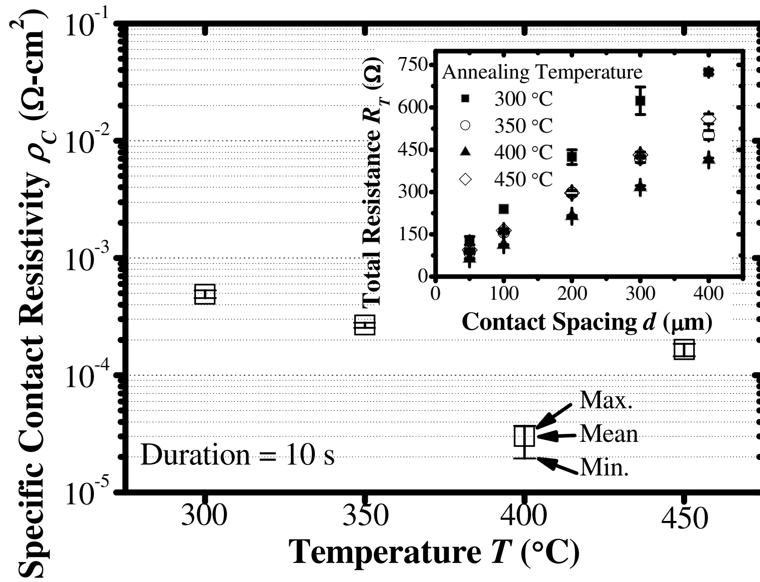


Fig. 2.12 Specific contact resistivity ρ_C at various formation temperatures was extracted using TLM test structures. The measured total resistance R_T versus contact spacing d is plotted in the inset.

can be transported across the palladium germanide and grown epitaxially on the GaAs substrate [2.34]-[2.35]. The effect of annealing temperature on PdGe formation is shown in Fig. 2.12. TLM test structures were employed to extract the specific contact resistivity ρ_C of the PdGe contacts [2.36]. Inset of Fig.2.12 shows the measured total resistance R_T as a function of various contact spacings with different annealing conditions. After annealing at 300 °C, Pd reacts with Ge to form PdGe. Since excess Ge exists, solid-phase transport and epitaxial growth of the Ge onto the GaAs will take place at higher temperature (~400 °C), leading to smaller ρ_C. After transport and epitaxy, GaAs will be separated from the PdGe by the grown Ge layer, as shown in Fig. 2.13. Lowest ρ_C of ~ 2.8×10^{-5} Ω-cm^2 can be obtained after annealing at 400 °C for 10 s. This is higher than ρ_C of ~ 10^{-6} Ω-cm^2 obtained in [2.34]. ρ_C could be reduced further with more process optimization.

Fig. 2.13 shows a schematic of the fabricated GaAs N-MOSFET as well as transmission electron microscopy (TEM) images of the *in-situ* SiH_4-passivated gate stack and PdGe ohmic contact region. Note that all the TEM results in this thesis were not obtained by me. An oxidized Si interfacial layer of ~ 1 nm was formed between HfAlO dielectric and GaAs, replacing the low quality native oxide. The composition of PdGe contact was investigated by energy dispersive X-ray (EDX) analysis. This PdGe based contact scheme can achieve smooth contact interface and low contact resistivity on N-type GaAs,

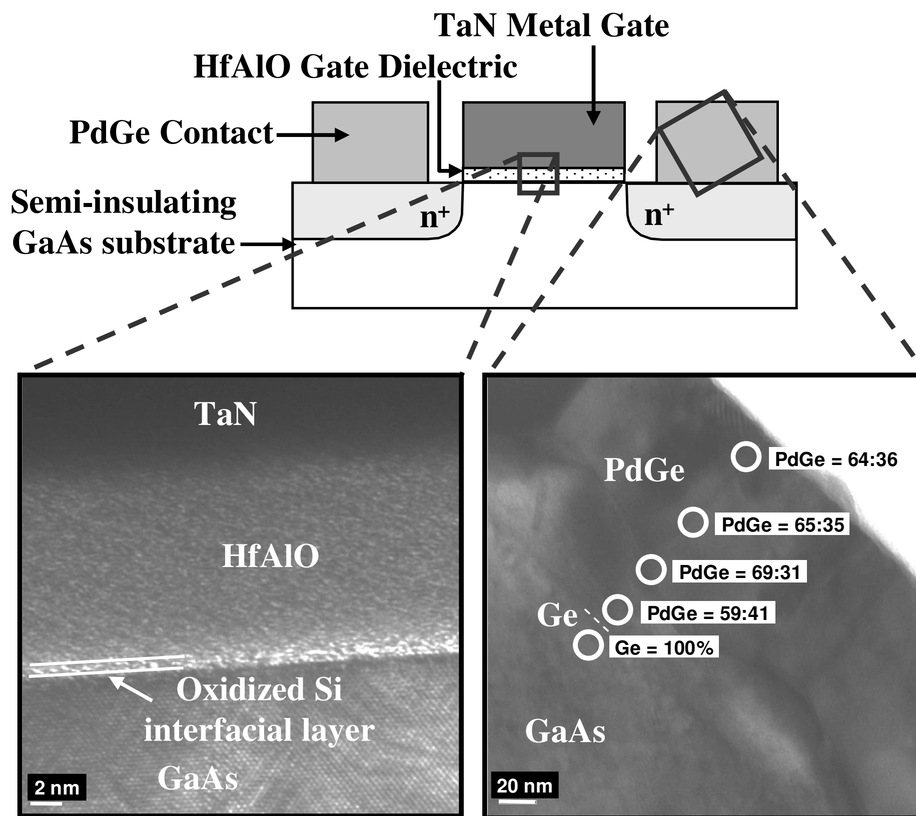


Fig. 2.13 Schematic and TEM pictures showing the key features of the GaAs N-MOSFET fabricated in this experiment: TaN/HfAlO gate stack formed with *in-situ* surface passivation process as well as a PdGe ohmic contact technology. An oxidized Si interfacial layer (~ 1 nm) was formed between HfAlO dielectric and GaAs. EDX analysis of the contact region reveals the composition of PdGe ohmic contact. A Ge layer was epitaxially grown on the GaAs surface by solid phase regrowth during contact formation.

which was also reported by [2.34]-[2.35]. This is the first successful integration of gold-free ohmic contacts on III-V MOSFET, suggesting PdGe is a possible alternative to replace gold-based contacts, which are commonly employed in many GaAs devices [2.9], [2.11], [2.13], [2.14], [2.18], [2.21], [2.22].

Fig. 2.14(a) plots the $I_{DS} - V_{GS}$ transfer characteristics of a GaAs N-MOSFET with *in-situ* SiH_4 surface passivation. Control transistors without *in-situ* surface passivation did not yield in our experiment, mainly due to the high interface state density and high gate leakage current. Threshold voltage V_T of this GaAs device with a gate length (L_G) of 3 μm is 0.44 V, as determined by linear extrapolation from the maximum transconductance at V_{DS} of 50 mV. Inset of Fig. 2.14(a) plots the transconductance G_m characteristics

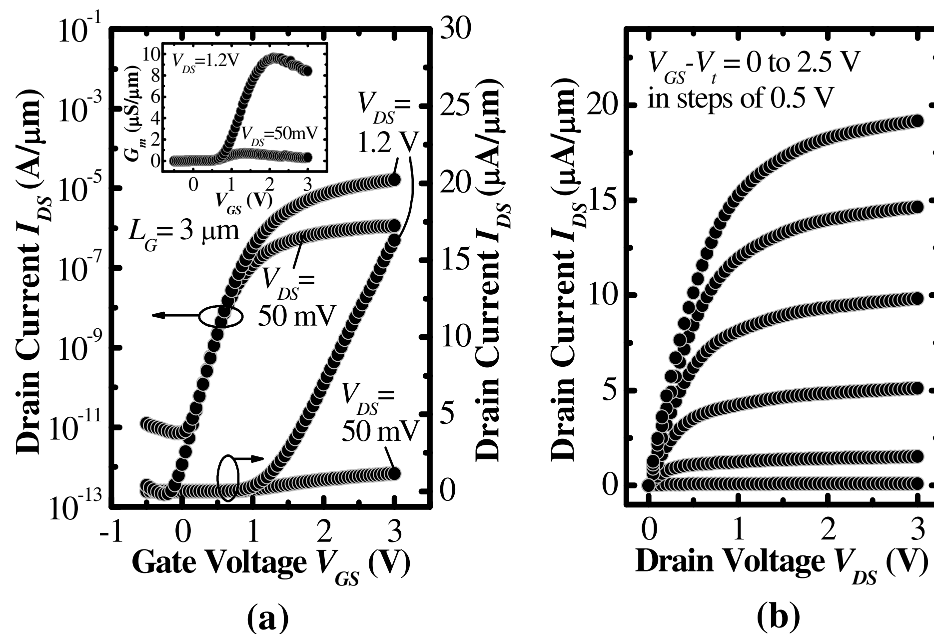


Fig. 2.14 (a) I_{DS}-V_{GS} curves of a surface channel GaAs MOS transistor with self-aligned S/D and L_G of 3 μm, showing good output characteristics. Inset plots the transconductance characteristics of the GaAs device. (b) I_{DS}–V_{DS} characteristics of the GaAs N-MOSFET at various gate overdrives.

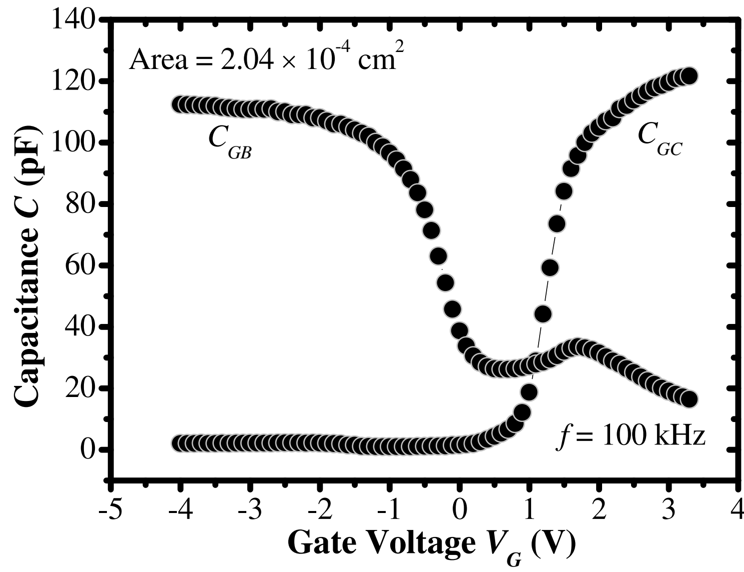


Fig. 2.15 Gate-to-bulk capacitance C_{GB} versus V_G and gate-to-channel capacitance C_{GC} versus V_G characteristics of a GaAs transistor.

of the GaAs transistor. The I_{DS}–V_{DS} characteristics of the GaAs device are shown in Fig. 2.14(b). This GaAs transistor demonstrates excellent saturation and pinch-off characteristics with reasonably low series resistance, even with a large separation of 5 μm between gate and S/D contacts. Much higher drive current and transconductance are expected when the EOT and the gate-to-contact separation are reduced.

Fig. 2.15 illustrates the gate-to-bulk capacitance C_{GB} as well as gate-to-channel capacitance C_{GC} of the GaAs N-MOSFET. EOT of this GaAs transistor is ~ 5.7 nm. Fig. 2.16 plots the extracted effective mobility μ_{eff} versus effective field E_{eff}, showing high peak electron mobility of 1150 cm^2/Vs. The effective electron mobility is extracted based on split C-V method [2.36] by using the I_D-V_{GS} characteristics at V_{DS} of 50 mV [Fig. 2.14(a)] and the total inversion charge density, which is obtained by integrating the measured C_{GC} curve [Fig. 2.15]. E_{eff} was obtained by dividing

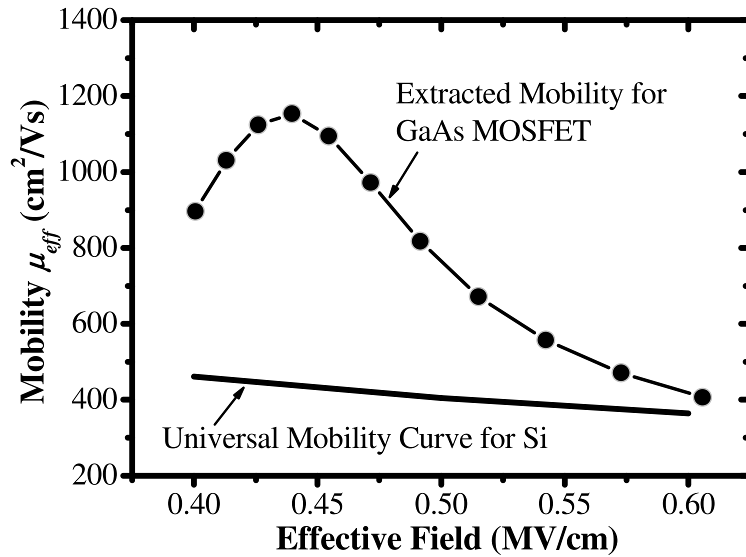


Fig. 2.16 Plot of effective carrier mobility μ_{eff} as a function of effective field for a surface channel GaAs N-MOSFET.

the total inversion charge density and depletion charge density with semiconductor dielectric function. It should be noted that the mobility extraction was done without correction for series resistance effects. The reduction in mobility at higher field is due to surface roughness scattering.

2.2.1.3 Summary

In summary, the impact of PDA and FGA conditions on the electrical characteristics of TaN/HfAlO/GaAs gate stack with *in-situ* vacuum anneal and SiH_4 passivation were studied systematically. Excellent *C-V* characteristics with low frequency dispersion of ~ 6 % and small hysteresis of ~ 150 mV can be achieved using optimized processing conditions. Using the *in-situ* surface passivation technique for gate stack formation, a self-aligned N-MOSFET with good transfer characteristics and high peak carrier mobility of 1154 cm^2/Vs was demonstrated.

2.2.2 $In_{0.18}Ga_{0.82}As$ N-MOSFET with *In-situ* SiH_4 Passivation

With a higher electron mobility than GaAs, InGaAs is more attractive for high speed CMOS logic applications. In this section, *in-situ* SiH_4 surface passivation technology was investigated to achieve high-quality gate stack on strained $In_{0.18}Ga_{0.82}As$. The physics and origin of this surface passivation technology for realizing high quality III-V gate stacks is extensively investigated.

2.2.2.1 Experiment

P-type Zn-doped (100)-oriented GaAs wafers with N_A of 1 - 5 × 10^{16} cm^{-3} were used as starting substrates. 100 nm Zn-doped GaAs buffer layer with N_A of 1 × 10^{17} cm^{-3} was then grown by Aixtron MOCVD reactor using trimethylgallium (TMGa), tertiarybutylarsine (TBA), and trimethylindium (TMIn) as precursors and H_2 as the carrier gas. Diethylzinc (DEZn) was also introduced into the reactor to dope the InGaAs epilayer with N_A of 1 × 10^{17} cm^{-3}. To prevent strain relaxation, thickness of the $In_{0.18}Ga_{0.82}As$ layer is limited to ~ 20 nm. After MOCVD epitaxial process, three step pre-gate clean in HCl, NH_4OH, and $(NH_4)_2S$ was carried out. The wafers were then quickly loaded into multiple-chamber gate cluster system for vacuum anneal at 600 °C for 60 s, SiH_4 treatment at a range of temperature from 300 to 500 °C for 60 s and at process pressure of 5 Torr (the flow rates of SiH_4 and N_2 are 60 and 250 sccm, respectively), and HfAlO high-*k* dielectric deposition. On a control wafer, vacuum anneal and SiH_4 treatment steps were skipped. PDA at 500 ˚C for 60 s was then performed to improve the quality of as-deposited HfAlO film. After reactive sputter deposition of TaN metal gate and gate

patterning, the fabrication process was completed with FGA (15 % H_2 and 85 % N_2) at 400 ^{o}C.

2.2.2.2 Results and Discussion

A. Physical Characterization of InGaAs Epilayer

The crystal quality of the 20 nm strained $In_{0.18}Ga_{0.82}As$ layer on GaAs was examined by high resolution X-ray diffraction (HRXRD) analysis. Fig. 2.17 shows the high resolution rocking curve of the (004) reflection from the InGaAs/GaAs heterostructure. The interface quality of the structure is confirmed by the clear interference pattern or Pendellösung oscillations in the rocking curve. This interference originates from the beating of X-ray wave fields inside the crystal which has almost perfectly parallel boundaries. The peak positions of the interference pattern are consistent with the Bragg angle θ calculated by using $2d \sin\theta = n\lambda$, where n is 138, 139, 140, and 141 for

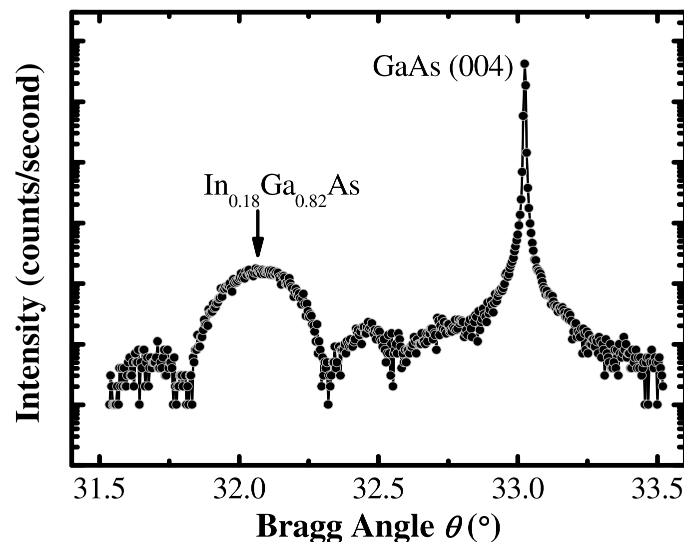


Fig. 2.17 High resolution XRD rocking curve of the (004) reflection on the $In_{0.18}Ga_{0.82}As$/GaAs structure. The clear interference pattern in the rocking curve reveals the high interface quality of the InGaAs structure.

wavelength λ of 1.54 Å and thickness d of 20 nm. The mismatch in lattice constants between $In_{0.18}Ga_{0.82}As$ and GaAs leads to the following homogeneous biaxial strain in the InGaAs epilayer, with z as the growth direction:

$$\varepsilon_{xx} = \varepsilon_{yy} = -\frac{a_{InGaAs} - a_{GaAs}}{a_{GaAs}}, \tag{2-2}$$

$$\varepsilon_{zz} = -\frac{2\sigma}{1-\sigma}\varepsilon_{xx} = -\frac{2\sigma}{1-\sigma}\varepsilon_{yy}, \text{ and} \tag{2-3}$$

$$\varepsilon_{xy} = \varepsilon_{yz} = \varepsilon_{zx} = 0, \tag{2-4}$$

where a_{InGaAs} is the lattice constant of unstrained $In_{0.18}Ga_{0.82}As$, a_{GaAs} is the lattice constant of bulk GaAs, and σ is the Poisson coefficient of InGaAs, which is 0.31. a_{InGaAs} of 5.726 Å is obtained from linear interpolation between a_{GaAs} of 5.653 Å and lattice constant of InAs a_{InAs} of 6.058 Å. Therefore, ε_{xx} and ε_{yy} of the InGaAs layer is -1.29 % and ε_{zz} is 1.16 %. As surface roughness can degrade the effective carrier mobility of surface channel transistor, atomic

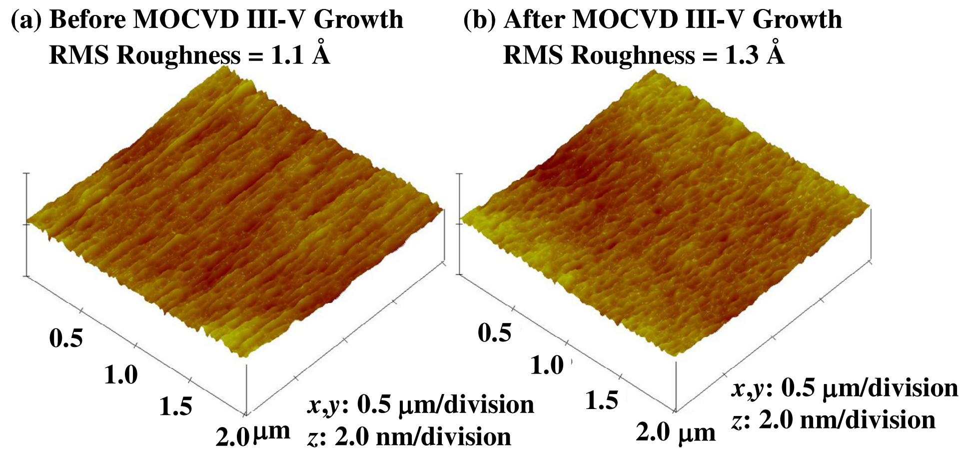


Fig. 2.18 AFM images of (a) GaAs before InGaAs growth, showing RMS surface roughness of 1.1 Å. (b) After the growth of $In_{0.18}Ga_{0.82}As$, the RMS surface roughness is 1.3 Å.

force microscopy (AFM) analysis was employed to investigate the surface morphology of the strained InGaAs epilayer. Fig. 2.18 shows the AFM images of (a) GaAs before MOCVD epitaxial process with root-mean-square (RMS) roughness of 1.1 Å, and (b) InGaAs after epitaxial process with RMS roughness of 1.3 Å. The surface roughness can be maintained after MOCVD III-V epitaxial process.

B. Physical Characterization of InGaAs Surfaces and MOS Stacks

X-ray photoelectron spectroscopy (XPS) analysis was employed to study the interfacial chemical bonding between high-*k* dielectric and InGaAs. The thickness of HfAlO is 1 nm so that the HfAlO/InGaAs interface is probe-able. Arsenic oxide was reported to act as defective states in the bandgap and play a critical role in the degradation of device performance [2.12], [2.37]. The As 3*d* core level spectra in Fig. 2.19 indicates that As-O bond at 44.6 eV was eliminated after vacuum anneal and SiH_4 passivation. The elimination of arsenic oxide may explain the improved electrical properties of the MOS capacitors with vacuum anneal and SiH_4 passivation. In addition, Si-O bond at 103.9 eV was observed in the Si 2*p* spectra of the samples with vacuum anneal and SiH_4 passivation (Fig. 2.20), indicating that the thin Si interfacial layer was oxidized.

Fig. 2.21 shows HRTEM micrographs of the fabricated strained InGaAs MOS capacitors: (a) without vacuum anneal and SiH_4 passivation, and (b) with vacuum anneal and SiH_4 passivation. The thickness of $In_{0.18}Ga_{0.82}As$ epilayer is ~ 20 nm. Fast Fourier transform diffractogram reveals good crystallinity of the strained InGaAs layer [inset of Fig. 2.21(a)]. HRTEM

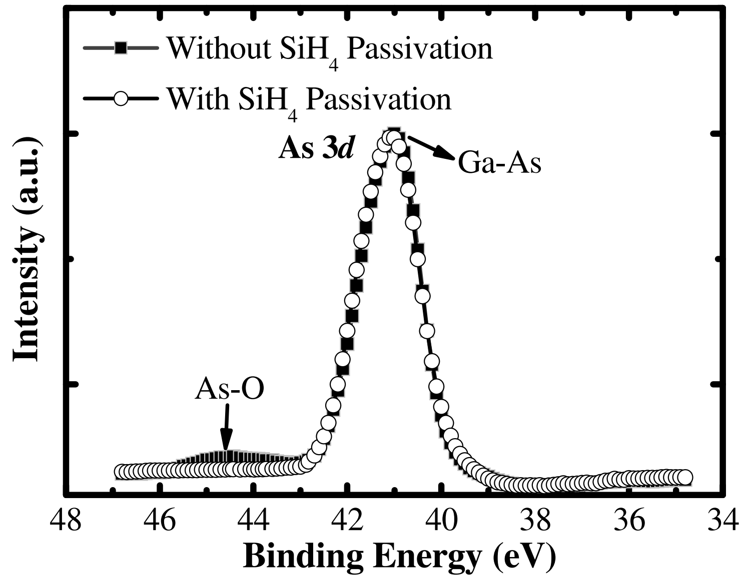


Fig. 2.19 As 3*d* XPS spectra show the significant reduction in As-O bond signal after vacuum anneal and SiH_4 treatment.

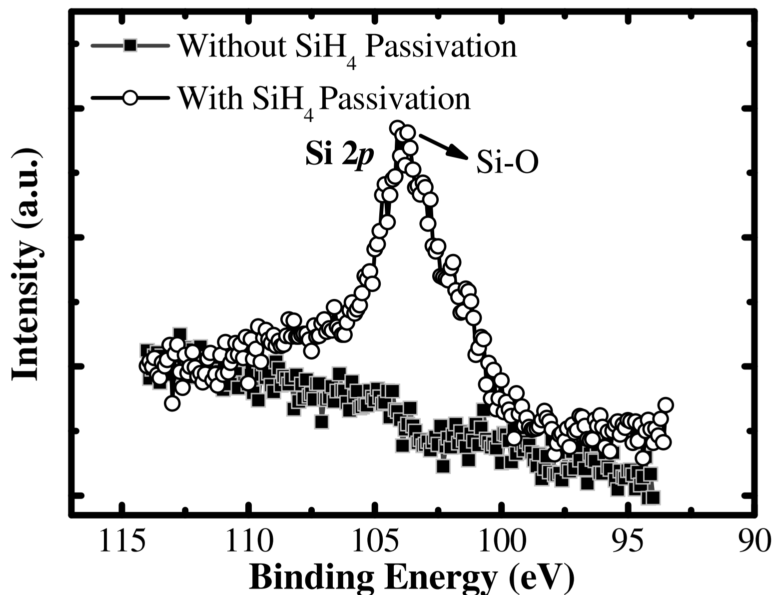


Fig. 2.20 Si 2*p* spectra verify the existence of Si-O bond at the interface in the samples with vacuum anneal and SiH_4 passivation, indicating that the thin Si interfacial layer was oxidized.

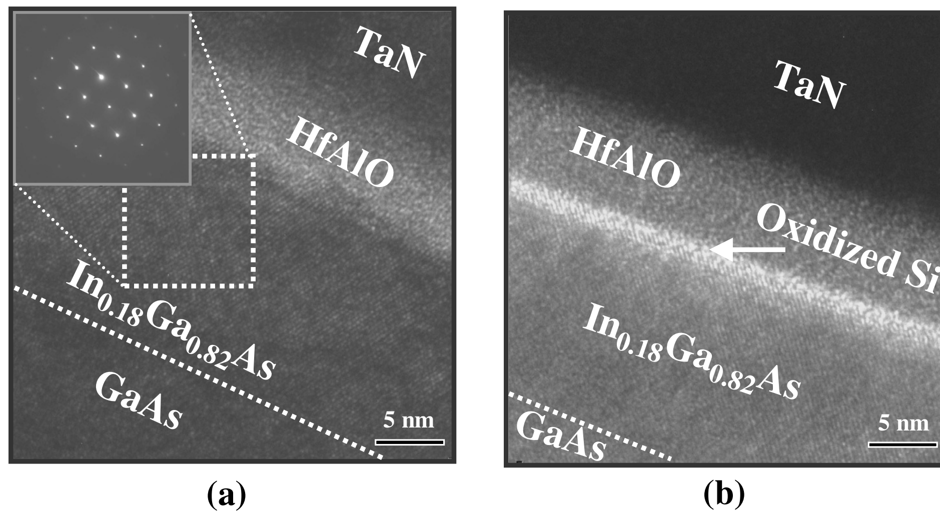


Fig. 2.21 HRTEM micrographs showing the cross-section of a completed TaN/HfAlO/InGaAs stack: (a) without, and (b) with vacuum anneal and SiH_4 passivation. In the samples with vacuum anneal and SiH_4 treatment, an oxidized silicon layer was observed. Diffractogram in the inset reveals excellent crystalline quality of the strained $In_{0.18}Ga_{0.82}As$ layer.

image in Fig. 2.21(b) shows an oxidized silicon layer with thickness of ~ 1.3 nm at the interface between HfAlO and InGaAs.

C. Electrical Characterization of InGaAs MOS Stacks

Fig. 2.22 reveals the *C-V* characteristics of InGaAs capacitors formed with and without SiH_4 passivation at various measuring frequencies. The SiH_4-passivated InGaAs capacitors exhibit excellent *C-V* characteristics with negligible frequency dispersion and smaller stretch-out. Significant reduction in hysteresis was also achieved (Fig. 2.23). A higher SiH_4 treatment temperature reduces hysteresis, possibly due to densification of the silicon interfacial layer. Fig. 2.24 plots D_{it} at various SiH_4 treatment temperatures, showing the effectiveness of SiH_4 passivation on InGaAs. D_{it} was evaluated using single-frequency *C-V* and *G-V* at 100 kHz. Fig. 2.25 plots the gate

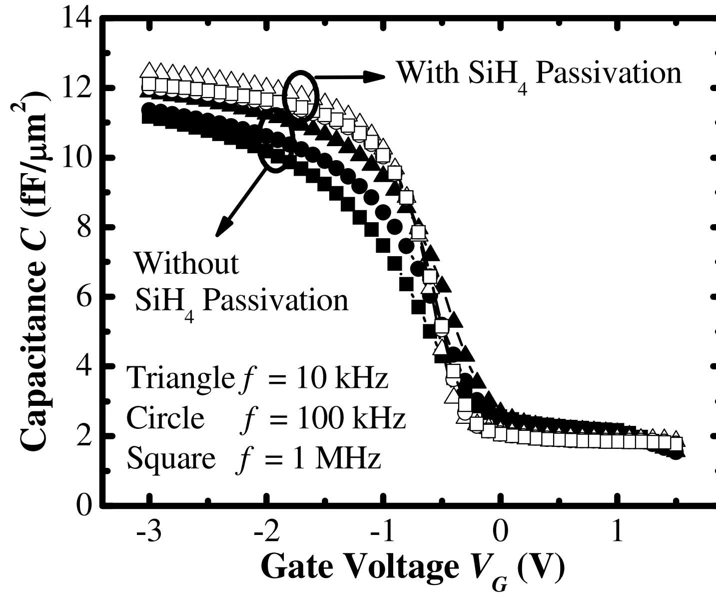


Fig. 2.22 *C-V* characteristics of TaN/HfAlO/InGaAs MOS capacitors characterized at frequencies of 10 kHz, 100 kHz and 1 MHz. Significant reduction in frequency dispersion was achieved with SiH_4 passivation.

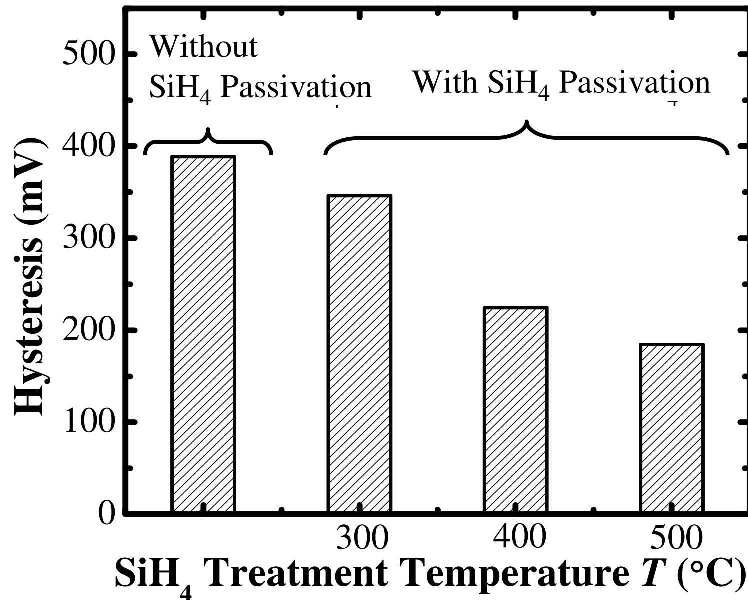


Fig. 2.23 Hysteresis versus SiH_4 treatment temperature ranging from 300 ˚C to 500 ˚C.

leakage current density J_G versus EOT. EOT was determined by comparing the accumulation capacitance with simulated C-V data. A reduction in J_G was observed in the SiH_4-passivated gate stack, which is likely attributed to suppressed surface states assisted tunneling [2.38]. With EOT of 2.3 nm, the InGaAs MOS capacitor demonstrates a low J_G of 1.54×10^{-5} A/cm^2 at $V_G = V_{FB} - 1$ V.

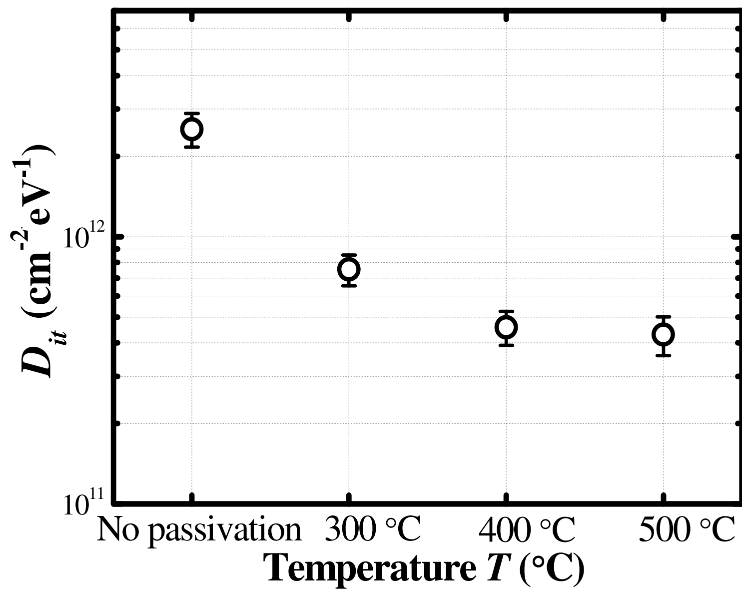


Fig. 2.24 D_{it} at various SiH_4 treatment temperatures. D_{it} as low as 3.5×10^{11} to 5.0×10^{11} cm^{-2}eV^{-1} can be achieved with additional SiH_4 treatment.

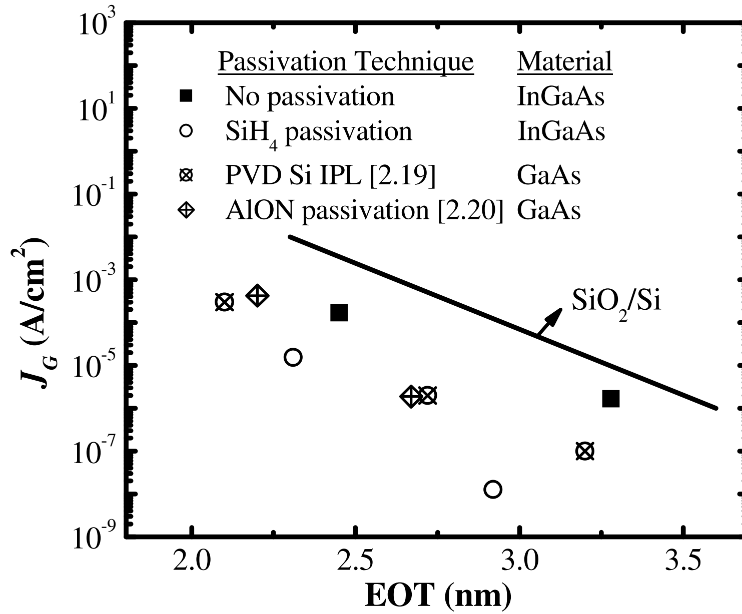


Fig. 2.25 The gate leakage current density J_G obtained at $V_G = V_{FB}$ - 1 V as a function of EOT.

2.2.2.3 Summary

In-situ SiH_4 surface passivation was applied on strain InGaAs to achieve high quality MOS gate stack. By introducing vacuum anneal for decomposition and desorption of native oxide and SiH_4 passivation, InGaAs capacitors with EOT of 2.3 nm was fabricated, demonstrating good *C-V* characteristics with D_{it} as low as $3.5 \times 10^{11} - 5.0 \times 10^{11}$ $cm^{-2}eV^{-1}$ and low J_G of 1.54×10^{-5} A/cm^2 at $V_G = V_{FB}$ - 1 V.

2.3 III-V Channel N-MOSFETs with *In-situ* SiH_4 + NH_3 Passivation

In this section, surface passivation employing a silane-ammonia gas mixture (SiH_4 + NH_3) is used to realize high quality MOS stacks on GaAs and InGaAs compound semiconductors. Section 2.3.1 and 2.3.2 show high quality gate stack formation on GaAs, and $In_{0.53}Ga_{0.47}As$, respectively, using *in-situ* vacuum anneal and SiH_4 + NH_3 passivation technology.

2.3.1 GaAs N-MOSFET with *In-situ* SiH_4 + NH_3 Passivation

In this section, SiH_4 + NH_3 surface passivation technology is presented to realize very high quality metal-gate/high-*k* dielectric stack on GaAs. Compared to a SiH_4-only passivation in Section 2.2, the addition of NH_3 improves the interfacial quality, providing better *C-V* characteristics and achieving lower interface state density. The SiH_4 + NH_3 passivation technology was integrated in enhancement-mode GaAs N-MOSFETs, together with a Hf-based gate dielectric.

2.3.1.1 Experiment

P-type Zn-doped (100)-oriented GaAs wafers with N_A of 1 - 5 × 10^{16} cm^{-3} were used in this experiment. After a three step pre-gate cleaning process similar to the one described in Section 2.2.1.1, the wafers were then quickly loaded into a multiple-chamber gate cluster system. Vacuum anneal at 600 °C for 60 s was performed before SiH_4 + NH_3 passivation at 400 °C for 60 s at a process pressure of 5 Torr (the flow rates of SiH_4, NH_3 and N_2 were 60, 60 and 250 sccm, respectively). To investigate the effect of the SiH_4 + NH_3

passivation, another three experimental splits were involved. In the first split, vacuum-annealed GaAs wafers went straight to HfAlO deposition, skipping the surface passivation step. In the second split, vacuum annealed GaAs wafers were passivated with SiH_4 only, followed by HfAlO deposition. In the last split, HfAlO was deposited on (100) Si wafers without surface treatment.

PDA at 500 °C for 60 s was performed prior TaN metal deposition. After gate patterning, S/D regions were formed by Si^+ and P^+ implantation at doses of 1×10^{14} cm^{-2} and 5×10^{13} cm^{-2}, respectively, and dopant activation at 850 °C in N_2 ambient. In the MOS capacitor fabrication, implant anneal at 850 °C was skipped in some samples for comparison. FGA at 400 °C was also done for all samples before PdGe metallization.

2.3.1.2 Results and Discussion

Fig. 2.26 compares the *C-V* characteristics of GaAs MOS capacitors with and without SiH_4 + NH_3 passivation before implant anneal at different measurement frequencies. EOT of the GaAs MOS capacitors with and without SiH_4 + NH_3 passivation are 2.3 nm and 2.8 nm, respectively. TaN/HfAlO/Si capacitors without implant anneal are also compared. EOT of GaAs capacitors with and without SiH_4 + NH_3 passivation at about 0.25-0.4 eV above valence band edge were estimated to be ~1×10^{11} and ~8×10^{11} $cm^{-2}eV^{-1}$, respectively. The midgap D_{it} of the Si capacitor was estimated to be ~7×10^{10} $cm^{-2}eV^{-1}$.

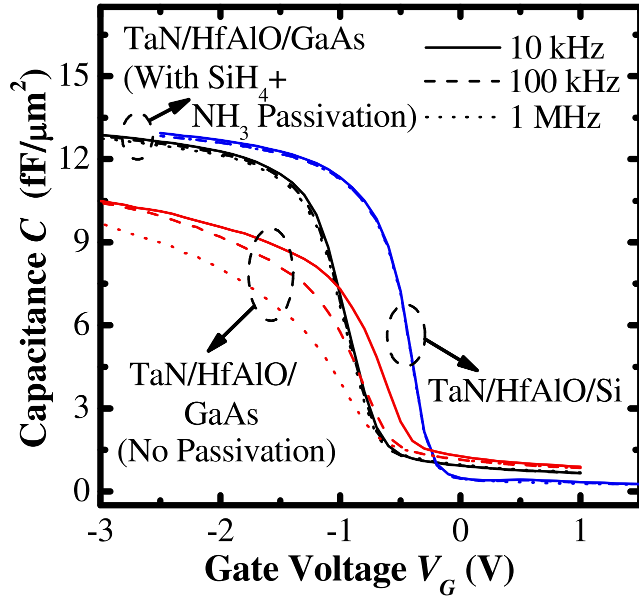


Fig. 2.26 *C-V* characteristics of GaAs MOS capacitors with and without SiH_4 + NH_3 passivation and before an implant anneal to simulate dopant activation process. *C-V* characteristics of a Si capacitor without implant anneal are also plotted for comparison. The SiH_4 + NH_3-passivated GaAs capacitor reveals electrical behavior comparable to Si capacitor.

Next, thermal stability of the gate stacks with and without implant anneal of 850 °C was investigated (Fig. 2.27). D_{it} of the SiH_4 + NH_3-passivated GaAs capacitors increased to ~7×10^{11} $cm^{-2}eV^{-1}$ after the implant anneal (inset of Fig. 2.27). Nevertheless, it is still much better than ~2.2×10^{12} $cm^{-2}eV^{-1}$ for capacitors without surface passivation. Gate-last low thermal budget fabrication process flow can be employed to take full advantage of this surface passivation technology. Hysteresis of the SiH_4 + NH_3-passivated GaAs capacitors with and without implant anneal is ~0.15 V and ~0.24 V, respectively. Hysteresis, caused by bulk oxide traps, can be improved through optimizing the PDA conditions.

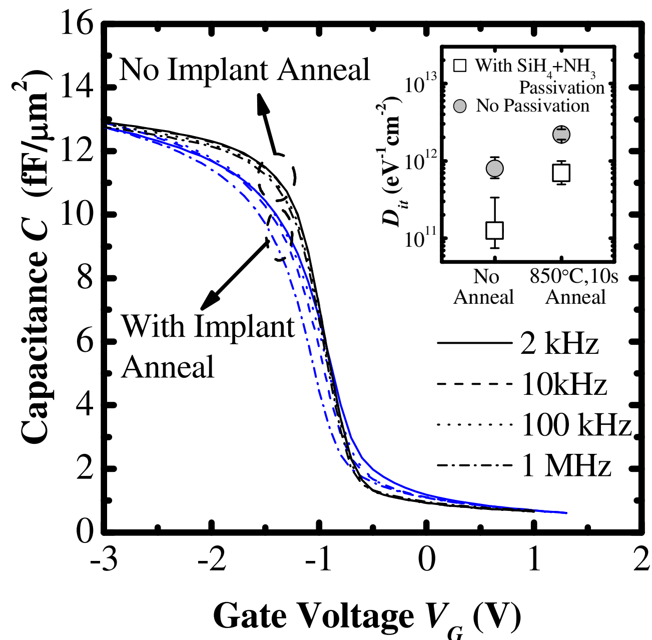


Fig. 2.27 *C-V* characteristics of SiH_4 + NH_3-passivated GaAs MOS capacitors before and after anneal. D_{it} of GaAs MOS capacitors with and without SiH_4 + NH_3 passivation at various implant anneal conditions was summarized in inset.

XPS was employed to investigate the interfacial chemical bonding between high-*k* dielectric and GaAs. The As 3*d* core level spectra in Fig. 2.28(a) provides clear evidence that SiH_4 + NH_3 passivation eliminates the As-O bond (at 44.6 eV) and forms the As-N bond. The NH_3 in the SiH_4 + NH_3 passivation is responsible for this effect, and is one of the key improvements made in this work. It is also likely that hydrogen dissociated from NH_3 passivates dangling bonds on the surface of GaAs and thereby decreases D_{it}. Furthermore, the Si-N layer on GaAs can protect the surface from the oxidizing ambient during a subsequent high-*k* dielectric deposition, while itself was oxidized to form silicon oxynitride SiO_xN_y, as confirmed by the Si 2*p* spectra in Fig. 2.28(b).

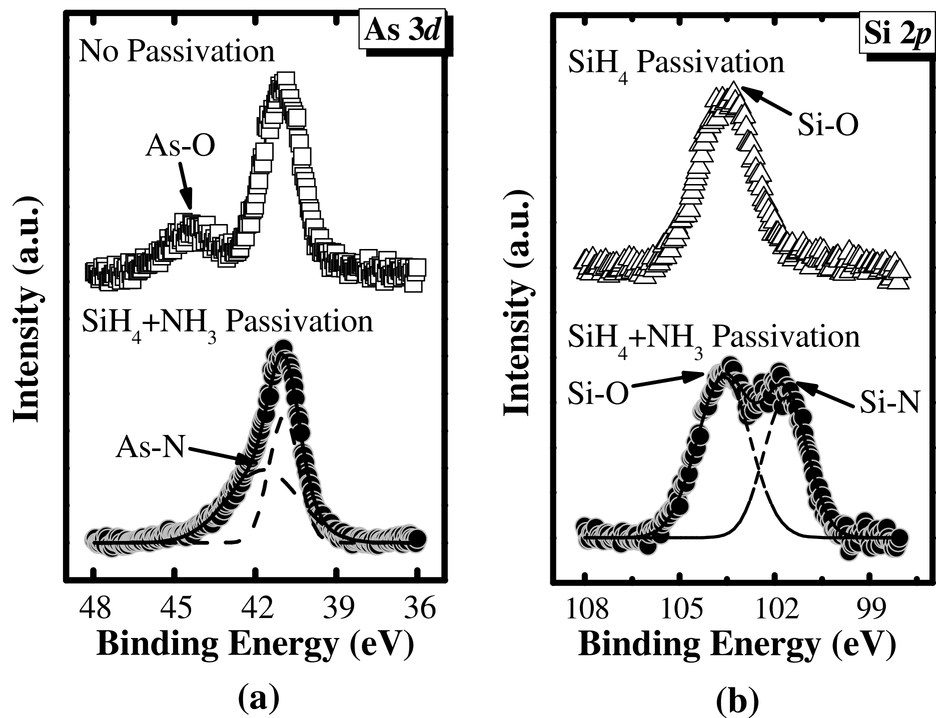


Fig. 2.28 High-resolution XPS spectra reveal the bonding structure at the HfAlO/GaAs. (a) As 3*d* spectra show the suppression of As-O bond after passivation, contributing to the improved interfacial quality. (b) Si 2*p* spectra show that SiO_xN_y interlayer was formed with the SiH_4 + NH_3 passivation, while SiO_x was formed with the SiH_4-only passivation.

TEM and SEM images in Fig. 2.29 show the fabricated GaAs N-MOSFET with TaN/HfAlO gate stack and gold-free PdGe S/D ohmic contact. The separation between the edge of the gate stack and PdGe contact is ~ 600 nm. Novel contact formation approach such as self-aligned contact metallization is needed to reduce the R_{SD} for further performance improvement.

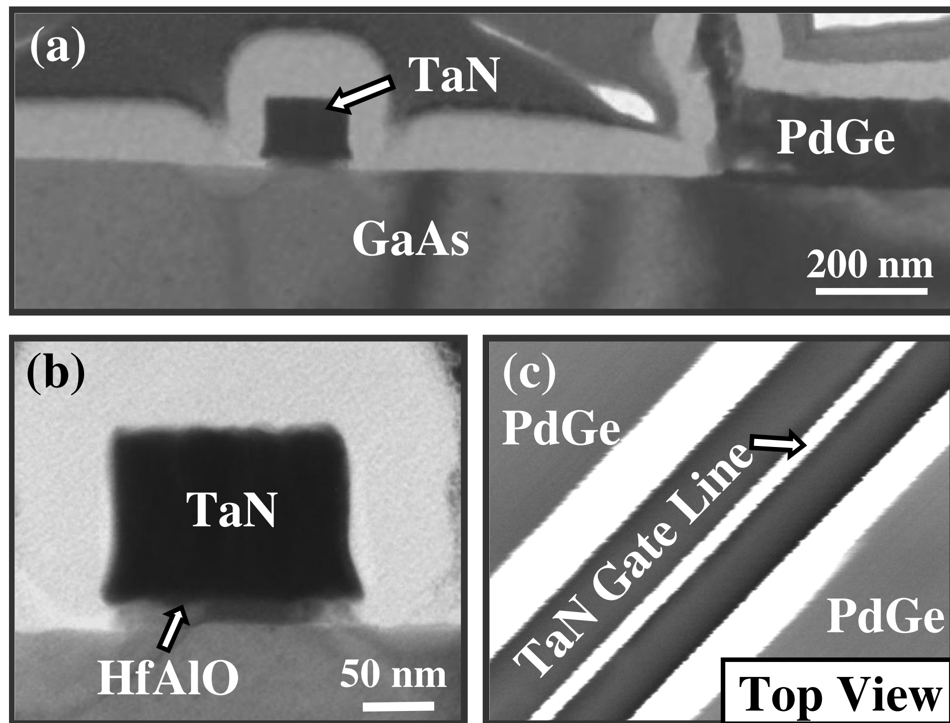


Fig. 2.29 (a), (b) TEM micrographs of a GaAs MOSFET with L_G of 160 nm and gold-free PdGe contact. (c) Top SEM image of the GaAs transistor.

Fig. 2.30 shows the *I-V* characteristics of a GaAs N-MOSFET with L_G of 250 nm. This surface channel GaAs N-MOSFET has a V_T of 0.55 V, drain-induced barrier lowering (DIBL) of 0.23 V/V, and subthreshold swing (SS) of 160 mV/decade. The short channel effect can be improved by shallower S/D implant conditions and higher channel doping concentration. Next, Fig. 2.31 shows the *I-V* characteristics of another GaAs N-MOSFET with L_G of 2 μm. This MOSFET has negligible DIBL, and SS of 98 mV/decade. Unlike narrow bandgap III-V MOSFETs that may suffer from high source-to-drain leakage due to band-to-band tunneling and thermal generation of minority carriers, GaAs N-MOSFETs provides a high I_{on}/I_{off} ratio of ~10^5 (I_{on} at V_G = 1.2V and V_D = 1.2V, I_{off} at V_G = 0V and V_D = 1.2V) and a low source-to-drain leakage

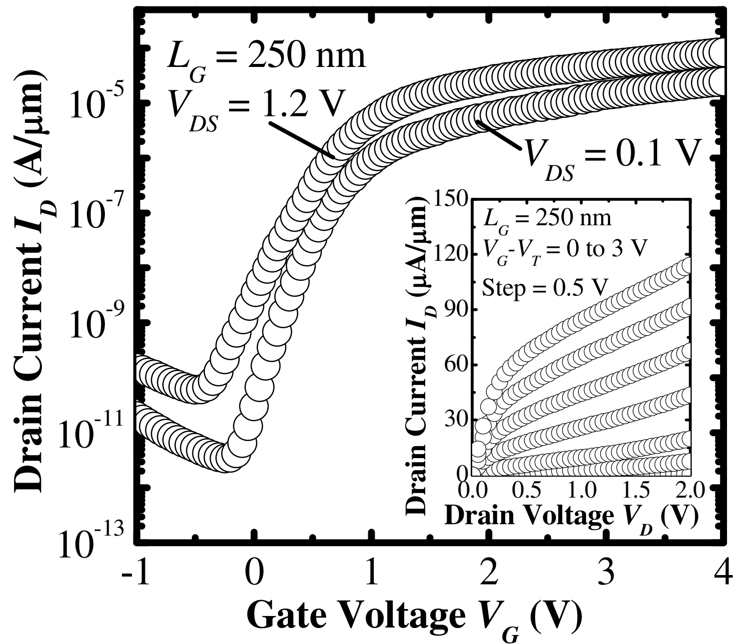


Fig. 2.30 I_D-V_G characteristics of SiH_4 + NH_3-passivated GaAs N-MOSFETs with L_G of 250 nm, showing good output characteristics. Inset plots the I_{DS}–V_{DS} curves of the GaAs device at various gate overdrives.

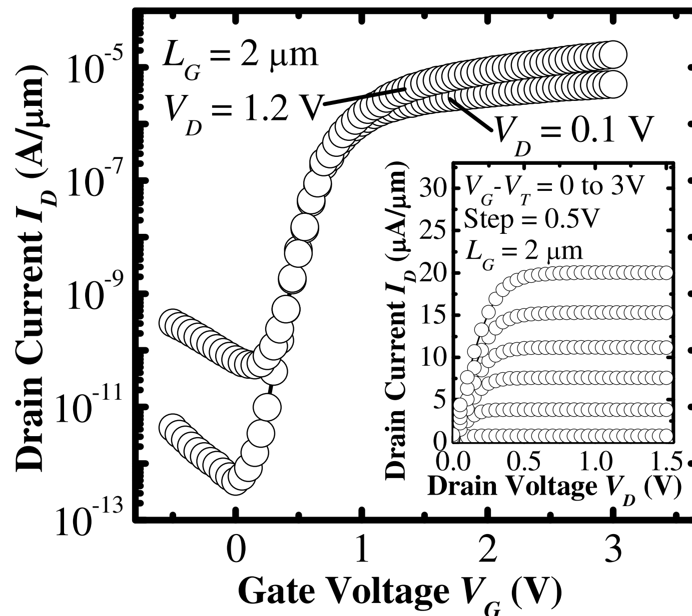


Fig. 2.31 I_D-V_G characteristics of SiH_4 + NH_3-passivated GaAs N-MOSFETs with L_G of 2 μm, showing good output characteristics. Inset plots the I_{DS}–V_{DS} curves of the GaAs device at various gate overdrives. The GaAs transistor demonstrates excellent saturation and pinch-off characteristics.

due to the large bandgap of GaAs. EOT and hysteresis of the GaAs MOSFETs are 4.2 nm, and ~0.22 V, respectively. Despite a gate-first high thermal budget process adopted here, the TaN/HfAlO/GaAs gate stack with SiH_4 + NH_3 surface passivation demonstrates high quality and good robustness.

Fig. 2.32 plots μ_{eff} of a SiH_4 + NH_3-passivated GaAs N-MOSFET versus the effective vertical field E_{eff}. The inversion carrier densities of the MOSFET are ~4.2 × 10^{11} cm^{-2} at E_{eff} of 0.1 MV/cm^2 and ~5.6 × 10^{12} cm^{-2} at E_{eff} of 0.5 MV/cm^2. Using conductance method at room temperature, the D_{it} of the MOSFET was estimated to be ~ 8×10^{11} $cm^{-2}eV^{-1}$. This GaAs N-MOSFET has a peak electron mobility of ~1920 cm^2/Vs after correction for interface trap charges [2.39]. The occurrence of peak mobility at lower effective field, as compared to Fig. 2.16, is due to lower channel doping concentration.

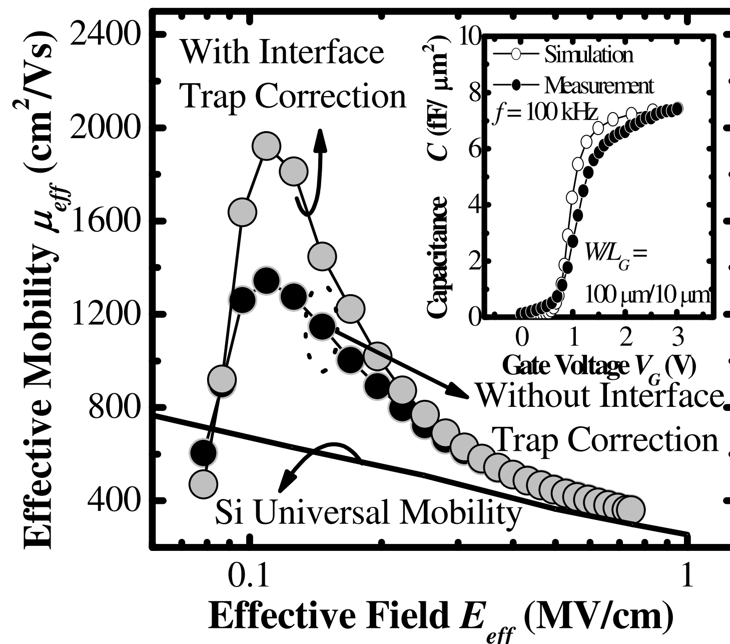


Fig. 2.32 Plot of μ_{eff} versus E_{eff} for a GaAs N-MOSFET. After correction for presence of interface trap charges, the peak electron mobility is ~1920 cm^2/Vs. The inset shows the simulated and measured inversion *C-V* characteristics of the GaAs N-MOSFET.

2.3.1.3 Summary

Surface passivation technique based on a $SiH_4 + NH_3$ gas mixture was demonstrated for achieving high-quality gate stack on GaAs. Significant improvement in interfacial properties is attributed to the desorption of native oxide during vacuum anneal and the formation of SiO_xN_y protective interfacial layer. Incorporation of this technology in the fabrication of an inversion-type GaAs N-MOSFET was also demonstrated.

2.3.2 InGaAs N-MOSFET with *In-situ* $SiH_4 + NH_3$ Passivation

In this section, $SiH_4 + NH_3$ passivation technology was applied on InGaAs with a higher indium composition, $In_{0.53}Ga_{0.47}As$. Significant improvement in D_{it}, SS, and I_{off} over control was achieved in $In_{0.53}Ga_{0.47}As$ MOSFETs.

2.3.2.1 Experiment

P-type Be-doped (100)-oriented $In_{0.53}Ga_{0.47}As$/InP substrates were used for this technology demonstration. The N_A of the 1 μm thick $In_{0.53}Ga_{0.47}As$ layer is 1 - 5 × 10^{16} cm^{-3}. After pre-gate clean in HCl, NH_4OH, and $(NH_4)_2S$, the wafers were loaded into a multiple-chamber MOCVD gate cluster system for vacuum anneal at 520 °C for 60 s at process pressure of ~ 1 × 10^{-5} Torr, and $SiH_4 + NH_3$ treatment at 400 °C for 60 s. For the control devices, vacuum anneal and $SiH_4 + NH_3$ passivation were skipped. MOCVD HfAlO high-*k* dielectric deposition was performed, before PDA at 500 ˚C for 60 s and reactive sputter deposition of TaN to form the gate electrode. After gate patterning, S/D regions were formed by implantation of Si^+ and P^+, and

followed by rapid thermal annealing (650 ˚C for 60 s in N_2 ambient) for dopant activation. Ti, followed by Pt, was then deposited to form the backside ohmic contact. Finally, PdGe contacts were integrated to from the S/D ohmic contacts.

2.3.2.2 Results and Discussion

Physical characterization using AFM was first performed to investigate the effect of vacuum anneal on the surface morphology of $In_{0.53}Ga_{0.47}As$. The RMS surface roughness of the $In_{0.53}Ga_{0.47}As$ surface before vacuum anneal was 0.10 nm [Fig. 2.33(a)]. Vacuum anneal at 520 °C for 60 s and 600 °C for 60 s increased the RMS surface roughness to 0.13 nm and 0.46 nm, respectively [Fig. 2.33(b) and (c)]. Severe deterioration of the surface roughness after vacuum anneal at 600 °C may reduce the carrier mobility of surface channel MOSFETs due to additional surface roughness scattering. The degradation of surface morphology is attributed to evaporation of highly volatile indium (In) atoms at temperatures higher than 560 °C, which leads to

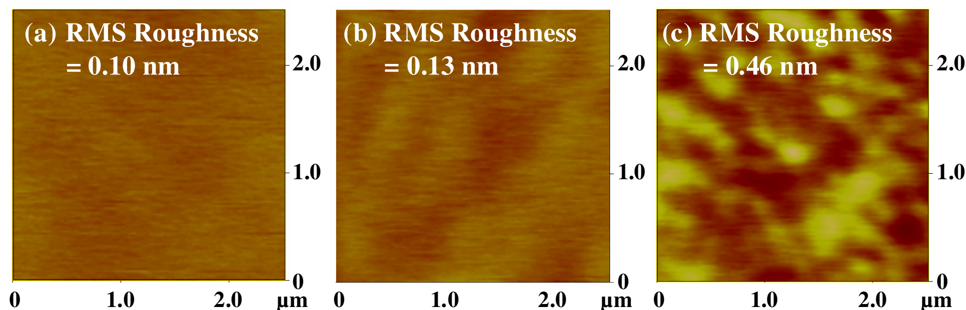


Fig. 2.33 AFM images of InGaAs surfaces (a) before vacuum annealing, and after vacuum anneal at (b) 520 °C for 60 s, and (c) 600 °C for 60 s. The AFM scan area is 2.5 µm by 2.5 µm. Severe degradation of surface roughness was observed after vacuum anneal at 600 °C for 60 s, and is attributed to the evaporation of indium.

a Ga-rich InGaAs surface [2.40]. As native oxide desorption is initiated at 510 °C [2.41], an annealing temperature of 520 °C was chosen for integration in a transistor fabrication flow to maintain good surface morphology as well as material composition of $In_{0.53}Ga_{0.47}As$.

TEM micrographs in Fig. 2.34 examine the MOS gate stacks formed on InGaAs (a) without vacuum anneal and SiH_4 + NH_3 passivation, and (b) with vacuum anneal (520 °C for 60 s) and SiH_4 + NH_3 passivation. Without additional vacuum anneal and passivation, a few monolayers of interfacial native oxide between HfAlO and InGaAs were observed [Fig. 2.34(a)]. This low quality native oxide is the root cause of Fermi level pinning and high D_{it}. For the SiH_4 + NH_3-passivated sample, an atomically flat InGaAs surface was seen without visible degradation [Fig. 2.34(b)]. High resolution TEM image in the inset of Fig. 2.34(b) confirms the presence of an interfacial layer with

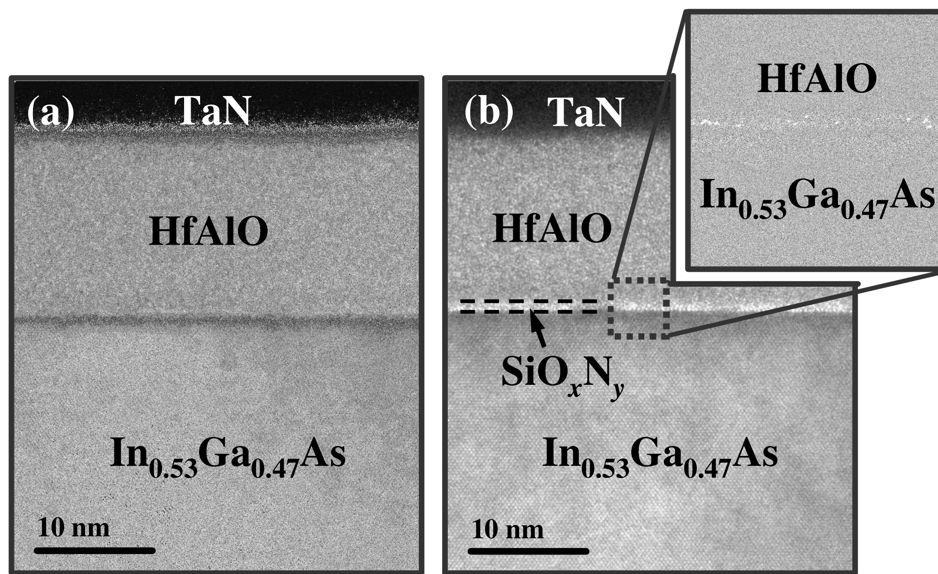


Fig. 2.34 Cross-sectional TEM images of the TaN/HfAlO/InGaAs stacks: (a) without and (b) with vacuum anneal and SiH_4 + NH_3 passivation. Inset reveals the existence of thin SiO_xN_y interfacial layer between HfAlO and InGaAs in the sample with vacuum anneal and SiH_4 + NH_3 passivation.

thickness of ~ 1 nm between HfAlO high-*k* dielectric and $In_{0.53}Ga_{0.47}As$.

The As 3*d* core level spectra in Fig. 2.35(a) reveal the As-O bond at 44.9 eV is present in the unpassivated control but is absent in the sample with SiH_4 + NH_3 passivation prior high-*k* dielectric deposition. In addition, SiH_4 + NH_3 passivation also leads to the suppression of In-O bond, as illustrated by In 3*d* core level spectra in Fig. 2.35(b). Examination of the Si 2*p* spectra in Fig. 2.35(c) reveals the SiO_xN_y interfacial layer.

Charge pumping analysis was conducted to evaluate the D_{it} of the HfAlO/InGaAs interface. The characterization was performed by sweeping the base level V_{base} of constant-amplitude trapezoidal gate pulse train from accumulation level to inversion level, while keeping the S/D terminals grounded. The amplitude V_a and frequency f of the gate pulses are 1 V and 200 kHz, respectively. The charge pumping current I_{CP} divided by f is plotted

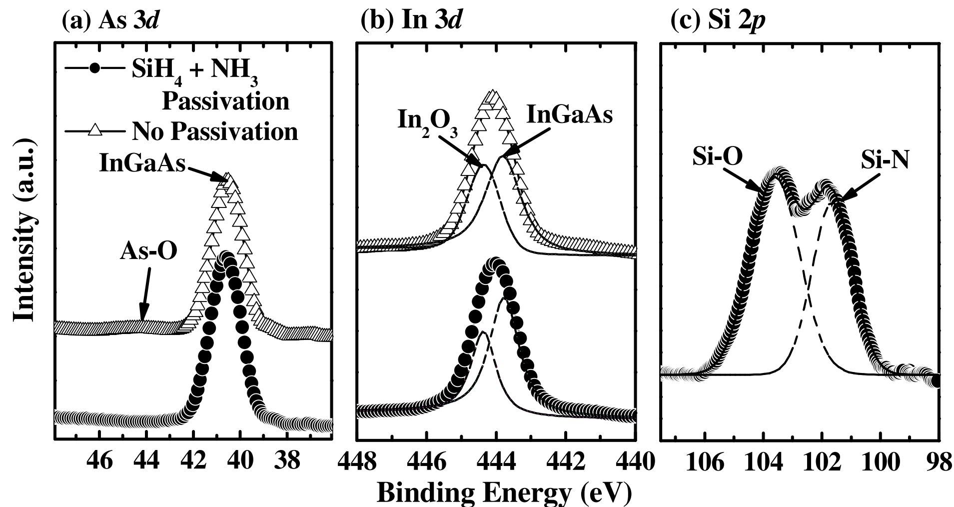


Fig. 2.35 (a) As 3*d* XPS spectra show the elimination of As-O bond after SiH_4 + NH_3 passivation. (b) With additional vacuum baking and SiH_4 + NH_3 passivation, In-O bond at the interface was suppressed, as illustrated by the deconvoluted components of the In 3*d* XPS spectra. (c) Si 2*p* spectrum of the SiH_4 + NH_3-passivated sample verifies the existence of Si-O and Si-N bonds, indicating the formation of a thin SiO_xN_y interfacial layer.

as a function of V_{base} for equal trapezoidal pulse rise time t_r and fall time t_f, *i.e.* $t_r = t_f$ (Fig. 2.36). Note that t_r and t_f are varied, taking values of 100, 200, 300, 400, 700, and 1000 ns. Devices with SiH_4 + NH_3 passivation have significantly lower I_{CP} than control devices, indicating a reduced number of interface states available for trapping and detrapping. I_{CP} for trapezoidal gate pulse waveform [2.42] is expressed as

$$I_{CP} = 2qD_{it} fA_G kT\left[ln\sqrt{t_r t_f} + ln\left(\frac{|V_{FB} - V_T|}{V_a} v_{th} n_s \sqrt{\sigma_n \sigma_p}\right)\right], \quad (2\text{-}5)$$

where T is temperature, A_G is transistor gate area, k is Boltzmann constant, V_{FB} is flatband voltage, v_{th} is the thermal velocity of the carriers, n_s is the surface concentration of minority carriers, σ_n and σ_p are capture cross sections of electrons and holes, respectively. Based on equation (2-5), the mean D_{it} over the energy range swept by the trapezoidal gate pulse with V_a of 1 V was extracted from the slope of I_{CP}/f versus $\ln[(t_r \cdot t_f)]$ (Fig. 2.37).

The mean D_{it} in the InGaAs N-MOSFETs with and without SiH_4 + NH_3 passivation were found to be 6.5×10^{11} cm^{-2}eV^{-1} and 4.2×10^{12} cm^{-2}eV^{-1}, respectively. Similar D_{it} level was also demonstrated in GaAs N-MOSFETs fabricated using the same passivation approach, as shown in Section 2.3.1. The significant reduction in D_{it} by introducing additional SiH_4 + NH_3 passivation is related to the suppression of interfacial native oxides and dangling bonds. First, Si-induced reduction of the III-V oxides occurs such that the oxygen previously bonded to III-V atoms is re-bonded with Si atoms to form SiO_x [2.43]. Second, SiN layer formed by SiH_4 + NH_3 treatment acts as barrier layer to protect the III-V surface from exposure to oxidizing ambient during subsequent MOCVD high-k dielectric deposition. It is also likely that

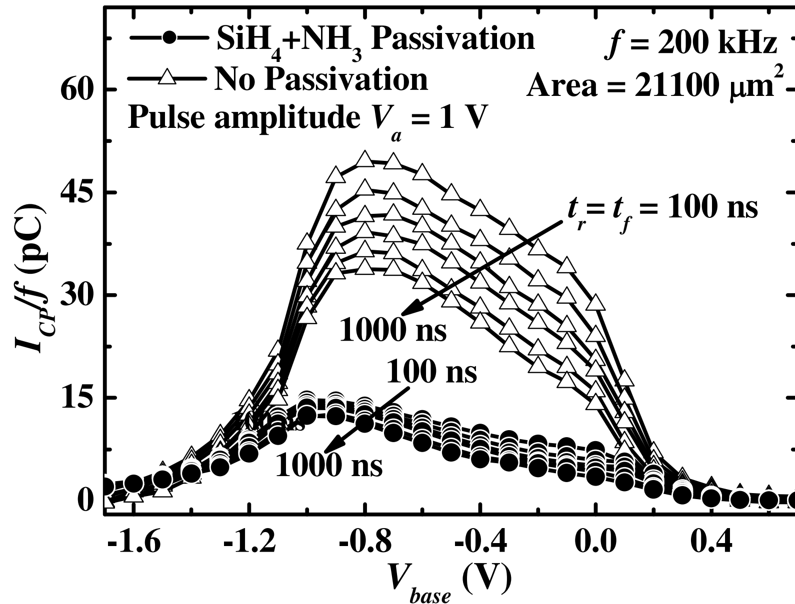


Fig. 2.36 I_{CP}/f versus V_{base} for $In_{0.53}Ga_{0.47}As$ N-MOSFETs with and without SiH_4 + NH_3 passivation for rise and fall time of gate pulses ranging from 100 ns to 1000 ns. Constant-amplitude trapezoidal gate pulse train was swept from accumulation to inversion level for interface characterization. Higher I_{CP} in the control devices indicates the presence of more interface states available for trapping-detrapping.

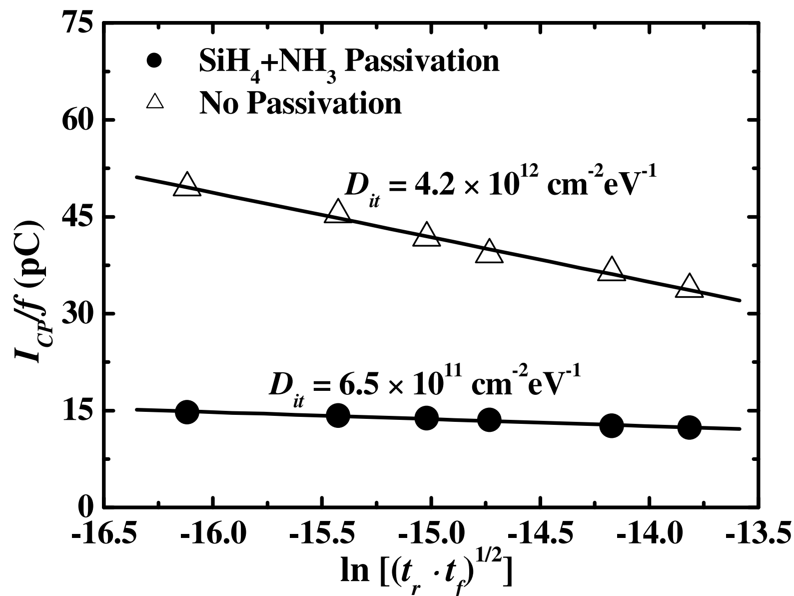


Fig. 2.37 A gentler slope in I_{CP}/f as a function of $\ln[(t_r{\cdot}t_f)]$ indicates a lower D_{it} level as seen from equation (2-5). The mean D_{it} of the $In_{0.53}Ga_{0.47}As$ N-MOSFETs with and without SiH_4 + NH_3 passivation were extracted to be 6.5×10^{11} cm^{-2}eV^{-1} and 4.2×10^{12} cm^{-2}eV^{-1}, respectively.

hydrogen dissociated from NH_3 and SiH_4 during the treatment further passivates dangling bonds on the InGaAs surface and thereby decreases D_{it}. Though good electrical characteristics were demonstrated by the InGaAs MOSFETs fabricated using gate-first transistor fabrication approach in this experiment, the SiH_4 + NH_3-passivated InGaAs MOSFETs are expected to achieve even better device performance such as lower D_{it} and steeper subthreshold if gate-last transistor fabrication scheme, *i.e.* without huge thermal budget for dopant activation, was adopted.

The impact of SiH_4 + NH_3 passivation on the electrical performance of InGaAs N-MOSFETs is further investigated. The SiH_4 + NH_3-passivated transistor shows improved subthreshold characteristics over the control transistor [Fig. 2.38(a)], and are related to D_{it} reduction due to the SiH_4 + NH_3 passivation process. Steeper SS gives rise to lower I_{off} and therefore higher I_{on}/I_{off} ratio. I_D-V_D output characteristics of the same pair of transistors are plotted in Fig. 2.38(b).

Fig. 2.39 plots the cumulative distribution of the SS of the InGaAs MOSFETs with and without SiH_4 + NH_3 passivation. SiH_4 + NH_3-passivated InGaAs N-MOSFETs have a median SS that is 300 mV/decade lower than that of control devices. Fig. 2.40 compares the I_{off} versus linear drain current I_{Dlin} characteristics of SiH_4 + NH_3-passivated MOSFETs and control transistors, showing I_{off} reduction by more than an order of magnitude at a fixed I_{Dlin} in the SiH_4 + NH_3-passivated devices. The performance enhancement is also illustrated in the I_{off} versus saturation drain current I_{Dsat} plot in Fig. 2.41.

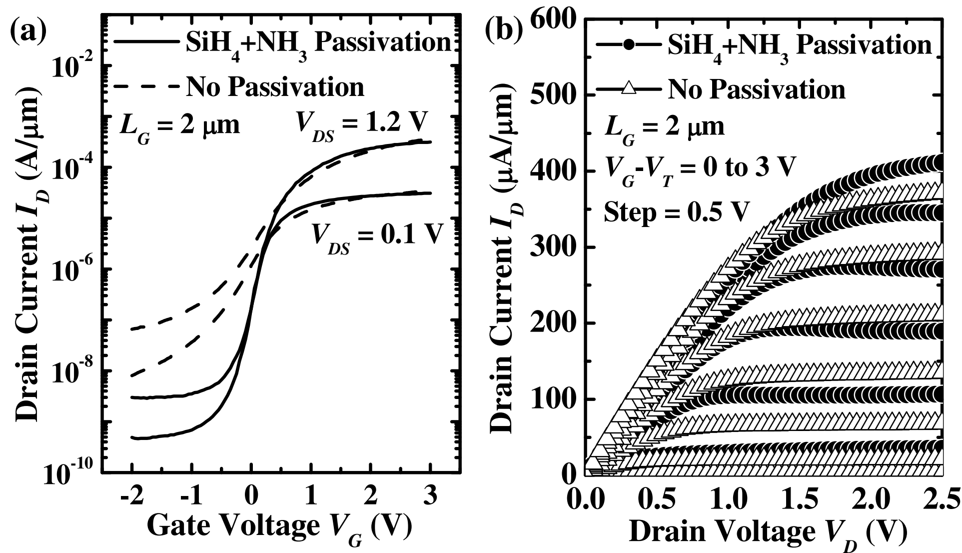


Fig. 2.38 (a) I_D–V_G curves reveal that SiH_4 + NH_3 passivation leads to significant improvement in the subthreshold characteristics of InGaAs N-MOSFETs. (b) I_D-V_D output characteristics of the same pair of transistors showing excellent saturation and pinch-off characteristics.

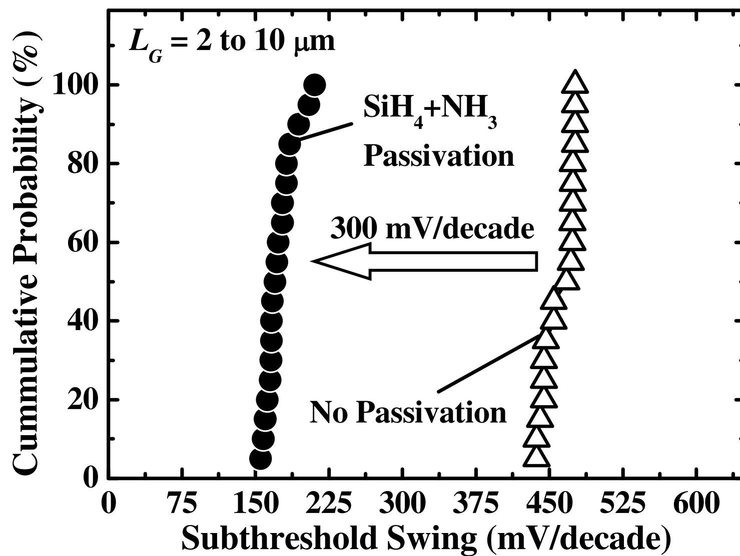


Fig. 2.39 Cumulative distribution of the SS of InGaAs N-MOSFETs with and without SiH_4 + NH_3 passivation. The SiH_4 + NH_3 passivation technology reduces SS by more than 300 mV/decade.

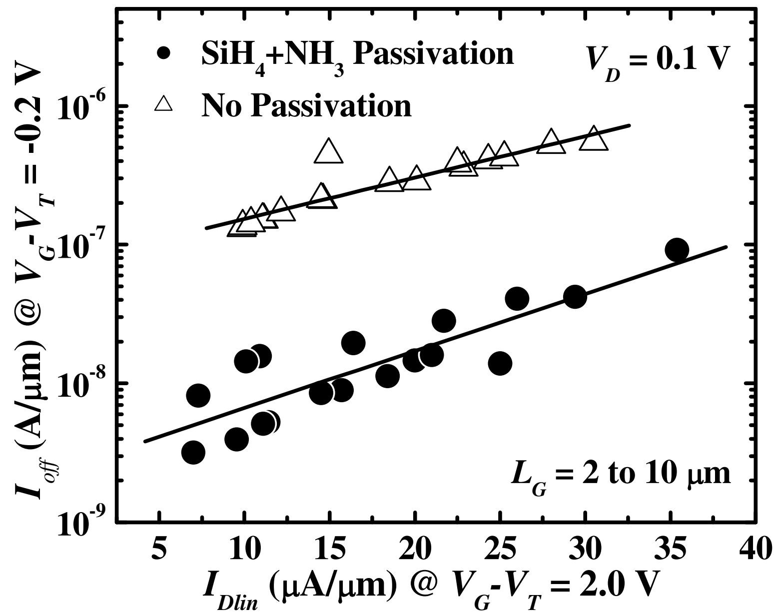


Fig. 2.40 Plot of I_{off} versus I_{Dlin} showing significant reduction in I_{off} for $In_{0.53}Ga_{0.47}As$ MOSFET with SiH_4 + NH_3 passivation. The reduction in I_{off} is attributed to the improvement in SS due to D_{it} reduction.

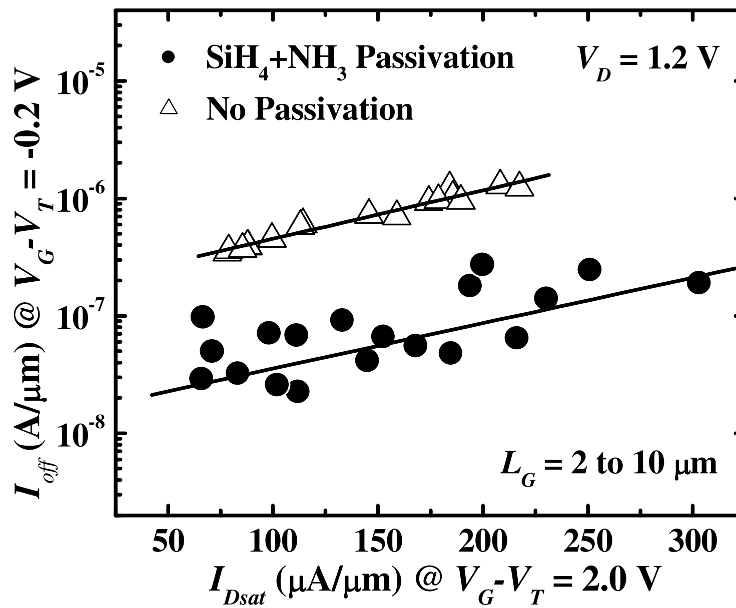


Fig. 2.41 I_{off} versus I_{Dsat} showing of InGaAs N-MOSFETs with and without SiH_4 + NH_3 passivation. Similar reduction in I_{off} was also achieved in $In_{0.53}Ga_{0.47}As$ MOSFET with SiH_4 + NH_3 passivation.

2.3.2.3 Summary

The effectiveness of SiH_4 + NH_3 passivation technology on $In_{0.53}Ga_{0.47}As$ N-MOSFETs has been demonstrated. The enhancement in interfacial properties is related to the desorption of native oxide during vacuum baking and the formation of a SiO_xN_y interfacial layer.

2.4 InGaAs N-MOSFETs with *In-situ* SiH_4 + NH_3 Passivation and Tetrafluoromethane (CF_4) Plasma Treatment

A high-*k* gate dielectric generally suffers from a high density of defects, which are mainly oxygen vacancies, contributing to charge trapping and mobility degradation [2.44]. Incorporation of F into high-*k* dielectric on Si and Ge was reported to improve MOSFET performance and reliability [2.45]-[2.48]. With a higher electronegativity than oxygen, F effectively passivates vacancies in ionic oxides by forming strong metal-F bonds [2.44] and interfacial defects by forming Si-F and Ge-F bonds [2.47]-[2.48]. F was also incorporated into ALD Al_2O_3 and ALD HfO_2 gate dielectrics of $In_{0.53}Ga_{0.47}As$ MOSFETs [2.49]-[2.50]. SiH_4 + NH_3 passivation of MOS stacks on GaAs and InGaAs using a multiple chamber MOCVD tool is demonstrated in Section 2.3. Significant improvement in the interfacial properties between HfAlO and III-V was achieved. Nevertheless, the effects of F on electrical characteristics of III-V MOSFETs with SiH_4 + NH_3 passivation have not been investigated.

In this section, multiple passivation methods comprising *in-situ* SiH_4 + NH_3 surface passivation and post-gate dielectric deposition treatment in CF_4 plasma were combined for further performance enhancement. Section 2.4.1

discusses the integration of CF_4 plasma treatment in the device fabrication process. Section 2.4.2 reports the results of physical and electrical characterization on the SiH_4+NH_3–passivated $In_{0.53}Ga_{0.47}As$ channel N-MOSFETs.

2.4.1 Experiment

P-type Zn-doped (100)-oriented InP wafers with N_A of 1×10^{18} cm^{-3} were used as starting substrates on which a 500 nm thick Be-doped $In_{0.53}Ga_{0.47}As$ layer with N_A of 1×10^{16} cm^{-3} was grown. A three step pre-gate cleaning process using HCl, NH_4OH, and $(NH_4)_2S$ solution was carried out before the wafers were loaded into a multiple-chamber MOCVD gate cluster system for vacuum anneal, SiH_4 + NH_3 treatment, and MOCVD HfAlO deposition. F was then introduced into the gate dielectric by CF_4 plasma treatment in an inductively coupled plasma (ICP) chamber using CF_4 + O_2 gas mixtures at a pressure of 100 mTorr and radio frequency power of 10 W for 1 minute. The flow rates of CF_4 and O_2 were 90 and 10 sccm, respectively. Oxygen was introduced to avoid possible deposition of carbon byproducts. This F treatment step was skipped for the control devices. PDA at 500 ˚C for 60 s in N_2 ambient was performed before reactive sputtering of TaN metal to form the gate electrode. After gate patterning, S/D regions were formed by Si^+ implant at dose of 1×10^{14} cm^{-2} and annealing at 600 °C in N_2 ambient. PdGe S/D ohmic contacts were integrated to complete the device fabrication.

2.4.2 Results and Discussion

HRTEM image of a F-treated HfAlO gate dielectric in an InGaAs

MOSFET is shown in Fig. 2.42(a). Fast Fourier transform diffractogram reveals good crystallinity of the $In_{0.53}Ga_{0.47}As$ epilayer [Fig. 2.42(b)]. Fig. 2.42(c) shows the F 1*s* XPS spectrum of HfAlO high-*k* dielectric after ICP CF_4 plasma treatment. The strong F peak at 686 eV confirms its incorporation in the dielectric. SIMS analysis [Fig. 2.43] was conducted to obtain the elemental distribution in the F-treated MOS gate stack before and after PDA. Considerable amount of F was found to pile up near the interface between high-*k* and InGaAs after PDA, where the charge trapping sites could be located.

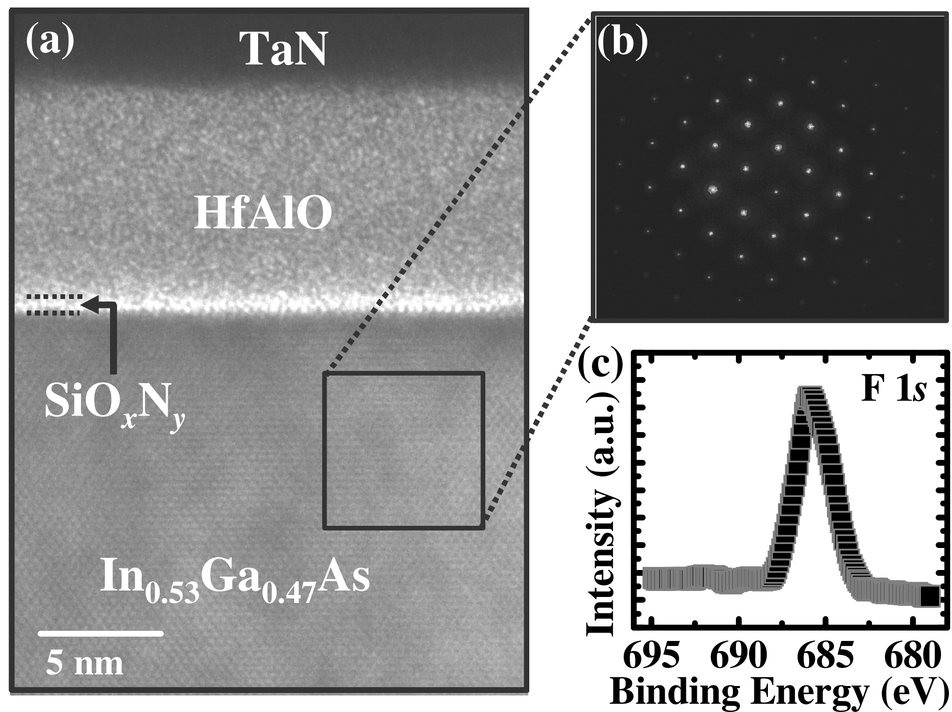


Fig. 2.42 (a) Cross-sectional TEM micrograph showing a F-treated MOCVD HfAlO gate dielectric formed on a SiH_4 + NH_3-passivated surface in a $In_{0.53}Ga_{0.47}As$ MOSFET. A thin SiO_xN_y interfacial layer between HfAlO and InGaAs was observed. (b) Diffractogram reveals excellent crystalline quality of the $In_{0.53}Ga_{0.47}As$ epilayer. (c) Strong peak in the F 1*s* spectrum reveals the incorporation of fluorine in the HfAlO film after ICP CF_4 plasma treatment. This peak is absent in the control sample.

Fig. 2.44(a) plots the I_D–V_G transfer characteristics of InGaAs N-MOSFETs with and without F treatment. The gate length is 2 µm. F treatment improves the subthreshold characteristics and I_{Dsat}. The SS of a F-treated InGaAs MOSFET was improved from 170 mV/decade to 156 mV/decade, indicating improvement in gate stack quality. Fig. 2.44(b) shows the I_D–V_D output characteristics of the InGaAs MOSFETs. Higher I_{Dsat} was achieved in the F-treated InGaAs MOSFET. This is likely attributed to the improved carrier mobility (to be shown later), resulting from the reduction in interface and oxide trapped charges.

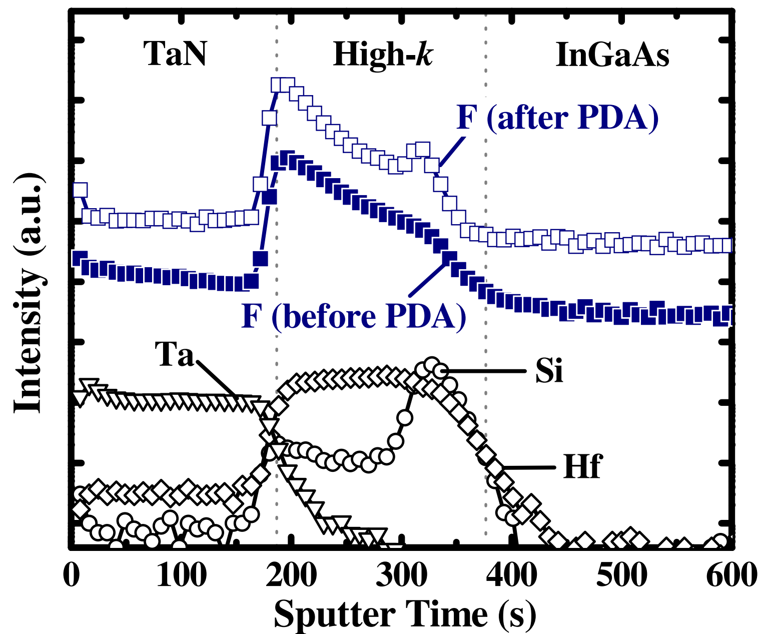


Fig. 2.43 SIMS profile reveals the elemental distribution of the TaN/HfAlO/InGaAs stack with SiH_4 + NH_3 passivation and F treatment. F tends to pile up at the HfAlO/SiO_xN_y interface after PDA.

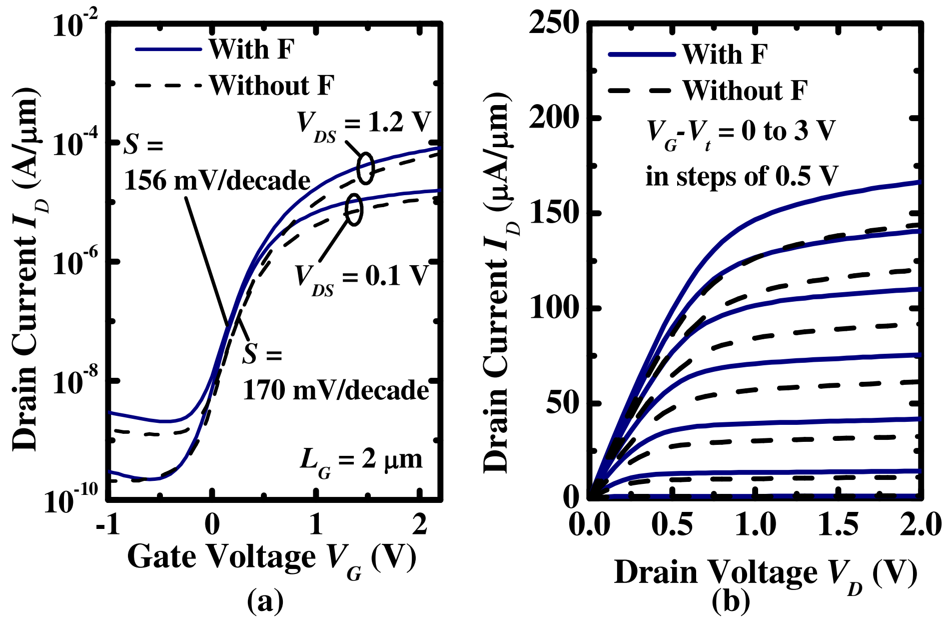


Fig. 2.44 (a) I_D–V_G and (b) I_D–V_D output characteristics of $In_{0.53}Ga_{0.47}As$ N-MOSFETs with and without F treatment. The F-passivated transistor demonstrates improvement in subthreshold characteristics and drive current.

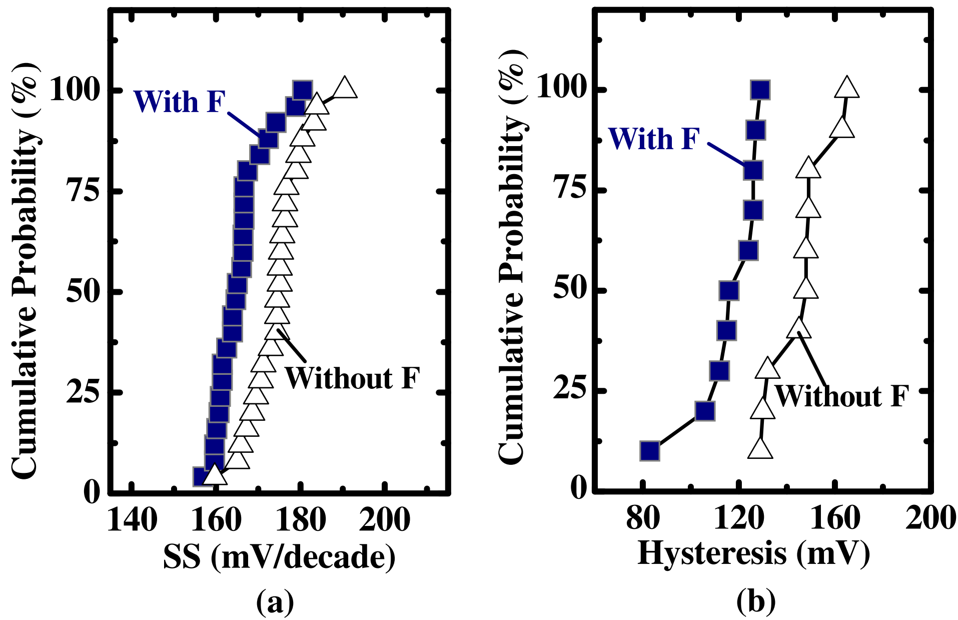


Fig. 2.45 Cumulative distribution of (a) SS, and (b) hysteresis of InGaAs N-MOSFETs with and without ICP CF_4 plasma treatment. Fluorine passivation leads to smaller SS, indicating reduced interface states in the MOS stack, and improved hysteresis, indicating the reduced number of bulk oxide traps.

Fig. 2.45(a) and (b) summarize the statistical distributions of SS and hysteresis in the *C*-*V* characteristics of InGaAs MOSFETs with and without F treatment. InGaAs MOSFETs with F-treated gate dielectric have a median SS that is lower than that of the controls. The improvement of SS indicates a reduction of interfacial states by F passivation. Reduction in hysteresis was also achieved with the incorporation of F, indicating a reduction in the number of oxide traps. The chemical bonding in Hf-rich HfAlO is ionic, which is different from covalent network structure in SiO_2. Oxygen vacancy states are highly localized on the orbitals of the Hf ions [2.44]. With shorter bond length than other halides such as Cl and Br, F would be more effective at repelling anti-bonding states into the oxide [2.44]. In addition, F is easily to be incorporated into the HfAlO film with smaller atomic radius than other halides. Additional F treatment is also likely to passivate the vacancy states in the SiO_xN_y by forming Si-F bonds. As a result, total oxide trapping states in the gate stack was reduced through F incorporation.

Fig. 2.46 plots the extracted μ_{eff} versus inversion charge density N_{inv} of InGaAs MOSFETs with and without F passivation. The effective electron mobility is extracted based on split *C*-*V* method. Both InGaAs transistors have comparable EOT of 3.2 nm. The F treatment improved the electron mobility μ_e in the high field or high inversion charge density N_{inv} region. Higher mobility contributes to a higher drive current, as observed in Fig. 2.44(a) and (b). The improvement of carrier mobility is attributed to improved gate dielectric quality, which gives a reduced density of trapped charges that contributes to carrier scattering. With improved subthreshold characteristiscs,

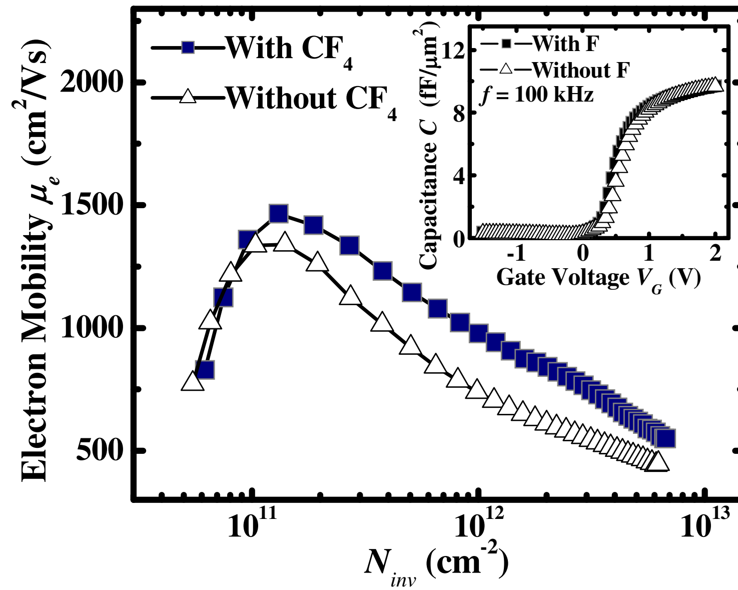


Fig. 2.46 Electron mobility μ_e as a function of inversion charge density N_{inv}. Improvement of carrier mobility at high field could be attributed to reduced number of interface traps. Inversion C-V characteristics indicate that the InGaAs MOSFETs have identical EOT of 3.2 nm.

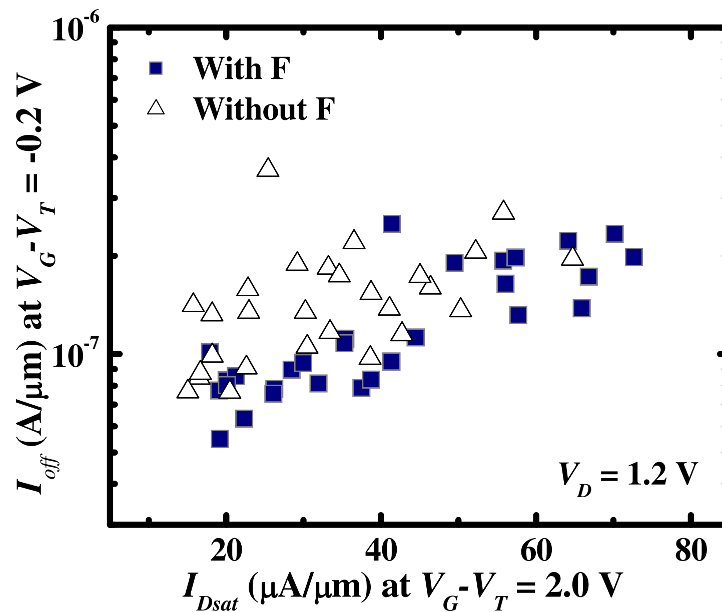


Fig. 2.47 Plot of off-state leakage I_{off} versus on-state saturation drain current I_{Dsat} showing significant reduction in I_{off} for $In_{0.53}Ga_{0.47}As$ MOSFET with additional F passivation. The reduction in I_{off} is attributed to the improvement in subthreshold swing due to improved gate stack quality.

the InGaAs MOSFETs with additional F incorporation show significant I_{off} reduction at a fixed I_{Dsat} [Fig. 2.47].

2.4.3 Summary

In summary, the effects of F treatment on MOCVD HfAlO gate dielectric in N-MOSFETs with a SiH_4 + NH_3-passivated $In_{0.53}Ga_{0.47}As$ surface channel were investigated. XPS and SIMS analysis confirmed the incorporation of F into the gate dielectric. F incorporation into the gate dielectric was found to improve the subthreshold characteristics and hysteresis of $In_{0.53}Ga_{0.47}As$ MOSFETs by reducing both interface and oxide trapped charges. The F-passivated $In_{0.53}Ga_{0.47}As$ MOSFETs also demonstrate improved drive current and carrier mobility.

2.5 Summary

In-situ interface engineering, comprising vacuum anneal for native oxide desorption and surface treatment, has been successfully demonstrated to realize high quality metal gate/high-*k* dielectric stack on III-V compound semiconductors. After vacuum anneal for the elimination of poor quality native oxide, a thin silicon interfacial layer was formed by SiH_4 treatment to effectively prevent the III-V's surface from exposure to an oxidizing ambient during MOCVD high-*k* dielectric deposition. Using this passivation, surface channel III-V N-MOSFETs were demonstrated.

MOSFET performance can be improved by introducing additional NH_3 in a SiH_4 passivation. The enhancement in interfacial properties is related to the formation of a SiO_xN_y interfacial layer that protects the GaAs or InGaAs surface from exposure to the oxidizing ambient during high-*k* dielectric

deposition. Inversion-type GaAs and InGaAs channel N-MOSFETs were fabricated with the SiH_4 and NH_3 passivation technology, showing good electrical characteristics with high electron mobility, high I_{on}/I_{off} ratio and low subthreshold swing.

The impact of combining multiple interfacial passivation methods such as *in-situ* SiH_4 + NH_3 passivation and CF_4 plasma treatment was investigated. Incorporation of F into the HfAlO high-*k* dielectric was found to improve the subthreshold characteristics and hysteresis of InGaAs MOSFETs due to the reduction in interface and oxide trapped charges. In addition, further improvement in drive current and carrier mobility was also achieved in the F-passivated InGaAs MOSFETs.

2.6 References

[2.1] G. G. Fountain, R. A. Rudder, S. V. Hattangady, R. J. Markunas, and J. A. Hutchby, "Demonstration of an N-channel inversion mode GaAs MISFET," in *IEDM Tech. Dig.*, 1989, pp. 887–889.

[2.2] M. Passlack, M. Hong, J. P. Mannaerts, S. N. G. Chu, R. L. Opila, and N. Moriya, "*In-situ* Ga_2O_3 process for GaAs inversion/accumulation device and surface passivation applications," in *IEDM Tech. Dig.*, 1995, pp. 383–386.

[2.3] F. Hasegawa, M. Onomura, C. Mogi, and Y. Nannichi, "Reduction of Schottky barrier heights by surface oxidation of GaAs and its influence on DLTS signals for the midgap level EL2," *Solid State Electron.*, vol. 31, no. 2, pp. 223–228, 1988.

[2.4] W. E. Spicer, Z. Liliental-Weber, E. Weber, N. Newman, T. Kendelewicz, R. Cao, C. McCants, P. Mahowald, K. Miyano, and I. Lindau, “The advanced unified defect model for Schottky barrier formation,” *J. Vac. Sci. Technol. B*, vol. 6, no. 4, pp. 1245–1251, 1988.

[2.5] F. Sankey, R. E. Allen, S.-F. Ren, and J. D. Dow, “Dangling bonds and Schottky barriers,” *J. Vac. Sci. Technol. B*, vol. 3, no. 4, pp. 1162–1166, 1985.

[2.6] M. Hong, J. Kwo, A. R. Mannaerts, and A. M. Sergent, “Epitaxial cubic gadolinium oxide as a dielectric for gallium arsenide passivation,” *Science*, vol. 283, no. 5409, pp. 1897–1900, 1999.

[2.7] J. Kwo, D. W. Murphy, M. Hong, R. L. Opila, J. P. Mannaerts, A. M. Sergent, and R. L. Masaitis, “Passivation of GaAs using $(Ga_2O_3)_{1-x}(Gd_2O_3)_x$, $0 \leq x \leq 1.0$ films,” *Appl. Phys. Lett.*, vol. 75, no. 8, pp. 1116–1118, 1999.

[2.8] K. Rajagopalan, R. Droopad, J. Abrokwah, P. Zurcher, P. Fejes, and M. Passlack, “1-µm enhancement mode GaAs N-channel MOSFETs with transconductance exceeding 250 mS/mm,” *IEEE Electron Device Lett.*, vol. 28, no. 2, pp. 100–102, 2007.

[2.9] Y. Xuan, T. Shen, M. Xu, Y.Q. Wu, and P. D. Ye, “High-performance surface channel In-rich $In_{0.75}Ga_{0.25}As$ MOSFETs with ALD high-*k* as gate dielectric,” in *IEDM Tech. Dig.*, 2008, pp. 371–374.

[2.10] D. Lin, G. Brammertz, S. Sioncke, C. Fleischmann, A. Delabie, K. Martens, H. Bender, T. Conard, W. H. Tseng, J. C. Lin, W. E. Wang, K. Temst, A, Vatomme, J. Mitard, M. Caymax, M. Meuris, M. Heyns, and

T. Hoffmann, "Enabling the high-performance InGaAs/Ge CMOS: a common gate stack solution," in *IEDM Tech. Dig.*, 2009, pp. 327–330.

[2.11] Y. Q. Wu, M. Xu, R.S. Wang, O. Koybasi, and P. D. Ye, "High performance deep-submicron inversion-mode InGaAs MOSFETs with maximum G_m exceeding 1.1 mS/μm: New HBr pretreatment and channel engineering," in *IEDM Tech. Dig.*, 2009, pp. 323–326.

[2.12] M. M. Frank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Muller, "HfO_2 and Al_2O_3 gate dielectrics on GaAs grown by atomic layer deposition," *Appl. Phys. Lett.*, vol. 86, no. 15, pp. 152904–152906, 2005.

[2.13] N. Goel, D. Heh, S. Koveshnikov, I. Ok, S. Oktyabrsky, V. Tokranov, R. Kambhampatic, M. Yakimov, Y. Sun, P. Pianetta, C.K. Gaspe, M.B. Santos, J. Lee, S. Datta, P. Majhi, and W. Tsai, "Addressing the gate stack challenge for high mobility $In_xGa_{1-x}As$ channels for NFETs," in *IEDM Tech. Dig.*, 2008, pp. 363–366.

[2.14] J. Huang, N. Goel, H. Zhao, C. Y. Kang, K.S. Min, G. Bersuker, S. Oktyabrsky, C.K. Gaspe, M.B. Santos, P. Majhi, P. D. Kirsch, H.-H. Tseng, J.C. Lee, and R. Jammy, "InGaAs MOSFET performance and reliability improvement by simultaneous reduction of oxide and interface charge in ALD (La)AlO_x/ZrO_2 gate stack," in *IEDM Tech. Dig.*, 2009, pp. 335–338.

[2.15] W. P. Li, X. W. Wang, Y. X. Liu, S. I. Shim, and T. P. Ma, "Demonstration of unpinned GaAs surface and surface inversion with gate dielectric made of Si_3N_4," *Appl. Phys. Lett.*, vol. 90, no. 19, p. 193503, 2007.

[2.16] Y. Cao, X. Li, J. Zhang, P. Fay, T. H. Kosel, and D. C. Hall, "Microwave performance of GaAs MOSFET with wet thermally oxidized InAlP Gate Dielectric," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 317–319, 2006.

[2.17] M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and R. Chau, "Advanced high-*k* gate dielectric for high-performance short-channel $In_{0.7}Ga_{0.3}As$ quantum well field effect transistors on silicon substrate for low power logic applications," in *IEDM Tech. Dig.*, 2009, pp. 319–322.

[2.18] I. Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, L. Yu, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and J. C. Lee, "Self-aligned n- and p-channel GaAs MOSFETs on undoped and p-type substrates using HfO_2 and silicon interface passivation layer," in *IEDM Tech. Dig.*, 2006, pp. 829–832.

[2.19] H.-C. Chin, M. Zhu, C.-H. Tung, G. S. Samudra, and Y.-C. Yeo, "*In situ* surface passivation and CMOS-compatible palladium-germanium contacts for surface-channel gallium arsenide MOSFETs," *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 553–556, 2008.

[2.20] M. Zhu, C.-H. Tung, and Y.-C. Yeo, "Aluminum oxynitride interfacial passivation layer for high-permittivity gate dielectric stack on gallium arsenide," *Appl. Phys. Lett.*, vol. 89, no. 20, p. 202 903, 2006.

[2.21] J. Lin, S. Lee, H.-J. Oh, W. Yang, G. Q. Lo, D. L. Kwong, and D. Z. Chi, "Plasma PH_3-passivated high mobility inversion InGaAs

MOSFET fabricated with self-aligned gate-first process and HfO_2/TaN gate stack," in *IEDM Tech. Dig.*, 2008, pp. 401–404.

[2.22] H. J. Oh, J. Q. Lin, S. A. B. Suleiman, G. Q. Lo, D. L. Kwong, D. Z. Chi, and S. J. Lee, "Thermally robust phosphorous nitride interface passivation for InGaAs self-aligned gate-first N-MOSFET integrated with high-*k* dielectric," in *IEDM Tech. Dig.*, 2009, pp. 339–342.

[2.23] F. Hyuga, H. Yamazaki, K. Watanabe, and J. Osaka, "Activation efficiency improvement in Si-implanted GaAs by P co-implantation," *Appl. Phys. Lett.*, vol. 50, no. 22, pp. 1592–1594, 1987.

[2.24] R. A. Morrow, "Electrical activation of silicon coimplanted with nitrogen, phosphorus, or arsenic in semi-insulating GaAs substrates grown by the liquid encapsulated Czochralski method," *J. Appl. Phys.*, vol. 64, no. 4, pp. 1889–1896, 1988.

[2.25] Y. Asaoka, "Desorption process of GaAs surface native oxide controlled by direct Ga-beam irradiation," *J. Cryst.Growth.*, vol. 251, no. 1–4, pp. 40–45, 2003.

[2.26] M.-G. Kang, S.-H. Sa, H.-H. Park, K.-S. Suh, and K.-H. Oh, "The characterization of etched GaAs surface with HCl or H_3PO_4 solutions," *Thin Solid Films*, vol. 308/309, pp. 634–642, 1997.

[2.27] M.-G. Kang, and H.-H. Park, "Surface preparation and effective contact formation for GaAs surface," *Vacuum*, vol. 67, no. 1, pp. 91–100, 2002.

[2.28] J. F. Fan, H. Oigawa, and Y. Nannichi, "The effect of $(NH_4)_2S$ treatment on the interface characteristics of GaAs MIS structures," *Jpn. J. Appl. Phys.*, vol. 27, pp. L1331–L1333, 1988.

[2.29] N. Wu, Q. Zhang, C. Zhu, D. S. H. Chan, M. F. Li, N. Balasubramanian, A. Chin, and D.-L. Kwong, “Alternative surface passivation on germanium for metal-oxide-semiconductor applications with high-*k* gate dielectric,” *Appl. Phys. Lett.*, vol. 85, no. 18, pp. 4127–4129, 2004.

[2.30] M. S. Joo, B. J. Cho, C. C. Yeo, D. S. H. Chan, S. J. Whang, S. Mathew, L. K.Bera, N. Balasubramanian, and D.-L. Kwong, “Formation of Hafnium–Aluminum–Oxide gate dielectric using single cocktail liquid source in MOCVD Process,” *IEEE Trans. Electron Devices*, vol. 50, no. 10, pp. 2088–2094, 2003.

[2.31] G. K. Dalapati, Y. Tong, W.-Y. Loh, H. K. Mun, and B. J. Cho, “Electrical and interfacial characterization of atomic layer deposited high-*k* gate dielectrics on GaAs for advanced CMOS devices,” *IEEE Trans. Electron Devices*, vol. 54, no. 8, pp. 1831–1837, 2007.

[2.32] T. W. Hickmott, “Annealing of surface states in polycrystalline silicon–gate capacitors,” *J. Appl. Phys.*, vol. 48, no. 2, pp. 723–733, 1977.

[2.33] W. A. Hill, and C. C. Coleman, “A single-frequency approximation for interface-state density determination,” *Solid State Electron.*, vol. 23, no. 9, pp. 987–993, 1980.

[2.34] E. D. Marshall, W. X. Chen, C. S. Wu, S. S. Lau, and T. F. Kuech, “Non-alloyed ohmic contact to n-GaAs by solid-phase epitaxy,” *Appl. Phys. Lett.*, vol. 47, no. 3, pp. 298–300, 1985.

[2.35] D. A. Ahmari, M. L. Hattendorf, D. F. Lemmerhirt, Q. Yang, Q. J. Hartmann, J. E. Baker, and G. E. Stillman, “Effects of alloy ambient on

PdGe contacts to n-type GaAs," *Appl. Phys. Lett.*, vol. 72, no. 26, pp. 3479–3481, 1998.

[2.36] D. K. Schroder, in *Semiconductor Material and Device Characterization*, p. 146, John Wiley & Sons, New Jersey, 2006.

[2.37] H.-L. Lu, M. Xu, S.-L. Ding, W. Chen, D. W. Zhang, and L. K. Wang, "Quantum chemical study of the initial surface reactions of HfO_2 atomic layer deposition on the hydroxylated GaAs (001)-4×2 surface," *Appl. Phys. Lett.*, vol. 89, no. 16, p. 162905, 2006.

[2.38] C. O. Chui, S. Ramanathan, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "Germanium MOS Capacitors Incorporating Ultrathin High-*k* Gate Dielectric," *IEEE Electron Device Lett.*, vol. 23, no. 8, pp. 473–475, 2002.

[2.39] W. Zhu, J.-P. Han, and T. P. Ma, "Mobility measurement and degradation mechanisms of MOSFETs made with ultrathin high-*k* dielectrics," *IEEE Trans. Electron Devices*, vol. 51, no. 1, pp. 98–105, 2004.

[2.40] T. Suzuki, and T. Nishinaga, "Surface diffusion and atom incorporation kinetics in MBE of InGaAs and AlGaAs," *J. Cryst. Growth*, vol. 111, no. 1–4, pp. 173–177, 1991.

[2.41] J. Osaka, K. Maezawa, H. Yokohama, and M. Yamamoto, "Highly uniform regrown $In_{0.53}Ga_{0.47}As$/AlAs/InAs resonant tunneling diodes on $In_{0.53}Ga_{0.47}As$," *Jpn. J. Appl. Phys.*, vol. 38, no. 2B, pp. 1204–1207, 1999.

[2.42] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. D. Keersmaecker, "A reliable approach to charge-pumping measurements in MOS

transistors," *IEEE Trans. Electron Devices*, vol. 31, vol. ED-31, pp. 42–53, 1984.

[2.43] I. Jimenez, F. J. Palomares, and J. L. Sacedon, "SiO_2 growth on GaAs by reduction of GaAs oxides: Separation of stoichiometric changes from SiO_2/GaAs band-lineup effects," *Phys. Rev. B*, vol. 49, no. 16, pp. 11117–11126, 1994.

[2.44] K. Tse, and J. Robertson, "Defect passivation in HfO_2 gate oxide by fluorine," *Appl. Phys. Lett.*, vol. 89, no. 14, p. 142914, 2006.

[2.45] H.-H. Tseng, P. J. Tobin, E. A. Hebert, S. Kalpat, M. E. Ramon, L. Fonseca, Z. X. Jiang, J. K. Schaeffer, R. I. Hedge, D. H. Triyso, C. C. Capasso, O. Adetutu, D. Sing, J. Conner, E. Luckowski, B.W. Chan, A. Haggag, S. Backer, R. Noble, M. Jahanbani, Y. H. Chiu, and B. E. White, "Defect passivation with fluorine in a Ta_xC_y/high-*k* gate stack for enhanced device threshold voltage stability and performance," in *IEDM Tech. Dig.*, 2005, pp. 696–699.

[2.46] M. Inoue, S. Tsujikawa, M. Mizutani, K. Nomura, T. Hayashi, K. Shiga, J. Yugami, J. Tsuchimoto, Y. Ohno, and M. Yoneda, "Fluorine incorporation into HfSiON dielectric for V_T control and its impact on reliability for poly-Si gate pFET," in *IEDM Tech. Dig.*, 2005, pp. 413–416.

[2.47] K.-I. Seo, R. Sreeenivasan, P. C.McIntyre, and K. C. Saraswat, "Improvement in high-*k* (HfO_2/SiO_2) reliability by incorporation of fluorine," in *IEDM Tech. Dig.*, 2005, pp. 417–420.

[2.48] R. Xie, M. Yu, M. Y. Lai, L. Chan, and C. Zhu, “High-*k* gate stack on germanium substrate with fluorine incorporation,” *Appl. Phys. Lett.*, vol. 92, no. 16, p. 163505, 2008.

[2.49] Y.-T. Chen, H. Zhao, J. H. Yum, Y. Wang, F. Xue, F. Zhou, and J. C. Lee, “Improved electrical characteristics of $TaN/Al_2O_3/In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistors by fluorine incorporation,” *Appl. Phys. Lett.*, vol. 95, no. 1, p. 013501, 2009.

[2.50] Y.-T. Chen, H. Zhao, Y. Wang, F. Xue, F. Zhou, and J. C. Lee, “Fluorinated HfO_2 gate dielectric engineering on $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect-transistors,” *Appl. Phys. Lett.*, vol. 96, no. 10, p. 103506, 2010.

Chapter 3

Lattice Mismatched $In_{0.4}Ga_{0.6}As$ Source/Drain Stressors with *In-situ* Doping for Strained $In_{0.53}Ga_{0.47}As$ Channel N-MOSFETs

3.1 Introduction

In Si CMOS technology, channel strain engineering has been widely adopted to extend the performance and scaling limits of Si MOSFETs [3.1]-[3.13]. Carrier mobility can be considerably enhanced through strain-induced modification of the electronic band structure [3.14]. In addition to the channel resistance R_{CH}, the magnitude of a transistor drive current is also determined by the source/drain (S/D) series resistance R_{SD} (Fig. 3.1). The combination of these two resistance components constitute to the total resistance R_{Total} between the source and drain contacts of a transistor, which is given by

$$R_{Total} = R_{Ch} + R_{SD}. \quad (3\text{-}1)$$

With the introduction of high mobility III-V channel materials and additional channel strain engineering, R_{Ch} is anticipated to be reduced dramatically. R_{SD} has also to be reduced such that the transistor drive current can be maximized

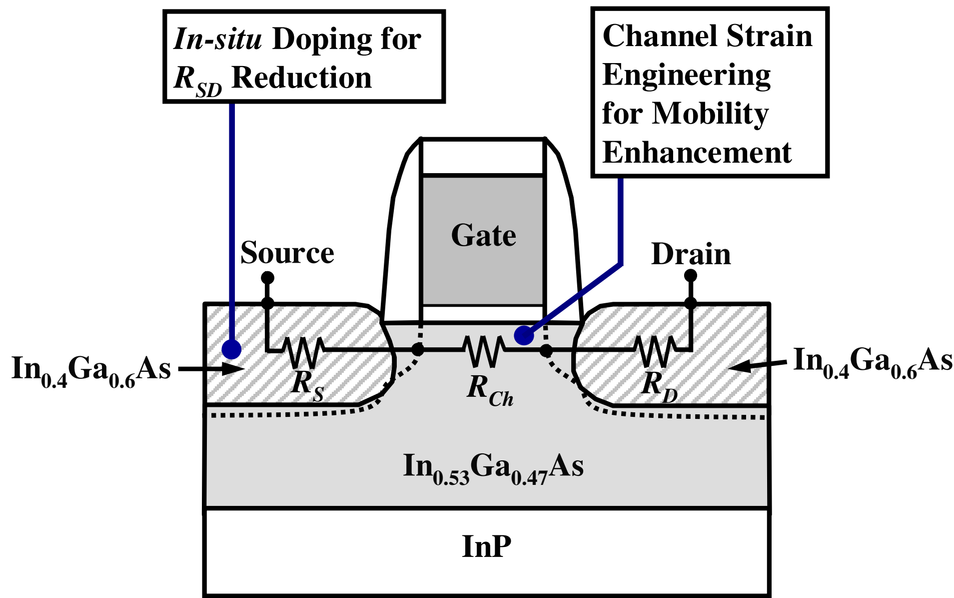


Fig. 3.1 Schematic illustration of the channel resistance (R_{Ch}) and the source/drain resistance (R_{SD}) of a transistor. The total resistance (R_{Total}) of the transistor is the summation of these resistance components. R_{Total} of the transistor is drastically reduced by high mobility InGaAs channel and additional channel strain engineering for R_{Ch} reduction and *in-situ* doping in the S/D regions for R_{SD} reduction.

with minimum R_{Total}.

To realize the full potential of III-V MOSFETs, channel strain engineering will be an important direction. The effect of strain on carrier transport in many III-V semiconductors, such as Gallium Arsenide (GaAs) and Indium Gallium Arsenide (InGaAs), is well-established [1.62]-[3.16]. However, the integration of process-induced strain to exploit the effect of local stressors such as lattice-mismatched S/D regions [3.12] for mobility enhancement in III-V channel MOSFETs has never been demonstrated. Furthermore, R_{SD} in III-V MOSFETs needs to be reduced to realize more performance benefits from the enhanced carrier transport. The incorporation of a high doping concentration in the S/D regions would also be important.

In this chapter, the concept and demonstration of a novel $In_{0.53}Ga_{0.47}As$

N-channel MOSFET with *in-situ* doped lattice-mismatched $In_{0.4}Ga_{0.6}As$ S/D regions for channel strain and S/D doping engineering are proposed and demonstrated (Fig. 3.1). The device concept and process development for this novel strained InGaAs MOSFET are described in Section 3.2. The lattice mismatch between $In_{0.4}Ga_{0.6}As$ S/D and $In_{0.53}Ga_{0.47}As$ channel is exploited to induce tensile strain in the channel for mobility enhancement. In addition, high S/D doping concentration, achieved by the *in-situ* doping process, further reduces R_{SD}. The key results in this technology demonstration are discussed in Section 3.3, followed by a conclusion in Section 3.4.

3.2 Device Concepts and Fabrication

3.2.1 Channel Strain Engineering By Lattice-Mismatched Source/Drain Stressors

By embedding a material in the S/D regions of a device structure that is lattice-mismatched with respect to the channel, beneficial strain can be locally introduced in the channel region. In Si CMOS technology, materials such as silicon-germanium (SiGe) and silicon-carbon (Si:C), which have lattice constants larger and smaller than that of Si, are employed to induce appropriate strain components in the transistor channel of P-MOSFETs [3.4]-[3.7] and N-MOSFETs [3.8]-[3.13], respectively.

Channel strain engineering can be introduced in III-V transistor by a similar approach. Fig. 3.2 illustrates the difference in the lattice constant of GaAs, $In_xGa_{1-x}As$, and InAs. InAs has a much larger lattice constant than GaAs. $In_xGa_{1-x}As$ alloy has an equilibrium lattice constant that is between the lattice constants of GaAs and InAs according to the Vegard's law,

$$a_{InGaAs} = (1-x)\, a_{GaAs} + x.a_{InAs} \quad (3\text{-}2)$$

where a_{GaAs} and a_{InAs} are the lattice constants of GaAs and InAs, respectively, and x is the mole fraction of In in the group III sublattice.

Schematic in Fig. 3.3 illustrates the origin of strain induced in an $In_{0.53}Ga_{0.47}As$ channel transistor featuring $In_{0.4}Ga_{0.6}As$ S/D stressors. The lattice interactions at the heterojunction between a pair of lattice-mismatched materials affect two major strain components: the vertical strain ε_y and the lateral strain ε_x. At the vertical heterojunction, the smaller $In_{0.4}Ga_{0.6}As$ lattice attempts to compress the larger $In_{0.53}Ga_{0.47}As$ lattice vertically, while itself takes on a vertical tensile strain. As a result, the $In_{0.53}Ga_{0.47}As$ lattice experiences vertical compressive strain which concomitantly contributes to a lateral tensile strain that extends throughout the channel region. However, at the horizontal heterojunction, the $In_{0.53}Ga_{0.47}As$ lattice experiences opposite lateral and vertical strains, which offsets against the strain components induced at the vertical heterojunction. Maximum strain level can then be found near the surface, where the carriers are conducted.

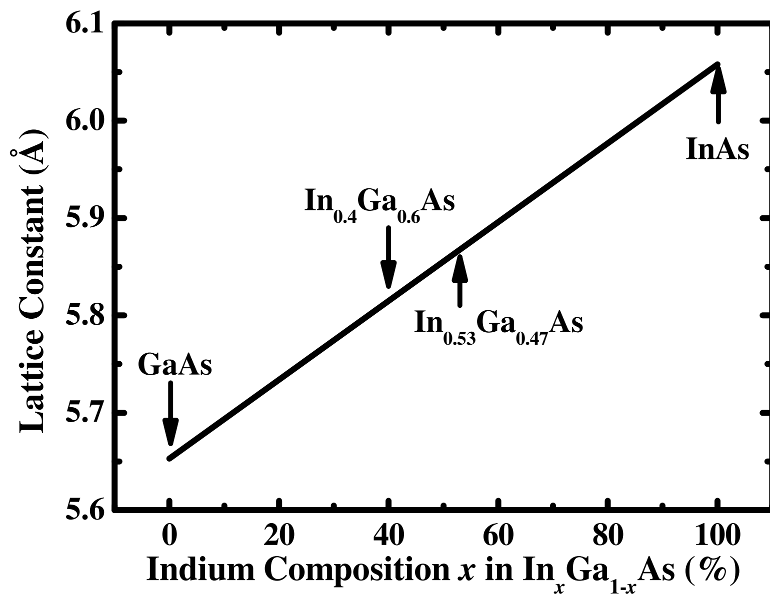


Fig. 3.2 Lattice constants of GaAs, $In_xGa_{1-x}As$, and InAs. The lattice constant of $In_xGa_{1-x}As$ can be tuned by varying the composition of indium.

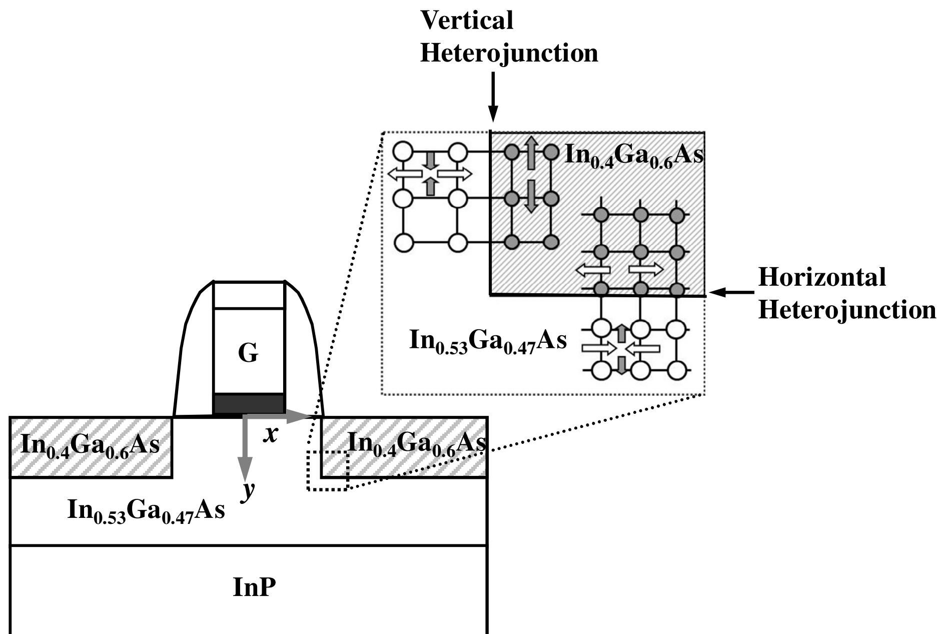
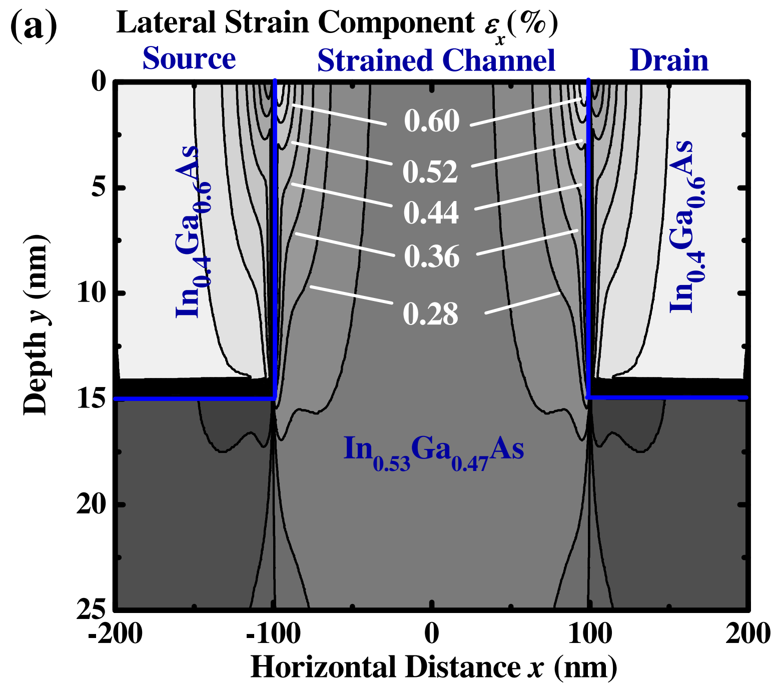


Fig. 3.3 Schematic illustration of a strained N-channel $In_{0.53}Ga_{0.47}As$ transistor with lattice-mismatched $In_{0.4}Ga_{0.6}As$ S/D stressors. The $In_{0.4}Ga_{0.6}As$ stressor stretches the $In_{0.53}Ga_{0.47}As$ lattice at both the horizontal and vertical heterojunctions, as shown in the inset.

A finite element study was performed to investigate the distribution of strain components in $In_{0.53}Ga_{0.47}As$ MOSFET structures with $In_{0.4}Ga_{0.6}As$ S/D regions, which is similar to Si transistor with SiGe S/D stressors [3.17]. Fig. 3.4(a) and (b) show the simulated lateral strain ε_x and vertical strain ε_y profile of $In_{0.53}Ga_{0.47}As$ MOSFET structures with $In_{0.4}Ga_{0.6}As$ S/D regions and gate length of 200 nm, respectively. Largest ε_x in the channel is observed to locate near the top surface of $In_{0.53}Ga_{0.47}As$ channel where the inversion layer is formed, therefore contributing favorably to drive current and carrier transport enhancement. The lateral tensile strain, induced along the channel of the transistor structure, decreases with increasing distance from the $In_{0.4}Ga_{0.6}As$ regions. In addition, the lateral tensile strain also decreases with increasing depth from the gate dielectric-$In_{0.53}Ga_{0.47}As$ interface. The vertical strain in the $In_{0.53}Ga_{0.47}As$ channel behaves similarly and is compressive in nature.



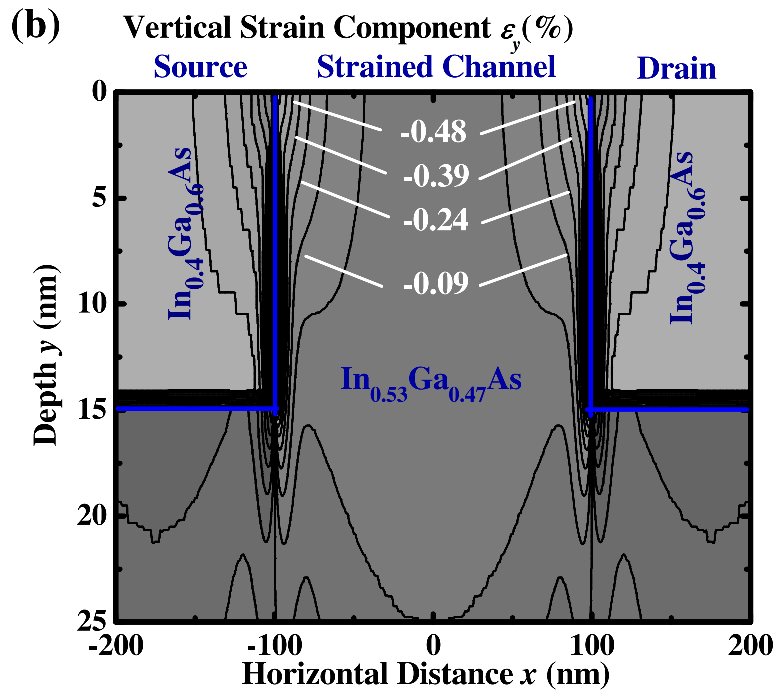


Fig. 3.4 Finite element simulation obtained the distribution of (a) lateral strain ε_x and (b) vertical strain ε_y in the strained $In_{0.53}Ga_{0.47}As$ channel. The S/D recess depth is 15 nm, and the separation between the $In_{0.4}Ga_{0.6}As$ source and drain regions is 200 nm.

Fig. 3.5 compares the average ε_x and ε_y in the transistor channel within top 5 nm from the gate dielectric-$In_{0.53}Ga_{0.47}As$ interface as a function of gate lengths. A larger strain is obtained in the transistor with the smaller gate length. As the gate length becomes smaller, the $In_{0.4}Ga_{0.6}As$ regions are placed closer together, giving rise to a larger strain in the channel. The increase in the strain induced in the channel with gate length downsizing is a significant advantage of this approach, since it leads to scalable performance enhancement.

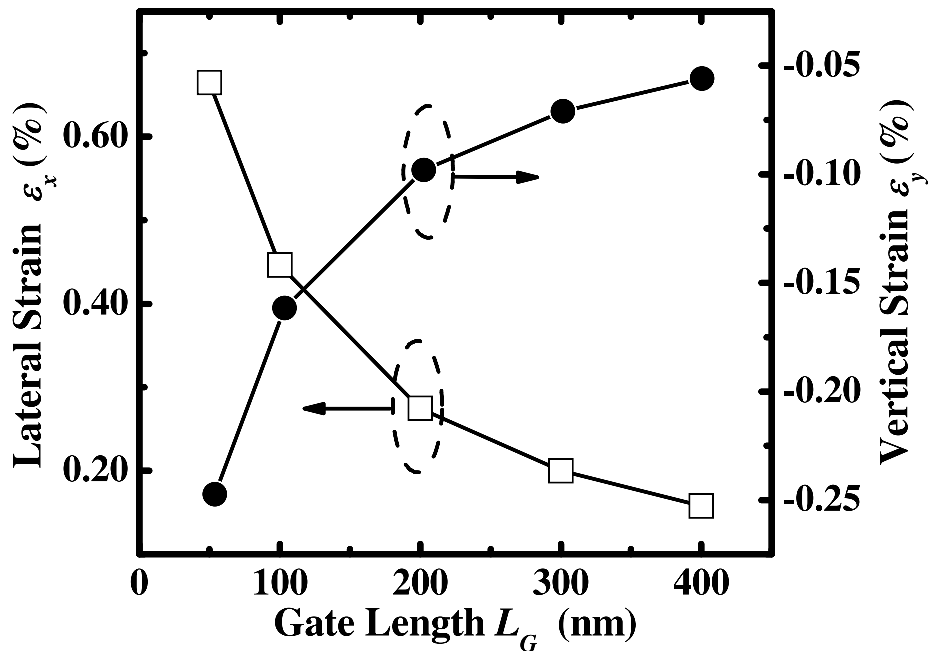


Fig. 3.5 Average lateral strain ε_x and vertical strain ε_y in the transistor channel within top 5 nm from the gate dielectric-$In_{0.53}Ga_{0.47}As$ interface at various gate lengths. Both strain components increase in magnitude with smaller gate length, and can be exploited for performance scaling.

3.2.2 Process Development of Selective InGaAs Epitaxy with *In-situ* Doping

Dilute HCl cleaning was performed to remove native oxide on the $In_{0.53}Ga_{0.47}As$ surface prior to selective epitaxial growth in a metal organic chemical vapor deposition (MOCVD) reactor. Trimethylgallium (TMGa), tertiarybutylarsine (TBA), and trimethylindium (TMIn) were employed as the precursors for the MOCVD process. Flow rates of TMGa, TBA, and TMIn were 9 sccm, 60 sccm, and 130 sccm, respectively. Silane (SiH_4) was introduced during the epitaxy process to achieve *in-situ* N-type doping. The pressure of the reactor during MOCVD epitaxy was 75 Torr. The MOCVD reactor was not directly operated by me.

Indium composition and growth temperature are the two key factors affecting the selective epitaxy of InGaAs [Fig. 3.6(a)]. When indium composition is low, Fig. 3.6(b) shows undesirable three-dimensional growth of InGaAs dots on S/D regions due to huge lattice mismatch with $In_{0.53}Ga_{0.47}As$. The islanding process relieves the stress accumulated at the InGaAs heterojunction. When indium composition is increased or lattice mismatch is reduced, two-dimensional growth mode becomes the dominant mechanism. SEM image in Fig. 3.6(c) show high quality InGaAs epitaxy with lattice mismatch of 0.9 % at the heterojunction. However, selectivity over silicon oxide (SiO_2) or silicon oxynitride (SiON) regions was not achieved. The growth temperature was increased to 635 °C to enable the desorption of nucleated seeds on SiO_2 or SiON regions for achieving high growth selectivity, as illustrated in Fig. 3.6(d).

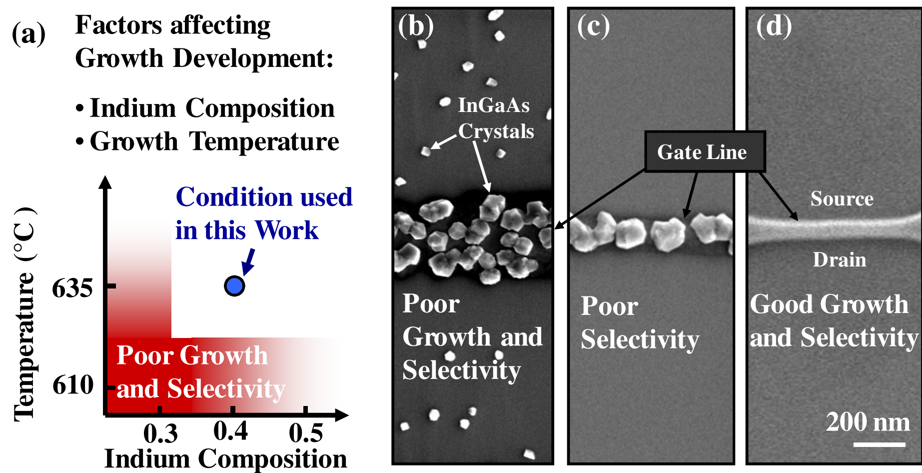


Fig. 3.6 (a) Indium composition and temperature are key factors affecting the growth. SEM images showing film quality and growth selectivity under different epitaxy conditions. (b) Huge lattice mismatch leads to three-dimensional growth of InGaAs dots. (c) Two-dimensional growth of InGaAs layer was achieved with smaller lattice mismatch. (d) Higher temperature enables the desorption of nucleated seeds on the gate lines to achieve selective growth.

High resolution X-ray diffraction (HRXRD) was employed to investigate the composition of indium in the InGaAs epilayer. The X-ray diffraction was performed on a separate monitor wafer, as the dimensions of the source/drain regions, 100 μm by 100 μm, are much smaller than the spot size of X-ray during HRXRD analysis, 3 mm by 12 mm. The composition of indium incorporated in the InGaAs layer was determined to be ~40 %, as shown in Fig. 3.7. $In_{0.4}Ga_{0.6}As$ has a lattice constant ~1 % smaller than that of $In_{0.53}Ga_{0.47}As$. Pendellösung oscillation fringes can be observed clearly, indicating high crystalline quality and flat interface of the structure. Cross-sectional transmission electron microscopy (TEM) image in Fig. 3.8 shows a transistor structure with $In_{0.4}Ga_{0.6}As$ stressor and SiON dummy gate. The recess depth formed by chorine (Cl_2)-based dry etching process is about 20

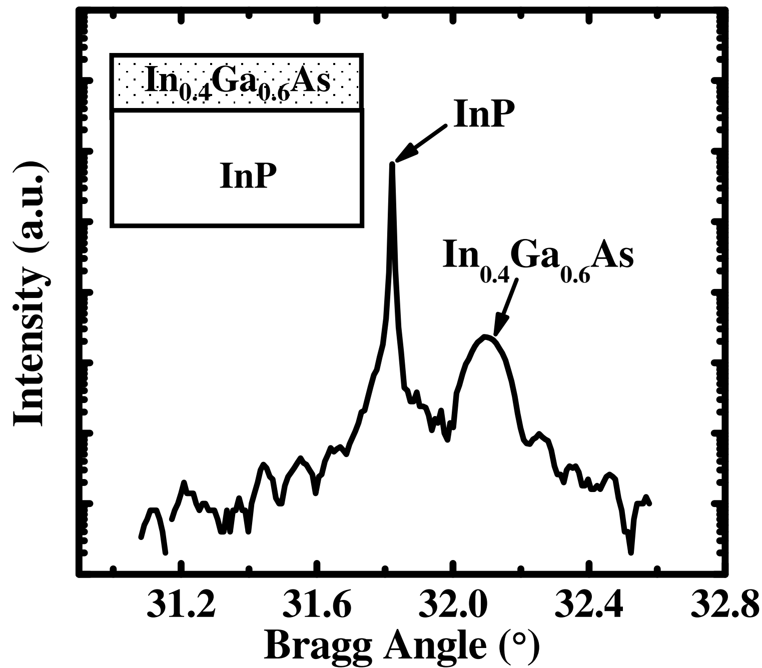


Fig. 3.7 The well-defined InGaAs peak in the high resolution XRD indicates high crystalline quality of the InGaAs epilayer. The composition of indium in the InGaAs epilayer was determined to be ~40 %.

nm. The regrown $In_{0.4}Ga_{0.6}As$ region demonstrates excellent crystalline quality and high growth selectivity over SiON.

Next, the sheet resistance of InGaAs film with *in-situ* doping during S/D regrowth process is investigated. Transmission line method (TLM) test structure with low resistance palladium germanide (PdGe) ohmic contacts was employed to accurately extract the sheet resistance value. Fig. 3.9 compares the sheet resistance of N-type InGaAs films formed by *in-situ* SiH_4 doping process and by Si^+ implantation and dopant activation. The implant conditions of the control were adjusted such that similar junction depths were obtained, as confirmed by secondary ion mass spectrometry (SIMS) analysis. ~ 20 % reduction in the sheet resistance was achieved using the *in-situ* doping process,

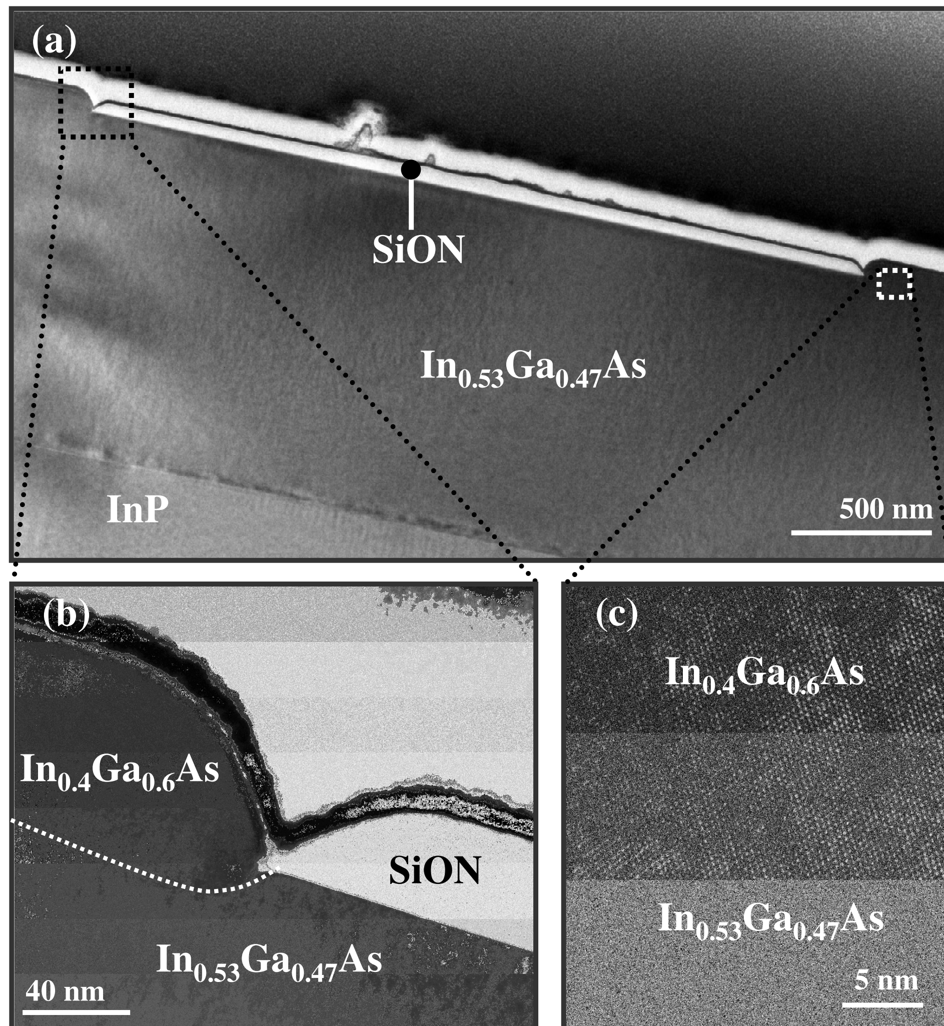


Fig. 3.8 Cross-sectional TEM micrographs showing (a) an $In_{0.53}Ga_{0.47}As$ transistor structure with SiON dummy gate and selective grown $In_{0.4}Ga_{0.6}As$ structures on the S/D regions, and (b) a zoomed-in view of a region in (a) which shows raised $In_{0.4}Ga_{0.6}As$ S/D structure and SiON dummy gate. The recess depth is about 20 nm and the thickness of $In_{0.4}Ga_{0.6}As$ stressor is 70 nm. (c) A high resolution zoomed-in view of a region showing the heterojunction highlighted in (a). Pseudomorphic epitaxy of $In_{0.4}Ga_{0.6}As$ on $In_{0.53}Ga_{0.47}As$ was achieved in this MOCVD process.

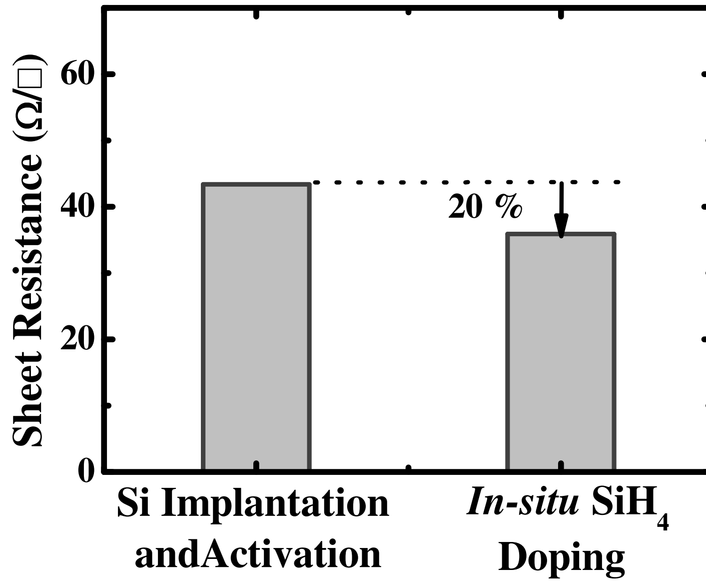


Fig. 3.9 Comparison of sheet resistance of N-type InGaAs layer formed by *in-situ* SiH_4 doping process and by Si^+ implantation and dopant activation. The sheet resistance is extracted using TLM test structure. *In-situ* SiH_4 doping process leads to significant reduction in R_{SD} for enhanced transistor performance.

which is crucial to reduce the R_{SD} of a transistor. R_{SD} cannot be improved by simply increasing the implant dose of Si^+ due to the difficulty to re-crystallize amorphous III-V material and the formation of Si on As site acceptors at high Si level.

3.2.3 Device Fabrication

The key process steps for forming an $In_{0.53}Ga_{0.47}As$ channel N-MOSFET with *in-situ* doped $In_{0.4}Ga_{0.6}As$ S/D stressors are summarized in Fig. 3.10. P-type Be-doped (100)-oriented $In_{0.53}Ga_{0.47}As$/InP substrates with a doping concentration N_A of 1 - 5 $\times 10^{16}$ cm^{-3} were used. After pre-gate cleaning in HCl, NH_4OH, and followed by $(NH_4)_2S$, the wafers were quickly loaded into a multiple-chamber gate cluster system, where 550 °C vacuum anneal, SiH_4 + NH_3 passivation, and MOCVD deposition of HfAlO were

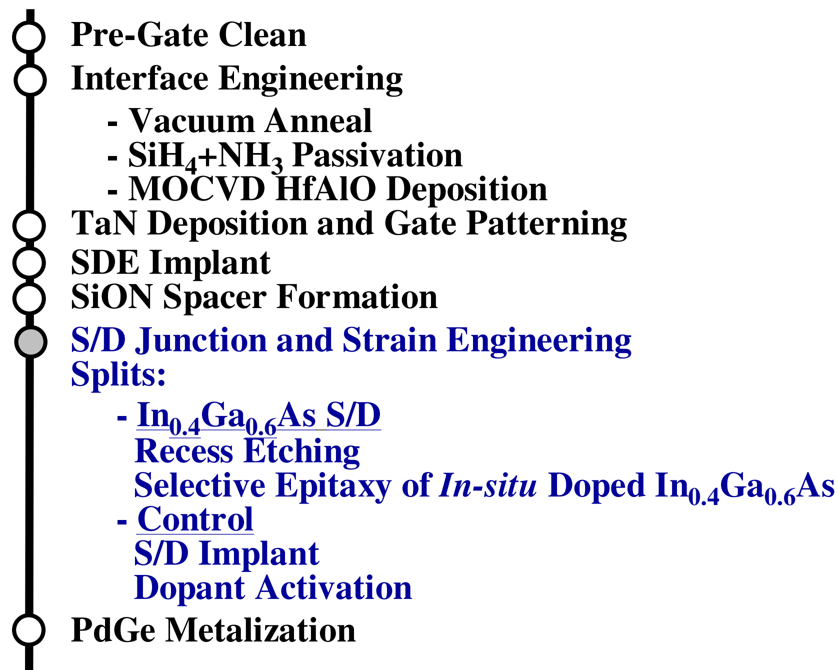


Fig. 3.10 Process sequence employed in transistor fabrication. The $In_{0.53}Ga_{0.47}As$ recess etch and $In_{0.4}Ga_{0.6}As$ selective epitaxy steps are introduced to replace S/D implant step in the fabrication process.

performed. This was followed by post-gate dielectric deposition anneal and reactive sputter deposition of TaN as gate electrode. A SiO_2 hardmask was deposited to cover the TaN gate during the selective epitaxy process. After gate patterning, S/D extension (SDE) implantation was performed before forming the SiON spacers.

Process steps for all devices are exactly the same except for the deep S/D formation step. For control devices, deep S/D regions were formed by self-aligned implantation (10^{14} Si atoms/cm^2 at 50 keV), and a rapid thermal annealing (650 ˚C for 60 s in N_2 ambient) to activate the dopants, including those in the SDE. For the strained MOSFETs, S/D recess etch was performed followed by selective epitaxy using MOCVD to form 50 nm thick *in-situ* doped single-crystalline $In_{0.4}Ga_{0.6}As$ S/D. The thermal budget from the

MOCVD growth (635 ˚C for 120 s) was used for dopant activation in the SDE. Finally, low resistance CMOS-compatible PdGe contacts were integrated for all devices.

3.3 Device Characterization and Analysis

In this section, the advantages of integrating *in-situ* doped $In_{0.4}Ga_{0.6}As$ S/D stressors to $In_{0.53}Ga_{0.47}As$ MOSFETs are evaluated based on comparison with control $In_{0.53}Ga_{0.47}As$ devices featuring $In_{0.53}Ga_{0.47}As$ S/D regions formed by implantation and dopant activation.

Fig. 3.11(a) shows I_D–V_D family of curves for a pair of surface channel $In_{0.53}Ga_{0.47}As$ MOSFETs with L_G of 200 nm. The $In_{0.53}Ga_{0.47}As$ MOSFETs demonstrate good saturation and pinch-off characteristics. A 28 % enhancement in drive current was achieved at a gate overdrive V_G–V_T of 3 V and V_D of 3 V in the strained channel device with *in-situ* doped lattice-mismatched $In_{0.4}Ga_{0.6}As$ S/D. Fig. 3.11(b) shows the I_D–V_G characteristics of the same pair of devices in the linear (V_{DS} = 100 mV) and saturation (V_{DS} = 1.2 V) regions. The devices exhibit comparable subthreshold swing of 200 mV/decade and drain-induced barrier lowering (DIBL) of 130 mV/V. It is obvious that $In_{0.53}Ga_{0.47}As$-channel N-MOSFET integrated with *in-situ* doped $In_{0.4}Ga_{0.6}As$ S/D stressors exhibits enhanced saturation drive current I_{Dsat} over control N-MOSFET. This clearly established the applicability of *in-situ* doped lattice-mismatched S/D stressors for InGaAs MOSFETs.

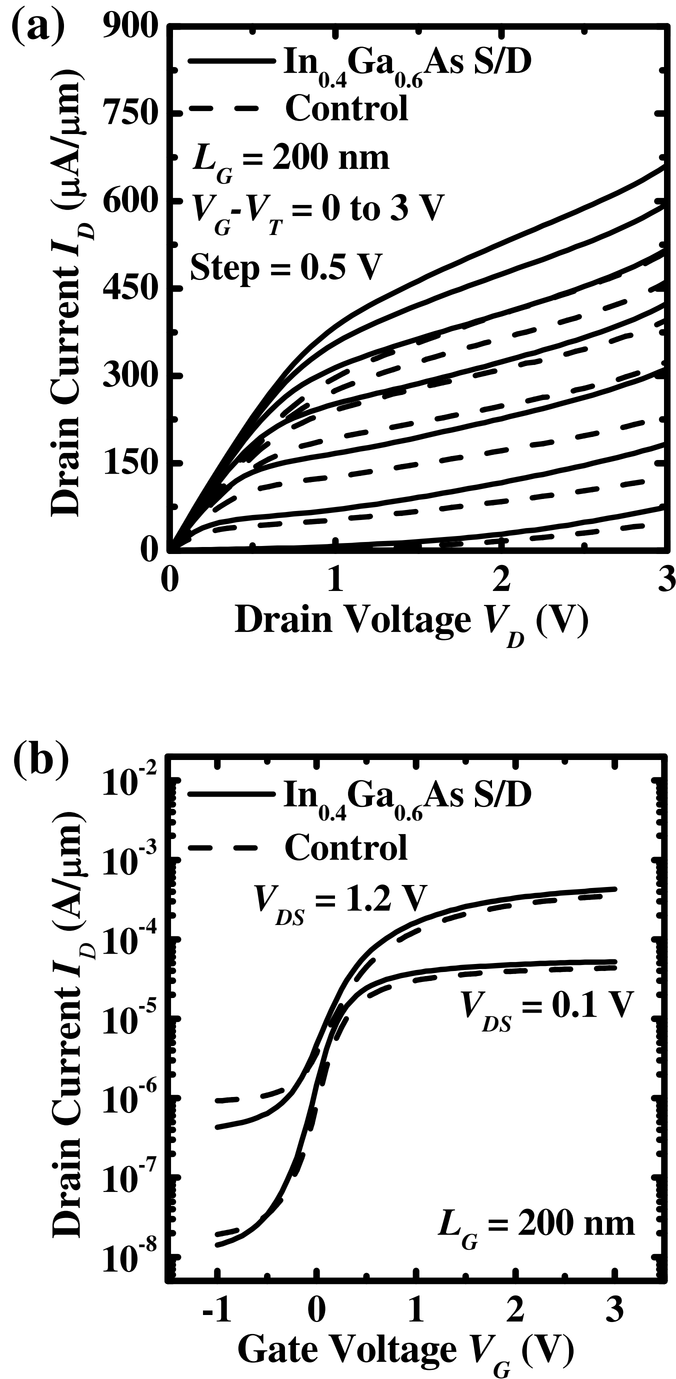


Fig. 3.11 (a) I_D–V_D, and (b) I_D–V_G characteristics showing current enhancement in the $In_{0.53}Ga_{0.47}As$ N-MOSFET with *in-situ* doped $In_{0.4}Ga_{0.6}As$ S/D regions over a control $In_{0.53}Ga_{0.47}As$ N-MOSFET. Both devices have a gate length of 200 nm. The control N-MOSFET has $In_{0.53}Ga_{0.47}As$ S/D regions.

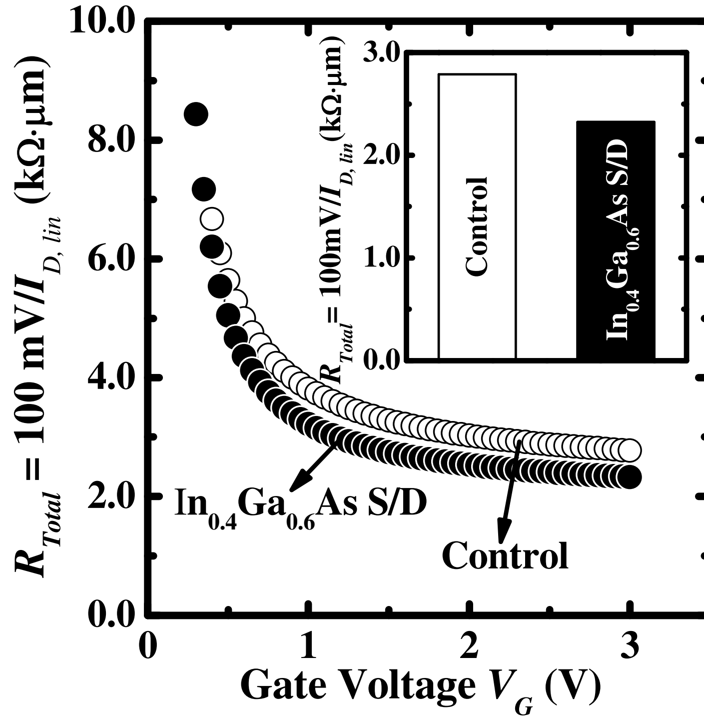


Fig. 3.12 R_{Total} as a function of V_G for strained $In_{0.53}Ga_{0.47}As$ N-MOSFET with *in-situ* doped $In_{0.4}Ga_{0.6}As$ S/D regions and control $In_{0.53}Ga_{0.47}As$ N-MOSFET. L_G is 200 nm and V_D is 0.1 V. Higher S/D doping level in N-MOSFET with *in-situ* doped $In_{0.4}Ga_{0.6}As$ S/D regions gives a reduced series resistance. Inset shows the extracted R_{SD} at V_G of 3 V.

The R_{Total} of a transistor measured at low drain bias decreases with increasing gate bias V_G, and approaches R_{SD} at large V_G. R_{Total} is calculated by dividing drain bias over measured drain current. R_{SD} is the sum of the source resistance R_S and drain resistance R_D, where R_S is equal to R_D for a symmetric device. Fig. 3.12 plots the R_{Total} versus V_G characteristics of the same pair of InGaAs transistors. *In-situ* doped $In_{0.4}Ga_{0.6}As$ S/D reduced the R_{SD} by ~ 20 %, as compared to the control device. This is attributed to higher doping concentration achieved by the *in-situ* SiH_4 doping process.

Fig. 3.13 shows the extrinsic linear transconductance $G_{m,ext}$. $G_{m,ext}$ is an affected by both carrier mobility and R_{SD}. To take out the effect of R_{SD}, the

intrinsic linear transconductance $G_{m,int}$ was extracted based on the following equations [3.18]:

$$G_{m,int} = \frac{G_m^0}{1-(R_S+R_D)\cdot G_D(1+R_S\cdot G_m^0)} \quad (3\text{-}3)$$

$$G_m^0 = \frac{G_{m,ext}}{1-R_S\cdot G_{m,ext}} \quad (3\text{-}4)$$

where G_D is the measured drain conductance or slope in I_D-V_D plot (dI_D/dV_D). Source resistance R_S and drain resistance R_D are half of R_{SD} obtained in Fig. 3.12. $G_{m,ext}$ is extrinsic transconductance or slope in I_D-V_G plot (dI_D/dV_G). Intrinsic linear transconductance $G_{m,int}$ is free from series resistance effects and is directly related to the carrier mobility. Using the R_S extracted from

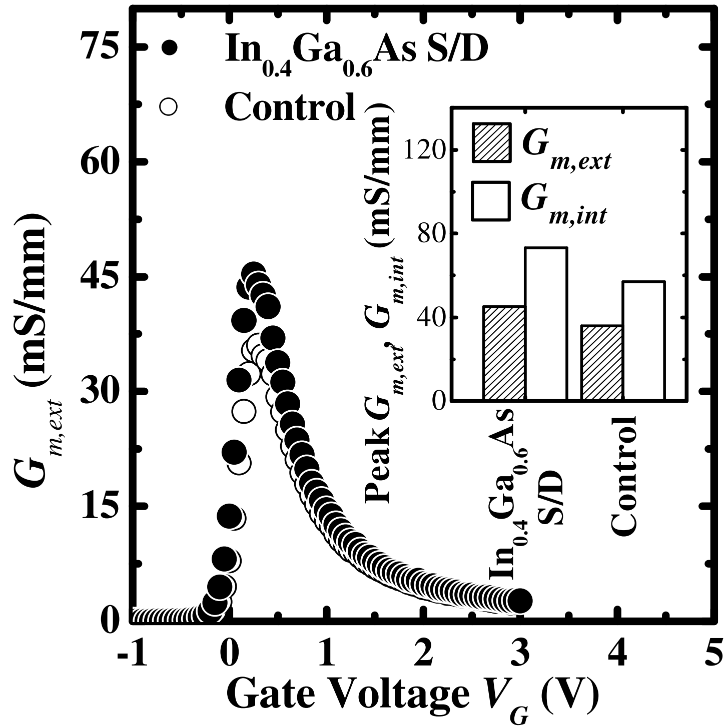
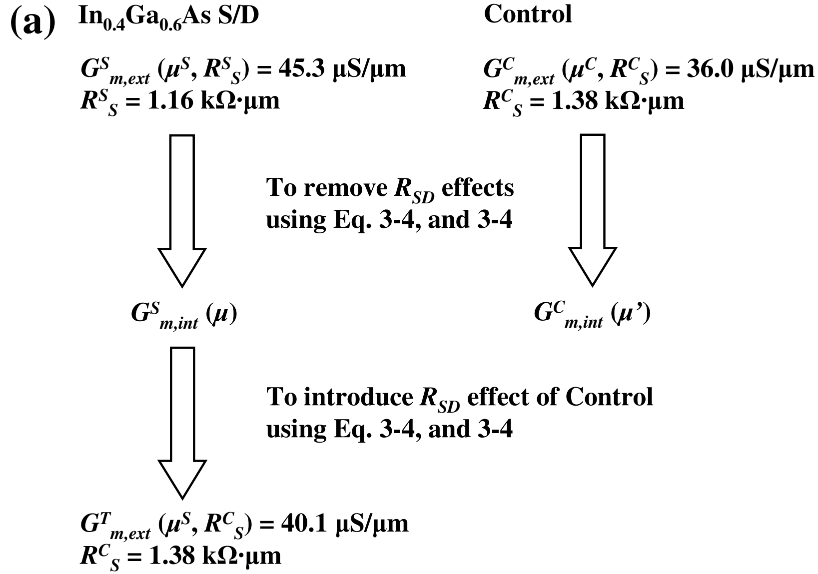


Fig. 3.13 Linear $G_{m,ext}$ versus V_G of strained and control devices at V_D of 0.1 V. The inset plots the extracted peak linear $G_{m,int}$ of both strained and control devices. The 28 % improvement in peak $G_{m,int}$ is due to improvement in carrier mobility.

Fig. 3.12, $G_{m,int}$ of strained $In_{0.53}Ga_{0.47}As$ MOSFET ($G^{S}_{m,int}$) and control ($G^{C}_{m,int}$) can be extracted using equations 3-3, and 3-4, respectively. The strained $In_{0.53}Ga_{0.47}As$ MOSFET demonstrates $G_{m,int}$ enhancement of ~ 28 % over the control device, indicating carrier mobility improvement [inset of Fig. 3.13]. This is attributed to lateral tensile strain induced in the transistor channel. Tensile strain modifies the Γ–valley minimum to become ellipsoidal and contributes to reduced effective mass along the transport direction [3.15]. Peak $G_{m,ext}$, which is also related to R_{SD}, increased from 36.0 μS/μm for the control transistor to 45.3 μS/μm for the strained transistor, giving a change in $G_{m,ext}$ of 9.3 μS/μm or 26 % enhancement. Fig. 3.14(a) shows the procedure to analyze the contribution from carrier mobility and R_{SD} to total $G_{m,ext}$ enhancement. $G_{m,ext}$ of the InGaAs device with mobility of the strain channel and R_S of the control ($G^{T}_{m,ext}$) can be calculated using equations 3-3, and 3-4. As illustrated by Fig. 3.14(b), change in $G_{m,ext}$ due carrier mobility enhancement can be estimated based on the difference between $G^{T}_{m,ext}$ and $G_{m,ext}$ of control ($G^{C}_{m,ext}$), as R_S is kept constant. Similarly, the difference between $G^{T}_{m,ext}$ and $G_{m,ext}$ of InGaAs device with $In_{0.4}Ga_{0.6}As$ S/D ($G^{S}_{m,ext}$) shows the enhancement due to R_S, as carrier mobility is the same. Our analysis shows that 44 % of $G_{m,ext}$ comes from mobility enhancement and 56 % of $G_{m,ext}$ comes from R_{SD} reduction. Further performance improvement is expected with device scaling due to increased channel strain with reduced separation between the $In_{0.4}Ga_{0.6}As$ S/D regions.

The I_{OFF}–I_{Dsat} characteristics in Fig. 3.15 show that *in-situ* doped $In_{0.4}Ga_{0.6}As$ S/D enhance I_{Dsat} by 25% at a fixed I_{OFF} of 10^{-6} A/μm. Larger enhancement is observed at shorter gate length due to enhanced strain effects.

Although the devices studied here do not have aggressively scaled gate lengths or comparable performance with state-of-the-art Si N-MOSFETs, the concept of lattice mismatched *in-situ* doped S/D was demonstrated and could be attractive for further exploration in future high performance III-V MOSFETs.



(b)

Difference between		Due to difference in
$G^S_{m,ext}$ (μ^S, R^S_S) and $G^C_{m,ext}$ (μ^C, R^C_S)	9.3 µS/µm	μ and R_S
$G^T_{m,ext}$ (μ^S, R^C_S) and $G^C_{m,ext}$ (μ^C, R^C_S)	4.1 µS/µm or 44 % of 9.3 µS/µm	μ
$G^S_{m,ext}$ (μ^S, R^S_S) and $G^T_{m,ext}$ (μ^S, R^C_S)	5.2 µS/µm or 56 % of 9.3 µS/µm	R_S

Fig. 3.14 (a) Schematic illustrating the extraction of $G^S_{m,int}$, $G^C_{m,int}$, $G^T_{m,ext}$ to analyze the contributions from carrier mobility and R_{SD} to total $G_{m,ext}$ enhancement, using equations 3-3, and 3-4. (b) By comparing among $G^S_{m,ext}$, $G^C_{m,ext}$, and $G^T_{m,ext}$, the contribution from carrier mobility and R_{SD} can be separated.

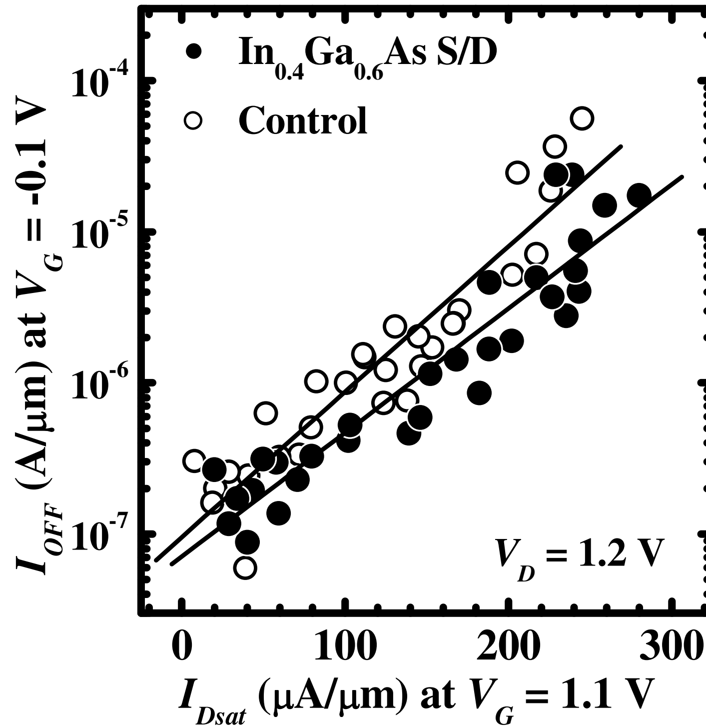


Fig. 3.15 Plot of off-state leakage I_{OFF} versus on-state saturation drain current I_{Dsat} showing significant enhancement in I_{Dsat} for $In_{0.53}Ga_{0.47}As$ MOSFET with *in-situ* doped $In_{0.4}Ga_{0.6}As$ S/D over control MOSFET.

3.4 Summary

The concept of channel strain engineering using lattice-mismatched S/D stressors and S/D doping engineering using *in-situ* SiH_4 doping process has been successfully demonstrated for the enhancement of electron mobility and the reduction of R_{SD} of III-V channel N-MOSFETs. For the first time, a novel strained-$In_{0.53}Ga_{0.47}As$ channel N-MOSFET, comprising *in-situ* doped lattice-mismatched $In_{0.4}Ga_{0.6}As$ S/D regions, was demonstrated. Due to the lattice interactions at the heterojunction between $In_{0.53}Ga_{0.47}As$ channel and $In_{0.4}Ga_{0.6}As$ S/D regions, beneficial strain components can be induced in the adjacent transistor channel region, leading to significant carrier transport improvement. Through finite element simulations, it has been verified that the

$In_{0.4}Ga_{0.6}As$ regions act as stressors, giving rise to lateral tensile strain and vertical compressive strain in the $In_{0.53}Ga_{0.47}As$ channel for enhanced electron mobility. In addition, with the achievement of higher N-type doping concentration by *in-situ* doping process in the S/D regions, significant reduction in R_{SD} was achieved, contributing to the reduction of total resistance in a transistor for performance enhancement. Significant improvement in drive current performance was observed, which could partially be attributed to strain-induced electron mobility enhancement and series resistance reduction due to *in-situ* S/D doping. Both effects are expected to become more prominent in aggressively scaled MOSFETs. This chapter clearly illustrates the potential of *in-situ* doped lattice-mismatched S/D stressor to extend the device performance of III-V transistors for future technology nodes.

3.5 References

[3.1] C. Hu, “Device challenges and opportunities,” in *VLSI Symp. Tech. Dig.*, 2004, pp. 4–5.

[3.2] H. M. Manasevit, I. S. Gergis, and A. B. Jones, “Electron mobility enhancement in epitaxial multilayer Si-SiGe alloys films on (100) Si,” *Appl. Phys. Lett.*, vol. 41, no. 5, pp. 464–466, 1982.

[3.3] R. People, J. C. Bean, D. V. Lang, A. M. Sergent, H. L. Stormer, K. W. Wecht, R. T. Lynch, and K. Baldwin, “Modulation doping in GeSi/Si strained layer heterostructures,” *Appl. Phys. Lett.*, vol. 45, no. 11, pp. 1231–1233, 1984.

[3.4] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, “A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors,” in *IEDM Tech. Dig.*, 2003, pp. 978–980.

[3.5] S. E. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, “Key differences for process induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs,” in *IEDM Tech. Dig.*, 2004, pp. 221–224.

[3.6] P. R. Chidambaram, B. A. Smith, L. H. Hall, H. Bu, S. Chakravarthi, Y. Kim, A. V. Samoilov, A. T. Kim, P. J. Jones, R. B. Irwin, M. J. Kim, A. L. P. Rotondaro, C. F. Machala, and D. T. Grider, “35% drive

current improvement from recessed-SiGe drain extensions on 37 nm gate length PMOS," in *VLSI Symp. Tech. Dig.*, 2004, pp. 48–49.

[3.7] D. Zhang, B. Y. Nguyen, T. White, B. Goolsby, T. Nguyen, V. Dhandapani, J. Hildreth, M. Foisy, V. Adams, Y. Shibo, A. Thean, D. Theodore, M. Canonico, S. Zollner, S. Baichi, S. Murphy, R. Rai, J. Jiang, M. Jahanbani, R. Nibble, M. Zavala, R. Cotton, D. Eades, S. Parsons, P. Montogomery, A. Martinez, B. Winstead, M. Medicino, J. Cheek, J. Liu, P. Grudoswki, N. Ramami, P. Tomasinini, C. Arena, C. Werkhoven, H. Kirby, C. H. Chang, C. T. Liu, H. C. Tuan, Y. C. See, S. Vankatesan, V. Kolagunta, N. Cave, and J. Mogab, "Embedded SiGe S/D PMOS on thin body SOI substrate with drive current enhancement," in *VLSI Symp. Tech. Dig.*, 2005, pp. 26–29.

[3.8] K. W. Ang, K. J. Chui, V. Bliznetsov, A. Du, N. Balasubramanian, M. F. Li, G. Samudra, and Y.-C. Yeo, "Enhanced performance in 50 nm N-MOSFETs with silicon-carbon source/drain regions," in *IEDM Tech. Dig.*, 2004, pp. 1069–1071.

[3.9] K.-J. Chui, K.-W. Ang, N. Balasubramanian, M.-F. Li, G. Samudra, and Y.-C. Yeo, "NMOSFET with silicon-carbon source/drain for enhancement of carrier transport," *IEEE Trans. Electron Devices*, vol. 54, no. 2, pp. 249–256, 2007.

[3.10] K.-W. Ang, K.-J. Chui, V. Bliznetsov, Y. Wang, L.-Y. Wong, C.-H. Tung, N. Balasubramanian, M. F. Li, G. S. Samudra, and Y.-C. Yeo, "Thin body silicon-on-insulator N-MOSFET with silicon-carbon source/drain regions for performance enhancement," in *IEDM Tech. Dig.*, 2005, pp. 503–506.

[3.11] K.-J. Chui, K.-W. Ang, H.-C. Chin, C. Shen, L.-Y. Wong, C.-H. Tung, N. Balasubramanian, M. F. Li, G. S. Samudra, and Y.-C. Yeo, "Strained silicon-on-insulator n-channel transistor with silicon-carbon source/drain regions for carrier transport enhancement," *IEEE Electron Device Letters*, vol. 27, no. 9, pp. 778–780, 2006.

[3.12] Y.-C. Yeo, "Enhancing CMOS transistor performance using lattice-mismatched materials in source/drain regions," *Semicond. Sci. Technol.*, vol. 22, pp. S177–S182, 2007.

[3.13] K.-W. Ang, K.-J. Chui, C.-H. Tung, N. Balasubramanian, G. S. Samudra, and Y.-C. Yeo, "Performance enhancement in uniaxial strained silicon-on-insulator N-MOSFETs featuring silicon-carbon source/drain regions," *IEEE Trans. on Electron Devices*, vol. 54, no. 11, pp. 2910–2917, 2007.

[3.14] G. E. Pikus, and G. L. Bir, *Symmetry and Strained-Induced Effects in Semiconductors*, New York, J. Wiley, 1974.

[3.15] C. Kopf, H. Kosina, and S. Selberherr, "Physical models for strained and relaxed GaInAs alloys: Band structure and low-field transport," *Sol.-State Elec.*, vol. 41, no. 8, pp. 1139–1152, 1997.

[3.16] S. Suthram, Y. Sun, P. Majhi, I. Ok, H. Kim, H. R. Harris, N. Goel, S. Parthasarathy, A. Koehler, T. Acosta, T. Nishida, H.-H. Tseng, W. Tsai, J. Lee, R. Jammy, and S. E. Thompson, "Strain additivity in III-V channels for CMOSFETs beyond 22 nm technology node," in *VLSI Symp. Tech. Dig.*, 2008, pp. 182–183.

[3.17] Y.-C. Yeo, and J. Sun, “Finite element study of strain distribution in transistor with silicon-germanium source and drain regions,” *Appl. Phys. Lett*., vol. 86, no. 2, p. 023103, 2005.

[3.18] S. Y. Chou, and D. A. Antoniadis, “Relationship between measured and intrinsic transconductances of FET’s,” *IEEE Trans. Electron Device*, vol. ED-34, no. 2, pp. 448–450, 1987.

Chapter 4

III-V Multiple-Gate Field-Effect-Transistors (MuGFETs) with High Mobility $In_{0.7}Ga_{0.3}As$ Channel and Epi-Controlled Retrograde-Doped Fin

4.1 Introduction

Device architectures, such as FinFETs or multiple-gate FETs (MuGFETs), are promising device architectures for extending device performance beyond the 22 nm technology node. The benefits derived from such a multiple-gate device architecture include: improved control of SCEs, enhanced volume inversion in the channel region, lower leakage currents, and reduced device variability arising from random dopant fluctuations. At present, technology development for MuGFETs has advanced significantly as it has been a topic of intensive research efforts over the last decade [4.1]-[4.8]. Nevertheless, significant technical challenges exist for the adoption of MuGFETs in high-volume manufacturing.

The integration of multiple gate structure in III-V MOSFETs would be another important direction to explore the full potential of III-V compound semiconductors. In addition, short channel effects (SCEs) are more severe in InGaAs MOSFETs due to its narrower bandgap and higher permittivity.

Recently, $In_{0.53}Ga_{0.47}As$ FinFETs with ALD Al_2O_3 were reported [4.9]. Materials with higher carrier mobility than $In_{0.53}Ga_{0.47}As$ should also be considered, such as $In_{0.7}Ga_{0.3}As$. Nevertheless, MuGFET with $In_{0.7}Ga_{0.3}As$ channel has not been demonstrated.

In this chapter, novel MuGFET or FinFET with InGaAs channel having an indium composition as high as 70% for enhanced carrier mobility, as well as an epi-controlled retrograde-doped fin, with lightly-doped $In_{0.7}Ga_{0.3}As$ channel on top of heavily-doped $In_{0.55}Ga_{0.45}As$ retrograde channel to suppress SCEs is explored. Fig. 4.1 shows the schematic representation of this novel InGaAs MuGFET structure. Transistor output characteristics with high saturation drain current and transconductance were obtained. In addition, significant improvement in the SCEs, such as drain-induced barrier lowering (DIBL), as compared to planar MOSFETs was achieved.

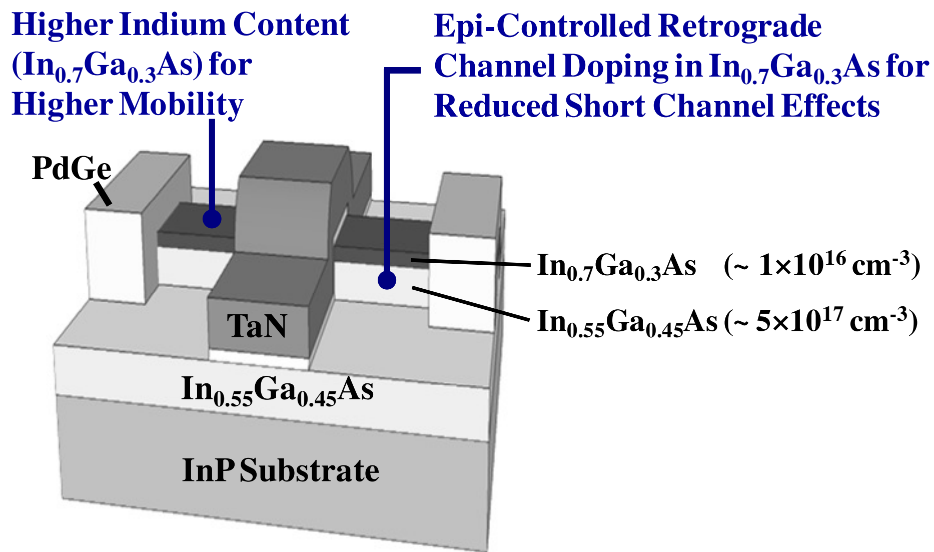


Fig. 4.1 Three-dimensional schematic of N-channel InGaAs MuGFET, comprising high mobility InGaAs channel with indium composition of 70 %, and precise epi-controlled retrograde-doped fin structure.

The fabrication process of the InGaAs MuGFET is first described in Section 4.2. Extensive device simulation and electrical characterization are discussed in Section 4.3. Section 4.4 summarizes the key achievements attained in this work.

4.2 Device Concepts

Extensive three dimensional device simulations using Synopsys's Sentaurus Technology Computer-Aided Design (TCAD) tool were performed to investigate the device performance and electrostatic control of the InGaAs MuGFET. Fig. 4.2 shows the mesh simulation grid of the InGaAs MuGFET structure used in the device simulation. The simulated device has a L_G of 150 nm, W_{fin} of 220 nm, and H_{fin} of 100 nm. For the device with retrograde-doped channel, the N_A of $In_{0.55}Ga_{0.45}As$ retrograde well and $In_{0.7}Ga_{0.3}As$ channel are 5×10^{17} cm^{-3}, and 1×10^{16} cm^{-3}, respectively. For the control without retrograde-doped channel, N_A of $In_{0.55}Ga_{0.45}As$ region is 1×10^{16} cm^{-3}.

Fig. 4.3 shows the conduction band (E_C) profile along the MuGFET at y = 2 nm and 20 nm from the top surface and at the center of the fin with W_{fin} = 220 nm. Improvement in DIBL can be clearly observed by having the retrograde-doped channel. Fig. 4.4 shows the distribution of electrostatic potential in the fin region of InGaAs with V_G of 1.2 V applied to (a) top gate (G_T) and both side gates ($G_{S1} + G_{S2}$), (b) G_T only. Significant difference in the electrostatic potential at the sides of the fin can be observed.

Fig. 4.5(a) and (b) show the distribution of current density along A-A' of the fin, as illustrated in the inset of Fig. 4.5(a), by applying gate bias V_G to $G_T + G_{S1} + G_{S2}$, and to G_T only, respectively. The electron density in the

inversion layer is still surface channel-like. In fact, many MuGFET designs are surface-channel devices, with the inversion layer formed on the top and sidewall surfaces rather than in the bulk of the fin. There are two paths for current flow in this multilayer structure by applying V_G to $G_T + G_{S1} + G_{S2}$ [Fig. 4.5(a)], *i.e.* current flow in the $In_{0.7}Ga_{0.3}As$ top layer (I_{Top}) and current flow along the $In_{0.55}Ga_{0.45}As$ sidewalls ($I_{Side1} + I_{Side2}$). I_{Top} and $I_{Side1}+ I_{Side2}$ can be obtained by integrating the current densities in the region, as specified by Fig. 4.5(a). I_{Top} and $I_{Side1}+ I_{Side2}$ were found to contribute ~66 % and ~34 % of the total drain current, respectively, at V_{GS} = 1.2 V and V_{DS} = 1.2 V.

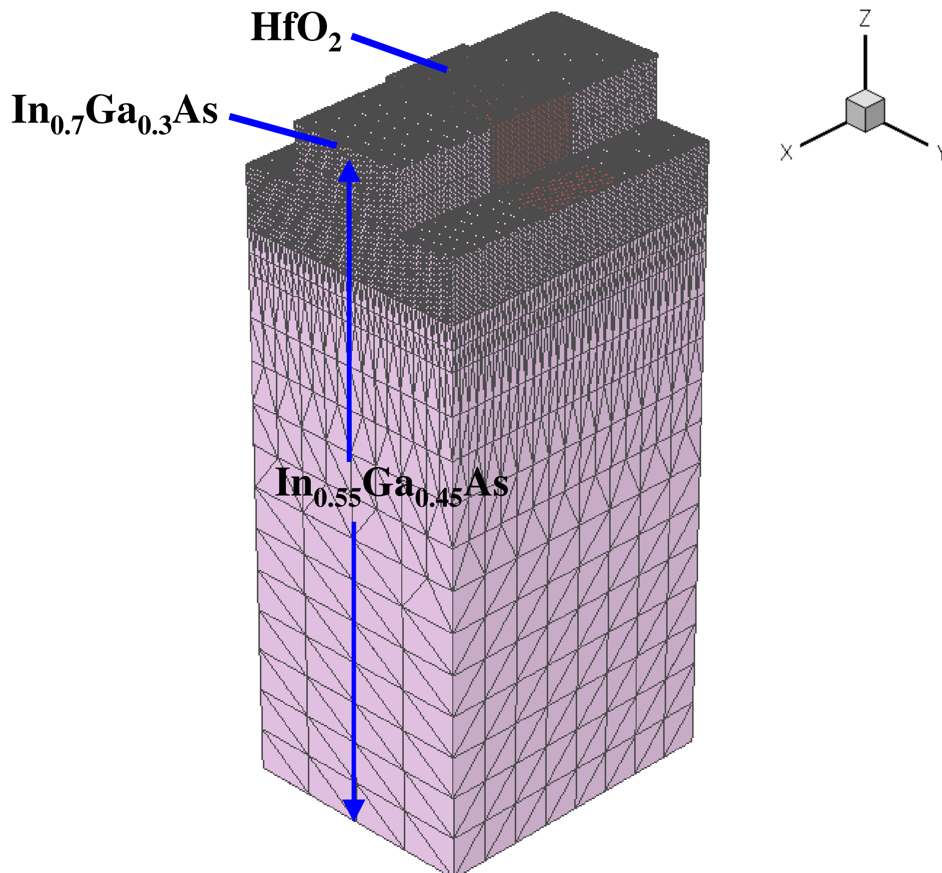


Fig. 4.2 Three-dimensional mesh grid of the InGaAs MuGFET structure used in the device simulation. In the channel region of the transistor, a mesh with tight grid spacing of 1 nm near the oxide-III-V interface is used as the carrier distribution gradient in the inversion layer is steep. The grid spacing is relaxed gradually towards the bulk.

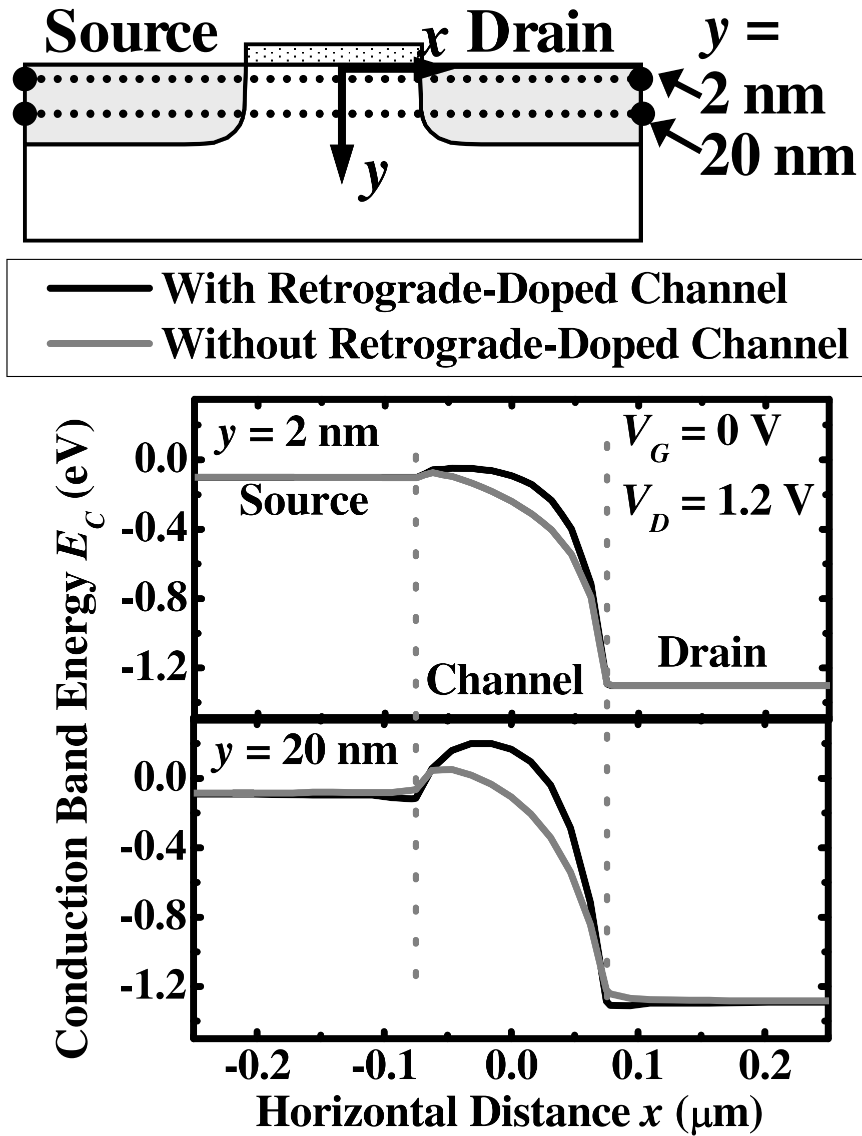


Fig. 4.3 Band diagram of conduction band (E_C) along the MuGFET at y = 2 nm and 20 nm from the top surface and at the center of the fin with W_{fin} = 220 nm, as illustrated in the top schematic.

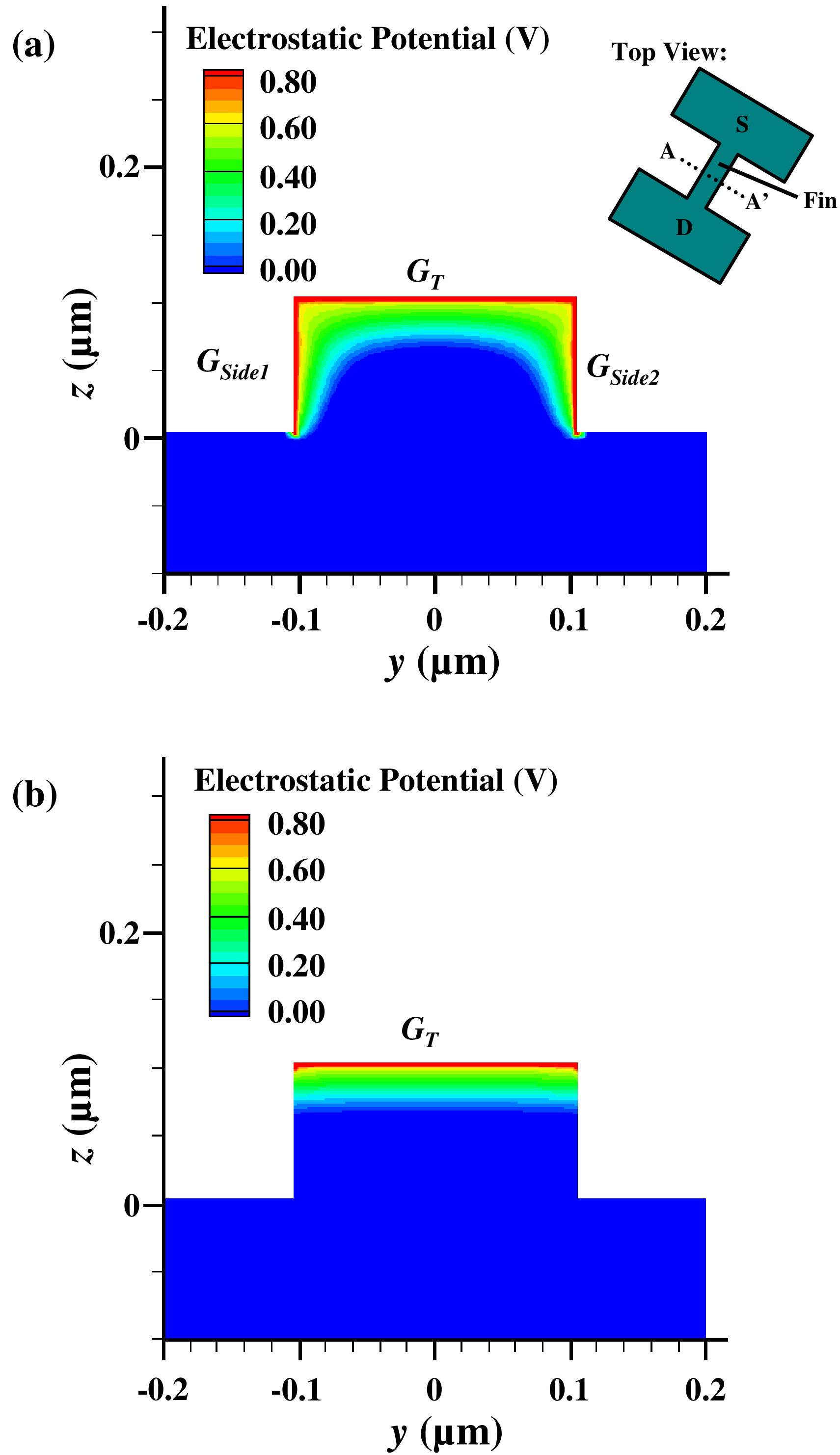


Fig. 4.4 Distribution of electrostatic potential in the fin region of InGaAs with V_G of 1.2 V applied to (a) $G_T + G_{S1} + G_{S2}$, (b) G_T only. V_D of 1.2 V was applied to both cases. Inset shows the position along A-A' of the fin for the analysis.

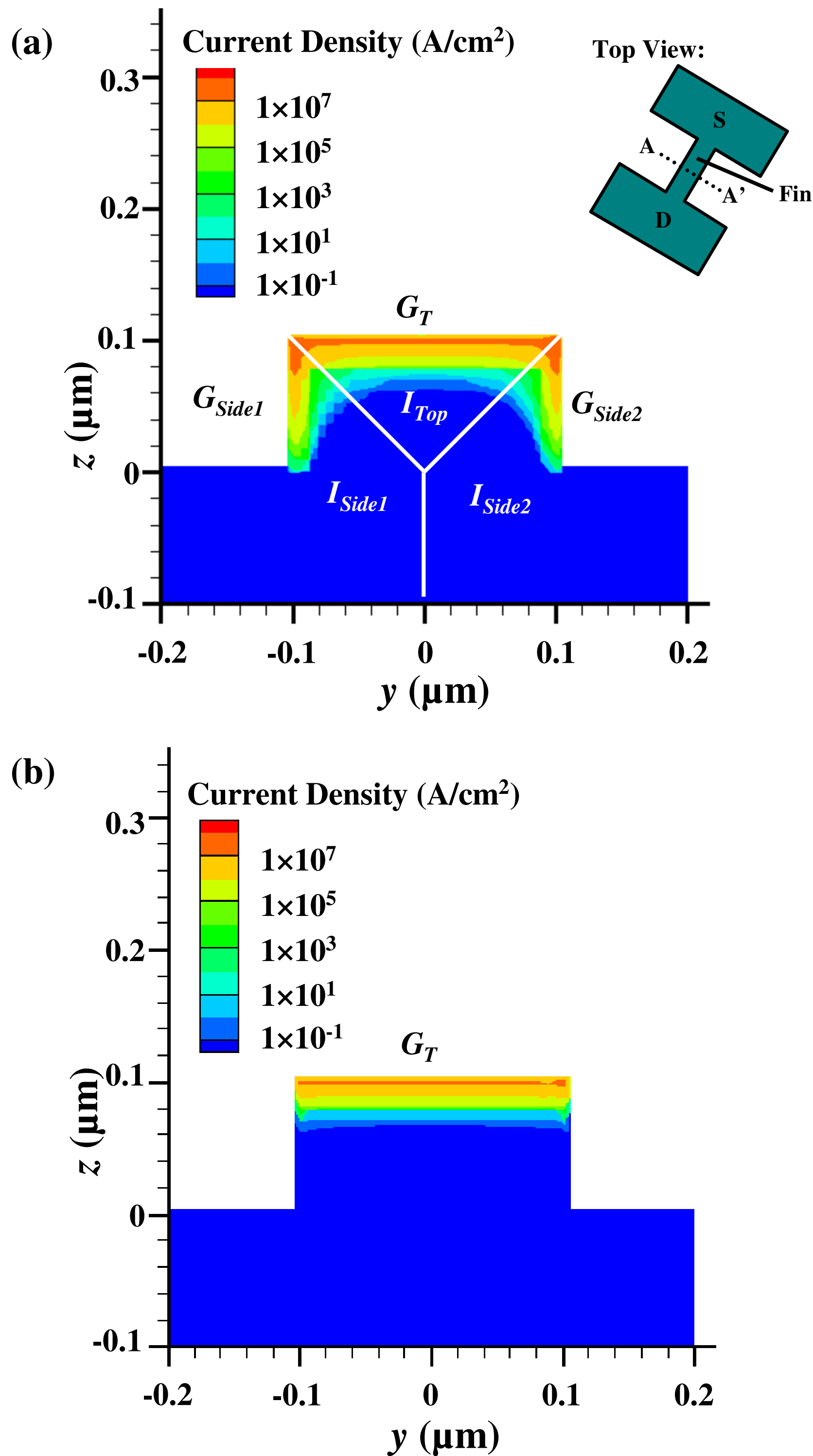


Fig. 4.5 Distribution of current density in the fin region of InGaAs with V_G = 1.2 V and V_D = 1.2 V applied to (a) G_T, G_{S1} and G_{S2}, and (b) G_T only. I_{Top} and I_{Side1} + I_{Side3} were obtained by integrating the current densities over the regions, as illustrated in (a). Inset shows the position along A-A' of the fin for the analysis.

4.3 Device Fabrication

The process flow for MuGFET fabrication is summarized in Fig. 4.6. Fig. 4.7 illustrates the key process steps. P-type Zn-doped (100)-oriented InP wafers with doping concentration N_A of 1 × 10^{18} cm^{-3} were used as starting substrates. A 1 µm thick Be-doped $In_{0.55}Ga_{0.45}As$ retrograde well with N_A of 5 × 10^{17} cm^{-3} and ~16 nm $In_{0.7}Ga_{0.3}As$ channel with a lower N_A of 1 × 10^{16} cm^{-3} were sequentially grown by molecular beam epitaxy (MBE) on the InP substrates. During the MBE process, the substrate temperature was 480-490 ºC and base pressure was 7–8×10^{-8} Torr. The fluxes of In, Ga, and As are 1.10×10^{-7}, 5.08×10^{-8}, and 1.00×10^{-5} Torr, respectively, giving a growth rate of 3.08 Å/s for the $In_{0.55}Ga_{0.45}As$ retrograde well. The cell temperature of Be was 830 ºC. During epitaxy of $In_{0.7}Ga_{0.3}As$ channel, the fluxes of In, Ga, and As are 1.90×10^{-7}, 5.08×10^{-8}, and 1.00×10^{-5} Torr, respectively, with the cell temperature of Be at 765 ºC. High-resolution X-ray diffraction (HRXRD) was employed to confirm the composition of the InGaAs layers (Fig. 4.8). Fig. 4.9 shows the vertical profile of Be dopants in the InGaAs epilayers. The high Be concentration at the surface is an artefact. The heavily-doped $In_{0.55}Ga_{0.45}As$ retrograde well is designed to minimize punchthrough effect and provide superior control of SCEs.

A 25 nm thick screen SiO_2 layer was first deposited, followed by formation of dummy photoresist gate pattern to define the source/drain (S/D) regions. Si^+ was then implanted at a dose of 1 × 10^{14} cm^{-2} and an energy of 30 keV. This defines the channel length L_{CH}. The dummy photoresist gate pattern was then removed. Fin lithography was then performed before a Cl_2-based plasma etch to define the InGaAs fins with a fin height H_{Fin} of 100 nm.

This removed the N^+ regions surrounding the fins. This was followed by dopant activation (600 ºC for 60 s) in N_2 ambient.

After pre-gate clean comprising sequential treatment in dilute H_2SO_4:H_2O_2:H_2O, HCl, NH_4OH, and $(NH_4)_2S$, the wafers were loaded into a multiple-chamber gate cluster system for vacuum baking, SiH_4+NH_3 passivation and MOCVD deposition of HfAlO (19 nm). CF_4 treatment and post-gate dielectric deposition anneal (PDA) at 500 ºC for 60 s were performed prior to reactive sputter deposition and patterning of TaN gate electrode. Low resistance CMOS-compatible PdGe contacts were finally integrated.

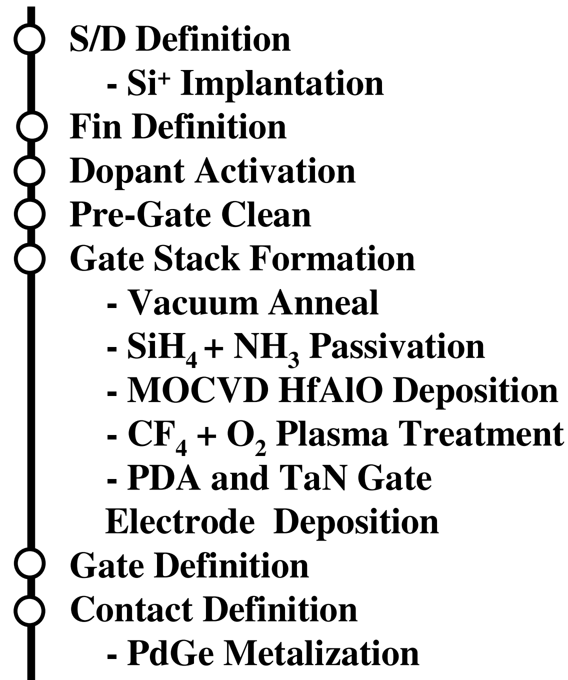
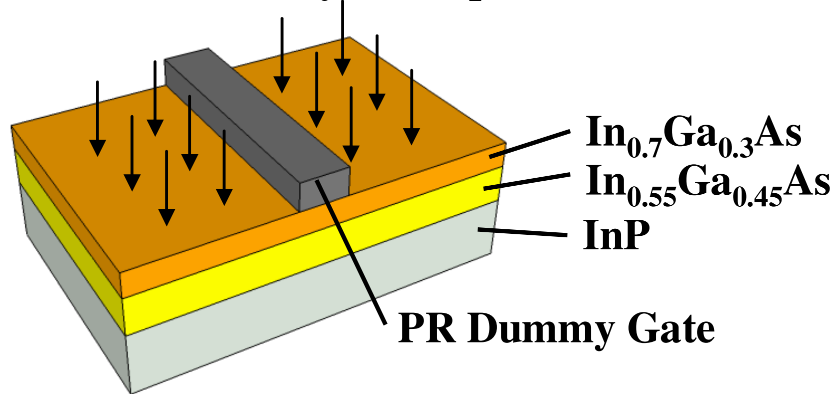
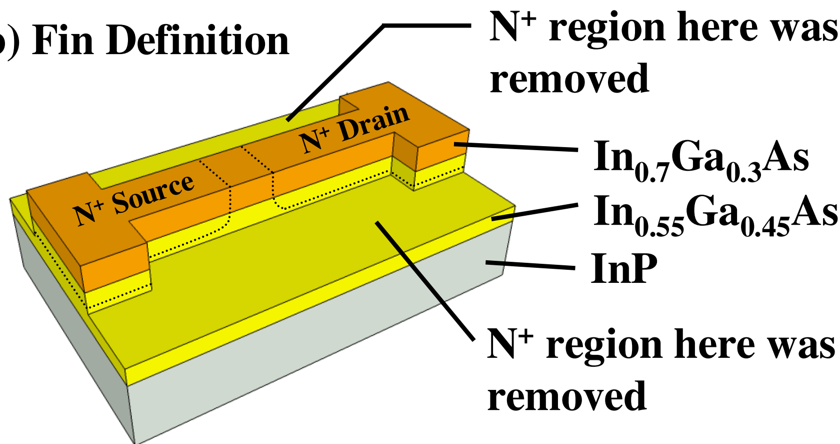


Fig. 4.6 Process sequence employed in transistor fabrication. A gate last fabrication approach was used in this device demonstration.





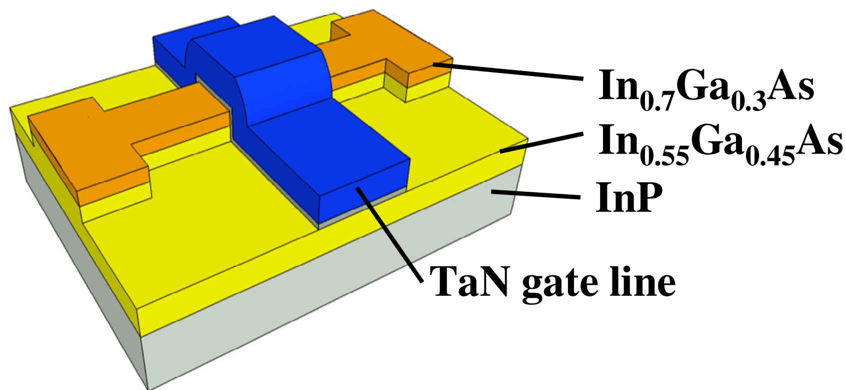


Fig. 4.7 Schematic illustration of the key process steps in the MuGFET fabrication. (a) Dummy photo resist (PR) gate pattern was used to define the S/D regions during Si^+ implantation. (b) Fin lithography was then performed before a Cl_2-based plasma etch to define the InGaAs fins with a H_{Fin} of 100 nm. This also removed the N^+ regions surrounding the fins. (c) After surface passivation and high-k dielectric deposition, TaN metal gate was reactively sputtered and patterned.

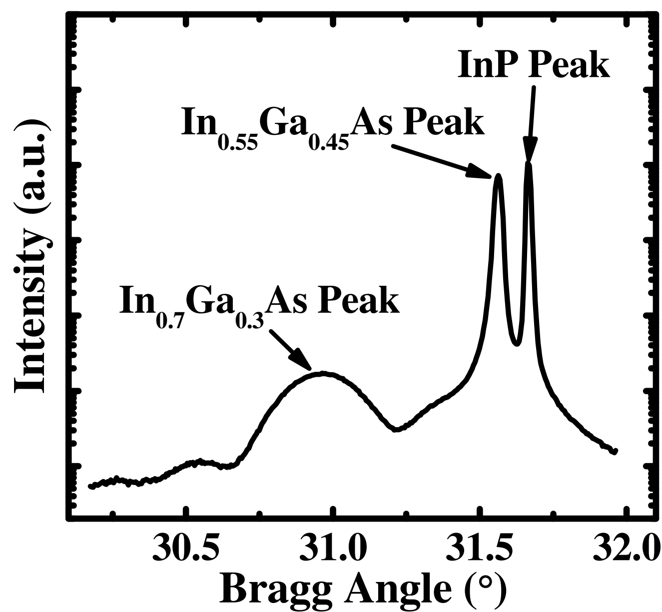


Fig. 4.8 HRXRD shows well-defined $In_{0.7}Ga_{0.3}As$ and $In_{0.55}Ga_{0.45}As$ peaks, indicating high crystalline quality of the epilayers.

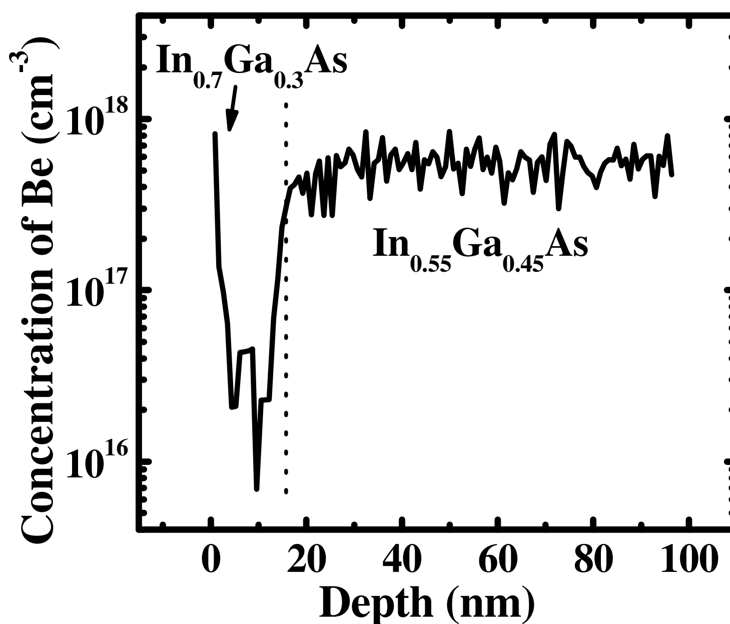


Fig. 4.9 SIMS profile reveals the elemental distribution of Be in the $In_{0.7}Ga_{0.3}As/In_{0.55}Ga_{0.45}As$ stack. The high Be concentration at the surface is an artefact.

4.4 Device Characterization and Analysis

Fig. 4.10(a) shows the top view Scanning Electron Microscopy (SEM) image of a completed InGaAs MuGFET with TaN gate line, $In_{0.7}Ga_{0.3}As$ fin and PdGe ohmic contacts. Transmission Electron Microscopy (TEM) image in Fig. 4.10(b) shows the cross-sectional view of the InGaAs MuGFET along line A-A', as indicated in Fig. 4.10(a). The thickness of $In_{0.7}Ga_{0.3}As$ layer is about 16 nm. The $In_{0.7}Ga_{0.3}As$ surface appears rough, and the roughening could be strain-induced as the thickness of $In_{0.7}Ga_{0.3}As$ is close to its critical thickness. A similar phenomenon in strained-layer epitaxy of InGaAs has also been reported [4.10]. TEM micrograph in Fig. 4.10(c) shows the fin structure along B-B', as indicated in Fig. 4.10(a). The InGaAs fin structure has a W_{Fin} of 220 nm and H_{Fin} of 100 nm.

Fig. 4.11 plots the I_D–V_G transfer characteristics of $In_{0.7}Ga_{0.3}As$ N-MuGFET with W_{Fin} of 220 nm in the linear (V_D = 100 mV) and saturation (V_D = 1.2 V) regions. L_{CH} is 130 nm. The I_{DS} is normalized by $W_{Fin} + 2 \times H_{Fin}$. With a multiple-gate architecture for better electrostatic control and a retrograde-doped fin for suppression of sub-surface punchthrough, SCEs in the channel region are well-controlled. The DIBL is 135 mV/V, which is very small considering that the physical thickness of the HfAlO dielectric is 19 nm. Subthreshold swing (SS) of the MuGFET is 230 mV/decade, which is indicative of a poor interface quality, and can be reduced by improving the surface passivation process and by reducing the EOT.

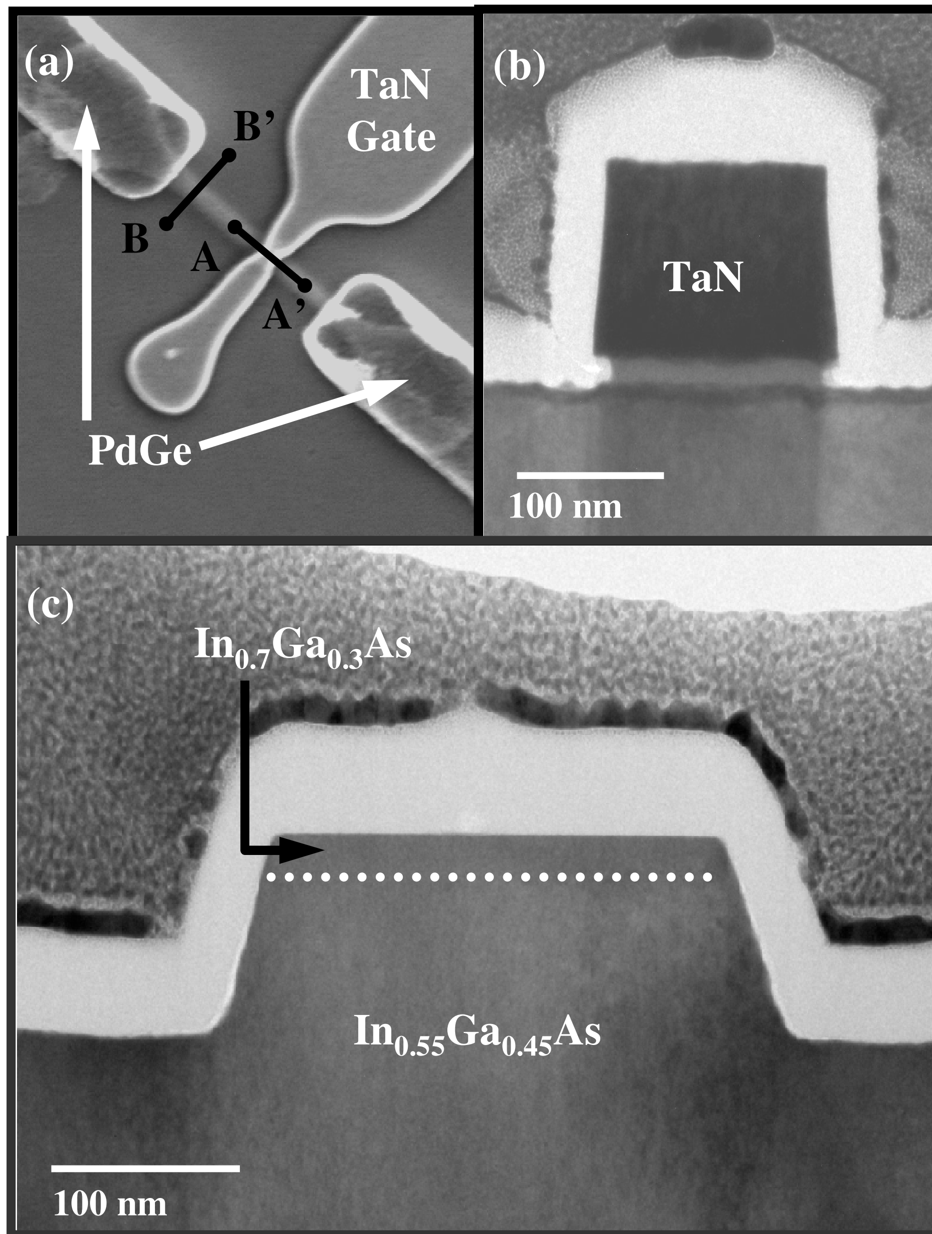


Fig. 4.10 (a) SEM image shows the top view of a fabricated MuGFET with TaN gate electrode, $In_{0.7}Ga_{0.3}As$ channel and PdGe ohmic contacts. (b) TEM micrograph showing the cross-sectional view of the InGaAs MOSFET along A-A', as indicated in the SEM image in (a). (c) TEM micrograph showing the cross-sectional view of the InGaAs fin structure along B-B', as indicated in (a). The InGaAs fin structure has a W_{Fin} of 220 nm and H_{Fin} of 100 nm.

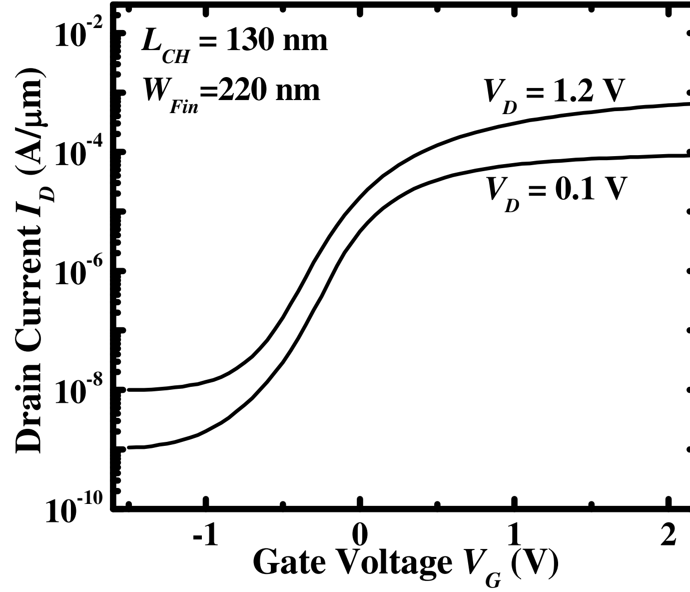


Fig. 4.11 I_D–V_G transfer characteristics of $In_{0.7}Ga_{0.3}As$ N-MuGFET with retrograde p-type $In_{0.55}Ga_{0.45}As$ fin.

I_D-V_D output characteristics are plotted in Fig. 4.12. Despite the relatively thick gate dielectric (19 nm of HfAlO), the InGaAs MuGFET demonstrates I_{Dsat} exceeding 850 μA/μm at V_{DS} of 2 V and $V_G - V_T$ of 3 V. This is partly due to the multiple-gate structure that contributes to suppressed DIBL and relaxation of the gate oxide thickness requirement. Further improvement in I_{Dsat} and DIBL can be realized through reduction of the EOT and further improvement in surface passivation. Parasitic S/D series resistance R_{SD} of the InGaAs FETs is ~ 1 kΩ-μm, which is similar to Ref. [4.9] and [4.11]. The R_{SD} is higher than HEMT structure as reported in Ref. [4.12]. This is related to low S/D doping concentration by implantation technique and integration of non-self-aligned ohmic contacts. R_{SD} has to be reduced to derive more performance benefits from enhanced carrier transport in the high mobility channel. In addition, the low S/D junction leakage is attributed to the low S/D implant dose of 1×10^{14} cm^{-2}, which reduces crystal damage.

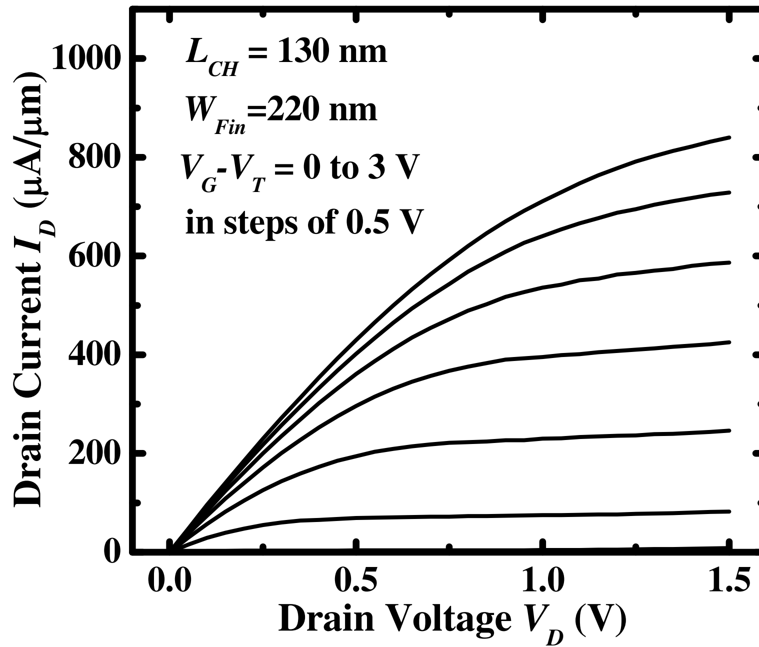


Fig. 4.12 I_D–V_D output characteristics of the InGaAs N-MuGFET in Fig. 4.11.

Fig. 4.13 shows DIBL of MuGFETs with various W_{Fin} at a fixed L_{CH} of 130 nm. DIBL is reduced with decreasing W_{Fin}, indicating better control of SCEs in the multiple-gate structure. Similar improvement in SCEs of MuGFETs with similar W_{Fin} was also reported by other groups [4.13], [4.14]. Further improvement in DIBL is expected through scaling of W_{Fin}. Fig. 4.14 shows that the DIBL of the devices is a weak function of L_{CH}, showing reasonable control of SCEs due to the multiple-gate structure and retrograde channel doping.

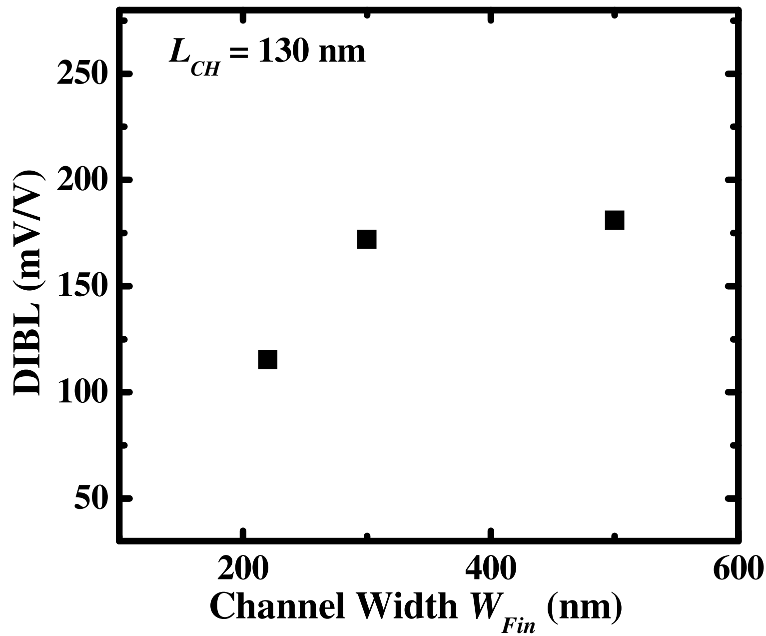


Fig. 4.13 DIBL versus channel width of the InGaAs transistors with retrograde channel doping. DIBL decreases with the reduction of channel width, indicating improved electrostatic control of the channel.

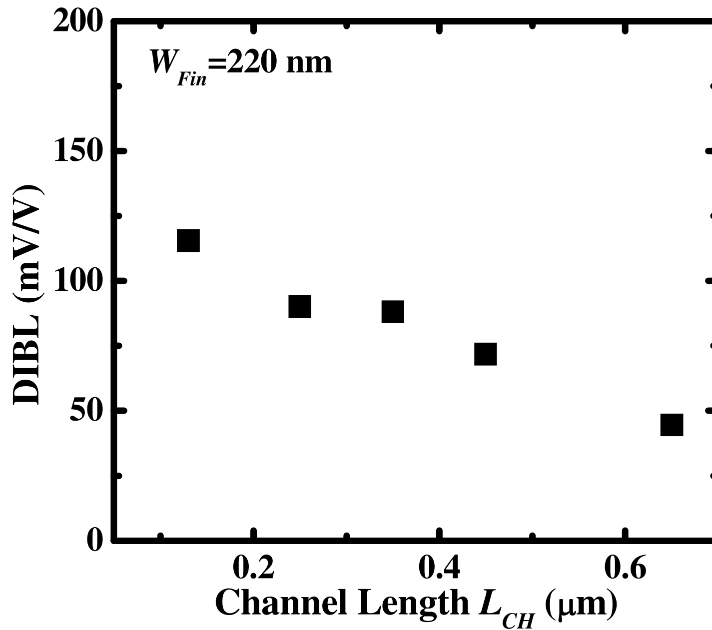


Fig. 4.14 DIBL of $In_{0.7}Ga_{0.3}As$ N-MuGFETs with retrograde doping as a function of L_{CH}.

4.5 Summary

In summary, multiple-gate device architecture and retrograde channel doping design were investigated for the improvement of the device performance of III-V channel MOSFETs. A novel III-V N-MuGFET with lightly-doped high mobility $In_{0.7}Ga_{0.3}As$ channel and epi-controlled retrograde-doped fin was fabricated for this technology demonstration. Through device simulations, it has been verified that the additional retrograde channel doping gives rise to improved control of SCEs. In addition, the electrical results further confirmed the significant improvement in SCEs, such as V_t roll-off and DIBL, which was realized by using the multiple-gate structure, as compared to the planar MOSFET. The $In_{0.7}Ga_{0.3}As$ N-MuGFETs demonstrate good electrical performance, showing DIBL of 135 mV/V, and I_{Dsat} exceeding 840 μA/μm at V_D of 1.5 V and $V_G - V_T$ of 3 V. The device architecture investigated in this chapter is very promising for achieving very high carrier mobility and improved short-channel effects in aggressively scaled III-V transistors.

4.6 References

[4.1] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, “FinFET–A self-aligned double-gate MOSFET scalable to 20 nm,” *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2320–2325, 2000.

[4.2] Yang-Kyu Choi, Tsu-Jae King, and Chenming Hu, “Nanoscale CMOS spacer FinFET for the Terabit era,” *IEEE Electron Device Lett.*, vol. 23, no. 1, pp. 25–27, 2002.

[4.3] J. Kedzierski, E. Nowak, T. Kanarsky, Y. Zhang, D. Boyd, R. Carruthers, C. Cabral, R. Amos, C. Lavoie, R. Roy, J. Newbury, E. Sullivan, J. Benedict, P. Saunders, K. Wong, D. Canaperi, M. Krishnan, K.-L. Lee, B. A. Rainey, D. Fried, P. Cottrell, H.-S.P. Wong, M. Ieong, W. Haensch, “Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation,” in *IEDM Tech. Dig.*, 2002, pp. 247–250.

[4.4] H. Shang, L. Chang, X. Wang, M. Rooks, Y. Zhang, B. To, K. Babich, G. Totir, Y. Sun, E. Kiewra, M. Ieong, W. Haensch, “Investigation of FinFET devices for 32 nm technologies and beyond,” in *VLSI Symp. Tech. Dig.*, 2006, pp. 66–67.

[4.5] T.-Y. Yang, K.-M. Tan, R. T. P. Lee, A. Du, C.-H. Tung, G. S. Samudra, W. J. Yoo, N. Balasubramanian, and Y.-C. Yeo, “Strained n-channel FinFETs with 25 nm gate length and silicon-carbon source/drain regions for performance enhancement,” in *VLSI Symp. Tech. Dig.*, 2006, pp. 68–69.

[4.6] A. Kaneko, A. Yagishita, K. Yahashi, T. Kubota, M. Omura, K. Matsuo, I. Mizushima, K. Okano, H. Kawasaki, T. Izumida, T. Kanemura, N. Aoki, A. Kinoshita, J. Koga, S. Inaba, K. Ishimaru, Y. Toyoshima, H. Ishiuchi, K. Suguro, K. Eguchi, and Y. Tsunashima, "High-performance FinFET with dopant-segregated Schottky source/drain," in *IEDM Tech. Dig.*, pp. 893–896, 2006.

[4.7] M. Guillorn, J. Chang, A. Bryant, N. Fuller, O. Dokumaci, X. Wang, J. Newbury, K. Babich, J. Ott, B. Haran, R. Yu, C. Lavoie, D. Klaus, Y. Zhang, E. Sikorski, W. Graham, B. To, M. Lofaro, J. Tornello, D. Koli, B. Yang, A. Pyzyna, D. Neumeyer, M. Khater, A. Yagishita, H. Kawasaki, and W. Haensch, "FinFET performance advantage at 22nm: An AC perspective," in *VLSI Symp. Tech. Dig.*, 2008, pp. 12–13.

[4.8] N. Collaert, A. De Keersgieter, A. Dixit, I. Ferain, L. –S. Lai, D. Lenoble, A. Mercha, A. Nackaerts, B. J. Pawlak, R. Rooyackers, T. Schulz, K. T. San, N. J. Son, M. J. H. Van Dal, P. Verheyen, K. von Arnim, L. Witters, K. De Meyer, S. Biesemans, M. Jurczak, "Multi-gate devices for the 32 nm technology node and beyond," *Solid-State Electronics*, vol. 52, pp. 1291–1296, 2008.

[4.9] Y. Q. Wu, R. S. Wang, T. Shen, J. J. Gu and P. D. Ye, "First experimental demonstration of 100 nm Inversion-mode InGaAs FinFET through damage-free sidewall etching," in *IEDM Tech. Dig.*, 2009, pp. 331–334.

[4.10] S. F. Yoon, "Growth of strained InGaAs/GaAs by molecular beam epitaxy: a surface morphology, Raman spectroscopy and

photoluminescence combined study," *Appl. Surf. Sci.*, vol. 78, no. 1, pp. 33–39, 1994.

[4.11] Y. Xuan, T. Shen, M. Xu, Y. Q. Wu, and P. D. Ye, "High-performance surface channel In-rich $In_{0.75}Ga_{0.25}As$ MOSFETs with ALD high-*k* as gate dielectric," in *IEDM Tech. Dig.*, 2008, pp. 371–374.

[4.12] M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and R. Chau, "Advanced high-*k* gate dielectric for high-performance short-channel $In_{0.7}Ga_{0.3}As$ quantum well field effect transistors on silicon substrate for low power logic applications," in *IEDM Tech. Dig.*, 2009, pp. 319–322.

[4.13] K. Hieda, F. Horiguchi, H. Watanabe, K. Sunouchi, I. Inoue, and T. Hamamoto, "New effects of trench isolated transistor using side-wall gates," in *IEDM Tech. Dig.*, 1987, pp. 736–739.

[4.14] D. Hisamoto, T. Kaga, Y. Kawamoto, and E. Takeda, "A fully depleted lean-channel transistor (DELTA)-a novel vertical ultra thin SOI MOSFET," in *IEDM Tech. Dig.*, 1989, pp. 833–836.

Chapter 5

Nanoheteroepitaxy of Gallium Arsenide on Strain-Compliant Silicon-Germanium Nanowires

5.1 Introduction

Heterogeneous integration of III-V compound semiconductors such as gallium arsenide (GaAs) on silicon (Si) substrates would enable the fabrication of high-speed transistors and optoelectronic devices on a Si platform and the realization of enhanced functionalities in integrated electronics. Tremendous research effort has been made to integrate GaAs on Si, including direct growth on Si islands [5.1], flip-chip bonding [5.2]-[5.3], insertion of a silicon-germanium (SiGe) graded buffer layer [5.4]-[5.5], and selective aspect ratio trapping (ART) method [5.6]. Antiphase domains (APDs) which typically form during the growth of polar III-V materials on non-polar materials, such as Si, have to be effectively suppressed. In addition, huge differences in lattice constant of ~ 4.1 % and thermal expansion coefficient of ~ 110 % between GaAs and Si impose immense challenges for direct integration of GaAs on Si. Use of compliant substrates may be an attractive approach to achieve dislocation-free heterostructure [5.1], [5.7]-[5.8]. Additional stress relief mechanisms in compliant substrate can significantly reduce the strain

energy in the compound semiconductor epilayer, increase the critical thickness, and facilitate the integration of lattice-mismatched materials.

In this chapter, a new method of forming GaAs on a Si-based substrate through selective migration-enhanced epitaxy (MEE) of GaAs on strain-compliant SiGe nanowire structures was reported. The physics of compliance in nanoscale heterostructures is exploited for accommodating strain at the GaAs-SiGe interface. The nanowire structure adopted here provides additional stress relief, as compared to the growth on planar structures, due to the substrate compliance effect or distribution of strain energy between the GaAs layer and the SiGe nanowire. $Si_{0.35}Ge_{0.65}$ nanowires formed by the germanium (Ge) condensation process [5.9] were employed as template for GaAs growth. The need for thick (> 1 μm) lattice-matched Ge buffer layer, expensive bulk III-V wafers for layer transfer, or chemical mechanical polishing (CMP) process steps was eliminated.

The fabrication process employed in the hetero-integration is first described in Section 5.2. Extensive finite element simulations and material characterization, including scanning electron microscopy (SEM), cross-sectional transmission electron microscopy (TEM), photoluminescence (PL), micro-Raman spectroscopy, and Auger electron spectroscopy, are discussed in Section 5.3. Section 5.4 summarizes the key achievements attained in this work.

5.2 Experiment

The starting materials were silicon-on-insulator (SOI) substrates with ~ 15 nm of (001) Si on 140 nm of buried oxide (BOX). A $Si_{0.85}Ge_{0.15}$ layer was

pseudomorphically grown by ultra-high vacuum chemical vapor deposition (UHVCVD) on the Si surface. The growth was carried out at 580 °C using disilane (Si_2H_6) and germane (GeH_4) as precursors. Schematics in Fig. 5.1 illustrate the two-stage Ge condensation process for the formation of silicon-germanium-on-insulator (SGOI) substrates. The wafer was oxidized in dry oxygen ambient. The first stage of the oxidation was carried out at 1050 °C, after which the temperature was ramped down to 900 °C for second stage of condensation in order to stay within the solidus curve of the Si–Ge phase diagram [5.10]. The oxidation of SiGe forms SiO_2 preferentially, due to the difference in the heats of formation between SiO_2 and GeO_2 [5.11]. The Ge atoms, which are rejected during the oxidation, pile up at the SiGe-oxide interface, leading to the formation of enriched SiGe alloy [5.12]. Ge atoms are thus condensed in the SiGe layer, as the out-diffusion of Ge is prohibited by the top and bottom SiO_2 layers. Oxidation at 1050 °C enables substantial diffusion of Ge atoms to maintain uniform distribution of Ge in the SGOI layer due to the large diffusion length of Ge (l_{Ge}), which is given by

$$l_{\mathrm{Ge}}=2\sqrt{Dt} \quad (5\text{-}1)$$

where D is diffusion coefficient [5.13], and t is the oxidation time. However, in the second oxidation stage where the concentration of Ge is relatively high, the oxidation temperature has to be reduced to below the melting point of SiGe at the highest targeted Ge concentration. Oxidation at a lower temperature of 900 °C leads to l_{Ge} of 5.06 nm, which is smaller than the final SiGe layer thickness, and this increases the potential of large strain levels to be built up due to the accumulation or pileup of Ge near the top SiO_2 region. Therefore, the annealing step at 900 °C in nitrogen ambient serves to

redistribute the Ge atoms in all directions, *i.e.* downwards and laterally. Oxidation continues after the Ge redistribution step. The intermittent redistribution of Ge atoms in the SGOI layer in between oxidation steps will minimize the pile up of Ge.

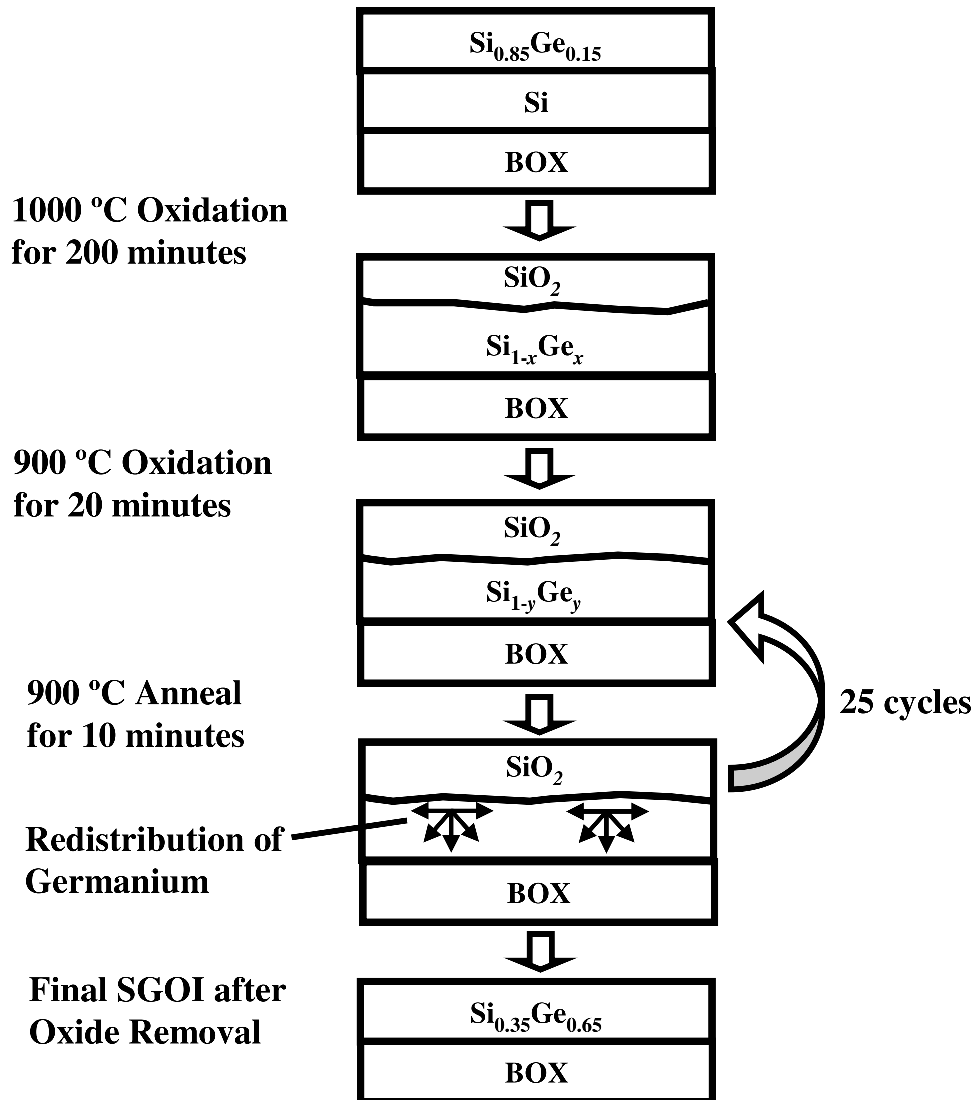


Fig. 5.1 Schematic illustrating the process flow for the fabrication of SGOI substrate using two-steps Ge condensation process at 1050 °C and 900 °C. Cyclical oxidation and annealing performed at 900 °C serve to improve the distribution of the Ge in the SiGe layer.

SEM images in Fig. 5.2(a) and (b) show the top view of SiGe surface after the Ge condensation process with and without this cyclical process, respectively. Significant improvement in the surface morphology was achieved by introducing the cyclical oxidation and annealing at 900 °C. High resolution X-ray diffraction (XRD) was employed to investigate the composition of Ge in the SiGe layer. Fig. 5.3 shows the high resolution rocking curve of the (004) reflection from the SGOI substrate. The composition of Ge incorporated in the SiGe layer was determined to be 65 %. Atomic force microscopy (AFM) analysis was also carried out to investigate the surface morphology of the SiGe layer. Fig. 5.4 shows the AFM image of the surface of a completed SGOI substrate. Low root-mean-square (RMS) roughness of ~0.44 nm was achieved by using the two-stage Ge condensation process.

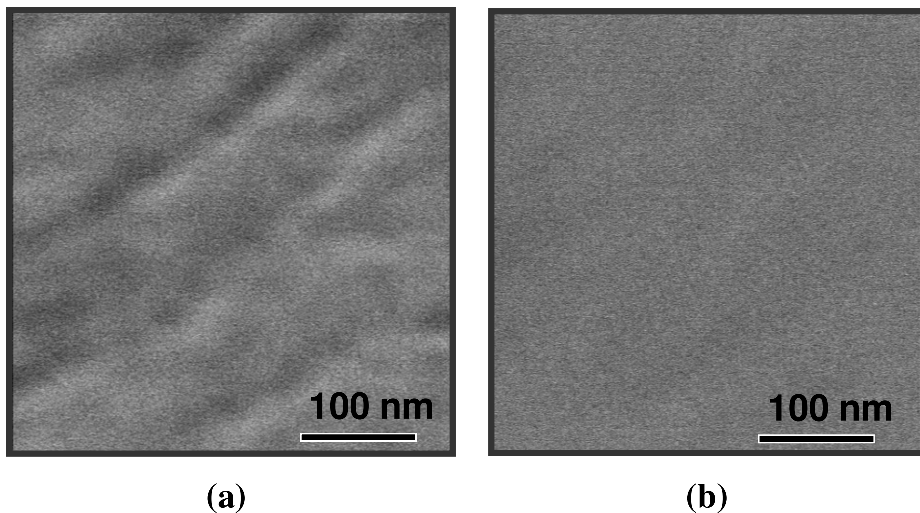


Fig. 5.2 SEM top view of the SiGe layer formed by Ge condenstation process (a) without, (b) with second stage of cyclical oxidation and annealing at 900 °C. The cyclical step significantly improves the surface morphology.

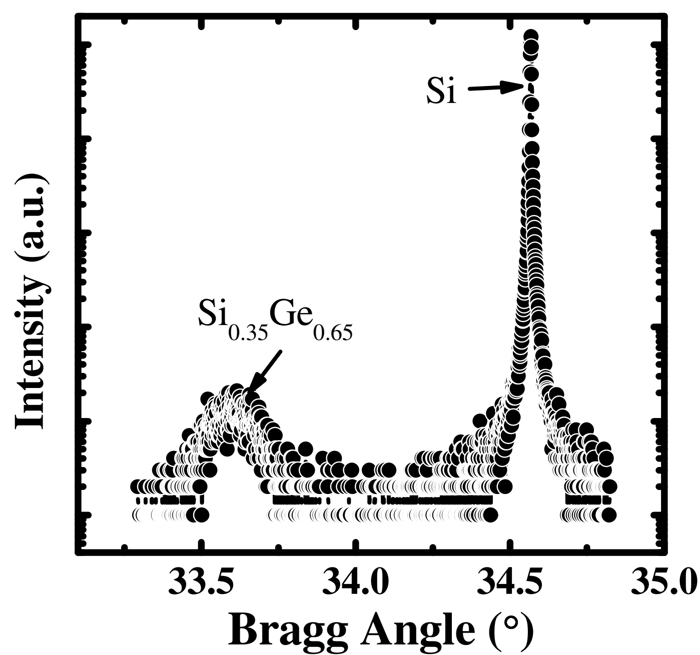


Fig. 5.3 The well-defined SiGe peak in the high resolution XRD indicates high crystalline quality of the SiGe layer. The composition of Ge in the SiGe layer was determined to be ~65 %.

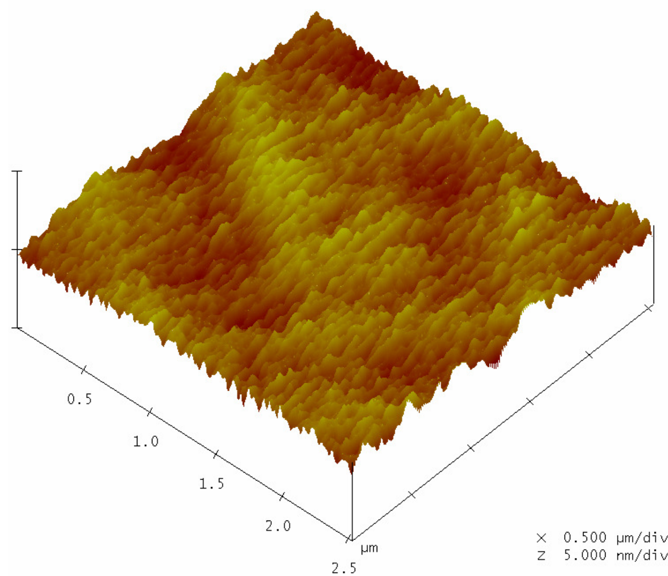


Fig. 5.4 AFM surface scanning of a completed SGOI substrate after oxide removal. The SGOI substrate exhibits low RMS roughness of ~0.44 nm.

Photolithography and dry etching were then used to define SiGe nanowires as well as large SiGe planar structures or pads on SiO_2. After native oxide removal in HF solution, the samples were immediately loaded into a molecular beam epitaxy (MBE) system. The MBE epitaxy was carried out in collaboration with research team from Nanyang Technological University. *In-situ* thermal annealing at 600 °C for 10 minutes was carried out to drive off water vapour in the transfer chamber. The pressure in the transfer chamber is ~ 9×10^{-10} Torr. Subsequently, the sample was loaded into the growth chamber and a second annealing step at 850 ^{o}C for 5 min under a background vacuum level of 10^{-8} Torr was conducted to further desorb any remaining native oxide on the SiGe surface and to form double atomic steps on the SiGe surface necessary for the suppression of anti-phase domain-related defects, as shown in the typical (2×2) reflection high-energy electron diffraction pattern [5.14]-[5.15]. High temperature annealing of vicinal (001) Ge and Si surfaces has been observed to produce a single-domain, double atomic-height stepped surface, *i.e.* the dimer rows run perpendicular to the step edges and the dimer bonds are parallel to the step edges [5.14]-[5.15].

The selective GaAs growth consists of two epitaxy steps: MEE process right after the *in-situ* thermal annealing step, followed by a standard GaAs MBE growth process. Fig. 5.5 shows the cross-sectional TEM images of epitaxy growth at temperatures of (a) 525 °C, (b) 580 °C, and (c) 625 °C. When growth temperature is low, Fig. 5.5(a) shows the growth selectivity over SiO_2 was not achieved. The GaAs crystals on SiO_2 are polycrystalline, as confirmed by the diffractogram in the inset of Fig. 5.5(a). The growth temperature was increased to 580 °C to enable the desorption of nucleated

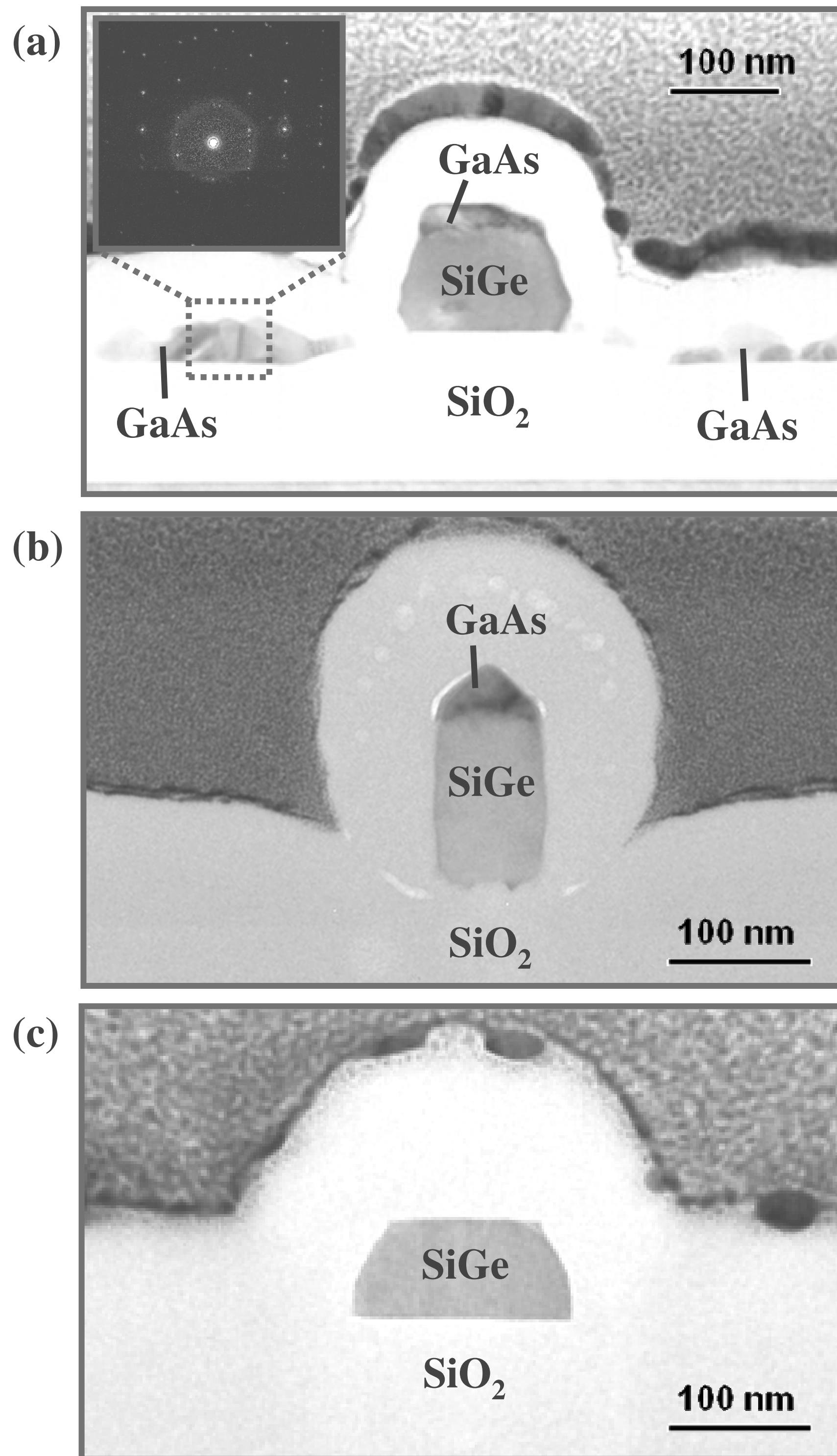


Fig. 5.5 TEM images showing film quality and growth selectivity under different epitaxy temperatures at (a) 525 °C, (b) 580 °C, and (c) 625 °C. Higher temperature enables the desorption of nucleated seeds on the SiO_2 to achieve selective growth. Diffractogram in the inset of (a) reveals that the GaAs grown on SiO_2 is polycrystalline.

seeds on SiO_2 regions for achieving high growth selectivity, as illustrated in Fig. 5.5(b). However, when growth temperature is increased to 625 °C, GaAs was not observed on both SiGe and SiO_2 regions [Fig. 5.5(c)]. This is attributed to high desorption rate of Ga and As seeds from both SiGe and SiO_2 regions.

The MEE process was performed by alternating the As and Ga shutter opening and closing cycles, each with 3 s opening time [5.16]. A 3 s growth interruption was inserted following each Ga and As shutter opening and closing cycle to provide sufficient time for each type of adatoms to form a complete monolayer covering the substrate surface before bonding occurs. This layer-by-layer growth mode achieved in MEE process affects the relaxation mechanism of the epitaxial layer. The Ga beam equivalent pressure (BEP) is is ~6×10^{-8} Torr, which was determined by ion gauge facing the Ga source. The As/Ga BEP ratio during this process was set at 30. The shutter opening time has been optimized to supply enough Ga and As adatoms to complete a monolayer of 2.83 Å growth during each cycle. The MEE process was repeated for ten cycles, corresponding to the growth of 10 monolayers (MLs) of GaAs. Subsequently, a standard GaAs MBE growth process was used to grow the remaining GaAs layer.

5.3 Device Characterization and Analysis

5.3.1 Compliance in Nanostructures and Simulation

The difference in lattice constant between GaAs and $Si_{0.35}Ge_{0.65}$ is 1.48 %. When GaAs is epitaxially grown on SiGe such that pseudomorphic growth is achieved, the lattice of GaAs is compressed horizontally due to the 1.48 %

lattice mismatch. In a large planar SiGe-on-insulator structure with limited or no substrate compliance, the GaAs epilayer is biaxially strained or deformed, as shown in Fig. 5.6(a), while the SiGe layer remains relaxed. Lattice interactions at the heterojunction between GaAs and SiGe in a planar SiGe-on-insulator structure are highlighted in Fig. 5.6(b). The critical thickness of the strained GaAs epilayer is limited by the level of stress energy that can be accumulated without defect formation.

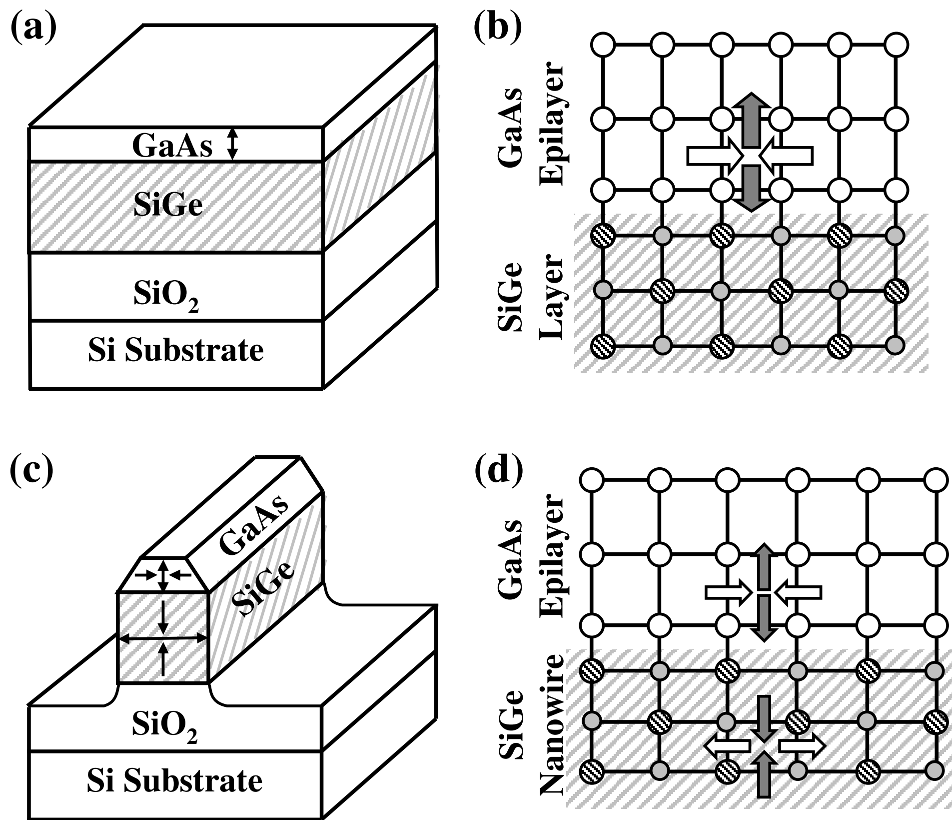


Fig. 5.6 (a) When a GaAs layer is grown on a planar SiGe layer or a large SiGe island with limited or no compliance, the GaAs epilayer is deformed or strained, whereas the SiGe layer is relaxed. In this case, as shown in (b), a high level of strain energy is stored in the GaAs epilayer as lateral compression and vertical tension. (c) The substrate compliance effect in SiGe nanowire structure enables both the nanowire and the epilayer to be deformed. The mismatched strain energy is thus distributed between the epilayer and nanowire, as shown in (d). The reduced strain energy accumulated in the epilayer suppresses the formation of defects.

As compared to the planar structure, additional stress relief mechanisms are available in a nanowire structure during heteroepitaxy, as illustrated in Fig. 5.6(c). Both the nanowire and the epilayer can deform laterally and vertically [Fig. 5.6(d)]. Thus, the strain energy due to lattice mismatch between the epilayer and the nanowire can be distributed in both materials. This substrate compliance effect reduces the amount of strain energy in the epilayer and enables the GaAs epilayer to remain coherent beyond the critical thickness that is characteristic of heteroepitaxy.

The physics of lattice interactions at the heterojunction of two nanostructured materials can be captured using a finite-element method [5.17]. The Young's modulus of 85.5 GPa and 111 GPa are used in the simulation for GaAs and SiGe, respectively. The Poisson's ratio of GaAs and SiGe are 0.31 and 0.266, respectively. Fig. 5.7(a) and 5.7(b) show the simulated lateral strain ε_x and vertical strain ε_y profile of GaAs/$Si_{0.35}Ge_{0.65}$ heterostuctures with width W of 100 nm, respectively. The thicknesses of GaAs and $Si_{0.35}Ge_{0.65}$ are 20 nm and 100 nm, respectively. In the GaAs region, the lateral strain ε_x is compressive (negative), and the vertical strain ε_y is tensile (positive). Conversely, in the SiGe nanowire region, ε_x is tensile and ε_y is compressive. The magnitude of ε_x is the highest at the heterojunction and decreases away from the heterojunction. The vertical strain ε_y in the SiGe nanowire region behaves similarly and is compressive in nature. The simulated lateral strain ε_x and vertical strain ε_y profile at the centre of GaAs/$Si_{0.35}Ge_{0.65}$ heterostuctures with W of 1 μm are shown in Fig. 5.8(a) and 5.8(b), respectively. Both ε_x and vertical strain ε_y are higher in magnitude than the heterostructure with W of 100 nm. The lateral strain ε_x and vertical strain ε_y components in the

$GaAs/Si_{0.35}Ge_{0.65}$ heterostuctures are plotted as a function of the depth *y* from the GaAs surface [Fig. 5.9(a) and 5.9(b)]. The *W* of the nanowire is varied from 100 nm to 2 μm. The compliance effect is larger for a narrower SiGe nanowire. It can be observed that the strain components in GaAs decrease in magnitude as *W* becomes smaller. In fact, for a 100 nm wide nanostructure, the GaAs is almost strain-free at the top surface.

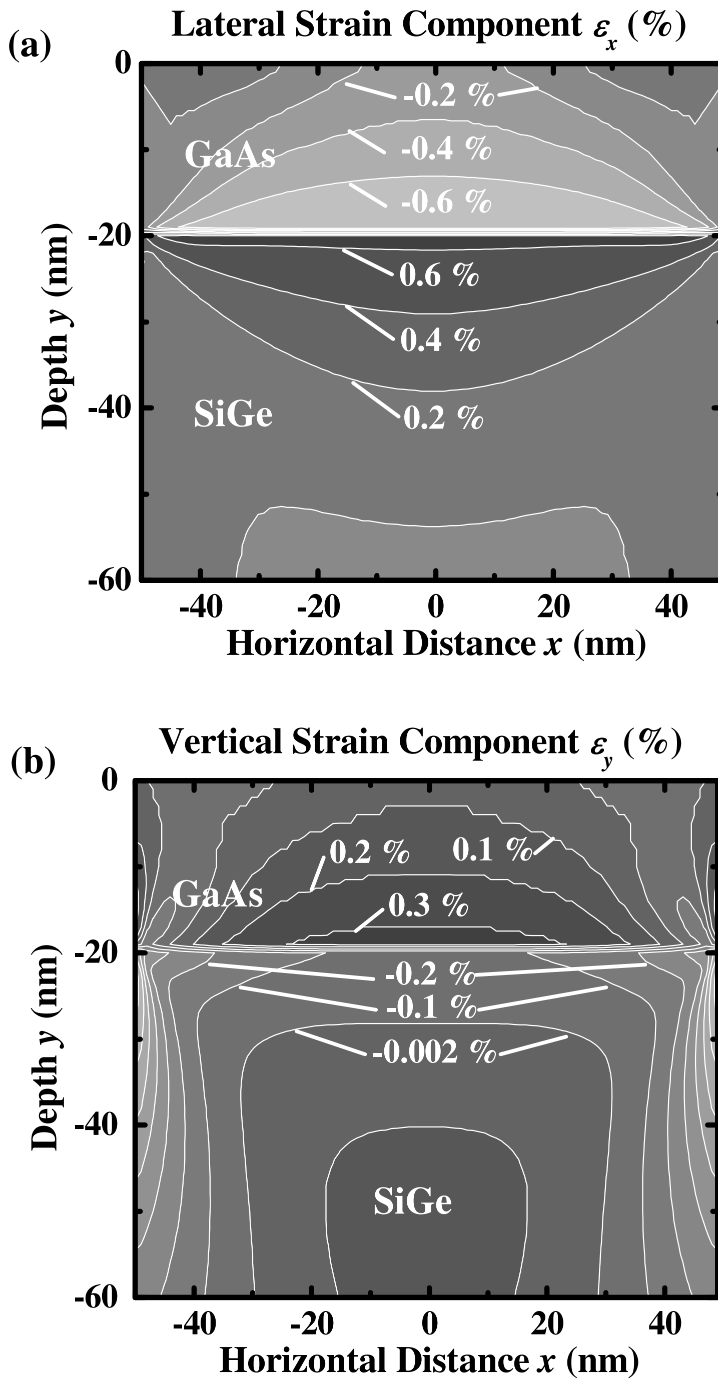


Fig. 5.7 Finite element simulation obtained the distribution of (a) lateral strain ε_x and (b) vertical strain ε_y in the GaAs/$Si_{0.35}Ge_{0.65}$ heterostructure with W of 100 nm. The magnitude of ε_x and ε_y is the highest at the heterojunction and decreases away from the heterojunction.

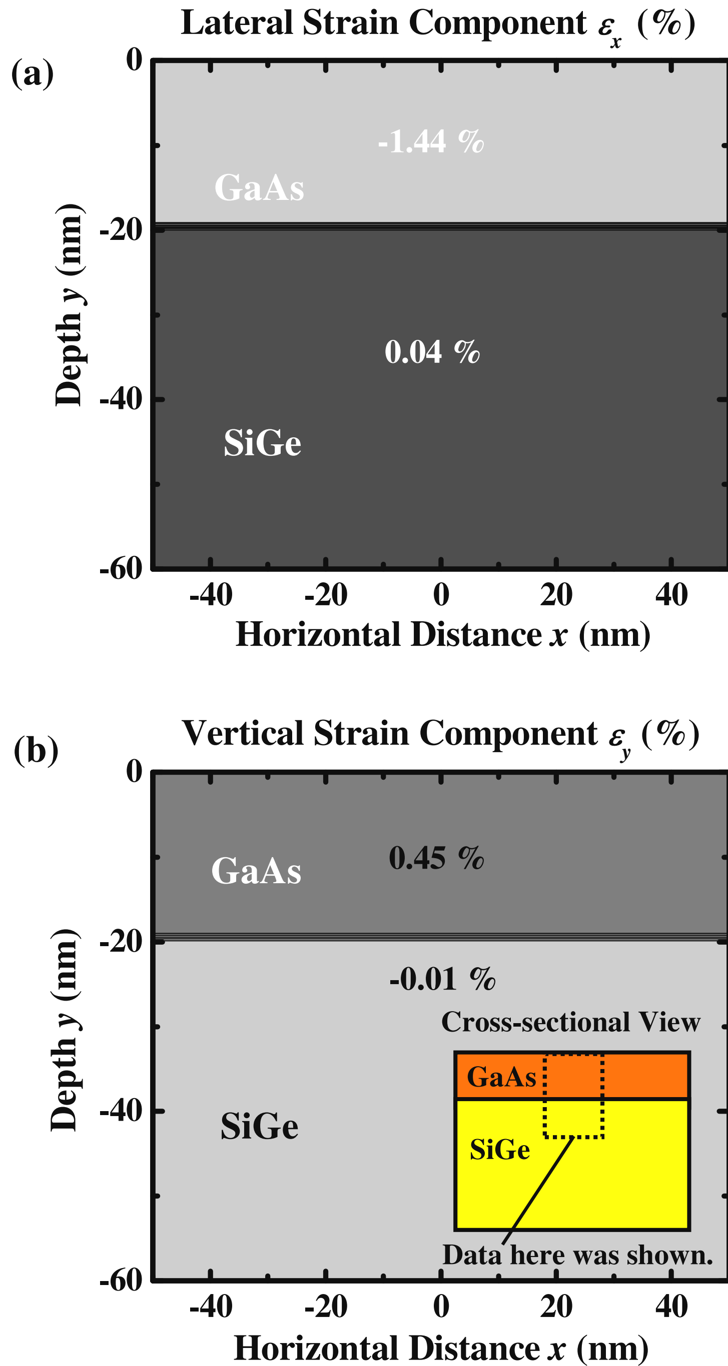


Fig. 5.8 Finite element simulation obtained the distribution of (a) lateral strain ε_x and (b) vertical strain ε_y in the GaAs/$Si_{0.35}Ge_{0.65}$ heterostructure with W of 1 μm. Both ε_x and ε_y are larger than the structure with W of 100 nm, as shown in Fig. 5.7. Inset shows the location of the GaAs/$Si_{0.35}Ge_{0.65}$ heterostructure for this analysis.

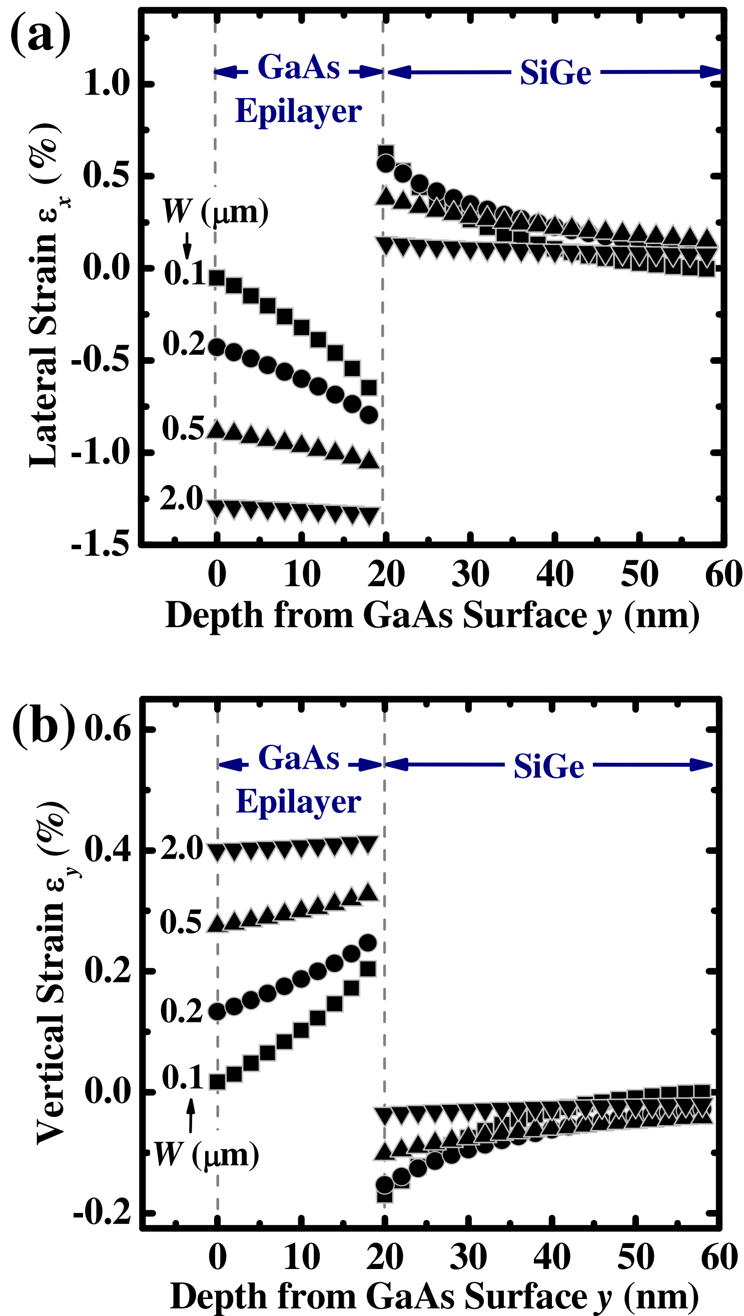


Fig. 5.9 Finite element simulation of (a) lateral strain ε_x and (b) vertical strain ε_y as a function of depth from the GaAs surface y in a GaAs/$Si_{0.35}Ge_{0.65}$ heterostructure formed on SiO_2. The thicknesses of the GaAs and SiGe layers are 20 nm and 100 nm. The width W of GaAs/SiGe nanostructure is varied (100 nm, 200 nm, 500 nm, and 2 μm). The strain in GaAs is significantly reduced for narrower structures.

5.3.2 Growth of Gallium Arsenide on $Si_{0.35}Ge_{0.65}$ Islands or Nanowires

SEM micrograph in Fig. 5.10(a) shows the top view of the GaAs layer grown on a planar $Si_{0.35}Ge_{0.65}$ structure. The surface of the epilayer is rough and filled with many GaAs islands. The islanding is related to the high level of stress built up in the mismatched strained systems [5.18]. The formation of isolated thick islands and interfacial misfit defects reduces total energy in the system as compared to a coherent GaAs/SiGe planar structure. Defects such as stacking faults and dislocations are clearly observed in these GaAs islands and at the interface between GaAs and SiGe, as shown in the cross-sectional TEM images in Fig. 5.10(b) and 5.10(c). These defects relieve the stress accumulated at the GaAs/SiGe heterojunction. Some of the defects are mostly confined in the (111) plane, indicating APDs in nature. The GaAs islanding can be suppressed at lower growth temperature, where the evaporation of As dimers is suppressed and the migration distance of the Ga adatoms is reduced. As a result, two-dimensional (2D) growth mode becomes the dominant mechanism. However, the selectivity of growth on SiGe regions and the crystalline quality of the GaAs layer will be compromised.

Next, the quality of the GaAs epitaxial layer formed on SiGe nanowires is investigated and compared with planar structure. The width of the nanowire is ~75 nm, as shown in the top-view SEM picture in Fig. 5.11(a). GaAs was not observed on the SiO_2 surface, indicating the excellent selectivity of the GaAs MEE process on SiGe regions. Focussed ion beam (FIB) milling was performed at the position indicated in Fig. 5.11(a) for subsequent TEM analysis. Pseudomorphic growth of GaAs on the top surface of SiGe is evident from the TEM micrographs in Fig. 5.11(b) and 5.11(c). The

thickness of the GaAs layer is between 20 to 35 nm. The GaAs lattice is well aligned to the SiGe lattice without any observable defects such as APDs or stacking faults. This is attributed to the compliant nature of the nanowire structure which allows stress relief or partition of strain energy between the GaAs layer and SiGe nanowire structure. It should be noted that many MBE growth experiments were performed, and the islanding of GaAs on large planar $Si_{0.35}Ge_{0.65}$ structures is not observed while good coverage is obtained on SiGe nanowires.

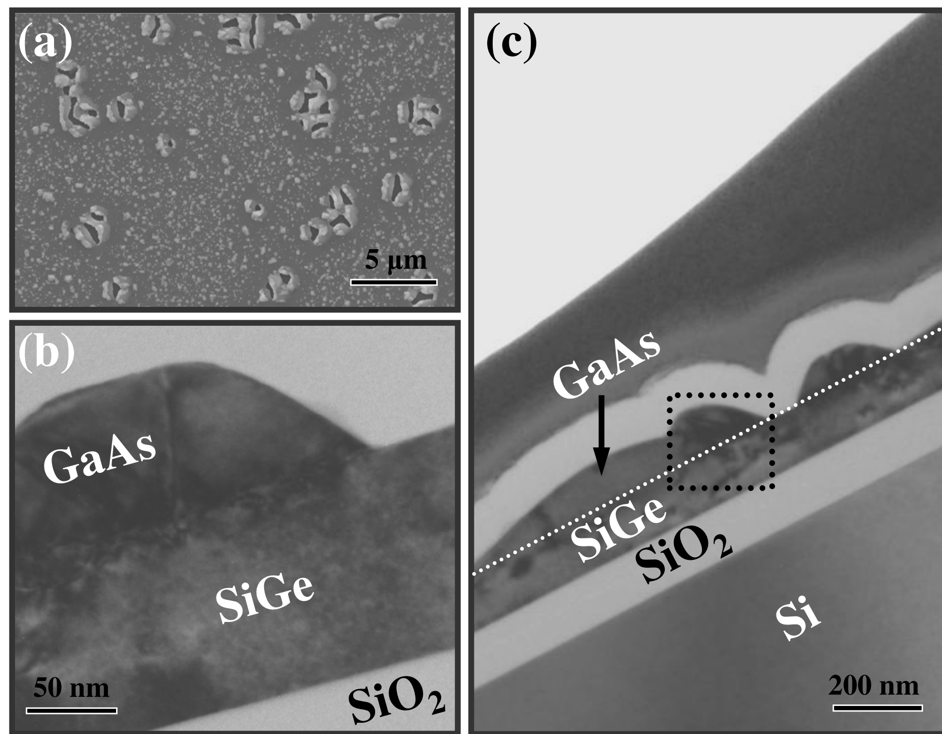


Fig. 5.10 (a) SEM image showing the top view of a layer of GaAs grown on planar SiGe-on-insulator structure. Island formation for stress relief results in a rough GaAs surface. The cross-sectional TEM image in (b) is a zoomed-in view of a region in (c) which shows nucleation of GaAs islands on the SiGe surface. Defects such as stacking faults and dislocations are clearly observed in these GaAs islands and at the interface between GaAs and SiGe. These defects relieve the stress due to lattice mismatch at the GaAs/SiGe heterojunction.

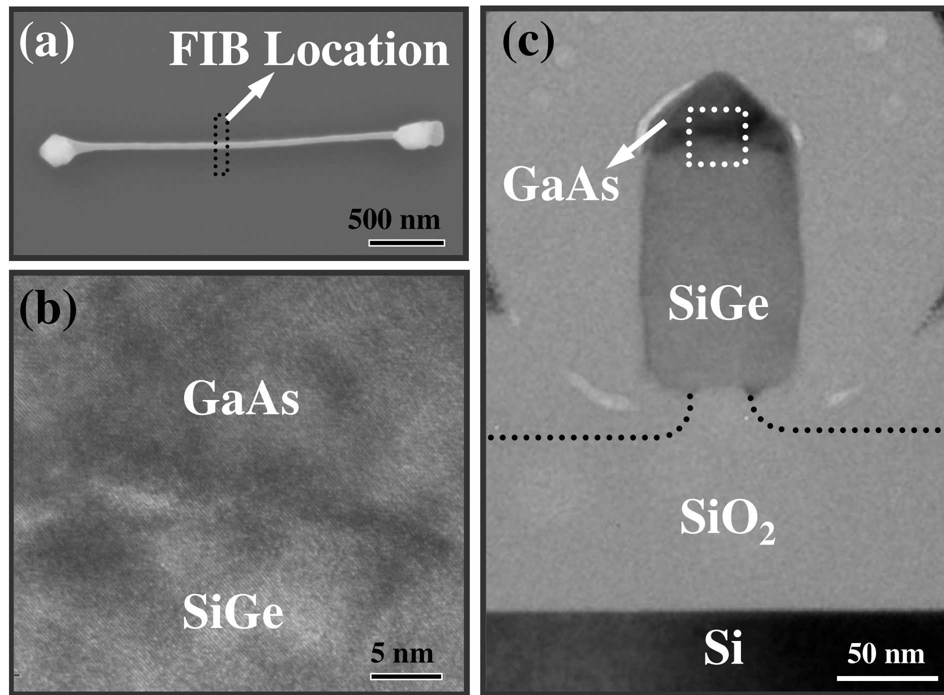


Fig. 5.11 (a) SEM image showing the top view of a $Si_{0.35}Ge_{0.65}$ nanowire with a width of 75 nm and a GaAs layer grown on it. Cross-sectional TEM micrographs in (b) and (c) show that the GaAs layer is pseudomorphically grown on SiGe. The GaAs lattice is well-aligned to the $Si_{0.35}Ge_{0.65}$ lattice and with no observable defects such as APDs or stacking faults.

Next, optical properties of the GaAs epilayer were investigated. Fig. 5.12 shows the PL spectrum of the GaAs on SiGe nanowire structure at room temperature, using 532 nm laser for excitation. Interference effects can be observed in the PL spectrum. This is attributed to multiple internal reflections of the luminescence [5.19]-[5.20] at various interfaces within the GaAs/SiGe/SiO_2/Si multi-layer structure, as illustrated in the inset of Fig. 5.12. The spectral structure due to multiple reflections by the incident light perpendicular to the surface can be analyzed using the following equation,

$$n\, d = (2m + 1)\, \lambda / 4, \qquad (5\text{-}2)$$

where n and d are the refractive index and the thickness of the material where internal reflection occurs, respectively. λ is the wavelength of each

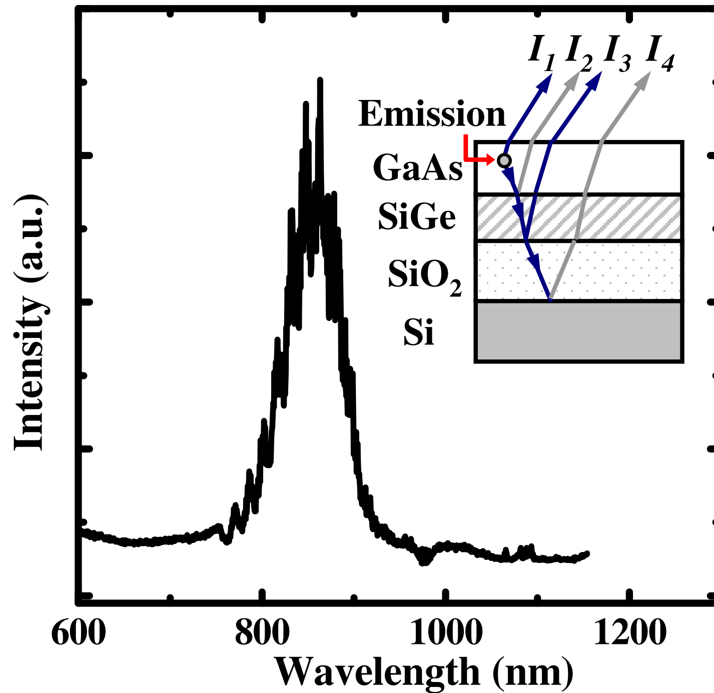


Fig. 5.12 Room temperature photoluminescence spectrum of GaAs on SiGe nanowire. Interference fringes can be observed, and are attributed to multiple reflections within the multi-layer structure, indicating abrupt and flat interface.

interference peak, and *m* is integer. Using equation (5-2), it was determinedthat the interference fringes in Fig. 5.12 are predominantly due to internal reflections between the GaAs-air and SiGe-SiO_2 interface, *i.e.* within the GaAs/SiGe stack, as illustrated by rays I_1 and I_3 in the inset of Fig. 5.12.

Raman spectroscopy was carried out to further investigate the crystalline structure of the GaAs layer grown by MEE at 580 °C. The Ramam spectroscopy was carried out in collaboration with research team from Nanyang Technological University. Fig. 5.13 plots the Raman spectra of GaAs grown on planar SiGe-on-insulator structure and on SiGe nanowire structure. The three main peaks correspond to Si-Si mode, Si-Ge mode, and Ge-Ge mode in the SiGe layer. The small peak at 520 cm^{-1} is the signal of Si-

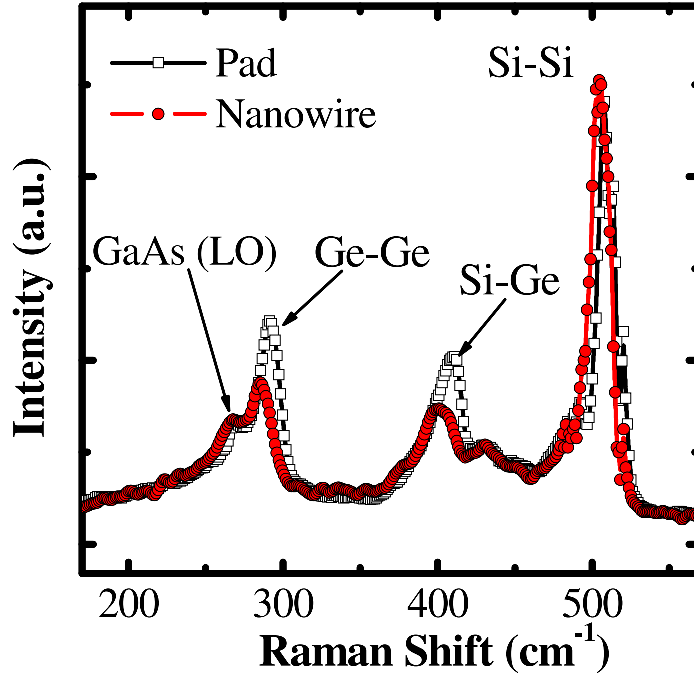


Fig. 5.13 Micro-Raman spectra of GaAs grown on planar SiGe-on-insulator structure and SiGe nanowire structure. The red shift in the Si-Si, Si-Ge, and Ge-Ge mode phonons in the nanowire structure, as compared to planar structure, indicates that the SiGe nanowire is under tensile strain.

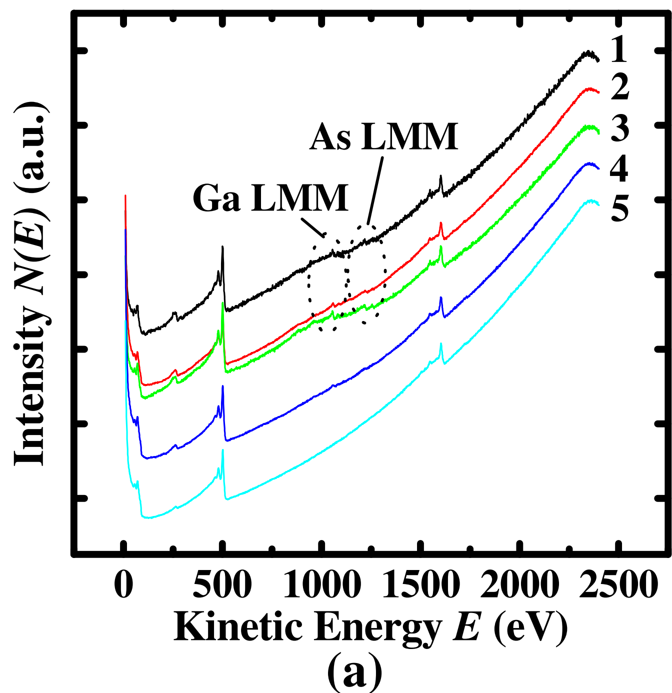
Si phonon from the underlying Si substrate. Note that the Ge-Ge phonon mode overlaps with the longitudinal optical (LO) phonon from GaAs. A red shift in the Si-Si, Si-Ge, and Ge-Ge mode phonons in the nanowire structure indicates that the SiGe region was stretched horizontally, which allows stress relief or distribution of strain energy to accommodate the lattice mismatch. The shift in the Raman frequency of the Si-Si phonons $\Delta\omega_{Si\text{-}Si}$ in SiGe alloy is related to biaxial strain ε by the relationship,

$$\Delta\omega_{Si\text{-}Si} = b\,\varepsilon, \qquad (5\text{-}3)$$

where b is the strain-shift coefficient of Si-Si mode phonons in SiGe alloys, which is equal to -730 ± 70 cm^{-1} [5.21]. The peak position of the Si-Si mode atomic vibrations can be clearly obtained from the Raman spectra in Fig. 5.13

with accuracy comparable to the stability of the horizontal axis calibration, *i.e.* 0.1 cm^{-1}. $\Delta\omega_{Si-Si}$ between planar SiGe-on-insulator structure and SiGe nanowire structure was found to be -2.3 ± 0.2 cm^{-1}. This peak shift in the Si-Si phonons suggested the SiGe nanowire structure is under additional 0.32 ± 0.06 % of lateral tensile strain, as compared to the planar SiGe-on-insulator structure.

It is difficult to achieve selective growth without polycrystalline deposition on the SiO_2 mask due to the high sticking coefficient of Ga atoms on the SiO_2 mask using solid source MBE. Therefore, to obtain the complete selectivity, it is necessary to grow the layers at high substrate temperatures (≥ 700 °C) [5.22] and/or at very slow growth rates [5.23] to enhance the Ga desorption on SiO_2. However, thermal damage may occur on the growth surface at high temperatures due to the evaporation of As molecules in the high vacuum environment during MBE process. In order to reduce the selective-growth temperature, desorption rate of Ga on SiO_2 should be increased at low temperature. This can be achieved by employing MEE, where Ga and As beams are alternatively supplied such that Ga atoms are supplied to the growing surface under an As-free or a very low As pressure atmosphere, as compared to normal MBE. As a result, the Ga desorption is enhanced by decreasing As pressure [5.24]. Auger electron spectroscopy was performed to investigate the growth selectivity of GaAs, as shown in Fig. 5.14. SEM micrograph in the inset of Fig. 5.14 indicates the five locations for the Auger point scanning. No GaAs island was observed in the SiO_2 region. Both Ga-LMM (1060 eV) and As-LMM (1222 eV) were detected in the nanowire regions (locations 1, 2 and 3), confirming the existence of GaAs on the



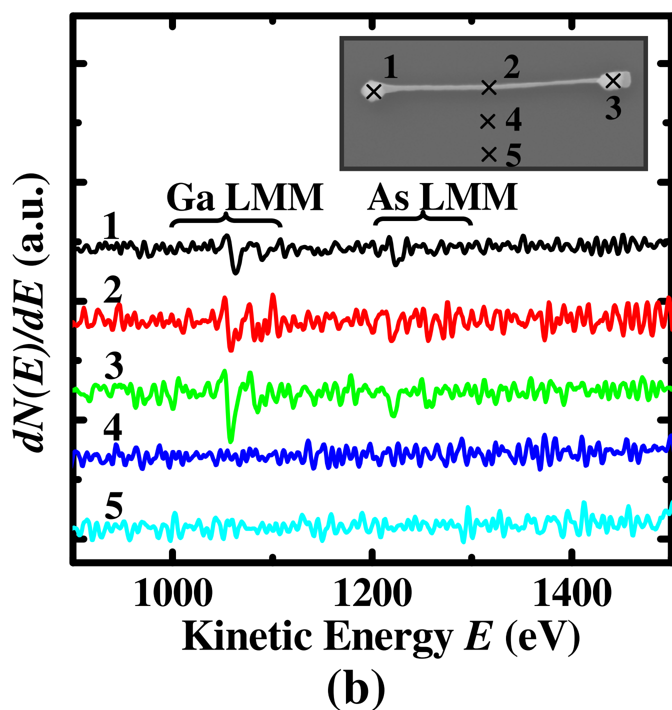


Fig. 5.14 (a) Direct, and (b) differential AES spectra at five locations as shown in SEM micrograph in the inset. Both Ga-LMM and As-LMM were detected in the nanowire regions (locations 1, 2 and 3), confirming the existence of GaAs on the nanowire. Neither Ga nor As was detected in the SiO_2 regions (locations 4 and 5), indicating the high selectivity of the migration-enhanced epitaxy method.

nanowire. No Ga and As was detected in the SiO_2 regions (locations 4

and 5), indicating high selectivity of the MEE method.

5.4 Summary

In this chapter, high quality GaAs growth on SiGe nanowires by MEE process was demonstrated. Compared to GaAs grown on planar SiGe-on-insulator structure, significant reduction in the defects in the GaAs layer grown on SiGe nanowires was confirmed by extensive SEM and cross-sectional TEM analysis. It is attributed to the additional stress relief mechanisms that significantly partition the strain energy between the epilayer and nanoscale underlying structure. The micro-Raman and AES measurements further confirm the good material property and growth selectivity of the GaAs using MEE. The new III-V integration scheme in this chapter may be promising for integrating high speed transistors and optoelectronic devices with advanced electronic circuits on Si platform.

5.5 References

[5.1] D. Zubia, S. Zhang, R. Bommena, X. Sun, S. R. J. Brueck, and S. D. Hersee, "Initial nanoheteroepitaxial growth of GaAs on Si(100) by OMVPE," *J. Electron. Mater.*, vol. 30, no. 7, pp. 812–816, 2001.

[5.2] K. Hjort, "Transfer of InP epilayers by wafer bonding," *J. Cryst. Growth*, vol. 268, no. 3–4, pp. 346–358, 2004.

[5.3] P. Chen, Y. Jing, S. S. Lau, D. Xu, L. Mawst, T. L. Alford, C. Paulson, and T. F. Kuech, "High crystalline-quality III-V layer transfer onto Si substrate," *Appl. Phys. Lett.*, vol. 92, no. 9, p. 092107, 2008.

[5.4] R. M. Sieg, J. A. Carlin, J. J. Boeckl, S. A. Ringel, M. T. Currie, S. M. Ting, T. A. Langdo, G. Taraschi, E. A. Fitzgerald, and B. M. Keyes, "High minority-carrier lifetimes in GaAs grown on low-defect-density Ge/GeSi/Si substrates," *Appl. Phys. Lett.*, vol. 73, no. 21, pp. 3111–3113, 1998.

[5.5] G. Vanamu, A. K. Datye, R. Dawson, and S. H. Zaidi, "Growth of high-quality GaAs on Ge/$Si_{1-x}Ge_x$ on nanostructured silicon substrates," *Appl. Phys. Lett.*, vol. 88, no. 25, p. 251909, 2006.

[5.6] J. Z. Li, J. Bai, J.-S. Park, B. Adekore, K. Fox, M. Carroll, A. Lochtefeld, and Z. Shellenbarger, "Defect reduction of GaAs epitaxy on Si (001) using selective aspect ratio trapping," *Appl. Phys. Lett.*, vol. 91, no. 2, p. 021114, 2007.

[5.7] D. Zubia, and S. D. Hersee, "Nanoheteroepitaxy: The Application of nanostructuring and substrate compliance to the heteroepitaxy of mismatched semiconductor materials," *J. Appl. Phys.*, vol. 85, no. 9, pp. 6492–6496, 1999.

[5.8] Y. Liang, W. D. Nix, P. B. Griffin, and J. D. Plummer, "Critical thickness enhancement of epitaxial SiGe films grown on small structures," *J. Appl. Phys.*, vol. 97, no. 4, p. 043519, 2005.

[5.9] G. H. Wang, E.-H. Toh, Y.-L. Foo, C.-H. Tung, S.-F. Choy, G. Samudra, and Y.-C. Yeo, "High quality silicon-germanium-on-insulator wafers fabricated using cyclical thermal oxidation and annealing," *Appl. Phys. Lett.*, vol. 89, no. 5, p. 053109, 2006.

[5.10] R. W. Olesinski, and G. J. Abbascian, "The Ge-Si (Germanium-Silicon) system," *Bull. Alloy Phase Diagrams*, vol. 5, no. 2, pp. 180–183, 1984.

[5.11] H. B. Kang, J. K. Choi, J. W. Lee, and C. W. Yang, "Dry oxidation behavior of epitaxial $Si_{0.7}Ge_{0.3}$ films," *Mater. Sci. Forum*, vol. 449–452, pp. 361–364, 2004.

[5.12] F. K. LeGoues, R. Rosenberg, T. Nguyen, F. Himpsel, and B. S. Meyerson, "Oxidation studies of SiGe," *J. Appl. Phys*., vol. 65, no. 4, 1724–1728, 1989.

[5.13] H. Klauk, T. N. Jackson, S. F. Nelson, and J. O. Chu, "Thermal stability of undoped strained Si channel SiGe heterostructures," *Appl. Phys. Lett.*, vol. 68, no. 14, pp. 1975–1977, 1996.

[5.14] R. M. Sieg, S. A. Ringel, S. M. Ting, E. A. Fitzgerald, and R. N. Sacks, "Anti-phase domainfree growth of GaAs on offcut (001) Ge wafers by molecular beam epitaxy with suppressed Ge outdiffusion," *J. Electron. Mater.*, vol. 27, no. 7, pp. 900–907, 1998.

[5.15] H. Tanoto, S. F. Yoon, W. K. Loke, K. P. Chen, E. A. Fitzgerald, C. Dohrman, and B. Narayanan, "Heteroepitaxial growth of GaAs on

(100) Ge/Si using migration enhanced epitaxy," *J. Appl. Phys.*, vol. 103, no. 10, p. 104901, 2008.

[5.16] I. Yoshiba, T. Iwai, T. Uehara, Y. Horikoshi, "Area selective epitaxy of GaAs with AlGaAs native oxide mask by molecular beam epitaxy," *J. Cryst. Growth*, vol. 301–302, pp. 190–193, 2007.

[5.17] Y.-C. Yeo, and J. Sun, "Finite-element study of strain distribution in transistor with silicon–germanium source and drain regions," *Appl. Phys. Lett.*, vol. 86, no. 2, p. 023103, 2005.

[5.18] D. J. Eaglesham, and M. Cerullo, "Dislocation-free Stranski-Krastanow growth of Ge on Si(100)," *Phys. Rev. Lett.*, vol. 64, no. 16, pp. 1943–1946, 1990.

[5.19] E. Namvar, and M. Fattahi, "Interference effects on the photoluminescence spectrum of GaN/$In_xGa_{1-x}N$ single quantum well structures," *J. Luminescence*, vol. 128, no. 1, pp. 155–160, 2008.

[5.20] Y. Fujiwara, H. Nishitani, H. Nakata, and T. Ohyama, "Structured photoluminescence spectrum in laterally anodized porous silicon," *Jpn. J. Appl. Phys.*, vol. 31, no. 12B, pp. L1763–L1766, 1992.

[5.21] F. Pezzoli, E. Bonera, E. Grilli, M. Guzzi, S. Sanguinetti, D. Chrastina, G. Isella, H. v. Kanel, E. Wintersberger, J. Stangl, and G. Bauer, "Phonon strain shift coefficients in $Si_{1-x}Ge_x$ alloys," *J. Appl. Phys.*, vol. 103, no. 9, p. 093521, 2008.

[5.22] A. Okamoto, and K. Ohata, "Selective epitaxial growth of gallium arsenide by molecular beam epitaxy," *Appl. Phys. Lett.*, vol. 51, no. 19, pp. 1512–1514, 1987.

[5.23] A. Okamoto, and K. Ohata, "Substrate temperature lowering in GaAs selective epitaxial growth by molecular beam epitaxy," *J. Appl. Phys.*, vol. 66, no. 7, pp. 3413–3415, 1989.

[5.24] S. Yokoyama, J. Oogi, D. Yui, and M. Kawabe, "Low-temperature selective growth of GaAs by alternately supplying molecular beam epitaxy," *J. Cryst. Growth*, vol. 95, no. 1–4, pp. 32–34, 1989.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

Geometrical scaling of conventional silicon (Si) transistors is reaching its fundamental limits after four decades of continuous downsizing of device dimensions. This thesis has sought to explore the application of III-V compound semiconductors as alternative channel materials for extending the performance limits of conventional Si CMOS technology. Various practical and manufacturable surface passivation technologies have been proposed and experimentally realized. In particular, novel *in-situ* surface techniques that comprise vacuum anneal for native oxide desorption, followed by surface treatment, have been demonstrated to effectively suppress native oxides of III-V for significant interface states density reduction. To explore the full potential of III-V MOSFETs, a novel III-V device structure comprising *in-situ* doped lattice-mismatched source/drain (S/D) regions was demonstrated for the reduction of S/D series resistance by high S/D doping and the enhancement of carrier mobility by channel strain engineering.

In addition to conventional bulk planar transistors, alternative device structure has also been explored in this work for effective control of short channel effects in aggressively scaled III-V channel MOSFETs. Such advanced structure makes use of multiple-gate and retrograde-doped channel

designs for improved electrostatic control and short channel effects so that good transistor turn-off characteristics can be achieved. Novel multiple gate field-effect-transistor (MuGFET) or FinFET with epi-controlled retrograde-doped fin has been demonstrated to implement this device concept.

Bulk III-V substrates are expensive, brittle and difficult to make in large diameters. From an economic standpoint, the success of any future CMOS technology will depend on its compatibility with the existing Si manufacturing infrastructure. An effective and potentially viable III-V material integration solution on Si substrate for future high volume semiconductor manufacturing was demonstrated through selective migration-enhanced epitaxy (MEE) of GaAs on strain-compliant SiGe nanowire structures.

6.2 Contributions of This Thesis

The major conclusion and contributions of this work are elucidated here.

6.2.1 *In-situ* Interfacial Engineering for High Quality MOS Stack Formation

The concept and demonstration of novel surface passivation techniques was exploited to realize high quality metal gate/high-*k* dielectric stacks on various III-V compound semiconductors, such as GaAs, and InGaAs [6.1]-[6.11]. This interface engineering technology is highly compatible with a matured high-*k* dielectric deposition process. The passivated III-V transistors

exhibit good electrical characteristics. These results open new avenues for interface passivation to explore the full potential of III-V channel MOSFETs.

6.2.2 Source/Drain Doping and Channel Strain Engineering for Performance Enhancement

In this technology demonstration, the concept of *in-situ* doped lattice-mismatched S/D stressors was examined to enhance the performance of $In_{0.53}Ga_{0.47}As$ channel N-MOSFETs [6.12]-[6.13]. Through finite element simulations, it has been verified that the $In_{0.4}Ga_{0.6}As$ regions act as stressors, giving rise to lateral tensile strain and vertical compressive strain in the $In_{0.53}Ga_{0.47}As$ channel for enhanced electron mobility. In addition, the *in-situ* SiH_4 doping process further boost the N-type S/D doping concentration, contributing to the reduction of total resistance in a transistor for performance enhancement. Significant improvement in drive current performance was observed, which could partially be attributed to strain-induced electron mobility enhancement and series resistance reduction due to *in-situ* S/D doping. Both effects are expected to become more prominent in aggressively scaled MOSFETs. This work provides new insights for device engineers to explore of the full potential of III-V MOSFETs for future technology nodes.

6.2.3 Multiple-Gate Transistor Structure with Retrograde-Channel Doping for Reduced Short Channel Effects

Advanced multiple-gate transistor structure with retrograde channel doping was investigated to improve gate control and suppress short channel effects. The device design and concept was evaluated by three-dimensional

device simulations. In addition, the electrical results further confirmed the significant improvement in short channel effects. The device architecture investigated here is very promising for achieving very high carrier mobility and improved short-channel effects in aggressively scaled III-V transistors.

6.2.4 Nanoheteroepitaxy of Gallium Arsenide on Strain-Compliant Silicon-Germanium Nanowires for Material Integration

Successful hetero-integration of GaAs on Si-based substrate through selective migration-enhanced epitaxy (MEE) of GaAs on strain-compliant SiGe nanowire structures was demonstrated [6.14]. Compared to GaAs grown on planar SiGe-on-insulator structure, significant reduction in the defects in the GaAs layer grown on SiGe nanowires was confirmed by extensive material characterization. It is attributed to the additional stress relief mechanisms that significantly partition the strain energy between the epilayer and nanoscale underlying structure. The photoluminescence and micro-Raman analysis further confirm the good material and optical properties of the GaAs epilayer. This new III-V integration scheme is attractive for integrating high speed transistors and optoelectronic devices with advanced electronic circuits on Si platform.

6.3 Future Directions

In summary, this thesis has conceptualized and embarked on the development of several exploratory concepts and technology options to address several key technical challenges of III-V MOSFET for advanced CMOS applications, such as novel surface passivation methods, advanced

device architectures, and new material integration scheme. Preliminary assessment has been verified and shown to be very promising for its adoption in future technology nodes. Nevertheless, several issues have been opened up in this thesis which deserves further investigation. Some of the suggestions for future directions in the field of III-V MOSFETs are highlighted in this section.

6.3.1 Passivation Studies on Other High Mobility III-V Materials

In Chapter 2, *in-situ* surface passivation methods were demonstrated to realize high quality MOS stacks on III-V compound semiconductors, such as GaAs, and InGaAs. With even higher electron mobilities than GaAs and InGaAs, other III-V materials, such as InAs, InSb, are also very attractive for high speed CMOS applications. Future extension of this work could be on other high mobility III-V compound semiconductors.

6.3.2 Source/Drain and Channel Strain Engineering

Chapter 3 shows that the incorporation of *in-situ* doped lattice-mismatched heterostructure in the S/D regions of an InGaAs MOSFET is a promising approach for reduced S/D series resistance, and enhanced electron mobility. The concepts developed in this thesis could provide insights to the development for III-V devices. Further extension of this work could be on the *in-situ* doping techniques for further increasing the S/D doping level. In addition, the integration of additional stressors, such as high stress SiN liner stressors, on improving channel strain effect could also be explored for further performance benefits.

6.3.3 Hetero-integration of Other High Mobility III-V Materials on Si Substrates

In Chapter 5, GaAs was successfully integrated on Si-based substrate through selective MEE on strain-compliant SiGe nanowire structures. Further development in this area should also focus on the integration of other III-V materials with even higher electron mobilities, such as InGaAs, InAs, and InSb.

6.3.4 III-V P-Channel Devices

Due to the attractive electron mobilities, existing developments on III-V devices are mainly focused on N-channel devices. Further work can also focus on III-V P-channel MOSFETs through material and channel strain engineering to enhance hole mobilities for advanced CMOS technology. For instance, III-V materials with attractive hole mobilities, such as GaSb and InGaSb, may be promising for III-V P-MOSFET applications [6.15].

6.4 References

[6.1] H.-C. Chin, M. Zhu, G. S. Samudra, and Y.-C. Yeo, "N-channel MOSFETs with *in-situ* silane-passivated gallium arsenide channel and CMOS-compatible palladium-germanium contacts," *International Conference on Solid State Devices and Materials*, 2007, pp. 1050–1051.

[6.2] H.-C. Chin, M. Zhu, G. S. Samudra, and Y.-C. Yeo, "N-channel GaAs MOSFET with TaN/HfAlO gate stack formed using *in situ* vacuum anneal and silane passivation," *J. Electrochemical Society*, vol. 155, no. 7, pp. H464–H468, 2008.

[6.3] H.-C. Chin, M. Zhu, C.-H. Tung, G. S. Samudra, and Y.-C. Yeo, "*In situ* surface passivation and CMOS-compatible palladium germanide contacts for surface channel gallium arsenide MOSFETs," *IEEE Electron Device Letters*, vol. 29, no. 6, pp. 553–556, 2008.

[6.4] H.-C. Chin, B. Wang, P.-C. Lim, L.-J. Tang, C.-H. Tung, and Y.-C. Yeo, "Realizing high quality metal-gate/high-permittivity dielectric stack on indium gallium arsenide by vacuum annealing and silane treatment," *International Conference on Solid State Devices and Materials*, 2008, pp. 1058–1059.

[6.5] H.-C. Chin, B. Wang, P.-C. Lim, L.-J. Tang, C.-H. Tung, and Y.-C. Yeo, "Study of surface passivation of strained indium gallium arsenide by vacuum annealing and silane treatment," *J. Applied Physics*, vol. 104, no. 9, p. 093527, 2008.

[6.6] H.-C. Chin, M. Zhu, Z.-C. Lee, X. Liu, K.-M. Tan, H. K. Lee, L. Shi, L.-J. Tang, C.-H. Tung, L.-S. Tan, and Y.-C. Yeo, "A new silane-

ammonia surface passivation technology for realizing inversion-type surface-channel GaAs n-MOSFET with 160 nm gate length and high-quality metal-gate/high-k dielectric stack," in *IEDM Tech. Dig.*, 2008, pp. 383–386.

[6.7] H.-C. Chin, M. Zhu, X. Liu, H.-K. Lee, L. Shi, L.-S. Tan, and Y.-C. Yeo, "Silane-ammonia surface passivation for gallium arsenide surface-channel n-MOSFETs," *IEEE Electron Device Letters*, vol. 30, no. 2, pp. 110–112, 2009.

[6.8] H.-C. Chin, M. Zhu, S.-J. Whang, C.-H. Tung, G. S. Samudra, and Y.-C. Yeo, "*In-situ* surface passivation and metal-gate/high-k dielectric stack formation for n-channel gallium arsenide metal-oxide-semiconductor field-effect transistors," *International Symposium on VLSI Technology, Systems and Applications* (*VLSI-TSA*), 2008, pp. 26–27.

[6.9] H.-C. Chin, Z. Lin, X. Liu, L.-S. Tan, and Y.-C. Yeo, "Inversion-type surface channel $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistors with metal-gate/high-k dielectric stack and CMOS-compatible PdGe contacts," *International Symposium on VLSI Technology, Systems and Applications* (*VLSI-TSA*), 2009, pp. 143–144.

[6.10] H.-C. Chin, X. Liu, X. Gong, and Y.-C. Yeo, "Silane and ammonia surface passivation technology for high mobility $In_{0.53}Ga_{0.47}As$ MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 5, pp. 973–979, 2010.

[6.11] H.-C. Chin, X. Gong, L. Wang, and Y.-C. Yeo, "Fluorine incorporation in HfAlO gate dielectric for defect passivation and effect on electrical

characteristics of $In_{0.53}Ga_{0.47}As$ n-MOSFETs," *Electrochemical and Solid-State Letters*, vol. 13, no. 12, pp. H440–H442, 2010.

[6.12] H.-C. Chin, X. Gong, X. Liu, Z. Lin, and Y.-C. Yeo, "Strained $In_{0.53}Ga_{0.47}As$ n-MOSFETs: Performance boost with *in-situ* doped lattice-mismatched source/drain stressors and interface engineering," in *VLSI Symp. Tech. Dig.*, 2009, pp. 244–245.

[6.13] H.-C. Chin, X. Gong, X. Liu, and Y.-C. Yeo, "Lattice mismatched $In_{0.4}Ga_{0.6}As$ source/drain stressors with in situ doping for strained $In_{0.53}Ga_{0.47}As$ channel n-MOSFETs," *IEEE Electron Device Letters*, vol. 30, no. 8, pp. 805–807, 2009.

[6.14] H.-C. Chin, X. Gong, T. K. Ng, W. K. Loke, C. P. Wong, Z. Shen, S. Wicaksono, S. F. Yoon, and Y.-C. Yeo, "Nanoheteroepitaxy of gallium arsenide on strain-compliant silicon-germanium nanowires," *J. Applied Physics*, vol. 108, no. 2, p. 024312, 2010.

[6.15] A. Nainani, T. Irisawa, Y. Sun, F. Crnogorac, and K. Saraswat, "A sub 350ºC GaSb pMOSFET with ALD high-k dielectric," *International Conference on Solid State Devices and Materials*, 2010, pp. 133–134.

Appendix A

List of Publications

Journal Publications

[1] M. Zhu, **H.-C. Chin**, C.-H. Tung, and Y.-C. Yeo, "*In-situ* silane passivation of gallium arsenide and deposition of high-permittivity gate dielectric for metal-oxide-semiconductor applications," *J. Electrochemical Society*, vol. 154, no. 10, pp. H879–H882, 2007.

[2] **H.-C. Chin**, M. Zhu, C.-H. Tung, G. S. Samudra, and Y.-C. Yeo, "*In situ* surface passivation and CMOS-compatible palladium germanide contacts for surface channel gallium arsenide MOSFETs," *IEEE Electron Device Letters*, vol. 29, no. 6, pp. 553–556, 2008.

[3] **H.-C. Chin**, M. Zhu, G. S. Samudra, and Y.-C. Yeo, "N-channel GaAs MOSFET with TaN/HfAlO gate stack formed using *in situ* vacuum anneal and silane passivation," *J. Electrochemical Society*, vol. 155, no. 7, pp. H464–H468, 2008.

[4] **H.-C. Chin**, B. Wang, P.-C. Lim, L.-J. Tang, C.-H. Tung, and Y.-C. Yeo, "Study of surface passivation of strained indium gallium arsenide by vacuum annealing and silane treatment," *J. Appl. Phys.*, vol. 104, no. 9, p. 093527, 2008.

[5] **H.-C. Chin**, M. Zhu, X. Liu, H.-K. Lee, L. Shi, L.-S. Tan, and Y.-C. Yeo, "Silane-ammonia surface passivation for gallium arsenide surface-channel n-MOSFETs," *IEEE Electron Device Letters*, vol. 30, no. 2, pp. 110–112, 2009.

[6] **H.-C. Chin**, X. Gong, X. Liu, and Y.-C. Yeo, "Lattice mismatched $In_{0.4}Ga_{0.6}As$ source/drain stressors with *in situ* doping for strained $In_{0.53}Ga_{0.47}As$ channel n-MOSFETs," *IEEE Electron Device Letters*, vol. 30, no. 8, pp. 805–807, 2009.

[7] **H.-C. Chin**, X. Liu, X. Gong, and Y.-C. Yeo, "Silane and ammonia surface passivation technology for high mobility $In_{0.53}Ga_{0.47}As$ MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 5, pp. 973–979, 2010.

[8] **H.-C. Chin**, X. Gong, T. K. Ng, W. K. Loke, C. P. Wong, Z. Shen, S. Wicaksono, S. F. Yoon, and Y.-C. Yeo, "Nanoheteroepitaxy of gallium arsenide on strain-compliant silicon-germanium nanowires," *J. Appl. Phys.*, vol. 107, no. 2, p. 024312, 2010.

[9] **H.-C. Chin**, X. Gong, L. Wang, and Y.-C. Yeo, "Fluorine incorporation in HfAlO gate dielectric for defect passivation and effect on electrical characteristics of $In_{0.53}Ga_{0.47}As$ n-MOSFETs," *Electrochemical and Solid-State Letters*, vol. 13, no. 12, pp. H440–H442, 2010.

[10] X. Gong, **H.-C. Chin**, S.-M. Koh, L. Wang, Ivana, Z. Zhu, B. Wang, C. K. Chia, and Y.-C. Yeo, "Source/drain engineering for $In_{0.7}Ga_{0.3}As$ n-channel metal-oxide-semiconductor field-effect transistors: Raised source/drain with in situ doping for series resistance reduction," *Japanese J. Applied Physics*, vol. 50, no. 4, 2011.

Conference Publications

[11] **H.-C. Chin**, M. Zhu, G. S. Samudra, and Y.-C. Yeo, "N-channel MOSFETs with *in-situ* silane-passivated gallium arsenide channel and

CMOS-compatible palladium-germanium contacts," *International Conference on Solid State Devices and Materials*, 2007, pp. 1050–1051.

[12] **H.-C. Chin**, M. Zhu, S.-J. Whang, C.-H. Tung, G. S. Samudra, and Y.-C. Yeo, "*In-situ* surface passivation and metal-gate/high-k dielectric stack formation for n-channel gallium arsenide metal-oxide-semiconductor field-effect transistors," *International Symposium on VLSI Technology, Systems and Applications* (*VLSI-TSA*), 2008, pp. 26–27.

[13] **H.-C. Chin**, B. Wang, P.-C. Lim, L.-J. Tang, C.-H. Tung, and Y.-C. Yeo, "Realizing high quality metal-gate/high-permittivity dielectric stack on indium gallium arsenide by vacuum annealing and silane treatment," *International Conference on Solid State Devices and Materials*, 2008, pp. 1058–1059.

[14] **H.-C. Chin**, M. Zhu, Z.-C. Lee, X. Liu, K.-M. Tan, H. K. Lee, L. Shi, L.-J. Tang, C.-H. Tung, L.-S. Tan, and Y.-C. Yeo, "A new silane-ammonia surface passivation technology for realizing inversion-type surface-channel GaAs n-MOSFET with 160 nm gate length and high-quality metal-gate/high-*k* dielectric stack," in *IEDM Tech. Dig.*, 2008, pp. 383–386.

[15] **H.-C. Chin**, Z. Lin, X. Liu, L.-S. Tan, and Y.-C. Yeo, "Inversion-type surface channel $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistors with metal-gate/high-k dielectric stack and CMOS-compatible PdGe contacts," *International Symposium on VLSI Technology, Systems and Applications* (*VLSI-TSA*), 2009, pp. 143–144.

[16] **H.-C. Chin**, X. Gong, X. Liu, Z. Lin, and Y.-C. Yeo, "Strained $In_{0.53}Ga_{0.47}As$ n-MOSFETs: Performance Boost with *in-situ* Doped Lattice-Mismatched Source/Drain Stressors and Interface Engineering," in *VLSI Symp. Tech. Dig.*, 2009, pp. 244–245.

[17] X. Liu, **H.-C. Chin**, L. S. Tan, and Y.-C. Yeo, "Metal-gate/high-permittivity dielectric stack on gallium nitride formed by silane surface passivation and metal-organic chemical vapor deposition," *International Conference on Solid State Devices and Materials*, 2009, pp. 1214–1215.

[18] **H.-C. Chin**, X. Gong, H. Guo, Q. Zhou, S.-M. Koh, H. K. Lee, L. Shi, and Y.-C. Yeo, "Performance boost for $In_{0.53}Ga_{0.47}As$ channel N-MOSFET using silicon nitride liner stressor with high tensile stress," *International Semiconductor Device Research Symposium*, 2009.

[19] X. Gong, **H.-C. Chin**, S.-M. Koh, L. Wang, Ivana, B. Wang, C. K. Chia, and Y.-C. Yeo, "Source/drain engineering for $In_{0.7}Ga_{0.3}As$ N-MOSFETs: Raised source/drain with *in situ* doping for series resistance reduction," *International Conference on Solid State Devices and Materials*, 2010, pp. 131–132.