DEVELOPMENT OF HIGH MOBILITY CHANNEL LAYER FORMATION TECHNOLOGY FOR HIGH SPEED CMOS DEVICES

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Growth means change and

change involves risk, stepping

from the known to the unknown.

- Author unknown

I chose NUS to pursue a Ph.D. in 2005 with luck when I had worked for 11 years and become an effective being in the company regardless of my will. Because, studying abroad has been one of my lifelong dreams. At least, I made the decision then because of that. However, at this moment when I am at the end of the course, I come to know that the journey was prepared only for me to grow along the way by the God. The Ph.D. course was so different from my expectations, but it was full of changes and thanks that I had never imagined. During my time at Silicon Nano Device Laboratory (SNDL), NUS in Singapore, I have learned so many things not only about the MOSFETs and semiconductor engineering but also about the values of spiritual virtues such as love, passion, patience, faith, and truth again. I will never forget the happiest moments when the unknown suddenly changes to the known in the lecture theater, in front of the Jusung Gate Cluster, in the seat of #151 bus, and so on… And there are so many people whom I thank for their kind help, insightful discussion, teaching, and shaping me during the past five years.

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ABSTRACT

As the gate length of complementary metal-oxide-semiconductor field-effect transistor (CMOSFET) approaches ~10 nm regime, the traditional Si CMOS scaling faces its fundamental limits. Among the proposed technical solutions, GaAs-based III-V compound semiconductors are actively being studied as a possible alternative for a high speed n-channel MOSFET (NMOSFET) due to their low effective electron masses, high electron mobilities, the accumulated knowledge, and the difficulty in Ge NMOSFET realization. However, the III-V MOSFET technology should address several critical issues with the device realization. The challenges include how to integrate a high quality III-V channel layer into Si platform and how to achieve the thermally stable III-V/high-*k* interface without Fermi level pinning.

In the first part of this thesis, novel approaches for GaAs-on-insulator (GaAs-OI) fabrication technology were explored to overcome the physical and technical challenges in growing the GaAs heteroepitaxial layer in Si platform. The cost-effective Ge-condensation technique was developed to provide a compositionally graded SiGe-on-insulator (SGOI) as a virtual substrate for the GaAs heteroepitaxy on Silicon-on-insulator (SOI). A modified two-step Ge-condensation resulted in 42 nm thick SGOI with 71 % Ge concentration on top of the SGOI with an excellent crystalline quality. For the first time, a device quality GaAs-OI structure has been realized on a Si wafer through the graded SGOI virtual substrate using molecular beam epitaxy with introduction of migration-enhanced epitaxy technique.

In the second part of this thesis, fabrication processes were developed to realize the NMOSFET integrated with metal-organic chemical vapor deposited (MOCVD) Hf-based high-*k*/metal gate stack on a GaAs-based III-V channel in a self-aligned gate-

first fabrication scheme. The main process steps included pre-deposition cleaning, HfO_2 and HfAlO MOCVDs, and Si implanted n^+ S/D formation processes. The focus was on improving III-V/high-*k* interface quality to mitigate Fermi level pinning issue. Electrical properties were investigated to optimize the material combinations and processes further. Consequently, enhancement mode NMOSFET with ~3 times higher peak mobility over the universal mobility of Si has been demonstrated with MOCVD HfAlO/TaN gate stack on $In_{0.53}Ga_{0.47}As$ channel.

Finally, a Si-compatible passivation technique using *in situ* PH_3 treatment is proposed, explored and investigated to improve the InGaAs NMOSFET performance. It was found that at low pressure PH_3-N_2 plasma condition, a 1 monolayer thick phosphorus nitride (P_xN_y) layer is formed with an underlying P-for-As exchanged layer as a minor product on InGaAs substrate in a wide range of process window. The improved interface quality of the P_xN_y-passivated $In_{0.53}Ga_{0.47}As$ is identified and compared with the non-passivated InGaAs and PH_3-based passivated InGaAs without P_xN_y layer with chemical and physical properties. The P_xN_y passivation greatly improved electrical properties of the InGaAs MOSFET devices. Technology demonstration with this novel P_xN_y passivation achieved the low subthreshold slope approaching the ideal value of 60 mV/dec as well as the significantly enhanced peak mobility in the inversion layer of ~5 times the universal Si mobility at the corresponding low field. Thermal stability of the P_xN_y-passivated interface was examined up to 750 ^oC with the self-aligned InGaAs/HfO_2 MOSFET devices by activating the S/D at different temperatures.

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LIST OF SYMBOLS AND ACRONYMS

Symbol/Acronym	Description
2D	two-dimensional
a	lattice constant
α	elastic strain
AFM	atomic force microscopy
ALD	atomic layer deposition
BE	binding energy
BEP	beam equivalent pressure
BOX	buried oxide
BTBT	band-to-band tunneling
CBO	conduction band offset
C_{gc}	gate-to-channel capacitance
CMOSFET	Complementary metal-oxide-semiconductor field-effect transistor
CMP	chemical mechanical polishing
C_{ox}	gate oxide capacitance
δ	plastic strain
DHF	dilute HF
DIBL	drain-induced barrier lowering
D_{it}	density of interface states
ε_o	permittivity of vacuum
EDS	energy dispersive X-ray spectroscopy
E_g	bandgap
E-mode	enhancement mode
EOT	electrical equivalent oxide thickness
f	lattice mismatch
FDSOI	fully depleted silicon-on-insulator
FGA	forming gas anneal
FWHM	full width at half-maximum
GaAs-OI	GaAs-on-insulator
GIDL	gate-induced drain leakage

G_m	transconductance
GOI	Ge-on-insulator
HA-2	$HfAl(OiPr)_5(MMP)_2$
h_c	critical thickness
HTB	hafnium tetra tert-butoxide, $Hf(OC(CH_3)_3)_4$
IC	integrated circuit
I_D	drain current of MOSFET
I_{Dsat}	MOSFET saturation current
III-V-OI	III-V-on-insulator
I_{leak}	leakage current
I_{off}	off-state current
I_{on}	on-state current
ITRS	International Technology Roadmap for Semiconductors
J_G	gate leakage current density
k	relative permittivity (dielectric constant) of dielectric
k_B	Boltzmann's constant
L	channel length of MOSFET
L_G	gate length of MOSFET
m^*	effective mass
μ	carrier mobility
MBE	molecular beam epitaxy
MEE	migration-enhanced epitaxy
MIGS	metal-induced gap states
ML	monolayer
MOCVD	metal-organic chemical vapor deposition
MOSFET	metal-oxide-semiconductor field-effect transistor
NMOSFET	n-channel MOSFET
PDA	post-deposition anneal
PDSOI	partially depleted SOI
PMOSFET	p-channel MOSFET
PVD	physical vapor deposition
q	electron charge
rf	radio-frequency

RHEED	reflection high-energy electron diffraction
rms	root-mean-square
R_{sh}	sheet resistance
RTA	rapid thermal anneal
S/D	source/drain
SCE	short-channel effects
SEM	scanning electron microscopy
SGOI	SiGe-on-insulator
SIMS	secondary ion mass spectroscopy
SOI	Si-on-insulator
SS	subthreshold slope
STS	scanning tunneling spectroscopy
T	temperature
τ	intrinsic delay
TEM	transmission electron microscopy
TOA	take-off angle
T_{ox}	equivalent oxide thickness of the gate dielectric
UHV CVD	ultrahigh-vacuum chemical vapor deposition
UTB	ultrathin body
VBM	valence band maximum
VBO	valence band offset
V_D	drain voltage
V_{dd}	power supply voltage
V_{FB}	flatband voltage
V_G	gate voltage
V_{th}	threshold voltage
W	channel width of MOSFET
XPS	X-ray photoelectron microscopy

CHAPTER 1

INTRODUCTION

The remarkable development in integrated circuit (IC) capability, which has been made over the past five decades, is due to the success on miniaturization of the IC component devices, such as transistors, capacitors, and resistors, mostly made by using semiconductors. The smaller the semiconductor devices can be made, the higher the IC performance is achievable per unit chip area. In addition, as multi-functional ICs are needed, the response time of the semiconductor devices should be one of the critical requirements for high-performance ICs. Therefore, most researches in microelectronics industry have thus focused on how to make smaller and faster semiconductor devices.

Among the semiconductor devices, metal-oxide-semiconductor field-effect transistor (MOSFET) is the most important building block today. Although the concept of the MOSFET was developed well in the early 1930s, the first MOSFETs suitable for commercial use appeared in the 1960s. It was mainly due to the discovery of a thermally oxidized Si structure MOSFET which was first demonstrated by Kahng and Atalla in 1960 [1]. Since then, the thermally oxidized Si structure MOSFETs have been widely used in ICs because of their simpler fabrication, higher density and lower power compared to the other types of devices. A schematic n-channel MOSFET (NMOSFET) is illustrated in Fig. 1.1 with its operation principle as a digital switch.

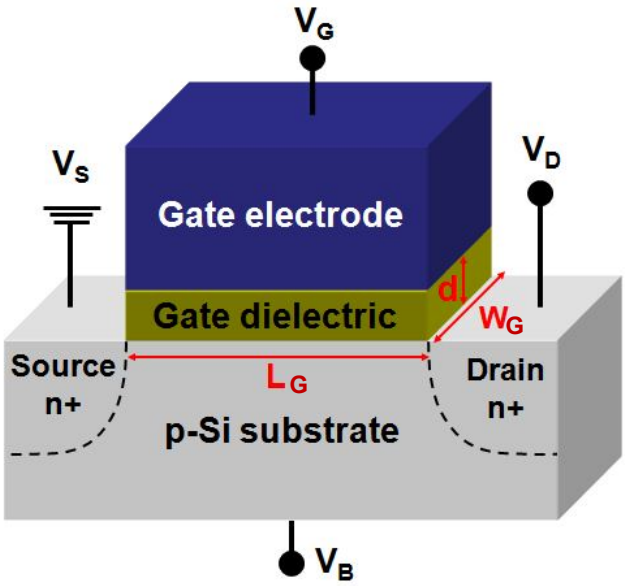


Fig. 1.1 Schematic of a Si NMOSFET structure. Gate dimension is defined by the gate length, L_G, the gate width, W_G, and the thickness of gate dielectric, d. If a large positive voltage is applied to V_G, the p-type Si surface under the gate ($W_G \times L_G$) is inverted and a conductive n-type channel is induced connecting the source and the drain.

The miniaturization, called scaling, of MOSFET has been achieved by simple reduction of its dimension to increase the transistor density without degradation of the device performance. Over a span of 30 years, the minimum feature size (~L_G) available in MOS technologies has been reduced by a factor of 200 (from ~20 to ~0.1 μm) and the area density of devices has increased by more than 40,000 times [2]. On the other hand, the gate stack system has been maintained as Si channel, SiO_2 gate dielectric, and highly doped poly-Si gate electrode. That is largely due to the system's superior properties such as low interface state density between SiO_2 and Si substrate, excellent thermal stability of SiO_2 on Si, and high dielectric breakdown field of SiO_2 [3]. However, the rapid scaling has brought this Si-based technology to the point where fundamental physical phenomena such as tunneling current of a thin SiO_2 dielectric film and tunneling current through the drain-to-body junction are beginning to impede the further progress. In order to overcome this difficulty, many new and innovative changes to the basic Si-based complementary MOSFET (CMOSFET) technology are

being explored, including new gate geometries, the use of strain to enhance the mobility, and the use of new gate stack materials. Thus this work of development of high mobility channel layer formation technology has been carried out for the innovative change.

The subsequent sections in this chapter provide the background and objectives of this work to find ways to extend the scaling and to resolve the fundamental issues in the traditional Si-based CMOS technology. Some of the most promising approaches to maintain the MOSFET scaling speed are reviewed with brief theoretical considerations. Finally, a scope of this work will be given, followed by the organization of this thesis.

1.1 MOS SCALING BEYOND THE 10 nm NODE

In this section, a brief overview of MOS scaling trend with present state-of-the-art CMOSFET technologies, industry targets for future progress, and challenges to accomplish the goal of MOS scaling beyond the 10 nm gate length will be presented as a background of this thesis.

1.1.1 OVERVIEW OF MOSFET SCALING

The continued scaling of MOSFET to reduce the cost per function with increased transistor density has been a driving force in IC industry. In 1965, G. E. Moore, the founder of Intel Corporation, predicted that the number of transistors placed on an IC would double every two years [4] and the statement, since then, has been known as Moore's law guiding the direction of progress as shown in Fig. 1.2.

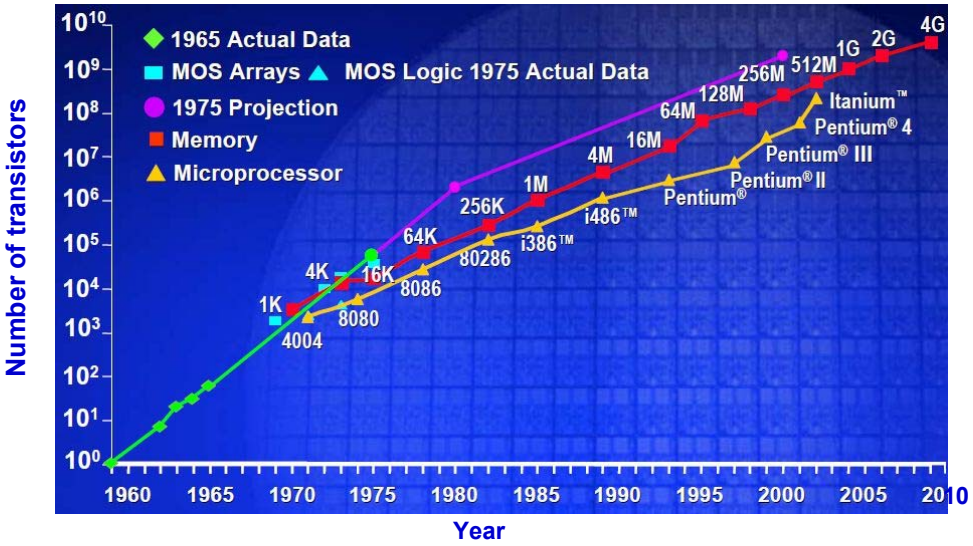


Fig. 1.2 Illustration of Moore's Law: The number of microprocessor transistors by year. [5]

The physical dimension scaling principle behind the Moore's law can simply be expressed by the long-channel MOSFET equation, in which the saturation drive current, I_{Dsat} of MOSFET can be depicted as follows:

$$I_{Dsat} = \frac{W}{2L}\mu C_{ox}\left(V_G - V_{th}\right)^2 = \frac{W}{2L}\mu\frac{\varepsilon_o k_{ox}}{d}\left(V_G - V_{th}\right)^2 \tag{1.1}$$

where W and L are the channel width and length respectively, μ is the carrier mobility in the channel, C_{ox} is the gate oxide capacitance density, V_G is the gate bias, V_{th} is the threshold voltage of the transistor, ε_o is the permittivity of vacuum, k_{ox} is the relative permittivity of the oxide, called dielectric constant, and d is the physical thickness of the oxide. The channel dimension (W×L) is regarded as same as the gate dimension (L_G×W_G) in an ideal self-aligned MOSFET structure. When the gate dielectric is SiO_2, k_{ox} is 3.9 and d is SiO_2 thickness, T_{ox}. The most important output parameter of MOSFET is the intrinsic delay, $\tau = CV/I$, where C is the total gate capacitance per transistor width, V is the power supply voltage, V_{dd}, and I is the saturation drive current per transistor width, I_{Dsat}. Hence, the MOSFET performance is directly proportional to I_{Dsat}. The gate length, L_G and T_{ox}, i.e. d in the case of SiO_2 dielectric, have been

reduced exponentially according to the equation (1.1) to increase I_{Dsat} and to decrease τ. Those L_G and T_{ox} scaling trends are illustrated in Fig. 1.3a and b, respectively [5].

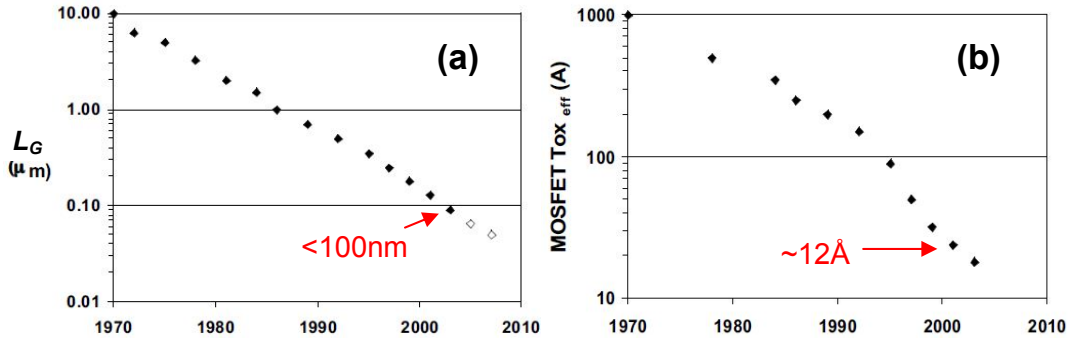


Fig. 1.3 (a) Gate length, L_G and (b) gate oxide thickness, T_{ox} changes in production MOSFET by year [5].

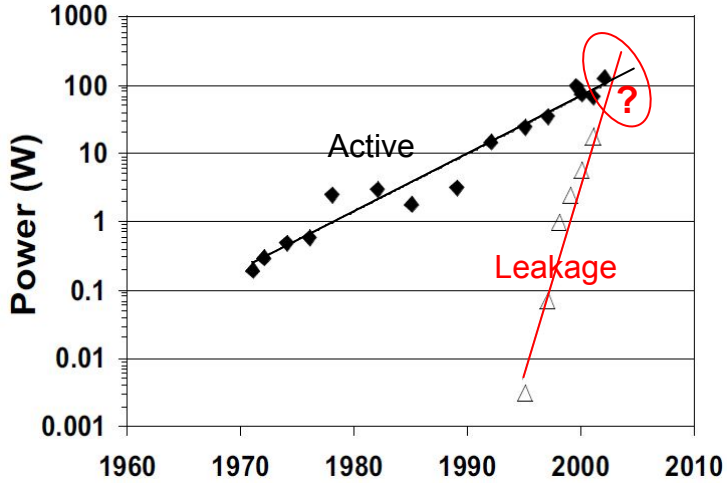


Fig. 1.4 Increasing power dissipation trend, which is illustrated from active power and standby power, i.e. leakage by production year from industry data. Traditional scaling will not be valid near the cross over point drawn by the extrapolations. [5]

This threat can be seen clearly in the active and standby power trends (Fig.1.4). Standby power, which is proportional to leakage currents in MOSFET, has increased exponentially in contrast to the increase of active power, which is affected by I_{Dsat} and V_{dd}^2. As the SiO_2 thickness, T_{ox} approaches around 4 nm, a fundamental quantum mechanical tunneling causes a high gate leakage current (J_G) regardless of the V_G

applied [6]. Moreover, as the L_G is scaled, independent control of channel by the gate is lost and the drain field also influences the ease of channel formation – called the short-channel effect (SCE). Due to these effects, the V_{th} reduces with decreasing L_G (V_{th} roll off), the V_{th} reduces with increasing V_D (drain-induced barrier lowering, DIBL) and the subthreshold slope (SS) is degraded, leading to higher OFF state currents, I_{Off}. Figure 1.3 shows that Si-based CMOS scaling is seriously confronted by inherent physical property limitation of SiO_2 as well as lithography technology to define the minimum feature size.

Therefore, in order to continue the MOSFET scaling to further improve the performance, innovative process techniques and new materials have been introduced and are being explored, including new gate geometries and multiple gates, the use of strain to increase mobility, the use of high-*k* dielectric/metal gate stack instead of SiO_2/poly-Si gate stack, and the use of metal source/drain (S/D). Actually, those performance boosters have been employed in microprocessor production from the 90 nm technology starting from mobility enhancement technique using stressors in S/D [7].

Figure 1.5 shows the state-of-the-art gate stacks of 32 nm logic technology developed with various performance boosters, maintaining the historic scaling trends [8]. The key performance boosters include the high-*k* gate dielectric with metal gate to reduce the gate leakage with scaled T_{ox}, the strained Si channel engineering to enhance the channel mobility with increased Ge fraction in SiGe stressor S/D, and the raised S/D to reduce parasitic resistance. Conventional scaling approaches, such as shrinking dimensions, lowering S/D resistance, reducing junction depth, optimizing channel doping and electric field, and so on, are also included.

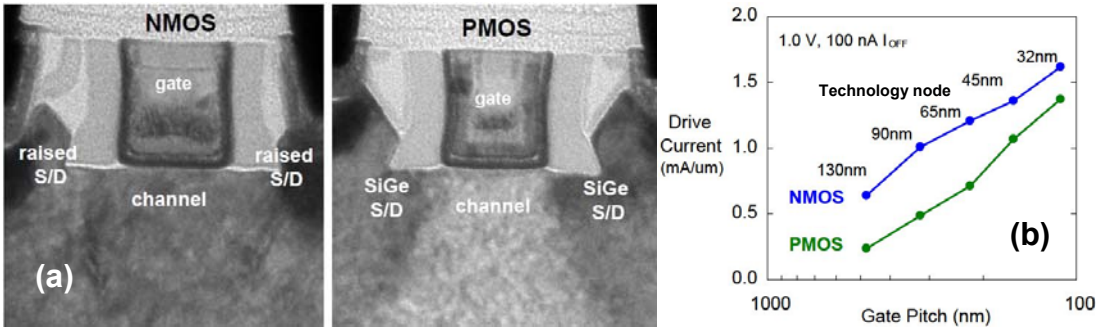


Fig. 1.5 (a) Cross section of NMOS and PMOS transistors showing high-*k*/metal gate, raised and embedded S/D regions in 32 nm logic technology. (b) I_D as a function of gate pitch (length for one gate and one S/D contact). [8]

Partially depleted Si-on-insulator (PDSOI) MOSFET is also available for the state-of-the-art 22 nm technology as shown in Fig. 1.6 [9]. Instead of the strained Si technology above, PDSOI structure is employed here.

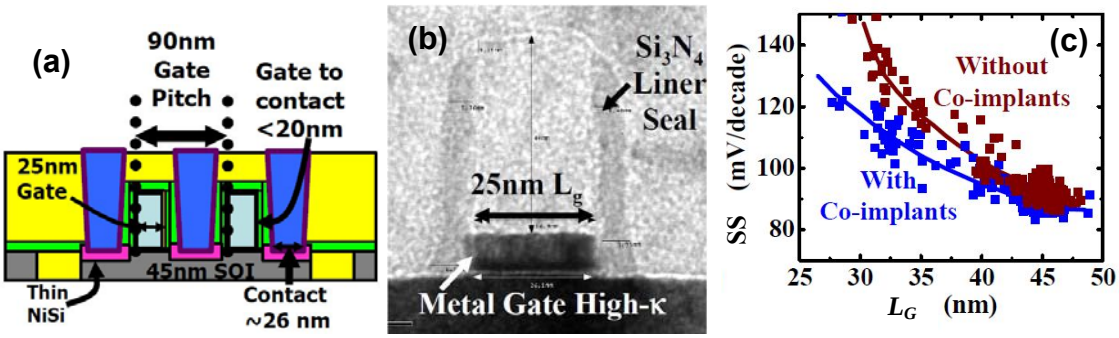


Fig. 1.6 (a) Cross section view of a MOSFET at 22 nm node dimensions. (b) TEM image of the gate stack (c) SS measurement showing gate length scaling with S/D engineering effect [9]

However, the introduction of more effective performance boosters will still be required to maintain the historic trend of 17 % performance improvement each year.

1.1.2 ITRS PROJECTIONS

Since 1994 the semiconductor industry has periodically created "roadmaps" showing how it expects CMOS technology to progress. The main aim of the roadmaps includes identifying key technical requirements and challenges critical to sustaining the historical scaling of CMOS technology and simulating the required research and development to meet the key challenges. According to the international technology roadmap for semiconductors (ITRS) 2009 edition, the new gate length scaling model, the *CV/I* speed metric with a slope of ~13 % instead of 17 % increase per year has been employed to project the future technology [10], due to the serious fundamental obstacles. The technology requirements reflect the needs of three different types of application: high-performance (HP), low-operating power (LOP), and low standby power (LSTP). The latest projections for key physical and electrical requirements are summarized in Table 1.1 where the device structure is planar bulk Si [10]. Those with grey background indicate there is no known manufacturable solution while those without data mean it has reached the theoretical limit of the scaling. According to these projections, it is hoped that MOSFET will reach physical gate length of 9.7 nm by 2021. However, as seen in the Table 1.1, it is not possible theoretically and technically with the conventional approach at the present time. Challenges to meet the requirements for the gate length below 10 nm are elaborated as follows.

1.1.3 CHALLENGES FOR FURTHER SCALING

Further reduction of CMOS dimensions poses more difficult challenges in meeting the requirements of the electrical parameters because those main indexes have significant trade-off with each other. If the electrical equivalent oxide thickness (EOT) decreases to increase I_{on}, the J_G increases exponentially, and if V_{dd} decreases to reduce

Table 1.1 High-performance (HP), low-operating power (LOP), and low standby power (LSTP) logic technology requirements where the transistor type is a planar bulk CMOSFET. [10]

(MPU: microprocessor unit; EOT: electrical equivalent oxide thickness; $J_{G,limit}$: the maximum allowed gate leakage current density at $V_G=V_{dd}$ and 25 ^{o}C; I_{on}: I_D at $V_G=V_D=V_{dd}$; Effective ballistic enhancement factor: a multiplying factor for I_{on} to meet the I_{on} required, which is largely due to quantum effects on mobility.)

Year of Production	***2009***	***2012***	***2015***	***2018***	***2021***
MPU Metal 1 ½ Pitch (nm)	54	32	21	15	10.6
Physical gate length for HP (nm)	29	22	17	12.8	9.7
Physical gate length for LOP (nm)	32	24	17	12.8	9.7
Physical gate length for LSTP (nm)	38	27	17	12.8	9.7
EOT for HP (nm)	1.32	1.06	0.82		
EOT for LOP (nm)	1.64	1.18			
EOT for LSTP (nm)	1.83	1.33			
$J_{G,limit}$ for HP (A/cm^2)	650	1000	1300		
$J_{G,limit}$ for LOP (A/cm^2)	0.09	0.13			
$J_{G,limit}$ for LSTP (A/cm^2)	86	110			
NMOS I_{on} for HP (mA/mm)	1210	1300	1680		
NMOS I_{on} for LOP (mA/mm)	700	798			
NMOS I_{on} for LSTP (mA/mm)	536	664			
μ enhancement factor by strain	1.8	1.8	1.8	1.8	1.8
Effective ballistic enhancement factor	1	1	1.19	1.42	1.69

: manufacturable solutions are not known

I_{off} then I_{on} decreases exponentially and so on. This is largely due to the quantum mechanical tunneling limitation on leakage currents and the thermodynamic limitation on the subthreshold behavior of the nano-scaled MOSFET approaching a few atomic layers' scale.

There are primarily two forms of tunneling leakages (J_{tunnel}): tunneling current through the gate dielectric and tunneling current through the drain-to-body junction, called band-to-band tunneling (BTBT). The first tunneling current varies exponentially as follows:

$$J_{tunnel} \sim \exp\left(-\frac{d}{d_o}\sqrt{m^*\theta_{barrier}}\right) \tag{1.2}$$

where d is the dielectric thickness, $d_o \approx 0.1$ nm, m^* is the effective mass in the barrier, and $\theta_{barrier}$ is the barrier height between the dielectric and the substrate channel in carrier transport [11]. The use of high-k dielectric instead of using a thinner dielectric can mitigate this issue and semiconductor industries have implemented high-k with metal gate to reduce EOT further eliminating poly-Si depletion effect. The other type of quantum mechanical tunneling affecting operation of MOSFET is BTBT at the drain end of the channel. Since the gate potential significantly modulates the BTBT current, it is often referred to as gate-induced drain leakage (GIDL) [11]. This occurs when $V_{DS} \geq E_g - \theta_{barrier}$ where V_{DS} is the drain to source voltage and E_g is the bandgap of Si. The band diagram of the off-state in a nano-scaled MOSFET is illustrated with a schematic of short channel FET structure in Fig. 1.7 [12, 13]. This BTBT current varies as $\exp(-L_{B2B}/\lambda_T)$, where L_{B2B} is the minimum physical distance from a point in the conduction band to a point in the valence band at the same energy, and $\lambda_T = 0.38$ nm, which is the characteristic length scale for the tunneling [13]. It has been reported that the BTBT current becomes dominant when the tunneling distance reduces to ~4

nm. This is typically ~1/3 of the channel length, which sets the minimum channel length to 12 nm.

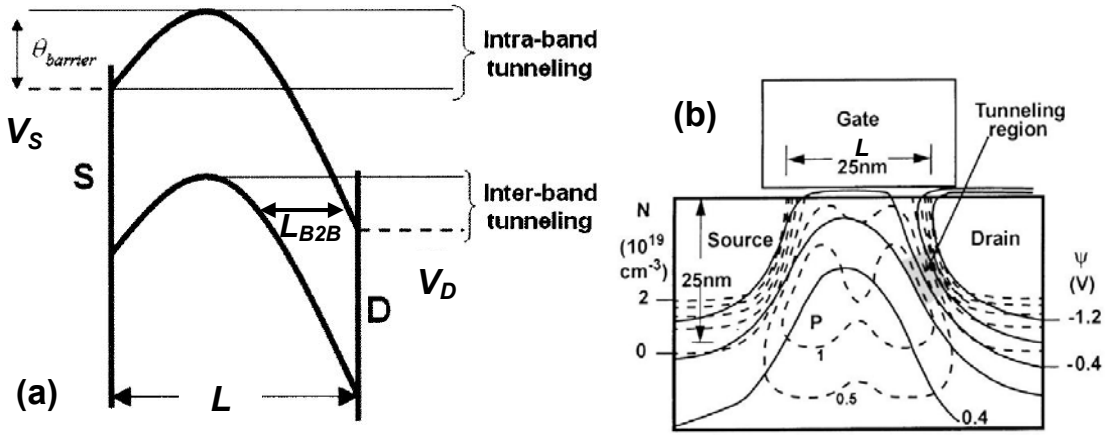


Fig. 1.7 (a) Band diagram in the off-state of an extremely scaled MOSFET indicating quantum mechanical tunneling mechanism. [12] (b) Advanced 25 nm gate-length FET structure showing the BTBT tunneling region. Solid contours are electrostatic potential, in 0.2 V intervals, and dashed contours indicate doping, in $5x10^{18}$ cm^{-3} intervals with open contours being n- type and closed contours p-type. Region of the shortest tunneling distance is shaded. [13]

In addition, the leakage current can be dominated by the direct tunneling from the source to the drain due to intra-band tunneling when $k_BT/q \leq \eta/\pi \cdot \sqrt{\alpha / 2m^*q}$, where α is the curvature of the bend bending which is related to the geometry of the device through the channel length, L, the effective barrier $\theta_{barrier}$, V_D: η is the ideality factor, m^* the effective electronic mass, q the electronic charge, k_B Boltzmann's constant, and T temperature [12]. For Si, $L \geq$ 7 nm is required to avoid the tunneling effect on the leakage current of a MOSFET when assuming $0.19m_o$ for m^*, 1.2 eV for $\theta_{barrier}$, and 0.5 V for V_D [12] while the other group estimates the minimum L of 4 nm assuming a square barrier [14].

The subthreshold current is another significant challenge that limits scaling because of the fundamentals of thermodynamics. The subthreshold current of a MOSFET originates in the high-energy tail of the statistical distribution of carriers in

its source region. Hence the SS has a fixed value depending on temperature and V_{th} of the MOSFET, more precisely the behavior of carrier diffusion at the source end of the channel. The subthreshold current varies exponentially with gate voltage as

$$I_D = I_{vt} 10^{\frac{(V_G - V_{th})}{S}} \tag{1.3}$$

where S is the SS and I_{vt} is the current at V_{th}. An equation for S is

$$S = n \frac{k_B T}{q} \ln 10 \tag{1.4}$$

where

$$n = 1 + \frac{C_d}{C_{ox}} \tag{1.5}$$

for an ideal interface which is free of surface trapping. C_d is the surface depletion-layer capacitance. Even if n is almost unity, V_{th} cannot be scaled without changing I_{off}, which is I_D at V_G = 0, unless T is scaled. Because I_{off} limits the scaled MOSFET, thermodynamics, i.e. S sets the lower limits of V_{th} and V_{dd} accordingly. Figure 1.8 depicts this relationship in a schematic I_D-V_G curve of MOSFET.

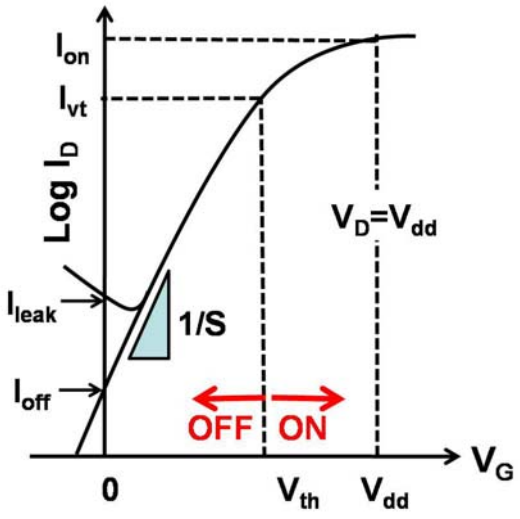


Fig. 1.8 Schematic I_D-V_G characteristic in log scale showing the factors affecting electrical parameter requirements.

1.2 APPROACHES FOR SCALING BEYOND THE 10 NM NODE

Fundamental limitations mentioned above have prompted researchers to investigate alternative materials and innovative MOSFET architectures to extend the roadmap of scaling beyond the gate length below 10 nm. The promising solutions include: (1) the high-*k* gate dielectric/metal gate stack to increase I_{on} and decrease I_{leak}; (2) the non-planar device structure to reduce junction leakage current and SCE; (3) the mobility enhancement using classical Si-based CMOS material to increase I_{on}; (4) the advanced channel material adoption to increase I_{on}.

1.2.1 HIGH-*k* GATE DIELECTRICS AND METAL GATE

Dielectrics with higher permittivity are essential to provide for the reduced T_{ox} without reducing the physical thickness of the dielectric material. There have been tremendous researches to find and develop a suitable high-*k*/metal gate stack to replace SiO_2/poly-Si stack, which is compatible with manufacturable CMOS technology with scalability. The introduction of high-*k* needs to satisfy certain criteria, such as being stable in contact with Si, being able to cope with a conventional thermal process, having band offsets over 1 eV for both conduction and valence bands, having an oxide interface which suppresses charge trapping centers, and not degrading the mobility of carriers in the MOSFET channel. After almost a decade of intense research, the family of hafnium-oxide-based materials, such as HfO_2, $HfSi_xO_y$, HfO_xN_y, and $HfSi_xO_yN_z$, emerges as a leading candidate in advanced CMOS applications [15–17] and the requirements for high-*k* introduction have now largely been solved. For example, the problem of mobility degradation, whether it is due to optical phonon scattering or remote charge scattering, is turned out to be partly a matter of reversible fast transient charge trapping affecting the mobility measurement [18].

However, it is reported that further scaling according to the device roadmap (Table 1.1) requires the development of high-*k* dielectrics with higher *k* values than 26 with ~5.0 eV bandgap, in order to scale EOT to ~0.5 nm [18]. In this projection, it is assumed that the minimum physical thicknesses of high-*k* and the interfacial SiO_2 are 1.2 and 0.3 nm, respectively [19]. Figure 1.9a indicates that the gate leakage current increase for ultrathin high-*k* (EOT < 1nm) is significantly dependent on E_g almost due to quantum mechanical tunneling. Figure 1.9b thus shows some available high-*k* materials [20]. In addition, it is strongly desired to develop an amorphous high-*k* dielectric rather than crystalline material because the thin physical thickness of sub-nm is required, where the grain boundary can be a considerable leakage source. Various dielectrics including ternary rare-earth metal oxides have been explored for the higher-*k*. However, the ternary rare-earth metal oxides have not concluded yet as the high-*k* material solution due to their chemical and thermal stability for MOSFET process [21, 22]. For example, amorphous $LaLuO_3$ showed a promising dielectric constant of 32 with a high E_g of ~5.5 eV [21], but the lanthanide elements diffused into the SiO_2 interface or the Si channel degrade the performance of devices [18].

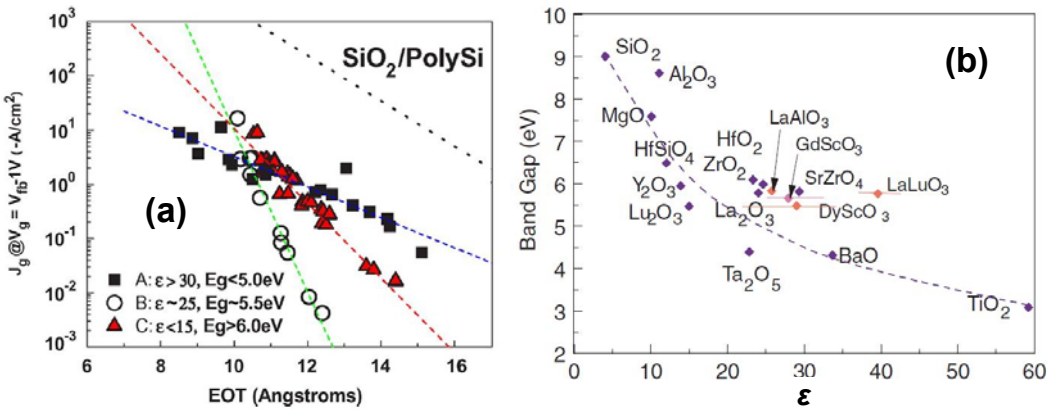


Fig. 1.9 (a) J_G as a function of EOT for three different high-*k* layers with various dielectric constants (shown as ε) and E_g [18]. (b) E_g vs ε for candidate high-*k* oxides for MOSFET scaling [20].

Another challenge on high-*k* replacing SiO_2 dielectric is related to the gate electrode material. Use of metal gate electrode instead of the doped poly-Si gate electrode would eliminate the poly-gate depletion effect (equivalent to ~0.3-0.4 nm-thick parasitic capacitor [24]) resulting in easier EOT scaling. In addition, the metal gate electrode can provide another benefit of low sheet resistance of the gate electrode. In order to achieve a suitable and symmetrical V_{th} for NMOSFET and PMOSFET, the metal gate electrode material must have a work function energy close to that of the Si conduction or valence bands, of 4.05 eV and 5.15 eV for NMOSFET and PMOSFET applications, respectively [25]. Recently, there are two approaches for changing n-type and p-type doped poly-gate electrodes into metal gates in a scaled CMOS device: a single midgap metal like TiN [26] or TaN [27] with different high-*k* dielectrics using a capping layer on the high-*k* [28, 29] and two kinds of metal with different metal work functions with a single dielectric [30]. However, the research on metal electrode has been quite empirical due to the lack of understanding of the high-*k*/metal gate system and the drawback of each approach significantly limits further scaling. The first approach adds an extra EOT due to the capping layer and the second one causes an integration problem due to the complexity of the processes and low thermal budget. It is reported that the flatband voltage (V_{FB}) of p-type metal electrode decreases with T_{ox} resulting in a low work function in a thin EOT region [31]. To solve this V_{FB} roll-off phenomenon, intensive works have been carried out theoretically and empirically but no solution has been published yet [18]. The difficulty to control V_{th} results from chemical reactions between the electrode and dielectric, causing defects and oxygen vacancies near the interface [32]. Most of metals are thermally unstable at high temperature: they either spike through the thin high-*k* dielectric as in the case of metals with work functions appropriate for NMOS, or they interact with the oxygen vacancies

in the high-*k* dielectrics, resulting in large V_{FB} shifts, as in the case of metals with work functions appropriate for PMOS [22]. In order to mitigate the concern over the thermal instability, the low temperature process scheme, called "gate-last" process has been proposed and developed in contrast to the conventional "gate-first" integration scheme. In this gate-last process, the activation of S/D is carried out before forming the high-*k*/metal gate stack, causing the integration process to become complex due to dummy processes [30] and also misalignment issues between the gate and S/D, limiting scalability of CMOS for both cases. On the other hand, the advantages of the gate-first process are the elimination of complex polishing steps, retention of channel strain in both NMOS and PMOS transistors, and scalability potential for future technology nodes. Intel used gate-last approach at 45 nm technology [30] while IBM developed the gate-first scheme at 32 nm node [33] in its production, and both manufacturers adopted Hf-based oxide for the high-*k* dielectrics.

The greatest concern for further EOT scaling originates from the unavoidable interfacial SiO_2 layer (0.3-0.5 nm for 1 or 2 atomic layers) between the high-*k* dielectric and the Si channel. However, eliminating or scaling the thickness of the interfacial SiO_2 results in mobility and reliability degradation [18, 22, 23]. Therefore it is critical to make use of mobility enhancement technique with an interface engineering, ensuring that the high-*k*/metal gate stack will not severely degrade the mobility of the deeply scaled CMOS devices.

1.2.2 NON-PLANAR MOSFET STRUCTURE

In order to control the SCE and to set the V_{th} properly, the channel doping has to be increased to an undesirably high value. This results in the degradation of electron and hole mobility in the channel due to increased impurity scattering and the increase

of the SS, BTBT, and GIDL leading to higher junction leakage [10]. In order to mitigate these undesirable effects, non-planar MOSFET structures have been proposed and under development for possible replacement of the bulk planar MOSFET. The non-classical MOSFET structures can be divided into two categories: the ultrathin body (UTB) MOSFET and the multiple-gate MOSFET.

The UTB is fabricated on a silicon-on-insulator (SOI) substrate with a small thickness of the Si semiconductor body. The SOI structure offers lower parasitic capacitance at the S/D regions and the better control toward SCE by reducing the body thickness. If the top Si film thickness is thinned down so that the semiconductor film under the gate is completely depleted in the off-state of the device, then it is referred to as a fully depleted SOI (FDSOI) MOSFET. The advantages of FDSOI which has the thinner body over partially depleted SOI (PDSOI) include eliminating the floating body effect, making the circuit design easier, and reducing the drain capacitance because the drain-to-body junction is greatly suppressed [11, 34]. Thanks to the better control to SCE, FDSOI can reduce the channel doping concentration so that the switching speed can be increased with the increased inversion layer mobility and without the expense of I_{off}. The SS can be improved near the ideal value of 60 mV/dec by optimizing the fabrication processes, as shown in the example of FDSOI (Fig.1.10) [35]. Hence the UTB FDSOI MOSFET provides better scalability than bulk Si device.

Another MOSFET structure to control the SCE is the multiple-gate MOSFET in which the gate control on the channel is increased by geometrically placing the gate as close to the channel. There can be double, triple, quadruple, and even cylindrical gates as seen schematically in Fig.1.11. The tighter gate coupling may be achieved by increasing the number of gate from single-gate FDSOI to multiple-gate. Since the gate control is increased with the multiple-gate, the requirements on the Si body thickness

can be relaxed as compared to the FDSOI at the same L_G to achieve comparable I_{off}. Although each of the multiple-gate structures has been proposed with various fabrication procedures [36-39], all of them are much more difficult to make than conventional MOSFETs [11]. Experimentally, the FinFET, where the channel is formed in a vertical Si fin and controlled by self-aligned gates on its two sides made on SOI substrate, is an attractive multiple-gate architecture in terms of its simple fabrication, and is under research and exploration [40, 41].

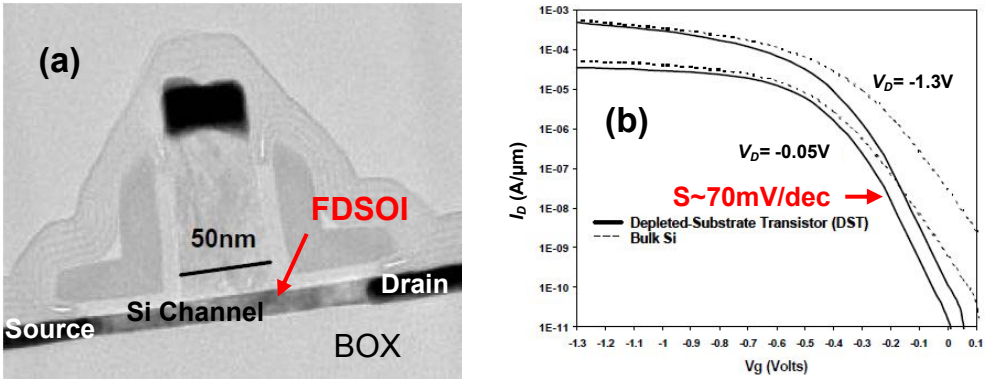


Fig. 1.10 (a) TEM image of UTB FDSOI transistor (b) I_D-V_G characteristics of the UTB FDSOI PMOSFET with the gate length of 70 nm in comparison with bulk Si PMOSFET. [35]

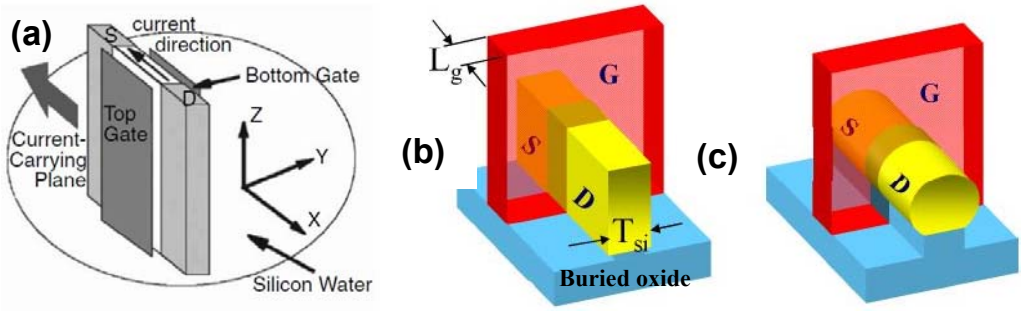


Fig. 1.11 Schematic illustrations of multiple-gate FETs. (a) Vertical double-gate FET [11], (b) triple-gate, and (c) nanowire FinFET structure. [47]

Based on the superior control over the SCE, the non-planar MOSFET structure can further extend the CMOS scaling to the smaller L_G region as predicted by ITRS in

Table 1.2 High-performance (HP) logic technology requirements where the transistor types include the UTB FDSOI and multiple-gate CMOSFET as well as the planar bulk structure. [10]

(MPU: microprocessor unit; EOT: electrical equivalent oxide thickness; $J_{G,limit}$: the maximum allowed gate leakage current density at $V_G=V_{dd}$ and 25 °C; I_{on}: I_D at $V_G=V_D=V_{dd}$; Effective ballistic enhancement factor: a multiplying factor for I_{on} to meet the I_{on} required, which is largely due to quantum effects on mobility.)

Year of Production	***2009***	***2012***	***2015***	***2018***	***2021***
MPU Metal 1 ½ Pitch (nm)	54	32	21	15	10.6
Physical gate length for HP (nm)	29	22	17	12.8	9.7
EOT for planar bulk (nm)	1.32	1.06	0.82		
EOT for UTB FD (nm)			1	0.94	
EOT for multiple-gate (nm)			1.17	1.04	0.97
$J_{G,limit}$ for planar bulk (A/cm^2)	650	1000	1300		
$J_{G,limit}$ for UTB FD (A/cm^2)			1300	1700	
$J_{G,limit}$ for multiple-gate (A/cm^2)			1300	1700	2200
NMOS I_{on} for planar bulk (mA/mm)	1210	1300	1680		
NMOS I_{on} for UTB FD (mA/mm)			1670	1830	
NMOS I_{on} for multiple-gate (mA/mm)			1490	1790	2000
μ enhancement factor by strain	1.8	1.8	1.8	1.8	1.8
Effective ballistic enhancement factor	1	1	1.19	1.42	1.69

: manufacturable solutions are not known

Fig.1.12 and Table 1.2 [10] compared to Table 1.1. However, to extend the scaling to beyond 10-nm-node, the body thickness well below 10 nm is projected and the impactof quantum confinement and surface scattering effects on such thin devices should be well understood.

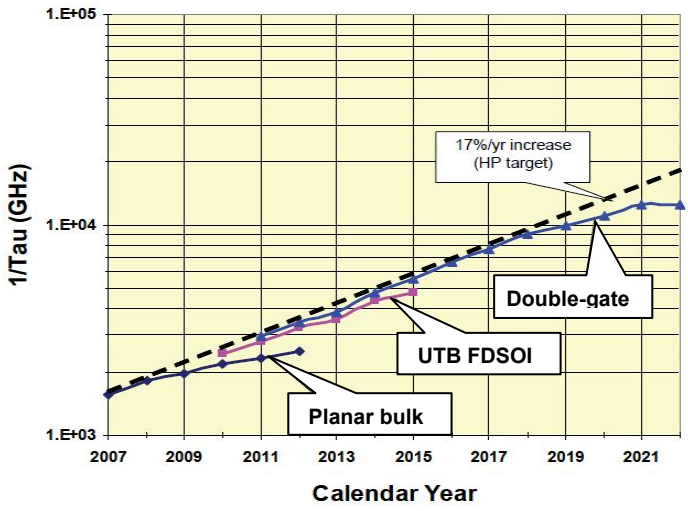


Fig. 1.12 Projection of the scaling of HP logic transistor intrinsic speed, 1/τ with different MOSFET structures. [10]

1.2.3 MOBILITY ENHANCEMENT TECHNIQUES

Since the CMOS scaling is now facing enormous challenges in the conventional scaling of physical dimensions including T_{ox}, researchers are now more attracted to the mobility term in the equation 1.1. Since the first mobility enhancement demonstration of strained-Si MOSFETs by Stanford group in 1992 [42], strained-Si channel technologies have made a steady and continuous progress and have been implemented in high volume manufacturing from 90 nm technology node [7]. One of the most innovative and successful performance boosters in CMOS scaling is the mobility enhancement using process-induced strained-Si channels due to its cost-

effective performance enhancement without any significant expense of other device parameters like I_{off}.

Strain is the mechanical response to an external stress and responsible for all the changes in the energy band structure and density of states. Strain can be introduced biaxially or uniaxially in Si depending on the process used to stress the channel. The mobility enhancement is basically understood as the subband-structure engineering caused by strain-induced band splitting. The Si conduction band is comprised of six equivalent valleys located at the X symmetry point in a Brillouin zone, with a transverse mass of $0.19m_o$ and a longitudinal mass of $0.92m_o$ as shown in Fig.1.13. When tensile stress is applied along the channel direction (compressive perpendicular to the interface) band splitting occurs between the four-fold Δ_4 valleys and the two-fold Δ_2 due to quantization. This causes an increase of electron occupancy in the Δ_2 valley with the smaller effective mass leading to an increased mobility. Furthermore, it has recently been reported that the uniaxial strain along <110> can reduce the effective mass of the Δ_2 valleys on (100) surfaces, which is expected to further increase I_{on} in scaled strained-Si channel [43].

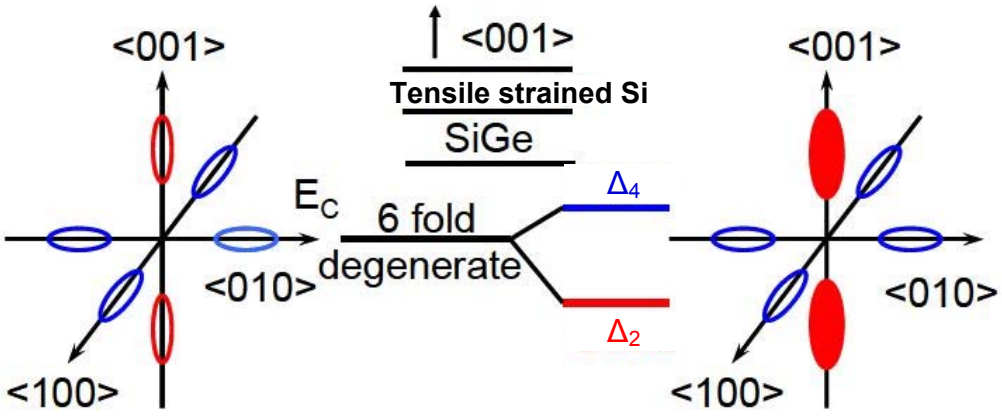


Fig. 1.13 Strain effect on conduction sub-bands of (001)Si.

Figure 1.14 shows two approaches to introduce the strain to the MOSFET channel. The development of strained-Si MOSFETs started with introducing biaxial strain using global strain technologies (Fig. 1.14a). The channel can be biaxially strained by growing Si channel on a relaxed $Si_{1-x}Ge_x$ buffer, which has a larger lattice constant than Si. Although the superior performance enhancement including mobility increase has been reported with various global strain technologies [42, 44, 45], this strained-Si technique has not been implemented to manufacturing due to the high substrate cost and inadequate material quality, such as dislocations and defects remaining in the substrates [46]. The more efficient uniaxial strain has been implemented by local strain technologies, in contrast to the global strain technologies, like SiGe-embedded S/D [7-9, 30] as schematically illustrated in Fig. 1.14b [47].

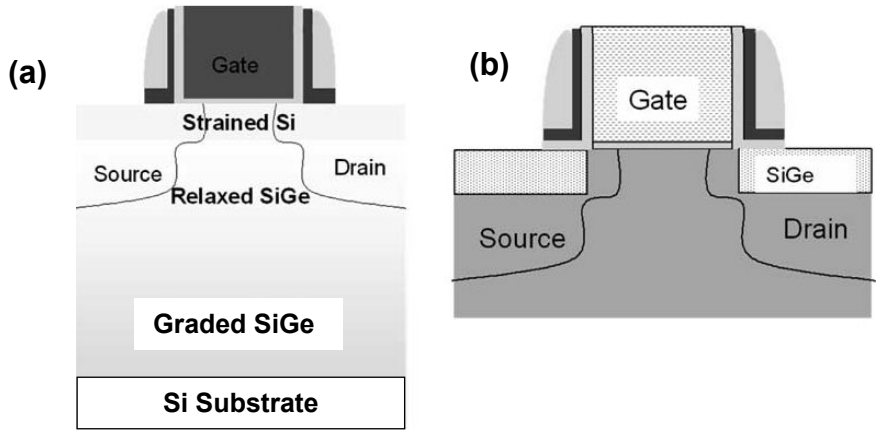


Fig. 1.14 Schematic showing the device cross section of (a) globally strained channel transistor and (b) local SiGe stressor next to gate. [47]

These local strain technologies include process-induced strain technique using shallow trench isolation (STI) [48], silicide formation [49], tensile/compressive nitride capping layer [7, 30, 50], and stress memorization techniques [51]. Although the local strain technology provides a much improved mobility enhancement compatible with a high volume production technology than the global strain technique, the amount of

stress decreases with the technology nodes due to the strong dependency on the transistor geometry. For instance, Intel has implemented a tensile nitride capping layer as a stressor for NMOS at 90 nm node but not at 45 nm node because of the reduced spacing between the gates, and changed Ge fraction in the SiGe-embedded S/D stressor from 17 % to 30 % for PMOS [52]. This strong dependence drawback on the geometries of the transistors may result in process complexity which eventually makes the local strain techniques to be not so effective in further scaling the MOSFETs [53, 54].

1.2.4 ADVANCED CHANNEL MATERIAL ENGINEERING

As predicted the saturation of the mobility enhancement due to strained-Si technologies and the carrier transport mechanism approaching ballistic regime for extremely scaled MOSFETs, alternative channel materials with light m^* including Ge and III-V semiconductors have been actively explored with the benefits of enhanced thermal velocity and injection at the source end. The theoretical background in choosing the alternative channel material of MOSFET is usually based on the scattering theory which has developed the carrier transport mechanism considering quasi-ballistic or ballistic transport in addition to the stationary carrier transport, which is dominant in long channel MOSFET. According to Lundstrom's scattering theory [66], the drain current of short channel MOSFET in saturation can be given as

$$I_{Dsat} = WC_{ox}v_{inj}\left(\frac{1-r}{1+r}\right)\left(V_G - V_{th}\right) = WqN_s^{source}v_{inj}\left(\frac{1-r}{1+r}\right) \tag{1.6}$$

where v_{inj} is injection velocity at the top of the barrier near the source edge, r is the backscattering rate near-source region, and N_s^{source} is the surface carrier concentration

near the source edge. The backscattering coefficient, r can be calculated from the mean free path λ and the critical distance l over which the channel potential drops by k_BT/q

$$r = \frac{l}{l+\lambda} \tag{1.7}$$

where $$l = \frac{k_B}{qE_s} \text{ and } \lambda = \tau\sqrt{\frac{2\pi k_B T}{m^*}} \tag{1.8}$$

with $E_s \approx V_D/L$ being the electric field (in the direction of transport) at the source end of the channel. In the ballistic limit $r = 0$, where the ballistic coefficient, $B = (1 - r)/(1 + r) = 1$, the maximum current is controlled by the injection velocity at the thermal source. These transport models by the channel length are illustrated in Fig. 1.15 [46]. Although it is expected that the importance of mobility vanishes as the transport mechanism approaches the full ballistic transport, still the mobility needs to be large because both velocity and mobility depend on m^* and, therefore, are correlated.

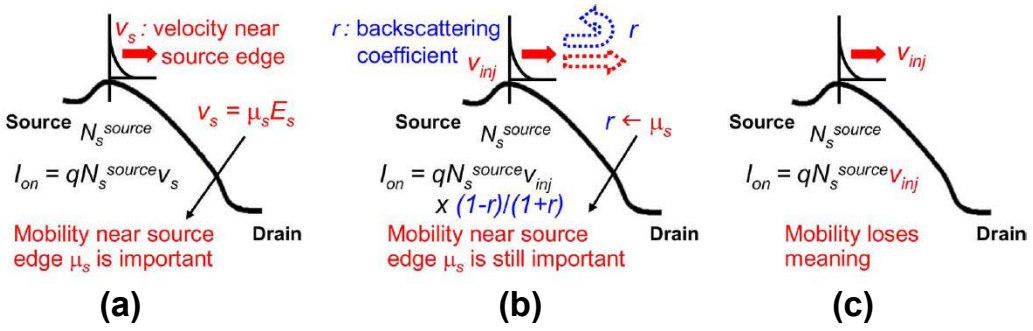


Fig. 1.15 Illustrations of carrier transport models to determine I_{on} (I_{Dsat}) as varying the channel length based on the scattering theory [55]. (a) Conventional transport in a long channel MOSFET. (b) Quasi-ballistic transport model for a short channel MOSFET. (c) Full ballistic transport model for an extremely short channel MOSFET [46].

By using new materials in the channel, which have lower carrier m^* in the channel length direction, higher drive current can be achieved in extremely scaled MOSFETs. Physical parameters of some promising candidates are listed in Table 1.3, including their carrier mobilities, bandgap, permittivity, conduction band minima

effective mass, and the thermal velocities [56]. Comparing to Si, Ge has higher mobility for both electron and hole. The compressively strained Ge channel has been recognized as a promising candidate for high-performance PMOSFETs [57, 58]. However, it has been reported so far that the performance of Ge NMOSFETs is very poor and the inversion-layer mobility of electrons has been even smaller than that of Si NMOSFETs [59]. Recent research result shows that the high interface state density (D_{it}) near the conduction band edge, high S/D parasitic resistance, and inversion charge loss due to trapping have been identified as the mechanisms responsible for Ge NMOS performance [60], and also Ge NMOSFET is not so attractive compared to III-V NMOSFET due to the technical issues.

Table 1.3 Physical and electrical parameters of selected semiconductors [56].

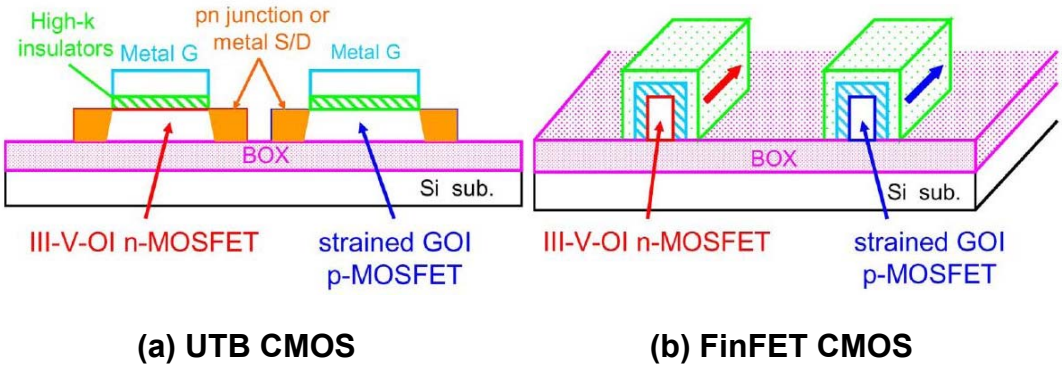
	Si	Ge	GaAs	$In_{0.53}Ga_{0.47}As$	InAs
Electron mobility, μ_e (cm^2/Vs)	1400	3900	8500	12000	40000
Effective electron mass ($/m_o$)	m_l:0.98 m_t:0.19	m_l:1.6 m_t:0.08	0.063	0.041	0.023
Hole mobility, μ_h (cm^2/Vs)	450	1900	400	300	500
Effective hole mass ($/m_o$)	m_{HH}:0.49 m_{LH}:0.16	m_{HH}:0.33 m_{LH}:0.043	m_{HH}:0.51 m_{LH}:0.082	m_{HH}:0.45 m_{LH}:0.052	m_{HH}:0.41 m_{LH}:0.026
Electron affinity (eV)	4.05	4.0	4.07	4.5	4.9
Energy bandgap (eV)	1.12	0.66	1.42	0.74	0.35
Electron thermal velocity (cm/s)	2.3×10^7	3.1×10^7	4.4×10^7	5.5×10^7	7.7×10^7
Hole thermal velocity (cm/s)	1.65×10^7	1.9×10^7	1.8×10^7	2×10^7	2×10^7
Dielectric constant	11.7	16.2	12.9	13.9	15.15
Lattice constant (Å)	5.43	5.66	5.65	5.869	6.058

Superior electron transport properties of III-V materials render them suitable as a potential candidate for high-speed NMOSFETs beyond strained-Si devices. In fact, the higher channel mobility with an enhancement factor of more than 4 can relieve the other tough requirements such as I_{on}, EOT and I_{off} for further scaling regime where there is no certain solution with Si so far.

There are some concerns on the intrinsic properties like intervalley scattering and high dielectric constant related to quantum confinement effects and tunneling effects for extremely scaled III-V NMOSFETs [46, 61]. On the other hand, it has been reported that the optimum design of S/D doping profile and ohmic contacts in III-V NMOSFETs can mitigate the drawbacks and outperform Si and Ge counterparts showing a good scalability [62]. Because those simulation-based estimations have posited an ideal high-*k*/metal gate stack on III-Vs, these technological challenges have drawn attraction for many researchers to search for thermodynamically stable gate dielectrics which can form unpinned Fermi level at the III-V/oxide interface. Despite the recent advancements in improving the high-*k*/III-V interface quality [63, 64], the performance of III-V FETs has yet to meet the expectation remaining the issues of compatibility with CMOS processes. These efforts include advanced high-*k* deposition techniques like *in situ* molecular beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD) and atomic layer deposition (ALD), the use of various interface passivation techniques. These studies will be reviewed in detail in Chapter 3 and 4.

In addition, to realize the deeply scaled MOSFETs with these high mobility materials, the device structure should be non-classical due to SCE as seen in the case of Si devices in the previous section. The gate stack should be high-*k*/metal gate stacks to maintain I_{off} low enough. As a consequence, many research groups have proposed the future ideal device structure as the one combining the carrier-transport enhanced

channels with UTB or multiple-gate configurations as illustrated in Fig. 1.16 [10, 46, 65].



(a) UTB CMOS **(b) FinFET CMOS**

Fig. 1.16 Ultimate CMOS structure composed of III-V NMOSFET and Ge PMOSFET [46]. (a) UTB platform (b) Multiple-gate architecture CMOS.

To achieve CMOS high performance, co-integration of different materials (i.e. III-V and Ge) on silicon may be necessary. However, formation of a crystalline quality thin III-V channel layer on Si substrate is a very difficult challenge due to the large lattice mismatch between III-V and Si over than 4 %. Recently, there has been a direct wafer bonding approach to build III-V-on-insulator (III-V-OI) demonstrating high mobility in NMOSFET devices [66], but it may add complexity of fabrication processes to integrate Ge PMOSFET together and have difficulty to apply on 300 mm or 450 mm large Si wafers.

Other possibilities beyond these alternative channel materials of Ge/III-Vs are low-dimensional materials such as carbon nanotube (CNT) and graphene nanoribbon [10]. These low-dimensional carbon nanomaterials may offer high thermal conductivity, high mobility, and ballistic electronic transport [67, 68]. Key challenges for CNTs to be viable in high performance FETs are the requirements for processes that provide a tight distribution of semiconductor bandgaps, with each nanotube placed in a desired location, with a specified direction, low contact resistance, and catalyst

compatible with CMOS. Among the carbon nanomaterials, graphene, a monolayer to a few layers of sp^2 bonded carbon in a honeycomb lattice, has been studied intensively since its discovery in 2004 [67] due to its unique electron physics, as well as possible applications to electronic devices. Especially, graphene and related graphitic structures have high mobility without alignment challenges. Without the alignment challenges graphene exhibits ambipolar carrier conduction [69], a carrier mobility as high as ~ 2×10^6 cm^2/Vs, and a defect density of ~$1\times10^{10}/cm^2$ [70]. Although the superior transport characteristics, the maturity of process technology is too far to integrate graphene in CMOS platform. The difficult challenges include: processes capable of depositing carbon nanomaterials on a CMOS compatible substrate, ability to deposit atomically uniform thicknesses of films, pattern and etch with low edge defect, development of basic fabrication techniques such as doping, contacts, etc., and integration with CMOS-compatible processes. Consequently, compared to the accumulated knowledge on theoretical and experimental works of Ge and III-V, carbon nanomaterials need much intensive researches for their device applications.

1.3 MOTIVATION AND OBJECTIVES

As devices are scaled beyond the 10 nm node, various architectural and material changes in the traditional Si-based MOSFET would be required for efficient operation of the transistor. As reviewed above, high-*k*/metal gate stacks on Ge and III-V channels with UTB or multiple-gate structure can offer the potential to extend the historical CMOS scaling beyond 10 nm. III-V MOSFET has been studied with a great deal of attention in the 1980s but the difficulty in the integration of MOS structure has caused the lost in interests. However, with the advanced high-*k* deposition technology, which enables the deposition at ultrahigh vacuum (UHV) and low temperature,

available now, it is the time to find the solution for III-V MOSFET integration again. The recent simulation works with double gate or UTB structure support this vision showing higher I_{on} and faster switching speed with scalability in ~10 nm L_G regime [62, 71].

However, there are many challenges to be settled to realize the ultimate CMOS structure composed of Ge PMOSFET and III-V NMOSFET. First, the formation of high-quality III–V materials on Si, SiO_2, or Ge-on-insulator (GOI) is mandatory [10, 46]. As shown in Table 1.3, most of the III-V semiconductors have larger lattice constants than Si. Hence direct epitaxial growth of III-V on Si causes defective film due to the large lattice mismatch. Among the enormous experimental approaches, the heteroepitaxy using Ge or graded $Si_{1-x}Ge_x$ buffer layers may provide a solution for the III-V and Ge integration on Si because SiGe/Ge system has landed well on CMOS technology. So far the heteroepitaxy has been carried out on Si bulk substrate with a very thick SiGe buffer layer over than a few μm [72]. Hence we have aimed to realize III-V heteroepitaxy on SOI with a thin SiGe buffer using a novel Ge condensation technique, which may enable III-V-on-insulator substrate structure. Ge condensation method is useful to fabricate $Si_{1-x}Ge_x$-on-insulator (SGOI) of high Ge fraction up to GOI using conventional SiGe epitaxy and oxidation processes which are very compatible with the present CMOS fabrication process [73].

Another difficult challenge for III-V MOSFET is the long-standing problem of passivation the defects that inevitably form between deposited gate insulators and III-V channel materials. A great deal of literature on the research of interface physics and chemistry of III-V/dielectric system has been reported [63, 64, 74]. Due to surface oxygen-related reaction, interfacial lattice defects, and stoichiometry perturbation, high interface state densities (D_{it} between 10^{12} - 10^{14} $cm^{-2}eV^{-1}$) between III-V and

dielectrics and Fermi level pinning have been commonly observed throughout the literature. In spite of the prominent endeavor in theoretical and experimental studies, still the realized electron mobility in inversion layer of III-V MOSFET has been far below its expectation resulting in the low performance of inversion mode NMOSFETs (Fig.1.17 [75]). The research on III-V MOSFET should be carried out using the state-of-the-art high-*k* deposition and surface passivation technology to understand the underlying physics and chemistry based on the experimental breakthrough. Those gate stack formation techniques, therefore, should include Hf-based high-*k* deposition, optimum pre-deposition chemical cleaning, and *in situ* surface passivation using novel materials. Accordingly, our second purpose of this study was to develop a new gate stack integration framework for III-V MOSFETs based on the state-of-the-art high-*k* deposition technology and compatible with CMOS manufacturing system. In addition, we aimed to develop a robust material approach for the interface engineering of III-V MOSFETs.

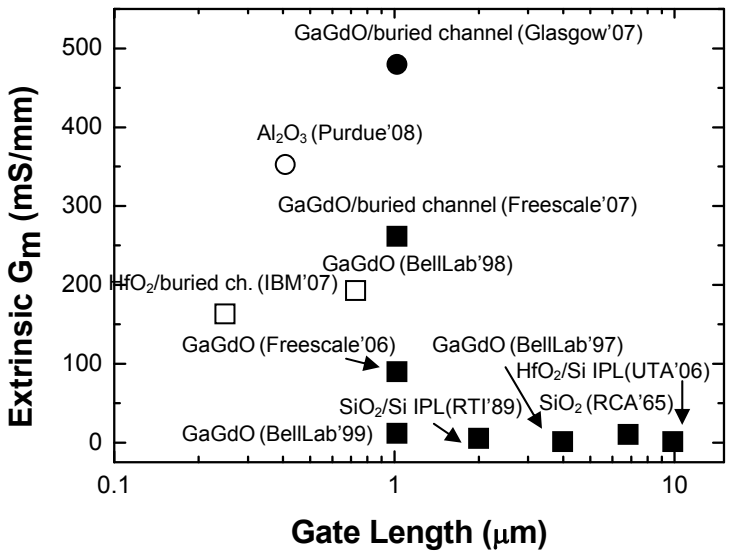


Fig. 1.17 Historical comparison of published dc transconductance, G_m of E-mode NMOSFETs from 1965 to 2008. Open symbols are high indium concentration channels of InGaAs (In≥0.53), whereas closed symbols are GaAs or InGaAs with low indium concentration channels. [75]

The research activities presented here are limited to GaAs-based III-V material. It should be mentioned that this research field has grown exponentially since about 2005, when our study has been initiated so that our study has contributed to the society in the time context. Even though the extrinsic parameter engineering to reduce series resistance between S/D and channel is also critical to demonstrate high mobility III-V NMOSFETs, this is beyond the scope of this study.

1.4 THESIS OUTLINE AND ORIGINAL RESEARCH CONTRIBUTIONS

In summary, to develop high mobility III-V channel layer formation technology for MOSFET devices in 10 nm node and beyond, important issues should be addressed and developed: (1) heteroepitaxial growth technique for GaAs-OI on Si platform; (2) identification and demonstration of III-V channel NMOSFET integrated with high-*k* and metal gate; (3) new material approach to passivate III-V surface for high thermal budget CMOS fabrication processes. In addition, these developments should be carried out on the basis of compatibility with Si-based CMOS manufacturing processes due to its effectiveness of process cost and time for research and development. These aspects were aimed to be explored and developed in this thesis with the hope that those can provide intuitive guidance and information for further scaling of CMOS with the carrier-transport enhanced channel materials.

Following this introduction chapter, Chapter 2 presents the technology to grow GaAs heteroepitaxial layer on SOI substrate using MBE and Ge condensation method. The GaAs-OI has been demonstrated with a device-quality in cost-effective fabrication processes and on Si platform, for the first time. The graded SGOI virtual substrate

formation technique would be useful to integrate the future PMOS on GOI and NMOS on GaAs-OI simultaneously on a large scale Si wafer.

Chapter 3 describes the chemical and physical properties of the interface to develop Hf-based high-*k* gate stack on GaAs-based III-V channel using MOCVD. The study of high-*k* material effects on GaAs and InGaAs III-V substrates is discussed. NMOSFET fabrication processes, such as pre-deposition cleaning and S/D activation, are examined to realize high electron mobility performance of the III-V NMOSFET with the high-*k*/metal gate stack in a self-aligned gate-first fabrication scheme.

In Chapter 4, a novel passivation technique using *in situ* PH_3 treatment is proposed, explored and investigated for InGaAs NMOSFET integrated with high-*k*/metal gate stack. For the first time in this field, it is found that phosphorus nitride (P_xN_y), a novel passivation material, which is composed of group V elements in covalent bonds, is formed on InGaAs substrate using PH_3-N_2 plasma in a wide range of process window and greatly improves electrical properties of the MOSFET devices. The improved interface quality is identified with physical, chemical, and electrical properties, demonstrating a high mobility NMOSFET with InGaAs/HfAlO/TaN gate stack integrated in self-aligned gate-first scheme. Thermal stability of the passivated interface is examined under different annealing conditions as well.

Consequently, Chapter 5 summarizes the results of cost-effective substrate and interface engineering techniques for GaAs-based III-V NMOSFET for CMOS applications and provides some suggestions for the possible further research in this area.

References

[1] D. Kahng and M. M. Atalla, “Silicon-Silicon dioxide field induced surface devices,” in *IRE Solid-State Device Research Conference*, Carnegie Inst. of Tech., Pittsburgh, 1960

[2] R. S. Muller, T. I. Kamins, and M, Chan, *Device Electronics for Integrated Circuits*, 3rd Ed., New York: Wiley, 2003, pp. 426-475

[3] Y. Taur and T.H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge: Cambridge Univ. Press, 1998.

[4] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, pp. 114-, 1965.

[5] G. E Moore, “No exponential is forever: but “Forever” can be delayed! [semiconductor industry],” in *Digest of Technical Papers – IEEE International Solid-State Circuits Conference*, 2003, pp. 20-23.

[6] K. F. Schuegraf, C. C. King, and C. Hu, "Ultra-thin silicon dioxide leakage current and scaling limit," in *Digest of Technical Papers - Symposium on VLSI Technology*, 1992, pp. 18-19

[7] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, et al., “A 90nm high-volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors,” in *IEDM Tech. Dig*., Dec. 2003, pp.978–980.

[8] P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, et al., “High performance 32nm logic technology featuring 2nd generation high-*k* + metal gate transistors,” in *IEDM Tech. Dig*., Dec. 2009, pp.659–662.

[9] B. S. Haran, A. Kumara, L. Adam, J. Changa, V. Basker, S. Kanakasabapathy, D. Horak, S. Fan, J. Chen, J. Faltermeier, et al., "22 nm technology compatible fully functional 0.1 μm2 6T-SRAM cell," in *IEDM Tech. Dig*., Dec. 2008, pp.625–628.

[10] Semiconductor Industry Association (SIA), *International Technology Roadmap for Semiconductors [Electronic Resource]: ITRS, 2009 Edition*., San Jose:SIA, 2009, retrieved from http://www.itrs.net

[11] D. J. Frank, "Practical CMOS Scaling," in *Silicon Nanoelectronics*, S. Oda and D. Ferry Ed., Boca Raton: CRC Press, 2006.

[12] W. Haensch, E. J. Nowak, R. H. Dennard, P. M. Solomon, A. Bryant, O. H. Documaci, A. Kumar, X. Wang, J. B. Johnson, and M. V. Fischetti, "Silicon CMOS devices beyond scaling," *IBM J. Res. Devel*., vol. 50, pp. 339-361, 2006.

[13] P. M. Solomon, J. Jopling, D. J. Frank, C. D'Emic, O. Documaci, P. Ronsheim, and W. E. Haensch, "Universal tunneling behavior in technologically relevant P/N junction diodes," *J. Appl. Phys*., vol. 95, pp. 5800-5812, 2004.

[14] V. V. Zhirnov, R. K. Cavin, H. A. Hutchby, and G. I. Bourianoff, "Limits to binary logic switch scaling – a gedanken model," in *Proc. IEEE*, vol. 91, pp. 1934-1939, 2003.

[15] D. C. Gilmer, R. Hegde, R. Cotton, J. Smith, L. Dip, R. Garcia, V. Dhandapani, D. Triyoso, D. Roan, A. Franke, et al., "Compatibility of silicon gates with hafnium-based gate Dielectrics,'' *Microelectron. Eng*., vol. 69, pp. 138, 2003.

[16] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "Hafnium and zirconium silicates for advanced gate dielectrics," *J. Appl. Phys*., vol. 87, pp.484, 2000.

[17] K. Takahashi, K. Manabe, T. Ikarashi, N. Ikarashi, T. Hase, T. Yoshihara, H. Watanabe, T. Tatsumi, and Y. Mochizuki, "Dual work function Ni-silicide/HfSiON

gate stacks by phase-controlled full-silicidation (PC-FUSI) technique for 45nm-node LSTP and LOP Devices,'' in *IEDM Tech. Digest*, Dec. 2004, pp. 91–94.

[18] B. H. Lee, S. C. Song, R. Choi, and P. Kirsch, "Metal electrode/high-k dielectric gate-stack technology for power management," *IEEE Trans. Electron Devices*, vol. 55, pp. 8-20, 2008.

[19] P. D. Kirsch, M. A. Quevedo-Lopez, H.-J. Li, Y. Senzaki, J. J. Peterson, S. C. Song, S. A. Krishnan, N. Moumen, J. Barnett, G. Bersuker, et al., "Nucleation and growth study of atomic layer deposited HfO_2 gate dielectrics resulting in improved scaling and electron mobility," *J. Appl. Phys*., vol. 99, p. 023508, 2006.

[20] J. Robertson, "Maximizing performance for higher *k* gate dielectrics," *J. Appl. Phys*., vol. 104, p. 124111, 2008.

[21] J. M. J. Lopes, M. Roekerath, T. Heeg, E. Rije, J. Schubert, S. Mantl, V. V. Afanasev, S. Shamuilia, A. Stesmans, Y. Jia, and D. G. Schlom, "Amorphous lanthanum lutetium oxide thin films as an alternative high-k gate dielectric," *Appl. Phys. Lett*., vol. 89, p. 222902, 2006.

[22] D. G. Schlom, S. Datta, and S. Guha, "Gate oxides beyond SiO_2," *MRS Bull.*, vol. 33, pp. 1017-1025, 2008.

[23] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, "Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-*k* insulator: The role of remote phonon scattering," *J. Appl. Phys*., vol. 90, pp. 4587–4608, 2001.

[24] E. P. Gusev, V. Narayanan, and M. M. Frank, "Advanced high-k dielectric stacks with poly-Si and metal gates: Recent progress and current challenges," *IBM J. Res. Devel*., vol. 50, pp. 387-410, 2006.

[25] I. De, D. Johri, A. Srivastava, and C. M. Osburn, "Impact of gate workfunction on device performance at the 50 nm technology node," *Solid State Electron*., vol. 44, pp. 1077–2022, 2000.

[26] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-k/metal–gate stack and its MOSFET characteristics," *IEEE Electron Device Lett.*, vol. 25, pp. 408-410, 2004.

[27] B. Doris, Y. H. Kim, B. P. Linder, M. Steen, V. Narayanan, D. Boyd, J. Rubino, L. Chang, J. Sleight, A. Topol, et al., "High performance FDSOI CMOS technology with metal gate and high-k," in *Tech. Dig. VLSI Symp.*, 2005, pp. 214-215.

[28] V. Narayanan, V. K. Paruchuri, N. A. Bojarczuk, B. P. Linder, B.Doris, Y. H. Kim, S. Zafar, J. Stathis, S. Brown, J.Arnold, et al., "Band-edge high-performance high-κ/metal gate n-MOSFETs using cap layers containing group IIA and IIIB elements with gate-first processing for 45 nm and beyond," in *Tech. Dig. VLSI Symp.*, 2006, pp. 178-179

[29] L. -Å Ragnarsson, T. Schram, E. Röhr, F. Sebaai, P. Kelkar, M. Wada, T. Kauerauf, M. Aoulaiche, M. J. Cho, S. Kubicek, et al., "Single-metal dual-dielectric (SMDD) gate-first CMOS integration towards low V_T and high performance," in *Proc. VLSI-TSA Symp.*, 2009, pp.49-50

[30] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, et al., "A 45nm logic technology with high-*k*+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100% Pb-free packaging," in *IEDM Tech. Digest*, Dec. 2007, pp. 247-250.

[31] H.-C. Wen, K. Choi, C. S. Park, P. Majhi, H. R. Harris, H. Niimi, H. B. Park, G. Bersuker, P. Lysaght, D. L. Kwong, et al., "Issues associated with p-type band-edge

effective work function metal electrodes: Fermi-level pinning and flatband roll-off," in *Proc. VLSI-TSA Symp.*, 2007, pp. 40-41.

[32] J. Robertson, "Band offsets and work function control in field effect transistors," *J. Vac. Sci. Technol. B*, vol. 27, pp. 277-285, 2009.

[33] M. Chudzik, B. Doris, R. Mo, J. Sleight, E. Cartier, C. Dewan, D. Park, H. Bu, W. Natzle, W. Yan, et al., "High-performance high-k/metal gates for 45nm CMOS and beyond with gate-first processing," in *Tech. Dig. VLSI Symp.*, 2007, pp. 194-195.

[34] Y. K. Choi, K. Asano, N. Lindert, V. Subramanian, T. J. King, J. Bokor, and C. Hu, "Ultrathin-body SOI MOSFET for deep-sub-tenth micron era," *IEEE Electron Device Lett.*, vol. 21, pp. 254-255, 2000.

[35] R. Chau, J. Kavalieros, B. Doyle, A. Murthy, N. Paulsen, D. Lionberger, D. Barlage, R. Arghavani, B. Roberds and M. Doczy, "A 50nm depleted-substrate CMOS transistor (DST)," in *IEDM Tech. Digest*, Dec. 2001, pp. 621-624.

[36] J. P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes, and C. Claeys, "Silicon-on-insulator "Gate-all-around device"," in *IEDM Tech. Digest*, Dec. 1990, pp. 595-598.

[37] J. T. Park, J. P. Colinge, and C. H. Diaz, "Pi-gate SOI MOSFET," *IEEE Electron Device Lett*., vol. 22, pp. 405-406, 2001.

[38] J. G. Fossum , L. Q. Wang , J. W. Yang , S. H. Kim, and V. P. Trivedi, "Pragmatic design of nanoscale multi-gate CMOS," in *IEDM Tech. Digest*, Dec. 2004, pp. 613-616.

[39] F. L. Yang, H. Y. Chen, F. C. Chen, C. C. Huang, C. Y. Chang, H. K. Chiu, C. C. Lee, C. C. Chen, H. T. Huang, C. J. Chen, et al., "25 nm CMOS omega FETs," in *IEDM Tech. Digest*, Dec. 2002, pp. 255-258.

[40] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "FinFET: A self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*, vol. 47, pp. 2320–2325, 2000.

[41] F. L. Yang, D. H. Lee, H. Y. Chen, C. Y. Chang, S. D. Liu, C. C. Huang, T. X. Chung, H. W. Chen, C. C. Huang, Y. H. Liu, et al., "5nm-gate nanowire FinFET," in *Tech. Dig. VLSI Symp.*, 2004, pp. 196-197.

[42] J. Welser, J. L. Hoyt, and J. F. Gibbons, "NMOS and PMOS transistors fabricated in strained-silicon/relaxed silicon-germanium structures," in *IEDM Tech. Digest*, Dec. 1992, pp. 1000-1002.

[43] K. Uchida, T. Krishnamohan, K. C. Saraswat, and Y. Nishi, "Physical mechanisms of electron mobility enhancement in uniaxial stressed MOSFETs and impact of uniaxial stress engineering in ballistic regime," in *IEDM Tech. Digest*, Dec. 2005, pp. 135-138.

[44] J. L. Hoyt , H. M. Nayfeh , S. Eguchi , I. Aberg , G. Xia , T. Drake , E. A. Fitzgerald and D. A. Antoniadis, "Strained silicon MOSFET technology," in *IEDM Tech. Dig.*, Dec. 2002, pp. 23-26.

[45] T. Numata , T. Irisawa , T. Tezuka , J. Koga , N. Hirashita , K. Usuda , E. Toyoda , Y. Miyamura , A. Tanabe , N. Sugiyama and S. Takagi "Performance enhancement of partially and fully depleted strained-SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, pp. 1030-1038, 2006.

[46] S. Takagi, T. Irisawa, T. Tezuka, T. Numata, S. Nakaharai, N. Hirashita, Y. Moriyama, K. Usuda, E. Toyoda, S. Dissanayake, et al., "Carrier-transport-enhanced channel CMOS for improved power consumption and performance," *IEEE Trans. Electron Devices*, vol. 55, pp. 21-39, 2008.

[47] P. R. Chidambaram, C. Bowen, S. Chakravarthi, C. Machala, and R. Wise, "Fundamentals of silicon material properties for successful exploitation of strain engineering in modern CMOS manufacturing," *IEEE Trans. Electron Devices*, vol. 53, pp. 944-964, 2006.

[48] C. Gallon, G. Reimbold, G. Ghibaudo, R. A. Bianchi, R. Gwoziecki,S. Orain, E. Robilliart, C. Raynaud, and H. Dansas, "Electrical analysis of mechanical stress induced by STI in short MOSFETs using externally applied stress," *IEEE Trans. Electron Devices*, vol. 51, pp. 1254–1261, 2004.

[49] A. Steegen, I. De Wolf, and K. Maex, "Characterization of the local mechanical stress induced during the Ti and Co/Ti salicidation in sub-0.25 μm technologies," *J. Appl. Phys.*, vol. 86, pp. 4290–4297, 1999.

[50] H. S. Yang, R. Malik, S. Narasimha, Y. Li, R. Divakaruni, P. Agnello, S. Allen, A. Antreasyan, J. C. Arnold, K. Bandy, et al., "Dual stress liner for high performance sub-45 nm gate length SOI CMOS manufacturing," in *IEDM Tech. Dig.*, Dec. 2004, pp. 1075–1077.

[51] A. Wei, M. Wiatr, A. Mowry, A. Gehring, R. Boschke, C. Scott, J. Hoentschel, S. Duenkel, M. Gerhardt, T. Feudel, et al., "Multiple stress memorization in advanced SOI CMOS technologies," in *Tech. Dig. VLSI Symp*., 2007, pp. 216–217.

[52] C. Auth, M. Buehler, A. Cappellani, C. H. Choi, G. Ding, W. Han, S. Joshi, B. McIntyre, M. Prince, P. Ranade, et al., "45nm high-k+metal gate strain-enhanced transistors," *Intel Technol. J*., vol. 12, pp. 77-85, 2008.

[53] G. Eneman, P. Verheyen, A. De Keersgieter, M. Jurczak, and K. De Meyer, "Scalability of stress induced by contact-etch-stop layers: A simulation study," *IEEE Trans. Electron Devices*, vol. 54, pp. 1446–1453, 2007.

[54] G. Eneman, P. Verheyen, R. Rooyackers, F. Nouri, L. Washington, R. Schreutelkamp, V. Moroz, L. Smith, A. De Keersgieter, M. Jurczak, and K. DeMeyer, "Scalability of the $Si_{1-x}Ge_x$ source/drain technology for the 45-nm technology node and beyond," *IEEE Trans. Electron Devices*, vol. 54, pp. 1647–1656, Jul. 2007.

[55] M. Lundstrom, "Elementary scattering theory of the Si MOSFET," *IEEE Electron Device Lett.*, vol. 18, pp. 361–363, 1997.

[56] M. Levinshtein, S. Runyantsev, and M. Shur Ed., *Handbook series on semiconductor parameters*, vol. 1, 2, Singapore: World Scientific Publishing Co., 1996.

[57] M. L. Lee and E. A. Fitzgerald, "Optimized strained Si/strained Ge dual-channel heterostructures for high mobility P- and N-MOSFETs," in *IEDM Tech. Dig*., Dec. 2003, pp. 429–432.

[58] O. Weber, Y. Bogumilowicz, T. Ernst, J. -M. Hartmann, F. Ducroquet, F. Andrieu, C. Dupré, L. Clavelier, C. Le Royer, N. Cherkashin, et al., "Strained Si and Ge MOSFETs with high-K/metal gate stack for high mobility dual channel CMOS," in *IEDM Tech. Dig*., Dec. 2005, pp. 137–140.

[59] N. Wu, Q. Zhang, N. Balasubramanian, D. S. H. Chan, and C. Zhu, "Characteristics of self-aligned gate-first Ge p- and n-channel MOSFETs using CVD HfO_2 gate dielectric and Si surface passivation," *IEEE Trans. Electron Devices*, vol. 54, pp. 733-741, 2007.

[60] D. Kuzum1, T. Krishnamohan, A. Nainani1, Y. Sun, P. A. Pianetta, H. S-. P. Wong, and K. C. Saraswat, "Experimental demonstration of high mobility Ge NMOS," in *IEDM Tech. Dig*., Dec. 2009, pp. 453-456.

[61] T. Skotnicki, C. Fenouillet-Beranger, C. Gallon, F. Boeuf, S. Monfray, F. Payet, A. Pouydebasque, M. Szczap, A. Farcy, F. Arnaud, et al., "Innovative materials,

devices, and CMOS technologies for low-power mobile multimedia," *IEEE Trans. Electron Devices*, vol. 55, pp. 96-130, 2008.

[62] S. E. Laux, "A simulation study of the switching times of 22- and 17-nm gate-length SOI nFETs on high mobility substrates and Si," *IEEE Trans. Electron Devices*, vol. 54, pp. 2304-2320, 2007

[63] R. M. Wallace, P. C. McIntyre, J. Kim, and Y. Nishi, "Atomic layer deposition of dielectrics on Ge and III–V materials for ultrahigh performance transistors," *MRS Bull*., vol. 34, pp. 493-503, 2009.

[64] M. Houssa, E. Chagarov, and A. Kummel, "Surface defects and passivation of Ge and III–V Interfaces," *MRS Bull*., vol. 34, pp. 504-513, 2009.

[65] D. Sadana, "New channel materials for future MOSFET technology," in *Proc. Sematech Meeting*, Dec. 2005.

[66] M. Yokoyama, T. Yasuda, H. Takagi, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka, and S. Takagi, "High mobility metal S/D III-V-On-Insulator MOSFETs on a Si substrate using direct wafer bonding," in *Tech. Dig. VLSI Symp*., 2009, pp. 242-243.

[67] T. Dürkop, S.A. Getty, E. Cobas, and M.S. Fuhrer. "Extraordinary mobility in semiconducting carbon nanotubes." *Nano Lett*., vol. 4, pp. 35-39, 2004.

[68] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S.K. Banerjee. "Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric." *Appl. Phys. Lett*., vol.94, p. 062107, 2009.

[69] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, pp. 666-669, 2004.

[70] E. H. Hwang, S. Adam, and S. Das Sarma, "Carrier transport in two-dimensional graphene layers," *Phys. Rev. Lett*., vol. 98, p. 186806, 2007.

[71] T. Mori, Y. Azuma, H. Tsuchiya, and T. Miyoshi, "Comparative study on drive current of III–V semiconductor, Ge and Si channel n-MOSFETs based on quantum-corrected Monte Carlo simulation", *IEEE Trans. Nanotechnol.*, vol. 7, pp. 237-241, 2008.

[72] M. T. Currie, S. B. Samavedam, T. A. Langdo, C. W. Leitz, and E. A. Fitzgerald, "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing," *Appl. Phys. Lett*., vol. 72, pp. 1718-1720, 1998.

[73] S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S. Takagi, "Characterization of 7-nm-thick strained Ge-on-insulator layer fabricated by Ge-condensation technique," *Appl. Phys. Lett*., vol. 83, pp. 3516-3518, 2003.

[74] C. W. Wilmsen Ed., *Physics and Chemistry of III-V Compound Semiconductor Interfaces*, New York: Plenum, 1985.

[75] I. G. Thayne, R. J. W. Hill, D. A. J. Moran, K. Kalna, A. Asenov, and M. Passlack, "Comments on "High performance inversion-type enhancement-mode InGaAs MOSFET with maximum drain current exceeding 1 A/mm"," *IEEE Electron Device Lett*., vol. 29, pp. 1085-1086, 2008.

CHAPTER 2

INTEGRATION OF GaAs EPITAXIAL LAYER ONTO Si-BASED SUBSTRATE

2.1 INTRODUCTION

The substrate engineering integrating GaAs channel with Si platform is an urgent research subject which enables high mobility III-V channel to boost CMOS performance beyond 10 nm node, as indicated in ITRS projections [1]. The success of emerging research materials depends on robust synthetic techniques that yield useful structural quality with the required control of defect, morphology, and the compatibility with manufacturable technology.

Reminding the requirements, in this chapter, we proposed a way of growing GaAs on Si which combines a conventional heteroepitaxy technique of virtual Ge substrate and a large-scale Si wafer-based Ge condensation method, utilizing the strengths while avoiding the drawbacks of those methods. Finally it was successfully demonstrated that a device quality GaAs can be grown on Si wafer with a GaAs-on-insulator (GaAs-OI) structure for the future GaAs/CMOS integration for the first time, in a novel and cost-effective way.

2.1.1 BACKGROUND AND MOTIVATION

Since the 1980s there has been a high level of activity in the study of heteroepitaxial GaAs on Si (GaAs/Si), which is the potential material for monolithic integration of optoelectronic and high speed devices with advanced Si-based electronic circuits. Recently a great deal of attention has been paid to III-V channel as a candidate for high performance of NMOSFETs beyond strained-Si devices as reviewed in the previous chapter. Monolithic integrations of III-V semiconductors with Si devices would enable to extend Moor's law beyond the 10 nm node overcoming Si's fundamental limitation as well as to provide various functionalities exploiting the mature III-V optoelectronic devices for future nanoelectronics applications. The monolithic integration should be based on parallel processing of CMOS and III-V devices thus producing economies of scale and reduced costs. However, the integration of III-V with Si CMOS has numerous technical challenges that have prevented it from being implemented to date on a large scale, chiefly due to large lattice mismatches between III-Vs and Si.

As mentioned above, the study of GaAs/Si for monolithic integrations has been carried out over more than two decades. Meanwhile, Si-based process technologies have been developed with a remarkable speed. Therefore, the study of GaAs heteroepitaxy on Si-based substrate should be renewed with the recent Si-based process technologies and the requirements for future applications. Because non-planar ultimate CMOS structures such as UTB structures and multiple-gate structures have being developed and predicted as future CMOS structures to mitigate the constraints of SCE and the power consumption issue, the eventual III-V/Si integration figure should be III-V-on-insulator (III-V-OI) in a large scale Si wafer. These approaches reflecting state-of-the-art CMOS technologies can also provide better knowledge for the research

society in choosing III-V semiconductor material as an alternative solution for carrier-transport enhancement of future scaled Si CMOS devices. Since GaAs has the smallest lattice constant among binary III-V semiconductors with a high electron mobility, this work of monolithic integration was carried out first for GaAs/Si system based on the accumulated knowledge on the system.

2.1.2 APPROACHES FOR HETEROEPITAXY OF HIGH MOBILITY CHANNEL ON Si

Techniques of monolithic integration of GaAs with Si substrate will be reviewed in this section.

Because the GaAs/Si system has a large lattice mismatch (~4.1 %) and a large difference in thermal expansion coefficient (~161 %) [2], a defective GaAs epitaxial layer grown on Si is often the inherent problem. Lattice mismatch refers to the difference in lattice constant between the epitaxial film and the substrate. For planar film growth the lattice mismatch is accommodated by a combination of elastic and plastic strains in the film. This lattice mismatch, f is defined as follows:

$$f = \frac{a_{sub} - a_{film}}{a_{sub}} = \alpha + \delta \tag{2.1}$$

where a_{sub} and a_{film} are the lattice constants of the substrate and epitaxial layer respectively, α is the elastic strain in the film, and δ is the plastic strain. When an epitaxial layer grows on a substrate, as the thickness of the film increases, the strain energy of the film increases, and above a certain "critical thickness, h_c," the elastic strain in the strained epilayer is relieved by forming misfit dislocations at the interface in the case of a general rigid solid substrate. Thus a film grown above h_c will contain a misfit dislocation array at the interface resulting in threading dislocation segments

which extend from the interface to the surface of the film. For semiconductor device applications, the threading dislocations affect device performance seriously which includes being a junction leakage point and a trap site. Hence, in working with relaxed lattice-mismatched heteroepitaxial films, growing the lattice-mismatched heteroepitaxial layer with a minimum of threading dislocations is a key concern.

Since the 1980s, there have been a number of innovative approaches to overcome the problem, such techniques as "compliant universal substrate" (CS) [3], SOI CS [4], epitaxial lift-off [5], flip-chip bonding [6], and nanoheteroepitaxy (NHE) [7,8]. However, the bonded or grown interface obtained by these techniques is known to deleteriously affect the electrical property for large-area scaling.

Another approach using an intermediate buffer was proposed using Ge/SiGe system, so called "Ge virtual substrate" [9-11]. GaAs can be directly grown on Ge, as the two materials have a small lattice mismatch (~0.17 %) and have almost the same thermal expansion coefficient. Table 2.1 summarizes material properties of Si, Ge, and GaAs. Therefore, Ge can serve as an intermediate layer for integration of GaAs on Si via a compositionally graded $Si_{1-x}Ge_x$ buffer layer as illustrated in Fig.2.1. The $Si_{1-x}Ge_x$ alloy system is fully miscible, thus allowing $Si_{1-x}Ge_x$ alloys of any Ge fraction to be deposited without phase separation issues. The compositionally graded $Si_{1-x}Ge_x$ with optimum gradient of Ge fraction up to $x = 1$ can thus be used for the growth of GaAs on Si with much reduced threading dislocations. Compositionally graded buffers are very useful as a virtual substrate for heteroepitaxial structures. However, although the lattice mismatch and thermal expansion coefficient difference between GaAs and Ge is not an issue in this case, challenges remain in growing a relaxed SiGe buffer directly on Si. Even though it can be achieved by gradually increasing the Ge concentration (~10 % Ge μm^{-1}) in SiGe and with chemical mechanical polishing (CMP) [10], the

thick (several tens μm) buffer layer still contains threading dislocations and is not suitable to fabricate CMOS devices on it (Fig. 2.2). In addition, the thick buffer layer can cause a serious interconnection issue between III-V and Si devices in a monolithic IC.

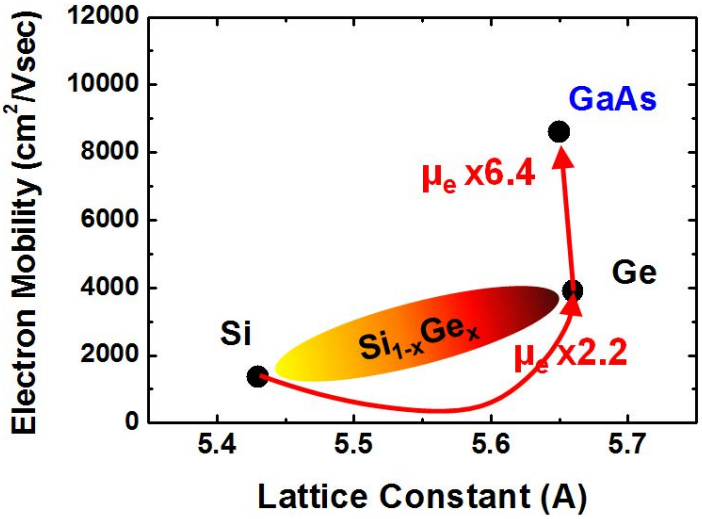


Fig. 2.1 Illustration of GaAs heteroepitaxial growth via compositionally graded $Si_{1-x}Ge_x$ buffer layer to overcome the lattice mismatch between GaAs and Si. The guide line is drawn schematically referring to experimental data of electron Hall mobility for unstrained $Si_{1-x}Ge_x$ at 300K [12].

Table 2.1 Material properties of Si, Ge, and GaAs at room temperature [13].

	Si	**Ge**	**GaAs**
Crystal structure	Diamond, 8 atoms/unit cell	Diamond, 8 atoms/unit cell	Zinc-blende, 8 atoms/unit cell
Lattice constant (Å)	5.43	5.66	5.65
Electron mobility, μ_e (cm^2/Vs)	1350	3900	8600
Hole mobility, μ_h (cm^2/Vs)	480	1900	250
Melting point (^oC)	1415	937	1238
Linear coefficient of thermal expansion $\Delta L/L\Delta T$ ($^oC^{-1}$)	2.5×10^{-6}	5.8×10^{-6}	5.9×10^{-6}

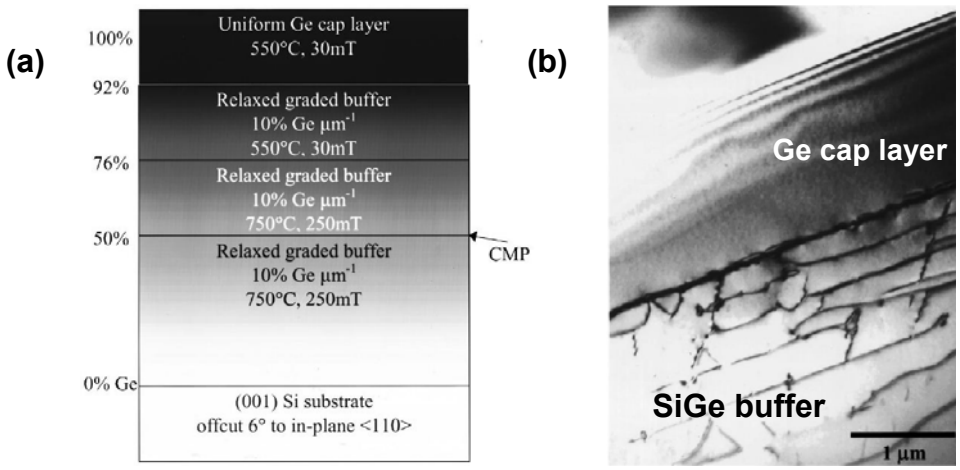


Fig. 2.2 (a) Schematic of the structure for optimized Ge heteroepitaxy on Si via graded SiGe buffer layers. Ge concentrations are indicated on the left. (b) Cross-sectional TEM image of the upper graded region [10].

2.1.3 OBJECTIVE

By reviewing the published data above, much progress has been made on GaAs heteroepitaxy on Si using Ge virtual substrate, especially considering compatibility with manufacturable technologies. However, any GaAs heteroepitaxial growth techniques in the point of view of an extension of CMOS scaling has not been realized yet. In order to integrate high electron mobility GaAs MOSFETs on the Si platform for future CMOS scaling, the eventual structure should be GaAs-OI. In this work, therefore, GaAs heteroepitaxial layer formation technique using SOI wafer is explored, developed, and demonstrated utilizing a compositionally graded SiGe buffer system and MBE process technique.

2.2 GaAs MBE GROWTH ON Si(100) VIA STRAINED SiGe

2.2.1 INTRODUCTION

GaAs heteroepitaxial growth on Si substrate with an intermediate SiGe buffer epilayer was investigated with emphasis on the initial growth conditions using UHV

CVD for SiGe growth and MBE for GaAs. Contrary to previous studies on GaAs growth on a relaxed SiGe buffer, this work was carried out by using a strained $Si_{1-x}Ge_x$ epitaxial layer, which has a similar lattice parameter with Si, as a buffer layer between GaAs and Si. The strain relaxation during GaAs MBE growth is investigated using microscopic observation.

2.2.2 EXPERIMENT

$Si_{1-x}Ge_x$ epitaxial layers were grown on 200 mm (100) p-type Si wafers in a UHV CVD-type epi-chamber using Si_2H_6 and GeH_4 gases after cleaning the wafers in a dilute HF (DHF, H_2O:HF=100:1 in volume) solution for 2 min, followed by *in situ* SF_6 dry cleaning in the epi chamber for 2 min to remove native oxides on the Si surface. Then $Si_{1-x}Ge_x$ epitaxial layers with Ge concentrations of 15 and 45 % and a pure Ge epitaxial layer were grown without breaking the vacuum. The $Si_{1-x}Ge_x$ layers and pure Ge epitaxial layer were grown at 520 ^oC and the thicknesses measured by spectroscopic ellipsometer were 30, 10, and 1.2 nm, respectively. The Ge concentration in $Si_{1-x}Ge_x$ epitaxial layer was confirmed by X-ray photoelectron spectroscopy (XPS). The atomic force microscopy (AFM) measurement results on these $Si_{1-x}Ge_x$ epi-layers showed no crosshatch pattern on the epi-layers, which confirmed the epi-layers were not relaxed but strained on the Si substrate. The root-mean-square (rms) values of the roughness of the epi-layers were less than 7 Å. GaAs epitaxial layers were then grown by MBE. The native oxide on the surface was etched away in a 1 % DHF solution for 2 min. The samples were degassed at 350 ^oC for 25 min in the MBE chamber at a pressure of ~10^{-6} Torr. Oxide desorption was carried out at 650 ^oC, by *in situ* thermal annealing for 20 min in the MBE chamber at a pressure of 2.5×10^{-8} Torr. The sample surface was monitored till a (2 × 2) streaky reflection high-

energy electron diffraction (RHEED) pattern was obtained. Next, the substrate temperature was reduced for the GaAs layer growth. GaAs epitaxial layers on SiGe/Si substrate were grown at 550 ^{o}C for 90 s at a growth rate of 0.4 μm/h. Transmission electron microscope (TEM) analysis was employed to confirm the atomic structure of the grown film.

2.2.3 RESULTS AND DISCUSSION

The AFM images of the GaAs layers grown on three different x values of $Si_{1-x}Ge_x$ on Si (x = 0.15, 0.45, 1) are shown in Fig. 2.3. The surface roughness of the GaAs epitaxial layer decreases with the increase of Ge concentration in $Si_{1-x}Ge_x$ layer. This indicates that the strain of the SiGe buffer layer is considerably relaxed at the MBE growth temperature, resulting in the reduction of the lattice mismatch with GaAs.

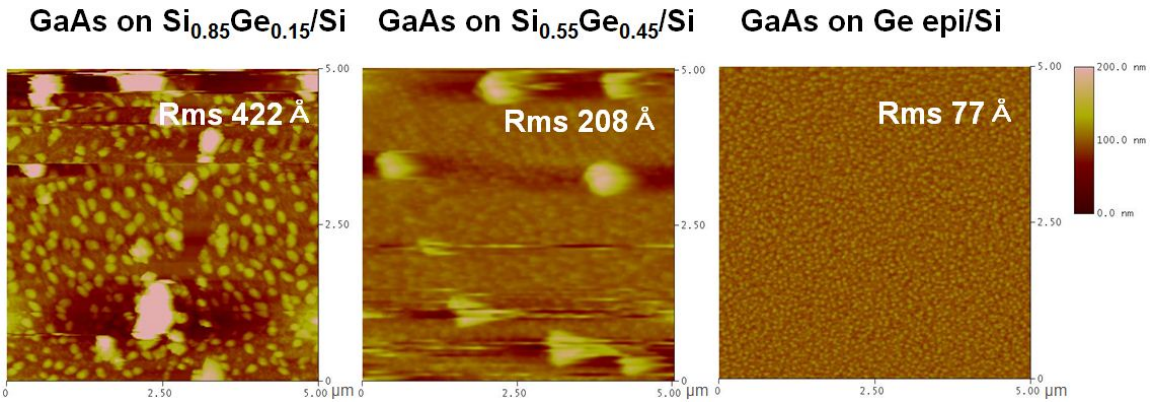


Fig. 2.3 AFM images of GaAs grown on strained $Si_{1-x}Ge_x$/Si substrate for x=0.15, 0.45, and 1.

Figure 2.4 shows a cross-sectional TEM image of GaAs on Si substrate where a 1.2 nm thick pure Ge epitaxial layer was used as a buffer layer. An 80 - 90 nm thick discrete Si layer with a significant amount of dislocations was generated in the silicon substrate as a result of strain caused by the deposition of GaAs/Ge on Si and the

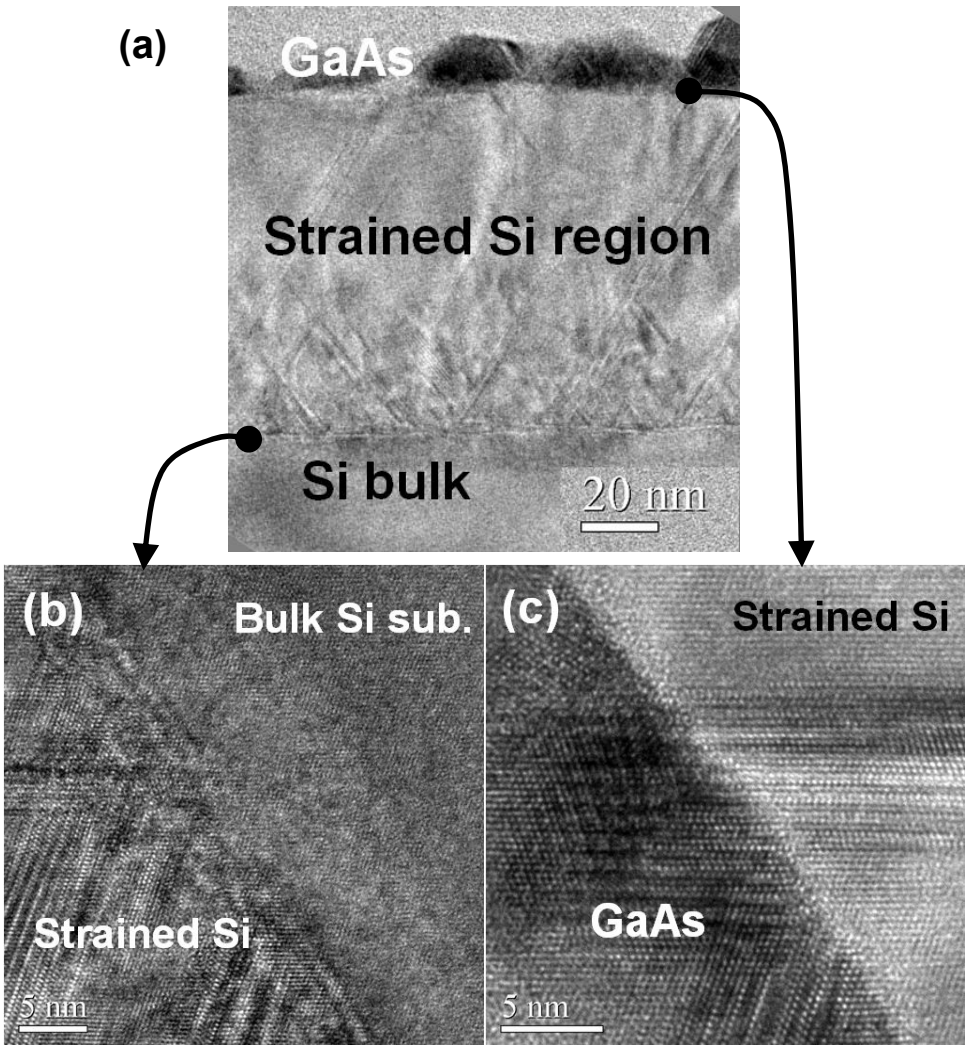


Fig. 2.4 TEM images of GaAs grown on strained Ge epi/Si substrate. GaAs MBE growth on the Si substrate results in island structures and a discrete Si layer with dislocation defects. (a) TEM image in a low magnification. (b) TEM image of the lower interface. (c) A high magnification TEM image of the interface between GaAs and Si.

different thermal expansion coefficients during the cooling step after deposition. At the interface, however, the lattice of GaAs was aligned with the Si lattice through the Ge interface layer as seen in Fig. 2.4b. The Ge interfacial layer is not clearly observable, but is detected by energy dispersive X-ray spectroscopy (EDS). It is a new finding that the substrate is plastically deformed with threading dislocations but not being confined the relaxation in the GaAs or Ge epitaxial layer by misfit dislocations. Typically

threading dislocations terminate on available free surfaces. It has been reported that, in GaAs/Si heteroepitaxy, the dislocation is generated in cooling stage of GaAs growth due to the thermal expansion mismatch between GaAs and Si and this thermal stress induces dislocation/dislocation propagation to the GaAs surface [14]. This interesting observation of the misfit strain remaining in a substrate can be explained only when a certain amount of plastic deformation is allowed after growth, in contrary to the previous report. It may be mainly due to the Ge layer which has lattice and thermal expansion parameters matched with GaAs.

2.2.4 CONCLUSION

From the interesting results presented above, we can practically conclude two aspects: (1) Ge concentration in the SiGe buffer layer is an important factor in growing GaAs heteroepitaxial layer using MBE. A high Ge concentration in the SiGe buffer layer is effective to form homogeneous nucleation and to relax the strain built up during the initial growth of GaAs leading to good alignment of GaAs on Si even when the buffer layer is a few atomic layers thick. (2) Dislocation generation in the substrate is unavoidable as long as a rigid Si substrate is used, although the lattice at the interface is well aligned with reduced dislocation defects.

2.3 CONCEPT OF GaAs HETEROEPITAXY ON A COMPOSITIONALLY GRADED SGOI

We propose a process scheme for the integration of GaAs to Si as illustrated in Fig. 2.5. Firstly, (a) SiGe layer with a low Ge concentration is grown on a thin SOI layer. The Ge concentration in the SiGe layer on SOI should be low enough for formation of a dislocation-free SiGe layer. Then, (b) using Ge condensation techniques

[15-17], SOI layer turns into Ge concentration graded SGOI during oxidation. In the oxidation process, Ge atoms are rejected from the oxidizing SiO_2 layers and diffuse into the remaining SGOI layer. After forming the SGOI layer with a high Ge concentration on top of the layer (c), the grown SiO_2 layer on the SiGe is removed by HF. Finally, GaAs epi-layer is grown on graded SiGe layer as shown in Fig. 2.5d. If the SGOI layer is thin enough, strains in the graded SGOI layer is partially relaxed due to the viscous flow of buried oxide (BOX) [18] during the high temperature condensation process. As a result, the lattice mismatch between GaAs and SGOI can be small. A high Ge fraction close to 1 at the surface of the SGOI is required to achieve GaAs on the SGOI without forming dislocations. One of the critical points in this process is that the initial SOI thickness and the final graded SiGe layer must be thin enough so that the lattice mismatch-induced and thermal stress-induced strains in the SGOI layer can be effectively relaxed by viscous flow of the BOX layer at a high temperature. Since the dislocations extends to bulk silicon approximately 80 nm deep from the interface at GaAs where a thin Ge buffer layer is used for the GaAs heteroepitaxial growth on silicon as shown in Fig. 2.4, the graded SGOI layer must be thinner than 80 nm to ensure stress release can be affected by the viscous flow of BOX.

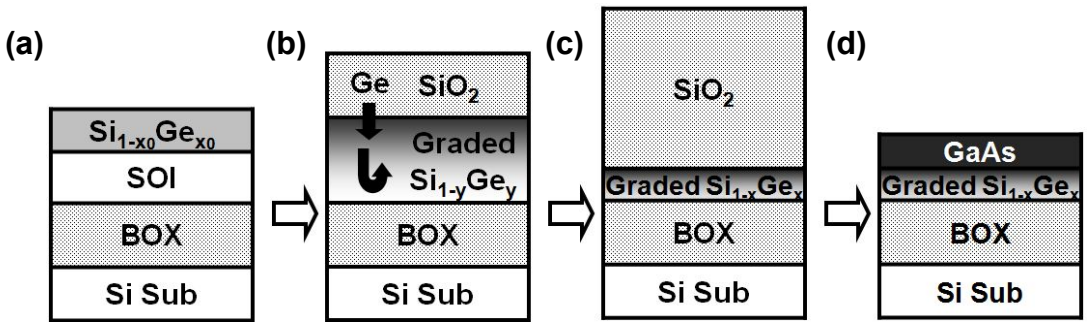


Fig. 2.5 Process flow of the fabrication of GaAs heteroepitaxial layer on a graded SGOI prepared by a Ge condensation method. (a) SiGe epilayer growth on SOI with low Ge concentration, x_0. (b) Ge condensation during oxidation. (c) Oxidation stops when graded SGOI is accomplished with high Ge concentration on the top of the SGOI layer. (d) After removing the top SiO_2 layer, MBE GaAs epitaxial layer is grown on the graded SGOI.

2.4 FABRICATION OF GRADED SGOI SUBSTRATE FOR GaAs HETEROEPITAXY

2.4.1 INTRODUCTION

To grow device quality GaAs heteroepitaxial layer on SGOI, Ge concentration on the top of the SiGe surface should be high enough to provide a similar thermal expansion coefficient with GaAs. In addition, the crystalline quality should be good enough not to evolve threading dislocations to the GaAs layer to be deposited. In this section, the first three processes of the proposed GaAs heteroepitaxy technique (Fig. 2.5a-c), which is named as a modified two-step Ge condensation, will be described.

2.4.2 MODIFIED TWO-STEP Ge CONDENSATION METHOD

It was reported that dry oxidation of SiGe film at high temperature results in growth of SiO_2 layer with Ge piling up behind it [19, 20]. This phenomenon was developed to a SGOI fabrication technology so called Ge condensation, which is based on oxidation of SiGe on SOI [15]. During the oxidation of SiGe layer on SOI substrate at a high temperature, Ge atoms are rejected from the oxide and condensed in the merged SGOI layers formed by interdiffusion between Si and Ge atoms. The total amount of Ge in the SiGe layer is preserved through the oxidation process so that cyclic thermal oxidations of a SGOI at temperatures lower than the melting point of the SiGe layer, which depends on the Ge fraction, can condense the SGOI up to GOI [16]. Because of the excellent film quality with a low cost of the process utilizing traditional oxidation techniques, Ge condensation method has been developed for a FD SOI-type high mobility SGOI/GOI channel into future CMOS technologies.

However, the Ge condensation method usually has two problems when a large area of the SiGe layer is oxidized. Those are crosshatch patterned surface and agglomeration as shown in Fig. 2.6.

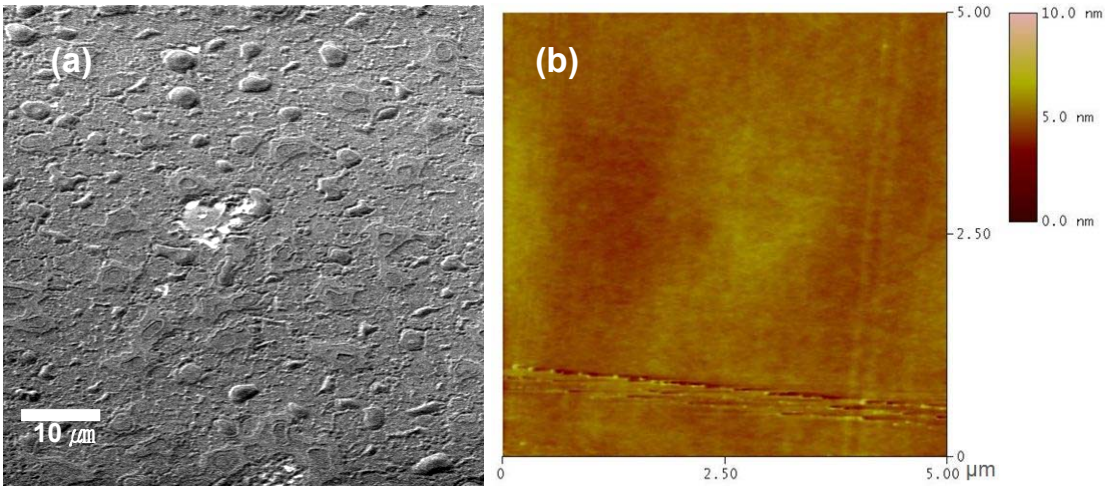


Fig. 2.6 Major issues in conventional Ge condensation: Scanning electron microscope (SEM) image of agglomeration (a) and AFM image of crosshatch patterned surface (b) after the conventional Ge condensation.

The crosshatch pattern indicates the evolution of misfit dislocation between the layers with different lattice constants when the SiGe becomes thicker than h_c at the corresponding Ge fraction. The agglomeration is due to non-uniform Ge concentration in SiGe during the condensation. The melting temperature of SiGe alloy decreases from 1414 to 938 ^{o}C as the fraction of Ge concentration increases from 0 to 1. The continuous Ge piling up at the interface of SiO_2/SiGe during high temperature oxidation and the migration of Ge can cause non-uniform Ge concentration at the interface. Therefore, if the condensation oxidation is done at a fixed temperature, locally high Ge concentration area starts to melt during the oxidation, resulting in agglomeration. Such problem becomes more serious when the SiGe oxidizing area is large. Practically it is difficult to avoid agglomeration when the target Ge concentration of the condensation is over 50 %.

To overcome these limitations, a two-step oxidation was applied to SiGe layer on a SOI substrate. First, the SiGe is oxidized at a high temperature until Ge concentration reaches to a certain level at which the melting temperature of the SiGe layer is around 100 ^{o}C higher than the oxidation temperature. Then, the oxidation temperature is gradually reduced to avoid the agglomeration but with the Ge piling up continuing to occur. Figure 2.7 shows the concept schematically with a phase diagram.

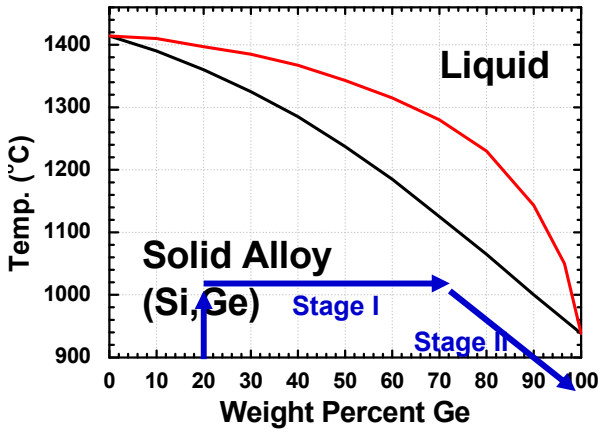


Fig. 2.7 Schematic illustration of a temperature profile for the two-step Ge condensation with a phase diagram of Si-Ge alloy.

Based on this consideration and through a number of trials, the oxidation recipe was determined in two steps as: (1) 1000 ^{o}C for 10 min, and (2) oxidation during ramping down to 700 ^{o}C with a ramp rate of 1 ^{o}C/min for our work. We found that the initial SiGe/SOI stack structure is another critical factor to avoid the problems. The lower Ge concentration for SiGe epi-layer and the thinner films for both are favored. Eventually, the initial film structure was determined as 34 nm thick SiGe with 18 % Ge on 33 nm thick SOI in this work. The Ge condensation area was a quarter of 200 mm wafer.

2.4.3 RESULTS AND DISCUSSION

Using the two-step Ge condensation method, a high Ge concentration of 71 % at the SiGe surface was achieved without any dislocations or agglomerations over the entire sample surface with no isolation field oxide pattern. Figure 2.8 shows AFM and TEM images and Ge depth profile measured by secondary ion mass spectroscopy (SIMS) of the compositionally graded SGOI after the modified two-step Ge condensation.

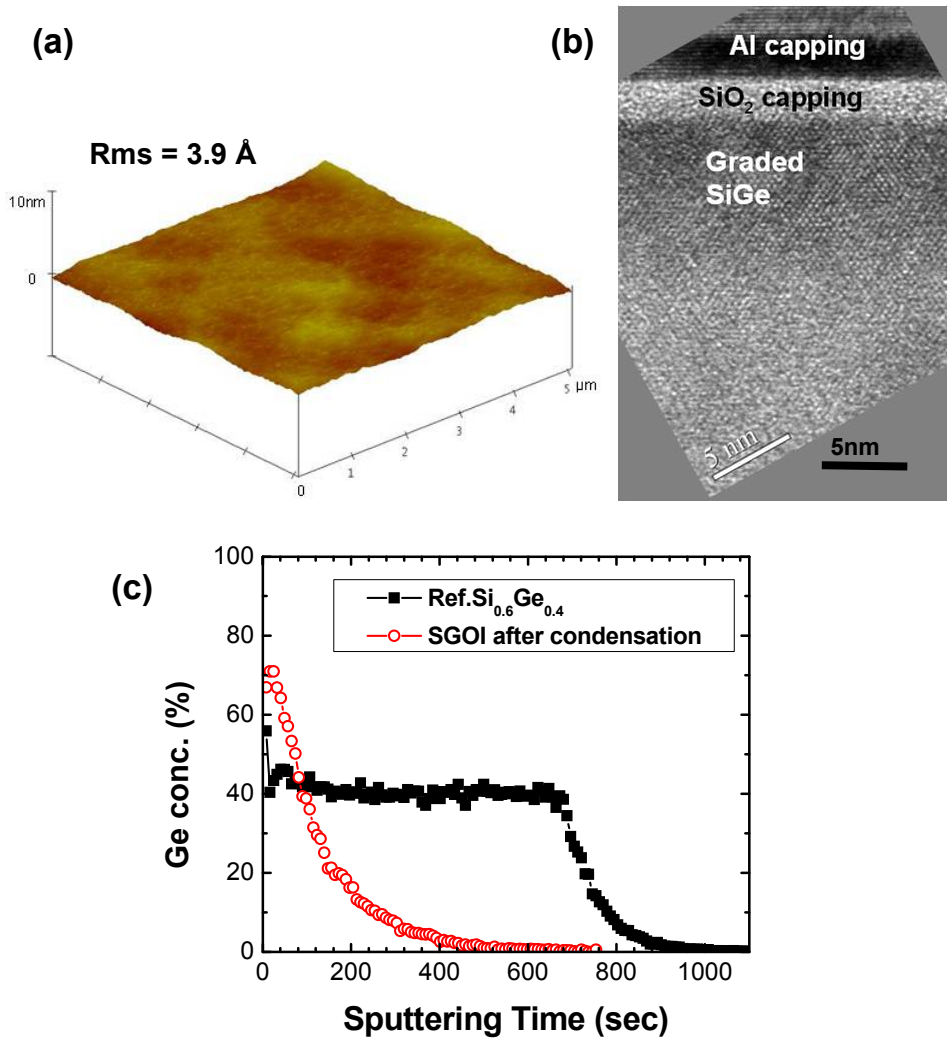


Fig. 2.8 Modified two-step Ge condensation result; (a) AFM image of graded SGOI after removal of SiO_2 grown during the oxidation. (b) TEM result of the graded SGOI of 42nm thickness. (c) SIMS depth profile of the graded SGOI. Ge concentration at the surface is around 71%.

The rms value of surface roughness of the SiGe after condensation was 3.9 Å over the area of 5 × 5 μm^2 (Fig.2.8a). According to the XTEM result as shown in Fig. 2.8b, the thickness was 42 nm and the lattice parameter of this SGOI layer was 5.57 ± 0.04 Å. The lattice parameter was estimated with reference to the distance between [111] planes of bulk Si substrate. The measured lattice parameter of SGOI, 5.57 ± 0.04 Å corresponds to equivalent Ge concentration of 63 ± 17 % in accordance with Vegard's linear rule [21]. This implies that pseudomorphic SGOI is formed without strain relaxation by dislocations within the SGOI layer so that the upper 5 - 10 nm is compressive and the rest is tensile strained. The Ge concentration gradient in Fig. 2.8c is much higher compared with other reports of Ge condensation using a single step oxidation [22].

Such a high Ge concentration gradient and the strained structure of SGOI layer in our modified Ge condensation can be explained, with the help of illustrations in Fig. 2.9. During the oxidation at a high temperature (Stage I), Ge diffusion and stress-relaxation in SGOI is dominant because of high Ge diffusivity and BOX viscosity. On the other hand, Ge accumulation on the $SiO_2/Si_{1-x}Ge_x$ interface is dominant at low temperature oxidation (Stage II) due to the relatively higher oxygen diffusivity compared to Ge diffusivity. This can be rationalized by the difference of the activation energy of diffusion, which is 1.17eV [23] for the oxygen diffusion in SiO_2 and 5.8eV [24] for Ge diffusion in Si crystal [22]. In addition, as the temperature decreases, the relaxation of the strain through the viscous flow of SiO_2 on the SGOI/BOX interface becomes smaller in the stage II, which results in the build-up of strain in SiGe layer.

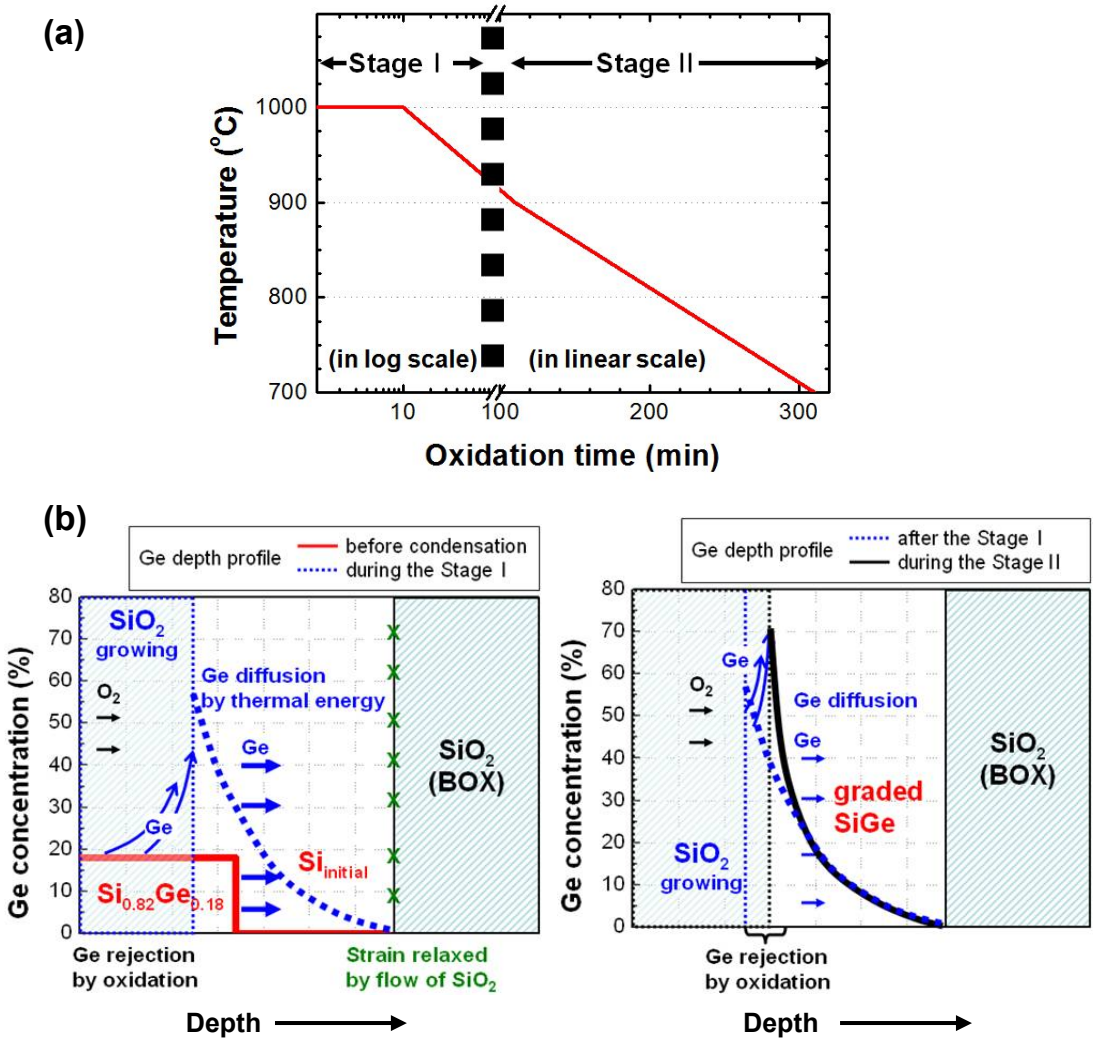


Fig. 2.9 (a) Schematic illustration of the modified two-step Ge condensation oxidation recipe. (b) Schematic drawing of the film structure with Ge profile at each stage.

2.4.4 CONCLUSION

To make a virtual substrate for GaAs heteroepitaxy on Si-based substrate using compositionally graded SiGe buffers with SOI structure, the Ge condensation technique was examined and developed. It was found that a modified two-step Ge condensation technique is effective to build a graded SGOI structure with high Ge fraction on the top surface and without defects such as agglomeration and misfit

dislocations in a large-scale wafer. Using the two-step Ge condensation method, a high Ge concentration of 71 % at the SiGe surface was achieved in 42 nm thick SGOI with a pseudomorphic film structure.

2.5 GaAs HETEROEPITAXY ON THE GRADED SGOI

2.5.1 MBE HETEROEPITAXY TECHNIQUE

MBE involves the direct physical transport of the elemental source to be grown to a heated substrate in a well-controlled, UHV system. Especially for the compound semiconductor, MBE is the most commercially viable technology to control the composition and crystal quality. An MBE growth chamber is equipped with a series of effusion cells to apply the constituent molecular beams, a substrate heater, and a RHEED unit to monitor the surface as a characteristic feature. A schematic drawing of the MBE chamber is illustrated in Fig.2.10.

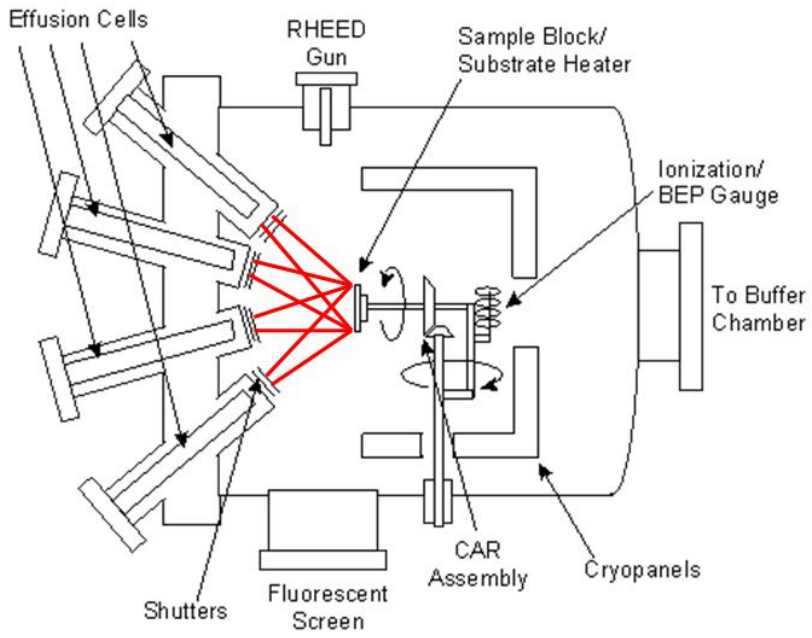


Fig. 2.10 Schematic of an MBE growth chamber showing the beam nature of particle flow from the effusion cell to the substrate.

In MBE, low-energy atoms or molecules arrive at the substrate where they move around without any chemical reaction taking place. Consequently, the cleanliness of the substrate at the atomic level is critical to accomplish a good epitaxy. As a common surface preparation technique before the molecular beam injection and after wet cleaning procedure, *in situ* thermal cleaning is employed. For GaAs homoepitaxy (GaAs on GaAs substrate), thermal cleaning is usually carried out at around 640 ^{o}C, at which point GaAs evaporates congruently [25]. Then diagnostic characterization is provided to determine the degree of surface cleanliness for the initiation of growth. A commonly used diagnostic is RHEED. If the surface is perfectly clean and flat, the electron beam diffracted by the surface shows a series of sharply defined streaks on a fluorescent screen. Rough surface or a significant surface contamination can be appeared as spotty patterns on the screen due to the electron beam penetration and scattering by the surface.

In addition, the crystal quality of GaAs heteroepitaxial layer depends on the film growth technique which consists of atomically controlled nucleation and film growth control. The growth rate of the epilayer is controlled by the flux of each constituent element, j based on the equation,

$$j = \frac{\cos\theta}{\pi l^2}\frac{dN_e}{dt} = 1.17\times10^{22}\frac{PA_e\cos\theta}{l^2\sqrt{MT}} \text{ molecules/cm}^2\text{s} \qquad (2.2)$$

where θ is the angle between the beam axis and the normal to the substrate plane, l the distance from the evaporating surface to the substrate, dN_e/dt is the impingement rate at the equilibrium pressure, P at the effusion cell temperature T, and M is the molecular weight of the species.

In order to control the flux of source more precisely, the design of chamber and effusion cells has been developed. However, the detailed discussion about the

equipment is beyond the scope of this work. Here the technical approach which can be developed in the aspect of process conditions will be discussed.

The process parameters which can control the epi-layer growth mechanism and eventually its quality are temperature and pressure for each source element, Ga and As for GaAs growth.

Another critical factor is related with sticking coefficient of the impinging element on the substrate. At typical GaAs growth temperature around 650 ^{o}C, the sticking coefficient of Ga can be taken as unity. On the other hand, As is disordered due to its high vapor pressure. The desorption energy of As is ~0.4 eV, whereas the bond strength of Ga-As is ~50 eV [25]. Hence, the absolute magnitude of flux should be optimized for each element in relation with the substrate temperature. Moreover, the growth condition is critical to establish that growth occurs in a two-dimensional (2D) layer-by-layer mode. For example, Ga surface diffusion length in the growth of (100) GaAs homoepitaxial layer is varied from ~200 to ~1900 Å where the growth condition is changed from As-stable condition to Ga-stable condition at 550 ^{o}C [25].

Because the substrate is the graded SGOI with high Ge fraction on surface in this work, a high temperature process which can alter the Ge fraction profile should be avoided. In fact, low-temperature MBE condition has been pursued to grow epitaxial layer in heteroepitaxy so far.

In addition to the approach which depends on the growth condition such as temperature and the element flux, migration-enhanced epitaxy (MEE) technique has been introduced as an effective nucleation method to achieve high quality GaAs/AlGaAs interfaces and widely adopted to various heteroepitaxy systems since then [26, 27]. In the MEE mode, the Groups III and V atoms are alternatively deposited on the substrate. As a result, the As concentration is reduced during the Ga

cycle which is believed to enhance the surface migration of Ga atoms and allow the growth of high quality material at low temperatures [28].

Based on these considerations, the development and optimization of MBE process have been carried out for growing device-quality GaAs on the graded SGOI.

2.5.2 EXPERIMENT

GaAs epitaxial layers were grown by MBE on the graded SGOI prepared by the modified two-step Ge condensation method. The range of temperature to grow GaAs epitaxial layers was 480 - 580 ^{o}C with a trial of MEE nucleation technique at 400 ^{o}C. The As_2/Ga beam equivalent pressure (BEP) of 15 was maintained for the co-evaporation at 0.4 μm/h and 20 for MEE at 0.1 μm/h. The MEE sequence was composed of opening the As shutter for 3 s, growth interruption for 3 s, Ga shutter opening for 3 s, and another 3 s of growth interruption. The MEE growth sequence was repeated for 5 cycles. Except for the addition of MEE nucleation step before MBE growth, the other processes, such as pre-cleaning, oxide desorption, RHEED checking, and the MBE growth time, are done in the same way as explained in Sec. 2.2.2. The growth of GaAs on the graded SGOI was estimated by the morphology and composition of the surface first using AFM and XPS. TEM was employed to evaluate the microstructure of the GaAs heteroepitaxial layer grown.

2.5.3 RESULTS AND DISCUSSION

Figure 2.11 shows the results of GaAs MBE growth without MEE nucleation on the 42-nm graded SGOI for different growth temperatures. The relative intensity of Ga/As to Ge in 3d peaks of each XPS measurement can be used as a monitoring tool for the formation of continuous GaAs epitaxial layer on the SGOI. The rms values of

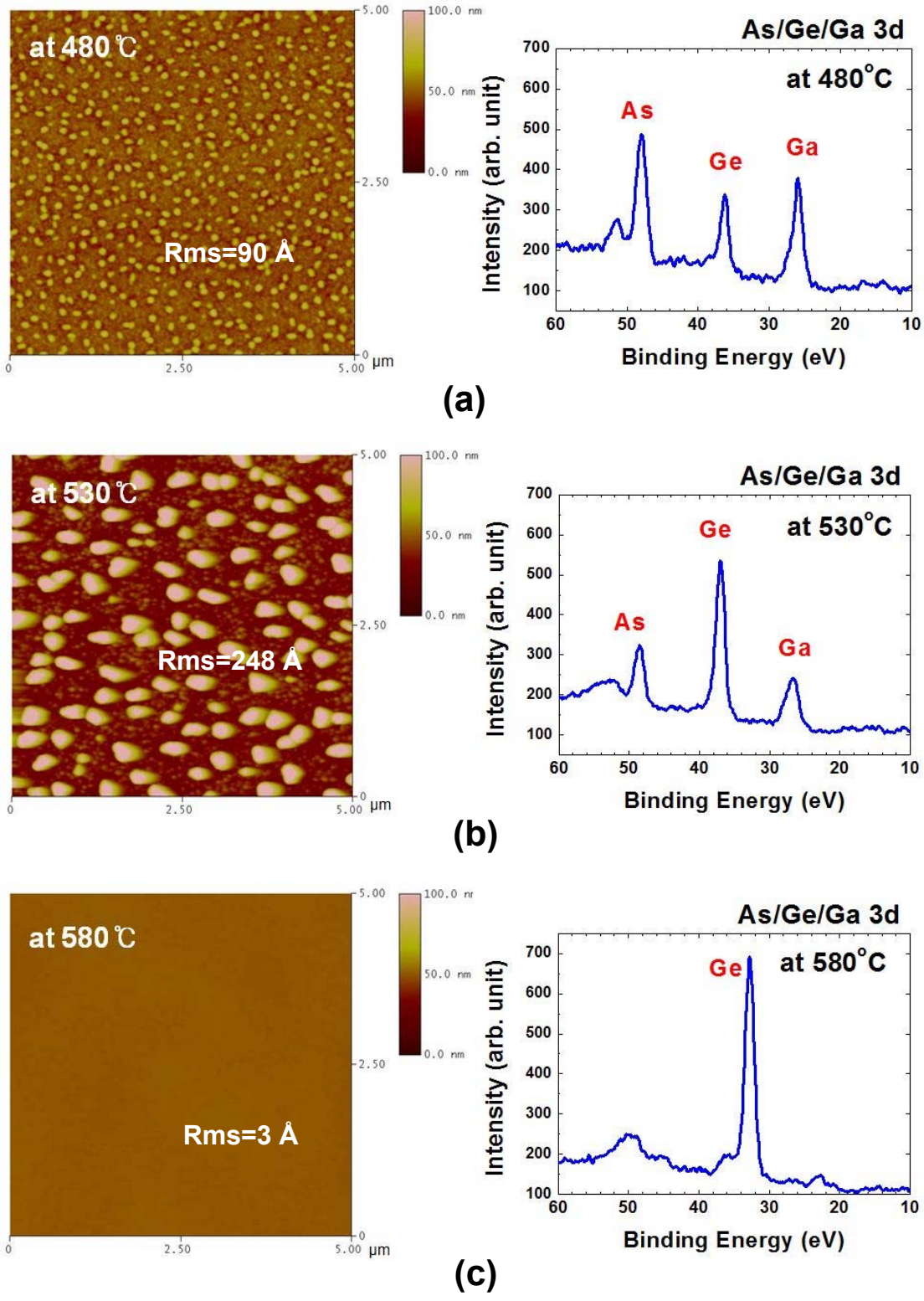


Fig. 2.11 Results of GaAs MBE growths on graded SGOI substrate without MEE nucleation at different MBE temperatures; (a) 480 °C, (b) 530 °C, and (c) 580 °C. GaAs is barely deposited and the measured surface roughness of 3 Å indicates just the surface of SGOI.

the surface roughness were 90, 248, and 3 Å for a, b, and c, respectively, over the area of 5 × 5 μm^2. The relative intensity of Ge peak to Ga/As peak is increasing in the XPS spectra by increasing the growth temperature, which means less coverage of GaAs on SiGe. Finally, the peaks from Ga and As 3d emissions almost disappear at 580 ^oC, indicating almost no growth of GaAs which results in very smooth surface. The island structure is attributed to a significant As re-evaporation and fast Ga migration on a non-GaAs substrate such as Ge [8] and Si [29] during the growth condition.

To overcome this problem, a low-temperature MEE nucleation method is applied. Figure 2.12 shows the results of GaAs MBE growth with MEE nucleation process step prior to MBE growth step. The MEE temperature was fixed at 400 ^oC while the MBE growth temperatures were varied to 480, 540, and 580 ^oC. The surface roughness in rms values measured by AFM were 14, 74, and 242 Å over the area of 5 × 5 μm^2 for 480, 540, and 580 ^oC MBE temperatures, respectively. The relative intensity of Ge peak to Ga/As peak in the XPS spectra shows a similar trend to the case of Fig. 2.11, but the temperature that the island structure started to form becomes higher when MEE nucleation is adopted. As a result, a smooth surfaced GaAs heteroepitaxial layer has been achieved by MBE growth at 480 ^oC with MEE nucleation at 400 ^oC. During the MEE step, the flux of As and Ga is lower than MBE growth and the temperature is also lower, hence the As dimers have covered up the whole surface uniformly and the migration distance of the Ga adatoms has become shorter. This means that the 2D growth mode becomes the dominant mechanism. By increasing the subsequent MBE growth temperature, Ga migration and As re-evaporation increase and three-dimensional (3D) growth mode becomes dominant, resulting in island formation.

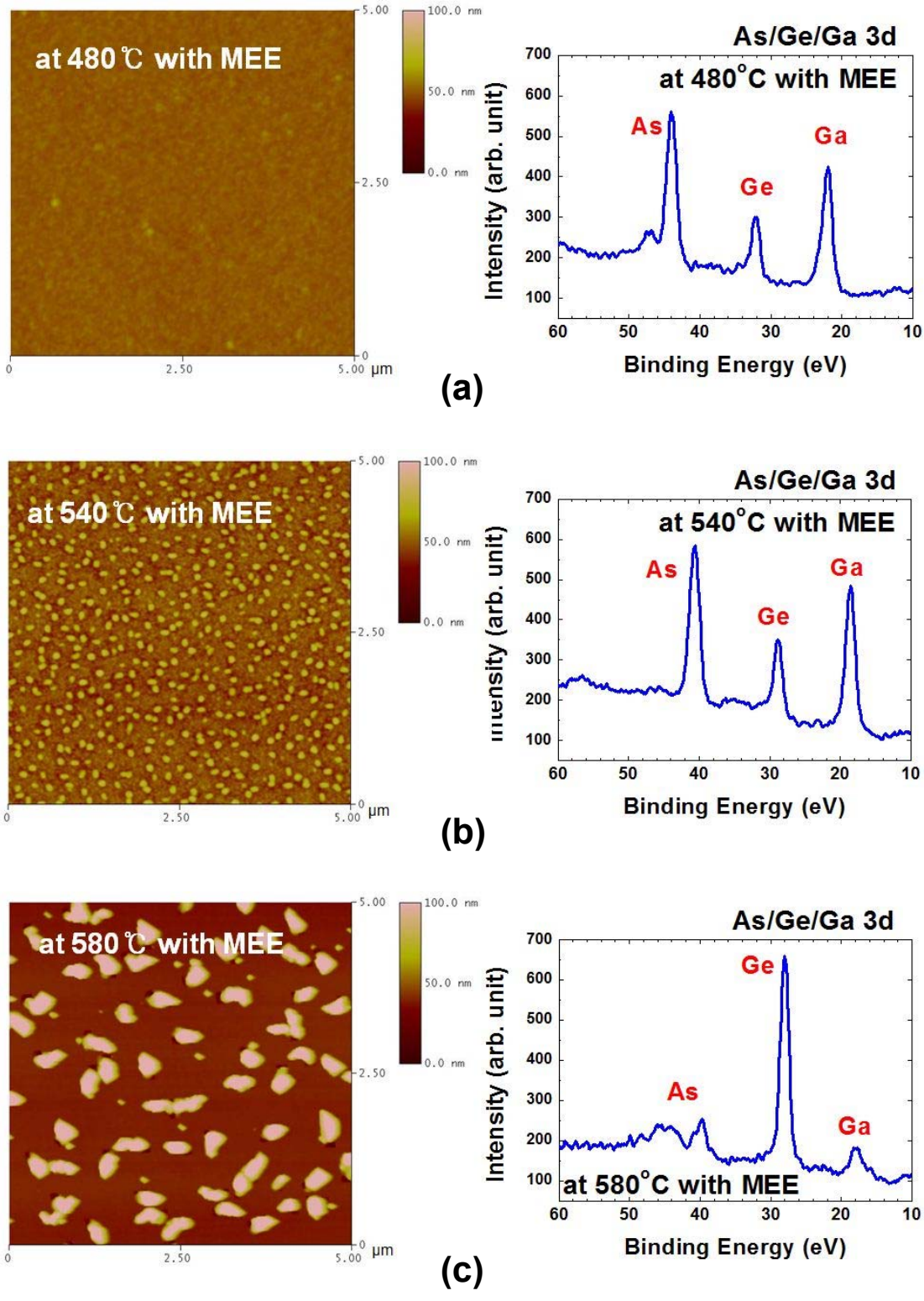


Fig. 2.12 Results of GaAs MBE growths on graded SGOI substrate with MEE nucleation at different MBE temperatures; (a) 480 °C. The XPS $3d_{2/5}$ peaks show a good coverage of GaAs layer on SGOI substrate. (b) 540 °C. GaAs coverage is still good but the surface roughness in rms becomes as high as 74 Å. (c) 580 °C. The GaAs islands are formed on the substrate.

TEM images of the GaAs heteroepitaxy layer on the SGOI substrate are presented in Figs. 2.13 and 2.14 for without MEE and with MEE, respectively. The GaAs layer grown without MEE nucleation shows a discrete film in 3D growth mode with dislocations starting from the interface between the epilayer and SGOI substrate (Fig. 2.13). On the other hand, continuous 8 - 10 nm thick GaAs layer has been grown on the graded SGOI without any dislocation defect in the range of the TEM observation when MEE nucleation has been employed (Fig. 2.14).

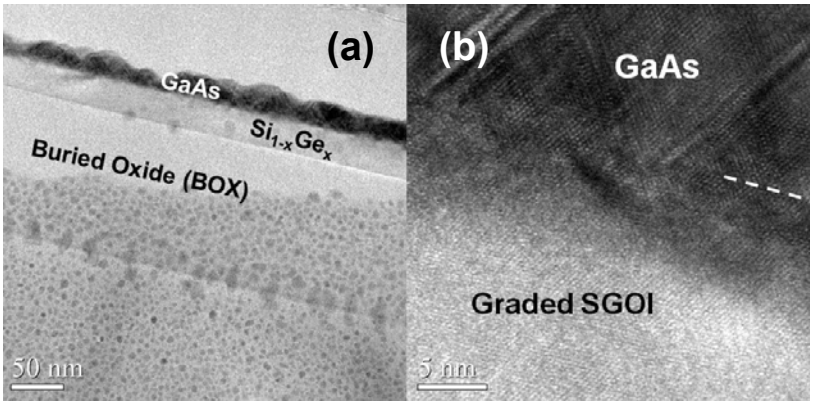


Fig. 2.13 TEM result of GaAs on graded SGOI grown by MBE at 480 ^{o}C without MEE nucleation. TEM images of (a) GaAs/graded SGOI/BOX stack and (b) the GaAs on SGOI at the interface.

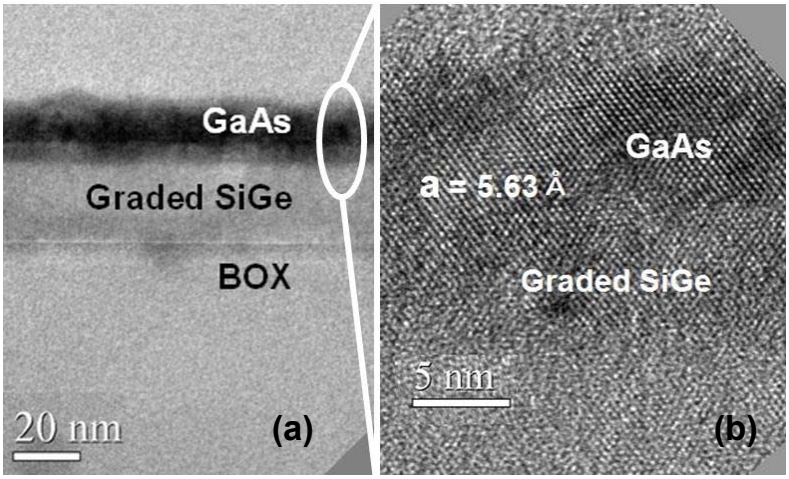


Fig. 2.14 TEM result of GaAs on graded SGOI grown by MBE at 480 ^{o}C with MEE nucleation at 400 ^{o}C (a) TEM image of GaAs/graded SGOI/BOX stack (b) High resolution TEM image of the GaAs on SGOI.

Figure 2. 14 shows that the GaAs lattice is well aligned to the SGOI lattice with significant suppression of dislocation defects, less than 2×10^5 cm^{-1} in a TEM specimen. The measured lattice constant indicates that the GaAs layer is not strained significantly. Any significant threading dislocations were not found in the SGOI also.

2.5.4 CONCLUSION

GaAs MBE growth condition was investigated and optimized for GaAs heteroepitaxial growth on the compositionally graded SGOI. Adopting MEE nucleation at 400 ^oC and low temperature MBE growth at 480 ^oC, a continuous GaAs epilayer was realized with much suppressed dislocation defects on Si-based substrate via graded SGOI structure developed. This result thus indicates the feasibility of GaAs channel NMOSFET on Si platform for future high-speed CMOS device.

2.6 SUMMARY

The compositionally graded SGOI platform is a way to enhance the utility of SiGe or Ge virtual substrate for III-V NMOSFET integration to Si-based CMOS device platform. Modified two-step Ge condensation method allows the SGOI to achieve Ge fraction as high as 71% on the top of the surface in a simple single oxidation process. MBE GaAs epilayer can be grown on the graded SGOI with a high Ge concentration on top and a thin (42 nm) based on the results that the higher Ge concentration close to 1 of the buffer $Si_{1-x}Ge_x$ layer is critical for GaAs to align the smaller SiGe or Si substrate and the buffer layer should be isolated with a thickness less than 80 nm.

Development of a series of the processes, including GaAs MBE growth and graded SGOI fabrication, resulted in successful demonstration of a device quality

GaAs-OI on Si-based substrate for the first time. The heteroepitaxial GaAs lattice is well aligned through the SiGe layer with 71% Ge concentration at the interface. The lattice constant of 5.63 Å of the GaAs epi-layer indicates an almost relaxed GaAs structure.

This compositionally graded SGOI platform has the promising feature of substrate engineering that enable co-integration of GOI PMOS and GaAs-OI NMOS for future carrier-transport enhanced CMOS technology. A major advantage of this platform is that the fabrication processes are fully compatible with manufacturable technology with cost-effective process conditions.

References

[1] Semiconductor Industry Association (SIA), *International Technology Roadmap for Semiconductors [Electronic Resource]: ITRS, 2009 Ed*., San Jose:SIA, 2009, retrieved from http://www.itrs.net

[2] Y. S. Touloukian, R. K. Kirby, R. E. Taylor, and T. Y. R. Lee, Ed., *Thermophysical Properties of Matter- Vol.13 of TPRC Data Series*, New York: Plenum, 1977.

[3] W. A. Jesser, J. H. van der Merwe, and P. M. Stoop, "Misfit accommodation by compliant substrates," *J. Appl. Phys.*, vol. 85, pp. 2129-2139, 1999.

[4] C. W. Pei, J. B. Heroux, J Sweet, W. I. Wang, J. Chen, and M. F. Chang, "High quality GaAs grown on Si-on-insulator compliant substrates," *J. Vac. Sci. Technol. B*, vol. 20, pp. 1196-1199, 2002.

[5] A. R. Hawkins, T. E. Reynolds, D. R. England, D. I. Babic, M. J. Mondy, K. Streubel, and J. E. Bowers, "Silicon heterointerface photodetector," *Appl. Phys. Lett*., vol. 68, pp. 3692-3694, 1996.

[6] J. M. Kuo, Y. C. Wang, K. W. Goossen, L. M. F. Chirovsky, S. P. Hui, B. T. Tseng, J. Walker, A. L. Lentine, R. E. Leibenguth, G. Livescu, et al., "Large array of GaAs modulators and detectors flip-chip solder bonded to silicon CMOS using InGaP as the selective etch stop for GaAs substrate removal", *J. Crystal Growth*, vol. 175-176, pp. 971-976, 1997.

[7] D. Jubia, S. H. Zaidi, S. D. Hersee, and S. R. J. Brueck, "Nanoheteroepitaxy: Nanofabrication route to improved epitaxial growth," *J. Vac. Sci. Technol. B*, vol. 18, pp. 3514-3520, 2000.

[8] P. J. Taylor, W. A. Jesser, J. D. Benson, M. Martinka, J. H. Dinan, J. Bradshaw, M. Lara-Taysing, R. P. Leavitt, G. Simonis, W. Chang, W. W. Clark Ⅲ, and K. A.

Bertness, "Optoelectronic device performance on reduced threading dislocation density GaAs/Si," *J. Appl. Phys*., vol. 89, pp. 4365-4375, 2001.

[9] E. A. Fitzgerald, Y. –H. Xie, D. Monroe, P. J. Silverman, J. M. Kuo, A. R. Kortan, F. A. Thiel, and B. E. Weir, "Relaxed Ge_xSi_{1-x} structures for III-V integration with Si and high mobility two-dimensional electron gases in Si," *J. Vac. Sci. Technol. B*, vol. 10, pp. 1807-1819, 1992.

[10] M. T. Currie, S. B. Samavedam, T. A. Langdo, C. W. Leitz, and E. A. Fitzgerald, "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing," *Appl. Phys. Lett*., vol. 72, pp. 1718-1720, 1998.

[11] J. A. Carlin, S. A. Ringel, E. A. Fitzgerald, M. Bulsara, and B. M. Keyes, "Impact of GaAs buffer thickness on electronic quality of GaAs grown on graded Ge/GeSi/Si substrates," *Appl. Phys. Lett*., vol. 76, pp. 1884-1886, 2000.

[12] F. Schaffler, "Electron and hole mobilities in Si/SiGe heterostructure," in *Properties of Silicon Germanium and SiGe:carbon*, E. Kasper and K. Lyutovich Ed., London: IEE, 2000, p. 198.

[13] A. S. Grove, *Physics and Technology of Semiconductor Devices*, New York: Wiley, 1967.

[14] N. Tachikawa and H. Mori, "Dislocation generation of GaAs on Si in the cooling stage," *Appl. Phys. Lett*., vol. 56, pp. 2225-2227, 1990.

[15] T. Tezuka, N. Sugiyama, and S. Takagi, "Fabrication of strained Si on an ultrathin SiGe-on-insulator virtual substrate with a high-Ge fraction," *Appl. Phys. Lett.*, vol. 79, pp. 1798-1800, 2001.

[16] S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S. Takagi, "Characterization of 7-nm-thick strained Ge-on-insulator layer fabricated by Ge-condensation technique," *Appl. Phys. Lett*., vol. 83, pp. 3516-3518, 2003.

[17] F. Gao, S. Balakumar, N. Balasubramanian, S. J. Lee, C. H. Tung, R. Kumar, T. Sudhiranjan, Y. L. Foo, and D.-L. Kwong, "High germanium content strained SGOI by oxidation of amorphous SiGe film on SOI substrates," *Electrochem. Solid State Lett.* vol. 8, pp.G337-G340, 2005.

[18] A. Powell, S. S. Iyer, and F. K. LeGoues, "New approach to the growth of low dislocation relaxed SiGe material," *Appl. Phys. Lett*., vol. 64, pp. 1856-1858, 1994.

[19] O.W. Holland, C. White, and D. Fathy, "Novel oxidation process in Ge+-implanted Si and its effect on oxidation kinetics," *Appl. Phys. Lett*., vol. 51, pp. 520-522, 1987.

[20] F. K. LeGoues, R. Rosenberg, T. Nguyen, F. Himpsel, and B.S. Meyerson, "Oxidation studies of SiGe," *J. Appl. Phys*., vol. 65, pp. 1724-1728 , 1989.

[21] H.-J. Herzog, "Crystal structure, lattice parameters, and liquidus-solidus curve of the SiGe system," in *Properties of Silicon Germanium and SiGe:carbon*, E. Kasper and K. Lyutovich Ed., London: IEE, 2000, p. 45.

[22] N. Sugiyama, T. Tezuka, T. Mizuno, M. Suzuki, Y. Ishikawa, N. Shibata, and S. Takagi, "Temperature effects on Ge condensation by thermal oxidation of SiGe-on-insulator structures", *J. Appl. Phys*. vol.95, pp.4007-4011, 2004.

[23] F. J. Norton, *Nature (London)*, vol. 191, p. 701, 1961.

[24] M. Ogino, Y. Onabe, and M. Watanabe, "The diffusion coefficient of germanium in silicon," *Phys. Status Solidi A*, vol. 72, pp. 535-541, 1982.

[25] S. K. Ghandhi, *VLSI fabrication principles: silicon and gallium arsenide*, 2nd Ed., New York: J. Wiley, 1994, p.279

[26] Y. Horikoshi, M. Kawashima, and H. Yamaguchi, "Low-temperature growth of GaAs and AlAs-GaAs quantum-well layers by modified molecular beam epitaxy," *Jpn. J. Appl. Phys*., vol.25, pp. L868-L870 , 1986.

[27] T. S. Rao, K. Nozawa, and Y. Horikoshi, "Growth of GaAs on hydrogen-fluoride treated Si (100) surfaces using migration-enhanced epitaxy," *Appl. Phys. Lett*., vol. 60, pp. 1606-1608, 1992.

[28] Y. Horikoshi, M. Kawashima, and H. Yamaguchi, "Migration-enhanced epitaxy of GaAs and AlGaAs ," *Jpn. J. Appl. Phys*., vol. 27, pp. 169-179, 1988.

[29] S. F. Fang, K. Adomi, S. Iyer, H. Morkoc, H. Zabel, C. Choi, and N. Otsuka, "Gallium arsenide and other compound semiconductor on silicon," *J. Appl. Phys*., vol. 68, pp. R31-R58, 1990.

CHAPTER 3

HIGH MOBILITY CHANNEL NMOSFET INTEGRATED WITH HIGH-*k*/METAL GATE

3.1 INTRODUCTION

3.1.1 MOTIVATION

One of the most difficult challenges in demonstrating the high-performance III-V NMOSFET, which is mostly based on GaAs, is to develop the deposition of high-*k* dielectrics with unpinned Fermi level, maintaining good interface properties after device fabrication. A poor dielectric interface due to a large D_{it} leads to Fermi level pinning, which makes the gate control over the channel conductance difficult in MOSFET device operation. Hence, a great deal of effort has been made to realize an oxide interface with GaAs with unpinned Fermi level. The factors causing the Fermi level pinning on GaAs are starting to be understood [1] and much progress has been made to form a high-quality gate dielectric on III-V semiconductor adopting an advanced Si process technology [2-4]. However, the realized device performance is not as good as anticipated by the intrinsic material properties of GaAs-based III-V semiconductors as reviewed in Chapter 1. Therefore better material combinations or techniques to integrate the good interface are needed to realize the carrier-transport superiority in MOSFET devices and understand the underlying physics to improve the device characteristics in the nano-scaled device regime.

To demonstrate high-performance III-V NMOSFET, which can extend CMOS scaling beyond 10 nm technology node, some process requirements can be considered for cost-effective mass production in the near future, as well as the interface quality requirements. First, the high-*k* dielectrics should be deposited with conformal step coverage because the non-planar channels of multiple-gate structures like FinFET will be used to suppress SCE for the deeply scaled MOSFETs. Therefore, ALD or MOCVD high-*k* deposition techniques would be more adequate for advanced III-V channels rather than physical vapor deposition (PVD) method. Secondly, the thermal stability of the high-*k* gate stack on III-V channels should be enough for the gate-first fabrication scheme. Although the use of metal gate electrode may reduce the thermal budget of MOSFET fabrication, the S/D activation or anneal step still needs to be carried out at a high temperature. The thermodynamic stability of high-*k*/metal gate stack on III-V channel, therefore, is another important requirement for MOSFET fabrication. Thirdly, enhancement mode (E-mode) MOSFET is favored because it is a 'normally-off' device, meaning when there is no gate bias applied, the channel is off, and this greatly reduces the standby power of devices and circuits. An E-mode MOSFET relies on semiconductor surface inversion to turn on. When considering the scalability of channel dimension, surface channel MOSFET with inversion-type E-mode may be the most adequate device type. The unequivocal demonstrations of GaAs E-mode transistor have made only after $Ga_2O_3(Gd_2O_3)$ dielectric integrations using UHV MBE dielectric deposition techniques recently [5]. Since that demonstration, advanced deposition techniques which are compatible with commercial MOS technology such as ALD [6] have explored and successfully demonstrated the E-mode GaAs MOSFET integrating with high-*k* dielectrics. However, the demonstrations have achieved in the gate-last scheme where the high-temperature S/D activation process is

carried out before the high-*k* deposition [5, 6], indicating that the gate stack is thermally unstable.

3.1.2 GaAs-BASED III-V MOSFET AND FERMI LEVEL PINNING

This section briefly reviews, the major research achievements on understanding and resolving the Fermi level pinning issue in GaAs-based III-V MOSFETs.

The difficulty in realizing E-mode GaAs MOSFET is the Fermi level pinning issue. High density of surface states over 10^{12} $eV^{-1}cm^{-2}$ is regarded one of the main causes of the Fermi level pinning in MOSFET. Many experiments to search working combination of dielectric and III-V for MOSFET devices were carried out in the 1980s and Wilmsen [7] provided a comprehensive and extensive summary of those works, giving fundamental knowledge on realizing and understanding the interface problem. However, it is difficult to find any significant breakthrough or plausible technical solution to solve the Fermi level pinning problem.

Absence of stable native oxide and low sublimation temperature of arsenic oxide (350 ^{o}C) have been pointed out as sources of the surface states without direct evidences. Eguchi and Katoda [8] provided a significant contribution that showed elemental As precipitated by solid-state interfacial reaction at the GaAs-based III-V semiconductor/oxide interface during annealing at 400-460 ^{o}C after anodic oxidation using laser Raman spectroscopy. The experimental result agreed with the solid-state interfacial reaction, which Schwartz et al. proposed as following formula [9]:

$$As_2O_3 + 2GaAs \rightarrow Ga_2O_3 + 4As \tag{3.1}$$

However, because this proposal was based on the assumption that the interfacial reaction between the mixed GaAs native oxides and GaAs is governed only thermodynamic factor, this reaction mechanism could explain the origin of the surface

states in a limited process condition and only in the case of GaAs. Hollinger et al. pointed out that native oxides of GaAs-based III-V semiconductors did not grow close to thermodynamic equilibrium and kinetic factors very often played a major role as a result of the XPS studies [10]. This study gave the academia better understanding of the local chemical bonding in III-V native oxides based on the empirical observation. However, GaAs E-mode MOSFET devices have not been realized until the *in situ* UHV MBE $Ga_2O_3(Gd_2O_3)$ dielectric is employed on the re-grown GaAs surface [5].

Recently the underlying physics and chemistry of the Fermi level pinning have been studied with advanced experiments, analysis techniques, and the successful fabrication of E-mode GaAs MOSFET. The microscopic surface studies of GaAs in an atomic level using scanning tunneling microscopy (STM) and scanning tunneling spectroscopy (STS) showed that oxidation mechanism by itself may generate substantial electronic defects instead of the decomposition of As_2O_3, resulting in Fermi level pinning [1,11]. Kummel *et al.* described their STM observations, wherein it was found that in the initial stage of oxidation, oxygen atoms displace top layer As atoms and consequently bond to the second layer Ga atoms [11]. The displaced As atoms from the top layer As dimers are localized at the nominal Ga vacancy sites in the trenches, generating isolated As_{Ga} antisites (As atoms on Ga sites in the GaAs lattice) and isolated undimerized As atoms with half-filled dangling bonds. On the other hand, at higher oxygen exposures, As pair displacement by oxygen atoms becomes more favorable, changing to the oxidation behavior previously observed with molecular oxygen [12]. STS experiments showed that the Ga_2O bonding to the As dimers leaves the Fermi level unpinned, while density functional theory (DFT) modeling shows that good electrical properties are due to Ga_2O restoring the surface As atoms to a more bulk-like charge state. This explains the successful demonstration of the E-mode GaAs

MOSFET using MBE $Ga_2O_3(Gd_2O_3)$ dielectric [5]. However, the Ga_2O passivation is not compatible with Si processes because it can be accomplished with *in situ* III-V re-growth and oxide MBE under UHV conditions. In addition, the material properties of $Ga_2O_3(Gd_2O_3)$ dielectric, such as the permittivity of 14.2 [13] and its hygroscopic nature upon air exposure [14, 15], are not adequate for CMOS applications compared to Hf-based high-*k* films from a scaling point of view. The validity of the Ga_2O passivation mechanism may also be limited only to GaAs or GaAs-based III-V with high composition of GaAs [16].

From those results based on experimental works, the presence of the unstable native oxide of GaAs causes the poor quality of GaAs-based III-V/dielectric interface, although it is still arguable which chemical species (AsO_x, GaO_x, or elemental As) is the exact cause and what mechanism works.

For the theoretical approach, Spicer et al. proposed the advanced unified defect model (AUDM) for GaAs to explain Fermi level pinning on III-V compound semiconductor [17]. The AUDM defined the pinning levels at 0.75 and 0.5 eV above the valence band maximum (VBM) as the As_{Ga} antisite defect. This model is highly advantageous in providing a quantitative electrical simulation tool where the Fermi level pinning occurs due to the elemental As at the GaAs-based III-V/oxide interface. However, it failed to prevent the evolution of defects.

Recently, Ye proposed a model of the gap state of GaAs based on the concept of metal-induced gap states (MIGS) based on their promising and wide-ranging unpinned Fermi level experimental results using ALD technique, which is the most important process technique in fabricating MOSFET [18]. However, Robertson suggested a native defect model for the D_{it} causing Fermi level pinning in FETs, which is based on Ga/As dangling bonds like Si/SiO_2 interfaces as a source of the interface

state with pointing out that MIGS do not exist in the semiconductor gap next to a wider bandgap oxide [19]. This native defect model has potential in that it possesses the advantage of defining the nature of the interface state as an extrinsic defect, that means developments of processing conditions in fabricating MOSFET to remove native defects can achieve the unpinned Fermi level in III-V MOSFET as well as understanding the III-V MOSFET device malfunction due to the Fermi level pinning.

3.1.3 OBJECTIVE

For the second part of this thesis, the development of Hf-based high-*k* deposition to integrate GaAs-based III-V NMOSFET and demonstration of high electron mobility NMOSFET integrated with the high-*k*/metal gate stack was aimed using the framework of CMOS compatible processes. The MOSFET fabrication includes MOCVD high-*k* deposition, TaN metal gate, and self-aligned MOSFET fabrication scheme, in contrast to the recent successful demonstrations based on the gate-last scheme [2, 5, 18]. To achieve unpinned Fermi level in MOSFETs, the fabrication process development has been carried out with emphasis on formation of a good III-V/high-*k* interface, wherein the presence of surface species such as GaAs-oxides is effectively suppressed. The impact of deposition conditions and material combinations on the interface properties of MOCVD high-*k* dielectrics on GaAs-based III-V substrates has been examined using XPS. The pre-deposition cleaning and S/D formation processes with the substrate effect have been examined using electrical properties. Consequently, a high-performance E-mode InGaAs channel NMOSFET has been demonstrated with the optimized fabrication processes of high-*k*/metal gate stack in a self-aligned gate-first process scheme. The process development for ohmic contact formation on III-V was not included in this work.

3.2 PROCESS OPTIMIZATION BY MATERIAL CHARACTERIZATION

We have investigated the impact of high-*k* deposition temperature and the combination of GaAs-based III-V and Hf-based MOCVD high-*k* materials on the interface properties of GaAs-based III-V/high-*k* system. We used GaAs and lattice matched $In_{0.53}Ga_{0.47}As$ on InP wafer for the GaAs-based III-V substrates. For the Hf-based MOCVD high-*k*, we studied HfO_2 and HfAlO deposition using hafnium tetra tert-butoxide [HTB, $Hf(OC(CH_3)_3)_4$] and bis(1-methoxy-2-methyl-2-propoxy) penta(2-propoxy) aluminum hafnium [HA-2, $HfAl(OiPr)_5(MMP)_2$] precursors, respectively. XPS was employed to investigate the III-V/high-*k* interfaces with an Al *Kα* X-ray source (1486.6 eV) at 90^o take-off angle (TOA). The XPS measurements were carried out *ex situ* but minimizing the air exposure less than 10 min. The dielectric film thickness was verified by ellipsometry. TEM was used to verify the interface quality.

3.2.1 MOCVD HIGH-*k* DEPOSITION

Although ALD has certain advantages in terms of control of interface and film homogeneity, if a simple CVD method can be devised to grow a high-*k* film on III-V with appropriate properties it would be easier to incorporate in a commercial industrial environment. One of the interesting findings of recent study on high-*k* deposition on GaAs-based III-V compounds is the phenomenon of self-cleaning of interfacial As-oxide during ALD Al_2O_3 and HfO_2 depositions [4, 20-24, 27]. The metal-organic precursors which show the self-cleaning effect on GaAs-based substrates are trimethyl aluminum, $Al(CH_3)_3$, i.e., TMA [4, 20-22], dimethyl aluminum hydride, $(CH_3)_2AlH$, i.e. DMAH [23], and tetrakis(ethyl methyl amino)hafnium, $Hf(NCH_3C_2H_5)_4$, i.e.,

TEMAH [21, 24, 27] to the present. Since the interfacial native oxide of GaAs is believed to be one of the well-known sources causing Fermi level pinning, this study examines the interfacial self-cleaning attribute of metal precursors for MOCVD HfO_2 and HfAlO to optimize their deposition temperatures. XPS was measured using JEOL JPS-9010MX spectrometer in this investigation.

3.2.1.1 HfO_2

For the deposition of CVD HfO_2 film in our experiment, we used an alkoxide, HTB as the metal precursor. HTB has some advantages compared to other hafnium molecular precursors. HTB has a relatively high vapor pressure (~0.07 Torr at 25 ^oC and ~1 Torr at 65 ^oC) thus minimizing the heating of precursor and delivery lines. It does not decompose at temperatures below 225 ^oC, significantly reducing complications due to chamber wall or gas phase reactions [25].

The MOCVD HfO_2 films were deposited on non-cleaned GaAs wafers using HTB (0.1 M in octane) and O_2 at 300, 350, and 400 ^oC. The chamber pressure was 0.4 Torr during film deposition with Ar carrier gas. The native oxide thickness measured before HfO_2 deposition was 1.3 nm and the thicknesses after a 2 nm thick film deposition at 300, 350, and 400 ^oC were 1.6, 2.5, and 1.7 nm, respectively. Figure 3.1 is an Arrhenius plot of the deposition rate as a function of temperature (ln rate vs 1/T), showing an activation energy of 52 kJ/mole. Deposition rates were evaluated by depositing 50 - 100 Å thick films on the GaAs substrates.

Figure 3.2 illustrates the As 3d and Ga 3d spectra of the non-cleaned GaAs samples after thin (~2 nm) HfO_2 dielectric depositions at different temperatures compared to the GaAs without HfO_2 deposition. The study of interfacial native oxide is critical to understand the electrical behavior of GaAs-based MOS devices.

Especially, As oxide is the well known unstable species that causes oxide-induced Fermi level pinning through dissociation into As atoms on the GaAs surface [9, 12, 28]. All of the samples show significant native oxide peaks, especially for As oxides at 44-46 eV. The broad As-O peak indicates various As oxides on GaAs surface. The As oxide peak can be deconvoluted into two peaks at 44-44.3 and 45.7-45.8 eV using Gauss-Lorentz fitting. The peak at lower binding energy (BE) corresponds to lower oxidation state attributed to As_2O_3 [22, 26] while the other to As_2O_5 [10, 22, 27].

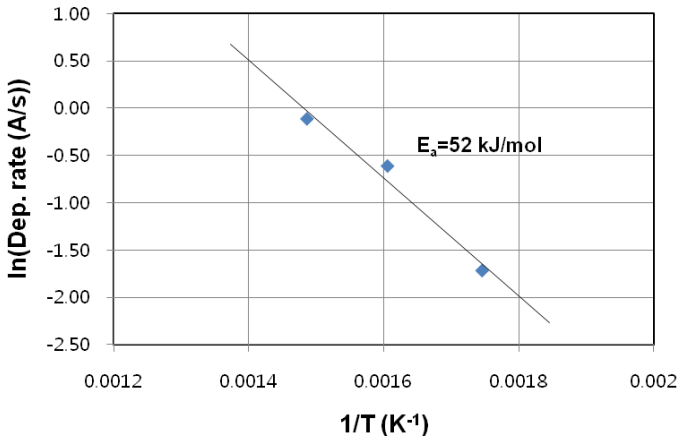


Fig. 3.1 Arrhenius plot of the logarithm of the HfO_2 deposition rate vs inverse temperature.

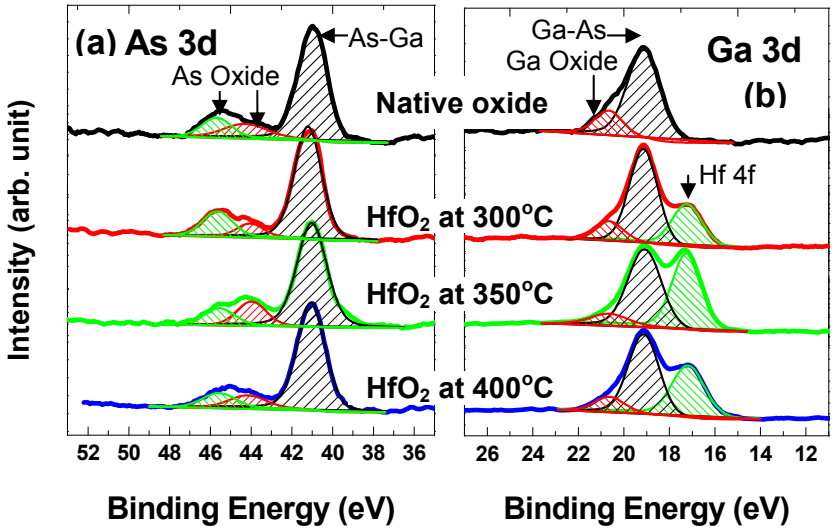


Fig. 3.2 (a) As 3d and (b) Ga 3d XPS spectra showing composition difference of surface oxide film for a native oxide and subsequent ~2 nm HfO_2 depositions at different temperatures on a GaAs surface.

Figure 3.3 shows the area ratio of As oxide peak over total As 3d peaks by the samples. The reduction of As oxide by the HfO_2 CVD, i.e., a self-cleaning phenomenon is not prominent comparing to the case of ALD using TEMAH precursor reported [21, 24, 27]. This can be due to the deposition condition where O_2 is used as an oxidant of HTB. However, the reduction of As oxide by CVD HfO_2 deposition is observed at 400 ^oC deposition. This reduction may be attributed to the thermal decomposition of As oxides rather than conversion reaction to more stable Ga oxide because any significant increase of Ga oxide is not observed for the 400 ^oC sample (Fig. 3.2b). Further study with the impact of oxidant gas and temperature is needed to understand the interfacial reaction during the HfO_2 deposition on GaAs where the alkoxide metal precursor, HTB is used.

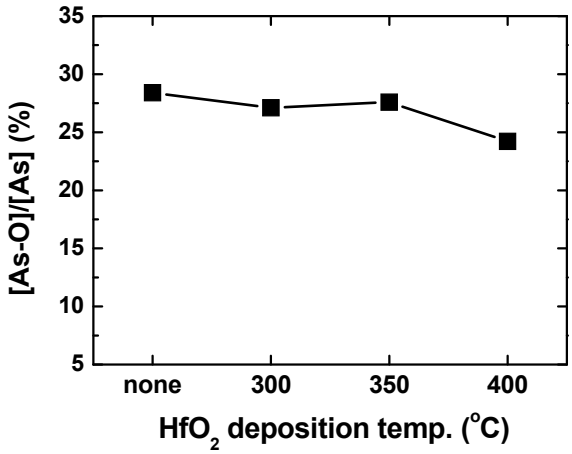


Fig. 3.3 The ratio of the peak area of As oxide peak to total As 3d area by the HfO_2 deposition temperature for the GaAs samples deposited 2 nm HfO_2.

In conclusion, HfO_2 deposition at 400 ^oC may integrate better interfacial quality in GaAs-based III-V/HfO_2 gate stack for NMOSFET than the other deposition temperatures in the MOCVD system that we used.

3.2.1.2 HfAlO

ALD Al_2O_3 has demonstrated a good quality interface with GaAs-based III-V compound so far [2, 18, 20-23]. The low *k* of ~9, however, may pose a serious limitation for Al_2O_3 to be used to further gate dielectric scaling into the regime of EOT of 1 nm. HfO_2 with low concentration of Al_2O_3, thus, can be a promising high-*k* candidate allowing a higher *k* than Al_2O_3 and better thermal stability than HfO_2 [29]. For the deposition of CVD HfAlO film, a single cocktail source of HA-2 was used. HfAlO deposition temperatures were varied from 350 to 450 ^oC, based on the previous experiments on Si wafers using the MOCVD system [29]. The Arrhenius plot of deposition rate as a function of temperature is presented in Fig. 3.4. The activation energy of 98 kJ/mol may show that the thermal decomposition of HA-2 plays more important role in HfAlO deposition than in HfO_2 deposition using HBT of which the activation energy is 52 kJ/mol. The thicknesses measured after the depositions of 2 nm thick HfAlO films for XPS sample preparations on non-cleaned GaAs wafers were 1.8, 0.9, and 0.9 nm for 350, 400, and 450 ^oC samples, respectively. These thickness results are much less than the thickness expected from the deposition rate.

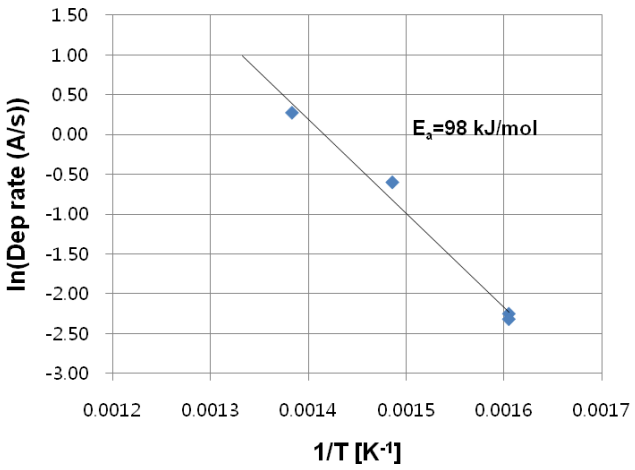


Fig. 3.4 Arrhenius plot of the logarithm of the HfAlO deposition rate vs inverse temperature.

In contrast to the XPS result of HfO_2 deposition using HTB, significant change in As oxide is observed for the HfAlO films covered on GaAs native oxide as shown in As 3d core level XPS spectra in Fig. 3.5a. The mixed As oxidation states of native oxide are reduced to As^{3+}, which can be fit with only one peak at 44.3-44.4 eV, after HfAlO deposition. In addition, the peak area of the As^{3+}, which may corresponds to As_2O_3, decreases with increase of HfAlO deposition temperature.

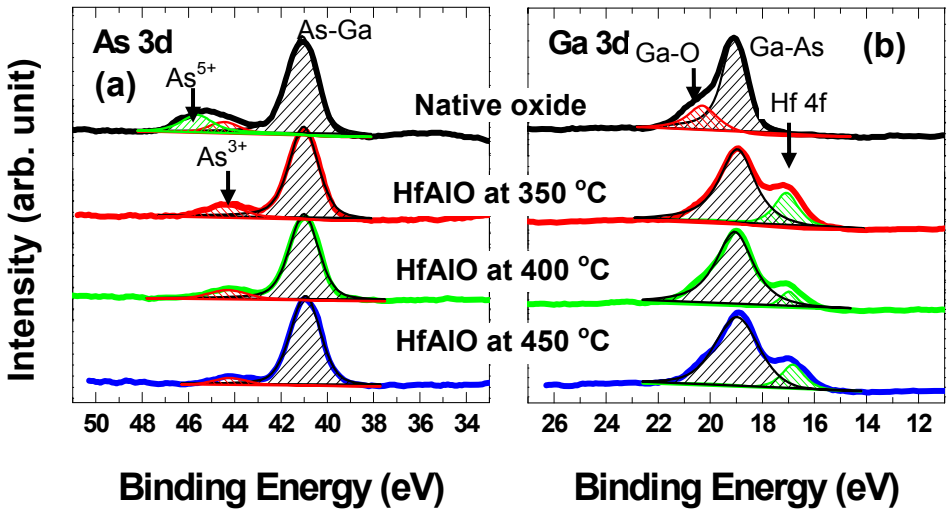


Fig. 3.5 (a) As 3d and (b) Ga 3d spectra showing the composition of surface oxide film for a native oxide of GaAs and subsequent ~2 nm HfAlO depositions on the non-cleaned GaAs surface at different temperatures.

The chemical composition of HfAlO deposited using HA-2 precursor depends on the relative decomposition of the source into Al_2O_3 and HfO_2. The HfO_2 composition, x in HfAlO [= $(HfO_2)_x(Al_2O_3)_{1-x}$] alloy dielectric increases from 0.45 to 0.9 with increase of deposition temperature from 350 to 450 ^oC [29]. It is reported that As^{3+} chemical state of native oxide of GaAs is significantly reduced first by Al_2O_3 deposition using TMA metal precursor, while As^{5+} peak is vanished more rapidly than As^{3+} by HfO_2 deposition using TEMAH source [21, 27]. Although the metal precursor used in this work is different from those in the previous reports [21, 27], the present

XPS result may indicate that the Hf-bonded precursor part plays a major role in the self-cleaning effect on removal of the native oxide where the HA-2 cocktail source is used. The self-cleaning phenomenon by the metal precursor can be supported by the fact that the removal of As_2O_5 before As_2O_3 is contradictory with thermodynamic equilibrium data. The Gibbs energies of formation are -187 and -137.7 kcal/mol for As_2O_5 and As_2O_3, respectively [10]. Therefore the removal of As oxide may not be governed by thermodynamic factor predominantly. Ga oxide reduction by HfAlO deposition is also found (Fig. 3.5b). It is reported that the reduction of Ga oxide is less than As oxide reduction in HfO_2 1 nm deposition on GaAs sample covered with native oxide where TEMAH source is used [21]. This is comparable with the present result. It is worth noting that HfAlO deposition is carried out without O_2 gas in contrast to HfO_2 deposition using HTB.

The peak area ratio of As oxide peak to total As 3d peak is illustrated as a function of deposition temperature of HfAlO CVD in Fig. 3.6.

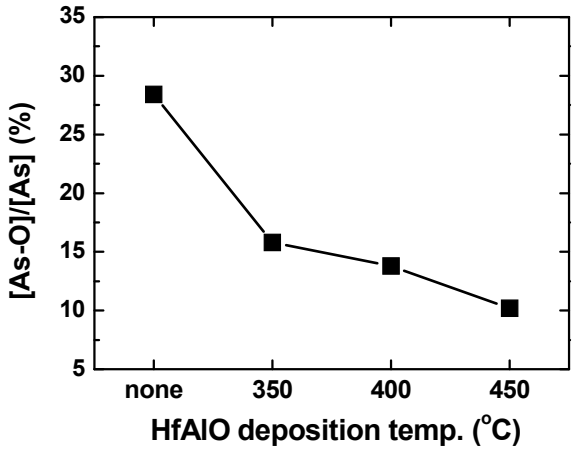


Fig. 3.6 The area ratio between the peaks from As oxide and total As 3d for the different GaAs samples where 2 nm thick HfAlO films were deposited on non-cleaned GaAs (indicated as native oxide) at different temperatures.

In summary, it is found that there is a self-cleaning effect in HfAlO CVD on GaAs using HA-2 metal precursor for the first time. The amount of As oxide is reduced to 35 % by HfAlO CVD at 450 ^{o}C on GaAs surface without any chemical treatment.

3.2.2 GaAs-BASED III-V/Hf-BASED HIGH-*k* INTERFACE

Among III-V semiconductors to be used for surface channel MOSFET applications, the ternary alloy $In_{0.53}Ga_{0.47}As$ lattice matched to InP is one of the most attractive material due to its high low-field electron mobility and saturation velocity allowing high cut-off frequency and switching speed. Recently, high-performance inversion-type E-mode III-V NMOSFETs were successfully demonstrated using InGaAs channel [6, 13, 15, 30, 31], showing that the drive current is improved with In concentration in InGaAs up to 0.65 [18]. The improvement of the GaAs MOSFET performance on InGaAs channel seems to be due to not only the material property of that III-V semiconductor itself, but also the better quality of III-V-dielectric interface, although the relative effectiveness is remained as a further research topic. Actually, since a few successful demonstrations of E-mode MOSFET on p-$In_{0.53}Ga_{0.47}As$ in the 1980s, it has been believed that $In_{0.53}Ga_{0.47}As$ can achieve more robust MOS structures with smaller D_{it} near midgap than those of GaAs MOS structures [32]. In spite of those believes, the interface study of p-$In_{0.53}Ga_{0.47}As$/dielectric has seldom been carried out to reveal what causes the improvement from GaAs system.

In this section, we present the study of the interface properties of MOCVD HfAlO and HfO_2 on p-$In_{0.53}Ga_{0.47}As$ channel layer comparing to the cases of p-GaAs substrate using XPS and TEM characterizations. In addition, the band offsets of GaAs and InGaAs/HfAlO and HfO_2 systems have been extracted by using XPS.

3.2.2.1 CHEMICAL AND PHYSICAL PROPERTIES OF INTERFACES

High-*k* dielectric layers were deposited both on Zn-doped p-GaAs wafers with a doping concentration of 1×10^{16} cm^{-3} and on p-type $In_{0.53}Ga_{0.47}As$/InP substrates. 200 nm p-doped 1×10^{18} cm^{-3} InP buffer and 500 nm p-doped 1×10^{17} cm^{-3} $In_{0.53}Ga_{0.47}As$ were sequentially grown by MBE on a 2-inch p^+ InP substrate. In order to investigate the impact of substrate material, both of the wafers underwent identical processing steps. The wafers were cleaned in a 10 % HCl solution, followed by a sulfur treatment dipping in a $(NH_4)_2S$ solution. Then the wafers were immediately loaded into a multi-chamber MOCVD system. High-*k* dielectric deposition and a post-deposition annealing (PDA) were carried out without breaking a vacuum in the MOCVD system. MOCVD HfO_2 film was deposited using HTB source at 400°C. For HfAlO deposition, HA-2 precursor was used and the deposition temperature was 450°C where the HfAlO film was composed of 90% HfO_2 and 10% Al_2O_3. In order to study the interfacial chemical structure and energy band alignments using XPS, a thin (~2 nm) and thick (~20 nm) high-*k* films were deposited on the substrates and PDA was done at 400°C for 1 min. In this experiment, high resolution XPS measurements were performed by using a VG ESCALAB 220i-XL system using monochromatic Al Kα source (1486.6 eV) with a pass energy of 10 eV.

Figure 3.7 shows the XPS spectra of the As 3d, Ga 3d, and In 3d peaks from the thin high-*k* dielectrics on p-$In_{0.53}Ga_{0.47}As$/InP and p-GaAs substrates. The As 3d spectra from the p-GaAs/HfAlO stack (iv), the p-GaAs/HfO_2 stack (iii), and the p-$In_{0.53}Ga_{0.47}As$/HfO_2 (i) samples show an additional peak at higher BE (44.5-46 eV) which represents As oxides with higher oxidation states of $As^{3+\sim5+}$ [10, 22, 26, 27] while it is not observed in the spectrum of the $In_{0.53}Ga_{0.47}As$/HfAlO sample (Fig. 3.7a-ii). Although there is a complex mixing from In 4d peak, Ga 3d peak, and Hf 4f

doublets in the range of BE from 16 to 20 eV, no significant shoulder due to Ga-O bond is observed near 20.4 eV [10] (Fig. 3.7b). In 3d spectra from the $In_{0.53}Ga_{0.47}As$/HfAlO and the $In_{0.53}Ga_{0.47}As/HfO_2$ samples also do not show an extra peak due to In-O bond significantly (Fig. 3.7c). However, the formation of In-O is clearly observed after annealing $In_{0.53}Ga_{0.47}As/HfO_2$ sample at 600 ^oC (Fig. 3.7c-v).

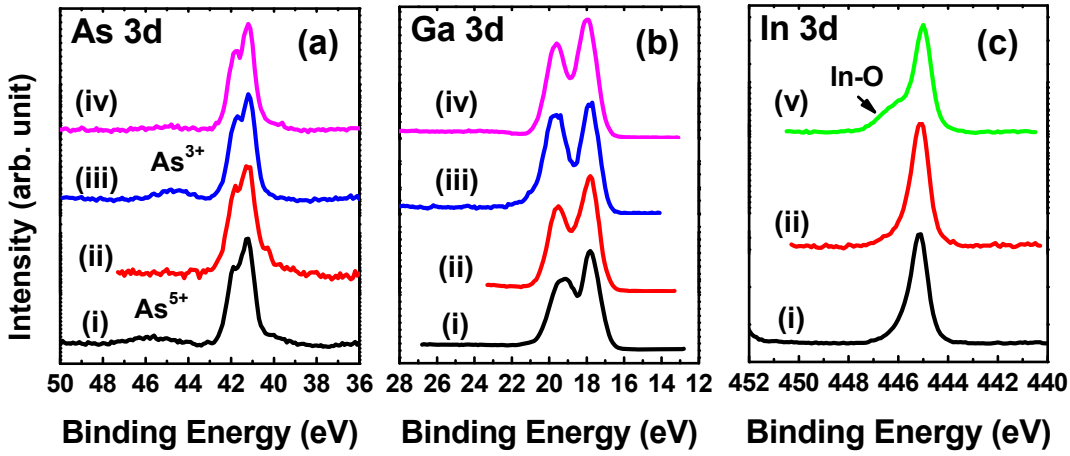


Fig. 3.7 XPS spectra of (a) the As 3d peak, (b) the Ga 3d peak, and (c) the In 3d peak for (i) 2nm thick HfO_2 on $In_{0.53}Ga_{0.47}As$, (ii) 2 nm thick HfAlO on $In_{0.53}Ga_{0.47}As$, (iii) 2 nm thick HfO_2 on GaAs, and (iv) 2 nm thick HfAlO on GaAs after annealing at 400 ^oC for 1 min. (v) is the In 3d peak for 2 nm thick HfO_2 on $In_{0.53}Ga_{0.47}As$ which annealed at 600 ^oC for 1 min after the dielectric deposition.

Chang et al. reported the self-cleaning effect of As oxide reduction by ALD HfO_2 using TEMAH source while the existence of In_2O_3, $In(OH)_3$ and Ga_2O_3 at the interface between the ALD HfO_2 and n-type $In_{0.53}Ga_{0.47}As$ channel layer was observed [33]. Our experimental observation is not consistent with the report, which may be attributed to the difference in high-*k* deposition process including pre-deposition wet-chemical cleaning process. It is reported that wet-chemicals applied prior to high-*k* depositions affect the surface native oxide species and their relative concentrations in

GaAs/high-*k* systems [21, 34]. Wet chemical treatment using HF or HCl reduces native oxide on GaAs significantly [4, 34]. Figure 3.8 shows the As 3d XPS spectra of the GaAs and $In_{0.53}Ga_{0.47}As$ surfaces measured immediately after HCl cleaning. The peaks due to the Ga-O or In-O bonds are not significantly observed in Ga 3d and In 3d spectra (not shown). Relatively intense As oxide peak is observed on the HCl cleaned GaAs as reported by Cheng et al. [34]. Compared to As 3d XPS line for the native oxide of GaAs in previous section (Fig. 3.2 and 3.5), As_2O_5 reduction is more remarkable than As_2O_3 decrease by HCl cleaning. The remained As_2O_3 after high-*k* deposition (Fig. 3.7a-iii and iv) is consistent with the XPS results of the self-cleaning and HCl cleaning experiments. In contrast to GaAs sample, no extra peak due to As-O bond is detected on the $In_{0.53}Ga_{0.47}As$ surface although the exposure time in the air is same with the GaAs sample.

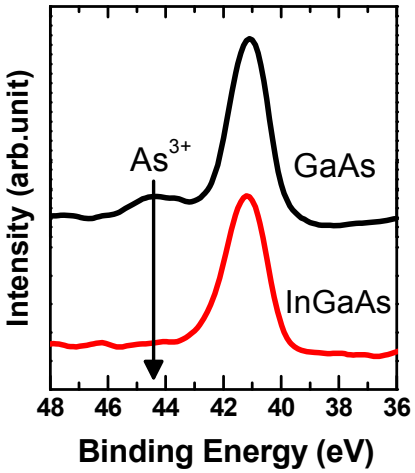


Fig. 3.8 XPS spectra of the As 3d peaks for GaAs and $In_{0.53}Ga_{0.47}As$ after HCl cleaning.

Based on these XPS results, the formation of the undesirable native oxide, especially for As oxide, appears to be significantly suppressed on $In_{0.53}Ga_{0.47}As$

surface. In terms of Gibbs free energy of oxide formation, As-oxide is less stable than the other oxides such as Ga_2O_3, $GaAsO_4$, In_2O_3, and $InAsO_4$ (As_2O_3: -137.7 kcal/mol; Ga_2O_3: -238.6 kcal/mol; $GaAsO_4$: ~-223 kcal/mol; In_2O_3: -198.6 kcal/mol; $InAsO_4$: -209.4 kcal/mol) [10]. On the other hand, according to the surface studies, *c*(4×4) structure, in which As dimers exist in the topmost layer with (4×4) periodicity, is known as the most stable and common surface structure model on GaAs(100) and InAs(100) [35]. Therefore, in mild oxidation conditions, the geometric preference toward oxygen atoms seems to be a major cause to form of As oxide which is thermodynamically less stable than the other oxides.

The study of surface reconstruction of InGaAs alloys shows that an asymmetric 3× structure, which is somewhat less As-rich than a *c*(4×4), tends to be stabilized with In concentration [35]. Although the reason for the surface reconstruction is not fully understood yet, the decrease of As coverage on the topmost layer and the change of the surface geometry due to the nature of mobile In at the surface during the air exposure or CVD seem to be a major cause for the suppression of As-oxide formation in $In_{0.53}Ga_{0.47}As$ surface.

As reported that the better interface quality in the GaAs/ALD HfAlO system due to reduction of the Ga and As native oxides formation compared to GaAs/HfO_2 system [36, 37], the $In_{0.53}Ga_{0.47}As$/HfAlO system shows reduced interface native oxide than $In_{0.53}Ga_{0.47}As$/HfO_2 with MOCVD. The improved interface quality for MOCVD HfAlO is observed in a TEM image with a clear transition from the amorphous dielectric to the crystalline semiconductor substrate of $In_{0.53}Ga_{0.47}As$ as shown in Fig. 3.9c, while as nonuniform interfacial layers are observed for HfO_2 and HfAlO on p-GaAs systems (Fig. 3.9a and b).

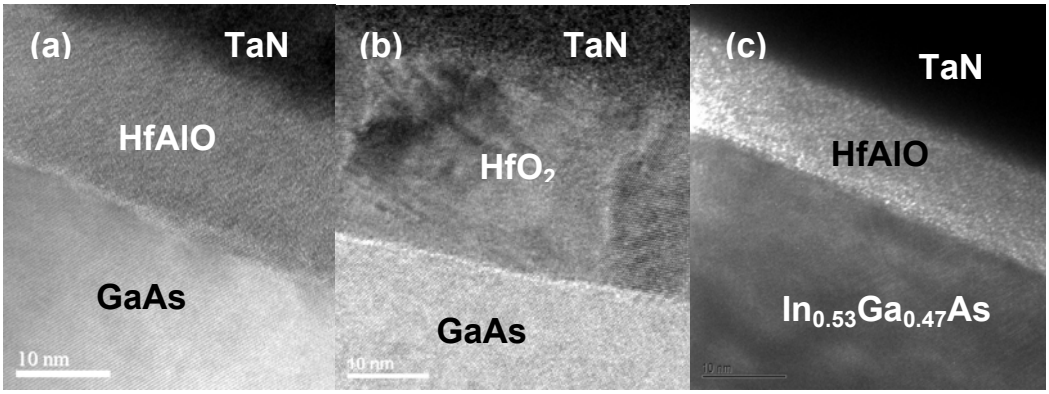


Fig. 3.9 TEM images showing the interfacial structures for the annealed samples at 400 ^{o}C of (a) HfAlO and (b) HfO_2 films on p-GaAs and (c) HfAlO on p-$In_{0.53}Ga_{0.47}As$ substrate.

3.2.2.2 BAND ALIGNMENT OF Hf-BASED HIGH-*k* ON GaAs-BASED III-V

To accomplish a good high-*k* gate stack, the high-*k* must have sufficient band offsets of over 1 eV to act a barrier for both electrons and holes as well as be stable in contact with the semiconductor [38]. The band alignments of MOCVD HfO_2 and HfAlO on p-GaAs and p-$In_{0.53}Ga_{0.47}As$/InP substrate surfaces are studied from the leading edges of the individual valence band XPS measurement [39].

High-*k* dielectric layers (~ 20 nm) were used as bulk high-*k* references. In XPS analysis, the As $3d_{5/2}$ peak and valence band edge from the p-GaAs substrate were chosen as the reference to determine the valence band offset (VBO) between the HfO_2 films and p-GaAs substrate. The core level positions and VBM of bulk materials combined with core level difference of heterojunction are used to calculate the VBO. The VBM is determined by using a linear extrapolation method. Figure 3.10 shows the core level spectra of As 3d of p-GaAs bulk with and without HfO_2 overlayer. The As 3d spectra show As $3d_{5/2}$ and As $3d_{3/2}$ doublets for p-GaAs substrate at 41.2 and 41.8 eV, respectively, indicating the high resolution of the XPS analyzer. Figure 3.10b exhibits the Hf 4f spectra observed from the HfO_2 layer on p-GaAs. It is evident that

the Hf $4f_{7/2}$ peak at 17.0 eV, separated by 1.7 eV from the Hf $4f_{5/2}$ peak at 18.7 eV, attributes to Hf bound to oxygen. The valence band edge of p-GaAs substrate was determined to be 0.37 eV by the linear extrapolation method, as shown in Fig. 3.10c. For thin films of HfO_2 on p-GaAs, the As $3d_{5/2}$ from the substrate is aligned to the same position as that of p-GaAs bulk substrate. The valence band edge of HfO_2 films was determined to be 3.22 eV. Therefore, the VBO between annealed HfO_2 films and p-GaAs was determined to be 2.85 eV, which is in good agreement with the reported calculated value by Robertson et al. (VBO between HfO_2 and GaAs is 3 eV) [38]. The VBO at p-GaAs/as-deposited HfO_2 is 2.81 eV. The VBO at p-GaAs/HfO_2 heterojunctions is lower compared to the calculated value, which may be due to the presence of interfacial layer of Ga and As oxides, as shown in Fig. 3.7 in the previous section.

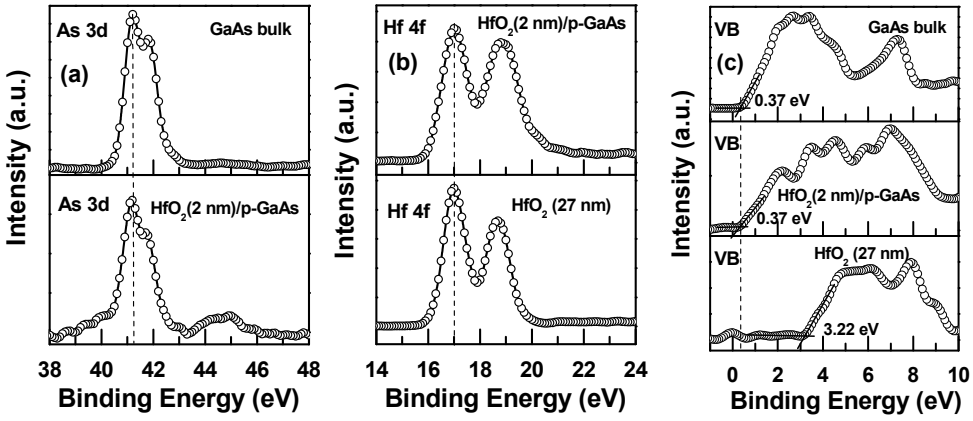


Fig. 3.10 (a) As 3d core level, (b) Hf 4f core level, and (c) valence band spectra of p-GaAs substrate and HfO_2 films deposited on p-GaAs and annealed at 400 ^{o}C in N_2 for 1 min. [37]

Figure 3.11 shows the XPS spectra of valence band for clean p-GaAs substrate and HfAlO films deposited on p-GaAs substrate. The valence band edge of HfAlO on p-GaAs was determined to be 3.35 eV. Therefore, by using the same method employed

above, the valence band offset is determined to be 2.98 eV at p-GaAs/HfAlO interface for annealed and as-deposited HfAlO films. This value of 0.13 eV is larger than that of p-GaAs/HfO_2 interface. The presence of Al_2O_3 in HfO_2 not only improves the interface quality but also increases VBO at HfO_2/p-GaAs interface. The conduction band offset (CBO) at p-GaAs/HfO_2 can be evaluated by subtracting the VBO and the band gap of the substrate (1.45 eV) [38] from the band gap of HfO_2 of 5.6 eV [40]. The band gap of HfAlO varies with Al_2O_3 mole fraction in HfO_2. According to Yu et al. [41], the band gap of HfAlO for 10% Al_2O_3 is 6.4 eV. Therefore, the CBO for p-GaAs/HfO_2, and p-GaAs/HfAlO interfaces are 1.3 and 1.97 eV, respectively. The CBO at p-GaAs/HfO_2 interface is in good agreement with the reported calculated value of 1.4 eV for HfO_2 films on GaAs substrate [38].

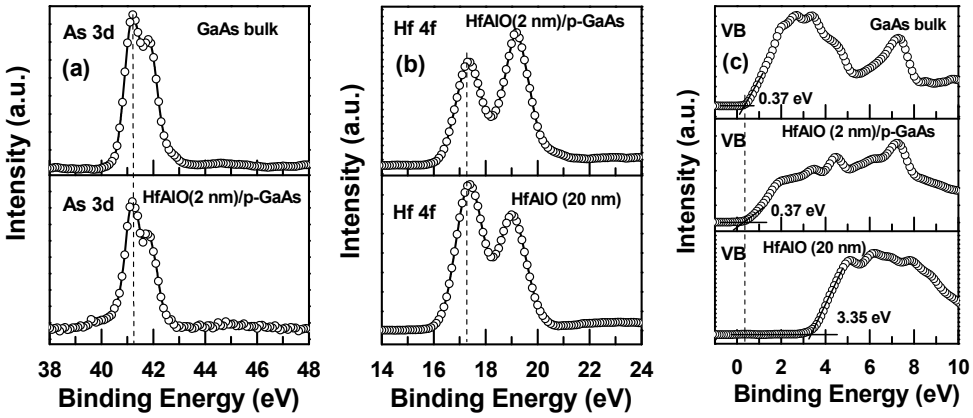


Fig. 3.11 (a) As 3d core level, (b) Hf 4f core level, and (c) valence band spectra of p-GaAs substrate and HfAlO films deposited on p-GaAs and annealed at 400 ^oC in N_2 for 1 min. [37]

The XPS spectra of valence band for clean p-$In_{0.53}Ga_{0.47}As$ substrate and HfO_2 and HfAlO films deposited on p-$In_{0.53}Ga_{0.47}As$ are illustrated in Fig. 3.12. VBO of 2.9 and 3.3 eV have been extracted for p-$In_{0.53}Ga_{0.47}As$/HfO_2 and p-$In_{0.53}Ga_{0.47}As$/HfAlO

interfaces, respectively where the substrate band gap of 0.74 eV is used. The corresponding CBO values have been estimated 1.9 and 2.4 eV sequentially.

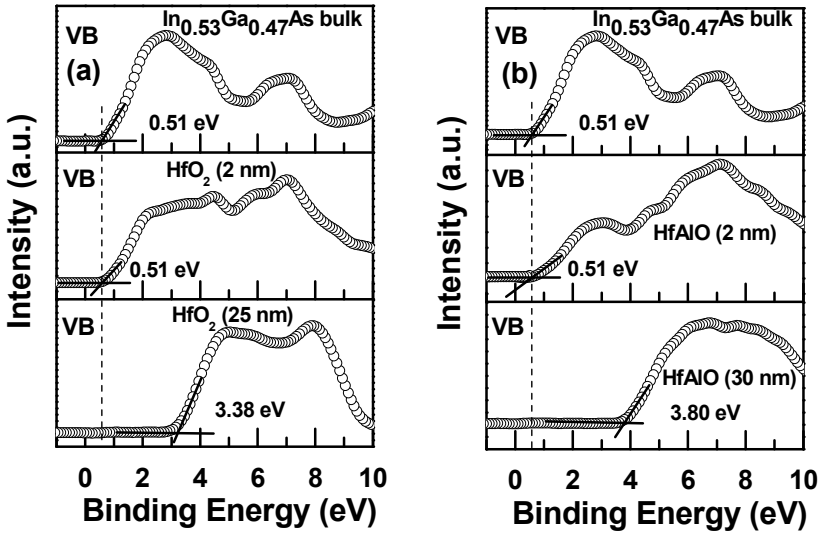


Fig. 3.12 Valence band spectra of (a) HfO_2films and (b) HfAlO films deposited on p-$In_{0.53}Ga_{0.47}As$ and annealed at 400 ^oC for 1 min.

In summary, the energy band structures of GaAs and $In_{0.53}Ga_{0.47}As$/MOCVD HfO_2 and HfAlO heterostructures are depicted in Fig. 3.13.

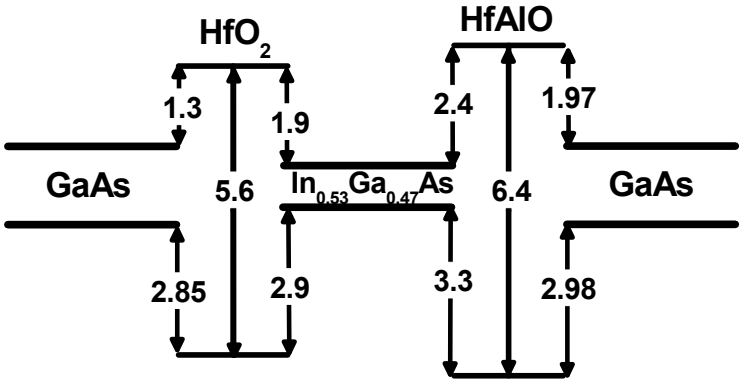


Fig. 3.13 Band alignment diagram for MOCVD HfO_2 and HfAlO on p-$In_{0.53}Ga_{0.47}As$ and p-GaAs estimated by XPS measurement. [42]

The band offsets of the studied Hf-based high-*k* dielectrics on GaAs and $In_{0.53}Ga_{0.47}As$ are adequate for the gate dielectric operation with energy barriers over 1 eV. Huang et al. reported the CBO value of 1.95 eV for p-$In_{0.53}Ga_{0.47}As$/ALD HfO_2 system obtained from the XPS and reflection electron energy loss spectroscopy (REELS) analyses [43]. This is in good agreement with the present experimental data.

3.3 PROCESS OPTIMIZATION BY ELECTRICAL CHARACTERIZATION

This section will present the process optimization by electrical characteristics of GaAs and InGaAs MOS devices, verifying the material characterization results above. Among the gate stack formation processes, the pre-gate dielectric cleaning step is usually too subtle to identify its effect on physical and chemical properties of the interfaces, although the cleaning process is critical to achieve the III-V/high-*k* interface without Fermi level pinning. Based on the concept of removal of native oxide layer and immediate surface passivation to prevent oxidation upon air exposure, the pre-gate dielectric chemical cleaning processes are examined with the effect of each cleaning step on electrical properties of the MOS devices. In addition to the unpinned Fermi level at the III-V/high-*k* interface of MOS structure, the S/D resistance including contact resistance, R_c and sheet resistance, R_{sh} of the n^+ S/D should be low enough to realize the MOSFET devices. Hence, the process parameters in the S/D formation processes, such as Si implantation dose and activation temperature are calibrated and optimized for a self-aligned MOSFET fabrication scheme. The substrate effect on the electrical properties of MOS capacitor is compared as well as on S/D electrical properties.

3.3.1 FABRICATION PROCEDURE OF MOSFET

The fabrication of MOSFETs started with 1% HF or 10% HCl chemical etching to remove native oxides on p-type GaAs (100) substrates (Zn, 1×10^{16} cm^{-3}) and on p-type $In_{0.53}Ga_{0.47}As$/InP substrates. 200 nm p-doped 1×10^{18} cm^{-3} InP buffer and 500 nm p-doped 1×10^{17} cm^{-3} $In_{0.53}Ga_{0.47}As$ were sequentially grown by MBE on a 2-inch p^{+} InP substrate. In order to investigate the impact of substrate material, both of the wafers underwent identical processing steps for MOS device fabrications.

Long channel MOSFET was fabricated using two masks to define the ring-shaped gate and contact patterns. The gate length is 5-20 μm and the width is 200-400 μm in our experiments, with an additional square area of 100×100 μm^{2} for probing. Figure 3.14 shows a microscope image of the long channel MOSFET after fabrication.

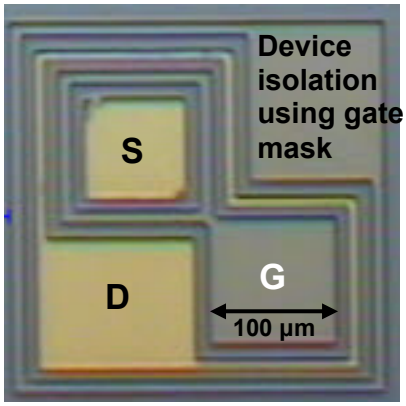


Fig. 3.14 A microscope image of a ring-shaped MOSFET where G, S and D present gate, source and drain regions, respectively.

The self-aligned long channel MOSFET fabrication procedure is listed with the process condition for each main process step in Table 3.1. In order to demonstrate E-mode GaAs NMOSFET, the process conditions for chemical cleaning prior to dielectric deposition, Si S/D implantation, and S/D activation steps have been examined with electrical properties by adding sulfur treatment, varying the amount of Si dose, and RTA at different temperatures, respectively.

Capacitance-voltage (*C-V*), current-voltage (*I-V*) characteristics were measured using a Agilent 4284A LCR meter and a HP 4156A semiconductor parameter analyzer, respectively. Four-point probe method was used to measure R_{sh} of n^+ S/D of the substrates.

Table 3.1 Fabrication process and condition for long channel GaAs NMOSFET

Process	**Condition**
Wet chemical cleaning	10 % HCl or 1 % HF to remove native oxides, 1 min $(NH_4)_2S$ for sulfur passivation, 5 min
MOCVD High-*k* deposition	HfO_2 at 400 ^oC using HTB precursor HfAlO at 450 ^oC using HA-2 source
In situ PDA	400 ^oC, 200 Torr, 1 min in N_2
TaN electrode deposition	Ta, 450W, RF 12W, 3 mTorr, Ar 25 sccm, N_2 5 sccm
Lithography	SNDL Single Tr. Mask
Gate patterning	Cl_2-based dry etching and O_2 plasma PR strip
Capping oxide deposition	SiO_2 10 nm using e-beam evaporator
S/D implantation	Si, 50keV, 1×10^{14} cm^{-2}
Capping oxide deposition	SiO_2 100 nm using e-beam evaporator
S/D RTA activation	600-800 ^oC for 10-60 s in N_2
Contact mask	SNDL Single Tr. Complementary Mask using negative PR
Metal deposition	AuGe 50 nm/Ni 25 nm/Au 50 nm for front contact
PR strip	Acetone/sonic, IPA, DI rinse
Metal deposition	Ti 25/Pd (or Pt) 25/Au 500 nm for back contact
Metal Alloying RTA	360-400 ^oC, 1 min in N_2
FGA	400 ^oC, 10 min in 10% H_2/N_2

3.3.2 S/D CHARACTERISTICS

In a self-aligned scheme, the thermal budget of the fabrication processes affecting the interfacial quality of the gate stack is determined by S/D activation temperature. The S/D activation temperature should be low enough to avoid the detrimental interfacial reaction in the III-V/high-*k*/metal gate stack and high enough to activate S/D n^+ region to flow the current through the inversion channel in the NMOSFET.

Firstly, the impact of S/D activation temperature on electrical properties was investigated with p-GaAs wafers. The dose of Si implantation was also examined in the range from 5×10^{14} to 2×10^{15} cm^{-2} at 5 keV. The dopant activation was carried out with 100 nm thick SiO_2 capping layer deposited on the implanted GaAs sample varying RTA temperature from 600 to 800 ^oC and annealing time for 10 s and 1 min. Four-point probe measurement was employed to measure the R_{sh} after removal of the capping oxide in 1% HF.

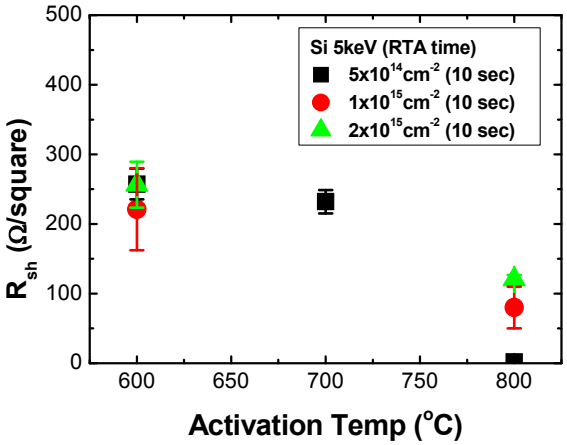


Fig. 3.15 R_{sh} of the p-GaAs samples activated at various RTA temperatures for 10 s after Si implantation at different dose conditions.

Figure 3.15 shows the dose effect on R_{sh} of the GaAs as a function of activation temperature. The error bar indicates the range of the measured data. The R_{sh} reduces

significantly to 5±2 Ω/square at 800 °C activation and at the lowest dose condition of 5×10^{14} cm^{-2} in the experimental range. RTA at 700 °C does not seem to be enough to activate Si dopant in GaAs lattice.

The impact of anneal time on R_{sh} is shown in Fig. 3.16 as a function of RTA temperature at 5×10^{14} cm^{-2} Si dose. It was observed that GaAs surface starts to show droplets due to evaporation from substrate when annealed at 800 °C for 1 min.

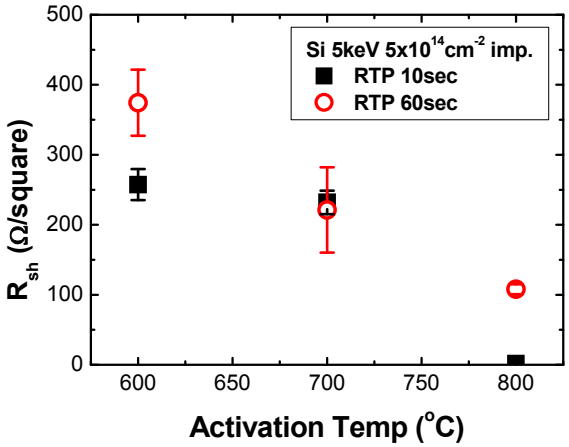


Fig. 3.16 R_{sh} of p-GaAs implanted Si with the dose of 5×10^{14} cm^{-2} as a function of activation RTA temperature. The effect of annealing time is shown.

Since Si is a shallow substitution amphoteric dopant, it acts as a donor when substituted for Ga (Si_{Ga}) and as an acceptor when forming Si_{As}. Therefore the both diffusion and electrical properties of the Si dopant will depend strongly on the population of Ga or As vacancies in GaAs. Si dopant concentration seems to exceed the available Ga vacancies where the dose is larger than 5×10^{14} cm^{-2} at 800 °C RTA wherein the excess Si may cause increase of R_{sh} by acting as impurity defects. Figure 3.16 shows a considerable dependency of R_{sh} on annealing time at 800 °C RTA, indicating that RTA at 800 °C is not a stable activation condition at even low Si implantation dose. It is believed that the high As vapor pressure at high temperature

induces Ga precipitation with decrease of Ga vacancies in the GaAs lattice. We, therefore, set the S/D formation condition to the lower Si dose of 1×10^{14} cm^{-2} and activation at 750 ^{o}C RTA for 1 min to fabricate GaAs MOSFET. This RTA condition is consistent with the report on effect of RTA for GaAs/SiO_2 interface and carrier profile behavior, where Ga out-diffusion is maximized at 750 ^{o}C with thick SiO_2 layer encapsulation [44]. Good rectifying junction characteristic between the n^+ S/D contact and back contact on p-GaAs was confirmed in GaAs MOSFET with the determined S/D formation condition as shown in Fig. 3.17.

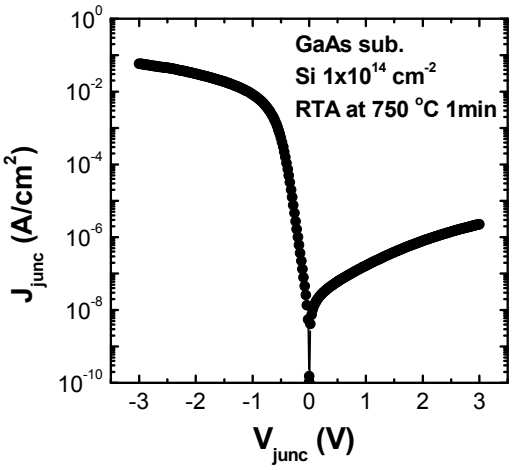


Fig. 3.17 Junction current density, J_{junc} vs the voltage applied between the Si implanted n^+ S/D and the p-GaAs substrate in GaAs NMOSFET.

3.3.3 SURFACE CLEANING EFFECT

The surface cleaning process prior to MOCVD high-*k* deposition has been evaluated in terms of electrical characteristics and device yield per substrate area.

Poor MOS capacitor characteristics were observed when HfO_2 and HfAlO MOS capacitors were fabricated on GaAs with its native oxide, i.e., without chemical cleaning. The gate leakage current was high as shown in Fig. 3.18 and the *C-V* was flat, not showing carrier modulation by the gate bias applied. As seen in sec.3.2.1, the

reduced As oxide in the interface of GaAs/HfAlO compared to GaAs/HfO_2 may be responsible for the reduced gate leakage of the HfAlO gate stack compared to HfO_2.

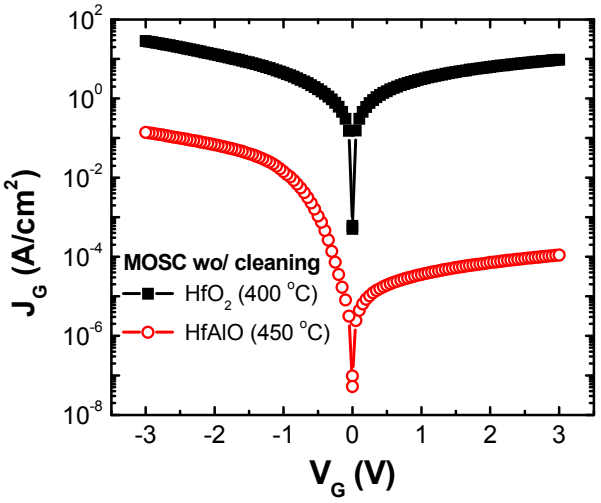


Fig. 3.18 J_G vs V_G plot of p-GaAs MOS capacitors with 8 nm MOCVD high-*k* film deposited at the optimized deposition temperature for each high-*k* without pre-deposition cleaning.

Figure 3.19a indicates that HF cleaning prior to high-*k* deposition dramatically reduces gate leakage of GaAs/HfO_2 gate stack. Similarly, Shin et al. reported the improvement of electrical characteristics of MOS capacitor integrated with ALD Al_2O_3 dielectric on $In_{0.2}Ga_{0.8}As$ by removal of native oxide using wet chemical cleaning [45]. EOT and V_{FB} of the GaAs MOS capacitor with 10 nm HfO_2 deposited at 400 °C have been changed by +0.5 nm and -0.1 V, respectively when sulfur treatment is followed after HF cleaning (Fig. 3.19b). The hysteresis measured from bidirectional *C-V* measurement at 1 kHz was 0.77 V for sulfur treated sample while 0.65 V for the sample cleaned in HF only. However, the number of functional MOS capacitor devices with the low gate leakage current ($<1\times10^{-6}$ A/cm^2) was increased to ~11 times when sulfur treatment is added after HF cleaning. These results indicate that the pre-deposition chemical treatment to remove native oxides and to passivate the surface with sulfur upon air exposure is critical to realize E-mode GaAs MOSFETs.

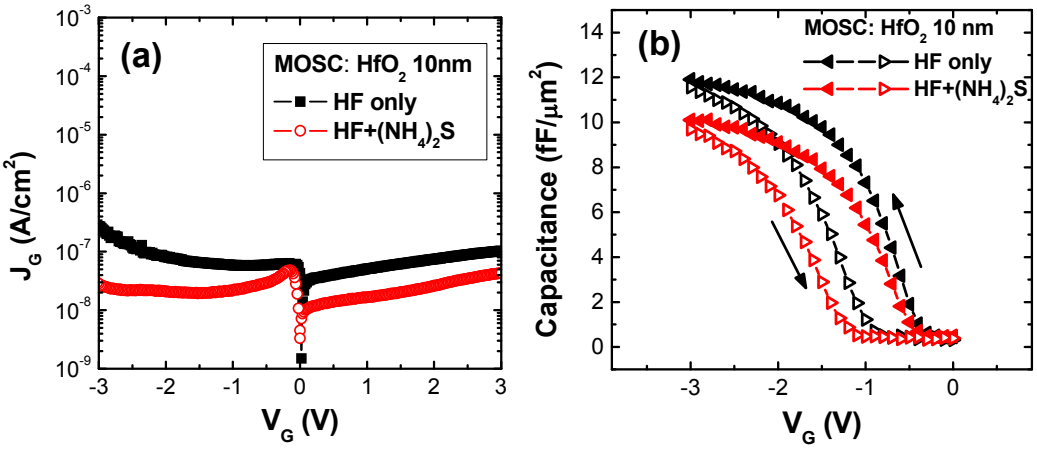


Fig. 3.19 (a) J_G vs V_G plots and (b) bidirectional *C-V* curves measured at 1 kHz for GaAs MOS capacitors with different pre-deposition cleanings before HfO_2 deposition.

3.3.4 III-V SUBSTRATE EFFECT

As InGaAs substrate material is less vulnerable to form native oxides on the surface than GaAs (Fig. 3.7-3.9), InGaAs is expected to realize high mobility NMOSFET easier than GaAs with unpinned Fermi level.

Electrical characteristics of HfAlO MOS capacitors fabricated on the different substrates are shown in Fig. 3.20. The *C-V* for p-$In_{0.53}Ga_{0.47}As$/HfAlO gate stack shows a sharper transition from the depletion region to the accumulation region than that obtained in p-GaAs/HfAlO, indicating the improved interface quality, with an excellent *C-V* curve fitting agreement with a simulated *C-V* (Fig. 3.20a and b).

The midgap D_{it} is estimated to be ~5×10^{11} $cm^{-2}eV$ by the Terman method [46] for p-$In_{0.53}Ga_{0.47}As$/HfAlO capacitor while ~9×10^{12} $cm^{-2}eV$ for p-GaAs/HfAlO. The smaller hysteresis in p-$In_{0.53}Ga_{0.47}As$/HfAlO system comparing to p-GaAs/HfAlO system shows the improved trapping behavior of the dielectric as well (Fig. 3.20c). Also HfAlO MOS capacitor on the p-$In_{0.53}Ga_{0.47}As$ substrate exhibits low leakage current (3.0×10^{-6} A/cm^2 at V_{FB}-1 V) as compared to that on p-GaAs (4.3×10^{-5} A/cm^2 at

V_{FB}-1 V, Fig. 3.20d). In addition to the improvement of the dielectric quality, the higher VBO and CBO of p-$In_{0.53}Ga_{0.47}As$/HfAlO can be another cause of the leakage reduction as shown the band alignments of HfAlO on p-$In_{0.53}Ga_{0.47}As$ and on p-GaAs substrate surfaces in Fig. 3.13.

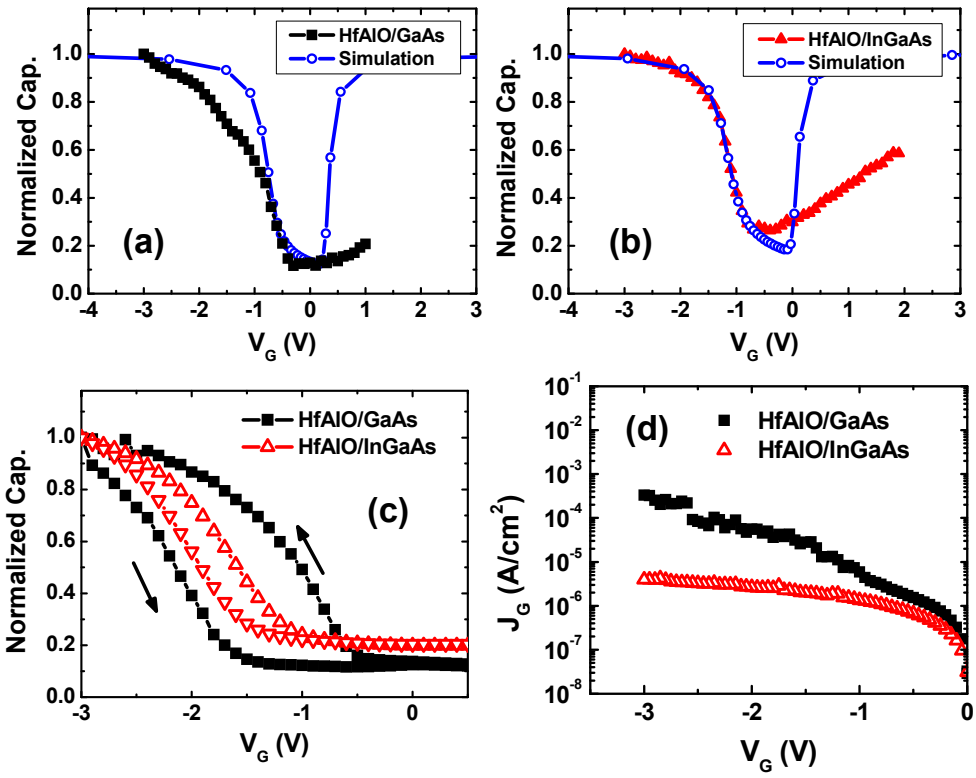


Fig. 3.20 (a) *C-V* characteristics of p-GaAs/HfAlO and (b) p-$In_{0.53}Ga_{0.47}As$/HfAlO MOS capacitors measured at 200 Hz with simulated *C-V* comparisons. (c) The bidirectional *C-V* characteristics of the capacitors measured at 10 kHz. The hysteresis of p-$In_{0.53}Ga_{0.47}As$/HfAlO capacitor at V_{FB} is 34% of it from GaAs/HfAlO capacitor. (d) J_G -V_G characteristics of the MOS capacitors. [42]

Since InGaAs shows better interface quality than GaAs, S/D activation processes were studied then to demonstrate InGaAs MOSFET integrated with high-*k*/metal gate in a self-aligned fabrication scheme. Figure 3.21 shows the n^+ S/D R_{sh} of $In_{0.53}Ga_{0.47}As$/InP substrate material by activation temperature and the junction characteristic of n^+/P junction by the voltage applied on S/D contact. In contrast to

GaAs substrate material, the activation of dopant can be achieved from ~600 ^{o}C RTA. Smooth surfaces were observed in the experiment range. Compared to the case of GaAs MOSFET, the lower thermal budget for S/D activation can benefit the interface quality by preventing its degradation during the high temperature process in a gate-first MOSFET fabrication scheme. A good rectifying junction characteristic was achieved by 600 ^{o}C RTA for n^{+} S/D activation on p-$In_{0.53}Ga_{0.47}As$/InP substrate (Fig. 3.21b).

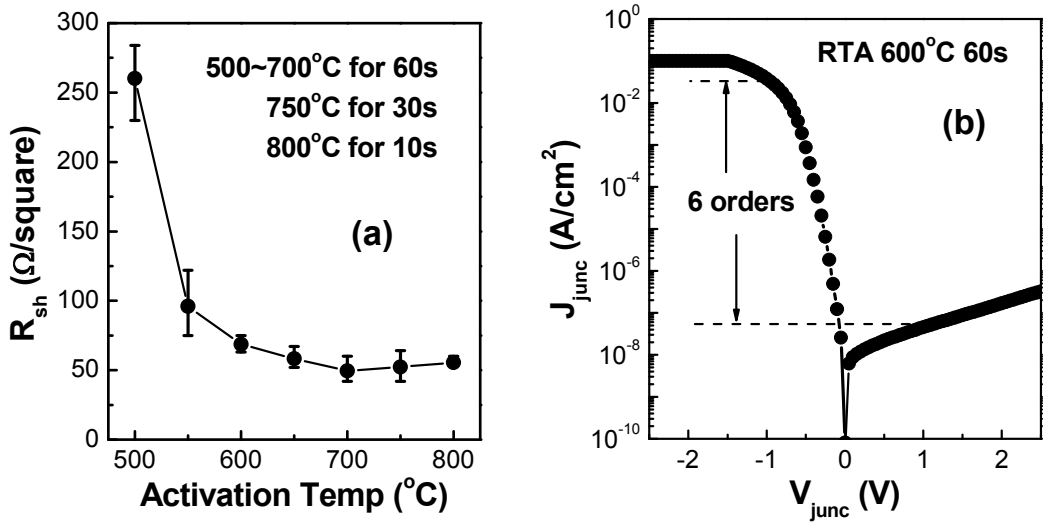


Fig. 3.21 (a) Sheet resistance of Si implanted n^{+} S/D with a dose of 1×10^{14} cm^{-2} at 50 keV on $In_{0.53}Ga_{0.47}As$/InP substrate by activation RTA temperature (b) Junction current density versus the voltage applied between the Si implanted n^{+} S/D contact and the p-substrate back contact in the InGaAs MOSFET. [47]

3.4 HIGH MOBILITY III-V NMOSFET INTEGRATED WITH HIGH-*k*/METAL GATE IN A SELF-ALIGNED SCHEME

Eventually, in this section, the demonstration of E-mode $In_{0.53}Ga_{0.47}As$ NMOSFET with HfAlO/TaN gate stack will be presented. We used the gate-first self-aligned process, direct deposition of MOCVD HfAlO on $In_{0.53}Ga_{0.47}As$ with sulfur

treatment prior to the dielectric film deposition. S/D activation was carried out at 600 ^{o}C using RTA. The electrical characteristics of the fabricated device were examined.

3.4.1 GATE STACK

InGaAs/HfAlO/TaN gate stack integrity is summarized in Fig. 3.22 as a result from the fabrication process optimization by material and electrical characterizations.

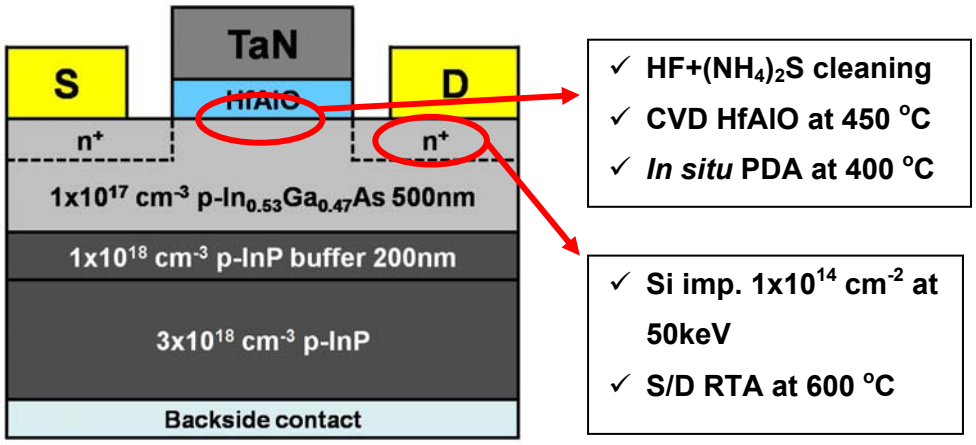


Fig. 3.22 Schematic cross section of the self-aligned $In_{0.53}Ga_{0.47}As$ NMOSFET integrated with a CVD HfAlO gate dielectric and a TaN metal gate. Key process conditions developed for the E-mode NMOSFET fabrication are listed in sequence.

3.4.2 PERFORMANCE OF MOSFET

Figure 3.23a shows that well-performed inversion capacitance is achieved, indicating that the conventional Fermi level pinning phenomenon on III-V is overcome in this $In_{0.53}Ga_{0.47}As$/HfAlO interface. J_G-V_G curve with grounding S/D and substrate is shown in Fig. 3.23b. At $V_G = \pm 2$ V, J_G is below 10^{-6} A/cm^2. This is comparable to the lowest reported gate leakage of CVD HfO_2 on GaAs with advanced surface treatment [48]. EOT of 4.15 nm is recorded. D_{it} value is determined to be 3×10^{12} cm^{-2}eV^{-1}.

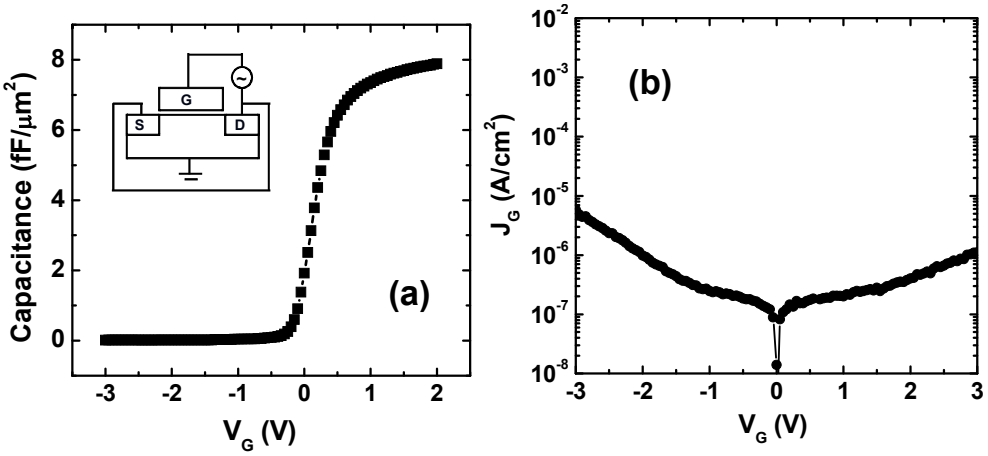


Fig. 3.23 (a) Inversion *C-V* measured at 100 kHz. Measurement configuration is inset into the *C-V* plot. (b) J_G-V_G with backside grounded.

Figure 3.24a shows the subthreshold performance of the fabricated $In_{0.53}Ga_{0.47}As$ NMOSFET with gate length of 4 μm, at drain biases of 0.05 and 1 V, respectively. The DIBL is 68.1 mV/V for this device. Considering the bandgap of $In_{0.53}Ga_{0.47}As$ is 0.74 eV, it is predicted that the source to drain leakage contributes a significant I_{off} due to the thermal generation of minority carriers [49] and BTBT. The I_{on} over the I_{off} at V_G = -1 V is over 4 orders for this device, comparable to that of the $In_{0.53}Ga_{0.47}As$/ALD high-*k* NMOSFET device reported [31]. SS of 196 mV/dec is obtained. The threshold voltage in this device is close to zero which causes an I_{off} at V_G = 0 V relatively high for enhancement operation. Metal work function tuning and SS engineering can achieve lower I_{off} at zero gate voltage. Figure 3.24b shows the linear scale I_D-V_G of the 4 μm gate length $In_{0.53}Ga_{0.47}As$ NMOSFET at V_D = 0.05 and 1 V as well as their G_m. Maximum G_m values are 3.3 and 34 mS/mm for V_D = 0.05 and 1 V, respectively.

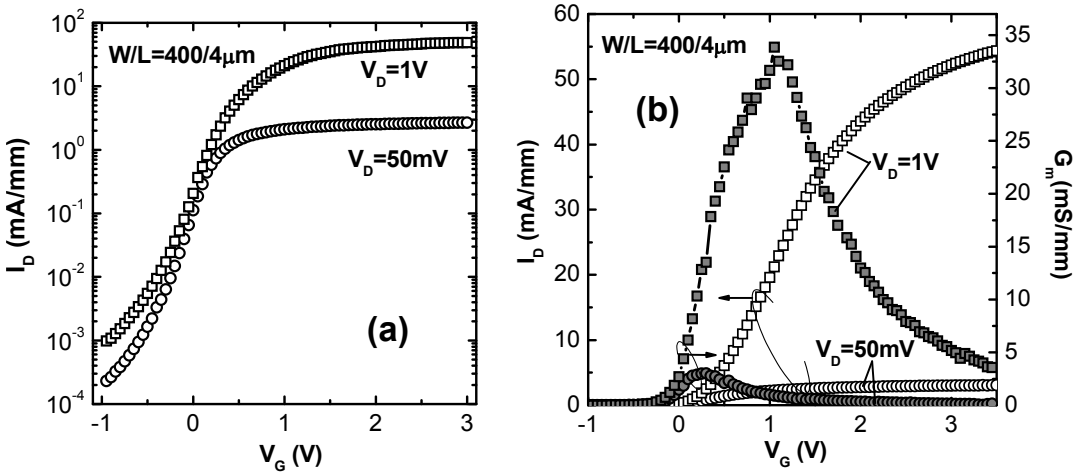


Fig. 3.24 (a) Log scale I_D-V_G at V_D = 50 mV and 1V showing subthreshold behavior of an $In_{0.53}Ga_{0.47}As$ NMOSFET with a gate length of 4 μm. (b) The linear scale I_D-V_G and transconductances as a function of the gate bias at V_D = 50 mV and 1V.

Figure 3.25 shows the I_D-V_D curve for the 4 μm gate length $In_{0.53}Ga_{0.47}As$ NMOSFET measured with V_G from 0 to 3 V in 0.5 V step in a bidirectional V_D sweeping. Negligible hysteresis appears for a wide range of biased voltages, indicating low bulk oxide trapped charges and low interface trap density in the $In_{0.53}Ga_{0.47}As$/HfAlO interface. Well-behaved I_D-V_D characteristics indicate an E-mode operation.

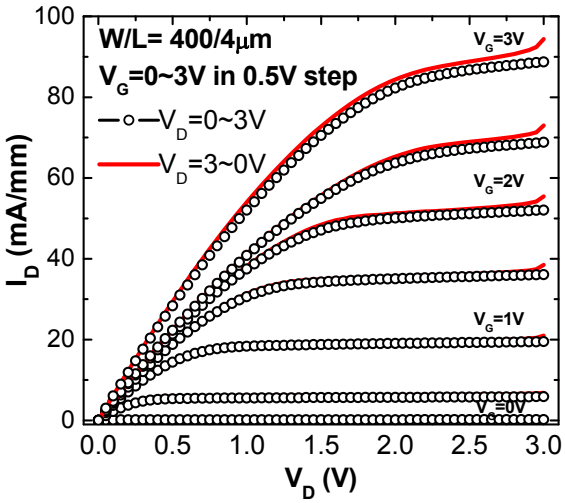


Fig. 3.25 I_D–V_D of an $In_{0.53}Ga_{0.47}As$ NMOSFET of 4 μm gate length in a bidirectional V_D sweeping for the hysteresis study.

As a result, Fig. 3.26 shows the electron mobility vs V_G for a 4 μm gate length $In_{0.53}Ga_{0.47}As$ NMOSFET, measured by the split *C-V* method without corrections. The peak mobility at low gate bias, i.e. low field, is 1560 cm^2/Vs. The present InGaAs NMOSFET has exhibited high low field electron mobility comparing to strained-Si NMOSFETs, where the peak mobility is ~800 cm^2/Vs [50]. Compared to the E-mode $In_{0.53}Ga_{0.47}As$/ALD high-*k* NMOSFETs [31], our device shows the higher mobility without correction and the smaller SS. This may contribute to the better $In_{0.53}Ga_{0.47}As$/MOCVD HfAlO interface than the $In_{0.53}Ga_{0.47}As$/ALD high-*k* interfaces. It can be noted that the reported mobilities in E-mode NMOSFETs, including the present result, are generally lower [31, 51] comparing with the bulk electron mobility as well as the Hall mobility of the flatband-mode MOSFETs of GaAs and InGaAs [49]. This may be probably due to the impurity scattering from a high channel doping and interface traps, indicating further works still need to improve the InGaAs/high-*k* interface quality.

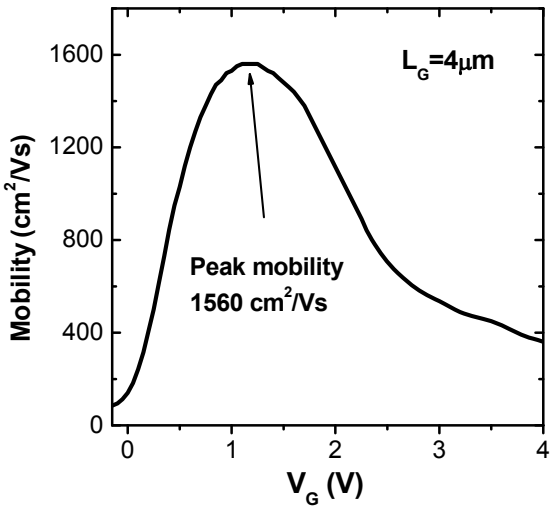


Fig. 3.26 Electron mobility vs V_G extracted from a split *C-V* method without correction for an $In_{0.53}Ga_{0.47}As$ NMOSFET of 4 μm gate length.

3.5 CONCLUSION

Based on the study of interfacial properties and the process optimizations using electrical properties, we successfully demonstrated the E-mode $In_{0.53}Ga_{0.47}As$ NMOSFET integrated with CVD HfAlO gate dielectric and TaN metal gate in a self-aligned fabrication scheme.

To find the high-*k* deposition condition where the interfacial native oxide is suppressed or converted into thermally stable species, the HfO_2 and HfAlO MOCVDs were examined with GaAs wafer at different deposition temperatures using XPS. It is found that the amount of interfacial As oxide on GaAs surface depends on the high-*k* deposition temperature, where the As oxide is reduced by increasing the deposition temperature. The improved interfaces with suppressed As oxide were observed at 400 ^oC for HfO_2 and at 450 ^oC for HfAlO CVD, respectively. The XPS analysis revealed that HfAlO CVD using HA-2 precursor has the self-cleaning effect on the removal of interfacial oxide of GaAs during the film deposition, for the first time.

It has been demonstrated that the alloying of InAs with GaAs ($In_{0.53}Ga_{0.47}As$) and the alloying of HfO_2 with Al_2O_3 (HfAlO) can significantly reduce native oxides formation at p-GaAs/HfO_2 interface using XPS. The band offsets for the GaAs-based III-V/Hf-based high-*k* systems were obtained by XPS also, showing that the electron barrier heights are over 1 eV for all the cases and higher for HfAlO dielectric than HfO_2 and higher for $In_{0.53}Ga_{0.47}As$ substrate then GaAs.

To realize GaAs-based III-V NMOSFET, the Si implanted n^+ S/D formation process conditions were primarily explored and optimized using electrical properties with the substrate effect. It was revealed that $In_{0.53}Ga_{0.47}As$ can accommodate lower thermal budget for MOSFET integration with enabling S/D activation at 600 ^oC while GaAs needs the activation at near 800 ^oC. In addition, the electrical characteristics of

MOS devices show that the HF chemical cleaning before HfO_2 deposition enhances the GaAs/HfO_2 interface quality, presenting much reduced gate leakage currents compared to the gate stack without the native oxide removal. Significant improvement in yield of functional MOS devices on GaAs was found when the sulfur treatment is adopted after the HF cleaning and before the high-*k* deposition.

The electrical characteristics of MOS capacitors with the combination of the chemical treatment (HF+$(NH_4)_2S$) and HfO_2 and HfAlO dielectric deposition at the optimized temperatures on GaAs and $In_{0.53}Ga_{0.47}As$ further substantiate the material characteristics analyzed.

Consequently, the $In_{0.53}Ga_{0.47}As$ NMOSFET integrated with HfAlO/TaN gate stack in a self-aligned fabrication scheme exhibited well behaved I_D-V_D and I_D-V_G curves with a sharp transition in inversion *C*-*V* characteristics, indicating unpinned Fermi level on the InGaAs/HfAlO interface. Peak electron mobility at low gate bias of 1560 cm^2/Vs, which is ~2 times higher than the mobility measured in the strained-Si channel NMOSFET, was demonstrated.

References

[1] D. L. Winn, M. J. Hale, T. J. Grassman, A. C. Kummel, R. Droopad, and M. Passlack, "Direct and indirect causes of Fermi level pinning at the SiO/GaAs interface," *J. Chem. Phys*., vol. 126, p. 084703, 2007.

[2] P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, S. N. G. Chu, S. Nakahara, H.-J. L. Gossmann, J. P. Mannaerts, M. Hong, K. K. Ng, and J. Bude, "GaAs metal–oxide–semiconductor field-effect transistor with nanometer-thin dielectric grown by atomic layer deposition," *Appl. Phys. Lett*. vol.83, pp.180-182, 2003.

[3] G. K. Dalapati, A. Sridhara, A. S. W. Wong, C. K. Chia, S. J. Lee, and D. Z. Chi, "Interfacial characteristics and band alignments for ZrO_2 gate dielectric on Si passivated p-GaAs substrate," *Appl. Phys. Lett*., vol. 91, p.242101, 2007

[4] M. M. Frank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabel, J. Grazul, and D. A. Muller, "HfO_2 and Al_2O_3 gate dielectrics on GaAs grown by atomic layer deposition," *Appl. Phys. Lett*., vol.86, p.152904, 2005.

[5] F. Ren, M. Hong, W. S. Hobson, J. M. Kuo, J. R. Lothian, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, "Demonstration of enhancement-mode p- and n-channel GaAs MOSFETs with $Ga_2O_3(Gd_2O_3)$ as gate oxide", *Solid State Electron*., vol. 41, pp. 1751-1753, 1997.

[6] Y. Xuan, H. C. Lin, P. D. Ye, and G. D. Wilk, "Capacitance-voltage studies on enhancement-mode InGaAs metal-oxide-semiconductor field-effect transistor using atomic-layer-deposited Al_2O_3 gate dielectric," *Appl. Phys. Lett*., vol. 88, pp. 263518, 2006.

[7] C. W. Wilmsen Ed., *Physics and Chemistry of III-V Compound Semiconductor Interfaces*, New York: Plenum, 1985.

[8] K. Eguchi and T. Katoda, "Characterization of precipitates in anodic oxidized $Ga_{1-x}Al_xAs$ and $Ga_{1-x}In_xAs$ by laser Raman spectroscopy," *Jpn. J. Appl. Phys*., vol. 24, pp. 1043-1048, 1985.

[9] C. D. Thurmond, G. P. Schwartz, G. W. Kammlott, and B. Schwartz, "GaAs oxidation and the Ga-As-O equilibrium phase diagram," *J. Electrochem. Soc.*, vol. 127, pp. 1366-1371, 1980.

[10] G. Hollinger, R. Skheyta-Kabbani, and M. Gendry, "Oxides on GaAs and InAs surfaces: An X-ray-photoelectron-spectroscopy study of reference compunds and thin oxide layers," *Phys. Rev.B*, vol. 49, pp. 11159-11167, 1994.

[11] S. I. Yi, P. Kruse, M. Hale, and A. C. Kummel, "Adsorption of atomic oxygen on GaAs (001)-(2×4) and the resulting surface structures", *J. Chem. Phys*., vol. 114, pp. 3215-3223, 2001.

[12] E. R. Weber, H. Ennen, U. Kaufmann, J. Windscheif, J. Schneider, and T. Wosinski, "Identification of As_{Ga} antisites in plastically deformed GaAs", *J. Appl. Phys*., vol. 53, pp. 6140-6143, 1982.

[13] F. Ren, J. M. Kuo, M. Hong, W. S. Hobson, J. R. Lothian, J. Lin, W. S. Tseng, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, "$Ga_2O_3(Gd_2O_3)$/InGaAs enhancement-mode n-channel MOSFETs," *IEEE Electron Device Lett*., vol. 19, pp. 309-311, 1998.

[14] M. Hong, Z. H. Lu, J. Kwo, A. R. Kortan, J. P. Mannaerts, J. J. Krajewski, K. C. Hsieh, L. J. Chou, and K. Y. Cheng, "Initial growth of $Ga_2O_3(Gd_2O_3)$ on GaAs: Key to the attainment of a low interfacial density of states," *Appl. Phys. Lett*., vol. 76, pp. 312-314, 2000.

[15] J. F. Zheng, W. Tsai, T. D. Lin, Y. J. Lee, C. P. Chen, M. Hong, J. Kwo, S. Cui, and T. P. Ma, "$Ga_2O_3(Gd_2O_3)/Si_3N_4$ dual-layer gate dielectric for InGaAs enhancement

mode metal-oxide-semiconductor field-effect transistor with channel inversion," *Appl. Phys. Lett*., vol. 91, p. 223502, 2007.

[16] M. Houssa, E. Chagarov, and A. Kummel, "Surface defects and passivation of Ge and III-V interfaces," *MRS Bull*., vol. 34, pp. 504-513, 2009.

[17] W. E. Spicer, Z. Liliental-Weber, E. Weber, N. Newman, T. Kendelewicz, R. Cao, C. McCants, P. Mahowald, K. Miyano, and I. Lindau, "The advanced unified defect model for Schottky barrier formation," *J. Vac. Sci. Technol*. *B*, vol. 6, pp. 1245-1251, 1988.

[18] P. D. Ye, "Main determinants for III-V metal-oxide-semiconductor field-effect-transistors," *J. Vac. Sci. Technol*. *A*, vol. 26, pp. 697-704, 2008.

[19] J. Robertson, "Model of interface states at III-V oxide interfaces," *Appl. Phys. Lett*., vol. 94, p. 152104, 2009.

[20] M. L. Huang, Y. C. Chang, C. H. Chang, Y. J. Lee, P. Chang, J. Kwo, T. B. Wu, and M. Hong, "Surface passivation of III-V compound semiconductors using atomic-layer-deposition-grown Al_2O_3," *Appl. Phys. Lett*., vol. 87, p. 252104, 2005.

[21] C. L. Hinkle, A. M. Sonnet, E. M. Vogel, S. McDonnell, G. J. Hughes, M. Milojevic, B. Lee, F. S. Aguirre-Tostado, K. J. Choi, H. C. Kim, J. Kim, and R. M. Wallace, "GaAs interfacial self-cleaning by atomic layer deposition," *Appl. Phys. Lett*., vol. 92, p. 071901, 2008.

[22] H. D. Lee, T. Feng, L. Yu, D. Mastrogiovanni, A. Wan, T. Gustafsson, and E. Garfunkel, "Reduction of native oxides on GaAs during atomic layer growth of Al_2O_3," *Appl. Phys. Lett*., vol. 94, p. 222108, 2009.

[23] H. L. Lu, X. L. Wang, M. Sugiyama, and Y. Shimogaki, "Investigation on GaAs surface treated with dimethylaluminumhydride," *Appl. Phys. Lett*., vol. 95, p. 212102, 2009.

[24] C.-H. Chang, Y.-K. Chiou, Y.-C. Chang, K.-Y. Lee, T.-D. Lin, T.-B. Wu, M. Hong, and J. Kwo, "Interfacial self-cleaning in atomic layer deposition of HfO_2 gate dielectric on $In_{0.15}Ga_{0.85}As$," *Appl. Phys. Lett*., vol. 89, p. 242911, 2006.

[25] S. Sayan, S. Aravamudhan, B. W. Busch, W. H. Schulte, F. Cosandey, G. D. Wilk, T. Gustafsson, and E. Garfunkel, "Chemical vapor deposition of HfO_2 films on Si (100)," *J. Vac. Sci. Technol. A*, vol. 20, pp. 507-512, 2002.

[26] J. K. Yang, M. G. Kang, and H. H. Park, "Characteristics of interfacial bonding distribution of Gd_2O_3–GaAs structure," *Vacuum*, vol. 67, pp. 161-167, 2002.

[27] C. Y. Kim, S. W. Cho, M. H. Cho, K. B. Chung, C. H. An, H. Kim, H. J. Lee, and D. H. Ko, "Interfacial reaction of atomic-layer-deposited HfO_2 film as a function of the surface state of an n-GaAs (100) substrate," *Appl. Phys. Lett*., vol. 93, p. 192902, 2008.

[28] T. T. Chiang and W. E. Spicer, "Arsenic on GaAs: Fermi-level pinning and thermal desorption studies," *J. Vac. Sci. Technol*. A, vol. 7, pp. 724-730, 1989.

[29] M. S. Joo, B. J. Cho, C. C. Yeo, D. S. H. Chan, S. J. Whoang, S. Mathew, L. K. Bera, N. Balasubramanian, and D. L. Kwong, "Formation of hafnium–aluminum–oxide gate dielectric using single cocktail liquid source in MOCVD process," *IEEE Trans. Electron Devices*, vol. 50, pp. 2088-2094, 2003.

[30] S. Koveshnikov, N. Goel, P. Majhi, H. Wen, M. B. Santos, S. Oktyabrsky, V. Tokranov, R. Kambhampati, R. Moore, F. Zhu, J. Lee, and W. Tsai, "$In_{0.53}Ga_{0.47}As$ based metal oxide semiconductor capacitors with atomic layer deposition ZrO_2 gate oxide demonstrating low gate leakage current and equivalent oxide thickness less than 1 nm," *Appl. Phys. Lett*., vol. 92, p. 222904, 2008.

[31] Y. Xuan, Y. Q. Wu, T. Shen, T. Yang, and P. D. Ye, "High performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al_2O_3, HfO_2 and HfAlO as gate dielectrics," in *IEDM Tech. Dig*., Dec. 2007, pp. 637-640.

[32] H. H. Wieder, J. L. Veteran, A. R. Clawson, and D. P. Mullin, "Accumulation mode $Ga_{0.47}In_{0.53}As$ insulated gate field-effect transistors," *Appl. Phys. Lett*., vol. 43, pp. 287-289, 1983.

[33] Y. C. Chang, M. L. Huang, K. Y. Lee, Y. J. Lee, T. D. Lin, M. Hong, J. Kwo, T. S. Lay, C. C. Liao, and K. Y. Cheng, "Atomic-layer-deposited HfO_2 on $In_{0.53}Ga_{0.47}As$: Passivation and energy-band parameters," *Appl. Phys. Lett*., vol. 92, p.72901, 2008.

[34] C. C. Cheng, C. H. Chien, G. L. Luo, C. K. Tseng, H. C. Chiang, C. H. Yang, and C. Y. Chang, "Improved electrical properties of Gd_2O_3/GaAs capacitor with modified wet-chemical clean and sulfidization procedures," *J. Electrochem. Soc*., vol. 155, pp.G56-G60, 2008.

[35] P. A. Bone, J. M. Ripalda, G. R. Bell, and T. S. Jones, "Surface reconstructions of InGaAs alloys," *Surf. Sci*., vol. 600, pp. 973-982, 2006.

[36] G. K. Dalapati, Y. Tong, W.-Y. Loh, H. K. Mun, and B. J. Cho, "Electrical and interfacial characterization of atomic layer deposited high-κ gate dielectrics on GaAs for advanced CMOS devices," *IEEE Trans. Electron Devices*, vol. 54, pp. 1831-1837, 2007.

[37] G. K. Dalapati, H. J. Oh, S. J. Lee, A. Sridhara, A. S. W. Wang, and D. Chi, "Energy-band alignments of HfO_2 on p-GaAs substrates," *Appl. Phys. Lett*., vol. 92, p.42120, 2008.

[38] J. Robertson and B. Falabretti, "Band offsets of high-*k* gate oxides on III-V semiconductors," *J. Appl. Phys*., vol. 100, p. 14111, 2006.

[39] E. A. Kraut, R. W. Grant, J. R. Waldrop, and S. P. Kowalczyk, "Precise determination of the valence-band edge in X-ray photoemission spectra: Application to measurement semiconductor interface potentials," *Phys. Rev. Lett.*, vol. 44, pp. 1620-1623, 1980.

[40] V. V. Afanas'ev and A. Stesmans, "Internal photoemission at interfaces of high-*k* insulators with semiconductors and metals," *J. Appl. Phys*., vol. 102, p. 81301, 2007.

[41] H. Y. Yu, M. F. Li, B. J. Cho, C. C. Yeo, M. S. Joo, D. L. Knowg, J. S. Pan, C. H. Ang, J. Z. Zheng, and S. Ramanathan, "Energy gap and band alignment for $(HfO_2)_x(Al_2O_3)_{1-x}$ on (100) Si," *Appl. Phys. Lett*., vol. 81, pp. 376-378, 2002.

[42] H. J. Oh, J. Q. Lin, S. J. Lee, G. K. Dalapati, A. Sridhara, D. Z. Chi, S. J. Chua, G. Q. Lo, and D. L. Kwong, "Study on interfacial properties of InGaAs and GaAs integrated with chemical-vapor-deposited high-k gate dielectrics using x-ray photoelectron spectroscopy," *Appl. Phys. Lett*., vol. 93, p. 62107, 2008.

[43] M. L. Huang, Y. C. Chang, Y. H. Chang, T. D. Lin, J. Kwo, and M. Hong, "Energy-band parameters of atomic layer deposited Al_2O_3 and HfO_2 on $In_xGa_{1-x}As$," *Appl. Phys. Lett*., vol. 94, p. 52106, 2009.

[44] M. Katayama, Y. Tokuda, Y. lnoue, A. Usami and T. Wada, "Ga out-diffusion in rapid-thermal-processed GaAs with SiO_2 encapsulants," *J. Appl. Phys*, vol. 69, pp. 3541-3546, 1991.

[45] B. H. Shin, D. H. Choi, James S. Harris, and P. C. McIntyre, "Pre-atomic layer deposition surface cleaning and chemical passivation of (100) $In_{0.2}Ga_{0.8}As$ and deposition of ultrathin Al_2O_3 gate insulators," *Appl. Phys. Lett*., vol. 93, p. 52911, 2008.

[46] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*, New York: Wiley, 1982.

[47] J. Q. Lin, S. J. Lee, H. J. Oh, G. Q. Lo, D. L. Kwong, and D. Z. Chi, "Inversion-mode self-aligned $In_{0.53}Ga_{0.47}As$ n-channel metal-oxide-semiconductor field-effect transistor with HfAlO gate dielectric and TaN metal gate," *IEEE Electron Device Lett*., vol. 29, pp. 977-980, 2008.

[48] F. Gao, S. J. Lee, D. Z. Chi, S. Balakumar, and D.-L. Kwong, "GaAs metal-oxide-semiconductor device with HfO_2/TaN gate stack and thermal nitridation surface passivation," *Appl. Phys. Lett*., vol. 90, p. 252904, 2007.

[49] M. Passlack, "OFF-state current limits of narrow bandgap MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, pp. 2773-2778, 2006.

[50] P. R. Chidambaram, C. Bowen, S. Chakravarthi, C. Machala, and R. Wise, "Fundamentals of silicon material properties for successful exploitation of strain engineering in modern CMOS manufacturing," *IEEE Trans. Electron Devices*, vol. 53, pp. 944-964, 2006.

[51] I. Ok, H. Kim,M. Zhang, T. Lee, F. Zhu, L. Yu, S. Koveshnikov,W. Tsai1, V. Tokranov, M. Yakimov, S. Oktyabrsky, and J. C. Lee, "Self-aligned n- and p-channel GaAs MOSFETs on undoped and p-type substrates using HfO_2 and silicon interface passivation layer," in *IEDM Tech. Dig*., Dec. 2006, pp. 829-832.

CHAPTER 4

NOVEL SURFACE PASSIVATION FOR FUTURE HIGH SPEED CMOS DEVICE APPLICATION

4.1 INTRODUCTION

Although the successful demonstration of $In_{0.53}Ga_{0.47}As$ E-mode MOSFET with high mobility was achieved as presented in the previous chapter, still the MOSFET device characteristics are poorer than expected. Especially the SS of ~200 mV/dec obtained suggests the needs in improving the interface quality.

In this chapter, a novel passivation for $In_{0.53}Ga_{0.47}As$ substrate using PH_3-based treatment technique will be discussed and analyzed by material and electrical properties of the $In_{0.53}Ga_{0.47}As$/high-*k* interface. The excellent interface quality of the passivated $In_{0.53}Ga_{0.47}As$ NMOSFET devices integrated with high-*k*/TaN gate stacks is demonstrated where P_xN_y is deposited on the InGaAs surface during the PH_3-based plasma-assisted treatment. Chemical and electrical properties of the P_xN_y passivated InGaAs/high-*k* interface are explored with the effect of passivation process conditions to understand the interface reaction.

4.1.1 SURFACE PASSIVATION FOR InGaAs/HIGH-*k* INTERFACE

The recent successful demonstrations of E-mode III-V MOSFETs using advanced Si-based process techniques, including ours presented in the previous chapter, and *in-situ* MBE [1-4] have shed light on the future of emerging III-V

nanoelectronics on Si platform. However, the most difficult challenge to overcome is still on how to control the interface qualities of III-V material systems in nanometer scale devices such that detrimental effects due to high-density surface states and related Fermi level pinning can be avoided. The common features which include SS over 150 mV/dec and limited thermal budget found in the fabrication processes of successful E-mode III-V MOSFETs [1-5] may indicate this surface state control issue on III-V surfaces. Moreover, as surface-to-volume ratio is much increased in nanometer scale devices, this surface state problem becomes more serious. Another most important feature of the future III-V MOS devices is a high-*k* dielectric/metal gate stack. Thus, the success of future III-V nanoelectronics strongly depends on the availability of a suitable and robust III-V surface passivation, which can control surface states and related Fermi level pinning, prior to high-*k* deposition [1, 6].

Based on the active researches on the III-V/high-*k* MOS systems for E-mode MOSFET applications [5] at this stage of the development, the most promising candidate for the III-V channel material for the future NMOS devices is InGaAs with high In composition. Recent theoretical and experimental works show that the electrical performance of the InGaAs MOS devices relies on the gate stack integration processes [5], indicating the defects can be controlled by improvement of those processes [7]. Especially, the InGaAs surface passivation process prior to high-*k* dielectric film deposition is a key step to achieve a good electrical performance. In order to maintain atomically abrupt interface between high-*k* and InGaAs substrate after the whole fabrication processing, a chemical stability should be provided by the passivation as well as a thermodynamic stability. Poor electrical properties can be caused by the uncontrolled InGaAs native oxide formation, metallic bond formation like Hf-Ga in the case of GaAs/HfO_2 high-*k* dielectric gate stack, and diffusion of

substrate constituent elements into the high-*k* film [8], or vice versa, during the integration processes, as observed in the studies of Ge MOSFETs [9-10]. Therefore the interface engineering of InGaAs/high-*k* system to passivate the defects, which can lead to interface traps, should be carried out in consideration of entire integration process.

The requirements for the InGaAs surface passivation to be a viable solution for the deeply scaled high-speed MOSFET applications can be listed as follows:

(1) To be thermodynamically stable to stand high-temperature processes applied after the gate stack formation.

(2) To be chemically stable not to react forming problematic spices such as As oxide and metallic compound, with high-*k* above and InGaAs below.

(3) To inhibit atomic interdiffusion between high-*k* and InGaAs

(4) Not to form low-*k* interfacial layer that hinders scalability of EOT.

(5) To exist in amorphous phase through the device processing or not to produce crystalline defects.

(6) To be compatible with Si-based MOSFET technologies in terms of process techniques and device architectures.

The passivation layer formed on InGaAs surface before high-*k* deposition can be sacrificed by evaporation or converted into its derivative compound which is thermodynamically more stable during the fabrication process with the satisfaction of these requirements.

4.1.2 OVERVIEW OF PASSIVATION TECHNIQUES

Passivating interfacial defects at III-V/insulator interfaces is a well-known difficult problem. Starting from the days of GaAs/Si_3N_4, GaAs/SiO_2 and GaAs/anodic oxide in 1970s [11, 12], almost all the conceivable passivation trials have been made

up to now with different degrees of success. For InGaAs E-mode MOSFETs, approaches currently attracting attention include, (1) sulfur-passivation using $(NH_4)_2S$ chemical treatment [13], (2) use of Si interface passivation layer (IPL) [2, 14-16], (3) $Ga_2O_3(Gd_2O_3)$ dielectric by UHV MBE [5, 16], and (4) amorphous Al_2O_3 using ALD [16, 17]. It would be the best if dielectric deposition alone can provide the low interface state density. However, $Ga_2O_3(Gd_2O_3)$ has insufficient *k* value (~14) and immature deposition technology. Amorphous Al_2O_3 has lower *k* value of 9 as well.

Sulfur-passivation by wet chemical treatment has been adopted in the E-mode MOSFET demonstrations as a practical and effective passivation of GaAs-based III-V surface after the native oxide removal by wet etching [4, 13, 17]. It is believed that the $(NH_4)_2S$ treatment leaves the cleaned InGaAs surface sulfur-terminated with a weak bonding of chemisorbed sulfur over the surface like the case of GaAs [18]. Thus, the formation of native oxides of InGaAs may be much suppressed during air exposure before loading the samples into the dielectric deposition chamber. However, the wet chemical treatment alone is not sufficient to accomplish a well-ordered surface passivation mainly due to the poor thermal stability of the sulfur bonds on surface [19].

So far, the Si interface layer technique has been successfully implemented to E-mode GaAs and InGaAs MOS devices, showing the most promising device performance in scaled devices [2, 14-15]. However the III-V/Si/high-*k* structure with the Si interface layer may have significant inherent issues. Although the Si/high-*k* interfaces have been well studied by present research groups with mature Si-based process techniques, it still faces Fermi level pinning issues as well as low-*k* interfacial layer problem [20]. If the Si interface layer in the III-V/Si/high-*k* stack is consumed by oxidation during the device fabrication processing, it would result in the low-*k* SiO_2 (*k* = 3.9) interfacial layer and the III-V/SiO_2 interface to be inevitably produced. The III-

V/SiO_2 interface has been reported as one of the sources of Fermi level pinning [21]. In addition, the III-V/Si interface should be examined with consideration of its thermodynamic stability and the doping level of the channel, which can be perturbed by Si diffusion into III-V [15]. Therefore, Si interface passivation with the narrow process window may increase process complexity in device fabrication in order to control the interface reaction. This is seen in the case where the addition of nitridation treatment after deposition of the Si interface layer [22] was to be carried out, and this may eventually limit the scalability of III-V MOSFET due to the two interfaces of III-V/Si and Si/high-*k*.

Since the most detrimental effects on the III-V/oxide interface come from the volatile V-oxide species [12], especially from AsO_x, passivating of the III-V surface in phosphorus-rich ambient to switch to a more stable P-terminated III-V surface [23] prior to dielectric deposition is a plausible approach to achieve a good interface of III-V materials for their MOS-device applications. It has been reported that the phosphorus passivation of $In_{0.53}Ga_{0.47}As$ [24] suppresses AsO_x on InGaAs and reduces density of interface states obtained for $Au/Ga_2O_3(Gd_2O_3)$/P-passivation/InGaAs MOS capacitors compared to the sample without passivation. The study showed the lowest D_{it} when a very thin GaP epi-layer deposition was used as the P-passivation method. However, the reported P-passivation method using *in situ* metal-organic vapor phase epitaxy (MOVPE) is not compatible with Si-based device industry. Any E-mode InGaAs MOSFET realization has not been reported with the P-passivation method also.

4.1.3 CONCEPT OF APPROACHES AND OBJECTIVE

PH_3-based process has been widely used in Si processing to make n^+ poly electrode using thermal or plasma process technique. We have reported that PH_3-based passivation using plasma improves electrical performance of the Ge MOSFET integrated with high-*k*/metal gate stack [25].

To realize high electron mobility MOSFET on $In_{0.53}Ga_{0.47}As$ with improved electrical performance, we have aimed to explore and study the PH_3-based passivation for $In_{0.53}Ga_{0.47}As$/MOCVD high-*k* interface. The chamber atmosphere filled with PH_3 and N_2 may suppress evolutions of the undesirable oxides and group V vacancies in the passivation process prior to dielectric deposition because all the constituents, including products, are composed of group V elements. In addition, the presence of hydrogen in the system can enhance the removal of V-group element segregation by forming volatile hydrides (VH_3) [23]. The passivation has been carried out using a commercialized multi-chamber CVD tool which is fully compatible with Si-based CMOS process. The MOS structure with the passivation is depicted in Fig. 4.1.

In order to assess the feasibility of this passivation technique for the III-V MOS device application in the near future, it is crucial to understand how and what kind of passivation layer is formed on the III-V surface by the PH_3-based thermal or plasma-assisted treatment and how practical the technique is. We have studied the PH_3-based passivation process at various conditions in order to get inspiration for understanding the interface passivation technique for further applications of the passivation.

Thermal stability of the passivated gate stack is another important requirement for the advanced III-V MOS device applications. The $HfO_2/In_{0.53}Ga_{0.47}As$ gate stack with the preliminarily optimized PH_3-based plasma-assisted passivation has been annealed at different S/D RTA temperatures up to 750 ^oC in a self-aligned gate-first

MOSFET fabrication scheme and the electrical characteristics of the fabricated MOSFETs have been examined.

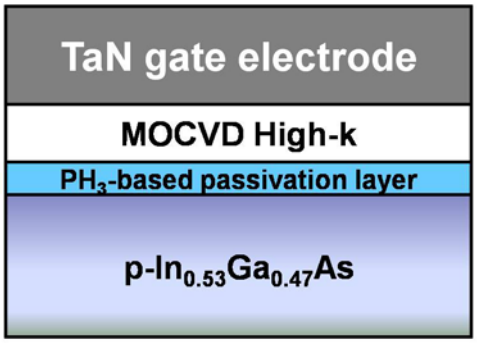


Fig. 4.1 Schematic MOS structure integrated with high-*k*/metal gate on InGaAs substrate passivated with PH_3-based passivation technique.

4.2 EXPERIMENT

4.2.1 PH_3-BASED PASSIVATION CONDITIONS

A p-type $In_{0.53}Ga_{0.47}As$ layer (Zn-doped, ~1 x 10^{17} cm^{-3}) grown by MBE on a p^+ InP wafer with an InP buffer layer was used in this study. The $In_{0.53}Ga_{0.47}As$ surface was cleaned by 1% dilute HF for 2 min to remove native oxides and treated in $(NH_4)_2S$ for 5 min at room temperature to prevent oxidation during the air exposure afterward. Subsequently, the samples were loaded in a multi-chamber CVD and the plasma PH_3-N_2 passivation was carried out in a PECVD-type passivation chamber. A schematic configuration of the multi-chamber CVD is illustrated in Fig. 4.2.

In the passivation processing, the chamber pressure was stabilized with PH_3 gas diluted at 1% with N_2 for 10 s first, followed by a main surface passivation step with rf (13.56 MHz) plasma. The process parameters of temperature, pressure, rf plasma power, and time were varied within the range of maximum hardware capacity to examine their effects on $In_{0.53}Ga_{0.47}As$ substrate. To inhibit the passivation layer growth by a CVD mechanism at low pressure and to achieve an effectively thin

passivation layer, the chamber pressure was fixed at 0.3 Torr for the plasma processes. This was the maximum pressure where the reddish plasma afterglow, which is evidence to show the presence of excited species in the plasma phase, was observed in an rf power range of 200-500 W.

The process condition of the higher pressure of 0.7 Torr with the application of rf plasma power, i.e., the condition where the afterglow was absent, was included to confirm how the afterglow phenomena affect the passivation result. In addition, the samples without passivation (labeled as none) and annealed in 1% PH_3/N_2 without plasma (sample A), which is based on an n-type doping condition using PH_3 for Si at high temperature and pressure [26], were also added for comparison. Detailed surface passivation conditions are listed in Table I.

Table 4.1 $In_{0.53}Ga_{0.47}As$ surface passivation conditions using 1% PH_3/N_2 treatment.

Sample no.	Temperature	Pressure	Plasma power	Time
A	550 ^oC	10 Torr	no plasma	1 min
B	430 ^oC	0.3 Torr	200 W	1 min
C	430 ^oC	**0.7 Torr**	200 W	1 min
D	430 ^oC	0.3 Torr	200 W	**5 min**
E	430 ^oC	0.3 Torr	**500 W**	1 min
F	**550 ^oC**	0.3 Torr	200 W	1 min
none	no treatment			

AFM and XPS were employed after the passivation to analyze the morphology and surface chemistry. The surface morphology of the passivated $In_{0.53}Ga_{0.47}As$ surface was investigated by AFM operating in a tapping mode with a conventional Si probe. XPS spectra were acquired using a JEOL JPS-9010MX spectrometer with a Mg Kα X-

ray source at 1253.6 eV with 10 eV pass energy. Under the measurement conditions, the overall resolution measured from the full width at half-maximum (FWHM) of the Cu $2p_{3/2}$ core level was 1.2 eV. All core level photoemission peaks were referenced to the As 3d core level (41.2 eV) to compensate for the charging effect in the overlayer. A detailed XPS analysis was performed using by angle-resolved XPS measurement at take-off angles (TOAs) (θ) of 30 and 90°. *In situ* Ar sputtering was used to etch the sample surface in order to obtain a bulk-like InGaAs surface and physically validate the passivated layer's thickness. The etching rate was controlled at ~1 Å/s after calibrating the input control parameters using a smooth 10 nm thick HfAlO dielectric layer on Si and ellipsometry for thickness verification.

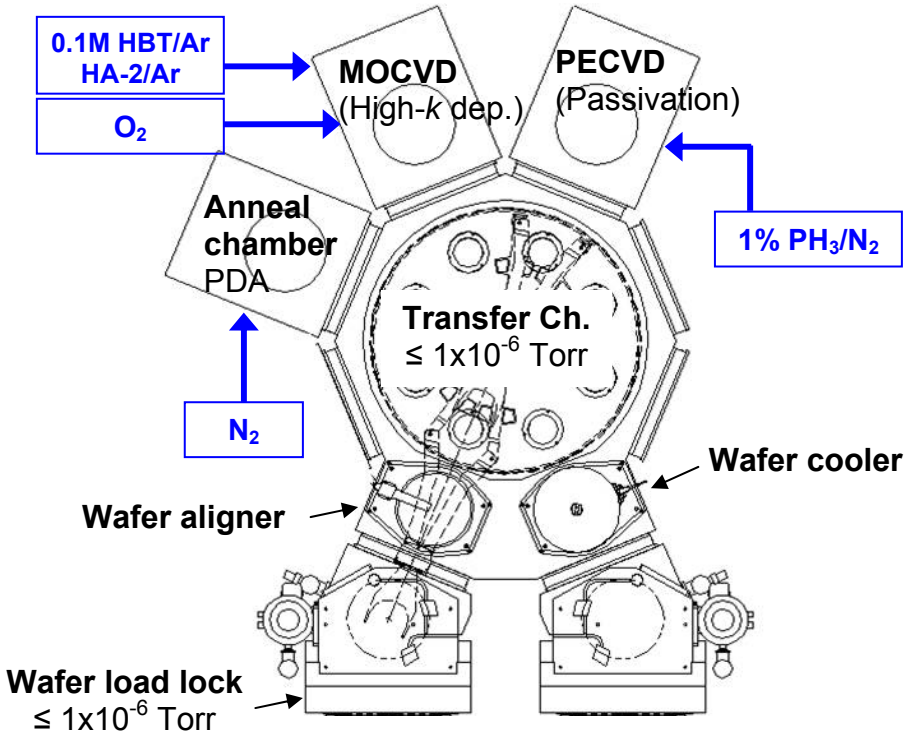


Fig. 4.2 Schematic drawing of the multi-chamber CVD used.

4.2.2 *IN SITU* HIGH-*k* INTEGRATION AND DEVICE FABRICATION

The $In_{0.53}Ga_{0.47}As/HfO_2/TaN$ MOSFET fabrication process flow with a self-aligned gate-first scheme in this passivation study is summarized in Fig. 4.3, reflecting the development works done in the previous chapter.

- MBE grown $In_{0.53}Ga_{0.47}As$ (Zn, ~1×10^{16} cm^{-3}) on InP substrate
- 1% HF and $(NH_4)_2S$ cleaning at room temperature
- **PH_3-based passivation using 1% PH_3/N_2 gas**
- MOCVD HfO_2 deposition at 400 ^oC using HBT and O_2
- PDA at 400 ^oC in N_2 for 30~60 sec

} ***In situ* process using muti-chamber CVD**

- Sputter TaN deposition 150nm
- Lithography (Long channel mask)
- Gate etch using RIE and high-k etching using 1% HF
- E-beam SiO_2 deposition 10 nm
- Si implantation (50 KeV/1×10^{14} cm^{-2})
- Encapsulation using e-beam SiO_2 100 nm
- RTA S/D activation at 600 ^oC 1 min (+ 700 ^oC 10 sec, 750 ^oC 5 sec for thermal stability estimation experiments)
- SiO_2 removal and S/D contact mask
- E-beam AuGe/Ni/Au deposition and lift-off
- Ti/Pt/Au backside contact deposition
- Metal alloy RTA at 400 ^oC for 1 min
- FGA at 400 ^oC in H_2+N_2 for 10 min

Fig. 4.3 Process flow of self-aligned InGaAs channel MOSFET with PH_3-based passivation process.

The PH_3-based passivation process is highlighted in the process flow. Note that *in situ* passivation process was carried out until PDA of HfO_2 dielectric layer, which was deposited on the passivated $In_{0.53}Ga_{0.47}As$, without a break of vacuum using a

multi-chamber CVD (Fig. 4.2). The base pressure of the system was maintained ≤ 1×10^{-6} Torr for the transfer chamber. PH_3-based passivation was conducted using 1% PH_3 diluted in N_2 in a PECVD chamber, followed by HfO_2 deposition using HBT and O_2 as a precursor and oxidant at 400 ^oC and 0.4 Torr. Then PDA was performed at 400 ^oC and 200 Torr in N_2 for 30-60 s without breaking the vacuum. The HfO_2 deposited sample was loaded into sputter to deposit TaN electrode film immediately.

In addition, the thermal stability of the passivated gate stack was examined with electrical properties of the MOSFETs by carrying out S/D activation RTA at different conditions of 600 ^oC 1 min, 700 ^oC 10 s, and 750 ^oC 5 s.

4.3 RESULTS AND DISCUSSION

4.3.1 MORPHOLOGY OF THE PASSIVATED $In_{0.53}Ga_{0.47}As$

Figure 4.4 shows AFM images of $In_{0.53}Ga_{0.47}As$ surfaces after different surface passivations as listed in Table. 4.1.

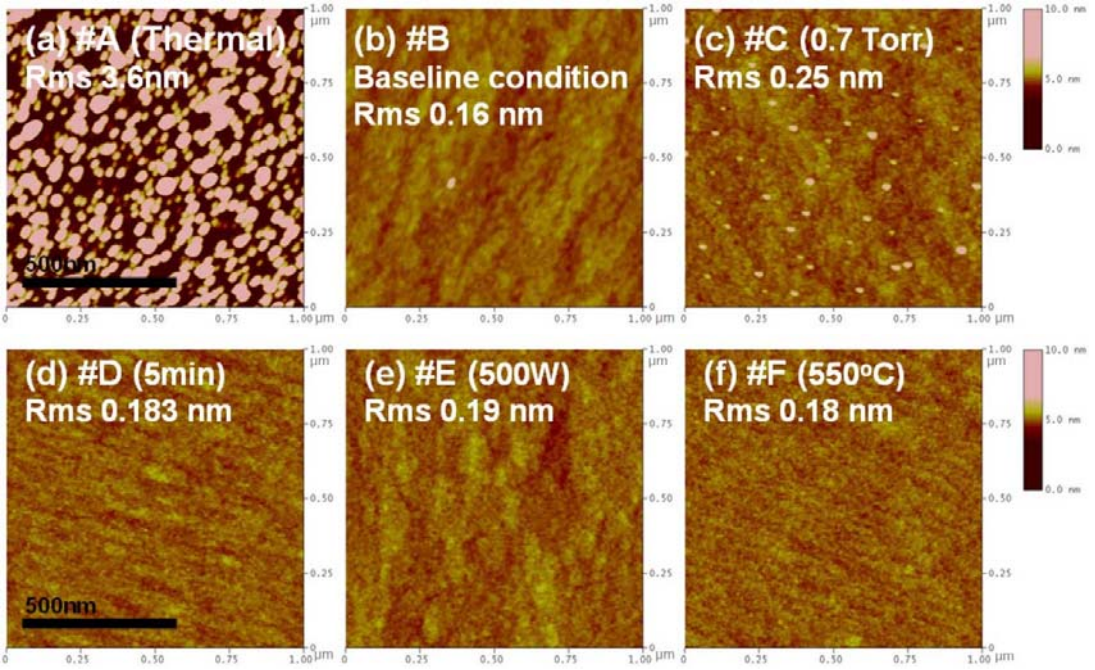


Fig. 4.4 AFM images of $In_{0.53}Ga_{0.47}As$ surfaces passivated with 1% PH_3/N_2 at different conditions as listed in Table 4.1.

Compared to the $In_{0.53}Ga_{0.47}As$ surface without passivation (rms = 0.15 nm, not shown), no significant changes are observed for samples B, D, E and F, while notable surface modification and increase of surface roughness are observed for samples A and C (rms = 3.6 and 0.25 nm respectively). Wallart and Priester reported that $In_{0.53}Ga_{0.47}As$ surface roughening occurs upon phosphorus incorporation, forming quaternary (InGaAsP) alloy through surface reconstruction, where PH_3 is used at 500 ^oC [27]. It was also reported that surface modifications such as protrusion and crosshatch have been observed when anion exchange reaction between group V atoms in reactants and substrate occurs on the III-V semiconductor surface [28, 29]. Therefore, the surface modifications observed in PH_3 annealed samples A and C, treated without afterglow discharge, may suggest that the P-for-As exchange reaction is the major type of phosphorus incorporation for the PH_3-based treatments of $In_{0.53}Ga_{0.47}As$. This is supported by the chemical analysis that is discussed in the following section. However, the obtained low values of rms surface roughness below 0.2 nm for samples B, D, E, and F without significant surface modifications like A and C indicate that the major reaction of the PH_3-N_2 plasma passivation on the $In_{0.53}Ga_{0.47}As$ surface at afterglow discharge conditions may be different from those of sample C and of the PH_3 annealed sample A.

4.3.2 CHEMISTRY OF THE PH_3-BASED PASSIVATION LAYER ON $In_{0.53}Ga_{0.47}As$ SURFACE

XPS analysis was carried out to investigate the effects of passivation process parameters such as pressure, time, plasma rf power, and temperature on the PH_3-based passivation chemistries where 1% PH_3/N_2 gas was used as a source reactant on the $In_{0.53}Ga_{0.47}As$ surface. Figure 4.5 shows the As 3d, Ga 3d, In 3d, P 2p, and N 1s core

level spectra, where the XPS TOA is 90°, for the $In_{0.53}Ga_{0.47}As$ samples prepared as listed in Table 4.1. The P 2p core level spectra in Fig. 4.5d well characterize the PH_3-passivated $In_{0.53}Ga_{0.47}As$ surfaces, drawing a distinction between samples A and C and the other samples B, D, E, and F.

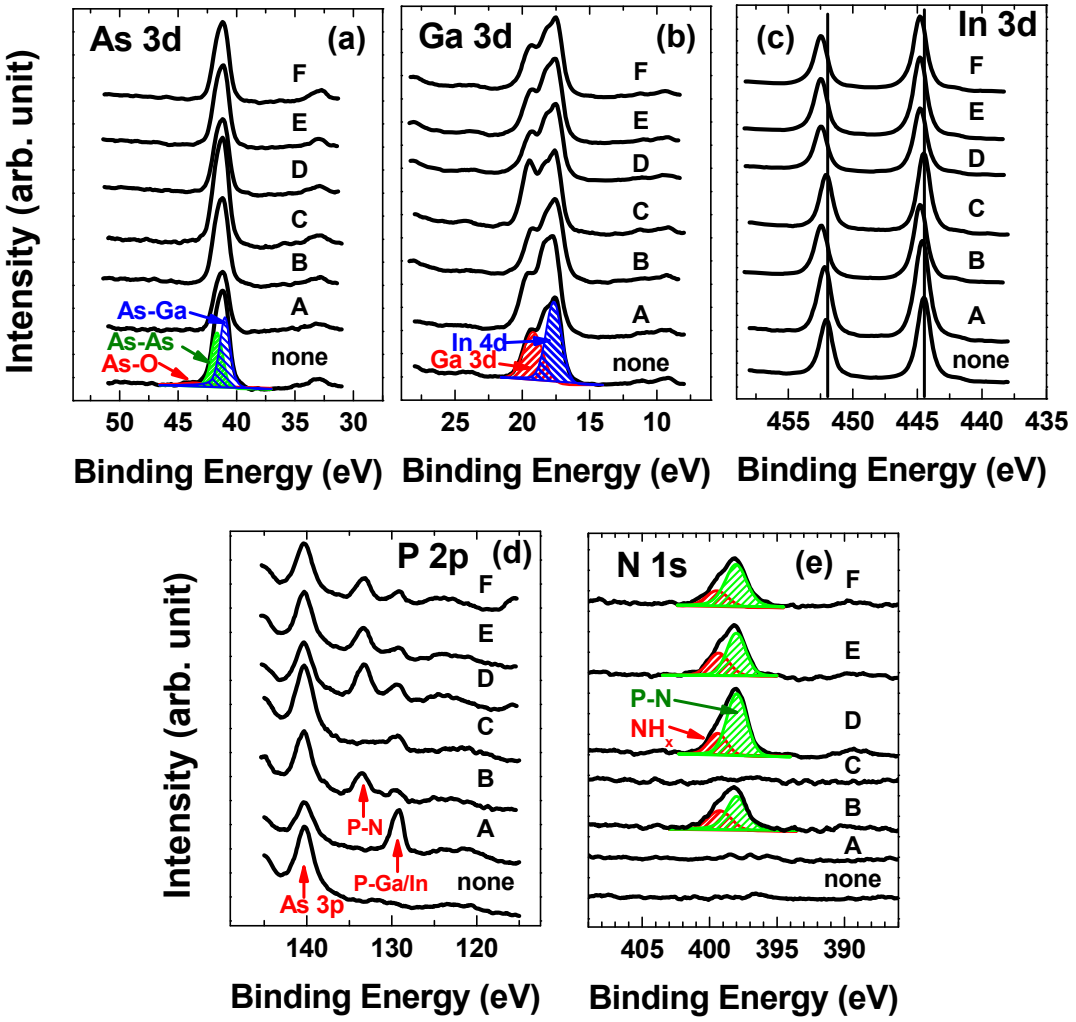


Fig. 4.5 XPS spectra for the $In_{0.53}Ga_{0.47}As$ surfaces with and without the PH_3-based passivation treatment as listed in Table 4.1; (a) As 3d, (b) Ga 3d, (c) In 3d, (d) P 2p, and (e) N 1s core level spectra for the different samples.

All of the PH_3-treated samples (A-F) exhibit P-metal (In/Ga) bond formation with the corresponding P 2p peak at BEs of 129.1-129.6 eV [23, 29]. As expected from the experimental design, the PH_3 annealed sample A shows the most intensive P-metal

bond peak (P $2p_{P\text{-}M}$) at 129.2 eV among the treated samples shown in Fig. 4.5d. Sample C shows a broad P $2p_{P\text{-}M}$ peak centered at 129.3 eV with reduced peak intensity compared to sample A, agreeing with the AFM results in Fig. 4.4a and c, where the surface roughness may reflect a degree of P-metal bonding. However, the additional high energy peaks at 133.3 ± 0.1 eV clearly appear for samples B, D, E, and F with Gaussian shapes (FWHM = 1.9, 1.9, 1.8, and 1.8 eV for samples B, D, E, and F, respectively) in their P 2p spectra, showing the formation of the P_xN_y compound (ref. BE = 132.8-134.5 eV) [24, 30-32] as shown in Fig. 4.5e for samples B, D, E, and F.

The broad (FWHM = 2.5, 1.9, 2.1, and 2.0 eV for samples B, D, E, and F, respectively) and asymmetric N 1s core level spectra with a shoulder at the higher BE region can be decomposed into two peaks, at 399.2 ± 0.1 and 398.0 ± 0.03 eV, with a range of values determining their fraction, regardless of the sample. Typical deconvolution results are displayed in Fig. 4.5e. The XPS results for samples B, D, E, and F show the well defined P $2p_{P\text{-}N}$ lines, indicating that P atoms occupy chemically equivalent sites and the asymmetric N 1s lines, with at least two different chemical states of N atoms in the passivation compound, agree well with the chemical and structural characteristics of P_xN_y. P_xN_y is composed of PN_4 tetrahedra with different linking types, resulting in detection of various chemical states of N atom and a single chemical state of P atom [32, 33].

The difference in physical and chemical surface properties between sample C and the P_xN_y-containing samples B, D, E, and F is consistent with the fact that the glow discharge is absent only for the treatment condition C among the process conditions where the rf plasma power is applied. Moreover, considering the morphological changes, the P-metal bonds in sample C may roughen the InGaAs surface, as previously reported [27], while such roughening does not occur for the other samples

B, D, E, and F, although the P $2p_{P\text{-}M}$ peak intensities of samples B, D, E, and F are comparable to sample C. Thus, among the passivation samples where the rf power is applied, samples B, D, E and F are differentiated by the glow discharge reaction during passivation, the smooth surface, and the formation of the P_xN_y layer. Nitrogen incorporation with P-N chemical bond formation occurs at 0.3 Torr where the glow discharge plasma of the PH_3-N_2 system is identified, suggesting that the plasma activated species including nitrogen may play a major role in passivating the InGaAs surface with P_xN_y at the low pressure PH_3-N_2 plasma system, while the sample C condition of 0.7 Torr shows neither the afterglow nor nitrogen incorporation into the InGaAs substrate. Similarly, it has been reported that the lower density of activated N species in N_2-H_2 and N_2-NH_3 plasmas at 1 Torr results in a much reduced thickness of GaN, which is produced from the nitridation of GaAs, compared to those at 0.2 Torr [34]. Bruno et al. reported that the emission intensities of excited species (H* and PH_x*) strongly decrease with the increase of chamber pressure in the range 0.1-1 Torr in the PH_3-H_2 plasma [35]. These papers on the plasma-activated species which depends on the pressure can support the formation of different passivation layers at 0.3 and 0.7 Torr in the PH_3-N_2 plasma investigated.

Since an anion exchange reaction, which is revealed by the P-metal bond in the InGaAs substrate where no sources of metal atoms are provided, is considerably observed on the passivated sample, the InGaAs surface composition was examined for the different passivation samples. The semi-quantitative analysis of the InGaAs substrate peaks is summarized in Table 4.2. Since a trace of As oxide was detected at around 44 eV in the As 3d line for the non-treated InGaAs sample (Fig. 4.5a), a bulk-like $In_{0.53}Ga_{0.47}As$ surface sample was prepared by *in situ* Ar sputtering ~10 Å on the non-treated sample, after the surface XPS measurement, and characterized as a bulk

reference surface. Sample A shows a significant change in the substrate composition (atomic ratio of In/As from their 3d peak intensities = 1.1, while it is equal to 0.5 for the bulk surface) with a substantial As depletion from the surface, indicating that P atoms replace As atoms, thus maintaining chemical bonds between anion and metal atoms on the surface, as clearly shown in Fig. 4.5a-d. Sample C presents a slight accumulation of As (In/As = 0.4) with increase in free As composition. On the contrary, samples B, D, E, and F maintain the substrate compositions obtained from In/As ratios as bulk InGaAs substrate.

Table 4.2 Summary of relative intensities of different XPS core level emissions from substrate elements and the binding types of As at the passivated $In_{0.53}Ga_{0.47}As$ surfaces. The As 3d and Ga 3d peaks were decomposed into different binding types and core levels without spin-orbit splitting. The number in parenthesis refers to the chemical shift from a main As-Ga/In component and the difference of BE of the decomposed emissions for As 3d and Ga 3d, respectively.

Sample ID	In 3d/As 3d	composition of As 3d			composition of Ga 3d	
		As-Ga/In	As-As	As-O	Ga 3d	In 4d
None	0.5	0.52	0.46 (0.6 eV)	0.02 (3.1 eV)	0.4	0.6 (1.6 eV)
A	1.1	0.6	0.4 (0.7 eV)	-	0.3	0.7 (1.7 eV)
B	0.5	0.6	0.4 (0.7 eV)	-	0.4	0.6 (1.6 eV)
C	0.4	0.5	0.5 (0.6 eV)	-	0.4	0.6 (1.7 eV)
D	0.5	0.6	0.4 (0.7 eV)	-	0.4	0.6 (1.6 eV)
E	0.5	0.6	0.4 (0.7 eV)	-	0.4	0.6 (1.6 eV)
F	0.5	0.6	0.4 (0.7 eV)	-	0.4	0.6 (1.6 eV)
Bulk	0.5	0.7	0.3 (0.7 eV)	-	0.5	0.5 (1.5 eV)

The type of chemical composition of As is important to examine the impact on electrical properties and the anion exchange reaction mechanism further. Hence, As 3d peaks (FWHM = 1.5 ± 0.01 eV) are compared by its decomposition into different

chemical states: As-O, As-As, and As-Ga/In bonds from As oxide, elemental As, and InGaAs components, reapectively, by the chemical shifts in the As 3d core level emission, as displayed in the first spectrum of Fig. 4.5a. The spin-orbit splitting was not taken into account due to the present resolution limit in the XPS measurement, and this may overestimate the elemental As composition whose chemical shift from As bonded with Ga or In (0.6 eV) [36] is close to the spin-orbit splitting of the As 3d emission (0.7 eV) [36]. Nevertheless, it is intuitively found that the As 3d peak analysis, especially the composition of elemental As, differentiates the passivation reactions coherently and agrees well with the observation of the In 3d BE shift by sample conditions. Figure 4.6 shows the BE of the In $3d_{5/2}$ core level emission for the different samples including the bulk sample, indicating that the peak position shifts to higher BE with the decrease in free As composition analyzed in Table 4.2.

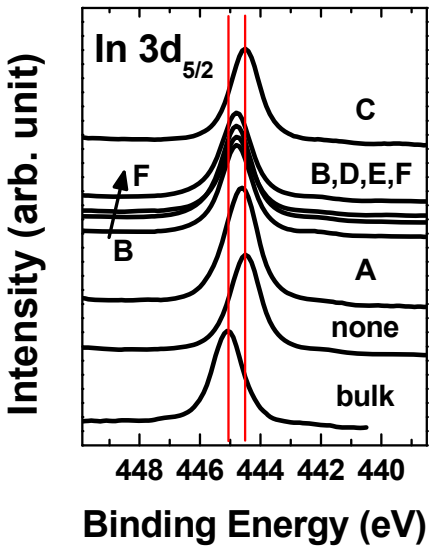


Fig. 4.6 In $3d_{5/2}$ core level spectra for the $In_{0.53}Ga_{0.47}As$ surfaces with and without passivations

This interesting relation between the As composition and the peak position of the In 3d core level can be explained by the fact that the As 3d peak is used as an

internal energy reference to circumvent the charging effect in our XPS measurement. The increase in the free As fraction moves the As 3d peak to higher BE, changing the peak shape accordingly, resulting in the appearance of the other core levels at lower BEs than the true BEs. The consequences appeared in the peak shifts of the relatively narrow In 3d peaks (FWHM = 1.2 ± 0.01 eV) to lower BE, with the increase in composition of elemental As at different $In_{0.53}Ga_{0.47}As$ samples. This explanation is consistent with the fact that the BEs of In 3d peaks in InGaAs and InP are similar at 444.4 eV [37], and so the validity is not controversial to be extended to the finding of sample A of which InP is a considerable composition of In atoms. Fortunately, the peak shift caused by the internal calibration is not sufficient to affect phosphorus- and nitrogen-related species analyzed from the P 2p and N 1s core levels above.

However, if the In 3d peak shift is explained by the possible indium chemical components such as InO_x (BE = 445.3 eV [38]), InN (BE = 444.8 eV [29]), and metallic In (BE = 443.6 eV [29]), it raises many inconsistencies with the composition analysis of the corresponding and related XPS core level emissions as well as with the bulk sample. For example, the In-N component can be determined with concentrations varying 0-3% from deconvolution analyses of the N 1s peaks (BE = 396.6 eV for N bonded in InN [39]) for samples B, D, E, and F but this disagrees with the result that the In 3d peak positions (Fig. 4.6) and Ga 3d/In 4d peak analysis (Table 4.2) are identical for those samples. Therefore, based on the observation of the In 3d peak shift in the present experiment, the PH_3-N_2 plasma passivation, which includes the P_xN_y layer, may allow us to achieve a more bulk-like $In_{0.53}Ga_{0.47}As$ interface with an effective suppression on detrimental As components such as AsO_x and free As. The suppression of free As for the effective PH_3-N_2 plasma treatment (samples B, D, E, and F) can be supported by the fact that active hydrogen species have often been

reported with its effect in promoting free As desorption by forming volatile AsH_x species in plasma treatments of GaAs [29, 34, 40].

4.3.3 CHEMISTRY OF THE P_xN_y PASSIVATION LAYER ON $In_{0.53}Ga_{0.47}As$ SURFACE

In order to further investigate the P_xN_y passivation, which is distinguished as the low pressure plasma-assisted process in the PH_3-N_2 system compared to the other PH_3-based treatments studied, the chemistry of the passivated layer is comparatively analyzed in detail including the effect of the process parameters (samples B, D, E, and F) using various XPS measurement techniques, which include angle-resolved measurement and depth profiling.

Since the phosphorus incorporated layer is composed of two apparent chemical species, i.e., P_xN_y and P-metal (In/Ga) bonded components, the impact of process condition on these phosphorus incorporations has been examined. Figure 4.7a shows the relative contribution of the P-N and P-M bonds determined by the ratios extracted from the peak area intensities of the P $2p_{P\text{-}N}$ and P $2p_{P\text{-}M}$ peaks, which are detected at 133.3 ± 0.1 and 129.3 ± 0.2 eV respectively, using the angle-resolved XPS measurement and deconvolution analysis for the different samples. The peak separation and quantification were carried out using deconvolution analysis with several fittings, i.e., at least three runs. As a result, the spread of quantification data is depicted with the average value in Fig. 4.7. The ratio of P $2p_{P\text{-}N}$/P $2p_{P\text{-}M}$, which is larger than 2, indicates that P_xN_y is a major phosphorus component incorporated into the passivation layer for all the P_xN_y passivated samples (B, D, E, and F). The angle-resolved result showing that the P $2p_{P\text{-}N}$/P $2p_{P\text{-}M}$ ratio is larger at the surface sensitivity enhanced XPS measurement (TOA = 30^o) reveals that the P_xN_y layer exists on top of

the P-metal bonded layer of the whole passivation layer. In addition, Fig. 4.7a indicates that the relative chemical composition of the phosphorus-incorporated layer is similar at/near the top surface in the quantification confidence level regardless of the sample, suggesting a conformal P_xN_y layer covers for the entire sample, agreeing with the AFM results. However, samples D, E, and F exhibit that the two phosphorus-containing layers become more distinguishable by depth than sample B, where the ratio of the two components is not so obviously different by depth in the confidence level estimated. This is seen especially in the deeper profiles measured at TOA=90°, which indicate that the P $2p_{P\text{-}N}$/P $2p_{P\text{-}M}$ ratio is reduced by processing $In_{0.53}Ga_{0.47}As$ for 5 min (sample D) or at 550 °C (F) compared to InGaAs treated at 430 °C for 1 min (B). The result of samples D and F may indicate that the passivation reaction mechanism is complex, with P_xN_y formation paths being controlled neither by a single path of gas phase deposition nor by CVD in a surface reaction controlled regime, and with P-metal bond formation kinetics where phosphorus diffusion into InGaAs can play a role.

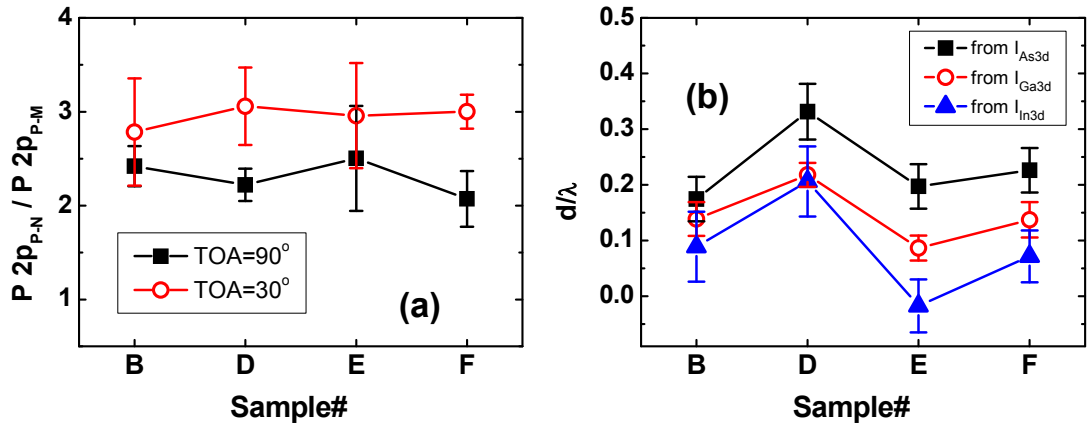


Fig. 4.7 (a) The P 2p peak area intensity ratios of P-N bond over P-metal bond components measured at TOAs of 30 and 90° for the different P_xN_y passivation samples of B, D, E, and F. (b) The passivation layer thickness determined from the XPS peak area intensities of As 3d, Ga 3d, and In 3d spectra for the P_xN_y passivation samples processed at different conditions. The thickness is represented by the unit of the attenuation length, λ. The error bar indicates the standard deviation.

The thicknesses of the passivation layers for the different P_xN_y passivation samples were calculated from the substrate peak intensities obtained at TOA = 90 and 30^o according to the equation [41]

$$d_{film} = \lambda_{film(s)} \sin\theta \ln \frac{I_s^\infty}{I_s} \tag{4.1}$$

where d_{film} is the film thickness, $\lambda_{film(s)}$ is the attenuation length of the emerging electron in the film, θ is the TOA, and I_s^∞ and I_s are the substrate peak intensities for the bulk and the passivation layer covered substrate, respectively. Figure 4.7b shows the passivation layer thicknesses obtained using different substrate peaks of As 3d, Ga 3d and In 3d, measured with error ranges introduced in the quantification. Since λ depends on the material properties of the film as well as the kinetic energy of the electron, the passivation layer thickness is thus represented by the unit λ. The thickness determined from the substrate XPS peak intensity depends on the element of substrate and the PH_3-N_2 plasma process condition. This result implies that the substrate elements may be involved differently in the passivation reactions according to the process conditions. Roughly, λ is inversely proportional to the electron BE and atomic number for different elements [42]. Thus, if there is neither a reaction between the overlayer and substrate nor a redistribution of the substrate atoms, the thickness of d/λ determined by each substrate element XPS peak intensity would be in the order of the atomic number, i.e., d/λ from In 3d > d/λ from As 3d ≥ d/λ from Ga 3d. However, the result of Fig. 4.7b shows that this is not the case and the thickness extracted from the As 3d line shows a larger value than those from In 3d and Ga 3d for all the P_xN_y passivation samples, indicating loss of As atoms from the InGaAs substrate during the passivation reaction. For the P_xN_y passivation, phosphorus and nitrogen atoms are incorporated and the P-metal bond forms by phosphorus incorporation simultaneously.

Therefore the P-for-As exchange reaction, which can result in the P-In/Ga bond instead of the As-In/Ga bond, may be responsible for the larger thickness extracted from the As 3d emission intensity. The tendency of the smaller thickness measured from the In 3d peak than that from the Ga 3d may be due to a preferred type of ordering of the cations in the affected InGaAs substrate, which definitely needs further systematic approach and careful investigations.

However, it is worth noting that the chemical compositions of the passivated InGaAs substrates of samples B, D, E, and F are similar, regardless of the process condition (Table 4.2), whereas the thickness analysis in Fig. 4.7b shows the difference between the P_xN_y passivation samples. The disagreement between the thickness and substrate component analyses may be because the passivation layer is atomically thin. Assuming the range of λ is 2-3 nm for the XPS measurement range used [42], the P_xN_y passivation layer thickness obtained can be as thin as 3-6 Å and even with the inclusion of the P-for-As exchanged layer, the thickest whole passivation layer becomes ~9 Å for sample D. In contrast, the sampling depth at TOA = 90^o, which is used for the component analysis, is considered as ~50 Å [41]. In order to confirm the estimation of the passivation layer thickness, XPS depth profile measurement was carried out for samples B, D, E, and F using *in situ* sputtering with an etching rate of ~1 Å/s.

Figure 4.8 shows the results of XPS depth profiles for the P 2p and N 1s spectra of the different P_xN_y passivation samples. Regardless of the process condition, all the peaks corresponding to the P-N bond almost dramatically disappeared after etching for 2 s, which is equivalent to the film thickness of ~2 Å according to the calibration. Moreover, in Fig. 4.8a, sample D clearly shows that the P-for-As exchanged layer locates under the P_xN_y layer with a considerable thickness compared to the other

samples. In Fig. 4.8b, N 1s peak profiles, which agree excellently with the P $2p_{P\text{-}N}$ profiles, obviously indicate that nitrogen is incorporated as a P_xN_y layer for all the P_xN_y passivated samples. Thus, it is revealed that ~1 monolayer (ML) thick P_xN_y layer is formed on the P-for-As exchanged layer by the low pressure plasma-assisted process of $In_{0.53}Ga_{0.47}As$ in the PH_3-N_2 system, independently of the process conditions investigated. This result may allow us to consider that the P_xN_y passivation mechanism in the system investigated is partly subjected to a self-limiting one. The thickness extracted from XPS substrate peak intensities in Fig. 4.7b therefore indicates the density of P_xN_y film screening XPS emission intensities for each sample rather than the passivation layer thickness directly.

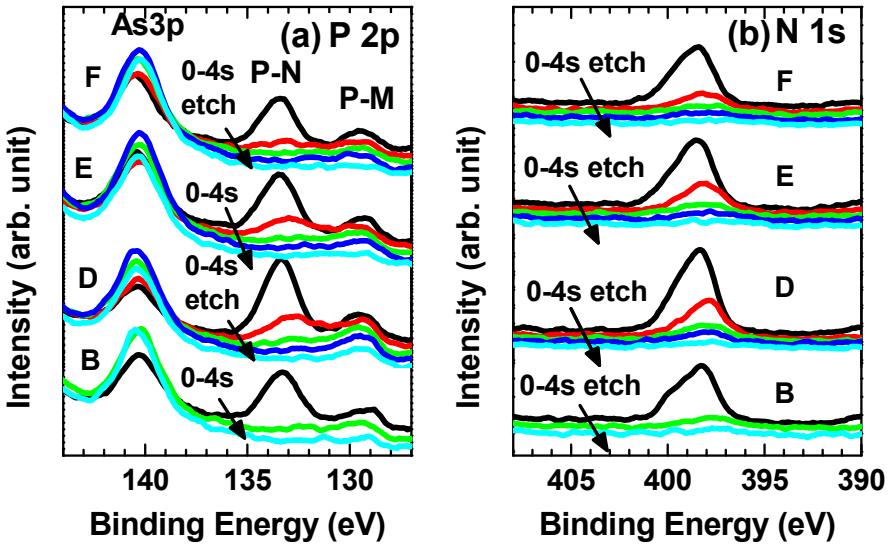


Fig. 4.8 XPS depth profiles for the different P_xN_y passivation samples B, D, E, and F of (a) P 2p and (b) N 1s core level spectra measured at TOA = 30°. *In situ* sputtering has been employed with a film etching rate of ~1 Å/s.

Based on the result that the nitrogen-incorporated layer is separated from the whole passivation layer that is affected by the treatment in the form of the P_xN_y layer, the atomic ratios of nitrogen/phosphorus for the P_xN_y layers can be extracted from N 1s and P $2p_{P\text{-}N}$ peak area intensities; these are 1.9 ± 0.1, 2.2 ± 0.1, 2.1 ± 0.1, and 2.6 ± 0.4

for samples B, D, E, and F, respectively. The stoichiometry of *y/x* of the P_xN_y layer formed on the InGaAs substrate is increased at the enhanced process conditions of time (5 min), rf plasma power (500 W), and temperature (550 ^oC) compared to the treatment at 430 ^oC and 200W for 1 min.

Based on the findings about the passivation layer structure, the amount of phosphorus and nitrogen incorporations was estimated from the relative peak area intensities against the InGaAs substrate of P/InGaAs and N/InGaAs from the P 2p, N 1s, In 3d, Ga 3d, and As 3d spectra at TOA = 90^o, with the chemical states of the incorporated species. The result is depicted in Fig. 4.9.

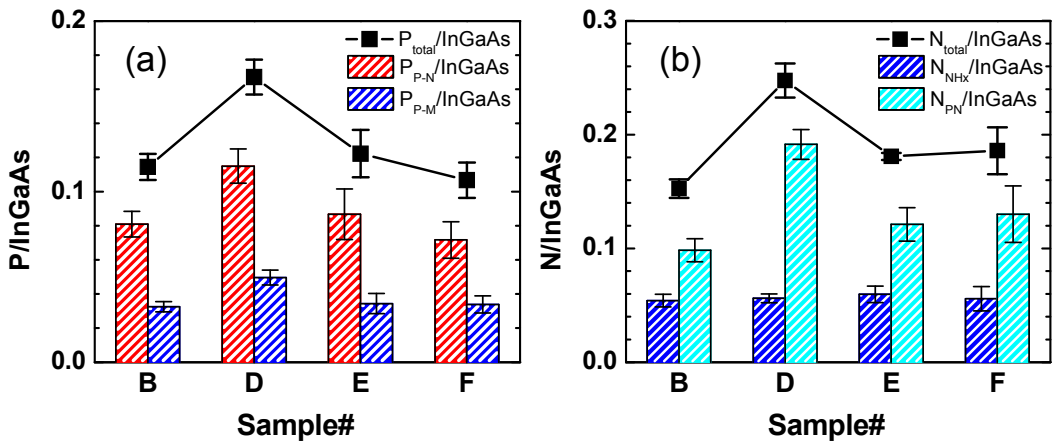


Fig. 4. 9 (a) The amount of phosphorus incorporation into the substrate from the relative XPS peak intensity of P/InGaAs for the P_xN_y passivated samples (B, D, E, and F) determined from the phosphorus chemical components of P-N and P-metal bond which are indicated as $P_{P\text{-}N}$ and $P_{P\text{-}M}$, respectively. P_{total}/InGaAs indicates the total amount of phosphorus incorporation. (b) The amount of nitrogen incorporation with relative intensity of N 1s line against the InGaAs substrate peaks for samples B, D, E, and F. The fractions of different chemical components of NH_x (where x=1 or 2) and P-N are indicated as N_{NHx}/InGaAs and N_{PN}/InGaAs, respectively, with total amount of nitrogen incorporation, N_{total}/InGaAs.

The total phosphorus incorporation is divided into P_xN_y and P-for-As exchanged layer components in Fig. 4.9a, shown as $P_{P\text{-}N}$ and $P_{P\text{-}M}$, respectively. The XPS profiles of the P_xN_y passivation layers for samples D, E, and F in Fig. 4.8 show

the 1 s etching profiles matching well with the degrees of phosphorus incorporation in the P_xN_y component layer in Fig. 4.9a, which are in the order of D > E > F. The amount of phosphorus incorporation in P_xN_y component is changed by 42, 7, and -11 % for samples D (5 min), E (500 W), and F (550 ^oC), respectively, compared to sample B (1 min, 200 W, and 430 ^oC). The amount of phosphorus incorporation into InGaAs substrate as the P-for-As exchanged layer is not significantly changed, with similar values of 6 and 4 % for samples E and F, respectively compared to sample B, while a 53 % increase is seen for sample D.

The effect of process condition on phosphorus incorporation is different for different chemical species of phosphorus. The P-for-As exchanged layer is affected significantly by time (5 min), but not by rf power (500 W) and temperature (550 ^oC) compared to the condition of sample B. Since P_xN_y is a covalent compound that decomposes above ~850 ^oC [33], the lower P-for-As exchanged layer may not be formed by phosphorus outdiffusion from the upper P_xN_y layer. If the outdiffusion mechanism plays a significant role in the anion exchanged layer growth in the PH_3-N_2 plasma system studied, the temperature effect would be more prominent than the time impact. In fact, the deposition of solid phosphorus has been reported as a main reaction in the plasma PH_3 system [35], and the P_xN_y layer has been synthesized by the plasma-assisted treatment of an amorphous phosphorus layer using N_2 plasma [32]. Therefore, the result of sample D showing the phosphorus incorporation in the P-for-As exchanged layer under the P_xN_y layer increasing significantly at longer processing time and the self-limiting tendency in P_xN_y deposition in the systems studied, enables us to suggest a mechanism that includes an intermediate phosphorus-rich layer which can be deposited competing with P_xN_y deposition and followed by P_xN_y formation by nitridation with the active nitrogen species.

The impact of the plasma passivation process condition on the incorporation of nitrogen in the P_xN_y layer exhibits different trends from the effects on phosphorus incorporation. Figure 4.9b shows that the amount of nitrogen incorporation is significantly increased for all the fortified process conditions by 62, 19, and 22 % for 5 min of treatment time (sample D), 500 W of rf power (E), and 550 ^oC of temperature (F), respectively, compared to sample B's condition of 1 min, 200W, and 430 ^oC. The nitrogen incorporation is examined by the chemical components that are obtained from the two components located at 399.2 ± 0.1 and 398.0 ± 0.03 eV by the decomposition analyses mentioned in the previous section and summarized in Fig. 4.9b. The BE separation of 1.2 eV between the BEs of those nitrogen components excellently agrees with the value of the N 1s BE difference between N atoms in the chemical environment of complete nitride $(Si)_3{\equiv}N$ and in NH_x (where x=1 or 2) reported in the atomic chemical environment identification experiment in the nitridation of Si by the Si/NH_3 system using N 1s XPS spectra analyses [43]. In order to support the existence of different nitrogen chemical states of $(P)_2{=}NH$, $P\text{-}NH_2$, and $(P)_3{\equiv}N$, the facts that include (1) P_xN_y has a characteristic networking structure based on the PN_4 tetrahedra linked in various ways such as sharing the nitrogen vertexes and edges [33]; (2) the hydrogen atoms can be covalently bonded to N atoms in various types of P-N skeleton of PN_4 tetrahedra connected as proven in the crystal structure of HPN_2 [44]; and (3) the presence of active hydrogen in the PH_3 plasma system [35] can be used. Thus, taking into account Si, the assignment that the 399.2 eV peak is for NH_x (where x=1 or 2) and the other for $(P)_3{\equiv}N$ would be plausible for the N 1s peak of nitrogen in P_xN_y layers formed in the $PH_3\text{-}N_2$ plasma system studied. These nitrogen components corresponding to the chemical environments of $P_{3-x}NH_x$ and $(P)_3{\equiv}N$ are indicated as N_{NHx} and N_{PN}, respectively, in Fig. 4.9b.

Figure 4.9b indicates that the increase in degree of nitrogen incorporation is mainly due to the lower BE component of nitrogen, which is assigned for N atom forming three covalent bonds with P atoms, while NH_x components remain the same by the change in passivation process conditions. The results reveal that the N_{NHx} component disappeared first for samples D, E, and F in the XPS profiles (Fig. 4.8b) and the amount of NH_x component is similar for all the samples, and this may imply that the nitrogen bonding with hydrogen exists on the very topmost surface of the P_xN_y passivation layer. In addition, this may indicate the presence of active hydrogen in the plasma system studied. The results of nitrogen incorporation do not conflict with the explanation on the mechanism that the P_xN_y layer can be formed not only by CVD reaction but also by nitridation of phosphorus in the interface layer formed during the passivation reaction.

On the basis of the above results and considerations, the passivation reactions in the InGaAs/PH_3-N_2 plasma system investigated may include (a) the P-for-As exchange reaction between InGaAs and PH_3 before the plasma exposure step that can occur in the PH_3-based treatments without the afterglow discharge; (b) the production of plasma-activated species of phosphorus, nitrogen, and hydrogen; (c) the gas phase reactions resulting in P_xN_y layer deposition; (d) phosphorus adsorption on the surface; (e) the P-for-As exchange reaction between InGaAs and the activated phosphine (PH_3*); (f) the nitridation of phosphorus at the surface by the activated nitrogen yielding P_xN_y and increasing its ratio y/x; (g) the P-for-As exchange reaction of the InGaAs surface with phosphorus diffused from the adsorbed phosphorus; and (h) evaporation of AsH_3 where P-for-As exchange reaction occur in the presence of hydrogen. The series of reactions can be listed as follows:

$$x\mathrm{PH_3} + \mathrm{InGaAs} \rightarrow \mathrm{InGaAs_{1-x}P_x} + x\mathrm{AsH_3(g)}\uparrow \qquad \text{(a, h)}$$

$$N_2 \rightleftarrows 2N^* \quad \text{(b)}$$

$$PH_3 \rightleftarrows PH_3^* \rightleftarrows P^*(g) + 3/2\ H_2 \quad \text{(b)}$$

$$xP^*(g) + yN^* \rightarrow P_xN_y(s)\downarrow \quad \text{(c)}$$

$$P^*(g) \rightleftarrows P(s)\downarrow \quad \text{(d)}$$

$$xPH_3^* + InGaAs \rightarrow InGaAs_{1-x}P_x + xAsH_3(g)\uparrow \quad \text{(e, h)}$$

$$xP(s) + yN^* \rightarrow P_xN_y(s)\downarrow \quad \text{(f)}$$

$$xP(s) + InGaAs \rightleftarrows InGaAs_{1-x}P_x + xAs \quad \text{(g)}$$

From a thermodynamic point of view, the bond strength of the reaction product PN (6.39 eV [45]) is greater than the P-P bond (5.07 eV [45]) and P/As-In/Ga bonds (2-3 eV [45]). Therefore, the higher chemical stability of P_xN_y can be the driving forces for the irreversible reactions. For the P-for-As exchange reactions, the bond strength of In/Ga-P bonds (2.05 and 2.38 eV, respectively [45]) is comparable with In/Ga-As (2.08 and 2.1 eV [45]) and, hence, the reaction mechanism may not be simple. However, the prevailing mechanism where the phosphorus layer adsorbed at the surface may be an intermediate product leading to the phosphorus doping into Si substrate [26] and the P-for-As anion exchange reaction of GaAs [28], can explain our result coherently. According to the model, the fast subsequent reactions of the adsorbed phosphorus with the active nitrogen and substrates would result in P_xN_y and P-for-As exchanged InGaAs (f and g) upon plasma exposure in the PH_3-N_2/InGaAs system studied. In addition, the extended processing time may cause further subsequent reactions of the P-for-As exchanged InGaAs surface with active hydrogen, which is the most movable species through the layers, and nitrogen producing the same products, and these can be formulated as

$$InGaAs_{1-x}P_x + xAs + 3/2\ H_2 \rightarrow InGaAs_{1-x}P_x + xAsH_3(g)\uparrow \quad \text{(i)}$$

$$InGaAs_{1-x}P_x + xAs + yN^* \rightarrow InGaAs + P_xN_y(s)\downarrow \quad \text{(j)}$$

The chemical stability and the volatility of the products may be the driving forces of the reactions. These reactions, including the further reactions on the P-for-As exchanged InGaAs interface (i and j), can explain the result of sample D where both the P_xN_y and P-for-As exchanged layers are increased by 5 min treatment but maintain the substrate composition like free As fraction to be the same as the 1 min processing of sample B.

Considering the self-limiting nature of P_xN_y monolayer formation regardless of the process conditions investigated, the reaction path of nitridation (f) seems to be more dominant than the gas phase reaction (c) under the plasma process conditions studied at 0.3 Torr. Similarly, this passivation tendency due to the P_xN_y layer inhibiting further nitridation has been reported in the plasma nitridation of GaP and InP substrates under process conditions similar to those in this study [29]. The increase in plasma power may enhance the electron density resulting in the number of activated species produced and, hence, this causes the plasma-assisted reactions to increase. The amount of phosphorus incorporation at the process condition of 1 min (samples B, E, and F) may be limited compared to nitrogen incorporation due to the concentration of PH_3 in the source (1 % PH_3/N_2) where phosphorus has more reaction paths than nitrogen. Sample F processed at 550 ^oC showed reduced amount of phosphorus in the P_xN_y layer slightly compared to the 430 ^oC sample (B), while nitrogen incorporation is significantly increased. The temperature effect on the phosphorus incorporation paths should be studied with further sophisticated experiments.

4.3.4 MOSFET CHARACTERISTICS OF THE PASSIVATED $In_{0.53}Ga_{0.47}As$/HIGH-*k*/TaN GATE STACKS

The effects of the PH_3-based passivation processes of $In_{0.53}Ga_{0.47}As$ on the electrical properties of the InGaAs/high-*k* interface were investigated by characterizing the fabricated MOSFETs and eventually a high mobility NMOSFET was demonstrated with the P_xN_y passivation technique.

All of the passivated MOSFETs show well-behaved E-mode I_D-V_D characteristics. Figure 4.10a shows typical output characteristics of the passivated $In_{0.53}Ga_{0.47}As/HfO_2$ MOSFET with a gate length of 4 μm at V_G = 0~3 V indicating that the P_xN_y layer passivation (samples B and D) enhances the drive current by a factor of more than 2 compared to the other types of PH_3-based passivation (samples A and C).

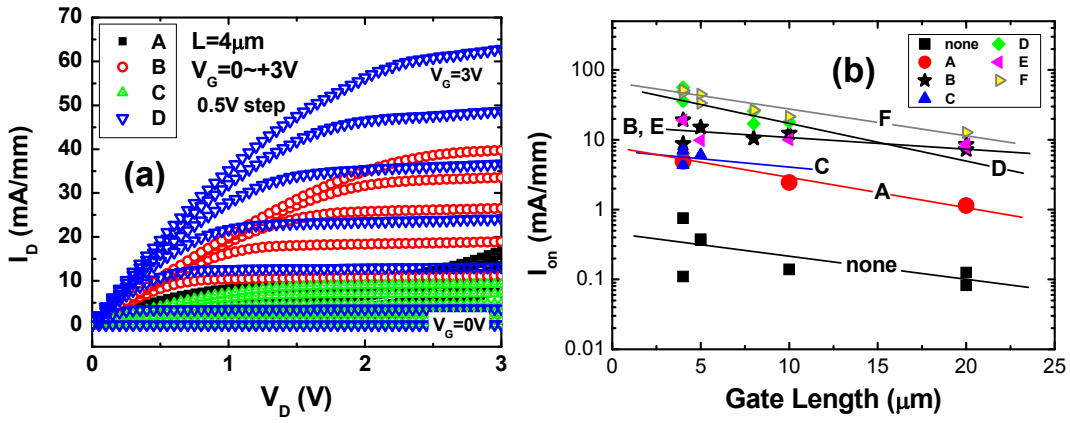


Fig. 4.10 (a) I_D-V_D characteristics for the $In_{0.53}Ga_{0.47}As/HfO_2/TaN$ MOSFET with different passivation conditions. (b) On-current, I_{on} which is I_D at V_G = 3 V and V_D = 1 V for the different passivation conditions as a function of gate length of the MOSFET devices.

Figure 4.10b shows I_{on}, which is I_D at V_G = 3 V and V_D= 1 V, as a function of gate length for the different MOSFETs with and without passivation. Higher drive currents are obtained from the PH_3-based passivation samples over the non-passivated sample and from the passivation samples with a P_xN_y layer over those without P_xN_y. Among the P_xN_y passivated MOSFETs, samples D and F tend to exhibit higher I_{on} than samples B and E. The considerable spread of data in Fig. 4.10b may be largely due to the immaturity of the III-V MOSFET fabrication processing. In order to further discern

the effects of the passivation process on MOSFET electrical properties, inversion *C-V* properties have been measured at different frequencies and compared for the different passivation samples.

From the inversion *C-V* measurement of the MOSFET devices at a low frequency of 1 kHz, similar EOTs of 2.3-2.5 nm were obtained for all the PH_3-based passivation samples (A-F), while a value of 2.8 nm was recorded for the non-passivated sample. The results of EOT for the samples imply that PH_3-based passivation suppresses the interfacial reactions, which can lead to low-*k* interfacial layer growth, compared to the non-passivated gate stack. Sample A, however, may not follow this trend, as its surface is too rough to identify its impact on the effective area of the capacitor and thereby on the EOT. The values of gate leakage current at $V_G = V_{FB} + 1$ V were 8×10^{-7}, 1.4×10^{-4}, and $2\text{-}3 \times 10^{-7}$ A/cm^2 for the non-passivated sample, PH_3-annealed sample A, and the other PH_3-based passivation samples (B-F), respectively. The rough surface morphology after PH_3 anneal, as seen in Fig. 4.4a, may be responsible for the higher gate leakage current of sample A through uneven high-*k* and TaN deposition on the rough surface where electron tunneling may occur at the sites where a very thin dielectric layer is deposited.

In III-V MOS devices, a large frequency dispersion in *C-V* characteristics is anomalous and this unexplained behaviors may be caused by fast traps in the disordered layer at the III-V/insulator interface [46]. Figure 4.11 shows inversion *C-V* plots at a high frequency of 1 MHz. The data were obtained using the split *C-V* measurement technique, which can estimate the gate-to-channel capacitance (C_{gc}) of devices showing a carrier accumulation response to an applied gate field where an inversion layer is being formed. Greatly improved inversion *C-V* curves with a sharp transition, i.e., without Fermi-level pinning, are achieved from the samples with the

P_xN_y passivation layer (B, D, E, and F), whereas degraded *C-V* curves are obtained from the non-passivated and PH_3-based passivation samples without a P_xN_y layer (A and C).

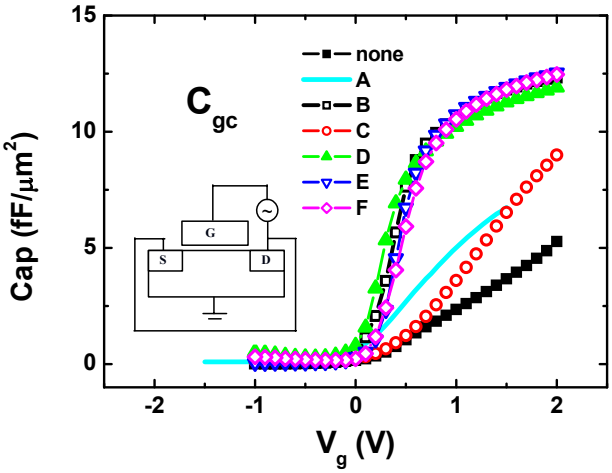


Fig. 4.11 Gate-to-channel capacitance (C_{gc}) versus gate voltage of the passivated and non-passivated $In_{0.53}Ga_{0.47}As$ MOSFETs measured at 1 MHz using split *C-V* method.

The frequency dispersion ($\Delta C_{1kHz\sim1MHz}/C_{1kHz}$ at V_G = 2 V) in C_{gc} is summarized in Fig. 4.12. The figure indicates that the frequency dispersion is strongly suppressed by the introduction of the P_xN_y passivation layer into the $In_{0.53}Ga_{0.47}As/HfO_2$ stack. Compared to the non-passivated sample, the frequency dispersion in C_{gc}-*V* is suppressed by 82-94 % for the P_xN_y passivated samples (B, D, E and F), while it is reduced by 10 % for sample A and 68 % for sample C. The hysteresis in the *C-V* curves is measured from a V_{FB} shift in a bidirectional *C-V* measurement at 100 kHz. P_xN_y layer passivation also effectively inhibits the *C-V* hysteresis (61-69 % reduction compared to the non passivated sample).

Although the trend is similar for the suppression of frequency dispersion and hysteresis according to the sample conditions, the hysteresis suppression by passivation is less remarkable than the improvement in frequency dispersion.

Furthermore, the hysteresis appears to approach a certain limit in the results of Fig. 4.12. This can be attributed to the variation in the defects causing the phenomena, even though the interface passivation influences those defects simultaneously.

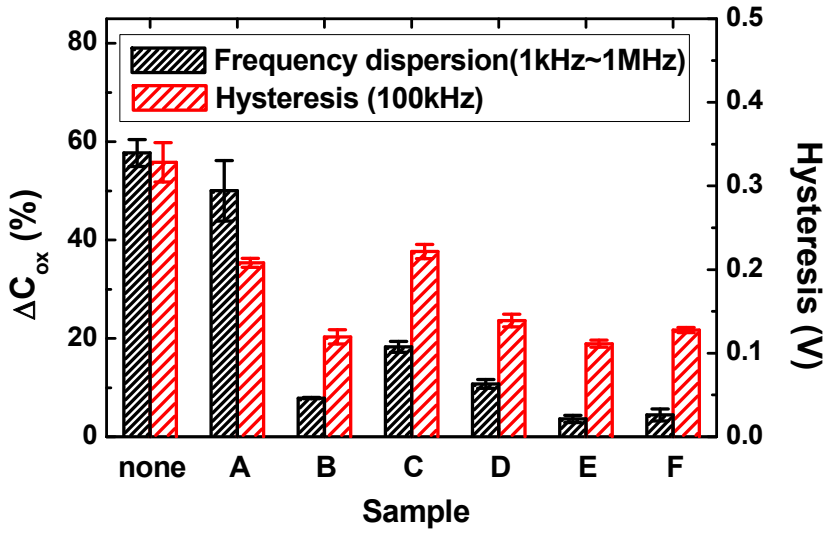


Fig. 4.12 Frequency dispersion obtained from the difference of inversion capacitance, C_{gc} at V_G = 2V between 1 kHz and 1 MHz and hysteresis measured from a V_{FB} shift in bidirectional *C-V* measurement at 100 kHz for different passivation conditions on $In_{0.53}Ga_{0.47}As/HfO_2$ MOSFET.

Hysteresis represents slow traps, whereas frequency dispersion may indicate fast traps. The interface qualities may thus more strongly affect frequency dispersion, while the interior dielectric qualities may have a greater impact on the hysteresis [47]. For the traps inside the dielectric, the capability of passivation layer to prevent interdiffusion of atoms between the gate stack layers would influence the dielectric qualities. This can be seen in the results of samples A and C. Sample A, which has a thicker P-for-As exchanged layer but a much worse surface morphology than sample C, exhibits a slightly lower hysteresis of 208 mV compared to that (222 mV) of sample C, which has a reduced P-for-As exchanged layer. This may reflect that the PH_3-based passivation prevents atomic interdiffusion, especially for As atoms, resulting in defects inside HfO_2, and this may have a greater impact than the degree of disorder in the

rough interfacial layer. Highly suppressed hysteresis of ~50 mV has been reported when MOCVD HfAlO is used instead of HfO_2 for a high-*k* gate stack with P_xN_y passivation (condition of sample B) [48], thus indicating the effect of dielectric quality on hysteresis also.

Improved interface quality by P_xN_y passivation is also exhibited in the comparison of SS presented in Fig. 4.13. Compared to the devices without passivation and annealed in PH_3 (sample A), a substantially reduced SS in a range of 90-120 mV/dec is achieved with the P_xN_y passivated samples. The trends of frequency dispersion and SS according to the passivation conditions agree well, indicating that these parameters mainly depend on interfacial qualities such as trap densities.

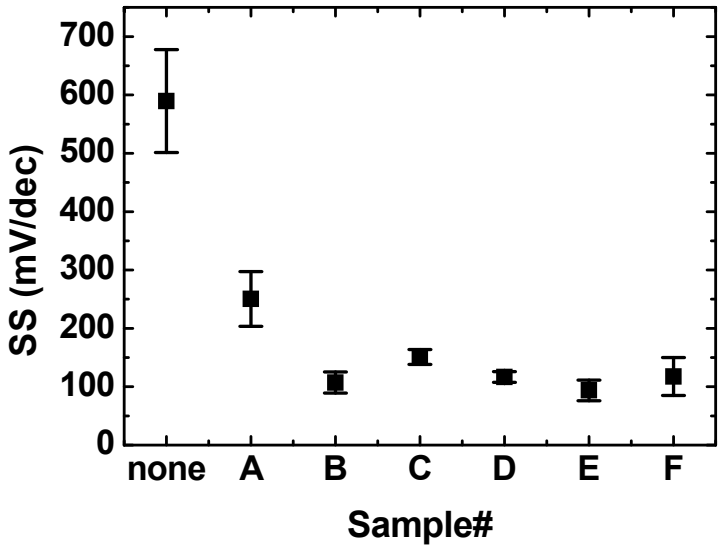


Fig. 4.13 SS for the MOSFETs with different passivation conditions.

As another factor affecting SS in the present P_xN_y passivation studies, the dielectric constant of the substrate can be considered due to the presence of the underlying P-for-As exchanged layer. The dielectric constant of $In_{0.53}Ga_{0.47}As$ is 11.6, while it is 13.8 for $In_{0.53}Ga_{0.47}As_{0.9}P_{0.1}$ [49]. As the substrate dielectric constant is lowered, an accordingly smaller SS can be achieved. The smallest SS value for sample

D was 109 mV/dec, whereas the other P_xN_y passivation samples showed the minimum SS values in the range 60-70 mV/dec, as seen in the data spread in Fig. 4.13. This may reflect the effect of the P-for-As exchanged layer under the P_xN_y passivation layer. Among the P_xN_y passivation samples, sample E demonstrates the best interface properties, showing the most reduced frequency dispersion and the realization of the theoretical limit value (60 mV/dec) of SS. However, the maximum current drivability of the MOSFET devices was not in a simple relation with the interface quality or capacitance for the different passivation conditions.

The D_{it} values of $In_{0.53}Ga_{0.47}As/HfO_2$ MOSFET devices were estimated using Hill's conductance method [50] and summarized in Table 4.3 for samples A, B, and C compared to the non-passivated sample. The expression used for calculating the interface trap density is given by

$$D_{it} = \frac{(2/qA)\cdot(G_{\max}/\omega)}{\left(\frac{G_{\max}}{\omega C_{ox}}\right)^2 + \left(1-\frac{C_m}{C_{ox}}\right)^2} \tag{4.2}$$

where G_{max} is the maximum conductance in the conductance-voltage (G-V) plot with its corresponding capacitance (C_m), C_{ox} is the oxide capacitance, ω is the angular frequency and $\omega=2\pi f$, where f is the measurement frequency, A is the capacitor area, and q is the elemental charge. Here the conductance values were used after series resistance, R_s correction [51] according to the series of equations follows;

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{4.3}$$

where G_{ma} and C_{ma} are the measured conductance and capacitance in strong accumulation and then corrected parallel conductance, G_c is

$$G_c = \frac{(G_m^2 + \omega^2 C_m^2)a}{a^2 + \omega^2 C_m^2} \tag{4.4}$$

where $a = G_m - (G_m^2 + \omega^2 C_m^2) R_s$, and C_m and G_m are the capacitance and the equivalent conductance measured across the terminals of the MOS capacitor, respectively. D_{it} is reduced by one order of magnitude by PH_3-based passivation. However, the extracted D_{it} value is much higher than expected from the improved *C-V*, *I-V* characteristics for sample B compared with sample A and C, indicating that the extracted D_{it} is not a sensitive indicator for the interfacial quality of the PH_3-based passivated InGaAs/HfO_2 MOS devices compared to the *C-V* frequency dispersion and SS. The extrinsic factor of the fabricated InGaAs device and the D_{it} characterization method, which has been developed for Si device estimation, can be considered as one of the reasons for the inaccuracy of the result quantifying interfacial quality [46].

Table. 4.3 Interface state density (D_{it}) estimated by Hill's conductance method for $In_{0.53}Ga_{0.47}As$ /HfO_2/TaN MOSFET with different PH_3-based passivations.

Sample#	D_{it}
A	4.9×10^{12} /eVcm^2
B	4.0×10^{12} /eVcm^2
C	5.5×10^{12} /eVcm^2
none	1.8×10^{13} /eVcm^2

Although the current drivability was not proportional to interfacial quality of the InGaAs/high-*k* MOSFET due to the immature fabrication, a high mobility NMOSFET with the peak mobility of 2557 cm^2/Vs at effective electric field, E_{eff} = 0.24 MV/cm has eventually been realized where the InGaAs MOSFET device was integrated with the P_xN_y passivation, MOCVD HfAlO, and TaN metal gate in a self-aligned scheme. Figure 4.14a shows the I_D-V_G characteristics of $In_{0.53}Ga_{0.47}As/P_xN_y$/HfAlO MOSFET with L_G = 17 μm at V_D = 1 and 0.05 V. SS was

98 mV/dec with negligible DIBL. The I_{on}/I_{off} ratio was about 5 orders. Mobility was extracted for the device using the split C-V method and it is shown in Fig. 4.14b as a function of E_{eff}. The mobility was not corrected by parasitic series resistance or D_{it}. In addition, with L_G = 600 nm, a high transconductance, G_m of 378 mS/mm was recorded at V_D = 1V (Fig. 4.15a). The high G_m in the present realization is compared with the reported E-mode InGaAs NMOSFETs in Fig. 4.15b.

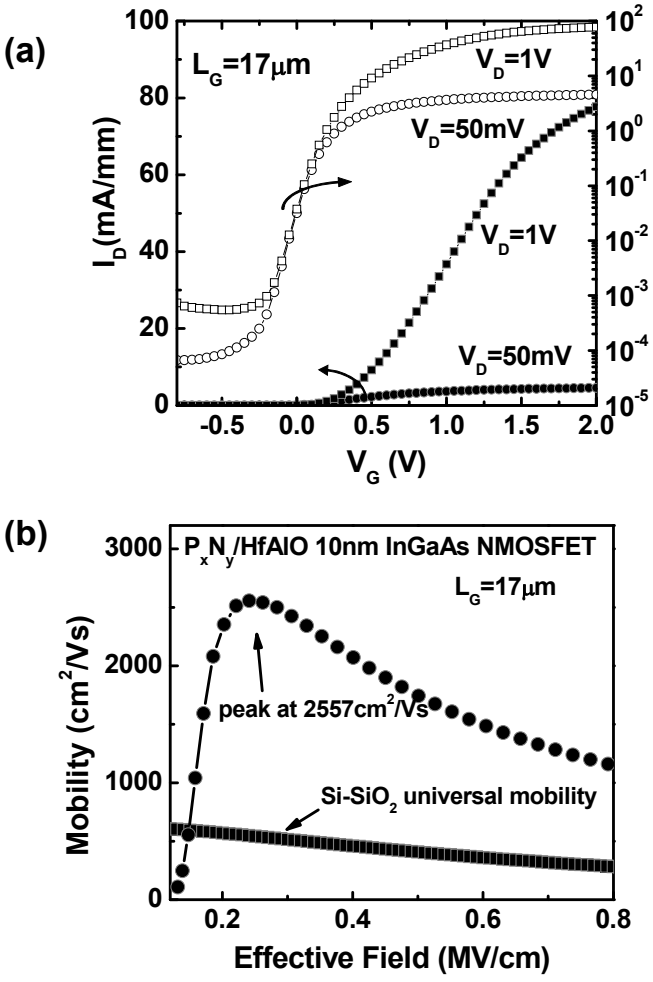


Fig. 4.14 (a) I_D-V_G characteristics of MOCVD HfAlO/TaN NMOSFET on P_xN_y-passivated $In_{0.53}Ga_{0.47}As$ (L_G = 17 μm). (b) Mobility vs effective electric field of the InGaAs device in comparison with the Si universal mobility curve.

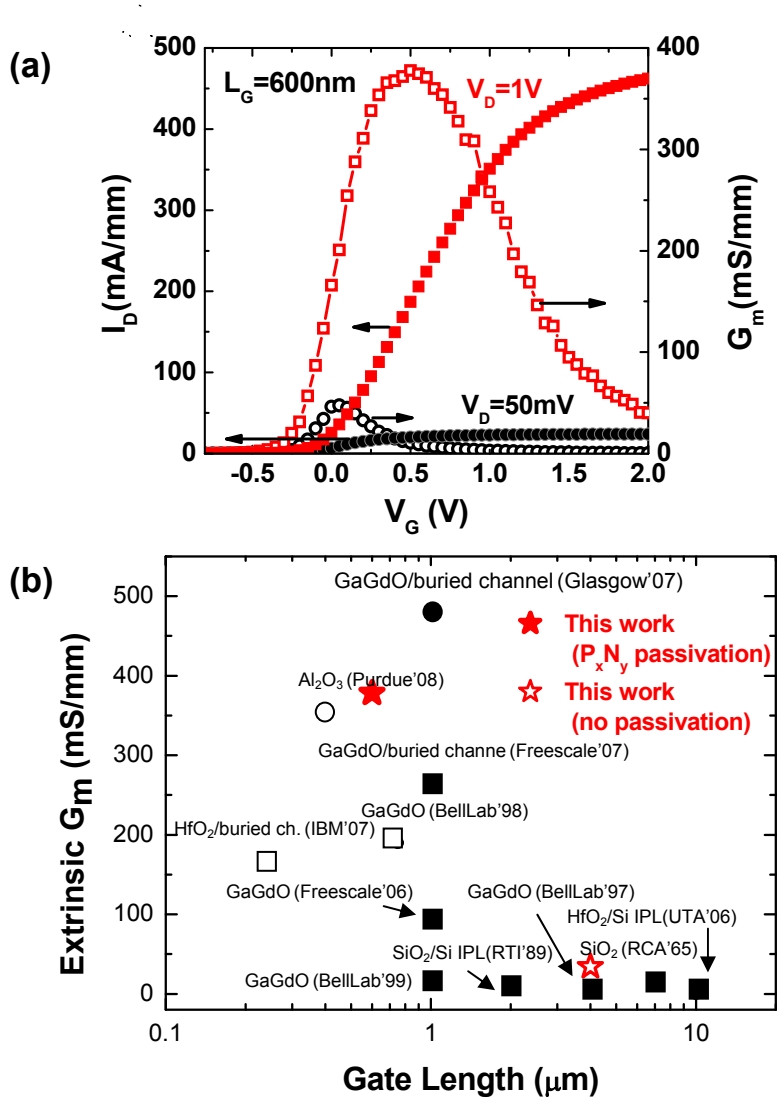


Fig. 4.15 (a) I_D-V_G characteristics of the P_xN_y-passivated InGaAs/HfAlO/TaN MOSFET with L_G = 600 nm, showing G_m of 378 mS/mm. (b) Comparison of G_m of the InGaAs NMOSFETs with and without the P_xN_y-passivation in this work with the published G_m of E-mode NMOSFETs from 1965 to 2008 (Fig. 1.17). Open symbols are high indium concentration channels of InGaAs (In≥0.53), whereas closed symbols are GaAs or InGaAs with low indium concentration channels in the previously reported data [52].

4.3.5 THERMAL STABILITY OF PHOSPHORUS NITRIDE PASSIVATED GATE STACK

In order for the P_xN_y passivation to be a promising interface engineering technique for III-V MOSFET device applications, thermal stability of the high-*k* gate stack with the passivation should be examined in a temperature range of device

fabrication. In this section, the thermal stability of the P_xN_y-passivated gate stack was studied with a self-aligned MOSFET fabrication process by increasing RTA temperature up to 750 ^oC in the S/D activation step. The P_xN_y passivation process condition was the condition of sample B in Table 4.1. For this experimental batch, FGA was not carried out in order to prevent a possible disturbing the effect of S/D RTA on electrical properties of the MOSFETs due to hydrogen incorporation into the gate stack during the FGA step.

Figure 4.16 shows TEM images of HfO_2 on InGaAs substrate with P_xN_y passivation layer after RTA at 600 ^oC for 1 min, 700 ^oC for 10 s, and 750 ^oC for 5 s compared to the non-passivated InGaAs/HfO_2/TaN gate stack annealed at 700 ^oC for 10 s.

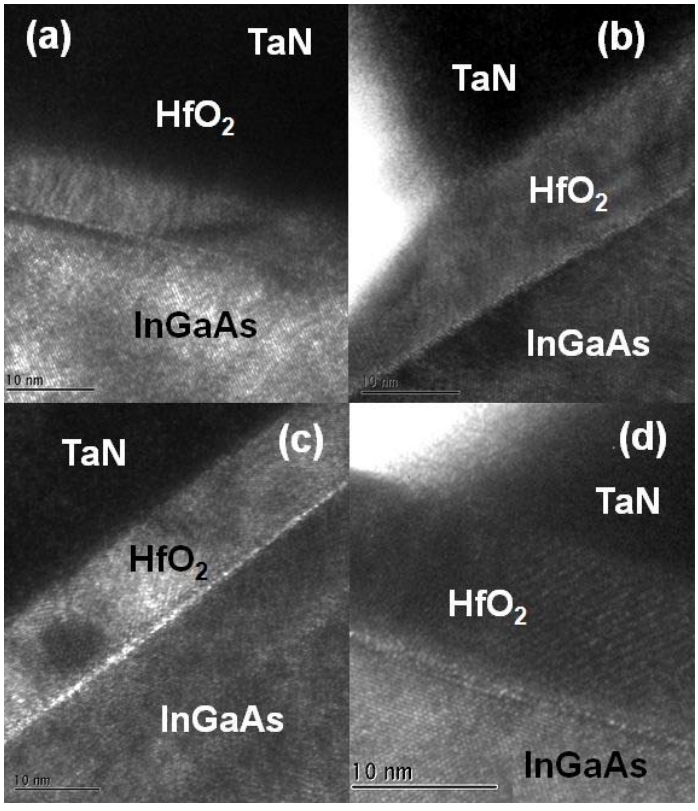


Fig. 4.16 Cross-sectional TEM images of InGaAs/HfO_2/TaN gate stack without P_xN_y passivation layer after anneal at 700 ^oC for 10 sec (a) and with the P_xN_y passivation layer after at 600 ^oC for 1 min (b), at 700 ^oC for 10 s (c), and 750 ^oC for 5 s (d). For substrate, $In_{0.53}Ga_{0.47}As$ is used for (a), (b), and (d) and $In_{0.7}Ga_{0.3}As$ for (c).

Without passivation, the interface of InGaAs/HfO_2 is degraded by 700 °C thermal process showing an unclear interface and some transition regions at the interface (Fig. 4.16a). Contralily, the atomically sharp and smooth interface between HfO_2 and InGaAs is maintained up to 750 °C RTA where the substrate is passivated with P_xN_y layer prior to HfO_2 deposition (Fig. 4.16b-d).

Thermal stability of the high-*k* gate stack on the P_xN_y passivated InGaAs was estimated with electrical properties of the MOSFET devices. Figure 4.17 shows the changes in MOS *C-V* characteristics of the 10 nm thick HfO_2 gate stack by S/D activation at different temperatures. The lower EOT of the passivated sample than directly deposited gate stack implies electrical improvement in the interfacial layer (Fig. 4.17a). Decrease of EOT by S/D activation temperature may be due to the densification of the HfO_2 film done PDA at 400 °C. Figure 4.17b shows V_{FB} changes by 700 °C RTA on the different gate stacks compared to those without the annealing. The V_{FB} changes by thermal process are effectively suppressed to 13-40 % with the P_xN_y passivation compared to the non-passivated HfO_2 gate stack.

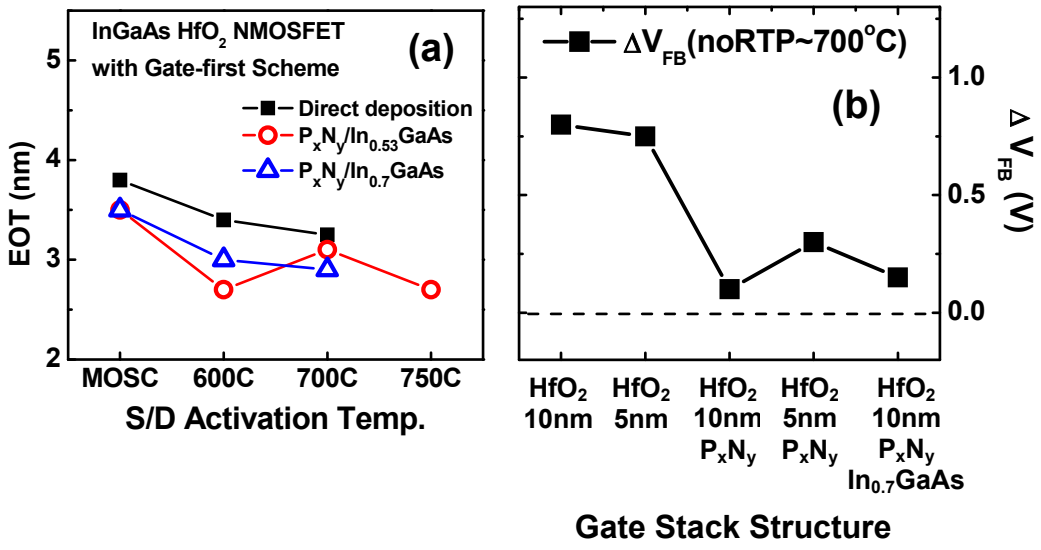


Fig. 4.17 (a) EOT vs. S/D activation temperature for 10 nm thick HfO_2 gate stacks on the InGaAs with and without P_xN_y passivation and (b) changes in V_{FB} by RTA at 700 °C for the MOS devices with different gate stacks on InGaAs.

Figure 4.18 shows that P_xN_y passivated gate stack with 5 nm thick HfO_2 exhibits excellent gate stack leakage behavior up to 700 °C RTA (<10^{-5} A/cm^2), whereas the non-passivated gate stack with the same HfO_2 thickness results in the gate leakage density of ~10 A/cm^2 at the same RTA temperature. The gate leakage density of this work is compared with the previous works from different gate stacks (Fig. 4.18b).

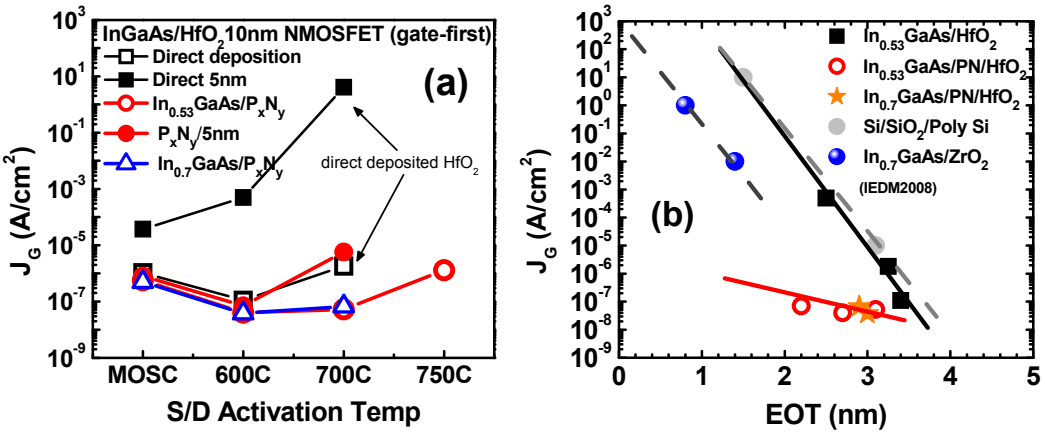


Fig. 4.18 (a) Gate leakage current density, J_G at $|V_{FB}+1V|$ for InGaAs/HfO_2 MOS capacitors with and without P_xN_y passivation as a function of S/D activation temperature and (b) J_G of this work in comparison with the reported results.

Figure 4.19a shows that SS of the MOSFET is degraded with annealing temperature. Nevertheless, the P_xN_y-passivated gate stack exhibits SS ~200 mV/dec after 750 °C RTA. However, the non-passivated MOSFET does not operate well, showing the large data spread even at 700 °C RTA. It may be noteworthy that SS value of the non-passivated MOSFET was ~200 mV/dec for this run, while the SS for the non-passivated sample was ~600 mV/dec in the run fabricated for the study of the P_xN_y passivation in the previous section. However, the P_xN_y-passivated MOSFET devices show SS values similar run to run, at 110-120 mV/dec in a mean value. SS, S in Eq. 1.4 and 1.5 can be rewritten as

$$S = n\frac{k_B T}{q}\ln 10 = 2.3\frac{k_B T}{q}\left(1+\frac{C_d + C_{it}}{C_{ox}}\right) = 2.3\frac{k_B T}{q}\left(1+\frac{\varepsilon_s / x_d + C_{it}}{C_{ox}}\right) \quad (4.5)$$

where k_B is Boltzmann's constant, T is temperature, q is the electronic charge, C_b is the depletion layer capacitance, C_{it} is the trap charge, C_{ox} is the oxide capacitance, ε_s is dielectric constant of the substrate, and x_d is the depletion layer thickness. Thus SS is correlated to the EOT, the substrate doping concentration, and the interface quality of substrate/dielectric. The large run-to-run variation of SS of the non-passivated MOSFET may indicate the unstable substrate/dielectric interface quality as well as the perturbed material property in the channel layer. In contrast, the P_xN_y-passivated InGaAs/HfO_2 gate stack is much less sensitive to the variation in device fabrication processing. This may be due to the stable interface quality of the P_xN_y-passivated InGaAs/HfO_2 gate stack as well as the P-for-As exchanged layer which can inhibit As-related defects in the InGaAs channel. Based on the excellent thermal stability and good interface of $In_{0.53}Ga_{0.47}As$ channel with HfO_2, SS is reduced to below 100mV/dec at the scaled EOT of 2.2 nm where the P_xN_y passivation layer is inserted at the interface (Fig. 4.19b).

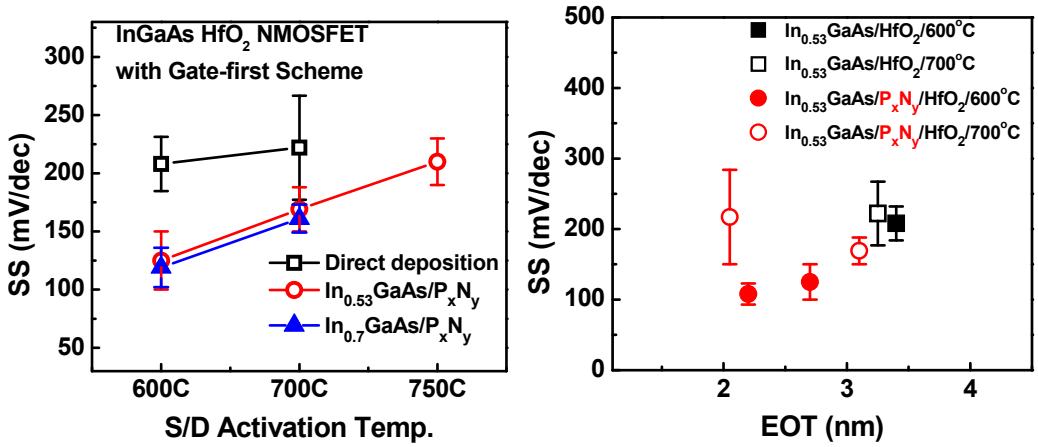


Fig. 4.19 P_xN_y passivation effect on SS of the InGaAs/HfO_2 MOSFETs: (a) SS vs S/D activation temperature where the HfO_2 is 2 nm thick and (b) SS scalability with EOT.

4.4 CONCLUSION

A novel *in situ* passivation process for the integration of an $In_{0.53}Ga_{0.47}As$/high-*k* gate stack using PH_3-N_2 plasma treatment has been studied in a practically wide process window and the effects of the process conditions on the interface quality have been investigated in terms of chemical, physical, and electrical properties. Comparative XPS and AFM studies describe the low pressure PH_3-N_2 plasma treatment of $In_{0.53}Ga_{0.47}As$ involving complex surface reactions between the activated species in PH_3-N_2 plasma and the InGaAs substrate, resulting in a smooth P_xN_y layer as a major product and a P-for-As exchanged layer below the P_xN_y layer. It is found that the P_xN_y passivation inhibits the evolution of undesired As species such as As oxide and free As compared to InGaAs surfaces without passivation or PH_3-based passivation of InGaAs without a P_xN_y layer. The XPS profile reveals the formation of an atomically thin (~ 1 ML) P_xN_y passivation layer on $In_{0.53}Ga_{0.47}As$ regardless of the process conditions for a PH_3-N_2 plasma process window where the temperature ranges from 430 to 550 ^oC, time from 1 to 5 min, and rf plasma power from 200 to 500 W. In addition, it is found that the stoichiometry and density of a 1 ML thick P_xN_y layer and the degree of P-for-As exchange reaction are varied by the conditions.

We have proposed reaction paths suggesting that a nitridation mechanism plays an important role combined with phosphorus incorporation paths based on the results of the self-limiting nature of P_xN_y film growth in the plasma PH_3-N_2/$In_{0.53}Ga_{0.47}As$ system. Considerably improved electrical properties are obtained with a P_xN_y passivation at the interface between HfO_2 and $In_{0.53}Ga_{0.47}As$, demonstrating suppressed frequency dispersion in inversion C-V by more than 80 % compared to the non-passivated sample and low SS values approaching 60 mV/dec.

On the basis of the superiroty of the P_xN_y passivation effect on the InGaAs/high-*k* interface quality, excellent G_m and electron mobility have been demonstrated in a $In_{0.53}Ga_{0.47}As$ surface channel NMOSFET fabricated by the self-aligned gate-first scheme. Thermal stability of the P_xN_y-passivated InGaAs/high-*k* gate stack has been examined up to 750 ^oC S/D activation RTA with the self-aligned gate-first MOSFET fabrication, showing a decent device operation without Fermi level pinning. In contrast, the non-passivated InGaAs NMOSFET shows a significant increase in the gate leakage current after 700 ^oC anneal as well as a degraded SS. TEM study on the InGaAs/HfO_2 interfaces agrees well with the electrical properties that depend on the RTA temperature and the P_xN_y passivation.

Although our preliminary studies exploring the effect of process parameter on P_xN_y passivation of $In_{0.53}Ga_{0.47}As$ in the plasma PH_3-N_2 system cannot provide a quantitative explanation of the effect of process parameters to confirm the proposed kinetics, the present study has demonstrated that the P_xN_y passivation process using PH_3-N_2 plasma is a promising and thermally robust interface engineering technique for a III-V/high-*k* interface for future low-power and high-speed transistors.

References

[1] N. Goel, D. Heh, S. Koveshnikov, I. Ok, S. Oktyabrsky, V. Tokranov, R. Kambhampatic, M. Yakimov, Y. Sun, P. Pianetta, C. K. Gaspe, M. B. Santos, J. Lee, S. Datta, P. Majhi and W. Tsai, "Addressing the gate stack challenge for high mobility $In_xGa_{1-x}As$ channels for NFETs," in *IEDM Tech. Dig*., Dec. 2008, pp. 363-366.

[2] Y. Sun, Edward W. Kiewra, Joel P. de Souza, James J. Bucchignano, Keith E. Fogel, Devendra K. Sadana, Senior Member, IEEE, and Ghavam G. Shahidi, "High-performance $In_{0.7}Ga_{0.3}As$-channel MOSFETs with high-*k* gate dielectrics and α-Si passivation," *IEEE Electron Device Letters,* vol. 30, pp. 5-7, 2009.

[3] Y. Q. Wu, W. K. Wang, O. Koybasi, D. N. Zakharov, E. A. Stach, S. Nakahara, J. C. M. Hwang and P. D. Ye, "0.8-V supply voltage deep-submicrometer inversion-mode $In_{0.75}Ga_{0.25}As$ MOSFET," *IEEE Electron Device Letters,* vol. 30, pp. 700-702, 2009.

[4] J. Q. Lin, S. J. Lee, H. J. Oh, G. Q. Lo, D. L. Kwong, and D. Z. Chi, "Inversion-mode self-aligned $In_{0.53}Ga_{0.47}As$ n-channel metal-oxide-semiconductor field-effect transistor with HfAlO gate dielectric and TaN metal gate," *IEEE Electron Device Lett*., vol. 29, pp. 977-980, 2008.

[5] M. Hong, J. Kwo, T. D. Lin, and M. L. Huang, "InGaAs metal oxide semiconductor devices with $Ga_2O_3(Gd_2O_3)$ high-*k* dielectrics for science and technology beyond Si CMOS," *MRS Bull*., vol. 34, pp. 504-513, 2009.

[6] H. Hasegawa and M. Akazawa, "Surface passivation technology for III-V semiconductor nanoelectronics," *Appl. Surf. Sci.*, vol. 255, pp. 628-632, 2008.

[7] J. Robertson, "Model of interface states at III-V oxide interfaces," *Appl. Phys. Lett*., vol. 94, p. 152104, 2009.

[8] P. T. Chen, Y. Sun, E. Kim, P. C. McIntyre,1 W. Tsai, M. Garner, P. Pianetta,Y. Nishi, and C. O. Chui, "HfO_2 gate dielectric on $(NH_4)_2S$ passivated (100) GaAs grown by atomic layer deposition," *J. Appl. Phys*., vol. 103, p. 34106, 2008.

[9] M. Houssa, G. Pourtois, M. Caymax, M. Meuris, M.M. Heyns, "Electronic properties of (100)Ge/Ge(Hf)O_2 interfaces: A first-principles study," *Surf. Sci*., vol. 602, pp. L25-L28, 2008.

[10] E.A. Chagarov and A.C. Kummel, "*Ab initio* molecular dynamics simulations of properties of *a*-Al_2O_3/vacuum and *a*-ZrO_2/vacuum vs *a*-Al_2O_3/Ge(100)(2×1) and *a*-ZrO_2/Ge(100)(2×1) interfaces," *J. Chem. Phys*., vol. 130, p. 124717, 2009.

[11] H. Hasegawa and T. Sawada, "On the electrical properties of compound semiconductor interfaces in metal/insulator/semiconductor structures and the possible origin of interface states," *Thin Solid Films*, vol. 103, pp. 119-140, 1983.

[12] C. W. Wilmsen Ed., Physics *and Chemistry of III-V Compound Semiconductor Interfaces*, New York: Plenum, 1985.

[13] H. C. Lin, W. -E. Wang, G. Brammertz, M. Meuris, and M. Heyns, "Electrical study of sulfur passivated $In_{0.53}Ga_{0.47}As$ MOS capacitor and transistor with ALD Al_2O_3 as gate insulator," *Microelectronic Engineer.*, vol. 86, pp. 1554-1557, 2009.

[14] S. Oktyabrsky, V. Tokranov, M. Yakimov, R. Moore, S. Koveshnikov, W. Tsai, F. Zhu, and J. C. Lee, "High-k gate stack on GaAs and InGaAs using *in situ* passivation with amorphous silicon," *Mat. Sci. Eng. B,* vol. 135, pp. 272-276, 2006.

[15] F. Zhu, H. Zhao, I. Ok, H. S. Kim, J. Yum, J. C. Lee, N. Goel, W. Tsai, C. K. Gaspe, and M. B. Santos, "Effects of anneal and silicon interface passivation layer thickness on device characteristics of $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistors," *Electrochem. Solid-State Lett*., vol. 12, pp. H131-H134, 2009.

[16] M. Houssa, E. Chagarov, and A. Kummel, "Surface defects and passivation of Ge and III-V interfaces," *MRS Bulletin*, vol. 34, pp. 504-513, 2009

[17] Y. Xuan, Y. Q. Wu, T. Shen, T. Yang, and P. D. Ye, "High performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al_2O_3, HfO_2 and HfAlO as gate dielectrics," in *IEDM Tech. Dig*., Dec. 2007, pp. 637-640.

[18] M. V. Lebedev, T. Mayer, and W. Jaegermann, "Sulfur adsorption at GaAs (100) from solution: role of the solvent in surface chemistry," *Surf. Sci*., vol. 547, pp. 171-183, 2003.

[19] T. Scimeca, Y. Muramatsu, M. Oshima, H. Oigawa, and Y. Nannichi, "Temperature-dependent changes on the sulfur-passivated GaAs (111)A, (100), and (111)B surfaces," *Phys. Rev. B*., vol. 44, pp. 12927-12932, 1991.

[20] K. Shiraishi, Y. Akasaka, N. Umezawa, Y. Nara, K. Yamada, H. Takeuchi, H. Watanabe, T. Chikyow, and T.-J. K. Liu, "Thoery of Fermi level pinning of high-*k* dielectrics," presented at *the 2006 International Conference on Simulation of Semiconductor Process and Devices* (Institute of electrical and Electronics Engineers, Monterey, US), 2006, pp. 306-313.

[21] D. L. Winn, M. J. Hale, T. J. Grassman, A. C. Kummel, R. Droopad, and M. Passlack, " Direct and indirect causes of Fermi level pinning at the SiO/GaAs interface," *J. Chem. Phys*. vol. 126, p. 84703, 2007.

[22] M. Akazawa and H. Hasegawa, "Formation of ultrathin SiN_x/Si interface control double layer on (001) and (111) GaAs surfaces for *ex situ* deposition of high-*k* dielectrics," *J. Vac. Sci. Technol. B*, vol. 25, pp. 1481-1490, 2007.

[23] G. Bruno, "Reactivity and control of III-V surfaces for passivation and Schottky barrier formation," *Appl. Surf. Science,* vol. 235, pp. 239-248, 2004.

[24] S. Pal, S. M. Shivaprasad, Y. Aparna, and B. R. Chakraborty, "Phosphorous passivation of $In_{0.53}Ga_{0.47}As$ using MOVPE and characterization of Au–Ga_2O_3 (Gd_2O_3)–$In_{0.53}Ga_{0.47}As$ MIS capacitor," *Appl. Surf. Sci*., vol. 245, pp. 196-201, 2005.

[25] S. J. Whang, S. J. Lee, G. Fei, N. Wu, C. X. Zhu, J. S. Pan, L. J. Tang, and D. L. Kwong, "Germanium p- & n-MOSFETs fabricated with novel surface passivation (plasma-PH_3 and thin AlN) and TaN/HfO_2 Gate stack," in *IEDM Tech. Dig*., Dec. 2004, pp. 307-310.

[26] T. Sato, I. Mizushima, N. Aoki, and Y. Tsunashima, "Dominant factor for the concentration of phosphorus introduced by vapor phase doping (VPD)," *Jpn. J. Appl. Phys*. Part 1, vol. 37, pp. 1162-1165, 1998.

[27] X. Wallart and C. Priester, "Experimental and theoretical investigation of $Ga_{1-x}In_xAs$ surface reactivity to phosphorus," *Phys. Rev. B*, vol. 68, p. 235314, 2003.

[28] A. S. Brown, M. Losurdo, P. Capezzuto, G. Bruno, T. Brown, and G. May, "Fundamental reactions controlling anion exchange during mixed anion heterojunction formation: Chemistry and kinetics of P-for-As exchange reaction," *J. Appl. Phys.,* vol. 99, pp. 093510-9, 2006.

[29] M. Losurdo, P. Capezzuto, G. Bruno, G. Leo, and E. A. Irene, "III-V surface plasma nitridation: A challenge for III-V nitride epigrowth," *J. Vac. Sci. Technol. A.,* vol. 17, pp. 2194-2201, 1999.

[30] Z. Meng, Y. Peng, Z. Yang, and Y. Qian, "Synthesis and characterization of amorphous phosphorus nitride," *Chem. Lett*. vol. 29. pp.1252-1253, 2000.

[31] Y.-H. Jeong, J.-H. Lee, Y.-H. Bae, and Y.-T. Hong, "Composition of phosphorus-nitride film deposited on InP surfaces by a photochemical vapor deposition technique and electrical properties of the interface," *Appl. Phys. Lett*. vol. 57, pp. 2680-2682, 1990.

[32] S. Vepřek, Z. Iqbal, J. Brunner, and M. Schärli, "Preparation and properties of amorphous phosphorus nitride prepared in a low-pressure plasma," *Philos. Mag. B*, vol. 43, pp. 527-547, 1981.

[33] W. Schnick, "Solid-state chemistry with nonmetal nitrides," *Ang. Chem. Int. Ed. Engl.* vol. 32, pp. 806-818, 1993.

[34] M. Losurdo, P. Capezzuto, G. Bruno, and E. A. Irene, "Chemistry and kinetics of the GaN formation by plasma nitridation of GaAs: An *in situ* real-time ellipsometric study," *Phys. Rev. B*, vol. 58, pp. 15878-15888, 1998.

[35] G. Bruno, M. Losurdo, and P. Capezzuto, "Study of the phosphine plasma decomposition and its formation by ablation of red phosphorus in hydrogen plasma," *J. Vac. Sci. Technol A*, vol. 13, pp. 349-358, 1995.

[36] Y. Sun, P. Pianetta, P.-T. Chen, M. Kobayashi, Y. Nishi, N. Goel, M. Garner, and W. Tsai, "Arsenic-dominated chemistry in the acid cleaning of InGaAs and InAlAs surfaces," *Appl. Phys. Lett*. vol. 93, p. 194103, 2008.

[37] B. V. Crist Ed., *Handbook of monochromatic XPS spectra*, New York:Wiley, 2000.

[38] R. J. Hussey, G. I. Sproule, J. P. McCaffrey, and M. J. Graham, "Characterization of oxides formed on InP, InGaAs, InAlAs, and InGaAs/InAlAs heterostructures at 300–500°C," *Oxid. Met*. vol. 57, pp. 427-447, 2002.

[39] Y. Bu, L. Ma, and M. C. Lin, "Laser-assisted chemical vapor deposition of InN on Si(100)," *J. Vac. Sci. Technol. A*, vol. 11, pp. 2931-2937, 1993.

[40] H.-L. Lu, L. Sun, S.-J. Ding, M. Xu, D. W. Zhang, and L.-K. Wang, "Characterization of atomic-layer-deposited Al_2O_3/GaAs interface improved by NH_3 plasma pretreatment," *Appl. Phys. Lett*. vol. 89, p. 152910, 2006.

[41] D. Briggs and M. P. Seah, *Practical surface analysis*, 2 ed. Chichester:John Wiley & Sons, 1990.

[42] P. J. Cumpson and M. P. Seah, "Elastic scattering corrections in AES and XPS. II. Estimating attenuation lengths and conditions required for their valid use in overlayer/substrate experiments," *Surf. Interface Anal*. vol. 25, pp. 430-446, 1997.

[43] J. L. Bischoff, F. Lutz, D. Bolmont, and L. Kubler, "Use of multilayer techniques for XPS identification of various nitrogen environments in the Si/NH_3 system," *Surf. Sci*. vol. 251-252, pp. 170-174, 1991.

[44] W. Schnick and J. Lücke, "Darstellung, kristallstruktur und IR-spektroskopische untersuchung von phosphor(V)-nitrid-imid, HPN_2," *Z. Anorg. Allg. Chem*. vol. 610, pp. 121-126, 1992.

[45] D. R. Lide Ed., *CRC Handbook of Chemistry and Physics* 90th ed. Cleveland :CRC Press, 2010.

[46] M. Akazawa and H. Hasegawa, "Admittance study of GaAs high-*k* metal-insulator-semiconductor capacitors with Si interface control layer," *J. Vac. Sci. Technol. B,* vol. 26, pp. 1569-1578, 2008

[47] T. Haimoto, T. Hoshii, S. Nakagawa, M. Takenaka, and S. Takagi, "Fabrication and characterization of metal-insulator-semiconductor structures by direct nitridation of InP surfaces," *Appl. Phys. Lett*., vol. 96, p. 12107, 2010.

[48] S. A. Suleiman, H. J. Oh, A. Du, C. M. Ng and S. J. Lee, "Study on thermal stability of plasma-PH_3 passivated $HfAlO/In_{0.53}Ga_{0.47}As$ gate stack for advanced metal-oxide-semiconductor field-effect transistor," *Electrochem. Solid-State Lett*. vol. 13, pp. H336-H338, 2010.

[49] M. Levinshtein, S. Rumyantsev, and M. Shur Ed., *Handbook series on semiconductor parameters*, Singapore:World Scientific, 1996.

[50] W. A. Hill and C. C. Coleman, "A single frequency approximation for interface state density determination," *Solid-State Electron.* vol. 23, pp. 987-993, 1980.

[51] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*, New York:Wiley, 1982.

[52] I. G. Thayne, R. J. W. Hill, D. A. J. Moran, K. Kalna, A. Asenov, and M. Passlack, "Comments on "High performance inversion-type enhancement-mode InGaAs MOSFET with maximum drain current exceeding 1 A/mm"," *IEEE Electron Device Lett*., vol. 29, pp. 1085-1086, 2008.

CHAPTER 5

CONCLUSIONS AND FUTURE RESEARCHES

5.1 CONCLUSION

The object of this thesis is to explore new materials and process techniques to develop the high mobility channel layer formation technology for high-speed CMOS devices, especially for NMOSFET on a III-V channel layer. In order to be viable in 10 nm technology node and beyond, the high mobility III-V NMOSFET fabrication approaches should include the substrate engineering for non-planar III-V device structures on Si platform and the III-V/high-*k* interface engineering for thermodynamically stable gate stacks without Fermi level pinning, as well as the compatibility with the cost-effective Si-based MOSFET technology.

The feasibility of GaAs channel NMOSFET on Si platform was explored with the framework of SOI structure and SiGe virtual substrate to overcome the large lattice mismatch (~4 %) between GaAs and Si. The heteroepitaxial growth technique for GaAs-OI on Si substrate via a compositionally graded SGOI platform was proposed and developed using XPS, SIMS, AFM and TEM analyses. It was found that a high Ge concentration in the SiGe buffer layer where GaAs nucleates to grow and a small thickness of SGOI virtual substrate play important roles to form homogeneous nucleation and to relax the strain built up during the initial growth of GaAs, leading to a good alignment of GaAs on the SGOI substrate. Modified two-step Ge condensation

method was developed to fabricate the graded SGOI with Ge fraction as high as 71% on top of the surface in a simple oxidation process, with an excellent crystalline quality. Adopting MEE nucleation at 400 ^{o}C and low-temperature MBE growth at 480 ^{o}C, a continuous GaAs epilayer was realized with much suppressed dislocation defects on a Si wafer via the graded SGOI structure. The well aligned heteroepitaxial GaAs lattice to the graded SGOI layer with the lattice constant of 5.63 Å may indicate almost relaxed GaAs structure. The device quality GaAs-OI on a Si wafer has been realized for the first time. A significant contribution of this work is that the compositionally graded SGOI platform can be a promising feature of substrate engineering that enable co-integration of GOI PMOS and GaAs-OI NMOS for future carrier-transport enhanced CMOS technology. In addition, this platform is fully compatible with the present manufacturable technology with the cost-effective process conditions as well.

In order to realize the high electron mobility NMOSFET with unpinned Fermi level, the GaAs-based III-V/Hf-based MOCVD high-*k* gate stack formation processes were examined and optimized on the basis of development of the III-V/high-*k* interface engineering techniques. The MOSFET fabrication processes, including the pre-gate dielectric cleaning, the high-*k* MOCVD, and the Si n^{+} S/D formation process steps, were examined and optimized first. The XPS study showed that the improved GaAs/high-*k* interfaces with suppressed As oxide were observed at 400 ^{o}C for HfO_2 and at 450 ^{o}C for HfAlO MOCVD, respectively, compared to the lower deposition temperatures. Thermal decomposition of As oxide may play an important role in the temperature dependence as well as chemical reactions between the metal precursor and GaAs surface covered with native oxides. The selective reduction of As^{5+} states in the GaAs/native oxide/HfAlO system revealed that the self-cleaning effect on the GaAs native oxide removal during HfAlO CVD, where the HA-2 precursor is used, for the

first time. Much improved electrical properties were obtained where HF chemical cleaning and $(NH_4)_2S$ chemical treatment are applied sequencially before the high-*k* deposition. With the evaluation of R_{sh} using the four-point-probe measurement and the junction characteristics between the n^+ S/D contact and back contact, the S/D formation condition was determined to the Si dose of 1×10^{14} cm^{-2} and the S/D activation at 750 ^oC RTA for 1 min to fabricate GaAs NMOSFET. It was found that $In_{0.53}Ga_{0.47}As$ substrate is easier to form an inversion layer on the surface than GaAs, showing much improved chemical and electrical properties of the III-V/high-*k* interfaces. In addition, Si dopant activation can be achieved at 600 ^oC RTA for n^+ S/D in the InGaAs substrate.

It has been demonstrated that the alloying of InAs with GaAs ($In_{0.53}Ga_{0.47}As$) and the alloying of HfO_2 with Al_2O_3 (HfAlO) can significantly reduce native oxides formation at p-GaAs/HfO_2 interface using XPS. The band offsets for the GaAs-based III-V/Hf-based high-*k* systems were obtained by XPS also, showing that the electron barrier heights are over 1 eV for all the cases and higher for HfAlO dielectric than HfO_2 and higher for $In_{0.53}Ga_{0.47}As$ substrate then GaAs. The electrical characteristics of MOS capacitors with the combination of the chemical treatment and HfAlO dielectrics on $In_{0.53}Ga_{0.47}As$ further substantiate the material characteristics.

Based on the study of interfacial properties and the process optimizations using electrical characteristics, we successfully demonstrated the E-mode NMOSFET of $In_{0.53}Ga_{0.47}As$ channel integrated with CVD HfAlO gate dielectric and TaN metal gate using a self-aligned fabrication scheme. Well behaved I_D-V_D and I_D-V_G curves were obtained with a sharp transition in inversion *C*-*V* characteristics, indicating unpinned Fermi level on the InGaAs/HfAlO interface. Peak electron mobility at low gate bias of

1560 cm^2/Vs was reported and this is ~ 2 times higher than even the mobility-enhanced strained Si NMOSFET [1] .

To improve the $In_{0.53}Ga_{0.47}As$ NMOSFET device performance, a passivation technique using *in situ* PH_3-based treatment has been proposed, explored and investigated for the InGaAs NMOSFET integrated with high-*k*/metal gate stack with the material and electrical characterizations. Comparative XPS and AFM studies revealed that the low pressure PH_3-N_2 plasma treatment of $In_{0.53}Ga_{0.47}As$ results in a smooth 1 ML thick P_xN_y layer as a major product and a P-for-As exchanged layer below the P_xN_y layer in a wide range of process window. The detailed XPS analysis with quantification also showed that the P_xN_y passivation inhibits the evolution of undesired As species such as As oxide and free As compared to InGaAs surfaces without passivation or PH_3-based passivation of InGaAs without a P_xN_y layer. We have proposed reaction paths suggesting that a nitridation mechanism plays an important role combined with phosphorus incorporation reactions based on the result of the self-limiting nature of P_xN_y film growth in the plasma PH_3-N_2/$In_{0.53}Ga_{0.47}As$ system.

With the P_xN_y passivation at the interface between HfO_2 and $In_{0.53}Ga_{0.47}As$, remarkably improved electrical properties were obtained, demonstrating the frequency dispersion reduction by more than 80 % compared to the non-passivated device and low SS approaching 60 mV/dec. As a result, by adopting the P_xN_y passivation into the gate stack, we have demonstrated $In_{0.53}Ga_{0.47}As$ NMOSFET with an electron mobility as high as 2557 cm^2/Vs, which is equivalent to the mobility enhancement factor of ~5 compared to the Si universal mobility. This higher channel mobility with an enhancement factor of more than 4 can relieve the other tough requirements such as I_{on}, EOT and I_{off} for further scaling regime where there is no certain solution with Si so far. In addition, the thermal stability of the $In_{0.53}Ga_{0.47}As/HfO_2$ gate stack was improved up

to 750 ^{o}C with the P_xN_y passivation on the InGaAs surface compared to the non-passivated sample.

5.2 SUGGESTIONS FOR FUTURE RESEARCHES

This thesis focuses on developing high electron mobility channel layer foramation technology as one of the technical solutions for the CMOS scaling beyond the 10 nm node. The present study shows that the developed graded SGOI structure with the cost-effectve Ge-condensation method and the novel P_xN_y passivation technique using PH_3-N_2 plasma are promising techniques for substrate and interface engineering for the deeply scaled non-planar CMOS integrated with high mobility channels of Ge and InGaAs. However, this vison should be demonstrated with more improved performance and further examined to understand the underlying chemistry and physics. Some of the suggestions for future researches in the field of the advanced InGaAs channel engineering are highlighted in this section.

(*i*) S/D Contact Engineering for III-V Devices

To further improve the InGaAs NMOSFET performance, reduction in S/D parasitic resistance is required. As seen in the low slope of I_D-V_D curves (Fig. 3.25 and 4.10), the drain current is considerably limited by the external resistance. Metal S/D contact technologies can be developed with spacer techniques to reduce the S/D parasitic resistance. The use of the PH_3-based passivation technique investigated in this thesis could provide insights to develop the alloyed contacts because the passivation may inhibit evolution of As_{Ga} sites by supplying group V elements. In addition, the concept of passivation developed in the preceding chapters of this dissertation could alleviate Fermi level pinning at the interface of III-V/metal contact [2,3].

(*ii*) Reliability Study of the Interface Engineered InGaAs MOSFET

Reliability is a critical aspect of process integration once the integration successfully demonstrates the electronic device operation with an acceptable electrical performance. The reliability of the III-V MOSFET should thus be examined with the interface engineering technique developed in the preceding chapter of this thesis. To accomplish this objective, adquate electrical reliability models and measurement tools should be developed for the III-V MOSFET devices as well. So far, a few reports are available in the literature on the reliability issues of III-V MOS devices [4].

As preliminarily seen in the statistical variations of the device performance depending on the P_xN_y passivation conditions in this dissertation, the interface quality could be differenciated further by sophisticated electrical characterizations with the effect of stress on the devices. Or, inversely, the device failure model can be studied with the controlled material properties at the InGaAs/high-*k* interface such as phosphorus concentration in the P-for-As exchanged layer, nitrogen concentration in the P_xN_y passivation layer, and the thickness of the P-for-As exchanged layer.

(*iii*) MOSFET Structure Engineering for III-V Non-planar Devices

As reviewed in Chapter. 1, the future CMOS device structure will be non-planar and multiple-gate structures to control SCE. Although III-V high mobility channel technology can relieve the relentless requirements in the Si-based CMOS scaling and extend the scaling beyond 10 nm node, the non-planar MOSFET structure would be eventually adopted into the carrier-transport enhanced channel platform. Identifying the challenges in the III-V non-planar structure realization and developing the 3D etching technology are required.

Recently, the first demonstration of InGaAs FinFET has been reported by P. D. Ye group in Purdue university, showing the better SCE compared to the corresponding

planar MOSFET [5]. The developed GaAs-OI structure through the graded SGOI virtual substrate could provide a novel platform to engineer device structures. For example, a GaAs nanowire MOSFET can be fabricated by a selective etching of the underlying SiGe layer after the gate defining on GaAs-OI substrate.

References

[1] P. R. Chidambaram, C. Bowen, S. Chakravarthi, C. Machala, and R. Wise, "Fundamentals of silicon material properties for successful exploitation of strain engineering in modern CMOS manufacturing," *IEEE Trans. Electron Devices*, vol. 53, pp. 944-964, 2006.

[2] N.Newman, W. E. Spicer, T. Kendelewicz, and I. Lindau, "On the Fermi level pinning behavior of metal/III-V semiconductor interfaces," *J. Vac. Sci. Technol. B*, vol. 4, pp. 931-938, 1986.

[3] R. L. Van Meirhaeghe, W. H. Laflere, and F. Cardon, "Influence of defect passivation by hydrogen on the Schottky barrier height of GaAs and InP contacts," *J. Appl. Phys*., vol. 76, pp. 403-406, 1994.

[4] T. Das, C. Mahata, G. K Dalapati, D. Chi, G. Sutradhar, P. K. Bose, and C. K. Maiti, "Reliability and breakdown characteristics of HfO_2-based GaAs metal-oxide-semiconductor capacitors with a thin Si interface layer," presented at *17th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2010, pp.1-4.

[5] Y.Q. Wu, R.S. Wang, T. Shen, J.J. Gu, and P. D. Ye, "First experimental demonstration of 100 nm inversion-mode InGaAs FinFET through damage-free sidewall etching," in *IEDM Tech. Dig*., Dec. 2009, pp. 331-334.

APPENDIX

LIST OF PUBLICATIONS

Journal Publications

[1] **H. J. Oh**, S. A. Suleiman, and S. J. Lee, "Interface engineering for InGaAs n-MOSFET application using plasma PH_3-N_2 passivation," *J. Electrochem. Soc*., vol. 157, pp. H1051-H1060, 2010.

[2] S. A. Suleiman, **H. J. Oh**, A. Du, C. M. Ng, and S. J. Lee, "Study on Thermal Stability of Plasma-PH_3 Passivated HfAlO/$In_{0.53}Ga_{0.47}As$ Gate Stack for Advanced Metal-Oxide-Semiconductor Field Effect Transistor," Electrochem. Solid-State Lett. vol. 13, pp. H336-H338, 2010.

[3] **H. J. Oh**, J. Q. Lin, S. J. Lee, G. K. Dalapati, A. Sridhara, D. Z. Chi, S. J. Chua, G. Q. Lo, and D. L. Kwong, "Study on interfacial properties of InGaAs and GaAs integrated with chemical-vapor-deposited high-k gate dielectrics using x-ray photoelectron spectroscopy," *Appl. Phys. Lett*., vol. 93, p. 62107, 2008

[4] G. K. Dalapati, **H. J. Oh**, S. J. Lee, A. Sridhara, A. S. W. Wang, and D. Chi, "Energy-band alignments of HfO_2 on p-GaAs substrates," *Appl. Phys. Lett*., vol. 92, p.42120, 2008.

[5] J. Q. Lin, S. J. Lee, **H. J. Oh**, G. Q. Lo, D. L. Kwong, and D. Z. Chi, "Inversion-mode self-aligned $In_{0.53}Ga_{0.47}As$ n-channel metal-oxide-semiconductor field-effect transistor with HfAlO gate dielectric and TaN metal gate," *IEEE Electron Device Lett*., vol. 29, pp. 977-980, 2008.

[6] W. Y. Loh, H. Zang, **H. J. Oh**, K. J. Choi, H. S. Nguyen, G. Q. Lo, and B. J. Cho, "Strained Si/SiGe channel with buried $Si_{0.99}C_{0.01}$ for improved drivability, gate stack integrity and noise performance," *IEEE Transactions on electron Devices*, vol. 54, No. 12, pp. 3292-3298, 2007.

[7] **H. J. Oh**, K. J. Choi, W. Y. Loh, T. Htoo, S. J. Chua, and B. J. Cho, "Integration of GaAs epitaxial layer to Si-based substrate using Ge condensation and low-temperature migration enhanced epitaxy techniques", *J. Appl. Phys*., vol. 102, p. 54306, 2007.

Conference Publications

[1] **H. J. Oh**, A. B. Sumarlina, and Sungjoo Lee, "High-k integration and interface engineering for III-V MOSFETs," in *The 219th Electrochemical Society Meeting*, *ECS Trans.*, vol. 35, May 2011, pp. 481-495.

[2] **H. J. Oh**, J. Q. Lin, S. A. B. Suleiman, G. Q. Lo, D. L. Kwong, D. Z. Chi, and S. J. Lee, "Thermally robust phosphorous nitride interface passivation for InGaAs self-aligned gate-first n-MOSFET integrated with high-*k* dielectric," in *IEDM Tech. Dig*., Dec. 2009, pp.339-342.

[3] J. Q. Lin, S. J. Lee, **H. J. Oh**, W. F. Yang, D. Z. Chi, G. Q. Lo, and D. L. Kwong, "Plasma PH_3-passivated high mobility inversion InGaAs MOSFET fabricated with self-aligned gate first process and HfO_2/TaN gate stack," in *IEDM Tech. Dig*., Dec. 2008, pp. 401-404.

[4] J. Lin, S. J. Lee, **H. J. Oh**, G. K. Dalapati, D. Z. Chi, G. Q. Lo, and D. L. Kwong, "Enhancement-mode $In_{0.53}Ga_{0.47}As$ n-MOSFET with self-aligned gate-first process and CVD HfAlO gate dielectric," in *Solid State Devices and Materials Conf. Ext. Abst.*, Sep. 2008, pp. 30-31.

[5] G. K. Dalapati, **H. J. Oh**, S. J. Lee, A. Sridhara, A. S. W. Wong, C. K. Chia, and D. Z. Chi, "Interfacial characteristics and band alignments for high-k gate dielectrics on p-GaAs substrate," *3rd MRS-S Conference on Advanced Materials*, Apr. 2008.

[6] H. Zang, W. Y. Loh, **H. J. Oh**, K. J. Choi, H. S. Nguyen, G. Q. Lo, and B. J. Cho, "Improved current drivability and gate stack integrity using buried SiC layer for strained Si/SiGe channel devices," in *The 211th Electrochemical Society Meeting*, *ECS Trans.*, vol. 6, May 2007, pp.105-110.

[7] Y. Tong, G. K. Dalapati, **H. J. Oh**, and B. J. Cho, "The effect of interfacial layer of high-*k* dielectrics on GaAs substrate," in *The 211th Electrochemical Society Meeting*, *ECS Trans.*, vol. 6, May 2007, pp.331-335.

[8] **H. J. Oh**, K. J. Choi, W. Y. Loh, T. Htoo, S. J. Chua, and B. J. Cho, "GaAs heteroepitaxy on SiGe-on-insulator using Ge condensation and migration enhanced epitaxy," in *The 211th Electrochemical Society Meeting*, *ECS Trans.*, vol. 6, May 2007, pp. 95-98.