TOP-DOWN ENGINEERED SILICON AND GERMANIUM NANOWIRE MOSFET

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2010

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B.Eng. (National University of Singapore) 2006

A THESIS SUBMITTED
FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

DEPARTMENT OF
ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE
2010

Acknowledgements

I would like to thank everyone that contributed in various ways to this thesis. First and foremost, I would like to take this opportunity to express my sincere gratitude to my advisors, Prof. Lee Sungjoo and Dr. Lo Guoqiang, Patrick for their invaluable guidance and encouragement throughout my 4 years' Ph.D. study at National University of Singapore. Without their help, I would not be able to overcome all those difficulties and walk all the way to here to write this thesis. I am greatly thankful to Prof. Lee for his kindness and patience in helping me on my research. Prof. Lee is an experienced advisor who could always point out the fundamental issues directly and gave practical suggestions on my research work. Moreover, he is also a kind elder who is patient and careful on helping me on my mistakes. I also truly appreciate the helpful guidance and support from Dr. Lo. I would like to thank Dr. Lo for providing me the opportunity to join the Institute of Microelectronics (IME), Singapore for my Ph.D research work, where I continuously get support from him on various matters. My appreciation also goes to Dr. Navab Singh from the Institute of Microelectronics, Singapore, for his valuable advice and technical discussions. Without his expertise and advice in semiconductor technology, I would not be able to undertake all my projects smoothly.

I would also like to express my deepest appreciation to Dr. Lap Chan and Dr. Ng Chee Mang for their supports and knowledge sharing. I like the Wednesday session and absorbed a lot of nutriment, technique and non-technique knowledge, from the interaction with them and the rest of the Special Group students.

I would also like to thank Dr. Yu Ming-Bin, Dr. Wei Yip Lo, Dr. Zhu Si Yang, for their assistance and discussion to conduct my process in the clean room. I benefited greatly through interactions with them. I would like to thank all the technical staff in Semiconductor Process Technology department, especially Mr. Deng Wei, for their kindness and help on my research works.

Special thanks also go to my seniors in Silicon Nano Device Lab (SNDL), National University of Singapore, especially Dr. Zang Hui, Dr. Jiang Yu, Dr. Fu Jia, Dr. Zhao Hui, Dr. Yang Weifeng, Dr. He Wei, Dr. Yang Jianjun, Dr. Gao Fei, Dr. Ren Chi, Dr. Tan Kian Ming, Dr. Shen Chen et al. for their assistance on many of my technical problems encountered during my graduate study. To my research buddies, Chin Yoke King, Wang Jian, Xie Ruilong, Lim Shiya, Phyllis, Li Yida, Sun Yuan, Lu Weijie et al., I would like to say that my research life would be much tougher without their help and discussion.

Last but not least, my thanks go to my parents for their supports and encouragements during my doctorial studying.

Abstract

A large part of the success of integrated circuits could be attributed to the continuous scaling of metal-oxide-semiconductor-field effect-transistors (MOSFETs), which lead to faster and cheaper transistors simultaneously. However, as the transistor dimensions shrink down to the sub-100 nm regime, it has become challenging to continuously improve transistors' performance by conventional scaling techniques. It is found that on-state current, power consumption and short channel effects have a tradeoff relationship with each others. As a result, any technique to improve transistor performance needs to overcome/mitigate the stringent constrains of this tradeoff.

The nanowire transistor architecture and germanium (Ge) channel are considered to be promising performance boosters to improve transistor performance which can effectively overcome/mitigate the tradeoff between on-state current, power consumption and short channel effects. In this thesis, nanowire gate-all-around (GAA) Schottky Barrier (SB)-MOSFETs and Ge nanowire transistors are studied as potential candidates for future high performance transistor applications.

Nanowire GAA MOSFETs integrated with 1-D NiSi Schottky source/drain (S/D) were explored and demonstrated on silicon (Si) nanowires with diameter down to 4 nm. Although NiSi has a high hole SB height of 0.46 eV, the Si nanowire SB-MOSFET still demonstrated a high on-state current and a subthreshold swing (SS) close to the ideal value 60 mV/dec. The performance improvement was attributed to the improved carrier injection as a result of the superior gate electrostatic control over the channel in the GAA nanowire device architecture.

As a potential performance booster, Ge nanowire transistors were explored. Ge nanowires (NWs) were fabricated on an epitaxial grown Ge layer by a novel technique of two-step etching with polymerization in between. Ge-nanowires (GeNWs) with diameter down to 14 nm were integrated with the TaN/High-k gate stack to form Ge nanowire pMOSFETs. The on/off ratio as high as 6 orders at -1.2 V V_{DS} was achieved on the 14 nm diameter Ge nanowire transistor. However, hole field effect mobility was low due to the surface roughness scattering and the Coulomb scattering caused by the heavy interface state trap density. To improve the GeNW surface topology, Epitaxial-Si over GeNW was employed. The Ge/Si core/shell nanowires were integrated with the TaN/HfO_2 gate stack to form GAA GeNW pMOSFETs. With the introduction of the Si epitaxial shell, the Ge nanowire transistor performance was significantly improved. A 200 nm gate length Ge/Si core/shell nanowire GAA pMOSFET demonstrated high on-state current of 150 μA/μm, a peak field effect mobility of 254 cm^2/V-s, and a backscattering coefficient of 0.31.

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List of Symbols

Symbol	Description	Unit
C	Capacitance	$fF/\mu m^2$
C_{ox}	Capacitance of gate oxide	$fF/\mu m^2$
ξ	Scaling factor	
P	Power consumption	W
X_j	S/D junction depth	nm
N_{sub}	Substrate doping	$/cm^3$
I_G	Gate leakage current	A
K	Gate dielectric constant	
E_G	Semiconductor bandgap	eV
E_C	Si conduction band-edge	eV
E_F	Fermi-level energy	eV
E_v	Si valence band-edge	eV
G_m	Transconductance	S
I_{Dsat}	Drain saturation current (per unit width)	A/μm
I_{off}	Off state current (per unit width)	A/μm
I_{on}	On state current (per unit width)	A/μm
I_D	Transistor drive current	A
μ_{eff}	Effective mobility	$cm^2/V\text{-}s$
μ_{FE}	Field effective mobility	$cm^2/V\text{-}s$
N_A	Substrate doping concentration atoms	$/cm^3$
τ	Intrinsic gate delay	s
V_{DS}	Drain voltage	V
V_{GS}	Gate voltage	V
V_{DD}	Supply Voltage	V
V_T	Threshold voltage	V
$V_{T,lin}$	Linear threshold voltage (Extracted in linear regime at low V_{DS})	V
L_G	Gate length	nm
q	Electronic charge	C
T_{ox}	Equivalent oxide thickness	nm
W	Transistor gate width	μm
ε_{Si}	Permittivity of silicon	F/cm^2
ε_{SiO2}	Permittivity of silicon oxide	F/cm^2
Φ_{bn}	Schottky barrier height for electrons	eV
Φ_{bp}	Schottky barrier height for holes	eV
V_{bi}	Built-in potential in Schottky diode	eV
V_F	Forward bias voltage	V
T	Temperature	K
R_c	Backscattering coefficient	

List of Abbreviations

AFM	Atomic force microscopy
ALD	Atomic layer deposition
BOX	Buried oxide
CMOS	Complimentary-Metal-Oxide-Semiconductor
CVD	Chemical vapor deposition
CET	Capacitance equivalent thickness
C-V	Capacitance-Voltage
CD	Critical dimensions
DG	Double-Gate
DHF	Diluted Hydrofluoric (acid)
DIBL	Drain induced barrier-Lowering
EDX	Energy dispersive X-ray
EELS	Electron energy loss spectroscopy
EOT	Equivalent oxide thickness
GAA	Gate-All-Around
Ge	Germanium
GIDL	Gate induced drain leakage
GOI	Germanium-On-Insulator
HK	high-κ (dielectric)
HM	Hard mask
HRTEM	High resolution transmission electron microscopy
ITRS	international technology roadmap for semiconductors
ICs	Integrated Circuits
I-V	Current-Voltage
LPCVD	Low pressure chemical vapor deposition
MG	Metal-Gate
MOSFET	Metal-Oxide-Semiconductor-Field-Effect-Transistor
NW	Nanowire
PDA	Post deposition annealing
PMD	Post metal dielectric
PR	Photoresist
PVD	Physical vapor deposition
PECVD	Plasma enhanced chemical vapor deposition
RF	Radio frequency
RMS	Root mean square
RTA	Rapid thermal annealing
RIE	Reactive ion etching
SBH	Schottky barrier height
SB-MOSFET	Schottky barrier MOSFET
SC-1	Standard cleaning-1 ($NH_4OH + H_2O_2 + H_2O$) solution
Si	Silicon
SS	Subthreshold swing
SCE	Short channel effects
S/D	Source/drain

SEM	Scanning electron microscopy
STEM	Scanning transmission electron microscopy
SOI	Silicon-On-Insulator
SG-NW	SiGe nanowire
TEM	Transmission electron microscopy
UHV	Ultra high vacuum
UTB	Ultra thin body
UTB-SOI	Ultra thin body Silicon-On-Insulator
VLS	Vapor liquid solid
XTEM	Cross-sectional transmission electron microscope

Chapter 1
Introduction

Nowadays, integrated chips (ICs) have been widely used and become a critical component in almost every aspects of our daily life. ICs mainly consist of planar silicon (Si) Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs) and the performance of the individual MOSFET is a key factor of the whole circuits' performance. Thus, intensive studies have been carried out to improve MOSFET performance ever since its invention in the early 1960s. This chapter will discuss various approaches to improve MOSFET performance and their challenges. At the end, it is the thesis organization.

1.1 Approaches to improve MOSFET performance

The schematic of an nMOSFET is shown in Fig. 1.1 (a). A MOSFET is an electrical switch and the current flowing between the two terminals of source & drain (S/D) is controlled by the electric field from the third terminal of gate (G). There are two operating modes of a transistor. One is the off-state at which its gate bias is the same as its source bias. At off-state mode, there is no current flow between the S/D. The other mode is on-state at which its gate bias is the same as its drain bias. At on-state mode, a thin layer of inversion charge below the gate electrode is formed by the electrical field from the gate electrode. This layer of charges connects the S/D and let the current flows between them. Fig. 1.1 (b)

shows a typical inverter circuit. If the input voltage (V_{IN}) is initially zero at ground voltage, nMOSFET is at off-state and pMOSFET is at on-state. In this case, the loading capacitor (C_{LOAD}) is charged and the output voltage (V_{OUT}) is at supply voltage (V_{DD}). When V_{IN} is switched from zero to supply voltage V_{DD}, nMOSFET turns to on-state and pMOSFET turns to off-state. In this case, C_{LOAD} is discharged through the nMOSFET. In this discharging process, V_{OUT} switches from V_{DD} to zero in response to the switching of V_{IN} from zero to V_{DD}. The responding speed of this circuit is determined by the on-state current of nMOSFET and the amount of charge stored in the loading capacitor C_{LOAD}. Similarly, the capacitor is charged through the pMOSFET when V_{IN} switches from V_{DD} to zero, and the responding speed of this circuit is determined by the on-state current of pMOSFET and the amount of charge stored in C_{LOAD}.

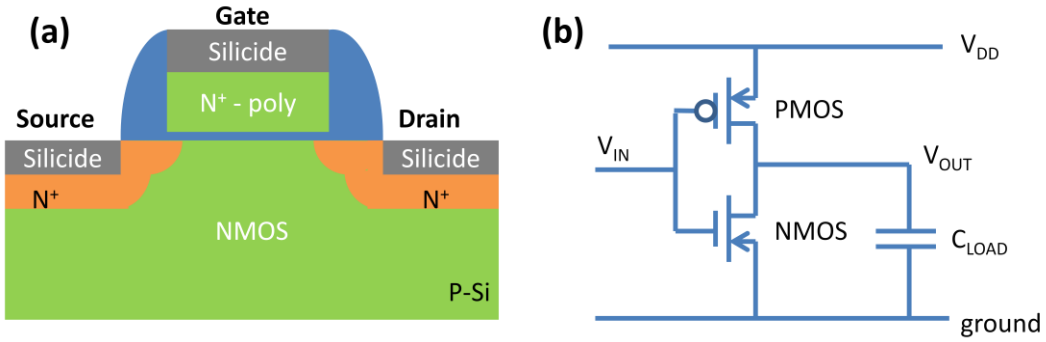


Figure 1.1: (a) Schematic of a conventional planar NMOS cross-sectional image and (b) a typical inverter circuit consisting of one NMOS and one PMOS.

As discussed above, the switching speed of the inverter circuit is determined by the on-state current of the transistors and the loading capacitor $C_{LOAD.}$ In real applications, C_{LOAD} consists of both the interconnect capacitance and transistors' capacitance, which is complicated and circuit dependent. For

simplicity, the speed of an individual transistor is evaluated by its intrinsic gate delay τ [1]:

$$\tau = \frac{C_{GATE} * V_{DD}}{I_{ON}} \tag{1.1}$$

where C_{GATE} is the transistor gate capacitance, V_{DD} is the supply voltage and I_{ON} is the on-state current. The on-state current of a long channel transistor can be described as:

$$I_{ON} = \frac{C_{ox} * \mu * W * (V_G - V_T)^2}{2L_G} \tag{1.2}$$

where C_{OX} is the gate capacitance per unit area, μ is the effective carrier mobility, W is the transistor width, V_G is the gate voltage, L_G is the channel length, and V_T is the threshold voltage which can be expressed as a portion of the supply voltage V_{DD}. Thus, $V_T = \alpha * V_{DD}$, where α is a constant between 0 and 1. At the on-state in which $V_G = V_{DD}$, after replacing I_{ON} with the equation 1.2, the intrinsic gate delay can be described as:

$$\tau = \frac{C_{GATE} * V_{DD}}{I_{ON}} = \frac{C_{OX} * W * L_G * V_{DD}}{I_{ON}} = \frac{2 * \alpha^2 * L_G^2}{\mu * V_{DD}} \tag{1.3}$$

According to the equation 1.3, there are four approaches to improve the transistor speed:

1. Increasing the supply voltage V_{DD};
2. Decreasing the constant α to have a smaller V_T;
3. Decreasing the transistor gate length L_G;
4. Increasing the carrier mobility μ.

Approach (1) and (2) are not preferred as the gain of speed by these approaches has a cost of higher power consumption. The power consumption of one transistor can be roughly described by [2]:

$$P \approx AfC_{LOAD}V_{DD}^2 + I_o * 10^{-\frac{V_T}{SS}} * V_{DD} + I_{LEAK} * V_{DD} \quad (1.4)$$

where A is a constant value, f is the operating frequency, I_o is the drain current at $V_G = V_T$, I_{LEAK} is the total leakage current including gate and junction leakages, SS is the subthreshold slope. The equation 1.4 clearly shows larger V_{DD} and smaller V_T would increase the power consumption significantly.

Approach (3) has been adopted by the semiconductor industry and kept improving the MOSFET performance for around four to five decades. This approach is generally referred as scaling down. The magic of scaling down is that it could improve the transistor performance and lower the fabrication cost simultaneously. However, it has become challenge to scale down further due to stringent constrains in the tradeoff between on-state current, power consumption and short channel effects in sub-100 nm technology node. This approach, including its advantages and challenges, will be discussed in details in section 1.2.

Approach (4) is an alternative and increasingly important approach of improving the MOSFET performance for advanced transistors. Since approach (3) of scaling down Si-MOSFET is much cheaper and easier, this approach has not being attractive for a long time. However, as the scaling of Si MOSFETs approaches its physical limit, this approach has attracted increasingly more attention recently. Some technologies under this category, such as strain

engineering, have been employed to improve the carrier mobility in sub-90-nm technology nodes already [3]. Furthermore, semiconductor with higher carrier mobility such as germanium (Ge) [4-8] and III-V compounds [1, 9, 10], have been intensively investigated as alternative channel materials for future transistors.

1.2 MOSFET scaling

1.2.1 Overview of MOSFET scaling

Perhaps, a large part of the success of the planar Si MOSFET is due to the fact that it can be scaled down to increasingly smaller dimensions, which gains two benefits simultaneously: (1) faster transistor, which means higher performance ICs; (2) lower cost per transistor as each transistor takes less area on the chips. This remarkable trend was first pointed out by Gordon Moore and well known as Moore's law, which predicts that the number of transistors per integrated circuit would double approximately every ~ 2 years within approximately the same size chip (Fig. 1.2)[1].

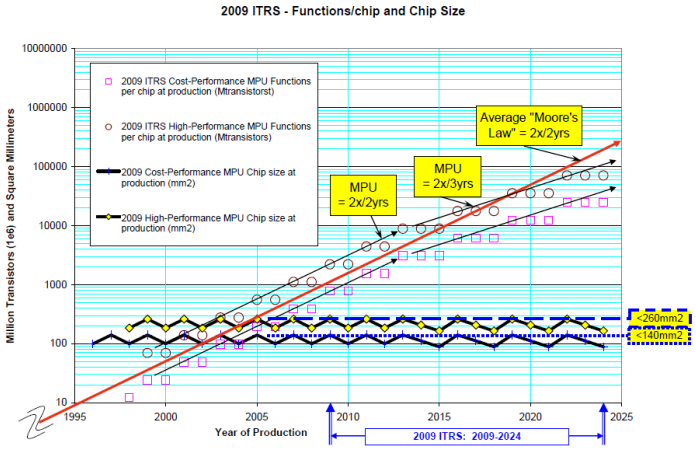


Figure 1.2: 2009 ITRS product technology trends: MPU product functions/chip and industry average "Moore's Law" and chip size trends[11].

Table 1.1: Transistor parameters in constant-voltage scaling and constant-field scaling, assuming long channel device and power = I_D*V_D.

Scaling factor: ξ	Before Scaling	Constant-Voltage	Constant-Field
Gate Length	L_G	ξL_G	ξL_G
Gate Width	W	ξW	ξW
Oxide Thickness	T_{ox}	T_{ox}	ξT_{ox}
Supply Voltage	V_{DD}	V_{DD}	ξV_{DD}
Drain Current	I_D	I_D	ξI_D
Power / Area	P	P/ ξ^2	P
Delay	τ	$\xi^2 \tau$	τ

There are two types of scaling, constant-voltage scaling and constant-field scaling. Table 1.1 shows the transistor parameters in the two scaling approaches. In constant-voltage scaling, only the lateral dimensions – the gate length L_G and gate width W of the transistor – are scaled down by the scaling factor **ξ;** while in constant-field scaling, the lateral and perpendicular dimensions as well as the supply voltage, are scaled down proportionally to maintain an approximately constant electrical field in the channel and the gate oxide.

In constant-voltage scaling, both the perpendicular dimensions and the supply voltage remains the same. Thus, as the gate length scales down, the electrical field between drain and source would keep increasing. At certain point, the electrical field is so strong that the Source/drain (S/D) depletion region would meet with each other and lead to mal-function transistors. Hence, the perpendicular dimension and the supply voltage need to be scaled down as well in

practical application, which is similar to constant-field scaling. In real application, it is generally required that the next generation of scaled-down circuit works faster than the last generation. This requirement is generally accomplished by not scaling down the supply voltage as aggressively as other parameters for a tradeoff with higher power density consumption.

1.2.2 Challenges of further scaling MOSFET

For a long time, a faster and cheaper transistor can be obtained by adopting the constant field scaling approach without causing any serious issues. However, it has been recognized that, in sub-100 nm regime, this conventional device scaling has confronted the difficulty that the three main performance indexes associated with MOSFET performance – on current, power consumption and short channel effects – have a tradeoff with each other, owing to several physical and essential limitations directly related to the device scaling down [10].

Short channel effects arise when the MOSFET channel length is scaled down to the same order of magnitude as the depletion-layer width of the S/D junction. As the gate length is reduced, drain and source become so close that the channel potential is influenced not only by the gate bias, but also by the drain bias. Thus, the potential barrier at channel is no longer effective to block the carrier transportation between source/drain. To suppress short channel effects, it is required to have thinner gate oxide, higher substrate doping (N_{sub}), smaller S/D junction depth (X_j), lower extension concentration and lower supply voltage (V_{DD}). However, it is obvious that those requirements conflict with those of higher I_{ON} and lower power consumption. Thinner gate oxide will increase gate leakage (I_G)

exponentially, which increase the power consumption significantly. It is reported that the direct tunneling current of I_G increases approximately one order with every 2 Å reduction of gate oxide thickness for a normal gate oxide thickness of 15 Å [12]. Smaller X_j and lower extension concentration increase S/D series resistance, which consequentially decrease on current significantly. The increase of N_{sub} is necessary in suppressing short channel effects in bulk MOSFETs; however, it increases I_{leak} due to junction tunneling current and gate induced drain leakage current. In addition, it causes the reduction of I_{ON} as it lowers the carrier mobility.

From equation 1.4, it is required to have smaller V_{DD}, larger V_T and thicker gate oxide to have lower power consumption. Apparently, smaller V_{DD} and larger V_T decrease I_{ON} while thicker gate oxide leads to worse short channel effect performance. On the other hand, achieving larger on-state current requires higher V_{DD}, smaller V_T, thinner gate oxide, higher extension concentration, higher junction depth and lower substrate doping, which apparently conflict with those of lower power consumption and better short channel effects immunity.

As a result, for any approach of further improving the MOSFET performance, it needs to overcome these difficulties or to mitigate these stringent constraints in this tradeoff, that is to satisfy the high performance and low power consumption against these physical limitations simultaneously. High-k/metal-gate, which can mitigate the tradeoff between gate leakage and equivalent-oxide-thickness (EOT) requirements, have already been implemented for advanced MOSFETs. Employing the nanowire gate-all-around (GAA) transistor architecture is another approach to reduce the stringent requirement on EOT. High mobility

semiconductor such as Ge has also attracted heavy attentions as alternative channel materials to improve on-state current without sacrificing the power consumption and short channel effects performance.

1.3 High-k/metal-gate for gate dielectric scaling

High-k gate dielectric is necessary to scales down the EOT further for advanced transistors. One of the main challenges to scale down advanced MOSFETs is the gate oxide scaling. As listed in table 1.1, the oxide thickness is required to be reduced by the scaling factor ξ for the next generation transistors. For the last four decades, the SiO_2 gate dielectric thickness has been scaled down and reached its physical limit. According to International Technology Roadmap for Semiconductors (ITRS), a MOSFET with gate length below 90 nm will need oxide thickness of less than 12 Å as shown in Fig. 1.3. That corresponds to only a few layers of SiO_2 atoms, and it is so thin that the gate leakage has already become a major portion of the transistor power consumption. Further scaling down the oxide thickness will increase the leakage current exponentially, as the gate leakage current increases approximately one order with every 2 Å reduction of SiO_2 thickness when the SiO_2 thickness is less than 15 Å [12]. An alternative gate dielectric with dielectric constant (k) greater than SiO_2 (k=3.9) has been proposed to reduce the gate tunneling leakage. With the benefit of higher dielectric constant, the gate dielectric physical thickness can be larger to suppress leakage current while maintain the same capacitive coupling to the channel. Among all the reported high-k materials, hafnium based oxide compound has already been employed by the semiconductor industry for its sufficiently large

bandgap (E_g ~ 5.6 eV) and fairly high k value ~ 20 - 25. Additionally, thermal stable HfO_2 with EOT ~ 10 Å has been demonstrated on both Si [13] and Ge [6]. However, many challenges remains on further scaling down the EOT of hafnium oxide based material, such as the undesired interfacial layer formed by oxygen atoms and the substrate. The dielectric constant (k value) of this interfacial layer, such as SiO_2 for high-k on Si substrate, is much lower compared than that of high-k materials, and it limits further scaling down of the gate stack EOT. Thus, more scientific and technological innovations are needed to continue the scaling.

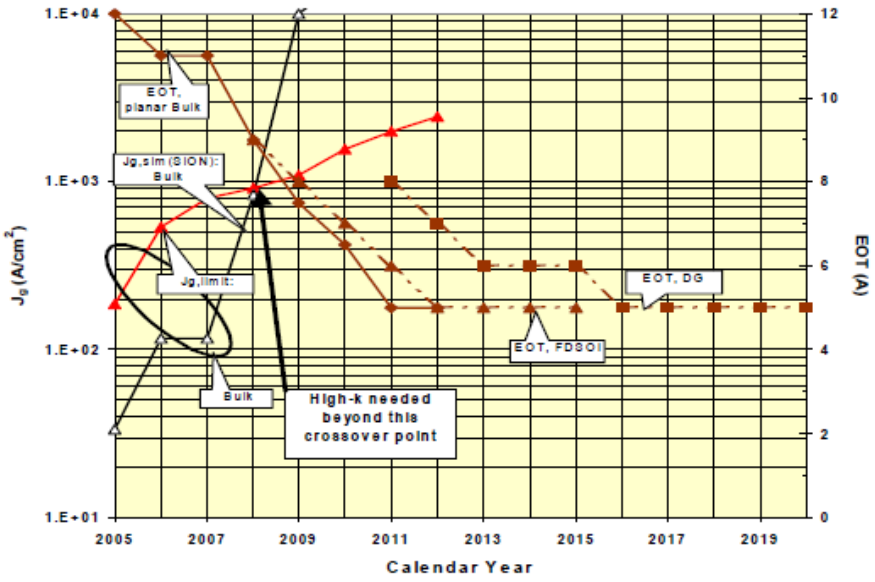


Figure 1.3: The limit of the gate leakage current ($J_{g,limit}$) required by ITRS versus the simulated gate leakage current ($J_{g,simulated}$) for high performance applications[11].

Another performance booster is the metal gate. The conventional gate electrode of heavily doped poly-Si has many advantages, such as adjustable work function, excellent compatibility to SiO_2 and superior thermal stability. As MOSFETs scales down, it is found that poly-Si electrode has several problems and it is no longer a suitable gate electrode for advanced MOSFETs. The first

problem is poly-depletion effect, which refers to the phenomenon that a thin layer of heavily doped poly close to the gate oxide is depleted and leads to ~ 3 - 5 Å thicker EOT. This phenomenon is ignored for a long time as the EOT of the conventional long channel transistors is large. However, since the EOT of advanced transistors has been scaled down to less than 15 Å already, the additional 3 - 5 Å EOT due to the poly depletion effect becomes a significant portion and makes further gate oxide scaling problematic. Another problem of poly gate is that, the gate oxide of advanced transistors is so thin that boron could easily diffuse through the gate oxide into the substrate channel, which leads to a shifted threshold voltage and larger the gate dielectric leakage. Moreover, for high-k dielectric applications, the thermal dynamical stability of poly on high-k gate stacks and work function's Fermi-level pinning effects are all well reported problems. As a replacement of poly-Si gate, metal gate electrodes do not have all of these problems.

High-k/metal-gate has become necessary for advanced transistors, as it is able to reduce the gate leakage current or suppress short channel effects without sacrificing other key transistor performance parameters. Dual work function metal gates are normally required for deeply scaled planar devices. However, mid-bandgap metal gate is adequate for a GAA device due to better electrostatic coupling of GAA architecture. Among all the metal gate candidates, TaN is one of the well reported metal electrodes and it is chosen as the metal gate in this work for its good thermal stability on high-k materials and their mid-bandgap work function.

1.4 Objectives and scopes

This project is to explore the top-down engineered nanowire GAA MOSFET for future transistor applications and to address its possible performance bottlenecks. The nanowire GAA architecture is well reported for its superior gate electrostatic coupling to the channel which is able to overcome/mitigate the stringent constraints in the tradeoff discussed in section 1.2; thus, it makes further scaling possible. In this project, two main issues are addressed:

1. The high parasitic series resistance of a nanowire GAA transistor limits its on-state current. The possible solution is studied in this project by replacing the heavily doped source/drain with highly conductive metal. The fabrication and understanding of the Si nanowire gate-all-around MOSFET with 1-D NiSi Schottky barrier source/drain is included in this thesis. The effective Schottky barrier height and Schottky barrier shape of Si nanowire and planar Schottky barrier MOSFETs are studied by both experimental data and MEDICI simulation in this project.
2. Ge is explored as a high carrier mobility channel and it is integrated with the nanowire GAA transistor architecture. A novel technique of fabricating Ge nanowires on an epitaxial Ge layer is presented in this thesis. The passivation layer of GeO_2 and Si shell are explored and characterized in this project. Ge nanowire transistors integrated with HfO_2/TaN gate stack are characterized and studied in this project.

1.5 Thesis organization

This thesis is organized in the following chapters:

Chapter 2 gives a background and literature review on nanowire and Ge transistors. The evolution of transistor architectures is presented and the motivation of developing nanowire GAA transistors is highlighted. The two main streams of nanowire fabrication technique - bottom-up and top-down techniques - are discussed. The background knowledge on Ge transistors is also discussed in chapter 2, including the motivation and major challenges of replacing Si channel with Ge channel. The development history of gate oxide of Ge MOSFETs is presented in chapter 2. Other challenges such as junction leakage and process integration are also discussed in chapter 2.

Chapter 3 presents the work of the Si nanowire gate-all-around MOSFET integrated with 1-D NiSi Schottky barrier source/drain. The background knowledge of Schottky barrier MOSFET is discussed first. The detailed fabrication processes of Si nanowire GAA MOSFETs integrated with 1-D NiSi Schottky source/drain are presented in this chapter. Device characterization is conducted on both Si nanowire and planar Schottky barrier MOSFETs. Carrier injection is found to be improved in nanowire GAA transistors in this chapter.

Chapter 4 presents the Ge nanowire pMOSFET on epitaxial Ge substrate. The detailed processes of Ge epitaxial growth on Si substrate and Ge nanowire formation on the epitaxial Ge substrate are presented and characterized. Ge nanowires integrated with HfO_2/TaN gate stack and GeO_2 passivation shell are demonstrated and characterized in this chapter.

Chapter 5 presents Ge/Si core/shell nanowire pMOSFETs. Epitaxial grown Si shell on Ge is explored as a technique to smooth the Ge surface. Additional implantation and Ni germanidation process through contact holes are employed to reduce the high series resistance of Ge nanowire transistors presented in chapter 4. Ge/Si core/shell nanowire pMOSFETs are characterized and studied in this chapter. The integration of the Si shell is found to be able to improve hole mobility in the Ge nanowire channel significantly.

Chapter 6 summarizes the major results and findings. It also provides some suggestions on future research.

Chapter 2
Literature Review

2.1 Nanowire gate-all-around architecture

As discussed in chapter 1, MOSFET scaling requires scaling down the gate oxide thickness to suppress short channel effects for conventional bulk transistors, which, however, trades off with power consumption. While employing high-K/metal-gate is an approach to overcome/mitigate this tradeoff, employing innovative transistor architectures is another effective approach. Those innovative transistor architectures are able to enhance the gate electrostatic coupling to the channel. As a result, short channel effects can be effectively suppressed without scaling down the gate oxide thickness when switching from the conventional transistor architecture to those innovative ones. Fig. 2.1 shows those transistor architectures that have been extensively explored in the last decades. They are the fully depleted silicon-on-insulator (FD-SOI) transistor [14-16], the double-gate transistor [17, 18], the tri-gate transistor [19-21], the π-gate transistor[22-24], the Ω-gate transistor[24-27] and the gate-all-around (GAA) nanowire transistor[28-30], with the gate electrostatic coupling capability becomes better and better.

Among all those innovative architectures, GAA nanowire MOSFETs have attracted intensive attentions from the research community for reasons discussed in the following paragraphs.

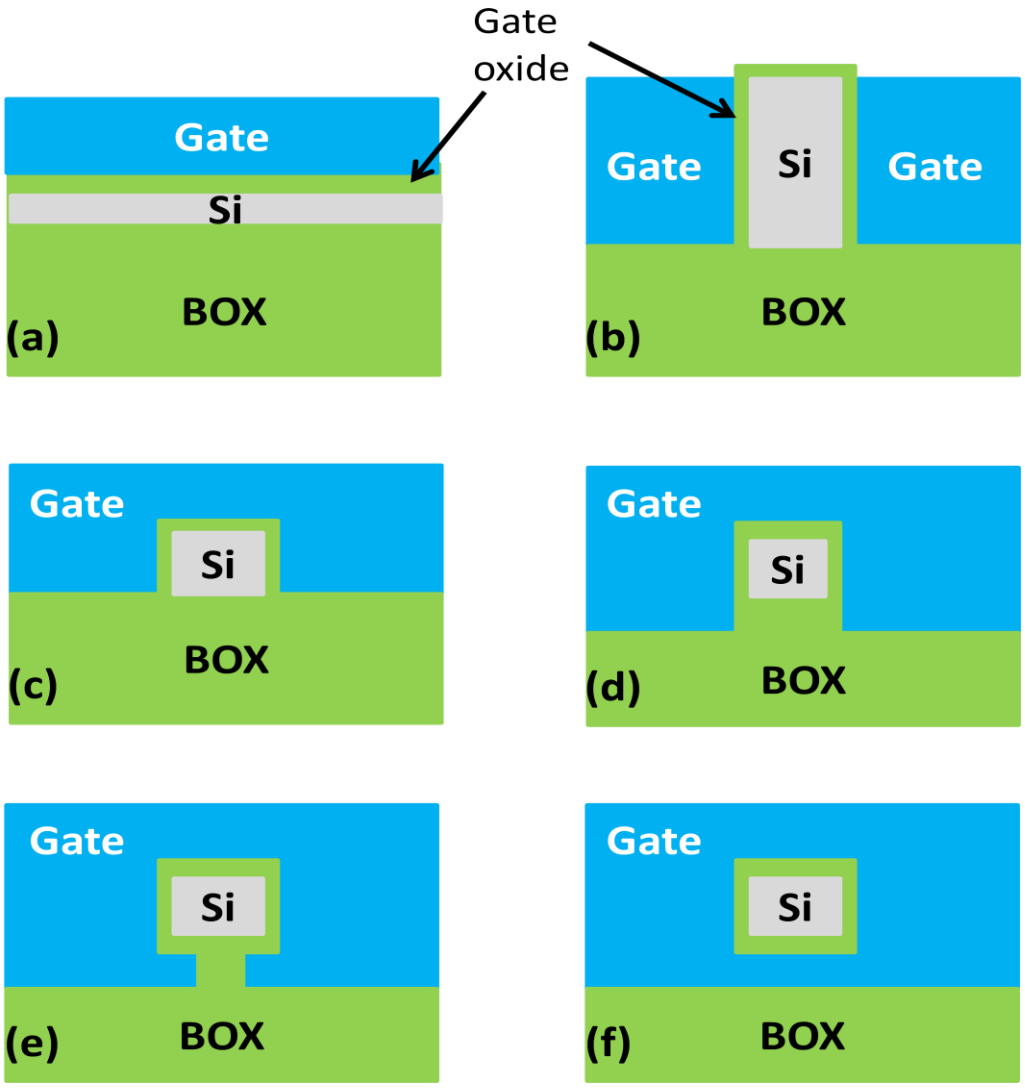


Figure 2.1: Schematics of transistor architecture evolution: (a) FD-SOI MOSFET; (b) double gate transistor; (c) Tri-gate transistor; (d) π-gate transistor; (e) Ω-gate transistor; (f) GAA transistor.

The first advantage of the nanowire GAA architecture is its best electrostatic control over the channel and thus it has the best scalability [27, 31, 32]. By solving the Poisson's equation for potential in a double-gate SOI and a nanowire GAA transistor architecture, it has been clearly shown that the GAA nanowire architecture has better immunity to short channel effects [17, 32, 33]. At 1997, Auth et al. showed that, compared with double-gate MOSFETs, the minimum

gate length of GAA transistors could be reduced up to 40 % while maintaining the same short channel performances with the same gate oxide and channel thickness[32]. Bescond et al. reported a simulation work on various device architectures with the gate length in sub-10-nm regime, and predicted that the GAA nanowire transistor has the best control over short channel effects[31]. His simulation work shows that a reasonable small subthreshold swing (SS) and drain induced barrier lowering (DIBL) are achievable at the sub-10-nm gate length regime with the GAA nanowire architecture.

Table 2.1: Summary of key device parameters of some of reported nanowire nMOSFETs.

	Ref. [29]	Ref.[34]	Ref. [35]	Ref. [27]	Ref. [36]
NW diameter (nm)	5	8	1.5	5	~5
Gate structure	GAA	GAA	GAA	Ω-gate	GAA
Gate type	Poly-Si	TiN	Poly-Si	Poly-Si	Poly-Si
Dielectric	SiO2	SiO2	SiO2	SiO2	SiO2
Lg(nm)	8	15	350	10	130
EOT (nm)	4	3.5	4	1.9	5
Vdd (V)	1.2	1	1.2	1	1.5
Ion (μA/μm)	3740	1440	2400	522	1039
Normalization	Diameter	Diameter	Diameter	---	Diameter
SS (mV/Dec)	75	72	60	75	72-74
DIBL (mV/V)	22	50	6	80	4~12
Ion/Ioff	$>10^7$	10^6	10^6	10^5	$>10^8$

Experimental works confirmed the excellent scalability of the nanowire transistor. At 2004, Yang et al. reported the first sub-10 nm gate length nanowire transistors [27] with fairly good short channel performance in terms of I_{on}/I_{off} ratio, SS and DIBL. The reported 10 nm gate length inversion mode nanowire nMOSFET achieved intrinsic gate delay of 0.22 ps, on/off ratio of 52200, SS of 75 mV/dec and DIBL of 80 mV/V. The reported 5 nm gate length Ω-gated accumulation mode nanowire pMOSFET achieved intrinsic gate delay of 0.48 ps, on/off ratio of 5 orders, SS of 63 mV/dec and DIBL of 14 mV/V. Those values are much better than those of reported double-gate FinFET [37], planar SOI [38, 39] and conventional bulk transistors [40] with similar gate length. Table 2.1 lists some of the reported nanowire transistor performance.

The second advantage of the nanowire GAA architecture is the higher carrier mobility. Firstly, the acoustic phonon scattering should be suppressed because of the reduced phase space for backscattering in 1-D system[41]. Secondly, the channel is intrinsic; thus, coulomb scattering is minimized. For a conventional bulk transistor, the channel doping level kept increasing to suppress short channel effects as device scales down. However, higher dopant concentration degrades the carrier mobility significantly. Lastly, the surface scattering is suppressed due to volume inversion effect[42], and reduced transverse electric fields due to the increased capacitive coupling of the geometry.

Another advantage of the nanowire architecture is the ultra low power consumption. This advantage enables the nanowire transistor of great potential in mobile electronics as well as bio-applications which require ultra-low power consumption. The leakage of the nanowire transistor is ultra-low, which is

possibly due to: (1) the channel leakage is suppressed by the superior gate coupling to the channel; (2) the S/D-channel junction leakage is minimized as a result of the minimized junction area; (3) the gate leakage is reduced due to the mitigation of gate oxide scaling. The ultra-low leakage in the nanowire transistor also partially contributed to its high on/off ratio.

Currently, there are two approaches to fabricate nanowires: bottom-up approach and top-down approach. These two approaches have their advantages and disadvantages and both of them will be discussed in the following two sections.

2.2 Nanowires fabricated by bottom-up approach

In bottom-up approach, nanowires are synthesized. There are a number of methods reported that can synthesize nanowires, such as template-directed growth [43-46], laser ablation growth [47-50], catalyst-assisted growth [51-56] and other methods [57]. Among those methods, vapor-liquid-solid (VLS) growth, one of the catalyst-assisted growth mechanisms, is the most well studied and reported methods for semiconductor nanowires synthesis [51-54, 58]. In VLS growth, the nano-scale particles of the catalyst are dispersed on a substrate. Then, the temperature is raised high enough to transform the catalyst nano-particles into liquid clusters. Those liquid catalytic clusters act as the energetically favored sites for localized decomposition of the vapor phase reactants, absorption of vapor phase reactants and crystallization of crystalline nanowires[59]. As the absorption and crystallization continues, the nanowires are grown from the catalytic clusters. The advantages of this approach are: (1) the size of the synthesized nanowire is determined by the size of the liquid catalytic cluster. The nanowire diameter as

small as 10 nm has been demonstrated with this technique; (2) uniform in-situ doping can be obtained by including the doping gas sources during the wire synthesis, and it can be well controlled to switching from n-type to p-type by simply switching the dopant gas sources. It is reported that Si[60], Ge [55, 57], SiGe and some III-V compounds nanowires[46] can be synthesized by this approach and the nanowire diameter and doping can be well controlled [61].

The bottom up approach has the advantage of low cost, as it does not require the expensive lithography process. However, the biggest challenge of this approach is to integrate those synthesized nanowires into functional ICs in a cost effective and reliable way. Typically, the synthesized nanowires are randomly spread over the wafer and they need complicated techniques to be integrated into device architecture for achieving specific functionalities. Some of the techniques reported for this purpose are 'pick-and-place' with AFM tip [62], liquid suspension[63], electric- or magnetic-field schemes[64-66], and fluid flow[59, 60]. Such processes lack control in repeatability and scalability. Moreover, the throughput is very low, which is a main economical factor for any new technique to be accepted in manufacture industry. These integration issues limit the nanowire fabricated by bottom-up approach from commercial applications.

2.3 Nanowires fabricated by top-down approach

In top-down approach, the pattern is first defined by lithography process and then transferred into the substrate to form fin-like structures, which are then converted into nanowires by trimming down the fins. Si nanowires have been successfully demonstrated with this technique, in which the converting process

normally is thermal oxidation followed by wet etch of oxide. The controllability and process window of the Si nanowire oxidation process is reported to be good due to a self-limiting effect, which refers to the phenomenon that the oxidation rate becomes slower and self-limiting as the Si-fin is trimmed down to nanowire size [35, 67-73].

The self-limiting oxidation of Si nanowires is first reported by Liu et al. at 1993[68]. It was reported that, unlike oxidation of planar Si surface where the oxide thickness increases along a parabolic curve, the oxide thickness over a Si column structure is self-limited and the final nanowire diameter was controlled by the oxidation temperature. It was reported that, the nanowire diameters were limited to be 11 and 6 nm after the dry oxidation of 30 nm diameter Si column at 800 and 850 ℃ separately for a long time [68]. In the following works, Liu et al. reported that the self-limiting phenomenon could be observed only when the oxidation temperature is below 950 ℃ and the main mechanism of the self-limiting effect was suggested to be attributed to the increase in the activation energy of oxide diffusivity as a result of the large stress in the formed oxide during the oxidation process [69]. In that work, 2-nm-wide Si nanowires with aspect ratio of more than 100 to 1 was achieved[69]. At 2000, Heidemeyer et al. reported the pattern dependent oxidation and the self-limiting effect in the oxidation of Si dots [70]. It was proposed that the oxidation rate decreases with increasing stress perpendicular to the Si surface and self-limiting occurs when the stress is over a critical value[70]. At 2008, Cui et al. suggested that the origin of the self-liming oxidation comes from the change of distribution of diffusion activation energy in the high density region which rises monotonically along with

the oxidation[71]. CMOS compatible process for nanowire fabrication utilizing the self-limiting oxidation has also been reported. Theng et al. explored the self-limiting technique for dual nanowire channels on SOI platform[73]. Although thin Si bridge is observed because the oxidation time is not long enough in Theng's work, the later work reported by Singh et al. successfully demonstrated circular single crystalline Si nanowire with diameter down to 3 nm formed by self-limiting oxidation on SOI wafers [35].

Unlike the bottom-up approach, the top-down approach does not have the integration issue as all the nanowires are printed by the lithography process. Moreover, the top-down fabrication process has the advantages of excellent repeatability, scalability, high throughput and compatible with the conventional CMOS process technology.

2.4 Germanium channel for future transistors

As discussed in chapter 1, replacing Si with other semiconductor having higher carrier mobility is another effective way to improve the MOSFET performance. The domination of Si MOSFETs in the ICs market could partially be attributed to the fact that Si has much better native oxide than its counterparts. The Si-SiO_2 system is perfect for MOSFET gate oxide, for its low interface state density, good thermal stability and low leakage current. However, this advantage of Si has gone as SiO_2 has been replaced by high-k gate dielectric, for suppressing gate leakage current while satisfying the EOT requirement. Thus, nowadays, other semiconductor with higher intrinsic carrier mobility, such as Ge, become very

attractive to be integrated with high-k gate dielectric for the future advanced transistors.

Table 2.2 lists the intrinsic materials properties of Si, Ge and a few popular III-V compounds. As shown in the table, Ge offers the highest intrinsic hole mobility, ~ 4 times higher than that of Si, and 2.5 times higher electron mobility than that of Si. Several times higher carrier mobility than the Si universal hole mobility has been demonstrated based on high-k/Ge system [6, 7]. Furthermore, a compressively strained Ge pMOSFET is demonstrated to have ten times or higher hole mobility against a Si pMOSFET [74-77]. As the scaling of the Si MOSFET approaches its physical limits, high-k/Ge system has received more and more attentions as an alternative way of improving the MOSFET performance [78]. Therefore, the Ge channel MOSFET is generally regarded as one of the most promising channel materials for high speed applications.

Table 2.2: Intrinsic material properties of Si, Ge and a few popular III-V compounds.

	Si	**Ge**	**GaAs**	**InP**	**InAs**	**InSb**
Electron mob. (cm^2/Vs)	1600	3900	9200	5400	40000	77000
Hole mob. (cm^2/Vs)	430	1900	400	200	500	850
Band gap (eV)	1.12	0.66	1.42	1.34	0.36	0.17
Permittivity	11.9	16	12	12.6	14.8	17
Melt Point (℃)	1415	937	1238	1059	941	525

2.5 Challenges of the Ge channel transistor

Although Ge has great potential of higher performance, there are several challenges associated with the fabrication of Ge MOSFETs.

2.5.1 Gate dielectric

The first and biggest challenge of fabricating Ge MOSFETs is the lacking of high quality gate stacks. Unlike Si, native Ge oxides (GeO and GeO_2) are water soluble and thermodynamically unstable[79]. This has been a bottleneck in introducing Ge channels into CMOS technology. Thermally grown native oxide of Ge is found to be primarily GeO_2 with small amounts of GeO_x ($x < 2$)[79]. GeO2 is water soluble, which not only leads to reliability concern but also makes the fabrication process challenge most of the cleaning processes have water. Furthermore, this Ge/GeO_x system is reported to have high interface state density (D_{it}) [80] which leads to lower mobility. GeO_xN_y has better thermal and chemical stability than native Ge oxides and it was once explored as a gate dielectric candidate. Shang *et. al*. reported ~ 40% enhancement in hole field effect mobility over the silicon universal curve [81] with this GeO_xN_y gate dielectric. Chui *et al*. studied the scalability of GeO_xN_y on Ge and reported CET down to 1.9 nm [82]. However, none of those works demonstrated GeO_xN_y as a suitable candidate for the future ultra-scaled MOSFET due to the high leakage based on experimental results. Probably the contribution of these studies is to use GeO_xN_y as a surface passivation layer in high-k/Ge system. Introducing nitrogen at the interface by annealing Ge in NH_3 ambient at 500-600 ℃ was first reported by Bai et al. [83] as an effective way to suppress gate leakage. The film grown by this technique is

found containing oxygen as well and its chemical composition is GeO_xN_y. However, the interface trap density of GeO_xN_y/Ge system is not sufficient low for high performance transistor application. Those traps reduce the mobility gains of replacing Si with Ge and lead to a large hysteresis in the MOS device.

To obtain high quality high-k/Ge interface, several other pre-gate surface passivation techniques have been investigated, such as PH_3 gas treatment[84], AlN_x passivation[84], sulfur passivation[85, 86], Si passivation [87, 88] and GeO_2 passivation[6, 89-91]. These surface passivation techniques can either reduce the interface state density or suppress the Ge out-diffusion into high-k dielectrics.

Recently, GeO_2 as an interfacial passivation layer has attracted a renewed attention. Takahashi et al. reported that GeO_2 decomposition is the root of high interface state density at the GeO_2/Ge interface and low interface trap density of thermally grown Ge oxide could be obtained once the decomposition of GeO_2 are suppressed [91]. Later, Xie et al. reported that high quality gate stack with D_{it} as low as 2×10^{11} $cm^{-2}*eV^{-1}$ could be achieved by incorporating fluorine passivation in GeO_2/Ge system, and reported hole mobility as high as three times of the Si universal hole mobility based on this system [6, 89, 90]. However, further reliability studies are needed for this approach.

The most popular and intensive studied approach is Si passivation [87, 92-95]. Wu et al., report that annealing Ge in SiH_4 right before HfO_2 deposition could suppress gate leakage and achieve ~ 140 % higher hole mobility [94]. Later, Bai et al. reported Si passivation achieved low D_{it} of 7×10^{10} $cm^{-2}*eV^{-1}$ and low gate leakage simultaneously [95]. The Si passivation layer works in such a way that it is consumed to form an interfacial layer before the underneath Ge reacts with

HfO_2. There are two advantages of this approach: (1) the formation of unstable GeO_2 could be minimized; (2) the dangling bonds between Si and Ge could be minimized, as the lattice mismatch between them is small enough to be handled by the ultra-thin Si layer. Hence, it could be expected to have the improved MOSFET performance. De Jaeger et al. reported that that the Si thickness must be controlled within a few monolayers to obtain a high quality, defect free Ge-HfO_2 interfacial layer on the planar substrate [93].

2.5.2 Junction leakage

The smaller bandgap of Ge compared with Si has been a concern because of its influence on band-to-band tunneling which leads to junction leakage. The reported junction leakage of n^+/p and p^+/n Ge diodes formed by boron and phosphorus implantation can be reduced to 10^{-4} A/cm^2 with annealing, which is considered acceptable for device operation[5]. However, it is still necessary to optimize the implantation and activation process to achieve this optimum result.

2.5.3 Process integration

Although Ge process is CMOS technology compatible, process integration issues should be taken care. For instance, the widely used chemical cleaning solution for Si such as piranha and SC1 cannot be used for Ge cleaning process. Process temperature is another issue. As shown in table 2.2, the melting temperature of Ge is 937 ℃. The melting temperature of nano-scale structure is reported to be lower than that of bulk material[96]. Thus, process temperature of

Ge device needs to be taken care, especially for Ge nanowires investigated in this project. Normally, the process temperature is kept to be below 600 ℃ for safety.

2.6 Summary

This chapter reviews the reported works on nanowire and Ge devices. GAA nanowire device architecture shows scaling advantage on its best gate coupling to the channel, which has been proved by both simulation works and experimental works. The nanowire fabrication methods are generally categorized into two groups, bottom-up and top-down approaches. Pros and cons of these two approaches are reviewed. The advantages of devices built on Ge are reviewed in this chapter. The Ge process challenges, including lacking of proper gate oxide, junction leakage and process integration, are reviewed in this chapter.

Chapter 3
Si Nanowire GAA MOSFETs Integrated with 1-D Schottky Barrier Source/Drain

3.1 Schottky diode

When metal is in contact with semiconductor, carriers move from the higher energy level to the lower energy level between the semiconductor and the metal. The redistribution of carriers leaves the fixed charge behind, forming a depletion region close to the semiconductor interface. This type of contact is referred as Schottky diode. Fig. 3.1 shows the energy band diagram of a typical Schottky diode on p-type silicon at equilibrium. $q\phi_{bn}$ is the Schottky barrier height (SBH) for electrons, $q\phi_{bp}$ is the SBH for holes, V_{bi} is the built-in potential and W is the depletion region width. Intuitively, the SBH depends on the affinity difference between the metal and the semiconductor as shown in Fig. 3.1. Experimental data shows that the SBH and the affinity difference is not a simply linear relationship. Further research attributes this difference to the Fermi-level pinning effect, which states that the interfacial states between the metal and the semiconductor offset the affinity difference.

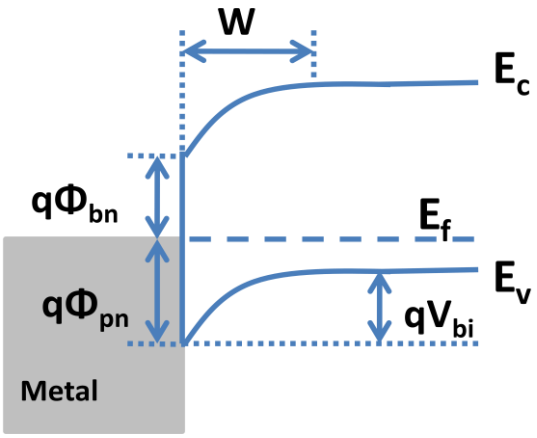


Figure 3.1: Schematic energy band diagram of a Schottky diode on p-type silicon.

Fig. 3.2 shows a Schottky junction under forward bias. For a Schottky junction, the net current has four components:

1. Holes travel from semiconductor to metal by thermal emission;
2. Holes travel from semiconductor to metal by quantum mechanical tunneling;
3. Recombination of electrons and holes in the depletion regime;
4. Electrons travel from metal to semiconductor by thermal emission.

For a Schottky diode presented in Fig. 3.2, the current from the recombination of electrons and holes normally can be neglected because of the low density of defect states. The current from the electrons travel from metal to semiconductor can be neglected because of the high thermal emission barriers. Thus, the net current can be approximately presented by the sum of thermal emission and quantum mechanical tunneling current. In Fig. 3.2, holes with energy higher than the Schottky barrier are able to overcome the barrier and

contribute to the net current by thermal emission (hole 1). For holes with energy lower than the barrier, it is still possible for them to tunnel through the barrier and contribute to the net current by quantum mechanical tunneling (hole 2).

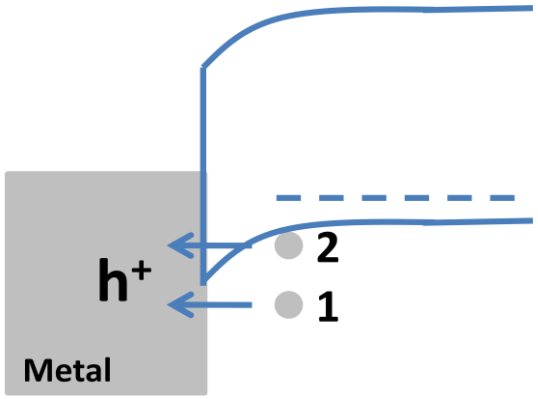


Figure 3.2: Schematic of hole transport mechanism in a Schottky diode. The energy of hole 1 is higher than the Schottky barrier, traveling from the semiconductor to the metal by thermal emission. Hole 2 travel from the semiconductor to the metal by quantum mechanical tunneling.

The depletion width W in a Schottky diode can be calculated with equation 3.1:

$$W = \sqrt{\frac{2\varepsilon_o \varepsilon_{Si}}{qN_A}(V_{bi} - V_F)} \tag{3.1}$$

where ε_{si} is the permittivity of Si, V_{bi} is the built-in potential and V_F is the applied forward bias. According to equation 3.1, the depletion width W decreases as the dopant concentration increases. For $N_A \geq 1 \times 10^{20}$ cm^{-3}, the depletion width is in the order of a few nanometers, and it is so thin that the tunneling current would become significant. For moderate doped semiconductor (ie. $N_A < 1 \times 10^{17}$ cm^{-3}), the diode current could be described by:

$$I = I_s[\exp\left(\frac{qV_F}{nkT}\right) - 1] \tag{3.2}$$

with

$$I_S = AA^{**}T^2 exp\left(\frac{q\emptyset_b}{kT}\right) \quad (3.3)$$

where I_s is the saturation current, A is the diode area and A** is the effective Richardson constant, ϕ_b is the SBH and n is the ideality factor. From equation 3.3, the ideality factor n can be derived as:

$$n = \frac{q}{kT}\frac{\partial V}{\partial[ln(I)]} \quad (3.4)$$

This parameter includes all the factors leading to a deviation of the Schottky diode in which n = 1.

3.2 Schottky barrier MOSFETs

3.2.1 Advantages of SB-MOSFETs

Fig. 3.3 shows the cross sectional view of a conventional and a Schottky barrier (SB) nMOSFET. The difference between a SB-MOSFET and a conventional MOSFET is that the heavily doped S/D in the conventional MOSFET is replaced by highly conductive metal in the SB-MOSFET, normally silicide for Si MOSFETs. The replacement of the p/n junction with the Schottky diode gives the SB-MOSFET several advantages:

1. Atomic abrupt junction. The interface between the metal and the semiconductor channel is atomic abrupt and can be accurately controlled by the reactant metal thickness and the process thermal budget, which implies high potential of scalability, especially applicable for the sub-10 nm gate length devices [97].

2. Simpler device fabrication. For SB-MOSFET, various implantations and the successive high temperature anneals are not needed any more; thus, it is easier for the integration of high-k/metal-gate due to its low-temperature fabrication process.
3. Reduced parasitic series resistance. The silicide has much lower sheet resistivity than heavily doped Si. This advantage is especially important for Ge channel devices, as the large S/D series resistance due to the low dopant solid solubility in Ge can be avoid by employing highly conductive germanide S/D.

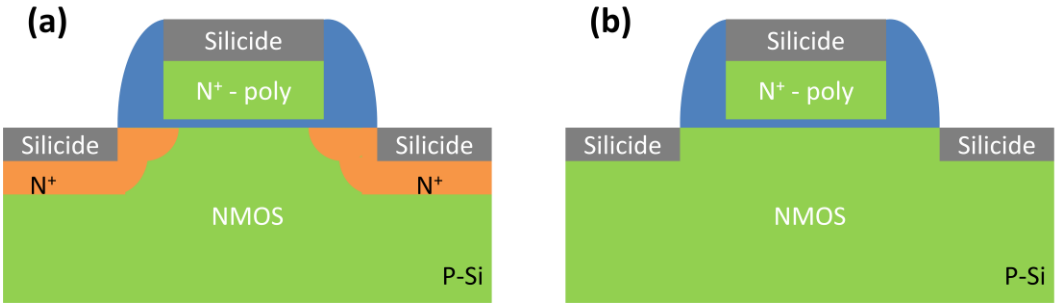


Figure 3.3: Schematic cross sectional view of (a) a conventional heavily doped S/D nMOSFET and (b) a Schottky barrier nMOSFET.

3.2.2 Operating principles of SB-MOSFETs

The operating principles of SB-MOSFETs are illustrated with the energy band diagrams in Fig. 3.4. Fig. 3.4 (a) shows the energy band diagram without gate and drain bias. The bending up of the energy band is due to the built-in potential between the metal and the semiconductor.

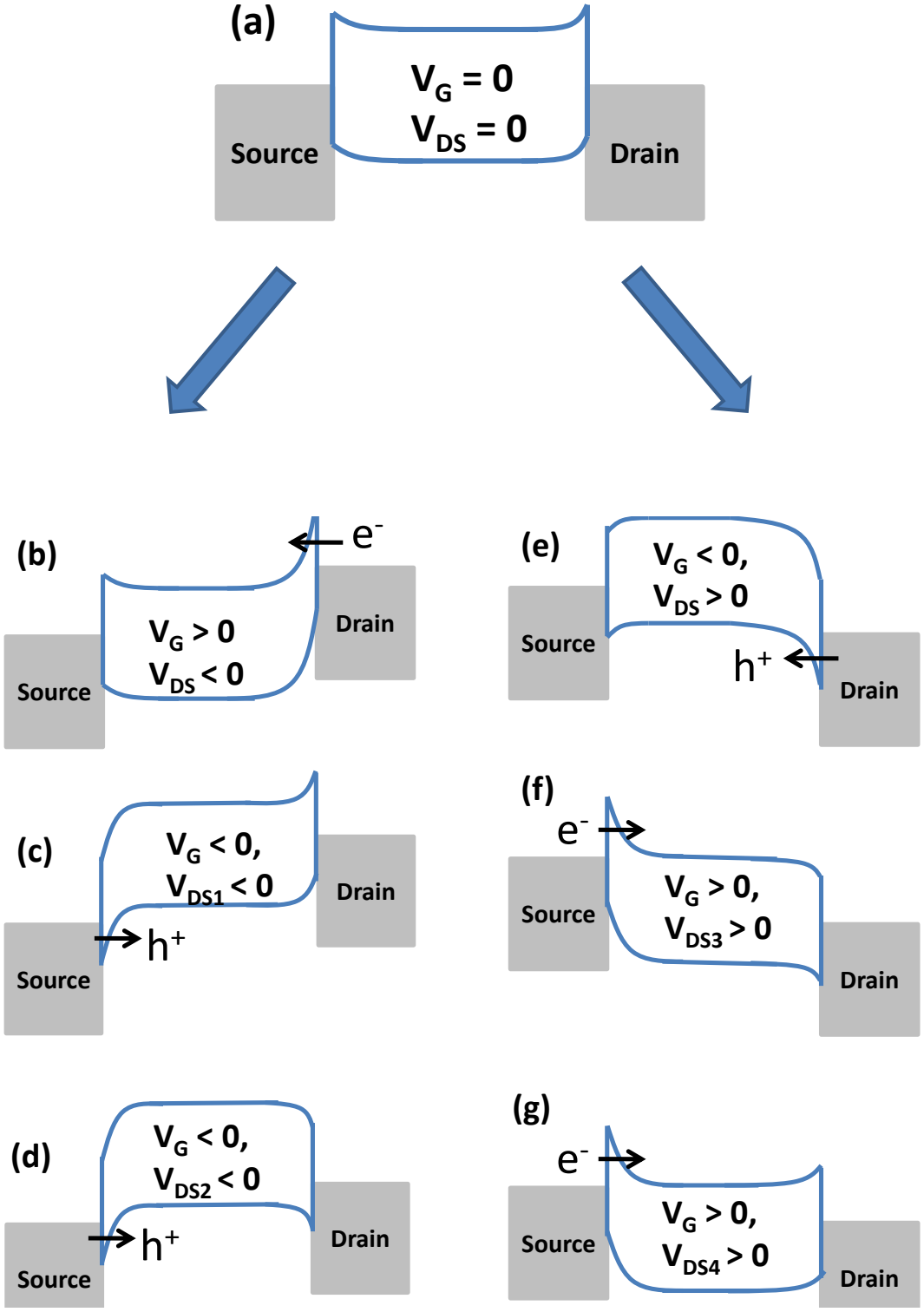


Figure 3.4: Energy band diagram of (b-d) SB-pMOSFETs and (e-g) SB-nMOSFET under various gate and drain bias. V_{DS2} is more negative than V_{DS1} and $V_{DS4} > V_{DS3}$.

A SB-MOSFET can function both as a pMOSFET and an nMOSFET, depending on the gate and the drain bias. Fig. 3.4 (b) – (d) illustrate the energy band diagrams when biasing the SB-MOSFET as a pMOSFET. At positive V_G, the energy band is pushed down by the gate bias, which leads to tunnel electron current at the drain side. As gate bias reduces, the energy band is pushed upward, and the Schottky barrier at the drain side gradually becomes thicker and leads to smaller leakage current. The leakage current of this SB-MOSFET is similar to, but have different mechanism from gate induced drain leakage (GIDL) of conventional MOSFETs. As the gate bias increases negatively, the energy band is pushed up and transformed from (b) to (c). In this process, the hole barrier at the source side gradually becomes transparent while the electron barrier at drain becomes thicker. Thus, tunneling electrons at drain side reduces exponentially while tunneling holes at source side increases exponentially, and the dominate transport carriers are switched from electrons to holes. A typical transfer characteristics of SB-pMOSFET is shown later in Fig. 3.12, in which, the net current first decreases and then increases as the gate bias increases negatively. This transfer output behavior of SB-MOSFET is named as ambipolar behavior [98] and it will be further discussed later. Fig 3.4 (d) shows that a forward biased Schottky barrier would exist at the drain side junction when the drain bias is small and the gate bias is large, which would limit the current at small drain bias. Fig. 3.4 (e)-(g) shows the energy band diagrams when biasing the same device as an nMOSFET and similar principles could be applied to understand the operations of SB-nMOSFET.

3.2.3 Challenges of SB-MOSFETs

In history, the investigation of SB-MOSFETs is based on planar transistor architecture. Simulation works show that the SB-MOSFET can be scaled down to sub-10 nm gate regime[99]. However, SB-MOSFET suffers from lower drive current compared with a conventional MOSFET having heavily doped S/D, as SB-MOSFET has an additional Schottky barrier at the source junction, which limits the on-state current.

Simulation works suggest that the S/D Schottky barrier height should be less than 0.1 eV in order to have comparable current drivability as the conventional p/n-doped S/D MOSFET [100, 101]. However, although a lot of efforts have been devoted to explore and characterize the various silicides, none of the reported silicides has a Schottky barrier height satisfying this requirement. Table 3.1 lists some of the typical SBH of heavily reported silicides. Among all the reported silicides, the best candidate for a pMOSFET is PtSi, which has the smallest Schottky barrier height for hole, ~ 0.2 eV [102]; the best candidates for nMOSFET are ErSi[103-107] and YbSi [104], which have the smallest Schottky barrier height for electron, ~ 0.27-0.36 eV. Apparently, the SBH of these silicides are not low enough to provide comparable high drive current as a conventional heavily doped S/D planar MOSFET and innovations are needed to lower down the SBH in SB-MOSFETs in order to have larger drive current.

Table 3.1: Commonly reported silicide Schottky barrier height on n-type Si.

Silicide	Φ_b (eV)	Preparation	Ref.
$TiSi_2$	0.61	-	[108]
$CoSi_2$	0.65	-	[108]
NiSi	0.67	-	[108]
$YSi_{1.7}$	0.39	Furnace	[103]
$ErSi_{1.7}$	0.39	Furnace	[103]
$ErSi_{1.7}$	0.36/0.35	Furnace	[103]
$ErSi_{2-x}$	0.41	RTA	[104]
$ErSi_{1.7}$	0.43/0.29	RTA	[104]
$ErSi_2$	0.27	UHV	[105]
$ErSi_2$	0.283	Furnace	[106]
$DySi_{1.7}$	0.37	Furnace	[103]
$YbSi_{1.7}$	0.27	RTA	[104]
$TbSi_{2-x}$	0.52	RTA	[104]
PtSi	0.9	Furnace	[102]

3.3 Advantages of Si nanowire GAA SB-MOSFETs

In view of lacking of silicide with sufficiently low Schottky barrier height, it is important to turn the efforts to minimize the Schottky barrier width to maximize the tunneling current. Fig. 3.5 shows the energy band diagram of a SB junction at various gate bias. Intuitively, we can see that at V_3, the SB width is

thinner and the drive current would be larger. In this way, the Schottky barrier width is modulated by the gate bias, leading to a lower effective Schottky barrier height. Thus, better gate coupling could lead to thinner Schottky barrier width at the same gate bias. As discussed in chapter 2, the nanowire GAA architecture is known for its best electrostatic control over the channel and it is considered as a potential candidate for the end-of-the-roadmap devices [32]. Thus, it is interesting to investigate the effects of nanowire GAA architecture on the SB-MOSFET.

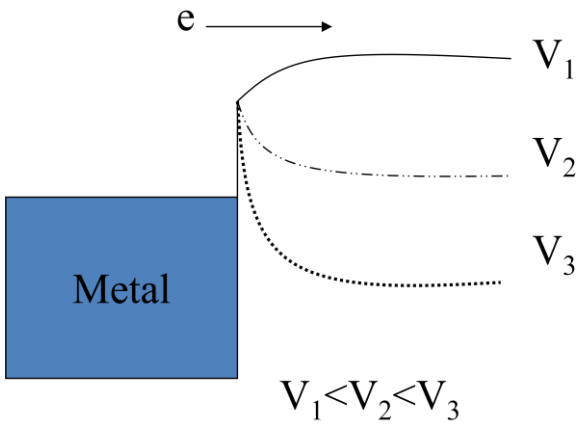


Figure 3.5: Schematic of gate modulation of Schottky barrier width.

Additionally, the nanowire GAA MOSFET suffers from high parasitic series resistance due to the narrow S/D conducting cross sectional area. The resistance R can be described as

$$R = \rho \frac{L}{A} \tag{3.5}$$

where ρ is the resistivity, L is the length and A is the conducting area. One potential solution of this problem could be to replace the S/D with highly conductive metal in the nanowire GAA Schottky barrier MOSFETs. For the heavily doped S/D nanowire MOSFETs, the resistivity ρ is limited by the dopant

solid solubility. The continual scaling of MOSFETs has reduced the channel resistance significantly, which has led to the increasing dominance of the parasitic series resistance in advanced MOSFETs [109, 110]. The narrower S/D conducting area in the nanowire device architecture makes the situation worse, leading to high S/D resistance forming a larger fraction of total resistance. In this point of view, lower S/D resistance is another advantage of nanowire GAA SB-MOSFET comparing with the heavily doped S/D in the nanowire GAA MOSFET.

In this chapter, nanowire GAA pMOSFETs integrated with 1-D Schottky barrier S/D will be discussed.

3.4 Si nanowire SB-MOSFETs fabrication

The process flow schematic is shown in Fig. 3.6. The starting material was 8" (100) silicon-on-insulator (SOI) wafers with a top Si (p-type, ~ 1×10^{15} cm^{-3}) thickness of 120 nm on a buried oxide (BOX) thickness of 150-nm. SiO_2/SiN (100 Å/700 Å) were used as the hard mask to define uniform fins (Fig. 3.6(a)), followed by S/D lithograph to define S/D (Fig. 3.6(b)). These two steps lithographs define the active area and they ensure the uniformity of Si-fins and thus, the uniformity of Si nanowires. Si-fins patterns with different drawn length from 200 to 1000 nm long and different width from ~ 40 nm width to 80 nm width were transformed into the Si layer by reactive ion etch and stopped at the BOX layer (Fig. 3.6(c)).

Si nanowires were formed by oxidation of the Si-fins in dry O_2 at 875℃ for 5 hours (Fig. 3.6(d)). Si fins in this experiment are positive sloped and the top width is less than the bottom width as shown in Fig. 3.7 (a). The oxidation rate at

the corner is much slower than that at the flat surface due to the stress effects; thus, the thermal oxidation results into a dumbbell shaped Si fin for initially wider Si fins. The dumbbell shape means larger Si width at the two ends connected with a thinner Si bridge as shown in Fig. 3.7 (b). If the initial Si fin width is smaller, the Si bridge connecting the two ends of the Si dumbbell will be fully oxidized and leads to two Si nanowires as shown in Fig. 3.7 (c). If the initial Si fin width is smaller enough (for the 40 nm Si fin in this experiment), the smaller top Si nanowire will be fully oxidized and only left one Si nanowire at the bottom as shown in Fig. 3.7 (d).

After 5 hours' oxidation, the Si nanowires were released from the oxide by dipping into 1:25 diluted HF. ~ 5 nm gate oxide was thermally grown as gate dielectric (Fig. 3.6(e)) and ~ 100 nm amorphous Si was deposited by low pressure chemical vapor deposition (LPCVD) successively. Gate implantation condition was phosphorous/$4\times10^{15}cm^{-2}$/25 KeV in 4 rotations with 45 degree tilted to the wafer surface, which leads to an Ω-shaped dopant profile surrounding the nanowires. The dopant was activated by rapid thermal annealing (RTA) at 1050 ℃ for 10 sec. In view of the dopant profile and the small dimension of Si-nanowire/gate-oxide, the poly directly below the Si nanowire is believed to be doped, and thus, forming a fully surrounding poly gate. SiN/SiO_2 was deposited as hard mask before the gate lithography. SiN/SiO_2 was deposited as hard mask before the gate lithography. The poly gate length was trimmed to expose the two ends of the Si nanowires near S/D pads for silicidation. This trimming was done by first trimming the gate photoresist in O_2 plasma, followed by trimming the hard mask (SiN/SiO_2) in phosphorous acid.

Planar Si Schottky barrier pMOSFETs are fabricated on the same wafer, following exactly the same processes described above. The only difference is the drawn width of planar devices is several micrometers instead of 50 nm fin width; therefore, the nanowire oxidation has ignorable impact over the planar devices.

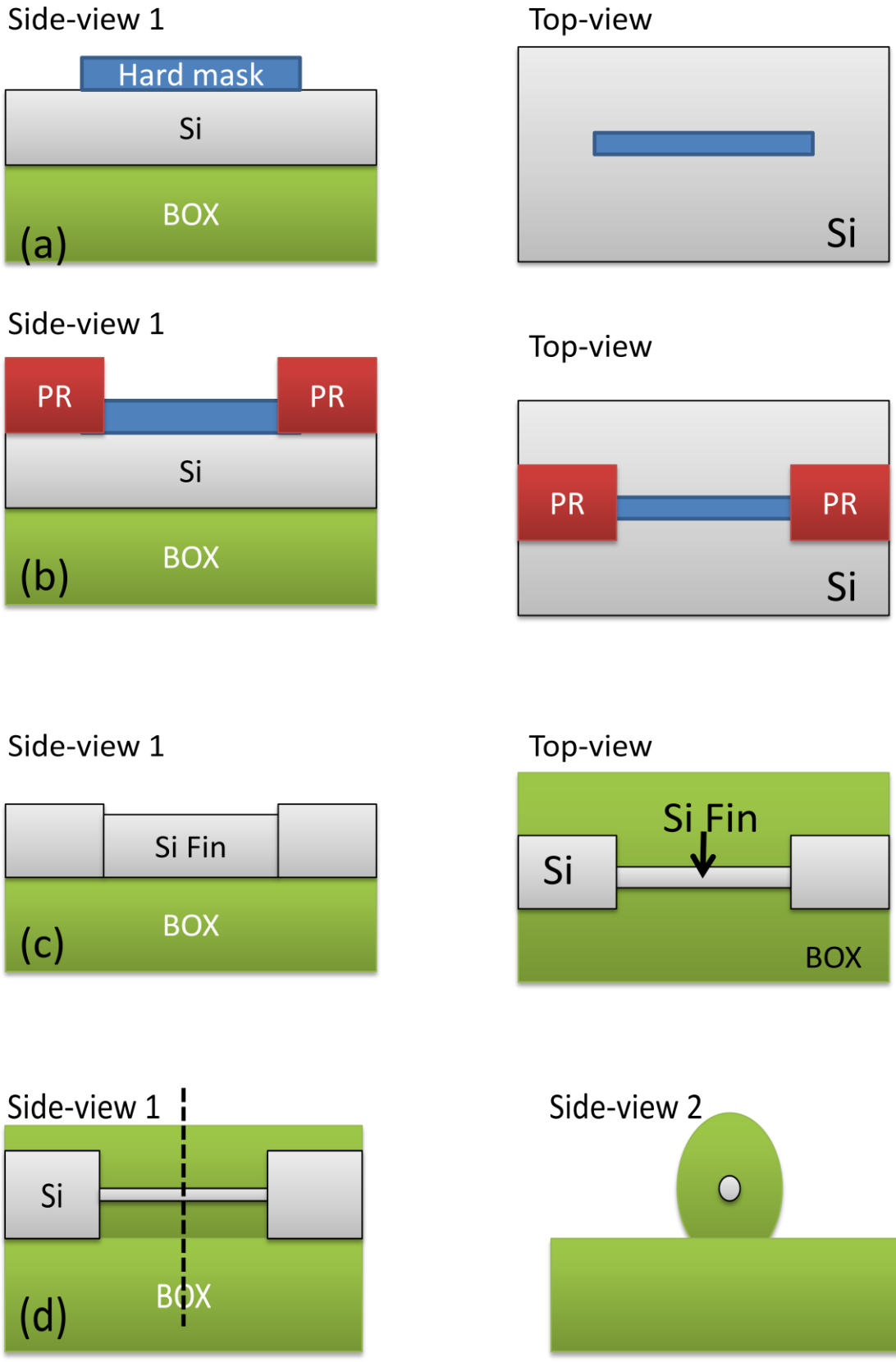
One of the challenge processes in this experiment is the poly gate etching. As shown in Fig. 3.6 (e), there is a distance (typically ~ 40 - 50 nm) between the Si nanowire and the BOX substrate and the poly in-between needs to be removed by over etch after the etching plasma reaches the Si nanowire. Since the chemistry property of Si nanowires and poly Si is the same, the gate oxide surrounding Si nanowire needs to be able to resist the poly Si over etch to protect the Si nanowire from the etching plasma; otherwise, the exposed two ends of the Si nanowire will be etched away and the S/D pads will be disconnected. The gate oxide is as thin as 5 nm in this experiment; thus, the poly Si over etch process needs to be optimized for high etch selectivity of poly Si over oxide. In this experiment, the poly etch is conducted in APPLIED MATERIALS PRECISION 5000, and the etch parameters are shown in table 3.2. The poly etching has two phases. The first phase is a standard poly etch, referred as “main etch” in table 3.2. The second phase is the optimized over etch process, referred as “over etch” in table 3.2. In order to achieving a selectivity of poly Si over oxide greater than 50, the pressure is increased from 70×10^{-3} Torr to 80×10^{-3} Torr; the power is reduced from 400 W to 75 W and the etch gas is switched from Cl_2 to HBr.

After the poly-Si gate patterning, gate hard mask was removed by phosphorous acid and diluted HF (Fig. 3.6(f)). Then, 100 Å SiO_2 / 150 Å SiN were deposited and etched to form the spacer (Fig. 3.6(g)). After a diluted HF dip

to clean the oxide on the S/D extension pads and the exposed nanowire edges, 1-nm Ti followed by 9-nm Nickel was sputtered by physical vapor deposition (PVD) system (Fig. 3.6(h)). NiSi was formed at the exposed Si nanowire tips and S/D pads by RTA process at 500C for 30 sec, and the excess Ni was successively wet removed by 10 min piranha (H_2SO_4+H_2O_2+H_2O, 1:1:5) (Fig. 3.6(i)). Standard metal contact formation and sintering process was done before the measurement.

Table 3.2: Etching parameters in PRECISION 5000 for highly selective etch of poly Si over oxide.

	Pressure	**Power**	**Gas**	**Flow rate**
Main etch	70 mTorr	400 W	Cl_2	60 sccm
			O_2	10 sccm
Over etch	80 mTorr	75 W	HBr	35 sccm
			O_2	5 sccm



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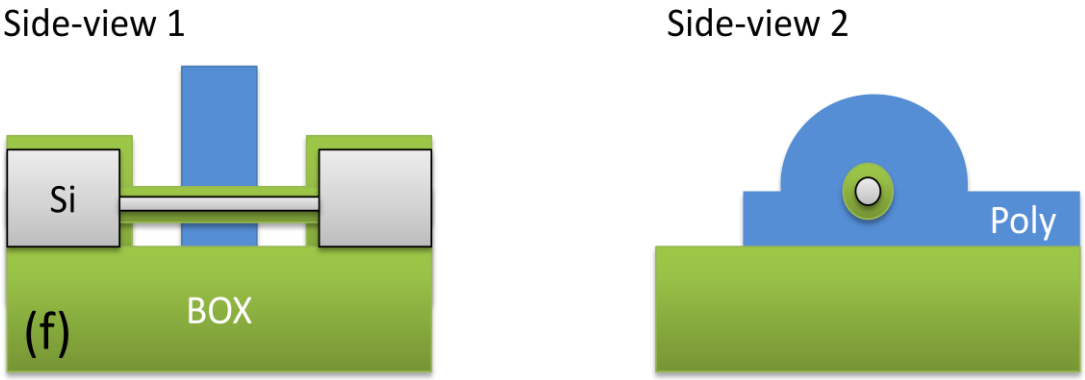

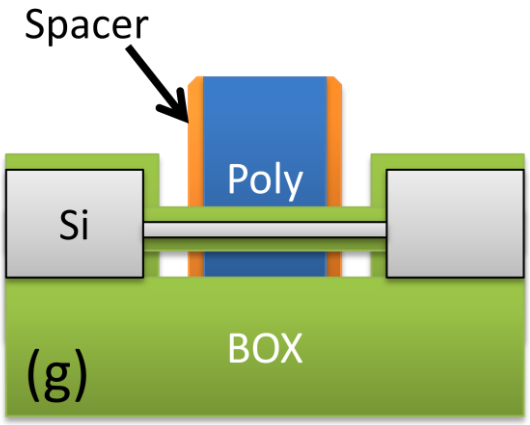

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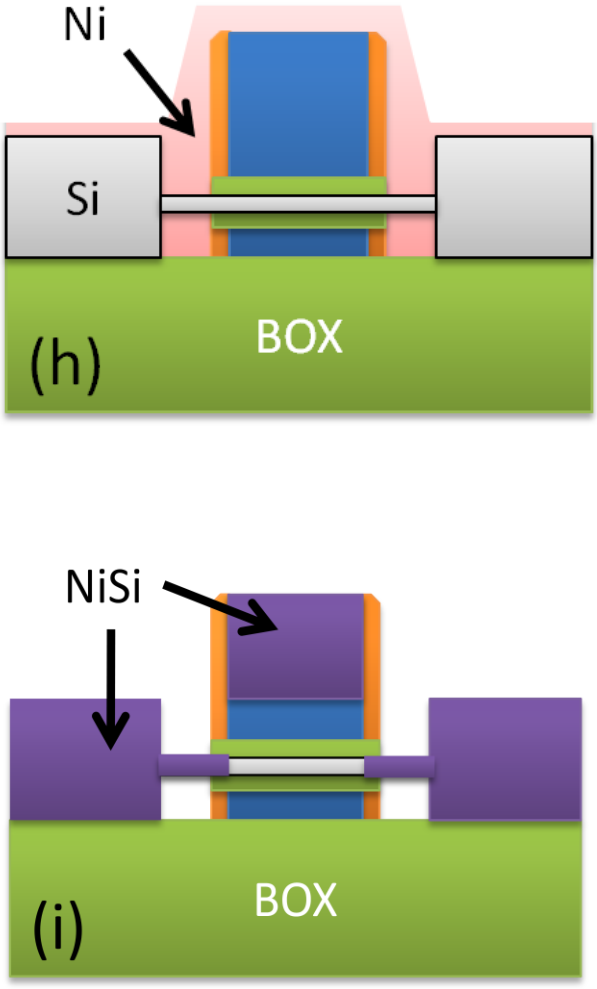

Figure 3.6: Schematics of the Si nanowire NiSi S/D MOSFET fabrication process. Schematics after (a) fin hard mask pattern and etch; (b) S/D photoresist pattern; (c) Si-fin etch; (d) self-retarded Si-fin oxidation; (e) gate oxide growth; (f) LPCVD amorphous Si deposition; (g) poly-gate etch and spacer formation; (h) oxide wet etch and Ni deposition; (i) Ni silicidation and Ni wet removal. From (a) to (c), the left side is the cross-sectional view and the right side is the top view. From (d)-(f), the left side is the side view and the right side is the cross-sectional view.

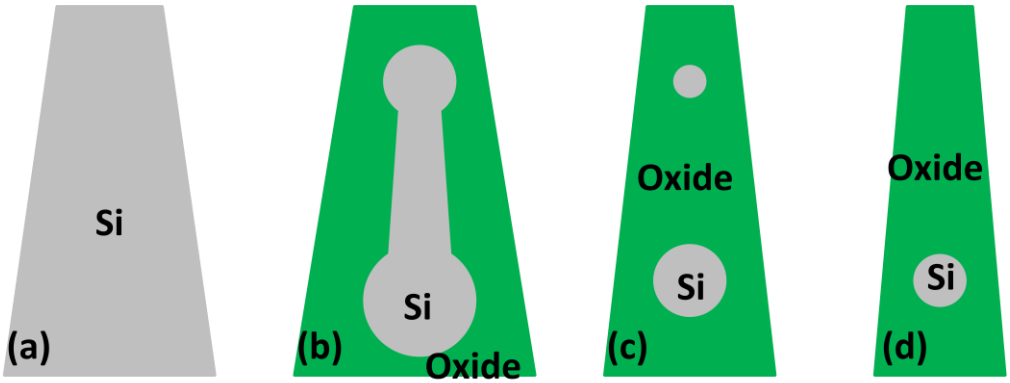

Figure 3.7: Schematics of the Si nanowire oxidation process. (a) Initial Si fin shape. (b) - (d) are after dry oxidation at 875 ℃ of (b) a wider Si fin, (c) an intermediate Si fin and (d) a thinner Si fin.

Fig. 3.8 (a) shows the secondary electron micrograph (SEM) image of the device after nanowire oxidation and oxide strip. Two nanowires are observed, with a smaller diameter nanowire on top and a bigger diameter nanowire at the bottom. The diameter difference between the two nanowires can be attributed to the initial Si fin geometry as shown in Fig. 3.7. Fig. 3.8(b) shows the SEM image after poly gate etch, which shows the two tips of the Si nanowire are exposed for silicidation process.

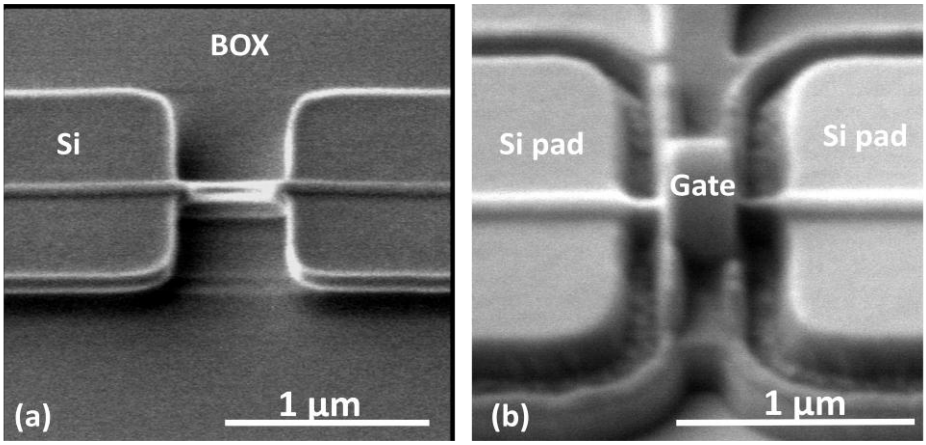

Figure 3.8: SEM image (a) after Si nanowire oxidation and oxide wet diluted HF strip and (b) after poly gate etch.

In previous studies, Lu et al. reported NiSi encroaches into a 37.5-nm Si nanowire after annealing, and the diffusion speed is reported to be 1.1 Å/s [111]; Appenzeller et al. reported NiSi has a faster diffusion speed along Si nanowires with smaller diameter and the diffusion length of Ni_2Si is over 100 nm along the Si nanowires with diameter ~ 50 – 100 nm at 280 ℃ for 30s [4]. Based on these works, we estimate the NiSi in our Si nanowire devices have encroached through the thin spacer (~ 15 nm, confirmed by TEM) after 500 ^{o}C, 30s RTA process and the final device structure schematic is shown in Fig. 3.6 (i), with NiSi encroached through the thin spacer.

3.5 Device physical characterization

Fig. 3.9 shows the cross sectional transmission electron microscope (TEM) image of an 80 nm wide Si fin after dry oxidation at 875℃ for 5 hours. Unfortunately, the TEM is not focused well that the Si lattice is not clear. However, it still could be observed that the oxide thickness close to the fin corner is obviously thinner than that at the middle of the fin height. The different oxide thickness could be attributed to the lower oxidation rate at the fin corner due to the larger compressive stress generated during oxidation. This stress retarded oxidation lead to a Si bridge connecting the wider top and bottom. Fig. 3.10 and Fig. 3.11 show the TEM images of a 12.5 nm height triangular shape Si nanowire and a 4 nm diameter circular nanowire cross section perpendicular to the gate extension. As shown in the TEM images, only one nanowire is left, suggesting the top thinner nanowire has been fully oxidized as explained in Fig. 3.7. The

surrounding oxide thickness is ~ 5 nm, slightly different at different surface orientation. An interesting phenomenon is that the 12.5 nm width Si nanowire is triangle shape while the 4 nm diameter Si nanowire is circular shape. The difference in nanowire shapes could be attributed to the difference of the initial fin width.

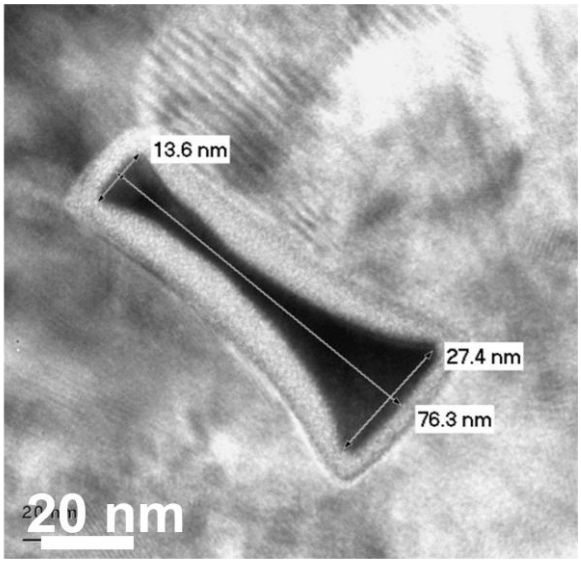

Figure 3.9: TEM image of 80-nm-wide Si fins after 875℃ dry oxidation.

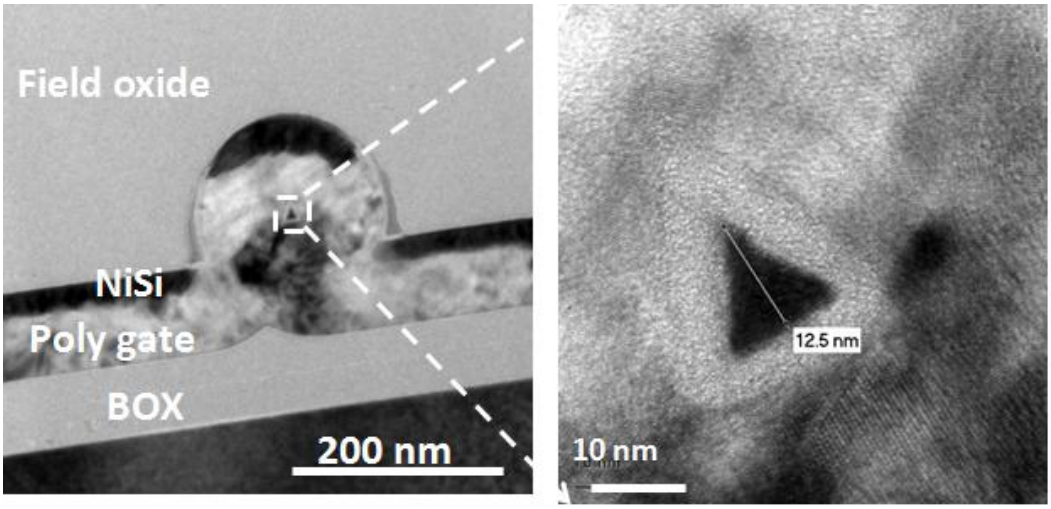

Figure 3.10: TEM images of a single 12.5-nm height triangular shape Si nanowire formed by dry oxidation at 875℃.

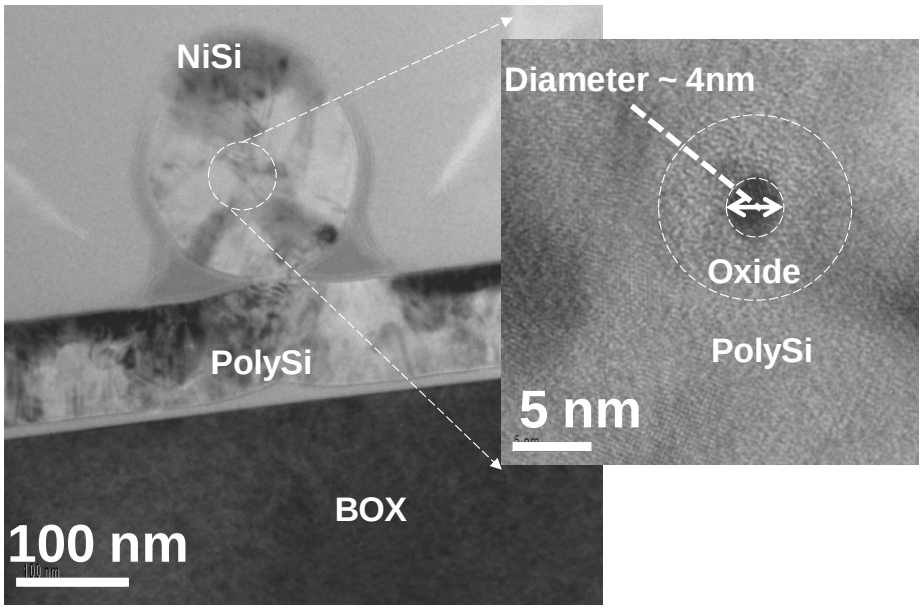

Figure 3.11: Cross sectional TEM images of a single 4 nm diameter Si nanowire formed by dry oxidation at 875℃. A circular Si nanowire surrounded by 5 nm gate oxide is observed.

3.6 Device IV characteristics

Fig. 3.12 (a) shows the experimental transfer characteristics of a 3 μm width and 850 nm gate length planar Si pMOSFET with NiSi Schottky barrier S/D. Typical ambipolar behavior of a SB-MOSFET is observed. For the hole current at negative gate bias, two different subthreshold regime could be identified, one with SS of 458 mV/dec and the other one with SS of 95 mV/dec separately. This could be illustrated by the energy band diagram shown in Fig. 3.12 (b). Initially, the valence band bends down due to the built-in potential. In this case, the carrier transport is dominated by thermal emission of holes from the source into the Si channel. As the gate bias increases negatively, the valence band would be pushed up, indicated by the symbols from □ to × in Fig. 3.12 (b). Thus, the barrier of

thermal emission become lower in a manner similar to the conventional heavily doped S/D MOSFET, leading to a small SS close to the theoretical value of 60 mV/dec. As gate bias increases more negatively, the valence band is pushed further upward from × to ○. In this case, the metal-semiconductor junction becomes a reverse biased Schottky barrier; thus, the current is limited by the Schottky barrier and a larger SS is observed.

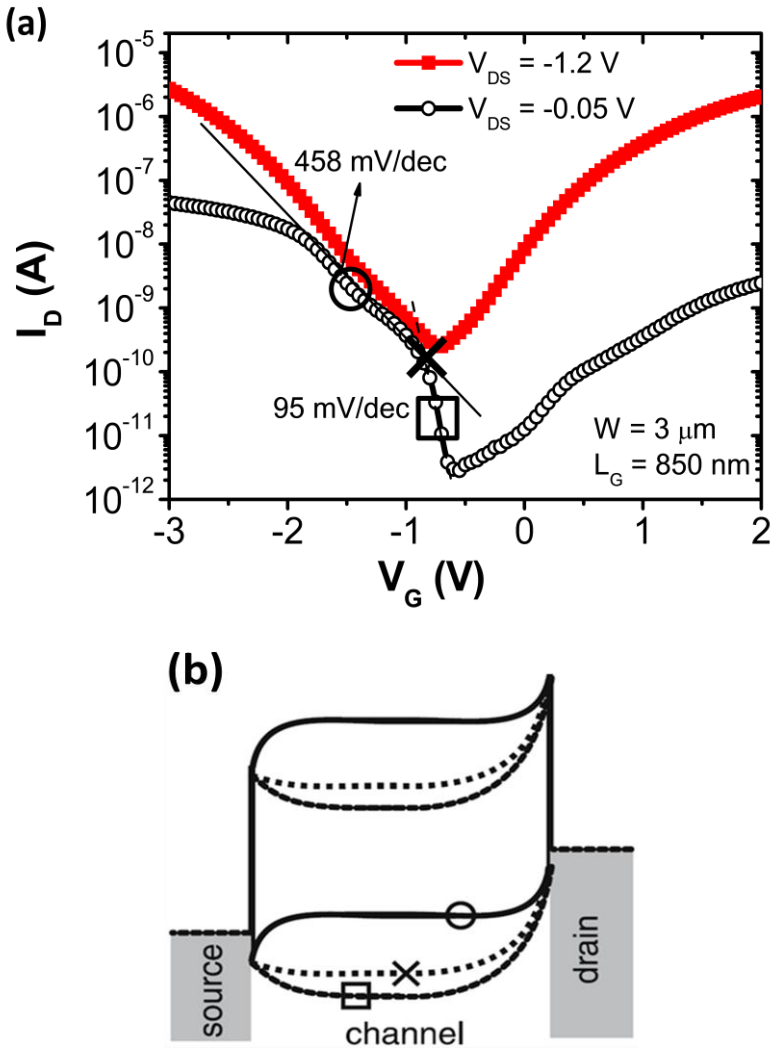

Figure 3.12: (a) I_DV_G characteristics of a planar Si Schottky barrier pMOSFET. (b) Energy band diagram of a Si Schottky barrier pMOSFET. The □, × and ○ stand for the regime under different gate bias in the I_DV_G and in the energy band diagram.

Fig. 3.13 shows the transfer characteristic of a 4 nm diameter Si nanowire (Fig. 3.11), a 12.5 nm width Si nanowire (Fig. 3.10) and a 1 um width planar SOI SB-MOSFETs on a single wafer without normalization. The gate length of the 4 nm diameter Si nanowire is 150 nm and the gate length of the 12.5 nm width Si nanowire and 1 um width planar SOI device are 850 nm. The planar SOI device shows a typical two subthreshold swing regime, showing the transition from thermal emission dominated current to tunneling dominated current as illustrated in Fig. 3.12(b). However, such transition disappeared in the transfer characteristics of Si nanowire Schottky barrier MOSFET as shown in Fig. 3.13, and lead to a small SS close to that of conventional heavily doped S/D transistors.

Ambipolar behavior could be observed on GAA Si nanowire SB-MOSFETs too; however, the off current is greatly suppressed by the GAA Si nanowire device structure as shown in Fig. 3.13. Fig. 3.13 did not show the electron current branch of the 4 nm diameter Si nanowire SB-MOSFET because the gate bias is not large enough at the positive side, ie., the net leakage current at the gate bias regime between -1V and 0V is so low that it is beyond the detection limit of the current analyzer. For a total suppression of ambipolar behavior, un-symmetry transistor architecture could be used [54].

The SS of the 4-nm diameter and the 12.5-nm width Si nanowire is 79 mV/dec and 86 mV/dec separately, which is much smaller than the 442 mV/dec of the 1-um width 100-nm body thickness top-gated planar SOI device. Since the Schottky barrier of NiSi for holes is ~ 0.46 eV[108], much larger than the thermal energy *kT*, carrier transport related to thermionic emission can be neglected and

the SS is dominated by the change of the tunneling probability through the Schottky barrier with changing gate bias. Even though the SS is influenced by changes of the depletion charge as well as by the trapped charges at the Si/SiO_2 interface with changing V_G, these factors has been estimated to be a minor effect on SS in un-doped SB-MOSFETs[112]. Therefore, SS represents a robust measurement of the carrier injection in SB-MOSFETs and the carrier injection has been improved in SB-MOSFETs based on Si nanowire GAA architecture. This improvement is significant in view of the SS of a 12.5-nm Si nanowire is 86 mV/dec while the theoretical SS of a 12.5-nm Si body top-gated planar SOI SB-MOSFET is ~ 254 mV/dec with the same gate oxide thickness[113]. Even though the gate length is the same, the Si nanowire GAA SB-MOSFETs achieved on current of 19 μA/μm from the 12.5-nm width Si nanowire with 850-nm gate length, which is much larger than the on current of 0.33 μA/μm from the 100-nm body thickness top-gated planar SOI device. Under -2.3 V gate bias and -1.2 V S/D bias, the 4-nm diameter, 150-nm gate length Si nanowire SB-MOSFET with 5-nm gate oxide achieved the small SS of 79 mV/dec and the large on-current of 207 μA/μm, which is comparable to those of conventional p/n doped S/D MOSFETs[35]. This on-current improvement can also be understood by the carrier injection improvement in Si nanowire GAA architecture.

The output characteristic of a 4 nm diameter Si nanowire GAA pMOSFET with 1-D NiSi Schottky S/D is shown in Fig. 3.14. It is interesting to find that the drain current increases by 100 μA/μm as gate overdrive increases from -0.5 V to -0.7 V, but it increases by over 200 μA/μm as gate overdrive increases from -1.1V to -1.3V. Since gate overdrive is linearly proportional to inversion carriers in the

channel, the non-linearity in drain current and gate overdrive suggests the current are still limited by the Schottky barrier. The effect of Schottky barrier could also be observed by the non-linearity in the linear regime in the output characteristics.

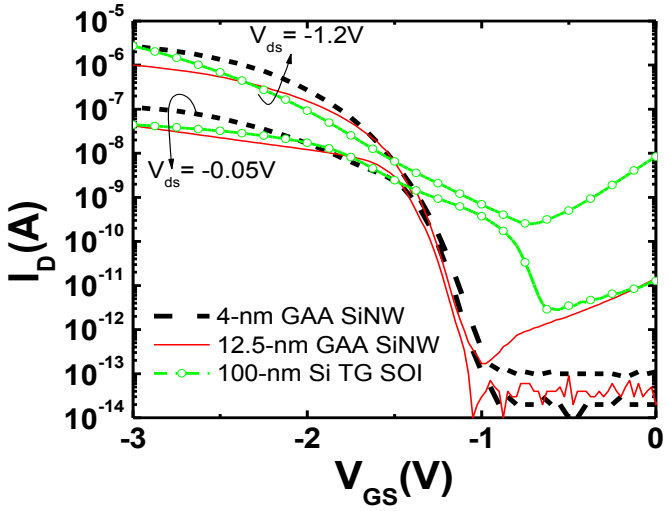

Figure 3.13: The I_DV_G characteristics of a 4-nm, 12.5-nm diameter GAA Si nanowire and a 100-nm Si thickness top-gate SOI NiSi S/D SB-MOSFETs.

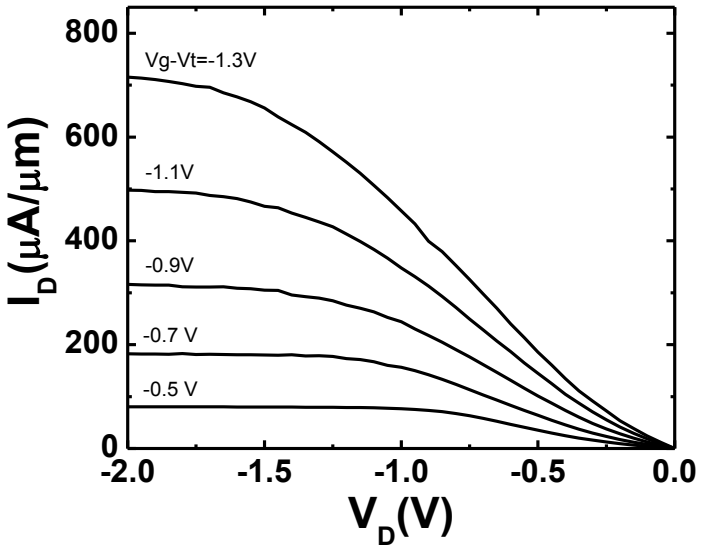

Figure 3.14: Output characteristics of a 4-nm diameter, 150 nm gate length NiSi Schottky barrier S/D Si nanowire GAA FET. The non-linearity of the linear region suggests the impact of Schottky barrier.

Fig. 3.15 shows the log plot of a 12.5 nm width Si nanowire GAA SB-MOSFET transfer characteristics at temperature from 260K to 360K. The corresponding linear plots are presented in Fig. 3.16. Clearly, at large negative gate bias, the hole current shows no temperature dependence at -1.2 V V_{DS} while it increases as temperature increases at -0.05 V V_{DS}. This difference could be explained by the energy band diagram shown in Fig. 3.4 (c) and (d) in section 3.2.2. At -1.2 V V_{DS}, drain current is limited only by the Schottky barrier at the source side; thus the drain current is dominated by tunneling current and shows no temperature dependence. At -0.05 V V_{DS}, there is another Schottky barrier at the drain side limiting the drain current. Since this barrier is low and it is forward biased, carriers transport by thermal emission mechanism at this junction. Thus the drain current become temperature dependent and is larger at higher temperature.

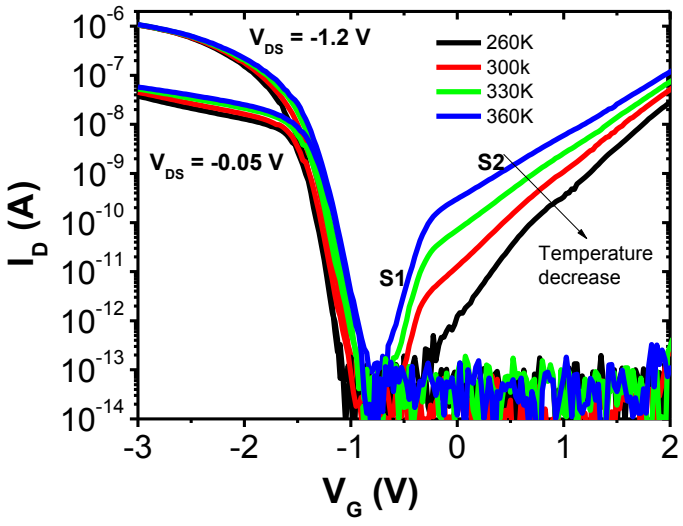

Figure 3.15: The transfer characteristics of a 12.5 nm width 850-nm gate length Si nanowire Schottky barrier MOSFET at temperature from 260 K to 360 K.

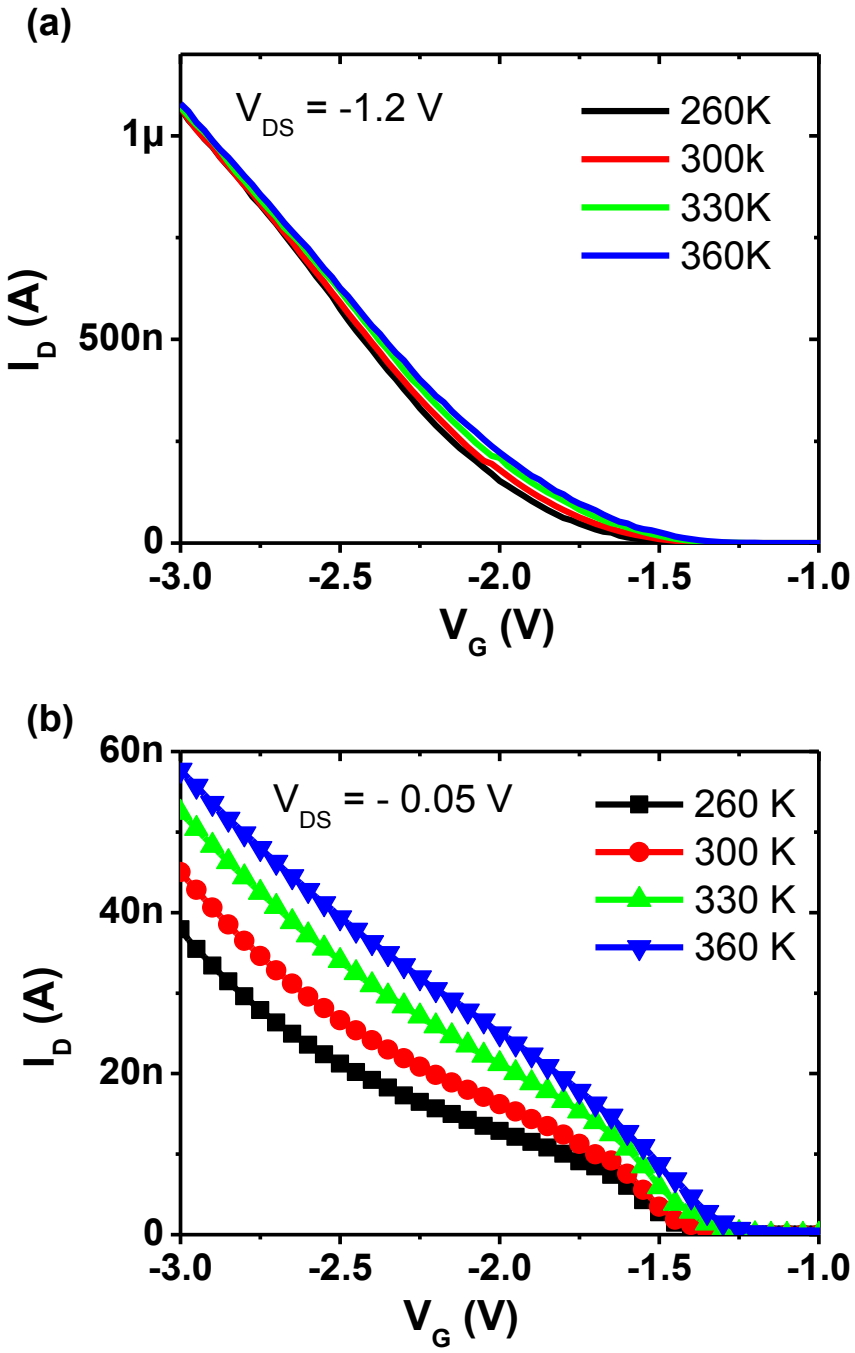

Figure 3.16: The linear plot of the transfer characteristic of a 12.5 nm width 850-nm gate length Si nanowire Schottky barrier MOSFET at temperature from 260 K to 360 K at (a) VDS = -1.2 V and (b) VDS = -0.05 V.

Another interesting phenomenon is that there are two slopes at the electron current branch, indicated by S1 and S2 in the graph. At 300K, the slope of S1

segment is 123 mV/dec while that is 484 mV/dec at S2 segment. As shown in the graph, the slope of S1 segment is temperature independent while the slope of S2 segment is temperature dependent, suggesting that the tunneling current is dominating at S1 segment and thermal emission current is dominating at S2 segment. Referring to the device structure of Si nanowire SB-MOSFETs, the electron current is limited by the Schottky junction at drain side at S1 regime and it is limited by the Schottky junction at source side at S2 regime.

3.7 Effective SBH in Si nanowire SB-MOSFETs

The subthreshold current of SB-MOSFET can be modeled using a thermionic emission equation:

$$I = wA^{**}T^2 \exp(-q\phi_{eff} / KT)[\exp(qV / KT) - 1] \quad (3.6)$$

where w is the physical geometry factor, A^{**} is the effective Richardson constant, k is the Boltzmann constant, T is temperature, and V is the source/drain bias. Equation 3.6 is generally used to derive the effective Schottky barrier height by assuming the current is dominated by thermionic current. In subthreshold regime ($V_G < V_T$), the Schottky barrier becomes thinner as the gate bias increases due to this gate modulation effect. In this process, the contribution of tunneling current will become larger while the contribution from the thermionic current will not change. Thus, the overall current will become less sensitive to the temperature change and the effective Schottky barrier height derived based on equation 3.6 becomes smaller as the percentage of tunneling current becomes larger.

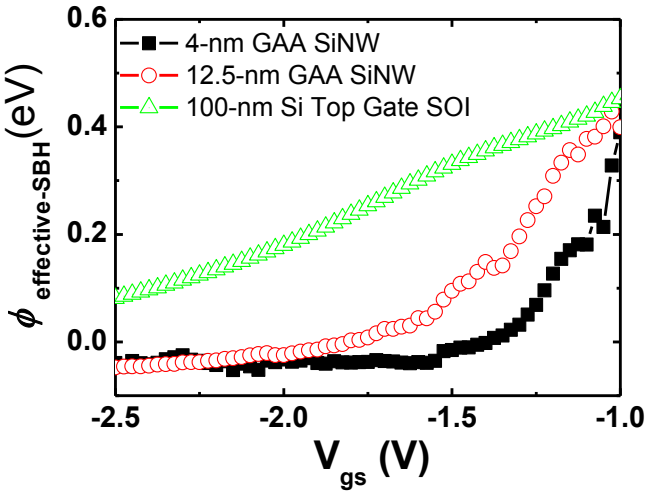

Figure 3.17: the effective Schottky barrier height of a 4-nm-diameter and a 12.5-nm-diameter Si nanowire GAA SB-MOSFET as a function of gate bias.

A series of subthreshold characteristics were measured at 260 ~ 360 K as presented in Fig. 3.16. The effective Schottky barrier height could be extracted from Arrhenius plot based on these data. The extracted effective SB heights from a 4 nm diameter, a 12.5 nm width Si nanowire GAA SB-MOSFETs and a 100 nm thick Si body top-gate SOI SB-MOSFET are plotted as a function of gate voltage as shown in Fig. 3.17. All of the three devices show ~ 0.46 eV effective Schottky barrier height at -1 V gate bias, close to its intrinsic Schottky barrier height. As the gate bias becomes larger (negatively), the effective Schottky barrier height of the 4 nm Si nanowire GAA SB-MOSFET decreases faster than that of the 12.5 nm Si nanowire GAA SB-MOSFET, and the effective Schottky barrier height of the Si nanowire GAA SB-MOSFET decreases faster than that of the top-gate SOI SB-MOSFET. This faster decrease of the effective Schottky barrier height suggests the carrier injection increased faster in the 4 nm Si nanowire than in the 12.5 nm Si nanowire GAA SB-MOSFETs, and faster in Si nanowire GAA SB-MOSFETs

than in top-gate SOI SB-MOSFET due to better gate coupling. This figure shows the tunneling current increases faster in smaller diameter nanowire SB-MOSFET than those larger diameter nanowire and planar SOI SB-MOSFETs.

3.8 Simulation study of the Schottky barrier junction

For a quantitative analysis on the impact of the gate structure over the tunneling current at the on state gate bias, the barrier shape of Schottky junction in top-gate planar SOI and Si nanowire GAA SB-MOSFETs were numerically solved by MEDICI. The gate oxide thickness is 5 nm as confirmed by TEM. The potential profile along the channel surface 2 nm below the gate oxide of top-gate planar SOI device and Si nanowire GAA SB-MOSFETs are plotted in Fig. 3.18. The potential profile of a 4 nm and a 12.5 nm top-gate planar SOI SB-MOSFETs were solved and plotted in the same graph for a fair comparison.

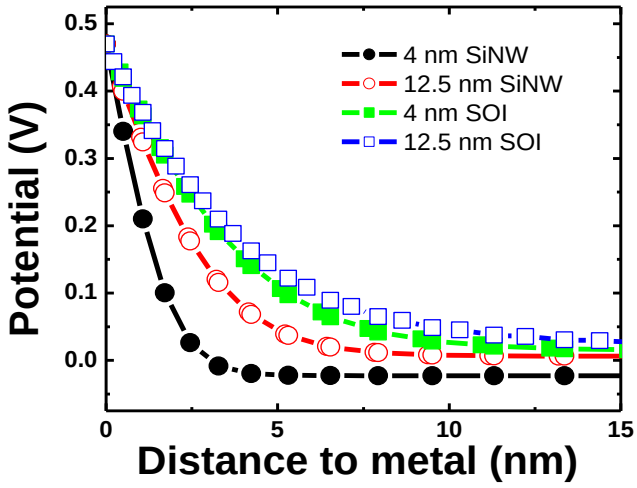

Figure 3.18: Calculated potential profile of the Schottky barrier at on-state. The circle ones represent the Si nanowire GAA SB-MOSFET and the square ones represent top-gate SOI SB-MOSFET.

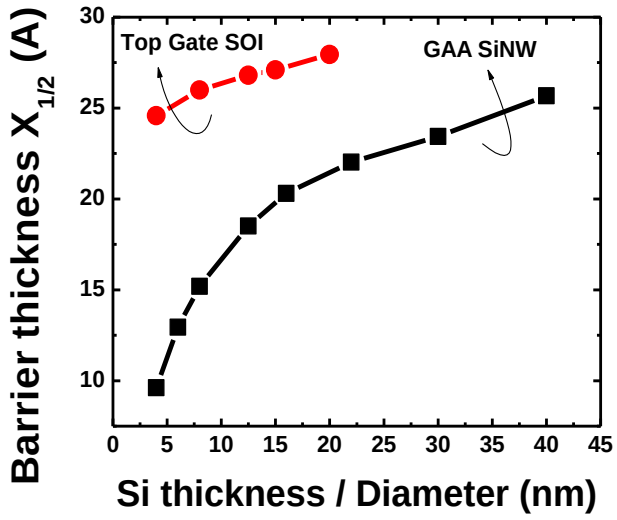

Figure 3.19: Calculated Full-Barrier-Width at Half Maximum (X1/2) as a function of the Si body thickness of top-gate SOI planar devices and Si nanowire diameters.

Since MEDICI is not able to model the tunneling current well, the current flow is not simulated. Simulation results agree with the expectation that thinner body top-gate planar SOI has thinner barrier [112]. An interesting finding is that the Schottky barrier width of the 12.5 nm width Si nanowire junction is thinner than that of a 4 nm top-gate SOI device at the on-state gate bias. This agrees with the experimental data, in which a 12.5 nm Si nanowire device have a SS of ~ 86 mV/dec while the theoretical SS for a 4 nm SOI is larger than 150 mV/dec [114]. The Barrier-Full-Width-at-Half-Maximum (FWHM, $x_{1/2}$) as a function of the SOI body thickness or the Si nanowire diameter is shown in Fig. 3.19. It clearly demonstrates the advantage of Si nanowire GAA SB-MOSFETs in terms of obtaining a thinner Schottky barrier at a given gate bias. Given the exponential dependence of tunneling current on the Schottky barrier width and the enhanced

barrier thinning effect of nanowire GAA transistor architecture, it has been demonstrated for the advantages of Si nanowire GAA MOSFET as an effective architecture to improve the electrical characteristics of SB-MOSFETs.

3.9 Summary and Discussion

Stress retarded oxidation was observed at dry oxidation at 875℃, and top-down Si nanowires with diameter down to 4 nm were fabricated by this technique. With CMOS compatible technology, the Si nanowire with diameter down to 4 nm and gate oxide thickness 5 nm was successfully integrated with GAA nanowire MOSFET architecture and 1-D NiSi Schottky S/D.

Greatly enhanced carrier injection in Si nanowire GAA SB-MOSFETs was demonstrated both by experimental data and quantitative simulation. The enhancement was attributed to the better gate modulation of the Schottky barrier height in Si nanowire GAA device architecture. With the advantage of the Si nanowire GAA architecture, the mid-band gap NiSi SB-MOSFETs achieved SS of 79 mV/dec on a 4 nm Si nanowire device and SS of 86 mV/dec on a 12.5 nm width device at room temperature.

Chapter 4
Ge Nanowire PMOSFETs on Epitaxial Grown Ge Substrate

4.1 Introduction

As described in Chapter 1, replacing conventional heavily doped S/D by metal could potentially be one of the performance boosters for advanced transistors, which is discussed in Chapter 3. In this Chapter, another performance booster, replacing Si channel with high mobility Ge channel, is explored.

Carriers in Ge have lower effective mass and higher mobility compared with Si, which have made Ge one of the promising high mobility channel materials for future nano-scale p-type MOSFETs. Surrounding-gate architecture – GAA and Ω-gate – is known to have superior gate coupling and thus excellent immunity against short-channel effects [27, 31, 32]. Therefore, the surrounding-gate Ge-nanowire (GeNW) MOSFET is of interest due to its combination of the high mobility of Ge and the advantages of the surrounding-gate nanowire architecture.

Table 4.1: Summary of some reported Ge MOSFETs.

	Ref. [55]	Ref. [115]	Ref.[54]	Ref. [53]	Ref. [116]	Ref. [117]
Material	Ge (VLS)	Ge-Ge (VLS)	Ge-Si (VLS)	Ge (VLS)	Ge-SiGe (VLS)	Ge
Structure	Back Gate	Back Gate	Top Gate	GAA	Top Gate	GAA
Dielectric	10 nm SiO_2	60 nm ZrO_2	4 nm HfO_2	4 nm Al_2O_3	10 nm HfO_2	Al_2O_3
Diameter (nm)	20	20	18	~20	36	W=250, H=?
L_G (nm)	5000	1500	190	3000	720	1300
V_{DS} (V)	-1	-2	-1	-1.5	-1	-2.1
$V_G - V_T$ (V)	-2	-2	-0.7	-2	-	~220
I_{ON} (μA/μm)	150	240	2100	~100	56	-
μ($cm^2V^{-1}s^{-1}$)	600	115	730	197	-	-
SS (mV/dec)	300	240	100	120	270	71
I_{MAX}/I_{MIN}	10^3	10^5	10^5	10^5	200	10^5
S/D	Pd	Ti	Ni	Ti	Boron	Boron

Ge nanowire transistors have been demonstrated based on bottom-up technique, in which the wires are synthesized. The first Ge nanowire transistor was reported by D. Wang et al. based on Vapor-Liquid-Solid (VLS) grown Ge nanowires at 2003[55]. At 2004, complementary Ge nanowire transistors were reported by Greytak et al., in which a Ge nanowire nMOSFET was demonstrated for the first time and the I_{on}/I_{off} ratio of Ge nanowire pMOSFET was improved to 5 orders [115]. Xiang et al. at 2006 demonstrated high performance Ge/Si core/shell nanowire transistors [54]. The I_{on} as high as 37 μA at V_{DD} = -1 V was

achieved on a 190 nm gate length 18 nm diameter Ge/Si core/shell nanowire transistor, and the hole mobility achieved 730 $cm^2V^{-1}s^{-1}$. In the subsequent works, sub-100 nm Ge/Si core/shell nanowire transistors were reported with reasonable SS and DIBL[118].

Several other transistor works based on VLS grown Ge nanowires have demonstrated reasonably good device performances [53, 119], and those works are listed in Table 4.1. Those works based on bottom-up approach have demonstrated the great potential of Ge nanowire transistors for high performance applications; however, as discussed in chapter 2, the challenge remains with their integration into circuits due to the lack of process repeatability, device reliability and fabrication throughput, which limit them from commercial applications.

The other approach is the top-down approach, in which the device integration can be as simple as the conventional planar devices. However, the Ge nanowire fabrication remains a challenge in top-down approach. Unlike silicon, there is no self-limiting oxidation effect [68] in Ge, and it makes the Ge nanowire fabrication challenging. Since the nanowire diameter is small and no self-retarded oxidation effect, the Ge nanowire would be easily fully oxidized. The process window of Ge nanowire oxidation is small and it could be one of the issues hindering the progress of Ge nanowire technology using top-down approach. Despite the intensive reports on Ge planar MOSFETs [6, 7, 89], only a few works are reported on SiGe-NW/Ge-beam transistors in top-down approach.

A direct approach of fabricating Ge nanowires in top-down approach is similar to the Si nanowire fabrication process. In this approach, Ge-fins are directly defined on Ge-On-Insulator (GOI) substrate by lithography & dry etch

processes. Then those Ge-fins are trimmed down into Ge-nanowires by oxidation process. The first challenge of this approach is to obtain high quality GOI substrate. A popular way of obtaining GOI substrate is to epitaxial grown SiGe on a SOI wafer with a thin top Si layer, and then transfers the wafer into GOI by Ge condensation. The Ge condensation technique was first introduced by Tezuka et al. [120] in 2001 and it has been intensively studied ever since then [120-126]. The process is described as follows. First of all, an epitaxial SiGe layer is grown on a SOI wafer and then the wafer is subjected to oxidation in furnace. During the high temperature oxidation, Si is selectively oxidized because the formation energy of SiO_2 is much lower than that of GeO_2 (ΔG = -732 kJ/mol for SiO_2 and ΔG = -376 kJ/mol for GeO_2). Furthermore, the solid solubility of Ge in SiO_2 is low; thus, Ge atoms are rejected from the oxide layer and diffuse towards the substrate. The diffusion of Ge is then blocked by the buried oxide layer due to the small diffusion coefficient of Ge in SiO_2. After oxidation, the top thermal oxide layer can be easily removed by using diluted HF and then the SGOI/GOI structure remains. The condensation process is illustrated in Fig. 4.1. Although this approach of the Ge nanowire fabrication process is direct, the Ge condensation process still needs further investigation. The challenges of Ge condensation technique include process condition optimization, Ge balling up issue due to high Ge content, amorphization due to oxidation at inappropriate temperature[127], self limited oxidation behavior, SiGe melting due to the low melting point of Ge and Ge loss due to formation of volatile GeO [127-135].

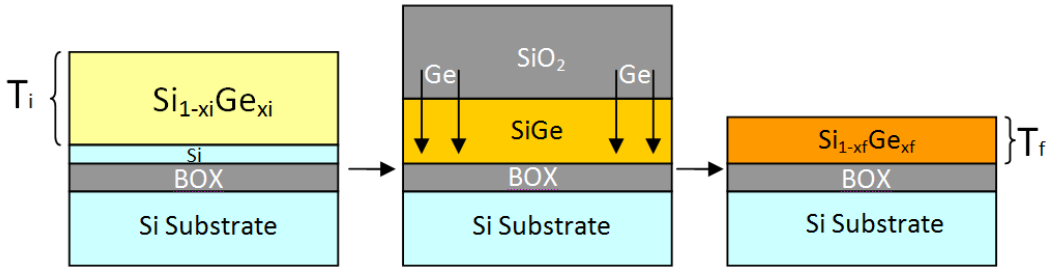

Figure 4.1: Schematic illustration of Ge condensation technique. T_i is the initial SiGe thickness and T_f is the final SiGe/Ge thickness.

Another proposed Ge nanowire fabrication technique is utilizing two/three dimensional Ge condensation, which is shown in Fig. 4.2. At 2008, T. Irisawa et al. have reported SiGe-NW MOSFETs with Ge content as high as 92% by utilizing three-dimensional Ge condensation technique [136]. In that work, the transconductance of SiGe nanowire with 92% Ge is much lower than that of the other SiGe nanowires with lower Ge concentration, and it is attributed to the higher defects in the SiGe nanowire with higher Ge concentration (>80% Ge percentage). At 2009, Balakumar et al. have reported SiGe nanowire formation with Ge content as high as 95% by the same technique [137], but no transistor work is reported.

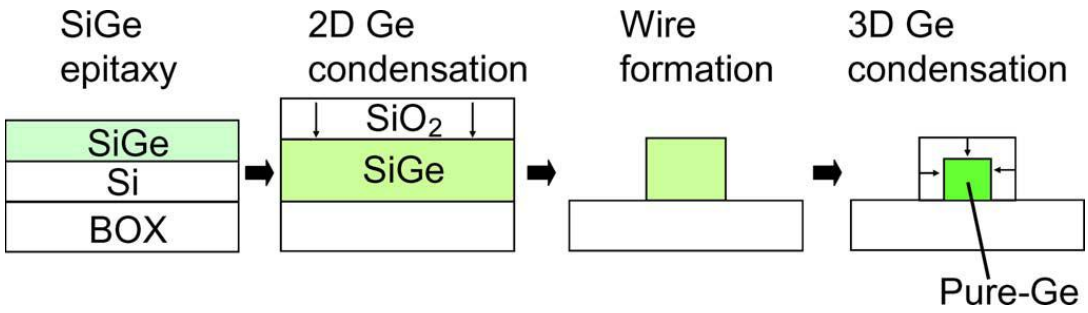

Figure 4.2: Schematic illustration of proposed fabrication procedures for Ge nanowire. Two/three dimensional Ge condensations are properly utilized [10].

Besides the possible heavy defects in the Ge nanowires, another challenge of fabricating Ge nanowires by two/three dimensional Ge condensation technique is the bending of Ge nanowires. Since Ge lattice is larger than that of Si, the replacement of Si atoms with Ge atoms in the fin/wire would lead to compressive stress. The compressive stress could not be released along the fin/wire as its two ends are anchored to the substrate. As a result, the wire bends when the accumulated compressive stress is over certain critical value. Fig. 4.3 shows the SEM image of a SiGe nanowire after two/three dimensional Ge condensation and oxide strip. The wire is found to be bended and it makes device fabrication based on this bended nanowire problematic. Probably, this is one of the reasons of no further report on pure Ge nanowire works based on this technique.

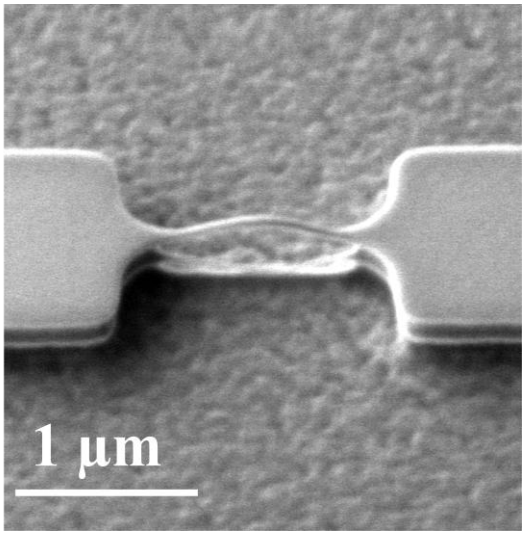

Figure 4.3: 45^{o} tilted SEM image of SiGe nanowire after three-dimensional Ge condensation and oxide strip. The nanowire bends due to large compressive stress induced by the replacement of Si atoms with Ge atoms.

At 2008, J. Feng et al. reported a technique to form local GOI substrate by rapid melt growth (RMG) technique and demonstrated a gate-all-around Ge-beam

pMOSFET with beam width × height ~ 250 × 75 nm based on that local GOI substrate [117]. However, no further works on Ge nanowire MOSFETs is reported yet and further investigation on this approach is needed.

In this chapter, a new top-down technique of Ge nanowire fabrication on epitaxial-grown Ge substrate is presented. Ge nanowires with diameter down to 14 nm are demonstrated and integrated into pMOSFETs with HfO_2/TaN gate stack.

4.2 Ge nanowires on epitaxial Ge substrate

4.2.1 High-quality Ge epitaxial growth on Si substrate

A high quality Ge epitaxial growth on Si substrate process is an essential part of this project. It is developed [138] and carried out in Institution of Microelectronics, Singapore. The Ge epitaxial growth is conducted in a cold wall ultra high vacuum chemical vapor deposition (UHV-CVD) epitaxial reactor, with a base pressure of 7×10^{-9} Torr. Right before loading the wafer into the chamber, the wafer was cleaned in SC1 ($NH_4OH : H_2O_2 : H_2O = 1 : 2 : 10$) for 10 minutes and diluted HF (1:200) for 2 minutes to clean the wafer and remove the oxide. The epitaxial-growth started with an ultra high vacuum annealing at 780 ℃ for 180 seconds, and then a few nanometers Si was epitaxial grown at 530 ℃ for 65 seconds. Next, ~ 30 nm SiGe buffer layer was grown at ~ 370 ℃ for releasing stress between the Si substrate and the Ge epitaxial layer. The Ge percentage in SiGe buffer layer increases as it grows by increasing GeH_4 gas flow rate. After that, ~ 30 nm Ge seed layer was grown at the same temperature. Finally, the temperature was raised to 550 ℃ for a high quality Ge layer growth. The GeH_4 gas flow is 240 sccm and the pressure is between 10^{-6} and 10^{-3} Torr.

In this process, the SiGe buffer layer as well as the Ge seed layer grown at low temperature of ~ 370 ℃ is to release the strain and confine the dislocations. Fig. 4.4 shows the high resolution transmission electron microscopy (HR-TEM) image. No obvious threading dislocation to the Ge surface can be observed and the surface defect density is characterized to be ~ 6 $\times 10^6$ /cm^2.

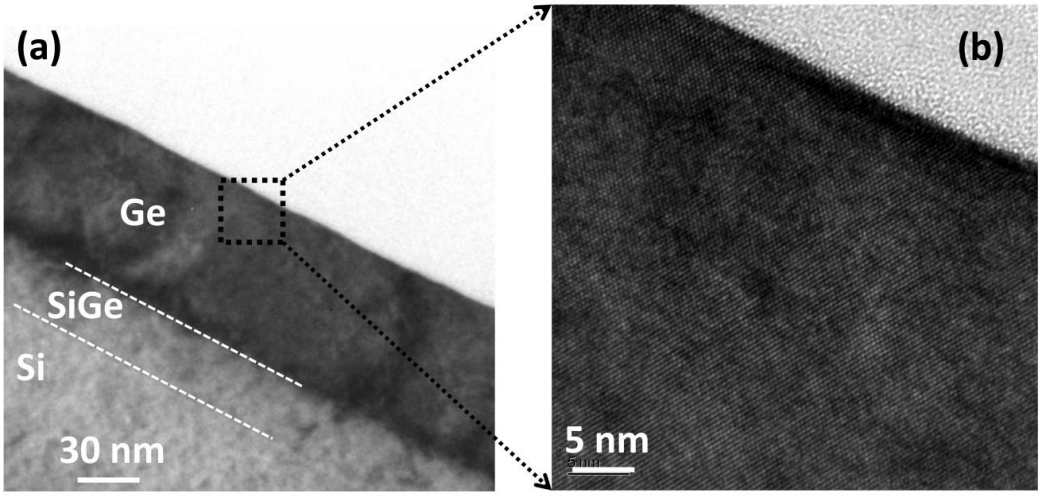

Figure 4.4: HR-TEM image of cross sectional view of Ge epitaxial grown on Si with ~ 30 nm SiGe buffer layer. The left side is the zoomed in view of the surface Ge lattice.

4.2.2 Ge nanowires fabrication on epitaxial Ge substrate

The fabrication process started with 8" SOI wafer having 70 nm thick top Si layer. The Si layer was thinned down to ~ 25 nm by cyclic thermal oxidation and oxide wet etching processes. A high quality strain-relaxed Ge layer (~ 100 nm) was grown as described in section 4.2.1.

The lateral Germanium nanowire fabrication started with the active area patterning. The active area, consisting of a narrow fin pattern connected to wider extension pads, was printed using alternating phase shift mask lithography in a KrF scanner (wave length 248 nm). The initial coated resist thickness was 3200 Å,

after exposure and resist development, the resist fin height was ~ 2700 Å and the fin CD was ~ 125 nm after lithography. The fin resist was trimmed in O_2 plasma to reduce the fin width to 60 nm. A two-step etching with polymerization in between was then used to transfer the resist patterns into the Ge layer. In the 1st etching step, the Ge was partially etched (~ 60 nm) by CF_4 : O_2 plasma. The recipe was fine tuned to have a straight etch profile. Since there is no etch stop layer, this step is controlled by time. As schematically illustrated in Fig. 4.5 using top view and cross sectional view drawings, the partial dry etching of Ge layer resulted in square (~ 60 nm × 60 nm) Ge-fins (Fig. 4.5 (a)). It was followed by a passivation phase with thin polymer deposition in the same etching chamber using C_4F_8 gas and a 2nd etch step which was an isotropic plasma etch to undercut the Ge fins laterally. The process parameters are listed in table 4.2.

Table 4.2: Process parameters of the passivation and isotropic etch in the Ge nanowire formation process.

	Passivation Phase	**Etch Phase**
Gas	C_4F_8 : 160 sccm	SF_6 : 100 sccm C_4F_8 : 30 sccm O_2 : 10 sccm
Pressure (mTorr)	1.2	1.2
Platen Power (W)	0	14
Coil Power (W)	600	600
Time (s)	7	14

The passivation and isotropic etch step transformed the Ge-fins into Ge-beams (Fig. 4.5 (b)). The power of the isotropic etching was optimized so that the Ge-fin sidewall remains protected by the polymer while the flat bottom was cleared for further etch. The encroachment below the Ge-fins was controlled by the isotropic etching time so that it was long enough to transfer the Ge-fins into Ge-beams while having little impact on the relatively wider Source/Drain (S/D) pads (Fig. 4.5 (b)). Lastly, the photo-resist was striped by O_2 plasma and Ge-beams are formed. The dimension of Ge beams depends on the initial fin width, the anisotropic and the successive isotropic etch rate, as well as the protecting polymer thickness. It is challenging to control the variability of these factors from experiment to experiment. In this work, the dimension variability of Ge beams was compensated by the following cyclic Ge oxidation process.

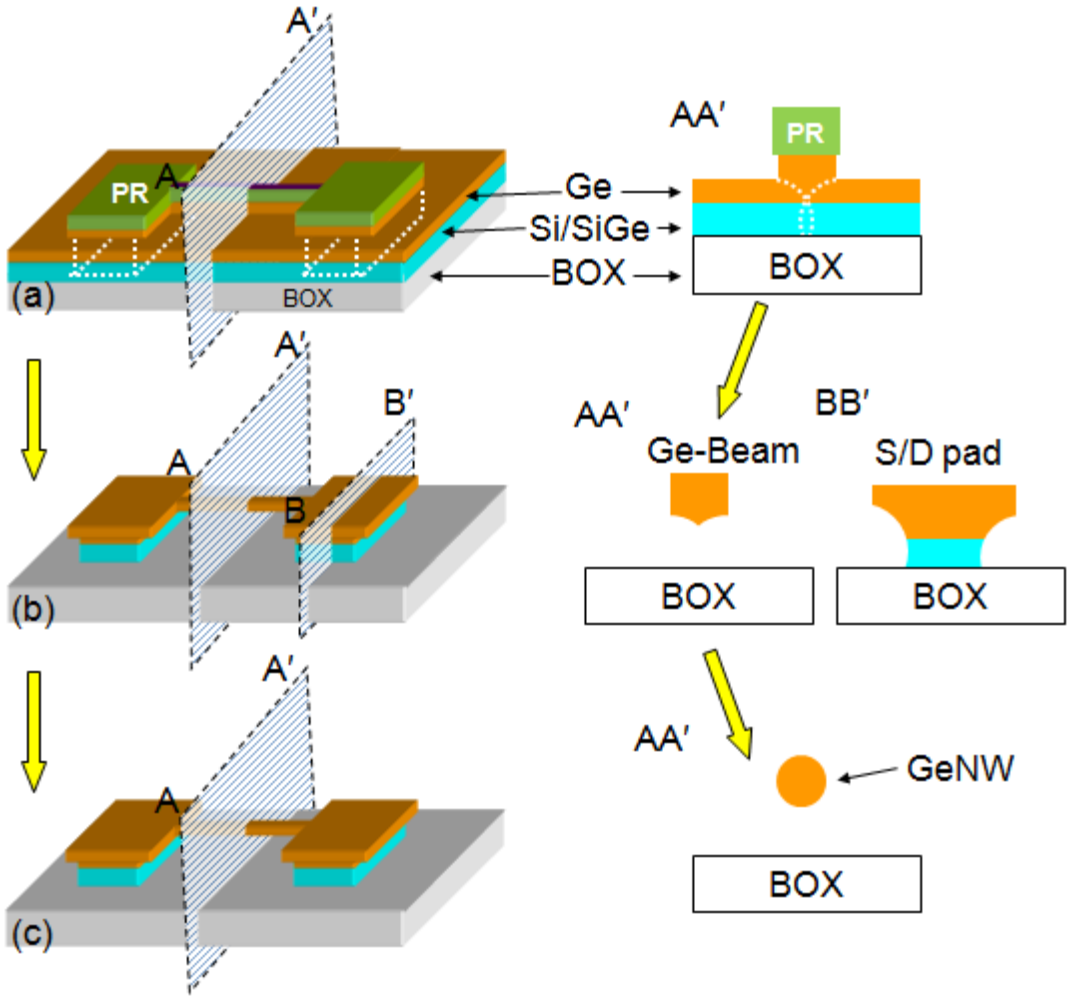

Figure 4.5: Schematics of the Ge nanowire formation process flow. (a) After fin patterning, photoresist trimming and anisotropic Ge etching. The dotted line indicates the consequential isotropic etching profile. The starting material is Ge (~100 nm) / SiGe (~30 nm) / Si (~25 nm) on BOX. (b) After isotropic etching and photoresist striping. The bottom Ge and SiGe/Si buffer layer are totally removed. (c) After cyclic thermal oxidation and wet etching of Ge oxide. The suspended Ge-beam is trimmed down to Ge nanowire. The left hand side is the 3-D schematics and the right hand side is the corresponding cross-sectional view.

After stripping photo-resist, the Si wafers normally will go through piranha and SC1 for cleaning the photo-resist and etch residues. However, both of these two chemicals attack germanium. In this project, only diluted HF was used

to clean the Ge wafer. After diluted HF clean, polymer over large area still could be observed over the wafer. Therefore new chemicals are needed for improved cleaning and surface preparation. In this project, it was found that the oxidation plus wet-etching processes could help to clean the wafer, possibly because the carbon based polymer and the substrate Ge could be oxidized at high temperature and consequentially be removed by the diluted HF dip. The wafer looks clean under SEM. However, two possible issues remain: (1) the resolution of the SEM in our lab is ~ 10 nm, so it is not high enough to confirm whether the surface is completely cleaned for high quality gate oxide formation; (2) although the polymer could be removed by the oxidation & wet-etching processes, the Ge surface becomes rougher as the polymer residues would be a sacrificial oxidation structures and thus affecting the local Ge oxidation.

Fig. 4.6 shows the tilted-view SEM image of the fabricated suspended Ge-beam connected to S/D pads after cleaning. It could be observed that the Si and SiGe buffer layers between the Ge-beam and the buried oxide were etched away during the isotropic etching process. At the end, the suspended Ge-beams were trimmed down to form Ge nanowires by cyclic rapid thermal oxidation at 500 ℃ and wet etching of Ge oxide (Fig. 4.5(c)).

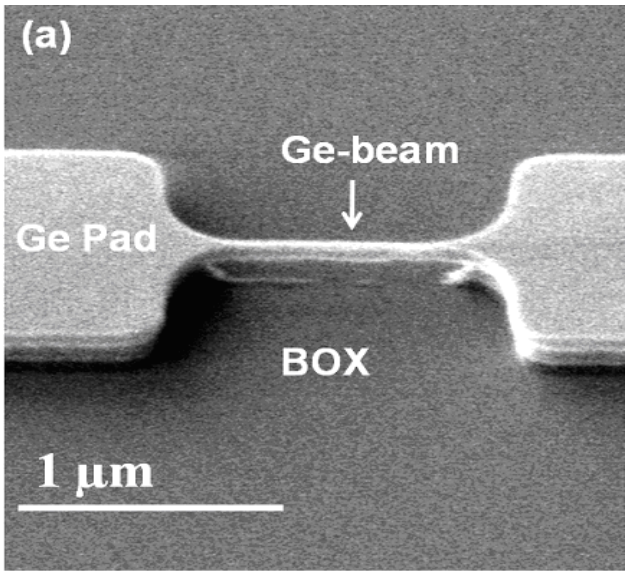

Figure 4.6: 45^{o} tilted SEM image of Ge-beam after beam formation and photoresist strip. The bottom SiGe buffer layer as well as the thin Si layer on BOX is totally removed.

This technique could be used to fabricate both Si and Ge nanowires. Besides single nanowire formation described above, multi-stacked nanowires could be fabricated by simply repeating the two-step etching processes. Fig. 4.7 shows the SEM image of a stacked three nanowires after repeating the two-step etching 3 cycles. Moreover, the beam size could be controlled by adjusting the isotropic etching time, so that certain nanowires could be thin and destroyed intentionally. This gives the flexibility of controlling the vertical position of nanowires as shown in Fig 4.8.

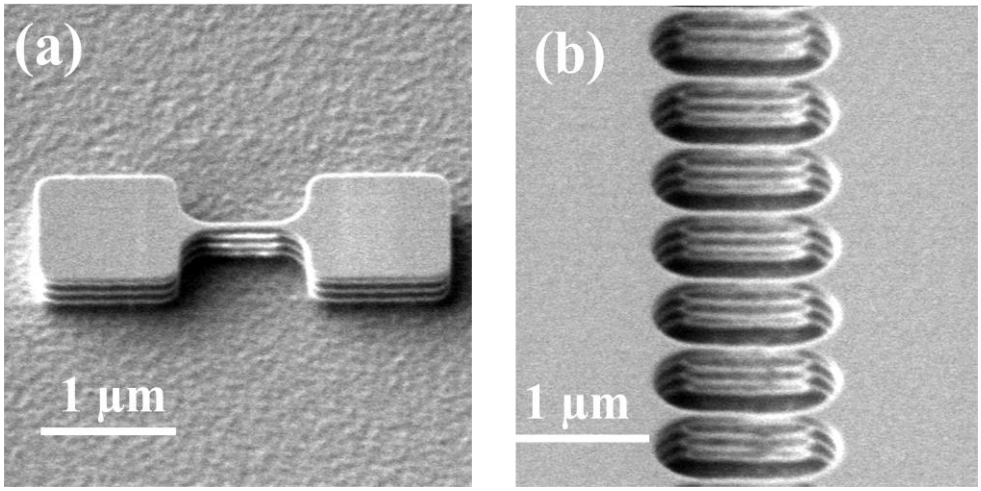

Figure 4.7: 45^{o} tilted SEM image of multi-stacked nanowires formed by repeating the two-step etching processes on testing Si wafer with (a) a single fin mask and (b) an array of fin mask.

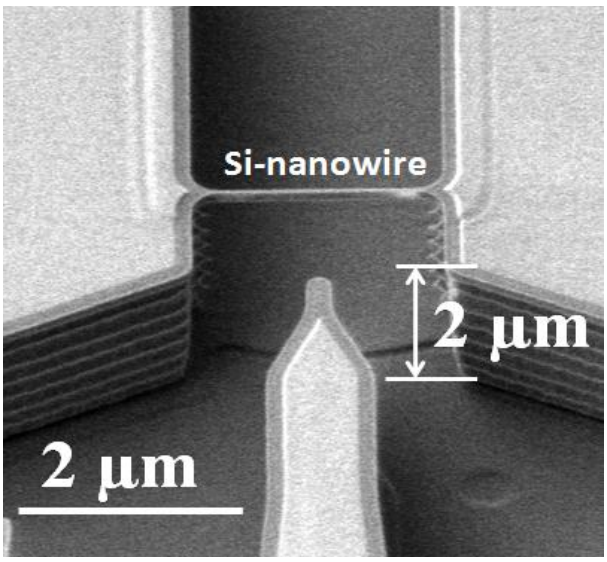

Figure 4.8: 45^{o} tilted SEM image of multi-stacked nanowires formed by repeating the two-step etching processes on testing Si wafer.

4.2.3 Ge surface roughness after Ge nanowire formation processes

It is difficult to directly characterize the Ge nanowire surface roughness as the nanowire surface itself is curved. Therefore, the surface roughness

investigation is conducted on planar Ge as a reference. All the process conditions, such as the RF power, gas flow and pressure are kept exactly the same to make sure the results relevant to the Ge nanowire surface roughness. The longest isotropic etch time in the experiment is set to be 15s to simulate the worst scenario. The process parameters and the surface roughness root mean square (RMS) of each split are shown in table 4.3. The surface roughness is characterized by atomic force microscope (AFM).

Table 4.3: Splits condition and results of the Ge surface roughness investigation.

Processes	**Description**	**Surface RMS**
epitaxial grown Ge		4 Å
Isotropic etch	2s passivation + 5s isotropic etch	6 Å
Isotropic etch	2s passivation + 15s isotropic etch	48 Å

The Ge surface roughness RMS is 4 Å before the two-step etch process. It becomes 6 Å after 5 sec isotropic etch and 48 Å after 15 sec isotropic etch. This result indicates that the Ge nanowire has severe surface roughness issue. The RMS is not proportional to the isotropic etch time possible because of the time needed to break though the carbon polymer layer. The surface roughness come from both of the isotropic etching and the oxidation & wet-cleaning processes.

4.3 Ge nanowire pMOSFETs fabrication

After the Ge nanowire formation processes, a 10 s rapid thermal oxidation process at 500 ℃ at one atmospheric pressure was employed to grow GeO_2 ~ 6.8 nm, followed by ~ 11 nm HfO_2 deposition by atomic layer deposition (ALD) system to form the gate dielectric. TaN was deposited by sputtering system to form the gate electrode. As shown in Fig. 4.9 (a), the TaN deposited on the top of a nanowire is not connected to the TaN deposited on the substrate as a result of the anisotropic deposition nature of the sputtering system. Simply increasing the thickness of TaN was not able to solve this problem as the shading area grows with the TaN thickness as shown in Fig. 4.9(b). In this project, an initial TaN layer ~ 800 Å was deposited first, then 500 Å USG was deposited and etched to form oxide spacer as shown in Fig. 4.9(c). Finally, another layer of ~ 300 Å TaN was deposited to connect the TaN on the top of the nanowire and the TaN on the substrate (Fig. 4.9(d)). Next, gate pattern was transferred into the TaN layer. Fig. 4.10(a) is the SEM image of the transistor after TaN gate patterning. Next, the source and drain were implanted with $BF_2/4\times10^{15}$ cm^{-2}/20 KeV. It was followed by dopant activation at 600 ^oC for 10 s in N_2 ambient. Standard metallization process was done and Fig. 4.10(b) is the SEM image of the transistor after metal line patterning. The fabrication was finally completed with a sintering process in forming gas at 400 ^oC for 30 min.

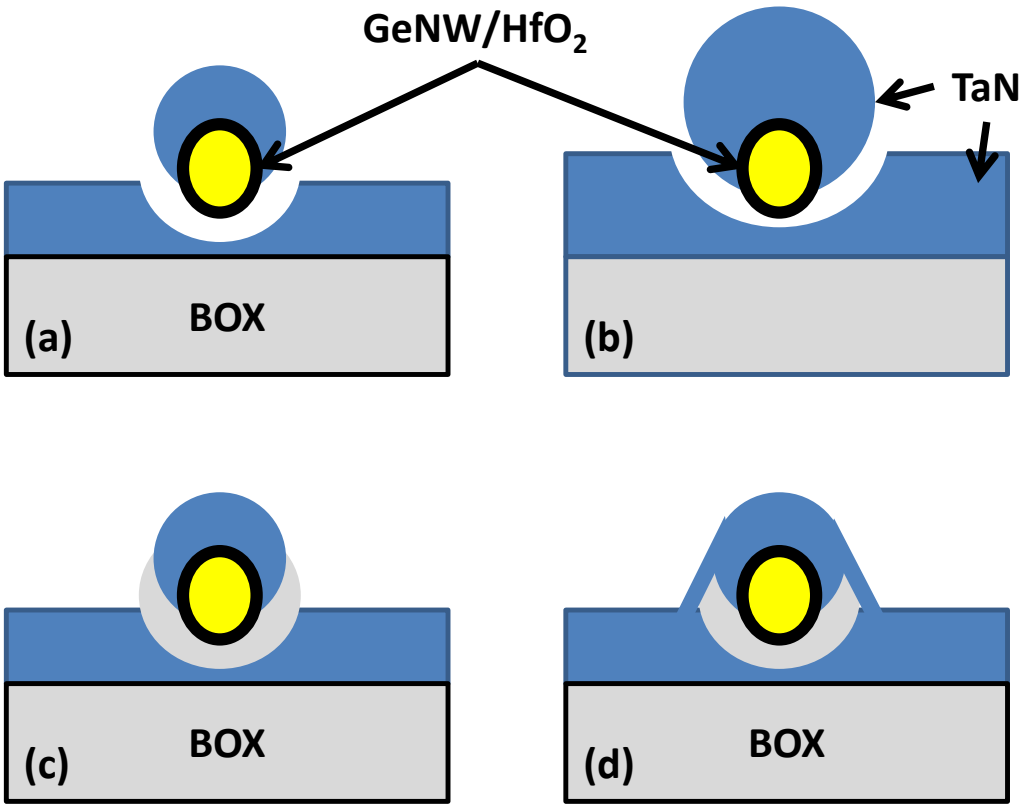

Figure 4.9: Schematics of (a) thin TaN layer deposition and (b) thick TaN layer deposition in sputtering system. (c) Schematic after undoped silica glass (USG) spacer formation and (d) schematic after spacer formation and another thin TaN layer deposition.

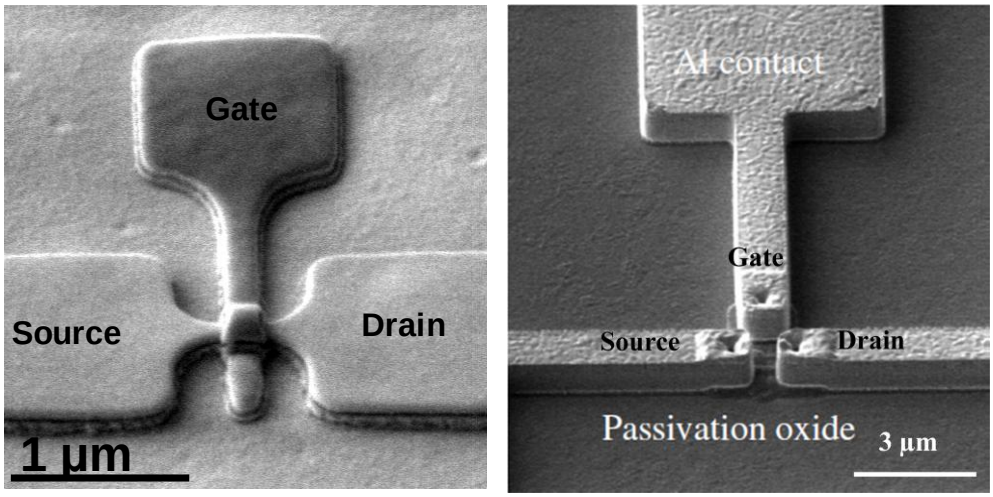

Figure 4.10: SEM image of Ge nanowire transistor (a) after TaN gate etch and (b) after Al contact etch.

4.4 Device channel TEM characterization

The fabricated devices were physically analyzed using scanning transmission electron microscope (STEM). Fig. 4.11 is the STEM image of the channel of the device perpendicular to the wire length through the gate extension. Interestingly, no material was found in the area where Ge-GeO_2 Core-Shell (C/S) structure should be (Fig. 4.11). It was possibly due to the dissolution of GeO_2 ring in the environmental moisture during sample preparation, which caused the Ge wire core to fall out. Therefore, we analyzed the GeO_2 thickness on the S/D planar areas using TEM and found it to be 6.8 nm at the <100> surface. Although GeO_2 shell thickness is expected to be orientation dependent, difference may not be much for initial few nanometers. The width × height of Ge-GeO_2 core-shell structure is 22.9 nm × 31.8 nm as shown in Fig. 4.11; thus, that of the Ge nanowire is 9.3 nm × 18.2 nm after deducting the 6.8 nm GeO_2 shell thickness from the two sides. For simplicity, the Ge nanowire is assumed to be circular with a diameter of 14 nm. Conformal ALD HfO_2 (~ 11 nm) was observed. In Fig. 4.11, the dark area between the Ge nanowire and the TaN on the BOX is a void during the gate formation processes, as explained in section 4.3.1. High resolution STEM image shows that the TaN gate electrode covers ~ 82% of the HfO_2/GeO_2/Ge nanowire gate stack, forming a Ω-gated MOSFET structure.

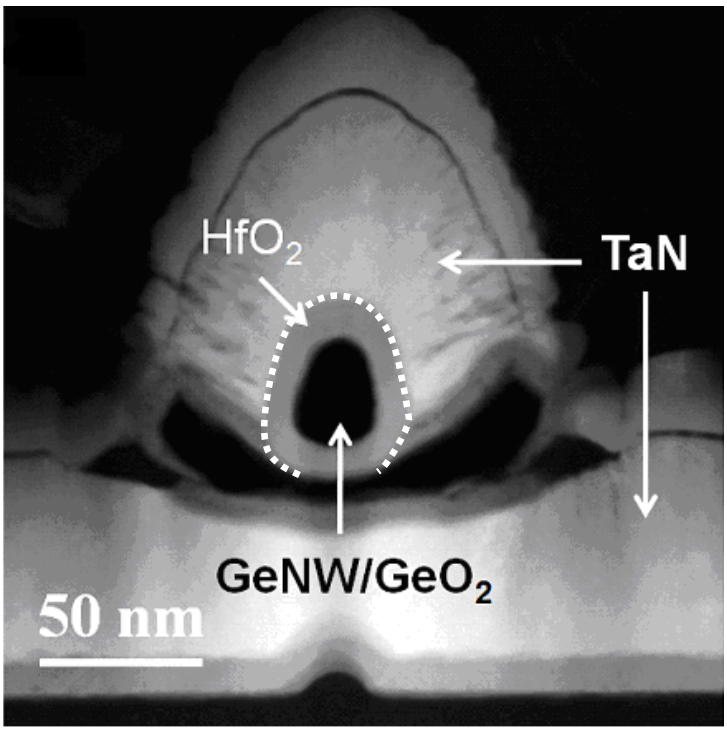

Figure 4.11: Cross-sectional STEM image of Ω-gated Ge nanowire with ~ 6.8 nm GeO_2 shell. GeNW/GeO_2 core/shell is 22.9 x 31.8 nm. The Ω-shaped dotted line is the interface between TaN and HfO_2 dielectric.

4.5 Ge nanowire pMOSFETs I-V characteristics

4.5.1 The Ge nanowire transistor performance

Fig. 4.12 shows the measured transfer and output characteristics of a Ge nanowire Ω-gated MOSFET. The Ge nanowire cross sectional view is shown in Fig. 4.11 and gate length is 300 nm. The I_{ON} of the Ge nanowire Ω-gated MOSFET is 1.98 μA at $V_G - V_T$ = -1.2 V, which is 45 μA/μm after normalization by perimeter. Although lightly-doped-drain (LDD) implantation was not conducted in this work to minimize the peak electrical field near the drain, the $I_{OFF,MIN}$ of the Ge nanowire Ω-gated MOSFET still achieved 0.52 pA even at V_{DS} = -1.2 V, which translates to 12 pA/μm after normalization by perimeter, and the

I_{ON}/I_{OFF} ratio achieved ~ 10^6 even at V_{DS} = -1.2 V. The SS of the Ge nanowire Ω-gated MOSFET is ~ 92 mV/dec at V_{DS} = -0.05 V, which is poorer than the ideal SS of 60 mV/dec.

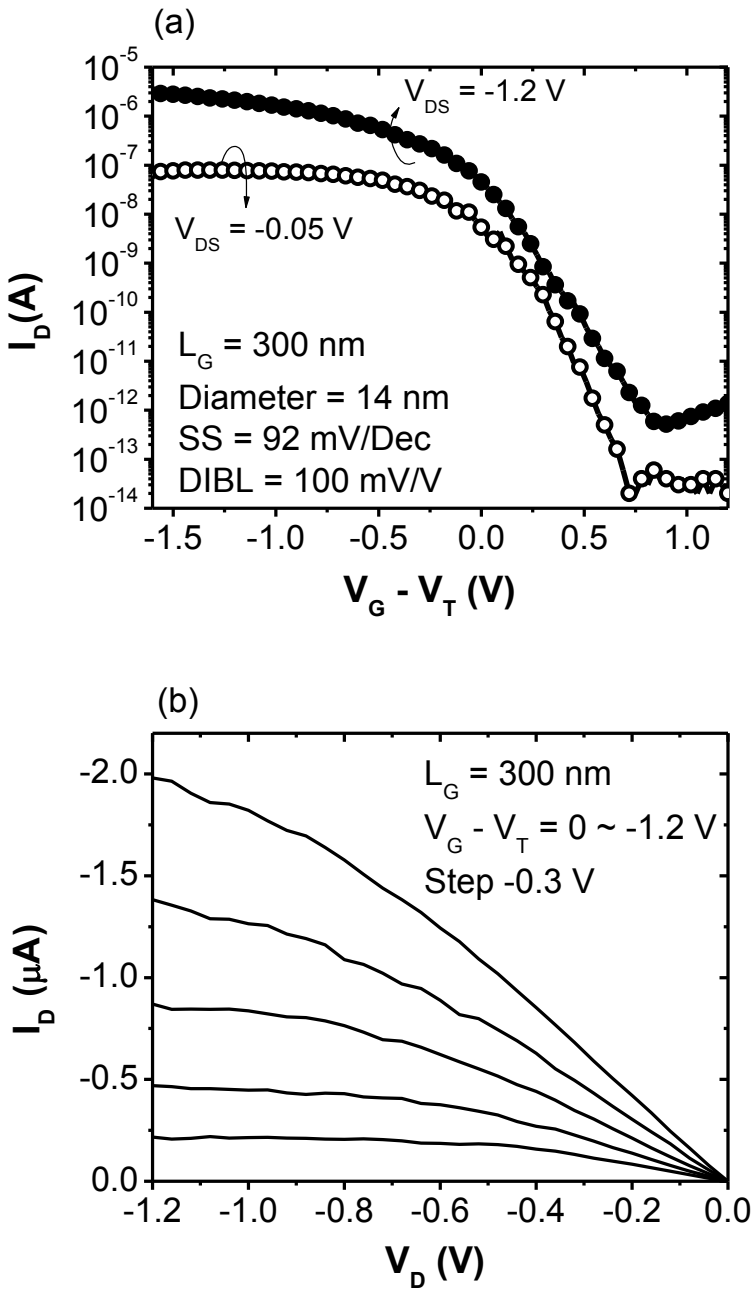

Figure 4.12: (a) I_D-V_G and (b) I_D-V_D characteristics of an Ω-gate GeO_2 shell GeNW transistor. The diameter of the GeNW is 14 nm and the gate length is 300 nm. GeNW is covered with 6.8 nm GeO_2 shell and 11 nm HfO_2 dielectric.

4.5.2 S/D resistance

Fig. 4.13 shows the total resistance of the Ge nanowire pMOSFETs at various gate lengths at the gate overdrive of -1.2 V. The estimated parasitic series resistance is ~ 360 KΩ, which is 15.8 KΩ-μm if normalizing by its perimeter. This parasitic series resistance is much larger than the required 0.2 KΩ-μm for the state-of-the-art devices, possibly due to no germanide process at the S/D pads. The large series resistance issue is solved by an additional implantation and nickel-germanidation process through the contact holes as presented in chapter 5.

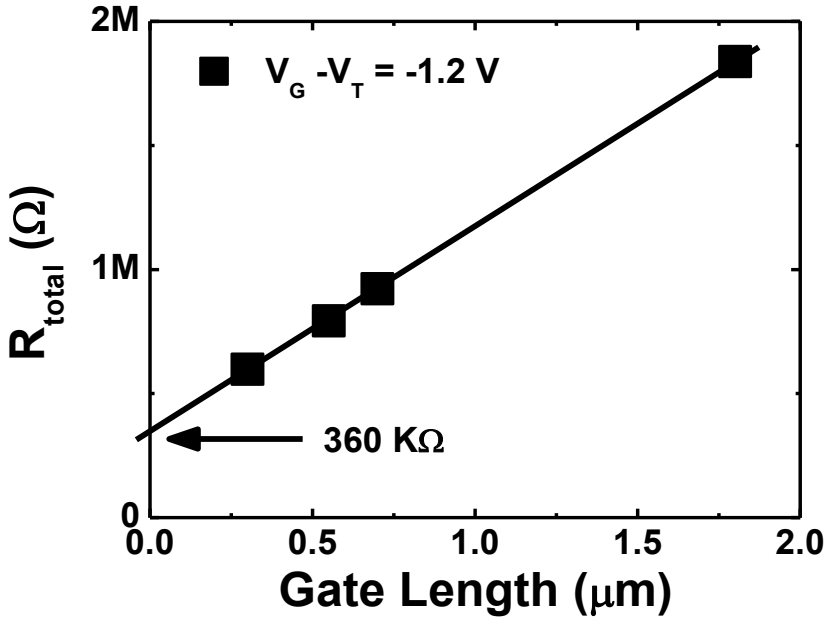

Figure 4.13: Total resistance of the Ge nanowire MOSFETs as a function of gate length at gate over drive of -1.2 V. The parasitic series resistance is extracted by linear extrapolating the total resistance to zero gate length.

4.5.3 Hole mobility characterization

Since the gate surface area is small (C_{area} ~ 14π × 300 nm^2), it is difficult to measure the gate capacitance using the split C-V method. Thus a calculated gate capacitance is used to estimate the mobility in this work. Assuming the

structure of an ideal core-shell cylindrical structure, where the capacitance of each one can be calculated using the formula:

$$\frac{C_G}{L_G} = \frac{A*2\pi\varepsilon_0\varepsilon_r}{\ln\left[{(r+T_{ox})}/{r}\right]} \quad (4.1)$$

where A = 82%, stands for the coverage of the Ω gate, C_G is the gate capacitance, L_G is the gate length, r is the radius of inner cylinder, T_{ox} is the dielectric thickness, ε_0 and ε_r are the permittivity of the vacuum and the relative permittivity of the gate dielectric. Confirmed with the STEM characterizations, the diameter of the Ge nanowire is 14 nm, the thickness of HfO_2 is 11 nm and the thickness of GeO_2 is 6.8 nm. The gate capacitor consists of the quantum capacitance, the capacitance of GeO_2 shell and the capacitance of HfO_2 shell.

Quantum capacitance is not a significant portion of the total gate capacitance as the diameter of 14 nm is not considered to be small enough [139]. Similar to Si-nanowire[140], it is reported that significant quantum confinement effects can be observed only when the Ge nanowire diameter is smaller than 5 nm[141]. Thus, the ideal cylindrical capacitance is reasonably accurate at the estimation of the gate capacitance of Si nanowires MOSFETs with nanowire diameter down to 9 nm [42]. Without considering the quantum capacitance, the capacitance can be calculated based on the two series connected cylindrical dielectric shells and it can be calculated as:

$$C_G = \frac{1}{({}^{1}/_{C_{GeO_2}} + {}^{1}/_{C_{HfO_2}})}, \quad (4.2)$$

If we take ε_{HfO2} as 20 and ε_{GeO2} as 7, then the gate capacitance is 3.672×10^{-12} F/cm.

The carrier mobility in the nanowire channel could be estimated by [63]

$$\mu_{eff} = \frac{G_m * L_G^2}{C_G * V_{DS}} \quad (4.3)$$

With the calculated C_G and $G_{m,max}$= 0.14 μS at V_{DS} = -0.05V after parasitic series resistance correction, the hole mobility in the Ge nanowire is calculated and plotted in Fig. 4.15. The peak hole mobility of ~ 22 $cm^2/V*s$ in a Ge nanowire is much lower than that of reported planar Ge MOSFETs [6, 7]. The reasons are the high channel/gate interface trap density and the channel surface roughness. The surface roughness is explained in section 4.2.3, and can be improved by epitaxial grown Si shell over Ge nanowire as presented in chapter 5.

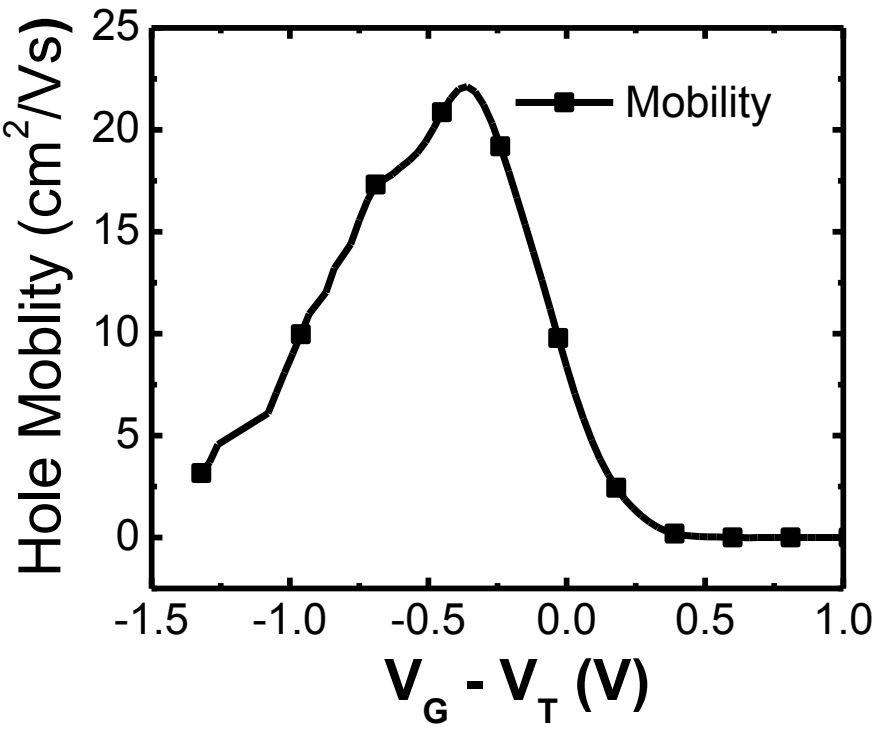

Figure 4.14: Hole mobility in a Ge nanowire as a function of the gate over drive. The peak mobility is ~ 22 $cm^2/V*s$ after S/D resistance correction.

4.5.4 Interface state density

The interface state density D_{it} can be estimated by

$$SS = \frac{kT}{q} * ln10 * (1 + \frac{C_D + C_{it}}{C_G}) \quad (4.4)$$

where SS is subthreshold slope, C_D is depletion capacitance, C_{it} = q*D_{it} is capacitance induced by interface state [142] and other symbols stand for their normal meaning. For the Ge nanowire MOSFET in this work, (kT/q)*ln10= 60 mV/dec at room temperature, SS = 92mV/dec and C_D = 0 (fully depleted body), so the D_{it} can be derived to be 2.73 *x* 10^{12} cm^{-1}*eV^{-1}.

4.6 Discussion

Besides the large parasitic series resistance, the low hole mobility is the main reason of the low drive current. The low mobility could be attributed to the fabrication processes. The first reason is the poor surface cleaning after Ge-beam formation, as the carbon based polymer formed by C_4F_8 plasma in Ge beams formation process cannot be effectively cleaning due to the lack of proper chemicals. The polymer residues before the GeO_2 gate stack formation possibly result in relatively high interface state density, which lowers the carrier mobility by Coulomb scattering. The second reason of low carrier mobility is the channel surface roughness, which are inherited from both the isotropic etching and the cleaning processes during wire formation. This Ge nanowire surface morphology issue could be improved by H_2 annealing as presented in chapter 5.

4.7 Summary

In this chapter, we dealt with the issues of the Ge nanowire fabrication on an epitaxial grown Ge layer using fully CMOS compatible top-down technology. Utilizing a two-step dry etch process scheme – anisotropic etch followed by isotropic etch with polymerization in between – followed by sacrificial oxidation, Ge nanowires down to 14 nm in diameter/width were fabricated on a high quality epitaxial Ge layer. Multi-stacked Ge nanowires are also demonstrated by this two-step etching processes. Ge nanowire pMOSFETs integrated with HfO_2/TaN gate stack demonstrate the I_{on}/I_{off} of 6 orders even at V_{DS} = -1.2V. The large parasitic series resistance suggests the S/D engineering needs to be optimized. The low mobility of the Ge nanowire MOSFETs was attributed to two reasons: the lack of proper chemicals for Ge surface cleaning and the Ge nanowire surface roughness. Possible solutions of the surface roughness problem will be explored in chapter 5.

Chapter 5
Ge/Si Core/Shell Nanowire PMOSFETs

5.1 Introduction

In chapter 4, Ge nanowires were fabricated on an epitaxial grown Ge layer and integrated into pMOSFETs. However, the parasitic series resistance is large (15.8 kΩ-μm) and the hole mobility is low (22 $cm^2V^{-1}s^{-1}$). The low carrier mobility is partially attributed to the surface roughness inherited from the Ge nanowire fabrication processes. In this chapter, Si epitaxial growth over the Ge nanowire is explored as a technique to reduce the Ge nanowire surface roughness. The hole mobility in the Ge nanowire channel is found to be significantly improved after the integration of an epitaxial-Si shell over the Ge nanowire. Additionally, the large parasitic series resistance is reduced by an extra implantation and nickel-germanidation process through the contact holes. With these two improvements, high performance Ge/Si core/shell nanowire pMOSFETs integrated with HfO_2/TaN gate stack are achieved.

5.2. The epitaxial-Si shell on a Ge nanowire

5.2.1 Process qualification of the epitaxial-Si shell on a Ge nanowire

Since the nanowire surface has different lattice orientation, the surface energy is difference for Ge atom epitaxial growth. So it is necessary to qualify the process of the Si epitaxial growth over Ge nanowires to check the feasibility, lattice quality and uniformity of an epitaxial Si-shell. This qualification was done on a testing run of Ge nanowire structure and the Si epitaxial growth process is described in the next paragraph.

After forming Ge nanowires by the two-steps etch process described in chapter 4, the wafer was cleaned in diluted HF (1:200) for 2 min right before the Si epitaxial growth process. The Si epitaxial growth was started with a 2 minutes annealing in a cold wall ultra-high vacuum epitaxial reactor at a pressure less than 3.7×10^{-6} Torr to dissolve the native Ge oxide at 500 ℃. Then the chamber temperature was reduced to 450 ℃ and flow 24 sccm Si_2H_6 gas to epitaxial grow Si. Lower process temperature is desired because of the following two benefits: (1) lower Si growth rate for better thickness control of the ultra-thin Si shell; (2) minimizing the inter-mixing of Si and Ge inter-diffusion for better interface quality. Thus a lower Si epitaxial growth temperature of 450 ℃ is selected.

Fig 5.1 shows cross-sectional high resolution transmission electron microscopy (HR-TEM) image of a Ge nanowire after Si epitaxial growth at 450 ^{o}C for 500 seconds. It could be observed that a high quality single crystalline Ge nanowire surrounded by a uniform ~ 1 nm thickness Si shell. It shows high quality and uniform epitaxial Si shell on Ge nanowire is achieved.

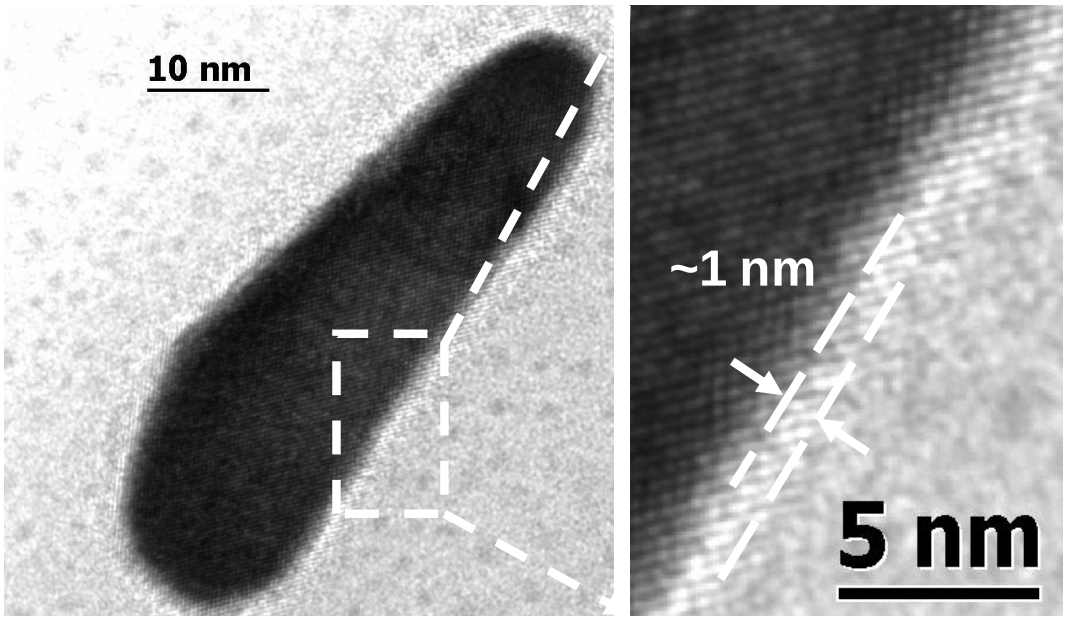

Figure 5.1: high resolution TEM image of the Ge nanowire cross section after epitaxial-Si shell grown at 450 ℃ for 500 seconds.

5.2.2 Epitaxial-Si growth process for Ge surface morphology improvement

Hydrogen annealing is generally used as an effective technique to improve the Si nanowire surface roughness [143] as well as heteroepitaxial Ge surface roughness [144]. It is reported that the formation of Si-H/Ge-H cluster lowers the diffusion barrier and thus allowing a higher diffusivity and surface atom mobility[144]. In this work, the Si_2H_6 would decompose into hydrogen atoms in the 450 ^oC Si epitaxial growth process and it can improve the Ge nanowire surface morphology. Since it is challenging to characterize the roughness of the nanowire surface due to its small surface area and surface curvature, planar Ge is employed to investigate the effect of Si epitaxial growth on Ge surface morphology.

Two Si wafers with a 300 nm epitaxial grown Ge layer were prepared and subjected to the Ge nanowire formation process: two-step etching process for 15 s

isotropic etching, followed by the oxidation & wet-etching cleaning process. Details of the processes were described in chapter 4. Next, the surface roughness of one wafer was characterized by atomic force microscope (AFM) while the Si epitaxial growth process was done on the other wafer. Then, the surface roughness of this wafer was characterized by AFM. It was found that the surface roughness was significantly improved by the Si epitaxial process. The surface roughness RMS was 48 Å for the wafer without Si epitaxial growth while it was improved to be 17 Å for the wafer gone through the Si epitaxial growth. This improvement could be attributed to the hydrogen dissolution from Si_2H_6 in Si epitaxial process, which helped to improve the Ge/Si surface roughness.

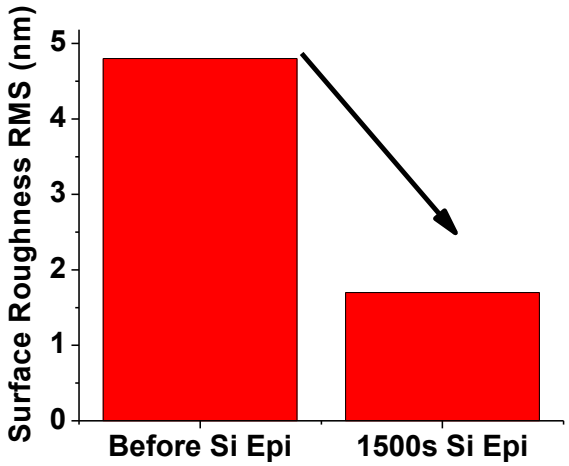

Figure 5.2: Ge surface roughness RMS before and after 1500 seconds Si epitaxial growth at 450 ℃.

5.3. Ge/Si core/shell nanowire pMOSFETs fabrication

The Ge nanowire was formed by the two-steps etching process described in chapter 4. After Ge nanowire formation, a Si shell was epitaxial grown over the

Ge nanowire at 450 ^{o}C for 1500 seconds, with process details described in section 5.2.1. The rest of the process is the same as the Ge nanowire pMOSFET fabrication processes described in chapter 4, except that an extra implantation of $BF_2/4\times10^{15}$ $cm^{-2}/20$ KeV and nickel germanidation processes through contact holes were employed to reduce the contact resistance.

5.4 Device channel physical characterization

Fig. 5.3 shows the TEM image of the channel of the device perpendicular to the wire length through the gate extension. Smooth Ge surface covered with conformal ALD HfO_2 (~ 11 nm) is observed. A void is observed below the Ge/Si core/shell nanowire. The reason of the formation of the void is described in chapter 4, which is due to the non-conformal nature of PVD deposition process. Nonetheless, the bottom of the Ge/Si core/shell nanowire is found to be covered with a layer of thin TaN (~ 3 nm), which could be clearly observed in the TEM image shown in Fig. 5.3. This layer of thin TaN makes the gate stack a full GAA structure. It is interesting to observe a different gate structure here, which is believed to be able to be attributed to the different distance between the nanowire and the substrate. The Ge core is ~ 50 nm × 32 nm, with a perimeter of ~ 140 nm. The ~ 2 nm white ring in between the Ge core and the HfO_2 dielectric comes from the epitaxial-Si shell and its composition is analyzed in the next chapter.

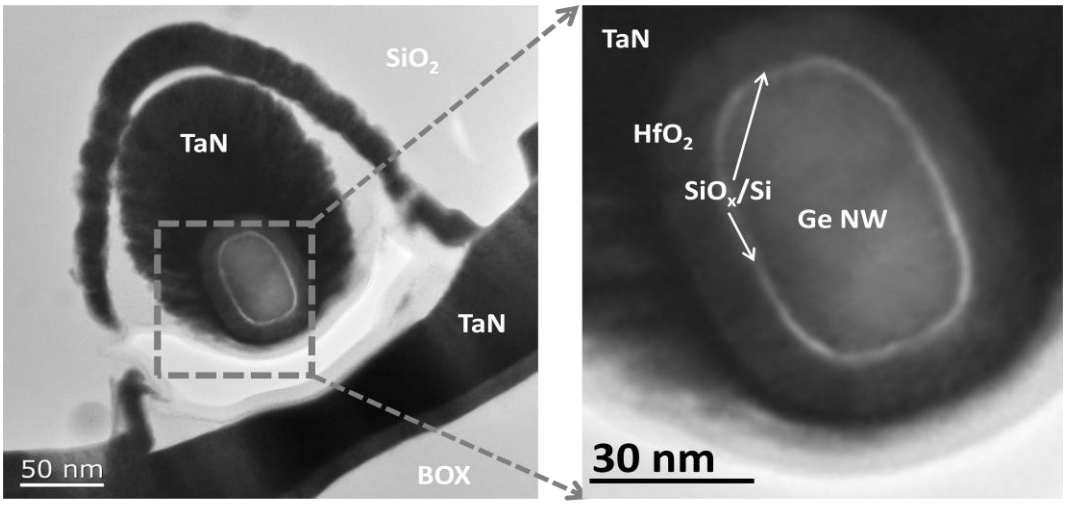

Figure 5.3: Transmission electron microscopy image of Ge/Si core/shell nanowire pMOSFET channel cross section. The left one is the zoomed in image which indicate the existence of a layer of thin TaN at the bottom of nanowire channel.

Fig. 5.4 (a) is the scanning transmission Electron Microscope (STEM) image of the channel, while (b) and (c) is the Electron Energy Loss Spectrum (EELS) signal from the three spots (points (1), (2), and (3)) indicated in the dark ring in Fig. 5.4 (a). Fig. 5.4 (b) shows the Si edge EELS analysis result of the epitaxial-Si shell. Besides the expected Si signal at the Si $L_{2,3}$ edge (~ 99 eV), Ge is also detected at the Ge $M_{2,3}$ edge at ~ 120 eV, suggesting some Ge atoms have out-diffused into the Si shell and formed GeO_x at the channel interface. The weak peak at 108 eV suggests the existence of Si^{4+} and the decreasing signal intensity suggests its concentration decreases from the HfO_2 side (point (1)) to the Ge core side (point (3)). The EELS oxygen edge analysis (Fig. 5.4(c)) shows that oxygen content at the Ge core side (point (3)) is half of that at the center point (point (2)) and the HfO_2 side (point (1)), which agrees with the decreasing Si^{4+} concentration. These results suggest that the observed dark ring consist mainly of SiO_x and Si.

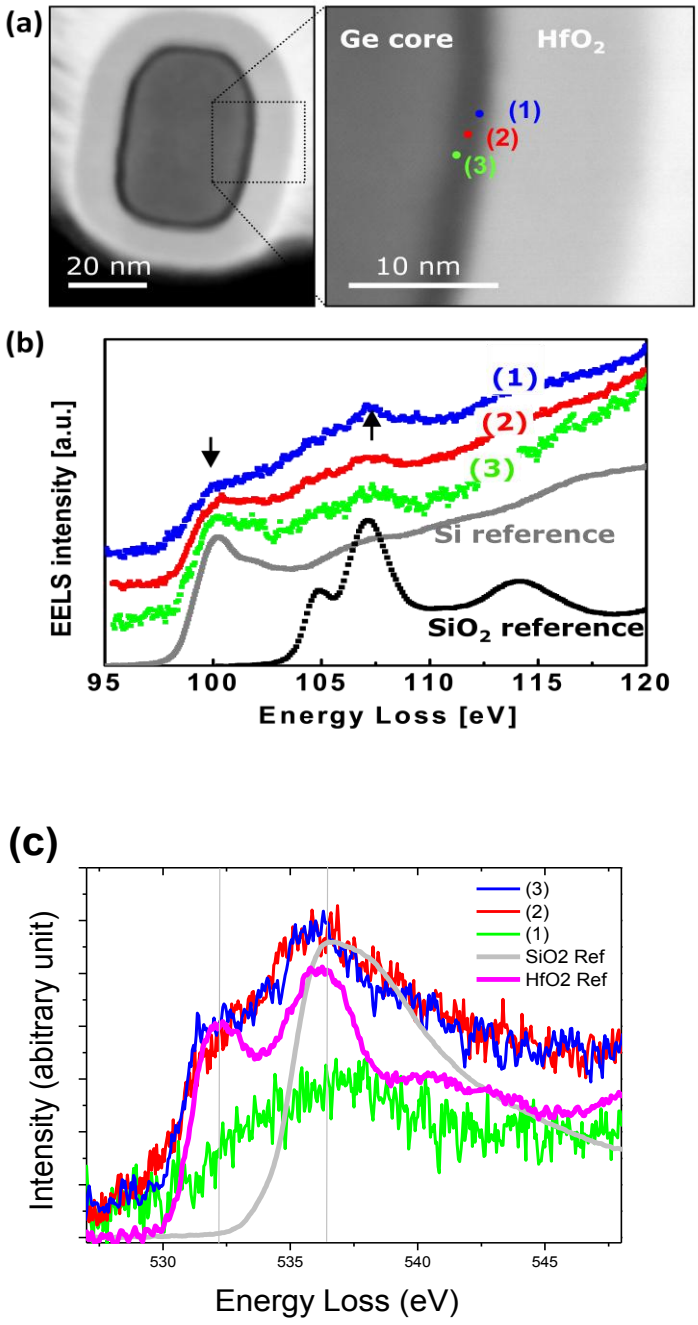

Figure 5.4: (a) STEM image of the Ge/Si core/shell nanowire pMOSFET channel cross section. (b) Si edge EELS signal at the three points of the epitaxial-Si shell indicated in (a), the two arrows indicate the peaks from Si and Oxygen. (c) Oxygen edge EELS signal at the three points of the epitaxial-Si shell indicated in (a).

5.5 Device I-V characterization

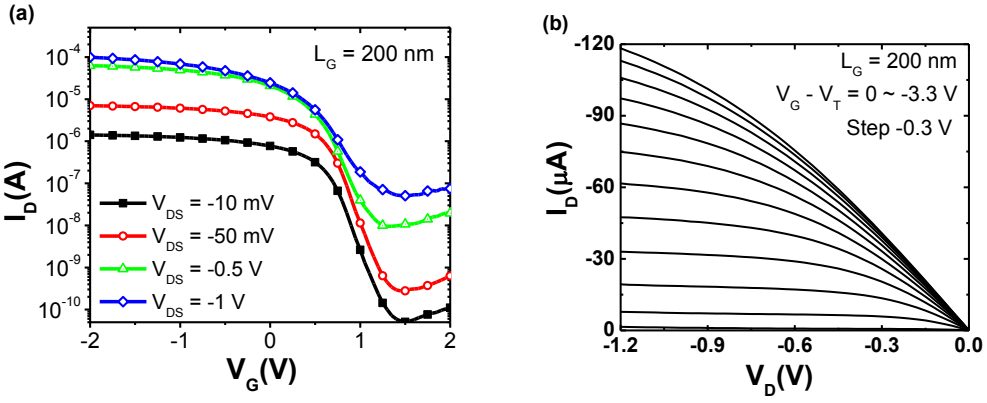

Figure 5.5: (a) I_D-V_G and (b) I_D-V_D characteristics of Ge/Si core/shell nanowire GAA PMOS. The Ge/Si core/shell nanowire diameter is 35 nm and gate length is 200 nm. The epitaxial-Si shell is with 2 nm and HfO_2 is 11 nm. Subthreshold slope is 162 mV/dec at V_{DS} =- 50 mV.

Fig. 5.5 shows the typical transfer and output characteristics of a 200 nm gate length Ge/Si core/shell nanowire pMOSFETs. A decent I_D-V_D output characteristic is shown in Fig. 5.5 (b). The drive current is 21 μA at V_G - V_T = 0.7 V and V_{DS} = -1 V, which is 150 μA/μm if normalizing by its perimeter. The SS is 162 mV/dec and the DIBL is 124 mV/V. Fig. 5.6 shows the transfer and output characteristics of the core/shell nanowire transistor with 100 nm gate length. As expected, the I_{ON} increased from 21 μA to 33 μA at V_G – V_T = -0.7 V and V_{DS} = -1 V when the transistor gate length decreased from 200 nm to 100 nm. Without device optimization, short channel effects start to be observed when the gate length scaling down from 200 nm to 100 nm, with the SS increasing from 162 mV/dec to 202 mV/dec and the DIBL increasing from 124 mV/V to 534 mV/V. Thinner gate dielectric thickness and optimized S/D doping profile is expected to suppress short channel effects. The I_{on}/I_{off} ratio maintained 10^4 for the 100 nm gate

length Ge/Si C/S NW MOSFETs, suggesting there is no significant leakage path along the channel.

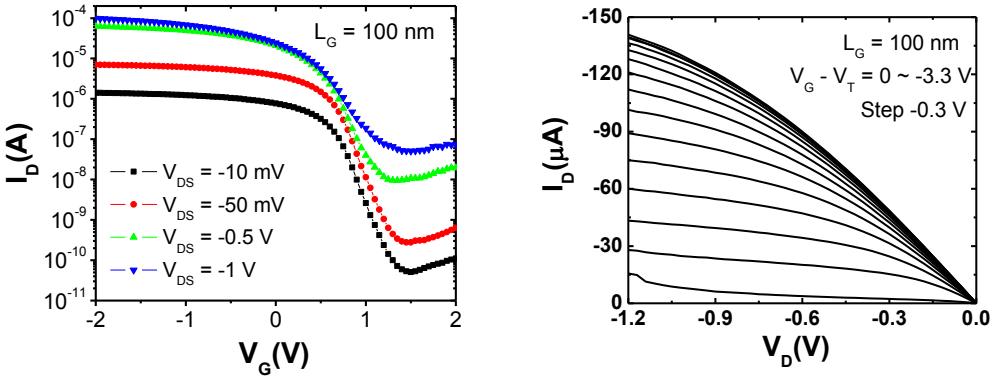

Figure 5.6: (a) I_D-V_G and (b) I_D-V_D characteristics of Ge/Si core/shell nanowire GAA pMOSFET. The Ge/Si core/shell nanowire diameter is 35 nm and gate length is 100 nm. Subthreshold slope is 202 mV/dec at V_{DS} =- 50 mV.

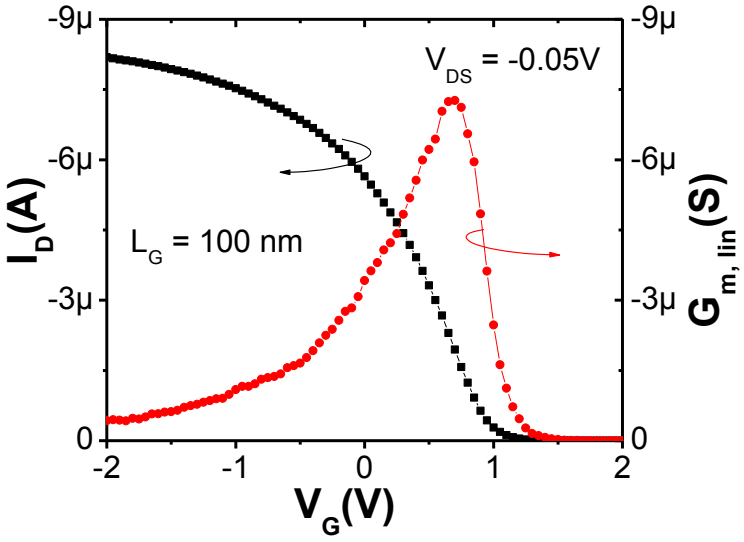

Figure 5.7: Linear I_D-V_G and G_m-V_G obtained from a Ge/Si core/shell nanowire GAA PMOS with 100 nm gate length. The peak transconductance is 7.27 μS.

Fig. 5.7 shows the linear I_D-V_G and G_m-V_G curves obtained from a Ge/Si core/shell nanowire GAA pMOSFET with 100 nm gate length, which demonstrated a peak transconductance of 7.27 μS at V_{DS} = - 0.05 V.

Fig. 5.8 presents the SS as a function of gate length. The long channel Ge/Si core/shell nanowire pMOSFETs, which are not expected to show any short channel effects, demonstrate consistent SS of ~ 160 mV/dec. The large SS suggests heavy trap density along the device channel. Based on the measured SS value, the interface state density D_{it} is estimated to be 7.5×10^{12} $cm^{-1} \cdot eV^{-1}$[142]. The high interface state density could be attributed to the Ge out-diffusion as shown by the EELS results. Those Ge atoms would segregate at the interface and generate defects [8]. Another possible reason is the defects due to the lattice mismatch between the Si shell and the Ge core. These traps along the channel surface degraded the SS performance and possibly increased the leakage current at the channel/drain junction. The trap density could be reduced by lowering the Si epitaxial process temperature [8] and employing a thinner Si shell.

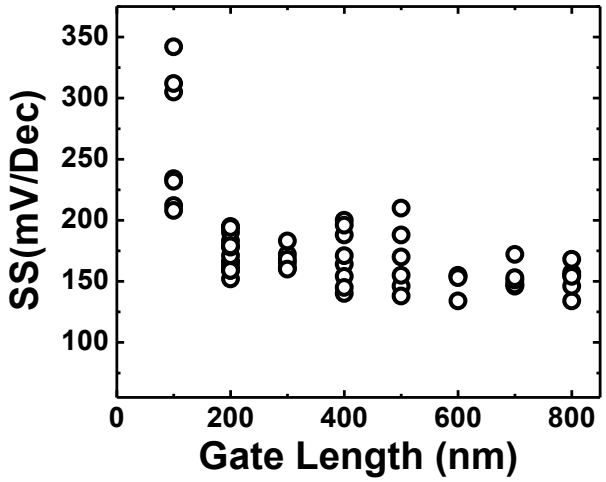

Figure 5.8: SS of Ge/Si core/shell nanowire GAA pMOSFET vs. gate length.

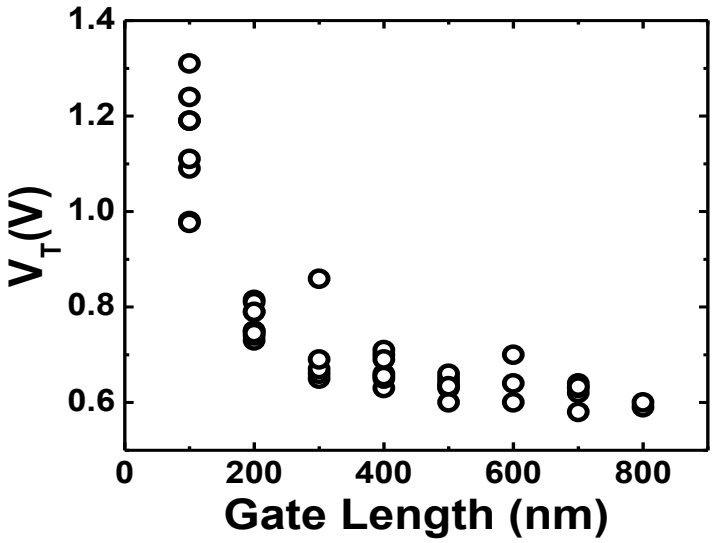

Figure 5.9: Threshold voltage of Ge/Si core/shell nanowire GAA pMOSFETs vs. gate length. V_T is ~ 0.7 V for long channel devices.

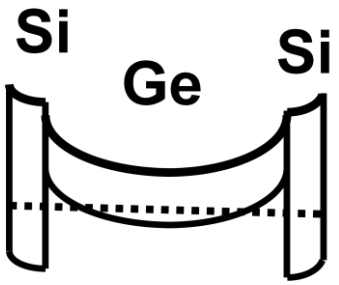

Figure 5.10: Energy band diagram of the Ge/Si core/shell structure. The dotted line is the Fermi level.

Fig. 5.9 presents V_T as a function of gate length, and shows ~ 0.7 V V_T of long channel devices. The large positive threshold voltage can be attributed to the work function of TaN, the heavy interface trap density and/or the interface-dipoles formed at the HfO_2/SiO_x interface[145], as well as the Fermi level alignment between Ge and Si in the core/shell heterostructure. All of these factors bring the Fermi level close to/below the valence band edge of the Ge nanowire as shown in Fig. 5.10 and thus forming hole gas inside the Ge nanowire without gate bias.

Low work function metal such as Al could be used to adjust V_T to the desired value[54].

Fig. 5.11 presents the total series resistance of a 200 nm gate length Ge/Si core/shell nanowire pMOSFET, with the total series resistance of ~ 7 kΩ at -4.5 V gate overdrive. The parasitic series resistance is extracted by extrapolating the total resistances of different gate length devices at various gate overdrives to an intersection point, as shown in Fig. 5.12. The extracted parasitic series resistance is ~ 3.5 kΩ, which is 490 Ω-μm after normalization by perimeter. The parasitic series resistance of this batch of devices is significantly lower than that of the Ge nanowire transistors presented in chapter 4. The reduction of the parasitic series resistance could be attributed to the additional implantation and nickel-germanide processes through the contact holes.

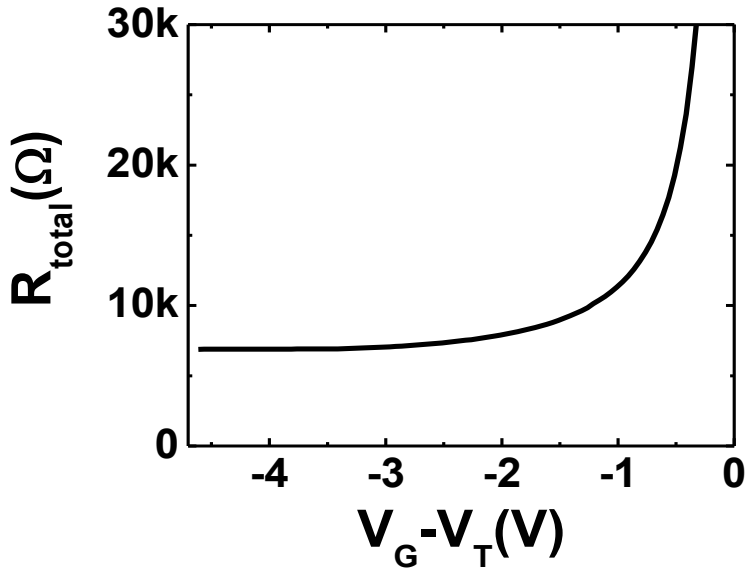

Figure 5.11: Total series resistance of a 200 nm gate length Ge/Si core/shell nanowire pMOSFET as a function of gate overdrive. The smallest total resistance is ~ 7 kΩ at -4.5 V gate overdrive.

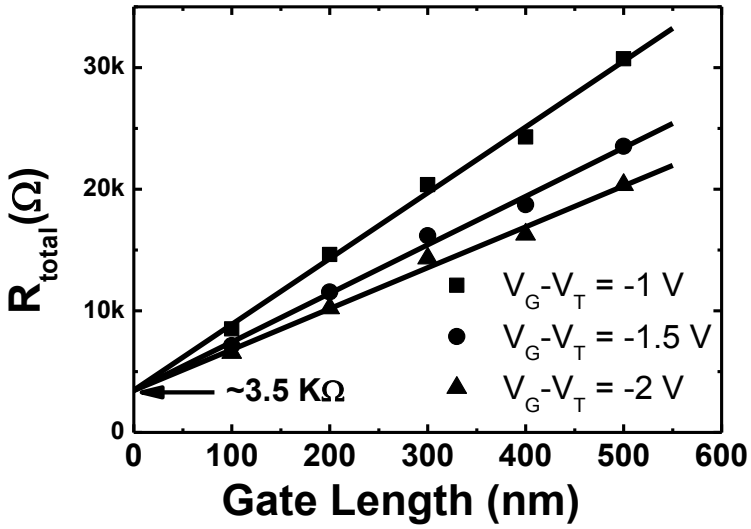

Figure 5.12: Total series resistance of Ge/Si core/shell nanowire pMOSFETs at various gate overdrives as a function of gate length. The parasitic series resistance is extracted by extrapolating the total series resistances of various gate length devices to an intersect point, which is ~ 3.5 kΩ for this batch of Ge/Si core/shell nanowire devices.

5.6 Hole mobility in the Ge/Si core/shell nanowire channel

The mobility is derived with the same method as described in chapter 4 by estimating the gate capacitance without considering quantum capacitance. The gate capacitor consists of two series connected cylindrical capacitors originated from HfO_2 and SiO_x respectively, and each of them could be calculated with the ideal cylindrical capacitor model $C_g = (2\ \pi\varepsilon_0\varepsilon_r L_g)/\ln[(r+T_{ox})/r]$, where T_{OX} is the dielectric thickness, r is the inner radius and L_g is the gate length. In this work, the thickness of interfacial SiO_x layer is assumed to be 1 nm based on above EELS results, which is about half of the Si interfacial layer between the Ge core and the

HfO_2. Dielectric constant is taken to be 1.7 for SiO_x and 20 for HfO_2 [53]. The hole mobility in Ge/Si core/shell channel is extracted by equation 4.3 after series resistance correction, and obtained a peak mobility of 254 $cm^2V^{-1}s^{-1}$.

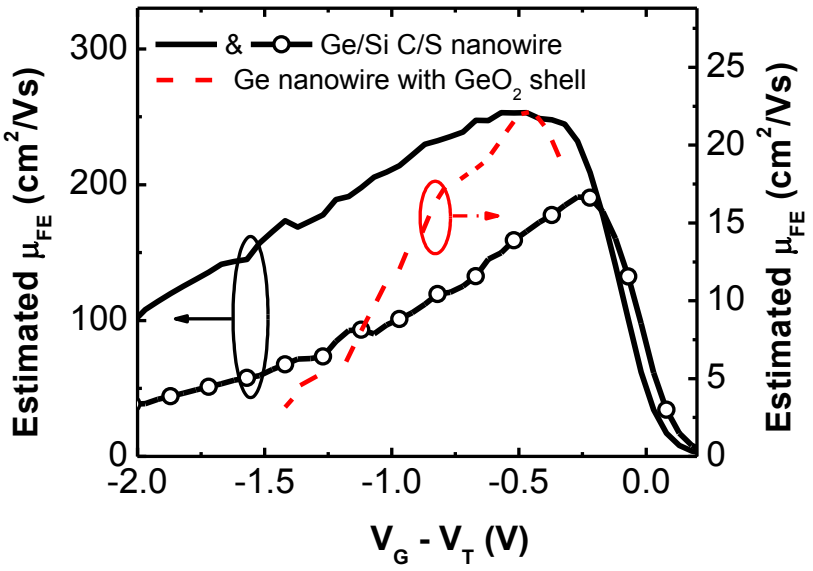

Figure 5.13: Estimated hole field-effect mobility (μ_{FE}) in the Ge/Si C/S nanowire and Ge nanowire with GeO_2 shell as a function of gate overdrives. The open circle curve is the hole mobility calculated without series resistance correction and the rest two lines are the hole mobility after series resistance correction. The dash line is the hole field-effect mobility in Ge nanowire with GeO_2 shell.

For comparison, the hole mobility of both the Ge nanowire pMOSFET presented in chapter 4 and the Ge/Si core/shell are plotted in Fig. 5.13. Compared with the Ge nanowire pMOSFET described in chapter 4, the introduction of epitaxial-Si shell improves the hole mobility to be 11.3 times higher. In Fig.5.13, as the gate overdrive increases, the hole mobility in the Ge/Si core/shell nanowire decreases much slower than that in the Ge nanowire with GeO_2 shell. It could be attributed to the improvement of surface roughness through Ge atom migration in

presence of H_2 in Si epitaxy process [144] as presented in section 5.2.2. Another reason for the improved mobility is the reduced Coulomb scattering as the Ge channel is sufficiently far removed from the surface defects scattering center. However, the epitaxial-Si shell thickness needs further optimization, as there is a tradeoff between hole mobility enhancement due to the compress stress on Ge core [146] and the low mobility in the Si shell, as well as the possible defects in Si shell which would degrade the device performance.

5.7 Hole injection in the Ge/Si core/shell nanowire channel

Fig. 5.14 presents the on state current of the Ge/Si core/shell nanowire pMOSFETs at $V_G - V_T$ = -0.7 V and V_{DD} = 1 V, as a function of gate length. As expected, the on state current increases as the gate length scaling down. To benchmark the transistors with their Si counterparts, the intrinsic gate delay τ=CV/I, where C is the gate capacitance, V is the supply voltage V_{DD} while I is the on-state current at $V_G = V_{DD}$. The gate capacitance is calculated with the cylindrical model as presented in mobility extraction. The intrinsic gate delay represents the fundamental RC (where R is the device resistance and C is the capacitance) delay of the device and provides a reference of the speed limit of the device which relatively insensitive to device width. Thus, it is a good reference to compared between different devices. Fig. 5.15 presents the intrinsic gate delay of over 20 Ge/Si core/shell nanowire transistors versus gate length. Si nanowire MOSFETs and the state-of-the-art Si planar MOSFETs are included for

comparison. The data shown in Fig. 5.15 clearly demonstrates the speed advantage of Ge/Si core/shell nanowire transistors over Si nanowire and Si planar transistors. The slope of intrinsic gate delay of the Ge/Si core/shell nanowire pMOSFET is ~ 1.75, while that of the state-of-the-art Si planar transistors is ~ 1.1, which means Ge/Si core/shell nanowire MOSFETs RC delay reduces fasters as the gate length scaling down and clearly demonstrated Ge/Si core/shell nanowire speed advantage in short gate length regime. This advantage could be explained by the lower backscattering coefficient in Ge/Si core/shell nanowire channel as discussed below.

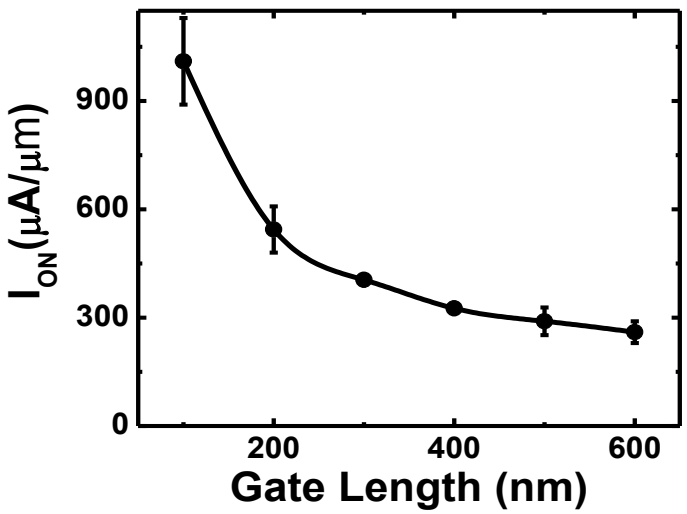

Figure 5.14: On-state current of Ge/Si core/shell nanowire pMOSFETs at $V_G - V_T$ = -0.7 V and V_{DD} = 1 V, as a function of gate length.

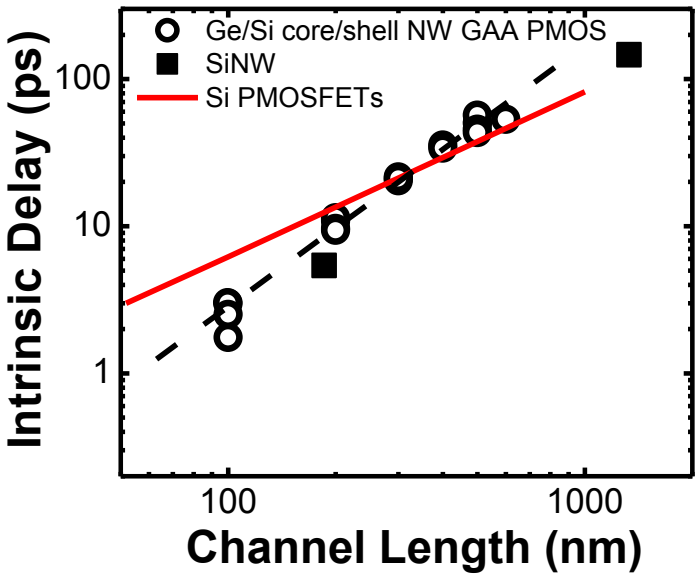

Figure 5.15: Intrinsic delay of Ge/Si core/shell nanowire pMOSFETs as a function of gate length. Si nanowire MOSFETs and state-of-the-art Si planar MOSFETs are included for comparison.

For short gate length transistors, non-stationary transport becomes more dominant and the carrier transport can be formulized [147] as:

$$I_D = WQ_{inj}v_{th}\left(\frac{1-R_c}{1+R_c}\right) \tag{5.1}$$

where W is the channel width, Q_{inj} is the inversion layer carrier density near the low field source, υ_{th} is the thermal injection velocity from the source accumulation layer to the channel inversion layer and R_c is the channel backscattering coefficient. R_c can be extracted by the following steps[147]:

1. Measure I_{DSAT} as a function of temperature and extract the backscattering related parameters:

$$\alpha = \frac{\Delta I_{DSAT}}{I_{DSAT,o}\Delta T} \tag{5.2}$$

$$\eta = \frac{\Delta V_{T,lin}}{\Delta T} \tag{5.3}$$

where ΔI_{DSAT} is the change of drain current over ΔT, $I_{DSAT,\ o}$ is the saturated current at base temperature and ΔT is the temperature difference between the base temperature where the backscattering coefficient is measured and another temperature. $\Delta V_{T,lin}$ is the change in linear threshold voltage.

2. Calculate λ/l

$$\frac{\lambda}{l} = \frac{4}{0.5-\left(\alpha+\frac{\eta}{V_G-V_{T,SAT}}\right)T} - 2 \tag{5.4}$$

where λ is the near-equilibrium mean-free-path, l is the critical distance of the injected carriers travel over a KT/q layer from the source, V_{TSAT} is the threshold voltage at the base temperature and T is the base temperature.

3. Derive backscattering coefficience R_c.

$$R_c = \frac{1}{1+\lambda/l} \tag{5.5}$$

Fig. 5.16 presents the I_D-V_G characteristics of a 200 nm Ge/Si core/shell nanowire pMOSFET after 13 times repeated measurements. Maximum threshold voltage difference is only 13 mV, indicating the stability of threshold voltage over repeating measurements. Fig. 5.17 presents the I_D-V_G characteristics of a 200 nm gate length Ge/Si core/shell nanowire pMOSFET at temperature from 296 K to 387 K. As shown in Fig. 5.17 (a), threshold voltage increase with temperature. The extracted linear threshold voltage is plot against the temperature and the

fitting gradient η is 1.46 mV/K as shown in the inset of Fig. 5.18. Fig. 5.17 (b) shows that the saturated current decreases as temperature increases, which could be attributed to the increased scattering at higher temperature. The normalized drain current change is perfectly linear as plotted in Fig. 5.18, giving a gradient α of -8.66 $\times 10^{-4}$ K^{-1}. Based on these two parameters, the backscattering coefficient of this 200 nm gate length Ge/Si core/shell nanowire pMOSFET can be extracted to be 0.31.

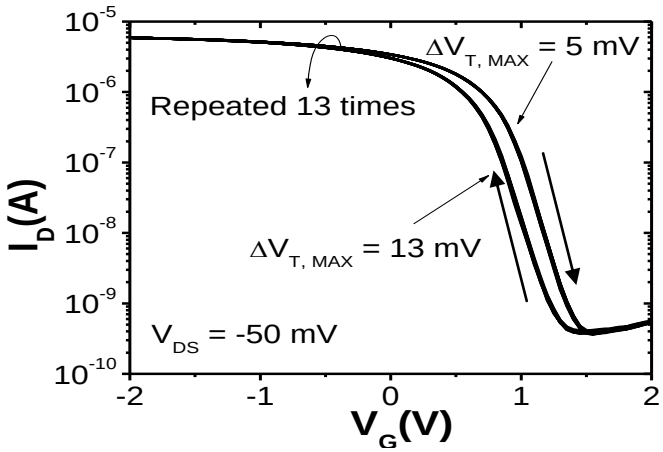

Figure 5.16: Drain current characteristics of a 200 nm gate length Ge/Si core/shell nanowire pMOSFETs at V_{DS} = -0.05 V with 11 times repeated measurements. The arrows indicate the gate bias sweeping directions.

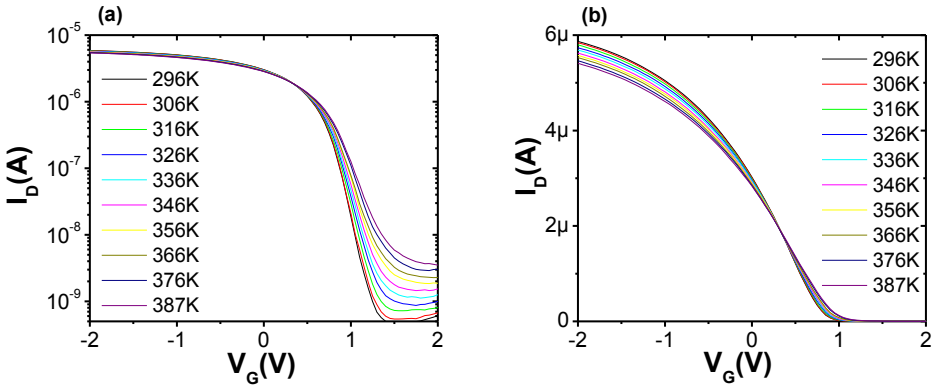

Figure 5.17: The (a) log scale plot and (b) linear scale plot of drain current of a 200 nm gate length Ge/Si core/shell nanowire pMOSFET V_{DS} = -0.05 V as a function of gate bias at different temperature.

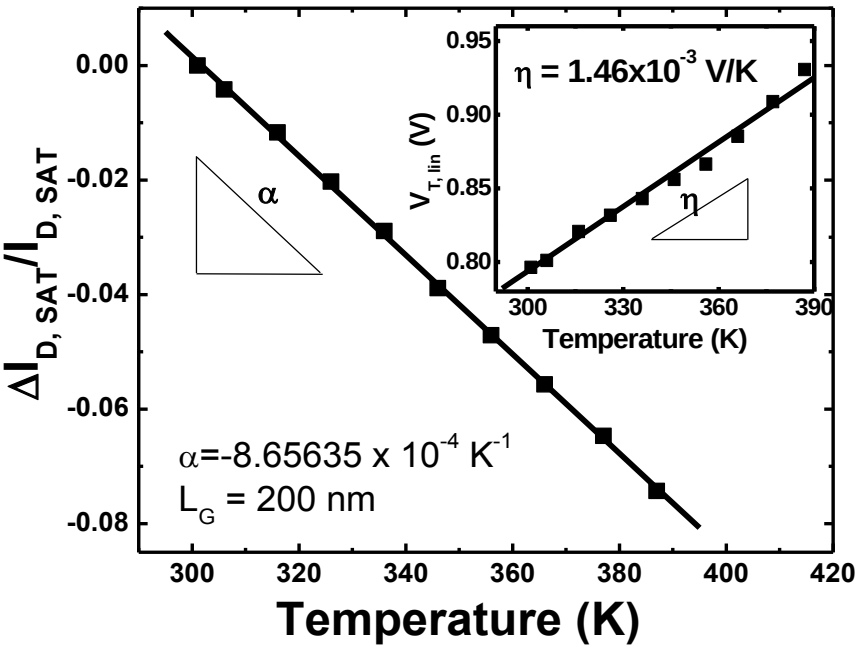

Figure 5.18: $I_{D, SAT}$ and $V_{T, Lin}$ (inset) variation of GAA Ge/Si core/shell pMOSFET as a function of temperature, from which the ballistic efficiency is extracted to be 0.524. $I_{D,SAT}$ is obtained at V_G = -1.5 V.

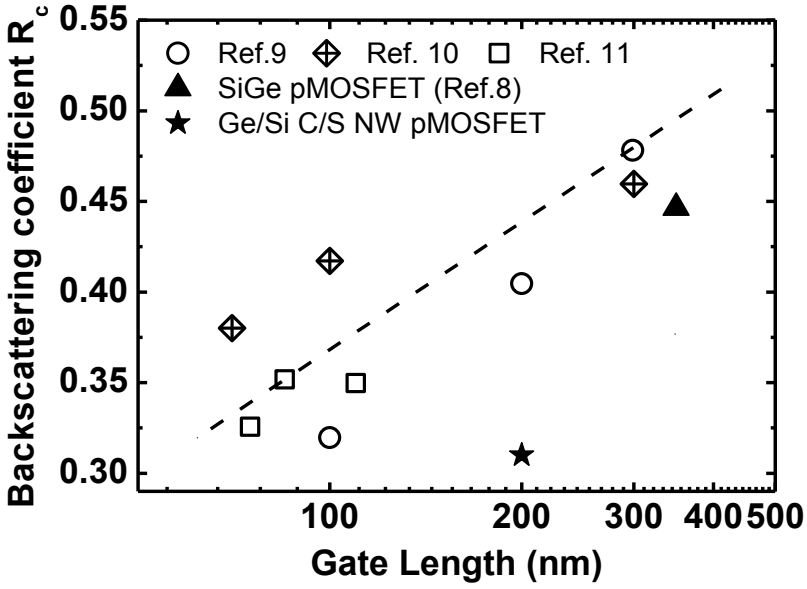

Figure 5.19: $I_{D, SAT}$ and $V_{T, Lin}$ (inset) variation of GAA Ge/Si core/shell pMOSFET as a function of temperature, from which the ballistic efficiency is extracted to be 0.524. $I_{D,SAT}$ is obtained at V_G = -1.5 V.

Fig. 5.19 compares the backscattering coefficient of the Ge/Si core/shell nanowire pMOSFET with those of reported Si MOSFETs and planar SiGe MOSFETs [17-20]. The backscattering coefficient (R_c) of a 200 nm gate length Ge/Si core/shell nanowire pMOSFET is 0.31, and it is lower than that of Si MOSFETs by ~ 22% at the same gate length. Since R_c is directly related to the drive current, lower R_c suggests higher on-state current and smaller gate delay τ. Thus, the reduction of R_c agrees with the speed advantage of the Ge/Si core/shell pMOSFET shown in Fig. 5.16.

5.8. Summary

Si epitaxial grown over Ge is demonstrated as an effective way to improve the Ge surface roughness and this technique was used to improve the Ge nanowire surface morphology problem inherited from the Ge nanowire fabrication processes. The Ge/Si core/shell nanowire GAA pMOSFETs integrated with HfO_2/TaN gate stack demonstrated high drive current and significantly improved mobility compared with the Ge nanowire pMOSFET in chapter 4. The use of an interfacial epitaxial-Si shell is an effective performance booster towards the integration of high-mobility Ge channel transistors. Backscattering coefficient is extracted to be 0.31 on a 200 nm gate length device Ge/Si core/shell nanowire pMOSFET.

Chapter 6
Conclusions and Recommendations

6.1 Conclusions

Nanowire transistors are considered as an important candidate of advanced MOSFETs for several reasons. Firstly, the nanowire GAA architecture is able to suppress short channel effects due to its superior gate electrostatic coupling over the channel. Secondly, carrier mobility in a nanowire is higher due to the suppressed scattering and volume inversion effect. Thirdly, power consumption in nanowire transistor is low as junction area is minimized and short channel effects are suppressed. High performance nanowire transistors have been demonstrated by both the bottom-up and the top-down approach.

In chapter 3, nanowire GAA MOSFETs integrated with 1-D NiSi Schottky S/D are studied. One of the challenges of the nanowire transistor is the large parasitic series resistance. The solution is proposed by replacing the heavily doped S/D with highly conductive metal. Historically, it is found that the on-state current of a SB-MOSFET is lower than that of a conventional MOSFET due to the additional Schottky barrier at the source junction and there is no reported silicide has Schottky barrier height sufficiently low to make the on-current comparable with the conventional heavily doped S/D MOSFETs. In chapter 3, the nanowire

GAA architecture is demonstrated to be able to effectively lowering the effective Schottky barrier height, and consequentially improve the SB-MOSFET performance. The experimental data demonstrates that a nanowire GAA SB-MOSFET has much better device performance than that of a planar SOI SB-MOSFET, showing larger on-state current, smaller leakage current and smaller SS. Moreover, the nanowire GAA SB-MOSFET with smaller nanowire diameter shows better performance. Simulation work confirms that the Schottky barrier width is much thinner in the nanowire GAA MOSFET if comparing with the planar SOI SB-MOSFET, because the potential in the channel could be pushed down/up more effective in the nanowire GAA architecture. Thus, it could be concluded that the nanowire GAA architecture is able to enhance the carrier injection in a SB-MOSFET and could be an effective way to mitigate the requirements of Schottky barrier height for achieving larger on-state current.

In chapter 4, Ge nanowire pMOSFETs were fabricated and studied. The higher intrinsic carrier mobility has made Ge one of the most attractive candidates as the channel material for future high performance transistors. Moreover, the advantage of Si/SiO_2 system has gone since SiO_2 has been replaced by high-k for suppressing short channel effects and gate leakage. Although the bottom-up Ge nanowire transistors have demonstrated high performances, no top-down Ge nanowires have been reported yet. In chapter 4, Ge nanowires with diameter down to 14 nm were fabricated on an epitaxial grown Ge layer by a novel technique of two-step etching with polymerization in-between. A thermally grown GeO_2 shell was employed as a passivation layer between the Ge nanowire and the HfO_2/TaN gate stack to fabricate a Ge nanowire pMOSFET. The on/off ratio of 6 orders is

achieved on a Ge nanowire pMOSFET, suggesting the leakage current is effectively suppressed by the nanowire transistor architecture. However, it is found that the hole mobility in the Ge nanowire channel is as low as 22 $cm^2V^{-1}s^{-1}$. The low hole mobility is attributed to the high interface trap state density and the surface roughness scattering. Large series resistance is identified to be another problem.

In chapter 5, a Si epitaxial shell was explored to improve the Ge nanowire MOSFET performance. Although the Ge nanowire surface has different lattice orientation, ultra-thin high quality and uniform Si shell was successfully epitaxial grown on the Ge nanowire in a UHV-CVD chamber at 500℃. It was found that the Si deposition process was able to smooth the Ge surface. In this chapter, Ge/Si core/shell nanowire GAA pMOSFETs were fabricated and characterized. Interestingly, a thin layer of TaN was found at the bottom of the Ge nanowire although the TaN was deposited by a PVD system, and the thin layer of TaN at the nanowire bottom made the transistor a fully GAA architecture. The epitaxial-Si shell was analyzed by EELS and it mainly consisted of Si, SiO_x. Some Ge atoms were found to be out-diffused into the Si-shell, and possibly accumulated at the channel surface leading to high interface trap density. Despite the high interface trap density, hole mobility in the Ge/Si core/shell channel achieved as high as 254 $cm^2V^{-1}s^{-1}$. The significant improvement of the hole mobility compared with that in the Ge nanowire presented in chapter 4 could be attributed to the surface smoothness improvement, the buried channel effect and the compressive stress from the Si shell. The series resistance of the transistor was reduced to its ~ 1% by introducing an additional implantation and nickel germanidation through

the contact holes. On-current of a 200 nm gate length Ge/Si core/shell nanowire pMOSFET achieved 150 μA/μm due to the improvements of the hole mobility and parasitic series resistances and its hole backscattering coefficient achieved 0.31, which is ~ 22% lower than its Si/SiGe counterparts.

6.2 Recommendations

Although the nanowire transistor architecture has attracted significant research attentions for its promising characteristics, the research of nanowire transistor is still at a relatively early stage. This project demonstrated two possible approaches of improving nanowire transistor performance. Based on the results obtained in this project, here are some recommendations for further studies on improving the nanowire transistor performance for future high performance applications.

1. The nanowire GAA SB-MOSFET integrated with lower SBH metal can be explored to achieve high performance. Although NiSi SBH on Si is ~ 0.46 eV, the transistor in chapter 3 still achieved nearly ideal SS and high on-state current. Silicide with lower SBH such as ErSi and PtSi are expected to achieve much better performance. In view of the increasingly dominant S/D resistance as the channel length scaling down, the advantages of nanowire SB-MOSFETs integrated with low SBH Silicide would be an interesting topic.

2. The Ge nanowire GAA SB-MOSFET would be an interesting topic to explore. Although carriers in Ge have much higher mobility than that in Si, the on-state current of Ge transistor is limited by large series resistance. The large series resistance in Ge transistors is due to the low dopant solid solubility and thus, has little room for improvement. This problem would be even worse for Ge nanowire transistors due to the architecture specified narrower extension area. A possible solution could be replacing the high resistance of doped S/D with highly conductive NiGe and employing the SB-MOSFET architecture. The hole Schottky barrier of NiGe on Ge is ~ 0.16 eV, which is much lower than that of 0.46 eV of NiSi on Si. Moreover, the integration of a Si shell on the Ge nanowire would form hole gas in the Ge nanowire channel. The accumulated holes at the Schottky junction would lead to an ultra-thin Schottky barrier width and lead to higher hole tunneling probability. In this case, the effective Schottky barrier height of NiGe on Ge/Si core/shell channel would be even lower than 0.16 eV due to the higher hole tunneling probability. Thus, compared with the Si nanowire counterpart, the Ge nanowire GAA MOSFET integrated with 1-D NiGe S/D is expected to have higher on-state current for its higher carrier mobility and lower S/D Schottky barrier.

3. C-V characterization could be carried out to investigate the intrinsic properties of nanowire transistors. If C-V characteristics could be measured, the interface traps and defects could be quantified and understand for further

surface engineering. Mobility could be extracted based on the C-V characteristics instead of the estimation in this project.

4. The Si shell thickness in a Ge/Si core/shell transistor could be optimized. There is a tradeoff on the Si shell thickness. In case of thicker Si shell, hole mobility in the Ge core would be larger as the stress on Ge core would be larger and scattering from surface defect are removed far away. Another benefit of thicker Si shell is that, channel surface defects would be lower as Ge out-diffusion would be suppressed more effectively. However, Ge channel would be buried deeper in case of a thicker Si shell, and more carriers would be transported through the low mobility Si shell to lower the on current. Furthermore, there would be a large amount of defects in the Ge/Si core/shell structure due to the lattice mismatch to reduce the on state current if the Si shell thickness is over the critical value. The Si shell epitaxial growth process also needs further optimization. It is reported lower process temperature could suppress Ge out-diffusion more effectively, which could be tried to obtain higher transistor performance.

5. Strain engineering could be explored on the nanowire transistors. Strain engineering is generally implemented as a performance booster on the conventional planar transistors; however, few works are done on Si and Ge nanowires. All of those widely used strain techniques on planar devices can be applied on nanowire transistors. Moreover, it would be interesting to

explore the strain in the core/shell structure which is unique to nanowire architecture.

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List of Publications

1. **J.W. Peng**, S. J. Lee, G. C. Albert Liang, N. Singh, S. Y. Zhu, G. Q. Lo and D. L. Kwong, "Improved Carrier Injection in Gate-All-Around Schottky Barrier Silicon Nanowire Field Effect Transistors," Applied Physics Letters, Vol. 84, 073503, 2008.

2. **J.W. Peng**, N. Singh, G. Q. Lo, M. Bosman, C. M. Ng and S. J. Lee, "Germanium Nanowire Metal-Oxide-Semiconductor Field-Effect-Transistor Fabricated by Complementary Metal-Oxide-Semiconductor Compatible Process," Electron Devices, IEEE Transactions on, Accepted.

3. **J. W. Peng**, N. Singh, G. Q. Lo and D.L. Kwong and S. J. Lee, "CMOS Compatible Ge/Si Core/Shell Nanowire Gate-All-Around pMOSFET Integrated with HfO2/TaN Gate Stack," Presented on IEEE International Electron Devices Meeting, Baltimore, MD, USA, 2009.

4. **J. W. Peng**, S. J. Lee, G. C. Albert Liang, N. Singh, C. M. Ng, G. Q. Lo and D. L. Kwong, "Gate-All-Around 4-nm Silicon Nanowire Schottky Barrier MOSFET with 1-D NiSi Source/Drain," Presented on International Conference on Solid State Devices and Materials, Tsukuba, Japan, 2008.

5. **J.W. Peng**, S.J. Lee, A. Agarwal, C.M. Ng, L. Chan, G.J. Zhang, N. Balasubramanian, "Nanowire Biosensor for Highly Sensitive and Fast Detection of Calcium Ions," Presented on International Conference on Materials for Advanced Technologies, Singapore, 2007.