A PROGRAMMABLE STIMULATOR FOR FUNCTIONAL ELECTRICAL STIMULATION

TAN YI JUN JASON

NATIONAL UNIVERSITY OF SINGAPORE

2010

A PROGRAMMABLE STIMULATOR FOR FUNCTIONAL ELECTRICAL STIMULATION

TAN YI JUN JASON

(B. Eng. (Hons.), National University of Singapore)

A THESIS SUBMITTED

FOR THE DEGREE OF MASTER OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2010

ACKNOWLEDGEMENTS

I would like to express my gratitude to all those who has given me support and rendered me help throughout the course of my MEng research project

First of all, I would like to sincerely thank both my supervisors, A/P Xu Yong Ping and Dr Wee Keng Hoong from DSO National Laboratories for their guidance and teaching. I have learnt a great deal from them. Special thanks to Mr Ng Kian Ann for his support and help in this project.

Secondly, I would like to extend my gratitude to GLOBALFOUNDRIES Singapore Pte Ltd, especially Dr Lap Chan and Dr Ng Chee Mang, for granting me a Joint-Industrial Programme post-graduate scholarship for my MEng studies.

Also, I would like to thank the lab assistants of the VLSI Signal Processing Lab, Mr Teo Seow Miang and Ms Zheng Huan Qun, and lab assistants from CALES-1 (eITU) lab as well. They had provided timely assistance whenever I faced problems with my Cadence account and administrative matters.

Last but not least, I would like to express my gratitude to my family, my girlfriend, Ms Ng Su Peng for their support and encouragement throughout the course of this post-graduate study.

TABLE OF CONTENTS

SUMMARY

Functional Electrical Stimulation or FES has been used widely for many applications, aiming to restore lost body functions due to nerve damage or injury. One of the applications of FES is to restore hand functions for patients suffering nerve damage along the arm such that neural signals from the brain cannot reach the hand muscles due to nerve denervation caused by the injury. Research work has been ongoing for such FES systems and current stimulator systems involve an implanted stimulator with wire leads to electrodes controlled wirelessly by an external unit. Implanting wire leads complicates the surgical process and external control unit is cumbersome for users and provides limited hand functions and programmability. Therefore, in recent years, numerous researches are done on neural recording, either from the brain cortex or from peripheral nerves such that these neural signals can act as triggers for stimulation, thereby eliminating the need for an external control unit. Hence, modern day FES systems usually consist of a front-end neural recording circuitry and a back-end stimulation circuit. The idea is to detect a neural signal, decodes it and sent information wirelessly to the stimulator circuit for adequate stimulation.

This thesis presents a programmable single-channel stimulator for such application. The overall system is implemented in two architectures and both architectures are incorporated into a single chip. Stimulation parameters like stimulus amplitude, pulsewidth and frequency are programmable. In recent years, concerns of tissue

damage due to stimulation are becoming the main focus of designing stimulator circuits and experiments show that rectangular balanced biphasic stimulus can reduce such tissue damage. Therefore, charge balance accuracy becomes one of the concerns in the design of the stimulator.

The proposed stimulator in this thesis has been implemented using AMS 2P4M 0.35um CMOS technology. It is also fabricated and verified with silicon results. Measurement results show that both stimulator versions are able to output a rectangular biphasic stimulus with programmable stimulation parameters. Achieved charge balance, for both stimulator versions, is also below the stated safety tolerance level of 0.4uC. A comparison study is also done to analyze the performance of each stimulator version. Lastly, some suggestions for improvements and future work are proposed to improve the overall stimulator circuit.

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS AND SYMBOLS

AMS	AustriaMicroSystems
CMOS	Complementary MOSFET
2P4M	2 poly-silicon layers, 4 metal layers process
CIS	Continuous Interleave Sampling
FES	Functional Electrical Stimulation
OTA	Operational Transconductance Amplifier
DAC	Digital to Analog Converter
ASIC	Application Specific Integrated Circuit
RC	Resistor-capacitor
FSM	Finite State Machine
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
pMOS	p-channel MOSFET
nMOS	n-channel MOSFET
pDAC	DAC implemented with pMOS transistors
nDAC	DAC implemented with nMOS transistors
LSB	Least Significant Bit
NSB	Non-Significant Bit
MSB	Most Significant Bit
PCB	Printed Circuit Board
ADC	Analog to Digital Converter

Opamp	Operational Amplifier
DC	Direct Current
SR	Set-Reset
I/O	Input/Output
LVS	Layout Versus Schematic
RFID	Radio Frequency Identification
ENG	Electronystagmogram

CHAPTER ONE: INTRODUCTION

1.1 History and applications of FES

The use of electricity for medical purposes can be traced back to as early as 46 AD when electrical discharges of animals like torpedo fish and electric eels were used to transfer current into human bodies for treating ailments such as headache and gout [1], [2]. The discovery of muscle contraction caused by electrical current in the 1800's by an Italian physician and physicist, Luigi Galvani, sparked intensive research interest in the area of electrical stimulation, aiming to restore body functions due to disabilities, till this very day [1]. It was until the 1960's when the concept of Functional Electrical Stimulation, or FES, was first described. A "functionally useful movement" was successfully induced by electrically stimulating a muscle with damaged nerves [3]. Since then, FES has been used extensively to try restoring lost body functions in people with neural injuries resulting from stroke, head injury or spinal cord injury or any neurological disorders. Applications of FES includes restoration of sight, hearing, limb functions, regulate heartbeat and bladder control (Fig. 1.1).

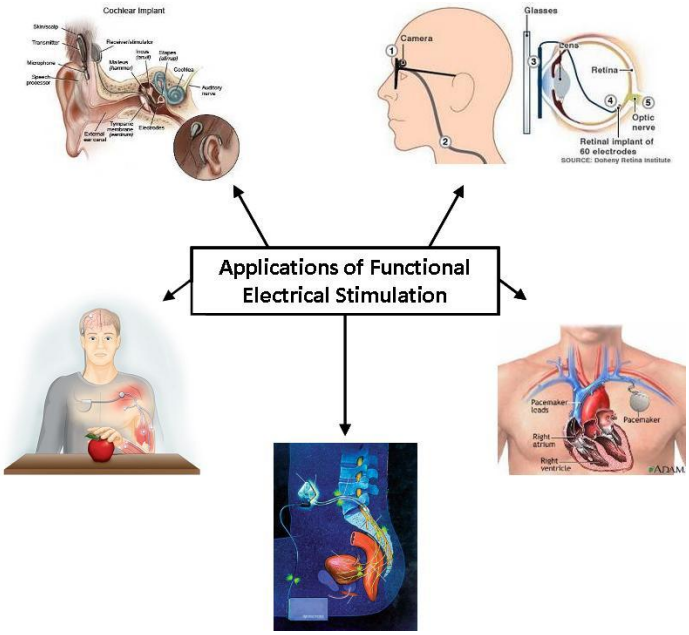

Fig. 1.1 Applications of FES [4]-[8]

Besides medical purposes, FES has also been used in sports training where athletes tone and build up their muscles through electrical stimulation. The following paragraphs provide brief descriptions on how FES is able to help restore various body functions as highlighted in Fig. 1.1.

1.1.1 Hearing Restoration [4]

One of the most successful applications of FES is in the area of hearing restoration. Today, there are many commercially available cochlear implants or bionic ears (Fig. 1.2) to aid people who are deaf or severely hard of hearing to distinguish sounds.

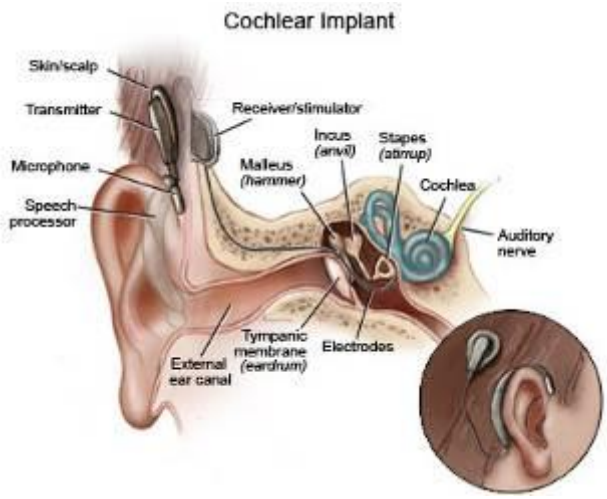

Fig. 1.2 Cochlear implant [4]

As shown in Fig. 1.2, a typical cochlear implant is made up of the following components, some of which are implanted while others are external.

- Microphone (external): captures sounds from the environment
- Speech processor (external): filters captured sounds to differentiate between audible speech and background noise and converts filtered sounds to electrical signals to be sent to the transmitter.
- Transmitter (external): transmits processed electrical signals from the speech processor to the receiver via electromagnetic induction.
- Receiver (implanted): receives electrical signals from the transmitter and decodes received signals. Electrical information is then sent to the stimulator.
- Stimulator (implanted): Converts electrical information from receiver into electrical impulses for stimulation.
- Electrodes (implanted): Implanted inside the cochlear as sites for stimulation. Impulses from the stimulator are sent to the auditory nerve system via the electrodes.

Cochlear implants have been effective thus far in helping deaf or almost deaf people recognize sounds and speech.

1.1.2 Heartbeat regulation [5]

Cardiac pacemakers have been around since the 1950's. At that time, pacemakers were large and had to be external devices. These days, pacemakers are implanted within the body with a fitted battery that can last for 5 to 10 years. Fig. 1.3 shows parts of a pacemaker implanted near the heart.

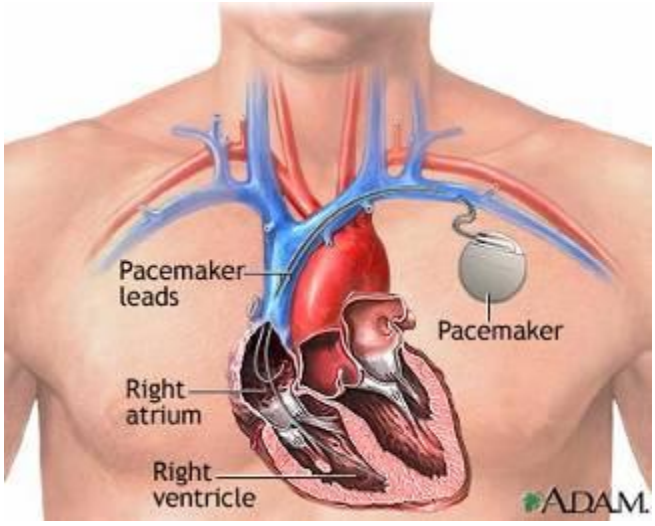

Fig. 1.3 Cardiac pacemaker [5]

The pacemaker has two main components,

- Generator: the main body of the pacemaker that consists of a mini processor for monitoring heartbeats and generating voltage impulses to the heart if there is any irregularity in detected heartbeats.
- Leads: connectors between the generator and the heart. These are inserted

into the heart mainly for transferring information from the heart to the generator and voltage impulses from the generator to the heart.

Cardiac pacemakers have proved to be very effective in heartbeat regulation and have been implanted in patients over the years.

1.1.3 Sight Restoration [6]

Inspired from the success of cochlear implants, research for visual neuroprosthesis or 'bionic' eye started in 1990's, aiming to use FES to restore sight. Electrical stimulation is done either on the retinal or at the brain cortex. Fig. 1.4 shows an example of a retinal-based bionic eye.

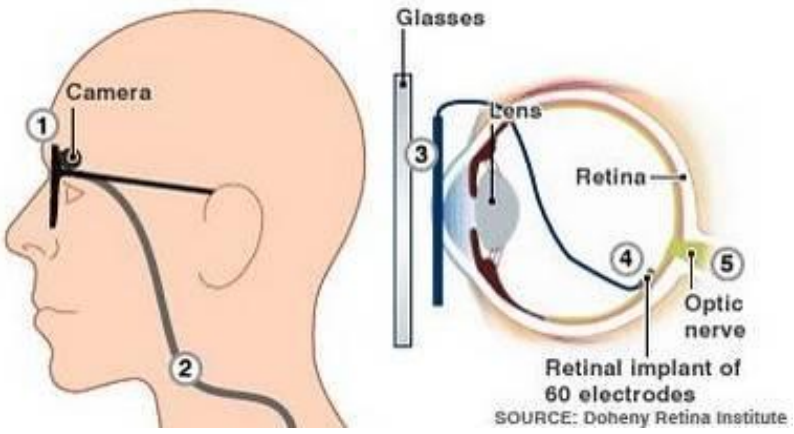

Fig. 1.4 Bionic eye [6]

Components of a bionic eye include,

- Camera: located on the glasses to capture images and signals are sent to external processing unit.
- Transmitter: attached to the glasses to transmit processed signals from the

external processing unit.

- Receiver: implanted under the surface of the eye. Receives signals from the transmitter and sends information to the electrodes.
- Electrodes: implanted on the retinal for stimulation.

Based on stimulation on the retinal, information is sent to the brain to be processed, hence generating an image for the patient with bionic eye. Cortex-based bionic eye on the other hand, stimulates the brain cortex directly. Currently, bionic eye has enjoyed some success in helping patients recognize shapes but those images induced from stimulation are still low in resolution. Face recognition is still not possible at the moment. Much research is still needed in this area to create better visual neuroprosthesis.

1.1.4 Bladder Control [7]

FES used in bladder control application is a relatively new concept where research is done to investigate the potential of FES as a bladder and bowel control mechanism for patients with spinal cord injury. An example of a bladder control FES system is shown in Fig. 1.5.

Fig. 1.5 Bladder control FES system [7]

Typical components of a bladder control FES system includes,

- Stimulator: provides stimulus to sacral nerves, responsible for bowel functions, on the spinal cord for bowel contractions.
- Wire leads: connectors between electrodes and stimulator. Acts as an electrical pathway for stimulus to reach the desired nerves.
- Cuff electrodes: attached to sacral nerves as sites of stimulation. Stimulus from the leads passes through the electrodes and stimulates the nerves.
- External control device: provides wireless power and control to the stimulator.

Bladder control FES systems are already used by patients suffering from incontinence and urinary tract infections due to spinal cord injuries. FES is proven to be effective in relieving the patients from bladder-related problems.

1.1.5 Limb Functions Restoration [8]

Last but not least, FES is also used in attempts to restore limb functions like standing, walking and grasping. Fig. 1.6 gives an overview of a FES system for hand and arm functions.

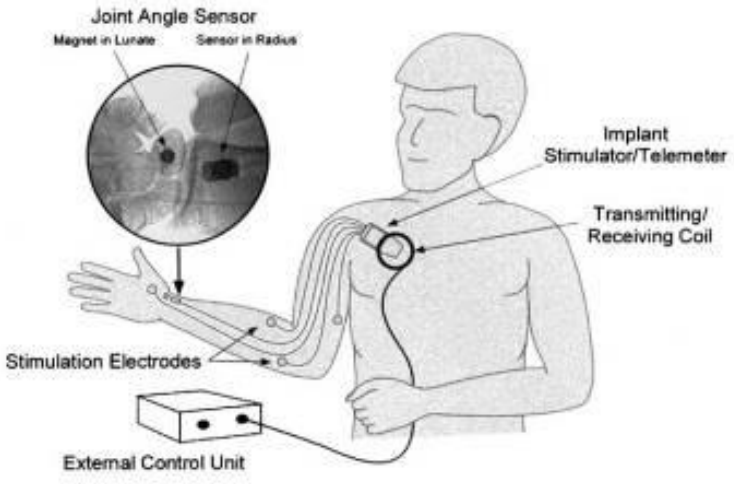

Fig. 1.6 FES system for hand and arm functions [8]

A typical FES system of this kind consists of the following components,

- External control unit: provides power, control signals for different grasping patterns to the stimulator. This is controlled externally by the user and information and power is transferred wirelessly to the implanted stimulator.
- Transmitter: Transmit power and information to the implanted stimulator.
- Receiver: Receives information from the transmitter and transfer it to the stimulator.
- Stimulator: Provides stimulus to the sites of stimulation based on the information from the external control unit.
- Electrodes: implanted on desired muscles and nerves as sites of stimulation.

In this particular system in [8], additional joint angle sensors are implanted at the wrist to detect wrist movements as an alternative control mechanism to trigger various grasping patterns.

In general, FES helps to restore different body functions by stimulating different groups of muscles or nerves. The trigger for stimulation can be from external control of taken from neural signals within the body. Cortex-based FES systems records neural signals from the brain cortex, decodes them and send processed information to stimulators for adequate stimulation. However, these systems are not preferred due to the involvement of the brain. Identifying the correct neural signals from the brain cortex and implantation on the brain cortex prove to be a challenge for researchers till this day. Any slight mistake can lead to disastrous results. An alternative solution is to record neural signals from peripheral nerves rather than the brain cortex. This reduces the risk of damage to the brain and identification of the correct neural signals to be recorded is also easier.

1.2 Muscle conduction techniques [1], [9]

FES has proved to be effective in restoring body functions due to neural damage especially spinal cord injury. This is achieved by electrically stimulating different groups of nerves or muscles depending on the application. In this section, the mechanism behind muscle conduction due to electrical stimulation is described.

To understand how muscle conduction works, it is important to learn about the chemical composition of the muscle environment. For brevity, focus will be placed on the main ions responsible for muscle conduction, namely sodium ions, Na^+ and potassium ions, K^+. Muscle conduction due to electrical stimulation works exactly the same way as nerve conduction, except that stimulation threshold for muscles is higher than that for nerves, which will be described later.

The muscle membrane forms a boundary that separates fluids within and outside the muscle cell. At rest, ions composition in both intracellular fluid and extracellular fluid creates a transmembrane potential of about -90mV, where the potential outside the muscle cell is taken as reference at 0V. This transmembrane potential of -90mV is also known as rest potential. The rest potential of a nerve cell is -70mV. Fig. 1.7 presents a simplistic view on the movements of ions and potential changes across the muscle membrane at rest.

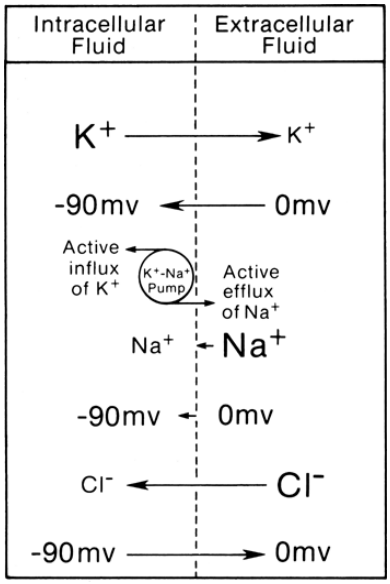

Fig. 1.7 Simplified view of Na^+, K^+ and Cl^- steady state fluxes

The K^+-Na^+ or Na-K pump in Fig. 1.7 is an enzyme that is present in the plasma membrane of every human cell to keep intercellular ions concentration at constant levels. For K^+, the efflux of K^+ across the membrane, due to concentration gradient and electrical force induced by transmembrane potential, is equal to the influx of K^+ due to the Na-K pump. Similarly, influx of Na^+ due to concentration gradient is low due to membrane resistance and electrical force across the muscle cell membrane. This is balanced by the efflux of Na^+ by the Na-K pump. Lastly, the concentration gradient of Cl^- exactly counters the electrical force causing no net movement of Cl^- across the membrane. Hence, Cl^- ions do not play a major role in muscle conduction.

During stimulation, electrons enter the extracellular fluid through the cathode electrode making the extracellular environment more negative, thereby increasing the transmembrane potential. This process is known as cathodal depolarization. Once the transmembrane potential increases to -55mV, an action potential is produced. This potential of -55mV is referred to as the threshold potential because any other potentials lower than this value will not induce any action potentials. Threshold potentials of both muscle cells and nerve cells are the same. In other words, to develop an action potential in a muscle cell, the transmembrance potential is required to increase from -90mV to -55mV, i.e. a magnitude of 35mV. This is higher than what is required to trigger nerve cells where the difference in rest potential, -70mV, and threshold potential, -55mV, is only 15mV. This explains why direct stimulation of muscles requires higher current levels than stimulating nerves.

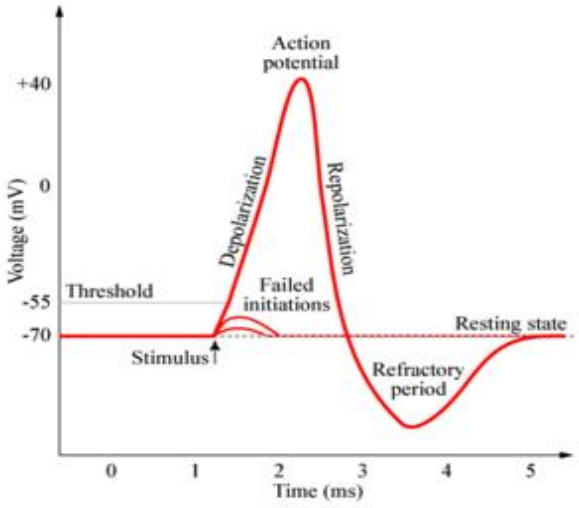

Fig. 1.8 Features of an action potential

An action potential is an event where the transmembrane potential rises and falls rapidly as shown in Fig. 1.8. Action potentials are neural signals responsible for information transfer along the nerves. During the depolarization phase, once the threshold potential is reached, Na^+ channels on the cell membrane are opened, allowing high concentrations of Na^+ ions to diffuse into the nerve or muscle cell due to increased permeability of Na^+ across the membrane. The increase in Na^+ concentration within the cell increases the intracellular potential resulting in a positive potential as high as +40mV. After which, the permeability of Na^+ drops while permeability of K^+ increases, creating an efflux of K^+. This lowers the transmembrane potential towards the rest potential. This phase is known as repolarization phase. During the refractory period, the Na-K pump tries to achieve the equilibrium between the concentration of Na^+ and K^+ ions concentration across the cell membrane back to the rest state. This completes one cycle of an action potential.

The fact that neural signals can travel along the nerves is because once an action potential is triggered at a spot on the cell membrane, it creates an intracellular current of Na^+ ions that flows into the adjacent regions, depolarizing those regions as well as shown in Fig. 1.9.

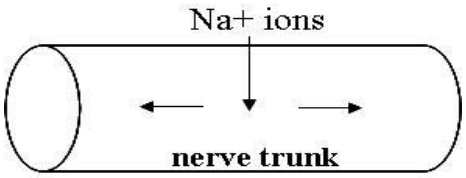

Fig. 1.9 Intracellular current during stimulation

When the adjacent regions reach threshold potential, action potentials are triggered at those regions which in turn give rise to more intracellular currents in more distant regions.

1.3 Types of stimulus waveforms

In FES, electrical stimulation involves passing current into the body, inducing action potentials in nerves or muscles which leads to muscle contractions. In this section, different types of stimulus waveforms will be described. Due to the adaptable nature of nerve and muscle fibers, if current injection occurs at a slow rate, muscle or nerve tissues will gradually adapt to the current level and redistribute the charges injected. When this happens, action potentials will not be triggered, meaning to ensure successful stimulation to take place, electrons injection has to be rapid or the increase in current has to be sudden. Hence, stimulation waveforms are usually rectangular in nature where current increase is almost instantaneous [1].

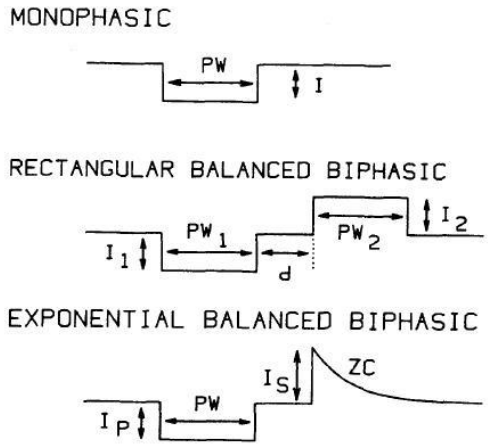

Fig. 1.10 Types of stimulation waveforms

There are three main types of stimulation waveforms as shown above, namely monophasic, rectangular balanced biphasic and exponential balanced biphasic [10], [11].

- Monophasic: consists of a repeating unidirectional or single phase stimulus commonly used in surface electrode stimulation.
- Rectangular Balanced Biphasic: consists of a cathodic phase to excite the nerves/muscles and an anodic phase that neutralizes the charge accumulated during the cathodic phase. Both cathodic phase and anodic phase are square-shaped and are supplied by active circuits. Delay between cathodic phase and anodic phase is known as interphasic delay. This is necessary to ensure that the effects due the cathodic phase are not neutralized immediately by the anodic phase. Else, excitation may not occur [12]-[15]. It is also reported that if the interphasic delay is longer than 80us, there is little difference between monophasic and biphasic waveforms in terms of tissue damage due to stimulation [10].

- Exponential Balanced Biphasic: similar to rectangular balanced biphasic. Only difference is that anodic phase is exponentially decaying. This is achieved with either a series blocking capacitor or a capacitive electrode.

In both rectangular balanced biphasic stimulus and exponential balanced biphasic stimulus, the amount of charge during the cathodic phase equals to that in the anodic phase. Both stimulus aims to achieve charge balance so as to reduce tissue damage from stimulation, to be described later.

1.4 Effects of stimulus parameters on stimulation

Referring to Fig. 1.10., each stimulation waveform is defined by three main parameters, namely, current amplitude, current pulsewidth and frequency. In this section, the effects of these parameters on responses generated from stimulation are described.

1.4.1 Lapicque's Law

In the 1990's, the principles of stimulation that describes the relationship between current amplitude and pulsewidth were introduced. This relationship, known as Lapicque's Law, named after a French neuroscientist Louis Lapicque, is shown in Fig. 1.11 [1].

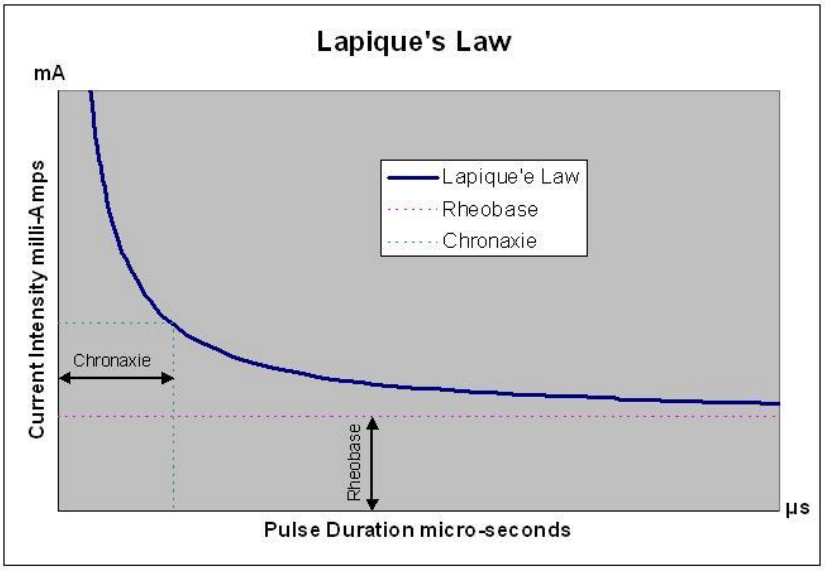

Fig. 1.11 Lapicque's Law

The above graph reflects that stimulation current intensity or amplitude is inversely proportional to current pulsewidth. In other words, an action potential can be triggered by either using a large current amplitude with small pulsewidth or small current amplitude with large pulsewidth. Lapicque defined two parameters, chronaxie and rheobase to describe the nature of stimulation. Rheobase is defined as the minimum stimulation current amplitude needed to trigger an action potential, independent of pulsewidth. Chronaxie is defined as the minimum stimulation pulsewidth for action potential to be triggered when current amplitude is twice the rheobase.

Over the years, research has been ongoing to investigate how parameters like current amplitude, pulsewidth and frequency affect stimulation. In-vivo experiments have been carried out on animals like rabbits, monkeys, cats, dogs and rats to observe muscle movements due to stimulation of different parameters.

In [16], biphasic current pulses of different amplitudes and pulsewidths were delivered to Long Evan rats subject and twitch threshold or stimulus amplitude needed for observable muscle twitch versus stimulus pulsewidth data were plotted as shown in Fig. 1.12.

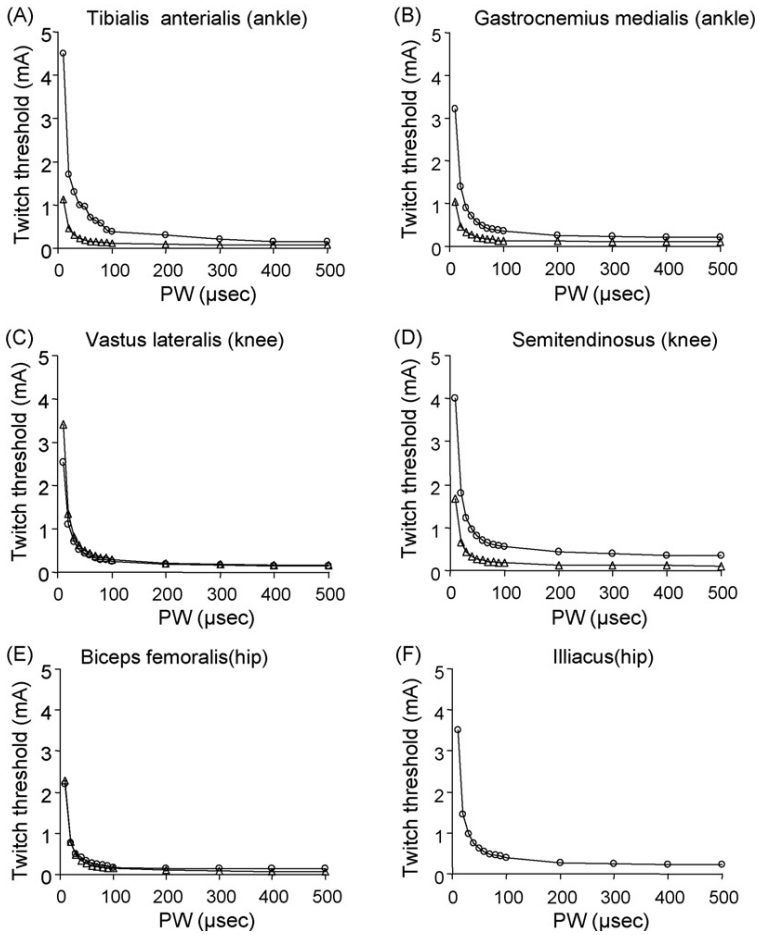

Fig. 1.12 Strength duration curves for different hindlimb muscles

Regardless of the stimulated muscle type, all six plots follow the trend described by Lapicque's Law as seen in Fig. 1.11. This proves the validity of Lapicque's Law and the relationship between stimulus amplitude and pulsewidth. From these experiments, average rheobase values for all muscles range between 0.14mA to 0.18mA. Chronaxie

values range from 40us to 90us. With that, the average minimum stimulus amplitude and pulsewidth to achieve observable muscle twitch is around 320uA and 65us respectively.

1.4.2 Stimulus amplitude versus generated muscle force

In [10], in-vivo experiments were done on adult cats and the force produced through electrical stimulation of the medial gastrocnemius muscle is measured using a rigid strain gage force transducer attached to the Achilles tendon. The figure below shows the measured force (normalized to a maximum force of 11.8N) versus stimulation amplitude. Stimulation pulsewidth is fixed at 30us.

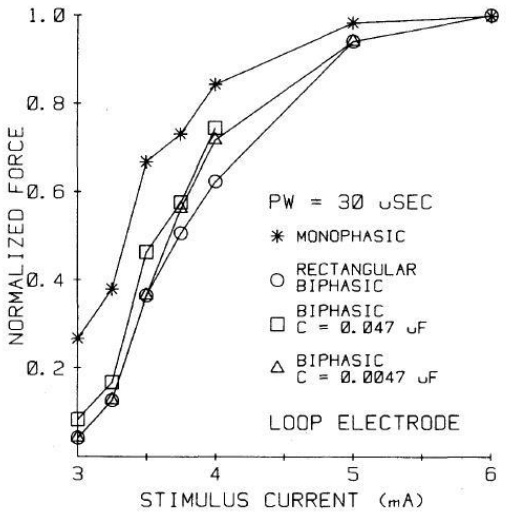

Fig. 1.13 Stimulation induced force versus stimulus current amplitude

Stimulation is done using all three types of stimulus waveforms, namely monophasic, rectangular balanced biphasic and exponential balanced biphasic with different discharging capacitor values. As shown in Fig. 1.13, as stimulus current increases, the

force measured increased as well. This shows that stimulation induced muscle force is directly proportional to stimulus current, irregardless of the type of stimulus waveform used. Another implication that can be inferred from the experimental results above is that monophasic stimulus produces a greater force at any stimulus current level than biphasic stimulus. This may be due to some cancellation effect on stimulation by the anodic phase in biphasic stimulus waveforms.

1.4.3 Stimulus pulsewidth versus torque generated

In [16], the effect of stimulus pulsewidth on torque generated due to single pulse twitch stimulation is investigated. Torque produced is calculated based on the forces and moments measured in all three dimensions. In this experiment, the current stimulus amplitude is fixed based at 1.5 times the twitch threshold current for 40us pulsewidth pulse obtained in Fig. 1.12.

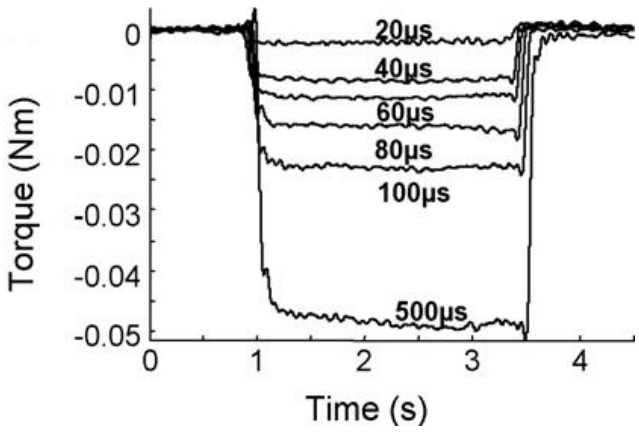

Fig. 1.14 Torque versus stimulus pulsewidth

Fig. 1.14 show that increasing pulsewidth leads to greater torque being generated. Hence, similar to stimulus amplitude, increasing stimulus pulsewidth results in greater muscle contraction.

1.4.4 Effect of stimulus frequency on stimulation response

Lastly, in [16], the effect of stimulation frequency on generated force from stimulated muscle was also investigated.

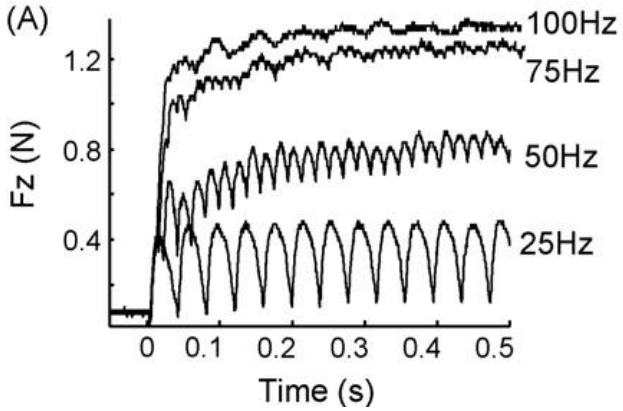

Fig. 1.15 Generated force due to stimulation versus stimulation frequency

Stimuli of fixed amplitude and pulsewidth but varying frequencies are delivered to the muscle and the measured force is shown above. As stimulation frequency increases, the measured force becomes more graded. Hence, this shows that to get a more gradual and steady response, stimulation is to be done at a higher frequency. Else, the response obtained from low frequency stimulation is simply a series of twitches. This probably will not provide any useful movements due to stimulation. However, if frequency stimulation is too high, it will lead to muscle fatigue [17].

Having investigated how primary stimulation parameters like stimulus amplitude, pulsewidth and frequency affect response generated from stimulation, it is also noteworthy to mention other secondary factors that may affect achieved responses. These includes distance between implanted electrode and desired muscle/nerve to be stimulated, types of electrodes used, size of nerve or muscle to be stimulated and also the condition of biological environment for stimulation [10], [18].

1.5 Stimulation electrodes and electrode circuit model

As seen from the applications described in section 1.1, electrodes act as the interface between the nerve/muscle tissues and the FES circuitry. They are the pathways for electrical signals to be transferred to the nerves/muscles for stimulation and also for action potentials to be picked up by circuits for neural recording. This is why electrodes are made from semiconductor materials like silicon for easy fabrication with metal, eg. Platinum, tips for electrical conductance. Electrodes can come in different packages like cuff electrodes where electrodes are wrapped around the nerve trunk or electrode arrays where electrodes are implanted across nerves or muscles in a planar way [19]. Fig. 1.16 shows the electrical equivalent circuit for a typical electrode.

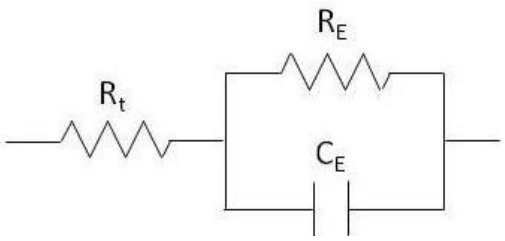

Fig. 1.16 Equivalent circuit model for an electrode

The electrode model shown in Fig. 1.16 consists of three main devices [20], [21]:

- R_t: tissue resistance (600Ω to 5kΩ)
- R_E: electrode/tissue interface resistance (1kΩ to 10kΩ)
- C_E: electrode/tissue interface capacitance (≈100nF)

The resistance and capacitance values given are based on literature and most papers simply model the electrode as a single resistor ranging from 1kΩ to 10kΩ. The total resistance across the electrode, i.e. $R_t + R_t$, limits the amount of current that can be delivered to the nerve/muscle tissue for stimulation.

1.6 FES and tissue damage

These days, most FES systems are implanted into the human body. Ideally, implanted FES systems must cause minimal damage to the human body for these to be valuable for medical research. Hence, biocompatibility of such systems becomes a critical issue. One such aspect is the tissue damage due to stimulation. To investigate tissue damage due to chronic stimulation, in-vivo experiments are conducted where animals are electrical stimulated continuously for hours and tissue damage around the stimulated region is quantified.

A comparison study on tissue damage caused by different stimulus waveforms is presented in [22]. It is reported that tissue stimulated with monophasic stimulus results in larger area of tissue damage than biphasic stimulus. The experimental results are shown in Fig. 1.17.

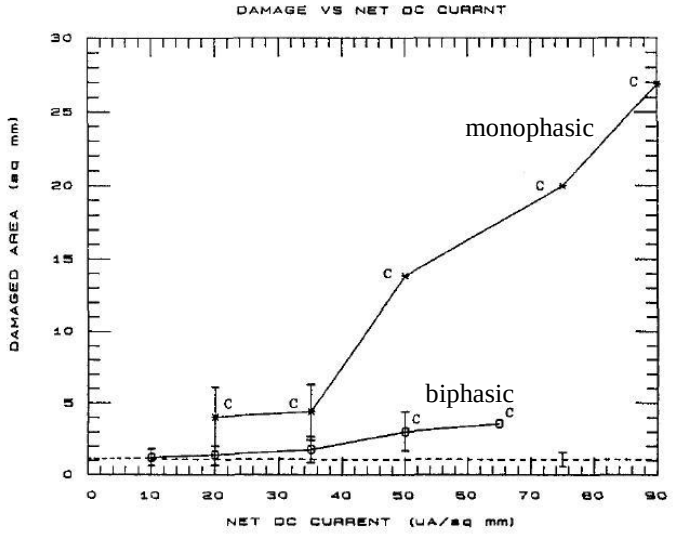

Fig. 1.17 Tissue damage versus net DC current

It is clear that monophasic stimulation causes much more tissue damage than biphasic stimulation. Also, higher stimulus amplitude results in larger areas of tissue damage. According to [22], tissue damage includes zone of degenerating and regenerating muscle fibers with scattered polymorphonuclear leukocytes, and a zone of coagulation necrosis.

Tissue damage occurs largely near the proximity of the electrode. Factors causing tissue damage from stimulation is still unclear at the moment. Most papers attribute tissue damage due to stimulation to electrochemical processes occurring at the electrode/tissue interface causing pH change in the biological environment near the electrode [23]-[25]. This explains why biphasic stimulation results in lesser tissue damage than monophasic stimulation. Electrochemical processes at the electrode surface are largely due to residual charges at the electrode after stimulation. In biphasic stimulation, the second phase helps to neutralize any residual charges on the

electrode after stimulation, thereby reducing the occurrence of electrochemical processes. Residual charges on the electrodes can cause corrosion on the electrode surface as well [25]. Electrode corrosion is undesirable as the state of the electrode affects the efficiency of stimulation and also, corroded electrodes have to be replaced, resulting in surgery needed for the removal of corroded electrodes and implantation of new ones.

In modern day FES applications, tissue damage due to stimulation becomes a critical issue. This is especially true for implanted FES systems where chronic stimulation is applied to the muscles or nerves over long periods of time. Tissue damage around the electrode not only jeopardizes the well-being of the patient using the FES system, it also reduces the effectiveness of stimulation. This is why implanted FES stimulators only output charge-balanced biphasic stimulus to reduce tissue damage caused by stimulation.

In-vivo experiments in [25] show that for monophasic stimulation, no increase in tissue damage is observed at current densities of $10uA/mm^2$ ($0.2uC/mm^2$/stimulus pulse at 50Hz) and for balanced biphasic stimulation, current densities can be higher at $0.4uC/mm^2$/stimulus pulse at 50Hz. These values have been used as safety tolerance levels for stimulation.

Other aspects on biocompatibility of implanted FES systems include,

- Biocompatibility of electrode material: implanted electrodes must not react with the biological environment and the physical properties of the electrode must not deteriorate over time
- Implantation techniques: implanting electrodes into the body causes physical damage to the tissue.

1.7 Scope and organization of thesis

This research project is part of an FES system that aims to restore hand functions for patients suffering from nerve damage such that nerve signals from their brain cortex can no longer travel to their hand muscles due to nerve denervation caused by the injury. The main idea behind this FES system is that neural signals from peripheral nerves are recorded and these signals are processed and information is sent wirelessly over to the stimulator for stimulation. Fig. 1.18 gives a simplified pictorial view of the proposed FES system.

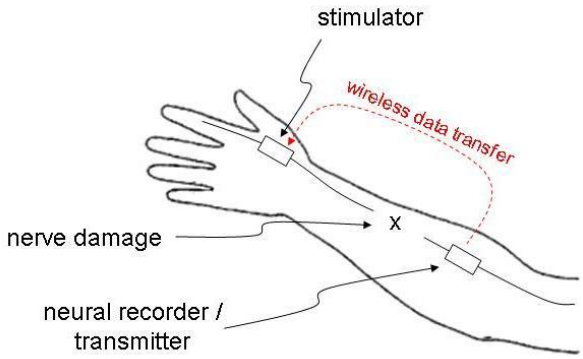

Fig. 1.18 Overview of proposed FES system

Typical to all FES systems, the proposed FES system consists of some standard components as mentioned below:

- Neural recorder with transmitter: records neural signals from intact nerves, process and decodes them and sends information to the stimulator wirelessly.
- Stimulator with receiver: receives information from neural recorder and stimulates muscles.
- Wireless power (not shown): provides power to all active circuits implanted within the arm.

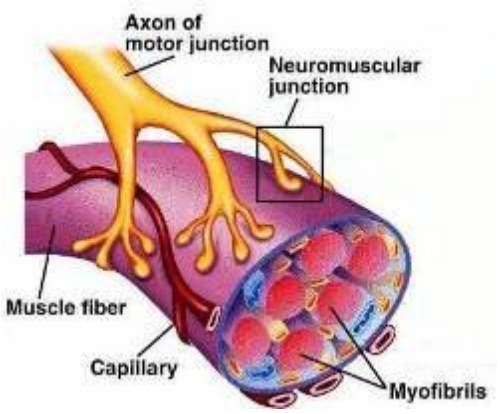

Fig. 1.19 Neuromuscular junction

Fig. 1.19 shows the target site of stimulation, i.e the neuromuscular junction, the interface between nerve and muscle. The neuromuscular junction is chosen as the site of stimulation because after a nerve injury that disconnects the nerves from the brain to the hand, the disconnected nerves connecting to the hand dies off after a while. Hence, nerve stimulation is not possible. In this proposed FES system, direct stimulation is done on muscles.

The main advantages of this system are as follows,

- Neural signals are recorded from intact peripheral nerves near the area of injury instead of the brain cortex, hence reducing risk of brain damage.
- System does not require an external control unit which can be bulky and cumbersome for its users.
- Transfer of data is done wirelessly, meaning no implanted wire leads are needed, thereby simplifying surgical process.

The scope of this research project covers the design and fabrication of a programmable stimulator that aims to produce rectangular charge-balanced stimulus with programmable amplitude, pulsewidth and frequency. A programmable stimulator means all three stimulation parameter must be tunable as it is difficult to quantify optimum parameters for stimulation. This is largely due to the nature of the biological environment where stimulation occurs. For example, stimulating the same muscle of different animals may require different sets of stimulation parameters to produce a similar response. Furthermore, the site of stimulation can differ between experiments and this will alter the stimulation environment because factors like distance of stimulation electrode from target muscle, cell damage due to electrode implantation and the condition of the muscle to be stimulated can be different. Hence, it is crucial that stimulation parameters can be adjusted such that if one set of parameters do not induce a reaction, these parameters can be tuned till a response is achieved. This will be described in more details in the later chapters.

This thesis begins by giving a brief history and introduction to FES, followed by some applications of FES and areas of concern involving stimulation. The subsequent chapters will provide reviews of previous work on stimulators and also detailed description of the entire design flow of the programmable stimulator from schematic design to layout and finally, measurement results. The stimulator is implemented using AMS CMOS 0.35um 2P4M technology. Finally, problems and limitations of stimulator design, proposed solutions and future work will be discussed in the last chapter.

CHAPTER TWO: REVIEW OF PREVIOUS WORK

2.1 Literature Review

To determine the specifications of the programmable stimulator, literature review is done to investigate previous published designs of stimulators, most of which have silicon measurement results and some were even used in in-vivo experiments. In the following sections, the design and specifications of six stimulators will be discussed. As mentioned in chapter one, charge balance is crucial for stimulation to reduce tissue damage. Therefore, the methods used to achieve charge balance and limitations of each stimulator will also be highlighted.

2.1.1 A Partial-Current-Steering Biphasic Stimulation Driver for Neural Prostheses [12]

This paper presents a 3-channel neural stimulator, implemented in AMS 0.35um 2P4M CMOS technology, for vestibular prosthesis. The block diagram of the overall system is shown below.

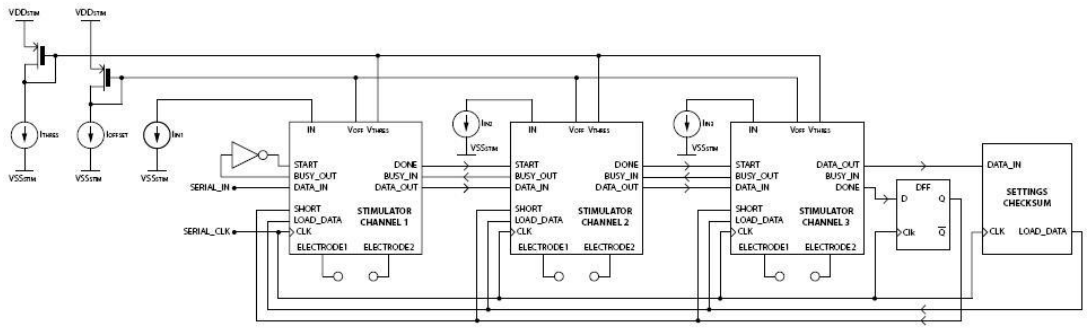

Fig. 2.1 Block diagram of stimulator

This stimulator incorporates a continuous-interleave-sampling (CIS) strategy to ensure only one channel stimulates at any time interval. Also, the overall system is mostly implemented using digital circuits, except for the current mirror network for generating output stimulus current. State machines and registers are used to store stimulation parameters received through wireless transmission and these are fully programmable by users. There are two binary-weighted DACs for each channel, a 3-bit DAC to allow tuning for patients threshold level (to set the minimum base current that a patient can feel a sensation) and a 6-bit DAC for gain control for larger stimulus current.

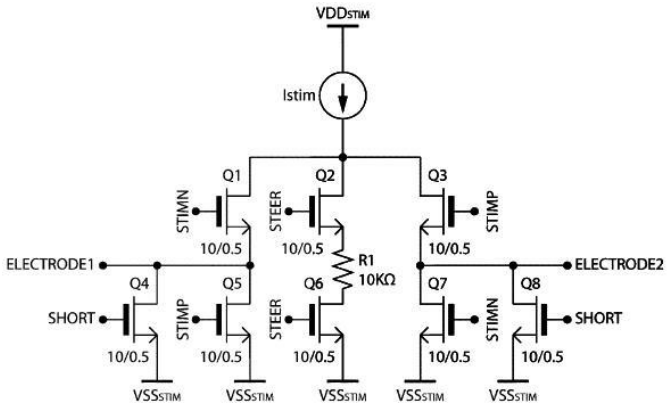

Fig. 2.2 Schematic for H-bridge with current steering

H-bridge configuration is used in this paper to deliver current in both directions to the electrode. Current steering technique is included such that prior to any turning on/off of the current mirror, current is steered from the output to a resistive load of 10kΩ for a short duration. This is to reduce glitches due to switching activity. This stimulator outputs a anodic-first, cathodic-last biphasic waveform. The ratio between the

cathodic amplitude and anodic amplitude is fixed at 4:1. To achieve charge balance, the anodic pulsewidth is set to be 4 times the cathodic pulsewidth. To ensure that there is no residual charge on the electrodes, they are shorted at the end of every stimulus waveform.

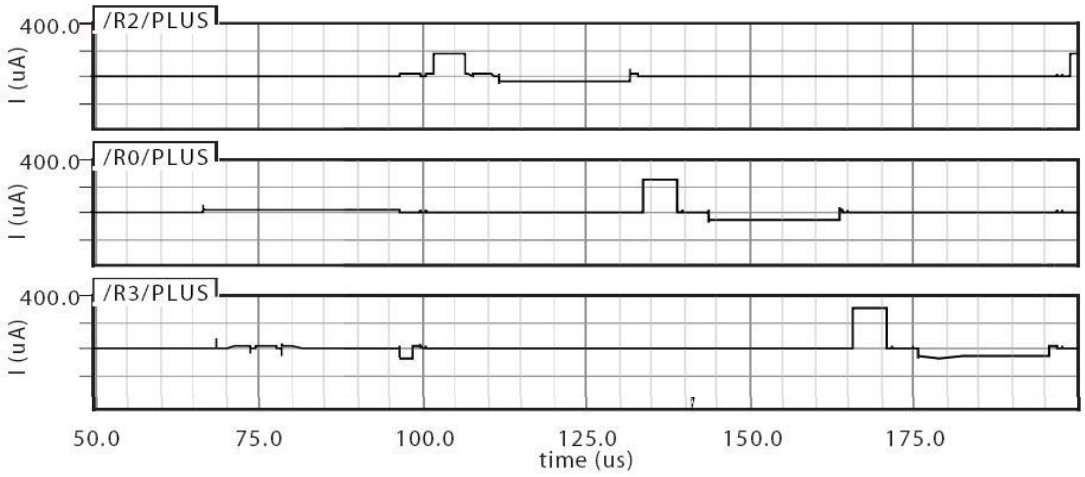

Fig. 2.3 Output waveforms of stimulator

Fig. 2.3 shows the output waveforms for 3 channels. It can be seen that the biphasic waveforms do not overlap each other and occurs in an interleaved manner. Although nothing has been mentioned about the interphasic delay, it can be inferred from above that the interphasic delay pulsewidth is the same as the anodic pulsewidth. Charge balance accuracy achieved is not mentioned.

Limitations of this stimulator includes,

- Ratio of anodic and cathodic current amplitude is fixed. Hence, pulsewidths are fixed as well.

- Irregularities can be observed on the waveforms implying that the stimulator may be delivering or sinking undesired charges from the electrodes.
- Current steering to transfer current to a resistive load leads to unnecessary power consumption during interphasic delay.

2.1.2 Towards a reconfigurable sense-and-stimulate neural interface generating biphasic interleaved stimulus [14]

This paper presents an eight channel neural stimulator using standard AMS 1P4M 0.35um technology. Fig. 2.4 gives an overview of the "sense-and-stimulate" system presented in [14].

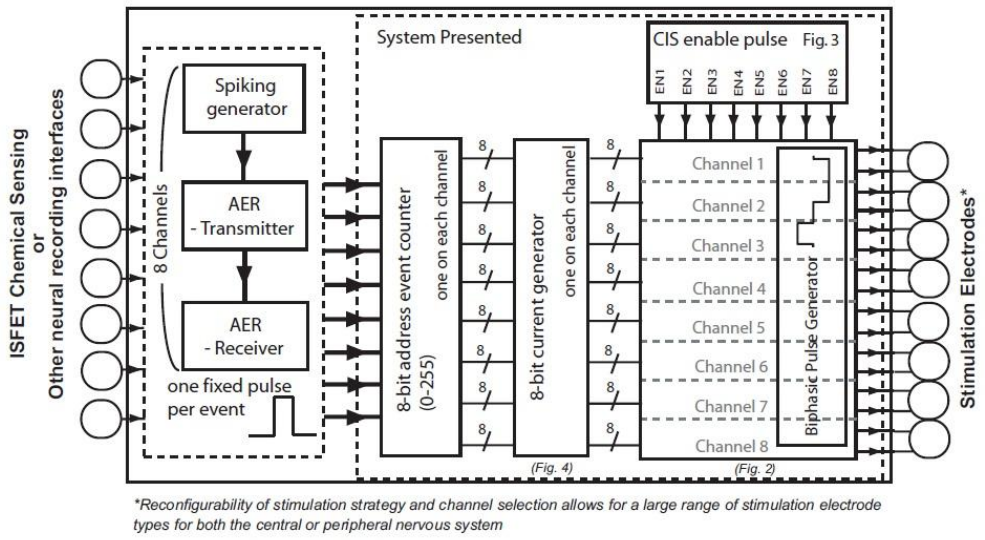

Fig. 2.4 System architecture

There are two main parts in the above system. The first part is the front-end of the system that consists of neural recording electrodes and circuitry to detect and sense any neural signals and these will be processed and decoded to activate a trigger for the

stimulator. Main focus in this paper is on the second part, i.e. the back-end of the system that is the stimulator. Stimulation parameters like amplitude, pulsewidth and frequency are generated within the system. First, stimulus amplitude is related to the neural spike or pulse rate detected by the front-end neural recording system, controlled with an 8-bit binary-weighted DAC. This parameter can also be programmed externally. Second, pulsewidth is controlled by counters and lastly, frequency of stimulation depends on the frequency of spike detection. Each stimulator channel outputs a stimulus in an interleaved manner such that at any time, only one stimulator gives an output. This is implemented based CIS strategy, similar to [12]. One reason behind this is to save power consumption such that the implanted circuit will not heat up too much causing tissue damage due to thermal heating.

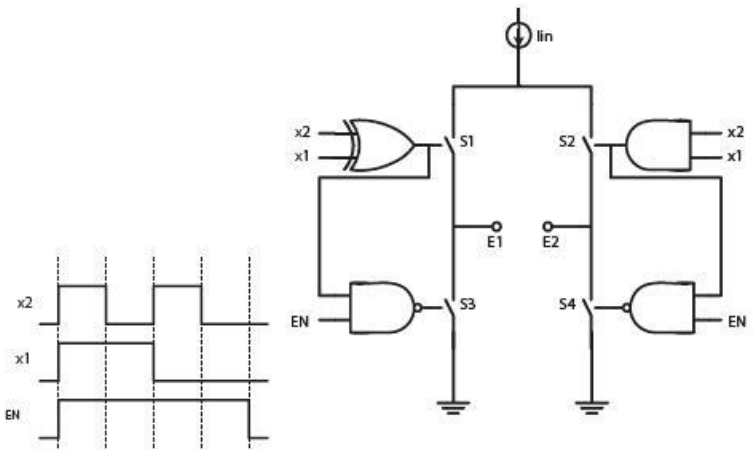

Fig. 2.5 Biphasic pulse generator to achieve charge balance

Fig. 2.5 shows the circuit for biphasic waveform generation implemented using the H-bridge configuration which is also used in [12]. Output current mirrors are

controlled by digital control signals, *x1* and *x2*, generated by a 2-bit ripple counter. *EN* signal depends on the DAC input code which determines which current mirrors to be turned on. E1 and E2 are the output terminals connecting to the electrode such that current can flow in both directions to the electrodes for both anodic and cathodic phases. This stimulator outputs an anodic-first, cathodic-last stimulus with a fixed interphasic delay.

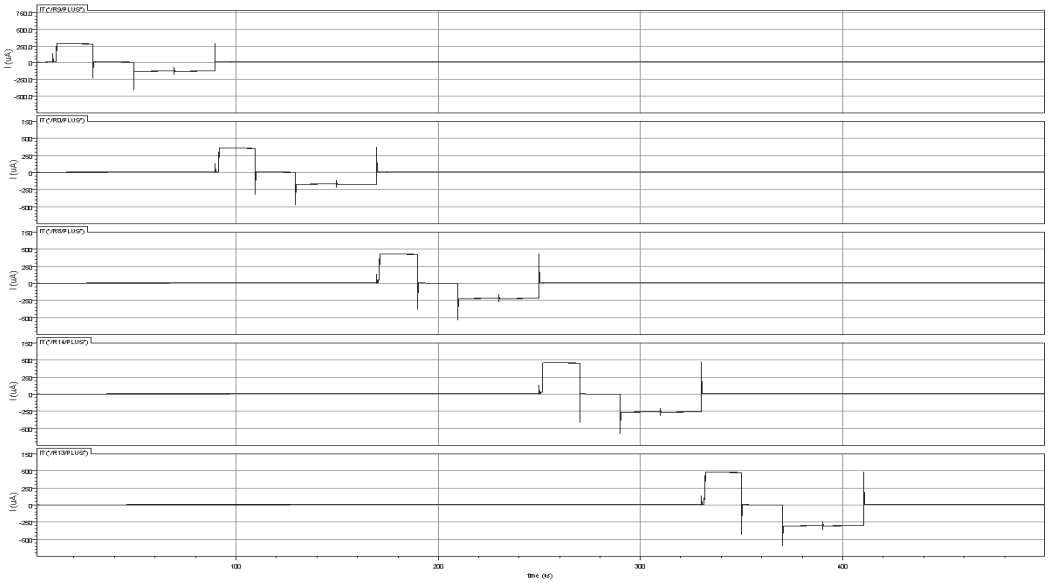

Fig. 2.6 Output waveforms of stimulator

Fig. 2.6 shows the output waveforms for five out of eight stimulation channels. It is clear that stimulus waveforms for each channel do not overlap each other. Also, the cathodic phase amplitude is set to be half the anodic phase amplitude. Hence, for charge balance, the cathodic pulsewidth is twice the anodic pulsewidth. However, there is no mention about the charge balance accuracy achieved.

Limitations of this stimulator include,

- Cathodic amplitude is always half the anodic amplitude. Hence, the cathodic amplitude is not programmable.
- Output waveform always consists of an interphasic delay that has the same pulsewidth as the anodic phase.
- Large glitches can be observed from the output waveforms. These glitches may cause unwanted twitches in the stimulated muscles.
- Stimulation pulsewidth is not programmable. Only way to adjust the pulsewidths is to change the clock frequency to the ripple counter.

2.1.3 An implantable ASIC for neural stimulation [21]

This paper presents a 4-channel neural stimulator, for stimulating motor muscles, realized using AMS 0.8um High Voltage CMOS technology. A block diagram of the overall system is shown below.

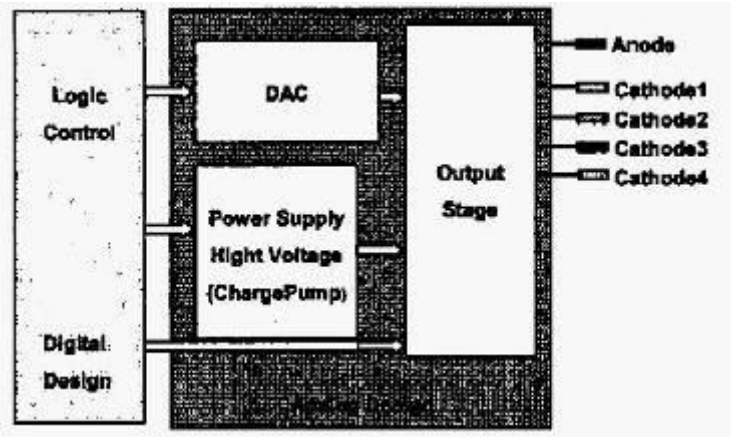

Fig. 2.7 Block diagram of stimulator

The stimulator system consists of the following,

- A digital logic control block (not described in the paper) that generates digital inputs for the DAC and nothing is mentioned about how stimulus parameters like frequency and pulsewidth are generated.
- An 8-bit DAC to provide different output current amplitudes.
- Power supply circuitry to provide power to the entire system.
- Output stage to amplify current output of the DAC and deliver current to all four outputs in different ratios at the same time.

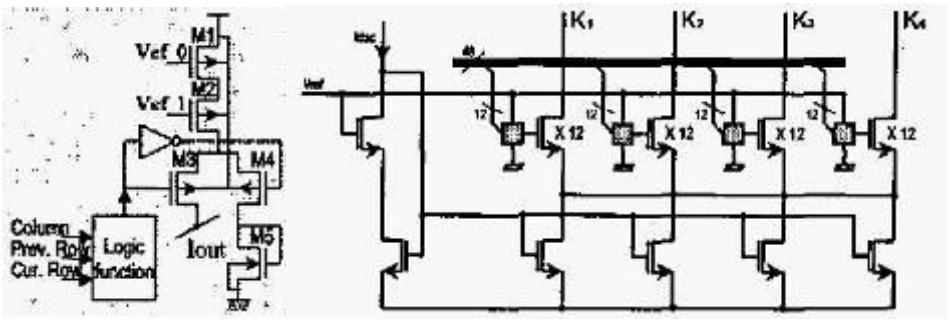

Fig. 2.8 Current cell of DAC and output stage

Fig. 2.8 shows the schematic of a single current cell of the DAC and an output stage. This is a current steering DAC where current either flows to the output Iout when M3 is on or through M4 to the ground terminal. Iout is then connected to the output stage to be amplified. There are four output terminals at the output stage, each connected to an electrode. In addition, each electrode is connected to a capacitor of 2uF in series to ensure there is no net DAC current caused by stimulation. Current output to each electrode is a ratio of the amplified current from the DAC. This stimulator outputs a biphasic anodic-first, cathodic-last stimulus with a cathodic amplitude fixed at 10% of

the anodic amplitude. However, there is no description of how the cathodic current is generated and scaled to one tenth of the anodic current.

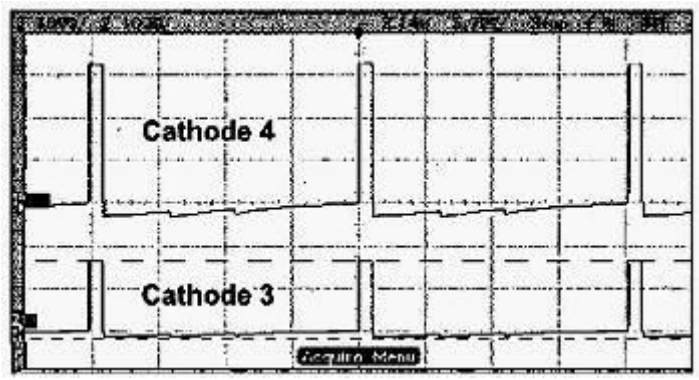

Fig. 2.9 Output waveforms for two channels

The output waveforms show that there is current output in both electrodes at the same time. In this case, the ratio of the current output at cathode 4 to that at cathode 3 is 2:1. Resistors are added sequentially, although not described in detailed, across all the electrodes to reduce the RC delay for discharging the series capacitor of each electrode, resulting in the 'jagged' current waveform during the cathodic phase. Charge balance accuracy achieved is not mentioned in this paper.

Limitations of this stimulator include,

- No option for interphasic delay.
- Current steering DAC results in wastage of power when current is 'steered' from the output to the ground.
- Cathodic amplitude is always one-tenth the anodic amplitude. Hence, the cathodic amplitude is not programmable.

2.1.4 Wireless Integrated Circuit for 100-Channel Neural Stimulation [26]

This paper presents a 100-channel neural stimulator, to stimulate motor and sensory nerve fibers, implemented in 0.6um 2P3M BiCMOS process. Fig. 2.10 shows a block diagram of the overall system.

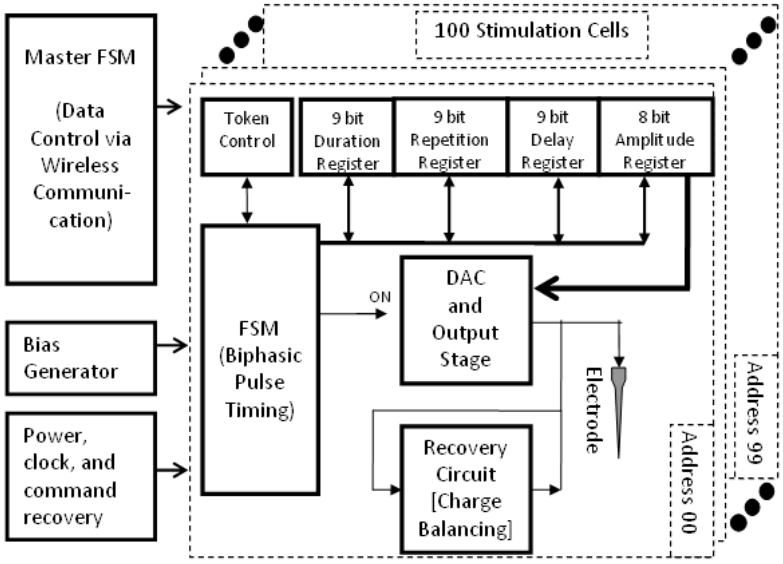

Fig. 2.10 Block diagram of overall system

The figure above shows the control circuitry along with a stimulator cell for a single channel. Each stimulator consists of four register to store information like stimulation pulsewidth (9-bit), frequency (9-bit), interphasic delay (9-bit) and amplitude (8-bit). Similar to [14], each of the 100 channels stimulates at different intervals and this is controlled by the token cell that prevents two stimulators to output current at the same time. Also, each stimulator has a DAC (8-bit), output stage, internal finite state machine or FSM for pulsewidth generation and a charge recovery circuit. The charge recovery circuit is used to provide current supply or sink to the electrode after a complete biphasic stimulus to ensure no residual charge is present on the electrode in

case charge balance is not completely achieved by the anodic phase. Components external to the stimulator cell consists of a master FSM for receiving data wirelessly and decoding received signals into digital input data, a bias generator to provide both current and voltage bias for all analog circuitry and a circuit block for power and clock control.

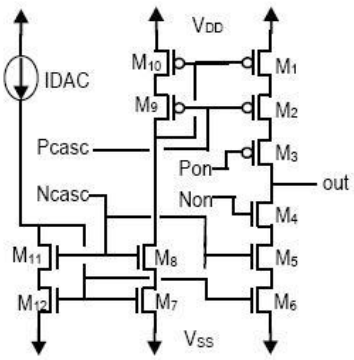

Fig. 2.11 Schematic of a single output stage

The output stage is a cascoded wide-swing (for high output resistance and high output swing) current mirror with current sourcing and sinking capability. Besides providing current output of opposite polarity, the output stage also amplifies the current of the DAC, i.e IDAC, by a factor of 10.

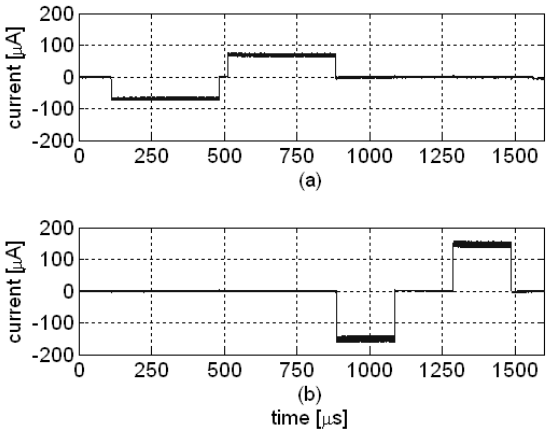

Fig. 2.12 Output waveforms for two channels

Fig. 2.12 shows the output waveforms of different current amplitude, pulsewidths and interphasic delay for two channels. It is important to note that these waveforms do not overlap each other, indicating that each stimulator cell outputs a current waveform at separate time intervals. Charge balanced is achieved by setting the same stimulation amplitude and pulsewidth for both cathodic phase and anodic phase. Charge balance accuracy is determined by how well matched the pMOS and nMOS transistors are at the output stage. In addition, any mismatch at the output stage leading to residual charges on the electrode will be removed by the charge recovery circuit. However, charge balance accuracy achieved and effectiveness of the charge recovery circuit is not mentioned in this paper.

Limitations of this stimulator include,

- Anodic amplitude and pulsewidth is always the same as that for the cathodic phase.
- Requires additional recovery circuitry to ensure charge balance is achieved

2.1.5 An Implantable Mixed Analog/Digital Neural Stimulator Circuit [27]

This paper presents a four channel stimulator, for restoring motor functions, implemented using MIETEC 2um CMOS technology. Figure below gives an overview of the stimulator.

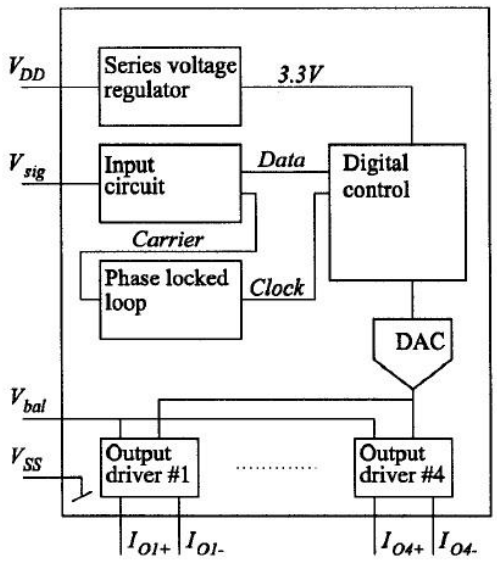

Fig. 2.13 Block diagram of stimulator

This stimulator consists of the following circuit blocks,

- Series voltage regulator: to regulate V_{DD} of 12V down to 3.3V for the digital control circuit
- Input circuit: extracts carrier for generating system clock and retrieving data transmitted to the stimulator.
- Phase locked loop: Generates accurate and stable system clock.
- Digital control: Process digital inputs for stimulation parameters like pulsewidth, amplitude and channel select.

- DAC (8-bit): Provide different levels of current output for stimulation.
- Output drivers: Current mirrors with control switches for current output of different polarity for biphasic generation and different current amplitudes.

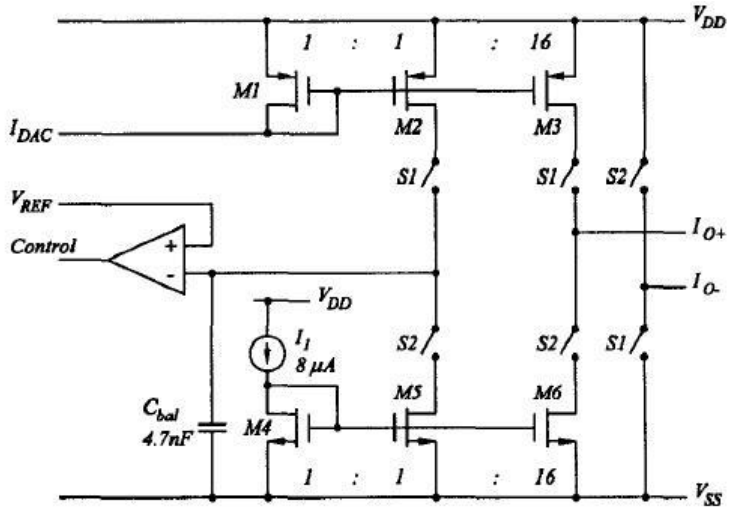

Fig. 2.14 Output driver stage

Fig. 2.14 shows the output driver stage for biphasic generation. The concept behind charge balance for this stimulator is to monitor the amount of charges introduced during both cathodic phase and anodic phase. This is done by mirroring and scaling down (in this case, factor of 16 is used) the output current to charge and discharge a capacitor. The voltage across this capacitor determines the amount of charges introduced in each phase. During the cathodic phase, switches S2 are on while switches S1 are off. Voltage across C_{bal} begins to drop until the cathodic phase ends. For the anodic phase, switches S1 are on while switches S2 are off. Hence, voltage across C_{bal} increases and once this voltage reach V_{REF}, the comparator output is used to end the anodic phase.

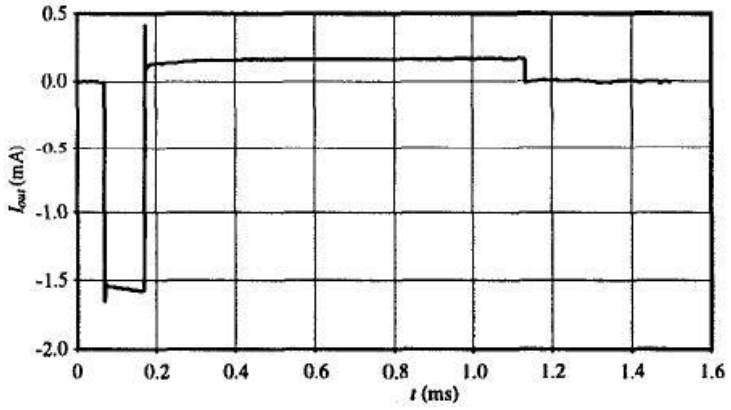

Fig. 2.15 Output waveform of stimulator

Fig. 2.15 shows a cathodic-first, anodic-last stimulus waveform without an interphasic delay. The anodic current amplitude is fixed at 128uA. In terms of charge balance accuracy, the mismatch of the amount of charges between cathodic phase and anodic phase is 5-10%.

Limitations of this stimulator include,

- Anodic current amplitude is always fixed at 128uA, irregardless of the cathodic current amplitude.
- C_{bal} is large (4.7nF) and has to be external.
- No option for interphasic delay.
- Large current glitches can be observed from the anodic phase of the output waveform (glitch amplitude at the anodic phase is approximately three times the anodic current amplitude).

2.1.6 A Matching Technique for Biphasic Stimulation Pulse [28]

This paper presents a single channel stimulator, using 0.5um high voltage CMOS technology, for neural prosthesis. Fig. 2.16 shows a simplified diagram of a biphasic stimulator.

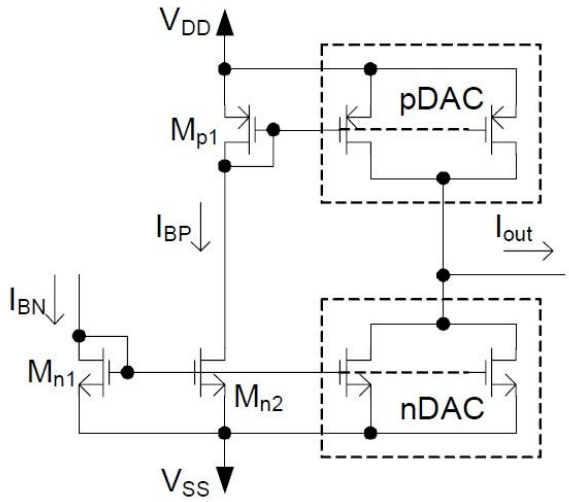

Fig. 2.16 Simplified diagram of a biphasic stimulator

In order to generate an output current in both directions, both pMOS DAC (pDAC) and nMOS DAC (nDAC) are required. nDAC provides current sink capability for the cathodic phase while pDAC provides current sourcing capability for the anodic phase. Although sourcing current can be done using nMOS transistors as well [12], [21], they suffer from body effect that will make current matching more difficult. Both nDAC and pDAC are biased using the same current source and the amplitude of the output current, Iout, is determined by the number of active current mirrors connected to the output node. Current mismatch is contributed by three factors. First, the biasing current for pDAC, I_{BP}, is a mirrored current from the current source, I_{BN}. Second,

mismatch can occurs between pDAC and nDAC in terms of linearity leading to different output current even when the input DAC code is the same. The third factor is due to the output impedance mismatch of both nDAC and pDAC.

This paper only focuses on solving current mismatch issue between the pDAC and the nDAC. Little information is given on the control and programmability of other stimulation parameters like frequency, pulsewidth and interphasic delay.

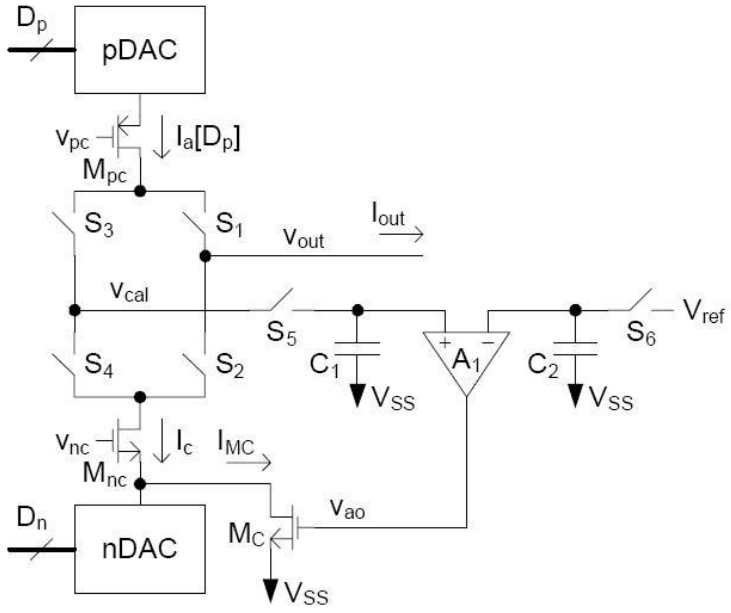

Fig. 2.17 Calibration operation to minimize current mismatch

The figure above shows the calibration method used to eliminate current mismatch between pDAC and nDAC. This stimulator outputs an anodic-first, cathodic-last biphasic stimulus. Anodic amplitude is determined by digital code D_p. Calibration is done during the interphasic delay. Both capacitors C_1 and C_2 are first precharged to Vref. Digital code, D_n is set to lower than D_p such that pDAC current is more than

nDAC current, creating a large mismatch. I_{MC} is the excess current due to mismatch from different input DAC codes and the other factors as well. I_{MC} charges C_1 causing an increase in voltage across C_1. The comparator outputs a logic '1', turning on transistor M_C that drains the excess current I_{MC}. In this way, M_C acts as a compensation transistor that provides additional current sink to reduce the current mismatch. In this way, the cathodic amplitude, I_c, is now the sum of I_{MC} and the current due to the nDAC and this current amplitude is equal to the anodic amplitude. After calibration, any current mismatch will be caused by charge injections from the switches.

Output waveforms are not presented in this paper but it is mentioned that without calibration, maximum current mismatch is 2% or 64uA for maximum current output of 3.2mA. With calibration, this mismatch reduces to 0.05% or 1.8uA for the same current output.

Limitations of this stimulator include,

- Calibration technique requires both cathodic amplitude and anodic amplitude to be the same.
- Time taken for calibration is 5us, meaning minimum interphasic delay has to be more than 5us. Therefore, there is no option to remove interphasic delay.

2.1.7 Comparison between reviewed stimulators

Having reviewed some stimulators in publications, a comparison is done on their specifications so as to set the basis to determine the specifications of the proposed stimulator in this project. Important specifications include stimulation parameters like amplitude, pulsewidth and frequency. This will reflect the typical range of values used for stimulation parameters. Most papers use a simple resistive load of different resistances, instead of the electrode equivalent model, described in Chapter One, for measurement results. All these information are tabulated below in Table 2.1.

Reference	**[12]**	**[14]**	**[21]**	**[26]**	**[27]**	**[28]**
Technology	0.35um 2P4M AMS CMOS	0.35um 1P4M AMS CMOS	0.8um HV CXZ AMS	0.6um 2P3M BiCMOS	2um MIETEC's CMOS	0.5um HV CMOS
Supply voltage	5V	3.3 V	3 V	5 V	12V (3.3 V for digital)	±8V and ±3V
DAC resolution and topology	6-bit (gain); 3-bit (threshold) binary-weighted	8-bit binary-weighted	8-bit thermometer-coded	8-bit R-2R	8-bit	7-bit binary-weighted
Stimulation amplitude range	Not mentioned	100uA to 5mA	up to 5mA (20uA step)	1uA to 255uA (1uA step)	up to 2mA	up to 3.2mA (25uA step)
Stimulation frequency	Not mentioned	100Hz to 20kHz	50Hz min	0.66 to 168Hz	Not mentioned	11.9Hz to 25kHz
Stimulation pulsewidth	Not mentioned	Not mentioned	20us to 1ms (5us step)	1.45us to 370us (725ns step)	up to 255us	10us to 635us
Interphasic delay	same as anodic pulsewidth	same as anodic pulsewidth	No delay	1.45us to 370us (725ns step)	No delay	10us to 635us
Output load used	Not mentioned	1 kΩ	Not mentioned	10 kΩ	2 kΩ	Not mentioned
Stimulus profile	Anodic-first, cathodic-last	Anodic-first, cathodic-last	Anodic-first, cathodic-last	Cathodic-first, anodic-last	Cathodic-first, anodic-last	Anodic-first, cathodic-last
Charge balance mismatch	Not mentioned	Not mentioned	Not mentioned	Not mentioned	5-10%	2% (w/o calibration) 0.05% (w calibration)

Table 2.1 Table of comparison on the specifications of different stimulators

2.2 Specifications of proposed programmable stimulator

Based on the previously published results and the targeted application, the following specifications have been decided for the stimulator to be designed and implemented in this project.

	Proposed specifications
Technology	0.35um 2P4M AMS CMOS
Supply voltage	1.8V to 3.3 V
DAC resolution and topology	10-bit hybrid topology
Stimulation amplitude range	10uA to 10mA
Stimulation frequency	10Hz to 100Hz
Stimulation pulsewidth	10us to 100us
Interphasic delay	< 80us (option to have no delay)
Output load used	100Ω to 10kΩ
Stimulus profile	Cathodic-first, anodic-last
Charge balance mismatch	5-10% or lower

Table 2.2 Specifications of proposed stimulator

2.2.1 Amplitude range

A wide range is chosen for amplitude because stimulus amplitude needed for muscle contractions induced from stimulation depends very much on the condition of the muscles, type of muscles to be stimulated and the distance between target muscles to be stimulated to the electrode. Hence, by having a wide range for output current, the amplitude can be adjusted in small steps till the desired amplitude is reached. For that, a 10-bit DAC is proposed.

2.2.2 Pulsewidth range

It has been reported in [10], [29] that stimulus with shorter pulsewidths results in better selectivity of nerve/muscle fibers and greater muscle contractions can be induced. Selectivity refers to the ability to target particular nerves/muscles to stimulate (especially small nerve/muscle fibers) without affecting other tissues in the proximity. In particular, *in-vivo* experiments in [10] reported that pulsewidths in the range between 10us to 100us results in greatest muscle contractions. This can be explained using stimulation theories described in chapter one. First of all, according to Lapicque's Law, stimulation pulsewidth is indirectly proportional to stimulation amplitude. Hence if short stimulation pulsewidths are used, amplitude must be large and large stimulus amplitude leads to greater muscle contraction. Also, the adaptability of nerve/muscle fibers described in chapter one mentioned that current injection has to occur at a fast rate, or else contractions may not be induced. Lastly, having large pulsewidth may result in a larger area of influence by the charges injected because charges are injected over a longer period of time [9]. This is why shorter pulsewidths result in better selectivity because if the area of influence is too large, spillover may occur [18], meaning that others muscles in the within the area of influence may be stimulated at the same time. This will lead to undesired muscle contractions causing undesired movement.

2.2.3 Interphasic delay range

Most papers do not give much detail on the significance of interphasic delay and such delay is not always present in stimulus waveforms as reflected in literature review. In fact, there are conflicting theories to whether an interphasic delay is required. It was reported in [10] that stimulus with zero interphasic delay provides best selectivity and biphasic stimulus with an interphasic delay of more than 80us results in similar effects on nerve/muscle tissues as a monophasic one. Other papers stated that interphasic delay is crucial to prevent the second phase to cancel out the effects of the first phase to ensure that nerve/muscle excitation occurs [12], [14]. Therefore, in order to investigate the significance of interphasic delay, the proposed stimulator must be able to produce biphasic stimulus with and without interphasic delay and this delay is limited to 80us.

2.2.4 Stimulus profile

Biphasic stimulus can either be cathodic-first, anodic-last or vice versa. Although there has no been any information on the implications on different biphasic profile, a cathodic-first, anodic-last profile has been chosen for this project. As mentioned in chapter one, in order to reach threshold potential of the nerve/muscle fibers, it is required to induce negativity outside the nerve/muscle cells. To do so, electrons must be injected and this is only possible via a cathodic current where electrons exits the electrode connected to the stimulator into the body.

2.3 The proposed muscle stimulators

In this thesis, two stimulators ("dual-slope stimulator" and "digital stimulator") with different charge balance schemes are proposed and implemented. The charge balance scheme in the "dual-slope stimulator" is analog in nature, while that in the "digital stimulator" is achieved using digital logic. Both stimulators have been fabricated in a single silicon chip.

CHAPTER THREE: DESIGN OF DIGITAL TO ANALOG CONVERTER

3.1 Architecture and schematic

3.1.1 DAC architecture

The main function of the DAC is to provide different current levels for stimulation, thus allowing stimulus amplitude to be programmable. A 10-bit DAC has been proposed to provide a wide range of current amplitude in small steps. Also, the DAC must have both current sinking and current sourcing capability so as to output current in both directions to the electrode. A simplified diagram of the DAC architecture is shown below.

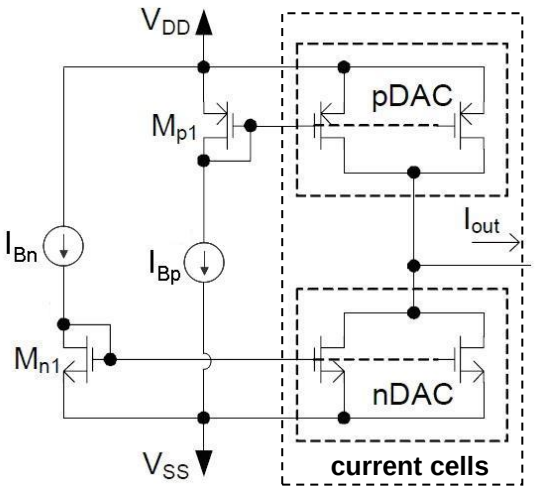

Fig. 3.1 Simplified view of DAC architecture

The above architecture is very similar to that shown in Fig. 2.16. The only difference is that instead of having a single biasing source, the pDAC and nDAC are biased separately to better match both currents. Biasing for the DAC is left external so that

biasing currents I_{Bn} and I_{Bp} can be tuned externally to match. This also allows the use of different supply voltages and the LSB current of the DAC to be tunable. In any case, main focus is not on the biasing circuitry but on the design and architecture of the DAC itself. The current mirrors of the pDAC and nDAC forms the current cells of the DAC.

Two common DAC architectures include thermometer-coded architecture and binary-weighted architecture. Thermometer-coded architecture gives better linearity and reduced glitching noise while binary-weighted architecture require much lesser transistors [30]. This is why high resolution DACs are usually implemented using a hybrid architecture consisting of both thermometer-coded and binary-weighted architectures [31]-[34]. The same hybrid architecture is also used for the 10-bit DAC in this project. Initially, a 2-bit LSBs binary-weighted, 8-bit MSBs thermometer-coded architecture with unit current cells was designed. The idea of allocating more bits to be implemented in thermometer-coded architecture and to use unit current cells (in this case 1023 current cells are needed for 10-bit resolution) is to achieve better linearity. However, the layout of the entire DAC with the current cells arranged in common centroid becomes too large to be practical for fabrication. Hence, the finalized architecture is a 2-bit LSBs binary-weighted, 4bit NSBs thermometer-coded and 4-bit MSBs binary-weighted. Unit current cells are used for the first 6-bits only while the last 4-bit MSBs use a larger current cell, equivalent to 64 unit current cells. For easy reference, the unit current cell will be referred to as

"LSB current cell" and the larger current cell will be referred to as "MSB current cell". In total, there are 63 LSB current cells and 15 MSB current cells. Thermometer-coded architecture for the NSBs is implemented with reference to [31].

By using mostly binary-weighted architecture and not using unit LSB current cells, the linearity of the DAC will be inevitably affected. However linearity of the DAC is not very crucial for this application because at any time, stimulation is done based on a single current level. Also, there is no specified fixed current value for stimulation. Hence even if the current steps are unequal, this does not affect the effectiveness of stimulation. Moreover, since both amplitude and pulsewidth are programmable, if a certain current level is too high or too low for a particular DAC input, the pulsewidth can be adjusted according, based on Lapicque's Law. Or, the DAC input can be reduced or increase as well to reach the required current level.

3.1.2 DAC schematic

For this project, since both versions are to be incorporated into a single chip, it makes sense to design such that both versions make use of the same 10-bit DAC. However, the dual-slope stimulator requires a scaled down version of the 10-bit DAC (to be explained in the next chapter). The current cells of both DACs are incorporated to form a single unit current cell. Fig. 3.2 shows the schematic of the LSB current cell along with each transistor's sizing in micrometers. MSB current cell has the same schematic just that the transistor's sizing are increased accordingly.

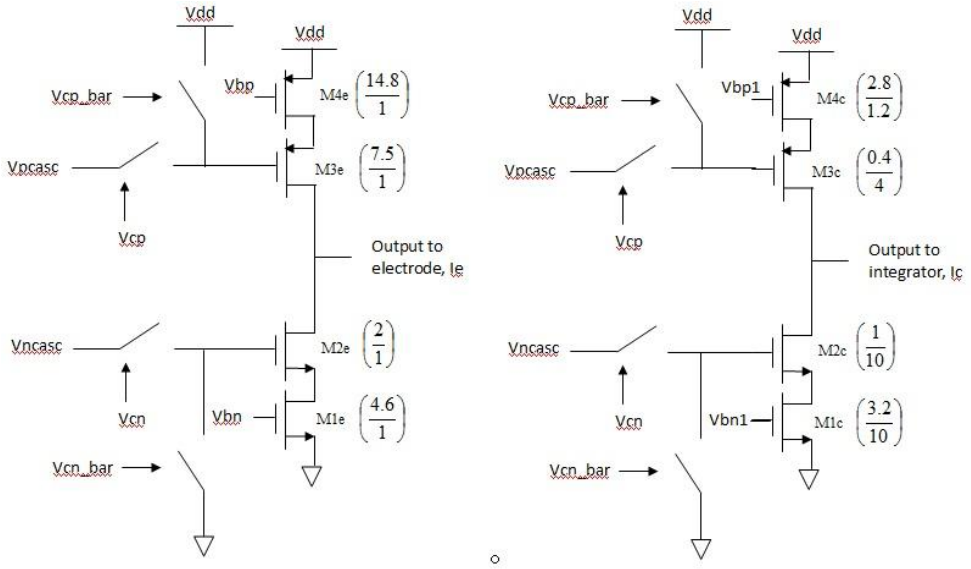

Fig. 3.2 Schematic of LSB current cell

From Fig. 3.2, there are two current mirrors, each biased separately by two current sources. The left current mirror has an output current of 10uA (1 LSB of the 10-bit DAC) while the one on the right has an output current of 1nA (1 LSB of scaled-down DAC). For the MSB current cell, the output current will be 640uA and 64nA respectively. The pMOS transistors correspond to the current cells of the pDAC and the nMOS transistors correspond to the current cells of the nDAC. For simplicity, both are combined together to form a single current mirror branch. Transistors M2e, M2c, M3e and M3c are cascode transistors that are used as switches as well. This increases the voltage headroom at the output rather than having three cascoded transistors where one acts solely as the switch. Also the cascade transistors are controlled via control signals, *Vcp* for pDAC and *Vcn* for nDAC. Here, a different switching scheme is used. Most DACs make use of current steering method to reduce switching glitches [31]-[34]. However, in this application, current steering

architecture results in wastage of power as shown in [12]. To reduce glitching, besides reducing the size of the cascode transistors to reduce parasitic capacitances at the output node, the control voltages of the cascode transistors, that act as switches as well, are limited to 0V to Vncasc for nMOS transistors, M2e and M2c, and Vdd to Vpcasc for pMOS transistors, M3e and M3c. Usually, switches are controlled using rail-to-rail voltages, causing large voltage change at the gates, causing switching glitches. By reducing the voltage change at the gate of the cascode transistors, glitches at the output node will also be reduced.

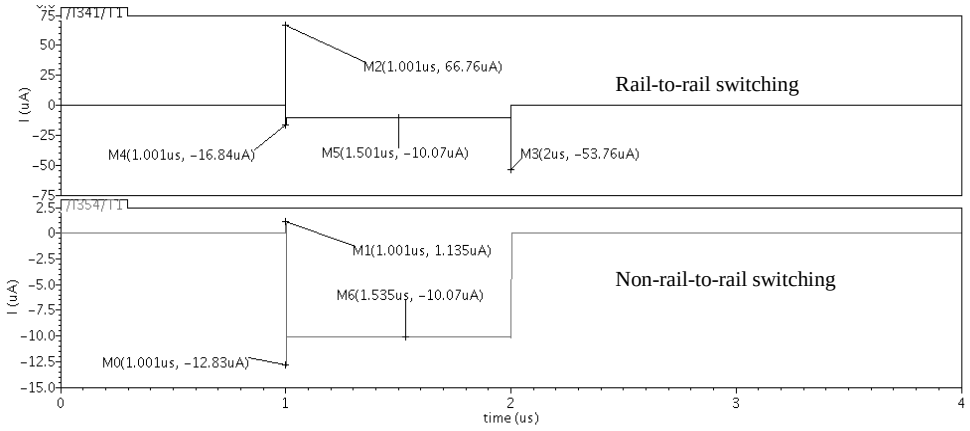

Fig. 3.3 Comparison between rail-to-rail and non-rail-to-rail switching

Fig. 3.3 shows cathodic current output of 10uA (1 LSB) using different switching schemes. It is obvious that if switching is not done from rail-to-rail, glitches are reduced at the output. This helps to prevent any unwanted twitches that may be caused by glitches.

3.1.3 DAC control logic

The main functions of the DAC are,

- to provide current sinking capability and current sourcing capability
- to be able to turn off all current output during interphasic delay
- able to output current in both directions during specific time period (i.e within desired stimulation pulsewidth)

As seen in Fig. 3.2, the cascode transistors are controlled by *Vcp* and *Vcn* for pMOS transistors and nMOS transistors respectively. These control signals determine when to turn on the pDAC for anodic stimulation or when to turn on the nDAC for cathodic stimulation also to turn off the entire DAC during interphasic delay. To generate these control signals, the DAC is controlled using three input signals, namely,

- *Din*: a 10-bit input that determines the digital code for DAC,
- *Phase*: a 1-bit digital input to determine if pDAC (*Phase* = logic '1') or nDAC (*Phase* = logic '0') is to be turned on,
- *Vc*: a 1-bit control signal such that when *Vc* is logic '1', there will be current output based on *Phase* and *Din* and when *Vc* is logic '0', there will be no current output irregardless of *Din* and *Phase*.

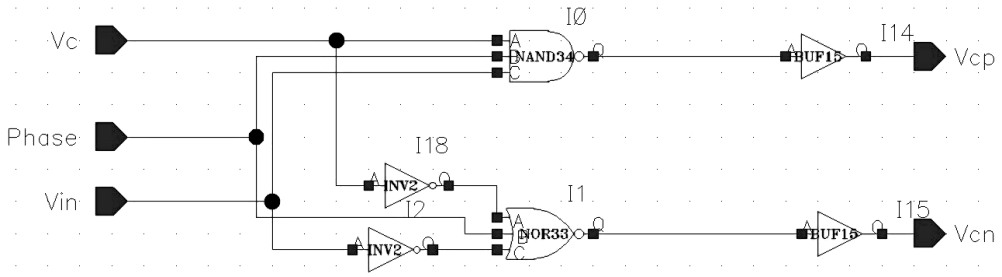

Fig. 3.4 DAC control logic

Fig. 3.4 shows the DAC control logic circuitry to generate *Vcn* and *Vcp*. Each current cell (both MSB current cell and LSB current cell) is controlled individually by this control logic circuit. Hence, there are a total of 78 (63 for LSB current cells and 15 for MSB current cells) of such control logic circuits. Table 3.1 gives the truth table of this digital logic circuit. Due to the hybrid architecture, *Vin* refers to different signals for different architecture. For LSBs and MSBs, *Vin* is a single bit in the first 2 bits and last 4 bits of the input DAC code, *Din* while *Vin*, for the NSBs (middle 4 bits), is an output from a thermometer decoder.

Vc	***Phase***	***Vin***	***Vcn***	***Vcp***	**Remarks**
0	x	x	0	0	No current output for interphasic delay and periods without stimulation
1	x	0	0	0	DAC input code is all logic ‘0’, therefore no current output
1	0	1	1	0	Cathodic current output
1	1	1	0	1	Anodic current output

Table 3.1 Truth table of control logic circuit

To summarize, Fig. 3.5 shows a block diagram of the DAC along with both input and output terminals.

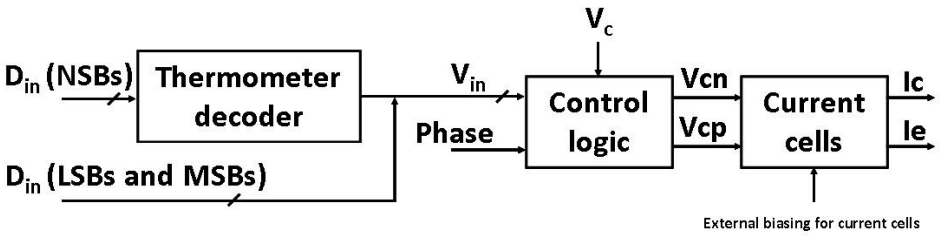

Fig. 3.5 Block diagram of 10-bit DAC

As shown in Fig. 3.5, the DAC has three inputs, *Din*, *Vc* and *Phase*, two output terminals, *Ie* and *Ic* and external biasing for the current cells. The next section describes the biasing of the DAC.

3.1.4 Biasing circuitry of the DAC

As mentioned before, biasing is left external to allow for tuning for better matching in pDAC and nDAC currents and also for different supply voltages. Cascode bias is also external via resistive dividers implemented on the PCB. Current cell bias is implemented as shown in the figure below.

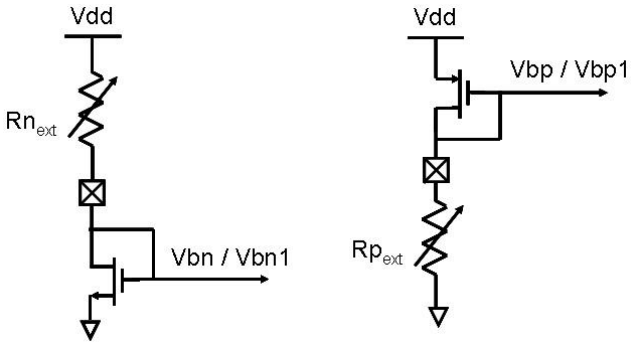

Fig. 3.6 Biasing current sources

The current source transistors are on-chip with their drains connected to external variable resistors. These resistors allow tuning for desired LSB currents for both

pDAC and nDAC even when supply voltage is changed. There are a total of 2 nMOS current sources, one to bias M1e and the other to bias M1c. The same goes for the pMOS current sources, one to bias M4e and the other to bias M4c. Both the current bias and cascode bias are used to bias all other circuitry like opamp and comparator in this proposed stimulator.

3.2 Layout and post-layout simulation

The DAC is implemented in Cadence and layout is drawn based on its schematic. Before starting on layout, schematic simulation is done to test the functionality of the DAC. To avoid repetitions, schematic simulation results are omitted since post-layout simulation results will be provided later in this section. Both LSB current cells and MSB current cells are arranged in common centroid for layout. Fig. 3.7 shows the layout of the LSB current cell and the MSB current cell respectively and Fig. 3.8 shows the layout of the overall 10-bit DAC.

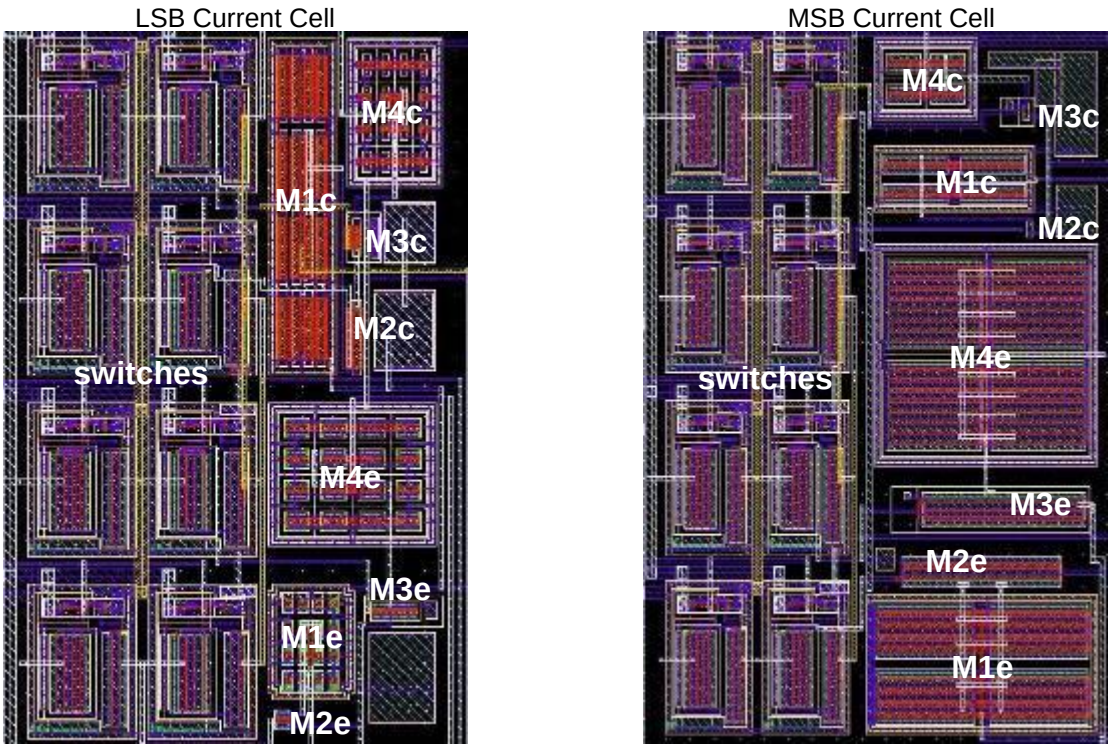

Fig. 3.7 Layout of LSB current cell and MSB current cell

Layout in Fig. 3.7 is labeled according to the schematic shown in Fig. 3.2. Dummy transistors are used for the current source transistors, M1e, M1c, M4e and M4c of the LSB current cell, for better matching. All current source transistors are split into four so as to arrange them in common centroid configuration. It can be seen that the transistors are larger in the MSB current cell and because of that, dummies are not used. Switches are implemented using transmission gates.

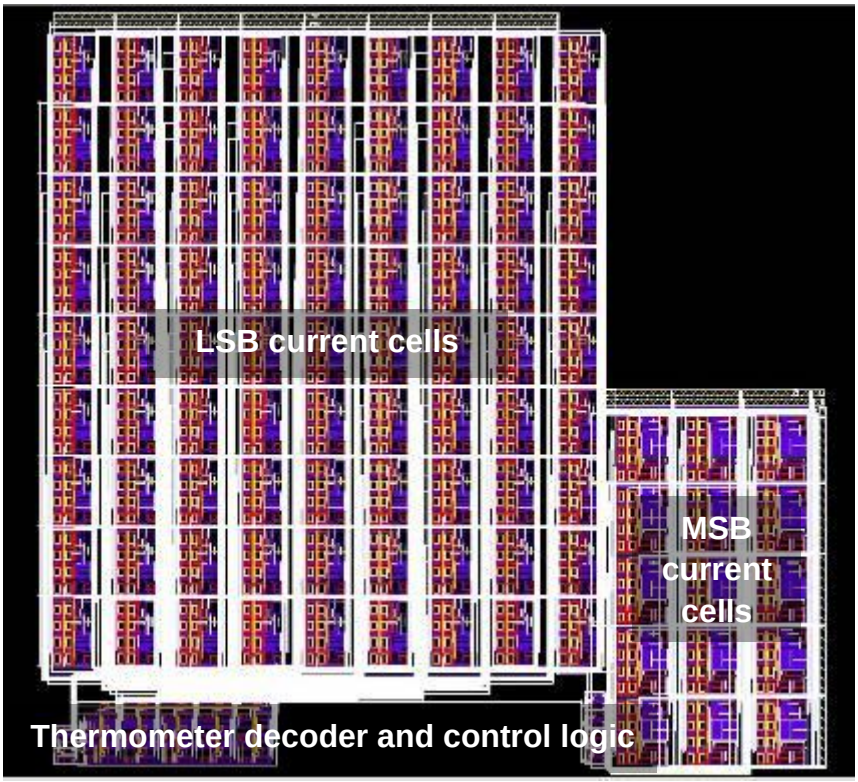

Fig. 3.8 Layout of entire 10-bit DAC

In all, the DAC consists of LSB current cells, MSB current cells, thermometer decoder for the NSBs and the control logic circuits for each current cell. Post-layout simulation is done after the layout is completed and the results for full-scale simulation of the nDAC and the pDAC are shown in Fig. 3.9 and Fig. 3.10 respectively.

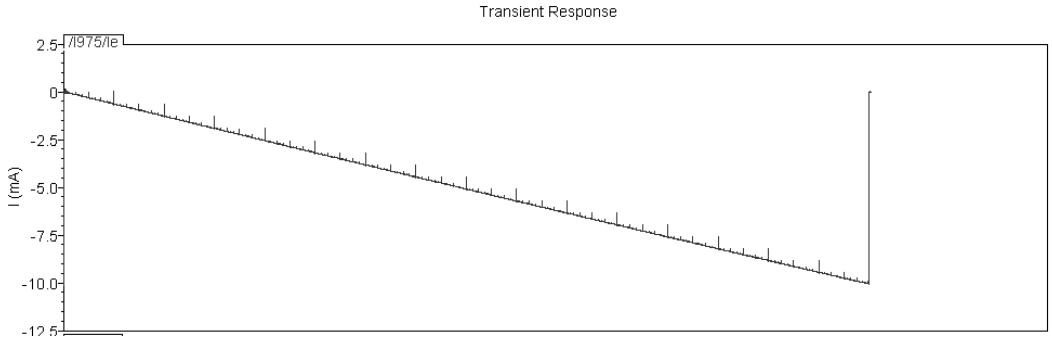

Fig. 3.9 Post-layout full-scale simulation for nDAC

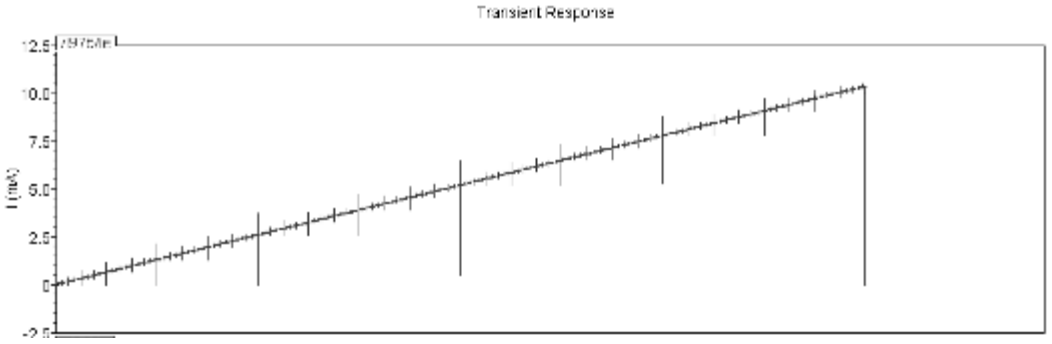

Fig. 3.10 Post-layout full-scale simulation for pDAC

Post-layout simulation shows that the implemented DAC is working and both pDAC and nDAC are able to output a current value ranging from 10uA to 10mA approximately.

CHAPTER FOUR: DUAL-SLOPE STIMULATOR

4.1 Design concept

In order to achieve charge balance, the amount of electrons injected into the body during cathodic phase has to match the amount of electrons drawn from the body in the anodic phase so as to reduce tissue damage as described in chapter one. To do so, there is a need to monitor charges flowing through the electrode during both phases. However, as the biological environment of the implanted electrode is constantly changing, it is difficult to monitor the current through or voltage across the electrode as these values will be fluctuating. Hence, a stable reference is needed to monitor the amount of charges supplied to and drawn out of the electrode.

The key design concept is this: instead of monitoring stimulation conditions at the electrode, current supplied to and drawn from the electrode can be replicated and scaled down to charge or discharge a capacitor. Here, this capacitor acts as a bucket where during the cathodic phase, charges (electrons) are injected into the body and a reduced amount of charges, by a fixed factor, are dumped into the capacitor at the same time. Voltage across the capacitor will begin to rise from an initial value. To achieve charge balance, this voltage has to fall back to its original value. During the anodic phase, charges are drawn from the electrode and charges, reduced by the same fixed factor, are discharged from the capacitor at the same time as well, causing the voltage across it to drop. Therefore, this capacitor acts as the stable reference to

monitor charges in both stimulation phases and the voltage across it determines if enough charges have been drawn out from the body through the electrode and becomes a control signal to end the anodic phase. This concept is similar to that in [27].

4.2 Architecture and functionality

This stimulator version is named the "dual-slope stimulator" because part of its architecture is taken from the dual-slope analog-to-digital converter (ADC). Fig. 4.1 shows a block diagram of this stimulator version.

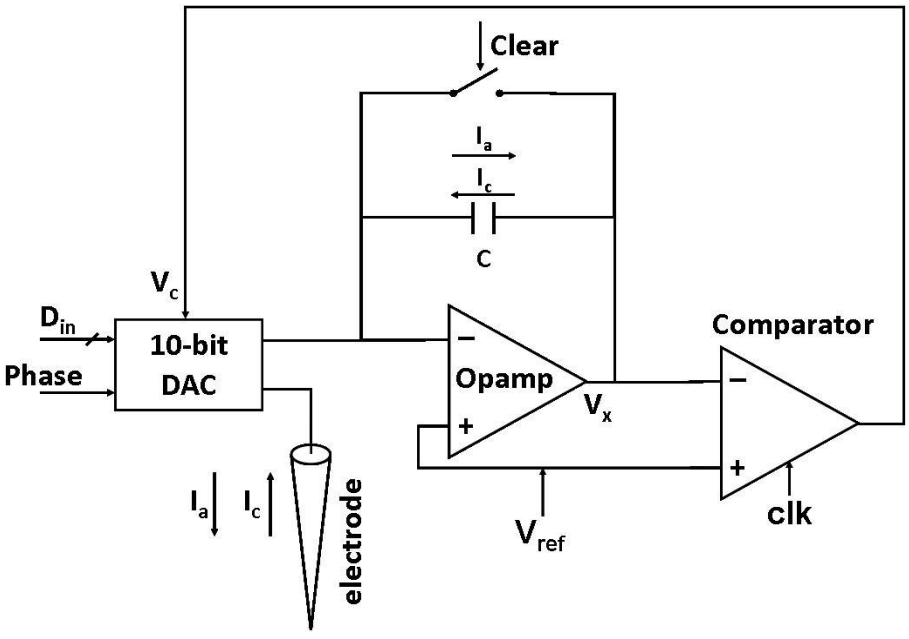

Fig. 4.1 Block diagram of dual-slope stimulator

There are three main circuit blocks in the dual-slope stimulator, namely, a 10-bit DAC, an integrator and a comparator. Details and functionality of the circuit blocks will be described in the following sections.

4.2.1 10-bit DAC

For this stimulator version, there are effectively two 10-bit DACs (as mentioned in chapter three). One DAC has a current output range of 10uA to 10mA and outputs to the electrode. The other DAC is a scaled down version with a current output range of 1nA to 1uA to be connected to the integrator. Current sources of this DAC are operating in weak inversion mode. The outputs of both DACs correspond to the two output terminals from the 10-bit DAC circuit block shown in Fig. 4.1. Biasing of both DACs are done externally. The main reason why a large scaling factor of 10,000 is used is to reduce the capacitor size so that this can be implemented on-chip unlike in [27] where the charging capacitor of 4.7nF has to be placed off-chip.

Since,

$$Q = C\Delta V \Leftrightarrow I = C\frac{dV}{dt}, \tag{4.1}$$

where C: capacitance of the integrator capacitor,

dV: voltage change across the capacitor,

dt: cathodic pulsewidth and

I: cathodic current amplitude to the integrator.

To calculate the maximum capacitance needed, the following values are chosen, dt = 100us (maximum pulsewidth), dV = 0.85V (to prevent voltage saturation at 1.8V supply voltage) and I=1uA (maximum current to the integrator). This set of values will result in a capacitance value of 117.6pF which can still be included on-chip. A smaller scaling factor will result in a larger capacitor needed.

4.2.2 Integrator and comparator

The integrator consists of an opamp with a capacitor connected in negative feedback. It integrates current flowing to or from the capacitor to produce "voltage slopes" at the output node, V_x as seen in Fig. 4.2 below.

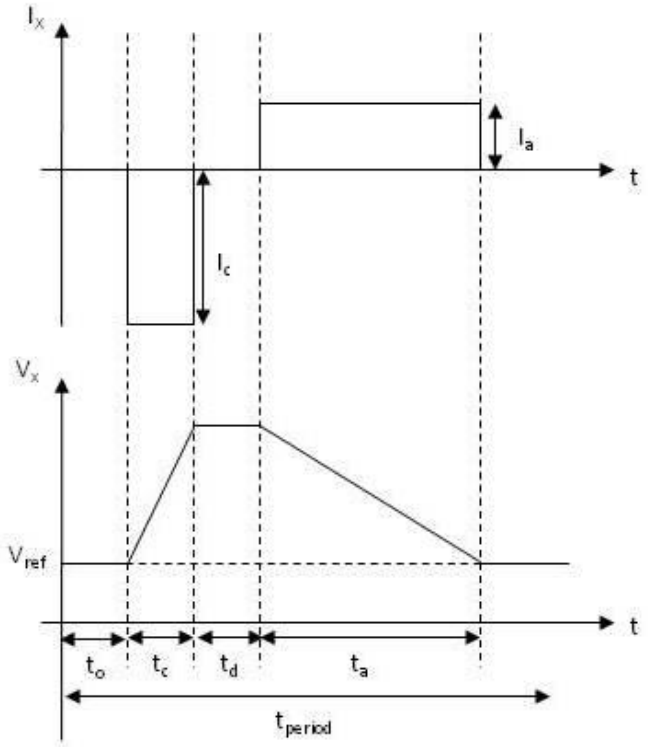

Fig. 4.2 Output current waveform and voltage across the capacitor V_x

For clarity, the variables in Fig. 4.2 are defined as follows,

- I_x: defined as current flowing into the capacitor, C
- I_a : anodic current amplitude
- I_c: cathodic current amplitude
- V_x: defined as voltage at the output of the opamp

- V_{ref}: reference voltage (fixed at half of vdd to have equal voltage headroom for pDAC and nDAC)
- t_o: autozero pulsewidth (to be described later)
- t_c: cathodic pulsewidth
- t_d: interphasic delay
- t_a: anodic pulsewidth
- t_{period}: period of one complete biphasic current waveform

During cathodic phase, current through the capacitor is integrated resulting in a positive slope. V_x rises, remains at a fixed value during interphasic delay and starts to drop during anodic phase. This stable voltage at the output of the integrator helps to monitor charges involved in both phases. The comparator then compares V_x with a reference voltage, V_{ref} and outputs a digital control signal to end the anodic phase, signifying that charge balance is achieved.

4.2.3 Modes of operation

The dual-slope stimulator is controlled using three input signals, *Din*, *Phase* and *Clear*. D_{in} provides the input digital code to the DACs and the time period where this digital code remains more than 0 determines the stimulation pulsewidth for both phases, *Phase* determines whether the nDAC or pDAC outputs current and *Clear* turns on the switch connected across the capacitor to short it so as to ensure that there are no charges stored prior to any stimulation. Another control signal for the DACs,

V_c, is generated from the comparator that turns off the DAC and ends the anodic phase. There are four phases of operation,

- Phase 1 (Autozero): *Clear* is logic '1' and capacitor is shorted before stimulation starts.
- Phase 2 (Cathodic phase): *Phase* and *Clear* are both logic '0'. Electrons are injected through the electrode and into the integrator at the same time. Cathodic current amplitude depends on D_{in}. V_c becomes logic '1' as now V_x is larger than V_{ref}.
- Phase 3 (Interphasic delay): If D_{in} is programmed to be all logic '0's, interphasic delay starts until a new set of D_{in} is input to the DACs to start the anodic phase. Hence, duration of interphasic delay depends on the duration at which D_{in} is all logic '0's.
- Phase 4 (Anodic phase): *Phase* is logic '1' while *Clear* remains logic '0'. A new set of input codes can be set for D_{in} to program the anodic amplitude. V_c remains at logic '1' until V_x falls below V_{ref} and the comparator changes V_c to logic '0' to turn off the DACs.

D_{in} and *Phase* are external input signals that allow programmability of the stimulus amplitude, interphasic delay and even the stimulus profile. Here are some examples,

- Having a larger D_{in} input during the anodic phase results in larger anodic current than cathodic current.
- A anodic-first, cathodic-last stimulus can also be produced by setting *Phase*

to be logic ‘1’ first to output an anodic current and then logic ‘0’ for cathodic current.

- If *Phase* is fixed at either logic ‘0’ or ‘1’, a monophasic stimulus is produced.

To demonstrate how a biphasic waveform can be generated using different combinations of input signals, Fig. 4.3 compares the output waveform with the required input signals, *Vin*, *Phase* and *Clear*.

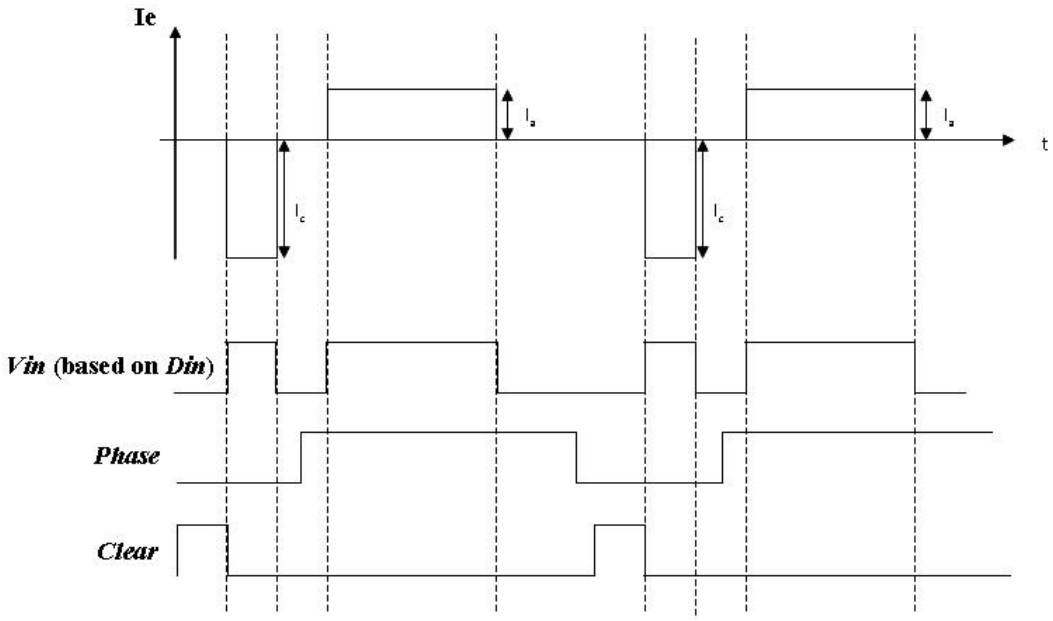

Fig. 4.3 Output waveform versus input signals

Using the above combination of input signals, a biphasic waveform can be generated. Amplitude is programmed via *Din*, and pulsewidth is determined by the time period where *Vin* is logic ‘1’ (at least one of the 10-bits of *Din* must be logic ‘1’ to produce a output current). Frequency of stimulation depends on the frequency of this combination of input signals as shown.

In summary, the dual-slope stimulator not only allows standard stimulation parameters like amplitude, frequency and pulsewidth, different stimulus profiles can also be achieved as well through different combinations of input signals.

4.3 Circuit blocks of the dual-slope stimulator

Implementing the dual-slope stimulator involves the design of the DACs (covered in chapter three), the integrator and the comparator. Details on the schematic and specifications of the integrator and comparator are given in the following sections.

4.3.1 Integrator design

The integrator consists of an opamp, a capacitor and a switch. Schematic of the opamp, with transistors sizing, is shown in Fig. 4.4.

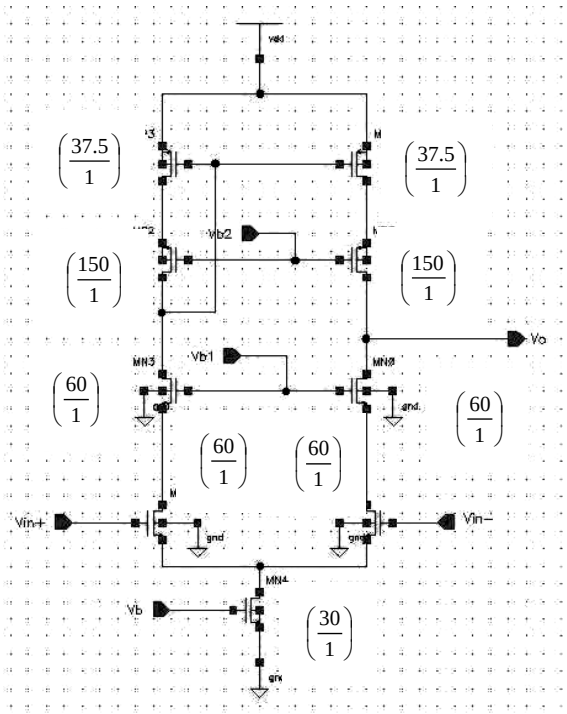

Fig. 4.4 Schematic of opamp

Telescopic architecture is chosen for stability and high gain. Simulation is done on the telescopic opamp and the bode plots are shown in Fig. 4.5.

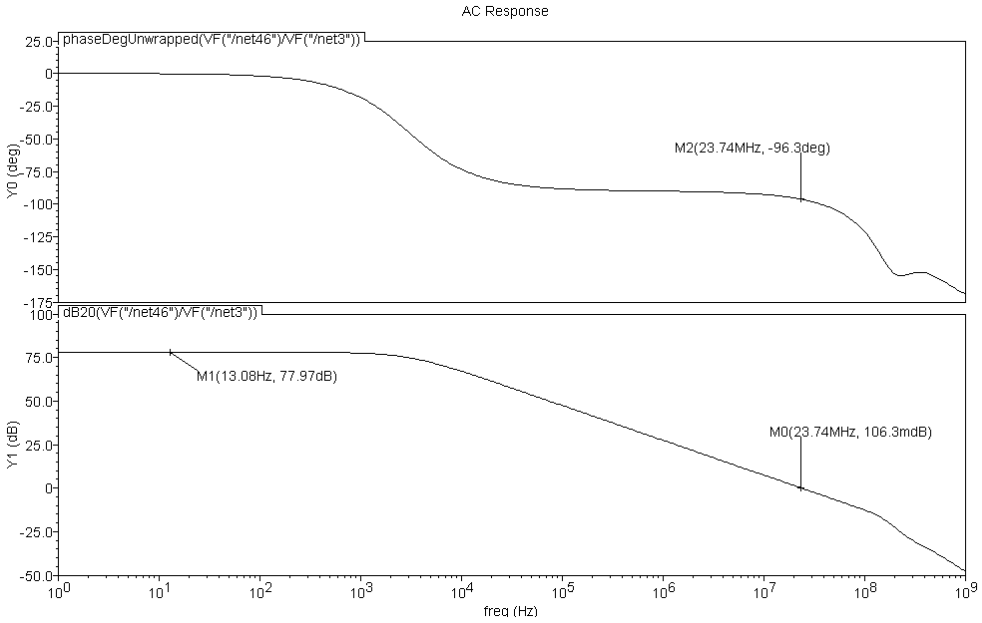

Fig. 4.5 Bode plots of the telescopic opamp

Based on the bode plots, the DC gain of the opamp is 77.97dB with a phase margin of 83 degrees. Total current consumption of the opamp is 30uA. Layout of the opamp is shown in Fig. 4.6.

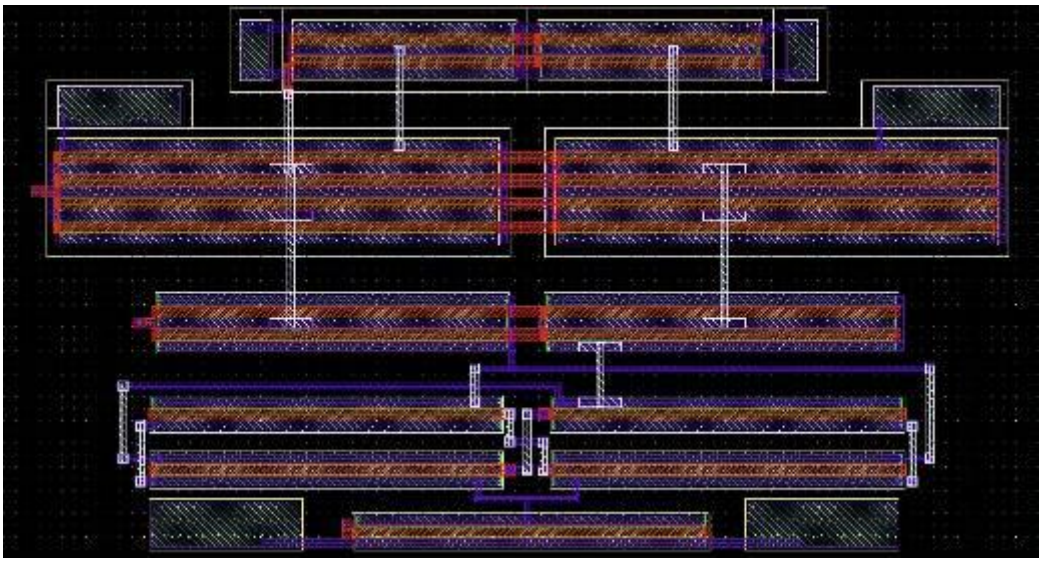

Fig. 4.6 Layout of telescopic opamp

Symmetric approach is used when drawing the layout of the opamp. Post-layout simulations show similar results as shown in Fig. 4.5.

4.3.2 Comparator design

There are two main types of comparators, namely the continuous-time comparator and latched comparator. In this application, speed is crucial because the comparator has to turn off the DAC very quickly once the voltage across the capacitor, V_x crosses below Vref. If the comparator is slow, it may lead to charge imbalance as there will be more charges in the anodic phase than the cathodic phase. Therefore, a latched comparator is used for this project. Schematic of the comparator is shown in Fig. 4.7.

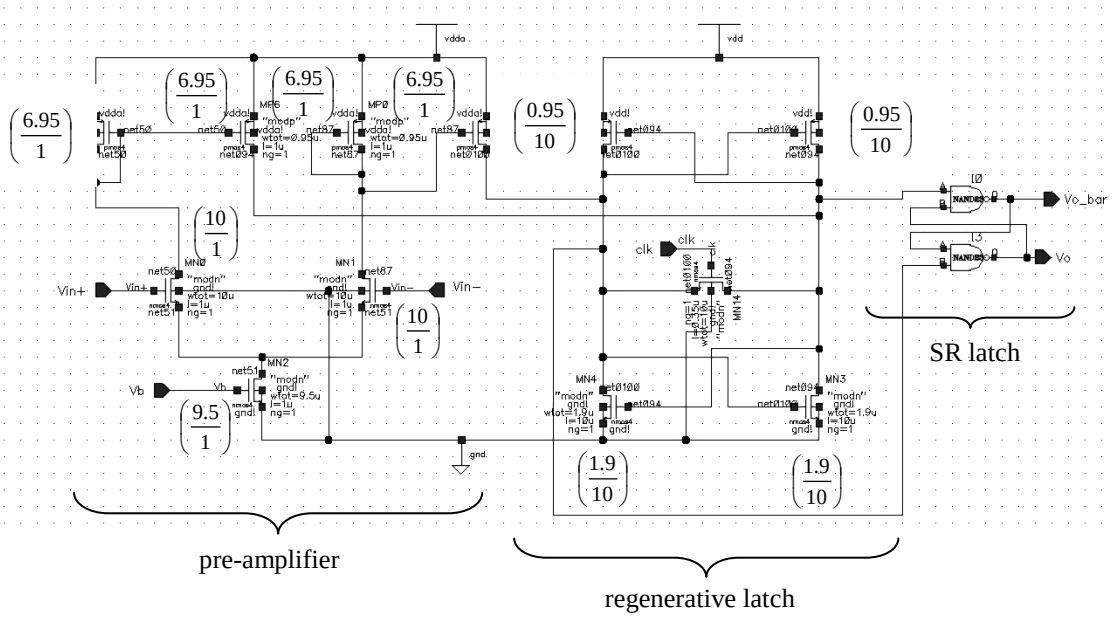

Fig. 4.7 Schematic of latched comparator

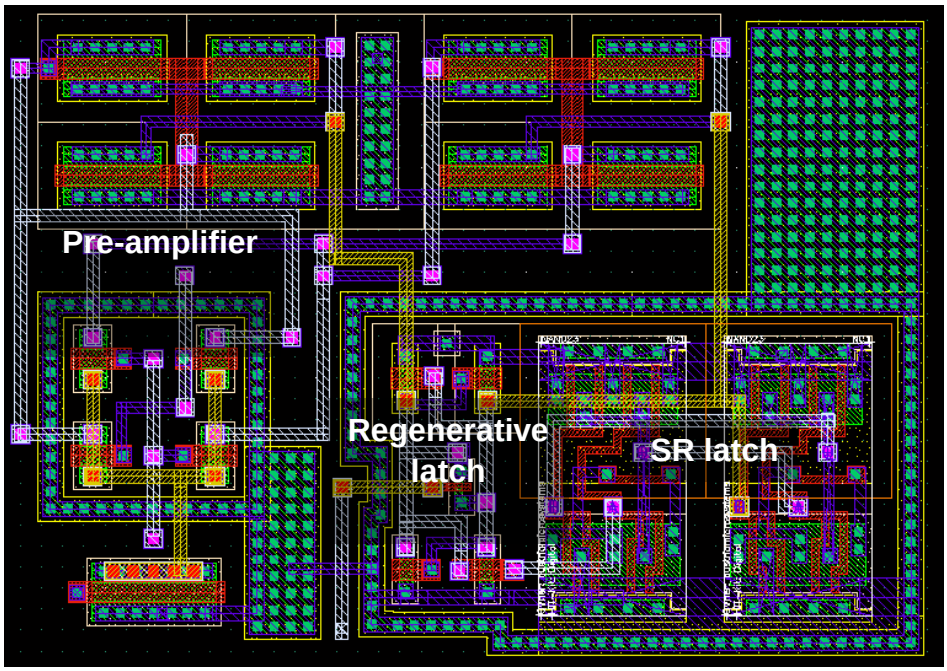

Fig. 4.8 Layout of comparator

Besides using common centroid configuration for input transistors of the pre-amplifier and mirroring transistors, the digital components of the comparator, i.e the regenerative latch and SR latch, are also separated from the pre-amplifier. Digital and analog supplies and ground terminals are separated as well.

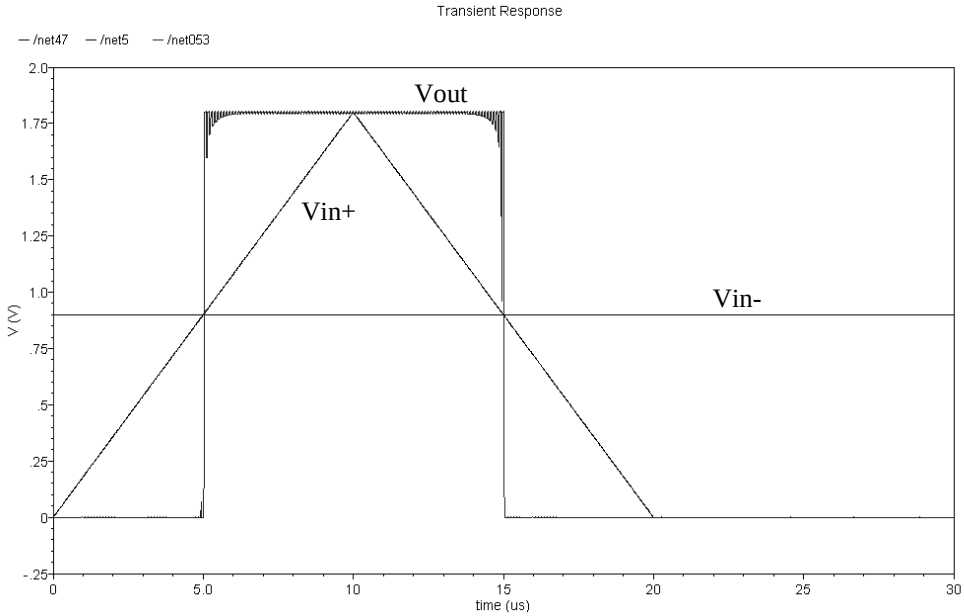

Fig. 4.9 Post-layout simulation of comparator

Post-layout simulation is done using an upward ramp followed by a downward ramp to simulate the "dual-slope" of the voltage across the capacitor, $V_{x,}$ so as to observe the switching speed of the comparator. It can be seen from Fig. 4.9 that the switching delay is in nanoseconds range. Clock frequency for the latch is 1MHz. Schematic simulation results are omitted because post-layout simulation gives similar results as schematic simulation results.

4.4 Layout and post-layout simulation

The various circuit blocks are connected according to Fig. 4.1. Layout of the dual-slope stimulator (excluding DAC) is shown in Fig. 4.10. Post-layout simulation is done at different stimulation current levels and pulsewidths.

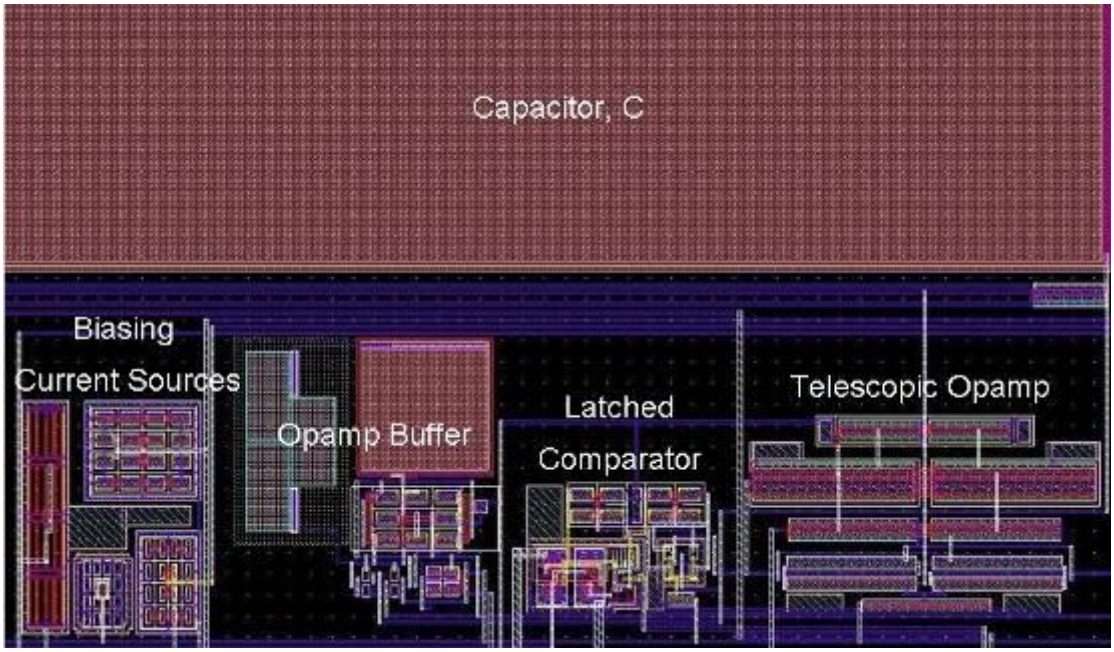

Fig. 4.10 Layout of dual-slope stimulator (excluding DAC)

Fig. 4.10 also shows the biasing current sources for the DAC and an opamp buffer to drive an external pad that allows V_x to be measured externally after fabrication.

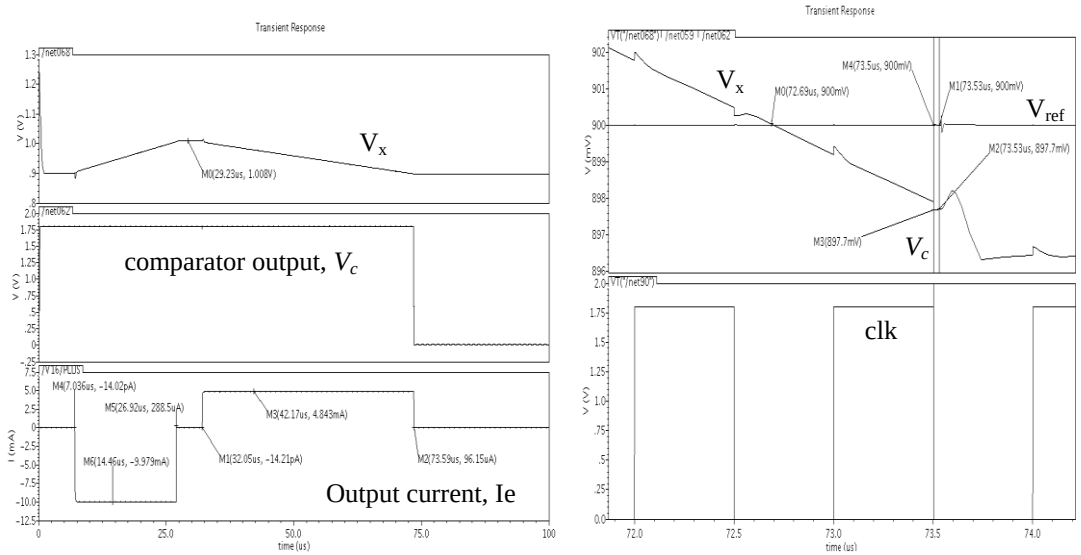

Fig. 4.11 Post-layout simulation result for dual-slope stimulator

The left plot gives the output current waveform of the stimulator. The output current waveform is a rectangular biphasic stimulus with a 9.979mA-20us cathodic phase and 4.843mA-41.59us anodic phase. The 'dual-slope' voltage, V_x along with the comparator output, V_c, are plotted together with the output current. The right plot gives an enlarged view of V_x, V_{ref} and the comparator output, V_c. It can be seen that there is a delay of 0.84us from the crossover point where V_x falls below V_{ref} to the crossover point of V_c below V_{ref}. In order words, the comparator switches off the DAC 0.84us after V_x crosses below V_{ref}. To calculate charge balance mismatch, the equation below is used.

$$Q = I \times t\,, \tag{4.2}$$

where Q = charge, I = current and t = pulsewidth.

Charge balance mismatch is calculated using,

$$charge\,balance\ mismatch = \left| \frac{cathodic\ charge - anodic\ charge}{cathodic\ charge} \right| \times 100\% \tag{4.3}$$

Based on Eqn. (4.2), cathodic charge is 199.58nC and anodic charge is 201.42nC. Hence, the excess charge is 1.84nC. Using Eqn. (4.3), the charge balance mismatch is 0.922%. Another important thing to note is that the comparator delay depends on the crossover time period. In Fig. 4.10, V_x falls below V_{ref} at the latch phase of the regenerative comparator. Therefore, it was until the next latch phase when *Vc* starts to change causing the total delay to be 0.84us. The actual comparator delay is only 30ns.

Table 4.1 summarizes the performance of the dual-slope stimulator for different pulsewidths and amplitudes based on post-layout simulations.

Cathodic amplitude (A)	**Anodic amplitude (A)**	**Cathodic pulsewidth (us)**	**Anodic pulsewidth (us)**	**Charge mismatch (C)**	**Charge balance mismatch (%)**
9.979m	4.834m	20	41.59	1.84n	0.922
2.488m	1.22m	20	42.59	2.19n	4.42
616.3u	303.3u	30	80.48	5.92n	32
150.3u	70.1u	85.21	192.62	696p	5.44

Table 4.1 Performance of dual-slope stimulator

Although it may seem that the charge balance mismatch percentage for the last row of data is very high, at 32%, the excess charge is only 5.92nC. This is still way below the safety tolerance level of 0.4uC/mm^2/stimulus pulse [25]. Also, the reason for such a high percentage of charge mismatch can be attributed to two factors. First of all, based on Eqn. (4.2), percentage mismatch is calculated with reference to the cathodic charge. Therefore if the cathodic charge is high, percentage mismatch will be lower for a given magnitude of charge mismatch. In other words, for a fixed value for the numerator (i.e |cathodic charge – anodic charge|), if the denominator (i.e. cathodic charge) becomes larger, charge balance mismatch percentage will be smaller. The second factor can be reflected from Fig. 4.12 below.

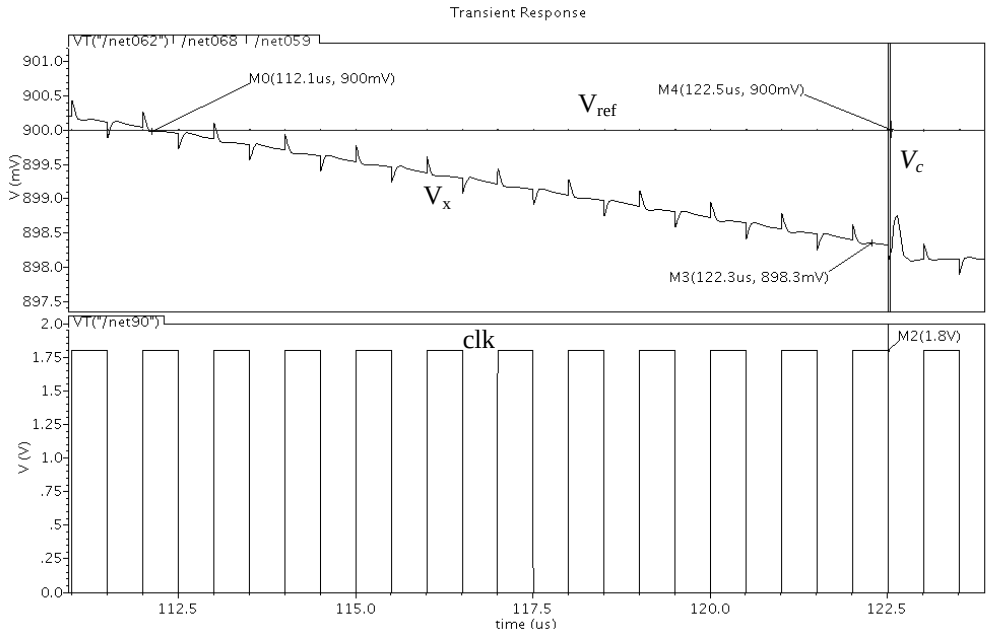

Fig. 4.12 Enlarged view of the crossover point for 616.3uA-30us stimulus

Fig. 4.12 shows the enlarged view of the crossover point for the third set of post-layout simulation results in Table 4.1. V_x falls below V_{ref} at 112.1us but it was until 122.5us then V_c changes from logic '1' to logic '0' to end the anodic phase. Referring to the clk waveform, it takes quite a number of clock cycles before the comparator can detect V_x is below V_{ref} and give the correct output. This is largely due to the offset of the comparator. With a small anodic current, the downward slope becomes gentler. Hence the voltage change over time becomes smaller (V_x only drops 1.7mV in 10us). Hence, it takes a longer time for V_x to fall to a certain value (the input offset value of the comparator) below V_{ref} before the comparator can output a change in logic. This leads to a large delay and hence, a large mismatch.

In summary, the dual-slope stimulator is indeed able to produce biphasic waveforms of different current amplitudes and pulsewidths. In fact, the dual-slope stimulator offers full programmability including amplitudes for both cathodic and anodic phases, interphasic delay and even the stimulus profile. This level of programmability is not available in any of the stimulators presented in chapter two. Charge balance achieved is also within the safety tolerance given in [25]. Based on the post-layout simulations, factors resulting in charge balance inaccuracies for the dual-slope stimulator are listed below.

- Comparator input offset and delay affects the time needed for the comparator to react once V_x falls below V_{ref} causing larger than desired anodic pulsewidth,
- Crossover point of V_x. Worst case is when V_x crosses V_{ref}, at the beginning of the latch phase of the comparator. Hence, it will take at least another clock period for the comparator to react. This means the worst case delay due to this factor will be 1us,
- Integrator offset and its finite transconductance introduces inaccuracies in the 'dual slope' voltage profile of V_x. Since control of the anodic phase is based on V_x, inaccuracies in V_x profile introduces error in charge balance,
- V_x profile, where a gentle downward slope for V_x make require a longer time for the comparator to detect that V_x is below V_{ref} and give a correct output (as reflected in Fig. 4.10),
- Matching inaccuracies between the DAC and the scaled down DAC also affects charge balance accuracy. This is because the scaled down DAC is

supposed to be a replicate to emulate the current delivered to the electrode. Hence, if the scaled down DAC is unable to correctly reflect the current ratios (ratio between cathodic current and anodic current) at the electrode, charge balance inaccuracies will occur.

CHAPTER FIVE: DIGITAL STIMULATOR

5.1 Design concept

Although the dual-slope stimulator is able to produce rectangular biphasic stimulus of programmable pulsewidth, amplitude and frequency, synchronized square-wave inputs are required (as shown in Fig. 4.3). As described in chapter one, if information on stimulation parameters are received wirelessly from the neural recording circuitry, such data will be in digital bits. Requiring synchronized square-wave inputs will add complexity to the entire FES system. In chapter two, most stimulators reviewed also make use of registers to store information on stimulation parameters. Hence, there is motivation to use digital bits to program stimulation parameters. Besides complexity in required input signals, most of the factors attributing to charge balance inaccuracies are due to analog circuitry (i.e integrator and comparator) of the dual-slope stimulator. If digital logic is used instead, issues like input offset, crossover point and finite transconductance will be eliminated. More importantly, only one DAC will be required if digital logic is used. This will be explained later. With the issues of the dual-slope stimulator, the digital stimulator is proposed, aiming to produce biphasic stimulus with better charge balance accuracy.

The main idea behind the operation of the digital stimulator is to make use of counters to program stimulation pulsewidth. Current amplitude is still controlled by the DAC. Since there are three phases in a biphasic stimulus, namely cathodic phase, anodic

phase and interphasic delay, separate counter can be used to keep track of each phase. Frequency of stimulation can be controlled via a clock signal that resets the counters. For simplicity, anodic current is fixed at half the cathodic current. This means that anodic pulsewidth has to be twice the cathodic pulsewidth and this can be easily implemented using digital flip-flops. Based on this idea, an overview of the digital stimulator is presented in Fig. 5.1.

5.2 Architecture and functionality

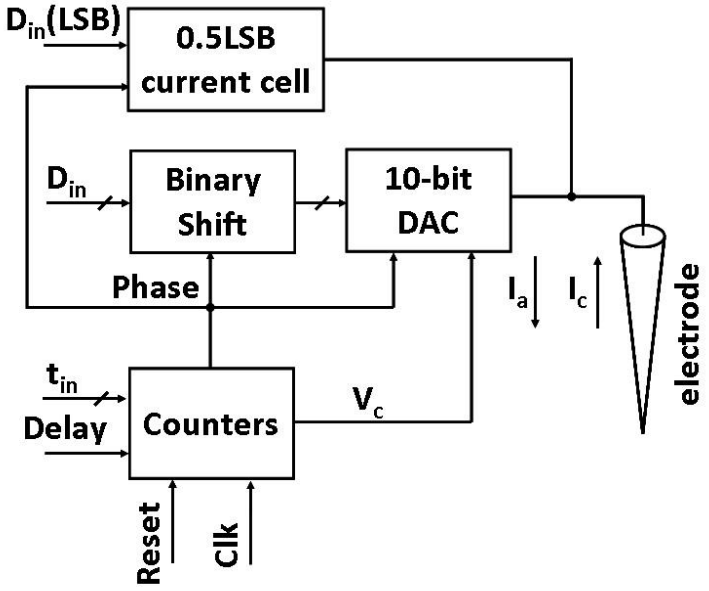

Fig. 5.1 Block diagram of the digital stimulator

The digital stimulator consists of these circuit blocks, a 10-bit DAC, a 0.5LSB current cell, a binary shift circuit and counters. Details and functionality of each circuit blocks will be described in the following sections.

5.2.1 10-bit DAC

This is the same 10-bit DAC used in the dual-slope stimulator to provide different current levels. For the digital stimulator, the scaled-down DAC is not used since there is no need to use a stable reference to monitor charges at the electrode in this version. Stimulation parameters are all controlled using digital logic.

5.2.2 Binary shift circuit

A ratio of 0.5 has been fixed between anodic current amplitude and cathodic current amplitude. The main reason why a ratio of 0.5 is used is that division by two can be simply achieved by shifting all 10 bits of *Din* to the right (towards the LSB) and replace the MSB of *Din* by a logic '0' to perform a division by two. By shifting *Din* only during the anodic phase, *Din* does not have to change throughout stimulation, unless new current amplitude is needed. This is unlike the dual-slope stimulator whereby *Din* has to be constantly changing to program pulsewidths and amplitude for both anodic and cathodic phases. This idea of having a fixed ratio for cathodic and anodic amplitudes is not new as this can be seen in most stimulators reviewed in chapter two as well. Binary shift circuits can be implemented using flip-flops but in this case, a simpler architecture is used.

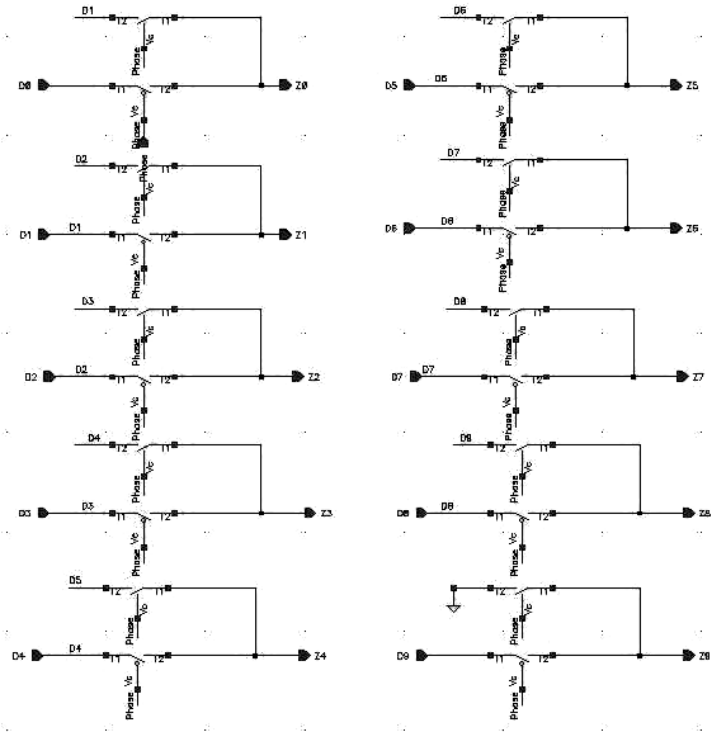

Fig. 5.2 Schematic of binary shift circuit

Transmission gates (half of which are active high while the others are active low) are use to shift *Din* by 1-bit towards the LSB to perform a division by two. There are two input signals to this circuit, namely *Din* and *Phase*. The switches are controlled by *Phase* and the outputs of this circuit are connected to the inputs of the DAC. When *Phase* is logic '0' (i.e cathodic phase), active low switches are on and there is no change to *Din*. However, during the anodic phase (*Phase* is logic '1'), active high switches are on and the outputs of this binary shift circuit are such that the *n*th bit input is connected to the *(n-1)*th bit output and the MSB of *Din* is replaced by logic '0'. In other words, during the anodic phase, the 3rd bit of *Din* will be connected to the 2nd input bit of the DAC and so on.

5.2.3 Counters

This circuit block consists of three counters, namely cathodic counter, anodic counter and interphasic counter. Each counts the time period for each phase. A block diagram showing how all three counters are connected to each other is shown in Fig. 5.3.

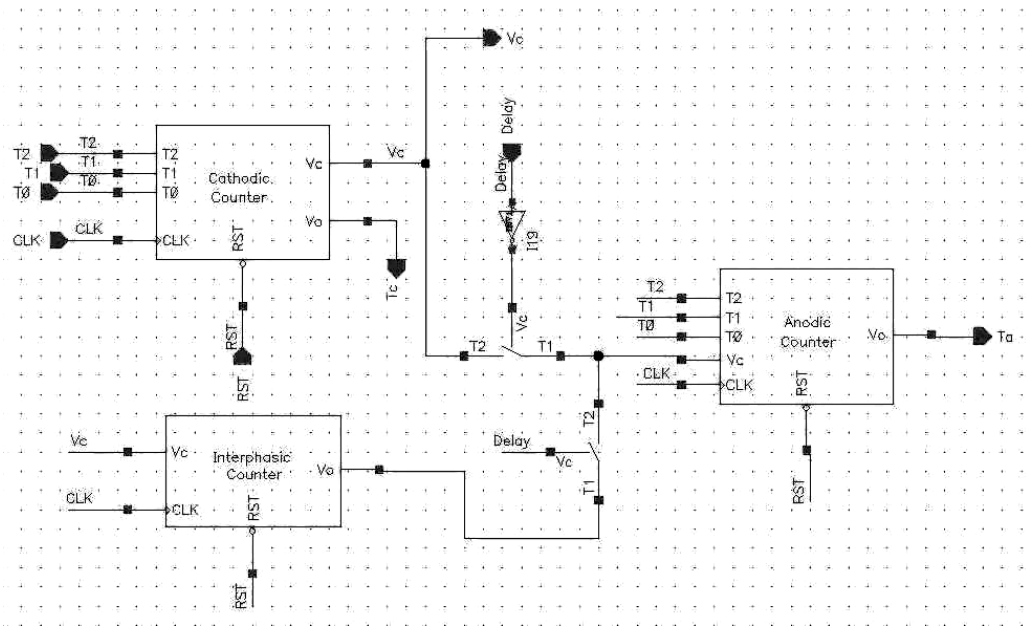

Fig. 5.3 Block diagram of counters

The basic idea behind the operation of these counters is that upon stimulation, cathodic counter will start counting first. Once this counter starts counting, *Vc* becomes logic '1'. This signal is used to control the DAC as well. During this period of time, cathodic current is output to the electrode. Once the cathodic counter finishes counting all its states, *Vc* goes to logic '0' and this triggers the next counter. If *Delay* is logic '1', *Vc* triggers the start of the interphasic counter to initiate interphasic delay. Once the interphasic counter finishes counter all its states, a similar control signal from the interphasic counter will trigger the anodic counter to start counting, thereby

starting the anodic phase. If *Delay* is logic ‘0’, anodic counter will be triggered immediately after cathodic counter ends, bypassing the interphasic counter. *Phase* signal is generated from the cathodic counter such that *Phase* is logic ‘0’ initially until the cathodic counter finishes counting and *Phase* goes to logic ‘1’ for anodic phase.

Fig. 5.4 to 5.6 shows the schematic of the cathodic counter, anodic counter and the interphasic counter. All counters are implemented using standard counter architecture. However, modifications are done to make these counters programmable.

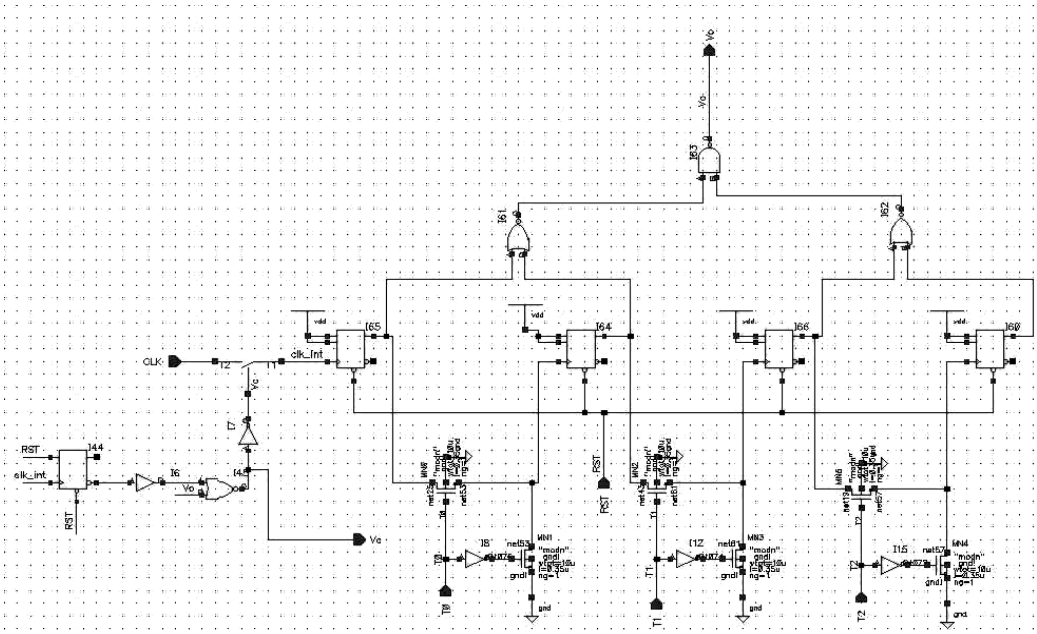

Fig. 5.4 Schematic of cathodic counter

The cathodic counter is a programmable counter that counts over variable time periods based on a 3-bit input t_{in}. Basically, t_{in} controls the switches that connect additional flip-flops to the overall counter to increase the counter resolution. A single flip-flop counter counts from 0 to 1. By adding another flip-flop to the counter, the

resolution is increased and it will count from 00 to 11. Table 5.1 shows different t_{in} input along with the time period that the cathodic counter counts and the corresponding counter states based on 100kHz *Clk* input. Logic gates are used at the outputs of the flip-flops such that once these outputs are all logic '1's, the output of these logic gates, *Vc*, disconnects the input clock signal, *Clk* to stop the counter. *Vc* is also used to trigger the start of the next counter.

t_{in}			**Counter period**	**Counter states**
$t_{in,2}$ (MSB)	$t_{in,1}$	$t_{in,0}$ (LSB)		
0	0	0	10us	0 to 1
0	0	1	30us	00 to 11
0	1	1	70us	000 to 111
1	1	1	150us	0000 to 1111

Table 5.1 Counter period based on different t_{in} input

Here, the counter period determines the cathodic pulsewidth for stimulation. *Clk* input determines the counter period. In short, irregardless of the frequency of *Clk* input, the cathodic counter is able to provide four different cathodic pulsewidths: 1 *Clk* period, 3 times *Clk* period, 7 times *Clk* period and 15 times *Clk* period.

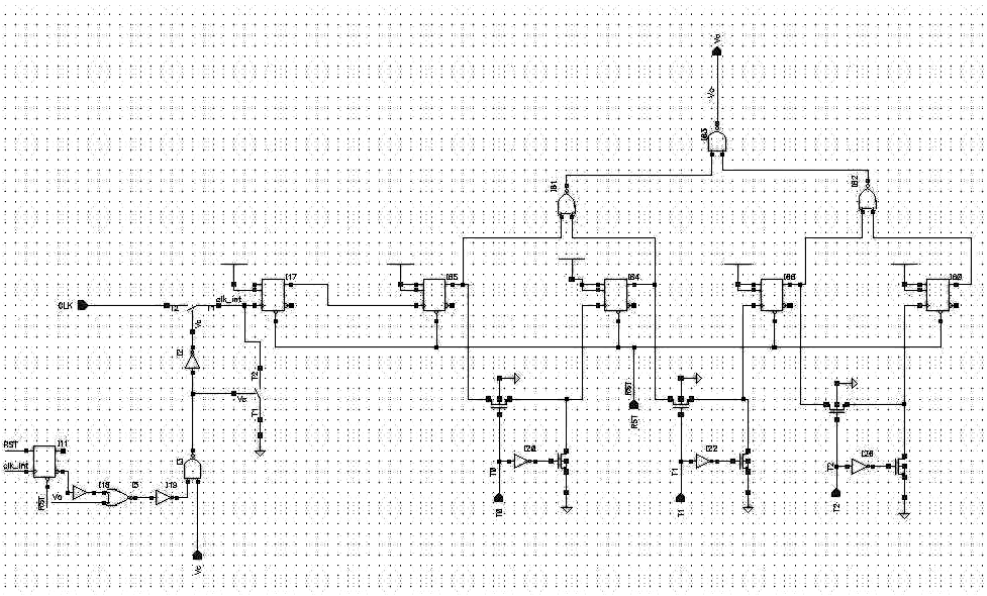

Fig. 5.5 Schematic of anodic counter

Architecture of the anodic counter is similar to the cathodic counter. In order to generate pulsewidths twice the cathodic pulsewidths, the *Clk* input passes through an additional flip-flop such that the clock input to the anodic counter is twice the period of *Clk*. Besides this, the anodic counter operates exactly like the cathodic counter.

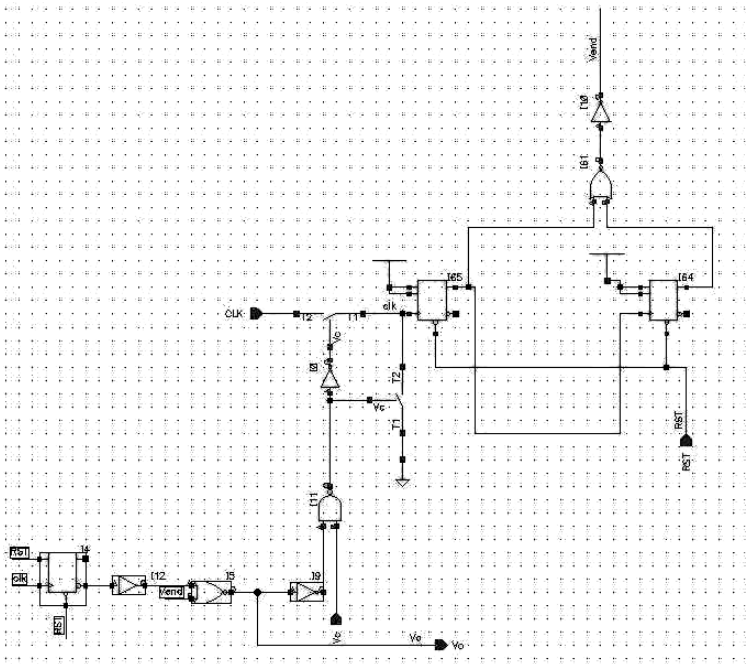

Fig. 5.6 Schematic of interphasic counter

The interphasic counter is a non-programmable counter unlike the anodic and cathodic counters. Interphasic pulsewidth is fixed at 30us (based on 100kHz *Clk* input). This interphasic delay duration is chosen arbitrary because it is mentioned in chapter one that any delay greater than 80us will results in monophasic effects. In addition, because there is no theory on the significance of the interphasic delay, programmability for interphasic delay may not be necessary.

5.2.4 0.5LSB current cell

The main function of the 0.5LSB current cell is to compensate the loss of current amplitude during the anodic phase when *Din* is an odd value. For example, if the decimal equivalent of *Din* equals 5, a binary shift of *Din* results in a decimal equivalent of 2. Therefore, this block is only used when the LSB of *Din* is logic '1' (when the decimal equivalent of *Din* is odd) and during the anodic phase. 0.5LSB current cell gives an anodic output current of 5uA and is implemented by a pMOS current mirror with half the transistors sizing shown in Fig. 3.2.

5.3 Layout and post-layout simulation

The digital stimulator is implemented in Cadence and schematic simulations are done to verify its functionality. After which, layout is drawn and post-layout simulations are carried out. Schematic simulations results are omitted since post-layout stimulations give similar results. In addition, post-layout simulations give better estimates to the actual circuit performance after fabrication.

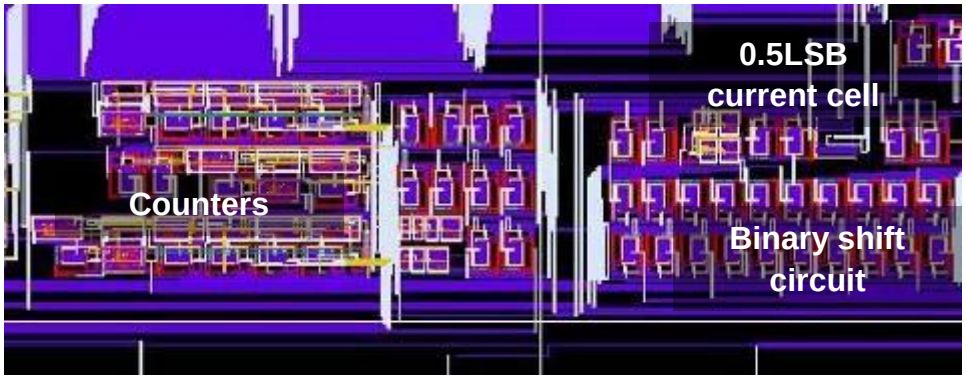

Fig. 5.7 Layout of digital stimulator excluding DAC

Fig. 5.7 shows the layout of the digital stimulator excluding the DAC. Post-layout simulations are done based on different *Din* and t_{in} inputs for different stimulus amplitudes and pulsewidths. Fig. 5.8 shows a 2.5mA-10us cathodic phase output waveform of the digital stimulator.

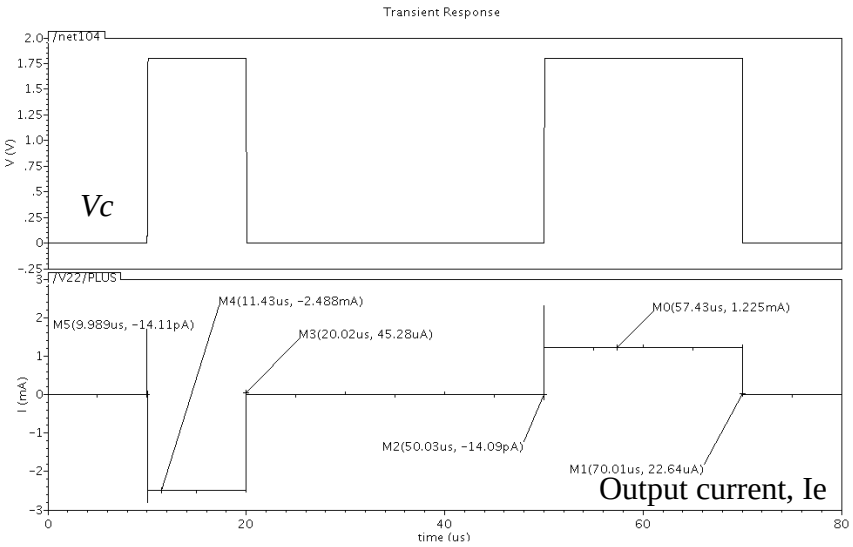

Fig. 5.8 Output waveforms of the digital stimulator

As mentioned before, *Vc* is a control signal generated by the counters to control the DAC. To be exact, *Vc* is generated from the cathodic counter during cathodic phase and from the anodic counter during the anodic phase. It can be seen from Fig. 5.8 that

there is current output only when *Vc* is logic '1'. An interphasic delay of 30us can also be observed. Table 5.2 summarizes the performance of the digital stimulator.

Cathodic amplitude (A)	**Anodic amplitude (A)**	**Cathodic pulsewidth (us)**	**Anodic pulsewidth (us)**	**Charge mismatch (C)**	**Charge balance mismatch (%)**	**Current Ratio**
146.7u	73.32u	30	60	1.8p	0.041	0.499
616.3u	308.1u	30	60	3p	0.016	0.499
2.488m	1.225m	10	20	380p	1.53	0.492
9.979m	4.848m	10	20	2.83n	2.84	0.449

Table 5.2 Performance of the digital stimulator

Results from Table 5.2 shows that the digital stimulator is able to achieved excellent charge balance accuracies of below 5%. In addition, the absolute charge mismatch is in pC to nC range which is much lower than the safety tolerance level of 0.4uC/mm^2/stimulus pulse [25]. Unlike the dual-slope stimulator, there is only one factor affecting the charge balance mismatch for the digital stimulator, i.e. the mismatch between the pDAC current and nDAC current. If the ratio of the anodic current is exactly half of the cathodic current, charge balance accuracy will be 100% since the pulsewidths are accurately controlled by the counters. However this is not the case as seen from the results in Table 5.2. Mismatch of the pDAC and nDAC can be due to difference in their output impedance and linearity.

CHAPTER SIX: MEASUREMENT RESULTS AND DISCUSSION

6.1 Overall layout and pins allocation

Both the dual-slope stimulator and the digital stimulator are incorporated into a single chip for fabrication. Hence, this single stimulator chip offers two versions of stimulators. Fig. 6.1 shows the overall layout of the stimulator chip and Fig. 6.2 shows a micrograph of the fabricated chip.

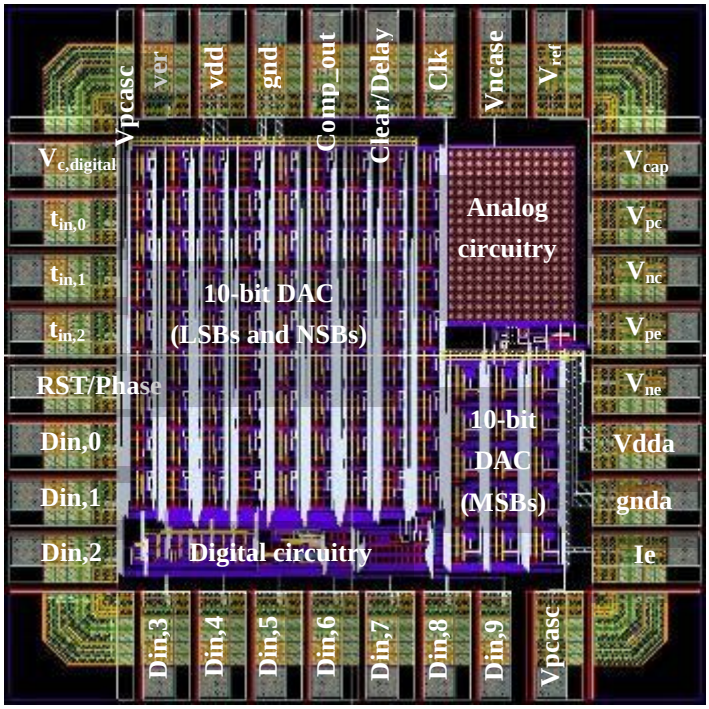

Fig.6.1 Overall layout and micrograph of the proposed stimulator

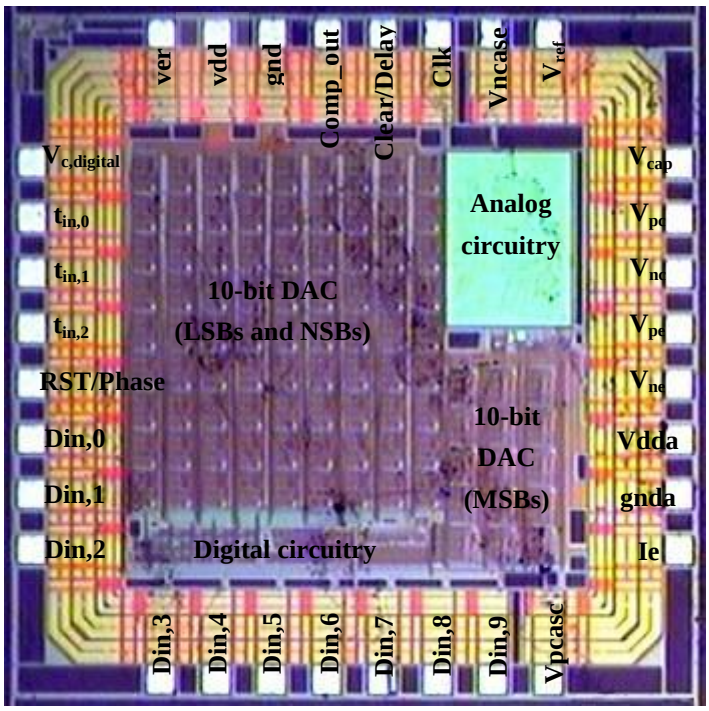

Fig. 6.2 Micrograph of the fabricated chip

Size of the overall layout including the pad frame is 2.1752mm by 2.1752mm. There are a total of 32 pins, 11 of which are analog I/O pins and 21 are digital I/O pins. To reduce the total number of pins needed, some of these input pins serve two functions for different stimulator versions. There are breaks in spacers to separate digital I/O pins analog I/O pins. Digital supplies and analog supplies are separated as well to prevent noise from noisy digital lines to be coupled into analog circuitry. Also, layout of the DAC is arranged in such a way to separate the analog circuits of the dual-slope stimulator from the digital circuits of the digital stimulator for this same reason. Table 6.1 gives description of each I/O pin of the proposed stimulator as labeled in Fig. 6.1 and Fig. 6.2.

Pin name	Remarks
Vc,digital	To observe *Vc* signal from the counters
$t_{in,0}$ to $t_{in,2}$	3-bit input for t_{in}
RST/Phase	This serves as *Reset* input for the digital stimulator and *Phase* input for dual-slope stimulator
Din,0 to Din,9	10-bit input for *Din*
Vpcasc	Input cascode voltage for pDAC
Ie	Current output terminal of the DAC to be connected to electrode
gnda	Analog ground terminal
Vdda	Analog vdd terminal
Vne	Pin to connect to external variable resistor to bias nDAC
Vpe	Pin to connect to external variable resistor to bias pDAC
Vnc	Pin to connect to external variable resistor to bias scaled-down nDAC
Vpc	Pin to connect to external variable resistor to bias scaled-down pDAC
Vcap	Output pin to monitor voltage across capacitor, V_x
Vref	Reference voltage for stimulation (half Vdd)
Vncasc	Input cascode voltage for nDAC
Clk	Clock input for counter if digital stimulator is chosen or for comparator if dual-slope stimulator is chosen
Clear/Delay	This serves as *Delay* input for the digital stimulator and *Clear* input for dual-slope stimulator
Comp_out	Output pin to monitor comparator output for the dual-slope stimulator
gnd	Digital ground terminal
vdd	Digital vdd terminal
ver	Input to determine which version of stimulator is active. Logic ‘0’: dual-slope stimulator chosen Logic ‘1’: digital stimulator chosen

Table 6.1 Pins allocation for the proposed stimulator

6.2 Measurement results

In order to test the fabricated chip, a PCB is designed to provide interface between the chip and the measurement equipment. In order to measure current output of the stimulator, an off-chip opamp with variable resistor feedback is connected to the current output terminal of the stimulator chip. Fig. 6.3 shows the configuration to measure output current.

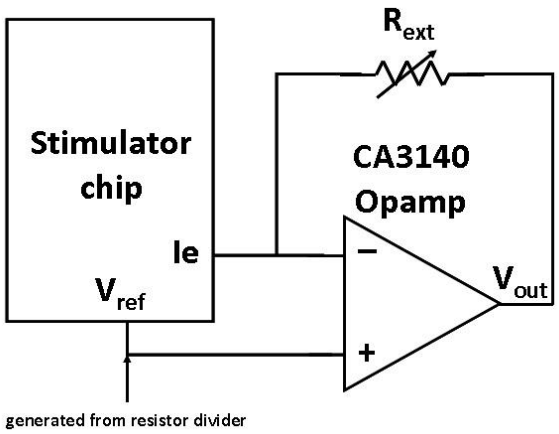

Fig. 6.3 Setup to measure stimulator output current

R_{ext} is an variable resistor that acts as the load of the stimulator. When there is no current output, V_{out} equals V_{ref} by virtue of negative feedback. During cathodic phase, current flows into the stimulator chip causing V_{out} to rise and the opposite occurs during anodic phase. V_{out} is measured using an oscilloscope and current amplitude is calculated by dividing the change in V_{out} with the resistance value of R_{ext}. CA3140 opamp is a MOS-input opamp with bipolar output stage. This is chosen because of its low input biasing current and high output current capability. V_{ref} is a voltage generated via an external resistor ladder and it is fixed at half the supply voltage.

6.2.1 DAC characterization

DAC characterization is done first by making use of the dual-slope stimulator and fixing the *Phase* input. *Phase* is fixed at logic '0' for nDAC characterization and logic '1' for pDAC characterization. Characterization is not done for the scaled-down DAC because it is not possible to measure current in the range of nano-amperes with existing test equipment. In order to do a full-scale measurement for the DAC, the pattern generator function of a logic analyzer is used to generate all the digital codes for the 10-bit input, *Din*.

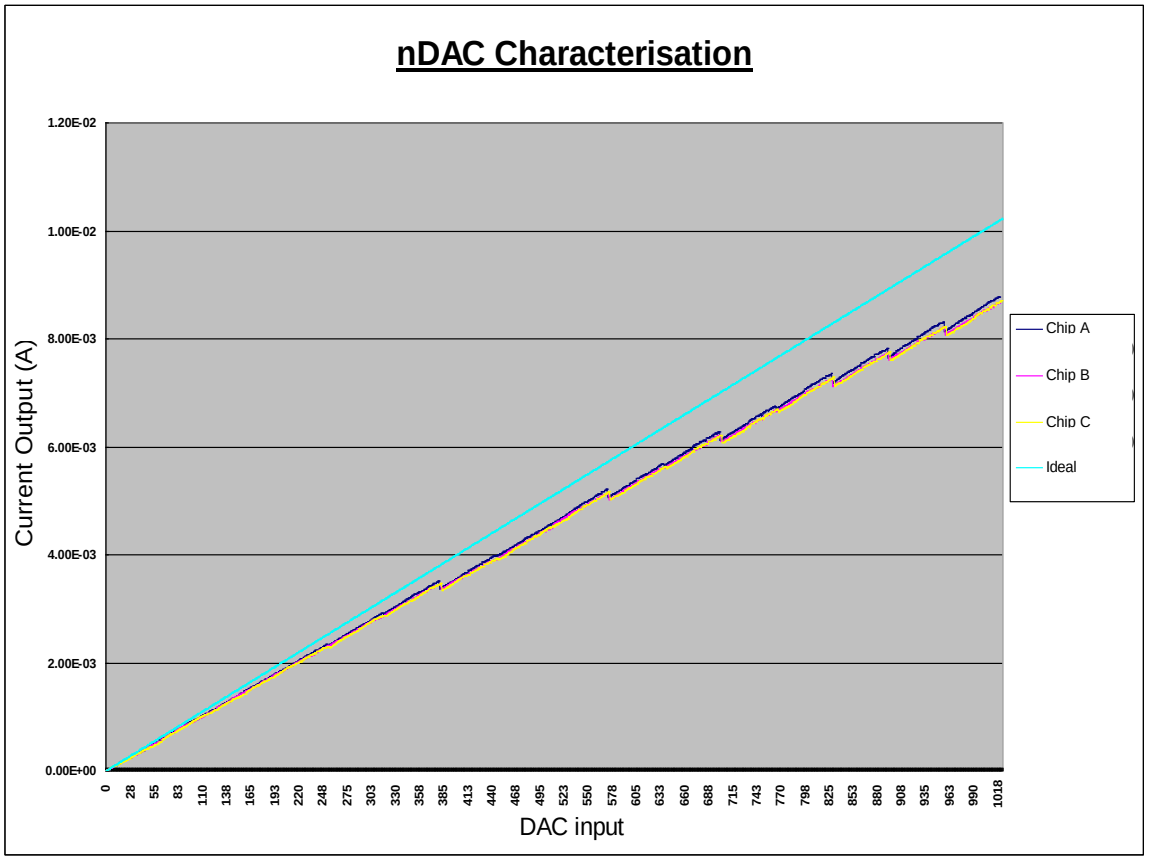

Fig. 6.4 Full-scale characterization of the nDAC

Fig. 6.4 shows the characterization of the nDAC for three separate chips (Chip A, B and C) and the value of R_{ext} used is also given. It can be seen that all three chips have similar performance and the DAC characteristics deviates more from the ideal line as the DAC input increases. Fig. 6.5 shows the percentage deviation from the ideal current output for all inputs.

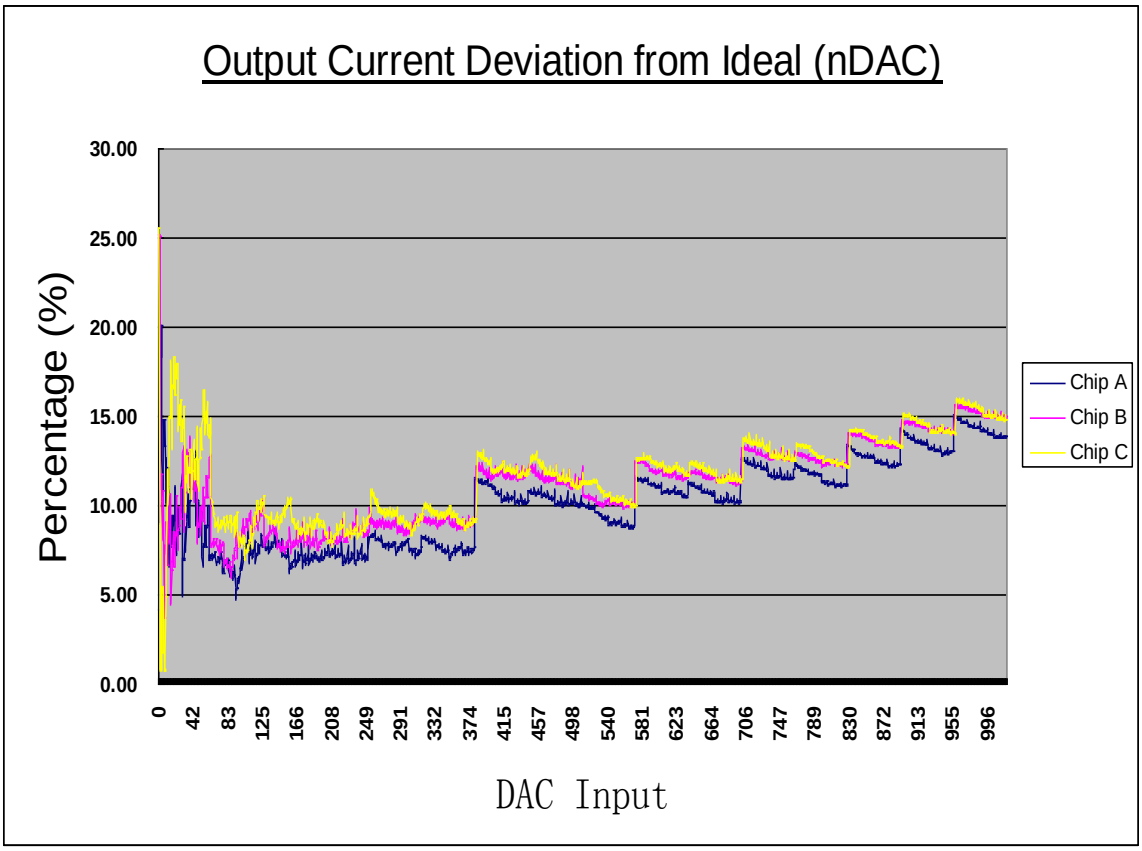

Fig. 6.5 Output current deviation from ideal values for nDAC

From Fig. 6.5, percentage deviation of the output current from the ideal values range between 5-20%. This can be attributed to the mismatch in the LSB current cell and MSB current cell. Measurements show that the MSB current cell outputs a current of 590uA instead of 640uA and the LSB cell outputs a current of 8.2uA instead of 10uA.

This explains why there is a deviation from ideal current values in the measurement results. Mismatch between MSB current cell and LSB current cell also results in a 'jagged' characteristic seen in Fig. 6.4 and Fig. 6.5 as *Din* increases. The output current range measured is from 8.2uA to 8.7mA. It is also important to note that the resolution of the oscilloscope used for measurement may not be high enough, resulting in inaccuracies in current measurement. Similar characterization is also done for the pDAC. Fig. 6.6 shows the full-scale characteristics of the pDAC.

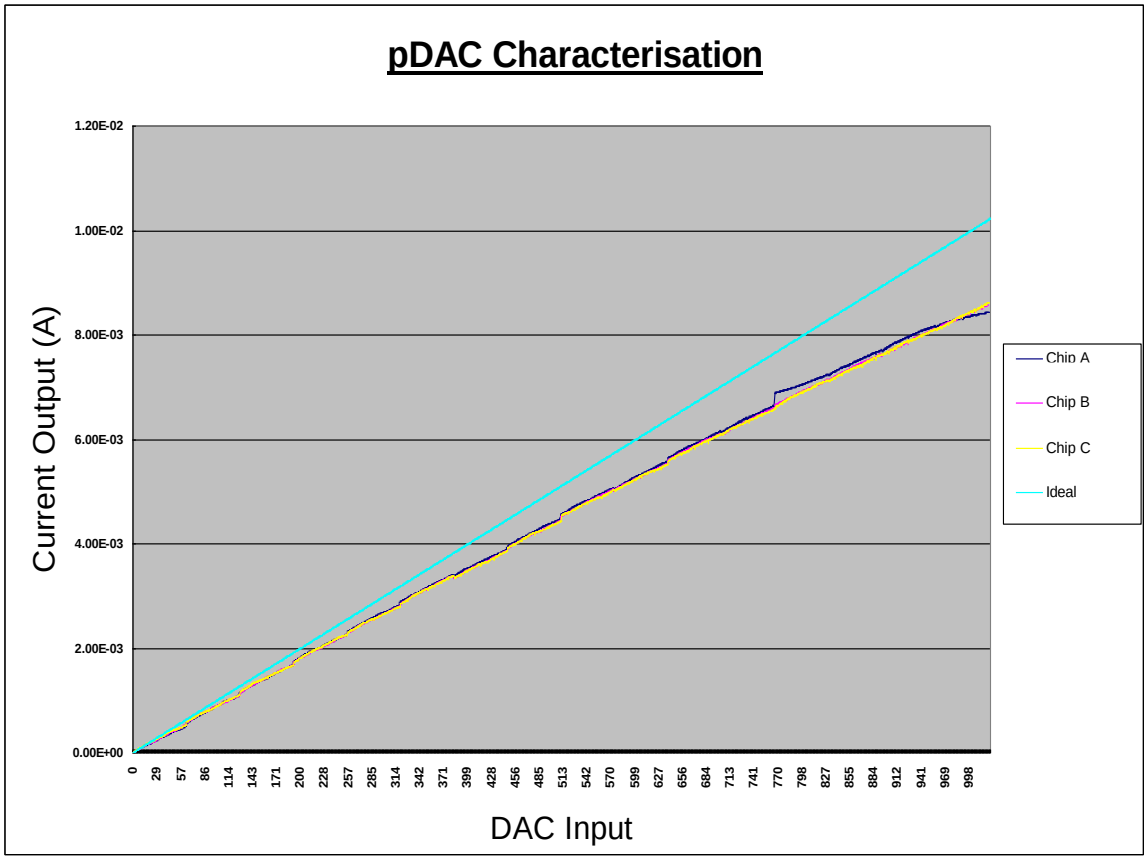

Fig. 6.6 Full-scale characterization of the pDAC

Similar to the nDAC characteristics, deviation from the ideal current values increases with DAC input code, *Din*. Percentage deviation from the ideal current output for all inputs for the pDAC is shown in Fig. 6.7.

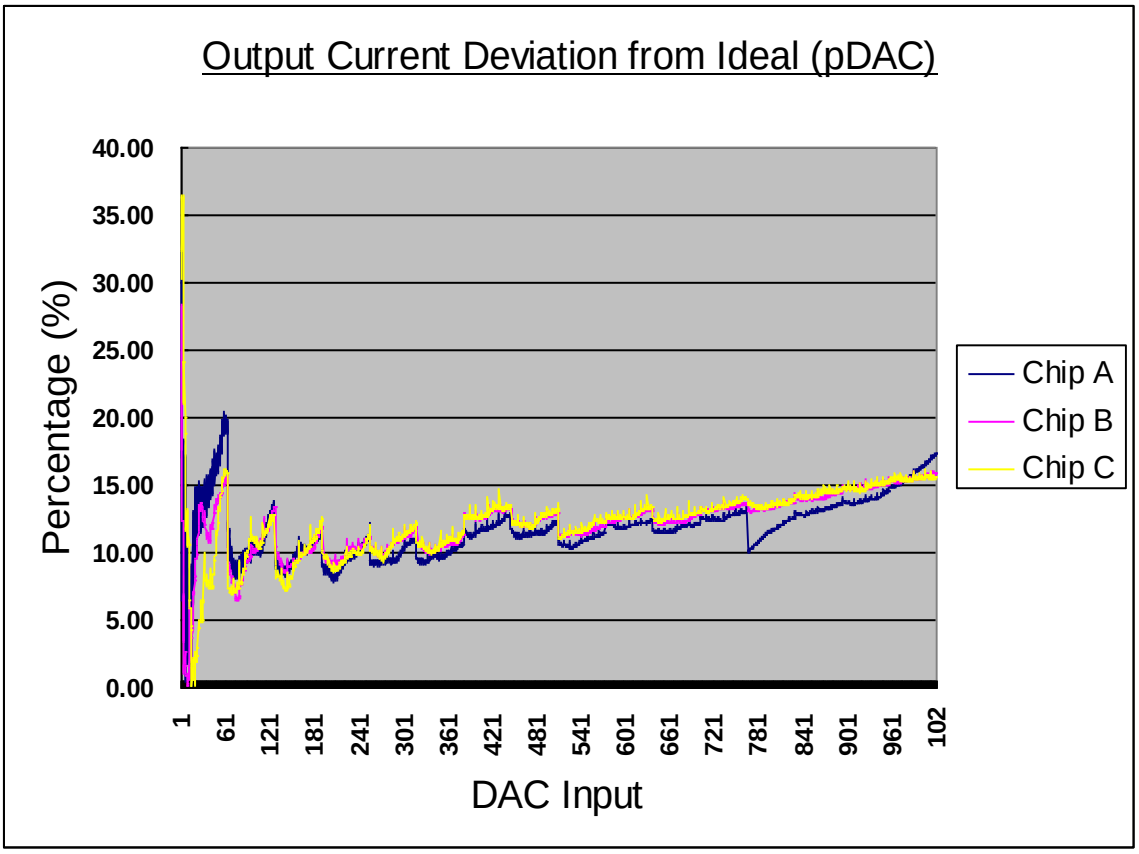

Fig. 6.7 Output current deviation from ideal values for pDAC

Measured LSB current of the pDAC is 12uA while the MSB current is 581.7uA. Output current range of the pDAC is from 12uA to 8.55mA. From Fig. 6.7, percentage deviation from ideal current values range between 5-20% as well for the pDAC. The same 'jagged' characteristic can be seen in pDAC characterization due to mismatch between the LSB current cell and MSB current cell.

Since there is a mismatch between the MSB current cells and LSB current cells, the 10-bit DAC is split into two parts: 6-bit LSB DAC with LSB current cells and 4-bit MSB DAC with MSB current cells. This is to test if the LSB current cells and MSB current cells are linear on their own and to verify that the 'jagged' characteristic is really due to their mismatch. Fig. 6.8 shows the nDAC characteristics for both 6-bit LSBs and 4-bit MSBs.

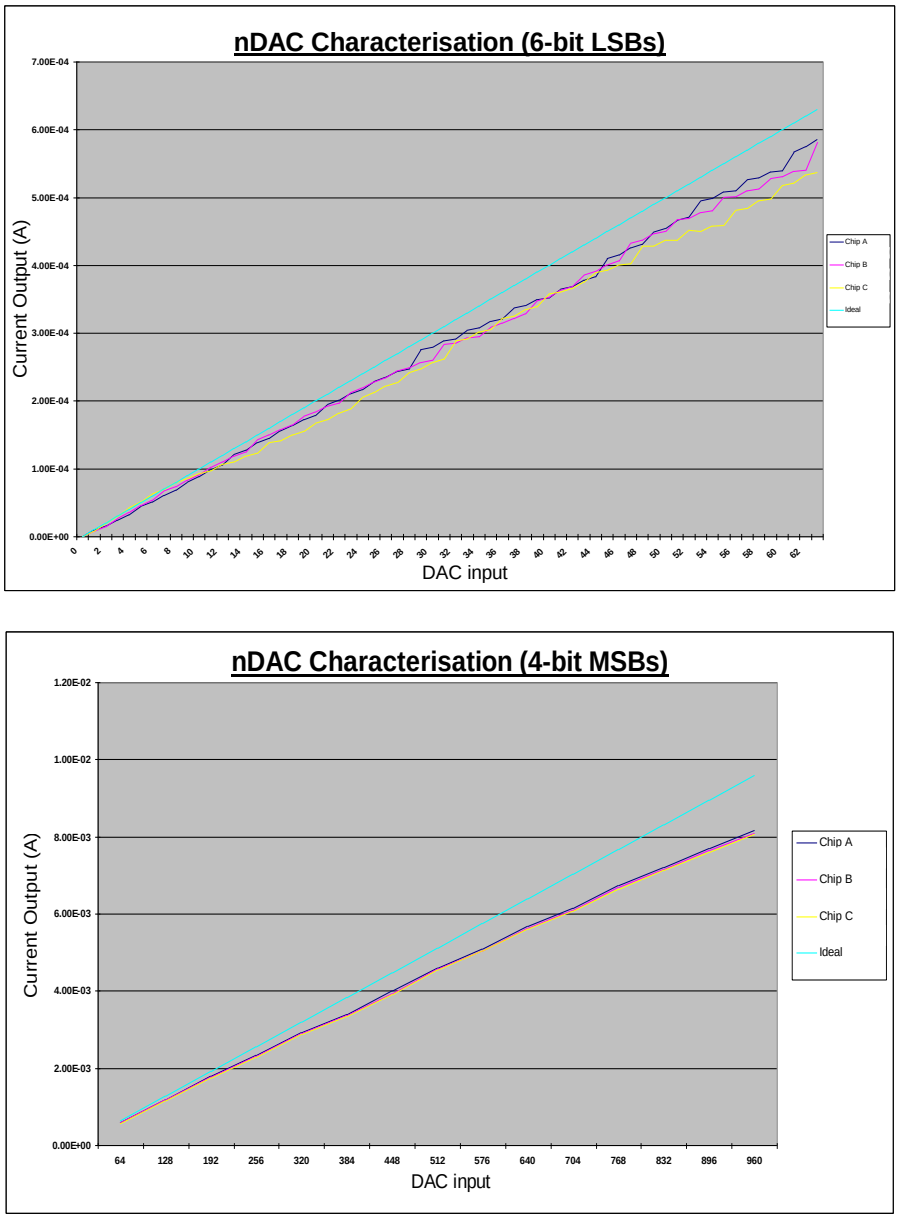

Fig. 6.8 nDAC characteristics for 6-bit LSBs and 4-bit MSBs

Once the 10-bit DAC is split according into 6-bit LSB DAC using the LSB current cells and 4-bit MSB with MSB current cells, the ‘jagged’ characteristic is no longer seen. This means on their own, the LSB current cells and MSB current cells are linear. Similar measurements are done for the pDAC.

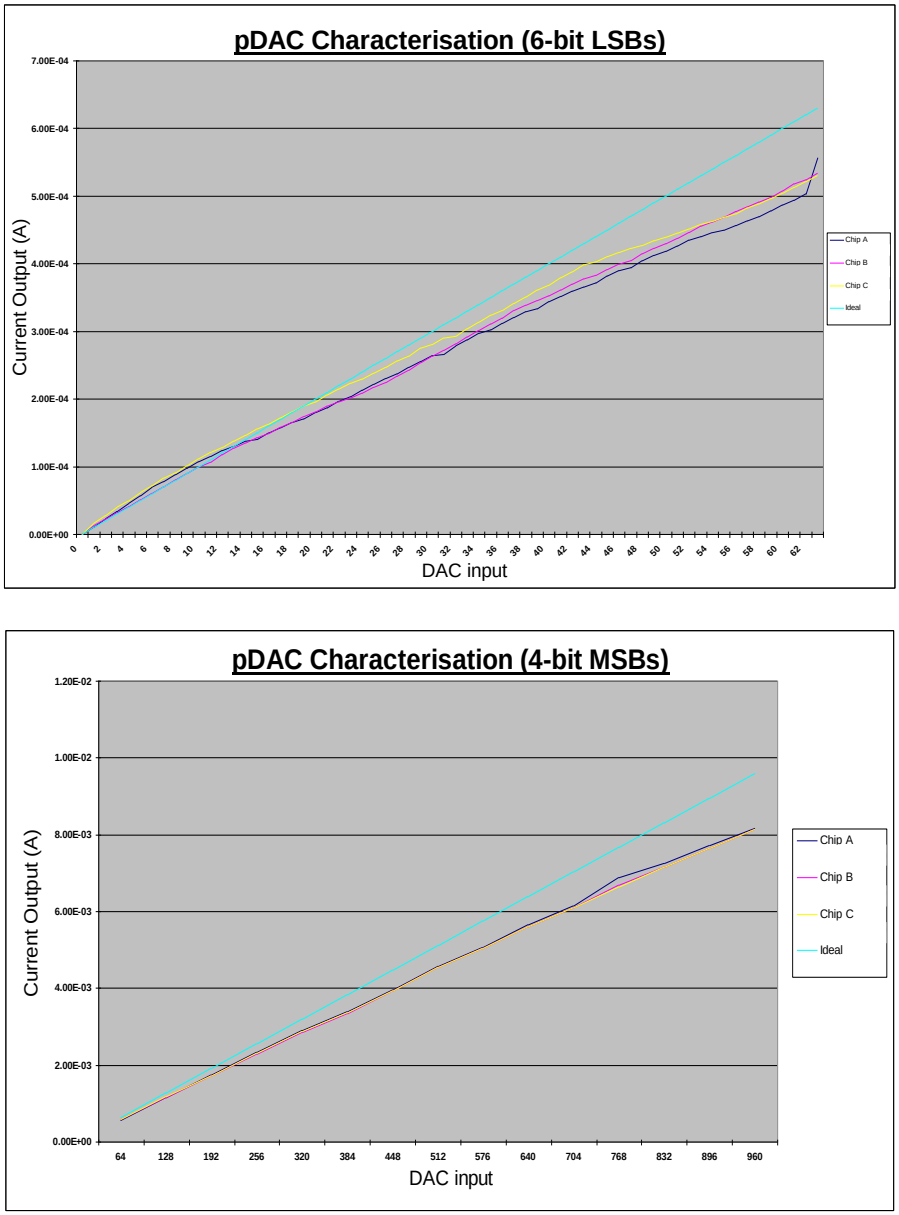

Fig. 6.9 pDAC characteristics for 6-bit LSBs and 4-bit MSBs

pDAC characteristics in Fig. 6.9 also verifies that the LSB current cells and MSB current cells are actually linear on their own. The 'jagged' characteristic is also not present if the pDAC is split according to LSB current cells and MSB current cells.

6.2.2 Dual-slope stimulator performance

Having done with the DAC characterization, measurements are done for the dual-slope stimulator. The pattern generator function of a logic analyzer is used to generate synchronized inputs for *Din*, *Clear* and *Phase*. Fig. 6.10 shows the measured waveform captured from an oscilloscope.

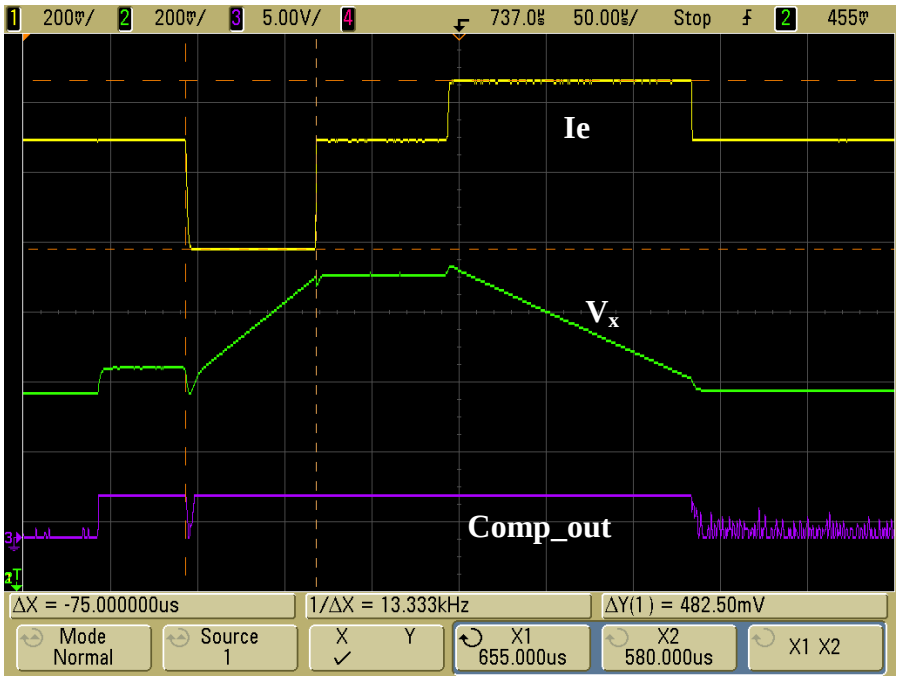

Fig. 6.10 Measured waveforms of the dual-slope stimulator

Three waveforms are captured using an oscilloscope, namely the current output, Ie, voltage across the capacitor, V_x and the output of the comparator, Comp_out. A

rectangular biphasic stimulus can be clearly seen from Fig. 6.10. The dual-slope profile of V_x can also be observed. It can also be seen that the comparator output changes to logic '0' after V_x falls to a certain value. Performance of the dual-slope stimulator is summarized in Table 6.2 below. Note that Ic = cathodic current amplitude; Ia = anodic current amplitude; Tc = cathodic pulsewidth and Ta = anodic pulsewidth.

	Ic (A)	**Ia (A)**	**Tc (s)**	**Ta (s)**	**Excess Charge (C)**	**Charge balance mismatch (%)**
Ic = Ia	4.49m	4.45m	200u	218u	71.09n	7.91
	697u	709u	1m	900u	31.45n	4.5
Ic > Ia	3.03m	2.22m	200u	246u	59.45n	9.8
	5.53m	3.15m	75.0u	140u	25.84n	6.2
	2.63m	764u	120u	376u	28.22n	8.9
	989u	798u	750u	1.03m	78.60n	10.6

Table 6.2 Performance of dual-slope stimulator

Measurement is done using different current amplitudes, pulsewidths and even stimulus profile. The first two rows are data of a biphasic profile where the anodic current amplitude is the same as the cathodic amplitude while cathodic current is greater than anodic current for the last four rows of data. The dual-slope stimulator is able to achieve charge balance mismatch of about 10%. The amount of charge imbalance is in nano-Coulombs range which is lower than the safety tolerance level of 0.4uC/mm^2/stimulus pulse [25].

6.2.3 Digital stimulator performance

Next, measurement is done for the digital stimulator. Initial measurements show that current amplitudes in both anodic and cathodic phases are the same. This is not desired because anodic amplitude is supposed to be half the cathodic amplitude due to the binary shift circuit that divides the DAC input, *Din*, by 2 during the anodic phase. Further investigations revealed that there is an error in layout.

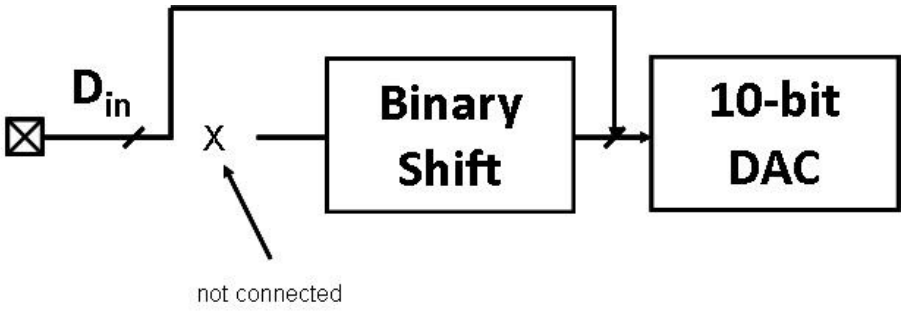

Fig. 6.11 Error in layout for the digital stimulator

As shown above, instead of connecting the input pads of *Din* to the binary shift circuit, they are connected directly to the DAC instead, hence bypassing the binary shift circuit. This explains why the anodic current is not half the cathodic current because no division of two has been performed during the anodic phase. To probe deeper, the reason why post-layout stimulation gives correct results even when there is such an error in layout is that post-layout stimulation is not done with I/O pads. In addition, LVS is not performed with pads as well. Therefore, this error has not been detected when doing post-layout simulations and LVS check.

To go around this problem such that the functionality of the digital stimulator can still be tested, the LSB current of the pDAC is reduced to 5uA to do a manual division by two. This is done by adjusting the external variable resistor value that biases the pDAC. Now, the pDAC outputs a current range of 5uA to 5mA which is half of the nDAC. Hence, even when *Din* is not divided by two, due to the error in layout, the anodic current amplitude will still be half the cathodic current amplitude. Fig. 6.12 shows the output current waveform captured from an oscilloscope.

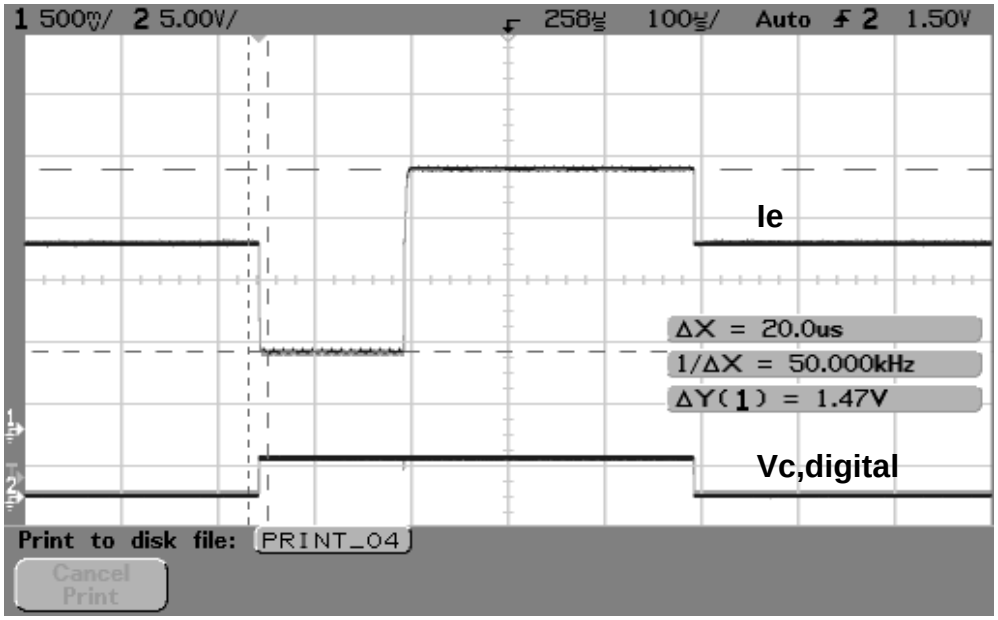

Fig. 6.12 Measured waveforms of the digital stimulator

The top waveform is the current output of the digital stimulator that is the desired rectangular biphasic stimulus. In this case, *Delay* is set at logic '0' such that there is no interphasic delay. The bottom waveform is the Vc,digital signal. This shows the interval at which the stimulator outputs a current. Since there is no interphasic delay, Vc,digital remains at logic '1' throughout the entire biphasic stimulus profile. Regions

with no current output correspond to Vc,digital having logic ‘0’. Performance of the digital stimulator is summarized in Table 6.3 below based on a 100kHz clock input.

Ic (A)	**Ia (A)**	**Ia/Ic ratio**	**Tc (s)**	**Ta (s)**	**Excess Charge (C)**	**Charge balance mismatch (%)**
4.642m	2.241m	0.483	10u	20u	1.61n	3.47
2.212m	1.124m	0.508	30u	60u	1.085n	1.63
375.1u	187.5u	0.500	70u	140u	93.41p	0.04
235.7u	114.5u	0.486	150u	300u	9.904n	2.80
592.6u	281.3u	0.475	10u	20u	299.69p	5.06
23.33u	11.68u	0.501	30u	60u	108.78p	0.16

Table 6.3 Performance of the digital stimulator

Despite the error made in layout, by tuning the pDAC such that it always outputs an anodic current half of the nDAC, a ratio of close to 0.5 is achieved between the anodic current amplitude and cathodic current amplitude. The counters work perfectly to give the exact desired pulsewidths. Charge balance mismatch achieved is around 5% and the amount of charge imbalance is in pico-Coulombs to less than 2nC range which is definitely below the safety tolerance of 0.4uC/mm^2/stimulus pulse [25].

CHAPTER SEVEN: CONCLUSION AND FUTURE WORK

7.1 Performance comparison

This thesis presents a programmable stimulator implemented in two architectures. First is an architecture that uses analog circuitry and the concepts behind dual-slope ADC to achieve charge balance and programmability of stimulation parameters. This is known as the "dual-slope stimulator". The other, the digital stimulator, is an architecture that uses digital logic to achieve charge balance and program stimulation parameters. Both architectures are then incorporated into a single chip, making use of the same DAC for different current levels. This chip has been fabricated and both stimulator versions have silicon results to prove their functionality. Here, a comparison is made between the two stimulator versions to see which architecture gives better charge balance accuracy.

	Dual-slope stimulator	**Digital stimulator**
Maximum excess charge (C)	78.60n	9.904n
Worst charge balance mismatch (%)	10.6	5.06

Table 7.1 Performance comparison between stimulator versions

From Table 7.1, the digital stimulator performs better in terms of charge balance accuracy. This is expected because charge balance accuracy for the digital stimulator is only affected by mismatch between pDAC and nDAC. For the dual-slope stimulator, there are more factors affecting charge balance accuracy (see chapter four for details). However, the dual-slope stimulator has merits over the digital stimulator

as well. Below summarizes the merits and drawbacks of each stimulator version.

	Dual-slope stimulator	Digital stimulator
Merits	• Full programmability for stimulation parameters • Mismatch between pDAC and nDAC does not affect charge balance accuracy • Able to generate different stimulus profiles including monophasic or anodic-first, cathodic-last stimulus	• Excellent charge balance accuracy achieved • Simple architecture • Easy to operate as only DC inputs are required
Drawbacks	• Charge balance accuracy limited by analog circuitry due to input offset and finite transconductance • Requires two DACs in total, including the scaled-down DAC • Linearity matching between the two DACs is hard to achieve, especially when the current amplitude of the scaled-down DAC is so small • Requires synchronized square-wave inputs	• Only generates cathodic-first, anodic-last biphasic stimulus profile • Anodic amplitude is always half the cathodic amplitude • Limited programmability on pulsewidth • Any mismatch between pDAC and nDAC will affect charge balance accuracy

Table 7.2 Merits and drawbacks for both stimulator versions

7.2 Second prototype of the proposed stimulator

The proposed stimulator is later included in a larger system that includes a neural recording system, a level-detection circuit, wireless power circuitry, clock generator and the stimulator circuit itself. This system aims to record a neural signal, amplifies it and feeds it to a level-detection circuit that will then trigger the stimulator to output

a biphasic stimulus. Fig. 7 shows the block diagram of the overall system.

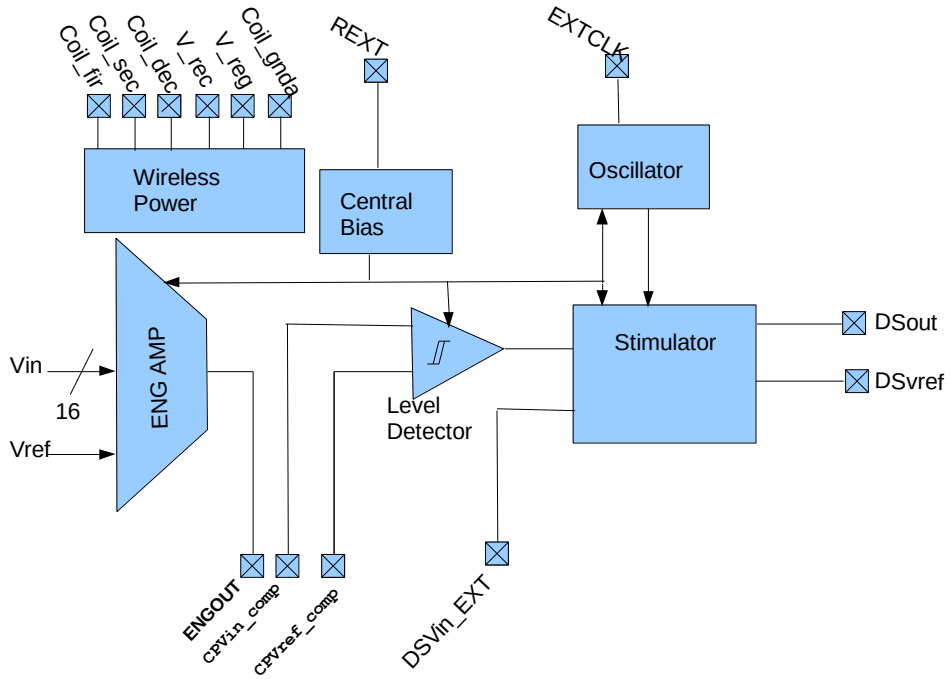

Fig. 7.1 Block diagram of overall neural system

This neural system consists of the following circuit blocks,

- Wireless power: this is a RFID circuit that aims to provide power to the entire system via wireless inductive link
- Central bias: a biasing circuit, implmented using bandgaps, that provides current bias to all circuit blocks, except RFID circuit
- Oscillator: generates clock signals of different frequencies for the stimulator and ENG amplifiers
- ENG amplifiers: 16-channel neural recording amplifiers with programmable gain
- Level detector: a comparator that compares the amplified neural signal against

a reference threshold voltage and triggers the stimulator to start stimulation

- Stimulator: The same programmable stimulator including both dual-slope and digital versions

This neural system has been implemented in Cadence and has been sent for fabrication. As the fabricated chips will only be back after a few months, measurement results are not included within the scope of this thesis. For this tapeout, several improvements have been made to the stimulator circuit. Fig. 7.2 shows an overview of the modified stimulator.

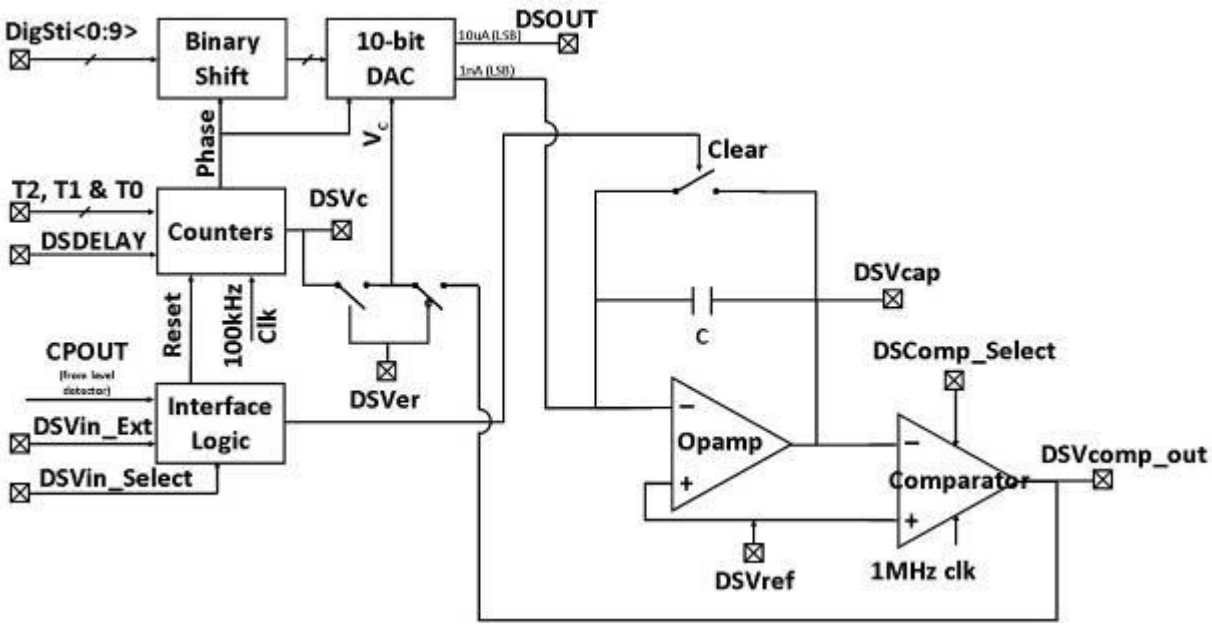

Fig. 7.2 Overview of the modified stimulator

Modifications have been made to the dual-slope stimulator such that its operation becomes easier. To overcome the issue of requiring synchronized square-wave inputs for the dual-slope stimulator, counters are used to program the cathodic phase, leaving

the anodic phase to be balanced by the dual-slop architecture. In other words, the dual-slope stimulator works exactly like the digital stimulator for the cathodic phase and interphasic delay phase. Hence, both stimulator versions are now controlled by the counters and through version select input, *DSVer*, the DAC is controlled via different circuitry to achieve charge balance. Besides the counters and the binary shift circuit, all other circuit blocks in Fig. 7.2 have been modified for better performance. The following sections provide details on the exact modification done to each circuit blocks.

7.2.1 Modifications to 10-bit DAC

First of all, for the DAC, a biasing circuit has been designed based on the central bias circuit to provide both current bias for the current cells and voltage bias for cascode voltages. In addition, a current splitting circuit based on [35] is used to generate current bias of 1nA for the scaled-down DAC from the 10uA LSB current source. Fig. 7.3 shows the schematic of the current splitting circuit with the current sources of the scaled-down DAC.

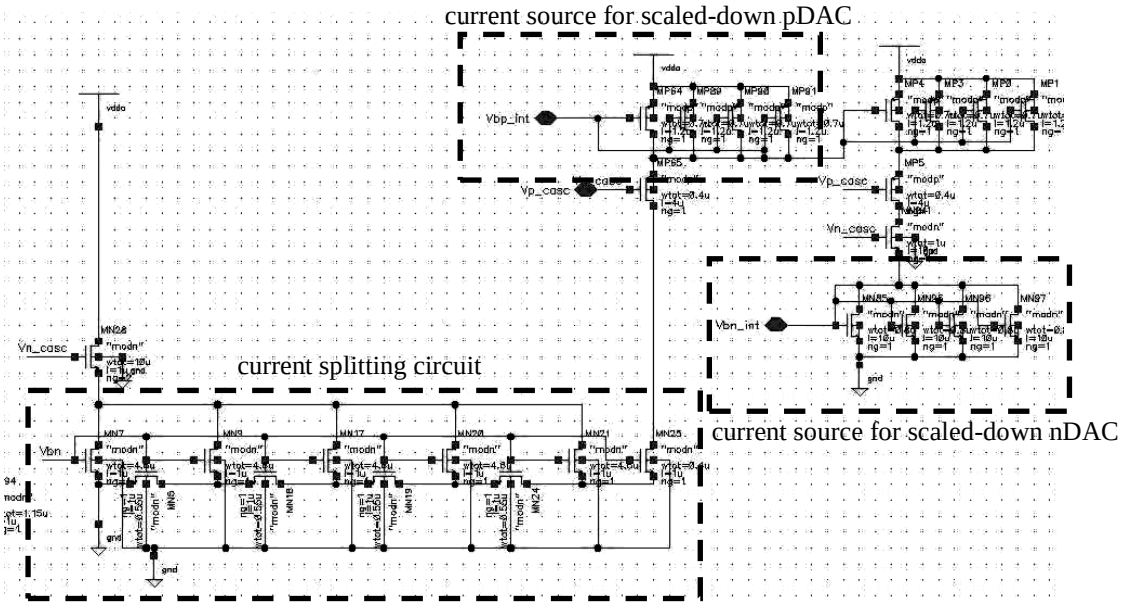

Fig. 7.3 Schematic of current splitting circuit

With the biasing circuit, all biasing is now done internally. Besides including a biasing circuit, a non-overlapping switching scheme has been implemented for all current cells to further reduce switching glitches.

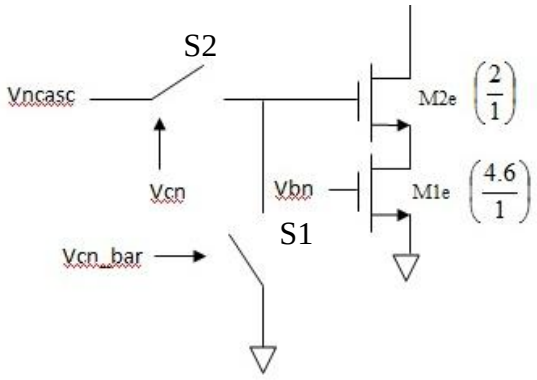

Fig. 7.4 Partial schematic of a current cell

The switches S1 and S2 are controlled such that only one of the switches will be on at any time. From Fig. 7.4, without non-overlapping switching, both S1 may switch off first before S2 switches on. This causes the gate of the cascode transistor M2e to be

floating momentarily and once S2 is on, a large voltage change may occur at the gate. But with non-overlapping switching, S2 will be on before S1 turns off. In this way, at any time, the gate of M2e will not be floating, thereby reducing switching glitches. Similarly, S1 will be on first before S2 goes off. Fig. 7.5 shows the schematic of the circuit that generates non-overlapping outputs. This is a typical non-overlapping clock generation circuit.

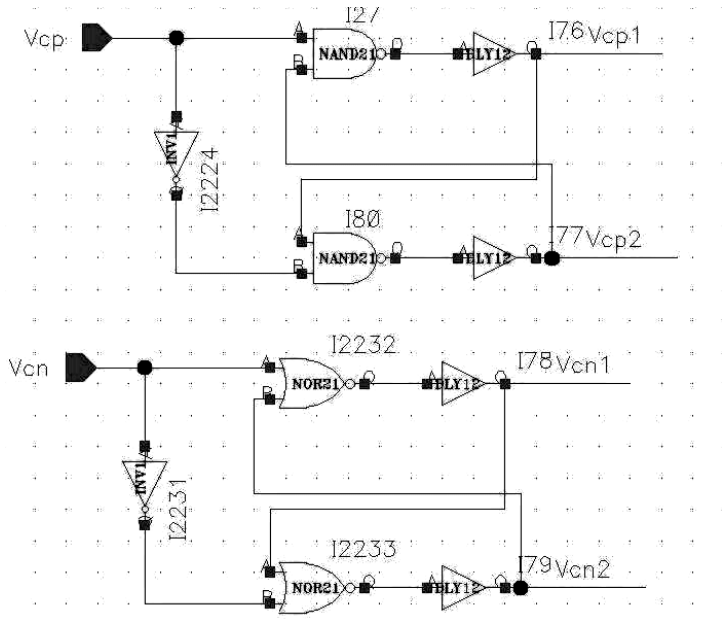

Fig. 7.5 Schematic of non-overlapping clock generation circuit

The control signals *Vcn* and *Vcp* are now input to this circuit to generate non-overlapping controls signals to control the switches of the current cells. Fig. 7.6 shows a block diagram of the DAC including the non-overlapping clock generation circuit.

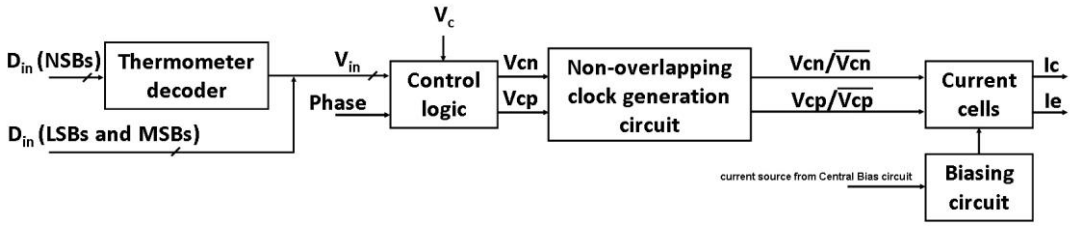

Fig. 7.6 Block diagram of improved DAC

Now, each current cell has its own clock generation circuit and this is added into the layout of each current cell as well. Fig. 7.7 shows the layout of the new current cells.

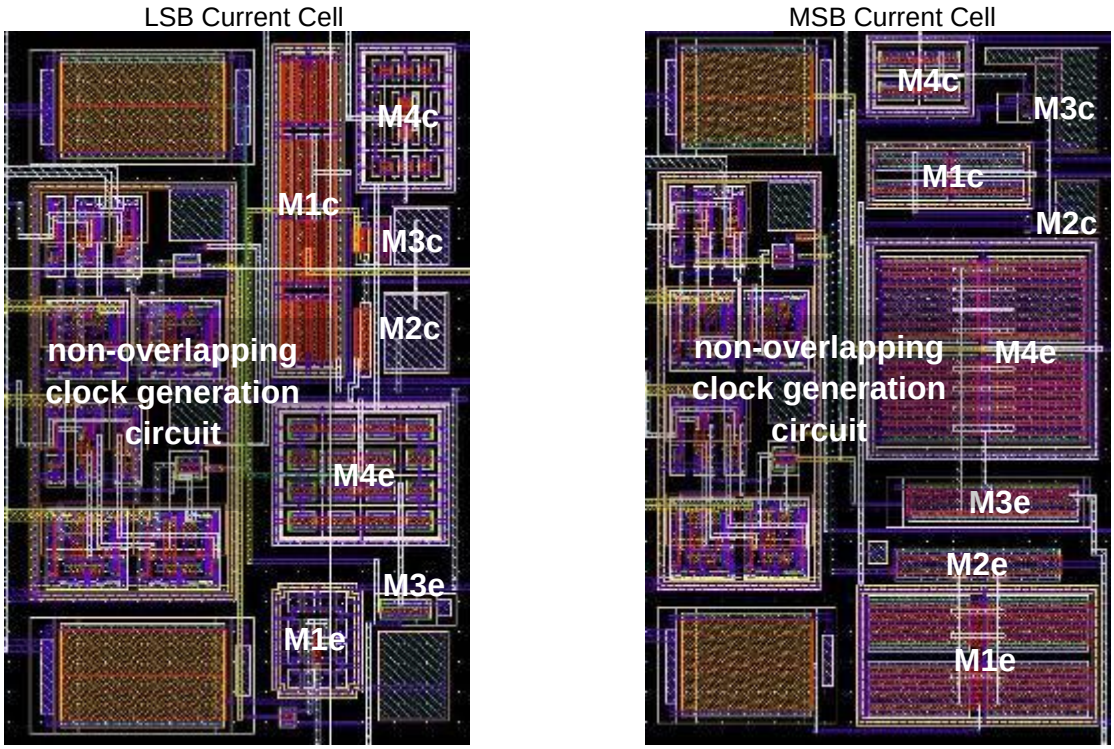

Fig. 7.7 Layout of new LSB current cell and MSB current cell

Fig. 7.7 is labeled according to the schematic of the current cell seen in Fig. 3.2 (see chapter three). Large decoupling pMOS capacitors are also added for the biasing lines.

7.2.2 Interface logic circuit

The interface logic circuit takes the output from the level detection circuit and triggers the stimulator to start stimulation. Fig. 7.8 shows the schematic of the interface logic circuit.

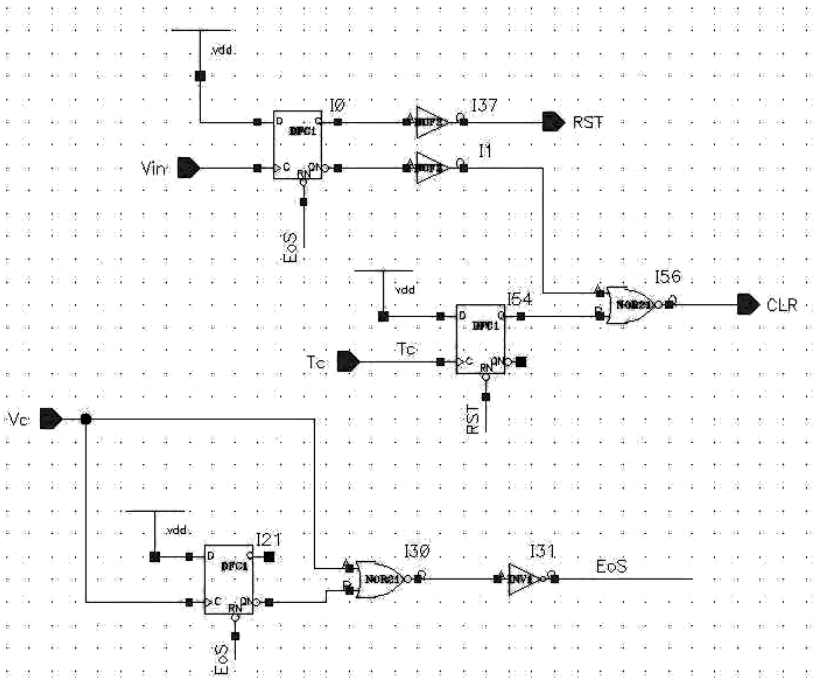

Fig. 7.8 Schematic of interface logic circuit

The main function of the interface logic circuit is to sense logic '1' from the output of the level detection circuit and triggers stimulation. During the course of a biphasic stimulus, any subsequent triggers from the level detection circuit will be ignored and once a complete biphasic stimulus has ended, the interface logic circuit resets itself and outputs *Clear* to short the capacitor, C, of the dual-slope stimulator and *Reset* to reset the counters.

7.2.3 Integrator opamp modifications

The opamp architecture is also changed so as to achieve higher gain for the integrator. A current-mirror operational transconductance amplifier or OTA is implemented and its schematic is shown in Fig. 7.9.

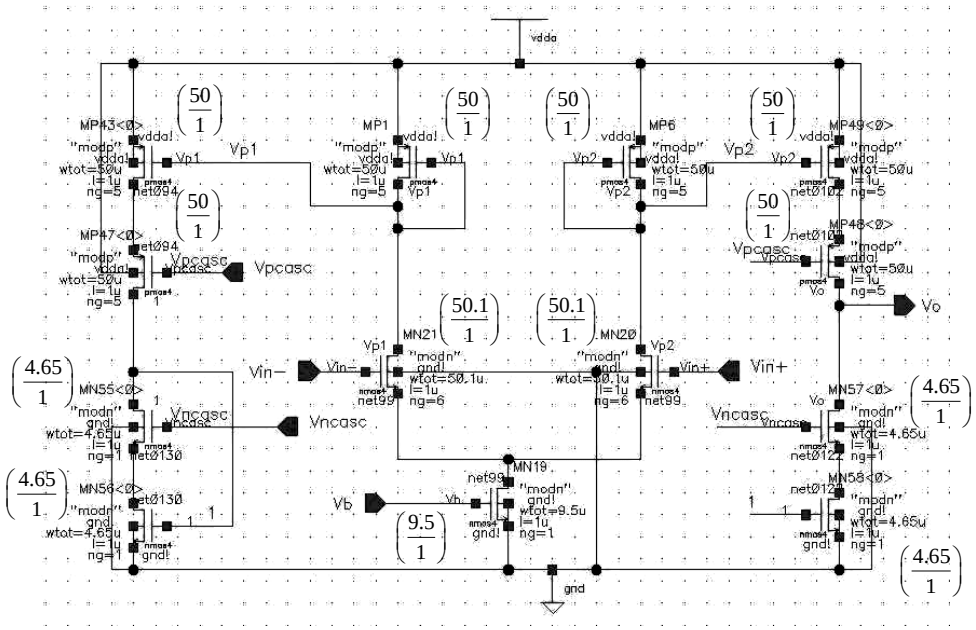

Fig. 7.9 Schematic of the current-mirror OTA

Total current consumption of the OTA is 40uA. Layout of the OTA is drawn symmetrically for better matching. Fig. 7.10 and Fig. 7.11 show the layout and post-layout bode plots of the current-mirror OTA respectively.

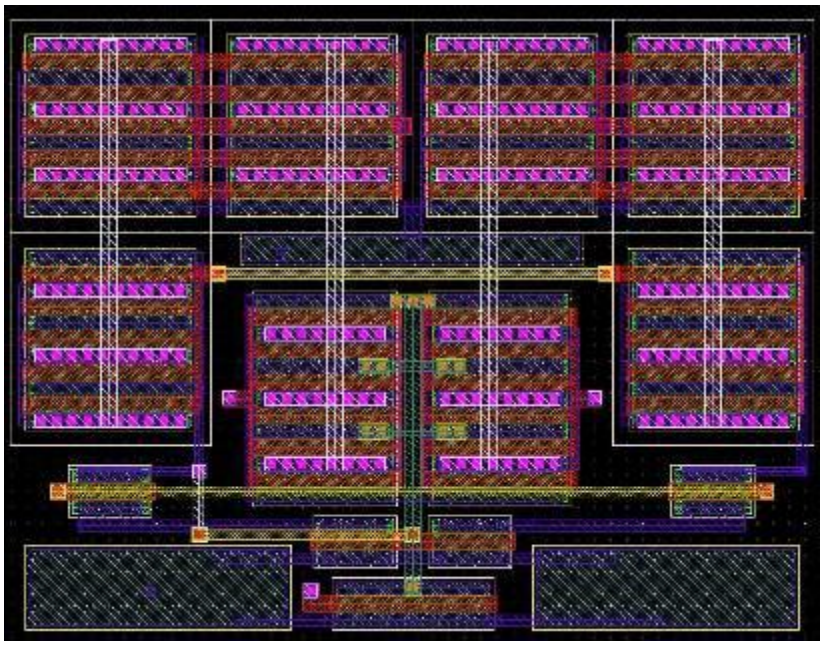

Fig. 7.10 Layout of current-mirror OTA

The layout of the current-mirror OTA is drawn in a symmetrical arrangement for better matching. Post-layout simulations are done after this to look at the gain and phase margin of the OTA.

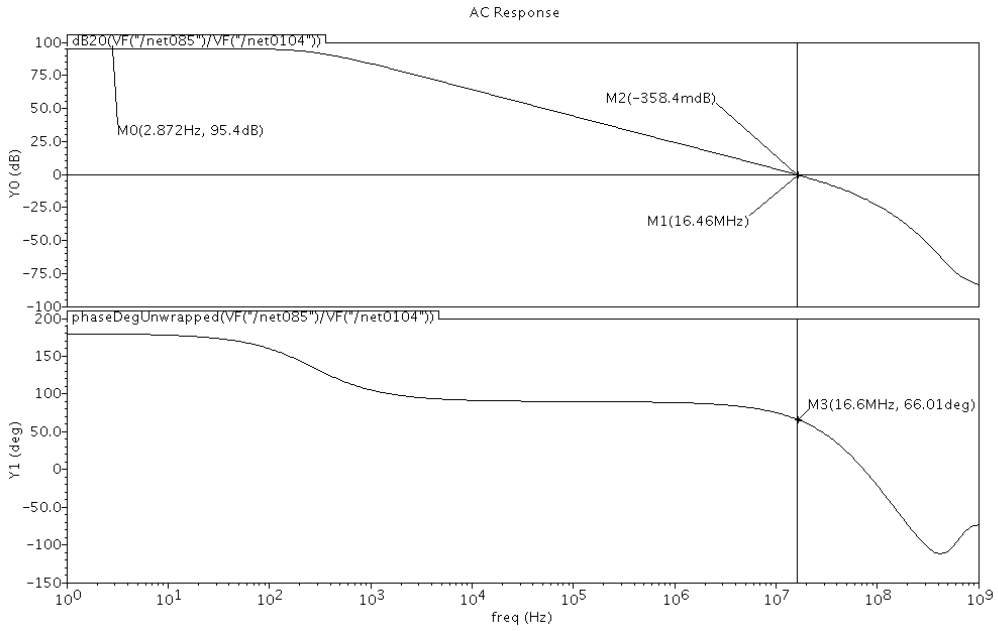

Fig. 7.11 Post-layout bode plots of current-mirror OTA

From the post-layout simulations, the DC gain achieved is 95.4dB which is higher than the gain of 77.97dB of the previous telescopic opamp. Phase margin is 66.01 degrees.

7.2.4 "Dual-version" comparator

As mentioned in chapter three, the crossover point of the voltage across the capacitor, V_x, affects charge balance accuracy due to track and latch phases of the latched comparator. This problem will be alleviated if a continuous-time comparator is used. However, the speed of a continuous-time comparator cannot match that of a latched comparator. To investigate which comparator architecture gives better charge balance accuracy, a "dual-version" comparator is implemented.

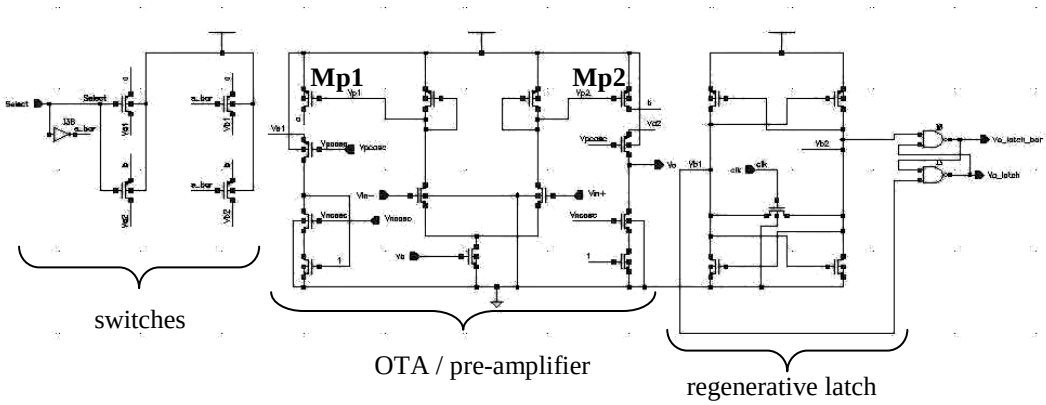

Fig. 7.12 Schematic of the "dual-version" comparator

Transistors, Mp1 and Mp2, are either connected to the pMOS cascode transistors below to complete the circuit of the OTA or to the regenerative latch to form a latched comparator. They are connected through switches on the right and these switches are controlled via an input signal, *DSComp_Select*. A logic '1' for *DSComp_Select* means

OTA architecture is selected and logic ‘0’ means latched comparator architecture is selected.

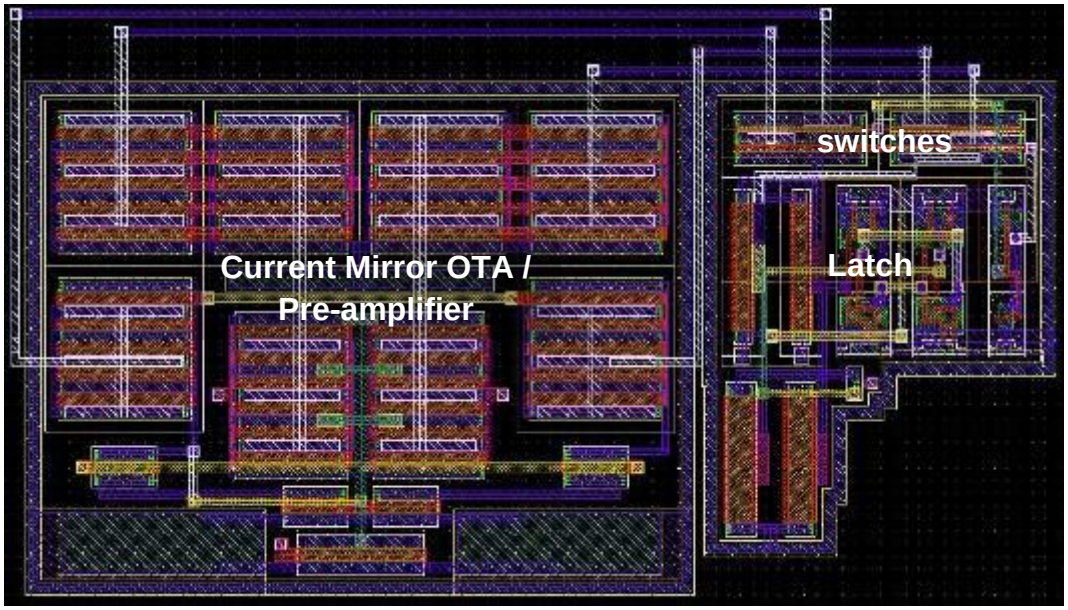

Fig. 7.13 Layout of the “dual-version” comparator

From Fig. 7.13, it can be seen that the right portion is exactly the same as the layout of the current-mirror OTA. Once again, digital circuitry is separated from analog part to reduce noise coupled into the OTA or pre-amplifier. Input offset cancellation technique is also implemented to eliminate input offset of the comparator. The offset of the comparator is sensed before the start of each stimulation cycle and this amount of offset is stored in a capacitor at the input of the comparator.

7.2.5 Layout and post-layout simulations

The neural system has been implemented in Cadence and the stimulator circuit has been integrated into the system. Layout of the entire neural system is shown below.

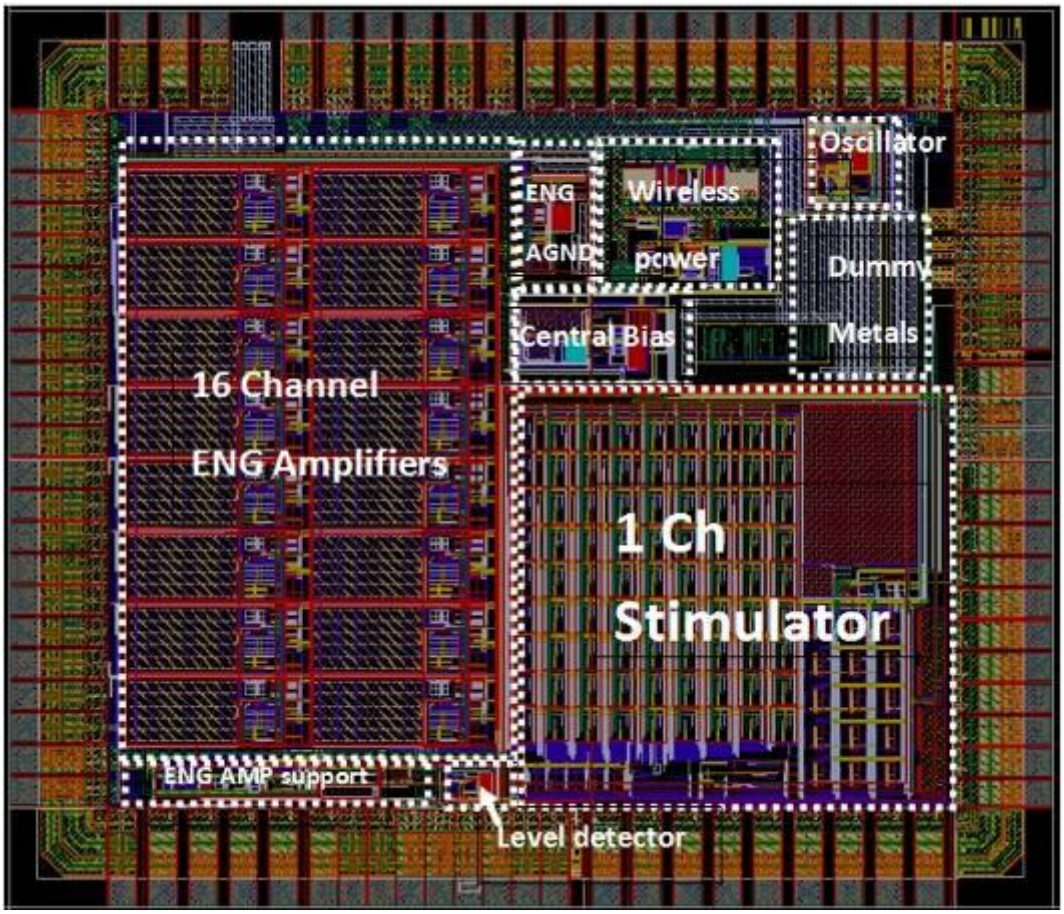

Fig. 7.14 Layout of the overall neural circuit

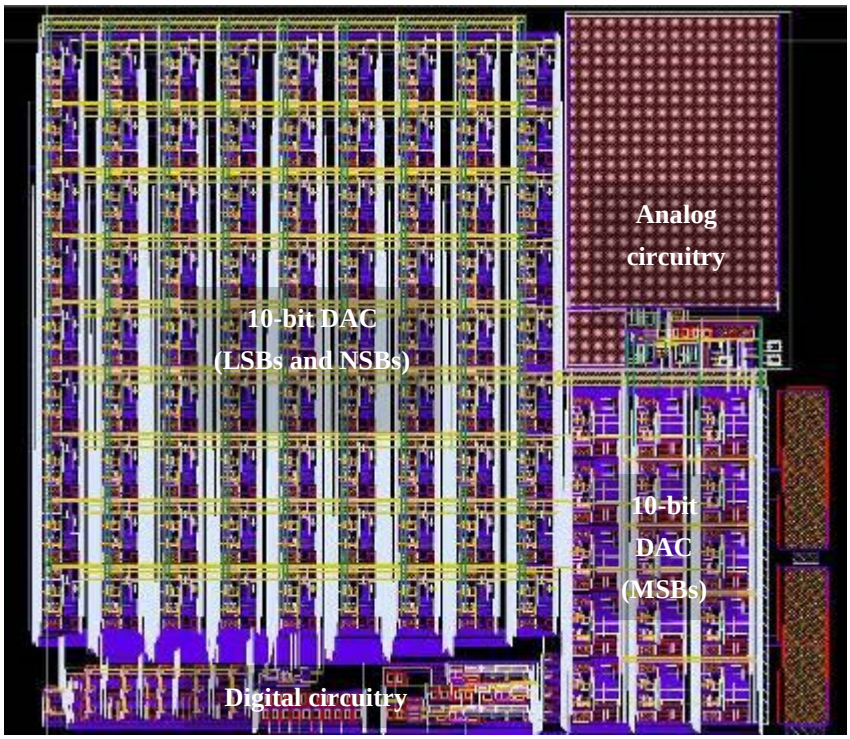

Fig. 7.15 Layout of the modified stimulator

The layout of the modified stimulator looks identical to the previous layout except that modifications mentioned in the previous sections have been included. Also, large pMOS decoupling capacitors are added for the biasing lines. Overall layout size of the stimulator remains the same as the previous tapeout. To prevent the same errors from happening, post-layout simulations and LVS checks are done with I/O pads. This will ensure that there will not be any routing errors in layout for this tapeout. Table 7.3 summarizes the performance of the modified stimulator based on post-layout stimulations.

Ic (A)	**Ia (A)**	**Tc (s)**	**Ta (s)**	**Excess Charge (C)**	**Charge balance mismatch (%)**
Digital Stimulator					
10.12m	5.101m	10u	20u	1.64n	1.67
7.074m	3.540m	70u	140u	800p	0.16
4.524m	2.264m	150u	300u	700p	0.10
2.143m	1.073m	30u	60u	10p	0.02
229.8u	1.150m	70u	140u	10p	0.06
9.990u	5.031m	150u	300u	10p	0.71
Dual-slope stimulator with OTA as comparator					
10.19m	5.101m	10u	22.5u	12.48n	14.58
7.037m	3.540m	10u	22.2u	7.86n	12.09
7.037m	3.540m	150u	301u	3.00n	0.38
Dual-slope stimulator with latched comparator					
10.19m	5.101m	10u	22.8u	14.5n	16.61
7.037m	3.540m	10u	22.9u	10n	15.07
7.037m	3.540m	150u	301u	2.83n	0.38

Table 7.3 Performance of the modified stimulator circuit

Based on post-layout simulation results, the performance of the digital stimulator remains better than the dual-slope stimulator even after modifications has been done

on the opamp and comparator. However, when compared to the previous design, the performance of the dual-slope stimulator has indeed improved. Previously, charge imbalance can go above 50nC. Now, this amount has been reduced to less than 20nC. This may be due to the input offset cancellation of the comparator and increased gain of the integrator opamp and the comparator. Also, comparing the charge balance accuracy achieved by using either the OTA comparator or latched comparator, it seems like both architectures gives similar charge balance accuracy.

7.3 Conclusion

This thesis presented two different muscle stimulator designs incorporated into a single silicon chip. Much focus is placed on charge balance accuracy achieved for the output biphasic stimulus and also programmability of stimulation parameters. This is so because as reflected in chapter two, most publications on stimulators did not mention about the charge balance accuracy achieved. With the implications on charge balance accuracy on tissue damage in chapter one in mind, it is important to strive to achieve charge balance accuracy as high as possible to ensure that implanted stimulators are safe for chronic use. In addition, stimulation parameters need to be programmable for experimental and calibration purposes. From literature review in chapter two, the only programmable stimulation parameters in all published stimulators are stimulation amplitude, frequency and pulsewidth. Other features of the biphasic stimulus like the interphasic delay, anodic current amplitude and the stimulus profile are fixed. Till now, there has not been any verification of the significance of

biphasic stimulus profile, which is dependent on features like the interphasic delay, ratio between anodic current amplitude and cathodic current amplitude and whether stimulus is cathodic-first, anodic-last or anodic-first, cathodic-last, on the effectiveness on functional electrical stimulation.

The dual-slope stimulator provides full programmability on stimulation parameters such that different stimulus profile can be achieved. Through different inputs, the dual-slope stimulator can output biphasic stimulus of all profiles be it cathodic-first or anodic-first. Cathodic or anodic monophasic stimulus outputs are also possible. This gives full flexibility on the calibration of the stimulator during animal experiments so that the effectiveness of different stimulation waveforms can be investigated. It is also noteworthy to mention that the dual-slope architecture has not been used in any published work. Although the methodology to achieve charge balance is similar to [27], efforts have been made in the design of the dual-slope simulator to allow the charging capacitor to be implemented on-chip.

The digital stimulator on the other hand, offers a much simpler architecture to meet the same objectives as the dual-slope stimulator. Although programmability of stimulation parameters is compromised, the charge balance accuracy achieved is higher as compared to the dual-slope stimulator and the controls of this stimulator are much simpler as well.

In summary, it is proven with silicon results that both stimulators can output programmable rectangular biphasic stimuli, with charge balance accuracy within safety tolerance levels. Besides that, both designs are incorporated into a single chip such that any stimulator version can be chosen via a digital input. Merits and limitations of both stimulators are also discussed and a comparison has been made between them to see which design gives better charge balance accuracy. Last but not least, improvements have been made in the second prototype to achieve better charge balance accuracy and this is verified through post-layout simulations.

7.4 Future work and challenges

Although the programmable stimulator is able to meet the proposed specifications, there are many areas that still require much research work to be done. A few of these are listed below.

- DAC linearity can be further improved by better DAC architectures, more stringent layout measures and better matching techniques for the current cells.
- Programmability of the digital stimulator can be enhanced by more complex logic circuits.
- Architecture of the dual-slope stimulator can be reviewed such that a scaled-down DAC may not be required. This is because due to the small current output of the scaled-down DAC, it is difficult to ensure linearity of this DAC. Also, since the current source transistors operate in weak inversion, any small change in gate bias voltage will cause a large difference in current

output, hence introducing inaccuracies.

- Investigate ways to include multi-channel stimulation using a single stimulator circuit. One proposed way is to multiplex the output terminal of the stimulator to different output electrodes.
- Include feedback architecture to detect conditions like over-stimulation or under-stimulation.
- Electrode impedance could also be monitored to detect electrode corrosion or even be a basis to adjust the supply voltage so as to output a consistent amount of stimulus current.

REFERENCES

[1] G. Boschetti, "Guide to Understanding Electro-Muscle Stimulation for Sport Training", *EMS Digest*, 2008, http://docs.google.com/Doc?docid=dgw665wn_33f8wb6ff9&hl=en#DIRECT_STIMULATION_OF_MUSCLE_F, retrieved 20th May 2009.

[2] M. Fairley, "FES: The 'Quiet' Revolution", The O&P EDGE, March 2008, http://www.oandp.com/articles/2008-03_01.asp, retrieved 19th Oct 2009.

[3] W. T. Liberson, H. J. Holmquest, D. Scot and M. Dow, "Functional electrotherapy: stimulation of the peroneal nerve synchronized with the swing phase of the gait of hemiplegic patients", *Arch Phys Med Rehabil*, vol. 42, pp. 101-105, 1961.

[4] "Cochlear Implants", *American Speech-Language-Hearing Association*, http://www.asha.org/public/hearing/treatment/cochlear_implant.htm, retrieved 11th Nov 2009.

[5] Tier Cardiology Group, "Understanding Pacemakers", *Cardiology Associates*, http://www.cardioassoc.com/patient_pgs/procedures/pacemaker.asp, retrieved 3rd Oct 2009.

[6] J. Fildes, “Trials for 'bionic' eye implants”, *BBC News*, Feb 2007, http://news.bbc.co.uk/2/hi/science/nature/6368089.stm, retrieved 3rd Oct 2009.

[7] Institute of Spinal Cord Injury, Iceland, “Functional Electrical Stimulation”, *HUMAN SPINAL CORD INJURY: NEW & EMERGING THERAPIES*, http://www.sci-therapies.info/FES.htm#Bladder-Bowel%20Management, retrieved 20th Dec 2009.

[8] P. H. Peckham, K. L. Kilgore, M. W. Keith, A. M. Bryden, N. Bhadra, F. W. Montague, “An Advanced Neuroprosthesis for Restoration of Hand and Upper Arm Control Using an Implantable Controller”, *J Hand Surg*, 27A, pp 265-276, 2002.

[9] W. S. Pease, H. L. Lew, E. W. Johnson, *Johnson's Practical Electromyography*, Lippincott Williams & Wilkins, 2007.

[10] P. H. Gorman and J. T. Mortimer, “The Effect of Stimulus Parameters on the Recruitment Characteristics of Direct Nerve Stimulation”, *IEEE Transactions on Biomedical Engineering*, vol. BME-30, no. 7, pp. 407 – 414, Jul 1983.

[11] X. Liu, A. Demosthenous, M. Rahal and N. Donaldson, “Recent advances in the design of implantable stimulator output stages”, *18th European Conference on Circuit Theory and Design*, pp. 204-207, Aug 2007.

[12] T. G. Constandinou, J. Georgiou and C. Toumazou, "A Partial-Current-Steering Biphasic Stimulation Driver for Neural Prostheses", *IEEE Transactions on Biomedical Circuits and Systems*, vol 2, Issue 2, pp.106 – 113, June 2008.

[13] J. C. Gwilliam and K. Horch, "A charge-balanced pulse generator for nerve stimulation applications", *Journal of Neuroscience Methods*, vol. 168, pp. 146 – 150, Sept 2007.

[14] A. Eftekhar, T. G. Constandinou, I. F. Triantis, C. Toumazou and E. M. Drakakis, "Towards a reconfigurable sense-and-stimulate neural interface generating biphasic interleaved stimulus", *3rd International IEEE/EMBS Conference on Neural Engineering*, pp. 438-441, May 2007.

[15] D. B. McCreery, W. F. Agnew, T. G. H. Yuen and L. A. Bullara, "Damage in peripheral nerve from continuous electrical stimulation: comparison of two stimulus waveforms", *Medical & Biological Engineering & Computing*, vol. 30, pp. 109 – 144, 1992.

[16] K. Ichihara, G. Venkatasubramanian, J. J. Abbas and R. Jung, "Neuromuscular electrical stimulation of the hindlimb muscles for movement therapy in a rodent model", *Journal of Neuroscience Methods*, vol. 176, pp. 213 – 224, 2009.

[17] A. C. D. Salter, J. R. Richmond and G. E. Loeb, "Prevention of Muscle Disuse Atrophy by Low-Frequency Electrical Stimulation in Rats", *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, vol. 11, no. 3, Sept 2003.

[18] W.M. Grill, Jr and J. T. Mortimer, "The effect of stimulus pulse duration on selectivity of neural stimulation", *IEEE Transactions on Biomedical Engineering,* Vol. 43, pp. 161-166, Feb 1996.

[19] A. Branner and R. A. Normann, "A multielectrode array for intrafascicular recording and stimulation in sciatic nerve of cats", Brain research bulletin, vol. 51, no. 4, pp. 293-306, 2000.

[20] M. Ortmanns, "Charge balancing in functional electrical stimulators: a comparative study", *IEEE International Symposium on Circuits and Systems,* pp. 573 – 576, 2007.

[21] J.D. Techer, S. Bernard, Y. Bertrand, G. Cathebras and D. Guiraud, "An implantable ASIC for neural stimulation", *IEEE International Workshop on Biomedical Circuits and Systems*, pp. S1/7/INV- S1/7/5-8, Dec 2004.

[22] A. Scheiner, J. T. Mortimer and U. Roessmann, "Imbalanced Biphasic Electrical Stimulation: Muscle Tissue Damage", Annual International Conference of the IEEE

Engineering in Medicine and Biology Society, vol. 12, no. 4, pp. 1486 – 1487, 1990.

[23]K. Nakauchi, T. Fujikado, A. Hirakata and Y. Tano, “A Tissue Change After Suprachoroidal-Transretinal Stimulation with High Electrical Current in Rabbits”, *Artificial Sight*, Springer New York, pp. 325-332, 2008.

[24]D. B. McCreery, W. F. Agnew, T. G. H. Yuen and L. A. Bullara, “Damage in peripheral nerve from continuous electrical stimulation: comparison of two stimulus waveforms”, *Medical & Biological Engineering & Computing*, vol. 30, pp. 109 – 144, 1992.

[25]J. T. Mortimer, D. Kaufman and U. Roessmann, “Intramuscular Electrical Stimulation: Tissue Damage”, *Annals of Biomedical Engineering*, vol. 8, pp. 235-244, 1980.

[26]B. K. Thurgood, N. M. Ledbetter, D. J. Warren, G. A. Clark and R. R. Harrison, “Wireless Integrated Circuit for 100-Channel Neural Stimulation”, *IEEE Biomedical Circuits and Systems Conf. (BioCAS 2008)*, pp. 129-132, Nov 2008.

[27]G. Gudnason, E. Bruun and M. Haugland, “An Implantable Mixed Analog/Digital Neural Stimulator Circuit”, *Symposium on Proceedings of the 1999 IEEE International Circuits and Systems, ISCAS '99*, vol.5, pp. 375 - 378, June 1999.

[28]E.K.F. Lee, and A. Lam, “A Matching Technique for Biphasic Stimulation Pulse”, *IEEE International Symposium on Circuits and Systems, ISCAS*, pp 817 – 820, May 2007.

[29]Q. Shen, D. Jiang and C. Tai, “Animal study on selective simulation of nerve fibers using biphasic rectangular pulses”, *Proceedings of the 20th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, vol. 20, no. 5, pp. 2546 - 2549, 1998.

[30]D. A. Johns and K. Martin, “Analog Integrated Circuit Design”, John Wiley & Sons, Inc., 1997.

[31]J. H. Kim and K. S. Yoon, “A 3.3V-70MHz Low Power 8-bit CMOS Digital to Analog Converter with Two Stage Current Cell Matrix Structure”, *IEEE 39th Midwest symposium on Circuits and Systems*, vol. 1, pp. 197-200, 1996.

[32]I. Benamrane and Y. Savaria, “Design techniques for high speed current steering DACs”, *IEEE NEWCAS*, pp. 1485-1488, 2007.

[33]M. Chandrasekhar Bh and S. Dasgupta, “A 1.2 volt, 90nm, 16-bit three way segmented digital to analog converter (DAC) for low power applications”, ISQED, pp. 447-450, 2009.

[34]C. Ionascu and D. Burdia, “Design and implementation of video DAC in 0.13μm CMOS technology”, *International Symposium on Signals, Circuits and Systems*, vol. 2, pp. 381-384, 2003.

[35] B. Linares-Barranco and T. Serrano-Gotarredona, “On the design and characterization of femtoampere current-mode circuits”, *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 1353-1363, 1993.