DESIGN AND IMPLEMENTATION OF A HIGH SPEED AND LOW POWER FLASH ADC WITH FULLY DYNAMIC COMPARATORS

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NATIONAL UNIVERSITY OF SINGAPORE

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Summary

This work primarily focuses on design and implementation of a high speed low power flash ADC with fully dynamic comparators. For flash ADC design, fully dynamic comparator offers several very desirable attributes, like high speed and low power consumption. As a result, a significant improvement of overall performance is expected. However, the application of fully dynamic comparator is restricted by a few things, among which large offset variation is a primary issue.

To capitalize the vast potential promised by fully dynamic comparator, we have first developed a background comparator offset calibration technique, which has provided a foundation for fully dynamic comparator's use in a flash ADC design. We use chopper to isolate offset from input signal, so that it can later be extracted by a LPF and we have also proposed a mechanism to adjust the comparator's offset. A proto type chip fabricated in AMS 0.35um CMOS technology has demonstrated its effectiveness. With 23 comparators tested, all of their offset voltages are brought down to below 0.8mV, while its initial value can be as high as above 20mV.

This technique is further developed and applied to a 6 bit 500MHz flash ADC design, which has been implemented in IBM 0.13um CMOS technology. The 63 fully dynamic comparators used in this 6 bit flash ADC are background calibrated in a serial manner, where a general control scheme is proposed. To optimize the calibration technique for use in such a system, SAR search algorithm is adopted for calibration of each comparator, instead of the linear search algorithm used initially. Simulation result has shown that the flash ADC, including T&H circuit, resistor ladder and encoder, consumes only 9.5mW of power running at 500MHz.

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List of Abbreviations

ADC	Analog to digital converter
CMFB	Common mode feedback
CMOS	Complementary metal oxide semiconductor
DAC	Digital to analog converter
DEMUX	Demultiplexer
DFF	D flip flop
DNL	Differential nonlinearity error
ENOB	Effective number of bits
FIR	Finite impulse response
INL	Integral nonlinearity error
FoM	Figure of merit
LPF	Low pass filter
LSB	Least significant bit
MOS	Metal oxide semiconductor
MUX	Multiplexer
OTA	Over transconductance amplifier
ROM	Read-only memory
SAR	Successive approximation registers

SNR	Signal to noise ratio
SNDR	Signal to noise plus distortion ratio
T&H	Track and hold
UWB	Ultra wide band

Chapter 1 Introduction

Over the years, development of digital integrated circuit has closely followed Moore's Law. As a result, transistor size has greatly shrunk and the speed of digital circuit has been exponentially increased. This trend, which still continues today, widens the gap between the digital circuit and its analog counterpart, for which the technology advance is not as beneficial. On one hand, there exists very high speed digital circuit with its ever growing processing power and efficiency. On the other hand, analog circuit struggles and largely fails to keep pace. To make matter worse, most of systems need to communicate with the real analog world at some point, so that analog interface circuit, although usually being the limiting factor in the whole system, is still indispensable. It is thus desirable to push the analog/digital boundary closer to the real world, where the system can take better advantage of the high speed digital circuit.

This trend puts high pressure on analog circuit designers to develop very high speed interface circuits, namely, analog to digital and digital to analog converters (ADCs and DACs) that can keep up with the digital world yet still maintains other desirable attributes like low power consumption and small chip area. With shrinking of available power

supply voltage and a number of new issues brought about by greatly reduced transistor size, this task seems to be more daunting than ever.

Particularly, there is a category of applications including disk read channel, UWB receiver and wired or wireless communication system demanding for high speed (above 500MHz) and comparatively low resolution (4 to 8 bits) ADCs. Among various ADC architectures, flash ADC suits this purpose favorably because of its inherent parallel thus very fast structure and low signal latency. Also, the large area overhead that comes with this structure is less severe when put in a low resolution context. Therefore, it is of great interest to develop high speed and low power flash ADC that can be integrated in these systems.

Although requirements for different applications may have emphasis on different aspects, the ultimate goal is always to push for higher performance at lower power consumption. To achieve this goal, researchers have come a long way from the conventional structure and developed various flash ADC designs, some of which will be discussed in Chapter 2. The most critical component in a flash ADC is the comparator, where a bunch of techniques are proposed to mitigate or circumvent the inherit tradeoff

between performance and accuracy. Comparator calibration techniques seem to be fairly effective in this aspect. By leaving the problem to after the chip's fabrication, where non idealities are determined and can be measured, rather than in the design phase, where they can only be described in a statistical sense, these techniques are more effiecient so as to avoid large overhead that usually results in large power consumption. They have the potential to give designers more freedom during the circuit design phase.

This work focuses on designing of a flash ADC that utilizes fully dynamic comparators, which is largely made possible by incorporating a background comparator offset calibration technique developed earlier. The resulted benefit is much relieved frontend design and significantly less power consumption, comparing to more conventional designs. This thesis is organized as follows. Chapter 2 gives an overview of existing flash ADC designs, where their performances are compared. Chapter 3 introduces a proposed background comparator calibration technique with circuit implementation in AMS 0.35um CMOS process and corresponding measurement results. Chapter 4 gives detailed account of a flash ADC design that utilizes fully dynamic comparators implemented in IBM 0.13um CMOS technology, together with its calibration and control circuits, while the last chapter concludes this work.

Chapter 2 Overview of Flash ADC Designs

To boost speed and reduce power consumption, in the mean time adapt to more advanced technology, the design of flash ADC has evolved from conventional structure to more complicated structures that incorporate techniques including resistive averaging, interpolation and sophisticated calibration. This chapter discusses several published flash ADC designs implemented in various technologies. Comparison of their performances is made in the hope of revealing the ongoing trend in this aspect.

2.1 Conventional Flash ADC

A conventional flash ADC (figure 2.1) has a track and hold (T&H) frontend, a comparator array and a digital decoder that converts the thermal meter code produced by the comparators to valid N bit binary output. Also, a resistor ladder is used to generate required reference voltage at the input of each comparator. The parallel structure ensures a high operation speed and minimized conversion delay. The necessity of a T&H circuit is mandated by the fact that due to clock delay, individual comparator may sample the

same input at different instants, causing severe problems under certain circumstances. However, adding an additional frontend stage that can hold the input while being sampled by the comparator array mitigates this problem and relaxes layout requirement of clock route.

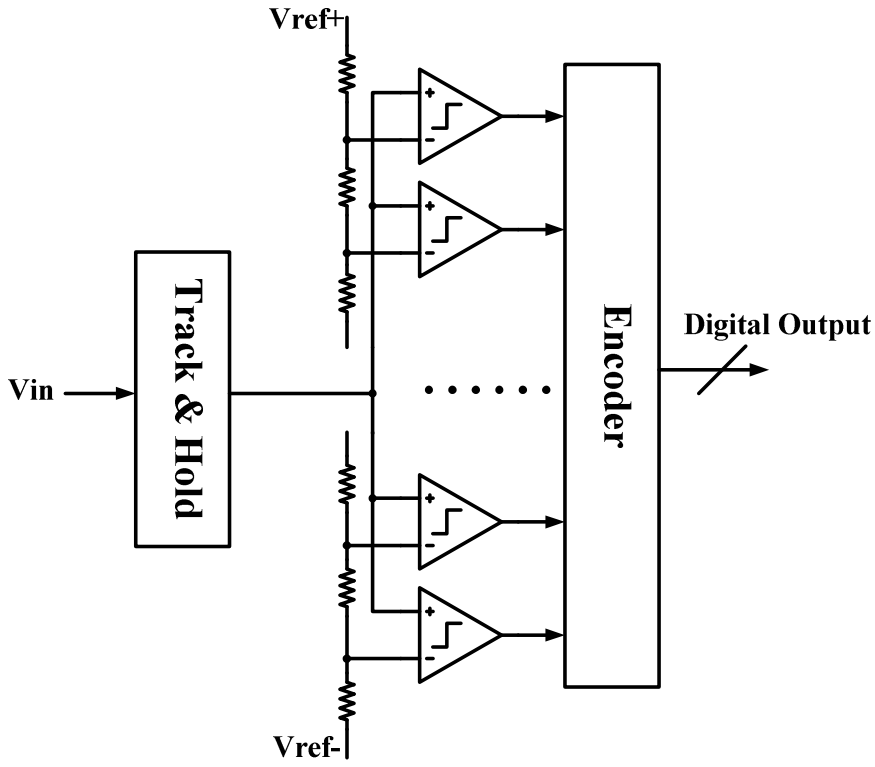

Figure 2.1 Typical conventional flash ADC design.

Evidently, comparator plays a very crucial part in this structure. Not only its speed determines the highest sampling rate achievable by the ADC, but also, its key

characteristics will largely affect the overall dynamic and static performance, especially note that the offset of each comparator directly contributes to DNL and INL, two very important performance indicators.

Assuming the comparator employs preamplifiers, as is often necessary for high speed flash ADC implemented in deep submicron technology, the overall offset is dominated by the first stage preamplifier, which can be approximated by the following equation [1],

$$\sigma_{OFFSET} = \frac{A_{VT}}{\sqrt{WL}} \tag{2.1}$$

where WL is the gate size of input transistor and A_{VT} is a process determined factor. Based on this equation, the only way to reduce offset variation is to increase the input transistor size. Once the size is determined, load capacitance of the T&H circuit can be subsequently estimated, which leads to its transconductance and power consumption. Also, kickback noise and different feedforward and feedback routes from the comparator to its reference input, along with mismatch considerations, determine the total resistance of the resistor ladder, which usually contributes a considerable portion of power consumption. Therefore, the comparator design assumes such a pivotal position in conventional flash ADC design that its importance can hardly be overstated.

2.2 Flash ADC Designs with Resistive Averaging and Interpolation

The simple tradeoff discussed above in the conventional structure is no longer an optimal or even viable solution for designs in deep sub micron technologies because of significantly reduced supply voltage and paramount need of low power design. If one still attempts to achieve the desired offset by simply increasing the transistor size, the likely result would be unacceptable power consumption and (or) chip area, as discussed above. It is easily identified that these tradeoffs primarily originate from input referred offset voltage prescribed by equation 2.1. Consequently, researchers have put a lot of efforts on circumventing this offset issue.

Kattmann and Barrow [2] proposed a technique to address this very problem. In the configuration shown in figure 2.2, all the preamplifiers are connected together by a resistive network. Thus the originally uncorrelated input offsets contributed by individual preamplifiers are correlated and their effect is averaged. In other words, their input referred offset contributions are reduced. The reduction factor (as an indication of its effectiveness) is determined by the ratio between the unit resistor R_2 in the resistive network and the load resistance R_1. This scheme, though proved to be effective, suffered

from several serious drawbacks. First of all, as the edge of the resistive network is not properly terminated, preamplifiers at both ends tend to cause a large INL. Moreover, the reduction of offset, i.e. the reduction of input transistor size, is still more or less limited.

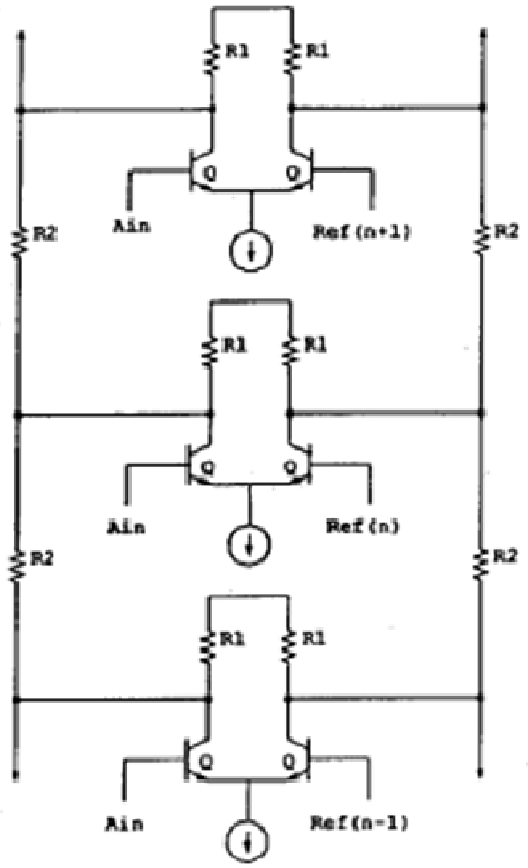

Figure 2.2 Resistive averaging [2].

Figure 2.3 shows another technique called interpolation [3], which is conceived from a totally different point of view. It aims to reduce the number of preamplifiers needed to

achieve the same number of bits at the ADC output. The comparators used in a flash ADC are essentially a bunch of zero crossing points, the function of which can be abstracted to comparing of the input voltage to a certain reference. In this aspect, the physical existence of comparators are not essential, as long as corresponding zero crossing points can be created. Considering that outputs from preamplifiers are linear, this can be easily achieved. Figure 2.3 shows two pair of differential outputs from two preamplifiers [3]. V_{X1} *and* V_{Y1} form a zero crossing point at V_{r1} while V_{X2} and V_{Y2} form another zero crossing point at V_{r2}, these are two original zero crossing points produced by two physical preamplifiers A_1 and A_2. If one takes a look at V_{Y1} and V_{X2} (or V_{Y2} and V_{X1}), their difference produce an additional zero cross point at

$$V_m = (V_{r1}+V_{r2})/2 \tag{2.2}$$

which is the same as output from another preamplifier inserted in the middle of A1 and A2 with V_m as its reference. Therefore, by simply applying this technique, the number of preamplifiers required, which is 2 to the power of the number of bits, can at least be halved.

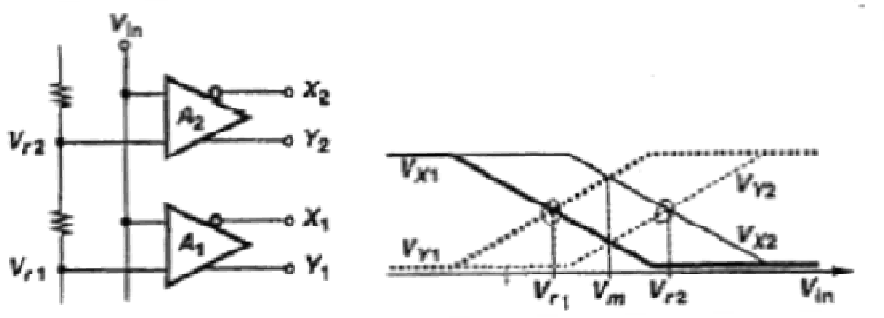

Figure 2.3 Interpolation [3].

Combining the two techniques together forms a more effective solution [4-7], as shown in figure 2.4. In this case, averaging resistors are in the mean time used as voltage divider so that even more zero crossing points can be created. To provide enough voltage gain while achieving high speed, there are usually multiple stages of preamplifiers involved and each stage is interpolated and averaged at its output. As a result of this powerful combination, the number of first stage preamplifiers needed is reduced by several times. For example, the 6 bit flash ADC shown in figure 2.4 [6] needs only 9 first stage preamplifiers, instead of 63 in the conventional structure. Although the resistive network still needs to be properly terminated so as to cause minimum distortion, it greatly relieves the requirement for the T&H circuit, whose g_m as well as power consumption can be accordingly minimized due to significantly less number of preamplifiers to drive.

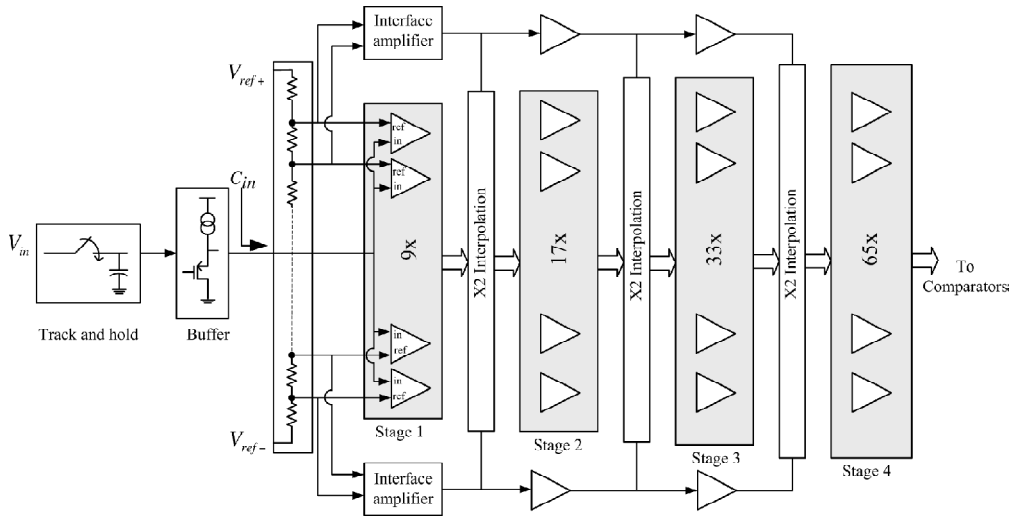

Figure 2.4 Preamplifier array with resistive averaging combined with interpolation [6].

Over the years, this combination of techniques has almost been pushed to its perfection by researchers around the world, but it is also limited in certain aspects. For one thing, the interpolation factor can only be so high that the outputs from adjacent preamplifiers do not exceed their output linear range. This is probably why most of these works choose a minimal interpolation factor of 2. For another, more importantly, this comparator structure with multi stage preamplifiers followed by a dynamic latch has its inherent disadvantages that restrict it from achieving high power efficiency, which will be discussed in the following paragraph.

One of the main reasons to add multi stage of preamplifiers is to suppress the large offset variation from the dynamic latch. The combined gain of all the stages has to be high enough so that when the latch's offset is referred back to the input, it becomes insignificant, as shown by equation 2.3,

$$\sigma_i = \frac{\sigma_{Latch}}{A_1 A_2 \cdots A_n} \tag{2.3}$$

where σ_i is latch offset variation referred back to the input of first stage and A_n is the gain of the n_{th} preamplifier. For the sake of power consumption, there should not be too many stages of preamplifiers as each stage consumes a considerable amount of power. However, if the number of stages is decreased, the gain of each stage has to be boosted so as to get the same overall gain while speed has to be maintained. This may lead to an even high power consumption in a single stage than multi stages of preamplifiers. Considering the simple preamplifier structure shown in figure 2.5, this would end up with an increase either in g_m of input transistor or load resistance R. Both are undesirable as larger g_m corresponds with larger current or *W/L* ratio, where larger R_1 may reduce the speed achievable and the effectiveness of averaging. In the end, the number of stages selected is a result of meticulous pondering over these complicated tradeoffs that involve

quite a number of factors. Nevertheless, the existence of several stages of preamplifiers results in a significant static power consumption.

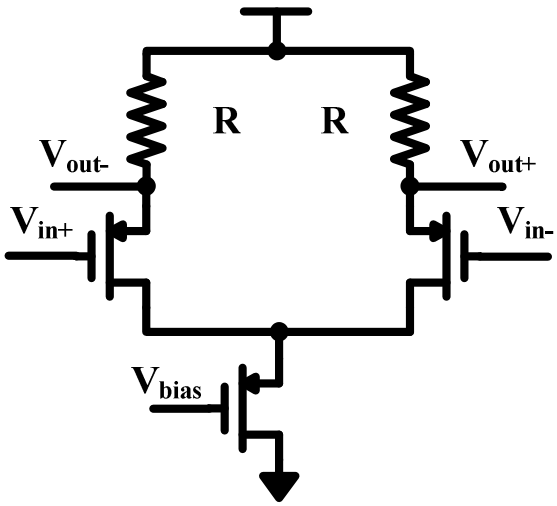

Figure 2.5 Preamplifier schematic.

Table 2.1 summarizes several published 6 bit flash ADC designs. The first four designs apply both interpolation and resistive averaging. And the last one [8] is a more conventional design list here for comparison. It can be seen that interpolation and resistive averaging do help to achieve a better result. Advance of technology also helps tremendously to reduce overall power consumption. However, it is worth noting that while analog part usually consumes more than half of the total power, preamplifiers take up at least 70% of power consumed by the analog part. In some sense, that huge amount

of power is mostly dedicated to tackle the offset problem, as the size of preamplifiers is prescribed by offset voltage.

Paper	Sampling Rate (MHz)	Supply voltage (V)	Process (um)	Total power (mw)	Analog power (mw)	Preamplifier power (mw)*
(Mic, 01)[4]	1300	3.3	0.35	545	272.5	233
(Aet, 02)[5]	1600	1.95(A) 2.35(D)	0.18	340	NA	NA
(Aym, 08)[6]	1600	1.5	0.13	180	126.3	106.1
(Kaz, 08)[7]	3500	0.9	0.09	98	46	32.3
(Koe) [8]	1000	3.3	0.35	700	535	304

Table 2.1 Summary of 6 bit flash ADC designs

*Calculated based on data given in paper

2.3 Flash ADC Designs with Calibration Techniques

Rather than averaging and interpolating to reduce the comparator offset, another possible solution is to find a way to calibrate it, which may get around the fundamental tradeoff shown in equation 2.1 in a more complete way, and in turn drastically reduce the size of preamplifiers [9], which is previously limited by linearity requirement. In certain cases, the use of preamplifiers can even be completely eliminated [10]. In [9], a foreground calibration scheme is proposed, which is illustrated in figure 2.6. During the calibration process, Ref[k], the ideal reference voltage of k_{th} stage, is attached to the

positive input of the preamplifier and the initial negative input is also set to Ref[k]. If the comparator does not have offset, the output, after passing an alternating amplifier A, should have a zero mean. If it is not the case, DFF in Digital Calibration Circuit will overflow and adjust the voltage at the negative input so as to compensate for the offset. The authors claim that by applying calibration, the required size of preamplifiers is reduced by 278 times, which means the load of T&H circuit is also reduce by 278 times. The flash ADC they designed consumes only 12mW of power at 800MHz sampling rate and though the data is not given directly, the analog part is estimated to have contributed only 3mW to total power consumption.

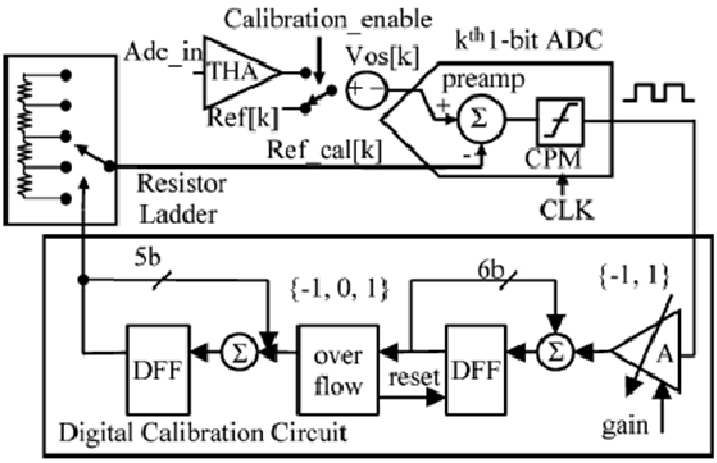

Figure 2.6 A comparator offset calibration scheme [9].

In [10], the authors proposed an even more aggressive foreground calibration technique that enables a 5 bit flash ADC design with almost complete dynamic components, even the need for reference ladder is eliminated by adopting built in reference. Also, folding technique is applied to halve the number of comparators needed.

Most of the benefits can be attributed to the fully dynamic comparator structure shown in figure 2.7. It is purposefully made imbalanced with a PMOS P4 acting as a MOS cap at the left side. The MOS cap can be sized in such a fashion that it causes an initial offset coarsely the same as the desired reference voltage. And N2 is used to finely calibrate that imbalance as well initial offset. An advantage of this structure is that it does not need a resistor ladder to generate the necessary reference voltage. Consequently, power consumption from the resistor ladder, which normally takes a considerable portion from the overall power, is removed.

While working at a sampling frequency of 1.75GS/s, this ADC consumes only 2.2mW of power and has a very low 50fJ/step FoM. Also, due to its dynamic nature, the total power consumption has a linear relationship with its sampling rate (figure 2.8),

which is similar to pure digital circuit and is highly desirable. From this impressive result we can see that improvement is huge as long as static power consumption is eliminated.

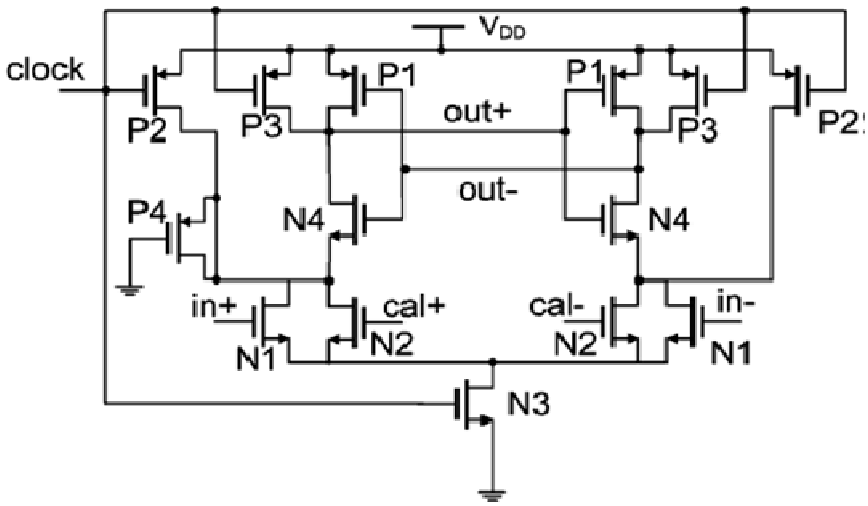

Figure 2.7 Imbalanced fully dynamic comparator [10].

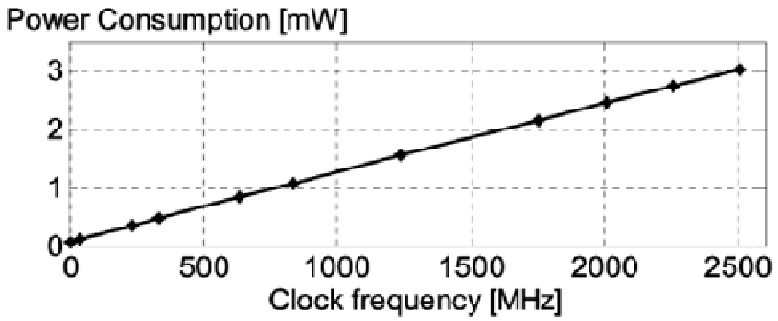

Figure 2.8 Power consumption versus clock frequency of fully dynamic flash ADC [10].

Paper	Sampling Rate (MHz)	Supply voltage (V)	Resolution (Bit)	Process (nm)	Total power (mw)
(Chu, 09)[9]	800	1.2	6	65	12
(Bob, 09)[10]	1750	1	5	90	2.2

Table 2.2 Summary of flash ADC with foreground calibration techniques

Table 2.2 summarizes performance of two ADC designs that use foreground calibration techniques. From Table 1.1 and Table 1.2, it can be concluded that calibration techniques generally achieve a better result comparing to interpolation and resistive averaging techniques. Even if one takes the more advanced processes into account, the power consumption is still one or two orders of magnitude less. However, they take additional calibration steps before the ADC can be put into use and once the calibration is done, it can no longer track the changes of conditions such as supply voltage, temperature and clock frequency. As pointed out in [10] and shown in figure 2.9, when the supply voltage or input common mode voltage changes with respect to the value at which the ADC is calibrated, its low frequency ENOB degrades. In certain applications, this can pose as a serious issue. If the operating point drifts far away from the optimal point, at which the flash ADC is calibrated, the overall performance of the whole system might deteriorate considerably due to the degradation of flash ADC performance. It is even

worse if the ADC in the mean time needs to run constantly and no time can be spared for occasionally recalibration. The price paid for maintaining a stable working environment can be huge.

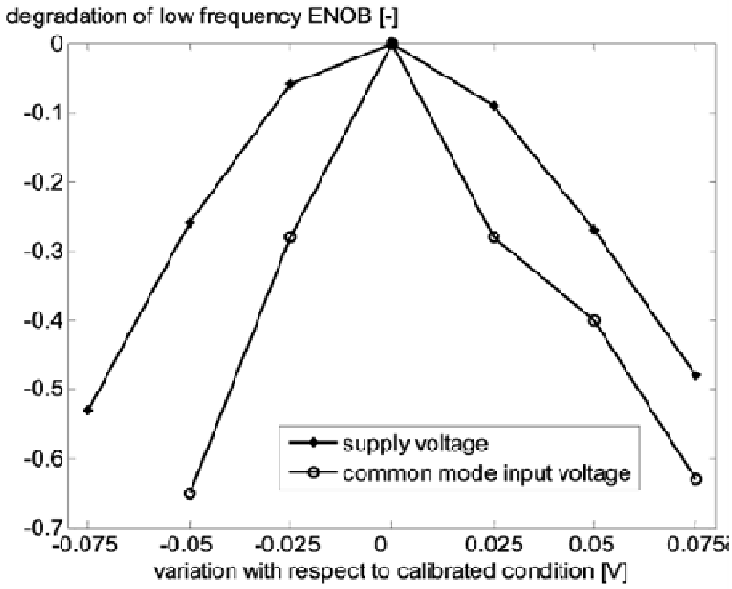

Figure 2.9 ENOB degradation of flash ADC with respect to supply voltage and input common mode voltage [10].

On the other hand, background calibration technique does not suffer from this problem. Due to its background nature, it will be able to adapt to environmental changes, as long as such changes can be compensated. The challenge lies in how the offset information can be extracted without interrupting the ADC's normal job. Moreover,

methods that can precisely calibrate the comparator offset without causing too much additional trouble should be developed. In [11], the authors resort to random chopping to achieve an averaging effect upon offset (figure 2.10). The input chopper S_1 and output chopper S_2 are controlled by the same random signal *r*. They claim that this technique, when used in a flash ADC, will improve dynamic performance because it will reduce the spurious tones while raising noise floor. However, as the offset is not further dealt with by calibration, it is unlikely to help with static performances in terms of DNL and INL. In [12], a background calibration technique also based on random chopping is proposed. Although a comprehensive analysis and abundant simulation results were given, no actual ADC was implemented, nor did the authors get into the details as how the comparator can be calibrated without causing much performance degradation.

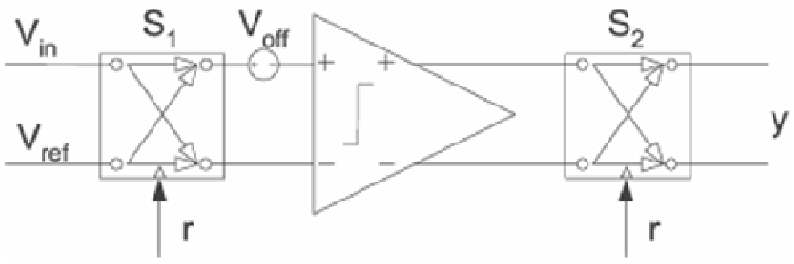

Figure 2.10 Comparator with random chopping [11].

Therefore, this work focuses on developing background comparator calibration technique and more importantly, its application to a low power and high speed flash ADC design.

Chapter 3 A Background Comparator Offset Calibration Technique

In this chapter, a background comparator offset calibration technique will be discussed in detail. This technique utilizes chopping to extract offset information without interrupting comparator's work. Also, the additional circuit developed to calibrate the comparator has negligible influence on its performance. A prototype chip was fabricated in AMS 0.35um CMOS technology and measurement result has demonstrated its effectiveness.

3.1 System Overview of the Proposed Background Comparator Offset Calibration Technique

To develop a background calibration technique, there are two major issues. One is to find a mechanism to extract the offset information in the background. The other is to make the comparator offset adjustable, preferably in a linearly way, within certain accuracy and range as mandated by the application. The rest is just to interface them and put them together in a feedback loop, where the offset will be automatically forced to

converge to a small value. The first issue will be discussed in the following section while the later will be introduced when it comes to circuit implementation.

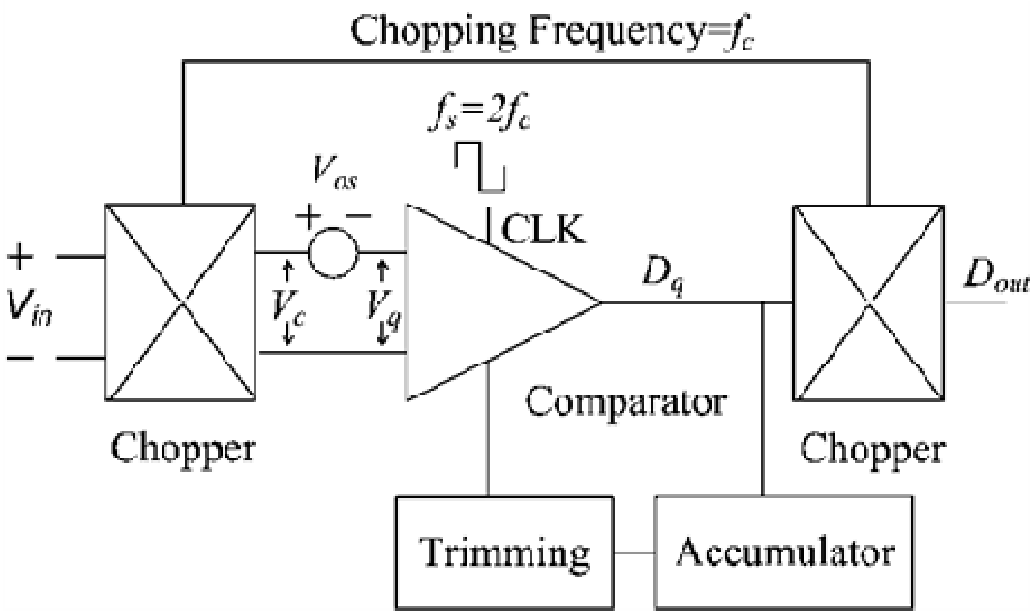

Figure 3.1 Comparator with proposed background calibration technique.

Figure 3.1 shows system architecture of the proposed technique. The background operation is guaranteed by the pair of choppers at both input and output. They are controlled by the same signal so they either pass the signal directly or invert both input and output at the same time. As a result, D_{out} will always be the same as the output of a

normal comparator. As will be discussed later, the comparator structure is slightly changed so that its offset can be adjusted. The accumulator is used to pick up the information of input referred offset voltage from D_q (see figure 3.1) and the trimming block is the interface between extraction and calibration, so that offset can be calibrated accordingly. Thus, when the comparator is at work, the input referred offset is forced by the feedback loop to converge at a low value determined by how precise it can be calibrated.

The key issue of this scheme is to effectively extract the offset. As in operational amplifier design, the first chopper at the comparator input moves the input signal V_{in}, which we assume originally expands from $-f_{in}$ to f_{in} in the frequency domain, to center around the chopping frequency f_c and its odd harmonicas. The relationship between V_c and V_{in} is determined by the following equations [13],

$$V_c(f) = \sum_{k=-\infty}^{+\infty} A_k V_{in}(f + k \cdot f_c) \tag{3.1}$$

$$A_k = \sin c(\frac{k}{2}) \tag{3.2}$$

where k is odd integer and f_c is the chopping frequency. Figure 3.2 shows the effect of input chopping. It might be of some interest to note that if chopping frequency f_c is

greater than input signal bandwidth f_{in}, the frequency band around dc will be void after chopping. So the input referred offset V_{os}, which occupies a very narrow frequency band near dc, is clearly separated from input signal in the frequency domain. Therefore, the signal bandwidth must be less than the chopping frequency for the technique to be effective.

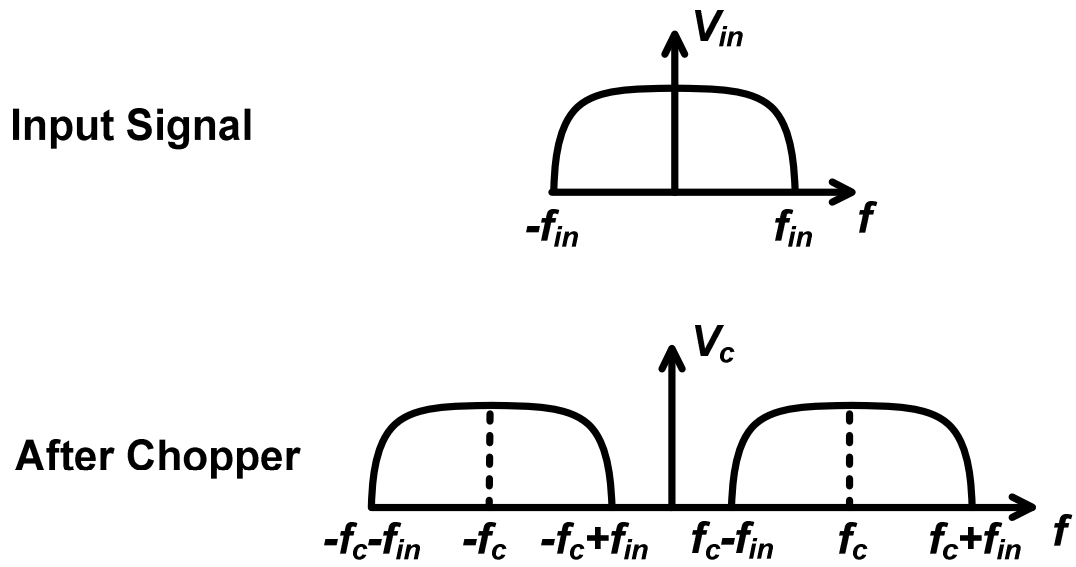

Figure 3.2 Effect of chopping for the input signal in the frequency domain.

Chopped input signal V_c, plus comparator input referred offset voltage V_{os}, is then quantized by the comparator. This process does two things. First, the signal is sampled by the comparator with clock frequency f_s that is purposely set to $2f_c$. From equation 3.1, the

input signal after chopper is centered around odd integer times of f_c, with the original signal bandwidth $f_{in} < f_c$. By sampling it at $2f_c$, the resulted signal would still be centered at odd times of f_c. Since $f_{in} < f_c$, it ensures no signal is aliased back to dc. Second, the nonlinear quantization takes place and transfers the analog input to digital output. From the amplitude spectrum of the output signal, it is found that the offset information is not spoiled by this process.

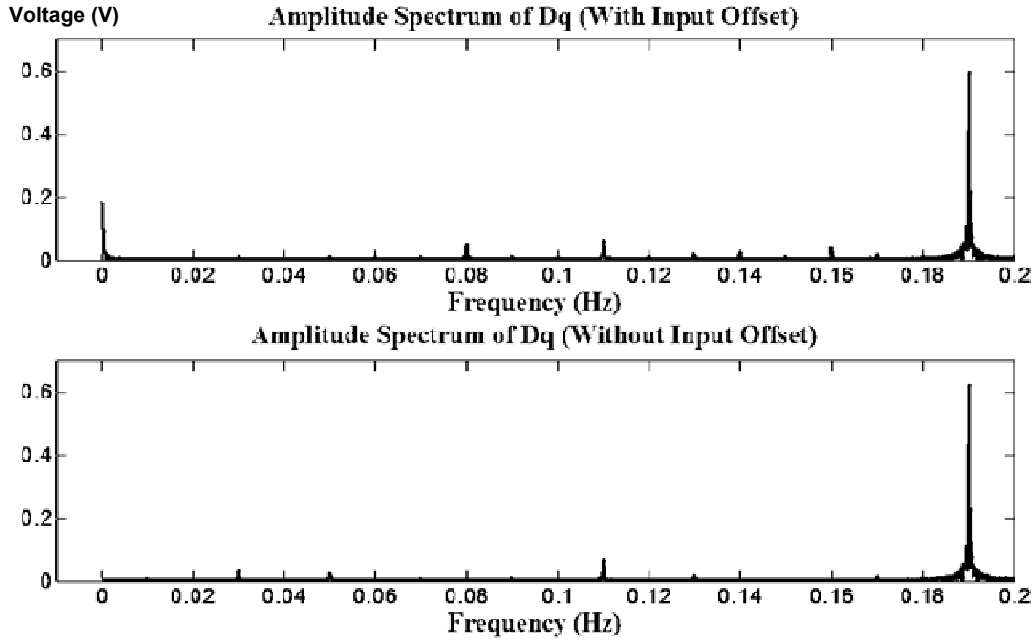

Figure 3.3 Amplitude spectrum of chopped comparator outputs with and without input offset voltage.

This can clearly be demonstrated in the frequency domain. Figure 3.3 shows amplitude spectrum of two comparator outputs with the same sine wave as the input, the only difference being one has and the other does not have input offset voltage. It is clearly seen that when the input referred offset is present (the upper graph), there is a spike at dc, which indicates offset voltage that sits around dc. Note that for the purpose of demonstration, the offset voltage is set to a comparatively large value in this simulation.

To retrieve offset information, the following stage needs to be a low pass filter (LPF), preferably with very low cut off frequency and high dc gain, because this LPF will eventually be put in a feedback loop, actual value of the input referred offset voltage is not important, as long as its sign is known. Based on this observation, a digital accumulator is selected to accomplish the task. By setting its output limits to N and $-N$ respectively, it will overflow whenever the output reaches either limit, and the direction it overflows indicates offset polarity. The accumulator can be regarded as a finite impulse response (FIR) digital LPF with the following system function

$$H(\omega) = \frac{1 - e^{-jN_s\omega}}{1 - e^{-j\omega}} \tag{3.3}$$

where N_s is the number of comparator output (the number of samples) accumulated before it overflows. From equation (3.3), we can see the dc gain, as well as the order of the FIR filter is determined by N_s. Figure 3.4 shows impulse response of a LPF with N_s= 1000.

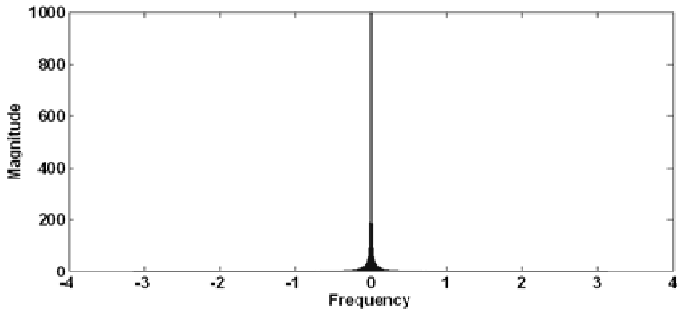

Figure 3.4 Impulse response of accumulator with N_s=1000.

This gives an interesting system property. Smaller offset generally ends up with larger N_s, as a larger number of samples needs to be averaged in order to pick the dc value out. For the system function of the FIR filter shown in equation (3.3), it means a larger dc gain and narrower cutoff frequency, which are both helpful to the signal to noise ratio (SNR). In that sense, the filter is adaptive so that it can still be effective even dealing with a small offset value. When N_s becomes very large, it approaches ideal accumulator that has the following system function

$$H(\omega)=\frac{1}{1-e^{-j\omega}} \tag{3.4}$$

In this extreme case, the gain of the ideal accumulator is infinite at dc.

Once the polarity of offset is known, the task of the following trimming stage is simple. As discussed earlier, it is essentially an interface circuit between the extraction part and calibration part. It does so by recording the number of overflow happened in the previous stage and according to the direction of each overflow, i.e. the sign of offset at that moment, it adjusts the comparator to compensate for it in a step by step manner, assume that the comparator can be adjusted linearly.

The last but not least is to actually make the comparator adjustable. While it is not going to be discussed in detail here, there are primarily two design issues involved. The first is how precise the comparator offset needs to be adjusted and the second is the calibration range. The former directly relates to the ADC that the comparator is applied to because the smallest calibration step should be a fraction of ADC's least significant bit (LSB). The calibration range, however, depends on the comparator's offset variation in a certain process, which is determined by its structure and transistor size. Assuming the variation can be described by Gaussian distribution, the calibration range needs to cover at least three times of the variation to ensure a high yield.

Once the components are connected together and feedback loop is formed, the comparator offset will diminish with the number of samples taken and eventually converges to the minimum calibration step. Figure 3.5 shows convergence behavior of the system with an initial offset voltage of 21mV, a calibration step of 1.8 mV and accumulator limit of 10. Random noise is also added before the input enters the comparator. The result shows that the comparator offset diminishes in an exponential way with respect to the number of samples and ends up fluctuating around the smallest step. From the figure, we can see that the last few steps take much more time than the first few steps.

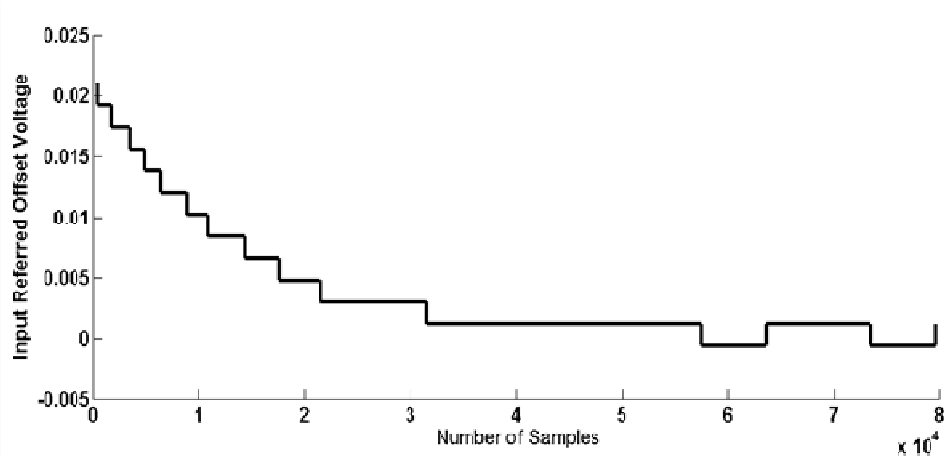

Figure 3.5 Convergence behavior of comparator offset with the calibration.

3.2 Circuit Implementation

A two stage comparator with a preamplifier followed by a fully dynamic latch [14] is used in this design, whose schematics are shown in figure 3.6. This kind of structure is also the choice of most flash ADC designs discussed earlier, except that they generally use multi stages of preamplifiers. The preamplifier has a certain amount of voltage gain to suppress the large offset from the dynamic latch, while the latch provides high speed comparison due to its positive feedback configuration. However, in this case, the preamplifier is not primarily employed to suppress offset, but rather for the convenience of adjusting its offset.

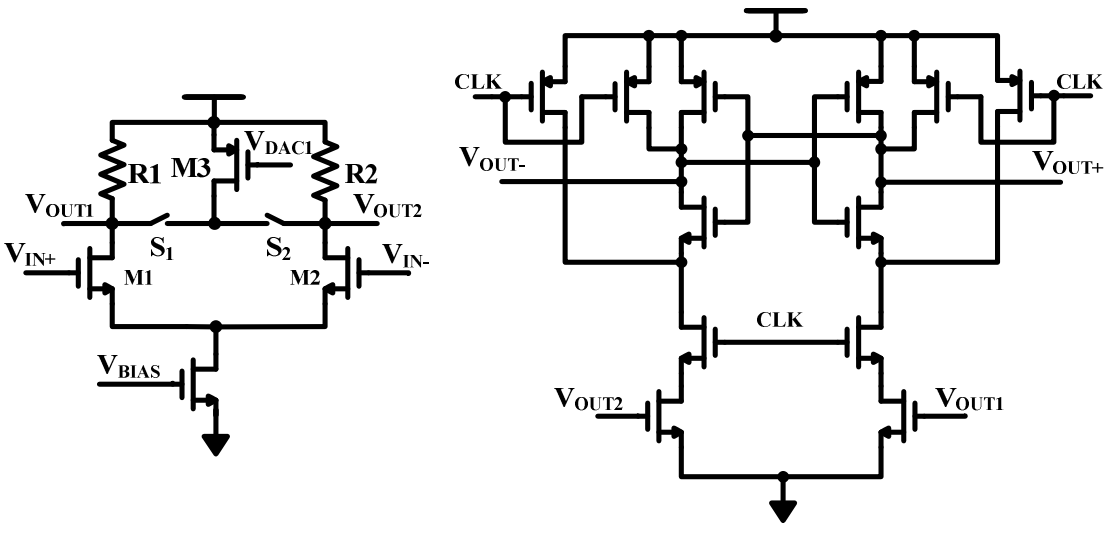

Figure 3.6 Two stage comparator with preamplifier followed by fully dynamic latch.

A PMOS transistor M3 acting as a controllable current source is inserted in parallel with two load resistors, with either S1 or S2 closed, so that the single transistor can compensate for offset in both directions. Using small signal approximation, the input referred offset is determined by the following equation

$$\Delta V_{OS} = \frac{I_3}{g_{m1,2}} \tag{3.5}$$

where I_3 is current injected by M3. The linear relationship between injected current and offset voltage shown by this equation is extremely desirable as it can be controlled in a straightforward and reliable way. The magnitude of this current is decided by a simple current output DAC, the output LSB of which, together with g_m of the input transistor, determines the LSB of offset calibration. In real application, g_m is determined by the bandwidth requirement for the preamplifier and we can easily set the LSB of DAC to achieve the desired minimal calibration step, which is set to around 0.5mV in our design. This method, with only two switches and a PMOS transistor, adds negligible load to the preamplifier and in the mean time provides linear and wide range offset calibration.

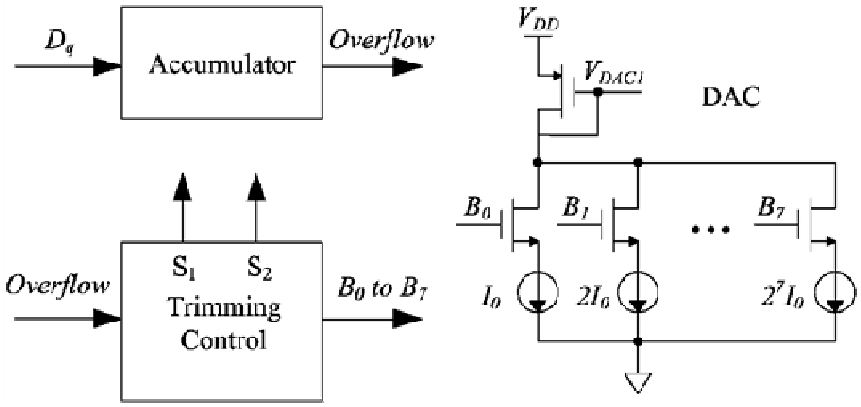

Figure 3.7 Block diagrams of the feedback loop.

Components that constitute the calibration circuit are shown in figure 3.7. As discussed earlier, an accumulator is used as a LPF to extract offset from comparator output. Its limit N is set to 64, 2 to the power of 6, so that it can be easily implemented with a 6 bit up/down counter. The trimming control part, acting as an interface between accumulator and the current DAC, records the number of overflow happened as well as the direction of each overflow and use that information to adjust DAC output current and switch control signal S1/S2. The DAC current output is binary coded and its output is controlled by NMOS switches. Each time overflow happens, its output current is increased or decreased by one LSB, depends on the direction. As the current is mirrored to M3 in the preamplifier, the offset is then calibrated by one LSB at a time. It is worth

noting that unlike a DAC used for data conversion, the output of this DAC does not have to be precise because it is in a feedback loop, the only concern is that its current output LSB should be restricted to below a certain limit in order to meet the calibration requirement. As a result, the design effort is greatly relieved and hence it can be realized with the simple structure as shown in figure 3.7.

For use in an ADC, the minimal calibration step should be set to a fraction of its LSB, and the calibration range should at least be able to cover 3 times of comparator offset variation to ensure a high yield. Together they will determine how many bits are needed for the trimming control circuit and DAC, as well as its LSB. The selection of accumulator limit involves tradeoff between convergence time and fluctuation after convergence. A smaller limit will certainly result in a faster convergence, but the residual offset will be bumpier. In addition, the limit must be large enough to make sure a strong averaging effect of the comparator output. Otherwise the probability of misjudgment will increase.

3.3 Measurement Results

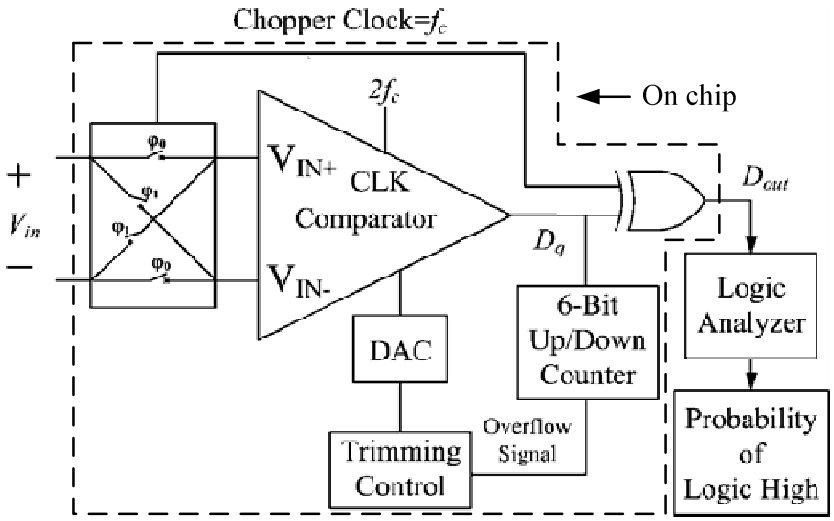

Figure 3.8 Configuration to measure comparator input referred offset voltage.

A prototype design has been fabricated in a 0.35μm standard CMOS process, and the test configuration shown in figure 3.8 is adapted to measure the comparator input referred offset voltage. Since output from the comparator is essentially a digital signal, the output chopper is implemented with a simple 2-input XOR gate.

Intuitively, measurement of input referred offset voltage can be achieved by the following process. Attach a fixed dc voltage V_{dc} at the comparator's negative input and

vary the voltage at the other input around V_{dc}. If this is an ideal comparator, there should be a point below which the output is logic high and above which the output is logic low at every sample. By definition of input referred offset voltage, it can be calculated by V_{dc} minus the input voltage value at that point.

However, due to noise of dc input signal, this point cannot be observed on oscilloscope. There is actually an input transition range within which output shows random behavior, bouncing between logic high and logic low with different samples. In this case, it is still possible to measure offset by using the same method as above. But instead of finding the point on oscilloscope, probability of output at a given dc input level is measured [15]. Since noise of dc input signal has a zero mean, what would happen at the point is that comparator output would have a 50% probability to be high. By taking a large number of samples (65536) at a given dc input level and calculating its probability, then varying the input signal accordingly and iterating the same process, the point that is conceptually equivalent to the point in the ideal case would be identified.

To test the effectiveness of proposed calibration technique, input offset voltage would be measured before and after calibration for comparison. A sine wave is injected for the

comparator to calibrate itself first, and then the input offset voltage is measured following the above method.

The sampling rate of the comparator is 10MHz, which makes chopping frequency 5MHz. The input sine wave has a frequency of 3.43MHz. Die photo of the test chip is shown in figure 3.9. Totally 23 comparators were tested. The histograms of their input referred offset voltages before and after calibration are shown in figure 3.10. The horizontal axis indicates the input referred offset voltage range in absolute terms and the vertical axis shows the number of comparators falls in that range. It is clearly shown that while the initial offset is as high as 25mV, after calibration, they are brought down to below 0.8mV.

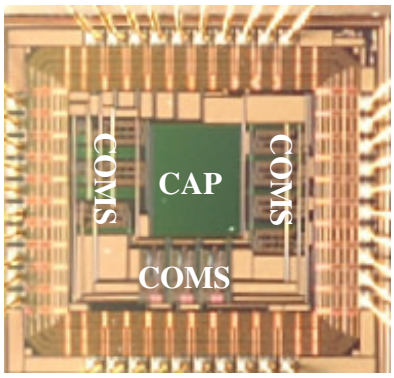

Figure 3.9 Die photo of the test chip.

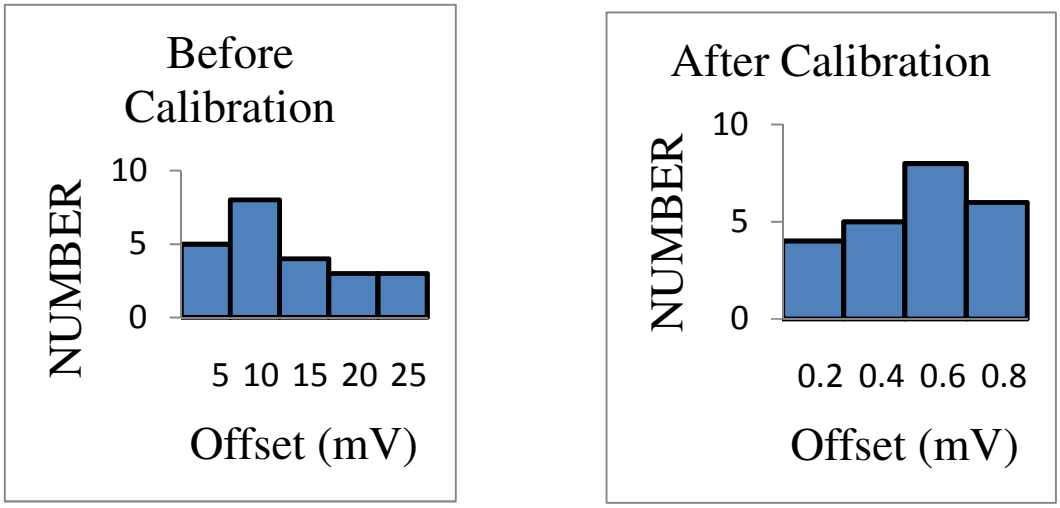

Figure 3.10 Histogram of comparator input referred offset voltage (absolute value) before and after calibration.

Chapter 4 Design of a 6 bit 500MHz Flash ADC Employing Fully Dynamic Comparators

As discussed in chapter 2, flash ADC designed with fully dynamic comparators shows a superior performance especially in terms of power consumption. Without multi stages of preamplifiers, large portion of analog power consumption can be eliminated. The limiting factor, however, is its large initial offset. Before it can be applied to a flash ADC, which has a stringent requirement for comparator offset, calibration techniques must be utilized to mitigate this problem. The background comparator offset calibration technique introduced in the previous chapter is tailored to suit the use on fully dynamic comparators here. With this technique, offset of each comparator is expected to be reduced to a fraction of the ADC's LSB and it would enable us to use small input transistor size that is limited by other issues rather than offset voltage. Thus the power consumed by comparators can be significantly reduced. The front end T&H circuit design would also benefit from this because lower capacitance and kickback noise is expected from the comparator array.

The major problem is to find a way to linearly adjust the fully dynamic comparator's offset voltage, while imposing minimal additional load to the comparator itself. This proves to be a hard task. Unlike the case with preamplifier that has a linear output range itself, where linear relation is easily obtained, the fully dynamic comparator operates by taking advantage of positive feedback and it is difficult to control it in a linear way. This, as will be shown in section 4.2, is solved by inserting binary coded MOS capacitor arrays to the critical nodes of the fully dynamic comparator. The use of fully dynamic comparators with calibration also imposes different requirements and tradeoffs from a more traditional flash ADC design. Needless to say, with 63 comparators to be calibrated, a general control scheme also needs to be designed, which involves generating additional clock signal, disabling and enabling calibration with a certain comparator and sharing some calibration components. Moreover, certain new issues have to be addressed with the T&H circuit.

This chapter will first show simulation results obtained from a system model to demonstrate its effectiveness and the rest will be dedicated to the detailed design of a 6 bit 500MHz flash ADC using IBM 0.13um CMOS technology.

4.1 System Model and Simulation

A 6 bit flash ADC system with background calibration is built with Matlab Simulink, which the structure of actual circuit design is based on. Major components of a 6-bit conventional flash ADC are 63 comparators. However, unlike conventional flash ADC, here each comparator is equipped with a background offset calibration block, as shown in figure 4.1 below.

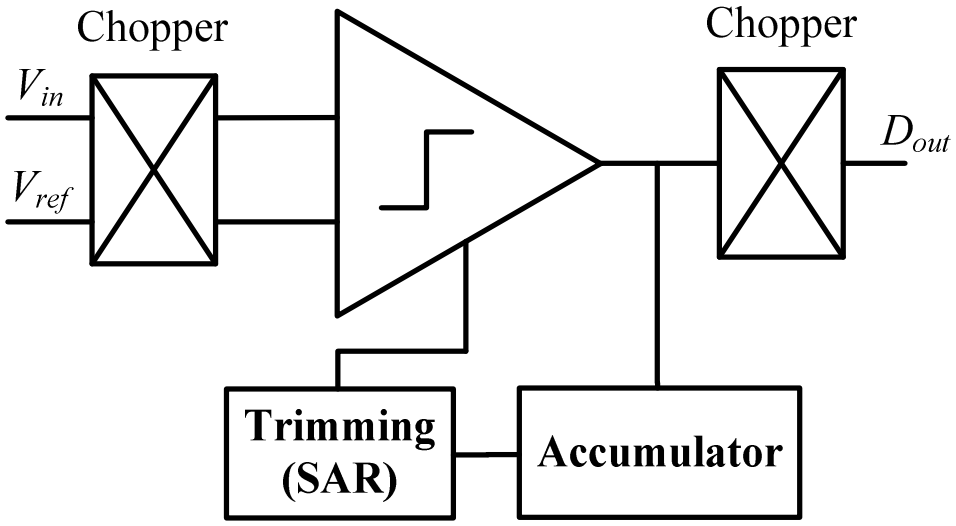

Figure 4.1 Comparator with calibration block

The principle of the background calibration block is essentially the same as that of the calibration scheme explained in Chapter 3. However, in the previous section, the offset is

calibrated by a linear search algorithm that change offset voltage in a step by step manner by the calibration LSB. This process may be optimized by utilizing successive approximation algorithm (SAR) [18]. By using SAR, the comparator is calibrated in a bit by bit manner and it works as follows.

At beginning, the most significant bit (MSB) value for the calibration is assumed, and the accumulator will then judge the polarity of the offset. If this proves to be too much, i.e. sign of the offset has been reversed, the MSB is unselected and the bit next to it is assumed. Otherwise if the offset is under compensated, i.e. sign of the offset has not changed, MSB is asserted and the bit next to it is assumed. This process is iterated to the last bit.

For an 8 bit calibration, the accumulator only needs to overflow 8 times to reach convergence with any initial offset value for SAR while the former method may need as many as 256 steps. At first glance, this may seem to be a great improvement to convergence time. However, convergence speed has not actually benefitted that much. As discussed in chapter 3, the convergence speed depends on residual offset and accumulator needs more time to pick the offset out when the residual is small. Therefore, majority of

calibration time is spent on the last few steps. Although SAR needs fewer steps to converge, the last several steps still take a long time because the residual offset is likely to be small. Under certain circumstances, like the offset is initially small, SAR may even take more steps than the previous method and converges slower. This point is illustrated by simulation results shown in figure 4.2 and figure 4.3. Figure 4.2 shows a comparator calibrated with SAR, the initial offset is 20mV, calibration LSB is 6 mV and it is a 5 bit calibration. Figure 4.3 shows a comparator calibrated using linear method with everything else set to be identical. In this case, SAR takes a larger number of samples, thus more time to finally converge.

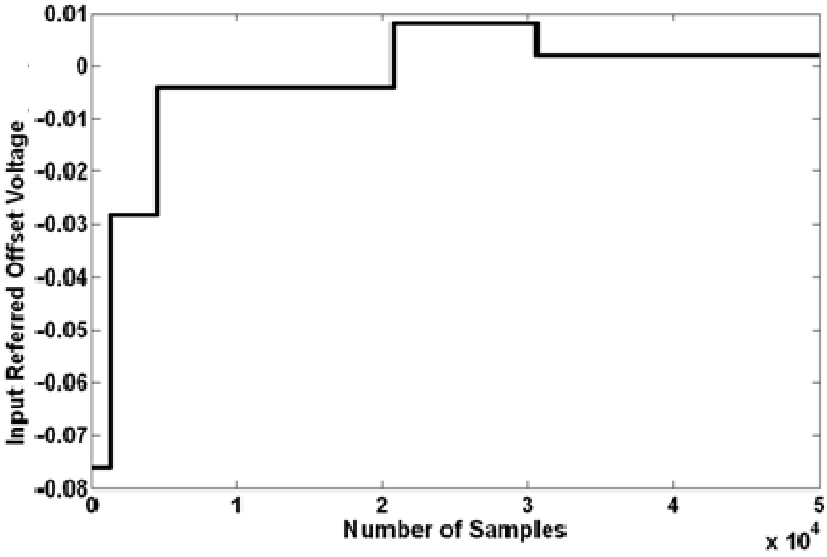

Figure 4.2 Convergence behavior of comparator offset with SAR algorithm.

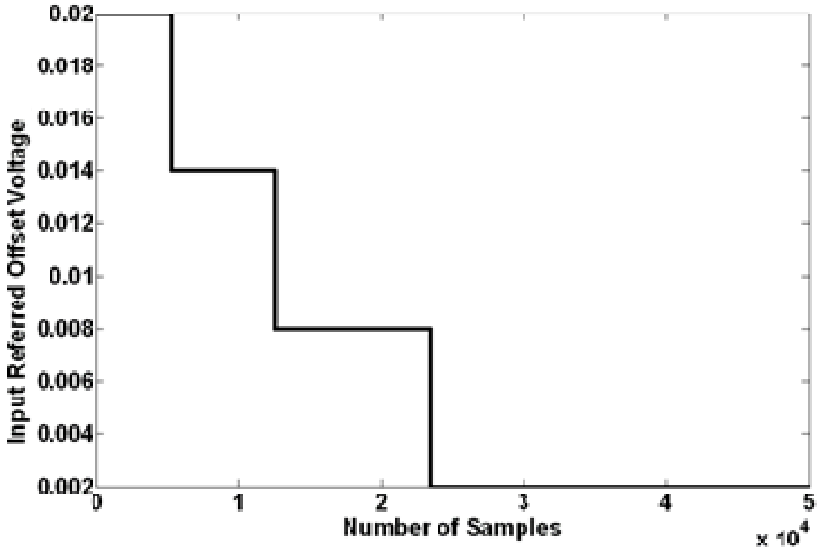

Figure 4.3 Convergence behavior of comparator offset with linear search algorithm.

As will be explained in Section 4.4, the selection of SAR instead of linear calibration logic here is due to practical circuit design constrains rather than convergence time considerations. With SAR, the indication of convergence can be simply obtained by monitoring its last bit where as in a linear search algorithm the convergence time is not easily estimated as it depends on various factors. With this critical information, all comparators can be calibrated in a series manner with a single set of accumulator shared among them.

As will be explained in Section 4.4, the selection of SAR instead of linear calibration logic here is due to practical circuit design constrains rather than convergence time considerations. With SAR, the indication of convergence can be simply obtained by monitoring its last bit where as in a linear search algorithm the convergence time is not easily estimated as it depends on various factors. With this critical information, all comparators can be calibrated in a series manner with a single set of accumulator shared among them.

The 6 bit flash ADC is modeled with 63 such comparators, each with its own background calibration block. The input offset is assumed to have a Gaussian (Normal) distribution, with zero mean and a 70mV variance, in accordance with Monte Carlo simulation result from comparator circuit implementation in Section 4.3. The calibration circuit has a LSB of 2mV and the SAR is of 8 bit, which ensures a ±256mV calibration range that covers ±3Δ of input offset distribution. The accumulator overflow limit is set to ±64, or 6 bit. Input signal is a 243MHz sine wave and the sampling rate is 500MHz, which makes the chopping frequency 250MHz. Simulation is first run with calibration blocks disabled so that offset at each comparator's input is not being calibrated. Figure

4.4 shows its static performance with measured DNL and INL. Dynamic performance is measured by PSD from its output. Resulted SNDR is 20.7687dB and ENOB is 3.1576. From figure 4.5, it can be seen that 3rd harmonica distortion is at -28.11dBFS.

When calibration blocks are enabled, only samples after 300000th are taken to obtain results, thus it is ensured that all comparators have already been properly calibrated. Not only drastic improvement is achieved with DNL and INL, as shown by figure 4.6, note that the scale of Y axis is different from figure 4.4. SNDR and ENOB has increased to 36.37dB and 5.75, respectively, as shown by figure 4.7. Now the 3rd harmonica distortion is at -53.45 dBFS.

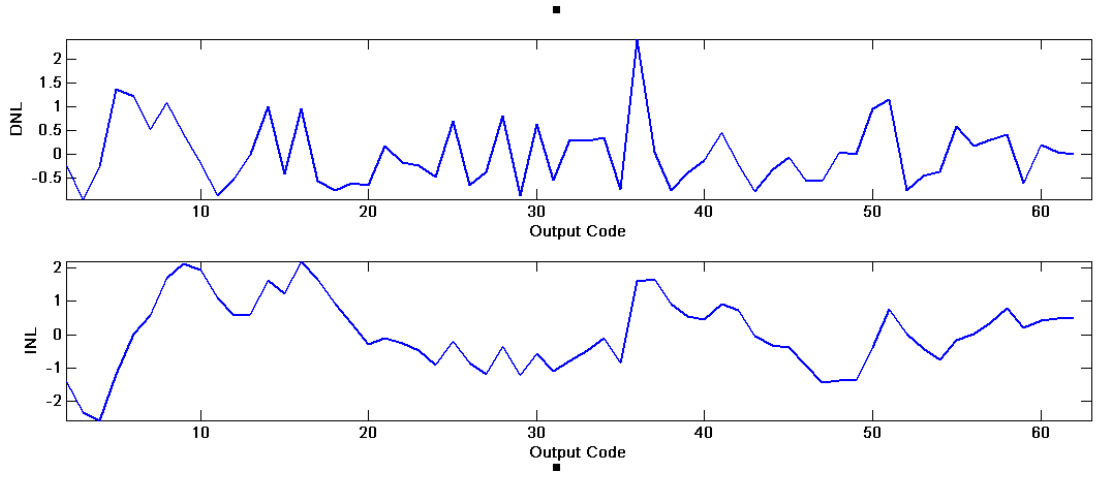

Figure 4.4 DNL and INL without calibration

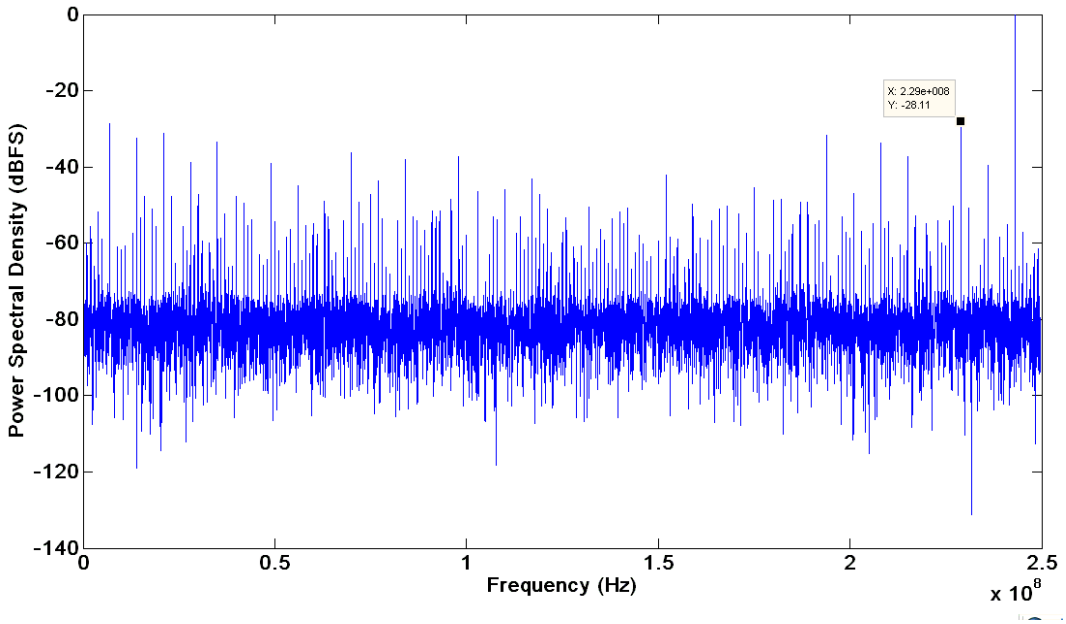

Figure 4.5 Output PSD without calibration

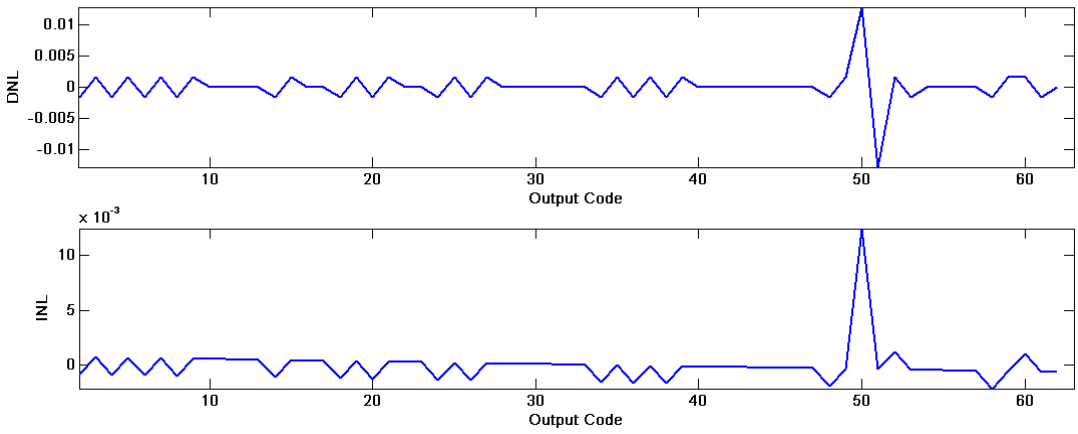

Figure 4.6 DNL and INL with calibration

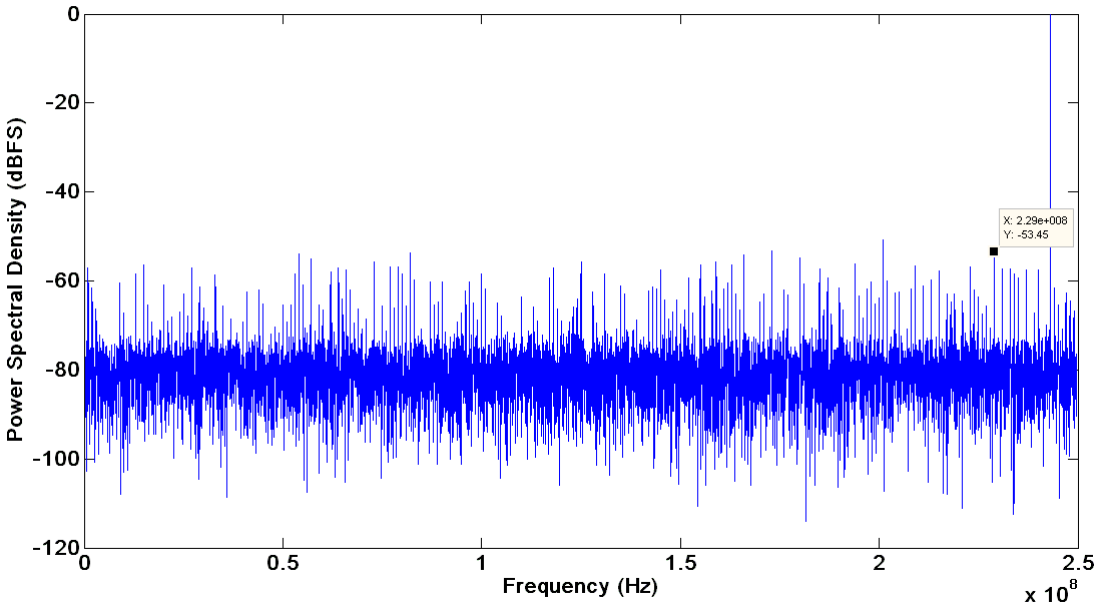

Figure 4.7 Output PSD with calibration

The system simulation result clearly demonstrates effectiveness of this background calibration scheme applied to a 6 bit flash ADC. The following sections within this chapter will discuss the implementation of such a system at circuit level in detail.

4.2 Track & Hold Circuit

T&H circuit is necessary for high speed flash ADC to avoid clock dispersion [3]. The high speed nature and moderate SNR requirement makes operational amplifier connected

in some sort of feedback configuration a less favorable solution even though they prevail in higher resolution architectures like pipelined ADC. To reach the desired speed, the OTA is expected to consume an unacceptable amount of power. Source follower, on the other hand, has some desirable attributes like low output resistance and high driving capability and is widely used in flash ADC designs [4], [6] and [7]. Source follower is therefore chosen for our design. To accommodate differential input, pseudo differential structure is implemented.

The first choice we have to make is between NMOS source follower and PMOS source follower. Although NMOS would seem to be a much better choice in terms of channel mobility, which in turn results in far superior power efficiency, the problem lies with body effect. In a single well process, using NMOS would introduce a large signal distortion due to body effect caused by large output swing. Therefore, PMOS source follower, as shown in figure 4.8, has to be used in spite of its inferior performance.

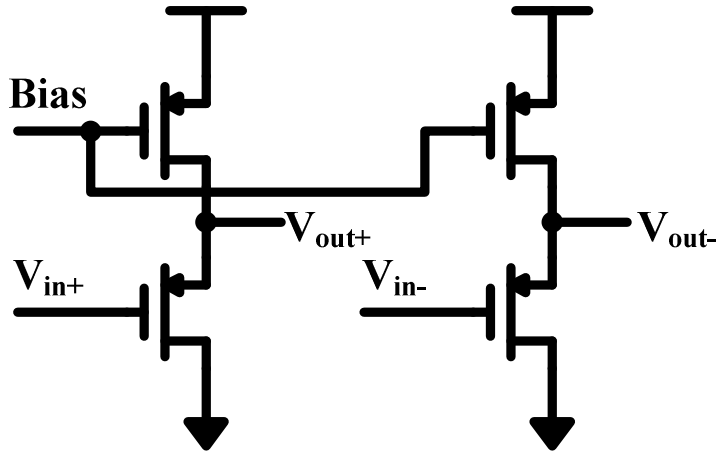

Figure 4.8 Pseudo differential PMOS source follower.

Another problem to be considered in this ADC design is the output common mode voltage. From figure 4.9, we can see that it is roughly calculated as the input common mode voltage plus gate source voltage of the input PMOS transistor. Due to process variation and mismatch, the output common mode cannot be precisely controlled and is expected to vary several tens of mVs, causing it to differ from common mode voltage of the reference. This is less likely an issue if preamplifiers are used in the first stage. As long as they have a reasonably large input linear range, the difference of common mode voltage between input signal and reference can be cancelled out and cause negligible error. However, the dynamic comparator we use here is highly nonlinear and the

difference will cause unwanted initial offset, which unfortunately cannot be corrected by calibration.

Common mode feedback circuit is the usual choice to bring this issue under control. However, conventional continuous common mode feedback (CMFB) technique [16] inevitably loads the output and simulations have revealed that it is very difficult to find a balance where output common mode voltage change can be tracked fast enough while CMFB does not load the circuit in a serious way. Therefore, a replica biasing scheme that consists of a feedback amplifier and a miniature source follower proportional to the output source followers is proposed (figure 4.8). V_{refc} is reference common mode voltage and V_{inc} is input common mode voltage. Because of feedback loop formed by a transconductance amplifier, the output common mode voltage is biased to be the same as reference common mode voltage at a given input common mode voltage. The good thing about this method is that reference common mode and input common mode voltage can be precisely controlled. The miniature source follower is sized to be 1/20 of the source followers used to drive the following stage, thus its power consumption is insignificant. This scheme has the advantage of not intruding the signal path and therefore does not put

any extra load to the output of source followers. A large capacitor is inserted between ground to *Bias* terminal, so as to reduce output feedback that may disturb the bias point.

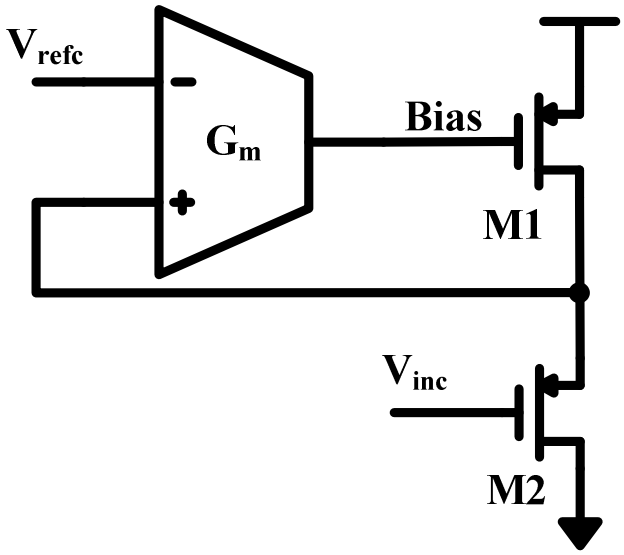

Figure 4.9 Replica biasing for the source follower.

The transconductance amplifier employs a folded cascode structure to obtain high gain. The feedback loop is actually formed by both the amplifier and PMOS transistor M1. Because the application here has virtually no requirement for bandwidth, the amplifier is designed to consume minimal power and no Miller compensation is needed. Instead, a large cap is inserted between *Bias* and ground to make the first pole dominant so as to solve the stability problem.

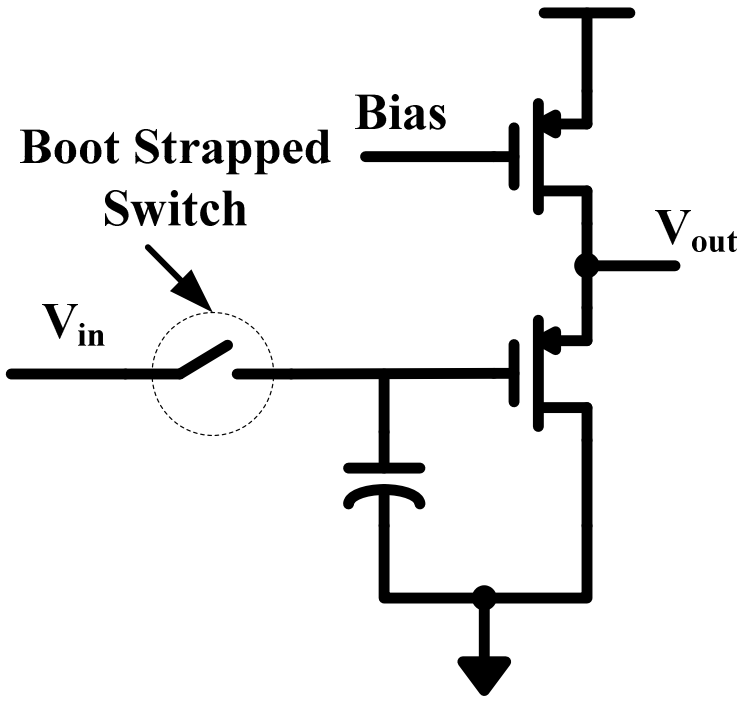

Figure 4.10 Source follower with sampling switch and capacitor.

The pseudo source followers are preceded by a pair switches and sampling caps to form the complete T&H circuit. The single ended version is shown in figure 4.10 for simplicity. The designed input range is 1V V_{pp} differential and the common mode is set close to 250mV. The output range is therefore 1V V_{pp} as well, because the gain of source follower is close to one. The output common mode voltage is raised by about a transistor threshold V_T, to 750mV. Each sampling switch needs to accommodate an input that

ranges from 0 to 500mV and a simple NMOS or transmission gate switch would induce a large signal dependent distortion. So a constant V_{gs} bootstrapped switch proposed by A.M. Abo and P.R. Gray in [17] is adapted here. In simulation, the proposed T&H circuit achieves a 61.59 dBc 3rd harmonica distortion with a 243 MHz input sine wave sampled at 500 MHz, as shown in figure 4.11.

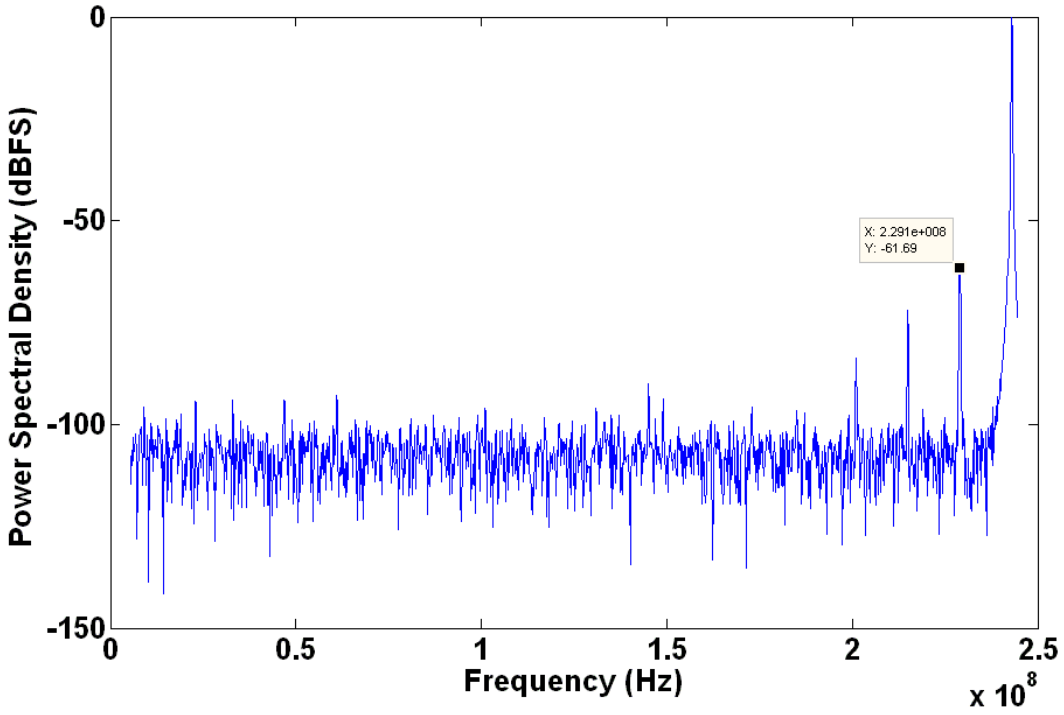

Figure 4.11Simulated output power spectral density of a 243MHz sine wave sampled by proposed T&H circuit at 500MHz.

4.3 Fully Dynamic Comparator and Calibration

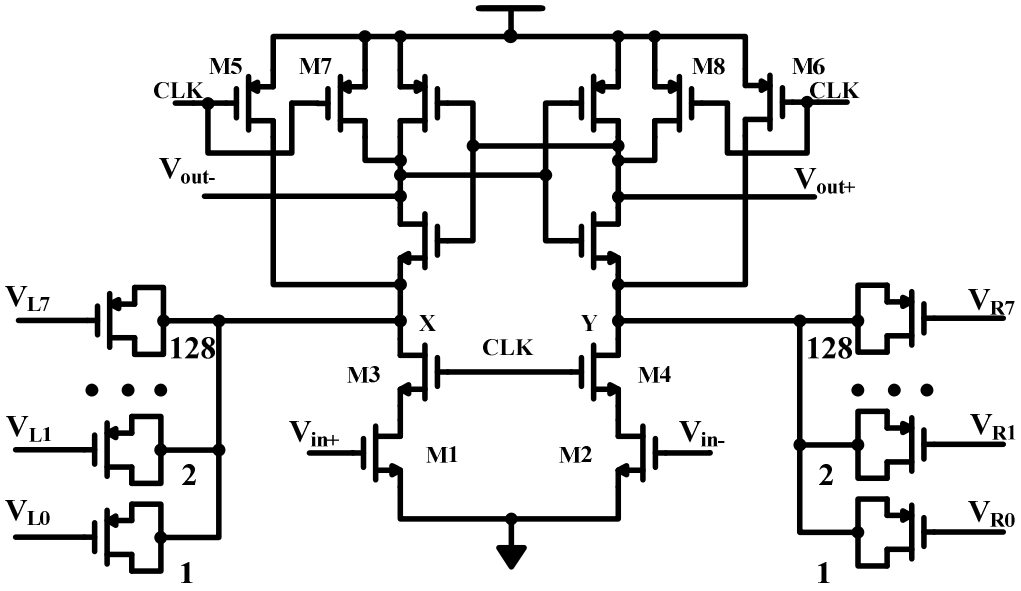

Figure 4.12 Fully dynamic comparator with MOS cap array.

Figure 4.12 demonstrates the comparator topology used in our design. Let us ignore the MOS cap array on both sides for the moment and focus on operation of the comparator. When the *CLK* signal is low, M3 and M4 are off and M5, M6, M7 and M8 are on. The output nodes and node X and Y will be charged to supply voltage. When the *CLK* becomes high, M3 and M4 are on, while M5, M6, M7 and M8 are off. Node X and Y will be discharged. Depending on the value of V_{in+} and V_{in-}, one node will be

discharged at a faster speed and then the comparator enters regeneration phase, where one output node will be pushed up to supply voltage and the other pulled down to ground. Figure 4.13 shows how the voltages at output nodes change at different phases within a complete clock cycle. Note that the comparator output is only valid during less than half of a clock period. This is undesirable as it significantly reduces processing time of the following stage and increases the probability of error. To solve this, a SR latch can be added to the comparator output so that the valid output is kept for almost one whole clock period, as shown in figure 4.14.

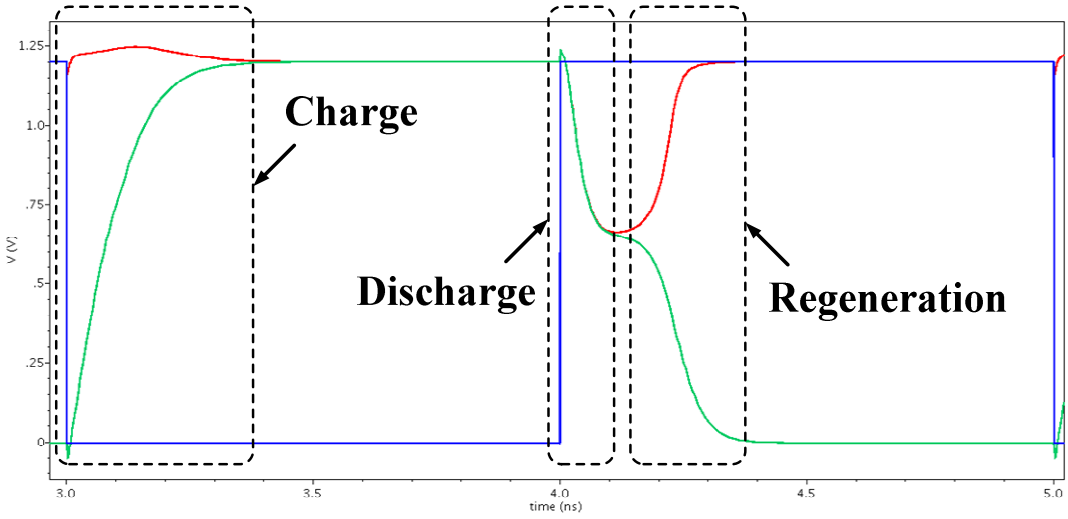

Figure 4.13 Comparator output voltage at different phases within one clock cycle.

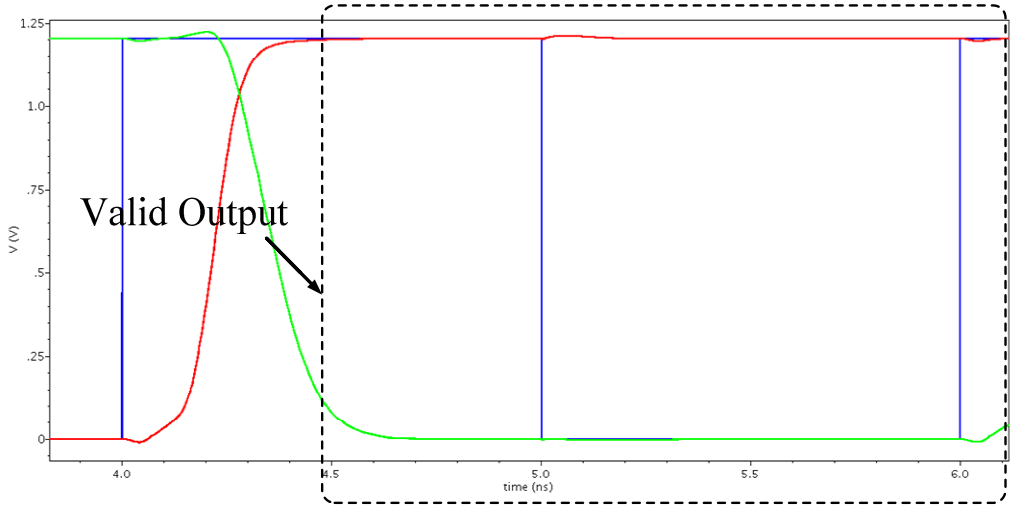

Figure 4.14 Comparator output with a SR latch.

As we do not use preamplifier here, if the same current injection concept as the one developed in the previous chapter is applied here, we would not have enjoyed the same linear relation between injected current and offset shift as in the two stage topology. Because this structure does not have a linear output region, the offset shift would have a non linear relationship with injected current and that makes control of calibration very difficult. This point is also proved by simulation results. To obtain the linearity, we have adopted a technique proposed in [18] for a different fully dynamic comparator structure but nevertheless shows similar results here.

The idea is to unbalance the capacitance at node X and Y as shown in figure 4.12 so that zero cross point is shifted. This can be achieved by inserting an array of PMOS caps at node X and Y and changing the control signal V_{RX} and V_{LX}. If V_{RX} and V_{LX} are both high, then node X and Y would see the same amount of parasitic capacitance and the comparator is balanced. If one signal with V_{RX} or V_{LX} is low, a channel would exist in the PMOS transistor, thus there is a capacitance difference ΔC caused by the channel charge. And shift of offset ΔV could be described by the following equation

$$\Delta V = \frac{I_D}{g_{m1,2}} \frac{\Delta C}{C_T} \tag{4.1}$$

where I_D and $g_{m1,2}$ are average current and transconductance of M1 and M2 during regeneration and C_T is the nominal total balanced capacitance at node X and Y. So this is a roughly linearly relation between the capacitance difference and offset shift, and binary sized PMOS transistors are placed symmetrically on both sides. The calibration can be done by digitally changing the control signal V_{RX} and V_{LX}, which is similar to DAC plus current source method developed in the previous chapter. The smallest MOS cap would determine the LSB of calibration, while the total capacitance offered would determine the calibration range.

We use 8 bit of binary coded MOS cap because of large offset variation shown by this particular comparator structure. Monte-Carlo simulation has demonstrated that with the transistor sizes we have chosen, standard variation of its offset is around 70mV. To ensure a high yield, the calibration range should be able to accommodate at least 3 times of that variation, roughly 200mV, on both positive and negative sides. Also, by simulation we have found that the lowest calibration step caused by the smallest PMOS cap is around 0.8mV. Therefore an 8 bit calibration circuit would have a 200mV calibration range. The penalty of this technique is that it increases load capacitance at node X and Y, thus sizes of M1, M2, M3, M4, M5 and M6 are increased accordingly. Increased sizes of M1 and M2 would cause the load of T&H circuit to increase as well, hence its power consumption. Also more kick noise is expected from the comparator array. As transistors M3 to M8 are driven by the clock driver, more power would also be needed from it.

The most important reason to adapt SAR logic is that the calibration is easily controlled with SAR. As shown in previous chapter, the total calibration time depends on initial offset voltage as well as other factors like frequency and amplitude of input signal. Thus, it is hard to determine whether offset has converged by timing the circuit. This is

especially true for the linear search method. If we assume the worst case for each comparator, for an 8 bit calibration we have to wait for 256 overflows. It is extremely time consuming if offset is initially low and has already converged within the first few steps. For a 6 bit flash ADC with 63 comparators calibrated in a serial fashion, this amount of time wastage is simply unacceptable.

However, things are much easier with SAR. As soon as the last bit is judged, we can move on to the next comparator and do not have to care about various conditions that could affect calibration time. Implementation of SAR logic needs a few D flip flops (DFFs). The SAR logic circuit used in the design is shown in figure 4.15 [19]. In this design, the *Q* output of last DFF in the upper row could be used as an indication signal for end of calibration because *Q* will only become high after the last bit is judged. We use two sets of this kind of SAR logic for each comparator, which has two sets of MOS cap arrays.

For the purpose of background offset extraction, two pairs of choppers are needed at the input of the comparator, as the input is differential. Each comparator in this flash ADC must have its own dedicated SAR logic circuit, which stores the calibration data

after it is done. However, the accumulator that used for extraction can be shared by 63 comparators, and this can easily be arranged by using multiplexers and demultiplexers. The system level design will be discussed more in the following section, while the block diagram for each comparator unit is shown in figure 4.16, which seems to have added a number of peripheral circuits, the function which will be discussed in the following paragraph.

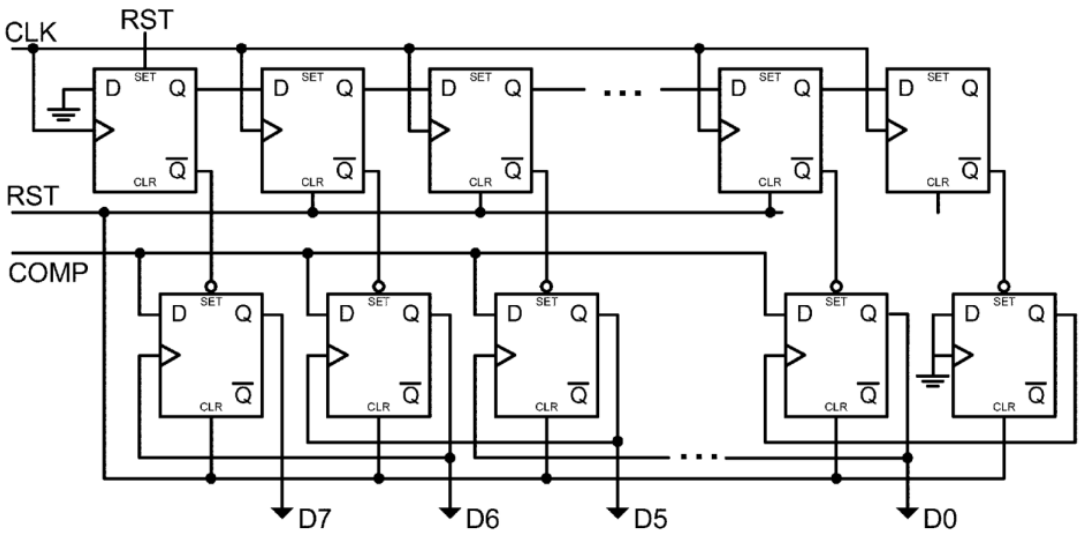

Figure 4.15 Schematic of SAR logic [19].

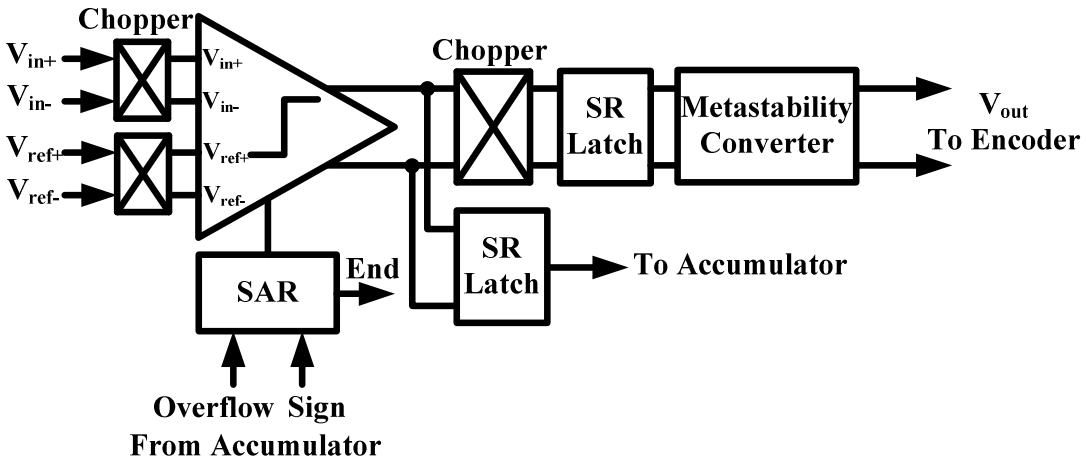

Figure 4.16 Comparator with circuits for calibration.

SAR logic takes two signals from accumulator. *Overflow* signal is a pulse that indicates an overflow has just happened and *Sign* is a logic input that indicates the direction of the overflow. *Overflow* is hooked up with *CLK* of the SAR logic circuit, while *Sign* is connected to *COMP*. So each time when an *Overflow* pulse arrives, it asserts or cancels the previous assumed bit based on *Sign* and moves on to assume the next bit. This process will repeat itself until the last bit is reached. In the case, the SAR logic outputs an *End* pulse to the control circuit to indicate the end of this comparator's calibration.

SR latch can maintain the output when both of its S and R input are high. Thus it will keep the output of the comparator valid for almost a fully clock cycle. The first SR latch is connected to the output before the second chopper. Its output is the input of the accumulator as it needs to average the chopped output signal rather than normal comparator output. This can also be understood by observing that the accumulator, acting as a digital LPF, can only filter out the offset with input signal moved to a higher frequency.

As can be seen from figure 4.16, output chopper is put between comparator output and the input of the second latch rather than at the output of the second latch. The reason to do so can be illustrated by simulation result shown in figure 4.17. The upper pair of differential output shows what happens when you put the chopper at the output of the SR latch. During the charge phase, SR latch will maintain the previous output until the next regeneration phase. If chopper changes direction during that time, the final output will accordingly be reversed. However, if the position of chopper is arranged as shown in figure 4.16, the chopper still changes direction during charge phase, but it would hardly

affect the output because both positive and negative output are high at that time, as can be seen in figure 4.17.

It is worth noting here that it is better to put a pair of inverters between the comparator and chopper because the chopper might cause imbalance at the comparator output, which results in inherent offset. Inverter can serve as a buffer and effectively solves this problem.

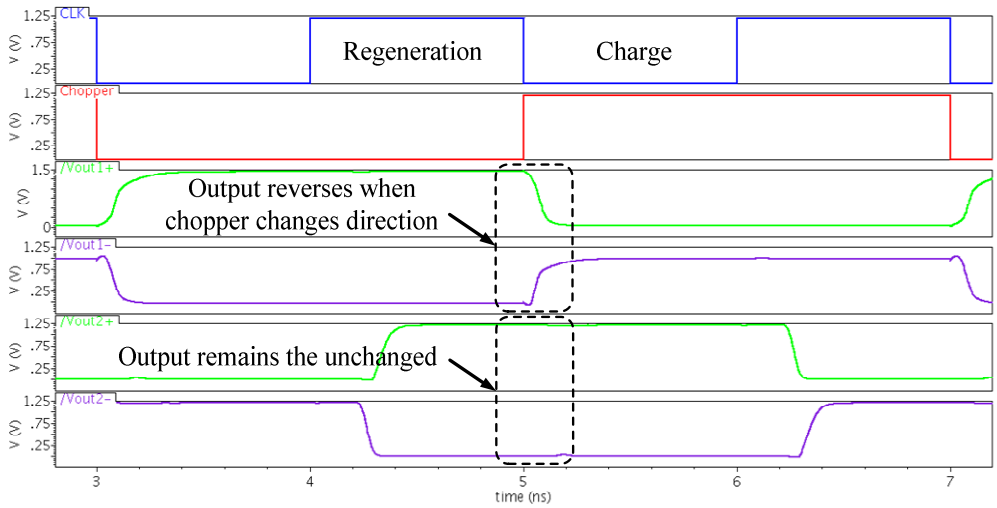

Figure 4.17 Simulation result of comparator output with chopper placed at different positions.

There is another block called metastability converter added in the output path and, as the name suggests, it is used to alleviate metastability error. When the input voltage happens to be very close to the reference voltage, the comparator output might not have enough time to regenerate to a valid logic value. This metastable output, when observed by the decoder, can be interpreted as either logic one or zero. Depending on the decoder used, this might cause very large errors. To solve this problem, metastability converter circuit [20] as shown in figure 4.18 can be used. When its input is at metastability state, both outputs are high so that in a Gray coded ROM decoder, only one LSB error would have resulted.

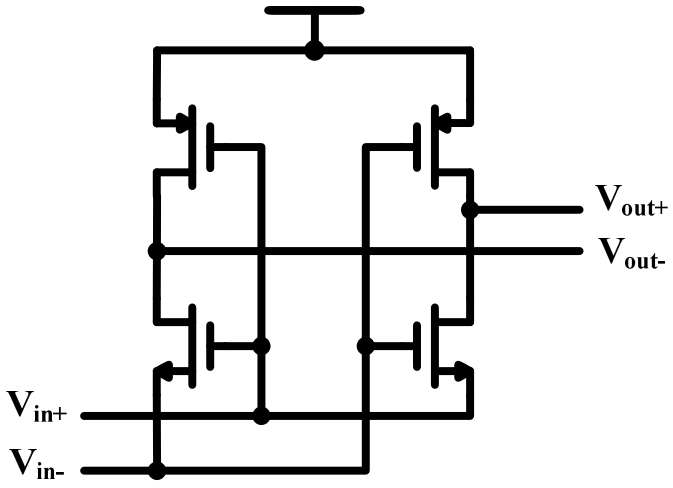

Figure 4.18 Metastability converter schematic.

The comparator, together with all the peripheral circuits shown in figure 4.16, contains all the components needed for interfacing with shared calibration circuit and following encoder circuit. The SAR logic, while consumes no power after the calibration is done, ends up occupying most area in layout. In our design, 63 units of such circuit are used to produce a 6 bit output.

4.4 Calibration Control Circuit

For a single comparator discussed in the previous section, the calibration control is easy. Only an accumulator is missing from a complete feedback loop. With 63 comparator calibrated in a serial manner, new issues like generation of end signal for each comparator's calibration, transition from one comparator to another and driving of choppers would certainly need to be addressed.

Accumulator is shared among all the comparators but SAR logic, because it also acts as registers, cannot be shared. When a single comparator is being calibrated, its output is hooked up with the accumulator and in turn, the accumulator overflow signal as well as

another signal that shows the sign of overflow is sent back to this particular comparator. At the end of each calibration, SAR logic will give out an end signal to indicate the end of calibration for this particular comparator. All the signals involved are digital, so that digital multiplexers and de multiplexers are proper choices to route the signals, as shown in figure 4.19. The channel selection block selects which comparator is being calibrated and controls all the MUXs and DEMUXs to establish a proper channel to and from the accumulator.

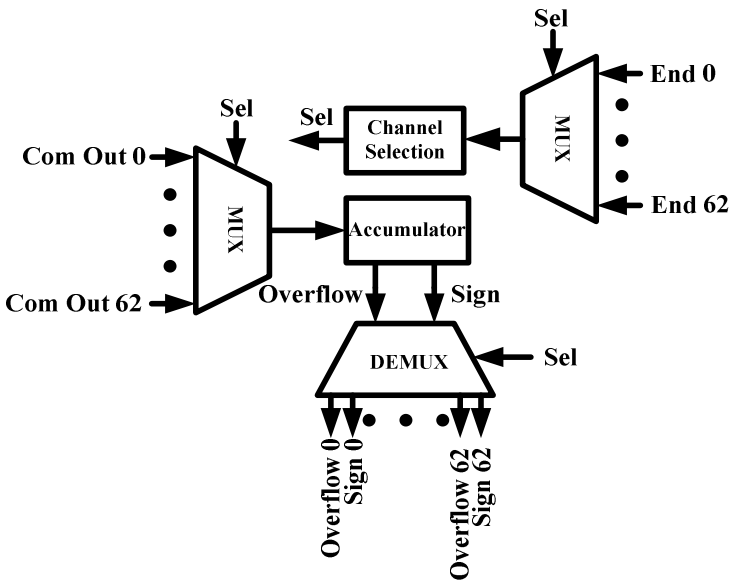

Figure 4.19 Calibration control block diagram.

The *Channel Selection* block shown in figure 4.19 is essentially a 6 bit counter with its clock input connected to a multiplexer, whose inputs are connected to comparators' *end* outputs. Depending on *Sel* signal, a certain *end* signal is select as the *Channel*

Selection's clock input. *Sel* is the 6 bit output from that counter and is initial set to zero. At the end of each calibration, a pulse will be sent from the comparator to *Channel Selection* block. It will cause the counter to count one time and the *Sel* will accordingly select the next channel. Thus calibration will automatically be done from the first channel to the last, after which the whole process would stop because no more pulse would be sent to the counter. Another DEMUX is actually employed to enable the selected comparator's choppers, while all the choppers from the other comparators would be disabled. At any given time, only one set of input choppers is working. The disturbance they may cause to T&H circuit and reference ladder is therefore minimized.

4.5 Encoder

Outputs from comparators form what is known as thermometer code. And it has to be converted by encoder to a binary code. Under ideal circumstance, in the thermometer code there should be a level below which all comparator outputs are ones while above which are all zeros. In reality, this assumption is challenged by two major problems, bubble error and metastability error [3].

Bubble error refers to the fact that sometimes there are zeros below a one. The number of zeros encircled by ones is nominated as the order of bubble error. Most of the time, only first order bubble error needs to be taken care of, as higher order bubble error is much less likely to occur. The probable causes of this error include different clock delay seen by different comparators and coparator offset [20], as shown in figure 4.20. While the first is mitigated by using a dedicated T&H circuit and the later is minimized by offset calibration, careful design of decoder is still necessary to bring this issue under control.

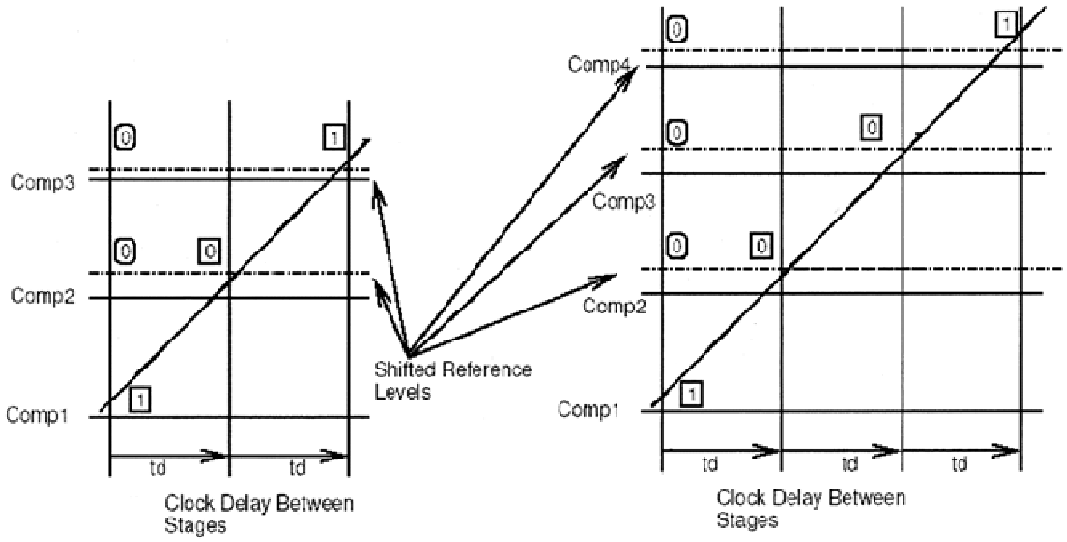

Figure 4.20 Illustration of first and second order bubble errors [20].

A simple way to avoid first order bubble error is to use 3 input AND gates to encode comparator outputs, as shown in figure 4.20. Only when the output of the current

comparator is one and the outputs of two above comparators are zero, the output of the AND gate can be set to one. Thus, first order bubble error is suppressed. Single ended output version is shown for simplicity here, but this also works well from differential comparator output.

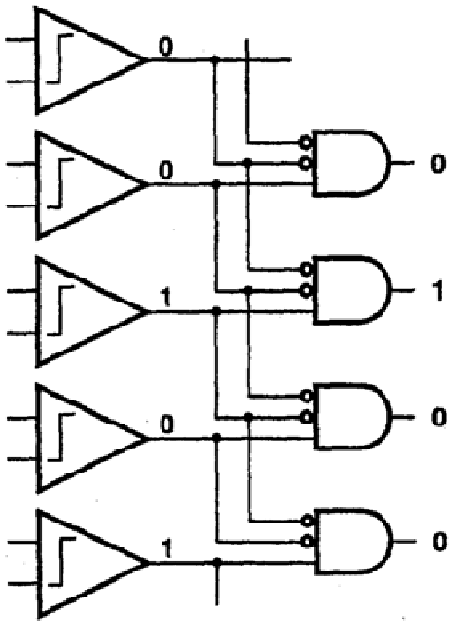

Figure 4.21 3 input AND gate used as encoder to suppress bubble error [3].

Metastability error happens when the input is very close to reference voltage. In that case, the comparator output may be balanced for a short period of time and may not be perceived as a valid logic. This output could be randomly interpreted as one or zero. This may cause the final output to have large errors. Figure 4.22 shows encoder implemented

as a binary coded ROM with comparator metastability error [20]. If the two undecided output Xs are both selected as one, then the ROM output is all zero which results in a half full scale error, as the correct output should be 100000 or 011111. Similar things would happen if both Xs are zero. The ROM output is all one and again causes a half scale error. Although these are two worst cases in this scenario that are only likely to happen when the input is close to half scale, less severe but still serious errors would occur in other cases.

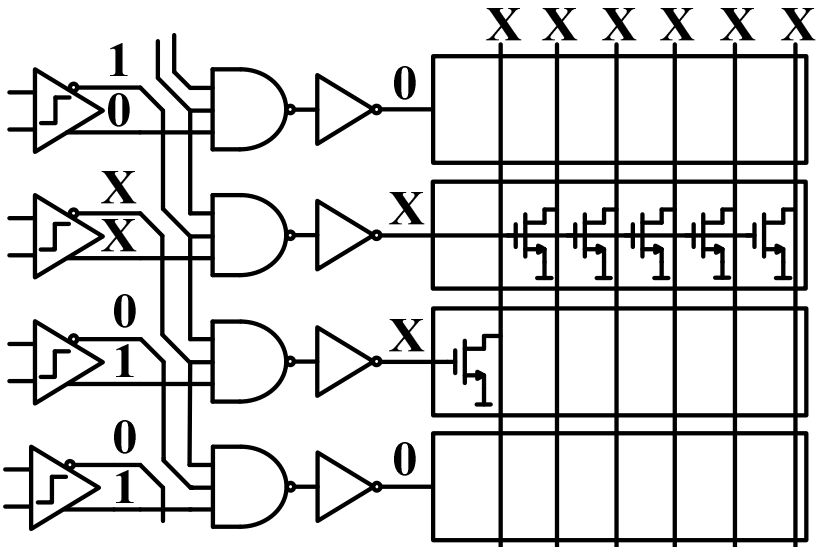

Figure 4.22 Binary coded ROM with metastability error [20].

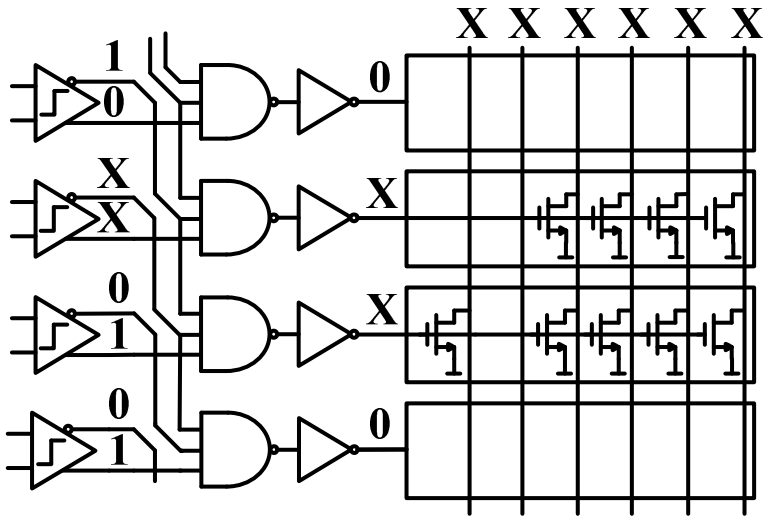

Figure 4.23 Gray coded ROM with metastability error [20].

Probability of this error can be greatly reduced if comparator regeneration time is decreased. However, the penalty is increased power consumption and thus it is not desirable to do so. Another effective way is to use Gray coded ROM as the encoder, as shown in figure 4.23. In Gray code, the adjacent two bit lines only differ in one bit. Therefore, if both bit lines are selected, ROM output would still be valid. As the input is close to the reference, it does not matter which of the two adjacent bit lines is selected. However, a large error would still occur if both bit lines are not selected. But this has already been taken care of by the metastability circuit shown in figure 4.18. The encoder in our design is implemented with 3 input AND gates and a Gray coded ROM.

Data lines of the ROM need to be charged at the first half of every clock cycle, then they would be selectively discharged by the 1 out of n code generated by AND gates. This, like the case with fully dynamic comparator output earlier, means ROM outputs are only valid for half a clock cycle. A bunch of specially designed DFFs are used as the solution to this problem [8], whose schematic is shown in figure 4.24 and the effect of DFF can be demonstrated by figure 4.25. By adding this DFF stage, the valid time for an output is increased from half a cycle to a full cycle.

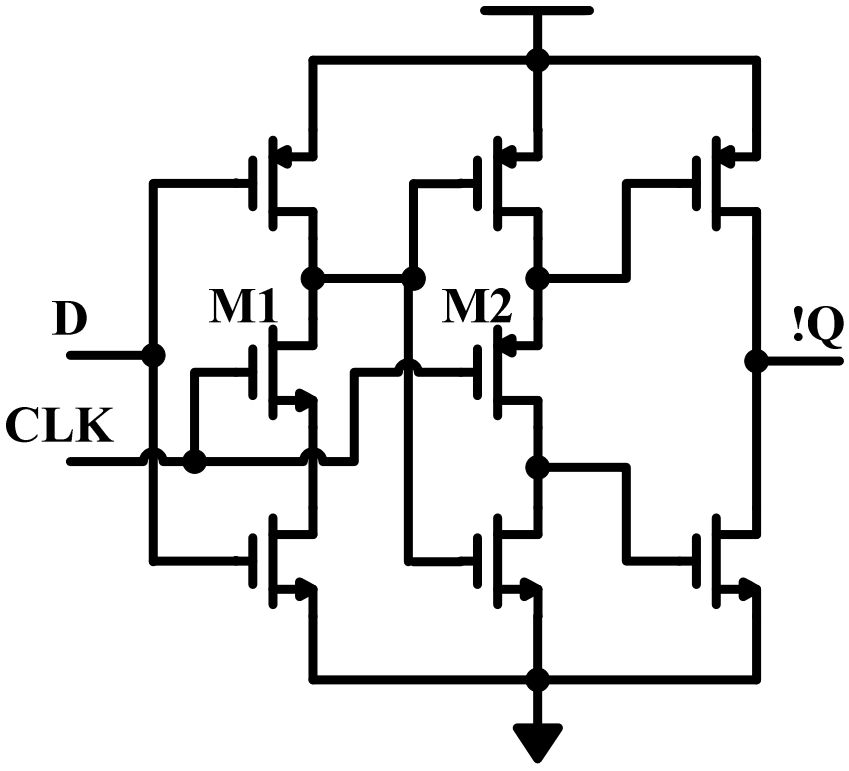

Figure 4.24 Schematic of DFF for ROM output.

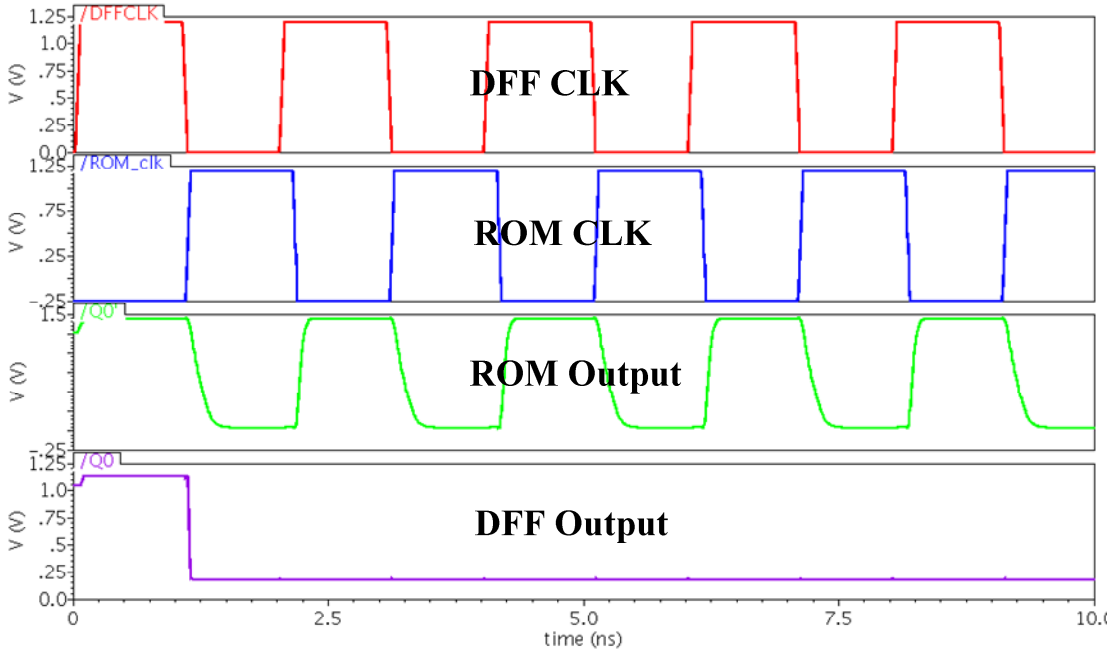

Figure 4.25 Simulation result of ROM output and DFF output.

4.6 Clock Driver

There are two major concerns involved in designing the clock driver. The first is timing and the second is driving capability. Timing means the clock of each block, including T&H circuit, comparator array, choppers and the encoder, needs to be properly arranged with respect to each other, so that the whole flash ADC would function in a reliable way. The demand for driving capability comes from the load it is driving. The

clock for the comparator array, for example, needs to have a very strong driving power so as to drive 63 comparators. Primarily, inverter chains and specifically designed delay blocks are used to manipulate the clock signals. Figure 4.26 shows simulation result of the clock driver outputs.

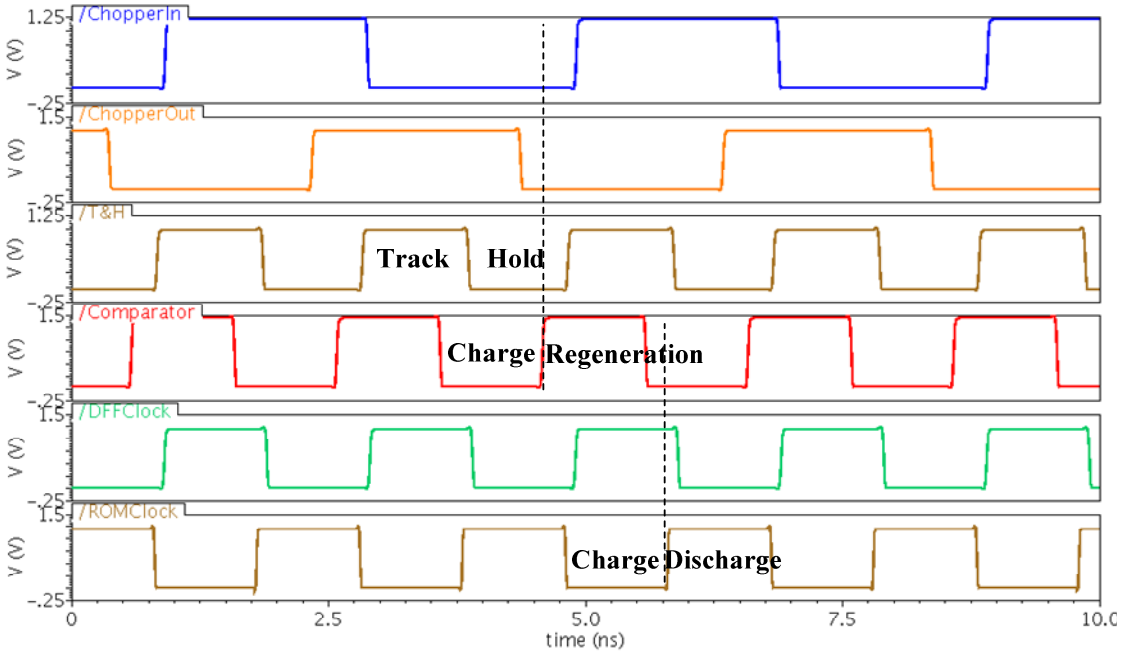

Figure 4.26 Simulation result of clock signals.

The timing relationship between various clock signals can be understood by first observing the clock of T&H circuit. In the track phase, T&H's output is not valid and it

needs some time to settle to the valid output after entering the hold phase. So the clock of comparators is arranged in such a way that regeneration happens near the end of hold phase, when the signal from T&H circuit has already stabilized. Regeneration only requires a certain amount of time, after which the change at comparator input would no longer affect its output. So T&H circuit can enter the next track phase, as long as enough time is left for the comparator to settle before the T&H output changes. Due to existence of SR Latch at the output of comparator, previous regeneration output is maintained during comparator charge phase and that is when ROM will discharge based on outputs from 3 input AND gates, as discussed in the previous section. The slight delay between ROM discharge and the end of comparator regeneration is kept for time needed by the AND gates to settle.

As for the choppers, input chopper should toggle while T&H circuit is entering track phase, causing minimal disturbance to T&H output. The output chopper, on the other hand, should change direction near the end of comparator's charge phase, when both outputs from comparator are high. However, input chopper and output chopper should be the same when the comparator starts to regenerate, otherwise the final output from

comparator would be reversed. As can be seen from figure 4.26, arrangement of input chopper and output chopper clocks satisfies all these requirements.

All the signals are generated by the clock driver block with a single clock input. Several issues are involved in designing this block. Chopper clock is produced by using a JK flip flop to double the input signal period. At a relative high speed like 500MHz, delay of the JK flip flop can no longer be ignored. So a delay block has been designed to match the delay of JK flip flop by identifying and copying the signal path of the JK flip flop. Layout of the delay block is also designed in an almost identical way. The simplest way to design the drivers, which are essentially inverter chains, is to make them identical. As long as it can meet the highest demand, it would certainly be adequate for all the other blocks. However, this is far from an optimized solution. As the load of each clock signal varies in order of magnitudes, it is better to design each inverter chain specifically suited for the block that needs to be driven, so that power is not wasted. In the end, layout of critical clock routes requires extra care because otherwise, they can cause serious signal delay.

4.7 Power Consumption of the Flash ADC

The whole flash ADC consumes 9.5mW of power running at 500MHz according to simulation result. Power consumption by calibration circuit is excluded as this part consumes no power after calibration is done. It is a very competitive result if we look back on chapter 2. The only two designs that have better performance in this aspect are both implemented in more advanced technologies and both of them adopt foreground calibration that cannot track ambient changes. Figure 4.27 shows the percent of power consumed by each block of the flash ADC.

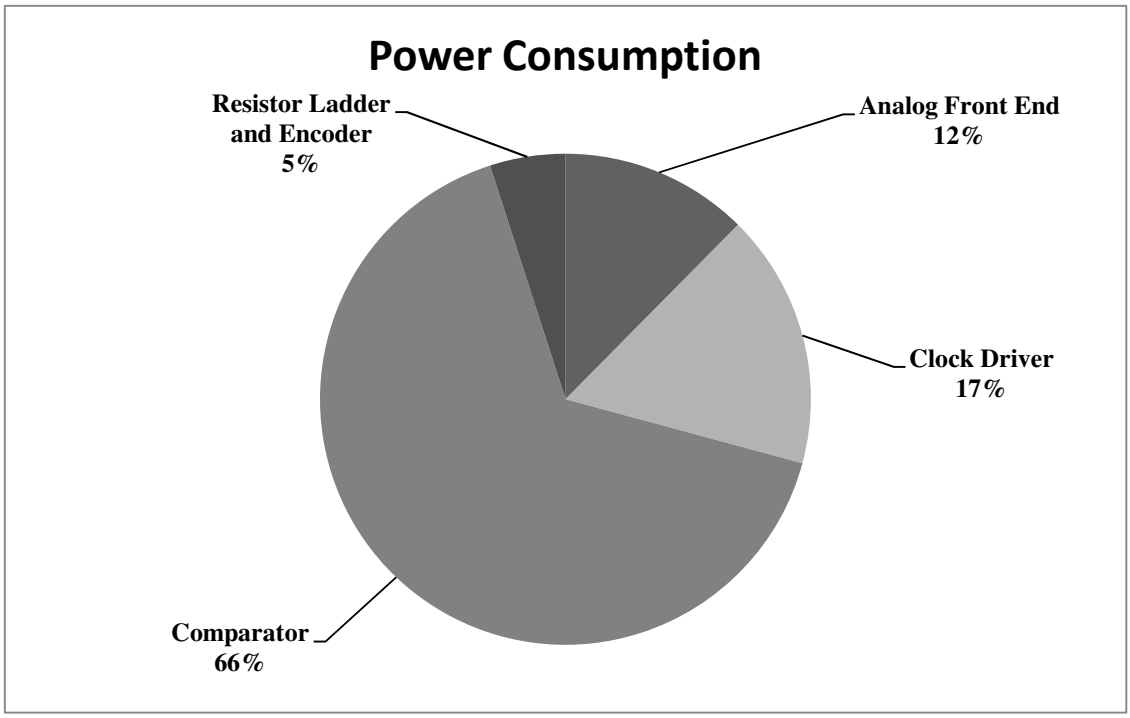

Figure 4.27 Percent of power consumption by each block of the flash ADC.

Obviously, majority of power is consumed by comparator array. As discussed in Section 4.3, MOS cap arrays are inserted to internal nodes of the fully dynamic comparator as a way to linearly adjust its offset. To cover the whole range dictated by comparator offset variation, total amount of capacitance added by the MOS caps must be large, which inevitably puts extra load on the comparator. To meet speed requirement, sizes of transistors have to be increased which in turn increases its power consumption. Therefore, the size of comparator is actually restricted by the calibration circuit. Moreover, a more powerful clock driver must be used to drive the enlarged transistors that are used to charge the output and internal nodes.

Figure 2.7 in chapter 2 shows an alternative fully dynamic comparator structure together with its calibration circuit [10]. It has an additional pair of NMOS transistors N2, which are used to fine tune the comparator's offset. So, instead of inserting MOS caps, it relies on an additional pair of input transistors to adjust the speed of discharging. However, this method is not applicable in our flash ADC design, as a very precise DAC is mandatory to generate the *Cal*+ and *Cal*- signal.

The design of resistor ladder and analog frontend has greatly benefited from calibration. As the transistor size, though limited by the calibration circuit, is still much smaller than it would have been if no calibration is utilized. This fact greatly relieves demands for resistor ladder and frontend, allowing significant power saving in those blocks.

4.8 Flash ADC Layout Design

The flash ADC has been implemented in IBM 0.13um standard CMOS technology and the whole system occupies a total area of 2.5 mm^2, the majority of which, again, is taken up by comparators. Special care is dedicated to route and distribute critical signals like various clocks. The principle is to minimize the signal length and make everything as symmetric as possible. The layout is shown in figure 4.28

Post layout simulation for the entire flash ADC was run to ensure the system is operational, as shown in Figure 4.29, where the first row is flash ADC outputs Q_0 to Q_5 in different colors. The second row I_a and the third row I_d represent currents from the analog

and digital source, respectively. The spike in I_d at 2ns is caused by the reset signal transition from 0 to 1. The bottom row shows the system clock signal running at 500 MHz.

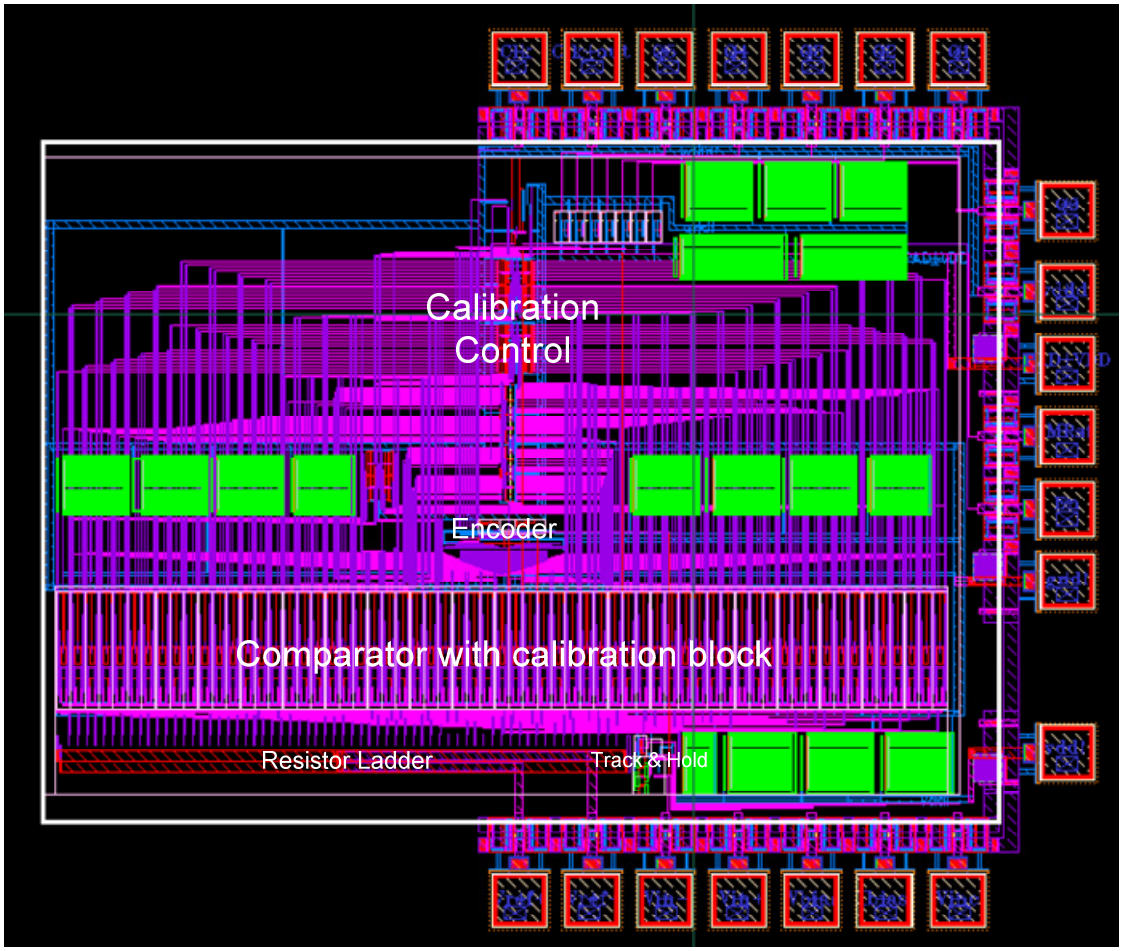

Figure 4.28 Flash ADC layout design

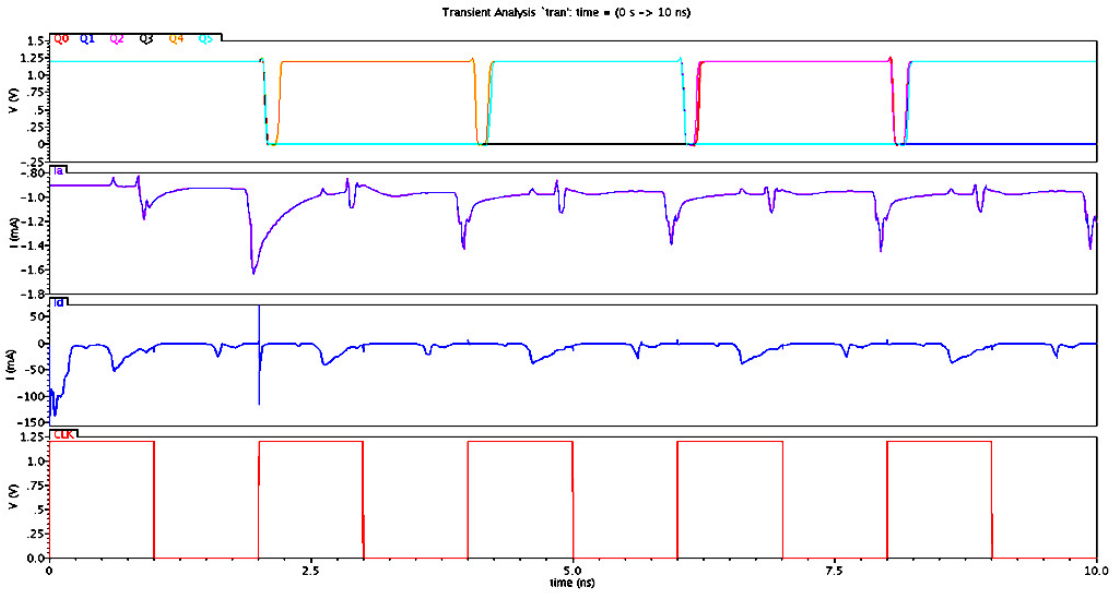

Figure 4.29 Post layout simulation results of the flash ADC

For the calibration technique to take effect, the circuit needs to run a large number (>100000) of samples. Given the complexity of the circuit and available computational power, the simulation time is too long to render it practical. Thus, schematic and post layout simulation results cannot be obtained to demonstrate the ADC's performance before and after calibration.

Chapter 5 Conclusion

Calibration technique shows great potential in high speed and low power flash ADC design. Instead of dedicating large amount of power and chip area to suppress offset, it solves the problem in a more fundamental and efficient way, which not only significantly reduces power consumption, but also greatly simplifies the design. Between foreground and background calibration technique, the later is probably a more universal solution as it is capable of tracking environmental changes. The challenging problem, however, is to obtain offset information without interrupting ADC from doing its normal job.

Major contribution of this work is the proposed comparator offset calibration technique, which is proven to be effective by prototype design in AMS 0.35um CMOS technology. This method helps designer to circumvent costly offset/area tradeoff so as to achieve a much better power efficiency. It also has virtue in its simplicity, as only a few additional components are used and most of them are digital blocks. The result is negligible additional power consumption by these circuits. Subsequent application of this technique to a 6 bit 500MHz flash ADC design in IBM 0.13um CMOS technology has

enabled the use of fully dynamic comparators. The benefits include complete elimination of static power consumption from comparators and much relieved front end design. Operating at a 1.2-V supply and running at 500MHz, the proposed flash ADC consumes only 9.5mW of power.

To further optimize power consumption and speed of this flash ADC, improvements should be made to the design of comparator. On one hand, comparator array is the dominant factor in terms of power consumption and the limiting factor in terms of speed. On the other hand, it plays such a pivotal role in the design process that everything else is largely determined by the comparator design. Particularly in this work, sizing of comparator is limited by extra loading from MOS caps used for calibration. It indicates that by either altering the structure of the comparator with reduced offset variation or developing more sophisticated calibration circuit that adds less loading, comparator size can be further decreased. It not only means the comparator array itself would demand less power, but also analog front end and clock driver can be expected to consume less power as well. Future work can focus in this direction to achieve the fullest potential.

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