INVESTIGATIONS INTO DESIGN AND CONTROL OF POWER ELECTRONIC SYSTEMS FOR FUTURE MICROPROCESSOR POWER SUPPLIES

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Ravinder Pal Singh

(B.Tech(Hons), IIT Kharagpur, India)

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Contents

Summary

Voltage Regulator Modules (VRMs) are used to provide power to the microprocessors. These modules are expected to deliver high currents upto 200A at low output voltages of around 1.2V. In order to reduce losses, microprocessors use dynamic voltage scaling, whereby the supply voltage to the microprocessor is adjusted with the computation load. To this end, the processor sends a 7-bit Voltage Identification (VID) code to the VRM, that dictates its output voltage.

Since the digital interface to the microprocessor is available to the VRM, the digital control is well suited for this purpose. However, the digital controllers have the drawbacks of reduction in phase margin due to presence of Zero Order Hold (ZOH) in Digital Pulse-Width Modulators (DPWM) and the limited resolution of the DPWM output. The digital controllers designed in this work take into account the reduction in phase margin due to presence of DPWM based ZOH. The effect of quantization of filter coefficients is also analyzed and a minimum word length filter structure is proposed for such controllers. In addition, a DPWM architecture is proposed to improve the time resolution of the DPWM. The proposed scheme is fabricated in the form of an Application Specific Integrated Circuit (ASIC) and is verified using experimental results.

The VRM control requires the inductor currents to be sensed. Thus, a current sensing method is described which is based on Giant Magneto Resistive (GMR)

effect. It is based on sensing the magnetic field generated by the flow of current. Using fundamental equations of the field distribution, it is shown how the sensor can be used for sensing the inductor current. Simulation and test results are provided to assist the analysis.

Due to high currents, it becomes essential to have multiphase topology, where the synchronous buck converters are connected in parallel such that each phase leg carries only a fraction of the total output current. However, the current control of such a topology will require N-current sensors. Thus, a sensing and sharing algorithm is proposed which uses only one current sensor.

The control of a VRM ensures the voltage regulation during steady state operation. However, the transient response of a DC-DC converter still gets governed by the fundamental equation of rate of change of inductor current. It is proportional to the voltage across the inductor and inversely proportional to the inductance. Two new circuit topologies are proposed which increases the slew rate of inductor current during transient and thus improve the transient response of the system. The performance of these topologies are verified with simulation and experimental results. These schemes give another design freedom to optimally design the converters, resulting in lower inductor current ripple and requiring smaller output capacitor as compared to the conventional schemes.

In all, this dissertation focuses on the design development and control of Voltage Regulator Modules for low voltage and high current applications. Theoretical developments have been appropriately supported with analytical and experimental results.

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List of Symbols

V_{in}	Input voltage (V)
V_{out}	Output voltage (V)
V_{ref}	Reference voltage (V)
I_o	Output current (A)
ΔI_o	Change in output current (A)
I_L	Inductor current (A)
ΔI_L	Inductor current ripple (A)
v_{ref}	Reference voltage for AVP (V)
i_o	Instantaneous output current (A)
R_{droop}	Droop resistance for AVP (Ω)
L	Circuit inductance (H)
L_k	Inductance of phase k (H)
r_L	dc resistance of inductor (Ω)
C_o	Output capacitance (F)
r_c	Equivalent resistance of output capacitor (Ω)
C_{in}	Input Capacitance (F)
r_{cin}	Equivalent resistance of input capacitor (Ω)

f_s	Switching frequency (Hz)
T_s	Switching period (s)
f_{CLK}	Clock Frequency (Hz)
T_{CLK}	Time period of the clock (Hz)
N_{ADC}	ADC Resolution (bits)
N_{DPWM}	DPWM Resolution (bits)
ρ_u	Slew rate of inductor current during step-up transient (A/s)
ρ_d	Slew rate of inductor current during step-down transient (A/s)
ρ_1	Available slew rate of inductor current (A/s)
ρ_2	Revised slew rate of inductor current (A/s)

Chapter 1

Introduction

Microprocessor scaling has consistently adhered to Moores law [1], thereby doubling the transistors every 18 months, as seen in Fig. 1.1 [2]. Increasing transistor density combined with the performance demanded from next-generation microprocessors result in increased processor power. Scaling of transistors also necessitates a reduction in the operating voltages both for reliability of the finer-dimension devices and for reducing the power consumed by the microprocessor.

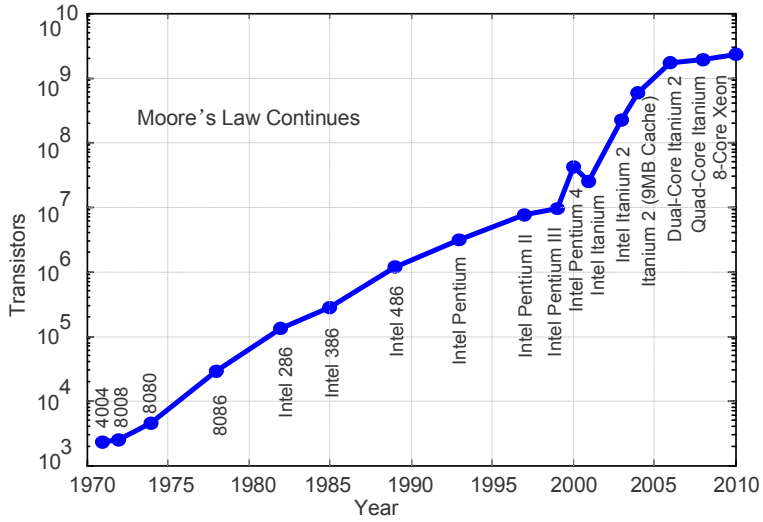

Figure 1.1: Intel CPU transistors double every 18 months (source:[2])

The power loss is $P_L \propto N \cdot C \cdot (V_{dd})^2 \cdot f_{clk}$ where, N is the number of cells, V_{dd} is the supply voltage, f_{clk} is the clock frequency and C is the capacitive loading of a single CMOS cell. Since the number of CMOS cells per die area is growing as predicted by the Moore's law, the net result is increased power consumption of the future microprocessors. Historical data on the increase in power for Intel microprocessors is included in Fig. 1.2 [3][4]. It is seen that the power doubles approximately every 36 months. This is attributed to simple analytical relation based on increasing clock frequency, transistor count and less aggressive voltage reduction. However, since the power consumption of the chip is large, any reduction in voltage will increase the supply current drawn by the microprocessors.

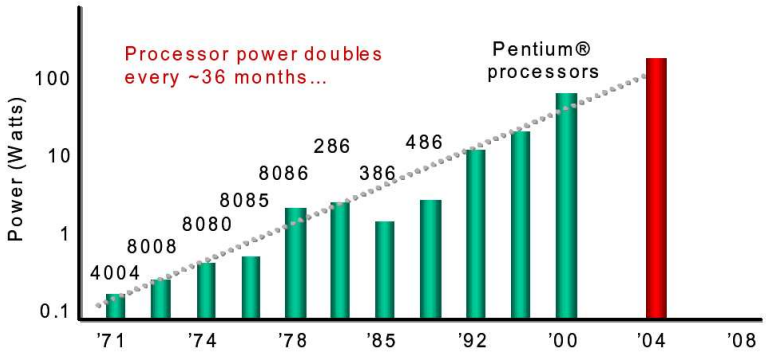

Figure 1.2: Historical power trend for Intel CPUs (source:[3])

According to Intel′s prediction, one can expect the power consumption of around 200W. The supply voltage will drop to below 1V and the supply current will be around 200A [4]. The output voltage tolerance is required to be less than 1% even in the presence of high slew rates of current drawn by the microprocessors. These tight required regulations, place an enormous burden on the circuits that provides power to the chip. These circuits are collectively referred to as Voltage Regulator Modules (VRMs).

Normally the VRMs supplying power to the microprocessors derive power from a 12V regulated bus [5][6]. For low voltage low current VRMs, a synchronous buck converter has been found to be suitable for such conversion. However if a single stage buck converter is used in 12V to 1V, 200A VRM, then due to the stringent voltage regulation requirements and due to the large slew rates of the current, large output filter will be required. Due to limited space on motherboards, such size of VRMs would not be feasible [7].

To meet the requirements of limited space on motherboard and the tight regulations, the power conversion must be done at higher switching frequencies. This will reduce the size of the required components and it will provide a fast transient response. The amount of required output filter size can also be reduced using an interleaving multiphase topology. With multiphase topology, the synchronous buck converters are connected in parallel, such that each phase leg carries only a fraction of the total output current. By operating the various converters in a phase-shifted manner, such a topology can offer decreased magnitude of output voltage ripple. It also helps in increasing the frequency of the voltage ripple. Thus, the size of filter components can be reduced to a greater extent.

In an interleaved buck converter topology, it is important to share the currents equally among various phases. However, due to variation in the inductor values, differences of components, connections and layout results in unequal current distribution among phases. This causes uneven distribution of losses and reduces the overall efficiency. Thus, appropriate current sharing mechanism is required to

distribute the current evenly among the phases.

In order to maintain good current sharing among the phases a current sensor needs to be added in a DC-DC converter. For a paralleled converter system, sensor needs to be added for each converter. The performance of any such design will depend on the performance of the current sensing technique. The output of current sensor should be linear in the operating range of VRMs and should have high bandwidth so as to sense the currents during load transients with high slew rate. Apart from the high output currents, the VRMs are expected to maintain tight voltage regulation even in the presence of such large load current transients.

This thesis focuses on the design development and control of Voltage Regulator Modules for low voltage and high current applications. All the above issues related to the VRM design have been considered. Followings are the major contributions of this work.

- The first important contribution is the development of digital controllers for interleaved buck converters. Problem of variations in inductor values among different phases has been brought out and a method to overcome them has been discussed. Such digital controllers can be implemented with simple Field Programmable Gate Array (FPGA) development kits for quick prototyping.

- Such implementation uses a Digital Pulse Width Modulator (DPWM) to control the duty ratio of the gate pulses. However, the time resolution of these pulses gets limited by the operating clock frequency of the FPGA board.

Thus, a scheme is presented which improves the time resolution as compared to the conventional architecture. The proposed scheme is fabricated in $0.35\mu m$ Austria Micro-Systems (AMS) process and is verified with experimental results.

- The third contribution is an isolated current sensor which works on the magnetic field developed by the current to be measured. Comprehensive analysis to evaluate the feasibility of such a current sensor has been carried out. Experimental results are presented to verify the working principle of such a sensor, when applied to high current applications.

- In an interleaved buck converter, a current sensor is normally employed for each phase so as to achieve current sharing among individual phases. Detailed analytical study has been done to establish the feasibility of a scheme which can reduce the number of sensors in such a system. Thus, a scheme is presented which uses a single current sensor to sense various currents and is independent of number of phases. The performance of such a scheme is verified with experimental results.

- In a buck converter, the slew rate of inductor current gets limited by the circuit parameters. The slew rate can be increased either by increasing the voltage across the inductor or by reducing the inductance. However, reduction of inductance will result in higher losses and on the other hand, the voltage across the inductor is limited by the input and output voltage. Another significant contribution is the development of circuit topology which increases

the slew rate of inductor current during dynamics. The performance of such a topology is verified with simulation and experimental results.

- Analytical verifications are presented to show that the step down load transient is more critical in a buck converter with low conversion ratio. Hence, a new topology is developed which improves the step-down load transients in such low voltage buck converters.

Altogether, this dissertation attempts to solve the above mentioned issues. There are 9 chapters in this dissertation, each with a specific focus. The organization of the thesis is as follows.

- The next chapter will give a literature survey of various solutions aimed to address the above mentioned issues. The performance of these methods has been critically analyzed. This will help to bring out the focus of the present work and also recognize the problems.

- Starting from the basic concepts, the need for a fast digital controller is discussed in chapter three. It gives the design development of such a controller which can be easily implemented on an FPGA platform.

- The fourth chapter discusses the limited time resolution of the gate pulses. It presents a hybrid digital PWM architecture which helps to improve the time resolution of such pulses.

- The fifth chapter evaluates various sensors which are used for current sensing. Identifying the need for a current sensor which is suitable for given low voltage

and high current applications, a current sensing method is proposed.

- In an N-paralleled converter N current sensors are required. The sixth chapter discusses the current sharing scheme which uses single sensor to sense the inductor current in a multiphase converter.

- Two new circuit topologies which improves the step-up and step-down load transients have been covered in chapter seven and chapter eight respectively.

- Finally, chapter nine concludes this thesis highlighting the major contributions of this research.

Chapter 2

Background and Problem Definition

2.1 Digital Control of Voltage Regulator Modules

Advances in processor technology have posed stringent requirements on the voltage regulator module (VRM) design. Due to stringent regulation requirements, the design of next generation VRMs need a thorough understanding of the performance and design trade-offs. The supply voltage of the microprocessor will drop to below 1 V and the supply current will be around 200 A [4]. For microprocessor loads, high slew rates of VRM output current are expected. In addition, the VRM output voltage regulation is required to be less than ± 1%.

In order to reduce losses, microprocessors use dynamic voltage scaling, whereby the supply voltage of the microprocessor is adjusted with the computational load [8]. To this end, the processor sends a 7-bit Voltage Identification (VID) code to

the VRM, that dictates its output voltage. Depending on the VID code, the output voltage level changes by 6.25mV step every $5\mu s$ [6].

Usually the analog control methods have been proposed for VRMs [7], [9], [10], [11]. Fig. 2.1(a) shows a typical analog voltage-mode control method. In this implementation, the digital VID code has to be converted to its equivalent analog signal V_{ref}. An error amplifier processes the output voltage error ($V_{ref} - V_{out}$) and realizes a compensator for the desired control action. It requires proper selection of passive components for realizing the desired compensators. However, component variations and aging effect are also commonly seen in analog control design which affects the system performance. Moreover, the presence of noise in the system makes it difficult to achieve a resolution of 6.25mV.

Since the reference voltage is available to the VRM as a digital code, it can be easily incorporated into the digital controllers. Recently, the digital controllers have gained attention due to their low quiescent power, immunity to analog component variations, ease of implementing advanced controller architecture and other advantages. Moreover, developments in Field Programmable Gate Arrays (FPGA) makes it a useful platform to design and validate the digital controllers. The controllers may then be fabricated to result in a digital controller integrated circuit (IC). However, the disadvantages of digital control include finite word length effects and sampling time delay due to presence of Zero order Hold (ZOH).

Although digital control is suited for VRM due to the digital interface to the

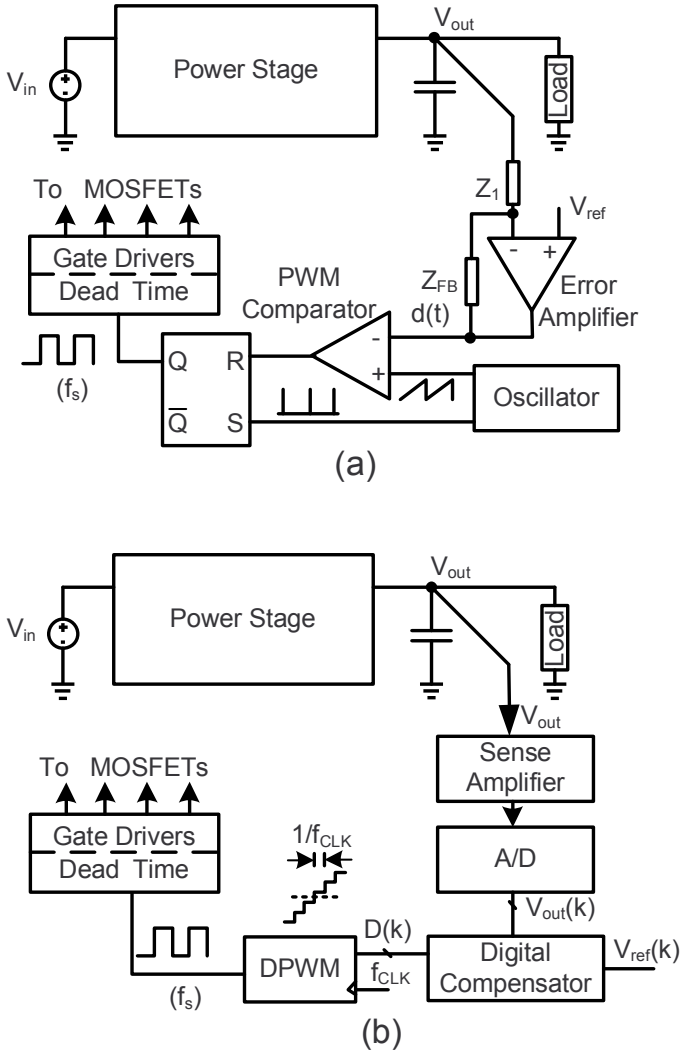

Figure 2.1: Block schematic of (a) Analog PWM controller and (b) Digital PWM controller.

microprocessor and the other generic advantages of digital control, it is a challenge to deliver the performance required of the next generation VRMs [4].

2.1.1 Digital Control of DC-DC Converters

A comparison of various digital control design approaches for DC-DC converters have been presented in [12] and [13].

A digital proportional + integral + derivative (PID) controller for DC-DC applications presented in [14], uses a lookup table. The lookup table maps the controller behavior to various values of the digitized error signal. Since the size of the lookup table depends on the range of the error signal and the desired regulation of the output voltage, this is scheme only suitable for small range of operating conditions.

For hand-held devices, DC-DC converter power supplies have to operate very efficiently to prolong battery life. To this end, [15] uses a load dependent operation that alternates between two discrete switching frequencies for the same output voltage. It achieves high efficiency by operating the converters in discontinuous conduction mode at light loads.

As opposed to analog control methods, digital control adds quantization noise. High resolution is required to minimize quantization noise. To this end, a high resolution Analog to Digital Converter (ADC) is required. Moreover, a high speed of conversion is necessary to achieve high control bandwidth. Such ADCs need large floor space in digital ICs. To overcome the problem of large floor space, [16] proposes a delay line ADC. However, due to process and temperature variations, the delay cannot be defined precisely. Hence, it requires calibration of ADC.

Increasing the resolution of ADC creates another problem. It has been shown [17] that, if the resolution of ADC is greater than the resolution of the Digital Pulse-Width-Modulator (DPWM) counter and there is no integral control action,

a limit cycle oscillation occurs. Therefore, it has been recommended that the resolution of DPWM be at least 1 bit higher than that of ADC. However, for a given clock frequency, increasing the DPWM resolution results in a lower switching frequency. To meet, the high switching frequency demand along with high resolution of DPWM, few methods have been proposed. For example, a digital PWM using a ring-oscillator-multiplexer scheme is implemented in [18]. On the other hand, a dither signal is used to increase the effective DPWM resolution while using a low resolution of the PWM counter [17] .

2.1.2 Digital Control of high current VRMs

Most digital control schemes for VRMs, proposed so far, are voltage-mode control. However, there are few examples of current mode control such as [19] and [20]. Current control facilitates current sharing in interleaved converters, which is a popular topology for VRMs.

A low complexity digital peak current control is presented in [20]. However, it results in variable switching frequency operation. The scheme uses low resolution digital-to-analog converters (DACs) to generate a droop compensated current and voltage reference signal. These are compared with the actual signals with help of an analog comparators. Though the scheme achieves a high current operation with a fast current control, its resolution is dictated by the DACs.

On the other hand an average current mode or voltage mode control, uses

the average value of the sampled state variable, respectively.

In order to achieve high bandwidth, over-sampling is used. In over-sampling, sufficient number of samples of the state variable are taken within a switching period. The average value of the state variable is then computed over the switching period. This average value is used to compute the duty ratio for the next switching period [21]. This introduces a ZOH behvaior in the system.

On the other hand, multi-sampling can be used to reduce the effect of ZOH in DPWM. In multi-sampling, multiple samples are taken within the switching period. Hence, the value of the state variable that is compared with the DPWM ramp is not equal to the sampled and held value at the start of the switching period. However, this method can introduce high frequency ripple due to the aliasing error in the sampled variable. To overcome this error, a repetitive filter is proposed [22] that eliminates the aliasing effect and thus achieves a control bandwidth that is similar to that of analog control.

A predictive current control [19] is proposed for VRMs. The scheme requires the converter parameter like inductor value (L) to formulate the control law. However, such scheme will require a disturbance observer to compensate for the unmodeled dynamics. An appropriate gain has to be calculated for the disturbance observer. Insufficient gain reduces the response time of the system while high gain causes limit cycle. Moreover, for current sharing, precise value of each phase inductor is required.

Previously reported models of interleaved converters assume all the inductors to be the same, in which case, the problem is reduced to having N synchronous buck converters in parallel. In practice, it is very difficult to have same value for all inductors. There can be $\pm 5 - 10\%$ variation in the inductor values, resulting in asymmetry in the phases. This results in uneven distribution of inductor current among individual phases. Thus, appropriate current sharing mechanism is required to distribute the current evenly among the phases. A current mode control is used to solve this problem which takes into account the variations among inductance values.

Thus, a digital control scheme with individual phase current loops is used to achieve current sharing during dynamics and steady state operation. In a typical digital control system, the duty ratio command is the fed to the Digital Pulse-Width-Modulator (DPWM) to produce the gate signals for the converter. Due to the nature of DPWM, such digital control systems are characterized by the presence of the Zero-Order-Hold (ZOH). Therefore the performance of these systems is a function of DPWM switching period. Thus, appropriate digital controllers need to be designed taking into account the performance degradation due to presence of DPWM based ZOH. Moreover, the performance also depends on quantization error, round-off and truncation errors. The effect of quantization of filter coefficients need to be analyzed and a minimum word length filter structure should be obtained.

2.2 Time Resolution of DPWM

Most digital control schemes use DPWM to obtain the gate pulses. However, the performance of such systems get limited due to the finite resolution of the DPWM pulses.

A typical block schematic for implementing a digital control is shown in Fig. 2.1(b). The control algorithm takes the digitized error signal $(V_{ref}(k) - V_{out}(k))$ and computes the discrete set of duty-cycle command $D(k)$. The duty ratio word is processed by DPWM which generates the gate pulses at the desired switching frequency (f_s).

To implement this, a counter based DPWM is commonly used which provides high linearity and is simple to design. However, the minimum time resolution of such a DPWM is equal to the time period of its clock. This puts stringent requirement on clock frequency if fine resolution of duty ratio is required, for example, in a VRM type application.

It has been shown in [10] and [23] that it is advantageous to obtain the VRM output from a $5V$ bus. Thus, for our analysis the input voltage has been chosen as $V_{in} = 5V$. For obtaining $\Delta V_{out} = 6.25mV$ with $V_{in} = 5V$, we need a resolution of

$$\Delta D = \frac{\Delta V_{out}}{V_{in}} = 0.00125 \tag{2.1}$$

If the switching frequency is $f_s = 1MHz$, this corresponds to a time resolution of $\Delta t = 1.25ns$. For obtaining such time resolution, the counter based DPWM has

to be operated at $800MHz$!

In general, for achieving N-bit resolution of the DPWM block, it needs to be clocked at $2^N.f_s$, where f_s is the switching frequency of the converter. For example, an 8-bit DPWM generating switching frequency of $f_s = 1MHz$ will require a clock frequency of $f_{CLK} = 256MHz$ and so on. To meet, the high switching frequency demand along with high resolution of DPWM, various methods have been proposed in the past. Some of these methods are described below.

It has been established that if the resolution of the DPWM counter is smaller than the resolution of ADC and there is no integral control action, a limit cycle oscillation occurs [17]. Therefore, it has been recommended that the resolution of DPWM be at least 1-bit higher than that of ADC. Thus, a dither signal is used to increase the effective DPWM resolution while using a lower-resolution DPWM counter. Introducing dither increases the overall resolution of the DPWM but it results in sub-harmonic oscillations. For M-bit increase in effective DPWM resolution, it will result in sub-harmonic oscillation at $f_s/2^M$, where f_s is the switching frequency of the converter. Moreover, a limit on the maximum possible increase in effective resolution is established in [17].

In order to increase the resolution of DPWM, a ring-oscillator-multiplexer based DPWM scheme is proposed [18]. The time-resolution of the output depends on the delay introduced by the cells in the ring-oscillator. However, for N-bit resolution this will require 2^N stage oscillator and a 2^N-to-1 multiplexer to select the

appropriate signal from the ring oscillator. Such an implementation of the DPWM module requires large silicon area, which increases exponentially with the number of resolution bits (N). Moreover, high-frequency operation of such an oscillator results in power loss. In order to reduce power, tapped delay line structure has been proposed [24], [25]. The tapped delay line operates at the switching frequency, thus reducing the power significantly. However, this scheme also requires 2^N stage delay line and a 2^N-to-1 multiplexer to select the appropriate signal from the delay line, which results in large silicon area.

In order to reduce the silicon area, segmented delay line has been proposed [25]. In such a scheme, the delay line is segmented into groups of smaller delay lines. The desired signal can be selected by using smaller multiplexer. In order to increase the resolution, such segments need to be cascaded and an appropriate multiplexer is used. Another variation of segmented delay line scheme is segmented binary weighted delay line based DPWM [26]. In such a scheme, the delay cells are designed to provide binary weighted delays. Although the number of delay cells is reduced, but the size of individual delay cells will vary as to provide the desired delay. The larger delay is generated by simply replicating the basic delay cells, resulting in the same overall number of delay cells.

Silicon area resulting from delay cells can be reduced by using a hybrid approach [16], [27]. It resolves the high-resolution duty ratio word into two groups: coarse duty-ratio command comprising of the most-significant bits and fine duty-ratio command comprising of the lower-significant bits. While the coarse duty

ratio is obtained using counter based DPWM, the fine duty ratio is obtained using standard delay-line structure. This can reduce the number of delay cells required, however, the area and power are still dictated by the effective increase in the DPWM resolution.

Similarly, [28] resolves the duty-ratio word into decimal part and integral part and two pulses are obtained using these parts. The decimal pulse slowly pre-charges the input capacitor of the driver IC through a series resistance. Based on the initial voltage at the capacitor, the delay-time of the gate pulse can be changed and hence the resolution of the duty-ratio. Since the scheme is based on the pre-charging the input capacitor, it requires the decimal pulse to be ahead of the integer part pulse. Furthermore, the decimal pulse should not be such that it results in a voltage greater than the threshold voltage. Thus, the operation of this scheme gets limited to a narrow range.

The above methods use a constant switching frequency and on-time is varied to adjust the duty-ratio. Alternately, a constant on-time modulation has been proposed in [29]. It uses counter based DPWM structure, which increases the switching period by T_{CLK} so as to reduce the duty ratio. The drawback of such a scheme is that for different values of duty cycle, the switching frequency is different. If the clock frequency is not large enough, this may result in significant variation in switching frequency.

With the advent of FPGA technology, it is also possible to increase the clock

frequency. Delay-locked loops (DLL) are commonly present on FPGA for obtaining the phase shifted clocks. Using these DLLs, it is possible to multiply or divide the clock frequency. The multiple of clock frequency is used to obtain the finer duty ratio pulses [30]. However, an increase in clock frequency by 4 will only result in a 2-bit increase in effective resolution of DPWM. Since the modern FPGAs can provide a maximum of $4f_{CLK}$, the scheme results in a limited improvement.

In order to overcome the limitations of the DLL method, Digital Clock Manager (DCM) circuit has been employed [31]. DCM is present on modern high-end FPGA boards and is essentially a delay locked loop along with the digital frequency synthesizer and a phase shifter [32], [33]. It can provide phase shifted versions of the input clock - 0 deg, 90 deg, 180 deg and 270 deg along with the multiples of input frequency $2f_{CLK}$ and $4f_{CLK}$. Using one DCM, a 2-bit increase in effective resolution of DPWM can be achieved. Such DCM circuits need to be cascaded for increasing the resolution further. In cascaded DCM structure, the subsequent DCM stage is operated at twice the clock frequency of its preceding DCM stage. In comparison, both the DLL scheme [30] and DCM architechture [31] benefit from the FPGA on board resources to implement the delay line. The latter relies on the phase of the input clock while the former relies on the multiple of the system clock.

In addition to increasing the system clock frequency, both the edges of the clock can also be exploited. In order to implement this, a counter based DPWM is used and the converter is operated in open-loop. Clock frequency of 100MHz and 200MHz is used and both the edges are used to increment the counter. As seen

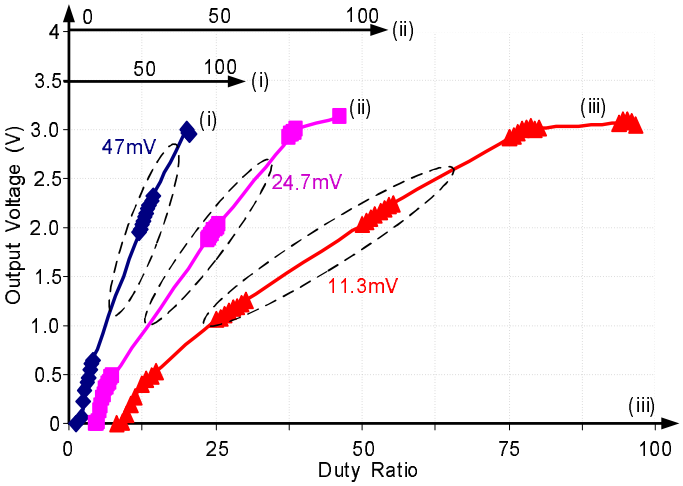

Figure 2.2: Experimental results for observing the resolution of output voltage. Case (i): Single Edge, 100MHz clock; Case (ii) Dual Edge, 100MHz clock; Case (iii) Dual Edge, 200MHz clock.

from Fig. 2.2, increasing the clock frequency can improve the duty ratio resolution and hence the output voltage variation. Using (2.1) we have

$$\Delta V_{out} = \Delta D \cdot V_{in} \tag{2.2}$$

For 100MHz clock, we have $\Delta D = 0.01$ or $\Delta D = 0.005$ for single edge and dual edge scheme respectively. Thus, for an input voltage of $V_{in} = 5\,V$, this results in $\Delta V_{out} = 50\,mV$ and $\Delta V_{out} = 25\,mV$. Similarly, using both the edges of 200MHz clock, $\Delta V_{out} = 12.5mV$ can be achieved. Thus, by using both positive and negative edges of the clock the time-resolution can be improved by two times. However, any further improvement in time-resolution requires the clock frequency to be increased which is not a viable solution.

The methods described above either increase the clock frequency or use a customized DPWM architecture. The schemes based on customized DPWM architec-

ture results in increased silicon area and power consumption, which is undesirable. On the other-hand, the schemes based on DLL and counter-based DPWM are not scalable in nature and provides resolution improvement only for a limited range.

Thus, a DPWM architecture is required which can improve the time resolution without having to increase the clock frequency or resulting in additional power loss.

Nonetheless, DPWM block needs to operate with a digital control scheme, which implements voltage mode control or current mode control. Such control schemes require the inductor current to be sensed. Current sensing is also required for load sharing among paralleled converters. The performance of such a system will depend upon the current sensor employed for this purpose.

2.3 Current Sensing Techniques

Numerous methods have been proposed and implemented for sensing the current. All these current sensing techniques can be broadly classified as non-isolated and isolated sensing techniques. The non-isolated sensing technique involves sensing the voltage drop across some resistive element in the circuit or by filtering the voltage across the inductor. On the other hand, the isolated measurement of an electric current is usually done by sensing the magnetic field created by the current to be measured. Some of these methods are listed here:

2.3.1 Series resistance

This method is based on putting a known sense resistor in series with the inductor and sensing the voltage across it. This method gains its popularity because of its simplicity, accuracy and relatively large bandwidth. However, such a current sensing scheme results in power loss. For example, in a 4-phase 100 A VRM, where each leg carries 25 A of current and output voltage is less than 1V, the additional drop across the sensing resistor can be significant, and will result in reduced efficiency. Thus a low resistance is required. A $1\,m\Omega$ resistance will give an output of 25 mV and results in a loss of 0.625 W, whereas $5\,m\Omega$ sense resistor will give an output of 125 mV but results in a loss of 3.125 W. By decreasing the sense resistance, the power loss can be reduced but the sensed voltage becomes small. Signals of such small magnitude are hard to sense in noisy environment. Thus, there exists a trade-off between efficiency and noise. Secondly, such a resistance will have positive thermal coefficient, which will cause the resistance to change with increase in temperature, resulting in inaccuracy in current measurement.

Another drawback of such a sensing method is the presence of parasitic inductance in the series resistor. Due to fast changing currents, the sensor output will not just be proportional to the magnitude but also to rate of change of current. Although non-inductive resistors are available, their inductance is of the order of nH. Therefore a compensation network is required to filter out the effect of the parasitic inductance.

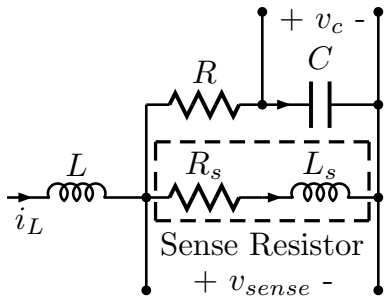

Figure 2.3: Compensation network to remove the effect of parasitic inductance.

A simple low-pass RC network is used to filter the voltage across the sense-resistor. One such arrangement is shown in Fig. 2.3. For $R_s + sL_s \ll R + 1/(sC)$, the voltage across the series-sense resistor is $v_{sense} = (R_s + sL_s)i_L$, where R_s is the resistance and L_s is the parasitic inductance associated with it. The voltage across the capacitor is

$$v_c = \frac{v_{sense}}{1 + sRC} = \frac{R_s + sL_s}{1 + sRC} i_L \tag{2.3}$$

$$v_c = R_s \frac{1 + sL_s/R_s}{1 + sRC} i_L \tag{2.4}$$

Hence, by ensuring $RC = L_s/R_s$, the sensed voltage will be proportional to the inductor current ($v_c = R_s \cdot i_L$).

PCB trace can also be used for sensing the current. However, if a small length of PCB track is used, the resistance will be small and the signal strength will be poor. A longer track is required in order to improve the signal strength. However, doing so will increase the inductance associated with it.

The effective series resistance (ESR) of the inductor can also be used for sensing the current. The voltage across the inductor can be used to sense the

current flowing through it. It is given as

$$v_L = L\frac{di_L}{dt} + r_L i_L \tag{2.5}$$

where r_L is the ESR of the inductor and i_L is the current flowing through the inductor. Thus the average current flowing through the inductor can be obtained by using a low pass filter [34]. It is fundamentally same as the resistive sensing method. But this method will require exact knowledge of the inductance and ESR. Thus this method is certainly not advisable if the components have large tolerances.

2.3.2 Inductor Voltage Sensing

This method uses the inductor voltage to measure the inductor current [35]. If the series resistance of the inductor is negligible, then the voltage across the inductor is given as

$$v_L = L\frac{di_L}{dt} \tag{2.6}$$

where L is the inductance and i_L is the inductor current. Thus the inductor current can be obtained by integrating v_L over time (Fig. 2.4).

$$i_L = \int \frac{1}{L} v_L dt \tag{2.7}$$

Such a scheme, however, requires exact value of the inductor. In practice, any inductor used in the converter will have an associated ESR.

$$v_L = L\frac{di_L}{dt} + r_L i_L \tag{2.8}$$

Integrating this over time will saturate the integrator due to the presence of DC term $r_L i_L$. Thus, this method will require compensation for the ESR of the induc-

tor.

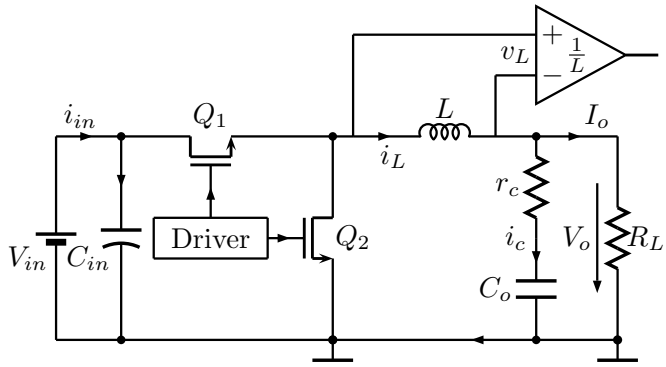

Figure 2.4: Inductor voltage sensing for obtaining the inductor current.

2.3.3 MOSFET $R_{ds,ON}$ Sensing

The on-state resistance of the MOSFET can also be used for sensing the current. The resistance of a MOSFET in its linear operating region is given as

$$R_{ds,ON} = \frac{L}{W \cdot \mu C_{ox} \cdot (V_{gs} - V_{th})} \tag{2.9}$$

where L and W are the channel length and width respectively, μ is the mobility of electrons, C_{ox} is the gate-oxide capacitance. Thus in its on-state, a MOSFET will have a voltage drop proportional the current flowing through the component ($V_{ds} = R_{ds,ON} \cdot I_{ds}$). The voltage drop can be sensed to get the current flowing through the MOSFET (Fig. 2.5). Such a scheme does not require any additional component. However, the on-state resistance are characterized by process variations. Usually the manufacturer provides the $R_{ds,ON}$ with 10-20% margin. Furthermore, the mobility of the carriers (μ) is dependent on temperature, which causes the resistance to change as the temperature changes. Thus, it requires proper calibration for accurate current sensing. One such method is presented in [36], but

it requires an additional precision sense resistor and a MOSFET for calibration purposes. Moreover, in any switching converter, there will be voltage ringing at the source drain terminals due to the presence of stray inductance and capacitances. Additional care needs to be taken to minimize the sensing errors due to such ringings.

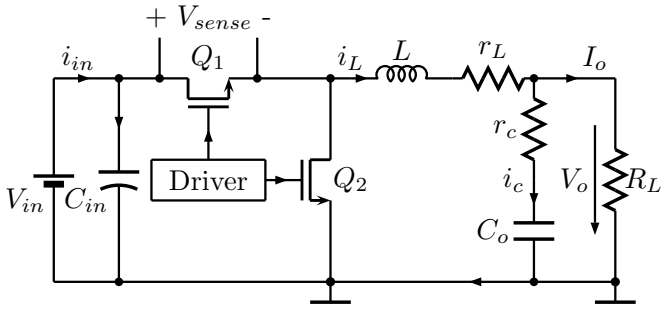

Figure 2.5: Current sensing based on MOSFET $R_{ds,ON}$.

2.3.4 SenseFET

This method is based on the principle of the paralleling MOSFETs [37]. If two MOSFETs with different on-state resistance are connected in parallel, the current distribution will be inversely proportional to their on-state resistance. The typical arrangement is shown in Fig. 2.6. The on-state resistance can be made different by changing the width of the MOSFET. The effective width of the senseFET is significantly smaller than the width of the main MOSFET (of the order of 100-1000). Thus the senseFET carries only a small fraction of the current. Such a current of small magnitude can be sensed by series sense resistance. Since the magnitude of the current is reduced, this guarantees that the power consumption is reduced and thus the efficiency does not get affected. But the power lost in this

method is determined by the output current and the sensing ratio.

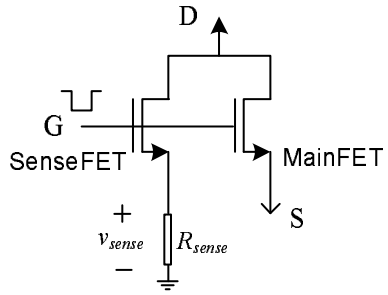

Figure 2.6: Current Sensing using SenseFET method.

The senseFETs are specially designed MOSFETs and it requires the matching of the MOSFETs. The matching accuracy decreases as the ratio of their size increases. Moreover, proper layout needs to be chosen to minimize the effect of mutual inductance among the devices. Even a small degree of inductive coupling between the main MOSFET and the senseFET current paths can cause significant errors during large rate of change of currents (di/dt).

The above mentioned methods do not provide isolation and they measure the current directly by sensing the voltage drop across the resistive elements in the circuit. On the other hand, the isolated measurement of an electric current is usually done by sensing the magnetic field created by the current to be measured. Some of these techniques are listed here:

2.3.5 Current Transformers (CT)

The current or voltage levels can be changed by using the transformer turns ratio. By stepping down the inductor current to a smaller level, it can be sensed

using resistive sensors. However, the main drawback of such a scheme is that transformer will block the average (DC value) of the the current. Moreover, depending upon the turns ratio, it will be a bulky and an expensive solution.

2.3.6 Rogowski Coil

A Rogowski coil is an air-cored toroidal coil placed round the conductor. The voltage induced in the coil is proportional to the rate of change of current in the conductor. This voltage is integrated to accurately produce the current waveform. In such a coil, it is important to ensure that the winding is as uniform as possible. A non-uniform winding makes the coil susceptible to magnetic pickup from the adjacent conductors or other sources of magnetic fields. To overcome this, a planar Rogowski Sensor is proposed in [38], which can be used for integrated power electronic modules (IPEMs). However, the main drawback is that Rogowski Coils cannot sense the DC current.

2.3.7 Hall Effect Sensor

Current sensing using hall effect devices have also been explored [39]. It is based on the magnetic field generated by the current carrying conductor. The sensor provides a voltage proportional to the magnetic field generated by the current flowing through the conductor. Unlike current transformer and Rogowski coil, it can sense both DC and AC currents. However, the presence of magnetic core makes such devices bulky. In addition, their measurement accuracy gets affected by tem-

perature variations. Thus, due to their large size, poor temperature characteristics and due to their high cost, they are not preferred.

The non-isolated methods mentioned above are either lossy or they rely on the component value. Methods based on SenseFET require special MOSFETs to be designed and they need to be properly matched. The isolated methods are bulky and have poor temperature characteristics. These methods are certainly not useful for high performance VRM type applications where output currents are high and it is desired to maintain good current sharing despite tolerances in component values. Thus a current sensing mechanism is required, which is independent of the value of external components, provides temperature independent sensing accuracy and is practically lossless.

Such a current sensor may be used for providing over-current protection. It may be used in current-mode control of DC-DC converters for improving the transient response of the closed loop system. Such current mode control may be based on average current or peak current control. Current sensing may also be used for load sharing among paralleled converters which is an important factor in the design of a such a paralleled converter system.

2.4 Current Sharing in Paralleled Converters

A number of current sharing approaches have been presented in literature [40]. Both passive sharing and active sharing methods have been used. Passive

current sharing involves putting droop resistance in series with the outputs. This droop resistance will create enough voltage drop under load to cause the converters to share the load current. On the other hand, in active current sharing method, an additional active circuit is employed to force the individual phase currents to match the reference phase current.

Droop method is commonly used for passive current sharing [41]. It programs the voltage drop across the droop resistance so as to achieve current sharing among paralleled modules. However, the current-sharing ability depends upon the droop characteristics and hence the regulation gets affected.

In active sharing method, a number of methods have been presented in literature. One way to achieve current sharing is by using a current mode control. Such a control scheme utilizes an outer voltage loop and an inner current loop. The current command of each phase is obtained by dividing the current reference generated by the outer voltage control loop. A typical realization is shown in Fig. 2.7(a). Single-wire current sharing method has been studied in literature [42], where current sharing among the paralleled DC-DC converters is achieved using a single wire current sharing control bus (Fig. 2.7(b)). The current sharing bus may be made to carry the information of maximum current command signal or the average of output currents of individual converters. This current command signal is compared with the individual currents and the current-sharing error is injected into the reference voltage. However, in such a scheme, the bandwidth of the current sharing response gets limited by the outer voltage loop. To overcome

this problem, the current-sharing error is injected into the inner current loop as in [43]. The scheme essentially works on the principles of current mode control.

Current-sharing in non-identical power modules has also been achieved by using O-ring connected power supply system [44]. MOSFETs are used as O-ring devices. Here parallel converters are connected through an O-ring architecture to provide power to a common load. Block schematic of such a scheme is shown in Fig. 2.7(c). In such a scheme, current sharing is achieved by selectively controlling the series MOSFETs (O-ring devices), which supplies the load current. In such a scheme, the sensed control variable (I_{sense}) is connected to the current sharing reference bus (I_{CSREF}) via a diode, as shown in Fig. 2.7(d). If the sensed variable is lower than the reference, the series MOSFET will be turned ON to power the load. Since the output currents from individual modules depend upon the output voltage of that module, thus the functionality of the current-sharing interface depends on the variation of output voltages resulting from individual phases. The current-sharing becomes inactive if the difference is less than the diode forward drop. Introducing an additional series MOSFET in current path results in losses and hence is certainly not a good solution for VRM type application.

Alternately, a master-slave architecture is used to ensure current sharing in a paralleled converter architecture [45]. In master-slave current sharing strategy, a dedicated master is included. The output current of the master becomes the reference for remaining modules. Alternately, a rotating master or an automatic master selection scheme can be incorporated. A typical realization of automatic

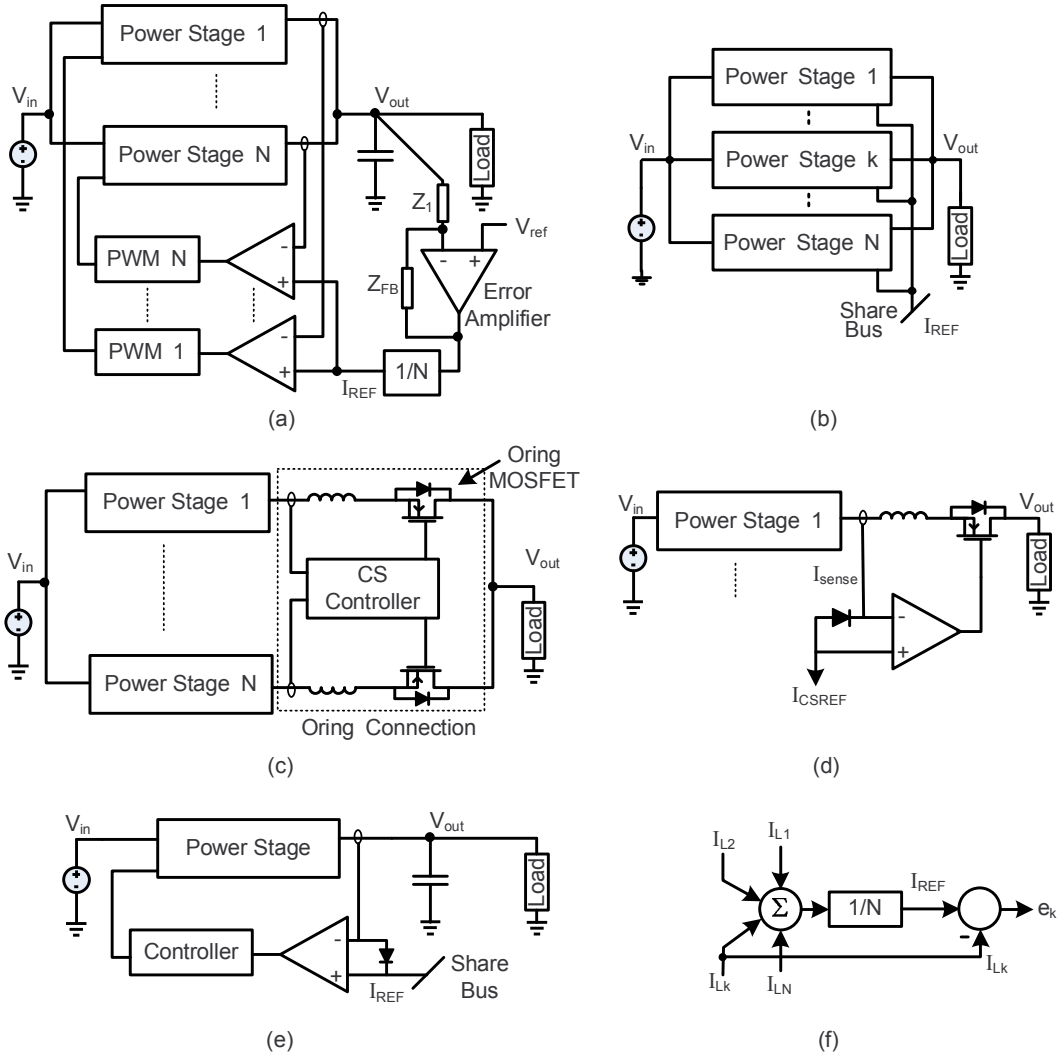

Figure 2.7: Various current sharing schemes: (a) Current Mode control (b) Single wire current sharing scheme (c) Paralleled converters connected with Oring-connection (d) Current Sharing controller used in O-ring architecture (e) An automatic master scheme

master scheme is shown in Fig. 2.7(e). This scheme automatically selects the module with the highest output current to be the master and adjusts the control signal to balance the currents. This type of algorithm provides sharing during steady state operation. However there may be poor current sharing during start-up transient and load transients. Moreover, failure of master will disable the entire system.

To mitigate the disadvantages of Master-Slave current sharing scheme, [46] proposes digital load distribution control. It proposes to increase or decrease the number of parallel converters sharing the load. When the load current increases the number of parallel converters is increased and vice-versa, so that each converter always operates at its nominal output rating. However, this scheme does not utilize the advantages of paralleled operation for all the loads.

Hotswap solution has been proposed in [47], which enables inserting or removing an extra phase without having to re-start the power supply. However, the current sharing interface is based on O-ring architecture. This results in additional losses due to a series MOSFET in each phase.

A voltage-mode hysteretic controller is presented in [11], where the output currents of each phase are sensed and compared with other phases to find the phase that carries the smallest current. The high-side switch of the phase that carries smallest current will be switched ON, while the other phases are turned OFF. Since the controller is based on small hysteresis window around the nominal output voltage, its switching frequency will depend upon the load current and the hysteresis window. Moreover, for a N-phase converter, this scheme would require N*(N-1)/2 comparators.

In [48], a scheme for parallel operation of converters is presented that uses the average of output current of individual converters as the current reference for individual phases. This average can be computed by considering all the phases

or by considering only a few phases at a time. A similar concept is used in most of the commercial products, for example in [49]-[51] the sensed phase currents are compared with the average current command signal. The average is computed by sampling the individual phase currents. The current mismatch error is generated for duty cycle correction. An increase (or decrease) in duty cycle command of a phase results in increase (or decrease) in the phase current.

In all these proposed schemes, the information about individual currents is needed. For a N-paralleled converters, N current sensors would be required. A scheme for estimating the phase current unbalance in N-paralleled converters has been proposed in [52]. It proposes to use the voltage drop at the effective series resistance (ESR) of the input capacitor. The voltage drop due to ESR is proportional to the inductor current of a particular phase during the turn-ON duration of its high-side switch. However, there may be instances when the conduction times of two or more phases overlap, leading to inaccuracy in estimation. Thus it proposes to analyze the harmonic contents of the waveform across the input capacitor. Such a method will be computationally intensive and is not suitable for low cost digital implementations.

It is desired to tightly regulate the output voltage while achieving current sharing among paralleled converters. A simple high-bandwidth voltage mode control method can tightly regulate the output voltage but may not ensure current sharing capability. The current mode control can easily solve the current sharing problem, but it requires individual current loops. It also requires an outer voltage

feedback loop to regulate the output voltage. Can a voltage mode controller be used while still maintaining the current sharing capability? It should be simple to implement, less computationally intensive and should be scalable in nature. To this end, investigations need to be carried out to determine the feasibility of such a controller.

Apart from current sharing, there is also a need to obtain fast transient response in such a system. Many control strategies have been proposed for controlling such a converter so as to obtain the desired steady-state and transient response. The transient response of any power supply is limited by the bandwidth of the feedback control loop [53]. An increase in the bandwidth will improve the transient response only when controllers are in the linear region. At high bandwidth, the controllers get saturated and produce a duty ratio of either 0 or 1. In such a case, the transient response of a converter gets limited by the available slew rate of the inductor current (di_L/dt).

2.5 Improving the Transient Response of a Converter

The rate of change of inductor current depends on the value of circuit inductance and the voltage across the inductance $|di_L/dt| = |v_L/L|$. The magnitude of the slew rate can be increased by increasing the magnitude of the voltage across the inductor or by reducing the inductance value. In the past various methods have been proposed to improve the transient response of the system. Some of these

methods are described below.

Reduction in inductance value can increase the slew rate, however it results in higher inductor current ripple and hence results in higher losses. The inductor current ripple can be kept small by reducing the voltage across the inductor as in [10], where a two-stage conversion is proposed which reduces the input to the second stage. For lower inductor voltages, the reduction of inductance can be achieved while keeping the inductor ripple small. This helps in reducing losses and attaining higher efficiencies. However, the dynamics get limited by the inductance values and the voltage across the inductor.

In [54] a stepping inductance topology is introduced, which has a higher inductance in steady state operation and under the transients the main inductance is shorted leaving only a small inductance. However such a stepping inductance topology has problems of higher voltage swings under inductor current recovery and sudden interruption of inductor current without any freewheeling action. High di/dt during sudden interruption of inductor current and the resulting over-voltage spikes lead to increased electromagnetic interference (EMI) problems. To overcome these, additional circuitry is required to clamp the voltage overshoots, resulting in higher losses. Thus, this method certainly has drawbacks and cannot directly be used for high slew rate applications.

Similarly in [55], coupled inductors have been used. Coupling helps in reducing the steady-state ripple. During transients, the small leakage inductances

determine the response. However, the performance of this scheme depends on the extent of coupling and the leakage inductance.

Apart from reducing the inductance value, transient response is improved by employing feedforward techniques using capacitor current [56] or the output current [57]. These methods suggest using a current transformer to sense the output current or the capacitor current to estimate the load disturbance. However, the leakage inductance and parasitic resistance associated with the current transformer will introduce an additional impedance in the current path. Thus, it will have significant voltage drop during large transients or at high load conditions.

Instead of shaping the converter's dynamics via the feedback loop, [58] tries to modify the load characteristics of the given converter. It proposes to add a load corrector across the load, which is essentially a bi-directional current source which provides the additional load current during a step-up load transient and sinks the excess load current during a step-down load transient. The transient response in such a system will depend on the dynamics of the bi-directional converter.

Non-linear control techniques have also been used to improve the dynamic response. In [59], it is proposed that in order to obtain an optimal response for a step-down load transient the duty cycle must be set to 0% for a specified period of time, keeping the high-side switch always off and then to 100% for an additional time interval, wherein the switch is kept on. The minimum on-times and off-times for the switch cannot be solved numerically. Hence, they are calculated offline using

MATLAB. Moreover, the controller essentially works in open-loop and requires the time instance for the load change to be known in advance, which is not possible for most of the cases.

A hysteresis voltage control is presented in [60], which is based on state-trajectory-prediction. It proposes to control the high-side switch by predicting the capacitor current (i_c) and the output voltage deviation from the desired value. The voltage deviation is minimum when the capacitor current $i_c = 0$. Thus, the high-side switch is turned-off at an instance which will keep the output voltage within the tolerance band. It can enhance the transient response of the buck converter, but the settling time and the voltage deviations gets limited by the inductor and capacitor size.

A similar scheme is presented in [61] and [62], where a capacitor charge balance control method is proposed to improve the transient response. It proposes to saturate the controller during the transients. For a step-up change in load current, it calculates the time durations for which the duty ratio is saturated to its minimum, keeping the switch always off and then next interval in which it is set to its maximum value, wherein the switch is kept on. According to the charge balance principle, when the charge added to the capacitor is equal to the charge removed from the capacitor, the inductor current (i_L) is equal to the load current and the output voltage returns to its reference voltage. This improves the transient response, but the response gets limited by the inductor and capacitor size.

Instead of calculating the minimum on and off times, [63] presents a method which models the linear controller response to that of the optimum control law based on the capacitor charge balance. However, the controller obtained using such a method depends upon the component values and the change in the load current.

Another work on nonlinear control is presented in [64]. It proposes the use of an ADC having non-uniform quantization characteristics. As a result, larger error signals are encoded to a higher value, resulting in the controllers to saturate faster. The use of such an ADC improves the transient response as compared to the case where an ADC having uniform quantization characteristics is used. However, the transient response still gets limited by the converter parameters.

A clamping circuit may also be used to limit the voltage overshoot during a step-down load transient. An inductive clamp circuit has been used in [65]. It proposes the use of an additional inductor and a switch across the output capacitor. During the load transient, the switch is turned-on such that the excess inductor current flows through the path provided by the additional inductor and the switch. This will improve the transient response, however, it will get limited by the inductance and the voltage across it.

In [66] a scheme is presented which proposes to add a diode in parallel to the synchronous MOSFET. During a step down load transient, the MOSFET is disabled and the inductor current is forced to flow through the diode. This results

in higher voltage drop and causes the inductor current to decay faster. However, the voltage across the inductor is still limited to $-(V_{out} + V_D)$, where V_D is the voltage drop across the diode.

The above mentioned methods, either try to reduce the inductance value or incorporate non-linear control action during the load transients. Reducing the inductance results in higher inductor current ripple and hence results in higher losses. On the other hand, a non-linear control action would saturate the controller faster. It would change the speed of the response to disturbance but the maximum slew rate gets limited by the inductance value and the voltage across it. Thus, there are limitations in these past approaches and the maximum slew rate which they can achieve is governed by the fundamental equation $|di_L/dt| = |v_L/L|$.

2.6 Summary

This chapter has briefly summarized the various control methods being used for low voltage/ high current applications. In all these methods, inductor current needs to be sensed for implementing current control or for achieving current sharing in a multiphase interleaved converter. Various current sensing and sharing schemes were discussed in this chapter and their advantages and disadvantages were brought out.

Furthermore, the response of a converter is limited by the slew rate of the inductor current. The schemes which are present in literature, either try to re-

duce the inductance value or incorporate non-linear control action during the load transients. The maximum slew rate they can achieve is dictated by the inductance value and the voltage across the inductor.

In all, state of the art methods of control of voltage regulator modules can be broadly divided in two classes - (a) analog control methods, such as [7], [9]-[11]; and (b) digital control methods, such as [12], [13], [16], [17], [19]-[21]. Due to generic advantages of digital control, it has recently gained popularity. It is also suited for VRM applications due to the available digital interface with the microprocessor. Moreover, developments in FPGAs makes it a useful platform to design digital controllers.

However, digital controllers are associated with finite word length effects and sampling time delay due to presence of zero order hold (ZOH). The next chapter is devoted to the development and analysis of high frequency digital controllers for such applications.

Chapter 3

Digital Control of VRMs

3.1 Introduction

In a typical digital implementation of a voltage mode control system, the output voltage is fed back to the Analog-to-Digital converter (ADC). It is then compared with the voltage reference DV_{ref} , which is a digital word. The reference can be either set inside the digital controller or can be provided from external sources such as the VID word from the microprocessor. The calculated voltage error $V_e(k) = DV_{ref} - V_o(k)$ is sent to the digital controller which produces the required duty ratio command. This duty ratio command is then fed to the Digital Pulse-Width-Modulator (DPWM) to produce the gate signals for the converter. The digital control system for PWM based converters are characterized by the presence of the Zero-Order-Hold (ZOH) due to the nature of DPWM. Therefore the performance of these systems is a function of DPWM switching period. Moreover, the performance also depends on quantization error, round-off and truncation errors.

3.1.1 Controller Design Methods

Controllers have to be designed to achieve desired closed loop performance. In frequency domain method small signal models are used to obtain the controllers in Laplace domain. Based on the small signal models, appropriate voltage and current controllers can be designed to obtain the desired performance of the closed loop system. However, if these controllers are translated to their discrete time equivalents, the resulting closed loop system will have degraded phase margin due to presence of ZOH. To alleviate this problem, direct design is used where the discrete time small-signal models of the plant have to be derived. The discrete time models can be obtained using state-space approach or using the step-invariant model of continuous time plant [13]. For a linear system defined by $\dot{\boldsymbol{x}} = A\boldsymbol{x} + B\boldsymbol{u}$, the system is discretized by using the sampling period T_s, where T_s is the PWM switching period. To get the discrete time state-space model of the form $\boldsymbol{x}(k+1) = \Phi\boldsymbol{x}(k) + \Gamma\boldsymbol{u}(k)$, where $\Phi = e^{A.T_s}$ and $\Gamma = \int_0^{T_s} e^{A\tau}B.d\tau$; Φ and Γ have to be evaluated. Computation of Φ and Γ are intensive and hence approximations have to be used [67]. The accuracy of the calculated value of Φ and Γ using approximate methods, depends on the dynamic range of the elements of matrix A and B. Hence, discrete time models are obtained by substituting $e^{sT_s} = z$ in time domain solution of the continuous time system. This involves computing $x(t) = L^{-1}[(sI - A)^{-1}.B.U(s)]$. In this thesis, frequency domain design and its discrete time equivalent is used. However, the decrease in phase margin due to ZOH produced by DPWM is compensated in the controller design.

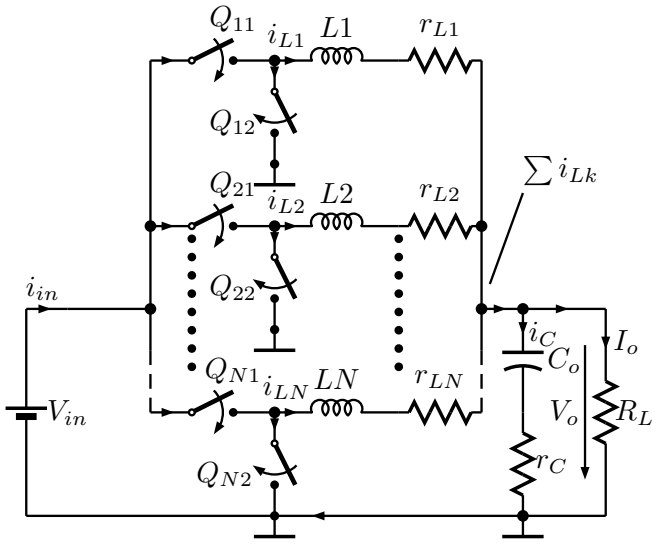

Figure 3.1: N-phase interleaved buck converter

3.1.2 Frequency Domain Design

Interleaved converter is commonly used for VRMs. Fig. 3.1 shows the simplified representation of an N-phase buck converter topology. In order to reduce the output voltage ripple and inductor current ripple, the phases are interleaved at $2\pi/N$ with respect to each other. Based on [68], the small signal control-to-output voltage and control-to-inductor current transfer functions for a 4-phase interleaved converter are obtained.

For a phase ($\#k$) in an interleaved converter, with an inductance of L_k, the parasitics can be decomposed as $r_k = r_{Lk} + r_{ds}$, where r_{Lk} is the series resistance of the inductor L_k, r_{ds} is the on-state resistance of the MOSFET. In Fig. 3.1, r_c is the ESR of output capacitance C_o and R_L is the effective load resistance. For the sake of simplicity, the ESR of the inductance has been ignored and only that

of the output capacitance is considered.

The control-to-output voltage and control-to-inductor current transfer functions are derived as in [69] and are given as:

$$\frac{\widehat{v}_{out}}{\widehat{d}} = \frac{(\sum L_{ijk})R_L s(1+C_o r_c s)V_{in}}{(\prod L)C_o(R_L+r_c)s^2 + ((\prod L) + R_L C_o r_c(\sum L_{ijk}))s + (\sum L_{ijk})R_L}$$
$$\frac{\widehat{i}_{L1}}{\widehat{d}} = \frac{L_2 L_3 L_4(1+C_o(R_L+r_c)s)V_{in}}{(\prod L)C_o(R_L+r_c)s^2 + ((\prod L) + R_L C_o r_c(\sum L_{ijk}))s + (\sum L_{ijk})R_L}$$
$$\frac{\widehat{i}_{L2}}{\widehat{d}} = \frac{L_1 L_3 L_4(1+C_o(R_L+r_c)s)V_{in}}{(\prod L)C_o(R_L+r_c)s^2 + ((\prod L) + R_L C_o r_c(\sum L_{ijk}))s + (\sum L_{ijk})R_L}$$

$$\frac{\widehat{v}_{out}}{\sum \widehat{i}_{Lk}} = \frac{R_L(1+C_o r_c s)}{1+C_o(R_L+r_c)s} \tag{3.1}$$

$$\sum \widehat{i}_{Lk} = \widehat{i}_{L1} + \widehat{i}_{L2} + \widehat{i}_{L3} + \widehat{i}_{L4} \tag{3.2}$$

where $\prod L = L_1 L_2 L_3 L_4$, $\sum L_{ijk} = L_1 L_2 L_3 + L_2 L_3 L_4 + L_1 L_3 L_4 + L_2 L_3 L_4$ and L_1, L_2 .. L_n are the inductances.

Previously reported models of interleaved converters assume all the inductors to be the same, in which case, the problem is reduced to having N synchronous buck converters in parallel. In practice, it is very difficult to have same value for all inductors. There can be $\pm 5-10\%$ variation in the inductor values, resulting in asymmetry in the phases. Moreover, the variations in parameters of semiconductor switches, connections and layout also add to this asymmetry.

The control-to-inductor current transfer functions can be used to study the

effect of inductance variation on the individual inductor currents. As seen from the transfer functions, variations in inductance affects the numerator and hence the gain of the transfer function, whereas the denominator remains same. This results in uneven distribution of load current among the phases. It can be illustrated using Fig. 3.2, which shows the step response of such transfer functions.

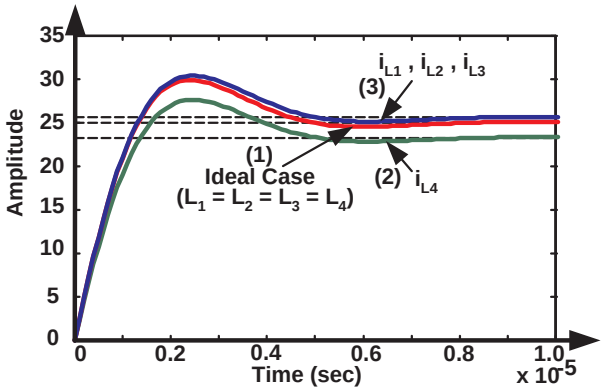

Figure 3.2: Step response of the inductor current transfer functions with parameter mismatch

Fig. 3.2 shows the inductor currents for a 4-phase, 100A converter. In ideal case, each inductor is expected to carry 25A of current, as shown in Fig. 3.2(1). Fig. 3.2(2) shows the inductor current, when L_4 is 10% higher than other inductors, while the balance of the load current is shared by L_1, L_2 and L_3 when $L_1 = L_2 = L_3$ as shown in Fig. 3.2(3).

The tolerances in the inductance play a very important role in distribution of the load current among various phases. The simulation result presented above is useful to understand the problem, but in practice the effect of tolerances appear in all phases simultaneously and which will result in different phase currents. Thus, appropriate current sharing mechanism is required to distribute the current evenly

among the phases. A current mode control is used here to solve this problem.

It has been shown in [10][23] that for VRM type applications, it is advantageous to have the input supply as 5V. Thus, the supply voltage of $V_{in} = 5V$ is chosen for this design. Using the model transfer functions and the given circuit specifications of $V_{in} = 5V$, $V_{out} = 1.25V$, $C_o = 2235\mu F$, $f_s = 1MHz$ per phase, the above transfer functions can be simplified to:

$$\begin{aligned} G_{vd}(s) &= \frac{\widehat{v}_{out}}{\widehat{d}} = \frac{1.207 \times 10^{-4}s + 54}{7.705 \times 10^{-9}s^2 + 2.315 \times 10^{-4}s + 10.8} \\ G_{i_kd}(s) &= \frac{\widehat{i}_{Lk}}{\widehat{d}} = \frac{3.21 \times 10^{-2}s + 8.64 \times 10^{2}}{7.705 \times 10^{-9}s^2 + 2.315 \times 10^{-4}s + 10.8} \\ G_{vi}(s) &= \frac{\widehat{v}_{out}}{\sum \widehat{i}_{Lk}} = \frac{3.492 \times 10^{-8}s + 0.01563}{3.716 \times 10^{-5}s + 1} \end{aligned} \tag{3.3}$$

3.1.3 Control Structure

A typical control structure for 4-phase interleaved buck converter is shown in Fig. 3.3. Here $G_{vd}(s)$ and $G_{i_kd}(s)$ are the control to output transfer functions as derived above. $C_v(s)$ and $C_{ik}(s)$ are the compensators for the voltage and current loop respectively. In this cascaded loop structure, the outer loop is the voltage loop, which provides the current reference for the inner loop. A current limiter for the inductor current is also applied to avoid large inductor current over-shoot.

In order to ensure the switching noise is eliminated from the measurements, one-fifth of the switching frequency is chosen as the crossover frequency ω_c of the inner current loop while maintaining a reasonable phase margin φ_{mi} of around 50^o.

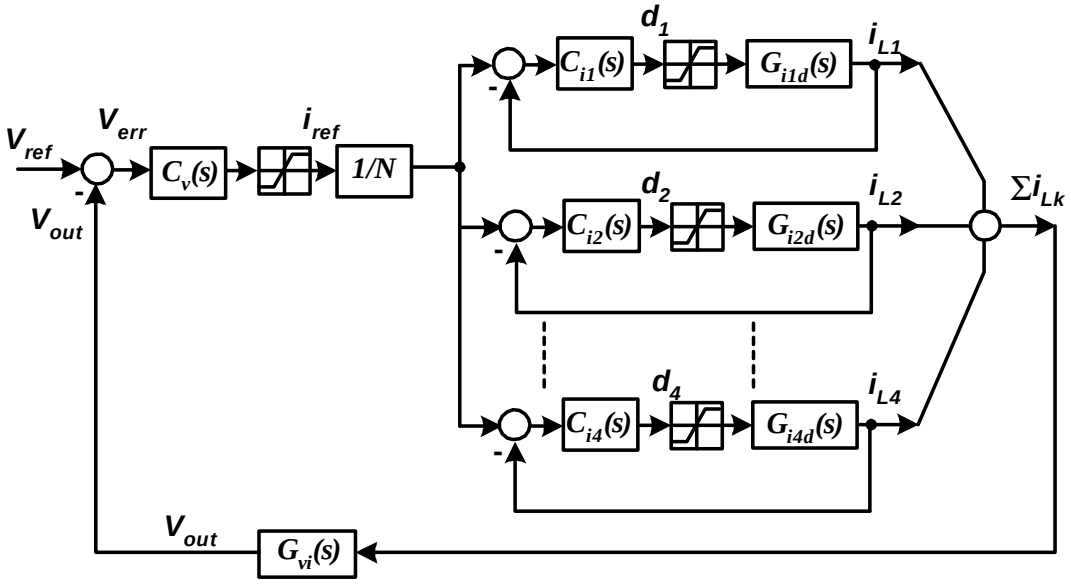

Figure 3.3: Cascaded control loop for 4-phase interleaved VRM

The PI controller for the inner current controllers $C_{ik}(s)$ is obtained as

$$C_{ik}(s) = \frac{0.2304s + 2.441 \times 10^5}{s} \tag{3.4}$$

Similarly, one fifth of the inner current loop crossover frequency is chosen as the outer voltage loop crossover frequency and φ_{mv} is around 60^o. The compensator $C_v(s)$ results in

$$C_v(s) = \frac{212.3s + 1.121 \times 10^8}{s} \tag{3.5}$$

3.1.4 Transformation to discrete-time controller

Having obtained these transfer functions for a multi-loop controller, a digital system needs to be designed such that it has the desired phase margin. The sampling frequency should be chosen such that it is much higher than the open-loop resonant frequency of the converters ($\omega_o = 1/\sqrt{LC}$).

The DPWM based systems are characterized by sampling and the presence of ZOH. Both of these result in delay associated with the hold. The presence of a zero-order-hold (ZOH) introduces a delay of $T_s/2$ which translates to a phase reduction of

$$\Delta\varphi_m = -\frac{\omega.T_s}{2} \tag{3.6}$$

where ω is the gain cross over frequency [67]. This reduction in the phase margin becomes worse when the sampling rate is low. At low sampling frequencies, direct conversion of continuous time controllers to discrete-time controllers may not be suitable.

In the analog system, the phase margin φ_{mv} was chosen as 60 degrees, while in the digital system with different sampling frequencies the system performance degrades with decrease in sampling frequency, as shown in Fig. 3.4. Fig. 3.5 shows the effect of variation in phase margin as a function of sampling frequency. It shows a decrease in phase margin when the sampling rate is reduced.

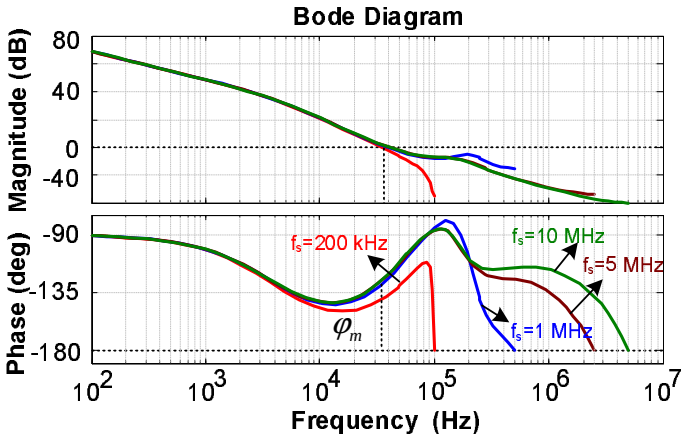

Figure 3.4: Bode plot of the system at various sampling rates

For 1MHz converter, the discrete models with a sampling frequency of 1MHz

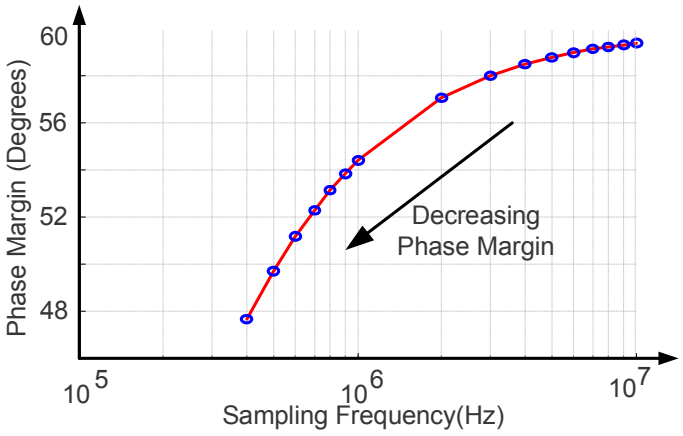

Figure 3.5: Effect of sampling frequency on phase margin of the compensated systems

with ZOH are given as:

$$\begin{aligned} G_{vd}(z) &= \frac{\widehat{v}_{out}}{\widehat{d}} = \frac{0.0189z - 0.01199}{z^2 - 1.969z + 0.9704} \\ G_{ik_d}(z) &= \frac{\widehat{i}_{Lk}}{\widehat{d}} = \frac{4.159z - 4.049}{z^2 - 1.969z + 0.9704} \\ G_{vi}(z) &= \frac{\widehat{v}_{out}}{\sum \widehat{i}_{Lk}} = \frac{9.398 \times 10^{-4}z - 5.249 \times 10^{-4}}{z - 0.9734} \end{aligned} \tag{3.7}$$

The ZOH delay compensated controllers are given as:

$$\begin{aligned} C_v(z) &= \frac{365.5z - 271.4}{z - 1} \\ C_{ik}(z) &= \frac{0.3142z - 0.2869}{z - 1} \end{aligned} \tag{3.8}$$

The bode plots for the continuous and discrete-time designs given in Fig. 3.6. Curve (a) shows the frequency response of the continuous time system, (b) is the response of the digital control system.

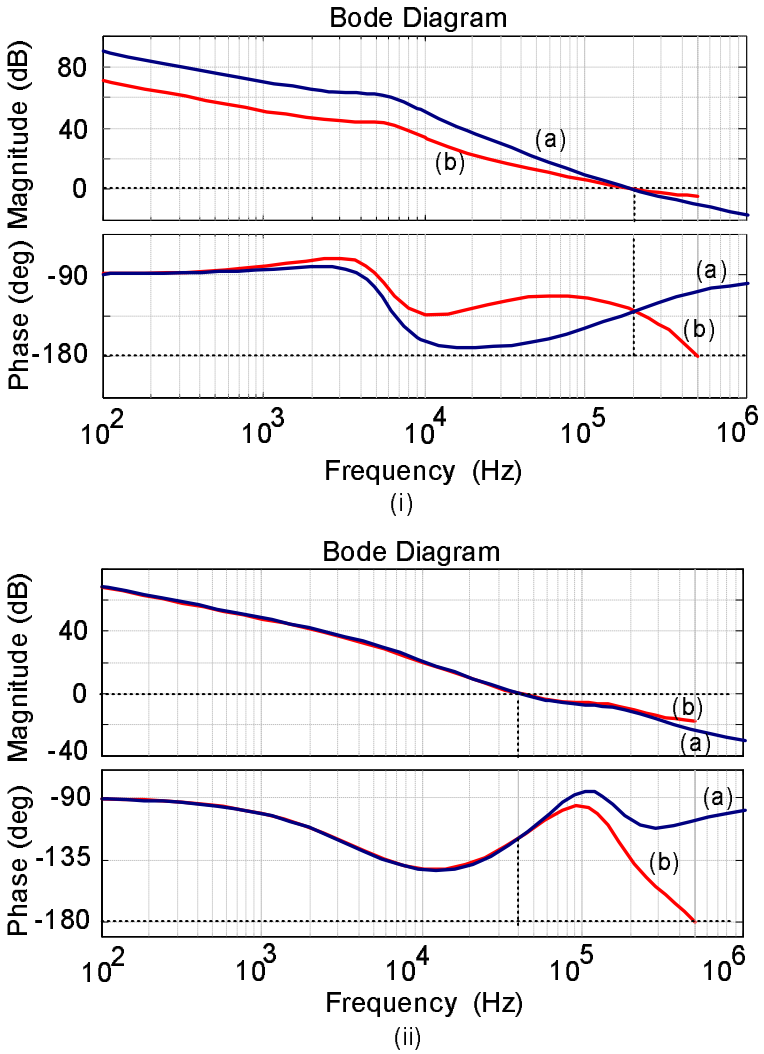

Figure 3.6: Bode plots of the system obtained by different methods. (i) Inner Current Loop (ii) Voltage Loop with inner current loop closed. Curves: (a) Continuous time system, (b) Digital control system

3.1.5 Current and Voltage Sensing

For current control, the inductor current needs to be sensed. Number of methods have been proposed and implemented in the past [70]. Resistive sensing is used for current control. The voltage across the sense resistor is expected to be proportional to the current flowing through it. However, due to parasitic inductance associated with the series resistance, the sensor output will not be proportional to

the current. Thus a simple low-pass RC network is used to filter the voltage across the sense-resistor. One such arrangement is shown in Fig. 3.7(a). For $R_s + sL_s \ll R + 1/(sC)$, the voltage across the series-sense resistor is $v_{sense} = (R_s + sL_s)I_L$, where R_s is the resistance and L_s is the parasitic inductance associated with it. The output of the sense amplifier is

$$v_{sa} = K_{sa}.v_c = \frac{K_{sa}.v_{sense}}{1 + sRC} = \frac{R_s + sL_s}{1 + sRC} I_L \tag{3.9}$$

$$v_{sa} = K_{sa}.R_s \frac{1 + sL_s/R_s}{1 + sRC} I_L \tag{3.10}$$

where K_{sa} is the gain of the sense amplifier. Hence, by ensuring $RC = L_s/R_s$, the sensed voltage will be proportional to the inductor current ($v_{sa} = K_{sa}.R_s.I_L$).

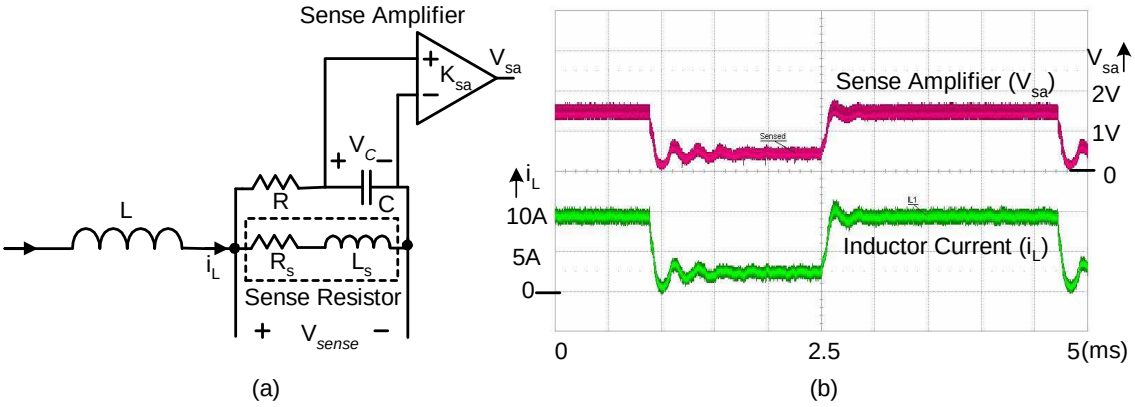

Figure 3.7: (a) Filtering the voltage across the sense resistor to eliminate the effects of parasitic inductance and (b) Output of the sense amplifier and the inductor current as measured using current probe.

Fig. 3.7 shows the current sensing circuit and its performance. The current sensing ratio used is 0.15V/A. Since average current control is desired, the average value of the inductor current can be obtained by sensing the current in the middle of the switch-on and switch-off intervals. In this implementation, resistive sensing is used along with the compensation for the parasitic inductance to sense the av-

erage inductor current(s) by sampling in the middle of the on-time. However sense resistance method is not very efficient for high current operations. The method was used primarily to verify the control and is not a suggested method of current measurement.

For sensing V_{out}, the output voltage is fed to an ADC. In order to eliminate measurement noise, 8 samples are taken within a switching period and averaged over the period to obtain $V_{out}(k)$.

3.1.6 Controller Implementation

The control algorithm takes the sample of the output voltage $V_{out}(k)$ and the inductor current $I_L(k)$ and gives the duty ratio word $D(k)$, which can be used to generate the gate signals for various leaves. The block schematic of a digital controller is shown in Fig. 3.8.

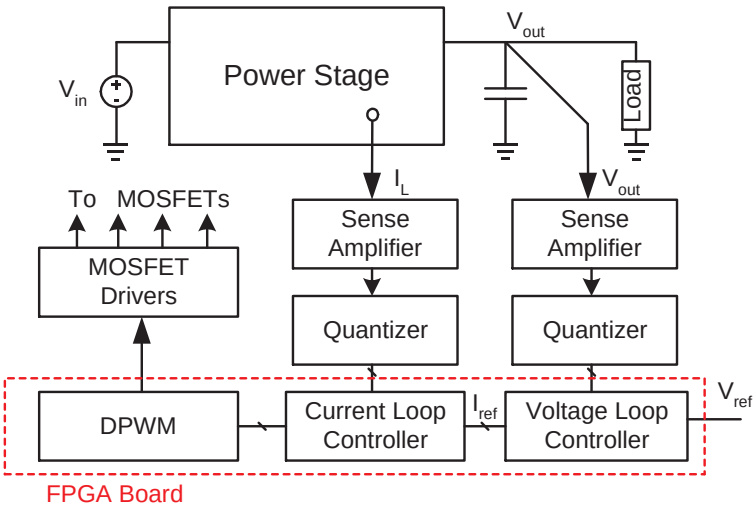

Figure 3.8: Schematic of digital controller design using FPGA

The controllers in eq. (3.8) are designed for a unity gain feedback. Including

the gains of the sensing circuit, the compensator for the equivalent unity feedback gain are:

$$\begin{aligned} C_v(z) &= \frac{I_{ref}(z)}{V_{err}(z)} = \frac{54.83z - 40.71}{z - 1} \\ C_{ik}(z) &= \frac{D(z)}{I_{err}(z)} = \frac{1.351z - 1.233}{z - 1} \end{aligned} \tag{3.11}$$

The controllers obtained above are based on a first order polynomials. These controllers can be re-written in the form of a difference equation. The output of the voltage compensator will give the current reference, whereas the duty ratio will be obtained from the output of the current compensator. Using the set of equations in (3.11), the difference equations are obtained as:

$$\begin{aligned} I_{ref}(k) - I_{ref}(k-1) &= 54.83V_{err}(k) - 40.71V_{err}(k-1) \\ D(k) - D(k-1) &= 1.351I_{err}(k) - 1.233I_{err}(k-1) \end{aligned} \tag{3.12}$$

Since its a first order difference equation, it can easily be realized using direct form of filter structure. Due to the fixed-point nature of the FPGA, a quantization process has to be carried out for the controller coefficients. The quantization process depends on the required precision of the filter coefficients. Such a quantized filter will dictate the word-length requirement for implementation.

Quantization of such a filter may lead to unstable systems when the poles of the filter fall outside the unit circle. Sensitivity of pole-zero locations has been widely studied for stability [67][71]. Though this gives the minimum word-length for stability, it may not give word length requirement for the desired performance.

For example, to implement the controller with a precision up to 2-decimal places, the quantization and rounding off process will require multiplication and division by 100. Since the controller has to be implemented on a digital platform, multiplication or division by powers of 2 can be achieved by using shift operations. Hence no hardware multipliers are necessary. Therefore, the eq. (3.12) is multiplied with $2^7 = 128$ on both sides, as this is closest to 100. Similarly for quantizing the coefficients up to third decimal place, the equation is multiplied by 2^{10}.

In general, for obtaining a precision up to n-decimal places, the coefficients are multiplied with 2^k, where k is given as:

$$k = round(log_2(10^n)) \tag{3.13}$$

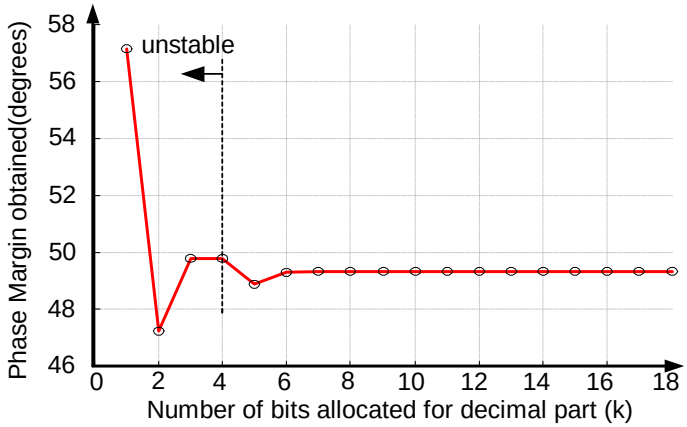

Figure 3.9: Effect of truncation on the filter coefficients in current controller

Fig. 3.9 shows the effect of truncation of the filter coefficients in current compensator. It can be clearly seen that for $k \geq 6$ bits, the performance of the system is not improved much. Using eq. (3.13), 6-bits for the decimal part means the coefficients are used with a precision of 10^{-2}.

Multiplying the equations using k=6 and rounding off the coefficients to the nearest integer, the difference equations are obtained as

$$I_{ref}(k) = [55V_{err}(k) - 41V_{err}(k-1)] + I_{ref}(k-1)$$

$$D(k) = 2^{-6}[86I_{err}(k) - 78I_{err}(k-1)] + D(k-1) \tag{3.14}$$

A filter structure as shown in Fig. 3.10 is used.

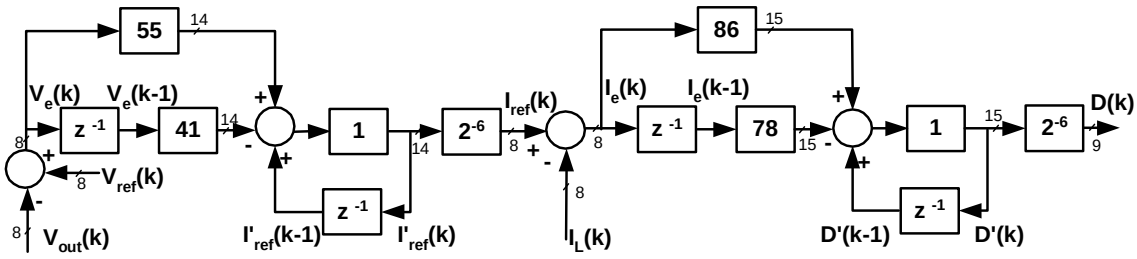

Figure 3.10: Direct Form : Filter realization

In the above realization, if the same truncation process is used for both the controllers, this controller will require 21-bit implementation, where 12-bits represent the coefficients, 1 bit for the sign and 8-bits for representing sampled signal. Different precision is used for the voltage and current controllers without degrading the performance. While the current controller is normalized by 2^6, the voltage controller is obtained by rounding off to give a coefficient format that is multiplied by 2^0. Thus for a 9-bit resolution in the duty ratio, these controllers can be implemented conveniently with 15-bit word size.

3.1.7 Stability Analysis

If the above system is realized using a difference equation, then it is clear that the pole nearest to the unit circle will be most sensitive to change in coefficient. The pole-zero sensitivity was studied to obtain the allowable change in the coefficients so as to have a stable system.

For a characteristic equation of the form

$$z^n + \alpha_1 z^{n-1} + ... + \alpha_n = 0 \tag{3.15}$$

which has roots $\lambda_1, \lambda_2..., \lambda_n$, the sensitivity of the roots due to change in coefficients can be obtained as in [67]

$$\delta\lambda_j = -\frac{\lambda_j^{n-k}}{\prod_{l\neq j}(\lambda_j - \lambda_l)}\delta\alpha_k \tag{3.16}$$

For example, the inductor current to duty ratio transfer function and the current controller is defined as

$$\begin{aligned} G_{ikd}(z) &= \frac{4.159z - 4.049}{z^2 - 1.969z + 0.9704} \\ C_{ik}(z) &= \frac{Az + B}{z - 1} \end{aligned} \tag{3.17}$$

The characteristic equation of the closed current loop can be obtained as $z^3 + (4.159A - 2.969)z^2 + (2.939 - 4.049A + 4.159B)z + (-4.049B - 0.9704) = 0.$

The poles of the closed inner loop are located at $z_1 = -0.21675$, $z_2 = 0.90505$ and $z_3 = 0.97385$. Thus a change in the coefficient by $(1 - 0.97385)$ will move the

pole to the unit circle and lead to instability. Hence the sensitivity of coefficients of the characteristic polynomial is given as $\delta\alpha_1 = -0.30271$, $\delta\alpha_2 = -0.31083$ and $\delta\alpha_3 = -0.31918$. These changes correspond to the following changes in coefficients A and B of our current controller as defined in eq. (3.17),

$$\Delta A \leq 0.0727, \Delta B \leq 0.0788 \tag{3.18}$$

Thus, in order to maintain a stable system, the change in coefficients should satisfy eq. (3.18). Thus the number of bits required for such sensitivity can be obtained as $log_2(min(\Delta A, \Delta B)) = 4$ bits.

This can be verified from Fig. 3.9, which shows the effect of truncation of the filter coefficients. As seen from the Fig. 3.9, the system is unstable if less than 4-bits are allocated for the fractional part. But keeping the system stable is not sufficient. We need to obtain the desired performance as well. If more than 6-bits are allocated for the fractional part, there is no significant improvement on the system performance. Thus the compensator can be obtained by normalizing with 2^{-6}.

Similarly the location of closed voltage loop poles can be obtained as $z_1 = 0.97344$, $z_2 = 0.91148$, $z_{3,4} = 0.8926 \pm i0.1493$ and $z_5 = -0.4835$. Clearly, the pole located close to the unit circle will be most sensitive to coefficient change. For this to happen, the compensator coefficients A and B should change by $\Delta A \leq 7.45, \Delta B \leq 1.67$. Thus, the voltage compensator can be obtained by rounding off process.

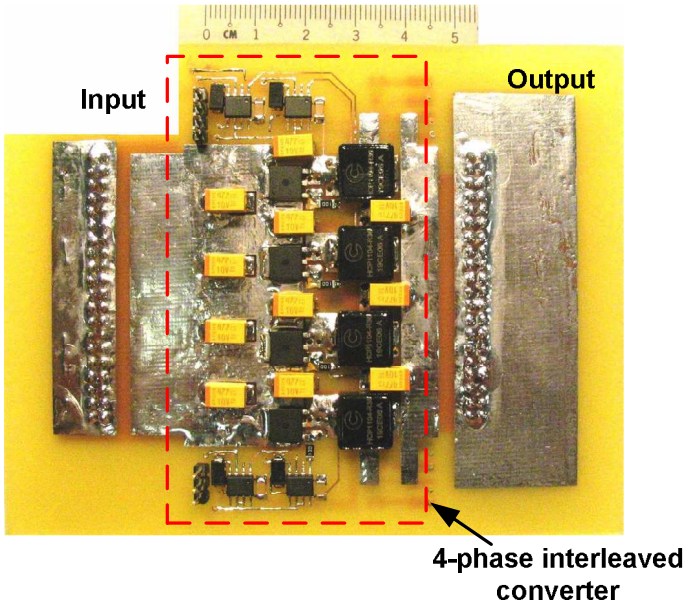

Figure 3.11: Photograph of the prototype of a 4-phase interleaved converter developed in the lab

3.1.8 Digital Dither

It has been shown that [17], if the resolution of ADC is greater than the resolution of the digital PWM (DPWM) counter and there is no integral control action, a limit cycle oscillation occurs. Therefore, it has been recommended that the resolution of DPWM be at least 1 bit higher than that of ADC. Digital dithering technique is used to improve the resolution of the DPWM modules, where the resolution of the DPWM counter is lower than the resolution of the ADC. It involves varying the duty cycle by an LSB over a few switching cycles, such that intermediate sub-bit level duty ratios are achieved. This is illustrated in Fig. 3.12(a). Here D and $(D+1)$ are the adjacent quantized duty ratios from the DPWM counter. If the duty ratio is allowed to alternate between D and $(D+1)$, an average duty ratio of D+(1/2)LSB is achieved. This realizes (1/2)LSB DPWM level which is equivalent

to an increase in resolution by 1-bit. This concept can be extended further to achieve 2-bit effective increase in DPWM resolution. In such a scheme, $(D+1)$ is introduced once every four switching periods, as shown in Fig. 3.12(b). Doing so, (1/4)LSB DPWM levels are obtained which is equivalent to an increase in DPWM resolution by 2-bits. It may be noticed that various dithering patters are possible, but not all will result in same improvement in resolution. For example, if two out of four switching periods are dithered, it will result in (1/2)LSB DPWM levels. Likewise, if all the switching periods are dithered, it will not result in an improved DPWM resolution as the overall duty ratio is increased to $(D+1)$. Thus, for a 2-bit increase in effective resolution, dither patterns of (1000), (0100), (0010) or (0001) may be used.

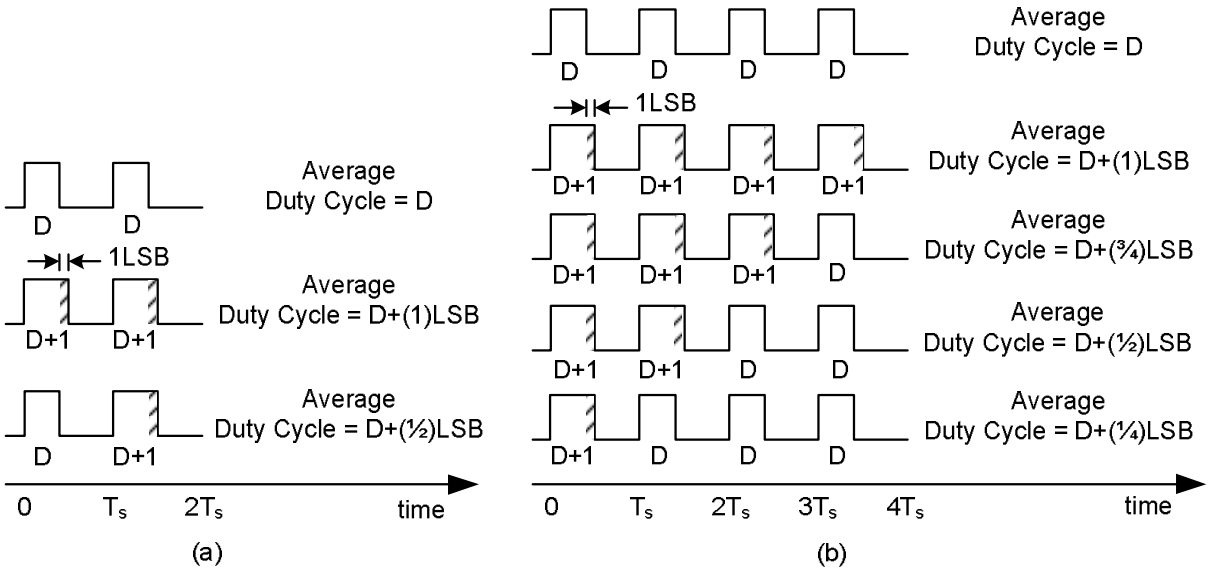

Figure 3.12: (a) Switching waveform patterns to realize 1-bit dither; (b) Switching waveform patterns to realize 2-bit dither.

Fig. 3.13 shows some of the switching waveform patterns for 3-bit dither sequence. When $(D+1)$ is introduced once every eight switching periods, (1/8)LSB

DPWM levels are obtained which is equivalent to an increase in DPWM resolution by 3-bits. For a dither sequence, there may be a different patterns which result in same improvement in DPWM resolution. For example, a dither pattern of (11000000), (10100000), (10001000) etc will result in a sub-DPWM level of (2/8) LSB. While (11000000) has lower fundamental frequency and thus produces higher output voltage ripple, (10001000) will produce a lower ripple and have high fundamental frequency. Thus, it is also important to select the dither pattern which results in low output voltage ripple.

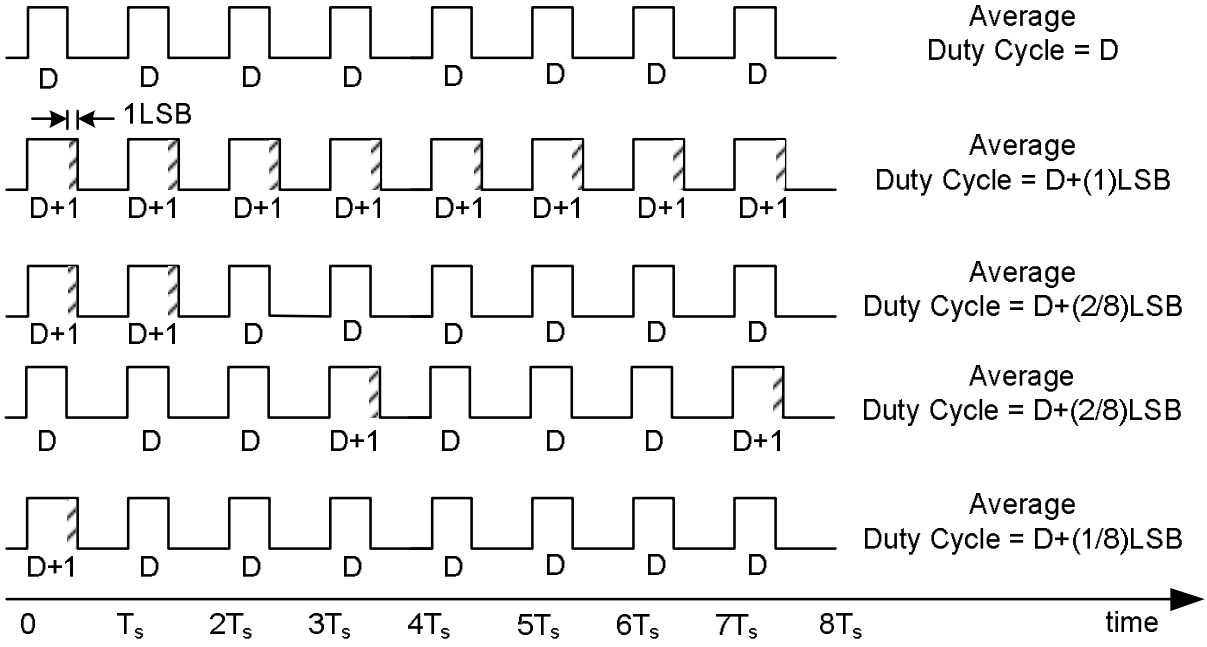

Figure 3.13: Switching waveform patterns to realize 3-bit dither.

3.2 Experimental Results

Fig. 3.11 shows the photograph of the prototype of the 4-phase interleaved converter. Due to large rate of change of the inductor current, it becomes necessary to reduce the stray inductances. A parasitic inductance at the input side results in

an overshoot in the switch voltage (V_{ds}) during its turn-off. Due to the parasitic inductance, the overshoot in V_{ds} of the top-side MOSFET was obtained as 6.9V, when the current is switched off from 24A to 0A in 11.2ns. The parasitic inductance can be calculated as 3.2nH. This overshoot results in higher switching losses, which forms a major component of total losses especially in the converters operating at high switching frequencies. Effort can be made to reduce the stray inductance of the circuit, but it gets limited by the package inductance. Typical stray inductance of a TO-220 package at 1MHz is 12nH, D2-PAK(TO-263) offers around 5nH and D-PAK(TO-252) offers around 2.5nH of package inductance [72]. Hence D-PAK MOSFETs were chosen for this design and effective input side inductance was observed to be 3.2nH. Package inductance of D-PAK(TO-252) alone will result in an overshoot of 5.8V and in our case an overshoot of 6.9V was observed.

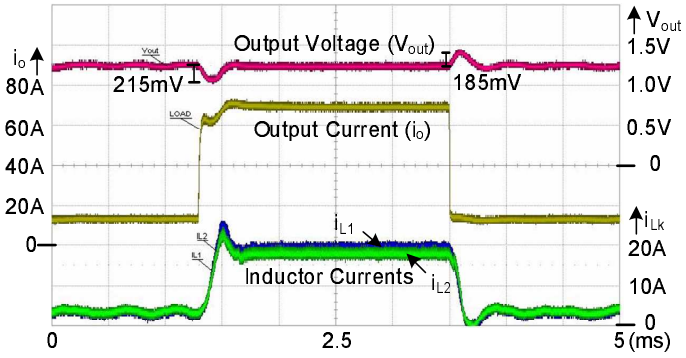

Figure 3.14: Result showing the dynamic response of digitally controlled 4-phase interleaved converter for a step load variation from 15A to 70A

The controller performance was tested on the 4-phase interleaved buck converter prototype with the following parameters: $V_{in} = 5V$, $V_{ref} = 1.25V$, $L = 1.2\mu H$, $f_s = 1MHz$ per phase. In the prototype, the ADC had 8-bit resolution and DPWM had 6-bit of hardware resolution. Thus, 3-bit digital dither was intro-

duced to increase the effective resolution of DPWM module to 6+3=9 bits. The calculated duty ratio was incremented by one, once every eight switching periods. This achieves a DPWM level of (1/8)LSB which is equivalent to an increase in DPWM resolution by 3-bits. The digital control algorithm has been implemented on a Spartan-3 Field Programmable Gate Array (FPGA) by Xilinx. The system was tested for load transients with a step-up change from 15A-70A and vice versa. Fig. 3.14 shows the dynamic response of the controller, when reference voltage is set as 1.25V. The load transients were generated by switching the load resistance.

The results shown above were to test the performance of the controllers. In practice the VRM output requires adaptive voltage positioning (AVP). In adaptive voltage positioning, the output voltage of the VRM is adapted to changes in the load. This causes the output voltage to droop with the load. Adaptive voltage positioning was implemented by changing the reference voltage in accordance with the load current. Reference voltage is defined as

$$v_{ref} = V_{ref} - i_o.R_{droop} \tag{3.19}$$

where V_{ref} is the nominal reference voltage at no load conditions, i_o is the load current and R_{droop} is the droop resistance obtained from the load line. In AVP, the output voltage is always positioned at a variable reference voltage v_{ref}, instead of a fixed reference voltage V_{ref}. Thus the converter behaves as a voltage source with an output impedance of R_{droop}.

Fig. 3.15 shows the dynamic response of the controller with adaptive voltage

positioning with a droop resistance of $R_{droop} = 1.5m\Omega$. It shows a droop of around 100mV for a load change from 15A to 80A. The output settles to the new reference voltage without any overshoot, thereby showing good damping of the system. Current sharing among various phases was also achieved during load dynamics.

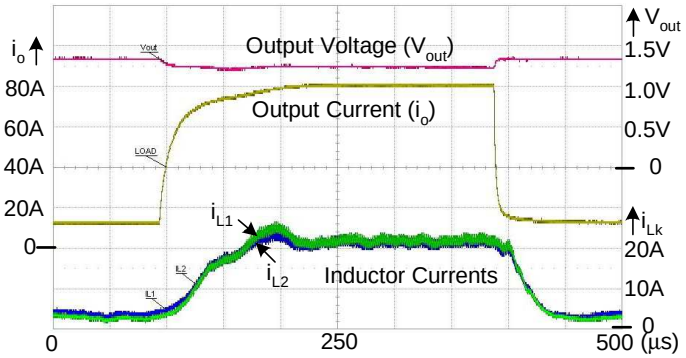

Figure 3.15: Result showing the dynamic performance of the controller with adaptive voltage positioning for a step load change from 15A to 80A

3.3 Summary

This chapter discussed the methods for obtaining the desired output voltage regulation in VRMs. An interleaved converter topology is commonly used for VRM applications. However, due to variations in component values among various phases, it results in current mismatch among individual phase currents. To mitigate this, controllers are designed for a 4-phase interleaved converter, which takes into account the variations among individual inductor currents. The digital controllers are designed taking into account the reduction in phase margin due to presence of DPWM based ZOH. The effect of quantization of filter coefficients is also analyzed and a minimum word length filter structure is proposed for such controllers.

Table 3.1: Parameters of the interleaved buck converter prototype

N	Number of Phases	4
V_{in}	Input Voltage	5V
L_k	Phase Inductors	$1.2\mu H$
C_o	Output Capacitor	5x470μF
V_{ref}	Reference Voltage	1.25V
ΔI_o	Load Step	65A
R_{droop}	Droop Resistance	$3m\Omega$
f_s	Switching Frequency	1MHz per phase
f_{si}	Sampling Frequency of Inductor Current	1MHz
N_{ADC}	ADC Resolution	8 bits
N_{DPWM}	DPWM Resolution	6 bit + 3 bit (dither)
f_{CLK}	System Clock Frequency	50MHz

The reduction of phase margin can be compensated in the controller design. However, the output regulation still depends upon the resolution of the duty ratio. The fine duty ratio either requires the switching frequency to be lowered or the clock frequency to be increased. The next chapter discusses the DPWM architecture and proposes to improve the time resolution of the gate pulses without having to increase the clock frequency.

Chapter 4

Time Resolution of the DPWM

4.1 Introduction

The digital controllers employ a Digital Pulse-Width Modulator (DPWM) to control the duty ratio of the gate pulses. However, the time resolution of the DPWM output depends upon its clock frequency. In general, for achieving N-bit resolution of the DPWM block, it needs to be clocked at $2^N.f_s$, where f_s is the switching frequency of the converter. To meet, the high switching frequency demand along with high resolution of DPWM, various methods have been proposed in the past. Such methods above can be broadly classified into following categories:

- introducing a dither in the DPWM output [17],
- using a customized DPWM architecture e.g ring-oscillator-multiplexer scheme [18], tapped delay-line [24], [25], etc,
- increasing the clock frequency [30].

The schemes based on customized DPWM architecture results in increased silicon area and power consumption, which is undesirable. On the other-hand, the schemes based on DLL and counter-based DPWM are not scalable in nature and provides resolution improvement only for a limited range. To this end, a scheme is proposed which does not multiply the clock-frequency, requires a few additional gates and is scalable in nature. The proposed scheme is also well suited for integration with the existing DPWM schemes.

4.2 Proposed Scheme

A counter based DPWM scheme is easier to implement but its time resolution gets limited by the clock edges. Unlike conventional counter based DPWM scheme, we propose a hybrid approach to improve the DPWM resolution. In this scheme, the processing is done in digital domain and a high resolution duty ratio word ($D(k)$) is obtained from the digital compensator. The counter based DPWM block handles the upper significant bits while the duty ratio correction block handles the remaining lower significant bits. The duty ratio correction block adopts a fine phase shift technique which can shift the input gate pulse by a fraction of clock period. By delaying the turn-off instance of the gate pulses, the time resolution of such pulses can be increased. The time resolution is now a function of the phase shift introduced in the signal, instead of the clock edges. A combination of resistors and a capacitors are used to provide a phase shift in the turn-off instances. The required values of these components can be easily realized in silicon and is thus

well suited for integration.

The basic principle of such a scheme and the typical waveforms are shown in Fig. 4.1. The working of this scheme can be explained as following: The PWM pulse obtained from DPWM is used to charge up an RC network. By using appropriate values of R and C, the delay in such a system can be controlled. If the input pulse is D, the shifted waveform is obtained as D_{new}, which has the same duty ratio as that of D. However, D_{new} will have a shift introduced at both turn-on and turn-off instances of the input gate pulse. To mitigate this, an OR gate is used for D and D_{new}. The output of the OR gate, D_{out} will have a shift in the turn-off instance alone. This shift is a function of the R and C values and helps in increasing the time resolution of the duty-ratio pulses. The improvement in time resolution can be obtained by observing the RC charging waveform.

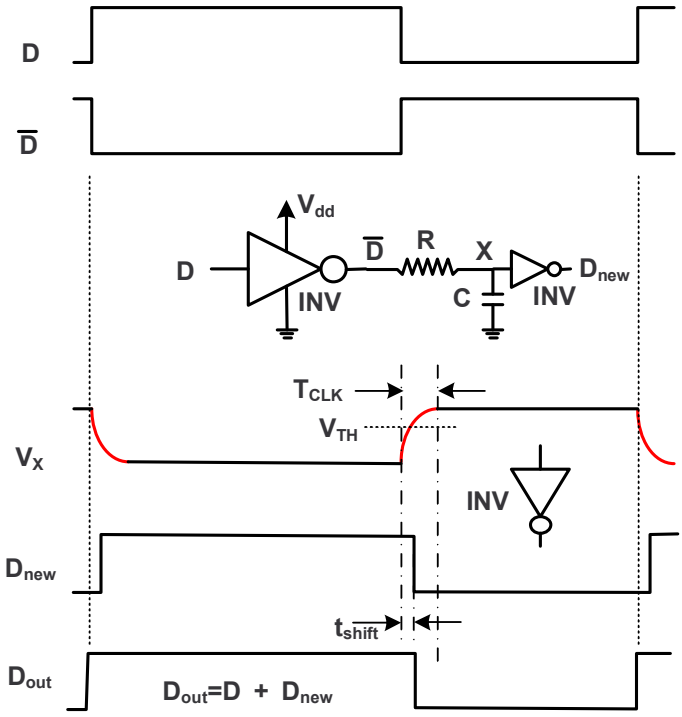

Figure 4.1: Schematic of the scheme for delaying the edges of the gate pulses

Consider a pulse of magnitude V_{dd} charging the capacitor. The capacitor voltage at time t is given as

$$v_c = V_{dd}(1 - e^{-t/RC}) \tag{4.1}$$

If the threshold voltage for the inverter is V_{TH}, the time taken by capacitor voltage to reach V_{TH} can be obtained by solving

$$V_{TH} = V_{dd}(1 - e^{-t/RC}) \tag{4.2}$$

Thus, the time-shift in gate pulse is obtained as

$$t_{shift} = -RC \cdot log_e(1 - \frac{V_{TH}}{V_{dd}}) \tag{4.3}$$

As a design example, we choose $V_{TH} = V_{dd}/2$ and the shift is obtained as $t_{shift} = 0.693RC$. In the conventional counter based DPWM block, the time resolution of the PWM pulses is limited by the clock period. As a result, the duty ratio resolution is T_{CLK}. By choosing appropriate RC, the shift can be controlled such that $t_{shift} = T_{CLK}/2$ and the time resolution can be improved to $T_{CLK}/2$.

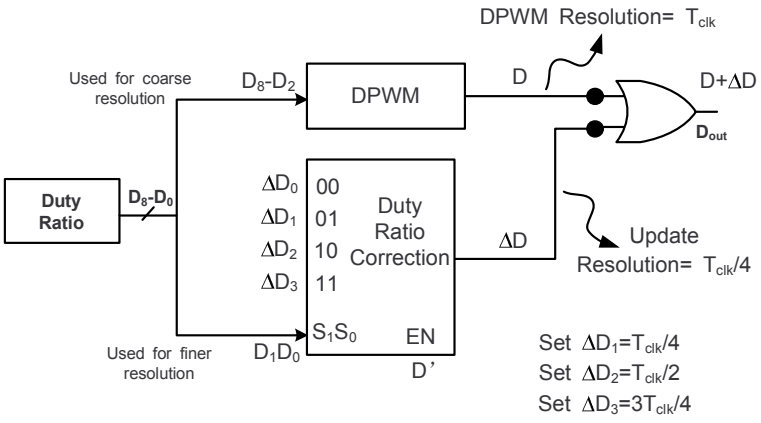

Figure 4.2: Block schematic of the proposed scheme. The duty ratio is updated based on the least significant bits.

4.2.1 Extending the scheme for finer resolution

The scheme presented above can be extended to obtain finer resolution. The block schematic for improving the time resolution to $T_{CLK}/4$ is shown in Fig. 4.2. In such a scheme, the processing is done in digital domain and a high resolution duty ratio word ($D(k)$) is obtained from the digital compensator. The counter based DPWM block handles the upper significant bits while the duty ratio correction block handles the remaining lower significant bits. The resolution of the duty ratio word is increased using the state of the lower significant bits. Here, a 9-bit duty ratio word ($D_8 - D_0$) is obtained from the digital compensator. The DPWM block handles the upper significant bits $D_8 - D_2$ and generates the pulses with coarse resolution. The scheme then updates the PWM pulses with ΔD_1, ΔD_2 or ΔD_3 depending upon the state of lower significant bits (LSB) $D_1 D_0$. Here ΔD_1, ΔD_2 and ΔD_3 are obtained according to the appropriate RC delays such that

$$\Delta D_1 = \frac{1}{4} T_{CLK} \tag{4.4}$$

$$\Delta D_2 = \frac{1}{2} T_{CLK} \tag{4.5}$$

$$\Delta D_3 = \frac{3}{4} T_{CLK} \tag{4.6}$$

Doing so will obtain the time resolution of $T_{CLK}/4$. It can be extended further by increasing the size of duty ratio correction block. The detailed schematic of the duty ratio correction block is shown in Fig. 4.3. A coarse duty ratio (D) is obtained from the counter based DPWM block as described above. The duty ratio correction block updates the PWM pulses with ΔD_1, ΔD_2 or ΔD_3 depending upon

the state of lower significant bits D_1D_0. Based on D_1D_0, only one of the shifted pulses will be available which is used to obtain the finer resolution pulses as D_{out}.

The scheme shown above provides 4x improvement in time resolution. It can be extended further by increasing the size of the duty ratio correction block. However, the extent of duty ratio correction will depend upon the matching of the resistances and capacitances for providing various time shifts. If the precise matching is not available, laser trimming or factory calibration process can be used for fine tuning the time shifts of duty ratio correction block.

In comparison, the proposed hybrid approach is similar to the delay-line and a multiplexer based approaches. Such approaches use a number of delay cells to realize a ring oscillator operating at the switching frequency. The power consumption is governed by the number of delay cells and the switching frequency. Unlike the other hybrid approaches, one delay cell is used at a time and the power to the rest of the delay cells is shut down. Since only one of the delay cells in the duty ratio corrector is used, it helps in reducing the dynamic power of the system.

4.2.2 Effect due to variation in component values

The proposed scheme uses resistors and capacitors to generate the shift in the duty ratio pulse. However, in practice there will be variations in the component values due to process mismatch. Thus, it is important to evaluate the effect of process variations. It has been established that in order to achieve a time resolution

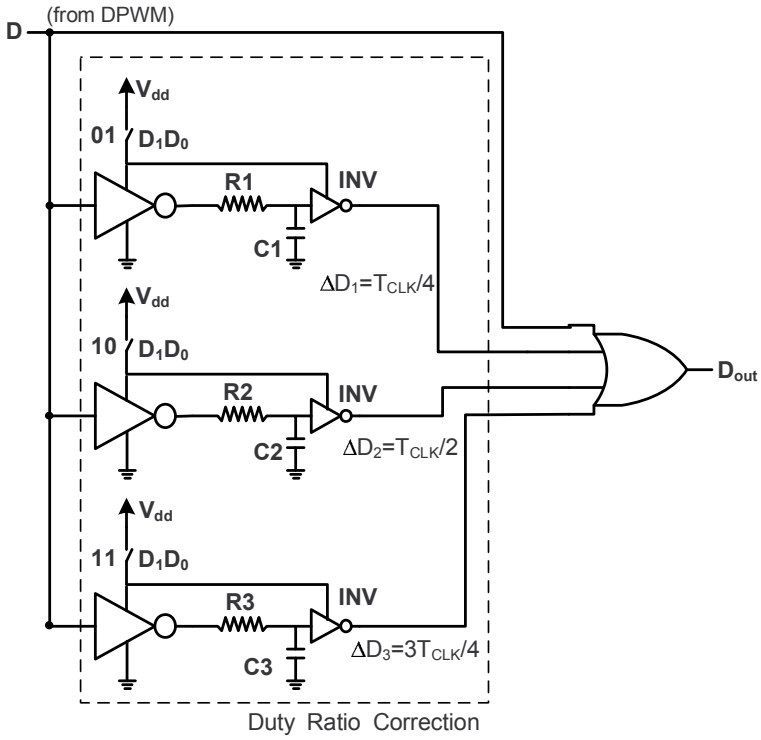

Figure 4.3: Detailed schematic of the proposed scheme. The duty ratio is updated based on the least significant bits.

of $T_{CLK}/2$, we have

$$t_{shift} = 0.693RC = T_{CLK}/2 \tag{4.7}$$

For a clock frequency of 50MHz, we may set $C = 1pF$ and $R = 14.43k\Omega$. The effect on time-shift due to component variations is obtained as

$$\partial t_{shift} = 0.693(R \cdot \partial C + C \cdot \partial R) \tag{4.8}$$

where ∂R and ∂C is the change in resistance and capacitance respectively. Thus if there is $\pm 5\%$ variation in the component values, the worst case change in delay will be $\pm 2ns$, which is within the desired resolution band of $T_{CLK}/2$.

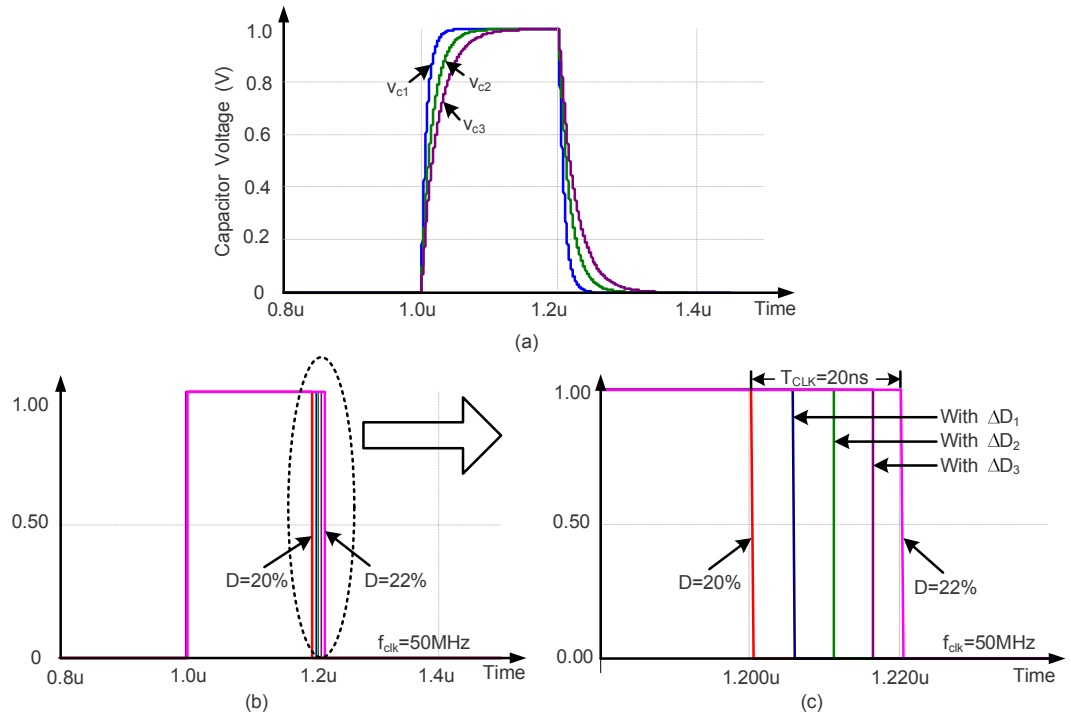

Figure 4.4: Simulation results showing the performance of the proposed scheme. (a) Resulting voltage waveforms at capacitors C1, C2 and C3; (b) The PWM pulses obtained using the proposed scheme and (c) The 4 possible duty ratios generated using the proposed scheme.

4.3 Simulation Results

The performance of the scheme for obtaining finer duty ratio was tested on Simplorer circuit simulator [73]. Fig. 4.4 shows the resulting waveforms. A clock frequency of $f_{CLK} = 50MHz$ was chosen to demonstrate the concept. Such clock frequencies are common on FPGA based development board and will provide a time resolution of $T_{CLK} = 20ns$. For $5V$ to $1V$ conversion, a typical duty ratio of 20% is produced. For a counter based DPWM, this corresponds to a duty ratio command of $D(k) = 10$. A next higher duty ratio command is $D(k) = 11$, which is equivalent to 22% duty ratio. By choosing the appropriate RC time constants,

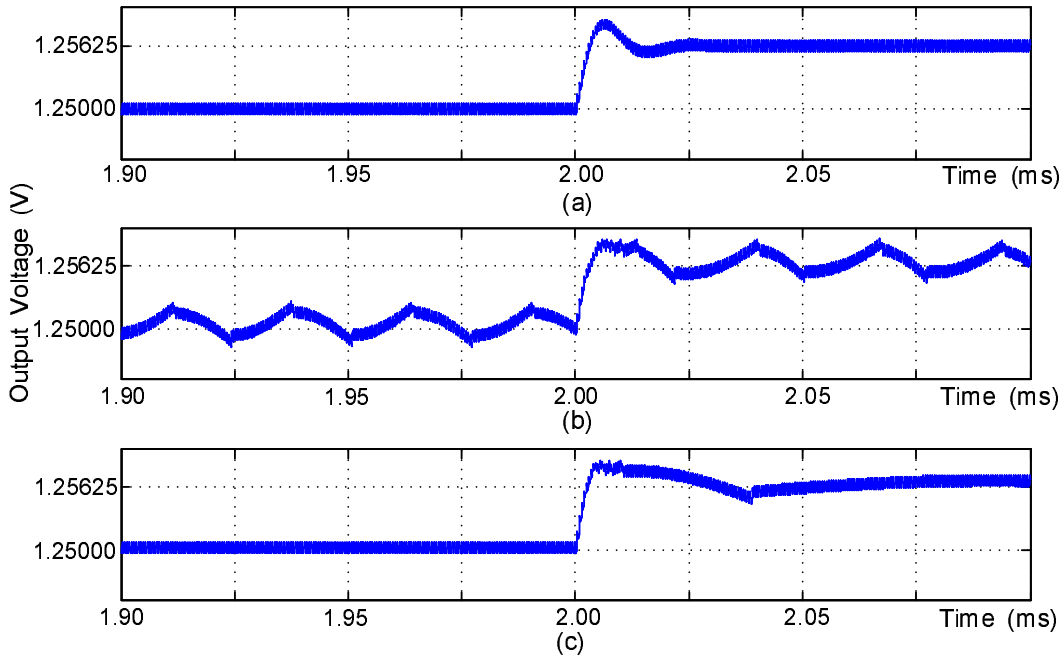

Figure 4.5: Simulation results showing the performance of three different control methods: (a) Analog control; (b)Conventional Digital Control and (c) Proposed Controller with duty ratio correction

a time resolution of $T_{CLK}/4$ is obtained. Fig. 4.4(a) shows the resulting voltage waveforms at different capacitors and the obtained duty ratio pulses are shown in Fig. 4.4(b)(c).

The performance of the proposed control scheme was tested on a buck converter with the following specifications: $V_{in} = 5V$, $V_{ref} = 1.25V$, $L = 1.2\mu H$, $C_o = 1000\mu F$, $f_s = 1MHz$. Three different control methods were simulated. The system was subjected to a change in reference voltage in steps of 6.25mV, which is equivalent to a change by 1 bit in a 7-bit VID word. The reference step was given at $t = 2ms$. Fig. 4.5 shows the comparison of three schemes. As seen from the results, the analog controller settles to new reference voltage in $10\mu s$, while the digital controller with 8-bit DPWM undergoes limit cycle oscillations due to poor

resolution in time. On the other hand, the proposed controller with 8-bit coarse and 2-bit duty-correction also settles to the new reference without any limit cycle oscillations.

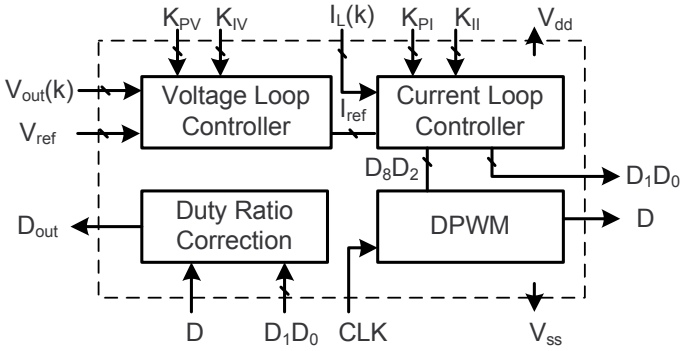

Figure 4.6: Block schematic of the chip architecture

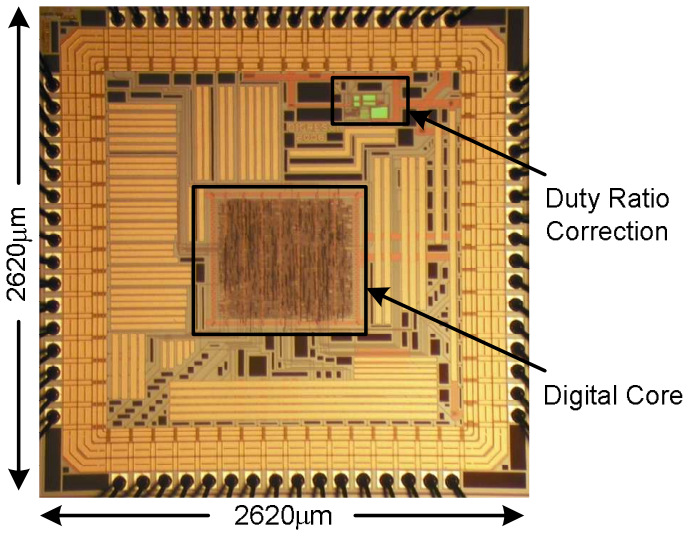

Figure 4.7: Micrograph of the fabricated ASIC, named DigResv1

4.4 Experimental Results

An Application Specific IC (ASIC) comprising of the digital controller and the duty ratio corrector was fabricated in Austria Micro-Systems (AMS) 0.35μm CMOS process. The chip architecture is shown in Fig. 4.6. It implements a

current mode control for a single phase DC/DC converter. The output voltage and inductor current are sampled using an external ADC. Five bit inputs are used for the proportional and integral gains of the digital controllers, which can be set from outside. The DPWM output and the two LSBs are brought out for monitoring purposes. The chip also has a provision of testing the duty ratio corrector alone externally supplying D and D_1D_0. Due to large number of test pins, the chip area was limited by the required I/O cells. Fig. 4.7 shows the micrograph of the fabricated chip. The digital core occupies an area of $877\mu m \times 796\mu m$, whereas the duty ratio corrector occupies only $138\mu m \times 200\mu m$.

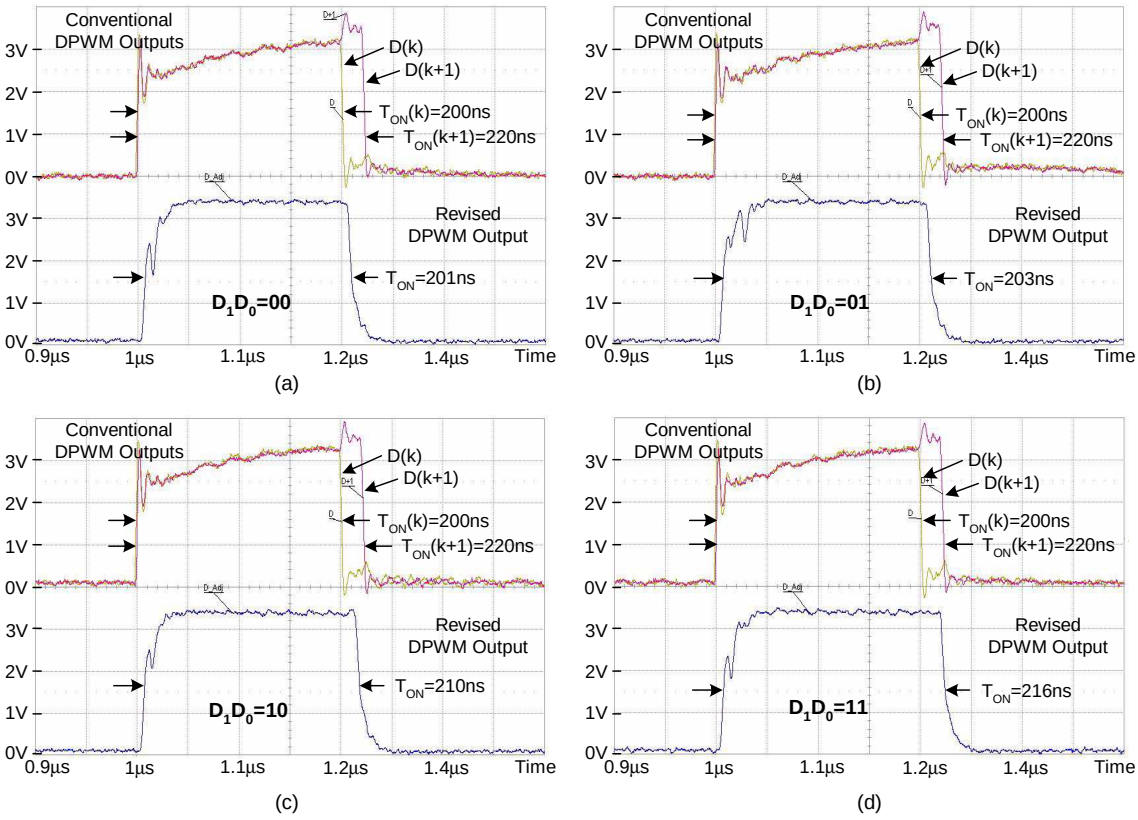

Figure 4.8: Experimental results showing the variation of duty ratio in accordance with duty-ratio correction command (D_1D_2)

For a controller working with $50MHz$ clock, the duty ratio resolution is T_{CLK}

(=20ns). In order to test the functionality of the duty ratio correction block, a $1MHz$ clock with a duty ratio of 20% ($T_{ON} = 200ns$) is generated using an FPGA board and is given as an input (D). The next higher duty ratio of 22% ($T_{ON} = 220ns$) is also captured for reference. As expected the time separation between $D(k)$ and $D(k+1)$ is observed as 20ns. With $D(k)$ as an input to the duty ratio corrector, the correction command (D_1D_0) is varied and the revised DPWM output observed for the given 4 cases (D_1D_0 = 00, 01, 10 and 11). Fig. 4.8 shows the corrected duty ratio pulses. For an input ON period of 200ns, the ON periods of 201ns, 203ns, 210ns and 216ns are obtained which are quite close to the expected durations of 200ns, 205ns, 210ns and 215ns. As seen from the experimental results, a resolution of $T_{CLK}/4$ (=5ns) is obtained which is 4-times improvement over the conventional scheme.

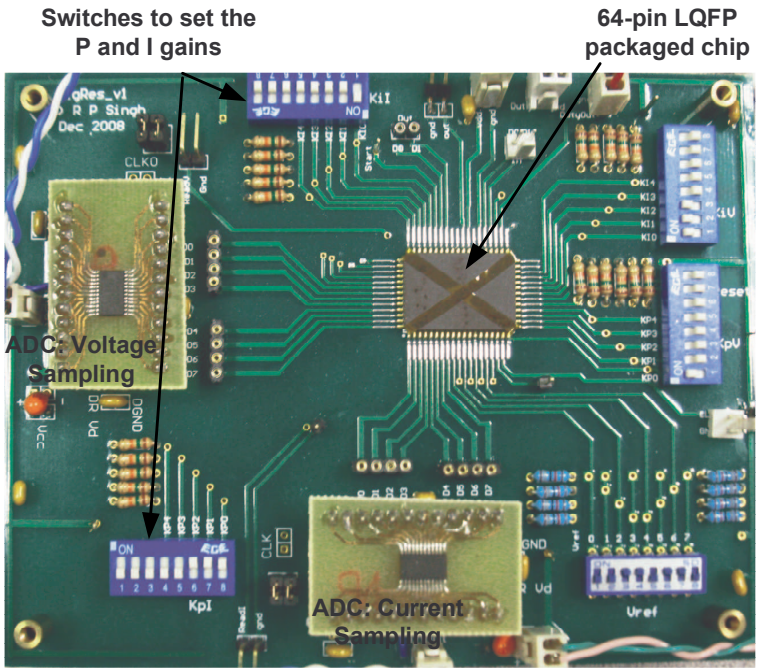

Figure 4.9: Experimental prototype of the controller realized using the fabricated ASIC and the off-chip ADCs

The above experiment was to test the duty-ratio corrector alone. However, a digital controller was also integrated on the same chip which is used to generate the gate pulses for a DC/DC converter. Fig. 4.9 shows the controller prototype realized using the fabricated ASIC. Two off-chip 8-bit ADCs with a dynamic range of 3.3V were used to sample the output voltage and the inductor current. The proportional and integral gains of the digital controllers were set using external switches. To emulate the VID code, the 7-bit reference V_{ref} is set from outside and the functionality of the chip was tested on a buck converter with the following specifications: $V_{in} = 5V$, $L = 1.2\mu H$, $C_o = 1000\mu F$, $f_s = 1MHz$ and $f_{CLK} = 50MHz$. The conventional scheme is realized by directly using the output from digital core. For realizing the proposed scheme, the DPWM output is connected to the duty-ratio correction block and the output of correction block is used as gate pulses. The VID is varied and the output voltage regulation is observed in these two cases. Fig. 4.10 shows the output voltage obtained in the two cases. As seen from the figure, the proposed scheme reduces the voltage regulation error resulting due to the finite time-resolution of DPWM.

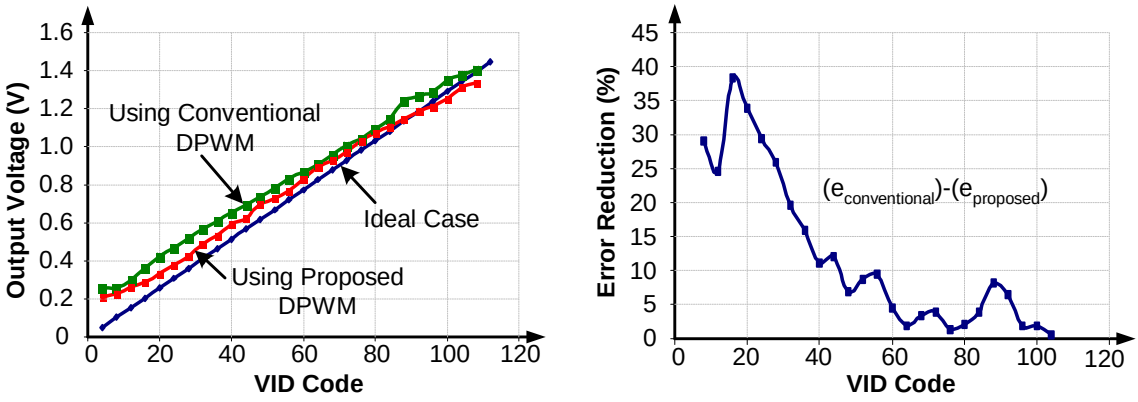

Figure 4.10: Experimental results the output voltage regulation for proposed case and conventional case.

4.5 Summary

This chapter has identified the challenges in achieving fine resolution of duty ratio when high switching frequency is required. Thus, it was proposed to improve the time resolution of the PWM pulses by updating their turn-off instances. Using such a scheme, the time resolution of analog domain and processing powers of digital implementation can be combined. From the experimental and simulation results, it is concluded that the proposed scheme is effective in improving the time resolution of the DPWM output without having to increase the clock frequency.

The scheme was tested on a single phase buck converter with a current mode control. A current controller requires the inductor current to be sensed. The next chapter discusses the available current sensing methods and brings about the advantages and disadvantages of various methods. It also proposes a new current sensing method, which is suitable for VRM type applications.

Chapter 5

Giant Magneto Resistive (GMR) effect based Current Sensing Technique

5.1 Introduction

Almost all DC-DC converters sense the inductor current for various purposes. Current sensing may be used for providing over-current protection. It may be used in current-mode control of DC-DC converters for improving the transient response of the closed loop system. Such current mode control may be based on average current or peak current control. Current sensing may also be used for load sharing among paralleled converters.

Numerous methods have been proposed and implemented for sensing the current. All these current sensing techniques can be broadly classified as non-isolated [34]-[37] and isolated sensing techniques [38]-[39]. The non-isolated methods mentioned above are either lossy or they rely on the component value. Methods based

on SenseFET require special MOSFETs to be designed and they need to be properly matched. The isolated methods are bulky and have poor temperature characteristics. These methods are certainly not useful for high performance VRM type applications where output currents are high and it is desired to maintain good current sharing despite tolerances in component values. Thus, a current sensing mechanism is required, which is independent of the value of external components, provides temperature independent sensing accuracy and is practically lossless.

5.2 Proposed Method

5.2.1 Description

In this chapter, a new scheme for sensing and controlling the inductor current is used. It is based on Giant Magneto Resistive (GMR) effect. GMR effect has been used extensively in the read heads in modern hard disk drives. Another application of the GMR effect is in non-volatile, magnetic random access memory (MRAM). In this work, this method is used for sensing the inductor current in low voltage/high current power supplies.

In GMR effect, a large change in electrical resistance occurs when thin, stacked layers of ferromagnetic and non-magnetic materials are exposed to a magnetic field [74]. Fig. 5.1 shows the working principle of GMR effect using stacked layers. Layer A which is a conductive, non-magnetic interlayer which is sandwiched between two ferromagnetic layers B. Among various combination of materials used

for forming these layers: Co, Fe, NiFe, CoFe and other alloys are used as ferromagnetic layers while Cr, Cu, Ag, etc are commonly used for the interlayer. The magnetic dipole moments in adjacent ferromagnetic layers (B) are antiparallel due to weak anti-ferromagnetic coupling between the layers. Thus the resistance offered by the BAB stack to the current flowing through the stacked layers (I_{GMR}) is high. Applying an external magnetic field helps in over coming the anti-ferromagnetic coupling, thus aligning the magnetic dipole moments in the alloy layer B along the direction of magnetic field. This results in reduction of electrical resistance of the BAB stack by 10% to 15%.

Fig. 5.1 shows the GMR effect when the current flow (I_{GMR}) is perpendicular to the plane of the layers. GMR effect is also observed when the current is in the plane of the layers. The former is called current-perpendicular-to-plane, or CPP sensor and the latter is called current-in-plane, or CIP sensor [75]. Usually the GMR effect in CPP is higher than in CIP. In both the cases, the resistance offered to the current flow can be reduced by applying external magnetic field. The magnetic field can be applied by using the current to be measured ($I_{measure}$). Change in current will change the magnetic field associated with the flow of current, thus causing the resistance to change. This change can be obtained by sensing the voltage across the Wheatstone bridge, as shown in the Fig. 5.2. The Wheatstone bridge in commercially available GMR sensors comprises of four identical multilayered GMR resistors [76]. Two of the resistors (R_g) are surrounded by flux concentrators, while the other two resistors are magnetically shielded, which allows them to act as base

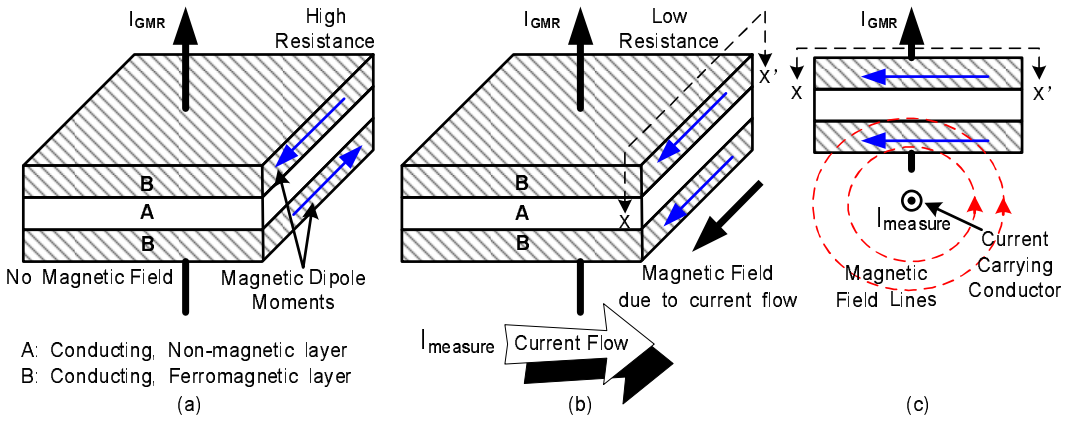

Figure 5.1: Working principle of Giant Magneto Resistive Effect. (a) Higher resistance due to anti-parallel magnetic moments, (b) Paralleled magnetic moments reduces the electrical resistance and (c) Cross section along XX' plane showing alignment of magnetic moments due to magnetic field.

resistance (R_b). The output voltage from such an arrangement can be obtained as

$$V_{sense} = \frac{R_b - R_g}{R_b + R_g} \cdot V_{cc} \tag{5.1}$$

The base resistance (R_b) is fixed and it does not change with change in magnetic field. However, the resistance R_g changes with magnetic field. The sensitivity of sensed output to the change in resistance R_g can be obtained as

$$\frac{\partial V_{sense}}{\partial R_g} = -\frac{2 \cdot R_b}{(R_b + R_g)^2} \cdot V_{cc} \tag{5.2}$$

Thus the Wheatstone bridge configuration can amplify the small change in resistance (R_g). The typical resistance offered by GMR is around $5\,k\Omega$. The fixed resistance is also designed to be the same. Thus when operating at 12 V power supply, it will result in a power consumption of $28.8\,mW$. This power consumed is practically independent of the current to be measured.

The Wheatstone bridge configuration in the commercially available GMR sensors [76] also help in providing temperature compensation. The bridge uses

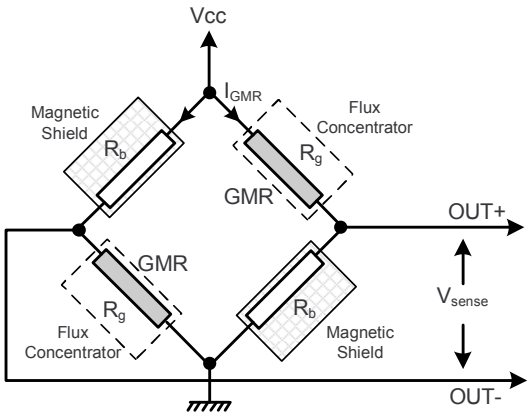

Figure 5.2: Wheatstone Bridge configuration available for sensing application.

four identical GMR resistors and all the resistors experience the same change in resistance due to temperature change. This cancels out the inherent temperature dependence [77]. Also, these ICs are sensitive in one direction in the plane of the IC, with a cosine scaled fall-off in sensitivity as the sensor is rotated away from the sensitive direction. These GMR sensors provide the same output for magnetic fields in the positive or negative direction along the axis of sensitivity. These sensors are characteriszed by high sensitivity to applied magnetic fields, excellent temperature stability, practically low power consumption and small size. Thus they can be suitable candidate for high current applications where resistive method can not be used due to the associated power losses and other methods cannot be used due to their complexity or the variations in the component values.

5.2.2 Work on Magnetoresistive effect

Anisotropic Magnetoresistance (AMR) property demonstrates the dependence of electrical resistance on the angle between the direction of current flow and the

orientation of magnetic field [78]. AMR effect has been used for current sensing in [79]. However, with the advent of GMR technology, the AMR technology has been surpassed. While the resistance change in AMR effect is approximately $2-4\%$, the GMR offers change in resistance upto $10-15\%$. Magneto-Impedance (MI) effect has also been explored which refers to the large variation of the impedance of a magnetic material carrying an AC current when subjected to an external field [38], [80], [81]. However due to its extremely high sensitivity, even small external magnetic fields can induce a significant error. Thus, the accuracy of MI sensor is highly susceptible to noise.

The GMR effect provides higher sensitivity than the AMR effect and is a better candidate for sensing large range of currents. Unlike MI sensors, its does not get significantly affected by small external fields. Thus due to their low cost, small size and minimum temperature dependence, the GMR sensors can be an alternative to the existing current sensors.

Although, the GMR sensors provide temperature compensation by using wheatstone bridge configuration, a GMR based temperature sensing method has been introduced in [77]. It decouples the temperature signal from the field measurement by using one half of the wheatstone bridge. It relies on a constant current supply as the bridge excitation. If a constant current source is applied, the voltage across the GMR elements will increase as the temperature increases. Such a method is proposed for motor drive modules, with main focus on combining a thermal sensor with the current sensor.

The GMR sensor is based on the magnetic field generated by the current flow. But the current density in a conductor depends upon its location in the cross-section of the conductor and the frequency spectrum of the current. A study on influence of eddy currents on magnetic field distribution due to closely lying conductors is presented in [82]. It establishes an optimum location for accurately capturing the entire spectrum of the current in motor drive applications. This is useful for point field-based current sensing using an integrated GMR sensor, which does not have a flux concentrator. However, in commercially available GMR sensors, the presence of on-chip flux concentrators increases the field at the sensor elements. Moreover, in switched mode power supply the AC component in the inductor current is designed to be much smaller than the DC component. Thus it is important to note the DC magnetic field distribution. In this paper, the optimum location for the magnetic field detector is established for average current sensing based on DC magnetic field distribution.

5.2.3 Magnetic Field distribution due to current carrying track

The work on GMR sensor is based around the commercially available GMR sensors [76]. The technical information provided by the manufacturer assumes the width of the current carrying track to be smaller than the IC width. However, for high current applications, the track widths are designed to be wider than the IC width. Thus, it is important to assess the performance of the sensor in these cases for high current applications. To this end, a mathematical framework was devel-

oped for correct positioning of the field sensor and to obtain its optimal response.

As mentioned earlier, the GMR sensor is based on magnetic field associated with the flow of current. The magnetic strength will depend upon the distance from the current carrying conductor. For example, the magnetic field density at a distance r due to current carrying wire is given as

$$B = \frac{\mu_o i}{2\pi r} \tag{5.3}$$

where i is the current (in amperes) flowing though the wire and μ_o is the permeability constant of free space ($\mu_o = 4\pi 10^{-7}\, Tm/A$). The farther the conductor, the weaker is the magnetic field. Thus the placement of the sensor with respect to the current carrying conductor becomes very critical. The magnetic field density can be studied to obtain the variations in the sensed output with change in position of the sensor.

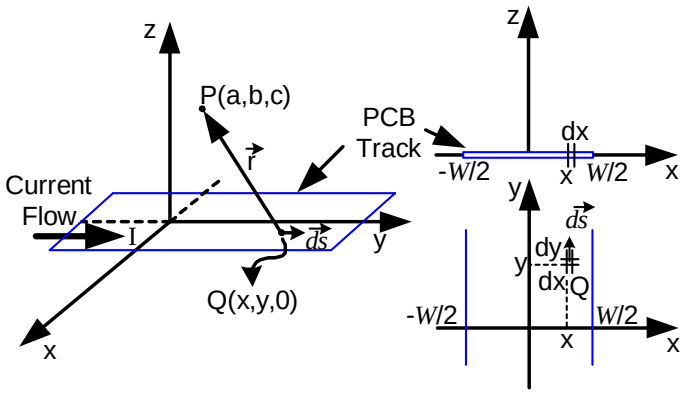

Figure 5.3: Magnetic field at point P due to a long current carrying PCB track.

The magnetic field density due to current carrying track can be obtained with the help of following analysis. Consider a long current carrying track in x-y plane, with its current flowing in y-direction as shown in Fig. 5.3. The track thickness is

assumed to be negligible as compared to other dimensions and is neglected. The magnetic field due to this current carrying track can be obtained at any arbitrary point having coordinates P(a,b,c). The magnetic field density due to an infinitesimal current carrying element ($\vec{ds}$) carrying a current di located at Q(x,y,0) is given as

$$d\vec{B} = \frac{\mu_o}{4\pi}\frac{di\vec{ds} \times \vec{r}}{r^3} \tag{5.4}$$

where $\vec{r}$ is the vector pointing from the current element at (Q) to the observation point (P).

Since the track is long enough, the point P is assumed to be in x-z plane. Thus, the coordinates of point P can be simplified as P(a,0,c). Current flowing in element at Q is $di = \frac{I}{W}dx$, where W is the width of the track. The current element orientation is $\vec{ds} = dy\hat{j}$ and the distance of current carrying element from the point under observation (P) is given as

$$\vec{r} = \vec{QP} = (a-x)\hat{i} - y\hat{j} + c\hat{k} \tag{5.5}$$

where $\hat{i}$, $\hat{j}$ and $\hat{k}$ are unit vectors along x, y and z-directions respectively.

This gives us the magnetic field density at P due to current carrying element Q as

$$d\vec{B} = \frac{\mu_o}{4\pi} \cdot \frac{Idx}{W}\frac{c\hat{i} + (x-a)\hat{k}}{(c^2 + (x-a)^2 + y^2)^{3/2}}dy \tag{5.6}$$

The magnitude of this magnetic field density at P is obtained as

$$|dB| = \frac{\mu_o}{4\pi} \cdot \frac{Idx}{W}\frac{(c^2 + (x-a)^2)^{1/2}}{(c^2 + (x-a)^2 + y^2)^{3/2}}dy \tag{5.7}$$

The GMR sensor has its axis of sensitivity along the x-y plane, while it is insensitive to z-component of magnetic field. As obtained in (5.6), there is no y-component of the field. Thus the total field in x-direction can evaluated by integrating (5.6) over the track area.

$$B_x = \int_{x=-W/2}^{x=W/2} \int_{y=-\infty}^{y=\infty} \frac{\mu_o}{4\pi} \cdot \frac{I \cdot dx}{W} \frac{c}{(c^2 + (x-a)^2 + y^2)^{3/2}} dy \tag{5.8}$$

Rearranging the terms we get

$$B_x = \frac{\mu_o}{4\pi} \frac{I}{W} \int_{-W/2}^{W/2} \int_{-\infty}^{\infty} \frac{c \cdot dy}{(c^2 + (x-a)^2 + y^2)^{3/2}} \cdot dx \tag{5.9}$$

$$B_x = \frac{\mu_o}{2\pi} \frac{Ic}{W} \int_{-W/2}^{W/2} \frac{dx}{((a-x)^2 + c^2)^{1/2}} \tag{5.10}$$

$$B_x = \frac{\mu_o}{2\pi} \frac{I}{W} [tan^{-1}(\frac{a + \frac{W}{2}}{c}) - tan^{-1}(\frac{a - \frac{W}{2}}{c})] \tag{5.11}$$

Using (5.11), the general expression of the magnetic field at any arbitrary point P(x,0,z) can be obtained by substituting a=x and c=z.

$$B_x = \frac{\mu_o}{2\pi} \frac{I}{W} [tan^{-1}(\frac{x + \frac{W}{2}}{z}) - tan^{-1}(\frac{x - \frac{W}{2}}{z})] \tag{5.12}$$

The magnitude decreases as one moves away from the current carrying track in the vertical direction. For a fixed height above the current carrying track, B_x will be maximum when $\frac{dB_x}{dx} = 0$. Clearly, the magnitude of the magnetic field density will be maximum at $x = 0$. The field decreases as one moves away from the center of the current carrying track and it attains the minimum as $x \to \pm\infty$.

The field distribution obtained using above analysis was plotted using MATLAB [83]. The results were verified using a 2-D finite element based field simulator

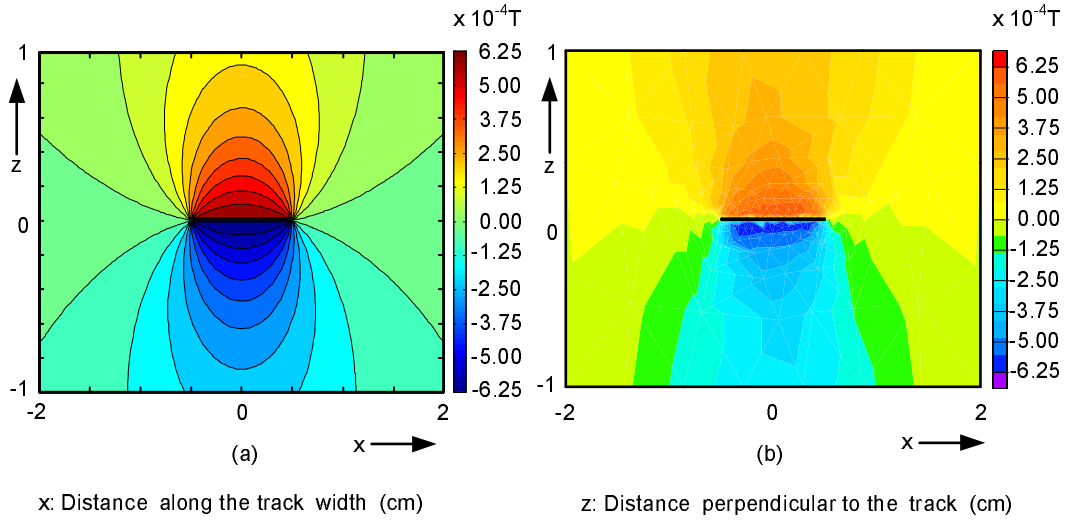

Figure 5.4: (a) Magnetic Field Distribution as obtained from MATLAB (b) Magnetic Field Distribution as obtained from QuickField.

QuickField [84]. Fig. 5.4 shows the field distribution using two methods. The current flow in both cases is set as 10 A and the track width is 1 cm. Notice a good agreement between the field patterns obtained by these two methods. The accuracy of the field distribution obtained in simulation depends upon the grid size. The coarse grid size in QuickField (student version) resulted in small mismatch in the two field patterns. This field pattern can be used to optimally place the sensor for desired accuracy in field sensing. To this end, various sensor placement configurations were studied and results are presented here.

5.2.4 Performance Evaluation

Fig. 5.5(a) shows an GMR magnetic field sensor (AA003-02 [76]) with its axis of sensitivity along the horizontal direction. In order to study the performance, the sensor was placed on the top of the PCB board and current was varied through

the track made on the bottom layer of PCB. The track width was $W = 5.5\,mm$ and the supply voltage (V_{cc}) was kept at 20 V. Fig. 5.5(b) shows the input-output characteristics of such a sensor. Fig. 5.5(c) shows the linearity of output voltage when the supply voltage was varied, while the current to be measured ($I_{measure}$) was kept constant. It shows the sensing gain varies linearly with the supply voltage. The supply voltages of 15 V$\sim$20 V are common in gate drivers and can also be used to power these sensors.

The sensor was also studied to verify the temperature independence. ETAC's HISPEC high temperature chamber was used to control the temperature. The PCB board having the GMR sensor was placed in the temperature chamber and current was forced through the PCB track. The sensor output was noted for various currents at various temperatures. Fig. 5.6 shows the input-output characteristics at two different temperatures, $T = 30^oC$ and $T = 70^oC$. It shows the sensing accuracy in these sensors is temperature independent.

As established earlier, the farther the conductor is, the weaker is the magnetic field. To study this effect, the current was made to flow through the bottom layer, while the sensor was placed on the top layer (Fig. 5.7(a)). In another set, the current was made to flow through a conductor lying on the sensor (Fig. 5.7(b)). In both these cases, the track or conductor width was same as the sensor width. Fig. 5.7(c) shows the output voltage obtained by these two configurations. It can be seen that configuration B records a steeper input output characteristics. In another study, a wider track was used and two sensors were placed, one in the

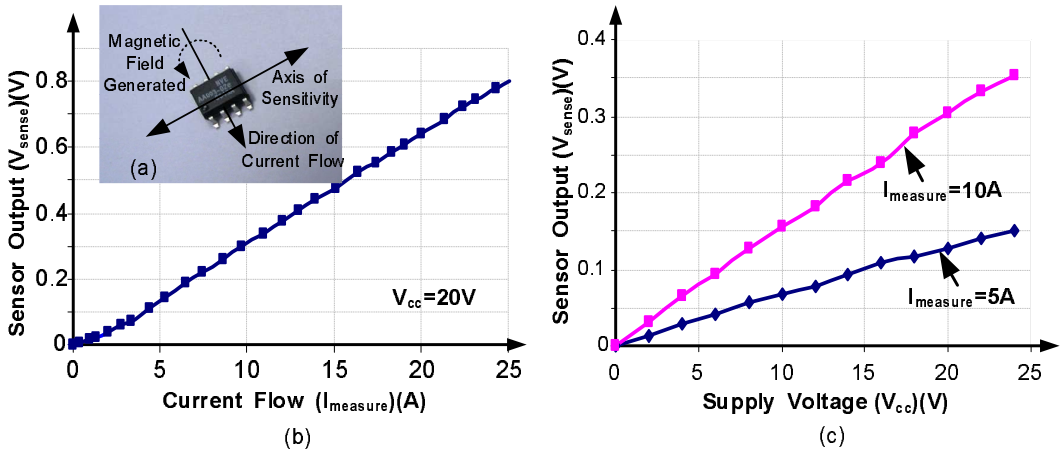

Figure 5.5: (a) Current detection using GMR magnetic field sensor whose axis of sensitivity is in the horizontal direction; (b) Input Output Characteristics of sensor at a supply voltage of 20 V and (c) Linearity of output voltage with varying supply voltage.

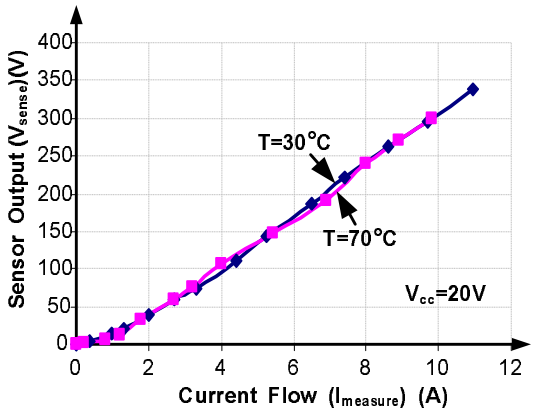

Figure 5.6: Input-Output characteristics at two different temperatures ($T = 30^oC$ and $T = 70^oC$)

center of the track and second at a distance of 1/4th of the track width as shown in Fig. 5.7(d). Fig. 5.7(e) shows the input output characteristics as obtained from these two sensors. Supply voltage (V_{cc}) in all these cases was kept at 20 V. This shows the sensing gain can be increased by placing the sensor close to center of the conductor. However, mismatch in the placement of sensor on a wider track does not have a significant change in the sensing gain.

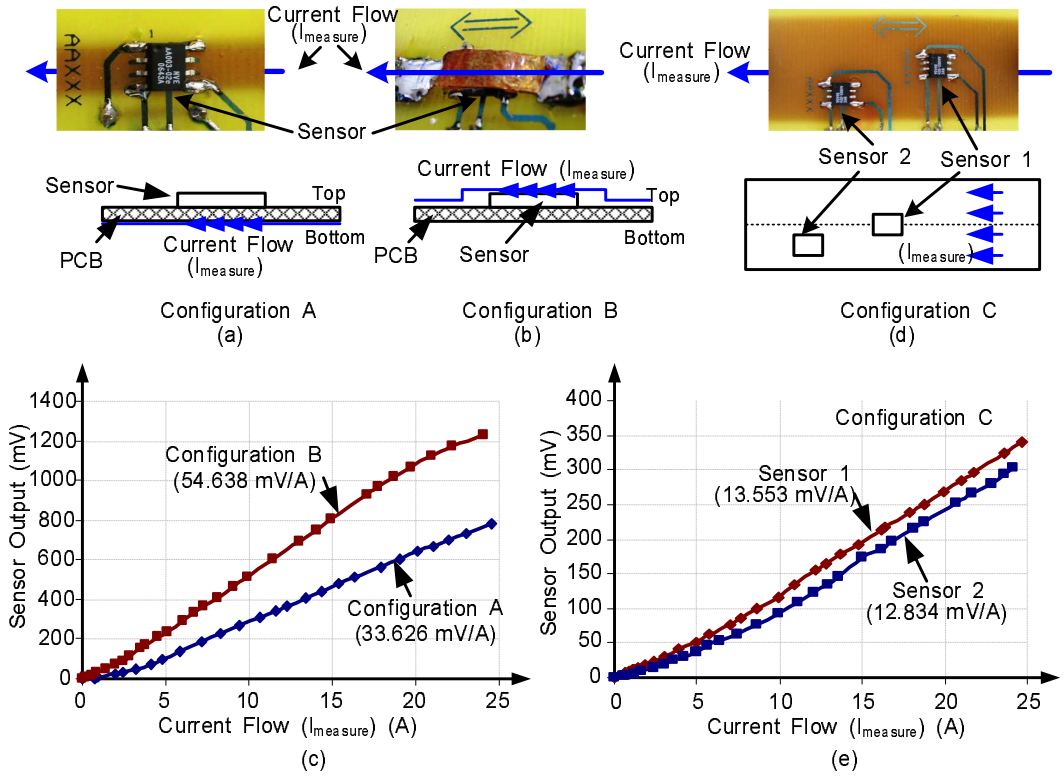

Figure 5.7: (a) Current flow through the bottom layer; (b) Current flow through a conductor placed on top on sensor; (c) Output voltage as obtained from configurations A and B; (d) Placement of sensors on a wider track; and (e) Input Output characteristics as obtained from configuration C.

This phenomenon can be explained with the help of the magnetic field density obtained in (5.12). The sensing ratio in configuration A (Fig. 5.7) is $33.626\,mV/A$, while for configuration B it was observed as $54.638\,mV/A$. This shows the sensor records a higher magnetic field in configuration B. Based on this, the location of sensor in the IC can be obtained. Lets say it is located at a distance of z_B from the top surface in configuration B and it is at a distance of z_A from the bottom surface, as shown in Fig. 5.8. $z_A + z_B$ includes the PCB thickness (1.6 mm) and the height of the sensor in SOIC8 package (1.55 mm). Thus,

$$z_A + z_B = 3.15\,mm \tag{5.13}$$

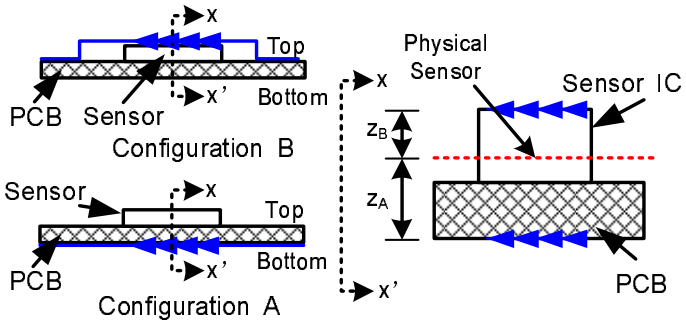

Figure 5.8: Determining the location of physical sensor in the Sensor chip.

Since the sensors are placed at the center of the track, x can be set as $x = 0$. Using the ratio of these sensing gains, we have,

$$(\frac{W_A}{W_B})[\frac{tan^{-1}(\frac{W_B}{2z_B}) + tan^{-1}(\frac{W_B}{2z_B})}{tan^{-1}(\frac{W_A}{2z_A}) + tan^{-1}(\frac{W_A}{2z_A})}] = \frac{54.638}{33.626} \tag{5.14}$$

where W_A and W_B are the track widths for configuration A and B respectively.

The width of tracks used in configuration A and B is $W_A = W_B = 5.5\,mm$. Solving (5.14) results in $z_A = 2.522\,mm$ and $z_B = 0.628\,mm$. This allows us to set $z = 2.522\,mm$ in (5.12) for further analysis, when the current is flowing through the layer lying under the PCB board having a thickness of 1.6 mm and the sensor is in SOIC8 package. Substituting $z = 2.522\,mm$ in (5.12), we get

$$B_x = \frac{\mu_o}{2\pi}\frac{I}{W}[tan^{-1}(\frac{x + \frac{W}{2}}{2.522 \times 10^{-3}}) - tan^{-1}(\frac{x - \frac{W}{2}}{2.522 \times 10^{-3}})] \tag{5.15}$$

Clearly the field is maximum in the plane lying along the center of the track ($x = 0$). The maximum field is obtained as

$$B_{max} = \frac{\mu_o}{\pi}\frac{I}{W}[tan^{-1}(\frac{\frac{W}{2}}{2.522 \times 10^{-3}})] \tag{5.16}$$

Since the sensor output voltage is proportional to the magnetic field, we have

$$v_{sense} = \alpha_v \cdot B_x =$$
$$\alpha_v \cdot \frac{\mu_o}{2\pi}\frac{I}{W}[tan^{-1}(\frac{x+\frac{W}{2}}{2.522\times10^{-3}}) - tan^{-1}(\frac{x-\frac{W}{2}}{2.522\times10^{-3}})] \quad (5.17)$$

where α_v is the proportionality constant. Simplifying (5.17), we get

$$\alpha_v = \frac{v_{sense}}{I}\frac{2\pi W}{\mu_o[tan^{-1}(\frac{x+\frac{W}{2}}{2.522\times10^{-3}}) - tan^{-1}(\frac{x-\frac{W}{2}}{2.522\times10^{-3}})]} \quad (5.18)$$

Using the data from configuration A (W=5.5 mm, sensing ratio=33.626 mV/A), the proportionality constant is obtained as $\alpha_v = 557.9859\, V/Tesla$. Using this, the sensing ratio is calculated as

$$K = \frac{v_{sense}}{I} = 557.9859 \cdot \frac{\mu_o}{2\pi W}[tan^{-1}(\frac{x+\frac{W}{2}}{2.522\times10^{-3}}) - tan^{-1}(\frac{x-\frac{W}{2}}{2.522\times10^{-3}})] \quad (5.19)$$

where W is the width of the track and x is the distance of the sensor from the center of the track.

For configuration C, the track width was $W_C = 23.0\, mm$. While sensor 1 was placed along the center of the track and the sensor 2 was placed at a distance of 1/4th of the track width. Using (5.19), the sensing ratios for these two cases can be obtained. The sensing ratio for sensor 1 can be obtained as 13.148 mV/A and for sensor 2 it is obtained as 12.533 mV/A. The predicted values using the above analysis match with the experimental values of 13.533 mV/A and 12.834 mV/A respectively, as obtained from input-output characteristics in Fig. 5.7.

Although configuration B gives higher sensing ratio, it would require routing the current over the sensor IC. Thus configuration A was chosen for further analysis,

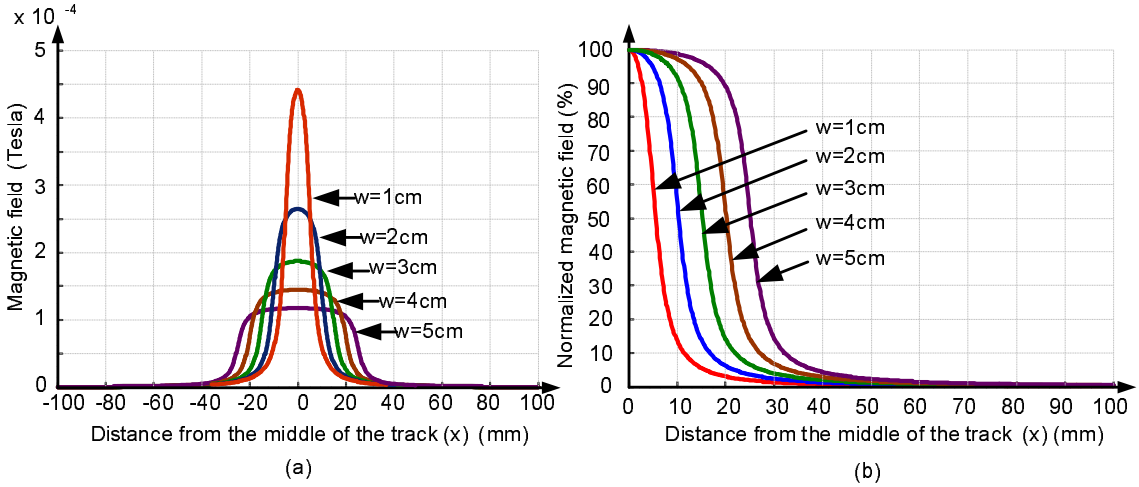

Figure 5.9: Curves showing magnetic field distribution for varying track widths carrying a current of 10 A.

as it can be realized using conventional PCB design. Based on the magnetic field distribution for configuration A, the magnetic field can be obtained as the point of observation moves away from the track. Thus, x is varied in (5.15) for different values of track widths. The current flowing through the track is 10 A in each case. Fig. 5.9(a) shows the magnetic field as a function of distance from the center of the current carrying track. As expected, the peak magnetic field occurs at the point lying above the center of the track. Using (5.15) and (5.16), the normalized magnetic field is obtained as the ratio of magnetic field at a distance x from the center of the track (B_x) to the maximum field for the given track width (B_{max}). Fig. 5.9(b) shows the normalized magnetic field as one moves away from the current carrying conductor.

Since the sensor is based on the magnetic field generated from the current carrying conductor, the sensed output depends upon the location of the sensor. For a reasonable accuracy of 90% or above, it would be interesting to note the range of

location which can give the desired accuracy. Using the normalized magnetic field, one can obtain the distance from the conductor for the desired accuracy. Fig. 5.10 shows the location of points from the center of the track where the magnetic field reduces to 90% of its peak value, B_{max}. This is marked by region ① in Fig. 5.10. Similarly, the field strength reduces to less than 10% in region ②. This shows if a second sensor is placed in region ② for sensing the current in another conductor, it will get influenced by the field due to first conductor. This gives us the distance (x) where the sensor should be placed with respect to the track to achieve the desired accuracy. For 90% or more accuracy it should be placed in region ①, such that $0 \leq x \leq x_1$. In order to reduce the interference to less than 10% among closely lying sensors, they should be separated by a distance such that $x \geq x_2$. For example, the track thickness of 20 mm provides $x_1 = 6.4\,mm$ and $x_2 = 16.8\,mm$. Thus for an accuracy of 90%, the sensor should not be farther than 6.4 mm from the center of the track.

5.3 Experimental Results

The performance of the proposed method for current sensing was tested on a buck converter prototype with the following parameters: $V_{in} = 5\,V$, $V_{ref} = 1.25\,V$, $L = 1.2\mu H$, $C_o = 1000\mu F$, $f_s = 1\,MHz$. Fig. 5.11 shows the photograph of the prototype of a buck converter which uses a GMR sensor. A wire loop is used to probe the inductor current. AA003-02 was used for current sensing with its supply voltage (V_{cc}) at 20 V. The GMR sensor was placed on the top of the PCB board

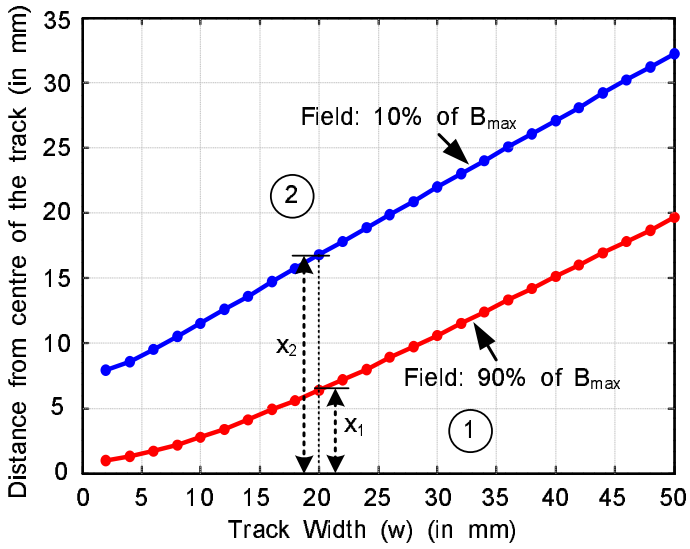

Figure 5.10: Curves showing the location of points where magnetic field reduces to 90% in configuration A. Region ① has magnetic field $>$ 90% of B_{max} and region ② has magnetic field $<$ 10% of B_{max}.

and current was made to flow through the bottom layer as in configuration A. The output of the sensor was amplified before sampling it for control purpose. The current sensing ratio used is 55mV/A. Since average current control is desired, the average value of the inductor current can be obtained by sensing the current in the middle of the switch-on and switch-off intervals. A digital controller was used to obtain the desired performance of the system. The inductor current and the output voltage was sampled using an ADC. The ADC had 8-bit resolution ($N_{ADC} = 8$) and DPWM had 6-bit of hardware resolution. Thus, 3-bit digital dither was introduced to increase the effective resolution of DPWM module to 6+3=9 bits ($N_{DPWM} = 9$). The controller was implemented on a Spartan-3 Field Programmable Gate Array (FPGA) by Xilinx operating at a clock frequency of 50 Mhz.

The dynamic response of inner current loop was studied to see the effect of step change in the reference current. Fig. 5.12(a) shows the response of the system

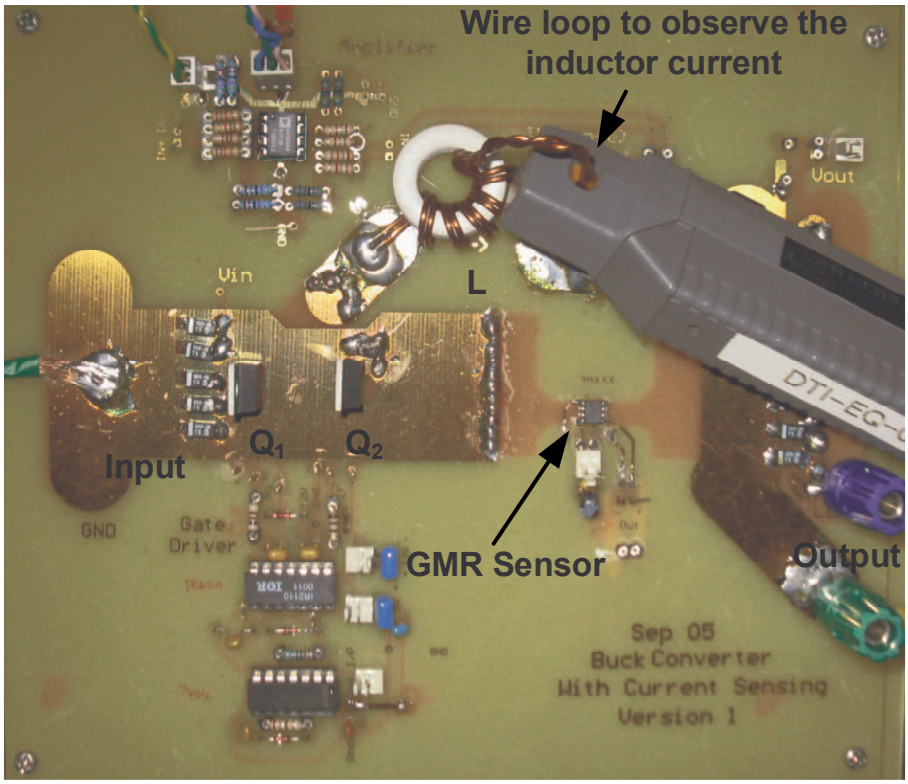

Figure 5.11: Experimental prototype of a buck converter which uses a GMR sensor for current sensing. A current probe is also used to observe the inductor current.

when the converter was subjected to step change in the reference current from 5 A to 15 A. The system was also tested for load transients with a step-up change from 3 A-12.5 A and vice versa. Fig. 5.12(b) shows the dynamic response of the average current mode controller, when reference voltage is set as 1.25 V. The load transients were generated by switching the load resistance.

The results shown above were to test the performance of the current sensor under load dynamics. In practice the VRM output requires adaptive voltage positioning (AVP). In adaptive voltage positioning, the output voltage of the VRM is adapted to changes in the load. This causes the output voltage to droop with the load. Adaptive voltage positioning was implemented by changing the refer-

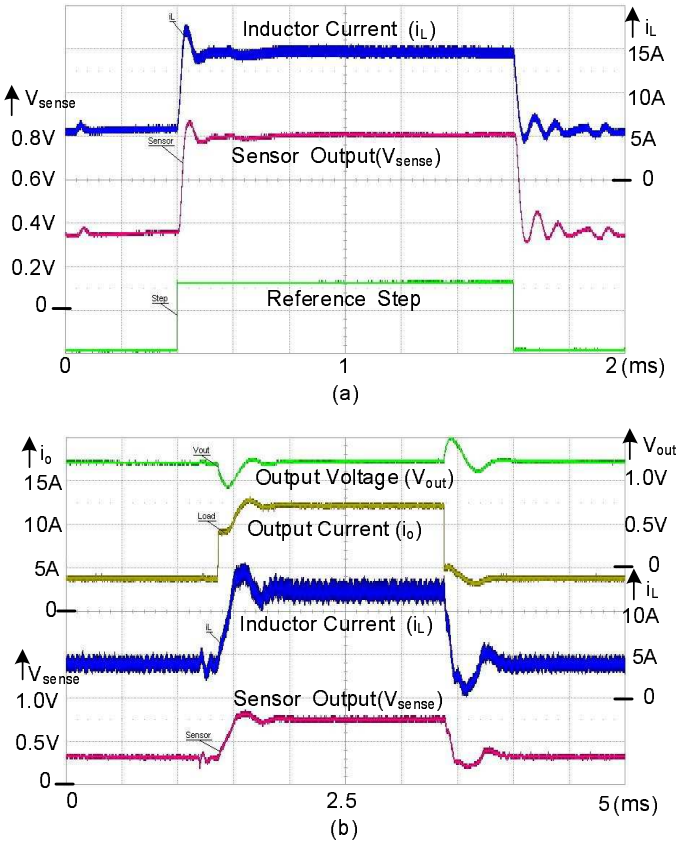

Figure 5.12: (a) Result showing the dynamic response of digitally controlled buck converter for a step change in current reference; (b) Output voltage with a step change in load current from 3A to 12A.

ence voltage in accordance with the load current. Reference voltage is defined as $v_{ref} = V_{ref} - i_o \cdot R_{droop}$, where V_{ref} is the nominal reference voltage at no load conditions, i_o is the load current and R_{droop} is the droop resistance obtained from the load line. Fig. 5.13 shows the dynamic response of the controller with adaptive voltage positioning with a droop resistance of $R_{droop} = 12m\Omega$. It shows a droop of around 130mV for a step change in load current from 3A to 13.5A.

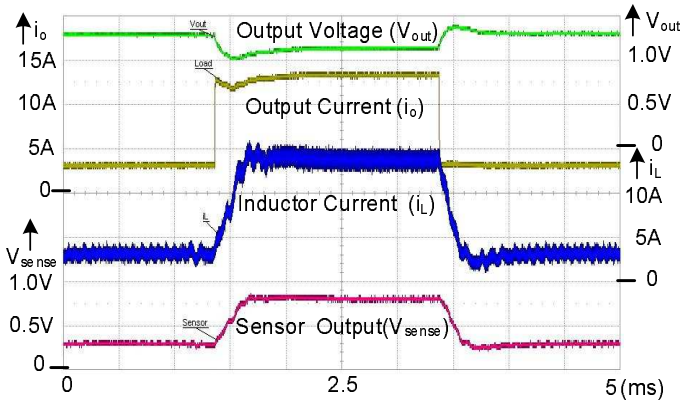

Figure 5.13: Result showing the dynamic performance of the controller with adaptive voltage positioning for a step load change.

5.4 Summary

In this chapter, a Giant Magneto Resistive (GMR) effect based current sensor is presented that can be used for low voltage high current VRMs. The method does not rely on the knowledge of component value, provides high sensitivity and results in negligible power loss. The sensor is based on magnetic field generated from the current carrying conductor. Thus the sensed output depends upon the location of the sensor. Various sensor placement configurations were analyzed and based on the theoretical framework, optimum location is derived for achieving the desired accuracy in current sensing. However, due to high currents in VRMs, an interleaved converter topology is preferred. Such a topology will require individual inductor currents to be sensed. In an N-phase converter, N current sensors are required. To this end, the next chapter explores the idea of reducing the current sensors in such a converter.

Chapter 6

Current Sharing in Multiphase Converters

6.1 Introduction

An interleaved multiphase converter topology is widely used for VRM applications. It provides paralleled paths for the output current, as a result a particular phase carries only a fraction of the total current. In such a topology, it is important to share the currents equally among various phases. However, due to variation in the inductor values, differences of components, connections and layout results in unequal current distribution among phases. This causes uneven distribution of losses and reduces the overall efficiency. Thus appropriate current sharing mechanism is required to distribute the current evenly among the phases.

A number of current sharing approaches have been presented in literature. These current sharing approaches can be broadly classified as - passive sharing methods [41] and active sharing methods [42] - [51]. Passive current sharing involves

putting droop resistance in series with the outputs. This droop resistance will create enough voltage drop under load to cause the converters to share the load current. On the other hand, in active current sharing method, an additional active circuit is employed to force the individual phase currents to match the reference phase current. In these schemes, the information about individual currents are required. For a N-paralleled converters, it requires N current sensors. The scheme proposed in [52] obtains the current unbalance by using the ESR of the input capacitor. However, such a method will be computationally intensive and is not suitable for low cost digital implementations.

The current mode schemes mentioned above require N-current sensors for achieving current sharing among N-paralleled converters. However, it is always desired to have a single sensor for N-phases. A scheme based on single current sensor has been proposed in [52]. It proposes to use the voltage drop across the effective series resistance (ESR) of the input capacitor to estimate the phase current unbalance in N-paralleled converters. The voltage drop due to ESR is proportional to the inductor current of a particular phase during the turn-ON duration of its high-side switch. However, there may be instances when the conduction times of two or more phases overlap, leading to inaccuracy in estimation. In order to overcome this error, computationally intensive harmonic analysis of the input capacitor voltage is proposed.

The active current sharing schemes require N-current sensors and the schemes based on single sensor are computationally intensive. Thus, a current sensing

scheme is proposed which is based on single sensor and has the following features:

1. It can sense the individual currents with a single sensor irrespective of the number of phases.
2. The loss in current sensor remains constant for any number of parallel phases and load current.
3. It is easier to implement and provides the various functionalities of a voltage regulating module.
4. It can be applied to any paralleled switching converter system.

6.2 Proposed Scheme

6.2.1 Current Sensing

Fig. 6.1(a) shows the conventional scheme which uses N-number of sensors to sense the individual input currents. Here (Q_{11}, Q_{12}) and (Q_{21}, Q_{22}) form the conventional buck converter. If a single sensor is used to sense the input current, then there may be instances when the conduction times of two or more phases overlap. This will lead to inaccuracy in current sensing. Fig. 6.1(b) shows the proposed scheme which uses single sensor. In the proposed scheme, additional switches Q_{13} and Q_{23} are added. By selectively turning on the switches Q_{13} and Q_{23}, the individual phase currents are forced to flow through the sensor. When Q_{13} is turned on instead of Q_{11}, the sensor will sense the input current of phase 1.

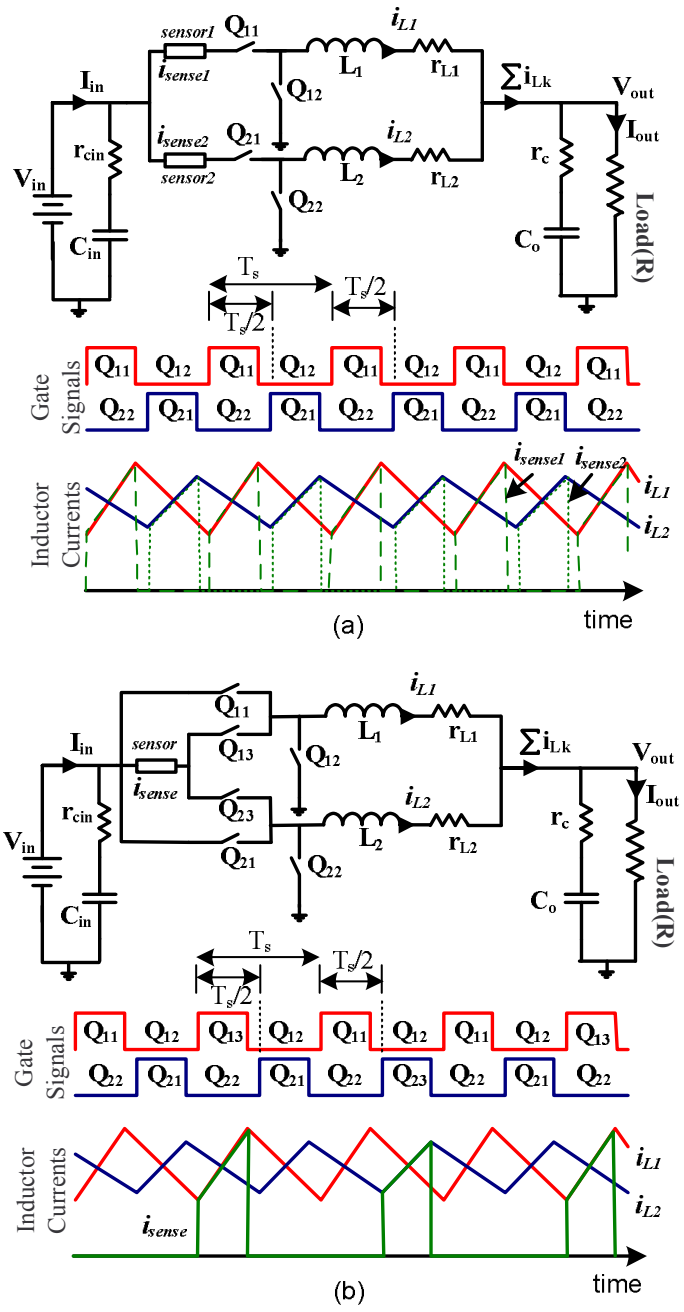

Figure 6.1: Current Sensing in a 2-phase interleaved buck converter

Similarly, by turning on Q_{23} instead of Q_{21}, input current of phase 2 (i_{L2}) can be measured.

In a multiphase system the phase currents are interleaved at $2\pi/N$ with respect to each other. In a 2-phase system, the gate pulses for phase 2 are phase

shifted by $T_s/2$ with respect to the gate pulses of phase 1, where T_s is the switching period. In order to avoid simultaneous turning on of Q_{13} and Q_{23}, an additional phase shift of $T_s/2$ is used. That is, the switching of Q_{23} is delayed by 1.5 time periods with respect to Q_{13}, as shown in Fig. 6.1(b). Thus, in a 2-phase system the switches Q_{13} and Q_{23} operate with a time period of $3T_s$, or in other words with a switching frequency of $f_s/3$, where f_s is the switching frequency of the converter. This enables the current sensing of the two inductor currents in a time-interleaved manner and avoids the simultaneous sensing of both the phases. The scheme can be used with any current sensor. For example, a GMR sensor can be used to sense the various inductor currents.

Although the proposed scheme is using higher number of switches, the increase in cost due to switches is much less than the cost of having N-such sensors. In addition, the switches can be integrated along with the control electronics resulting in a power module. On the other hand, the GMR sensor still has to be external to the ASIC.

In order to verify the functionality of the current sensing scheme, a two phase interleaved converter was tested. The converter was operated in open loop and the duty ratio of phase 1 was kept higher than that of phase 2, so as to result in different phase currents. The current through the sensor was obtained using a current probe. Fig. 6.2 shows the two inductor currents and the sensed current as obtained using a current probe. A wire loop was used to sense the current using current probe. This introduces an additional inductance while switching the

auxiliary switches. As a result the inductor current ripple in the two phases slightly varies during their turn on.

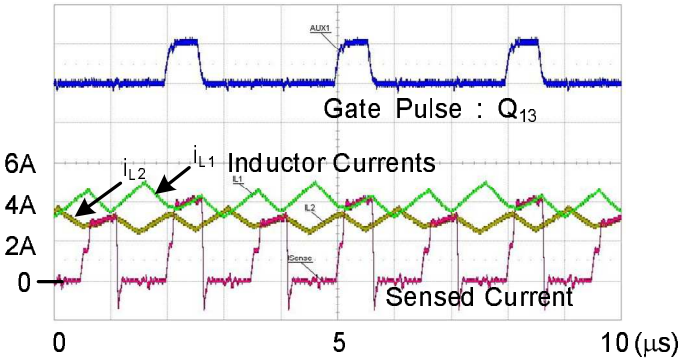

Figure 6.2: Current sensing in a 2-phase system using single sensor

The current probe used above was to verify the functionality of the sensing circuit. In actual circuit, the wire loop was removed and a Giant-Magneto Resistive (GMR) effect based current sensor was used [76], [85]. It senses the magnetic field associated with the current to be measured. The typical resistance offered by commercially available GMR is around $5\,k\Omega$. Thus when operating at 12 V power supply, it will result in a power consumption of $0.028\,W$. This power consumed is practically independent of the current to be measured.

6.2.2 Power Loss Analysis

For the circuit operation described above, (Q_{11}, Q_{12}) and (Q_{21}, Q_{22}) form the conventional buck converter. The individual currents are sensed by switching Q_{13} and Q_{23}. This allows the individual phase currents to flow through the sensor. Thus, for a given converter, either Q_{11} or Q_{13} will be switched at a time. Since Q_{11} and Q_{13} are identical and only one of them will be switched at a time, the scheme

does not result in additional losses.

6.2.3 Current Sharing

Fig. 6.3 shows the control architecture which is used for current sharing among individual phases. For simplicity only two phases are shown. As shown in the Fig. C_v is the voltage controller, G_{i1d} and G_{i2d} are the control to inductor current transfer function for phase 1 and phase 2 respectively. G_{vi} is the total inductor current to output voltage transfer function and C_{12} is the current sharing controller used for balancing the individual currents. The proposed scheme is based on difference in individual phase currents. The control strategy utilizes only voltage controller. In a multi-phase converter, each phase takes the same duty ratio which is obtained from voltage compensator. However under load dynamics, the phase having the minimum inductance may carry the entire difference of the load current. Moreover, in steady state, the phases may carry different currents due to variations among individual phases. To mitigate this, the duty ratio is compensated for each phase depending upon the current mismatch in the phase currents. This can be explained by considering the inductor current dynamics which is given by

$$i_L(k+1) = i_L(k) + (D(k).V_{in}(k) - V_{out}(k))\frac{T_s}{L} + \delta i_L \tag{6.1}$$

where $D(k)$ is the duty ratio, i_L is the average inductor current and δi_L accounts for current due to un-modelled parameters resulting from mismatches and other non-idealities. Current sharing of parallel phases is inherently guaranteed by properly compensating for δi_L for different phases. Thus the duty ratio of various phases

is compensated based on the circuit parameters. For this, only a voltage mode control loop is required which gives the desired duty ratio $D(k)$. Based on this duty ratio, the duty ratio for various phases are adjusted so as to account for unwanted disturbances.

$$d_1(k) = D(k) - \Delta d_{12}, d_2(k) = D(k) + \Delta d_{12}, ... \tag{6.2}$$

where Δd_{12} is obtained based on the circuit parameters.

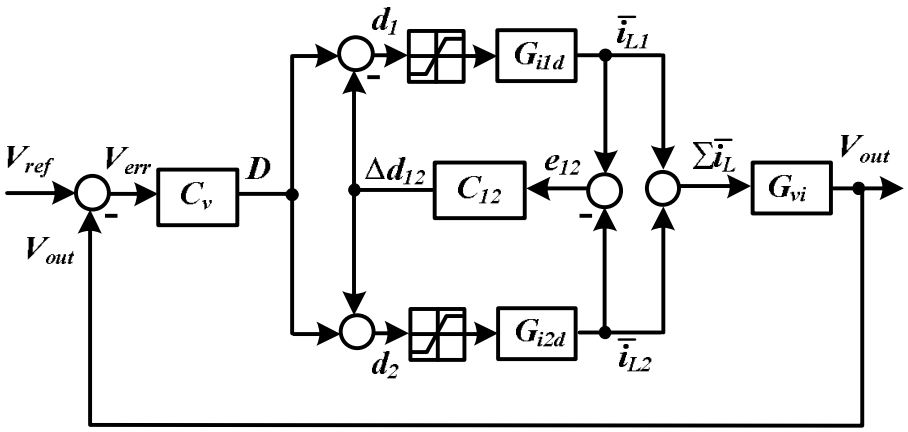

Figure 6.3: Two phase control architecture with duty ratio compensation for current sharing

Since the current sharing is based on difference in the individual average phase currents, the current sharing does not get affected by the bandwidth of the outer voltage loop.

In the scheme shown in Fig. 6.3, Δd_{12} is computed based on the mismatch in the average inductor currents $\overline{e}_{12} = \overline{i}_{L1} - \overline{i}_{L2}$. An increase (or decrease) in duty ratio command of a phase results in increase (or decrease) in the phase current.

Thus, the duty ratios are compensated as,

$$d_1(k) = D(k) - C_{12}.\overline{e}_{12} \tag{6.3}$$

$$d_2(k) = D(k) + C_{12}.\overline{e}_{12} \tag{6.4}$$

where C_{12} is the current sharing (CS) controller.

For implementing this scheme, the difference in the individual currents is used. The individual currents are sampled and stored according to the sensing scheme described above. The duty ratios of individual phases are then updated based on the current mismatch among the phases.

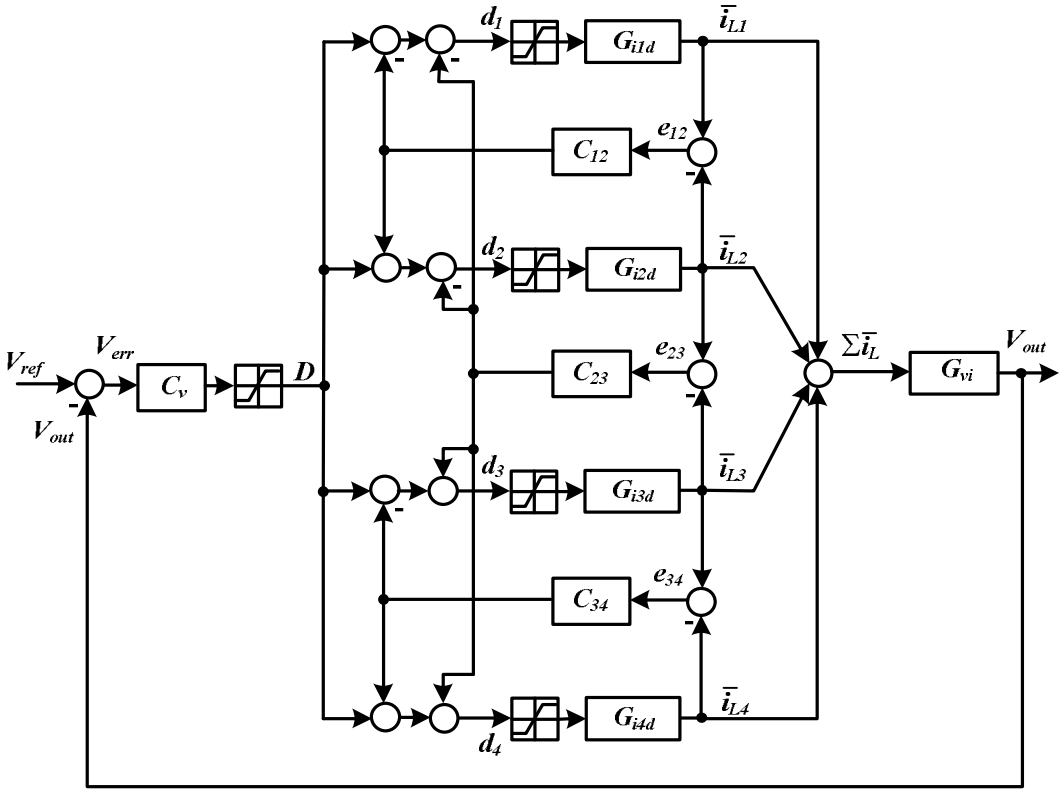

Figure 6.4: The proposed control architecture as applied to a 4-phase interleaved converter

The current sharing scheme shown above is for two-phase converter. The

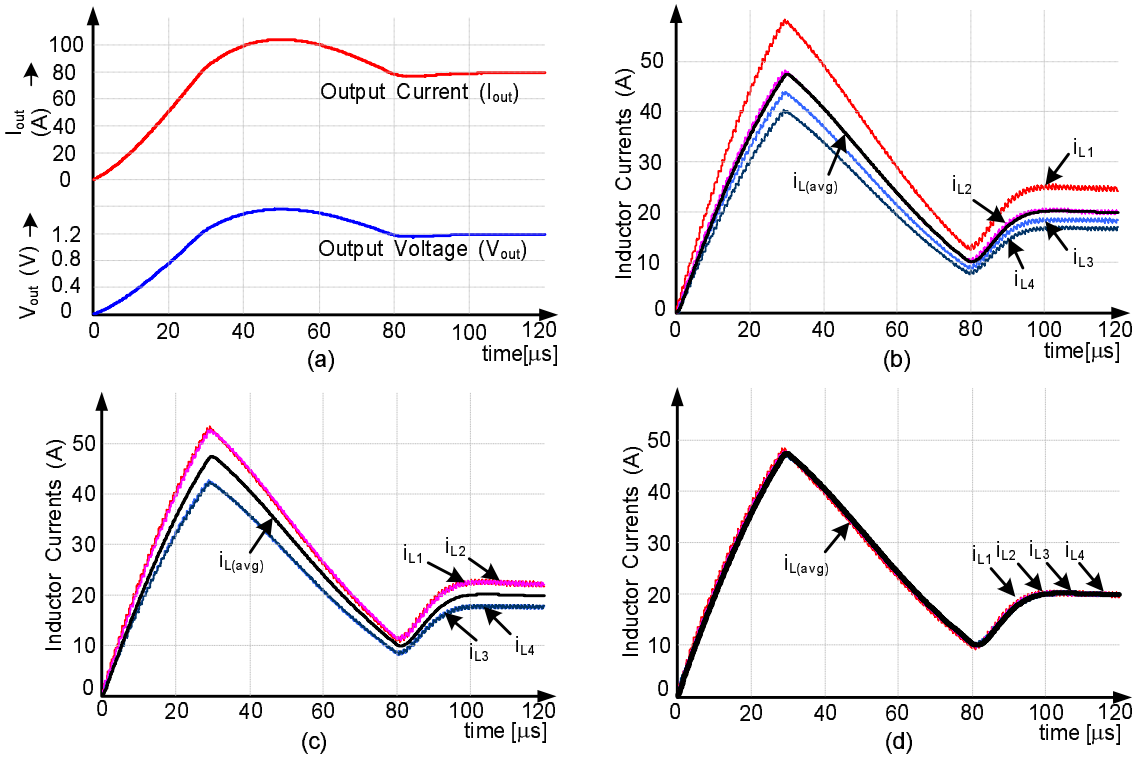

Figure 6.5: Simulation results showing the performance of the scheme during startup transient (a) Output voltage and output current, (b) Distribution of load current among individual phases, (c) Mismatch between i_{L1}, i_{L2} and i_{L3}, i_{L4} and (d) Balanced inductor currents using proposed scheme

scheme is scalable in nature and can be extended to any number of paralleled converters. Fig. 6.4 shows the scheme as applied to a 4-phase interleaved converter. The duty ratio compensation is applied based on the difference between any two phases. Compensating the duty ratios based on $\bar{e}_{12} = \bar{i}_{L1} - \bar{i}_{L2}$ and $\bar{e}_{34} = \bar{i}_{L3} - \bar{i}_{L4}$ will ensure these errors go to 0, however, there may still be current offsets between $\bar{i}_{L1}, \bar{i}_{L2}$ and $\bar{i}_{L3}, \bar{i}_{L4}$.

This can be observed in Fig. 6.5 which shows the simulation results when the proposed scheme is applied to a 4-phase interleaved converter. In order to have non-identical phases, the inductance values were changed. The following parameters

are used for the simulation: $V_{in} = 5V$, $V_{ref} = 1.2V$, $I_{out} = 80A$, $L_1 = 1.0\mu H$, $L_2 = 1.2\mu H$, $L_3 = 1.3\mu H$, $L_4 = 1.4\mu H$ and $f_s = 1MHz$ per phase. The system was simulated using SIMPLORER Simulation System [73]. Fig. 6.5(a) shows the output voltage and output current during the start-up transient and during the steady-state while Fig. 6.5(b) shows the distribution of the load current among the individual converters. It also shows the average of the output current of the individual converters ($i_{L(avg)}$). Fig. 6.5(c) shows the distribution of load current when the duty ratios are compensated based on $\overline{e}_{12} = \overline{i}_{L1} - \overline{i}_{L2}$ and $\overline{e}_{34} = \overline{i}_{L3} - \overline{i}_{L4}$. As seen from the simulation results, average output currents $\overline{i}_{L1}$ and $\overline{i}_{L2}$ match (i.e. $\overline{e}_{12} = 0$) and average output currents $\overline{i}_{L3}$ and $\overline{i}_{L4}$ match (i.e. $\overline{e}_{34} = 0$), however, the offsets are still to be compensated between $(\overline{i}_{L1}, \overline{i}_{L2})$ and $(\overline{i}_{L3}, \overline{i}_{L4})$. To compensate the mismatch between these two pairs $(\overline{i}_{L1}, \overline{i}_{L2})$ and $(\overline{i}_{L3}, \overline{i}_{L4})$ an extra compensation based on $(\overline{i}_{L(1,2)} - \overline{i}_{L(3,4)})$ is used. Using $\overline{e}_{23} = \overline{i}_{L2} - \overline{i}_{L3}$ and compensating for their mismatch, the average output currents $\overline{i}_{L2}$ and $\overline{i}_{L3}$ can match (i.e. $\overline{e}_{23} = 0$). This can be verified from Fig. 6.5(d) which shows the distribution of load currents in the four phases.

6.2.4 Stability Analysis

The scheme presented in Fig. 6.3 can be simplified as shown in Fig. 6.6. For the sake of simplicity only one of the phase is shown. Under steady state operation, the voltage error approaches 0 ($V_{err} \rightarrow 0$). Hence a PI controller controlling the voltage will give a constant duty ratio output (D). However, applying the same

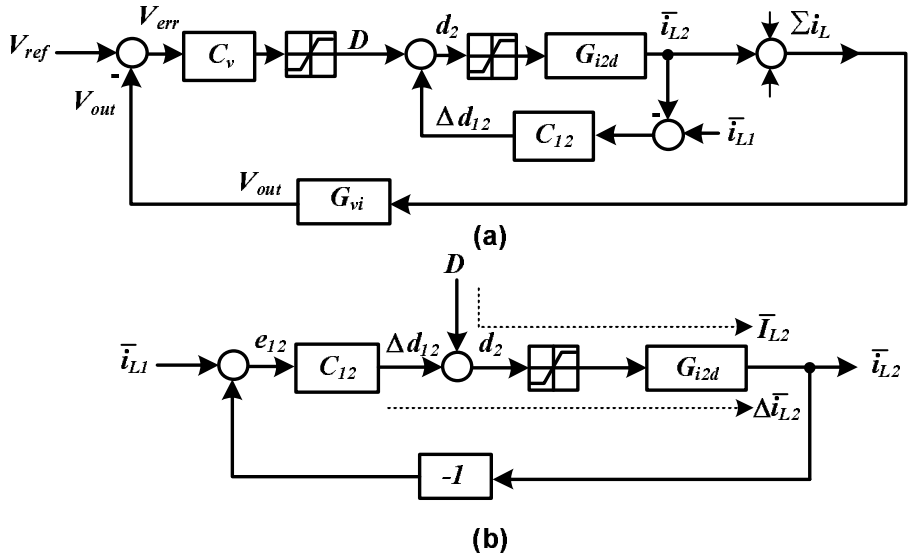

Figure 6.6: (a) Simplified control architecture based on duty ratio compensation for achieving current sharing (b) Constant duty ratio D being updated based on current mismatch

duty ratio to various phases results in different inductor currents. Here $\bar{i}_{L1}$ and $\bar{i}_{L2}$ are the average inductor current of phase 1 and 2 respectively and $\bar{e}_{12} = \bar{i}_{L1} - \bar{i}_{L2}$ is the measure of mismatch in the two phase currents. It is desired that $\bar{i}_{L2}$ should follow $\bar{i}_{L1}$. Thus, the duty ratio of phase 2 is corrected as shown in Fig. 6.6(a).

For phase 2, assume that $\overline{I}_{L2}$ is the current due to steady state duty ratio (D) and $\Delta\bar{i}_{L2}$ is the change in current due to duty ratio correction (Δd_{12}), as shown in Fig. 6.6(b). Based on this, the transfer functions to describe the system can be obtained as following:

$$\bar{i}_{L2} = \frac{G_{i2d}}{1 + G_{i2d}C_{12}} D + \frac{G_{i2d}C_{12}}{1 + G_{i2d}C_{12}} \bar{i}_{L1} \tag{6.5}$$

where C_{12} is the current sharing controller and G_{i2d} is the control to inductor current transfer function for phase 2. Using this, the sensitivity (S) of closed-loop

transfer function to changes in the C_{12} can be evaluated as

$$S_{C_{12}}^{i_{L2}} = \frac{C_{12}}{i_{L2}} \frac{\partial i_{L2}}{\partial C_{12}} = \frac{1}{1 + G_{i2d} C_{12}} \tag{6.6}$$

Using (6.5) and (6.6), if the gain of loop transfer function is sufficiently high, closed-loop performance can be made insensitive to changes in G_{i2d} and the phase current $\bar{i}_{L2}$ follows $\bar{i}_{L1}$. But this may not result in a stable system. For maintaining the stability of the system, the inductor current balancing control is analyzed to determine the upper bound of controller gain. Using (6.1), the duty ratio is adjusted such that the average currents are balanced. An increase in the duty ratio of one converter results in increase in output current of that converter. The output current of other converter(s) will decrease so as to maintain the same total current. If $\bar{e}_{12} = \bar{i}_{L1} - \bar{i}_{L2}$ is the current mismatch, then for a damped system we have to compensate for $\bar{e}_{12}/2$. Thus, for a stable system, we have the inequality as

$$|\Delta d_{12}(k).V_{in}(k).\frac{T_s}{L}| \leq |\bar{e}_{12}| \tag{6.7}$$

Thus, the upper bound of the gain is obtained as

$$\frac{\Delta d_{12}(k)}{\bar{e}_{12}(k)} \leq \frac{L}{V_{in} \cdot T_s} \tag{6.8}$$

This upper bound ensures that the change in duty ratio ($\Delta d_{12}(k)$) should not be such that it changes the sign of the current error. Since the change in current is proportional to the change in the duty ratio, thus a simple low-gain P-control can be used to balance the inductor currents. Substituting the values ($V_{in} = 5V$, $L = 1.2\mu H$, $T_s = 1\mu s$), the upper bound of gain is obtained as $\max |C_{12}| = 0.24$.

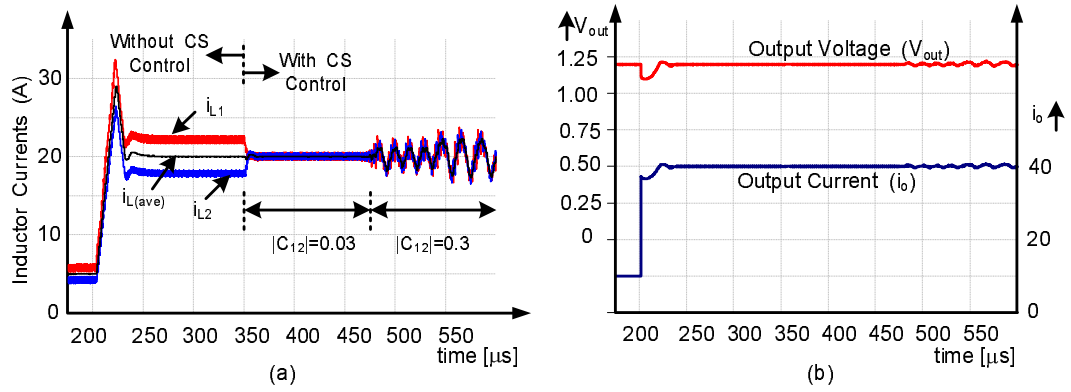

Figure 6.7: Simulation results showing the effect of increasing the gain of the current sharing controller

The unstable operation resulting from high-gain of current sharing (CS) controller can be observed in Fig. 6.7. It shows the simulation results when the proposed scheme is applied to a 2-phase interleaved converter. In order to have non-identical phases, the inductance values were changed. The following parameters were used for simulations: $V_{in} = 5V$, $V_{ref} = 1.2V$, $f_s = 1MHz$ per phase, $L_1 = 1.0\mu H$, $L_2 = 1.2\mu H$, $C_o = 2350\mu F$ and $r_c = 3m\Omega$. The system was subjected to a load change of 10A to 40A. Fig. 6.7(a) shows the distribution of load current among individual converters while Fig. 6.7(b) shows the output voltage and output current during the load transient. The current sharing controller was enabled at $t = 350\mu s$ with $|C_{12}| = 0.03$, resulting in sharing of average phase currents. However, it results in unstable operation when the gain of the current sharing controller (C_{12}) was increased to 0.3, which is greater than the limit given by (6.8).

6.2.5 Accuracy in current sharing

The accuracy in current sharing among various phases of a VRM is required to be within 10% of the rated output current [5]. The proposed scheme uses only a low gain P-control to achieve current sharing. Thus, due to the nature of the current sharing controller, there may still be current mismatch among the individual phases. The accuracy of current sharing can be obtained by evaluating the difference in the various inductor currents under steady state. For example, for a 2-phase system, the difference ($|i_{L1} - i_{L2}|$) can be studied as the measure of current sharing. The final value theorem is used to evaluate the measure of current sharing between phase i carrying current i_{Li} and phase j carrying a current of i_{Lj}.

$$\Delta I_{ij} = \lim_{s \to 0} |i_{Li} - i_{Lj}|, i \neq j \tag{6.9}$$

As mentioned earlier, the current mismatch $e_{ij} = i_{Li} - i_{Lj}$ is processed by C_{ij} to obtain the change in the duty ratio. We analyze a simple P-controller which is used as current sharing compensator. The upper limit on the gain of current sharing controller was established as $\max |C_{ij}| = 0.24$. In a fixed point implementation, we should have $e_{ij}(k).C_{ij} \geq 1$ for producing a minimal change in the duty ratio. Thus the accuracy of current sharing is $|e_{ij}(k)| \leq \frac{1}{|C_{ij}|}$. For example, in a typical digital implementation, where an ADC with resolution of V_q is used to sample the sensed current and the CS controller is $C_{ij} = \frac{1}{8} = 0.125$, then the current mismatch is

$$|e_{ij}| \leq 8.V_q \tag{6.10}$$

For an 8-bit ADC with a dynamic range of 3.3V ($V_q = 12.8mV$), we get the $|e_{ij}| \leq 0.1024$. Thus, with the sensing gain of 0.22V/A (when a full scale current of 15A results in 3.3V sensed output), the accuracy in current sharing is obtained as $\Delta I_{ij} \leq 0.465A$. In a multiphase VRM, where each phase carries a current of 15A, this control scheme will ensure 3.1% accuracy in current sharing, which is well within the 10% requirement of VRM 9.0 specifications.

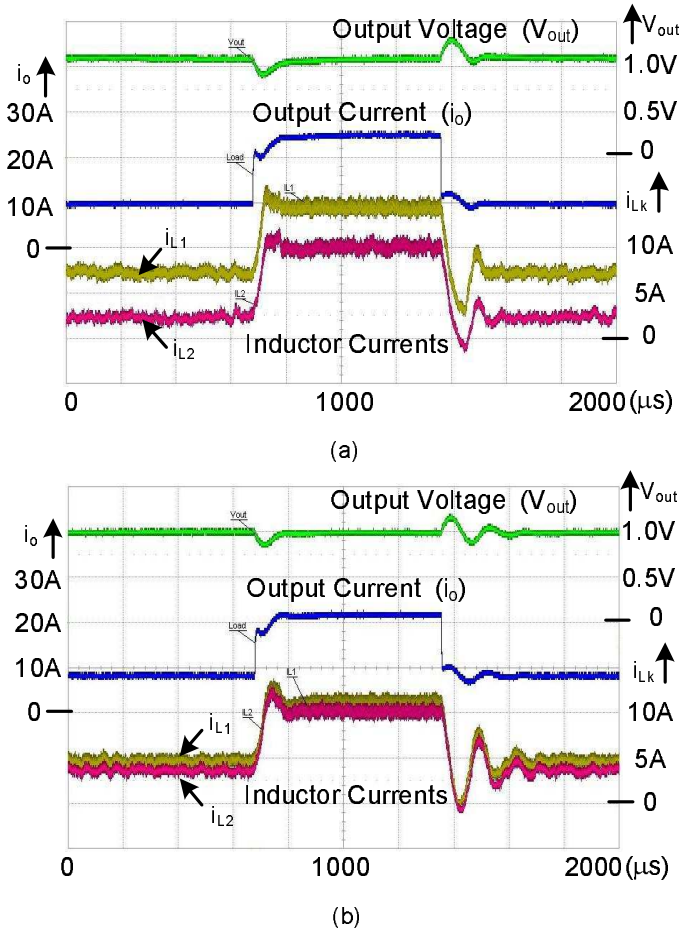

Figure 6.8: Experimental results showing the output voltage and distribution of inductor currents during load transients (a) Current controller is disabled (b) Result showing the dynamic performance of the controller when current controller is enabled

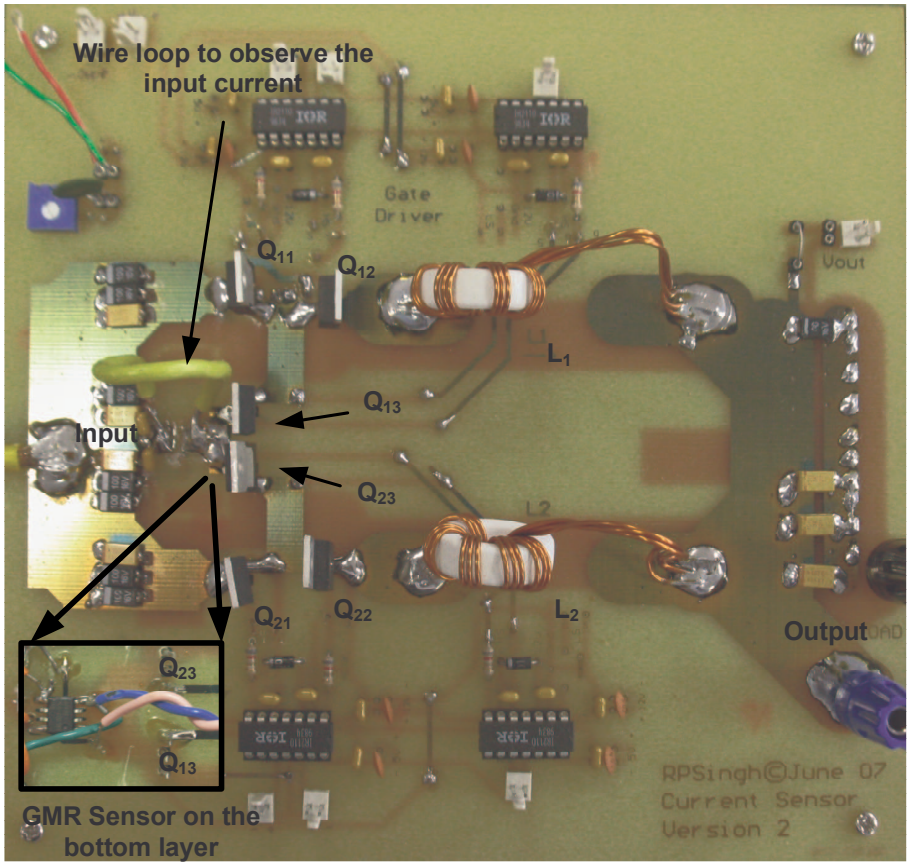

Figure 6.9: Experimental prototype of the two phase converter used to demonstrate the proposed current sensing scheme.

6.3 Experimental Results

The performance of the proposed method for current sensing was tested on a buck converter prototype with the following parameters: $V_{in} = 5\,V$, $V_{ref} = 1.25\,V$, $L = 1.2\mu H$, $C_o = 3200\mu F$ (tantalum), $f_{sw} = 1\,MHz$ and N=2 phases. Fig. 6.9 shows the prototype which was built in the laboratory. A wire loop used to verify the functionality of the sensing scheme. After the functionality was verified, the loop was replaced with a copper trace such that the current flows along the top layer. The GMR sensor AAL002 was used for current sensing with its supply

voltage at 12 V. The sensor was placed on the bottom layer of the PCB board and current was made to flow through the top layer. Since average current control is desired, the average value of the inductor current can be obtained by sensing the current in the middle of the switch-on and switch-off intervals. A digital controller was used to verify the performance of the system. In the prototype, the ADC had 8-bit resolution ($N_{ADC} = 8$) and DPWM had 6-bit of hardware resolution. Thus 3-bit digital dither was introduced to increase the effective resolution of DPWM module to 6+3=9 bits ($N_{DPWM} = 9$). The controller was implemented on a Spartan-3 FPGA board from Xilinx.

Fig. 6.8(a) shows the response of the system when the converter was subjected to load transients with a step-up change in the phase current from 5A per phase to 10A and vice versa. The load transients were generated by switching the load resistance. In order to see the current mismatch among the two phases, the current controller is disabled and is working with a voltage controller only. The reference voltage is set as 1V. Fig. 6.8(a) shows the distribution of the inductor currents in a voltage mode controlled multiphase converter. In order to test the performance of the current sensing and sharing method using a single current sensor, the current controller is enabled. Fig. 6.8(b) shows the response of the system when the converter was subjected to similar load transients. It shows good sharing of the inductor currents after compensating the duty ratios of the two phases.

These results were to test the performance of the current sensor under load dynamics. In practice the VRM output requires adaptive voltage positioning (AVP).

In adaptive voltage positioning, the output voltage of the VRM is adapted to changes in the load. This causes the output voltage to droop with the load. Adaptive voltage positioning was implemented by changing the reference voltage in accordance with the load current. Reference voltage is defined as $v_{ref} = V_{ref} - i_o \cdot R_{droop}$, where V_{ref} is the nominal reference voltage at no load conditions, i_o is the load current and R_{droop} is the droop resistance obtained from the load line. Fig. 6.10 shows the dynamic response of the controller with adaptive voltage positioning for a step change in load current from 10A to 25A and vice versa.

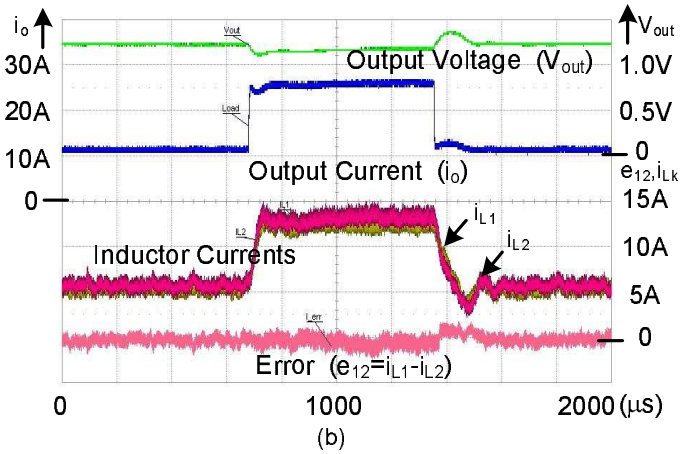

Figure 6.10: Experimental results showing the dynamic performance of the controller with adaptive voltage positioning for a step load change

6.4 Summary

Voltage mode-control can be used to obtain high bandwidth of the closed loop systems, however it does not ensure current distribution. Current mode control can be used but it requires individual current loops and hence it will require N-sensors for N-paralleled converters. Reducing the number of sensors impose

an extra computational overhead on the current sharing controller. Thus, a current sharing scheme is presented, which uses single sensor to sense the individual currents. The scheme is independent of the number of converters in the paralleled system. A GMR based current sensor is used which is practically lossless. The proposed sharing scheme can be implemented easily on a digital platform and provides various functionalities of a voltage regulating module. The proposed scheme is independent of the number of converters in the paralleled system. The functionality of the current sensing method is experimentally verified on a 2-phase interleaved buck converter, both under steady state and under load transients.

Current sensing is used for providing various functionalities in DC-DC converters. It may be used for over-current protection or for achieving load sharing among paralleled converters. It may also be used for implementing current-mode control for improving the transient response of the closed loop system. The current mode control will improve the transient response of the system, but the response gets limited by the slew rate of the inductor current. For a buck converter with large conversion ratio ($V_{in} >> V_{out}$), the step-down transients last longer than the step-up transients. To this end, the next chapter develops a new circuit topology, which helps in improving the step-down transient response in such a buck converter.

Chapter 7

Improving the Step-Down Transient Response

7.1 Introduction

During a step-down load transient, a large amount of charge is absorbed by the output capacitor in a very short time. This results in an overshoot in the output voltage. Similarly, during a step-up load transient, capacitor removes the required charge so as to meet the load current demand. This results in a voltage undershoot if the capacitor cannot provide the required current sufficiently fast. In a buck converter, the inductor voltage determines the slew rates during step-up (ρ_u) and during step-down load transients (ρ_d), as illustrated using Fig. 7.1. Due to different slew rates, an asymmetrical transient response occurs during increase and decrease in load.

The slew rates depend upon the voltage across the inductor and are given as:

$$\rho_u = \frac{di_L}{dt}|_{up} = \frac{V_{in} - V_{out}}{L} \tag{7.1}$$

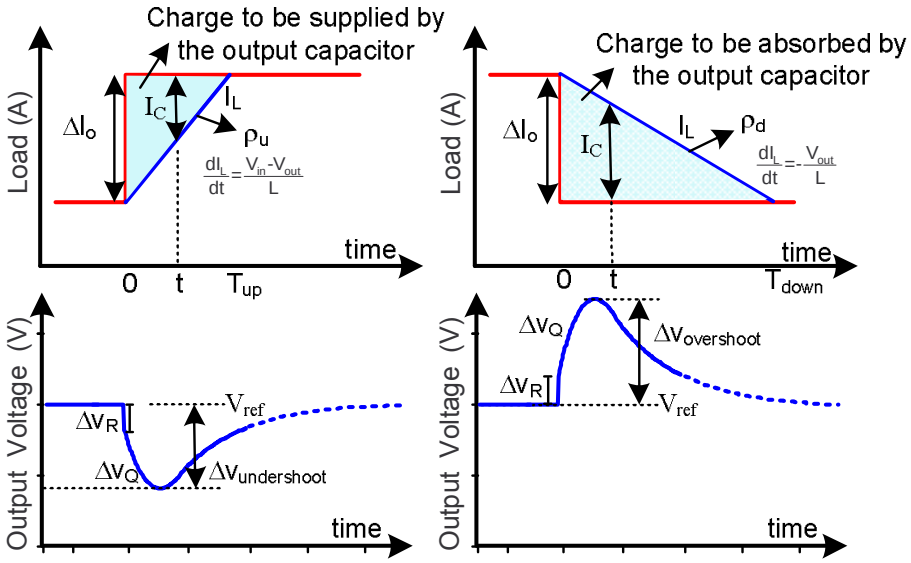

Figure 7.1: Charging and discharging of the output capacitor during sudden change in load current

$$\rho_d = \frac{di_L}{dt}|_{down} = -\frac{V_{out}}{L} \tag{7.2}$$

For a given change in load current (ΔI_o), the time taken by the inductor current to attain the new value will be $T_{up} = \frac{\Delta I_o}{\rho_u}$ and $T_{down} = \frac{\Delta I_o}{\rho_d}$ respectively. The step-down transient will last longer than the step-up transient if it satisfies the following condition,

$$T_{down} > T_{up} \tag{7.3}$$

$$\frac{\Delta I_o}{\rho_d} > \frac{\Delta I_o}{\rho_u} \tag{7.4}$$

$$\frac{\Delta I_o \cdot L}{V_{out}} > \frac{\Delta I_o \cdot L}{V_{in} - V_{out}} \tag{7.5}$$

This can be simplified as

$$V_{in} > 2 \cdot V_{out} \tag{7.6}$$

Since (7.6) is normally the case for a low conversion ratio buck converter, the rate of increase of inductor current is much higher as compared to the rate of decrease of

inductor current. Thus, for a given change in load current, the charge supplied by output capacitor is smaller than the charge absorbed by the capacitor. This results in larger voltage overshoot as compared to the voltage undershoot. The following example evaluates the condition which results in larger overshoot as compared to the undershoot.

The undershoot of output voltage for a ΔI_o step-up change in load current can be obtained as (see Appendix A)

$$\Delta v_{undershoot} = \frac{1}{2}(\frac{\Delta I_o^2}{\rho_u.C_o} + \rho_u.r_c^2.C_o), \frac{\Delta I_o}{\rho_u} > r_c.C_o \tag{7.7}$$

$$\Delta v_{undershoot} = \Delta I_o.r_c, \frac{\Delta I_o}{\rho_u} \leq r_c.C_o \tag{7.8}$$

where r_c is the effective series resistance of the output capacitor, C_o is the output capacitance and ρ_u is the slew rate of the inductor current. Similarly, the voltage overshoot for the same step-down change in load current can be obtained as

$$\Delta v_{overshoot} = \frac{1}{2}(\frac{\Delta I_o^2}{\rho_d.C_o} + \rho_2.r_c^2.C_o), \frac{\Delta I_o}{\rho_d} > r_c.C_o \tag{7.9}$$

$$\Delta v_{overshoot} = \Delta I_o.r_c, \frac{\Delta I_o}{\rho_d} \leq r_c.C_o \tag{7.10}$$

where ρ_d is the rate of change of inductor current.

Assuming $\frac{\Delta I_o}{\rho_u} > r_c.C_o$ and $\frac{\Delta I_o}{\rho_d} > r_c.C_o$, the voltage overshoot will be higher than the voltage undershoot, if the following condition is satisfied:

$$\Delta v_{overshoot} - \Delta v_{undershoot} > 0 \tag{7.11}$$

$$\frac{1}{2}(\frac{\Delta I_o^2}{\rho_d.C_o} + \rho_d.r_c^2.C_o) - \frac{1}{2}(\frac{\Delta I_o^2}{\rho_u.C_o} + \rho_u.r_c^2.C_o) > 0 \tag{7.12}$$

The above expression can be simplified as

$$\frac{1}{2}(\rho_u - \rho_d)[\frac{\Delta I_o^2}{\rho_u.\rho_d.C_o} - r_c^2.C_o] > 0 \tag{7.13}$$

Using (7.6), the slew rates have the relation $\rho_u > \rho_d$. Thus for (7.13) to be true,

$$\Delta I_o > r_c.C_o.\sqrt{\rho_u.\rho_d} \tag{7.14}$$

Using (7.1) and (7.2), this can be simplified as

$$\Delta I_o > \frac{r_c.C_o}{L}.\sqrt{(V_{in} - V_{out}).(V_{out})} \tag{7.15}$$

Similarly, in another case when $\frac{\Delta I_o}{\rho_u} < r_c.C_o$ and $\frac{\Delta I_o}{\rho_d} > r_c.C_o$, the difference between voltage overshoot and undershoot is

$$\Delta v_{overshoot} - \Delta v_{undershoot} > 0 \tag{7.16}$$

$$\frac{1}{2}(\frac{\Delta I_o^2}{\rho_d.C_o} + \rho_d.r_c^2.C_o) - (\Delta I_o.r_c) > 0 \tag{7.17}$$

$$(\Delta I_o - \rho_d.r_c.C_o)^2 > 0 \tag{7.18}$$

which is always true. Using the relation $\frac{\Delta I_o}{\rho_2} > r_c.C_o$, it can be established that for an asymmetrical transient response, the load change should satisfy

$$\Delta I_o > \rho_d.r_c.C_o \tag{7.19}$$

As a design example, the following parameters are used $V_{in} = 5\,V$, $L = 1.2\mu H$, $C_o = 408\mu F$ (tantalum) and $r_c = 1\,m\Omega$. Using the above analysis, it can be deduced that $\Delta I_o > 0.34\,A$ at an output voltage of $1\,V$ will produce an asymmetrical transient response. This can also be seen from Fig. 7.2 which shows

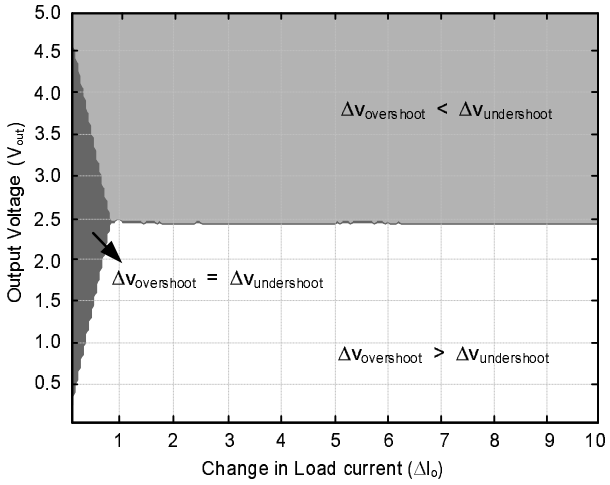

Figure 7.2: Region showing the comparison of voltage overshoot and undershoot for load transients of different magnitudes

the comparison of voltage overshoot and voltage undershoot for load transients of different magnitudes at various output voltages.

If the change in load current satisfies (7.15) or (7.19) depending upon the time constant of the output capacitance ($r_c.C_o$), it will result in an asymmetrical transient response with a higher voltage overshoot than the undershoot. One way to reduce the overshoot is to increase the size of the output capacitance. This is undesirable as it increases the size of the voltage regulating module. Another way to reduce the voltage overshoot is to decrease the inductor current faster. However, the rate of change of inductor current depends on the value of circuit inductance and the voltage across the inductance $|di_L/dt| = |v_L/L|$. The magnitude of the slew rate can be increased by increasing the magnitude of the voltage across the inductor or by reducing the inductance value.

In the past various methods have been proposed to improve the transient re-

sponse of the system. These methods rely on one or more of the following methods:

- Increasing the size of the output capacitor to reduce the voltage overshoot
- Reducing the circuit inductance so as to increase the rate of change of inductor current [10],[54],[55]
- Using feed-forward techniques to shape the load characteristics [56] - [58]
- Using non-linear control action during the load transients [59]- [64]
- Including an additional clamping circuit to limit the voltage overshoot [65], [66].

The above mentioned methods, either try to reduce the inductance value or incorporate non-linear control action during the load transients. Reducing the inductance results in higher inductor current ripple and hence results in higher losses. On the other hand, a non-linear control action would saturate the controller faster. It would change the speed of the response to disturbance but the maximum slew rate gets limited by the inductance value and the voltage across it. Thus, there are limitations in these past approaches and they can not be directly applied to meet the challenging requirements of high currents at high slew rates and tight voltage regulation.

In a buck converter, when the high side MOSFET is turned off, the voltage across the inductor is $v_L = -V_{out}$, which limits the slew rate of inductor current during a step-down load transient. In the proposed scheme, the slew rate during

such a transient is increased by increasing the magnitude of voltage across the inductors. The voltage across the inductor is changed by applying negative input voltage across it. Fig. 7.3 shows the proposed topology and the three modes of operation.

In the proposed scheme, the voltage across the inductor is changed during transient load. During transients, the fast rate of change of inductor current is achieved by applying a negative voltage across the inductor. When the load transient is over and the fast rate of change is no longer required, the voltage across the inductor is reduced and eventually restored to its original value. In doing so, the steady state ripple is kept to a minimum while providing fast dynamics during transients.

The proposed scheme, by increasing the slew rate of the inductor current in DC-to-DC converters, achieves the following:

1. Reduced voltage overshoots during load transients in DC to DC converters.
2. Faster settling times of output voltage during transients.
3. Smaller output capacitor as it can provides reduced voltage undershoots.
4. Maintains a lower ripple current in the inductor of DC to DC converters.

In short, the proposed scheme is capable of providing fast dynamic performance during transients without significantly deteriorating the steady state behavior.

7.2 Proposed Scheme: Working Principle

A sudden decrease in the load current will cause an overshoot in the output voltage. To mitigate this overshoot effect, the current absorbed by the output capacitor of the DC to DC converter during such a transient has to be decreased. This is achieved by changing the slew rate of the inductor current. For a constant value of inductance, the slew rate depends on the voltage across the inductor. It is proposed to increase this rate during the load transients. The increased rate has to be sustained as long as the load is changing and is restored to its original value once the transient is over.

Fig. 7.3 shows the proposed topology. It is derived from the conventional buck converter topology. Switch Q_1 and D_1 comprises of the conventional buck converter. In the proposed scheme, Q_2 and D_2 are added. During the steady state operation, switch Q_2 is kept on. As a result, it works as a normal buck converter, with Q_1 as its high-side switch and diode D_1 as the free-wheeling diode. However, during step-down load transients, Q_2 is disabled and the current is forced through D_2. It may be noted that during step-down transients, the circuit disconnects the input voltage ground from the output voltage ground. Thus, the proposed scheme requires a floating power supply. The main power source for the VRM on mother board is 12V, which is obtained from a Switched Mode Power Supply (SMPS). The SMPS is essentially a full bridge rectifier followed by a forward converter. The output of such a transformer based power converter is floating which can be used

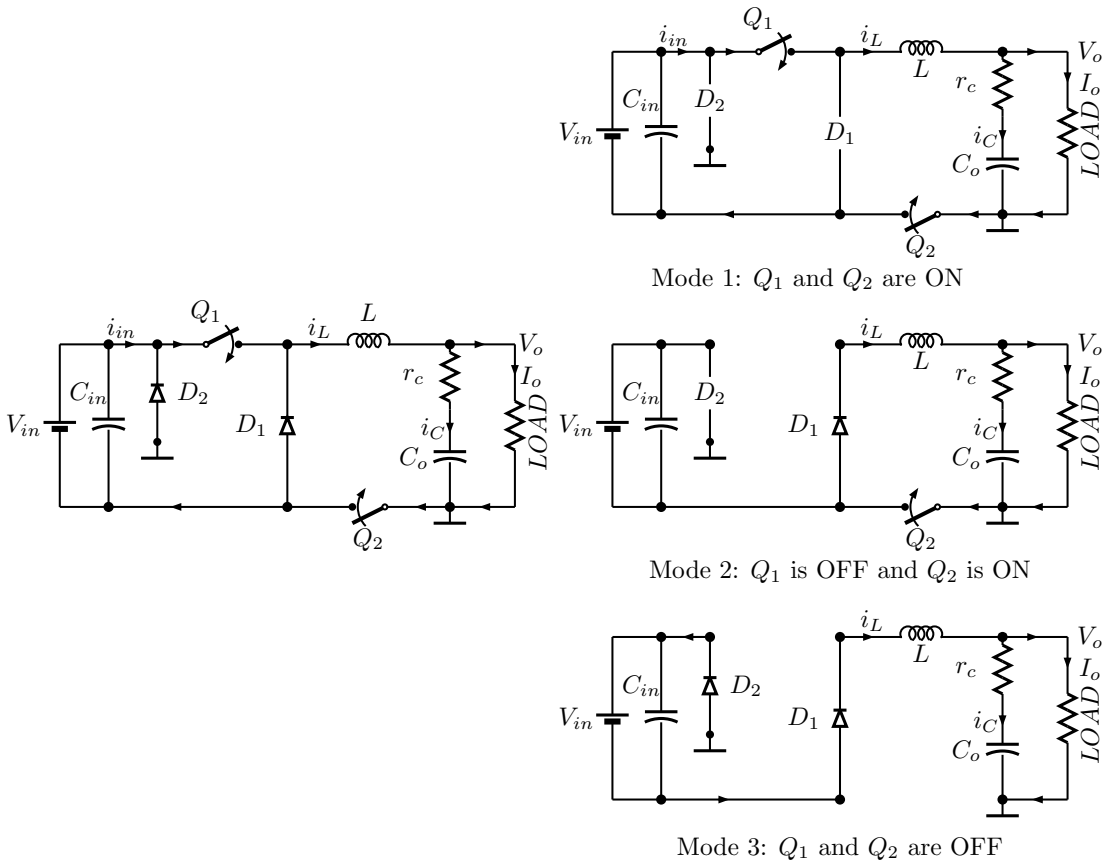

Figure 7.3: (a) The proposed converter for improving the step-down load transients. (b) Equivalent circuit during its three modes of operation.

as the input for the proposed scheme.

The operation of the circuit can be divided into three modes. The equivalent circuit during these modes are given in Fig. 7.3(b)

Mode 1: Q_1 and Q_2 are on and the inductor current is increasing. The voltage across the inductor is $v_L = V_{in} - V_{out}$.

Mode 2: Q_1 is turned off, while Q_2 is still on. The inductor current flows through the free-wheeling diode D_1. As a result, the current in the inductor is

decreasing. The voltage across the inductor is $v_L = -V_{out}$.

Mode 3: Q_1 and Q_2 are turned off. The inductor current flows through D_2, D_1 and through the input capacitance. The voltage across the inductor is $v_L = -V_{in} - V_{out}$. As a result, the inductor current decreases at a much higher rate.

It may be noted that Mode 1 and Mode 2 are similar to the conventional buck converter. In addition to these, Mode 3 is introduced during step-down load transients so as to improve the dynamic response of the system. In the conventional buck converter, the inductor current will decrease with a rate of $-V_{out}/L$ while in the proposed scheme, it can decrease at a rate of $(-V_{in} - V_{out})/L$. Thus for a given change in load current (ΔI_o), the time taken for the inductor current to fall to the new level can be obtained as:

$$T|_{conv} = \frac{\Delta I_o \cdot L}{V_{out}} \tag{7.20}$$

$$T|_{proposed} = \frac{\Delta I_o \cdot L}{V_{out} + V_{in}} \tag{7.21}$$

This gives us the improvement over the conventional scheme as

$$\frac{T|_{proposed}}{T|_{conv}} = \frac{V_{out}}{V_{in} + V_{out}} \tag{7.22}$$

Assume that the output voltage does not change appreciably and is held constant during such a transient. Thus, for $V_{in} = 5V$ and $V_{out} = 1V$, it will provide a 6x improvement in the fall time. In this analysis, we have assumed ideal diodes and ideal switches. A more accurate analysis can be obtained by considering the voltage drop across these devices.

7.2.1 Switching Algorithm

Since it is intended to increase the slew rate of inductor current, it needs to have a switching algorithm which decides to operate the converter in Mode 3, as described above. The working of the error based control algorithm is explained using the current loop only. Later the idea can be extended to obtain the algorithm based on the output voltage.

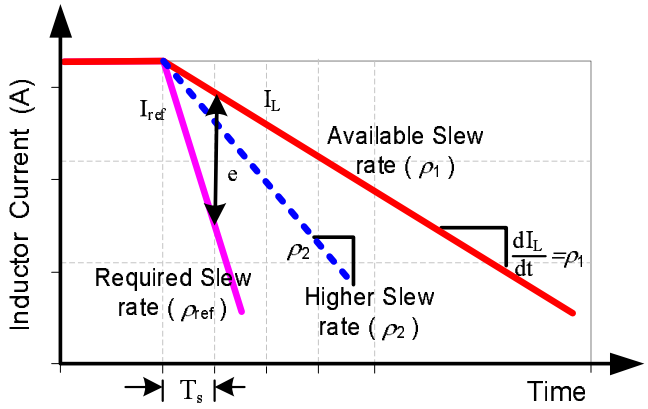

Figure 7.4: Difference in the slew rates - required and available

Current Mode Control: Suppose there is a sudden change in reference current at time $t = 0$. The available slew rate due to circuit inductance is ρ_1 A/s while the required rate is ρ_{ref} A/s ($\rho_{ref} > \rho_1$), as shown in Fig. 7.4. A higher rate of ρ_2 A/s is also available by operating the converter in Mode 3, as described above. In a current mode controlled converter, current error is processed. By the end of one sampling instance, the current error in the normal case will be $e = (\rho_{ref} - \rho_1).T_s$ where T_s is the sampling period. The idea here is to minimize the error by increasing the available slew rate ρ_1 to ρ_2. By using ρ_2, the error will be $e = (\rho_{ref} - \rho_2).T_s$. Thus it will reduce the error by $\Delta e = (\rho_2 - \rho_1).T_s$. This can

be used as the current threshold for the proposed design.

$$e_{th} = (\rho_2 - \rho_1).T_s \tag{7.23}$$

If the error is higher than the e_{th}, the converter is switched to Mode 3 operation, otherwise it continues to operate with its normal conditions. For example, in a buck converter with $V_{in} = 5V$, $V_{out} = 1V$ and having an inductance of $1\mu H$, a slew rate of $1A/\mu s$ is available during the step down operation. Using the proposed scheme, will correspondingly achieve $6A/\mu s$. Thus, if the error after a duration T_s is higher than e_{th}, that is $e > (6-1).T_s$, then the converter is operated in Mode 3, else it continues in its normal operation.

The proposed scheme was first tested on a buck converter having only the current loop. The converter parameters are $V_{in} = 5V$, $C_o = 408\mu F$, $L = 1.2\mu H$, $f_s = 1MHz$. The system was subjected to a 10A step change in reference current (I_{ref}) from 15A to 5A. For a given controller, the performance was compared with the normal case. Same controller was used in both the cases, except that an additional Mode 3 was used as per the proposed scheme. An over current signal based on the current error was used to switch to Mode 3 operation. It is seen from the simulation results in Fig. 7.5, the fall time and the settling time are improved by increasing the magnitude of voltage across the inductor during transients.

Voltage Mode Control: A switching algorithm based on output voltage can also be formulated, which increases the slew rate during the step-down operation, so as to keep the voltage overshoot within the permissible limits.

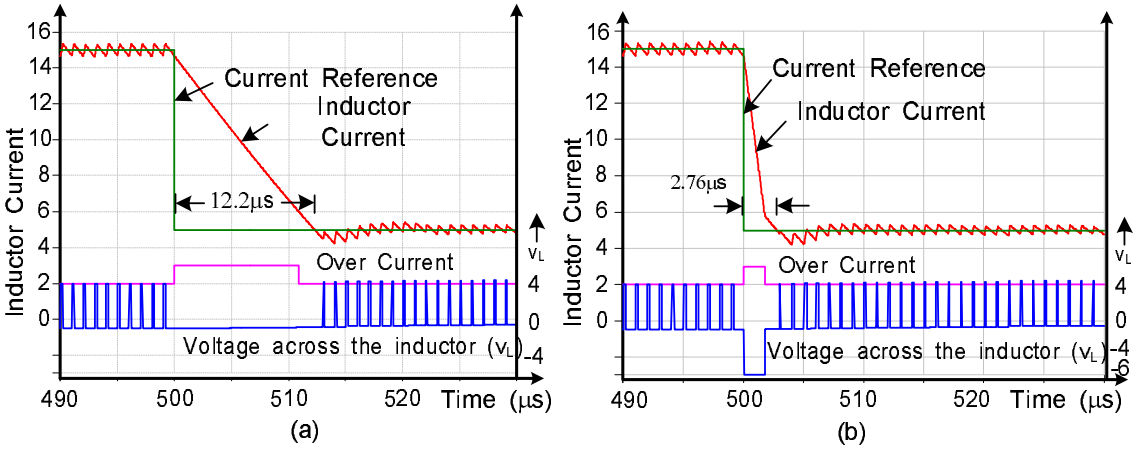

Figure 7.5: Simulation result showing the performance of the proposed scheme during a step change in current reference. (a) Conventional Scheme (b) Proposed scheme using the same converter parameters as the conventional scheme

Consider a power converter having its output voltage regulated at V_{ref}. During a step-down load transient, a large amount of charge is added to the capacitor in a very short time. This results in an overshoot in the output voltage. Two factors contribute to the voltage drop; voltage drop due to resistance $dV_R = i_c.r_c$, and voltage drop due to discharge of the capacitor $dV_Q = \Delta Q(t)/C_o$. Here, C_o is the output capacitor and r_c is the effective series resistance of the capacitor.

A hysteresis based control algorithm is also established which is used to switch the mode of operation, so as to obtain an improved transient response. In such a method, two threshold voltages are defined above the nominal output voltage (V_H and V_L), with $V_H > V_L$. While the output voltage remains below the upper threshold (V_H) converter is working with the normal conditions. If the step-up load transient is observed, the output voltage will start to increase. Once the output voltage increases above the upper threshold (V_H), the Mode 3 is enabled and the converter starts to respond with increased slew rate. The normal operation is re-

stored, once the output voltage falls below the lower threshold voltage (V_L). The thresholds can be chosen smaller than the limits imposed by the output voltage regulation specifications under load dynamics. This will ensure the voltage overshoot remains within the permissible limits. It can be verified by using the following example, in which the higher slew rate is switched after the output voltage has increased to a certain level.

In this analysis, ρ_1 is the available slew rate and the higher slew rate (ρ_2) is applied at a time instance t_1 during the load transient, as shown in Fig. 7.6. At any any arbitrary instance t ($t > t_1$), the capacitor current can be evaluated as

$$i_c(t) = \Delta I_o - \rho_1 t_1 - \rho_2(t - t_1) \tag{7.24}$$

The charge absorbed by the capacitor during the interval $(0 - t_1)$ is given by

$$\Delta Q_1(t) = \frac{1}{2} t_1(2\Delta I_o - \rho_1 t_1) \tag{7.25}$$

where ΔI_o is the change in the load current. The charge absorbed by the capacitor during the interval $(t_1 - t)$ is given by

$$\Delta Q_2(t) = \Delta I_o(t - t_1) + (\rho_2 - \rho_1)t_1 t - (\rho_2 - \rho_1)t_1^2 + +\frac{1}{2}\rho_2(t_1^2 - t^2) \tag{7.26}$$

Thus, the total charge absorbed by the output capacitor in time $(0 - t)$ is $\Delta Q_1 + \Delta Q_2$, which is obtained as

$$\Delta Q(t) = \Delta I_o t + (\rho_2 - \rho_1)t_1 t - \frac{1}{2}(\rho_2 - \rho_1)t_1^2 - \frac{1}{2}\rho_2 t^2 \tag{7.27}$$

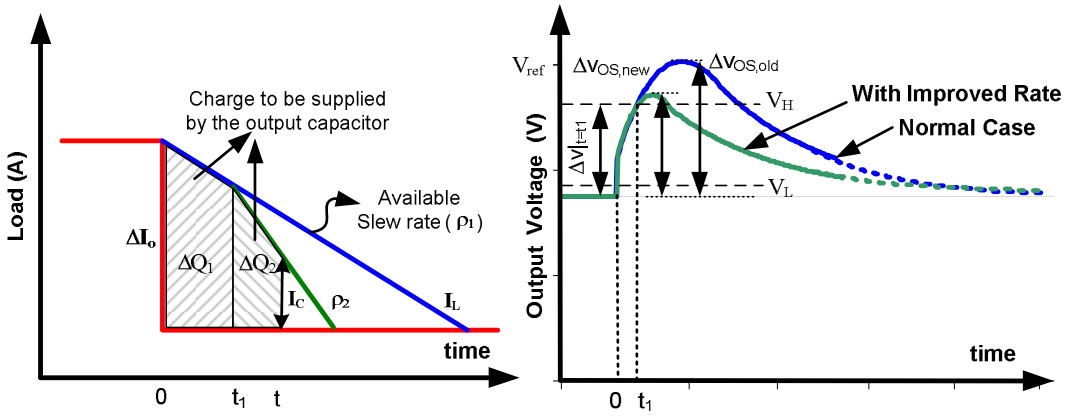

Figure 7.6: Typical waveforms during step change in the load. The input voltage is switched after time t_1

The voltage overshoot during such a case can be expressed as,

$$\Delta v(t) = \frac{\Delta Q(t)}{C_o} + i_c(t).r_c$$

$$\Delta v(t) = \frac{\Delta I_o}{C_o}t + (\rho_2 - \rho_1)(\frac{t_1 t}{C_o} - \frac{1}{2}\frac{t_1^2}{C_o}) - \frac{\rho_2 t^2}{2C_o} + (\Delta I_o - \rho_1 t_1 - \rho_2(t - t_1))r_c \quad (7.28)$$

The overshoot will be maximum, when $\frac{\Delta v(t)}{dt} = 0$. The time instance can be obtained as

$$t = \frac{1}{\rho_2}(\Delta I_o + (\rho_2 - \rho_1)t_1 - \rho_2 r_c C_o) \quad (7.29)$$

Substituting this t in (7.28), overshoot is obtained as

$$\Delta v_{OS,new} = \frac{1}{2C_o\rho_2}[\Delta I_o^2 + C_o^2\rho_2^2 r_c^2 + 2\Delta I_o(\rho_2 - \rho_1)t_1 + \rho_1(\rho_1 - \rho_2)t_1^2] \quad (7.30)$$

The normal case voltage overshoot can be obtained by substituting $\rho_1 = \rho_2$ and $t_1 = 0$ in (7.30) as

$$\Delta v_{OS,old} = \frac{1}{2}(\frac{\Delta I_o^2}{\rho_1.C_o} + \rho_1.r_c^2.C_o) \quad (7.31)$$

For the proposed scheme to be effective, the voltage overshoot should decrease by

increasing the slew rate,

$$\Delta v_{OS,old} - \Delta v_{OS,new} > 0 \tag{7.32}$$

$$\frac{\rho_2 - \rho_1}{2C_o\rho_1\rho_2}[-C_o^2 r_c^2 \rho_1\rho_2 + (\Delta I_o - \rho_1 t_1)^2] > 0 \tag{7.33}$$

Since $\rho_2 > \rho_1$, the above expression is simplified as

$$[-C_o^2 r_c^2 \rho_1\rho_2 + (\Delta I_o - \rho_1 t_1)^2] > 0 \tag{7.34}$$

This is a quadratic equation in t_1. This gives us the time instance before which the higher slew rate should be switched on so as to reduce the voltage overshoot.

$$t_1 < \frac{\Delta I_o}{\rho_1} \pm C_o r_c \sqrt{\frac{\rho_2}{\rho_1}} \tag{7.35}$$

The value with the plus sign corresponds to the time instance after the transient is over. Thus the value with the negative sign is retained .

$$t_1 < \frac{\Delta I_o}{\rho_1} - C_o r_c \sqrt{\frac{\rho_2}{\rho_1}} \tag{7.36}$$

Under the limiting case, the maximum value of time interval is obtained when t_1 approaches its upper limit. The voltage change at this instance is obtained by substituting

$$t_1 = \frac{\Delta I_o}{\rho_1} - C_o r_c \sqrt{\frac{\rho_2}{\rho_1}} \tag{7.37}$$

in (7.28). The voltage change is obtained as

$$\Delta v(t)|_{t=t_1} = \frac{\Delta I_o^2}{2C_o\rho_1} + C_o r_c^2 \sqrt{\rho_1\rho_2} - C_o r_c^2 \rho_2 \tag{7.38}$$

Thus, for the given load change (ΔI_o), if the Mode 3 is switched before the voltage rises by the value given in (7.38), the overshoot can be reduced. This sets the limit

on the threshold values (V_H) for the hysteresis controller.

$$V_H \leq V_{ref} + \Delta v(t)|_{t=t_1} \tag{7.39}$$

$$V_H \leq V_{ref} + (\frac{\Delta I_o^2}{2C_o\rho_1} + C_o r_c^2 \sqrt{\rho_1\rho_2} - C_o r_c^2 \rho_2) \tag{7.40}$$

The threshold voltage is chosen such that it satisfies the limit imposed in (7.40). If the output voltage rises above the threshold voltage (V_H), the converter will switch to Mode 3, so as to increase the slew rate and hence to reduce the voltage overshoot during the load transient. This also corresponds to a time instance defined by (7.37). Applying the negative inductor voltage within time t_1, after the load transient occurs, will reduce the voltage overshoot. The input can be restored to its normal value once the output voltage decreases below the lower threshold voltage (V_L). The lower threshold is chosen close to the reference voltage such that $V_H > V_L$.

The above analysis was done for a buck converter having a voltage loop only. However, a cascaded voltage and current control loop is recommended for improved dynamic response. This is because, the main component of the solution that brings about the improvement is based on increase in inductor current slew rate, hence an inner current loop is advantageous. The foregoing analysis based on voltage controlled converters is also applicable for converters operating with cascaded control loops. In order to verify the this, a buck converter with the following parameters was simulated: $V_{in} = 5V$, $C_o = 408\mu F$, $r_c = 1m\Omega$, $L = 1.2\mu H$, $f_s = 1MHz$. The system was subjected to a 10A step change in load current (I_o) from 15A to 5A. The load transients were generated by switching the

load resistance. The converter was operated with cascaded control loops, where the reference voltage was kept constant as $V_{ref} = 1V$. For the given converter parameters, the upper limit on the voltage overshoot given in (7.38) is obtained as 145.7mV. A voltage overshoot of 40mV was used to enable the switching algorithm ($V_H = 1.040\,V$), which is within the limit obtained in (7.40). For a given controller, the performance was compared with the normal case. Same controller was used in both the cases, except that an additional error based switching algorithm was used to apply a higher magnitude of voltage across the inductor. It is seen from the simulation results in Fig. 7.7, the voltage overshoot and the settling time are improved by increasing the magnitude of the voltage across the inductor during the step-down transients. The increased input voltage helps in increasing the slew rate of the inductor current and hence results in faster transient response.

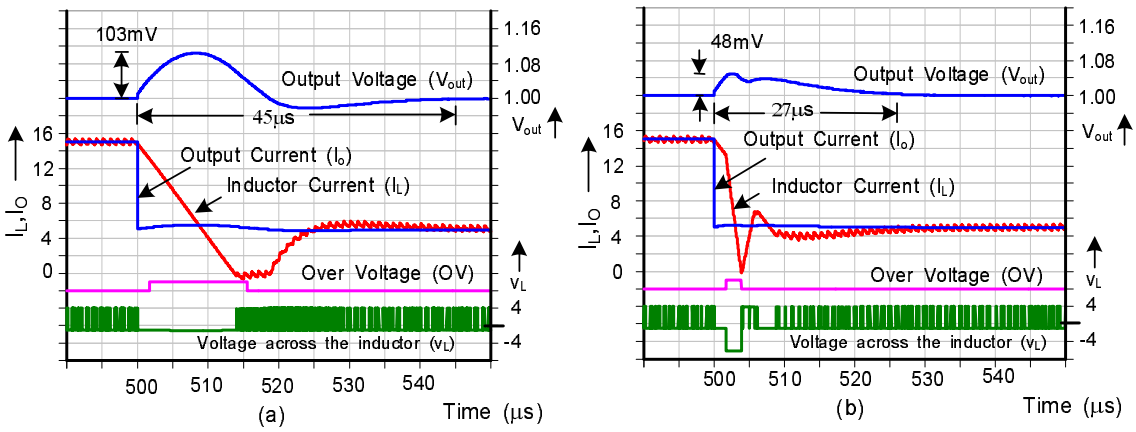

Figure 7.7: Simulation result showing the performance of the proposed scheme during a step change in load current. (a) Conventional Scheme (b) Proposed scheme using the same converter parameters as the conventional scheme

The above mentioned analysis was based on a buck converter so as to improve its transient response. These arguments can be extended to improve the step-down transient response of other topologies as well. It is concluded that it is possible

to increase the step-down slew rate of the inductor current without reducing the inductance. The increased slew rate results in faster transient response. This will also reduce the size of the output capacitor.

7.2.2 Output Capacitor Design

During a step-down load transient, the output capacitor absorbs the excess of inductor current. This results in voltage overshoot. The voltage overshoot for a given load transient is obtained in (7.31). The relation (7.31) is used to find the required capacitance for a given voltage overshoot. In a conventional buck converter, for a 10 A change in load current and a voltage overshoot less than $100mV$, it would require an output capacitance of $C_o = 601.5\mu F$. By using the proposed scheme, the voltage overshoot is obtained in (7.30) which also includes the delay in activation of Mode 3. In our system, the maximum delay between the occurrence of load transient and the activation of Mode 3 is around $1\mu s$. Hence the worst case value of capacitance to maintain the given voltage overshoot during such a transient is $180.7\mu F$ which amounts to 69.9% reduction in output capacitance.

7.2.3 Slew rate determines the fall time

The fall time of inductor current during a step-down transient can be decreased by having a high bandwidth and by having high slew rates. However at high bandwidth, the linear PI controllers get saturated and produce a duty ratio of either 0 or 1. Under such condition, the fall time is determined only by the slew rate

in the circuit. The slew rate is determined by $di_L/dt = v_L/L$. For step-down transients, the slew rate in conventional circuit is limited to $di_L/dt = -V_{out}/L$. On the other hand, in the proposed circuit the slew rate becomes $di_L/dt = -(V_{in}+V_{out})/L$. For example, in a buck converter with $V_{in} = 5V$, $L = 1.2\mu H$ and an output voltage of $1V$, the minimum fall time achievable for a 10A change in inductor current will be $12\mu s$. As opposed to that in the proposed circuit, the voltage across the inductor is $-(V_{in} + V_{out})$, thus for $V_{out} = 1V$, the fall time can be reduced to $2\mu s$.

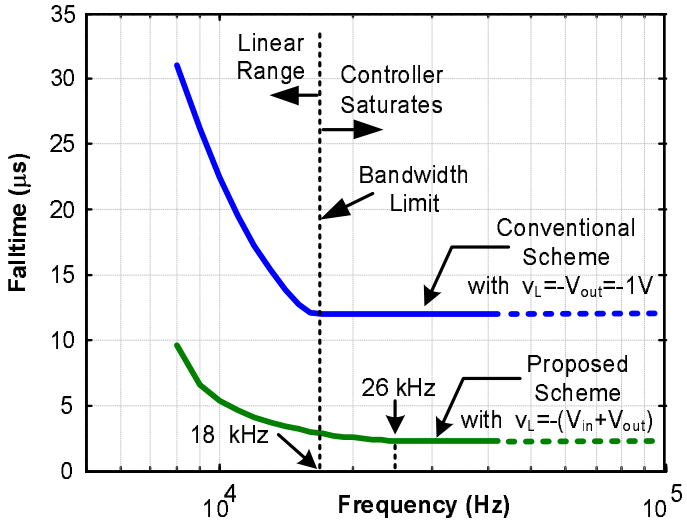

Figure 7.8: Reducing the fall time by increasing the slew rate of the inductor current

Thus, an increase in bandwidth can reduce fall time only in linear range where the controllers are not saturated. However, increasing the slew rate brings about a reduction in fall time under the maximum limits of circuit operation. In addition, high slew rates will produce faster fall times for the same bandwidth in the proposed method. This can be seen from Fig. 7.8. It shows the fall time for a buck converter having the following parameters: $V_{in} = 5V$, $L = 1.2\mu H$, $C_o = 408\mu F$, $r_c = 1m\Omega$ and $V_{out} = 1V$. The controllers are designed for a given

bandwidth and the fall time of the closed loop system is obtained for a 10A change in the reference current, which is greater than the condition established in (7.15). It is seen that in conventional scheme, increasing the bandwidth reduces the fall time in the linear range. However, beyond 18kHz the fall time is determined by the slew rate in the circuit. Whereas in the proposed scheme, the fall time is reduced by increasing the slew rate.

7.2.4 Power Loss Analysis

In a practical circuit, synchronous rectifiers will be used instead of the diodes, as shown in Fig. 7.9. For the circuit operation described earlier, the inductor current will flow through switch Q_2. Since Q_2 will be on during normal operation, the conduction loss in switch Q_2 can be obtained as [23]

$$P_{Q2} = [I_o^2 + \frac{\Delta I^2}{12}].R_{on,Q2} \tag{7.41}$$

where I_o is the output current, ΔI is the inductor current ripple, $R_{on,Q2}$ is the on-state resistance of switch Q_2.

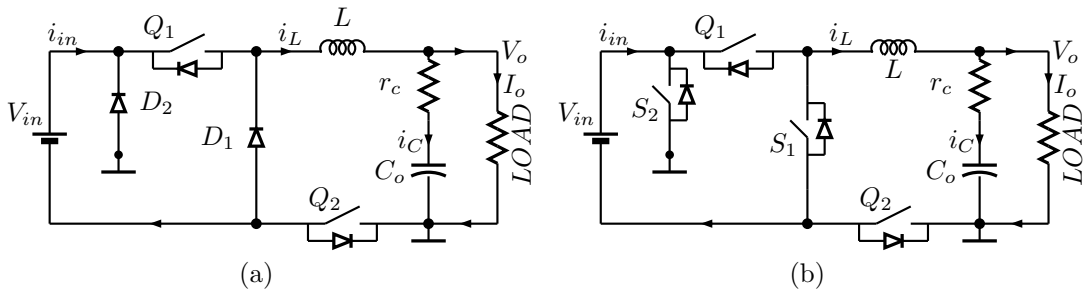

Figure 7.9: (a) The proposed scheme using diodes. (b) The diodes are replaced by synchronous rectifiers

For this analysis, the data of the commercially available MOSFETs can be

used which have the specifications suitable for such a low-voltage high-current application. Considering our specifications and the ratings, Infineon 25V n-channel MOSFET IPB03N03LA seems appropriate. Hence the on-resistance of the semiconductor switches is taken as $2.2m\Omega$. An interleaved buck converter is commonly used for high current VRMs, where the load current is shared by the paralleled modules. An inductor current of around 10A to 20A is common in an individual buck converter in such a topology. For a 5V-1V/10A buck converter having the inductor current ripple of 1A, the conduction loss incurred in the switch Q_2 will be 0.220W, which is 2.2% of the output power. Thus, in the proposed scheme, a 6x improvement in the response time is achieved at the expense of additional loss of 0.220W.

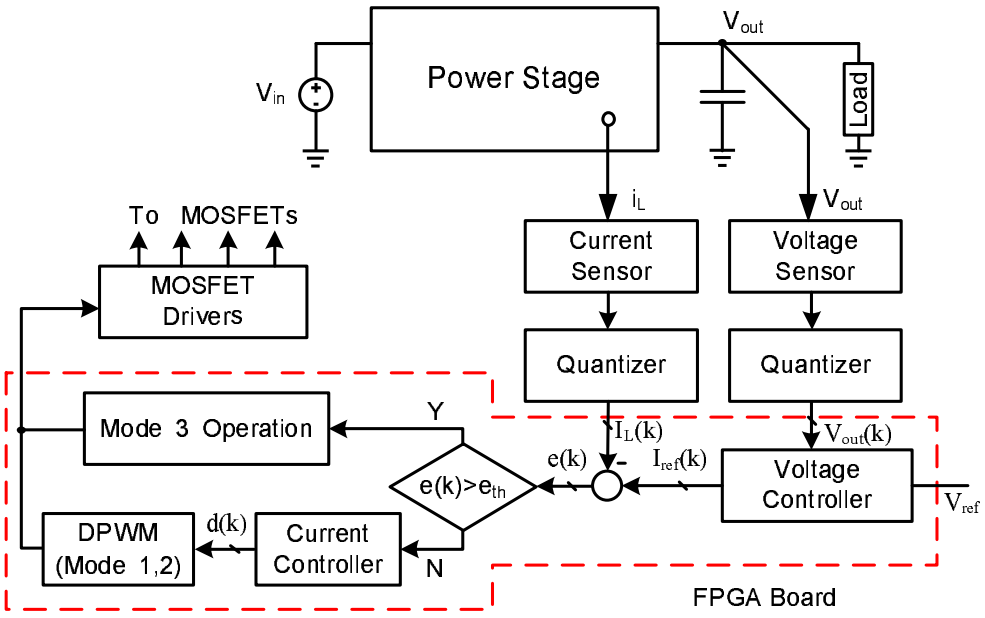

Figure 7.10: Schematic of digital controller design using FPGA

7.2.5 Implementation of Proposed Scheme

A digital controller was used to obtain the desired performance of the system. The digital controller performs various tasks including the voltage and current control, digital pulse width modulation and implementing the switching algorithm. The block schematic of a digital controller is shown in Fig. 7.10. The control algorithm requires the output voltage (V_{out}) and the inductor current (I_L). The sampled voltage is processed using the voltage controller to obtain the current reference (I_{ref}). The current error is obtained as ($e = I_{ref} - I_L$). The threshold current error (e_{th}) for switching to Mode 3 is obtained in (7.23). It depends on the slew rates ρ_1 and ρ_2, which are fixed for the given converter parameters. If the current error exceeds the threshold, the converter is switched to Mode 3 to increase the slew rate, else it continues in its normal operation.The scheme shown above is based on the current error. However, the scheme based on voltage error is also possible as described earlier.

7.3 Experimental Results

The performance of the proposed method was tested on a buck converter prototype with the following parameters: $V_{in} = 5\,V$, $V_{ref} = 1\,V$, $L = 1.2\mu H$, $C_o = 220\mu F + 4 \times 47\mu F$ (tantalum), $r_c = 1\,m\Omega$, $f_s = 1\,MHz$. Fig. 7.11 shows the experimental prototype which was used to demonstrate the proposed scheme. The full load current of the converter is limited to 16 A. Such currents are typical in the

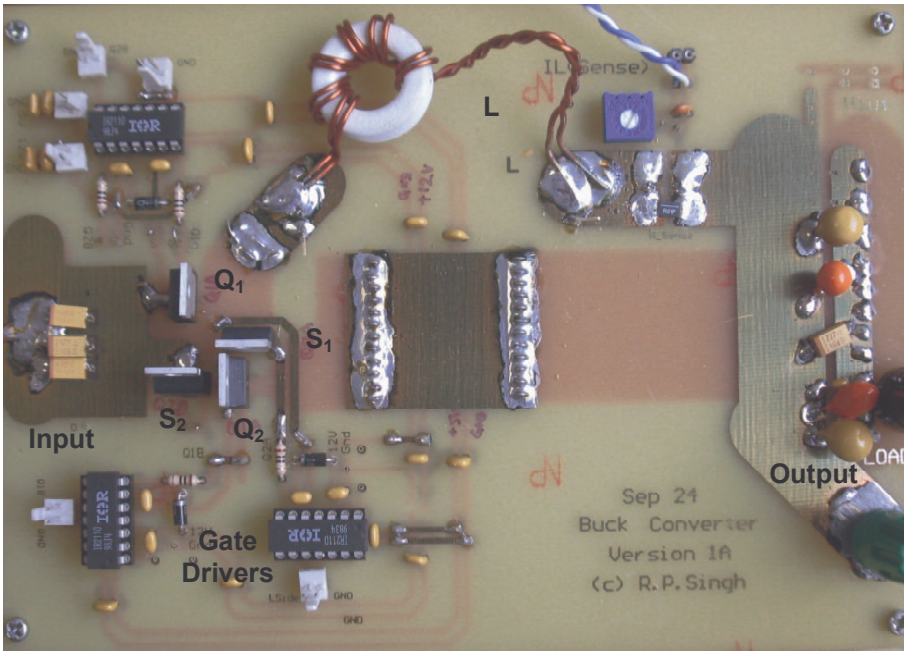

Figure 7.11: Experimental prototype of the buck converter used to demonstrate the proposed scheme.

individual converters of an interleaved buck converter topology, which is commonly used in VRMs. Since the main objective was to see the improvement in the slew rate of inductor current, it was demonstrated on a 1 V/16 A buck converter. A digital controller was used to verify the performance of the proposed scheme. The inductor current and the output voltage was sampled using an ADC. The ADC had 8-bit resolution ($N_{ADC} = 8$) and DPWM had 6-bit of hardware resolution. Thus 3-bit digital dither was introduced to increase the effective resolution of DPWM module to 6+3=9 bits ($N_{DPWM} = 9$). The controller was implemented on a Spartan-3 FPGA board from Xilinx operating at a clock frequency of 50MHz.

The dynamic response of inner current loop was studied to see the effect of step change in the reference current. Fig. 7.12 shows the response of the system when the converter was subjected to step change in the reference current from 16 A

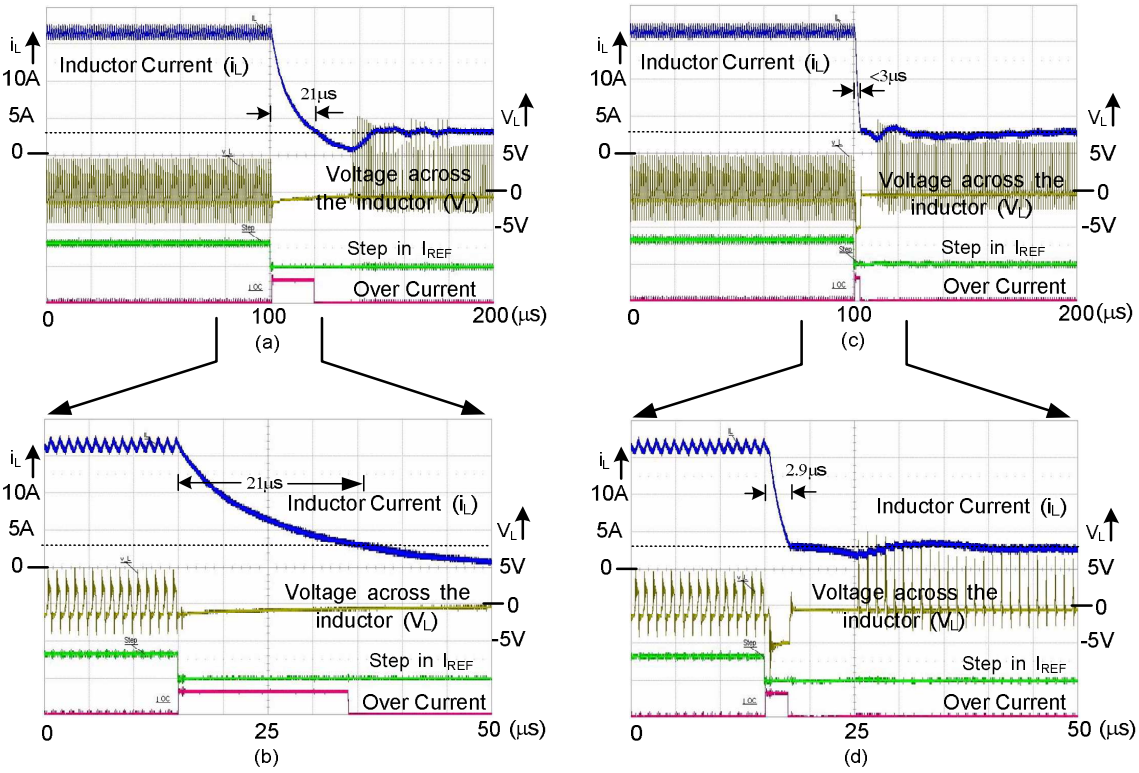

Figure 7.12: Experimental result showing the performance of the system with a step change in reference current. (a),(b) Conventional converter (c),(d) Proposed buck converter

to 3 A. Fig. 7.12 (a),(b) shows the response of current loop in a conventional buck converter, while Fig. 7.12 (c),(d) shows the response of the proposed scheme. Same PI controller was used in both these cases, except that an over current signal was used in Fig. 7.12 (c),(d) to apply a negative voltage across the inductor.

In conventional scheme, assuming the output voltage constant, the rate of change of inductor current will be $-V_{out}/L$, whereas in the proposed scheme it will be $(-V_{in} - V_{out})/L$. For $V_{in} = 5\,V$, $V_{ref} = 1\,V$, $L = 1.2\mu H$, one would expect 6x improvement in the response time. As seen from the experimental results, 7x improvement is obtained by using the proposed scheme. The fall time in conventional case is $21\mu s$, which is reduced to less than $3\mu s$ with the proposed scheme.

Since this result is based on inner current loop alone, the output voltage decreases following a decrease in inductor current. This results in the slew rate to change during the step down transient resulting in a larger fall times than predicted.

The system was also tested for load transients with a step-down change from 12 A-2.5 A. Fig. 7.13 shows the dynamic response of the converter. Cascaded voltage and current controllers were used to regulate the output voltage with its reference voltage set at 1 V. It shows the change in the output voltage during load transient. The load transients were generated by switching the load resistance and the voltage undershoot (ΔV_{out}) is obtained by using the AC coupling in a passive probe. Fig. 7.13 (a) is the conventional scheme, while Fig. 7.13 (b) is using the proposed scheme. Same controllers were used in both these cases, except that an additional over voltage signal was used in Fig. 7.13 (b) to apply negative voltage across the inductor. The overshoot in conventional scheme is 226 mV which is reduced to 161 mV using the proposed scheme. The transient time is also reduced from $235\mu s$ to $144\mu s$.

7.4 Summary

For a low conversion buck converter, a step-down load transient is more critical than the step-up load transient. During a step-down load transient, the maximum rate of decrease of inductor current depends upon the circuit inductance and the output voltage. As a result, the step-down transients last longer than then step-up transient. To this end, a new buck topology is presented which provides

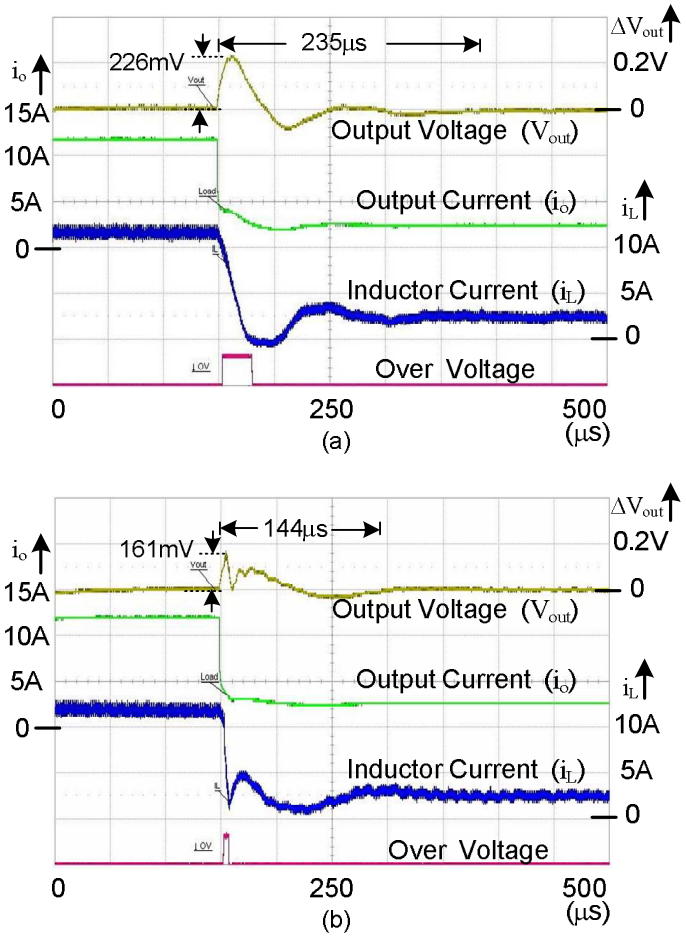

Figure 7.13: Experimental result showing the output voltage and inductor current during load transients in a buck converter with cascaded control loops (a) Response of the Conventional buck converter (b) Response of the proposed buck converter

improved step-down transient. From the experimental and simulation results, it is concluded that the proposed scheme is effective in improving the step-down transient response. Using the proposed scheme, it is possible to increase the slew rate of the inductor current, without having to reduce the inductance.

The proposed scheme improves the step-down transient response, thus reducing the voltage overshoots. In practical microprocessor applications, the voltage overshoots have long term reliability concerns whereas the voltage undershoots di-

rectly impacts the overall performance of the system. Thus it is also important to reduce the voltage undershoots during a step-up load transient. The next chapter proposes such a scheme.

Chapter 8

Improving the Step-Up Transient Response

8.1 Introduction

During a step-up change in load current, the charge supplied by output capacitor is more than the charge absorbed by the capacitor. This results in an undershoot of the output voltage. One way to reduce the undershoot is to increase the size of the output capacitance. This is undesirable as it increases the size of the voltage regulating module. Another way to reduce the voltage undershoot is to increase the inductor current faster. However, the rate of change of inductor current depends on the value of circuit inductance and the voltage across the inductance $|di_L/dt| = |v_L/L|$. The magnitude of the slew rate can be increased by increasing the magnitude of the voltage across the inductor or by reducing the inductance value.

In the past various methods have been proposed to improve the transient re-

sponse of the system. These methods rely on one or more of the following methods:

- Increasing the size of the output capacitor to reduce the voltage overshoot
- Reducing the circuit inductance so as to increase the rate of change of inductor current [10],[54],[55]
- Using feed-forward techniques to shape the load characteristics [56] - [58]
- Using non-linear control action during the load transients [59]- [64]
- Including an additional clamping circuit to limit the voltage overshoot [65], [66].

The above mentioned methods, either try to reduce the inductance value or incorporate non-linear control action during the load transients. However, the maximum possible slew rate is limited by the inductance value and the voltage across it. On the other hand, a non-linear control action would saturate the controller faster. It would change the speed of the response to disturbance and the best they can achieve is the maximum slew rate. They can't exceed the available slew rate. Secondly, the transient response will be governed by the instance at which the non-linear control action is applied and the duration it is applied. Thus, there are drawbacks in the previous schemes which limit their applications. These past approaches are unable to address the generic problem of high slew rates and meet the challenging requirements of high currents at high slew rates and tight voltage regulation.

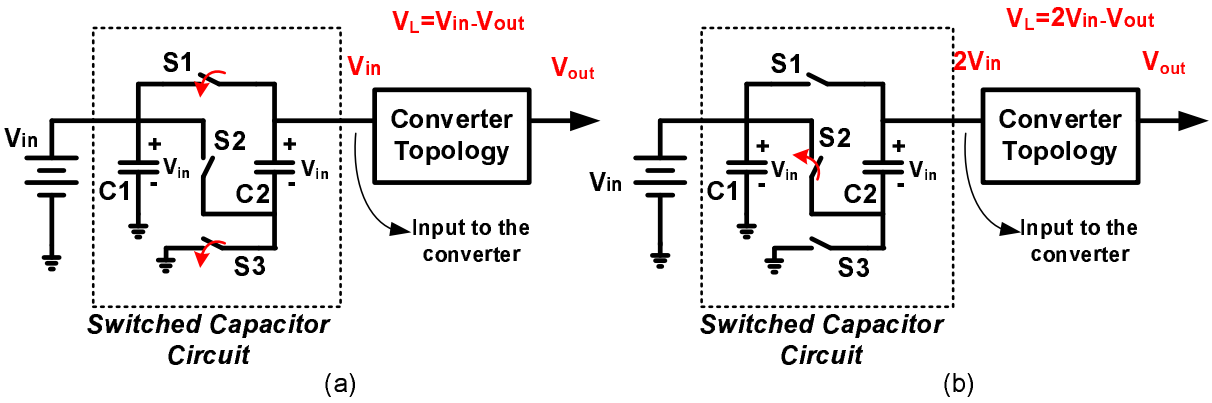

Figure 8.1: Working principle of the proposed scheme. The voltage across the inductor is changed by altering the input voltage

8.2 Proposed Scheme

The inductor current slew rate is given as $di_L/dt = v_L/L$, where v_L is the voltage across the inductor and L is the inductance. In a buck converter, when the high side MOSFET is turned on, the voltage across the inductor is $v_L = V_{in} - V_{out}$. Thus the slew rate depends on the circuit inductance, the input and the output voltage. Fig. 8.1 shows the working principle of the proposed scheme, which increases the slew rate by changing the voltage across the inductors. The voltage across the inductor can be changed by altering the input voltage. This is realized using a multilevel voltage generator, such as a switched capacitor circuit for obtaining different voltage levels. In Fig. 8.1(a) the voltage across the inductor is $v_L = V_{in} - V_{out}$, whereas in Fig. 8.1(b) it is increased to $v_L = 2V_{in} - V_{out}$. The Fig. shows only two levels of input voltage, it can be extended to obtain higher voltage levels.

Switched-capacitor based circuits have been used for voltage conversion [86]

- [89]. In this scheme, a switched-capacitor circuit is used to increase the input voltage to the converter. Increasing the input voltage increases the slew rate of inductor current without having to reduce the inductance value. The capacitor network provides the desired voltage level based on a switching algorithm, which uses knowledge of the circuit behavior. Moreover, since it has to work with a closed loop control, it has to have the correct logic interfaces with the outer loop. Thus, the proposed scheme includes the following: 1) an energy storage element, 2) a switching system, 3) an error based switching algorithm and 4) a feedback loop.

In the proposed scheme, the voltage across the inductor is changed during transient load. During transients, the fast rate of change of inductor current is achieved by increasing the voltage across the inductor. When the load transient is over and the fast rate of change is no longer required, the voltage across the inductor is changed to its original value. In doing so, the steady state ripple is kept to a minimum while providing fast dynamics during transients. This is realized using a switched capacitor circuit, which can generate multiples of an input voltage by appropriately controlling the switches associated with the circuit. The switches are ON only for a small duration. During startup, the switches are turned ON to charge the switched capacitor network. During transients, selective switches are turned ON again to increase the input voltage as required. By doing so, the slew rate of inductor current is increased which provides faster dynamic response to a load transient.

The proposed scheme achieves higher slew rates without having to reduce

Table 8.1: Slew rate comparison for different levels of input voltages in a buck converter

Inductance	$L = 1\mu H$		
Scheme Used	Normal scheme	Proposed Scheme	
Number of Voltage Levels	n=1	n=2	n=5
Slew Rate Achieved	$4\,\mathrm{A}/\mu s$	$9\,\mathrm{A}/\mu s$	$24\,\mathrm{A}/\mu s$
Equivalent Inductance*	1 μH	0.44 μH	0.166 μH
Inductance	$L = 100nH$		
Scheme Used	Normal scheme	Proposed Scheme	
Number of Voltage Levels	n=1	n=2	n=5
Slew Rate Achieved	$40\,\mathrm{A}/\mu s$	$90\,\mathrm{A}/\mu s$	$240\,\mathrm{A}/\mu s$
Equivalent Inductance*	100 nH	44.4 nH	16.6 nH

* Inductance required to obtain the slew rate using the normal scheme with constant input voltage

the inductance value. Table 8.1 shows the achievable slew rates for different levels of input voltage. Nominal input voltage is $V_{in} = 5\,V$ and the output voltage is assumed to be $V_{out} = 1\,V$. It is assumed, the input voltage can be increased by integral multiples as nV_{in}. In the conventional scheme, the input voltage is constant ($n = 1$). The table shows the slew rates for two different cases, one where 2 input levels are available ($n = 2$) and second where 5 input levels are available ($n = 5$). The table 8.1 gives the slew rates for a single buck converter. The slew rates can be increased further by paralleling operation, as in the case of an interleaved buck converter. It is concluded that for a single buck converter, it is possible to increase the slew rate of the inductor current without reducing the inductance. For example, with $100\,nH$ inductance a slew rate of $40\,\mathrm{A}/\mu s$ can be

achieved. By using $5V_{in}$, a slew rate of $240\,\mathrm{A}/\mu s$ can be achieved, which would have required an inductance of $16.6\,nH$ in the normal case. Such small inductors are difficult to fabricate. The high slew rates mentioned above are common in voltage regulator modules. For meeting such high slew rates, inductance value has to be reduced in nH range. However, smaller inductance will result in higher steady state ripple resulting in higher losses in the circuit. Thus, the proposed scheme can be used in such applications allowing us to increase the slew rate without reducing the inductance any further. The increased slew rate will result in faster transient response. This will also reduce the size of the output capacitor.

The proposed scheme, by increasing the slew rate of the inductor current in DC-to-DC converters achieves the following:

1. Reduced voltage undershoots during load transients in DC to DC converters.
2. Faster settling times of output voltage during transients.
3. Smaller output capacitor as it can provides reduced voltage undershoots.
4. Maintains a lower ripple current in the inductor of DC to DC converters.
5. It can be applied to any switched mode power converter for increasing the slew rate of inductor current.

In short, the proposed scheme is capable of providing fast dynamic performance during transients without significantly deteriorating the steady state behavior.

8.2.1 Working Principle

A sudden increase in the load current will cause an undershoot in the output voltage. To mitigate this undershoot effect, the average current supplied to the output capacitor of the DC to DC converter has to be increased to match the current supplied by the output capacitor to the load. This is achieved by changing the slew rate of the inductor current. For a constant value of inductance, the slew rate depends on the voltage across the inductor. The slew rate is increased by increasing the voltage across the inductor. The increased rate has to be sustained as long as the load is changing. Hence, to minimize the undershoot, the control scheme needs to sense the drop in output voltage. If the drop in the output voltage is above the permissible limit, the control algorithm is activated to change the voltage across the inductor, resulting in an appropriate slew rate that can reduce the time for the drop in the output voltage.

Since it is intended to increase the slew rate of inductor current, so the working of the error based control algorithm is explained using the current loop only. Later the idea can be extended to obtain the algorithm based on the output voltage.

Case I: Converters having current control loop: In DC-to-DC converters having an inner current loop and an outer voltage loop, the inductor current I_L is sensed for control purposes. I_L is compared with the desired reference current, I_{ref} and the current error is compensated. In the proposed scheme, an error based switching algorithm is used to decide the multiple of input voltage that needs to be

applied so as to minimize the current error. The scheme is shown in Fig. 8.2 which obtains the required input voltage (nV_{in}) to be applied to the converter. This can be explained with the following example.

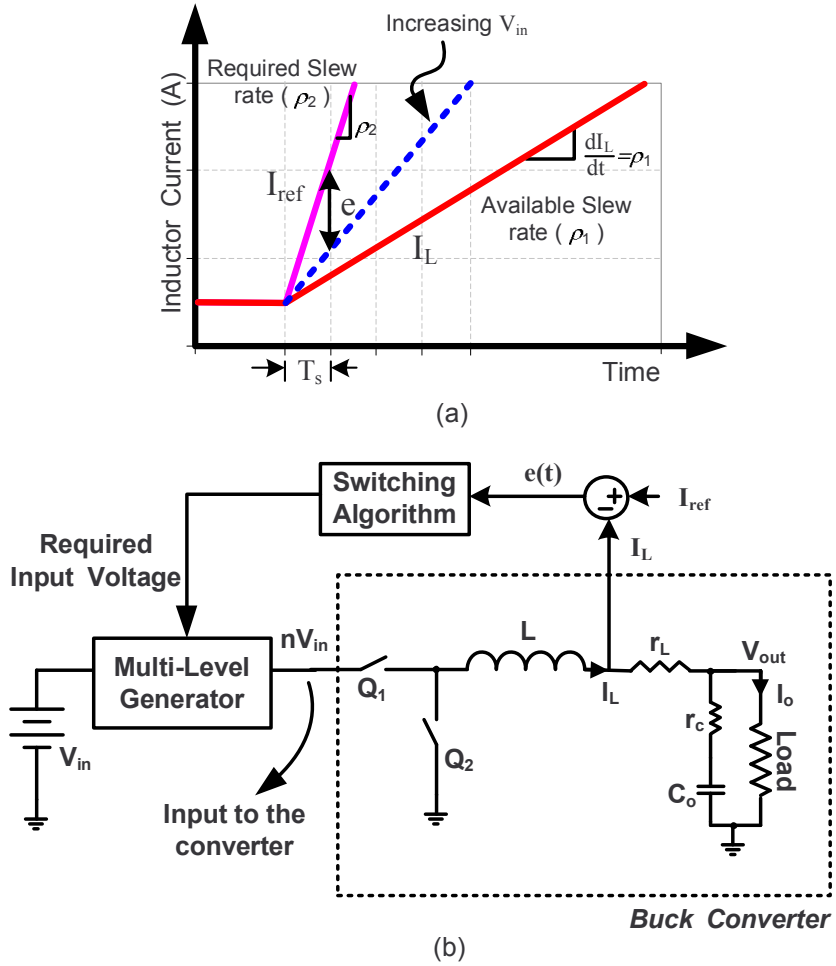

Figure 8.2: Difference in the slew rates - required and available. The slew rate is increased by increasing the input voltage.

Suppose there is a sudden change in reference current at time $t = 0$. The available slew rate due to circuit inductance is ρ_1 A/s while the required rate is ρ_2 A/s ($\rho_2 > \rho_1$), as shown in Fig. 8.2. By the end of one sampling instance, the current error will be $e = (\rho_2 - \rho_1).T_s$ where T_s is the sampling period. The idea here is to minimize the error by increasing the available slew rate ρ_1. The rate

ρ_1 is determined by the voltage across the inductance, where $\rho_1 = (V_{in} - V_{out})/L$. The rate ρ_1 can thus be increased by increasing the input voltage. It is assumed that the input voltage can be increased by integral multiples of V_{in}. The required input voltage $(n.V_{in})$ can be calculated such that the error e as shown in (8.1) is minimized.

$$e = (\rho_2 - \frac{nV_{in} - V_o}{L})T_s \tag{8.1}$$

For example, in a buck converter with $V_{in} = 5V$, $V_{out} = 1V$ and having an inductance of $1\mu H$, a slew rate of $4A/\mu s$ is available. Doubling the input voltage to $2V_{in}$ achieves a slew rate of $9A/\mu s$ and tripling the input voltage to $3V_{in}$ will correspondingly achieve $14A/\mu s$. Thus, if the error after a duration T_s is within the range $(9-4).T_s < e < (14-4).T_s$, then the input voltage is increased to $2V_{in}$. If the error is more than $(14-4)T_s$, the input voltage is increased to $3V_{in}$.

In general, it is desirous to find the input voltage such that the error is minimized. In other words, n is calculated such that the error lies within the range:

$$(\frac{nV_{in} - V_{out}}{L} - \frac{V_{in} - V_{out}}{L})T_s < e < (\frac{(n+1)V_{in} - V_{out}}{L} - \frac{V_{in} - V_{out}}{L})T_s \tag{8.2}$$

Or equivalently,

$$\frac{(n-1)V_{in}}{L}T_s < e < \frac{(n)V_{in}}{L}T_s \tag{8.3}$$

This gives the required input voltage $n.V_{in}$ which is to be obtained using the multi-level voltage generator. Once the required input voltage $n.V_{in}$ is known,

the feedback control of the proposed system will send relevant signal(s) to the multilevel voltage generator to generate the required input voltage $n.V_{in}$. Using (8.3), the minimum error required to apply a higher input voltage is obtained as

$$e_{th} > \frac{V_{in}}{L} T_s \tag{8.4}$$

Thus, if the error after a duration T_s is higher than e_{th}, a higher input voltage is applied else it continues in its normal operation.

In the example given in Fig. 8.3, the processing block takes in the inductor current I_L and the desired reference current I_{ref} as the input. The error in the inductor current is obtained as $e = I_{ref} - I_L$. Based on the error, the required input voltage is obtained. In this figure, there are 3 switches S1-S3 in the voltage summer, which helps in achieving twice the input voltage. This can be easily extended to generate higher multiples of the input voltage.

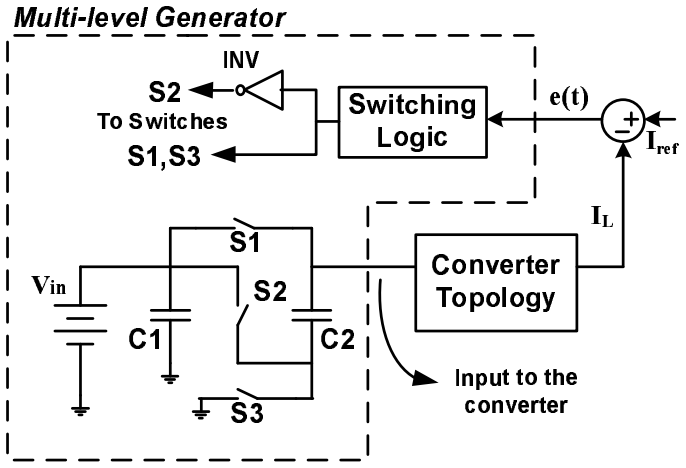

Figure 8.3: Multi-level generator applied to a power converter

In order to verify the current control with increased slew rate, let us consider the inner current loop of a buck converter. The converter parameters are $V_{in} = 5V$,

$C_o = 408\mu F$, $L = 1\mu H$ and $f_s = 1MHz$. The system was subjected to a 10A step change in reference current (I_{ref}) from 5A to 15A. Two different cases were simulated, one where only 2 input levels are available and second where 5 input levels are available. For a given controller, the performance was compared with the normal case where input voltage is kept constant. Same controller was used in all the three cases, except that an additional error based switching algorithm was used to switch the input voltage. It is seen from the simulation results in Fig. 8.4, the rise time and the settling time are improved by increasing the input voltage during transients.

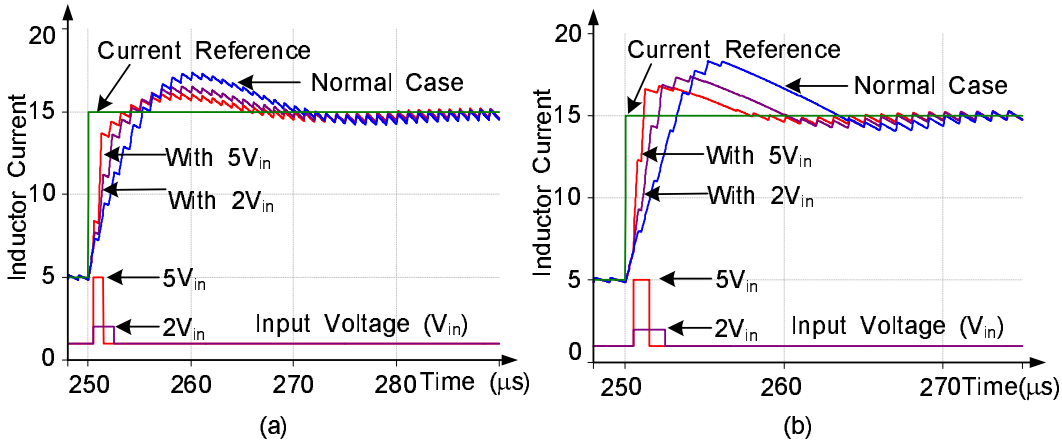

Figure 8.4: Simulation result showing the performance of the proposed scheme during a step change in current reference. (a) Closed loop bandwidth of 50kHz (b) Closed loop bandwidth of 100kHz

Case II: Switching Algorithm based on Hysteresis Control: A switching algorithm based on output voltage can be formulated, which increases the input to the converter, thus increasing the slew rate of inductor current and keeps the voltage undershoot within the permissible limits.

Consider a power converter having its output voltage regulated at V_{ref}. Dur-

ing a step-up load transient, a large amount of charge is removed from the capacitor in a very short time. This results in a drop in the output voltage. Two factors contribute to the voltage drop; voltage drop due to resistance $dV_R = i_c.r_c$, and voltage drop due to discharge of the capacitor $dV_Q = \Delta Q(t)/C_o$. Here, C_o is the output capacitor and r_c is the effective series resistance of the capacitor, as shown in Fig. 8.5.

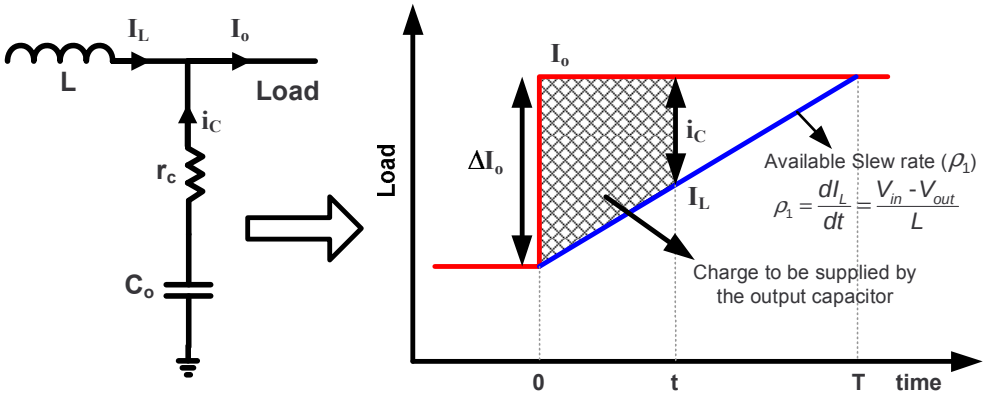

Figure 8.5: Discharging of output capacitor during sudden load change

A hysteresis based control algorithm is established which is used to switch the desired input voltage, so as to obtain an improved transient response. In such a method, two threshold voltages are defined below the nominal output voltage (V_{LH} and V_{LL}), with $V_{LH} > V_{LL}$. While the output voltage remains above the lower threshold (V_{LL}) converter is working with the nominal input voltage. If the step-up load transient is observed, the output voltage will start to decrease. Once the output voltage falls below the lower threshold (V_{LL}), the input voltage is increased and the converter starts to respond with increased slew rate, recharging the output capacitors. The input voltage is restored, once the output voltage increases above the upper threshold voltage (V_{LH}). The thresholds can be chosen smaller than the

limits imposed by the output voltage regulation specifications under load dynamics. This will ensure the voltage drop remains within the permissible limits. It can be verified by using the following example, in which the input voltage is switched after the output voltage has dropped to a certain level.

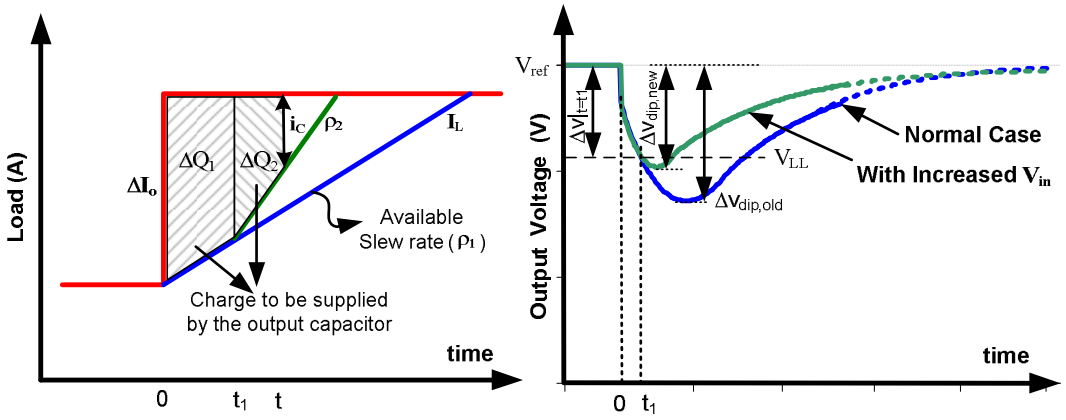

Figure 8.6: Typical waveforms during step change in the load. The input voltage is switched after time t_1

In this analysis, ρ_1 is the available slew rate and the higher slew rate (ρ_2) is applied at a time instance t_1 during the load transient, as shown in Fig. 8.6. At any any arbitrary instance t ($t > t_1$), the capacitor current can be evaluated as

$$i_c(t) = \Delta I_o - \rho_1 t_1 - \rho_2 (t - t_1) \tag{8.5}$$

The charge supplied by the capacitor during the interval $(0 - t_1)$ is given by

$$\Delta Q_1(t) = \frac{1}{2} t_1 (2\Delta I_o - \rho_1 t_1) \tag{8.6}$$

where ΔI_o is the change in the load current. The charge supplied by the capacitor during the interval $(t_1 - t)$ is given by

$$\Delta Q_2(t) = \Delta I_o (t - t_1) + (\rho_2 - \rho_1) t_1 t - (\rho_2 - \rho_1) t_1^2 + \frac{1}{2} \rho_2 (t_1^2 - t^2) \tag{8.7}$$

Thus, the total charge supplied by the output capacitor in time $(0-t)$ is $\Delta Q_1+\Delta Q_2$, which is obtained as

$$\Delta Q(t) = \Delta I_o t + (\rho_2 - \rho_1)t_1 t - \frac{1}{2}(\rho_2 - \rho_1)t_1^2 - \frac{1}{2}\rho_2 t^2 \tag{8.8}$$

The voltage drop during such a case can be expressed as,

$$\Delta v(t) = \frac{\Delta Q(t)}{C_o} + i_c(t).r_c$$

$$\Delta v(t) = \frac{\Delta I_o}{C_o}t + (\rho_2 - \rho_1)(\frac{t_1 t}{C_o} - \frac{1}{2}\frac{t_1^2}{C_o}) - \frac{\rho_2 t^2}{2C_o} + (\Delta I_o - \rho_1 t_1 - \rho_2(t - t_1))r_c \tag{8.9}$$

The undershoot will be maximum, when $\frac{\Delta v(t)}{dt} = 0$. The time instance can be obtained as

$$t = \frac{1}{\rho_2}(\Delta I_o + (\rho_2 - \rho_1)t_1 - \rho_2 r_c C_o) \tag{8.10}$$

Substituting this t in (8.9), undershoot is obtained as

$$\Delta v_{dip,new} = \frac{1}{2C_o\rho_2}[\Delta I_o^2 + C_o^2\rho_2^2 r_c^2 + 2\Delta I_o(\rho_2 - \rho_1)t_1 + \rho_1(\rho_1 - \rho_2)t_1^2] \tag{8.11}$$

The normal case voltage undershoot can be obtained by substituting $\rho_1 = \rho_2$ and $t_1 = 0$ in (8.11) as

$$\Delta v_{dip,old} = \frac{1}{2}(\frac{\Delta I_o^2}{\rho_1.C_o} + \rho_1.r_c^2.C_o) \tag{8.12}$$

For the proposed scheme to be effective, the voltage undershoot should decrease by increasing the slew rate,

$$\Delta v_{dip,old} - \Delta v_{dip,new} > 0 \tag{8.13}$$

$$\frac{\rho_2 - \rho_1}{2C_o\rho_1\rho_2}[-C_o^2 r_c^2\rho_1\rho_2 + (\Delta I_o - \rho_1 t_1)^2] > 0 \tag{8.14}$$

Since $\rho_2 > \rho_1$, the above expression is simplified as

$$[-C_o^2 r_c^2 \rho_1 \rho_2 + (\Delta I_o - \rho_1 t_1)^2] > 0 \tag{8.15}$$

This is a quadratic equation in t_1. This gives us the time instance before which the higher slew rate should be switched on so as to reduce the voltage undershoot.

$$t_1 < \frac{\Delta I_o}{\rho_1} \pm C_o r_c \sqrt{\frac{\rho_2}{\rho_1}} \tag{8.16}$$

The value with the plus sign corresponds to the time instance after the transient is over. Thus the value with the negative sign is retained.

$$t_1 < \frac{\Delta I_o}{\rho_1} - C_o r_c \sqrt{\frac{\rho_2}{\rho_1}} \tag{8.17}$$

Under the limiting case, the maximum value of time interval is obtained when t_1 approaches its upper limit. The voltage drop at this instance is obtained by substituting

$$t_1 = \frac{\Delta I_o}{\rho_1} - C_o r_c \sqrt{\frac{\rho_2}{\rho_1}} \tag{8.18}$$

in (8.9). The voltage drop is obtained as

$$\Delta v(t)|_{t=t_1} = \frac{\Delta I_o^2}{2C_o\rho_1} + C_o r_c^2 \sqrt{\rho_1 \rho_2} - C_o r_c^2 \rho_2 \tag{8.19}$$

Thus, for the given load change (ΔI_o), if the input voltage is increased before the voltage drops to the value given by (8.19), the undershoot can be reduced. This sets the limit on the threshold values (V_{LL}) for the hysteresis controller.

$$V_{LL} \geq V_{ref} - \Delta v(t)|_{t=t_1} \tag{8.20}$$

$$V_{LL} \geq V_{ref} - (\frac{\Delta I_o^2}{2C_o\rho_1} + C_o r_c^2 \sqrt{\rho_1 \rho_2} - C_o r_c^2 \rho_2) \tag{8.21}$$

If the output voltage drops below the threshold voltage (V_{LL}), the controller will switch the input voltage to a higher level, so as to reduce the voltage undershoot during the load transient. This also corresponds to a time instance defined by (8.18). Switching the input voltage to a higher level within time t_1, after the load transient occurs, will reduce the voltage undershoot. The input can be restored to its normal value once the output voltage increases above the upper threshold voltage (V_{LH}). The upper threshold is chosen close to the reference voltage such that $V_{LH} > V_{LL}$.

The above analysis was done for a buck converter having a voltage loop only. However, a cascaded voltage and current control loop is recommended for improved dynamic response. This is because the main component of the solution that brings about the improvement is based on increase in inductor current slew rate, hence an inner current loop is advantageous. The foregoing analysis based on voltage controlled converters is also applicable for converters operating with cascaded control loops. In order to verify the this, a buck converter with the following parameters was simulated: $V_{in} = 5V$, $C_o = 408\mu F$, $r_c = 3m\Omega$, $L = 1.2\mu H$, $f_{sw} = 1MHz$. The system was subjected to a 10A step change in load current (I_o) from 5A to 15A. The load transients were generated by switching the load resistance. The reference voltage was kept constant as $V_{ref} = 1V$. For the given converter parameters, the upper limit on the voltage drop given in (8.19) is obtained as 27.6mV. A voltage drop of 25mV was used to enable the switching algorithm ($V_{LL} = 0.975\,V$). For a given controller, the performance was compared with the normal case where in-

put voltage is kept constant. Two cases were simulated - one a converter having 2 levels of input voltage and second a converter having 5 levels of input voltage. Same controller was used in all the three cases, except that an additional error based switching algorithm was used to switch the input voltage. It is seen from the simulation results in Fig. 8.7(a), the voltage undershoot and the settling time are improved by increasing the input voltage during transients. This is also seen from Fig. 8.7(b) which shows the inductor current in the three cases. The increased input voltage helps in increasing the slew rate of the inductor current and hence results in faster transient response.

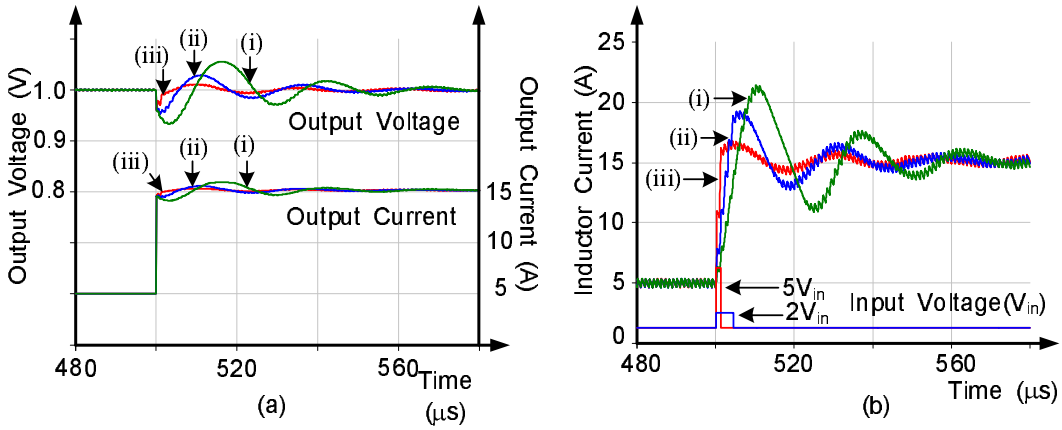

Figure 8.7: Simulation result showing the performance of the proposed scheme during a step change in the load current. (i) Normal case where input voltage is kept constant, (ii) Converter having 2 levels of input voltage and (iii) Converter having 5 levels of input voltage.

The simulation results shown above were to test the performance of the proposed scheme. It is concluded that it is possible to increase the slew rate of the inductor current without reducing the inductance. The increased slew rate results in faster transient response. This will also reduce the size of the output capacitor.

8.2.2 Switched Capacitor Circuit Design

Fig. 8.1 shows the use of a switched capacitor network to increase the input voltage to a converter. The input voltage to the converter is changed during load transient. When the load transient is over and the fast rate of change is no longer required, the voltage is reduced and eventually restored to its original value. Under such a load transient, the excess of inductor current is provided by the series connected capacitor $C2$ and $C1$, as shown in Fig. 8.1(b). Fig. 8.8 shows the excess charge supplied by the capacitor network during a step-up load transient. The charge supplied by the capacitors is obtained as

$$\Delta Q = \frac{1}{2}\Delta I_o^2(\frac{1}{\rho_1} - \frac{1}{\rho_2}) \tag{8.22}$$

where ρ_1 is the available slew rate due to circuit inductance, ρ_2 is the increased slew rate and ΔI_o is the change in the inductor current.

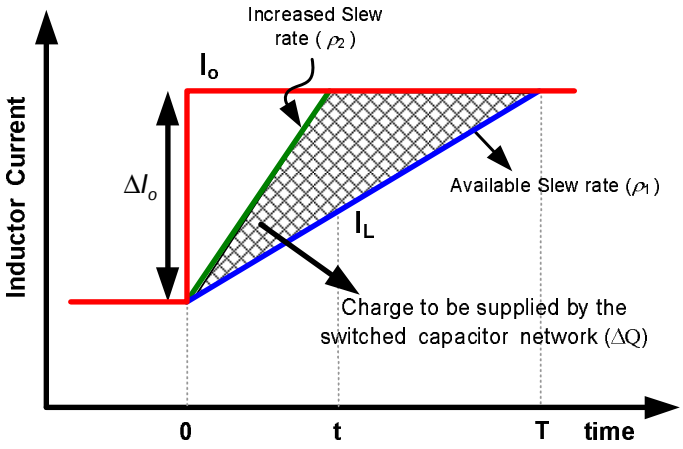

Figure 8.8: Charge supplied by the switched capacitor network to increase the slew rate of inductor current.

Fig. 8.1 shows the scheme for obtaining two input levels (with n=2). Capacitor $C1$ is connected across the input source and it can be considered as a part

of the input capacitor. As a result the voltage across capacitor $C1$ will be V_{in}. The excess of charge delivered will cause the voltage across $C2$ to decrease. In this work, the voltage drop across the capacitor is designed to be less than $\pm 1\%$ of its steady state value.

$$\Delta v_{C2} = \frac{\Delta Q}{C2} = \frac{1}{2}\frac{\Delta I_o^2}{C2}(\frac{1}{\rho_1} - \frac{1}{\rho_2}) \leq 1\% V_{in} \tag{8.23}$$

Thus, the required capacitance value of $C2$ can be calculated as

$$C2 \geq \frac{1}{2}\frac{\Delta I_o^2}{0.01 V_{in}}(\frac{1}{\rho_1} - \frac{1}{\rho_2}) \tag{8.24}$$

For the above mentioned parameters, $V_{in} = 5\,V$, $V_{out} = 1\,V$, $L = 1\,\mu H$, $n = 2$, the slew rates are $\rho_1 = 4\,A/\mu s$ and $\rho_2 = 9\,A/\mu s$. For a 10 A change in load current, the capacitance is obtained $C2 \geq 138.9\mu F$. If 5% variation is allowed in the capacitance voltage, the required capacitance will be $C2 \geq 27.7\mu F$.

The voltage drop for a given load transient is obtained in (8.12). The relation (8.12) is used to find the required capacitance for a given voltage undershoot. In a buck converter with its input voltage fixed, for a 10 A change in load current and a voltage undershoot less than $30mV$, it would require an output capacitance of $C_o = 857.9\mu F$. By using the proposed scheme where $2 \cdot V_{in}$ is available, it would require an output capacitance of $C_o = 381.3\mu F$ for obtaining the same voltage drop. But in order to implement this, $C2$ of $138.8\mu F$ is added, as obtained in eq. (8.24). Thus, in the proposed scheme the total capacitance required is $381.3\mu F + 138.8\mu F = 520.1\mu F$, which is 39.6% less than the capacitance required in the normal case ($C_o = 857.9\mu F$). If 5% variation is allowed in the capacitance voltage, the required capacitance will 52.3% less than the normal case.

The above mentioned algorithm formulations were designed for a buck converter so as to improve its transient response. These arguments can be extended to other topologies as well.

8.2.3 Slew rate determines the rise time

The rise time of inductor current during a step-up transient can be decreased by having a high bandwidth and by having high slew rates. However at high bandwidth, the linear PI controllers get saturated and produce a duty ratio of either 0 or 1. Under such condition, the rise time is determined only by the slew rate in the circuit. The slew rate is determined by $di_L/dt = v_L/L$. For step-up transients, the slew rate in a conventional buck converter circuit is limited to $di_L/dt = (V_{in} - V_{out})/L$. On the other hand, in the proposed circuit the slew rate becomes $di_L/dt = (nV_{in} - V_{out})/L$. For example, in a buck converter with $V_{in} = 5V$, $L = 1.0\mu H$ and an output voltage of $1.2V$, the minimum rise time achievable for a 10A change in inductor current will be $2.6\mu s$. As opposed to that in the proposed circuit, the voltage across the inductor is $(nV_{in} - V_{out})$, thus for $n = 2$, the rise time can be reduced to $1.2\mu s$ and for $n = 5$, it can be reduced to $0.42\mu s$.

Thus, an increase in bandwidth can reduce the rise time only in linear range where the controllers are not saturated. However, increasing the slew rate brings about a reduction in rise time under the maximum limits of circuit operation. In addition, high slew rates will produce faster rise times for the same bandwidth in the proposed method. This can be seen from Fig. 8.9. It shows the rise time for

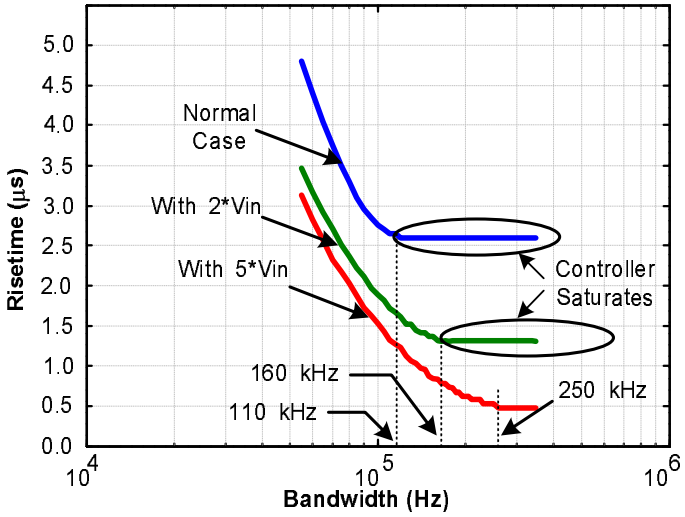

Figure 8.9: Reducing the rise time by increasing the slew rate of the inductor current

a buck converter with the given parameters. The controllers are designed for a given bandwidth and the rise time of the closed loop system is obtained for a 10A change in the reference current. It is seen that in conventional scheme, increasing the bandwidth reduces the rise time in the linear range. However, beyond 110kHz the rise time is determined by the slew rate in the circuit. Whereas in the proposed scheme, the rise time is reduced by increasing the slew rate.

8.2.4 Power Loss Analysis

The simplified schematic of the proposed scheme is shown in Fig. 8.10. It shows a buck converter using a switching algorithm based on current error ($e(t)$). The converter has a switched capacitor network at its input which can generate V_{in} and $2V_{in}$. Under the normal operating conditions, switch $S1$ and $S3$ will be on, such that the input to the converter is V_{in}. As a result the input current will flow through the switch $S1$. The current flowing through $S1$ will be same as that

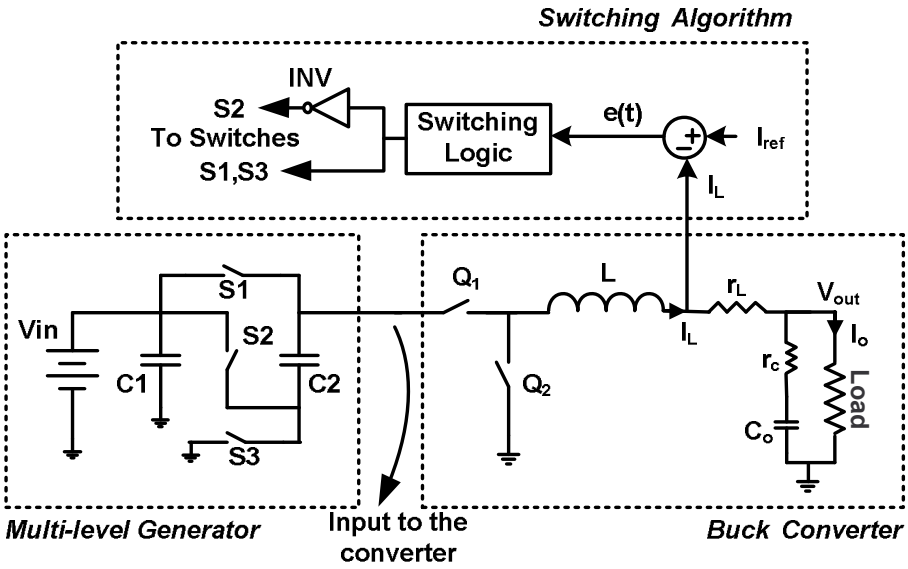

Figure 8.10: Block schematic of the proposed scheme showing a buck converter and a switched capacitor network at its input

in the control FET (Q_1) of the buck converter. Thus, the conduction loss in the switch $S1$ can be obtained as [23]

$$P_{S1} = [I_o^2 + \frac{\Delta I^2}{12}].R_{on,S1}.D \tag{8.25}$$

where I_o is the output current, ΔI is the inductor current ripple, $R_{on,S1}$ is the on-state resistance of switch S1 and D is the duty ratio of Q1. Only during transients, $S2$ will be turned on and $S1$,$S3$ will be switched off, such that the input to the converter is $2V_{in}$. Since this will be done only during the load transients and will last only for a few micro-seconds, the switching losses in the switched capacitor network can be neglected.

For this analysis, the data of the commercially available MOSFETs is used which have the specifications suitable for such a low-voltage high-current application. Considering our specifications and the ratings, Infineon 25V n-channel MOSFET IPB03N03LA seems appropriate. Hence the on-resistance of the semi-

conductor switches is taken as $2.2m\Omega$. The switching frequency of the converter is 1MHz. For 1V/20A buck converter having an input voltage of 5V and inductor current ripple of 1A, the conduction loss and switching loss in the Control FET are 0.216W and 0.802W respectively. Similarly for the Synchronous FET these loses are 0.864W and 0.797W respectively. In the proposed scheme, the conduction losses incurred in the switch S1 will be 0.216W, which is 0.90% of the output power. Although it results in increased conduction loss, the increase does not significantly affect the overall efficiency.

Furthermore, the on-resistance ($R_{ds,ON}$) of a MOSFET depends upon its breakdown voltage [90], [91] as:

$$R_{ds,ON} \propto V_{br}^{2\sim2.5} \tag{8.26}$$

As the proposed scheme intends to increase the input voltage during load transients, this will require MOSFETs of higher breakdown voltage to be used. Even in practice, the MOSFETs are usually chosen having breakdown voltages around 2-2.5 times the input voltage. This is to take into account the ringing produced during device turn-on and turn-off. In our application, where the input voltage is $V_{in} = 5V$, n-channel MOSFETs with breakdown voltage of 25V were chosen. n-channel Power MOSFETs with breakdown voltage less than 20V are difficult to find. Since 25V is well within the range, our prototype did not result in increased losses due to use of over rated devices.

8.2.5 Implementation of Proposed Scheme

A digital controller was used to obtain the desired performance of the system. The digital controller performs various tasks including the voltage and current control, digital pulse width modulation (DPWM) and implementing the switching algorithm. The block schematic of a digital controller is shown in Fig. 8.11.

The control algorithm requires the output voltage (V_{out}) and the inductor current (I_L) to be sensed. The sampled voltage is processed using the voltage controller to obtain the current reference (I_{ref}). The sensed inductor current is used to obtain the current error as $e = I_{ref} - I_L$. The threshold current error (e_{th}) for switching to a higher input voltage is obtained in (8.4). It depends on the inductance value L, V_{in} and T_s which are fixed for a given converter. If the current error exceeds the threshold, the converter is multilevel voltage generator is switched to apply a higher input voltage to the converter, else it continues in its normal operation. The scheme shown above is based on the current error. However, the scheme based on voltage error is also possible as described earlier.

8.3 Experimental Results

Fig. 7.11 shows the experimental prototype of a buck converter which was used to demonstrate the proposed scheme. The buck converter parameters are: $V_{in} = 5\,V$, $V_{ref} = 1\,V$, $L = 1.2\mu H$, $C_o = 220\mu F + 4 \times 47\mu F$ (tantalum), $r_c = 1\,m\Omega$, $f_s = 1\,MHz$. Although any number of input levels can be used to improve the

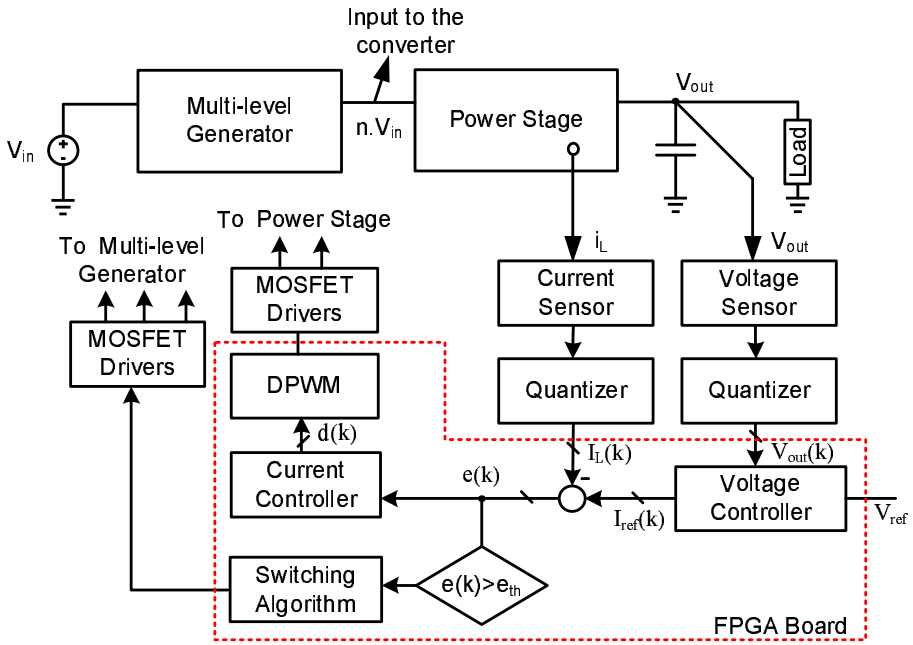

Figure 8.11: Block schematic of the proposed scheme

slew rate, only 2 input levels were used ($n = 1, 2$) to verify the functionality of the scheme. The storage capacitors in switched capacitor network comprises of $C_1 = C_2 = 2 \times 220\mu F + 100\mu F$. A digital controller was used to obtain the desired performance of the system. The controller was implemented on a Spartan-3 Field Programmable Gate Array (FPGA) by Xilinx.

The main component of the solution that brings about the improvement is based on increase in inductor current slew rate. In order to verify this, the dynamic response of inner current loop was studied to see the effect of step change in the reference current. Fig. 8.13 shows the response of the system when the converter was subjected to step change in the reference current from 5 A to 12.5 A. In Fig. 8.13(a) the input to the converter is kept constant, whereas in Fig. 8.13(b) input voltage is switched based on the switching algorithm. Same PI controller was used in both

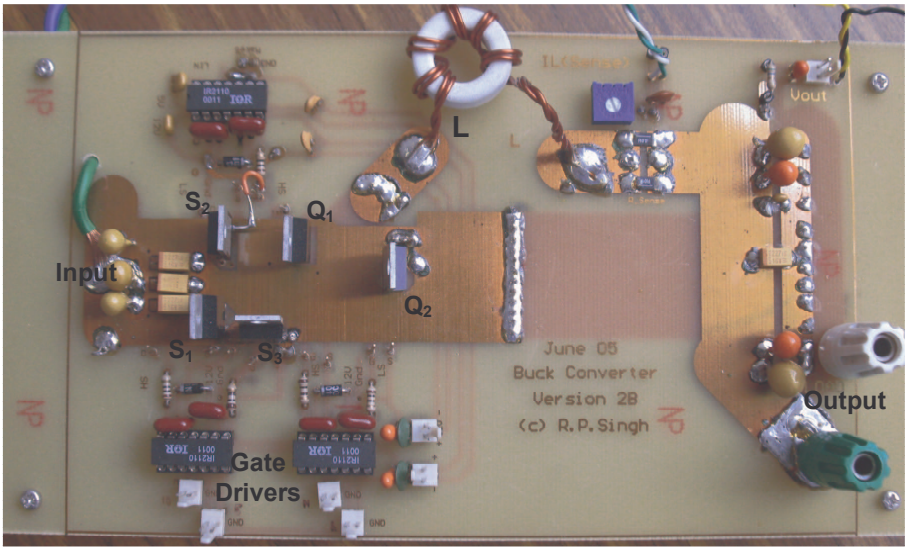

Figure 8.12: Experimental prototype of the buck converter used to demonstrate the proposed scheme.

these cases, except that an additional error based switching algorithm was used in Fig. 8.13(b). For large conversion ratios where $V_o \ll V_{in}$, the inductor current slew rate is approximately proportional to the input voltage. By applying $2V_{in}$, the slew rate can be doubled. As seen from the experimental results, 2x improvement is seen by using two levels of input voltage. The rise time in conventional case is $8\mu s$, which is reduced to $4\mu s$ with the proposed scheme. The settling time is also reduced from $60\mu s$ to $40\mu s$ as seen from the experimental results.

The results shown above were to test the performance of the inner current loop under load dynamics. In practice, a voltage control loop is used to regulate the output voltage. Thus, cascaded voltage and current controllers were used to regulate the output voltage with its reference voltage set at 1 V. The system was also tested for load transients with a step-up change from 2.5 A-12.5 A. Fig. 8.14 shows the dynamic response of the converter. It shows the change in the output

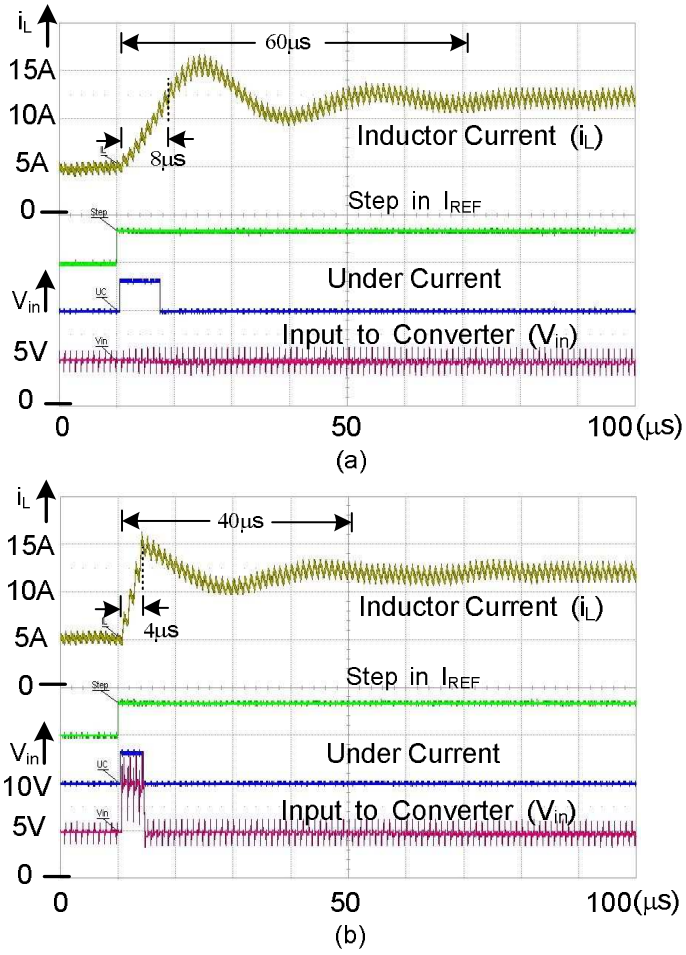

Figure 8.13: Experimental result showing the performance of the system with a step change in reference current. (a) Conventional converter with input voltage constant (b) Converter with switched input voltage

voltage during load transient. The load transients were generated by switching the load resistance and the voltage undershoot (ΔV_{out}) is obtained by using the AC coupling in a passive probe. Fig. 8.14(a) is the conventional scheme, while Fig. 8.14(b) is using the proposed scheme. Same controllers were used in both these cases, except that an additional error based switching algorithm was used in Fig. 8.14(b). The slew rate of the inductor current in conventional scheme was measured to be $0.70A/\mu s$, which is increased to $1.14A/\mu s$ with the proposed scheme. The undershoot in conventional scheme is 200 mV which is reduced to 120 mV using the

proposed scheme. The transient time is also reduced from $200\mu s$ to $100\mu s$.

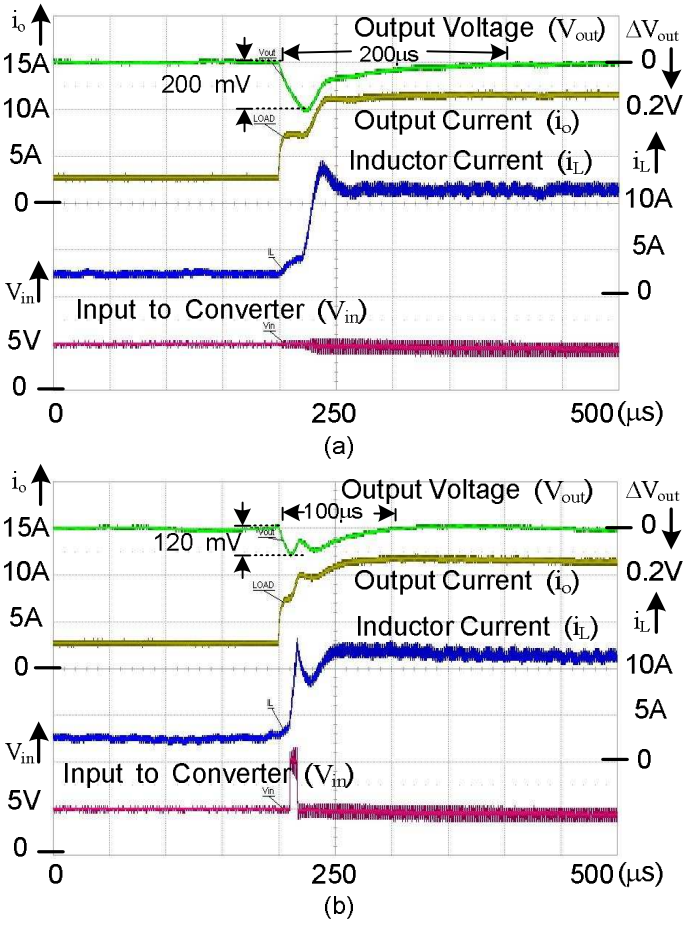

Figure 8.14: Experimental result showing the output voltage and inductor current during load transients in a buck converter with cascaded V+I control loops (a) Conventional converter with input voltage constant (b) Converter with switched input voltage

The results shown above were based on converter with an inductance of $1\mu H$. Smaller inductance value may be used to increase the slew rate. However, smaller inductance will result in higher inductor current ripple and hence increased power loss. Nonetheless, if a lower inductance is used for higher slew rates, the slew rate can be increased further by using the proposed scheme. In order to verify this, a two phase buck converter was built and tested. It uses the per phase inductance of $L_1 = L_2 = 100nH$ and an output capacitance of $540\mu F$. A cascaded voltage and

current controller is used to regulate the output voltage with its reference voltage set at 1 V. Fig. 8.15 shows the dynamic response of the converter during a step-up load transient from 10 A-24 A. The undershoot in conventional scheme is 225 mV which is reduced to 100 mV using the proposed scheme. The transient time is also reduced from 200μs to 140μs.

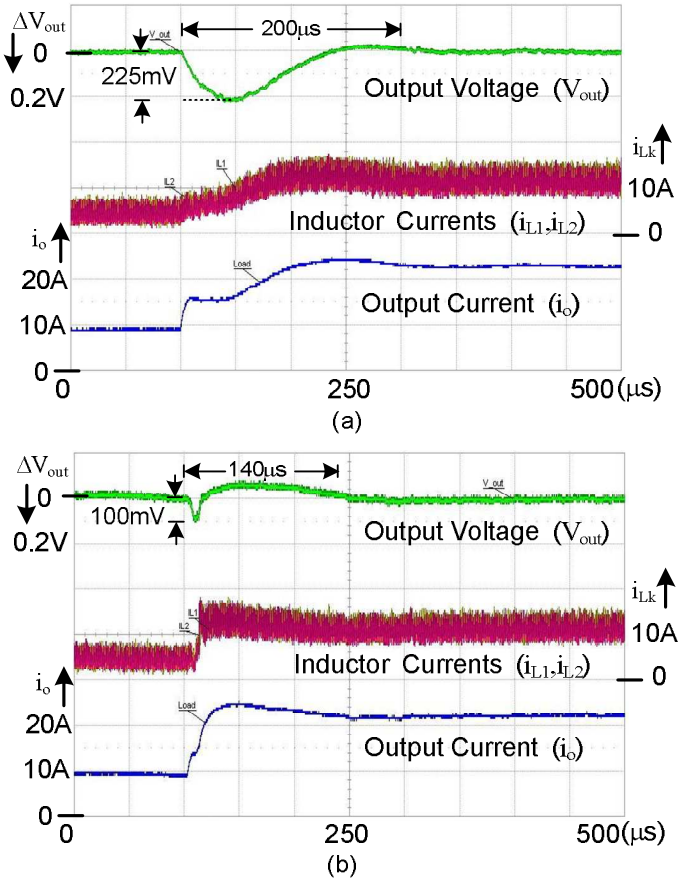

Figure 8.15: Experimental result showing the output voltage and inductor current during load transients in a buck converter with cascaded V+I control loops (a) Conventional converter with input voltage constant (b) Converter with switched input voltage

8.4 Summary

The transient response of any switched mode power supply gets limited by the component values. The rate of change of inductor current depends on the value of circuit inductance and the voltage across the inductance $di_L/dt = v_L/L$. This rate can be increased by increasing the voltage across the inductor or by reducing the inductance value. In this paper, a scheme is presented which proposes to increase the input voltage to increase the rate of change of inductor current. The scheme is experimentally verified on a single phase buck converter and a two phase buck converter operating at 1 MHz per phase.

From the experimental and simulation results, it is concluded that the proposed scheme is effective in improving the step-up transient response. Using the proposed scheme, it is possible to increase the slew rate of the inductor current, without having to reduce the inductance. This scheme gives another design freedom to optimally design the converters, resulting in lower inductor current ripple and requiring smaller output capacitor as compared to the conventional schemes.

Chapter 9

Conclusions

Voltage Regulator Modules (VRMs) provide power to the microprocessors. These modules are expected to deliver high currents upto 200A at low output voltages of around 1.2V. Due to high currents, it becomes essential to have multiphase topology where the synchronous buck converters are connected in parallel such that each phase leg carries only a fraction of the total output current. By operating the various converters in a phase-shifted manner, such a topology offers decreased magnitude of output voltage ripple. It also helps in increasing the frequency of the voltage ripple. Thus, the size of filter components can be reduced to a greater extent.

In an interleaved buck converter topology, it is important to share the currents equally among various phases. However, due to variation in the inductor values, differences of components, connections and layout results in unequal current distribution among phases. This causes uneven distribution of losses and reduces the overall efficiency. In order to achieve good current sharing among the

different phases, a current sensor needs to be added in a DC-DC converter. Due to N-paralleled converters in a multiphase topology, N-sensors are generally employed.

The microprocessors also exhibit load changes according to the change in computational load. These load transients affect the output voltage regulation. The voltage regulation can be improved by increasing the output capacitance but the transient response still gets limited by the rate of change of inductor current.

This thesis has investigated some of the existing problems related to the design and control of low voltage/ high current voltage regulator modules. The problems which are investigated in this thesis are broadly classified into following categories:

1. Digital control of Voltage Regulator Modules
2. Current sensing in low voltage/high current applications
3. Current sharing in multiphase interleaved converters
4. Circuit topology for improving the transient response

The proposed solutions are verified in simulation and experimentally demonstrated to show the functionality of the schemes. Following are the important features of the proposed solutions.

- Chapter 3 of this dissertation describes the development and analysis of high frequency digital controllers. The controller are designed in frequency domain

and when converted to discrete-time controllers, they result in lowering of phase due to presence of ZOH. They can be directly designed in discrete-time, but it requires complex mathematic manipulations. Thus, it is proposed to design the controllers in frequency domain and compensate for the reduction in phase due to presence of ZOH.

- Another limitation of the digital controllers is the time resolution of the DPWM output pulses. For a given switching frequency(f_s), the N-bit DPWM has to be clocked at $2^N f_s$. Thus, chapter 4 investigates a DPWM scheme which is aimed at improving the resolution without increasing the clock frequency. The proposed scheme provides 2-bit increase in the time resolution. Operating at a clock frequency of 50MHz, a resolution of $T_{CLK}/4$ (=5ns) is obtained which is 4-times improvement over the conventional scheme (=20ns).

- In chapter 5, a current sensing method is described which is based on Giant Magneto Resistive effect. It is based on sensing the magnetic field generated by the flow of current, as shown in Fig. 5.1. The change in magnetic field manifests itself in the change of resistance and the sensed output is obtained by sensing the voltage across the resistive network. The typical resistance offered by GMR is around $5\,k\Omega$. Thus, when operating at 12 V power supply, it will result in a power consumption of $0.0288\,W$. This power consumed is practically independent of the current to be measured and it does not rely on the knowledge of component value.

  Since, the sensor is based on magnetic field generated from the current car-

rying conductor, the sensed output depends upon the location of the sensor. Various sensor placement configurations are analyzed in the chapter and based on the theoretical framework, optimum location is derived for achieving the desired accuracy in current sensing.

- For sensing inductor currents in an multi-phase interleaved converters, N current sensors are required. Chapter 6 explores the possibility of a scheme which uses single current sensor. The proposed scheme presented in Fig. 6.1(b) uses single sensor to sense the inductor currents. The current sharing among individual phases is based on the difference in the average phase currents. The individual currents are sampled and stored. The duty ratio of individual phases is then updated so as to achieve current sharing. A simple low gain P-controller is used to achieve current sharing among individual phases. For a 4-phase 60A VRM, where each phase carries 15A of current, the control scheme will ensure 0.68% accuracy in current sharing, which is well within the 10% requirement of VRM 9.0 specifications. Moreover, the scheme is scalable in nature and can be applied to any number of phases.

- It is shown in chapter 7, for a low conversion ratio buck converter, a step-down transient will last longer than the step-up load transient. The transient response gets limited by the fundamental equation of rate of change of inductor current, as

$$\frac{di_L}{dt} = \frac{v_L}{L} \tag{9.1}$$

where v_L is the voltage across the inductor and L is the inductance. The

existing methods either try to reduce the inductance value or use a non-linear control to improve the transient response, but they can't exceed the available slew rate.

The step-down transient response is improved without having to reduce the inductance value. In a conventional buck converter, the maximum slew rate available during step-down load transient is

$$\frac{di_L}{dt} = \frac{-V_{out}}{L} \tag{9.2}$$

In the proposed scheme, the slew rate is increased to

$$\frac{di_L}{dt} = \frac{-(V_{in} + V_{out})}{L} \tag{9.3}$$

Thus, for a buck converter with an input of 5V and an output voltage of 1V, it will provide 6x improvement in the slew rate. The scheme works as a normal buck converter under steady-state, and increases the slew rate only during transients.

- Another circuit topology is presented in chapter 8, which improves the step-up transient response. The proposed scheme increases the voltage across the inductor during transient. In a conventional buck converter, the maximum slew rate available during step-up load transient is

$$\frac{di_L}{dt} = \frac{V_{in} - V_{out}}{L} \tag{9.4}$$

In the proposed scheme, input voltage is increased to nV_{in} which provides an increased slew rate of

$$\frac{di_L}{dt} = \frac{(nV_{in} - V_{out})}{L} \tag{9.5}$$

Thus, by increasing the input voltage to $2V_{in}$, a 2x improvement in the slew rate is expected. The proposed scheme as shown in shown in Fig. 8.3 is scalable in nature and can be extended to obtain higher slew rates. The increased slew rates improve the transient response of the converter. This also reduces the demand on the output capacitor size.

These schemes give another design freedom to optimally design the converters, resulting in lower inductor current ripple and requiring smaller output capacitor as compared to the conventional schemes.

Appendix A

Introduction

The chapters 7 and 8 use the voltage overshoot and voltage undershoot resulting due to a step-down or a step-up load transient. This appendix gives the detailed derivation of the expression given in the chapters. First, the expressions for voltage undershoot is obtained during a step-up load transient. The expression for voltage overshoot are obtained based on symmetry.

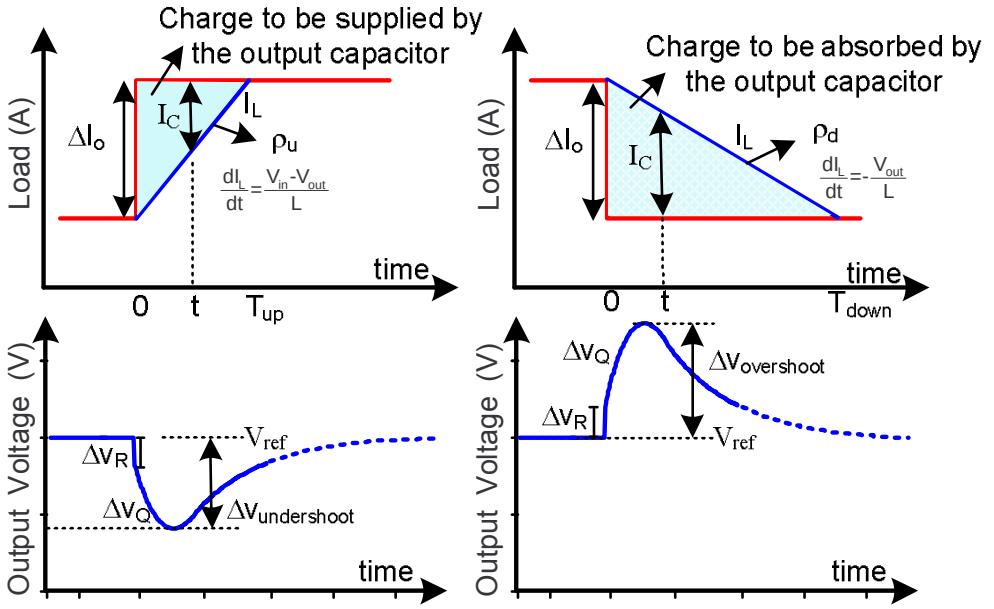

Figure A.1: Charging and discharging of the output capacitor during sudden change in load current

Derivation of voltage undershoot

If there is a step-up change in load current at $t = 0$, then at any any arbitrary instance t, the capacitor current can be evaluated. This is the current flowing out of capacitor so as to provide the excess of load current.

$$i_c(t) = \Delta I_o - \rho_u t \tag{A.6}$$

where ΔI_o is the change in the load current and ρ_u is the slew rate of the inductor current, as shown in Fig. A.1. The charge supplied by the capacitor during the interval $(0 - t)$ is given by

$$\Delta Q(t) = \frac{1}{2} t(2\Delta I_o - \rho_u t) \tag{A.7}$$

Two factors determine the output voltage at the given instance; voltage drop due to resistance $\Delta V_R = i_c(t).r_c$, and voltage drop due to discharge of the capacitor $\Delta V_Q = \Delta Q(t)/C_o$. Thus, the output voltage in this case is given as

$$V_{out}(t) = V_{ref} - (\frac{\Delta Q(t)}{C_o} + i_c(t).r_c) \tag{A.8}$$

Alternatively, the voltage drop during step-up change in load current can be expressed as,

$$\begin{aligned} \Delta v(t) &= \frac{\Delta Q(t)}{C_o} + i_c(t).r_c \\ \Delta v(t) &= \frac{\Delta I_o}{C_o} t - \frac{1}{2}\frac{\rho_u}{C_o} t^2 + \Delta I_o.r_c - \rho_u.r_c.t \end{aligned} \tag{A.9}$$

The undershoot will be maximum, when $\frac{\Delta v(t)}{dt} = 0$ or for $t = T - r_c.C_o$, where T is the time taken by the inductor current to attain the new value $T = \frac{\Delta I_o}{\rho_u}$. It is

known that $t > 0$, thus we obtain $T > r_c.C_o$, the RC time constant of the output capacitor. Substituting this t in (A.9),

$$\Delta v_{undershoot} = \frac{\Delta I_o}{C_o} T - \frac{\rho_u.T^2}{2.C_o} + \frac{\rho_u.r_c^2.C_o}{2} \tag{A.10}$$

Eliminating T from this relation,

$$\Delta v_{undershoot} = \frac{1}{2}(\frac{\Delta I_o^2}{\rho_u.C_o} + \rho_u.r_c^2.C_o) \tag{A.11}$$

For $t = 0$ (or $T = r_c.C_o$), the undershoot is obtained as

$$\Delta v_{undershoot} = \Delta I_o.r_c \tag{A.12}$$

Similarly, the overshoot for the same change in load current can be obtained as

$$\Delta v_{overshoot} = \frac{1}{2}(\frac{\Delta I_o^2}{\rho_d.C_o} + \rho_d.r_c^2.C_o) \tag{A.13}$$

where ρ_{DN} is the rate of change of inductor current during the step-down load transient. For $t = 0$ (or $T = r_c.C_o$), the overshoot is obtained as

$$\Delta v_{overshoot} = \Delta I_o.r_c \tag{A.14}$$

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List of Publications

Journals

1. R.P. Singh and A.M. Khambadkone, "Giant Magneto Resistive (GMR) effect based Current Sensing Technique for Low Voltage/High Current Voltage Regulator Modules", *IEEE Transactions on Power Electronics*, vol 23, no. 2, March 2008, pp 915-925.

2. R.P. Singh and A.M. Khambadkone, "A Buck Derived Topology with Improved Step-down Transient Performance" *IEEE Transactions on Power Electronics*, vol 23, no. 6, November 2008, pp 2855-2866.

3. R.P. Singh and A.M. Khambadkone, "Current Sensing in N-paralleled Converters using Single Current Sensor", *IEEE Transactions on Industry Applications*, vol 46, no. 3, June 2010, pp 1212-1219.

Conferences

1. R.P. Singh, A.M. Khambadkone, G.S. Samudra, and Y.C. Liang, "Optimal power converter topology for powering future microprocessor demands," in *IEEE Industrial Electronics Conference (IECON'04) proceedings*, Nov 2004, vol. 1, pp. 530-535

2. R.P. Singh, A.M. Khambadkone, G.S. Samudra, and Y.C. Liang, "Modelling, analysis and design of cascaded forward and interleaved converter for powering future microprocessors," in *IEEE Power Electronics and Drive Systems (PEDS'05) proceedings*, Nov 2005, vol 1, pp 430-435.

3. R.P. Singh, A.M. Khambadkone, G.S. Samudra, and Y.C. Liang, "An FPGA based Digital Control Design for high-frequency DC-DC Converters", in *IEEE Power Electronics Specialists Conference (PESC'06) proceedings*, June 2006, pp. 1-6.

4. R.P. Singh and A.M. Khambadkone, "Giant Magneto Resistive (GMR) effect based Current Sensing Technique for DC/DC Converters", in *IEEE Industrial Electronics Conference (IECON'07) proceedings*, Nov 2007, pp. 1420-1425.

5. R.P. Singh and A.M. Khambadkone, "Input Voltage Switched DC-DC Converter with Improved Transient Performance", in *IEEE Applied Power Electronics Conference and Exposition* (APEC), Feb 2008, pp. 824-830.

6. R.P. Singh and A.M. Khambadkone, "Current Sensing in N-paralleled Converters using Single Current Sensor", in *IEEE Industrial Applications Society (IAS) Annual Meeting*, Oct 2008, pp. 1-7.

Invention Disclosure

1. A.M. Khambadkone and R.P. Singh, "Multi-level Voltage Switched high slew rate generator for switched mode power converters", Provisional Patent Application at USPTO vide application No. 60/829,156 dated 10 Dec, 2006.