INVESTIGATION OF HIGH-*K* GATE DIELECTRICS FOR ADVANCED CMOS APPLICATION

YU XIONG FEI

NATIONAL UNIVERSITY OF SINGAPORE

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YU XIONG FEI

(B. Eng., ZheJiang University)

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In order to maintain historical trends of improved device performance, the continued aggressive scaling of CMOS devices for leading-edge technology is driving the conventional SiO_2/SiON gate dielectrics to their physical limits due to excessive gate leakage current and reliability concerns. High dielectric constant (*k*) gate dielectrics, as the replacement of the SiO_2/SiON, have been extensively investigated in the past few years, because of their potential for reducing gate leakage current while keeping the equivalent oxide thickness (*EOT*) thin. Timely implementation of the high-*k* gate dielectrics will involve dealing with four major challenging issues, including (1) thermal stability, (2) mobility degradation, (3) charge trapping induced threshold voltage (V_{th}) instability, and (4) Fermi level pinning induced high V_{th}.

The main purpose of this thesis was to overcome the four major challenges, and also attempt to integrate the high-*k* gate dielectrics to conventional self-aligned poly-Si gate and advanced metal gate process.

In **Chapter 2**, we proposed a novel HfTaO gate dielectric with high dielectric constant, sufficient high crystallization temperature, good thermal stability, strong boron penetration immunity, low interface state density (D_{it}), high mobility, and excellent V_{th} instability. These suggest that the HfTaO is a very promising candidate as an alternative gate dielectric for future CMOS application.

A novel HfTaON/SiO_2 gate stack, which consists of a HfTaON film with *k* value of 23 and a 10-Å SiO_2 interfacial layer, was proposed for low standby power application in **Chapter 3**. This gate stack provided much lower gate leakage current against SiO_2, good interface properties and thermal stability, excellent transistor characteristics, superior carrier mobility and negligible V_{th} instability. These excellent properties observed in the HfTaON/SiO_2 may be mainly attributed to the good physical and electrical characteristics in HfTaO, and the insertion of SiO_2 interfacial layer.

In **Chapter 4**, the experimental results demonstrated that the gate dopant penetration may remarkably affect the gate leakage current in n^+ poly-Si/HfO_2 devices. Based on the experimental results and physical analyses, a hypothesis of generation of dopant-related defects at grain boundaries in crystallized HfO_2 film was proposed. These imply that the phosphorus or arsenic penetration is also significant concern for poly-Si/HfO_2 devices.

In **Chapter 5**, we have demonstrated that the unacceptably high V_{th} induced by the Fermi Level pinning at poly-Si/high-*k* interface was effectively suppressed by inserting a poly-SiGe gate electrode. The acceptable V_{th} of 0.3 V for nMOS and -0.49 V for pMOS was successfully achieved in the poly-Si/poly-SiGe/Al_2O_3/HfO_2 device. This finding could make a great breakthrough for integration of high-*k* gate dielectric into conventional poly-Si gate process.

Finally, the impacts of nitrogen on charge trapping induced V_{th} instability in high-*k* gate dielectric with metal and poly-Si gates have been extensively studied. A novel phenomenon, which the incorporated nitrogen in high-*k* film played opposite role in charge trapping induced V_{th} instability between the devices with metal and poly-Si gate, was demonstrated in **Chapter 6**.

Overall, the results of all studies presented in this thesis may contribute to a good understanding of material properties, electrical characteristics and reliability in high-*k* gate dielectrics for advanced CMOS application. Several approaches presented in this thesis can be used to effectively solve the major challenges for implementation of the high-*k* gate dielectrics.

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Chapter 1

Introduction

1.1 Introduction of Device Scaling

1.1.1 Evolution of ULSI Technology

It has been sixty years since the invention of the bipolar transistor (1947), around fifty years since the invention of the integrated circuit (IC) technology (1958), and more than forty-five years since the invention of the metal oxide semiconductor field effect transistor (MOSFET, 1960). During the period, there has been an unprecedented growth of the semiconductor industry, which has made an enormous impact on the way people work and live. At the beginning of the semiconductor industry, the semiconductor market was broadly based on bipolar transistors. In the last three decades, the most prominent growth area of the semiconductor industry has been in silicon IC technology, which has evolved from small-scale integration (SSI), to medium-scale integration (MSI), to large-scale integration (LSI), to very-large-scale integration (VLSI), and finally to ultra-large-scale integration (ULSI). By far, the ULSI technology has infiltrated practically every aspect of our daily life.

The most important ULSI device is, of course, the MOSFET because of its advantages in device miniaturization, low power dissipation, and high yield compared to all other semiconductor devices. The MOSFET also serves as a basic component for many key device building blocks, including the complementary metal oxide semiconductor (CMOS), the dynamic random access memory (DRAM), and the static

random access memory (SRAM). Therefore, the ULSI device is almost synonymous with the silicon MOSFET.

The sustained growth in ULSI technology is driven by the continuous scaling of MOSFET to ever smaller dimensions. The benefits of miniaturization, such as higher packing densities, higher circuit speeds, and lower power consumption, have been the key factors in the evolutionary progress leading to today's computers and communication systems that offer superior performance, dramatically reduced cost per function, and much reduced physical size, in comparison with their predecessors.

The primary motivation for continuous scaling of MOSFET is to increase transistors per chip, which may reduce cost effectively. During the most of time in semiconductor industry's history, the behavior of scaling of MOSFET has followed the well-known Moore's law, which predicts that the number of transistors per chip would be double every 18 months [1]. At this rate, the transistors per chip have been increased from 10^3 in the year of 1972 to more than 10^9 of today's leading-edge technology. In the meantime, cost per function has decreased at an average rate of ~ 25-30% per year per function [2]. In the past fifty years, cost per function has gone down by 100 million times. By 2000, the price per bit is less than 0.1 milli-cents for a 64-megabit memory chip. Similar price reductions are expected for logic ICs. Additional benefits from device miniaturization include improvement of device speed and reduction of power consumption. Higher speed leads to expanded IC functional throughput rates, so that future ICs can perform data processing, numerical computation, and signal conditioning at 100 and higher gigabit-per-second rates [3]. Reduced power consumption results in lowering of the energy required for each switching operation. The required energy, called the power-delay product, has decreased by six orders of magnitude since 1960 [4].

1.1.2 Device Scaling Approaches

ULSI technology evolution in the past few decades has followed the path of device scaling for achieving "*smaller, cheaper and faster*" circuit. MOSFET scaling

has been propelled by the rapid advancement of lithographic techniques for delineating channel length of 1 μm and below. However, the MOSFET with channel length below 1 μm normally results in short-channel effect. For a short-channel MOSFET, the depletion charge controlled by the gate is reduced because part of the depletion charge under the gate is controlled by the source-drain junctions [5]. The most undesirable short-channel effect is a reduction in the gate threshold voltage (V_{th}) at which the device turns on, especially at high drain voltages. Full realization of benefits of new high-resolution lithographic techniques therefore requires the suitable device scaling rules that can keep short-channel effects under control at very small dimensions.

There are various sets of device scaling rules aimed at reducing the device size while keeping device function, such as constant-field scaling, constant-voltage scaling, and the generalized scaling rules [6-8].

In constant-field scaling, it was proposed that one can keep short-channel effects under control by scaling down the vertical dimensions (gate insulator thickness, junction depth, etc.) along with the horizontal dimensions, while also proportionally decreasing the applied voltages and increasing the substrate doping concentration (decreasing the depletion width). The principle of constant-field scaling is to scale the device voltages and the device dimensions (both horizontal and vertical) by a same factor, so that the electric field remains unchanged. However, the requirement to reduce the applied voltages by the same factor as the reduction of physical dimension in constant-field scaling is difficult to implement since the threshold voltage and sub-threshold slope are not easily controlled for scaling [9]. If the scaling of threshold voltage is lower than other factors, the drive current would be reduced. Thus, a constant-voltage scaling rule was proposed to address this issue, where the voltages remain unchanged while device dimensions are scaled. However, constant-voltage scaling will result in an extremely high electric field, which causes unacceptable leakage current, power consumption, and dielectric breakdown as well as hot-carrier effects [9]. To avoid the extreme cases of constant-field and constant-voltage scaling, a generalized scaling approach has been developed, where the electric field is scaled

by a factor of κ while the device dimensions are scaled by a factor of α [7]. In **Table 1.1**, the technology scaling rules for constant-field, constant-voltage and generalized scaling schemes are compared.

Table 1.1: The technology scaling rules for constant-field, constant-voltage and generalized scaling [6-8]

MOSFET Device and Circuit parameters	Multiplicative Factor for MOSFET's		
	Constant E	Constant V	Generalized
Device Dimensions (T_{ox}, L_g, W, X_j)	$1/\alpha$	$1/\alpha$	$1/\alpha$
Voltage (V)	$1/\alpha$	1	κ/α
Electric Field (E)	1	α	κ
Capacitance ($C = \varepsilon A/t$)	$1/\alpha$	$1/\alpha$	$1/\alpha$
Inversion Layer Charge Density (Q_i)	1	α	κ
Circuit Delay Time ($\tau \sim CV/I$)	$1/\alpha$	$1/\alpha^2$	$1/\kappa\alpha$
Power per Circuit ($P \sim VI$)	$1/\alpha^2$	α	κ^3/α^2
Power-Delay Product per Circuit ($P\tau$)	$1/\alpha^3$	$1/\alpha$	κ^2/α^3
Circuit Density ($\propto 1/A$)	α^2	α^2	α^2
Power Density (P/A)	1	α^3	κ^3

(α: Dimensional Scaling Factor; κ: Voltage Scaling Factor)

In reality, the CMOS technology evolution has followed mixed steps of constant-field, constant-voltage and generalized scaling, as shown in **Table 1.2**.

Table 1.2: CMOS ULSI technology generations [9]

Feature Size (μm)	Power-Supply Voltage (V)	Gate Oxide Thickness (Å)	Oxide Field (MV/cm)
2	5	350	1.4
1.2	5	250	2.0
0.8	5	180	2.8
0.5	3.3	120	2.8
0.35	3.3	100	3.3
0.25	2.5	70	3.6

1.1.3 Scaling and Improved Performance

The industry's demand for greater integrated circuit functionality and performance at lower cost requires an increased circuit density, which has translated into a higher density of transistors on a chip. This rapid shrinking of the transistor feature size has forced the channel length and gate dielectric thickness to also decrease rapidly.

From a ULSI circuit performance point of view, an improved performance requires to reduce the dynamic response (i.e., charging and discharging) of the MOSFET, associated with a decrease of switching time τ. The switching time is limited by the fall time required to discharge the load capacitance or the rise time required to charge the load capacitance by the drive current. In the case where parasitic capacitances are ignored, an increase in the device drive current I_D results in a decrease in the switching time or improvement on the performance. The drive current can be written as:

$$I_D = \frac{W}{L}\mu C_{inv}\left(V_G - V_{th}\right)V_D, (V_D << V_G) \quad (1\text{-}1)$$

Where W is the width of the transistor channel, L is the channel length, μ is the channel carrier mobility (assumed constant here), C_{inv} is the capacitance density

associated with the gate dielectric when the underlying channel is in the inverted state, V_G and V_D are the voltages applied to the transistor gate and drain, respectively, and the threshold voltage is given by V_{th}. Initially, I_D increases linearly with V_D and then eventually saturates to a maximum when $V_{D,\,sat} = V_G - V_{th}$ to yield, then

$$I_{D,sat} = \frac{W}{L}\mu C_{inv}\frac{(V_G - V_{th})^2}{2} \tag{1-2}$$

The term $(V_G - V_{th})$ is limited in range due to reliability and room temperature operation constraints, since too large a V_G would create an undesirable, high electric field across the oxide. Furthermore, V_{th} cannot easily be reduced below about 200 mV. This is due to the non-scalability of the sub-threshold slope, and also reducing V_{th} below 200 mV would lead to high off-state leakage current I_{off}. Typical specification temperature (≤100 ºC) could therefore cause statistical fluctuations in thermal energy, which would adversely affect the desired the V_{th} value. Thus, even in this simplified approximation, a reduction in the cannel length or an increase in the gate capacitance will result in an increased $I_{D,\,sat}$.

If one ignores quantum mechanical and depletion effects from a Si substrate and gate, the gate capacitance is given by

$$C = \frac{k\varepsilon_0 A}{t_{eq}} \tag{1-3}$$

Where k is the dielectric constant (also referred to as the relative permittivity) of the gate dielectric, ε_0 is the permittivity of free space (=8.85×10^{-3} fF/μm), A is the area of the gate, and t_{eq} is the equivalent oxide thickness (*EOT*) of the gate dielectric. It is easily seen then that a decrease in the t_{eq} of dielectric results in an increase in the gate capacitance.

The term *EOT* represents the theoretical thickness of SiO_2 that would be required to achieve the same capacitance density as the dielectric. For example, if the capacitor dielectric is SiO_2, the *EOT* is the thickness of the SiO_2. If the capacitor dielectric is an alternative dielectric, such as high-k gate dielectric, the physical thickness of the high-k ($t_{high\text{-}k}$) employed to the *EOT* can be obtained form the expression:

$$\frac{EOT}{k_{SiO_2}} = \frac{t_{high-k}}{k_{high-k}} \tag{1-4}$$

or simply,

$$t_{high-k} = \frac{k_{high-k}}{k_{SiO_2}} EOT = \frac{k_{high-k}}{3.9} EOT \tag{1-5}$$

Thus, a dielectric with a relative permittivity of 19.5 affords a physical thickness of 50 Å to obtain *EOT* of 10 Å.

Consequently, the improved performance associated with the increase in the device drive current I_D of MOSFET requires rapid shrinking of MOSFET channel length, which has forced the gate dielectric thickness (*EOT*) to also decrease rapidly. The channel length of MOSFET has been scaled from 25 μm of the first MOSFET to the ~0.035 μm (65 nm node) of today's leading-edge technology, while the gate dielectric thickness has been decreased from 1000 Å to around 12 Å, respectively. Scaling theory in conjunction with observation of past industry trends (e.g., Moore's law) has led to the creation of so-called roadmaps for semiconductor technology. The most public and widely agreed roadmap is the International Technology Roadmap for Semiconductors (ITRS) [2]. The ITRS is a statement of the historical trend as well as a projection of the future device needs and performances as perceived at the time of formulation of the roadmap. Based on the prediction of ITRS, the MOSFET with channel length of 10 nm and equivalent oxide thickness of 5 Å would be required for mass production by the year of 2015.

1.2 Scaling Limits for Conventional Gate Dielectrics

1.2.1 Limitations of SiO_2 as the Gate Dielectric for Advanced CMOS Devices

For the past several decades, the robust SiO_2 has always been used as the gate dielectric in CMOS technology. The use of amorphous, thermally grown SiO_2 as the gate dielectric offers several key advantages in CMOS processing, including a stable (thermodynamically and electrically), high-quality interface as well as superior

electrical isolation properties. In modern CMOS processing, the defect charge densities are of the order of $10^{10}/cm^2$, and midgap interface state densities are ~ $10^{10}/cm^2$-eV in SiO_2/Si system. Moreover, hard breakdown fields (electric fields that result in a catastrophic increase in the resultant tunneling current through the dielectric) of 15 MV/cm are routinely obtained in SiO_2 regardless of the transistor dimensions. In addition, minimal low-frequency *C-V* hysterisis and frequency dispersion (< 10 mV), minimal dielectric charging and interface degradation, and the sufficiently high carrier mobility (both electrons and holes) can be usually obtained for the MOSFET with SiO_2/Si system [2]. The apparent robust natures of SiO_2, coupled with industry's acquired knowledge of oxide process control, have been the key elements enabling the continuous scaling of SiO_2 gate dielectric for the past several decades in CMOS technology.

Despite this remarkable contribution of SiO_2, the continuous scaling of SiO_2 gate dielectric thickness is problematic in advanced CMOS technology. The major concerns are the unacceptably high leakage current under the required operating voltages, boron penetration from poly-Si gate, and reliability issue.

Since the dominant transport mechanism through gate dielectric less than ~30 Å thick is by direct tunneling of electrons or holes, the leakage current increases exponentially with decreasing thickness due to the fundamental quantum mechanical rules [10]. For example, a typical leakage current density for 15-Å-thick SiO_2 at 1 V is ~1 A/cm^2. As the SiO_2 thickness approaches 10 Å, the leakage current density increases to 100 A/cm^2 at the same operating voltage. Based on experimental evidence of the excellent electrical properties of such ultra-thin SiO_2 film, it has been demonstrated that MOSFET with SiO_2 thickness as thin as 13-15 Å continue to operate satisfactorily, however, the high leakage currents of 1-10 A/cm^2 (at V_{DD}) were measured for such devices [11]. The rapid increase in leakage current with the decrease of the SiO_2 thickness would lead to heat dissipation and power consumption problems regarding to the operation of CMOS devices, especially with respect to standby power dissipation. As first reported by Timp et al. [12], scaling of CMOS structures with SiO_2 gate dielectric thinner than about 10-12 Å results in no further

gains in transistor drive current, which is due to the high gate leakage induced inversion charge loss.

In addition to leakage current increasing with scaled SiO_2 thickness, the issue of boron penetration through the SiO_2 gate dielectric is a significant concern. The large gradient between the heavily doped poly-Si gate electrode, the undoped SiO_2 and lightly doped Si channel causes boron to diffuse rapidly through a ultrathin SiO_2 upon thermal annealing, which results in a higher concentration of boron in the channel region. A change in channel doping then causes a shift in V_{th}, which clearly alters the intended device properties in an unacceptable way [13].

An equally important issue regarding ultrathin SiO_2 gate dielectric is oxide reliability [14-16]. The carriers traveling through the SiO_2 gate dielectric may generate defects including carrier traps and interface states, and upon accumulation to the critical density, the dielectrics properties will be degraded. The accumulated charge to breakdown values (Q_{bd}) for the dielectrics decreases with the thickness [14]. Recently, it was predicted that oxide films thinner than ~ 14 Å may not achieve the reliability required by the industry roadmap [15].

1.2.2 SiON and Si_xN_y/SiO_2 Gate Dielectrics

The concerns regarding high leakage currents, boron penetration and reliability of ultra-thin SiO_2 have led to materials structures such as SiON and Si_3N_4/SiO_2 stacks for near-term gate dielectric alternatives. These structures provide a slightly higher k value than SiO_2 (pure Si_3N_4 has k ~7) for reduced leakage due to the physically thicker film (as discussed in **Eq. 1-5**), reduced boron penetration and better reliability characteristics [17-19]. Furthermore, small amounts of N (~0.1%) at or near the Si channel interface have been shown to control channel hot-electron degradation effects [20]. However, large amounts of N near this interface degrade device performance, which is attributed to several factors, including excess charge induced by N atoms, a high defect density arising from bonding constraints imposed at the interface [21] (which causes increased channel carrier scattering), and from the defect

levels in the Si-nitride layer which reside near the valence band of Si. In contrast, improved electrical properties have been obtained by using Si_xN_y/SiO_2 gate stack, which can achieve *EOT*<17 Å with a leakage current of ~10^{-3} A/cm^2 at 1.0 V bias [22].

Table 1.3: ITRS 2005 for the scaling of dielectric thickness with year [2]

Year	***2005***	***2006***	***2007***	***2008***	***2009***
Physical gate length for high performance (nm)	32	28	25	22	20
Physical gate length for low operating power (nm)	45	37	32	28	25
Physical gate length for low standby power (nm)	65	53	45	37	32
EOT for high performance (Å)	12	11	11	9	7.5
EOT for low operating power (Å)	14	13	12	11	10
EOT for low standby power (Å)	21	20	19	16	15
Maximum gate leakage for high performance (A/cm^2)	188	536	800	909	1100
Maximum gate leakage for low operating power (A/cm^2)	33	41	78	89	100
Maximum gate leakage for low standby power (A/cm^2)	0.015	0.019	0.022	0.027	0.031

(*The dark color indicates no solution until now*)

This leakage current is ~ 100 times lower than that for a pure SiO_2 layer of the same *EOT*, and the leakage reduction arises from both a physically thicker film and from a small amount of N at the channel interface.

Despite these encouraging results from a variety deposition and growth techniques, scaling with the SiON and Si_xN_y/SiO_2 appears to be limited to *EOT*~13 Å [23]. Below this, the effects of gate leakage, reliability or electron channel mobility degradation will most likely prevent further improvements in devices performance. On the other hand, it has been suggested that 7 Å is the physical thickness limit for SiO_2 or SiON, because the SiO_x sub-oxide region at any oxide/Si interface is ~3.5 Å thick and there are two oxide/Si interfaces at the channel and the gate electrode. According to the most recent ITRS, the current gate dielectrics (SiO_2 or SiON) may only represent current two years near-term solutions for scaling the CMOS transistors [2], as shown in **Table 1.3**.

Consequently, the aggressive shrinking of gate dielectric thickness is driving the conventional SiO_2 or SiON gate dielectrics to its physical limit and the research groups in semiconductor industry have difficulty in searching any alternative gate dielectric candidates for future CMOS application.

1.3 Alternative High-*k* Gate Dielectrics

As discussed in the previous sections, the continued aggressive scaling of the MOSFETs for leading-edge technology in order to maintain historical trends of improved device performance is driving the conventional SiO_2 or SiON gate dielectric to its physical limits. The major concerns are unacceptably high leakage current under the required operating voltages, boron penetration from poly-Si gate, and reliability issue. As an alternative to SiO_2 or SiON gate dielectric, many works have been done on high-*k* materials as a means to provide a substantially thicker (physical thickness) dielectric for reduced leakage current and improved gate capacitance. According to ITRS 2005, the high-*k* gate dielectric will be required beginning in ~2008 [2]. Therefore, the timely implementation of high-*k* gate dielectric is an imperative task

for maintaining the historical trend of device scaling in semiconductor industry.

1.3.1 Selection Guidelines for High-*k* Gate Dielectrics

All of the alternative high-*k* materials must meet a set of criteria to perform as successful gate dielectric. In this section, a systematic consideration of the required properties of the appropriate high-*k* materials will be discussed for the gate dielectric application.

1.3.1.1 Permittivity and Barrier Height

Selection of a gate dielectric with a higher permittivity than that of SiO_2 is clearly essential. As mentioned in **Eq. 1-5**, a dielectric with a higher permittivity may provide a physically thicker film to achieve the same *EOT*, and also reduce the leakage current. However, it has been reported that the materials with ultra-high permittivity may cause fringing field induced barrier lowering effect when it was used as the gate dielectric [24]. The fringing field induced barrier lowering effect predicts that the device off-state leakage current increases as *k* value increases (become significant especially when $k>25$), which is due to that a significant fringing field at the edge of a high-*k* dielectric could lower the barrier for carriers transport into the drain, and hence seriously degrade the on/off characteristics of the device. It is therefore appropriate to find a dielectric with moderate *k* value for advanced CMOS gate dielectric application. A single dielectric layer with k~12–25 could allow a physical dielectric thickness of 35–50 Å to obtain the *EOT* values required for 65 nm CMOS and beyond.

In order to obtain low leakage currents, it is desirable to find a gate dielectric that has large band offset for both electrons and holes (ΔE_C and ΔE_V). Since the ΔE_C and ΔE_V of many potential gate dielectrics have not been reported, the closest, most readily attainable indicator of band offset is the band gap (E_G) of the dielectric. A large E_G generally corresponds to a large ΔE_C, but the band structure for some materials has a large valence band offset ΔE_V which constitutes most of the band gap

of the dielectric (such as Ta_2O_5).

The E_G of the dielectric should be balanced against its dielectric constant. The dielectric constant generally increases with increasing atomic number for a given cation in a metal oxide. However, the band gap energy of the metal oxides tends to decrease with increasing atomic number [25]. **Table 1.4** shows the comparison of relevant properties for various gate dielectric materials. As can be seen, the band gap energy tends to decrease with increasing the dielectric constant.

Table 1.4 Comparison of relevant properties for various gate dielectric materials. [26-28]

Dielectric	Dielectric constant (K)	Gap energy (eV)	Electron barrier to Si (eV)
SiO_2	3.9	8.8	3.15
Si_3N_4	7.8	5.1	2.1
Al_2O_3	8 – 11.5	~6.5 - 8.7	~2.4 - 2.8
ZrO_2	22 – 28	~5.5 - 5.8	~1.4 - 2
$ZrSiO_4$	10 – 12	~6	1.5
HfO_2	25 – 30	~5.25 - 5.7	~1.5 - 1.9
$HfSiO_4$	~10	~6	1.5
TiO_2	~80	3.5	~1.2
Ta_2O_5	~25	~5	~0.3 - 0.5

1.3.1.2 Thermodynamic Stability on Si and Film Morphology

For all thin gate dielectrics, the interface with Si plays a key role, and in most cases is the dominant factor in determining the overall electrical properties. Most of the high-*k* metal oxide systems investigated so far have unstable interfaces with Si:

the reaction between high-*k* materials and Si during high thermal budget process to form an undesirable interfacial layer. Moreover, the thickness of the undesirable interfacial layer normally increases with the temperature of process, which results in an increased *EOT* (thermodynamic instability). The thermal stability of gate oxides on silicon in the subsequent high-temperature process also has a critical impact on the Si/dielectric interface quality. One high-temperature process from a typical CMOS process flow is the source/drain (S/D) activation annealing (up to 1000°C), for which the gate dielectric must undergo such high-temperature annealing. Also, the increase in the interfacial layer due to the high-temperature annealing is desirable to be suppressed.

On the other hand, most of alternative gate dielectrics are polycrystalline films after the subsequent high-temperature process, but it is desirable to select a material which remains in an amorphous structure after such process. The polycrystalline gate dielectrics may be problematic because grain boundaries serve as high-diffusion paths of oxygen and dopants, causing undesirable interfacial layer growth, electrical instability, and defect generation [29]. In addition, grain size and orientation changes throughout the polycrystalline film could cause significant variations in dielectric constant, leading to irreproducible properties.

1.3.1.3 Interface Quality

A clear goal of any potential high-*k* gate dielectric is to obtain a sufficiently high-quality interface with the Si channel, as close as possible to that of SiO_2. The typical production SiO_2 gate dielectrics have a midgap interface state density (D_{it}) of ~2×10^{10} states/cm^2, whereas most of the high-*k* materials show D_{it} ~10^{11}-10^{12} states/cm^2. Obviously, it is difficult to deposit any high-*k* material creating a better interface than that of SiO_2. Due to the high D_{it} observed in high-k gate dielectrics, degradation in leakage current and carrier mobility are therefore expected. The ideal gate dielectric stack could have an interfacial layer comprised of several monolayers of Si-O containing material to improve interface properties, and also a high-*k* film on

top of the interfacial layer to provide physically thicker gate dielectric.

1.3.1.4 Process Compatibility

A crucial factor in determining the final film quality and properties is the method by which the dielectrics are deposited in a fabrication process. The deposition process for the dielectric must be compatible with current or expected CMOS processing, cost, and throughput. Physical vapor deposition (PVD) methods have provided a convenient means to evaluate materials systems for alternate dielectric applications. However, the damage inherent in a sputtering PVD process results in surface damage and thereby creates unwanted interfacial states. For this reason, chemical vapor deposition (CVD) methods, such as metal organic chemical vapor deposition (MOCVD) and atomic layer chemical vapor deposition (ALCVD), have proven to be quite successful in providing uniform coverage over complicated device topologies.

On the other hand, a significant issue for integrating any advanced gate dielectric into standard CMOS is that the dielectric should be compatible with poly-Si gate process. Poly-Si gates are desirable because dopant implant conditions can be tuned to create the desired V_{th} for both nMOS and pMOS, and also the process integration schemes are well established in industry. Moreover, metal gate are very desirable for eliminating dopant depletion effects and sheet resistance constraints, thus the metal gate has been widely investigated for future CMOS gate application.

1.3.1.5 Reliability

The electrical reliability of a new gate dielectric must also be considered critically for application in CMOS technology. The determination of whether or not a high-*k* dielectric satisfies the strict reliability criteria requires a well-characterized materials system. Moreover, recent lessons from the scaling changes associated with ultrathin SiO_2 may come into play with the high-*k* dielectric. Several major reliability issues observed in high-*k* gate dielectric are described as follows:

(1) Charge Trapping in High-*k* Gate Dielectrics

Most of the high-*k* dielectrics contain large amounts of fixed charge compared to SiO_2, independent of the high-*k* film deposition technique. The charge trapping centers responsible for the fixed charge are likely to occur within the bulk of the high-*k* film as well as at the interfaces between the high-*k* film and the gate electrode and the interfacial layer. The presence of charge trapping centers fundamentally influences reliability of high-*k* stack and poses a challenge for achieving the reliability goals.

Hysteresis of the *C-V* trace is frequently observed during *C-V* measurements of high-*k* stacks, with a magnitude that depends quite strongly on the measurement conditions, and the relative thickness of the high-*k* and interface layers. Rapid charging and discharging of defects at the high-*k*/Si interface have been suggested to explain these effects.

The V_{th} instabilities induced by the positive biased temperature stress instability (PBTI) and negative biased temperature stress instability (NBTI) are the key factors that limit successful integration of the high-*k* gate dielectrics. Process optimization of both the interface and high-*k* layers is vital to ensure acceptably low V_{th} shifts for both nMOS and pMOS over the circuit operational life.

(2) Hot Carrier Aging

The reliability impact of trapping of energetic hot carriers thus far has received little attention, but is a concern because high-*k* materials have reduced energy barriers for electron and hole injection. Hot carrier injection and charge trapping effects have the potential to be more significant compared to SiO_2.

(3) Dielectric Breakdown

Among all of the reliability issues associated with high-*k* gate dielectrics, the time dependent dielectric breakdown (TDDB) has been most intensively studied.

Depending on bias polarity, constant voltage stress of high-*k* stacks can result in soft- or hard-breakdown characteristics. Hard breakdown is favored with gate injection and decreasing thickness of the high-*k* layer relative to the interfacial layer. On the other hand for substrate injection, and thicker high-*k* layers, degradation of gate current is observed, followed by hard-breakdown. These effects in high-*k* dielectrics have been explained in terms of the breakdown of the interfacial layer with the polarity dependence of the breakdown resulting from the current limiting action of the interfacial layer with the polarity dependence of the breakdown resulting from the current limiting action of the high-*k* layer. Increase in gate current noise, which are typically associated with soft-breakdown in SiO_2, do not appear to correlate with breakdown of the high-*k* stack, implying that soft breakdown definitions may need to be modified for high-*k* stacks [30].

(4) Plasma-induced Damage

Almost no published data is currently available for the high-*k* gate dielectrics. This could be a serious yield and reliability issue since it involves charge trapping during processing.

(5) Defects

Since the intrinsic properties determine the ultimate capability of gate dielectric materials, the reliability at the circuit level is strongly driven by defects in high-*k* film. New defect types will be important and need to be characterized.

The details of the reliability issues in high-*k* gate dielectrics can be found in references [31-33].

1.3.2 Evolution of High-*k* Gate Dielectric

Many of the high-*k* materials initially chosen as potential alternative gate dielectric candidates were inspired by memory capacitor applications. The most commonly high-*k* gate dielectric candidates have been investigated such as Ta_2O_5,

$SrTiO_3$ and Al_2O_3, which have permittivity ranging from 10 to 80, and have been employed mainly due to their maturity in memory capacitor applications. Although the permittivity of Ta_2O_5 (~26) is very suitable for the gate dielectric application, however, the Ta_2O_5 are not thermally stable in direct contact with Si (this thermodynamic stability is not a requirement for memory capacitors, since the dielectric is in contact with the electrodes, which are typically nitrided poly-Si or metal in memory capacitors) [34], and an interfacial buffer layer of SiO_2 may be necessary to prevent the interfacial reaction between Ta_2O_5 and silicon. This may increase process complexity and impose thickness scaling limit of gate dielectric. Also, the conduction band offset (ΔE_c) for Ta_2O_5 is even much less than 1 eV [25], it will likely preclude using the Ta_2O_5 for gate dielectric application, since electron transport would lead to unacceptably high leakage currents. At the same time, it has been reported that the materials with ultra-high permittivity such as $SrTiO_3$ (k~80) may cause fringing field induced barrier lowering effect when it was used as the gate dielectric [24]. The barrier lowering effect induced by fringing fields from the gate-to-source/drain may weaken the gate control capability and degrade the short channel performance in MOSFET. Moreover, the approach of using $SrTiO_3$ requires sub-monolayer control of the channel interface for dielectric deposition [35]. This interface helps reduce reaction due to the thermodynamic instability of $SrTiO_3$ on Si, and also helps to accommodate the difference in lattice constants between Si and $SrTiO_3$. Thus, the thermal stability of $SrTiO_3$ in direct contact with Si is not so good, which is the similar problem as with Ta_2O_5, and the interfacial buffer layer of SiO_2 may also be necessary to prevent the interfacial reaction between $SrTiO_3$ and silicon. Unlike the thermally unstable Ta_2O_5 and $SrTiO_3$, Al_2O_3 shows excellent thermal stability in direct contact with Si [25], and the band offset of Al_2O_3 is ~2.8 eV [27]. Hence, Al_2O_3 may provide lower leakage current compared to other high-k gate dielectric. However, the Al_2O_3 gate dielectric shows poor reliability characteristics such as V_{th} instability induced by charge trapping effect [36]. Also, the permittivity of Al_2O_3 is only around 10 [25], which may not provide adequate benefits compared to conventional SiO_2 or SiON gate dielectric.

Due to the difficulties in searching for a suitable high-*k* gate dielectric among the mature materials for memory capacitor applications mentioned above, several groups have studied some novel high-*k* materials, such as Y_2O_3, La_2O_3, TiO_2, ZrO_2 and HfO_2. Guha et al. recently reported that the Y_2O_3 gate dielectric showed very low leakage current and interface state density, and also little or no flat band voltage shift. They also reported the formation of a thick interfacial layer due to interaction between Y_2O_3 and Si substrate [37]. The formation of thick interfacial layer indicates that the thermal stability of Y_2O_3 in direct contact with Si is still a serious issue. In the same paper, Guha et al. also investigated La_2O_3 gate dielectric. The authors reported that the La_2O_3 gate dielectric exhibited low leakage currents, but a thick interfacial layer formation, which was similar to the case of Y_2O_3, and a large flat band voltage shift of -1.4 V [37]. These results indicate that both thermal and electrical stability of La_2O_3 are not suitable for gate dielectric application. Moreover, full transistors using CVD TiO_2 as the gate dielectric were first reported by Campbell et al. [38]. The authors found that the TiO_2 gate dielectric showed a thick interfacial layer formation, unacceptably high leakage current and large interface state density of $10^{12}/cm^2$-eV. These results indicate that the TiO_2 film may not be suitable for the gate dielectric application due to the problems of thermal instability and very high gate leakage current.

Alternate dielectric materials of ZrO_2 and HfO_2 were reported in the 1970's and 80's for the purpose of optical coatings and DRAM applications. It was found that the degradation of the chemical properties for ZrO_2 as compared to HfO_2 might be due to the interaction of the poly-silicon gate electrode with the ZrO_2 [39], as well as the interaction of ZrO_2 with the silicon substrate to form silicide. For CVD ZrO_2 deposited on Si substrate, during annealing in UHV ambient, interfacial SiO_x triggers the formation of Zr-silicide at the channel interface, which are decomposed from ZrO_2 [40].

Recently, HfO_2 has been extensively studied among various candidates of high-*k* material due to its suitable dielectric constant (22~25) [41], relatively wide band gap (~5.6eV) with sufficient band offset (~1.4 eV) [27], and acceptable thermal

stability in direct contact with Si [42]. Moreover, for further improving the thermal stability and crystallization temperature, several research groups incorporated silicon, aluminum or nitrogen into HfO_2 to form Hf-based gate dielectrics, such as HfSiO [43], HfAlO [44], HfON [45], HfSiON [46] and HfAlON [47]. All of these Hf-based gate dielectrics exhibit good thermal stability and high crystallization temperature. Besides, some excellent electrical and reliability data were also reported on the Hf-based gate dielectrics, such as the HfTiO with k value of approximately 50 [48]. Thus far, the Hf-based gate dielectrics show the most promising characteristics for advanced CMOS application, and a lot of research groups from semiconductor industry and academia have made a great effort to implement the Hf-based gate dielectric in future CMOS technology.

1.3.3 Major Challenges of Hf-based Gate Dielectrics Implementation

Among various candidates of high-*k* materials, the Hf-based gate dielectrics show the most promising characteristics for advanced CMOS application. Many excellent results, including physical, electrical and reliability characteristics, were reported on the Hf-based gate dielectrics. However, there are still several major challenges for integration of the Hf-based gate dielectrics. The major challenges include (1) thermal stability issue, (2) mobility degradation, (3) charge trapping induced V_{th} instability, and (4) high V_{th} induced by Fermi-level pinning effect, which are described as below.

Besides these major challenges, some process issues of the Hf-based gate dielectric, such as the film deposition and etching, may also be carefully considered.

1.3.3.1 Thermal Stability

Compared to most of high-*k* materials, HfO_2 film shows acceptable thermal stability in direct contact with Si during high thermal budget CMOS process. However, unlike the conventional SiO_2 gate dielectric, the HfO_2 film crystallizes at a temperature below 500 ºC, which results in formation of grain boundaries in the HfO_2

film due to high temperature CMOS process (~1000 ºC). The grain boundaries in fully or partially crystallized gate dielectric can be the fast paths for oxygen and dopants diffusion into gate dielectric and even channel region in silicon substrate, causing low-*k* interfacial layer growth, electrical instability, and defect generation [29]. For further improving the thermal stability, incorporation of Si, Al or N into HfO_2 film was proposed to form HfSiO (HfSiON) or HfAlO (HfAlON), which remains amorphous structure after the high temperature process. Unfortunately, the dielectric constant of HfO_2 (~25) is significantly degraded by incorporating the Si or Al. The lower dielectric constant obtained in HfSiO (HfSiON) or HfAlO (HfAlON) is due to the oxide of Si or Al with much lower dielectric constant (SiO_2 ~3.9, Al_2O_3 ~7) compared to HfO_2. This may compromise the benefits of the HfSiO (HfSiON) or HfAlO (HfAlON) gate dielectrics and limit the continuous scaling of gate dielectric thickness. Consequently, the high-*k* gate dielectric with good thermal stability and also reasonable dielectric constant is still problematic.

1.3.3.2 Mobility Degradation

The carrier mobility in MOSFET channel is significantly lower than that in bulk silicon, due to additional scattering mechanisms. Lattice or phonon scattering is aggravated by the presence of crystalline discontinuity at the surface boundary, and surface roughness scattering severing severely degrades mobility at high normal fields. Channel mobility is also affected by processing conditions that alter the gate oxide interface properties, such as oxide charge and interface traps. The channel mobility was treated as a constant by defining an effective mobility as:

$$\mu_{eff} = \frac{\int_0^{x_i} \mu_n n(x) dx}{\int_0^{x_i} n(x) dx} \tag{1-6}$$

which is essentially an average value weighted by the carrier concentration in the inversion layer. Empirically, it has been found that when μ_{eff} is plotted against an effective field E_{eff}, there exists a universal relationship independent of the substrate

bias, doping concentration, and gate oxide thickness. The effective normal field is defined as the average electric field perpendicular to the gate oxide interface experienced by the carriers in the channel. Using Gauss's law, one can express E_{eff} in terms of the depletion and inversion charge densities:

$$E_{eff} = \frac{1}{\varepsilon_{Si}}\left(|Q_d| + \frac{1}{2}|Q_i|\right) \tag{1-7}$$

where $|Q_d| + \frac{1}{2}|Q_i|$ is the total silicon charge inside a Gaussian surface through the middle of the inversion layer. For low drain voltages, the effective field can be expressed as:

$$E_{eff} = \frac{V_t + 0.2}{3t_{EOT}} + \frac{V_g - V_t}{6t_{EOT}} \tag{1-8}$$

At high drain voltages, Q_i decreases toward the drain end of the channel. [9]

Hf-based gate dielectrics, as the most promising replacement of conventional SiO_2 or SiON, have attracted great attentions in the past few years, because of significant reduction of gate leakage current and good thermal stability. However, serious mobility degradation can be observed in most of the Hf-based gate dielectrics [49]. Many recent studies have explored the fact of mobility degradation, such that surface electron mobility in the HfO_2 nMOS was generally inferior to that of SiO_2 [50]. Incorporation of Al into HfO_2 resulted in further mobility degradation [29], and HfON showed lower carrier mobility compared to HfO_2 [51]. It has been proposed that coulomb scattering due to interface states and oxide charge in high-*k* is a major cause for mobility degradation [52], and soft optical phonons in high-*k* could also contribute to the mobility degradation [53]. The mobility degradation observed in high-*k* gate dielectrics results in a meaningless replacement of conventional SiO_2 or

SiON by high-*k*, which is the one of most important issues for implementation of high-*k* gate dielectric.

1.3.3.3 Charge Trapping Induced V_{th} Instability

Hf-based gate dielectrics exhibit significant charge trapping and de-trapping, which causes the V_{th} instability during operation, is a key integration challenge for their application in future COMS technology [54]. A. Kerber et al. proposed a pulsed I_d-V_g measurement to accurately measure effects due to fast trapping and de-trapping in HfO_2 [55]. In that paper, the HfO_2 film showed a large amount of hysteresis and V_{th} shift, especially when the pulsed I_d-V_g measurements were used. Moreover, it has been reported that the V_{th} shifts are observed under positive and negative biases in high-*k* gate stack [56]. The charge trapping under positive bias stress is more severe compared to conventional SiO_2-based gate dielectric, which is believed to happen due to filling of pre-existing bulk traps. On the other hand, the negative bias temperature instability (NBTI) induced V_{th} shifts in pMOS is qualitatively similar to those observed in SiO_2 or SiON devices, which is mainly due to the depassivation of Si-H bonds at the oxide/Si interface [56]. The charge trapping induced V_{th} instability in Hf-based gate dielectrics is very important reliability issue, which may seriously compromise the application of Hf-based gate dielectric.

1.3.3.4 Fermi Level Pinning Induced High V_{th}

Although the Hf-based gate dielectrics provide much lower leakage current in contrast to SiO_2, Fermi level pinning induced unacceptably high V_{th}, in particular for pMOS, is a serious challenge for integration of the Hf-based gate dielectrics into the mature poly-Si gate or even the advanced metal gate process [57]. In the same paper, it has been proposed that the V_{th} behavior in poly-Si/high-*k* device is dominated by the Fermi level pinning effect, which is different from the poly-Si/SiO_2 device. A reasonable mechanism suggests that the oxygen transport out of high-*k* gate dielectric into Si results in oxygen vacancies and associated electron traps within the dielectric,

as well as the formation of a dipole at the poly-Si/high-*k* interface, which causes the Fermi level pinning and increased V_{th} [58]. Moreover, the Fermi level pinning effect was also observed in high-*k* gate dielectric with metal gate electrode, which may be due to the existence of metal induced gap states [59]. The unacceptably high V_{th} induced by Fermi level pinning is a crucial issue in high-*k* gate dielectric, which also seriously compromises the implementation of high-*k* gate dielectric. The details of the Fermi Level pinning effect will be discussed in **Chapter 5**.

1.4 Major Achievements and Organization of This Thesis

In this thesis, the implementation of high-*k* gate dielectrics for advanced CMOS technology is the overall objective. In particular, this thesis will present several approaches to address the four major challenges for integration of the high-*k* gate dielectrics, including (1) thermal stability issue, (2) mobility degradation, (3) charge trapping induced V_{th} instability, and (4) Fermi level pinning induced high V_{th} mentioned above. In addition, a particular phenomenon of gate doping penetration induced excessive leakage current in poly-Si/high-*k* device will be presented in this thesis. Finally, the impact of nitrogen on charge trapping induced V_{th} instability will be discussed in metal-gate and poly-Si-gate/high-*k* devices, respectively. The specific objectives of each part and corresponding values are listed as follows:

In the first part, the Ta was incorporated into HfO_2 gate dielectric to form HfTaO gate dielectric by using reactive DC magnetron co-sputtering system. The purpose of this part of the study was to develop a novel Hf-based gate dielectric, which may possess high crystallization temperature, good thermal, and also maintain a high dielectric constant. X-ray diffraction (XRD) and high-resolution transmission electron microscope (TEM) were used to investigate the crystallization temperature of HfTaO gate dielectric, and the interfacial layer in HfTaO gate dielectric was examined by X-ray photoelectron spectroscopy (XPS). Moreover, the hysteresis for HfTaO MOS capacitor and the static (DC) and pulsed I_d-V_g measurement for HfTaO MOSFET were used to examine the electrical stability in HfTaO gate dielectric.

Mobility in HfTaO gate dielectric was also extracted by the standard split *C-V* method, and then compared with pure HfO_2 gate dielectric. The details of this study will be presented in **Chapter 2**. This study presents an excellent high-*k* gate dielectric candidate of HfTaO, which may possess sufficiently high crystallization temperature, good thermal and electrical stability, high carrier mobility, and also maintain a high dielectric constant. In addition, the results of this study may suggest a broader hypothesis for further research into the effect of high-*k* film morphology on charge trapping induced V_{th} instability, and also contribute a better understanding of mobility degradation in high-*k* gate dielectric.

In the second part, a thin SiO_2 layer (~1 nm) was inserted between HfTaON and Si substrate to form a novel HfTaON/SiO_2 gate stack. The aim of this part of the research was to investigate the effect of the insertion of SiO_2 layer on interface properties of high-*k* gate dielectric, and also determine whether the mobility degradation in high-*k* gate dielectric might be suppressed by insertion of the thin SiO_2 layer. To examine the interface properties of HfTaON/SiO_2 gate stack, the charge pumping current measurement was performed for the HfTaON/SiO_2 MOSFET, and the interface state density (D_{it}) of HfTaON/SiO_2 gate stack was also calculated based on the measured charge pumping current. Moreover, the mobility in HfTaON/SiO_2 gate stack was extracted by the standard split *C-V* method, and then compared with conventional pure SiO_2 gate dielectric and the HfTaON gate dielectric without the inserted SiO_2 layer. The detailed results of this study will be presented in **Chapter 3**. The research introduces a very promising HfTaON/SiO_2 gate stack for advanced low standby power application, which may provide good thermal and electrical stability, low gate leakage current, excellent interface properties, and superior electron and hole mobility. The results of this research may be of importance in explaining the major reason of mobility degradation in high-*k* gate dielectric, and also propose an effective method to suppress the mobility degradation for advanced low standby power CMOS application.

In the third part, HfO_2 nMOS capacitors with different doping concentration poly-Si gates were fabricated. The aim of this part of the research was to investigate

the effect of gate doping penetration on gate leakage current in poly-Si/HfO_2 nMOS devices. To examine the variety of gate leakage currents, the *J-V* curves were compared for the HfO_2 nMOS devices using poly-Si gates with different gate doping concentrations. Conducting atomic force microscopy (C-AFM) was applied to examine the current images of the HfO_2 films and TEM was used to check possible diffusion paths of dopant in the HfO_2 film. The detailed results of this study will be presented in **Chapter 4**. The study presents a particular phenomenon of gate doping penetration induced excessive gate leakage current in poly-Si/high-*k* device, which may provide a rule to successfully fabricate the poly-Si/high-*k* devices. Moreover, the results of this study may propose a reasonable explanation for the excessive gate leakage current normally observed in poly-Si/HfO_2 devices, and also make a useful contribution on the integration of high-*k* gate dielectrics into conventional poly-Si gate process.

In the forth part, a novel high-*k* transistor structure of poly-Si/poly-SiGe/ Al_2O_3/HfO_2 was developed. The major purpose of this part of study was to determine whether the unacceptably high V_{th} induced by Fermi level pinning effect in poly-Si/high-*k* structure might be suppressed by using poly-SiGe gate and Al_2O_3 capping layer. MOSFETs with HfO_2 gate dielectrics and poly gate were fabricated and the differences of V_{th} for the poly-Si/HfO_2, poly-Si/Al_2O_3/HfO_2, and poly-Si/poly-SiGe/Al_2O_3/ HfO_2 MOSFETs were compared. To examine the effects of poly-SiGe gate and Al_2O_3 capping layer on electrical and reliability characteristics, the measurements of transconductance (G_m) and V_{th} shift due to constant voltage stress were also made for the poly-Si/HfO_2, poly-Si/Al_2O_3/HfO_2, and poly-Si/poly-SiGe/ Al_2O_3/HfO_2 MOSFETs. The details of this study will be presented in **Chapter 5**. The study presents a novel poly-Si/poly-SiGe/high-*k* device structure, which may effectively suppress the Fermi level pinning induced high V_{th} and propose a feasible method to successfully integrate high-*k* gate dielectric into the mature poly-Si gate process. Moreover, the results of this study could be very useful for exploring the origin of the Fermi level pinning effect at poly-Si/high-*k* interface.

In the fifth part, the nitrogen was incorporated into HfO_2 and HfAlO gate

dielectrics by using plasma nitridation. The purpose of this part of the study was to investigate the role of nitrogen on charge trapping induced V_{th} instability in metal-gate and poly-Si-gate/high-*k* devices, respectively. To examine the impact of nitrogen on charge trapping induced V_{th} instability, the constant voltage stresses were applied and the V_{th} shifts were measured. Moreover, the *C*-*V*, *J*-*V*, and transistor characteristics were measured to examine the effect of nitrogen on electrical characteristics in high-*k* devices. The details of this study will be presented in **Chapter 6**. This research reports a novel finding in which the nitrogen in high-*k* gate dielectric play a different role in charge trapping induced V_{th} instability between metal-gate and poly-Si-gate/high-*k* devices. The results of this research may provide a guide line to optimize the deposition of high-*k* gate dielectric for suppressing the charge trapping induced V_{th} instability, and also contribute a better understanding of this charge trapping induced V_{th} instability in high-*k* gate dielectric.

In general, the results of all studies presented in this thesis may contribute to a good understanding of material properties, physical, electrical and reliability characteristics in high-*k* gate dielectric for advanced CMOS application.

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Chapter 2

A Novel HfTaO with Excellent Properties for Gate Dielectric Application

2.1 Introduction

The industry's demand for greater integrated circuit functionality and performance at lower cost requires continuous scaling of device dimensions. This aggressive shrinking is driving the conventional SiO_2 or SiON gate dielectric to its physical limits due to excessive gate leakage current and reliability concerns. High dielectric constant (*k*) material, as a replacement of the conventional gate dielectrics, have attracted great attentions in the past few years, because of their potential for reducing gate leakage current while keeping the equivalent oxide thickness (*EOT*) thin. Among various candidates of high-*k* material, HfO_2 has been extensively studied due to its suitable dielectric constant (22~25) [1], relatively wide band gap (~5.6 eV) with sufficient band offset (~1.4 eV) [2], and acceptable thermal stability in contact with Si [3]. However, HfO_2 crystallizes at temperature below 500^{o}C. Grain boundaries in fully or partially crystallized gate dielectric may be the fast paths for oxygen and dopants diffusion into gate dielectric and even channel region in silicon substrate, causing low-*k* interfacial layer growth, electrical instability, and defect generation [4]. To increase the crystallization temperature, there have been reported on silicon, aluminum or nitrogen incorporated into HfO_2 to form Hf-based gate dielectrics, such as HfSiO [5], HfAlO [6], HfON [7], HfSiON [8] and HfAlON [9].

All of these materials exhibit high crystallization temperature and good thermal stability in contact with Si to withstand the conventional 900-1000ºC activation annealing.

As discussed in **Chapter 1**, there are still many challenges to hold back the actual application of the high-*k* materials. One of the major challenges in the high-*k* gate dielectrics is the serious mobility degradation relative to SiO_2 [10]. Many recent studies have explored the fact of mobility degradation, such that surface electron mobility in the HfO_2 nMOSFETs is generally inferior to that of SiO_2 [11]. Incorporation of Al into HfO_2 results in mobility degradation [4], and HfON shows lower carrier mobility compared to HfO_2 [12]. Moreover, electrical instability induced by charge trapping is another key factor to limit successful integration of high-*k* films. Significant amount of hysteresis and threshold voltage (V_{th}) shift in HfO_2 films have been reported [13].

Considering the main requirements on thermal stability, surface carrier mobility and electrical stability in high-*k* gate dielectrics, Hf-silicates (HfSiO and HfSiON) are the most promising candidates for integration. There have been several reports on the incorporation of both Si and N into HfO_2, which were found to improve thermal stability significantly [8], [14]. Inumiya *et al*. demonstrated HfSiON MOSFETs using plasma oxidation and nitridation, which provided excellent interface properties and high mobility [15]. In the report [13], HfSiON films showed good electrical stability, such as 10 times lower V_{th} shift caused by constant voltage stress compared to HfO_2. Unfortunately, the dielectric constant of HfSiON is significantly degraded due to the incorporated SiO_2 with low *k* value (~3.9) [16]. According to a report [17], HfSiON with optimized composition remained amorphous up to 1100 ºC whereas dielectric constant decreased to ~10. The disadvantage of low *k* value in Hf-silicates may not provide adequate benefits compared to conventional SiO_2 or SiON gate dielectrics and limit the continuous scaling of gate dielectric thickness. In terms of application, the Hf-silicates appears to be very promising materials for low power devices rather than high speed device, which requires further scaling down of *EOT* to less than 10 Å in the near future [12].

In this chapter, we propose a novel Hf-based gate dielectric by examining the effects of Ta inclusion in HfO_2 on the crystallization temperature, thermal stability, interface quality, leakage current, electrical stability and surface carrier mobility. Material studies indicate that the crystallization temperature of HfO_2 is significantly increased by adding Ta. Moreover, the results of extensive electrical characterization demonstrate that the interface state density and charge trapping are decreased considerably. Consequently, the peak electron mobility in HfTaO MOSFETs is more than twice higher than that in HfO_2. Simultaneously, the dielectric constant of HfTaO is no obvious degradation compared to HfO_2, which is due to the Ta oxide with high dielectric constant (~26) [16].

2.2 Experiments

The nMOSFETs were fabricated on 6-inch p-type Si substrates (N_A=1×10^{15} cm^{-3}) using the conventional self-aligned MOSFET process. After standard pre-gate clean with diluted HF dipping, NH_3 interface treatment was performed by rapid thermal annealing (RTA) at 700ºC for 10 sec. It has to mention that the NH_3 treatment could degrade the interface quality and mobility of device, even though it may inhibit the formation of the low-*k* interfacial layer during deposition and high temperature annealing. The films of HfO_2 and HfTaO with two different Ta compositions were deposited by reactive DC magnetron co-sputtering at room temperature, followed by post-deposition annealing (PDA) in N_2 ambient at 700ºC for 40sec to form high quality gate dielectrics. The sputtering of gate dielectrics was performed in Ar + O_2 (Ar: O_2 = 25: 2) ambient, and the Ta concentrations in HfTaO films were controlled by the ratio of the power applied to Hf and Ta target. X-ray photoelectron spectroscopy (XPS) results showed that the compositions of three samples are HfO_2, HfTaO with 29% and 43% Ta (refer to $Hf_{0.71}Ta_{0.29}O_x$ and $Hf_{0.57}Ta_{0.43}O_y$). 200-nm thick TaN metal gate was deposited by reactive DC sputtering using Ta target in Ar + N_2 (Ar : N_2 = 5 : 1) ambient. After gate patterning, the energy of 50 KeV phosphorous was implanted with a dose of 5×10^{15} cm^{-2}. Source and drain activation annealing was then conducted

at atmospheric pressure in N_2 ambient at different temperatures from 900ºC to 1000ºC for 30 sec. Sintering was done at 420^{o}C in forming gas for 30 min after Al metallization.

Thick films (~400 Å) subjected to annealing at various temperatures were prepared for x-ray diffraction (XRD) measurement to investigate the crystallization temperature of all samples. XPS and high-resolution transmission electron microscope (TEM) were used to analyze composition of films, bonding structure, interfacial layer and crystallization of the HfO_2 and HfTaO films. Electrical characteristics were evaluated using HP4156A precision semiconductor parameter analyzer and HP4284A precision LCR meter. *C-V* curves were measured at 1 MHz and simulated to determine *EOT* and flat-band voltage (V_{fb}) with quantum effects taken into account. Standard two-level, constant amplitude charge pumping current measurement was used to evaluate the interface state density (D_{it}). Electron mobility was calculated by a standard split *C-V* method on transistors with W/L ratio of 400μm/20μm.

2.3 Results and Discussion

2.3.1 Physical Characteristics of HfTaO

Fig. 2.1 shows the XRD spectra for HfO_2, HfTaO with 29% Ta, HfTaO with 43% Ta, and Ta_2O_5 films as a function of annealing temperature. The films under examination are with the similar physical thickness (~400 Å). Except for the as-deposited films, all samples were annealed under the specified temperature by either RTA or furnace annealing (below 600^{o}C) in N_2 ambient. The annealing times were 30 sec for RTA and 30 min for furnace annealing. According to the XRD spectra, the crystallization temperatures of HfO_2, HfTaO with 29% Ta, HfTaO with 43% Ta and Ta_2O_5 films are 400°C, 700°C, 1000ºC and 800ºC respectively, as summarized in **Fig. 2.2**. Similar crystallization temperatures of pure HfO_2 (~400ºC) [18] and Ta_2O_5 (~700ºC) [19] have been reported. It was interesting to note that the crystallization temperature of 43% Ta HfTaO film is higher than that of pure HfO_2 and Ta_2O_5. There

is not a clear understanding of the mechanism behind this phenomenon. It is possible to speculate that the phenomenon could be attributed to the breaking of the periodic crystal arrangement or the inhibition of continuous crystal growth in dielectric by incorporating Ta into HfO_2 film.

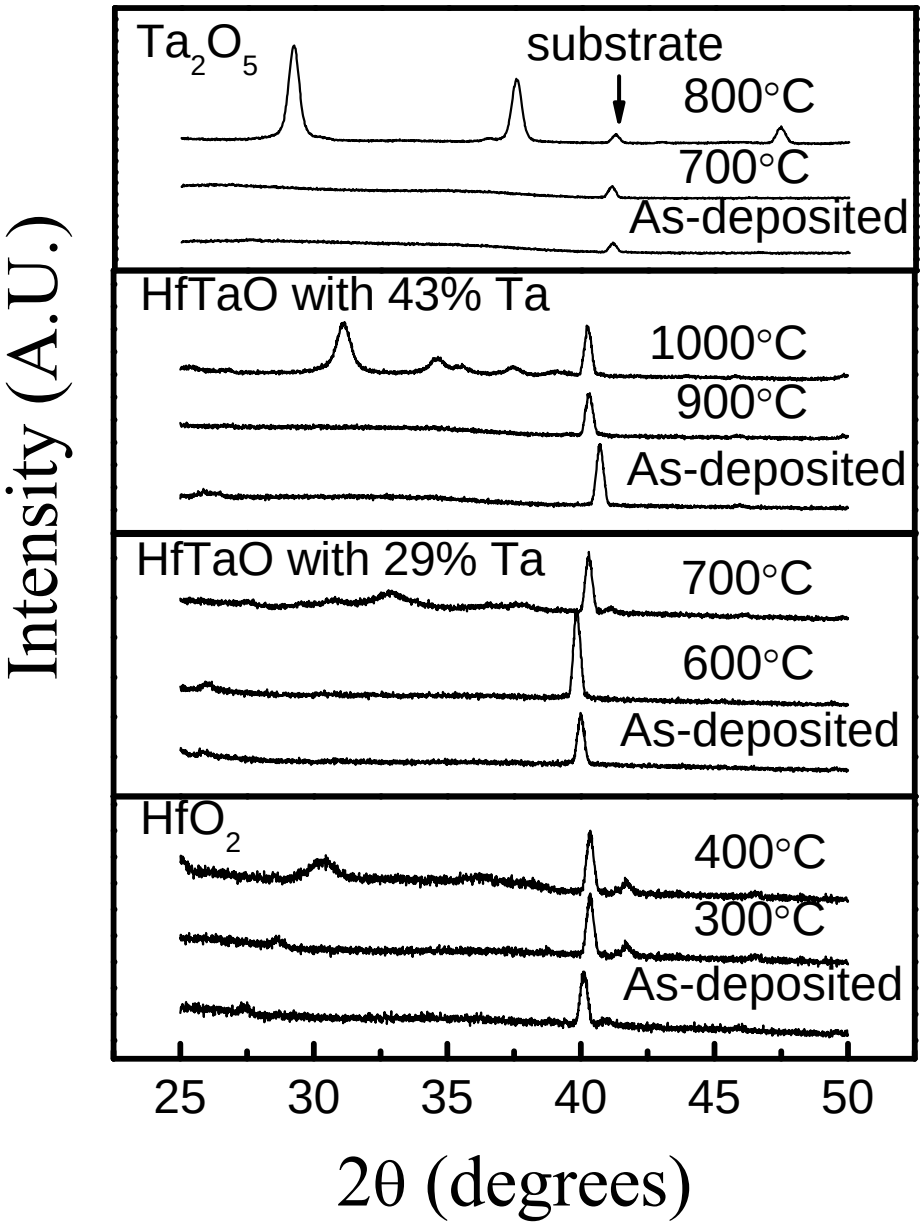


Fig. 2.1: XRD spectra of HfO_2, HfTaO and Ta_2O_5 films for as-deposited and different temperature annealing in N_2 ambient. The crystallization temperature of HfO_2 film is increased up to 1000^o C by incorporating 43% Ta.

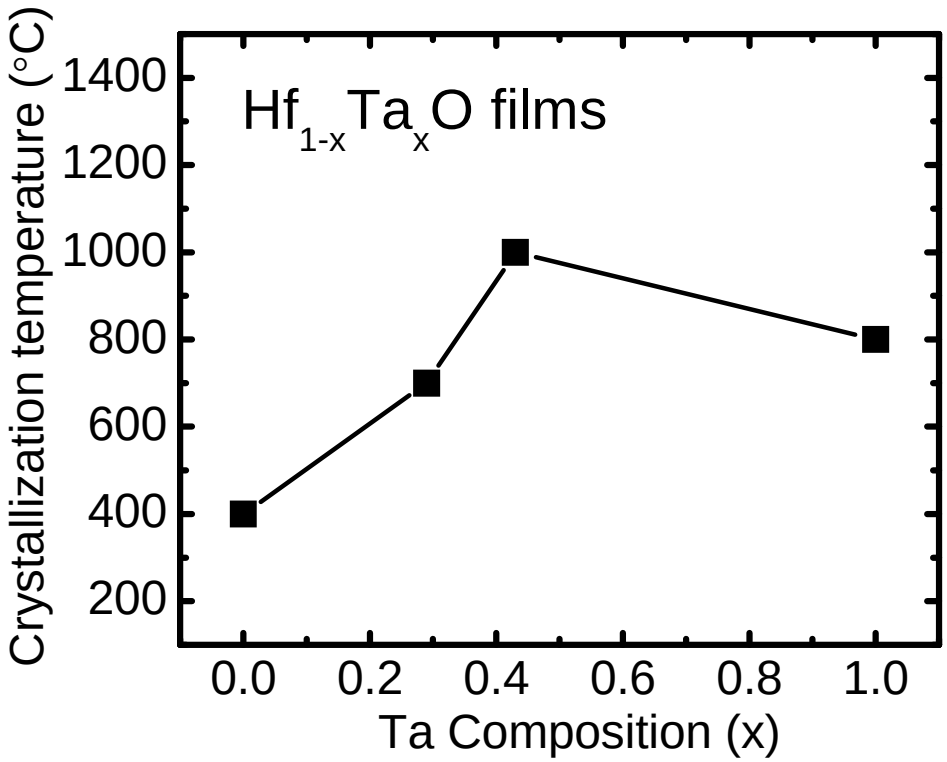


Fig. 2.2: Crystallization temperatures of HfTaO films as a function of Ta composition. It is noted that the crystallization temperature of HfTaO with 43% Ta is higher than that of pure HfO_2 and Ta_2O_5.

The high-resolution TEM micrographs of HfO_2 and HfTaO with 43% Ta gate dielectrics, after PDA at 700^o C for 40 sec and activation annealing at 950^o C for 30sec, are shown in **Fig. 2.3**. The TEM pictures confirmed that the HfO_2 film is fully crystallized whereas the HfTaO with 43% Ta film remains amorphous structure after such annealing. Before activation annealing, the physical thicknesses of HfO_2 and HfTaO with 43% Ta films were 54.7 and 51.4 Å (measured by ellipsometer), respectively. After activation annealing, the physics thicknesses of HfO_2 and HfTaO with 43% Ta films were 41 and 38.7 Å (measured by TEM images), respectively. From the TEM images, the interfacial layers (IL) of HfO_2 and HfTaO with 43% Ta samples were 18.9 and 12 Å, respectively. It was noted that the HfTaO with 43% Ta film provides a thinner IL compared to that of HfO_2. This may be attributed to the fact

that 43% Ta HfTaO film remains amorphous after such annealing, and effectively blocks oxygen diffusion through the grain boundaries to form low-*k* interfacial layer.

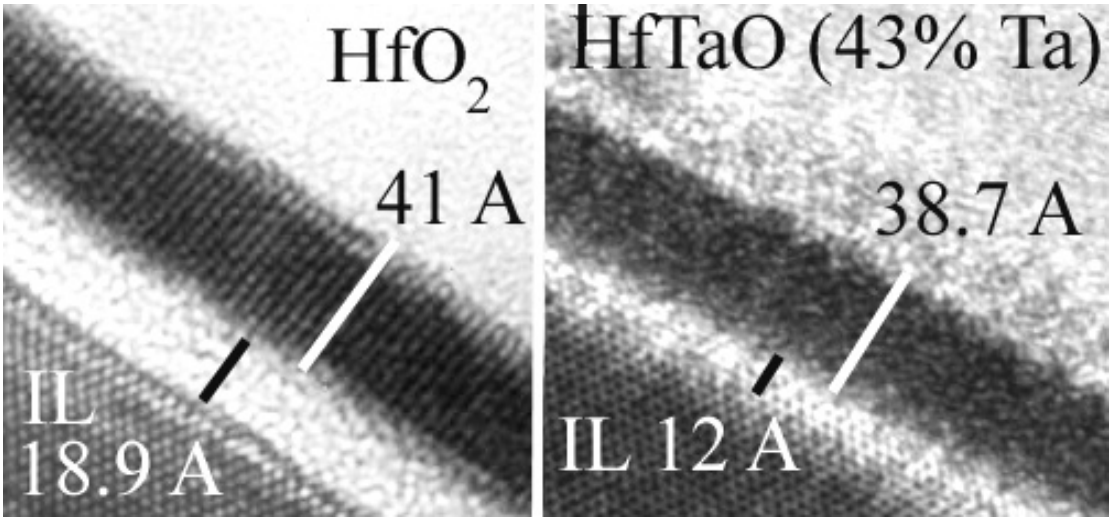


Fig. 2.3: TEM micrographs of HfO_2 and HfTaO with 43% Ta films after activation annealing at 950ºC for 30 sec. The HfO_2 film shows fully crystallized and HfTaO with 43% Ta film remains amorphous structure.

XPS measurement was performed on all films with physical thickness of ~50 Å after PDA at 700° C for 40 sec and activation annealing at 950° C for 30sec in N_2 ambient. **Fig. 2.4** (a) and (b) show Hf *4f* and Ta *4f* photoelectron regions for HfO_2 and HfTaO samples. It has been reported that the Hf-Si peak appears at 14.3 eV when the HfO_2 film is annealed at a given annealing condition in UHV ambient [20], and Ta-Si peak should be located at the binding energy lower than Ta *4f* peak. In these figures, no evident Hf-Si or Ta-Si peak was observed. This indicates that Hf, Ta and Si atoms are only bonded to O atoms as nearest neighbors.

Analysis of the XPS Si *2p* peaks is shown in **Fig. 2.5** after PDA at 700° C for 40 sec and activation annealing at 950° C for 30sec. The two peaks are attributed to the Si substrate (~99.3 eV) and the interfacial layer (~102.8 eV). As increasing the Ta composition from 0 to 43%, there was an increase in intensity of the peak located around 102.8 eV as well as a slight shift towards high binding energy. Si bonded to oxygen in a pure SiO_2 layer is located at ~103.6 eV [21]. The difference of binding

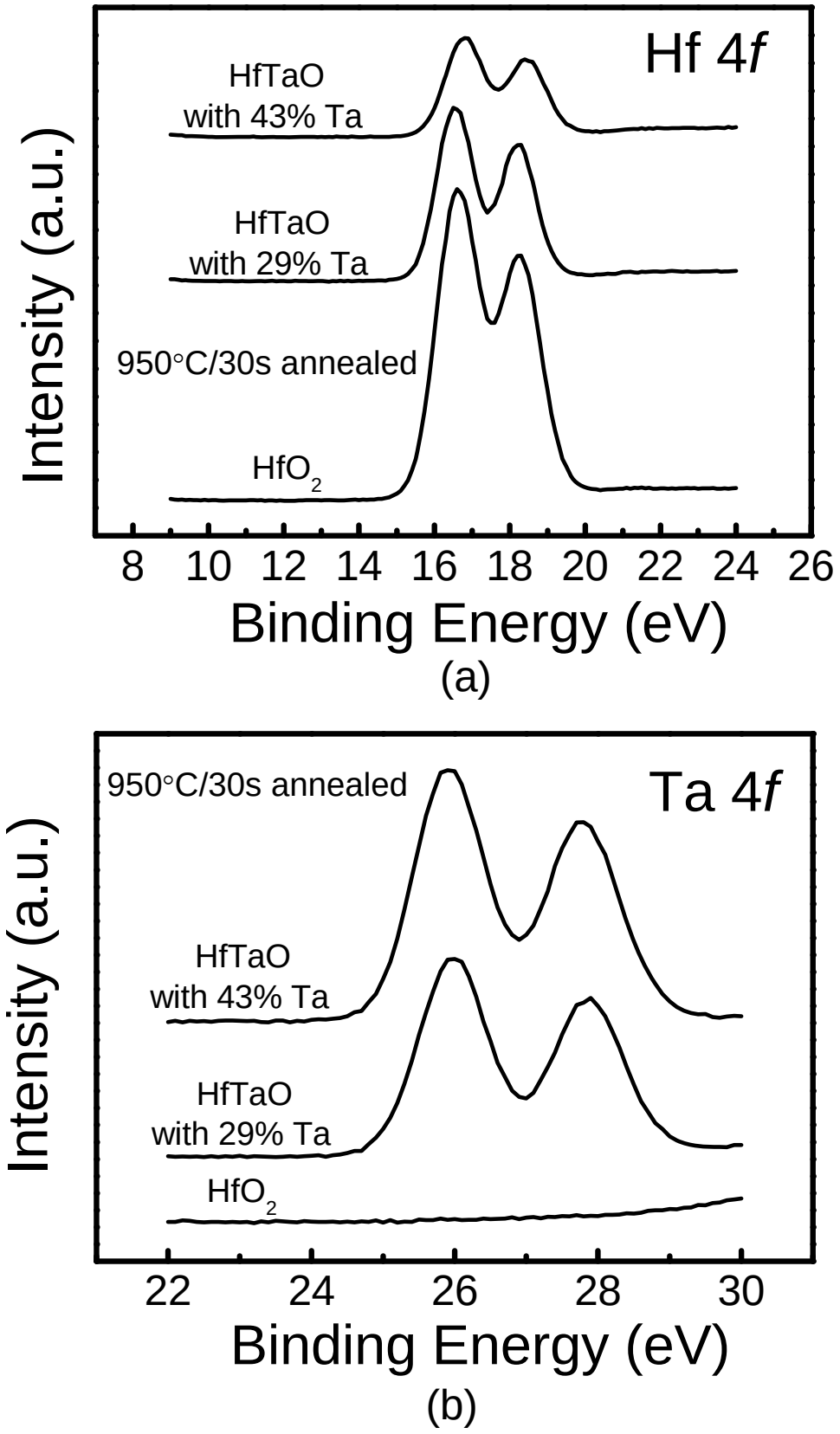


Fig. 2.4: XPS spectra for (a) Hf 4*f* core level and (b) Ta 4*f* core level taken from HfO_2, HfTaO with 29% and 43% Ta films after PDA at 700^{o} C for 40 sec and activation annealing at 950^{o} C for 30sec. Any evidence of Hf-Si or Ta-Si bonds formation can not be observed in the films.

energy between SiO_2 and the interfacial layer was around 0.8eV, indicating that the composition of interfacial layer is a silicate-like compound [22]. The increased peak intensity in interfacial layer indicates that the atomic percentage of Si-O bonds is increased by adding Ta. This implies that the interfacial layer between high-*k* and Si substrate tends toward a SiO_2-like layer with increasing the Ta composition in the high-*k* film. It also suggests a chemical similarity of the HfTaO/Si interface to high quality SiO_2/Si interface due of the high atomic percentage of Si-O bonds in the interfacial layer between HfTaO and Si substrate.

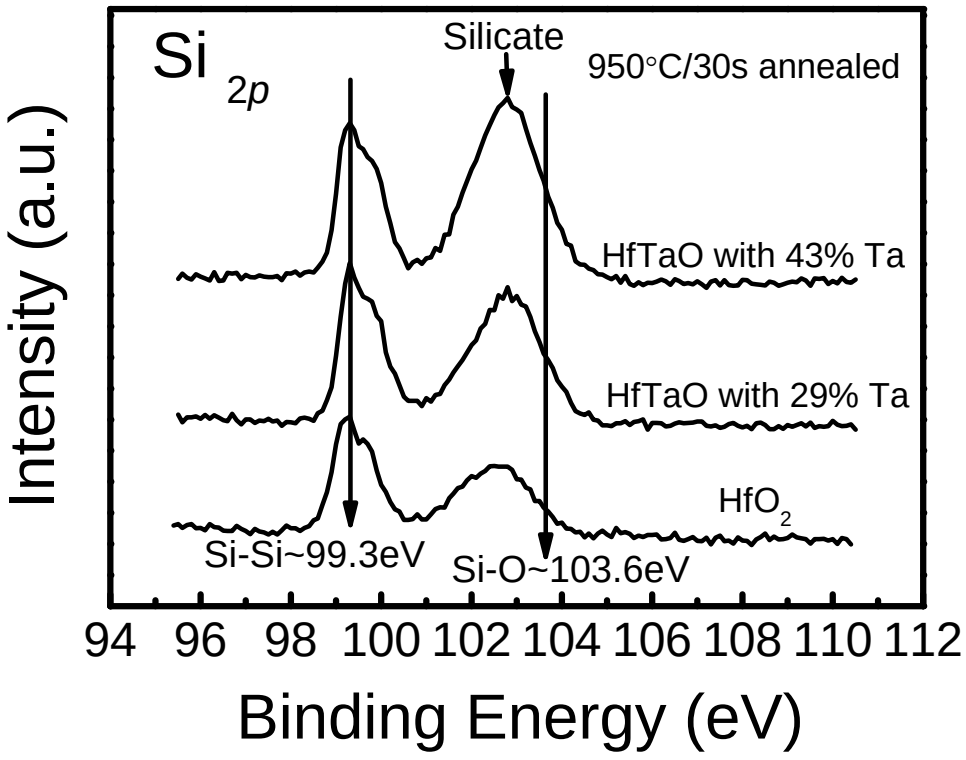


Fig. 2.5: XPS spectra for Si 2*p* peaks of HfO_2, HfTaO with 29% and 43% Ta films after PDA at 700° C for 40 sec and activation annealing at 950° C for 30sec. The silicate-like IL peak (102.8 eV) slightly shifts to high binding energy with Ta composition, as well as with increased intensity.

2.3.2 *C-V, J-V,* Thermal Stability and Interface Properties of HfTaO

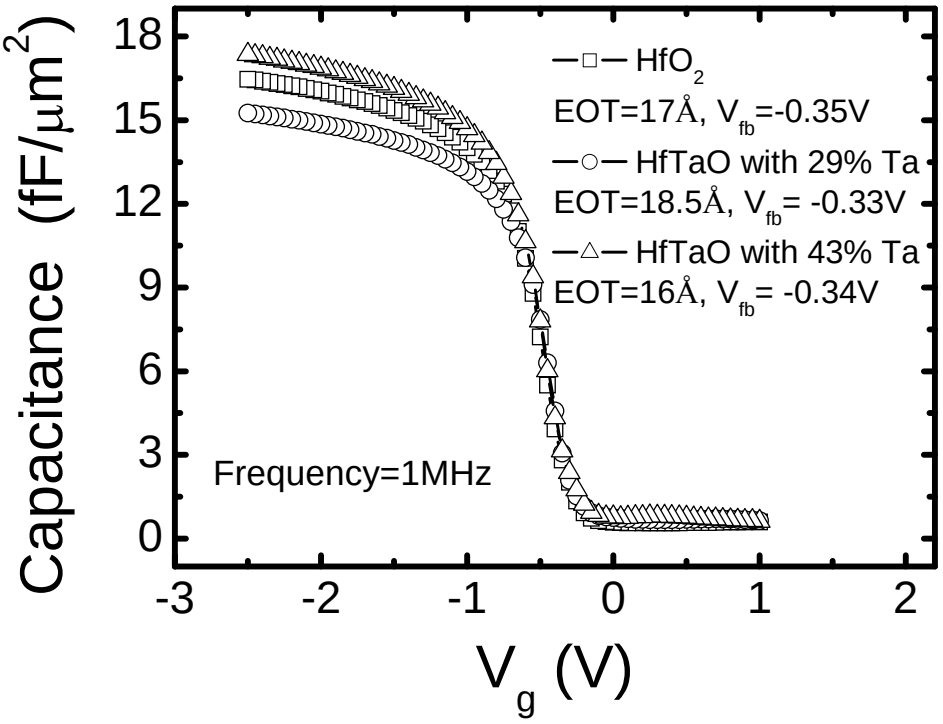


Fig. 2.6: Typical *C-V* curves of MOS capacitors with HfO_2, HfTaO with 29% and 43% Ta gate dielectrics after activation annealing at 950° C for 30sec. The HfO_2 and HfTaO capacitors show similar flat band voltage, indicating that negligible fixed charges were introduced by incorporating Ta into HfO_2.

Fig. 2.6 shows typical capacitance-voltage (*C-V*) characteristics of HfO_2 and HfTaO gate dielectrics after activation annealing at 950ºC for 30 sec. *EOT* of HfO_2, HfTaO with 29% Ta, and HfTaO with 43% Ta, which were extracted from the *C-V* curves measured at 1 MHz after considering the quantum effect, were 17, 18.5 and 16 Å, respectively. Since the physical thicknesses measured by ellipsometry were 54.7 Å for HfO_2, 56.8 Å for 29% Ta HfTaO and 51.4Å for 43% Ta HfTaO films respectively, it was noted that the HfTaO films with similar physical thicknesses exhibit similar *EOT* compared to HfO_2. This indicates that the HfTaO shows similar dielectric constant with pure HfO_2 (k~25), and no obvious degradation is observed by

incorporating Ta into HfO_2. As shown in **Fig. 2.6**, the HfO_2 and HfTaO capacitors exhibited similar flat band voltage (V_{fb}), indicating that negligible fixed charges were introduced by incorporating Ta into HfO_2. The corresponding current-voltage (*J-V*) characteristics for the films represented in **Fig. 2.6** are compared in **Fig. 2.7**. It was

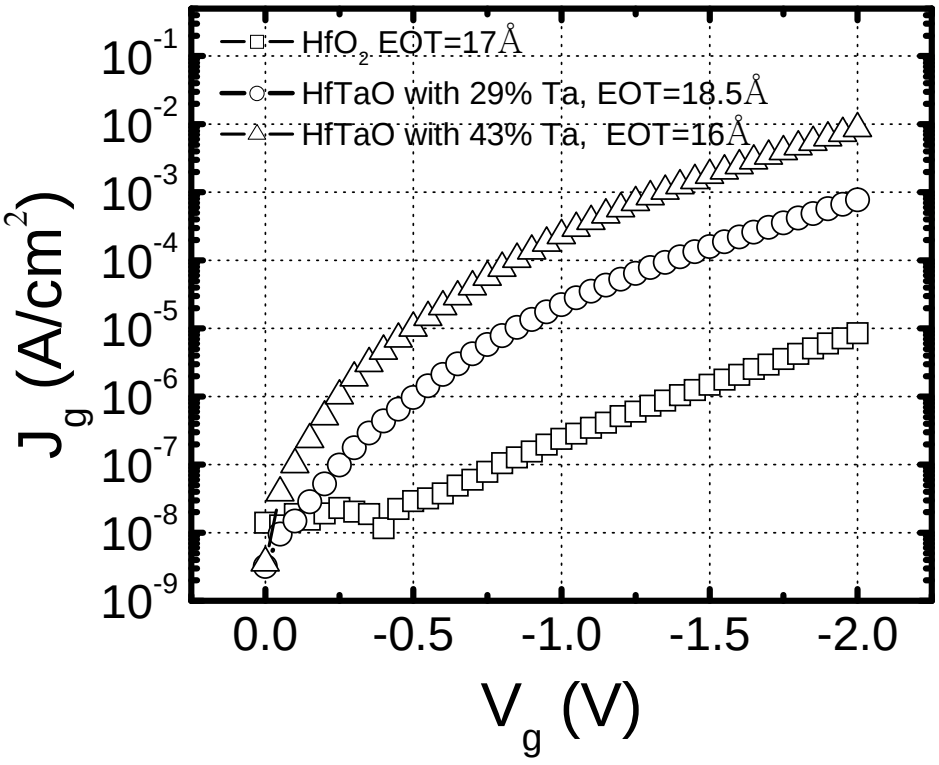


Fig. 2.7: Typical *J-V* curves of MOS capacitors with HfO_2, HfTaO with 29% and 43% Ta gate dielectrics after activation annealing at 950°C for 30 sec. HfTaO dielectrics show higher leakage current compared to HfO_2.

found that the leakage currents of HfTaO films increase with Ta composition. **Fig. 2.8** compares the leakage currents of HfO_2, HfTaO and some published results as a function of *EOT*. All of data in this figure were collected in the accumulation region at V_{fb}-1V. Although the leakage currents of HfTaO films were higher than that of pure HfO_2 due to the lower band offset of Ta oxide (1~1.5 eV) [16], it is still comparable to HfSiO [23], HfAlO [24], HfSiON [17], and HfAlON [9]. This can be explained by the HfTaO films exhibiting higher dielectric constant than those materials, which may

result in reduced gate leakage current due to the thicker physical thickness of HfTaO film at the same *EOT*.

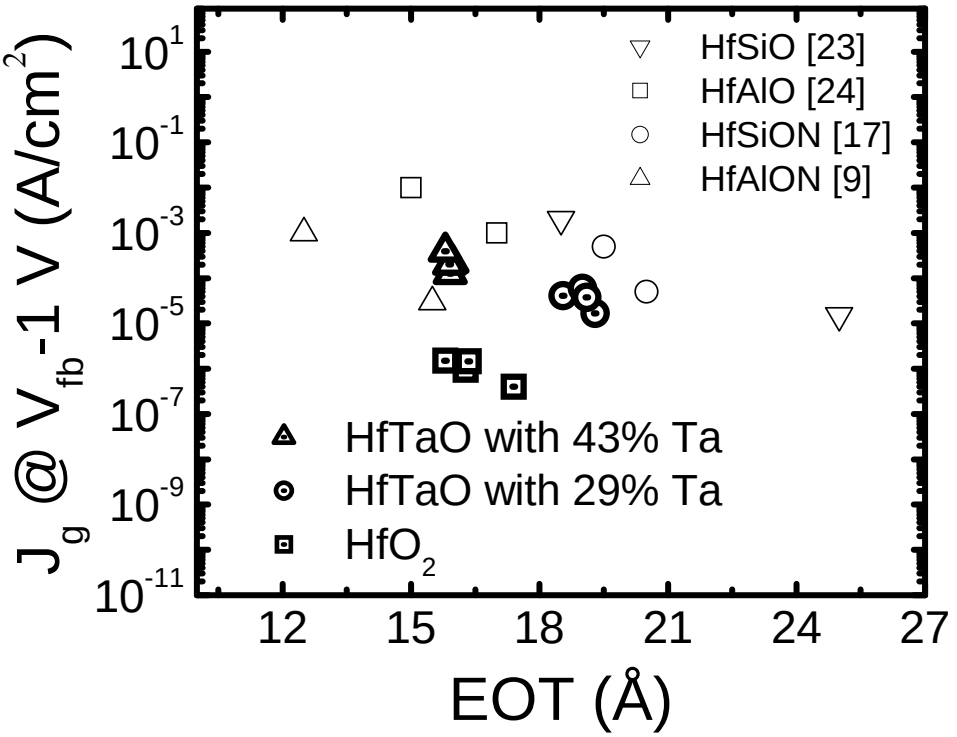


Fig. 2.8:Comparison of leakage currents vs. *EOT* for HfO_2, HfTaO and published results. Even the leakage currents of HfTaO films are higher than HfO_2, still comparable to HfSiO [23], HfSiON [17], HfAlO [24], and HfAlON [9].

Fig. 2.9 illustrates thermal stability by comparing the variation of *EOT* and leakage current for HfO_2 and HfTaO with 43% Ta samples with TaN metal gate after different temperature annealing. It was clearly observed that *EOT* increases with increasing annealing temperature and the enhancement of *EOT* in HfO_2 is higher than that of HfTaO. This may be attributed to the fact that the amorphous HfTaO films effectively block oxygen diffusion through the grain boundaries to form low-*k* interfacial layer. On the other hand, the leakage current density did not change obviously with annealing temperature for both HfO_2 and HfTaO. Although the HfO_2 films were fully crystallized, the leakage current of HfO_2 was still lower than that of amorphous HfTaO. It was also noted that the leakage currents of HfTaO with 43% Ta

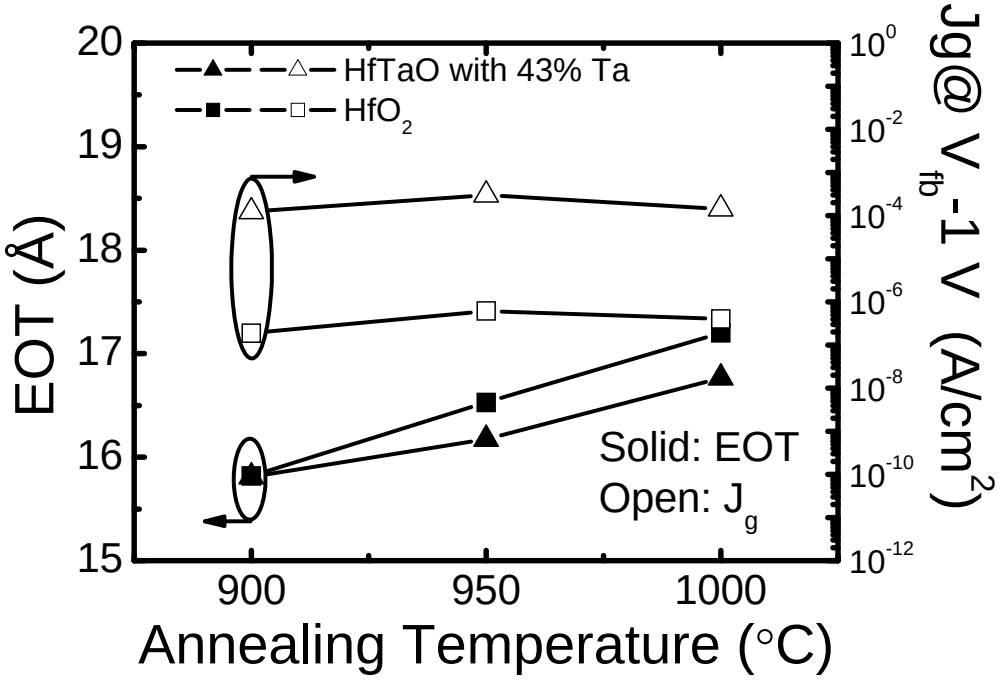


Fig. 2.9: *EOT* and gate leakage currents as functions of the activation annealing temperature. The increased *EOT* in HfO_2 is slight higher than that in HfTaO.

after 900ºC and 1000ºC annealing are similar, even though the HfTaO with 43% Ta film remained amorphous after annealing at 900ºC and became crystallized after annealing at 1000 ºC (based on the XRD results shown in **Fig. 2.1**). It suggests that the crystalline structures of high-*k* films have no obvious effect on the leakage current with TaN metal gate, which is similar with the results reported in [25].

Negligible frequency dispersion of the HfTaO with 43% Ta capacitance between 10 kHz, 100 kHz and 1 MHz is shown in **Fig. 2.10**. This indicates that the interface traps cannot respond at high frequency [26]. **Fig. 2.11** (a) shows hysteresis for HfO_2 and HfTaO with 43% Ta films after activation annealing at 950ºC for 30 sec. The hysteresis was quantified by the difference in V_{fb} during the voltage sweeps without delay time between ±3 V. **Fig. 2.11** (b) compares the hysteresis for the HfO_2 and HfTaO capacitors as a function of activation annealing temperature. The hysteresis for HfO_2 film was significantly improved by incorporating Ta, and also the

increase in annealing temperature. The improvement on the hysteresis indicates that the interface traps may be significantly reduced by incorporation of Ta into HfO_2 and the increase in activation annealing temperature, which may be due to the increased atomic percentage of Si-O bonds in interfacial layer as discussed in **Fig. 2.5**.

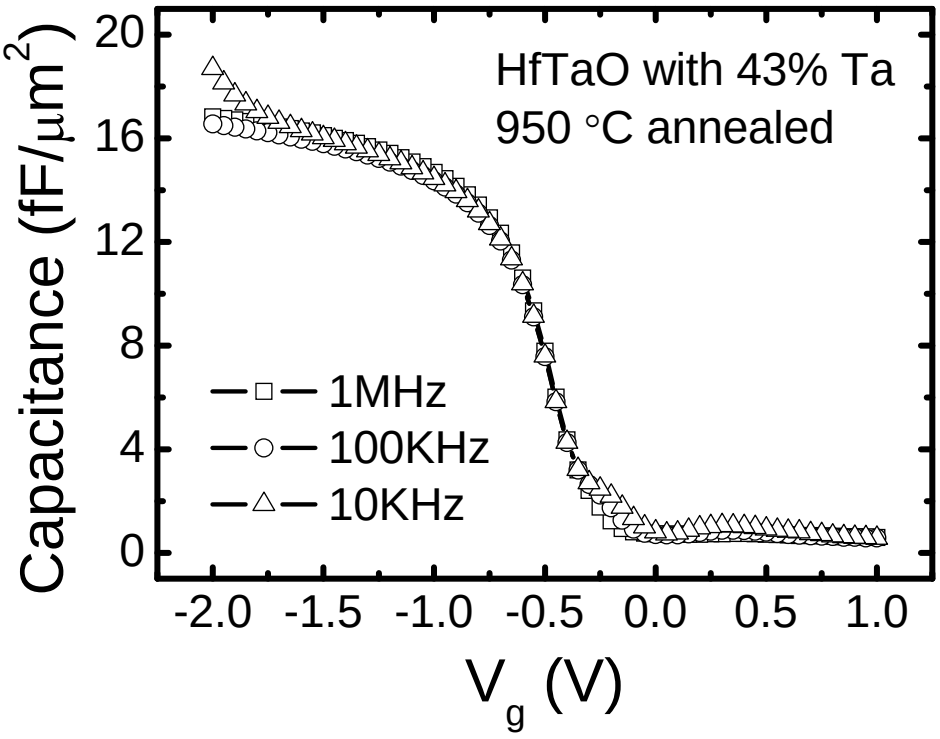
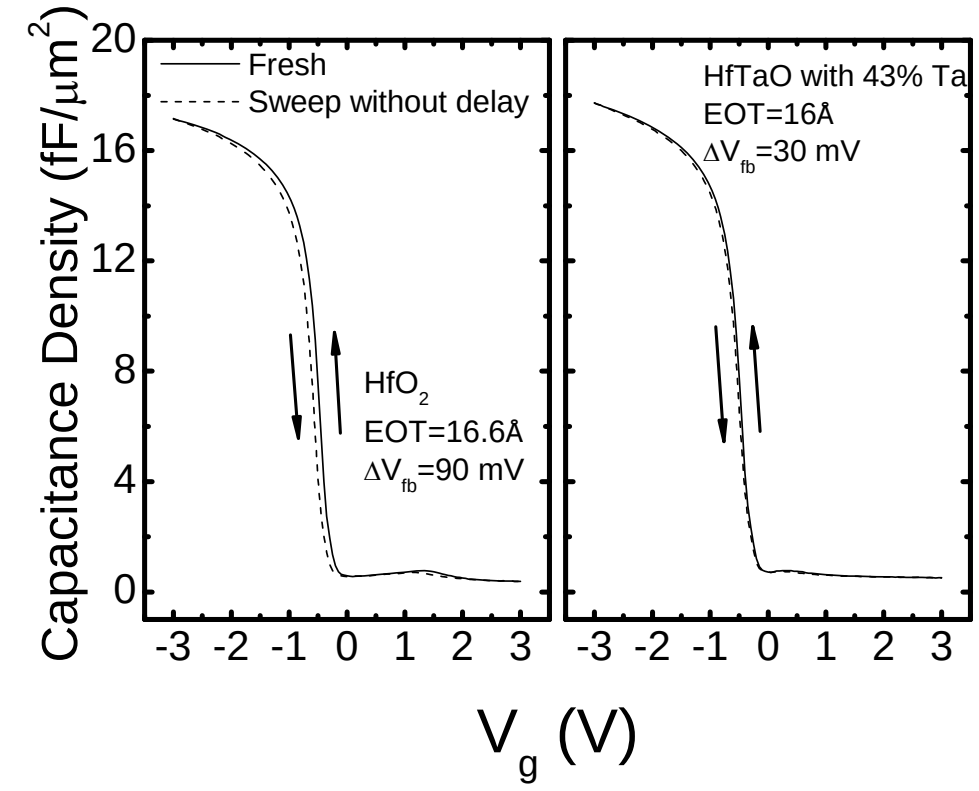
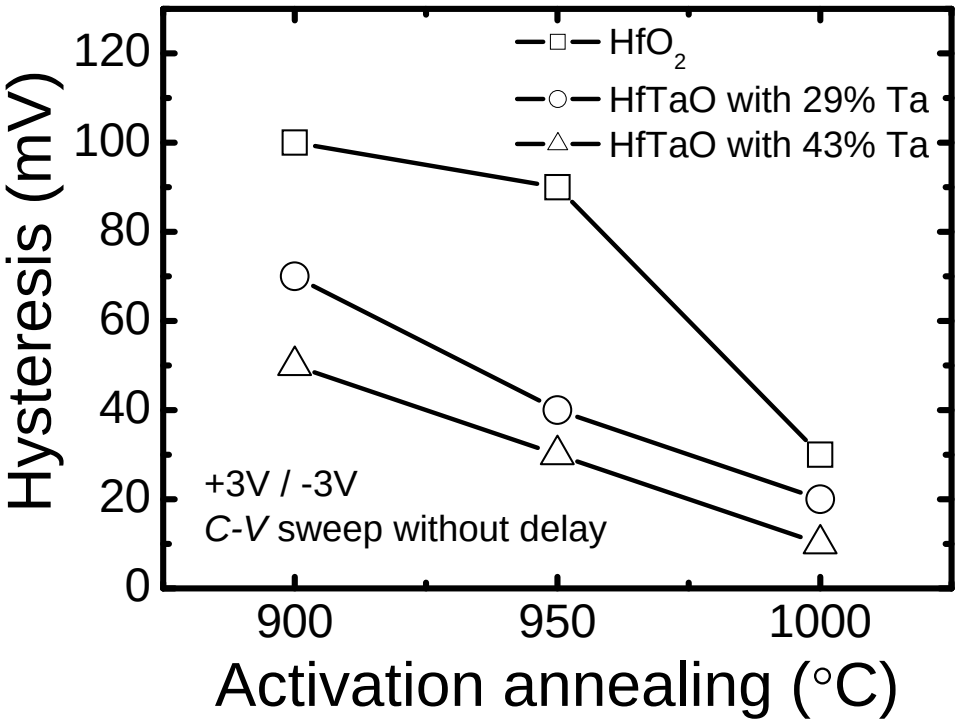


Fig. 2.10: Negligible frequency dispersion of the HfTaO with 43% Ta capacitance between 10 KHz, 100 KHz and 1 MHz. This indicates that the interface traps in the HfTaO gate dielectric can not respond at high frequency.



(a)



(b)

Fig. 2.11: (a) Hysteresis of HfO_2 and HfTaO with 43% Ta films after annealing at 950ºC for 30 sec. (b) Hysteresis of HfO_2 and HfTaO films as a function of activation annealing temperature. The hysteresis was quantified by the difference in V_{fb} during the voltage sweeps between ±3 V.

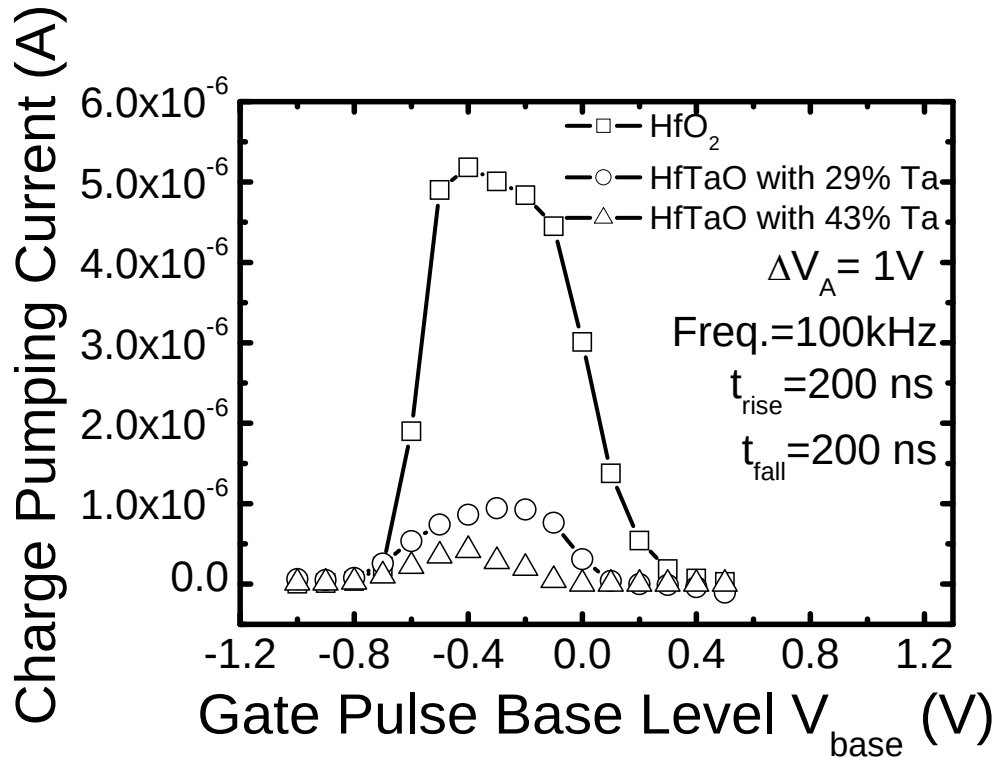


Fig. 2.12: Charge pumping current measured on nMOSFETs with HfO_2 and HfTaO gate dielectrics after activation annealing at 950ºC for 30 sec. By incorporating Ta into HfO_2 film, the charge pumping current is reduced by one order of magnitude.

Charge pumping currents in HfO_2 and HfTaO nMOSFETs after activation annealing at 950ºC for 30 sec, which is effective in quantitatively evaluating D_{it} [27], are compared in **Fig. 2.12**. Standard two-level and constant amplitude charge pumping method was used. The extracted D_{it} in HfO_2, HfTaO with 29% and 43% Ta films were 2.8×10^{12}, 5.1×10^{11} and 2.3×10^{11} cm^{-2}, respectively. It was noted that the D_{it} is reduced by one order of magnitude by incorporating Ta into HfO_2 film. This may be due to the formation of high atomic percentage of Si-O bonds at HfTaO/Si interface and it tends to high quality SiO_2/Si interface.

2.3.3 Charge Trapping Induced Electrical Instability in HfTaO

High-*k* gate dielectrics exhibit significant charge trapping and de-trapping, which cause the threshold voltage (V_{th}) instability during operation, are key integration challenges for their application in future CMOS technology [28]. In particular, the charge trapping under positive bias stressing (for nMOS devices) is known to be more severe compared to conventional SiO_2-based gate dielectrics, which is believed to happen due to filling of pre-existing bulks traps in high-*k*. This charge trapping effect may cause V_{th} shifts, and also drive current degradation over device operation time [29].

2.3.3.1 Static (DC) Measurement Technique

The electrical instability of CMOS devices with conventional gate dielectrics is commonly studied using static (DC) measurement technique. **Fig.2.13** illustrates the principle of the static (DC) measurement technique. Firstly, a fresh I_d-V_g curve

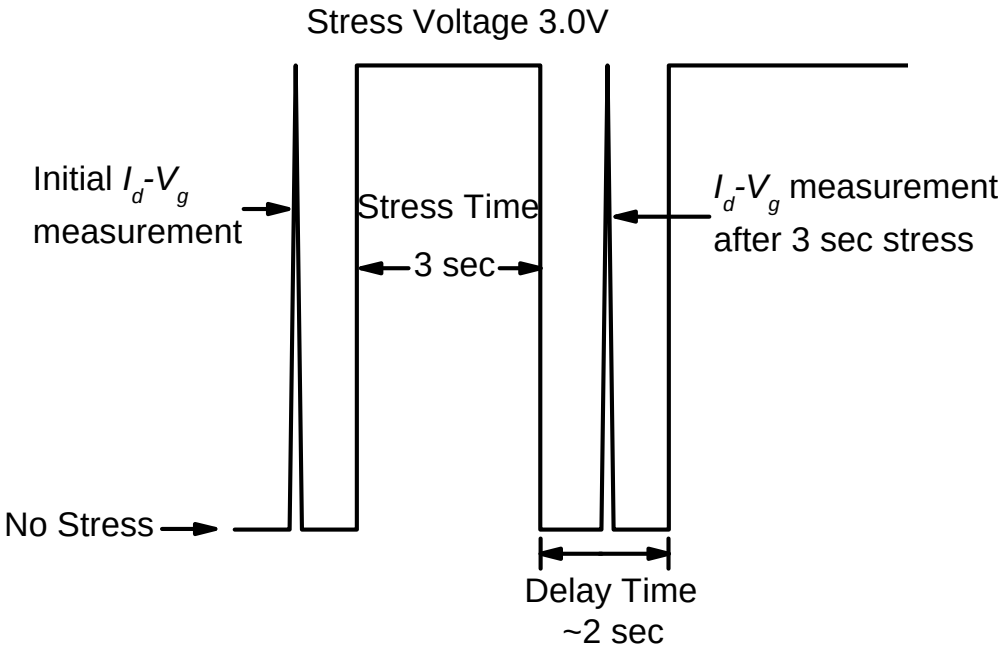


Fig. 2.13: Schematic diagram of the static (DC) measurement technique.

was measured to determine the initial V_{th}. Then a constant voltage stress was applied at gate electrode for a relevant time (3 to 1000 sec in this experiment), followed by a measurement of I_d-V_g curve again to identify the V_{th} shift after the constant voltage stress. It has to note that there was a delay time (~2 sec in this experiment) during the measurement of I_d-V_g, in which no constant voltage stress was applied. Since the charged traps due to the constant voltage stress could discharge during this delay time, a shorter delay time is desirable to minimize the impact of discharging.

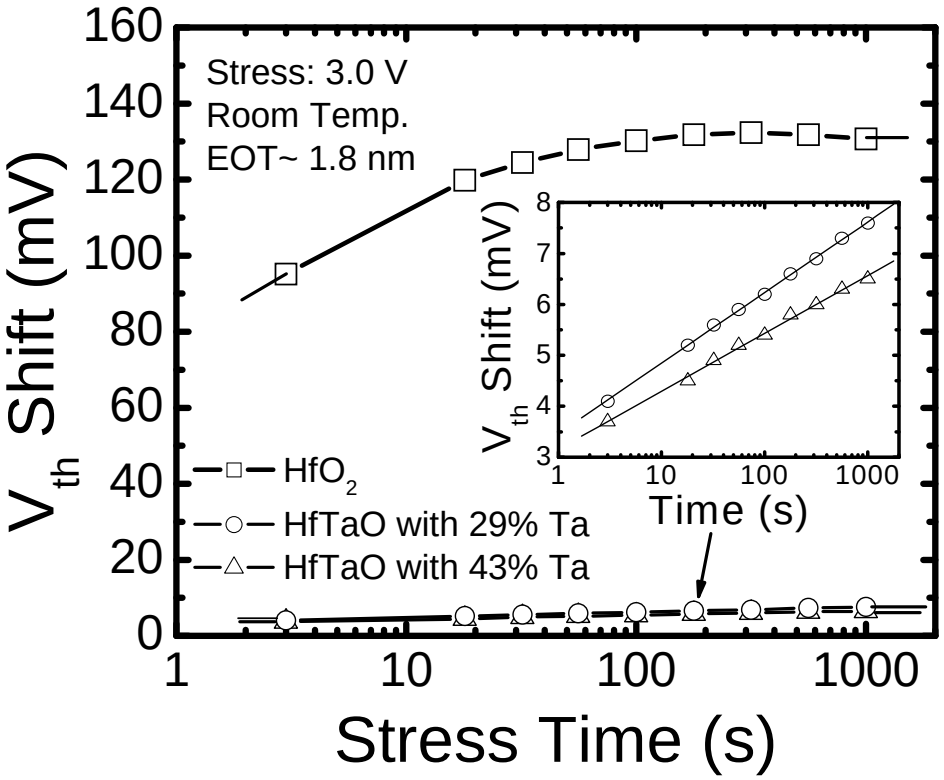


Fig. 2.14: Comparison of the V_{th} shifts due to constant voltage stress of 3.0 V in HfO_2 and HfTaO films measured by static (DC) technology. HfTaO has about 20 times lower V_{th} shift than HfO_2, indicating that HfTaO films have ultra lower traps compared to HfO_2.

By applying the static (DC) measurement technique, the V_{th} instability in HfO_2 and HfTaO gate dielectrics were examined. **Fig. 2.14** shows comparison of the V_{th} shift (ΔV_{th}) due to constant voltage stress in HfO_2 and HfTaO films. The stress of 3.0 V was applied at gate terminal, and I_d-V_g curve was measured to estimate the V_{th} shift. To ensure the V_{th} shift occurs only due to the stress voltage, I_d-V_g was measured using a limited voltage of 1.2 V. For each measurement, a fresh device with EOT around 18 Å was used. As shown in **Fig. 2.14**, ΔV_{th} increases with stress time and a huge amount of V_{th} shift in HfO_2 film whereas negligible shift in HfTaO. The data clearly show that HfTaO has about 20 times lower V_{th} shift than HfO_2, indicating that HfTaO films have much lower bulk traps compared to HfO_2. This is possibly due to the lack of crystallization in HfTaO films resulting in a significantly lower number traps compared to HfO_2 [13]. The severe V_{th} instability observed in the fully crystallized HfO_2 film could be related to grain boundaries with weaker bond strength and easy trapping.

Fig. 2.15 (a) and (b) show the constant voltage stress induced variations of subthreshold swing and transconductance (G_m), respectively. As shown in **Fig. 2.15** (a), no obvious degradation of subthreshold swing with stress time was observed. Since subthreshold swing is a measure of interface trap density, it is concluded that no interface traps were generated during stress. Similar behavior was also reported by another group in Al_2O_3 and HfO_2 films [29]. It is already known that the coulomb scattering due to the charged traps in gate dielectric may degrade the drive current of MOSFET. As shown in **Fig. 2.15** (b), the constant voltage stress induced charge trapping results in a reduction of ~10% G_m in HfO_2 film but almost no degradation in HfTaO films. This implies that the coulomb scattering induced by charged traps in gate dielectric is remarkably reduced by incorporating Ta into HfO_2 film, and then the degradation of drive current is also suppressed.

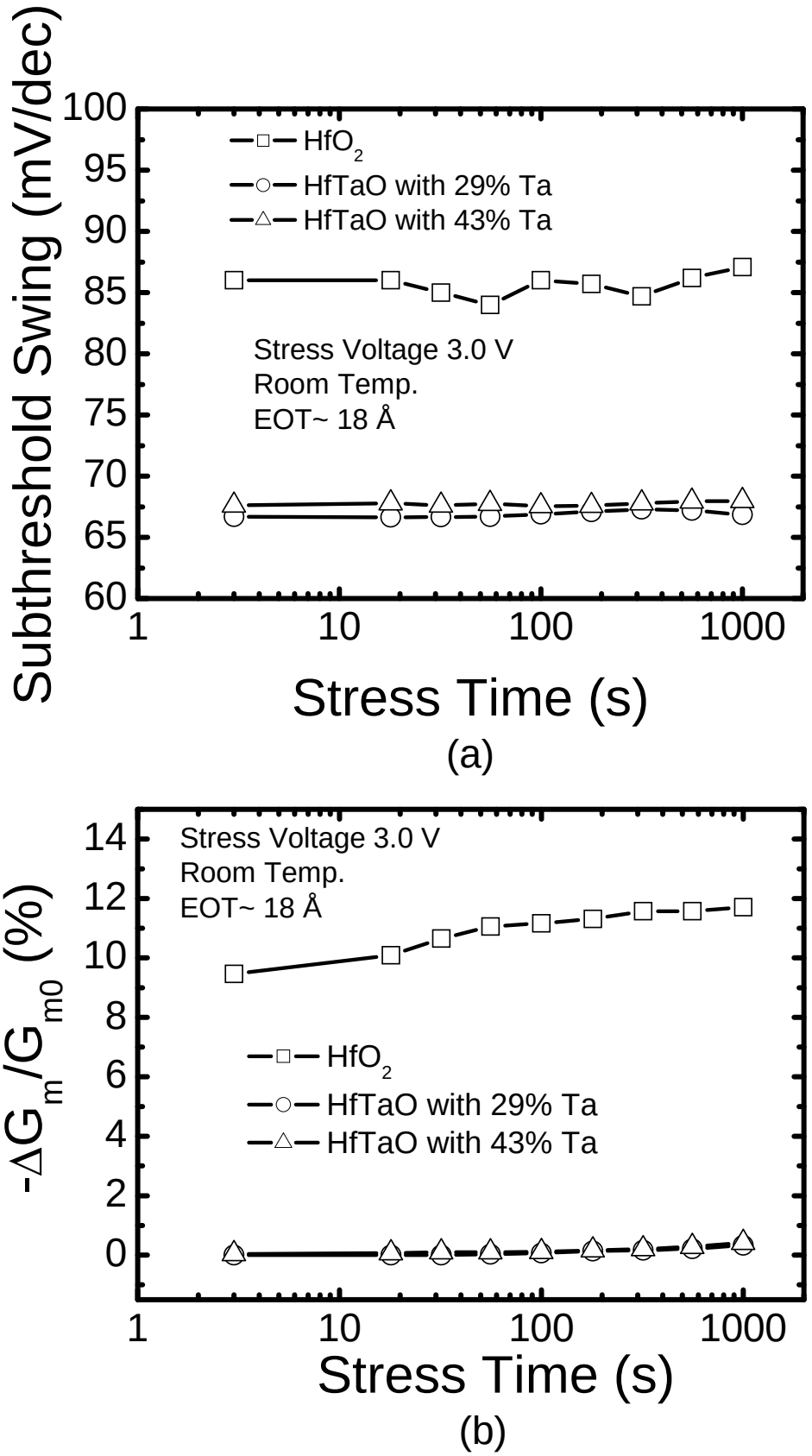


Fig. 2.15: (a) Subthreshold swing and (b) transconductance (G_m) variations as a function of constant voltage stress time. Negligible variations of subthreshold swing and G_m can be observed in HfTaO films.

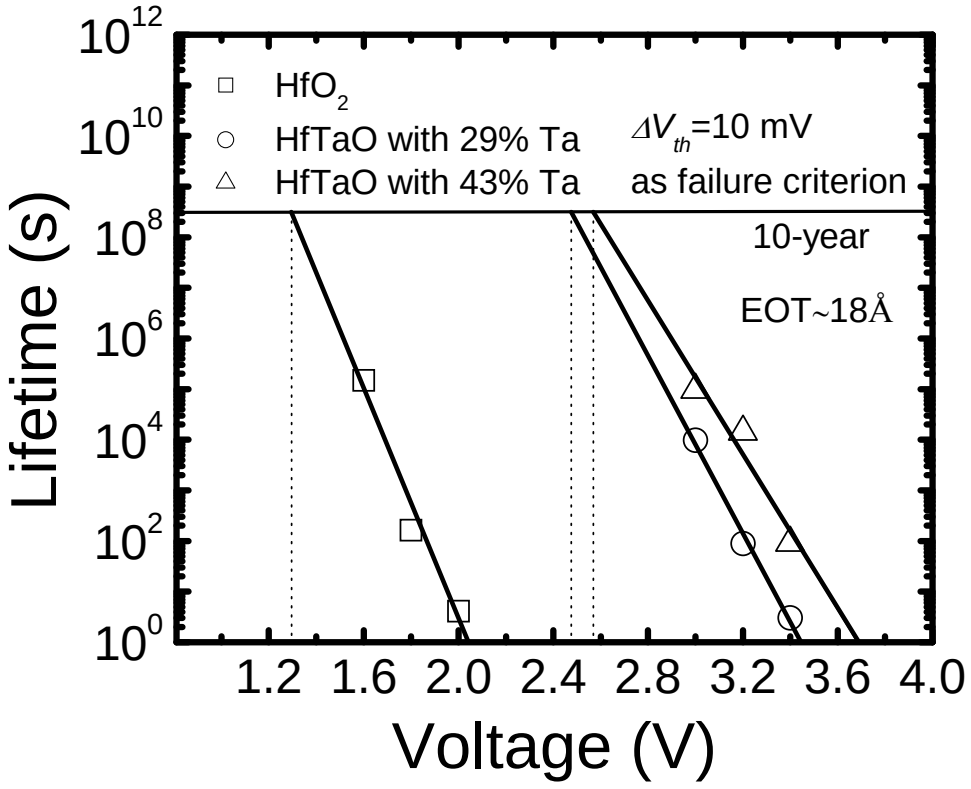


Fig. 2.16: Lifetime projection of charge trapping induced V_{th} shifts for HfO_2 and HfTaO gate dielectrics. The device lifetime of HfO_2 gate dielectric is greatly prolonged by incorporating Ta.

The 10-year lifetime projections of charge trapping induced V_{th} shift in nMOSFETs with HfO_2 and HfTaO films were extrapolated in **Fig. 2.16**. The failure criterion was defined at ΔV_{th} = 10 mV. The projected operating voltages with 10-year lifetime of HfO_2, HfTaO with 29% and 43% Ta nMOSFETs were 1.30 V, 2.47 V and 2.58 V, respectively. This indicates that the incorporation of Ta into HfO_2 greatly prolong the device lifetime.

2.3.3.2 Transient (Pulsed I_d-V_g) Measurement Technique

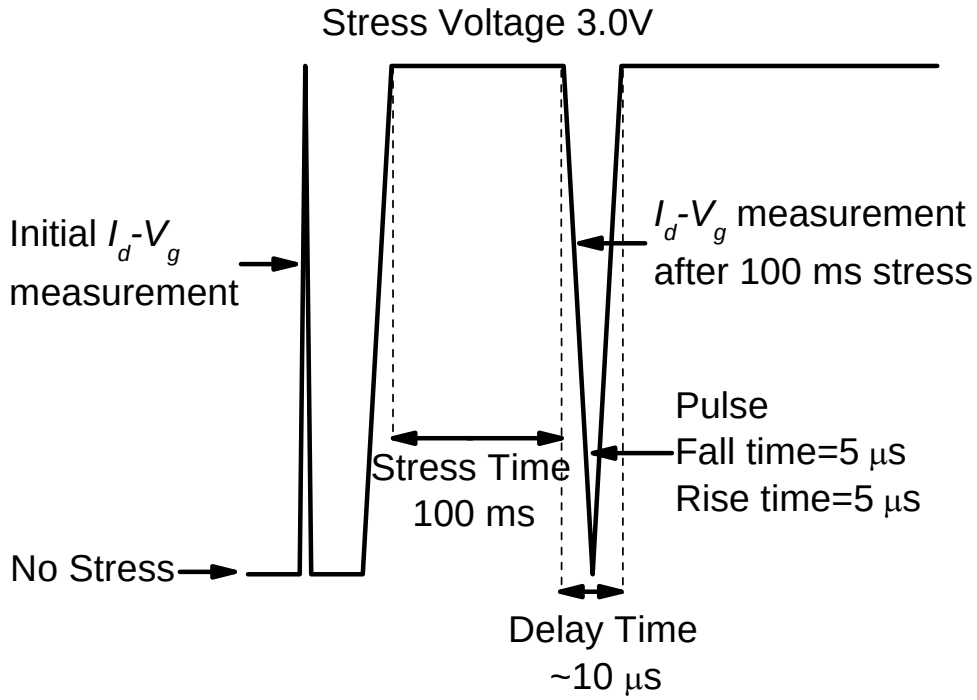


Fig. 2.17: Schematic diagram of the transient (pulsed I_d-V_g) measurement technique.

It has been reported that high-*k* gate dielectric film shows a large amount of V_{th} shift, especially when a transient measurement was used. A. Kerber et al. proposed the transient (pulsed I_d-V_g) measurement technique to accurately estimate fast charge trapping and de-trapping in HfO_2 [30]. **Fig.2.17** illustrates the schematic diagram of the transient (pulsed I_d-V_g) measurement technique. In this technique, the gate (V_g) and drain (V_d) biases are simultaneously recorded using a digital scope and converted into a I_d-V_g measurement. Compared to the conventional static (DC) measurement technology mentioned above, the pulsed I_d-V_g measurement technique enables drive current measurement down to the μs range (depend on the fall and rise times of

applied pulse) with short stress pulses, and more important, a short time delay (~10 μs in this experiment) between stressing and measurement, as shown in **Fig.2.17**. By using this pulsed I_d-V_g measurement technique with very short delay time, the discharging of charged traps may effectively minimize during the measurement of I_d-V_g. The detailed measurement setup can be found in [30].

Fig. 2.18 (a) shows comparison of the V_{th} instability in nMOSFETs with HfO_2 and HfTaO gate dielectrics using the pulsed I_d-V_g measurement technology. The 3.0 V stress was applied at the gate electrode and I_d-V_g curve was measured using a pulse with 5 μs fall and rise times. Compared to the results measured by static (DC) technology as shown in **Fig. 2.14**, the V_{th} shifts obtained by pulsed I_d-V_g technique were significantly enhanced. This is due to the conventional static (DC) measurement with a longer delay time severely underestimate the fast trapping and de-trapping effects in high-*k* gate dielectrics compared to the pulsed I_d-V_g measurement [30]. In **Fig. 2.18** (a), the data clearly show that V_{th} shift in HfTaO are much lower than HfO_2 film. This indicates that the HfTaO films have fewer bulk traps, as well as suppressed charge trapping compared to HfO_2. The reduction in drain current as a function of stress time is shown in **Fig. 2.18** (b). No significant changes in the drain currents were observed in nMOSFETs with HfTaO gate dielectrics whereas the drain current in nMOSFETs with HfO_2 film showed degradation over 8%. This is attributed to the suppression of charge trapping by adding Ta into HfO_2. Moreover, ~10% degradation in G_m was observed in HfO_2 film after long-time (1000 sec) stress in **Fig. 2.15** (b), however, the reduction of ~8% in drain current even after 100 ms stress was found in **Fig. 2.18** (b). This implies that the charge trapping at even very short time may be important for electrical instability in high-*k* gate dielectric.

Both results measured by the static (DC) and transient (pulsed I_d-V_g) measurement technologies clearly show that the charge trapping induced V_{th} shifts in HfTaO films are much lower than that in HfO_2. This indicates that the HfTaO films show excellent electrical stability and have ultra lower bulk traps compared to HfO_2, which is possibly due to the lack of crystallization in HfTaO films resulting in a significantly lower number traps.

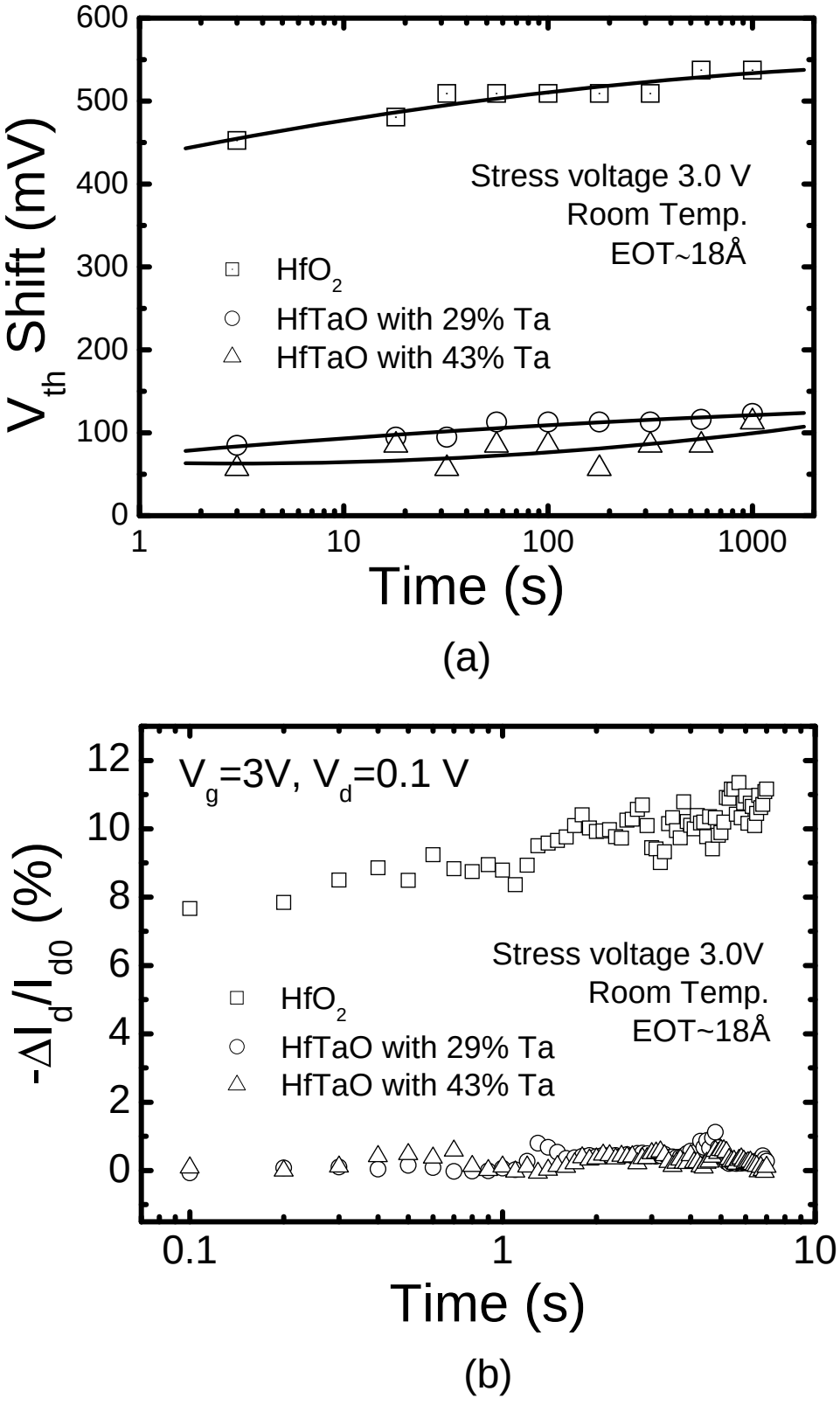


Fig. 2.18: (a) Comparison of the V_{th} shifts due to constant voltage stress of 3.0 V in HfO_2 and HfTaO films measured by pulsed I_d-V_g technology. (b) Charge trapping induced drain current degradation as a function of constant voltage stress time.

2.3.4 Transistor Characteristics and Mobility of HfTaO Gate Dielectric

Transistor characteristics of HfO_2 and HfTaO gate dielectrics (EOT~18Å) were investigated using nMOSFETs with a device dimension of channel width/length ratio of 400 μm/20 μm. **Fig. 2.19** (a) shows I_d-V_g characteristics of HfO_2 and HfTaO nMOSFETs after activation annealing at 950ºC for 30 sec. As can be seen, both 29% and 43% Ta HfTaO films exhibited excellent subthreshold swings of 69 and 67 mV/dec, which were much lower than HfO_2 film (85 mV/dec). This is due to the high quality interface properties of HfTaO gate dielectrics. The corresponding I_d-V_d characteristics for the films represented in **Fig. 2.19** (a) are shown in **Fig. 2.19** (b). The drain current of HfO_2 nMOSFETs was observably enhanced by incorporating Ta into HfO_2 at the same gate overdrive.

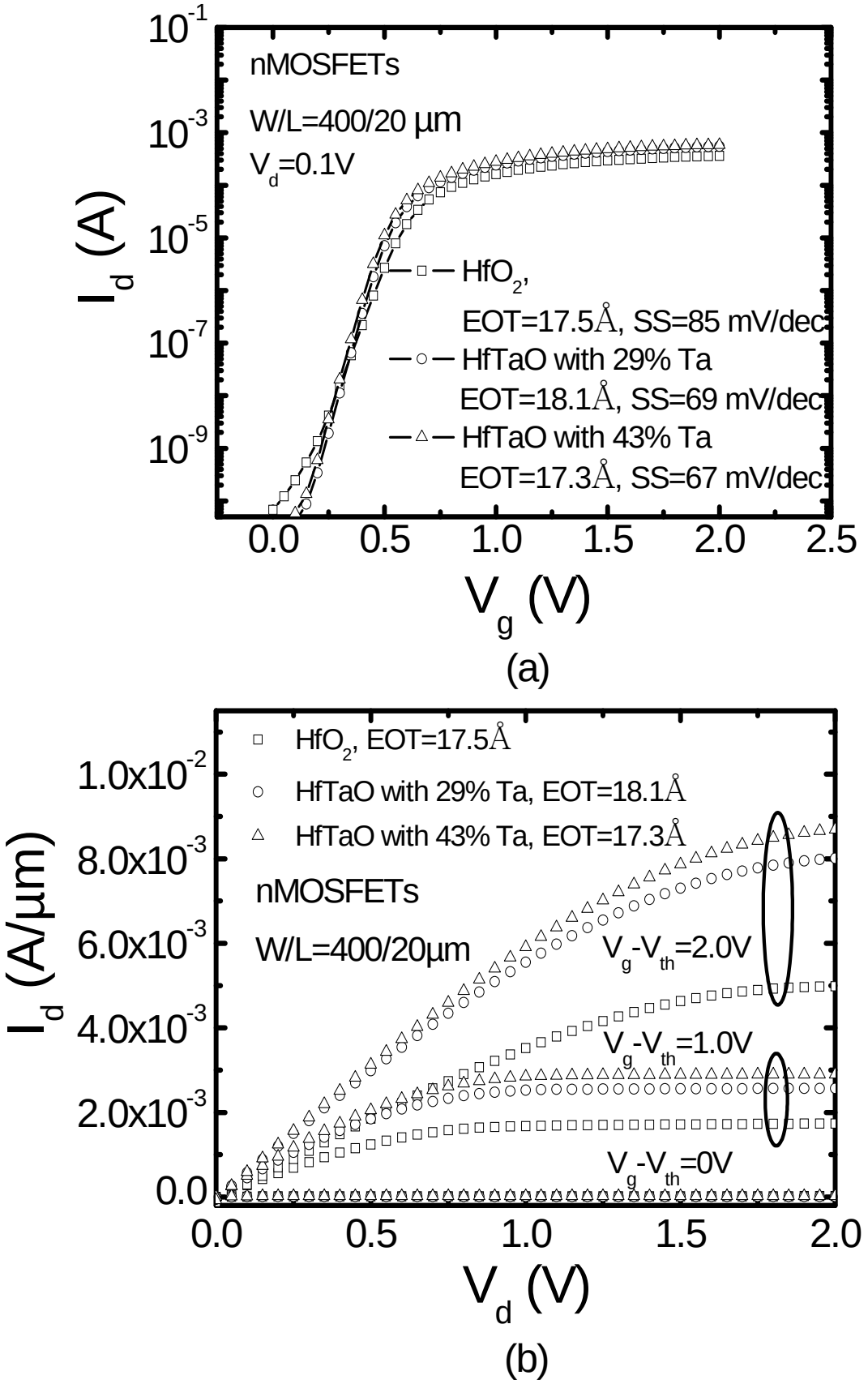


Fig. 2.19: (a) I_d-V_g and (b) I_d-V_d curves of nMOSFETs with HfO_2 and HfTaO gate dielectrics. HfTaO nMOSFETs show higher drain current and lower subthreshold swing compared to HfO_2.

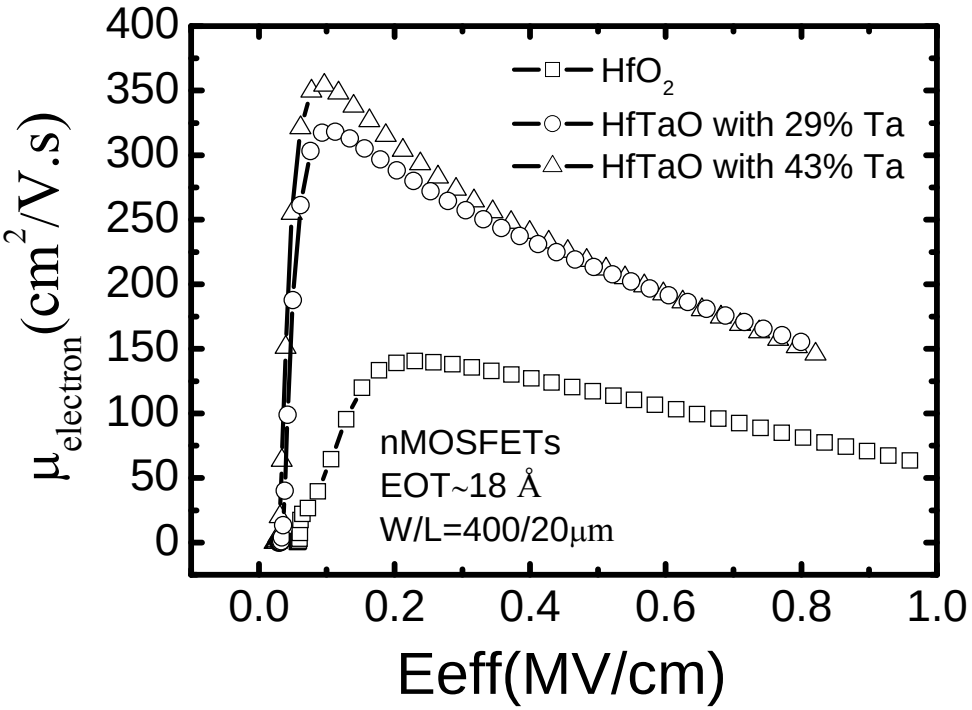


Fig. 2.20: Effective electron mobility of nMOSFETs with HfO_2 and HfTaO gate dielectrics extracted by split *C-V* method. HfTaO nMOSFETs show much higher electron mobility than that of HfO_2.

Fig. 2.20 depicts effective electron mobility ($\mu_{electron}$) for HfO_2 and HfTaO nMOSFETs after activation annealing at 950ºC for 30 sec. The electron mobility was extracted by standard split *C-V* method [31]. As can be seen, the peak electron mobility in HfO_2, HfTaO with 29% and 43% Ta nMOSFETs were 140, 318 and 354 cm^2/V-s respectively, and the mobility in nMOSFETs with HfO_2 gate dielectric was significantly increased by incorporating Ta. It has been reported that coulomb scattering due to interface trapped charge is the dominant mechanism of mobility degradation for HfO_2 gate dielectric MOSFETs at low-fields regime [32]. Also, the trapped charge in high-*k* bulk is a "minor" contribution to the mobility degradation [30]. Thereby, the improved mobility in HfTaO nMOSFETs is attributed to the lower interface state density and bulk traps in the HfTaO films compared to HfO_2, especially at low effective field region where coulomb scattering dominates mobility behavior.

2.3.5 Suppression of Boron Penetration in HfTaO Gate Dielectric

It is well known that the issue of boron penetration through the SiO_2 gate dielectric is a significant concern. The large gradient between the heavily doped poly-Si gate electrode, the undoped SiO_2 and lightly doped Si channel causes boron to diffuse rapidly through a ultra-thin SiO_2 upon thermal annealing, which results in a higher concentration of boron in the channel region. A change in channel doping then causes a shift in V_{fb} or V_{th}, which clearly alters the intended device properties in an unacceptable way, as discussed in **Chapter 1**. Moreover, grain boundaries in a crystallized high-*k* gate dielectric may be the fast paths for dopant diffusion (such as boron penetration) into the gate dielectric and even to the channel region in the silicon substrate, causing electrical instability and defect generation [4]. To increase the crystallization temperature of high-*k* material, or reduce the grain boundaries in high-*k* film has been demonstrated to be an effective approach for suppressing the boron penetration [33]. In this part, the boron penetration behavior in HfTaO gate dielectric will be discussed by examining the V_{fb} shift after high temperature annealing.

The device fabrication in this study was similar with that introduced in section 2.2. The nMOS and pMOS capacitors were fabricated on 6-inch Si (100) wafers with a resistivity of 10 ohm-cm. After standard pre-gate clean with diluted HF dipping, NH_3 interface treatment was performed by rapid thermal annealing (RTA) at 700ºC for 10 sec, in order to inhibit the formation of the low-*k* interfacial layer during deposition and high temperature annealing. The HfO_2 and HfTaO with 29% and 43% Ta films were deposited by reactive DC magnetron co-sputtering at room temperature, followed by post-deposition annealing (PDA) in N_2 ambient at 700ºC for 40sec to form high quality gate dielectrics. Low pressure chemical vapor deposition (LPCVD) amorphous-Si film with thickness of 200 nm was deposited as gate electrode. After gate patterning, phosphorous for nMOS capacitors was implanted at 50 KeV with a dose of 5×10^{15} cm^{-2}. Boron-implanted (Boron, 20 KeV, 5×10^{15} cm^{-2}) pMOS capacitors were used to investigate boron penetration behavior. Then gate dopant activation annealing was performed by RTA in N_2 ambient (850-1000^{o} C, 30 sec). Sintering was

done at 420° C in forming gas ambient for 30 min after Al metallization. Electrical characteristics of the MOS capacitors with an electrode area of 2.5×10^{-5} cm^2 were measured using HP4284A LCR meter and HP4156A. The *EOT* and V_{fb} were extracted by Quantum-Mechanical CV simulator program (published by UC Berkeley Device Group), taking into account the poly-Si depletion and quantum mechanical effects.

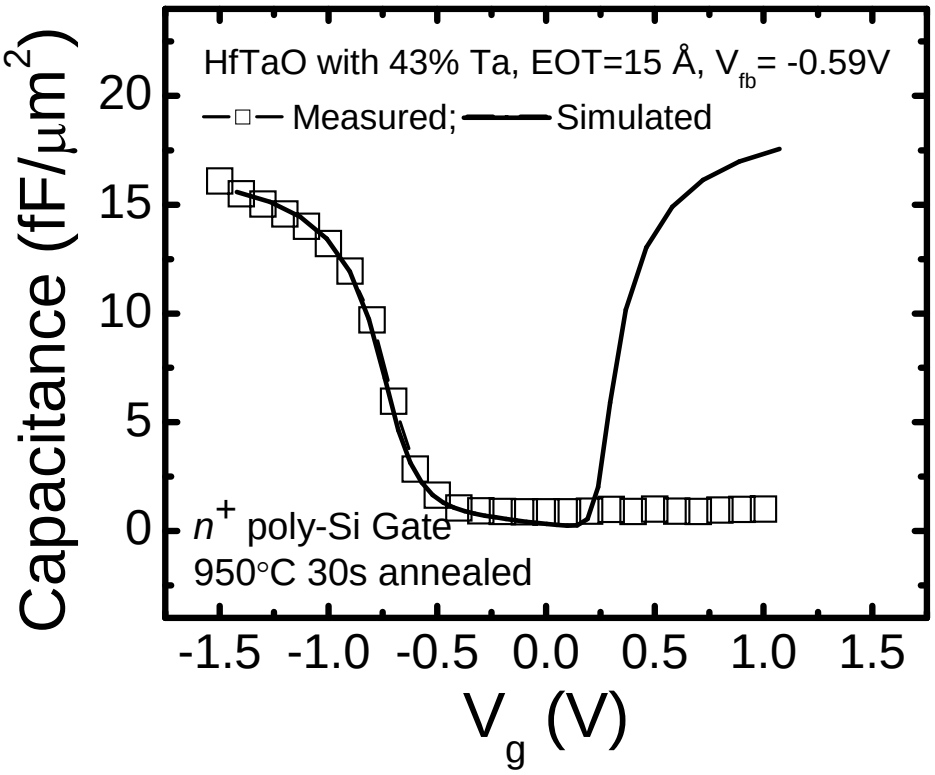


Fig. 2.21: *C-V* characteristic of 43% Ta HfTaO nMOS capacitor with poly-Si gate after activation annealing at 950° C for 30sec. The measurement was done at frequency of 1MHz and room temperature.

The *C-V* characteristic of n^+ poly-Si/HfTaO (43% Ta)/p-Si MOS capacitor with *EOT* of 15 Å is shown in **Fig. 2.21**. The simulated curve with poly-Si depletion and quantum mechanical corrections is indicated by solid symbols. As shown in this figure, the measured *C-V* curve fits well to the simulated curve, which indicates good interface property between HfTaO and Si substrate.

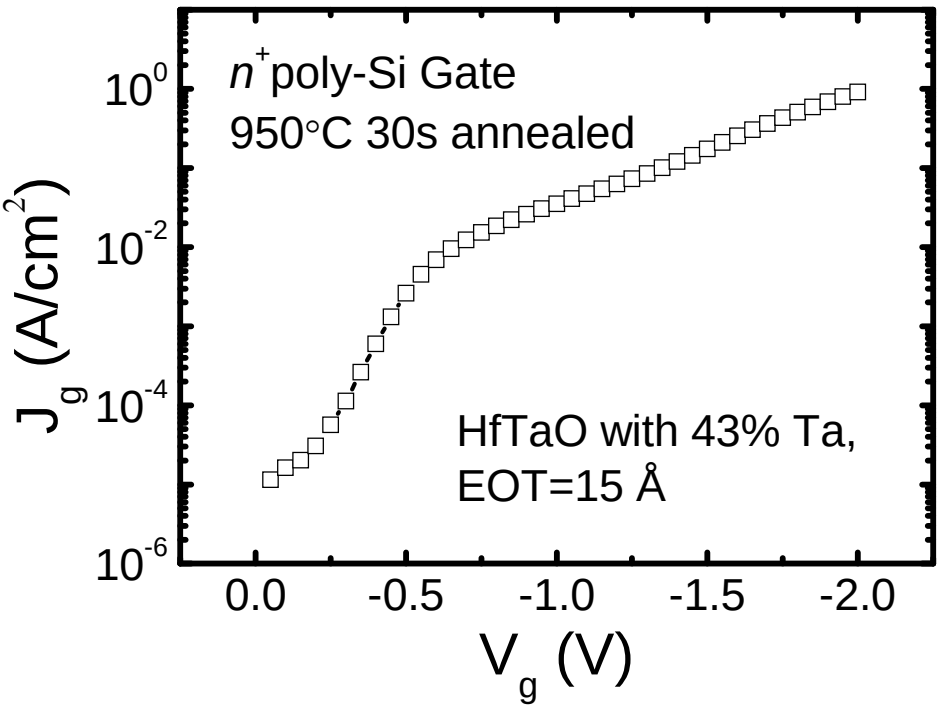


Fig. 2.22: *J-V* characteristic of HfTaO nMOS capacitor with poly-Si gate after activation annealing at 950^o C for 30 sec.

Fig. 2.22 shows the corresponding *J-V* curve for the sample illustrated in **Fig. 2.21**. Although the leakage current of poly-Si/HfTaO device was reduced by around two orders of magnitude compared to conventional poly-Si/SiO_2, it was much higher than that of TaN/HfTaO shown in **Fig. 2.7**. The possible reason will be discussed in **Chapter 4**. As shown in the **Fig. 2.22**, the leakage current curve exhibits two distinct regions, which reflects different conduction mechanisms at low and high bias regions. According to the simulation results, the leakage current is dominated by Frenkel-Poole emission at the low electric field region. At the high electric field region, it is believed that the leakage current is dominated by Fowler-Nordheim tunneling.

Boron from the *p*+ poly-Si gate electrode could easily diffuse not only through the thin gate dielectric, but also into the channel region during activation annealing. **Fig.2.23** shows the monitoring of flat band voltage shift as a function of activation

annealing condition in pMOS capacitors. The boron penetration induced flat band voltage shift in HfO_2 film was significantly suppressed by incorporating Ta. The negligible flat band voltage shift of HfTaO with 43% Ta film was observed up to 950° C annealing temperature. The excellent boron penetration immunity of 43% Ta HfTaO may be attributed to its amorphous structure, which remains after high temperature annealing in the device fabrication process.

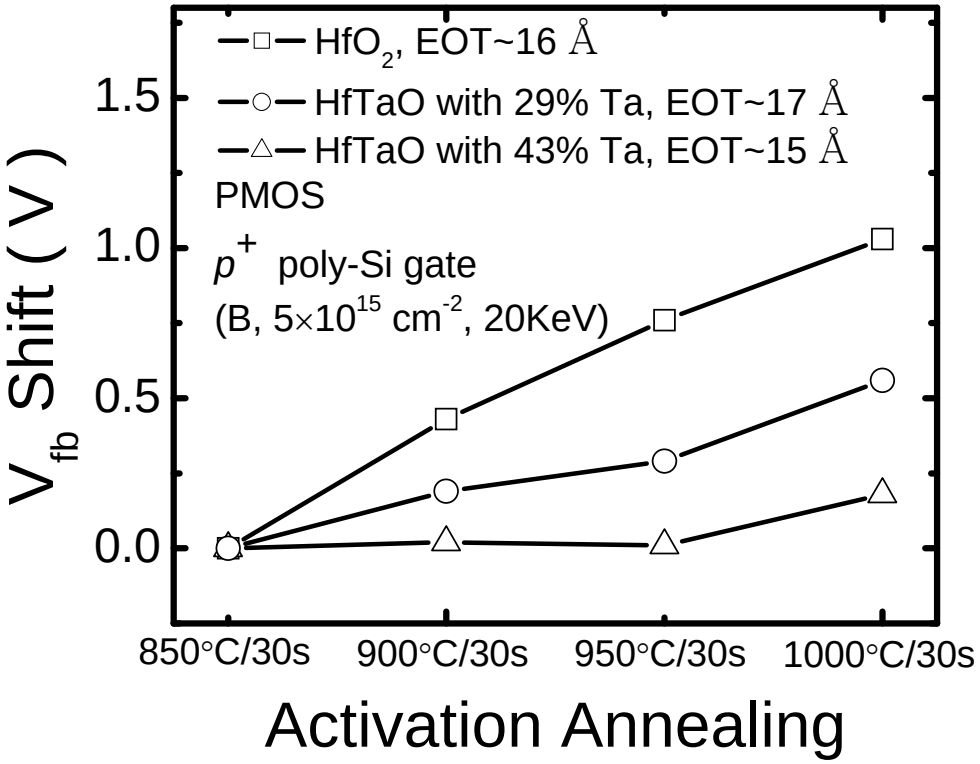


Fig. 2.23: Comparison of the V_{fb} shift in HfO_2 and HfTaO pMOS capacitors after various temperature annealing. HfTaO films show stronger immunity to boron penetration than HfO_2, due to its high crystallization temperature.

2.4 Conclusion

In summary, we proposed a novel Hf-based gate dielectric by examining the effects of Ta inclusion in HfO_2 on the thermal stability, leakage current, dielectric constant, interface properties, electrical stability and surface carrier mobility. Material studies indicated that the crystallization temperature of HfO_2 is significantly enhanced by incorporating Ta. This could be attributed to the breaking of the periodic crystal arrangement or the inhibition of continuous crystal growth in dielectric by adding Ta into HfO_2 film. It was also observed that the HfTaO film shows good thermal stability compared to HfO_2, which is believed to be due to the suppressed oxygen diffusion in the HfTaO film with high crystallization temperature. Moreover, the results of extensive electrical studies demonstrated that the interface state density (D_{it}) in HfO_2 film decreased significantly by incorporating Ta, and also the peak electron mobility in HfTaO MOSFETs is more than two times higher than that in HfO_2. The improvements on D_{it} and mobility observed in HfTaO may be mainly due to the formation of a high quality interfacial layer between HfTaO and Si substrate. It should be noted that the D_{it} and mobility in HfTaO are still incomparable with that in conventional SiO_2 gate dielectric. In addition, charge trapping induced threshold voltage (V_{th}) instability in HfO_2 and HfTaO films were examined by using static (DC) and pulsed I_d-V_g measurement techniques, and the V_{th} shift in HfTaO film was much lower than HfO_2. This indicates that electrical instability in HfO_2 film is significantly improved by incorporating Ta, and the HfTaO has significantly less bulk traps than HfO_2. This is possible due to the lack of crystallization in HfTaO films resulting in a significantly lower number traps compared to HfO_2. On the other hand, even though the leakage current of HfTaO film was higher than that of pure HfO_2 due to the lower band offset of Ta oxide, it is still comparable to the most high-*k* gate dielectrics, such as HfSiO, HfAlO, HfSiON, and HfAlON. This may be explained by that the HfTaO with higher dielectric constant provides a physically thicker film to reduce leakage current compared to those high-*k* gate dielectrics at the same *EOT*. The excellent properties observed in HfTaO gate dielectric suggest that it is a very promising

candidate as the alternative gate dielectric for future CMOS application.

An interesting phenomenon, which the crystallization temperature of HfTaO with 43% Ta film was higher than the two compositive materials of HfO_2 and Ta_2O_5, was reported in high-*k* materials for the first time. Moreover, the experimental results appear to confirm that the charge trapping induced V_{th} instability may be affected by the film morphology of high-*k* gate dielectric. Since the root causes of these two findings are not very clear yet, further work would be needed to identify the mechanisms involved in these phenomena. This might be helpful for further investigation of high-*k* gate dielectrics.

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Chapter 3

Advanced HfTaON/SiO_2 Gate Stack for Low Standby Power Application

3.1 Introduction

The industry's demand for greater integrated circuit functionality and performance at lower cost requires continuous scaling of device dimensions. This aggressive shrinking is driving the conventional SiO_2 or SiON gate dielectric to its physical limits due to excessive gate leakage current and reliability concerns. High dielectric constant (*k*) materials, as an alternative to SiO_2 or SiON gate dielectric, have been widely investigated by both academia and industry for the past few years, because of their potential in reducing equivalent oxide thickness (*EOT*) while maintaining low gate leakage current. Among various candidates of high-*k* materials, HfO_2 has been focused due to its suitable dielectric constant (22~25) [1], relatively wide band gap with sufficiently high band offset [2], and acceptable thermal stability in contact with Si [3]. Although the HfO_2 gate dielectric provides much lower gate leakage current compared to conventional SiO_2 at a same *EOT*, serious mobility degradation can be observed in HfO_2 devices whatever with poly-Si [4] or metal [5] gate. On the other hand, HfO_2 crystallizes at temperature around 500 ºC. Grain boundaries in the fully or partially crystallized HfO_2 film may act as the fast paths for diffusion of oxygen or dopants into gate dielectric and even channel region in silicon substrate, causing undesirable growth of interfacial layer (IL), electrical instability,

and defects generation [6]. The limitations discussed above constrain the application of HfO_2 as gate dielectric for advanced CMOS technology.

Recently, Hf-silicates (HfSiO and HfSiON) have been highlighted for the gate dielectric application because of its high crystallization temperature, good thermal stability in direct contact with Si, excellent boron penetration immunity and good reliability [7-11]. Unfortunately, compared to most high-*k* materials, the Hf-silicates show lower *k* values due to the incorporation of SiO_2 (*k*=3.9). For example, it has been reported that the optimized HfSiON showed excellent performance whereas its *k* value decreases to 10 [12]. On the other hand, even though the channel mobility in Hf-silicates is higher than those in most high-*k* gate dielectrics (HfO_2, HfON, HfAlO, and HfAlON etc.), it is still incomparable with that in current SiO_2 or SiON gate dielectric. To suppress the mobility degradation in Hf-silicates, two major approaches have been proposed: (1) insertion of an ultra-thin SiO_2 IL between Hf-silicates and Si substrate [13, 14] or (2) formation of a SiO_2-like IL by interface engineering (such as plasma oxidation or post deposition treatment in oxygen ambient) [15, 16]. By using the two approaches, the channel mobility in Hf-silicates can be comparable with that in SiO_2 or SiON. However, the disadvantage of low *k* value in Hf-silicates is seriously magnified due to the inserted SiO_2 or SiO_2-like IL with even lower *k*, which may compromise the benefits of Hf-silicates and limit the continuous scaling of the gate dielectric thickness. Consequently, it is possible to speculate that a bulk dielectric with sufficiently high *k* value and an ultra-thin SiO_2 IL are preferred as gate stack for advanced CMOS application.

As discussed in **Chapter 2**, a novel HfTaO material was developed as an alternative high-*k* gate dielectric. The HfTaO shows high crystallization temperature up to 1000ºC, good thermal stability, acceptable gate leakage current, good interface properties, excellent electrical stability, and improved carrier mobility, moreover, the HfTaO provides high dielectric constant. As a promising high-*k* candidate, the HfTaO has potential to integrate with an ultra-thin SiO_2 interfacial layer for advanced CMOS application.

In this study, electrical characteristics of a novel HfTaON/SiO_2 gate stack,

which consists of a HfTaON film with *k* value of ~23 and a 10-Å SiO_2 IL, have been investigated for advanced CMOS application. The gate stack of HfON/SiO_2 as the control sample was also fabricated and characterized. Both HfTaON/SiO_2 and HfON/SiO_2 gate stacks provided much lower gate leakage current compared to SiO_2, good interface properties, excellent transistor characteristics and superior carrier mobility. In addition, compared to the HfON/SiO_2, improved thermal stability was observed in the HfTaON/SiO_2 gate stack. On the other hand, the charge trapping induced threshold voltage (V_{th}) instability was examined for the HfTaON/SiO_2 and HfON/SiO_2 gate stacks. The HfTaON/SiO_2 gate stack exhibited significant suppression of the V_{th} instability compared to the HfON/SiO_2, in particular for nMOSFETs. The excellent characteristics observed in HfTaON/SiO_2 gate stack suggest that it is a very promising to replace the conventional SiO_2 or SiON as gate dielectric for advanced CMOS application, especially for the low standby power application.

3.2 Experiments

The devices were fabricated on 6-inch Si substrates (1-10 Ω-cm) using the conventional self-aligned MOSFET process. After standard pre-gate clean with diluted HF dipping, 10-Å SiO_2 was grown on the Si substrates as IL by rapid thermal oxidation (RTO) at 1000ºC. HfON and HfTaON films with thickness of ~25 Å were then deposited onto the SiO_2 IL by reactive DC co-sputtering of Hf and Ta targets in Ar/N_2/O_2 ambient, and followed by post deposition annealing (PDA) in N_2 with 5% O_2 ambient at 700ºC for 30 sec. The compositions of PDA annealed HfON and HfTaON films, specified as N/(N+O)=20% and Ta/(Hf+Ta)=25%, were examined by X-ray photoelectron spectroscopy (XPS). TaN metal with thickness of 1500 Å was deposited as gate electrode by reactive DC sputtering, and patterned by dry etch using Cl_2 etching gas. After gate patterning, As and BF_2 (energy of 70 KeV and 35 KeV, respectively) were implanted with a dose of 1×10^{15} cm^{-2}. The post metal annealing (PMA) at 1000 ºC for 10 sec was performed to activate source/drain. To examine

thermal stability of the gate stacks, some MOS capacitors were also annealed by different PMA conditions (no PMA, 900ºC/30s, 950ºC/30s and 1000ºC/10s). Finally, the samples were annealed at 420ºC in forming gas for 30 min after Al metallization.

Electrical characteristics were evaluated using HP4156A precision semiconductor parameter analyzer and HP4284A precision LCR meter. *C-V* curves were measured at 100 KHz, *EOT* and flat-band voltage (V_{fb}) were determined using Quantum-Mechanical *CV* simulator program (published by UC Berkeley Device Group), taking into account the quantum mechanical effects. Charge pumping current measurement was extensively used to evaluate the interface state density (D_{it}), and the carrier mobility was calculated using the standard split *C-V* method on transistors with W/L ratio of 400μm/20μm.

3.3 Results and Discussion

3.3.1 Physical Characteristics of HfTaON/SiO_2 Gate Stack

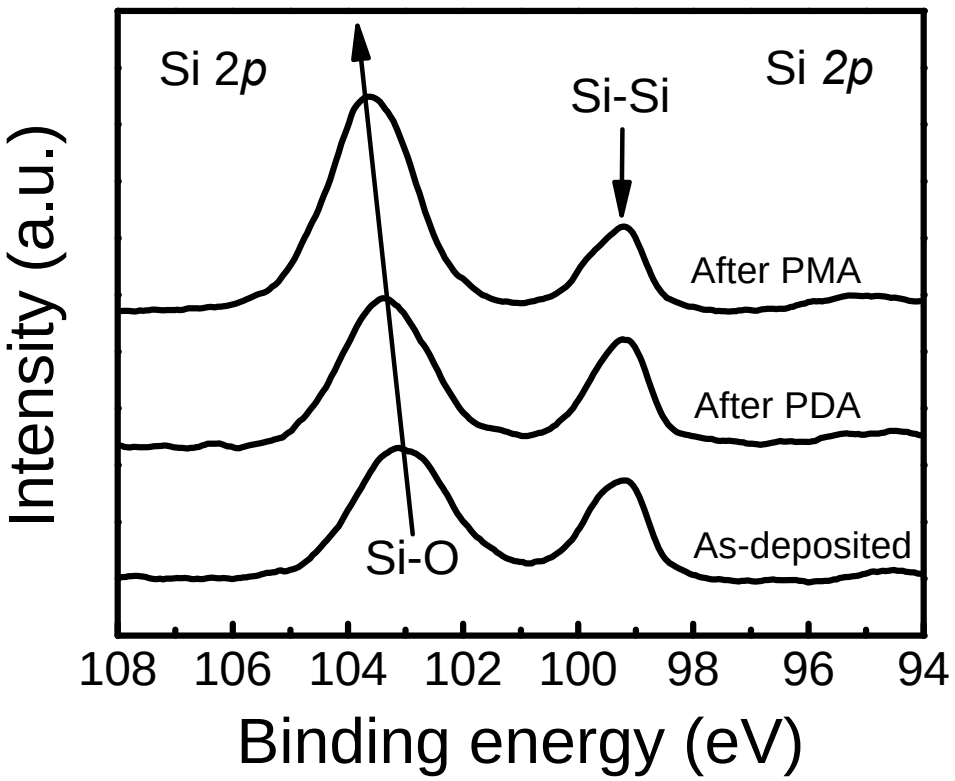
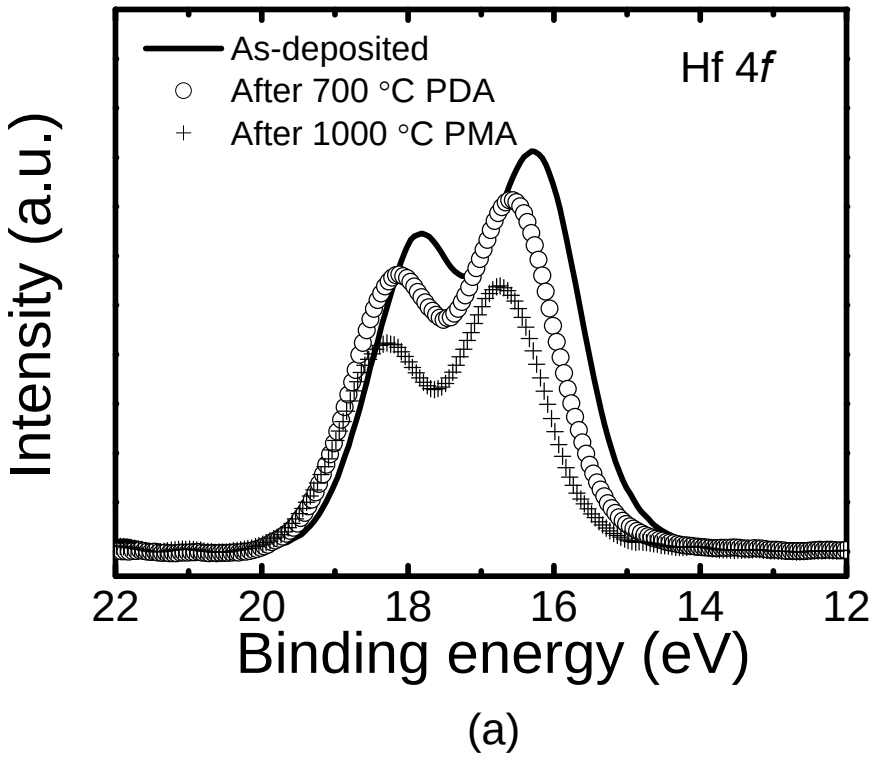


Fig. 3.1: Si 2*p* XPS spectra for as-deposited, 700ºC PDA and 1000ºC PMA annealed HfTaON/SiO_2 films. The Si-O peak slightly shifts to higher position and the intensity is increased with annealing temperature.



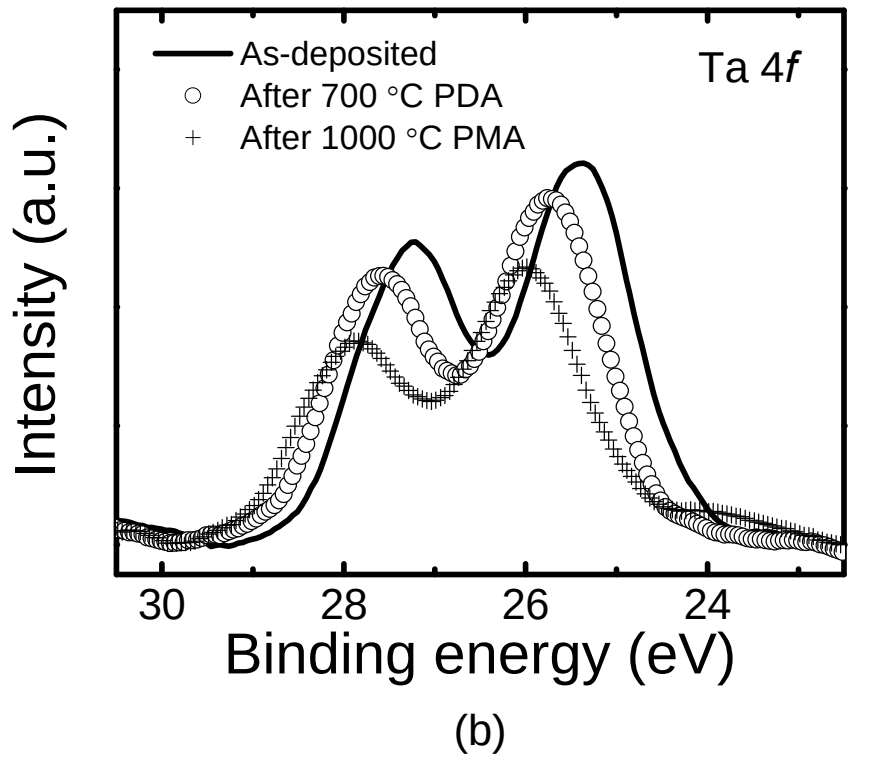


Fig. 3.2: XPS peaks of (a) Hf 4*f* and (b) Ta 4*f* for as-deposited, 700ºC PDA and 1000ºC PMA annealed HfTaON/SiO_2 gate stack. It is notable that both Hf and Ta peaks move towards higher binding energy, and the intensity of the peaks are decreased with annealing temperature. No evidence of Hf-Si and Ta-Si bonds formation are observed in high temperature annealed films.

Fig. 3.1 shows the Si *2p* XPS spectra for as-deposited, 700ºC PDA and 1000ºC PMA annealed HfTaON/SiO_2 films. It was found that the binding energy of Si-O peak slightly shifts to higher energy position, and the intensity of the peak is increased with annealing temperature. This suggests that the thickness of SiO_2 IL may slightly increase with annealing temperature. Comparison of Hf *4f* and Ta *4f* XPS spectra for HfTaON/SiO_2 film with or without PDA and PMA are shown in **Fig. 3.2** (a) and (b). It was noted that both Hf and Ta peaks move towards higher binding energy, and the intensity of the peaks decrease after annealing. These XPS results indicate that Hf and Ta silicates may be formed between the HfTaON and SiO_2 after annealing [17, 18]. This is consistent with previous report in which the high-*k* film in direct contact with SiO_2 is unstable during high temperature annealing because of the spontaneous formation of silicates [19].

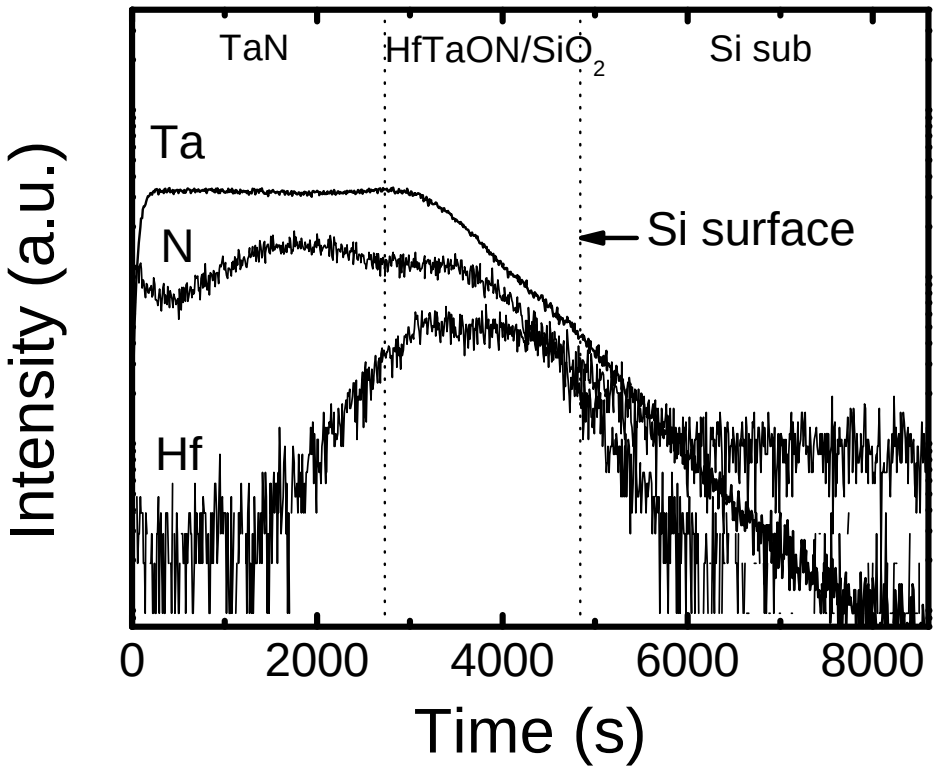


Fig. 3.3: SIMS profiles of Hf, Ta and N in HfTaON/SiO_2 film after annealing at 1000ºC. The Hf, Ta, and N atoms mainly distribute away from Si surface.

Fig. 3.3 shows SIMS profiles of Hf, Ta and N in HfTaON/SiO_2 film after

annealing at 1000ºC. It was observed that the Hf, Ta, and N atoms mainly distribute away from Si surface. It is commonly believed that the high-*k* and N in direct contact with Si surface may degrade the interface properties. By inserting the SiO_2 between HfTaON and Si substrate as a buffer layer, it may suppress the diffusion of Hf, Ta and N to Si surface, and also improve the interface properties.

The high-resolution TEM micrographs of (a) HfON/SiO_2 and (b) HfTaON/SiO_2 films, after PMA at 1000^{o}C for 10sec, are shown in **Fig. 3.4**. The noticeable difference between the HfON/SiO_2 and HfTaON/SiO_2 samples was that the HfON film is partially crystallized whereas the HfTaON film remains amorphous structure after the annealing at 1000^{o}C. There have been several reports on incorporating N into high-*k* film to increase crystallization temperature [20, 21]. Although the crystallization temperature of HfO_2 (~500ºC) may be increased by several hundred degrees due to the incorporation of N, the HfON film still became

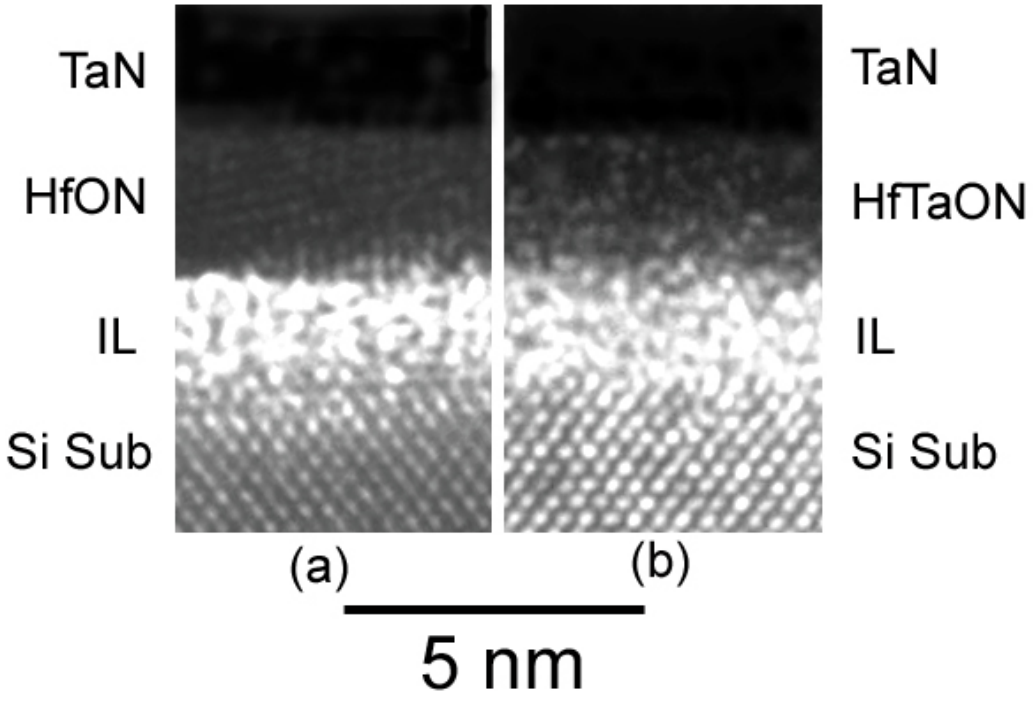


Fig. 3.4: TEM micrographs of (a) HfON/SiO_2 and (b) HfTaON/SiO_2 gate stack after PMA at 1000ºC for 10 sec. The HfON film is partially crystallized and the HfTaON remains amorphous structure.

crystallized after the annealing at 1000°C. On the other hand, the crystallization temperature of HfO_2 can be significantly enhanced by adding Ta as discussed in **Chapter 2**, and further increased by incorporation of N. This may explain the finding of HfTaON with amorphous structure after the annealing at 1000°C. In addition, as discussed in **Chapter 2**, although the incorporation of Ta into HfO_2 has made notable gains in performance enhancement, the high Ta composition in HfO_2 may degrade the gate leakage current. Hence, the Ta composition in HfO_2 was optimized and the HfTaON with 25% Ta was chosen in this study. In **Fig. 3.4**, it was also noted that the physical thicknesses of IL in both HfON/SiO_2 and HfTaON/SiO_2 samples are thicker than that of prior 10-Å SiO_2. Based on the XPS results shown in **Fig. 3.1** and **3.2**, it is believed that the increase in IL thickness is due to the interaction (formation of silicates) between the high-*k* films (HfON and HfTaON) and 10-Å SiO_2 during the high temperature annealing.

To examine the impact of the interaction between HfTaON and SiO_2 during high temperature annealing, the TEM pictures of HfTaON/SiO_2 gate stacks (a) without and (b) with the PMA at 1000°C for 10sec, and also (c) the corresponding *C-V* characteristics are shown in **Fig. 3.5**. It was found that the IL thickness in HfTaON/SiO_2 gate stack without the PMA was 10.3 Å shown in **Fig. 3.5** (a). Since the pre-grown SiO_2 IL was around 10 Å and the interaction between the HfTaON and SiO_2 IL may be neglected in the case of the HfTaON/SiO_2 gate stack without the high temperature PMA, it is possible to assume that the 10.3-Å IL shown in **Fig. 3.5** (a) is pure SiO_2. Considering the *EOT* of 14.8 Å (**Fig. 3.5** (c)) and the physical thickness of 26.6 Å (**Fig. 3.5** (a)) for the HfTaON film without PMA, it was calculated that the *k* value of the HfTaON film is around 23, which is similar to the reported *k* value of pure HfO_2 [1]. After performing the PMA at 1000ºC for 10 sec, the accumulation capacitance for HfTaON/SiO_2 gate stack decreased observably (**Fig. 3.5** (c)), and the corresponding *EOT* increased from 14.8 Å to 17.7 Å. This is due to the increase in the IL thickness after the PMA, which is confirmed by the observation in the TEM picture (**Fig. 3.5** (b)).

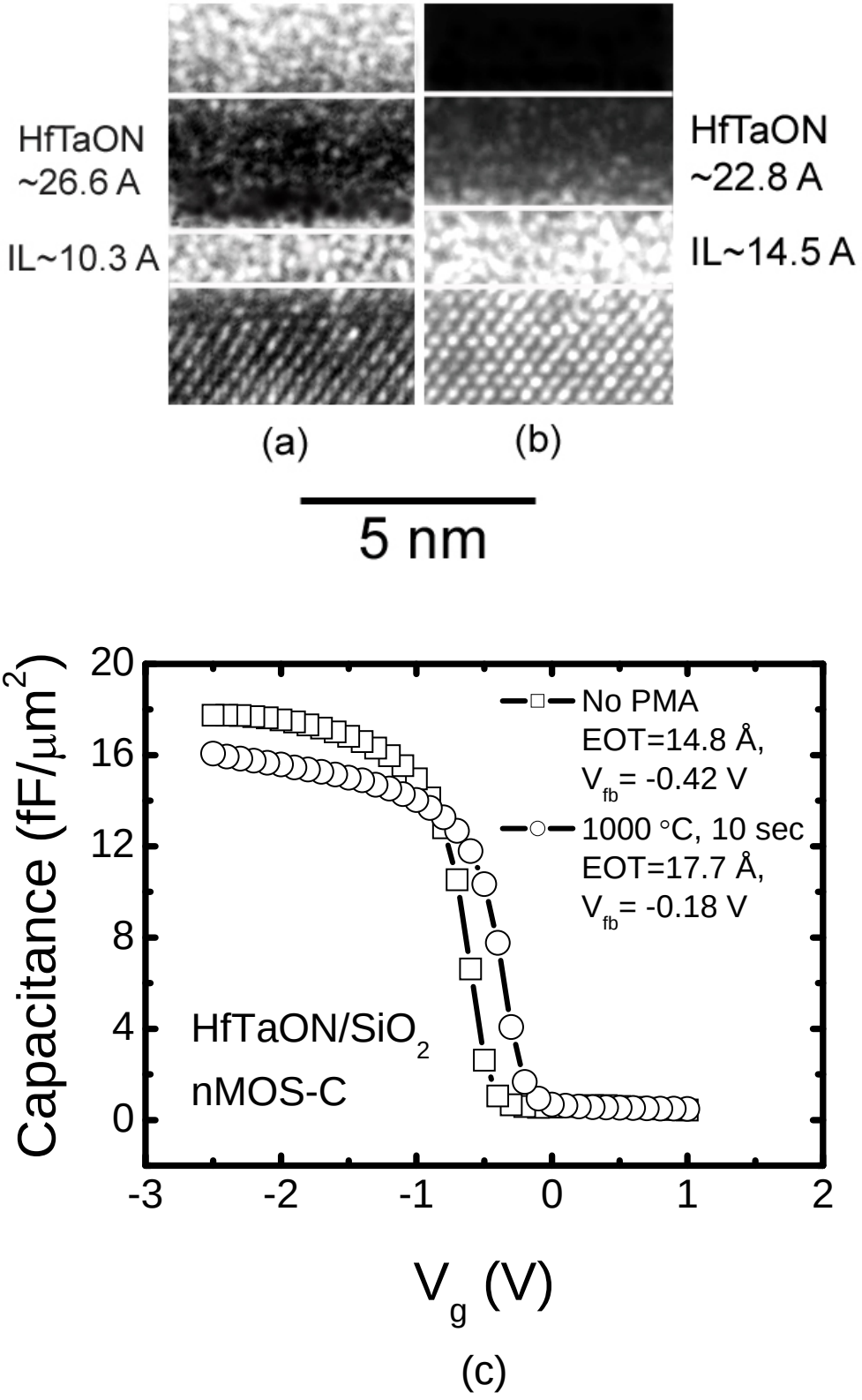


Fig. 3.5: TEM pictures of HfTaON/SiO_2 gate stack (a) without and (b) with PMA at 1000ºC for 10 sec. (c) corresponding *C-V* curves of HfTaON/SiO_2 nMOS capacitors without and with PMA at 1000ºC for 10 sec.

3.3.2 Thermal Stability of HfTaON/SiO₂ Gate Stack

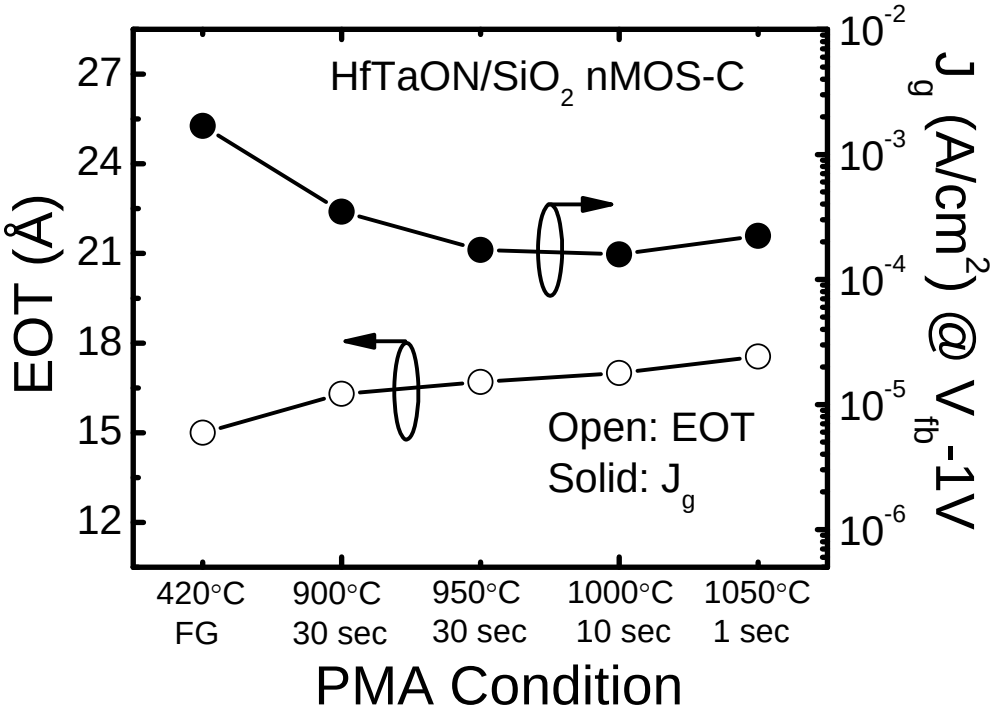


Fig. 3.6: *EOT* and gate leakage current as a function of the PMA condition. The increase in *EOT* with PMA temperature from 420ºC to 1050ºC is less than 3 Å for HfTaON/SiO_2. The gate leakage current decreases slightly with the PMA temperature, which is mainly due to the increase in *EOT*.

Some MOS capacitors were also annealed by different PMA conditions to evaluate thermal stability of the HfTaON/SiO_2 gate stack. In **Fig. 3.6,** the thermal stability of the gate stack was examined by comparing the variation of *EOT* and leakage current after different PMA. By incorporating N into HfTaO and inserting the SiO_2 interfacial layer, the good thermal stability in HfTaON/SiO_2 film was observed. **Fig. 3.7** compares the increase in *EOT* (ΔEOT) for HfON/SiO_2 and HfTaON/SiO_2 after activation annealing ($T \geq 900$ºC). The results of HfO_2 and HfTaO (presented in **Chapter 2**) are also included for comparison. It was clearly observed that the *EOT* increases with PMA temperature in all samples, and the ΔEOT is obviously suppressed by inserting SiO_2 IL and incorporating N in both HfO_2 and HfTaO films. It was also noted that the HfTaON/SiO_2 provides the smallest ΔEOT in **Fig. 3.7**, which

indicates that the HfTaON/SiO_2 gate stack shows the best thermal stability among those samples. This can be attributed to the HfTaON films with amorphous structure and the insertion of the SiO_2 IL, which may effectively suppress oxygen diffusion through the gate stack and the increase in IL thickness.

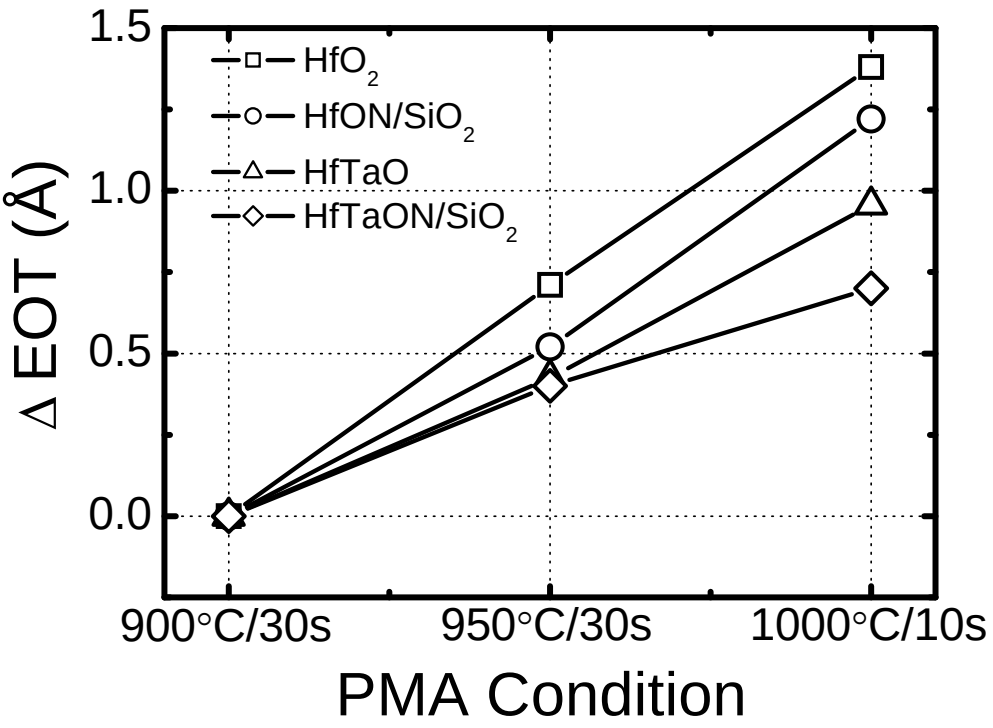


Fig. 3.7: The increase in *EOT* as a function of PMA conditions for HfO_2, HfON/SiO_2, HfTaO and HfTaON/SiO_2 gate stacks. The HfTaON/SiO_2 exhibits the lowest increase in EOT compare to other gate stacks, which indicates that the HfTaON/SiO_2 shows the best thermal stability among those gate stacks.

3.3.3 *C-V* and *J-V* of HfTaON/SiO_2 Gate Stack and Interface Properties

Fig. 3.8 shows typical *C-V* curves of (a) nMOSFETs and (b) pMOSFETs with HfON/SiO_2 and HfTaON/SiO_2 gate stacks after PMA at 1000ºC for 10 sec. The HfON/SiO_2 and HfTaON/SiO_2 gate stacks exhibited similar flat band voltage (V_{fb}), indicating that negligible fixed charges were introduced by adding Ta. It was also found that the *EOT* of the gate stack extracted in transistors are 1~2 Å higher than that

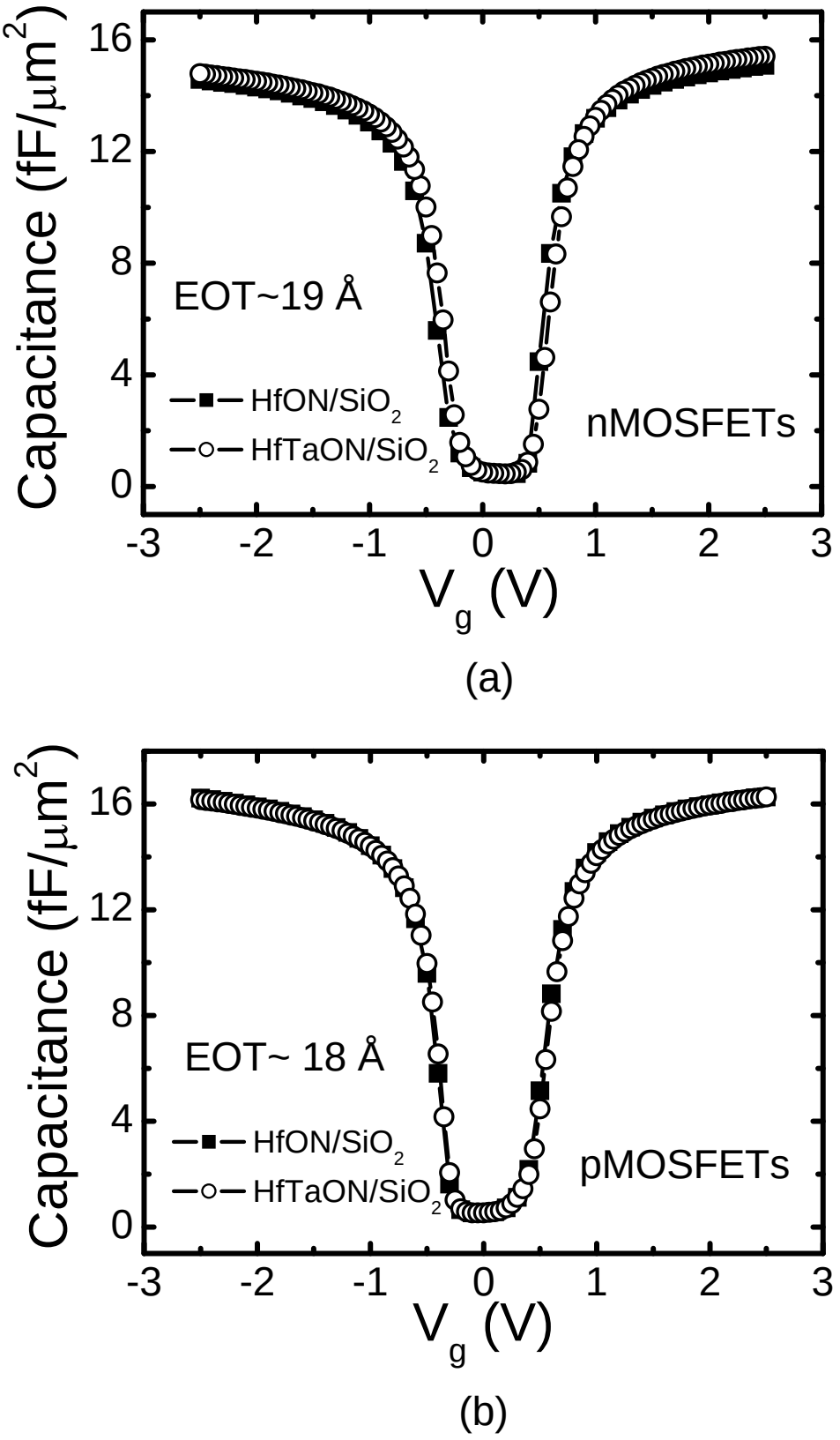


Fig. 3.8: Typical *C-V* characteristics of (a) nMOSFETs and (b) pMOSFETs with HfON/SiO$_2$ and HfTaON/SiO$_2$ gate stacks. The HfON/SiO$_2$ and HfTaON/SiO$_2$ gate stacks show similar flat band voltage.

in capacitors (**Fig. 3.5** (c)), even though the gate dielectrics and process conditions were totally same for both devices. The reason of the increased *EOT* in transistors is not clear yet.

Fig. 3.9 compares the leakage currents of (a) nMOSFETs and (b) pMOSFETs with HfON/SiO_2 and HfTaON/SiO_2 gate stacks as a function of *EOT*. The leakage currents of HfTaON/SiO_2 gate stack were higher than those of HfON/SiO_2 for nMOSFETs, whereas the HfTaON/SiO_2 exhibited similar leakage currents with the HfON/SiO_2 for pMOSFETs. This is due to the fact that Ta oxide has a lower conduction band offset (ΔE_C) and similar valance band offset (ΔE_V) compared to Hf oxide [22]. As shown in **Fig. 3.9** (a) and (b), the leakage currents of HfON/SiO_2 and HfTaON/SiO_2 gate stacks were much lower than those of conventional poly-Si/SiO_2 [23] for both nMOS and pMOSFETs.

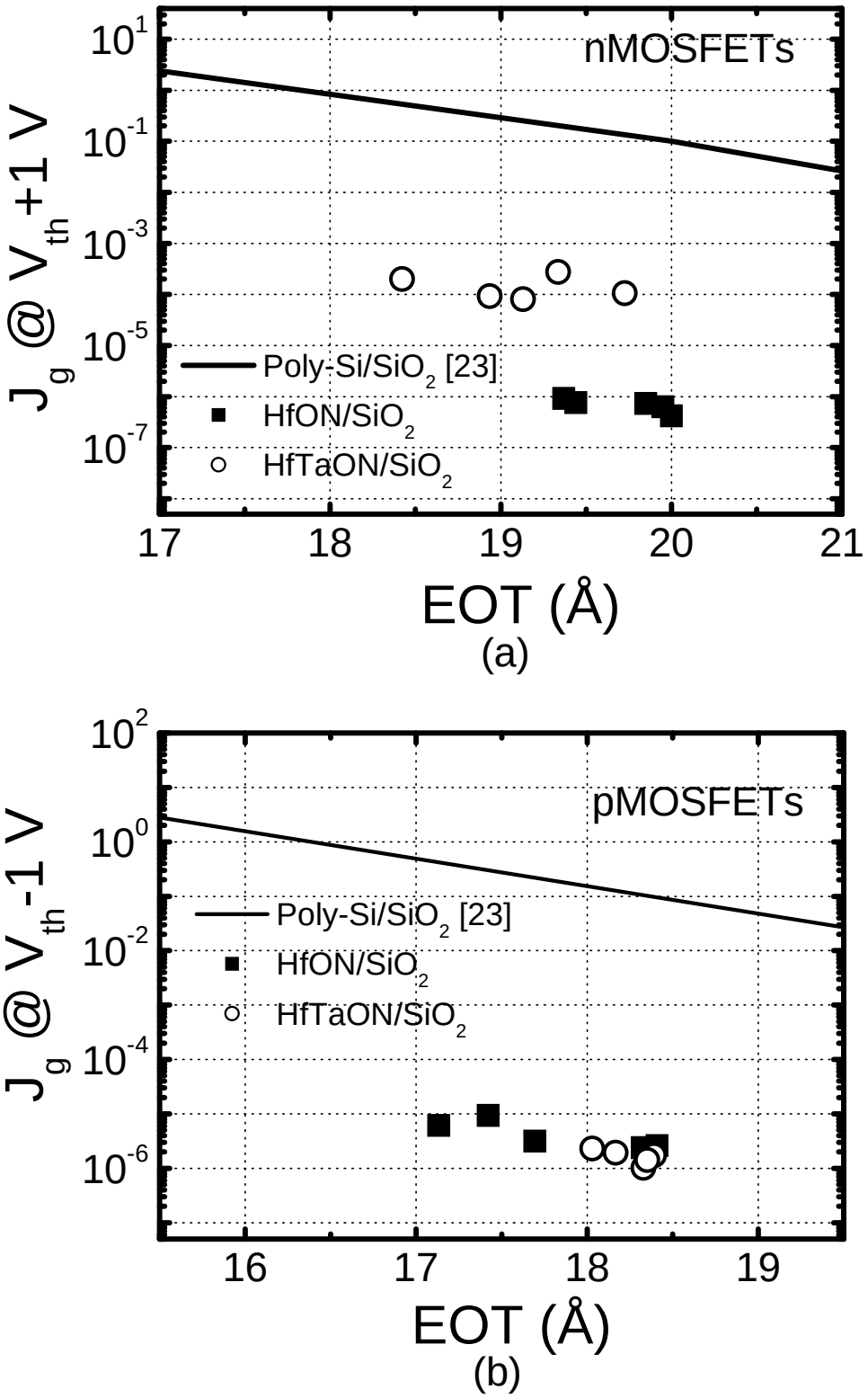


Fig. 3.9: *EOT* dependences of gate leakage currents at V_g=V_{th} ± 1V for (a) nMOSFETs and (b) pMOSFETs with HfON/SiO_2 and HfTaON/SiO_2 gate stacks, respectively. The gate leakage currents of HfTaON/SiO_2 are higher than HfON/SiO_2 in nMOSFETs, whereas similar with HfON/SiO_2 in pMOSFETs.

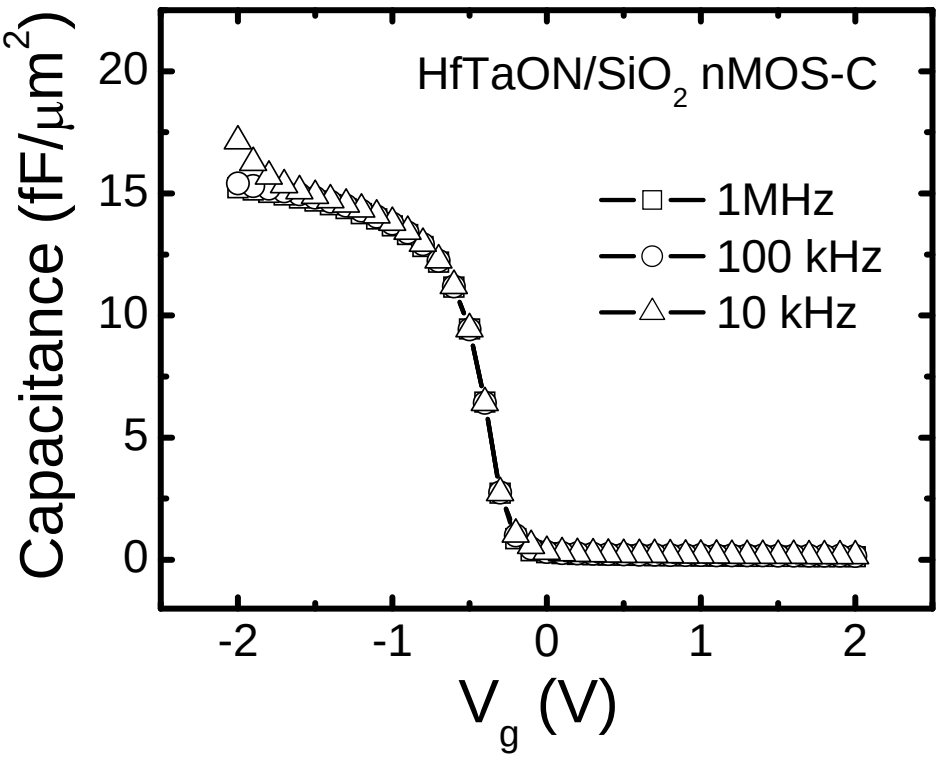


Fig. 3.10: HfTaON/SiO_2 nMOS capacitor shows negligible frequency dispersion at frequency range from 10 kHz to 1 MHz.

Negligible frequency dispersion in HfTaON/SiO_2 nMOS-C from 10 kHz to 1 MHz is shown in **Fig. 3.10**, which indicates that the interface traps cannot respond at high frequency. Almost no hysteresis was observed in HfTaON/SiO_2 films after sweeping between 3V to -3V (**Fig. 3.11**).

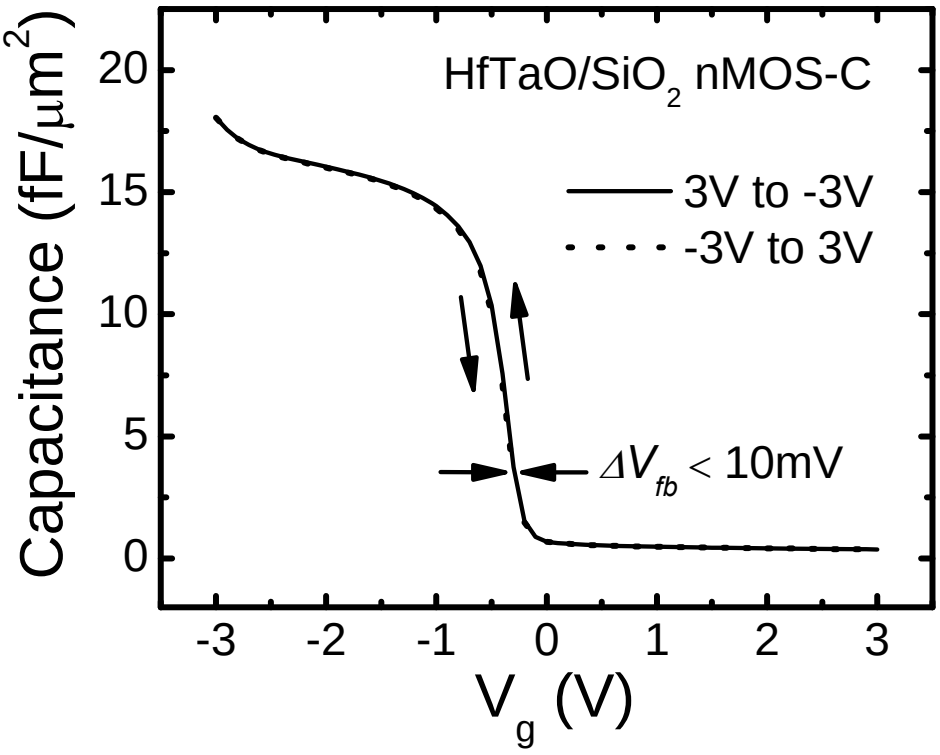


Fig. 3.11: Almost no *C-V* hysterisis for nMOS capacitor with HfTaON/SiO_2 gate stack after sweeping between 3 V and -3 V.

The interface state density (D_{it}) in nMOSFETs with HfON/SiO_2 and HfTaON/SiO_2 gate stacks, which were quantitatively evaluated by a standard two-level and constant amplitude charge pumping method, are compared in **Fig. 3.12**. For comparison, the D_{it} in nMOSFETs with 35-Å-thick SiO_2, HfO_2 and HfTaO (presented in **Chapter 2**) are also included. The calculated D_{it} were 9.7×10^{9} cm^{-2} in SiO_2, 2.8×10^{12} cm^{-2} in HfO_2, 5.1×10^{11} cm^{-2} in HfTaO with 29% Ta, 3×10^{10} cm^{-2} in HfON/SiO_2 and 2.8×10^{10} cm^{-2} in HfTaON/SiO_2, respectively. It was noted that the D_{it} were significantly reduced by inserting SiO_2 IL for both HfON/SiO_2 and HfTaON/SiO_2 cases. Also, the HfON/SiO_2 and HfTaON/SiO_2 gate stacks exhibited similar D_{it}, although the HfO_2 without the SiO_2 IL showed much higher D_{it} compared to that HfTaO. These suggest that the insertion of the SiO_2 IL is the key point to improve the interface properties in high-*k* gate stacks. On the other hand, the D_{it} in HfON/SiO_2 and HfTaON/SiO_2 were slightly higher than that in pure SiO_2, which

could be due to the slight diffusion of N, Hf or Ta through the SiO_2 IL and then degradation of the interface properties during high temperature annealing.

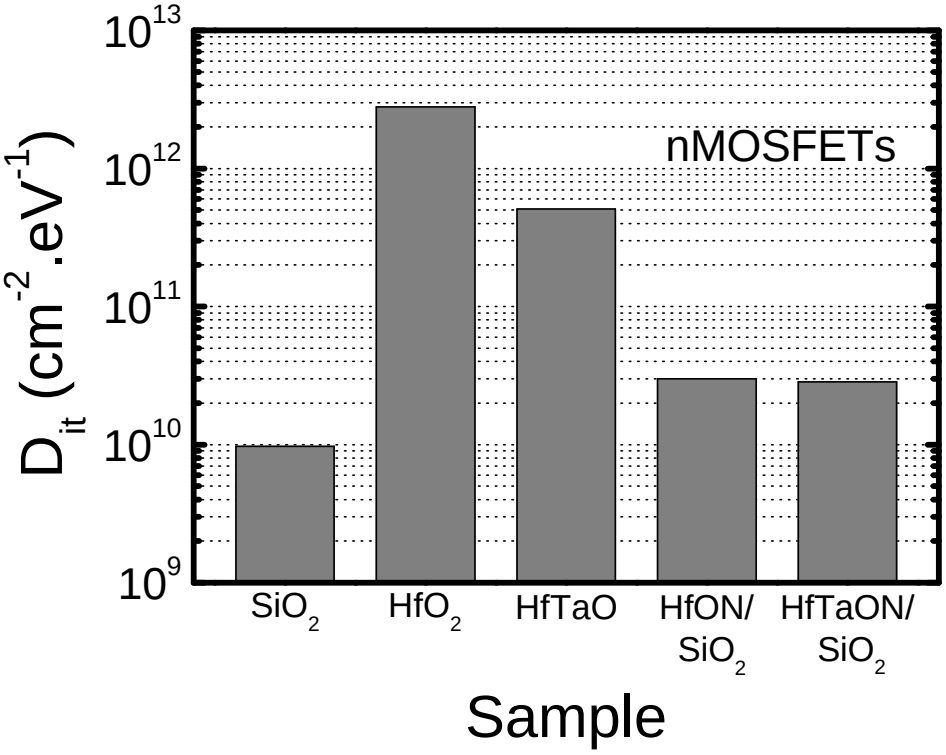


Fig. 3.12: Comparison of D_{it} at the midgap for nMOSFETs with SiO_2, HfO_2, HfTaO, HfON/SiO_2 and HfTaON/SiO_2 gate stacks. The HfON/SiO_2 and HfTaON/SiO_2 gate stacks show similar D_{it}, however, they are still slightly higher than that in SiO_2.

3.3.4 Transistor Characteristics of HfTaON/SiO$_2$ Gate Stack

Fig. 3.13 shows I_d-V_g characteristics of MOSFETs with HfON/SiO_2 and HfTaON/SiO_2 gate stacks after PMA at 1000ºC for 10 sec. As can be seen, both HfON/SiO_2 and HfTaON/SiO_2 exhibited excellent subthreshold swing. This can be explained by the good interface properties observed in the HfON/SiO_2 and HfTaON/SiO_2 gate stacks. Moreover, the result of similar V_{th} shown in HfON/SiO_2 and HfTaON/SiO_2 MOSFETs confirms that the negligible fixed charges are induced by the incorporation of Ta. The corresponding I_d-V_d characteristics for the HfON/SiO_2

and HfTaON/SiO_2 films are shown in **Fig. 3.14**. Both HfON/SiO_2 and HfTaON/SiO_2 MOSFETs provided similar drain currents at the same gate overdrive.

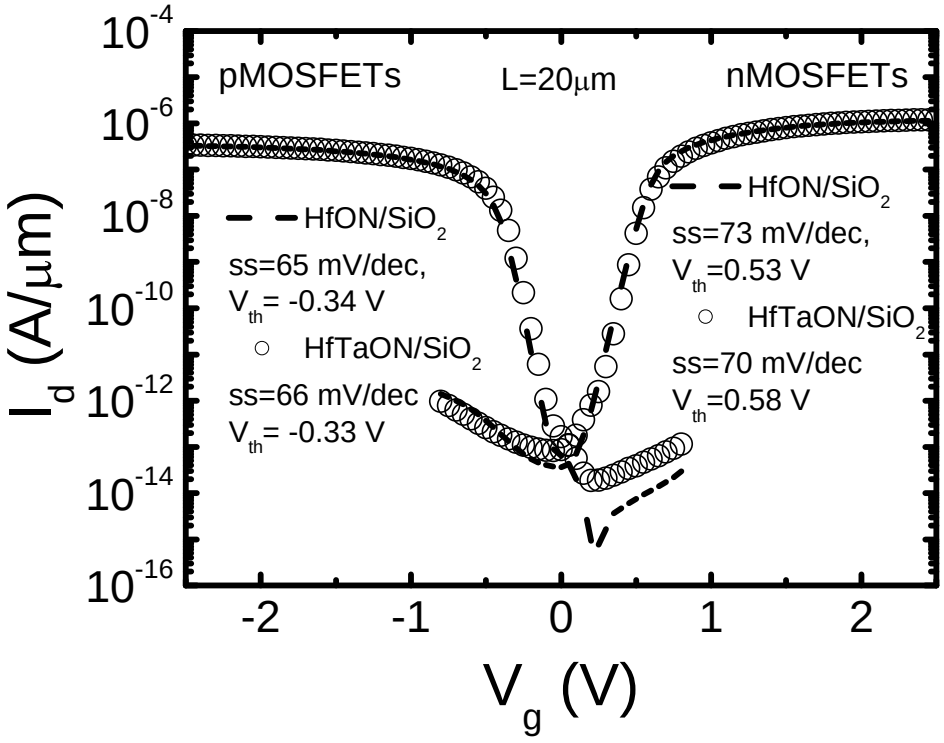


Fig. 3.13: I_d-V_g curves for MOSFETs with HfON/SiO_2 and HfTaON/SiO_2 gate stacks. The HfON/SiO_2 and HfTaON/SiO_2 gate stacks show similar threshold voltages and sub-threshold swings for both nMOS and pMOSFETs.

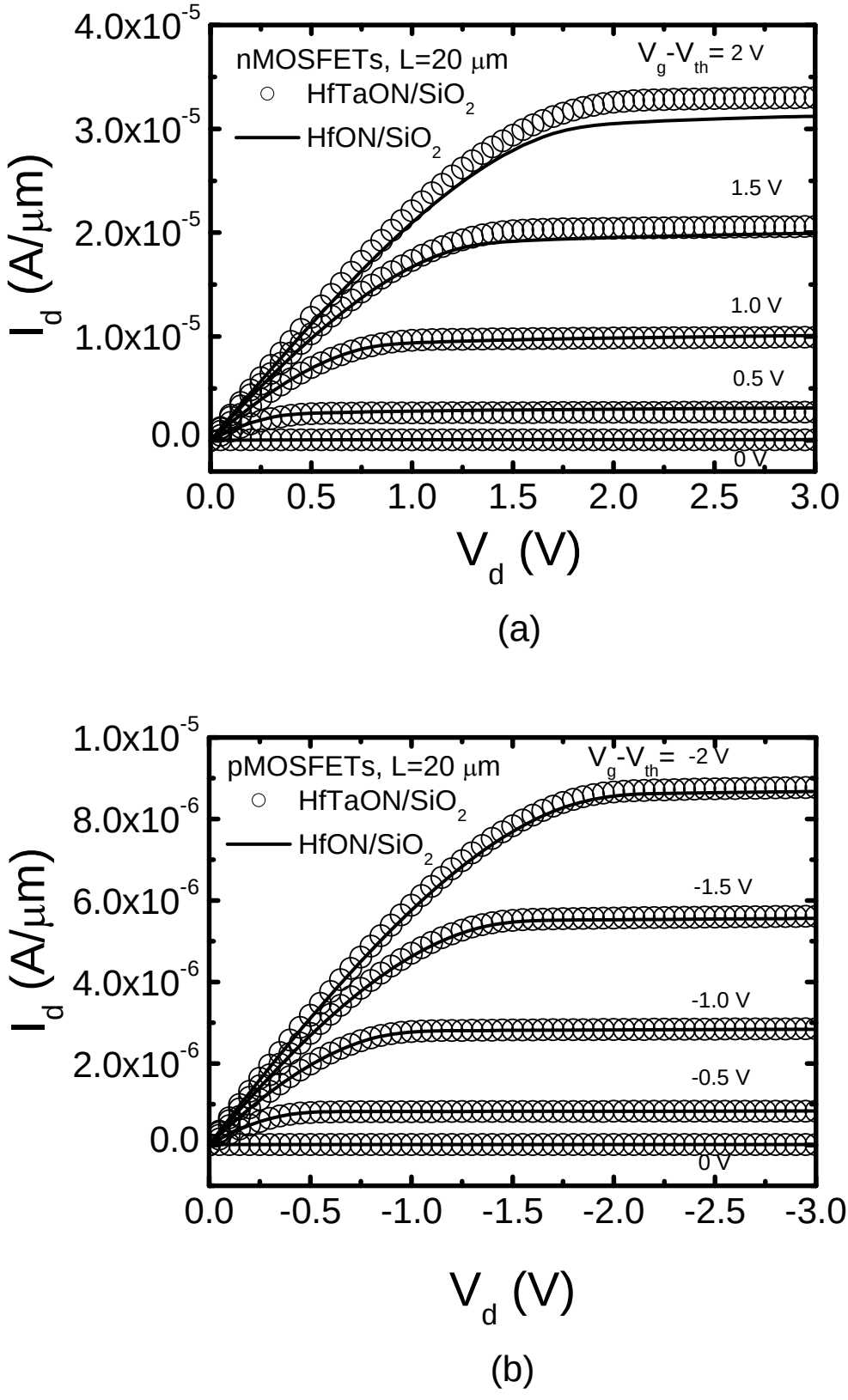


Fig. 3.14: I_d-V_d characteristics for (a) nMOSFETs and (b) pMOSFETs with $HfON/SiO_2$ and $HfTaON/SiO_2$ gate stacks.

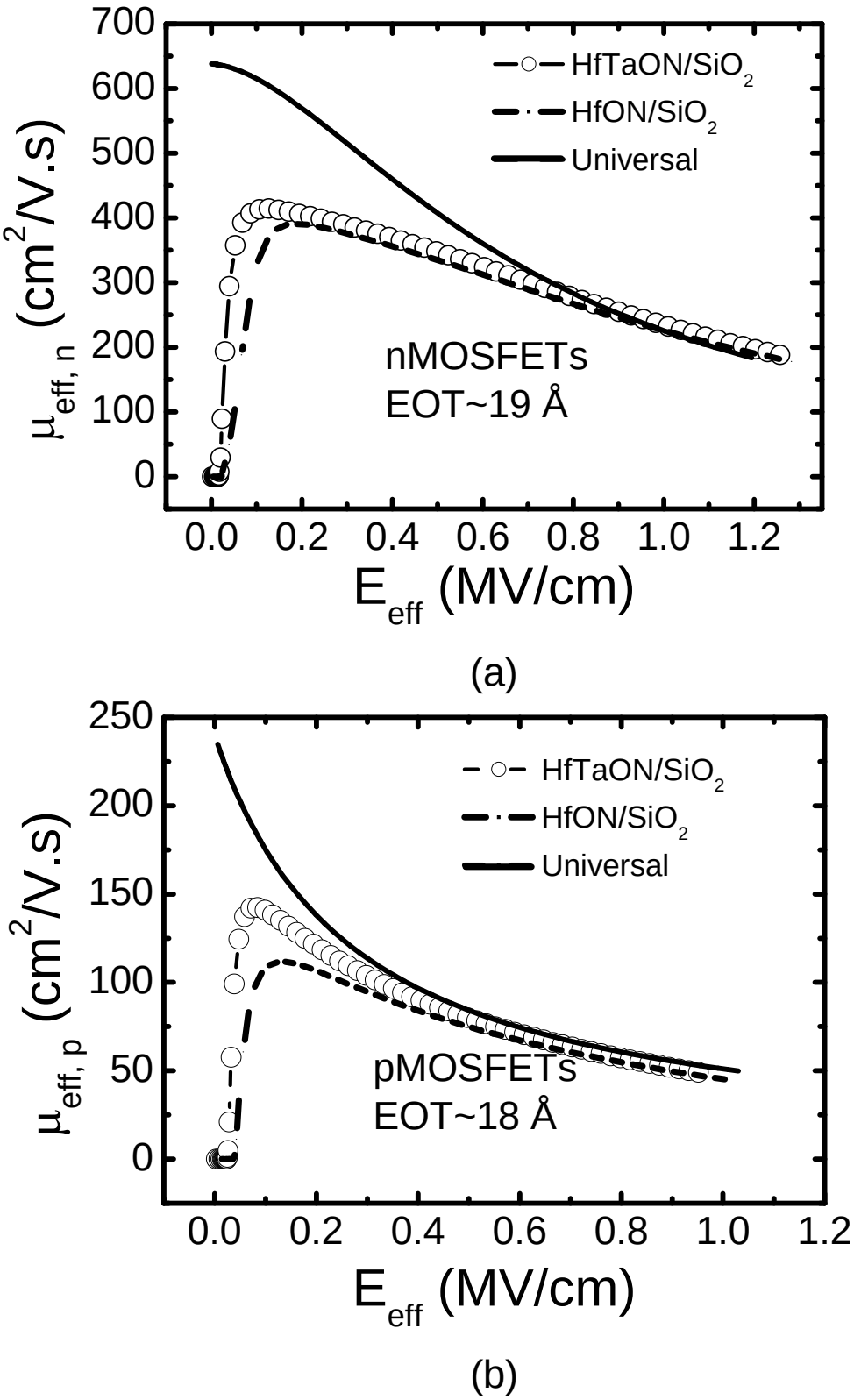


Fig. 3.15: Comparison of (a) electron and (b) hole mobility in HfON/SiO$_2$ and HfTaON/SiO$_2$ MOSFETs. Both electron and hole mobility in HfON/SiO$_2$ are slightly lower than those in HfTaON/SiO$_2$ at low effective filed region, but almost no difference at middle or high effective filed region.

Fig. 3.15 depicts (a) electron and (b) hole mobility, which obtained by split *C-V* method, in MOSFETs with HfON/SiO_2 and HfTaON/SiO_2 gate stack after activation annealing at 1000ºC for 10 sec. It was noted that both electron and hole mobility in HfON/SiO_2 nMOSFET were slightly lower than in HfTaON/SiO_2 at low effective field region, but almost no difference was found at middle or high effective filed region. At the operation voltage of devices, in which the effective field is about 0.8 MV/cm, electron mobility of 100% and hole mobility of 96% of universal curves were obtained in both HfON/SiO_2 and HfTaON/SiO_2 gate stacks. It should be noted that the electron mobility in HfO_2 and HfTaO without the SiO_2 IL were 81 and 155 cm^2/V-s (as presented in **Chapter 2**) at 0.8 MV/cm, which were only 28% and 54% of the universal curves. By inserting the SiO_2 IL, the mobility in HfO_2 and HfTaO gate dielectrics may be increased significantly. The remarkable improvements on the carrier mobility imply that the ultra-thin SiO_2 IL in the high-*k* gate stacks play a key role in the mobility behavior.

3.3.5 V_{th} Instability in HfTaON/SiO_2 Gate Stack

It is well known that the most high-*k* gate dielectrics exhibit significant charge trapping effect, which causes the V_{th} shift during operation. The charge trapping induced V_{th} instability is a key challenge for integration of high-*k* gate dielectric for future CMOS application [24]. **Fig. 3.16** shows comparison of the V_{th} instability in (a) nMOSFETs and (b) pMOSFETs with HfON/SiO_2 and HfTaON/SiO_2 gate stacks after PMA at 1000 ºC for 10 sec. The constant voltage stresses of $V_{th}\pm$ 2 and $V_{th}\pm$ 2.5 V were applied at the gate electrode, and the conventional static (DC) measurement with 100 μs delay time (as discussed in **Chapter 2**) was used to examine the V_{th} instability. As shown in **Fig. 3.16**, the V_{th} shifts in HfTaON/SiO_2 MOSFETs were much lower than those in HfON/SiO_2 under the same constant voltage stress. This indicates that the charge trapping induced V_{th} instability in HfON/SiO_2 gate stack is significantly suppressed by incorporating Ta, which could relate to the different film morphology observed in HfTaON and HfON films. It was already known that the HfTaON remains

amorphous structure and the HfON is partially crystallized after PMA at 1000 ºC for 10 sec (**Fig. 3.4**). The grain boundaries in the crystallized film could be with weak bond strength and easy to be trapped. It was also noted that the improvement on V_{th} shift by adding Ta is more evident in nMOSFETs rather than pMOSFETs. The V_{th} shift in HfTaON/SiO_2 nMOSFETs is more than 10 times lower than in HfON/SiO_2, however, the V_{th} shift in HfTaON/SiO_2 is only around 2 times lower compared to HfON/SiO_2 for pMOSFETs. It is commonly believed that the V_{th} shift under positive stress in nMOSFETs is caused by filling of pre-existing bulk traps in high-*k* film. On the other hand, the V_{th} shift under negative stress in pMOSFETs is qualitatively similar to those observed in SiO_2 and SiON devices, which is mainly due to the depassivation of Si-H bonds at the oxide/Si interface [25]. The incorporation of Ta into HfON has a strong impact on the high-*k* bulk film, whereas it may not affect the oxide/Si interface severely due to the insertion of SiO_2 IL. This may explain the finding of the improvement on V_{th} instability by adding Ta is more effective in nMOSFETs rather than pMOSFETs in the HfTaON/SiO_2 gate stack.

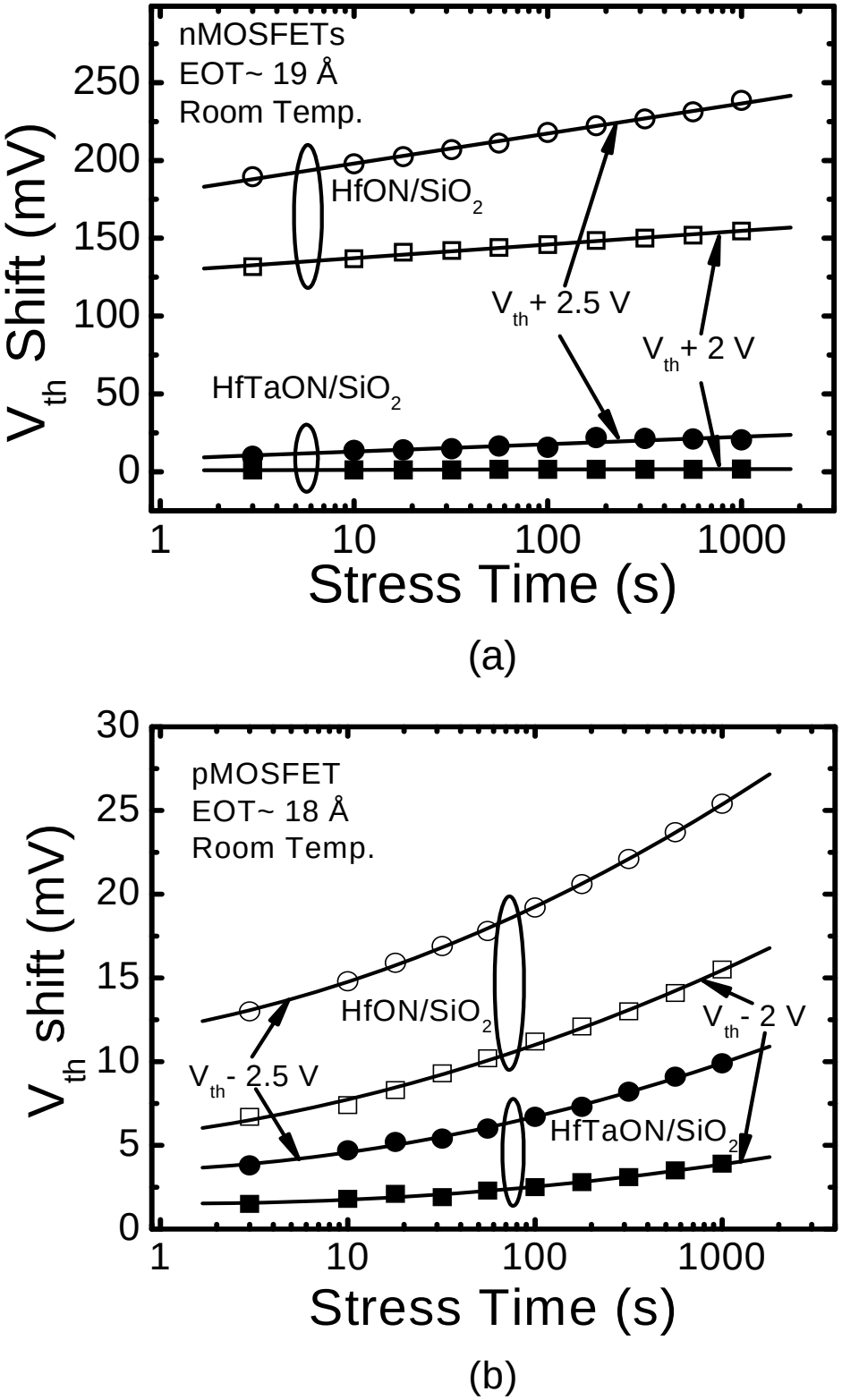


Fig. 3.16: V_{th} instability for (a) nMOSFETs and (b) pMOSFETs with $HfON/SiO_2$ and $HfTaON/SiO_2$ gate stacks under constant voltage stresses. The V_{th} shift in $HfON/SiO_2$ is remarkably suppressed by incorporating Ta.

3.4 Conclusion

Table 3.1: Comparison of device performances between the HfTaON/SiO$_2$ gate stack and Hf-silicates devices. The HfTaON/SiO$_2$ shows lower leakage current and higher carrier mobility compared to those published results.

	EOT (Å)	J_g (A/cm^2) @ V_{fb}-1V	$\mu_{electron}(\mu_{hole})/\mu_{universal}$ @0.8MV/cm	Ref.
HfTaON/SiO$_2$	16.6	1.6×10^{-4}	100% (96%)	This work
HfTaO	18.6	4.1×10^{-5}	54%	VLSI2004 [26]
HfSiO/SiO$_2$	18.6	2×10^{-3}	95%	VLSI2003 [13]
HfSiO	17.2	8×10^{-4}	100% (90%)	IEDM2004 [27]
HfSiON/SiO$_2$	17.5	1×10^{-3}	80%	VLSI2003 [10]
HfSiON	17.1	2×10^{-3}	80% (80%)	VLSI2002 [8]

In this work, a novel HfTaON/SiO$_2$ gate stack, which consists of a HfTaON film with *k* value of 23 and a 10-Å SiO$_2$ interfacial layer, was proposed for advanced CMOS application. The HfTaON/SiO$_2$ gate stack provided much lower gate leakage current compared to SiO$_2$, good interface properties, excellent transistor characteristics and superior carrier mobility. Compared to HfON/SiO$_2$, improved thermal stability was also observed in the HfTaON/SiO$_2$ gate stack. Moreover, the charge trapping induced V_{th} instability was examined for the HfTaON/SiO$_2$ and HfON/SiO$_2$ gate stacks by using the conventional static (DC) measurement technology. The HfTaON/SiO$_2$ gate stack exhibited significant suppression of the V_{th} instability compared to the HfON/SiO$_2$, in particular for nMOSFETs. These excellent performances observed in the HfTaON/SiO$_2$ can be attributed to the good physical and electrical characteristics shown in HfTaO film, which were presented in **Chapter 2**. Also, the incorporation of N into HfTaO may further improve the thermal stability of gate stack, and the very low D_{it} and superior carrier mobility shown in this gate stack may be mainly attributed to the insertion of SiO$_2$ interfacial layer between

HfTaON film and Si substrate. **Table 3.1** summarizes the device performance for the HfTaON/SiO_2 gate stack and some published results. Compared to those published results observed in the Hf-silicates, the HfTaON/SiO_2 gate stack showed lower gate leakage current and higher carrier mobility. The excellent performances observed in HfTaON/SiO_2 gate stack indicate that it has potential to replace the conventional SiO_2 or SiON as gate dielectric for advanced CMOS application.

On the other hand, the superior carrier mobility shown in HfTaON/SiO_2 gate stack is mainly due to the insertion of the 10-Å SiO_2 interfacial layer. By comparing the carrier mobility in the high-*k* with or without the SiO_2 layer, it is concluded that the SiO_2 interfacial layer plays a key role for the suppression of mobility degradation. However, the insertion of SiO_2 interfacial layer may limit the continuous scaling of dielectric thickness, and the HfTaON/SiO_2 gate stack appears to be very promising candidate for low standby power application rather than high performance application, which requires further scaling down of *EOT* to less than 10 Å in the near future [28]. In fact, among all of high-*k* candidates, almost none can completely meet the requirements for high performance CMOS application yet. Therefore, further work is needed to develop a novel high-*k* gate stack with sufficiently good performance for the advanced high performance CMOS application, which is a serious challenge faced by the semiconductor researcher currently.

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Chapter 4

Effect of Gate Dopant Penetration on Leakage Current in n^+ Poly-Si/HfO_2 Device

4.1 Introduction

In order to maintain the continued scaling of CMOS devices, high-*k* gate dielectric will be required as the replacement of conventional SiO_2 or SiON, because of their potential in reducing equivalent oxide thickness (*EOT*) while maintaining low gate leakage current. A significant issue for integrating any advanced gate dielectric into standard CMOS process is that the dielectric would be compatible with poly-Si gate electrode, rather than require a metal gate. Poly-Si gate electrode is desirable because dopant implant conditions can be tuned to create the desired threshold voltage (V_{th}) for both nMOS and pMOS, and the process integration schemes are well established in industry. For CMOS scaling in a long term, however, current roadmap predictions indicate that poly-Si gate technology will likely be phased out by 2008, after which a metal gate substitute appears to be required. Advanced metal gates are very desirable for eliminating dopant depletion effects and sheet resistance constraints. In addition, use of metal gates in a replacement gate process could lower the required thermal budget by eliminating the need for dopant activation anneals in the poly-Si electrode. It is therefore desirable to focus efforts on high-*k* dielectric materials systems which are compatible with the conventional poly-Si gate and also the potential metal gate materials.

4.2 Review of Literature

HfO_2 gate dielectric, as one of promising high-*k* candidates, has been widely investigated for the past few years. There have been demonstrated that the HfO_2 gate dielectric exhibited much low gate leakage currents whatever with the conventional poly-Si [1-3] or advanced metal [4-6] gate. However, the observation of excessive gate leakage current or even initial breakdown, in particular for the devices with n^+ poly-Si gate, was also reported in HfO_2 gate dielectric by several research groups. Gilmer et al. found that the poly-Si/HfO_2 MOS capacitors showed very high leakage current, whereas the insertion of an amorphous Al_2O_3 capping layer between the poly-Si gate and the HfO_2 film was able to reduce the leakage current by four orders of magnitude [7]. Morisaki et al. reported that a severe gate leakage current was observed in HfO_2 film with poly-Si gate, and the poly-Si/SiN/HfO_2 device exhibited 6-order-lower leakage current [8]. Kaushik et al. demonstrated that the HfO_2 film with poly-Si gate (deposited at high temperature) provided shorted device, however, with amorphous-Si gate (deposited at low temperature) exhibited acceptable leakage [9]. Moreover, a strong dependence of gate leakage current density on the device area, for which the device with larger area showed a larger leakage current density, was observed in the poly-Si/HfO_2 devices [8-11].

In **Chapter 2**, the gate leakage currents of HfO_2, HfTaO with 29% and 43% Ta films were presented in the devices with TaN metal gate. As shown in **Fig. 4.1**., the leakage currents of the films increased with increasing Ta composition in the devices with metal gate. This is an apprehensible result since the incorporated Ta-oxide with lower band offset may result in the increased leakage current. Moreover, the gate leakage currents of HfO_2, HfTaO 29% and 43% Ta films have also been investigated in the devices with poly-Si gate. **Fig. 4.2** compares the gate leakage currents of HfO_2, HfTaO with 29% and 43% Ta in nMOS capacitors with n^+ poly-Si gate. It was noted that the gate leakage currents of the films decrease with increasing Ta composition in the devices with n^+ poly-Si gate. This result observed in the high-*k* gate dielectrics with poly-Si gate is opposite to that shown in the devices with metal gate. It was also

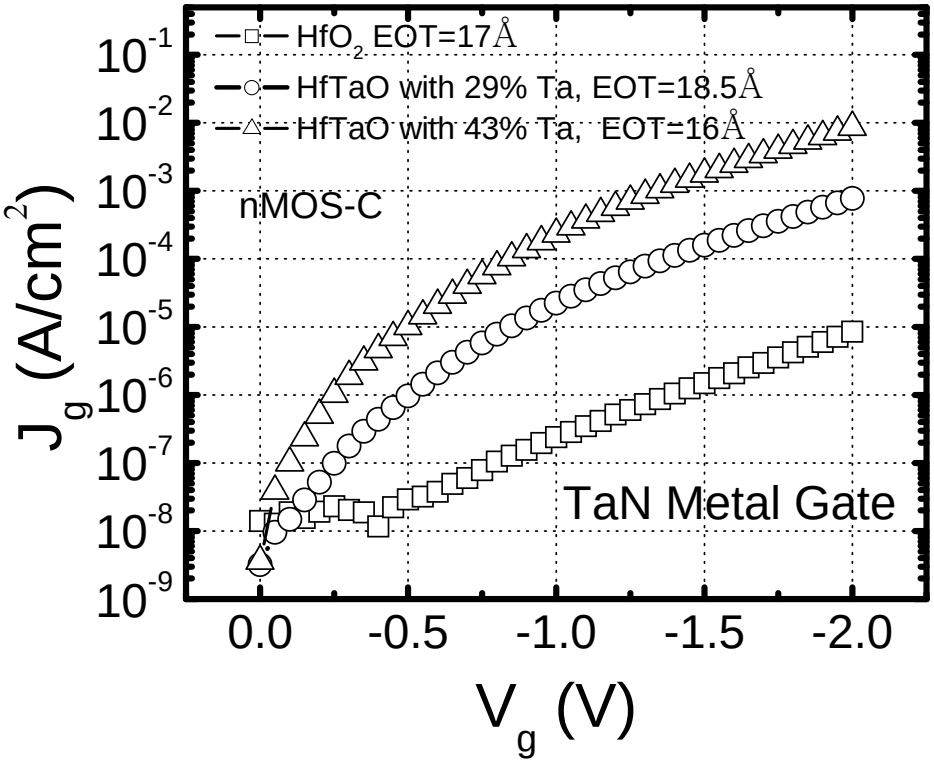


Fig. 4.1: Typical *J-V* curves of TaN metal gate MOS capacitors with HfO_2, HfTaO with 29% and 43% Ta dielectrics after activation annealing at 950° C for 30 sec. HfTaO dielectrics show higher leakage current compared to HfO_2.

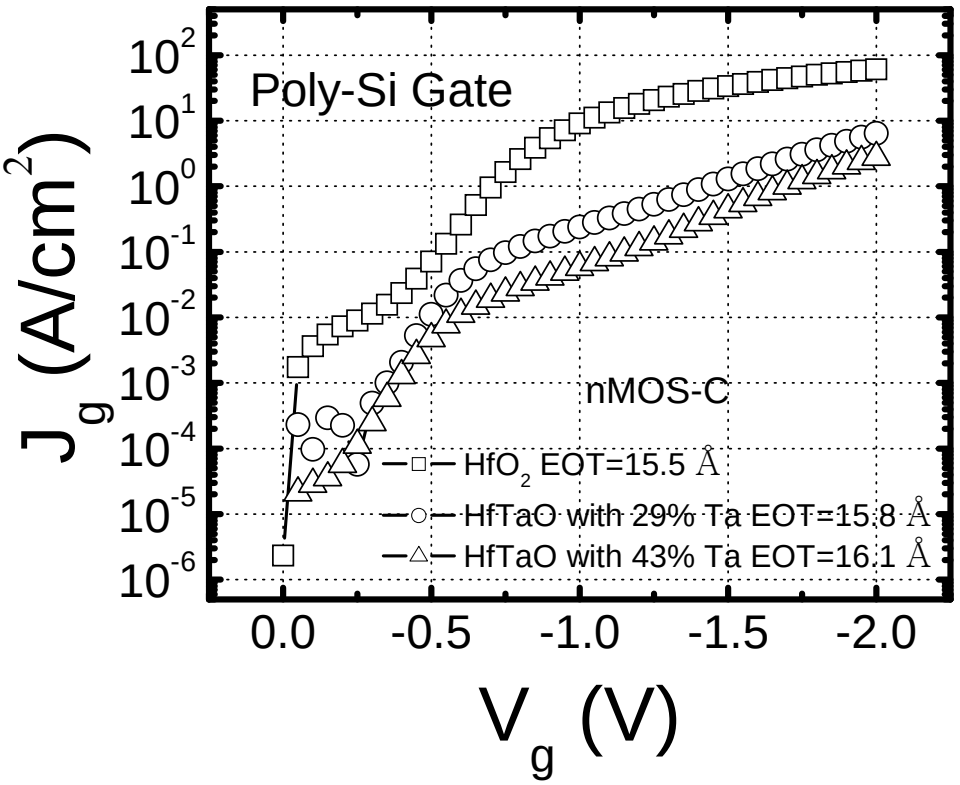


Fig. 4.2: Typical *J-V* curves of n^+ poly-Si gate MOS capacitors with HfO_2, HfTaO with 29% and 43% Ta dielectrics after activation annealing at 950° C for 30 sec. HfTaO dielectrics show lower leakage current compared to HfO_2.

found that the gate leakage currents in poly-Si/high-*k* devices are much higher than that in metal gate devices. It is already known that the major difference between HfO_2 and HfTaO is the film morphology and the incorporation of Ta into HfO_2 may effectively suppress the crystallization of the film. Hence, it is possible to speculate that the different behaviors of gate leakage currents in the poly-Si and metal gate devices may relate to the change of film morphology.

Several mechanisms have been proposed to explain the findings of the excessive leakage current and its device-area-dependence in the poly-Si/HfO_2 devices. One possible explanation is that the excessive leakage current was caused by the interaction (silicidation) between poly-Si and HfO_2 during high temperature annealing [8]. However, this may not explain the fact of the dependence of leakage current density on the device area, and also there is almost no report on the formation of silicides in the poly-Si/HfO_2 stack [11]. On the other hand, it has been proposed that the grain boundaries in crystallized HfO_2 film possibly increased the gate leakage current [12]. Although this may explain the device-area-dependence of leakage current density because the grain boundaries in crystallized HfO_2 film may significantly affect the larger devices rather than the smaller devices, it is not consistent with the experimental result in which the fully crystallized HfO_2 showed lower leakage current compared to the amorphous HfTaO in metal gate devices, as shown in **Fig. 4.1**. Hence, the root of the excessive leakage current and its device-area-dependence in the poly-Si/HfO_2 devices is not clear yet.

In this study, the experimental results demonstrated that the doping concentration of poly-Si gate may remarkably affect the gate leakage current in n^+ poly-Si/HfO_2 devices. The poly-Si/HfO_2 devices with low gate doping concentration showed very low leakage currents, which were also comparable with that in TaN metal gate device. On the other hand, the poly-Si/HfO_2 devices with heavy gate doping concentration were shorted. For the first time, the conducting atomic force microscopy (C-AFM) was applied to examine the current images of the HfO_2 films with excessive leakage currents, and evident leakage paths were observed. Based on the experimental results and the physical analyses (C-AFM, TEM and SIMS), the

excessive leakage currents and the evident leakage paths observed in the high leaky HfO_2 films may be attributed to the penetration of the excessive dopants from the n^+ poly-Si gate. It is also possible to speculate that the diffusion of excessive dopants from the n^+ poly-Si gate into the HfO_2 film, especially through the grain boundaries in the crystallized film, could generate dopant-related defects, which may induce the evident leakage paths and significantly increase the gate leakage current in the n^+ poly-Si/HfO_2 devices. This hypothesis can sufficiently explain the previous findings of the correlative dependence of gate leakage current on the deposition temperature of Si gate, device area, and capping layer of gate dielectric in poly-Si/HfO_2 devices. Also, different behaviors of gate leakage currents in the HfTaO devices with poly-Si and metal gate, as shown in **Fig. 4.1** and **4.2**, can be adequately explained by this hypothesis.

4.3 Experiments

The n^+ poly-Si/HfO_2 MOS capacitors were fabricated on 6-inch p-Si (100) wafers with a resistivity of 10 ohm-cm. After active area definition, 13 nm HfO_2 film were deposited by metal organic chemical vapor deposition (MOCVD) technique after standard pre-gate clean with diluted hydrofluoric-last processes. Post-deposition annealing in N_2 ambient was followed by rapid thermal annealing (RTA) at 700^{o}C for 30 sec. Two-step-deposition of poly-Si gate electrode was performed by low pressure chemical vapor deposition at 540ºC (amorphous silicon film as-deposited). Firstly, an un-doped silicon film was deposited on the top of the HfO_2, and then followed by an *in situ* P-doped silicon film. The doping concentration of Si gate was controlled by the ratio of the two silicon film thicknesses, and total thickness of the Si gate was fixed as 200 nm. Some devices using TaN metal gate with a thickness of 200 nm were also prepared as the references. **Table 4.1** summarizes the splits of four Si gate devices and one TaN metal gate device, which are defined as S-1, S-2, S-3, S-4 and M-1 respectively, and also the doping concentration of the Si gates. After gate patterning, the gate activation annealing was performed at 1000^{o}C in N_2 ambient for 10 sec.

Sintering was done at 420^o C in forming gas ambient for 30 min after Al metallization.

Table 4.1: Summary of the formation of gate stacks for the poly-Si gate, TaN metal gate devices, and also the doping concentration of the poly-Si gates.

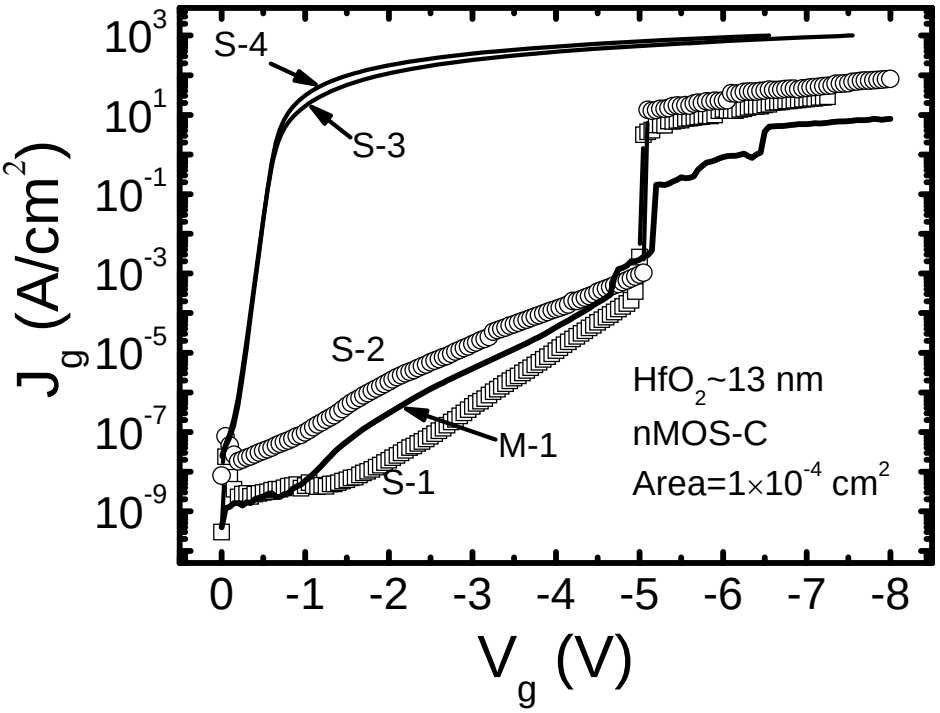
Sample	HfO_2 (nm)	Un-doped poly-Si (nm)	P-doped poly-Si (nm)	P-doping concentration (atom/cm^{-3})
S-1	13	130	70	~6.5×10^{19}
S-2	13	70	130	~1.5×10^{20}
S-3	13	20	180	~2.8×10^{20}
S-4	13	0	200	~2.9×10^{20}
M-1	13	200-nm TaN metal gate		

The phosphorus-diffusion profiles were characterized by secondary-ion-mass spectrometry (SIMS) using Cs^+ ion primary beam with a net energy of 15 KeV. To evaluate the surface morphology and leakage paths in the HfO_2 films, the poly-Si gates were chemically removed by using diluted KOH at room temperature, and then C-AFM was used for surface analysis. The capacitance versus voltage (*C-V*) at 100 KHz and the leakage current density versus voltage (*J-V*) characteristics of the nMOS capacitors with an electrode area of 1×10^{-4} cm^2 were measured using HP4284A LCR meter and HP4156A semiconductor parameter analyzer respectively. *EOT* and flat-band voltage (V_{fb}) were determined using Quantum-Mechanical *CV* simulator program (published by UC Berkeley Device Group), taking into account the poly-Si depletion and quantum mechanical effects.

4.4 Results and Discussion

4.4.1 *C-V* and *J-V* Characteristics

Fig. 4.3 (a) illustrates the gate leakage currents for the nMOS capacitors as a



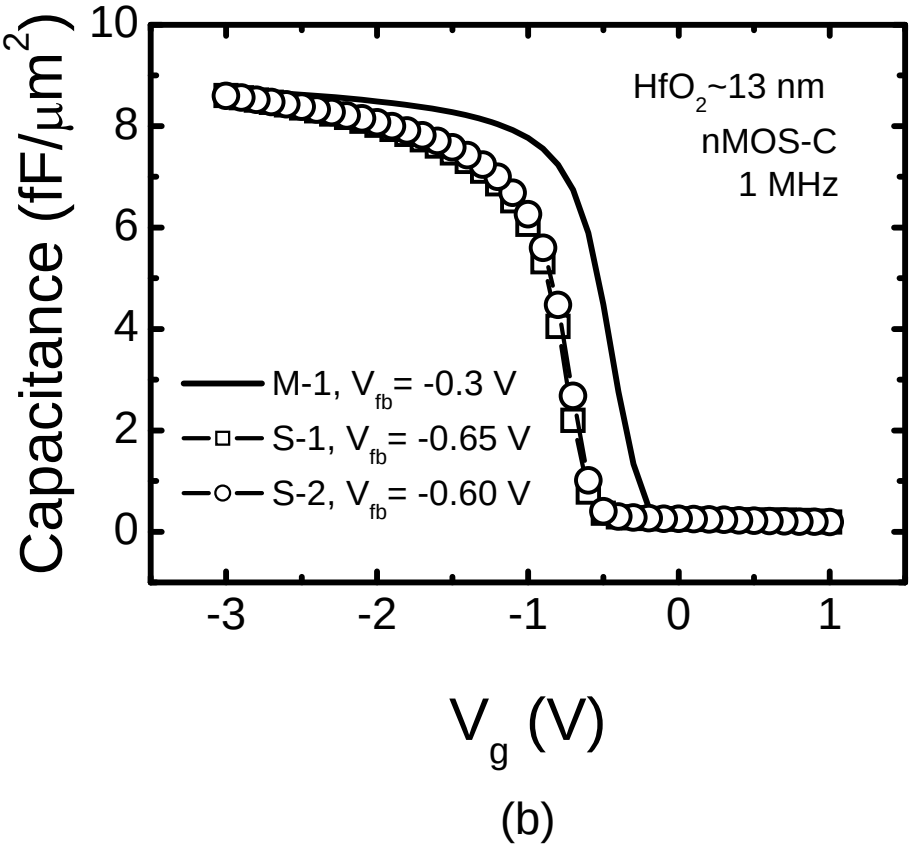


Fig. 4.3: (a) Comparison of gate leakage currents for the n^+ poly-Si gate and metal gate devices as a function of the gate bias. (b) *C-V* characteristics for S-1, S-2 and M-1 nMOS capacitors. The *C-V* curves of S-3 and S-4 cannot be measured due to the excessive gate leakage currents.

function of gate bias, and the corresponding *C-V* curves are shown in **Fig. 4.3 (b)**. As shown in **Fig. 4.3 (a)**, the S-3 and S-4 samples with heavy doping poly-Si gate exhibited excessive leakage currents, whereas the S-1 and S-2 with low doping poly-Si gate showed much low leakage currents which were also comparable with that of the metal gate device (M-1). Due to the excessive leakage currents in S-3 and S-4, *C-V* curves for the two devices cannot be measured. Conversely, the S-1, S-2 and M-1devices showed well-behavior *C-V* plots, similar capacitances in accumulation region, and reasonable flat band voltages in **Fig. 4.3 (b)**.

4.4.2 Physical Characteristics

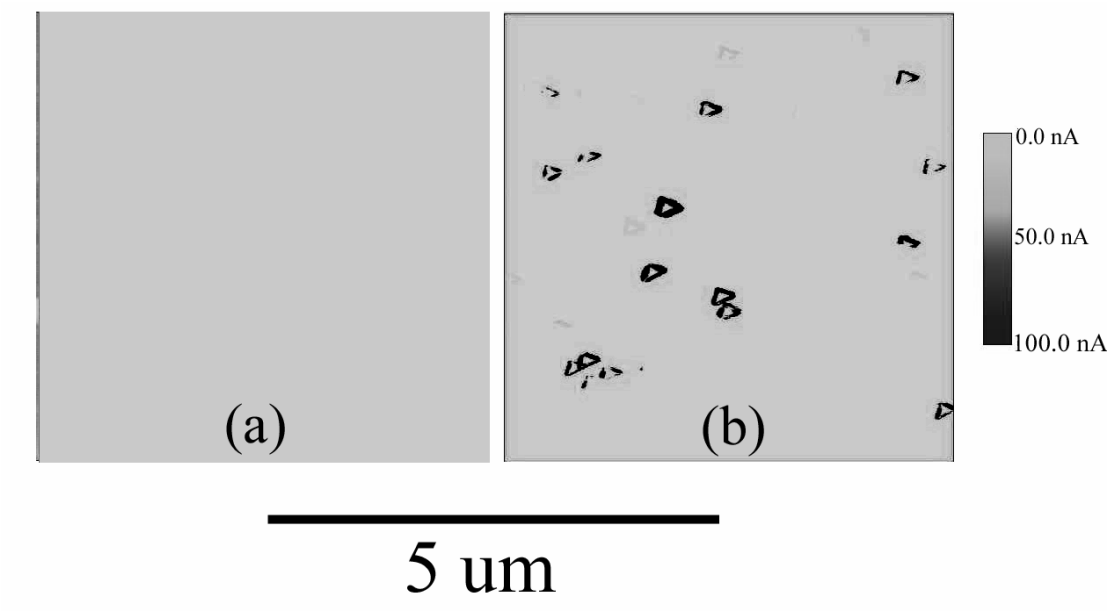


Fig. 4.4: C-AFM current images of samples (a) S-1 and S-2, (b) S-3 and S-4 after removal of the poly-Si gates. The evident leakage paths are found in the HfO_2 films with heavy doping poly-Si gate (S-3 and S-4), whereas no leakage path are observed in the HfO_2 films with low doping poly-Si gates (S-1 and S-2) at the tip bias of 40 mV.

In order to evaluate the root of the excessive gate leakage current in the high leaky devices, the poly-Si gates were chemically removed by diluted KOH at room temperature, and then C-AFM was applied for current image analysis. It should be

noted that the thicknesses of HfO_2 films after removal of poly-Si gates (measured by ellipsometer) was around 13.1 nm, which is almost same as that of deposited HfO_2 prior to the poly-Si gate. This suggests that the removal of poly-Si gates by diluted KOH may not affect the HfO_2 gate dielectric severely. **Fig. 4.4** shows the C-AFM current images at a very small tip bias of 40 mV for the HfO_2 films after removal of poly-Si gates. As shown in **Fig. 4.4 (a)**, no leakage paths were observed in the S-1 and S-2. However, the S-3 and S-4 exhibited evident leakage paths with annular shape in **Fig. 4.4 (b)**. These are consistent with previous results that the S-3 and S-4 showed much higher gate leakage currents than S-1 and S-2. A similar C-AFM image of the leakage paths with the annular shape was also observed in a recent study on the evolution of leakage paths in HfO_2/SiO_2 dielectrics [13].

Some research groups suggested that the excessive gate leakage currents observed in poly-Si/HfO_2 devices were caused by the interaction between poly-Si and HfO_2 during high temperature annealing [8], however, it is not consistent with our experimental results which the S-1 and S-2 devices with the same process flow showed much lower gate leakage currents compared to S-3 and S-4. Since the only difference in process among the four poly-Si gated devices (S-1, S-2, S-3 and S-4) is the doping concentration of poly-Si gate, the significant enhancement in gate leakage currents and the evident leakage paths observed in S-3 and S-4 devices may be related to the dopants diffusion from the poly-Si gate. It is well known that HfO_2 is anticipated to become more crystalline upon annealing at a high temperature (~500^o C). The grain boundaries in the crystallized HfO_2 film may act as the high-diffusivity paths for the dopants in poly-Si gate. **Fig. 4.5** shows the TEM image of the high leaky poly-Si gated devices (S-3 and S-4) after activation annealing at 1000ºC for 10 sec. As can be seen, a smooth interface between poly-Si and HfO_2 was obtained after the annealing at 1000ºC, and no evident defects or silicides were found at this poly-Si/HfO_2 interface. Moreover, fully crystallized HfO_2 film with a grain boundary was clearly observed. It was also noted that the dimension of HfO_2 grain is comparable to those of leakage paths observed in **Fig. 4.4 (b)**. Based on the observation in C-AFM and TEM images, it is possible to speculate that the evident

leakage paths observed in S-3 and S-4 could be related to the grain boundaries in the fully crystallized HfO_2 film. This may be the reason why the leakage paths showed annular shape.

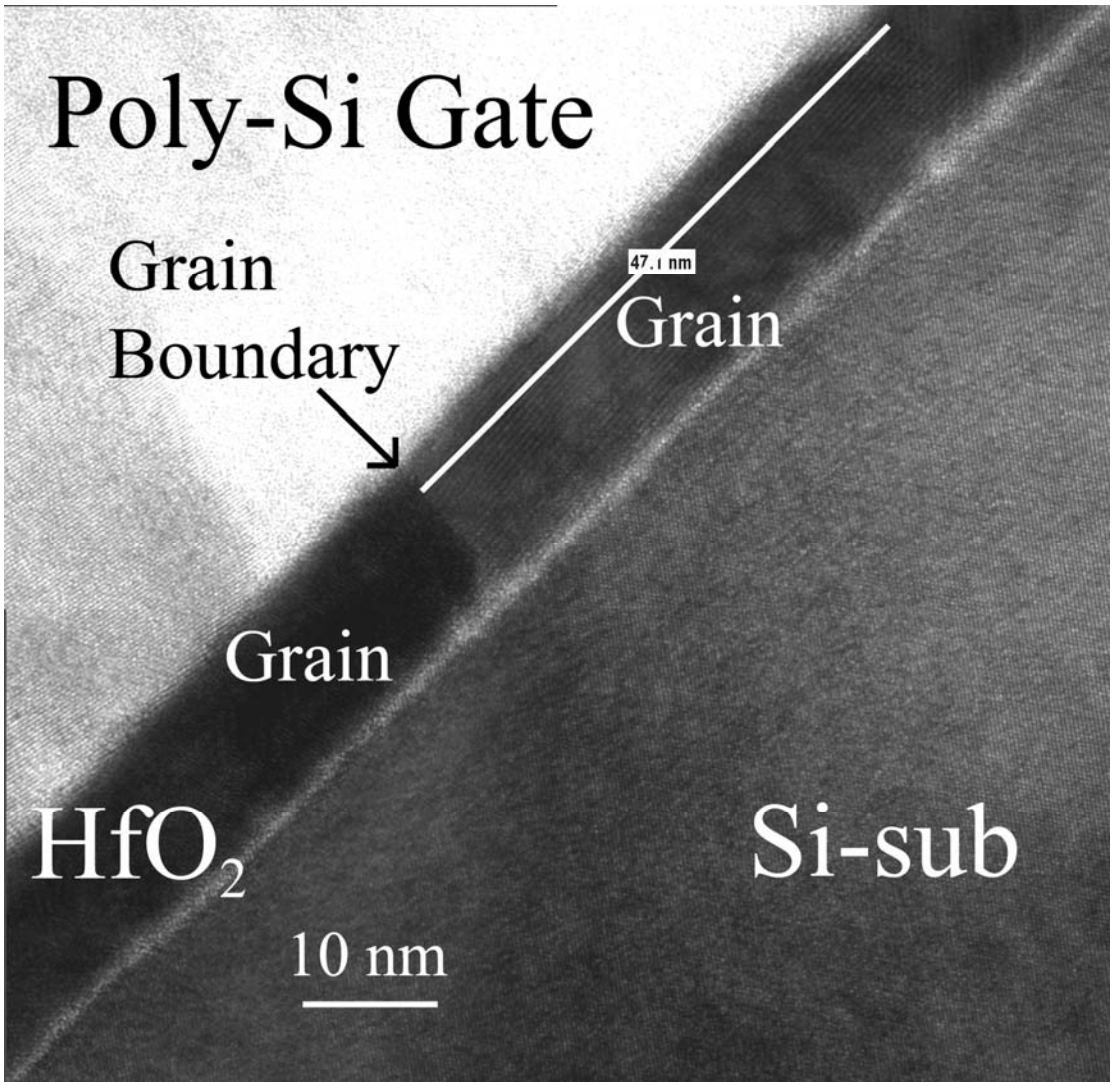


Fig. 4.5: TEM image of the high leaky HfO_2 films (S-3 and S-4) with poly-Si gate after activation annealing at 1000ºC for 10 sec. The HfO_2 film shows crystallized structure with obvious grain boundary.

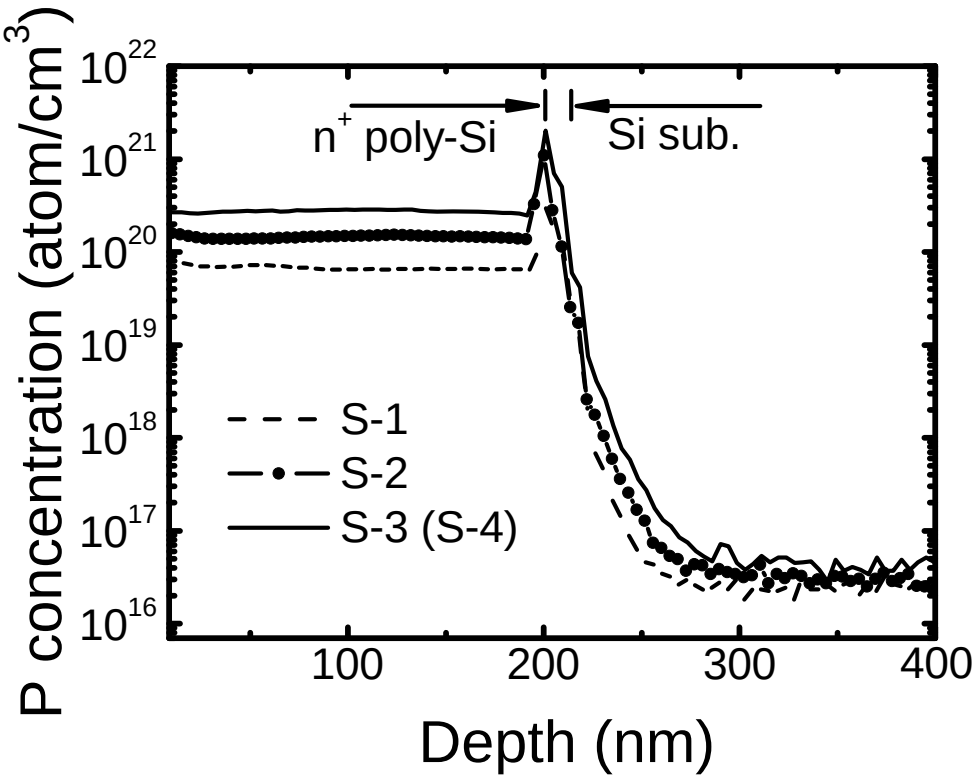


Fig. 4.6: SIMS profiles of phosphorus in the n^+ poly-Si/HfO_2 stacks after activation annealing at 1000ºC for 10 sec. The diffusion of phosphorus into HfO_2 gate dielectric becomes more serious with increasing the doping concentration of poly-Si gate. (S-3 and S-4 show similar phosphorus-diffusion profiles.)

The secondary-ion-mass spectrometry (SIMS) profiles of phosphorus in the poly-Si/HfO_2 stacks after the annealing at 1000ºC for 10 sec are shown in **Fig. 4.6**. The phosphorus-doping concentrations of the poly-Si gates were 6.5×10^{19} /cm^3, 1.5×10^{20} /cm^3, 2.8×10^{20} /cm^3 and 2.9×10^{20} /cm^3 for S-1, S-2, S-3 and S-4, respectively. Due to the poly-Si gate with heavy doping in S-3 (S-4), the diffusion of phosphorus into HfO_2 films after the annealing became more serious in S-3 (S-4) rather than in S-1 and S-2. Moreover, it should be noticed that the peaks of phosphorus-profiles at the poly-Si/HfO_2 interface, which are due to the sudden change of sputter rate and ion yield during the SIMS analysis, should not be taken as indication of high phosphorus concentration at the interface [14].

4.4.3 Discussion

It is well known that boron from p^+ poly-Si gate may easily diffuse not only through the gate dielectric layer but also into the channel region during the high thermal budget process. The issue of boron penetration is a significant concern for both SiO_2/SiON and high-*k* gate dielectrics, which may result in interface degradation and threshold voltage shifts. After in-depth studies, the boron penetration is now well understood in the SiO_2/SiON [15-18] and HfO_2 based gate dielectrics [19-22]. On the other hand, since the diffusion coefficients of phosphorus and arsenic in HfO_2 are about four orders of magnitude greater than those in SiO_2 and the segregation coefficients of phosphorus and arsenic at the poly-Si/HfO_2 interface are less than 1, the phosphorus or arsenic penetration are also significant in HfO_2 gate dielectric rather than in SiO_2 [23]. It is therefore important to evaluate the impact of phosphorus or arsenic penetration on the gate dielectric properties in n^+ poly-Si/HfO_2 devices.

Based on our experimental results and the physical analyses, the excessive leakage currents and the evident leakage paths observed in S-3 and S-4 may be attributed to the diffusion of the excessive dopants from the n^+ poly-Si gate. It is also possible to speculate that the diffusion of excessive dopants from n^+ poly-Si gate into HfO_2 film, especially through grain boundaries in the film, could generate dopant-related defects (or a “special silicidation” with dopant-related characteristic), which may induce the evident leakage paths and significantly increase the gate leakage current in the n^+ poly-Si/HfO_2 devices. This hypothesis may sufficiently explain the previous findings of the correlative dependence of gate leakage current on the deposition temperature of Si gate, device area, and capping layer of gate dielectric in poly-Si/HfO_2 devices. Also, different behaviors of gate leakage currents in the HfTaO devices with poly-Si and metal gate, as shown in **Fig. 4.1** and **4.2**, can be adequately explained by this hypothesis.

4.5 Conclusion

In summary, the experimental results demonstrated that the gate dopants penetration may remarkably affect the gate leakage current in n^+ poly-Si/HfO_2 devices. The poly-Si/HfO_2 devices with low gate doping concentration exhibited very low leakage currents, whereas the devices with heavy gate doping concentration showed excessive leakage currents. The current images examined by C-AFM confirmed the existence of evident leakage paths in the highly leaky HfO_2 films. It is possible to speculate that the diffusion of excessive dopants from n^+ poly-Si gate into the HfO_2 film, especially through the grain boundaries in the film, could generate dopant-related defects (or a "special silicidation" with dopant-related characteristic), which may induce the evident leakage paths and significantly increase the leakage current in the n^+ poly-Si/HfO_2 devices. This hypothesis may sufficiently explain the previous findings of the correlative dependence of gate leakage current on the deposition temperature of Si gate, device area, and capping layer of gate dielectric in poly-Si/HfO_2 devices. Also, different behaviors of gate leakage currents in the HfTaO devices with poly-Si and metal gate can be adequately explained by this hypothesis. These results imply that phosphorus or arsenic penetration is also significant concern for poly-Si/HfO_2 device, and an amorphous capping layer between HfO_2 and poly-Si gate or incorporation of N into HfO_2 may be needed to suppress the dopant penetration in n^+ poly-Si/HfO_2 device.

On the other hand, the root of the significant increase in gate leakage current induced by the dopants penetration, or the generation of dopant-related defects is unclear yet. The impact of the dopants penetration on other electrical properties in poly-Si/HfO_2 device, such as carrier mobility, charge trapping induced threshold voltage instability, and gate dielectric breakdown, is still unknown. In addition, the influence of the dopants penetration on other high-*k* materials is also unexplored. We suggest that more work should be done to identify the mechanisms behind this phenomenon of dopant induced excessive leakage current, and also verify the impact of the dopant penetration on overall properties in n^+ poly-Si/high-*k* devices.

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Chapter 5

Effective Suppression of Fermi Level Pinning in Poly-Si/High-*k* by Inserting Poly-SiGe Gate

5.1 Introduction

SiO_2 or SiON has been the gate dielectric of choice over other dielectrics for several decades due to its outstanding physical and electrical properties on Si substrates. As CMOS devices are continuously scaled to increase performance and reduce cost, the gate leakage current becomes unacceptably high when the SiO_2 or SiON gate dielectric is scaled to a thickness range (< 2 nm) where direct tunneling is the dominant conduction mechanism. In order to maintain the continued scaling of CMOS devices, high-*k* gate dielectric will be required as the replacement of conventional SiO_2 or SiON, because of their potential in reducing equivalent oxide thickness (*EOT*) while maintaining low gate leakage current. A significant issue for integrating the high-*k* gate dielectric into standard CMOS process is that the dielectric would be compatible with poly-Si gate electrode. The poly-Si gate electrode is desirable because dopant implant conditions can be tuned to create the desired threshold voltage (V_{th}) for both nMOS and pMOS, and the process integration schemes are well established in industry.

Hf-based gate dielectrics, as the most promising high-*k* candidates, have been widely investigated for the past few years. There have been reported that the Hf-based gate dielectrics with poly-Si gate may provide much lower leakage current and

comparable mobility in contrast to poly-Si/SiO_2 devices [1, 2]. However, Fermi level pinning induced unacceptably high threshold voltage (V_{th}), in particular for pMOSFET, is a serious challenge for integration of the Hf-based gate dielectrics into mature poly-Si gate process [3]. Recent results indicate that the high V_{th} cannot be sufficiently lowered by simply adjusting the channel implants [4].

In general, V_{th} shifts reported for poly-Si gate CMOS devices with the Hf-based gate dielectrics, such as HfO_2 [5-7], HfSiO [4], HfON [8, 9], and HfSiON [10, 11] follow the same trend. The pMOS V_{th} is shifted in the negative direction by as much as 0.75 V relative to the SiO_2 control, whereas the V_{th} for nMOS devices is much closer to the SiO_2 control [3]. On the other hand, the V_{th} for typical Al_2O_3 pMOS devices is close to the SiO_2 controls whereas the V_{th} for Al_2O_3 nMOS devices is higher than the SiO_2 control [12-14]. Many publications attribute the findings of high V_{th} to positive fixed charge for HfO_2 and negative fixed charge for Al_2O_3. Although the fixed charges issue could explain the relative V_{th} shifts reported in HfO_2 pMOS or Al_2O_3 nMOS, it cannot adequately explain why the V_{th} shifts for nMOS and pMOS devices with same dielectrics are much different since fixed charges should shift the nMOS and pMOS V_{th} in the same direction [15]. Therefore, it is very important to identify the root of the high V_{th} issue observed in poly-Si/high-*k* devices.

5.2 Fermi Level Pinning at Poly-Si/high-*k* Interface

5.2.1 Theoretical Background

To understand the cause of these V_{th} shifts observed in the poly-Si/high-*k* gate stacks, it is necessary to consider the entire gate stack structure. Because an interfacial layer (IL) is typically found between the high-*k* and the Si substrate, there are several possible gate stack regions that may contribute to the V_{th} shift as illustrated in **Fig. 5.1**. Defects and charges within the gate stack may result in substantial V_{th} shifts.

There are many device parameters that can influence the V_{th} of a device. The flat-band voltage (V_{fb}) for a simple MOS capacitor structure can be described by [15]:

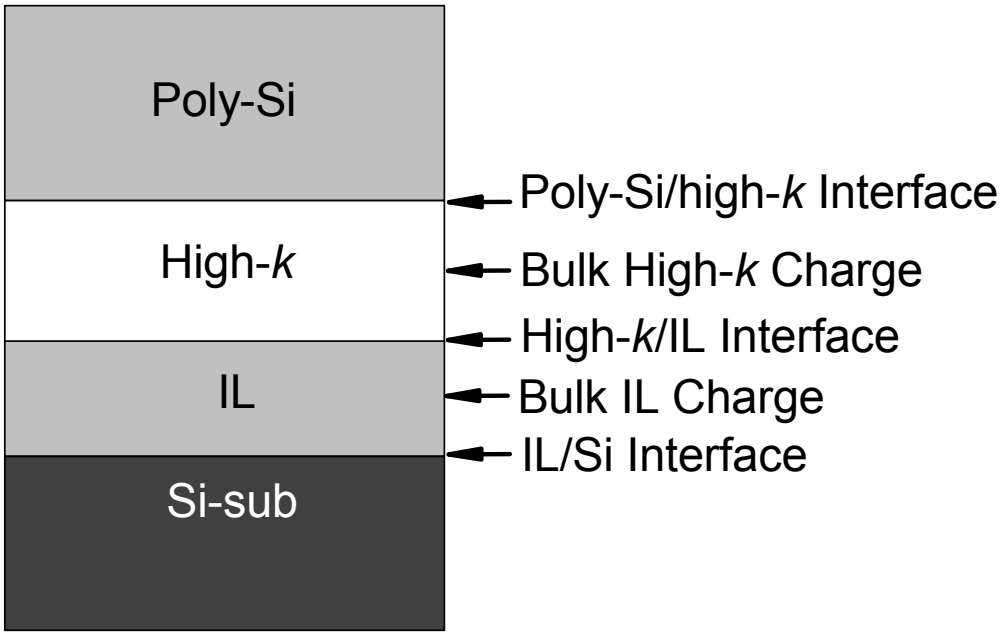


Fig. 5.1: Possible location of charges, which cause the Vth, shift.

$$V_{fb} = (\phi_M - \phi_S) - \sum_x \frac{Q_x}{C_x} \tag{1}$$

where the parameters are defined as:

ϕ_M : gate work function;

ϕ_S : substrate work function;

Q_x : oxide charge at distance *x* from poly-Si interface;

C_x : capacitance at distance *x* from poly-Si interface.

The summation term in (1) represents the shift in V_{fb} due to the charges within the gate stack. All of the parameters that may influence V_{fb} are included in (1). To derive an expression for a high-*k*/IL bi-layer gate dielectric like the one shown in **Fig. 5.1**, it may assume that the charge within the high-*k* is located near the high-*k*/IL interface and that the charge within the IL is located near the IL/Si interface. This results in the following expression for the summation term:

$$\sum_x \frac{Q_x}{C_x} = \left(\frac{Q_{Hk} + Q_{Hk/IL}}{C_{Hk}} \right) + \left(\frac{Q_{IL} + Q_{IL/Si}}{C_{IL}} \right) \quad (2)$$

where the parameters are defined as:

Q_{Hk} : charges located with the high-*k* layer;

Q_{IL} : charges located within the IL layer;

$Q_{Hk/IL}$: charges located at the high-*k*/IL interface;

$Q_{IL/Si}$: charges located at the IL/Si-substrate interface;

C_{Hk} : capacitance of the high-*k* layer;

C_{IL} : capacitance of the IL layer.

Using these expressions, it is possible to experimentally separate out the effect of each gate stack region in **Fig. 5.1**.

5.2.2 Fermi Level Pinning at Poly-Si/High-*k* interface

C. Hobbs et al. have systemically investigated the effect of each gate stack on the high V_{th} issue observed in poly-Si/high-*k* devices [3]. By varying the IL thickness, the impact of Q_{IL} and $Q_{IL/Si}$ on the V_{th} was studied. The high-*k* thickness was varied to determine the impact of Q_{Hk} and $Q_{Hk/IL}$. The impacts of ϕ_M and ϕ_S were studied by varying the gate and substrate doping, respectively. The authors reported that changing the poly-Si doping from n^+ to p^+ does little to shift the high-*k* *C*-*V*, which was unlike SiO_2. The effect was also independent of well doping and occurred even if a thick thermal oxide was grown prior to the high-*k*. This indicates that charges at the IL/Si interface or in the IL bulk are not the primary cause of the high V_{th} observed in poly-Si/high-*k* devices. On the other hand, the authors also studied the *C*-*V* characteristics of nMOS and pMOS devices with varied thick high-*k* layers, which was to examine the role of high-*k*/IL interface and high-*k* bulk charges on the high V_{th}. It was found that V_{fb} in those devices have no significant dependence on the thickness of high-*k* layer for either nMOS or pMOS, and are substantially shifted compared to

the SiO_2 controls. This indicates that the high-*k*/IL interface and high-*k* bulk charges are not likely the cause of the high V_{th} observed in poly-Si/high-*k* devices. Finally, the authors claimed that the poly-Si/high-*k* interface is playing a major role in the high V_{th} issue, which was based on the extracted gate work function of poly-Si gate on high-*k* shown in [3]. In that paper, the high V_{th} issue induced by Fermi Level pinning effect at the poly-Si/high-*k* interface was presented for the first time.

In particular, the Fermi Level at poly-Si (no matter n^+ or p^+ poly-Si gate) interface is pinned just below the Si conduction band (E_C) in the device with HfO_2 gate dielectric, as shown in **Fig. 5.2**. This causes that the V_{th} for poly-Si/HfO_2 pMOS is much higher than the SiO_2 control, whereas the V_{th} for poly-Si/HfO_2 nMOS devices is closer to the SiO_2 control.

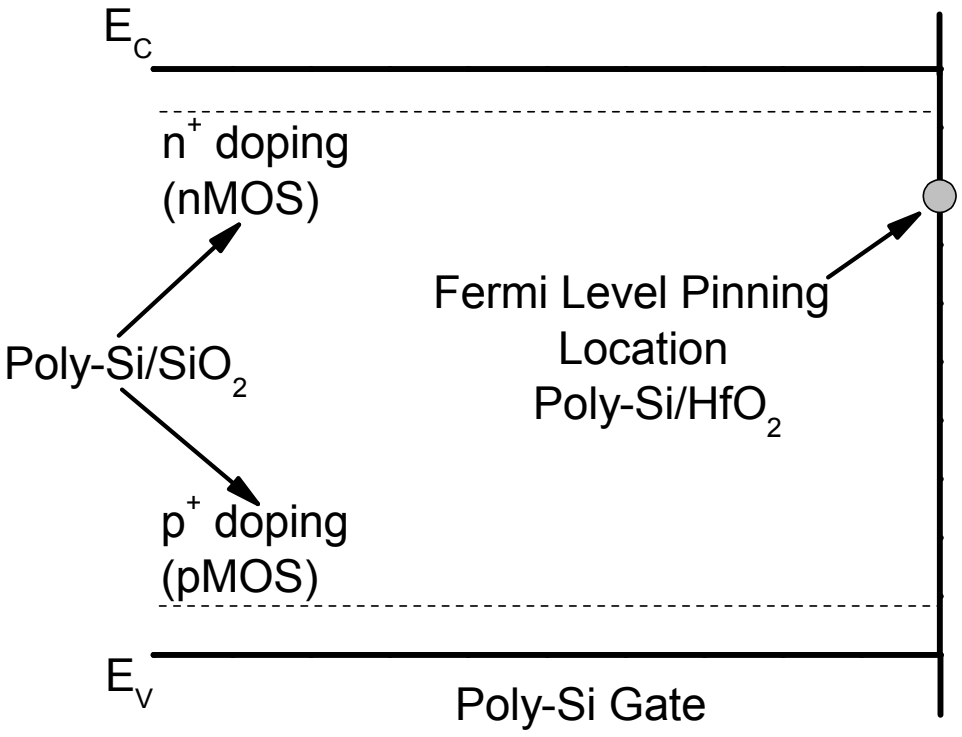


Fig. 5.2: Fermi Level Pinning Location in poly-Si/HfO_2.

In the device with Al_2O_3 gate dielectric, the Fermi Level at poly-Si (no matter n^+ or p^+ poly-Si gate) interface is pinned just above the Si valence band (E_V), as shown in **Fig. 5.3**, which induces the V_{th} for typical Al_2O_3 pMOSFET is close to the

SiO_2 control whereas the V_{th} for Al_2O_3 nMOSFET is higher than the SiO_2 control.

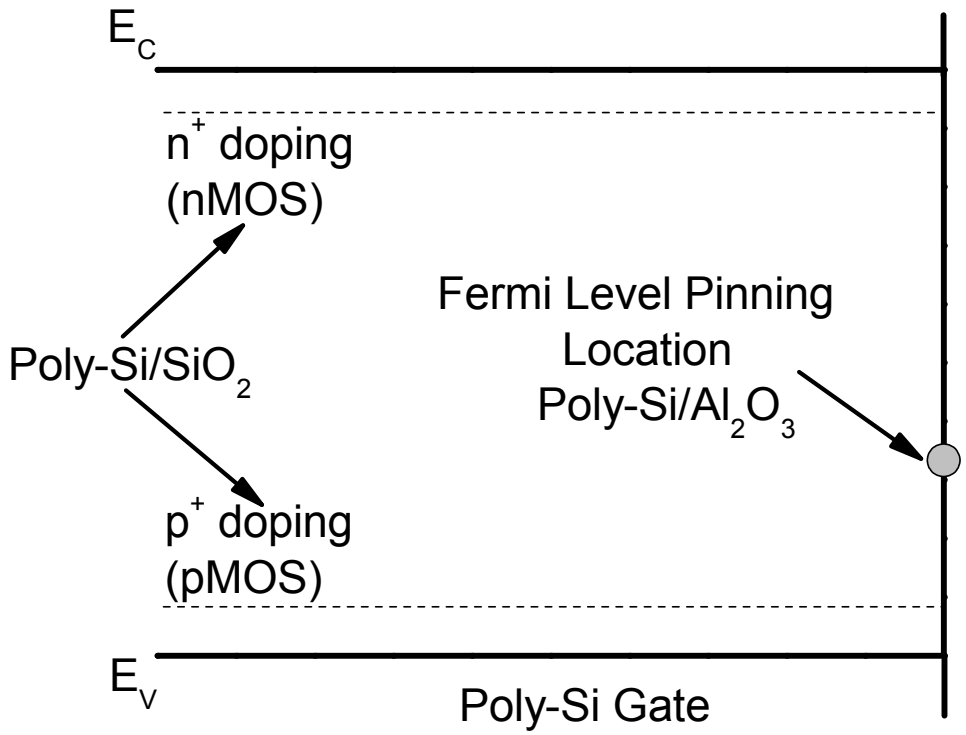


Fig. 5.3: Fermi Level Pinning Location in poly-Si/Al_2O_3.

Now, most of researchers believe that the Fermi Level pinning effect is the root of the high V_{th} issue in poly-Si/high-*k* devices.

5.2.3 Possible Mechanism of Fermi Level Pinning Effect

There are several possible mechanisms, which were proposed to explain the Fermi Level pinning induced high V_{th} in poly-Si/high-*k* devices.

5.2.3.1 Interfacial Bonding (Si-Hf or Si-O-Al Bond)

C. Hobbs et al. reported the Fermi Level pinning effect at the poly-Si/high-*k* interface for the first time [3]. In that paper, pMOS devices with n^+ and p^+ gates were fabricated with 0-20 cycles of Atomic Layer Deposition (ALD) HfO_2 on 23 Å of thermal SiO_2. As shown in **Fig. 5.4**, only one HfO_2 ALD cycle was necessary to shift

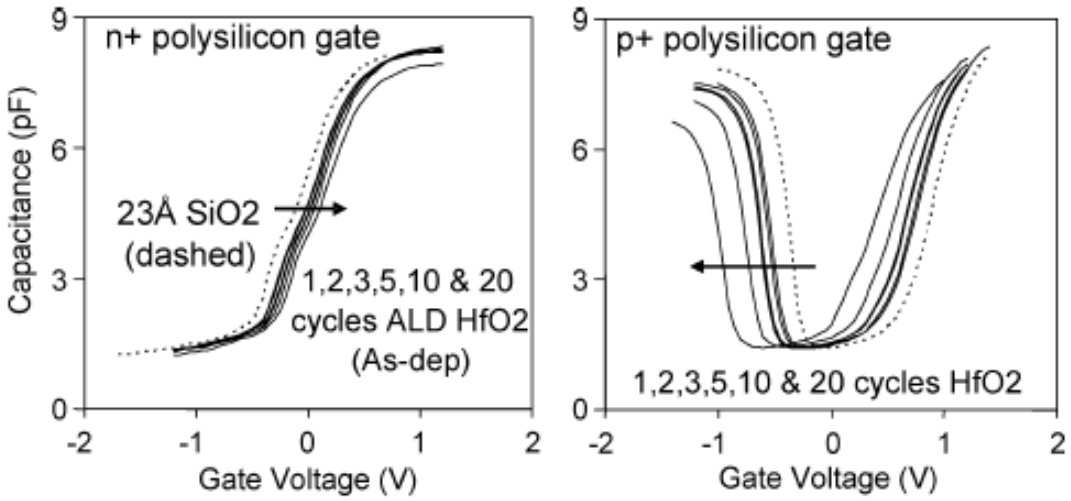


Fig. 5.4: *C-V* curves for as-deposited sub-monolayer ALD HfO_2 pMOS devices with n^+ gate (left) and p^+ gate (right). Note that for each subsequent ALD cycle, the *C-V* curve for the n^+ gate shifts to the right whereas the *C-V* curve for p^+ gate shifts to the left. [3]

the *C-V* curves. The p^+ gate *C-V* curve was shifted to the left whereas the n^+ gate *C-V* curve was shifted to the right. Subsequent ALD HfO_2 cycles continued to monotonically shift the V_{fb}. The devices with p^+ gate had a larger V_{fb} shift than those with n^+ gate. Moreover, the V_{fb} shift (ΔV_{fb}) for n^+ and p^+ gates showed strong saturation effect on the number of ALD HfO_2 cycles, as shown in **Fig. 5.5**. The initial region represented the change in the V_{fb} for increasing surface coverage of the sub-monolayer HfO_2. Once surface coverage was completed, the ΔV_{fb} became constant.

In the same paper, a similar experiment was performed using 0-10 cycles of Al_2O_3 on 23 Å SiO_2 to study the effect of the poly-Si/Al_2O_3 interface on pMOS devices with n^+ and p^+ gates. Plots of V_{fb} as a function of the number of Al_2O_3 cycles are shown in **Fig. 5.6**. Compared to the HfO_2, the Al_2O_3 had several similar characteristics: (1) only one ALD cycle was necessary to shift the V_{fb}; (2) subsequent ALD cycles continued to shift the V_{fb}; and (3) the ΔV_{fb} for n^+ and p^+ gates showed strong saturation effect on the number of ALD HfO_2 cycles. Moreover, the Al_2O_3 differed from the HfO_2 in opposite shift for n^+ and p^+ gate devices, which the devices with n^+ gate showed a larger V_{fb} shift than those with p^+ gate.

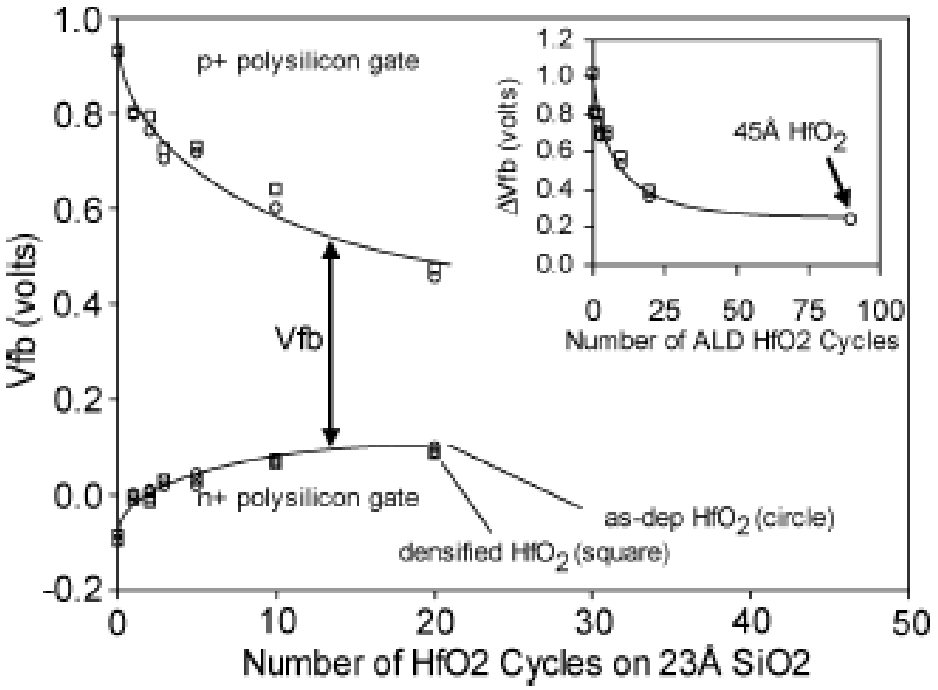


Fig. 5.5: V_{fb} versus number of HfO_2 ALD cycles. (Inset: ΔV_{fb} versus number of HfO_2 ALD cycles.) [3]

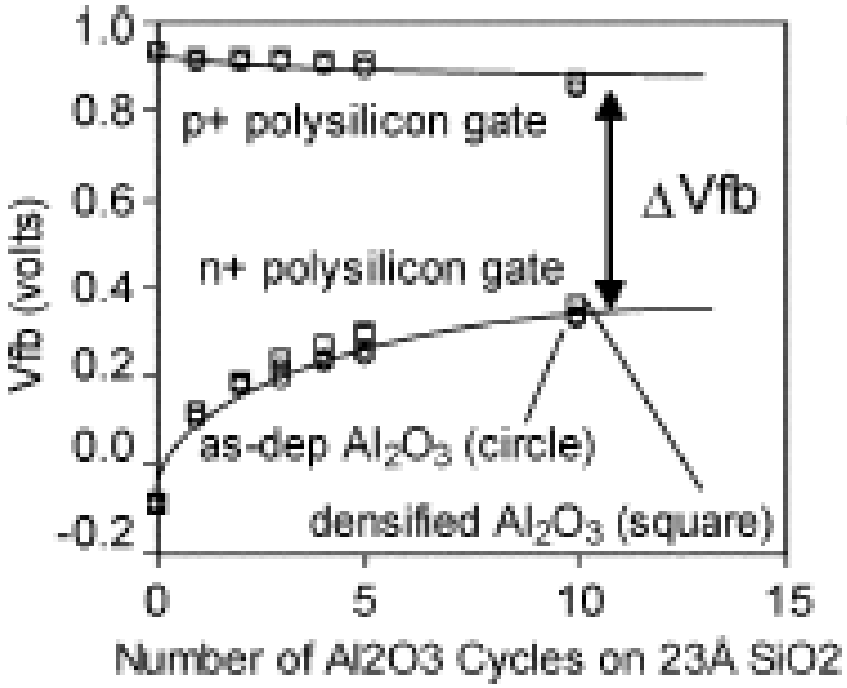


Fig. 5.6: V_{fb} versus number of HfO_2 ALD cycles. [3]

According to the results observed in the HfO_2 and Al_2O_3 gate dielectrics with poly-Si gate, C. Hobbs et al. proposed the different Fermi Level pinning locations of HfO_2 and Al_2O_3 as illustrated in **Fig. 5.2** and **5.3**. Moreover, the authors suggested that the pinning occurred due to the interfacial Si-Hf and Si-O-Al bonds for HfO_2 and Al_2O_3, respectively. For the HfO_2 gate dielectric, the interfacial Si-Hf bonds created dipoles. This pinned the Fermi Level just below the poly-Si conduction band and increased the poly-Si depletion of p^+ gates. For Al_2O_3 gate dielectrics, the Si-O-Al bonds pinned the Fermi Level just above the Si valence band. Also, the Al at the interface behaved as a dopant and increased the poly-Si depletion of n^+ gates.

However, the interfacial bonding model may not explain the experimental result which the V_{fb} difference between the devices with n^+ and p^+ gate was obviously reduced by a very small amount ALD HfO_2 deposition, as shown in **Fig. 5.5**.

5.2.3.2 HfB_2 Formation

To explain the unacceptably high V_{th} observed in the pMOS devices with Hf-based gate dielectric and poly-Si gate, T. Aoyama et al. proposed the model of HfB_2 formation [16]. Since the Fermi Level of HfB_2 was near the Si conduction band, the high V_{th} in the pMOS devices could be due to the work function of HfB_2, which was formed by chemical bonding of Hf and B at the p^+ poly-Si and Hf-based gate dielectric interface.

However, the authors also granted that the existence of HfB_2 at the top interface have not been observed yet. Hence, this model may not be a reasonable explanation for the Fermi Level pinning effect in poly-Si/high-*k* devices.

5.2.3.3 Oxygen Vacancy Formation

Removal of one oxygen atom with negative charge from a HfO_2 crystal results in generation of two surplus electrons basically in Hf *5d* levels, as shown in **Fig. 5.7**. This is the universal nature of ionic crystals and much different from covalent SiO_2 in which oxygen vacancy (*Vo*) formation mainly results in local structural changes such

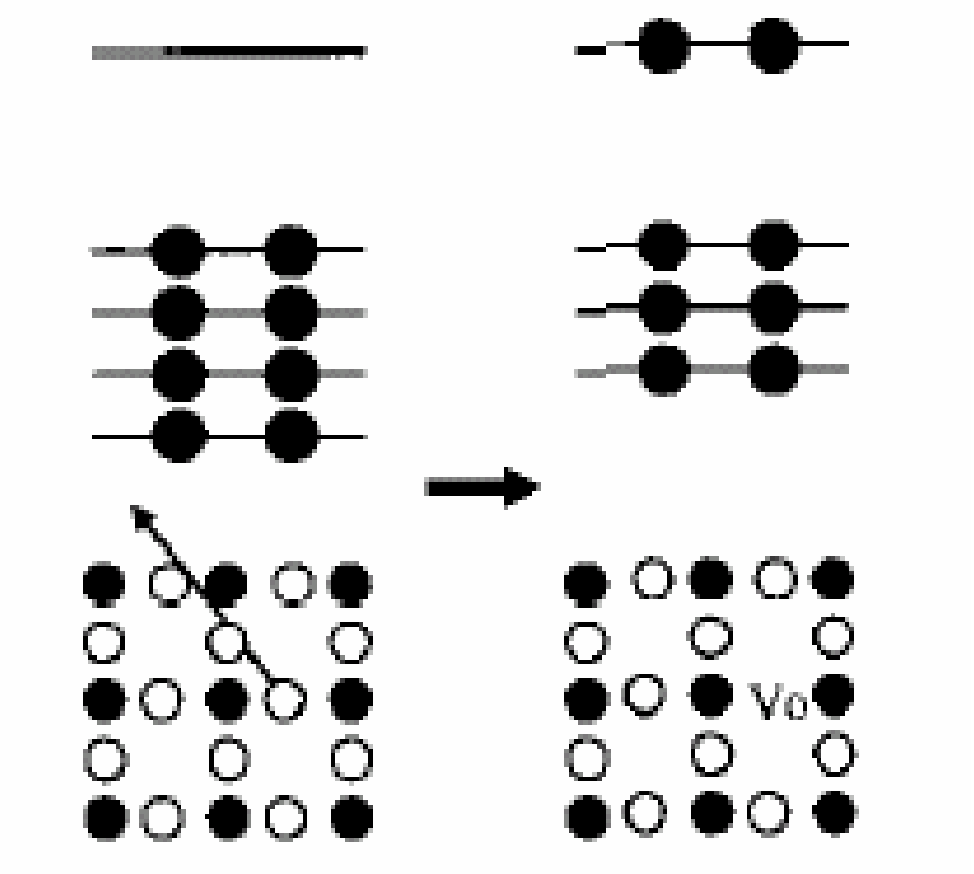


Fig. 5.7: Schematic illustration of generation of two surplus electrons by *Vo* formation in HfO_2. [21]

as Si-Si bond formation [17]. The generation of surplus electron induced by *Vo* formation may cause remarkable increase in electron entropy, and effectively reduce the formation energy of *Vo*. This implies that further formation of *Vo* may be easy in HfO_2. The formation of associated electron traps induced by oxygen vacancies has also been reported for many other metal oxides, such as ZrO_2 [18], TiO_2 [19], and Ta_2O_5 [20].

If the oxygen vacancies are formed near the poly-Si/HfO_2 interface, the generated electrons may transfer across the interface and induce an interface dipole, as shown in **Fig. 5.8**. A recent publication [21] suggests that the oxygen transport out of high-*k* gate dielectric into Si results in oxygen vacancies and associated electron traps within the dielectric, as well as the formation of a dipole at the poly-Si/high-*k* interface, which causes the Fermi level pinning and increased V_{th}.

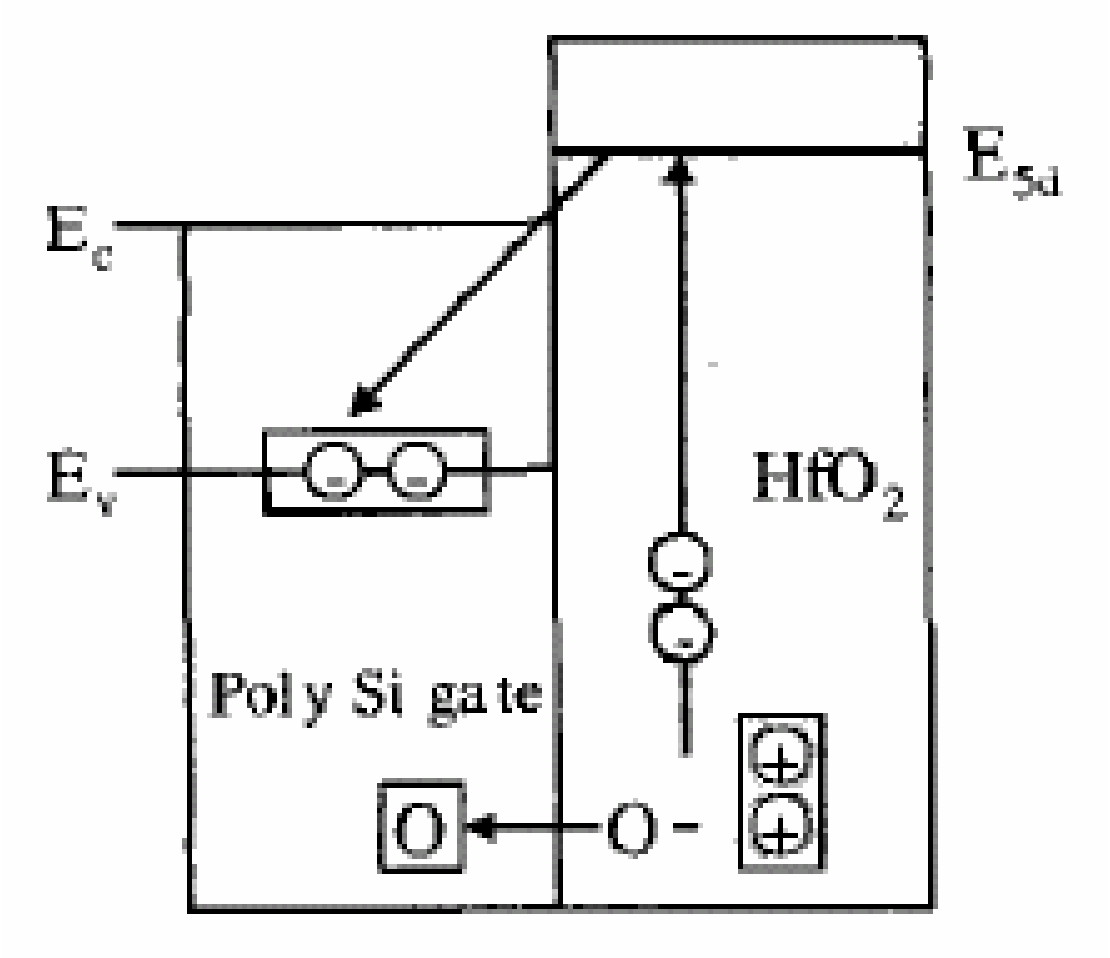


Fig. 5.8: Schematic illustration of *Vo* formation and subsequent electron transfer across the interface in poly-Si/HfO_2 structure. [21]

Since the oxygen vacancy model shows good agreement with experimental results, it is commonly believed that the formation of oxygen vacancy and associated electron traps within the high-*k* dielectric may be the intrinsic origin of the high V_{th} issue observed in poly-Si/high-*k* devices.

5.3 Poly-SiGe for Gate Electrode Application

5.3.1 Background of Poly-SiGe Gate

In recent years, the continuing miniaturization of Si MOSFET for increased chip packing density and performance has resulted in significant research efforts in suppression of so-called "short-channel effect" (SCE). The SCE, which are caused by an increased influence of the drain potential on the source depletion region, may result in low V_{th} issue (V_{th} roll-off behavior) in short channel devices. The SCE effect is usually tackled by raising the substrate doping level to reduce the lateral extension of the drain depletion region. This, however, can result in significant deterioration of performance of the transistors: the reduced carrier mobility in a heavily doped region results in a decreased current drivability (I_{Dsat} or I_{ON}) of the devices, while the subthreshold swing (*ss*) is increased, resulting in higher level of off-state leakage currents (I_{OFF}).

Heavily-doped n- and p-type poly-Si gates (dual poly-Si gate) have been conventionally used in modern CMOS technologies. This dual gate technology offers several advantages, including reduced SCE by surface-channel operation of both nMOS and pMOS devices, and low and symmetrical V_{th} for low-power operation. However, new problems such as the poly-gate-depletion effect (PDE) and boron penetration emerge as the dimensions of devices enter the deep-submicron regime. In the deep-submicron devices, the gate dielectric thickness is very thin, and then the PDE and boron penetration have become critical issues. The approaches contradict each other to suppress the PDE and boron penetration by controlling the poly-Si gate doping and annealing condition. These technical problems impose strict limitations on the process window and therefore the resultant device performance [22, 23].

Poly-SiGe has been widely reported as an alternative gate electrode over the conventional poly-Si gate due to low temperature for dopant activation, low gate sheet resistance, suppressed PDE and boron penetration [24-30]. It is also well known that the poly-SiGe gate has good compatibility with the standard CMOS process and the

dopant activation in poly-SiGe is comparable to poly-Si gate [24]. Therefore, poly-SiGe is a promising material for advanced dual gate application.

5.3.2 Review of Literature

T. J. King et al. reported that the resistivity of the boron-doped poly-SiGe film, which decreases with increasing Ge content, is substantially lower than that of the poly-Si film. In contrast, the resistivity of phosphorus-doped poly-SiGe film decreases only slightly with increasing Ge content for Ge mole fractions below ~45%, and increases considerably for higher Ge mole fractions [25], as shown in **Fig. 5.9**.

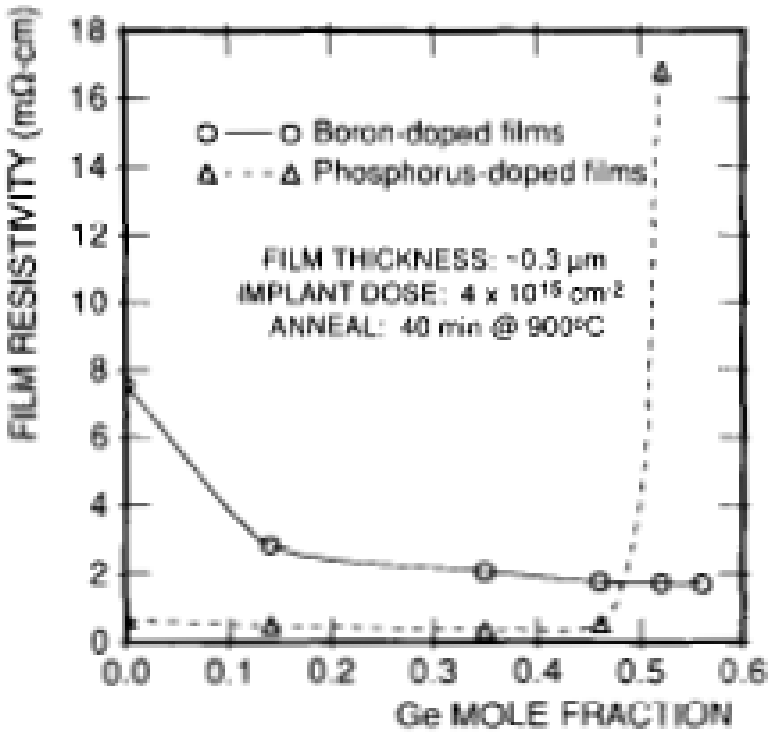


Fig. 5.9: Resistivity of heavily doped poly-SiGe films. [25]

The authors also demonstrated that the anneal temperature required to activate the boron decreases dramatically with increasing Ge content in the film, as shown in **Fig. 5.10**. For example, the resistivity of the SiGe film with 52% Ge annealed at 500 °C for 60 sec is almost same as that of the Si film annealed at 900 °C and 1000 °C for 30 sec [25]. Alternatively, much lower implant doses of boron can be used for poly-SiGe films than for poly-Si films to achieve the same film resistivity. For the application of poly-SiGe as a gate electrode material, these reductions in required dose and anneal temperature can help to alleviate the problem of boron penetration in boron-doped gate CMOS technology.

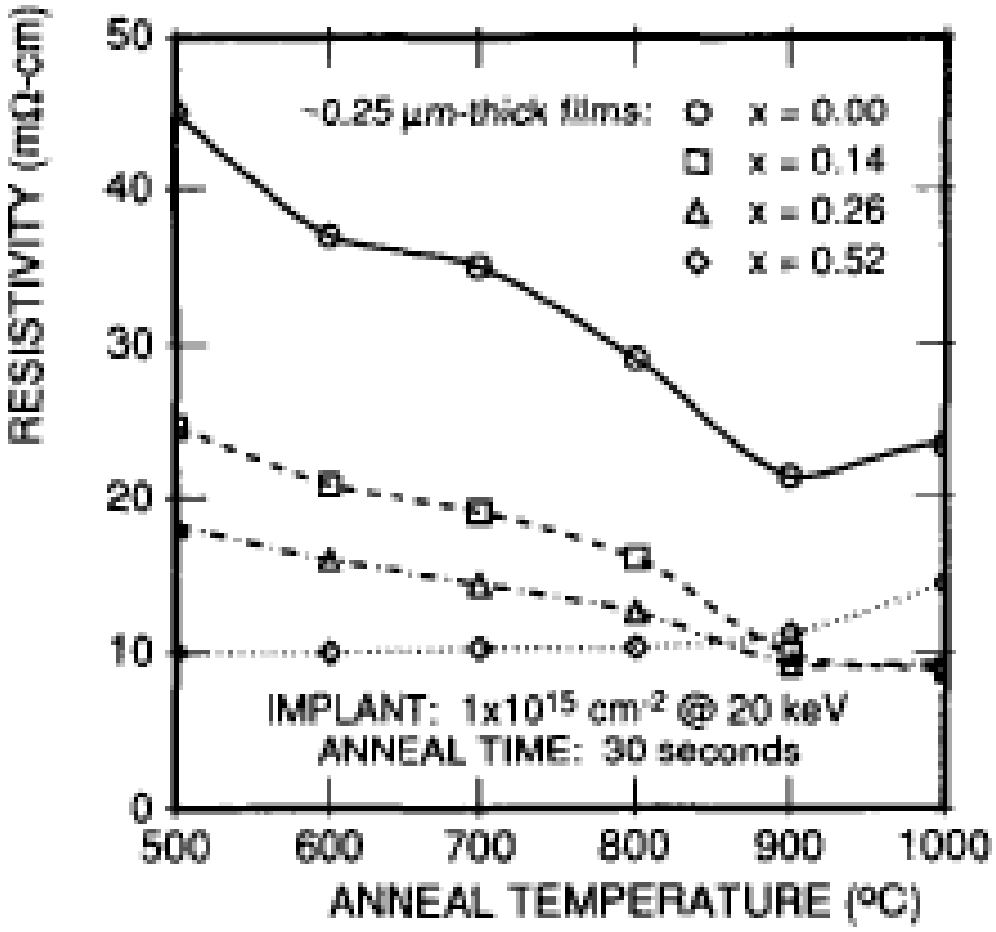


Fig. 5.10: Resistivity of poly-SiGe films implanted with boron and then annealed for 30 sec each at successively higher temperatures. [25]

The low resistivity observed in n- and p-type poly-SiGe gates is due to the enhanced activation of dopants compared to poly-Si gate. W. C. Lee et al. reported that [27]:

(1) For phosphorus-doped (n-type) poly gates, the active dopant concentration reaches its maximum value at ~20% Ge content for various gate implant doses, which might result from the competition between increased secondary grain growth and lower phosphorus solid solubility with higher Ge content in poly-SiGe.

(2) For boron-doped (p-type) poly gates, the active dopant concentration shows a rapid increase as Ge content increases up to 20% and then a slower increase for higher Ge contents, which may be attributed to the increasing grain size with Ge content.

In the conventional poly-Si gate, there is a trade off between boron penetration and PDE. Higher boron implant dose (or higher annealing temperature) would improve PDE but worsen the boron penetration issue. In the poly-SiGe gate, the PDE is effectively suppressed due to the high dopant activation rate and low sheet resistance. The boron penetration is also alleviated in poly-SiGe gate, which may be attributed to the large grain size in SiGe film attained after post annealing and then less grain-boundary-enhanced diffusion. Therefore, both boron penetration and PDE can be improved simultaneously by substituting a SiGe gate for the Si gate at the same gate doping level. A large process window also exists for the p-type SiGe gated devices to obtain sufficiently high active boron concentration to suppress PDE without significant boron penetration through the gate oxide.

Compared to poly-Si gate, the work function of p^+ poly-SiGe decreases significantly, whereas the work function of n^+ poly-SiGe decreases only slightly, as Ge content is increased [25]. A comparison of the conduction-band and valence-band energy levels in bulk crystalline Si, SiGe, and Ge materials is shown in **Fig. 5.11** [15]. (The energy levels in SiGe are assumed to be intermediate to those in Si and Ge.) Si and Ge have similar electron affinities, however, Ge has a much smaller bandgap. Therefore, a relatively large energy difference (>0.5eV) exists between the valence-band edges of Si and Ge. The work function $q\Phi$ is defined to be the

difference between the free-electron (vacuum) energy E_0 and the Fermi level E_f. Since the Fermi level position is close to the conduction-band in a heavy doped n-type semiconductor, whereas is close to the valence-band in a heavy doped p-type semiconductor, the work function of n^+ SiGe can be expected to decrease only slightly with increasing Ge content, whereas the work function of p^+ SiGe can be expected to decrease noticeably with increasing Ge content.

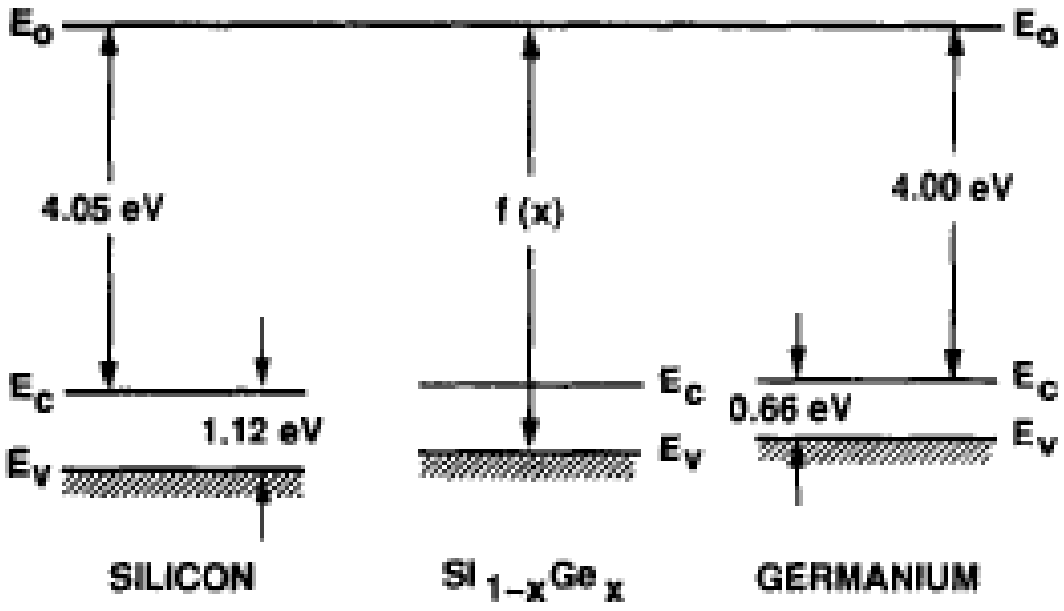


Fig. 5.11: Comparison of energy band levels in Si, SiGe, and Ge. [15]

W. C. Lee et al. also reported the variations of work function for n-type, p-type poly-SiGe gates, and the reduction in energy bandgap with Ge content [27], as shown in **Fig. 5.12**. For n^+ poly-SiGe gate, the variation of work function was negligible with increasing Ge content; while for p^+ poly-SiGe gate, the work function was significantly reduced as Ge content increases. The energy bandgap of the poly-SiGe gate was found to decrease with increasing Ge content. Assuming the work function of n^+ and p^+ poly-Si gate are 4.05 and 5.17 eV respectively (normal case in dual poly-Si gate process), then the work function of poly-SiGe gates may be easily calculated based on W. C. Lee's experimental results, as summarized in **Table 5.1**.

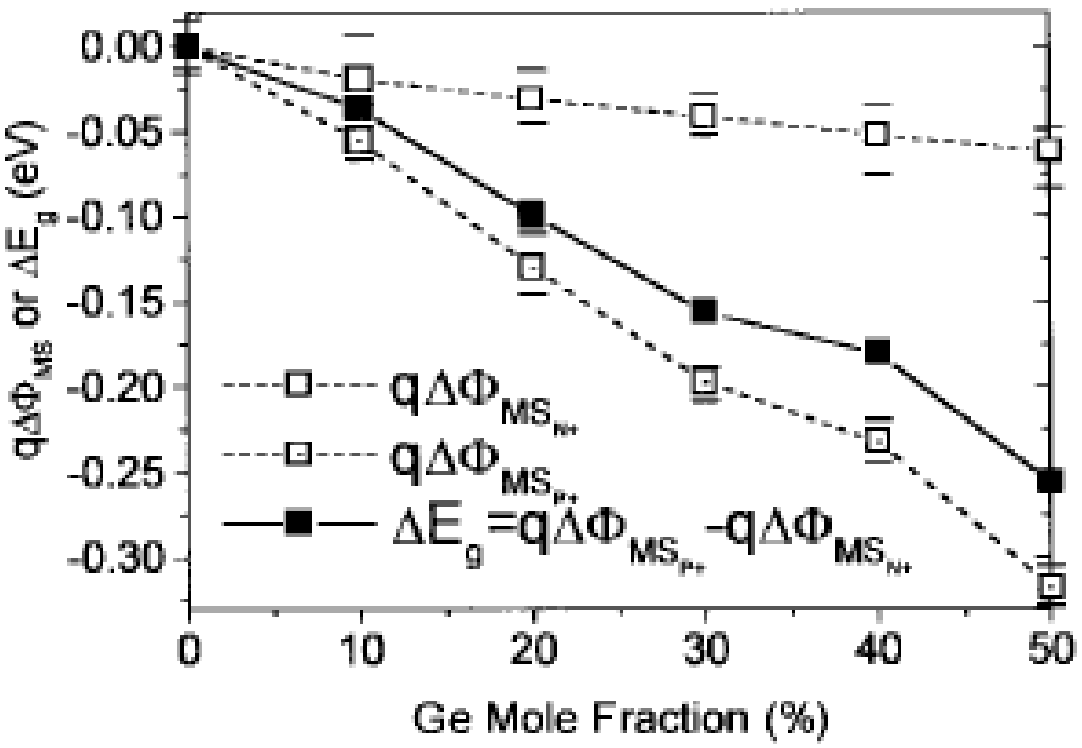


Fig. 5.12: Reduction in poly-SiGe energy bandgap as a function of Ge mole fraction. The error bars represent the deviation of Φ_{MS} for each poly-SiGe film. [27]

Table 5.1: Variations of work function (WF) for n^+ and p^+ poly-SiGe gates with increasing Ge content. (Based on the experimental results in **Fig. 5.12**)

Poly-$Si_{1-x}Ge_x$	**WF for n^+ gate**	**WF for p^+ gate**	**Energy bandgap**
Poly-Si	~4.05 eV	~5.17 eV	1.12 eV
10% Ge	~4.03 eV	~5.11 eV	1.08 eV
20% Ge	~4.02 eV	~5.04 eV	1.02 eV
30% Ge	~4.01 eV	~4.97 eV	0.96 eV
40% Ge	~4 eV	~4.94 eV	0.94 eV
50% Ge	`~3.99 eV	~4.85 eV	0.86 eV

(Assuming WFs for n^+ and p^+ poly-Si gates are 4.05 and 5.17 eV, respectively.)

According to the work function summarized in **Table 5.1**, in poly-SiGe/SiO_2 devices, the V_{th} for nMOS would be slightly decreased, whereas the V_{th} for pMOS would be increased by increasing Ge content [28].

Compared to the devices with poly-Si gate, the poly-SiGe gated devices showed slight improvement on drive current for nMOS and noticeable improvement on pMOS performance [29, 30]. The slight improvement on the nMOS current drivability is caused by better n-type gate activation, and the noticeable improvement on pMOS performance is mainly due to the smaller gate work function of poly-SiGe, which leads to a lower E_{eff}, and therefore improved current drive [29].

In summary, compared to the conventional poly-Si gate, the poly-SiGe gate shows lower sheet resistance, suppressed PDE, good immunity to boron penetration, and also improved device performance, in particular for pMOS. Since the poly-SiGe gate has good compatibility with standard CMOS process, it is therefore a promising material for advanced dual gate CMOS application.

5.4 Suppression of Fermi Level Pinning in Poly-SiGe/high-*k*

5.4.1 Background

It is well known that the Fermi level pinning induced unacceptably high V_{th}, in particular for pMOSFET, is a serious challenge for integration of the HfO_2-based gate dielectrics into the mature poly-Si gate process [3]. To overcome this issue, a HfSiON film with Hf-gradient-profile has been proposed, however, this approach limits the *EOT* scaling because a HfSiON film with low *k* value (Hf content below 10%) is needed at the poly-Si gate and dielectric interface [31]. Also, it has been reported that the insertion of ultra-thin Al_2O_3 between HfSiO and poly-Si can effectively reduce V_{th} in pMOSFET, but the V_{th} in nMOSFET increased [32]. Recently, a symmetrical V_{th} (±0.5 V) was achieved by dual gate dielectrics of HfSiON for nMOSFET and Al_2O_3/HfSiON for pMOSFET [33]. Unfortunately, the process integration of this approach becomes more complicated since it needs to deposit two different gate

dielectrics on the same wafer.

In this study, the V_{th} for three gate stacks of poly-Si/HfO_2 (SH), poly-Si/Al_2O_3/HfO_2 (SAH) and poly-Si/poly-SiGe/Al_2O_3/HfO_2 (GAH) were examined for both nMOS and pMOSFET. Acceptable V_{th} of 0.3 V for nMOSFET and -0.49V for pMOSFET were successfully achieved in the GAH gate stack. Moreover, the transconductance (G_m) and V_{th} stability in the GAH gate stack were remarkably improved compared to the SH and SAH devices. It is believed that the low V_{th} and good V_{th} stability observed in GAH gate stack may be mainly due to the effective suppression of Fermi Level pinning at the poly-SiGe/high-*k* interface.

5.4.2 Experiment

The nMOS and pMOSFET were fabricated on 6-inch Si (100) wafers with a resistivity of 10 ohm-cm using a conventional self-aligned MOSFET process. After standard Radio Corporation of American (RCA) clean, three gate stacks of SH, SAH, and GAH were deposited. **Table 5.2** summarizes the process flow of the three gate stacks formation. Metal organic chemical vapor deposition (MOCVD) and Atomic Layer Deposition (ALD) systems were used to deposit the HfO_2 and Al_2O_3 films respectively, and followed by post deposition annealing (PDA) in NH_3 ambient

Table 5.2: The process flow of poly-Si/HfO_2 (SH), poly-Si/Al_2O_3/HfO_2 (SAH) and poly-Si/poly-SiGe/Al_2O_3/HfO_2 (GAH) gate stacks formation. The Ge content is ~30% in SiGe gate.

Gate stack	Poly-Si/HfO_2	Poly-Si/Al_2O_3/HfO_2	Poly-Si/Poly-SiGe/ Al_2O_3/HfO_2
IL (RTO SiO_2)	~0.6 nm	~0.6 nm	~0.6 nm
MOCVD HfO_2	~4.0 nm	~2.5 nm	~2.5 nm
ALCVD Al_2O_3	0	~0.7 nm	~0.7 nm
PDA	NH_3, 700ºC, 30s	NH_3, 700ºC, 30s	NH_3, 700ºC, 30s
Gate	Si~150 nm	Si~150 nm	Si/SiGe~100/50 nm
EOT	~2 nm	~2 nm	~2 nm

at 700 ºC for 30 sec to incorporate N into the high-*k* gate dielectrics (N content~5%). Si and SiGe films were deposited as gate electrodes by low-pressure chemical vapor deposition (LPCVD) at 540 ºC and 600 ºC, respectively. The composition of SiGe film with 30% Ge was examined by X-ray photoelectron spectroscopy (XPS). After gate patterning, arsenic and BF_2^+ were implanted for nMOS and pMOSFET, and followed by activation annealing at 900 ºC. Finally, alloy was carried out at 400 ºC after Al metallization.

5.4.3 Suppressed Fermi Level Pinning by Poly-SiGe Gate

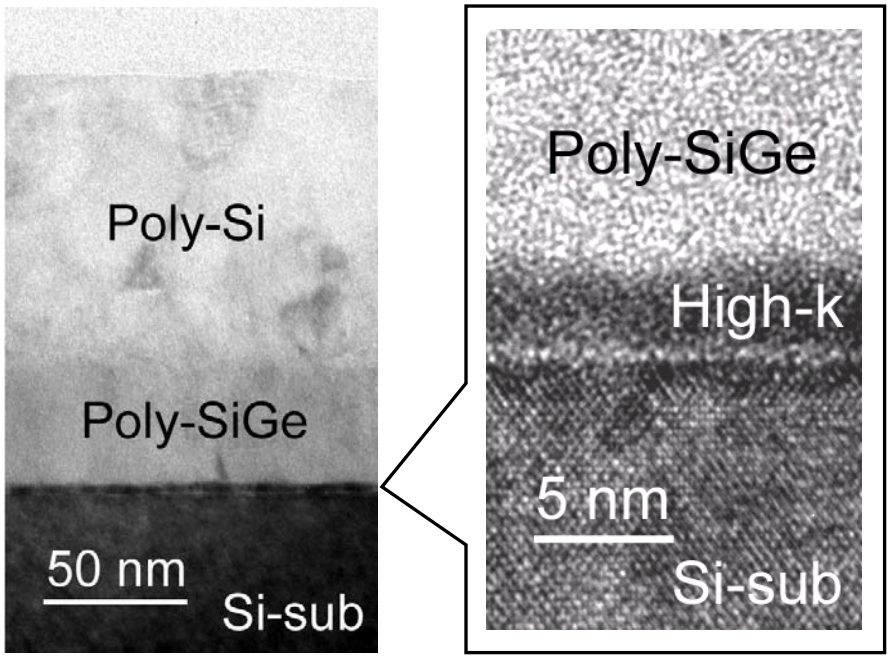


Fig. 5.13: TEM image of poly-Si/poly-SiGe/Al_2O_3/HfO_2 (GAH) gate stack (left) and high resolution TEM image of the high-*k* gate dielectric of Al_2O_3/HfO_2 (right).

Fig 5.13 shows the transmission electron microscopy (TEM) images of GAH gate stack (left) and the high resolution TEM image of Al_2O_3/HfO_2 gate dielectric (right). In order to reduce the SiGe surface roughness, a thin amorphous Si layer (Si seed layer) deposition prior to the SiGe growth was commonly used in the case of the SiGe growth on the SiO_2. However, as shown in **Fig. 5.13**, a smooth SiGe film is obtained on the Al_2O_3/HfO_2 even without the Si seed layer, which is consist with other

group's report [34]. Considering the facts of good thermal stability at poly-Si/Al_2O_3 interface [35], excellent dopants penetration immunity of Al_2O_3 [36], sufficient high permittivity of HfO_2 (~25), and superior interface properties at SiO_2/Si-substrate, the high-*k* gate dielectric in GAH was optimized as Al_2O_3/HfO_2 with SiO_2 interfacial layer. **Fig. 5.14** shows the SIMS profiles of Al, Hf, Si, and N in the gate stack of Al_2O_3/HfO_2 with SiO_2 interfacial layer. A high Al concentration at the top surface and a high Si concentration at the bottom surface were confirmed in this gate stack.

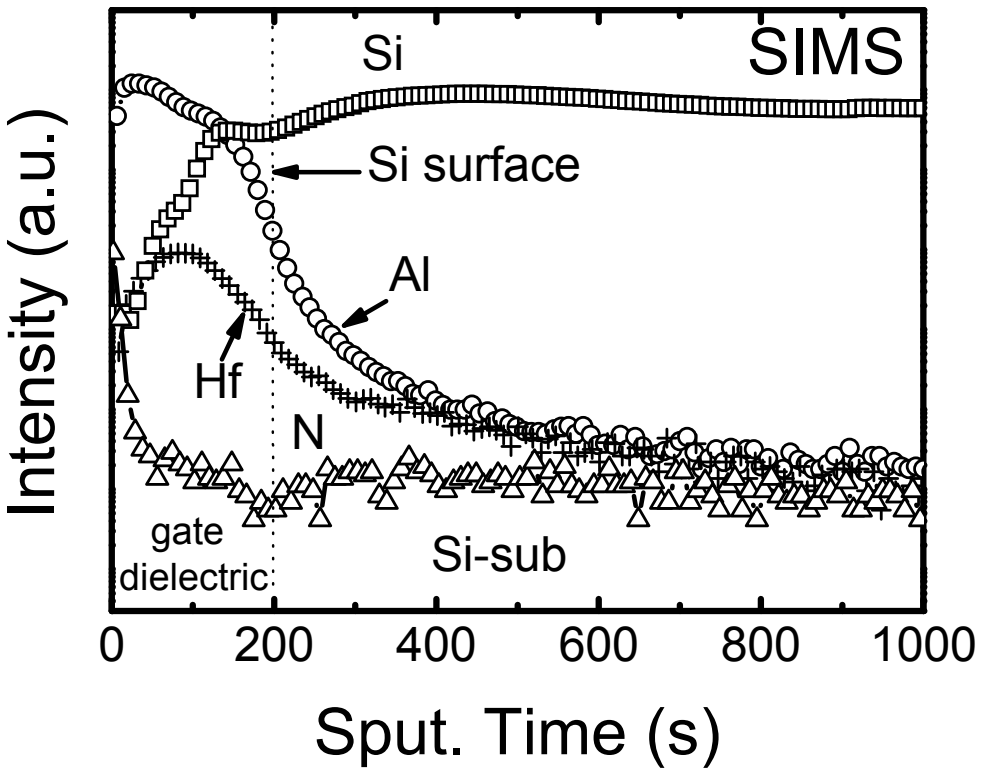
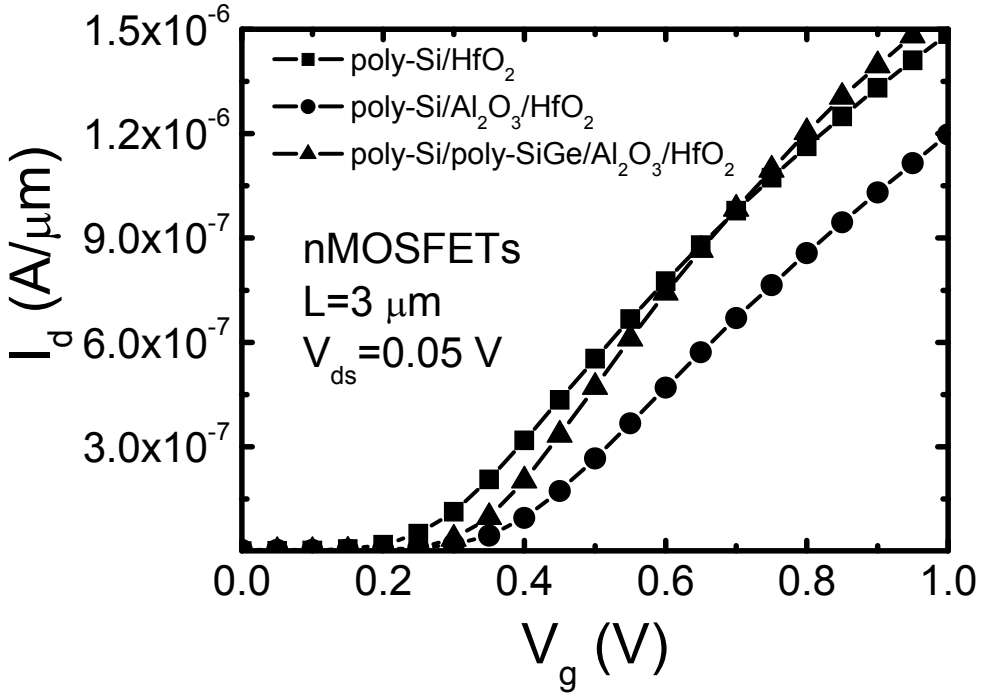
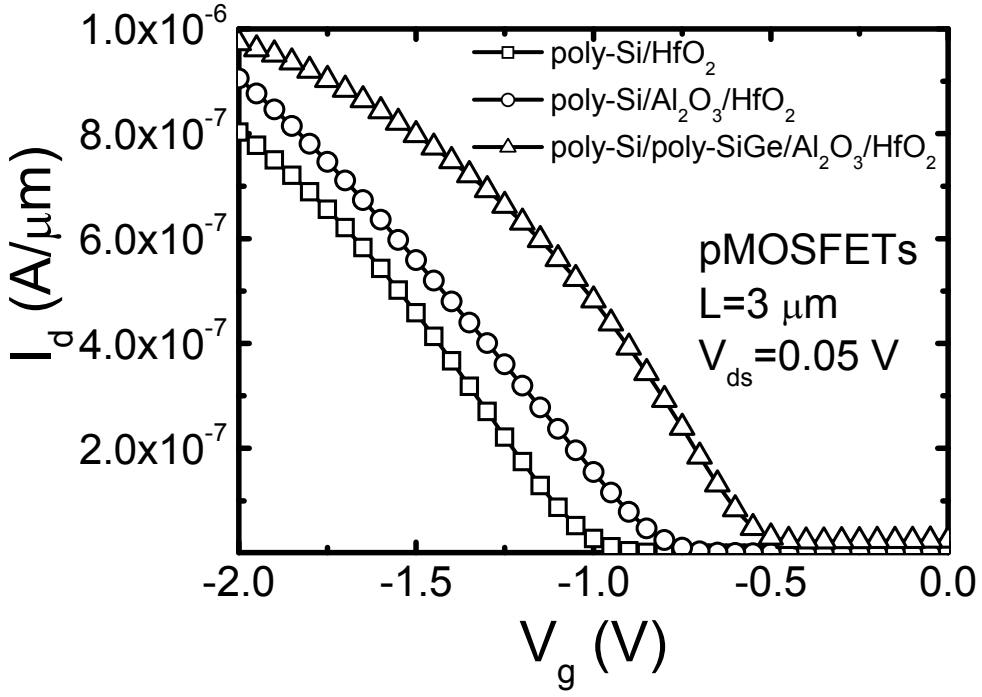


Fig. 5.14: SIMS profiles of Al, Hf, Si, and N in Al_2O_3/HfO_2/SiO_2 gate stack after activation annealing at 900 ºC. The concentration of N incorporated by PDA is around 5% (XPS result).

Fig. 5.15 (a) and (b) show the drain current versus gate voltage (I_D-V_G) characteristics of nMOS and pMOSFETs with the SH, SAH, and GAH gate stacks, respectively. As can be seen in **Fig. 5.15** (a), the V_{th} for nMOSFET with SH gate stack was increased from 0.27 to 0.37 V after inserting the Al_2O_3 capping layer, and then



(a)



(b)

Fig. 5.15: (a) I_D-V_G curves for nMOSFETs with SH, SAH and GAH gate stacks. The V_{th} for SH, SAH, and GAH nMOSFETs are 0.27, 0.37 and 0.30 V, respectively.
(b) I_D-V_G curves for pMOSFETs with SH, SAH and GAH gate stacks. The V_{th} for SH, SAH, and GAH pMOSFETs are -1.02, -0.81 and -0.49 V, respectively.

decreased to 0.3 V for GAH gate stack. In **Fig. 5.15** (b), the V_{th} for SH pMOSFET was tuned from -1.02 to -0.81 V by inserting the Al_2O_3 capping layer, then further reduced to -0.49 V by using poly-SiGe gate. The tunable V_{th} for both nMOS and pMOSFETs are summarized in **Fig. 5.16**. It is well known that both HfO_2 and Al_2O_3

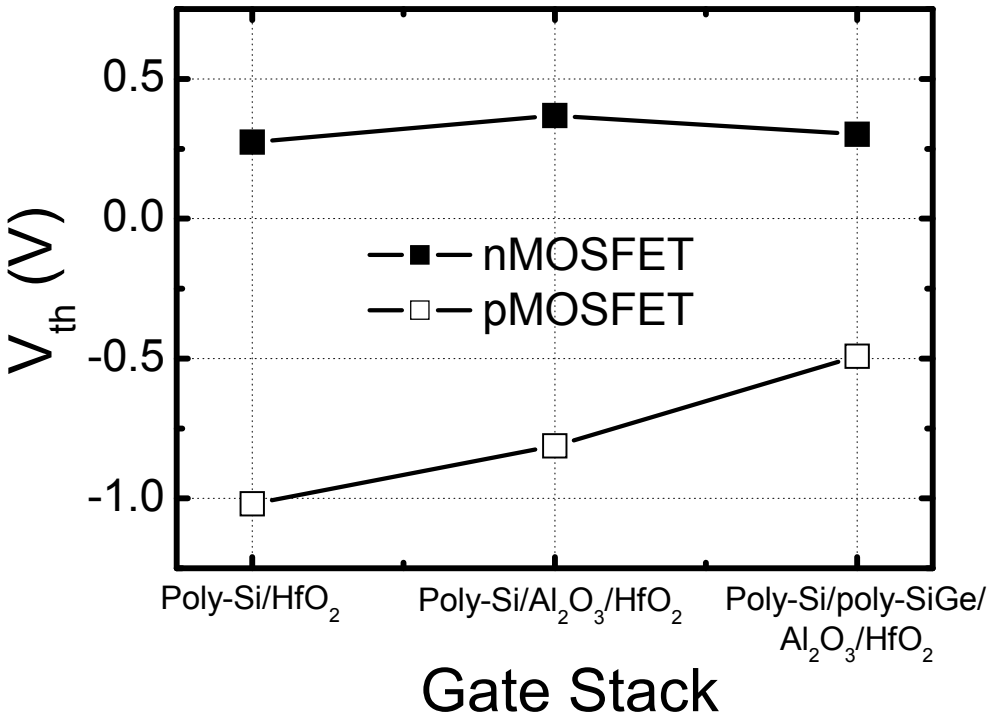


Fig. 5.16: Comparison of V_{th} for both nMOS and pMOSFETs with SH, SAH, GAH gate stacks. The V_{th} is tunable by using the poly-SiGe gate and Al_2O_3 capping layers.

exhibit the Fermi level pinning effect at the poly-Si/metal oxide interface, and the Fermi level pinning positions for HfO_2 and Al_2O_3 are located near the conduction and valence band, respectively [3]. As a result, there is no significant impact of the Fermi level pinning on the V_{th} for poly-Si/HfO_2 nMOSFET, however, the V_{th} for poly-Si/HfO_2 pMOSFET becomes unacceptably high. Conversely, the poly-Si/Al_2O_3

pMOSFET provides a reasonable V_{th} whereas the V_{th} for poly-Si/Al_2O_3 nMOSFET is higher than the expectation. As shown in **Fig. 5.16**, the V_{th} for poly-Si/HfO_2 pMOSFET was reduced by inserting the Al_2O_3 capping layer, while the V_{th} for the nMOSFET was slightly increased. Due to the asymmetrical pinning positions between HfO_2 and Al_2O_3, the impact of the Al_2O_3 capping layer on V_{th} for pMOS is stronger than nMOS, which is consist with other groups' results [32, 37]. Moreover, the V_{th} for SAH nMOSFET decreased slightly (from 0.37 to 0.3 V) and the V_{th} for the pMOSFET remarkably reduced (from -0.81 to -0.49 V) after inserting the poly-SiGe gate. This result contradicts the previous observation in SiO_2 devices, in which the replacement of poly-Si by poly-SiGe gate may decrease the V_{th} for nMOSFET slightly and increase the V_{th} for pMOSFET due to the variety of gate work function [28]. The contradiction shown in pMOSFET may be due to the effective suppression of Fermi level pinning effect at poly-SiGe/high-*k* interface. It is well known that the V_{th} behavior in poly-Si/high-*k* device is dominated by the Fermi level pinning effect, which is different to SiO_2 case [3]. A reasonable mechanism suggests that the oxygen transport out of high-*k* gate dielectric into Si results in oxygen vacancies and associated electron traps within the dielectric, as well as the formation of a dipole at the poly-Si/high-*k* interface, which causes the Fermi level pinning and increased V_{th} [21]. Takeuchi et al. further pointed out that the oxygen transport out of high-*k* is easy to occur in contact with Si rather than Ge because of the larger Gibbs free energy change for Ge [38]. This theory can systematically explain our findings of the suppressed Fermi level pinning by inserting the poly-SiGe gate since the poly-SiGe gate can retard the oxygen transport out of the high-*k* and formation of oxygen vacancies compared to the poly-Si gate. Hence, the reduction in V_{th} for pMOSFET observed in GAH stack may result from the competition between the increased V_{th} due to the reduced gate work function and the effectively suppressed Fermi level pinning by inserting the poly-SiGe gate.

Fig. 5.17 compares the G_m characteristics which are corresponding to the I_D-V_G curves shown in **Fig. 5.15**. It was found that the GAH gate stack provides higher G_m compared to SH and SAH, in particular for the pMOSFET. This is

consistent with previous reports in [29, 30].

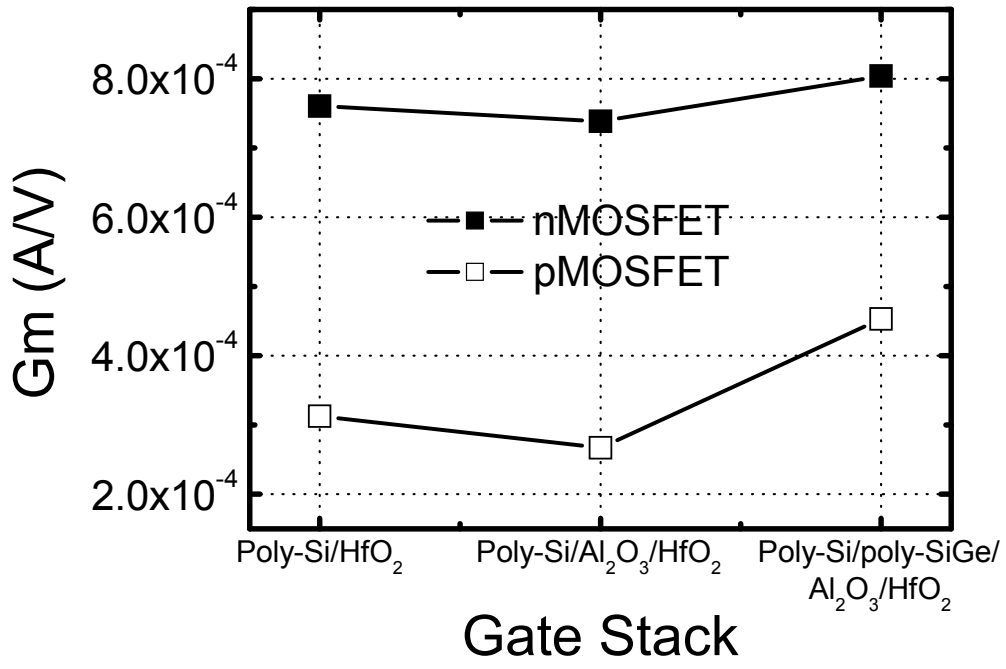
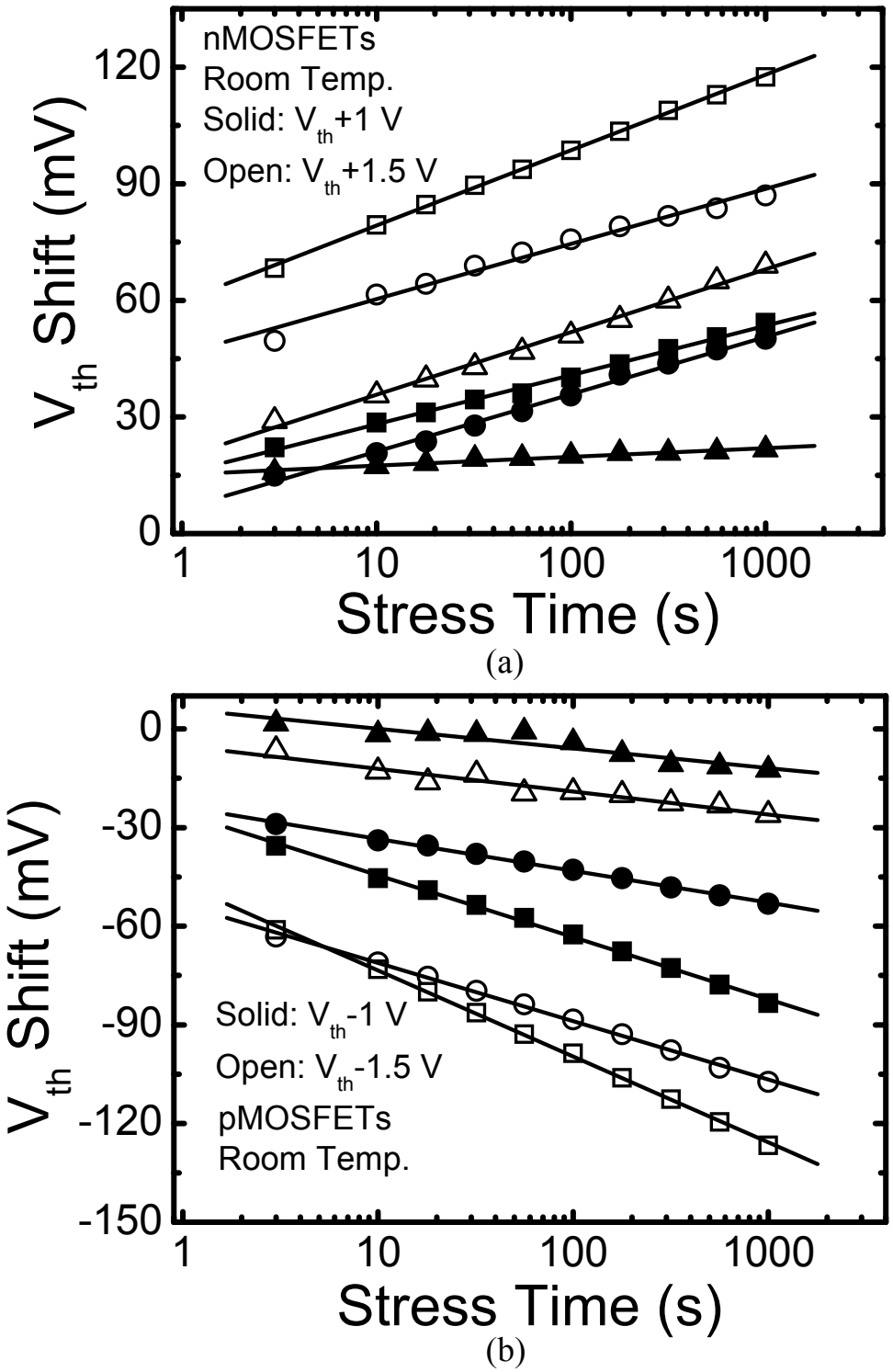


Fig. 5.17: Comparison of G_m for both nMOS and pMOSFETs with SH, SAH, and GAH gate stacks. The G_m in GAH gate stack is higher than in SH and SAH, in particular for pMOSFETs.

In addition, HfO_2-based gate dielectrics exhibit significant charge trapping and de-trapping, which causes the V_{th} instability during operation, is also a key integration challenge for their application in future CMOS technology. **Fig. 5.18** shows comparison of the V_{th} instability for (a) nMOS and (b) pMOSFETs with SH, SAH, and GAH gate stacks. The constant voltage stresses of $V_{th} \pm 1$ and $V_{th} \pm 1.5$ V were applied at the gate electrode and the conventional DC measurement was used to examine the V_{th} shift. It was found that the V_{th} shifts in GAH gate stack are much lower than those in SH and SAH under the same constant voltage stress. This result indicates that the GAH gate stack exhibits better V_{th} stability and lower traps compared to SH and SAH, which also appears to confirm the suppressed formation of oxygen vacancies and associated electron traps by using the poly-SiGe gate electrode.



■, □ Poly-Si/HfO_2; ●, ○ Poly-Si/Al_2O_3/HfO_2; ▲, △ Poly-Si/Poly-SiGe/Al_2O_3/HfO_2

Fig. 5.18: Comparison of the V_{th} instability for (a) nMOS and (b) pMOSFETs with SH, SAH and GAH gate stacks. The GAH gate stack shows good V_{th} stability compared to SH and SAH gate stacks.

5.5 Conclusion

The critical issue of unacceptably high V_{th} induced by Fermi Level pinning at poly-Si/high-*k* interface was introduced. This may be the most challenging issue for integration of advanced HfO_2-based gate dielectrics into the conventional dual poly-Si gate CMOS process.

In this study, we have demonstrated that the unacceptably high V_{th} induced by the Fermi level pinning at poly-Si/high-*k* interface was effectively suppressed by inserting a poly-SiGe gate electrode. The V_{th} of 0.3 V for nMOSFET and -0.49 V for pMOSFET was successfully achieved in poly-Si/poly-SiGe/Al_2O_3/HfO_2 devices. The G_m and V_{th} stability were also improved by using the poly-SiGe gate. Since the poly-SiGe gate is fully compatible with the mature poly-Si gate process, the application of poly-SiGe gate could be a promising solution for the integration of high-*k* gate dielectric into the conventional CMOS process. Moreover, the results observed in this experiment could be very useful for further exploring the origin of the Fermi Level pinning effect in high-*k* gate dielectric.

Restricted by the equipment for deposition of poly-SiGe film used in this work, however, the electrical characteristics of poly-SiGe gated devices may not be completely examined by comparing to conventional poly-Si gated devices. Moreover, the effects of Ge content in poly-SiGe gate and thickness of Al_2O_3 capping layer on Fermi Level pinning induced V_{th} shift are not investigated in this study. Therefore, further work should be done to confirm the results presented in this study, and also explore the effects of the Ge content in poly-SiGe gate and thickness of Al_2O_3 capping layer on the Fermi Level pinning effect in high-*k* gate dielectric.

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Chapter 6

Impact of Nitrogen in High-*k* Gate Dielectric on Charge Trapping Induced V_{th} Instability

6.1 Introduction

In order to maintain the continued scaling of CMOS devices, high-*k* gate dielectric will be required as the replacement of conventional SiO_2 or SiON, because of their potential in reducing equivalent oxide thickness (*EOT*) while maintaining low gate leakage current. Among various high-*k* candidates, Hf-based materials show the most promising characteristics for advanced gate dielectric application, and have been extensively investigated by both academia and industry for the past few years.

A challenging issue for integration of high-*k* gate dielectric into current CMOS process is that the dielectric would be compatible with conventional poly-Si gate. The poly-Si gate electrode is always attractive because its process integration schemes are well established in industry. Recently, incorporation of nitrogen in high-*k* gate dielectric has been widely utilized to improve thermal stability and suppress boron penetration in the devices with conventional poly-Si gate [1, 2]. There were also demonstrated that the high-*k* gate dielectric may benefit from the incorporated nitrogen due to enhancement on dielectric constant [3], increase in crystallization temperature [4], and statistical improvement of breakdown characteristics [5]. In addition, the high nitrogen concentration in dielectric caused degradation of interface properties and carrier mobility were reported in poly-Si/high-*k* devices [5, 6].

Consequently, it seems that the impact of the incorporated nitrogen on physical and electrical characteristics of high-*k* gate dielectric has been studied systemically in the devices with poly-Si gate. However, almost no result was reported on the impact of nitrogen on charge trapping induced V_{th} instability in poly-Si/high-*k* devices, although the charge tapping induced V_{th} instability is a very important reliability issue for implementation of high-*k* gate dielectric.

On the other hand, advanced metal gate, as a replacement of the conventional poly-Si gate, is very desirable for eliminating dopant depletion effects and sheet resistance constraints in future CMOS technology. Moreover, use of metal gate as a replacement of conventional poly-Si gate process could lower the required thermal budget by eliminating the need for dopant activation anneals in the poly-Si gate. According to the projections in 2005 International Technology Roadmap for Semiconductor (ITRS), high-*k* gate dielectric and advanced metal gate electrode will be required to meet the scaling goals by 2008. This suggests that the high-*k* gate dielectric with metal gate electrode could be more preferable for future CMOS application rather than the poly-Si/high-*k* structure. Numerous research groups have studied on tuning of metal gate work function [7, 8], electrical performance [9, 10], and also reliability [11, 12] in metal gate/high-*k* device. However, only a few research groups worked on the effects of nitrogen into high-*k* on electrical characteristics in metal gate device. In particular, the impact of nitrogen on charge trapping induced V_{th} instability in high-*k* is also unclear for metal gate device.

Therefore, it is necessary to examine the effects of nitrogen into high-*k* gate dielectric on the electrical characteristics in metal gate device, and also the impact of nitrogen on charge trapping induced V_{th} instability in high-*k* gate dielectric with both metal and poly-Si gate electrodes.

In this chapter, firstly, the effects of nitrogen in HfON gate dielectric has been studied on device characteristics in nMOSFETs with TaN metal gate, in particular on charge trapping induced V_{th} instability issue. Compared to HfO_2, the improvement of gate capacitance, slightly increase in gate leakage current and degradation of interface properties were observed in the HfON devices. Moreover, the incorporated nitrogen

induced mobility degradation in the HfON gate dielectric particularly occurred at low effective field region, almost no degradation was observed at medium or high field region. On the other hand, the impact of nitrogen on charge trapping induced V_{th} instability was examined in the HfO_2 and HfON gate dielectrics with TaN metal gate. Compared to HfO_2, the HfON gate dielectric showed a noticeable degradation of V_{th} instability probably caused by the incorporated nitrogen. These suggest that the incorporation of nitrogen in high-*k* gate dielectric needs to be carefully control for metal gate device due to the degradation of most of electrical characteristics.

Secondly, the impacts of nitrogen on charge trapping induced V_{th} instability in HfAlON gate dielectrics with TaN metal and poly-Si gates have also been investigated. A novel phenomenon, which the incorporated nitrogen in HfAlON gate dielectric played an opposite role in charge trapping induced V_{th} instability between the devices with TaN metal and poly-Si gates, was demonstrated. The results of this research may provide a guideline to optimize the formation of high-*k* gate dielectric for suppressing the charge trapping induced V_{th} instability, and also contribute a better understanding of charge trapping related V_{th} instability in high-*k* gate dielectric.

6.2 Effects of N in HfON on Electrical Characteristics

6.2.1 Experiments

The nMOSFETs were fabricated on 6-inch p-type Si wafers (10 ohm-cm) using the conventional self-aligned MOSFET process. After standard pre-gate clean with diluted HF dipping, 1-nm SiO_2 was grown on the Si wafer as interfacial layer (IL) by rapid thermal oxidation at 1000^{o} C. HfO_2 film with a thickness of 5 nm was deposited by metal organic chemical vapor deposition (MOCVD), and followed by post-deposition annealing (PDA) in N_2 ambient at 700^{o} C for 20 sec. Plasma nitridation were implemented to incorporate nitrogen for some HfO_2 samples in an N_2/Ar plasma. Post-nitridation annealing (PNA) was carried out in N_2 with 5% O_2 ambient at 800^{o} C for 5 sec. The compositions of PNA annealed HfON film, specified

as N/(N+O)=7%, were examined by X-ray photoelectron spectroscopy (XPS). To maintain the same thermal budget, the HfO_2 samples were also performed the PNA. A 150-nm TaN was deposited by reactive DC sputtering as a metal gate. After gate patterning, the As with a dose of 1×10^{15} cm^{-2} was implanted at an energy of 70 KeV. Source/drain activation annealing was then conducted in N_2 ambient at 1000° C for 10 sec. Finally, sintering was done at 420° C in forming gas ambient for 30 min after Al metallization.

6.2.2 Results and Discussion

Fig. 6.1 illustrates the *C-V* characteristics of TaN metal gate nMOSFETs with HfO_2 and HfON gate dielectrics. The equivalent oxide thicknesses (*EOT*) of the HfO_2 and HfON films were 2.74 and 2.67 nm, respectively. It was noted that the HfON film

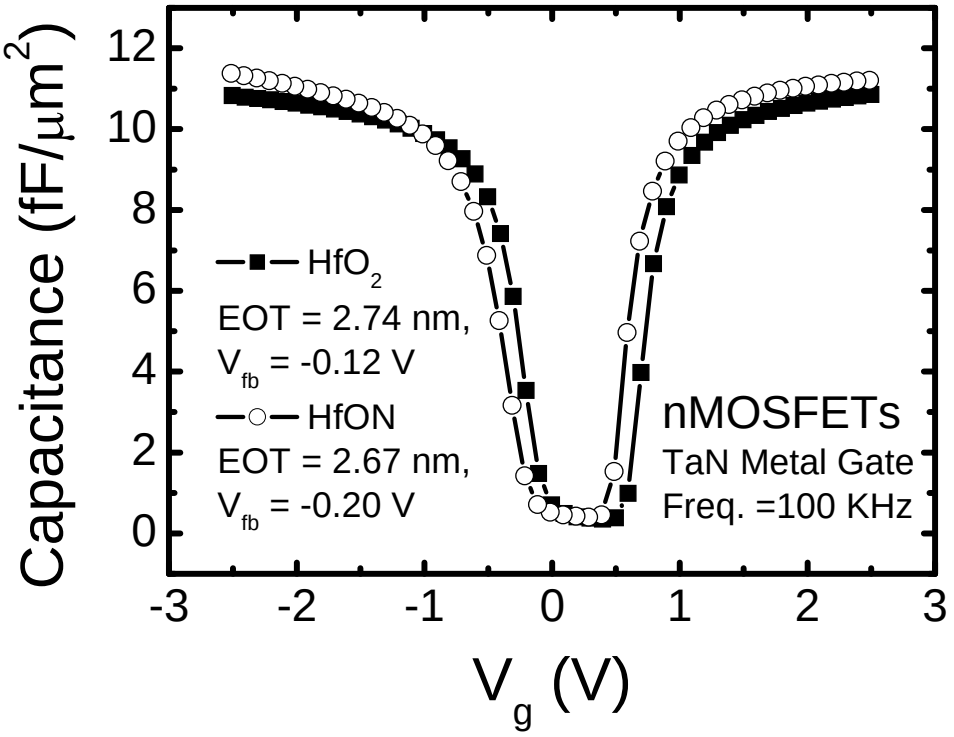


Fig. 6.1: *C-V* curves of TaN metal gate nMOSFETs with HfO_2 and HfON gate dielectrics. The HfON gate dielectric shows higher gate capacitance and negative shift in V_{fb} compared to HfO_2.

provides higher gate capacitance compared to HfO_2 even though the physical thicknesses of the two dielectrics are same. This implies that the incorporated nitrogen may increase the *k* value of HfO_2, which could be due to the formation of Hf-N bonds [13], and also the improved thermal stability of gate dielectric by adding nitrogen. Moreover, the flatband voltage (V_{fb}) in HfON film shifted to negative position compare to that in HfO_2. This implies that the incorporation of nitrogen may introduce positive fixed charges in the HfO_2 film, which is similar to that in SiO_2/SiON [14].

Fig. 6.2 compares the gate leakage currents of TaN metal gate nMOSFETs with HfO_2 and HfON gate dielectrics as a function of *EOT*. The gate leakage currents of HfON gate dielectric were slightly higher than those of HfO_2 at the same *EOT*. A similar result of higher gate leakage current induced by higher nitrogen concentration was also reported in a recent study on the HfSiON gate dielectric [5].

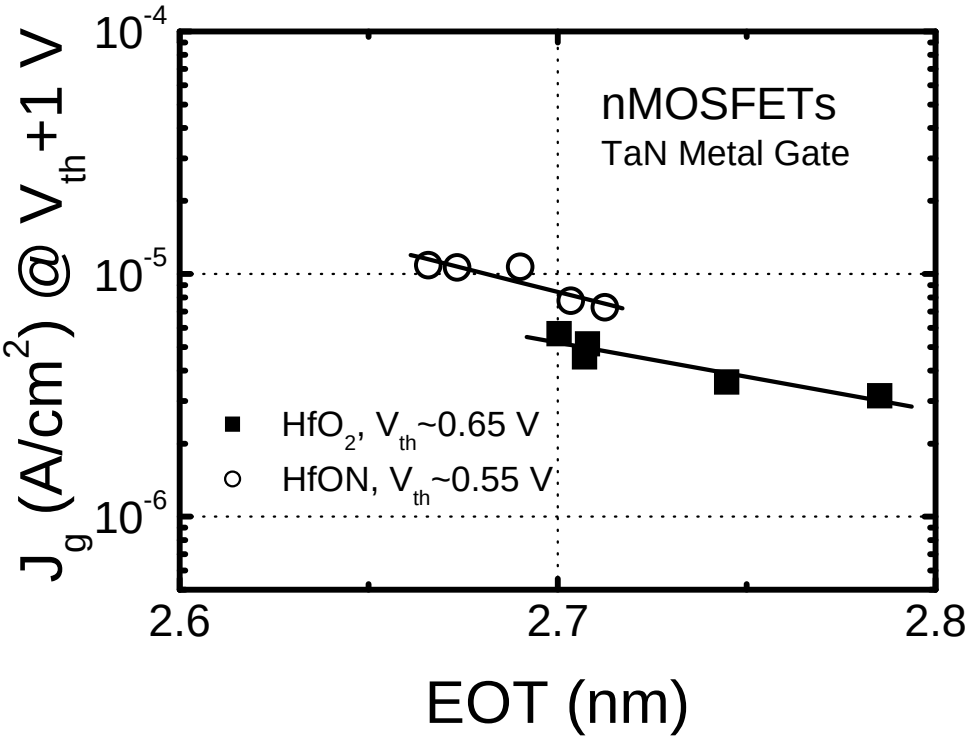


Fig. 6.2: *EOT* dependence of gate leakage currents at V_g=V_{th}+1V for TaN metal gated nMOSFETs with HfO_2 and HfON gate dielectrics. The leakage currents of HfON gate dielectric are slightly higher than those of HfO_2.

It is well known that the nitrogen in gate dielectric may penetrate the dielectric and pile up at the Si interface during the nitridation or subsequent annealing, which may degrade the interface properties of gate dielectric. **Fig. 6.3** shows subthreshold characteristics for TaN metal gate nMOSFETs with HfO_2 and HfON gate dielectrics. The subthreshold swings of HfO_2 and HfON gate dielectrics were 71 and 87 mV/dec, respectively. This indicates that the interface quality of HfON gate dielectric is degraded compared to that of HfO_2, which is induced by the incorporated nitrogen.

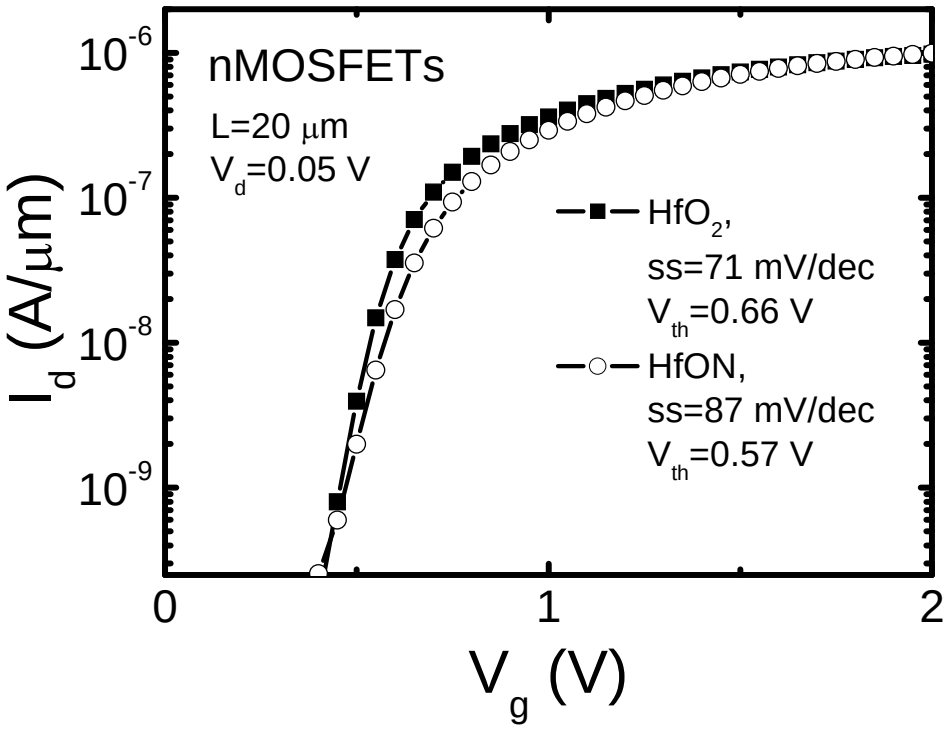


Fig. 6.3: Subthreshold characteristics for TaN metal gate nMOSFETs with HfO_2 and HfON gate dielectrics. The HfON exhibits higher subthreshold slope compared to HfO_2.

Fig. 6.4 compares the electron mobility in TaN metal gate nMOSFETs with HfO_2 and HfON gate dielectrics obtained by split *C-V* method. It was noted that the electron mobility in HfON nMOSFET was lower than that in HfO_2 at low effective field region, but almost no difference was found at middle or high effective filed

regions. The mobility degradation at low effective field region observed in HfON may be adequately explained by increase in coulomb scattering due to the incorporated nitrogen caused interface traps. Moreover, at the operation voltage of device, whose effective field is about 0.8 MV/cm, the electron mobility of 85% of universal curve was obtained in both HfO_2 and HfON devices.

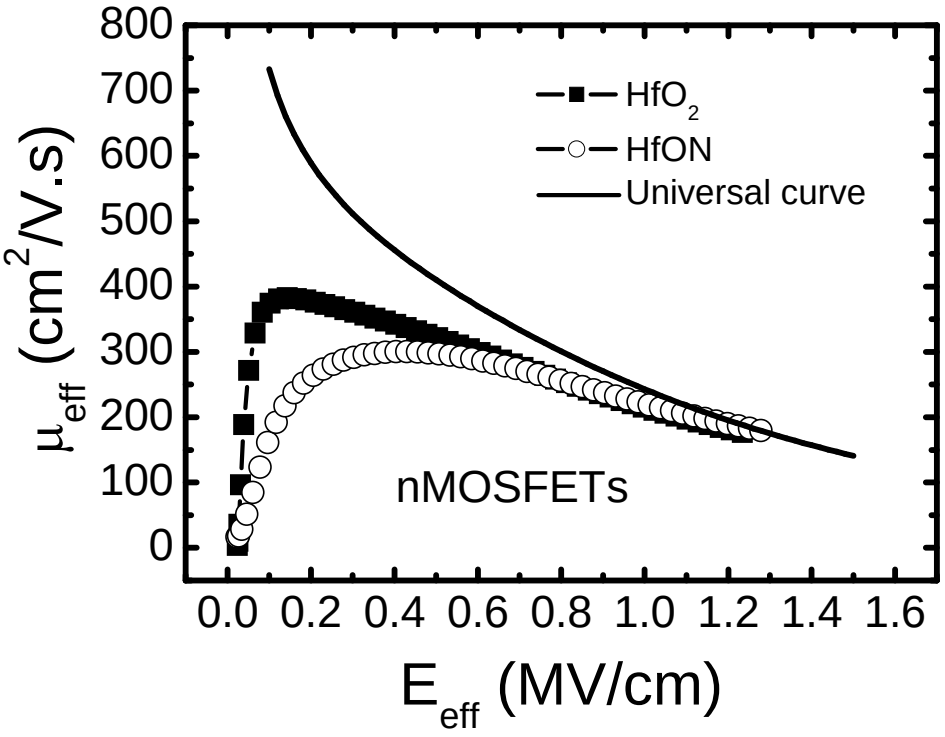
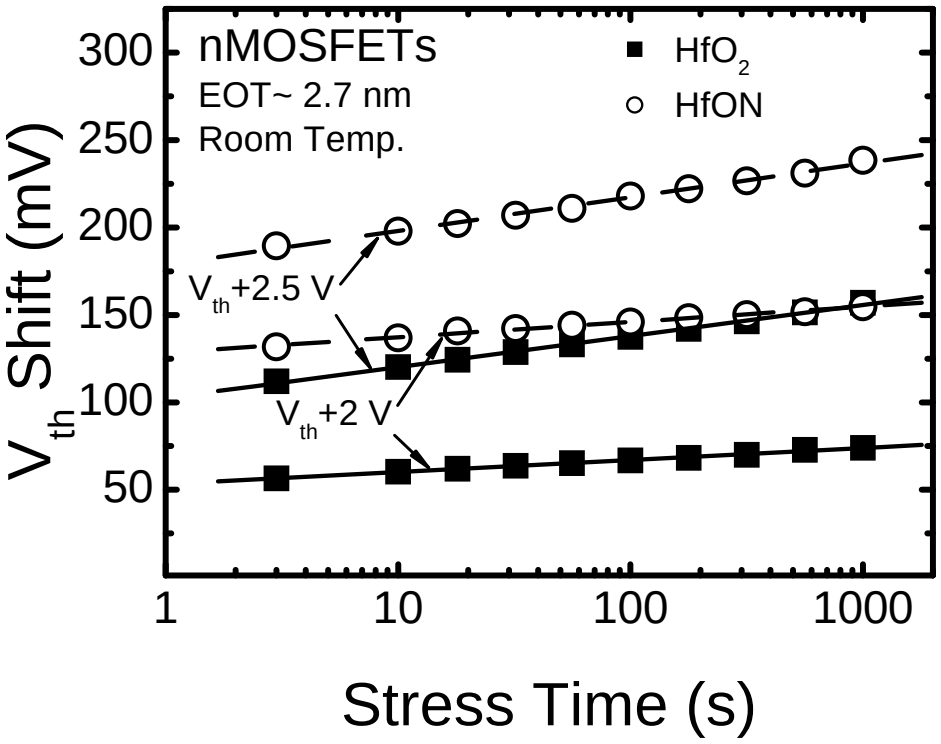
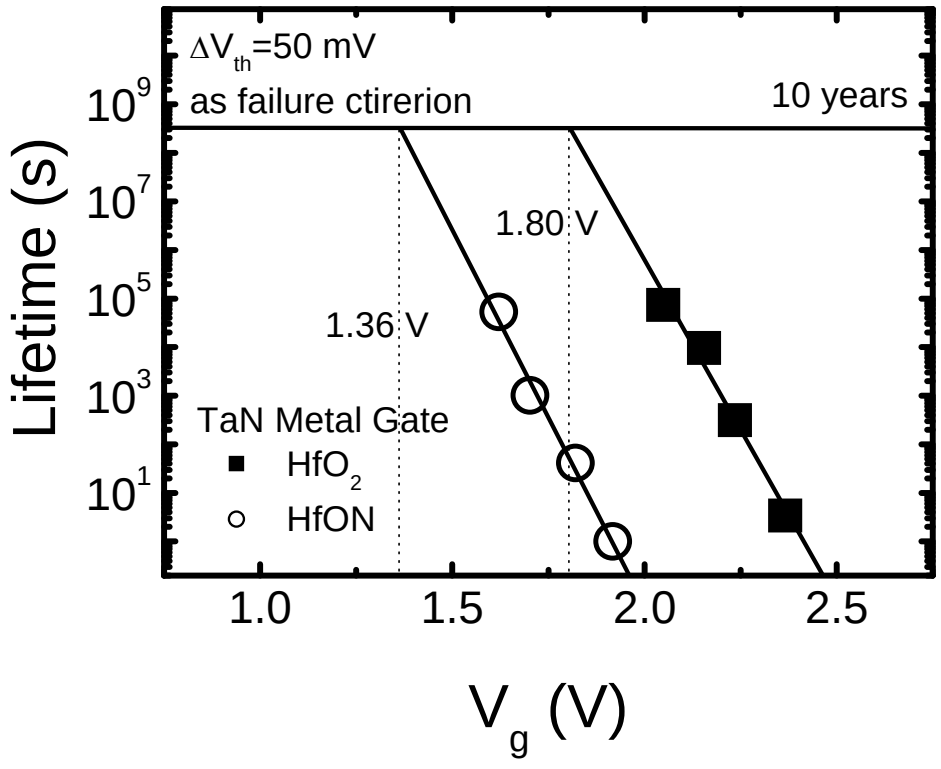


Fig. 6.4: Effective electron mobility of TaN metal gate nMOSFETs with HfO_2 and HfON gate dielectrics. The electron mobility of HfON is lower than that of HfO_2 at low effective field region (<0.5 MV/cm), whereas almost no difference is found at medium and high effective field region.

It has been reported that the most high-*k* gate dielectrics exhibit significant charge trapping effect, which causes the V_{th} shift during operation. The charge trapping induced V_{th} instability is a key challenge for integration of high-*k* gate dielectric in future COMS technology [15] **Fig. 6.5** (a) shows comparison of the V_{th} shifts under constant voltage stresses (V_{th}+2 and 2.5 V) in TaN metal gate nMOSFETs



(a)



(b)

Fig. 6.5: (a) Dependence of the V_{th} shifts on stress time at various stress voltages for TaN metal gate nMOSFETs with HfO_2 and HfON gate dielectrics.
(b) Lifetime projection of V_{th} shift for TaN metal gate nMOSFETs with HfO_2 and HfON gate dielectrics.

with HfO_2 and HfON gate dielectrics. It was found that the V_{th} shifts in HfON gate dielectric is around 1.5 times higher than that in HfO_2 under the same constant voltage stress. This indicates that the V_{th} instability induced by charge trapping is more serious in HfON rather than in HfO_2. The lifetime projection of V_{th} shifts in HfO_2 and HfON nMOSFETs are shown in **Fig. 6.5** (b). The failure criterion was set as ΔV_{th}=50 mV and the operating voltages of projected 10-year lifetime were 1.80 V for HfO_2 and 1.36 V for HfON. It is commonly believed that the V_{th} shift under positive stress in nMOSFETs is caused by filling of pre-existing bulk traps in high-*k* [16]. Compared to HfO_2, the degradation of V_{th} instability and lifetime projection shown in HfON film could be attributed to increased pre-existing bulk traps due to the incorporation of nitrogen.

6.2.3 Conclusion

The effects of nitrogen in HfON gate dielectric have been investigated on the device characteristics in TaN metal gate nMOSFETs, in particular on charge trapping induced V_{th} instability issue. Compared to HfO_2, the improvement of gate capacitance, slightly increase in gate leakage current and degradation of interface properties were observed in the HfON devices. Moreover, the incorporation of nitrogen induced mobility degradation in the HfON gate dielectric particularly occurred at low effective field region, almost no difference was found at medium or high effective field regions. On the other hand, the impact of nitrogen on charge trapping induced V_{th} instability was examined in the TaN metal gate nMOSFETs with HfO_2 and HfON gate dielectrics. Compared to HfO_2, the HfON gate dielectric showed a noticeable degradation of V_{th} instability, which could be attributed to the increase in pre-existing bulk traps caused by the incorporated nitrogen. These results suggest that the incorporation of nitrogen in high-*k* gate dielectric needs to be carefully control for metal gate device due to the degradation of most of electrical characteristics.

6.3 Impact of Nitrogen on Charge Trapping Induced V_{th} Instability

6.3.1 Experiments

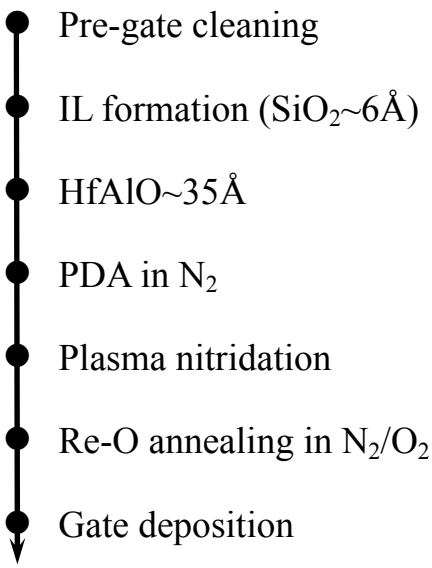


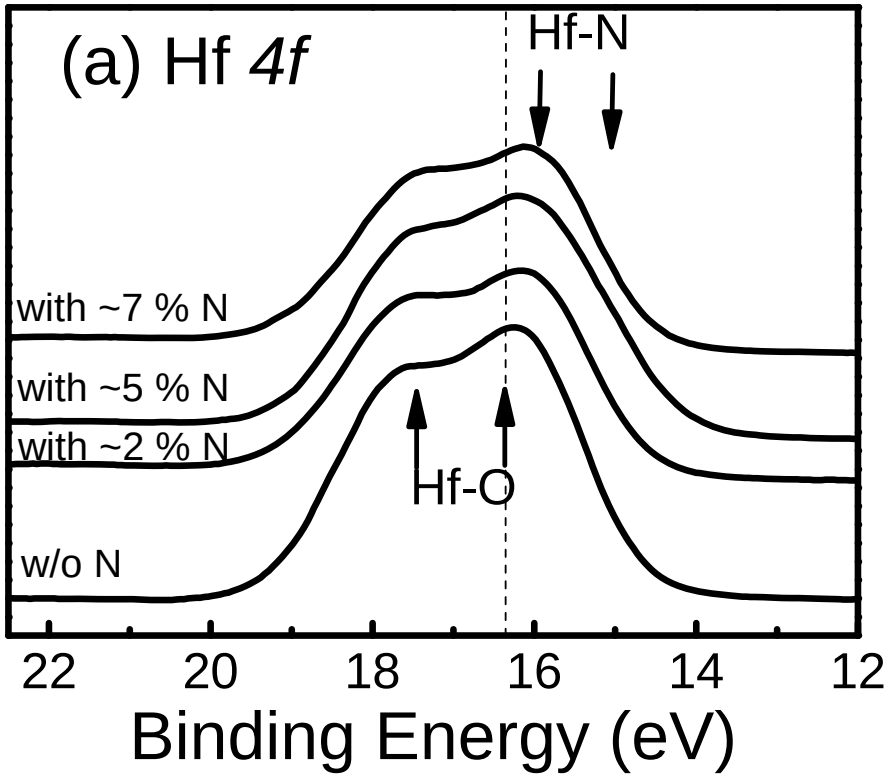
Fig. 6.6: Process flow of gate stacks formation (HfAlO with 26% Al).

The nMOS transistors were fabricated on 8-in Si substrates (6-9 Ω-cm) using conventional self-aligned MOSFET process. After standard pre-gate clean with diluted HF dipping, ~ 6 Å SiO_2 was growth as interfacial layer (IL) by rapid thermal oxidation at 1000^{o}C. 35-Å HfAlO with 26% Al was deposited on the SiO_2 IL by metal organic chemical vapor deposition (MOCVD), and followed by post-deposition annealing (PDA) in N_2 ambient at 700^{o}C for 20 sec. Plasma nitridation were implemented to incorporate nitrogen for some HfAlO samples in N2/Ar plasma. Re-oxidation annealing was carried out in N_2 with 5% O_2 ambient at 900^{o}C for 5 sec. The process flow of gate stack formation is summarized in **Fig. 6.6**. By controlling the power of plasma nitridation, HfAlON with 2%, 5% and 7% nitrogen (examined by XPS) were obtained. To maintain the same thermal budget, the HfAlO samples (without plasma nitridation) were also performed the re-oxidation annealing. Both TaN metal and poly-Si with thickness of 1500 Å were deposited by reactive DC

sputtering and low pressure chemical vapor deposition (LPCVD) as gate electrode, respectively. After gate patterning, arsenic at energy of 70 KeV were implanted with a dose of 1×10^{15} cm^{-2}. Then activation annealing was performed at 950 ºC for 20 sec. Finally, alloy was done at 400 ºC after Al metallization.

Electrical characteristics were evaluated using HP4156A precision semiconductor parameter analyzer and HP4284A precision LCR meter. *C-V* curves were measured at 100 KHz, and *EOT* and flat-band voltage (V_{fb}) were determined using Quantum-Mechanical *CV* simulator program (published by UC Berkeley Device Group), taking into account the quantum mechanical and poly-Si depletion effects. The transistor characteristics and V_{th} instability induced by charge trapping were measured using the transistors with W/L dimension of 400μm/3μm.

6.3.2 Results and Discussion



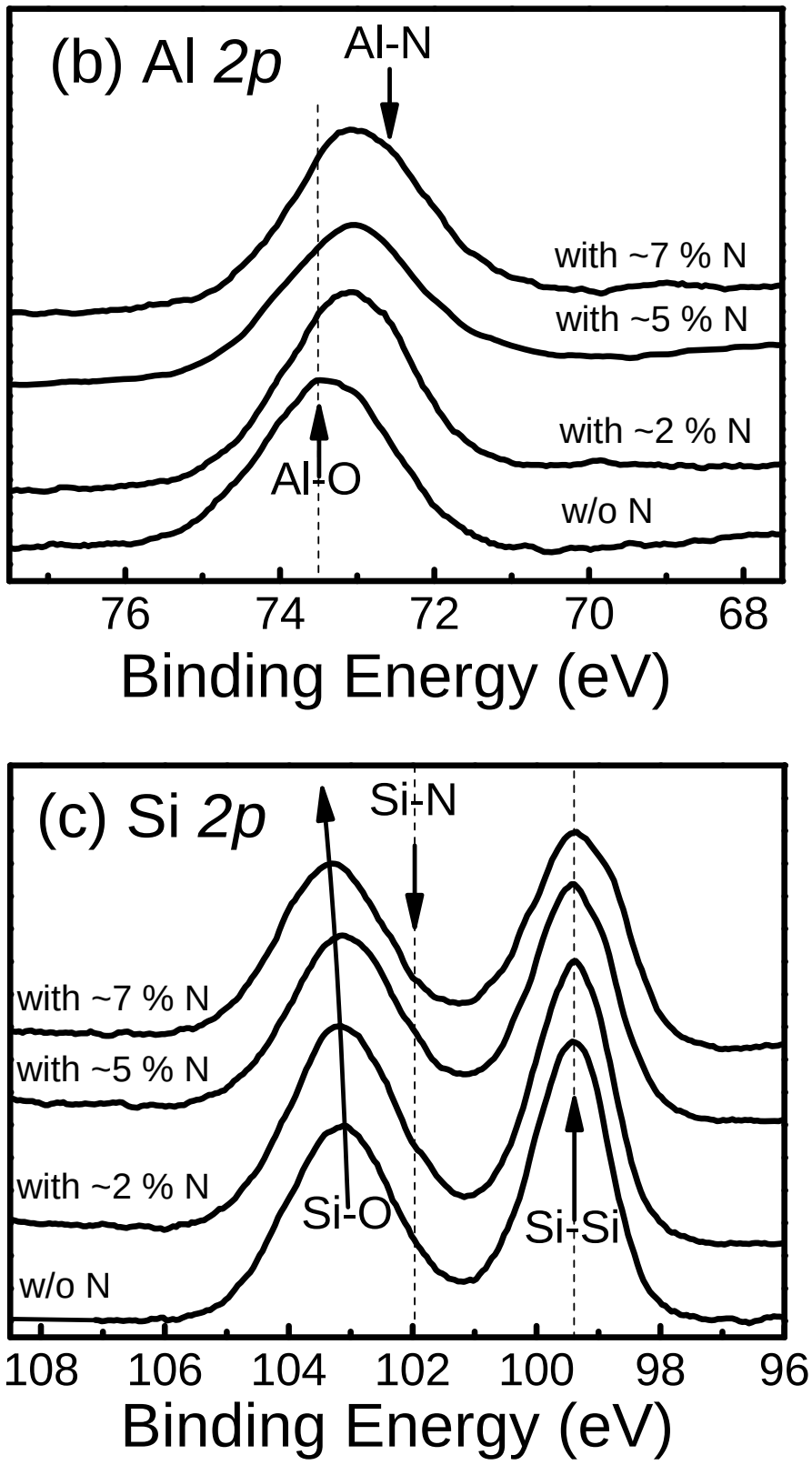


Fig. 6.7: XPS spectra of (a) Hf *4f*, (b) Al *2p*, and (c) Si *2p* for HfAlO with and without nitridation. It is noted that the Hf-O and Al-O bonds move to lower binding energy position (Hf-N and Al-N) and the Si-O bond shifts to high binding energy.

Fig. 6.7 shows the (a) Hf *4f*, (b) Al *2p*, and (c) Si *2p* XPS spectra of HfAlO with and without nitridation. It was clearly found that the Hf-O and Al-O bonds move to lower binding energy positions after nitridation, which suggest the formation of the Hf-N and Al-N bonds in the dielectrics. At the same time, the Si-O bond shifted to higher binding energy, which indicates almost no Si-N bonds formation (should shift to lower binding energy if it is formed). These XPS results suggest that the incorporated nitrogen mainly distributes into the HfAlO layer after the plasma nitridation and subsequent annealing.

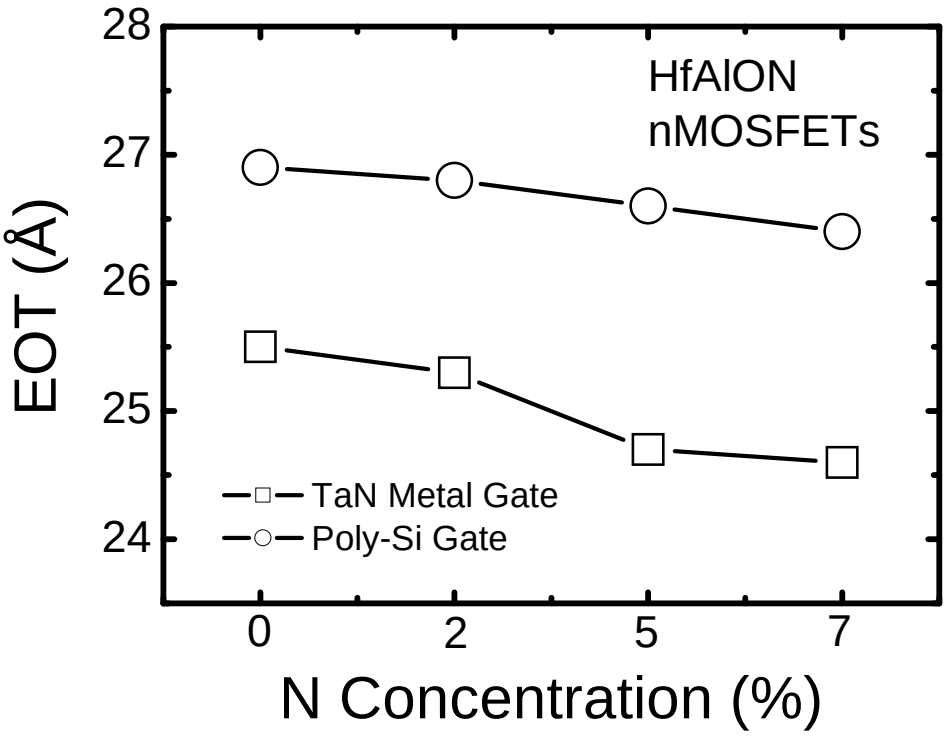


Fig. 6.8: *EOT* as a function of N concentration in HfAlON gate dielectrics for both TaN and poly-Si gate nMOSFETs.

Fig. 6.8 shows *EOT* as a function of nitrogen concentration in HfAlON gate dielectrics for TaN and poly-Si gate nMOSFETs. It was noted that the *EOT* of gate dielectrics slightly decreases with nitrogen concentration for both devices. This may be due to the increased *k* value of HfAlO, which is possible due to the formation of Hf-N bonds [13], and also the improved thermal stability by incorporating nitrogen.

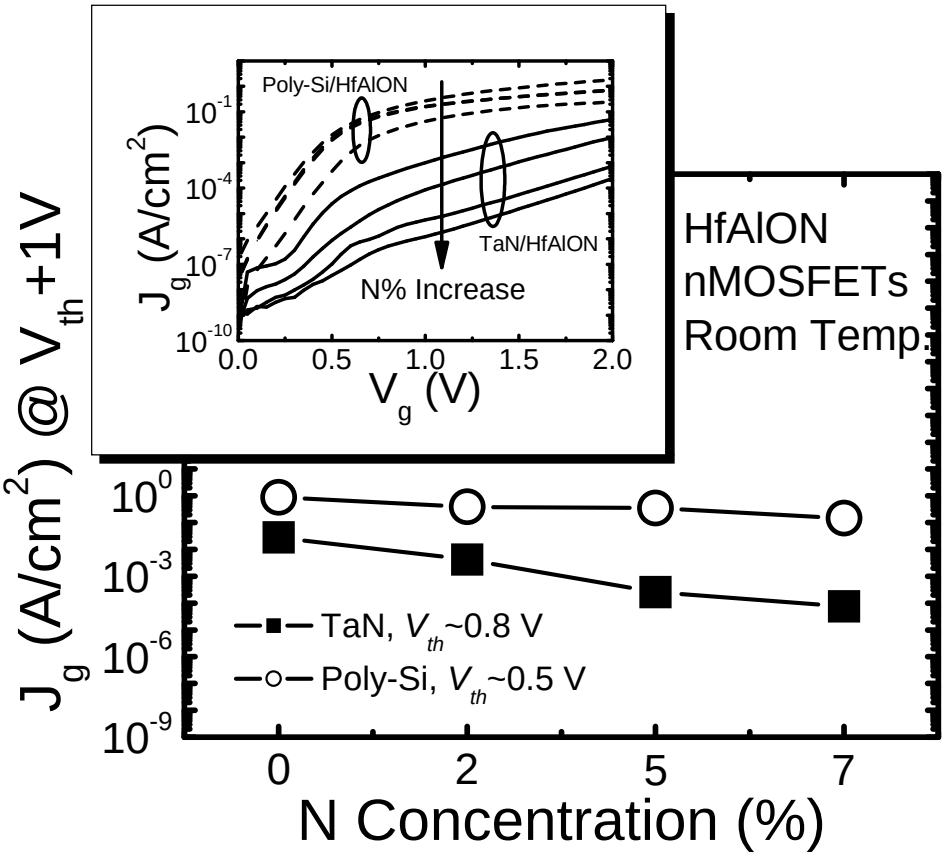
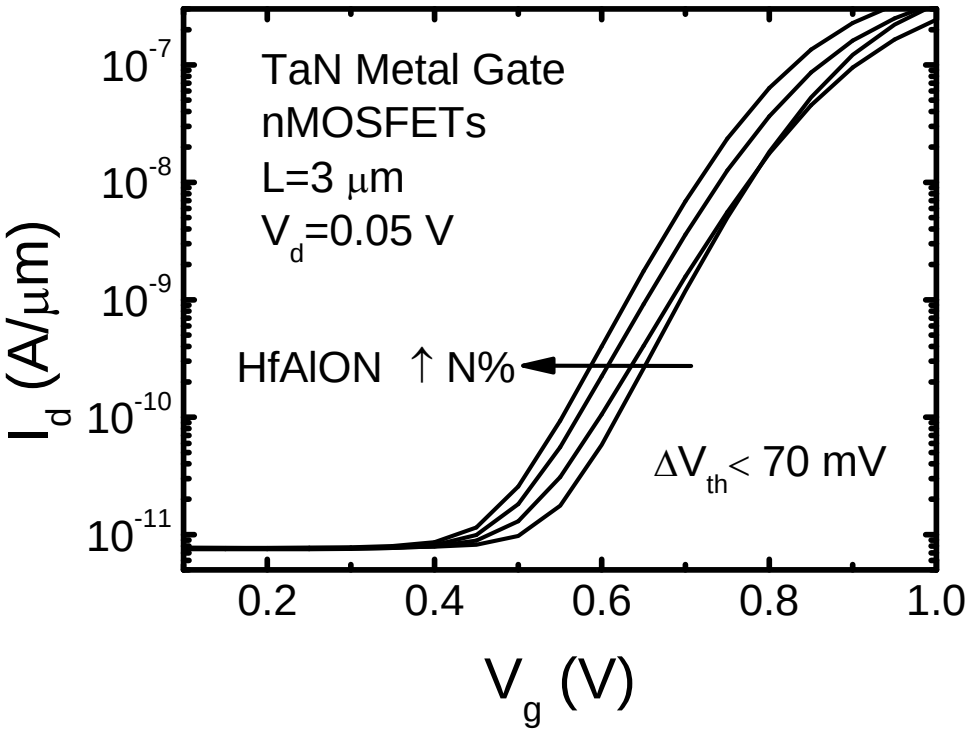
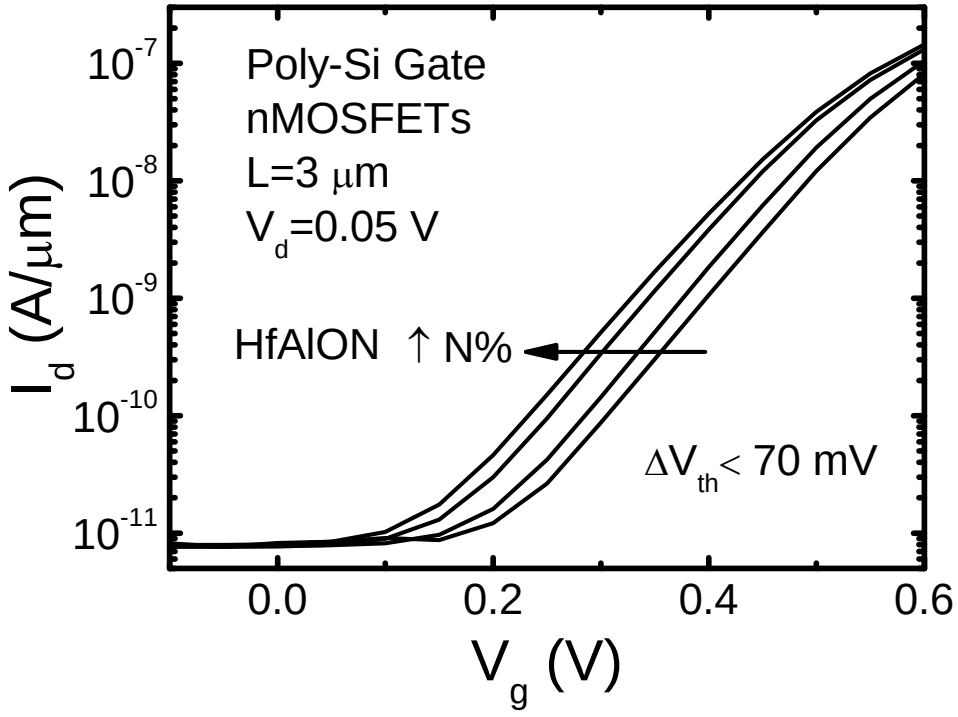


Fig. 6.9: Gate leakage currents (at V_g=V_{th}+1V) as a function of the N concentration in HfAlON gate dielectrics for TaN and poly-Si nMOSFETs, and also the corresponding J_g-V_g curves are shown in the inset.

Fig. 6.9 compares the gate leakage currents (at V_g=V_{th}+1V) of HfAlON gate dielectrics with TaN metal and poly-Si gates, and also the corresponding J_g-V_g curves are shown in the inset. The decreased gate leakage currents of the HfAlON films with increasing N concentration were observed in both TaN and poly-Si devices, which is similar to the previous report on the HfSiON gate dielectric [3]. However, this is inconsistent with the observation in the TaN/HfO_2 device (**Fig. 6.2**). It seems that the gate leakage current behaviors of the HfAlO (possibly amorphous structure) and HfO_2 (fully crystallized structure) films may be different. It was also noted that the HfAlON films with poly-Si gate show high leakage currents compared to those with TaN metal gate, irrespective of N concentration in the films. It has been reported that some



(a)



(b)

Fig. 6.10: Comparison of I_d-V_g characteristics for (a) TaN metal and (b) poly-Si gate nMOSFETs with HfAlON with 0%, 2%, 5% and 7% nitrogen.

defects as well as higher interface roughness might be formed at poly-Si/HfAlO interface and supposed to induce high gate leakage current [17]. This could be the reason why the HfAlON films with poly-Si gate show higher leakage currents than those with TaN metal gate, as observed in **Fig. 6.9**.

Fig. 6.10 illustrates the I_d-V_g characteristics of TaN metal and poly-Si gate nMOSFETs with HfAlON gate dielectrics. The V_{th} in HfAlON films shifted to negative position with increasing nitrogen concentration. This implies that the incorporation of nitrogen may introduce positive fixed charges in the HfAlON films, which is similar to that in SiO_2/SiON [14].

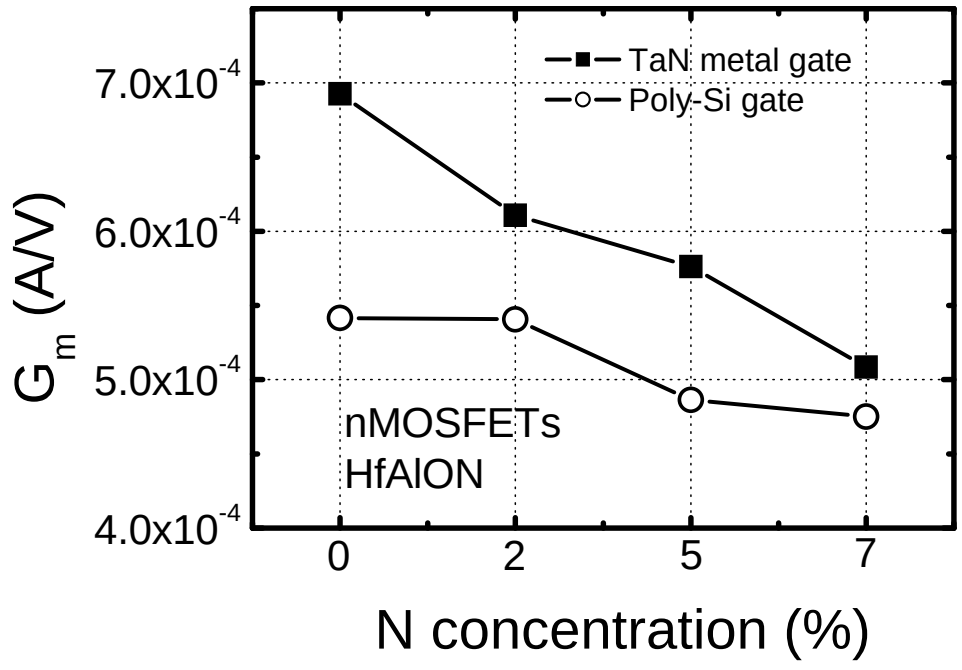


Fig. 6.11: Variation of G_m as a function of nitrogen concentration in HfAlON films for TaN metal and poly-Si gate nMOSFETs.

Fig. 6.11 shows the variation of transconductance (G_m) as a function of nitrogen concentration in HfAlON films for TaN metal and poly-Si gate nMOSFETs. The G_m of HfAlON gate dielectrics slightly decreased with increasing nitrogen concentration for both TaN metal and poly-Si gate nMOSFETs, indicating the degradation of device performance due to the incorporation of nitrogen in HfAlON. It

is well known that the incorporation of nitrogen into gate dielectric may degrade interface properties, which causes the increase in subthreshold swing (*ss*), as shown in **Fig. 6.12**. The degradation of interface properties due to the incorporation of nitrogen into gate dielectric compromises the device performance, which may be minimized by optimizing the process of plasma nitridation and subsequent re-oxidation annealing.

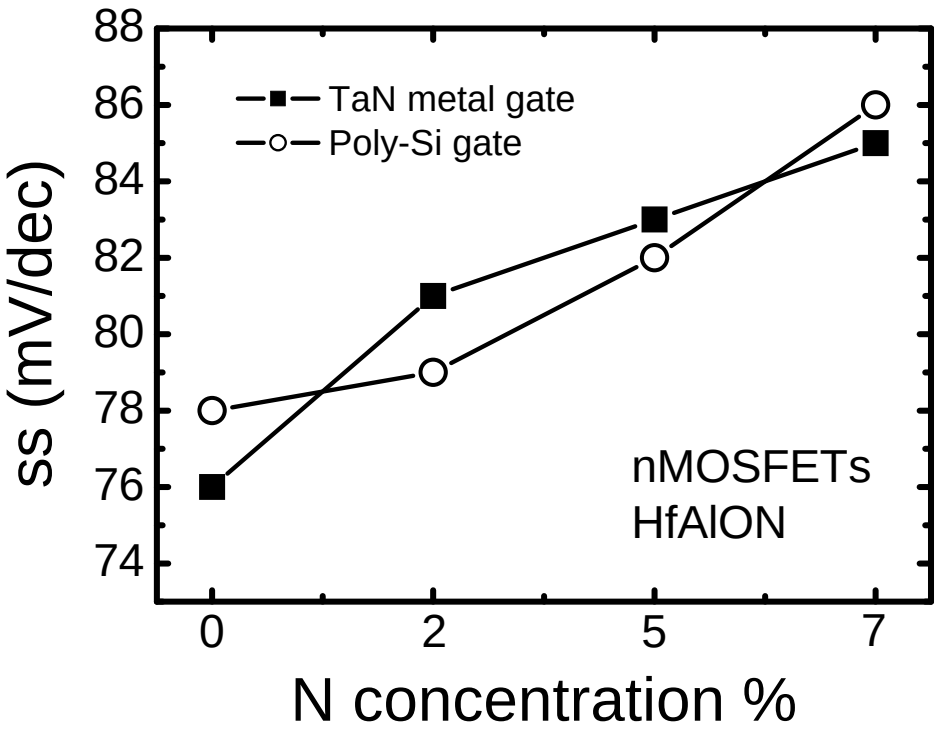


Fig. 6.12: Variation of *ss* as a function of nitrogen concentration in HfAlON films for TaN metal and poly-Si gate nMOSFETs.

It is well known that the most high-*k* gate dielectrics exhibit significant charge trapping effect, which causes the V_{th} shift during operation. In particular, the charge trapping under positive bias stressing (for nMOSFET) is known to be more severe compared to conventional SiO_2/SiON gate dielectrics [18-20], which is believed to happen due to filling of pre-existing bulk traps in high-*k* film. This charge trapping induced V_{th} instability is a key challenge for integration of high-*k* gate dielectric in future CMOS technology [21]. **Fig. 6.13** compares the charge trapping induced V_{th}

instability characteristics in HfAlO films (without nitridation) between TaN metal and poly-Si gate nMOSFETs. The constant voltage stresses of V_{th} + 1.5 and 2 V were applied at the gate electrode and the conventional static (DC) measurement with 100 μs delay time (as discussed in **Chapter 2**) was used to examine the V_{th} instability. As shown in **Fig. 6.13**, the V_{th} shifts in poly-Si gate devices were around 10 times higher than that in TaN metal gate devices, which is consistent with the observation in [22]. In contrast to the high-*k* gate dielectric with metal gate electrode, the significant charge trapping induced V_{th} instability observed in poly-Si/high-*k* devices could be mainly attributed to the additional electron trapping at oxygen vacancies caused by the poly-Si/high-*k* interaction (as discussed in **Chapter 5**).

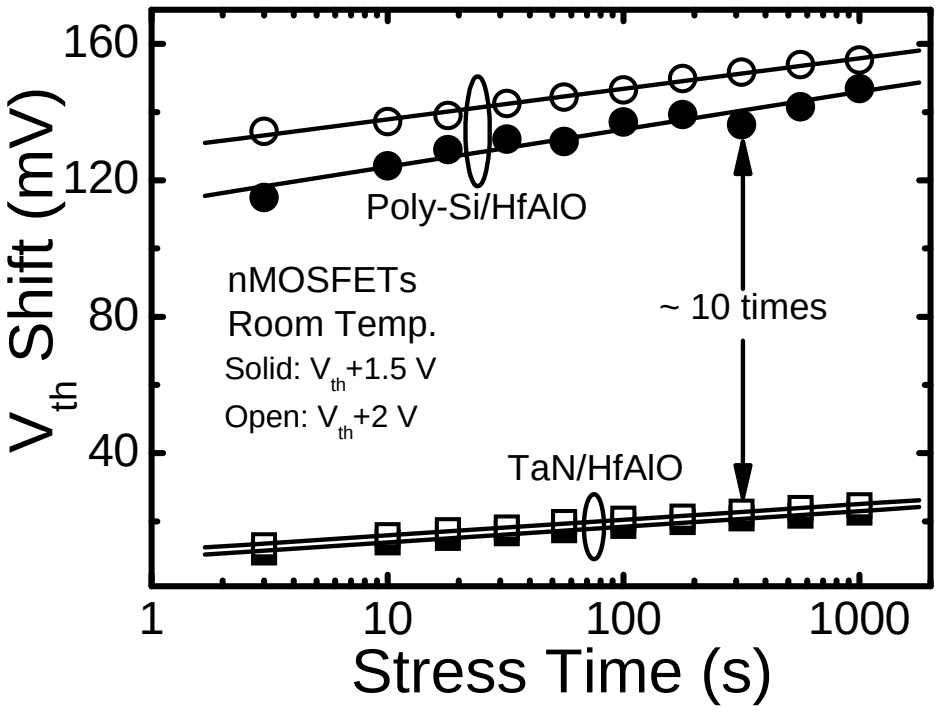
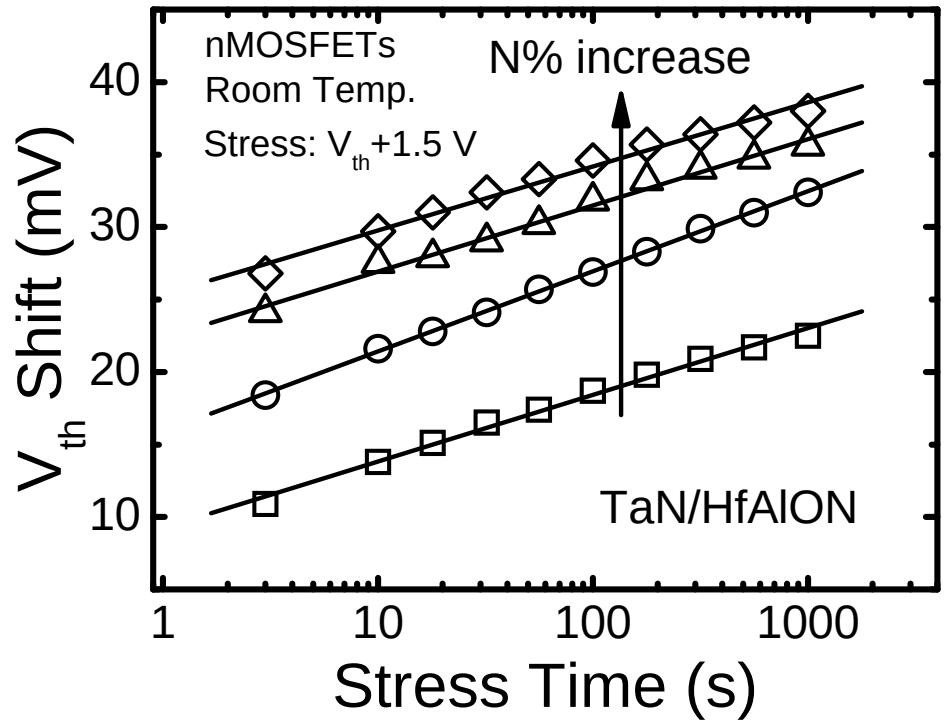
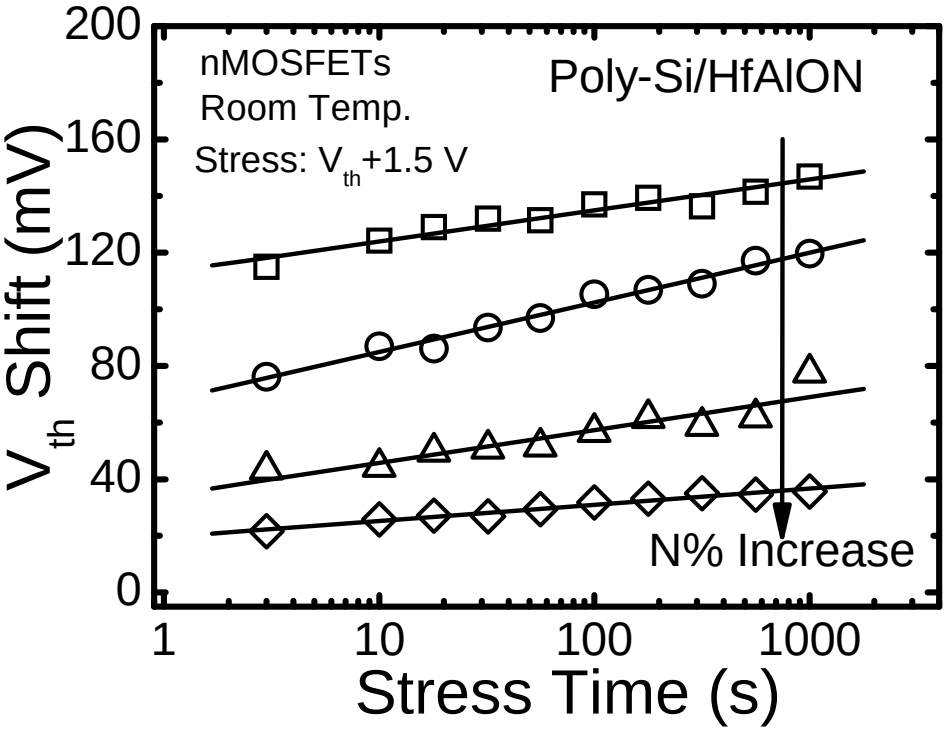


Fig. 6.13: Comparison of charge trapping induced V_{th} shift in HfAlO films between TaN metal and poly-Si gate nMOSFETs.

The impacts of nitrogen concentration on charge trapping induced V_{th} shift in HfAlON nMOSFETs with TaN metal and poly-Si gate are shown in **Fig. 6.14** (a) and



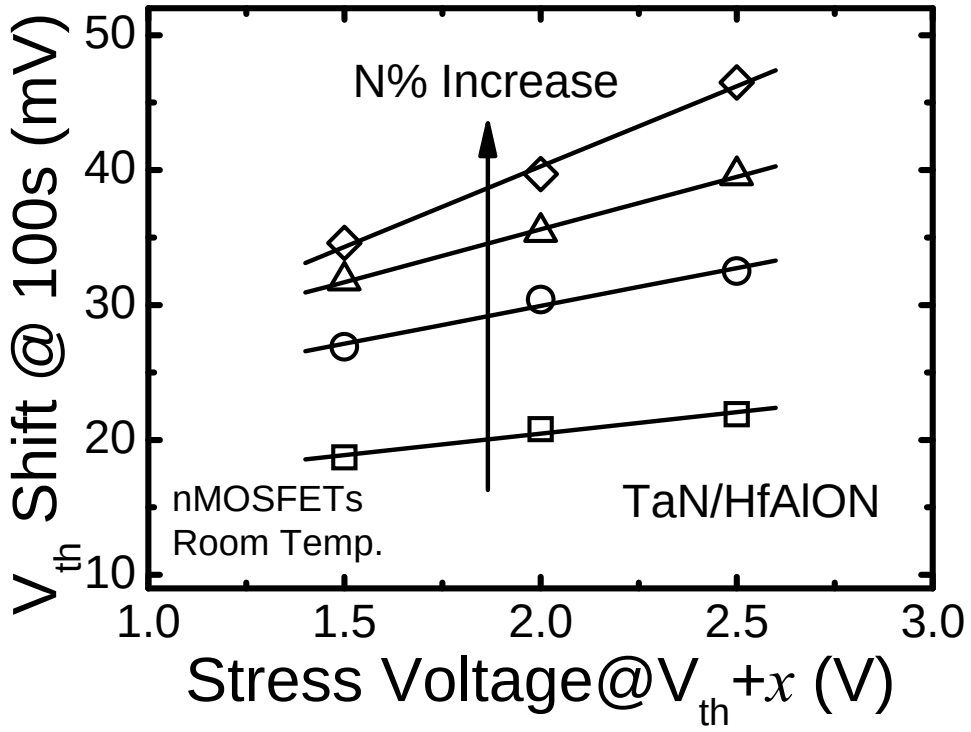
(a)



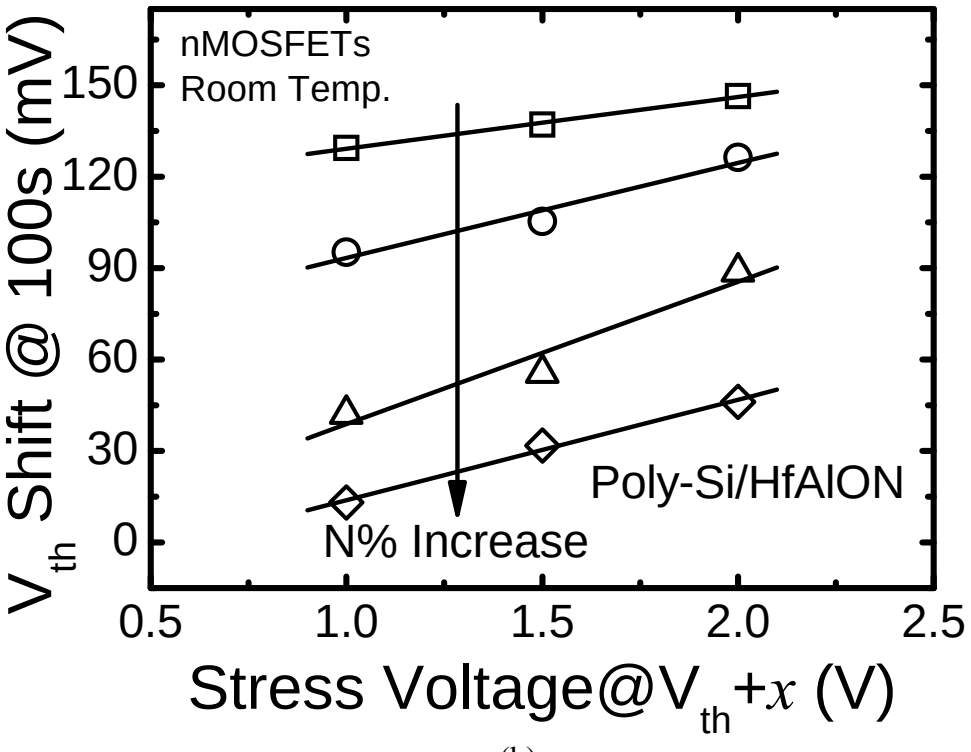
(b)

Fig. 6.14: (a) V_{th} shift in HfAlON nMOSFETs with TaN metal gate. The V_{th} shift increases with increasing nitrogen concentration.
(b) V_{th} shift in HfAlON nMOSFETs with poly-Si gate. The V_{th} shift decreases with increasing nitrogen concentration.

(b), respectively. Obviously, the incorporated nitrogen in HfAlON gate dielectrics played an opposite role in charge trapping induced V_{th} instability between TaN metal and poly-Si gate nMOSFETs. The V_{th} shift in HfAlON nMOSFETs with TaN metal gate increased with increasing nitrogen concentration, whereas decreased with increasing nitrogen concentration in poly-Si gate device. It was also noted that the incorporation of nitrogen into high-*k* gate dielectric may affect the V_{th} instability remarkably in poly-Si gate devices rather than in TaN metal gate devices. **Fig. 6.15** (a) and (b) show the charge trapping induced V_{th} shifts in HfAlON films after 100 sec stress as a function of stress voltages for TaN metal and poly-Si gate nMOSFETs. For TaN metal gate devices, the charge trapping induced V_{th} instability was degraded with increasing nitrogen in HfAlON film. In contrast, the charge trapping induced V_{th} instability was improved by incorporating nitrogen for poly-Si gate devices. The degradation of the V_{th} instability observed in the TaN metal gate devices, which is consistent with the previous findings in TaN/HfON devices (**Fig. 6.5**), is believed to be due to the increase in pre-existing bulk traps caused by incorporating N into the gate dielectric. The significant improvement on V_{th} instability in poly-Si gate devices is possibly due to the remarkable suppression of electron trapping at oxygen vacancies by incorporating N into high-*k* gate dielectric. It has been reported that the incorporation of N into high-*k* gate dielectric makes the oxygen vacancies less active as electron trap defects [23]. The first-principles calculations also suggest that N atoms favorably occupy the nearest neighbor oxygen sites to oxygen vacancies. As a result, electron charge traps at oxygen vacancies are remarkably suppressed due to the strong repulsive Coulomb interactions between electrons and negatively charged N^{3-} ions [24]. This implies that the incorporation of N into gate dielectric may significantly improve the charge trapping induced V_{th} instability in poly-Si/high-*k* device. Moreover, suppression of dopant penetration caused defects and reduction of gate leakage current by incorporating N into gate dielectric could also contribute to the improvement on the V_{th} instability in poly-Si/high-*k* device. On the other hand, it has to mention that the severer V_{th} shift of 137 mV (1.5 V stress at 100 sec) in HfAlO film with poly-Si gate can be significantly reduced to 31 mV by incorporating 7%



(a)



(b)

Fig. 6.15: (a) V_{th} shifts for HfAlON nMOSFETs with TaN metal gate as a function of applied stress voltages.
(b) V_{th} shifts for HfAlON nMOSFETs with poly-Si gate as a function of applied stress voltages.

nitrogen into the gate dielectric. The improved V_{th} shift in poly-Si/HfAlON is comparable with that of 20.8 mV in TaN/HfAlO device.

6.3.3 Conclusion

The impacts of nitrogen on charge trapping induced V_{th} instability in high-*k* gate dielectric with metal and poly-Si gates have been extensively studied. Compared to the high-*k* gate dielectric with metal gate, a severe V_{th} instability was observed in poly-Si/high-*k* devices. A novel phenomenon, which the incorporated nitrogen in high-*k* film played an opposite role in charge trapping induced V_{th} instability between metal and poly-Si gate devices, was demonstrated. In metal gate devices, the charge trapping induced V_{th} instability was degraded by incorporating nitrogen in high-*k* film. In contrast, the charge trapping induced V_{th} instability was improved by incorporating nitrogen in poly-Si gate devices. The significant improvement on V_{th} instability in poly-Si gate devices could be mainly attributed to the remarkable suppression of electron trapping at oxygen vacancies by incorporating N into high-*k* gate dielectric. The results of this research may provide a guideline to optimize the formation of high-*k* gate dielectric for suppressing the charge trapping induced V_{th} instability, and also contribute a better understanding of the charge trapping effect in high-*k* gate dielectric.

6.4 Summary and Major Contributions

In the first part, the effects of nitrogen in HfON gate dielectric have been investigated on the electrical characteristics in TaN metal gate nMOSFETs, in particular on charge trapping induced V_{th} instability. Compared to HfO_2, the improvement of gate capacitance, slightly increase in gate leakage current and degradation of interface properties were observed in the HfON devices. Moreover, the incorporation of nitrogen induced mobility degradation in the HfON gate dielectric particularly occurred at low effective field region, no degradation was observed at medium or high effective field region. On the other hand, the impact of nitrogen on

charge trapping induced V_{th} instability was examined in the TaN metal gate nMOSFETs with HfO_2 and HfON gate dielectrics. Compared to HfO_2, the HfON gate dielectric showed a noticeable increase in V_{th} instability, which could be attributed to the increase in pre-existing bulk traps caused by the incorporated nitrogen. These experimental results suggest that the incorporation of nitrogen in high-*k* gate dielectric needs to be carefully controlled for metal gate device due to the degradation of most of electrical characteristics.

In the second part, the impacts of nitrogen on charge trapping induced V_{th} instability in HfAlON gate dielectric with TaN metal and poly-Si gates have been extensively studied. Compared to the HfAlON gate dielectric with TaN metal gate, a severe V_{th} instability was observed in poly-Si/HfAlON devices. A novel phenomenon, which the incorporated nitrogen in high-*k* film played an opposite role in charge trapping induced V_{th} instability between the devices with TaN metal and poly-Si gate, was demonstrated. For TaN metal gate devices, the charge trapping induced V_{th} instability was degraded by incorporating nitrogen into HfAlO film. In contrast, the charge trapping induced V_{th} instability was improved by incorporating nitrogen for poly-Si gate devices. The significant improvement on V_{th} instability in poly-Si gate devices could be mainly attributed to the remarkable suppression of electron trapping at oxygen vacancies by incorporating N into high-*k* gate dielectric. The results of this research may provide a guideline to optimize the formation of high-*k* gate dielectric for suppressing the charge trapping induced V_{th} instability, and also contribute a better understanding of charge trapping effect in high-*k* gate dielectric.

On the other hand, it is not clear why the HfO_2 and HfAlO films show different gate leakage current behavior after incorporating nitrogen. It could be related to the structure of the HfAlO (amorphous) and HfO_2 (fully crystallized) films. We suggest that more work should be done to identify the mechanisms behind this phenomenon.

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Chapter 7

Conclusions and Future Work

The main purpose of this thesis was to overcome the four major challenges for the implementation of high-*k* gate dielectrics, including the thermal stability, mobility degradation, charge trapping induced threshold voltages (V_{th}) instability, and unacceptably high V_{th} induced by Fermi Level pinning (as discussed in **Chapter 1**), and also attempt to integrate the high-*k* gate dielectric to conventional self-aligned poly-Si gate and advanced metal gate process.

This chapter discusses and summarizes the results of the research work described in the previous five chapters. Moreover, the major contributions of this thesis are reviewed and suggestions for future work are discussed.

5.1 Summary of Results

As discussed in **Chapter 2**, we proposed a novel Hf-based gate dielectric by examining the effects of Ta inclusion in HfO_2 on the thermal stability, leakage current, dielectric constant, interface properties, electrical stability and surface carrier mobility. Material studies indicated that the crystallization temperature of HfO_2 is significantly enhanced by incorporating Ta. This could be attributed to the breaking of the periodic crystal arrangement or the inhibition of continuous crystal growth in dielectric by incorporating Ta into HfO_2 film. It was also observed that the HfTaO film shows good thermal stability compared to HfO_2, which can be attributed to the suppressed oxygen diffusion in the HfTaO film with lack of crystallization. Moreover, the results of

extensive electrical studies demonstrated that the interface state density (D_{it}) in HfO_2 film decreased significantly by incorporating Ta, and also the peak electron mobility in HfTaO MOSFETs is more than two times higher than that in HfO_2. The improvements on D_{it} and mobility observed in HfTaO may be mainly due to the formation of a high quality interfacial layer between HfTaO and Si substrate. It should be noted that the D_{it} and mobility in HfTaO are still incomparable with that in conventional SiO_2 gate dielectric. In addition, charge trapping induced V_{th} instability in HfO_2 and HfTaO films were examined by using static (DC) and pulsed I_d-V_g measurement techniques, and the V_{th} shift in HfTaO film was much lower than HfO_2. This indicates that electrical instability in HfO_2 film is significantly improved by incorporating Ta, and the HfTaO film contains ultra-lower bulk traps compared to HfO_2. This is possible due to the lack of crystallization in HfTaO films resulting in a significantly lower number traps compared to HfO_2. On the other hand, even though the leakage current of HfTaO film was higher than that of pure HfO_2 due to the lower band offset of Ta oxide, it is still comparable to the most high-*k* gate dielectrics, such as HfSiO, HfAlO, HfSiON, and HfAlON. This can be explained by that the HfTaO with higher dielectric constant provides a physically thicker film to reduce leakage current compared to those high-*k* gate dielectrics at the same *EOT*.

As discussed in **Chapter 3**, a novel HfTaON/SiO_2 gate stack, which consists of a HfTaON film with *k* value of 23 and a 10-Å SiO_2 interfacial layer, was proposed for advanced low standby power application. The HfTaON/SiO_2 gate stack provided much lower gate leakage current against SiO_2, good interface properties, excellent transistor characteristics and superior carrier mobility. Compared to HfON/SiO_2, improved thermal stability was also observed in the HfTaON/SiO_2 gate stack. Moreover, the charge trapping induced V_{th} instability was examined for the HfTaON/SiO_2 and HfON/SiO_2 gate stacks by using the conventional static (DC) measurement technology. The HfTaON/SiO_2 gate stack exhibited significant suppression of the V_{th} instability compared to the HfON/SiO_2, in particular for nMOSFETs. These excellent performances observed in the HfTaON/SiO_2 can be attributed to the good physical and electrical characteristics shown in HfTaO film,

which were presented in **Chapter 2**. Also, the incorporation of N into HfTaO may further improve the thermal stability of gate stack, and the very low D_{it} and superior carrier mobility shown in this gate stack may be mainly attributed to the insertion of SiO_2 interfacial layer between HfTaON film and Si substrate. Compared to some published results observed in the Hf-silicates, the HfTaON/SiO_2 gate stack showed lower gate leakage current and higher carrier mobility.

As discussed in **Chapter 4**, the experimental results demonstrated that the gate dopant penetration may remarkably affect the gate leakage current in n^+ poly-Si/HfO_2 devices. The poly-Si/HfO_2 devices with low gate doping concentration exhibited very low leakage currents, whereas the devices with heavy gate doping concentration showed excessive leakage currents. The current images examined by C-AFM confirmed the existence of evident leakage paths in the HfO_2 films with excessive leakage currents, whereas no leakage paths were observed in those with low leakage currents. Moreover, fully crystallized HfO_2 film with a grain boundary was clearly observed in TEM picture. The dimension of HfO_2 grain was comparable to those of leakage paths observed in the high leaky HfO_2 films. The SIMS profiles of phosphorus in the poly-Si/HfO_2 gate stack demonstrated that the diffusion of phosphorus into HfO_2 films after the annealing is more serious in the films with excessive leakage currents rather than those with low leakage currents. Based on the experimental results and physical analyses, it is possible to speculate that the diffusion of excessive phosphorus from n^+ poly-Si gate into the HfO_2 film, especially through the grain boundaries in the film, could generate phosphorus-related defects, which may induce the evident leakage paths and significantly increase the leakage current in the n^+ poly-Si/HfO_2 devices.

As discussed in **Chapter 5**, the critical issue of unacceptably high V_{th} induced by Fermi Level pinning at poly-Si/high-*k* interface was introduced. This is the most challenging issue for integration of advanced Hf-based gate dielectrics into the conventional dual poly-Si gate CMOS process. In this chapter, we have demonstrated that the unacceptably high V_{th} induced by the Fermi level pinning at poly-Si/high-*k* interface was effectively suppressed by inserting a poly-SiGe gate electrode. The

acceptable V_{th} of 0.3 V for nMOSFET and -0.49 V for pMOSFET was successfully achieved in poly-Si/poly-SiGe/Al_2O_3/HfO_2 device. The G_m of transistors was also improved by using the poly-SiGe gate, in particular for the pMOSFET. It was also found that the charge trapping induced V_{th} instability is significantly improved in this poly-Si/poly-SiGe/Al_2O_3/HfO_2 device. The suppression of Fermi Level pinning effect and the improvements on G_m and V_{th} instability in the poly-Si/poly-SiGe/Al_2O_3/HfO_2 device may be due to the suppressed formation of oxygen vacancies and associated electron traps by using the poly-SiGe gate electrode.

As discussed in **Chapter 6**, firstly, the effects of nitrogen in HfON gate dielectric have been investigated on the device characteristics in TaN metal gate nMOSFETs, in particular on charge trapping induced V_{th} instability issue. Compared to HfO_2, the improvement of gate capacitance, slightly increase in gate leakage current and degradation of interface properties were observed in the HfON devices. Moreover, the incorporation of nitrogen induced mobility degradation in the HfON gate dielectric particularly occurred at low effective field region, almost no difference was found at medium or high effective field regions. On the other hand, the impact of nitrogen on charge trapping induced V_{th} instability was examined in the TaN metal gate nMOSFETs with HfO_2 and HfON gate dielectrics. Compared to HfO_2, the HfON gate dielectric showed a noticeable degradation of V_{th} instability, which could be attributed to the increase in pre-existing bulk traps caused by the incorporated nitrogen. Secondly, the impacts of nitrogen on charge trapping induced V_{th} instability in HfAlON gate dielectric with TaN metal and poly-Si gates have been systemically studied. Compared to the HfAlON gate dielectric with TaN metal gate, a severe V_{th} instability was observed in poly-Si/HfAlON devices. A novel phenomenon, which the incorporated nitrogen in high-*k* film played an opposite role in charge trapping induced V_{th} instability between the devices with TaN metal and poly-Si gate, was demonstrated for the first time. For TaN metal gate devices, the charge trapping induced V_{th} instability was degraded with increasing nitrogen in HfAlON film. In contrast, the charge trapping induced V_{th} instability was improved by incorporating nitrogen for poly-Si gate devices. The degradation of V_{th} instability in TaN metal gate

devices may be attributed to the increase in pre-existing bulk traps caused by incorporating N into the gate dielectric. The significant improvement on V_{th} instability in poly-Si gate devices is possibly due to the remarkable suppression of electron trapping at oxygen vacancies by incorporating N into high-*k* gate dielectric.

5.2 Major Contributions and Suggestions of Future Work

In previous works, the characteristics of HfO_2, such as crystallization temperature, thermal and electrical stability, are improved by adding Al_2O_3 or SiO_2 into HfO_2 film. These approaches, which incorporate the lower dielectric constant materials (Al_2O_3 and SiO_2) into HfO_2 film, may degrade the dielectric constant of HfO_2, and also compromise the benefits of high-*k* gate dielectric. For the first time, we developed the HfTaO gate dielectric by incorporating the Ta oxide with high dielectric constant into HfO_2, as presented in **Chapter 2**. This gate dielectric exhibits significantly improved crystallization temperature, thermal and electrical stability compared to HfO_2, and also no degradation of dielectric constant. The excellent characteristics of HfTaO gate dielectric indicate that it is a very promising candidate as the alternative gate dielectric for future MOSFET application. On the other hand, the electrical stability in high-*k* gate dielectrics is one of major challenge for its real implementation. The significant improvement on electrical stability by incorporating Ta into HfO_2 gate dielectric is a considerably important advantage of HfTaO film for gate dielectric application. In **Chapter 2**, an interesting phenomenon, which the crystallization temperature of HfTaO is higher than the two compositive materials of both HfO_2 and Ta_2O_5, was reported in high-*k* field for the first time. In addition, the experimental results appear to confirm that the charge trapping induced V_{th} instability may be affected by the film morphology (amorphous or crystallized structure) of high-*k* gate dielectric. Since the root causes of these two phenomena are not very clear yet, further work would be needed to identify the mechanisms involved in these phenomena. This might be helpful for further investigation on high-*k* gate dielectrics.

The mobility degradation in high-*k* gate dielectric is a serious issue for CMOS

application. As presented in **Chapter 3**, the superior carrier mobility shown in HfTaON/SiO_2 gate stack indicates that it has the potential to replace the conventional SiO_2 and SiON as gate dielectric for advanced CMOS application. The insertion of ultra-thin SiO_2 is an important factor in the suppression of mobility degradation in high-*k* gate stack. By comparing the carrier mobility in the high-*k* with or without the ultra-thin SiO_2 layer, it is concluded that the SiO_2 interfacial layer play a key role for the suppression of mobility degradation. However, the insertion of SiO_2 interfacial layer may limit the continuous scaling of dielectric thickness, and the HfTaON/SiO_2 gate stack appears to be very promising candidate for low standby power application rather than high performance application, which requires further scaling down of *EOT* to less than 10 Å in the near future. In fact, among all of high-*k* candidates, almost none can completely meet the requirements for high performance CMOS application yet. Therefore, further work is needed to develop a novel high-*k* gate stack with sufficiently good performance for the advanced high performance CMOS application, which could be a serious challenge for the further investigation of high-*k* gate dielectric.

In previous works, many research groups demonstrated that the HfO_2 gate dielectric exhibited much low gate leakage currents with poly-Si gate. However, the observation of excessive gate leakage current or even initial breakdown, in particular for the devices with n^+ poly-Si gate, was also reported in HfO_2 gate dielectric with poly-Si gate by several research groups. These reports contradicted each other imply that the poly-Si gate device with HfO_2 gate dielectric has a narrow process window, which strongly dependents on the deposition temperature of poly-Si gate, the device area, and the capping layer of gate dielectric. Several mechanisms have been proposed to explain the findings of the excessive leakage current and the narrow process window issue in the poly-Si/HfO_2 devices. However, almost none can explain the experimental results successfully. In **Chapter 4**, we have demonstrated that the gate dopants penetration may remarkably affect the gate leakage current in n^+ poly-Si/HO_2 devices. A hypothesis for generation of dopant-related defects is also proposed in this chapter, which may sufficiently explain the previous findings of the correlative

dependence of gate leakage current on the deposition temperature of Si gate, the device area, and the capping layer of gate dielectric in poly-Si/HfO_2 devices. These results imply that phosphorus or arsenic penetration is a significant concern for poly-Si/HfO_2 device, and an amorphous capping layer between HfO_2 and poly-Si gate or incorporation of N into HfO_2 may be needed to suppress the dopant penetration in n^+ poly-Si/HfO_2 device. This is very important from viewpoint of poly-Si/high-*k* CMOS production. However, the root of the significant increase in gate leakage current induced by the dopants penetration, or the generation of dopant-related defects is unclear yet. The impact of the dopants penetration on other electrical properties in poly-Si/HfO_2 device, such as carrier mobility, charge trapping induced threshold voltage instability, and gate dielectric breakdown, is still unknown. In addition, the influence of the dopants penetration on other high-*k* materials is also unexplored. We suggest that more work should be done to identify the mechanisms behind this phenomenon of dopant induced excessive leakage current, and also verify the impact of the dopant penetration on overall properties in n^+ poly-Si/high-*k* devices.

The findings discussed in **Chapter 5**, which are the effective suppression of Fermi Level pinning effect, and also the acceptable V_{th} in poly-Si/polySiGe/Al_2O_3/ HfO_2 CMOS devices, could make a great breakthrough for real implementation of high-*k* gate dielectric. Since the poly-SiGe gate is fully compatible with the mature poly-Si gate process, the application of poly-SiGe gate could be a promising solution for the integration of high-*k* gate dielectric into the conventional CMOS process. The most challenging issue in the implementation of high-*k* gate dielectric seems to be overcome by this approach. Moreover, the results observed in this experiment could be very useful for further exploring the origin of the Fermi Level pinning effect in high-*k* gate dielectric. Restricted by the equipment for deposition of poly-SiGe film used in this work, however, the electrical characteristics of poly-SiGe gated devices may not completely be examined by comparing to conventional poly-Si gated devices. Moreover, the effects of Ge content in poly-SiGe gate and thickness of Al_2O_3 capping layer on Fermi Level pinning induced V_{th} shift are not investigated in this study. Therefore, further work should be done to confirm the results presented in this study,

and also explore the effects of the Ge content in poly-SiGe gate and thickness of Al_2O_3 capping layer on the Fermi Level pinning effect in high-*k* gate dielectric.

Finally, as presented in **Chapter 6**, the effects of nitrogen in high-*k* gate dielectric have been systemically investigated on the electrical characteristics in metal gate device. The experimental results suggest that the incorporation of nitrogen in high-*k* gate dielectric needs to be carefully control for metal gate device due to the degradation of most of electrical characteristics. Moreover, the impacts of nitrogen on charge trapping induced V_{th} instability in high-*k* gate dielectric with metal and poly-Si gates have been extensively studied. A novel phenomenon, which the incorporated nitrogen in high-*k* film played opposite role in charge trapping induced V_{th} instability between the devices with metal and poly-Si gate, was demonstrated for the first time. The results of the research may provide a guideline to optimize the formation of high-*k* gate dielectric for suppressing the charge trapping induced V_{th} instability, and also contribute a better understanding of charge trapping effect in high-*k* gate dielectric. On the other hand, it is not clear why the HfO_2 and HfAlO films show different gate leakage current behavior after incorporating nitrogen. It could be related to the structure of the HfAlO (amorphous) and HfO_2 (fully crystallized) films. We suggest that more work should be done to identify the mechanisms behind this phenomenon.

Appendix

List of Publications

Journal Publications

1. **X. F. Yu**, C. X. Zhu, M. F. Li, A. Chin, M. B. Yu, A. Y. Du, and D. L. Kwong, "Mobility enhancement in TaN metal gate MOSFETs Using Tantalum incorporated HfO_2 gate dielectrics," ***IEEE Electron Device Letter***, vol. 25, no. 7, pp. 501-503, Jul. 2004.

2. **X. F. Yu**, C. X. Zhu, M. F. Li, A. Chin, A. Y. Du, W. D. Wang, and D. L. Kwong, "Electrical characteristics and suppressed boron penetration behavior of thermally stable HfTaO gate dielectrics with polycrystalline-silicon gate," ***Applied Physics Letter***, vol. 85, no. 14, pp. 2893-2895, Oct. 2004.

3. **X. F. Yu**, C. X. Zhu, M. B. Yu, and D. L. Kwong, "Improvements on surface carrier mobility and electrical stability of MOSFETs using HfTaO gate dielectric," ***IEEE Transactions on Electron Devices***, vol. 51, no. 12, pp. 2154-2160, Dec. 2004.

4. **X. F. Yu**, M. B. Yu and C. X. Zhu, "Advanced HfTaON/SiO_2 gate stack with high mobility and low leakage current for low standby power application," ***IEEE Electron Device Letter***, vol. 27, no. 6, pp. 498-501, Jun. 2006.

5. **X. F. Yu**, M. B. Yu, and C. X. Zhu, "Effective suppression of Fermi-level pinning

in poly-Si/HfO_2 gate stack by using poly-SiGe gate," ***Applied Physics Letter***, vol. 89, no. 16, 163508, Oct. 2006.

6. **X. F. Yu**, M. B. Yu, and C. X. Zhu, "A comparative study of HfTaON/SiO2 and HfON/SiO2 gate stacks with TaN metal gate for advanced CMOS application," ***IEEE Transactions on Electron Devices***, vol. 54, no. 2, pp. 284-290, Feb. 2007.

7. **X. F. Yu**, M. B. Yu, and C. X. Zhu, "Impact of nitrogen in HfON gate dielectric with metal gate on electrical characteristics, with particular attention to threshold voltage instability," ***Applied Physics Letter,*** vol. 90, no. 10, 103502, Mar. 2007.

8. **X. F. Yu**, J. D. Huang, M. B. Yu, and C. X. Zhu, "Effect of gate doping concentration on leakage current in n^+ poly-Si/HfO_2 and examination of leakage paths by conducting atomic force microscopy," accepted by ***IEEE Electron Device Letter***.

9. **X. F. Yu**, M. B. Yu, and C. X. Zhu, "The role of nitrogen on V_{th} instability in HfAlON high-*k* gate dielectric with metal and poly-Si gate electrodes," accepted by ***IEEE Transactions on Electron Devices***.

Conference Publications

1. **X. F. Yu**, C. X. Zhu, Q. C. Zhang, N. Wu, H. Hu, M. F. Li, A. Chin, D. S. H. Chan, W. D. Wang, and D. L. Kwong, "Improved crystallization temperature and interfacial properties of HfO_2 gate dielectrics by adding Ta_2O_5 with TaN metal gate," ***2003 International Semiconductor Device Research Symposium (ISDRS-03)***, Dec. 2003, Washington D.C., USA.

2. **X. F. Yu,** C. X. Zhu, X. P. Wang, M. F. Li, A. Chin, A. Y. Du, W. D. Wang and D. L. Kwong, "High mobility and excellent electrical stability of MOSFETs using a novel HfTaO gate dielectric," ***IEEE Symposium on VLSI Technology 2004 (VLSI-2004)***, pp. 110-111, Jun. 2004, Honolulu, USA.

3. **X. F. Yu**, C. X. Zhu, M. B. Yu, M. F. Li, A. Chin, C. H. Tung, D. Gui, and D. L. Kwong, "Advanced MOSFETs using HfTaON/SiO_2 gate dielectric and TaN metal gate with excellent performances for low standby power application," ***IEEE International Electron Device Meeting 2005 (IEDM-2005)***, pp. 27-30, Dec. 2005, Washington D.C., USA.

4. M. F. Li, C. X. Zhu, X. P. Wang, and **X. F. Yu**, " Novel hafnium-based compound metal oxide gate dielectrics for advanced CMOS technology," ***12th Workshop on Gate Stack Technology and Physics***, keynote speech, Feb. 2007, Mishima , Japan.