NOVEL DEVICES FOR ENHANCED CMOS PERFORMANCE

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NATIONAL UNIVERSITY OF SINGAPORE

2006

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(B.Eng. (Hons.) NUS)

A THESIS SUBMITTED

FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2006

Novel Devices for Enhanced CMOS Performance

ABSTRACT

Complementary Metal Oxide Semiconductor (CMOS) transistors form the basis of many integrated circuit products, such as microprocessor, random access memory (RAM), and digital signal processor (DSP). Continual transistor miniaturization, including scaling down of the transistor gate length and gate dielectric thickness, has been the technology trend for the past few decades. Aggressive CMOS transistor scaling has driven CMOS transistors into the nanoscale regime, making it the most widespread nanotechnology in production today. Further transistor scaling becomes increasingly challenging and faces many difficulties related to physical limitations. A new and emerging trend is the exploration of alternative ways to enhance CMOS transistor performance besides size reduction. The proposed research will be on investigation of novel CMOS transistor structures to enhance performance. The main focus will be on different schemes to form strained silicon transistors for enhanced performance over conventional silicon CMOS transistors where the silicon is not strained. When the crystal lattice of silicon is strained, the electronic properties of silicon will be modified. By engineering the strain introduced, the strain-induced modification of electronic properties can be made to improve the mobility of carriers (*i.e.* electrons and holes) in silicon. This leads to a higher drive current for CMOS transistors and a corresponding increase in speed of integrated circuits formed using these transistors. Faster integrated circuit speed enables new products or applications with faster computational power or increased functionality.

ACKNOWLEDGEMENTS

First and foremost, I would like to thank my main advisor, A/Prof Ganesh S Samudra for his immense guidance and support through these 4 years of my PhD candidature. I have learnt a lot from him, especially in the field of device physics and TCAD simulation work. He has been extremely supportive and has given me the freedom to explore and try out new ideas. I still remember the time when I first ask him what the main focus of my work is about and his answer was "The sky's the limit!".

I wish to also thank to my other advisor, Dr Yee-Chia Yeo, who has provided me with a lot of guidance and advice these 2 years. I will miss all the long conversations which we always begin on-track but wandered out of scope when new ideas come to our minds. I have benefited a lot through the interactions with members of his research group, both during and after the weekly meetings. In my opinion, the collaborative and enjoyable atmosphere in our group is really unique and I'm proud to be part of it.

Special thanks to my research buddy, Kah Wee, who has been a great partner in terms of research work as well as a great friend. I'll never forget the times when we stayed overnight in the cleanroom, running processes and rushing the manuscript for conferences when it is only hours away from the submission dateline. I'll also miss all the entertaining conversations and jokes we shared during lunch and while waiting for processes to complete in the cleanroom.

I wish to express the genuinely enjoyable insights and exchange of perspectives between the official as well as unofficial mentors from Chartered Semiconductors. I would like to thank Dr. Francis Benistant who has given me the chance to learn TCAD simulation and for providing me with the resources to run my never-ending simulation jobs, and the aggressive optimism of Dr. Liu Jinping whose enthusiasm continues to propel endlessly. To the Special Project students, I am grateful for having a wonderful research atmosphere to work in. Some direct contributors which cannot go without mention, Vincent Leong for the TCAD calibration training and valuable comments on TCAD work.

And I would also want to take this opportunity to dedicate a big thank you to a very special person - my wife who has been in many ways very supportive and considerate during my entire PhD candidature. Special mention also goes to my parents, siblings and friends whom knowingly or not giving me the most appreciative support.

Thank you all!

TABLE OF CONTENTS

ABSTRACT i

ACKNOWLEDGEMENT ii

TABLE OF CONTENTS iv

LIST OF FIGURES viii

LIST OF TABLES xviii

LIST OF SYMBOLS xix

LIST OF ABBREVIATIONS xx

CHAPTER 1

Literature Review 1

1.1 Motivation 1

1.2 Background 3

1.2.1 Present Technology Trend : Novel Devices and Architecture for Enhanced Performance CMOS Performance 3

1.2.2 Channel Strain Engineering 5

1.2.3 Silicon-On-Insulator (SOI) for reduced parasitic capacitance C 11

1.3 Objectives of the research 11

1.4 Outline of the report 12

CHAPTER 2

Source Drain On DEpletion Layer (SDODEL) for Reduced Junction Capacitance 13

2.1 Background 13

2.2 Simulation Results 15

2.2.1 Reduction in Junction Capacitance 15

2.3 Experimental Results 20

2.3.1 Reduction in Junction Capacitance 22

2.3.2 Subthreshold Characteristics 23

2.3.3 Verification of restoration of V_t though simulation 24
2.3.4 Circuit Speed Measurement 25
2.3.5 Breakdown Voltage 26
2.3.6 Junction Leakage. 27
2.3.7 Simulation of SDODEL transistors at shorter gate lengths 28
2.4 Summary 30

CHAPTER 3

Fabrication of Strained Si / relaxed SiGe CMOSFETs 31
3.1 Background 31
3.2 Device Fabrication 33
3.3 Electrical Characterization 34
3.3.1 Drive Current Enhancement 34
3.3.2 Sub-threshold Characteristics 37
3.3.3 Circuitry Speed 42
3.4 Summary 43

CHAPTER 4

Characterization of Strained MOSFET structures with S/D Stressors . 45
4.1 Background 45
4.2 MOSFET Structure Fabrication 47
4.2.1 Strained MOSFET Structure Fabrication 47
4.2.2 Strain Characterization 49
4.3 Electron Dispersion Spectroscopy (EDS) Analysis 54

CHAPTER 5

Strained nMOSFETs using SiC S/D Regions 57
5.1 Strained nMOSFETs with SiC S/D on Bulk substrate 57
5.1.1 Background 57
5.1.2 Device Fabrication 59

5.1.3 Electrical Characterization ……62
A. *I-V Characteristics* ……62
B. *P-N Junction Characteristics* …… 67
5.2 Strained nMOSFETs with SiC S/D on SOI substrate ……69
5.2.1 Background……69
5.2.2 Device Fabrication ……70
5.2.3 Electrical Characterization ……74
A. I_{Dsat} *Dependence on Gate Length* L_G *and Device Width W* … 74
B. I_{Dsat} *Dependence on Channel Orientation* …… 76
C. *Dual Stressors Effect on* I_{Dsat} *and Dependence on Channel Orientation* …… 80
5.3 Summary …… 85

CHAPTER 6

Strained pMOSFETs with Ge condensed S/D Regions …… 87
6.1 Strained SOI pMOSFETs with Condensed SiGe S/D ……87
6.1.1 Background ……87
6.1.2 Device Fabrication ……89
6.1.3 Electrical Characterization ……91
6.1.4 Material Characterization ……96
6.2 Strained UTB pMOSFETs with Condensed SiGe S/D ……99
6.2.1 Background ……99
6.2.2 Optimization of Device Structure and Process Conditions for Increased Strain Effects …… 100
6.2.3 Fabrication of Strained UTB pMOSFETs with SiGe S/D ……101
6.2.4 Electrical Characterization ……105
6.3 Summary ……109

CHAPTER 7

Conclusion …… 110
7.1 Summary …… 110
7.1.1 Source / Drain On Depletion Layer (SDODEL) CMOSFET for Reduced Parasitic Capacitance …… 110

7.1.2 Strained Si on Relaxed SiGe MOSFET 110
7.1.3 Material Characterization of Strained Si MOSFET Structures 111
7.1.4 Strained nMOSFETs with SiC S/D Regions 111
7.1.5 Strained pMOSFETs with Condensed SiGe S/D Regions 112
7.2 Future work 112
References 113
List of Conference / Publication 121
List of Patents 123

LIST OF FIGURES

Figure 1.1 : Germanium has a larger lattice constant (5.658Å) than Silicon (5.431Å). By Vegard's law. the lattice constant of $Si_{1-x}Ge_x$ will have a larger lattice constant than Si. When silicon is epitaxially grown on $Si_{1-x}Ge_x$, the silicon layer will be stretched biaxially ……....……..…….……..…… 5

Figure 1.2 : Different type of globally strained silicon substrate wafers. (a) Strained Si / Relaxed SiGe (b) Strained silicon / Relaxed SiGe – On – Insulator (SGOI) (c) Strained Si Directly – On – Insulator (SSDOI) ……. 7

Figure 1.3 : Various techniques to introduce different type of strain to the channel region of MOS devices …… 8

Figure 1.4 : Valence band structure of (a) unstrained Si and (b) tensile strained Si on $Si_{1-x}Ge_x$. Tensile strain lowers the energy of the heavy hole and spin-orbit sub bands relative to the light hole sub band and modifies the shape of the sub bands [28] …..…… 9

Figure 1.5 : Schematic representation of the constant energy ellipses for (a) unstrained Si and (b) strained Si [10] ……..…… 10

Figure 1.6 : Conduction band splitting and sub-band energies lineups of Si under biaxial tensile strain [10] ……..……..... 10

Figure 2.1 : Schematic illustration of Silicon On DEpletion Layer (SODEL) nMOSFET. The counter-doped layer (shaded) is of the same doping type as the source/drain regions. As a result of the counter-doped layer, an enlarged depletion region as indicated by the gray region and bounded by dashes is achieved. SODEL pMOSFET has the same structure but of opposite dopant-type …….……...… 14

Figure 2.2 : Schematic of a simulated Source/Drain on Depletion Layer (SDODEL) nMOSFET transistor structure showing counter-doped regions (shaded) beneath the source/drain regions. The counter-doped regions are of the same doping type as the source/drain regions. As a result of the counter-doped regions, the depletion region as indicated by the gray region and bounded by dashes is significantly enlarged over that of the control transistor. The original boundary of the depletion region in the control transistor is indicated by dotted lines. SDODEL pMOSFET has the same structure but of opposite dopant-type…….....…….……...…… 15

Figure 2.3 : (a) Simulated SDODEL nMOSFET device with a gate length of 65nm and (b) Concentration profile of dopants along a vertical line A-A' as depicted in (a) …..... 16

Figure 2.4 : (a) Simulated SODEL nMOSFET device with a gate length of 65nm and (b) Concentration profile of dopants along a vertical line A-A' as depicted in (a) …..... 17

Figure 2.5 : (a) Simulated SDODEL pMOSFET device with a gate length of 65nm and (b) Concentration profile of dopants along a vertical line B-B' as depicted in (a) ……. 18

Figure 2.6 : (a) Simulated SODEL pMOSFET device with a gate length of 65nm and (b) Concentration profile of dopants along a vertical line B-B' as depicted in (a) …..... 19

Figure 2.7 : Measured SIMS results for n-channel SDODEL at S/D regions ……....……..... 21

Figure 2.8 : Measured SIMS results for p-channel SDODEL at S/D regions ……...…… 21

Figure 2.9 : Measured junction capacitance C_j as a function of drain-body bias V_{db} for SDODEL and control (a) nMOSFETs and (b) pMOSFETs, showing significant reduction of C_j for the SDODEL device ……..… 22

Figure 2.10 : Box plot showing a comparison of junction capacitance between SDODEL and control n and pMOSFET devices ……..….. 23

Figure 2.11 : Sub-threshold characteristics for SDODEL and control nMOSFETs, at V_{ds} = 0.05V and 1.95V …….…... 24

Figure 2.12 : Gate delay of an inverter stage plotted against the sum of reciprocals of the drive currents of the n and pMOSFETs. The gate length is 0.16 μm. The device widths are 10 μm and 20 μm for the nand pMOSFETs, respectively. Experimental data is obtained from ring oscillators from different dies. Reduction of the inverter gate delay is as high as 15% at the same ($|I_{dsat,n}^{-1}| + |I_{dsat,p}^{-1}|$) at V_{dd} = 1.8 V ……..... 26

Figure 2.13 : Box plot showing a comparison of junction leakage current between SDODEL and control Si MOSFETs …….….. 28

Figure 2.14 : Simulated capacitance reduction and off-state leakage current I_{off} as a function of gate length. Significant reduction in junction capacitance for SDODEL nMOSFETs can be observed for gate lengths down to 50 nm, while keeping I_{off} close to the specifications of the International Technology Roadmap for Semiconductors (ITRS) [1] …… 29

Figure 3.1 : (a) Graded $Si_{1-x}Ge_x$ and relaxed $Si_{1-x}Ge_x$ layer helps to reduce the amount of defects at the relaxed $Si_{1-x}Ge_x$ surface. Relaxed Si has a smaller lattice constant than relaxed $Si_{1-x}Ge_x$ …….…….. 32

Figure 3.1 : (b) Si atoms will try to retain the in-plane lattice constant of the relaxed $Si_{1-x}Ge_x$ layer below. As a result the Si layer becomes tensile strained in the *x* and *y* directions (biaxial) ……..……..…… 33

Figure 3.2 : Schematic showing cross-section of CMOSFET structures fabricated on strained Si / relaxed $Si_{1-x}Ge_x$, for x = 0.15 and 0.2. A twin-well process with STI isolation was employed ……..…….... 34

Figure 3.3 : I_{DS}-V_{DS} characteristics of 0.18 μm strained and control nMOSFETs. Enhancement of about 16% and 20% in linear drain current is obtained for strained nMOSFETs with 15% Ge and 20% Ge (in the relaxed SiGe layer) respectively. I_{DS} enhancement at high V_{DS} is observed at low gate overdrive but diminishes at high gate overdrive due to self heating effects ……... 35

Figure 3.4 : I_{DS}-V_{DS} characteristics of 20 μm strained and control nMOSFETs. Enhancement of about 65% and 75% in linear drain current is obtained for strained nMOSFETs with 15% Ge and 20% Ge (in the relaxed SiGe layer) respectively. This enhancement is much higher than that in the short channel (0.18 μm) strained devices. No degradation in I_{DS} enhancement in the saturation regime at high gate overdrive ……..…… 36

Figure 3.5 : I_{DS}-V_{DS} of strained and control nMOSFETs with a gate length of 0.18 μm. A decrease in threshold voltage V_t along with degradation in sub-threshold characteristics is observed in the strained devices ……. 38

Figure 3.6 : V_t roll-off characteristics of the strained and control nMOSFETs. V_t decreases with increasing Ge % in the relaxed SiGe layer ……..…… 38

Figure 3.7 : Bandgap alignment (Type II) of strained Si on relaxed $Si_{1-x}Ge_x$ buffer layer substrate……..…….. 39

Figure 3.8 : (a) Presence of misfit dislocations found at the strained si and relaxed SiGe interface and (b) top-view photo-emission analysis of a wide channel strained Si transistors. A localized leakage path is observed. [11] ……..……..…….. 40

Figure 3.9 : Box plot showing measured I_{off} values over a range of 5 dies for control and strained nMOSFETs at gate length of 0.18 μm ……..……..……. 41

Figure 3.10 : Comparison of overlap capacitance C_{OV} between control and strained nMOSFETs. With increasing Ge % in the relaxed SiGe layer, overlap capacitances increases . 42

Figure 4.1 : Schematic of transistor structures with epitaxially grown SiGe or SiC in the source/drain regions to form source/drain (S/D) stressors ……. 48

Figure 4.2 : Cross-sectional transmission electron microscopy (TEM) image of a structure with (a) $Si_{0.75}Ge_{0.25}$ S/D stressors and (b) $Si_{0.99}C_{0.01}$ S/D stressors. The gate electrode has a feature size of 35 nm and the pitch of the gate array pattern is 240 nm ……. 49

Figure 4.3 : A high magnification HRTEM image of a transistor structure with $Si_{0.75}Ge_{0.25}$ stressors in the source/drain region. The region enclosed by the dashed line features a SiGe material which was pseudomorphically grown on the recessed Si source/drain region …….……. 50

Figure 4.4 : (a) The reciprocal space diffractogram is obtained by Fast Fourier Transform (FFT) of a selected region in the TEM image of Figure 4.3. The diffractogram is then filtered to obtain (b) the (002) reflection and (c) the (220) reflection, which contain information about the lattice spacings in the vertical and lateral directions, respectively. The intensity profile for the (002) reflection is shown in (d). The separation between the intensity peaks is twice the separation *d* from *O* to each peak, and can be translated into real space lattice spacing *a* using $d = 2\pi/a$ …..... 51

Figure 4.5 : The distribution of strain components in a transistor structure with $Si_{0.75}Ge_{0.25}$ stressors in the source/drain regions. (a) Large lateral compressive strain is observed near the heterojunction and directly beneath the Si surface. (b) The Si lattice is stretched in the vertical direction, and a vertical tensile strain is induced …….……52

Figure 4.6 : The distribution of (a) the lateral strain component and (b) the vertical strain component in a transistor structure with $Si_{0.99}C_{0.01}$ source/drain stressors. A relatively large lateral tensile strain ε_{xx} was induced in Si near the Si-$Si_{0.99}C_{0.01}$ heterojunction. The magnitude of the lateral tensile strain decreases with increasing *z*. The $Si_{0.99}C_{0.01}$ lattice also interacts with the Si lattice to induce a vertical compressive strain in the Si channel ……..... 53

Figure 4.7 : Distribution of the simulated lateral strain component ε_{xx} (in %) in the Si channel and $Si_{0.987}C_{0.013}$ S/D regions, using a finite element method for gate length of (a) 30 nm and (b) 50 nm. In this simulation, a recess depth of 20 nm was used. The horizontal distance from the $Si_{0.987}C_{0.013}$−strained-Si heterojunction at the Si surface is denoted by *x* while the vertical distance from the Si surface is denoted by *y*….. 54

Figure 4.8 : A simple schematic illustrating how EDS in a TEM system works. X-rays generated by the interaction of the incident electrons with the sample are collected by the detector which feeds the signal to a computer to generate elemental spectrums.……..…….. 55

Figure 4.9 : An example of a TEM image which illustrates the elemental composition of the TEM sample ……... 56

Figure 5.1 : (a) Schematic diagram of a proposed nMOSFET structure with selective epitaxially grown SiC in the source/drain (S/D) regions. The inset illustrates a magnified Si channel and SiC S/D sidewall heterojunction which induces a vertical compressive strain component, leading to a lateral tensile strain in the channel of the nMOSFET due to smaller lattice constant of SiC with respect to Si. (b) pMOSFET structure with selective epitaxially grown $Si_{1-x}Ge_x$ in the source/drain. Due to larger lattice constant of $Si_{1-x}Ge_x$, a compressive strain is induced in the channel of the pMOSFET ……..….. 59

Figure 5.2 : Ratio of amount of carbon in substitutional sites C_{Sub} to the total amount of carbon incorporated C_{Total}, denoted by η (substitutional efficiency factor or substitutionality) plotted against C_{Total}. η decreases with C_{Total}, implying the limitations of introducing high carbon %. Results are benchmarked with previous work on SiC epitaxy [55] …….. 61

Figure 5.3 : (a) Cross sectional TEM image of a 50 nm gate length nMOSFET with $Si_{0.987}C_{0.013}$ S/D. The spacers and a hardmask that covered the metal gate during the selective epitaxy of $Si_{0.987}C_{0.013}$ were removed. (b) Conduction band profile from the source to the drain, illustrating enhanced electron injection velocity from the source into the strained-Si channel ……..…….. 63

Figure 5.4 : (a) Output characteristics of 50 nm gate length nMOSFET with $Si_{0.987}C_{0.013}$ S/D regions, demonstrating 50% drive current I_{Dsat} enhancement at a gate over-drive (V_{GS} - V_t) of 1.0 V. Inset shows comparable extracted series resistance, attributing the majority of the drive current enhancement to strain effects. (b) Drain current I_{DS} enhancement factor as a function of drain bias V_{DS} and gate overdrive ($V_{GS} - V_t$). I_{DS} enhancement increases with higher drain bias and decreases with increasing gate over-drive ……..….. 64

Figure 5.5 : (a) The extracted electron mobility shows 100% enhancement at low effective vertical field regime but decreases at higher effective field. The mobility is extracted using the linear drain current equation at low V_{DS} = 0.1 V. (b) Drive current I_{Dsat} as a function of L_G, as obtained from the fabricated devices, showing increasing I_{Dsat} enhancement with decreasing L_G ……..... 65

Figure 5.6 : (a) Transconductance G_m versus gate over-drive, $V_{GS} - V_t$, for uniaxial tensile strained nMOSFET. A 40% enhancement in G_m is observed over the control device. (b) Transconductance G_{mmax} as a function of gate length for control and strained NMOSFET. G_{mmax} improvement can be observed down to L_G=50 nm ……. 66

Figure 5.7 : (a) I_{DS}-V_{GS} characteristics of both strained and control device. The inset plots the subthreshold swing versus physical gate length L_G of both strained and control devices. (b) *C*-*V* characteristics showing the elimination of gate depletion effects by the use of metal gate electrode ……... 67

Figure 5.8 : (a) Comparable N+ diode junction leakage measurement at different voltage bias for both control and nMOSFET with SiC S/D. (b) Temperature dependence of junction leakage currents for both devices implies similar current leakage mechanisms ……..… 68

Figure 5.9 : Comparable junction capacitance between control and nnMOSFETs with SiC S/D indicate full speed benefit feasibility from I_{Dsat} enhancement ……..... 69

Figure 5.10 : Cross sections of (a) control SOI nMOSFET, and SOI nMOSFETs with silicon-carbon $Si_{1-y}C_y$ epitaxial layer formed on (b) recessed and (c) unrecessed source/drain (S/D) regions. (d) Picture of a SOI nMOSFET with raised $Si_{0.99}C_{0.01}$ S/D regions, as obtained using Scanning Electron Microscopy (SEM). A SiON hardmask caps the TaN gate during the selective epitaxy process. Good $Si_{0.99}C_{0.01}$ epitaxial growth selectivity is demonstrated …….. 71

Figure 5.11 : Process sequence employed in the fabrication of SiC S/D transistors. TaN metal gate is used to eliminate the polysilicon gate depletion effect ……... 71

Figure 5.12 : (a) Transmission electron microscopy (TEM) image of SOI transistor featuring TaN metal gate, high-k gate dielectric, and $Si_{0.99}C_{0.01}$ S/D regions. (b) High-resolution TEM image and Fast Fourier transform (FFT) diffractograms, revealing the excellent crystalline quality of the $Si_{0.99}C_{0.01}$ region after S/D implant and dopant activation at 950°C for 30 s ……..… 72

Figure 5.13 : High resolution XRD spectra shows excellent crystalline quality of the SiC film on Si with 1% substitutional carbon ……... 73

Figure 5.14 : (004) and (224) reciprocal space maps show perfect alignment between the SiC and Si peaks, indicating pseudomorphic epitaxial growth ……..... 73

Figure 5.15 : (a) I_{DS}-V_{DS} characteristics for 90 nm gate length nMOSFET with SiC selectively grown on recessed S/D regions. Drive current I_{Dsat} enhancement of 25% is observed (b) nMOSFET with SiC S/D formed on unrecessed regions shows larger I_{Dsat} as compared to the control transistor ……..…. 74

Figure 5.16 : (a) The I_{DS}-V_{GS} characteristics of a 90 nm gate length SiC S/D nMOSFET shows higher linear and saturation drive current over the control SOI transistor. (b)

Transconductance G_m of SiC S/D nMOSFET shows ~21% improvement over the unstrained control device ……... 75

Figure 5.17 : (a) Drive current I_{Dsat} enhancement increases with decreasing gate length L_G. Raised SiC formed on recessed S/D regions shows a higher I_{Dsat} improvement. (b) Increasing device width W leads to a higher drain current enhancement …….. 76

Figure 5.18 : The plan view of a nMOSFET formed on a (001) surface with an arbitrary source-to-drain or channel orientation θ. When θ = 0º, the channel orientation is along a [110] crystal direction ……..… 77

Figure 5.19 : (a) While the I_{Dsat} of the control nMOSFET is independent of channel orientation, a uniaxial strained nMOSFET with SiC S/D has the highest I_{Dsat} when its channel direction is oriented along the [010] crystal direction. (b) Both I_{Dsat} and G_m improvement due to uniaxial tensile strain are the largest for the [010]-oriented nMOSFET, in agreement with piezoresistance properties of bulk Si …… 77

Figure 5.20 : (a) Six-fold degenerate conduction band valleys in unstrained Si. (b) In strained Si with uniaxial tensile strain along [110], preferential electron population in valleys 5 and 6 (in gray, top and bottom left) occurs. When uniaxial tensile strain is applied along [010] (bottom right), anisotropic population of Δ_4 valleys could additionally lead to mobility enhancement [27] ……. 79

Figure 5.21 : The longitudinal piezoresistance coefficient π_l is the most negative in the [010] direction (or θ = 45°). Applying a tensile longitudinal stress in the [010] direction will lead to the largest reduction in resistance, compared to other directions ….. 79

Figure 5.22 : TEM image of a SOI nMOSFET with SiC S/D and tensile stress etch-stop-layer ESL ……. 80

Figure 5.23 : I_{DS}-V_{DS} characteristics of nMOSFETs with SiC S/D and tensile stress SiN ESL shows 55% enhancement in I_{Dsat} at a gate overdrive of 1V ……... 81

Figure 5.24 : Significant I_{Dsat} enhancement contributed by SiC S/D and SiN ESL, with highest improvement observed for [010]-oriented nMOSFETs ……..…. 81

Figure 5.25 : Drive current I_{Dsat} of SiC S/D device shows strong dependence on channel orientations, consistent with the directional dependence of piezoresistance coefficients ……..……. 82

Figure 5.26 : Significant increase in G_m of 69% is observed for SiC S/D and SiN liner nMOSFETs over control devices ……..... 83

Figure 5.27 : Strained devices oriented along [010] channel show higher maximum G_{msat} enhancement than those oriented along [110] channel direction ……... 83

Figure 5.28 : Series resistance extraction at high gate bias shows 10% improvement in R_{series} for strained device due to the raised S/D ……. 84

Figure 5.29 : Comparable gate leakage characteristics of both strained and control devices, showing no strain induced degradation of gate oxide quality ……..... 85

Figure 6.1 : Stress simulation results using TAURUS process simulator. The average lateral strain ε_{xx} (calculated from SiGe source-end to the centre of the transistor channel, and at a depth of 5 nm below the Si/SiO_2 interface) as a function of SiGe embedded depth is plotted for various body thicknesses. A higher average strain in the Si channel can be achieved with deeper SiGe embedded depth and thinner body thickness. The inset shows the transistor structure adopted in the simulation……. 88

Figure 6.2 : Schematic showing the formation of SiGe S/D stressors. (a) After forming the gate stack and spacers in a conventional CMOS process, (b) SiGe is selectively grown on the S/D regions. Oxidation or Germanium condensation is then performed to drive Ge into the S/D regions to give the final structure as shown in (c) ……... 89

Figure 6.3 : Device fabrication sequence, showing the insertion of a SiGe selective epitaxy step and a Ge condensation step in a standard process flow ……. 90

Figure 6.4 : TEM image of a transistor structure after Ge condensation. The Ge was driven into the S/D regions during the Ge condensation process ……. 90

Figure 6.5 : I_{DS}-V_{DS} characteristics of strained pMOSFET with condensed SiGe S/D regions at a gate length of 90 nm, showing significant 37% drive current I_{Dsat} enhancement over the control pMOSFET. Inset plots the subthreshold characteristics for a pair of closely-matched strained and control devices with comparable off-state leakage I_{off}, DIBL, and subthreshold swing …….. 91

Figure 6.6 : Inter-band energy splitting increases with increasing strain ε_{xx} (open and closed circle symbols). Increasing uniaxial compressive strain ε_{xx} along the [110] channel direction reduces the hole effective mass in the same direction (square symbols). The simulation results were obtained using k·p effective mass theory, employing a 6×6 Luttinger-Kohn Hamiltonian with strain terms included. Hole quantization effects in the Si inversion layer of p-MOSFETs was modeled using a triangular well approximation. The vertical electric field at the Si surface is given by E_s ……..... 92

Figure 6.7 : Drive current I_{Dsat} as a function of L_G, before (solid symbols) and after correction (open sybols) for series resistance R_s. In both cases, I_{Dsat} enhancement increases with decreasing L_G. Improvement in *Rs* accounts for 13% in I_{Dsat} enhancement …93

Figure 6.8 : I_{off}-I_{on} characteristics comparing the drive current performance of control and strained p-MOSFET with condensed SiGe S/D regions, demonstrating 28% improvement in the on-state saturation current I_{on} at a fixed off-state leakage I_{off} of 100 nA/μm ……. 94

Figure 6.9 : (a) Comparison of transconductance G_m at the same gate overdrive illustrates an improvement of 60% (b) Maximum transconductance G_{mmax} as a function of gate length. Enhancement in G_m increases with decreasing gate length ……..…... 95

Figure 6.10 : (a) High resolution TEM image showing the SiGe S/D formed by Ge condensation and the adjacent channel region. Diffractogram at a specific position in the channel region reveals the presence of lateral compressive strain (b) Lateral strain profile at various depths below the Si surface, extracted from an analysis of the HRTEM image, showing lateral compressive strain along the [110] channel direction ….. 96

Figure 6.11 : Profile of Ge concentration of as-deposited SiGe sample (no Ge condensation) and SiGe samples that went through different Ge condensation conditions, as obtained using Auger Electron Spectroscopy. Different temperatures (900-1000°C) and oxidation durations were used. The Ge condensation process clearly increases the Ge concentration …….…..... 97

Figure 6.12 : (a) Assuming a final device structure with a Ge content of 50% in the S/D, (b) an initial SiGe layer with thickness t_{epi} that is assumed to be epitaxially grown and fully oxidized, one can derive the amount of t_{epi} required for different t_{body} (c) ……. 98

Figure 6.13 : (a) TAURUS stress simulations reveal that the induced compressive strain in the transistor channel in Figure 6.1 is largest when SiGe S/D regions extend to the buried oxide (BOX). (b) The channel strain induced increases with reduced body thickness and increased Ge content in the S/D regions ……..…101

Figure 6.14 : (a) Schematic illustrating selective epitaxial growth of SiGe layers on S/D regions of pMOSFET structure before condensation (oxidation) process. (b) Condensation of SiGe layers on the S/D regions in 3 (a), Ge is driven into the Si S/D regions in the process ……102

Figure 6.15 : Thickness of oxide formed by oxidation of $Si_{0.75}Ge_{0.25}$ layers on Si S/D regions of pMOSFET structure as a function of time …….…... 102

Figure 6.16 : Ge content depth profile (obtained from EDS of TEM samples) for an optimized S/D Ge epitaxial and condensation process and an unoptimized one. With an unoptimized process, Ge content drops with increasing depth, with the SiGe embedded at a depth of only half that of the SOI body thickness ……..... 104

Figure 6.17 : (a) TEM image of a 70 nm gate length strained UTB pMOSFET with condensed SiGe S/D regions. (b) EDS analysis on magnified TEM image at S/D region showing Ge content of more than 40% across the entire S/D region. Diffractogram reflects good crystallinity. (c) HRTEM image of the channel region beneath the gate. The body thickness is 8 nm ……...…….…. 104

Figure 6.18 : (a) I_{DS}-V_{DS} characteristics of $Si_{0.54}Ge_{0.46}$ S/D and control UTB transistors with L_G = 70 nm for gate overdrives $|V_{GS} - V_t|$ of 0 to 1 V in steps of 0.2 V. The strained $Si_{0.54}Ge_{0.46}$ S/D pMOSFET shows more than 70% increase in I_{DS} at a gate overdrive of 1 V. (b) I_{Dsat} enhancement increases with decreasing gate length L_G due to the closer proximity of SiGe S/D regions to the Si channel, which leads to larger compressive strain in the channel ……..… 106

Figure 6.19 : Strained $Si_{0.54}Ge_{0.46}$ S/D pMOSFETs show significant drive current enhancement over the control devices. The measured I_{Dsat} gain is approximately half of that in I_{Dlin} due to the smaller sensitivity of I_{Dsat} on channel mobility gain …… 106

Figure 6.20 : (a) Extracted series resistance for the $Si_{0.54}Ge_{0.46}$ S/D and control devices is comparable. At high gate-overdrive and at low V_{DS}, the channel resistance is assumed to be negligible, the overall source-to-drain resistance mainly contributed by resistance at the source and drain side. (b) I_{DS}-V_{GS} characteristics of $Si_{0.54}Ge_{0.46}$ S/D and control UTB pMOSFETs. Strained UTB pMOSFET devices with condensed $Si_{0.54}Ge_{0.46}$ S/D shows improved short channel characteristics over control devices …….. 107

Figure 6.21 : (a) $Si_{0.54}Ge_{0.46}$ S/D pMOSFET shows improved subthreshold swing over control devices for all gate lengths. Excellent subthreshold swing of less than 70 mV/decade is obtained for the $Si_{0.54}Ge_{0.46}$ S/D pMOSFET. (b) DIBL characteristics against physical gate length for both control and strained devices ……... 108

Figure 6.22 : (a) Transconductance *Gm* as a function of gate bias VGS for both $Si_{0.54}Ge_{0.46}$ S/D and control pMOSFETs at both high and low V_{DS}. (b) Increasing G_{mmax} with decreasing gate length L_G. $Si_{0.54}Ge_{0.46}$ S/D pMOSFETs reveal a larger increase in G_{mmax} with reducing L_G due to the larger strain effect of the SiGe S/D regions ... 108

LIST OF TABLE

Table 2.1 : Comparison of electrical parameters of SDODEL, SODEL and control nMOSFET structures. At comparable V_{tlin}, I_{dsat} and I_{off}, reduction in junction capacitance can be observed in both the SDODEL and SODEL nMOSFETs. SODEL nMOSFETs are also noted to have a smaller V_{bd} ……..……....…….. 17

Table 2.2 : Comparison of electrical parameters of SDODEL, SODEL and control pMOSFET structures At comparable V_{tlin}, I_{dsat} and I_{off}, reduction in junction capacitance can be observed in both the SDODEL and SODEL pMOSFETs. SODEL pMOSFETs are also noted to have a smaller V_{bd} ……..……..…. 19

Table 2.3 : By adjustment of V_t implant dose and energy, the V_{tlin} and I_{off} can be matched to that of the control device without degrading the I_{dsat} and junction capacitance ……..... 25

Table 2.4 : Comparison of breakdown voltages, V_{bd} for SDODEL and control MOSFETs for different channel lengths ……..….. 27

LIST OF SYMBOLS

Symbol	Description	Unit
a_{Ge}	Lattice constant of germanium	Å
a_{Si}	Lattice constant of silicon	Å
C_j	Junction capacitance (per unit area)	F/cm^2
ε	Maximum strain between silicon and germanium (=4.2%)	None
ε_{xx}	Strain component in x direction	None
ε_{yy}	Strain component in y direction	None
ε_{zz}	Strain component in z direction	None
G_m	Transconductance	S
I_{DS}	Drain current (per unit width)	A/μm
I_{Dsat}	Drain saturation current (per unit width)	A/μm
I_{off}	Off state current (per unit width)	A/μm
m_0	Free electron mass (=9.1 x 10^{-31}kg)	kg
m_l	Longitudinal effective electron mass	kg
m_t	Transverse mass effective electron mass	kg
μ_{eff}	Effective mobility	cm^2/V-s
N_A	Substrate doping concentration	atoms/cm^3
η	Carbon substitution efficiency	None
S_{xx}	Stress component in x direction	Pa
S_{yy}	Stress component in y direction	Pa
S_{zz}	Stress component in z direction	Pa
t_d	Circuit delay	s
v	Poisson's ratio	None
V_{bd}	Breakdown voltage	V
V_{DS}	Drain voltage	V
V_{GS}	Gate voltage	V
V_{dd}	Supply Voltage	V
V_t	Threshold voltage (Extracted at maximum transconductance)	V
V_{tlin}	Linear threshold voltage (Extracted in linear regime at low V_{DS})	V

V_{Tsat}	Saturation threshold voltage (Extracted in saturation regime at high V_{DS})	V
x	Mole fraction of Ge	None
Y	Young's Modulus	Pa

LIST OF ABBREVIATIONS

BOX	Buried Oxide
CBED	Convergent Beam Electron Diffraction
CMOS	Complimentary Metal-Oxide-Semiconductor
CVD	Chemical Vapour Deposition
DIBL	Drain Induced Barrier Lowering
EDS	Energy Dispersive X-Ray Spectroscopy
ESL	Etch-Stop-Layer
FFT	Fast Fourier Transform
HH	Heavy Hole
HRTEM	High Resolution Transmission Electron Microscopy
ITRS	International Technology Roadmap for Semiconductors
LH	Light Hole
LOCOS	Local Oxidation of Silicon
LPCVD	Low Pressure Chemical Vapour Deposition
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
PECVD	Plasma Enhanced Chemical Vapour Deposition
RTA	Rapid Thermal Annealing
SCE	Short Channel Effects
S/D	Source / Drain
SDE	Source Drain Extension
SDODEL	Source / Drain On Depletion Layer
SEM	Scanning Electron Microscopy
SODEL	Silicon On Depletion Layer
SOI	Silicon-On-Insulator
STI	Shallow Trench Isolation
TCAD	Technology Computer Aided Design
TEM	Transmission Electron Microscopy
UHV	Ultra High Vacuum
UTB	Ultra Thin Body
XRD	X-Ray Diffraction

CHAPTER 1

Literature Review

1.1 Motivation

Device scaling is essential for the continued improvement in CMOS technology. Gordon Moore predicted that the speed performance of integrated circuits would double every 18-24 months. Until now, this is achieved mainly by the down sizing of conventional silicon (Si) CMOS devices. However, with the progression of each technology node, sustaining the performance improvement to meet the ITRS roadmap [1] through scaling alone becomes increasingly difficult to maintain. Therefore, new materials and novel device structures are essential in order to keep up with the expected level of performance improvement as required by the roadmap. In order to propose alternatives for device performance enhancement, it is essential to look at the equation that governs circuitry speed. The time delay of a circuit can be approximated by the simple equation,

$$\text{time delay } t_d = \frac{CV_{dd}}{I} \tag{1.1}$$

where C is the parasitic capacitance, V_{dd} is the supply voltage and I is the transistor drive current. The shorter the time delay t_d, the faster will be the speed at which the circuit operates. According to equation (1.1), there are 3 parameters (C, V_{dd} *and* I) which can affect the speed performance of circuits. By adjustment of one or a combination of any of these 3 parameters, circuitry speed can be improved. The conventional method of device

scaling serves to increase the drive current I. This in turn leads to a reduction in time delay and faster circuitry speed. However, as gate dimensions are reduced further into the sub 100nm regime, suppression of increasingly high off-state current and severe short channel effects becomes difficult. This leads to improved performance at the expense of high power consumption, which is highly undesirable in low standby power applications like laptops and cellular phones. The gate dielectric thickness can also be reduced to increase drive current only to be met with the same problem of high gate leakage currents. There is also little room in reducing supply voltage V_{dd} as reducing the supply voltage will reduce the gate-overdrive, eventually causing a reduction in I. In addition, V_{dd} also needs to be kept as low as possible to keep active power P_{Active} and standby power $P_{Standby}$ to a minimum. The equations are as given.

$$\text{Active Power Consumption } P_{Active} = C.V_{dd}^{2}.f \tag{1.2}$$

$$\text{Standby Power Consumption } P_{Standby} = W.I_{off}.V_{dd} \tag{1.3}$$

On the other hand, reduction in device parasitic capacitance C is another viable option to improve circuit speed performance.

In this thesis, various ways to improve the circuitry speed, by means of either reduction in parasitic capacitance C and/or increase in drive current I, will be explored as the power supply voltage is mainly dictated by power consumption and roadmap requirements.

1.2 Background

1.2.1 Present TechnologyTrend : Novel Devices and Architecture for Enhanced CMOS Performance

As explained earlier in equation (1.1), the key to enhancing circuit performance lies in the manipulation of the 3 parameters (*C, V_{dd} and I).* In a bid for continual performance enhancement and meeting the requirements of the Moore's Law, which until now is heavily reliant on device scaling, there is an ever increasing need to introduce new structures and materials into the present CMOS technology. At present, many types of device architectures and materials are being aggressively explored with the hope of improving CMOS devices performance.

Some of these include the use and implementation of metal gates [2] – [6], high-k gate dielectrics [7], [8], channel strain engineering [9] – [17], silicon-on-insulator (SOI) substrates [18] - [20], shallow junction formation [21] and/or a combination of some of these features [22] for continual improvements in CMOS device performance.

As the gate length and gate dielectric thickness are reduced, the use of polysilicon as the gate material aggravates the problem of poly depletion, high gate resistance and dopant penetration from the gate [1], [2]. To alleviate these problems, some have suggested the use of metal as the gate material [2] – [6]. This not only solves the problem of gate depletion and dopant penetration but also reduces the gate resistance. By eliminating the effects of poly depletion, a higher equivalent oxide capacitance can be achieved. This in turn give rise to an increase in drive current *I*. However, there are

issues related to implementation of metal as the gate material of CMOS device and these include the choice of metal materials, new physics of metal gate dielectric interface and possible schemes of integrating metal gate material into the CMOS process.

In line with the scaling of gate length, the gate dielectric thickness has to be reduced, to increase gate oxide capacitance. However, as the thickness of the gate oxide is reduced, gate leakage and power consumption of the MOS transistors will increase tremendously. One solution would be the use of high-k dielectric in place of silicon dioxide as the gate dielectric. This allows a physically thicker high-k dielectric to achieve the same or lower electrical thickness at a lower leakage current than silicon dioxide [6], [7]. Challenges of using high-k include threshold voltage, V_t instability, mobility degradation and thermal stability [22].

For many years, channel strain engineering [9] - [17] has also been actively pursued to improve drive current *I*. Introduction of appropriate strain, in the channel of MOSFET devices, causes an increase in carrier mobility as a result of smaller carrier effective mass and reduction in scattering. To date, there can be many different ways to introduce strain at the channel region of the devices. The next section will give a more detailed description of the different ways to strain Si

So far, the methods described help to improve circuitry speed by increasing the drive current *I*. As explained earlier, reduction in parasitic capacitance *C* also can help to achieve the same purpose of increasing circuitry speed. One way to reduce *C* is by using

silicon-on-insulator (SOI) substrates [18] - [20] instead of the conventional bulk silicon substrate. However, the high cost of such SOI substrates can be the major deterring factor in its implementation into present CMOS device manufacturing.

1.2.2 Channel Strain Engineering

As mentioned in the previous section, the channel of the MOSFET devices can be strained by various methods to obtain an improvement in mobility and drive current. The various ways of introducing strain can be generally classified into 2 main categories, global strain [9] – [11] and local strain [12] – [17] techniques.

The global strain technique [9] – [11] generally make use of a different material, with a mismatch lattice constant like silicon germanium (SiGe), directly beneath the silicon (Si) channel. The strain induced is biaxial and is already inherent in the substrate right from the beginning of the CMOS process flow.

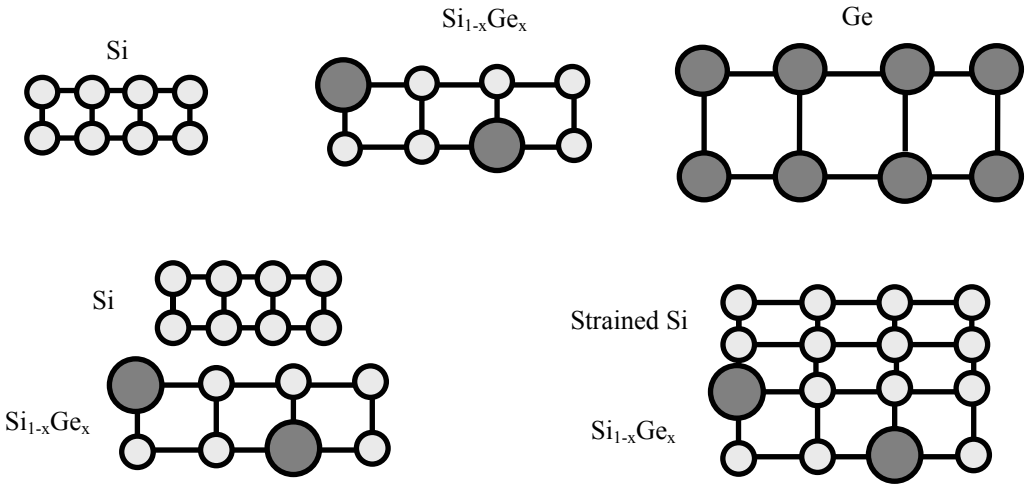


Figure 1.1 : Germanium has a larger lattice constant (5.658Å) than silicon (5.431Å). By Vegard's law. the lattice constant of $Si_{1-x}Ge_x$ will have a larger lattice constant than Si. When silicon is epitaxially grown on relaxed $Si_{1-x}Ge_x$, the silicon layer will be stretched biaxially

Figure 1.1 illustrates how a mismatch material, like SiGe, can induce a biaxial strain in the Si layer above it. Germanium (Ge) has a larger lattice constant (5.658Å) than Si (5.431Å). By Vegard's law, the lattice constant of $Si_{1-x}Ge_x$ is a linear interpolation between the lattice constant of Si and Ge. This is governed by the following expression,

$$a_{Si1-xGex} = xa_{Ge} + (1-x)\, a_{Si} \tag{1.4}$$

where x is the Ge mole fraction and a_{Ge} and a_{Si} are the lattice constant of Ge and Si, respectively. $Si_{1-x}Ge_x$, in the relaxed state, will therefore have a larger lattice constant than Si. When a thin layer of Si is epitaxially grown on relaxed $Si_{1-x}Ge_{x,}$ the Si layer will try to retain the in-plane lattice constant of the underlying $Si_{1-x}Ge_x$. This causes the Si layer to be stretched (tensile strain) biaxially in both directions.

Figure 1.2 shows the different types of globally strained silicon substrate wafers formed using the global strain technique. Figure 1.2 (a) and (b) make use of a graded SiGe layer to form a low-defect density relaxed SiGe layer [23], [24] and a buffer relaxed SiGe layer before a biaxial tensile strained Si layer is epitaxially grown. The substrate in figure 1.2 (c) is formed using (a) and the strained layer is then transferred onto the BOX by wafer bonding [25].

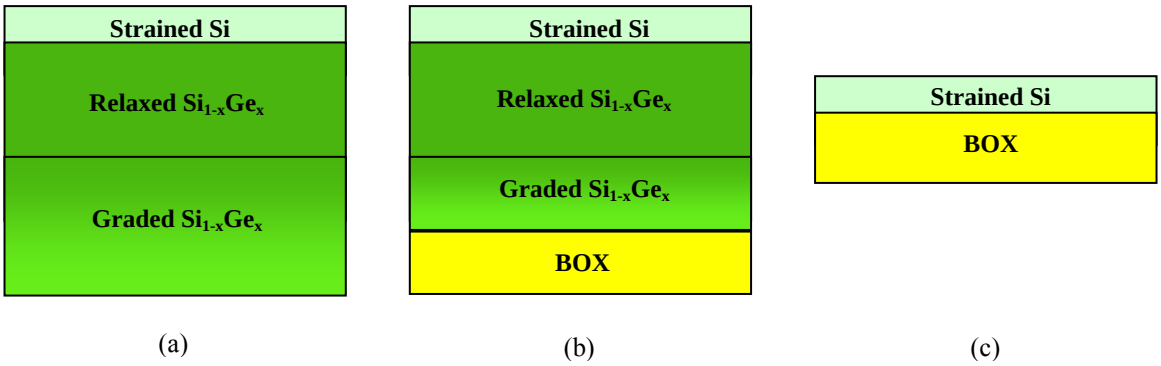


Figure 1.2 : Different types of globally strained silicon substrate wafers. (a) strained Si / relaxed SiGe (b) strained silicon / relaxed SiGe – on – insulator (SGOI) (c) strained Si directly – on – insulator (SSDOI)

The other technique to induce strain in the Si channel is the local strain technique [12] – [17]. Strain is introduced locally only at specific regions of the device (mainly channel region). The strain need not be introduced right from the start of the process flow but at intermediate steps in the CMOS process flow. Figure 1.3 shows the various different ways to locally strain the MOSFET devices. Some examples include using STI isolation to introduce compressive strain to the channel region of pMOSFETs [12], [13], silicide-induced stress [14] and nitride Etch Stop Layer (ESL) to introduce tensile strain to nMOSFETs [15], [16]. By introducing material with a different lattice constant (e.g. SiGe) from Si into the source/drain (S/D) regions of the device, strain can also be incorporated to the channel region of the device [17]. The strain introduced in various directions on the nMOSFETs and pMOSFETs and its impact on device performance has been reported by Ge *et al* [26].

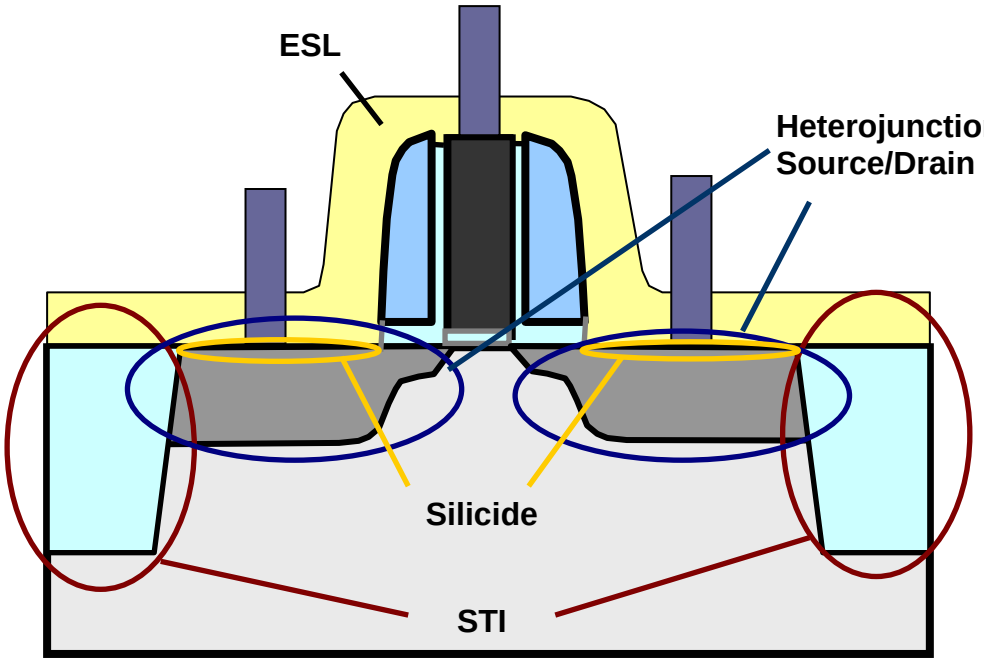
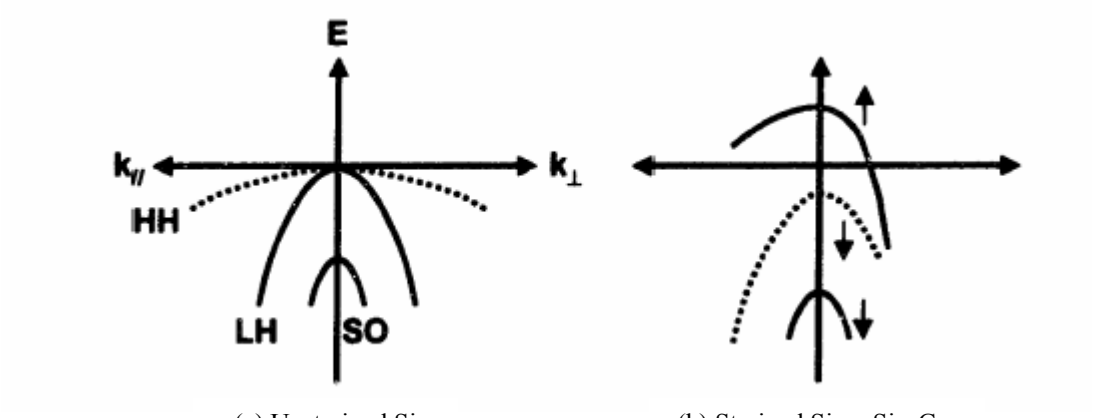


Figure 1.3 : Various techniques to introduce different type of strain to the channel region of MOS devices.

The presence of strain can affect the electronic band structure of Si, which changes the electrical properties of Si. Figure 1.4 shows the valence band structure of unstrained silicon and silicon under biaxial tensile strain. The valence band of Si is composed of the heavy hole, light hole and spin-orbit sub bands. In unstrained Si, the heavy hole and light hole subbands are degenerate at the Γ point, while the spin-orbit sub band is located only 0.44eV below these 2 subbands. As a result, holes in unstrained Si experience a higher rate of intervalley scattering, which is the primary limitation on hole mobility in bulk Si. When Si is subjected to a biaxial tensile strain, the energy of the heavy hole and spin-orbit sub bands is lowered relative to the light hole subband, leading to reduced intervalley scattering. Tensile strain also modifies the shape of the valence sub bands, lowering the in-plane and out-of-plane effective mass of holes. Alternatively, uniaxial compressive strain in the lateral or source-to-drain direction of the transistor can also improve hole mobility as described in [27].



(a) Unstrained Si (b) Strained Si on $Si_{1-x}Ge_x$

Figure 1.4 : Valence band structure of (a) unstrained Si and (b) tensile strained Si on $Si_{1-x}Ge_x$. Tensile strain lowers the energy of the heavy hole and spin-orbit subbands relative to the light hole sub band and modifies the shape of the sub bands [28].

On the other hand, the effect of tensile strain on the electronic conduction band structure can be illustrated as shown in Figure 1.5, which shows the six-fold degenerate conduction band of an unstrained Si at Δ valley along the [100] direction of the Brillouin zone with equal electron population in each valley. The constant energy surface is ellipsoidal with the longitudinal effective mass, m_l=0.916m_o, and transverse effective mass, m_t=0.19m_o, with free electron mass denoted by m_o. When biaxial tensile strain is induced, the six-fold degeneracy at conduction band minima is lifted by lowering the two- fold perpendicular valleys (Δ_2) with respect to the four-fold in-plane valleys (Δ_4) as described in Figure 1.4(b). Hence electron population preferentially occupies the lower energy Δ_2 valley where the effective in-plane transport mass is significantly reduced due to the lower transverse mass m_t in parallel to the Si/SiO_2 interface. The strain-induced band splitting between subband energies in the Δ_2 and Δ_4 valleys (Figure 1.6) has also been reported to suppress inter-valley phonon scattering and lead to the enhanced electron mobility. Like in the case of biaxial tensile strain, uniaxial tensile strain, induced along the lateral or

source-to-drain direction of the transistor have a similar effect on the conduction band and electrical properties of Si [27].

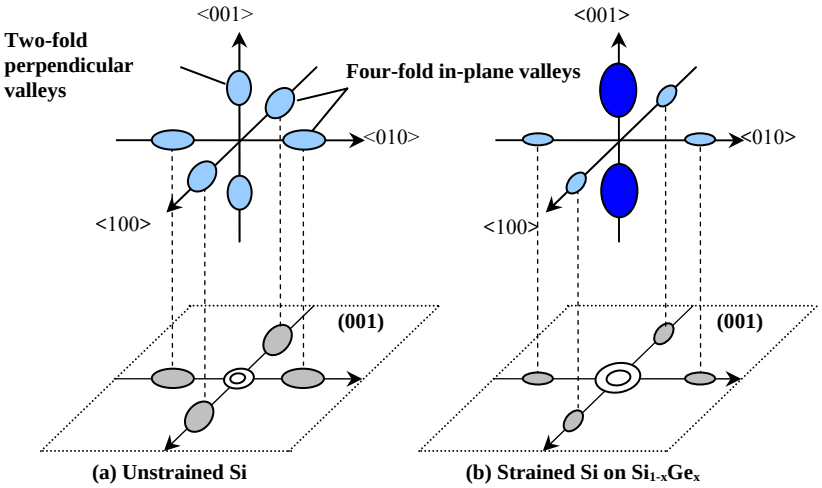


Figure 1.5 : Schematic representation of the constant energy ellipses for (a) unstrained Si and (b) tensile strained Si [10].

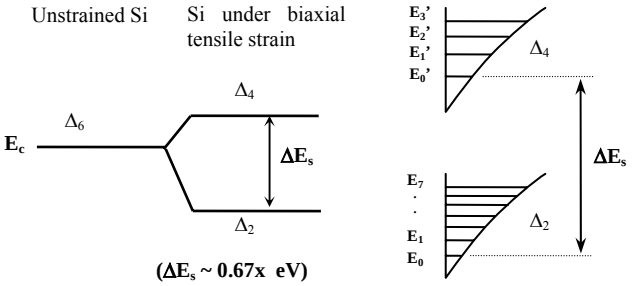


Figure 1.6 : Conduction band splitting and sub-band energies lineups of Si under biaxial tensile strain [10].

1.2.3 Silicon-On-Insulator (SOI) for reduced parasitic capacitance C

One of the main advantages of using SOI substrate is the reduction in parasitic capacitance *C* to improve circuitry speed. The source/drain (S/D) junctions of SOI MOSFETs usually touch or are very close to the underlying buried oxide (BOX). This effectively reduces the surface area of the junction, contributing to an overall reduction in junction capacitance. Other advantages of using SOI substrates include prevention of latch-up, improved short channel effects, radiation hardness and lower leakage currents.

In summary, CMOS performance can be enhanced by implementation of new device structures and materials. Channel strain engineering is one promising method to improve the drive current *I* of MOSFET devices. At present, there are many different techniques to introduce different type of strain in various directions in the transistor channel. On the other hand, parasitic capacitance *C* can be reduced significantly by the implementation of MOSFET devices on SOI substrates.

1.3 Objectives of the research

The main objective of this thesis is to explore various ways to enhance the performance of CMOS device, and ultimately resulting in an improvement in speed performance of integrated circuits. This can be achieved by reducing the parasitic capacitance *C* of the transistor or increasing the transistor drive current *I*. Lower cost alternatives to SOI substrates will be explored for reduction in parasitic capacitance *C*. In

addition, focus will also be given to the various methods of inducing strain in the channel of MOSFET devices for enhanced device performance.

1.4 Outline of the report

Chapter 1 includes a brief discussion of the recent technology to improve the performance of the MOSFET devices. For eventual improvement in device performance at the circuitry level, the drive current *I* could be increased or parasitic capacitance *C* reduced. Strained engineering has been identified as one promising method to improve drive current *I* while the use of SOI substrates also helps to reduce parasitic capacitance *C*. In chapter 2, a low cost alternative to SOI substrates for reduction in parasitic capacitance is explored. Electrical characterization of fabricated devices is performed at the transistor as well as the circuit level. TCAD simulation is also being done concurrently for optimization of the devices and projection of its feasibility for future technology nodes. Chapters 3, 4, 5 and 6 discuss the various methods of inducing and characterizing strain components in the Si channel. Characteristics and challenges of globally strained Si devices will be discussed in chapter 3, while chapter 4 describes some of the methods in characterizing and predicting strain components in strained Si MOSFET structures. Chapter 5 and 6 elaborates on locally strained n and pMOSFETs using lattice mismatched source/drain (S/D) stressors. The last chapter summarizes the results and discussions in earlier chapters before finally proposing possible future work.

CHAPTER 2

Source Drain On DEpletion Layer (SDODEL) for Reduced Junction Capacitance

2.1 Background

Reduction in transistor parasitic capacitances allows circuits to operate at higher speeds or at lower power for a given speed. Silicon-On-Insulator (SOI) technology is able to achieve significant improvement in circuit performance by greatly reducing the source and drain junction (S/D) capacitance, but issues such as history effect, self-heating effect, and high wafer cost bring challenges for its widespread adoption. A pseudo-SOI technology was recently demonstrated [29], [30] on bulk substrate to realize reduced junction capacitances without the disadvantages associated with partially-depleted SOI. The pseudo-SOI technology employs a silicon-on-depletion layer (SODEL) transistor (Figure 2.1) in which a depletion layer due to an internal built-in potential is established beneath the channel, source, and drain regions of a bulk transistor, leading to reduced junction capacitance. However, the significantly increased depletion volume may lead to increased cross-talk and generation current, and the depletion region beneath the channel region may result in higher source-to-drain leakage in nanoscale devices. To suppress short-channel effects, an epitaxial silicon layer is employed to form a thin channel layer over the depletion layer [29], but this increases process complexity and incurs additional cost.

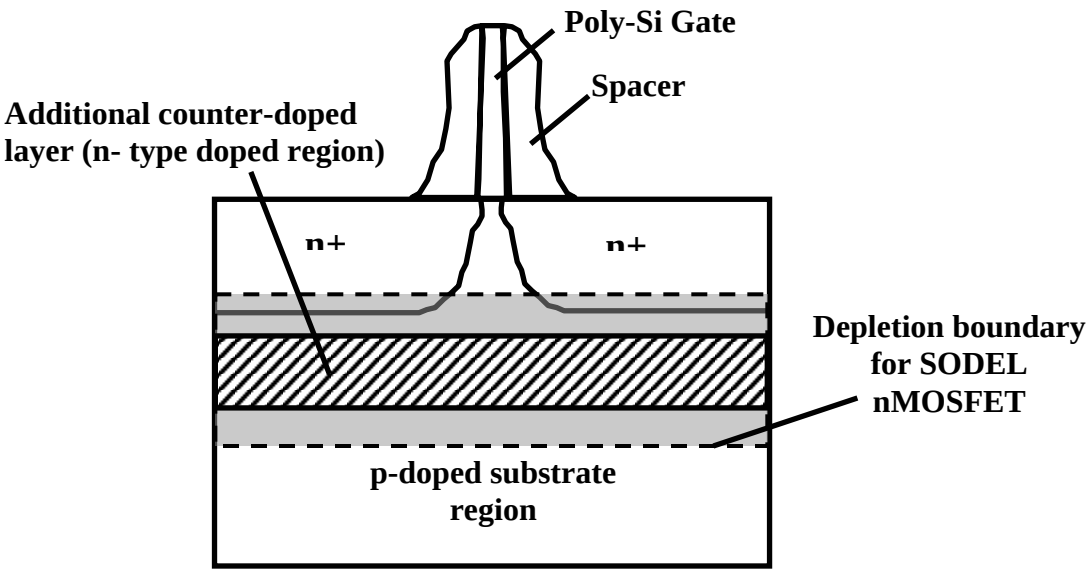


Figure.2.1 : Schematic illustration of Silicon On DEpletion Layer (SODEL) nMOSFET. The counter-doped layer (shaded) is of the same doping type as the source/drain regions. As a result of the counter-doped layer, an enlarged depletion region as indicated by the gray region and bounded by dashes is achieved. SODEL pMOSFET has the same structure but of opposite dopant-type.

In this work, an alternative structure which employs a simple and low-cost fabrication process [31] is proposed. An additional high energy, low dose implant of the same conductivity type as the S/D is introduced at the deep S/D or S/D extension implant step. This forms a counter-doped region beneath and separated from the S/D regions. This counter-doped region is fully depleted at zero gate bias, contributing to an increased depletion width and a significantly reduced junction capacitance. The resulting transistor structure is called a Source/Drain-on-Depletion (SDODEL) transistor (Figure 2.2).

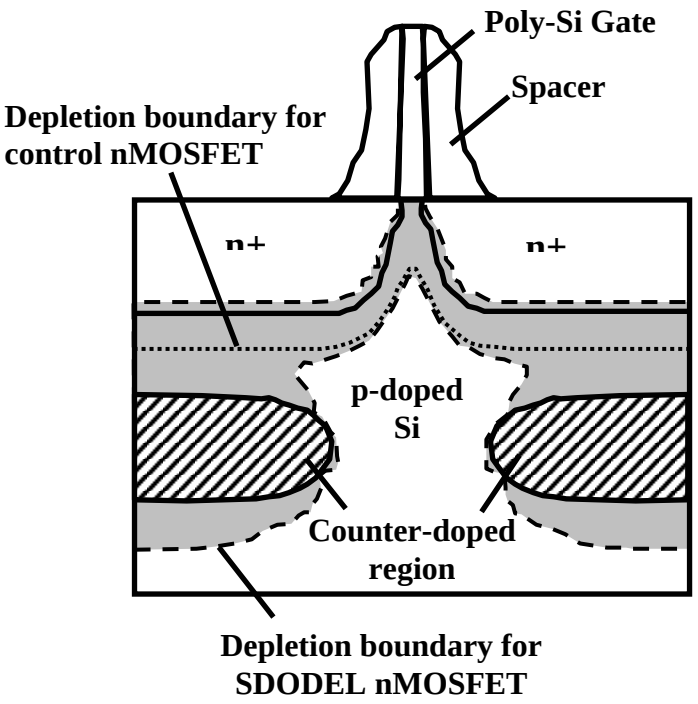


Figure 2.2 : Schematic of a simulated Source/Drain on Depletion Layer (SDODEL) nMOSFET transistor structure showing counter-doped regions (shaded) beneath the source/drain regions. The counter-doped regions are of the same doping type as the source/drain regions. As a result of the counter-doped regions, the depletion region as indicated by the gray region and bounded by dashes is significantly enlarged over that of the control transistor. The original boundary of the depletion region in the control transistor is indicated by dotted lines. SDODEL pMOSFET has the same structure but of opposite dopant- type.

2.2 Simulation Results

2.2.1 Reduction in Junction Capacitances (Simulation)

To demonstrate and compare the junction capacitance reduction in SDODEL [31] and SODEL (Inaba *et al* [29]) devices, SYNOPSYS process and device simulators [32], [33] are used to simulate 3 device structures (SDODEL, SODEL and control). This simulation work is carried out using simulation decks that have been previously calibrated based on 90nm technology node. For both SDODEL and SODEL nMOSFETs, phosphorus (P) implant is introduced at different stages of the process flow

to form the depletion regions and depletion layer respectively. In the case of the SDODEL nMOSFET, the additional P implant is introduced at the S/D implant step whereas in the case of the SODEL nMOSFETs, a blanket P implant is added at the beginning of the process flow to form the depletion layer. The simulated structure for both devices is given in Figure.2.3 and Figure.2.4. The gate length of the simulated devices is 65nm. For fair comparison, the V_t adjust implant step in the process simulation has been tuned to obtain comparable linear threshold voltage, V_{tlin}, I_{Dsat} and I_{off} in all 3 types of devices. Electrical data were obtained by performing device simulation on the process simulated device structures. A comparison of the junction capacitance, breakdown voltage, V_{bd}, V_{tlin}, I_{off} and I_{dsat} of all the 3 different devices are as summarized in Table.2.1.

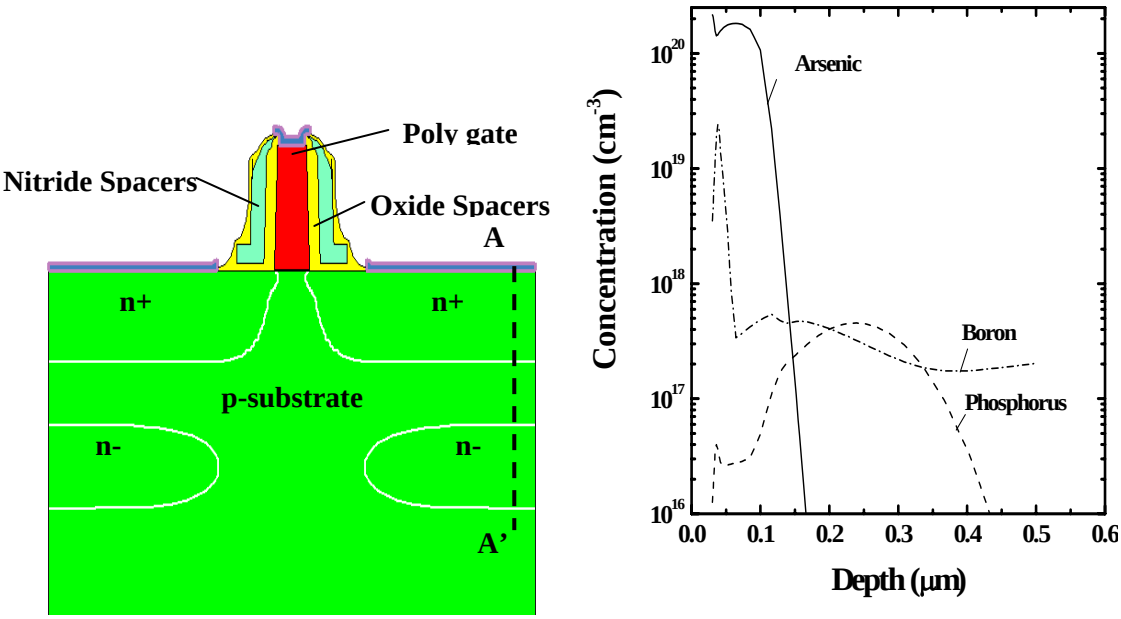


Figure.2.3 : (a) Simulated SDODEL nMOSFET device with a gate length of 65nm and (b) Concentration profile of dopants along a vertical line A-A' as depicted in (a).

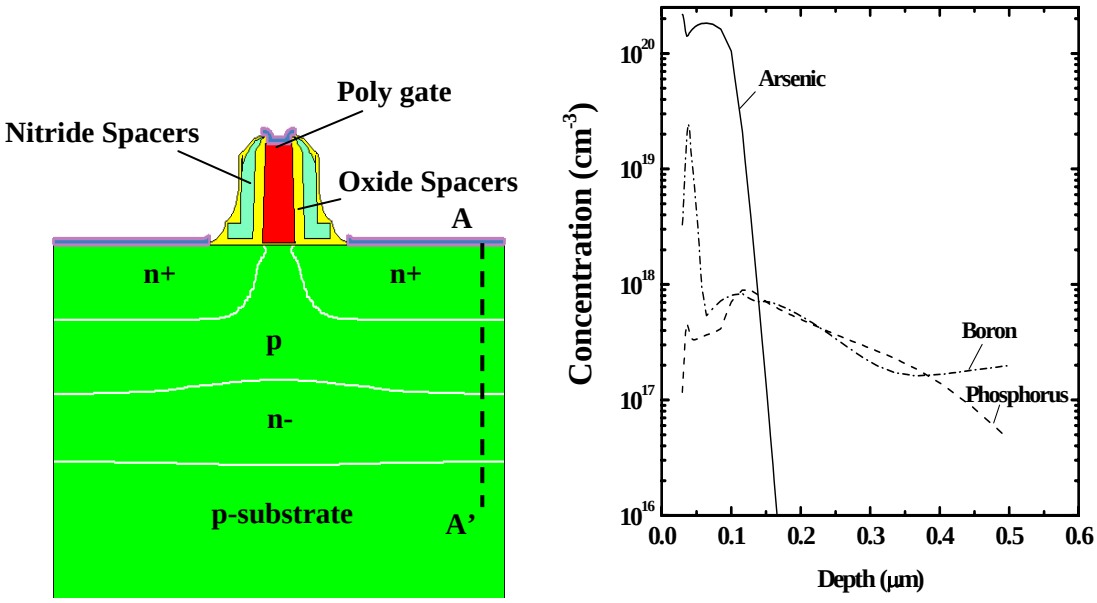


Figure.2.4 : (a) Simulated SODEL nMOSFET device with a gate length of 65nm and (b) Concentration profile of dopants along a vertical line A-A' as depicted in (a).

	Using Phosphorus		(Control)
	SDODEL	SODEL	Conventional Si
	(Before S/D implant)		
Energy (keV)	155	60	~
Dose (atoms/cm^2)	8.70E+12	3.50E+13	~
Channel Implant	B(2.1e13, 15keV)	B(2.75e13, 15keV)	~
C_j @ 0V (F/cm^2)	6.54E-08	1.20E-07	2.00E-07
C_j @ 1.2V (F/cm^2)	3.60E-08	3.36E-08	1.32E-07
I_{off} (nA/μm)	30.5	35	26.4
V_{tlin} (V)	0.2	0.2	0.2
I_{dsat} (μA/μm)	1165	1162	1179
Breakdown Voltage (V_{bd})	3	2.6	3.2
(@1μA/μm)			

Table.2.1 : Comparison of electrical parameters of SDODEL, SODEL and control nMOSFET structures. At comparable V_{tlin}, I_{dsat} and I_{off}, reduction in junction capacitance can be observed in both the SDODEL and SODEL nMOSFETs. SODEL nMOSFETs are also noted to have a smaller V_{bd}

As shown in Table 2.1, both SDODEL and SODEL nMOSFETs can achieve about a 70% reduction in junction capacitance C_j compared to the control nMOSFETs. However, between the two, SODEL nMOSFETs suffer from a much lower breakdown voltage V_{bd}. In the case of our proposed SDODEL nMOSFETs, the simulated breakdown voltage V_{bd} is higher and close to that of the control nMOSFETs.

Next, the same simulation procedures have been carried out to simulate the pMOSFET structures. However, a different dopant (Boron) implant is added this time to form the depletion regions and the depletion layer in the SDODEL and SODEL pMOSFETs respectively. The simulated structures for both pMOSFETs are as given in Figure.2.5 and Figure.2.6. The gate length of all the simulated devices is 65nm. Similarly, the V_t adjust implant is tuned to obtain comparable V_{tlin}, I_{dsat} and I_{off} in all the SDODEL, SODEL and control pMOSFET devices. A comparison of the electrical parameters of the 3 types of devices are tabulated in Table.2.2.

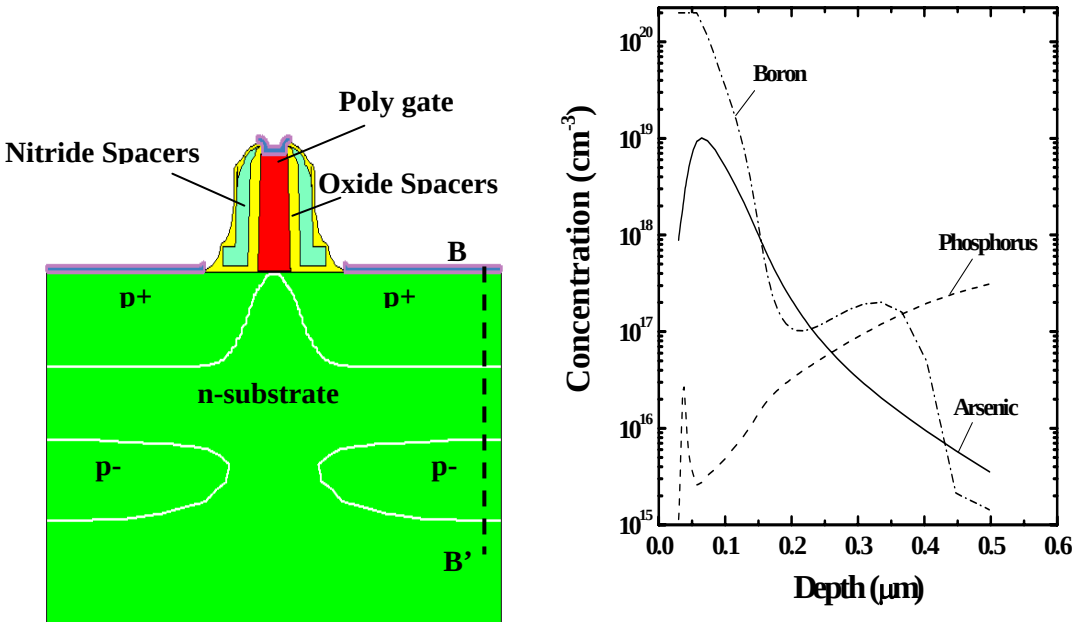


Figure.2.5 : (a) Simulated SDODEL pMOSFET device with a gate length of 65nm and (b) Concentration profile of dopants along a vertical line B-B' as depicted in (a).

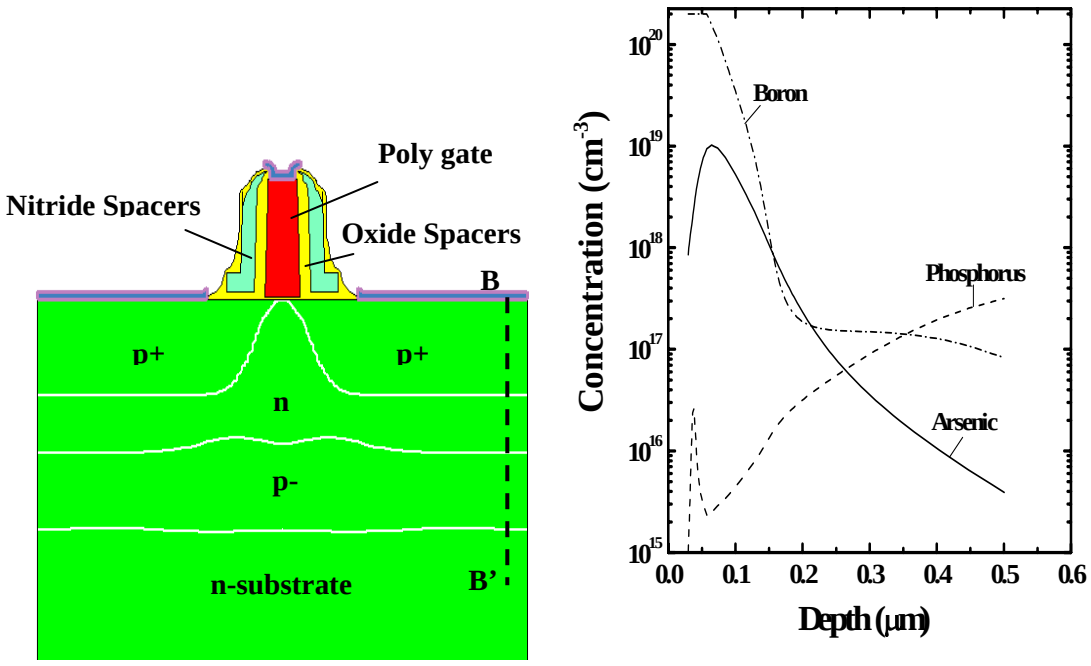


Figure.2.6 : (a) Simulated SODEL pMOSFET device with a gate length of 65nm and (b) Concentration profile of dopants along a vertical line B-B' as depicted in (a).

	Using B		(Control)
	SDODEL	SODEL	Conventional Si
	(After S/D implant)		
Energy (keV)	90	70	~
Dose (atoms/cm^2)	3.20E+12	9.80E+12	~
Channel Implant	As (7.5e12, 130)	As (9.2e12, 130)	~
C_j @ 0V (F/cm^2)	7.78E-08	8.12E-08	2.54E-07
C_j @ 1.2V (F/cm^2)	7.50E-08	7.30E-08	1.44E-07
I_{off} (nA/μm)	-6.8	-7.85	-6.8
V_{tlin} (V)	-0.3	-0.3	-0.3
I_{dsat} (μA/μm)	-305	-309	-305
Breakdown Voltage (V_{bd})	-4.4	-4.15	-4.45
(@1μA/μm)			

Table.2.2 : Comparison of electrical parameters of SDODEL, SODEL and control pMOSFET structures. At comparable V_{tlin}, I_{dsat} and I_{off}, reduction in junction capacitance can be observed in both the SDODEL and SODEL pMOSFETs. SODEL pMOSFETs are also noted to have a smaller V_{bd}

At the same V_{tlin}, I_{dsat} and I_{off}, the junction capacitance of both SDODEL and SODEL pMOSFET devices are 50% lower than that of the control pMOSFETs. However, like in the case of the nMOSFETs, the V_{bd} of SODEL pMOSFET devices are also found to be lower in magnitude than that in the SDODEL and control pMOSFETs.

2.3 Experimental Results

A standard CMOS fabrication process based on 0.18μm technology node was used in this experiment. SDODEL and control devices of various gate lengths ranging from 0.16 μm to 20 μm are fabricated. After forming the poly-silicon (poly-Si) gate electrode and spacers, an additional high energy and low dose implant of about $1x10^{13}$ cm^{-2} was separately introduced for the n and pMOSFET transistors. The additional implant formed doped regions beneath the S/D regions that are separated from each other. The implant employed phosphorus dopants for nMOSFETs, and boron dopants for pMOSFETs. The vertical concentration profile of the dopants through the source or the drain region is shown in Figure 2.7 and Figure 2.8 for the SDODEL n and pMOSFETs respectively, depicting a counter-doped region beneath the source or drain regions formed by the additional implant. Subsequent fabrication process follows the conventional CMOS process and no effort was made to optimize the transistor performance. Cobalt silicide and two metallization layers were used. Control devices were fabricated using a CMOS process without the additional implant step. Ring oscillator circuits were also realized for comparison of circuit performance.

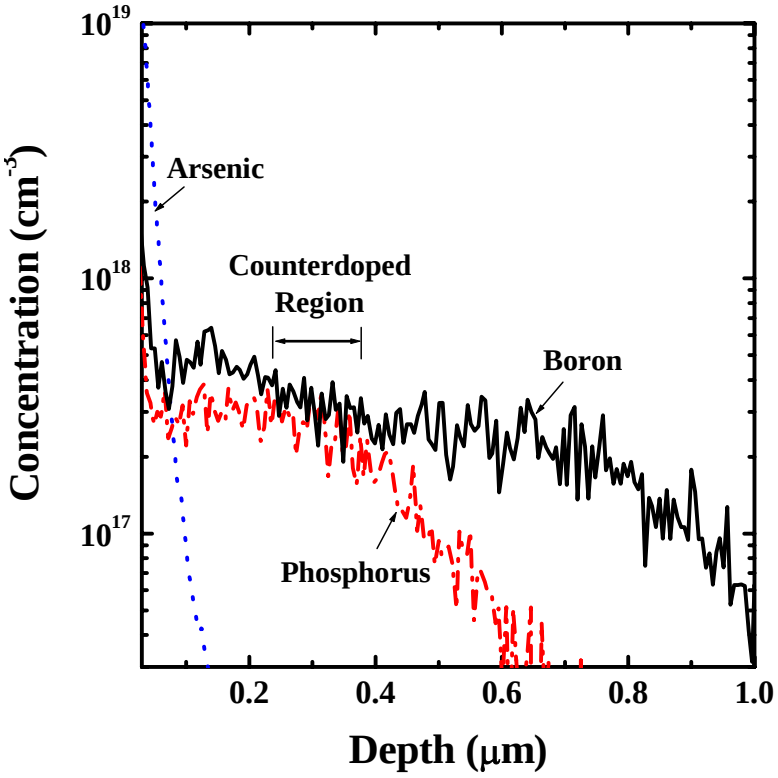


Figure 2.7 : Measured SIMS results for n-channel SDODEL at S/D regions.

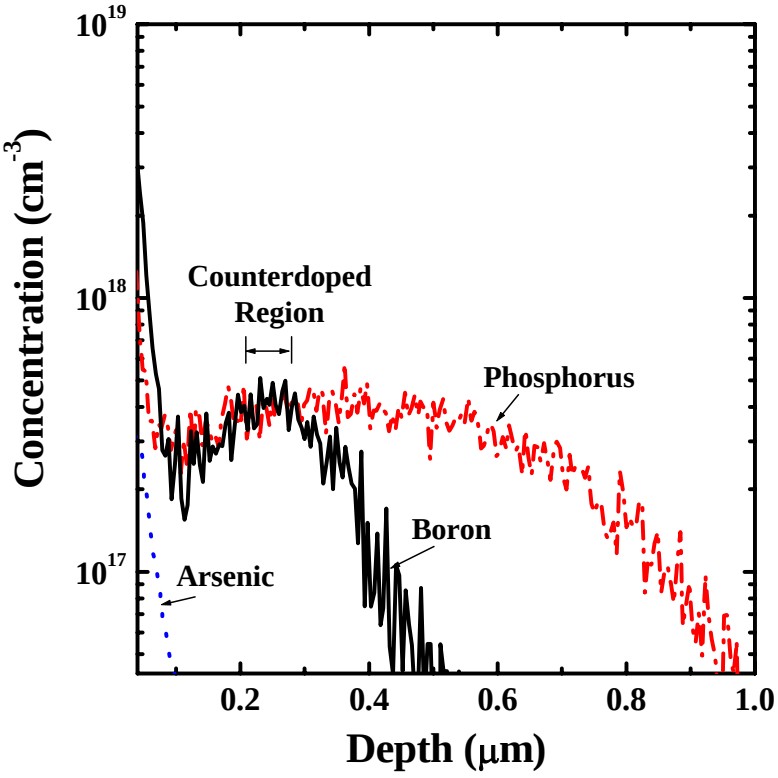


Figure 2.8 : Measured SIMS results for p-channel SDODEL at S/D regions.

2.3.1 Reduction in Junction Capacitance (Experimental Measurements)

The measured junction capacitance C_j of the SDODEL n and pMOSFET devices as a function of drain-body bias V_{db} is shown in Figure 2.9 (a) and (b). In comparison with control devices, C_j (at a bias voltage equal to the supply voltage V_{dd}) has been reduced by more than 40% and 70% for the SDODEL n and pMOSFETs respectively. Junction capacitance measurements for a sample size of 5 devices of each type have been performed and depicted by the box plot in Figure 2.10.

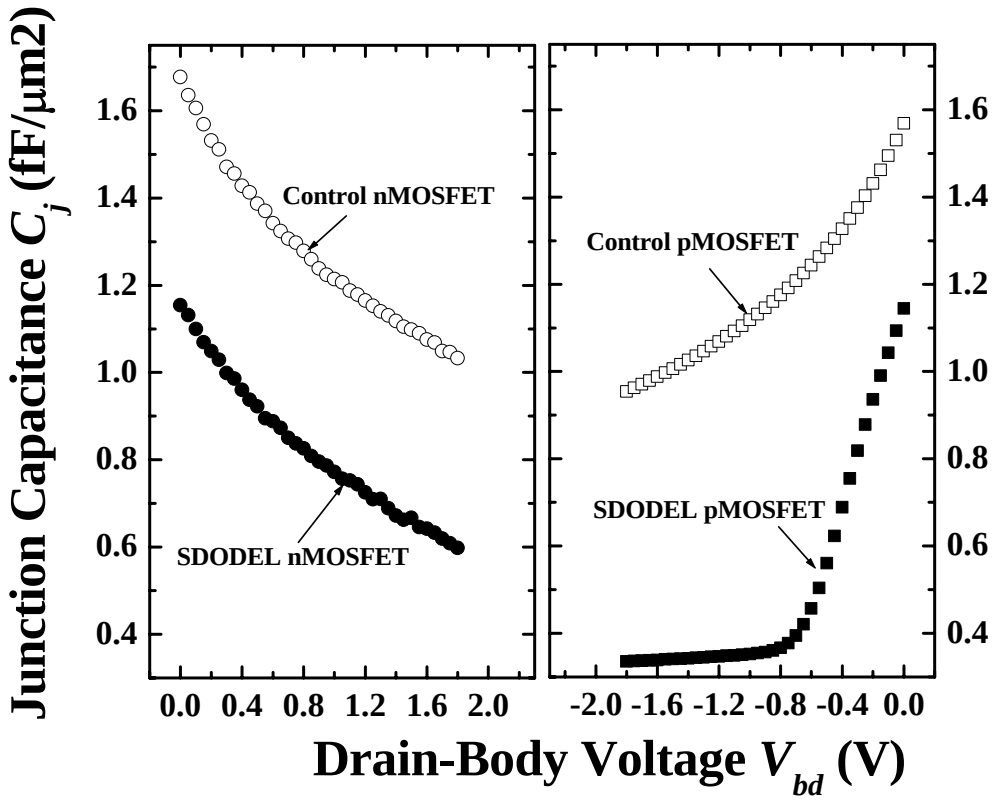


Figure 2.9 : Measured junction capacitance C_j as a function of drain-body bias V_{db} for SDODEL and control (a) nMOSFETs and (b) pMOSFETs, showing significant reduction of C_j for the SDODEL device.

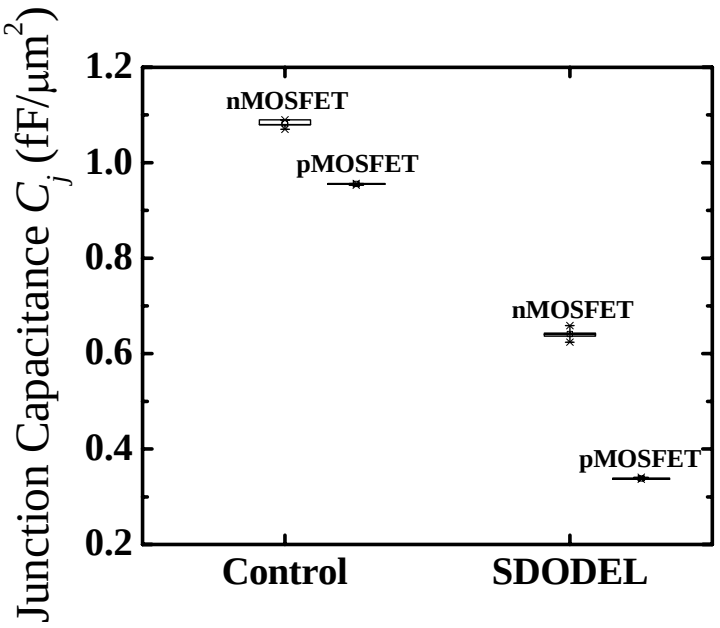


Figure.2.10 : Box plot showing a comparison of junction capacitance between SDODEL and control n and pMOSFET devices.

2.3.2 Sub-threshold Characteristics

Fig. 2.11 plots the sub-threshold characteristics of a SDODEL and a control nMOSFET device. The sub-threshold slope and DIBL of the SDODEL nMOSFET is observed to be comparable to that of the control nMOSFET. A slight decrease in threshold voltage V_{tlin} of about 20 mV for the SDODEL nMOSFETs is observed in measurements, accounting for a slight increase in the off-state leakage current I_{off}. This decrease might be attributed to a slight reduction in the average doping concentration below the channel region due to lateral diffusion of counter-doping implant. The reduction in V_{tlin} and increase in I_{off} can be compensated for and optimized by adjusting the channel implant. In the following section, it can be shown through simulation that with optimization, V_{tlin} and I_{off} can be restored without any degradation in drive current.

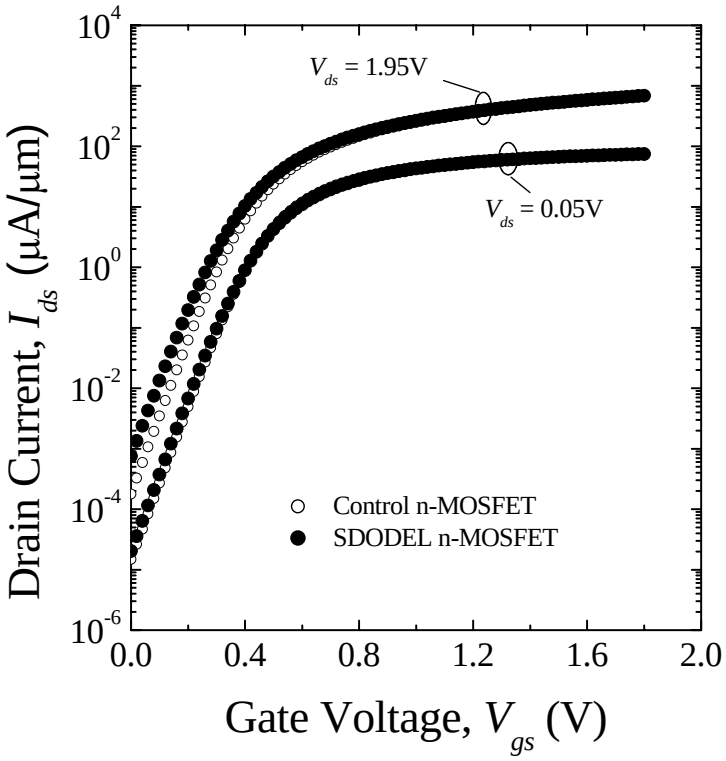


Figure.2.11 : Sub-threshold characteristics for SDODEL and control nMOSFETs, at V_{ds} = 0.05V and 1.95V.

2.3.3 Verification of restoration of V_{tlin} through simulation

In the previous section, the fabricated SDODEL nMOSFET device shows a slightly lower V_{tlin} and higher I_{off} than the control possibly due to a slight reduction in the average doping concentration below the channel region. This section serves to verify via simulation that by changing the V_t adjust implant, the V_{tlin} and I_{off} can be restored. Using a simulation deck that has been calibrated based on the same 0.18μm process technology used in section 2.3.2, the V_t adjust implant condition for the SDODEL device is optimized. Table 2.3 shows the summarized results after optimization of the channel implant dose. It can be clearly shown from simulation that by adjusting the V_{tlin} of the SDODEL devices to

match that of control devices, I_{off} can be greatly reduced while still maintaining the same I_{dsat}.

	SDODEL nMOSFET		Control nMOSFET	
	Simulation	**Measured**	**Simulation**	**Measured**
V_t implant dose	1.1 x nVT	nVT	nVT	nVT
I_{off} (pA/μm)	90	529	74	247
V_{tlin} (V)	0.4	0.38	0.4	0.4
Sub-threshold Slope (mV/decade)	75.8	76.0	78.7	79.0
I_{dsat} (μA/μm)	605	694	595	696
C_j at 0V (pF)	2.495	7.62	9.0	11
C_j at 1.8V (pF)	1.64	3.94	5.45	6.82

Table 2.3: By adjustment of V_t implant dose and energy, the V_{tlin} and I_{off} can be matched to that of the control device without degrading the I_{dsat} and junction capacitance

2.3.4 Circuit Speed Measurement

The impact of the reduced junction capacitance on ring oscillator speed is then investigated by measuring the average gate delay of an inverter in a 127-stage inverter ring oscillator. Fig. 2.12 shows the gate delay of an inverter stage plotted against the sum of the reciprocal of the drive currents of the n and pMOSFETs. A linear fit of the data for both types of devices (lines in Fig.2.12) shows an almost parallel shift of about 3 ps, attributed to the reduction in junction capacitance in SDODEL devices. For an inverter

comprising SDODEL n and pMOSFETs, the gate delay t_d is reduced by about 15% in comparison to a control inverter at the same $1/|I_{dsat,n}| + 1/|I_{dsat,p}|$.

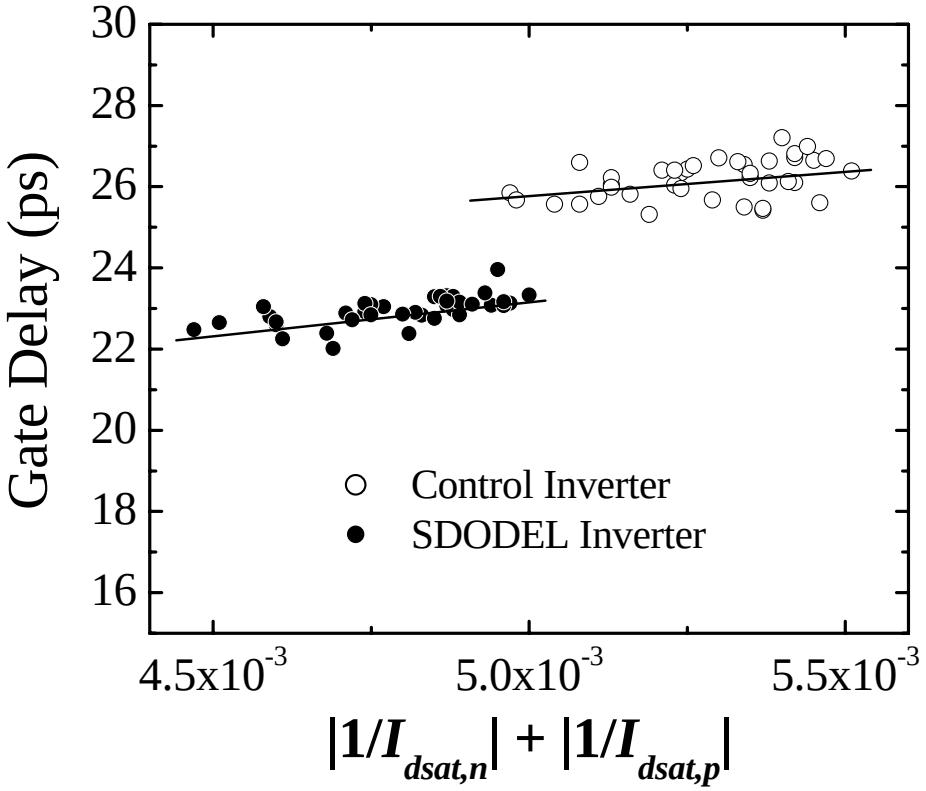


Figure 2.12 : Gate delay of an inverter stage plotted against the sum of reciprocals of the drive currents of the n and pMOSFETs. The gate length is 0.18 μm. The device widths are 10 μm and 20 μm for the nand pMOSFETs, respectively. Experimental data is obtained from ring oscillators from different dies. Reduction of the inverter gate delay is as high as 15% at the same ($|I_{dsat,n}^{-1}| + |I_{dsat,p}^{-1}|$) at V_{dd} = 1.8 V.

2.3.5 Breakdown Voltage

Next, the measured breakdown voltage, V_{bd}, of the fabricated SDODEL devices is compared with that of the control. Conventionally, V_{bd} is measured as the drain bias V_d at which the I_d reaches 0.1μA x device width, with both V_g and V_s set at 0V.

From measurements, the V_{bd} shows a similar trend as that observed in simulation (section 2.2). The measured breakdown voltage V_{bd} of SDODEL nMOSFETs is very close to control nMOSFETs. On the other hand, SDODEL pMOSFET devices have lower breakdown voltages at gate lengths of 0.18μm and 0.16μm. However, it should be noted that these values are still within manufacturing's specifications of more than 2.5 times of V_{dd}. Table 2.4 shows the breakdown voltages for both SDODEL and control n and pMOSFETs. These highlight an added advantage of SDODEL devices over SODEL-like devices as simulated SODEL-like devices have lower source-to-drain breakdown voltage, V_{bd}.

nMOSFET			**pMOSFET**		
Physical Gate Length L_G (μm)	**SDODEL V_{bd} (V)**	**Control V_{bd} (V)**	**Physical Gate Length L_G (μm)**	**SDODEL V_{bd} (V)**	**Control V_{bd} (V)**
0.16	4.46	4.62	0.16	-3.50	-5.06
0.18	4.60	4.56	0.18	-4.46	-5.62
0.2	4.62	4.58	0.2	-5.58	-5.62

Table.2.4 : Comparison of measured breakdown voltages, V_{bd} for SDODEL and control MOSFETs for different channel lengths

2.3.6 Junction Leakage

Figure 2.13 compares the junction leakage between control and SDODEL diode structures. Area intensive diode structures, with an area of 6600μm^2, are measured, at a reverse bias of 1.1 x V_{dd}, over a sample size of 5 dies. The junction leakage values are comparable for both devices, implying that the introduction of the depletion layer beneath the source/drain has no negative impact on the junction leakage.

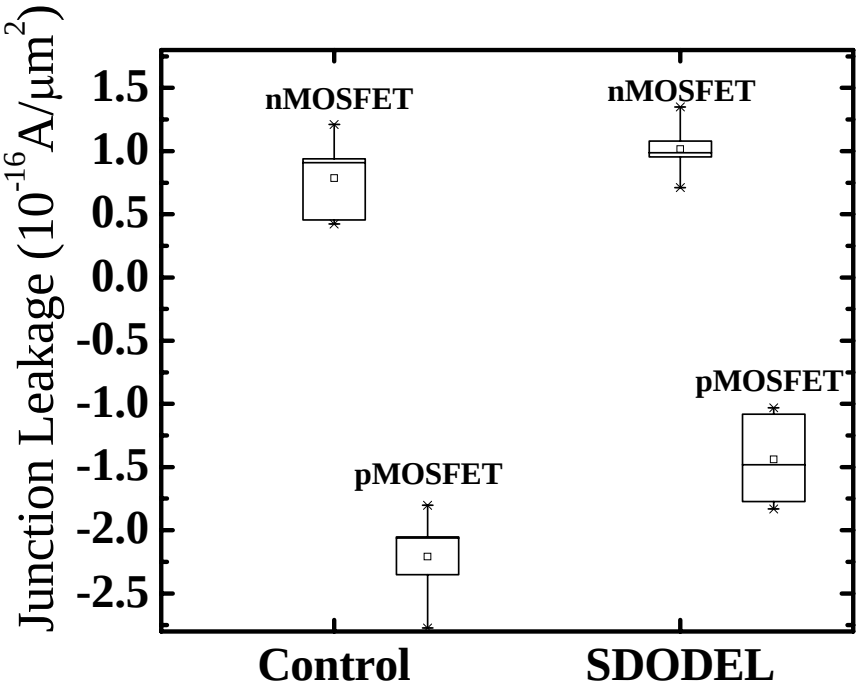


Figure 2.13 : Box plot showing a comparison of junction leakage current between SDODEL and control Si MOSFETs

2.3.7 Simulation of SDODEL devices at shorter gate lengths

Finally, to explore the feasibility of SDODEL MOSFETs at even shorter gate lengths, SDODEL nMOSFETs with gate length as small as 50 nm are simulated using the SYNOPSYS process and device simulators. V_t adjust implant are tuned to match the V_{tlin} of the SDODEL devices to that of the control devices. Both the SDODEL and control devices also have I_{off} that are adjusted close to the I_{off} requirements set by the 2003 ITRS roadmap [1]. At each gate length, the SDODEL and control devices have the same threshold voltage V_{tlin}, I_{off} and saturation drain current I_{dsat}. Fig. 2.14 shows the reduction in junction capacitance in the SDODEL MOSFETs over the control devices at different gate lengths. The junction capacitances for transistors at each gate length are compared at

a drain-body bias V_{db} equal to the supply voltage of that technology node, V_{dd}. Simulation results show a larger reduction in junction capacitance than found in experiments. This is probably due to the additional optimization performed in the simulations that was not done in device fabrication. Therefore, there is potential to achieve even better reduction in junction capacitance using optimized SDODEL transistor designs for gate lengths down to 50 nm.

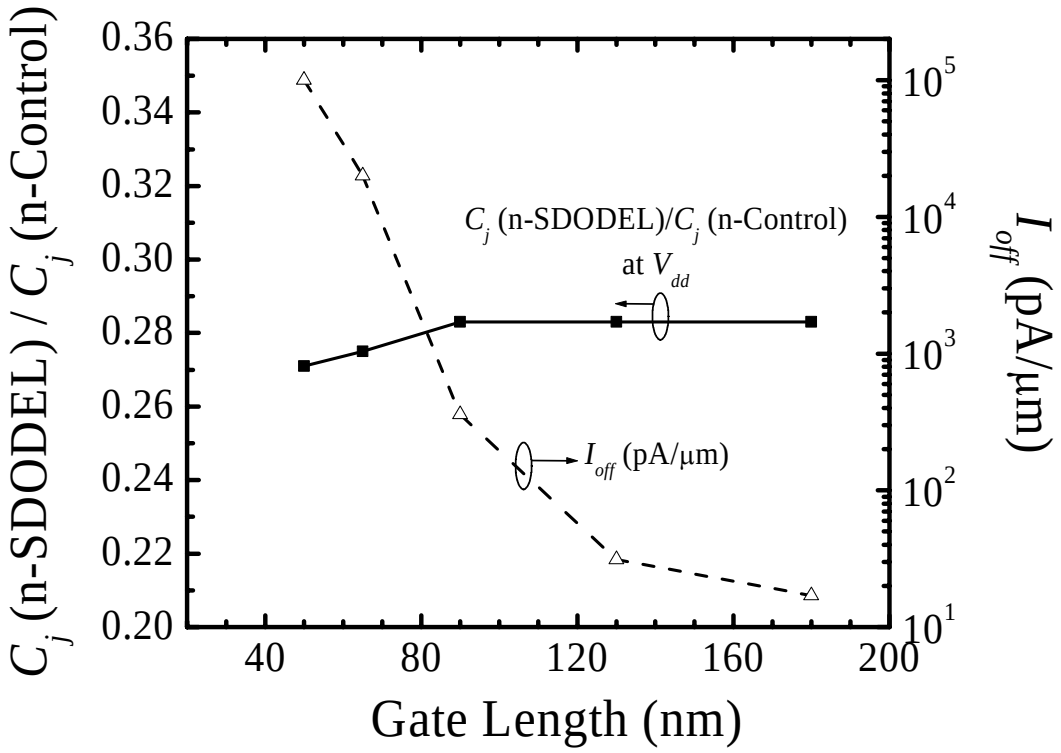


Figure 2.14 : Simulated capacitance reduction and off-state leakage current I_{off} as a function of gate length. Significant reduction in junction capacitance for SDODEL nMOSFETs can be observed for gate lengths down to 50 nm, while keeping I_{off} close to the specifications of the International Technology Roadmap for Semiconductors (ITRS) [1].

2.4 Summary

A low cost alternative to SOI in reducing source/drain junction capacitance was demonstrated using a novel SDODEL transistor structure. A simple process involving the insertion of a high energy, low dose implantation step of the source/drain doping type to a conventional CMOS process was employed to realize the SDODEL transistors. The SDODEL transistors showed significantly reduced junction capacitance, leading to a 15% reduction in inverter gate delay. A process and device simulation study shows that the improved performance in SDODEL transistors can be achieved for gate lengths down to 50 nm. Therefore, SDODEL MOSFETs potentially provide a low cost alternative for improvement in circuitry speed by reduction of parasitic capacitance *C*. In the following chapters, other alternatives to improve circuit speed (by increasing drive current *I)* will be explored

CHAPTER 3

Fabrication and Characterization of Strained Si / Relaxed SiGe CMOSFETs

3.1 Background

As discussed in Chapter 1, increasing the drive current I of transistors can reduce the time delay t_d of integrated circuits. Conventional downsizing of MOSFET has been met with immense challenges as device dimension scaled into the nano-regime. In recent years, channel strain engineering has become one promising method to improve the drive current without degradation in other electrical parameters. We can classify all the various Si channel strain-inducing approaches into 2 main categories – global or local strain approach. The global approach generally makes use of globally strained substrates where strain is already induced in the starting substrate before the start of the process flow [9] – [11].

In this chapter, strained Si on relaxed SiGe substrates, which employs 3 epitaxial layers on bulk Si, will be used (Fig. 3.1). These substrates are first formed by epitaxially growing a graded layer of $Si_{1-x}Ge_x$ layer, with Ge mole fraction x starting from zero to its final target value, on bulk Si wafers. This is followed by the growth of a relaxed $Si_{1-x}Ge_x$ buffer layer with x fixed at its final target value. These 2 layers (about 2 – 4 μm thick) help to produce a relaxed $Si_{1-x}Ge_x$ layer with reduced defects [23], [24]. The second layer

of relaxed $Si_{1-x}Ge_x$ serves as a platform for the growth of the biaxial tensile strained Si layer (third and topmost layer). According to Vegard's law, relaxed Si will have a lattice constant that is smaller than that of $Si_{1-x}Ge_x$ (Fig. 3.1 (a)). When a Si layer is epitaxially grown on the relaxed $Si_{1-x}Ge_x$ layer, the Si atoms will try to retain the in-plane lattice constant of the $Si_{1-x}Ge_x$ layer, causing the epitaxial Si layer to be in biaxial (in the *x* and *y* direction) tensile strain (Fig. 3.1 (b)). CMOSFET devices are then fabricated on such biaxial-tensile strained Si / relaxed SiGe substrates for electrical characterization.

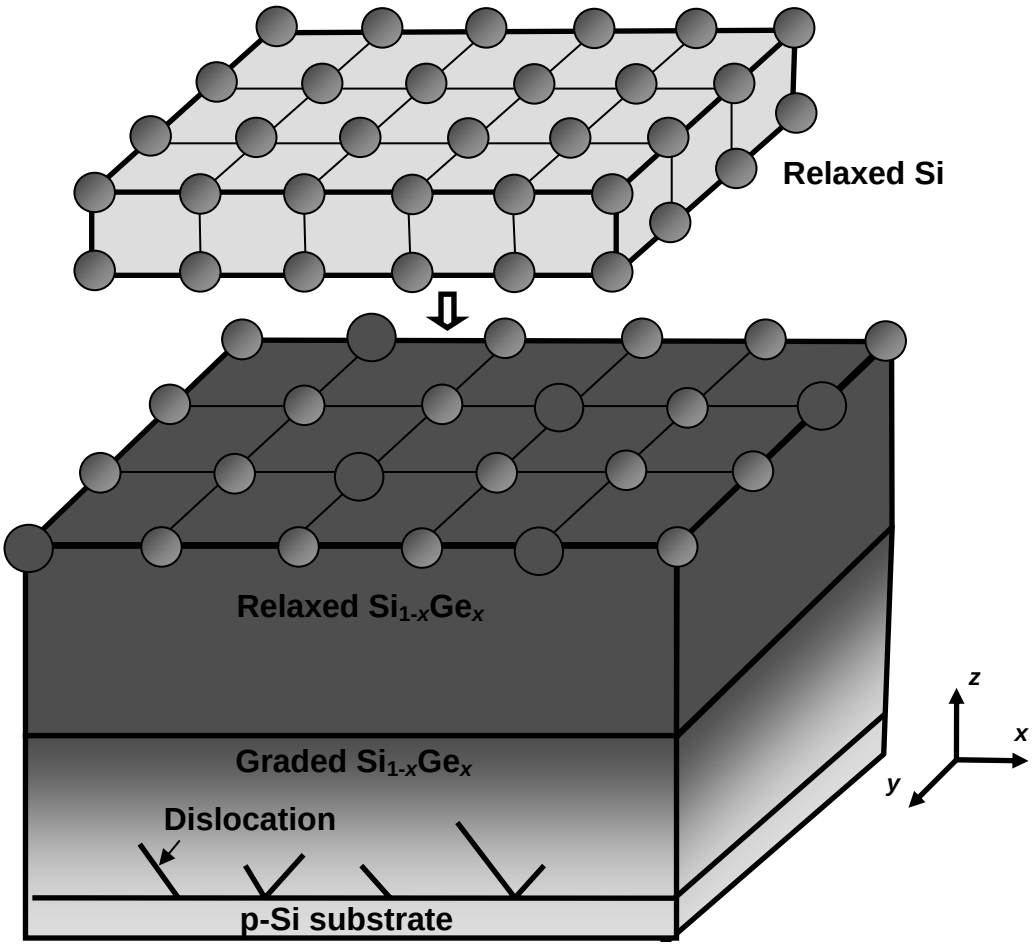


Figure 3.1 : (a) Graded $Si_{1-x}Ge_x$ and relaxed $Si_{1-x}Ge_x$ layer helps to reduce the amount of defects at the relaxed $Si_{1-x}Ge_x$ surface. Relaxed Si has a smaller lattice constant than relaxed $Si_{1-x}Ge_x$.

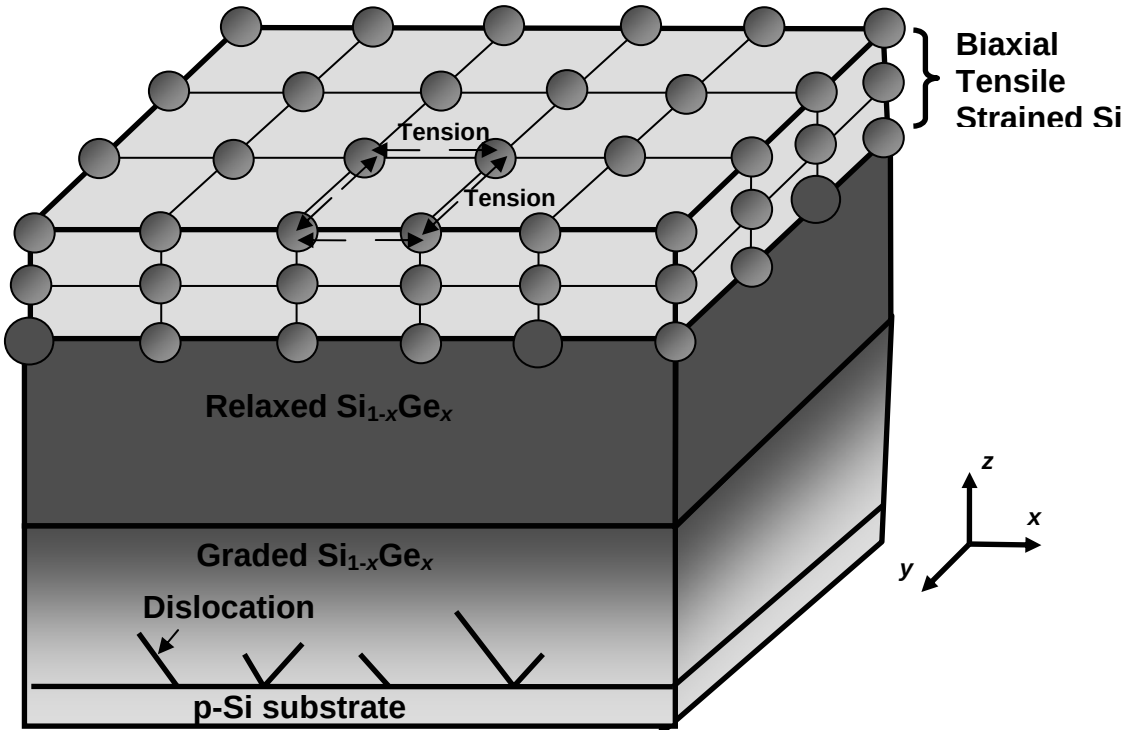


Figure 3.1 : (b) Si atoms will try to retain the in-plane lattice constant of the relaxed $Si_{1-x}Ge_x$ layer below. As a result, the Si layer becomes tensile strained in the *x* and *y* directions (biaxial).

3.2 Device Fabrication

A standard CMOS fabrication process based on 0.18 μm technology node was used in this experiment. CMOSFET devices of various gate lengths ranging from 0.16 μm to 20 μm are fabricated using strained Si / relaxed $Si_{1-x}Ge_x$ (for x = 0.15 and 0.2) substrates. A schematic of the fabricated strained MOSFET devices is shown in Fig. 3.2. Apart from minor adjustments made to the STI step to minimize the thermal budget and Si consumption of the strained Si layer, no other effort was made to change the process flow or to optimize the transistor performance. Cobalt silicide and two metallization layers were used. Control devices were fabricated using an identical CMOS process using bulk

Si substrate. Ring oscillator circuits were also realized for comparison of circuit performance.

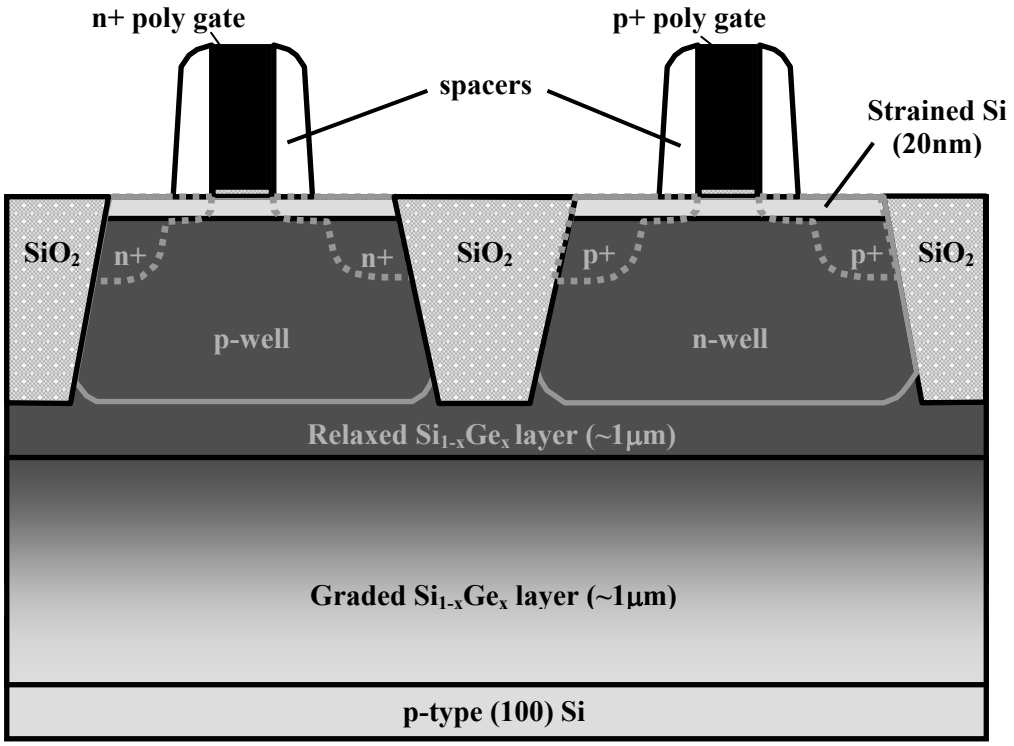


Figure 3.2 : Schematic showing cross-section of CMOSFET structures fabricated on strained Si / relaxed $Si_{1-x}Ge_x$, for x = 0.15 and 0.2. A twin-well process with STI isolation was employed.

3.3 Electrical Characterization of strained Si MOSFET devices

3.3.1 Current Drive Enhancement

The I_{DS}-V_{DS} characteristics of both strained and control n and pMOSFET devices are measured over a range of gate lengths (from 0.16 μm to 20 μm). Drain current I_{DS} enhancement can be observed in the strained Si nMOSFETs. However, no enhancement in I_{DS} is observed in the strained Si pMOSFETs for both Ge concentration splits of 15%

and 20%. Figure 3.3 and Figure 3.4 compares the I_{DS}-V_{DS} characteristics of strained and control nMOSFETs at gate lengths of 0.18 μm and 20 μm respectively. Drain current I_{DS} enhancement can be observed at both long (20 μm) and short (0.18 μm) gate lengths. As discussed previously in chapter 1, biaxial tensile strain induced in the Si channel can modify the conduction band structure of Si, resulting in the enhancement of the electron mobility. This, in turn, gives rise to an increase in I_{DS}. In addition, I_{DS} enhancement also increases with increasing Ge concentration in the relaxed SiGe layer (from 15% Ge to 20% Ge). This can be explained by the larger strain induced in the Si channel when Ge % in the underlying SiGe layer increases. As a result, higher drain current I_{DS} enhancement is observed in the nMOSFETs with relaxed $Si_{0.8}Ge_{0.2}$ layer (20% Ge) compared to that with relaxed $Si_{0.85}Ge_{0.15}$ layer (15% Ge).

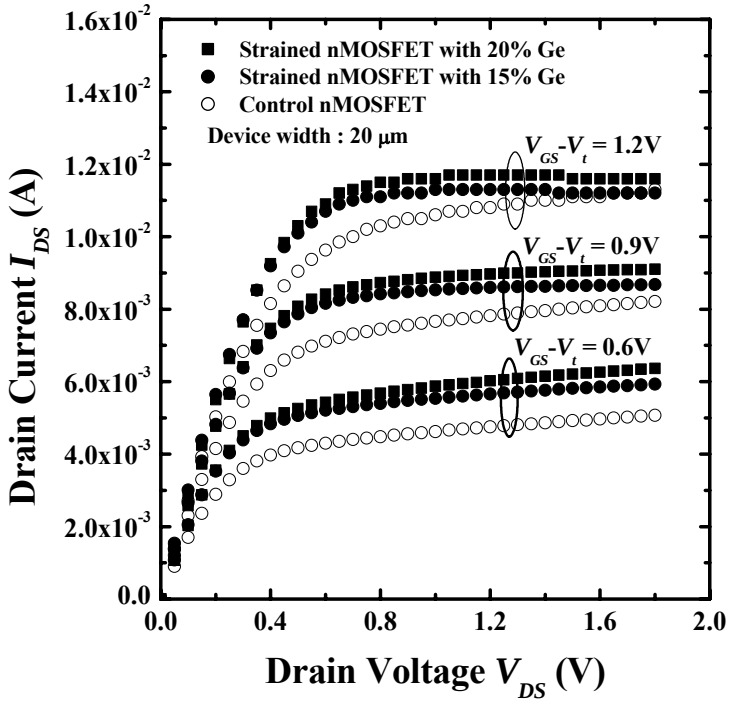


Figure 3.3 : I_{DS}-V_{DS} characteristics of 0.18 μm gate length strained and control nMOSFETs. Enhancement of about 16% and 20% in linear drain current (at a gate overdrive of 0.9V) is obtained for strained nMOSFETs with 15% Ge and 20% Ge (in the relaxed SiGe layer) respectively. I_{DS} enhancement at high V_{DS} is observed at low gate overdrive but diminishes at high gate overdrive due to self heating effects.

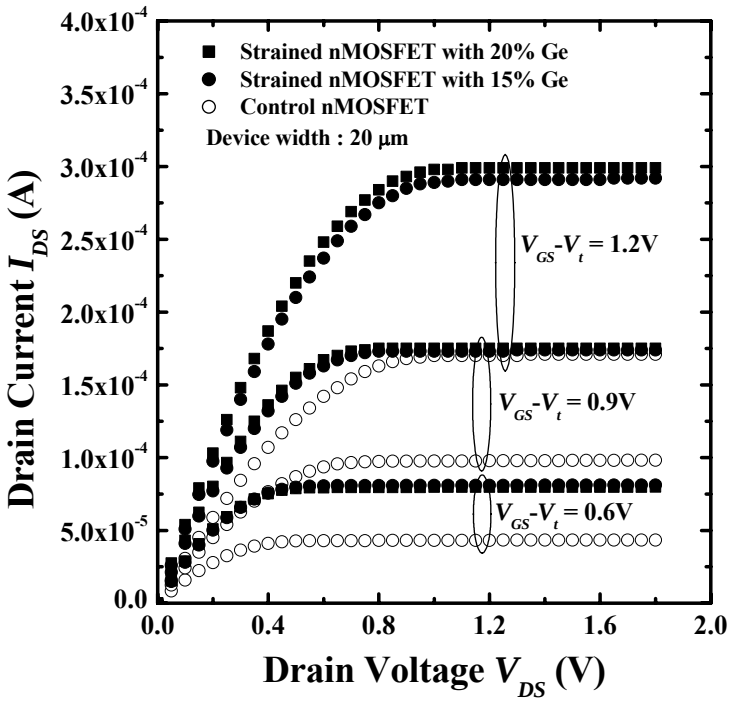


Figure 3.4 : I_{DS}-V_{DS} characteristics of 20 μm gate length strained and control nMOSFETs. Enhancement of about 65% and 75% in linear drain current (at a gate overdrive of 0.9V) is obtained for strained nMOSFETs with 15% Ge and 20% Ge (in the relaxed SiGe layer) respectively. This enhancement is much higher than that in the short channel (0.18 μm) strained devices. No degradation in I_{DS} enhancement in the saturation regime at high gate overdrive.

In addition, higher I_{DS} enhancement (about 70%) is also observed in the long channel (20 μm) nMOSFETs as compared to 10% enhancement in the short channel (0.18 μm) devices at the same gate overdrive of 0.9V. One explanation is that at high drain bias, where the lateral electric field becomes very high, there is less dependence of I_{DS} on mobility as velocity saturation dominates. Another explanation could be the self heating effect, in strained Si / relaxed SiGe substrates, which becomes more prominent as the channel length is scaled down and drain current is increased. SiGe is a poorer conductor of heat than Si, therefore it is not able to dissipate the heat generated in the channel as efficiently as Si. This leads to increased heating effect which results in larger carrier scattering in the channel. Self heating effect is especially pronounced at higher gate bias

($V_{GS} - V_t = 1.2V$) (Figure 3.3), where no drain current enhancement is observed. The V_t in this case refers to the threshold voltage extracted at maximum transconductance in the linear regime of the device at low V_{DS}.

3.3.2 Sub-threshold Characteristics

Figure 3.5 plots the I_{DS}-V_{GS} characteristics of strained Si / relaxed SiGe and control nMOSFETs at 0.18 μm gate length. At this gate length, the strained nMOSFETs show a decrease in threshold voltage V_t by about 0.15V to 0.25V. These strained nMOSFETs (solid circle and solid square symbols) also show degradation in sub-threshold slope, off-state leakage current I_{off} and DIBL. The decrease in V_t and increase in I_{off} is also observed in the long gate length (20 μm) devices but sub-threshold slope and DIBL remains comparable. The V_t roll-off characteristics of the strained and control nMOSFETs is depicted in Figure 3.6. Poorer control of short channel effects (SCE) is observed in the strained devices. In addition, V_t decreases with increasing Ge concentration in the relaxed SiGe layer (i.e. increasing strain in strained Si layer) at all the gate lengths measured.

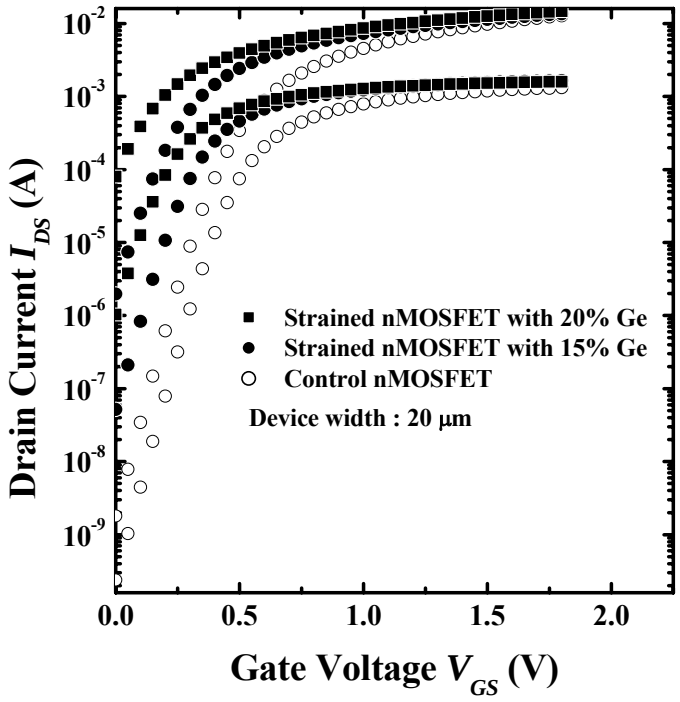


Figure 3.5 : I_{DS}-V_{DS} of strained and control nMOSFETs at a gate length of 0.18 μm. A decrease in threshold voltage V_t along with degradation in sub-threshold characteristics is observed in the strained devices.

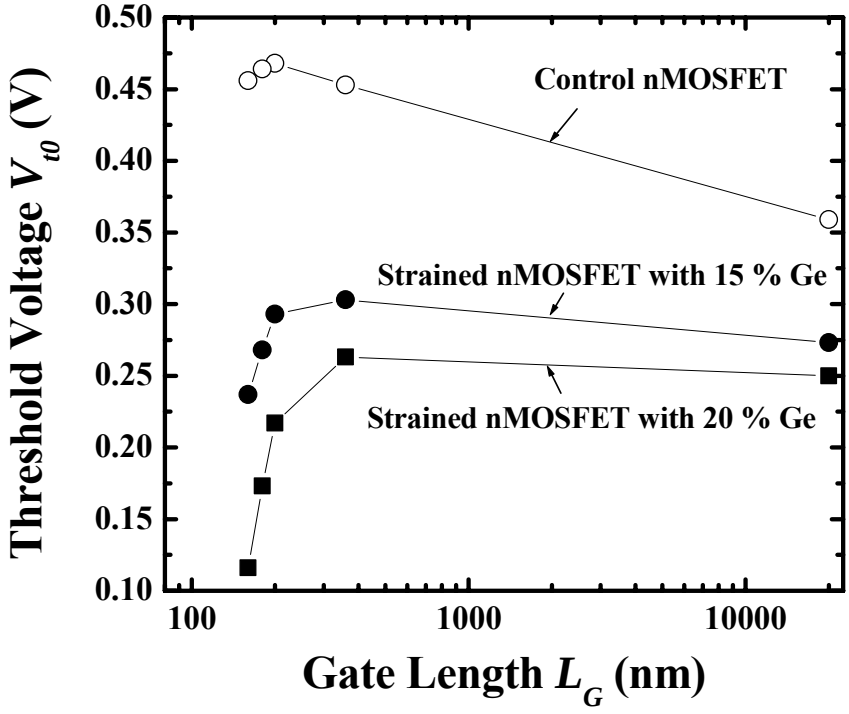


Figure 3.6 : V_t roll-off characteristics of the strained and control nMOSFETs. V_t decreases with increasing Ge % in the relaxed SiGe layer.

The decrease in V_t can be attributed to a few reasons. The first reason is due to the presence of the conduction and valence band offset in the strained Si / relaxed SiGe heterostructure. Figure 3.7 shows the band alignment of strained Si on relaxed SiGe substrates. For strained Si nMOSFETs, the conduction band offset makes the fermi level closer to the conduction band, which in turn, induces more electrons in the inversion layer with the same gate bias. Also, with this type of band alignment, electrons tend to be confined at the strained Si, in the channel, making the channel easier to invert. Thus, the band offset lowers the threshold voltage and makes the channel depletion shallower.

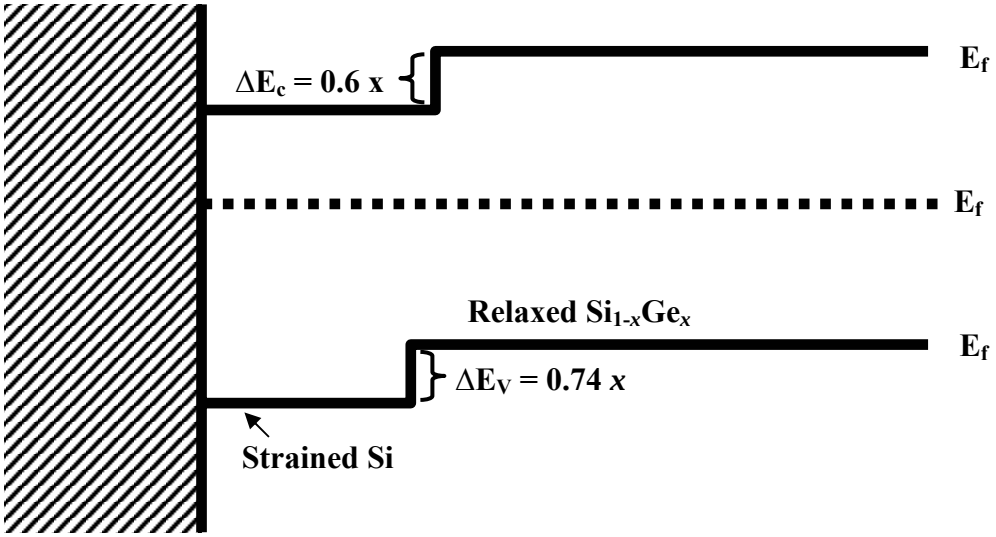


Figure 3.7: Bandgap alignment (Type II) of strained Si on relaxed $Si_{1-x}Ge_x$ buffer layer substrate

Another reason that causes the V_t shift of the strained Si MOSFETS is due to the difference in diffusitivity of dopants in the SiGe layer. Boron diffusion is retarded [34] while Arsenic and Phosphorus diffusion is enhanced in the presence of Ge atoms [35]. In the case of nMOSFETs, B segregation in the relaxed SiGe layer beneath the gate, away from the strained Si channel, results in the drop in V_t. This can be visualized as a lower V_t

implant dose, usually targeted at the channel region. In addition, the enhanced diffusion of As and P in SiGe could mean that the there would be more lateral diffusion of these dopants from the source and drain region into the region below the gate and channel. This could indirectly lower substrate doping, N_A which reduces V_t.

Yet another reason could be due to the presence of misfit dislocations at the strained Si / relaxed SiGe interface. Partial relaxation of the strained Si layer can lead to misfit dislocations at the strained Si / relaxed SiGe interface. As shown in Figure.3.8, these misfit dislocations can act as alternative paths for the diffusion of dopants from the source and drain to diffuse into regions below the gate at the strained Si / relaxed SiGe interface [11]. This may also lower substrate doping, N_A, lowering V_t.

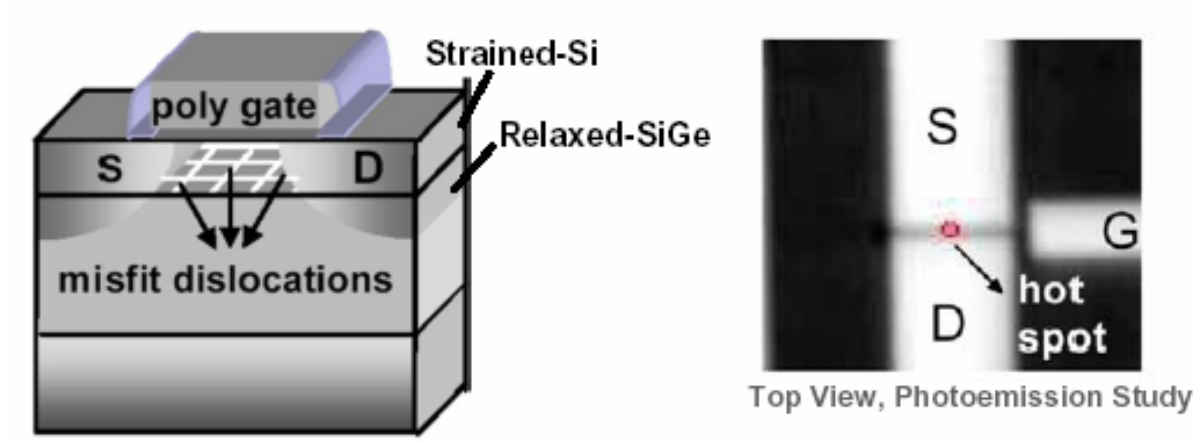


Figure 3.8 : (a) Presence of misfit dislocations found at the strained Si and relaxed SiGe interface and (b) top-view photo-emission analysis of a wide channel strained Si transistors. A localized leakage path is observed. [11]

In the case of strained Si pMOSFETs, the V_t is higher. This could be due to the valence band offset that causes holes to be confined in the SiGe layer at the Si/ SiGe interface, resulting in a parasitic buried channel. However in this work, pMOSFETs are of less interest as no enhancement is observed, consistent with earlier works [9] - [11].

As illustrated earlier in Figure 3.5, a higher off-state leakage current I_{off} is observed in the strained Si nMOSFETs. In fact, the higher the Ge % in the relaxed SiGe layer, the higher the I_{off} in the strained device. This increase in I_{off} could be attributed to two reasons. One reason for the increase is due to the reduction in V_t of the strained devices. The other reason contributing to the increase in I_{off} is the presence of misfit dislocations (Figure 3.8) found at the strained Si and relaxed SiGe interface, which provide alternative current paths from source to the drain even at off-state mode. Both reasons also explain the observation where higher off-state leakage current is found in nMOSFETs with higher Ge % in the relaxed SiGe layer. Higher Ge % would imply a lower V_t and the presence of more dislocations, resulting in higher I_{off}. Figure 3.9 shows a box plot of the I_{off} of the control and strain devices measured over a sample of 5 dies.

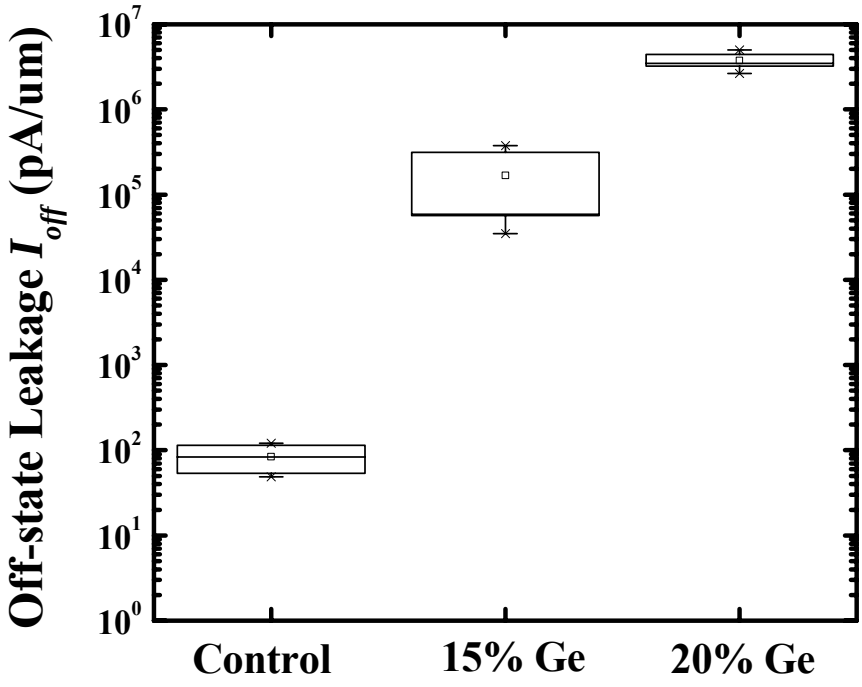


Figure 3.9 : Box plot showing measured I_{off} values over a range of 5 dies for control and strained nMOSFETs at gate length of 0.18 μm.

3.3.3 Circuitry Speed

As discussed previously in chapter 1, increase in drive current, I, should theoretically result in a reduction in time delay t_d. However, time delay measurements on a 127-stage ring oscillator reveal no improvement in circuitry speed at all. The time delay in both cases is about 26 ps.

This could be attributed to the fact that the increase in drive current is compensated by the increase in loading parasitic capacitance *C* which comprises of several components, including source / drain junction capacitance and overlap capacitances. Figure 3.10 illustrates the gate to source / drain overlap capacitance C_{OV} measurements as a function of the applied bias for both control and strained Si devices.

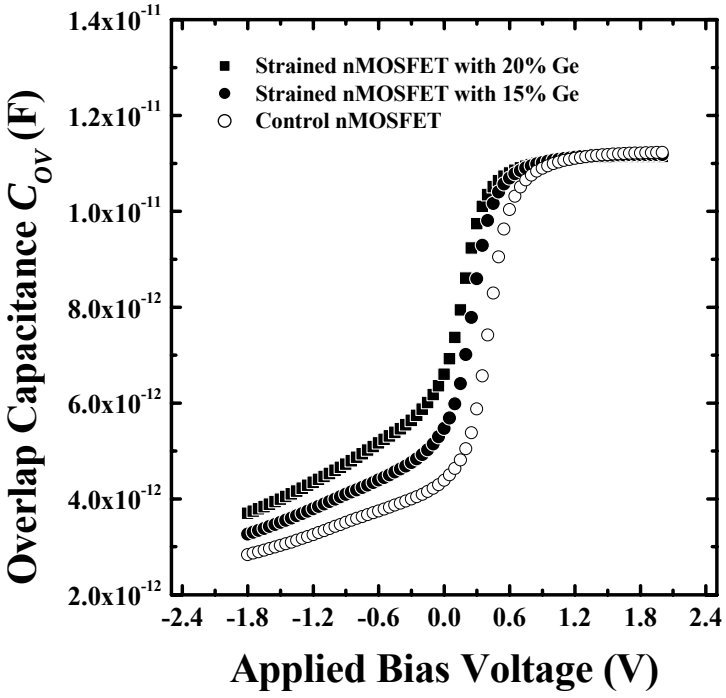


Figure 3.10 : Comparison of overlap capacitance C_{OV} between control and strained nMOSFETs. With increasing Ge % in the relaxed SiGe layer, overlap capacitances increases.

From measurements (Figure 3.10), the overlap capacitance C_{OV} increases with Ge concentration in the relaxed SiGe layer. This can be explained by the enhanced lateral diffusion of the SDE region in strained Si / relaxed SiGe nMOSFETs. In addition, an increase in misfit dislocations, threading from the source to the drain, also increases the number of paths that aid the lateral diffusion of SDE dopants into the channel region beneath the gate. With an increase in overlap capacitance, the increase in drive current might have been compensated by this increase in loading capacitance, attributing to the only slight or no improvement in the time delay t_d.

3.4 Summary

In summary, global strained Si / relaxed SiGe CMOSFETs have been fabricated. No drain current I_{DS} enhancement can be observed in the strained pMOSFETs. While enhancement in I_{DS} is demonstrated in the strained nMOSFETs, the leakage current I_{off} is also much higher than that in the control devices due to lowering of the threshold voltage. Degradation in sub-threshold characteristics is also found in the strained nMOSFETs. Therefore, HALO pocket implant optimization might be required in order to improve the sub-threshold and electrical characteristics of MOSFET devices fabricated using strained Si / relaxed SiGe substrates. However, there are still issues like the misfit dislocations and self-heating effects which can pose serious problems in the implementation of devices on strained Si / relaxed SiGe substrates. In addition, thermal budget of the entire process flow had to be kept to a minimum as out-diffusion of Ge from the relaxed SiGe layer to the Si-SiO_2 gate dielectric interface can result in interface trapped charges. In the

following chapters, a more cost effective and manufacturable approach to induce beneficial strain in n and pMOSFETs will be discussed extensively. But prior to that, some material characterization techniques to help characterize strained Si MOSFET structures will be discussed in the following chapters.

CHAPTER 4

Characterization of Strained MOSFET Structures with S/D Stressors

4.1 Background

Recently, channel strain engineering has been aggressively explored for enhancement in transistor performance. One attractive approach to enhance carrier mobility and transistor drive current makes use of strain-induced effects. It has been shown that hole mobility is considerably enhanced in a pMOSFET employing silicon-germanium (SiGe) stressors in the source and drain (S/D) regions [17]. Therefore, in order to better understand how stresses occur, in how far they are harmful or beneficial for the devices and how to control them, it is mandatory to characterize the structure of such strained MOSFET devices.

First and foremost, one main priority is the characterization of the strains in these devices experimentally or through modeling, such that this information can be taken into account during the design phase. At present, there are various techniques to provide information on strain in Si - the convergent beam electron diffraction (CBED) method of transmission electron microscopy (TEM), x-ray micro-diffraction (XRD) and micro-raman spectroscopy. These three techniques each have their pros and cons. Raman spectroscopy is the easiest to apply, but has limited spatial resolution. The x-ray micro-diffraction resolution is better, but at this moment only in one direction. The Raman

spectroscopy suffers from the fact that it measures a weighted value of stress with depth. X-rays can distinguish between different strain values at different depths, but careful data analysis must be carried out to obtain a complete strain profile. X-ray micro-diffraction also required large blanket size samples (at least hundreds of microns) for characterization. CBED has the best resolution and can be applied on thin cross-sectional samples with uniform strain along the depth. It also offers nanometer resolution and the capability to produce a 2-dimensional strain profile. But this technique is tedious and requires rigorous analysis of the HOLZ lines [36], [37]. In this chapter, we propose an alternative technique to characterize strains in the Si channel of MOSFET structures by analysis of the cross-sectional high resolution TEM (HRTEM) image at the channel region. This technique allows a 2-directional strain profile mapping of the structure and has a resolution comparable to that of the CBED technique. In order to describe and demonstrate the feasibility of this strain characterization technique, dummy MOSFET structures employing SiGe S/D stressors have been fabricated. In addition, as lateral tensile strain ε_{xx} and vertical compressive strain ε_{zz} would improve the electron mobility [26], [27] in nMOSFETs, a novel nMOSFET structure comprising a Si channel sandwiched between silicon-carbon (SiC) S/D stressors is proposed and fabricated for the first time to elucidate the channel strain distribution before its implementation at device level. The extracted strain profiles are then verified using finite element stress simulation results.

Apart from strain characterization, extraction of the Ge content in the S/D regions in the transistor structure is also essential to provide more information on strain induced in the channel. Energy dispersive x-ray spectroscopy (EDS), a technique used to extract

information on the quantitative content of specific regions on the cross TEM sample will be discussed.

4.2 Strain Analysis of MOSFET Structures with S/D Stressors

4.2.1 Strained MOSFET Structure Fabrication

For demonstration of this strain characterization technique, dummy MOSFET structures with SiGe and SiC S/D stressors are fabricated. Dummy MOSFET structures were used in place of actual MOSFET device in order to reduce the process time. Bulk Si substrates with (001) surface orientation were employed in this experiment. Gate pattern with a minimum feature size of 35 nm was formed on the substrates using 248 nm wavelength lithography and photoresist trimming techniques. The source-to-drain direction is along a [110] crystal direction. A 40 nm deep Si recess was etched in the S/D regions using dry plasma etch. The process was tuned so that the sidewall profile of the recess was tapered. Dilute HF solution was used for removal of any native oxide in the recessed regions prior to epitaxial growth in an ultra high vacuum chemical vapor deposition (UHVCVD) chamber. For growing SiC in the S/D recess regions, disilane (Si_2H_6) and dilute monomethylsilane (SiH_3CH_3) precursor gases were used. Chlorine (Cl_2) was intermittently introduced to achieve selective epitaxial growth. A low growth temperature (~600°C) was employed to avoid carbon precipitation. The mole fraction of carbon incorporated in the SiC stressor is 1%. $Si_{0.99}C_{0.01}$ has a lattice constant ~0.6% smaller than that of Si. On another wafer, selective epitaxy of $Si_{0.75}Ge_{0.25}$ in the S/D regions was performed at 600°C using Si_2H_6, GeH_4, and Cl_2 gases. $Si_{0.75}Ge_{0.25}$ has a

lattice constant ~1% larger than that of Si. Figure 4.1 illustrates a schematic of the transistor structures while Figure 4.2 shows the cross-sectional TEM image of the fabricated transistor structures with (a) $Si_{0.75}Ge_{0.25}$ and (b) $Si_{0.99}C_{0.01}$ S/D stressors.

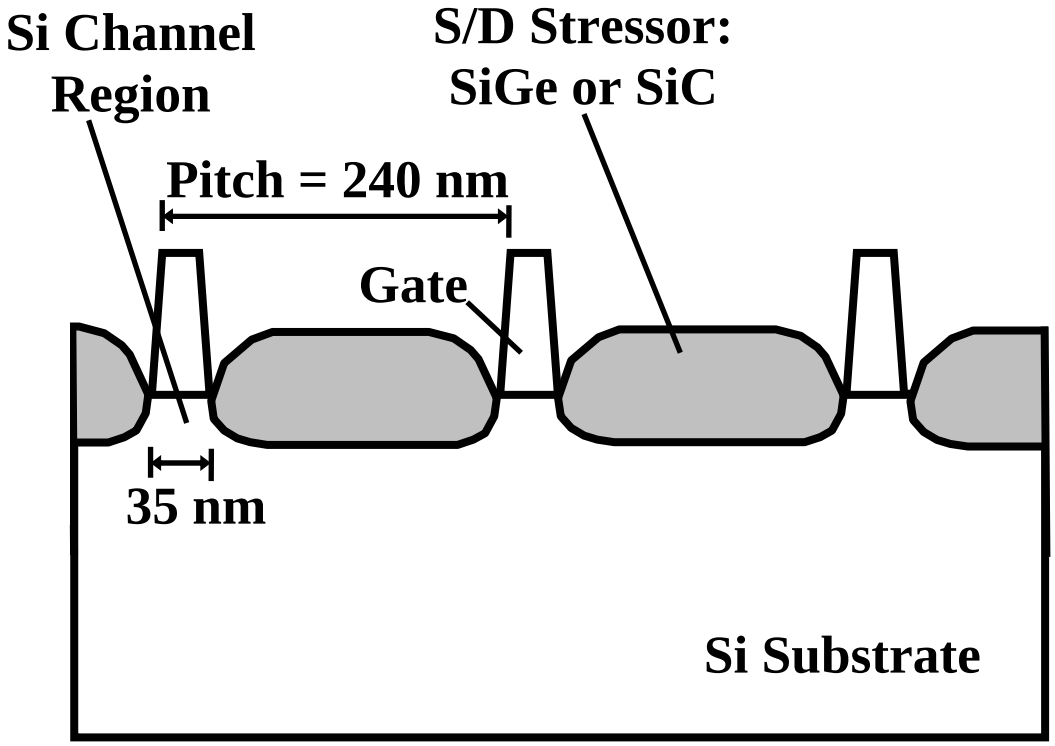


Figure 4.1 : Schematic of transistor structures with epitaxially grown SiGe or SiC in the source/drain regions to form source/drain (S/D) stressors.

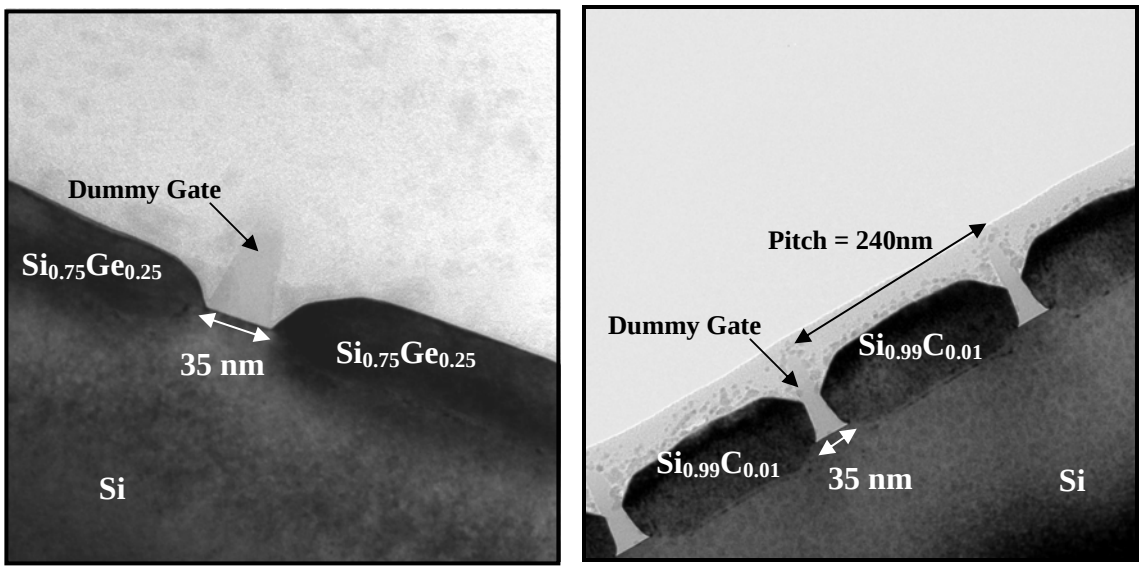


Figure 4.2 : Cross-sectional transmission electron microscopy (TEM) image of a structure with (a) $Si_{0.75}Ge_{0.25}$ S/D stressors and (b) $Si_{0.99}C_{0.01}$ S/D stressors. The gate electrode has a feature size of 35 nm and the pitch of the gate array pattern is 240 nm.

4.2.2 Strain Characterization

Figure 4.3 shows a high magnification view of the $Si_{0.75}Ge_{0.25}$ stressor and the strained Si channel depicted in Figure 4.2 (a). A 3 nm × 3 nm image or region of interest, as indicated by the solid square in Figure 4.3, was selected for Fast Fourier Transform (FFT) analysis to produce the diffractogram in Figure 4.4 (a). The bright spot at the center *O* of the diffractogram corresponds to the DC component of the image intensity in the 3 nm × 3 nm region. High spatial frequency components appear away from *O*, and each spatial frequency peak corresponds to a periodicity found in the selected image. The separation *d* between *O* and a spatial frequency peak is directly proportional to the reciprocal of the atomic spacing *a* in the direction from *O* to the peak, i.e. $d = 2\pi/a$. The (002) and (220) reflections, as selected by a filtering process [Figure 4.4 (b) and (c)], contain information on the vertical atomic spacing a_z (in the [001] direction) and the lateral atomic spacing a_x (in the [110] direction), respectively. Figure 4.4 (d) shows the

intensity profile of the filtered (002) peaks. Examination of the intensity profiles of Figure 4.4 (b) and (c) obtained a_z and a_x, the local lattice parameters for the region of interest. The above analysis was repeated for an array of 3 nm × 3 nm regions throughout the HRTEM image to obtain a_x and a_z as a function of (x, z). To calculate the percentage change in the lattice constants or the strain components for an arbitrary location (x, z), we employ $\varepsilon_{xx} = (a_x - a_{x,ref})/a_{x,ref}$ and $\varepsilon_{zz} = (a_z - a_{z,ref})/a_{z,ref}$, where $a_{x,ref}$ and $a_{z,ref}$ are the atomic spacings in a reference region that is not strained. A region in the HRTEM image where the ratio a_z/a_x corresponds to a_z/a_x of Si ($\sqrt{2}$) was chosen as the reference region. Strain distorts the crystal lattice and causes this ratio to deviate from $\sqrt{2}$. In Figure 4.3, the dotted square region is thus designated the reference region.

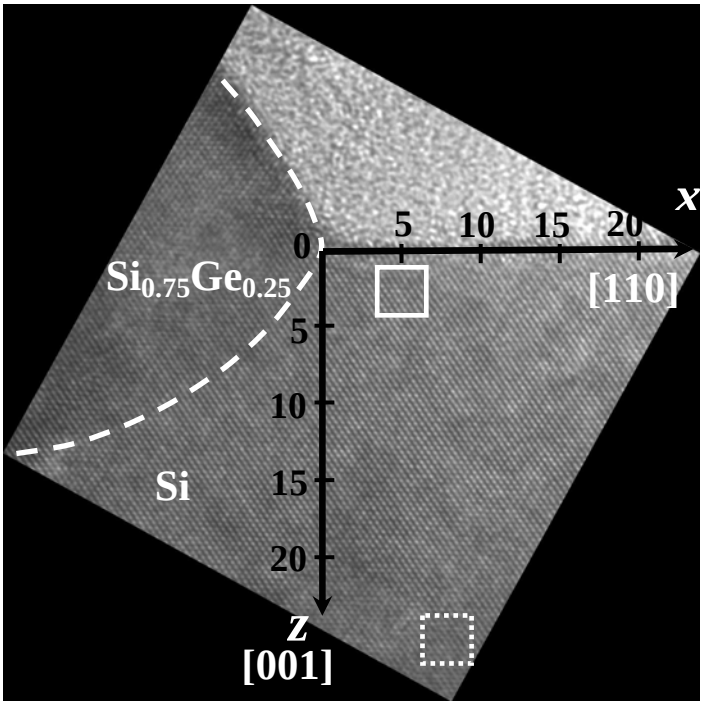


Figure 4.3 : A high magnification HRTEM image of a transistor structure with $Si_{0.75}Ge_{0.25}$ stressors in the source/drain region. The region enclosed by the dashed line features a SiGe material which was pseudomorphically grown on the recessed Si source/drain region.

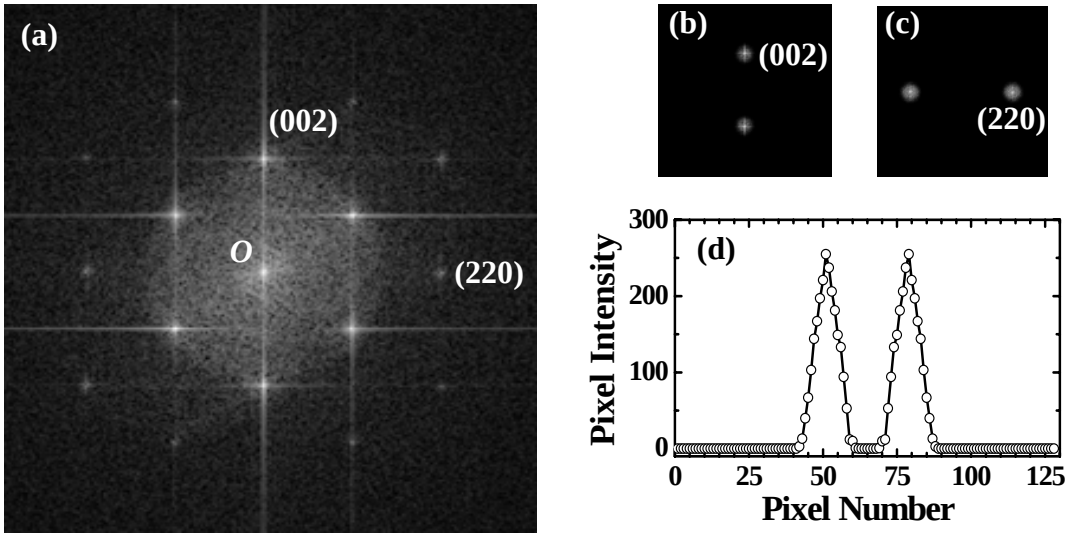


Figure 4.4 : (a) The reciprocal space diffractogram is obtained by Fast Fourier Transform (FFT) of a selected region in the TEM image of Figure 4.3. The diffractogram is then filtered to obtain (b) the (002) reflection and (c) the (220) reflection, which contain information about the lattice spacings in the vertical and lateral directions, respectively. The intensity profile for the (002) reflection is shown in (d). The separation between the intensity peaks is twice the separation *d* from *O* to each peak, and can be translated into real space lattice spacing *a* using $d = 2\pi/a$

The distribution of lateral strain ε_{xx} and vertical strain ε_{zz} in the channel region sandwiched between the $Si_{0.75}Ge_{0.25}$ S/D stressors is then examined. Figure 4.5 (a) reveals that ε_{xx} is generally compressive, i.e. negative. Near the Si surface and the SiGe stressor, the lateral lattice constant is 0.8 % smaller than that in the reference (strain free) region. The magnitude of this compressive ε_{xx} decreases with increasing depth *z*. Figure 4.5 (b) plots the distribution of the vertical strain component ε_{zz}, showing a large tensile strain near the SiGe stressor and directly beneath the Si surface. The depth profile for both ε_{xx} and ε_{zz} investigated in this work are consistent with a simulation study using a similar structure [38]. Both the compressive ε_{xx} and tensile ε_{zz} contribute to hole mobility enhancement in a p-channel transistor.

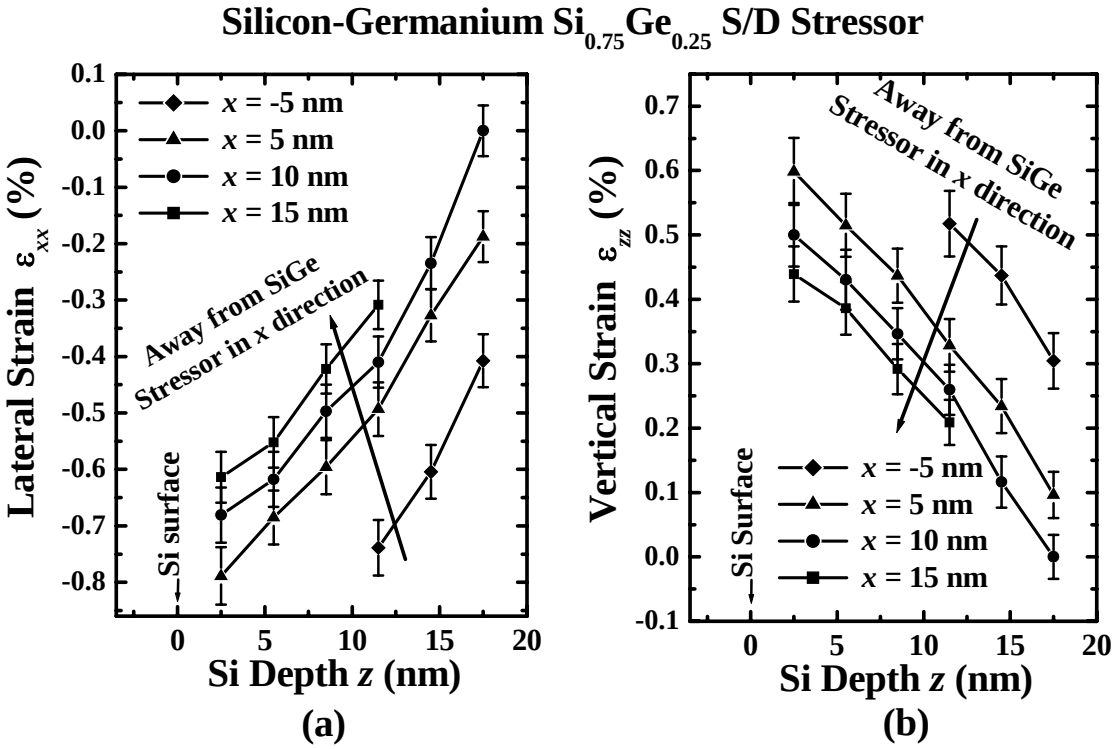


Figure 4.5 : The distribution of strain components in a transistor structure with $Si_{0.75}Ge_{0.25}$ stressors in the source/drain regions. (a) Large lateral compressive strain is observed near the heterojunction and directly beneath the Si surface. (b) The Si lattice is stretched in the vertical direction, and a vertical tensile strain is induced.

Next, the same strain analysis technique as described above is being applied onto the MOSFET structures with $Si_{0.99}C_{0.01}$ S/D. The lattice mismatch at the sidewall heterojunction between the Si channel (having a larger lattice constant in the relaxed state) and $Si_{0.99}C_{0.01}$ S/D (having a smaller lattice constant in the relaxed state) gives rise to a vertical compressive strain which in turn leads to a lateral tensile strain in the Si channel. Figure 4.6 (a) shows the resulting spatial distribution of the lateral strain ε_{xx} in the Si channel of the fabricated structure with $Si_{0.99}C_{0.01}$ S/D.

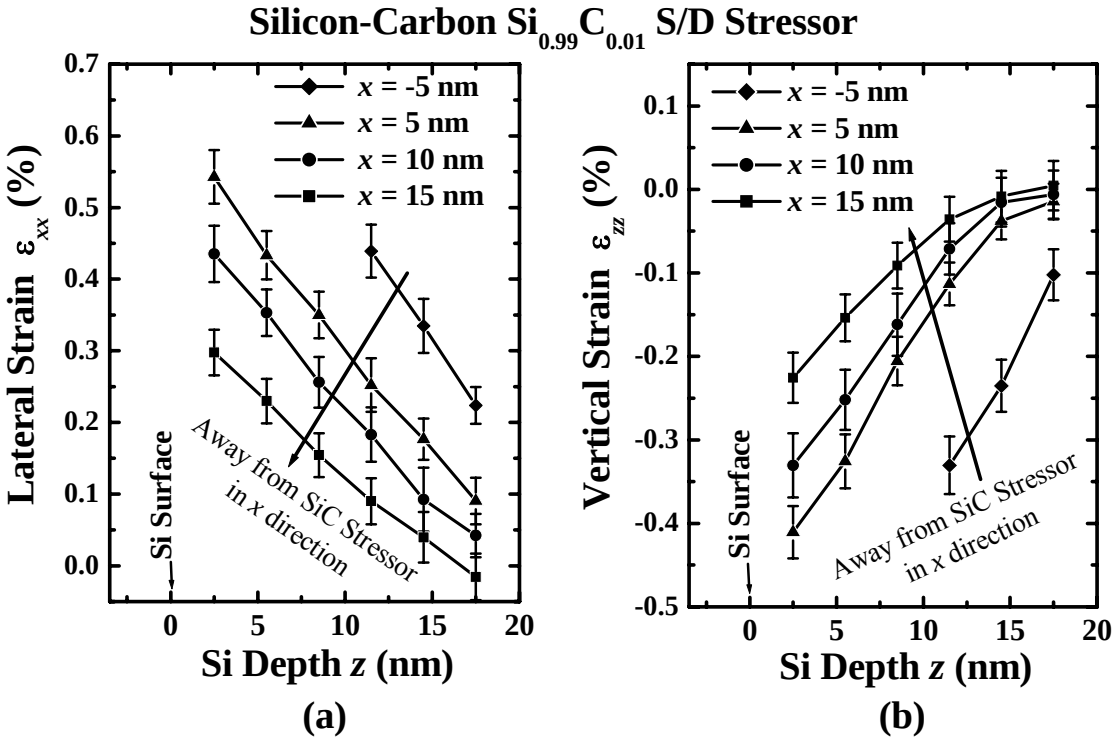


Figure 4.6 : The distribution of (a) the lateral strain component and (b) the vertical strain component in a transistor structure with $Si_{0.99}C_{0.01}$ source/drain stressors. A relatively large lateral tensile strain ε_{xx} was induced in Si near the Si-$Si_{0.99}C_{0.01}$ heterojunction. The magnitude of the lateral tensile strain decreases with increasing *z*. The $Si_{0.99}C_{0.01}$ lattice also interacts with the Si lattice to induce a vertical compressive strain in the Si channel.

The magnitude of ε_{xx} is the largest in the vicinity of the stressor, and decreases with increasing depth. ε_{xx} also decreases towards the middle of the Si channel. $Si_{0.99}C_{0.01}$ has a smaller lattice constant than Si, leading to a vertical compression of the Si lattice adjacent to the $Si_{0.99}C_{0.01}$ stressor. Figure 4.6 (b) clearly shows this vertical compression in the Si channel region. The magnitude of ε_{zz} decreases with increasing depth in the Si substrate as expected. A finite element study using the ANSYS simulation tool was independently performed to investigate the distribution of strain components in MOSFET structures with SiC S/D regions [Figure 4.7 (a), (b) and (c)] and the results are found to be in good agreement with the extracted strain profile.

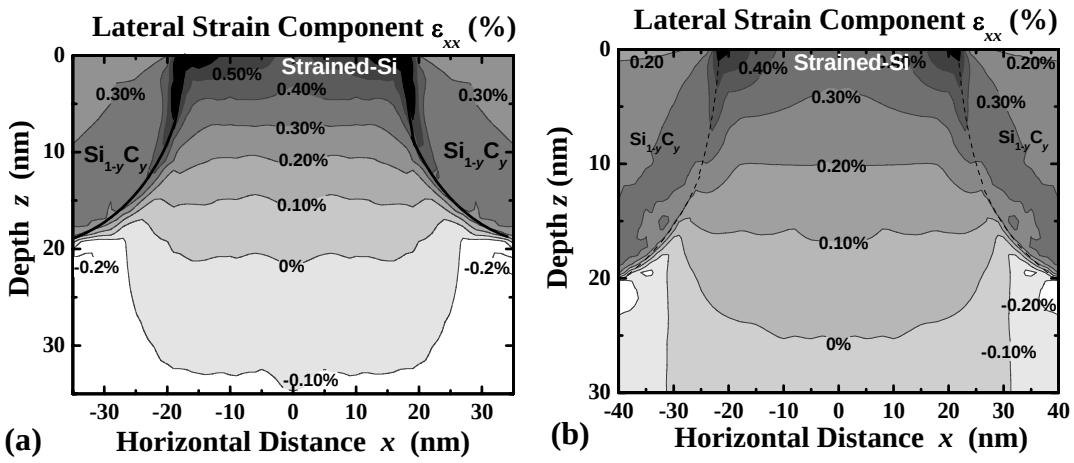


Figure 4.7 : Distribution of the simulated lateral strain component ε_{xx} (in %) in the Si channel and $Si_{0.987}C_{0.013}$ S/D regions, using a finite element method for gate length of (a) 30 nm and (b) 50 nm. In this simulation, a recess depth of 20 nm was used. The horizontal distance from the $Si_{0.987}C_{0.013}$–strained-Si heterojunction at the Si surface is denoted by *x* while the vertical distance from the Si surface is denoted by *y*.

4.3 Energy Dispersive X-Ray Spectroscopy (EDS) Analysis

In MOSFET structures with SiGe S/D regions, it would be of interest to know the Ge content in the S/D regions for an indirect inference to the strain induced in the channel and correlation to the electrical data of the device. Energy Dispersive X-Ray Spectroscopy (EDS) [39] can also be applied to the TEM samples that are being prepared for strain analysis described in the previous section of this chapter. In particular, this technique would be extremely useful for the analysis of condensed SiGe S/D regions in a novel pMOSFET device that will be discussed in one of the subsequent chapters. A simple illustration of the concept of EDS is shown in Figure 4.8. An electron beam, when focused on a sample generates characteristic x-rays with energy unique to the ionized atom. The x-rays are then collected by a detector which generates charge pulses proportional to the each specific x-ray energy, generating a spectrum which shows the

elemental make-up of the sample. The beam can be focused into very small beam size, down to 5 nm. Therefore, this technique can be used to detect the elemental make-up at different location of the cross TEM sample of the MOSFET structure. Figure 4.9 shows an example of a TEM image revealing the Ge content (within an accuracy of 2% to 3%) in the SiGe S/D regions.

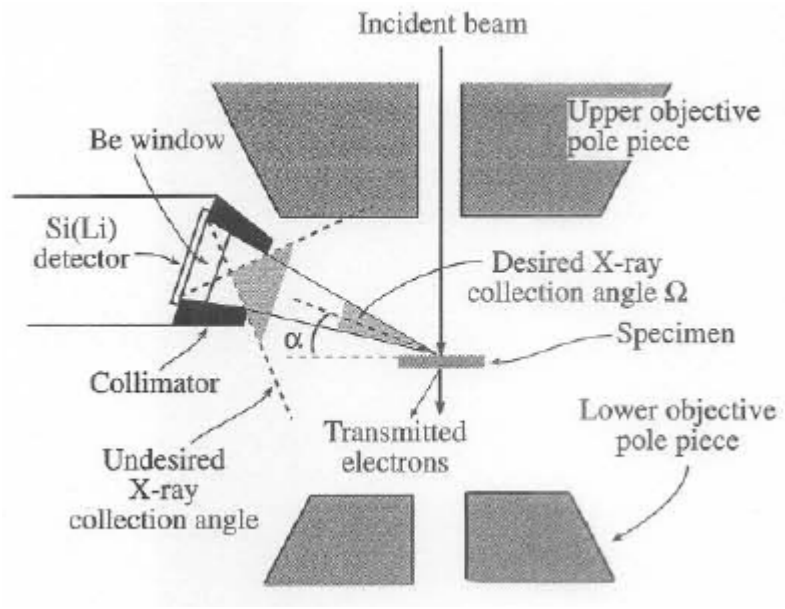


Figure 4.8 : A simple schematic illustrating how EDS in a TEM system works. X-rays generated by the interaction of the incident electrons with the sample are collected by the detector which feeds the signal to a computer to generate elemental spectrums [39].

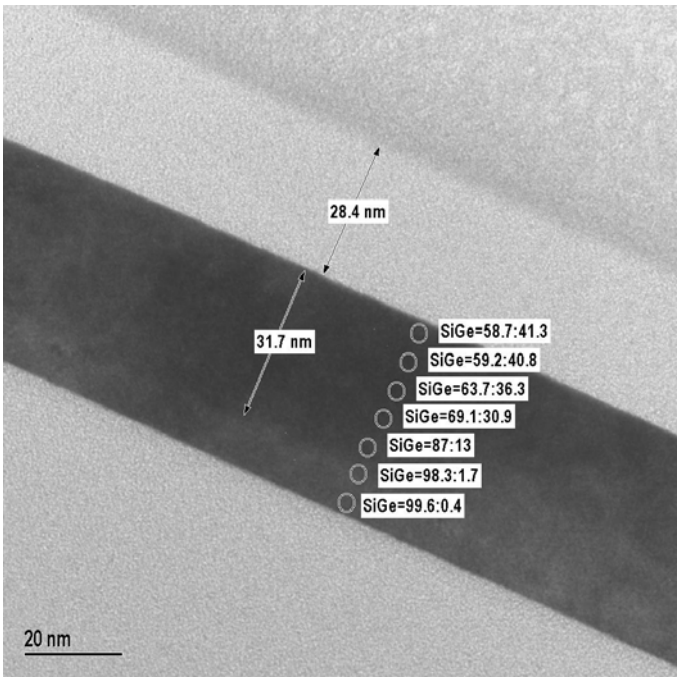


Figure 4.9 : An example of a TEM image which illustrates the elemental composition of the TEM sample.

4.4 Summary

In summary, a new technique to characterize strain in MOSFET structures with S/D stressors via analysis of HRTEM images is proposed. Both experimental and simulated results are found to be in good agreement. In addition, a novel structure with SiC S/D is fabricated to show the presence of lateral tensile strain and vertical compressive strain in the Si channel, making it a viable option for enhanced device performance in nMOSFETs for future technology nodes. The TEM EDS system has also been discussed briefly. This technique is suitable for characterization of strained MOSFET structures with SiGe S/D regions due to its capability of obtaining the elemental composition at different locations of a MOSFET structure with excellent resolution down to 5 nm.

CHAPTER 5

Strained nMOSFETs using SiC S/D Regions

5.1 Strained nMOSFETs with SiC S/D on Bulk Substrate

5.1.1 Background

Scaling of the metal-oxide-semiconductor field-effect transistor (MOSFET) has led to significant improvement in speed performance and integrated circuit density. In addition to device scaling, further improvement in transistor speed performance is achievable by enhancing the carrier transport properties. The carrier mobility in silicon (Si) can be improved by strain-induced modification of the electronic band structure [40], leading to significant drive current enhancement [9] – [11], [41]. Furthermore, high carrier mobility opens up the possibility of near-ballistic operation in aggressively scaled transistors. Carriers under ballistic transport encounter no scattering in the channel, and the transistor drive current I_{Dsat} is determined by the source injection velocity v_{inj} [42], [43]. Therefore, increasing v_{inj} through strain induced band engineering will also be important for maximizing the performance of the ballistic MOSFET [44].

In nMOSFETs, one way to enhance the electron mobility is to use a biaxial tensile strained-Si channel formed on a relaxed silicon-germanium (SiGe) layer [9]-[11], [41], [45]-[47]. However, high defect density and self-heating effects are associated with the strained-Si/SiGe substrate, and the approach has limited manufacturability due to a narrow process window [11], [46]. A more cost-effective and manufacturable approach to

improve electron mobility is to employ a high-stress silicon nitride (SiN) etch-stop-layer (ESL) which mechanically couples uniaxial tensile stress to the transistor channel region [15]-[17], [48]. Yet another approach to introduce uniaxial tensile strain in the Si channel is through the integration of a source and drain (S/D) material with a smaller lattice constant than Si [Fig. 1(a)]. A candidate material is silicon-carbon ($Si_{1-y}C_y$ or SiC), where the substitutional carbon is introduced in Si to result in a substantial reduction in the lattice constant compared to Si, as discussed in chapter 4. SiC S/D can be easily integrated in nMOSFETs in a CMOS process, similar to the integration of SiGe S/D in pMOSFETs [Fig. 1(b)] [17], [48], [49].

In this first part of the chapter, we report the concept and demonstration of a novel nMOSFET with silicon-carbon ($Si_{0.987}C_{0.013}$) S/D stressors for enhancing the drive current performance on bulk Si substrate. Due to the uniaxial tensile strain induced in the channel, electron mobility is enhanced. In addition, the novel device structure has several advantages over existing strained Si nMOSFET structures. First, the conduction band offset ΔE_c at the SiC–strained-Si heterojunction at the source end of the transistor could also provide for enhanced source injection velocity v_{inj}, which plays a vital role for carrier transport in the quasi-ballistic regime. Second, due to the raised S/D structure used, the series resistance could be reduced.

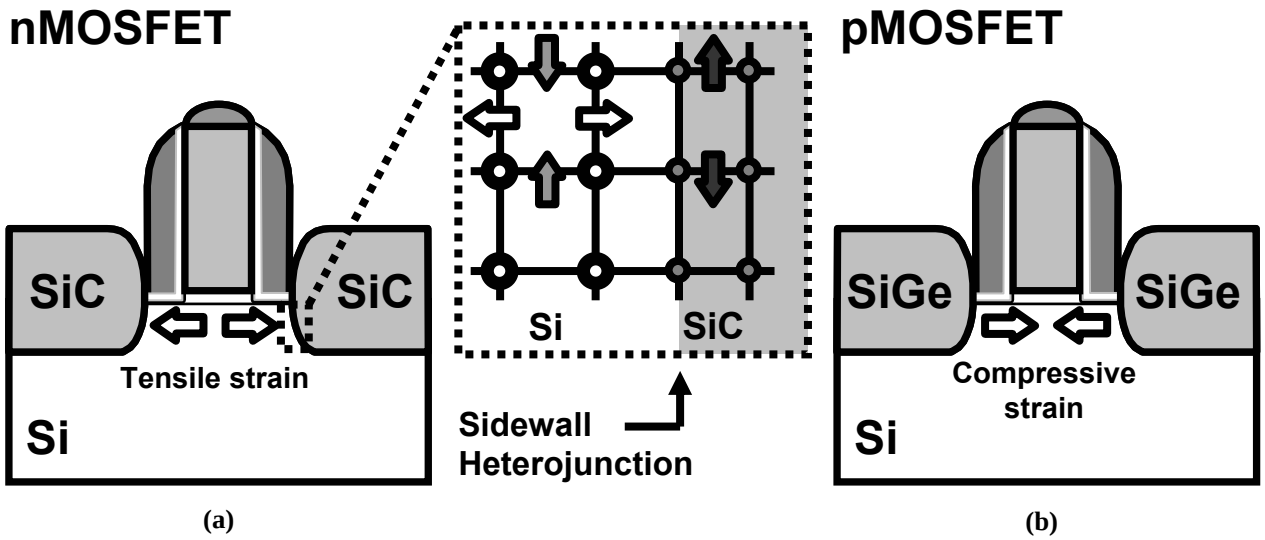


Figure 5.1 : (a) Schematic diagram of a proposed nMOSFET structure with selective epitaxially grown SiC in the source/drain (S/D) regions. The inset illustrates a magnified Si channel and SiC S/D sidewall heterojunction which induces a vertical compressive strain component, leading to a lateral tensile strain in the channel of the nMOSFET due to smaller lattice constant of SiC with respect to Si. (b) pMOSFET structure with selective epitaxially grown $Si_{1-x}Ge_x$ in the source/drain. Due to larger lattice constant of $Si_{1-x}Ge_x$, a compressive strain is induced in the channel of the pMOSFET.

5.1.2 Device Fabrication

nMOSFETs with $Si_{0.987}C_{0.013}$ S/D regions were fabricated using a single mask process [50]. The nMOSFET devices were fabricated on bulk Si substrate with (100) surface orientation. Threshold voltage V_t adjust and well implants were performed prior to atomic-layer deposition of HfAlO gate dielectric and sputter deposition of TaN metal gate. The equivalent SiO_2 thickness of the HfAlO gate dielectric is 3 nm. Silicon oxide was deposited on the TaN film as a hardmask. Gate patterning employed optical lithography and photo-resist trimming to reliably obtain gate lengths L_G down to 50 nm. After gate etch, a thin silicon oxynitride spacer was formed by plasma-enhanced chemical vapor deposition. This was followed by a Si recess etch of ~40 nm and a selective epitaxial growth of SiC in the S/D regions. Source and drain implantation and annealing were then performed. Along the lateral direction, the N+/P junction is located inside the

SiC/Si heterojunction. As a result, the ΔE_c at the SiC-strained-Si heterojunction at the source end of the transistor could provide for enhanced source injection velocity v_{inj} [44].

The epitaxial growth of SiC faces limitation in total incorporation of all the carbon into substitutional sites. We define a carbon substitutional efficiency factor η, also known as substitutionality, as the fraction of total carbon concentration incorporated in substitutional sites, as given by

$$\eta = \frac{C_{Sub}}{C_{Total}} \tag{5.1}$$

where C_{Total} is the total carbon concentration in the silicon and C_{Sub} is the concentration of carbon in substitutional sites.

From Figure 5.2, it can be seen that η decreases with increasing total incorporated carbon C_{Total}. The total carbon incorporated, C_{Total}, is determined by SIMS analysis while the atomic percentage of substitutional carbon, C_{Sub} is determined by XRD analysis. Substantial incorporation of substitutional carbon can give rise to larger induced strain in the transistor channel. By employing 1.3% substitutional carbon a lattice mismatch of 0.56% can be achieved [51], which can lead to substantial enhancement in drive current. Higher substitutional carbon % can be achieved by increasing the total carbon concentration C_{Total}. However, this will also lead to an increase in interstitial carbon concentration, which could pose problems like higher interface traps at the gate dielectric [52]-[54].

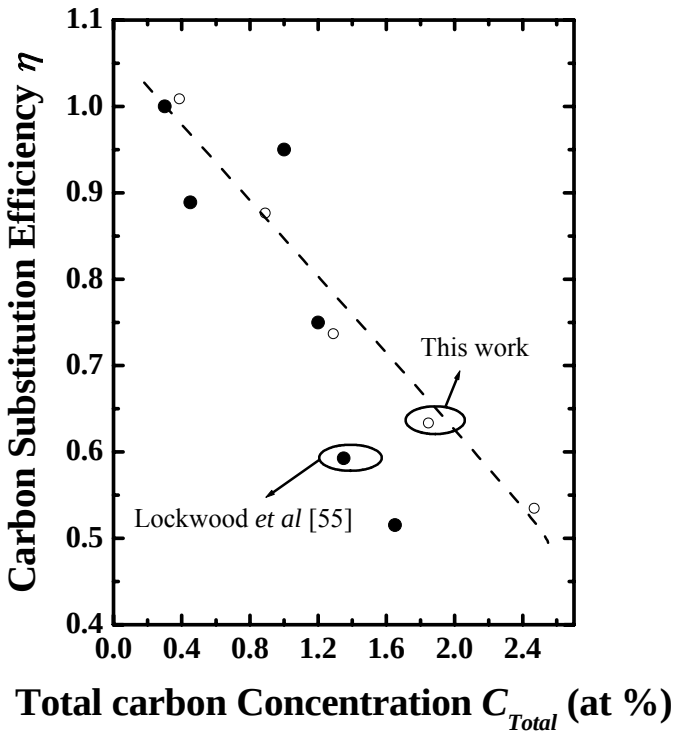


Figure 5.2 : Ratio of amount of carbon in substitutional sites C_{Sub} to the total amount of carbon incorporated C_{Total}, denoted by η (substitutional efficiency factor or substitutionality) plotted against C_{Total}. η decreases with C_{Total}, implying the limitations of introducing high carbon %. Results are benchmarked with previous work on SiC epitaxy [55].

On the control wafer, the Si recess etch and selective epitaxy steps were not performed. The S/D implant conditions for the devices were such that similar junction depths were obtained, as estimated using TSUPREM IV process simulation so that series resistance differences will be reduced.

5.1.3 Electrical Characterization

A. I-V Characteristics

Figure 5.3 (a) shows the cross sectional TEM image of a 50 nm gate length nMOSFET with $Si_{0.987}C_{0.013}$ S/D regions. One benefit of using SiC in the S/D regions is the enhanced electron mobility as a result of the lateral tensile strain and vertical compressive strain induced in the Si channel. Another benefit arises from the presence of a band offset ΔE_c at the heterojunction between the SiC source and the strained-Si channel. Strain results in an energy splitting in the conduction band of Si, leading to an energy band diagram as schematically illustrated in Figure 5.3 (b). This band offset (~65 meV [56]) could enable injection of electrons with additional energy ΔE_c, or at a higher velocity as explained by T. Mizuno *et al.* [44]. Both the enhanced electron mobility and increased injection velocity will result in a higher drive current for nMOSFETs. Figure 5.4 (a) plots the I_{DS}-V_{DS} characteristics of a 50 nm gate length control nMOSFET (open symbols) and strained nMOSFET with $Si_{0.987}C_{0.013}$ S/D regions (solid symbols). A 50% enhancement in drive current can be observed at a gate over-drive (V_{GS} - V_t) of 1.0 V and V_{DS} = 1.5V. Extraction of series resistance for both devices was performed and shown in the inset of Figure 5.4 (a). At high gate-overdrive, the channel resistance is assumed to be negligible, the overall source-to-drain resistance is mainly contributed by resistance at the source and drain side [60]. Comparable series resistance values were obtained. Figure 5.4 (b) explores the dependence of the drain current I_{DS} enhancement on gate over-drive and drain bias V_{DS} for the devices considered in Figure 5.3 (a). For a given gate over-drive, the I_{DS} enhancement increases with increasing V_{DS}. This is consistent with heterojunction barrier lowering with increasing V_{DS}, leading to enhanced carrier injection from the source

[44]. It is also observed that increasing gate over-drive, (V_{GS} - V_t) results in a decrease in the I_{Dsat} enhancement, which is in good agreement with Figure 5.5 (a) where mobility enhancement reduces with increasing effective vertical field. The mobility is estimated using the linear drive current equation at low V_{DS} of 0.1V, $I_{DS} = \mu_{eff} C_{ox} \frac{W}{L}(V_G - V_t)V_{DS}$, where the oxide capacitance C_{ox} was calculated assuming an EOT of 3 nm.

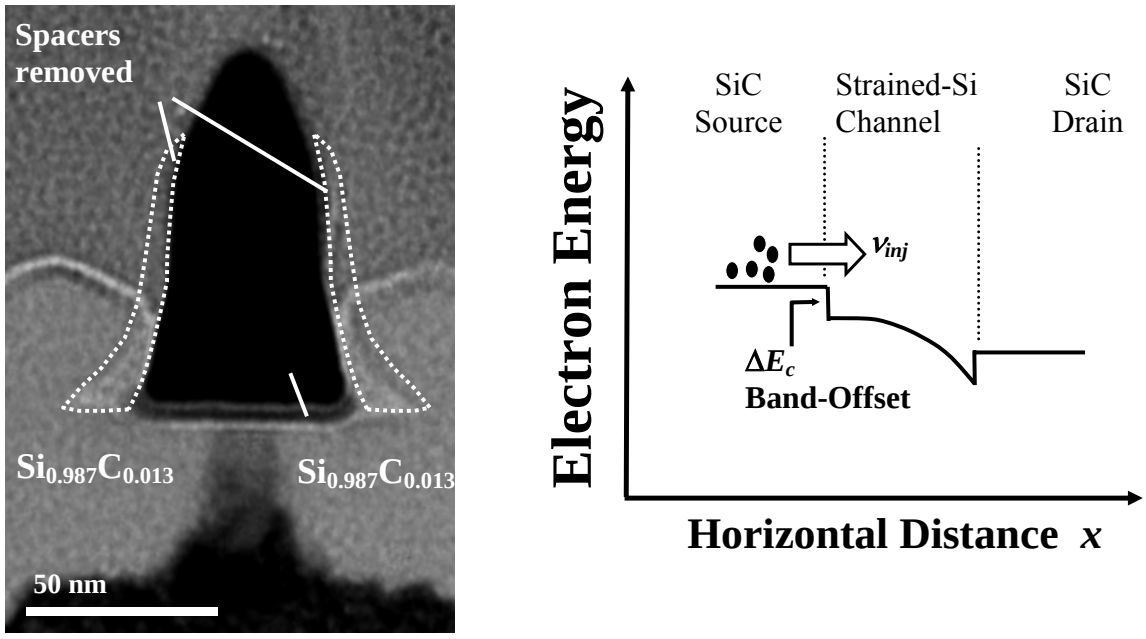


Figure 5.3 : (a) Cross sectional TEM image of a 50 nm gate length nMOSFET with $Si_{0.987}C_{0.013}$ S/D. The spacers and a hardmask that covered the metal gate during the selective epitaxy of $Si_{0.987}C_{0.013}$ were removed. (b) Conduction band profile from the source to the drain, illustrating enhanced electron injection velocity from the source into the strained-Si channel.

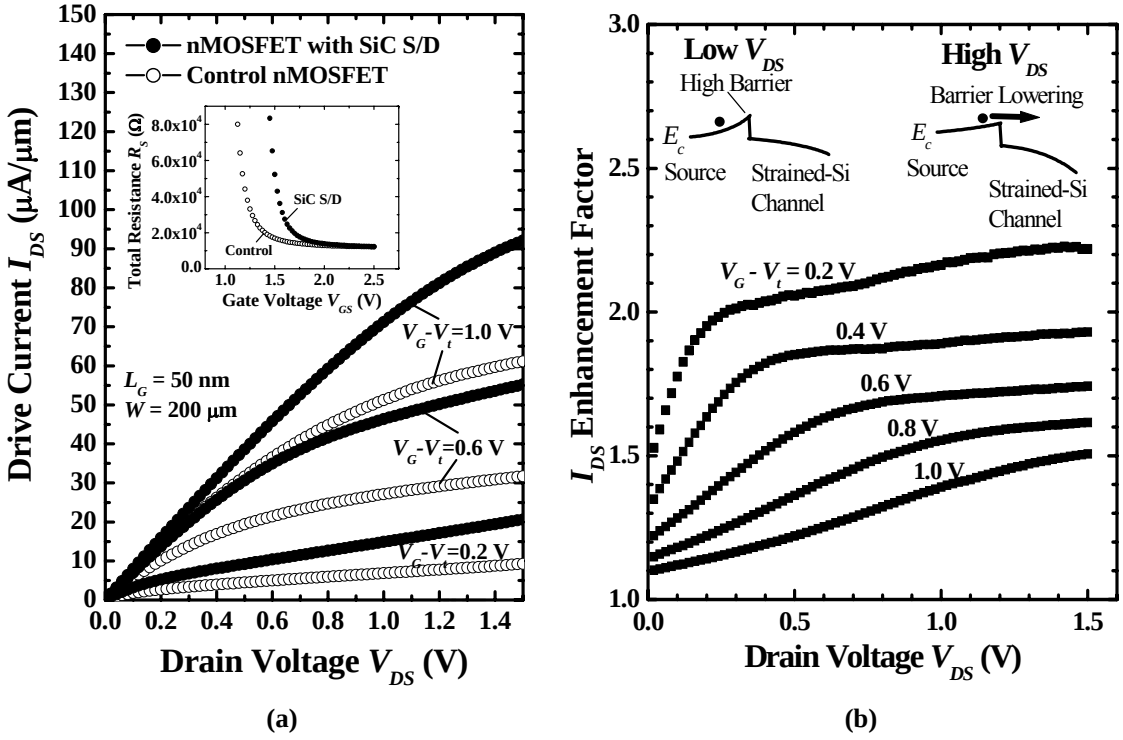


Figure 5.4 : (a) Output characteristics of 50 nm gate length nMOSFET with $Si_{0.987}C_{0.013}$ S/D regions, demonstrating 50% drive current I_{Dsat} enhancement at a gate over-drive (V_{GS} - V_t) of 1.0 V. Inset shows comparable extracted series resistance, attributing the majority of the drive current enhancement to strain effects. (b) Drain current I_{DS} enhancement factor as a function of drain bias V_{DS} and gate overdrive (V_{GS} − V_t). I_{DS} enhancement increases with higher drain bias and decreases with increasing gate over-drive.

Figure 5.5 (b) plots the drive current I_{Dsat} as a function of L_G, showing that nMOSFETs with $Si_{0.987}C_{0.013}$ S/D have larger I_{Dsat} enhancements at smaller L_G. This is attributed to the increase in the average strain level in the Si channel with a reduction in the spacing between the SiC S/D stressors, leading to increased mobility and also a larger ΔE_c. Therefore, I_{Dsat} enhancement due to strain effects and high electron injection velocity is expected to be even more pronounced in the sub-50 nm L_G regime.

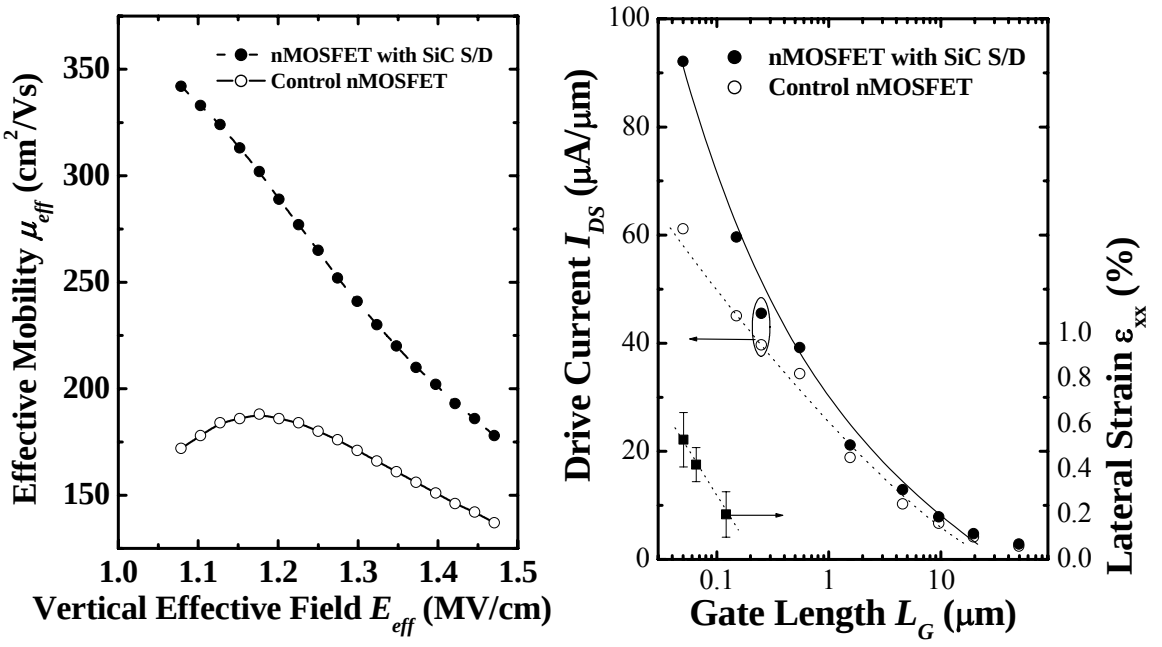


Figure 5.5 : (a) The extracted electron mobility shows 100% enhancement at low effective vertical field regime but decreases at higher effective field. The mobility is extracted using the linear drain current equation at low V_{DS} = 0.1 V. (b) Drive current I_{Dsat} as a function of L_G, as obtained from the fabricated devices, showing increasing I_{Dsat} enhancement with decreasing L_G.

A 40% enhancement in maximum transconductance is observed over the control devices in Figure 5.6 (a). The G_m-L_G plot (Figure 5.6 (b)) reveals the continual improvement in transconductance with decreasing L_G down to 50 nm. I_{DS}-V_{GS} characteristics are compared in Figure 5.7 (a). The inset in Figure 5.7 (a) plots the subthreshold swing as a function of the gate length in both SiC S/D and control nMOSFETs, showing a slightly higher subthreshold swing for the strained devices. At the minimum gate length of 50 nm, the transistor with SiC S/D regions has a slightly larger DIBL (0.245 V/V) compared to the control nMOSFET (0.176 V/V), possibly due to enhanced diffusion of As S/D dopants in SiC alloys [57].

The slightly higher V_t of the transistor with SiC S/D could be attributed to the successful formation of the SiC–strained-Si heterojunction outside the n^+ source region [44]. Figure 5.7 (b) shows the *C-V* characteristics of the devices, which indicates the elimination of gate depletion effects through the use of TaN metal gate. Gate leakage current density for both devices are comparable and less than 1×10^{-4} A/cm^2 at a gate overdrive of 1V..

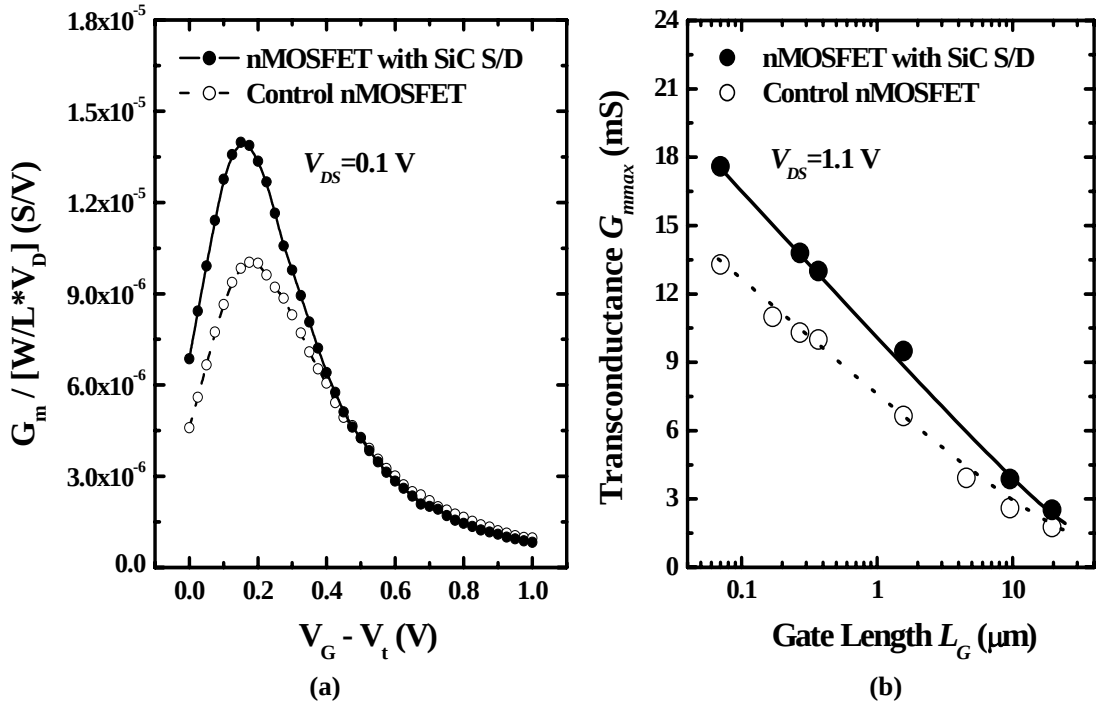


Figure 5.6 : (a) Transconductance G_m versus gate over-drive, $V_{GS} - V_t$, for uniaxial tensile strained nMOSFET. A 40% enhancement in G_m is observed over the control device. (b) Transconductance G_{mmax} as a function of gate length for control and strained NMOSFET. G_{mmax} improvement can be observed down to L_G=50 nm.

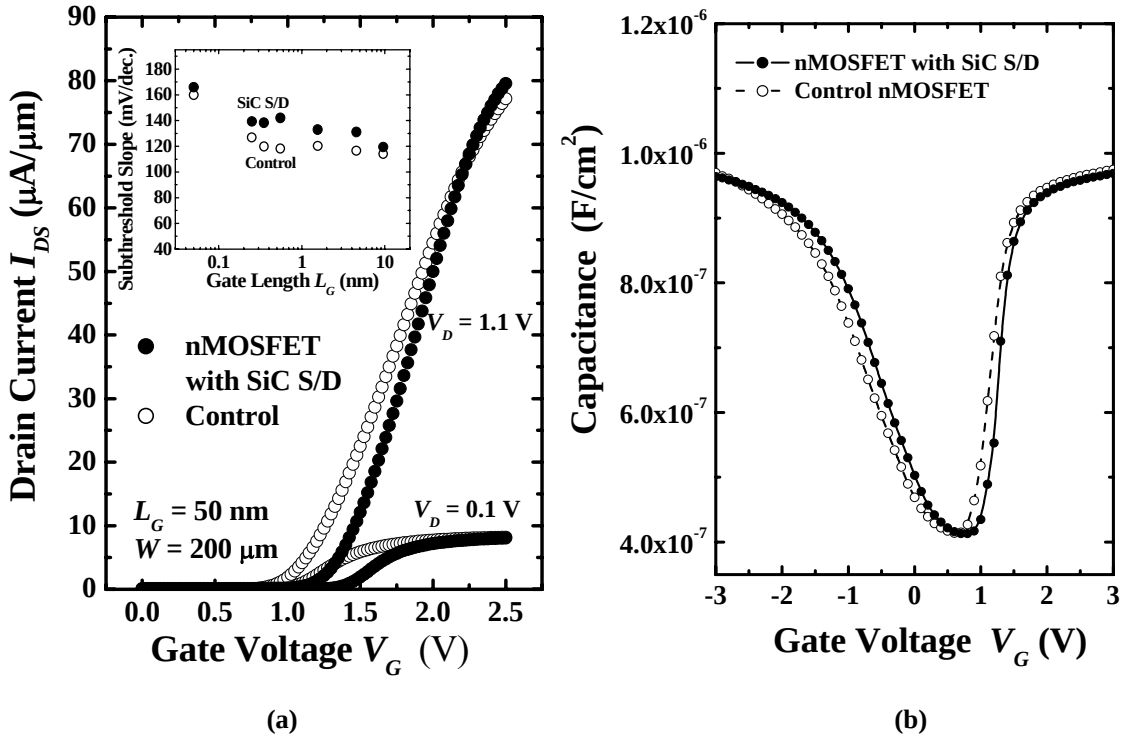


Figure 5.7 : (a) I_{DS}-V_{GS} characteristics of both strained and control device. The inset plots the subthreshold swing versus physical gate length L_G of both strained and control devices. (b) *C-V* characteristics showing the elimination of gate depletion effects by the use of metal gate electrode.

B. P-N Junction Characteristics

P-N junction diodes structures with pad size of 100 μm by 100 μm were fabricated to investigate the N+ source/drain to P- substrate diode junction characteristics. The target junction depth obtained from simulation is about 120 nm from the surface of the S/D regions. Therefore, the N+/P- junction depth is close to the SiC/Si heterojunction and any defects near the heterojunction could result in higher junction leakage. Figure 5.8 (a) plots the junction leakage of both SiC S/D and control nMOSFETs over a range of applied voltage bias. Comparable leakage values were obtained. Figure 5.8 (b) depicts the junction leakage current under a reverse bias condition of 1.5V with temperature

dependence between the range of 300K to 490K. Comparable temperature dependence of junction leakage current of SiC S/D and control nMOSFETs indicates similar junction leakage mechanisms. Junction capacitance measurements of both devices are shown in Figure 5.9. Comparable junction capacitance eliminates the possibility of reduction in circuit speed benefits from the increased current drive.

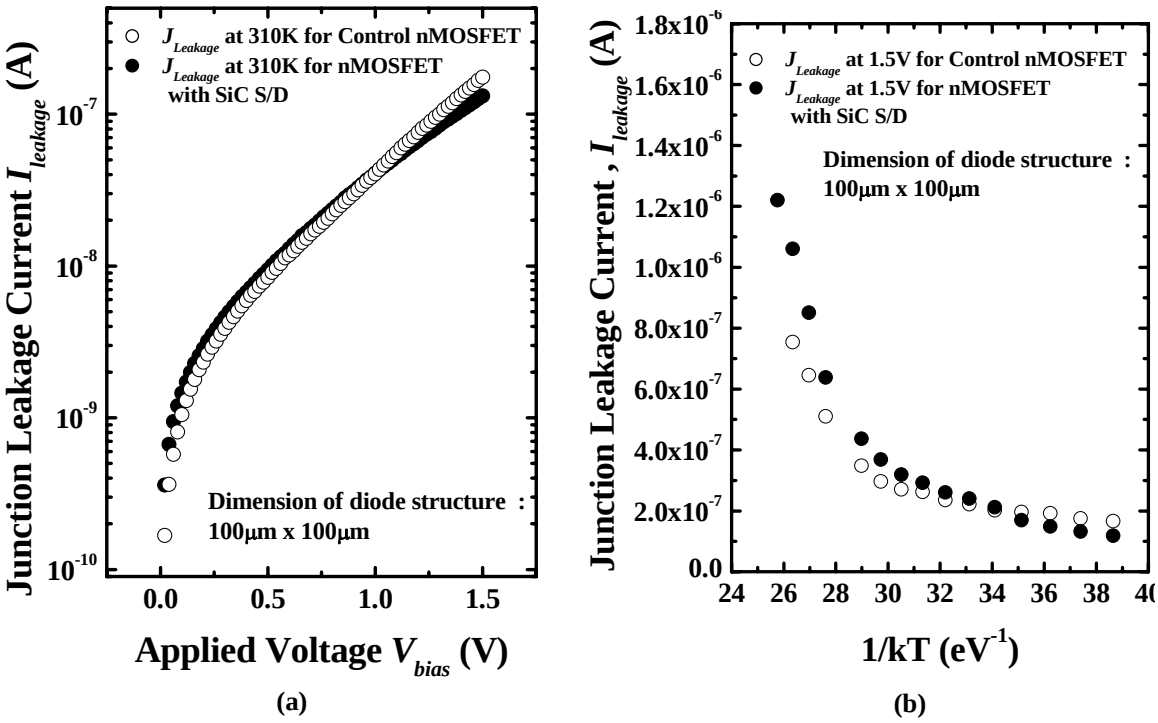


Figure 5.8 : (a) Comparable N+ diode junction leakage measurement at different voltage bias for both control and nMOSFET with SiC S/D. (b) Temperature dependence of junction leakage currents for both devices implies similar current leakage mechanisms.

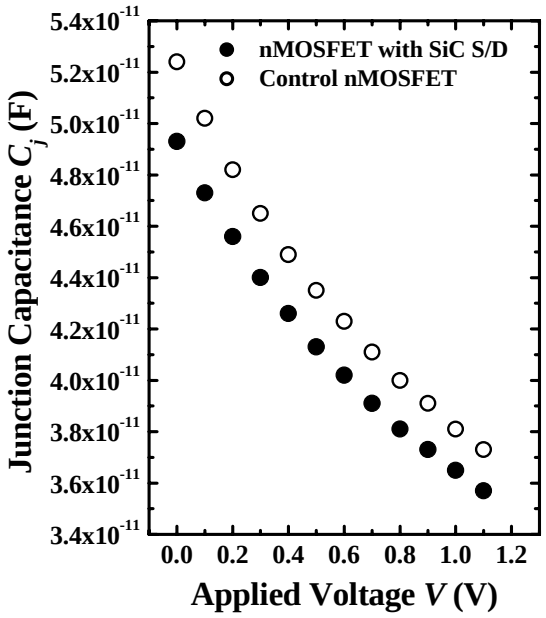


Figure 5.9 : Comparable junction capacitance between control and nMOSFETs with SiC S/D indicate full speed benefit feasibility from I_{Dsat} enhancement.

5.2 Strained nMOSFETs with SiC S/D on SOI Substrate

5.2.1 Background

In the earlier section, it has been demonstrated that the use of SiC in the S/D regions can be one effective way to induce beneficial strain in the Si channel to help improve the drive current of nMOSFETs on bulk Si substrates. On the other hand, silicon-on-insulator (SOI) substrates can help to further improve the device performance by reducing parasitic junction capacitance, improve short channel effects and prevent latch-up. In this section, we report the introduction of uniaxial tensile strain in thin body Silicon-on-Insulator (SOI) nMOSFETs by employing silicon-carbon (SiC or $Si_{1-y}C_y$) S/D regions. The $Si_{1-y}C_y$ material incorporates a low carbon mole fraction y (~0.01), but the

lattice mismatch between Si and $Si_{1-y}C_y$ is substantial. Due to this lattice mismatch, the SiC S/D regions act as stressors to induce a lateral tensile strain component ε_{xx} and a vertical compressive strain component ε_{zz} in the adjacent Si channel region. This leads to significant electron mobility and drive current enhancement.

5.2.2 Device Fabrication

Figure 5.10 shows the cross-section of transistor structures investigated in this work. The process sequence for device fabrication is depicted in Figure 5.11. 8-inch SOI substrates were used. Active regions were defined using a LOCOS isolation process. Threshold voltage V_t adjust and well implants were performed prior to atomic-layer deposition of HfAlO gate dielectric and sputter deposition of TaN metal gate. 248 nm optical lithography and photo-resist trimming were employed for gate patterning to reliably obtain sub-100 nm feature sizes. After metal gate etch, S/D extension (SDE) implant was done. This was followed by liner oxide deposition and SiN spacer formation. On one wafer, a Si recess etch of ~20 nm was performed followed by a selective epitaxial growth of undoped $Si_{1-y}C_y$ in the S/D regions using an Anelva UHV- CVD system. The carbon mole fraction y incorporated in the $Si_{1-y}C_y$ is 0.01. The resulting device, as illustrated in Figure 5.10 (b), comprises a SiC epitaxial layer that extends to a depth d below the gate dielectric interface. On another wafer, $Si_{1-y}C_y$ was selectively grown on unrecessed S/D regions [Figure 5.10 (c)]. The SiC S/D regions are raised on both wafers. Figure 5.10 (d) shows a SEM picture of the raised SiC S/D regions. On the control wafer, Si recess etch and selective epitaxy steps were not performed. All wafers underwent S/D ion implantation (As^+) and dopant activation using rapid thermal annealing at 950°C for

30 s. The S/D implant conditions for the control and strained-channel transistors were such that the dopant profiles in the S/D regions are similar, as estimated using TSUPREM process simulation.

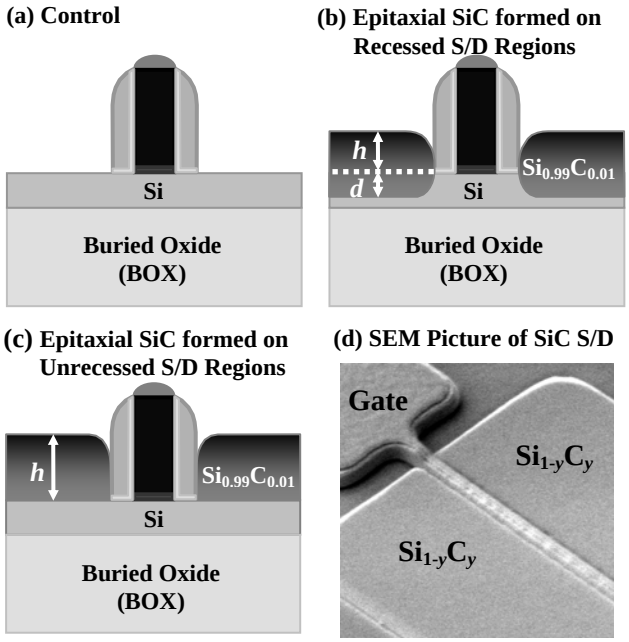


Figure 5.10 : Cross sections of (a) control SOI nMOSFET, and SOI nMOSFETs with silicon-carbon $Si_{1-y}C_y$ epitaxial layer formed on (b) recessed and (c) unrecessed source/drain (S/D) regions. (d) Picture of a SOI nMOSFET with raised $Si_{0.99}C_{0.01}$ S/D regions, as obtained using Scanning Electron Microscopy (SEM). A SiON hardmask caps the TaN gate during the selective epitaxy process. Good $Si_{0.99}C_{0.01}$ epitaxial growth selectivity is demonstrated.

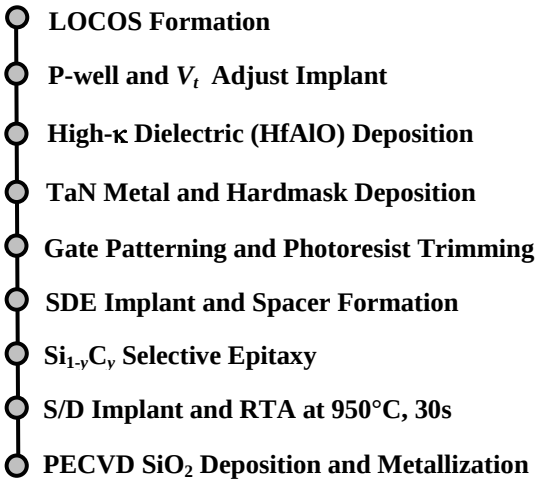


Figure 5.11 : Process sequence employed in the fabrication of SiC S/D transistors. TaN metal gate is used to eliminate the polysilicon gate depletion effect

A cross-section TEM image of a fabricated SOI nMOSFET with raised SiC S/D regions, TaN metal gate, and high-permittivity HfAlO gate dielectric is shown in Figure 5.12 (a). High-resolution TEM image [Figure 5.12 (b)] clearly shows pseudomorphic epitaxial growth of SiC on Si. Fast Fourier transform (FFT) diffractogram reveals good crystalline quality of SiC region after the S/D implant and dopants activation [Figure 5.12 (b) inset]. Figure 5.13 plots the high resolution XRD spectra which shows the successful formation of SiC film with 1% substitutional carbon concentration. (004) and (224) reciprocal space maps reveal perfect alignment of SiC and Si intensity peaks, illustrating lattice alignment along the heterojunction as a result of the pseudomorphic epitaxial growth (Figure 5.14).

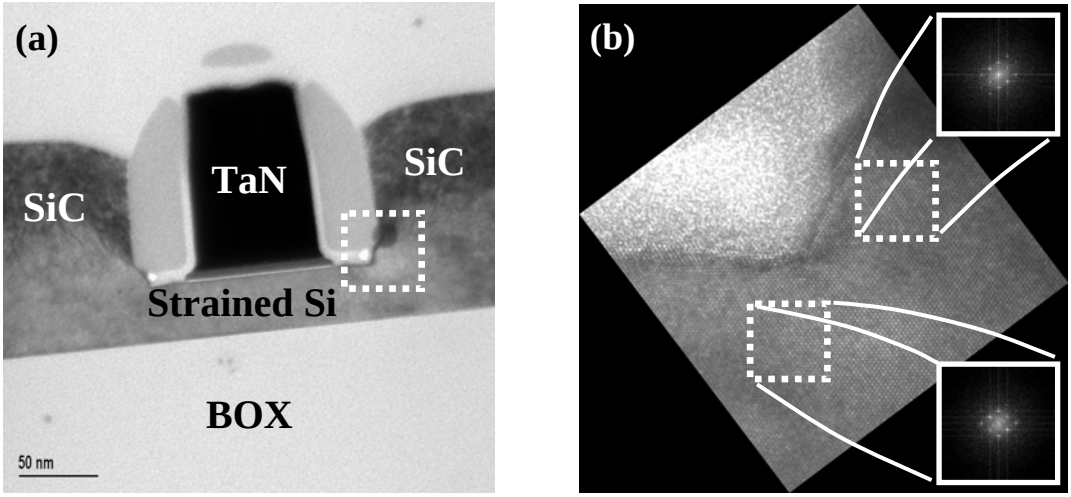


Figure 5.12 : (a) Transmission electron microscopy (TEM) image of SOI transistor featuring TaN metal gate, high-k gate dielectric, and $Si_{0.99}C_{0.01}$ S/D regions. (b) High-resolution TEM image and Fast Fourier transform (FFT) diffractograms, revealing the excellent crystalline quality of the $Si_{0.99}C_{0.01}$ region after S/D implant and dopant activation at 950°C for 30 s.

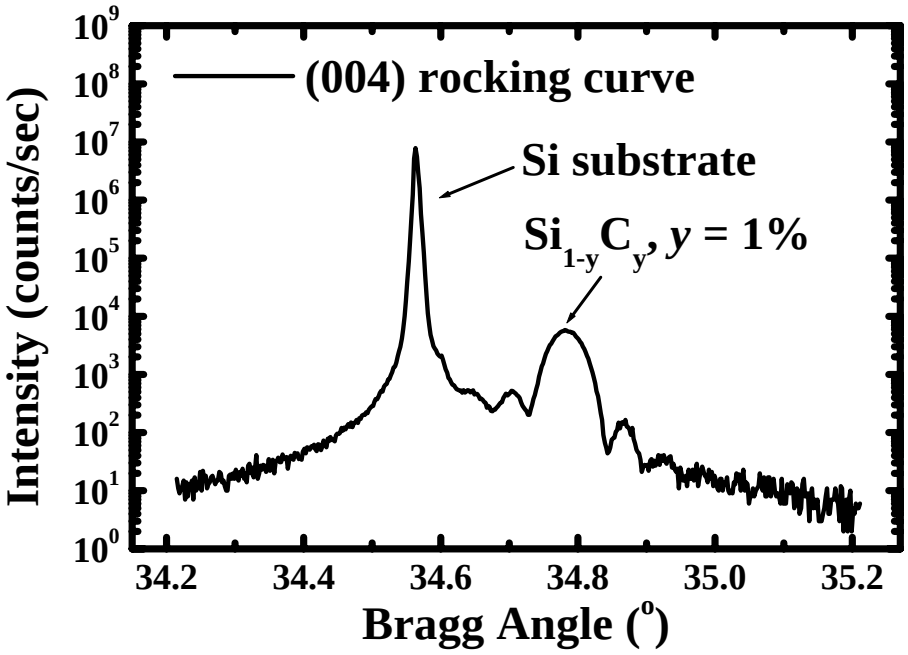


Figure 5.13 : High resolution XRD spectra shows excellent crystalline quality of the SiC film on Si with 1% substitutional carbon.

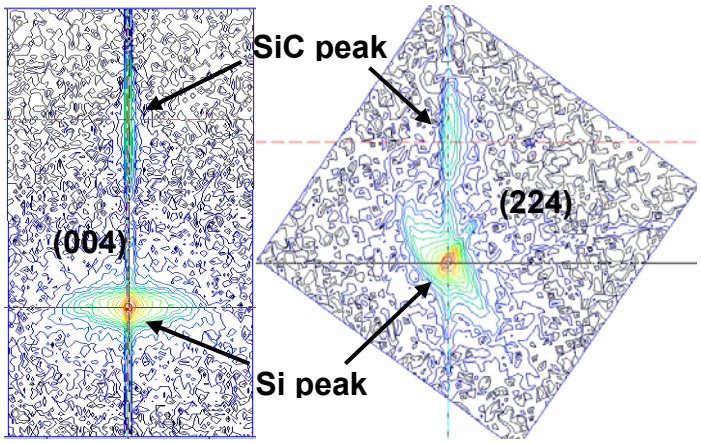


Figure 5.14 : (004) and (224) reciprocal space maps show perfect alignment between the SiC and Si peaks, indicating pseudomorphic epitaxial growth.

5.2.3 Electrical Characterization

A. I_{Dsat} Dependence on Gate Length L_G and Device Width W

The I_{DS}-V_{DS} characteristics of a control SOI transistor and SOI transistor with SiC S/D regions are compared in Figure 5.15 (a). A 25% enhancement in drain current I_{DS} over a control device at a gate over-drive (V_G - V_t) of 1.0 V is achieved for a 90 nm gate length nMOSFET with raised SiC regions formed on recessed S/D (d = 20 nm). I_{Dsat} enhancement is higher when the SiC is formed on recessed S/D regions than on unrecessed S/D regions (Figure 5.15 (a) and (b)). This could be attributed to the enhanced strain effects due to the closer proximity of the SiC S/D regions to the Si channel.

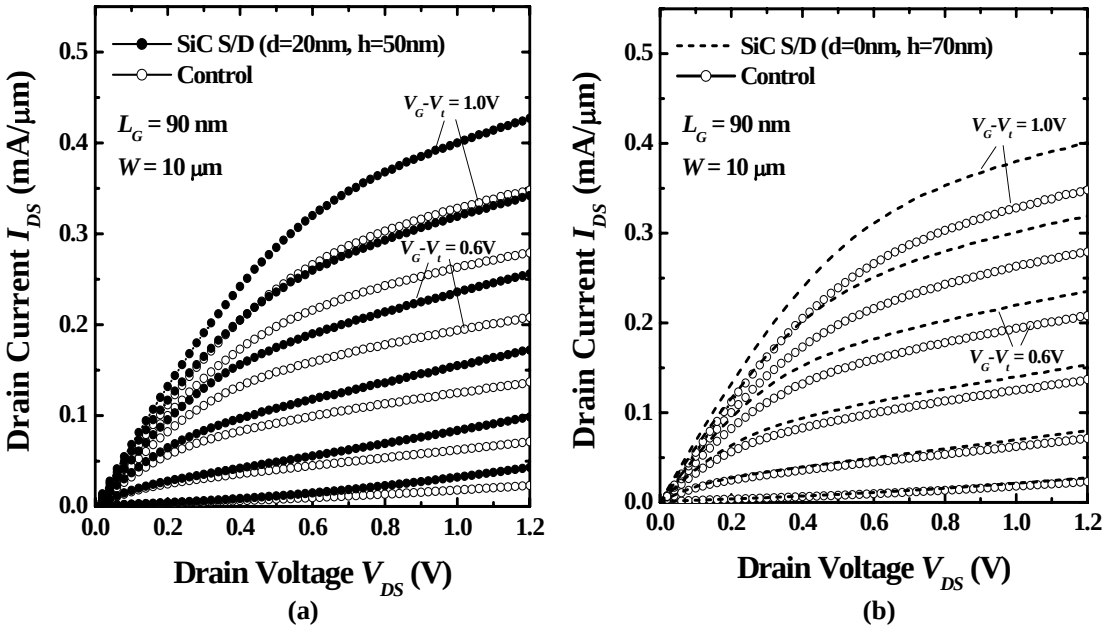


Figure 5.15 : (a) I_{DS}-V_{DS} characteristics for 90 nm gate length nMOSFET with SiC selectively grown on recessed S/D regions. Drive current I_{Dsat} enhancement of 25% is observed (b) nMOSFET with SiC S/D formed on unrecessed regions shows larger I_{Dsat} as compared to the control transistor.

Figure 5.16 (a) shows the I_{DS}-V_{GS} characteristics of both control and SiC S/D devices. It is noted that arsenic diffusion during the dopant activation process is enhanced in SiC [57],

and this results in a slightly larger DIBL in transistors with SiC stressors formed on recessed S/D regions [Figure 5.16 (a)]. The transconductance G_m of SiC S/D transistor is ~21% higher than a control transistor [Figure 5.16 (b)]. The I_{Dsat}-L_G plot [Figure 5.17 (a)] shows continual improvement in I_{Dsat} with decreasing L_G down to 70 nm. The measured I_{Dsat} enhancement improves with increasing device width [Figure 5.17 (b)]. This can be due to the larger volume of SiC S/D stressors for straining the Si channel when the device width is increased.

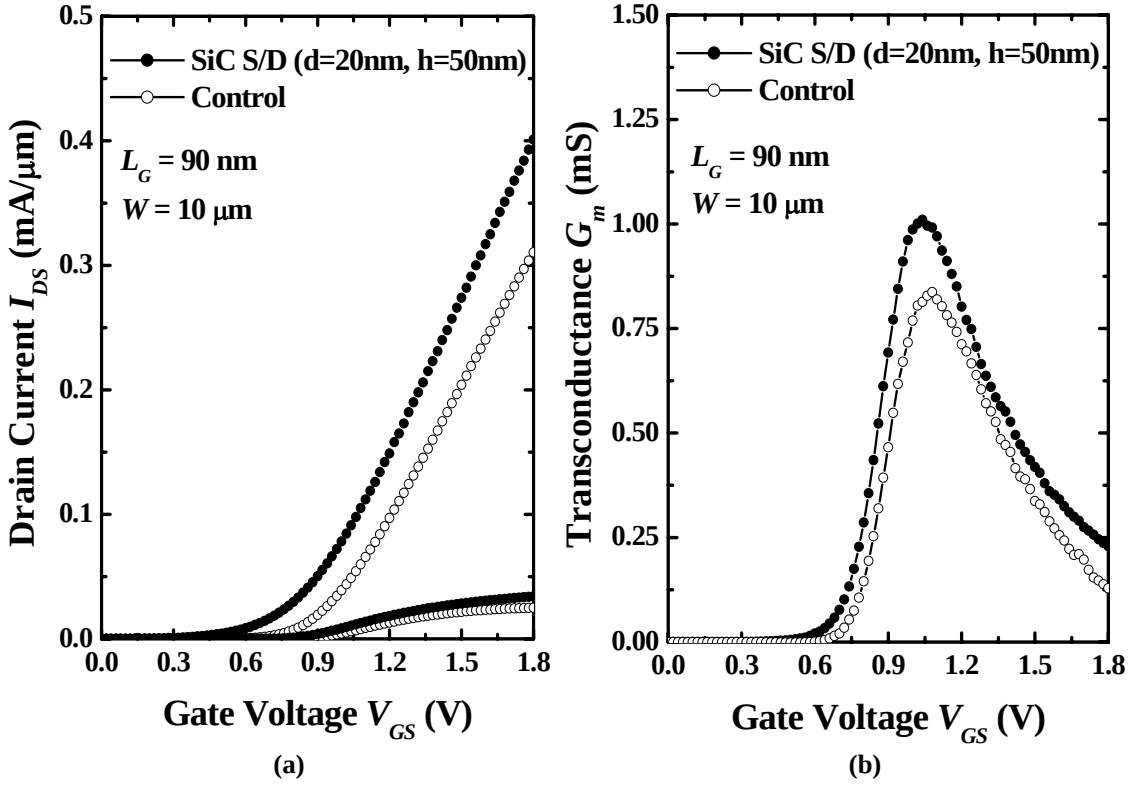


Figure 5.16 : (a) The I_{DS}-V_{GS} characteristics of a 90 nm gate length SiC S/D nMOSFET shows higher linear and saturation drive current over the control SOI transistor. (b) Transconductance G_m of SiC S/D nMOSFET shows ~21% improvement over the unstrained control device.

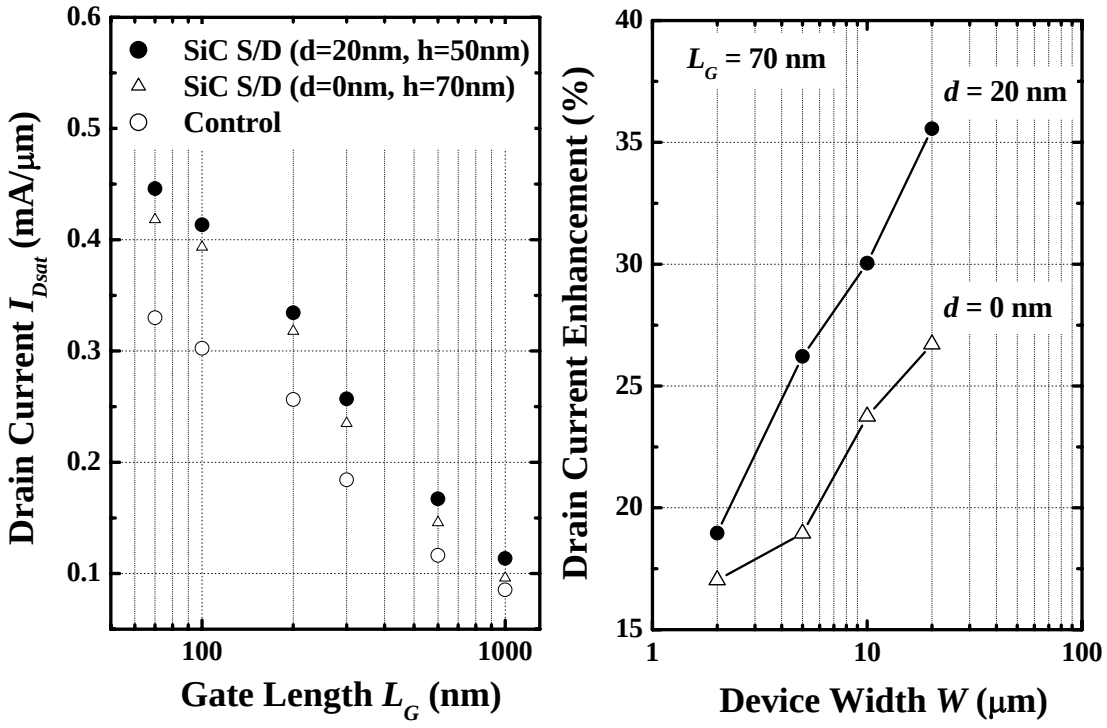


Figure 5.17 : (a) Drive current I_{Dsat} enhancement increases with decreasing gate length L_G. Raised SiC formed on recessed S/D regions shows a higher I_{Dsat} improvement. (b) Increasing device width W leads to a higher drain current enhancement.

B. I_{Dsat} Dependence on Channel Orientation

The dependence of I_{Dsat} on channel orientation is investigated next. A plan view of a transistor with an arbitrary channel orientation on the (001) Si surface is outlined in Figure 5.18, where the channel orientation θ is taken with reference to the [110] direction. The I_{Dsat} of the unstrained control transistors is observed to be independent of the channel orientation [Figure 5.19 (a)]. On the other hand, the drive current of a uniaxial tensile strained nMOSFET is strongly dependent on the channel direction. A nMOSFET with the [010] channel direction and with uniaxial tensile strain along the S-to-D direction has the highest I_{Dsat} enhancement over a control device with the same channel orientation [Figure 5.19 (a)].

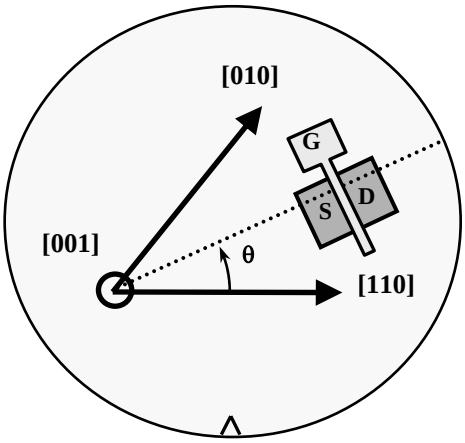


Figure 5.18 : The plan view of a nMOSFET formed on a (001) surface with an arbitrary source-to-drain or channel orientation θ. When θ = 0º, the channel orientation is along a [110] crystal direction.

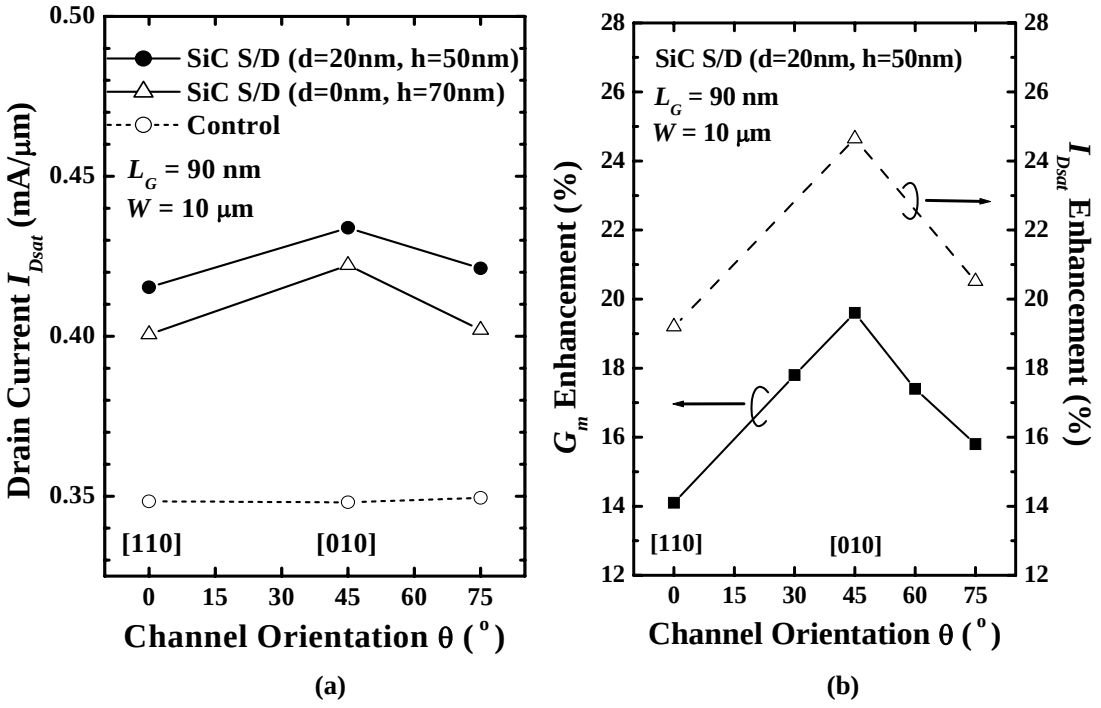


Figure 5.19 : (a) While the I_{Dsat} of the control nMOSFET is independent of channel orientation, a uniaxial strained nMOSFET with SiC S/D has the highest I_{Dsat} when its channel direction is oriented along the [010] crystal direction. (b) Both I_{Dsat} and G_m improvement due to uniaxial tensile strain are the largest for the [010]-oriented nMOSFET, in agreement with piezoresistance properties of bulk Si.

Figure 5.20 illustrates the effect of uniaxial tensile strain in the [110] and [010] directions on the conduction band valleys at the Δ point. Strain lifts the six-fold degeneracy at the conduction band by lowering the two-fold perpendicular valleys (Δ_2) with respect to the four-fold in-plane valleys (Δ_4). This results in preferential electron re-population in the lower energy Δ_2 valleys where the in-plane transport mass is lower. It is interesting to note that a uniaxial tensile strain along [010] channel direction leads to anisotropic electron population among the Δ_4 valleys. Additional electron population in two of the four Δ_4 valleys results in smaller in-plane transport mass, and could lead to larger I_{Dsat} enhancement [27]. Figure 5.19 (b) depicts the percentage enhancement in the transconductance and drive current as a function of channel orientations. Both G_m and I_{Dsat} enhancement are largest along the [010] channel direction. This is also in good qualitative agreement with reported piezoresistance coefficients for Si [51]. The fractional change in resistance of n-type bulk Si due to mechanical stress σ is given by [58].

$$\frac{\Delta\rho}{\rho} \approx \left|\pi_l \sigma_l + \pi_t \sigma_t\right| \tag{5.1}$$

where π_l and π_t are the longitudinal and transverse piezoresistance coefficients, respectively (Figure 5.21), and σ_l and σ_t are the longitudinal and transverse stress components, respectively. For a given longitudinal tensile stress (positive σ_l), the largest reduction in resistance or largest enhancement of electron mobility is expected when the carrier conduction is in the [010] direction [Figure 5.21]. This is consistent with the experimental observation in Figure 5.19 (b).

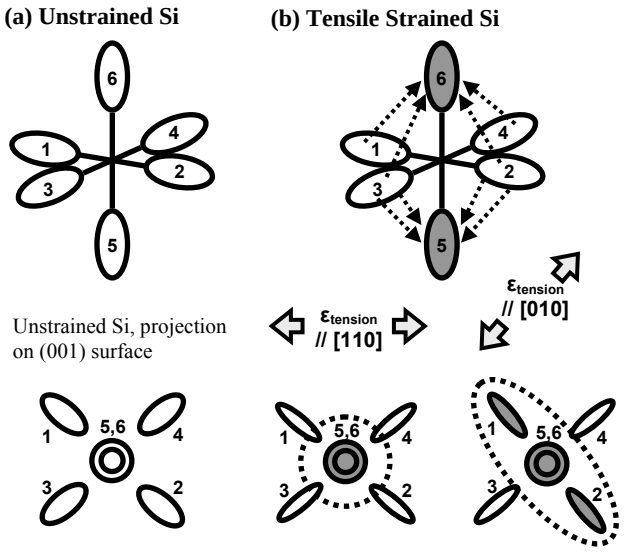


Figure 5.20 : (a) Six-fold degenerate conduction band valleys in unstrained Si. (b) In strained Si with uniaxial tensile strain along [110], preferential electron population in valleys 5 and 6 (in gray, top and bottom left) occurs. When uniaxial tensile strain is applied along [010] (bottom right), anisotropic population of Δ_4 valleys could additionally lead to mobility enhancement [27].

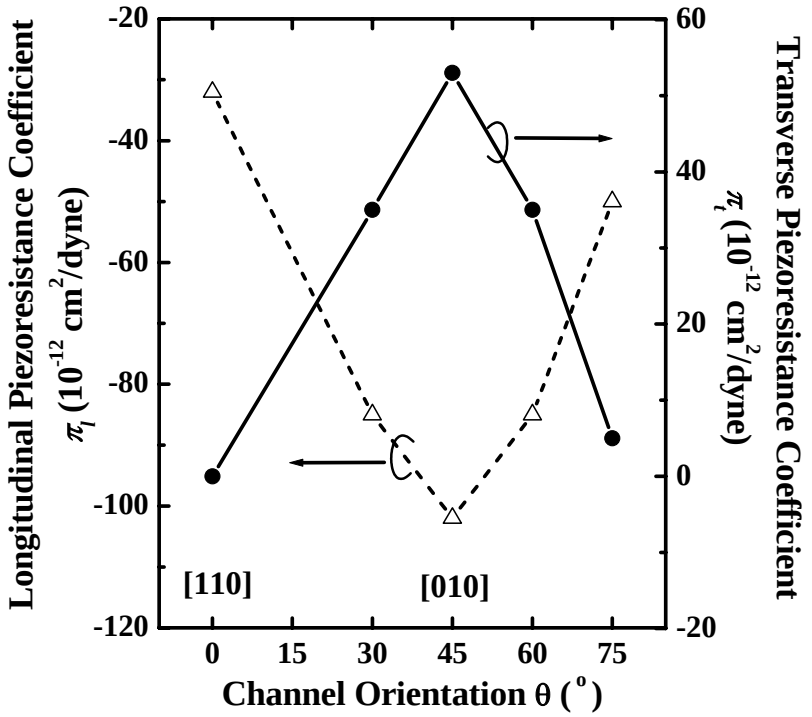


Figure 5.21 : The longitudinal piezoresistance coefficient π_l is the most negative in the [010] direction (or $\theta = 45°$). Applying a tensile longitudinal stress in the [010] direction will lead to the largest reduction in resistance, compared to other directions.

C. Dual Stressors Effect on I_{Dsat} and Dependence on Channel Orientation

Next, similar SOI nMOSFETs with SiC S/D are again fabricated. But this time, an additional tensile stress SiN etch-stop-layer (ESL) was integrated together with SiC source/drain (S/D). Recently, high-stress silicon nitride (SiN) ESL has been widely adopted to induce uniaxial tensile strain in nMOSFETs to boost electron mobility [15], [16]. In this section, we further report on the integration of both SiC source/drain (S/D) and tensile stress SiN ESL stressors to examine the strain effects of the dual stressors on drive current and its dependence on channel orientation. A TEM image of the fabricated strained SOI nMOSFETs with SiC S/D and tensile stress ESL is as shown in Figure 5.22.

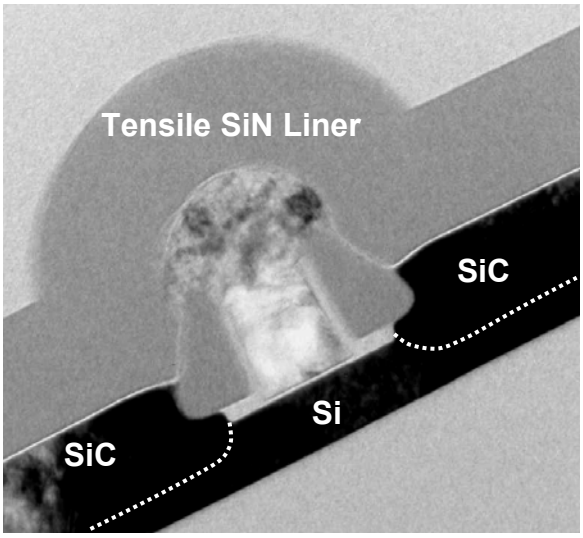


Figure 5.22 : TEM image of a SOI nMOSFET with SiC S/D and tensile stress etch-stop-layer ESL.

Figure 5.23 shows the I_{DS}-V_{DS} characteristics of 50 nm gate length transistors with the [110] and [010] channel orientations. For both orientations, the use of SiC S/D increases the I_{Dsat} significantly, and the addition of a tensile stress SiN ESL improves I_{Dsat} further. A [110]-oriented nMOSFET with dual stressors demonstrates an I_{Dsat} enhancement of 46% at a gate over-drive of 1.0 V (Figure 5.24), compared with a control

device of the same orientation. For the [010]-oriented n-MOSFET, SiC S/D and SiN ESL improves the I_{Dsat} by 55%.

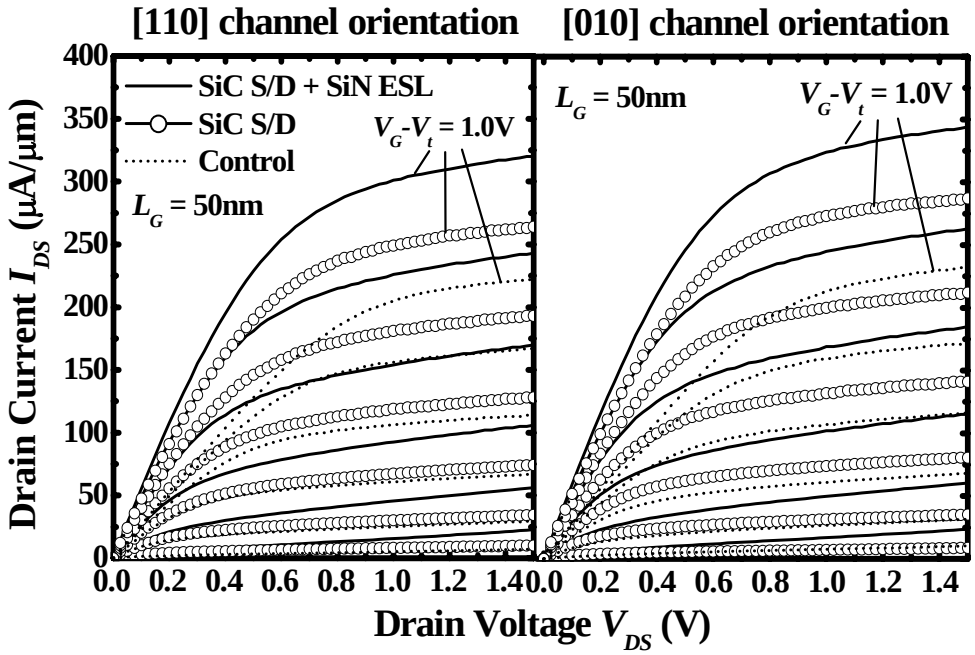


Figure 5.23 : I_{DS}-V_{DS} characteristics of nMOSFETs with SiC S/D and tensile stress SiN ESL shows 55% enhancement in I_{Dsat} at a gate overdrive of 1V.

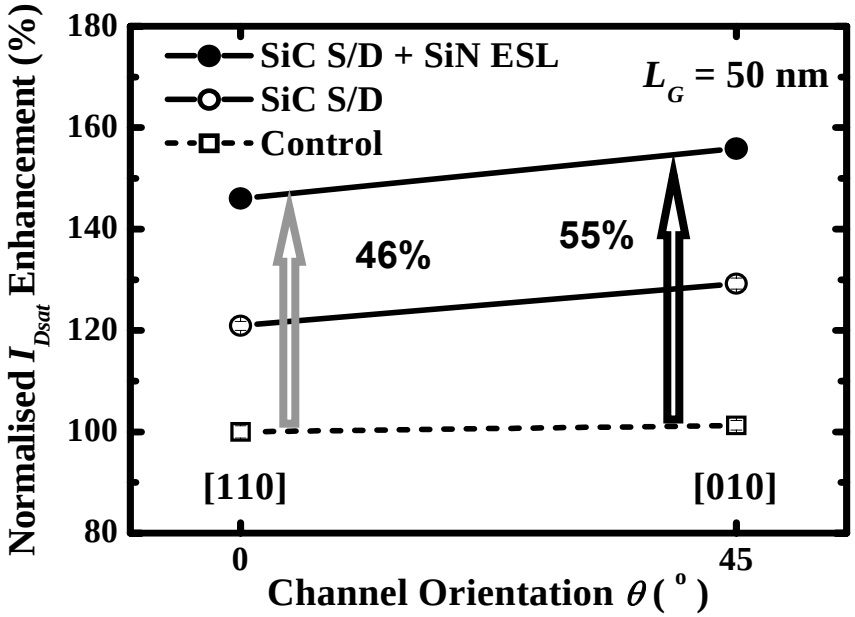


Figure 5.24 : Significant I_{Dsat} enhancement contributed by SiC S/D and SiN ESL, with highest improvement observed for [010]-oriented nMOSFETs.

Figure 5.25 summarizes the I_{Dsat} data for devices with 5 different channel orientations, including [110] (θ = 0°) and [010] (θ = 45°). The I_{Dsat} enhancement due to the uniaxial tensile strain introduced by the SiC S/D or the SiN ESL is the largest for n-MOSFETs with the [010] channel orientation (θ = 45°). This is attributed to the anisotropic electron population at the Δ_4 valley which results in smaller conductivity mass and thus higher mobility enhancement [27], [59]. Figure 5.26 shows the saturation transconductance G_m of strained and control devices. For both [110] and [010] oriented transistors, the percentage maximum G_m enhancement is highest when dual stressors are employed (Figure 5.27).

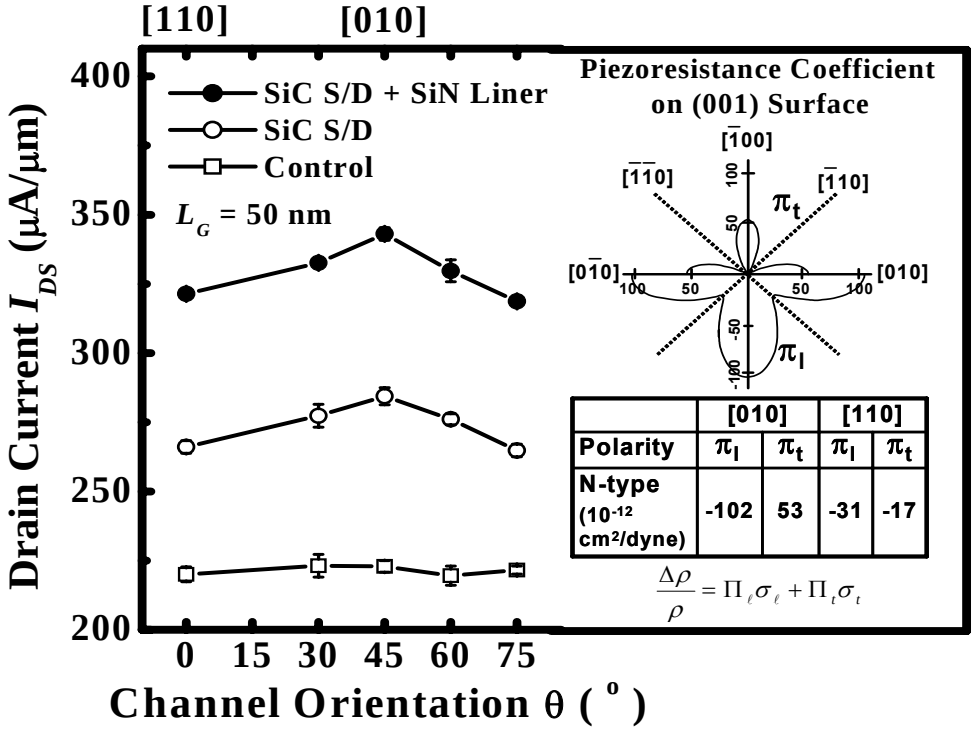


Figure 5.25 : Drive current I_{Dsat} of SiC S/D device shows strong dependence on channel orientations, consistent with the directional dependence of piezoresistance coefficients.

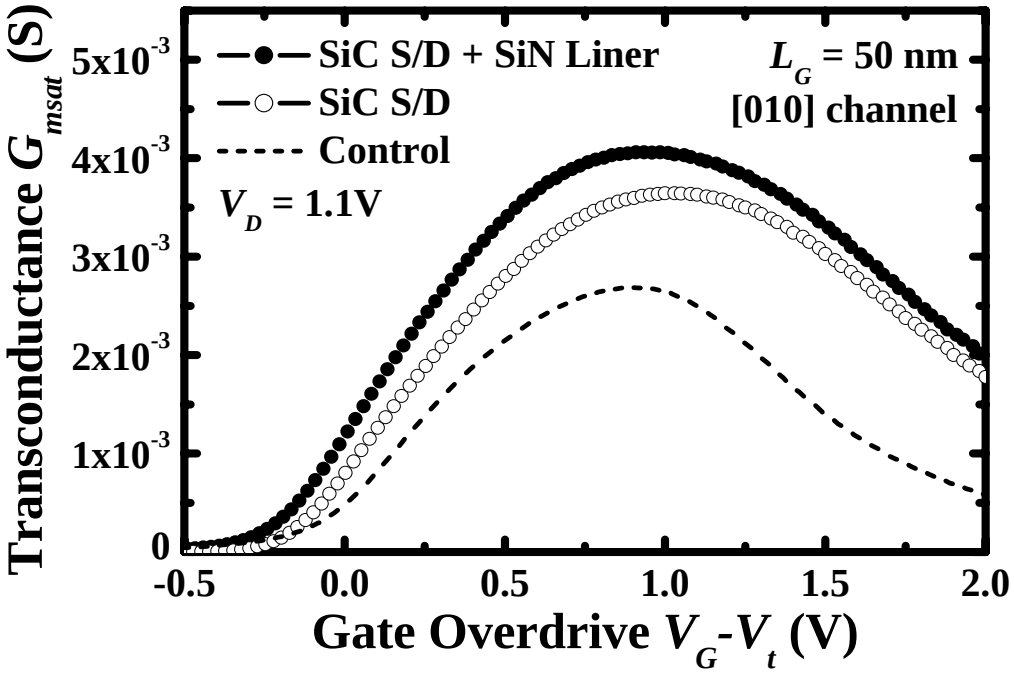


Figure 5.26 : Significant increase in G_m of 69% is observed for SiC S/D and SiN liner nMOSFETs over control devices.

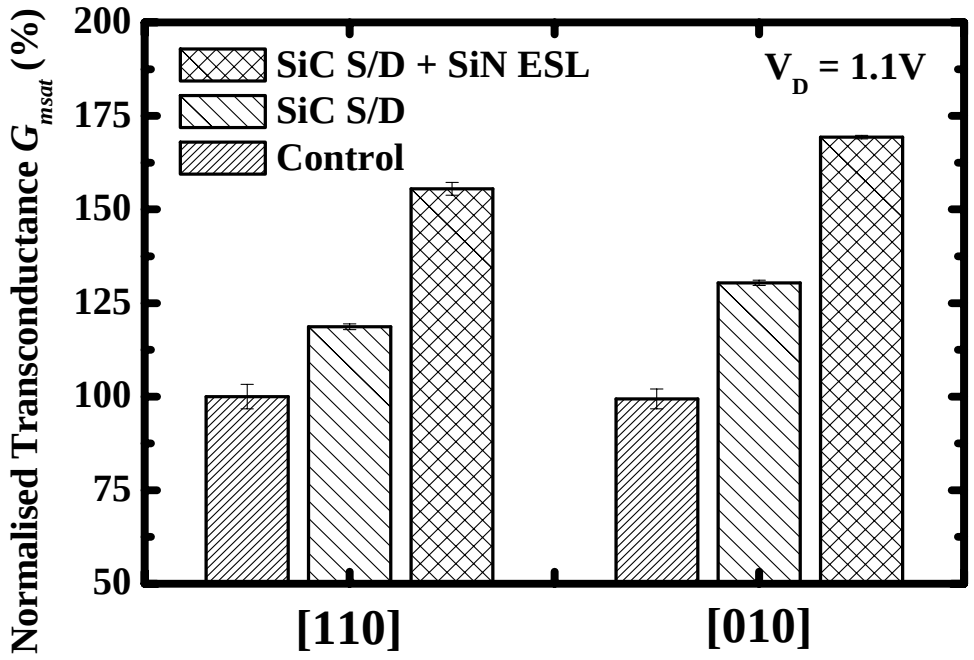


Figure 5.27 : Strained devices oriented along [010] channel show higher maximum G_{msat} enhancement than those oriented along [110] channel direction

Figure 5.28 plots the series resistance of control and SiC S/D devices extracted based on extrapolation of total resistance at high gate bias and low V_{DS} of 50 mV (inset). With reference to the inset in Figure 5.28, at high gate-overdrive, the channel resistance is assumed to be negligible, with the overall source-to-drain resistance mainly contributed by resistance at the source and drain side. It is observed that SiC S/D device shows a 10% reduction in series resistance R_{series} due to the raised source/drain. The slight reduction in R_{series} accounts for ~2% I_{Dsat} enhancement observed in the strained nMOSFETs. Comparable gate leakage current densities were observed for all devices (Figure 5.29), showing no degradation in gate oxide quality in the presence of strain.

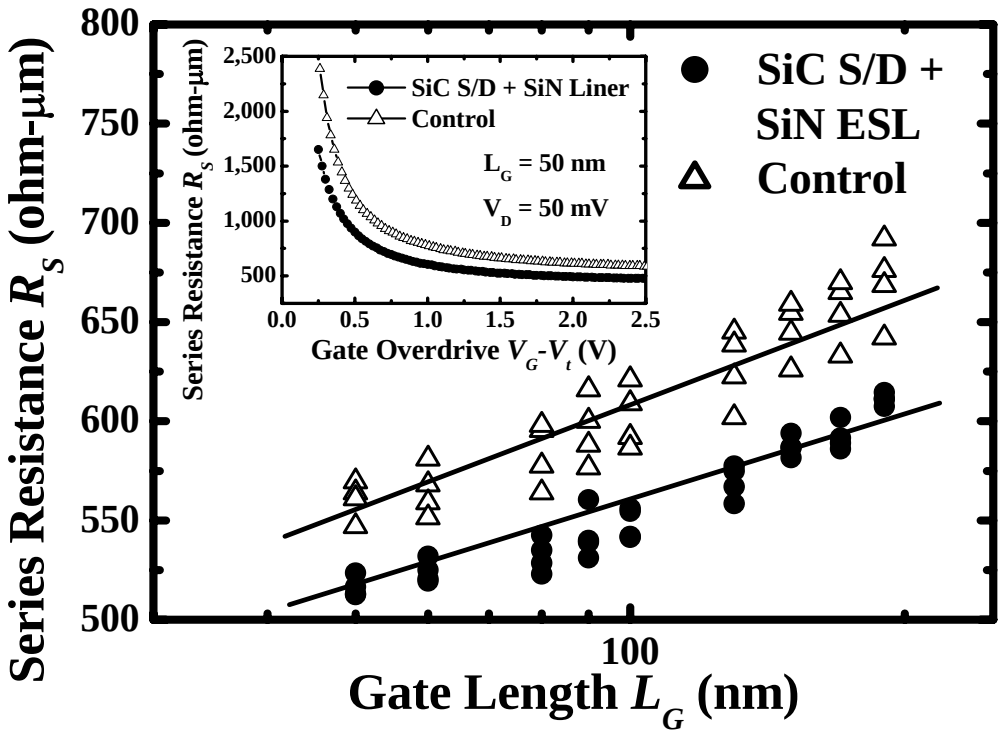


Figure 5.28 : Series resistance extraction at high gate bias shows 10% improvement in R_{series} for strained device due to the raised S/D.

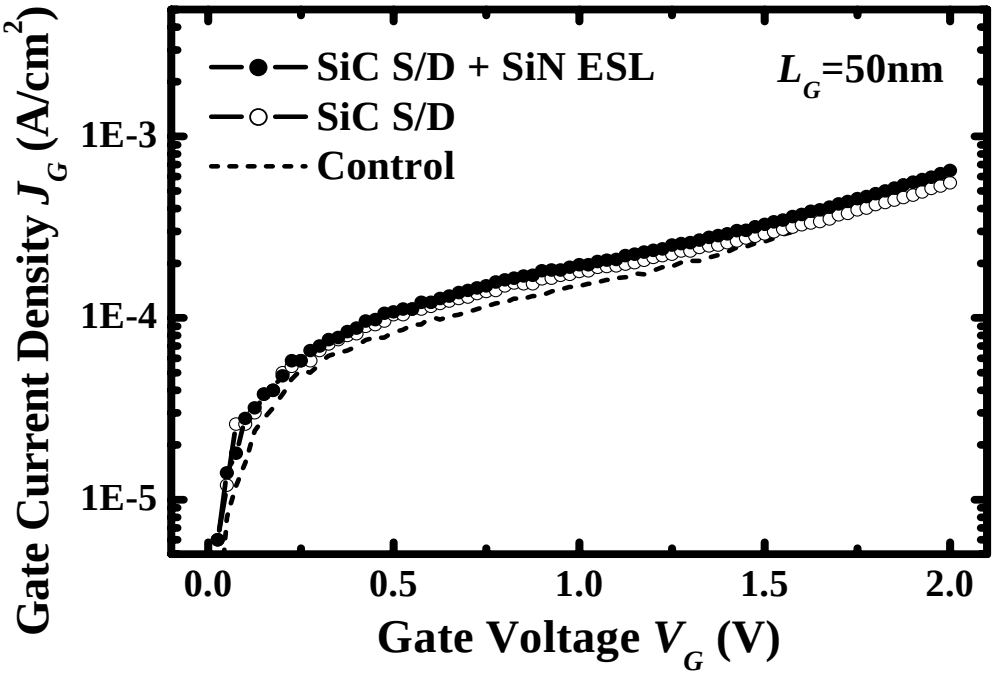


Figure 5.29 : Comparable gate leakage characteristics of both strained and control devices, showing no strain induced degradation of gate oxide quality.

5.3 Summary

A novel strained-Si nMOSFET comprising SiC S/D regions was demonstrated. The strained device was first demonstrated on bulk Si substrate, featuring TaN metal gate with HfAlO high-k dielectric. Through stress simulations and HRTEM analysis, we verified that the SiC regions act as stressors, giving rise to lateral tensile strain and vertical compressive strain in the channel to enhance electron mobility. Significant enhancement in drive current was observed. This could also be attributed to the SiC–strained-Si heterojunction which enables increased electron injection velocity at the source end. Both effects are expected to become more prominent with device scaling, making this device structure attractive for future high-speed ballistic transistors. Selective epitaxial growth of SiC stressors enables source and drain regions to be raised, which reduces the series

resistance and further improve the drive current. This novel strained nMOSFET with SiC S/D was next implemented on SOI substrate to the its desirable advantages like suppression of short channel effects, reduced junction capacitance, lower off-state leakages and elimination of latch-up. In addition, the drive current of tensile strained SiC S/D nMOSFET shows dependence on device width and channel orientation. Additional tensile ESL was then integrated to investigate the multiple-stressors effect on the electrical performance of these strained nMOSFETs with SiC S/D on SOI substrate. The next chapter explores strained pMOSFETs with SiGe S/D on SOI substrate, complementary to the strained nMOSFET with SiC S/D regions discussed in this chapter.

CHAPTER 6

Strained pMOSFETs with Ge Condensed S/D Regions

6.1 Strained SOI pMOSFETs with Condensed SiGe S/D

6.1.1 Background

Strain-induced effects are being aggressively exploited for improving carrier mobility and transistor drive current I_{Dsat} in addition to device scaling [9]-[17], [41], [45] – [48]. In bulk pMOSFETs, SiGe S/D stressors induce uniaxial compressive strain in the Si channel and enhance hole mobility [17]. This approach employs the additional steps of a Si recess etch in the S/D regions, followed by a selective epitaxy of SiGe. Strained SOI pMOSFETs with SiGe S/D were also reported [61]. Simulations indicate that embedding SiGe in the S/D regions leads to a larger compressive stress, showing that the S/D recess etch prior to SiGe S/D epitaxy is necessary (Figure 6.1). However, as the SOI thickness is further scaled down, implementation of the SiGe S/D structure becomes more challenging due to difficulties in controlling the recess etch depth and in performing selective epitaxy on an ultra-thin Si layer.

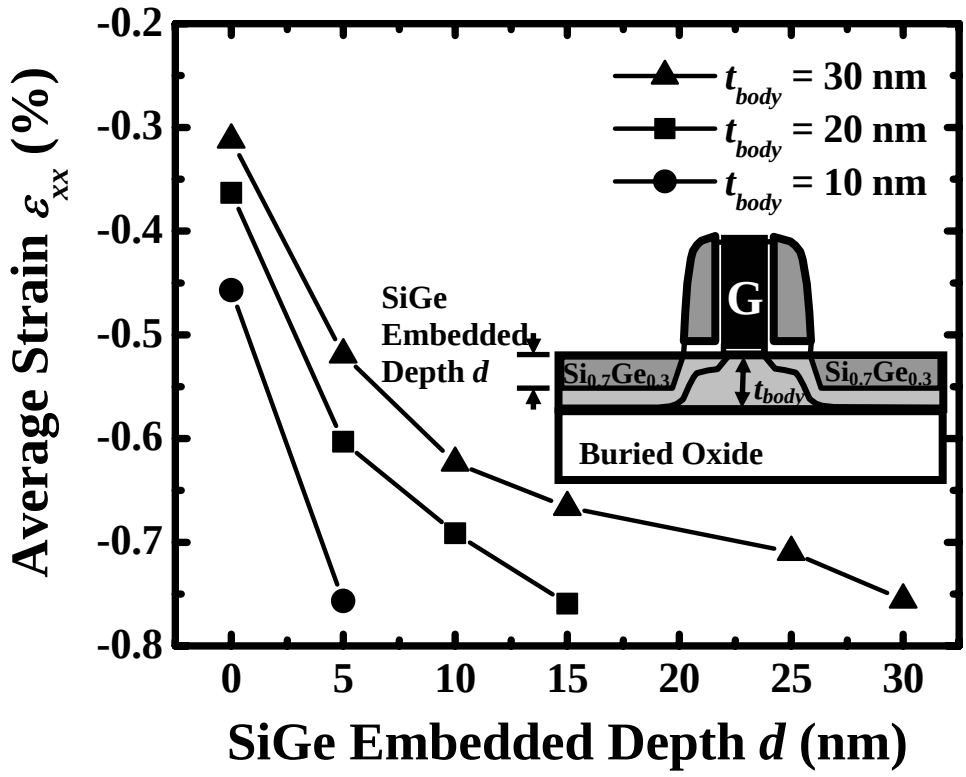


Figure 6.1 : Stress simulation results using TAURUS process simulator. The average lateral strain ε_{xx} (calculated from SiGe source-end to the centre of the transistor channel, and at a depth of 5 nm below the Si/SiO_2 interface) as a function of SiGe embedded depth is plotted for various body thicknesses. A higher average strain in the Si channel can be achieved with deeper SiGe embedded depth and thinner body thickness. The inset shows the transistor structure adopted in the simulation.

In this chapter, we report a new approach of fabricating uniaxial compressive-strained pMOSFETs with SiGe S/D without the need for a recess etch. SiGe is selectively grown on unrecessed S/D regions, and subject to local condensation [62] to drive Ge into the S/D regions (Figure 6.2). The final device structure is shown in Figure 6.2 (c). In addition, this technique could be used to increase the Ge content in the S/D regions. This approach is promising for high-performance transistors, especially ultra-thin body SOI transistors, due to the elimination of a recess etch step and the ease of tunability of the Ge content without excessive thermal budget.

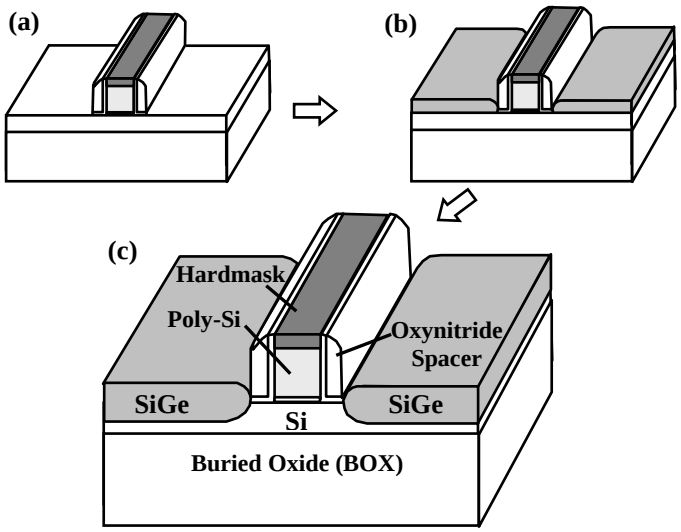


Figure 6.2 : Schematic showing the formation of SiGe S/D stressors. (a) After forming the gate stack and spacers in a conventional CMOS process, (b) SiGe is selectively grown on the S/D regions. Oxidation or Germanium condensation is then performed to drive Ge into the S/D regions to give the final structure as shown in (c). Si selectively oxidizes in Ge condensation process, driving Ge inside S/D and increasing Ge percentage.

6.1.2 Device Fabrication

The device fabrication process is depicted in Figure 6.3. After isolation and well formation, threshold voltage *Vt* adjust implant was performed. This was followed by thermal oxidation to form 3 nm SiO_2 gate dielectric and poly-Si gate deposition. The gate stack was covered by a SiO_2 hardmask. Gate patterning employed 248 nm optical lithography and photo-resist trimming to reliably obtain sub-100 nm feature sizes. After poly-Si gate etch, a 40 nm silicon oxynitride spacer was formed. This was followed by a selective epitaxial growth (SEG) of $Si_{0.7}Ge_{0.3}$ on the S/D regions. The $Si_{0.7}Ge_{0.3}$ S/D regions were subjected to dry oxidation at 950°C to drive Ge into the S/D regions. Figure 6.4 shows a cross-section TEM image of a MOSFET structure after Ge condensation. On a control wafer, selective Si epitaxy was performed to slightly raise the source and drain regions to maintain the same device structure as the transistor with condensed SiGe S/D.

S/D implantation and dopant activation (RTA at 900°C for 150 s) were then performed on all devices. SiO_2 deposition, contact hole etch, and metallization were performed to complete the device fabrication.

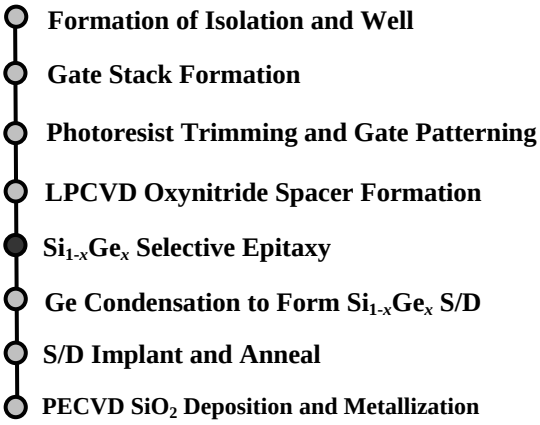


Figure 6.3 : Device fabrication sequence, showing the insertion of a SiGe selective epitaxy step and a Ge condensation step in a standard process flow.

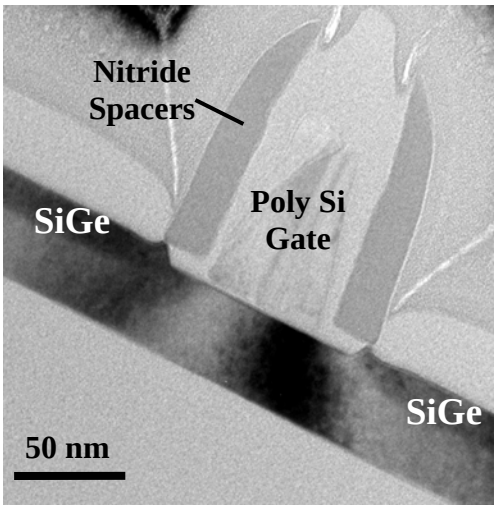


Figure 6.4 : TEM image of a transistor structure after Ge condensation. The Ge was driven into the S/D regions during the Ge condensation process.

6.1.3 Electrical Characteristics

Figure 6.5 (a) plots the I_{DS}-V_{DS} characteristics of the control and strained pMOSFETs with a gate length of 90 nm. Significant drive current I_{Dsat} enhancement of about 37% is achieved in the strained transistor over a control device at a gate overdrive (V_{GS}-V_t) of 1.0 V. Figure 6.5 inset shows the I_{DS}-V_{GS} characteristics of both control and strained pMOSFET with SiGe S/D stressors. Both control and strained devices exhibit comparable off-state leakage I_{off}, DIBL, and subthreshold swing, showing no degradation in subthreshold characteristics with drive current enhancement. The significant I_{Dsat}

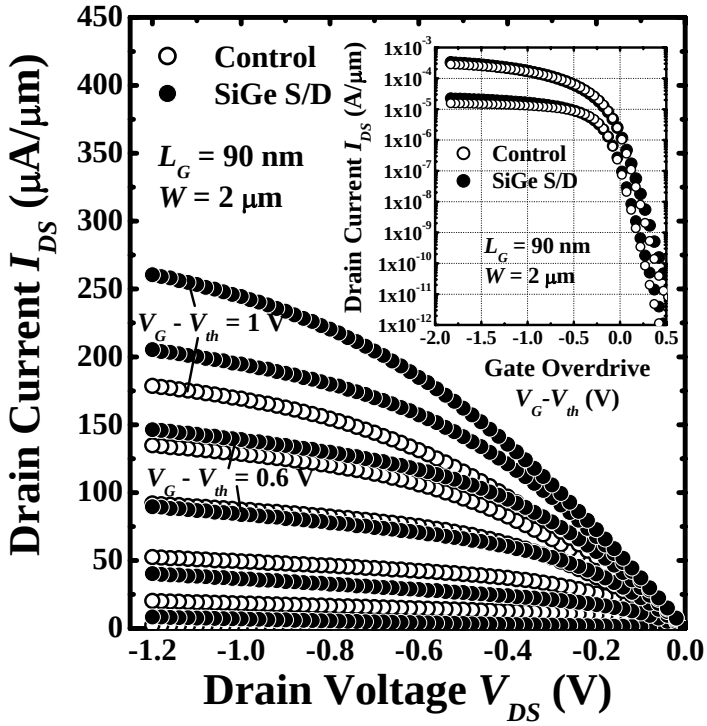


Figure 6.5 : I_{DS}-V_{DS} characteristics of strained pMOSFET with condensed SiGe S/D regions at a gate length of 90 nm, showing significant 37% drive current I_{Dsat} enhancement over the control pMOSFET. Inset plots the subthreshold characteristics for a pair of closely-matched strained and control devices with comparable off-state leakage I_{off}, DIBL, and subthreshold swing

enhancement can be attributed to the lateral compressive strain induced in the transistor channel as a result of the lattice mismatch between the SiGe stressors and Si, thereby modifying the electronic band structures. Uniaxial compressive strain lifts the degeneracy of the heavy hole (HH) and light hole (LH) sub-bands at the Γ point and increases the inter-band energy splitting, $\Delta_{E1\text{-}E2}$, (Figure 6.6), contributing to the suppression of optical phonon scattering. In addition, strain modifies the curvature of the topmost energy sub-band and reduces the hole effective mass (Figure 6.6). This in turn gives rise to significant enhancement in drive current I_{Dsat} as illustrated in Figure 6.5. However, strain effects only accounts for a portion of the I_{Dsat} enhancement. A fraction

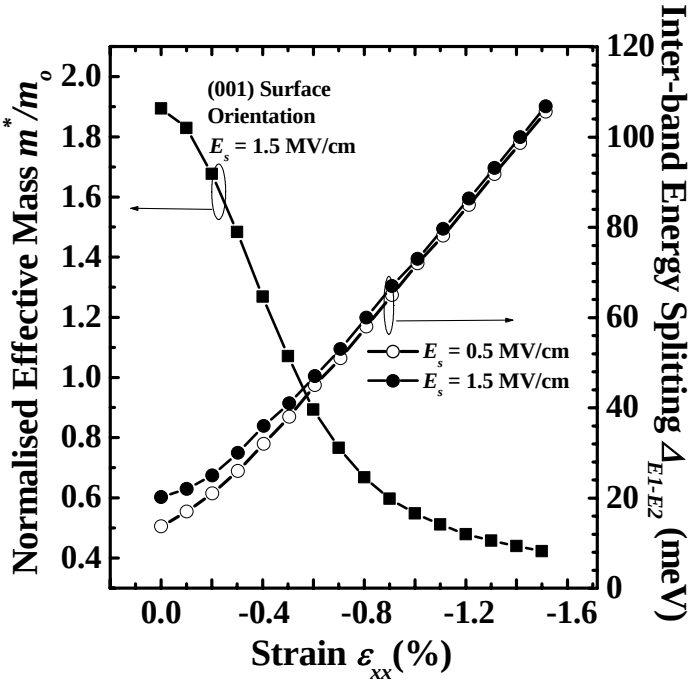


Figure 6.6 : Inter-band energy splitting increases with increasing strain ε_{xx} (open and closed circle symbols). Increasing uniaxial compressive strain ε_{xx} along the [110] channel direction reduces the hole effective mass in the same direction (square symbols). The simulation results were obtained using k·p effective mass theory, employing a 6×6 Luttinger-Kohn Hamiltonian with strain terms included. Hole quantization effects in the Si inversion layer of p-MOSFETs was modeled using a triangular well approximation. The vertical electric field at the Si surface is given by E_s.

of this current enhancement is attributed to the lower series resistance in the strained pMOSFETs. This occurs, even with raised Si S/D for the control device, because of the better activation of boron atoms in the presence of Ge. The inset in Figure 6.7 plots the R_S-V_{GS} characteristics of both devices at low V_{DS}. At high gate-overdrive, the channel resistance is assumed to be negligible, the overall source-to-drain resistance is mainly contributed by resistance at the source and drain side [60]. About 45% improvement in series resistance is observed for the strained device with condensed SiGe S/D regions. Upon correction of potential drop as a result of the series resistance, at the gate and the source-to-drain end, the enhancement in drive current I_{Dsat} can be obtained. Figure 6.7 explores the I_{Dsat} enhancement as a function of physical gate length L_G before (solid symbols) and after (open symbols) correcting for the difference in series resistance R_s.

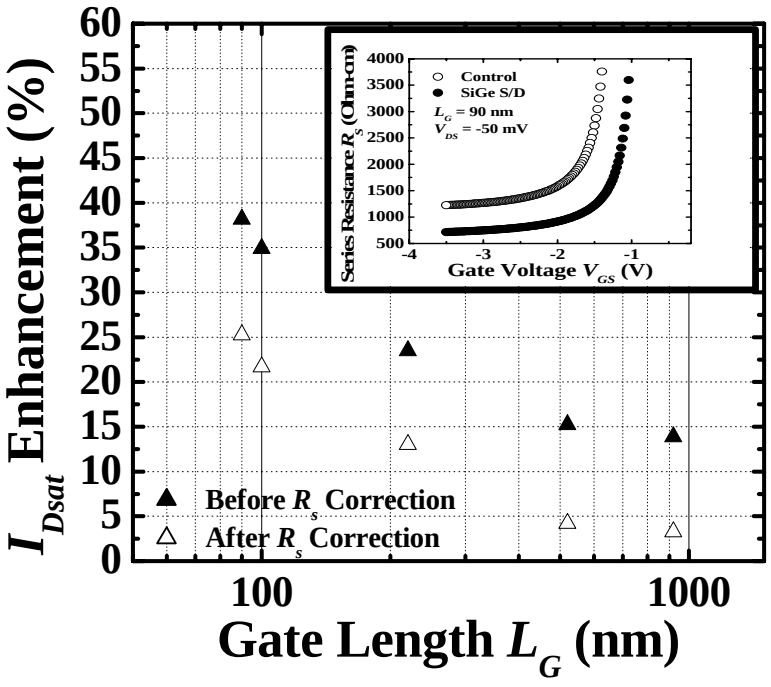


Figure 6.7 : Drive current I_{Dsat} as a function of L_G, before (solid symbols) and after correction (open sybols) for series resistance R_s. In both cases, I_{Dsat} enhancement increases with decreasing L_G. Improvement in *Rs* accounts for 13% in I_{Dsat} enhancement.

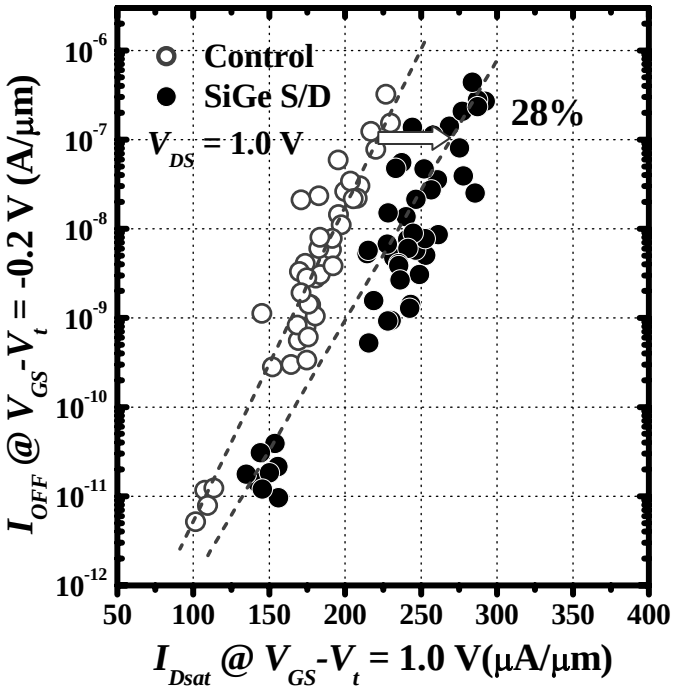


Figure 6.8 : I_{off}-I_{on} characteristics comparing the drive current performance of control and strained p-MOSFET with condensed SiGe S/D regions, demonstrating 28% improvement in the on-state saturation current I_{on} at a fixed off-state leakage I_{off} of 100 nA/μm.

In both cases, current enhancement increases with smaller L_G due to the increasing lateral, compressive strain induced in the Si channel as the SiGe S/D regions are being brought closer together [38]. The improvement in R_s for the strained pMOSFETs with condensed SiGe S/D stressors accounted for approximately 13% enhancement in drive current. Figure 6.8 plots the I_{off}-I_{on} characteristics for the control pMOSFETs and strained pMOSFETs with condensed SiGe S/D regions after series resistance correction. At a fixed off-state leakage I_{off} of 100 nA/μm (measured at V_{DS} = -1.0 V and V_{GS} = V_{Tsat} - 0.2 V where V_{Tsat} is the saturation threshold voltage extracted at V_{GS} = V_{DD}), strained pMOSFETs show an enhanced saturation drive current I_{on} performance (measured at V_{DS} = -1.0 V and V_{GS} - V_{Tsat} = -1.0 V) of up to 28% as compared to the control transistors after correction for series resistance. A 60% enhancement in maximum transconductance

G_{mmax} is observed at low V_{DS} (Figure 6.9 (a)) and the G_{mmax} enhancement improves with decreasing L_G (Figure 6.9 (b)). This trend is in good agreement with Figure 6.7 where drive current I_{Dsat} also increases with decreasing gate length L_G.

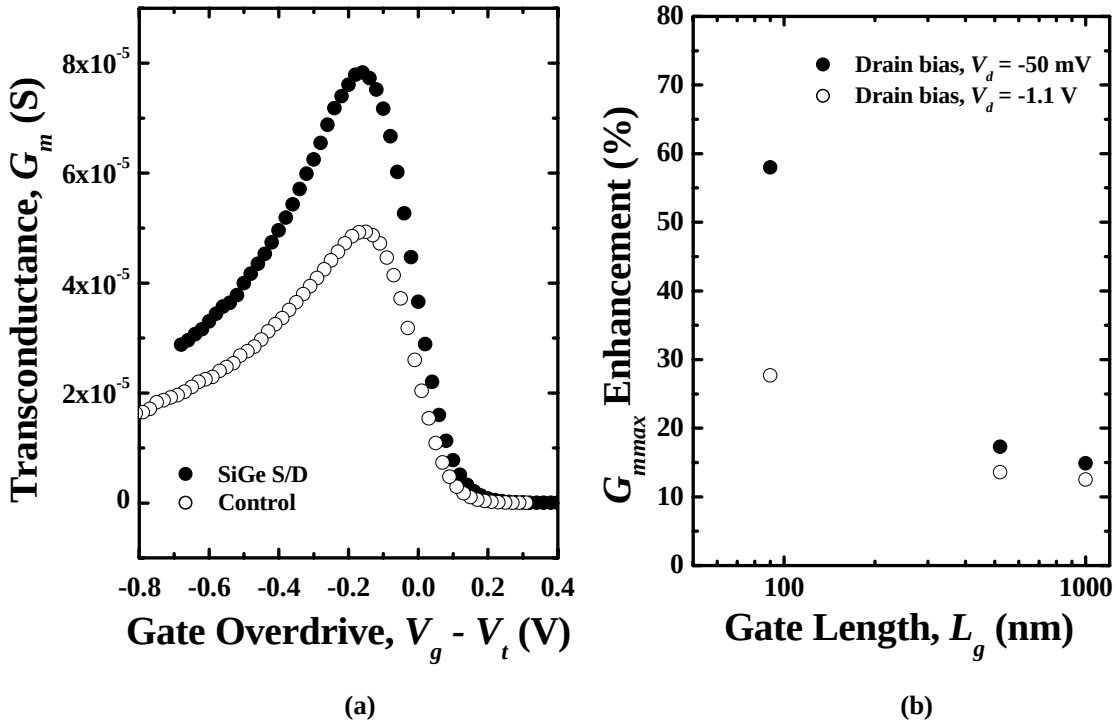


Figure 6.9 : (a) Comparison of transconductance G_m at the same gate overdrive illustrates an improvement of 60% (b) Maximum transconductance G_{mmax} as a function of gate length. Enhancement in G_m increases with decreasing gate length.

6.1.3 Material Characterization

Structural analysis of a transistor structure with SiGe S/D formed by local condensation technique was performed. Figure 6.10 (a) shows a high resolution TEM (HRTEM) image of the channel region near to the SiGe S/D stressor after condensation at 950°C. Strain effects were investigated by analyzing the diffractogram at specific locations in the image and comparing it with a reference location in the same image where the strain is assumed to be negligible. Details of the strain analysis technique has been discussed earlier in chapter 4. Figure 6.10 (b) shows the lateral compressive strain ε_{xx} in the Si channel. The magnitude of ε_{xx} is the largest in the vicinity of the stressor, and decreases with increasing depth and towards the middle of the Si channel.

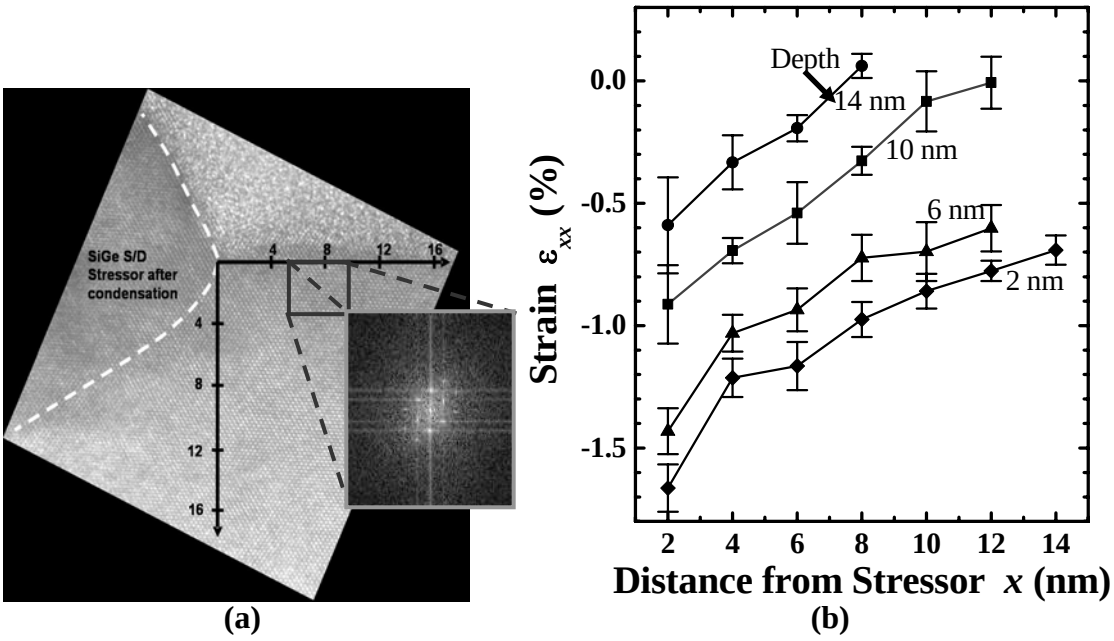


Figure 6.10 : (a) High resolution TEM image showing the SiGe S/D formed by Ge condensation and the adjacent channel region. Diffractogram at a specific position in the channel region reveals the presence of lateral compressive strain (b) Lateral strain profile at various depths below the Si surface, extracted from an analysis of the HRTEM image, showing lateral compressive strain along the [110] channel direction.

Auger analysis was also carried out on samples that went through different oxidation conditions. The Ge depth profiles obtained from the various oxidation conditions are plotted in Figure 6.11. It is observed that the Ge concentration in the S/D regions can be increased above the as-grown concentration level. This highlights one of the key advantages of this approach, i.e. increasing the Ge concentration above the level achieved by epitaxy.

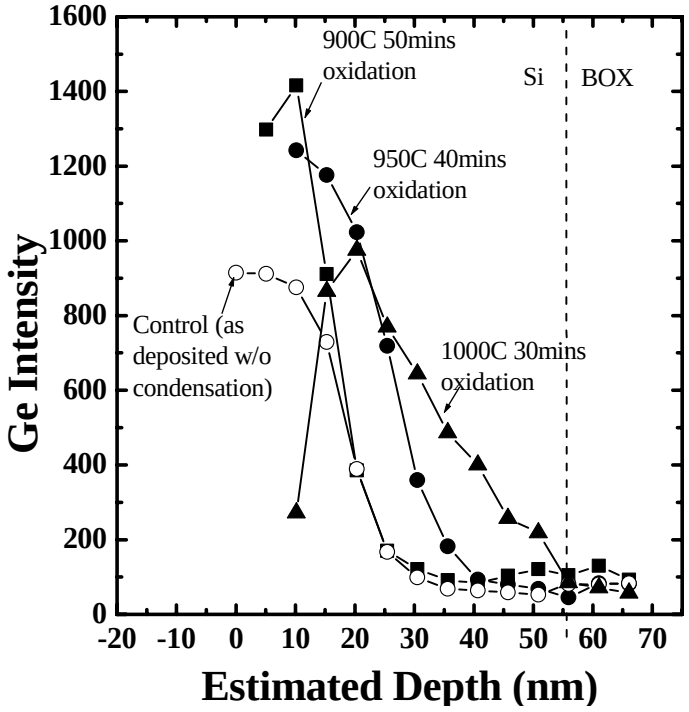


Figure 6.11 : Profile of Ge concentration of as-deposited SiGe sample (no Ge condensation) and SiGe samples that went through different Ge condensation conditions, as obtained using Auger Electron Spectroscopy. Different temperatures (900-1000°C) and oxidation durations were used. The Ge condensation process clearly increases the Ge concentration.

In addition, a thinner SOI substrate requires a thinner SiGe epi thickness or a reduced thermal budget to drive Ge into the S/D regions. Assuming a target final Ge content of 50% in the S/D regions with a final thickness *x*, the required initial SiGe thickness and its Ge content are shown in Figure 6.12 (c). It is assumed that the grown

SiGe will be entirely oxidized. For example, to form a 5 nm $Si_{0.5}Ge_{0.5}$ S/D, one needs to grow 8.3 nm of $Si_{0.7}Ge_{0.3}$ on 5 nm of Si, and fully consume the 8.3 nm of $Si_{0.7}Ge_{0.3}$ in the Ge condensation process. As a result, with reducing body thickness, a lowered thermal budget or higher Ge content in the S/D regions can be achieved, making this process a viable option for future high-speed ultra-thin-body devices.

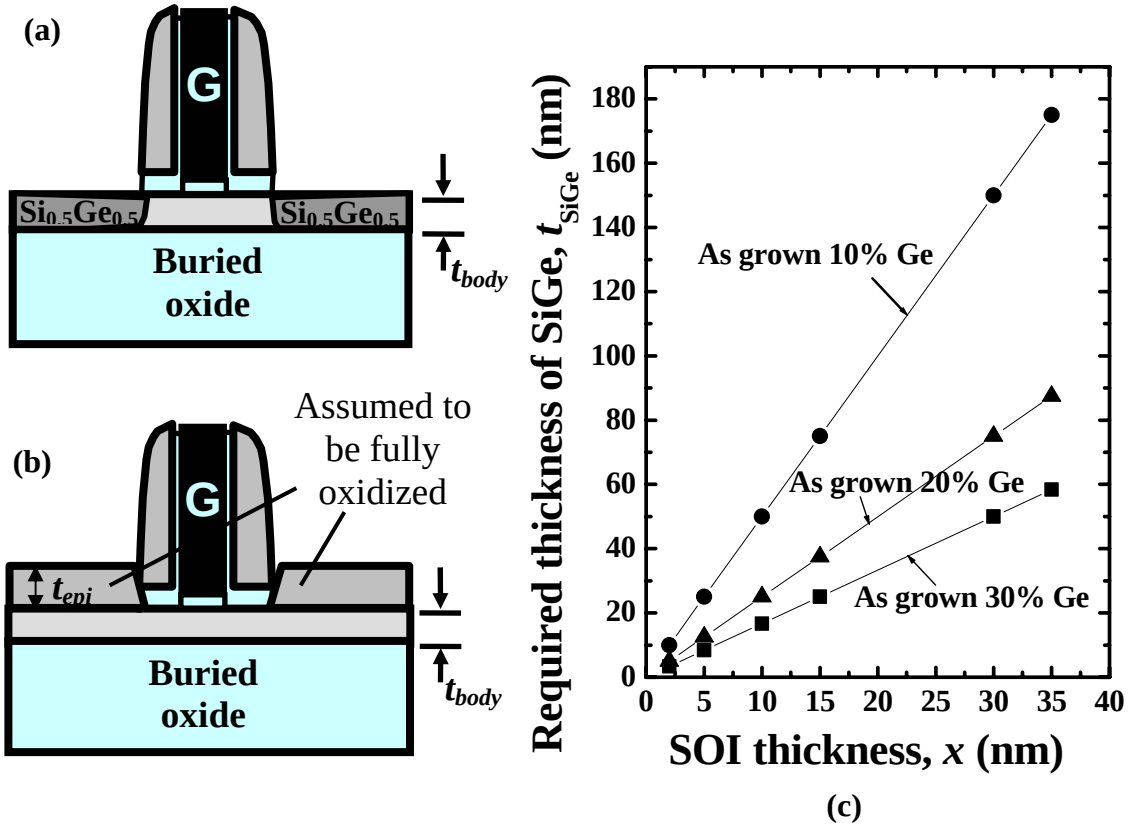


Figure 6.12 : (a) Assumed final device structure with a Ge content of 50% in the S/D, (b) an initial SiGe layer with thickness t_{epi} that is assumed to be epitaxially grown and fully oxidized to give device in (a), (c) the amount of t_{epi} required for different t_{body}.

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6.2 Strained UTB pMOSFETs with Condensed SiGe S/D

6.2.1 Background

As field-effect transistor gate lengths are being scaled into the nano-regime, new device solutions are essential to sustain effective control of short channel effects. Silicon-On-Insulator (SOI) technology is a promising approach for its excellent suppression of short channel effects (SCE), prevention of latch-up, low junction leakages and reduced parasitic capacitances [18] – [20]. As the gate length is scaled further, the SOI body thickness has to be reduced to even thinner layers for better control of short channel effects. Likewise, as described in the previous section, strain engineering can help to further extend the performance limits of CMOS devices. Incorporation of strain into the Si channel modifies the electronic valence sub-bands to result in higher carrier mobility, eventually leading to a larger drive current. In the earlier section of this chapter, a novel approach of fabricating uniaxial compressive-strained pMOSFETs using local condensation of SiGe [63] has been proposed to alleviate potential problems of controlling the recess etch depth and in performing selective epitaxy on an ultra-thin Si layer. In addition, the Ge content in the S/D regions can be increased as a result of the condensation process.

In this section, we further report on the concept and demonstration of this approach of using local Ge condensation to form a novel strained UTB P-channel transistor with 8 nm body thickness and with SiGe S/D stressors extending to buried oxide (BOX) for increased strain effects. The final Ge content in the SiGe S/D regions is also one of the highest reported to date in strained pMOSFETs using embedded SiGe S/D regions.

6.2.2 Optimization of Device Structure and Process Conditions for Increased Strain Effects

Assuming a UTB MOSFET device structure similar to that in Figure 6.1 with embedded SiGe S/D depth *d* and Si body thickness t_{body}. Stress simulation is performed using TAURUS process simulator to investigate the impact of varying the depth of the embedded SiGe S/D regions on the strain induced in the Si channel. Figure 6.13 (a) plots the simulated compressive strain in the Si channel as a function of depth of the embedded SiGe S/D. A larger compressive stress in the Si channel is induced as the depth of the SiGe S/D regions is increased deeper and deeper towards the buried oxide (BOX). An optimum strain is achieved when S/D regions extend to the top interface of the BOX, therefore enclosing the Si channel on both sides. Figure 6.13 (b) plots the strain in the channel as a function of Ge percentage in the S/D regions for different body thicknesses. Increasing the Ge percentage in the S/D regions increases the compressive strain in the channel. In addition, a thinner body thickness can also result in a higher compressive strain in the channel. It is therefore evident that a UTB transistor with Ge-enriched S/D extending all the way to the BOX will derive the most benefit from the SiGe S/D stressor to give superior performance.

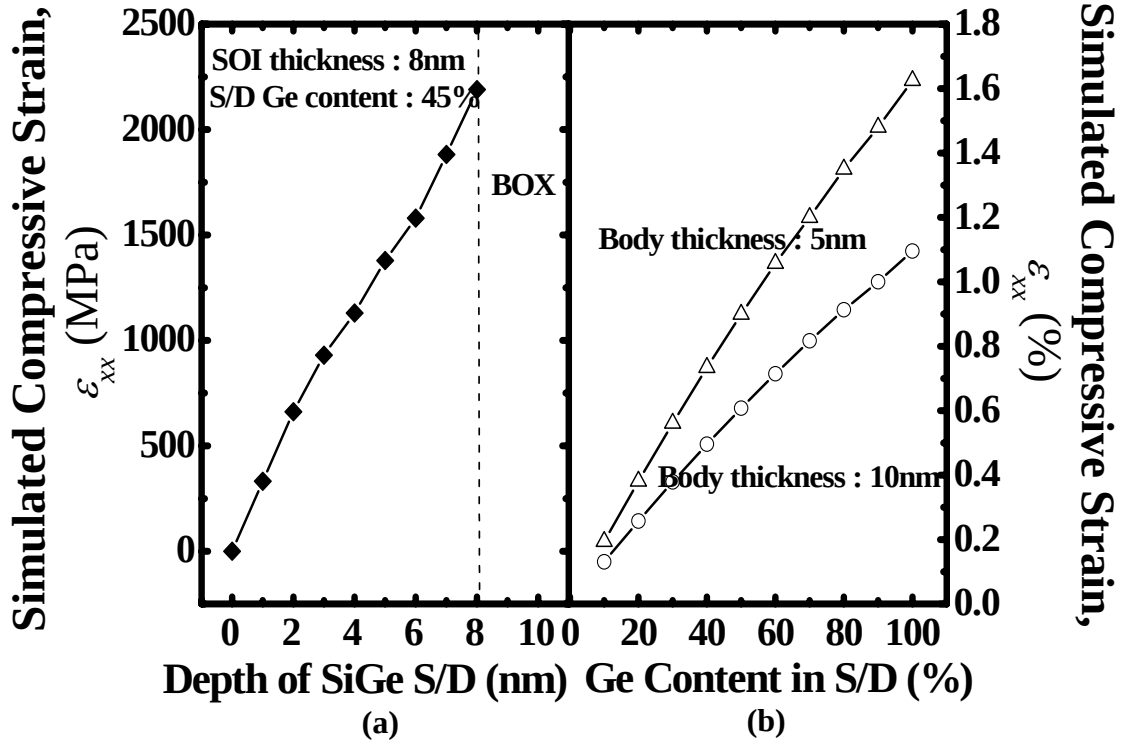

Figure 6.13 : (a) TAURUS stress simulations reveal that the induced compressive strain in the transistor channel in Figure 6.1 is largest when SiGe S/D regions extend to the buried oxide (BOX). (b) The channel strain induced increases with reduced body thickness and increased Ge content in the S/D regions.

6.2.3 Fabrication of Strained UTB pMOSFETs with SiGe S/D

The proposed fabrication process flow of the strained UTB pMOSFET introduces 2 more process steps into a conventional pMOSFET process flow. After mesa formation, threshold voltage V_t adjust and punchthrough implants were performed. 248 nm optical lithography and photo-resist trimming was employed for gate patterning and gate stack formation. This is followed by spacer formation. Selective epitaxial growth of $Si_{0.75}Ge_{0.25}$ was performed on the S/D regions followed by Ge-condensation at 900^0C to increase the Ge content to more than 40%. Figure 6.14 shows the schematic of a UTB transistor

structure with SiGe layers grown on the S/D regions before oxidation (a) and during the condensation (oxidation) step (b). Figure 6.15 plots the oxidation rate of SiGe

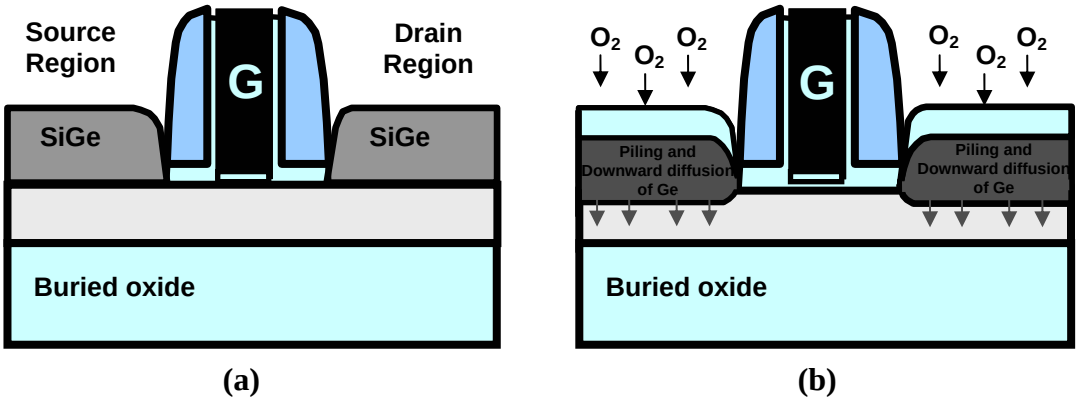

Figure 6.14 : (a) Schematic illustrating selective epitaxial growth of SiGe layers on S/D regions of pMOSFET structure before condensation (oxidation) process. (b) Condensation of SiGe layers on the S/D regions in 3 (a), Ge is driven into the Si S/D regions in the process.

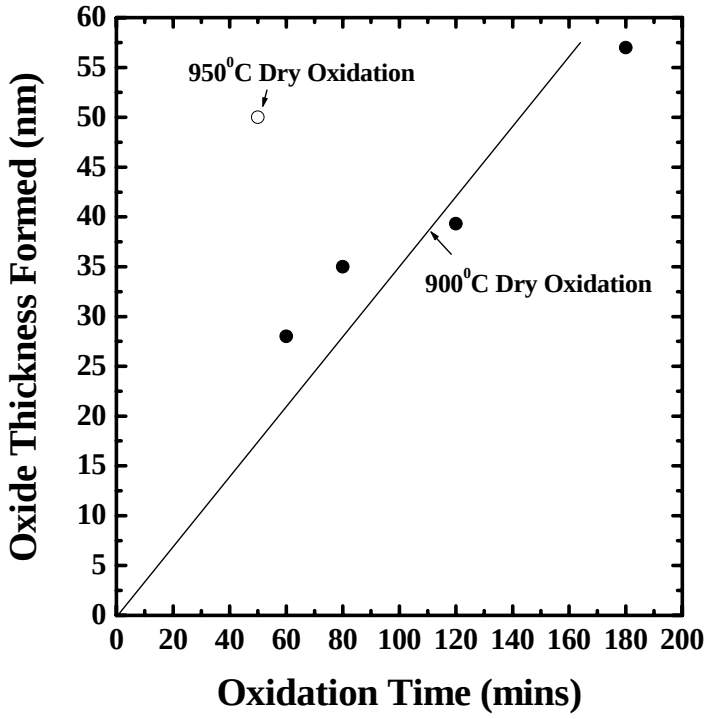

Figure 6.15 : Thickness of oxide formed by oxidation of $Si_{0.75}Ge_{0.25}$ layers on Si S/D regions of pMOSFET structure as a function of time.

at 900^0C. Energy Dispersive X-Ray Spectroscopy (EDS) analysis is performed on TEM samples of MOSFET structures with condensed SiGe S/D to obtain the Ge content profiles for various condensation conditions. As shown earlier in Figure 6.13, optimal strain in the channel can be achieved when the embedded depth of the SiGe S/D regions reaches all the way to the BOX. In order to achieve this structure, the epitaxial growth and condensation of the SiGe layers at the S/D regions have to be optimized. Figure 6.16 compares the Ge content depth profile for an optimized S/D Ge condensation process and an unoptimized process. With an unoptimized process, Ge content drops quickly with increasing depth, with the SiGe embedded at a depth of only half that of the SOI body thickness. This happens when the as-grown SiGe on the S/D regions is not sufficiently thick to provide enough Ge atoms to be fully driven to the BOX. An optimized process gives a fairly uniformly Ge profile with the SiGe S.D regions embedding all the way into the BOX for increased strain effects. On the control wafer, selective epitaxy of Si is done to form raised Si S/D to minimize differences in series resistance. S/D implantation and dopant activation steps were performed before contact and metallization to complete the fabrication. Figure 6.17 (a) shows the cross-section TEM image of a 70 nm gate length strained-Si UTB pMOSFET, featuring an 8 nm thick body region enclosed by condensed SiGe S/D regions. A high resolution TEM (HRTEM) image of the S/D region is illustrated in Figure 6.17 (b). Energy Dispersive X-Ray Spectroscopy (EDS) measurements at various points along a line from the surface to the buried oxide reveal a fairly uniform Ge concentration of above 40% in the S/D region. Diffractogram [inset of Figure 6.17 (b)] obtained at the S/D regions reveals good crystalline quality.

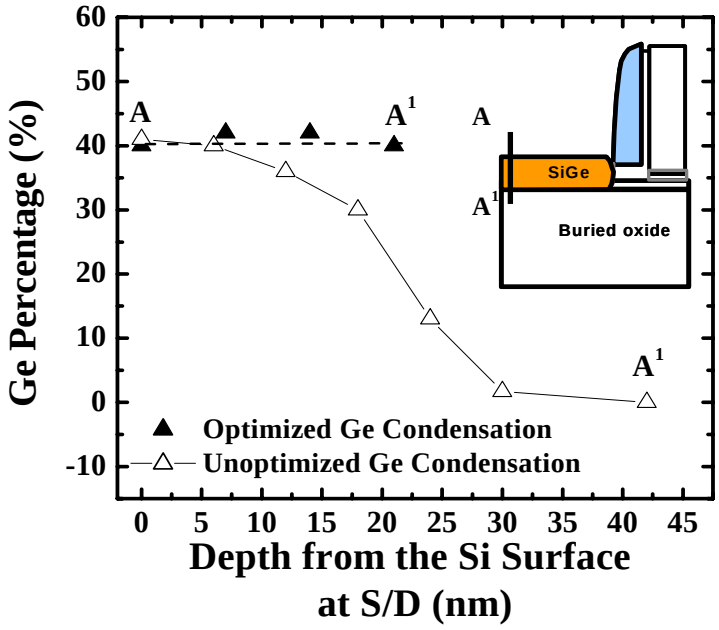

Figure 6.16 : Ge content depth profile (obtained from EDS of TEM samples) for an optimized S/D Ge epitaxial and condensation process and an unoptimized one. With an unoptimized process, Ge content drops with increasing depth, with the SiGe embedded at a depth of only half that of the SOI body thickness.

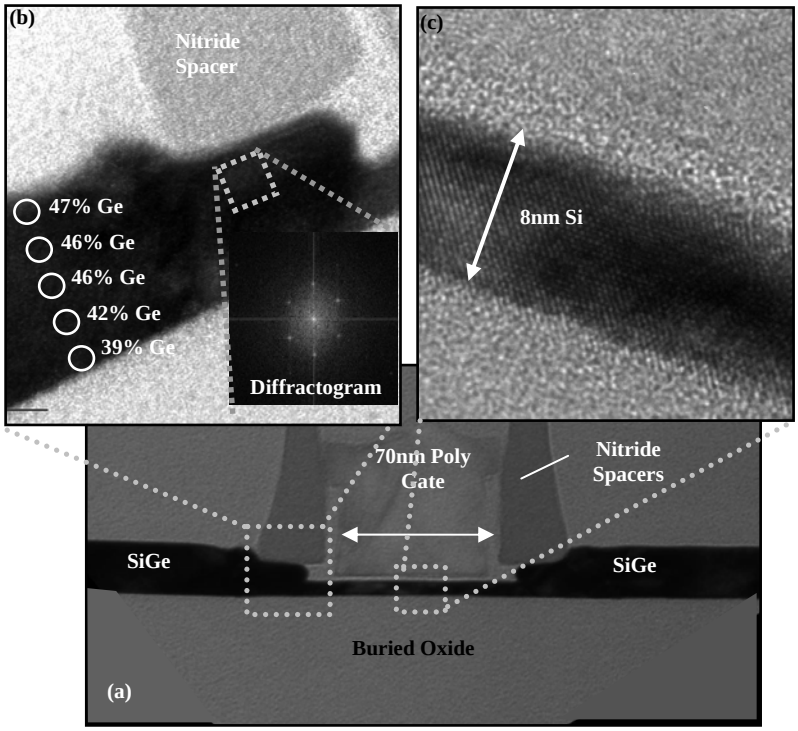

Figure 6.17 : (a) TEM image of a 70 nm gate length strained UTB pMOSFET with condensed SiGe S/D regions. (b) EDS analysis on magnified TEM image at S/D region showing Ge content of more than 40% across the entire S/D region. Diffractogram reflects good crystallinity. (c) HRTEM image of the channel region beneath the gate. The body thickness is 8 nm.

6.2.4 Electrical Characterization

Figure 6.18 (a) shows the I_{DS}-V_{DS} characteristics of 70 nm gate length control and strained UTB pMOSFET with $Si_{0.54}Ge_{0.46}$ S/D at various gate overdrives $|V_{GS} - V_t|$. I_{Dsat} enhancement of more than 70% was observed for the strained UTB pMOSFETs. The uniaxial compressive strain due to the SiGe S/D modifies the valence sub-band structure in the Si channel to result in lower hole effective mass, higher hole mobility, and improved I_{Dsat}. I_{Dsat} as a function of L_G is illustrated in Figure 6.18 (b), showing increasing I_{Dsat} enhancement with decreasing physical gate length L_G. This can be explained by the higher strain induced in the Si channel when L_G becomes smaller [9]. Figure 6.19 plots the amount of enhancement in saturation drain current (I_{Dsat}) against that in linear drive current (I_{Dlin}). Appreciable improvement in both I_{Dlin} and I_{Dsat} is observed in the $Si_{0.54}Ge_{0.46}$ S/D transistors. The measured I_{Dsat} gain is found to be approximately half of the I_{Dlin} due to its smaller sensitivity to the channel mobility enhancement [10]. Figure 6.20 (a) shows that the extracted series resistance in both strained and control devices are comparable, implying that the enhancement is predominantly attributed to strain effects. Note that this series resistance is very high compared to the one shown in Fig. 6.7 inset, which leads to much reduced drive current. Careful process and device optimization needs to be done if reduced series resistance needs to be achieved in UTB devices. I_{DS}-V_{GS} curves for both devices (Figure 6.20 (b)) illustrate improved subthreshold characteristics over the control UTB pMOSFETs. This could be partly due to the retarded boron diffusion in the presence of Ge [34] in the S/D regions, leading to a better controlled vertical and lateral diffusion profile for boron. As a result, a shallower and more abrupt S/D junction could be obtained in the strained device.

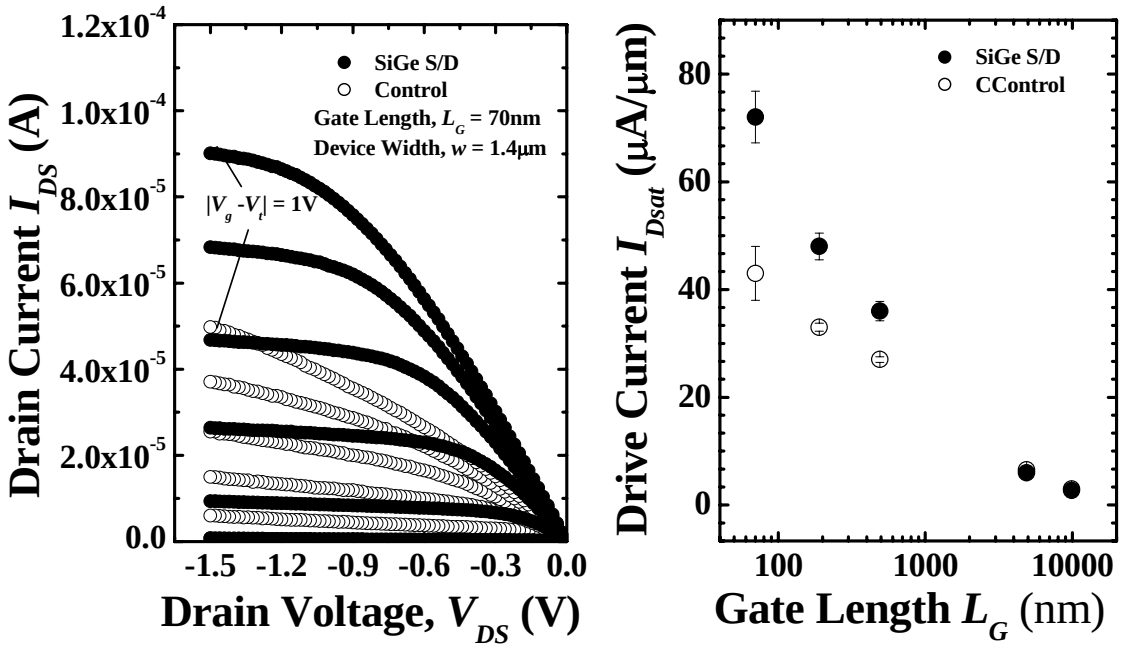

Figure 6.18 : (a) I_{DS}-V_{DS} characteristics of $Si_{0.54}Ge_{0.46}$ S/D and control UTB transistors with L_G = 70 nm for gate overdrives $|V_{GS} - V_t|$ of 0 to 1 V in steps of 0.2 V. The strained $Si_{0.54}Ge_{0.46}$ S/D pMOSFET shows more than 70% increase in I_{DS} at a gate overdrive of 1 V. (b) I_{Dsat} enhancement increases with decreasing gate length L_G due to the closer proximity of SiGe S/D regions to the Si channel, which leads to larger compressive strain in the channel.

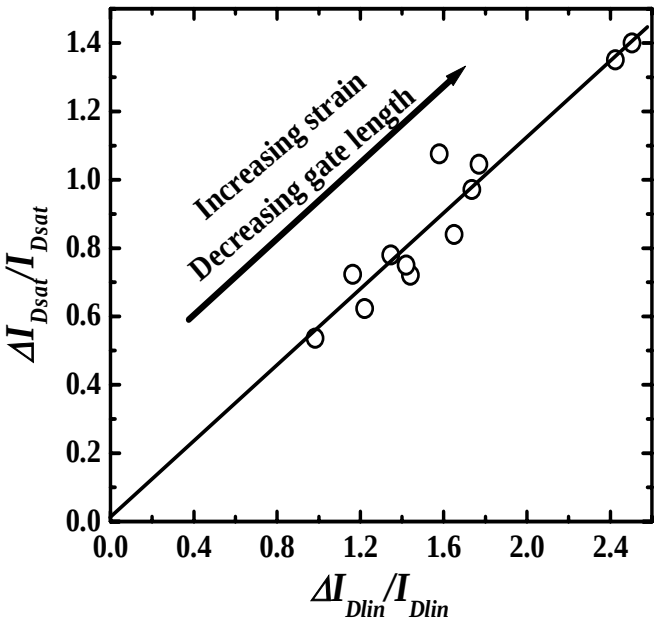

Figure 6.19 : Strained $Si_{0.54}Ge_{0.46}$ S/D pMOSFETs show significant drive current enhancement over the control devices. The measured I_{Dsat} gain is approximately half of that in I_{Dlin} due to the smaller sensitivity of I_{Dsat} on channel mobility gain.

The subthreshold swing and DIBL as a function of L_G for both devices are illustrated in Figure 6.21 (a) and (b), respectively. Excellent subthreshold swing of about 67 mV/decade and DIBL of 0.04V/V were achieved in the strained UTB pMOSFETs with $Si_{0.54}Ge_{0.46}$ S/D regions. Improvement in subthreshold and DIBL is observed for the strained devices. Figure 6.22 (a) depicts the transconductance G_m as a function of gate voltage V_{GS} for 70 nm gate length control and strained UTB pMOSFETs. G_m enhancement can be observed at both high and low V_{DS}. Dependence of transconductance G_m as a function of gate length L_G is depicted in Figure 6.22 (b). Strained UTB pMOSFETs with condensed $Si_{0.54}Ge_{0.46}$ S/D regions shows larger increase in both saturation and linear G_{mmax} than control UTB pMOSFETs with decreasing L_G. This illustrates the increase in G_{mmax} with decrease in physical gate length L_G, which can be easily explained by the increase in induced compressive strain in the transistor channel with reducing distance between the SiGe S/D regions.

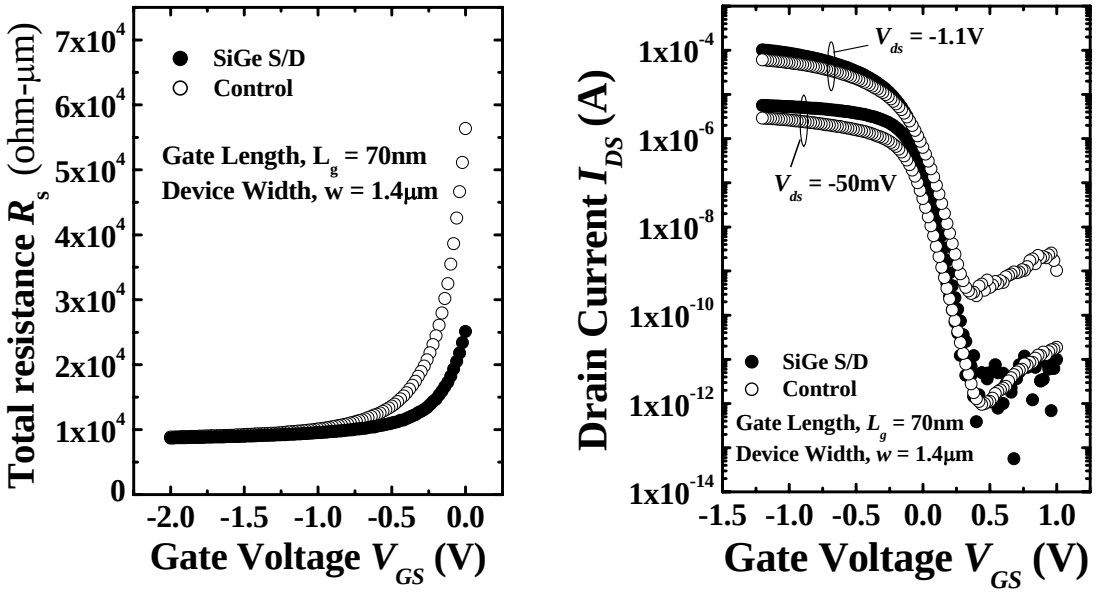

Figure 6.20 : (a) Extracted series resistance for the $Si_{0.54}Ge_{0.46}$ S/D and control devices is comparable. At high gate-overdrive and at low V_{DS}, the channel resistance is assumed to be negligible, the overall source-to-drain resistance mainly contributed by resistance at the source and drain side. (b) I_{DS}-V_{GS} characteristics of $Si_{0.54}Ge_{0.46}$ S/D and control UTB pMOSFETs. Strained UTB pMOSFET devices with condensed $Si_{0.54}Ge_{0.46}$ S/D shows improved short channel characteristics over control devices.

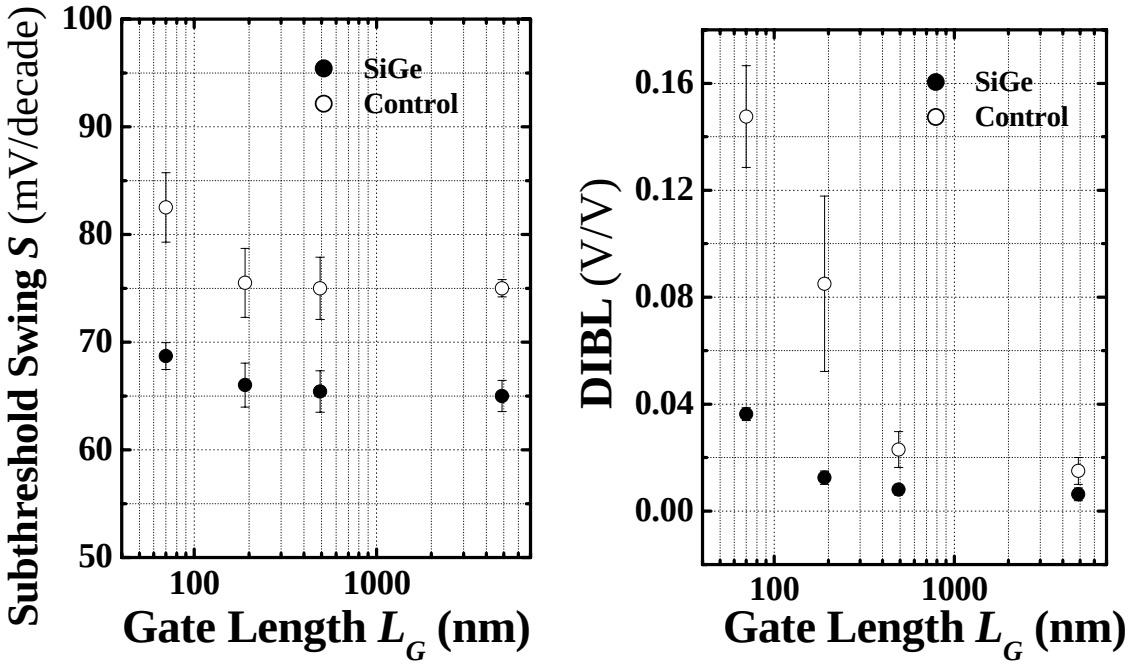

Figure 6.21 : (a) $Si_{0.54}Ge_{0.46}$ S/D pMOSFET shows improved subthreshold swing over control devices for all gate lengths. Excellent subthreshold swing of less than 70 mV/decade is obtained for the $Si_{0.54}Ge_{0.46}$ S/D pMOSFET. (b) DIBL characteristics against physical gate length for both control and strained devices

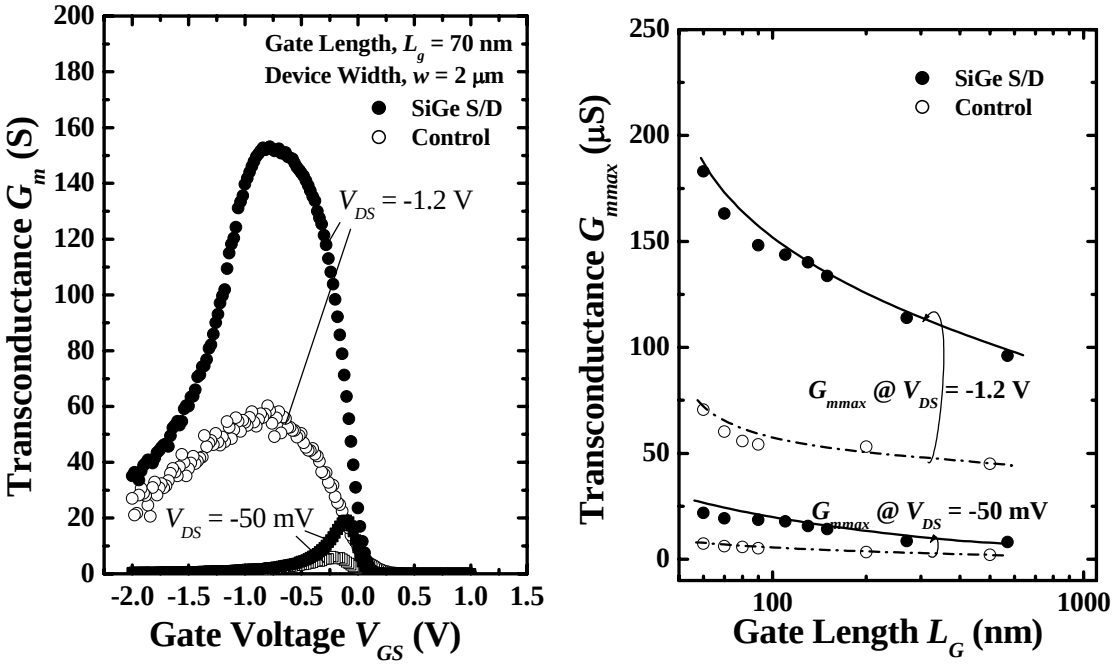

Figure 6.22 : (a) Transconductance *Gm* as a function of gate bias VGS for both $Si_{0.54}Ge_{0.46}$ S/D and control pMOSFETs at both high and low V_{DS}. (b) Increasing G_{mmax} with decreasing gate length L_G. $Si_{0.54}Ge_{0.46}$ S/D pMOSFETs reveal a larger increase in G_{mmax} with reducing L_G due to the larger strain effect of the SiGe S/D regions.

6.3 Summary

A novel strained-Si pMOSFET comprising SiGe S/D regions formed by local Ge condensation has been demonstrated. By using local Ge condensation, a Si recess etch step in the formation of SiGe S/D can be eliminated. Ge concentration in the source/drain can also be increased using the Ge condensation process, resulting in higher strain in the channel for enhanced hole mobility. This allows the implementation of SiGe S/D structures on ultra thin body SOI devices. Therefore, strained UTB pMOSFETs with 8 nm body thickness were demonstrated. The Ge content (~46%) in the S/D regions is the highest reported to date, realized using a Ge condensation technique. Significant I_{Dsat} enhancement was observed in the strained UTB pFET at 70 nm gate length. Excellent device performance can be achieved with this integration scheme, making it a promising option for future high speed devices.

CHAPTER 7

Conclusion

7.1 Summary

This thesis has examined several novel device structures for enhancement in MOSFET device performance. The key contributions are summarized below followed by recommendations for future work.

7.1.1 Source/Drain On Depletion Layer (SDODEL) CMOSFET for Reduced Parasitic Junction Capacitances.

Complementary MOSFET devices with better performance have been fabricated. By simply adding a high energy, low dose implant of the same conductivity type as the S/D, a low, counter-doped layer can be formed beneath the S/D regions. Reduction in parasitic junction capacitance for both n and pMOSFETs have been demonstrated. Fabricated ring oscillator structures also experimentally verify the improvement in circuitry speed. In addition, simulation has been performed to project the feasibility of SDODEL devices for future sub-50nm high speed devices.

7.1.2 Strained Si on Relaxed SiGe MOSFET

Complementary CMOS device have been fabricated using a conventional 0.18 μm technology node process flow. Electrical device characterization was performed and drive current enhancement was observed in the strained devices fabricated on strained Si /

relaxed SiGe substrates. However, there are also various issues and challenges related to strained Si on relaxed SiGe. Some of these issues and challenges have been addressed.

7.1.3 Material Characterization of Strained Si MOSFET Structures

An alternative technique to analyze strain distribution in MOSFET structures have been proposed. This technique involves the analysis of high resolution TEM (HRTEM) images. In particular, this method has been applied on MOSFET structures with S/D stressors. Another technique which involves the use of EDS on TEM images to characterize the Ge content in SiGe S/D regions have also been discussed.

7.1.4 Strained nMOSFETs with SiC S/D Regions

A novel strained nMOSFET structure featuring SiC S/D regions is proposed. Devices are fabricated for electrical and material characterization. The use of SiC S/D regions induces a lateral tensile and vertical compressive strain in the Si channel of the device, which benefits electron mobility to give a larger drive current. The implementation of such a structure on SOI substrate for further enhancement in device performance was carried out. Channel orientation dependence and multiple stressor effect are also investigated.

7.1.5 Strained pMOSFETs with Condensed SiGe S/D Regions

The implementation of SiGe S/D regions on thin body SOI substrates faces potential challenges like control of Si S/D recess etch depth and difficulty in growing SiGe on extremely thin layer of Si. A novel device structure using local condensation is proposed to alleviate these problems. This structure has also been applied on ultra-thin-body SOI substrates with less than 10nm of Si.

7.2 Future Work

There are several issues opened up by this thesis that deserve further exploration. These include :

- Silicidation of SiC S/D regions.
- The effect of various S/D annealing on C substitutional efficiency.
- Laser annealing of SiC S/D regions to explore possibility of increasing C substitutional efficiency.
- To further increase Ge content in the SiGe S/D MOSFETs to investigate whether higher Ge content in the S/D regions can lead to higher drive current enhancement.
- To fabricate local condensed SiGe S/D on different surface orientation.
- Reliability issues of SiC S/D and condensed SiGe S/D devices.

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