LOW-VOLTAGE LOW-POWER CONTINUOUS-TIME DELTA-SIGMA MODULATOR DESIGNS

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Time flies. It has been five years since I came to NUS to pursue my Ph. D. degree. When I look back, I feel thankful, because I did not walked alone on this long and winding road.

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SUMMARY

Driven by the growing market of portable products, low-power design issue becomes more and more important in recent years. The low-power trend for the digital circuitry has been achieved by the scaling CMOS technology, which keeps offering transistors smaller size and lower supply voltage. However, the supply voltage reduction considerably degrades the performance of the analog/mixed-signal circuits, e.g. the analog-to-digital converter. As a promising candidate for the analog-to-digital conversion, the Delta-Sigma modulator has obtained many attentions from the industry and the academic. This research has focused on the low-voltage low-power Delta-Sigma modulator designs in the advanced CMOS technology. Various efforts have been devoted on the system-level and the circuit-level.

On the system-level, the continuous-time input-feedforward topology is adopted due to its attractive potential for low-voltage and low-power designs. The design method for the continuous-time topology is presented. Simulink-based models for the continuous-time Delta-Sigma modulator are proposed. Based on the models, nonidealities in the CT Delta-Sigma modulator are simulated and analyzed, and their solutions are given.

Three design examples are presented.

The first design is a 1.2-V 4^{th}-order single-bit wideband Delta-Sigma modulator. A novel structure is proposed for implementing the feedforward and summing part. Implemented in a 0.13-μm CMOS technology, this design achieves 68-dB dynamic range over 1.25-MHz signal bandwidth with a 160-MHz sampling frequency. The power consumption is 2.7-mW, and the core area of the modulator is 0.082 mm^2. The measurement results verify that the proposed feedforward and summing structure is effective to reduce the power consumption with a small silicon area.

The second design is a 1-V 4th-order 1.5-bit audio Delta-Sigma modulator. The 1.5-bit input-feedforward topology with optimized coefficients is used. The feedforward and summing part is embedded into the 1.5-bit quantizer. A simple dynamic element matching circuit is designed to improve linearity. Designed in a 0.13-µm CMOS technology, the modulator shows a peak signal-to-quantization noise and distortion ratio of 97.3-dB over 20-kHz signal bandwidth. The power consumption is 42.6-µW, and the chip area is 0.125 mm^2. Compared to other low-voltage audio Delta-Sigma modulators, this design shows very low power and very small area.

The third design is a 0.6-V 4th-order single-bit audio Delta-Sigma modulator. A simple and power-efficient amplifier structure with body-driven gain-enhanced technique is proposed. A novel rail-to-rail input common-mode feedback circuit is presented for the low-voltage operation. Implemented in a 0.13-µm CMOS technology, the design shows an 82-dB dynamic range with 28.6-µW power consumption. The measurement results show that with the proposed circuits the design achieves low power consumption, while maintaining a good resolution.

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LIST OF SYMBOLS

A-A	Anti-Aliasing
ADC	Analog-to-Digital Converter
ASP	Analog Signal Processing
BP	Band-Pass
CMFB	Common-Mode FeedBack
CT	Continuous-Time
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processing
DT	Discrete-Time
DR	Dynamic Range
ENOB	Effective Number Of Bits
FFT	Fast Fourier Transform
FOM	Figure-Of-Merit
HRZ	Half-delayed Return to-Zero
LP	Low-Pass
LSB	Least-Significant-Bit
MSB	Most-Significant-Bit
NRZ	None-Return to-Zero
NTF	Noise Transfer Function
OSR	OverSampling Ratio
PCB	Printed Circuit Board
PSD	Power Spectral Density

rms	Root-Mean-Square
RZ	Return to-Zero
SC	Switched-Capacitor
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise-and-Distortion Ratio
SQNR	Signal-to-Quantization Noise Ratio
SOC	System-On-Chip
STF	Signal Transfer Function

CHAPTER 1

INTRODUCTION

1.1 Background

Digital signal processing (DSP) has many advantages over analog signal processing (ASP), such as higher reliability, higher accuracy, smaller size, lower power consumption, and more functionality. In addition, the rapid development in CMOS VLSI technology ensures the economical implementation for the DSP circuitry. Therefore, the current trend in communication systems tends to push signal processing into the digital domain as much as possible. As the interface between the analog world and the digital world, the analog-to-digital converter (ADC) is a necessary and critical part, because it directly determines the resolution of the input signal to the DSP circuitry.

The Delta-Sigma ADC is one of the most popular ADCs. By using oversampling technique, noise-shaping technique, and digital filtering technique, the Delta-Sigma ADC can achieve superior resolution up to 24-bit [Ti07]. Furthermore, without accurate analog component matching requirement, the Delta-Sigma ADC provides good compatibility with the digital CMOS VLSI technology, and therefore, it can be easily integrated with the DSP circuitry.

Nowadays, many companies (e.g. Analog Devices, Texas Instruments, and so on) are involved in the Delta-Sigma ADC design, and Delta-Sigma ADCs have been applied in a large amount of applications. Low-pass Delta-Sigma ADCs have been widely employed in high-precision audio applications [AD93] [Bur94] [Cry94] [Pil94] [TI95]. Band-pass Delta-Sigma ADCs have been used to digitize the signals at IF stage, exhibiting interesting characteristics for the suppression of out-of-band noise and channel selection [Jan97] [Kim09] [Lu10]. Besides the analog-to-digital

data conversion, Delta-Sigma modulators are also employed in many other applications, like the switching Class-D amplifier [Kan08], the polar transmitter [Jau04], the fractional-N phase-locked loops (PLL) [Ril93] [Ken99] [Jia10], and so on.

Due to the development of CMOS technology and the innovations of circuits, the performance of the Delta-Sigma modulator continues to improve, and the figure-of-merit (FOM), which is used to quantify the need energy per conversion step, is reduced to very low values [Mit06] [Cha08]. Recently, the research on Delta-Sigma Modulators has entered some new areas. One trend for the Delta-Sigma modulator is to operate at higher frequencies for wideband wireless and wired communication applications, like CDMA, UMTS, ASDL, WiMAX, video, wireless base-stations, and so on. Due to the oversampling technique, the traditional sigma-delta ADCs were only popular at low-speed high-resolution applications. However, Delta-Sigma ADCs are currently capable of processing signal bandwidths higher than 1 MHz [Yan01] [Mag09] [Bos10], even up to more than 20 MHz [Yag05] [Mit06] [Mal08] [Par09a]. Another trend for the Delta-Sigma modulator design is to design the system with low supply voltage. In some recently-reported designs for audio applications, the modulators are operated with sub-1V supply voltages [Pel98] [Sau02] [Ahn05] [Goe06] [Pun07] [Kim08] [Roh08] [Cha08] [Par09] [Mic11], which shows the possibility to reduce the analog supply down to the same level as the digital supply for system-on-chip (SOC) applications.

1.2 Motivation

For both wide-band and audio-band Delta-Sigma modulators, the low-power design has become an important issue, especially for the portable applications.

The continuous-time (CT) Delta-Sigma modulator can be a better candidate for the low-power design, when compared to its discrete-time (DT) counterpart. Traditional Delta-Sigma modulators are implemented with DT loop filters. Based on the switched-capacitor (SC) technique, the DT

Delta-Sigma modulator can easily achieve good resolution and linearity. Delta-Sigma modulators can also be implemented with CT loop filters, which are based on active-RC and/or Gm-C filters. CT Delta-Sigma modulators have the advantages of higher speed, lower power, and inherent anti-aliasing filter, and hence, they have attracted more attention recently. However, CT Delta-Sigma modulators are sensitive to some nonidealities, such as the clock jitter, the excess loop delay, the time-constant variation, and so on. All of these nonidealities increase the difficulties to design a CT Delta-Sigma modulator.

Furthermore, the trade-offs between the supply, the power, and the performance must be taken into considerations. The scaling supply tends to degrade the performance of the circuit, and it is often the case that a higher current is needed to compensate this performance degradation. Therefore, carefully designs are required, and usually, innovations are needed to improve the FOM of the circuit.

This research targets the low-voltage low-power designs for CT Deltas-Sigma modulators, which are highly desirable but full of challenges. The low-voltage design is driven by the advanced CMOS VLSI technology, and the low-power design is driven by the growing market of portable products. In this research, various techniques and innovations will be utilized on the system-level, the circuit-level, layout-level, and PCB-level. To verify those techniques and innovations, design examples will be presented.

1.3 List of Publications

Jinghua Zhang, Libin Yao, Bo Shi, Yong Lian, "A 0.6-V 82-dB 28.8-μW Continuous-Time Audio Delta-Sigma Modulator," submitted to *IEEE Journal of Solid-State Circuits*.

Jinghua Zhang, Libin Yao, Bo Shi, Yong Lian, "A 1-V 42.6-μW 1.5-bit Continuous-Time Delta-Sigma Modulator for Audio Applications," *IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics (PrimeAsia)*, Sept. 2010.

Jinghua Zhang, Libin Yao, Yong Lian, "A 1.2-V 2.7-mW 160MHz Continuous-Time Delta-Sigma Modulator with Input-Feedforward Structure," *IEEE Custom Integrated Circuits Conference*, pp. 475−478, Spet. 2009.

Jinghua Zhang, Bo Shi, Yong Lian, "Performance Evaluation on Polar Transmitters Using Delta and Delta-Sigma Modulations," *IEEE International Conference on Information, Communications & Signal Processing*, 2007.

1.4 Thesis Organization

This work covers the theoretical analysis, the system-level design and the circuit implementation, and the test setup of low-voltage low-power CT Delta-Sigma modulators. The organization of the thesis is as follows.

Chapter 2 reviews the basics of the Delta-Sigma modulator, including its operating principle and different types. In addition, literature review on low-voltage low-power Delta-Sigma modulator designs is also given.

Chapter 3 discusses the system-level issues. The system-level design methodology of the CT Delta-Sigma modulator will be described. The Simulink-based model for the CT Delta-Sigma modulator will be proposed. Based on the model, nonidealities in the CT Delta-Sigma modulator will be analyzed.

Chapter 4 presents the low-voltage and low-power CT Delta-Sigma design for the wideband applications. A 1.2-V 1-bit input-feedforward Delta-Sigma modulator with 1.25-MHz signal

bandwidth will be presented. A novel structure for the feedforward and summing part will be proposed to save the power consumption and the chip area, and to simplify the circuit design.

Chapter 5 presents two low-voltage and low-power CT Delta-Sigma designs for the audio applications. One modulator operates with a 1-V supply using the 1.5-bit input-feedforward topology. The novel feedforward and summing structure is be used for the 1.5-bit quantizer. A simple dynamic element matching circuit is designed to improve its linearity. The other modulator operates with a 0.6-V supply using the 1-bit input-feedforward topology. A simple and power-efficient amplifier structure is used. To increase its dc gain, body-driven gain-enhanced technique is proposed. A novel rail-to-rail input CMFB circuit is presented for the low-voltage operation.

Chapter 6 concludes this research and provides some suggestions for the future research.

CHAPTER 2

LITERATURE REVIEW OF DELTA-SIGMA MODULATORS

2.1 Introduction

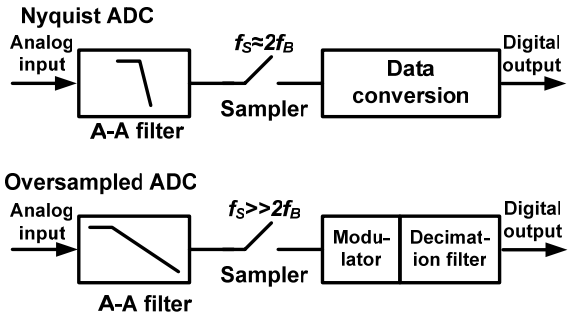
Analog-to-digital converters can be classified into Nyquist ADCs and oversampled ADCs. Fig. 2.1(a) shows the structures of these two types of ADCs, both of which comprise an anti-aliasing filter (A-A filter), a sampler, and an analog-to-digital conversion block. Due to the different data conversion techniques, Nyquist ADCs can be divided into successive approximation ADCs, pipeline and interpolation ADCs, flash ADCs and so on. The Delta-Sigma ADC is a kind of oversampled ADCs.

As the name implies, the oversampling clock frequency f_s is much higher than the Nyquist rate $2f_B$, where f_B is the signal bandwidth. The relationship between f_s and f_B can be described by the parameter oversampling ratio (OSR), which is defined as:

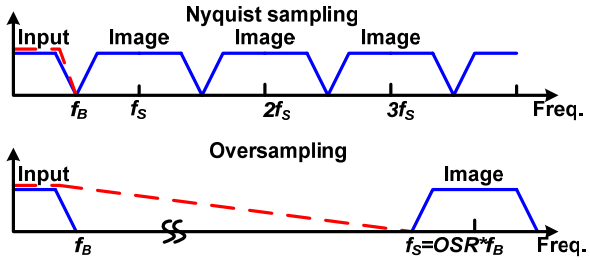
$$OSR = \frac{f_s}{2f_B}. \tag{2.1}$$

The oversampled ADC has some advantages over the Nyquist ADC.

First, as shown in Fig. 2.1(b), the oversampled ADC allows an A-A filter with much wider transition band due to its oversampling effect.



(a)



(b)

Figure 2.1: Blocks of the Nyquist ADC and the oversampled ADC (a), A-A filter requirements of the Nyquist ADC and the oversampling ADC (b).

Second, the oversampled ADC relaxes the requirements on the analog circuitry and shows better compatibility with the digital circuitry. The Nyquist ADC requires very accurate analog components to achieve high resolution [Sch05]. However, the accuracy requirement on the analog components is greatly relaxed in the oversampled ADC, since its modulator's output can be only one-bit [Sch05]. Therefore, the oversampled ADC is easier to implement with the digital circuitry. This advantage makes the oversampled ADC very suitable for system-on-chip systems.

Third, the oversampled ADC can achieve much higher resolution than the Nyquist counterpart. Subject to the process mismatches of the analog components like resistors and capacitors, the maximum resolution in Nyquist ADCs is about 12 bit [Sch05]. However, as mentioned above, the accuracy requirements on the analog components are relaxed in the oversampled ADC. Furthermore, for the Delta-Sigma ADC, the in-band quantization noise can be greatly suppressed

by utilizing the oversampling technique and noise-shaping technique, which will be discussed later in this chapter. As a result, the maximum resolution of an Delta-Sigma ADC can be achieved up to 24-bit (e.g. *Texas Instruments* ADS1274).

The trade-off for the high resolution is the limited signal bandwidth, and hence, Delta-Sigma ADCs are traditionally used for the narrow-band high resolution applications (see Fig. 2.2).

In this chapter, an overview on the Delta-Sigma modulator will be given. The organization is as follow. An introduction to the basics of the Delta-Sigma modulator is given in section 2.2 based on the simplest 1st-order Delta-Sigma modulator. The general model of the Delta-Sigma modulator is also introduced. Section 2.3 introduces various types of Delta-Sigma modulators. Section 2.4 is the literature review for the low-supply low-power Delta-Sigma modulator designs.

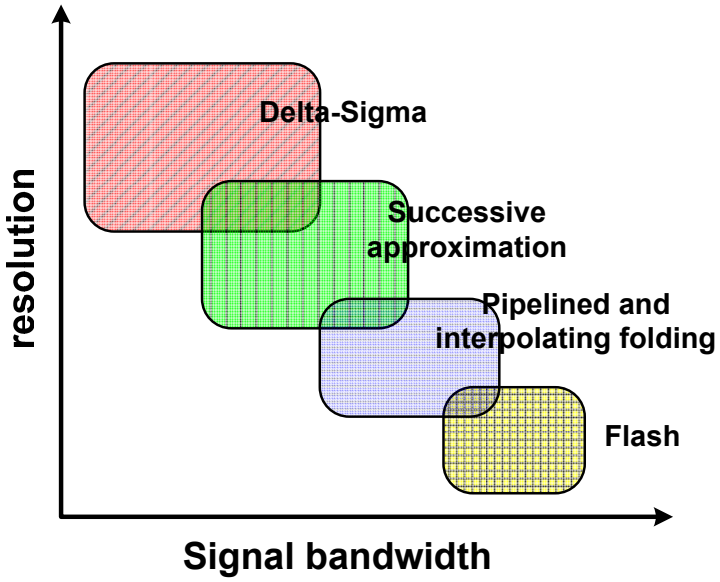
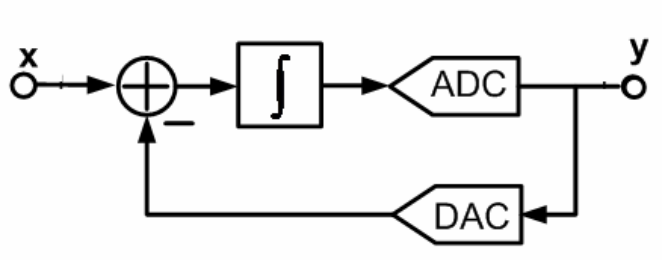


Figure 2.2: Resolution versus signal bandwidth plot for Delta-Sigma ADCs and Nyquist ADCs.

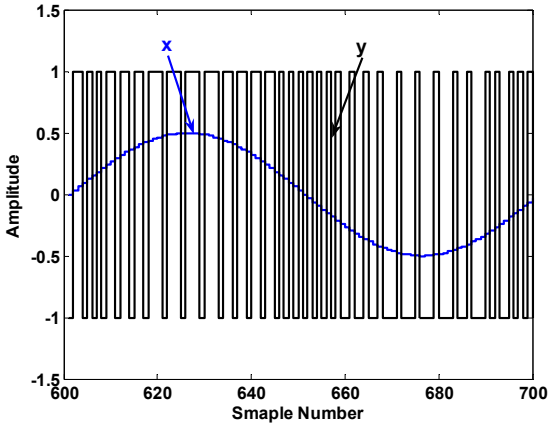
2.2 Basic Operation of the Delta-Sigma Modulator

2.2.1. Signal Transfer Function and Noise Transfer Function

As shown in Fig. 2.3(a), the Delta-Sigma modulator comprises three basic building blocks: the loop filter, the coarse ADC, and the DAC in the feedback loop. The coarse ADC can be implemented by a 1-bit quantizer, and hence the output of the Delta-Sigma modulator is bit stream, as shown in Fig. 2.3(b).



(a)



(b)

Figure 2.3: Delta-Sigma modulator block (a), and input output waveforms (b).

To illustrate the basic operation of the Delta-Sigma modulator, the linear model of the 1st-order Delta-Sigma modulator in *z*-domain is shown in Fig. 2.4. In this model, the quantizer is modeled as a unity gain amplifier plus the quantization noise $E(z)$. The transfer function of the loop filter in the 1st-order Delta-Sigma modulator is:

$$I(z) = \frac{1}{z-1}. \tag{2.2}$$

The transfer function of the output Y can be expressed as:

$$Y(z) = z^{-1} \cdot X(z) + (1 - z^{-1}) \cdot E(z) = STF \cdot X(z) + NTF \cdot E(z), \tag{2.3}$$

where STF stands for Signal Transfer Function, and NTF stands for Noise Transfer Function. Equation 2.3 indicates that the input signal passed the modulator with a delay, and the quantization noise $E(z)$ is shaped by a high-pass filter, whose pole/zero and magnitude are shown in Fig.2.5. Due to the high pass filter, the quantization noise is suppressed in the signal band. This effect is called noise shaping [Nor97].

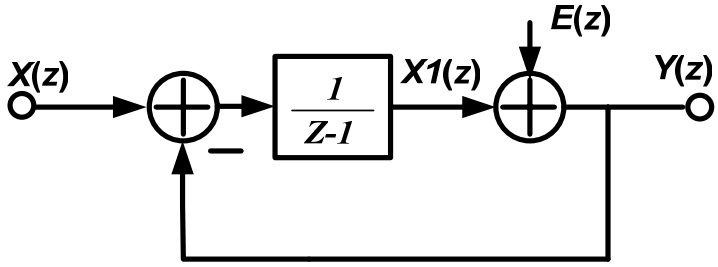
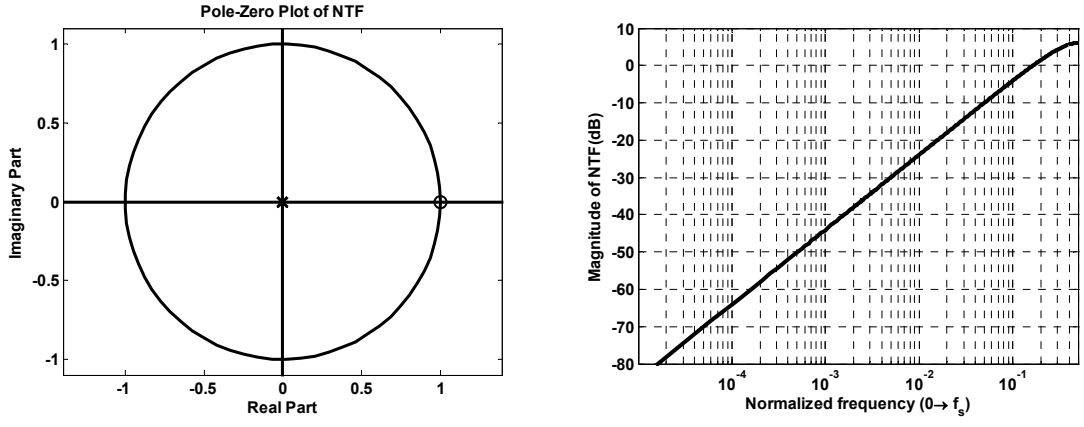


Figure 2.4: Linear model of the 1st-order Delta-Sigma modulator.



(a) (b)

Figure 2.5: NTF of the 1st-order Delta-Sigma modulator: (a) pole and zero, (b) the magnitude.

2.2.2. Quantization Noise

The quantization noise in the Delta-Sigma modulator is modeled as white and independent on its input. This assumption is accurate enough for most applications [Gra90] [Che00]. Thanks to W.R. Bennett's famous analysis of the quantization noise, the quantization noise power can be expressed as [Ben48]:

$$e^2 = \frac{1}{q}\int_{-\frac{q}{2}}^{\frac{q}{2}} e^2 de = \frac{q^2}{12}, \tag{2.4}$$

where q is the quantization step.

For the Nyquist-rate ADC, since the quantization noise is spread uniformly from dc to $f_s/2$, its in-band noise power spectral density (PSD) can be simply derived as:

$$S_{e,Nyquist}(f) = \frac{e^2}{f_s/2} = \frac{q^2}{12 \cdot f_B}. \tag{2.5}$$

Similarly, for an oversampling ADC, its in-band noise PSD can be simply derived as:

$$S_{e,OS}(f) = \frac{e^2}{f_s/2} = \frac{q^2}{12 \cdot OSR \cdot f_B}, \tag{2.6}$$

where OSR is oversampling ratio defined in Eq. 2.1.

In the Delta-Sigma modulator, the quantization noise is further shaped by the NTF of the modulator. For the 1st-order Delta-Sigma modulator, its NTF (see Eq. 2.3) can be translated to $1-e^{-j2\pi f/fs}$ in the steady state. If OSR is assumed much larger than 1, i.e. in the signal bandwidth, $f/f_s << 1$, the NTF can be approximately expressed as $2\sin(\pi f/f_s)$. With the noise shaping as well as the oversampling technique, the in-band noise PSD of the 1st-order Delta-Sigma modulator can be derived as:

$$S_{q,\Delta\Sigma}(f) = \left|NTF(z)\right|^2 \cdot S_{e,OS}(f) \approx (2\sin(\pi f / f_s))^2 \cdot S_{e,OS}(f) = \frac{\pi^2 q^2 f^2}{12 \cdot (OSR)^3 \cdot f_B^3}. \tag{2.7}$$

Fig.2.6 shows the noise PSDs of the three types of ADCs. Thanks to the oversampling and noise shaping techniques, Delta-Sigma ADCs show much less in-band noise than the other two ADCs, and this is why Delta-Sigma ADCs are able to achieve much higher resolution.

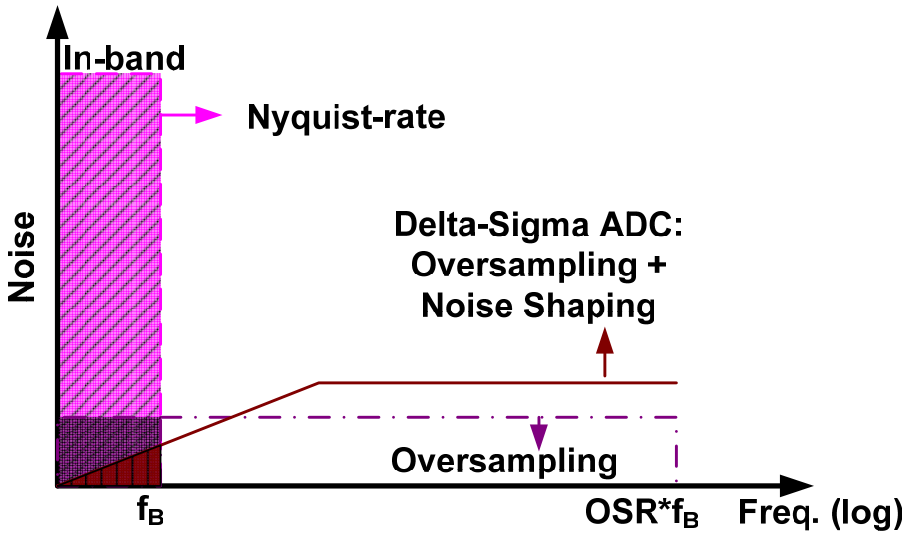


Figure 2.6: In-band noise of the Nyquist ADC, the oversampled ADC, and the Delta-Sigma modulator.

2.2.3. Performance Parameters

In the previous section, the principles of the Delta-Sigma modulator have been discussed. To measure its performance, some parameters will be introduced in this section.

A. *Signal-to-Noise Ratio* (*SNR*) and *Signal-to-Noise-and-Distortoin Ratio* (*SNDR*)

SNR is defined as the ratio between the signal power and the in-band noise power, which can be expressed as:

$$SNR = 10\log\frac{X_{rms}^2}{E_{rms}^2}. \tag{2.8}$$

If the input signal is a sinewave with the amplitude of A, its power can be dervied as:

$$X_{rms}^2 = \frac{A^2}{2}. \tag{2.9}$$

The in-band noise power can be derived as:

$$E_{rms}^2 = \int_0^{f_B} S_q(f)df, \tag{2.10}$$

where $S_q(f)$ is the noise PSD, and f_B is the signal bandwidth. By substituing Eq. 2.7 into Eq. 2.10, and combining Eq. 2.8-Eq. 2.10, the SNR for the 1st-order Delta-Sigma modulator is:

$$SNR_1 = 10\log\frac{18A^2(OSR)^3}{\pi^2 q^2}. \tag{2.11}$$

One thing should be noted is that, the noise here consists of quantization noise only. In practice, Delta-Sigma modulators suffer from many other kinds of noise, which will be covered in the following chapters.

Similarly, SNDR is defined as the ratio between the signal power and the total in-band noise and distortion power.

B. *Peak Signal-to-Noise Ratio*

Peak SNR refers to the the maximum ratio between the signal power and the in-band noise power. For a sine wave input, the max amplitude is $q/2$, the peak SNR can be derived from Eq. 2.11:

$$SNR_{1,P} = 10\log\frac{9(OSR)^3}{2\pi^2} = 10\log\frac{9}{2\pi^2} + 30\log(OSR) = -3.4dB + 30\log(OSR). \tag{2.12}$$

Equation 2.12 indicates that for a 1st-order Delta-Sigma modulator, the peak SNR increases 9dB with a double OSR.

C. *Effective Number of Bit* (*ENOB*) /*Resolution*

The resolution of the Delta-Sigma modulator can also be expressed by effective number of bits, which is defined as:

$$ENOB = \frac{SNR_{peak} - 1.76dB}{6.02dB}. \tag{2.13}$$

D. *Dynamic Range* (*DR*)

Dynamice range refers to the ratio of the maximum signal power, for which the modulator still works well, to the minimum detectable signal power. The dynamic range can be measured by the SNR versus input plot. The maximum signal power refers to the highest input amplitude, for which the modulator's SNR is 3 dB lower than its peak SNR. The minimum signal power refers to the input amplitude, for which the modulator's SNR is 0 dB.

E. *Figure-Of-Merit* (*FOM*)

There are many definitions for FOM, among which the one adopted in this resarech is defined as:

$$FOM = \frac{Power}{2 \cdot f_B \cdot 2^{(SNDR-1.76)/6.02}}, \tag{2.14}$$

where the power consumption, the singal bandwidth, and SNDR are taken into consideration.

2.2.4. Frequency Domain Response

The frequency domain response of the Delta-Sigma modulator is used to measure the modulator's resolution. The output spectrum can be estimated by the fast Fourier transform (FFT) [Hay02]. To avoid the energy leakage, the output is multiplied by a window before it is shown in the frequency domain. Hanning window is adopted in this thesis, whose function is:

$$Hann(n) = \frac{1}{2}[1 - \cos(\frac{2\pi n}{N})], \quad n = 0,1,...N-1. \tag{2.15}$$

The output spectrum for a sinusoid input signal are shown in Fig. 2.7. As shown in the figure, without Hanning window, the signal power spreads into adjacent bins, and the notch at dc

disappears. While with Hanning window the output spectrum can correctly reflect the noise-shaping effect.

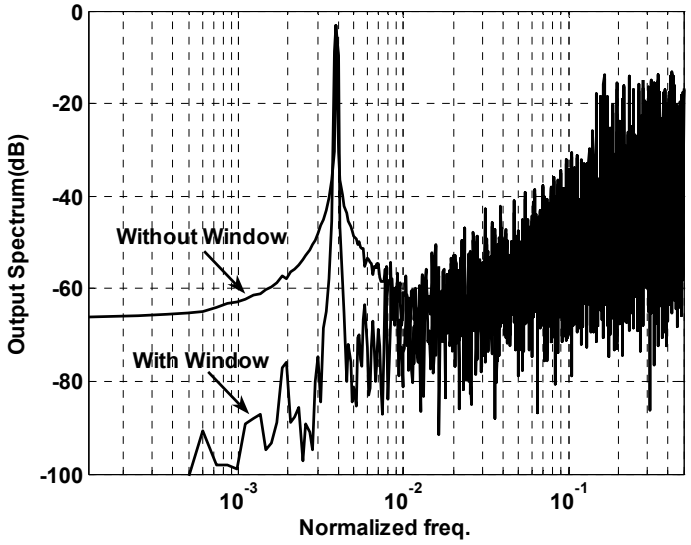


Figure 2.7: Output spectrum of the 1st-order Delta-Sigma modulator, with and without windowing.

The behaviors of the 1st-order Delta-Sigma modulator for constant input signals are also studied [Fri88] [Sch05]. Studies show that, for a constant rational number, e.g. a/b (a and b are integers), the modulator output will be a periodic sequence with a period of T. $T = b$ if both a and b are odd, and $T = 2b$ if a or b is even [Hei93]. The periodic sequences generated by rational constant inputs are called *limit cycles*. For the output spectrum with limit cycles, it is discrete, and it consists of tones generated at frequency f_s/T and its harmonics. Fig. 2.8 shows, for example, the output spectrum for a constant input of 1/100. Actually, even if the input signal is an irrational constant, quantization noise will also consist of tones [Can81] [Gra89].

Limit cycles also emerge for the slowly varying input voltages. The solution to limit cycles is either dithering the modulator, or increasing the modulator's order [Gra89] [Bra91] [Sch05].

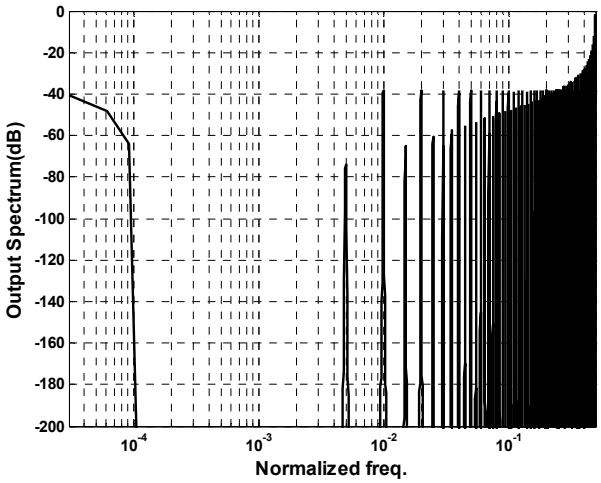


Figure 2.8: Output spectrum of the 1st-order Delta-Sigma modulator, for a constant input of 1/100.

2.2.5. General Model for Delta-Sigma Modulators

The order of the Delta-Sigma modulator can be increased by introducing more integrators in the loop filter. Higher order Delta-Sigma modulators can be implemented with various topologies [Cha90]. For the general case, the n[th]-order Delta-Sigma modulator can be modeled with a two-input one-output filter and a quantizer, which is shown in Fig. 2.9. The two inputs of the filter are connected to the input signal *X* and the feedback output signal *Y*, respectively. The modulator's NTF and STF can be expressed by *L* and *G*:

$$NTF(z) = \frac{1}{1 - L(z)},$$

$$STF(z) = \frac{G(z)}{1 - L(z)} = G(z) \cdot NTF(z). \tag{2.16}$$

Ideally, for an n[th]-order Delta-Sigma modulator, its NTF can be derived as:

$$NTF_n(z) = (1 - z^{-1})^n, \tag{2.17}$$

while the magnitude of its STF should be one at least in the signal band. Based on Eq. 2.16, NTF magnitudes with different orders are shown in Fig. 2.10. According to the figure, the higher order modulator shows more aggressive in-band noise-shaping effect.

In the similar way described in Section 2.2.3, the peak SNR of an n^{th}-order Delta-Sigma modulator can be derived as:

$$SNR_{n,P} = 10\log\frac{3(2n+1)(OSR)^{2n+1}}{2\pi^{2n}}. \tag{2.18}$$

Equation 2.18 indicates that, SNR increases 3(2n+1) dB with a double OSR.

Based on Eq. 2.18, peak SNRs with different orders and different OSRs can be estimated. Fig. 2.11, which shows the SNRs of 1^{st} to 5^{th}-order Delta-Sigma modulators, indicates that a Delta-Sigma modulator can achieve more than 20-bit resolution with proper order and OSR. One thing should be noted, the practical Delta-Sigma modulator always shows worse performance than the ideal one, due to many practical nonidealities, which will be discussed in the following chapters.

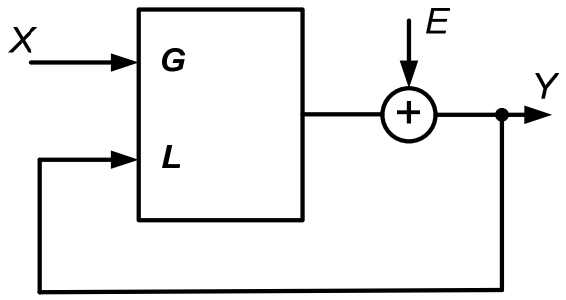


Figure 2.9: General linear model of the Delta-Sigma modulator.

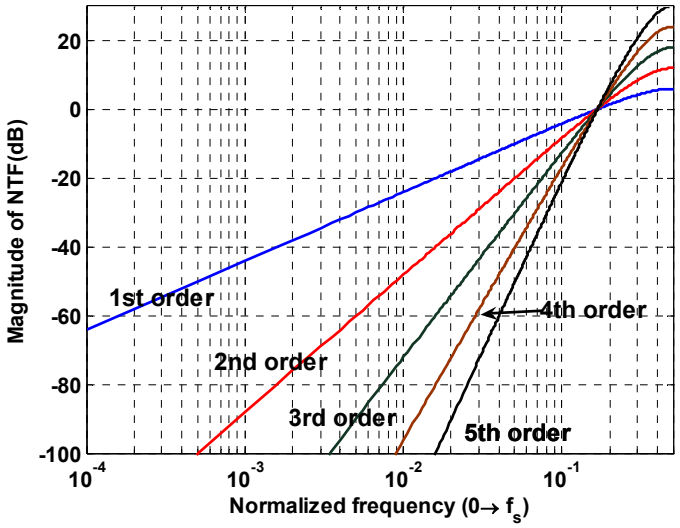


Figure 2.10: Ideal NTF magnitudes of the 1st to the 5th-order Delta-Sigma modulators.

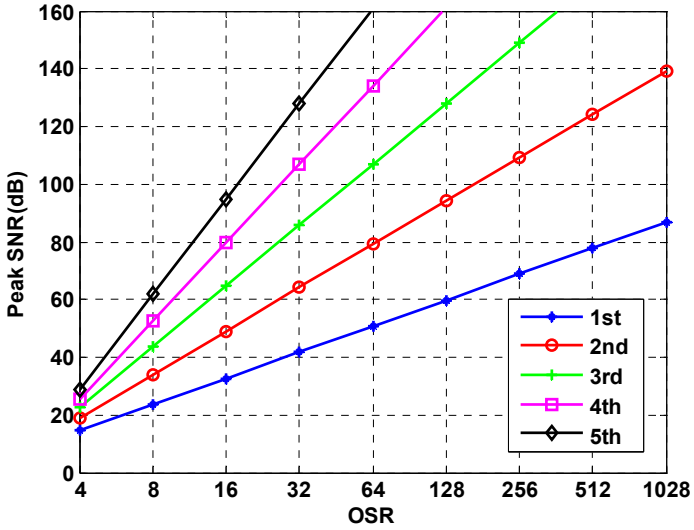


Figure 2.11: Ideal peak SNR vs. OSR plots of the 1st to the 5th-order Delta-Sigma modulators.

2.3 Different Types of Delta-Sigma Modulators

2.3.1. Discrete-Time and Continuous-Time Delta-Sigma Modulators

In the previous sections, input signals are sampled before the modulator, and hence, modulators work in Discrete-Time (DT), or, in *z*-domain. Delta-Sigma modulators can also work in continuous-time domain, if the sampler is moved into the loop filter, as shown in Fig. 2.12.

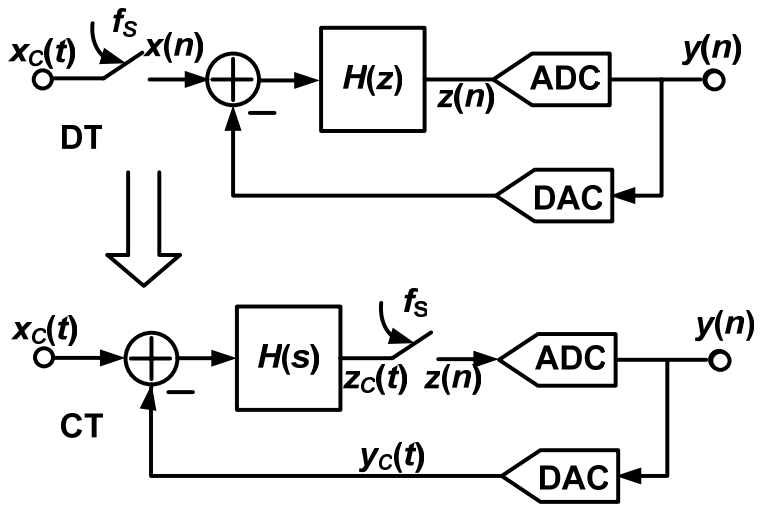


Figure 2.12: Translation from the discrete-time Delta-Sigma modulator to the continuous-time Delta-Sigma modulator.

DT Delta-Sigma modulators, which are based on Switched-Capacitor (SC) circuits, are more popular than CT Delta-Sigma modulators in the early years. DT Delta-Sigma modulators are attractive because they tend to be easier to implement, and to be easier to achieve good accuracy and good linearity [Sch05]. Furthermore, since the coefficient of SC filter is related to the capacitance ratio only, the SC circuit is independent on the clock rate, i.e. the clock frequency of a DT Delta-Sigma modulator can vary in a very wide range. In contrast, CT Delta-Sigma modulators suffer from many nonidealities, such as the clock jitter, the excess loop delay, and the

time-constant variation. However, CT Delta-Sigma modulators start to draw more and more attentions recently, due to the following reasons.

First, the CT Delta-Sigma modulator can achieve higher speed than the DT Delta-Sigma modulator. The sampling rate of a DT modulator is limited by the amplifier's unity gain frequency f_u. This is because that the settling performance is an exponential function of f_u/f_s for a switched-capacitor circuit [Gre86]. Generally speaking, to prevent the accumulation of errors that degrade the SNR, a condition of $f_u \geq 5f_s$ should be met [Jes01]. However, in a CT modulator, such exponential relation does not exist, and the limitation on the speed of the modulator is released [Nor97]. Roughly, the condition of $f_u=f_s$ is sufficient, which can be verified by the system-level simulations in Chapter 3. Therefore, the CT modulator can be operated much faster than the DT modulator.

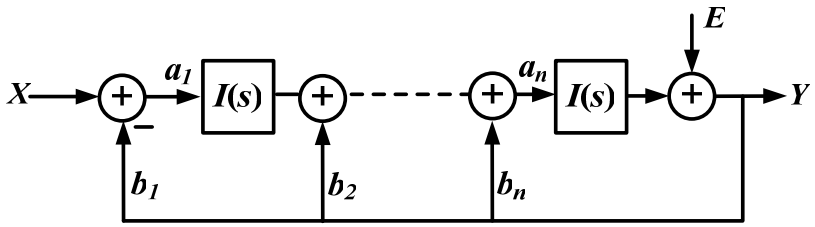
Second, the CT Delta-Sigma modulator tends to consume less power than the DT Delta-Sigma counterpart, mainly due to two reasons. 1) As discussed above, the CT loop filter relaxes the amplifier's settling requirement. 2) The CT loop filter eliminates the switches and their boost circuits, which are required in the low-voltage DT loop filter.

Third, due to its inherent anti-aliasing property, the CT Delta-Sigma modulator eliminates the anti-aliasing filter, which is required in the DT Delta-Sigma modulator. In other words, the CT Delta-Sigma modulator is equivalent to the DT Delta-Sigma modulator with a pre-filter ahead [Che00] [Sch05]. In addition, it is proven that, higher-order modulators have more anti-alias protection [Sch05].

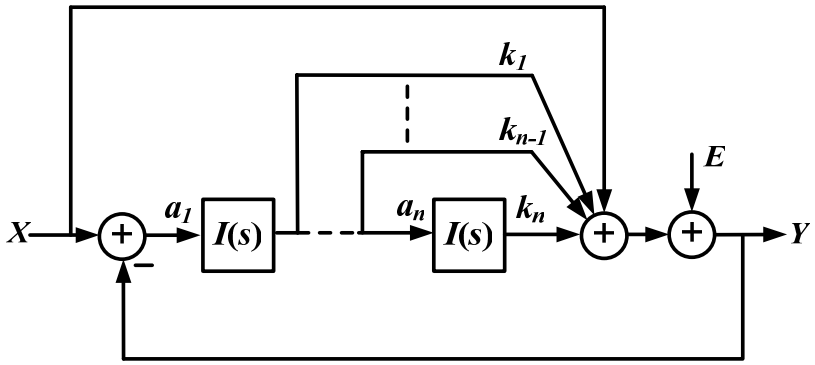
Fourth, the CT Delta-Sigma modulator has a potential advantage of noise performance. For switched-capacitor based DT Delta-Sigma modulators, its noise power is determined by kT/C, where C is the sampling capacitance. To suppress the noise power, the capacitance may be very large (~10^2 pF), which could cause nonlinear settling of input and nonlinear sampling in the input switch [Sig90].

2.3.2. Feedback and Input-Feedforward Delta-Sigma Modulators

As shown in Fig. 2.13, Delta-Sigma modulators can be implemented with the distributed feedback topology or the feedforward topology, where $I(s)$ equals $1/s$, representing the integrator.



(a)



(b)

Figure 2.13: Linear models for the n-th order Delta-Sigma modulator, with the distribute feedback topology (a), and the input-feedforward topology (b).

One main disadvantage of the feedback topology is that, since the Delta-Sigma modulator quantizes the amplitude of the input at the comparator, every integrator output contains the component of the input. This can be proven by deriving the loop filter's input, which is:

$$X - Y = X - (STF \cdot X + NTF \cdot E) = (1 - z^m) \cdot X - NTF \cdot E\,, \tag{2.19}$$

where E represents the quantization noise. Usually, STF contains at least one delay ($m \geq 1$), so the input contains not only the component of quantization noise, but also the component of the signal [Sil01]. The signal involvement results in large voltage swings at integrator outputs, leading to stringent linearity requirements to amplifiers, especially for the low-voltage applications [Sil01].

To solve this problem, the input-feedforward topology was introduced [Sil01]. As shown in Fig.2.13 (b), in this topology, the input signal X and integrator outputs are fed to the quantizer, and the output Y is fed back to the input of the 1st integrator only. The STF of the input-feedforward Delta-Sigma modulator can be easily derived [Sil01]:

$$STF_{I-FF}(s) = 1. \tag{2.20}$$

The input of the loop filter can be derived:

$$X(s) - Y(s) = X(s) - (STF_{I-FF}(s) \cdot X(s) + NTF_{I-FF}(s) \cdot E(s)) = -NTF_{I-FF}(s) \cdot E(s). \tag{2.21}$$

Equation 2.22 indicates that the loop filter contains the shaped quantization noise only. Without the input signal component, the internal voltage swings are significantly reduced, hence, the linearity requirements to amplifiers are relaxed. Fig. 2.14 compares the internal voltages of the 4th-order Delta-Sigma modulators with feedback and input-feedforward topologies. It is clearly shown that, in the input-feedforward topology, the internal signals are much smaller than that in the feedback topology. The reduced internal swings make the input-feedforward topology more suitable for the low-voltage low-power design, which will be discussed in Chapter 4 and Chapter 5.

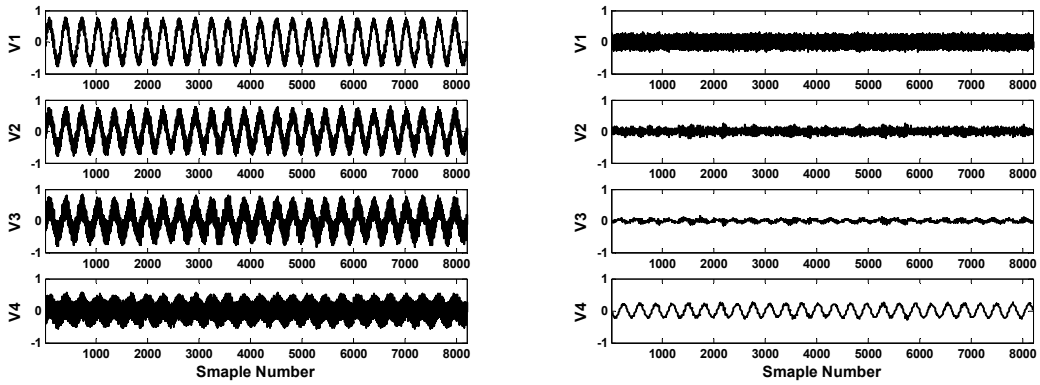


Figure 2.14: Internal waves of the 4th-order Delta-Sigma modulators, with the feedback topology (a), and with the input-feedforward topology (b). Vi is the i-th integrator's output.

2.4 Literature Review on Low-Voltage Low-Power Delta-Sigma Modulators

The development of low-power electronics has become an important issue for both academic institutes and industrial companies since the early 1980's [Gol00]. With the growing market of the portable products and the emergence of the concept of "Green IT", this issue becomes more and more important in recent years. For commercial portable applications (e.g. mobile phones, handheld multimedia, etc.), lower power directly leads to the longer battery lifetime and/or smaller battery size (product weight). Furthermore, low-power consumption also helps to reduce the cost of heat removal, which is very important for high-integration circuits, even in non-portable applications [Raj02]. In addition, due to the increasing attention to the environmental protection, power consumption has become a critical design metric for the companies to fulfill their legal and moral obligations [IBM07].

2.4.1 Low-Voltage Low-Power Design Challenges

The low-power trend for the digital circuitry has been achieved by the continuing scaling CMOS technology. With the dimension scaling, supply voltage also scales down proportionally to fullfil the reliability requirement by keeping the electrical field at the same level in the device. More important, the lower voltage directly reduces the power consumption of the digital circuitry [Ben01].

For the analog-to-digital converter, its supply is required to decrease to the same level as the digital supply, at least in SOC applications. By integrating all the digital, analog and even radio frequency (RF) circuits on a chip, SOC applications tend to achieve low cost, small size and weight with multifunction performance. Furthermore, due to the elimination of the wire bonding, SOC applications tend to achieve high reliability and broad-band performance [Puc81].

However, ADCs only marginally benefit from the CMOS scaling down technology with respect to following aspects.

First, the minimum size normally cannot be used for analog transistors due to the constraint of offset voltage [Lan98]. The offset is caused by the mismatch. The standard deviation of mismatch is approximately in inverse proportion to the transistor area, i.e. the product of the width and the length [Pel89]. Thus, transistors with much larger than the minimum size are usually required in ADCs, especially in those converters whose resolutions depend directly on matching, such as pipelined ADCs. Since the minimum size is not allowed, ADCs cannot achieve the maximum speed/bandwidth that the process provides.

Second, additional current is needed to maintain the same signal-to-thermal noise ratio in the low-supply operation [Vit94]. With the reduced voltage, the signal swing decreases. Consequently, the signal power decreases, which can be expressed as:

$$P_S \propto V_{DD}^2. \tag{2.22}$$

If the noise floor is kept unchanged, the dynamic range decreases. The sources that contribute to the noise floor include resistors, amplifiers, and some circuit nonidealities. In a SC based DT Delta-Sigma modulator, the noise power, as mentioned in Section 2.3.1, can be expressed as the well-known formula:

$$P_{NR,SC} = \frac{kT}{C} \propto \frac{1}{C}, \tag{2.23}$$

where k is Boltzmann constant, T is the temperature, and C is the sampling capacitance.

In a RC based CT Delta-Sigma modulator, the noise power of the input resistor can be expressed as:

$$P_{NR,RC} = 4kT \cdot R \cdot BW, \tag{2.24}$$

where BW is the signal bandwidth. Since the product of integration resistance and capacitance is constant (see Chapter 4), Eq. 2.24 can also be translated into:

$$P_{NR,RC} \propto \frac{1}{C}, \tag{2.25}$$

Eq. 2.23 and Eq. 2.25 indicate that, the noise power of the resistor, no matter it is from a SC based or a RC based Delta-Sigma modulator, is inversely proportional to the relative capacitance. Consequently, to keep SNR unchanged, the capacitance of the input stage need to be increased by four times for a half reduction of the supply voltage, which leads to increased current consumption and increased area.

The situation for amplifiers is similar. For the input transistor of an amplifier, its thermal noise is inversely proportional to its transconductance, and its flicker noise is inversely proportional to its area (product of its width and length). Therefore, to keep SNR unchanged in a reduced-supply Delta-Sigma modulator, the transconductances and the sizes of the input amplifier need to be increased to lower down both the thermal noise power and the flicker noise power. Due to the increased transconductance, the current consumption is increased.

Third, voltage headrooms are greatly reduced in low-voltage ADCs. As the supply voltage decreases, the threshold voltage and the drain-source saturation voltage do not scale down at the same rate. The threshold voltage needs to be kept at a certain value to limit the leakage current. For the drain-source voltage, a good estimation of 0.15 V is required to maintain transistors working in saturation region [Tsi99]. In this case, the amplifier's input range, and output range are greatly reduced with the reduced supply [Yan00], especially in cascade circuits. The constraint of signal swings may bring many problems in the analog signal processing. For example, in Delta-Sigma modulators, the integrator coefficients are required to be reduced in order to keep a good linearity performance with the smaller signal swing. In the RC based CT Delta-Sigma modulator, the reduced integrator gain leads to the larger integration capacitance, if the integration resistance is kept unchanged. The larger integration capacitance will consume more current. Another example arises from common-mode feedback circuits. Because the input

range of a CMFB circuit is reduced to a very small value under the low-voltage operation, any deviation of the common-mode voltage may lead the CMFB circuit out of work.

Fourth but not the last, the gain of an amplifier tends to be degraded due to the reduced output resistance with the scaling down CMOS technology. It is well-known that the output resistance of a transistor can be expressed as:

$$r_o = \frac{\Delta V_{DS}}{\Delta I_{DS}} = \frac{V_A}{I_{DS}}, \tag{2.26}$$

where V_A is the Early voltage, defined as [Gra01]:

$$V_A == \frac{I_{DS}}{\partial I_{DS} / \partial V_{DS}} \propto L_{eff}, \tag{2.27}$$

where L_{eff} is the effective channel length. Eq. 2.26 and Eq. 2.27 indicate that the output resistance decreases with the channel length. Furthermore, the limited drain-source voltage also degrades the output resistance [Raz00].

To sum up, the low-power analog designs under low-voltage operation is a necessary target but full of challenges for the designers. The next section will focus on low-voltage low-power solutions for Delta-Sigma modulators.

2.4.2 Low-Voltage Low-Power Design Techniques in Delta-Sigma Modulators

This section will review the available techniques, which arise from the circuit level, the system level and the process level, for designing low-voltage low-power Delta-Sigma modulators.

A. *Voltage Boosting Technique*

Since the threshold voltage of the transistor does not scale at the same rate as the supply voltage does, it leads to difficulties in driving switches in the low-voltage analog circuits. The on-resistance of a transistor switch can be approximately derived as:

$$r_{on} = \frac{\partial V_{DS}}{\partial I_{DS}} \approx \frac{L}{\mu C_{ox} W (V_{GS} - V_{TH} - V_{DS})}. \tag{2.28}$$

For example, assuming the threshold voltage, the supply voltage and the signal common-mode are 0.3 V, 1 V, and 0.5 V respectively, there is only 0.2 V left for the gate to overdrive. Furthermore, the case can be worse if body effect and signal/process variation effect are taken into consideration. The small overdriving voltage directly leads to the large on-resistance, which may degrade the speed performance of the circuit [Cho95]. According to Eq. 2.28, increasing the transistor width can help to decrease the on resistance, but result in larger parasitic capacitance and larger clock feedthrough [Cho95] [Cro94].

To solve this problem, the simplest way is to increase the gate voltage of the transistor. The gate voltage can be increased on-chip by voltage multipliers, or bootstrapping technique. A simple clock booster is shown in Fig. 2.15 [Au97], by which the output voltage can jump to $(2V_{DD}-V_{TH})\cdot C_1/(C_1+C_{load})$. Voltage multiplier technique is widely used in switched-capacitor based Delta-Sigma modulators [Gri96] [Des01] [Par09].

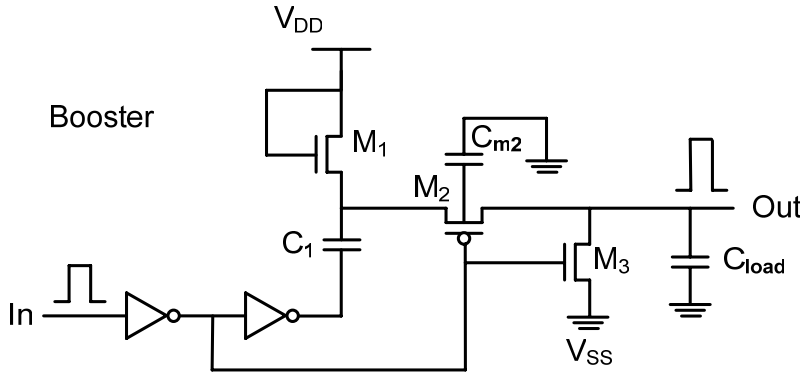


Figure 2.15: Schematic of a clock booster.

The drawbacks of the voltage multiplier include: 1) The multiplier circuit is noisy and not compatible with sensitive analog circuits. If the boosted voltage is used as the supply voltage, the power supply rejection issue should be taken care [Raj02]. 2) The multiplier circuit consumes

additional power and area. 3) Sometimes, boosting voltage beyond the supply may lead to reliability problems, especially for sub-micron CMOS processes [Yan00].

B. *Sub-Threshold Technique*

Fig. 2.16 shows the simulated current versus gate-source voltage curve. When the gate-source voltage is right below its threshold voltage, the channel is partially or weakly inverted, which generates some electron charges that can carry some current. This region is known as sub-threshold, or weak inversion region. Sub-threshold designs have obtained many attentions in recent years due to the need for low voltage and low power applications [Vit77] [Per08] [Joc09] [Zou09] [Vit09], and also in Delta-Sigma modulator [Roh09].

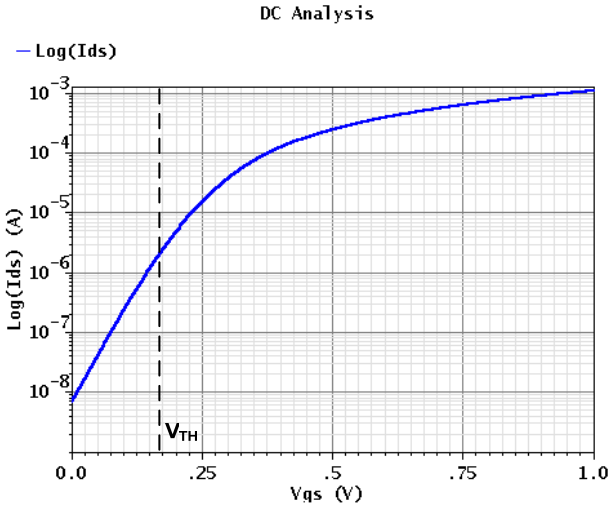


Figure 2.16: Current versus gate-source voltage curve in a NMOS transistor.

Under the sub-threshold region, the MOS transistor behaves like a bipolar transistor. That is, the sub-threshold current varies exponentially with the gate-source voltage, which can be expressed as [All87]:

$$I_{DS,ST} = I_{D0}\frac{W}{L}\exp(\frac{V_{GS}-V_{TH}}{nkT/q}), \tag{2.29}$$

where I_{D0} is a process-dependant parameter, n is the sub-threshold slope factor, k is Boltzmann constant, T is the temperature, q is the charge of an electron. As shown in Fig. 2.16, the sub-threshold region provides the highest slope, and therefore provides maximum current efficiency for a MOSFET.

Under the sub-threshold region, the transconductance can be derived as:

$$g_{m,ST} = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{I_{DS}}{nkT/q}. \tag{2.30}$$

And the ratio of transconductance to the drain-source current is:

$$\frac{g_{m,ST}}{I_{DS,ST}} = nkT/q. \tag{2.31}$$

Fig. 2.17, which shows the simulated curve of the transconductance versus the drain-source current ratio, indicates that the sub-threshold region also provides the maximum g_m/I_{DS}. In this case, sub-threshold circuits can achieve highest gain, or can achieve highest bandwidth, for a given current. In addition, operating under sub-threshold region, MOSFET requires lower headroom, which leads to lower supply voltage, and/or larger signal swings even in cascaded structures [Raj02] [Per08].

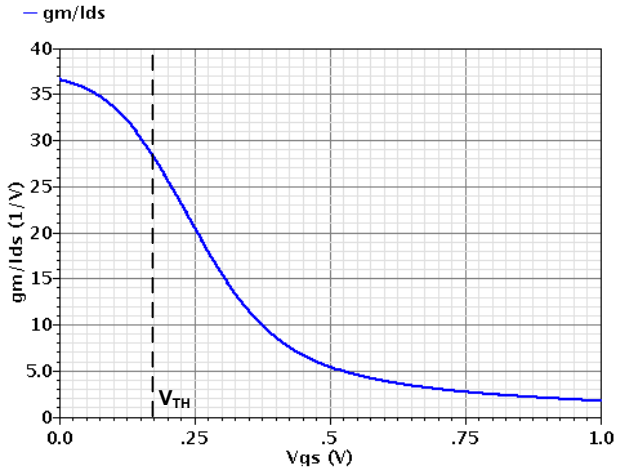


Figure 2.17: Simulated curve of the g_m/I_{ds} versus the gate-source voltage.

However, under the sub-threshold region, absolute values of currents and transconductances are very low, which results in very low speeds and high noise. Thus, the sub-threshold technique is only suitable for applications with not-high SNRs and low speeds, such as biomedical and biotelemetry applications. Furthermore, considerations may need to be taken for the drain/source-substrate currents, since they may not be negligible compared to the drain-source current when the transistor works in the sub-threshold region.

C. *Floating-Gate Technique*

Another technique for Low–supply analog designs is floating-gate. The layout, schematic symbol and equivalent circuit of a two-input floating-gate MOSFET are shown in Fig. 2.18. As shown in the figure, there are two kinds of polysilicon layers, one is for the floating gate, and the other is for the control gate. As the name implies, the floating gate is isolated from any dc path to ground by S_iO_2, which prevents charges on the floating gate from leaking [Ram95].

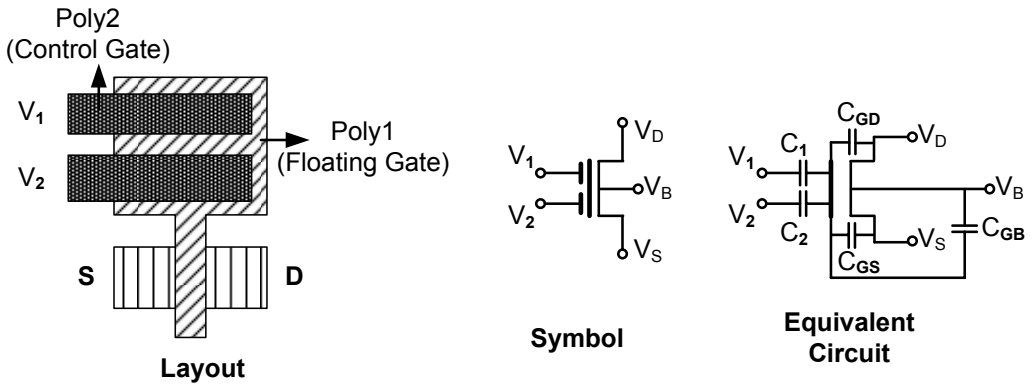


Figure 2.18: Layout/symbol/equivalent circuit of a two-input floating-gate MOSFET.

The external voltages V_1 and V_2 control the transistor through capacitance coupling. Together with other coupling factors, the voltage of the floating gate can be derived with the help of the equivalent circuit in Fig. 2.18 [Yan00]:

$$V_{FG} = (Q_{FG} + C_{GD}V_D + C_{GS}V_S + C_{GB}V_B + \sum_{i=1}^{2} C_i V_i) / C_\Sigma , \quad (2.32)$$

where Q_{FG} is the static charge on the floating gate, and C_Σ is the total capacitance seen from the floating gate.

One promising characteristic of the floating-gate technique is that the threshold voltage can be tuned by programming the static charge Q_{FG} on the floating gate. Q_{FG} can be programmed by ultra-violent light shining, Fowler-Nordheim tunneling, and hot-electron injection [Yan00] [Has01]. With the programming circuit, the threshold voltage can be tuned lower than its standard value, and thus ultra low-voltage analog design is possible [Ber01] [Mun01] [Ram01] [Has01], including Delta-Sigma modulators [Per02] [Per04].

However, there are some drawbacks that limit the popularity of the floating-gate technique [Yan00] [Raj02]. 1) According to Eq. 2.32, the voltage of the floating gate depends on the coupling from the drain voltage, and therefore the output impedance of the floating-gate transistor is less than that of the conventional MOSFET. In this point, the dc gain of the floating-gate transistor is low. 2) The equivalent transconductance of the floating-gate transistor is also lower than that of the conventional counterpart, which results in higher thermal noise. 3) The threshold programming may need complex programming circuit and high programming voltage. 4) The floating-gate technique tends to be area consuming, since the area of the floating gate is usually much larger than the channel area. 5) This technique also requires process support, which tends to increase the chip cost.

D. *Body-Driven Technique*

Till now, in all the low-voltage techniques discussed, the transistor is driven by the gate voltage. As discussed above, the gate-driven transistor suffers from the limited signal range, due to the constraint from its threshold voltage. For example, as shown in the left of Fig. 2.19, for a gate-driven transistor, to work in the saturated inversion region, its input common-mode voltage should satisfy the following equation:

$$V_{IN,CM} = V_G = V_{GS} + V_S \geq V_{DSat} + V_{THN} + V_S \,. \tag{2.33}$$

Assuming this transistor is an input of a differential amplifier, and assuming $V_{DSat} = V_S = 0.1$ V, $V_{THN} = 0.3$ V, the common-mode voltage of the transistor should be larger than 0.5 V, and the supply voltage should be larger than 1 V if the common-mode voltage is assumed as half of the supply.

The constraints from the threshold voltage and from the drain-source saturation voltage can be greatly relaxed if the transistor is driven by its body. As shown in the right of Fig. 2.19, in a body-driven transistor, the drain and source are connected normally, the gate is a dc biasing voltage, and the input is applied at the body terminal.

Figure 2.19: Gate-driven NMOS transistor (left), and body-driven NOMS transistor.

The advantages of this technique are as follows.

First, a large input range can be achieved, because the depletion junction between the body and the source allows negative, zero and slightly positive bias voltage. As an example, for the body-driven NMOS transistor in Fig. 2.19, its input range can be from 0 V to V_S+0.65 V, where 0.65 V is the voltage that can activate a bipolar device. This is almost a rail-to-rail range for a sub-1V circuit. In addition, forward-biasing of the body-source junction can also be used to lower down the threshold voltage. The threshold voltage dependency on the body-source voltage can be expressed as [Che96]:

$$V_{TH} = a_1 + a_2\sqrt{a_3 - V_{BS}}\,, \tag{2.34}$$

where a_1, a_2, and a_3 are three process-dependent parameters.

Second, the supply voltage of a body-driven circuit can be reduced to a very small value, which is slightly higher than the threshold voltage. According to Eq. 2.33, a supply voltage not less than V_G is possible for a body-driven circuit, which is almost half of the gate-driven counterpart.

The body-driven technique has been applied many analog circuits in literature [Mul95] [Che96] [Bla98] [Cha05] [Cha07]. One application in the Delta-Sigma modulator was reported in [Pun07]. In this design, the supply voltage is reduced to 0.5 V, which exactly equals to the threshold voltage.

The body-driven technique also suffers from some drawbacks.

First, the body-driven technique requires isolated body terminals. For CMOS circuits, the tripe-well process is needed to drive the bodies of both PMOS and NMOS transistors, which increases the cost of the chip greatly.

Second, bulk-driven circuits have poor gain and noise performance due to their smaller transconductance. The transconductance of a bulk-driven MOSFET is derived as [Bla98]:

$$g_{mb} = \frac{di_{DS}}{dv_{BS}} = \frac{\gamma g_m}{2\sqrt{2\phi_F - V_{BS}}} = \eta \cdot g_m , \tag{2.35}$$

where g_m is the gate-driven transconductance, γ is the body-effect coefficient, and Φ_F is electrostatic potential. Typically, the ratio of g_{mb} to g_m (η in Eq. 2.35) is from 20% ~ 40% [Bla98]. The smaller body-driven transconductance results in lower gain and higher thermal noise.

Third, body-driven circuits tend to achieve lower intrinsic gain-bandwidth due to its lower transconductance and higher input capacitance. For a gate-driven circuit, its intrinsic gain-bandwidth can be expressed as:

$$f_{T,GD} \approx \frac{g_m}{2\pi C_{gs}}, \tag{2.36}$$

where C_{gs} is the gate-source capacitance. And for a body-driven circuit, its intrinsic gain-bandwidth can be expressed as [Bla98]:

$$f_{T,BD} \approx \frac{g_{mb}}{2\pi(C_{bs}+C_{bsub})} = \frac{\eta g_m}{2\pi(C_{bs}+C_{bsub})}, \tag{2.37}$$

where C_{bs} is the bulk-source capacitance, and C_{bsub} is the well-substrate capacitance. For saturated strong inversion MOSFETs, the two bandwidths can be approximately related as [Bla98]:

$$f_{T,BD} \approx \frac{\eta}{3.8} f_{T,GD}. \tag{2.38}$$

Fourth, matching between the two transistors in a body-driven circuit may be a problem, because MOSFETs are fabricated in different wells.

Fifthly, theoretically latch-up may occur due to the forward biasing of body-source voltage. However, as discussed above, this problem can be neglected if the transistor is only slightly forward biased.

E. *Other Low-Voltage Low-Power Techniques*

Many other techniques have been reported in recent publications. Among this, one technique is gain-bandwidth compensation technique [Ort04]. In [Ort04], system-level optimization is utilized, so that gain-bandwidth of the amplifier can be reduced below sampling frequency. However, in practical design, gain-bandwidth is only one of many points that should be considered. Besides it, the slew rate, the noise and so on are also needed to be considered. For example, usually a large input transconductance is required for the 1st amplifier to achieve an enough low thermal noise, and thus the gain-bandwidth, which is proportional to g_m, cannot be made too small. In addition, gain-bandwidth compensation technique needs additional feedback loop, which may increase the design complexity. Another technique is the assisted opamp technique [Pan10]. By using additional assisted circuit, the slew rate requirement of the amplifier can be relaxed. Another technique is to use inverter-based switched-capacitor circuit to replace the traditional amplifier [Vel08] [Cha08]. Although the inverter-based circuit has limited performance, it is suitable for low-voltage low-power design.

2.5 Conclusion

By employing the oversampling technique, the noise-shaping technique, and the digital filtering technique, Delta-Sigma ADCs show many advantages, such as relaxed requirements on anti-aliasing filter and analog circuitry, high resolution, and good compatibility to digital circuitry. This chapter covers the basics of the Delta-Sigma modulator. The operation principle is presented based on the ideal simplest 1^{st}-order Delta-Sigma modulator, and is extended to a general model for higher-order modulators. Different types of Delta-Sigma modulators are introduced, including the discrete-time and the continuous-time topologies, the feedback and the input-feedforward topologies. A literature review for the low-voltage low-power techniques for Delta-Sigma modulator is also included.

In the following chapters, design issues of continuous-time Delta-Sigma modulators will be discussed. The next chapter will present system-level designs and considerations.

CHAPTER 3

SYSTEM-LEVEL DESIGNS AND SIMULATIONS OF CONTINUOUS-TIME DELTA-SIGMA MODULATORS

3.1 Introduction

In Chapter 2, basics of Delta-Sigma modulators are discussed, including the operations and the topologies of Delta-Sigma modulators. In the following chapters, detailed design issues will be addressed.

A simplified flow chart for designing a Delta-Sigma modulator is shown in Fig. 3.1. The Delta-Sigma modulator design is carried out on the system level first, and followed by the circuit level design. This is an iterative process between the two levels. Compared to the circuit-level simulation, the system-level simulation is conducted in a more abstract way, where much less parameters are needed to be dealt with. Therefore, the system-level simulation has higher timing efficiency, but lower accuracy than the circuit-level simulation.

In this chapter, system-level designs and simulations of continuous-time Delta-Sigma modulators will be discussed. System-level designs include the topology selection, the coefficient determination (NTF calculation), and so on. Designing the CT transfer function is more difficult than designing the DT transfer function, since the traditional system-level design methodologies and tools are based on discrete-time loop filters [Dia91] [Bri99] [Cha01] [Fan03]. In this case, a recommended procedure for the CT design is to find a DT transfer function first, and then, map it to the equivalent CT transfer function [Sch96] [Nor97] [Che00] [Baj04]. System-level simulations include simulations for SNQR, DR, stability, internal swings, nonidealities, and so on.

As mentioned in Chapter 2, continuous-time Delta-Sigma modulators suffer from many nonidealities, such as the clock jitter, the excess loop delay, and so on. Those nonidealities may seriously degrade the performances of the modulators, and hence, necessary considerations must be paid to them.

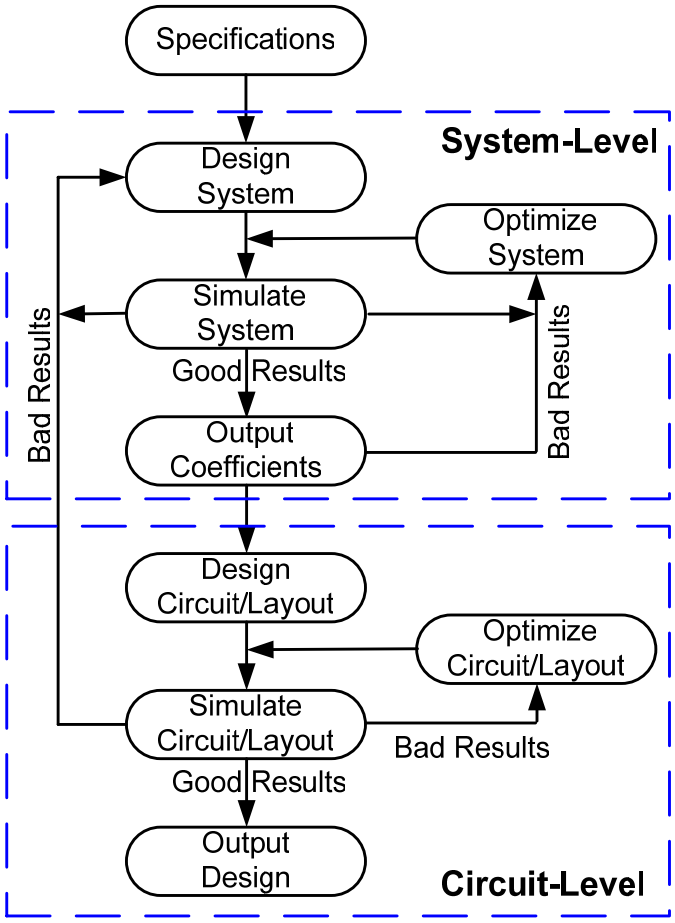


Figure 3.1: Simplified flow chart for designing Delta-Sigma modulators.

The organization of this chapter is as follows. Section 3.2 presents the method of mapping the DT

Delta-Sigma modulator to the equivalent CT Delta-Sigma modulator. In Section 3.3, a Simulink based model will be proposed for the CT Delta-Sigma modulator simulations, and then various nonidealities will be discussed.

3.2 Exploiting the Equivalent Continuous-Time Delta-Sigma Modulator

The models for the DT modulator and the CT modulator are shown in Fig. 3.2. It is clear that, the input signal is sampled before the loop filter in the DT Delta-Sigma modulator, and is sampled before the quantizer in the CT Delta-Sigma modulator. To convert the discrete-time output to the continuous-time signal before it is fed back to the input, the CT DAC (see Fig. 3.2) acts as a discrete-to-continuous converter. Normally, the zero-order-hold pattern is adopted in the CT DAC, which can be expressed as the time-limited rectangular pulses [Che00]:

$$r_{(\alpha,\beta)}(t) = u(\alpha) - u(\beta) = \begin{cases} 1, \alpha \le t < \beta, 0 \le \alpha < \beta \le 1 \\ 0 \end{cases}, \tag{3.1}$$

where the clock period is normalized to 1. The zero-order-hold DAC pulse can also be expressed in the *s*-domain [Che00]:

$$R_{(\alpha,\beta)}(s) = \frac{\exp(-\alpha s) - \exp(-\beta s)}{s}. \tag{3.2}$$

There are three main types of DAC pulses: non-return to-zero (NRZ), return to-zero (RZ), and half-delayed return to-zero (HRZ). The three DAC pulses and their Laplace transforms are shown in Table 3.1.

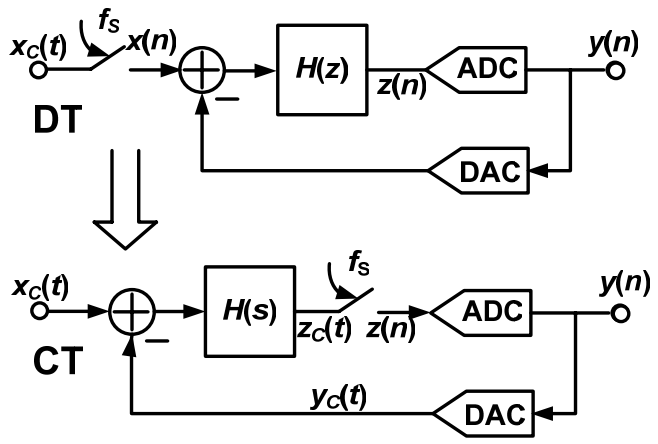
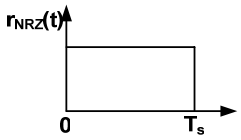
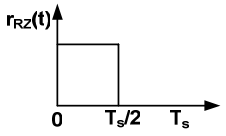
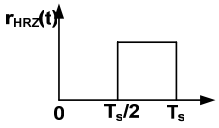


Figure 3.2: Models for the discrete-time Delta-Sigma modulator and the continuous-time Delta-Sigma modulator.

Table 3.1 DAC pulses and their s-domain responses.

	NRZ	RZ	HRZ
(α, β)	(0, 1)	(0, 0.5)	(0.5, 1)
Impulse response			
Transfer function	$R_{NZ}(s) = \frac{1-\exp(-T_S s)}{s}$	$R_{RZ}(s) = \frac{1-\exp(-T_S s/2)}{s}$	$R_{(\alpha,\beta)}(s) = \frac{\exp(-T_S s/2)-\exp(-T_S s)}{s}$

As mentioned in Section 3.1, the CT Delta-Sigma modulator is designed by mapping it from an equivalent DT Delta-Sigma modulator. The open loops of the DT and CT Delta-Sigma modulators are shown in Fig. 3.3. According to the *symbol pulse-invariance* transformation proposed in [Gar86], the open-loop impulse responses of the CT and the DT modulators should be the same at sampling points, if the two modulators are equivalent. Such a relation can be expressed as [Thu91]:

$$Z^{-1}\{H(z)\} = L^{-1}\{R_{DAC}(s)H(s)\}|_{t=n}, \tag{3.3}$$

where $R_{DAC}(s)$ is the transfer function of the CT DAC.

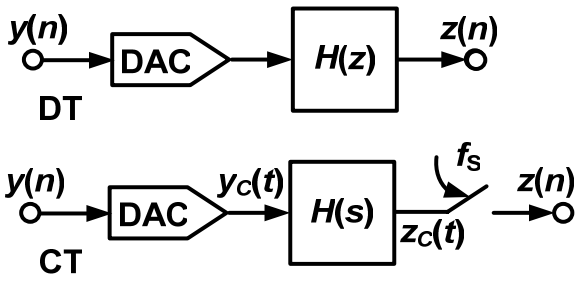


Figure 3.3: Open-loops of the discrete-time Delta-Sigma modulator and the continuous-time Delta-Sigma modulator.

The equivalent CT transfer function can be developed in state-space by using Matlab tool [Sch96]. The translation procedure is shown in Fig. 3.4. First, the DT transfer function is translated to the state-space matrix. And then, the DT state-space matrix is converted to the CT state-space matrix. Finally, the CT state-space matrix is converted to the CT transfer function.

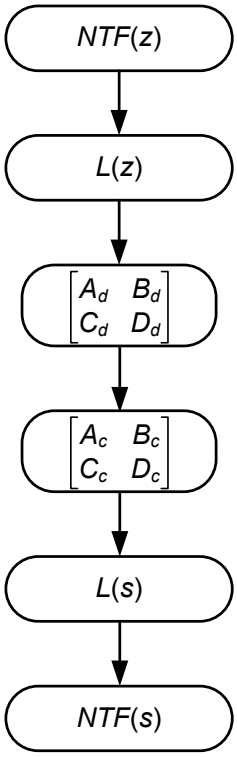


Figure 3.4: Flow chart for exploiting the equivalent CT Delta-Sigma modulator from a DT Delta-Sigma modulator.

As an example, let's translate a 2nd-order DT Delta-Sigma modulator to its equivalent CT modulator. Using Eq. 2.18, the NTF and the loop filter transfer function of the 2nd-order DT Delta-Sigma modulator is:

$$NTF_2(z) = (1 - z^{-1})^2, \tag{3.4}$$

According to Eq. 2.16, its loop filter transfer function can be derived as:

$$L_2(z) = \frac{-2z + 1}{(z-1)^2}. \tag{3.5}$$

And its block diagram is shown in Fig. 3.5(a).

Assuming the DAC pulse is NRZ, the Matlab commands for the mapping are as follows [Che00]:

```
[Ad, Bd, Cd, Dd] = tf2ss ([0 -2 1], [1 -2 1]); % translate L2(z) to the state-space
SSd = ss (Ad, Bd, Cd, Dd, 1); % generate state-space model of L2(z)
SSc = d2c (SSd); % convert the DT state-space to the CT state-space
[Numc, Denc] = ss2tf (SSc.a, SSc.b, SSc.c, SSc.d) % generate CT transfer function
```

And Matlab returns:

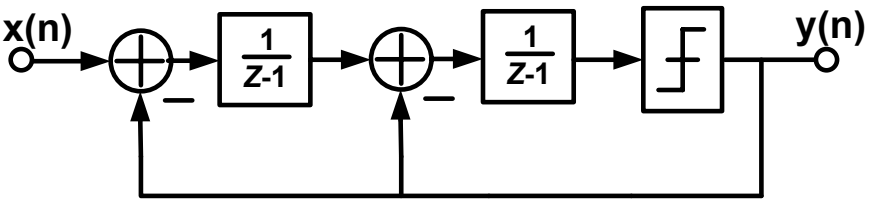
```
Numc =      0   -1.5000    -1.0000
Denc = 1.0000    0.0000    -0.0000
```

which indicates the transfer function of the equivalent CT loop filter is:

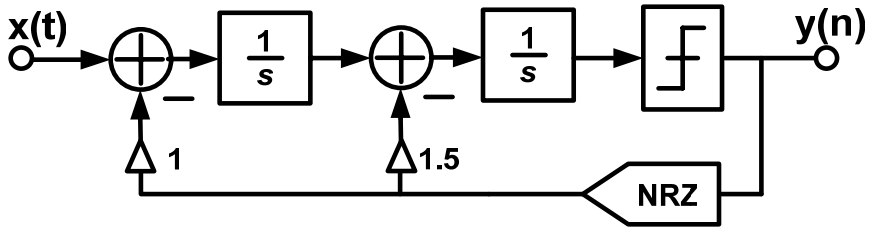
$$L_{2\_NRZ}(s) = \frac{-1.5s - 1}{s^2}. \tag{3.6}$$

And its block diagram is shown in Fig. 3.5(b). Its NTF is thus derived as:

$$NTF_{2\_NRZ}(s) = \frac{s^2}{s^2 + 1.5s + 1}. \tag{3.7}$$



(a)



(b)

Figure 3.5: Block diagram of the 2nd-order Delta-Sigma modulator, with the discrete-time implementation (a), and with the continuous-time implementation (b).

For the general DAC case with variables α and β (see Eq. 3.1 and Eq. 3.2), its CT state-space matrix is same as the NRZ state-space matrix except the B parameter [Nor97], which is represented as `SSc.b` in the previous Matlab codes. The B parameter for the general DAC pulse can be expressed as [Nor97]:

$$B_{C(\alpha,\beta)} = \frac{(SSd.a - I)\cdot B_{C(0,1)}}{\exp[SSc.a\cdot(1-\alpha)] - \exp[SSc.a\cdot(1-\beta)]}, \tag{3.8}$$

where $B_{C(0,1)}$ represents the B parameter for the NRZ case. One thing should be noted is that, for the 2nd-order modulator, $SSc.a$ is singular:

$$SSc.a = \begin{bmatrix} 1 & -1 \\ 1 & -1 \end{bmatrix}, \tag{3.9}$$

which leads to a zero denominator in Eq. 3.8. This case can be avoided by adding a small enough value on the SSc.a matrix [Che00]. The commands for the general DAC case are shown below:

```
[Ad, Bd, Cd, Dd] = tf2ss ([0 -2 1], [1 -2 1]);
SSd = ss (Ad, Bd, Cd, Dd, 1);
```

```
SSc = d2c(SSd);

Ac = [1 -1; 1 -1.0001]; % avoid singular SSc.a in the 2nd-order modulator

SSc.b = inv(expm(Ac*(1-alfa))-expm(Ac*(1-beta)))*(SSd.a-eye(2))*SSc.b;

[Numc, Denc] = ss2tf (SSc.a, SSc.b, SSc.c, SSc.d)
```

For the RZ-DAC case, $\alpha = 0$, $\beta = 0.5$, and Matlab returns:

```
Numc =      0   -2.5000    -2.0000

Denc = 1.0000    0.0000    -0.0000
```

which indicates the transfer function of the CT loop filter with RZ DAC is:

$$L_{2\_RZ}(s) = \frac{-2.5s - 2}{s^2}, \tag{3.10}$$

and its NTF is thus derived as:

$$NTF_{2\_RZ}(s) = \frac{s^2}{s^2 + 2.5s + 2}. \tag{3.11}$$

For the HRZ-DAC case, $\alpha = 0.5$, $\beta = 1$, and Matlab returns:

```
Numc =      0   -3.5000    -2.0000

Denc = 1.0000    0.0000    -0.0000
```

which indicates the transfer function of the CT loop filter with HRZ DAC is:

$$L_{2\_HRZ}(s) = \frac{-3.5s - 2}{s^2}, \tag{3.12}$$

and its NTF is thus derived as:

$$NTF_{2\_HRZ}(s) = \frac{s^2}{s^2 + 3.5s + 2}. \tag{3.13}$$

3.3 Simulations of Nonidealities in CT Delta-Sigma Modulators

3.3.1 Simulink-Based Model for the Continuous-Time Delta-Sigma Modulator

As mentioned in Section 3.1, the traditional simulation tools deal with DT Delta-Sigma modulators only [Dia91] [Bri99] [Cha01] [Fan03]. In [Ben98], a Matlab based tool was proposed for CT Delta-Sigma modulators, but it is based on DT equivalent models. In this section, simple Simulink-based CT models are proposed for simulating CT Delta-Sigma modulators directly.

As an example, Fig. 3.6 shows the Simulink-based model for the 2nd-order CT Delta-Sigma modulator. In the model, the loop filter comprises two continuous-time *Integrator* blocks and two *Gain* blocks, and the quantizer comprises a *Zero-Order-Hold* block and a *Switch* block. The DAC pulse is modeled as the product of the quantizer output and a DAC multiplier, as shown in Fig. 3.7. For the NRZ DAC pulse, the DAC multiplier is 1. Actually, for CT modulators with NRZ pulses, its quantizer output can be connected to the input directly. For the RZ or HRZ DAC pulses, the relevant multiplier is generated by a *Pulse Generator* block built in Simulink. By adjusting the delay time of the *Pulse Generator* block, the RZ or the HRZ pulse can be generated. In our system-level simulation, all the clock periods are normalized to 1, the delay time for RZ is 0, and for HZ is 0.5. The output waves of those three DACs are shown in Fig. 3.8.

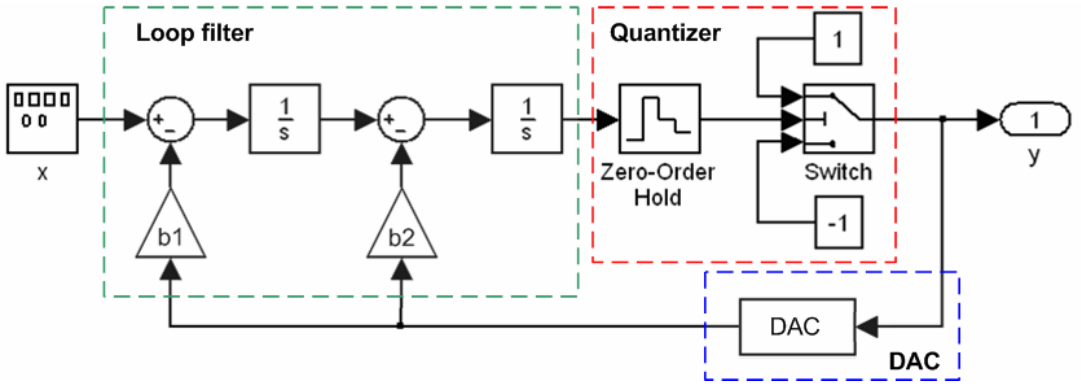


Figure 3.6: Block diagram of the Simulink-based model for the 2nd-order continuous-time Delta-Sigma modulator.

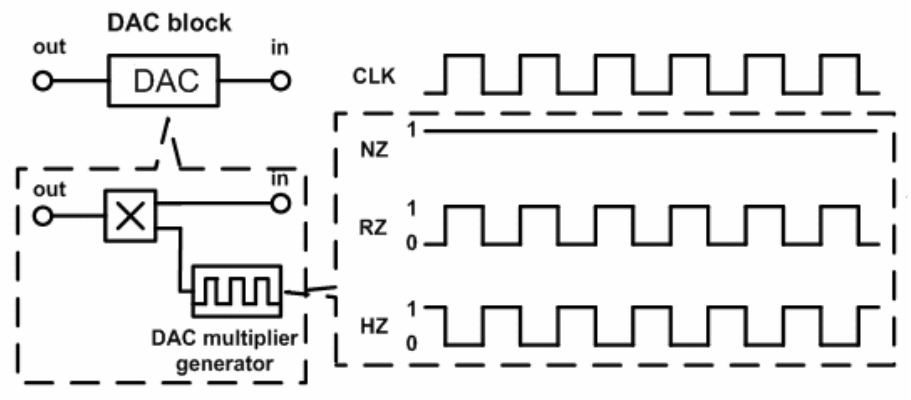


Figure 3.7: Simulink-based continuous-time DAC block.

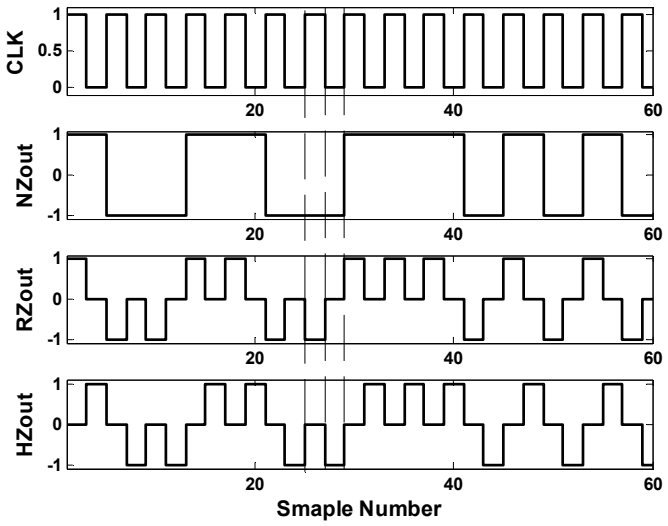


Figure 3.8: Simulated DAC outputs with NRZ, RZ and HRZ pulses.

Base on the proposed CT model, nonidealities in CT Delta-Sigma modulators can be simulated and analyzed.

3.3.2 Signal-Dependent Quantizer Gain

In Chapter 2, the quantization gain is assumed always to be one. However, this case is not true when input signal approaches its full range.

The simulated outputs of the 2nd-order CT Delta-Sigma modulator for the full-range input (the dashed curve), and for the −40-dBFS input (the solid curve) are shown in Fig. 3.9. According to the simulation results, when the input approaches its full range, the noise-shaping effect degrades, the in-band noise increases, and harmonic distortions emerge. As the result, the modulator shows nonlinear SNR/SNDR vs. input curves, which are shown in Fig. 3.10.

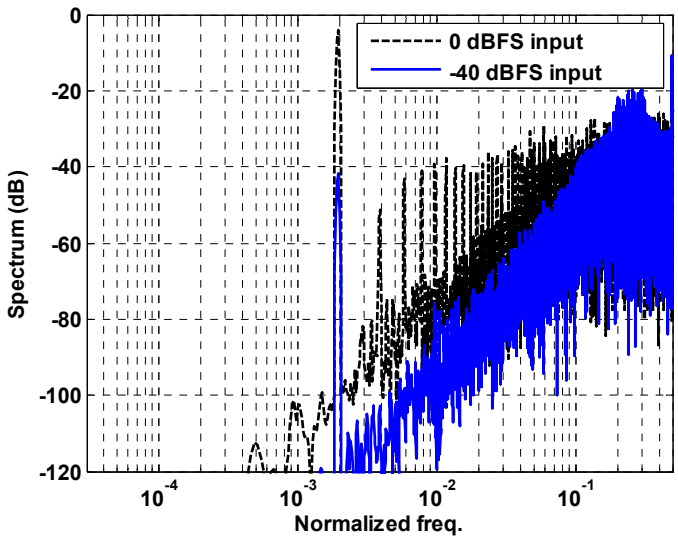


Figure 3.9: Spectrum of the 2nd-order Delta-Sigma modulator for the 0-dBFS input (the top curve), and for the −40-dBFS input (the bottom curve).

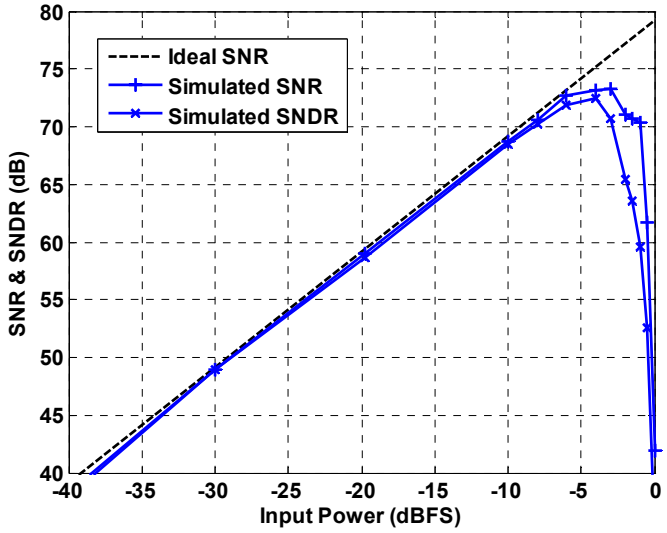


Figure 3.10: SNR/SNDR vs. input plot of the 2nd-order Delta-Sigma modulator.

The nonlinear effect can be analyzed by introducing *effective quantizer gain* k_q in the Delta-Sigma modulator model [Sch05], as shown in Fig. 3.11. The modulator output y could be expressed as:

$$y = k_q \cdot z = k_1 z + k_3 z^{-3}. \tag{3.14}$$

With the effective quantizer gain k_q, the loop filter transfer function and the NTF of the Delta-Sigma modulator can be expressed as:

$$L_{kq} = k_q L_u(s), \tag{3.15}$$

$$NTF_{kq}(s) = \frac{1}{1 - k_q L_1(s)} = \frac{NTF_u(s)}{k_q + (1 - k_q) NTF_u(s)}, \tag{3.16}$$

where L_u and NTF_u represent the transfer functions with the unit quantizer gain.

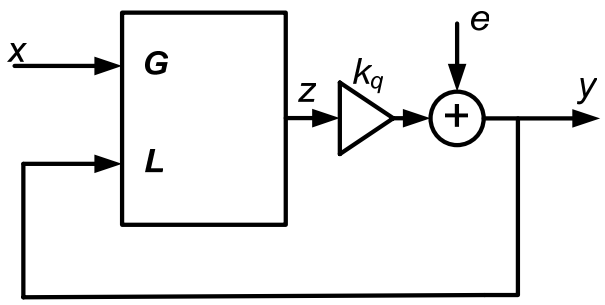


Figure 3.11: Linear model of the Delta-Sigma modulator with effective quantizer gain.

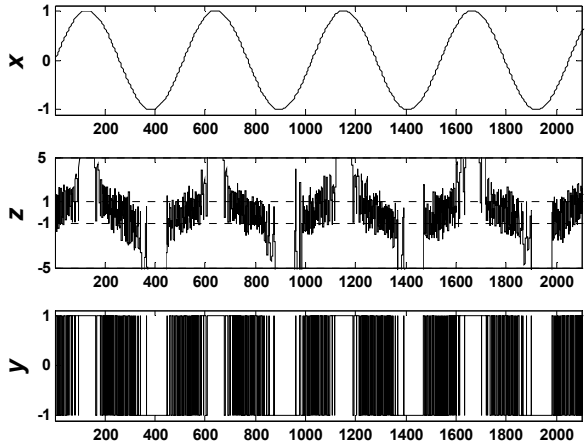


Figure 3.12: Simulated waves of the 0-dBFS input signal (x), the quantizer input (z), and the quantizer output (y) in a 2nd-order Delta-Sigma modulator.

When the input amplitude is small, the quantizer input z is also small, and the output y shows approximately equals $k_1 z$, and the modulator shows good linearity. However, when the input amplitude approaches to its full range, quantizer input z becomes very large, which can be verified by the simulation results, as shown in Fig. 3.12. In this case, the range of z is much larger than the quantization levels, and the quantizer is *overloaded*. At this time, the factor of $k_3 z^{-3}$ (see Eq. 3.14) can not be neglected, which leads to a reduced quantizer gain. According to

Eq. 3.15 and Eq. 3.16, the reduction of k_q degrades the noise-shaping effect, and the in-band noise increases. Furthermore, the nonlinear quantizer gain introduces harmonic distortions. Therefore, the quantizer input should be constrained in a small range.

3.3.3 Stability Issues

Any Delta-Sigma modulator with the 3rd or higher order suffers from stability problem [Cha90] [Sch93] [Hei93] [Bai94] [Dun94]. The simplest way to avoid unstable system is to scale its coefficients to some certain values [Hei93]. Including the effective quantizer gain and the scaling factors, the general model for the *n*-th order input feedforward Delta-Sigma modulator is shown in Fig. 3.13.

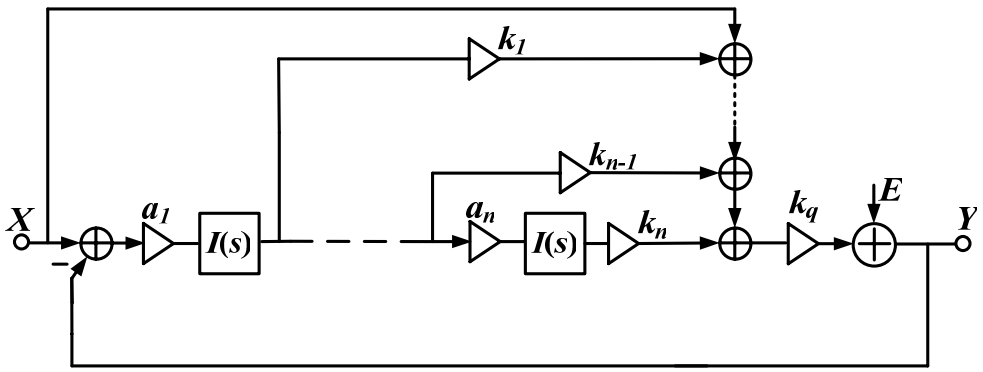


Figure 3.13: Linear model for the *n*th-order input-feedforward Delta-Sigma modulator.

Assuming the transfer function of the integrator is:

$$I(s) = \frac{1}{s}. \tag{3.17}$$

According to Fig. 3.13, the transfer function of its loop filter can be derived as:

$$L(s) = -k_q \sum_{i=1}^{n} k_i s^{-i} \prod_{j=i}^{i} a_j \,. \tag{3.18}$$

And its NTF can be derived as:

$$NTF(z) = \frac{1}{1 + k_q \sum_{i=1}^{n} k_i s^{-i} \prod_{j=i}^{i} a_j}, \tag{3.19}$$

For very-low frequencies, the NTF can be approximately expressed as:

$$NTF(z) \approx \frac{s^n}{k_q k_i \prod_{j=i}^{i} a_j}. \tag{3.20}$$

For the Delta-Sigma modulator with the distributed feedback topology, similar equations can be derived.

Equation 3.20 shows a trade-off between the stability and the SNR of the modulator. The smaller scaling factors provide less aggressive NTF, thus the modulator becomes more stable. However, on the other hand, the less aggressive NTF increases the in-band noise floor, and the SNR is reduced.

For a Delta-Sigma modulator with fixed coefficients, its stability can be analyzed with the variable quantizer gain k_q (see Fig. 3.11) [Bai94]. The procedure is as follows. First, the NTF of the modulator is calculated, and its poles are expressed as a function of the effective quantizer gain k_q. Second, the stability is examined by tracking the roots' loci of the NTF. Fig. 3.14 shows the root locus plot of a 4^{th}-order Delta-Sigma modulator. To keep the modulator stable, their roots should be within the unit circle. The value of k_q, with which the root is located exactly at the unit circle, is named as critical gain. As shown in the Fig. 3.14, the critical gain for this Delta-Sigma modulator is 1.21. In other words, if the effective quantizer gain k_q is less than 1.21, the modulator tends to be unstable. Obviously, less critical gain means better stability performance.

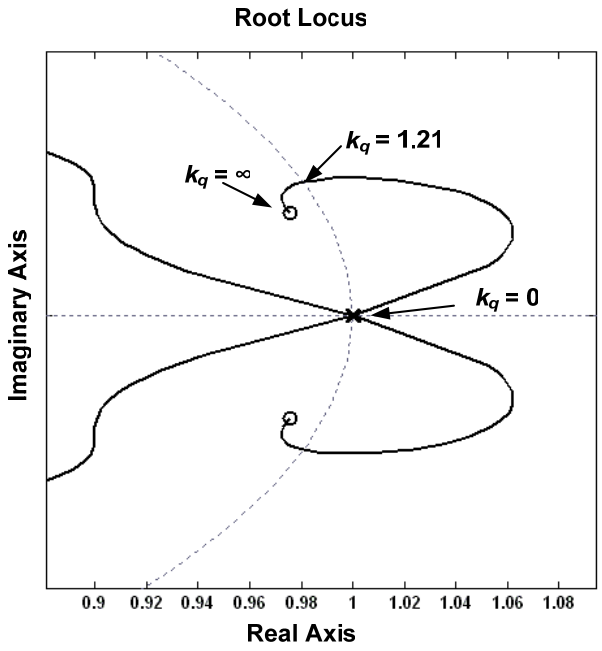


Figure 3.14: Root loci of a 4th-order Delta-Sigma modulator.

Another stability related parameter is *overload level*. Overload level refers to the maximum input amplitude, for which the Delta-Sigma modulator is still stable. For most publications, this level is defined as the highest amplitude, for which the modulator's SNR is 6 dB lower than its peak value. The overload level can be found by plotting SNR vs. input curve. For example, for the 2nd-orderDelta-Sigma modulator without scaling, its overload level is about −1.4 dBFS, as shown in Fig. 3.10. Obviously, higher overload level means better stability performance.

3.3.4 Excess Loop Delay Effect

The excess loop delay refers to the delay between the edge of the quantizer clock and the feedback pulse [Che99-b]. This delay is unavoidable, since it is caused by the nonzero switching time of the transistors and the speed of the quantizer. Fig. 3.15 shows the ideal and the delayed NRZ pulses, where the excess loop delay is represented as τ_d. According to Eq. 3.1, for the ideal NRZ, $\alpha = 0$, and $\beta = 1$. However, for the delayed NRZ, $\alpha = \tau_d$, and $\beta = 1+\tau_d$, as shown in Fig. 3.15.

To analyze the effect of the excess loop delay, the delayed NRZ pulse is modeled as the sum of two pulses. One is a pulse in the current clock period, the other is a pulse extending to the next period (see Fig. 3.16) [Che99-b]. Thus the delayed NRZ pulse can be expressed as [Che99-b]:

$$r_{(\tau_d, 1+\tau_d)}(t) = r_{(\tau_d, 1)}(t) + r_{(0,\tau_d)}(t-1). \tag{3.21}$$

It has been proven that, the delayed NRZ portion, which extends to the next period, introduces one more order to the loop-filter transfer function, and may degrade the stability performance of the modulator [Che99-b]. The HRZ DAC pulse suffers the similar problem. The situation for RZ is better, since there is no pulse extending to the next period if the excess loop delay is less than half clock period.

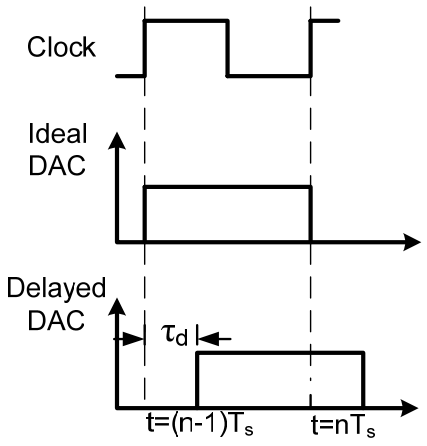


Figure 3.15: Ideal NRZ pulse and the delayed NRZ pulse.

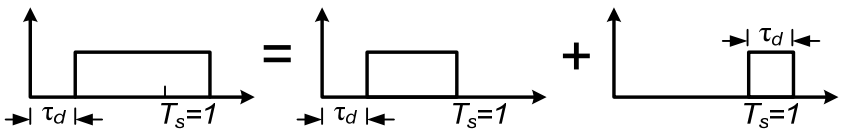


Figure 3.16: Linear combination of the delayed NRZ pulse.

For NRZ, RZ and HRZ pulses, the excess loop delay effect can be simply simulated by adding a delay block in the feed back loop, which is shown in Fig. 3.17. Fig. 3.18 shows the simulated spectrum of the CT Delta-Sigma modulators with the non-delayed NRZ DAC pulse and the delayed NRZ DAC pulse. A 4th-order Delta-Sigma modulator with coefficients a_i = [0.2, 0.4, 0.1, 0.1] k_i = [0.81, 0.92, 0.7, 2] is used for the simulation. As shown in Fig. 3.18, the delayed DAC pulse increases the noise floor. The impacts of the excess loop delay on the SNRs of the Delta-Sigma modulators with the NRZ and the RZ DAC pulses are shown in Fig. 3.19. The inputs for the modulators are both a sinusoid wave with −3-dBFS amplitude. As the figure indicates, the modulator with the NRZ DAC pulse becomes unstable when excess loop delay exceeds 17% of the clock period, and the modulator with RZ DAC pulse can tolerate a delay up to 58% of the clock period. The simulation results verify that the RZ DAC pulse shows much higher tolerance to the excess loop delay.

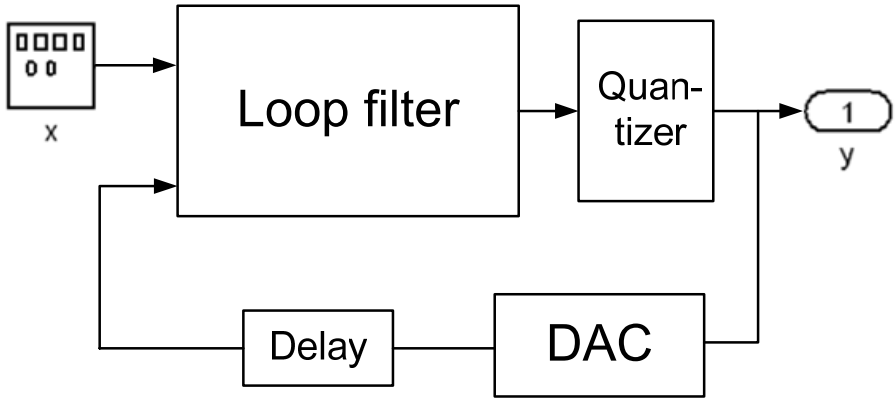


Figure 3.17: Simplified Simulink-based model for the excess loop delay simulation.

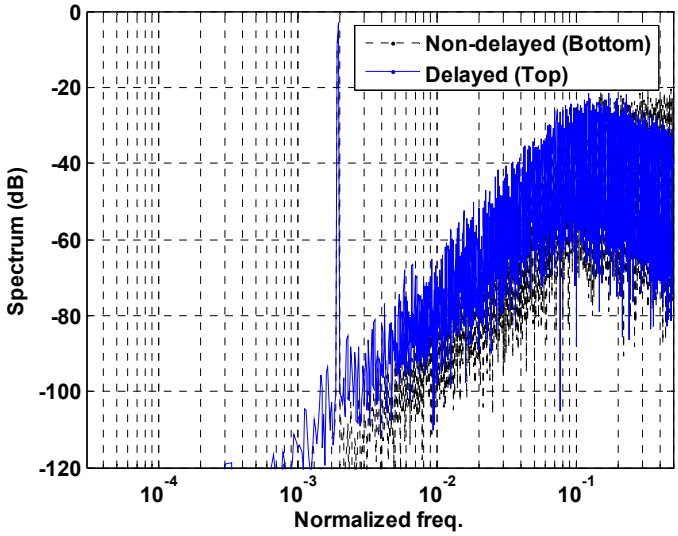


Figure 3.18: Output spectrum of a 4th-order CT Delta-Sigma modulators with the ideal NRZ DAC pulse (bottom), and with the delayed DAC pulse (top).

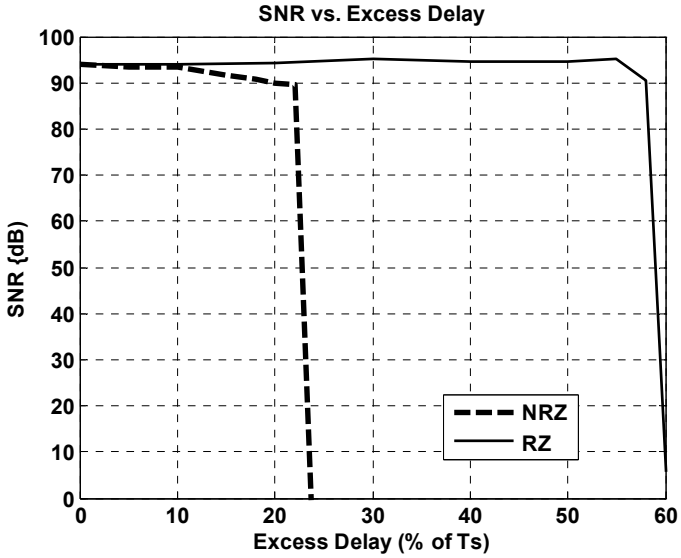


Figure 3.19: Impacts of the excess delay on the SNRs of a 4th-order CT input-feedforward Delta-Sigma modulators, with NRZ DAC pulse (dashed line), and with RZ DAC pulse (solid line), for the −3-dBFS input.

A simple way to limit the practical delay within the tolerance is to use single-bit quantizer. Because the single-bit quantizer does not need dynamic element matching circuits, its delay is much less than the multi-bit counterpart. If the practical excess loop delay is higher than its tolerance, additional compensation techniques are necessary. A remedy to relieve the influence of the excess loop delay is to use an additional digital latch in the DAC [Che00] [Yan04].

For example, for a 4th-order DT input-feedforward Delta-Sigma modulator, whose coefficients are a_i = [0.2, 0.4, 0.1, 0.1], k_i = [1, 1, 1, 2] [Yao05], its loop filter transfer function can be derived as:

$$L(z) = \frac{-0.2z^3 + 0.52z^2 - 0.448z + 0.1264}{(z-1)^4}. \tag{3.22}$$

If one delay is extracted from the loop filter, its transfer function can be translated into:

$$L(z) = z^{-1}[-0.2 + \frac{-0.28z^3 + 0.752z^2 - 0.6736z + 0.2}{(z-1)^4}]. \tag{3.23}$$

After mapping this DT transfer functoin to the CT couterpart, an optimized structure is obtained, which is shown in Fig. 3.20, the coefficients become a_i = [0.2, 0.4, 0.1, 0.1], k_i = [1.4, 1.1, 1.2, 2], b_2 = 0.2. Since one clock delay is introduced in the DAC, this modulator can tolerate an excess loop delay more than one clock period. The trade-off for the improved performance is the increasd circuit complexity. As shown in Fig. 3.20, an additional DAC path (DAC2 in Fig. 3.20) is needed, which is fed back to the input of the quantizer.

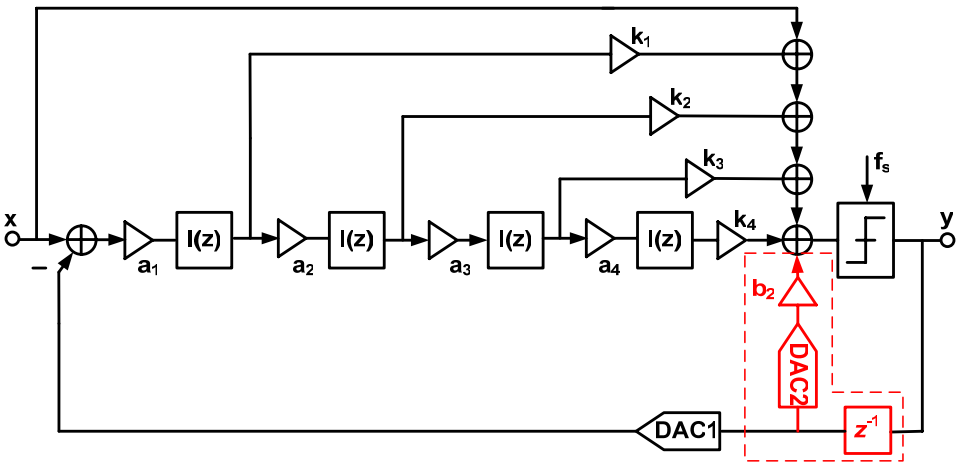


Figure 3.20: Delay-immune structure for a 4th-order CT input-feedforward Delta-Sigma modulator, the additional feedback loop (DAC2) is shown in the dashed box.

3.3.5 Clock Jitter Effect

Clock jitter refers to the timing uncertainty of the clock. Such a jitter is Gaussian distributed, and is specified by its rms value or standard deviation value. Fig. 3.21 shows the ideal clock (on the top), and the jittered clock (on the bottom), where shadows represent the uncertain regions. Clock jitter results in an error sequence in the DAC signal. In Fig. 3.22, a jittered NRZ DAC pulse is given, which can be modeled as the sum of an ideal pulse and an error sequence caused by clock jitter. The error sequence can be expressed as [Ris94]:

$$e_{NRZ}(n) = [y(n) - y(n-1)]\frac{\beta_n}{T_s}, \tag{3.24}$$

where $y(n)$ is the n-th DAC output, and β_n is the time error at the n-th sampling point. This error sequence of the DAC introduces additional noise. The jitter noise is not shaped by the loop filter, since it is directly fed back to the input, and hence it may seriously degrade the CT Delta-Sigma modulator's resolution.

In [Ris94], the signal-to-jitter noise ratio is estimated by the following equation:

$$SNR_{NRZ} = 10\log\frac{OSR \cdot A^2/2}{\sigma_y^2(\sigma_\beta/T_s)^2}, \tag{3.25}$$

where σ_y is the variation of the modulator output y, σ_β is the rms of the clock jitter, and A is the input amplitude. For the single-bit Delta-Sigma modulator σ_y is around 2.7 and 2.8 [Che00].

CT Delta-Sigma modulators with the RZ and the HRZ DAC pulses are more sensitive to the clock jitter effect [Che99-a]. As shown in Fig. 3.23, for the NRZ DAC pulse, the clock jitter only affects when the output signal switches. However, for the RZ DAC pulse, the clock jitter effects in every clock period. The case in the HRZ pulse is the same as that in the RZ pulse. Thus one can expect more jitter noise in the RZ/HRZ pulse than that in the NRZ pulse.

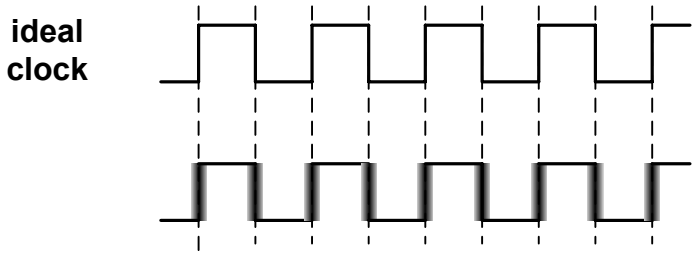


Figure 3.21: Ideal clock and the jittered clock.

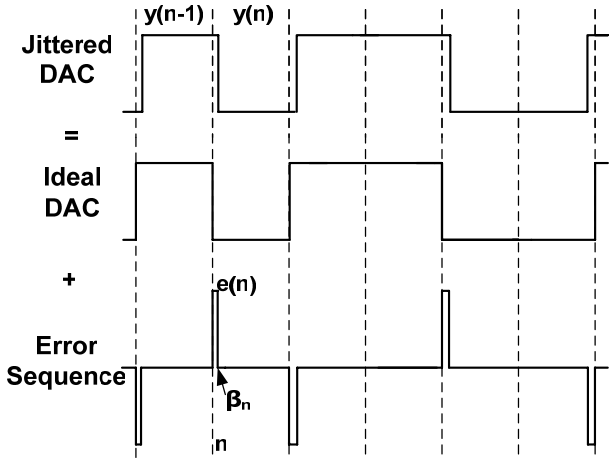


Figure 3.22: Linear combination of the jittered NRZ pulse.

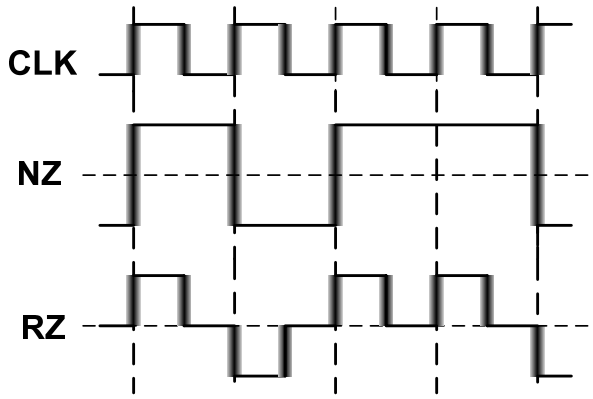


Figure 3.23: Jittered NRZ and RZ pulses.

The Simulink-based models for the clock jitter simulations are shown in Fig. 3.24. The clock jitter is modeled as a random noise. One trick for the models is that, the random noise is added to the DAC output, not the clock. That is, the timing error β_n (see Eq. 3.24) is translated into the output error. Since the DAC error is the product of the output and the jitter, this translation is reasonable.

The spectrum of the CT Delta-Sigma modulators with and without the clock jitter is shown in Fig. 3.25. Obviously, the jitter noise whitens the band of interest. Fig 3.26 shows the impacts of the clock jitter on the SNRs of the 4^{th}-order CT input-feedforward Delta-Sigma modulators, with the NRZ DAC pulse and the RZ DAC pulse, respectively. The simulation results verify that the NRZ DAC pulse is less sensitive to the clock jitter. Compare to the RZ DAC pulse, the NRZ pulse provides about 3-dB improvement in the SNR, if the noise is dominated by the clock jitter noise.

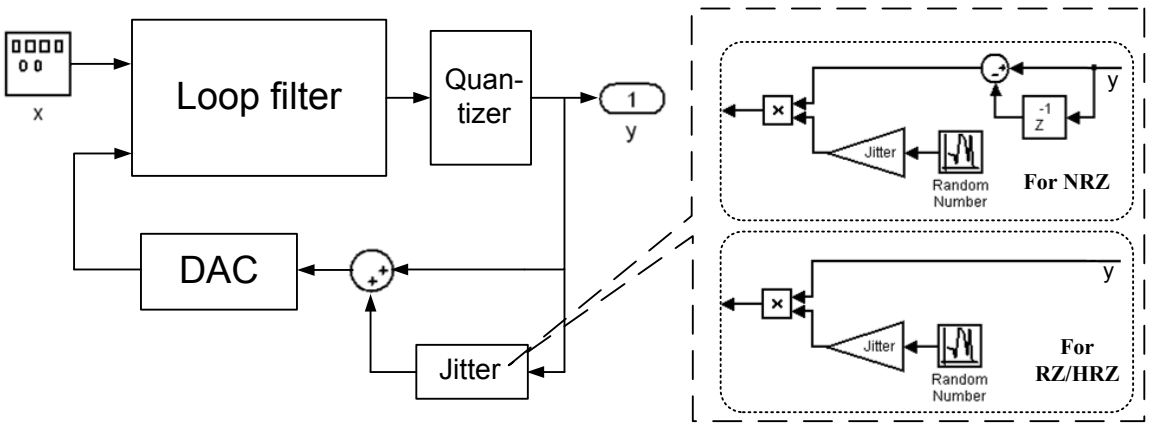


Figure 3.24: Simplified Simulink-based model for the clock jitter simulation.

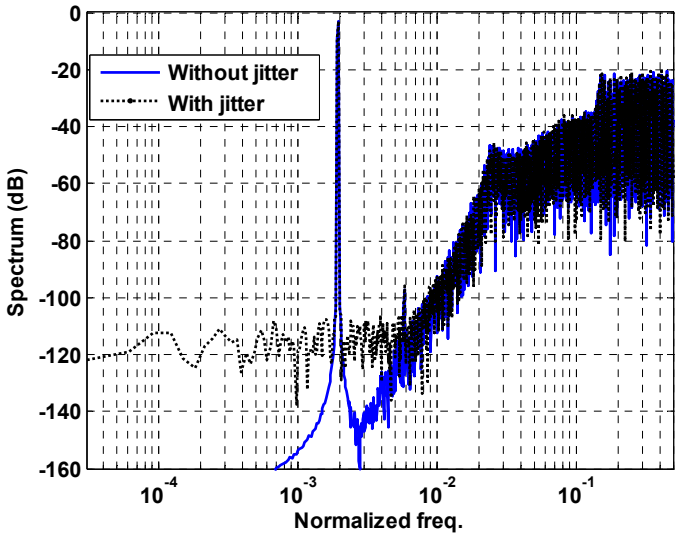


Figure 3.25: Output spectrum of the ideal (bottom) and the jittered (top) 4th-order CT Delta-Sigma modulators with NRZ DAC pulses.

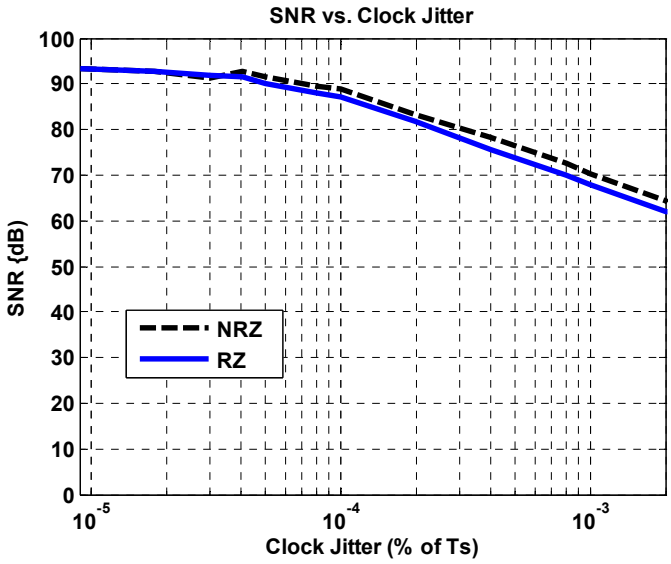


Figure 3.26: Impacts of the clock jitter on the SNRs of 4th-order CT input-feedforward Delta-Sigma modulators, with NRZ pulse (dashed line), and with RZ pulse (solid line), for the −3-dBFS input.

Like the excess loop delay, the clock jitter is unavoidable. There are few methods to reduce the influence of the clock jitter. The most direct solution is to use accurate clock source, which has small enough jitter. In addition, as what has been discussed, the NRZ DAC pulse can be used. The multi-bit quantizer is another solution, since it shows less sensitive to the clock jitter than the single-bit [Gee02]. When applying the multi-bit DAC pulse, the difference of two adjacent pulses will be less than that in the single-bit DAC pulse, and hence the impact of clock jitter is suppressed. In some papers, clock jitter effect is relieved by using other jitter-insensitive DAC waves, like the sinusoid DAC wave [Lus02], the triangular and the quadratic-characteristic DAC waves [Ger06], or the switched-capacitor DAC wave [Ort05]. With the fixed clock jitter, these DAC waves provide less charge errors than the zero-order hold DAC waves. However, they increase the difficulties in synthesizing systems and implementing circuits.

3.3.6 Unequal DAC Rise/Fall Time Effect

The asymmetric DAC rise/fall time also causes problems like the additional noise and the harmonic distortions.

For example, assuming the fall time of the DAC signal is zero and the rise time is t_r, two NRZ sequences are shown in Fig, 3.27. One NRZ wave represents the signal sequence of "1, 1, −1, −1", and the other represents "−1, 1, −1, 1". The dark region refers to signal "1", and the light region refers to signal "-1". Ideally, the total energies (or the area) of the two DAC feedbacks should be zero for the 4 clock periods, since both of them have two 1s and two −1s. However, due to the unequal rise/fall time, the total energies of the two DAC feedbacks are different. As shown in Fig. 3.27, for the signal "1, 1, −1, −1", the positive energy is $2T_s - t_r + t_r / 4 = 2T_s - 3t_r/4$, and the negative energy is $2T_s + t_r/4$, thus the total energy is $-t_r$. However, for the signal "−1, 1, −1, 1", the total energy is $2t_r$. Due to the unequal rise/fall times, the NRZ feedback energy deviates the ideal case, and becomes signal-dependent. In other words, the NRZ feedback energy not only depends on the numbers of 1s and −1s, but also depends on how those 1s and −1s switch. As a result, the noise floor increases and harmonic distortions emerge [Che00].

The situation for the RZ/HRZ response is much better. Fig. 3.28 shows the RZ responses with the same signals. The RZ pulses always return to zero in every clock period, which is like a kind of reset to make the pulse have the same start point at every clock period. Therefore, every signal 1 has the identical energy, so does signal −1. As the result, the unequal rise/fall time effect in the RZ DAC feedback only introduces a gain error to the Delta-Sigma modulator.

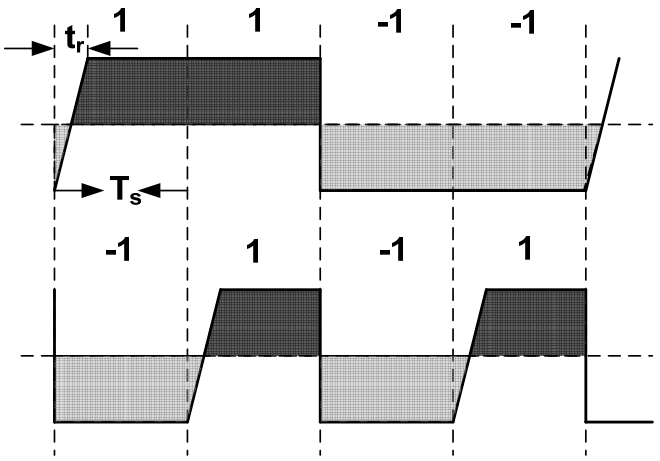


Figure 3.27: NRZ pulses with the unequal rise/fall time.

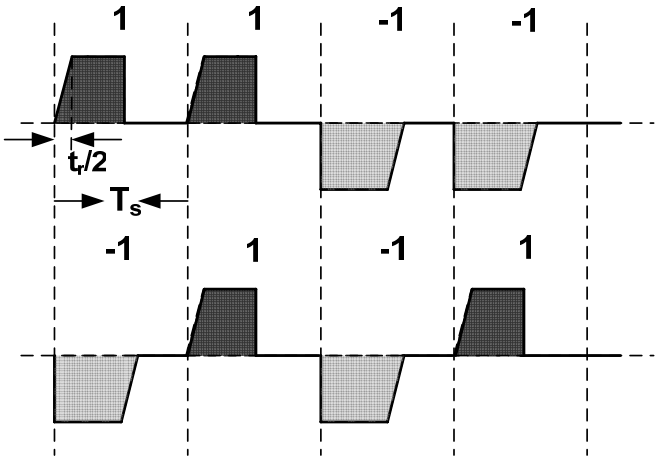


Figure 3.28: RZ pulses with the unequal rise/fall time.

Similar to the clock jitter effect, the effect of the unequal rise/fall time can be modeled by changing the feedback pulse area. The Simulink-based models for the unequal rise/fall time simulations are shown in Fig. 3.29. As an example, the fall time is set to be zero, and the rise time value is set by the user. Fig. 3.30 shows the output spectrum of the CT Delta-Sigma modulators with the equal and with the unequal rise/fall DAC time. The DAC shape is NRZ. The simulation

results verify that the unequal DAC rise/fall time increases the noise floor and causes harmonic distortions. Fig 3.31 shows the impacts of the unequal DAC rise/fall time on the SNRs of the 4th-order CT input-feedforward Delta-Sigma modulators, with the NRZ DAC pulse and with the RZ DAC pulse. The simulation results verify that the RZ DAC shape is much less affected by this effect.

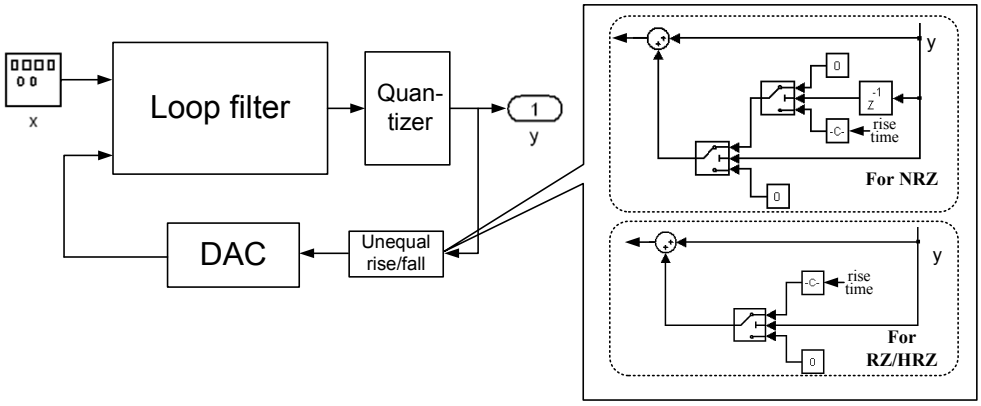


Figure 3.29: Simplified Simulink-based model for the unequal DAC rise/fall time simulation.

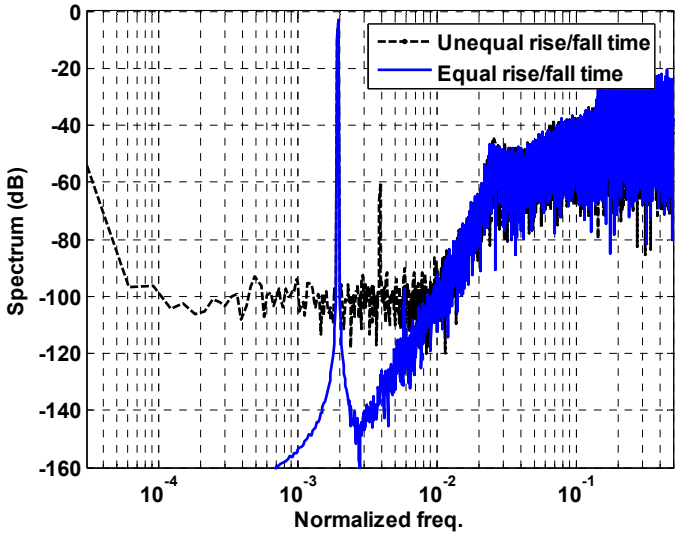


Figure 3.30: Output spectrum of the CT Delta-Sigma modulators with the equal (bottom) and the unequal (top) rise/fall time, the DAC shape is NRZ.

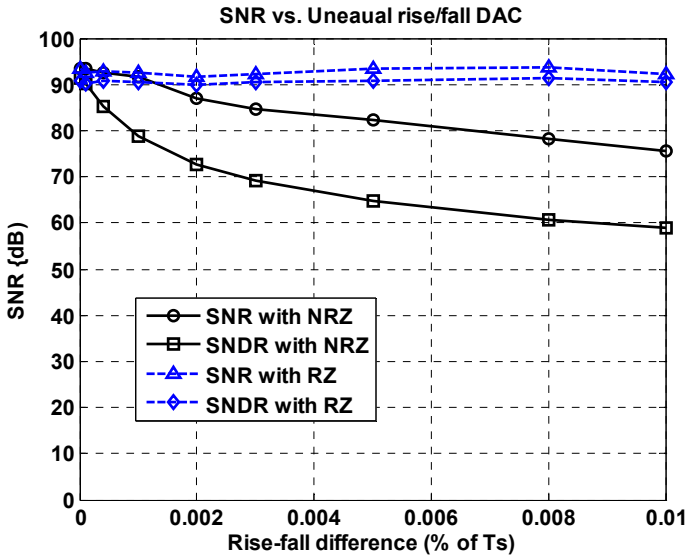


Figure 3.31: Impacts of the unequal DAC rise/fall time on the SNRs/SNDRs of the 4th-order CT input-feedforward Delta-Sigma modulators, with the NRZ pulse, and with the RZ pulse, for the −3-dBFS input.

There are some solutions for the problem caused by the unequal DAC rise/fall time. One solution is to use the RZ/HRZ DAC shape. Another solution is to use the differential circuitry. Despite the unequal DAC rise/fall time, the differential circuit can produce symmetrical DAC pulses [Jen95].

3.3.7 Finite Amplifier Gain and Gain-Bandwidth Effect

Usually the CT integrator can be implemented in the form of Gm-C filter or active-RC, which is shown in Fig. 3.32. Ideally, transfer functions of the Gm-C and the active-RC integrator can be derived as:

$$I_{Gm-C}(s) = \frac{g_m}{sC} = a\frac{f_s}{s}, \tag{3.26}$$

$$I_{RC}(s) = \frac{1}{sRC} = a\frac{f_s}{s}, \tag{3.27}$$

where *a* represents the integrator gain, or the time-constant. According to Eq. 3.26 and Eq. 3.27, there is only one pole, which is located at dc, as shown in Fig. 3.33.

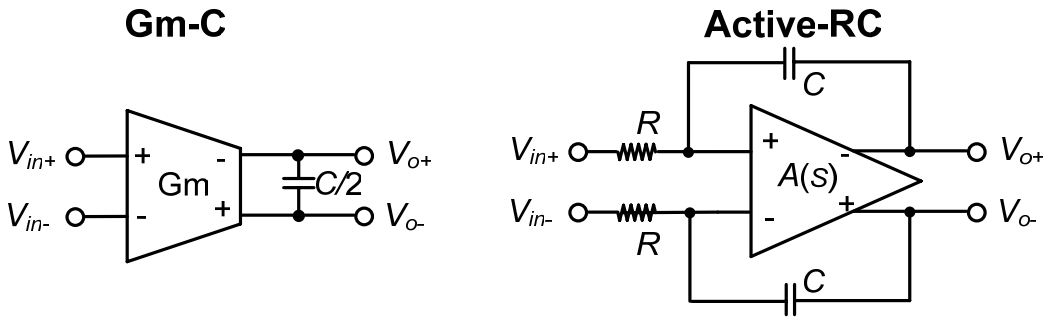


Figure 3.32: Circuit diagrams of Gm-C filter (left) and active-RC filter (right).

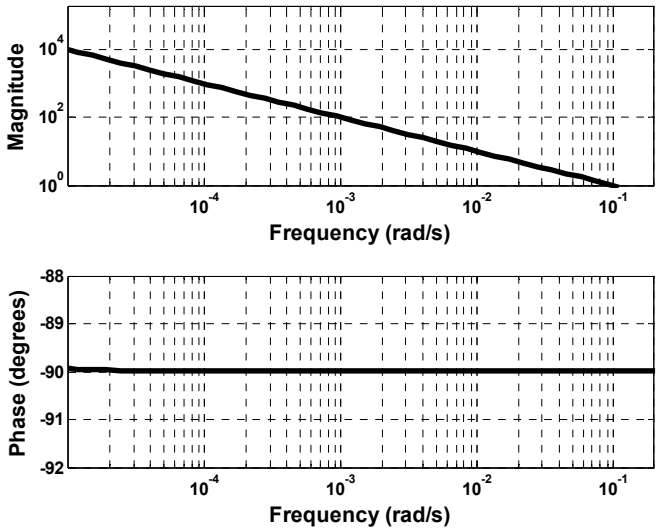


Figure 3.33: Bode plot of the ideal integrator.

In practical, the amplifier suffers from nonidealities, such as the finite gain and the finite gain-bandwidth. Due to these two nonidealities from the amplifier, the transfer function of the

integrator deviates from its ideal case. For example, with the finite amplifier gain, the transfer function of the active-RC integrator is derived as:

$$I_{RC}(s) = \frac{1}{sRC} \cdot \frac{1}{1 + (1 + \frac{1}{sRC})\frac{1}{A_0}} = a \cdot \frac{1}{s(1 + \frac{1}{A_0}) + \frac{a}{A_0}}, \tag{3.28}$$

where A_0 represents the dc gain of the amplifier. According to Eq. 3.28, due to the finite amplifier gain, the pole of the integrator is pushed away from dc to $a/(A_0+1)$, as shown in Fig.3.34. Usually, this effect is known as *leaky integration* [Nor97].

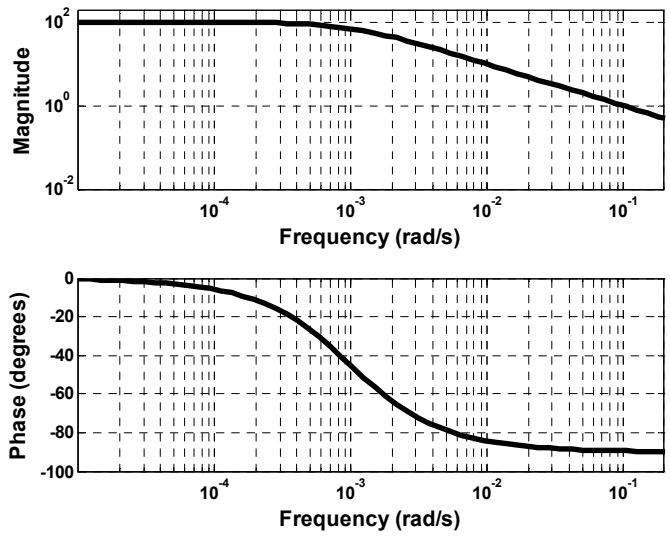


Figure 3.34: Bode plot of the integrator with the finite amplifier gain.

The impact of the amplifier's finite gain-bandwidth is also needed to be considered. For a single-pole amplifier with finite gain, its transfer function can be expressed as:

$$A(s) = \frac{GB}{s + GB / A_0}. \tag{3.29}$$

where GB represents the gain-bandwidth, and $\omega_{p\text{-}amp}$ represents the pole of the amplifier. The transfer function of the active-RC integrator can be derived as:

$$I_{RC}(s) = \frac{a \cdot GB}{s^2 + s(GB + a + GB/A_0) + a \cdot GB/A_0}, \tag{3.30}$$

which indicates that one non-dominant pole is introduced into the integrator, as shown in Fig. 3.35.

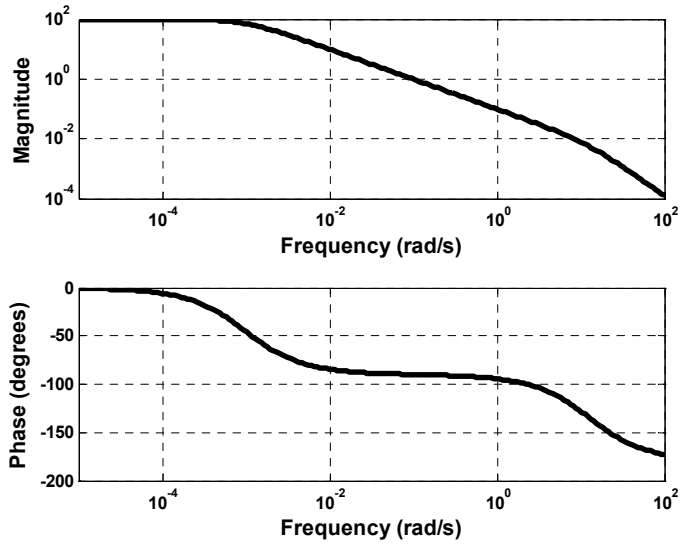


Figure 3.35: Bode plot of the integrator with the finite amplifier gain and finite gain-bandwidth.

By affecting the transfer function of the integrator, the finite gain and gain-bandwidth of the amplifier affects the NTF, as well as the SNR of the modulator. To simulate the effect of the finite amplifier gain and gain-bandwidth, the transfer function of the integrator is replaced by Eq. 3.30 in the Simulink model. Fig. 3.36 shows the spectrum of the CT modulators with different amplifier gains and gain-bandwidths. As shown in Fig. 3.36, low gain and low gain-bandwidth will degrade the noise-shaping effect of the modulator. Fig. 3.37 shows the SNR degradation of

the 4th-order input-feedforward CT Delta-Sigma moudlator due to the amplifier gain and bandwidth. The figure shows that the input-feedforward CT modulator is not sensitive to the amplifier gain and gain-bandwidth variatoins, and the SNR does not obviously degrade even with very low gain (40 dB) and very low gain-bandwith (f_s) are allowed. Such results are not surprising, since the low dc gain requirement has been proven by other publications [Yao04] [Roh08] , and the low gain-bandwidth requirement is also in accordance to the other publication [Cha92].

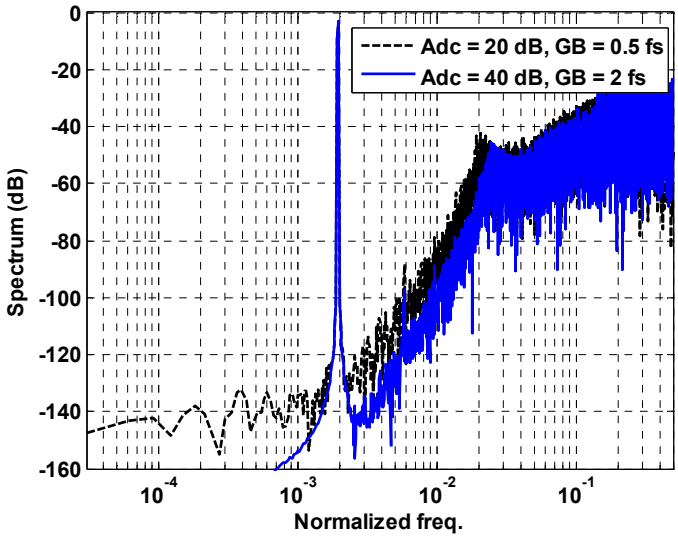


Figure 3.36: Output spectrum of the 4th-order CT input-feedforward Delta-Sigma modulators with different amplifier gains and gain-bandwidths.

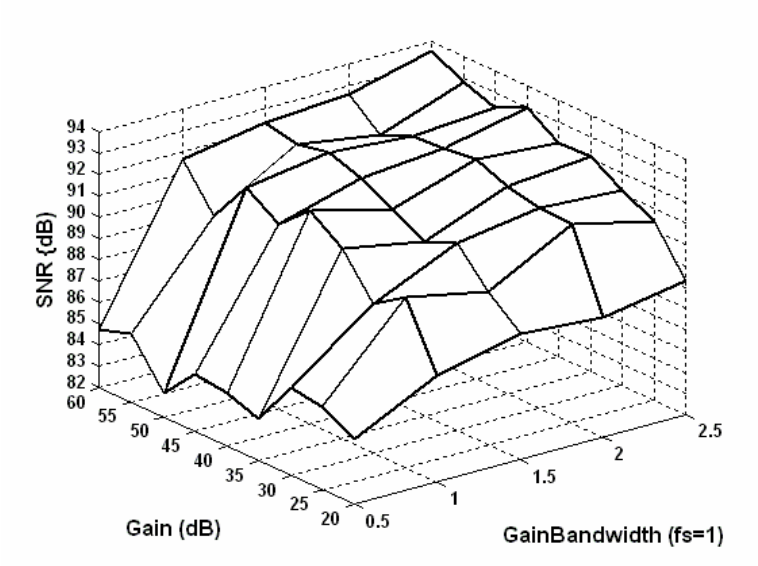


Figure 3.37: Impacts of finite amplifier gain and gain-bandwidth on the SNR of the 4th-order CT input-feedforward Delta-Sigma modulator, for the −3-dBFS input.

3.3.8 Finite Amplifier Slew Rate Effect

Although the CT Delta-Sigma modulator relaxes the amplifier's settling requirement, slew rate may become a limiting factor of amplifier's current, especially in the low-power design.

The Simulink-based integrator model for the slew rate simulation is shown in Fig. 3.38, where a subsystem is created after the ideal integrator. The slew rate is set by a constant number *SR*. For every output of the ideal integrator, which is represented by z in the figure, its slew rate is calculated, which equals $[z(n)-z(n-1)]/T_{s\_SR}$. The clock period T_{s_SR} for calculating the slew rate can be made much smaller than the clock period of the Delta-Sigma modulator to ensure an accurate result. The calculated slew rate is then compared with the number *SR*. If the real slew rate is smaller than *SR*, the integrator output $y(n) = z(n)$. If the real slew rate is larger than *SR*, the integraor output $y(n) = z(n-1)\pm SR$.

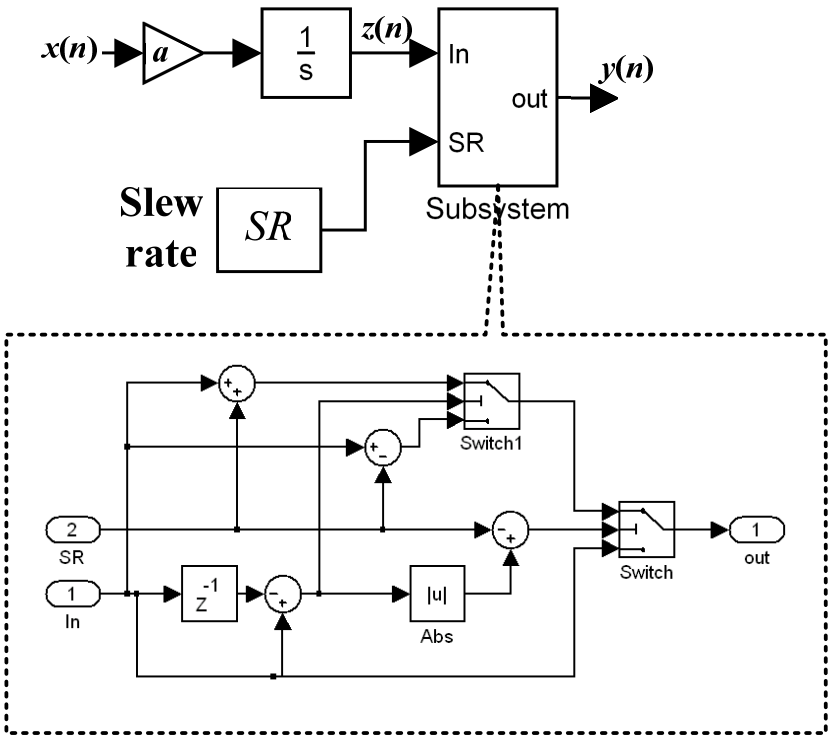


Figure 3.38: Simulink-based integrator model for the slew rate simulation.

The slew rate effect of the 1st integrator is simulated, since the 1st integrator has the dominant impact on the modulator's performance. The spectrum of the CT Delta-Sigma modulators with different slew rates in the 1st amplifiers are shown in Fig. 3.39, which indicates that insufficient slew rate increases the noise floor and causes hamonic distortions. Fig 3.40 shows the plot of the SNR versus the 1st amplifier's slew rate. The figure shows that a slew rate about 0.3*Vref/fs is needed for this modulator to achieve a good SNR. Of course, the slew rate requirements for different Delta-Sigma modulators are different.

Obviously, the slew rate depends on the output swing of the integrator, if the sampling clock period is fixed. To lower down the slew rate requirement, one can scale the integrator gain to a small value. Another solution to lower down the slew rate requirement is to use proper DAC shapes. For example, with the same integrator time constant, the NRZ DAC shape shows less slew rate requirement than the RZ/HRZ or switched-capacitor DAC shapes [Ort06].

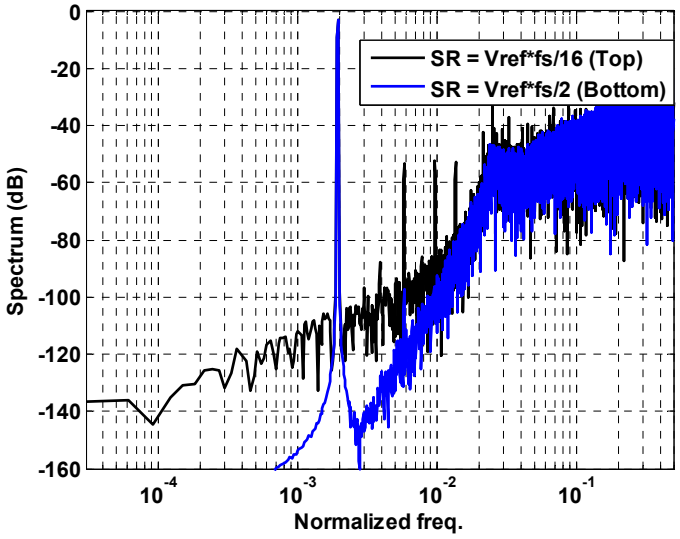


Figure 3.39: Output spectrum of the 4th-order CT Delta-Sigma modulators with different slew rates in the 1st amplifiers.

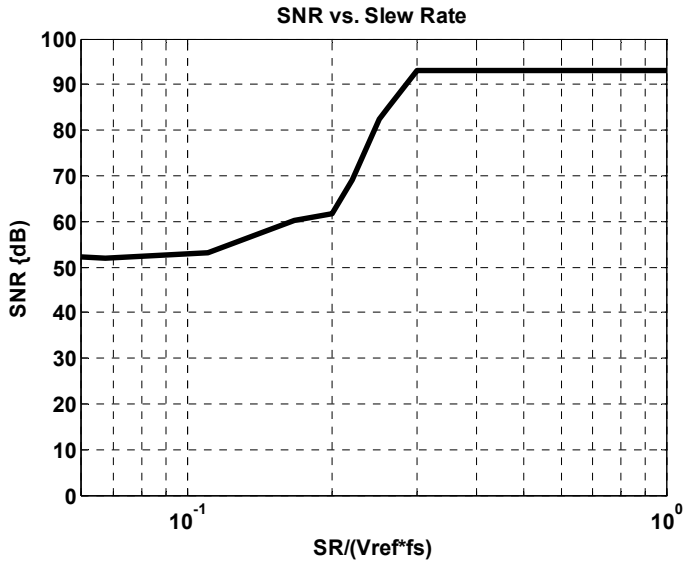


Figure 3.40: Impacts of the 1st amplifier's slew rate on the SNR of the 4th-order CT input-feedforward Delta-Sigma modulator, for the −3-dBFS input.

3.3.9 Time-Constant Variation Effect

Due to the unavoidable process variations to resistors and capacitors, time-constants of the integrators deviate from the expected values. Since time constants determine the NTF of the modulator (see Eq. 3.19), large shifts of the time constants may degrade the performance of the CT Delta-Sigma modulator greatly.

The simulated SNR versus time-constant variation plot is shown in Fig. 3.41. In the simulations, the four time-constants are assumed to be varied at the same rate. According to Fig. 3.41, a variation within ±10% is required to limit the SNR degradation within 3 dB.

Trimming can be one solution to the problem of time-constant variations. However this method is at the expense of high chip cost. A widely used solution is to design tunable integration resistances and/or capacitances, which will be further discussed with the design examples in the following chapters.

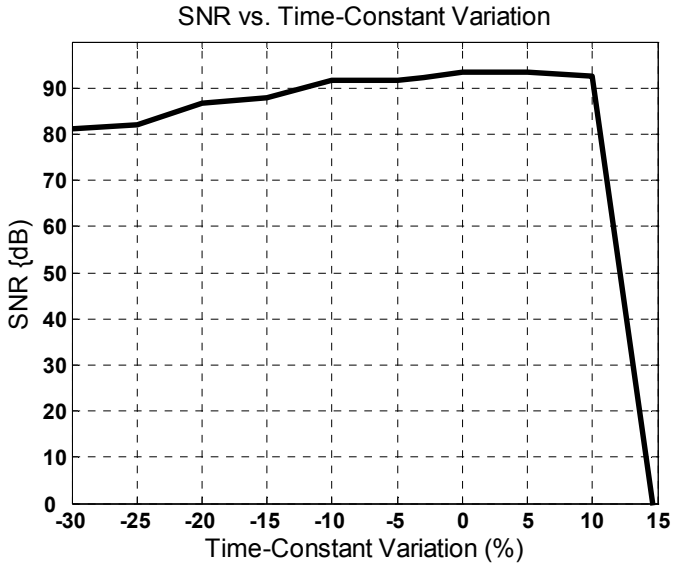


Figure 3.41: Impacts of the time-constant variation on the SNR of the 4th-order CT input-feedforward Delta-Sigma modulator, for the −3-dBFS input.

3.3.10 Quantizer Hysteresis Effect

In practical, the quantizer suffers from hysteresis effect.

The effect of hysteresis is shown in Fig. 3.42. Just like a Schmitt trigger, the comparator does not switch exactly at the reference voltage (which is 0 for a 1-bit quantizer). The hysteresis effect causes more noise, but such noise can be shaped by NTF in the same way as the quantization noise, and hence usually its influence can be neglected.

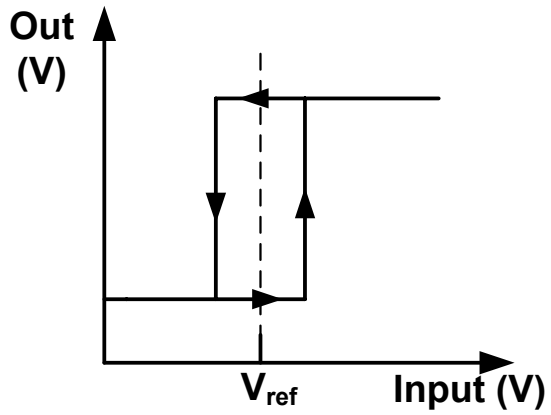


Figure 3.42: Hysteresis effect in the quantizer.

3.4 Conclusion

This chapter discusses the system-level issues in CT Delta-Sigma modulators. The method for exploiting a CT Delta-Sigma modulator from a DT Delta-Sigma modulator is introduced. Then Simulink-based models for CT Delta-Sigma modulators are proposed. With the models, nonidealities in CT Delta-Sigma modulators are analyzed and simulated Unlike DT Delta-Sigma modulators, CT Delta-Sigma modulators suffer from many nonidealities. Since those nonidealities may greatly degrade the performance of the modulator, and hence necessary

considerations must be paid to them in practical designs. In Table 3.2, the main nonidealities together with their solutions are summarized, which can be taken as a reference for practical designs.

The circuit-level designs will be presented with the design examples in the following chapters.

Table 3.2 Main nonidealities in CT Delta-Sigma modulators.

Nonidealities	Impacts	Solutions
Overload	- More noise - Distortions - Unstable system	- Limited input range - Time constant scaling - Multi-bit quantizer
Excess loop Delay	- More noise - Unstable system	- Use simple circuit (1-bit quantizer) - Use RZ DAC shape - Additional latch in DAC
Clock jitter	- More noise	- Accurate clock source - Multi-bit - Jitter-insensitive DAC shapes
Unequal DAC rise/fall time	- More noise - Distortions	- Use RZ/HRZ pulses, - Differential circuitry
Amplifier finite gain/gain-bandwidth	- More noise - Distortion	- Design amplifier with enough gain and gain-bandwidth
Amplifier finite slew rate	- More noise - Distortions	- Design amplifier with enough slew rate
Time constant variation	- Unstable system	- Trimming - Resistance/Capacitance tuning
Quantizer hysteresis	- More noise	- Reset circuitry

CHAPTER 4

A 1.2-V 2.7-mW 160-MHz CONTINUOUS-TIME DELTA-SIGMA MODULATOR WITH INPUT-FEEDFORWARD STRUCTURE

4.1 Introduction

The wide-bandwidth, high-resolution, and high-linearity analog-to-digital converter is an essential building block in communication systems. By utilizing the oversampling and noise shaping techniques, the Delta-Sigma modulator shows its superiority in the resolution and linearity, and has obtained many attentions from both institutes and companies. Traditionally, Delta-Sigma modulators are applied in the narrow-band applications, such as audio applications, due to their oversampling principles [Nor97]. With the advancement of the CMOS technology, it is possible to design Delta-Sigma modulators with bandwidths more than 1 MHz and resolutions of 10-14 bits [Gia03] [Pat04] [Yan04] [Li07]. Power consumption is another key performance for communication devices, especially for portable devices, because it directly determines the battery lifetime and the battery size (the product weight).

Our work targets the low-power solutions for low-voltage wideband Delta-Sigma modulators. A 1.2-V fourth-order single-bit continuous-time Delta-Sigma modulator with 1.25-MHz signal bandwidth is presented, which can be applied for many communication applications like Bluetooth, Asymmetrical Digital Subscriber line (ADSL), CDMA, and so on.

The continuous-time loop input-feedforward topology is employed, since it provides attractive potential for higher-speed and/or lower-power operations by relaxing the settling time requirement on amplifiers, when compared to its discrete-time counterpart. The input-feedforward topology is chosen, because it provides smaller internal swings, which is more suitable for low-voltage operations than the distribute feedback topology [Sil01]. However, the advantages of the CT input-feedforward topology are at the expense of some design challenges. The CT Delta-Sigma modulator is sensitive to nonidealities, such as the clock jitter, the excess loop delay, and the time-constant variation. These nonidealities possibly degrade the modulator's performance greatly, and hence considerations to them are needed during the design. The implementation of the forward and summation part is another issue to be addressed. In the reported designs, CT feedforward paths are implemented with transconductors [Gia03] [Pat04] [Yan04] [Li07] or feedforward capacitances [Sch04]. However, the additional transconductors, which introduce lots of additional transistors, increase the power consumption, the area, and the circuit complexity, and the large feedforward capacitances increase the loads of the integrators, as well as the power and the area. To solve these problems, a simple power and area efficient structure for the CT feedforward and summing part is proposed in this design [Zha09], in which only one pair of transistors with small parasitic capacitances involve in each feedforward path.

The organization of this chapter is as follows. Section 4.2 discusses architecture-level issues, including the topology selection and optimization, and the considerations to the impacts of nonidealities on this CT Delta-Sigma modulator. Section 4.3 presents the circuit implementation of the building blocks. The test setup issues and measurement results are presented in Section 4.4. Section 4.5 concludes the chapter.

4.2 Architecture-Level Design

4.2.1 Loop Topology

A. *Single-Bit Input-Feedforward Topology*

As discussed in Chapter 2, Delta-Sigma modulators can be implemented with the distributed feedback topology and the feedforward topology.

In the traditional feedback topology, every integrator output contains the component of the input signal, which results in large internal voltage swings, and leads to stringent linearity requirements to amplifiers, especially in the low-voltage applications [Sil01].

According to Eq. 2.27, the input-feedforward loop filter processes the shaped quantization noise only, and hence the internal voltage swings are significantly reduced. Since the threshold voltage of the transistor does not scale down at the same rate as the supply does, the allowable voltage swing is greatly reduced under the low voltage supply. In this case, the feedforward topology, which provides smaller voltage swings, is more suitable for the low-voltage applications than the feedback topology. Furthermore, the reduced internal swing also relaxes the amplifier's linearity requirement, the amplifier's slew rate requirement, as well as the current consumption. Therefore, the input-feedforward topology is adopted in this design.

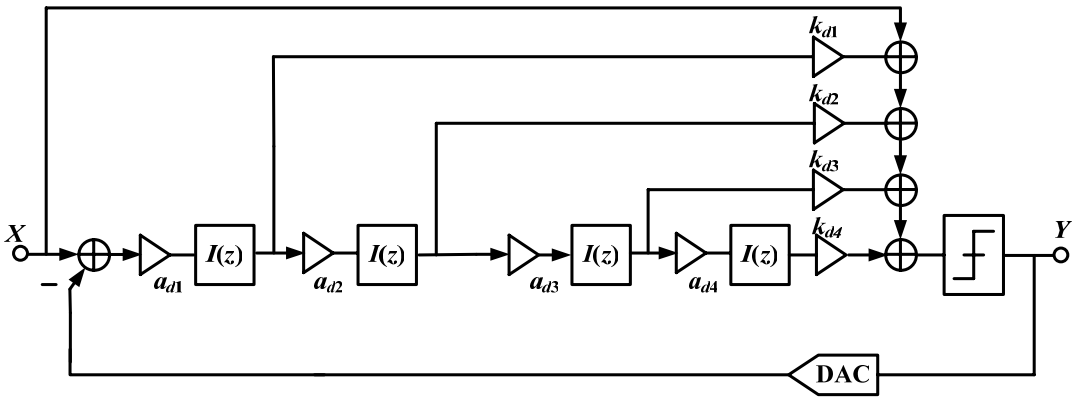


Figure 4.1: The 4th-order discrete-time input-feedforward Delta-Sigma modulator structure.

A 4th-order single-bit DT Delta-Sigma modulator with optimized coefficients is used as the original model for this design [Yao05], as shown in Fig. 4.1. Since the inherently linear single-bit quantizer is used, the calibration circuits are avoided, and hence the digital part of the single-bit Delta-Sigma modulator can be implemented with much lower power and much smaller area than that of the multi-bit counterpart. Based on the original model, zero optimization technique is utilized to further suppress the in-band quantization noise. And then it is mapped to the equivalent CT Delta-Sigma modulator.

B. *Zero Optimization*

The coefficients of the original structure are given in [Yao05], which are a_d = [0.2, 0.4, 0.1, 0.1], k_d = [1, 1, 1, 2]. By substituting the integrator's transfer function with 1/(z-1), the transfer function of the loop filter can be derived as:

$$L(z) = \sum_{i=1}^{4} \frac{k_i \prod_{j=1}^{i} a_j}{(z-1)^i}. \tag{4.1}$$

According to Eq. 2.16, NTF = 1/(1-L(z)). By combining Eq. 2.16 and Eq. 4.1, and substituting coefficient values, the NTF of this structure can be derived as:

$$NTF(z) = \frac{(z-1)^4}{z^4 - 3.8z^3 + 5.48z^2 - 3.552z + 0.8736}, \tag{4.2}$$

where the quantize gain is assumed to be unity. With this NTF, the peak SQNR is about 94 dB with an oversampling ratio of 64.

Equation 4.2 implies that, the time constants a_i (i=1-4) only affect the locations of the NTF's poles, whereas, the zeros are kept unchanged at dc ($z = e^0 = 1$). However, by moving the zeros away from dc, the in-band noise power can be further suppressed [Nor97].

To optimize the NTF for the best SNR performance, the in-band noise power is derived as:

$$Noise_{in-band} = \int_0^{\omega_B} E_{psd}(\omega) \cdot \left|NTF(\omega)\right|^2 d\omega . \tag{4.3}$$

where $E_{psd}(\omega)$ is the power spectral density of the noise, and ω_B is the signal bandwidth.

According to Eq. 4.2, the NTF magnitude is proportional to $|1- e^{-j\omega}|^4$, by replacing z with $e^{j\omega}$. For the band of interest, its frequencies are much lower than the sampling frequency, due to the oversampling effect. If the sampling frequency is normalized to 1, $e^{-j\omega}$ approximately equals $1-j\omega$, and hence the in-band magnitude of NTF is proportional to ω^4. Assuming NTF zeros are away from dc to $e^{\pm j\alpha}$ and $e^{\pm j\beta}$, the in-band NTF magnitude becomes proportional to $(\omega^2-\alpha^2)\cdot(\omega^2-\beta^2)$. Therefore, the in-band noise power can be translated into:

$$Noise_{in-band} \propto \int_0^{\omega_B} (\omega^2 - \alpha^2)^2 \cdot (\omega^2 - \beta^2)^2 d\omega = N(\alpha, \beta) . \tag{4.4}$$

In Eq. 4.4, the approximation is made by assuming that $E_{psd}(\omega)$ is a constant. This is true because the quantization noise in the Delta-Sigma modulator can be seen as white noise [Gra90] [Che00]. By finding the minimum value of Eq. 4.4, the optimized zeros for the 4th-order Delta-Sigma modulator can be derived as [Nor97]:

$$\alpha = \pm\sqrt{\frac{3}{7} + \sqrt{(\frac{3}{7})^2 - \frac{3}{35}}}\,\omega_B ,$$

$$\beta = \pm\sqrt{\frac{3}{7} - \sqrt{(\frac{3}{7})^2 - \frac{3}{35}}}\,\omega_B . \tag{4.5}$$

According to Eq. 4.5, for an OSR of 64 with the normalized frequency 1, the optimized zero locations are α = ±0.0167, and β = ±0.04230. Thus the relevant values of those zeros are 0.9999±0.0167i, and 0.9991±0.0423i, which approximately equal to 1±0.0167i, and 1±0.0423i. And the optimized numerator of the NTF can be derived as:

$$(z^2 - 2z + 1.0003)(z^2 - 2z + 1.0018) . \tag{4.6}$$

The two pairs of optimized zeros can be implemented by using two local feedbacks in the modulator, as shown in Fig. 4.2. The numerator of its NTF can be derived as:

$$(z^2 - 2z + 1 - g_{d1}a_{d1}a_{d2})(z^2 - 2z + 1 - g_{d2}a_{d3}a_{d4}), \tag{4.7}$$

where g_{d1} and g_{d2} are the local feedback coefficients. Combining Eq. 4.6 and Eq. 4.7, the local feedback coefficients can be determined:

$$g_d = [0.0037, 0.18]. \tag{4.8}$$

The NTF of the optimized structure is changed to:

$$NTF_{op}(z) = \frac{z^4 - 4z^3 + 6.002z^2 - 4.004z + 1.002}{z^4 - 3.8z^3 + 5.482z^2 - 3.556z + 0.8755}. \tag{4.9}$$

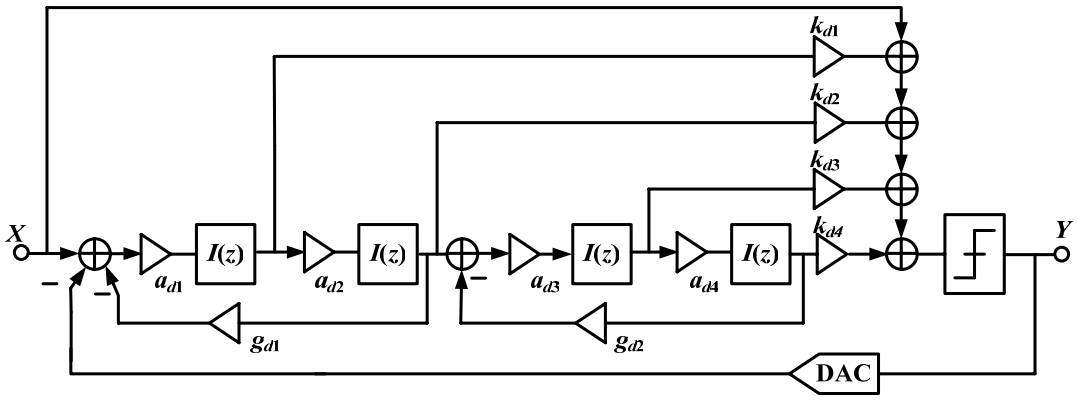
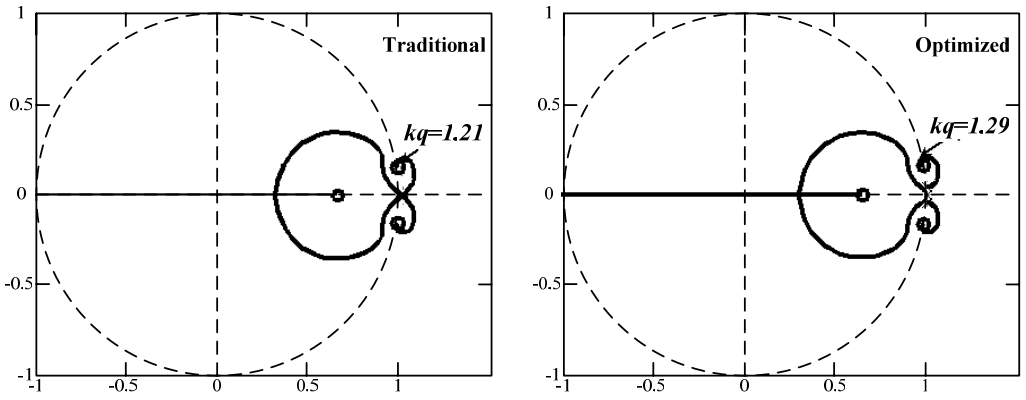


Figure 4.2: The 4th-order discrete-time input-feedforward Delta-Sigma modulator structure with two local feedbacks.

The denominator of Eq. 4.9 is almost the same as that of Eq. 4.1, which implies that, the poles are kept almost unchanged after the zero optimization. In other words, the stability performance is kept almost unchanged in the optimized structure. This can be proved by the root locus plots in Fig. 4.3. As shown in the figure, after zero optimization, the critical quantizer gain changes from 1.21 to 1.29, just a little bit higher than before. In addition, the STF is still 1, which is not changed.

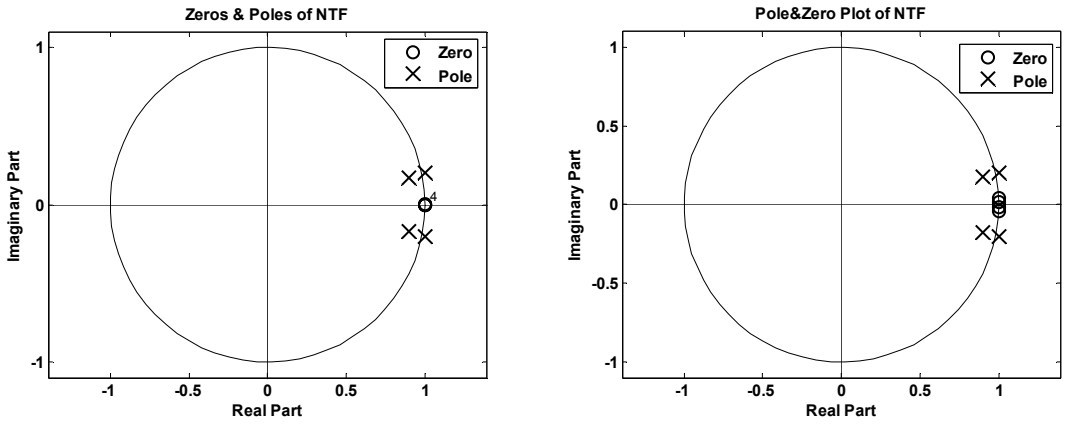
Fig. 4.4 shows the zero/pole plots of the 4th-order input-feedforward Delta-Sigma modulators with the traditional structure, and with the zero-optimized structure. As shown in the figure, the optimized zeros are moved away from dc. In Fig. 4.5, the magnitudes of the two NTFs are compared. Since the zeros are moved into the band of interest, the in-band magnitude of the zero-optimized NTF tends to be flat.

Fig. 4.6 shows the output spectrum of the traditional and the zero-optimized input-feedforward modulators, where the solid lines represent the cumulative noise powers, f_B is the signal bandwidth. Simulation results show that the peak SQNR of the zero-optimized modulator is 107 dB, which is 13 dB higher than the traditional one.



(a) (b)

Figure 4.3: Root locus plots of the 4th-order input-feedforward Delta-Sigma modulators, with the traditional structure (a), and with the zero-optimized structure (b).



(a) (b)

Figure 4.4: The zero/pole plots of the 4th-order input-feedforward Delta-Sigma modulators, with the traditional structure (a), and with the zero-optimized structure (b).

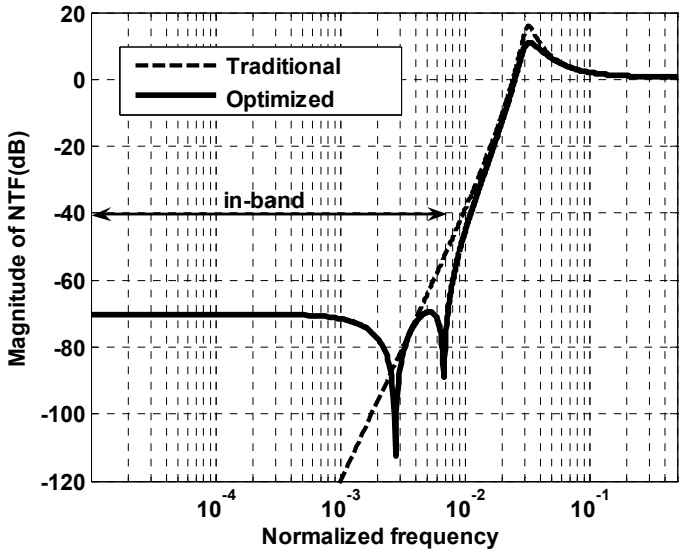
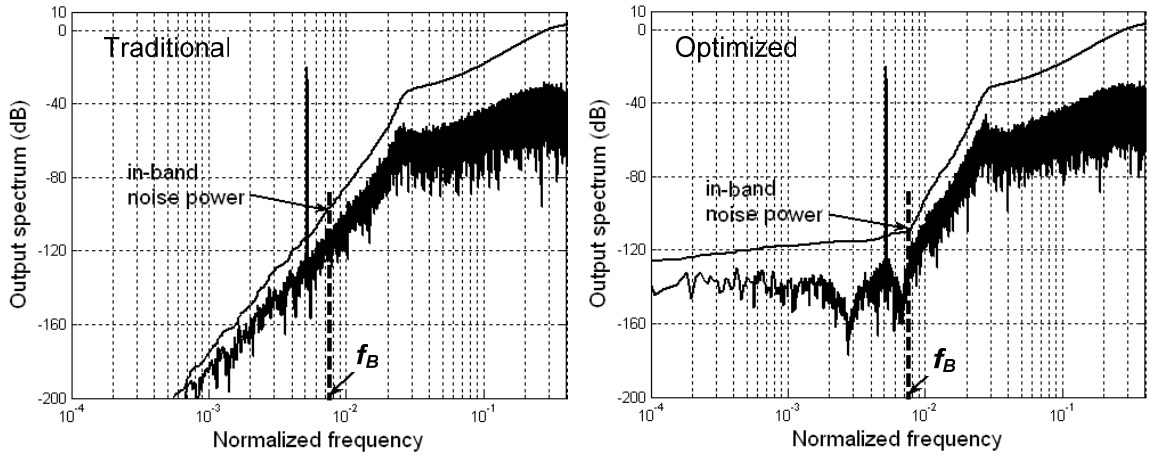


Figure 4.5: NTF magnitudes of the 4th-order input-feedforward Delta-Sigma modulators, without zero optimization (dashed line), and with zero optimization (solid line).



(a) (b)

Figure 4.6: Output spectrum of the 4th-order input-feedforward Delta-Sigma modulators, without zero optimization (a), and with zero optimization (b).

The trade-off for the SQNR improvement is the circuit complexity. According to Fig. 4.2, two additional feedback loops are introduced in the zero-optimized structure. Considering that g_{d1} is too small to implement, this local feedback loop is eliminated in this design. Simulation results show that such a simplification only causes about 2.5-dB SQNR degradation.

The zero-optimized DT Delta-Sigma modulator was mapped to the equivalent CT Delta-Sigma modulator with the method discussed in Chapter 3. The 4th-order continuous-time input-feedforward Delta-Sigma modulator structure used in this design is shown in Fig. 4.7. Its coefficients are listed in Table 4.1.

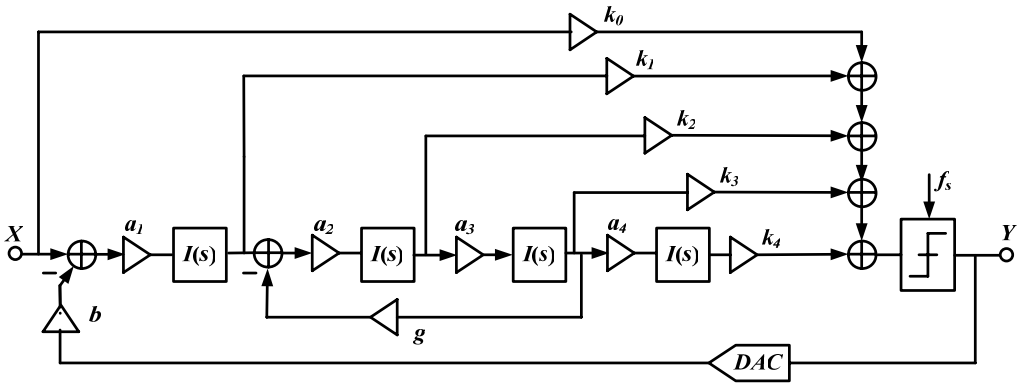


Figure 4.7: The 4th-order continuous-time input-feedforward Delta-Sigma modulator.

Table 4.1 Loop coefficients for the 4th-order 1-bit continuous-time wideband Delta-Sigma modulator with the input-feedforward topology.

a_1	0.1	k_1	0.4
a_2	0.4	k_2	0.46
a_3	0.1	k_3	0.35
a_4	0.4	k_4	0.25
b	2	g	0.045
k_0	0.25		

4.2.2 Considerations to the nonidealities in the Continuous-Time Delta-Sigma Modulator

Necessary considerations must be given to the internal swing, and nonidealities, such as the clock jitter and the excess loop delay, since they possibly degrade the performance of CT Delta-Sigma modulators seriously.

As discussed in Chapter 3, clock jitter refers to the timing uncertainty of the clock, and results in error sequence in DAC signals. For the wideband and uncorrelated jitter, the DAC error sequence introduces white in-band noise, and hence degrades the modulator resolution [Ris94]. In Fig. 4.8, the impact of the clock jitter on the SNR of the Delta-Sigma modulator with a −3-dBFS input is illustrated, where the clock jitter is expressed as the percentage of the clock period T_s. The non-

return-to-zero pulse is chosen as the shape of DAC in this design. Compared to the Return-to-Zero and the Half-delayed Return-to-Zero pulses, the NRZ pulse is less sensitive to the clock jitter effect [Che99-a]. Furthermore, the NRZ DAC pulse relaxes the slew rate requirement to the 1st integrator, such that the amplifier can possibly consume less power.

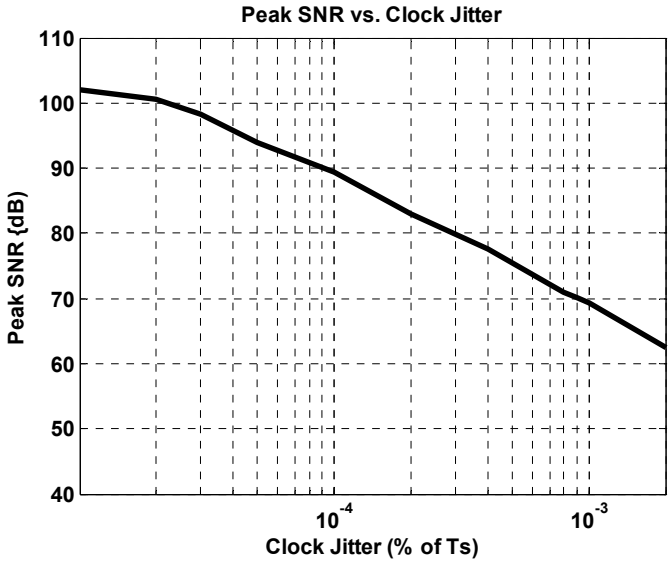


Figure 4.8: Impact of the clock jitter on the SNR of the 4th-order 1-bit wideband Delta-Sigma modulator, for the −3-dBFS input.

Excess loop delay refers to the delay between the edge of the quantizer clock and the feedback pulse. Such a delay can increase the noise floor, and even lead to an unstable system [Che99-b]. The impact of the excess loop delay on the SNR of the Delta-Sigma modulator with a −3-dBFS input is shown in Fig. 4.9. As the figure indicates, the modulator becomes unstable when the excess loop delay exceeds 17% of the clock period, which is around 1 ns for this design. Thanks to the single-bit quantizer and 0.13-μm process used, the quantizer latency can be kept much smaller than 1 ns. In this case, the excess loop delay is not a problem for this design, and hence

there is no necessary for additional compensation techniques, which are usually applied in multi-bit CT Delta-Sigma modulators [Gia03] [Pat04] [Yan04] [Li07].

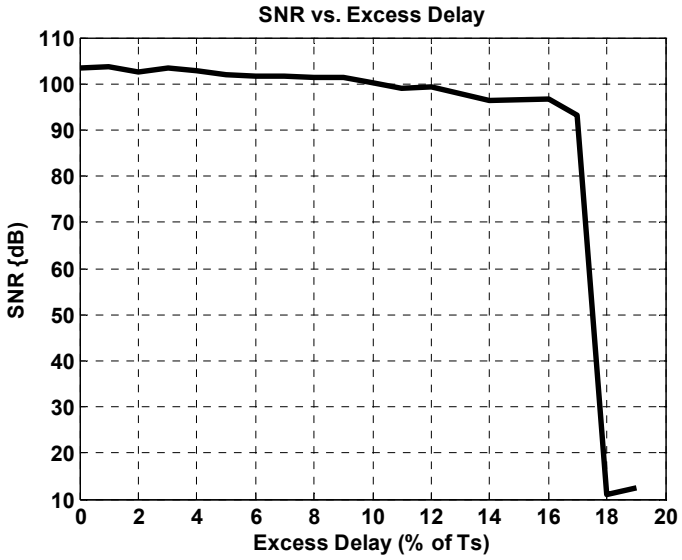


Figure 4.9: Impact of the excess delay on the SNR of the 4th-order 1-bit wideband Delta-Sigma modulator, for the −3-dBFS input.

4.3 Circuit Implementation

4.3.1 Proposed Structure

As mentioned in Section 4.1, in some traditional designs, CT feedforward paths can be implemented with transconductors, by which signals are converted from voltage into current before they are summed [Gia03] [Pat04] [Yan04] [Li07]. As an example for a 4th-order input-feedforward Delta-Sigma modulator, five transconductors are necessary [Yan04], as shown in Fig. 4.10. Each transconductor comprises some transistors, including the input pair, the loads, and the current source, which increase power consumption, area, and also complex the circuit design.

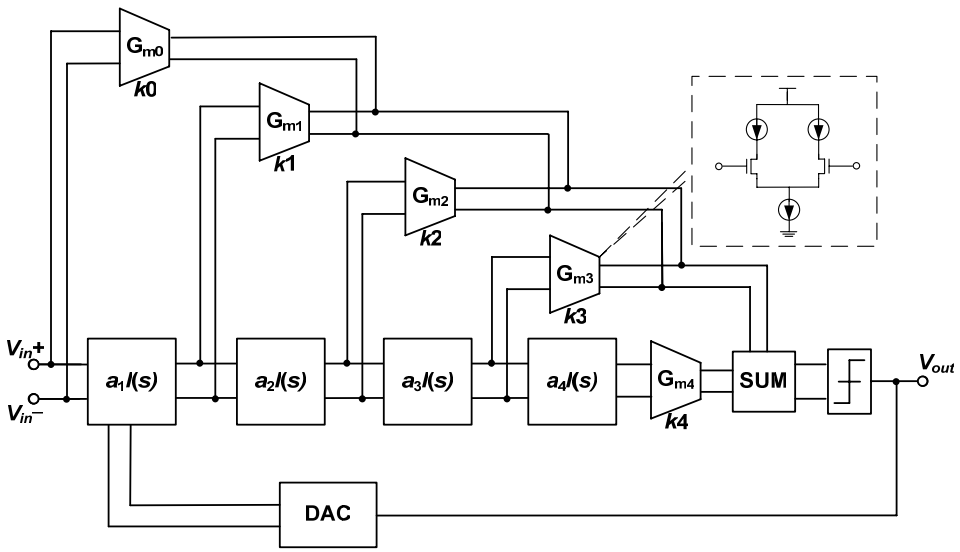


Figure 4.10: Traditional 4th-order continuous-time input-feedforward Delta-Sigma modulator, with transconductors in feedforward paths.

To save the feedforward transconductors, a simple structure was proposed in [Sch04]. In this structure, all the integrators are implemented with active-RC filters, and the feedforward coefficients are realized as the ratios of the feedforward capacitances to the integration capacitance. As shown in Fig. 4.11, for a 4th-order input-feedforward Delta-Sigma modulator, the feedforward coefficients can be implemented by satisfying the equation below:

$$k_i : k_4 = C_{ki} : C_4, \tag{4.10}$$

where k_i (i = 0-4) represents the feedforward coefficient, C_{ki} (i = 0-3) represents the feedforward capacitance, and C_4 is the integration capacitance of the 4th integrator.

However, the additional loads, i.e. the feedforward capacitances C_{ki}, were introduced to integrators. The feedforward capacitances are comparable with the integration capacitance C_4, which is normally at least hundreds of fF or even a few pF. And therefore, an amount of current and area are consumed by the feedforward capacitances.

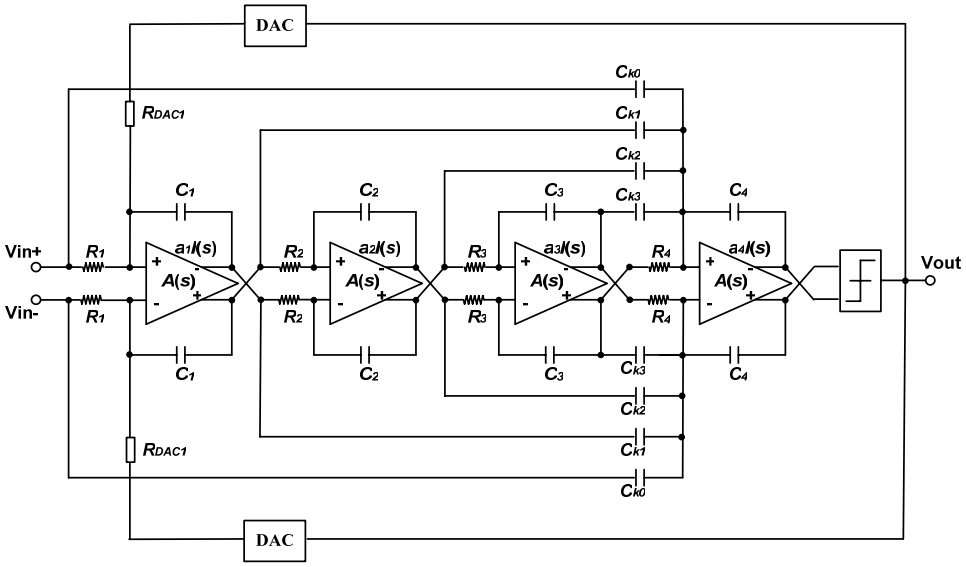


Figure 4.11: Traditional 4th-order continuous-time input-feedforward Delta-Sigma modulator, with capacitors in feedforward paths.

A novel structure is proposed for the feedforward and summing part in this design [Zha09], as shown in Fig. 4.12. The integrator outputs are directly connected to input transistors of the quantizer, and only one pair of transistors involve in each feedforward path. The additional loads of integrators are determined by the input capacitances of the quantizer. These capacitances can be limited to relatively small values (less than 50 fF in this design) by sizing input transistors of the quantizer. In this way, the new structure possibly consumes much lower power in the feedforward paths, compared to conventional structures mentioned above. Similarly, the new structure possibly consumes much less area as well. The operation of this structure will be explained in Section 4.3.4 with the quantizer design.

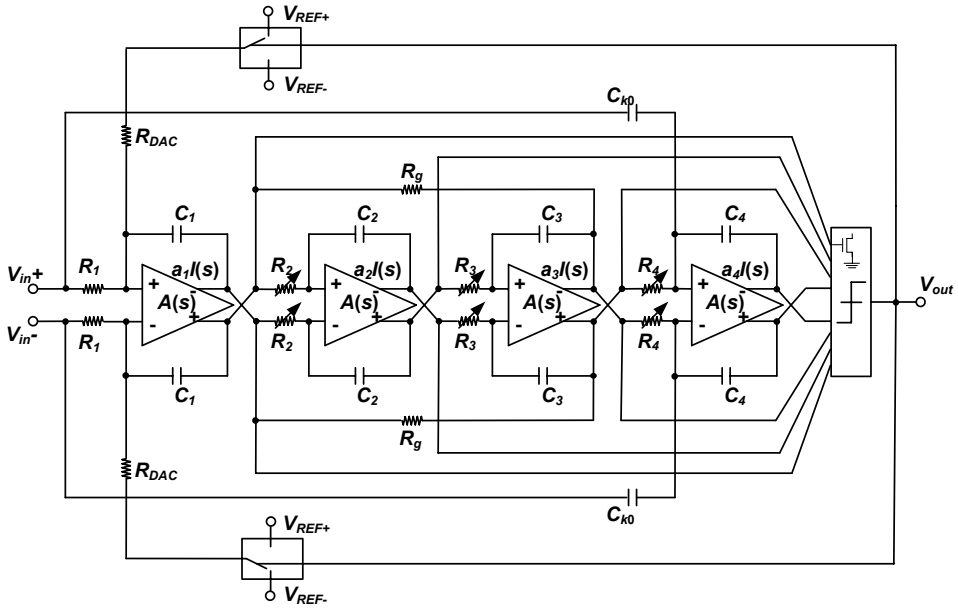


Figure 4.12: Proposed 4th-order input-feedforward Delta-Sigma modulator, the feedforward paths are embedded in the quantizer.

4.3.2 Noise Analysis

As shown in Fig. 4.12, all the integrators are implemented with active-RC filters due to their good linearity and parasitic insensitivity. Furthermore, the active-RC filter is very suitable for the low-voltage operation, because its virtual ground relaxes the constraint of amplifier's input range.

As no nonidealities are shaped by the loop filter, the input stage directly determines the performance of the modulator. To analyze the noise contributions of the input stage, a schematic model is shown in Fig. 4.13. As shown in Fig. 4.13, there are three main noise sources at the input stage, including the input resistors R_1, the DAC resistors R_{DAC}, and the 1st amplifier. Obviously, the noise from R_1 is input referred. The input-referred noise of the 1st amplifier and R_{DAC} will be derived as follows.

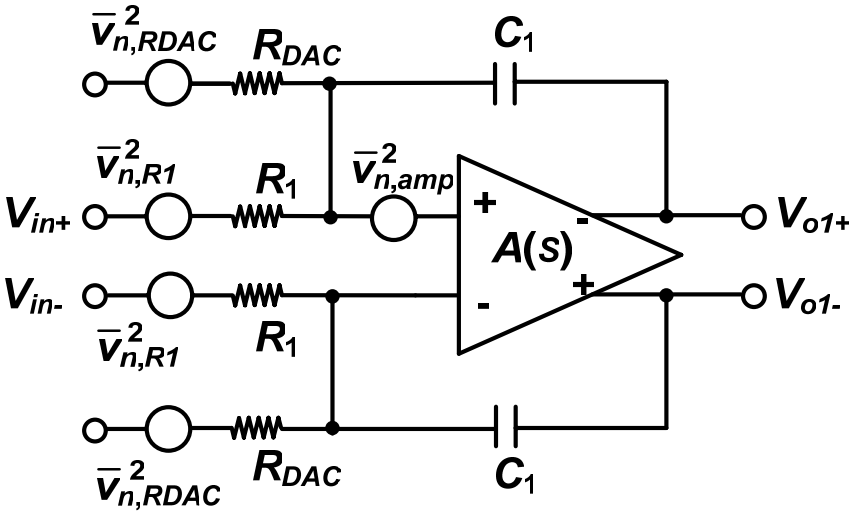


Figure 4.13: Noise sources at the input stage.

It is well known that the input-referred noise equals the output referred noise divided by the gain, which can be expressed as:

$$\sqrt{\overline{v}^2_{n,in}} = \frac{\sqrt{\overline{v}^2_{n,out}}}{A_v}. \tag{4.11}$$

where A_v is the gain of the input stage. Assuming the amplifier is the only noise source, the transfer function of its noise can be derived as:

$$A(s)\left(\sqrt{\overline{v}^2_{n,out}}\frac{R_1}{R_1 + R_{DAC} \,//\, 1/sC_1} + \sqrt{\overline{v}^2_{n,amp}}\right) = \sqrt{\overline{v}^2_{n,out}}, \tag{4.12}$$

where $A(s)$ is the gain of the amplifier. Assuming the amplifier has infinite gain and gain-bandwidth, the output noise can be approximately expressed as:

$$\sqrt{\overline{v}^2_{n,out}} \approx \frac{R_1 + R_{DAC} \,//\, 1/sC_1}{R_1}\sqrt{\overline{v}^2_{n,amp}}. \tag{4.13}$$

The gain of the input stage can also be derived as:

$$A_v = \frac{v_{out}}{v_{in}} \approx \frac{R_{DAC} \,//\, 1/sC_1}{R_1}. \tag{4.14}$$

Combining Eq. 4.11, Eq. 4.13, Eq. 4.14, the input-referred noise of the amplifier can be derived as:

$$\begin{aligned}\sqrt{\overline{v_{n,in,amp}^2}} &= \frac{\sqrt{\overline{v_{n,out}^2}}}{A_v} \approx \frac{R_1 + R_{DAC} \,//\, 1/sC_1}{R_1}\sqrt{\overline{v_{n,amp}^2}} \cdot \frac{R_1}{R_{DAC} \,//\, 1/sC_1} \\ &= \left(1 + \frac{R_1}{R_{DAC}} + \frac{R_1}{1/sC_1}\right)\sqrt{\overline{v_{n,amp}^2}} \\ &\approx \left(1 + \frac{R_1}{R_{DAC}}\right)\sqrt{\overline{v_{n,amp}^2}}\,. \end{aligned} \tag{4.15}$$

The input-referred noise of the DAC resistances can be derived in the similar way. Therefore, the total input-referred noise power can be expressed as:

$$\overline{v_{n,in}^2} \approx 2\left(\overline{v_{n,R_1}^2} + \overline{v_{n,R_{DAC}}^2}\frac{R^2}{R_{DAC}^2}\right) + \overline{v_{n,amp}^2}\left(1 + \frac{R}{R_{DAC}}\right)^2, \tag{4.16}$$

which is consistent with the expression in [Ger03].

4.3.3 Integrator Design

The integrators are implemented with active-RC filters, and their coefficients a_i (i = 1-4, see Table 4.1) are realized by products of integration resistances and capacitances. The transfer function of the integrator is:

$$\frac{a_i f_s}{s} = \frac{1}{sR_iC_i}, \tag{4.17}$$

As mentioned in Section 4.3.2, the input resistors contribute input-referred noise to the modulator. Based on Eq. 4.16, the input-referred noise due to the input resistors is:

$$N_{p,R_1} = 8kTf_BR_1, \tag{4.18}$$

where k is Boltzmann constant, T is temperature, f_B is the signal bandwidth.

Within the tolerable in-band noise, the maximum value should be chosen for R_1 due to the two reasons. First, according to Eq. 4.17, larger R_1 leads to smaller C_1, and hence lower power consumption. Second, the larger R_1 also leads to the better linearity performance. The third harmonic distortion of the active-RC filter can be expressed as [Bre99]:

$$HD_3 \approx \frac{V_{in}^2}{64 g_m R_1^3 I_D^2}(1 + R_1 / R_{DAC}), \tag{4.19}$$

where V_{in} is the input amplitude, g_m is the transconductance of the amplifier, and I_D is the current of the amplifier. Eq. 4.19 proves that HD_3 can be reduced by increasing the integration resistance. In this design, R_1 = 64 kΩ, giving the thermal noise 85 dB below the full-scale input signal.

The fully-differential two-stage Miller compensation amplifier is used in the integrator, whose schematic is shown in Fig. 4.14. The fully-differential technique is applied to suppress the even-order harmonics and common-mode noise. One common-mode feedback (CMFB) loop for the two-stage amplifier is applied. As shown in Fig. 4.15, the CMFB circuit senses the output common-mode through two large resistors, and provides the control biasing voltage directly to the first stage. NMOS transistors M_{5A} and M_{5B} are carefully sized to achieve a good phase margin of the CMFB loop.

The amplifier noise includes the thermal noise and the flicker noise. The thermal noise power of the amplifier can be derived as:

$$\overline{v}_{n,th}^2 \approx 8kT\gamma\left(\frac{1}{g_{m1}} + \frac{g_{m4} + g_{m5}}{g_{m1}^2}\right), \tag{4.20}$$

And the flick noise of the amplifier can be derived as:

$$\overline{v}_{n,1/f}^2 = \frac{1}{f}\frac{2K_P}{C_{ox}(WL)_1} + \frac{1}{f}\frac{2K_N}{C_{ox}(WL)_4}\frac{g_{m4}^2}{g_{m1}^2} + \frac{1}{f}\frac{2K_N}{C_{ox}(WL)_5}\frac{g_{m5}^2}{g_{m1}^2}. \tag{4.21}$$

The total noise power of the amplifier can be expressed as:

$$N_{p,Amp} = 8kT\gamma(\frac{1}{g_{m1}} + \frac{g_{m4}+g_{m5}}{g_{m1}^2})f_B + \frac{2}{C_{ox}}(\frac{K_P}{(WL)_1} + \frac{K_N}{(WL)_4}\frac{g_{m4}^2}{g_{m1}^2} + \frac{K_N}{(WL)_5}\frac{g_{m5}^2}{g_{m1}^2}) \cdot \ln(f_B / f_{\min}) .$$

(4.22)

Based on Eq. 4.22, PMOS transistors M_{1A}, M_{1B}, and NMOS transistors M_{4A}, M_{4B}, M_{5A}, M_{5B} are sized with large dimensions to lower down the flicker noise. The total biasing current value of the 1st integrator is 0.96 mA to ensure reasonable low thermal noise.

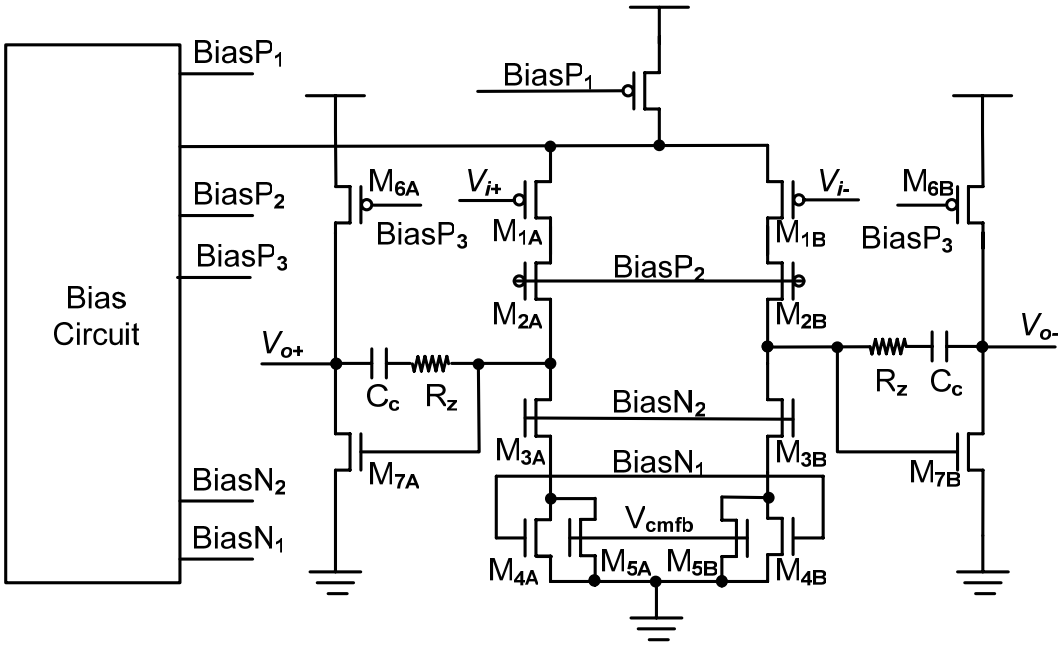


Figure 4.14: Two-stage Miller compensation amplifier.

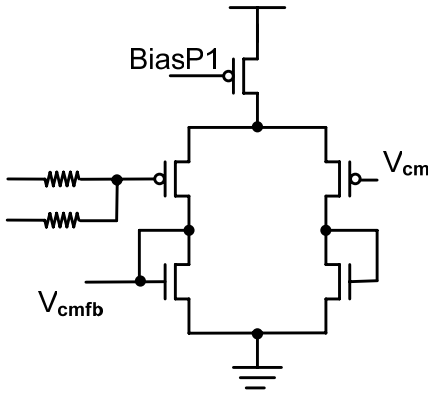


Figure 4.15: Common-mode feedback circuit.

For the following stages, their nonidealities are suppressed by the noise-shaping effect, as shown in Fig. 4.16. Therefore, the noise and slew rate requirements on the following stages are relaxed. For the simplicity, amplifiers of the 2nd to 4th integrators are designed with the same parameters. To reduce the power consumption, small capacitance is chosen for integration capacitors C_2-C_4 (see Fig. 4.12), which is 200 fF. The total static current consumed by the three integrators is 0.84 mA. The simulated performances of the amplifiers are shown in Table 4.2.

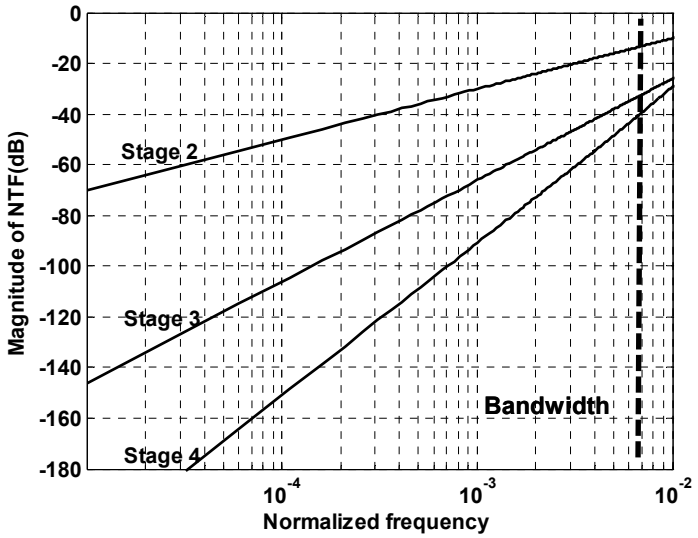


Figure 4.16: Noise shaping effects at different stages in the modulator.

Table 4.2 Simulated performances of the amplifiers in the 1-bit wideband Delta-Sigma modulator.

Parameter	1st	2nd-4th
GBW (MHz)	430	404
dc gain (dB)	76.3	75.4
Phase Margin (degree)	70	68
In-band noise (μV)	19.58	-
Load (fF)	980	200
Static Current (μA)	960	280

4.3.4 Quantizer Design

As shown in Fig. 4.17, the quantizer comprises one comparator and one D latch. Different from other two-input comparators, an eight-input comparator is used in this design. The eight inputs are connected with the integrator outputs from the 1st stage to the 4th stage, which are represented as V_{o1} to V_{o4} in Fig. 4.17.

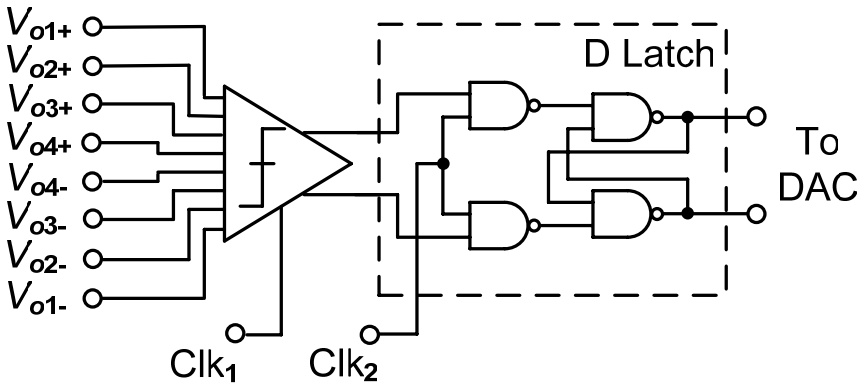


Figure 4.17: Circuit blocks of the quantizer.

The feedforward coefficients are realized with a power-efficient and area-efficient structure [Zha09]. In this structure, the combination of feedforward paths and the summing of the

feedforward coefficients is embedded into the comparator. Fig. 4.18 shows the eight-input comparator used in this design. The eight inputs are connected to the outputs of the four integrators, which are represented as V_{o1}, V_{o2}, V_{o3}, and V_{o4}, respectively. The input transistors M_i (i=1-4) are designed with the same length but different widths.

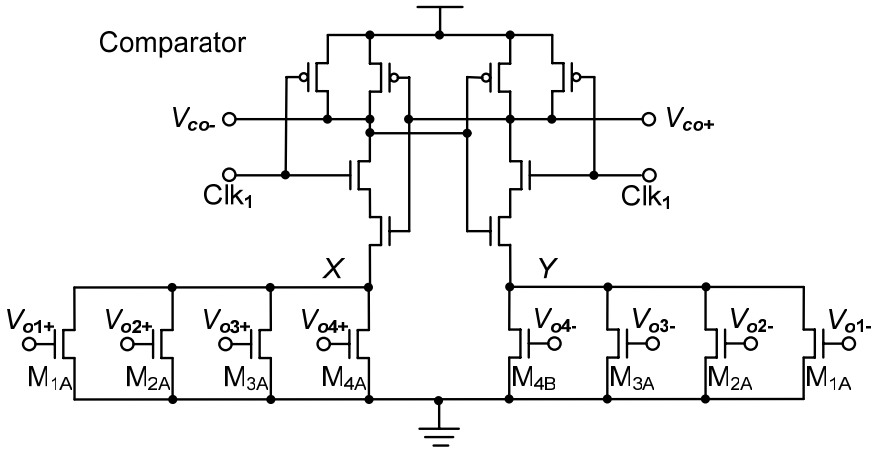


Figure 4.18: Schematic of the multi-input comparator.

The operation of the comparator is as follows. When Clk_1 is at GND, the comparator is reset. Its outputs V_{co+}, V_{co-} are driven to VDD and nodes X and Y are pulled down to GND. When Clk_1 changes to VDD, the comparator is activated. Due to the small integrator outputs and the low threshold voltage, transistors M_1-M_4 are working under linear region. The currents at nodes X and Y can be derived as:

$$I_X = \sum_{i=1}^{4} I_i = \mu_n C_{ox} \sum_{i=1}^{4} \frac{W_i}{L} (V_{oi+} - V_{THN} - \frac{V_X}{2}) V_X \,, \tag{4.23}$$

$$I_Y = \sum_{i=1}^{4} I_{i+4} = \mu_n C_{ox} \sum_{i=1}^{4} \frac{W_i}{L} (V_{oi-} - V_{THN} - \frac{V_Y}{2}) V_Y \,, \tag{4.24}$$

where V_X and V_Y are voltages at nodes X and Y, L is the channel length, W_i=W_{i+4}, representing the channel width of the transistor, and V_{THN} is the threshold voltage of transistors. By approximately assuming that $V_X = V_X$, and their values are near zero, Eq. 4.23 and Eq. 4.24 can be translated into:

$$I_X - I_Y = \frac{\mu_n C_{ox} V_X}{L} \sum_{i=1}^{4} W_i \cdot V_{oi}\,, \tag{4.25}$$

where $V_{oi} = V_{oi+} - V_{oi-}$, representing the difference of the i-th integrator output. The comparator senses this current difference, and amplifies its outputs to the full logic levels. According to Eq. 4.25, feedforward coefficients k_i (i = 1, …, 4) can be realized as the ratios of channel widths by satisfying the following equation:

$$k_1 : k_2 : k_3 : k_4 = 1 : 2 : 1 : 1 = W_1 : W_2 : W_3 : W_4\,. \tag{4.26}$$

The analysis above is conducted based on the assumption that the comparator input transistors work under linear region. This assumption is true for the typical case. Simulation shows that for a -3dBFS input signal, more than 99% of the integrator outputs are controlled within ±50% of the reference, which is ±0.3 V in this design. Since the common-mode level is 0.6 V, most of the integrator outputs are higher than 0.3 V. Considering that the threshold voltage V_{TH} is 0.16V, the comparator input transistors work under linear region. In practice, variations in the threshold voltage and in the integrator output swings may slightly lead the input transistors out of linear region, and hence will introduce coefficient errors. The random mismatches in the multi-input transistors also cause feedforward coefficient errors. However, because the feedforward signals are summed at the quantizer input, any error in the feedforward coefficient k_i (i = 1-4) can be suppressed by the noise-shaping effect. As to the input feedforward coefficient k_0, if k_0 is assumed to vary with the amplitude of the input signal X (see Fig. 4.7), the STF can be derived as:

$$STF = \frac{V}{U} = \frac{k_0(U) + L(s)}{1 + L(s)}, \tag{4.27}$$

where $L(s)$ represents the loop filter consisting of four integrator coefficients a_i (i=1-4) and four feedforward coefficients k_i (i=1-4). The relationship between the loop filter $L(s)$ and the NTF can be easily derived as [Sch05]:

$$L(s) = \frac{1}{NTF(s)} - 1\,. \tag{4.28}$$

Substituting Eq. 4.28 into Eq. 4.27, the STF can be derived as:

$$STF = \frac{V}{U} = NTF(s) \cdot \left[k_0(U) - 1\right] + 1. \tag{4.29}$$

Eq. 4.29 indicates that the non-linear part of the input feedforward coefficient is shaped by the noise transfer function. For the safety, the large input feedforward signal is implemented into the 4th integrator by the ratio of the feedforward capacitance C_{k0} to the integration capacitance C_4 (see Fig. 4.12), which is similar to the structure in [Sch04].

With this structure, each feedforward coefficient is realized by only one pair of transistors. In this design, transistors M_i (i=1−4) are sized so that their maximum gate-source capacitance is less than 50 fF. In this way, the feedforward paths consume very small current and area.

One problem in the comparator is that its regeneration time varies with the different input signals. As illustrated in Fig. 4.19, the regeneration time of the comparator increases if the input decreases. To avoid the impact of this signal-dependent effect, the digital output needs to be re-timed before it is fed back to the input. This retiming is carried out by introducing another clock Clk_2 in the D latch that follows the comparator. Clk_2 rises after Clk_1 rises and falls before Clk_1 falls. The schemes of Clk_1 and Clk_2 as well as the outputs of the comparator and D latch are shown in Fig. 4.20.

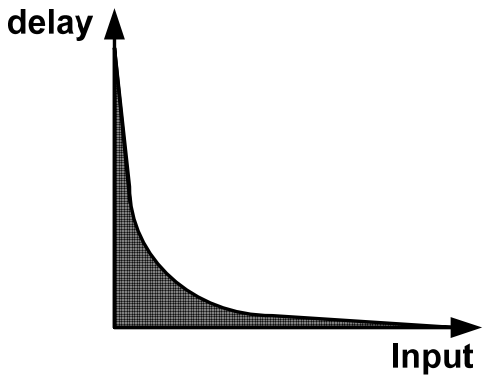


Figure 4.19: Signal-dependent comparator regeneration time.

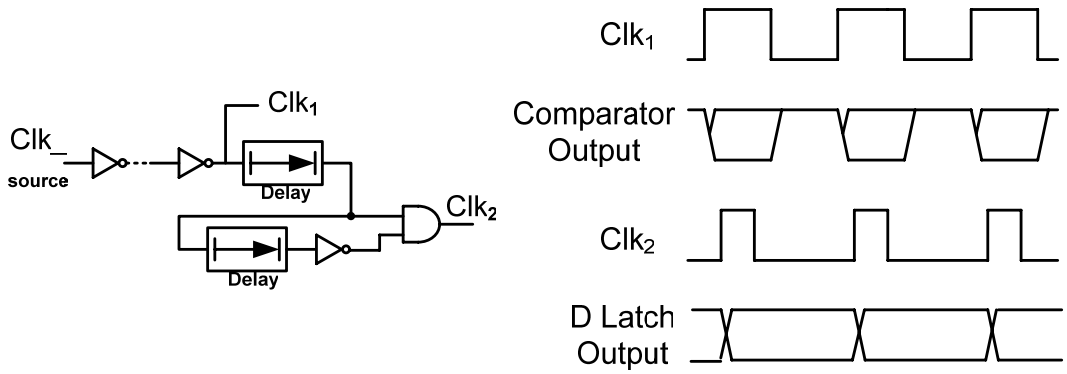


Figure 4.20: Scheme of the clocks for the comparator and the D latch.

4.3.5 Time-Constant Tuning

As discussed in Chapter 3, the performance of the CT Delta-Sigma modulator will be degraded by large time-constant shifts, which are caused by unavoidable process variations of resisters and capacitors. The total RC variation could be up to ±30% with the process used in this design. The solution to this nonideality is to tune either integration resistances or integration capacitances.

The capacitance tuning is not feasible in this design, since relatively small integration capacitances have been chosen to reduce the power, as mentioned before. Therefore, resistance tuning is adopted in this design. In Fig. 4.21, the tunable resistor is shown. A four-bit digital signal D[3:0] is used as the tuning signal to tune the integration resistances synchronously, achieving a tuning range of [R, R+15R^*], and a tuning unit of R^*.

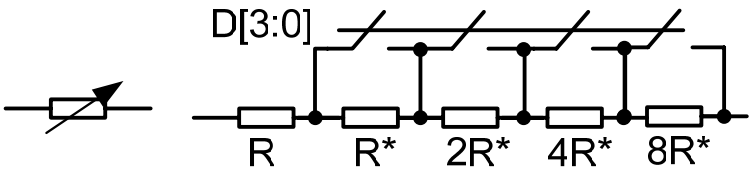


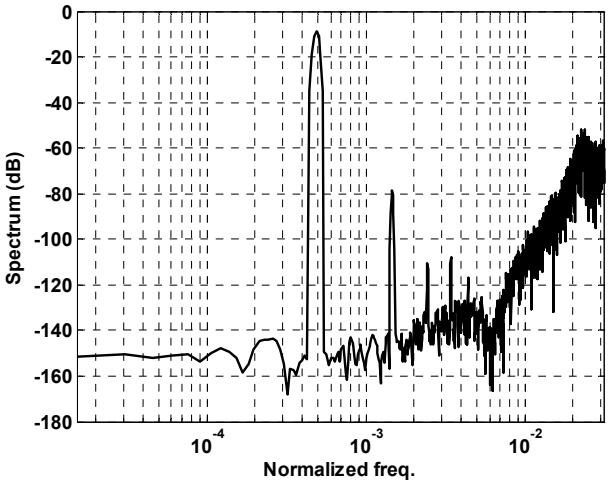
Figure 4.21: Tunable resistor.

One problem of the resistance tuning lies in the switches controlled by the tuning signal. When one switch is closed, its on resistance r_{on} can be expressed as:

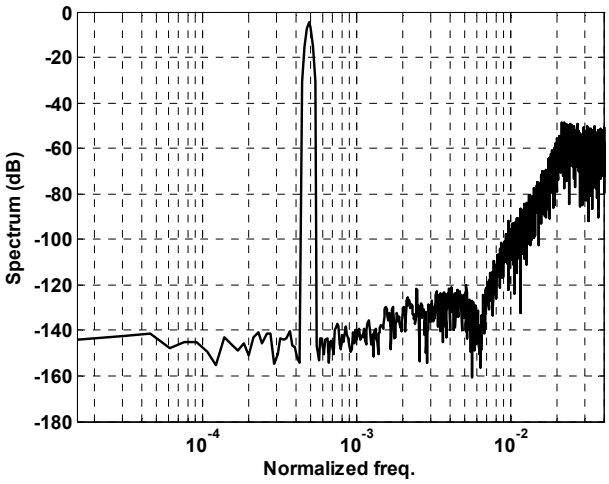
$$r_{on} = \frac{\partial V_{DS}}{\partial I_{DS}} = \frac{L}{\mu C_{ox} W (V_{GS} - V_{TH} - V_{DS})}, \tag{4.30}$$

where $V_{GS,}$ V_{DS}, V_{TH} are the gate-source voltage, drain-source voltage and threshold voltage, respectively. Equation 4.30 indicates that the switch's on-resistance is not linear, which will introduce distortions. The modulator with tunable integration resisitors R_1, R_2, R_3, and R_4 (see Fig. 4.12), was simulated. Fig. 4.22(a) shows the simulated output spectrum, where odd-order distortions emerge. Since there is no shaping effect at the input stage, distortions are mainly caused by the switches in R_1. To solve this problem, R_1 is fixed and only R_2 R_3 R_4 are tuned in this design. Fig. 4.22(b) shows the simulated output spectrum of the modulator with fixed R_1 and tunable R_2 R_3 R_4. The modulator shows good linearity performance without visible distortions, as any nonidealities at 2nd to 4th stages can be suppressed.

One question arising with the fixed R_1 is that, can the modulator tolerate the large time-constant variation at the 1st integrator? To answer this question, two worst cases have been simulated, in which the time-constant a_1 (see Fig. 4.7) is set with +30% variation and −30% variation respectively. SNR curves for a −3dBFS input are plotted versus time-constants a_2-a_4 (see Fig. 4.7) in Fig. 4.23. Time-constants a_2-a_4 are assumed to vary by the same percentage. The solid line represents the case when a_1 varies +30%, and the dashed line represents the case when a_1 varies -30%. According to the simulated results shown in Fig. 4.23, tunable resistances (see Fig. 4.21) have been carefully chosen for R_2 R_3 R_4 to keep a_2-a_4 within ±12% variations, and therefore, the modulator can be kept stable.



(a)



(b)

Figure 4.22: Output spectrum of the modulators with tunable R_1 R_2 R_3 R_4 (a), and the modulator with tunable R_2 R_3 R_4 but fixed R_1 (b), the input signal amplitude is −4dBFS.

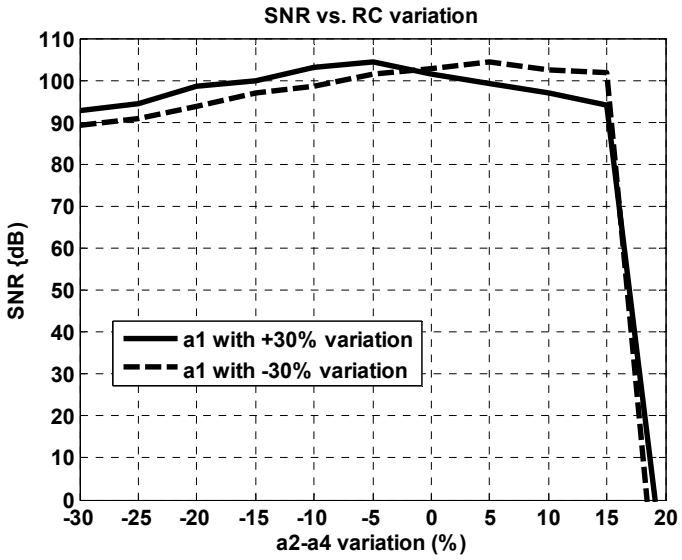


Figure 4.23: SNR versus time-constant variations in the 2^{nd}-4^{th} integrators, the input signal amplitude is −3 dBFS.

4.3.6 Layout

The prototype modulator was fabricated in a standard 0.13-μm CMOS process. High-resistivity poly resistors and Metal-Insulator-Metal (MIM) capacitors were used for their high linearity. Fig. 4.24 shows the chip die photo of the modulator, and the main blocks are labeled. Due to the novel structure for the feedforward and summing part, the core area of the modulator is 0.082mm^2.

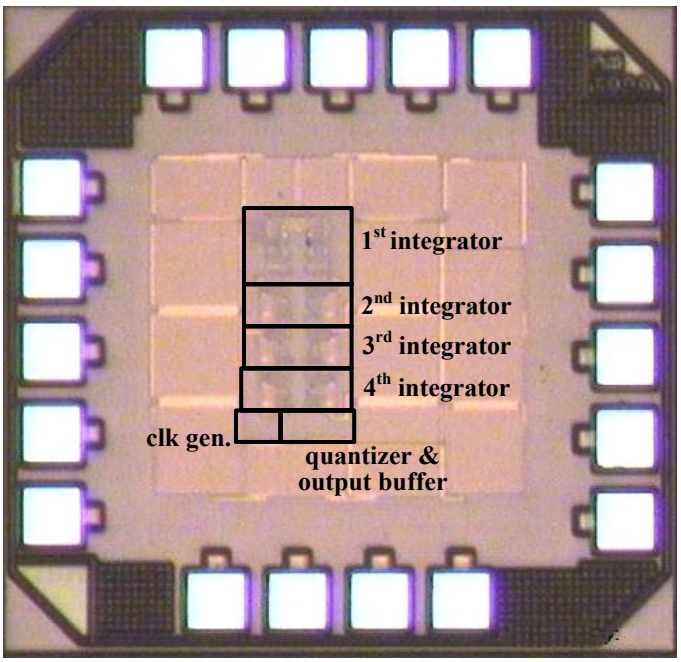


Figure 4.24: Die micrograph of the input-feedforward continuous-time wide-band Delta-Sigma modulator.

4.4 Test Setup

4.4.1 Printed Circuit Board Design

The printed circuit board (PCB) was designed to test the prototype chip. As shown in Fig 4.25, the PCB comprises four layers. The top and bottom layers are used to route signal lines, and the second and third layers are used as ground planes and supply planes, respectively.

As shown in Fig. 4.25, the ground and power planes are placed next to each other with less than 5-mil distance. In this way, the two planes form a bypass capacitance without ESR (effective series resistance) and ESL (effective series inductance). The ground and power planes are split for analog and digital uses. Analog and digital components are placed over respective planes.

Surface mount capacitors are used to minimize ESR and ESL, and the decoupling capacitors are placed near the pins. The differential input signals are routed with short and symmetrical lines.

The clock signal is routed with the straight, short line with a 50-Ω termination resistance.

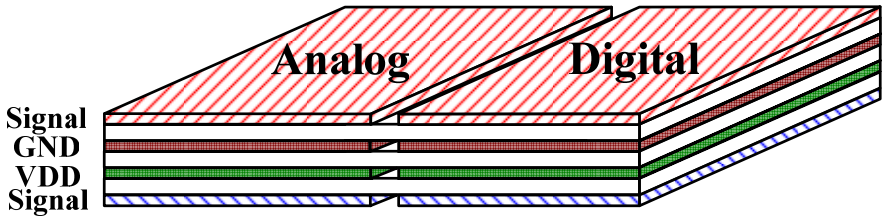
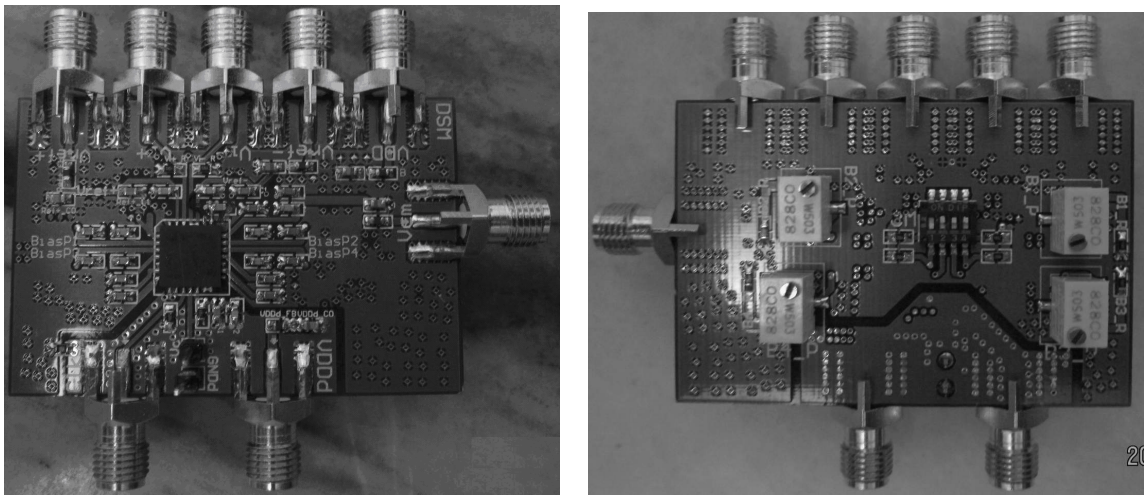


Figure 4.25: Four-layer printed circuit board.

The top view of the PCB is shown in Fig. 4.26(a). Almost all the analog and digital signals are routed on the top layer. Biasing and tuning circuits, which generate dc signals, are placed on the bottom layer as shown in Fig. 4.26(b).



(a) (b)

Figure 4.26: Photos of the printed circuit board, (a) the top view, (b) the bottom view.

4.4.2 Test Environment Setup

Fig. 4.27 shows the diagram for the test setup. The differential input signals are provided by synthesized function generator SRS (Stanford Research Systems) DS360 with ultra-low distortion.

Agilent 8133A pulse generator is used to provide the low-jitter clock. The prototype chips have been tested. The output data were captured by the mixed signal oscilloscope MSO6104A, and then processed with Matlab codes in a PC.

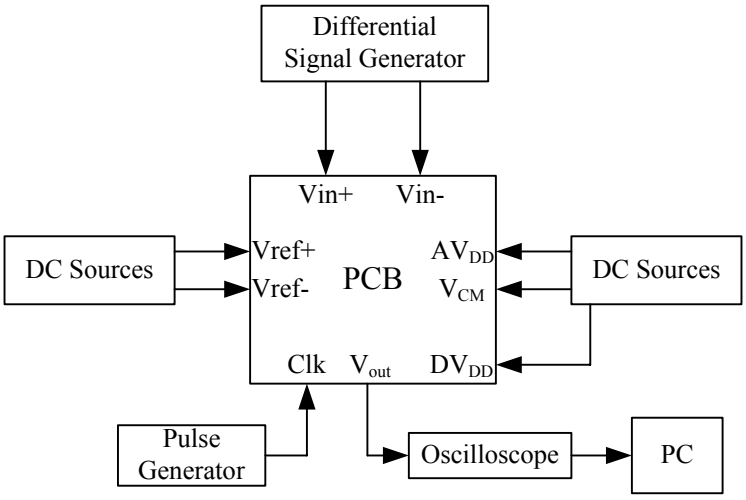


Figure 4.27: Experimental test setup.

4.5 Measurement Results

The prototype chips have been tested. Fig. 4.28 and Fig. 4.29 show the measured output spectrum for a −4-dBFS 80-kHz input signal and for a −48-dBFS 80-kHz input signal, respectively. As the figures illustrate, the in-band noise is dominated by the white noise. The clock jitter may account for this white noise. Since the clock generation circuit shares the same supply with other digital circuits, the high clock jitter may be generated by the noisy supply. For the designs in Chapter 5, dedicated supplies are used for clock generators. Another possible source for the high noise floor is the reference. In this design, no on-chip decoupling capacitors are put between the two reference levels. Since the reference noise is input-referred, it can be dominant. On-chip decoupling capacitors are also used in the designs in Chapter 5.

SNR and SNDR curves versus the input power are shown in Fig. 4.30. Measurement results show an achieved peak SNR of 67 dB, a peak SNDR of 66.1 dB, and a DR of 68 dB. The measured

performances are summarized in Table 4.3. Thanks to the CT input-feedforward topology, and the novel feedforward structure, the power consumption of the analog circuit is 2.5 mW. Thanks to the single-bit quantizer, the power consumption of the digital circuit (including the quantizer, DAC circuit, and clock generator) is 0.2 mW.

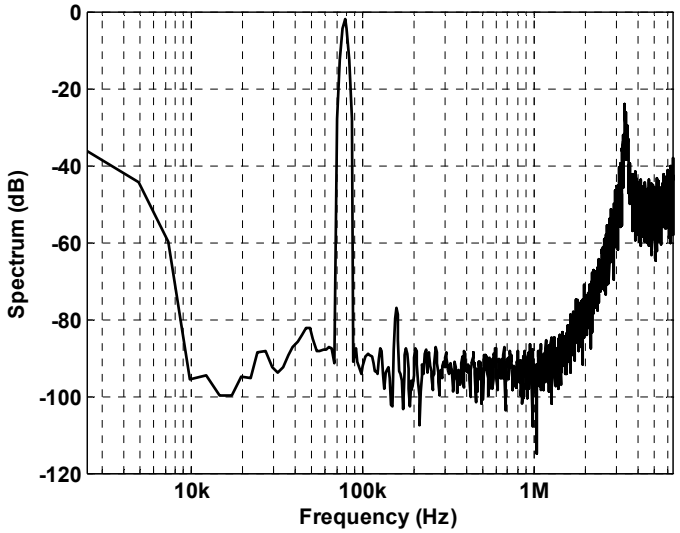


Figure 4.28: Measured output spectrum for the −4-dBFS 80-kHz input, FFT bins are 65536.

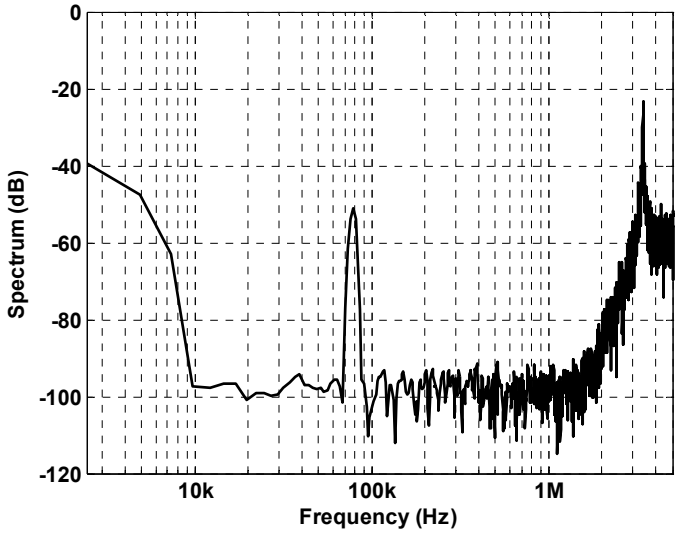


Figure 4.29: Measured output spectrum for the −48-dBFS 80-kHz input, FFT bins are 65536.

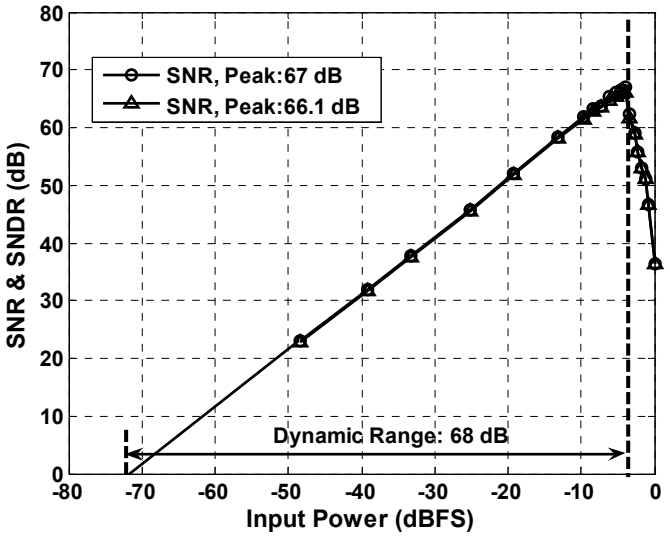


Figure 4.30: SNR/SNDR versus the input power.

Table 4.3 Measured performance summary of the 1-bit wideband Delta-Sigma modulator.

Signal Bandwidth (BW)	1.25 MHz
Clock Frequency (Fs)	160 MHz
Oversampling Ratio (OSR)	64
Peak SNDR	66.1 dB
Peak SNR	67 dB
Dynamic Range	68 dB
Supply Voltage	1.2 V
Power Consumption	2.5 mW (A), 0.2 mW(D)
Core Area	0.19mm$_{\times}$0.43mm
Technology	0.13-μm CMOS

Table 4.4 shows the performances of some wideband continuous-time feedforward Delta-Sigma modulators, including this design, where FOM stands for the figure-of-merit, and is defined in Eq. 2.14.

Compared to the other wideband continuous-time feedforward Delta-Sigma modulators, the proposed Delta-Sigma modulator achieves the lowest power (2.7 mW) and the smallest area (0.082 mm^2), while maintaining a good FOM.

Table 4.4 Comparison with other wideband feedforward continuous-time Delta-Sigma modulators.

Ref	BW/Fs (MHz)	SNDR (dB)	Power (mW)	Supply (V)	Tech. (μm)	FOM (pJ/conv.)	Area (mm^2)
[Gia03]	15/300	61	65	1.5	0.13	2.36	-
[Pat04]	15/300	63.7	70	1.5	0.13	1.87	-
[Yan04]	1.1/35.2	83	62	3.3	0.5	2.44	5.76
[Li07]	2.5/60	80.5	50	2.5	0.25	1.16	2.73
[Son08]	2/150	63.4	2.7	1.5	0.25	0.56	0.42
[Dör05]	2/104	71	3	1.5	0.13	0.25	0.3
This work	1.25/160	66.1	2.7	1.2	0.13	0.65	0.082

4.6 Conclusion

This chapter presents a wideband 4^{th}-order single-bit continuous-time Delta-Sigma modulator. To reduce the power consumption of the modulator, several low-power design strategies are utilized on the system level and the circuit level. The input-feedforward topology is adopted due to its attractive potential for the low-voltage low-power design. Zero optimization technique is used to further reduce the in-band noise. A novel structure, in which the feedforward and summing part is embedded in the quantizer, is proposed to save the power consumption and the chip area, and to simplify the circuit design. Small integration capacitances are chosen for the low power consumption. Resistance tuning is used to solve the time-constant variations. Clocked at 160 MHz, the Delta-Sigma modulator achieves 68-dB dynamic range with 2.7-mW power consumption under 1.2-V supply voltage. The core area of the modulator is 0.082 mm^2. The

measured results verify that the proposed continuous-time Delta-Sigma structure is effective to reduce the power consumption with a small silicon area.

CHAPTER 5

LOW-VOLTAGE LOW-POWER CONTINUOUS-TIME DELTA-SIGMA MODULATORS FOR AUDIO APPLICATIONS

5.1 Introduction

Chapter 4 represents the low-voltage low-power Delta-Sigma modulator for wide-band applications. This chapter will focus on low-power solutions for audio Delta-Sigma modulators. The supply voltages will be further reduced to 1 V and 0.6 V. The organization is as follow: Section 5.2 presents a 1-V 1.5-bit continuous-time Delta-Sigma modulator. A 0.6-V single-bit continuous-time Delta-Sigma modulator for audio applications will be described in Section 5.3. Section 5.4 concludes this chapter.

5.2 A 1-V 42.6-μW 1.5-bit Continuous-Time Audio Delta-Sigma Modulator

5.2.1 Introduction

In this section, a 1-V fourth-order continuous-time Delta-Sigma modulator with 1.5-bit quantizer is presented. This design is targeted for audio applications that demand high resolution, low supply voltage, and low power consumption.

As discussed in Section 2.4, analog designers face many challenges in low-voltage low-power designs. Some audio Delta-Sigma modulators, which are operating at 1V or even lower, have been reported recently [Yao04] [Ahn05] [Pun07] [Kim08] [Roh08] [Par09] [Mic11]. Among these designs, the switched-capacitor based discrete-time loop filter is popular [Yao04] [Ahn05] [Kim08] [Roh08] [Par09] [Mic11], mainly due to its good accuracy and good linearity [Sch05]. Compared to DT Delta-Sigma modulators, CT Delta-Sigma modulators tend to consume less power mainly due to two reasons. First, CT loop filters relax settling requirements on amplifiers. Second, CT loop filters eliminate switches and their boost circuits. Although CT Delta-Sigma modulators suffer from some nonidealities, low-speed operation (e.g. in audio applications) relieves the impacts of the clock-related nonidealities, such as the clock jitter, and the excess loop delay. Therefore, the continuous-time audio Delta-Sigma modulator shows an attractive potential for the low-power design.

The objective of this section is to explore low-power solutions for low-voltage continuous-time Delta-Sigma modulators. To lower down the power consumption, techniques on system-level and circuit-level are utilized. The input-feedforward topology, with the optimized coefficients, is utilized to reduce internal signal swings as well as the power consumption. A three-level quantizer with simple dynamic element matching (DEM) is used to improve resolution and stability. A novel feedforward and summation structure is applied in the 1.5-bit modulator to reduce the power consumption and the chip area, and to simplify the circuit.

A 1-V 20-kHz 1.5-bit 100.9-dB continuous-time Delta-Sigma modulator is presented. The modulator, designed in a 0.13-μm CMOS technology, achieves 100.5-dB peak SQNR (Signal-to-Quantization Noise Ratio), and 97.5-dB peak SQNDR (Signal-to-Quantization Noise-and-Distortion Ratio) over a 20-kHz signal bandwidth with a 2.56-MHz clock. The power consumption of the modulator is 42.6 μW under a 1-V supply, and the chip core area is 0.125 mm^2.

The rest of the section is organized as follows. Section 5.2.2 presents the system-level design, including the coefficients optimization, and the considerations to the impacts of nonidealities on this CT Delta-Sigma modulator. Section 5.2.3 addresses the circuit design issues, including the designs of the loop filter, the quantizer and the DAC circuit. A novel feedforward and summing part for the 1.5-bit CT Delta-Sigma modulator will be presented to save power and area, and to simplify the circuit. The post-simulation results are provided in Section 5.2.4. Section 5.2.5 concludes the design.

5.2.2 System-Level Design

A. *Optimized Coefficients for the 1.5-bit Single-loop Input-Feedforward Topology*

Fig. 5.1 shows the 4th-order 1.5-bit continuous-time Delta-Sigma modulator with single-loop input-feedforward topology. The input-feedforward topology is adopted since it is suitable for low-supply and low-power applications, which has been discussed in Chapter 4.

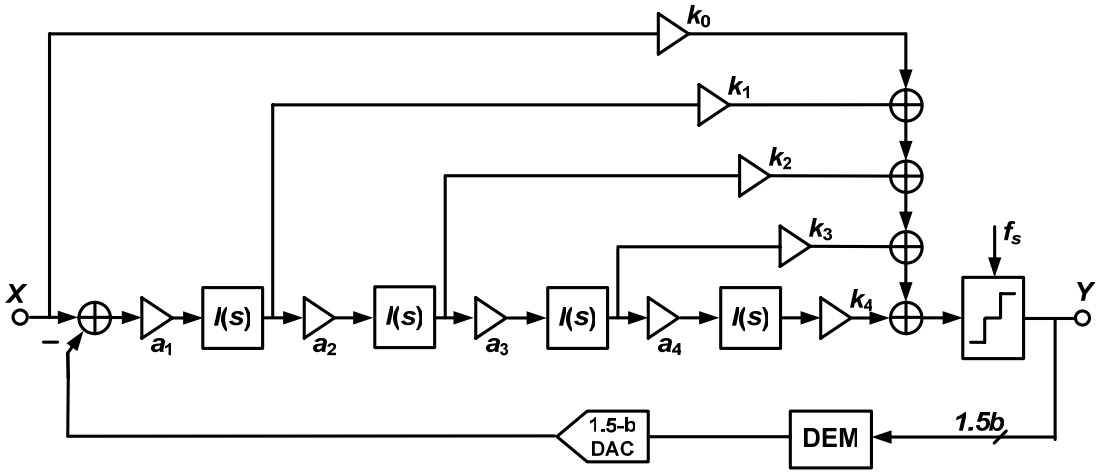


Figure 5.1: Structure of the 4th-order 1.5-bit continuous-time Delta-Sigma modulator with single-loop input-feedforward topology.

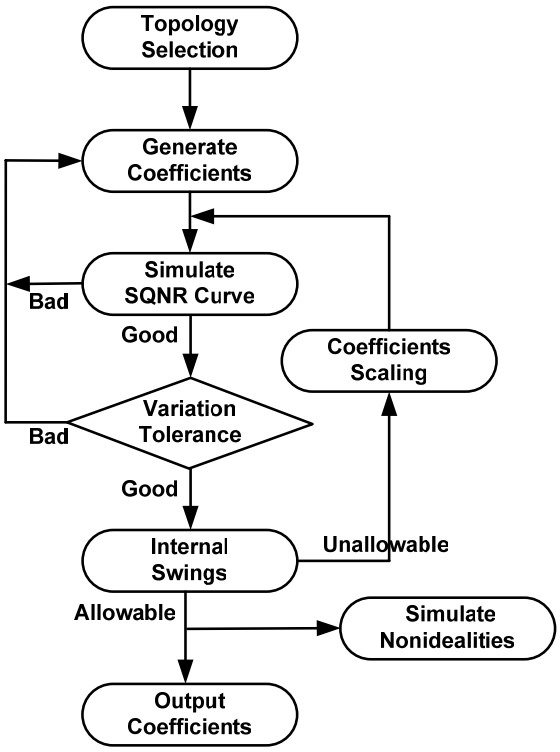


Figure 5.2: Flow chart of the system-level designs and simulations.

The coefficients of the topology are optimized by behavioral simulations. A topology with good loop coefficients should satisfy following requirements. 1) It has a good SQNR. 2) It shows a good stability. In other words, it has high overload level, and it provides good tolerance to time-constant variations. 3) Its internal swings should be scaled within an allowable range for the circuit implementation. The simplified flow chart for the system-level designs and simulations is shown in Fig. 5.2. As shown in Fig. 5.2, after the topology is selected, Matlab codes were written to carry out a number of behavioral simulations with different combinations of coefficients *a* and *c* (see Fig. 5.1). One advantage of the input-feedforward topology is that, its STF is always unity [Sil01], independent to its loop coefficients. Based on the three requirements, one set of optimized coefficients were selected, which are shown in Table 5.1. With those coefficients, the modulator can achieve a peak SQNR of 105.6 dB, and an overload level of −1.8 dBFS. The

internal swings at peak SQNR are shown in Fig. 5.3. For a 1-V supply voltage, such internal swings are less than the output range of the two-stage Miller compensation amplifiers used in this design, which will be discussed in Section 5.2.3.

Table 5.1 Loop coefficients for the 4th-order 1.5-bit continuous-time audio Delta-Sigma Modulator with the input-feedforward topology.

a_1	0.52	k_1	1
a_2	0.35	k_2	1.5
a_3	0.33	k_3	0.75
a_4	0.21	k_4	1
k_0	1		

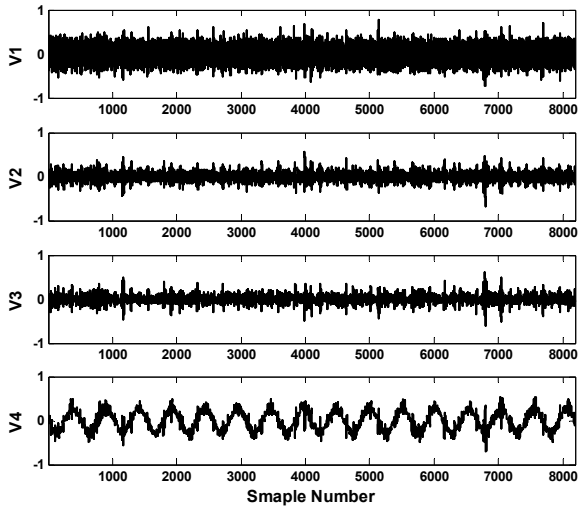


Figure 5.3: Simulated internal swings of the 4th-order 1.5-bit Delta-Sigma modulators. Vi is the i-th integrator output.

B. *Three-Level Quantizer*

The three-level quantizer is utilized in this design, considering that it behaves like a multi-bit quantizer but without complex correction circuits. Over the single-bit quantizer, the 1.5-bit quantizer shows many advantages. First, by increasing the quantization levels, the quantization

noise is reduced in the 1.5-bit quantizer. Second, due to the smaller quantization error, the 1.5-bit Delta-Sigma modulator tends to be more stable. The more stable modulator allows more aggressive NTF, which results in further reduction of in-band quantization noise. Simulations show that the peak SQNR of the three-level Delta-Sigma modulator is 10 dB higher than that of the single-bit modulator counterpart [Yao05]. Third, the three-level modulator is less sensitive to the clock jitter effect due to the smaller quantization step.

C. *Considerations to the Nonidealities in the CT Delta-Sigma Modulator*

Note that DAC signals are fed back to inputs, their nonidealities are not shaped by the loop filter. In other words, the nonidealities in the feedback loop degrade the performance of the modulator directly. Like what have been done in Chapter 4, the clock jitter effect, and the excess loop delay effect are simulated here.

The clock jitter's impact on the SNR of the 4^{th}-order 1.5-bit input-feedforward Delta-Sigma modulator is shown in Fig. 5.4, where the timing error is represented as the percentage of the clock period T_s. To suppress the impact of the clock jitter effect, NRZ pulse is chosen as the shape of DAC in this design, because it is less sensitive to the clock jitter effect when compared to RZ and HRZ counterparts [Che99-a]. According to the simulation results, the clock jitter should be less than 66 ps to achieve a peak SNR higher than 90 dB.

The effect of the excess loop delay is simulated, and the SNR curve versus the delay is shown in Fig. 5.5, where the input amplitude is −3-dBFS, and the delay is represented as the percentage of the clock period T_s. Thanks to the optimized coefficients used, the modulator can tolerate a delay up to 18% of the clock period, which is 70.3125 ns for this design. Since much smaller delay can be achieved with the 0.13-μm CMOS technology used, there is no necessity for additional compensation techniques.

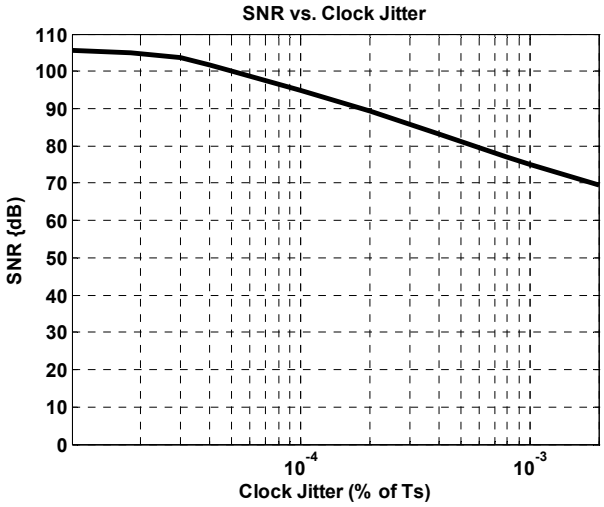


Figure 5.4: Impact of the clock jitter on the SNR of the 4th-order 1.5-bit input-feedforward Delta-Sigma modulator with NRZ DAC pulse, for the −3-dBFS input.

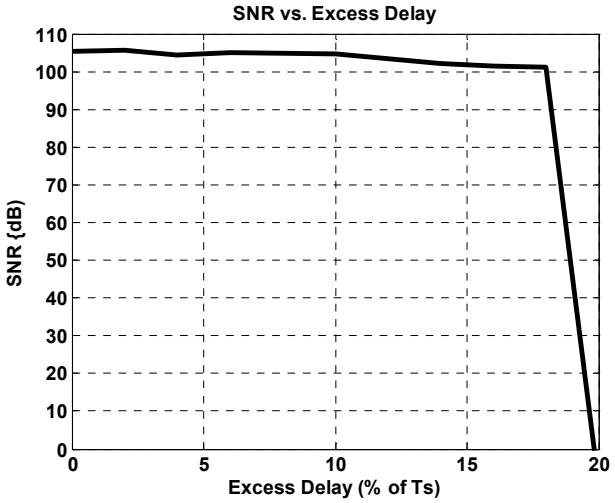


Figure 5.5: Impact of the excess delay on the SNR of the 4th-order 1.5-bit input-feedforward Delta-Sigma modulator with NRZ DAC pulse, fot the −3-dBFS input.

5.2.3 Circuit Implementation

Fig. 5.6 shows the circuit blocks of the fourth-order 1.5-bit CT Delta-Sigma modulator. The circuit implementation includes building blocks like the loop filter, the quantizer and the DAC

feedback circuit. The organization of this section is as follows. In Section A, the integrator design will be presented. The proposed feedforward and summing part, together with the quantizer design, will be discussed in Section B. Since the quantizer is more than 1-bit, the DAC is no longer inherently linear. Therefore, the linearity issue will be addressed in Section C. Finally, the tuning circuit, which is used to compensate the variation of the time constants, will be described.

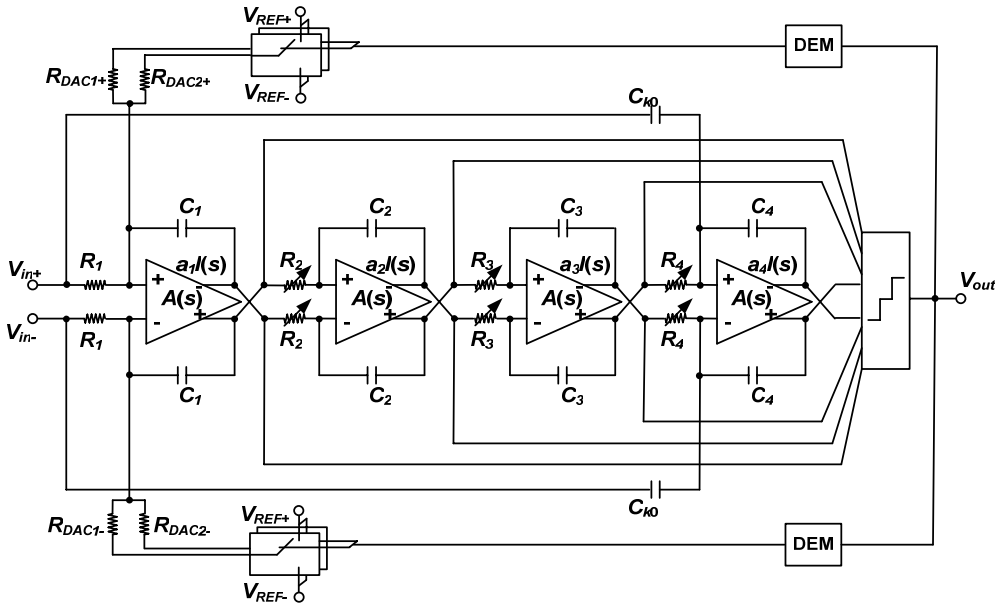


Figure 5.6: Circuit blocks of the 1.5-bit 4th-order input-feedforward Delta-Sigma modulator.

A. *Integrator Design*

All the integrators are implemented with active-RC filters due to their good linearity and parasitic insensitivity. Furthermore, the active-RC filter is very suitable for low-voltage operations, because its virtual ground relaxes the constraint of amplifier's input range. Coefficients a_i (i = 1−4, see Table 5.1) are realized by products of integration resistances and capacitances.

The performance of the modulator is mainly determined by the first integrator, whose nonidealities are not suppressed by the loop filter. The maximum value of the integration resistance R_1 is limited

by the dynamic range requirement. In this design, R_1=180 kΩ, giving thermal noise lower than 93 dB below the full scale input signal.

Low supply voltage restricts the choice of circuit topologies due to the limited voltage headroom. As shown in Fig. 5.7, the fully-differential two-stage Miller compensation amplifier is utilized for the integrator in this design. Compared to the single-stage amplifiers, such as telescopic amplifier or folded-telescopic amplifier, the two-stage amplifier is more suitable for low-voltage circuits due to its comparable dc gain but larger output swing. Fully-differential technique is applied to increase signal swings, and to suppress even-order harmonics and common-mode noise. The common-mode feedback circuit is also shown in Fig. 5.7, which senses the output common-mode and provides the control biasing voltage directly to the first stage. NMOS input transistors are sized with large dimension to lower down the flicker noise. The total supply current of the 1st integrator is 19.6 μA, which ensures enough low thermal noise. Simulations show that the total in-band noise from the amplifier is 72.25 pV^2, about 101 dB lower than the full scale input power. Such a supply current also ensures good linearity and slew rate performances, which can be proven by the post-layout simulation results in Section 5.2.4. Simulated performances of the 1st op amp are shown in Table 5.2.

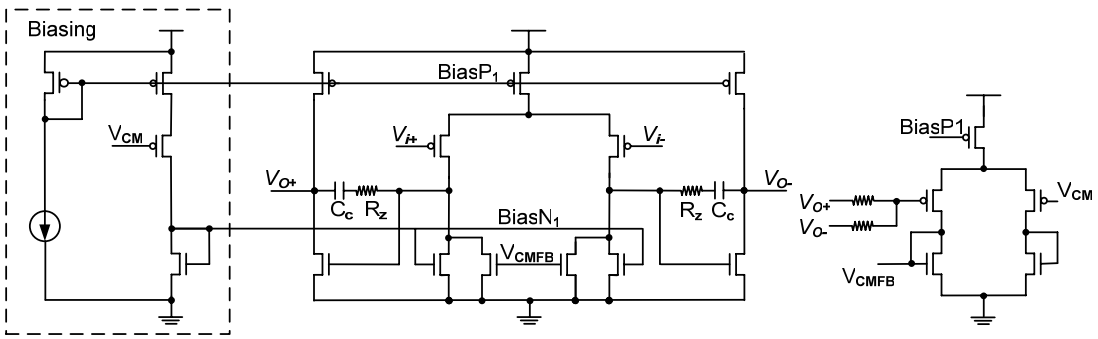


Figure 5.7: Two-stage miller compensation amplifier, with its biasing circuit, and its CMFB circuit.

Table 5.2 Simulated performances of the 1st amplifier in the 1.5-bit audio Delta-Sigma modulator.

Parameter	Amplifier
GBW (MHz)	8
dc gain (dB)	56
Phase Margin (degree)	32.1
In-band noise (μV/dB)	8.5
Load (pF)	4.18
Static Current (μA)	19.6

The 2nd to 4th integrators share the same op amp structure with the 1st integrator. Thanks to the noise-shaping effect, op amps in these integrators have much more relaxed requirements with respect to noise, linearity, and slew rate. The total supply current of 16.3 μA is sufficient to meet the relaxed requirements on noise and linearity for the three integrators.

B. *Proposed 1.5-bit Feedforward Path, Summing Block, and Comparator*

In traditional Continuous-time Delta-Sigma modulators, feedforward paths are implemented with transconductors, and the signals are fed forward and summed in current [Zwa96] [Bre00]. Additional transconductors increase the power consumption, the area, and the circuit complexity. In [Sch04], the feedforward paths were implemented by capacitors. Although this structure simplifies the modulator by eliminating feedforward transconductors, it adds additional loads to the 1st to 3rd integrators, which consume more current, and increase the chip area. In Chapter 4, a structure was proposed, in which the feedforward and summation part is embedded in the quantizer. By eliminating additional feedforward transconductors and feedforward capacitors, this structure is proved to be power and area efficient [Zha09]. The structure in Chapter 4 is proposed for the single-bit modulator, in this design, this structure is extended for the 1.5-bit modulator.

For the 1.5-bit quantizer, its transfer curve is shown in Fig. 5.8, where the y axis is the digital output D_1D_0, and x axis is the ratio of the quantizer input V_{Qin} to the reference voltage V_{REF}, which

is 1 V for this design. According to Fig. 5.1, the quantizer input is the sum of the feedforward signals, which can be expressed as:

$$V_{Qin} = k_0 \cdot V_{in} + \sum_{i=1}^{4} k_i \cdot V_{Oi} \,, \tag{5.1}$$

where V_{in} is the input signal, and $V_{Oi} = V_{Oi+} - V_{Oi-}$, is the i-th (i= 1−4) integrator's output signal. The digital output D_1D_0 is a two-bit signal, whose Most-Significant-Bit (MSB) D_1 turns to 1 when $V_{Qin} > +V_{REF}/3$, and whose Least-Significant-Bit (LSB) D_0 turns to 1 when $V_{Qin} > -V_{REF}/3$. Fig. 5.9 shows the quantizer circuit blocks, which consist of two comparators and two D latches. As shown in Fig. 5.9, the MSB is generated by the comparator with the name Com1, and the LSB is generated by the comparator with the name Com0. Comparators inputs comprise integrator outputs ($V_{O\pm}$[1:4]), and two fractions ($V_{R\pm}$) of the reference voltage.

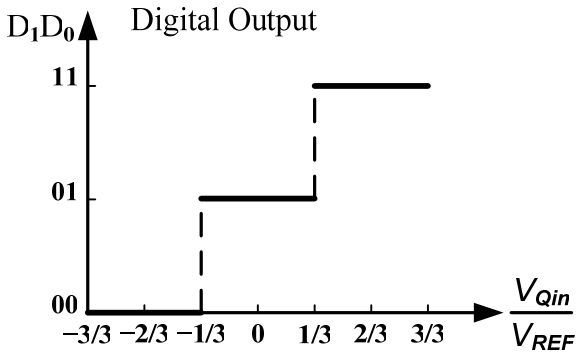


Figure 5.8: Transfer curve of the 1.5-bit quantizer.

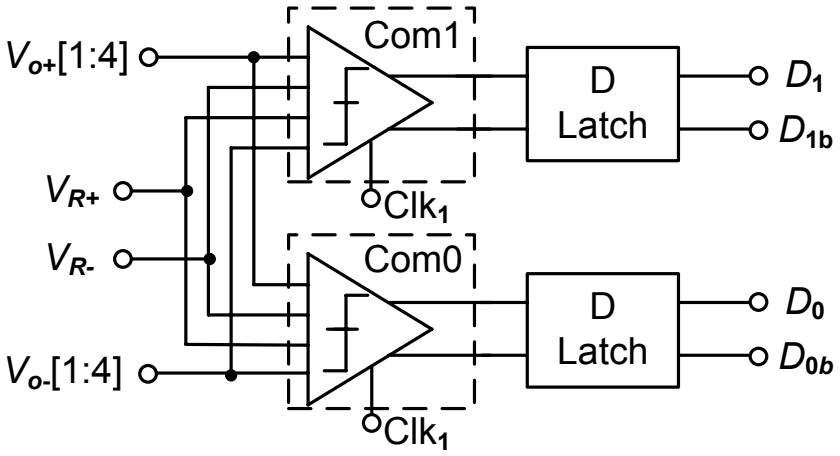


Figure 5.9: Circuit blocks of the 1.5-bit comparator.

Fig. 5.10(a) shows the schematic of the comparator Com1, which is used to generate the MSB D_1. The same conditions, which have been described in Chapter 4, are required to be satisfied before the comparator is able to work well as the feedforward and the summing part. With the help of Fig. 5.10(a), the operation of the comparator Com1 can be explained. When Clk_1 is at GND, the comparator is reset. Its outputs are driven to VDD and nodes X_1 and Y_1 (see Fig. 5.10(a)) are pulled down to GND. When Clk_1 turns to VDD, the comparator is activated. Due to the small internal swings in the input-feedforward topology, the comparator inputs are higher than the transistor threshold voltage, and transistors M1-M5 are working under liner region. The current at X_1 and Y_1 can be derived:

$$I_{X1} = \sum_{i=1}^{5} I_{iA} = \mu_n C_{ox} \cdot [\sum_{i=1}^{4} \frac{W_i}{L} \cdot (V_{Oi+} - V_{THN} - \frac{V_X}{2}) \cdot V_X + \frac{W_5}{L} \cdot (V_{R-} - V_{THN} - \frac{V_X}{2}) \cdot V_X],$$

(5.2)

$$I_{Y1} = \sum_{i=1}^{5} I_{iB} = \mu_n C_{ox} \cdot [\sum_{i=1}^{4} \frac{W_i}{L} \cdot (V_{Oi-} - V_{THN} - \frac{V_X}{2}) \cdot V_X + \frac{W_5}{L} \cdot (V_{R+} - V_{THN} - \frac{V_X}{2}) \cdot V_X],$$

(5.3)

where L is the channel length, W_i representing the channel width of the transistor Mi, and V_{THN} is the threshold voltage of transistors M1-M5. Assuming $V_X = V_Y \approx 0$V, Eq. 5.2 and Eq. 5.3 can be translated into:

$$I_{X1} - I_{Y1} = \frac{\mu_n C_{ox} V_X}{L} \cdot (\sum_{i=1}^{4} W_i \cdot V_{Oi} - W_5 \cdot V_R), \tag{5.4}$$

where $V_R = V_{R+} - V_{R-} = V_{REF}/3$, representing the threshold reference (see Fig. 5.13) for the digitizing. Based on Eq. 5.1 and Eq. 5.4, the feedforward coefficient k_i can be implemented by the ratios between the channel widths by the following equation:

$$k_1 : k_2 : k_3 : k_4 : 1 = W_1 : W_2 : W_3 : W_4 : W_5 . \tag{5.5}$$

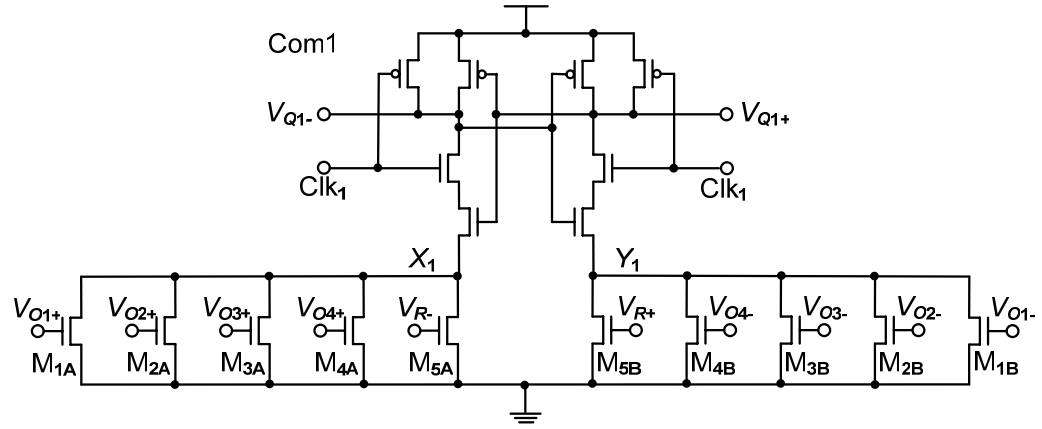
Because the large input signal may lead the transistor out of linear region, and may cause problem, its feedforward coefficient k_0 is implemented by the ratio of C_{k0}/ C_4 (see Fig. 5.6).

According to Eq. 5.4 and Eq. 5.5, if the sum of the feedforward signals is larger than V_R, the comparator will generate the high logic signal. Otherwise, the comparator will generate the low logic signal.

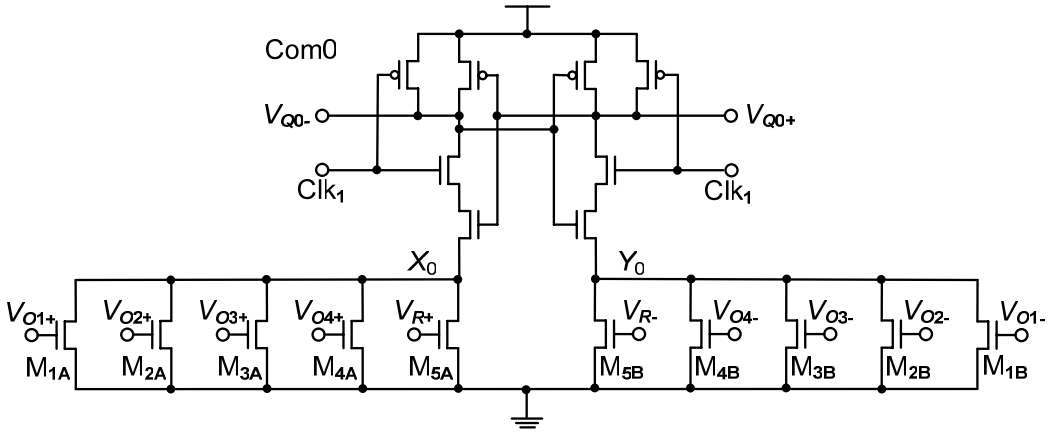
The comparator Com0, which generates the LSB D_0, is exactly the same as Com1, except that the connections for V_{R+} and V_{R-} are exchanged (see Fig. 5.10(b)). The similar operation can be derived for the comparator Com0:

$$I_{X0} - I_{Y0} = \frac{\mu_n C_{ox} V_X}{L} \cdot (\sum_{i=1}^{4} W_i \cdot V_{Oi} + W_5 \cdot V_R), \tag{5.6}$$

The comparator generates the high logic signal if the sum of the feedforward signals is larger than $-V_R$, and generates the low logic signal for the otherwise case.



(a)



(b)

Figure 5.10: Multi-input comparators for the MSB signal (a), and for the LSB signal (b).

Because the capacitance values of the transistors can be limited to small values (less than 100 fF for each comparator in this design), only very few power is needed for the feedforward paths. Similarly, the area for the feedforward path is also very small. Therefore, by embedding the feedforward and summation part into the comparator, the modulator tends to be power and area efficient.

C. *DAC Design*

As shown in Fig. 5.6, the DAC circuit comprises switches, resistors, and DEM circuit. For the 1.5-bit DAC, there are two 1-bit DAC paths in each feedback branch. Since the quantization levels are more than two, the DEM circuit is required to improve the modulator's linearity.

The DAC linearity depends on the matching of the switches and resistors in the feedback path. For the simplicity, the switches are assumed ideal, i.e., their on-resistances are assumed zero, and their off-resistance are assumed infinite. For the 1.5-bit quantizer, the simplified DAC circuit diagram is shown in Fig. 5.11. There are three cases based on different values of the digital output D_1D_0. Ideally, all DAC resistors are matched, and $V_{REF+} = -V_{REF-} = V_{REF}/2$. When $D_1D_0 = 00$ (Case 1), the feedback current is $2V_{REF}/R_{DAC}$, where R_{DAC} is the DAC resistance. When $D_1D_0 = 01$ (Case 2), the feedback current is zero, and when $D_1D_0 = 11$ (Case 3), the feedback current is $-2V_{REF}/R_{DAC}$. In this way, the DAC signal is linear.

The situation is different, when there are mismatches in the DAC resistors. For example, assuming $R_{DAC1+} = (1+\Delta_1)\cdot R_{DAC}$, $R_{DAC2+} = (1+\Delta_2)\cdot R_{DAC}$, $R_{DAC1-} = (1+\Delta_3)\cdot R_{DAC}$, and $R_{DAC2-} = (1+\Delta_4)\cdot R_{DAC}$, the feedback currents are changed. For Case 1, the feedback current is derived as:

$$I_1 = I_0 \cdot (1 + \Delta_x), \tag{5.7}$$

where $I_0 = 2V_{REF}/R_{DAC}$, and Δ_x is a $\Delta_{1\text{-}4}$ related parameter. For Case 2, the feedback current is derived as:

$$I_2 = \frac{V_{REF}}{2R_{DAC}} \cdot \left(\frac{1}{1+\Delta_1} - \frac{1}{1+\Delta_2}\right) - \frac{V_{REF}}{2R_{DAC}} \cdot \left(\frac{1}{1+\Delta_3} - \frac{1}{1+\Delta_4}\right). \tag{5.8}$$

And for Case 3, the feedback current is derived as:

$$I_3 = -I_0 \cdot (1 + \Delta_x). \tag{5.9}$$

According to Eq. 5.7, Eq. 5.8, and Eq. 5.9, the DAC circuit is not linear due to the mismatch between R_{DAC1+} and R_{DAC2+}, and the mismatch between R_{DAC1-} and R_{DAC2-}.

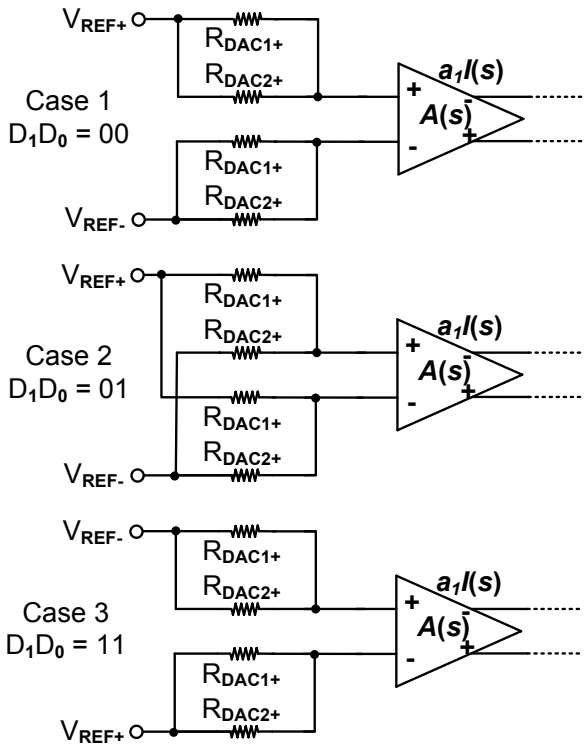


Figure 5.11: Different cases in the 1.5-bit DAC circuit.

A simple Dynamic Element Matching (DEM) circuit is thus applied to eliminate the mismatch impact, which is shown in Fig. 5.12. The principle operation of this DEM circuit is similar to what is described in [Kim08], that is, to toggle the two switches in each branch when $D_1D_0 = 01$. The DEM circuit is shown in Fig. 5.13(a). There is a T flip-flop in the DEM, generating the toggle signal for the switch-controlling signals SW_1 and SW_2. Fig. 5.13(b) shows the simulated waves. Table 5.3 gives the truth table for the DEM circuit.

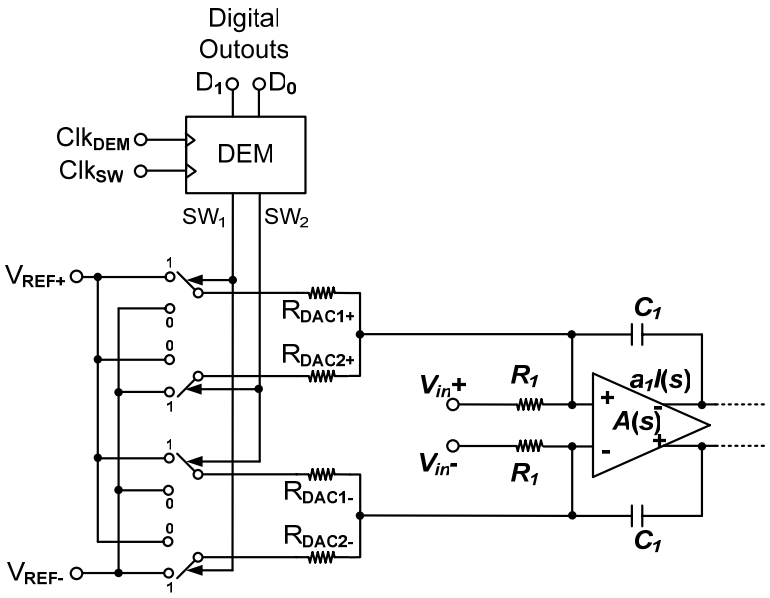
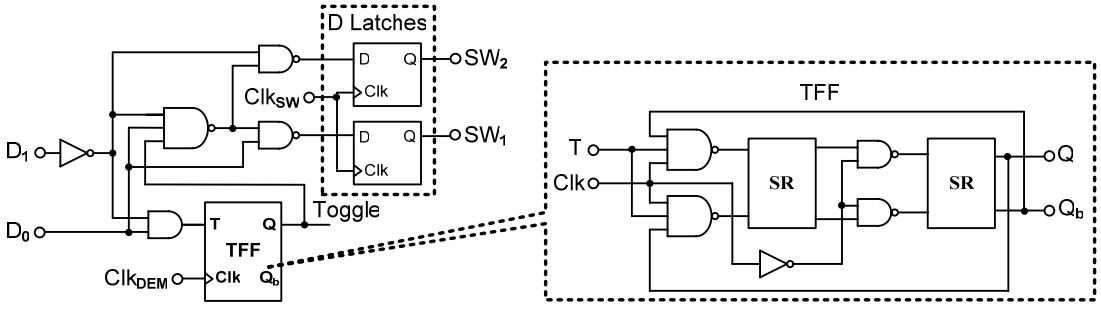
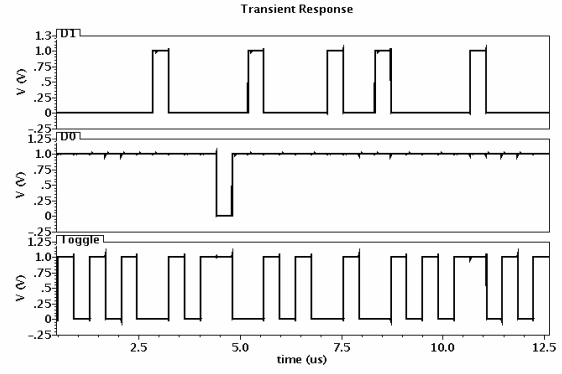


Figure 5.12: 1.5-bit DAC circuit including the DEM block.



(a)



(b)

Figure 5.13: The DEM circuit (a), and the simulated waves of the T flip-flop (b).

Table 5.3 Truth table for the DEM circuit.

D_1	D_0	Toggle	SW_1	SW_2
0	0	X	1	0
0	1	1	1	1
0	1	0	0	0
1	1	X	0	1

D. RC Time Constant Tuning

To prevent the performance degradation caused by the time constant shift, tunable integration resistors are provided. Similar to what is presented in Chapter 4, Each tunable resistor is controlled by a four-bit digital signals $D_{Tune}[3:0]$, and only R_2, R_3, and R_4 (see Fig. 5.6) are tuned. Fig. 5.14 shows the two worst cases for the time constant variation. In the figure, the y axis is the value of the SNR for the −3dBFS input, and the x axis is the percentage variations of the 2nd to the 4th integrator's time-constants a_2-a_4, which are assumed to vary by the same percentage. The solid line represents the case when a_1 varies +30%, and the dashed line represents the case when a_1 varies -30%. According to Fig. 5.14, the tunable resistance values are chosen to keep the variations of a_2-a_4 within ±10%, and therefore, the modulator is kept stable.

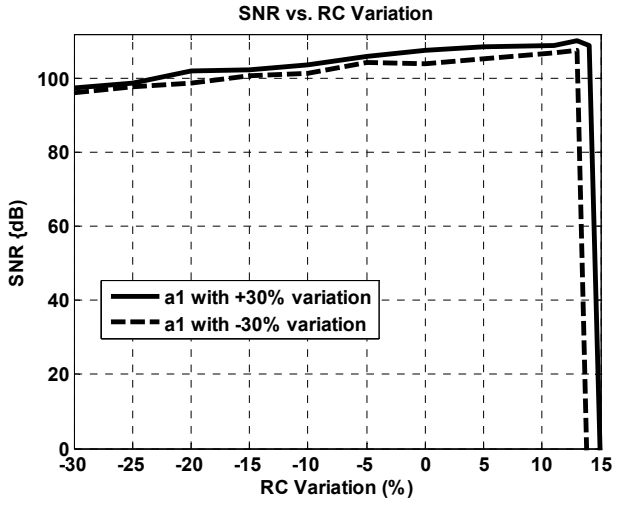


Figure 5.14: SNR versus time-constant variations in the 2nd-4th integrators. The input signal amplitude is −3 dBFS.

5.2.4 Post-Layout Simulation Results

The modulator was designed with a standard 0.13-μm CMOS process. Fig. 5.15 shows the chip layout. Due to the novel structure for the feedforward and summation part, the core area of the modulator is 0.125 mm^2.

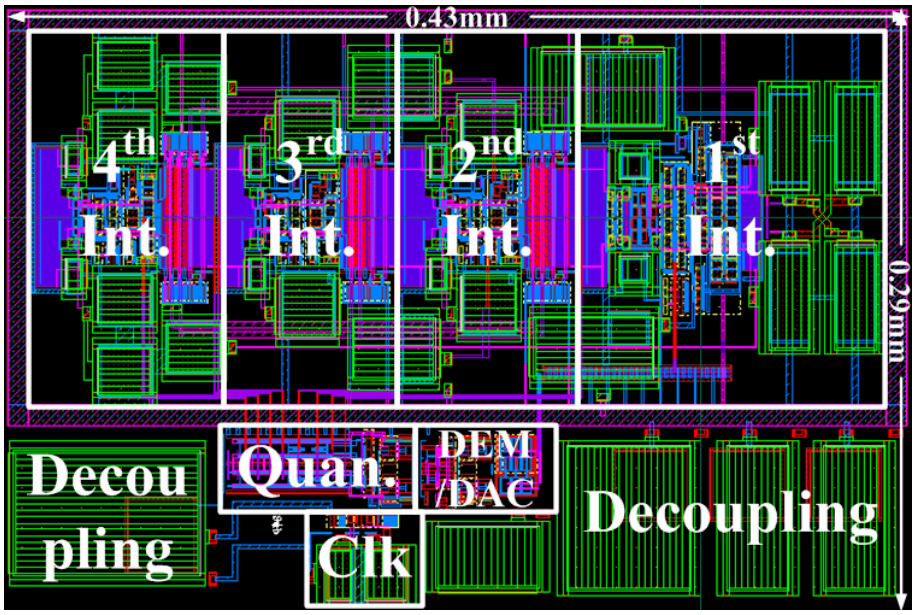


Figure 5.15: Layout of the 1.5-bit continuous-time audio Delta-Sigma modulator.

The chip, with post-layout RC extraction, has been simulated for various sinusoidal inputs. The data were captured in the workstation, transferred to a PC, and then processed with Matlab codes. Fig. 5.16 and Fig. 5.17 show the simulated output spectrum without DEM and with DEM, respectively. The input is a −3 dBFS 5-kHz sinusoid signal, and a 1% mismatch is added in DAC resistors. The post-layout simulation results verify that the DEM improve the linearity.

SQNR and SQNDR curves versus the input power are shown in Fig. 5.18. Simulated results show that the modulator achieves a peak SQNDR of 97.3 dB, a peak SNR of 100.5 dB, and a dynamic

range of 100.9 dB. Thanks to the novel feedforward structure and the 1.5-bit quantizer used, power consumptions for the analog circuit and digital circuit are 38.8 μW and 3.8 μW, respectively. The simulated performances are summarized in Table 5.4. Table 5.5 shows the performance comparison with other low-voltage audio Delta-Sigma modulators. Compared to other audio Delta-Sigma modulators, this design shows good power and area performances

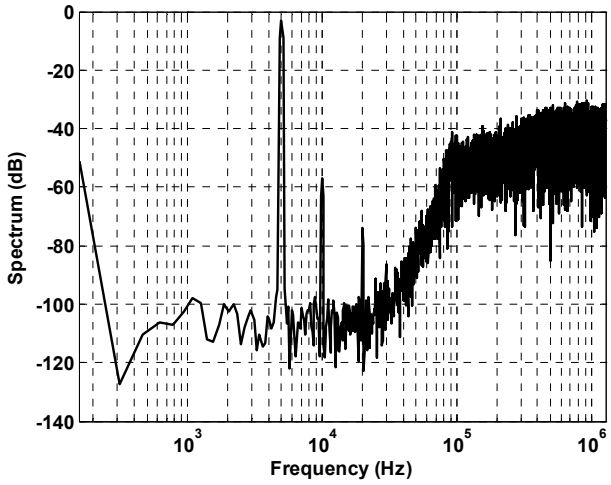


Figure 5.16: Simulated output spectrum without DEM for the −3-dBFS 5-kHz input signal, the DAC resistance mismatch is 1%, FFT bins are 65536.

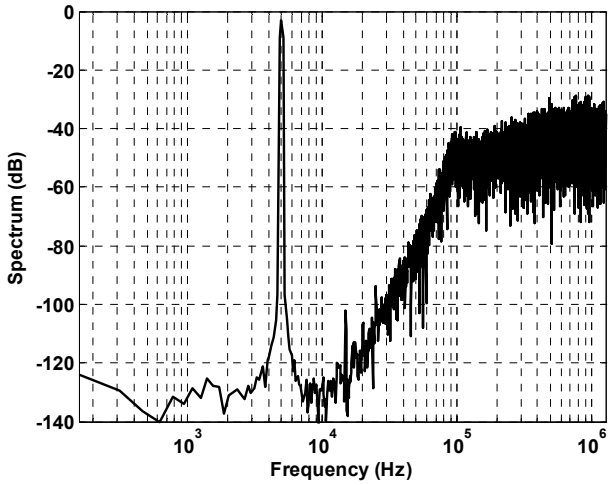


Figure 5.17: Simulated output spectrum with DEM for the −3-dBFS 5-kHz input signal, the DAC resistance mismatch is 1%, FFT bins are 65536.

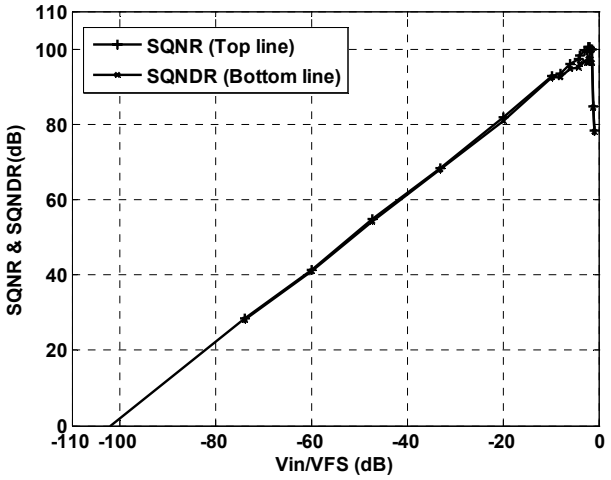


Figure 5.18: SQNR/SQNDR versus the input power.

Table 5.4 Simulated performance summary of the 1.5-bit audio Delta-Sigma modulator.

Signal Bandwidth (BW)	20 kHz
Clock Frequency (Fs)	2.56 MHz
Oversampling Ratio (OSR)	64
Peak SQNDR	97.3 dB
Peak SQNR	100.5 dB
Dynamic Range	100.9 dB
Supply Voltage	1 V
Power Consumption	38.8 μW (A), 3.8 μW(D)
Core Area	0.43mm×0.29mm
Technology	0.13-μm CMOS

Table 5.5 Comparison with other low-voltage audio Delta-Sigma modulators.

Ref	Type	BW (kHz)	SNDR (dB)	Power (μW)	Supply (V)	Tech. (μm)	Area (mm^2)
[Yao04]	DT	20	81	140	1	0.09	0.18
[Pel98]	DT	16	62	40	0.9	0.5	0.85
[Ahn05]	DT	24	81	1000	0.6	0.35	2.88
[Pun07]	CT	25	74	300	0.5	0.18	0.6
[Kim08]	DT	24	89	1500	0.9	0.13	1.44
[Roh08]	DT	20	73.1	60	0.9	0.13	0.42
[Cha08]	DT	20	81	36	0.7	0.18	0.72
[Par09]	DT	25	95	870	0.7	0.18	2.16
This Work*	CT	20	97.3**	42.6	1	0.13	0.13

* Simulated results. **With quantization noise only.

5.2.5 Conclusion

Section 5.2 presents a 4^{th}-order 1.5-bit continuous-time Delta-Sigma modulator for low-power audio applications. To reduce the power consumption, several low-power design strategies are utilized on the system level and the circuit level. The input-feedforward topology is adopted due to its attractive potential for the low-voltage and low-power design. The coefficients are optimized to achieve a good SQNR and to maintain a good stability. A novel structure, in which the feedforawrd and summation part is embedded in the quantizer, is proposed for the 1.5-bit quantizer to save the power consumption and the chip area, and to simplify the circuit design. A simple DEM circuit is used to improve linearity. Operating under 1-V supply, this design achieves 100.9-dB dynamic range with a power consumption of 42.6 μW. The chip area is 0.125 mm^2. The simulated results verified that the proposed continuous-time Delta-Sigma structure is effective to reduce the power consumption with a small area.

5.3 A 0.6-V 28.6-µW 82-dB Continuous-Time Audio Delta-Sigma Modulator

5.3.1 Introduction

In this section, a sub-1 V single-bit fourth-order continuous-time Delta-Sigma modulator will be presented. This design is targeted for audio applications that demand high resolution, ultra low supply voltage, and ultra low power consumption.

Sub-1 V audio Delta-Sigma modulators are gaining popularity recently. Several modulator designs have been reported recently [Pel98] [Sau02] [Ahn05] [Goe06] [Kim08] [Roh08] [Par09] [Cha08] [Mic11] [Pun07]. Among these designs, the switched-capacitor based DT loop filters [Pel98] [Sau02] [Ahn05] [Goe06] [Kim08] [Roh08] [Par09] [Cha08] [Mic11] seem to be preferred choices compared to their CT counterparts. The DT modulator is attractive because it exhibits good accuracy and good linearity [Sch05]. In this section, we will show that it is possible for a CT modulator to achieve the best FOM in audio frequency range by carefully selecting modulator architecture and exploring circuit level innovation. We demonstrate our techniques through the design of a 0.6-V single-bit CT Delta-Sigma modulator. The modulator, implemented in 0.13µm standard CMOS process, and the dynamic range is targeted at more than 80 dB.

The organization of this section is as follows. Section 5.3.2 addresses the architecture-level issues. Section 5.3.3 presents circuit-level designs, including the proposed power-efficient and gain-enhanced amplifier and the rail-to-rail input CMFB circuit. Section 5.3.4 presents layout considerations. Section 5.3.5 presents the setup for the testing. Measurement results are shown in Section 5.3.6. Section 5.3.7 concludes this design.

5.3.2 Modulator Architecture

The system-level issues are discussed in this section. First, the topology of the modulator is carefully selected for the low-power low-voltage design. The effects of the clock related non-idealities are analyzed, and requirements on the amplifier are presented.

As shown in Fig. 5.19, the topology of this design is similar to the topology presented in Chapter 4, except that the local feedback loop is eliminated. The single-bit quantizer is used in the input-feedforward topology. By eliminating the dynamic element matching circuit, the single-bit quantizer tends to consume less digital power and area, and also it helps to simplify the digital design.

The order and the oversampling ratio of the modulator are determined based on the quantization noise requirement. In this design, the thermal noise from the circuit is set as the dominant component in order to reduce the power consumption of the amplifiers, which will be discussed in Section 5.3.3. The non-dominant quantization noise is then set at 10 dB below the circuit noise. For our targeted DR of more than 80 dB, a fourth order topology with an OSR of 64 is selected, which achieves a peak signal-to-quantization noise ratio of 94 dB based on simulation results. The coefficients, which are rounded to two decimals, are also shown in Fig. 5.19. The feedforward coefficients are adjusted to one or two, so that they can be easily embedded into the comparator with multi-finger transistors.

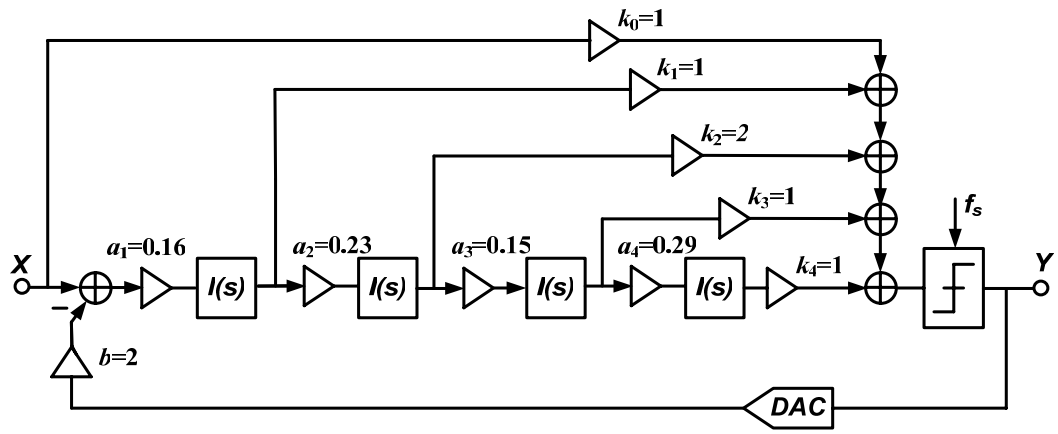
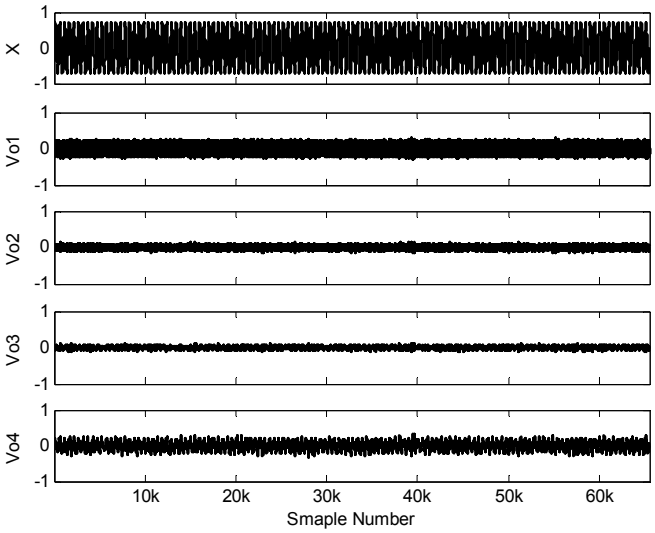
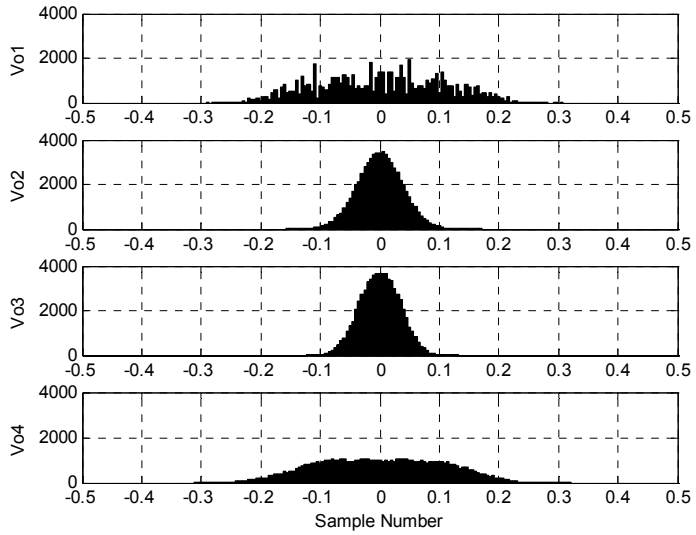


Figure 5.19: Structure of the 4th-order 1-bit continuous-time audio Delta-Sigma modulator.

The internal swing at the output of each integrator is another important factor to the sub-1 V operation. The simulated internal swings for a -3dBFS input signal are shown in Fig. 5.20 (a) and (b), where the full-scale amplitude is normalized to 1 (differential peak-to-peak amplitude is 2), and the references are normalized to ±1. In the simulation, the output of the 4th integrator V_{o4}, contains the input signal X also (see Fig. 5.19), this is because on the circuit-level, the input feedforward coefficient is embedded in the 4th integrator (see section 5.3.3). One thing should be noted is that, since the single-bit quantizer is used, the integrators in the feedforward modulator still contain the suppressed signal component. At the 4th integrator, such component and the feedforward signal cancel each other to some extent, and that is why the 4th integrator output swing is much smaller than the input signal. According to Fig. 5.20 (b), more than 99% of V_{o1} and V_{o4}, and 100% of V_{o2} and V_{o3} are controlled within ±24% of the reference.



(a)



(b)

Figure 5.20: -3dBFS input signal and integrator output waves (a), and integrator output histogram (b), X represents the input signal, V_{oi} (i=1,2,3,4) represents the i-th integrator output, the full-scale amplitude is normalized to 1 (differential peak-to-peak amplitude is 2), and the references are normalized to ±1.

As mentioned in Section 5.2.1, low-speed applications relieve the impacts of the clock-related nonidealities. According to the simulation results, to achieve a SNR higher than 90 dB, the maximum jitter tolerance is about 19 ps, and the delay tolerance is about 59 ns. The low-jitter can be realized with low-jitter clock source and careful design. As to the excess loop delay, thanks to

the 0.13-μm process and the single-bit quantizer used, the practical excess loop delay can be well designed within 59 ns. Hence, no additional compensation technique is required.

5.3.3 Circuit Implementation

In this section, we discuss the details of circuit implementation. The modulator is realized in a 0.13-μm standard CMOS process. Since the sum of the PMOS and NMOS threshold voltages can be designed not larger than 0.4 V, the supply voltage is designed at 0.6 V. Fig. 5.21 shows the circuit blocks of the single-bit fourth-order CT Delta-Sigma modulator. The resistances and capacitances are also shown in the figure. In this design, R_1 = 300 kΩ and R_{DAC} = 150 kΩ, giving a thermal noise around 85-dB lower than the full-scale input signal.

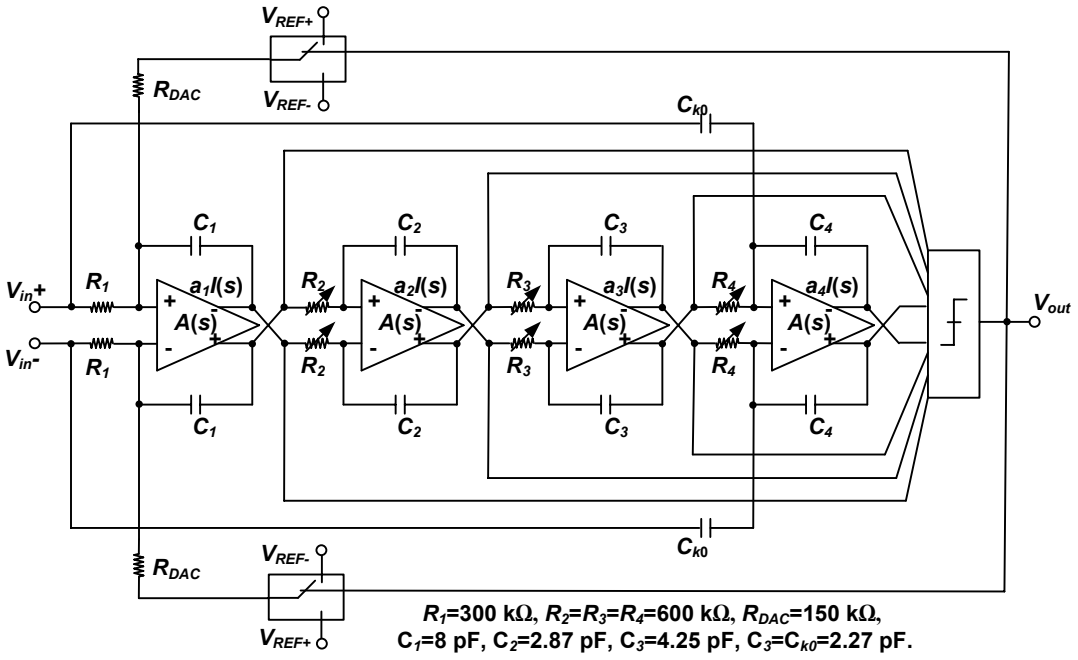


Figure 5.21: Circuit blocks of the 4th-order 1-bit continuous-time audio Delta-Sigma modulator.

A. *Proposed Gain-Enhanced Partially Body-Driven Amplifier*

For low-power low-voltage designs, simple and power-efficient circuits are always preferred [Lan98]. With the simple structure, the amplifier has very few transistors and very small device capacitances, so that it tends to be power and area efficient.

A power-efficient and gain-enhanced fully-differential single-stage amplifier is developed for the modulator. The fully-differential structure provides large output swing, even-order harmonic suppression, and good PSRR/CMRR performance. The single-stage topology eliminates the compensation capacitors, which in turn improves the power-efficiency as there is no need for driving the compensation capacitors [Yao03]. The detailed circuit is shown in Fig. 5.22. The input common-mode voltage V_{A_cm} is set at half V_{DD} and is limited by the drain-source voltage of M_0, V_{DS0}, and the gate-source voltage of M_1, V_{GS1}, i.e.:

$$V_{Ai\_cm} = \frac{V_{DD}}{2} = V_{DS0} + V_{GS1}. \tag{5.10}$$

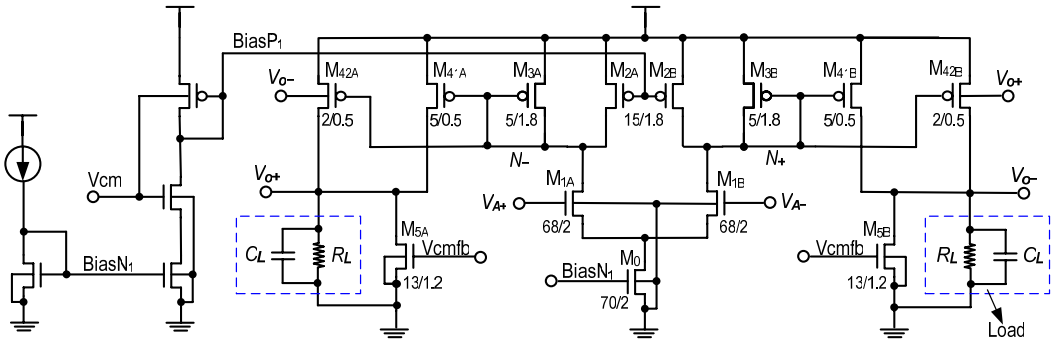


Figure 5.22: Proposed power-efficient gain-enhanced amplifier with body-driven technique (PMOS bodies are connected to the common-mode voltage $V_{cm} = V_{DD}/2$, unless otherwise noted).

M_{1A} and M_{1B} are biased at moderate inversion region to keep V_{GS1} low for low-voltage operation. The threshold voltages of PMOS transistors M_{2A}, M_{2B}, M_{3A}, M_{3B}, M_{41A} and M_{41B} are moderated by connecting their bodies to the common-mode voltage V_{cm}, which is set to 0.3 V as the half of the supply voltage. Although the threshold voltages can be further reduced if the bodies of these

PMOS transistors are connected to the ground, this is not recommended due to much larger leakage current and possible latch-up caused by the supply voltage variation.

The single-stage amplifier does not make use of telescopic or folded-cascoded structure in order to maximize signal swings, but at the cost of limited gain. One way to boost the gain is to place two current sources M_{2A} and M_{2B} in parallel with the diode-connected transistors M_{3A} and M_{3B} [Yao03]. The dc gain at node *N* (see Fig. 5.22) can be expressed as:

$$A_{diff1} = \frac{g_{m1}}{g_{ds1} + g_{ds2} + g_{ds3} + g_{m3}}, \tag{5.11}$$

where g_m represents the transconductance and g_{ds} represents the output conductance. By increasing the size ratio of M_2 to M_3, g_{m3} is reduced, and hence the gain at *N* is increased. However, g_{m3} cannot be chosen too small, because the pole at *N* is non-dominant and it should be kept far away from the amplifier's gain-bandwidth [Yao03]. As shown in Fig. 5.22, the size ratio of transistors M_2 to M_3 is selected as 3, which provides a dc gain around 15.6 dB, and a non-dominant pole 6 times larger than the amplifier's gain-bandwidth.

Note that the first three amplifiers in the active-RC integrators drive integration resistors of the subsequent stages, i.e. R_2 to R_4 in Fig. 5.21. To minimize the dc gain degradation caused by the loading effect, the resistances of R_2 to R_4 should be set much higher than those of the output resistances of the amplifiers, which can be very high in the low-power designs. However, the very high integration resistances should be avoided especially in the second stage, since they may become one of dominant noise sources. In addition, the high integration resistance leads to the large parasitic capacitance, which in turn affects the performance of the amplifier, such as the slew rate and the frequency response. To boost the dc gains without involving large integration resistors, a body-driven gain-enhancement technique is proposed for the modulator. The gain boost circuit involves transistors M_{42A} and M_{42B}, which form a cross-coupled pair at their body terminals as shown in Fig. 5.22. The introduction of M_{42A} and M_{42B} provides a negative resistance at the output node. In this way, the overall output resistance of the amplifier is effectively

increased, leading to an enhanced differential dc gain. The overall dc gain of the proposed single-stage amplifier can be derived as:

$$A_{diff} \approx \frac{g_{m1}}{g_{ds1} + g_{ds2} + g_{m3}} \cdot \frac{g_{m41} + g_{m42}}{g_{ds41} + g_{ds42} + g_{ds5} + \frac{1}{R_L} - g_{mb42}}, \qquad (5.12)$$

where R_L is the resistance of the second to the fourth integrators, which is 600 kΩ in this design. In addition, the cross-coupled output transistors realize class-AB characteristic, and hence increase the slew rate of the amplifier.

Noted that there is a trade-off between the gain and the stability in the cross-coupled structure, the size of M_{42A}/M_{42B}, which is shown in Fig. 5.22, was selected so that g_{mb42} is around 0.7 of the sum of g_{ds41}, g_{ds42}, g_{ds5} and $1/R_L$. Simulations prove that such a selection ensures a stable amplifier with a high enough dc gain. Fig. 5.23 shows the frequency responses of the 1st amplifier under process, voltage, and temperature variations. The voltage variation is set as ±10%, and the temperature variation is from -40°C to 125°C. All the devices are simulated with different process corners, except the loading resistors. Since the integration resistances R_2-R_4 can be tuned (see Section III.E), the loading resistances in the simulation are replaced by ideal resistances with ±10% variation. As shown in Fig. 5.23, the worst-case dc gain and gain-bandwidth of the 1st amplifier is higher than 40dB and the sampling frequency, respectively, which are sufficient for achieving the targeted SNR, based on the discussion in Chapter 3. In addition, the amplifier is stable under all the corners.

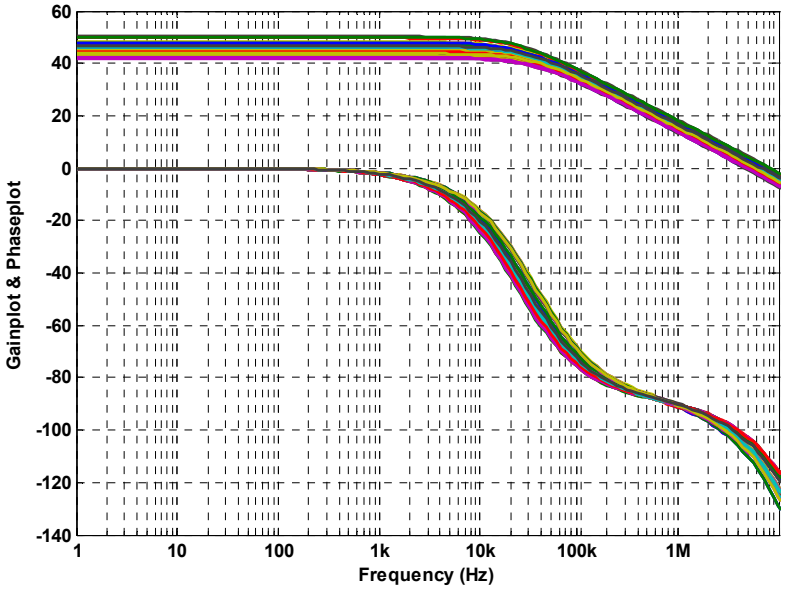


Figure 5.23: Bode plot of the 1st amplifier across process voltage temperature variations.

The typical simulation results of the 1st amplifier are summarized in Table 5.6. With the gain-enhancement technique, the typical dc gain of the 1st amplifier is increased from 35.7 dB to 46.6 dB. The total biasing current of the 1st amplifier (including the biasing and the CMFB circuit) is designed at 19.3 µA. The input transistors M_{1A} and M_{1B} are designed with large transconductance and large dimension to minimize the amplifier's thermal and flicker noises.

Table 5.6 Simulated performances of the 1st amplifier in the 1-bit audio Delta-Sigma modulator.

Parameter	Amp1
GBW (MHz)	5.13
dc gain Pro./Con. (dB)	46.6/35.7
Phase Margin (degree)	73.4
In-band noise (µV)	6.5
Load (pF//kΩ)	8//600
Static Current (µA)	19.3

For the 2nd to the 4th integrators, their nonidealities are suppressed by the noise-shaping effect, and hence amplifier's requirements are relaxed. The dc gains of these three amplifiers are set at around 38 dB, and the gain-bandwidths are designed no higher than 1.5 f_s. The total static current consumed by the three integrators is around 15.3 μA.

B. *Proposed Body-Driven Rail-to-Rail Input Common-Mode FeedBack Circuit*

CMFB circuit is necessary in the active-load fully-differential amplifier to control its common-mode voltage. Low-voltage operation limits the input range of the continuous-time CMFB circuit. In the traditional CMFB circuit, as shown in Fig. 5.24, the input voltage range V_{ic} is in the range:

$$V_{GS2} - |V_{TH1}| < V_{ic} < V_{DD} - |V_{DSat0}| - |V_{TH1}|. \tag{5.13}$$

Under sub-1V supply operation, the common-mode voltage of the amplifier, which is normally around half V_{DD}, is very likely to lead the CMFB circuit out of the saturation region, resulting speed degradation, even a malfunction circuit under even lower supply voltage. One way to solve this problem is to shift the common-mode level of the amplifier from $V_{DD}/2$ to one within the input range of the CMFB circuit [Kim08]. Such approach requires additional circuit while causing no improvement to the CMFB input range. Another solution is to use a resistor pair together with a current tail in the CMFB circuit but with a complex biasing for the reliability over process, supply, and temperature variations [Pun07] [Cha05].

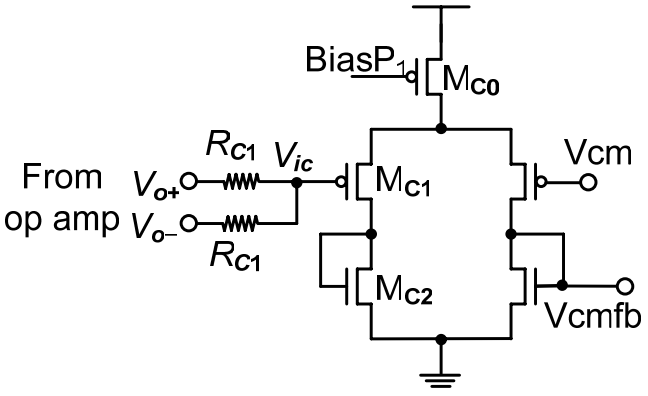


Figure 5.24: Traditional CMFB circuit.

In our design, a body-driven rail-to-rail CMFB circuit is proposed, as shown in Fig. 5.25, whose input are four body-input transistors. The bodies of transistors M_{C1A} and M_{C1B} are connected to the amplifier's outputs, and the bodies of transistors M_{C1C} and M_{C1D} are connected to the common-mode voltage V_{cm}. The output signal V_{cmfb} is fed back to the amplifier to control its output common-mode level (see Fig. 5.22). The diode-connected transistor M_{C2B} is used to control the output impedance, and the gain of the CMFB circuit can be derived as:

$$A_{CMFB} \approx \frac{2 \cdot g_{mb1}}{g_{m2}}. \tag{5.14}$$

The CMFB circuit dc gain is around -4dB, and the dc gain of the whole CMFB loop, which includes transistors M_5, M_{41} and M_{42} (see Fig. 5.22), is at 16.4 dB with a 1.1 MHz GBW and 76 degree phase margin.

Since the depletion junction between the body and the source allows positive, zero and slightly negative bias voltage, a rail-to-rail common-mode input range can be achieved for the proposed CMFB circuit under 0.6-V supply voltage or below. Furthermore, the proposed CMFB circuit has no impact on the amplifier's dc gain and saves the area by eliminating the sensing resistors (R_{C1} in Fig. 24).

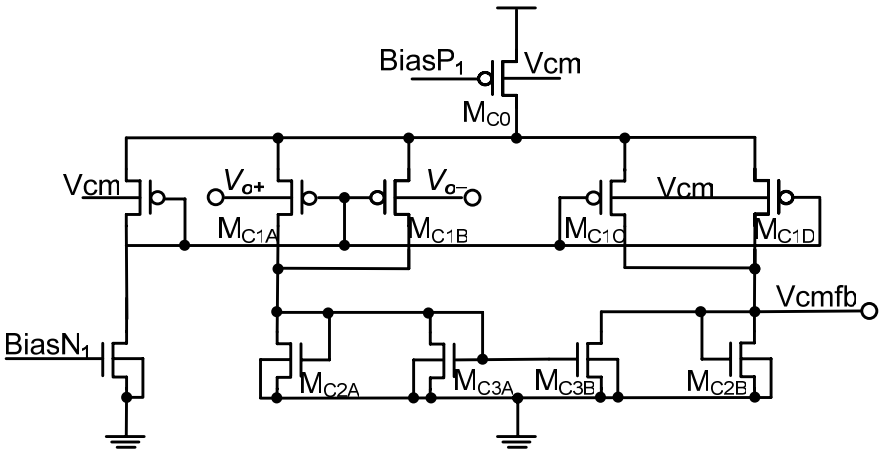


Figure 5.25: Proposed body-driven rail-rail input CMFB circuit.

One problem with this CMFB circuit is that, its input transistors M_{C1A} and M_{C1B} detect directly the amplifier's output swing rather than the amplifier's output common-mode level. The large swing at the bodies of M_{C1A} and M_{C1B} may lead to even-order harmonics at the CMFB output node V_{cmfb} (see Fig, 5.25). The simulation for a -3dBFS input shows that, thanks to the feedforward topology, the second-order harmonic distortion at the 1st amplifier's CMFB output V_{cmfb} is -87.4dBFS only. In addition, the influence of the distortion at V_{cmfb} can be rejected by the fully-differential structure. The measurement results in section IV also prove that the 2nd-order distortion is well suppressed.

C. *Other Circuit Designs*

The quantizer, DAC, and RC time-constant tuning circuits are similar to those in the wide-band Delta-Sigma modulator, which is presented in Chapter 4.

For the sampling clock, since the lowest frequency our low-jitter pulse generator (Agilent-8133A) can generate is about 31 MHZ, a 4-bit counter is designed to down convert the high frequency before it is used by the modulator. A dedicated supply is used for the clock generator to reduce the clock jitter effect.

5.3.4 Layout

The prototype modulator was fabricated in a standard 0.13-μm CMOS process. High-resistivity poly resistors and Metal-Insulator-Metal (MIM) capacitors were used for their high linearity. Several layout techniques are used to ensure a good performance, such as common-centroid layout for the 1st integration capacitors, inter-digitation for the multi-finger transistors, dummy cells for transistors, guard rings for analog/digital separation. Fig. 5.26 shows the chip die photo of the modulator, and the main blocks are labeled. Due to the novel structure for the feedforward and summation part, the core area of the modulator is 0.11 mm^2.

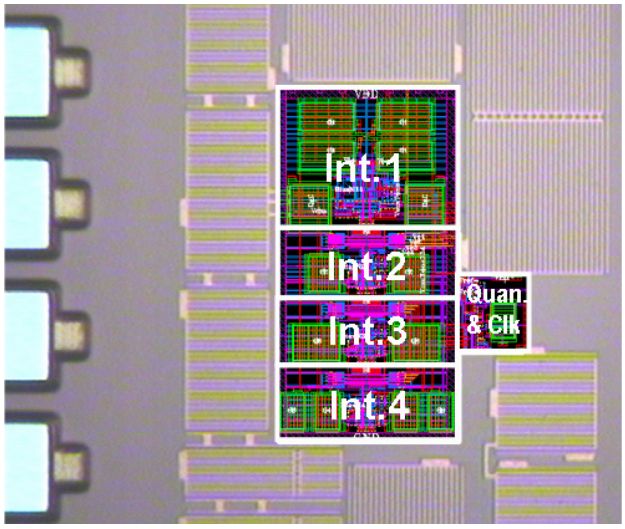


Figure 5.26: Die micrograph of the single-bit audio Delta-Sigma modulator.

5.3.5 Test Setup

All the dc signals are generated on the board, including the analog supply, digital supply, biasing voltages, and references. To lower down noise, dc signals are originated from low-noise voltage references (Texas Instruments REF5020), tuned by potentiometers, driven by low-noise low-distortion amplifiers (Texas Instruments OPA350 series), and filtered by RC filters, as shown in Fig. 5.27.

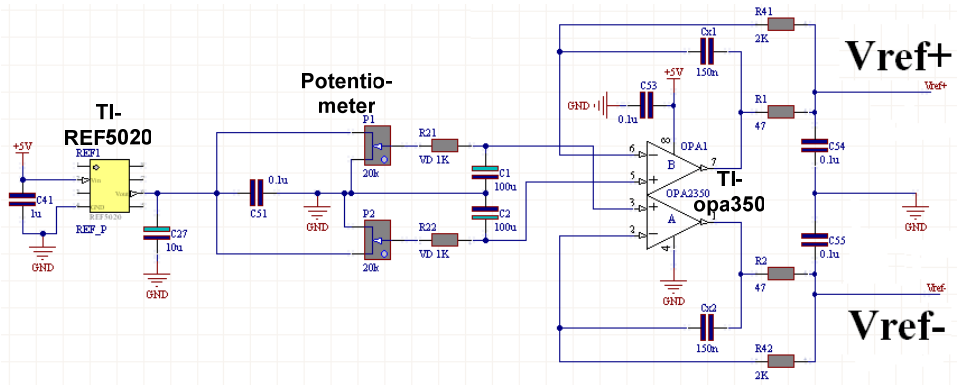


Figure 5.27: PCB schematic for the generation of reference voltages.

Four-layer PCB was designed to test the prototype chip. The top and bottom layers are used to route signal lines, and the second and third layers are used as ground planes and supply planes, respectively. The top view of the PCB is shown in Fig. 5.28.

Fig. 5.29 shows the diagram of the test setup. SRS DS360 is used to generate the differential input signals. Agilent 8133A pulse generator is used to provide low-jitter clock. The prototype chips have been tested. The output data were captured by the Agilent 1672G logic analyzer and then processed with Matlab in a PC. Current is measured with Agilent 34401A multi meter.

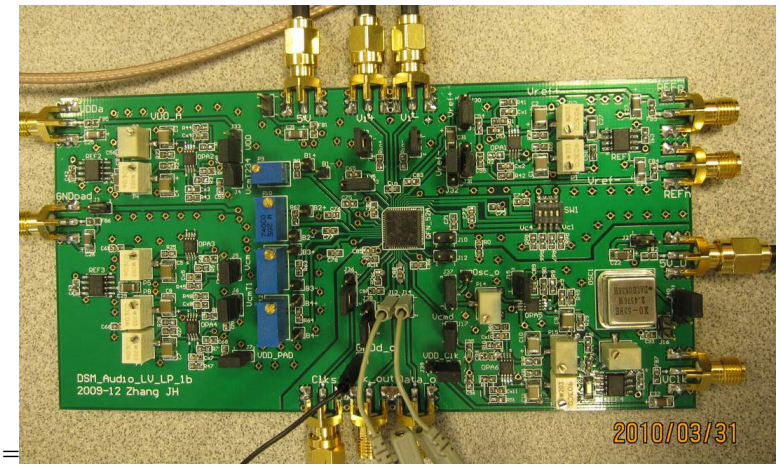


Figure 5.28: Testing PCB for the single-bit audio Delta-Sigma modulator.

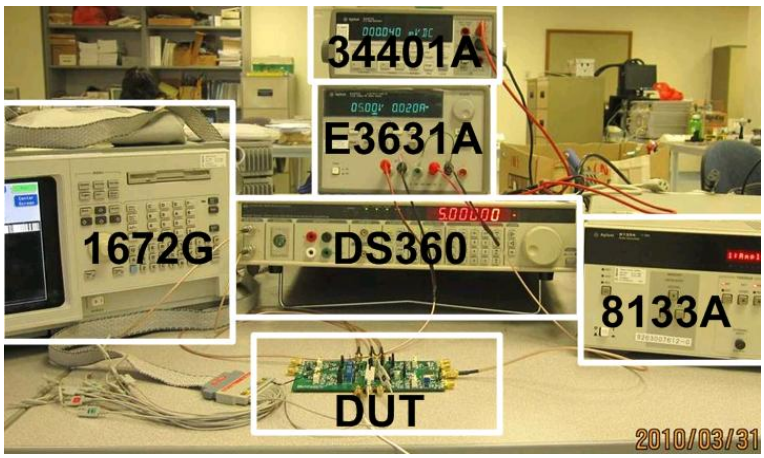


Figure 5.29: Test setup environment of the single-bit audio Delta-Sigma modulator.

5.3.6 Measurement Results

The prototype chip has been tested. Low-distortion function generator (SRS DS360) is used to generate the differential input signals. Clock generator (Agilent-8133A) with less than 1-ps jitter is used to provide accurate clock source. The output data are captured by a logic analyzer (Agilent 1672G) and then processed with Matlab codes in a PC. Figure 5.30 shows the measured output spectrum for a 0.5-V 5-kHz input signal. The SNR and SNDR curves versus the input power are shown in Fig. 5.31. Measurement results show that the modulator achieves a peak SNDR of 79.1 dB, a peak SNR of 80.1 dB, and a DR of 82 dB, and the design target is met.

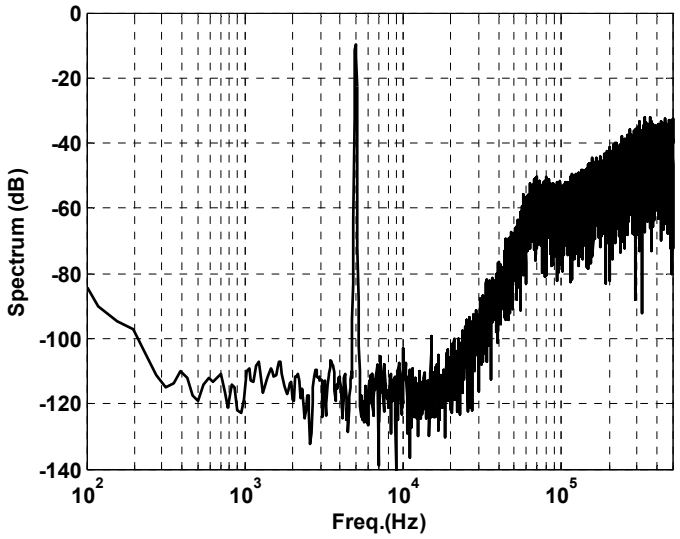


Figure 5.30: Measured output spectrum for the 1-$V_{pp\text{-}diff}$ 5-kHz input, FFT bins are 65536.

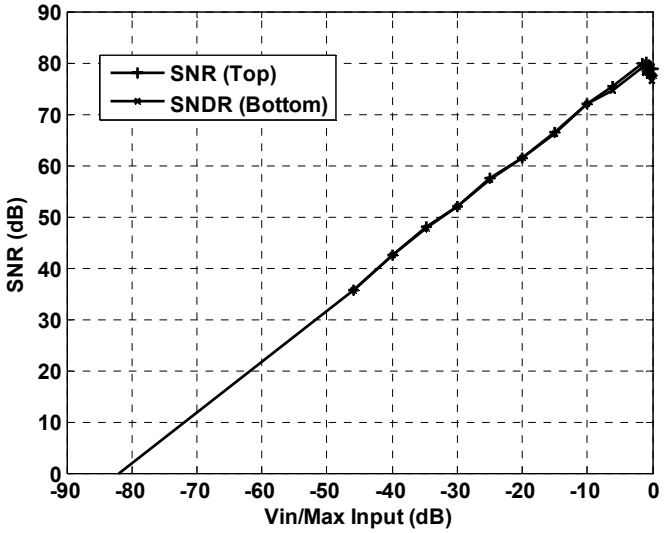


Figure 5.31: SNR/SNDR versus the input power.

The measured performances are summarized in Table 5.7. The peak SNRs and SNDRs under ±10% supply variations are also given in the table. The measured power consumption for the analog part is 22 μW, and for the digital circuit (including the quantizer, DAC circuit, and clock generator) is 6.6 μW. With 0.6-V supply, the modulator's performance under different temperatures are also measured and shown in Fig. 5.32. Due to the equipment limitation, the temperature range is from 25°C to 80°C. According to the results, there is less than 1.8 dB degradation in SNR and SNDR across the temperatures.

Table 5.8 compares this design with recent reported sub-1V audio Delta-Sigma modulators, where FOM is calculated by $FOM = Power/(2 \cdot BW \cdot 2^{(SNDR\text{-}1.76)/6.02})$. Compared to other sub-1 V audio Delta-Sigma modulators, this work shows good performance in the power consumption, area, and FOM.

Table 5.7 Measured performances of the 1-bit audio Delta-Sigma modulator at 25°C.

Signal Bandwidth	20 kHz		
Clock Frequency	2.56 MHz		
OverSampling Ratio	64		
Input Range	1.2 $V_{pp\text{-}diff}$		
Supply Voltage	0.54 V	0.60 V	0.66 V
Dynamic Range		82 dB	
Peak SNR	76.9 dB	80.1 dB	79.6 dB
Peak SNDR	76.3 dB	79.1 dB	78.5 dB
Power Consumption	22 μW (A), 6.6 μW (D)		
Core Area	0.39mm×0.27mm		
Technology	0.13-μm standard CMOS single-well		

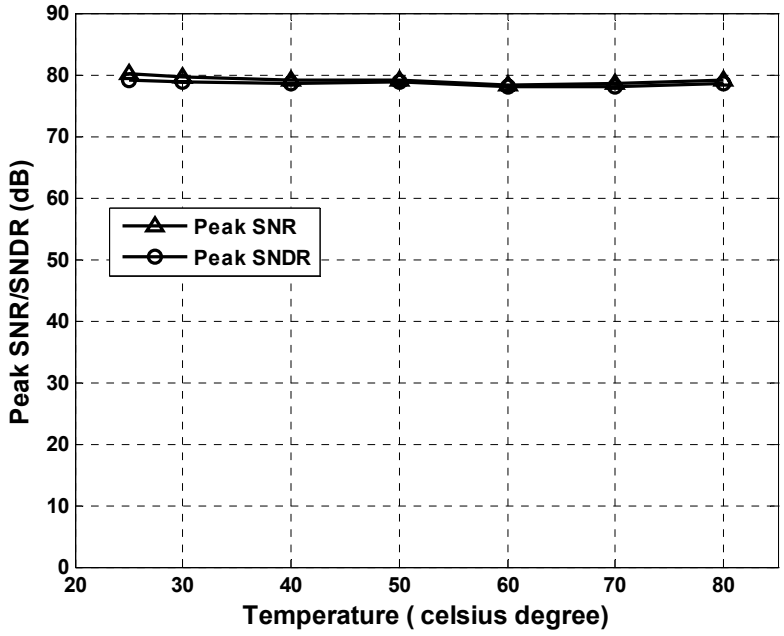


Figure 5.32: Peak SNR/SNDR versus temperature variations, the supply voltage is 0.6V.

Table 5.8 Comparison with other sub-1V audio Delta-Sigma modulators.

Ref	Type	BW (kHz)	SNDR (dB)	Power (μW)	Supply (V)	Tech. (μm)	FOM (pJ/conv.)	Area (mm^2)
[Pel98]	DT	16	62	40	0.9	0.5	1.215	0.85
[Ahn05]	DT	24	81	1000	0.6	0.35	2.272	2.88
[Pun07]	CT	25	74	300	0.5	0.18	1.465	0.6
[Kim08]	DT	24	89	1500	0.9	0.13	1.357	1.44
[Roh08]	DT	20	73.1	60	0.9	0.13	0.406	0.42
[Cha08]	DT	20	81	36	0.7	0.18	0.098	0.72
[Par09]	DT	25	95	870	0.7	0.18	0.379	2.16
[Mic11]	DT	10	61	7.5	0.25	0.13	0.409	0.34
This Work	CT	20	79.1	28.6	0.6	0.13	0.097	0.11

5.3.7 Conclusion

Section 5.3 has presented a low-voltage low-power continuous-time Delta-Sigma modulator design for audio applications. To minimize power consumption while maintaining good performance, several low-power techniques are utilized at both system and circuit levels. Our goal is to come up with a simple structure and energy efficient circuit for low-voltage operation. At the system-level, the CT loop filter is employed to eliminate the switches in the DT loop filter, which relaxes the settling requirements on amplifiers. The input-feedforward topology is adopted for its suppressed internal swings. At the circuit-level, a simple and power-efficient single-stage amplifier structure is developed for the low-voltage operation. To compensate its dc gain degradation in the amplifier, body-driven gain-enhancement technique is proposed. To relax the input range constrain of the CMFB circuit, a body-driven rail-to-rail input CMFB circuit is proposed. The realization of feedforward coefficients is embedded in the quantizer, so as to save power and chip area, and to simplify the circuit design. The core area of the modulator is 0.11 mm^2. Clocked at 2.56 MHz, the Delta-Sigma modulator achieves 82-dB dynamic range with 28.6-μW power consumption under 0.6-V supply voltage and 25°C. The performance is measured maintained over a ±10% supply variation and 25°C to 80°C temperature variation. The

measured results verified that the proposed techniques successfully reduce the power consumption under low-voltage supply while maintaining good performance.

5.4 Conclusion

This chapter presents low-voltage low-power continuous-time Delta-Sigma modulator designs for audio applications. Two design examples are given.

In the first design example, a 4^{th}-order 1.5-bit input-feedforward topology with optimized coefficients is adopted. The feedforawrd and summation part is embedded in the 1.5-bit quantizer to save the power and the area. A simple DEM circuit is used to improve linearity. The post-layout simulation shows that the modulator achieves a 100.9-dB DR under 1-V operation, and the power consumption is 42.6 μW.

In the second design example, the supply voltage is lowered down to 0.6 V. A power-efficient and gain-enhanced amplifier, and a rail-to-rail input CMFB circuit are proposed. The body-driven technique is only utilized in PMOS transistors to avoid using high-cost triple-well process. The Delta-Sigma modulator achieves 82-dB dynamic range with 28.6-μW power consumption. The measurement results verify that the modulator achieves a good performance while the power consumption is reduced to a very low level.

CHAPTER 6

CONCLUSIONS

6.1 Thesis Summary

The Delta-Sigma ADC is one of the most popular analog-to-digital converters, due to its high resolution, high linearity, and good compatibility with the digital circuitry. The research work has focused on the low-voltage low-power continuous-time Delta-Sigma modulator design. The low-voltage low-power design is motivated by the growing market of the portable products.

Before detailed designs, the basics of the Delta-Sigma modulator are first reviewed in Chapter 2. The principle operation of the Delta-Sigma modulator is based on the oversampling technique and the noise-shaping technique. By using high oversampling ratio and high order, the Delta-Sigma modulator can achieve very high resolution. The various types of Delta-Sigma modulators are also introduced. Among these topologies, the continuous-time input-feedforward topology is adopted in the presented designs, due to its attractive potential for the low-voltage low-power design. Literature review on the low-voltage low-power Delta-Sigma modulator designs is also give in Chapter 2.

To achieve successful low-voltage low-power designs, both system-level and circuit-level issues have been addressed. The main work and key contributions of this research are summarized below:

Chapter 3 presents the system-level designs and simulations. The method for exploiting a CT topology from a DT counterpart is given. The Simulink-based model for the CT Delta-Sigma modulator is proposed. Based on the model, nonidealities in the CT Delta-Sigma modulator are simulated and analyzed, some solutions are given. Some of these nonidealities may degrade the

modulator's performance greatly, and careful considerations on them are required during the following designs. These nonidealities include the clock jitter, the excess loop delay, the time-constant variation, and the finite amplifier gain and gain-bandwidth.

In Chapter 4, a 4^{th}-order single-bit input-feedforward CT Delta-Sigma modulator with 1.25-MHz signal bandwidth is presented for the wideband applications. A power and area efficient structure is proposed, in which the feedforward and summing part is embedded into the quantizer. The design was fabricated with advanced IBM 0.13-μm CMOS technology, and has been tested with the designed PCB. Clocked at 160 MHz, the Delta-Sigma modulator achieves 68-dB dynamic range. The modulator consumes 2.7-mW power consumption under 1.2-V supply voltage. The core area of the modulator is 0.082 mm^2. The measurement results verify that the proposed feedforward and summing structure is effective to reduce the power consumption with a small silicon area

Chapter 5 presents two low-voltage and low-power CT Delta-Sigma designs for the 20-kHz audio applications. A 1-V 1.5-bit input-feedforward CT topology is presented first. The feedforawrd and summing part is embedded in the 1.5-bit quantizer. A simple dynamic element matching circuit is designed to improve linearity. Designed in IBM 0.13-μm CMOS technology, and simulated with post-layout RC extraction, the modulator shows a peak signal-to-quantization noise ratio of 100.5-dB with a 42.6-μW only power consumption. The other design is a 0.6-V single-bit input-feedforward CT Delta-Sigma modulator. A simple and power-efficient amplifier structure is used to lower down the power consumption. The body-driven gain-enhanced technique is proposed to compensate the gain degradation in the low-voltage operation. In addition, a novel rail-to-rail input CMFB circuit is presented for the low-voltage operation. The body-driven technique is only utilized in PMOS transistors to avoid using high-cost triple-well process. Fabricated with IBM 0.13-μm CMOS technology, the design shows a 82-dB dynamic range with 28.6-μW power consumption. Compare with other audio Delta-Sigma modulators, this design shows good performance in the power consumption, the area, and FOM.

6.2 Future Work Suggestions

This research explores some low-voltage low-power design techniques for the Delta-Sigma modulator. The continuous-time input-feedforward topology, and the novel feedforward and summing structure have been proven to be effective for the low-voltage and low-power design. Based on these techniques, it is worth exploring the Delta-Sigma modulator designs under 0.5-V or even lower supplies. The suggestions to the future work are shown below:

1) Low-voltage amplifier design

Amplifier is an important part, which constraints the minimum supply voltage of the CT Delta-Sigma modulator. In Section 5.4, a 0.6-V fully-differential amplifier is designed. Since the input common-mode voltage of the amplifier is set at half of the supply, it constraints the minimum supply voltage (see Eq. 5.27). For the active-RC filter, its input common-mode voltage can be shifted away from the half of the supply [Kar00] [Bul00]. However, this technique needs one additional current source/tail, which consumes more power. Another solution is to use pseudo-differential amplifier. Since there is one less stacked transistor in this structure, the supply voltage of the pseudo-differential amplifier can be reduced lower than that of the traditional differential amplifier. However, the main problem of the pseudo-differential amplifier is the low CMRR performance. Thus, compensation technique is required.

2) Multi-bit input-feedforward CT Delta-Sigma modulator design

In Section 5.3, a 1.5-bit Delta-Sigma modulator is designed. In the future work, the quantizer level can be further increased. As discussed in Chapter 3, the multi-bit quantizer shows many advantages over the single-bit quantizer, such as the lower quantization noise, better stability, and less sensitivity to the clock jitter. However, the multi-bit quantizer needs additional comparators, which increase the loads of the integrators. One solution is to use successive approximation register (SAR) technique in the quantizer. However, how to sample and hold the signal when

SAR is working is a problem. Another problem of the multi-bit Delta-Sigma modulator is that, it requires the correction circuits in the DAC circuit. These correction circuits consume more power and area. Furthermore, they will increase the excess loop delay, which may degrade the resolution of the modulator. Therefore, delay compensation technique may be needed.

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