NOVEL MODELLING METHODS FOR MICROWAVE GaAs MESFET DEVICE

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Summary

As one of the most widely used microwave devices, the gallium arsenide metal semiconductor field effect transistor (GaAs MESFET) dominates in modern MIC/MMIC applications such as switches, power amplifiers, low noise amplifiers, oscillator, etc. Reliable modelling methodology and accurate device models of GaAs MESFET are currently extremely important and in great demand.

In this thesis, both small signal and nonlinear large signal models of GaAs MESFETs have been investigated. This study first involves investigation and comparison of different small-signal parameter extraction techniques. A reliable analytical small signal model extraction approach is subsequently presented. For the first time, a novel analytical approach for extracting all the 15 equivalent circuit elements of GaAs MESFET devices has been proposed with no subsidiary circuit such as Cold-FET or Hot-FET techniques. On the other hand, for the relatively high operating frequencies, a new GaAs MESFET distributed model based on accurate EM simulation and quasi-optimization method has also been proposed in this thesis. This distributed model can be adopted to describe complex parasitic effects in device layouts and to predict the electrical characteristics of unconventional device structures for better MMIC performance.

For the large-signal modelling of GaAs MESFET, a new empirical model is

developed. To further refine the drain current description, a set of power series function is introduced in the improved drain current expression for the correlations between modulation parameters α, λ and biasing condition V_{ds} & V_{gs}. Moreover, a new gate terminal charge model for C_{gs} and C_{gd} description is also proposed under gate charge conservation law. The model expressions and their derivatives are continuous over the entire device bias range. This new large signal model can be easily implemented in CAD software and is very useful in the nonlinear microwave circuit simulation. For complete model evaluation, a Ku-band power amplifier has been designed and fabricated using 0.18 um TOSHIBA® GaAs MESFET technology. Simulated and measured amplifier performances have been investigated and good agreement has been demonstrated.

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a_1, a_2, a_3	Model parameters for the new drain-source current model
b_1, b_2, b_3	Model parameters for the new drain-source current model
$C_1 ... C_{11}$	Model parameters for the new gate charge model
C_b	The fringing capacitance due to depletion layer extension at each side of the gate in the improved gate capacitance model
C_{dc}	Capacitor modelling the drain electrode to conduction channel feedback current
C_{ds}	Drain-to-Source capacitance of a MESFET device
C_{gd}	Gate-to-Drain capacitance of a MESFET device
C_{gd0}	Gate-to-Drain capacitance at zero V_{gs} bias, model parameter for the new gate charge model
C_{gs}	Gate-to-Source capacitance of a MESFET device
C_{gs0}	Gate-to-Source capacitance at zero V_{gs} bias
C_{pd}	Parasitic capacitance associated with the drain of a MESFET device
C_{pg}	Parasitic capacitance associated with the gate of a MESFET device
D_{gs}	Gate-to-Source junction diode
D_{gd}	Gate-to-Drain junction diode
f_0	Fundament frequency
$2f_0$	Second harmonic frequency
$3f_0$	Third harmonic frequency
g	Model parameter for the new drain current model
g_{ds}	Output conductance of a MESFET device
g_m	Transconductance of a MESFET device
I_{ds}	Drain-to-Source current of a MESFET device
I_{Dsat}	Saturation drain source current of a MESFET device with zero gate-to-source bias applied
I_{gs}	Current flowing through the gate terminal of the MESFET device
k	Boltzmann's constant
L	Gate length of a MESFET device
L_d	Parasitic drain inductance of a MESFET device
L_d	Parasitic gate inductance of a MESFET device
L_s	Parasitic source inductance of a MESFET device
m	Capacitance gradient factor in diode capacitance model

R_{ch}	Channel resistance at cold-FET $V_{gs}>V_{bi}$ condition
R_d	Parasitic drain resistance of a MESFET device
R_g	Parasitic gate resistance of a MESFET device
R_{gd}	Resistor introduced in some small signal equivalent circuits to fit the Y_{12}
R_i	Equivalent charge resistance of a MESFET device
R_s	Parasitic source resistance of a MESFET device
R_{ds}	Output resistance of a MESFET device
P_{in}	Input power for device and amplifier measurement
P_{out}	Device or amplifier output power
q	Electronic charge
Q_g	Gate charge of a MESFET device
$S_{11},S_{12},S_{21},S_{22}$	S-parameter of the device
V_{bi}	Build-in voltage of the Schottky gate
V_{ds}	Drain-to-Source voltage
V_{Dsat}	Drain-to-Source saturation voltage
V_{gd}	Gate-to-Drain voltage
V_{gs}	Gate-to-Source voltage
$V_{pinchoff},V_{T0},V_p$	Pinch-off or threshold voltage of a MESFET device
V_{ST}	Model parameter for the new drain current model
$Y_{11},Y_{12},Y_{21},Y_{22}$	Y-parameter of the device
$Z_{11},Z_{12},Z_{21},Z_{22}$	Z-parameter of the device
α	Parameter introduced in the improved parasitic capacitance model
β, γ, μ_{crit}	Model parameter for the new drain current model
τ	Transconductance delay

Chapter 1

Introduction

Today, the gallium arsenide metal semiconductor field effect transistor (GaAs MESFET) has served as the driving force behind the impressive technological advancements of microwave and millimeter-wave integrated circuits. Due to its relatively simple geometry with great versatility and outstanding performance, the GaAs MESFET has become one of the most important semiconductor devices in MMIC technology and digital GaAs ICs. In this chapter, the general overview of GaAs MESFET and the device model is presented, followed by the objectives and the structure of this dissertation.

1.1 Overview of GaAs MESFET

1.1.1 History of GaAs MESFET

The first development of a prototype gallium arsenide field effect transistor using a Schottky gate was undertaken by Mead in 1966 [1]. In 1967, a GaAs MESFET was first fabricated by Hopper and Lehrer [2]. A significant step was made by Turner et al in 1971 [3], when 1 μm gate length GaAs MESFET was fabricated, giving f_{max} equal to 50GHz and useful gain up to 18GHz. With the development of the

quality of GaAs materials and basic FET prototype technology, rapid progress was achieved for GaAs MESFET devices in the direction of both low noise and high power applications. The first low noise GaAs MESFET was reported by Leichti et al. [4] in 1972. And later in 1973, the first high power GaAs MESFET was announced by Fukuta et al. in Fujitsu [5]. With the early progress of GaAs MESFET technology, this had been followed by rapid improvement of the device performance. Intensive studies have been done in increasing its output power, operating frequency and power added efficiency as well as improving the distortion qualities and noise figure.

In addition to the discrete FET area, there also has been rapid development in both monolithic microwave integrated circuits (MMICs) and digital GaAs integrated circuits. MMIC technology has become popular since middle 1970s, and the first GaAs digital IC was reported in 1974 [6].

In the late 70s and the 80s, the GaAs MESFET was developed mainly for low volume, high performance military and space based systems. The manufacturing technology was not mature enough to support the cost and volume requirement for the consumer mass market. By the early 1990s, however, GaAs MESFET manufacturing technology was maturing rapidly, cost was reduced. As a result, GaAs technology became more competitive with other process technologies. Since then, the GaAs MESFET device and GaAs integrated circuits have found a wide range of applications, such as in wireless systems. Now, the GaAs MESFET is widely used in different microwave and millimeter wave systems, and has become the most important active device in both hybrid and monolithic microwave integrated circuits (HMIC and

MMIC) design. Typical applications include both low noise and power amplifiers, as well as transfer switches, attenuators, oscillators, and mixers. The demand for mobile and personal communication systems has increased the use of GaAs MESFET for high-speed digital and analog integrated circuits.

Other transistor technologies have been developed to cover a variety of applications in high frequency application from 1GHz to more than 100GHz. GaAs based heterojunction devices including high electron mobility transistor (HEMT) and heterojunction bipolar transistor (HBT) provide several performance advantages. In the case of HEMT technology, it has the advantage of higher frequency performance (f_T, f_{max}), and lower noise figure than that achievable by MESFET of similar gate length. GaAs HBT technology has high transconductance, high power density, and excellent matching of a bipolar transistor. Also, the HBT transistor can operate from a single power supply. GaAs HBTs are commonly used for high power amplification applications. InP transistors (HBTs, HEMTs) would dominate at extremely high frequency. Wide band-gap FETs will be used in high power amplifiers. However, their market share is small because SiC substrate is expensive, and SiC and GaN technology is still in an embryonic stage compared to GaAs. Despite the superior performance of these technologies mentioned above, GaAs MESFET technology remains competitive for various applications. Its performance is adequate for many areas, and has a lower cost.

In recent years, GaAs MESFET technology is also facing serious competition from silicon and silicon-germanium technologies in RF and microwave applications.

CMOS continues to advance to smaller geometries. SiGe BiCMOS gives good performance for RF and high speed. Compared to silicon, GaAs has a higher electron mobility and peak drift velocity. The electron velocity at low field is sufficiently high so that high switching speed and therefore high cut-off frequency can be achieved. The primary advantages for using GaAs over silicon are large transconductance, low ON resistance, and fast switching speed. Unlike Silicon, a semi-insulting GaAs substrate can be formed. This contributes to the simple structure of the GaAs MESFET, and the high resistivity of the GaAs substrate results in very small parasitic capacitance. GaAs technology also has the strength of integrating RF functions in stripline and coplanar design into MMICs. The drawback of MESFET technology is a limitation related to the voltage swing limited by the gate-leakage current; this reduces the noise margin of the circuit. On the other hand, silicon technologies have been more matured, and provide a higher level of integration. Silicon technologies also have the advantage of integrating analog design with digital design. This makes it possible to design single chip ICs for mixed signal systems. For SiGe devices, the low breakdown voltage limits their usage in power applications. Compared to SiGe devices, the GaAs FET gives more efficient power amplification. In summary, Si and SiGe RF, high speed ICs are assuming an increasing portion of RF front-end for many wireless applications below 5GHz. Their applications also cover highly integrated digital data transceivers and optical communications. GaAs devices normally dominate when higher frequency and increased power requirement are addressed.

GaAs MESFET is the workhorse of GaAs Technology. Its gate length on the

market ranges from 0.18μm to 0.5μm. To sum up, GaAs MESFET has wide applications even though it is facing strong competition from other device technologies.

1.1.2 Overview of Device Model

In the early days, microwave circuit design was based upon a low volume cut-and-try approach in which a preliminary design was built, tested and optimized until the desired performance is obtained. The circuit was then redesigned and fabricated. This approach was engineering labor intensive and not compatible with low production costs. The computer-aided design (CAD) then emerged to permit the circuit design to be completed, simulated and fully tested in the computer before its fabrication. Nowadays, with the development of GaAs FET and MMIC techniques, MMICs are widely available for commercial and military application. MMICs require a long process cycle to complete and the development cost is high. In addition, as a result of hardware prototype limitations, it is usually impossible to access internal circuit points to make alterations when circuit performance is unsatisfactory. Therefore, it is very important to accurately simulate the circuit during the design stage, so as to closely correlate the design result with its practical performance. Commercially available CAD software such as Agilent®-ADS and Cadence® SpectreRF are widely employed in microwave system design. The accuracy of simulation results of these CAD tools is largely based on an accurate prediction of the device involved in the circuit. As a result, accurate models for both active and passive

devices and elements are greatly needed. Specifically, since GaAs MESFETs are the main building blocks of a large number of microwave applications, it is absolutely necessary to develop accurate GaAs FET models to improve the circuit performance prediction.

Currently a good number of GaAs MESFET models exist, and each of them can be classified into specific categories. For example, these FET models can be grouped into physically based model, empirical model and experimental model based on their derivation. Among these three, the empirical model can be easily implemented into circuit simulators. Thus, they are most widely used by circuit designers and in device libraries. Moreover, according to different types of their prediction performance, these FET models can also be grouped into small-signal model and large-signal model. Small-signal model mainly focuses on the scattering-parameter of the device whilst the large-signal model is important for nonlinear MESFET modelling. Although much work has been done in the modelling of GaAs MESFET, accurate linear and nonlinear models of this active device are still in great demand.

1.2 Objectives

The purpose of this work was to develop new approaches to accurately model GaAs MESFETs devices. First the small signal modelling methodology is studied as it is the basis of large signal modelling. The goal of the investigation is to find a reliable analytical extraction method by which all the values of extrinsic and intrinsic elements in the equivalent circuit of GaAs MESFET small signal model can be

accurately extracted. Improvement is also made over some existing models for the S-parameter matching performance. Secondly, when GaAs MESFETs operate at higher working frequency beyond 30 GHz, some parasitic elements should be added into the equivalent circuit to take into account their effect which could be ignored in the low frequency region. Therefore, a new distributed small-signal model based on electromagnetic field theory and circuit analysis should be subsequently investigated to meet the requirement. Although the main focus of this work lies in GaAs MESFET, distributed small signal modelling methodology for GaAs HBT would also be studied in this part as the issues are similar.

For the large signal modelling, the aim of this work is to develop a new empirical large signal model for accurate description of the most important GaAs MESFET nonlinear behavior, including drain current I-V and gate capacitance characteristics. Furthermore, these models discussed above should give an accurate representation of device operation under different bias conditions. They should be easily implemented into a circuit simulator, and the model parameters should be extracted with reasonable effort.

1.3 Scope of the work

Chapter 2 provides a brief discussion of the operation of GaAs MESFET and a review of the existing models. First, a basic description of the MESFET device is presented. Topics addressed are the MESFET physical structure and different MESFET operation regions. After examining the basic device operations, the small

signal equivalent circuit and the physical original of the equivalent circuit elements are introduced. This is followed by nonlinear properties in MESFET and some second order effects. Finally, existing MESFET modelling approaches are discussed, including small signal models and nonlinear models. An overview of the small-signal parameter extraction method, physical model, empirical model, and experimental model are presented.

Small signal modelling methodology for GaAs MESFET and discussion of model parameters extraction techniques form the subjects of Chapter 3. The main aim of this chapter is to provide an analytical and more accurate small signal equivalent circuit parameter extraction method. First, some important concepts for parameter extraction are addressed, including de-embedding technique and the selection of an objective function. This is followed by a discussion of small signal model parameter determination methodologies. Both cold-FET and hot-FET techniques are covered. For most of these traditional small signal modelling methods, the results of some extrinsic parameters vary more or less with different biasing conditions, which would decrease the accuracy of its s-parameter performance. This violates the assumption that parasitic elements should be independent of biasing voltage. Moreover, the traditional cold-FET technique will bring irreversible damage to the GaAs MESFET device itself. This analytical method effectively eliminates the conventional cold-FET and hot-FET modelling constraints and allows an ease in inline process tracking. In addition, the resulting parasitic capacitances are independent of bias, which is in agreement with theory. Based on the discussions in the earlier sections, the following

sections in Chapter 3 focus on the investigation and comparison of different small signal parameter extraction methods. Numerical results are compiled and compared. As a result of the investigation, a reliable analytical small signal parameter extraction method is proposed.

In Chapter 4, a novel distributed small-signal model for GaAs MESFET/HBT at millimeter-wave frequencies is proposed. This new approach integrates the electromagnetic simulation of the outer extrinsic passive part of a GaAs FET, the coupled transmission lines for the fingers and the Gupta multi-port connection into an efficient global distributed modelling approach. For the first time, the values of the entire GaAs MESFET intrinsic model elements used in the active elementary cells can be subsequently extracted through the explicit analytical expressions derived through the quasi-optimization method. Good agreement between the measured and the simulated results has been demonstrated. This model also allows the designer to have better control over the whole transistor design. Furthermore, it serves as one of the valuable steps towards global modelling of millimeter-wave devices and circuits.

The drain current I-V characteristic and gate charges are the most important MESFET nonlinear properties. Their accuracies are critical for the overall performance of the device model. Chapter 5 first focuses on GaAs MESFET drain current I-V models. First, a discussion on the most commonly used drain current models is presented. Then an improved drain current model and its formulation are described in the following section. Model parameters are extracted for various MESFET devices. The performance of the new model is compared with the measured

device response as well as with the modelling results using other available models. The improved current model gives a better accuracy in predicting device compared with several traditional models. After introducing the new drain current model, the remaining section of Chapter 5 focuses on the GaAs MESFET charge model. This part starts with a discussion of the most commonly used gate capacitance models. The model formulation, its advantage and deficiency are explored. The model accuracy is examined with the help of measurement data. Following the discussion of existing models, a new gate charge model is proposed. The new model is very accurate in describing device junction capacitances under various device operating conditions. The performance prediction in the linear region, saturation knee region, sub-threshold region and at V_{ds}=0 is greatly improved over the conventional models. The new expressions and their derivatives are continuous. Moreover, the new model obeys the terminal charge conservation law, which helps to solve the non-convergence problem in simulation. Finally, device measurement data is employed to verify the accuracy of the new gate charge model. The performance of the new model is also compared with other models.

Chapter 6 focuses on the verification of the proposed new models. In this chapter, the simulation and measurement result of a Ku-band MMIC amplifier designed with the new model are presented. In this MMIC design, the new analytical extraction method is employed to obtain the small signal equivalent circuit elements at multi-bias points. The improved nonlinear drain current I-V model and new gate capacitance model are implemented into the circuit simulator. The model evaluation

includes S-parameter analysis, gain compression and harmonic output response. Measurement and simulation results are presented and compared. As a result of the investigation, these new models are found to be very accurate, and can be easily implemented into commercially available circuit simulators.

Chapter 7 is a summary of the work of this thesis. Appendix A provides a detailed description of some existing empirical models. The small signal parameter extraction formulations are presented in Appendix C.

To summarize, new approaches for GaAs MESFETs small-signal modelling are proposed. Also, a new GaAs MESFET empirical model with improved drain I-V characteristic equation and new capacitance-voltage expression is demonstrated. It is hoped that the study will lead to more accurate modelling methodologies for the GaAs MESFET and its MMIC design in the future.

1.4 Original Contributions

The original contributions of this dissertation are summarized as follow:

- For the first time, a novel analytical approach for extracting all the 15 equivalent circuit elements of GaAs MESFET devices has been proposed. This reliable analytical method can eliminate the conventional cold-FET and hot-FET modelling constraints and allow an ease in inline process tracking. The resulting extrinsic small signal parameters are independent of biasing voltage. In contrast to the conventional approaches, no subsidiary circuit such as Cold-FET or Hot-FET has been adopted.

- The conventional lumped models may not be sufficiently accurate at relatively high operating frequencies due to their frequency-independent equivalent circuits. In this dissertation, a creative distributed modelling approach for GaAs MESFET/HBT has been proposed for modern MMIC design. With electromagnetic simulation, this distributed model can precisely describe complex coupling effects in device layouts and predict the electrical characteristics of unconventional device structures for better MMIC performance.

- An empirical approach is employed in our nonlinear modelling due to its

accuracy and simple implementation in circuit simulators. A new empirical large-signal model of GaAs MESFET, based on an improved drain current characteristic and a new gate charge (gate capacitance) model, is proposed in this dissertation.

- An improved empirical model for GaAs MESFET drain current I-V characteristics is formulated. A set of power series functions are introduced in the improved drain current expression for the correlations between modulation parameters α, λ and biasing condition V_{ds} & V_{gs}. The resulting improved current expression gives better performance where compared with existing drain-current models.

- A new gate charge model has been proposed in this study. Terminal charge conservation has been accounted for in the new gate charge model and the model equations and their derivatives are continuous over the entire device operation regions, which helps to solve conventional non-convergence problems in CAD simulation. Compared with other traditional models, its performance prediction in the linear region, saturation knee region and at V_{ds}=0 is greatly improved.

1.5 Publications

Listed below are the publications generated in the course of this research:

1.5.1 Journal Papers

1. B. L. Ooi, Z. Zhong and M. S. Leong, “Analytical Extraction of Extrinsic and Intrinsic FET Parameters,” *IEEE Trans. Microwave Theory Technology*, vol.57, no. 2, pp.254-261, 2009

2. B. L. Ooi, Z. Zhong, Y. Wang, et al, “A Distributed Millimetre-Wave Small-Signal HBT Model Based on Electromagnetic Simulation,” *IEEE Trans. Vehicular Technology*, vol. 57, no. 5, pp.2667-2674, 2008

3. B. L. Ooi , M. S. Leong, Z. Zhong, et al, "An EBG spatial power combiner”, *Microwave and Optical Technology Letters,* vol. 50, no. 6, pp.1534-1536, 2008

4. Z. Zhong and M. S. Leong, “A Novel Consistent Charge Model of GaAs MESFETs for the Design of Ku-band Power Amplifiers,” Submitted to *IEEE Trans. Microwave Theory Technology*, 2010

1.5.2 Conference Papers

1. Z. Zhong and B. L. Ooi, “Distributed Small Signal Modelling for Multi-port GaAs FETs,” *2008 International Symposium on Antenna and Propagation*

(ISAP'08), Taipei, On Oct. 27-30, 2008

2. B. L. Ooi, M. S. Leong, Z. Zhong et al, "An Efficient Algorithm for Analyzing Large Microstrip Structure Using Macro-Basis-Function and Progressive Method", *IEEE Applied Electromagnetics Conference* (AEMC 2007), Kolkata, India, Dec. 19-20, 2007.

Chapter 2

Basic Operation and Device Models

The overall electrical characteristics of the GaAs MESFET are mainly determined by the electrical property of the semiconductor material and the nature of the physical contact to the material. Knowledge of the device physical structure and properties is helpful for both device modelling and microwave circuit design. In the first part of this chapter, a brief description of MESFET operation is presented. It covers the basic construction of the device, the major operating regions, the small signal equivalent circuit, important nonlinear properties, and some second order effects. The second part of this chapter gives an overview of GaAs MESFET models, including the nonlinear and the small signal models. A variety of models have been proposed for the GaAs MESFET. For small signal models, the difference of various models lies in the equivalent circuit topology selection and the way the equivalent circuit parameters are extracted. For nonlinear models, according to how these models are derived, they can be classified into physical model, empirical model, experimental model and the more recently developed black-box model. Various MESFET models have been used by both device and circuit designers. Different applications and designs place different requirements on the model. Therefore, an understanding of the

features of various modelling approaches is helpful for choosing the right model, and constructing new models for different applications.

2.1 Device Description

A cross-section view of a GaAs MESFET is shown in Figure 2.1 [7], which illustrates its basic structure. Three metal electrode contacts are shown to be formed onto a thin semiconductor active channel layer. Source and drain are ohmic contacts, while gate is a Schottky contact. The gate metal forms a Schottky barrier diode, which gives a depletion region between the source and the drain. The gate depletion region and the semi-insulating substrate form the boundary of the conducting channel. A potential applied to the drain causes electrons to flow from the source to the drain. Any potential applied on the gate causes a change in the shape of depletion region, and a subsequent change in current flow.

For microwave operations, the most critical dimension is the “length” of the gate along the carrier path. The shorter the gate length, the higher becomes the signal frequency. If the FET is to handle a large amount of signal current, the gate width must be increased appropriately.

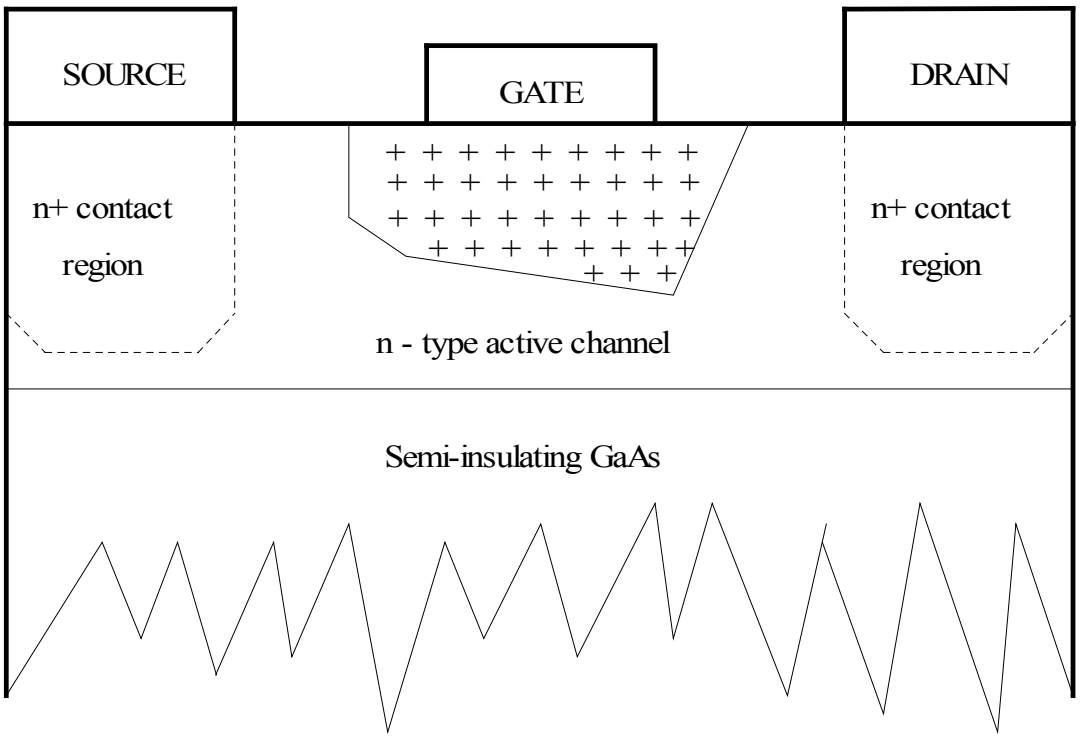


Figure 2.1 Cross-sectional view of a GaAs MESFET

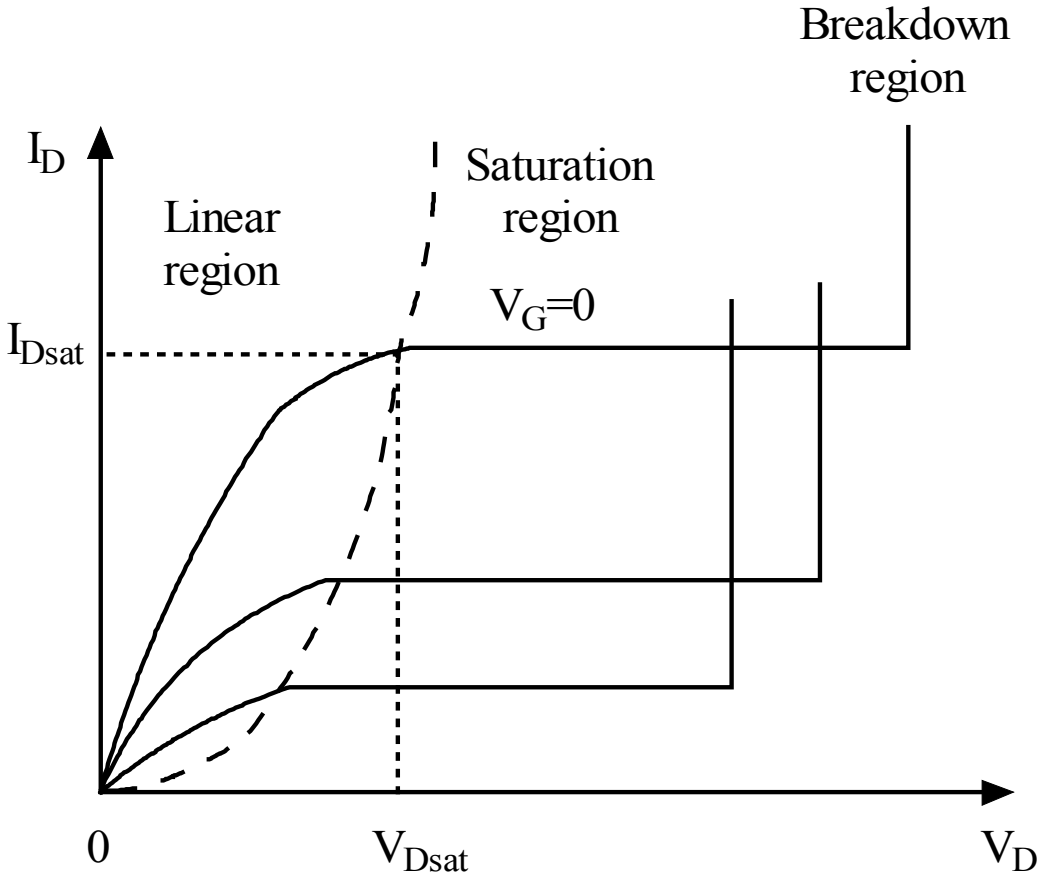


Figure 2.2 Basic current-voltage characteristics of a MESFET

The current-voltage relationships of a MESFET are illustrated in Figure 2.2. The channel current is plotted as a function of applied drain-source potential for different gate-source voltage levels. Three regions of operation can be identified from the figure. They are the linear region, the saturation region and the breakdown region. In the linear region, current flow is approximately linear with drain voltage. As drain potential increases, the depletion region at the drain end of the gate becomes larger than at the source end. Since the electrical field increases with the drain-source potential, a related increase in electron velocity occurs; this simultaneously makes a linear increasing current through the channel region. Increasing the drain voltage results in the electrons reaching their maximum limiting velocity at the drain end of the gate. At this point, the current no longer increases with increasing drain bias, the device is said to be saturated, and its operation enters saturation region. Finally, when gate and drain bias become very large, the device enters the breakdown region, where the drain current increases sharply.

The Schottky barrier of the gate contact creates a layer beneath the gate that is completely depleted of free charge carriers. No current can flow through this region since there are no free carriers exist in it. Moreover, the existence of the depletion layer reduces the available cross-section area for current flow between the source and drain. The depletion layer penetrates deeper into the active channel when reverse bias is applied to the gate. If the gate is made sufficiently negative, the depletion region will extend across the entire active channel and the conduction channel is closed. This essentially allows no current to flow. The gate potential to accomplish this

phenomenon is known as the pinch-off voltage $V_{pinch-off}$. And at this point, the device operates in pinch-off region.

2.2 Physical Meaning of Small-Signal Equivalent Circuit Elements

Figure 2.3 shows a commonly used MESFET small-signal equivalent circuit topology. This equivalent circuit has served as an accurate small-signal model for virtually all GaAs MESFETs [11]. It has been shown to provide an accurate match to measured S-parameters at least through 25GHz [17], and could be used at higher frequency by adding some parasitic elements in the equivalent circuit. This huge amount of S-parameter data of a single GaAs MESFET can be reduced to a set of 15 frequency-independent variables as shown in this equivalent circuit. Basically, all these 15 unknowns can be divided into two parts:

(i) The intrinsic elements g_m, g_{ds}, C_{gs}, C_{gd} (which includes, in fact, the drain-gate parasitic), C_{ds}, R_i and τ inside of the dashed line box, whose values are function of the bias conditions.

(ii) The extrinsic elements L_g, C_{pg}, R_g, L_s, R_s, R_d, C_{pd} and L_d, which are independent of the biasing conditions.

The same equivalent circuit is shown in Figure 2.4, superimposed on a GaAs MESFET device cross section, indicating the physical origin of each equivalent circuit element. From this figure, it is easy to recognize that each lumped element in the equivalent circuit of a GaAs MESFET is related with a corresponding physical part of the transistor.

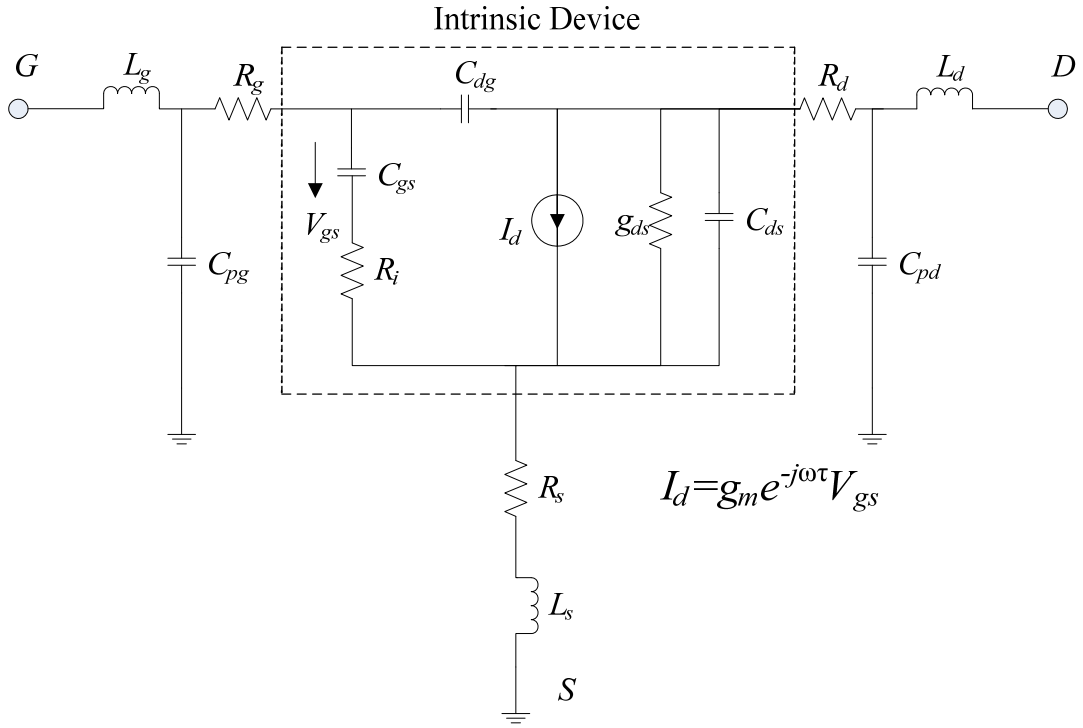


Figure 2.3 Small-signal Equivalent Circuit of a Field Effect Transistor

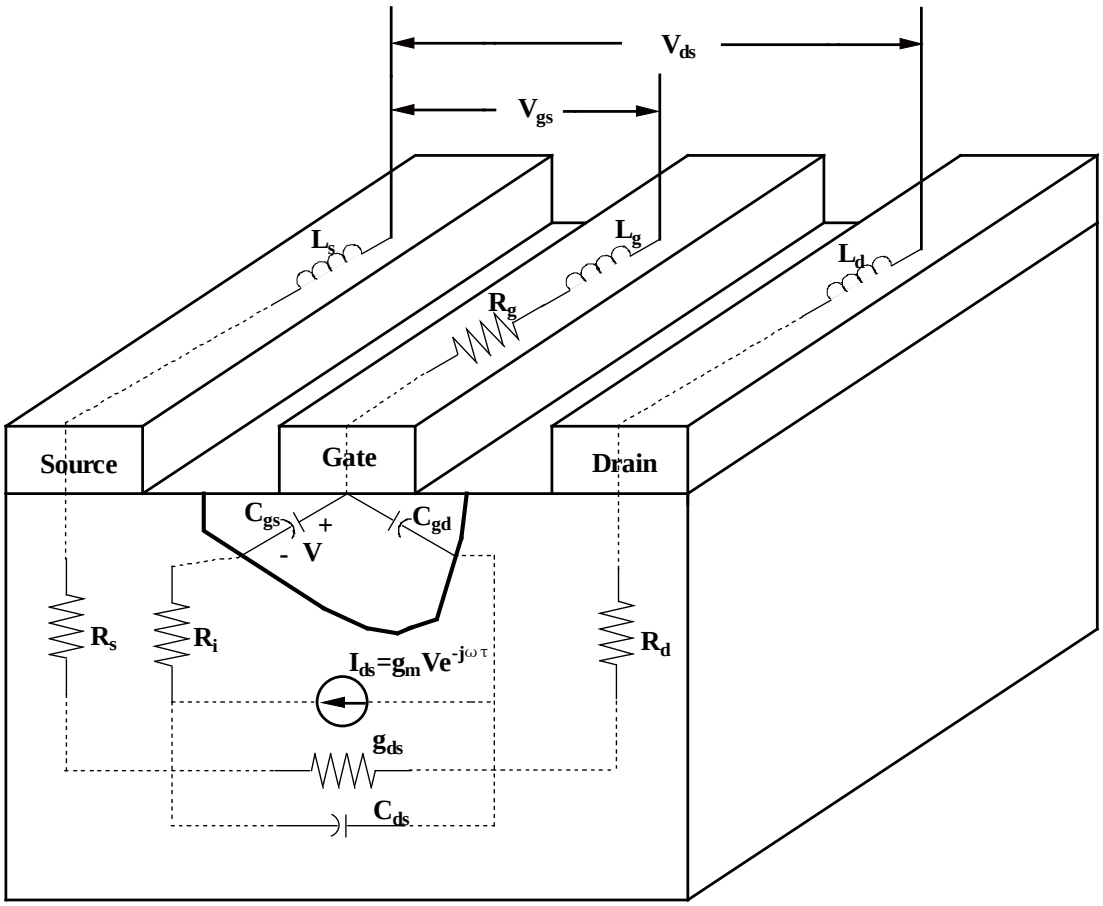


Figure 2.4 Physical origin of the GaAs MESFET small signal model

2.2.1 Parasitic Inductances L_g, L_d and L_s

These parasitic elements are introduced to account for the inductances arising from metal contact pads deposited on the device surface and bonding wires on the package. Parasitic inductances have an important impact on device performance especially at high frequency. They must be accurately characterized. Among L_g, L_d and L_s, gate inductance L_g is usually the largest. The typical values of L_g and L_d are on the order of 10 to 100pH, source inductance L_s is often small, around 10pH for on wafer and chip devices. Bond wire and package will add additional parasitic inductances that in many cases dominate the device parasitics, and they must be accounted for in the circuit model.

2.2.2 Parasitic Resistances R_s, R_d and R_g

Gate resistance R_g physically arises from the metallization resistance of the gate Schottky contact. Resistances R_s and R_d are introduced to represent the contact resistances of drain and source ohm contacts as well as any bulk resistance leading to the active channel. The values of these resistors are on the order of 1Ω [7]. Investigation and measurements show a slight bias dependent behavior of these resistances. However, they are normally considered to be constant in commonly used large-signal models.

2.2.3 Parasitic Capacitances C_{pg} and C_{pd}

Parasitic capacitances arise primarily from metal contact deposited on the device

surface and bonding wires on the package. Like parasitic inductances, parasitic capacitances are related to the device structure. For some devices on wafer, C_{pg} and C_{pd} could be ignored in the low frequency region without introducing significant error to the equivalent circuit due to their small values (on the order of 1pF).

2.2.4 Intrinsic Capacitances C_{gs}, C_{gd} and C_{ds}

The behavior of the depletion region beneath the gate of a MESFET is determined by the bias applied to the device terminals. The variation of the space charge region is caused by both gate-to-source potential and gate-to-drain potential. Gate charge Q_g is considered to be the space charge beneath the gate that varies with gate bias and drain bias. The gate-source capacitance C_{gs} is the derivative of the space charge with respect to the gate-source bias V_{gs}, when the gate-drain voltage is constant:

$$C_{gs} = \left.\frac{\partial Q_g}{\partial V_{gs}}\right|_{V_{gd}=const} . \tag{2.1}$$

The gate-drain capacitance C_{gd} is the derivative of the space charge with respect to the gate-drain bias V_{gd}, when V_{gs} is constant:

$$C_{gd} = \left.\frac{\partial Q_g}{\partial V_{gd}}\right|_{V_{gs}=const} . \tag{2.2}$$

The gate drain capacitance C_{gd} is smaller in magnitude than C_{gs} under normal bias conditions. However, it is critical in accurate S-parameter prediction.

The drain-source capacitance C_{ds} in the equivalent circuit is introduced to model

the geometric capacitance effect between drain and source electrodes.

2.2.5 Transconductance g_m

The incremental change in the output current I_{ds} of a MESFET for a given change in input voltage V_{gs} is measured by the device transconductance g_m. Transconductance g_m provides the intrinsic gain mechanism of the device. Mathematically, it is defined as the derivative of drain current with respect to gate-source biasing voltage:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} . \tag{2.3}$$

The value of transconductance shifts at low frequency, and the frequency at which this shift occurs varies. Both the gate length and the gate width of MESFET affect the transconductance values. The g_m value changes directly with gate width and inversely with gate length.

2.2.6 Output Conductance g_{ds}

The incremental change in output current I_{ds} with the output voltage V_{ds} is measured by the device output conductance gds. Mathematically, the output conductance is defined as the derivative of drain current with respect to the drain-source biasing voltage:

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} . \tag{2.4}$$

Output conductance tends to increase as device gate length decreases. Low frequency dispersion of output conductance is more significant than with the

transconductance. The RF value is of primary concern for small-signal modelling.

2.2.7 Charging Resistance R_i

The charging resistance R_i is of questionable physical meaning, and its value is difficult to extract. It is included in the equivalent circuit mainly to improve the fitting of S_{11}.

2.2.8 Transconductance Delay τ

When gate biasing voltage changes, the drain current I_{ds} needs some time to respond to this change. The transconductance delay τ represents the inherent delay to this process. The physically meaning of the transconductance delay is the time it takes for the charge to redistribute itself after a changing in gate voltage.

2.3 Nonlinear Properties in Large Signal Models

Large signal models are required for circuit simulation that is involved in predicting either large signal or nonlinear performance. In Figure 2.5 a typical equivalent circuit for a MESFET large-signal model is shown. The equivalent circuit is divided into the extrinsic parasitic elements and the intrinsic device. The extrinsic elements include C_{pg}, C_{pd}, L_g, L_d, L_s, R_g, R_d, and R_s, which are independent of biasing conditions. The intrinsic device is enclosed by the dashed-line box. All the nonlinear elements lie within the dashed-line box. The main nonlinear elements include the drain source current I_{ds}, gate capacitances C_{gs} and C_{gd}, as well as diode D_{gs} and D_{gd}.

The drain source current I_{ds} is represented by a voltage controlled current source. The control voltages are V_{gs} and V_{ds}. From I_{ds}, transconductance and output conductance are derived.

Gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} are included to model the behavior of the depletion charge under the gate.

Diode D_{gs} represents the forward-bias gate current, which is important in modelling device breakdown under inverted drain-source bias condition. Diode D_{gd} is included to model drain-gate avalanche current.

Among these nonlinear properties, the most important are the drain source current and the gate capacitances. They are included in most nonlinear GaAs MESFET models.

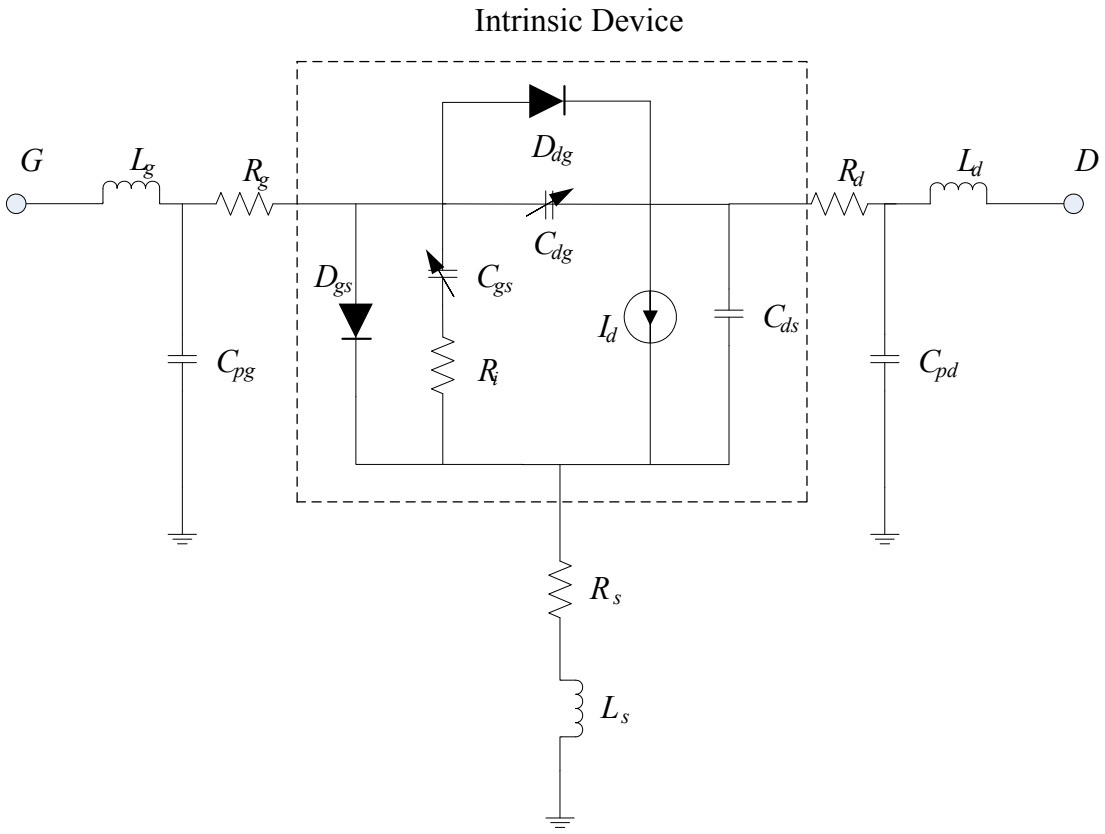


Figure 2.5 An equivalent circuit for MESFET large-signal model

2.4 Second Order Effects

Some of the observed MESFET behavior deviates from the basic principles under particular operating conditions. These are called second-order effects. Of particular importance are the low-frequency dispersion of device transconductance and output conductance, the behavior of the device near pinch-off, namely the sub-threshold effects, and self-heating effects.

2.4.1 Frequency Dispersion

Low-frequency dispersion phenomena in III-V FETs usually arise from the long time constants (from fractions to hundreds of microseconds) associated with deep level traps and surface state densities. The effects of these phenomena have great impact on device electrical characteristics. These effects can be macroscopically observed as causing low-frequency dispersion of the measured drain current characteristics. In terms of the derivatives of current, they cause a discrepancy between the DC and RF characteristics of transconductance and output conductance. Low frequency shifts in output conductance and transconductance values are observed for microwave MESFETs. The shifts in transconductance are typically smaller than shifts in output resistance. As frequency is increased above DC, measured device output resistance can drop by as much as an order of magnitude. The characteristic frequencies at which these decreases occur vary from less than 100Hz to approximately 100KHz. Drops in transconductance values are typically on the order of 5% to 30% of the DC value, and also occur at widely varying frequencies.

2.4.2 Self-heating Effect

Heat is generated in the channel region of the MESFET due to the drain current flow and the resulting power dissipation. Most of the heat is generated under the gate near the drain end since this region sustains most of the V_{ds}, and as a result, most of the power is dissipated here. This self-heating process can cause a temperature difference as great as 100˚C between the channel and the bottom of the chip. As V_{ds} increases, more power is dissipated in the channel, making it even hotter. This leads to a decrease in the effective electron mobility, which in turn causes a decrease in drain current and a negative output conductance. Thermal effects on output conductance are related to the combined degradations of saturation velocity v_s, peak velocity v_p, and low-field carrier mobility μ due to self-heating in the channel region. A significant self-heating effect is often observed in the high power region of the drain current I-V characteristics.

Figure 2.6 shows the measured dc drain current I-V characteristics. The decrease of drain current due to self-heating at high current region can be observed. In Figure 2.7, output conductance as a function of V_{ds} for a 16×125um GaAs MESFET is presented. As observed, under high current operation, the self-heating effect leads to negative output conductance.

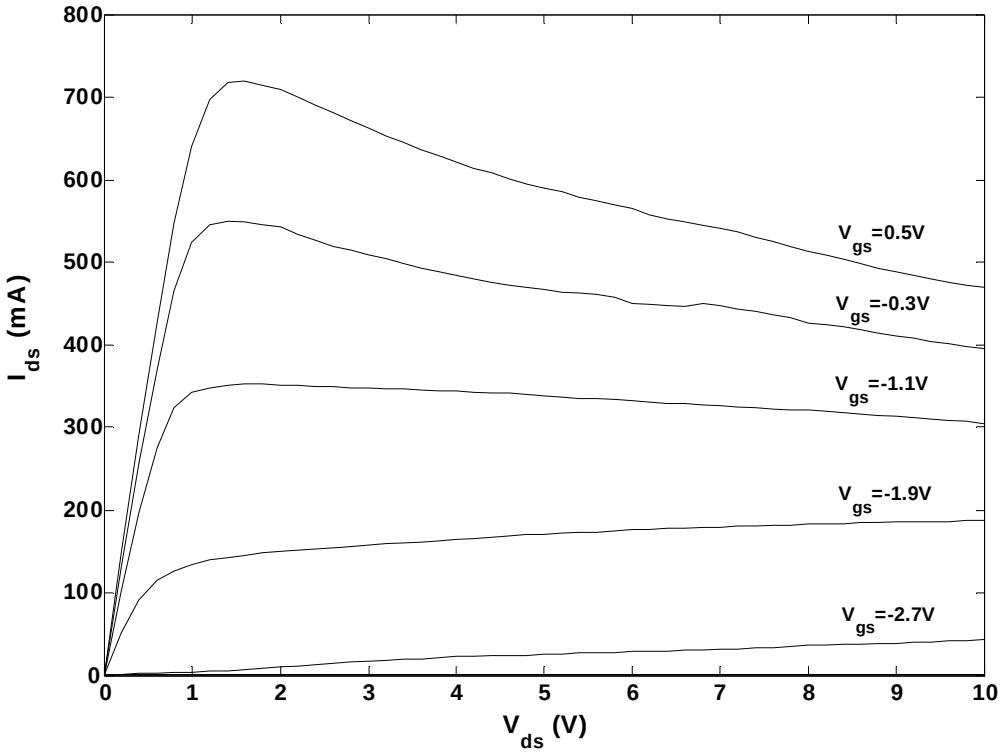


Figure 2.6 Measured DC drain current as a function of V_{ds} for a 16×125um GaAs MESFET, V_{gs}=-2.7V~0.5V.

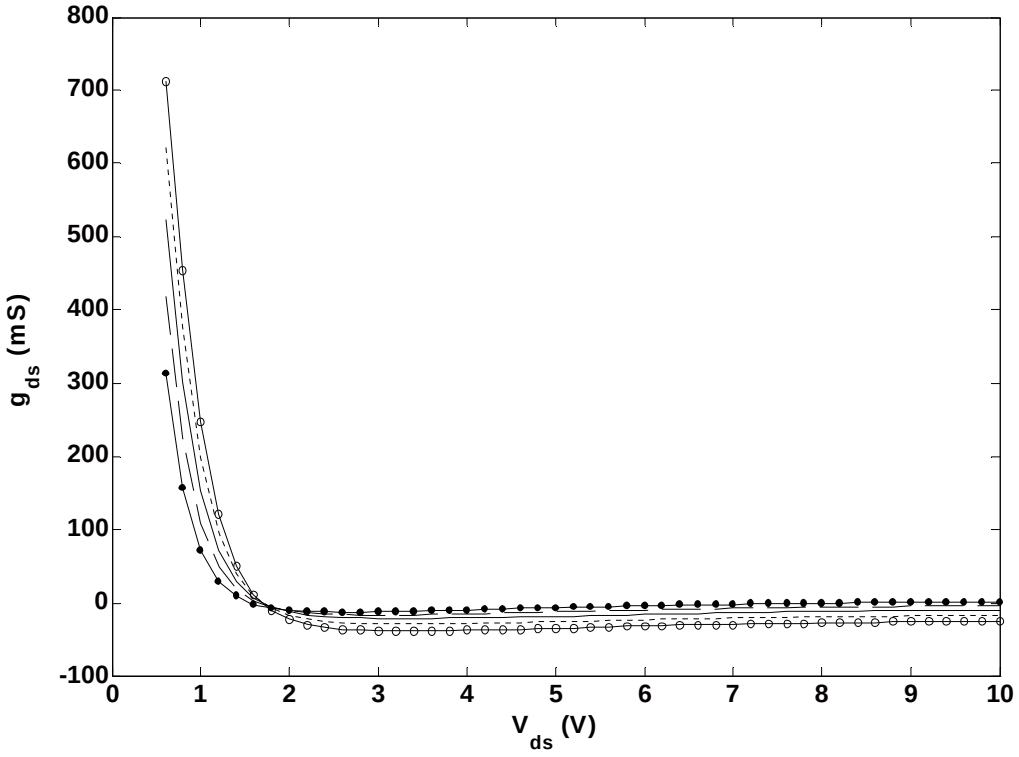


Figure 2.7 Output conductance g_{ds} Vs. V_{ds} for a 16×125um GaAs MESFET, V_{gs}=-1.1V~0.5V

(—•— V_{gs}=-1.1V, —— V_{gs}=-0.7V, ——V_{gs}=-0.3V, -----V_{gs}=0.1V, —o— V_{gs}=0.5V).

2.4.3 Sub-threshold Effect

When a MESFET is biased near pinch-off, the physical phenomena that dominate device performance are different from those that govern device behavior under normal operating conditions. The threshold voltage is defined as the applied gate voltage under which the channel is completely depleted of free carriers. The classical depletion model is derived based on the abrupt depletion approximation. The model assumes that the expulsion of free carriers within the depletion region is total and that the substrate is a perfect insulator. In reality, however, the transition from depleted to neutral region takes place over a few Debye lengths due to the presence of mobile carriers at the depletion boundary. Consequently, when the gate-channel and channel-substrate depletion regions approach each other within this distance, the channel mobile carrier density will decline less rapidly than predicted by the abrupt depletion approximation. Using the abrupt depletion approximation leads to significant underestimation of the channel mobile carrier density, particularly in the sub- and near threshold regions. The noticeable effect of the sub-threshold region is the exponential dependence of the drain current on the gate bias.

Figure 2.8 shows the measured drain current characteristics around pinch-off region, for which $V_{pinch\text{-}off}$ equals to -1.21V. As can be seen from the figure, around pinch-off region, instead of a sudden cutoff, the drain current gradually goes to zero.

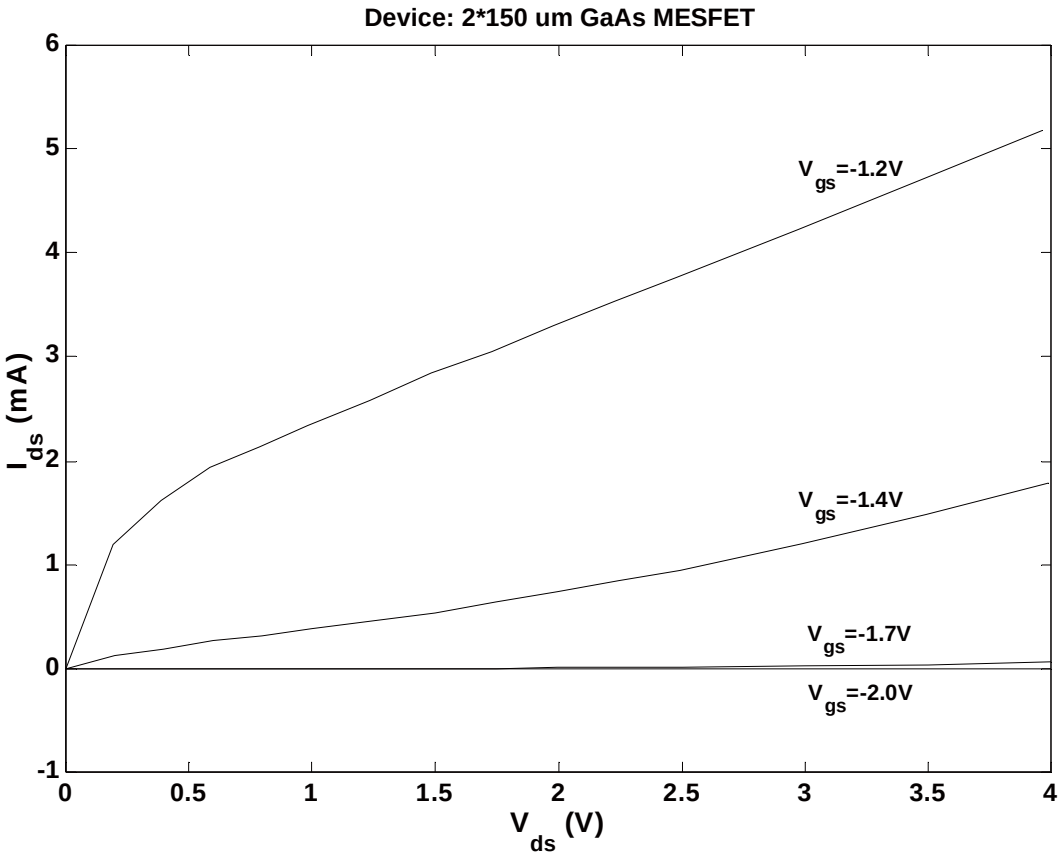


Figure 2.8 Measured drain current characteristics around pinch-off region, $V_{pinchoff}$ = -1.21V.

2.5 Existing Small Signal Modelling Approaches

Determination of the small signal equivalent circuit parameters is the focus of most small signal modelling approaches. Various approaches have been proposed to extract extrinsic and intrinsic elements, most of which are based on the so-called cold-FET and hot-FET measurement techniques. The small signal parameter extraction process can be classified into two categories, the optimization based techniques and directly analytical techniques. Typically, they are combined to yield accurate results. The primary goal of these techniques is to uniquely determine the equivalent circuit elements.

The intrinsic FET topology is such that a Y-parameter analysis of the equivalent

circuit results in relatively simple expressions that can be equated to the measured Y-parameter data. Minasian [8] first described such a technique. FUKUI [9] proposed an approach to estimate the basic device parameters of the GaAs MESFET in 1979, which is still used for the determination of parasitic resistance. Diamant and Laviron [10] suggested in their work, that the S-parameters measured at zero drain bias voltage can be used for evaluating device parasitics because the equivalent circuit is much simpler. Dambrine et al. [11] first combined cold FET and hot FET technique in direct determination of both the extrinsic and intrinsic small-signal parameters. This approach has been quoted by different researchers. In the work of Reynoso-Hernandez et al [12], a technique was proposed to overcome the inconsistencies between DC and RF methods. Later, a reliable RF analytical technique for extracting parasitic elements of FETs was proposed [13]. Some other analytical techniques have been presented in [14-16], [18-21]. Most of the analytical methods mentioned above need additional measurements such as DC or/and RF characterization under various conditions beside S-parameter measurement under normal operating condition.

The most common solution to determine the elements of the small signal equivalent circuit has been through minimizing the difference between measured and computed S-parameters versus frequency. Curtice and Camisa [22] used zero drain bias voltage condition to optimize the device parasitic parameters. Vaitkus [23] has shown that unique values of the circuit elements are difficult to obtain because the final optimized values depend on the starting values. To obtain a unique solution of

the model parameters, additional measurements [22], a partition approach [24], or an automatic decomposition technique [25] have been introduced. But uncertainties still exist with respect to the initial value problem. A new MESFET small-signal model parameter extraction approach based on optimization with multi-plane data fitting and bi-directional search was presented in the work of Lin and Kompa [26], which attempts to solve the local minimum problem and has proved to yield good result.Also, different optimization approaches have been reported to obtain global minimum. Simulated annealing [27] has been used with excellent results for device modelling for global minimum, but it takes a long time for the optimization to complete.

Although much work has been done, the extraction of small signal parameters is still a difficult task, especially the problem of how to uniquely determine equivalent circuit elements, and how to solve the problem of local minimum. Thus, a reliable extraction process needs to be worked out.

2.6 Existing Nonlinear MESFET Models

Extensive researches have been done in the field of GaAs MESFET large signal modelling. Numerous models have been proposed to account for different aspects of device performance. However, modelling of a MESFET device is very complicated, and if the model is to be used in a circuit simulator, additional requirements have to be imposed on the model formulation. As a result, no single model can meet all application requirements. An accurate MESFET model is thus greatly in demand, and the interest in this field will continue to grow.

There are several requirements for a large-signal MESFET model.

(i) It should be accurate for all operating conditions.

(ii) It should accurately describe I-V characteristics and S-parameters as a function of bias and frequency.

(iii) It should observe energy and charge conservation. Also, it should take into account such physical phenomena as trap effects and self-heating. The model itself and model parameters should be mathematically and physically consistent with each other.

(iv) Device static behavior, small-signal behavior, and large-signal behavior predicted by the model should relate to each other with no contradictions. The model formulations and their derivatives should provide a continuous transition to different operation regions, so as to avoid non-convergence problem in circuit simulation especially for designs with increasing complexity.

GaAs MESFET large signal models are usually classified into three categories, namely, physically based model [18, 63-70], empirical model [35-62] and table-based model [28-34]. Some of the physically based models are very simple and cannot describe the volt-ampere and voltage-capacitance characteristics with acceptable accuracy. Other popular physically based models, as the BSIM3v3 model, are too complicated and may not be as accurate for overall bias conditions. Moreover, microwave parasitic effects in GaAs MESFET are not easy physically predictable. Table-based models, such as the HP Root model [17], may only be accurate for the

characterized structures and measurement conditions. An empirical analytical modelling approach is a valid compromise between physical models and data-based models, which has been proven successful in GaAs MMIC development.

Currently, the empirical model is the most preferable approach for microwave circuits design and device nonlinear modelling. As shown in the above references, a variety of analytical models have been developed. The main differences in all these works lie in the empirical equations that describe the DC I-V characteristics and the capacitance-voltage relationships of the device. All of these models are capable of expressing the device I-V and C-V properties with some success. However, they are usually not accurate in certain device operation region. There have been no established models so far, thus, new effort to improve the modelling accuracy is still of great interest.

Chapter 3

Parameter Extraction Technologies for GaAs MESFET Small Signal Model

3.1 Introduction

The small-signal model of GaAs MESFET is extremely important for microwave circuit design. For some circuit designs, the simulation is based on the small-signal model, and for others, small-signal simulation is the starting point. Small-signal models provide a link between measured S-parameters and the electrical processes occurring within the device. Each equivalent circuit element provides a lumped element approximation to some aspect of the device physics. A physically meaningful circuit topology provides an excellent match to the measured S-parameters over a wide frequency range. When equivalent circuit elements are properly extracted, the model is valid beyond the frequency range of measurements, thus providing the possibility of extrapolating device performance to frequencies beyond measurement capabilities of some equipment. Furthermore, accurate small signal modelling is also the basis for accurate large signal and noise modelling.

In this chapter, major issues in small signal equivalent circuit parameter extraction

are discussed and both cold-FET and hot-FET techniques are investigated with conventional small signal parameter extraction methodologies. For most of these traditional small signal modelling methods, the results of some extrinsic parameters vary more or less with different biasing conditions, which would decrease the accuracy of its s-parameter performance. For example, in the Dambrine's model [11], the calculated parasitic capacitor C_{pd} varies with the V_{gs} values under which the cold-FET measurement data is collected. Moreover, for all the traditional methods using Cold-FET method, a very large forward gate current is adopted, which would produce an irreversible damage to the transistor. To solve these problems, a novel analytical extraction method for extrinsic and intrinsic FET parameters is proposed. This analytical method could eliminate the conventional cold-FET and hot-FET modelling constraints and allows an ease in inline process tracking. The resulting extrinsic small signal parameters are independent of biasing voltage. In addition, a better s-parameter agreement can be achieved compared with the conventional methods.

3.2 De-embedding Technique

Figure 3.1 shows a typical GaAs MESFET small-signal equivalent circuit. The equivalent circuit is divided into the extrinsic parasitic elements and the intrinsic device. The extrinsic elements include C_{pg}, C_{pd}, L_g, L_d, L_s, R_g, R_d, and R_s, which are independent of the biasing conditions. The intrinsic device is enclosed by a dashed line box; the intrinsic elements include g_m, g_{ds}, C_{gs}, C_{gd}, C_{ds}, R_i and τ, which are

considered to be bias dependent. The intrinsic device exhibits a PI topology.

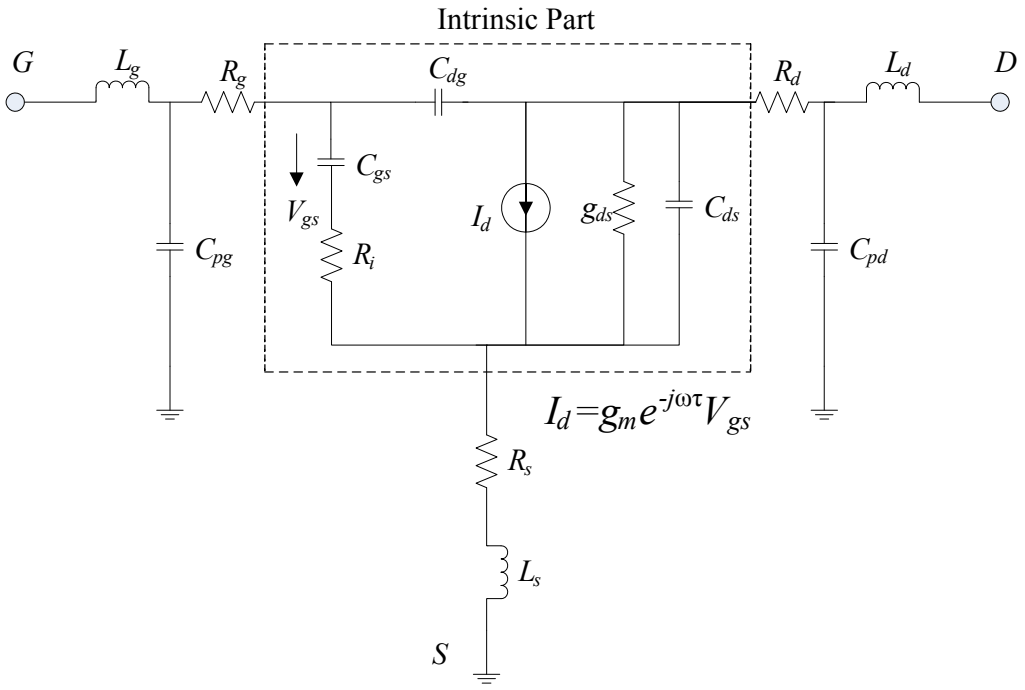


Figure 3.1 GaAs MESFET small-signal equivalent circuit including parasitic elements

As such, it is more convenient to use the admittance (Y) parameters to characterize its electrical properties. Once the values of the parasitic components are known, their effects on the measured device properties can be eliminated by matrix operations. As a result, the intrinsic device Y-parameter (or S-parameter) can be derived afterwards. This process is called de-embedding. After de-embedding, measured device data can be transferred to the inner device. The de-embedding technique is also critical for accurate device measurement. High frequency measurements are always influenced by the parasitic components (chip influences, packaging, testing fixture). This makes the determination of the model parameters for the intrinsic device complicated. It is possible to measure and characterize the

parasitic components of the chip, the package of the transistor, or the test fixture alone. As the GaAs MESFET extrinsic elements are either in series or in parallel with the intrinsic device, the de-embedding of series and parallel parasitic elements forms the basis for this procedure.

3.2.1 De-embedding of Series Parasitics (Z-Matrix)

Figure 3.2 shows the adding of the Z-parameter of the device under test and the parasitic Z-matrices. Both Zpara1 and Zpara2 are the Z-matrices of two parasitic component networks in series connection with the device under test ZDUT. The following relation exists,

$$Z_{total} = Z_{para1} + Z_{DUT} + Z_{para2}. \tag{3.1}$$

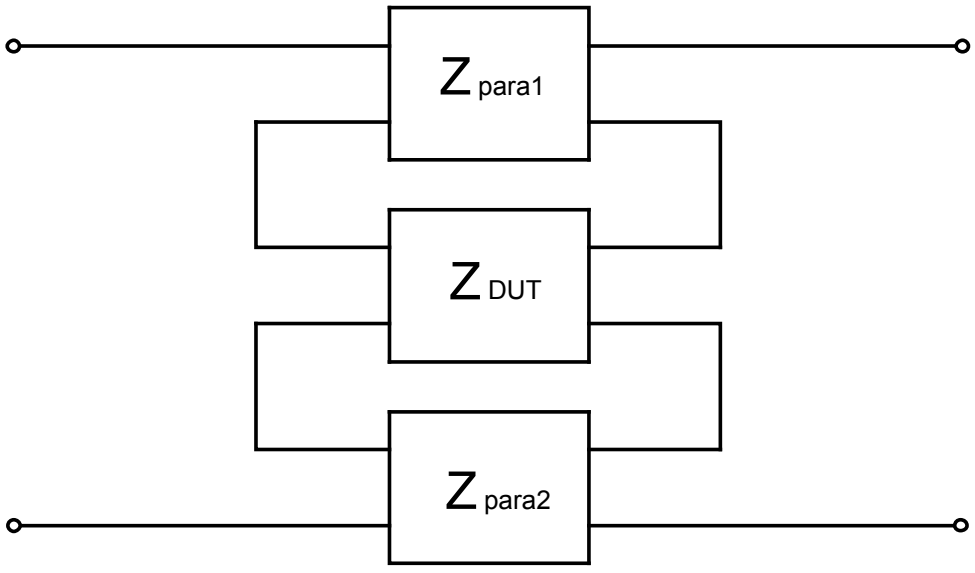


Figure 3.2 Adding of device Z-parameter and the series parasitic elements Z-matrices.

Once the parasitic components Zpara1 and Zpara2 are known, they can be eliminated by subtracting the parasitic Z matrix from the measured data Ztotal. The

de-embedding of series parasitics is expressed as in the following expression:

$$Z_{DUT} = Z_{total} - (Z_{para1} + Z_{para2}) = Z_{total} - Z_{para} . \quad (3.2)$$

3.2.2 De-embedding of Parallel Parasitics (Y-matrix)

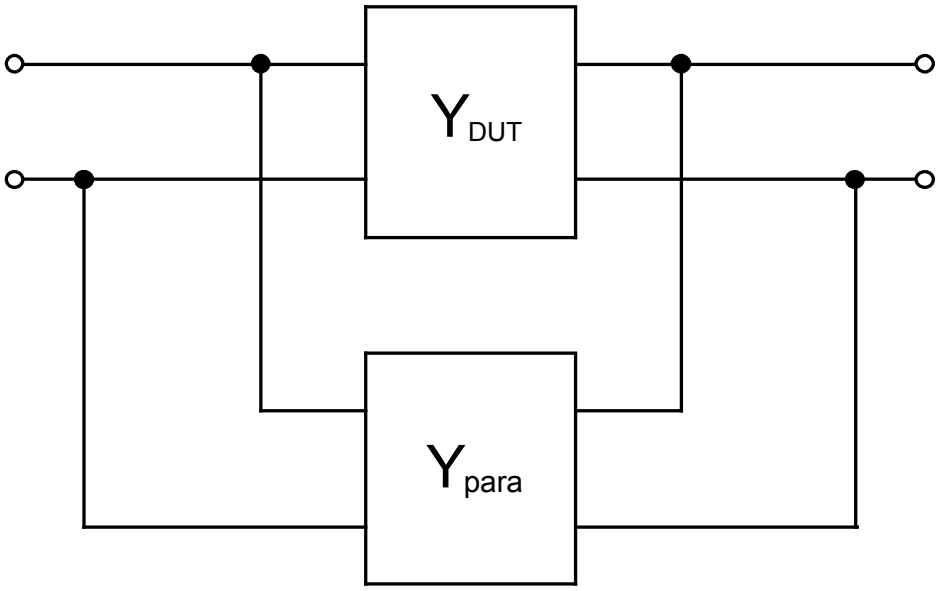


Figure 3.3 Adding of device Y-parameter and the parallel parasitic elements Y-matrices.

Figure 3.3 shows the adding of the Y-parameter of the device under test and the parasitic Y-matrices. Y_{para} is the Y-matrix of the parasitic components network in parallel connection with the device under test YDUT. The following relation exists,

$$Y_{total} = Y_{DUT} + Y_{para} . \quad (3.3)$$

Once the parasitic components are known, they can be eliminated by subtracting the Y matrix Y_{para} from the measured data Y_{total}. The de-embedding of parallel parasitics is expressed as in the following expression:

$$Y_{DUT} = Y_{total} - Y_{para} . \quad (3.4)$$

3.2.3 A Typical De-embedding Procedure for GaAs MESFET Device Parasitics

Figure 3.4 summarizes the parasitic de-embedding method for extracting the intrinsic device Y-parameters. It has the following procedures:

(i) Measure the device S-parameters at the extrinsic plane. The device S-parameter is denoted as S_{total}.

(ii) Transfer device S-parameter S_{total} to Z-parameter Z_{total}, and then, subtract R_g and Rd, This will remove the series parasitic resistor effects, and the resulting Z-parameter is now denoted as Z_1.

(iii) Transfer device Z-parameter Z_1 to Y-parameter Y_1, and then, subtract C_{pg} and C_{pd}. This will remove the parallel parasitic capacitor effects, and the resulting Y-parameter is now denoted as Y_2.

(iv) Transfer Y-parameter Y_2 to Z-parameter, and then, subtract the parasitic resistors R_s and the parasitic inductors L_g, L_d, L_s. This will remove series parasitic component effects, and lead to Z-parameter Z_{in} of the intrinsic device.

(v) Transfer the intrinsic Z-parameter Z_{in} to Y-parameter Y_{in} or S-parameter S_{in} whichever is desirable for intrinsic device description.

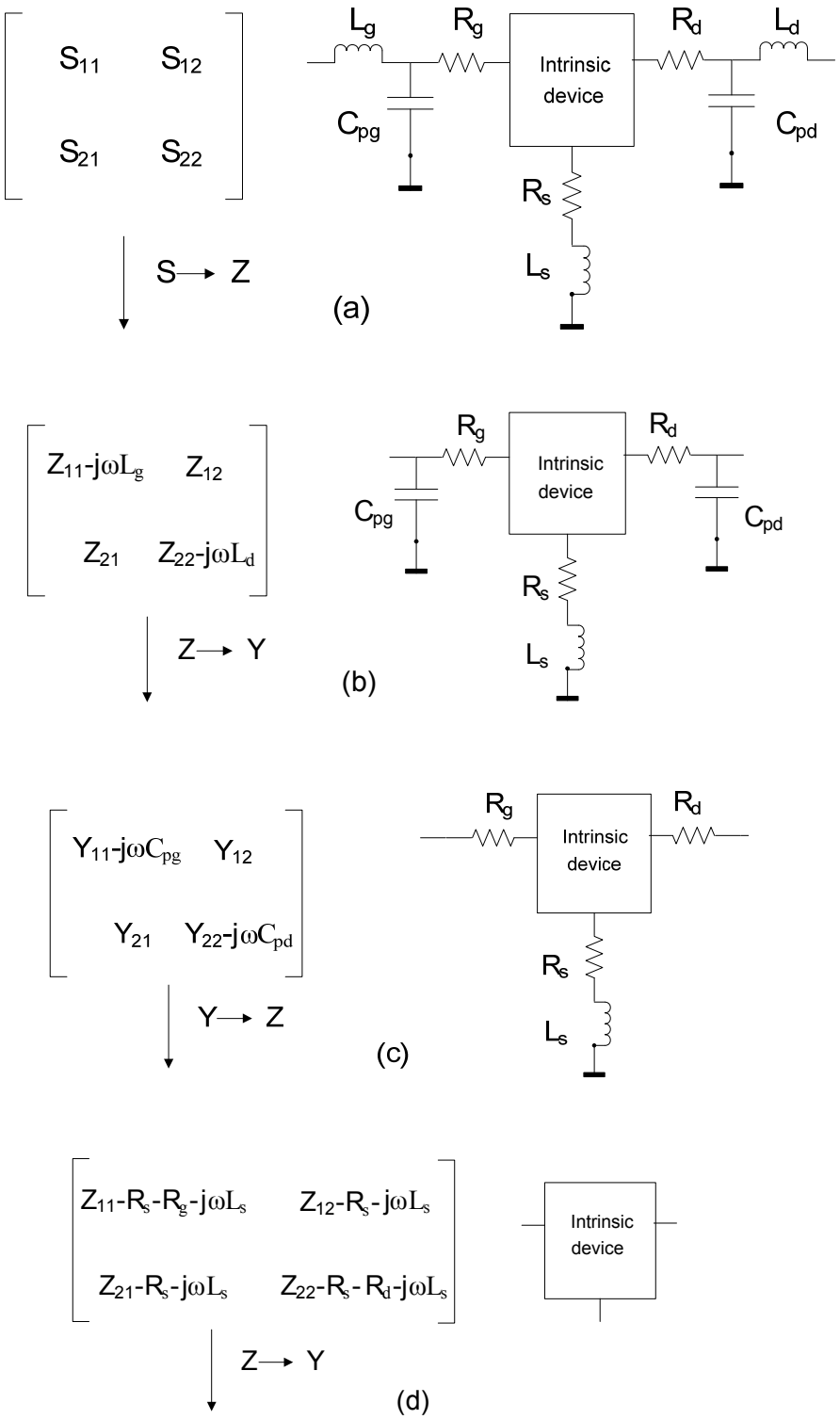


Figure 3.4 De-embedding Method for Extracting the Device Intrinsic *Y* Matrix

3.3 Traditional Method for Parameter Extraction

3.3.1 Cold-FET Techniques

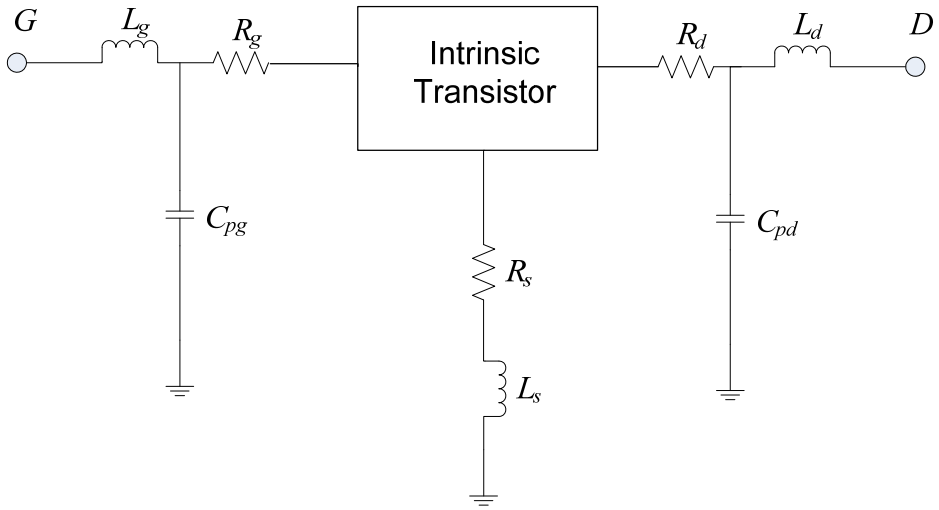


Figure 3.5 Circuit topology of GaAs MESFET with parasitic elements

Figure 3.5 shows the circuit topology of GaAs small signal model which is most frequently used for GaAs MESFET parameter extraction. The extrinsic elements include parasitic resistance R_g, R_d, R_s, parasitic capacitance C_{pg}, C_{pd}, and parasitic inductance L_g, L_d, L_s. Cold-FET techniques determine these parasitic elements from S-parameter data measured at various V_{gs} value, with floating drain condition, i.e. V_{ds}=0.

3.3.1..1 Extraction of Parasitic Resistances and Inductances

Parasitic resistances and inductances are computed from the measurement of S-parameters with DC forward gate bias ($V_{gs}>V_{bi}>0$, Vbi is build-in voltage) and floating drain for different I_{gs} currents. Under forward gate bias ($V_{gs}>V_{bi}>0$) conditions, the equivalent circuit can be shown as in Figure 3.6. The most widely used

model is proposed by Dambrine et al. [11], in which the influence of parasitic capacitances C_{pg} and C_{pd} are neglected. Thus, a simple model is proposed as below.

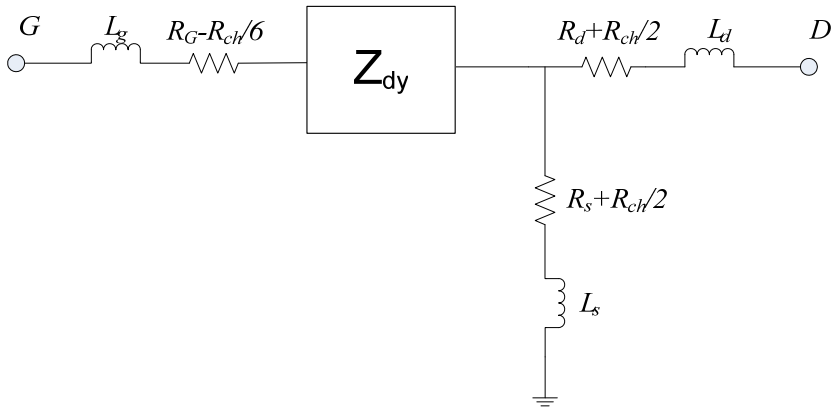


Figure 3.6 Small-signal equivalent circuit with floating drain at $V_{gs}>V_{bi}>0$

$$Z_{11} = R_s + R_g + \frac{R_{ch}}{3} + Z_{dy} + j\omega(L_s + L_g)\,, \tag{3.5}$$

$$Z_{12} = Z_{21} = R_s + \frac{R_{ch}}{2} + j\omega L_s\,, \tag{3.6}$$

$$Z_{22} = R_s + R_d + R_{ch} + j\omega(L_s + L_d)\,. \tag{3.7}$$

where R_{ch} is the channel resistance under the gate and Z_{dy} is the equivalent impedance of the Schottky barrier. Z_{dy} can be written as

$$Z_{dy} = \frac{R_{dy}}{1 + j\omega C_g R_{dy}} \quad \text{with} \quad R_{dy} = \frac{nKT}{qI_g} \tag{3.8}$$

where n is the ideality factor; k is the Boltzmann constant; T is the temperature; C_g is the gate capacitance; and I_g is the DC gate current. As the gate current increases, R_{dy} decrease and C_g increases but the exponential behavior of R_{dy} versus V_{gs} is the dominant factor; consequently the term $R_{dy}C_g\omega$ tends to zero for gate current densities close to 5×10^7-10^8 A/m^2. Therefore, the real and imaginary parts of the Z-parameter turn to these expressions shown below:

$$\mathrm{Re}(Z_{11}) = R_s + R_g + \frac{R_{ch}}{3} + \frac{n_s kT}{qI_{gs}}, \tag{3.9}$$

$$\mathrm{Re}(Z_{12}) = R_s + \frac{R_{ch}}{2}, \text{ and} \tag{3.10}$$

$$\mathrm{Re}(Z_{22}) = R_s + R_d + R_{ch}. \tag{3.11}$$

$$\mathrm{Im}(Z_{11}) = j\omega(L_s + L_g) \tag{3.12}$$

$$\mathrm{Im}(Z_{12}) = \mathrm{Im}(Z_{21}) = j\omega L_s \tag{3.13}$$

$$\mathrm{Im}(Z_{22}) = j\omega(L_s + L_d) \tag{3.14}$$

In the second approach, the effect of parasitic capacitances C_{pg} and C_{pd} is considered. Therefore, it gives general Z-parameters expressions for GaAs MESFETs under forward gate bias ($V_{gs}>V_{bi}>0$) conditions. The corresponding Z parameters are expressed as follows [12,13].

$$Z_{11}(\omega) = \left\{(R_1 + R_3) + \omega^2 C_{pg}(R_1 + R_3)(L_s - C_{pd}R_3^{\,2})\right\} + j\omega\left\{\left(L_s + L_g\right) - \left[C_{pd}R_3^{\,2} + C_{pg}(R_1 + R_3)^2\right]\right\} \tag{3.15}$$

$$Z_{12}(\omega) = \left\{R_3 + \omega^2 L_s\left[C_{pd}(R_2 + R_3) + C_{pg}(R_1 + R_3)\right]\right\} + j\omega\left\{L_s - R_3\left[C_{pd}\left(R_2 + R_3\right) + C_{pg}(R_1 + R_3)\right]\right\} \tag{3.16}$$

$$Z_{22}(\omega) = \left\{(R_2 + R_3) + \omega^2 C_{pd}(R_2 + R_3)(L_s - C_{pg}R_3^{\,2})\right\} + j\omega\left\{\left(L_s + L_d\right) - \left[C_{pg}R_3^{\,2} + C_{pd}(R_2 + R_3)^2\right]\right\} \tag{3.17}$$

$$R_1 = R_g - \frac{R_{ch}}{6} + \frac{n_s kT}{qI_{gs}} \tag{3.18}$$

$$R_2 = R_d + \frac{R_{ch}}{2} \tag{3.19}$$

$$R_2 = R_s + \frac{R_{ch}}{2} \tag{3.20}$$

Real parts of cold-FET Z-parameters are used to determine the parasitic resistors. At low frequency (f<5GHz), the ω^2 terms in the above equations can be ignored. Thus, $\mathrm{Re}(Z_{ij})$ depends only on the access resistances. This eventually leads to the following expressions which are the same with Dambrine's method.

$$\mathrm{Re}(Z_{11}) = R_s + R_g + \frac{R_{ch}}{3} + \frac{n_s kT}{qI_{gs}}, \tag{3.21}$$

$$\mathrm{Re}(Z_{12}) = R_s + \frac{R_{ch}}{2}, \text{ and} \tag{3.22}$$

$$\mathrm{Re}(Z_{22}) = R_s + R_d + R_{ch}. \tag{3.23}$$

$\mathrm{Re}(Z_{12})$ and $\mathrm{Re}(Z_{22})$ are directly related to R_s, R_d and R_{ch}. For $\mathrm{Re}(Z_{11})$, the extraction of the access resistances is achieved by noting that the plot of $\mathrm{Re}(Z_{11})$ versus $1/I_{gs}$ is a straight line. $\mathrm{Re}(Z_{11})_0$ denotes the intercept point of the plot with y-axis, where the gate current is large enough to break the gate of transistor.

It equals to

$$\mathrm{Re}(Z_{11})_0 = R_s + R_g + \frac{R_{ch}}{3} \tag{3.24}$$

If R_{ch} is ignored, the access resistances are given by

$$R_s = \mathrm{Re}(Z_{12}) \tag{3.25}$$

$$R_d = \mathrm{Re}(Z_{22}) - \mathrm{Re}(Z_{12}), \text{ and} \tag{3.26}$$

$$R_s = \mathrm{Re}(Z_{11})_0 - \mathrm{Re}(Z_{12}). \tag{3.27}$$

Parasitic inductances are calculated using imaginary parts of the cold-FET Z-parameters. They are determined by the following equations.

$$L_s = \frac{\mathrm{Im}(Z_{12})}{\omega} + A_s , \tag{3.28}$$

$$L_d = \frac{\mathrm{Im}(Z_{22}) - \mathrm{Im}(Z_{12})}{\omega} + A_d , \tag{3.29}$$

$$L_g = \frac{\mathrm{Im}(Z_{11}) - \mathrm{Im}(Z_{12})}{\omega} + A_g . \tag{3.30}$$

$$A_s = R_3 \left[C_{pd}(R_2 + R_3) + C_{pg}(R_1 + R_3) \right] \tag{3.31}$$

$$A_d = C_{pd} R_2 (R_2 + R_3) - C_{pg} R_1 R_3 \tag{3.32}$$

$$A_g = C_{pg} R_1 (R_1 + R_3) - C_{pd} R_2 R_3 \tag{3.33}$$

The influence of A_s A_d and A_g are neglected at low frequency (f<5GHz) as the influence of parasitic capacitances C_{pg} and C_{pd} is relatively very small under such low frequency. Therefore, equations 3.28 to 3.30 will also draw the same conclusion shown below with Dambrine's method. The detailed experiment results will be presented next to verify the reasonable approximation.

$$L_s = \frac{\mathrm{Im}(Z_{12})}{\omega}, \tag{3.34}$$

$$L_d = \frac{\mathrm{Im}(Z_{22}) - \mathrm{Im}(Z_{12})}{\omega}, \tag{3.35}$$

$$L_g = \frac{\mathrm{Im}(Z_{11}) - \mathrm{Im}(Z_{12})}{\omega} . \tag{3.36}$$

A 4×50μm TOSHIBA GaAs MESFET device (gate length 0.18μm) is biased at $V_{gs}>V_{bi}$, floating drain condition, the S-parameters are measured and transformed into Z-parameters. The real parts of the Z-parameters as a function of frequency are shown in Figures 3.7. It is noticed from this figure that at frequencies below 5GHz, Re(Zij) is almost constant, its variation with frequency is small. This is as predicted by equations 3.25 to 3.27. At low frequencies, the ω^2 terms in equations 3.15 to 3.17 can

be ignored. Thus, parasitic resistances are computed from Re(Zij) values in this frequency range. Also noted from the figures, when the frequency increases, Re(Zij) become frequency dependent. This is because the ω^2 term in equations 3.22 to 3.24 can no longer be neglected.

The imaginary parts of the Z parameters as a function of frequency are shown in Figures 3.8. It can be seen that the imaginary parts of Z-parameters increase almost linearly with frequency, as predicted by equations 3.34 to 3.36.The plot of Re(Z11) versus $1/I_{gs}$ is shown in Figure 3.9, and as expected by equation 3.25, a straight line is observed.

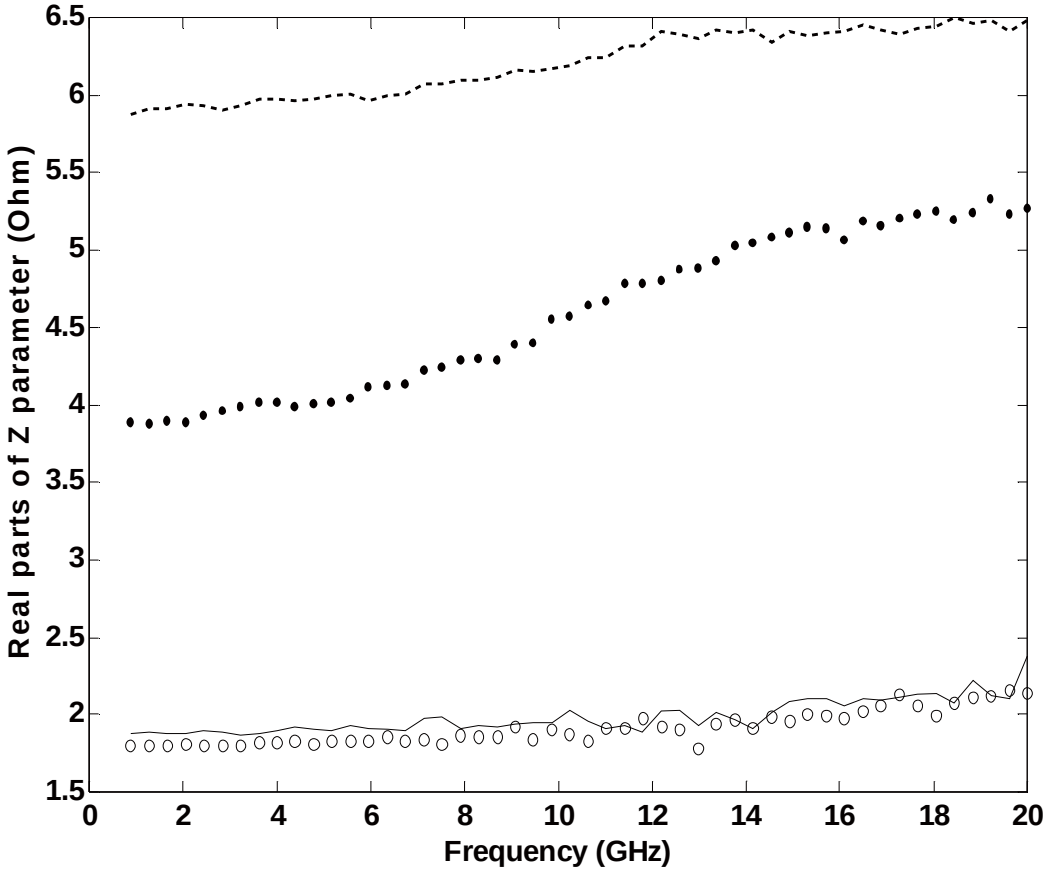


Figure 3.7 Real parts of Z parameters versus frequency, 4×50μm MESFET

($V_{gs}>V_{bi}$, floating drain, ---- Z_{11}, —— Z_{12}, ○○○ Z_{21}, ●●● Z_{22}).

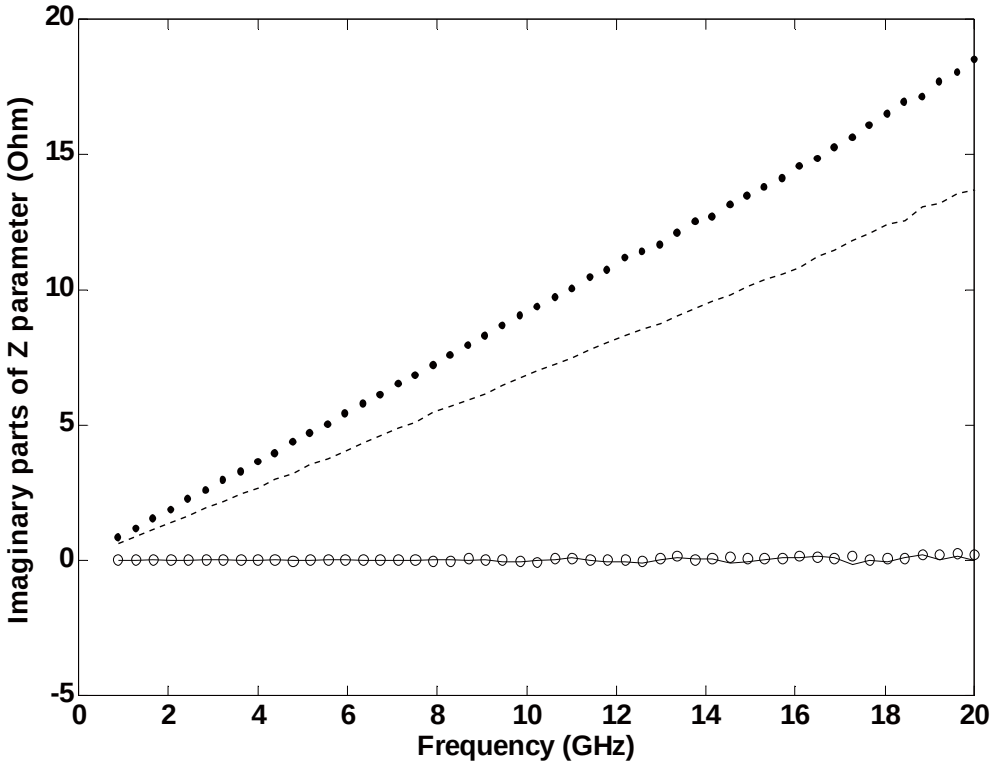


Figure 3.8 Imaginary parts of Z parameters versus frequency, 4×50μm MESFET

(V_{gs}>V_{bi}, floating drain, ---- Z_{11}, —— Z_{12}, ○○○ Z_{21}, ●●● Z_{22}).

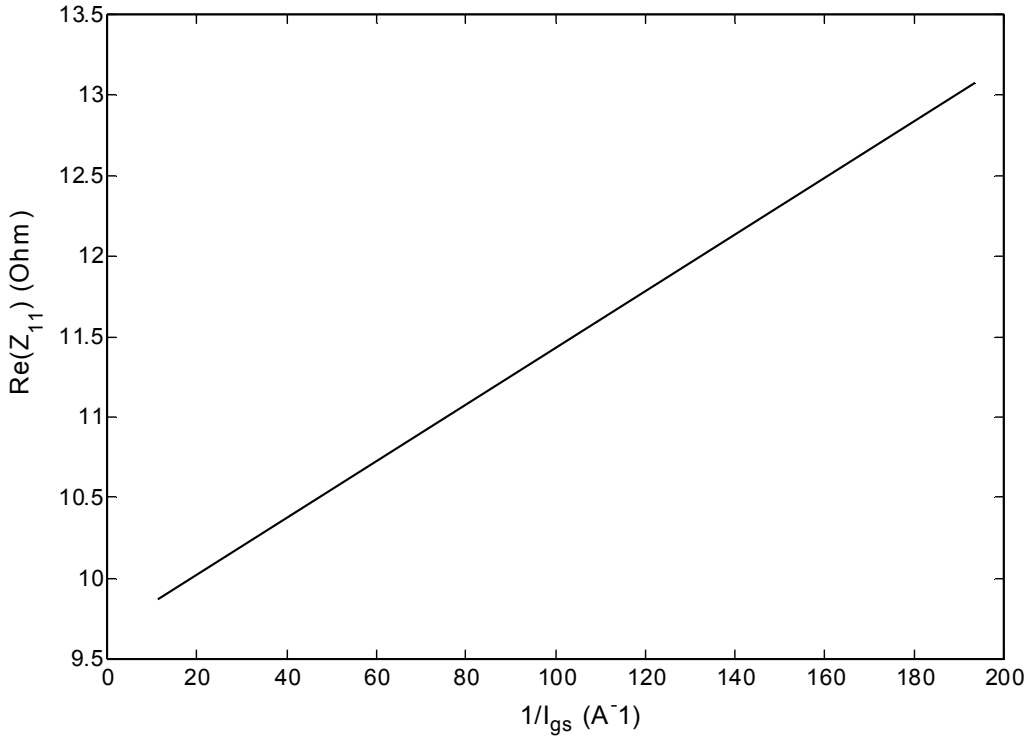


Figure 3.9 Real part of Z_{11} Vs $1/I_{gs}$ for a 4×50um GaAs MESFET

(Vgs>Vbi>0, floating drain).

3.3.1..2 Extraction of Parasitic Capacitances

The input and output C_{pg} and C_{pd} parasitic capacitance are measured by suppressing the conductivity of the channel [11]. As a matter of fact, at zero drain bias and for a gate voltage lower than the pinch-off voltage V_p, the intrinsic gate capacitance (i.e., under the gate) cancels, as does the channel conductance. Under these biasing conditions, the FET equivalent circuit is shown in Figure 3.9.

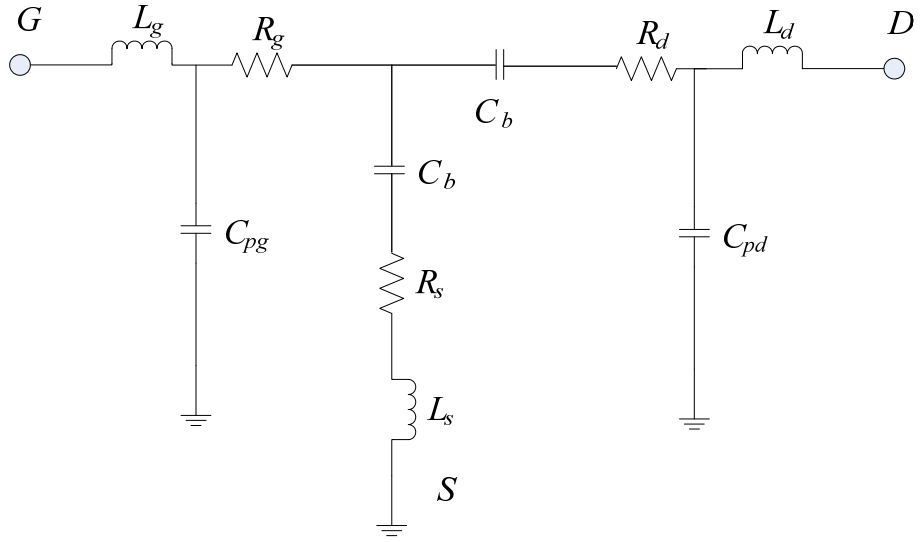


Figure 3.10 Small-signal equivalent circuit of a FET at zero drain bias voltage and gate voltage lower than the pinch-off voltage

In this figure, C_b represents the fringing capacitance due to the depleted layer extension at each side of the gate. For the frequencies up to few giga-hertz, the resistances and inductances have no influence on the imaginary part of the Y parameters, which can be written as

$$\mathrm{Im}(Y_{11}) = j\omega(C_{pg} + 2 \cdot C_b) \tag{3.37}$$

$$\mathrm{Im}(Y_{12}) = \mathrm{Im}(Y_{21}) = -j\omega C_b \tag{3.38}$$

$$\mathrm{Im}(Y_{22}) = j\omega(C_{pd} + C_b) \tag{3.39}$$

Thus, the values of these three unknowns C_b, C_{pg} and C_{pd} can be obtained using equation 3.37 to 3.39.

$$\mathrm{Im}(Y_{11}) = j\omega(C_{pg} + 2 \cdot C_b) \tag{3.40}$$

$$\mathrm{Im}(Y_{12}) = \mathrm{Im}(Y_{21}) = -j\omega C_b \tag{3.41}$$

$$\mathrm{Im}(Y_{22}) = j\omega(C_{pd} + C_b) \tag{3.42}$$

A 2×150 μm and a 2×100μm GaAs MESFET device, are biased at $V_{gs}<V_p$, $V_{ds}=0$, the S-parameters were measured and transformed into Y-parameters. The imaginary parts of the Y-parameters as a function of frequency are shown in Figures 3.11 and 3.12 respectively.

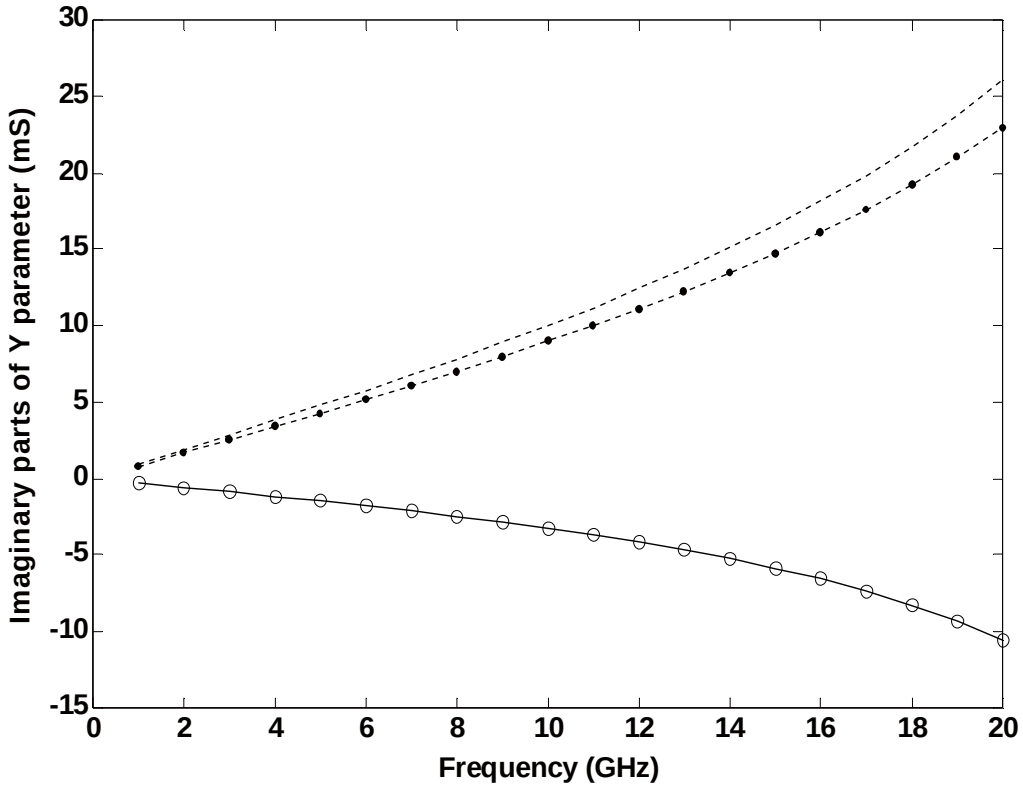


Figure 3.11 Imaginary parts of Y parameters against frequency. Measured at $V_{ds}=0$, V_{gs}=-5.0V<V_p, 2×150μm GaAs MESFET (---- Y_{11}, —— Y_{12}, ○○○ Y_{21}, --●-- Y_{22}).

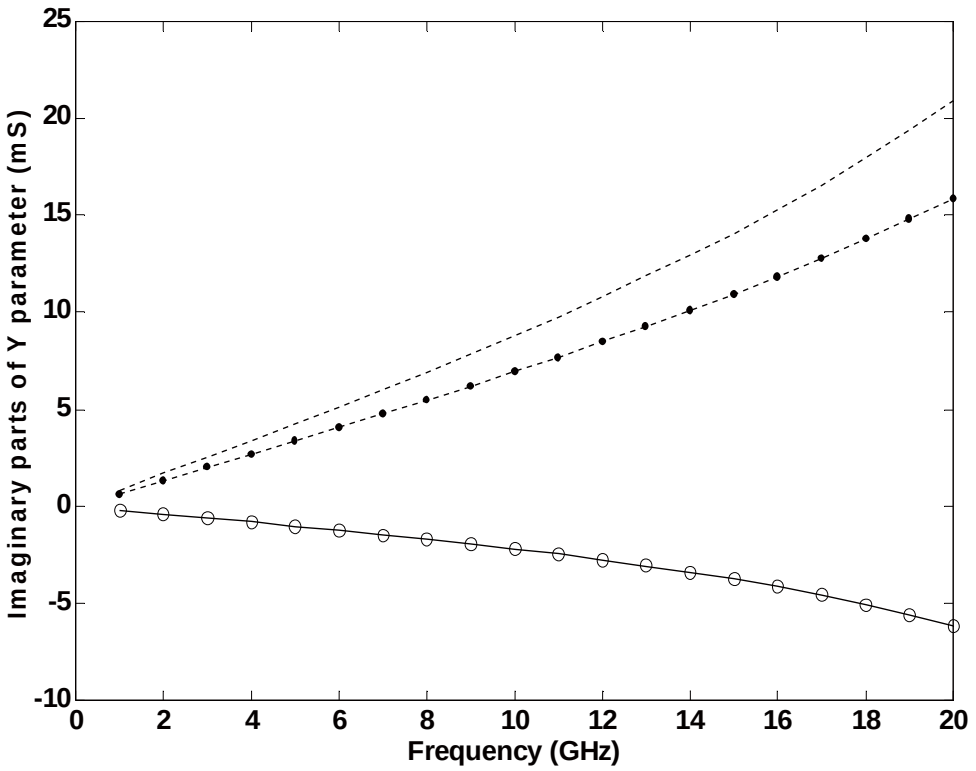


Figure 3.12 Imaginary parts of Y parameters against frequency. Measured at V_{ds}=0, V_{gs}=-5.0V<V_p, 2×100 μm GaAs MESFET(---- Y_{11}, —— Y_{12}, ○○○ Y_{21}, --●-- Y_{22}).

As shown in these two figures above, for both devices, at low frequencies (below 10GHz), the imaginary parts of the Y parameters increase linearly versus frequency. This is in good agreement with the assumption that at low frequencies (below 10GHz), the influence of parasitic resistances and inductances on Im(Y_{ij}) can be neglected, and the imaginary parts of Y parameters only depend on the parasitic capacitances.

3.3.2 Hot-FET Techniques and Optimization Method

The intrinsic elements of MESFET equivalent circuit are usually determined from Hot-FET (V_{ds}>0) S-parameter measurement data after the de-embedding of extrinsic elements. Two intrinsic elements extraction approaches based on hot-FET techniques are most commonly used. They are analytical and optimization methods.

3.3.2..1 Analytical Method

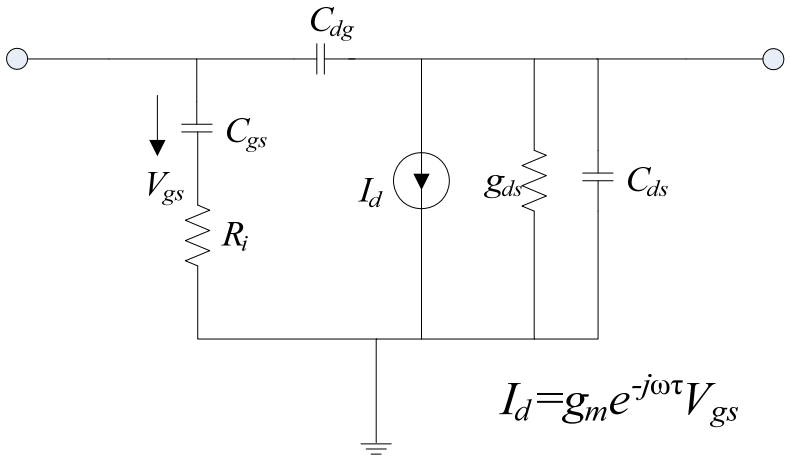


Figure 3.13 The small-signal equivalent circuit for intrinsic device of GaAs MESFET

In the analytical method, the intrinsic elements are directly derived from the intrinsic Y-parameters. Figure 3.13 shows the small signal equivalent circuit for the intrinsic device of GaAs MESFET. From this equivalent circuit topology, the intrinsic device Y-parameter matrix has the following expression:

$$Y_{\text{int}} = \begin{bmatrix} \dfrac{sC_{gs}}{1+sC_{gs}R_i} + sC_{dg} & -sC_{dg} \\ \dfrac{g_m e^{-s\tau}}{1+sC_{gs}R_i} - sC_{dg} & g_{ds} + s(C_{dg} + C_{ds}) \end{bmatrix} \tag{3.43}$$

Separating the Y-matrix into their real and imaginary parts, the elements of the small-signal equivalent circuit can be determined analytically as follows:

$$C_{gd} = -\frac{\text{Im}(Y_{12})}{\omega} \tag{3.44}$$

$$C_{gs} = -\frac{\text{Im}(Y_{11}) - \omega C_{gd}}{\omega}\left(1 + \frac{\left(\text{Re}(Y_{11})\right)^2}{\left(\text{Im}(Y_{11}) - \omega C_{gd}\right)^2}\right) \tag{3.45}$$

$$R_i = \frac{\mathrm{Re}(Y_{11})}{\left(\mathrm{Im}(Y_{11}) - \omega C_{gd}\right)^2 + \left(\mathrm{Re}(Y_{11})\right)^2} \tag{3.46}$$

$$g_m = \sqrt{\left(\left(\mathrm{Re}(Y_{21})\right)^2 + \left(\mathrm{Im}(Y_{21}) + \omega C_{gd}\right)^2\right)\left(1 + \omega^2 C_{gs}^2 R_i^2\right)} \tag{3.47}$$

$$\tau = \frac{1}{\omega}\arcsin\left(\frac{-\omega C_{gd} - \mathrm{Im}(Y_{21}) - \omega C_{gs} R_i \,\mathrm{Re}(Y_{21})}{g_m}\right) \tag{3.48}$$

$$C_{ds} = \frac{\mathrm{Im}(Y_{22}) - \omega C_{gd}}{\omega} \tag{3.49}$$

$$g_{ds} = \mathrm{Re}(Y_{22}) \tag{3.50}$$

3.3.2..2 Optimization Method

The determination of MESFET equivalent circuit elements with optimization based approach is traditionally carried out by minimizing the error function in a way that all elements are changed simultaneously and independently by the optimization engine until the min. of the error function is reached. As a physically based MESFET equivalent circuit model usually consists of a large number of elements (normally>12), the optimization may be easily trapped into a local minimum which is a fundamental problem in optimization procedures. Lots of work has been done to solve this problem. Some approaches focus on the mathematical separation of variables, dividing the optimization into several steps. During each step, only some of the elements are changed by the optimizer to match the measured data. Other approaches focus on reducing the number of optimization variables, for example, using the cold-FET method to determine the initial values of extrinsic parasitic elements.

3.4 A novel analytical extraction method for extrinsic and intrinsic GaAs MESFET parameters

3.4.1 Introduction

The small signal FET equivalent circuit plays a pivotal role in the accurate characterization and development of the FET large-signal model and can provide great insight into the physical matching of the active device. Therefore, great emphasis has in recent past been placed in the small-signal equivalent circuit parameters extraction [9-26, 71-87]. Numerous techniques of small signal extraction methods have been proposed in the literature. These methods include the direct extraction method [11], [20], the optimization method or the combined technique of both the direct and optimization method [62, 71-85].

Of these methods, the Dambrine model [11] or the improved model by Berroth [20] has become the de-facto standard for the extraction of parasitic inductances, resistances and capacitances, and it seems to have been widely used irrespective of the type of equivalent circuits being adopted. These conventional methods can bring permanent damage to the transistor as the result of a very large forward gate current. In addition, for these traditional small signal modelling methods, the results of some extrinsic parameters vary more or less with different biasing conditions, which would decrease the accuracy of its s-parameter performance. In Dambrine model, the parasitic capacitances have to be extracted from the linear combination of the Y-parameters under Cold-FET modelling, i.e. V_{ds}=0V, V_{gs}<V_{pinch}, whereas the

parasitic inductances and resistances have to be extracted from the Z-parameters under Hot-FET modelling, i.e. V_{ds}=0V, V_{gs}>V_{pinch}. Shown in these extensive procedures as in [72], it is well noted that unreliable C_{pg} and C_{pd} values could be obtained after applying the Dambrine's [11] and White's model [71]. In this section, a novel analytical extraction is presented with better s-parameter performance. The exact equation can easily achieve inline process-tracking rather than approximate solution, as used in the Dambrine model. The analytical method is a more reliable and consistent model that fully removes the required constraints as imposed above and the need of optimization in the eventual extraction procedures.

3.4.2 Novel analytical method

The intrinsic part of a FET is indicated by the dashed box as shown in Figure 3.1 and is usually characterized by the Y-parameters below, in which τ is the transconductance delay.

$$Y_{\text{int}} = \begin{bmatrix} \dfrac{sC_{gs}}{1+sC_{gs}R_i} + sC_{dg} & -sC_{dg} \\ \dfrac{g_m e^{-s\tau}}{1+sC_{gs}R_i} - sC_{dg} & g_{ds} + s(C_{dg} + C_{ds}) \end{bmatrix}. \tag{3.51}$$

The extrinsic parameters are closely related to the intrinsic parameters through

$$Z_{total} = L_{ext} + \left(Y_{pad} + \left(R_{ext} + Y_{\text{int}}^{-1} \right)^{-1} \right)^{-1}, \tag{3.52}$$

Where

$$R_{ext} = \begin{bmatrix} R_g + R_s + sL_s & R_s + sL_s \\ R_s + sL_s & R_d + R_s + sL_s \end{bmatrix}, \tag{3.53}$$

$$L_{ext} = \begin{bmatrix} sL_g & 0 \\ 0 & sL_d \end{bmatrix}, \tag{3.54}$$

and

$$Y_{pad} = \begin{bmatrix} sC_{pg} & 0 \\ 0 & sC_{pd} \end{bmatrix}. \tag{3.55}$$

To demonstrate our proposed approach, matrix manipulation coupled with total and conventional least squares method will be adopted in the subsequent explanation. In general, a brute force least squares arrangement of equation 3.52 will usually lead to an ill-posed problem, resulting in wrong extraction values for all the extrinsic and intrinsic parameters. However, if a simple re-arrangement of equation 3.52 is first performed, the influence of the extrinsic inductances can be made more dominant and eventually, leading to more accurate extrinsic inductances extraction values.

$$\left(Z_{total} - L_{ext}\right)\left(Y_{pad} + Y_{\text{int}}\left(R_{ext}Y_{\text{int}} + I\right)^{-1}\right) - I = 0$$

$$\Rightarrow Z_{total} = \left(R_{ext} + L_{ext} - Z_{total}\left(Y_{pad}R_{ext} + I\right)\right)Y_{\text{int}}Y_{pad}^{-1} + \left(L_{ext}Y_{pad}R_{ext}Y_{\text{int}} + I\right)Y_{pad}^{-1} + L_{ext} \tag{3.56}$$

From the second column of equation 3.56, we have

$$Z_{12}^{total} = \frac{-Z_{11}^{total}\left(a_5 s^2 + a_6 s - a_7\right) + a_8 s^3 + a_9 s^2 - a_{10} s + {a_{11}}/{s} + a_{12}}{a_1 s^2 + a_2 s + {a_3}/{s} + a_4 + 1}, \tag{3.57}$$

$$Z_{22}^{total} = \frac{-Z_{22}^{total}\left(a_5 s^2 + a_6 s - a_7\right) + a_{13} s^3 + a_{14} s^2 - a_{15} s + {a_{16}}/{s} + a_{17}}{a_1 s^2 + a_2 s + {a_3}/{s} + a_4 + 1} \tag{3.58}$$

where

$$a_1 = C_{ds}L_s, \tag{3.59}$$

$$a_2 = g_{ds}L_s + C_{dg}R_d + C_{ds}(R_d + R_s)\,, \tag{3.60}$$

$$a_3 = \frac{g_{ds}}{C_{pd}}\,, \tag{3.61}$$

$$a_4 = \frac{1}{C_{pd}}(C_{dg} + C_{ds} + C_{pd}g_{ds}(R_d + R_s))\,, \tag{3.62}$$

$$a_5 = \frac{C_{pg}C_{ds}L_s}{C_{pd}}\,, \tag{3.63}$$

$$a_6 = \frac{C_{pg}}{C_{pd}}(g_{ds}L_s - C_{dg}R_g + C_{ds}R_s)\,, \tag{3.64}$$

$$a_7 = \frac{1}{C_{pd}}(C_{dg} - C_{pg}g_{ds}R_s)\,, \tag{3.65}$$

$$a_8 = \frac{C_{pg}}{C_{pd}}C_{ds}L_gL_s\,, \tag{3.66}$$

$$a_9 = L_g a_6\,, \tag{3.67}$$

$$a_{10} = L_g a_7 - \frac{a_5}{C_{pg}}\,, \tag{3.68}$$

$$a_{11} = a_3 R_s\,, \tag{3.69}$$

$$a_{12} = \frac{a_6}{C_{pg}}\,, \tag{3.70}$$

$$a_{13} = L_d a_1\,, \tag{3.71}$$

$$a_{14} = L_d a_2\,, \tag{3.72}$$

$$a_{15} = a_4 L_d + L_d + \frac{a_5}{C_{pg}}\,, \tag{3.73}$$

$$a_{16} = \frac{1}{C_{pd}} + a_3(R_d + R_s), \tag{3.74}$$

$$a_{17} = \frac{a_2}{C_{pd}} + a_3 L_d . \tag{3.75}$$

Re-arranging the real and imaginary terms of equation 3.57 into matrix form, we achieve

$$[A][K]^{-1}[K][x] = [\overline{A}][X] = [B], \tag{3.76}$$

where the normalized unknowns $[X] = [K][x]$, $Y_o = 1/Z_o = 0.02$, $\omega_o = 2\pi f_{\max}$, $f_{\max}$ is the maximum frequency point,

$$[x]^T = [a_{12} \quad a_{10} \quad a_9 \quad a_8 \quad a_7 \quad a_6 \quad a_5 \quad a_4 \quad a_3 \quad a_2 \quad a_1 \quad a_{11}], \tag{3.77}$$

$$[K] = \text{diag}\left[Y_o \quad Y_o\omega_o \quad Y_o\omega_o^2 \quad Y_o\omega_o^3 \quad 1 \quad \omega_o \quad \omega_o^2 \quad 1 \quad \frac{Y_o}{\omega_o} \quad \omega_o \quad \omega_o^2 \quad \frac{1}{\omega_o} \right] \tag{3.78}$$

The k_{th}-element of the real and imaginary matrix elements of $[\overline{A}]$ and $[B]$ are respectively given as

$$[\overline{A}_k] = [\overline{A}_{11,k} \quad \overline{A}_{12,k}], \tag{3.79}$$

$$[B_k] = \begin{bmatrix} Z_{12r,k}^{total} \\ Z_{12i,k}^{total} \end{bmatrix}, \tag{3.80}$$

where subscript r and i denote respectively the real and imaginary term, N is the maximum number of frequency points, the normalized frequency, $\hat{f}_k = f_k / f_{\max}$, for $k = 1, 2, ...N$,

$$[\overline{A}_{11,k}] = \begin{bmatrix} Z_o & 0 & -Z_o\hat{f}_k^2 & 0 & Z_{11r,k}^{total} & Z_{11i,k}^{total}\hat{f}_k \\ 0 & Z_o\hat{f}_k & 0 & -Z_o\hat{f}_k^3 & Z_{11i,k}^{total} & -Z_{11r,k}^{total}\hat{f}_k \end{bmatrix}, \tag{3.81}$$

$$\left[\overline{A}_{12,k}\right]=\begin{bmatrix} Z_{11r,k}^{total}\hat{f}_k^2 & -Z_{12r,k}^{total} & \dfrac{-Z_o Z_{12i,k}^{total}}{\hat{f}_k} & Z_{12i,k}^{total}\hat{f}_k & Z_{12r,k}^{total}\hat{f}_k^2 & 0 \\ Z_{11i,k}^{total}\hat{f}_k^2 & -Z_{12i,k}^{total} & \dfrac{Z_o Z_{12r,k}^{total}}{\hat{f}_k} & -Z_{12r,k}^{total}\hat{f}_k & Z_{12i,k}^{total}\hat{f}_k^2 & \dfrac{-1}{\hat{f}_k} \end{bmatrix} \tag{3.82}$$

In general, the measured Z-parameters are often contaminated with measurement noise. To alleviate the effect of this noise, a total least squares method [85] will be adopted to solve equation (3.79). The total least squares method is simply performed by first augmenting equation (3.79) into $\left[\overline{A};-B\right]$ and followed by a singular value decomposition on the resultant matrix, i.e. in Matlab® notation, $\left[u,\sigma,v\right]=svd\left(\left[\overline{A};-B\right]\right)$. The unknown solution $\left[X\right]$ is then subsequently assigned with the values of the last column of v divided by the last element of v, i.e. in Matlab notation,

$$\left[X\right]=v(1:\text{end}-1,\text{end})/v(\text{end},\text{end}). \tag{3.83}$$

To improve the condition number of $\left[\overline{A};-B\right]$, a row pivot coupled with a scaling is first performed before the singular value decomposition. The scaling involves dividing each column of the augmented matrix with the square root of the sum of the square of the column elements. Using equation (3.83), both L_g and R_s can be evaluated in terms of the elements of $\left[X\right]$ from

$$L_g=\frac{Z_o X_4}{\omega_o X_7}, \tag{3.84}$$

$$R_s=\frac{X_{12}}{Z_o X_9}, \tag{3.85}$$

Similarly, following the same approach as above, equation (3.58) can be recast

into the same form as in equation (3.76) with the new unknown being

$$\left[x\right]^T = \left[a_{17} \quad a_{15} \quad a_{14} \quad a_{13} \quad a_7 \quad a_6 \quad a_5 \quad a_4 \quad a_3 \quad a_2 \quad a_1 \quad a_{16}\right], \tag{3.86}$$

$$\left[K\right] = \text{diag}\left[Y_o \quad \omega_o Y_o^{\,2} \quad \omega_o^{\,2} Y_o^{\,2} \quad \omega_o^{\,3} Y_o \quad Y_o \quad \omega_o Y_o \quad \omega_o^{\,2} Y_o \quad 1 \quad \frac{Y_o}{\omega_o} \quad \omega_o Y_o \quad \omega_o^{\,2} \quad \frac{Y_o^{\,2}}{\omega_o} \right] \tag{3.87}$$

And the k_{th} element of the real and imaginary matrix elements of the new $\left[\overline{A}\right]$ and $\left[B\right]$ are respectively given as

$$\left[\overline{A}_k\right] = \left[\overline{A}_{11,k} \quad \overline{A}_{12,k}\right], \tag{3.88}$$

$$\left[B_k\right] = \begin{bmatrix} -Z_{22r,k}^{total} \\ -Z_{22i,k}^{total} \end{bmatrix}, \tag{3.89}$$

where

$$\left[\overline{A}_{11,k}\right] = \begin{bmatrix} Z_o & 0 & -Z_o^2 \hat{f}_k^{\,2} & 0 & Z_o Z_{21r,k}^{total} & Z_o Z_{21i,k}^{total} \hat{f}_k \\ 0 & Z_o^2 \hat{f}_k & 0 & -Z_o \hat{f}_k^{\,3} & Z_o Z_{21i,k}^{total} & -Z_o Z_{21r,k}^{total} \hat{f}_k \end{bmatrix} \tag{3.90}$$

$$\left[\overline{A}_{12,k}\right] = \begin{bmatrix} Z_o Z_{21r,k}^{total} \hat{f}_k^{\,2} & -Z_{22r,k}^{total} & \dfrac{-Z_o Z_{22i,k}^{total}}{\hat{f}_k} & Z_o Z_{22i,k}^{total} \hat{f}_k & Z_{22r,k}^{total} \hat{f}_k^{\,2} & 0 \\ Z_o Z_{21i,k}^{total} \hat{f}_k^{\,2} & -Z_{22i,k}^{total} & \dfrac{Z_o Z_{22r,k}^{total}}{\hat{f}_k} & -Z_o Z_{22r,k}^{total} \hat{f}_k & Z_{22i,k}^{total} \hat{f}_k^{\,2} & \dfrac{-Z_o^2}{\hat{f}_k} \end{bmatrix} \tag{3.91}$$

By augmenting $\left[\overline{A}\right]$ and $\left[B\right]$, followed by the total least squares method, L_d can be extracted from the unknown elements of $\left[X\right]$ namely,

$$L_d = \frac{Z_o X_4}{\omega_o X_{11}}, \tag{3.92}$$

Again, in here, the row pivot with scaling is performed before the singular value decomposition so as to improve the condition number. To evaluate the parasitic

capacitances and the remaining parasitic resistances, we first evaluate

$$[Y]=\left([Z_{total}]-[L_{ext}]\right)^{-1}=\left[Y_{pad}\right]+\left([R_{ext}]+[Y_{\text{int}}]^{-1}\right)^{-1}, \tag{3.93}$$

and follow by a re-arrangement of equation (3.93) to make the parasitic capacitances more dominant for extraction. The steps in doing so are detailed below:

$$\left([Y]-\left[Y_{pad}\right]\right)\left([R_{ext}][Y_{\text{int}}]+[I]\right)=[Y_{\text{int}}].$$

$$\Rightarrow[Y]=\left[Y_{pad}\right]+\left([I]-\left([Y]-\left[Y_{pad}\right]\right)[R_{ext}]\right)[Y_{\text{int}}] \tag{3.94}$$

From the second column of equation (3.94), we obtain

$$Y_{12}=\frac{-Y_{11}\left(\frac{C_{pd}}{C_{pg}}a_5s^2+\frac{C_{pd}}{C_{pg}}a_6s+C_{pd}a_{11}\right)+C_{pd}\left(a_5s^3+a_6s^2-a_7s\right)}{\frac{C_{pd}}{C_{pg}}a_5s^2+a_2s+C_{pd}a_{16}}, \tag{3.95}$$

$$Y_{22}=\frac{-Y_{21}\left(\frac{C_{pd}}{C_{pg}}a_5s^2+\frac{C_{pd}}{C_{pg}}a_6s+C_{pd}a_{11}\right)+C_{pd}\left(a_1s^3+a_2s^2+a_4s+a_3\right)}{\frac{C_{pd}}{C_{pg}}a_5s^2+a_2s+C_{pd}a_{16}}. \tag{3.96}$$

Re-arranging the real and imaginary terms of equation (3.95) into matrix form, we achieve

$$[C][W]^{-1}[W][x]=\left[\overline{C}\right][X]=[D], \tag{3.97}$$

where the new normalized unknowns $[X]=[W][x]$,

$$[W]=\text{diag}\left[\omega_o \quad \omega_o^2 \quad Y_o\omega_o^3 \quad Y_o \quad \omega_o \quad \omega_o^2 \quad 1 \quad Y_o\omega_o\right], \tag{3.98}$$

$$[x]^T=\left[C_{pd}a_7 \quad C_{pd}a_6 \quad C_{pd}a_5 \quad C_{pd}a_{11} \quad \frac{C_{pd}}{C_{pg}}a_6 \quad \frac{C_{pd}}{C_{pg}}a_5 \quad C_{pd}a_{16}-1 \quad a_2\right] \tag{3.99}$$

and the k_{th} element of the real and imaginary terms of the $\left[\overline{C}\right]$ and $[D]$ are

respectively given in terms of the Y-parameter elements as

$$\left[\overline{C}_k\right]=\left[\overline{C}_{11,k}\quad \overline{C}_{12,k}\right], \tag{3.100}$$

$$\left[D_k\right]=\begin{bmatrix} Y_{12r,k} \\ Y_{12i,k} \end{bmatrix}, \tag{3.101}$$

where

$$\left[\overline{C}_{11,k}\right]=\begin{bmatrix} 0 & -\hat{f}_k^2 & 0 \\ -\hat{f}_k & 0 & -Z_o\hat{f}_k^3 \end{bmatrix}, \tag{3.102}$$

$$\left[\overline{C}_{12,k}\right]=\begin{bmatrix} -Z_oY_{11r,k} & Y_{11i,k}\hat{f}_k & \left(Y_{11r,k}+Y_{12r,k}\right)\hat{f}_k^2 & -Y_{12r,k} & Z_oY_{12i,k}\hat{f}_k \\ -Z_oY_{11i,k} & -Y_{11r,k}\hat{f}_k & \left(Y_{11i,k}+Y_{12i,k}\right)\hat{f}_k^2 & -Y_{12i,k} & -Z_oY_{12r,k}\hat{f}_k \end{bmatrix}. \tag{3.103}$$

Using the scaled row pivoting, and the total least squares method as outline above, the unknown C_{pg} can be extracted from

$$C_{pg}=\frac{Z_oX_3}{\omega_oX_6}. \tag{3.104}$$

Similarly, by recasting equation (3.96) in the same form as equation (3.97), we have

$$\left[E\right]\left[P\right]^{-1}\left[P\right]\left[x\right]=\left[\overline{E}\right]\left[X\right]=\left[F\right], \tag{3.105}$$

where the normalized unknowns $\left[X\right]=\left[P\right]\left[x\right]$,

$$\left[P\right]=\text{diag}\left[1\quad \omega_o\quad \omega_o^2\quad \omega_o^3\quad Y_o\quad \omega_o\quad \omega_o^2\quad 1\quad Y_o\omega_o\right], \tag{3.106}$$

$$\left[x\right]^T=\left[C_{pd}a_3\quad C_{pd}a_4\quad C_{pd}a_2\quad C_{pd}a_1\quad C_{pd}a_{11}\quad \frac{C_{pd}}{C_{pg}}a_6\quad \frac{C_{pd}}{C_{pg}}a_5\quad C_{pd}a_{16}-1\quad \frac{C_{pd}}{C_{pg}}a_2\right] \tag{3.107}$$

and the k_{th} element of the real and imaginary terms of the $\left[\overline{E}\right]$ and $\left[F\right]$ are

respectively given in terms of the Y-parameter elements as

$$\left[\overline{E}_k\right]=\left[\overline{E}_{11,k}\quad \overline{E}_{12,k}\right], \tag{3.108}$$

$$\left[F_k\right]=\begin{bmatrix} Y_{22r,k} \\ Y_{22i,k} \end{bmatrix}, \tag{3.109}$$

where

$$\left[\overline{E}_{11,k}\right]=\begin{bmatrix} 1 & 0 & -\hat{f}_k^2 & 0 \\ 0 & \hat{f}_k & 0 & -\hat{f}_k^3 \end{bmatrix}, \tag{3.110}$$

$$\left[\overline{E}_{12,k}\right]=\begin{bmatrix} -Z_o Y_{21r,k} & Y_{21r,k}\hat{f}_k & \left(Y_{21r,k}+Y_{22r,k}\right)\hat{f}_k^2 & -Y_{22i,k} & Z_o Y_{22i,k}\hat{f}_k \\ -Z_o Y_{11i,k} & -Y_{21i,k}\hat{f}_k & \left(Y_{21i,k}+Y_{21i,k}\right)\hat{f}_k^2 & -Y_{22r,k} & -Z_o Y_{22r,k}\hat{f}_k \end{bmatrix} \tag{3.111}$$

Using the scaled row pivoting and the outlined total least squares method mentioned above, the unknown C_{pd} is thus obtained from

$$C_{pd}=\frac{X_4}{\omega_o X_7}. \tag{3.112}$$

Having extracted the parasitic capacitances, its contribution to the Y-parameter can thus be removed through either

$$\left[Z\right]=\left(\left[Y\right]-\left[Y_{pad}\right]\right)^{-1}=\left[R_{ext}\right]+\left[Y_{\text{int}}\right]^{-1},$$

$$\Rightarrow\left[Y_{\text{int}}\right]\left(\left[Z\right]-\left[R_{ext}\right]\right)-\left[I\right]=0, \tag{3.113}$$

or

$$\left[\overline{Y}\right]^{-1}=\left(\left[Y\right]-\left[Y_{pad}\right]\right)^{-1}=\left[R_{ext}\right]+\left[Y_{\text{int}}\right]^{-1}$$

$$\Rightarrow\left(\left[I\right]-\left[\overline{Y}\right]\left[R_{ext}\right]\right)\left[Y_{\text{int}}\right]-\left[\overline{Y}\right]=0, \tag{3.114}$$

From equation (3.113), the 1st matrix element of the 1st column will result in

$$Z_{21} = \frac{Z_{11}\left(s^2 b_1 + s\left(b_2 + b_5\right)\right) + s^2 b_3 + s b_4 + 1}{s\left(b_1 s + b_5\right)}, \tag{3.115}$$

where

$$b_1 = C_{dg} C_{gs} R_i, \tag{3.116}$$

$$b_2 = C_{gs}, \tag{3.117}$$

$$b_3 = b_2\left(L_s + b_5 R_g R_i\right), \tag{3.118}$$

$$b_4 = b_2\left(R_g + R_s + R_i\right), \tag{3.119}$$

$$b_5 = C_{dg}. \tag{3.120}$$

Taking the sum of the squares of the real and imaginary terms of equation (3.115) and imposing the derivative of each unknown to be zero, we arrive at the following expression:

$$[A][X]^T = [B], \tag{3.121}$$

where

$$[X] = \begin{bmatrix} \omega_o^2 b_1 & \omega_o b_5 & \omega_o b_2 & \omega_o^2 b_3 & \omega_o b_4 \end{bmatrix}, \tag{3.122}$$

$$[B] = \begin{bmatrix} \sum_{k=1}^{N} \hat{f}_k^2 \left(Z_{11r,k} - Z_{21r,k}\right) \\ \sum_{k=1}^{N} \hat{f}_k \left(Z_{11i,k} - Z_{21i,k}\right) \\ \sum_{k=1}^{N} \hat{f}_k Z_{11i,k} \\ -\sum_{k=1}^{N} \hat{f}_k^2 \\ 0 \end{bmatrix}, \tag{3.123}$$

$$[A]=\begin{bmatrix} Q_{11} & Q_{12} & Q_{13} \\ Q_{12}^T & \sum_{k=1}^{N}\hat{f}_k\left|Z_{11,k}\right|^2 & Q_{23} \\ Q_{13}^T & Q_{23}^T & Q_{33} \end{bmatrix}, \tag{3.124}$$

$$Q_{11}=\begin{bmatrix} \sum_{k=1}^{N}\hat{f}_k^4\left|Z_{11,k}-Z_{21,k}\right|^2 & 0 \\ 0 & \sum_{k=1}^{N}\hat{f}_k^2\left|Z_{11,k}-Z_{21,k}\right|^2 \end{bmatrix}, \tag{3.125}$$

$$Q_{12}=\begin{bmatrix} \sum_{k=1}^{N}\hat{f}_k^3\left(Z_{11r,k}Z_{21i,k}-Z_{11i,k}Z_{21r,k}\right) \\ \sum_{k=1}^{N}\hat{f}_k^2\left(Z_{11i,k}\left(Z_{11i,k}-Z_{21i,k}\right)+Z_{11r,k}\left(Z_{11r,k}-Z_{21r,k}\right)\right) \end{bmatrix}, \tag{3.126}$$

$$Q_{13}=\begin{bmatrix} \sum_{k=1}^{N}\hat{f}_k^4\left(Z_{11r,k}-Z_{21r,k}\right) & \sum_{k=1}^{N}\hat{f}_k^3\left(Z_{21i,k}-Z_{11i,k}\right) \end{bmatrix}, \tag{3.127}$$

$$Q_{23}=\begin{bmatrix} \sum_{k=1}^{N}\hat{f}_k^3\left(Z_{11i,k}-Z_{21i,k}\right) & -\sum_{k=1}^{N}\hat{f}_k^2\left(Z_{11r,k}-Z_{21r,k}\right) \\ \sum_{k=1}^{N}\hat{f}_k^3 Z_{11i,k} & \sum_{k=1}^{N}\hat{f}_k^2 Z_{11r,k} \end{bmatrix}, \tag{3.128}$$

$$Q_{33}=\begin{bmatrix} \sum_{k=1}^{N}\hat{f}_k^4 & 0 \\ 0 & \sum_{k=1}^{N}\hat{f}_k^2 \end{bmatrix}, \tag{3.129}$$

By solving the unknowns from equation (3.121), the unknowns C_{dg} , C_{gs} , R_i , R_g and L_s can be obtained through the unknowns $[X]$, namely,

$$C_{dg}=\frac{X_2}{\omega_o}, \tag{3.130}$$

$$C_{gs}=\frac{X_3}{\omega_o}, \tag{3.131}$$

$$R_i=\frac{X_1}{X_2X_3}, \tag{3.132}$$

$$R_g = \frac{X_5}{C_{gs}\omega_o} - \left(R_s + R_i\right), \tag{3.133}$$

$$L_s = \frac{X_4 - R_g X_1}{\omega_o^2 C_{gs}}, \tag{3.134}$$

Similarly, from the 1st element of the 2nd column of equation (3.114), we obtain

$$\overline{Y}_{12} = \frac{-\overline{Y}_{11}\left(s^2\, a_1/b_6 + s\, b_8/b_6 + b_9\right) - sb_5/b_6}{s^2 a_1/b_6 + sb_7 + 1}, \tag{3.135}$$

where

$$b_6 = 1 + g_{ds}\left(R_d + R_s\right), \tag{3.136}$$

$$b_7 = \frac{g_{ds}L_s + C_{dg}R_d + C_{ds}\left(R_d + R_s\right)}{1 + g_{ds}\left(R_d + R_s\right)}, \tag{3.137}$$

$$b_8 = g_{ds}L_s - C_{dg}R_g + C_{ds}R_s, \tag{3.138}$$

$$b_9 = \frac{g_{ds}R_s}{1 + g_{ds}\left(R_d + R_s\right)}, \tag{3.139}$$

Use the same least squares approach outlined as above, we re-formulate equation (3.135) into

$$[A][X]^T = [B], \tag{3.140}$$

Where

$$[X] = \begin{bmatrix} b_9 & \omega_o b_7 & \omega_o b_8/b_6 & \omega_o b_5/b_6 & \omega_o^2 a_1/b_6 \end{bmatrix}, \tag{3.141}$$

$$[B]=\begin{bmatrix} -\sum_{k=1}^{N}\left(\overline{Y}_{11r,k}\overline{Y}_{12r,k}+\overline{Y}_{11i,k}\overline{Y}_{12i,k}\right) \\ -\sum_{k=1}^{N}\widehat{f}_k\left(\overline{Y}_{12i,k}\overline{Y}_{11r,k}-\overline{Y}_{11i,k}\overline{Y}_{12r,k}\right) \\ -\sum_{k=1}^{N}\widehat{f}_k\overline{Y}_{12i,k} \\ \sum_{k=1}^{N}\widehat{f}_k^2\left(\overline{Y}_{12r,k}\left(\overline{Y}_{11r,k}+\overline{Y}_{12r,k}\right)+\overline{Y}_{12i,k}\left(\overline{Y}_{11i,k}+\overline{Y}_{12i,k}\right)\right) \end{bmatrix}, \tag{3.142}$$

$$[A]=\begin{bmatrix} \overline{Q}_{11} & \overline{Q}_{12} & \overline{Q}_{13} \\ \overline{Q}_{12}^T & \sum_{k=1}^{N}\widehat{f}_k^2\left|Z_{11,k}\right|^2 & \overline{Q}_{23} \\ \overline{Q}_{13}^T & \overline{Q}_{23}^T & \overline{Q}_{33} \end{bmatrix}, \tag{3.143}$$

$$\overline{Q}_{11}=\begin{bmatrix} \sum_{k=1}^{N}\left|\overline{Y}_{11,k}\right|^2 & \sum_{k=1}^{N}\widehat{f}_k\left(\overline{Y}_{11i,k}\overline{Y}_{12r,k}-\overline{Y}_{11r,k}\overline{Y}_{12i,k}\right) \\ \sum_{k=1}^{N}\widehat{f}_k\left(\overline{Y}_{11i,k}\overline{Y}_{12r,k}-\overline{Y}_{11r,k}\overline{Y}_{12i,k}\right) & \sum_{k=1}^{N}\widehat{f}_k^2\left|\overline{Y}_{12,k}\right|^2 \end{bmatrix} \tag{3.144}$$

$$\overline{Q}_{12}=\begin{bmatrix} 0 \\ \sum_{k=1}^{N}\widehat{f}_k^2\left(\overline{Y}_{11i,k}\overline{Y}_{12i,k}+\overline{Y}_{11r,k}\overline{Y}_{12r,k}\right) \end{bmatrix}, \tag{3.145}$$

$$\overline{Q}_{13}{}^T=\begin{bmatrix} \sum_{k=1}^{N}\widehat{f}_k\overline{Y}_{11i,k} \\ -\sum_{k=1}^{N}\widehat{f}_k^2\left(\overline{Y}_{11r,k}\left(\overline{Y}_{11r,k}+\overline{Y}_{12r,k}\right)+\overline{Y}_{11i,k}\left(\overline{Y}_{11i,k}+\overline{Y}_{12i,k}\right)\right) \end{bmatrix}, \tag{3.146}$$

$$\overline{Q}_{23}=\begin{bmatrix} \sum_{k=1}^{N}\widehat{f}_k^2\overline{Y}_{12r,k} & \sum_{k=1}^{N}\widehat{f}_k^3\left(\overline{Y}_{11r,k}\overline{Y}_{12i,k}-\overline{Y}_{11i,k}\overline{Y}_{12r,k}\right) \\ \sum_{k=1}^{N}\widehat{f}_k^2\overline{Y}_{11r,k} & \sum_{k=1}^{N}\widehat{f}_k^3\left(\overline{Y}_{11i,k}\overline{Y}_{12r,k}-\overline{Y}_{11r,k}\overline{Y}_{12i,k}\right) \end{bmatrix}, \tag{3.147}$$

$$\overline{Q}_{33}=\begin{bmatrix} \sum_{k=1}^{N}\widehat{f}_k^2 & -\sum_{k=1}^{N}\widehat{f}_k^3\left(\overline{Y}_{11i,k}+\overline{Y}_{21i,k}\right) \\ -\sum_{k=1}^{N}\widehat{f}_k^3\left(\overline{Y}_{11i,k}+\overline{Y}_{21i,k}\right) & \sum_{k=1}^{N}\widehat{f}_k^4\left|\overline{Y}_{11,k}+\overline{Y}_{12,k}\right|^2 \end{bmatrix}. \tag{3.148}$$

By solving the unknowns from equation (3.140), the unknowns C_{ds} , g_{ds} and R_d can

be obtained through $[X]$, namely,

$$C_{ds} = \frac{C_{dg} X_5}{\omega_o X_4 L_s}, \tag{3.149}$$

$$g_{ds} = \frac{1}{L_s}\left(\frac{C_{dg} X_3}{X_4} + C_{dg} R_g - C_{ds} R_s \right), \tag{3.150}$$

$$R_d = \frac{1}{g_{ds}}\left(\frac{\omega_o C_{dg}}{X_4} - 1 \right) - R_s \tag{3.151}$$

The unknown g_m is found through the total least squares solution of the following expressions:

$$U \sum V^T = svd\left([A; B] \right)$$

$$= svd\left(\begin{bmatrix} 1 & 0 & -\frac{\hat{f}_k^2}{2} & 0 & \hat{f}_k \left(Y_{21i,k}^{\text{int}} - Y_{12i,k}^{\text{int}} \right) & -\left(Y_{21r,k}^{\text{int}} - Y_{12r,k}^{\text{int}} \right) \\ 0 & -\hat{f}_k & 0 & \frac{\hat{f}_k^3}{6} & -\hat{f}_k \left(Y_{21r,k}^{\text{int}} - Y_{12r,k}^{\text{int}} \right) & -\left(Y_{21i,k}^{\text{int}} - Y_{12i,k}^{\text{int}} \right) \end{bmatrix} \right) \tag{3.152}$$

$$g_m = \frac{V(1, end)}{V(end, end)}. \tag{3.153}$$

The unknown τ can be obtained through the conventional least squares solution of

$$\zeta_r + j\zeta_i = \left[\left(Y_{21}^{\text{int}} - Y_{12}^{\text{int}} \right)\left(1 + j\omega C_{gs} R_i \right) \right]^{\frac{1}{\hat{f}_k}}, \tag{3.154}$$

$$\tau = \frac{1}{\omega_0 N} \sum_{k=1}^{N} \left| \tan^{-1}\left(\frac{\zeta_i}{\zeta_r} \right) \right|. \tag{3.155}$$

3.4.3 Numerical results and discussion

The proposed algorithm can be easily implemented using the Matlab 7.0 software on a personal computer (Pentium IV or above). First, to test the validity and accuracy of this new analytical modelling method, three different types of TOSHIBA® GaAs MESFETs, namely, 2×150μm, 8×150μm and 16×150μm have been adopted in this study. S-parameters from 1GHz up to 30GHz are measured under a wide biasing range of V_{gs}=-2.0~0.5V, V_{ds}=0.0~4.0V. The new analytical method and the commonly adopted conventional Dambrine's method [11] are used for their parasitic and intrinsic elements determination. Parasitic elements' values of three GaAs MESFETs extracted from these two methods are displayed in Table 3.1, Table 3.2 and 3.3, respectively. In addition, the parasitic and intrinsic values extracted from Dambrines's method.

Table 3.1 Parasitic Elements Extracted from 2×150μm GaAs MESFET

New Analytical Method							
C_{pg} (fF)	C_{pd} (fF)	L_g (pH)	L_d (pH)	L_s (pH)	R_g (Ω)	R_d (Ω)	R_s (Ω)
177.72	86.62	85.43	23.20	15.01	1.68	0.78	0.33
Dambrine's Method							
C_{pg} (fF)	C_{pd} (fF)	L_g (pH)	L_d (pH)	L_s (pH)	R_g (Ω)	R_d (Ω)	R_s (Ω)
208.84	56.15	88.86	19.87	15.26	1.43	0.91	0.35

Table 3.2 Parasitic Elements Extracted from 8×150μm GaAs MESFET

New Analytical Method							
C_{pg} (fF)	C_{pd} (fF)	L_g (pH)	L_d (pH)	L_s (pH)	R_g (Ω)	R_d (Ω)	R_s (Ω)
190.86	91.65	84.31	62.75	11.36	1.25	0.92	0.38
Dambrine's Method							
C_{pg} (fF)	C_{pd} (fF)	L_g (pH)	L_d (pH)	L_s (pH)	R_g (Ω)	R_d (Ω)	R_s (Ω)
233.15	75.68	83.94	60.17	12.13	2.08	0.77	0.53

Table 3.3 Parasitic Elements Extracted from 16×150μm GaAs MESFET

New Analytical Method							
C_{pg} (fF)	C_{pd} (fF)	L_g (pH)	L_d (pH)	L_s (pH)	R_g (Ω)	R_d (Ω)	R_s (Ω)
210.86	69.51	85.81	84.32	7.15	0.72	1.96	0.43
Dambrine's Method							
C_{pg} (fF)	C_{pd} (fF)	L_g (pH)	L_d (pH)	L_s (pH)	R_g (Ω)	R_d (Ω)	R_s (Ω)
149.39	23.89	86.95	82.17	8.06	0.64	1.62	0.85

Intrinsic elements calculated from these two methods are shown in Table 3.4 to 3.6, the calculation is under the biasing condition V_{gs}=0.0V, V_{ds}=5.0V.

As shown in Tables 3.4 – 3.6, for the intrinsic elements extraction of GaAs MESFETs, negative values can be observed for C_{ds} from the traditional method. However, these negative values had no physical meaning, thus cannot be used in circuit simulation. In contrast, the new approach leads to reasonable results for parasitic element values. The results for parasitic element values from the two

methods differ mainly in two capacitors C_{pg} and C_{pd}. As mentioned earlier, extrinsic small signal parameters are independent of biasing voltage. Therefore, the stabilities of these two extrinsic capacitors will be investigated later for multiple biasing points to show that the new approach gives a better extraction for both C_{pg} and C_{pd} than the traditional method.

Table 3.4 Intrinsic Elements Extracted from 2×150μm GaAs MESFET (V_{gs}=0.0V, V_{ds}=5.0V)

New Analytical Method						
C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	R_i (Ω)	g_{ds} (mS)	g_m (mS)	τ (pS)
329.91	22.74	42.75	2.53	6.55	92.93	0.054
Dambrine's Method						
C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	R_i (Ω)	g_{ds} (mS)	g_m (mS)	τ (pS)
329.18	22.73	-10.68	2.61	6.34	91.82	0.054

Table 3.5 Intrinsic Elements Extracted from 8×150μm GaAs MESFET (V_{gs}=0.0V, V_{ds}=5.0V)

New Analytical Method						
C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	R_i (Ω)	g_{ds} (mS)	g_m (mS)	τ (pS)
1617.14	113.06	114.76	1.35	18.80	397.05	0.055
Dambrine's Method						
C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	R_i (Ω)	g_{ds} (mS)	g_m (mS)	τ (pS)
1623.79	113.14	-77.37	1.86	18.24	398.95	0.055

Table 3.6 Intrinsic Elements Extracted from 16×150μm GaAs MESFET (V_{gs}=0.0V, V_{ds}=5.0V)

New Analytical Method						
C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	R_i (Ω)	g_{ds} (mS)	g_m (mS)	τ (pS)
2787.98	263.58	345.12	0.59	41.6	942.56	0.055
Dambrine's Method						
C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	R_i (Ω)	g_{ds} (mS)	g_m (mS)	τ (pS)
2783.41	257.64	163.22	0.87	44.7	985.06	0.055

Figure 3.14 to 3.16 show the comparison between the modeled and the measured S-parameter. Equivalent circuit element values use the results calculated from the novel analytical modelling method. It can be seen that the modeled S-parameter is in good accordance with the measured S-parameter.

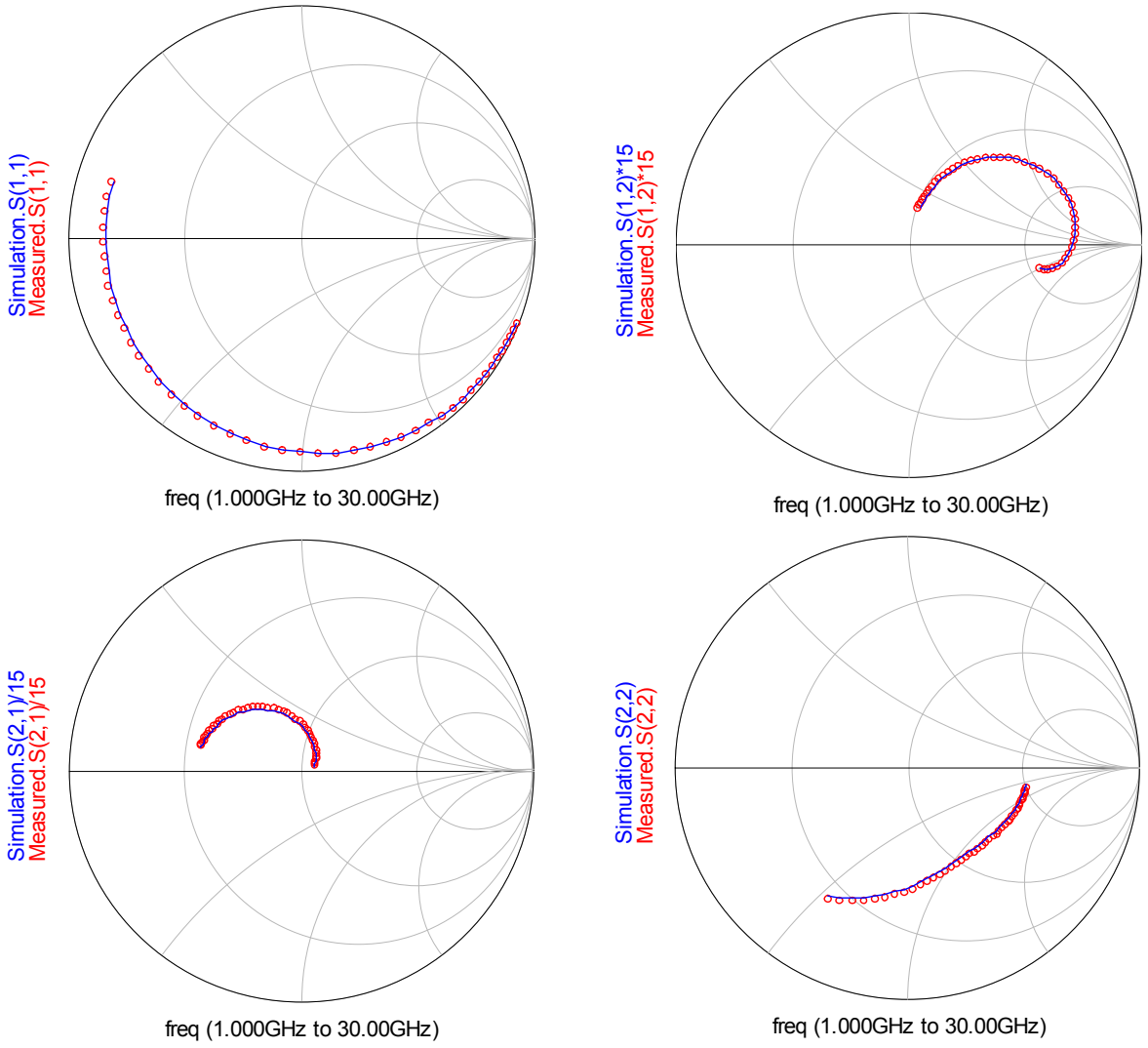
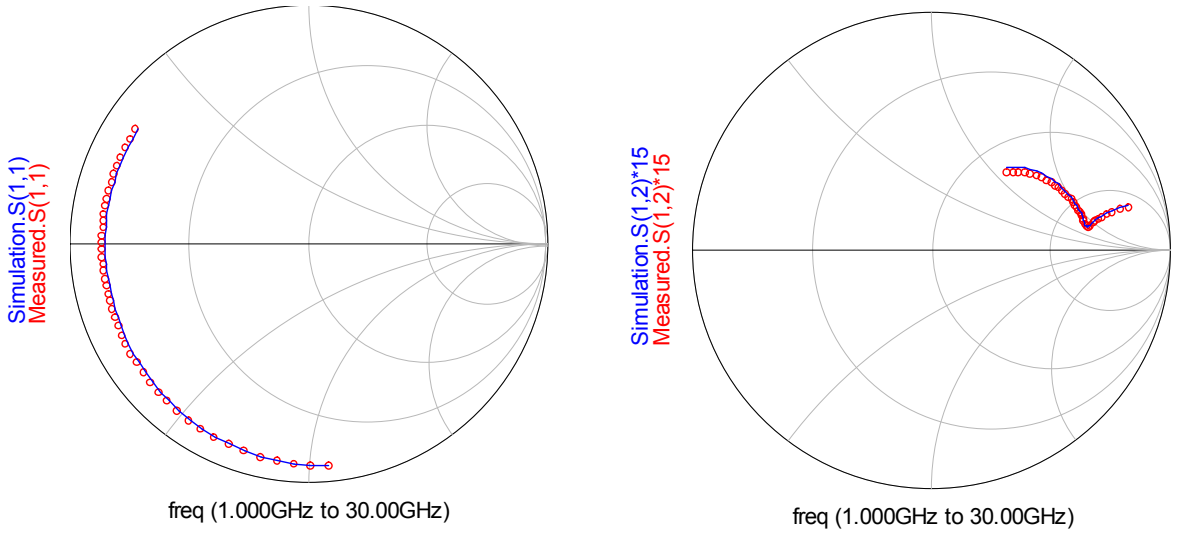


Figure 3.14 Measured (circle) and simulated (solid) S-parameters (2*150um GaAs MESFET)



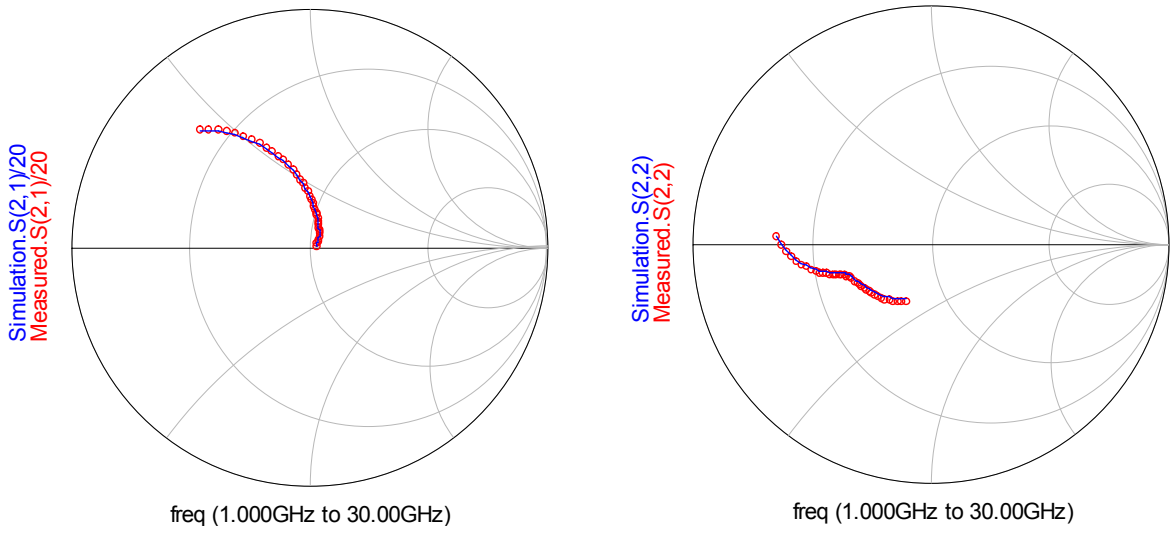


Figure 3.15 Measured (circle) and simulated (solid) S-parameters (8*150um GaAs MESFET)

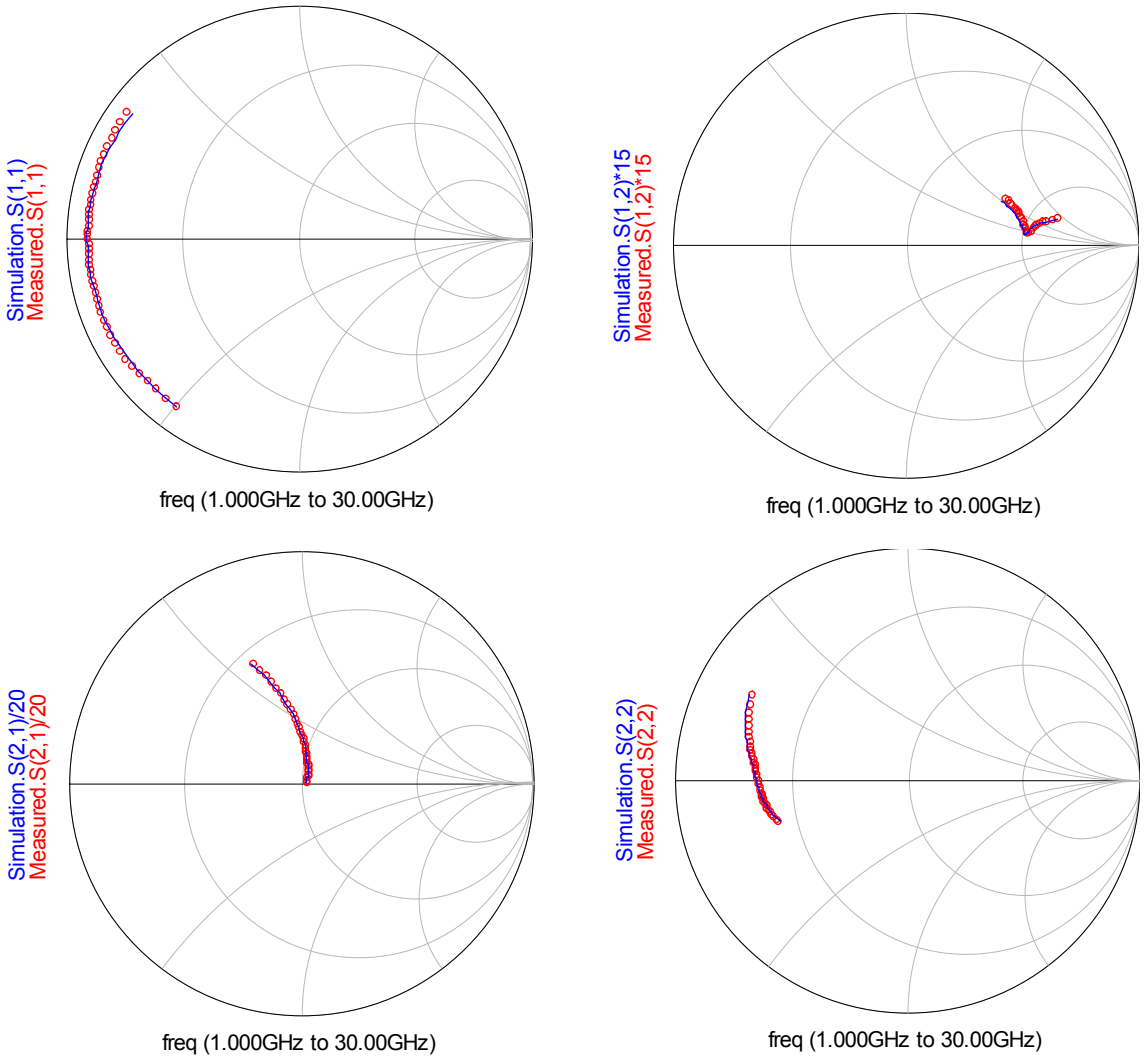


Figure 3.16 Measured (circle) and simulated (solid) S-parameters
(16*150um GaAs MESFET)

Tables 3.7 to 3.9 give the RMS error of the modeled S-parameter by the new method and Dambrine's method. The biasing range is Vgs=-2.0~0.5V, Vds=0.0~4.0V, totally 285 biasing points are taken within this range, and the frequency range is from 1GHz to 30GHz. It can see from Table 3.7 to 3.9, the RMS error of S11, S12, S21 and S22 are all very small for the new analytical method investigated over a wide operating range. Compared with Dambrine's model, it is clear that the new method gives a better fitting performance in the S-parameter description of GaAs MESFETs.

Table 3.7 RMS Error of Modeled S-parameter for 2×150μm GaAs MESFET, Equivalent Circuit Elements Extracted from Dambrine's and new analytical methods

V_{gs}=-2.0-0.5V, V_{ds}=0.0-4.0V, f=1-30GHz

	S_{11}	S_{12}	S_{21}	S_{22}
Dambrine's Method	0.012	0.033	0.046	0.305
New Method	0.006	0.011	0.008	0.017

Table 3.8 RMS Error of Modeled S-parameter for 8×150μm GaAs MESFET, Equivalent Circuit Elements Extracted from Dambrine's and new analytical methods

V_{gs}=-2.0-0.5V, V_{ds}=0.0-4.0V, f=1-30GHz

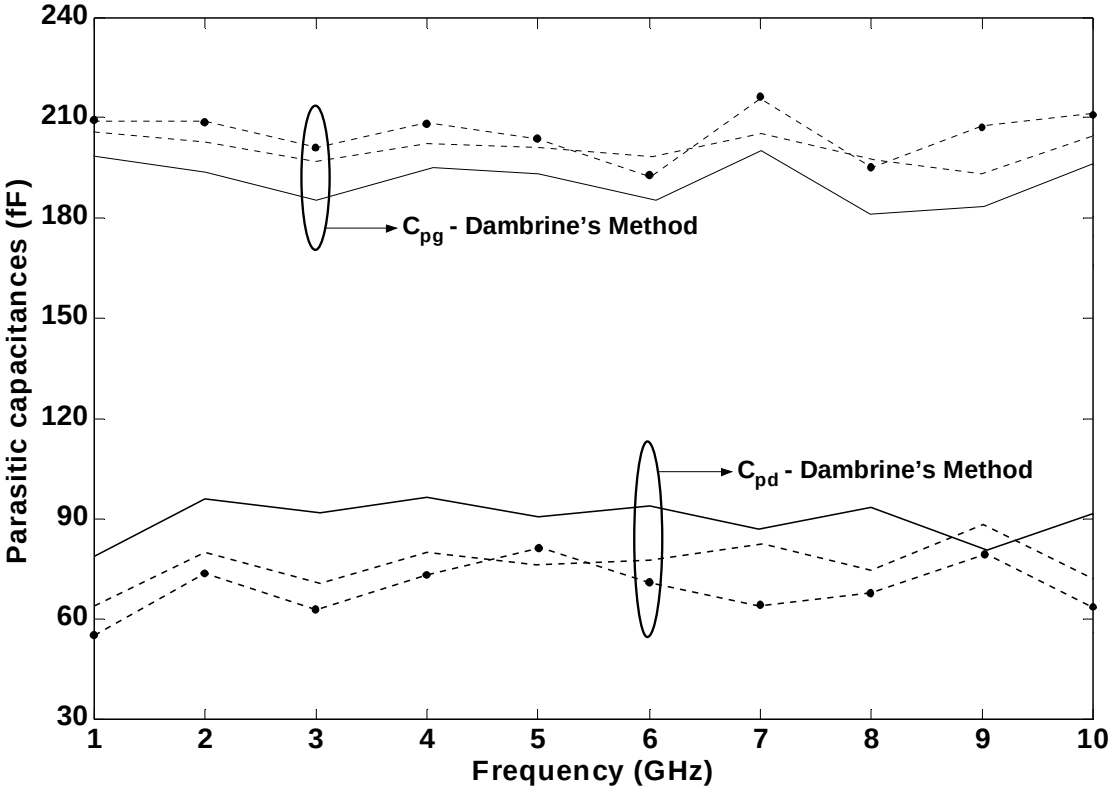
	S_{11}	S_{12}	S_{21}	S_{22}
Dambrine's Method	0.019	0.024	0.021	0.232
New Method	0.007	0.012	0.008	0.016

Table 3.9 RMS Error of Modeled S-parameter for 16×150μm GaAs MESFET, Equivalent Circuit Elements Extracted from Dambrine's and new analytical methods

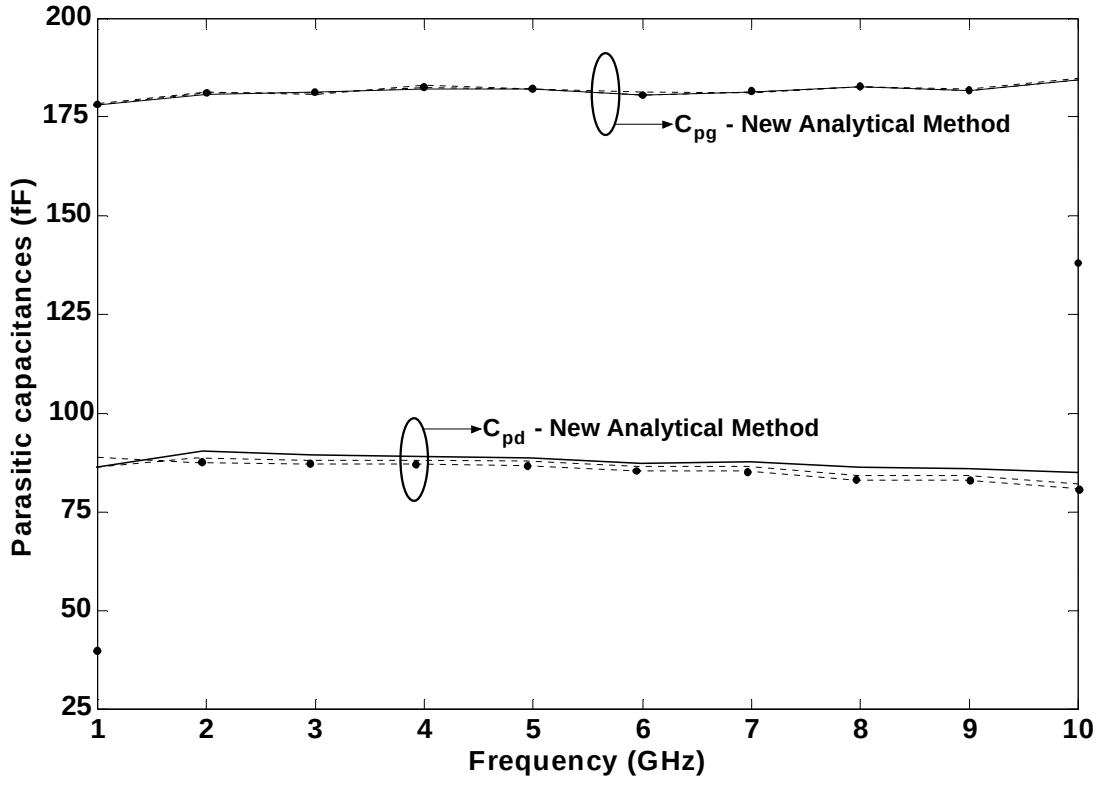
V_{gs}=-2.0-0.5V, V_{ds}=0.0-4.0V, f=1-30GHz

	S_{11}	S_{12}	S_{21}	S_{22}
Dambrine's Method	0.021	0.044	0.024	0.031
New Method	0.016	0.016	0.013	0.011

To test the reliability of the algorithm, the same TOSHIBA® 2×150μmGaAs MESFET device was used in the investigation. S-parameter measurement was taken from 1 to 10 GHz under three different V_{gs} biasing voltage, -5.0V, -2.0V, –1.7V, –0.8V, –0.4V, and –0.2V. Parasitic capacitances C_{pg} and C_{pd} are calculated based on the traditional method and the new analytical method, the result is shown in Figures 3.17. It can be seen from this figure, calculated C_{pg} and C_{pd} values using the Dambrine's method cannot keep constant with the variation of frequency and biasing conditions. In contrast, reasonable and consistent parasitic capacitances achieved from our new method are almost independent with frequency and V_{gs}, which proves the accuracy and stability of this novel approach.

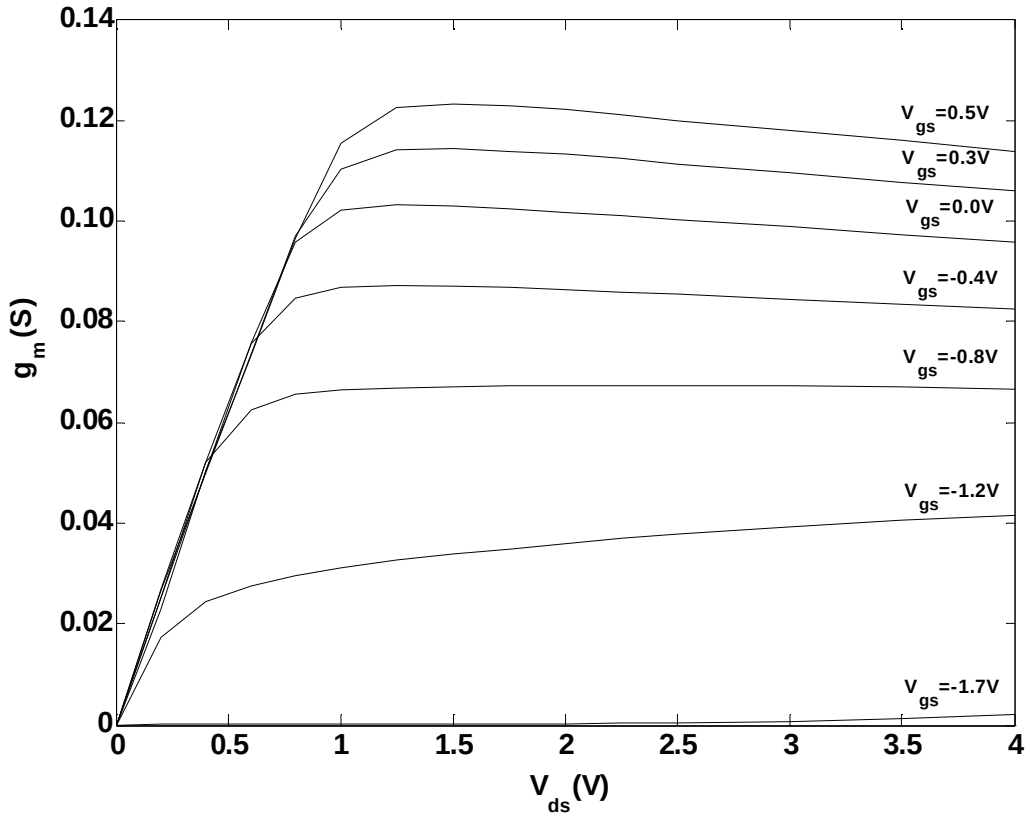


(a)

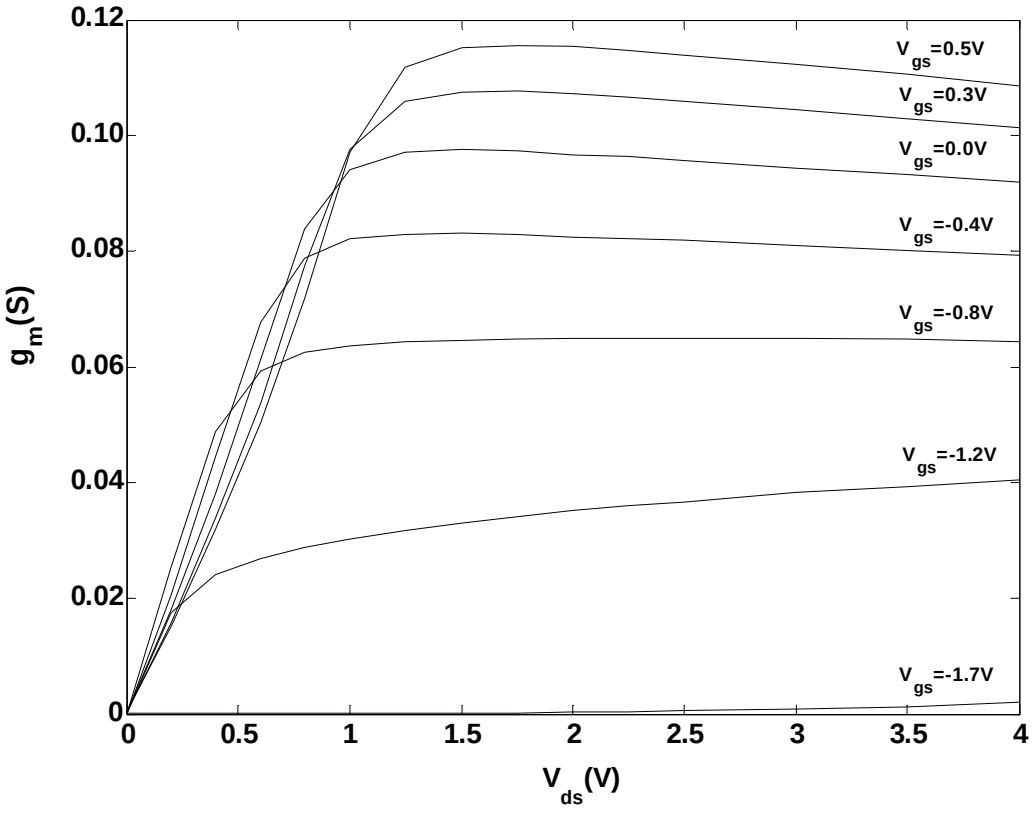


(b)

Figure 3.17 Calculated C_{pg} and C_{pd} (a) by Dambrine's Method (Vds=0.0V, —— Vgs=-5.0V, -----Vgs=-2.0V, --●-- Vgs=-1.7V). (b) by new analytical Method (Vds=0.0V, —— Vgs=-0.8V, -----Vgs=-0.4V, --●-- Vgs=-0.2V).



(a)



(b)

Figure 3.18 Calculated results for gm vs. biasing condition

(a) New analytical method (b) Dambrine's method.

Figure 3.18 shows the extracted g_m versus biasing voltage. The result for the new analytical method is shown in Figure 3.18 (a) whilst Figure 3.18 (b) shows the result for the traditional Dambrine's method. It can be seen from Figure 3.18 (a), that the calculated result of g_m is reasonable, and no unusual result that is against real device operation is observed. But from Fig 3.18 (b), there is overlapping of g_m in the linear and knee region, which cannot be observed in real device operation. Thus, from the g_m result, it can be concluded that the new analytical method is more appropriate for large-signal modelling as compared with the conventional extraction method.

Table 3.10 Extracted and furnished elements' values

Variables	EPA018A			EPA025A		
	Input Data	New Method	Error (%)	Input Data	New Method	Error (%)
L_g (nH)	0.18	0.18	7.9e-10	0.10	0.10	2E-10
R_s (Ω)	0.13	0.13	8.6e-4	0.83	0.83	5.4E-4
L_d (nH)	0.22	0.22	2.1e-9	0.18	0.18	9E-10
C_{pg} (pF)	0.06	0.06	1.3e-8	0.17	0.17	5.6E-8
C_{pd} (pF)	0.06	0.06	7.0e-8	0.17	0.17	1.4E-7
C_{dg} (pF)	0.021	0.021	1.0e-7	0.014	0.014	2.4E-6
C_{gs} (pF)	0.3	0.3	2.8e-7	0.33	0.33	2.5E-6
R_i (Ω)	0.29	0.29	2.4e-5	1.9	1.9	6.1E-5
R_g (Ω)	0.5	0.5	1.9e-4	1.8	1.8	3.0E-4
L_s (nH)	0.057	0.057	1.0e-8	0.071	0.071	4.0E-7
C_{ds} (pF)	0.011	0.011	5.3e-8	0.044	0.044	6.7E-6
g_{ds} (Ω^{-1})	1.5E-3	1.5E-3	3.9e-5	3.6E-3	3.6E-3	9.8E-5
R_d (Ω)	1.0	1.0	1.1e-4	1.38	1.38	1.2E-3
g_m (mS)	55	55	1.2e-4	84	84	2.2E-4
τ (pS)	2.5	2.5	6.9e-6	2.0	2.0	9.0E-6

To test the convergence ability of this algorithm, two different Excelics® semiconductor transistors, namely, EPA018A and EPA025A, have been investigated. The EPA018A is extracted under V_{ds}=6V, I_{ds}=0.5I_{dss} whereas the EPA025A is extracted under V_{ds}=8V, I_{ds}=0.5I_{dss}. These two sets of resulting S-parameters are then calculated from their equivalent circuit whose parameters are provided by the official datasheet [88]. The extracted parameter values are given in Table 3.10. The provided parameters values adopted from Excelics [88] are also reproduced in Table 3.10 for comparison. As shown in Table 3.10, all the extracted parameters' values for all the transistors are very close to the furnished parameters values from Excelics [88]. The worst case errors for all the parameters' values are, in general, all less than 1%.

In the error testing phase, the new analytical extraction method is validated with input data subject to the artificial measurement errors. In this experiment, Monte Carlo methods (or Monte Carlo experiments) [116], which is a class of computational algorithms that rely on repeated random sampling to compute their result, are adopted to add the uniformly distributed random errors to the S-parameter measurement data. Figure 3.19 shows the plot of its extraction output errors vs. artificially added measurement errors. From this illustration, although the output errors increase rapidly with the adding errors, the output parameter values still remain credible (less than 1%) even the maximum measurement errors reach to 6%, which is far beyond the industry measurement standard specification. Therefore, our new analytical extraction method based on least squares method is very robust against measurement errors.

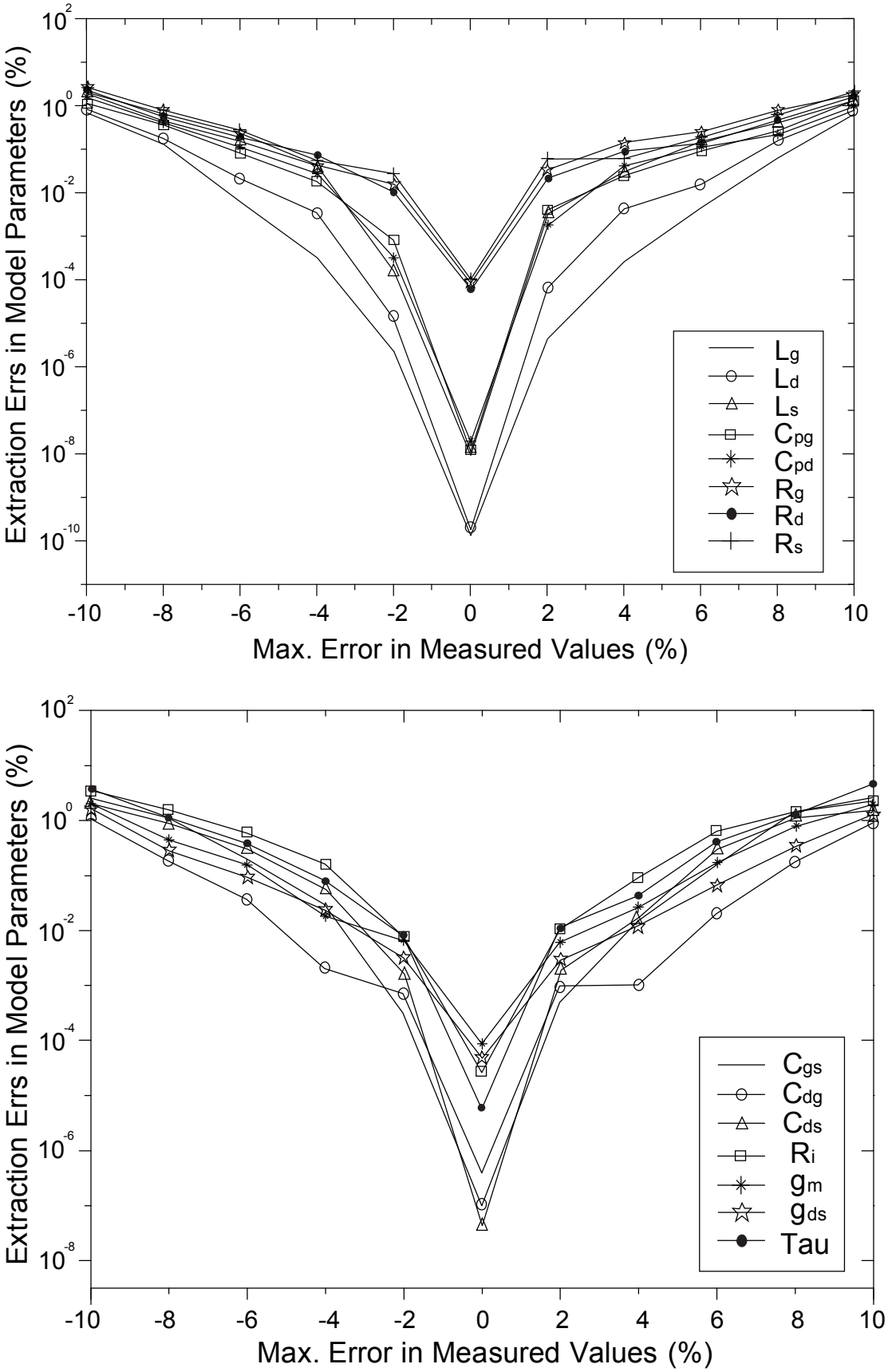


Figure 3.19 Extraction errors of all EC elements vs. maximum measurement errors for the new analytical extraction method

3.5 Conclusion

In this Chapter, major issues of the small signal modelling of GaAs MESFETs are discussed, which include de-embedding techniques, and the determination of small signal model parameters. For the first time, a novel analytical approach for extracting all the 15 equivalent circuit elements for FET devices has been proposed. In contrast to the conventional approach, no subsidiary circuit such as Cold-FET or Hot-FET has been adopted. Comparisons of S-parameter performance in a wide frequency range have subsequently been presented together with the stabilities of parasitic capacitors to verify the better prediction of this novel analytical extraction approach. Reasonable and precise transconductance achieved from this novel method also prove its accuracy and stability. Furthermore, in the error testing phase, this novel method is robust against measurement errors.

On the other hand, the conventional lumped models, based on simple linear rules or completely empirical expressions, may not be sufficiently appropriate at relatively high operating frequencies due to its frequency-independent equivalent circuit. Therefore, a novel distributed modelling approach for GaAs MESFET will be proposed in the next chapter for modern MMIC design.

Chapter 4

A New Distributed Small-Signal Model for GaAs MESFET/HBT

In this chapter, a novel distributed small-signal model for GaAs MESFET at millimetre-wave frequencies is proposed with the aim of providing an accurate and efficient tool for microwave device/MMIC design. This new approach is based on precise electromagnetic simulation and RF circuit analysis of the electron device with distributed cells. As the similarity of issues, this novel method can also be adopted for GaAs HBT small signal modelling. For the first time, the values of the entire GaAs MESFET and HBT intrinsic model elements used in the active elementary cells can be extracted through the quasi-optimization method and explicit analytical expressions. Good agreement between the measured and the simulated results has been demonstrated. This model also allows the designer to have better control over the whole transistor design. Furthermore, it serves as one of the valuable steps towards global modelling of millimeter-wave devices and circuits.

4.1 Introduction

In recent years, the increasing demands for high performance communication systems require MMICs to operate at higher frequencies. The continuous pressure toward low cost microwave communication products has eventually led to a continuous increase of integration density of MMICs. Meanwhile, with this increase of operation frequencies for MMICs, a more complete and accurate millimeter-wave active device modelling is thus needed. The increase of operating frequencies makes the geometry of the millimeter-wave active devices more compatible with the wavelength. As such, wave propagation and electromagnetic interaction must be included in the model in order to account for their important influences on the device's electrical performance [90]. The increment of integration density of MMICs also adversely affects the device's normal electrical performance. The unwanted effects such as the electromagnetic coupling and the unintended radiation must be accurately modeled at higher frequencies.

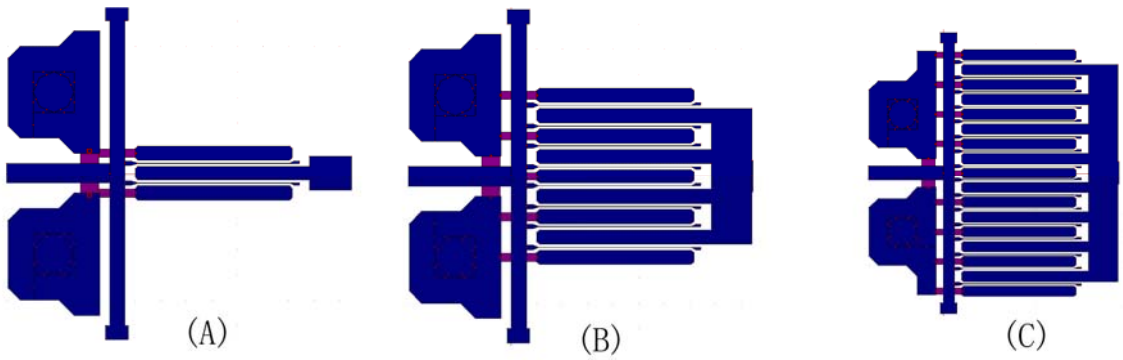


Figure 4.1 Various kinds of TOSHIBA GaAs MESFETs
(A) 2-finger; (B) 8-finger; (C) 16-finger

As shown in Figure 4.1, take various kinds of TOSHIBA GaAs MESFETs for instance, the coupling and lossy effects provided by their large via-holes connected to souce and the multi-finger coupled transmission lines must be taken into account in their small-signal models for accurate high-frequency performance predictions.

In practical MMIC design, the task to accurately predict actual behaviour of these microwave active devices with large layout structure and operating at millimetre-wave frequencies is very crucial and challenging. A distributed characterization of the active device geometry is thus inevitable. In addition, a robust scaling ability of the microwave active devices should be investigated in order to provide an accurate behaviour of the microwave active device as the functions of their layout sizes and finger numbers. The reduction of cost and time in MMIC development is imperative and always requires that the MMIC performance can be optimized efficiently to meet the circuit specifications in a possibly short time. Therefore, a good active device modelling method for MMIC design should provide the designers with the ability to optimize the metallic layouts or finger numbers of the active devices without any geometric limitations. Conventional approach, which adopts the lump elements modelling technique, is unable to accurately predict the device characteristic for different large layout structure. The distributed effects of the fingers and its surrounding are often neglected in the conventional lump element approach and there is no efficient way to optimise the individual fingers using the lump element approximation. The lump element model is also unable to allow the

inclusion of actual GaAs transistor metallic topology, material stratification and the losses in the dielectric and metallization for the simulation.

Different distributed microwave active device models were proposed in the literature to take into account the inherent electromagnetic wave effects. Several global microwave active device models have been proposed, which have robust prediction and optimization capabilities. Some authors [91-93] have developed distributed semiconductor device models which have combined complex semiconductor transport models with full-wave solution of Maxwell's equations. The key aspect of such a modelling method is how to couple Maxwell's equations with the semiconductor hydrodynamic equations. Several techniques such as FDTD method [94] have been adopted to solve this problem. Another approach for the distributed model is to present the active device area studied as a cascade of elementary cells, which are fed by lumped passive networks [95, 96]. This method is applicable to MMIC CAD, and can include electromagnetic signal propagation along the device passive structure. A hybrid method that consists of the integration of the equivalent circuit model and the full-wave model has also been proposed in [90] and [97]-[101]. In such a method, a commercial electromagnetic simulator is adopted to analyse the complex electromagnetic phenomena of the device extrinsic passive part, while the equivalent circuit is used to describe the linear or nonlinear behaviour of the device intrinsic active part. The most important aspect of this method is that the measured data, the electromagnetic simulation results and the scattering parameters of the intrinsic active part are linked through matrix manipulations.

With the continuous improvements of MMICs, one of the new trends for the simulation of complex microwave structure is the “global approach” [91, 92], which couples an electromagnetic analysis and a microwave circuit simulation. Similarly, a new concept, termed the “global modelling” [91, 92], which is related to the active device modelling for MMIC design, has been highlighted and studied continuously. In order to overcome the problems brought by various conventional device modelling methods and apply the new concept of “global modelling”, a novel global and complete approach to characterize the small-signal performance of GaAs MESFET is proposed in this chapter. Regarding the trade-off between simulation accuracy and model development efficiency, we use MoM method in commercial software such as IE3D to rigorously characterize the GaAs MESFET extrinsic domain. A “multi-port connection method” [89] is subsequently applied to link the scattering parameters of the extrinsic and intrinsic domains. Next, an equivalent circuit element extraction technique for determining the intrinsic small-signal model elements is developed. A comparison of the S-parameters between the measured and simulated data has shown good agreement by using our proposed technique. Moreover, the new method is able to accurately predict the unknown electrical responses of other new FET transistors which strongly differ in device geometry.

The main objectives of our proposed model are to enhance model synthesis capability and to raise accuracy of model fitting performance. The accuracy of our modelling method enables the inclusion of actual GaAs transistor metallic topology, material stratification and the losses in the dielectric and metallization. Due to the

scaling capability of our model, the actual performance of some new large-sized GaAs MESFET transistors can be predicted. Furthermore, optimization ability of our method should provide MMIC designers with more freedom to choose a GaAs transistor with arbitrary device geometry, which can be separately adjusted and simulated without any geometric limitations. Through the global modelling approach, the process engineer can now have a greater freedom to experiment with new materials and its effect can thus be included automatically in the EM simulation. In addition, because of the similarity in the issues, this novel method can also be adopted for GaAs HBT small signal modelling, which will also be presented later in this chapter.

4.2 The New Distributed Modelling Method

4.2.1 The basic structure of the novel distributed small-signal model

This new distributed small-signal model is based on accurate electromagnetic simulation and RF circuit analysis of the electron device with distributed cells. It can be separated into two parts: extrinsic passive part and intrinsic active parts. Here uses a typical MESFET layout for example to demonstrate the whole modelling procedures. As shown in Figure 4.2, the distributed GaAs MESFET small-signal model consists of two separated parts, i.e. extrinsic passive and intrinsic active parts. Extrinsic part includes the whole metallic structure of the transistor device, whilst the intrinsic part refers to several active elementary cells to model the semiconductor electrical

behaviours of the device fingers. The intrinsic part, which located under the metallic finger as a multi-layer semiconductor structure, is interconnected with the extrinsic part by means of some internal ports named “local access points” [98].

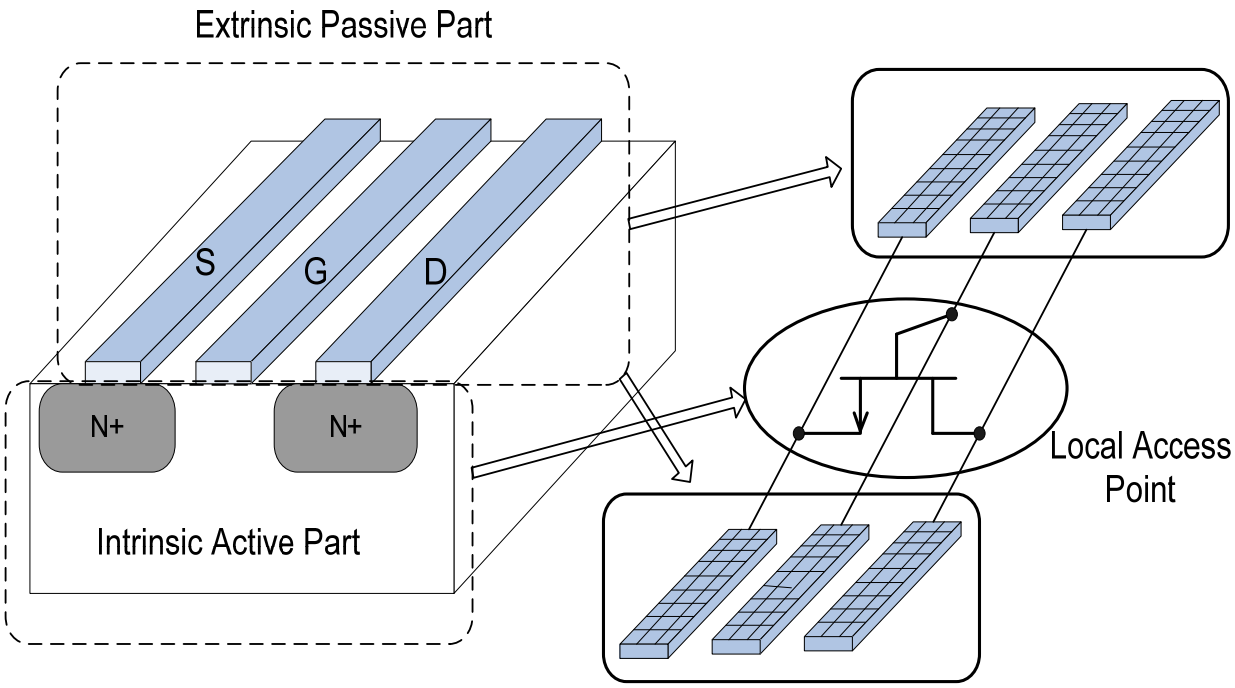


Figure 4.2 A typical MESFET transistor layout and an equivalent representation of the FET extrinsic and intrinsic parts

The extrinsic part, which models the electromagnetic effects in the extrinsic region, is shown in figure 4.2. Here use 2-finger GaAs MESFET device for example. In the proposed method, first describe the extrinsic passive structures of the transistor with IE3D through its geometric parameters of the device GDS files provided by the foundry. Then divide the whole passive structure into several multi-ports models: input part, FET stripe channels and output part, whose dimensions are identically the same with the measured 2-finger GaAs FET layout. The extrinsic passive structure of

a GaAs MESFET is characterized in terms of multi-port S-parameters, instead of the conventional lumped element approach, by means of a global full-wave electromagnetic simulation. Meanwhile, sufficient fine mesh cell is needed to prevent unambiguous oscillatory waveform. The other multi-finger GaAs MESFETs/HBTs are simulated with the same principle as 2-finger GaAs MESFET.

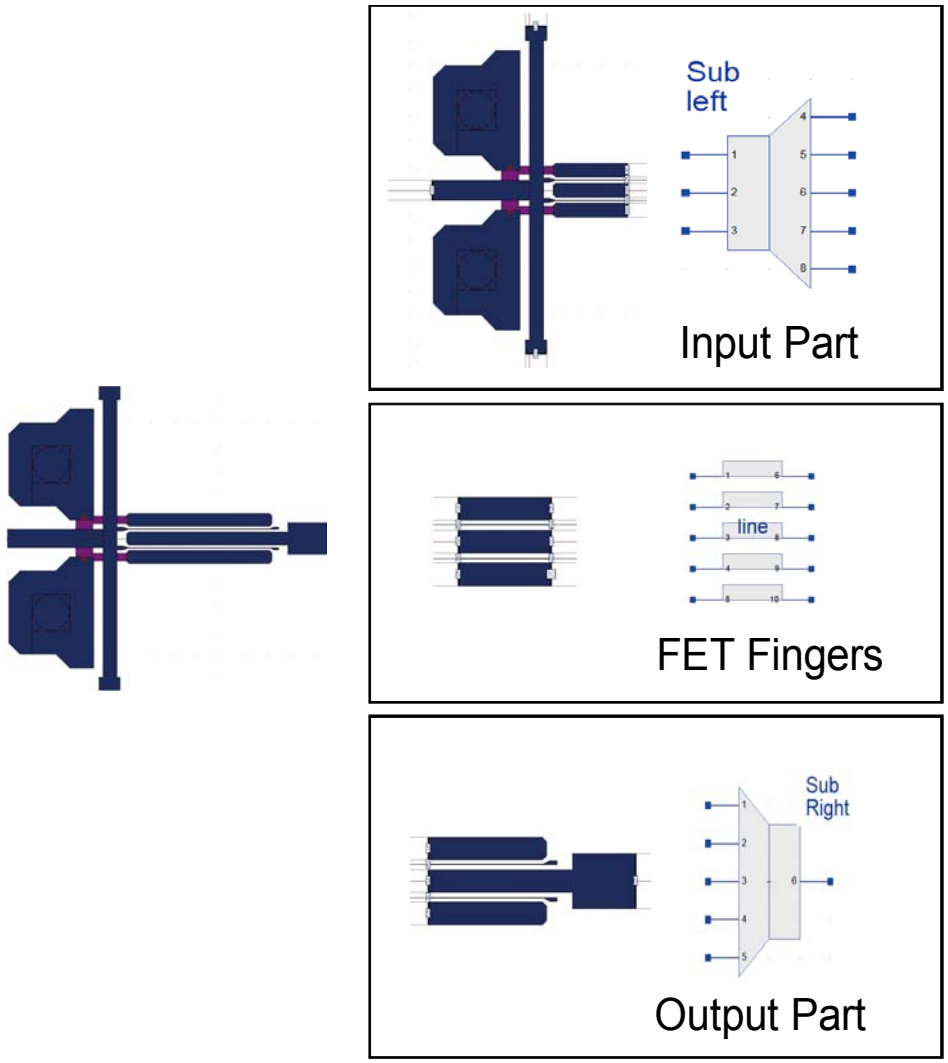


Figure 4.3 Extrinsic part of 2-finger GaAs MESFET

The extrinsic part enables the inclusion of actual GaAs transistor metallic topology, material stratification and the losses in the dielectric and metallization. The

benefits of electromagnetic simulation are that it not only takes into account the influence of elements located near the active device and notably the source via-holes, but also permits the prediction of the behaviour of devices with various gate widths. Due to the scaling capability of our model, the actual performance of some new large-sized GaAs MESFET transistors can be predicted.

The intrinsic part of this model, as mentioned before, is the active semiconductor channel region under the metallic structure of the transistor. As shown in Figure 4.4, the intrinsic part of GaAs MESFET is modelled with the equivalent circuit under its metallic structure within the dashed box. For GaAs HBT, a standard hybrid-π equivalent circuit for bipolar transistor small-signal modelling is used to describe the electrical response of the intrinsic active part of a HBT transistor. The equivalent circuit of its intrinsic part is also shown under the fingers of GaAs HBT in Figure 4.5. The s-parameters of these intrinsic active parts of GaAs MESFETs and HBTs can be easily obtained through the multi-port connection method which will be introduced in the next section. Two novel extraction methodologies for the components of intrinsic active parts of GaAs MESFETs and HBTs will also be presented later in this chapter.

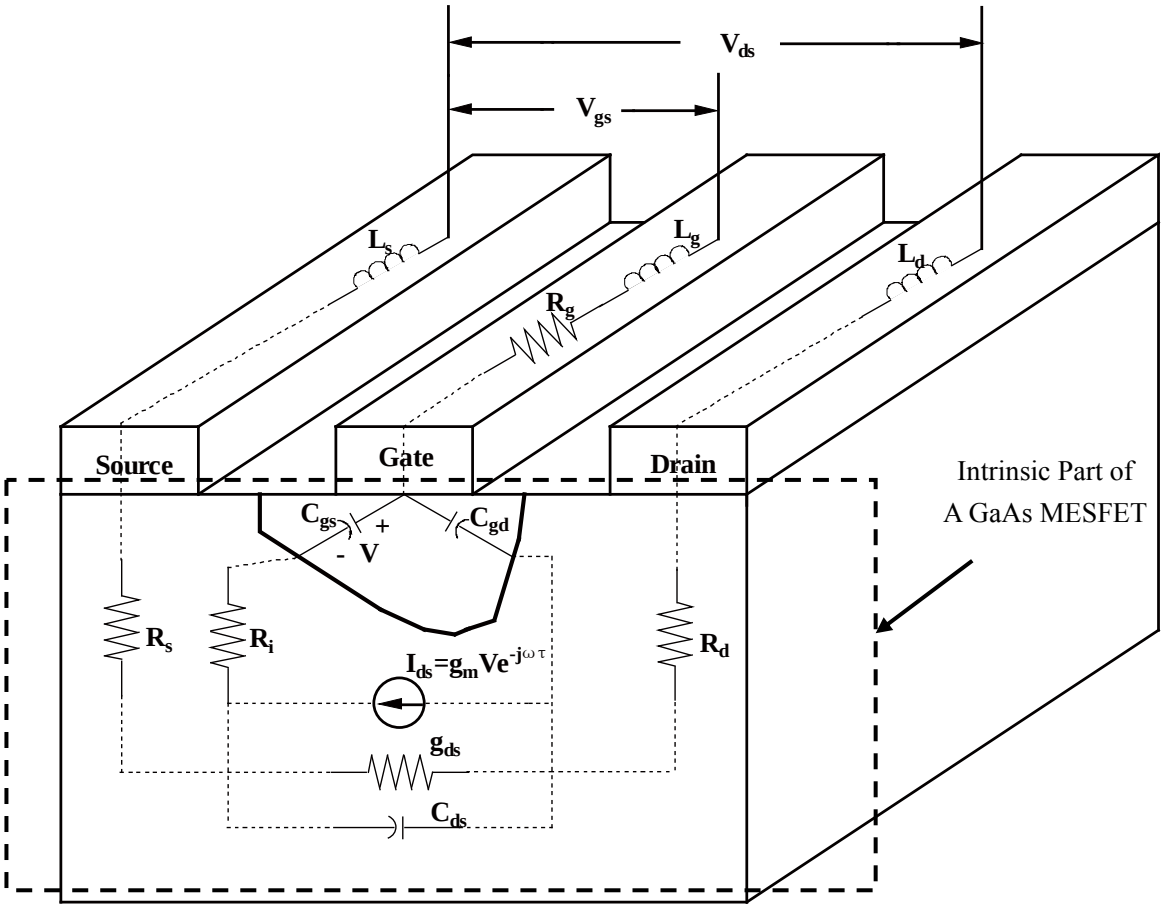


Figure 4.4 Intrinsic part of a GaAs MESFET (indicated within the dashed box)

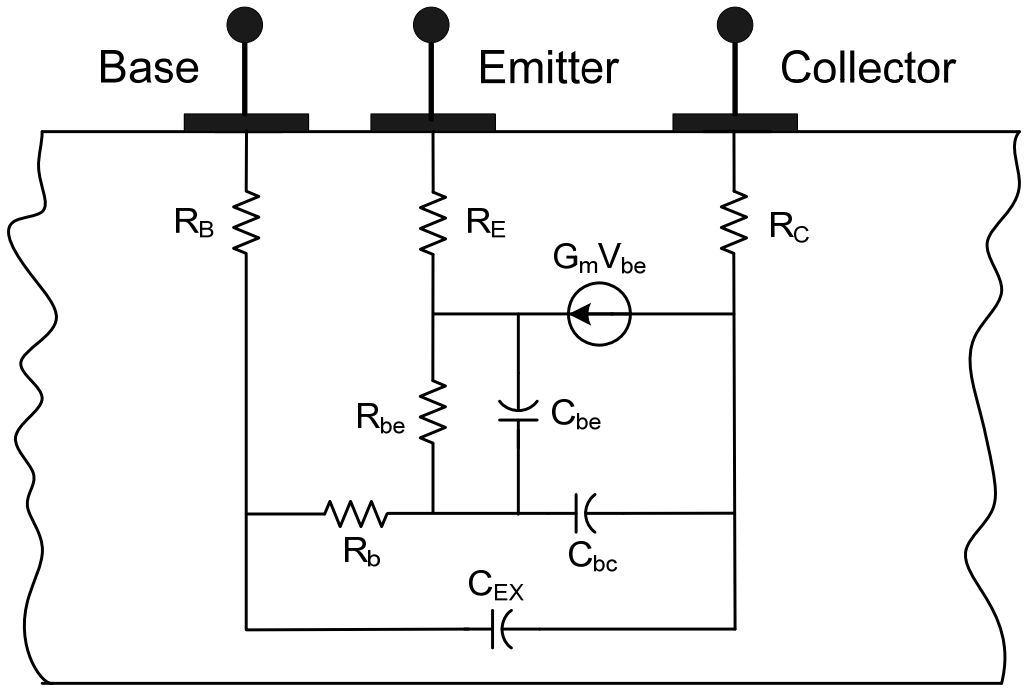


Figure 4.5 Intrinsic part of a GaAs BJT (indicated within the dashed box)

4.2.2 Electromagnetic Analysis of Extrinsic Part of GaAs Transistor Structure

In this method similar to [100, 101], the commercial electromagnetic simulator software IE3D has been used to obtain the S-matrix for the extrinsic part of the transistor structure, which can replace the lumped extrinsic elements. In this way, both parasitic capacitances and inductances related to the internal access points and connection lines have been naturally taken into account. As shown in Figure 4.6, each active elementary cell (AEC) is formed by three "local access points" placed on gate, drain and source electrodes for the same transistor finger group. Moreover, each of the AEC is characterized by the same intrinsic lumped-element equivalent circuit model. In order to connect the electromagnetic simulation results with the small-signal model of the active elementary cell, "internal access points" in each device finger must be included in the device layout for electromagnetic simulation in IE3D. Therefore, the S-matrix calculated by electromagnetic simulation must include the general input /output terminals and all the "internal access points". In Figure 4.6, ports 1 and 2 are general input and output terminals for the whole GaAs MESFET. Ports 3, 3', 4, 4', … and 2n+2, 2n+2' are different "internal access points" for the following analysis procedures, where n is the number of AEC.

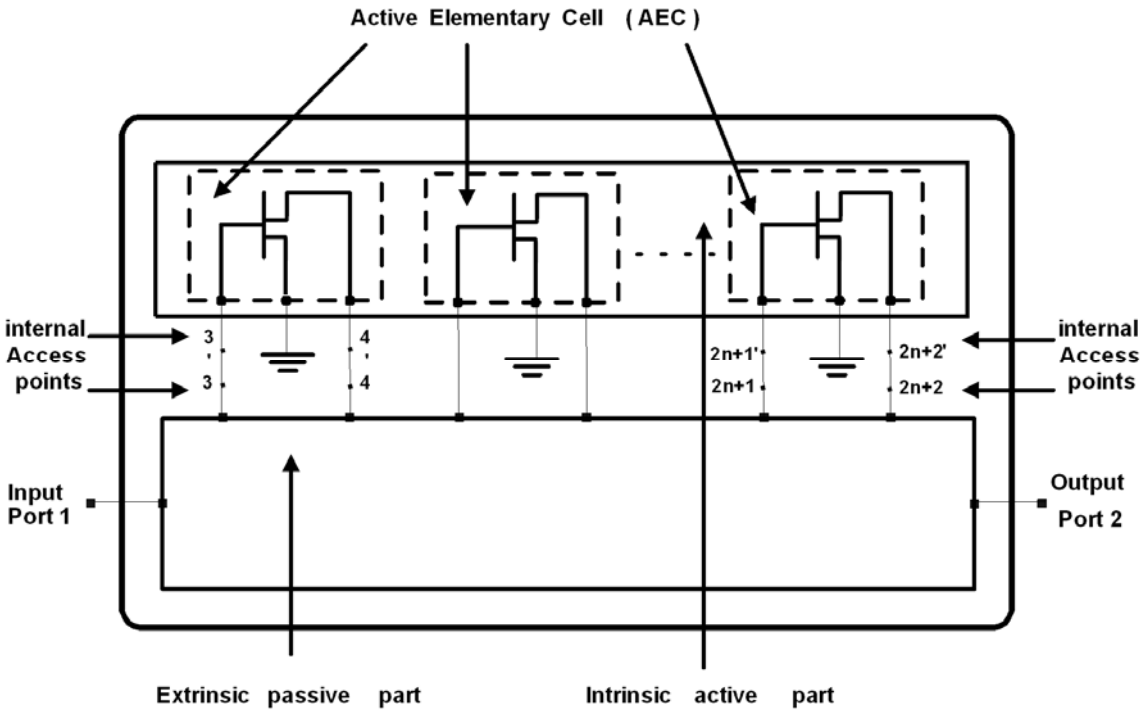


Figure 4.6 GaAs MESFET with active elementary cells (AECs)

In this novel distributed model, the passive structure of the transistor is characterized through its scattering matrix, S_{EM}, which is computed by means of electromagnetic simulation on the basis of device geometry and material parameters. Thus, electromagnetic propagation and coupling effects are considered for the passive structure. All the active elementary cells are described by the same scattering matrix, S, which can be identified once the FET transistor total scattering matrix, S_M, has been measured.

So, we have

$$\begin{bmatrix} b_1 \\ b_2 \\ : \\ : \\ b_{2n+1} \\ b_{2n+2} \end{bmatrix} = S_{EM} \begin{bmatrix} a_1 \\ a_2 \\ : \\ : \\ a_{2n+1} \\ a_{2n+2} \end{bmatrix}, \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = S_M \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}, \begin{bmatrix} b_{(2n+1)'} \\ b_{(2n+2)'} \end{bmatrix} = S \begin{bmatrix} a_{(2n+1)'} \\ a_{(2n+2)'} \end{bmatrix} \tag{4.1}$$

where

$$S_{EM}=\begin{bmatrix} S_{EMA} & S_{EMB} \\ S_{EMC} & S_{EMD} \end{bmatrix}, S_M=\begin{bmatrix} S_{M11} & S_{M12} \\ S_{M21} & S_{M22} \end{bmatrix}, \text{and } S=\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}. \quad (4.2)$$

The matrices, S_{EMA} , S_{EMB} , S_{EMC} and S_{EMD} , are obtained by the matrix decomposition of S_{EM} . The dimension of S_{EMA} is 2 by 2, S_{EMB} is 2 by 2n, S_{EMC} is 2n by 2 and S_{EMD} is 2n by 2n.

Through the "multi-port connection method" [89], we have:

$$\begin{bmatrix} b_p \\ b_c \end{bmatrix}=\begin{bmatrix} S_{pp} & S_{pc} \\ S_{cp} & S_{cc} \end{bmatrix}\begin{bmatrix} a_p \\ a_c \end{bmatrix} , \quad (4.3)$$

where

$$b_p=\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} , b_c=\begin{bmatrix} b_3 \\ \vdots \\ b_{2n+2} \\ b_{3'} \\ \vdots \\ b_{(2n+2)'} \end{bmatrix}, \; a_p=\begin{bmatrix} a_1 \\ a_2 \end{bmatrix} , \; a_c=\begin{bmatrix} a_3 \\ \vdots \\ a_{2n+2} \\ a_{3'} \\ \vdots \\ a_{(2n+2)'} \end{bmatrix} , \quad (4.4)$$

$$S_{pp}=S_{EMA}, S_{pc}=\begin{bmatrix} S_{EMB} & 0 \end{bmatrix} , S_{cp}=\begin{bmatrix} S_{EMC} \\ 0 \end{bmatrix} , S_{cc}=\begin{bmatrix} S_{EMD} & 0 \\ 0 & S_T \end{bmatrix}, \quad (4.5)$$

The dimension of S_{pc} is 2 by 4n, S_{cp} is 4n by 2, S_{cc} is 4n by 4n and S_T is 2n by 2n. And

$$S_T = \begin{bmatrix} S & & & & & \\ & \ddots & & & & \\ & & S & & & \\ & & & S & & \\ & & & & \ddots & \\ & & & & & S \end{bmatrix}, \quad \begin{bmatrix} b_3 \\ \vdots \\ b_{(2n+2)} \\ b_{3'} \\ \vdots \\ b_{(2n+2)'} \end{bmatrix} = \Gamma \begin{bmatrix} a_3 \\ \vdots \\ a_{(2n+2)} \\ a_{3'} \\ \vdots \\ a_{(2n+2)'} \end{bmatrix}, \quad \Gamma = \begin{bmatrix} 0 & I \\ I & 0 \end{bmatrix}. \tag{4.6}$$

In here, I is an identity matrix with dimension of 2n by 2n.

Finally, we can derive equations (4.7) and (4.8) below from equations (4.3) to (4.6)

$$S_p = S_M = S_{pp} + S_{pc}(\Gamma - S_{cc})^{-1} S_{cp} \quad , \tag{4.7}$$

and

$$S_{EMA} + S_{EMB}(-S_{EMD})^{-1}(S_T S_{EMD} - I)^{-1} S_{EMC} = S_M - S_{EMB}(-S_{EMD})^{-1} S_{EMC} \tag{4.8}$$

Based on equations (4.7) and (4.8), we can derive the scattering matrix S, for the intrinsic active part of GaAs MESFET at each frequency point.

4.2.3 Extraction Methodology for Intrinsic Active Part of GaAs MESFET

After s-parameter matrix of the intrinsic part has been derived, in this section, with the existing s-parameter matrix, the determination for each intrinsic component of the transistor will be discussed. As shown in figure 4.7, a standard small-signal equivalent circuit for MESFET active elementary cells is used to describe the electrical response of the intrinsic active part of a MESFET transistor.

In the equivalent circuit, drain resistance R_d and source resistance R_s have been included as parasitic model elements, because other external inductances and

capacitances in the conventional equivalent circuit can be fully taken into account by full-wave electromagnetic simulation [38]. As mentioned before in Chapter 2.2.2, although these two resistors are normally considered to be constant in commonly used models, investigation and measurements show a slight bias dependent behaviour of these resistances.

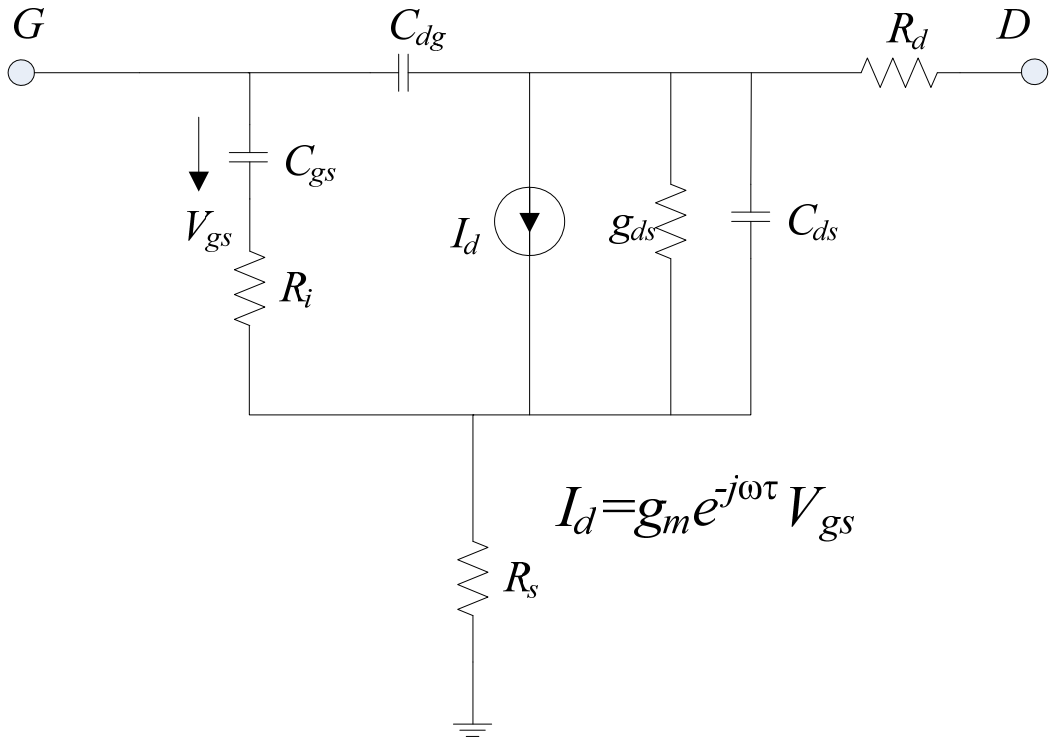


Figure 4.7 Equivalent Circuit of Active Elementary cells (AECs)

Normally there are two most common solutions to determine the elements of the intrinsic part of transistors. One is the optimization method and other is analytical method. The determination of MESFET equivalent circuit elements with optimization based approach is traditionally carried out by minimizing the error function in a way that all elements are changed simultaneously and independently by the optimization engine until the minimum of the error function is reached. However, from Figure 4.7, the adopted physically based microwave MESFET equivalent circuit model consists

of 9 elements while only a set of S-parameter can be used for known conditions under different frequencies. As a result, the optimization may be easily trapped into a local minimum which is a fundamental problem in optimization procedures. On the other hand, for analytical methods, the analytical solutions in chapter 3.3.2.1 are unavailable as two more parasitic resistors added to the traditional intrinsic equivalent circuit. Therefore, they require additional measurement steps to fix the values of all components in this equivalent circuit. Therefore, neither optimization based on data-fitting techniques nor the analytical methods could efficiently yield reliable results.

For our novel distributed small-signal model, a novel quasi-optimization data fitting approach is presented to solve the problem, which is an analytical optimizer based data-fitting technique. It is well-known that the nearer the starting values of the model parameters, the higher the probability of reaching the global minimum. Thus, to reach the global minimum, suitable starting values are necessary. This quasi-optimization is made in two steps: the first step is for analytical data extraction and the second step is for data-fitting optimization. To reduce the number of variables for analytical data extraction, the parasitic resistances R_d and R_s are ignored in the first step. Therefore, the equivalent circuit of GaAs MESFET's intrinsic active part turns to the conventional case shown in figure 3.11, which has seven intrinsic elements, and can be uniquely determined by the four intrinsic Y-parameters.

Following this, the second step is carried out. In this step, the standard MESFET intrinsic equivalent circuit (Figure 4.7) is adopted. The values of intrinsic

elements getting from the first step are used as the initial values for optimization. Since these initial values from analytical methods are very close to the real values, the optimization is very easy to arrive at a global minimum. The optimization program is realized by the commercial RF circuit design software ADS, whose schematic in ADS is shown as Figure 4.8. From this figure, it is clear that the optimization program resolve the elements of the small signal equivalent circuit through minimizing the difference between measured and computed S-parameters versus a wide frequency range from 1 to 40 GHz.

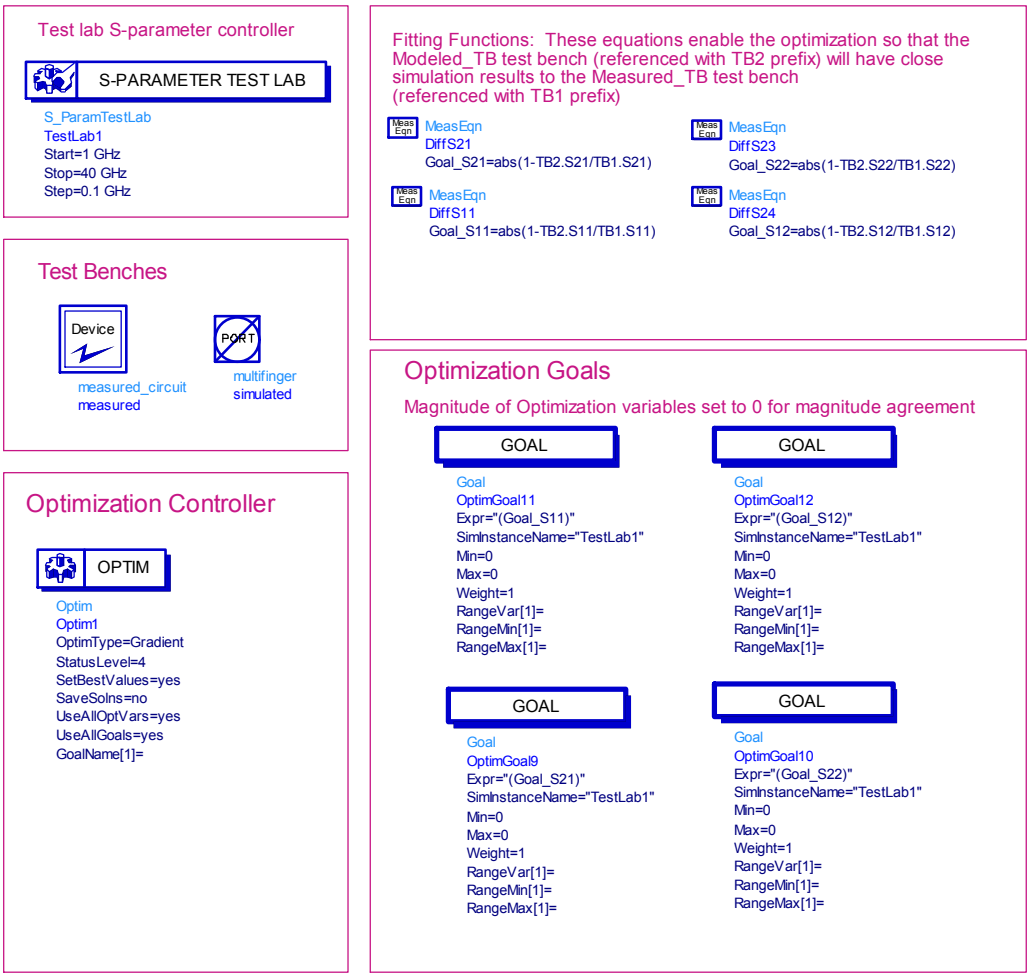


Figure 4.8 Optimization program for the S-parameter fitting

4.2.4 Extraction Methodology for Intrinsic Active Part of GaAs HBT

A standard hybrid-π equivalent circuit for bipolar transistor small-signal modelling is used to describe the electrical response of the intrinsic active part of a HBT transistor. Several explicit analytical expressions are derived, which can be used to determine all the intrinsic model elements. For the first time, the values of the entire GaAs HBT intrinsic model elements used in the active elementary cells can be extracted through these explicit analytical expressions.

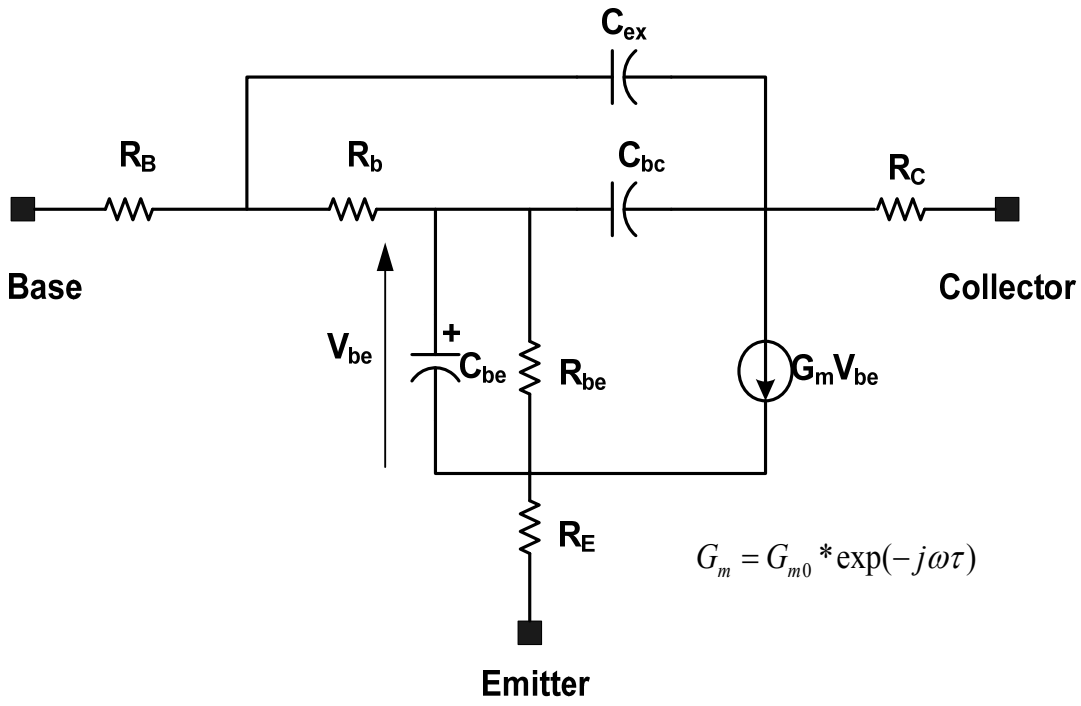


Figure 4.9 A hybrid-π equivalent circuit for HBT small-signal modelling.

Figure 4.9 shows the typical hybrid-π equivalent circuit for HBT small-signal modelling. In the equivalent circuit, only emitter resistance R_E, external base resistance R_B and collector resistance R_C have been included as extrinsic model

elements, because other parasitic inductances and capacitances in the conventional equivalent circuit can be fully taken into account by full-wave electromagnetic simulation [99].

Based on the equivalent circuit we adopted, we can determine all Z-parameters as follows [102]:

$$Z_{11} = \frac{R_b Z_1}{R_b + Z_1 + Z_2} + \frac{R_b Z_2}{(1 + G_m Z_3)(R_b + Z_1 + Z_2)} + \frac{Z_3}{1 + G_m Z_3} + R_B + R_E, \tag{4.9}$$

$$Z_{12} = \frac{R_b Z_2}{(1 + G_m Z_3)(R_b + Z_1 + Z_{2)}} + \frac{Z_3}{1 + G_m Z_3} + R_E, \tag{4.10}$$

$$Z_{21} = \frac{R_b Z_2 - G_m Z_3 Z_1 Z_2}{(1 + G_m Z_3)(R_b + Z_1 + Z_2)} + \frac{Z_3}{1 + G_m Z_3} + R_E \quad , \tag{4.11}$$

$$Z_{22} = \frac{R_b Z_2 + Z_1 Z_2}{(1 + G_m Z_3)(R_b + Z_1 + Z_2)} + \frac{Z_3}{1 + G_m Z_3} + R_C + R_E \quad , \tag{4.12}$$

where

$$Z_1 = \frac{1}{j\omega C_{ex}}, \tag{4.13}$$

$$Z_2 = \frac{1}{j\omega C_{bc}}, \tag{4.14}$$

and

$$Z_3 = R_{be}\left(\frac{1 - j\omega C_{be} R_{be}}{1 + \omega^2 C_{be}^2 R_{be}^2}\right). \tag{4.15}$$

Let

$$A = Z_{11} - Z_{12}, \tag{4.16}$$

$$B = Z_{22} - Z_{21}, \tag{4.17}$$

$$C = Z_{11} + Z_{22} - Z_{12} - Z_{21}, \tag{4.18}$$

and

$$D = Z_{11} + Z_{21} - Z_{12} - Z_{22}. \tag{4.19}$$

Putting equations (4.13) - (4.19) into equations (4.9)-(4.12), we can get

$$\mathrm{Re}(C) - R_B - R_C = (R_B - \mathrm{Re}(D) - R_C) + 2\omega^2 R_b C_{bc}, \tag{4.20}$$

$$\mathrm{Im}(C) = -2\omega R_b C_{bc}(\mathrm{Re}(D) + R_C - R_B) - \mathrm{Im}(D), \tag{4.21}$$

$$\mathrm{Re}(A) - R_B = -\omega\,\mathrm{Im}(B) R_b C_{bc} \tag{4.22}$$

$$\mathrm{Im}(A) = [\mathrm{Re}(B) - R_C][\omega R_b C_{bc}] \tag{4.23}$$

$$[\mathrm{Re}(C) + \mathrm{Re}(D) - 2R_B][\mathrm{Re}(D) - R_B + R_C] = -\omega[\mathrm{Im}(C) + \mathrm{Im}(D)], \tag{4.24}$$

and

$$R_B = \mathrm{Re}(A) + \frac{\mathrm{Im}(A) \cdot \mathrm{Im}(B)}{\mathrm{Re}(B) - R_C} \tag{4.25}$$

From equations (4.24) to (4.25), we can obtain the values of R_B and R_C. In addition, we have

$$\frac{R_b C_{bc}(C_{ex} + C_{bc})}{(C_{ex} + C_{bc})^2 + \omega^2 R_b{}^2 C_{ex}{}^2 C_{bc}{}^2} + R_B = \mathrm{Re}(A) \tag{4.26}$$

$$\frac{-\omega R_b^2 C_{ex} C_{bc}^2}{(C_{ex} + C_{bc})^2 + \omega^2 R_b{}^2 C_{ex}{}^2 C_{bc}{}^2} = \mathrm{Im}(A) \tag{4.27}$$

and

$$\frac{-R_b C_{ex} C_{bc}}{\omega^2 R_b{}^2 C_{ex}{}^2 C_{bc}{}^2 + (C_{ex} + C_{bc})^2} + R_C = \mathrm{Re}(B), \tag{4.28}$$

$$\frac{-(C_{ex}+C_{bc})}{\omega^3 R_b{}^2 C_{ex}{}^2 C_{bc}{}^2+\omega\ (C_{ex}+C_{bc})^2}=\mathrm{Im}(B) \tag{4.29}$$

From equations (4.25) and (4.29), we can obtain the values of R_b, C_{ex} and C_{bc}.

For the small-signal transistor operating condition, we have from [103]:

$$G_{m0}=\frac{qI_c}{KT}, \tag{4.30}$$

$$R_{be}=\frac{\beta}{G_{m0}} \tag{4.31}$$

$$G_m=G_{m0}\exp(-j\omega\tau) \tag{4.32}$$

and

$$\tau=-\frac{1}{\omega}tg^{-1}[\frac{\mathrm{Im}(G_m/G_{m0})}{\mathrm{Re}(G_m/G_{m0})}]. \tag{4.33}$$

Therefore, we can obtain the values of C_{be}, G_m and R_E from equations (4.9) to (4.12) and (4.30) to (4.33).

4.3 Model Realization in ADS

The final step of this distributed modelling is to combine the extrinsic passive and intrinsic active parts together into one practicable device which can be implemented in the RF circuit design software Agilent-ADS. The extrinsic part, exported from IE3D as several data items, is connected with the equivalent active circuits obtained by the quasi-optimization program. As shown in Figure 4.10 and 4.11 below, the final model of this 2-finger GaAs FETs is a 2-port component which can be used in further MMIC design.

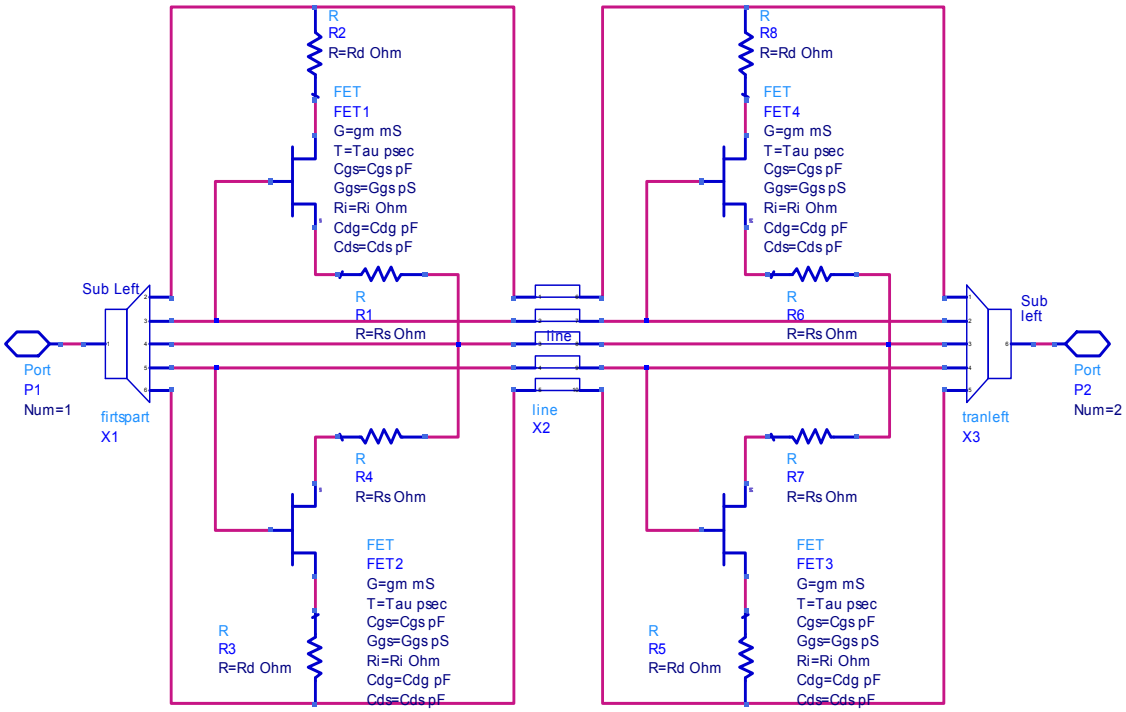


Figure 4.10 A small-signal distributed model of GaAs MESFET in ADS

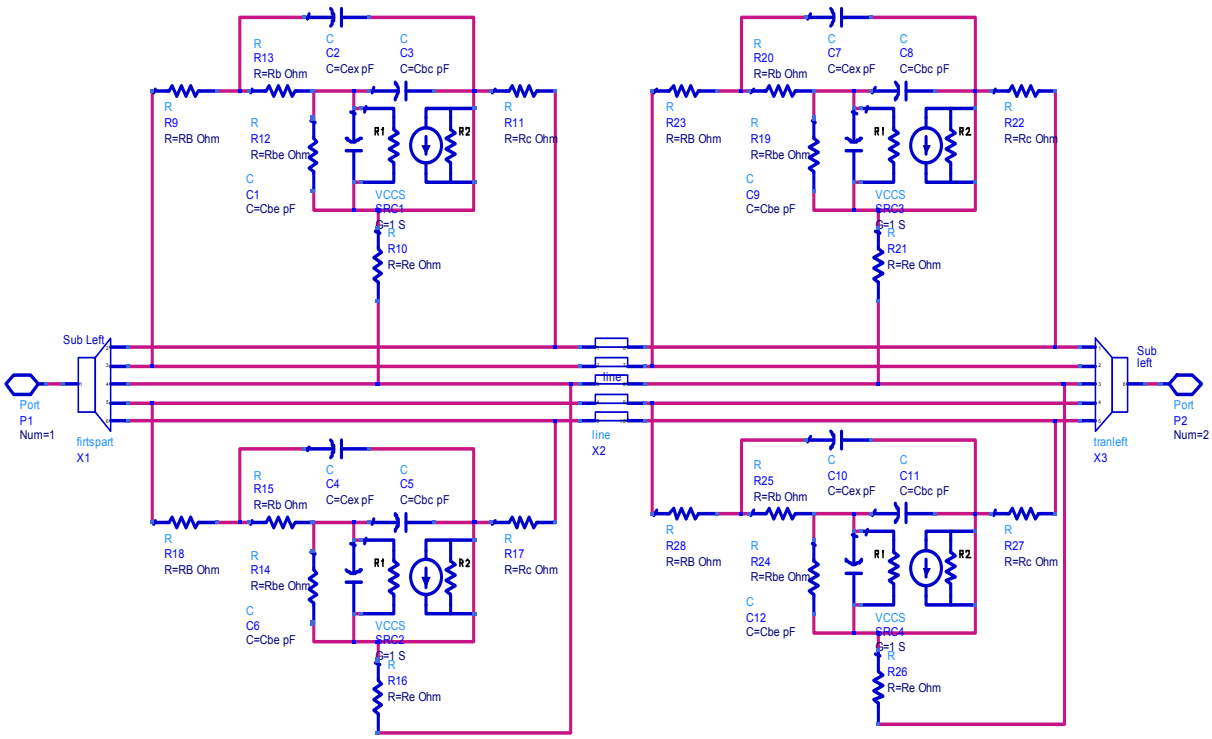


Figure 4.11 A small-signal distributed model of GaAs BJT in ADS

4.4 Model Verification and Discussion

4.4.1 Model Verification

In order to verify this novel distributed model, GaAs MESFETs with different structures (4×100μm, 8×125μm, and 16×125μm) were measured and simulated to validate the proposed approach. The S-parameters of these MESFETs were measured directly on-wafer with 50-Ohm input/output impedance up to frequency of 40 GHz using a pulse modulated high frequency measurement system. The biasing condition is V_{ds}=5V and V_{gs}=-0.5V for 4×100μm and V_{ds}=7V and V_{gs}=-0.5V for 8×125μm and 16×125μm. Through the geometric parameters of the device GDS files provided by the foundry, the scattering matrices of the extrinsic passive structures were computed by using IE3D electromagnetic simulator. Due to the small structure involved, the time taken by the IE3D computation is only a few seconds (less than 10 seconds). In order to calculate the S-matrix of each active elementary cell, MATLAB programs have been developed by using the calculation method described in Chapter 4.2.2. The ADS program based on the quasi-optimization method has been used to derive the values for all the small-signal model elements. Finally, simulation in the frequency domain was implemented by using Agilent-ADS simulator.

Figures 4.12 to 4.14 are the comparisons between the measured S-parameters and the simulated results. From these figures, it is observed that relatively good agreement between measured and simulated data can be achieved. As all the high frequency coupling effects and add on parasitic elements of GaAs MESFET have been taken

into account by the accurate EM simulation procedure, the matching performance of this novel model could maintain satisfied results from the low frequency range to the concerned high frequency region.

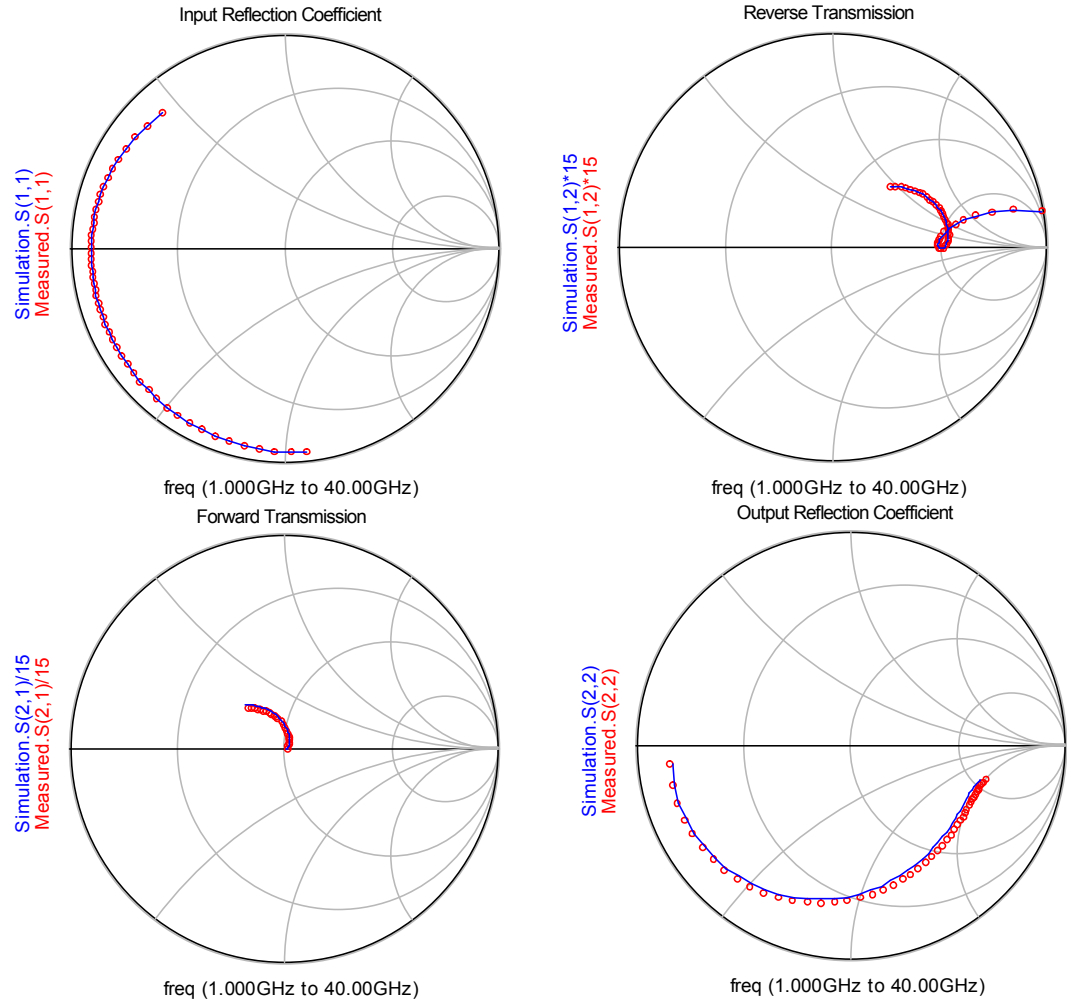
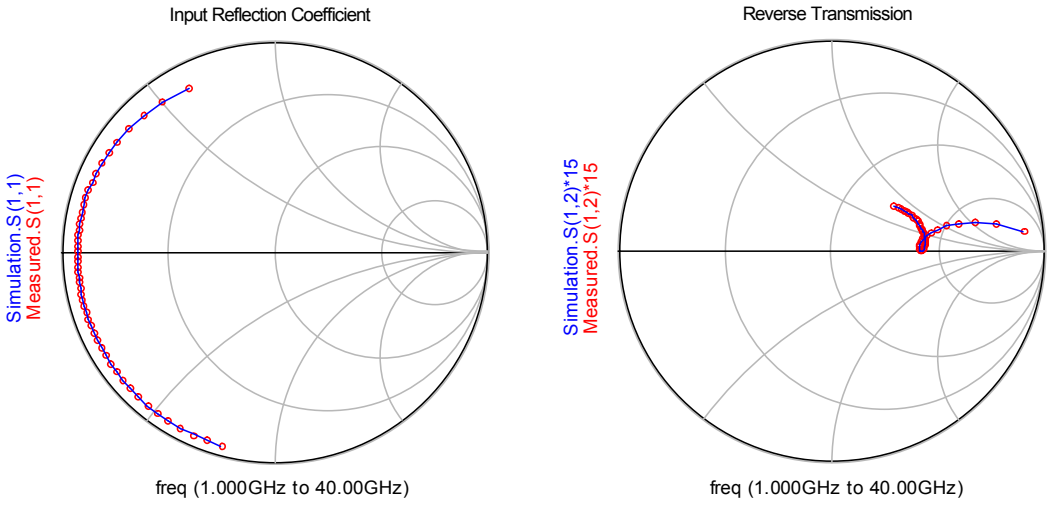


Figure 4.12 Measured (circle) and simulated (solid) S-parameters for 4-finger GaAs MESFET (V_{gd}=5V and V_{gs}=-0.5V, gate-width = 100μm)



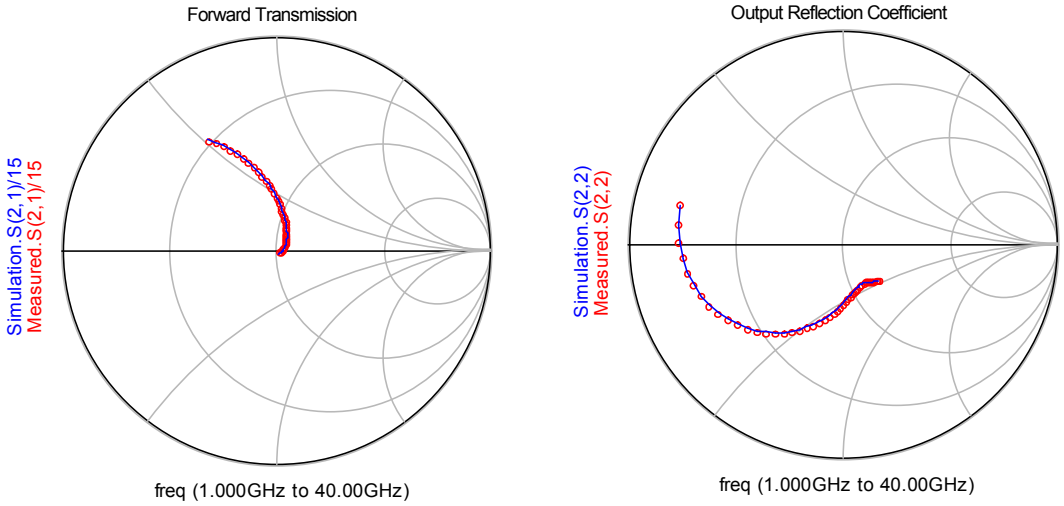


Figure 4.13 Measured (circle) and simulated (solid) S-parameters for 8-finger GaAs MESFET (V_{gd}=7V and V_{gs}=-0.5V, gate-width = 125µm)

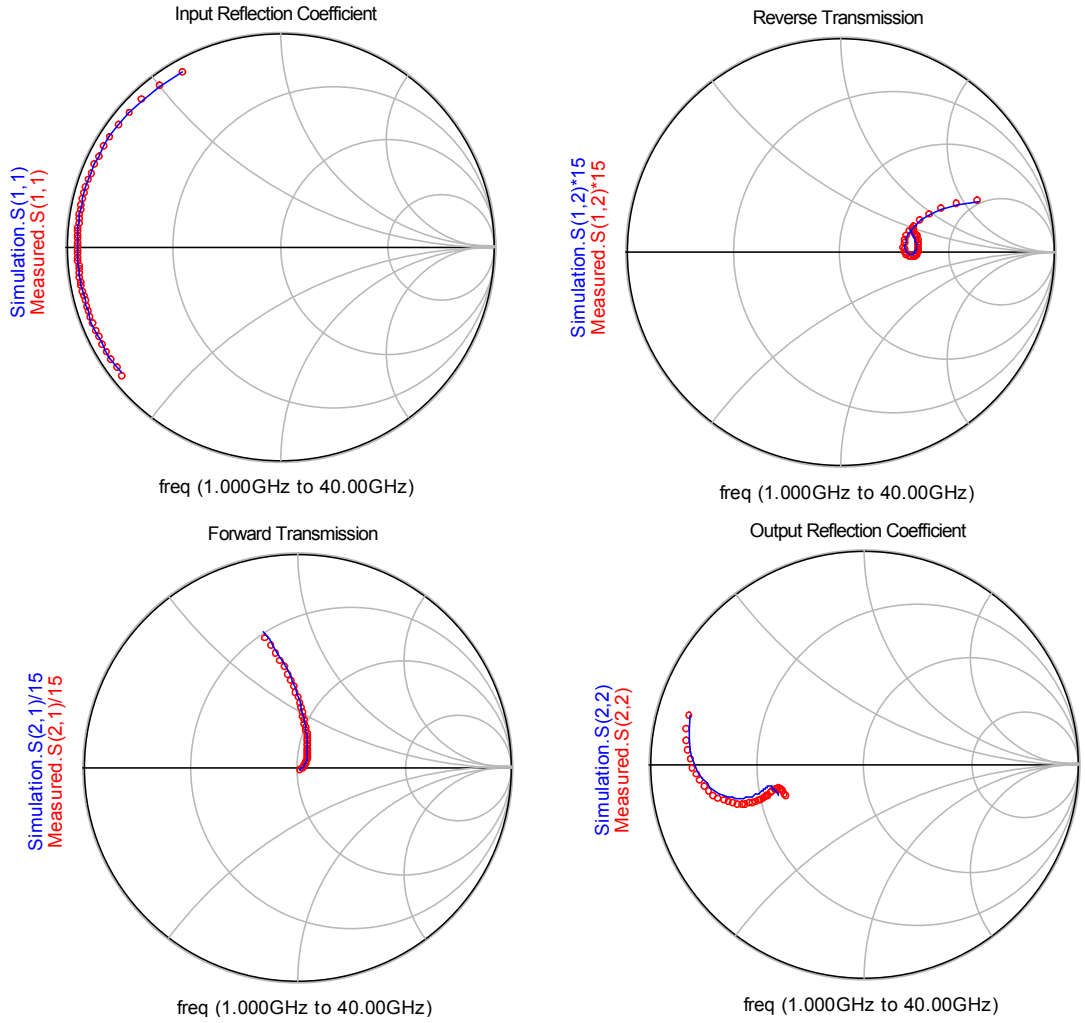


Figure 4.14 Measured (circle) and simulated (solid) S-parameters for 16-finger GaAs MESFET (V_{gd}=7V and V_{gs}=-0.5V, gate-width = 125µm)

To further verify the overall and the high frequency fitting performance of this new distributed model, the maximum fitting error and the RMS error of S-parameter obtained from the new model are listed in Table 4.1 together with the most commonly used traditional model Dambrine's and White's models [11] [73] for comparison. The calculation is made under six bias levels for V_{gs} (V_{gs}=-0.5V, -0.4V, -0.3V, -0.2V –0.1V, 0.0V), while V_{ds} changes from 0.0V to 10.0V (on-wafer 4×100μm device), totally 606 biasing points are taken within this range. The first two columns in the table represent the fitting error in the low frequency region from 1 GHz to 20 GHz. The second two columns show the model error in the high frequency region from 21 GHz to 40 GHz, and the last two columns give the error for the entire working frequency region.

It can be seen from Tables 4.1 that the new distributed model gives remarkable improvement in accuracy over the two traditional small signal models over the entire device working frequency region, both maximum fitting error and RMS error are greatly reduced. Based on Table 4.1, the novel distributed model gives smallest RMS error at low frequency range as compared to other two commonly used small signal models. Moreover, the matching performance of this new distributed model in high frequency region is much better than the results given by the other two models in this region. This is because complicated coupling effects and parasitic components are employed in the novel model for its whole working frequency range. In addition, quasi-optimization program is introduced to give better fit. Considering measurement uncertainty, this novel distributed model is very accurate for its overall performance.

Table 4.1 Max Error and RMS Error of Modeled S-parameter, Equivalent Circuit Elements Extracted from novel distributed model and Dambrine's model

V_{gs}=-2.0-0.5V, V_{ds}=0.0-4.0V, f=1~40GHz

	Freq = 1~20 GHz		Freq = 21~40 GHz		Freq = 1~40 GHz	
	Max Err (%)	RMS. Err (%)	Max Err (%)	RMS. Err (%)	Max Err (%)	RMS. Err (%)
Dambrine's Method						
S_{11}	6.28	1.31	25.80	5.32	25.80	4.63
S_{12}	8.96	6.19	18.21	10.32	18.21	7.61
S_{21}	10.84	4.23	23.17	9.71	23.71	6.63
S_{22}	6.96	3.59	24.34	7.41	24.34	5.39
White's Method						
S_{11}	7.43	1.44	24.74	7.45	24.74	4.95
S_{12}	9.66	5.41	19.52	10.75	19.52	8.67
S_{21}	11.41	3.93	21.93	11.40	21.93	8.76
S_{22}	6.07	3.23	21.55	9.23	21.55	5.89
Novel Distributed Model						
S_{11}	3.15	0.67	4.61	1.45	4.61	0.83
S_{12}	5.59	1.21	6.91	1.48	6.91	1.20
S_{21}	6.78	0.82	7.60	0.88	7.60	0.86
S_{22}	1.92	1.54	2.26	2.41	2.26	1.72

As the similarity of issues, this novel method can also be adopted for GaAs HBT small signal modelling. Therefore, AlGaAs/GaAs HBTs with different structures were measured and simulated to validate the proposed approach. The S-parameters of HBTs were measured directly on-wafer up to frequency of 40GHz using a pulse modulated high frequency measurement system. The biasing condition is V_{BE}=1.34V, V_{CE}=3.0V. The analytical equations in Chapter 4.2.4 have been used to derive the values for all the small-signal model elements. Finally, simulation in the whole frequency domain is also implemented by using Agilent-ADS simulator.

First in order to check the fitting performance of our distributed model, we choose HBT transistors with two different structures, whose emitter sizes are 2×3μm×20μm and 2×3μm×40μm. Figures 4.15 to 4.16 are the comparisons between the measured S-parameters and the simulated results. From these figures, it is observed that relatively good agreement between measured and simulated data can be achieved. Second, in order to check the actual scaling capability of our proposed modelling method, the model was adopted to predict the actual electrical behaviors of various HBT transistors, which are different from those used in the previous steps. The prediction was carried out on the basis of the model element values of active elementary cells which are already known. Figures 4.16 to 4.17 show the measured and predicted S-parameters for the HBTs (4×3μm×40μm and 6×3μm×40μm). The prediction above was carried out on the basis of known active elementary cell of the HBT whose size is 2×3μm×40μm. From these figures, the prediction and synthesis capabilities of our proposed model can be verified.

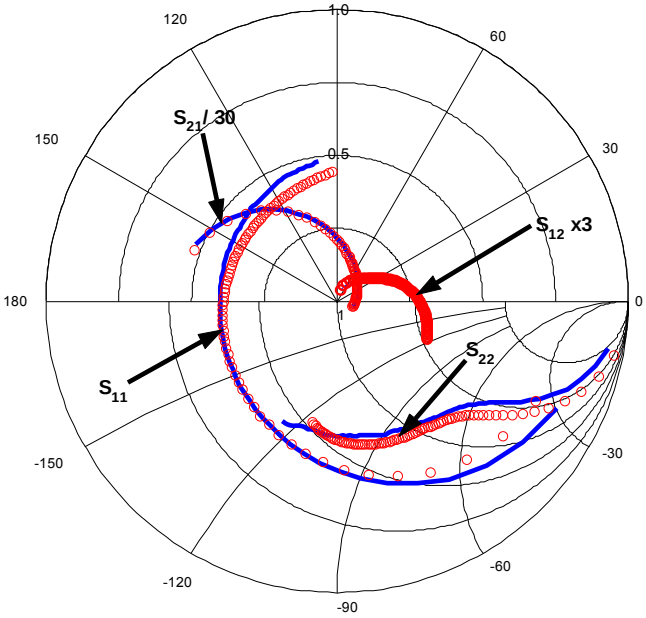


Figure 4.15 Measured (circle) and simulated (solid) S-parameters for HBT (2×3μm×20μm).

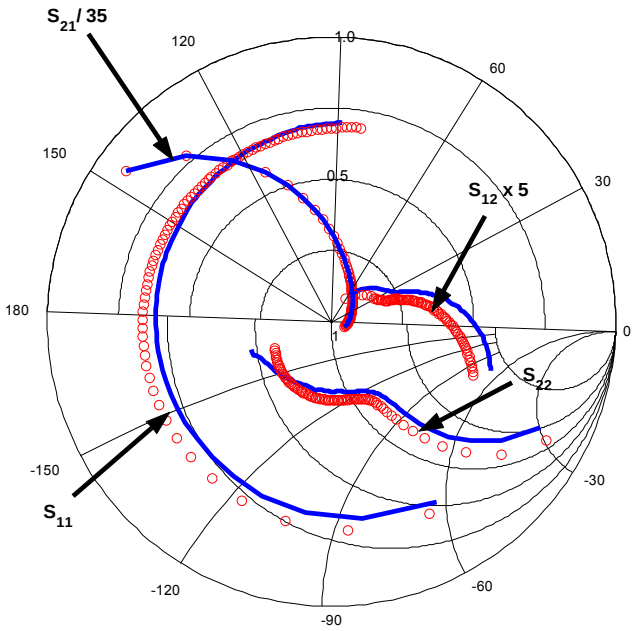


Figure 4.16 Measured (circle) and simulated (solid) S-parameters for HBT (2×3μm×40μm).

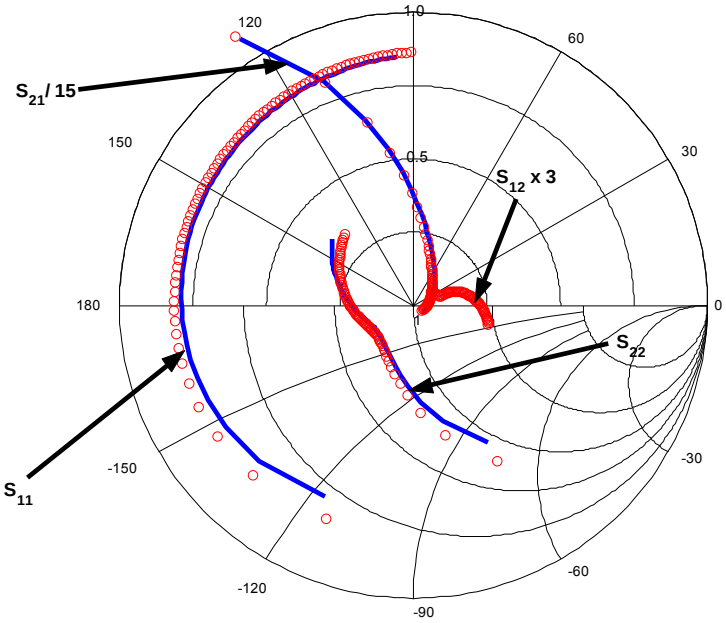


Figure 4.17 Measured (circle) and simulated (solid) S-parameters for HBT (4×3μm×40μm).

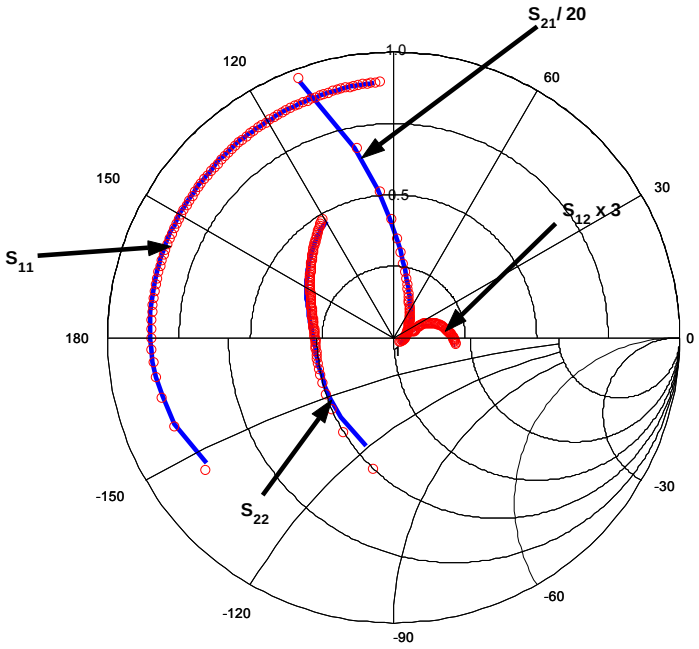


Figure 4.18 Measured (circle) and simulated (solid) S-parameters for HBT (6×3μm×40μm).

4.4.2 Discussion

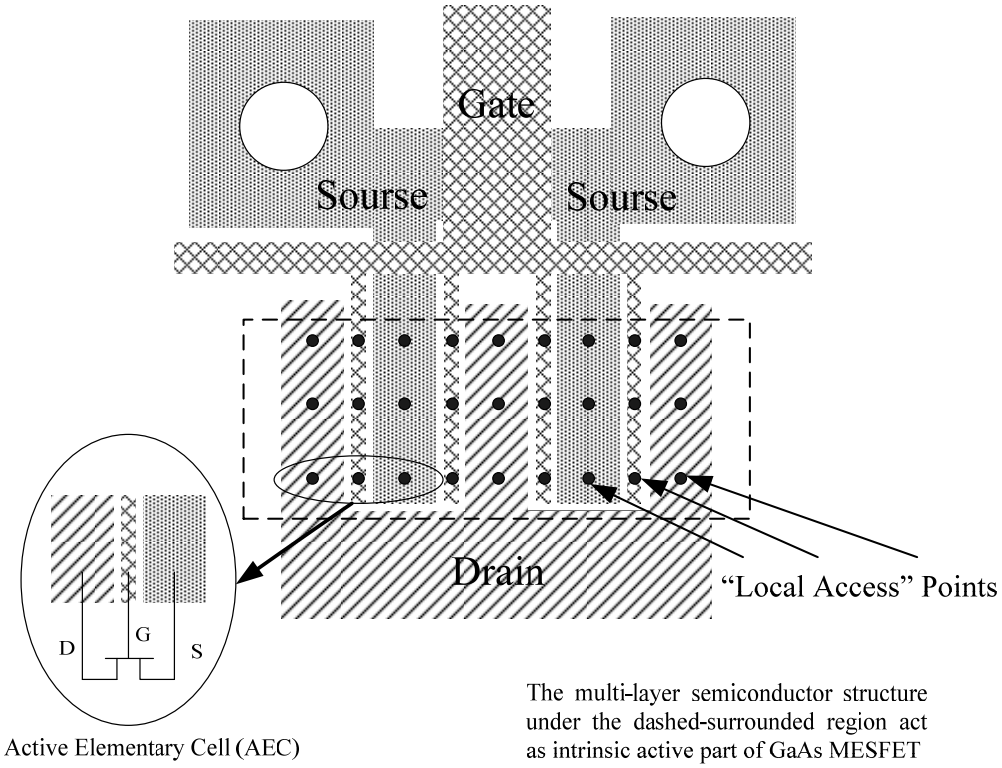


Figure 4.19 A typical MESFET transistor layout and an equivalent representation of the FET extrinsic and intrinsic parts

There are several possible reasons for the small discrepancies observed between measured data and simulated results. First, in our electromagnetic simulation, it is assumed that a planar isotropic semi-insulating GaAs substrate locates beneath the transistor metal structure. In reality, the MESFET/HBT is fabricated with a non-planar multi-layer semiconductor structure. Moreover, in our method, the effect of current flow on the electromagnetic field distribution under the non-planar transistor passive structure has been omitted. Second, in our method, one reference plane for Active Elementary Cells (AECs) has been assumed and the finger structure of the transistor has been simplified. One of the reasons for selecting one "local access point" along

the device finger is for simplicity in our analysis. In our approach, we fixed the local access point at the centre of each fingers as shown in the inset of Figure 4.19 so as to speed up the computation. Furthermore, the effect of gate grounding via holes to the location of local access points needs to be investigated further.

4.5 Conclusion

A novel approach to the distributed small-signal modelling of GaAs MESFETs has been proposed, with the purpose of taking into account the various wave-effects related to transistor metallic geometry. The modelling method is based on accurate electromagnetic simulation of extrinsic passive part of a MESFET transistor. Meanwhile, the intrinsic active part of a MESFET transistor is characterized by a modified small-signal model for the transistor. The significance of our proposed modelling method is that it can provide a more comprehensive and efficient tool for transistor optimization and more accurate performance prediction for various transistors with different layout structures.

The proposed novel method is based on the electromagnetic simulation of metallic parts of the device and biased S-parameter measurements of a GaAs MESFET. Then, the S-parameters of the intrinsic part of the transistor are calculated by using the novel quasi-optimization procedures. In general, our method is useful especially for those GaAs MESFET large-sized devices at millimetre-wave frequency. The proposed method can provide attractive information about the transistor with arbitrary metallization. As the need for any additional database is omitted and design

flexibility for the device design has been enhanced, the proposed method is very useful to those MMIC designers to obtain accurate predictions of their various designs. Based on electromagnetic simulation, this method can be used to include complex coupling effects in device layouts and to predict the electrical characteristics of unconventional device structures for better MMIC performance. Also, this method is accurate enough to describe many full-wave effects which cannot be covered by the conventional parasitic networks. Therefore, this method can be regarded as a preliminary step for the global, fully layout and process oriented design approach. In our proposed modelling method, actually any linear or nonlinear, description of a FET transistor, which includes lumped or distributed equivalent elements, can be adopted.

Chapter 5

A New Large-Signal Model for GaAs MESFETs

5.1 Introduction

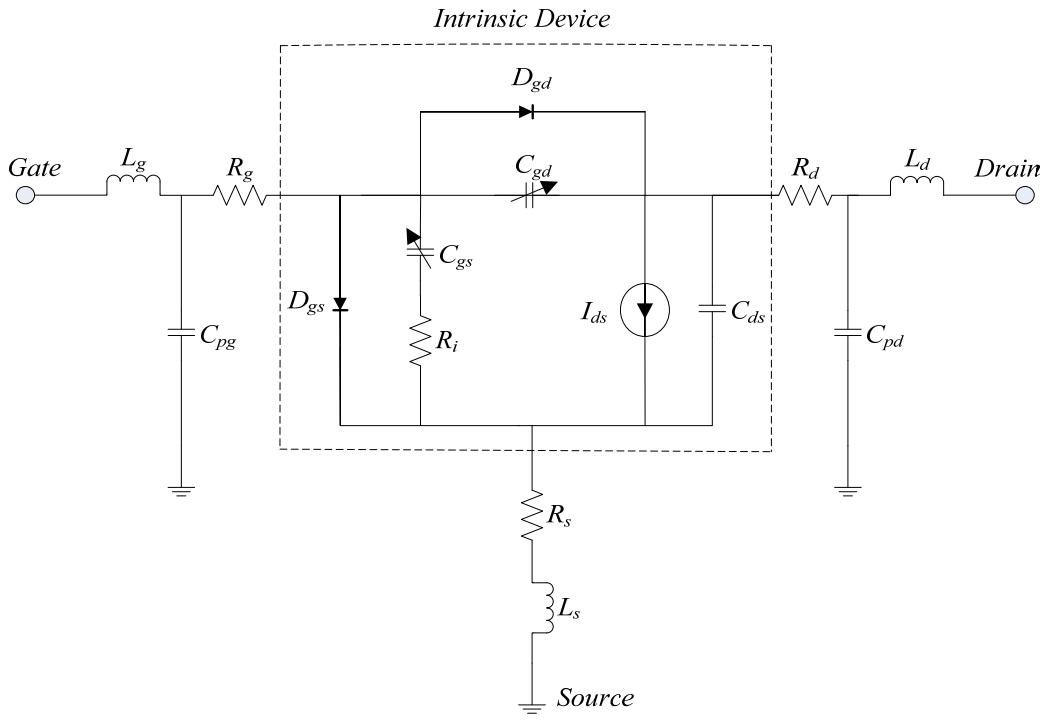


Figure 5.1 Equivalent circuit for GaAs MESFET large-signal model

Figure 5.1 shows a typical equivalent circuit for a MESFET large-signal model. The intrinsic device is enclosed by the dashed-line box, which also defines the

intrinsic device plane. All the nonlinear elements lie within the dashed-line box. Among these nonlinear characteristics, the drain current I-V characteristic and gate charges are the most important GaAs MESFET nonlinear properties. Their accuracies are critical to precisely model the nonlinear characteristic even the overall performance of the MESFET device.

In this chapter, several commonly used drain current models are first investigated with an improved drain current model. Subsequently, to illustrate its advantages, the performances of the new model and other available models are compared with the measured device response. Then, following the discussion of two famous existing gate charge models, a new gate charge model is proposed. The new gate charge model is very accurate in describing device junction capacitances under various device operating conditions. The performance prediction in the linear region, saturation knee region, sub-threshold region and at V_{ds}=0 is greatly improved over the conventional models. The new charge model formulation and its derivatives are continuous. Moreover, it obeys the terminal charge conservation law, which helps to solve the non-convergence problem in simulation. Finally, GaAs MESFET device measurement data is employed to verify the accuracy of the new gate charge model. Furthermore, the performance of the new charge model is also compared with other models to validate its advantage and accuracy.

5.2 A New Drain Current Model for GaAs MESFET

5.2.1 An Examination of the Existing Empirical Drain Current Models

A variety of analytical models have been developed to describe the drain current operation characteristics of MESFET. All of these models are capable of expressing the device properties with some success. In most of the current models as in references [40, 50, 53, 56], the drain current expressions can be described as the product of two functions:

$$I_{ds}(V_{gs},V_{ds}) = F_1(V_{gs},V_{ds}) \cdot F_2(V_{gs},V_{ds}) \tag{5.1}$$

where, both F_1 and F_2 are functions of V_{gs} and V_{ds}. The first function is mainly aimed at describing the drain current variation with the gate voltage, while the second term focuses on the modelling of drain current variation with the drain voltage. Empirical Drain Current models often adopt the hyperbolic tangent dependence for $F_2(V_{gs},V_{ds})$.

In this section, several commonly used drain current models are investigated. They are Curtice-Quadratic model [46, 53], Chalmers model [56], and Advanced Curtice-Quadratic model [53]. All of these models describe the drain current characteristics in the form of equation 5.1. The drain current expressions of some existing GaAs MESFET models are listed in Table 5.1. A detailed model formulation of each model can be found in Appendix A.

Table 5.1 Drain Current Expressions of Some Existing GaAs MESFET Models

Model	Drain current expression
Curtice-Quadratic	$I_{ds} = \beta(V_{gs} - V_{T0})^2(1+\lambda V_{ds})\tanh(\alpha V_{ds})$
Chalmers	$I_{ds} = I_{pk}\left[1+\tanh(\psi)\right](1+\lambda V_{ds})\tanh(\alpha V_{ds})$ $\psi = P_1(V_{gs} - V_{pk}) + P_2(V_{gs} - V_{pk})^2 + P_3(V_{gs} - V_{pk})^3 + \ldots$
Advanced Curtic-Quadratic	$I_{ds} = \dfrac{\beta}{(1+\mu_{crit}V_{gst})}(V_{gs} - V_{T0} - \gamma V_{ds})^{V_{gexp}}(1+\lambda V_{ds})\tanh(\alpha V_{ds})$

5.2.2 An Improved Drain Current Model

As shown in Table 5.1, these commonly used empirical nonlinear drain current expressions proposed by Curtice model [46, 53] and Chalmers model [56] are all using the format of I_{pk}= A*(1+λV_{ds})*tanh(αV_{ds}) to describe the drain-source current performance. The first part A of the equation is used to model the relationship between the maximum drain-source current increment vs V_{ds} & V_{gs}, whilst α determines the voltage at which the drain current characteristics saturate, and λ is the channel length modulation parameter related to the drain conductance. Generally, the shorter the gate length is, the greater the slope of Ids. In all these proposed models, α and λ are simulated as constants, but from the measured data, we can observe that, in fact, the slope of Ids in the saturation region, varies with V_{gs}. The change of the

channel length modulation parameter is partly due to the change of channel shape at different dc bias. As such, we propose the following power series function to substitute for the constants α and λ:

$$\alpha = a_1(V_{gs} - V_1) + a_2(V_{gs} - V_1)^2 + \ldots \tag{5.2}$$

$$\lambda = b_1(V_{gs} - V_2) + b_2(V_{gs} - V_2)^2 + \ldots \tag{5.3}$$

where a_0, a_1, a_2, b_0, b_1, b_2, and V_1, V_2 are the matching parameters. Therefore, our new drain current revised model is shown as below:

$$I_{ds} = \frac{\beta}{\left(1 + \mu(V_{gs} - V_{T0new})\right)}(V_{gs} - V_{T0new})^{V_{gexp}}(1 + \lambda_{new}V_{ds})\tanh(\alpha_{new}V_{ds}) \tag{5.4}$$

$$\alpha_{new} = a_1(V_{gs} - V_1) + a_2(V_{gs} - V_1)^2 + a_3(V_{gs} - V_1)^3 \tag{5.5}$$

$$\lambda_{new} = b_1(V_{gs} - V_2) + b_2(V_{gs} - V_2)^2 + b_3(V_{gs} - V_2)^3 \tag{5.6}$$

$$V_{T0new} = V_{T0} + \gamma V_{ds} \tag{5.7}$$

5.2.3 Comparison of Varies Drain Current Models

A $6 \times 125\mu m$, and a $16 \times 125\mu m$ sub-micron gate-length MESFET devices (wafer device, gate length is 0.18μm) are used to verify the improved drain current model. Theire S-parameter data are measured under multi-bias condition. The small-signal equivalent circuit models are extracted using the analytical extraction method. All the parasitic element values are kept constant in the large-signal model. The extracted parasitic element values are listed in Table 5.2 and Table 5.3.

Table 5.2 Parasitic Element Values of the Small-signal Equivalent Circuit
(6×125μm GaAs MESFET Wafer device)

C_{pg} (fF)	C_{pd} (fF)	L_g (pH)	L_d (pH)	L_s(pH)	R_s(Ω)	R_g(Ω)	R_d(Ω)
132.9	130.1	79.62	48.37	18.46	2.17	1.54	0.43

Table 5.3 Parasitic Element Values of the Small-signal Equivalent Circuit
(16×125μm GaAs MESFET Wafer device)

C_{pg} (fF)	C_{pd} (fF)	L_g (pH)	L_d (pH)	L_s(pH)	R_s(Ω)	R_g(Ω)	R_d(Ω)
94.8	122.5	93.64	160.56	53.46	1.58	2.76	1.84

Pulsed DC I-V characteristics of the device are measured at the extrinsic bias plane. After de-embedding of the parasitic elements, DC I-V characteristics at intrinsic device plane are obtained. The large signal model parameters are extracted from the drain current I-V data at the intrinsic device plane, and are listed in Table 5.4 and Table 5.5 respectively for the 6×125μm and 16×125μm GaAs MESFET. All the parameter extractions are performed by an in-house developed software running under MATLAB® by MathWorks. A simplex algorithm is used for the optimization.

Table 5.4 Model Parameters for the improved drain current model
(6×125μm GaAs MESFET)

β	μ_{crit}	γ	$VGEXP$	V_1	V_2
0.12	0.15	0.012	1.53	-2.59	-1.6
a_1	a_2	a_3	b_1	b_2	b_3
0.69	0.036	-0.028	-0.09	0.10	-0.03

Table 5.5 Model Parameters for the improved drain current model

(16×125μm GaAs MESFET)

β	μ_{crit}	γ	$VGEXP$	V_1	V_2
0.33	0.23	0.005	1.89	-3.86	-2.1
a_1	a_2	a_3	b_1	b_2	b_3
0.79	-0.18	-0.012	-0.14	0.11	-0.02

Figure 5.2 and 5.3 show the comparison between the modeled drain current with the measured data of these two high-power GaAs MESFET respectively.

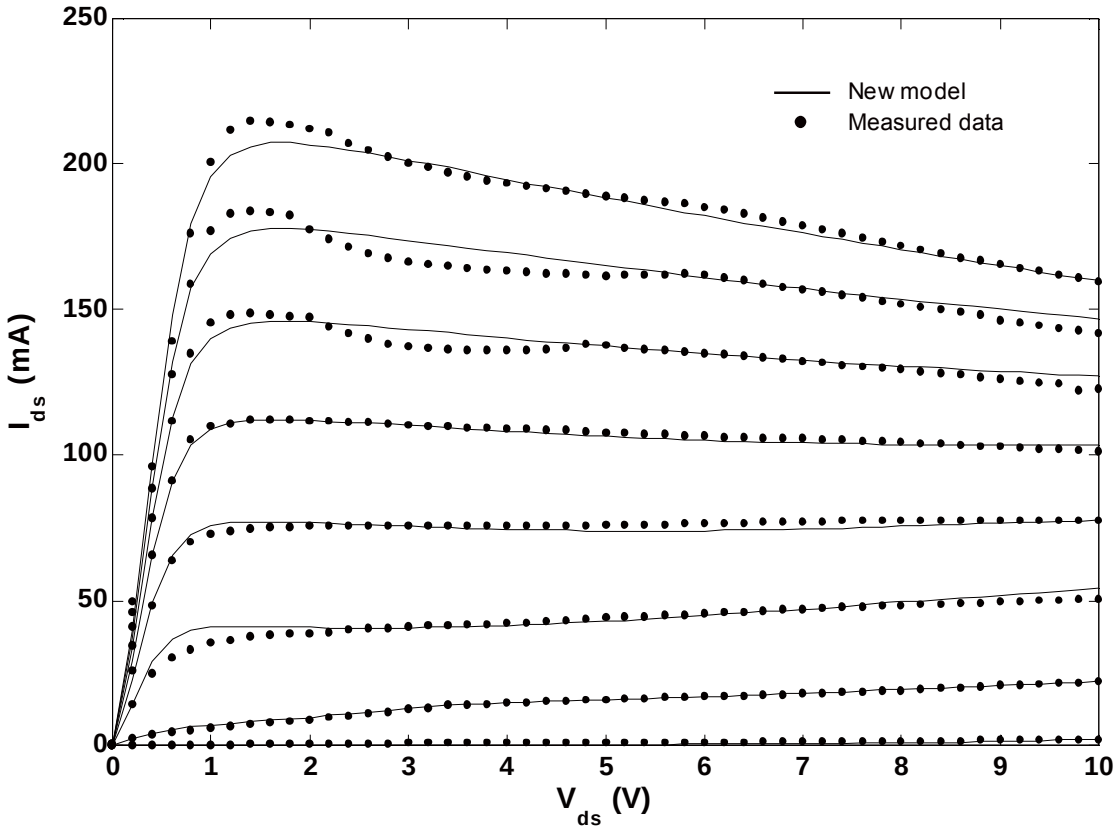


Figure 5.2 Comparison of measured and modeled drain current characteristics by the new model, 6×125μm MESFET wafer device, V_{gs}=-3.1 V – 0.5V.

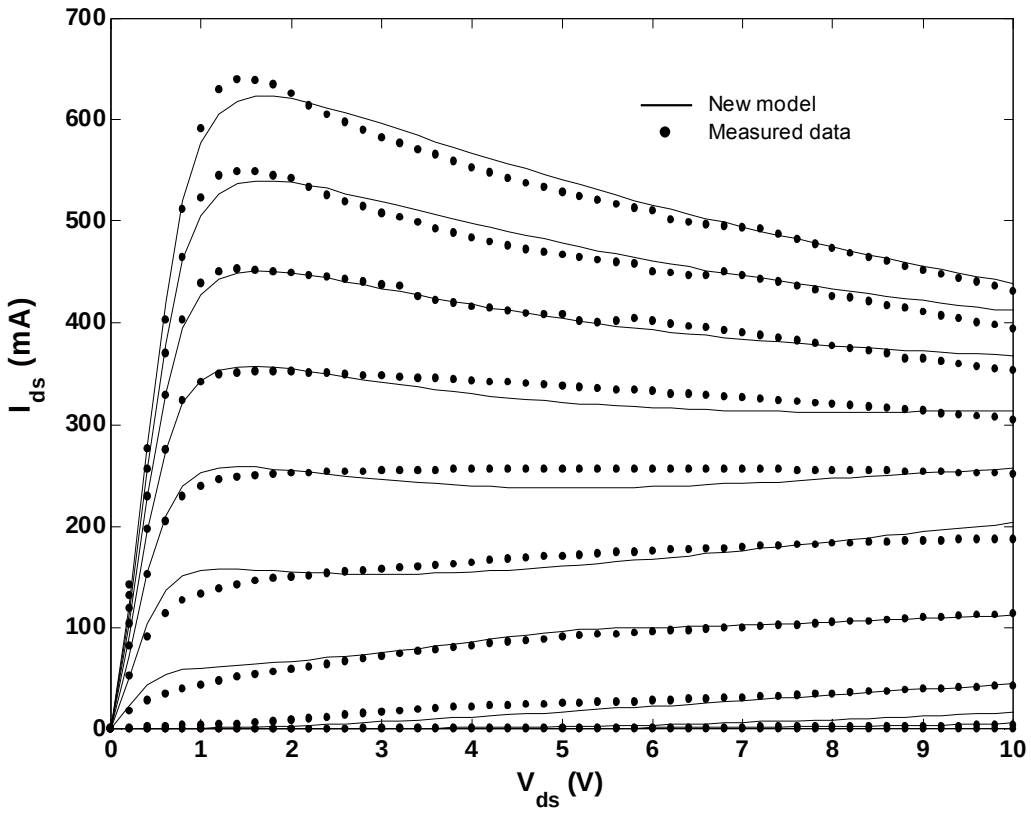


Figure 5.3 Comparison of measured and modeled drain current characteristics by the new model, 16×125μm MESFET wafer device, V_{gs}=-3.1 V – 0.5V.

As observed from Figures 5.2 and 5.3, the new model provides accurate prediction of device drain current for both high current and low current operation. The current drop at high current due to self-heating effect is precisely modeled. A small fluctuation is observed for Ids measurement data, especially at high current region. This can be caused by the practical measurement setup errors.

To compare the accuracies of these drain current expressions of varies models, models parameters are extracted for a 2×125μm GaAs MESFET device using Curtice Quadratic model, Advanced Curtice model, Chalmer's model and the new model, respectively. The modelling results are compared with the measured data. The purpose is to compare the performance of the new model with other commonly used models. The modeled drain current results using Curtice Quadratic model, Advanced

Curtice model, Chalmer's model and the new model are plotted in Figure 5.4 together with the measured data.

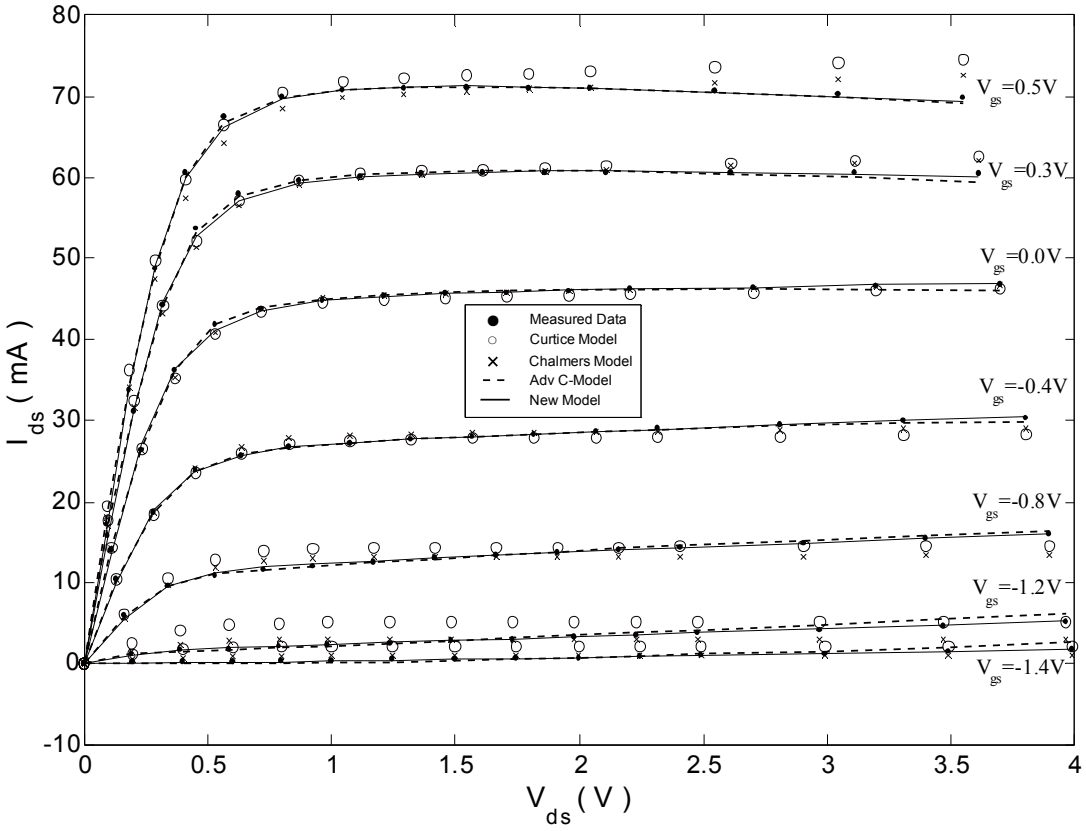


Figure 5.4 Comparison of measured and modeled drain current characteristics of the new model, Curtice model, Chalmers model and Advanced Curtice model, 2*125μm wafer device.

It is seen that the overall performance of Curtice model [46, 53] is poor. The fitting error is quite significant in the linear region, the knee region and the saturation region especially as the drain current is reduced. Also, it has a conditional cutoff in the pinch-off region. Chalmers model [56] offers an improvement over the Curtice model. The fitting accuracy in the linear region and the saturation region is much better, and the transition to pinch-off is continuous. But, the fitting of the Chalmers model in the knee region, saturation region and for small drain current is still poor. Both the

Advanced Curtice model [53] and the proposed improved model give very accurate fitting results over various device operation regions. The new model also gives continuous transition over different operating conditions.

Figures 5.2 to 5.4 show that the simulated drain current results using the new model completely match the measured I-V characteristics. The two results are in good agreement in different device operation regions, especially the linear and knee regions that are difficult to model. The small negative I_{ds} vs. V_{ds} slope for large I_{ds} is well described by the new model. The modeled drain current goes smoothly to zero when V_{gs} approaches or drops below pinch-off.

The maximum fitting error and the RMS error of Curtice model, Chalmers model, Advanced Curtice model and the new model are calculated and listed in Table 5.6 for comparison. The calculation is made under five bias levels for Vgs, while Vds changes from 0.5V to 4.0V (on-wafer 2*125μm GaAs MESFET device). Table 5.6 shows that both the maximum fitting error and the RMS error are greatly reduced for the new model as compared to Curtice model and Chalmers model. The maximum fitting error and RMS error for both the Advanced Curtice model and the new model are very small. But, near pinch-off condition ($V_{gs} = -1.2V$, $V_{pinch\text{-}off} = -1.21V$), the new model produces a much better fitting result as compared to Advanced Curtice model. The proposed drain current model gives the best performance in the comparison to other commonly used models. Furthermore, the new model can be easily implemented into EDA tools, and could be very useful in microwave circuit simulation.

Table 5.6 Comparison of the Maximum Fitting Error and RMS Error of the New Model with Curtice Model, Chalmers Model and Adv Curtice Model (2×125umWafer device)

Models	V_{gs} =0.5V V_{ds}=0.5V~4V		V_{gs} =0.0V V_{ds}=0.5V~4V		V_{gs} =-0.5V V_{ds}=0.5V~4V	
	Max. Err. (%)	RMS Err. (%)	Max. Err. (%)	RMS Err. (%)	Max. Err. (%)	RMS Err. (%)
Curtice Model	6.77	3.26	2.81	1.48	7.73	3.91
Chalmers Model	5.19	2.71	2.70	1.08	6.13	3.83
Adv C-Model	1.90	0.78	1.81	0.72	1.46	0.53
New Model	1.17	0.55	1.54	0.50	0.56	0.26

Models	V_{gs} =-0.8V V_{ds}=0.5V~4V		V_{gs} =-1.2V V_{ds}=0.5V~4V	
	Max. Err. (%)	RMS Err. (%)	Max. Err. (%)	RMS Err. (%)
Curtice Model	18.83	11.14	146.81	82.60
Chalmers Model	16.75	8.78	45.47	27.39
Adv C-Model	2.43	1.20	17.89	10.13
New Model	1.82	1.01	8.31	4.75

5.3 A New Gate Charge Model for GaAs MESFET

5.3.1 Introduction

The large signal equivalent circuit as shown in Figure 5.1 is used to model the nonlinear performance of a MESFET. As mentioned before, there are a few nonlinear properties in the equivalent circuit. Among them, the most important ones are the DC I-V characteristics and the nonlinear gate capacitance C_{gs} and C_{gd}. Charge (capacitance) modelling of MESFET is very important for accurately simulating transistor nonlinear behavior. The accuracy of the charge (capacitance) model affects the simulation result for frequency dependent characteristics like S-parameter, as well as nonlinear properties including distortion, harmonic analysis, third order intermodulation product (TOI), and ACPR (Adjacent-Channel Power Ratio) etc. Therefore, charge (capacitance) modelling is very important for the design of nonlinear circuits using MESFETs, especially power amplifiers. Accurate estimation of quantities of interest for power amplifier at the design stage demands an accurate MESFET capacitance model.

In Chapter 2, the basic operation of the MESFET is briefly discussed. Physically, the depletion layer beneath the gate creates a continuous space-charge region under the gate that expands from the source region to the drain region. The charge in this depletion region is balanced by an equal amount of charge on the gate electrode. The gate charge changes with gate to source and drain to source voltage. As a result, C_{gs} and C_{gd} each depend on both V_{gs} and V_{ds}, they are not two-terminal capacitors that

depend only on the voltage across them. The gate drain capacitance C_{gd} is considerably smaller in magnitude than C_{gs} except in a certain transition region where both drain and source voltages are approximately equal. Charge is a constitutive relation that cannot be directly measured. The nonlinear capacitances are usually extracted from S-parameter measurement in the whole transistor working domain. There are different ways in modelling MESFET charge (capacitance). Physical models as proposed by Takada et al. [104], Shur et al. [105,106], Snowden et al. [107-109] and D'Agostino and Beti-Beruto [110] require a detailed knowledge of the device physical construction to fit measurement data. Multi-dimensional spline functions are employed in table-based models. The empirical model is the most commonly used approach in GaAs MESFET nonlinear modelling, it uses analytical functions to describe bias dependence of the capacitances. Extensive work has been done in MESFET charge modelling, and several models have been proposed. But, the number of models is less than that of DC I-V models for which a large variety of empirical formulations have been proposed. The existing MESFET capacitance models can be classified into two groups. In the first group of models, analytical equations are found to fit C_{gd} and C_{gs} separately, and the equations do not satisfy terminal charge conservation. These models may be difficult to implement in circuit simulators whose capacitance is always the derivative of an internal state variable (charge). In addition, the simulation may have convergence problems if charge conservation is not maintained. These include the model proposed by Scheinberg et al. [111], Angelov et al. [56], and Rodriguez et al. [58]. In the second group, analytical

equations are proposed for terminal charge, and the capacitor values are derived from the partial derivatives of charge with respect to the appropriate voltages, such as Statz model [50] and the model proposed by Parker and Skellern [35].

It is complicated to precisely model the MESFET gate capacitances. Most existing models are capable of accurately describing capacitance performance in only certain device operation regions. Modelling in the linear region and in the saturation knee region is difficult, and normally the inaccuracy is most significant. Capacitance fitting at V_{ds}=0 and in sub-threshold region are generally poor too. Charge (capacitance) performance is critical in predicting the nonlinear characteristics of MESFETs and circuits using them. Thus, accurate capacitance modelling is important.

In the following sections, some widely used gate capacitance models are first investigated. A new gate charge model is subsequently proposed. The model equation is unique, and it is accurate under various device biasing conditions. Most specially, the performance prediction in the linear region, saturation knee region, sub-threshold region and at V_{ds}=0 is greatly improved. A sub-micron MESFET device is adopted to verify the proposed model. Gate capacitances C_{gs} and C_{gd} are extracted from measured S-parameters in the whole device working region under various biasing levels. Terminal voltages at the intrinsic device are used in model parameter extraction of the nonlinear charge model. Terminal voltages at the intrinsic device plane are obtained after de-embedding of the parasitic elements.

5.3.2 Some Existing Empirical Gate Capacitance Models

Two of the most widely used MESFET capacitance models are the models based on PN junction depletion capacitance formula [7] and Statz model [50]. In this section, these two models are compared and discussed. A detailed model formulation of each model can be found in Appendix A.

5.3.2.1 Diode Junction Capacitor Model

In the diode junction capacitance model, both C_{gs} and C_{gd} are modeled as two terminal capacitors whose capacitances only depend on the voltage cross them. Gate-source and gate-drain capacitance share the same expression which is given by equation 5.8, and is expressed as:

$$C_{gs,gd} = \frac{C_{gs0,gd0}}{\left(1 - \frac{V_{gs,gd}}{V_{bi}}\right)^{m}} \tag{5.8}$$

In equation 5.8, C_{gs0} and C_{gd0} represent gate–source and gate-drain capacitance at zero V_{gs} bias respectively, V_{bi} is the built-in voltage of the Schottky gate, and m is the capacitance gradient factor. In some models like the Curtice model, m is assumed to be 0.5. However, with m as model parameter it allows C-V relationship to be more accurately modeled. Equation 5.8 was originally developed for silicon devices, and it works well for silicon-based devices. However, model accuracy is poor when equation 5.8 is applied to GaAs MESFET devices. This is because of the linear approximation law, i.e. ($\log(C_{gs0,gd0}/C_{gs,gd}) = m \cdot \log(V_{bi}-V_{gs,gd}) - m \cdot \log(V_{bi})$). Also, the model assumes C_{gs} and C_{gd} only depends on the voltage across them, drain-source

voltage dependence is not included. This assumption does not agree with real GaAs MESFET device operation and large fitting errors can be introduced into simulations, especially for operation at low drain to source voltage.

5.3.2.2 Statz Model

In the Statz model [50], a simple gate charge Q_g expression was proposed. The model was based on the observation of the measured C_{gs} and C_{gd} characteristic. Gate source capacitance C_{gs} can be approximated by the diode junction capacitance model in the normal bias range where $V_{ds}>>0$. Gate drain capacitance C_{gd} is small in this same voltage range as compared to C_{gs}, Its value is approximately constant and nearly independent of V_{gs} or V_{gd}. The Statz model gate charge expressions are given as follows.

For $V_n>V_{max,}$

$$Q_g = C_{gs0}\left[2V_{bi}\left(1-\sqrt{1-\frac{V_{\max}}{V_{bi}}}\right)+\frac{V_n-V_{\max}}{\sqrt{1-\frac{V_{\max}}{V_{bi}}}}\right]+C_{gd0}V_{eff2} \tag{5.9}$$

$$C_{gs}=\frac{\partial Q_g}{\partial V_{gs}}=\frac{C_{gs0}K_2K_1}{\sqrt{1-\frac{V_{\max}}{V_{bi}}}}+C_{gd0}K_3 \tag{5.10}$$

$$C_{gd}=\frac{\partial Q_g}{\partial V_{gd}}=\frac{C_{gs0}K_3K_1}{\sqrt{1-\frac{V_{\max}}{V_{bi}}}}+C_{gd0}K_2 \tag{5.11}$$

For $V_n\leq V_{max,}$ $Q_g = 2C_{gs0}V_{bi}\left(1-\sqrt{1-\frac{V_n}{V_{bi}}}\right)+C_{gd0}V_{eff2}$, (5.12)

$$C_{gs} = \frac{\partial Q_g}{\partial V_{gs}} = \frac{C_{gs0} K_2 K_1}{\sqrt{1 - \frac{V_n}{V_{bi}}}} + C_{gd0} K_3 \tag{5.13}$$

$$C_{gd} = \frac{\partial Q_g}{\partial V_{gd}} = \frac{C_{gs0} K_3 K_1}{\sqrt{1 - \frac{V_n}{V_{bi}}}} + C_{gd0} K_2 \tag{5.14}$$

Where

$$V_n = \frac{1}{2}\left[V_{eff1} + V_{T0} + \sqrt{(V_{eff1} - V_{T0})^2 + \delta^2} \right] \tag{5.15}$$

$$V_{eff1} = \frac{1}{2}\left[V_{gs} + V_{gd} + \sqrt{(V_{gs} - V_{gd})^2 + \left(\frac{1}{\alpha}\right)^2} \right] \tag{5.16}$$

$$V_{eff2} = \frac{1}{2}\left[V_{gs} + V_{gd} - \sqrt{(V_{gs} - V_{gd})^2 + \left(\frac{1}{\alpha}\right)^2} \right] \tag{5.17}$$

V_{max} = 0.5, δ=0.2, and

$$K_1 = \frac{\partial V_n}{\partial V_{eff1}} = \frac{1}{2}\left[1 + \frac{V_{eff1} - V_{T0}}{\sqrt{(V_{eff1} - V_{T0})^2 + \delta^2}} \right] \tag{5.18}$$

$$K_2 = \frac{\partial V_{eff1}}{\partial V_{gs}} = \frac{\partial V_{eff2}}{\partial V_{gd}} = \frac{1}{2}\left[1 + \frac{V_{gs} - V_{gd}}{\sqrt{(V_{gs} - V_{gd})^2 + \left(\frac{1}{\alpha}\right)^2}} \right] \tag{5.19}$$

and $K_3 = \frac{\partial V_{eff1}}{\partial V_{gd}} = \frac{\partial V_{eff2}}{\partial V_{gs}} = \frac{1}{2}\left[1 - \frac{V_{gs} - V_{gd}}{\sqrt{(V_{gs} - V_{gd})^2 + \left(\frac{1}{\alpha}\right)^2}} \right]$. (5.20)

Equations 5.16 and 5.17 are employed to achieve a gradual transition of capacitance values near V_{ds}=0. V_{eff1} and V_{eff2} represent the bigger and the smaller value between V_{gs} and V_{gd} respectively. Parameter α produces a smooth transition

width of $1/\alpha$ in the value of V_{eff1} and V_{eff2} as a function of V_{gs} and V_{gd}. The transformation in equation 5.15 is employed to model capacitance beyond pinch-off. In the pinch-off region, the gate-source capacitance drops to a small value which is normally determined by the fringing capacitance of the depletion region. The smooth transformation of equation 5.15 would set V_n to V_{eff1} before pinch-off, and to V_{T0} when V_{eff1} is biased beyond pinch-off. Parameter δ stands for the voltage range over which the transition between V_{eff1} and V_{T0} occurs, and is set to 0.2.

From equations 5.9 and 5.12, we can see that charge Q_g does not change if the values of V_{gs} and V_{gd} are inter-changed. This is achieved through the transformation of equations 5.16 and 5.17. Thus, the model yields a symmetry behavior of the transistor. For positive V_{ds} (normal operation model), C_{gs} shows diode capacitance behavior with V_{gs}, whereas in the reverse-biased direction ($V_{ds}<0$), C_{gs} approaches C_{gd0}. On the other hand, C_{gd} is close to C_{gd0} when $V_{ds}>0$, and exhibits diode capacitance behavior with V_{gd} when $V_{ds}<0$. Thus, when $V_{ds}<0$, the role of drain and source reversed, and the source becomes the effective drain, so V_{gd} not V_{gs} becomes the important gate voltage.

V_{max} is introduced to solve the singularity in junction capacitance when V_{eff1} becomes positive and is equal or greater than V_{bi}. The value of Veff1 is limited to a maximum value of V_{max} when $V_{eff1} \geq V_{max}$ (V_{max} sets to 0.5V). This limits the value of junction capacitance. The choice of V_{max} determines the maximum capacitance value, for voltage beyond V_{max}, the junction capacitances are assumed to remain constant. This is reflected by equations 5.9 to 5.11.

5.3.3 The New Gate Charge Model

The gate charge (capacitance) modelling is very important in accurately describing MESFET's nonlinear behavior, and therefore is critical for predicting the performance of nonlinear circuits like power amplifiers. Accurate simulation of the voltage dependency of C_{gs} and C_{gd} is difficult to achieve. In the linear region, both C_{gs} and C_{gd} change fast with V_{gs} and V_{ds}. In the saturation region, C_{gs} is almost independent of V_{ds}, and C_{gd} shows little variation with V_{gs}. However, more difficulty would be imposed to find a suitable gate charge expression as terminal charge conservation has to be taken into consideration in the gate charge model to avoid possible convergence problem in simulation. Therefore, the following charge conservation law is chosen for deriving the gate charge [112, 114].

$$V_{gs} = V_{gs0} + v_{gs};\ \ V_{ds} = V_{ds0} + v_{ds} \tag{5.21}$$

$$i_{gs} = C_{gs}(V_{gs}, V_{ds}) \cdot \frac{dV_{gs}}{dt}, \tag{5.22}$$

$$i_{gd} = C_{gd}(V_{gs}, V_{ds}) \cdot \frac{dV_{gd}}{dt}, \tag{5.23}$$

$$i_g = i_{gs} + i_{gd} = \left[C_{gs}(V_{gs}, V_{ds}) + C_{gd}(V_{gs}, V_{ds}) \right] \frac{dV_{gs}}{dt} - C_{gd}(V_{gs}, V_{ds}) \frac{dV_{ds}}{dt} = \frac{dQ_g}{dt} \tag{5.24}$$

$$dQ_g = C_{gs}(V_{gs}, V_{ds}) \cdot dV_{gs} + C_{gd}(V_{gs}, V_{ds}) \cdot d(V_{gs} - V_{ds}), \tag{5.25}$$

$$dQ_g = \left[C_{gs}(V_{gs}, V_{ds}) + C_{gd}(V_{gs}, V_{ds}) \right] \cdot dV_{gs} - C_{gd}(V_{gs}, V_{ds}) \cdot dV_{ds} \tag{5.26}$$

New equations for gate charge and capacitances are:

$$Q_g = F_1 + F_2 * \tanh(c_8 \cdot V_{ds}) + F_3 \cdot V_{ds} - C_{gd0} \cdot V_{ds}, \tag{5.27}$$

$$C_{gs}+C_{gd}=\frac{\partial Q_g}{\partial V_{gs}}=f_1+f_2\cdot\tanh(c_8\cdot V_{ds})+f_3\cdot V_{ds}\,, \tag{5.28}$$

$$C_{gd}=-\frac{\partial Q_g}{\partial V_{ds}}=-\left(F_2\cdot c_8\cdot sech^2(c_8\cdot V_{ds})+f_3-C_{gd0}\right), \tag{5.29}$$

$$F_1=c_1\cdot V_{gs}+c_2\cdot e^{c_3\cdot V_{eff1}^2+c_4\cdot V_{eff2}}\,, \tag{5.30}$$

$$f_1=\frac{\partial F_1}{\partial V_{gs}}=c_1+c_2\cdot e^{c_3\cdot V_{eff1}^2+c_4\cdot V_{eff2}}\cdot\left(2c_3\cdot V_{eff1}\cdot dV_{eff1}+c_4\cdot dV_{eff2}\right), \tag{5.31}$$

$$F_2=c_7\cdot V_{eff1}+c_5\cdot\left(e^{c_6\cdot V_{eff1}^2}-\frac{V_{eff2}}{V_{eff1}+V_{eff2}}\right), \tag{5.32}$$

$$f_2=\frac{\partial F_2}{\partial V_{gs}}=c_7\cdot dV_{eff1}+c_5\cdot\left(2c_6\cdot V_{eff1}\cdot dV_{eff1}\cdot e^{c_6\cdot V_{eff1}^2}-\frac{dV_{eff2}\cdot V_{eff1}-dV_{eff1}\cdot V_{eff2}}{\left(V_{eff1}+V_{eff2}\right)^2}\right), \tag{5.33}$$

$$F_3=c_9\cdot V_{gs}+c_{10}\cdot V_{eff2}^{\frac{3}{2}}+c_{11}\cdot V_{eff1}^2\,, \tag{5.34}$$

$$f_3=\frac{\partial F_3}{\partial V_{gs}}=c_9+\frac{3}{2}\cdot c_{10}\cdot dV_{eff2}\cdot\sqrt{V_{eff2}}+2c_{11}\cdot V_{eff1}\cdot dV_{eff1}, \tag{5.35}$$

$$V_{eff1}=\frac{1}{2}\cdot\left(V_{gsto}+\sqrt{V_{gsto}^2+\delta}\right), \tag{5.36}$$

$$V_{eff2}=\frac{1}{2}\cdot\left(\sqrt{V_{gsto}^2+\delta}-V_{gsto}\right), \tag{5.37}$$

$$dV_{eff1}=\frac{\partial V_{eff1}}{\partial V_{gs}}=\frac{1}{2}\cdot\left(1+\frac{V_{gsto}}{\sqrt{V_{gsto}^2+\delta}}\right), \tag{5.38}$$

$$dV_{eff2}=\frac{\partial V_{eff2}}{\partial V_{gs}}=\frac{1}{2}\cdot\left(\frac{V_{gsto}}{\sqrt{V_{gsto}^2+\delta}}-1\right), \tag{5.39}$$

$$V_{gsto}=V_{gs}-V_{TO} \tag{5.40}$$

Due to the uncertainties with fabrication process and measurements, it is hard to

develop expressions for junction capacitances of a MESFET from physical point of view. Therefore, the new gate charge (capacitance) model is not derived from device physics. It is primarily developed to provide more accuracy. Thus, most of the model parameters do not convey any physical meaning.

In the above equations, c_1 to c_{11} and C_{gd0} are model parameters for accurate curve fitting. We note that V_{TO} is the pinch-off voltage which is also used to define drain current I-V characteristics. Hence V_{TO} can be kept the same as that used in DC I-V model. If so, a compromise is made between DC and AC modelling accuracy. It is worth noting that improvements in CV modelling can be achieved if V_{TO} is extracted differently from DC I-V characteristics. δ is a parameter introduced to model the voltage range over which the transition to the sub-threshold and the pinch-off region occurs. Finally, V_{gs} and V_{ds} are the intrinsic terminal voltages.

$$\frac{\partial Q_g^2(V_{gs},V_{ds})}{\partial V_{gs}\cdot\partial V_{ds}} = \frac{\partial\left(\frac{\partial Q_g(V_{gs},V_{ds})}{\partial V_{gs}}\right)}{\partial V_{ds}} = \frac{\partial\left[C_{gs}(V_{gs},V_{ds})+C_{gd}(V_{gs},V_{ds})\right]}{\partial V_{gs}\cdot\partial V_{ds}}$$

$$= \frac{\partial\left(\frac{\partial Q_g(V_{gs},V_{ds})}{\partial V_{ds}}\right)}{\partial V_{gs}} = -\frac{\partial C_{gd}(V_{gs},V_{ds})}{\partial V_{gs}}$$

$$= f_2\cdot c_8\cdot sech^2(c_8\cdot V_{ds})+f_3 \qquad (5.41)$$

The new nonlinear gate charge model can accurately describe the MESFET behavior around various bias regions: linear, knee, saturation, and pinch-off regions. The integral condition in equation 5.41 is satisfied, and this gate charge can thus be considered as a state variable. The new model observes terminal charge conservation

law, and is continuous under different bias condition.

5.4 Numerical Results and Discussions

5.4.1 Model Parameter Extraction

The same TOSHIBA 2*150μm sub-micron gate-length MESFET device (wafer device) as in Chapter 3 is used to verify the new gate charge model. The S-parameter data is measured at multi-bias conditions ($V_{gs} = -2.0\text{V} \sim 0.5\text{V}$, $V_{ds} = 0.0\text{V} \sim 4.0\text{V}$, totally 285 biasing points). The small-signal equivalent circuit models are extracted under multi-bias conditions using the novel analytical method without any Cold-FET and Hot-FET procedures. All the parasitic element values are kept constant in the large-signal model. The extracted parasitic element values are listed in Table 5.7. The nonlinear capacitances were acquired from S-parameter measurement in the frequency range of 1-30GHz. They are represented in the whole working domain as shown in Figures 5.5 and 5.6 for C_{gs} and C_{gd} respectively ($V_{gs} = -2.0\text{V} \sim 0.5\text{V}$, $V_{ds} = 0.0\text{V} \sim 4.0\text{V}$).

Table 5.7 Parasitic Element Values For 2×150μm GaAs MESFET

C_{pg}(fF)	C_{pd} (fF)	R_g(Ω)	R_d(Ω)
177.72	86.62	1.68	0.78
R_s(Ω)	L_g(pH)	L_d(pH)	L_s(pH)
0.33	85.43	23.20	15.01

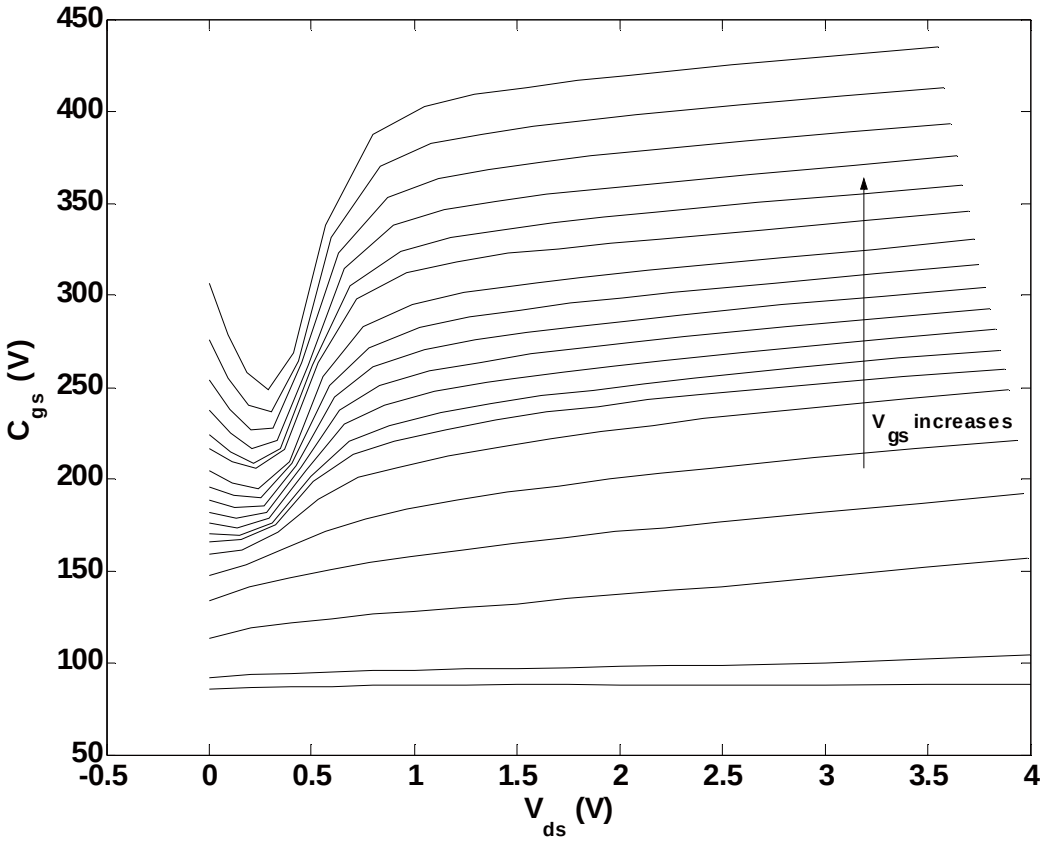


Figure 5.5 C_{gs} extracted from S-parameter as a function of V_{gs} and V_{ds} (V_{gs}=-2.0~0.5V, V_{ds}=0.0~4.0V).

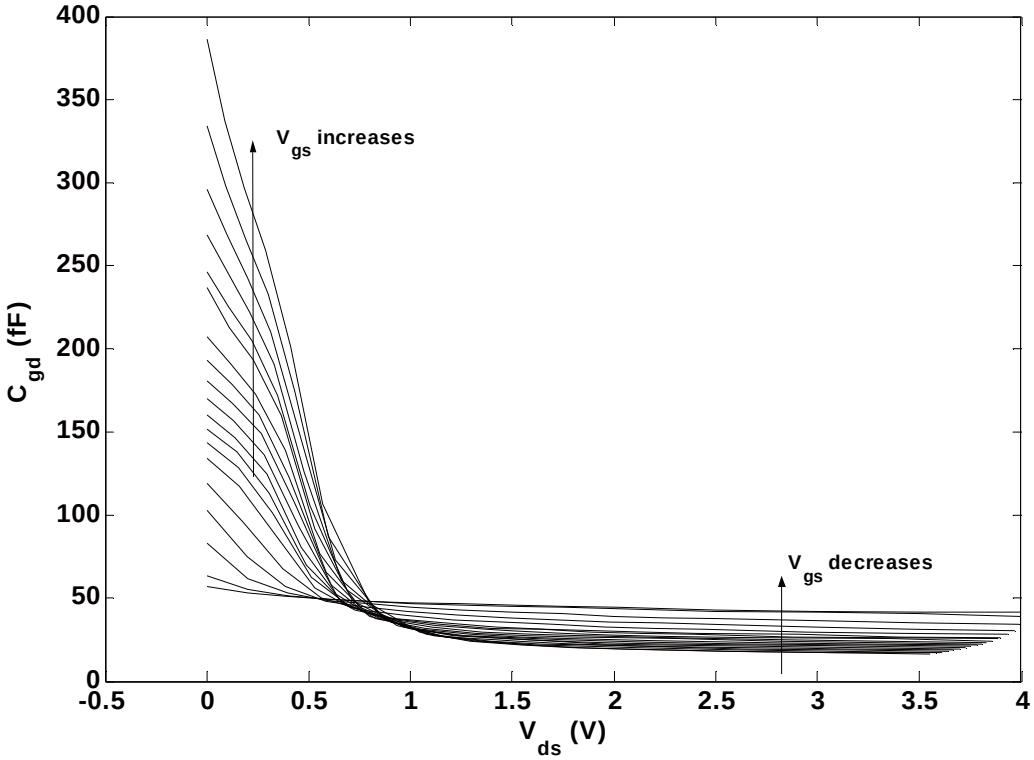


Figure 5.6 C_{gd} extracted from S-parameter as a function of V_{gs} and V_{ds} (V_{gs}=-2.0~0.5V, V_{ds}=0.0~4.0V).

Table 5.8 Parameters for New Gate Charge Model (2×150μm GaAs MESFET)

C_1	C_2	C_3	C_4	C_5	C_6	C_7
260.8	146.9	0.304	0.58	-26.8	0.44	-35.7
C_8	C_9	C_{10}	C_{11}	δ	C_{gd0}	
2.07	17.5	13.0	-3.02	0.65	16.05	

The model parameters for the new gate charge model are extracted at the intrinsic device plane, and are listed in Table 5.8 ($V_{TO} = -1.21V$ from DC I-V model). Notice that in our model extraction, V_{TO} is kept the same as in DC I-V model, which is to compromise between the model extraction complexity and the model accuracy. To get better accuracy, V_{TO} may be considered as an ac model parameter. All the parameter extractions are performed by an in-house developed software running under MATLAB® by MathWorks. A simplex algorithm is used for the optimization.

5.4.2 Modelling Results and Discussions

Figures 5.7 and 5.8 show the comparison between the modeled C_{gs} and C_{gd} using the new model and gate capacitances extracted from measured S-parameter for the 2×150μm sub-micron gate-length GaAs MESFET. The pinch-off voltage of the device is -1.21V. For clear display, only results under Vgs=-2.0V, -1.4V, -1.2V, -1.0V –0.5V, 0.0V and Vds=0.0-4.0V are plotted for C_{gs}. For C_{gd}, the results are plotted for V_{gs}=-1.4V, -1.0V –0.5V, 0.0V and V_{ds}=0.0-4.0V, this is because in the saturation region, Cgd shows small variation with V_{gs}.

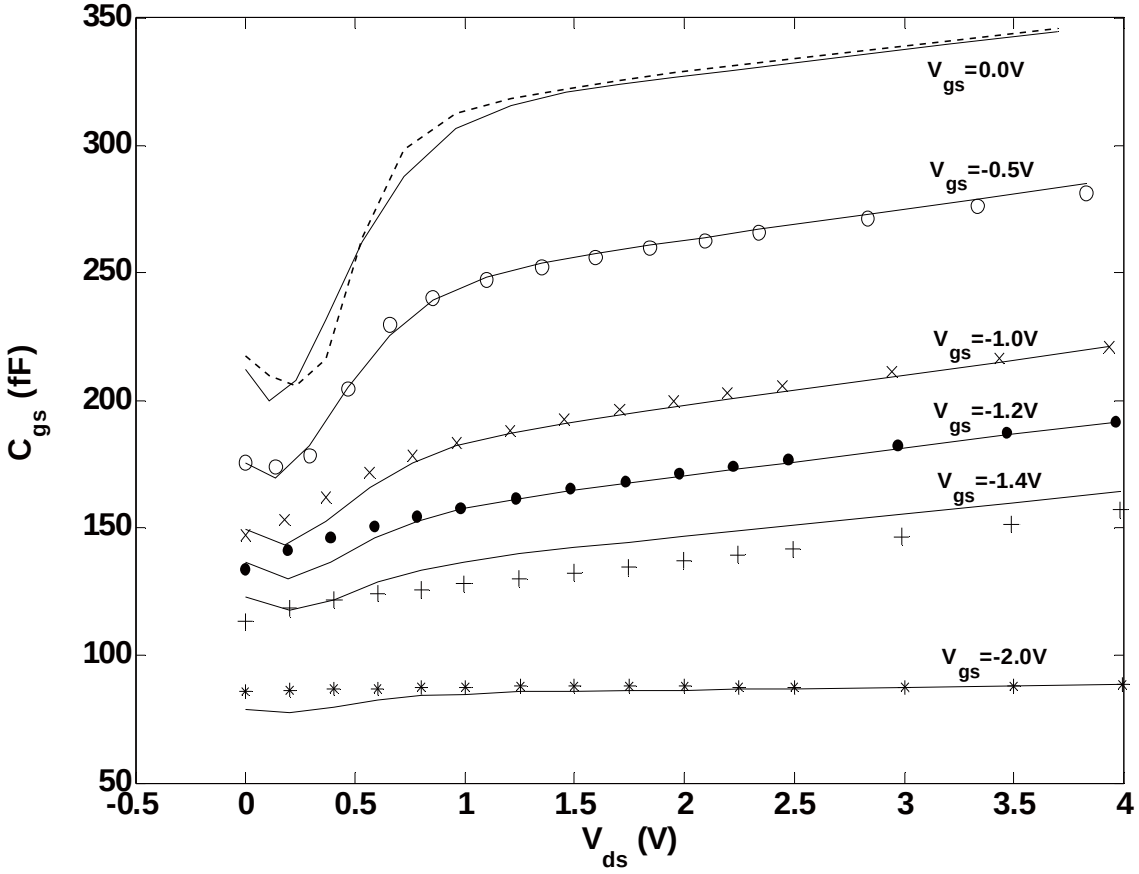


Figure 5.7 Comparison between modeled C_{gs} using the new model and measured C_{gs} extracted from S-parameter for 2×150μm GaAs MESFET (—— Modeled, ----Measured V_{gs}=0.0V, ○○○Measured V_{gs}=-0.5V, ×××Measured V_{gs}=-1.0, ●●●Measured V_{gs}=-1.2V, +++Measured V_{gs}=-1.4V, ***Measured V_{gs}=-2.0V)

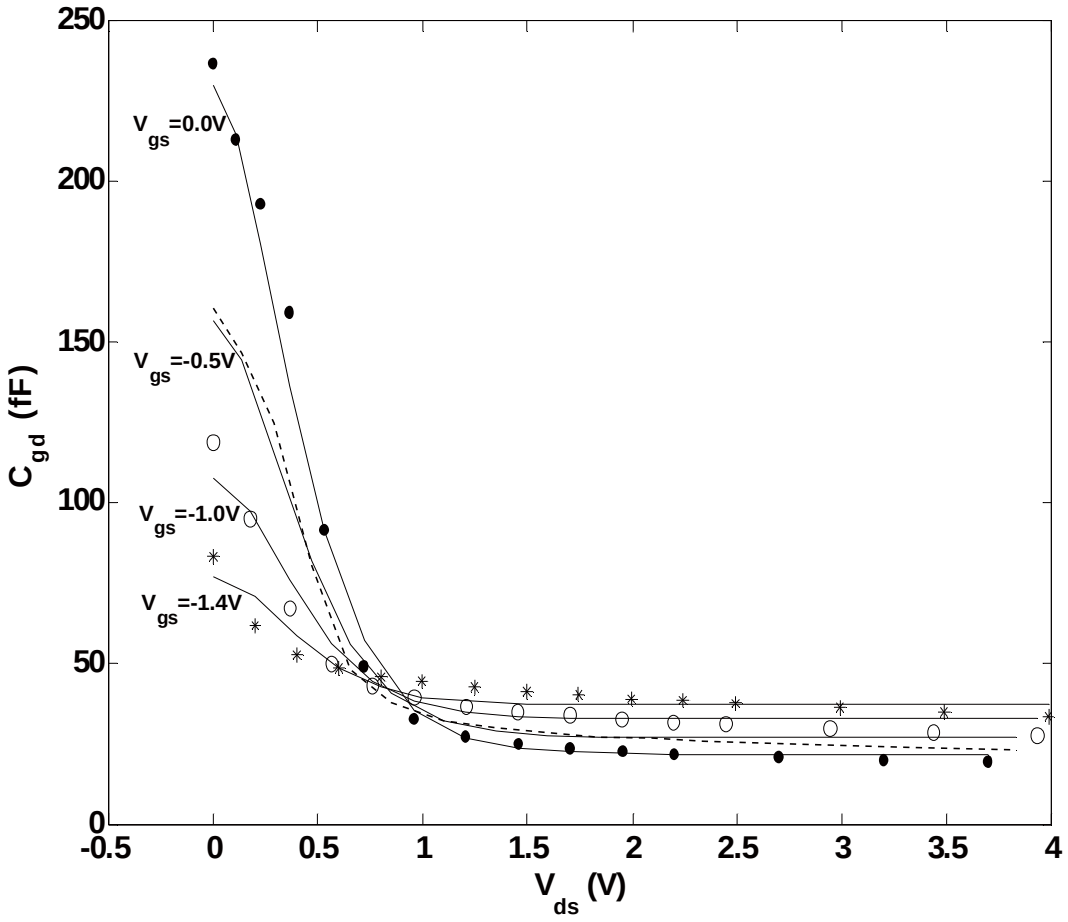


Figure 5.8 Comparison between modeled C_{gd} using the new model and measured C_{gd} extracted from S-parameter for 2×150μm GaAs MESFET (—— Modeled, ●●● Measured V_{gs}=0.0V, ----Measured V_{gs}=-0.5V, ○○○ Measured V_{gs}=-1.0V, *** Measured V_{gs}=-1.4V)

From Figures 5.7 and 5.8, it can be seen that the proposed new model gives very accurate fitting results over various device operation regions, especially in the linear region where the variation of C_{gs} and C_{gd} is not well defined. And in the saturation region, the model is able to follow the small variation of C_{gs} with V_{ds} and C_{gd} with V_{gs}. The model is also capable of modelling nonlinear capacitances in the pinch-off region and for $V_{gs}>V_{bi}$.

The new model gives a continuous transition over different operation conditions, and its derivatives are continuous. Figures 5.9 to 5.12 give the derivatives of C_{gs} and C_{gd} with respect to V_{gs} and V_{gd} for the 2×150μm wafer device.

To validate the model continuity with respect to V_{gs}, $\partial C_{gs}/\partial V_{gs}$ vs. V_{gs} and $\partial C_{gd}/\partial V_{gs}$ vs. V_{gs} characteristics predicted by the new model are calculated and shown in Fig 5.9 and 5.10. In Fig 5.9, the modeled $\partial C_{gs}/\partial V_{gs}$ vs. V_{gs} characteristics are shown together with modeled and measured C_{gs} vs. V_{gs} performance. V_{ds} is fixed at 2.0V where the device operates in the saturation region. It is noted that the modeled C_{gs} results match the measured ones closely. In addition, the $\partial C_{gs}/\partial V_{gs}$ vs. V_{gs} curve by the new model is continuous and the transition between pinch-off and normal operation region is smooth.

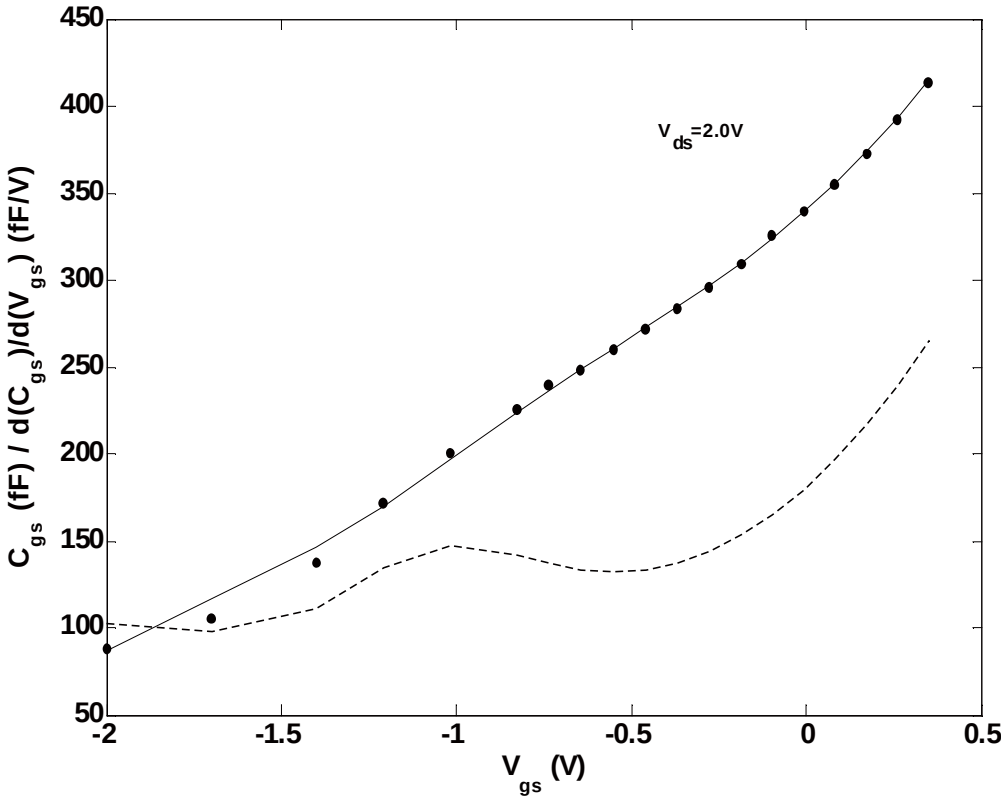


Figure 5.9 C_{gs} vs. V_{gs} and $\partial C_{gs}/\partial V_{gs}$ vs. V_{gs} characteristics for a 2×150μm wafer device (—— C_{gs} by the new model, ●●● C_{gs} measured, ------ $\partial C_{gs}/\partial V_{gs}$ by the new model).

The modeled $\partial C_{gd}/\partial V_{gs}$ vs. V_{gs} characteristics are plotted together with the modeled and measured C_{gd} vs. V_{gs} characteristics in Fig 5.10. The measurement results have shown that device C_{gd} vs. V_{gs} characteristics behave differently in the

linear and saturation regions, as can also be observed from Fig 5.8. In the linear region where V_{ds} is small, C_{gd} increases as V_{gs} increases. On the other hand, in the saturation region, C_{gd} decreases as V_{gs} increases. Therefore, in Figure 5.10, $\partial C_{gd}/\partial V_{gs}$ vs. V_{gs} performance is plotted under V_{ds}=0.2V and V_{ds}=2.0V where the device operates in the linear and saturation region respectively. It is clear that the modeled C_{gd} precisely matches the measurement data. The $\partial C_{gd}/\partial V_{gs}$ vs. V_{gs} curve is continuous and well behaved. For V_{ds}=0.2V, it has a positive value due to the fact that C_{gd} increases as V_{gs} increases. For Vds=2.0V, it shows a negative value because in saturation region, C_{gd} decreases as V_{gs} increases.

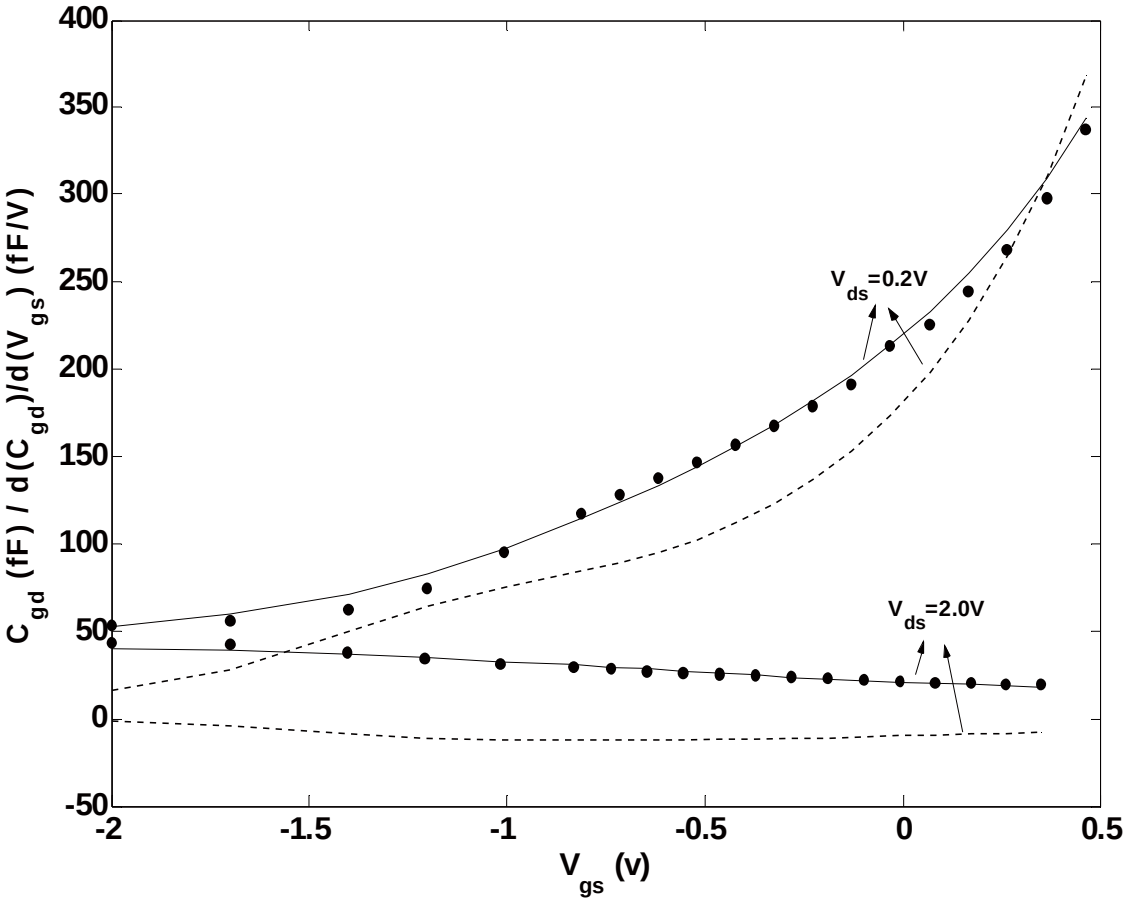


Figure 5.10 C_{gd} vs. V_{gs} and $\partial C_{gd}/\partial V_{gs}$ vs. V_{gs} characteristics for a 2×150μm wafer device (—— C_{gd} by the new model, ●●● C_{gd} measured, ------ $\partial C_{gd}/\partial V_{gs}$ by the new model).

Moreover, to illustrate the model continuity with respect to V_{ds}, $\partial C_{gs}/\partial V_{ds}$ vs. V_{ds} and C_{ds} vs. V_{ds} characteristics predicted by the new model are calculated and shown in Figs 5.11 and 5.12. Fig 5.11 provides the modeled $\partial C_{gs}/\partial V_{ds}$ vs. V_{ds} characteristics as well as the modeled and measured C_{gs} vs. V_{ds} performance. The plots are taken under V_{gs}=-0.2V and V_{gs}=-2.0V where the device operates in the normal and pinch-off region respectively.

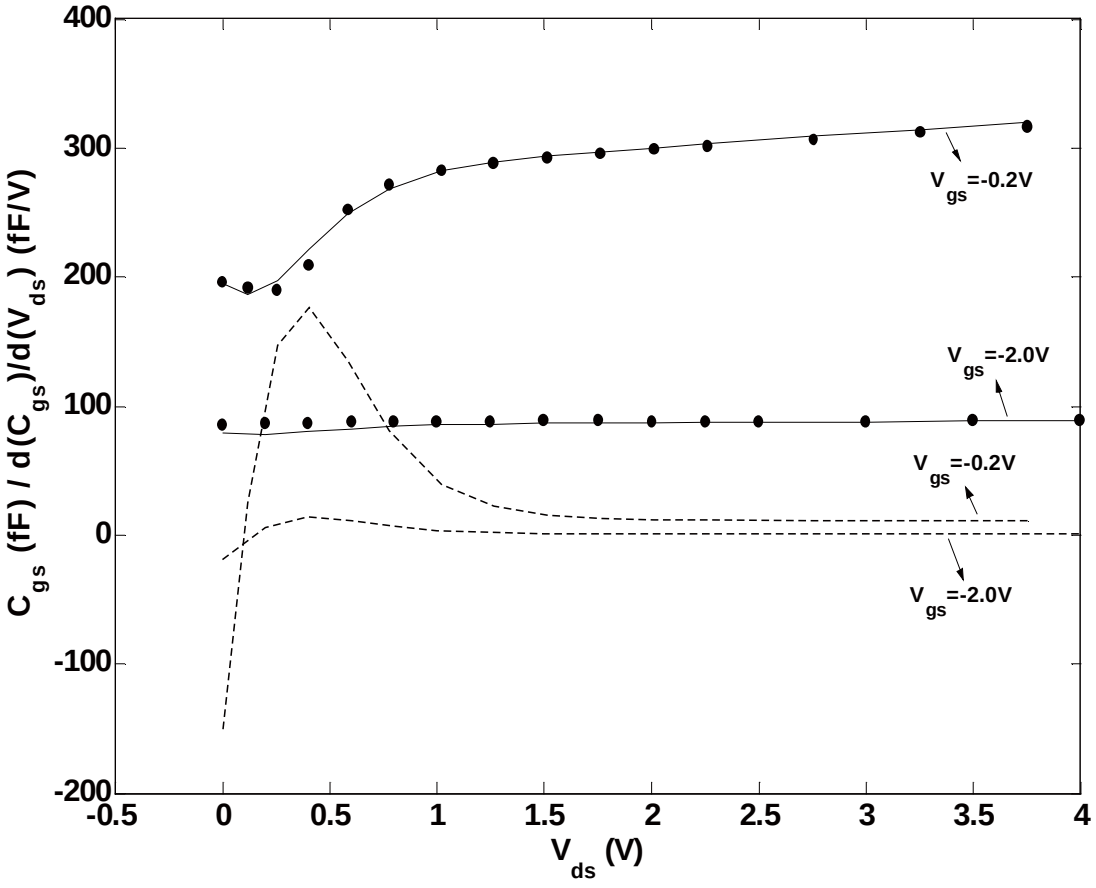


Figure 5.11 C_{gs} vs. V_{ds} and $\partial C_{gs}/\partial V_{ds}$ vs. V_{ds} characteristics for a 2×150μm wafer device (—— C_{gs} by the new model, ●●● C_{gs} measured, ------ $\partial C_{gs}/\partial V_{ds}$ by the new model).

As can be seen from Figure 5.11, the C_{gs} vs. V_{ds} property is different in the normal operating region and in the pinch-off region. In the pinch-off region, C_{gs}

shows little variation with V_{ds}. However, in the normal operating region, C_{gs} changes rapidly with V_{ds} in the linear and knee region. These properties are reflected in the $\partial C_{gs}/\partial V_{ds}$ vs. V_{ds} plot of Figure 5.11 where C_{gs} is almost constant in the pinch-off region, and changes fast in the linear region when V_{gs}=-0.2V. The derivative of C_{gs} with respect to V_{ds} by the new model is continuous which also provides a smooth transition between various operation regions.

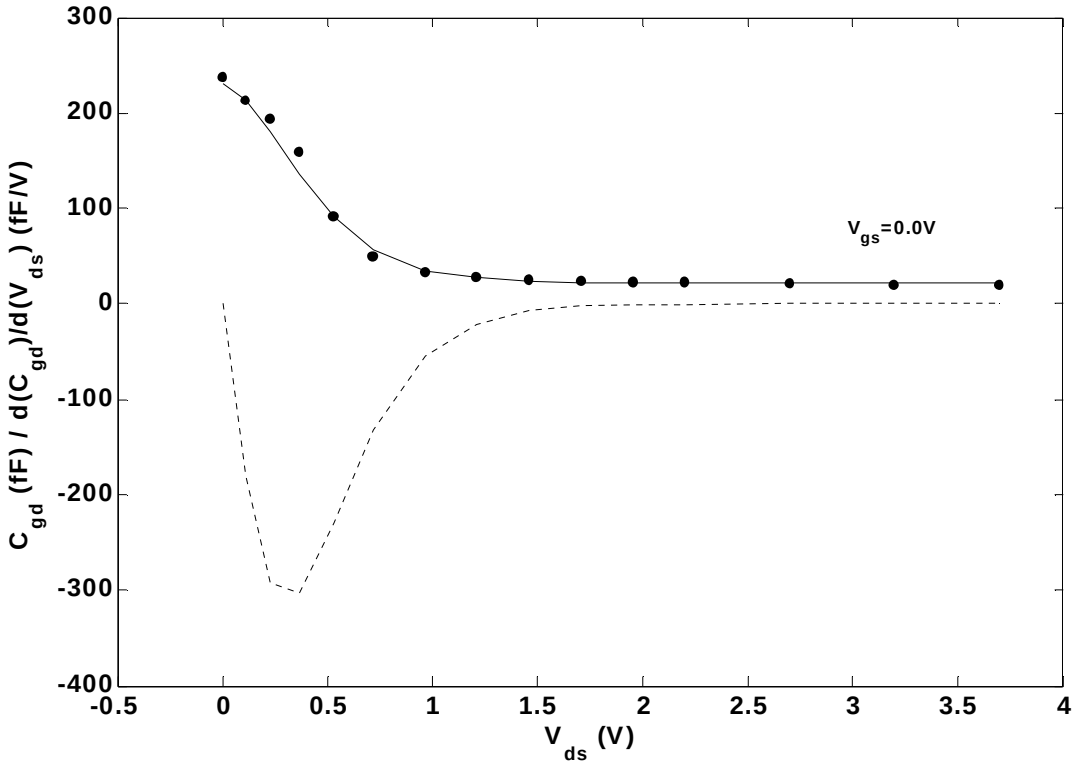


Figure 5.12 C_{gd} vs. V_{ds} and $\partial C_{gd}/\partial V_{ds}$ vs. V_{ds} characteristics for a 2×150μm wafer device (—— C_{gd} by the new model, ●●● C_{gd} measured, ------ $\partial C_{gd}/\partial V_{ds}$ by the new model)

The modeled $\partial C_{gd}/\partial V_{ds}$ vs. V_{ds} characteristics are plotted together with the modeled and measured C_{gd} vs. V_{ds} characteristics in Figure 5.12 where V_{gs} is fixed at 0.0V. As can be seen, the modeled C_{gd} results by the new model accurately match the measurement data whilst the $\partial C_{gd}/\partial V_{ds}$ vs. V_{ds} curve is continuous and well behaved.

Also, the transitions in the linear region, the knee region and the saturation region are smooth.

The measured and computed response achieved with the diode junction capacitance model, Statz model and the new model for C_{gs} when operating solely against V_{gs} (V_{ds} at fixed value) are shown in Figure 5.13. As observed from this figure, the junction capacitance model provides very poor accuracy. The Statz model gives noticeable improvement over junction capacitance model. However, the Statz model accuracy is still poor at certain device bias points compared with our new model. It is clear that the new capacitance model provides the best accuracy as the measurement and its modeled data show a very close agreement.

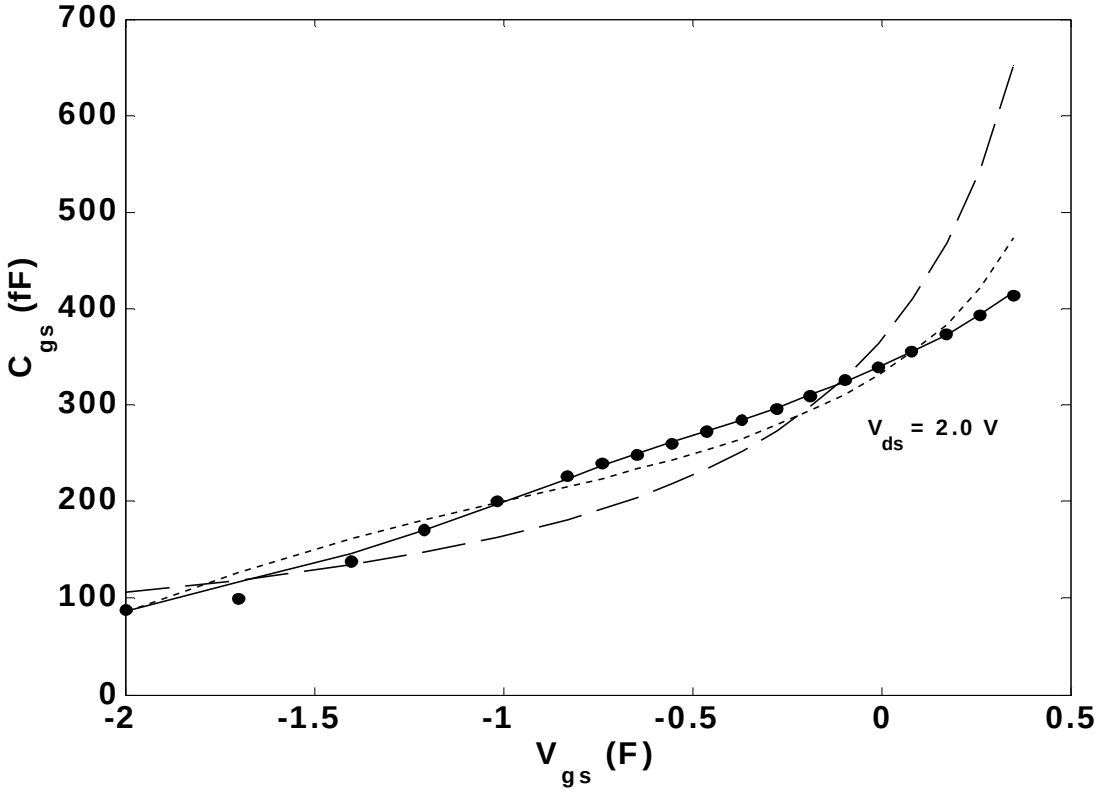


Figure 5.13 Comparison of measured and modeled C_{gs} data (●●● measured data, —— new model, ------ Statz model, – – –Diode junction capacitance model)

The same tendency of model accuracy for C_{gd} is exhibited as for C_{gs}. In Figure 5.14, modeled C_{gd} result with diode junction capacitance model, Statz model and the new model are compared to the measurement result. This figure shows the operating behavior of C_{gd} with V_{gd}, with V_{gs} being fixed. Undoubtedly again the new model offers obvious advantage over the other two models, as its modeled result matches measurement data closely.

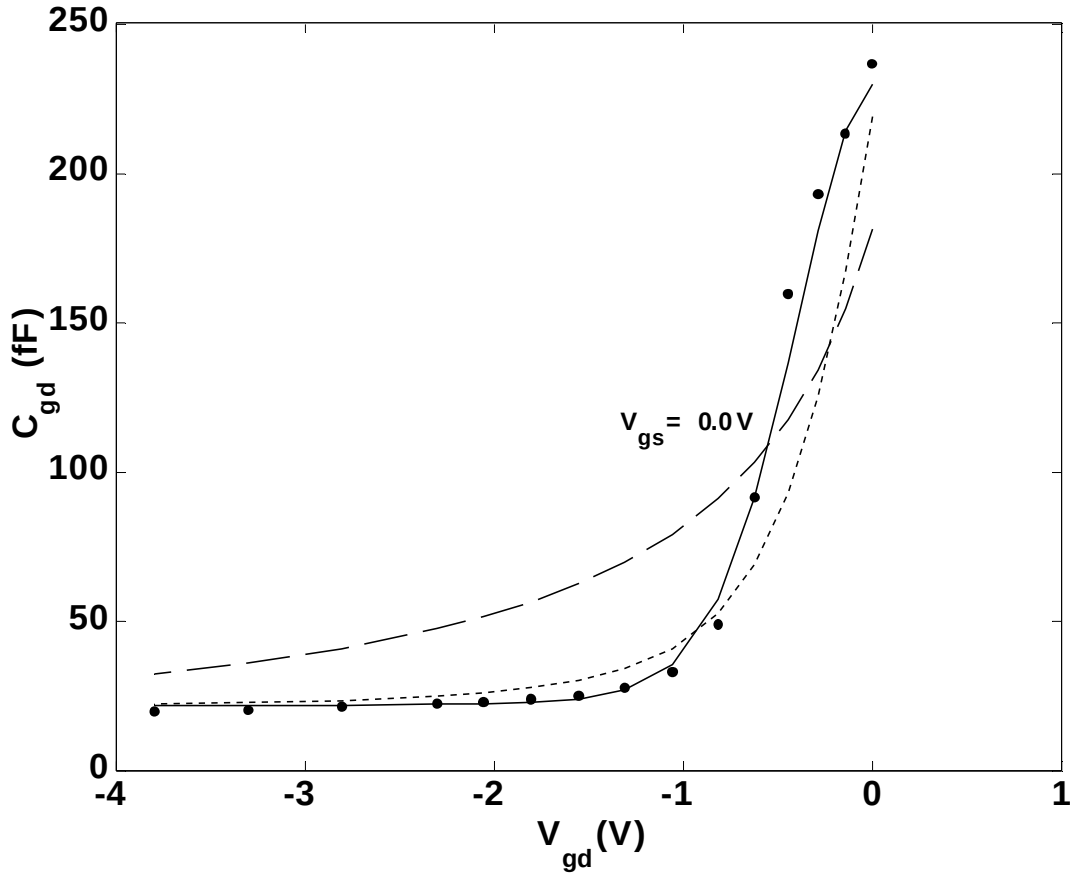


Figure 5.14 Comparison of measured and modeled C_{gd} data (●●● measured data, —— new model, ------ Statz model, – – –Diode junction capacitance model)

To further compare the accuracy of this new model, the maximum fitting error and the RMS error of C_{gs} and C_{gd} obtained from the new model are listed in Tables 5.9

and 5.10 respectively together with the results from the diode junction capacitance model [7] and Statz capacitance model [50]. The calculation is made under six bias levels for V_{gs} (V_{gs}=-2.0V, -1.4V, -1.2V, -1.0V –0.5V, 0.0V), while V_{ds} changes from 0.0V to 4.0V. The first two columns in the tables represent the fitting error in the linear region whilst the second two columns for the saturation region. The error for the entire working region is also given in the last two columns. It can be seen from Tables 5.9 and 5.10 that the new model gives remarkable improvement in accuracy over the diode junction capacitance model and Statz model through each device working region as both of its maximum fitting error and RMS error are greatly reduced. Especially, C_{gs} modeling in linear region is very accurate, whereas the other two models appear to give big error in this region. Modeling error for C_{gd} by the new model appears to be a bit high. However, it still shows great improvement over the other two models. Considering measurement uncertainty, the model is very accurate.

Table 5.9 Comparison of C_{gs} accuracies of Diode Model, Statz Model and the New Model for a 2×150μm GaAs MESFET

	V_{gs}=-2.0V~0.0V V_{ds}=0.6V		V_{gs}=-2.0V~0.0V V_{ds}=2.5V		V_{gs}=-2.0V~0.0V V_{ds}=0.0V~4.0V	
Models	Max. (%)	RMS (%)	Max. (%)	RMS (%)	Max. (%)	RMS (%)
Diode	54.2	23.7	17.5	11.8	65.6	18.3
Statz	26.9	15.6	14.3	7.3	26.9	10.4
New	6.9	4.3	6.5	2.7	10.0	3.6

Table 5.10 Comparison of C_{gd} accuracies of Diode Model, Statz Model and the New Model for a 2×150μm GaAs MESFET

	V_{gs}=-2.0V~0.0V V_{ds}=0.6V		V_{gs}=-2.0V~0.0V V_{ds}=2.5V		V_{gs}=-2.0V~0.0V V_{ds}=0.0V~4.0V	
Models	Max. (%)	RMS (%)	Max. (%)	RMS (%)	Max. (%)	RMS (%)
Diode	36.5	22.1	114.0	57.0	191.5	57.1
Statz	26.9	15.6	14.3	7.3	26.9	28.7
New	14.4	9.5	7.2	4.4	17.6	8.5

The newly proposed gate charge model is more complicated than the diode junction capacitance model and Statz model, and it contains more model parameters. Therefore, it is very accurate in describing device junction capacitances, and it obeys the terminal charge conservation law which helps to solve non-convergence problem in simulation. In addition, the model is continuous. The above discussions show that the new model is capable of accurately representing the actual device behavior over an extended range of operation conditions. The new model can be easily implemented in CAD software, and could be very useful in nonlinear circuit simulation.

5.5 Conclusion

In this chapter, a new large-signal model for GaAs MESFETs is proposed. It consists of an improved drain current expression and a new gate charge model. A set

of power series function is introduced in the improved drain current expression to add on the correlations between modulation parameters α, λ and biasing condition V_{ds} & V_{gs}. The new charge model formulation and its derivatives are continuous. It obeys the terminal charge conservation law, which helps to solve the non-convergence problem in CAD simulation. The performance prediction of the new large-signal model in the linear region, saturation knee region, sub-threshold region and at V_{ds}=0 is greatly improved over the conventional models under various device operating conditions.

Chapter 6

A Ku-band GaAs MESFET MMIC Power Amplifier for Model Verification

6.1 Introduction

In the previous chapters, small signal modelling methodologies and reliable parasitics extraction techniques were presented, also an improved GaAs MESFET I-V model and new gate charge model were proposed. In each chapter, the proposed methodologies and the new large-signal model were verified by extensive measurement data and circuit design. In this chapter, a Ku-band GaAs MESFET MMIC power amplifier has been designed and fabricated based on the proposed new model and extraction methodologies to evaluate this study. The MMIC power amplifier is designed and fabricated using 0.18 um TOSHIBA® GaAs MESFET technology. Instead of foundry models, the new nonlinear model is used for the active GaAs MESFETs used in the design. Measurement and simulation results are compared, including S-parameter analysis, gain compression and harmonic output prediction of this power amplifier.

6.2 A GaAs MESFET MMIC Power Amplifier

6.2.1 Circuit Topology and Specification

To verify the accuracy of the proposed nonlinear model at circuit level, a MMIC power amplifier was designed and fabricated using a 0.18μm GaAs MESFET process. In the amplifier design, models for the active MESFET devices were extracted from on-wafer device measurement data using the proposed new model, and implemented in Agilent MDS using SDD. For passive devices like microstripe lines and capacitors, foundry models were used. The designed amplifier operates from 11.5 to 15 GHz with a gain of 25dB and maximum output power (P_{1dB}) of 36dBm. The detailed design specification of the amplifier is shown in Table 6.1.

Table 6.1 Design Specification of Ku-band MMIC Power Amplifier

Item	Value			Unit
	Minimum	Typical	Maximum	
Working Frequency	11.5	13.0	15.0	GHz
Small Signal Gain	24.8	25.0	26.3	dB
Output Power (P1dB)	35.8	36.0	36.4	dBm
Input Return Loss (S_{11})	12	14	---	dB
Output Return Loss (S_{22})	10	12	---	dB
Die's Size		5×5		MM^2
IC Process	TOSHIBA® 0.18um GaAs MESFET PROCESS			

The circuit topology of the MMIC power amplifier is shown in Figure 6.1. In the design, power combining technique is used with 3-stage topology as shown in Figure 6.1. This amplifier was constructed using fourteen high power GaAs MESFETs. At the input port, RF power is first divided into two identically parts then get amplified through 2-finger GaAs MESFETs. Each 2-finger GaAs MESFET drives two 8-finger GaAs MESFET in parallel, and each of these two 8-finger FET drives another two 16-finger FET in parallel. Due to the largest max drain current capability, eight 16-finger GaAs FETs are adopted in the third stage to meet output power requirement. Finally, the output power is combined at the output port of this GaAs MESFET MMIC power amplifier. These active MESFETs are designed to operate in class AB mode.

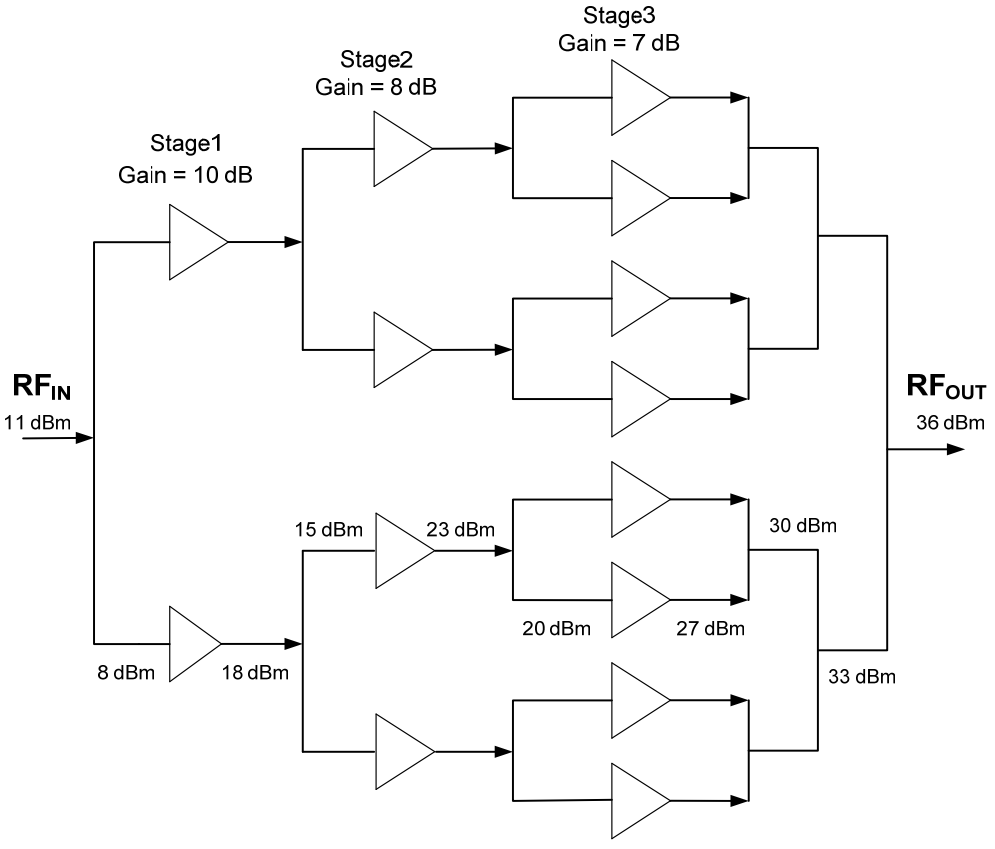


Figure 6.1 Circuit topology of Ku-band GaAs MESFET MMIC power amplifier

Figure 6.2 shows the actual layout microphotograph of the designed GaAs MESFET MMIC power amplifier. As mentioned before in the specification, it has a size of 5mm×5mm.

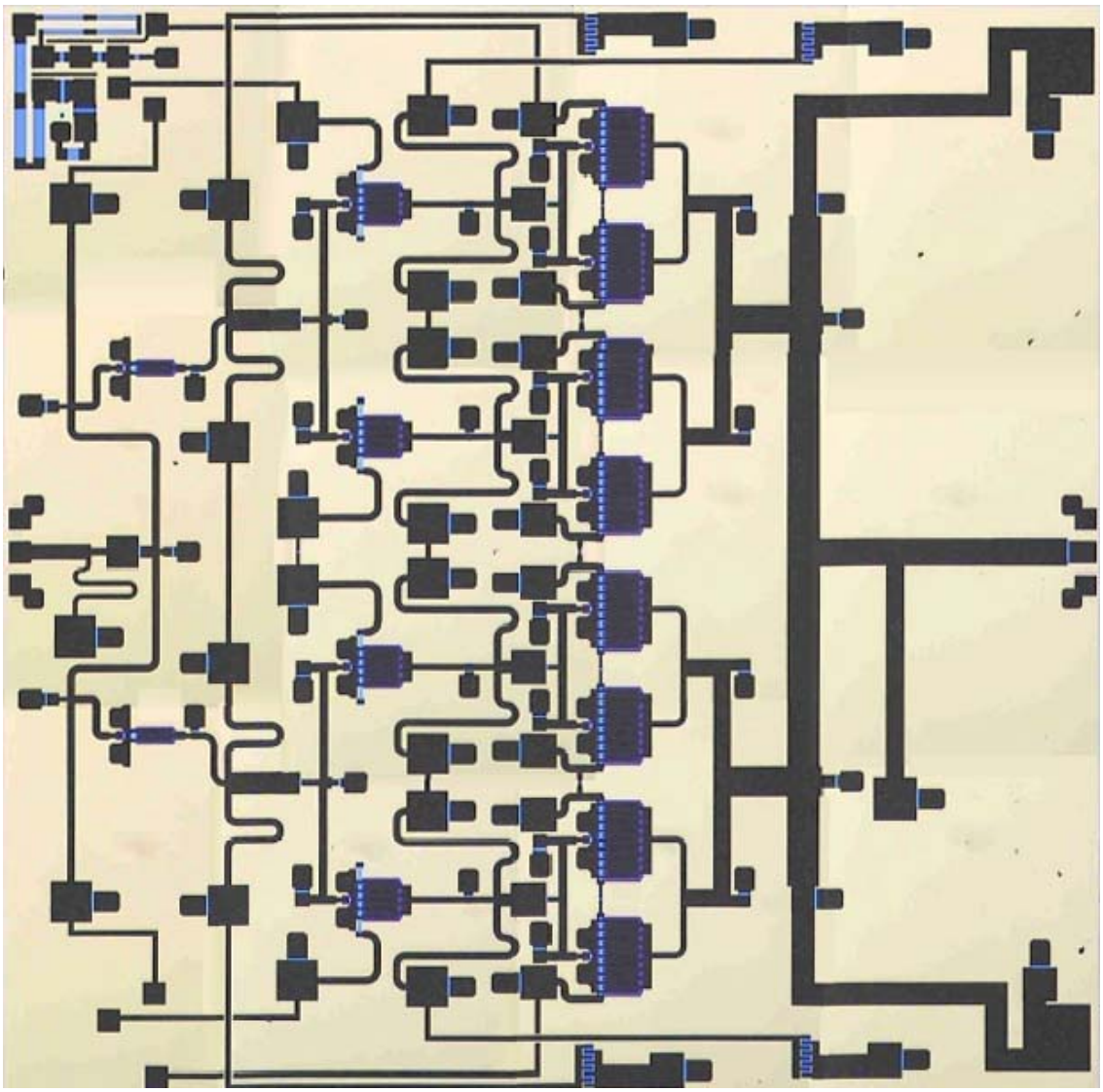


Figure 6.2 Photo of the GaAs MMIC power amplifier layout.

6.2.2 Device Modelling Result

The sizes of the GaAs MESFETs used in the PA design are 2×150μm, 8×150μm and 16×150μm. Figure 5.1 shows the large signal model used in GaAs MESFETs devices modelling. The nonlinear gate current I_{gd} and I_{gs} use the foundry

model. For Ids and capacitance C_{gd} and C_{gs}, the new models are used. Models for the three MESFETs are optimized to fit the measurement result. On-wafer device measurement was made using HP 85124A pulse modelling system. S-parameter data, DC characteristics and pulse I-V measurement data were collected.

The measured and modeled pulse I-V results of the three devices are given in Fig 6.3 to 6.5, with pulse widths smaller than 1μs. These nonlinear modelling results based on pulse I-V measurement were employed in the amplifier design to simulate the large signal RF behavior. Figure 6.6 shows the comparison between the modeled gate capacitance C_{gs}, C_{gd} and the gate capacitances value extracted from small signal model at multi-bias points for the $8 \times 150\mu m$ device. The result is shown for V_{gs}=-2.5~0.25V and V_{ds}=7.0V which is the drain DC biasing point for the MESFET.

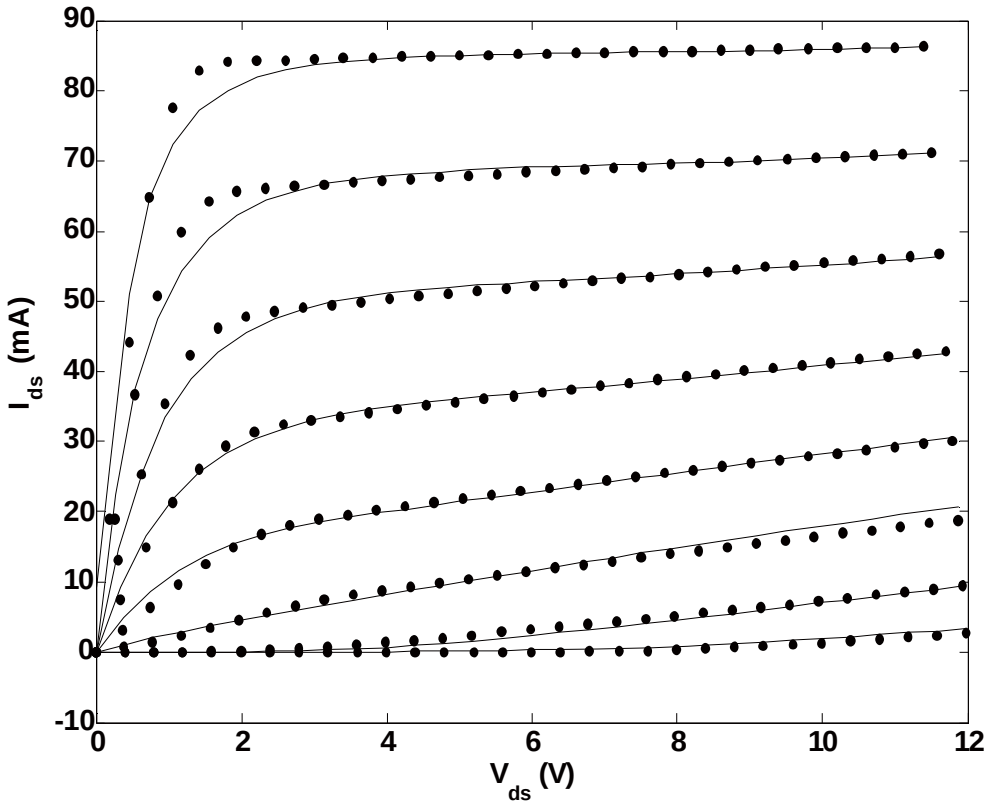


Figure 6.3 Comparison of modeled and measured pulse I-V result for the $2 \times 150\mu m$ device (V_{gs} = –3.0-0.5V, V_{ds} = 0-12V, ●●● measured, —— modeled).

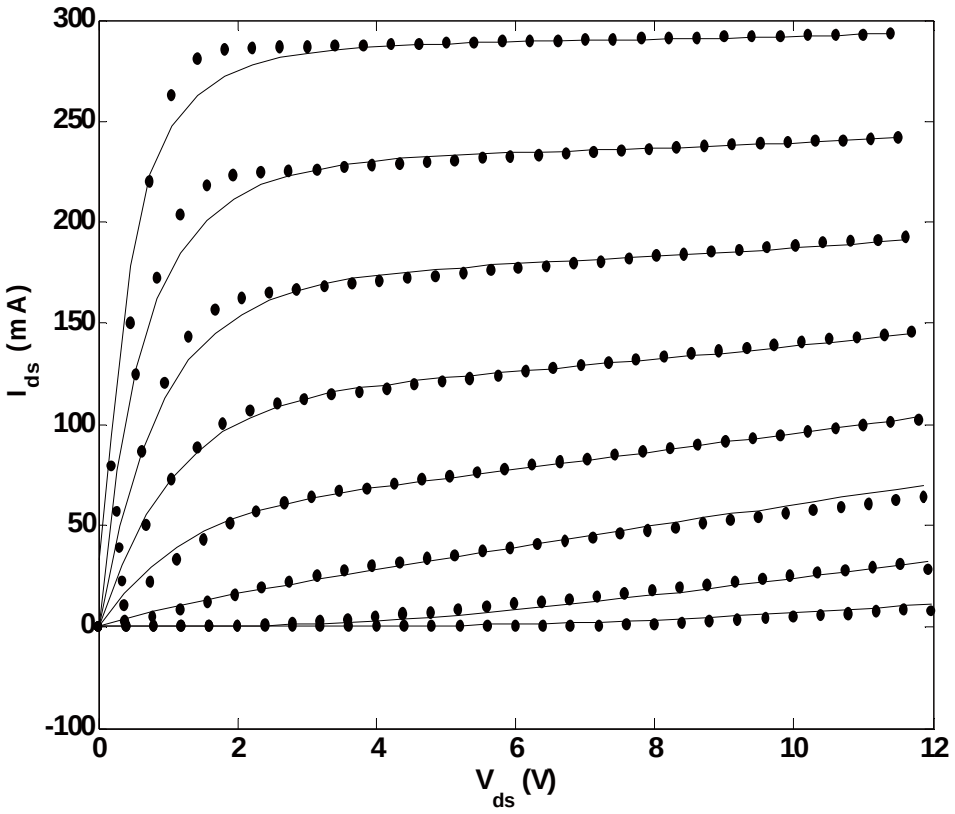


Figure 6.4 Comparison of modeled and measured pulse I-V result for the 8×150μm device (V_{gs} = –3.0-0.5V, V_{ds} = 0-12V, ●●● measured, —— modeled).

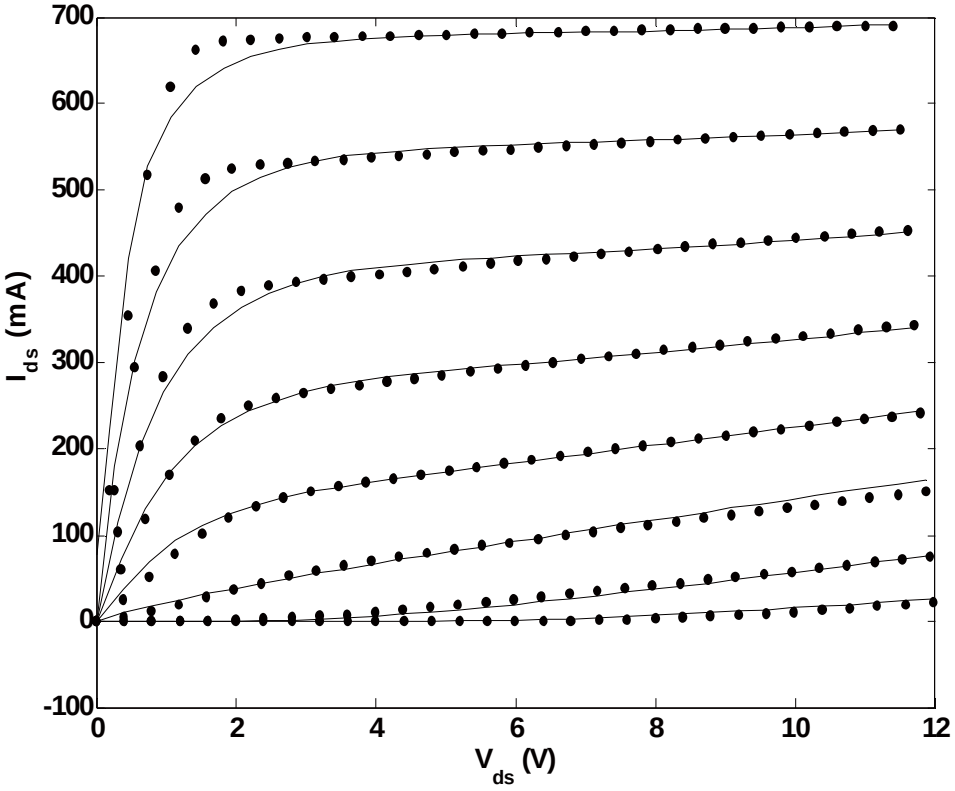


Figure 6.5 Comparison of modeled and measured pulse I-V result for the 16×150μm device (V_{gs} = –3.0-0.5V, V_{ds} = 0-12V, ●●● measured, —— modeled).

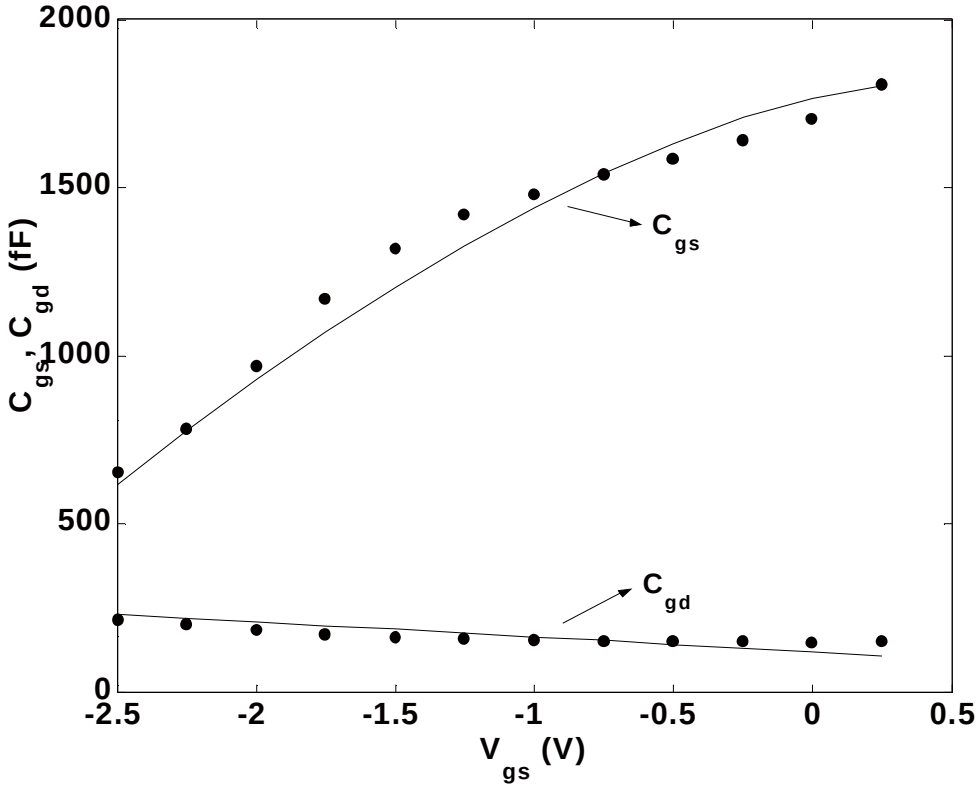


Figure 6.6 Comparison of modeled and measured gate capacitances at V_{ds}=7.0V for the 8× 150μm device (V_{gs} = –2.5-0.25V, ●●● measured, —— modeled).

Figures 6.7 to 6.9 show the comparison between measured and simulated S-parameter for the three device respectively, the devices were biased at V_{gs}=-0.5V, V_{ds}=7.0V and the frequency range is from 500MHz to 20GHz. Figures 6.4 to 6.10 show good agreement between measurement and modeled result for the three GaAs MESFETs.

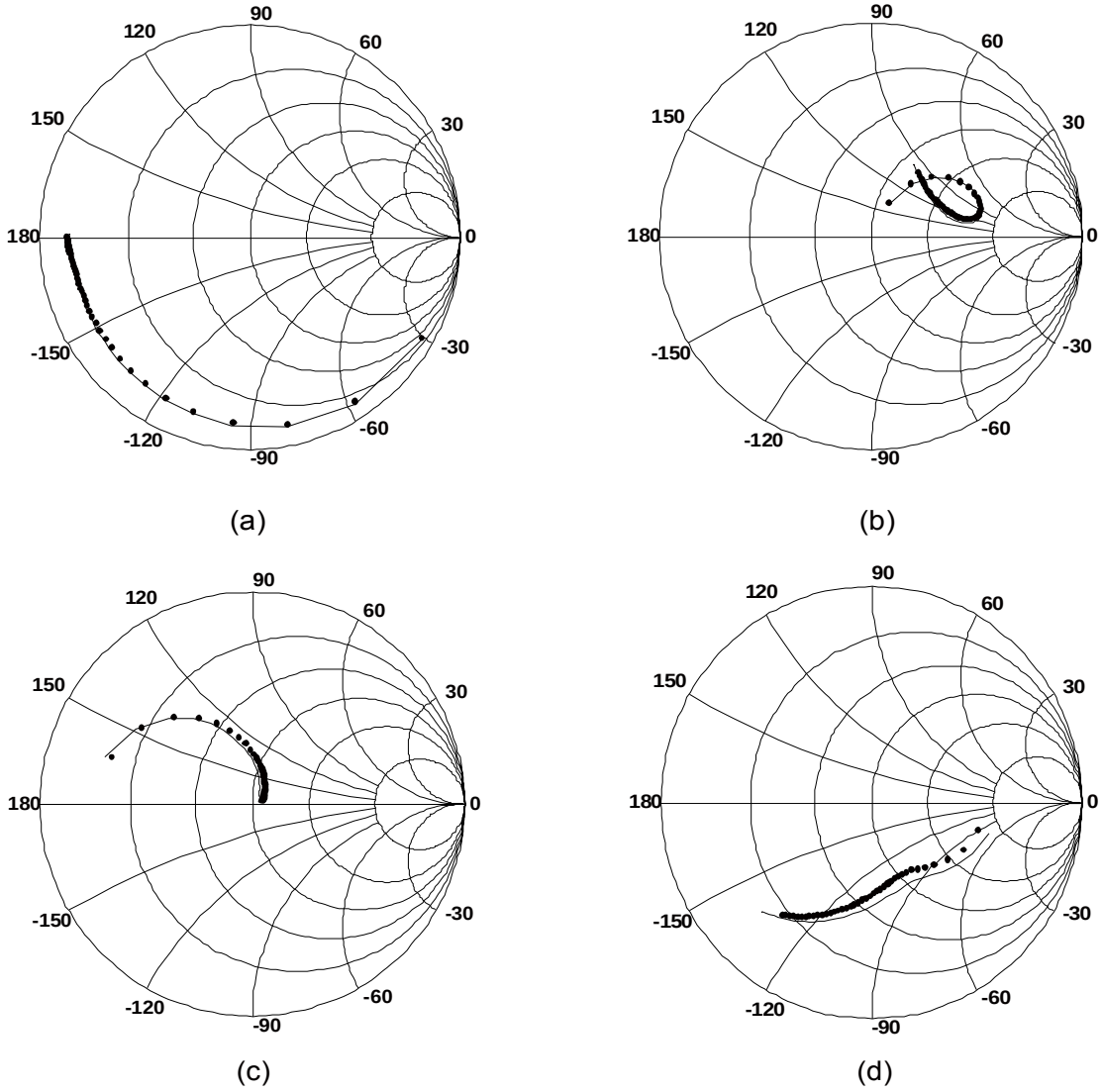
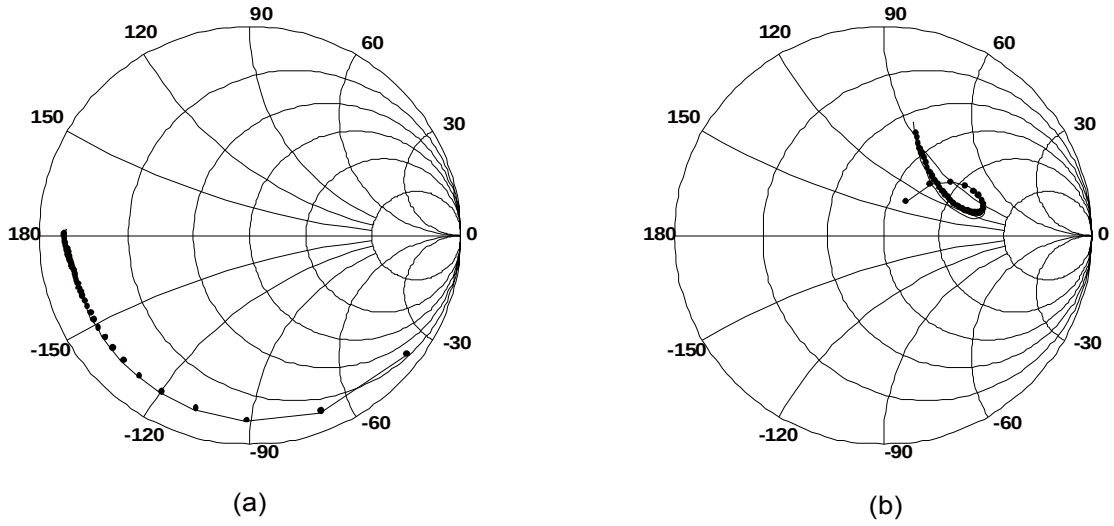


Figure 6.7 Modeled and simulated S-parameter for 2×150μm MESFET (V_{gs}=-0.5V, V_{ds}=7V, f=0.5-20GHz, ●●● measured, —— modeled). (a) S_{11}, (b) S_{12}×10, (c) S_{21}/15, and (d) S_{22}.



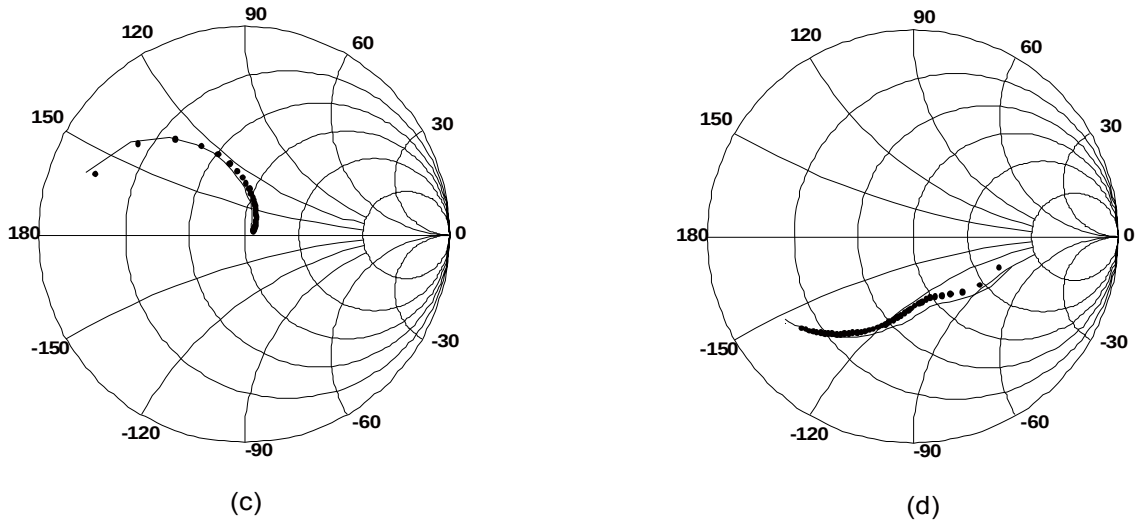


Figure 6.8 Modeled and simulated S-parameter for 8×150μm MESFET (V_{gs}=-0.5V, V_{ds}=7V, f=0.5-20GHz, ●●● measured, —— modeled). (a) S_{11}, (b) S_{12}×10, (c) S_{21}/15, (d) S_{22}.

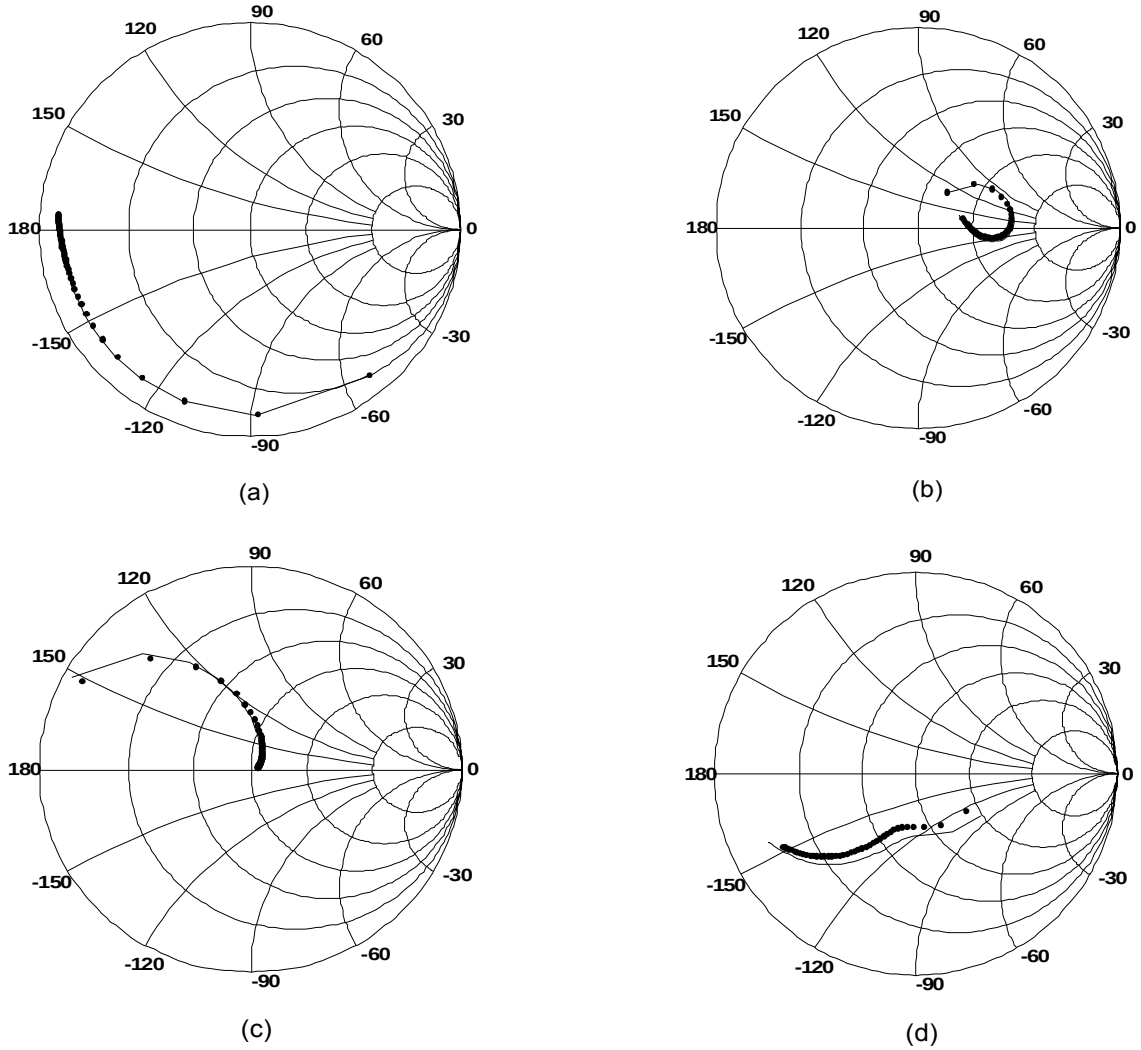


Figure 6.9 Modeled and simulated S-parameter for 16×100μm MESFET (V_{gs}=-0.5V, V_{ds}=7V, f=0.5-20GHz, ●●● measured, —— modeled). (a) S_{11}, (b) S_{12}×10, (c) S_{21}/15, (d) S_{22}.

6.3 Comparison of Simulation and Measurement Results

The measurement of the MMIC power amplifier was accomplished by means of a Cascade probe station. The MMIC power amplifier chip was mounted on a CuW chip carrier. Two PCBs were also constructed as test fixtures to provide the DC power supply. Figure 6.10 is the picture of the test fixture for the power amplifier chip.

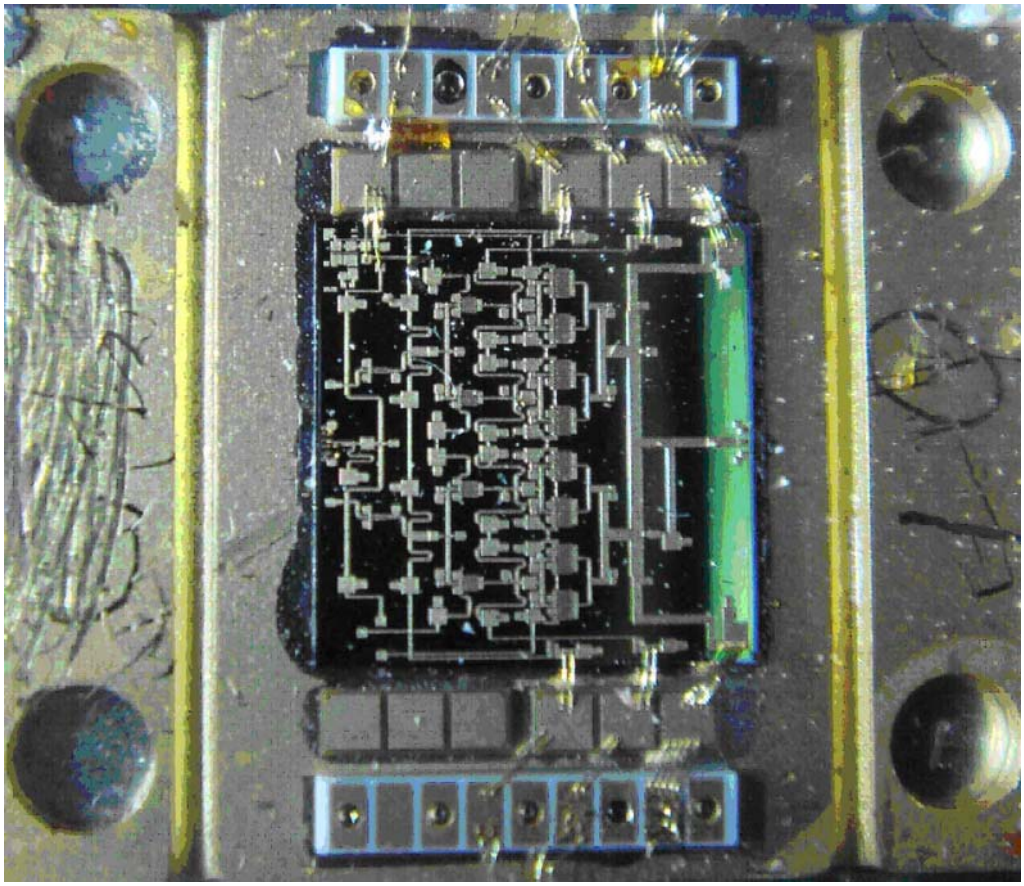


Figure 6.10 Top view of the test chip with DC bias circuit.

Table 6.2 lists all the equipment used in the measurement and Figure 6.11 shows the complete set-up for the power amplifier measurement.

Table 6.2 List of the Equipments Used during the MMIC Power Amplifier Measurement

S-parameter measurement	Power measurement
1x S-parameter Measurement System (Hewlett & Packard) - 8510C Network Analyzer - 85110A S-parameter test set (1~50GHz) - 83650B Signal generator (10M~50GHz) - 11612V Bias Network (400M~50GHz) 1x Cascade Summit 9000 Wafer Probe Station	2x Regulated DC Power Supply - Kenwood for drain voltage supply - GW for gate voltage supply 1x RF Signal Generator 2~20GHz (Rohde & Schwarz) 1x Power meter (Rohde & Schwarz) 1x Peak Power Analyzer (HP 8991A) 1x Spectrum Analyzer 9K~26.5GHz (LG)

Figure 6.11 The complete set-up for the amplifier measurement and testing.

The simulated and measured results for the amplifier power output versus power input response are plotted in Figures 6.12 to 6.14 for input frequency of 11.5GHz, 13GHz and 15GHz respectively. For each measurement and simulation, the input power was swept from 1dBm to 14dBm. Figures 6.12 to 6.14 show excellent agreement between the measured and simulated output power response versus input power level. Using 13GHz input power of Figure 6.13 for example, the measured output power appears to have a higher value than the simulated result for most input power levels, with the maximum difference being 0.8dBm. Although the difference tends to increase as the input excitation level increases, the discrepancies between measured and simulated output power versus input power results at all the three frequencies are very small.

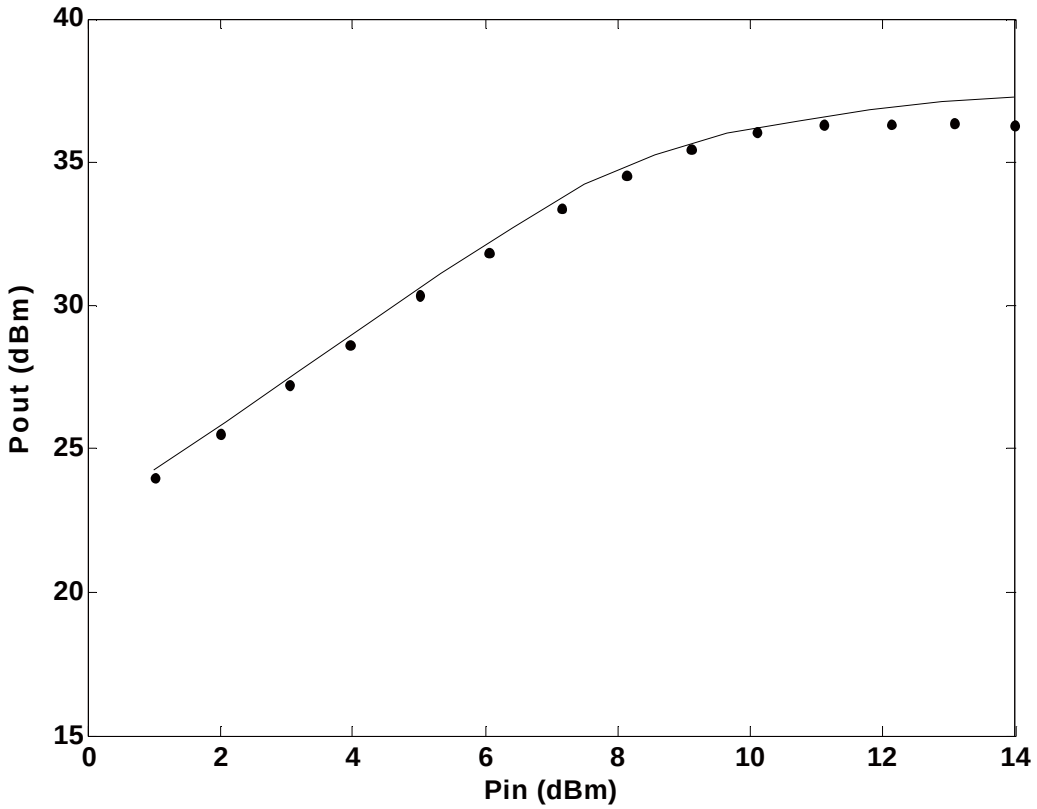


Figure 6.12 Measured and simulated P_{in}-P_{out} behaviour of the Ku-band MMIC Power Amplifier at 11.5 GHz (●●● Measured, —— Simulated).

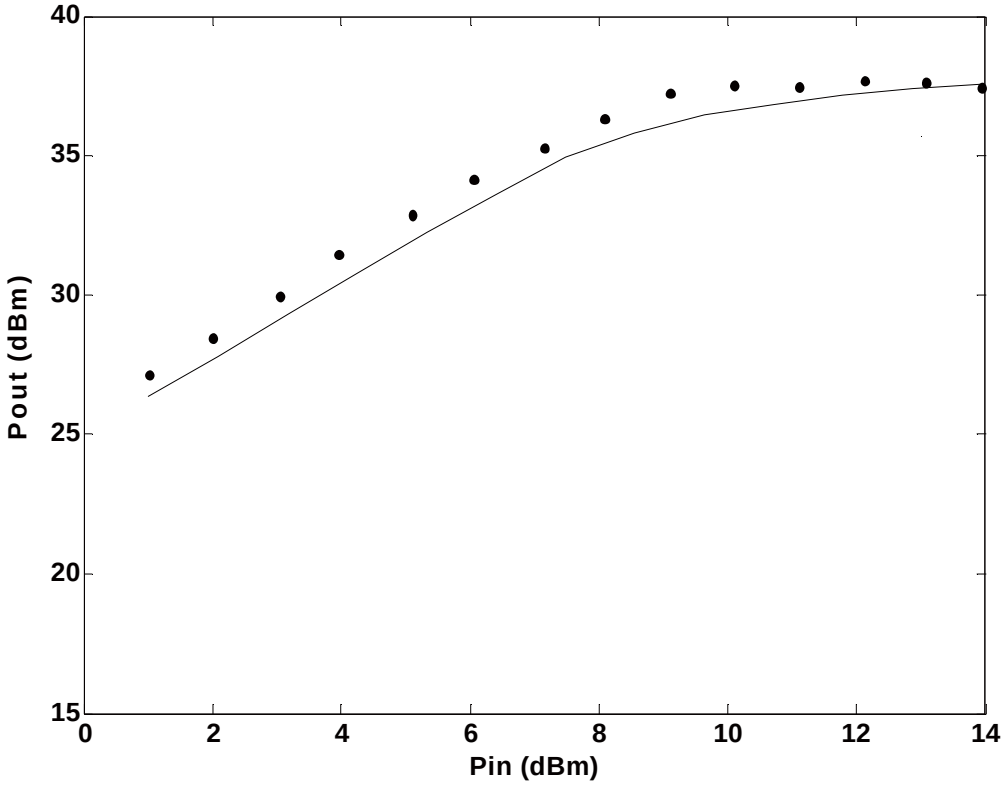


Figure 6.13 Measured and simulated P_{in}-P_{out} behaviour of the Ku-band MMIC Power Amplifier at 13 GHz (●●● Measured, —— Simulated).

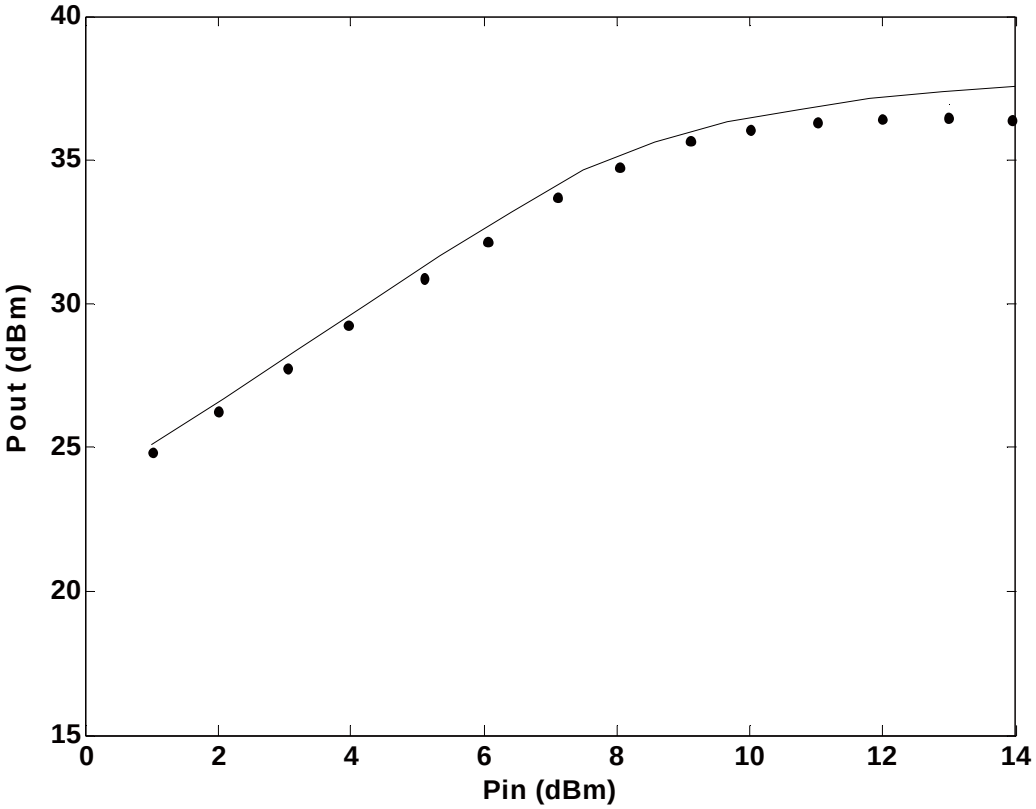


Figure 6.14 Measured and simulated P_{in}-P_{out} behaviour of the Ku-band MMIC Power Amplifier at 15 GHz (●●● Measured, —— Simulated).

In Figure 6.15, the small-signal gain versus frequency performance is plotted. Both simulation and measurement results are shown for comparison. As observed from the figure, the measured and simulated result shows good agreement. In the working frequency range of 11.5-16GHz, the maximum discrepancy between measured and simulated data occurs at 13.7GHz, with the difference being 0.45dB. One possible reason for this discrepancy may be due to the process variation during fabrication of the MMIC amplifier. Taking this into consideration, the measurement result can be considered to be in close agreement with the simulation result.

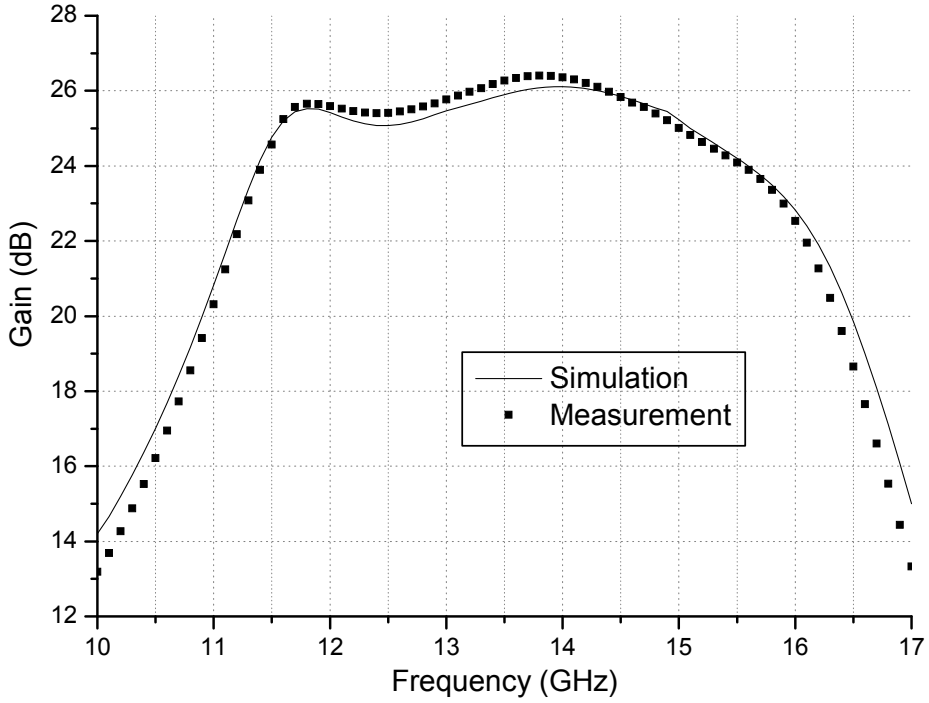


Figure 6.15 Simulated vs. measured S_{21} performance of the Ku-band power amplifier.

Moreover, the third order inter-modulation distortions (TOI) are measured and compared. The two-tone input signals are at 13.00 GHz and 13.01 GHz respectively, and the input power is 5dBm. The experiment results also obtain a good agreement for its TOI characteristics which is shown in Figure 6.16 and 6.17.

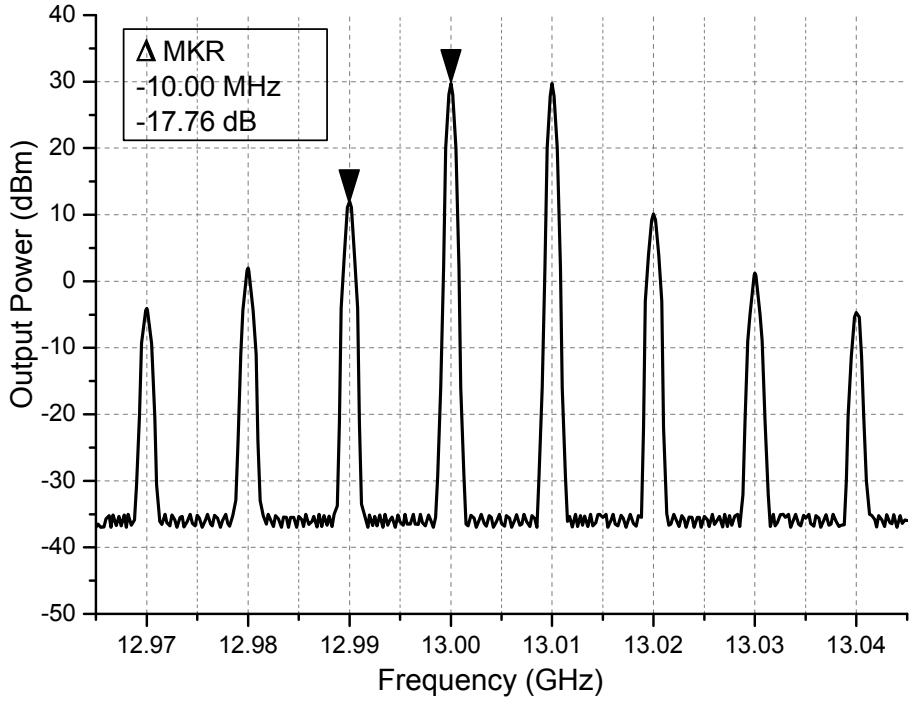


Figure 6.16 Measured third-order intermodulation distortion of the Ku-band power amplifier (P_{in}= 5 dBm).

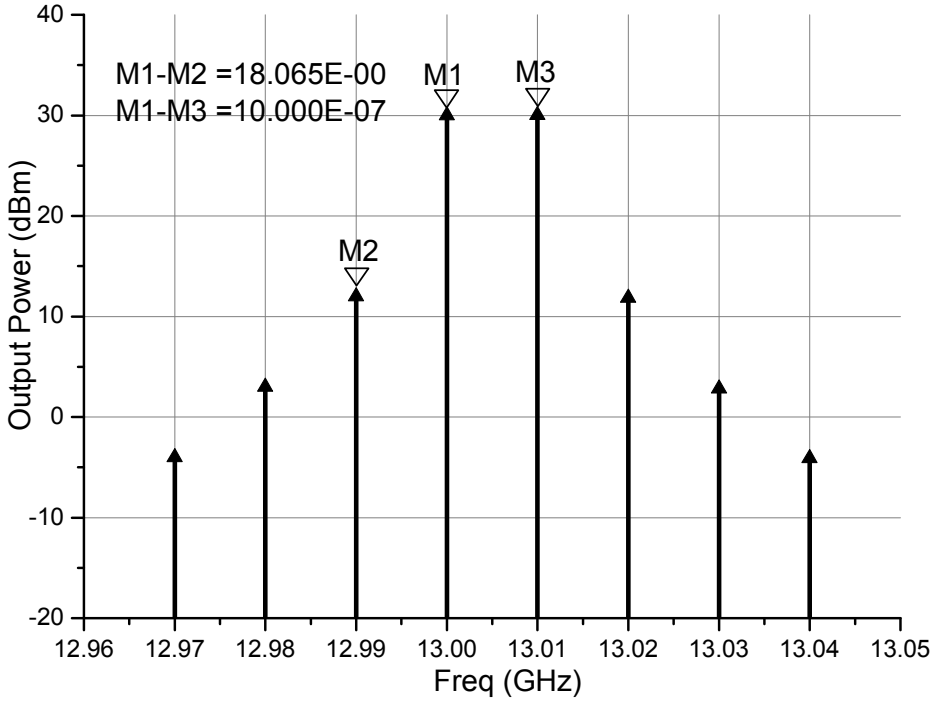


Figure 6.17 Simulated third-order intermodulation distortion of the Ku-band power amplifier (P_{in}= 5 dBm).

From the above MMIC power amplifier design result, it can be seen that the overall simulated response agrees very well with the measurement, especially for output power and gain performance. This demonstrates the accuracy of our new drain current and gate capacitance model, both of which were employed for the simulation of the active MESFETs in the power amplifier.

6.4 Conclusion

In this chapter, the performance of the newly proposed large-signal model was evaluated at the MMIC design level. The comparison between simulation and measurement results clearly confirms the accuracy of the model. The model can be easily implemented into circuit simulators like Agilent® ADS and will be very useful for nonlinear microwave circuit design.

Chapter 7

Conclusion

Today's IC and MMIC development heavily relies on circuit simulation. Simulation and prediction of circuit performance using circuit simulators have become the essential parts of the design flow. Currently, the GaAs MESFETs devices are widely used in high-speed circuits and microwave applications. Therefore, it is in great demand to have accurate models to facilitate the design of circuits employing GaAs MESFETs devices.

In this thesis, extensive work is carried out in the field of GaAs MESFETs modelling. It covers both small signal and nonlinear large signal models of GaAs MESFETs.

This study first involves investigation and comparison of different small-signal parameter extraction techniques. A reliable analytical model extraction approach is subsequently presented. For the first time, a novel analytical approach for extracting all the 15 equivalent circuit elements for FET devices has been proposed. This analytical method could eliminate the conventional cold-FET and hot-FET modelling constraints and allows an ease in inline process tracking. The resulting extrinsic small signal parameters are independent of biasing voltage. In contrast to the conventional

approaches, no subsidiary circuit such as Cold-FET or Hot-FET has been adopted. Comparisons of S-parameter performance in a wide frequency range up to 30GHz have also been presented together with the stabilities of parasitic capacitors to verify the better prediction of this novel analytical extraction approach.

Due to its uniform equivalent circuit, the conventional lumped models, relying on simple linear rules or completely empirical expressions, may not be sufficiently accurate and appropriate at relatively high operating frequencies. Therefore, a creative distributed modelling approach for GaAs MESFET has been proposed in this thesis for modern MMIC design. The novel modelling method is based on accurate electromagnetic simulation of extrinsic passive part of a MESFET transistor. Meanwhile, the intrinsic active part of a MESFET transistor is characterized by a modified small-signal model of transistor. With electromagnetic simulation, this distributed model can be adopted to describe complex coupling effects in device layouts and to predict the electrical characteristics of unconventional device structures for better MMIC performance. Also, this proposed model is accurate enough to provide a more comprehensive and efficient tool for different layout structures transistors optimization and MMIC design. In this proposed distributed modelling method, any more linear or nonlinear description of a FET transistor, which includes lumped or distributed equivalent elements, can be adopted. Therefore, it can be regarded as a preliminary step for the global, fully layout and process oriented design approach.

An empirical approach is employed in our nonlinear modelling due to its accuracy

and simple implementation in circuit simulators. New empirical models for device DC I-V characteristics and gate charge (gate capacitance) behavior, which are the most important GaAs MESFET nonlinear properties, are proposed in this thesis. First, the performances of commonly used I-V and C-V models are investigated. Then, an improved empirical model for GaAs MESFET drain current I-V characteristics has been proposed. A set of power series function is introduced in the improved drain current expression for the correlations between modulation parameters α, λ and biasing condition V_{ds} & V_{gs}. The improved current expression gives better performance from the comparison with the existing drain current models. Gate capacitances are partial derivatives of terminal charge with respect to appropriate voltage. In this work, a new gate charge model has also been proposed to meet the demand in simulating device nonlinear characteristics. Terminal charge conservation has been accounted for in the new gate charge model, and this helps to solve possible non-convergence problem in simulation. The new charge model is more sophisticated than the diode junction capacitance model and Statz model. Compared with these two conventional models, its performance prediction in the linear region, saturation knee region and at V_{ds}=0 is greatly improved. Moreover, it is worth mentioning that the new charge model observes terminal charge conservation, and the model equations and their derivatives are continuous over the entire device operation regions. Therefore, this new large signal model of GaAs MESFETs with improved drain current expression and new charge equations can be easily implemented in CAD software and very useful in the nonlinear microwave circuit simulation.

Model verification was performed along with the introduction of the new large signal model and extraction methodology. Both wafer device and packaged device are used for this purpose. Extensive measurement data was collected including S-parameter at multi-bias conditions, DC I-V characteristics, pulse I-V measurements, and single-tone/two-tone large signal measurement result. Comparison is made between measured result and modeled result. For complete model evaluation, a Ku-band power amplifier was designed and fabricated using 0.18 um TOSHIBA® GaAs MESFET technology. The amplifier is constructed from fourteen high power GaAs MESFETs, power combining technique being used in the design. The new current and charge models are used for the active GaAs MESFETs and the models are implemented in circuit simulator. Measurement and simulated amplifier response shows good agreement.

In conclusion, this thesis has investigated different modelling techniques of GaAs MESFETs and successfully developed novel modelling methods for its small-signal and large-signal models. From both device level and circuit level, these new modelling methods presented have been proven to be capable of accurately representing device small signal and nonlinear behaviors. These new small-signal and large-signal models can be further strengthened by including such effects as frequency dispersion, thermal analysis and by providing the capability of device scaling. These can be addressed in possible future work.

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APPENDIX A

Large Signal Empirical MESFET Models

A.1 Curtice-Quadratic GaAs MESFET Model

One of the first large-signal MESFET models to be used in a large-signal circuit simulator was proposed by Van Tuyl and Liechti [45], and later simplified by Curtice [46]. The Curtice model consists of drain-source current I_{ds}, junction capacitance C_{gs} and C_{gd}.

Empirical equations for drain-source current:

$$I_{ds} = \beta\left(V_{gs} - V_{TO}\right)^2\left(1+\lambda V_{ds}\right)\tanh\left(\alpha V_{ds}\right),$$

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = 2\beta\left(V_{gs} - V_{TO}\right)\left(1+\lambda V_{ds}\right)\tanh\left(\alpha V_{ds}\right), \text{ and}$$

$$g_{ds} = \beta\lambda\left(V_{gs} - V_{TO}\right)^2\tanh\left(\alpha V_{ds}\right) + \beta\alpha\left(V_{gs} - V_{TO}\right)^2\left(1+\lambda V_{ds}\right)\operatorname{sech}^2\left(\alpha V_{ds}\right).$$

Model equations for gate-source capacitance C_{gs} and gate-drain capacitance C_{gs}:

$$C_{gs,gd} = \frac{C_{gs0,gd0}}{\left(1 - \frac{V_{gs,gd}}{V_{bi}}\right)^m}$$

Where, V_{gs} and V_{ds} are the intrinsic terminal voltages, and β, V_{TO}, λ, α, C_{gs0}, C_{gd0} and V_{bi} are model parameters.

A.2 Curtice-Ettenberg (Curtice-Cubic) GaAs MESFET Model

Curtice and Ettenberg [61] altered the square-law relationship between the saturation current and the gate-source voltage of the original Curtice model to a cubic approximation. The new equation for the drain-source current and its derivatives are:

$$I_{ds} = \left(A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3\right)\tanh\left(\gamma V_{ds}\right),$$

$$g_m = \left(A_1 V_2 + 2A_2 V_1 V_2 + 3A_3 V_1^2 V_2\right)\tanh\left(\gamma V_{ds}\right)$$

$$g_{ds} = \left(A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3\right)\operatorname{sech}^2\left(\gamma V_{ds}\right)\gamma - \beta V_{gs}\left(A_1 + 2A_2 V_1 + 3A_3 V_1^2\right)\tanh\left(\gamma V_{ds}\right) + \frac{1}{V_{ds0}}$$

$V_1 = V_{gs}\left[1 + \beta\left(V_{ds0} - V_{ds}\right)\right]$, and

$V_2 = \left[1 + \beta\left(V_{ds0} - V_{ds}\right)\right]$.

Where, V_{gs} and V_{ds} are the intrinsic terminal voltages, A_0, A_1, A_2, A_3, γ and β are model parameters, V_{ds0} is the drain source voltage at which the A_i coefficients are evaluated. Gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} are same as Curtice-Quadratic model.

A.3 Advanced Curtice Quadratic GaAs MESFET Model

The advanced Curtice model is a modified version of the original Curtice model. The pinch-off potential is modified to account for drain-source voltage dependence. The transconductance parameter β is also modified to fit the actual device transconductance behavior.

The drain source current and its derivatives are expressed as [62]:

$$I_{ds} = \beta_{eff} V_{gst}^{VGEXP}\left(1 + \lambda V_{ds}\right)\tanh\left(\alpha V_{ds}\right)$$

$$V_T = V_{TO} + \gamma V_{ds}$$

$$V_{gst} = V_{gs} - V_T$$

$$\beta_{eff} = \frac{\beta}{1 + \mu_{crit} V_{gst}}$$

$$g_m = I_{ds}\left(\frac{VGEXP}{V_{gst}} - \frac{\mu_{crit}}{1 + \mu_{crit} V_{gst}}\right), \text{ and}$$

$$g_{ds} = \beta_{eff} V_{gst}^{VGEXP}\left(1 + \lambda V_{ds}\right)\frac{\alpha}{\cosh^2\left(\alpha V_{ds}\right)} + \beta_{eff} V_{gst}^{VGEXP}\lambda \tanh\left(\alpha V_{ds}\right) - g_m \gamma$$

Where, V_{gs} and V_{ds} are the intrinsic terminal voltages, β, μ_{crit}, γ, λ, α, V_{T0}, and VGEXP are model parameters.

A.4 Statz Model (Statz Raytheon GaAs MESFET Model)

The drain source current and its derivatives are expressed as [58]:

For $0<V_{ds}<3/\alpha$,

$$I_{ds} = \frac{\beta\left(V_{gs} - V_{TO}\right)^2}{1 + b\left(V_{gs} - V_{TO}\right)}\left[1 - \left(1 - \frac{\alpha V_{ds}}{3}\right)^3\right]\left(1 + \lambda V_{ds}\right),$$

$$g_m = \left[1 - \left(1 - \frac{\alpha V_{ds}}{3}\right)^3\right]\left(1 + \lambda V_{ds}\right)\left[\frac{2\beta\left(V_{gs} - V_{TO}\right)}{1 + b\left(V_{gs} - V_{TO}\right)}\right] - \frac{b\beta\left(V_{gs} - V_{TO}\right)^2}{\left[1 + b\left(V_{gs} - V_{TO}\right)\right]^2},$$

$$g_{ds} = \left[1 - \left(1 - \frac{\alpha V_{ds}}{3}\right)^3\right]\lambda + \alpha\left(1 + \lambda V_{ds}\right)\left(1 - \frac{\alpha V_{ds}}{3}\right)^2\frac{\beta\left(V_{gs} - V_{TO}\right)^2}{1 + b\left(V_{gs} - V_{TO}\right)},$$

For $V_{ds} \geq 3/\alpha$,

$$I_{ds} = \frac{\beta\left(V_{gs} - V_{TO}\right)^2}{1 + b\left(V_{gs} - V_{TO}\right)}\left(1 + \lambda V_{ds}\right),$$

$$g_m = \frac{\left[1 + b\left(V_{gs} - V_{TO}\right)\right]2\beta\left(V_{gs} - V_{TO}\right) - b\beta\left(V_{gs} - V_{TO}\right)^2}{\left[1 + b\left(V_{gs} - V_{TO}\right)\right]^2}\left(1 + \lambda V_{ds}\right),$$

$$g_{ds} = \frac{\lambda\beta\left(V_{gs} - V_{TO}\right)^2}{1 + b\left(V_{gs} - V_{TO}\right)}.$$

Model equations for gate-source capacitance C_{gs} and gate-drain capacitance C_{gd}:

For $V_n > V_{max}$,

$$Q_g = C_{gs0}\left[2V_{bi}\left(1 - \sqrt{1 - \frac{V_{\max}}{V_{bi}}}\right) + \frac{V_n - V_{\max}}{\sqrt{1 - \frac{V_{\max}}{V_{bi}}}}\right] + C_{gd0}V_{eff2}$$

$$C_{gs} = \frac{\partial Q_g}{\partial V_{gs}} = \frac{C_{gs0}K_2K_1}{\sqrt{1 - \frac{V_{\max}}{V_{bi}}}} + C_{gd0}K_3$$

$$C_{gd} = \frac{\partial Q_g}{\partial V_{gd}} = \frac{C_{gs0}K_3K_1}{\sqrt{1 - \frac{V_{\max}}{V_{bi}}}} + C_{gd0}K_2$$

For $V_n \le V_{max}$, $Q_g = 2C_{gs0}V_{bi}\left(1 - \sqrt{1 - \frac{V_n}{V_{bi}}}\right) + C_{gd0}V_{eff2}$,

$$C_{gs} = \frac{\partial Q_g}{\partial V_{gs}} = \frac{C_{gs0}K_2K_1}{\sqrt{1 - \frac{V_n}{V_{bi}}}} + C_{gd0}K_3$$

$$C_{gd} = \frac{\partial Q_g}{\partial V_{gd}} = \frac{C_{gs0}K_3K_1}{\sqrt{1 - \frac{V_n}{V_{bi}}}} + C_{gd0}K_2$$

Where

$$V_n = \frac{1}{2}\left[V_{eff1} + V_{T0} + \sqrt{(V_{eff1} - V_{T0})^2 + \delta^2}\right]$$

$$V_{eff1} = \frac{1}{2}\left[V_{gs} + V_{gd} + \sqrt{(V_{gs} - V_{gd})^2 + \left(\frac{1}{\alpha}\right)^2}\right]$$

$$V_{eff2} = \frac{1}{2}\left[V_{gs} + V_{gd} - \sqrt{(V_{gs} - V_{gd})^2 + \left(\frac{1}{\alpha}\right)^2}\right]$$

V_{max} = 0.5, δ=0.2, and

$$K_1 = \frac{\partial V_n}{\partial V_{eff1}} = \frac{1}{2}\left[1 + \frac{V_{eff1} - V_{T0}}{\sqrt{(V_{eff1} - V_{T0})^2 + \delta^2}}\right]$$

$$K_2 = \frac{\partial V_{eff1}}{\partial V_{gs}} = \frac{\partial V_{eff2}}{\partial V_{gd}} = \frac{1}{2}\left[1 + \frac{V_{gs} - V_{gd}}{\sqrt{(V_{gs} - V_{gd})^2 + \left(\frac{1}{\alpha}\right)^2}}\right]$$

and $K_3 = \frac{\partial V_{eff1}}{\partial V_{gd}} = \frac{\partial V_{eff2}}{\partial V_{gs}} = \frac{1}{2}\left[1 - \frac{V_{gs} - V_{gd}}{\sqrt{(V_{gs} - V_{gd})^2 + \left(\frac{1}{\alpha}\right)^2}}\right]$.

A.5 Chalmers Model

Angelov et al. [64] presented a new nonlinear model that is capable of describing both MESFET and HEMT. The model equations are:

$$I_{ds} = I_{pk}\left[1 + \tanh(\psi)\right](1 + \lambda V_{ds})\tanh(\alpha V_{ds}),$$

$$\psi = P_1(V_{gs} - V_{pk}) + P_2(V_{gs} - V_{pk})^2 + P_3(V_{gs} - V_{pk})^3 + \ldots,$$

$$C_{gs} = C_{gs0}\left[1 + \tanh(\psi_1)\right]\left[1 + \tanh(\psi_2)\right]$$

$$C_{gd} = C_{gd0}\left[1 + \tanh(\psi_3)\right]\left[1 - \tanh(\psi_4)\right]$$

$$\psi_1 = P_{0gsg} + P_{1gsg}V_{gs} + P_{2gsg}V_{gs}^{\ 2} + P_{3gsg}V_{gs}^{\ 3} + \ldots$$

$$\psi_2 = P_{0gsd} + P_{1gsd}V_{ds} + P_{2gsd}V_{ds}^{\ 2} + P_{3gsd}V_{ds}^{\ 3} + \ldots$$

$$\psi_3 = P_{0gdg} + P_{1gdg}V_{gs} + P_{2gdg}V_{gs}^{\ 2} + P_{3gdg}V_{gs}^{\ 3} + \ldots, \text{ and}$$

$$\psi_4 = P_{0gdd} + \left(P_{1gdd} + P_{1cc}\right)V_{ds} + P_{2gdd}V_{ds}^{\ 2} + P_{3gdd}V_{ds}^{\ 3} + \ldots$$

APPENDIX B

TEE Network and PI Network Conversion

B.1 TEE Network to PI Network Conversion

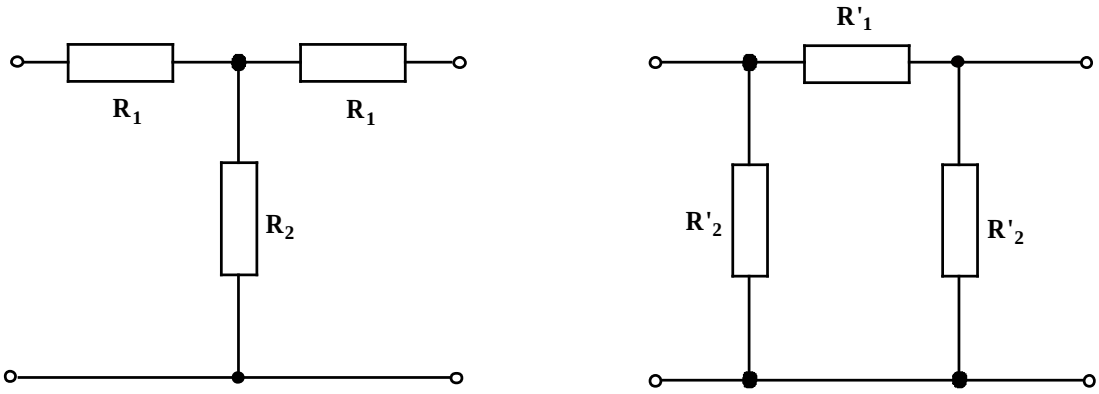

Figure B.1 TEE network to PI network conversion.

$$R_1^{'} = \frac{R_2}{R_1} \cdot 2R_2 + R_1 ; \quad R_2^{'} = 2R_2 + R_1$$

B.2 PI Network to TEE Network Conversion

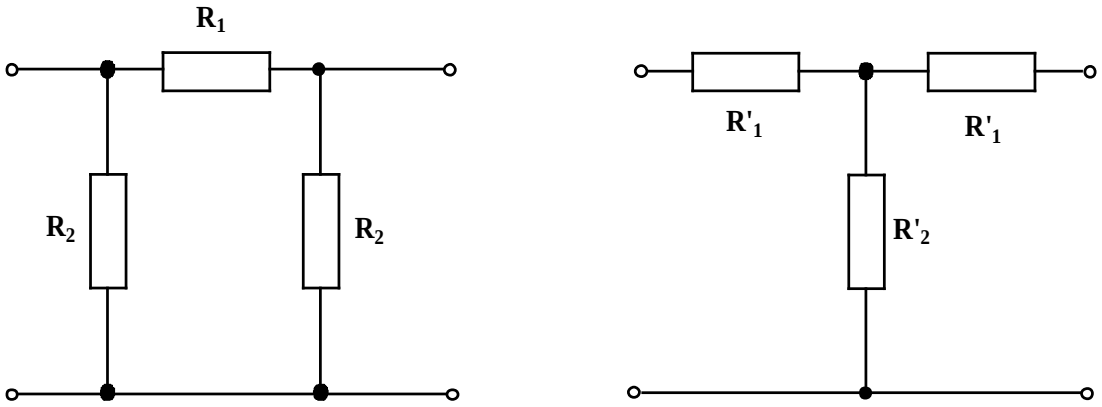

Figure B.2 PI network to TEE network conversion.

$$R_1^{'} = \frac{R_1 \cdot R_2}{2R_2 + R_1} ; \quad R_2^{'} = \frac{R_2^{\,2}}{2R_2 + R_1}$$

APPENDIX C

Small Signal Parameter Extraction Formulation

Figure 3.1 shows the most commonly used GaAs MESFET small signal equivalent circuit topology. The intrinsic device has seven elements C_{gs}, C_{gd}, R_i, g_m, τ, g_{ds} and C_{ds}. The parameter extraction formulae are separately derived for two methods based on different control voltage in the equivalent circuit.

C.1 Control Voltage V Taken from the Voltage Between C_{gs}

For the small-signal equivalent circuit in Figure 3.1, the Y-parameter of the intrinsic device can be expressed as the following form if the control voltage V is taken from the voltage between Cgs.

$$Y_{\text{int}} = \begin{bmatrix} \dfrac{\omega^2 R_i C_{gs}^{\ 2}}{1+\omega^2 R_i^{\ 2} C_{gs}^{\ 2}} + j\omega\left(C_{dg} + \dfrac{C_{gs}}{1+\omega^2 R_i^{\ 2} C_{gs}^{\ 2}}\right) & -j\omega C_{dg} \\ \dfrac{g_m e^{-j\omega\tau}}{1+j\omega C_{gs} R_i} - j\omega C_{dg} & g_{ds} + j\omega(C_{dg} + C_{ds}) \end{bmatrix}$$

$$\omega R_i C_{gs} = \frac{\mathrm{Re}\left(Y_{11}\right)}{\mathrm{Im}\left(Y_{11}\right) + \mathrm{Im}\left(Y_{12}\right)}$$

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12})}{\omega}$$

$$g_{ds} = \mathrm{Re}(Y_{22})$$

$$C_{ds} = \frac{\mathrm{Im}(Y_{22}) + \mathrm{Im}(Y_{12})}{\omega}$$

$$C_{gs} = \frac{\left[\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12})\right]^2 + \left[\mathrm{Re}(Y_{11})\right]^2}{\omega \cdot \left[\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12})\right]}$$

$$R_i = \frac{\mathrm{Re}(Y_{11})}{\left[\mathrm{Im}(Y_{11}) - \omega C_{gd}\right]^2 + \left[\mathrm{Re}(Y_{11})\right]^2} = \frac{\mathrm{Re}(Y_{11})}{\left[\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12})\right]^2 + \left[\mathrm{Re}(Y_{11})\right]^2}$$

$$g_m = \sqrt{\left(\left(\mathrm{Re}(Y_{21})\right)^2 + \left[\mathrm{Im}(Y_{21}) - \mathrm{Im}(Y_{12})\right]^2\right)\left(1 + \omega^2 C_{gs}^2 R_i^2\right)}$$

$$\tau = \frac{1}{\omega}\arcsin\left(\frac{\mathrm{Im}(Y_{12}) - \mathrm{Im}(Y_{21}) - \omega C_{gs} R_i \,\mathrm{Re}(Y_{21})}{g_m}\right)$$

C.2 Control Voltage V Taken from the Voltage across R_i and C_{gs}

For small-signal equivalent circuit in Figure 3.1, the Y-parameter of the intrinsic device can be expressed as the following form if the control voltage V is taken from the voltage cross C_{gs} and R_i.

$$Y_{\mathrm{int}} = \begin{bmatrix} \dfrac{\omega^2 R_i C_{gs}^{\ 2}}{1 + \omega^2 R_i^{\ 2} C_{gs}^{\ 2}} + j\omega\left(C_{dg} + \dfrac{C_{gs}}{1 + \omega^2 R_i^{\ 2} C_{gs}^{\ 2}}\right) & -j\omega C_{dg} \\ g_m e^{-j\omega\tau} - j\omega C_{dg} & g_{ds} + j\omega(C_{dg} + C_{ds}) \end{bmatrix}$$

$$g_m = \sqrt{\left(\mathrm{Re}(Y_{21})\right)^2 + \left[\mathrm{Im}(Y_{21}) - \mathrm{Im}(Y_{12})\right]^2}$$

$$\tau = \frac{1}{\omega}\arctan\left(\frac{\mathrm{Im}(Y_{12}) - \mathrm{Im}(Y_{21})}{\mathrm{Re}(Y_{21})}\right)$$

The expressions for C_{gd}, g_{ds}, C_{ds}, C_{gs}, and R_i are the same as those described in Appendix C.1.