HIGH PERFORMANCE CONTROL OF A THREE-PHASE PWM RECTIFIER

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2008

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A THESIS SUBMITTED

FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

DEPARMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2008

Acknowledgements

I would like to express my gratitude to all those who gave me their support to complete this thesis. First and foremost, I am deeply indebted to my supervisor Prof. Ramesh Oruganti whose constant guidance, sustaining encouragement and stimulating suggestions helped me all the time during my doctoral research and writing up this thesis. Without him, I could not have finished my research work smoothly. As a mentor, he was always there to discuss my ideas, to help me to think through my problems and to teach me to write academic papers. I would like to express my sincere thanks to him for his patience during my learning process. As an experienced advisor, he was always there to help me to reduce stress due to my challenging research, to advise research schedules and to provide opportunities for me to attend conferences and future career. I would like to thank for his considerateness and kindness to me and all his students. I learnt a lot from him not only to be a precise researcher but also to be a nice person.

I would like to give my thanks to Prof. Panda, my co-supervisor, for his invaluable advice and help throughout my study. I will never forget his always timely help and his unreserved supervision in the advanced control field. Without his effort, it would have taken longer for me to finish my research.

I would also like to thank Prof. Bhat for his encouragement, guidance and support. From him, I learnt how to be a precise scholar.

I would like to thank Prof. Loh Ai Poh, Prof. Dipti Srinivasan, Prof. Xu Jian-Xin and Prof. Wang Qin-Guo for their valuable comments and suggestions.

I am grateful to National University of Singapore for supporting this research project through the research grant R-263-000-190-112.

I thank lab officers Mr. Woo Ying Chee, Mr. Chandra, Mr. Teo Thiam Teck and Mr. Seow Hung Cheng for their kind help whenever I have troubles. Special thanks go to Mr. Abdul Jalil Bin Din for his prompt PCB fabrication services and Mr. Johari Bin Khamis for his timely components provision.

As a research scholar, my stay in the Centre for Power Electronics of NUS was made pleasant by many of my friends. Foremost among them is Dr. Viswanathan Kanakasabai, who not only shares with me his knowledge, but also his happiness. Among the other friends, I would like to thank Chen Yu, Cao Xiao, Heng Deng, Hu Ni, Krishna Mainali, Kong Xin, Li Yanlin, Liu Min, Qin Meng, Marecar Hadja, Niu Pengying, Ravinder Pal Singh, Sahoo S. K., Wang Wei, Wu Xinhui, Wei Guannan, Xu Xinyu,Ye Zhen, Yang Yuming and Zhou Haihua.

Deep in my heart are special thanks to my husband, Deng Heng. His love has accompanied me through bad and good moments. Finally, I want to thank my parents who made all this possible. I dedicate this thesis to them and to Prof. Ramesh Oruganti.

Table of Contents

SUMMARY

The three-phase boost type PWM rectifier has been widely used as an improved utility interface in recent years since it has the potential to operate with sinusoidal line currents at a desired power factor and with nearly constant *dc* output voltage with a small output capacitor. However, due to its inherent multi-input and multi-output (MIMO) non-linear structure and non-minimum phase feature, designing a proper controller for such a converter is generally a challenging task even under balanced supply voltage operating conditions. In addition, supply voltage imbalance, which is a common occurrence in a power system, complicates the control task further.

The aims of the work reported in this thesis can be brought under three categories:

- To develop an accurate but simple control-oriented model for a PWM rectifier under balanced operating conditions
- To evaluate reported power regulation schemes for a PWM rectifier under unbalanced operating conditions and to propose and investigate new schemes if needed.
- To investigate high performance current tracking schemes for the control of unbalanced line currents in a PWM rectifier and to propose and investigate new schemes if needed.

Firstly, to facilitate controller design and to give meaningful insight into the

behavior of PWM rectifiers, a simple dual single-input single-output (SISO) model was developed by separating the *d*-axis and the *q*-axis dynamics through appropriate feed-forward decoupling and near unity power factor assumption. The effectiveness of the proposed model was verified experimentally in both the frequency and time domains. It was found that the proposed *d*-axis equivalent SISO model was similar to a traditional *dc*-*dc* boost converter. This finding opens up possible new avenues for controlling three-phase PWM rectifier systems with the well-developed analysis and design techniques of *dc*-*dc* converters. As examples, the voltage-mode and current-mode controllers commonly used with *dc*-*dc* controllers were successfully implemented on the PWM rectifier, and this also further justifies the effectiveness of the proposed dual SISO model.

Next, in order to maintain constant *dc* output voltage and sinusoidal line currents when operating under unbalanced supply voltage conditions, an output power control (OPC) method is proposed. Also, an improved realization of the existing partial output power control (POPC) method, which results in overcoming the performance limitations encountered with the POPC method reported in literature, is suggested. A third new method, called voltage oriented control (VOC) method capable of excellent input side performance was also proposed. Experimental comparisons among the four control schemes, namely, the existing input power control (IPC) method and the proposed schemes, OPC, POPC with the proposed improved realization, and the VOC methods were carried out using a 1 kW laboratory prototype. Experimental results show that both the proposed OPC method

and the POPC method with the improved realization can provide high input side and output side performances. Investigations have also been presented to show that the effective power factor (EPF) definition evaluates the power flow condition more fairly than the more common vector power factor (VPF) definition in an unbalanced system.

Thirdly, in order to achieve excellent input side performance, current tracking schemes based on both integral variable structure control (IVSC) and iterative learning control (ILC) were proposed and implemented in the stationary frame. Experimental comparisons with the widely used dual current controller (DPIC) and a newly developed P + Resonant controller (P+RC) were also carried out. Results show that the proposed ILC based hybrid current controller (Hybrid ILC) achieves excellent steady-state performance with good transient response suggesting this to be a promising technique for controlling periodic currents commonly existing in power converters applications.

In conclusion, this thesis studies fully the issues related a PWM rectifier system operating under both balanced and unbalanced conditions and also suggests future work related to this field.

List of Publication Associated to the Research Work

Journal papers:

1. B. Yin, R. Oruganti, S. K. Panda, and A. K. S. Bhat, "An output-power-control strategy for a three-phase PWM rectifier under unbalanced supply conditions," *IEEE Trans. on Industrial Electronics*, vol. 55, No. 5, May 2008, pp:2140-2151.
2. B. Yin, R. Oruganti, S. K. Panda, and A. K. S. Bhat, "A simple single-input-single-output (SISO) model for a three-phase PWM rectifier," *IEEE Trans. on Power Electronics*, vol. 24, no.3, March, 2009, pp:620-631.

Conference papers:

1. B. Yin, R. Oruganti, S. K. Panda, and A. K. S. Bhat, "A novel instantaneous power control strategy for a PWM rectifier under unbalanced input voltage conditions," in *Proc.* the 30th *IEEE* Conf. *Industrial Electronics Society*, Busan, Korea 2004, pp251-256.
2. B. Yin, S. K. Panda, R. Oruganti and A. K. S. Bhat, "A Novel Current Regulation Scheme for Boost Type PWM Rectifier Based on Iterative Learning Control," in *Proc.* the *IEEE Conf. Power System Technology*, Singapore. 2004, pp: 1786-1791.
3. B. Yin, R. Oruganti, S. K. Panda, and A. K. S. Bhat, "High-Performance Control of a Boost Type PWM Rectifier under Unbalanced Operating Conditions with Integral Variable Structure Control," *Proceedings of the 36th IEEE Power Electronics Specialists Conference (PESC 2005)*, June 2005, pp:1992-1997.
4. B. Yin, R. Oruganti, S. K. Panda, and A. K. S. Bhat, "Control of a three-phase PWM rectifier Based on a dual single-input single-output linear model," *The 6th International Conf. on Power Electronics and Drive Systems*, 2005, pp: 456-461.
5. B. Yin, R. Oruganti, S. K. Panda, and A. K. S. Bhat, "Experimental verification of a dual single-input single-output model of a three-phase boost-type PWM Rectifier" *in Proc. the 31th IEEE Conf. Industrial Electronics Society*, North Carolina, USA, 2005.
6. B. Yin, R. Oruganti, S. K. Panda, and A. K. S. Bhat, "Performance comparison of voltage mode control and current mode control of a three-phase PWM Rectifier based on a dual SISO model," *in Proc. the 32th IEEE Conf. Industrial Electronics Society*, Paris, France 2006, pp: 1908-1914.

List of Tables

List of Figures

CHAPTER 1

INTRODUCTION

1.0 Background

In many power electronic applications, an *ac*-to-*dc* converter, widely known as a 'rectifier' [1, 2], is used as a front-end converter for interfacing the power electronic equipment with the utility system. Traditionally, such *ac*-to-*dc* power conversion has been accomplished by means of diodes which are essentially uncontrolled power semiconductor switches，or by thyristors which may be viewed as semi-controlled switches. In several power electronic systems, such as in switch-mode *dc* power supplies, *ac* motor drives or *dc* servo drives, the *ac* to *dc* uncontrolled diode rectifier or the line-commutated thyristor rectifier, has been used at the front end to provide an uncontrolled or controlled *dc* output voltage.

However, such implementations can cause severe harmonic pollution problems

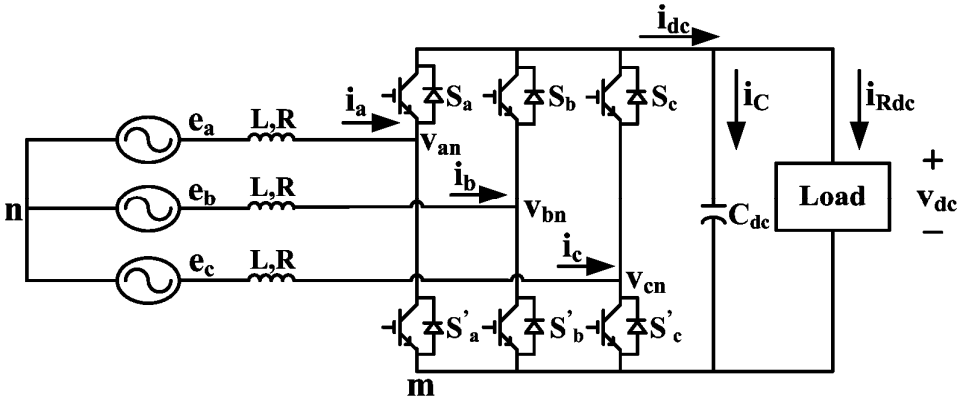


Fig. 1.1 Configuration of a three-phase boost-type PWM rectifier

in the utility grid. As the current drawn from the utility is highly distorted with a poor power factor, problems such as voltage distortion, additional losses due to high RMS current value, possible over-voltages due to system resonance conditions, and errors in metering and malfunction of utility relays are known to occur [3, 4]. Due to these problems, limits have been placed in recent times on the harmonic content of the line current of utility interfaced equipment by many standards and guidelines [5-7], such as IEC 1000-3-2, IEC 1000-3-4 and IEEE Std 519. In all such cases, where the amount of distorted current injected into the utility is limited by harmonic standards and guidelines, *ac* to *dc* rectifiers using diodes or thyristors cannot normally be used.

In addition, rectifiers using diodes or thyistors can only provide low quality *dc* output voltage. A large capacitor is normally required for smoothing the *dc* output voltage which increases the converter size, make the dynamic response slow and can decrease its reliability [1]. In the case of thyristor controlled rectifiers, the use of a large output capacitor also increases the system time constant and this when coupled with the low switching frequency degrades the dynamic performance of the system.

Due to the above, the demand for improved utility interface in various applications has increased substantially. By using semiconductor switches such as IGBTs (Insulated-Gate Bipolar Transistor), high frequency switching and better input and output performances become possible.

Among the available high performance three-phase rectifiers, the boost-type

Pulse-Width-Modulated (PWM) rectifier incorporating IGBTs (Fig. 1.1) has become the leading candidate in most three-phase *ac*-to-*dc* applications because of its salient attributes. By properly controlling a boost-type PWM rectifier, line currents drawn from the utility can be made to be sinusoidal and in phase with their corresponding supply voltages. Besides input current shaping and power factor correction, the *dc* output voltage provided by the rectifier can be maintained constant without the need for any large output-side energy storage elements. This is a consequence of the fact that the instantaneous power flow in any balanced three-phase *ac* system is constant. In addition, such a rectifier has bidirectional power delivery capability which is required in many *ac* and *dc* motor drive systems. These desirable attributes have made such PWM rectifiers very popular in three-phase *ac*-to-*dc* applications, for example, as the front-end converter for uninterruptible power supply systems (UPS) and inverter-fed variable-voltage and variable-frequency (VVVF) *ac* motor drives in industrial processes [8].

However, controlling the PWM rectifier system is not an easy task even under balanced operating conditions due to the complex nature of the system. The desirable attributes of PWM rectifiers mentioned in the previous paragraph can be fully realized under ideal balanced supply voltage conditions only with a properly implemented control scheme. Additionally, the presence of supply voltage imbalance in a PWM rectifier system will typically lead to forgoing the advantages by giving rise to a *dc* output voltage ripple at twice the line frequency as well as low order harmonics in the utility side line currents.

In order to take full advantage of the strengths of the PWM rectifier under both balanced and unbalanced supply voltage conditions, it is important to investigate the issues associated with a three-phase boost-type PWM rectifier operating under both these conditions. The following two sections will present briefly the issues associated with the operation of a three-phase PWM rectifier.

1.1 PWM rectifier system operating under balanced supply voltage conditions

Normally, the control objectives of a PWM rectifier system are to regulate the *dc* output voltage and to shape the line currents so as to achieve unity power factor operation on the *ac* side. However, designing a proper controller for such a PWM rectifier system is generally a challenging task even in a balanced system. The available state-space-averaged model [26, 28] for the three phase rectifier under balanced supply conditions does not give much insight into the design of the controllers due to the rectifier's complex non-linear multi-input multi-output (MIMO) structure and the presence of a non-minimum phase feature in the system operation. Besides complicating the controller design, the presence of the non-minimum phase feature in this non-linear MIMO system also prevents us from fully understanding the behavior of the PWM rectifier system.

Extensive research has been carried out by other researchers on the modeling and control of PWM rectifier systems. Some simple MIMO linear models have been developed in [18, 19]. However, in these models, the non-minimum phase property

inherent in the PWM rectifiers has been neglected. Although this simplifies the system model and hence the controller design, the resulting closed-loop system will only operate stably within certain ranges of system parameters. This is because the information on the location of the non-minimum phase property determines the realizable closed loop bandwidth of the PWM rectifier system. Thus, it is important for a designer be able to include in the PWM rectifier model the non-minimum phase property in order to predict system performance and stability more accurately.

Therefore, issues associated with the PWM rectifier system operating under balanced supply voltage conditions mainly involve the need for the development of a simple, accurate and informative model with which the behavior of a PWM rectifier can be explained and explored easily and control schemes can be designed and implemented without much difficulty.

1.2 PWM rectifier system operating under unbalanced supply voltage conditions

Although the PWM rectifier has the flexibility to control the power flow between the utility and the *dc* load, its performance can be sensitive to supply voltage imbalance [8]. To maintain a good operating environment for power customers, levels of imbalance of utility supply voltages should be typically maintained at less than 1% as prescribed by IEEE Std 1159-1995 [6]. However, due to poor enforcement of these standards, the imbalance in input supply is a common phenomenon in power utility, particularly in a weak *ac* system and may emerge

because of the following reasons [5-11].

- Uneven distribution of single phase loads. Voltage imbalances due to imbalances in phase loads can be particularly severe if large single phase loads, such as arc furnaces are used [6-7].
- Asymmetrical winding of transformers which will cause different voltage drops in each phase.
- Unbalanced transmission impedance per phase which can also give rise to voltage imbalances.
- Influences due to fault or damage occurring in the transmission network.

Regardless of the causes, appearance of supply voltage imbalance will severely affect the behavior of a PWM rectifier. It would prevent the advantages of the rectifier system, such as low distortion input current and low ripple output *dc* voltage, from being fully realized.

Thus, the issues associated with a PWM rectifier system operating under unbalanced supply voltage conditions are mainly centered around two aspects, namely, developing a power regulation scheme with which the potential of a PWM rectifier can be partially or fully realized and current tracking schemes with which the required unbalanced line currents can be effectively tracked.

1.3 Research objectives

The overall purpose of the research work reported in this thesis is to investigate and solve some of the main control problems associated with a three-phase

boost-type PWM rectifier operating under both balanced and unbalanced supply voltage conditions.

The main objectives of the research work are as follows:

To develop a simple, yet physically insightful model that is useful in the analysis and control of the PWM rectifier under balanced supply conditions.

To investigate and propose power regulation scheme(s) which can provide both high input performance and high output performance for a PWM rectifier system operating under unbalanced supply conditions.

To evaluate the input and output performance of power regulation schemes under unbalanced supply conditions with appropriate performance indices.

To propose effective current tracking scheme(s) which can achieve high performance control of the unbalanced line currents in an unbalanced system.

1.4 Thesis contributions

The major contributions of the thesis are as follows:

1. Dual single-input single-output (SISO) model for a PWM rectifier:

A dual SISO model, which simplifies the widely used state-space-averaged model, has been developed for the three-phase PWM rectifier operating under balanced supply conditions. This model which is based on neglecting the effect of the *q*-axis current on the *d*-axis dynamics is shown to be true under unity or near unity power factor conditions. The proposed model helps us significantly in

understanding the underlying behavior of a PWM rectifier system. It is also a useful tool in the design of the controllers. These aspects are explained in greater detail below:

- In the proposed dual SISO model, the actual MIMO system is decoupled into two large-signal SISO systems in which the *q*-axis model is a first order linear system determining the power factor regulation, whereas the *d*-axis model is a second-order non-linear system determining the power delivery. The roles played by the *d*-axis and the *q*-axis models in power delivery and power factor management are clearly brought out by the model. This finding provides a better understanding of the underlying operating principle of the PWM rectifier.
- The complex non-minimum phase feature inherent in an *ac*-to-*dc* rectifier becomes a simple RHP zero appearing in the small-signal control-to-output transfer function of the proposed *d*-axis model. This finding gives insight into achievable closed loop performance simplifying the controller design process for a PWM rectifier system.
- The fact that the *d*-axis large-signal SISO model is similar to that of the well-known *dc*-*dc* boost converter makes it possible to extend the system analysis and control design concepts of *dc*-*dc* converters to the three-phase rectifiers. In order to verify this, voltage mode and current mode controllers, which are two well documented control techniques for *dc*-*dc* boost converters, were designed and implemented based on the proposed small

signal dual SISO model. These successful implementations demonstrate the effectiveness of the dual SISO model. They also allow the possibility of better controller designs in the future based on the non-linear large signal dual SISO model.

2. Output power control scheme (OPC):

An output power control (OPC) scheme has been proposed for improved performance under unbalanced supply voltage conditions. A good feature of the proposed method is that the current commands are given by a set of simple equations which can be easily implemented. The controller is shown to achieve excellent output performance and near unity vector power factor at the input. The performance of the controller is shown to be significantly better than the existing control schemes identified in this thesis work as 'input power control (IPC) method' [48-49] and 'partial output power control (POPC) method'[1] [52].

3. Improving the existing 'partial output power control (POPC) method':

The control method proposed in [52], identified in the present work as the POPC method aims to realize unity vector power factor operation at the input while achieving excellent *dc* side performance. This method was then investigated, particularly the reason for its failure in fulfilling the performance goals. An additional closed loop in the process of generation of the current commands was

[1] Please note that this method has been called "modified output power control method" in our earlier publications [99]. However, we feel that the name "partial output power control method" describes this method more accurately.

found to be inadvertently introduced; this was identified as the possible reason for the degradation in performance encountered in experimental investigations.

An improved implementation of the POPC method has been proposed. With the proposed realization, both high input side performance and output side performance have been achieved experimentally.

4. Evaluation of power regulation schemes:

Based on a study of the definition of power factor, it was found that the concept of ‘vector power factor (VPF)’, which is normally used to evaluate the power flow condition in a three phase system, only considers the effect due to reactive power flow in the system. It has been identified in this work that the concept of 'effective power factor (EPF)' is more appropriate to assess the power flow condition as it takes into account the extent of system imbalance besides reactive power in degrading the efficiency of power transmission.

Using the concept of EPF, the performances of the different ‘power-oriented’ control schemes, viz., IPC, OPC and POPC (with the modification suggested), are all evaluated in detail and compared. An additional control method, called ‘voltage oriented control (VOC)’ with potential for high input side performance was also suggested and evaluated. Of the methods evaluated, the OPC method and the POPC method (with the suggested modification) were shown to provide optimal performances.

5. High performance tracking current control scheme:

All PWM rectifier schemes require accurate and fast acting current control schemes in order to achieve good input side performance. The current control scheme must be capable of high tracking performance under steady-state without compromising the dynamic performance. Two high performance tracking current control schemes, 1) a hybrid current control scheme based on iterative learning control (Hybrid ILC) and 2) an integral variable structure control (IVSC) have been proposed and implemented for this purpose. The proposed schemes were compared with two schemes proposed by other researchers, viz., dual PI current controller (DPIC) and P + Resonant current controller (P+RC). A detailed comparison of the results shows that the Hybrid ILC current control scheme provides the best steady-state performance and good transient performance suggesting that it is a promising control technique for this application. This current control technique can also be applied for the control of periodic currents commonly existing in other power converter applications.

1.5 Thesis organization

The reminder of the thesis is organized as follows:

Chapter 2 presents a literature survey on control schemes for a PWM rectifier under both balanced and unbalanced operating conditions. Models of the PWM rectifier used in these different control schemes are also introduced in this chapter.

Chapter 3 develops a dual SISO model for a three-phase rectifier and verifies the proposed model by experimentally examining the open loop characteristic of the *d*-axis model in both frequency domain and time domain. Both direct voltage mode controller and inner current loop based schemes are designed and implemented based on the proposed model in this chapter.

Chapter 4 investigates the power regulation methods for PWM rectifier systems under unbalanced operating conditions. An output power control (OPC) method is then proposed to provide high output performance and good input performance. With the OPC method, the resulting vector power factor is shown to be close to unity.

Chapter 5 is devoted to the improvements carried out in the implementation of the partial output power control (POPC) method. In this chapter, the reasons for the poor performance with this method are first investigated and attributed to the particular implementation method adopted. Another way to realize the POPC scheme has also been proposed. With this implementation, it was shown that this control method results in excellent performance both on the output side and on the input side for the given operating conditions.

In Chapter 6, it is suggested that the concept of effective power factor should be used to evaluate power regulation schemes instead of vector power factor and the reasons for the same are discussed. Using the concept of EPF, the performances of the different ‘power-oriented’ control schemes, viz., IPC, OPC and POPC (with the modification suggested) and an additional ‘voltage oriented control (VOC)’ are

assessed by comparison based on peak-to-peak voltage on the *dc* output voltage, total harmonic distortion (THD) in the each phase current and the achieved effective power factor.

Chapter 7 proposes current tracking schemes based on integral variable structure control (IVSC) and iterative learning control (ILC). For comparison purposes, the widely used dual current controller (DPIC) and the recently developed P + Resonant current (P+RC) controller are also discussed and implemented. It is shown that the ILC based hybrid control scheme (Hybrid ILC) achieves excellent stead-state performance and good dynamic response.

Chapter 8 summarizes the work presented in the thesis and suggests future work that may be carried out in this area.

CHAPTER 2
LITERATURE SURVEY ON CONTROL SCHEMES FOR THREE-PHASE PWM RECTIFIERS

2.0 Introduction

As mentioned in Chapter 1, the aim of a control system under balanced operating condition is to fully realize the performance goals that are achievable in a PWM rectifier system. On the other hand, under unbalanced operating conditions, the control system should aim to compensate the supply voltage imbalance and realize the performance goals to a maximal extent. In this chapter, literature survey on control schemes for a three-phase boost-type PWM rectifier system operating under both balanced and unbalanced conditions is presented. The pros and cons of various solutions mentioned in the literature are briefly discussed. This sets the stage for the research work reported in the thesis from Chapter 3 onwards.

Another class of rectifier is unidirectional rectifier. The requirement for the unidirectional rectifier, for example, telecom application control concepts, is even more severe, including phase loss. However, this is not within scope of this research and is not considered here.

As these control schemes are proposed based on different models, a brief review of the models of a PWM rectifier system available in the literature is presented at the beginning of this chapter. This background information will be helpful in better understanding the control schemes discussed in this chapter and also the rest of the

thesis.

The problems associated with PWM rectifiers operating under balanced conditions are also explored in Appendix A. A good understanding of these problems is beneficial in identifying the key issues which should be addressed by the proposed solutions.

2.1 Models of a PWM rectifier operating under balanced supply voltages

In this section, models of the PWM rectifier which have been used in different control schemes are introduced.

2.1.1 Model in the *a-b-c* frame

The voltage-source type PWM rectifier is shown in Fig. 1.1, where e_a, e_b, e_c represent supply voltages and i_a, i_b, i_c represent input currents. Parameters L and R are the inductance value and the resistance value of the synchronous inductance. The voltage equation of the rectifier in the *a-b-c* frame can be expressed as:

$$\bar{e}_n = L\frac{d\bar{i}}{dt} + R\bar{i} + \bar{v}_n, \tag{2.1}$$

where $\bar{e}_n = \begin{bmatrix} e_{an} & e_{bn} & e_{cn} \end{bmatrix}^T$, $\bar{i} = \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^T$ and $\bar{v}_n = \begin{bmatrix} v_{an} & v_{bn} & v_{cn} \end{bmatrix}^T$.

The averaged voltage at the terminal of the rectifier $\bar{v}_m$ can be represented with averaged switching functions as follows.

$$\bar{v}_m = \frac{(\bar{u}+1)\cdot v_{dc}}{2} \tag{2.2}$$

where $\bar{u} = [u_a \quad u_b \quad u_c]^T$ is switching functions in *a-b-c* frame within a range of [-1 1]. Also $\bar{v}_m = [v_{am} \quad v_{bm} \quad v_{cm}]^T$, $v_{mn} = -\frac{1}{3}(v_{am} + v_{bm} + v_{cm})$ and $\bar{v}_n = \bar{v}_m + v_{mn} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \begin{bmatrix} v_{am} \\ v_{bm} \\ v_{cm} \end{bmatrix}$ with $e_{an} + e_{bn} + e_{cn} = 0$.

The averaged voltage at the terminal of the rectifier $\bar{v}_m$ can also be represented by:

$$\bar{v}_m = \bar{d} \cdot v_{dc}, \tag{2.3}$$

where $\bar{d} = [d_a \quad d_b \quad d_c]^T$ is the duty ratio in the *a-b-c* frame. The values of d_a, d_b and d_c will be within the range [0 1].

The relationship between the averaged switching functions and duty ratio can be expressed as follows:

$$\bar{d} = \frac{1 + \bar{u}}{2}. \tag{2.4}$$

The differential equation for the *dc* side of the rectifier can be expressed as:

$$C\frac{dv_{dc}}{dt} = i_{dc} - i_{Rdc}, \tag{2.5}$$

where $i_{dc} = \frac{(u_a + 1) \cdot i_a}{2} + \frac{(u_b + 1) \cdot i_b}{2} + \frac{(u_c + 1) \cdot i_c}{2} = \frac{u_a \cdot i_a + u_b \cdot i_b + u_c \cdot i_c}{2}$ with $i_a + i_b + i_c = 0$ and $i_{Rdc} = \frac{v_{dc}}{R_{dc}}$.

Equations (2.1) and (2.5) represent the PWM rectifier system model in *a-b-c* frame. All the variables in (2.1) except v_{dc}, i_{dc} and i_{Rdc} will be *ac* quantities under steady-state operation.

2.1.2 Model in the stationary frame (SF)

The rectifier system model can be converted into two decoupled systems through *a-b-c* to α-β transformation as follows.

$$\begin{cases} L\dfrac{di_\alpha}{dt} = e_\alpha - Ri_\alpha - v_\alpha \\ L\dfrac{di_\beta}{dt} = e_\beta - Ri_\beta - v_\beta \end{cases}, \tag{2.6}$$

where i_α , i_β and e_α , e_β are the α-axis and β-axis currents and voltages respectively. Variables v_α and v_β are the α-axis and β-axis control inputs with $v_\alpha = u_\alpha v_{dc}/2$ and $v_\beta = u_\beta v_{dc}/2$, respectively, where u_α, and u_β are the α-axis and β-axis averaged switching functions.

The differential equation for the *dc* side of the rectifier can be expressed as

$$C\frac{dv_{dc}}{dt} = i_{dc} - i_{Rdc}, \tag{2.7}$$

where $i_{dc} = \dfrac{3\cdot(u_\alpha \cdot i_\alpha + u_\beta \cdot i_\beta)}{4}$ and $i_{Rdc} = \dfrac{v_{dc}}{R_{dc}}$.

2.1.3 Models in the synchronously rotating frame (SRF)

For modeling and control design, it is convenient to transform the three-phase variables into a synchronously rotating frame by the Park transformation [48], as variables will become *dc* quantities in the SRF under balanced steady-state operating conditions. The voltage equations in the SRF can be written as follows:

$$\begin{cases} L\dfrac{di_d}{dt} = -Ri_d + \omega L i_q + e_d - v_d \\ L\dfrac{di_q}{dt} = -Ri_q - \omega L i_d + e_q - v_q \end{cases} \tag{2.8}$$

Here, e_d, e_q and i_d, i_q denote the supply voltages and the supply current components in the *d*-axis and *q*-axis, respectively. Variables v_d, v_q are the *d*-axis and *q*-axis voltages at the input of the rectifier and these form the control inputs. These are given by $v_d = u_d\ v_{dc}/2$ and $v_q = u_q\ v_{dc}/2$, where u_d, u_q are *d*-axis and *q*-axis averaged switching functions.

The differential equation on the *dc* side of the rectifier in can be written as [28]

$$C\frac{dv_{dc}}{dt} = i_{dc} - i_{Rdc} \tag{2.9}$$

with $i_{dc} = \dfrac{3\cdot(u_d \cdot i_d + u_q \cdot i_q)}{4}$ and $i_{Rdc} = \dfrac{v_{dc}}{R_{dc}}$.

By multiplying both sides of (2.9) with v_{dc} and applying $v_d = u_d\ v_{dc}/2$ and $v_q = u_q\ v_{dc}/2$, the power balance equation between *dc* side and the terminal of the converter can be written as given below.

$$p_{dc} = Cv_{dc}\frac{dv_{dc}}{dt} + v_{dc}i_{Rdc} = \frac{3}{2}(v_d i_d + v_q i_q) = p_T \tag{2.10}$$

Here, p_{dc} is the instantaneous power consumed on the *dc*-side, and p_T is the instantaneous power consumed at the input terminals of the converter. As shown in Fig. 2.1, $p_T = p_{in} - p_L - p_R$ where p_{in} is instantaneous power provided by the *ac* supply, p_L and p_R are the instantaneous power absorbed / delivered by the inductors and the resistors. We assume lossless, ideal operation of the rectifier here. Taking v_{dc} and i_q

as output variables, the system represented by (2.8) and (2.9) is of non-minimum phase as the resultant internal dynamics is unstable as presented in appendix A. The non-minimum phase feature appears as right half plane (RHP) zeros in a linear system. This is investigated in Chapter 3.

In [27], the differential equation on the *dc* side of the rectifier has been written as follows

$$C\frac{dv_{dc}}{dt}=\frac{3}{2v_{dc}}(e_d i_d+e_q i_q)-i_{Rdc}. \tag{2.11}$$

Once again by multiplying both sides with $v_{dc,}$ the power balance equation can be written as given below [19].

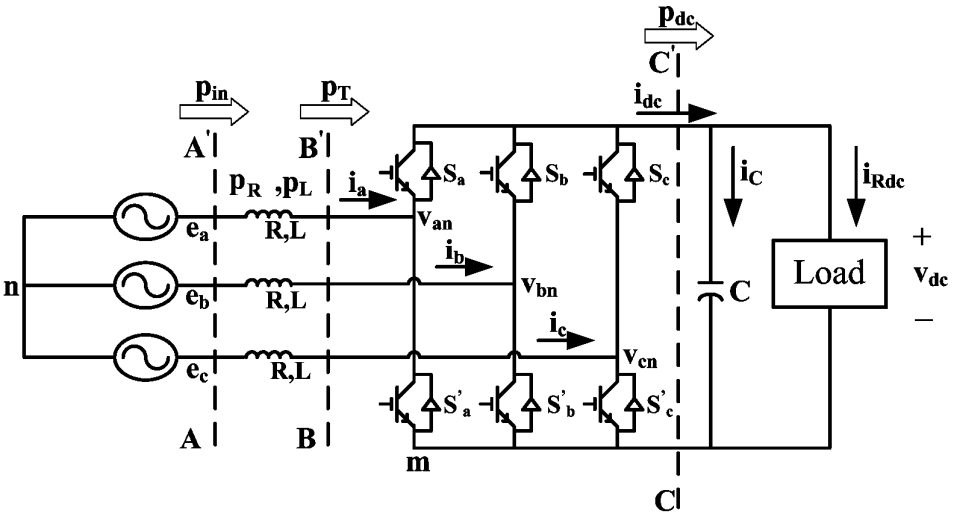


Fig. 2.1 Structure of a three phase *ac* to *dc* PWM rectifier

$$p_{dc}=\frac{1}{2}C\frac{dv_{dc}^2}{dt}+\frac{v_{dc}^2}{R_{dc}}=\frac{3}{2}(e_d i_d+e_q i_q)=p_{in} \tag{2.12}$$

As can be seen from the power balance equations, the model represented by (2.8) and (2.10) is more accurate than the modified one represented by (2.8) and

(2.12). In the latter model, the energy stored in the inductors and power consumed by the parasitic resistors have been ignored.

However, combining the power equation in (2.12) and the voltage equations in (2.8) results in a MIMO linear system as shown in (2.13) below [19].

$$\begin{bmatrix} \frac{dv_{dc}^2}{dt} \\ \frac{di_d}{dt} \\ \frac{di_q}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{2}{R_{dc}C} & \frac{3e_d}{C} & 0 \\ 0 & -\frac{R}{L} & \omega \\ 0 & -\omega & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} v_{dc}^2 \\ i_d \\ i_q \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ -\frac{1}{L} & 0 \\ 0 & -\frac{1}{L} \end{bmatrix} \begin{bmatrix} v_d - e_d \\ v_q \end{bmatrix}, \tag{2.13}$$

assuming $e_q = 0$.

Besides the system becoming linearized, the non-minimum phase feature of the rectifier also disappears in (2.13) because of the absence of the right half plane (RHP) zero from the resultant system transfer function.

TABLE 2.1 MODELS OF A PWM RECTIFIER SYSTEM

Type	Description	Equations
Model A	Model in *a-b-c* natural frame	(2.1) and (2.5)
Model B	Model in *α-β* stationary frame	(2.6) and (2.7)
Model C	Model in *d-q* synchronously rotating frame with non-minimum phase property	(2.8)and (2.9) / (2.10)
Model D	Model in d-q synchronously rotating frame ignoring non-minimum phase property	(2.8) and (2.11) / (2.12)
Model E	MIMO linear model in d-q synchronously rotating frame ignoring non-minimum phase property	(2.13)

The models for the PWM rectifier system enumerated so far are summarized in Table 2.1. For the sake of convenient citation, names such as Model A, Model B etc are assigned for each model. By ignoring the energy stored in the inductors, Models

D and E have ignored the non-minimum phase property of the system.

2.2 PWM rectifier systems operating under balanced supply voltage conditions – a literature survey

Over the past few decades, there have been extensive studies on the control schemes for PWM rectifier systems operating under balanced supply voltage conditions. These schemes mainly focus on how to fully bring forth the excellent characteristics expected of a PWM rectifier system, namely, sinusoidal line current at unity power factor (or at any arbitrary power factor) with low total harmonic distortion (THD) and constant *dc* output voltage. Depending on the controller's nature and aim, the control schemes in the literature can be roughly classified into three broad categories as shown in Table 2.2. The models for the PWM rectifier employed in these controllers have been discussed and summarized in Section 2.1.

TABLE 2.2 CLASSIFICATION OF CONTROL SCHEMES FOR OPERATION UNDER BALANCED SUPPLY CONDITIONS

Linear controllers	Non-linear controllers	Sensorless control strategies
[12~22]	[23~31]	[32~34]

2.2.1 Linear controllers

Although the state-space-averaged model of a PWM rectifier has a non-linear MIMO structure, many linear controllers have been developed for these systems. The linear controllers can be divided according to the frame in which they are implemented, namely, controllers implemented in the *a-b-c* frame and controllers implemented in the synchronous rotating frame (SRF) frame.

2.2.1.1 Controllers implemented in the *a-b-c* frame

An indirect current control scheme proposed in [12] and a control scheme aimed at minimizing harmonic distortion and obtaining unity power factor operation proposed in [13] have been generalized as a phase and amplitude control (PAC) method and have been analyzed in [14]. These control schemes determine the required control effort/ control input according to circuit equations given by Model *A* in Section 2.1. For instance, the current effort / current input is obtained by solving circuit equations based on Kirchhoff's voltage law with the assumption of a given operating power factor and *dc* output voltage reference. The phase and amplitude of the *ac* side current are thus indirectly controlled as a result of the prescribed control law.

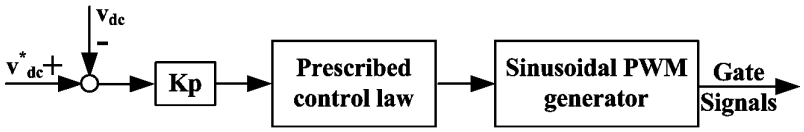


Fig.2.2 Schematic diagram for indirect current control or phase and amplitude control

The control scheme has a simple structure and provides a good switching pattern resulting in a reduction in the steady-state input current harmonics and also the output *dc* voltage ripple [14]. In addition, in the control schemes in [12] and [13], only a *dc* output voltage controller is employed whose output determines the requisite current amplitude input for the control law as shown in Fig. 2.2. Thus, current sensing and current feedback loop are avoided reducing component count and lowering cost. However, the control law used in the indirect current control is

heavily dependant on the circuit parameters, and hence will be affected by parameter variations. The control law is also dependent on the operating conditions, such as the load, and the performance is affected as the operating condition changes. In addition, with the phase and amplitude control, a *dc* current offset is present on the *ac* side of the converter during transients deteriorating the stability of the PWM rectifier system [15, 16].

A predicted-current control scheme with fixed switching frequency has been proposed in [15] and analyzed in [16]. The controller consisting of separate voltage regulation and current compensation loops for each phase can provide fast dynamic response with a good switching pattern and low system complexity. State feedback controller [17] has also been proposed to compensate for the current offset or *dc* current component on the *ac* side and reduce oscillations of the *dc* current during transients. However, since their control laws are dependent on circuit and system parameters, both these schemes are also sensitive to parameter variations and operating condition changes as is the case with phase and amplitude control [12, 13].

2.2.1.2 Controllers implemented in the SRF

It is well-known that all the time-variant variables associated with a three-phase PWM rectifier become constant *dc* quantities in SRF (see Models C, D & E in Section 2.1) in a balanced system. Therefore, modeling and control of a PWM rectifier in the *SRF* is very popular. The control tasks in a PWM rectifier system are simplified from tracking requirements into regulation requirements, thanks to the

coordinate transformation.

A. W. Green et al. [18] attempted to control the *d*-axis and *q*-axis dynamics separately based on the Model E outlined in Section 2.1. In their scheme, the *q*-axis current was regulated with only a feed-forward decoupling controller whereas the *dc* output voltage was regulated with a lag-lead compensator. Yang Ye *et al.* [19] applied a state feedback control to the system so that poles were arbitrary placed in the closed-loop system using the MIMO linear Model E of Section 2.1. However, as explained in Section 2.1, this model ignores the energy stored in the inductors resulting in the disappearance of the non-minimum phase feature and also the non-linear property in both cases. Although the non-minimum phase feature is absent in the models proposed in [18] and [19], it does exist in the real boost-type PWM rectifier. The existence of this non-minimum phase feature can be expected to impose a strict limit on the achievable closed loop performance of the real system. The simplified models are valid only if the closed-loop system has been designed to be within this limit.

Model C described in Section 2.1 is an accurate model which retains the non-linear MIMO structure and non-minimum phase feature of the real system. However, as this complex model does not give much insight into the design of controllers for a PWM rectifier system, linearized models have been developed so that linear control can be applied. An optimal linear quadratic regulator with integral action (LQI regulator) [21] and a pole placement controller [20] have been applied to a PWM

rectifier system based on such linearized models. The fact that such linear control techniques have been well developed in control theory facilitates effective analysis and design of such controllers. However, controllers designed by applying linear control theory to the linearized systems at a given operating point guarantee system stability against only small perturbations from the operating point of both states and input variables. In addition, the resulting linearized system is still a MIMO system with coupled *d*-axis and *q*-axis dynamics. Besides, after linearization, the accuracy of the resulting model remains to be evaluated.

Since all the time-variant variables associated with a three-phase PWM rectifier become constant *dc* quantities in the synchronously rotating frame (*SRF*) in a balanced system, proportional-integral (*PI*) regulators with a cascaded structure in the SRF as shown in Fig. 2.3, namely, an outer voltage loop regulator with inner *d*-axis and *q*-axis current regulators can provide zero steady-state error regulation for both currents and *dc* output voltage by providing infinite gain at zero frequency [22]. The control scheme is simple and robust to parameter variations, which makes it very popular in controlling the PWM rectifier system. However, here [22] also the transfer functions used for controller design do not include the non-minimum phase feature inherent in a PWM rectifier system. In addition, the overall stability of the system has yet to be discussed in [22].

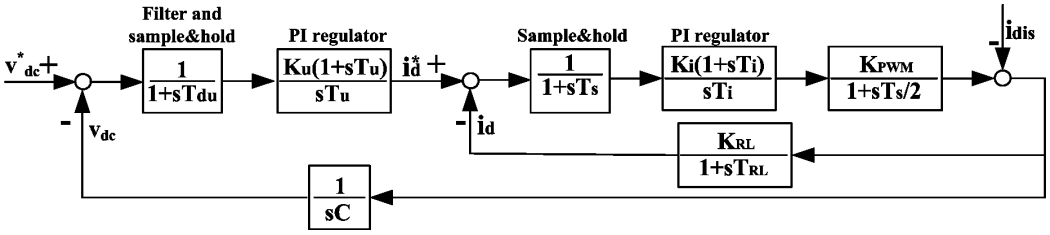


Fig. 2.3 Schematic diagram for a PWM rectifier system with a cascaded structure using *PI* controllers

2.2.2 Non-linear controllers

As a PWM rectifier has a non-linear MIMO structure and exhibits a non-minimum phase feature, many non-linear control techniques have been applied with the aim of achieving high performances both on the input side and on the output side. Some of these controllers have clearly separate current compensation loop and voltage regulation loop and have been classified below as multi-loop control schemes whereas others which control the system as a whole have been classified as system level control schemes.

2.2.2.1 Multi-loop control schemes

A hystersis current control (HCC) scheme based on a non-linear feedback loop with a two-level hystersis compensator has been employed in [23] in a PWM rectifier system. Such an HCC based system has been widely used in the current loop to control the input current of power converters, as it has merits of simplicity, high robustness and good accuracy [28]. However, the major problem of HCC is that its average switching frequency varies with operating point causing excessive stress on switching devices when the load is heavy. In addition, the variable switching frequency generally complicates switching noise filter design. Ways to coordinate

the phase current controllers so as to result in a performance close to a PWM controller have been proposed in literature [101]. However, this needs further investigation.

Sliding mode controller (SMC) is one of the most popular non-linear controllers. The SMC is well known for its insensitivity to parameter variations and system disturbances. Sliding mode control based on a two time-scale approach has been developed in [24] for a three-phase PWM rectifier. The *dc* output voltage was indirectly regulated with the *d*-axis and *q*-axis current references being calculated based on *dc* voltage reference and the system parameters. Once the *d*-axis and *q*-axis currents reach their sliding surfaces in SMC, the *dc* output voltage will settle at its desired value. The scheme was implemented in SRF which would make the state and control variables *dc* quantities under steady-state. However, as confirmed in [24] through simulation results, the system does not guarantee zero steady-sate error due to the open-loop control of the *dc* output voltage.

The integral variable structure controller (IVSC) is an alternative tracking scheme for PWM rectifier systems as it has been successfully applied in many applications such as motion control [79], UPS systems [80] and robot [83]. The integral variable structure controller consists of an integral controller for achieving a zero steady-state error under transient and a variable structure control (VSC) for enhancing the robustness [80]. Therefore, IVSC has twin merits of zero steady-state error and robustness to parameter variations and system disturbances. In the present

research, IVSC based current control has been investigated in α-β stationary frame.

As all the variables in the *a*-*b*-*c* and α-β frames are periodic, a learning controller such the repetitive controller (RC) or the iterative learning control (ILC) can be considered a good choice for the current control of PWM rectifiers.

Ref [25] applies repetitive control theory to the case of a three phase PWM rectifier. The basic concept of repetitive control theory originates from the internal model principle. According to this, zero tracking of any reference input in steady-state can be accomplished if a generator of the reference input is included in a stable closed-loop system. A digital repetitive control scheme is shown in Fig. 2.4. The error between current reference and actual current is modified using a plug-in repetitive controller as shown in Fig. 2.4. By doing so, zero steady-state error can be achieved.

Besides the cascaded structure, shown in Fig. 2.4 with solid line, a parallel structure, where the repetitive controller or the iterative learning controller is in parallel with the feedback controller, shown with dashed line in Fig. 2.4, have also been widely recommended for use in controlling UPS systems [35-39, 91], motion control systems [88-89] and robots [40-41, 85-87]. The learning control based hybrid controller capitalizes on the advantages of both the conventional feedback controller and the plug-in learning controller: the fast dynamic response offered by the feedback controller and the high precision tracking ability provided by the learning controller.

In the present research, iterative learning control based hybrid control has been explored to achieve high performance current control in the α-β stationary frame during both steady-state and transient operations.

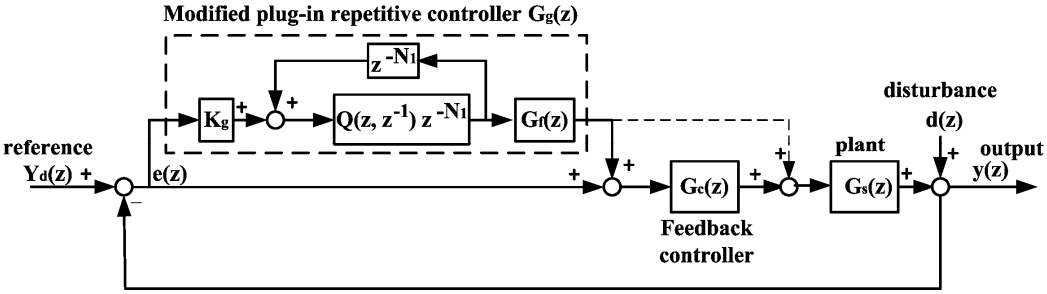


Fig.2.4 "Plug-in" repetitive control system

2.2.2.2 System level control schemes

The control of a PWM rectifier is a challenging task because besides having MIMO non-linear structure, the rectifier also exhibits a non-minimum phase feature. Appendix A shows a detailed analytical and qualitative discussion of the non-minimum phase feature of the rectifier model based on [26]. It is worth noting that the non-minimum phase feature in a linear system refers to the system having right half plane zeros whereas it has been generalized to nonlinear systems by identifying the stability of the zero dynamics [31]. The presence of non-minimum phase feature imposes a strict constraint on the achievable closed-loop performance. It also considerably complicates the task of designing a controller since many effective non-linear techniques involving model inversion, such as feedback linearization and input-output linearization, can not be directly used in systems with a non-minimum phase variable.

Lee T.S. shows in [26] that direct control of the *dc* output voltage by means of input-output linearization is not possible as the *dc* output voltage is a non-minimum phase output variable. If carried out, the resultant internal dynamics of the *d*-axis current will be unstable. On the other hand, by selecting the *d*-axis and the *q*-axis currents as dummy output variables, input-output linearization can be applied and a first-order stable zero dynamics system can be obtained for the *dc* output voltage. Regulation of the *dc* output voltage can be achieved indirectly once the *d*-axis current is well-controlled.

In apparent contrast, direct control of the *dc* output voltage has been realized by means of input-output feedback linearization in [27], by using the simplified rectifier model, Model D, described in Section 2.1. It may appear that the prediction in [26] and the approach in [27] contradict each other. However, it is worth noting that the non-minimum phase feature inherent in a three-phase boost-type PWM rectifier is not reflected in the simplified model in [27]. It will be shown in Chapter 3 that design ignoring RHP zero is possible provided the switching frequency is low such that the RHP zero is at or beyond the Nyquist frequency or if the closed loop system bandwidth is deliberately or otherwise designed to be low.

Lyapunov's direct method has been proposed to guarantee a sufficient stable region in the state space for the system against large-signal disturbances [28]. On the basis of the Lyapunov stability theory, the Lyapunov function is defined such that it is positive definite and its derivative is negative definite. The errors between the

controlled variables and their equilibrium values are used as new variables to construct the positive definite Lyapunov function. The system will settle down to equilibrium point eventually when the errors approach zero. Therefore, the control objective can be achieved directly by suitably selecting the switching functions to satisfy the stability conditions of Lyapunov's direct method. Although the system has good dynamic response, being based on Lyapunov's method, a steady-state error exists under a larger load variation as discussed in [31]. This may be attributed to the fact that the values of the equilibrium points at steady state, which depend on circuit parameters and load resistance, are required during controller realization.

Passivity is a fundamental property of electrical circuits. A passive system is a system that can not store more energy than is supplied to it. The passivity-based controller design methodology involves the shaping of the closed-loop energy function to a desired energy function. A hybrid passivity based control has been proposed for a PWM rectifier in [29] with the aim of determining the switching sequences to drive the *dc* output voltage to its desired value while maintaining all the internal signals bounded.

An obvious way to ensure good small-signal transient performance at any operating point is to tune the proportional and integral gains of the *PI* controller to their optimum values as the operating point changes [42]. 'Extended linearization' provides an analytical and systematic way for the design of such a gain scheduling scheme. Ref [31] presents an extended linearizing controller for a three-phase PWM

rectifier. The experimental results obtained with the extended linearization method have been compared with results obtained using a Lyapunov based method [28] suggesting that a faster tracking response can be obtained with the former scheme. However, as indicated in [31], systems with both the Lyapunov controller [28] and the gain scheduled controller [31] suffer from steady-state errors due to sensitivity to parameter variations and parasitic uncertainties.

As mentioned in Section 1.1, the presence of the non-minimum phase feature in the non-linear MIMO model complicates the control design for a PWM rectifier. This suggests the need to develop a simple but more informative model which can accurately predict both large signal and small signal performance and which can simplify the controller design and give clear physical insight into the behavior of a PWM rectifier system.

2.2.3 Sensorless control strategy

For proper control of a PWM rectifier, three sets of sensors are necessary, namely, *dc* output voltage sensor, line current sensors and supply voltage sensors, for the construction of the voltage and current loop controllers. In order to reduce the cost of a PWM rectifier system, a few sensorless control schemes have been proposed [32]-[34]. These schemes aim to maintain the desired attributes of a PWM rectifier without supply voltage sensors or line current sensors. The schemes can be classified as supply voltages sensorless schemes and line currents sensorless schemes.

2.2.3.1 Supply voltages sensorless schemes

It may be viewed that *dc* output voltage and line current signals are anyway needed for implementing over-voltage protection and over-current protection. On the other hand, sensing of *ac* voltages is not needed for any protection purposes. Hence it is desirable to develop schemes without the need for supply voltage sensors thereby simplifying the implementation.

Direct power control (DPC) of a PWM converter without *ac* power source voltage sensors has been proposed in [32] and its schematic is illustrated in Fig. 2.5. In the scheme, the active and reactive powers drawn from the *ac* mains are estimated using the measured *dc* output voltage, three-phase currents and the generated switching states. The optimum switching states for the converter are appropriately selected from a switching table based on instantaneous errors between the estimated active and reactive powers and the reference values. As a result, the power errors can be restricted within a set of chosen hystersis bands.

The method has the merit of simplicity with no separate PWM voltage modulation block, no current regulation loops and also no coordinate transformation required. However, high values of the inductances and sampling frequency are needed in the scheme in order to obtain accurate estimation of the power values. In addition, a large error will occur when estimation is calculated at the moment of switching action due to the dependence of the power estimation on the switching state as given in [32].

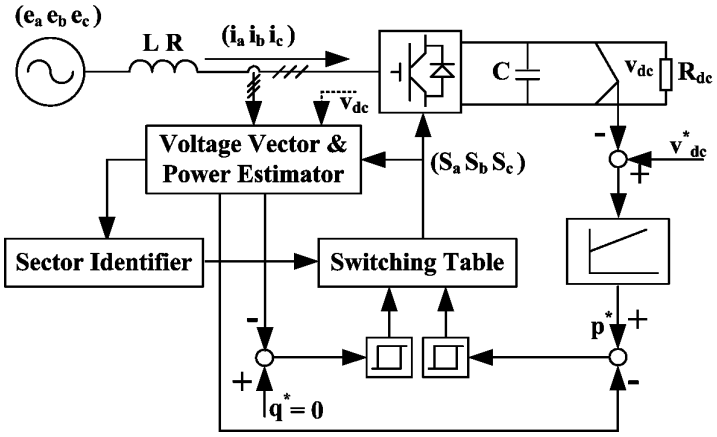


Fig. 2.5 Configuration of direct power control of PWM rectifiers

To reduce the requisite sampling frequency, a virtual-flux based direct power control (VF-DPC) scheme with a simple and noise-resistant power estimation algorithm has been proposed in [33]. In this scheme, the active power and reactive power were estimated with a virtual line flux vector and measured line currents. The VF-DPC scheme is claimed to overcome the disadvantages of the DPC scheme while retaining all the merits of the DPC method.

2.2.3.2 Line currents sensorless scheme

Using available information of the switching states in one switching period, it is possible to reconstruct the three-phase *ac* current from the *dc* output current [34] provided that two active vectors are present for at least enough time to be sampled in one switching period. However, when the modulation index is low, the on-time of the active vectors may not be long enough to obtain a reliable value of the *dc* output current.

Two line-currents sensorless schemes, based on adjusting the duty cycles within

one switching period without changing the average voltage, and predictive state observer has been proposed in [34] to solve the problems due to unreliable *dc* output current with low modulation index. Although line currents can be estimated with the proposed schemes reducing cost and complexity of the setup, the line current sensors are preferable for over-current protection especially during transients during which the current estimator based system protection may not function properly.

2.2.4 Summary

Figure 2.6 indicates the classification scheme adopted for PWM rectifiers operating under balanced supply conditions and summarizes the various control schemes discussed so far.

Based on the literature survey on rectifier operation under balanced supply conditions in Section 2.2, and the importance of the various unresolved issues, the following topics were taken up for further research:

- ***Development of a simple but accurate model for a PWM rectifier system***

As discussed in the literature survey in linear and non-linear controller sections, the fact that the PWM rectifier model has a MIMO non-linear structure with non-minimum phase feature complicates non-linear controllers design whereas the fact that linear or linearized model may not accurately reflect the complete behavior of a PWM rectifier limits the stable operating range of a PWM rectifier. Therefore, the need to develop a simple but accurate model capable of predicting both small signal and large signal performances is one of the main aims of this work.

- ***Development of an integral variable structure control based current control***

Based on literature survey, it was found that the integral variable structure control has merits of both the zero steady-state error offered by traditional integral control and the robustness offered by variable structure control (VSC). Thus, IVSC based current control was investigated in the present work.

- ***Development of an iterative learning based hybrid current control***

It was found that the learning control based hybrid controller has merits of both the fast dynamic response offered by conventional feedback controller and the high precision tracking ability provided by the learning controller. Thus, iterative learning control based hybrid control was explored in the present work.

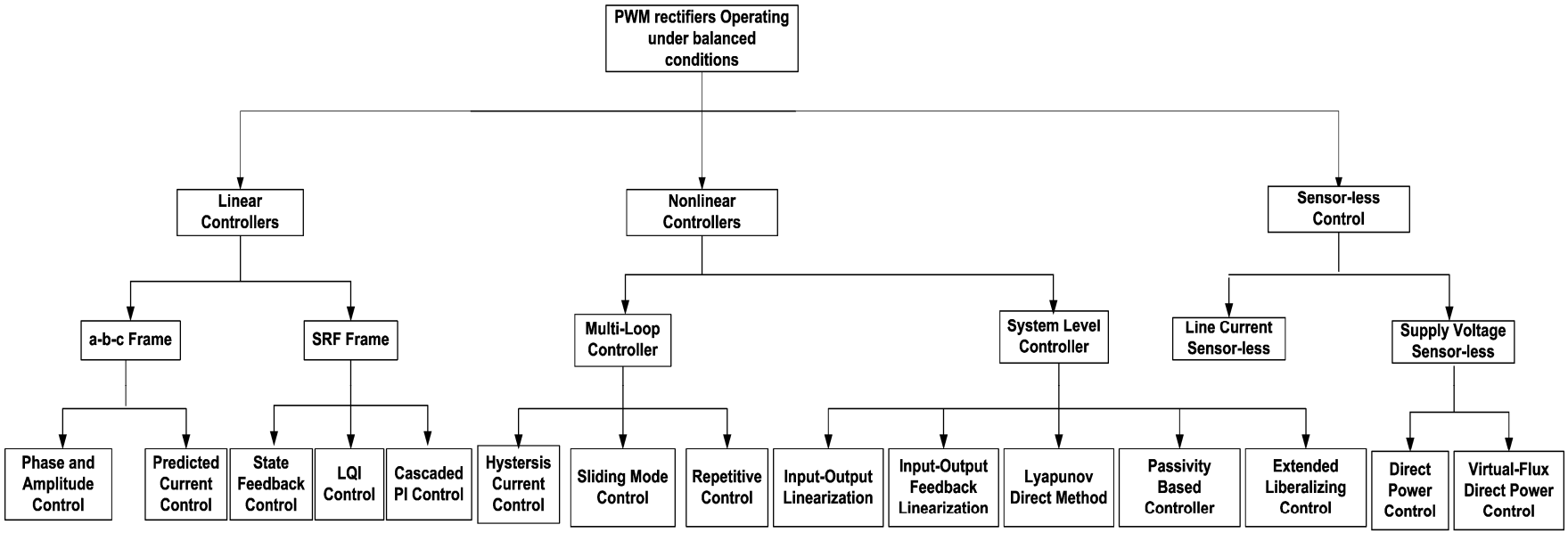


Fig. 2.6 Classification of control schemes for a PWM rectifier operating under balanced supply voltage conditions

2.3 PWM rectifiers operating under unbalanced supply voltage conditions– a literature survey

As mentioned in Chapter 1, PWM rectifiers are sensitive to a supply voltage imbalance. With the appearance of the supply voltage imbalance, the excellent features of PWM rectifiers can not fully achieved.

Extensive research work [8, 11, 43-59] has been carried out on appropriately compensating the effect of supply voltage imbalance on a PWM rectifier. Much attention has been focused on how to obtain proper current commands so as to maintain the high performance both on the input side and on the output side as is the case in a balanced system.

Among the several schemes investigated, some have been generalized directly from control schemes for the balanced PWM rectifier system by making the currents in phase with either the supply voltages [43, 57] or the positive sequence supply voltages [44, 57]. As the resulting current commands have direct relationships to the supply voltages, these methods may be called "voltage-oriented control (VOC) methods".

When the current commands are aligned to positive sequence voltages, second harmonic components will occur in both the *dc* output voltage and the *dc* output power in an unbalanced system. The presence of second harmonics on the dc output voltage will reduce life span of dc link capacitor and affect control performance of the dc load. Some control schemes aim to eliminate such second harmonic ripple in the *dc*

output voltage by adding additional switch functions [45] or injecting compensation currents [46] and these may be called "ripple-oriented control (ROC) methods".

An alternative to eliminating the *dc* power ripple which would otherwise be produced is to directly generate the current commands so as to maintain constant instantaneous active power and zero reactive power thereby achieving constant *dc* output voltage and high power factor operation [47]-[53]. As current commands are obtained by solving a set of power condition equations, these control schemes may be called as "power-oriented control (POC) methods".

Table 2.3 summarizes the classification of the schemes under unbalanced supply conditions.

TABLE 2.3 CLASSIFICATION OF CONTROL SCHEMES FOR PWM RECTIFIER SYSTEMS UNDER UNBALANCED SUPPLY VOLTAGE CONDITIONS

VOC method	ROC method	POC method
[43~44, 57]	[45~46]	[47~53]

2.3.1 Voltage-oriented control methods

One of the control objectives of a PWM rectifier fed by a balanced supply system is for the line current to be in phase with the corresponding supply voltage so that unity power factor operation can be achieved. However, such a control objective will not result in good performance under unbalanced supply voltage conditions. With an unbalanced supply, when current is in phase with its corresponding voltage [43, 57], a second harmonic power ripple will be present in the input power as given by the following power balance equation:

$$p = \overline{p} + \tilde{p} = v^p i^p + v^n i^n + v^p i^n \cos(2\omega t + \theta_v^p + \theta_v^n) + v^n i^p \cos(2\omega t + \theta_v^n + \theta_v^p) \qquad (2.14)$$

Here, p is the instantaneous active power, $\overline{p}$ is the constant portion of p and $\tilde{p}$ is the ac portion of p. The variables v^p and v^n are the amplitudes of the positive and negative sequence supply voltages, i^p and i^n are the amplitudes of the positive and negative sequence line currents and θ_v^p, θ_v^n and θ_i^p, θ_i^n are their corresponding angles.

Eq. (2.14) can be obtained from (E.18) in Appendix *E* by making the current angles equal to the voltage angles. With this control approach, the line currents are unbalanced but sinusoidal. Hence, with the scheme in [43, 57], large active power oscillation will occur on the *dc* side.

When the line current is aligned to its positive sequence supply voltage [44], a second harmonic power ripple will still be present as determined by the following:

$$p = \overline{p} + \tilde{p} = v^p i^p - v^n i^p \cos(2\omega t + \theta_v^n - \theta_v^p) \qquad (2.15)$$

Eq. (2.15) can be obtained from (E.18) in Appendix E by making the positive sequence current angle equal to the corresponding voltage angle and by making the negative sequence current magnitude equal zero. With this control approach, the line currents are theoretically balanced and sinusoidal. In addition, as mentioned in [57] the power ripple on the *dc* side is reduced compared to the earlier approach in [43].

As may be noted, these methods which are directly generalized from control schemes for the balanced system cannot provide satisfactory regulation of the *dc* output voltage when the supply is unbalanced. Considerable power ripple exists in the

system leading to second harmonic on the *dc* side output voltage.

2.3.2 Ripple-oriented control method

An analytical algorithm to selectively cancel the generated second harmonic component in the *dc* output voltage under unbalanced supply voltage conditions has been proposed in [45]. It was found that the presence of the second harmonic component in the *dc* output voltage under unbalanced operating condition with only a balanced switching function is due to the product term formed by the negative sequence voltage component and the positive sequence switching function. Therefore, selective cancellation of the second harmonic component can be achieved by suitably making the converter switch functions unbalanced. This is done by keeping the positive sequence switching function in phase with the positive sequence voltage and the negative sequence switching function out of phase with the negative sequence voltage. Furthermore, the ratio of the positive sequence switching function to the negative sequence switching function is made equal to that of the positive sequence voltage to the negative sequence voltage. The algorithm can also be formulated as follows:

$$\alpha + \beta = \lambda + \theta \qquad \text{and} \qquad A_{mn} = -\frac{A_{mp} v^n}{v^p} \tag{2.16}$$

Here, A_{mp} and A_{mn} are amplitudes of the positive and negative sequence switching functions and α and λ are their corresponding phase angles as given in [45]. Variables v^p, and v^n are the amplitudes of the positive and negative sequence supply voltages and θ and β are their corresponding phase angles.

As an extension of the analysis in [45], it was established that selective cancellation of the second harmonic component of the instantaneous power can also be obtained by suitably "counter unbalancing" the line currents [46]. Thus, current commands were formed not only by positive sequence current commands but also by negative sequence current commands calculated based on the instantaneous ripple power as shown in Fig. 2.7. By injecting the negative sequence currents to the system, both input and output performance can be improved to some extent. However, it has been acknowledged in [46] that some unwanted high order harmonics are also generated which introduces harmonics into the *ac* system.

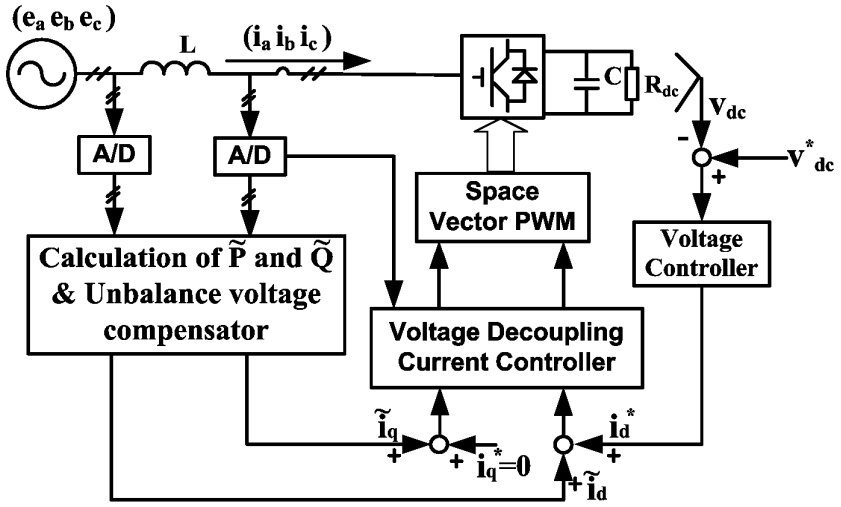


Fig. 2.7 Implementation of an unbalanced compensation scheme

2.3.3 Power-oriented control method

The instantaneous active and reactive powers, *p-q* method [47], have been widely used to calculate reactive current and active current components in many three-phase PWM converter applications. With the *p-q* theory, the rectifier/ inverter

line current commands can be obtained from the required active and reactive power by using the power inverse transformation as follows.

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \frac{1}{e_\alpha^2 + e_\beta^2} \begin{bmatrix} e_\alpha & -e_\beta \\ e_\beta & e_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \tag{2.17}$$

Here, i_α^* and i_β^* are the α-axis and β-axis current commands in the stationary frame, respectively and e_α and e_β are the corresponding supply voltages. Variables p and q are the instantaneous active and reactive power required by the PWM rectifier. Although the *dc* output voltage is well regulated with the current commands given in (2.17), the line currents will be distorted under unbalanced supply voltage conditions.

To overcome this, a generalized model for a PWM rectifier operating under unbalanced supply voltage conditions has been proposed by Rioual et al. [48]. The positive and negative sequence current commands needed for a constant *dc* output voltage and zero average input reactive power are then derived from the model. In this work, the input power was made constant and equal to the average power required for supplying the *dc* side load and the converter losses. Closed form solutions for the current commands were then obtained making the implementation of the control scheme easy. However, both the *d*-axis and the *q*-axis currents were controlled in the synchronously rotating frame (SRF) and according to [49], this would result in tracking errors when only proportional integral (PI) type of current controllers are used.

To overcome this problem, Song et al. [49] have proposed a *dual current control* scheme shown in Fig. 2.8 in which the positive-sequence currents are regulated by PI

controllers in the positive sequence SRF and the negative-sequence currents are regulated by PI controllers in the negative sequence SRF. Since the currents become *dc* components in the positive and negative sequence SRF*s*, accurate current regulation is obtained by using four individual feedback PI controllers. The control methods for the three-phase PWM rectifier presented in [48] and [49] may be termed as *input power control* (IPC) strategies.

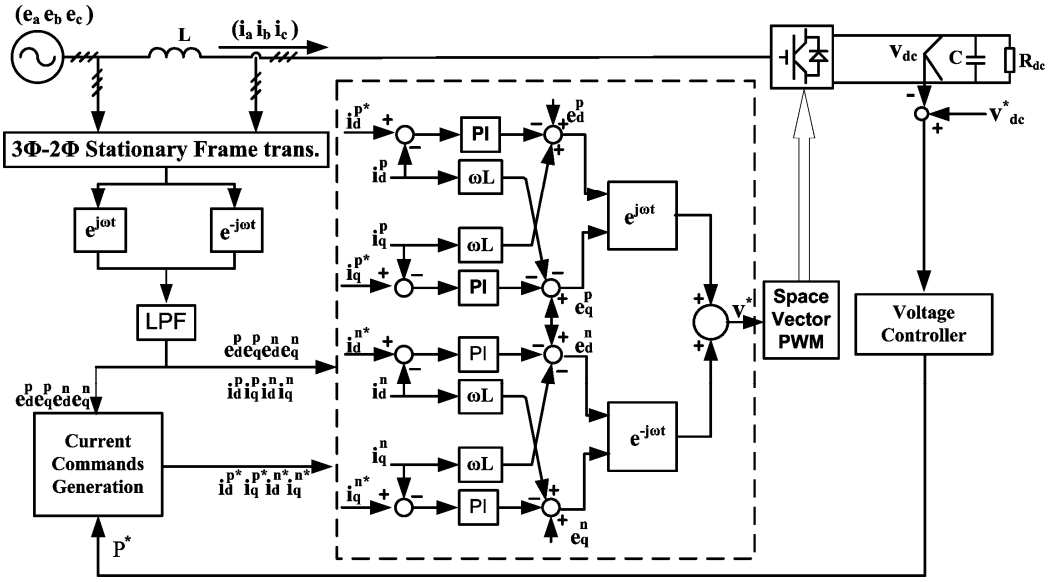


Fig.2.8 Structure of an input power control (IPC) scheme with a dual current controller

Even with a constant instantaneous input power p_{in}, the power p_{dc} on the *dc* side in [48] and [49] is not constant under unbalanced supply voltage conditions because of non-zero instantaneous power p_L in the line inductances. This oscillatory power will cause power ripple on the *dc* side thus leading to fluctuations in the *dc* output voltage. Suh et al. [51] proposed eliminating this disadvantage by nullifying the instantaneous ripple power at the rectifier bridge input terminals (BB') instead of at the supply input terminals (AA'). Furthermore, as in [48] and [49], zero average

reactive power was maintained at the supply input terminals with the aim of obtaining unity vector power factor operation. Current commands to fulfill these conditions are obtained by iteratively solving a set of highly nonlinear power equations in real time which increases the complexity of implementation. The method can, in principle, maintain nearly constant *dc* output voltage and sinusoidal line currents at unity vector power factor as desired. However, most of the simulation results in [51] indicate the existence of a steady-state error in the *dc* output voltage. The experimental results in [51] show, in addition to poor regulation, considerable ripple in the *dc* output voltage. The set of non-linear equations proposed in [51] has been solved in [52] by assuming that both the supply voltages and the rectifier bridge input voltages are known variables. However, as in [51], the experimental results provided in [52] show a steady-state error and also an observable ripple in the *dc* output voltage when operating with a 15% magnitude unbalance in one phase. The reason for this relatively poor performance in [52] is not clear. However, experimental results obtained as part of the present research based on the control scheme in [52] also indicates the poor *dc* side steady state performance.

In the method proposed in [53], zero instantaneous output ripple current is maintained in order to ensure a constant *dc* output voltage. However, the proposed control algorithm needs a great deal of computation steps for DSP control as pointed out in [51].

The control methods for the three-phase PWM rectifier presented in [51-52] may

be termed as *partial output power control* (POPC) strategies[1].

It was found that the input inductance impedance imbalance also contributes second harmonic power ripple on the *dc* side. The issue of complete harmonic elimination with adjustable power factor under extreme unbalanced operating conditions with unbalanced impedances has also been addressed in [11].

2.3.4 Summary

Fig 2.9 summarized control schemes for a PWM rectifier operating under unbalanced supply voltage conditions which has been discussed so far.

As may be seen from the discussions above, the IPC approach is simple but can only regulate the instantaneous output power roughly due to neglecting the instantaneous power handled by the inductances. On the other hand, the POPC approaches can theoretically nullify the *dc* output voltage ripple but the resulting output performance is not satisfactory according to some of the experimental results given in [52]. Therefore, one of the objectives of the present work is to nullify the instantaneous power ripple at the rectifier bridge input terminals instead of at the supply input terminals with a simple closed loop solution thereby simplifying the implementation and providing high performance on both input and output side.

On the other hand, the instantaneous power regulation scheme proposed in [52] does theoretically provide promising solutions for unbalanced voltage correction, in

[1] Please note that this method has been called "modified output control method" in out earlier publication [99]. However, we fell that the name "partial output power control method" is more accurate to reflect the content described in this scheme and hence in this thesis this latter term is used.

spite of not very good performance in the experimental results with only a slight magnitude unbalance in one phase. Therefore, one of the objectives in the future research is to identify the reasons for the mismatch between theoretical analysis and experimental realization for the partial output power control scheme and to resolve this problem, if possible.

As discussed above, considerable research work has so far been carried out to compensate for the unbalanced supply voltage with the aim of obtaining high performance on both the input and output sides of the PWM rectifier system. Therefore, another objective in this work is to evaluate these schemes under unbalanced supply conditions with appropriate performance indices.

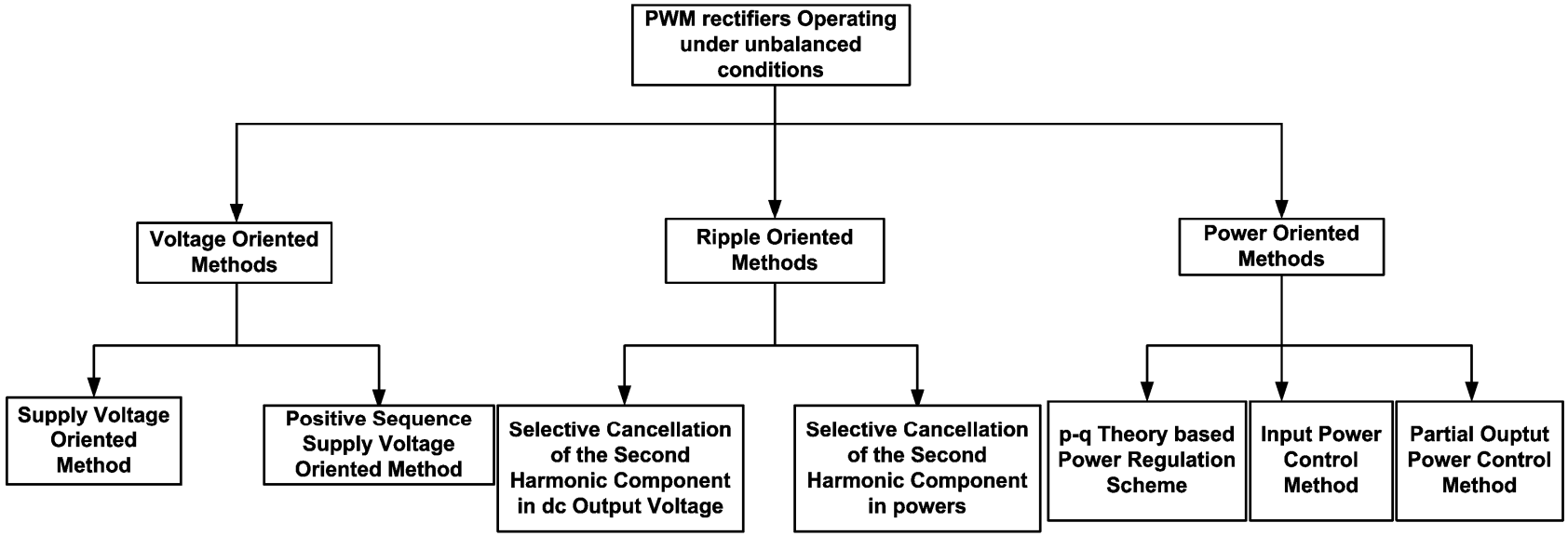


Fig. 2.9 Classification of control schemes for a PWM rectifier operating under unbalanced supply voltage conditions

2.4 Conclusions

In this chapter, a detailed literature survey on the solutions to the problems associated with a three-phase PWM rectifier operating under both balanced and unbalanced supply voltage conditions has been presented. A brief review of the models of a PWM rectifier system available in literature has also been included in Section 2.2. The problems associated with PWM rectifiers operating under balanced conditions have been outlined in Appendix A.

Based on the literature survey of rectifier operating under balanced supply conditions in Section 2.2, it may be concluded that there is a need to come up with a simpler but more informative model than the existing models thereby simplifying the controller design for a PWM rectifier system. Accordingly, Chapter 3 focuses on development of an accurate but simple model for PWM rectifiers under balanced supply conditions. The chapter also presents simple voltage-mode and current-mode controllers based on the proposed model.

Based on the literature survey in Section 2.3, it may be concluded that there is a need to come up with a power regulation scheme which can achieve high input-side and output-side performance under unbalanced supply conditions. Accordingly, Chapter 4 proposes an output power control (OPC) scheme capable of fulfilling the main objectives of a high performance PWM rectifier. In Chapter 5, the problems existing in the schemes proposed in [52] are also investigated and identified. Based on

this an improved implementation of this scheme which is capable of achieving excellent performance has been suggested. Lastly, four power regulation schemes have been evaluated and compared in terms of total harmonic distortion of line current, peak-peak *dc* output voltage ripple and effective power factor in Chapter 6.

Based on the literature survey on rectifier operation under balanced supply conditions in Section 2.2, it may also be concluded that integral variable structure control (IVSC) based current control and learning based hybrid current control may provide high performance current tracking during both steady-state and transient stages. Accordingly, Chapter 7 focuses on implementation of both IVSC based current control and an ILC based hybrid current control (Hybrid ILC). The chapter also evaluates control performances of four different current controllers, namely, dual current control (DPIC), P + Resonant current control (P+RC), integral variable structure current control (IVSC) and proposed ILC based hybrid current control (Hybrid ILC).

CHAPTER 3

THREE-PHASE BOOST-TYPE PWM RECTIFIER UNDER BALANCED SUPPLY VOLTAGE CONDITIONS

3.0 Introduction

In this Chapter, a simple single-input single-output (SISO) model for the three phase rectifier operation under balanced supply conditions and unity power factor (UPF) operation is constructed by separating the *d*-axis and the *q*-axis dynamics through appropriate non-linear feed-forward decoupling. The validity of the proposed model is first verified experimentally in the frequency domain under open-loop operation of the PWM rectifier. It is found that the proposed SISO model exhibits a close similarity to a *dc-dc* boost converter under both large-signal and small-signal operating conditions, which makes it possible to extend the system analysis and control design techniques of *dc-dc* converters to the three-phase PWM rectifier. Based on this insight, the usefulness of the model is further demonstrated through closed-loop operation of the rectifier with both voltage mode and current mode control.

3.1 Background

Several models for PWM rectifiers operating under balanced input supply conditions are available in the literature [19, 22, 26-28, 60]. As mentioned in Chapter 2, the popular state-space-averaged model [22, 26, 28] does not give sufficient insight into

controller design due to its complex multi-input multi-output (MIMO) non-linear structure and the presence of the non-minimum phase feature. The models in [19, 27] do simplify the system structure and controller design by overlooking the inherent non-minimum phase feature in a PWM rectifier. This is particularly so in [19], where the establishment of a MIMO linear model theoretically enables arbitrary pole placement in the closed-loop system. However, although the non-minimum phase feature is absent in the models proposed in [19, 27], it does exist in the real boost-type PWM rectifier. The existence of this non-minimum phase feature imposes a strict limit on the achievable closed loop bandwidth of the real system. The simplified models in [19, 27] are valid only if the closed-loop system operates within this limit. Thus, the information regarding the location of the non-minimum phase feature in the model is required for proper controller design even if the simplified models in [19, 27] are used.

A novel reduced-order (RO) small-signal model has been proposed in [60]. The three-phase PWM rectifier has been modeled here as a *dc-dc* converter with equivalent power transfer capability and small-signal characteristics. However, the second-order RO model proposed is a *one-sixth line frequency averaged model* which only captures the equivalent power transfer capability of the converter. In addition, the establishment of the RO model neither reduces the number of required current controllers nor simplifies the control task from a tracking into regulation problem. Three identical current controllers are needed for tracking purposes based on this model. Besides, the significance of the rooted non-minimum phase feature in the design of the controller is not brought out in the RO model.

The fact that the non-minimum phase feature of a PWM rectifier presents itself as a

right half plane (RHP) zero in the small-signal transfer function from current reference to *dc* output voltage in a control-oriented model has been explored in the research reported in [61-64]. In this approach [61-64], linear decoupling terms were applied to the overall PWM rectifier model in order to reduce the cross-coupling between the *d*- and *q*-axes currents. The current loops were closed with conventional P-type average current-mode controllers. Thus, the control-oriented model between the *dc* output voltage and the *d*-axis current reference can be obtained by performing a small-signal analysis. The control-to-output transfer function, $G_c = \hat{v}_{dc} / \hat{i}_d^*$, where variable $\hat{v}_{dc}$ is the perturbation of the *dc* output voltage and variable $\hat{i}_d^*$ is the perturbation of the *d*-axis current reference, is shown to contain an RHP zero and a stable pole. This transfer function has been obtained by an approximation of the *measured frequency response* in the low and mid-frequency range. The control-oriented model presented by this control-to-output transfer function facilitates voltage loop design as the model reduces to a single-input single-output system after the current loop is closed [63]. The presence of the RHP zero in both a three-phase PWM rectifier system and a *dc*-*dc* boost converter shows an apparent similarity between them. These results give important insights into the behavior of a three-phase PWM rectifier system.

However, the control transfer function developed in [61-62] links the *dc* output voltage to only the *d*-axis reference current. Furthermore, this link is established through the use of experimental frequency response characteristics and also by assuming a certain form of current controller (P-Type). More importantly, the control-oriented model does not link the output voltage to the operation of the rectifier switches as would

be expected in a detailed model of a power converter.

The present chapter builds upon the earlier work in [61-64] to obtain a simple and accurate control-oriented model for the three-phase PWM rectifier. It proposes a simple single-input single-output (SISO) model for a three-phase rectifier. In the proposed model, the MIMO system is first decoupled into two SISO systems in which the *q*-axis model is a first order linear system determining the regulation of power factor, while the *d*-axis model, which is shown to be similar to that of a traditional *dc*-*dc* boost converter, is a second-order non-linear system determining the power delivery. Thereafter, a simple SISO model can be obtained for the *d*-axis operation, when the *q*-axis current is controlled at zero or near. It was found that the proposed SISO model is similar to the model of a *dc*-*dc* boost converter under both large-signal and small-signal operations. In the small signal model, the complex non-minimum phase feature inherent in an *ac*-to-*dc* rectifier becomes a simple RHP zero appearing in the small-signal control-to-output transfer function between the *dc* output voltage and an 'equivalent' duty cycle of the system, which will be defined later.

The proposed SISO system can be operated in a "quasi open-loop" mode with output variable being the *dc* output voltage and the control input being the equivalent duty cycle. This open loop characteristic of the SISO model is examined in the frequency domain. It is found that the measured frequency response shows an excellent agreement with the predicted response. This finding validates the proposed SISO model.

The fact that the SISO model shows a close similarity to that of a traditional *dc*-*dc* boost converter makes it possible to extend the system analysis and control design of

dc-dc converters to the three-phase rectifier. By utilizing the small signal control-to-output transfer functions, both voltage mode control scheme and current mode control scheme, which are simple and well-documented techniques often used in *dc-dc* converters, are applied to a three-phase PWM rectifier in this chapter. The steady-state performance and also transient performance are all experimentally investigated. Experimental results show that the proposed controllers can provide both satisfactory steady-state performance and good transient performance thus further showing the usefulness of the proposed model. As may be expected, the inner current loop based scheme results in better overall performance.

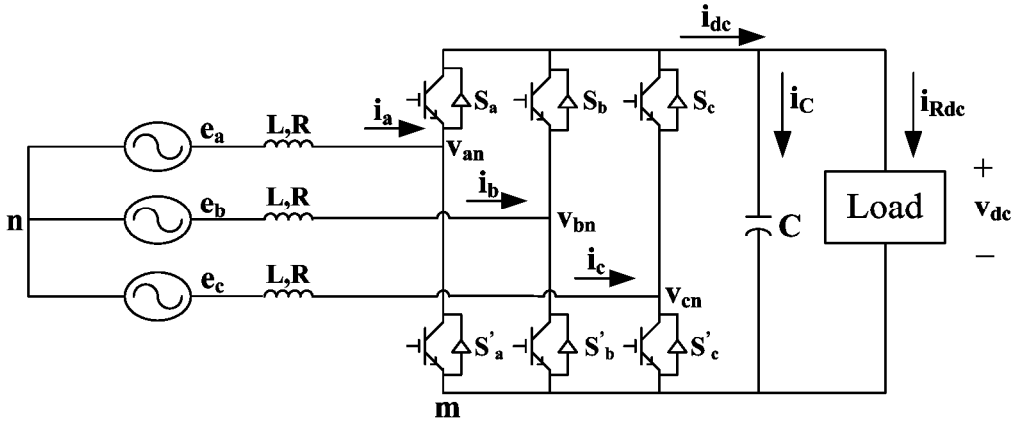


Fig. 3.1 Structure of a three-phase *ac* to *dc* PWM rectifier

3.2 A dual SISO model of a three-phase PWM rectifier

In this section, the proposed dual SISO model of the three-phase boost rectifier is derived.

3.2.1 Equivalent circuit for a three-phase PWM rectifier

The voltage-source type PWM rectifier is shown in Fig. 3.1. Here, e_a, e_b, and e_c represent the source voltages and i_a, i_b, and i_c represent the input currents. Parameters L

and R are the inductance and parasitic resistance values of the synchronous inductance. The system differential equations in d-q synchronously rotating frame (*SRF*) are given below [22, 26, 28].

$$\begin{cases} L\dfrac{di_d}{dt} + Ri_d - \omega L i_q = e_d - v_d \\ L\dfrac{di_q}{dt} + Ri_q + \omega L i_d = -v_q \end{cases} \tag{3.1}$$

$$C\frac{dv_{dc}}{dt} = \frac{3}{4}(u_d i_d + u_q i_q) - i_{Rdc} \tag{3.2}$$

Here, e_d, e_q, and i_d, i_q denote the input voltages and the input currents in the SRF and v_d, v_q are the control inputs and, in fact, denote the average voltages at the rectifier input terminals, again in the *SRF*. The variables v_d, v_q are related to the *dc* output voltage as follows.

$$\begin{cases} v_d = u_d v_{dc}/2 \\ v_q = u_q v_{dc}/2 \end{cases}, \tag{3.3}$$

where u_d, u_q are the d-axis and q-axis averaged switching functions, respectively. The range of the switching functions is between 0 and 1.

Under steady state operating conditions, variables in (3.1) and (3. 2) will be *dc* quantities.

Multiplying (3.2) by v_{dc} on both sides and applying (3.3), we can show that

$$Cv_{dc}\frac{dv_{dc}}{dt} + v_{dc}i_{dc} = \frac{3}{2}(v_d i_d + v_q i_q) \tag{3.4}$$

Equation (3.4) shows the power balance between the *dc* side and the *ac* side of the

converter. The equivalent circuit based on (3.1) and (3.4) is shown in Fig. 3.2. This is similar to the circuit model developed earlier by other researchers [65].

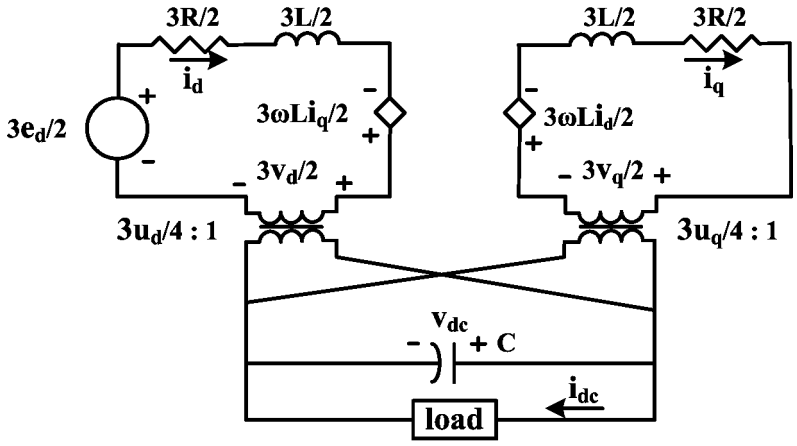


Fig. 3.2 Equivalent circuit in SRF

3.2.2 Non-linear feed-forward decoupling controller

In Fig. 3.2, the coupling terms between the *d*-axis and the *q*-axis are represented by the two current-controlled dependent-voltage sources. Decoupling may be achieved, if the effects of these two voltage sources are nullified by appropriately adjusting the control inputs v_d and v_q as given below.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} v_{d1} + v_{d2} \\ v_{q1} + v_{q2} \end{bmatrix} \tag{3.5}$$

In (3.5), v_{d1} and v_{q1} represent the feed-forward decoupling control parts with

$$\begin{bmatrix} v_{d1} \\ v_{q1} \end{bmatrix} = \begin{bmatrix} u_{d1}\dfrac{v_{dc}}{2} \\ u_{q1}\dfrac{v_{dc}}{2} \end{bmatrix} = \begin{bmatrix} \omega L i_q \\ -\omega L i_d \end{bmatrix}, \tag{3.6}$$

where u_{d1} and u_{q1} are the portions of the switching functions, u_d and u_q corresponding to

the non-linear decoupling controller with $u_{d1}=2\omega Li_q/v_{dc}$ and $u_{q1}=-2\omega Li_d/v_{dc}$.

With this decoupling control, the differential equation on the *ac* side can be rewritten as follows.

$$\begin{cases} L\dfrac{di_d}{dt}+Ri_d=e_d-v_{d2} \\ L\dfrac{di_q}{dt}+Ri_q=-v_{q2} \end{cases} \tag{3.7}$$

Decoupling control has been performed in the development of control-oriented model in earlier research [61-64] also. As mentioned earlier in Section 3.1, a control-oriented model has been developed in [63] by first introducing the decoupling terms and then implementing current loops. However, the linear decoupling terms $u_{d1}=\omega Li_q/v_{dc\_ref}$ and $u_{q1}=-\omega Li_d/v_{dc\_ref}$ used in [63] leads to decoupling the dynamics of *d*-axis and *q*-axis only when $v_{dc}= v_{dc\_ref.}$ At other operating points and under transients, these decoupling terms do not lead to the desired simplification of the system dynamics.

By substituting (3.5) and (3.6) into (3.4), the differential equation on the *dc* side can be written as follows.

$$Cv_{dc}\frac{dv_{dc}}{dt}+v_{dc}i_{dc}=\frac{3}{2}(v_{d2}i_d+v_{q2}i_q) \tag{3.8}$$

The term $v_{q2}i_q$ represents the effect of *q*-axis dynamics on the *d*-axis. However, under balanced supply voltage and unity or near unity power factor conditions, the magnitude of this term will be insignificant due to the zero average value of i_q. Thus, this term will usually be negligible and can be viewed as a small disturbance in the *d*-axis. It has been shown experimentally in Section 3.3 that the presence of a small magnitude of *q*-axis

current of either polarity has a negligible effect on the *d*-axis dynamics, thus justifying the neglecting of the term $v_{q2}i_q$ in (3.8).

Thus, (3.8) can be approximated as

$$Cv_{dc}\frac{dv_{dc}}{dt}+v_{dc}i_{dc}=\frac{3}{2}v_{d2}i_d\,, \tag{3.9}$$

with $v_{d2}=u_{d2}v_{dc}/2$. Here, u_{d2} is the system control input and is a portion of switching function u_d.

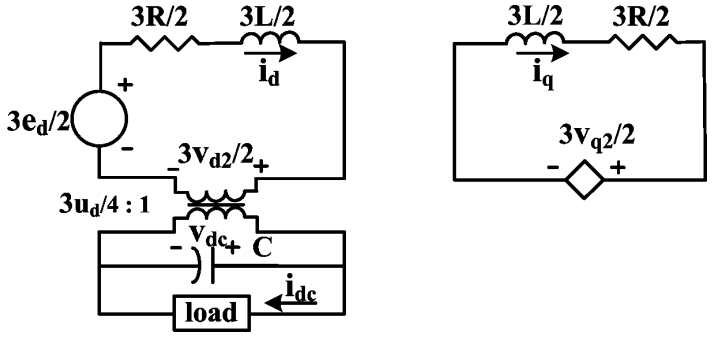


Fig. 3.3 Equivalent circuit in *SRF* after decoupling and neglecting of *q*-axis disturbance on *d*-axis dynamics

The equivalent circuit based on (3.7) and (3.9) is shown in Fig. 3.3. It can be seen that the *d*-axis and *q*-axis dynamics are totally decoupled in this model. This model which is based on neglecting the effect of the *q*-axis current on the *d*-axis dynamics is true under unity or near unity power factor conditions.

3.2.3 A simple SISO model

After the above decoupling and simplification assuming near unity power factor operation, a three-phase boost-type PWM *ac-dc* rectifier becomes a dual SISO system. From (3.7) and (3.9), the differential equations can be rewritten as:

$$\begin{cases} L\dfrac{di_d}{dt} + Ri_d = e_d - \dfrac{1}{2}u_{d2}v_{dc} \\ C\dfrac{dv_{dc}}{dt} + i_{dc} = \dfrac{3}{4}u_{d2}i_d \end{cases} \tag{3.10}$$

$$L\frac{di_q}{dt} + Ri_q = -v_{q2} \tag{3.11}$$

The *q*-axis model given in (3.11) is a first-order linear system responsible for power factor regulation, whereas the *d*-axis model is a second-order non-linear system which determines the power delivery. The *q*-axis behavior can be represented in the frequency domain by a simple first order transfer function as shown below.

$$\frac{i_q(s)}{v_{q2}(s)} = \frac{1}{Ls + R} \tag{3.12}$$

Next we will compare the averaged model obtained for a three-phase PWM rectifier with a *dc* to *dc* boost converter (Fig. 3.4 (a)). The *dc* to *dc* boost converter's state-spaced averaged equations under continuous conduction mode (CCM) of operation are given as follows.

$$\begin{cases} L\dfrac{di_d}{dt} + Ri_d = e_d - (1-d)v_{dc} \\ C\dfrac{dv_{dc}}{dt} + \dfrac{v_{dc}}{R_{dc}} = (1-d)i_d \end{cases}, \tag{3.13}$$

where *d* is the duty ratio of the boost converter.

The similarity of this model with the *d*-axis averaged model of the three-phase PWM rectifier represented by (3.10) becomes obvious if u_{d2} is replaced by (*1*-*d*) in (3.10). This suggests the *d*-axis equivalent circuit shown in Fig. 3.4(b) for the three-phase PWM

rectifier.

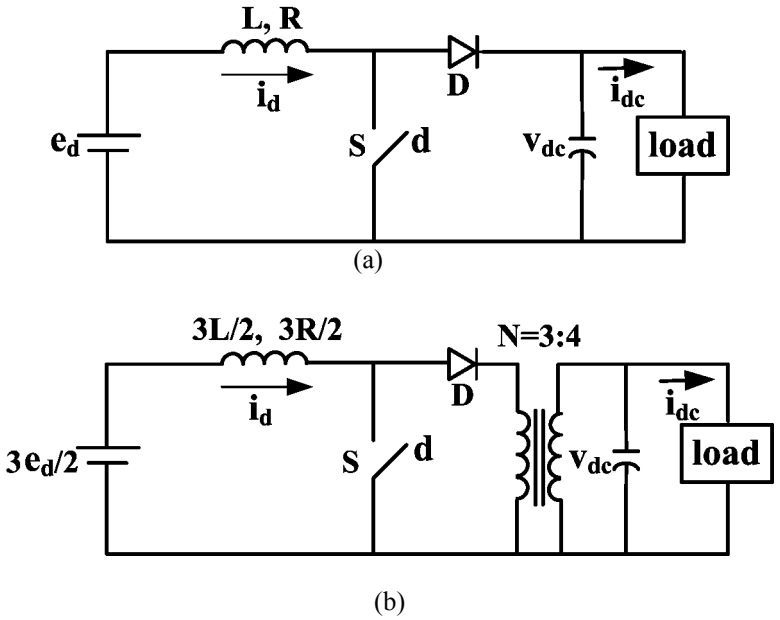


Fig. 3.4 (a) A *dc* to *dc* boost converter (b) Proposed *d*-axis equivalent circuit for the three-phase PWM rectifier

In Fig. 3.4(b), the switch *S* is assumed to operate at an 'equivalent' duty cycle *d* resulting in a switching function u_{d2}. Under steady-state operating conditions, ideally, the *dc* output voltage in the equivalent converter of Fig. 3.4 (b) will be as follows.

$$\frac{V_{dc}}{E_d} = \frac{2}{(1-D)} \tag{3.14}$$

Here *D* is the steady-state equivalent duty cycle, V_{dc} is the average output *dc* voltage and E_d is the *d*-axis supply voltage.

As in a *dc* to *dc* boost converter, the effect of circuit losses will be to reduce the gain, especially at high duty ratio values. For example, by including the inductor resistance *R*, it can be shown from Fig. 3.4(b) that

$$\frac{v_{dc}}{e_d} = \frac{2(1-D)}{(1-D)^2 + 8R/3Z_{dc}} \tag{3.15}$$

where Z_{dc} is the load impedance.

The *dc* output voltages of the equivalent converter under steady-state operating conditions with and without the inclusion of the parasitic resistance of the inductors are summarized in Table 3.1.

Note: The dc-dc boost converter shown in Fig. 3.4(b) can enter discontinuous conduction mode (DCM) also. However, such an operating mode does not exist in a three-phase PWM rectifier. Therefore, it might be more appropriate to replace both the diode D and the switch S with two bidirectional switches, each consisting of a unidirectional switch and an anti-parallel diode.

Fig. 3.5 shows an equivalent *d*-axis SISO system obtained through applying the decoupling controller and ensuring unity power factor regulation. The figure shows the implementation of 1) the de-coupling control, 2) $abc \leftrightarrow dq$ transformations that are needed and also 3) the *q*-axis current control loop to keep i_q at zero. In this manner, we can operate the three-phase rectifier in a "quasi open-loop" mode with the variable *d* (u_{d2}) being treated as the control input of the *d*-axis system and v_{dc} being the system output. As shown in Fig. 3.5, the *d*-axis current output i_d may also be treated as an output if needed, for example if a current mode control scheme is implemented.

It must be noted that the operation of the equivalent switch *S* in Fig. 3.4 (b) is only partially linked to the operation of the actual six switches of the converter. The operation of the switches of the converter is in fact determined by the complete switching functions

u_d, u_q and the employed PWM technique. The transformation of complete switching functions u_d, u_q in SRF into switching functions u_a, u_b and u_c in the *a*-*b*-*c* natural frame is defined in (2.2) of Chapter 2. The transformed switching functions u_a, u_b and u_c can be used to switch the six switches of the PWM rectifier in different ways depending on the actual PWM scheme adopted. The relationship between switching functions and duty ratio in a-b-c frame has been defined in (2.4) of Chapter 2. In this work, a standard sinusoidal PWM (SPWM) scheme has been employed.

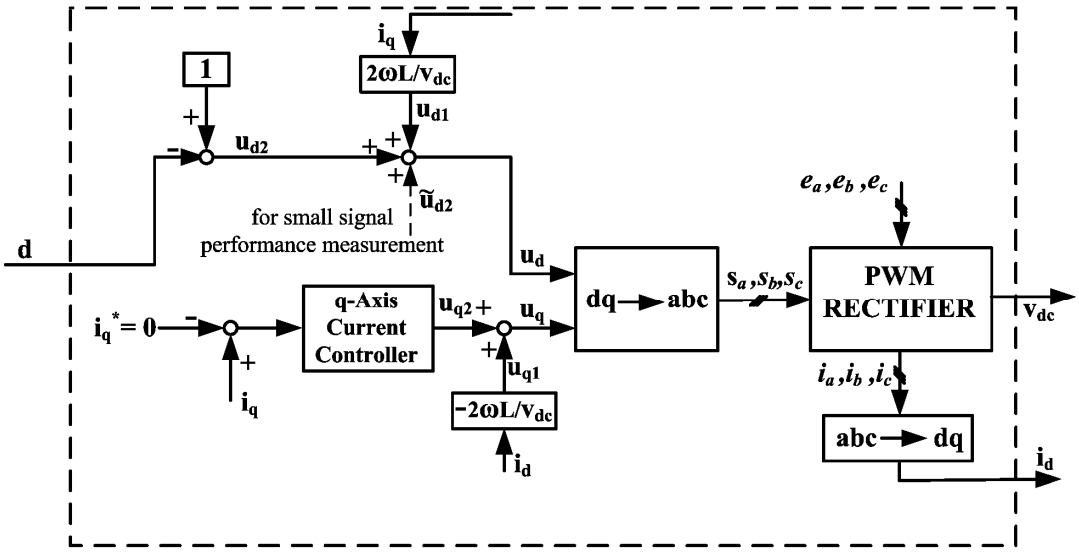


Fig. 3.5 Block diagram for realizing the equivalent *d*-axis SISO system of the PWM rectifier

It is also worth noting that the models given in Fig 3.3 and Fig. 3. 4 (a) & (b) are valid for any kind of loads. Other type of loads, such as a dc-dc buck converter operating in continuous current mode or a PWM VSI supplying a permanent magnet synchronous motor running at constant speed can also be modeled using their input impedances as given in [62]. The influence of these loads on the control transfer function can be analyzed by replacing resistance R_{dc} with the corresponding load input impedance Z_{in}. This will complicate the analysis and verification of the use of the simple *SISO* model. Since our

aim is only the verification of the proposed PWM rectifier model, a simple resistive load, R_{dc}, has been made use of in the rest of the chapter.

3.2.4 Small signal model using the state space averaging approach

The state-spaced averaged equations of the equivalent circuit shown in Fig. 3.4 (b) can be written as

$$\begin{bmatrix} \dot{v}_{dc} \\ \dot{i}_d \end{bmatrix} = \begin{bmatrix} -\dfrac{1}{R_{dc}C} & \dfrac{3}{4C}(1-d) \\ -\dfrac{(1-d)}{2L} & -\dfrac{R}{L} \end{bmatrix} \begin{bmatrix} v_{dc} \\ i_d \end{bmatrix} + \begin{bmatrix} 0 \\ \dfrac{1}{L} \end{bmatrix} e_d \,. \tag{3.16}$$

Ignoring the parasitic resistance R, the average current and output voltage can be obtained from (3.16) as

$$V_{dc} = \frac{2E_d}{1-D} \quad \text{and} \quad I_d = \frac{8E_d}{3R_{dc}(1-D)^2} \tag{3.17}$$

Perturbations are introduced in the control inputs for obtaining the small signal model. Let the perturbed variables be $v_{dc} = V_{dc} + \hat{v}_{dc}$, $i_d = I_d + \hat{i}_d$, $d = D + \hat{d}$ and $e_d = E_d + \hat{e}_d$.

Applying the perturbed variables to (3.16), removing the *dc* terms and neglecting the higher order nonlinear terms, the small-signal model can be obtained as follows.

$$\dot{\hat{x}} = A\hat{x} + f\hat{d} + b\hat{e}_d \tag{3.18}$$

where $\hat{x} = \begin{bmatrix} \hat{v}_{dc} & \hat{i}_d \end{bmatrix}^T$, $A = \begin{bmatrix} -\dfrac{1}{R_{dc}C} & \dfrac{3}{4C}(1-D) \\ -\dfrac{(1-D)}{2L} & -\dfrac{R}{L} \end{bmatrix}$, $f = \begin{bmatrix} -\dfrac{2E_d}{R_{dc}C(1-D)^2} \\ \dfrac{2E_d}{L(1-D)} \end{bmatrix}$ and

$$b = \begin{bmatrix} 0 \\ \dfrac{1}{L} \end{bmatrix}.$$

Taking Laplace Transform and again neglecting the inductor parasitic resistance R, we obtain the following expressions for the variations of the output voltage $\hat{v}_{dc}(s)$ and input current $\hat{i}_d(s)$ for perturbations in the duty cycle *d (s)*.

$$F_v(s) = \frac{\hat{v}_{dc}(s)}{\hat{d}(s)}\Big|_{\hat{e}_d=0} = [1 \quad 0](sI - A)^{-1} f = \frac{2e_d}{(1-D)^2} \frac{1 - \dfrac{8L}{3R_{dc}(1-D)^2} s}{1 + \dfrac{8L}{3R_{dc}(1-D)^2} s + \dfrac{8LC}{3(1-D)^2} s^2} \tag{3.19}$$

$$F_i(s) = \frac{\hat{i}_d(s)}{\hat{d}(s)}\Big|_{\hat{e}_d=0} = [0 \quad 1](sI - A)^{-1} f = \frac{16e_d}{3D^3 R_{dc}} \frac{1 + \dfrac{R_{dc}C}{2} s}{1 + \dfrac{8L}{3R_{dc}(1-D)^2} s + \dfrac{8LC}{3(1-D)^2} s^2} \tag{3.20}$$

The equations given in (3.19) and (3.20) are the 'quasi open-loop' transfer functions of the three-phase PWM rectifier. They have been arrived at under the assumption that the de-coupling control given in (3.6) has been implemented and also that the *q*-axis current is being regulated at zero.

The transfer functions of the equivalent converter under steady-state operating conditions are summarized in Table 3.1.

The transfer function in (3.19) is similar to that of a conventional boost *dc-dc* converter derived based on an averaged model. Like a *dc-dc* boost converter, the three-phase boost-type PWM rectifier also suffers from the problem of RHP zero in control-to-output transfer function.

TABLE 3.1 COMPARISON BETWEEN A *DC*-*DC* BOOST CONVERTER AND A THREE-PHASE *AC*-*DC* RECTIFIER

	dc-dc boost converter	Three-phase PWM rectifier (Proposed SISO model)
Equation	$\begin{cases} L\frac{di_d}{dt}+Ri_d=e_d-(1-d)v_{dc} \\ C\frac{dv_{dc}}{dt}+i_{dc}=(1-d)i_d \end{cases}$	$\begin{cases} L\frac{di_d}{dt}=-Ri_d+e_d-(1-d)\frac{v_{dc}}{2} \\ C\frac{dv_{dc}}{dt}=-i_{dc}+\frac{3}{4}(1-d)i_d \end{cases}$
Voltage Conversion Ratio	$\frac{v_{dc}}{e_d}=\frac{1}{(1-D)}$ (without parasitic elements considered) $\frac{v_{dc}}{e_d}=\frac{(1-D)}{(1-D)^2+R/Z_{dc}}$ (with inductors' parasitic resistance)	$\frac{v_{dc}}{e_d}=\frac{2}{(1-D)}$ without parasitic elements considered) $\frac{v_{dc}}{e_d}=\frac{2(1-D)}{(1-D)^2+8R/3Z_{dc}}$ (with inductors' parasitic resistance)
Small Signal Analysis	$\frac{\hat{v}_{dc}(s)}{\hat{d}(s)}=\frac{e_d}{(1-D)^2}\frac{1-\frac{L}{R_{dc}(1-D)^2}s}{1+\frac{L}{R_{dc}(1-D)^2}s+\frac{LC}{(1-D)^2}s^2}$ $\frac{\hat{i}_d(s)}{\hat{d}(s)}=\frac{2e_d}{R_{dc}(1-D)^3}\frac{1+\frac{R_{dc}C}{2}s}{1+\frac{L}{R_{dc}(1-D)^2}s+\frac{LC}{(1-D)^2}s^2}$ $\frac{\hat{v}_{dc}(s)}{\hat{i}_d(s)}=\frac{R_{dc}(1-D)}{2}\frac{1-\frac{L}{(1-D)^2R_{dc}}s}{1+\frac{R_{dc}C}{2}s}$	$\frac{\hat{v}_{dc}(s)}{\hat{d}(s)}=\frac{2e_d}{(1-D)^2}\frac{1-\frac{8L}{3R_{dc}(1-D)^2}s}{1+\frac{8L}{3R_{dc}(1-D)^2}s+\frac{8LC}{3(1-D)^2}s^2}$ $\frac{\hat{i}_d(s)}{\hat{d}(s)}=\frac{16e_d}{3R_{dc}(1-D)^3}\frac{1+\frac{R_{dc}C}{2}s}{1+\frac{8L}{3R_{dc}(1-D)^2}s+\frac{8LC}{3(1-D)^2}s^2}$ $\frac{\hat{v}_{dc}(s)}{\hat{i}_d(s)}=\frac{3R_{dc}(1-D)}{8}\frac{1-\frac{8L}{3(1-D)^2R_{dc}}s}{1+\frac{R_{dc}C}{2}s}$

By setting numerator of (3.19) zero, the corner frequency of RHP zero can be obtained below

$$f_z=\frac{3R_{dc}(1-D)^2}{16\pi L} \tag{3.21.a}$$

By substituting (3.17) into (3.12.a), (3.21.b) can be obtained. Similarly, using relationship $p_{dc}=3E_dI_d/4$ in (3.21.b), (3.21.c) can be obtained.

$$f_z=\frac{E_d}{2\pi LI_d} \tag{3.21.b}$$

$$f_z=\frac{3E_d^2}{4\pi Lp_{dc}} \tag{3.21.c}$$

This location, as in a *dc-dc* boost converter, is closest to the imaginary axis in the

complex *s*-plane under minimum supply voltage and maximum load. The achievable overall closed loop bandwidth will be limited to a frequency much less than the frequency location of the RHP zero under the worst case operation.

It can be seen from Table 3.1 that the frequency of RHP zero for a three-phase PWM rectifier is 3/8 times that of a *dc*-*dc* boost converter for a similar operating condition. However, as a three-phase PWM rectifier system typically operates at a switching frequency much lower (10 times or more) than that of a *dc*-*dc* boost converter, the expected overall closed loop bandwidth of a three-phase rectifier may not be as high as that in a *dc*-*dc* boost converter system. Thus, the RHP zero imposes a stricter limitation on the achievable performance of the controller in the case of a *dc*-*dc* boost converter than in the case of a PWM rectifier.

Next we will investigate briefly the significance of the RHP zero in a three-phase PWM rectifier. Let us suppose that the line inductors are designed such that the voltage drop across the inductor under full load is *x*% of the supply voltage. The output power P_{dc} and the inductor value can be expressed as follows:

$$P_{dc} = \frac{3}{2} E_d I_d \quad \text{and} \quad L = \frac{xE_d}{100\omega I_d} \quad , \tag{3.22}$$

where I_d is the full-load *d*-axis current and ω is the line frequency in rad/sec.

Substituting (3.22) into (3.21), we have

$$f_z = \frac{100 f}{x} , \tag{3.23}$$

where *f* is the line frequency in *Hz*.

From (3.23), it may be noted that the RHP zero location for a given line frequency depends only on the inductor choice. Table 3.2 shows the location of RHP zero corresponding to the choice of the inductor value for a line frequency of 50 *Hz*.

TABLE 3.2 THE LOCATION OF RHP ZERO CORRESPONDING TO THE CHOICE OF THE INDUCTOR VALUE

x (%)	1	2	3	4
f_z (Hz)	5000	2500	1667	1250

Thus, the effect of the RHP zero on the achievable performance will become significant at a higher switching frequency for a given inductor size. For example, let x equal 2% and the switching frequency be 6 *kHz*. From Table 3.2, this results in the corner frequency of RHP zero being at 2.5 *kHz*. In this case, the presence of RHP zero will indeed affect the closed loop performance of the PWM rectifier and limit the achievable closed loop bandwidth. Thus, the effect of the RHP zero on the achievable performance may be expected to be more pronounced at low and medium power applications, where the switching frequency will be on the high side.

It is also worth noting that during inverter-mode operation, when energy is being fed into the *ac* mains, an *ac*-to-*dc* converter can be represented as a buck converter which contains a left *s*-half-plane zero [61]. Thus, in the inverter-mode operation, the PWM rectifier system does not suffer from the RHP zero problems. This is true in the case of a *dc*-*dc* boost converter also. A two-switch *dc*-d*c* boost converter merely acts as a buck converter during reverse energy flow and thus may be expected not to suffer from any RHP zero problem.

Likewise, the resonant corner frequency and the damping ratio can be calculated as

$$f_0 = \frac{1-D}{2\pi}\sqrt{\frac{3}{8LC}} \quad \text{and} \quad \varsigma = \frac{1}{2R_{dc}} \cdot \frac{1}{(1-D)}\sqrt{\frac{8L}{3C}} \tag{3.24}$$

where $(1-D) = \frac{2E_d}{V_{dc}}$.

Here, f_0 is the resonant corner frequency with $\omega_0=2\pi f_0$ and ς is the damping ratio. Their values can be found by matching the denominator of (3.20) with the expression $\omega_0^2 + 2\varsigma\omega_0 s + s^2$. It may be noted that besides depending on the values of line inductance and output capacitance, both the resonant frequency and the damping ratio are dependent on the steady-state duty cycle. The damping ratio is also dependent on the load conditions. For a load of 45 Ω, the resonant corner frequency is 110 Hz and the damping ratio is 0.1181. The zero and the poles are all dependent on the operating duty cycle making control design more difficult.

3.2.5 Limitation on achievable performance of the voltage loop

With the equivalent SISO system as given in Fig. 3.5, a simple closed loop control scheme can be implemented for controlling the output voltage as shown in Fig. 3.13 (a). Here, the PWM rectifier operated in a quasi open-loop fashion described above is placed within a voltage control loop to regulate the *dc* output voltage. This simple direct voltage mode control will be investigated to bring out the limits imposed by the RHP zero on the performance of the three-phase PWM rectifier.

It is well known that the output performance of a single-phase power factor correction unit is limited by the slow response of the bulky capacitor. This drawback is overcome by a three-phase PWM rectifier as it successfully gets rid of the line frequency

related ripple on the *dc* side. This allows a ripple-free output voltage operation to be achieved even with a small filter capacitor. As a result, it may seem that the constraint on achievable performance of the voltage loop is totally eliminated because of the fast change in the *dc* output voltage in response to changes in the delivered output power. However, this is not really the case, as the achievable performance of the voltage loop depends not only on the size of the capacitor but also on the location of the RHP zero in the system transfer function.

To illustrate how these two factors (small size of output capacitor and the presence of RHP zero) affect the output performance, the dynamic operation under a step increase in *d*-axis duty ratio is explained qualitatively in the following. This explanation is similar to that normally given for describing the time domain effect of the RHP zero in a *dc* to *dc* boost converter [42, 66].

A step increase of the on-time of the virtual switch (corresponding to a step decrease in switching function u_{d2}) in the equivalent circuit of Fig. 3.4 (b) increases the discharging time of the output capacitor within a switching period. This results in the output voltage initially dipping, however with a delay due to the output side time constant τ ($=R_{dc}C$). Eventually, the *d*-axis input current will build up because of the increased on-time of the switch due to the higher duty ratio value. This increased input inductor current will then result in greater charge flowing into the output capacitor and raising the output voltage even with the reduced capacitor charging time. Thus, the *dc* output voltage initially changes in the 'wrong' direction and exhibits an undershoot during the immediate interval following the step-increase in the duty ratio. Following this initial undershoot, the output voltage recovers and increases ultimately to a higher

value as demanded by the increased duty ratio. This provides the physical insight into why the non-minimum phase feature (the RHP zero) exists in a PWM rectifier system.

In a voltage mode control scheme, if a step increase is given to the reference voltage, the resulting increase in the duty cycle *d* (decrease in the switching function u_{d2}) will cause an initial dip in the *dc* output voltage. The voltage loop can start to correct the voltage error only after the *dc* output voltage begins to increase again following this initial dip. If the voltage control loop attempts a faster restoration of the *dc* output voltage, a positive feedback action will take place and instability will occur. Therefore, although size reduction in the output capacitor will improve achievable output performance to some extent, the constraint on dynamic performance is imposed by the non-minimum phase feature and is thus rooted in the fundamental behavior of the boost-type PWM rectifier system.

3.3 Experimental verification of the proposed dual SISO model

The proposed control scheme was implemented on a DSPACE DSP system (DS1104), which uses a floating processor MPC8240 as the main processor, and a TMS320F240 motion control DSP as an interface with the power converter. The specifications for the experimental three-phase boost-type PWM rectifier are shown in Table 3.3.

TABLE 3.3 EXPERIMENTAL RECTIFIER SPECIFICATIONS

Supply voltage (phase voltage)	Output voltage	Switching frequency	L	C	R_{dc}
$60V_{RMS}$, 50Hz	200V	10kHz	4.15mH	136μF	45~180Ω

For model verification purposes, the operating conditions were chosen such that the effect of RHP zero on the system performance was pronounced. As corner frequency of RHP zero is a function of square of supply voltage, using a low supply voltage is a simple way to push the RHP zero close to the imaginary axis for the power delivered and value of inductors used. Large valued inductors were used for the same purpose and also for increasing the rectifier input admittance [63] thus reducing the sensitivity to the three-phase *ac* source especially during open-loop operation. In addition, as stated earlier, resistive load was used on the *dc* side for model verification purposes.

This part of the experiment focused on the investigation of three aspects of the developed analytical model. These are the verification of the proposed quasi open-loop operation of the equivalent *d*-axis SISO model in the frequency domain, the verification of the assumption neglecting the *q*-axis disturbance on the *d*-axis performance and lastly the verification of the expected undershoot (overshoot) in the dc output voltage response for a step increase (decrease) in the equivalent duty ratio.

As the location of the RHP zero is closest to the imaginary axis in the complex s-plane under maximum *d*-axis current and minimum supply voltage condition based on (3.21.a), experiments were carried out with a supply voltage of $60V_{RMS}$ (phase voltage), 50 *Hz* and a load of 45*Ω*. This results in the worst RHP zero location with regard to the specifications in Table 3.3. The corresponding value of e_d is 84.8 *V*.

As indicated in Fig. 3.5, de-coupling control v_{d1}, v_{q1} (corresponding to u_{d1}, u_{q1}) were employed. Additionally, a current controller (corresponding to u_{q2}) was used in the *q*-axis to make the effect of *q*-axis current on the *d*-axis insignificant again as shown in Fig. 3.5.

As the *q*-axis dynamics is a first order system represented by (3.12), a simple proportional integral controller with a proportional gain of 25 and an integral gain of 1695 was employed. To bring the converter to a certain operating point (200V output voltage, here), the duty ratio *d* can be selected based on (3.14).

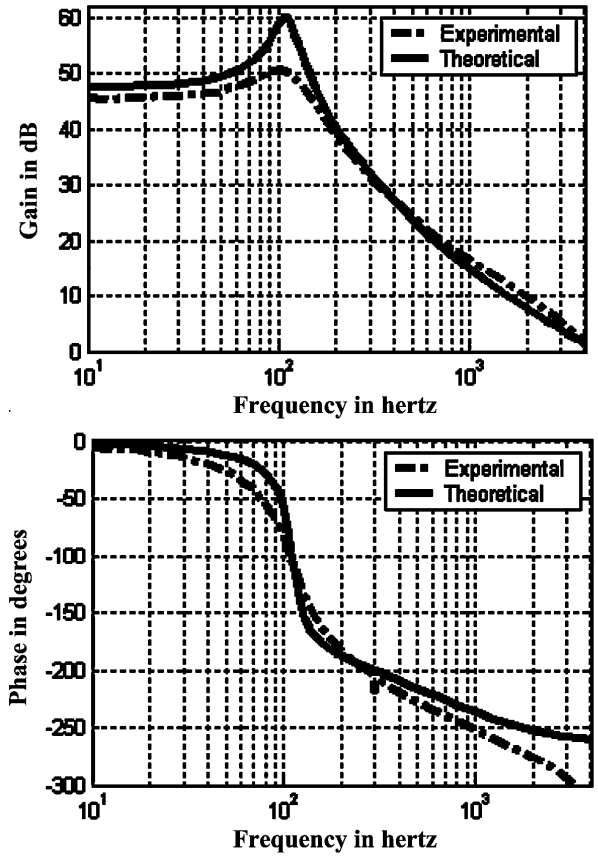


Fig. 3.6 Control-to-*dc* output voltage Bode plots under a supply voltage of $60V_{RMS}$, $50Hz$ and a load resistor of 45Ω - Quasi open-loop operation

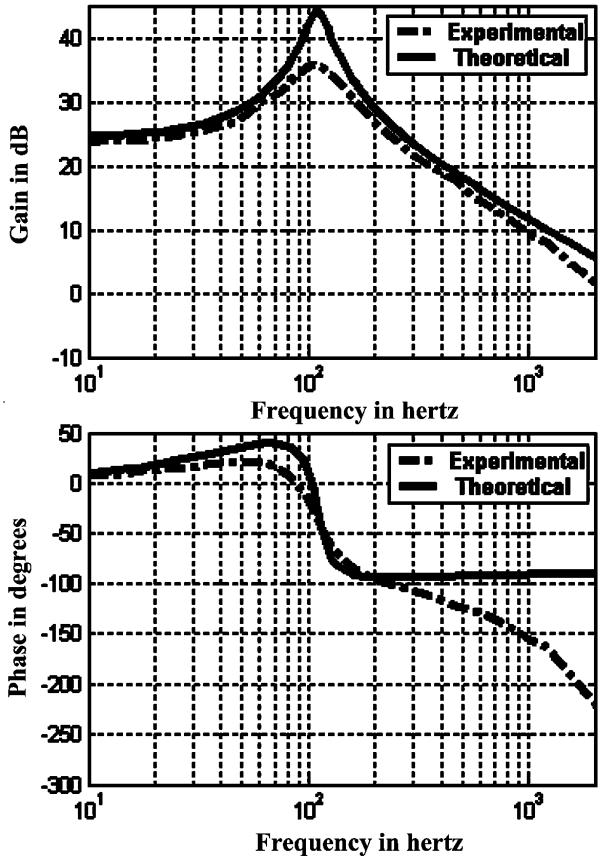


Fig. 3.7 Control-to-*d*-axis current Bode plots under a supply voltage of $60V_{RMS}$, $50Hz$ and a load resistor of 45Ω - Quasi open-loop operation

For the purpose of measuring the control to output transfer functions, a perturbation signal $\tilde{u}_{d2}$ was introduced from a HP4194A gain-phase analyzer into the control input as shown in Fig. 3.5. Fig. 3.6 shows that the measured control to dc output voltage Bode Plots closely match the theoretical Bode plots obtained based on the ideal transfer function (3.19). From the theoretical curve in Fig. 3.6, it may be seen that at a frequency of about $110Hz$ (using equation (3.24)), the PWM rectifier has a pair of complex poles which results in the phase rolling down from 0 degrees to -180 degrees and the slope of the magnitude (gain) curve changing from 0 dB/decade to -40 dB/decade. The presence of the RHP zero at about 466 *Hz* (using equation (3.21)) may be understood by the slope of the gain increasing from -40 dB/decade to -20 dB/decade and the phase rolling further down

towards -270 degrees. The measured curve has a similar shape except for a more damped response caused by the parasitic losses in the system. As mentioned in the introduction section, the presence of the RHP zero with a corner frequency of 466 *Hz* will limit the closed-loop bandwidth to a frequency much less than this value.

Fig. 3.7 shows that the experimental control to *d*-axis current Bode Plots against the theoretical Bode plots obtained based on the ideal transfer function (3.20). From the theoretical curve in Fig. 3.7, it may be seen that at a frequency of about 110*Hz* (using equation (3.24)), the PWM rectifier has a pair of complex poles which results in the phase rolling down from 0 degrees to -180 degrees and the slope of the magnitude (gain) curve changing from 0 dB/decade to -40 dB/decade. Similarly, the measured curve has a similar shape except for a more damped response caused by the parasitic losses in the system.

Next, how changes in the *q*-axis current affect the dynamics of *d*-axis was investigated experimentally. The key to the proposed dual SISO model (3.9) is the viewing of the term $v_{q2}i_q$ as a small disturbance from *q*-axis to *d*-axis in (3.8). To verify the effectiveness of the dual SISO model in ignoring this term, the small signal control to output frequency response curves were determined again with the *q*-axis current being regulated to be a non-zero value of ± 2 A. As the *d*-axis current is 7.5 A in both the cases, the corresponding power factors are around 0.966 leading and lagging, respectively. The power factor value was obtained by taking the ratio of real power (*P*) over apparent power (*S*) as given below.

$$PF = \frac{p}{S} = \frac{3e_d i_d / 2}{3\sqrt{e_d^2 + e_q^2}\sqrt{i_d^2 + i_q^2} / 2} = \frac{i_d}{\sqrt{i_d^2 + i_q^2}} \tag{3.25}$$

Fig. 3.8 shows the differences in the experimental magnitude and phase plots of the control-to-output frequency responses between unity power factor and lagging power factor operations (dashed line) and between unity power factor and leading power factor operations (solid line). As may be noticed, the differences introduced by even such a large variation in the *q*-axis current on the small signal transfer functions are quite insignificant, typically less than 1 dB in magnitude and 5 degrees in phase for most of the frequency range. Therefore, the ignoring of the small disturbance due to the *q*-axis current on the *d*-axis dynamics in this model is justified so long as the power factor is kept close to unity.

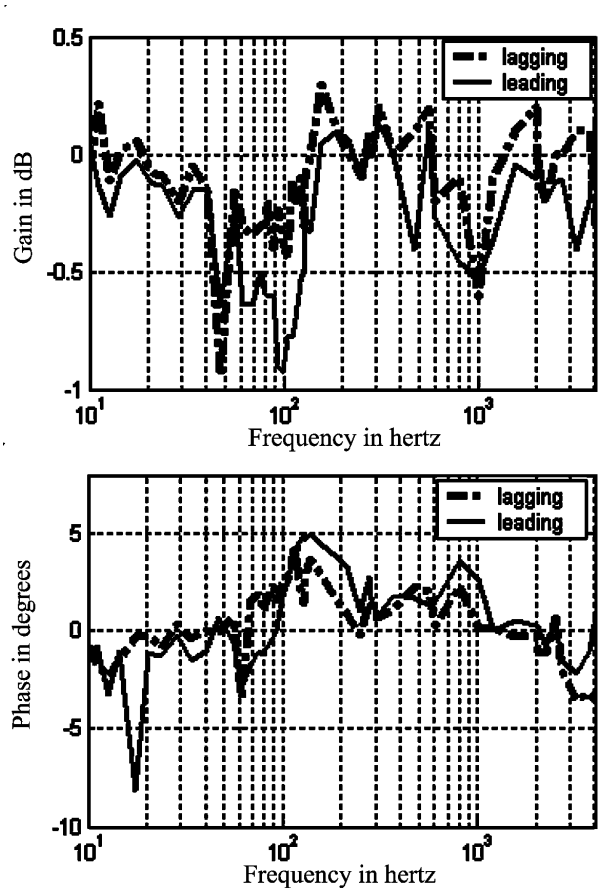


Fig. 3.8 Magnitude and phase difference curves between unity power factor operation and leading power factor operation (solid line) and between unity power factor operation and lagging power factor operation (dashed line) with a supply voltage of $60V_{RMS}$, $50Hz$ and a load resistor of 45Ω - Quasi open-loop operation

The experimental verification of the frequency domain responses provided in Fig. 3.6, Fig. 3.7 and Fig. 3.8 demonstrate the effectiveness of the proposed dual SISO model. Fig. 3.6 also shows the presence of the RHP zero in the system transfer function. Next, the effect of this RHP zero on the behavior of the PWM rectifier in time domain is examined.

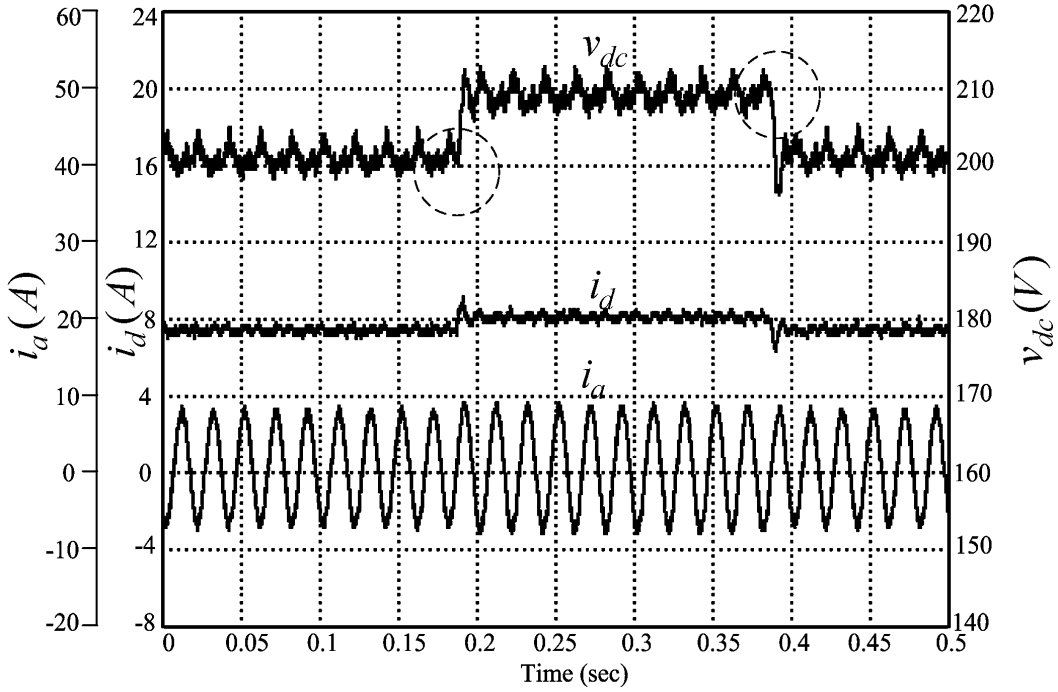


Fig. 3.9 Output voltage, *d*-axis current and a-phase current waveforms for a step change in *d*-axis duty ratio d from 0.21 to 0.25 and back to 0.21 under a supply voltage of $60V_{RMS}$, $50Hz$ and a load resistor of 45Ω - Quasi open-loop operation

It is known that in a system with an odd number of real RHP zeros, the step response initially starts off in the wrong direction as pointed out in [67] and as explained earlier. As a result, if the duty ratio d increases in a step fashion, the output voltage should exhibit an undershoot initially before finally reaching a higher value. To demonstrate this, a step change in d from 0.21 to 0.25 back to 0.21 was applied to the experimental system and the corresponding responses are shown in Fig. 3.9. The undershoot (for *d* from 0.21 to 0.25) and overshoot (for *d* from 0.25 to 0.21) are not found to be obviously noticeable in the

experimental response. Even though the RHP zero is present here, the effect is not visible because of presence of noise in the experiment system.

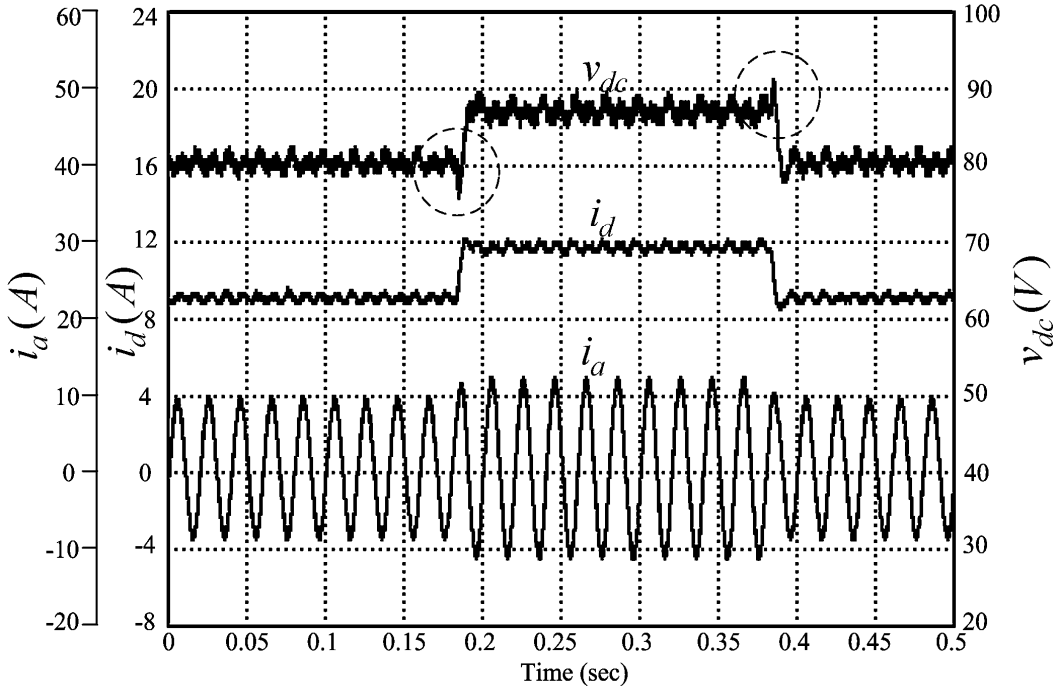


Fig. 3.10 Output voltage, *d*-axis current and a-phase current waveforms for a step change in *d*-axis switching function d from 0.45 to 0.55 and back to 0.45 under a supply voltage of $20V_{RMS}$, $50Hz$ and a load resistor of 20Ω - Quasi open-loop operation

In order to increase system damping and make the effect of RHP zero more pronounced, an experiment was carried out with a supply voltage of $20V_{RMS}$, 50 *Hz* and a load of 20Ω with a step change in d from 0.45 to 0.55 and back to 0.45. With this new operating point, the resultant damping ratio theoretically increases from 0.127 to 0.41 based on (3.24) whereas the theoretical RHP zero corner frequency shifts from 404*Hz* to 87*Hz* based on (3.21). The resultant experimental waveforms are shown in Fig. 3.9. As expected, in this case, there is a clearly noticeable undershoot (overshoot) in the dc output voltage for a step increase (decrease) in duty ratio.

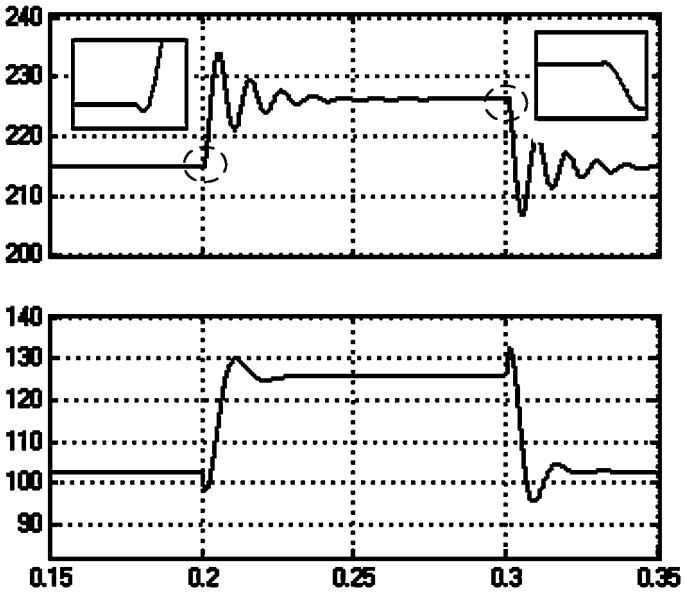


Fig. 3.11 Simulated step responses (a) a step change in *d*-axis switching function d from 0.21 to 0.25 and back to 0.21 under a supply voltage of $60V_{RMS}$, 50*Hz* and a load resistor of 45*Ω* (b) a step change in *d*-axis switching function d from 0.45 to 0.55 and back to 0.45 under a supply voltage of $20V_{RMS}$, 50*Hz* and a load resistor of 20*Ω*

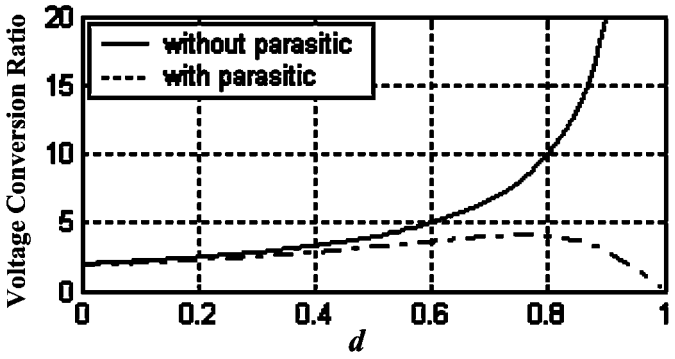


Fig. 3.12 Effect of parasitic loss on voltage conversion ratio (without inductor parasitic resistance / with inductor parasitic resistance of value 1*Ω*)

To further justify the experimental results, simulations were carried out based on the averaged large-signal model given by (3.10). Fig. 3.11 (a) shows the simulated response for a step change in duty ratio from 0.21 to 0.25 and back to 0.21 under a supply voltage of 60 V_{RMS}, 50 *Hz* and a load resistor of 45 *Ω*. As in the experimental results, characteristic undershoot (overshoot) is not obvious and can be observed only under zoomed in

conditions. Fig. 3.11 (b) shows the simulated step response in duty ratio from 0.45 to 0.55 and back to 0.55 under a supply voltage of 20 V_{RMS}, 50Hz and a load resistor of 20 Ω. The characteristic undershoot and overshoot become obvious under this operating point. Thus both the simulated and the experimental results show the expected time response behavior which is the hallmark of systems with an RHP zero.

It may be noted that the duty ratios d used in the open loop experiment do not correspond to the predicted values based on (3.14). For example, in Fig. 3.9, the d-axis duty ratio was set equal to 0.21. The ideal theoretical dc output voltage for this duty cycle with a d-axis supply voltage e_d of 84.8V equals 214.8 V as shown in Fig. 3.11 (a). As against this value, the actual experimental dc output voltage reaches only 200 V as may be seen from Fig. 3.9. This reduction may be attributed to unaccounted converter losses. Equations (3.14), (3.15) and Fig. 3.12 show how the voltage conversion ratio is reduced when parasitic losses are assumed to exist in the circuit. The curve in Fig. 3.12 was obtained by assuming a loss resistor of value 1 Ω in series with the inductance. Though the losses in the converter will occur in several components, for illustrative purposes the parasitic loss was assumed to occur only in the inductor. With the loss included, the transfer ratio declines when d approaches unity. This is the reason why the duty ratios used in the experiment are always greater than the calculated values.

3.4 Voltage mode control and current mode control - design examples and experimental results

In this section, both single loop voltage and multi-loop current mode control are designed based on the small signal transfer functions. One purpose is to experimentally

evaluate and compare the performances of the PWM rectifier with these two controllers. Another purpose is to justify further the effectiveness of the proposed dual SISO model.

Table 3.4 shows the small signal *d*-axis transfer functions of the three phase rectifier obtained using the quasi *dc-dc* boost converter model shown in Fig. 3.4(b). Using these, appropriate compensators can be designed utilizing simple linear frequency domain techniques. Table 3.4 also shows the open loop and the closed loop performance functions of the audio susceptibility and the output impedance. This information allows performance evaluation of the designed controllers.

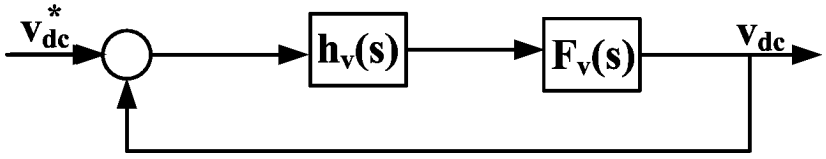
Just as a conventional boost *dc-dc* converter, a three-phase boost-type PWM rectifier also suffers from the problem of right half plane (RHP) zero in control-to-output transfer functions of $F_v(s)$ and $F_{vi}(s)$ as shown in Table 3.4 and as discussed earlier. The knowledge of RHP zero's location is vital to the successful design of a stable controller for the rectifier, as the presence of the RHP zero imposes a strict limit on the achievable closed loop performance.

The specifications for the three-phase boost-type PWM rectifier are shown in Table 3.3. The location of the RHP zero (see Table 3.2) is closest to the imaginary axis in the complex s-plane under maximum load condition, as mentioned earlier. Thus, the controllers are designed for the worst case with a load of 45 Ω. The requirements in the design of a closed loop controller are fast transient response time, low output impedance, low audio susceptibility [68] and desired phase margins.

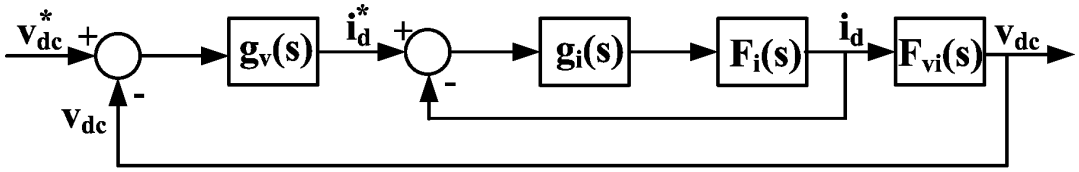
3.4.1 Voltage Mode Control Design

The voltage mode controller shown in Fig. 3.13.a has a single loop structure. A

three-pole and two-zero compensator $h_v(s)$ which has three cascaded stages $h_{v1}(s)$, $h_{v2}(s)$, $h_{v3}(s)$ with ($h_v(s)= h_{v1}(s) \cdot h_{v2}(s) \cdot h_{v3}(s)$) is adopted here. The first stage $h_{v1}(s)$ achieves the desired phase margin at the desired bandwidth. The second stage $h_{v2}(s)$ is designed to meet the desired steady state error. The third stage $h_{v3}(s)$ is used to neutralize the effect of the equivalent series resistance (ESR) of the dc output capacitor.



(a)



(b)

Fig. 3.13 Structure of voltage mode control and current mode control

The compensator function $h_{v1}(s)$ is selected to be a simple lead-lag compensator. The zero of $h_{v1}(s)$ is taken as the complex pole pair ω_0 of the system and the pole of $h_{v1}(s)$ is chosen to be ten times ω_0. The compensator function $h_{v2}(s)$ is selected to be a simple proportional-integral (PI) controller. The proportional gain is set to unity and the integral gain is selected such that the loop gain at *dc* is large enough to eliminate steady-state error with acceptable error convergence speed. At the same time, this compensator function must not affect the phase and gain margins already designed. The inclusion of the ESR, r_c, in the system model will result in an additional left half plane (LHP) zero on the control-to-output transfer function $F_v(s)$. The compensator function $h_{v3}(s)$ is selected to be

a single-pole function with the pole located close to the zero frequency of 1/ (Cr_c). This third stage also reduces the effect of switching noise by canceling the 20 dB/dec upwards slope in the loop transfer function resulting from the LHP zero due to the ESR. For simplicity, the transfer functions shown in Table 3.1 do not show the effect of the ESR of the *dc* output capacitor.

Finally, the *dc* gain of the three-pole and two-zero compensator is selected such that the desired gain crossover frequency is achieved.

3.4.2 Current mode control design

The current mode controller shown in Fig. 3.13.(b) has a widely-used cascaded structure. In designing a multi-loop controller, one first designs the inner loop. The current controller $g_i(s)$ is constructed by two cascaded stage compensators $g_{i1}(s)$ and $g_{i2}(s)$ where the first stage $g_{i1}(s)$ is selected as a lead-lag compensator and the second stage $g_{i2}(s)$ is chosen as a proportional-integral controller. The design of the cascaded stage compensator $g_i(s)$ is similar to the design of the first two stages of the single-loop controller.

Once the current loop is closed, the converter can be treated as a new open loop plant with transfer function $F_{vi}(s)$ given by Table 3.4. The voltage regulator g_v(s) contains three poles and one zero. The first pole is placed at the origin for tight dc output voltage regulation. The second pole is placed at the corner frequency of the RHP zero to compensate the 20 dB/dec upwards slope resulting from RHP zero. The third pole is placed in order to cancel the ESR zero. The zero is placed such that the denominator of the transfer function $F_{vi}(s)$ is cancelled out. The *dc* gain is again selected to meet the

requirements of the cross-over frequency.

TABLE 3.4 CLOSED LOOP SMALL SIGNAL TRANSFER FUNCTIONS

	Voltage mode control	Current mode control
Control Gain $F_v(s)=\frac{\hat{v}_{dc}}{\hat{u}_{d2}}$ $F_i(s)=\frac{\hat{v}_{dc}}{\hat{i}_d}$ $F_{vi}(s)=\frac{\hat{i}_d}{\hat{u}_{d2}}$	$F_v(s)=\frac{2e_d}{D^2}\frac{1-\frac{8L}{3R_{dc}D^2}s}{\Delta(s)}$	$F_i(s)=\frac{16e_d}{3D^3R_{dc}}\frac{1+\frac{R_{dc}C}{2}s}{\Delta(s)}$ $F_{vi}(s)=\frac{3DR_{dc}}{8}\frac{1-\frac{8L}{3R_{dc}D^2}s}{1+\frac{R_{dc}C}{2}s}$
Open loop audio susceptibility	$F(s)=\frac{2}{D}\frac{1}{\Delta'(s)}$	
Open loop output impedance	$Z_o(s)=-\frac{8L}{3D^2}\frac{s}{\Delta'(s)}$	
Closed loop audio susceptibility	$F'(s)==\frac{F(s)}{1+T_v(s)}$	$F''(s)=\frac{F(s)}{1+T_i(s)}$
Closed loop output impedance	$Z_o'(s)=\frac{Z_o(s)}{1+T_v'(s)}$	$Z_o''(s)=\frac{Z_o(s)}{1+T_i'(s)}$

Here, $\Delta(s)=1+\frac{8L}{3R_{dc}D^2}s+\frac{8LC}{3D^2}s^2$, $\Delta'(s)=1+\frac{8LC}{3D^2}s^2$, $T_v(s)=F_v(s)h_v(s)$, $T_i(s)=F_v(s)g_v(s)g_i(s)$, $T'_v(s)=F'_v(s)h_v(s)$ and $T_i(s)=F'_v(s)g_v(s)g_i(s)$ where $h_v(s)$ is voltage mode controller shown in Fig. 3.13.(a), $g_i(s)$ and $g_v(s)$ being the outer and inner loop controllers of the current mode control as shown in Fig. 3.13.(b) , and $F'_v(s)= F_v(s)\Delta(s)/\Delta'(s)$.

3.4.3 The *q*-axis controller design

The dynamics of *q*-axis is represented by a first-order system given in (3.12). A simple proportional-integral controller is designed for unity power factor regulation as follows.

$$C(s)=k_p+\frac{k_i}{s} \tag{3.26}$$

with $k_p = 2\pi fL$ and $k_i = 2\pi fR$.

The open-loop and closed-loop transfer function of the PWM rectifier can be written as

$$G_o(s) = \frac{2\pi f}{s} \tag{3.27}$$

$$T(s) = \frac{1}{Ts + 1} \tag{3.28}$$

where $T = 1/2\pi f$, f is the bandwidth of closed loop system with proportional integral controller.

3.5 Closed loop experimental verification of the proposed controllers

The proposed control scheme was implemented on a DSPACE DSP system (DS1104), which uses a floating processor MPC8240 as the main processor, and a TMS320F240 motion control DSP as an interface with the power converter. The specifications for the experimental three-phase boost-type PWM rectifier are as shown previously in Table 3.3.

As the *d*-axis equivalent circuit shown in Fig. 3.4.(b) does not independently exist on the hardware prototype, the de-coupling controllers *and* an effective current controller in *q*-axis should be implemented as mentioned earlier in Section 3.1.5. A proportional integral controller with a proportional gain of 0.25 and an integral gain of 16.95 was employed to determine the control effort u_{q2} for the *q*-axis control.

At the worst case loading of 45 Ω, the corner frequency of the RHP zero is 466 Hz, the corner frequency of the resonant peak (complex pole pair) is 110 Hz and the corner frequency of the LHP zero associated with the output capacitor's ESR is 2054 Hz with an estimated ESR value of 0.57 Ω.

Based on the design procedure given in Section 3.3.1, the three poles of the compensator for the voltage mode control were located at 0 Hz for tight *dc* regulation, 1100 Hz as ten times of ω_0 and 2054 Hz to cancel out the effect of ESR, respectively. The two zeros of the compensator were located at the resonant frequency of 110 Hz and at a frequency of 20 Hz determined by the integral gain of the PI controller. Here, the realizable closed loop bandwidth is limited by the corner frequency of the RHP zero. Thus, the *dc* gain used in the experiment was chosen as 0.0045 such that the cross-over frequency realized was 200 *Hz* and the phase margin achieved was 35.3^{o}.

Similarly, for the current mode control, the poles of the compensator of inner loop were located at 0 Hz for tight *dc* regulation and 1100 Hz at ten times of ω_0 and zeros were placed at the resonant frequency of 110 Hz and at a frequency of 200 Hz determined by the integral gain of the *PI* controller. With the above design, the cross-over frequency realized is 1000 *Hz* which is $1/10^{th}$ of the switching frequency and the phase margin achieved is 118^{o} for the inner loop. One of the advantages of the multi-loop controller is that the bandwidth of the *d*-axis current controller is not limited by the location of the RHP zero. The poles of the outer loop compensator were located at 0 Hz for tight *dc* regulation, 466 Hz to compensate the effect of the RHP zero and 2054 Hz to cancel out the effect of ESR, respectively and the zero was placed at 52 Hz to compensate for the pole due to the output filter circuit in the transfer function $F_{vi}(s)$. The *dc* gains for inner loop and outer

loop were 0.0373 and 35.1 respectively. The cross-over frequency is 80*Hz* which is less than $1/10^{th}$ time of the bandwidth of the inner loop and the phase margin achieved is 70.5^{o} for the outer loop. Integrator anti-windup technique was also employed to deal with saturation of the proportional-integral controller in both cases.

3.5.1 Measurement of open-loop loop transfer function Bode plots

Fig. 3.14 shows the experimental loop transfer function Bode plots measured with the HP4194A gain-phase analyzer along with the analytically calculated results using the transfer function in Table 3.4. With voltage mode control, the experimental cross-over frequency and phase margin are 173 *Hz* and 39.5^{o}. The better measured phase margin is likely due to two factors. Firstly, the damped response due to the parasitic losses causes loop gain to cross 0 *dB* at a frequency less than the predicted value. Secondly, parasitic losses also account for a much flatter phase response.

The measured cross-over frequency with a current mode controller is 68 *Hz* and the phase margin achieved is 70^{o} whereas the theoretical cross-over frequency is 80 *Hz* and the phase margin achieved is 70.5^{o}. The small discrepancy may again be attributed to the parasitic losses in the inductors and switches.

Fig. 3.14 also shows that the multi-loop system has a lower cross-over frequency but a much simpler dynamics. The fact that the single loop system (voltage mode controller) has a much higher cross-over frequency than the multiple loop system (current mode controller) does not necessarily imply that the former will have better closed loop performance than the latter. This will be discussed further in Section 3.5.3.

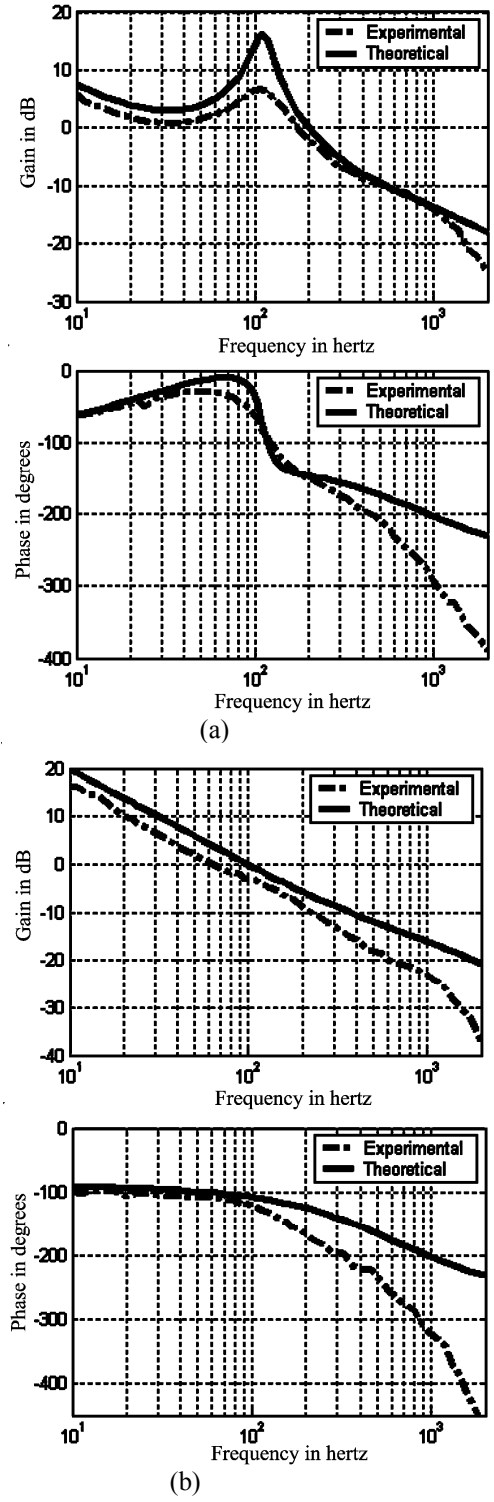


Fig. 3.14 Loop transfer function Bode plots under maximum load (45Ω): (a) with voltage mode controller, and (b) with current mode controller

3.5.2 Steady-state operation - experimental results

Fig. 3.15 shows the steady-state waveforms with both the voltage and the current mode controllers. The experimental current THD values with both controllers are given in Table 3.5. The resultant three-phase currents are also balanced and in phase with their corresponding supply voltages as shown in Fig. 3.17 in both the cases. Fig.3.16 shows the frequency spectrums of the experimental a-phase current.

Fig 3.15(a) and Fig. 3.17(a) show that even though the *d*-axis current is not controlled directly, the resultant input currents have reasonably low THD values and are balanced and in phase with their corresponding phase voltages. From Fig. 3.15 and Fig. 3.16, it can be also seen that multi-loop system provides better steady-state performance with lower input current harmonics than the single-loop system.

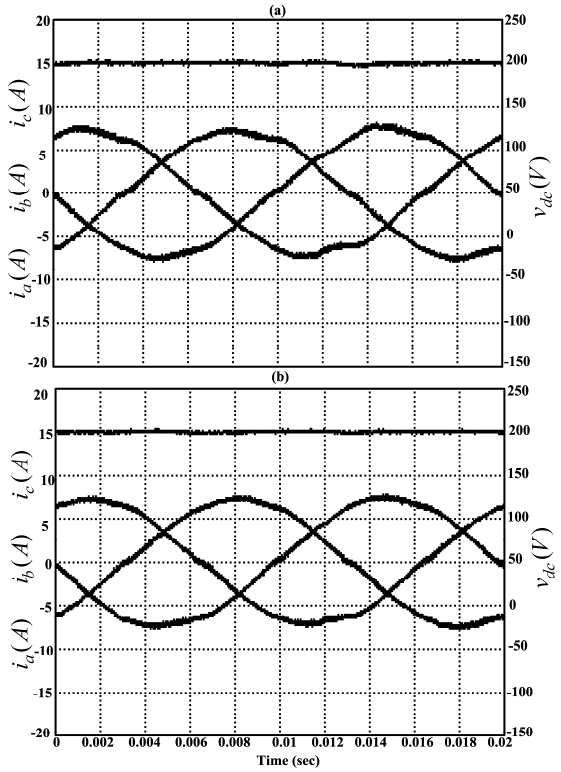


Fig. 3.15 Waveforms under steady-state operation: three-phase balanced current and output voltage: (a) Voltage mode control. (b) Current mode control

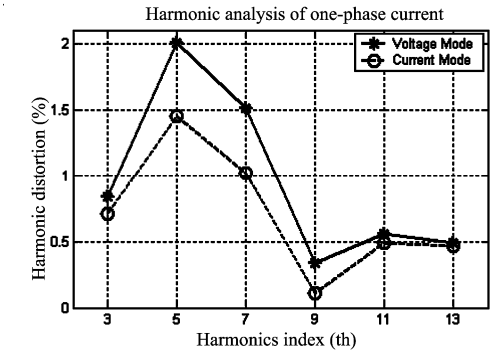


Fig. 3.16 Frequency spectra of a-phase current

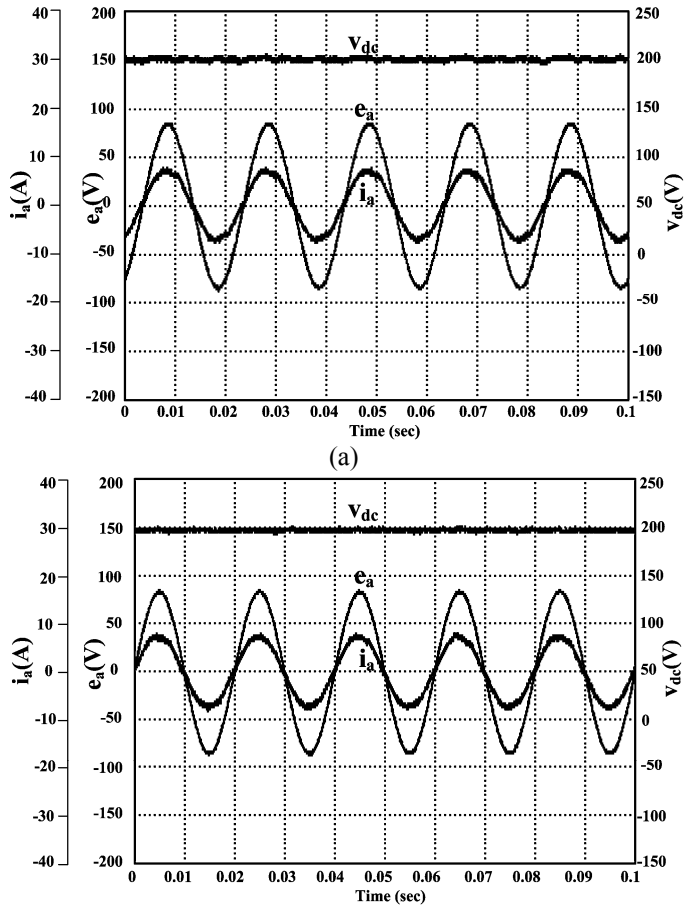


Fig. 3.17 Steady-state waveforms - a-phase current, a-phase supply voltage and *dc* output voltage: (a) Voltage mode control. (b) Current mode control

3.5.3 Transient operation - experimental results

Fig. 3.18 shows the transient responses of the *dc* output voltage and the *d*-axis current for a step change in the voltage reference from 225 V to 175 V and back to 225 V

with a 45 Ω load under both voltage mode and current mode control. The transition times and peak values of the overshoot and undershoot during step changes with both the controllers are summarized in the Table 3.5. It is worth noting that multi-loop system exhibits a faster transition than the single loop system. However, as shown in Fig. 3.14, the loop transfer function bode plot of the single loop system has a much higher crossover frequency than the multi-loop system. The apparent contradiction can be interpreted by considering the theoretical closed loop transfer function Bode plots shown in Fig. 3.19. As the dynamics of the single loop system is quite complex, its closed-loop magnitude curve crosses 0 dB several times. The open-loop loop transfer function Bode plots can not accurately indicate the closed-loop characteristics in this case. In addition, the negative loop gain in the low frequency from around 10 *Hz* to 100 *Hz* as shown in Fig. 3.19 also accounts for damped responses of the *dc* output voltage in single loop system.

On the other hand, with the current mode control, directly controlling the current feeding the output stage makes the voltage to current transfer function a first order system with an RHP zero thus largely simplifying the dynamic behavior of the feedback control system. Besides faster overall dynamics, having a current control loop makes it easy to implement over-current protection. In the present implementation, the *d*-axis current is limited to 10A for safe operation.

Fig. 3.20 shows the transient responses of the *dc* output voltage, *d*-axis current and a-phase current for a step change in the load from 45 Ω to 60 Ω and back to 45 Ω. The transition times and the peak values during the step transitions with both controllers are also summarized in the Table 3.5. The single loop system exhibits a slightly better transient performance for the load step change. This can be explained with the

theoretical frequency responses of output impedance shown in Fig. 3.21. It can be seen that both the controllers provide attenuation of the open-loop output impedance; however, the output impedance with the single-loop control is much lower than that with the multi-loop control in the frequency range between 10 *Hz* and 200 *Hz*. This is the likely reason that the single loop system exhibits a slightly better transient performance for load step changes.

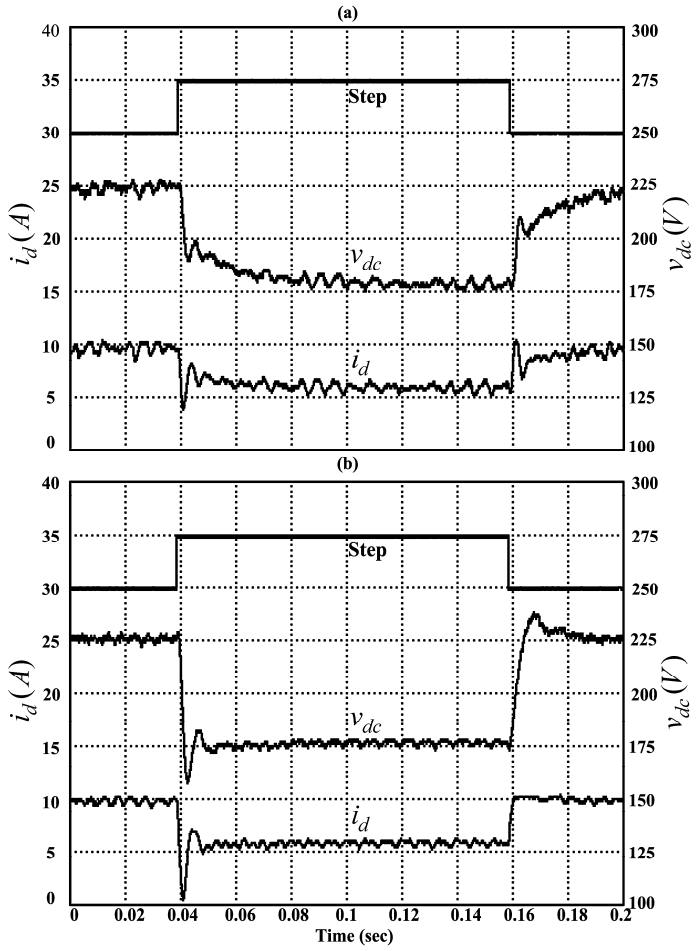


Fig. 3.18 Experimental step response for a step change in voltage reference:
(a) Voltage mode control. (b) Current mode control.

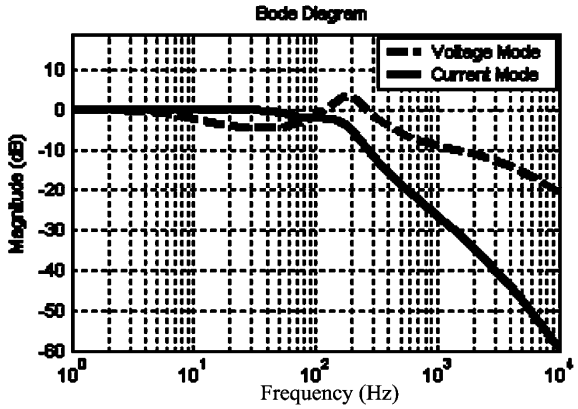


Fig. 3.19 Comparison of theoretical closed loop transfer function Bode plots

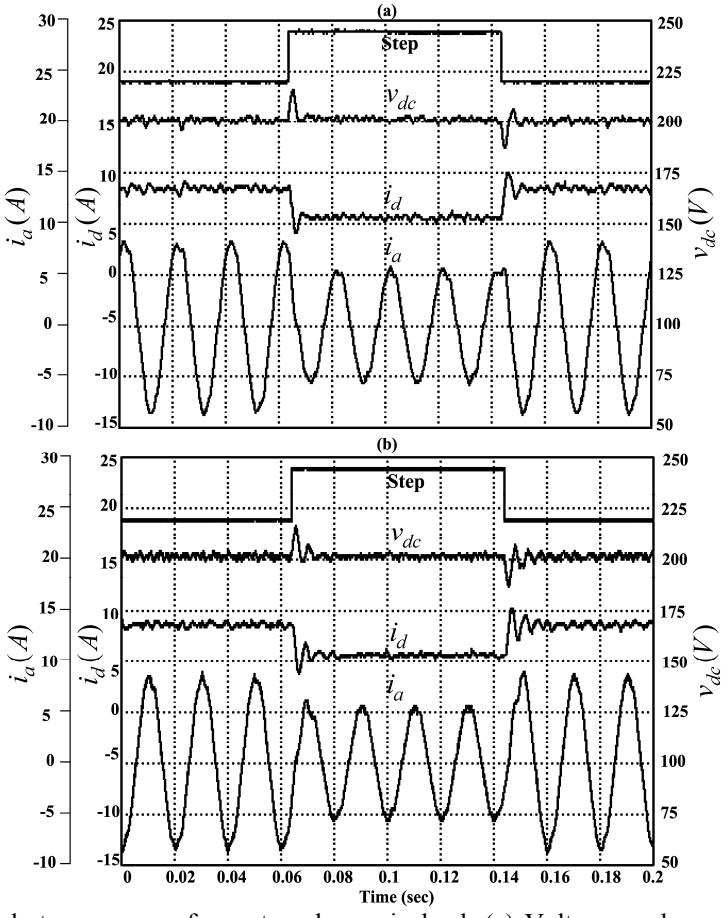


Fig. 3.20 Experimental step response for a step change in load: (a) Voltage mode control. (b) Current mode control.

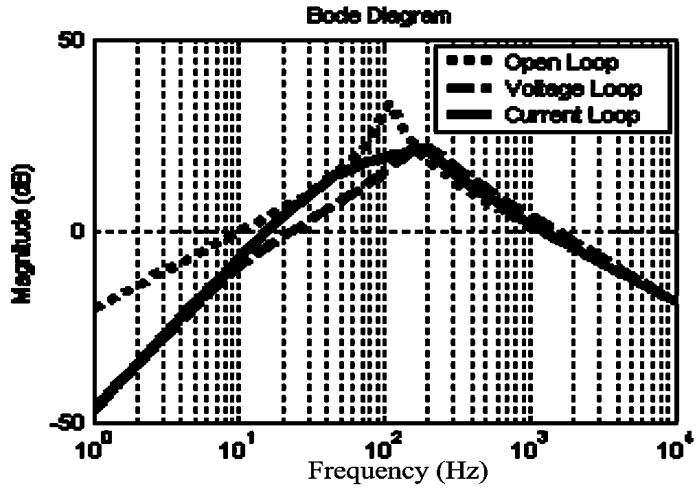


Fig. 3.21 Comparison of theoretical output impedance curves

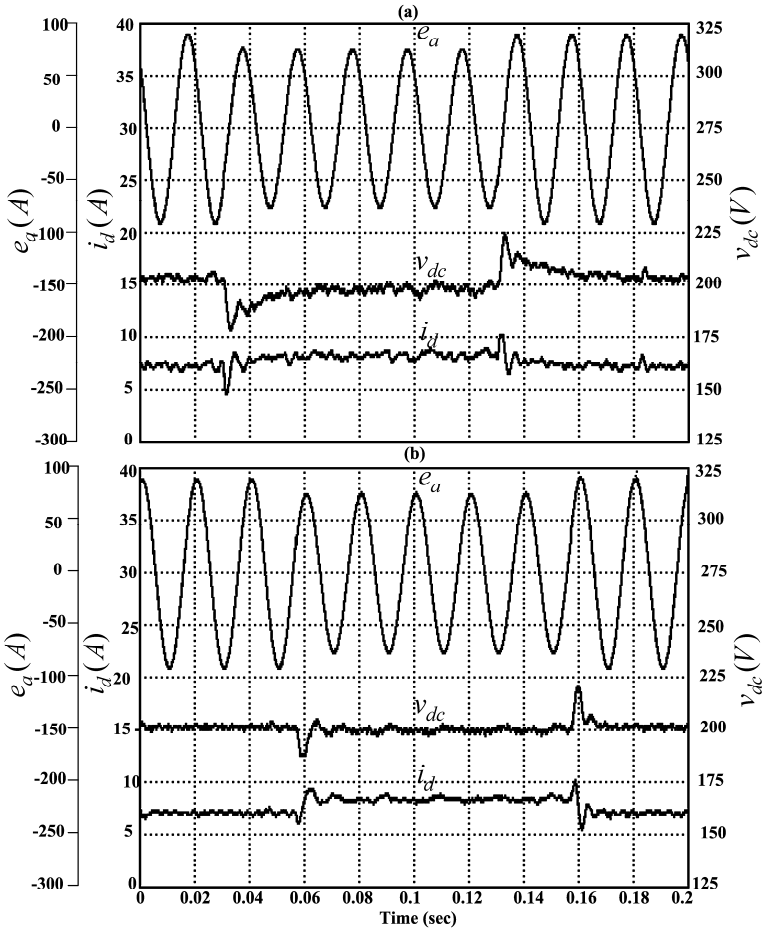


Fig. 3.22 Experimental step response for a step change in supply voltage: (a) Voltage mode control. (b) Current mode control.

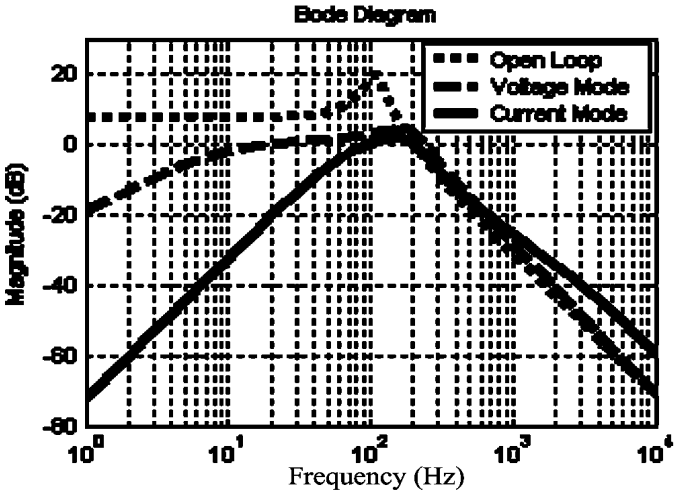


Fig. 3.23 Comparison of theoretical audio susceptibility performance

TABLE 3.5 SUMMARIES OF COMPARISON RESULTS

	Voltage mode control			Current mode control		
Current (THD)	3.86%			2.87%		
Step Change in Voltage Reference	Response time (ms)	Rise	10	Response time (ms)	Rise	3
		Fall	9		Fall	3
	Overshoot (V)		0	Overshoot (V)		13.5
	Under shoot (V)		0	Under shoot (V)		18
Step Change in *dc* Load	Response time (ms)	Rise	0.5	Response time (ms)	Rise	1.6
		Fall	0.9		Fall	1.4
	Overshoot (V)		15.5	Overshoot (V)		16.5
	Under shoot (V)		12.5	Under shoot (V)		12.5
Step Change in Supply Voltage	Response time (ms)	Rise	6	Response time (ms)	Rise	1.8
		Fall	7		Fall	2
	Overshoot (V)		25	Overshoot (V)		20.5
	Under shoot (V)		22	Under shoot (V)		12.5
Advantages/ Disadvantages	1) Simple to implement 2) Complex closed loop dynamics			1) Easy for implementing over-current protection 2) Simple closed loop dynamics 3) Overall superior performance		

Fig. 3.22 shows the experimental transient responses of the dc output voltage and *d*-axis current for a step change in the supply voltage from 65V (RMS) to 55V (RMS) and

back to 65V (RMS) under 45Ω load, which is supplied by a 1500VA/phase ac power supply/analyzer HP 6834B. The transition times and peak values during step transitions with both controllers are again summarized in Table 3.5. The transient response for a multi-loop system is much better than for the single loop system. This coincides with the comparison results of single loop and multi-loop audio susceptibility shown in Fig. 3.23. It can be seen that the multiple loop system provides much more attenuation at low frequency than the single loop system. This is the likely reason that the multiple loop exhibits better transient performance during supply voltage step changes.

From the summary of results provided in Table 3.5 and the discussion so far, we note that both the voltage mode controller and the current mode controller yield satisfactory steady-state and transient performance. The theoretical audio susceptibility and output impedance response curves for both the voltage mode control system and the current mode control system shown in Fig. 3.21 and Fig. 3.23 provide a large attenuation at low frequencies compared to the open loop system, also shown in these figures.

Among the two control systems, the current mode control system exhibits similar or better performance than the voltage mode control system in most aspects. The advantages and disadvantages of current mode control and voltage mode control are summarized in Table 3.5.

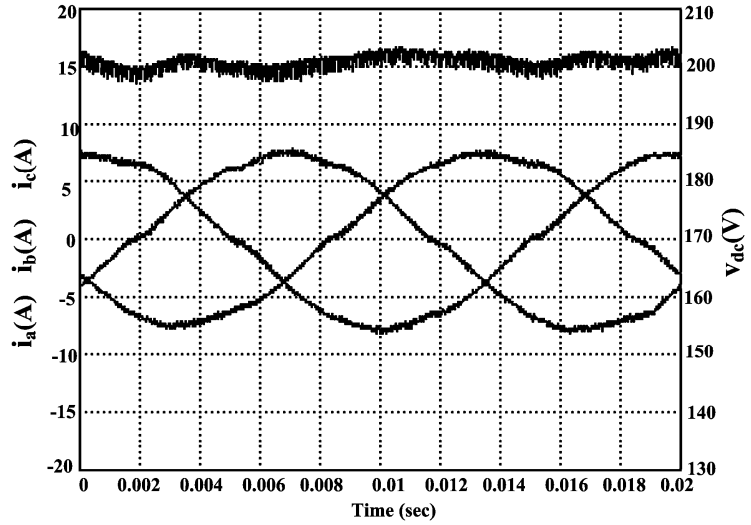
3.5.4 Experimental results under unbalanced supply voltage operation

When fed by a balanced *ac* supply, the PWM rectifier, if properly controlled, is capable of drawing three-phase balanced sinusoidal currents at a unity power factor and

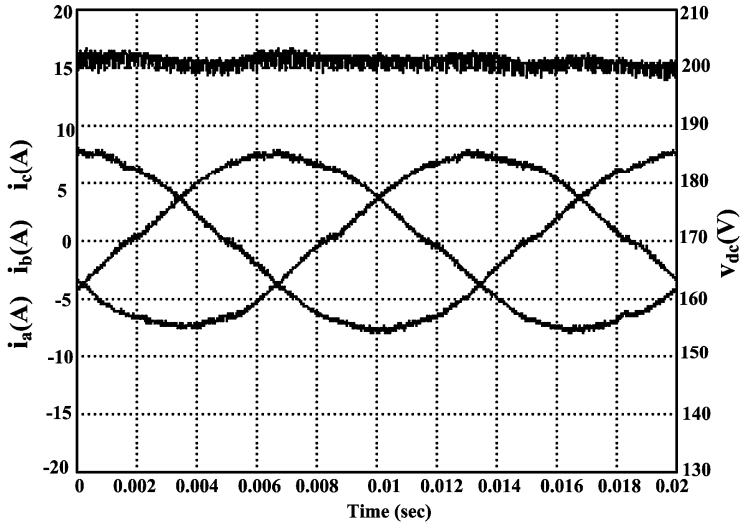
maintain the *dc* output voltage nearly constant with a small filter capacitor as shown in the above experimental results. However, unbalanced supply conditions occur frequently especially in a weak utility grid. Unbalanced supply voltages can be caused by many factors as mentioned in Chapter 1.

Since the modeling and control described in this chapter have been carried out assuming balanced supply conditions, it is important to study the effect of supply voltage unbalance on the performance of the proposed schemes. With this in view, the performance of the proposed voltage mode and current mode control schemes were experimentally investigated under unbalanced supply voltage conditions.

Firstly, a 1V imbalance was introduced in one of the phases (a-phase) using the *ac* power supply. Thus, the supply voltages (phase voltages) were kept at $59\sqrt{2}\sin\omega t$, $60\sqrt{2}\sin(\omega t+240^\circ)$ and $60\sqrt{2}\sin(\omega t-120^\circ)$. The experimental results obtained with both voltage mode and current mode controllers are shown in Fig. 3.24. As shown in Fig. 3.24, the 1.67% amplitude imbalance introduced in one of the phase voltages does not affect much the performance of the system with both voltage mode controller (Fig. 3.24(a)) and current mode controller (Fig. 3.24(b)). As with the results obtained under balanced supply voltage, the system with the current mode controller delivers slightly better results than the system with the voltage mode controller as seen from waveforms in Fig 3.24. Thus, we may conclude that both controllers are robust to slight imbalance in supply voltage.



(a)



(b)

Fig. 3.24 Waveforms for steady-state operation: three-phase balanced current and output voltage: (a) Voltage mode control. (b) Current mode control---under 1.67% magnitude unbalance in a-phase

Next, a 10% magnitude imbalance was introduced to a-phase voltage. The line voltages were kept at $54\sqrt{2}\sin\omega t$, $60\sqrt{2}\sin(\omega t + 240^\circ)$ and $60\sqrt{2}\sin(\omega t - 120^\circ)$. The results with both voltage mode controller and current mode controller are shown in Figs. 3.25 (a) and (b).

It can be seen from Fig. 3.25(a) that under voltage mode control, the dc output

voltage is affected quite significantly. A second harmonic ripple can be clearly seen to be present in the dc output voltage. On the other hand, the dc output voltage with current mode controller is much flatter than that with the voltage mode controller as may be seen in Fig. 3.25.b. The three-phase currents are more distorted as shown in Fig. 3.25.b and also from Table 3.6.

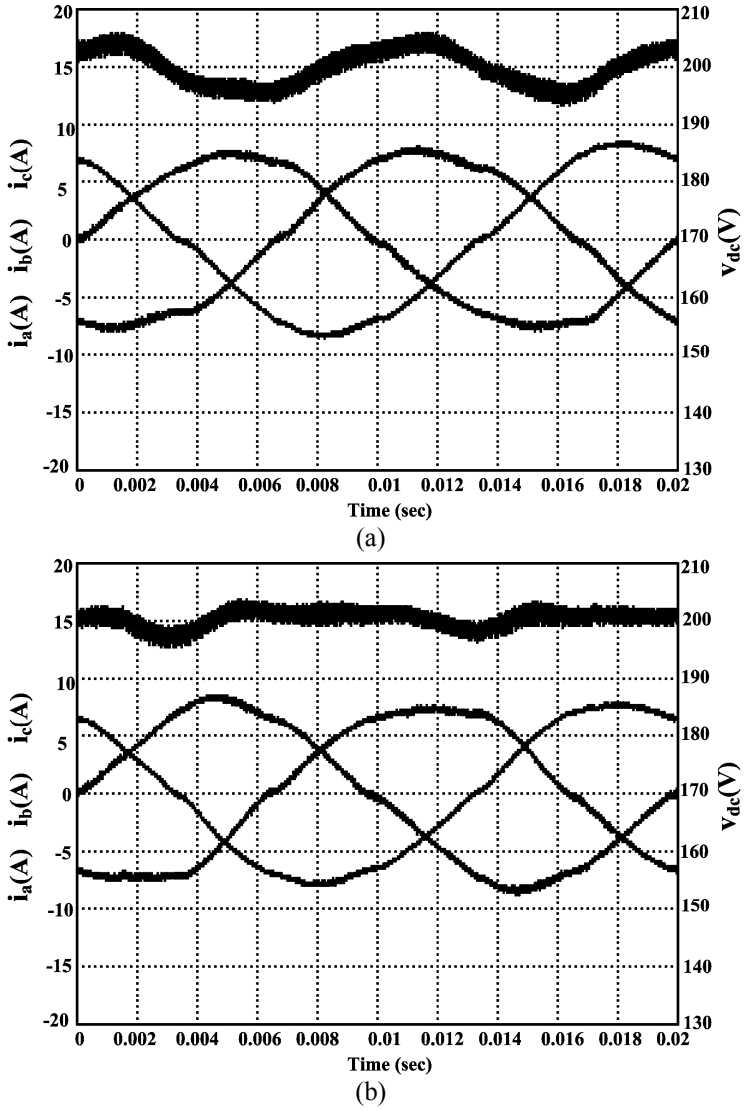


Fig. 3.25 Waveforms for steady-state operation: three-phase balanced current and output voltage: (a) Voltage mode control. (b) Current mode control---under 10% magnitude unbalance in a-phase

TABLE 3.6 TOTAL HARMONIC DISTORTION OF EXPERIMENTAL RESULTS

	Voltage Mode Control	Current Mode Control
THD of i_a (%)	5.6	7.31
THD of i_b (%)	5.08	4.17
THD of i_c (%)	5.25	7.07
Peak to Peak Ripple v_{dc} (V)	11.5	7.5

The RMS values of three-phase currents with voltage mode control are 5.28A (a-phase), 5.7 A (b-phase), 5.43A (c-phase) whereas the peak values of three-phase currents with current mode control are 5.50A (a-phase), 5.52A (b-phase), 5.46A (c-phase). The THDs of the three-phase currents and the peak-to-peak ripple voltage of the dc output voltage are summarized in Table 3.6. It can be concluded that in a system with the current mode controller, the *dc* output voltage is more robust to supply voltage imbalance than system with the voltage mode control. It can be also the concluded that both the voltage mode and the current mode controllers are robust to a slight supply voltage imbalance. However, both controllers can not provide satisfactory performance under the presence of large imbalance.

3.6 Conclusions

In this chapter, a dual SISO model for a three-phase PWM rectifier has been developed to facilitate the design of controllers and to provide meaningful insights into the behavior of a PWM rectifier system. The open loop characteristic of the proposed *d*-axis model has been investigated through analysis, simulations and experiments in both frequency domain and time domain.

Voltage mode and current mode control techniques, widely used in *dc* to *dc* converters, have been implemented for controlling a PWM rectifier system based on the insight that both the *d*-axis model and its equivalent circuit exhibit similarities to those of

dc to *dc* boost converters. Successful implementation of both voltage mode and current mode controllers further justify the validity of the proposed dual SISO model. This also further suggests that it may be feasible to control the PWM rectifier systems with other well-developed control design and system analysis techniques of *dc*-*dc* converters.

The effectiveness of the proposed voltage mode and current mode controller under the presence of supply voltage imbalance has been experimentally examined. It was found that both controllers can provide satisfactory performance in the face of a small supply voltage imbalance. However, under a large supply voltage imbalance, the line current is seen to be fairly distorted and a ripple appears on the dc voltage. One way to address this is to make the outer voltage loop very slow as usually done in a single phase power factor correction (PFC) application. However, this would degrade the overall dynamic performance. As the control model and techniques developed in this chapter will not be effective, there is a need to develop control schemes for PWM rectifiers which will be effective even under large supply voltage imbalances. This issue will be fully investigated in Chapter 4.

Chapter 4

Output Power Control Strategy for a Three-Phase PWM Rectifier under Unbalanced Supply Voltage Conditions

4.0 Introduction

Chapter 3 developed a dual SISO model for a PWM rectifier under balanced operating conditions and successfully implemented both voltage mode and current mode control based on the proposed model. It was found that both voltage mode and current mode controlled systems can provide high performance operation under a slight unbalanced supply voltage conditions. However, as expected, with a 10% amplitude imbalance in one phase voltage, significant second harmonic ripple occurred on the *dc* output voltage in the system with the voltage mode controller. On the other hand, significant distortion in the three-phase currents appeared in the system with the current mode controller. Thus, the control methods used in the balanced PWM rectifier system can not be directly extended to an unbalanced PWM rectifier system.

As discussed in Chapter 2, the input power control (IPC) approach in literature [48, 49] for tackling unbalanced supply conditions is relatively simple but can only roughly regulate the instantaneous output power due to the neglecting of the instantaneous power

handled by the inductances. Also, the partial output power control (POPC) method[1] in [51, 52] can, in principle, maintain nearly constant *dc* output voltage and sinusoidal line currents at unity vector power factor as desired. However, the experimental results provided in [51, 52] show a considerable second harmonic ripple and also an observable steady-state error in the *dc* output voltage when operating with a 15% magnitude imbalance in one phase as mentioned in Chapter 2 Section 2.3.

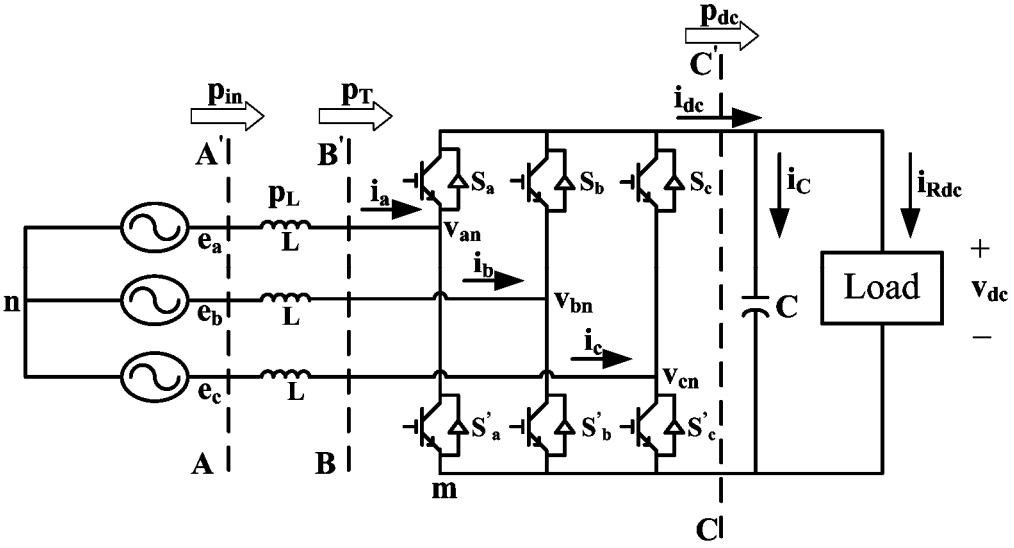


Fig. 4.1 Structure of a three phase *ac* to *dc* PWM rectifier

In this chapter, an output power control (OPC) strategy which aims to achieve excellent performances on both the output side and input side of the rectifier is proposed. In the proposed method, constant instantaneous power and zero reactive power are both maintained at the rectifier bridge input terminals. This enables simple closed form solutions for the current commands to be obtained while transferring a

[1] The method in [51, 52] has been given the name 'modified output power control' in the papers published [99] as part of the current research. The name 'partial output power control' is perhaps an accurate description of the method. Hence, in this report, the two names have been used interchangeably for this control method.

desired constant power to the *dc* side under steady-state. Delivering a constant power to the output side ensures that the output *dc* voltage is maintained constant with no or negligible low-harmonic ripple voltage. Also, due to the closed form solutions for the current commands, the implementation is simplified significantly. Thus, the proposed method has the twin advantages of ease of implementation and excellent performance. Experimental results obtained with a 1 kW laboratory prototype have been presented to verify the effectiveness of the proposed output power control method.

4.1 Positive- and negative- sequence equivalent circuits for an unbalanced PWM rectifier system

In this section, the positive and negative sequence equivalent circuits for an unbalanced PWM rectifier system are developed from fundamental concepts.

We assume in this work that the variables, although unbalanced, are sinusoidal. As is known, the unbalanced three-phase variables can be represented as the orthogonal sum of positive and negative sequence components as follows.

$$\begin{cases} x_a = x_a^p + x_a^n = x^p \cos(\omega t + \theta_x^p) + x^n \cos(\omega t + \theta_x^n) \\ x_b = x_b^p + x_b^n = x^p \cos(\omega t + \theta_x^p - 2\pi/3) + x^n \cos(\omega t + \theta_x^n + 2\pi/3) \\ x_c = x_c^p + x_c^n = x^p \cos(\omega t + \theta_x^p + 2\pi/3) + x^n \cos(\omega t + \theta_x^n - 2\pi/3) \end{cases}, \tag{4.1}$$

where x_a, x_b and x_c are the three-phase variables in the *a*-*b*-*c* frame, with x_a^p , x_b^p, x_c^p and x_a^n , x_b^n, x_c^n being the three-phase positive and negative sequence components, respectively. Also, variables x^p and x^n are the peak amplitudes of the positive and the

negative sequence variables, respectively, variables θ_x^p and θ_x^n are the corresponding phase angles and ω is the angular frequency of the power supply. In (4.1), the variable x can denote the source voltage, the line current or the rectifier bridge input voltage (averaged over a switching cycle).

It is worth noting that zero sequence components are not addressed in a three-phase PWM rectifier system. As zero sequence current is absent, zero sequence power does not exist in a three-phase three-wire PWM rectifier system notwithstanding the presence of the zero sequence supply voltage. Therefore, the *dc* side performance of an *ac*-to-*dc* power converter is not affected by the presence of the zero sequence voltage components.

For analysis and controller design purposes, it would be more convenient if the three-phase variables are transformed into a stationary α - β frame (SF) or a synchronous rotating d - q frame (SRF). The notion of an instantaneous space phasor, widely used in ac machines, can be extended to bring forth the ideas of the instantaneous current and voltage space vectors [69]. The transformations to the SF and SRF are shown graphically using phasor diagrams in Fig. 4. 2.

Let $\vec{x}_s$ be the instantaneous space vector of the three-phase variables, x_a, x_b and x_c, with $\vec{x}_s = \frac{2}{3}(x_a + e^{j2\pi/3}x_b + e^{-j2\pi/3}x_c)$. The space vector can be written as a summation of positive and negative sequence components in the SF or SRF as given below.

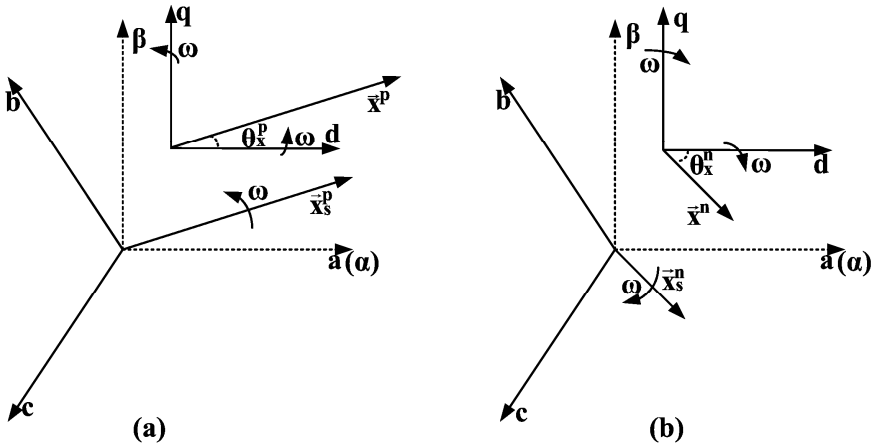


Fig. 4.2 Vector diagrams of a positive sequence component and a negative sequence component in different frames at t=0. a). a positive sequence vector diagram b) a negative sequence vector diagram

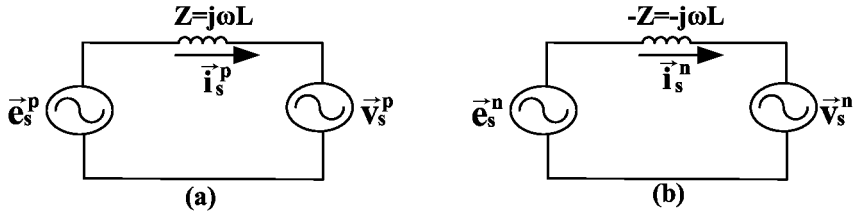


Fig. 4.3 Input side equivalent circuits: a) for the positive sequence system b) for the negative sequence system

$$\vec{x}_s = \vec{x}_s^p + \vec{x}_s^n = e^{j\omega t}\vec{x}^p + e^{-j\omega t}\vec{x}^n = x_\alpha + jx_\beta \tag{4.2}$$

Here, variables x_α and x_β are the projections of the space vector on the α-axis and β-axis, respectively. Variable $\vec{x}_s^p$ is the positive sequence space vector in SF with $\vec{x}_s^p = x^p e^{j(\omega t+\theta_x^p)}$ which is rotating counter-clockwise with a constant velocity ω and $\vec{x}_s^n$ is the negative sequence space vector in SF with $\vec{x}_s^n = x^n e^{-j(\omega t+\theta_x^n)}$ which is rotating clockwise with a constant velocity ω as shown in Fig. 4.2. Vector $\vec{x}^p$ is the positive sequence stationary vector in the positive sequence SRF with $\vec{x}^p = x_d^p + jx_q^p = x^p e^{j\theta_x^p}$ and $\vec{x}^n$ is the negative sequence stationary vector in the negative sequence SRF with $\vec{x}^n = x_d^n + jx_q^n = x^n e^{-j\theta_x^n}$ again as shown in Fig. 4.2.

Vectors x_d^p and x_q^p are projections of the positive sequence components on the *d*-axis and *q*-axis, respectively. Likewise, x_d^n and x_q^n are the projections of the negative sequence components on the *d*-axis and *q*-axis, respectively.

In Fig. 4.1, e_a, e_b, e_c represent source voltages and i_a, i_b, i_c represent input currents. Parameter *L* is the inductance value of the line inductances. If the supply voltage is balanced, then only the positive sequence voltage component exists and the Kirchoff's voltage equation on the ac side of the rectifier in SF is given by

$$\vec{e}_s^{\,p} = L\frac{d\vec{i}_s^{\,p}}{dt} + \vec{v}_s^{\,p} = j\omega L\vec{i}_s^{\,p} + \vec{v}_s^{\,p}, \tag{4.3}$$

where $\vec{e}_s^{\,p}$ and $\vec{i}_s^{\,p}$ denote the positive sequence supply voltage and current vectors in the SF with $\vec{e}_s^{\,p} = e^p e^{j(\omega t+\theta_e^p)}$ and $\vec{i}_s^{\,p} = i^p e^{j(\omega t+\theta_i^p)}$. Also, $\vec{v}_s^{\,p}$ denotes the positive sequence rectifier bridge input voltage vector in the SF. The equivalent circuit on the input side, based on (4.3) the positive sequence variables, is shown in Fig. 4.3(a).

Similarly, the voltage equation on the *ac* side of the rectifier for negative sequence in SF is given by the following and the corresponding equivalent circuit is shown in Fig. 4.3(b).

$$\vec{e}_s^{\,n} = L\frac{d\vec{i}_s^{\,n}}{dt} + \vec{v}_s^{\,n} = -j\omega L\vec{i}_s^{\,n} + \vec{v}_s^{\,n} \tag{4.4}$$

Here, $\vec{e}_s^{\,n}$ and $\vec{i}_s^{\,n}$ denote the negative sequence input voltage and current vectors in SF with $\vec{e}_s^{\,n} = e^n e^{-j(\omega t+\theta_e^n)}$ and $\vec{i}_s^{\,n} = i^n e^{-j(\omega t+\theta_i^n)}$. Also, $\vec{v}_s^{\,n}$ denotes the negative

sequence rectifier bridge input voltage vector in the SF.

Unlike the equivalent circuit shown in [53], the equivalent impedance in the negative sequence equivalent circuit in Fig. 4.3 is negative (= $-Z$) with $Z = j\omega L$. The negative sign here is simply due to the opposite direction of rotation of the negative sequence vectors and has no other special significance.

4.2 Proposed output power control strategy

4.2.1 Background

The instantaneous power balance between the *ac* side and the *dc* side gives rise to the following condition.

$$p_{in} = p_T + p_L \tag{4.5}$$

Here, p_{in} is the instantaneous power provided by ac supply, p_T is the instantaneous power consumed at the terminal of the converter and p_L is the instantaneous power absorbed / delivered by the inductors. In (4.5), p_L is non-zero in the unbalanced case even though the average power absorbed in the inductors is zero. In the input power control methods [48] and [49], the input power is controlled to be equal to a desired value P_{in}^*. The power condition equations in the input power control method are as follows.

$$\begin{cases} \overline{p}_{in} = P_{in}^* \\ \tilde{p}_{in} = 0 \\ \overline{q}_{in} = 0 \end{cases}, \tag{4.6}$$

where P_{in}^{*} is the desired average power at the supply input terminals, $\overline{p}_{in}$ is the constant portion (average) of the input power p_{in}, $\tilde{p}_{in}$ is the *ac* ripple portion of the input power with $p_{in} = \overline{p}_{in} + \tilde{p}_{in}$ and $\overline{q}_{in}$ is the constant portion (average) of the supply input reactive power. The choice of the power conditions in (4.6) has the important merit of being easily solvable in order to obtain the line current commands which satisfy them. However, as mentioned earlier, the output power of the rectifier (p_{dc}) will not be constant under unbalanced supply voltage conditions because of the non-zero instantaneous power (p_L) absorbed /delivered by the line inductances. This non-zero active power will result in ripple on the dc output voltage. The presence of ripple on the dc output voltage will reduce the life span of the dc link capacitor and degrade the control performance of dc load. In a typical wind turbine system [102], for example, the dc output voltage feeds a three phase inverter, whose output, in turn, controls the generator. The presence of the second order harmonic is known to affect the control performance of the generator significantly.

In order to overcome the above problem, ref. [51] has modified the conditions in (4.6) so as to keep the ripple power $\tilde{p}_T$ at the bridge input terminals zero instead of $\tilde{p}_{in}$ at the supply input terminals. This method aims to avoid the ripple power appearing at the output (assuming that the ripple power in the bridge rectifier is zero), while keeping the average reactive power at the supply input terminals zero. The power condition equations in [51, 52] are as follows.

$$\begin{cases} \overline{p}_{in} = P_{in}^{*} \\ \tilde{p}_T = 0 \\ \overline{q}_{in} = 0 \end{cases} \tag{4.7}$$

Here, $\tilde{p}_T$ is the *ac* ripple portion of the instantaneous rectifier bridge input power. As may be noted, the first and the third power condition equation are satisfied at the supply input terminals while the second condition is satisfied at the rectifier bridge input terminals, hence the name partial output power control (POPC) method in this work.

In [51], the current commands to fulfill the conditions in (4.7) were obtained by iteratively solving a set of highly nonlinear equations in each sampling interval which increases the complexity of implementation. On the other hand, ref. [52] has proposed solving (4.7) by assuming that the rectifier bridge input voltages are also known variables. However, as mentioned earlier, experimental results in both [51] and [52] show a considerable second harmonic ripple and also a significant steady-state error in the *dc* output voltage when operating with only a 15% magnitude unbalance in one phase.

4.2.2 Proposed control strategy

In the proposed method, the following set of power condition equations is assumed.

$$\begin{cases} \overline{p}_T = P_T^{*} \\ \tilde{p}_T = 0 \\ \overline{q}_T = 0 \end{cases} \tag{4.8}$$

Here, P_T^{*} is the desired average power at the rectifier bridge input terminals, $\overline{p}_T$

is the constant portion (average) of the rectifier bridge input power p_T and $\tilde{p}_T$ is the *ac* ripple portion with $p_T = \overline{p}_T + \tilde{p}_T$. The variable $\overline{q}_T$ is the constant portion (average) of the reactive power at the rectifier bridge input terminals. As may be noted, these equations are similar to those in (4.6), with the important distinction being that the power balance conditions now have to be satisfied *at the rectifier bridge input terminals* instead of *at the supply input terminals*. This avoids the ripple power appearing at the output (assuming that the ripple in the bridge power loss is negligible). Also, unlike the previously proposed control method in [51], the power conditions in (4.8) are easily solvable and the scheme can be implemented without requiring the rectifier input terminal voltages to be available.

The physical meaning of the first equation in (4.8) is that the instantaneous power at the rectifier bridge terminal is kept constant at the desired value P_T^*. During system operation, this value will be equal to the sum of the power delivered to the *dc* side and the losses in the power semiconductor switches of the rectifier. Thus, by regulating p_T to be constant, nearly constant power transfer to the *dc* side is achieved. It may be noted, however, that if power losses in the inductors are neglected, $\overline{p}_{in} = \overline{p}_T$ and the first equation in (4.8) is the same as the first equation in (4.6) & (4.7). An underlying meaning of the second equation in (4.8) is that the instantaneous power in the line inductances is provided by the ripple portion of the input power, that is $\tilde{p}_{in} = p_L$. The last equation in (4.8) indicates that, in the proposed method, the average reactive power is made to be zero at the rectifier bridge input terminals. This is the main difference between the methods in [48-52] and the present method. Thus, in the present method, no

attempt is made to enforce unity power factor operation at the *ac* input terminals.

The instantaneous active and reactive powers at the rectifier bridge input terminals are given below based on the definitions given in [70].

$$p_T = v_a i_a + v_b i_b + v_c i_c = \frac{3}{2}(v_\alpha i_\alpha + v_\beta i_\beta) \tag{4.9.1}$$

$$q_T = \frac{3}{2}(v_\beta i_\alpha - v_\alpha i_\beta) \tag{4.9.2}$$

With unbalanced supply voltages, the apparent power at the rectifier bridge input terminals is given by

$$S = \frac{3}{2}\vec{v}\vec{i}^{\,*} = p_T + jq_T = \frac{3}{2}(v_\alpha i_\alpha + v_\beta i_\beta) + j\frac{3}{2}(v_\beta i_\alpha - v_\alpha i_\beta). \tag{4.10}$$

Substituting expressions of the voltage space vector $\vec{v}$ and the current space vector $\vec{i}$ using (4.2) into (4.10), the instantaneous active and reactive power can be expressed as

$$p_T(t) = \overline{p}_T + p_{Tc}\cos(2\omega t) + p_{Ts}\sin(2\omega t) \tag{4.11.a}$$

$$q_T(t) = \overline{q}_T + q_{Tc}\cos(2\omega t) + q_{Ts}\sin(2\omega t), \tag{4.11.b}$$

where p_{Tc} , q_{Tc}, p_{Ts} and q_{Ts} are the coefficients of the second order harmonic ripple components of the active and reactive power.

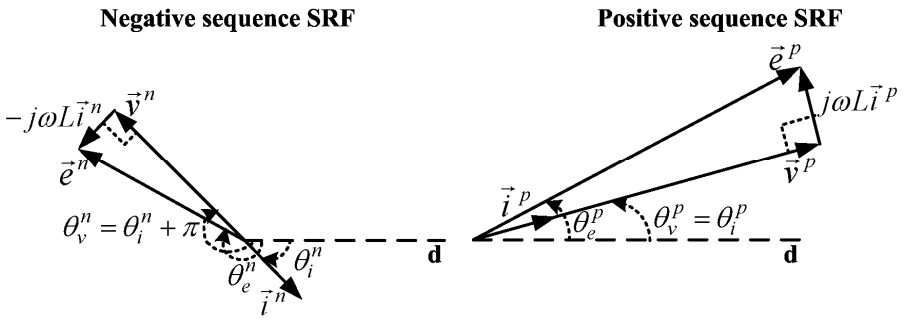


Fig. 4.4 Phasor diagram of the output power control method

Expressing the power coefficients in matrix form, we have the following power condition equation.

$$\begin{bmatrix} \frac{2}{3}P_T^* \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} v_d^p & v_q^p & v_d^n & v_q^n \\ -v_q^p & v_d^p & -v_q^n & v_d^n \\ v_d^n & v_q^n & v_d^p & v_q^p \\ v_q^n & -v_d^n & -v_q^p & v_d^p \end{bmatrix} \begin{bmatrix} i_d^{p*} \\ i_q^{p*} \\ i_d^{n*} \\ i_q^{n*} \end{bmatrix} \tag{4.12}$$

The solution to (4.12) is

$$\begin{bmatrix} i_d^{p*} \\ i_q^{p*} \\ i_d^{n*} \\ i_q^{n*} \end{bmatrix} = \frac{2P_T^*}{3D} \begin{bmatrix} v_d^p \\ v_q^p \\ -v_d^n \\ -v_q^n \end{bmatrix}, \tag{4.13}$$

where $D = [(v_d^p)^2 + (v_q^p)^2 - (v_d^n)^2 - (v_q^n)^2] = (v^p)^2 - (v^n)^2$.

Eq. (4.13) also indicates that

$$\vec{i}^{\,p*} = k\vec{v}^{\,p}, \quad \vec{i}^{\,n*} = -k\vec{v}^{\,n} \quad \text{and} \quad \frac{i^{p*}}{v^p} = \frac{i^{n*}}{v^n} = k \tag{4.14}$$

with $k=2P_T^*/3D$. The condition, $v^p > v^n$, is assumed here.

The solution in (4.13) is of the same form as that in [49] with the rectifier bridge input voltages replacing the supply input voltages. Thus, (4.13) assumes that the voltages at the rectifier bridge input terminals are known variables. However, these voltages are not smooth but include a very large switching ripple due to the operation of the switches in the rectifier. Also, in order to implement the dual current control scheme for the inner current loop as in [49], the input supply voltages are required to be measured anyhow (see Fig. 4.5). Thus, it is preferable to express (4.13) in terms of supply input voltages rather than rectifier bridge input voltages. This is done as follows.

The phasor diagrams shown in Fig. 4.4 are constructed by using the relationships given by (4.3), (4.4) and (4.14). As shown in the figure, both the positive and the negative sequence components form their triangles counter-clockwise. Since the two triangles are geometrically similar, we may write

$$\frac{i^{p*}}{e^p} = \frac{i^{n*}}{e^n} = k_1 \quad . \tag{4.15}$$

Based on (4.13) and the phasor diagram in Fig. 4.4, the variable i_d^p can be expressed as given below.

$$i_d^{p*} = k v_d^p = k v^p \cos\theta_v^p \tag{4.16}$$

Here, as shown in Fig. 4.4, v^p is related to e^p by the equation $v^p = e^p \cos(\theta_e^p - \theta_v^p)$. The following trigonometric relationships can be shown to be true.

$$\cos\theta_v^p = \cos(\theta_e^p - \theta_v^p - \theta_e^p) = \cos(\theta_e^p - \theta_v^p)\cos\theta_e^p + \sin(\theta_e^p - \theta_v^p)\sin\theta_e^p \tag{4.17.a}$$

$$e_d^p = e^p \cos\theta_e^p \quad \text{and} \quad e_q^p = e^p \sin\theta_e^p \tag{4.17.b\&c}$$

$$\sin(\theta_e^p - \theta_v^p) = \omega L k_1 \text{ and } \cos^2(\theta_e^p - \theta_v^p) = 1 - (\omega L k_1)^2 \tag{4.17.d\&e}$$

$$\cos(\theta_e^p - \theta_i^p) = \cos(\theta_e^p - \theta_v^p) = \frac{k_2}{k_1} \tag{4.17.f}$$

with $k_2 = 2p_{dc}/3[(e^p)^2 - (e^n)^2]$.

Using the above relationships and (4.16), i_d^{p*} can be written as

$$i_d^{p*} = k_2 e_d^p + k_1^2 \omega L e_q^p \tag{4.18}$$

with $k_2 = 2p_{dc}/3[(e^p)^2 - (e^n)^2]$.

The other input current variables can be obtained in a similar manner. The final equations for the input currents can be shown to be

$$\begin{cases} i_d^{p*} = i^p \cos\theta_i^p = k_2 \cdot e_d^p + k_1^2 \omega L \cdot e_q^p \\ i_q^{p*} = i^p \sin\theta_i^p = k_2 \cdot e_q^p - k_1^2 \omega L \cdot e_d^p \\ i_d^{n*} = i^n \cos\theta_i^n = -k_2 \cdot e_d^n - k_1^2 \omega L \cdot e_q^n \\ i_q^{n*} = -i^n \sin\theta_i^n = -k_2 \cdot e_q^n + k_1^2 \omega L \cdot e_d^n \end{cases}, \tag{4.19}$$

where k_1 and k_2 are as defined in (4.15) and (4.18).

Combining (4.17.e) and (4.17.f), parameter k_1 can be related to the other parameters as given below.

$$k_1^2 = (1 - \sqrt{1 - 4\omega^2 L^2 k_2^2}) \big/ 2\omega^2 L^2 \tag{4.20}$$

In the proposed output power control scheme, given the desired *dc* output

power P_T^*, eq. (4.19) determines the values of the four current commands to be set. Each component of the current commands in (4.19) has two parts, one proportional to the corresponding voltage component and the other proportional to the corresponding orthogonal voltage component. The first term contributes to the constant power portion of the input power required by the *dc* load while the second term contributes to the oscillatory power in the inductors. The first term in each current component in (4.19) is the complete solution in the case of the input power control method in [49]. Therefore, it can be seen that the present method accounts for the ripple power in the inductors thereby ensuring that constant output power is delivered.

4.2.3 Control Scheme

The overall control block diagram of the proposed scheme is shown in Fig. 4.5. The overall scheme may be seen to be similar to those in [49] & [51]. The differences in the schemes arise mainly due to the approach taken in implementation of the current commands generation block as mentioned in the previous section. Here, the output of the voltage controller forms the average rectifier bridge input power reference, P_T^* which is used to generate the current commands for the inner current loops as per (4.19). The dual current controller in [49] is made use of to regulate the positive and negative sequence currents separately in their corresponding reference frames.

As pointed in [49], one major advantage of the dual current controller is that all the variables become time-invariant in their corresponding frames. Also, cross-coupling compensation from the corresponding orthogonal axis is introduced as shown in Fig. 4.5 to improve the tracking capacity of the current regulator**.** In [22], analytical expressions

for calculating the gains and the time constants of both the inner current controllers and the outer voltage controller are derived. The PI control design method used in [22] is generally followed in the design of the controllers here**.**

In the proposed control scheme, the implementation of (4.19) requires that the unbalanced three-phase variables be separated into positive and negative sequence *d* and *q* components in real time. In our scheme, the simple sequence separation schemes used in [49] and [51] have been adopted. Other detection methods, besides the time delaying method [51] and notch filter method [49], have also been proposed earlier to carry out this separation in [50, 71-73]. In [71], positive sequence symmetrical component and its phase angle have been estimated by recursive mean which may cause measurement

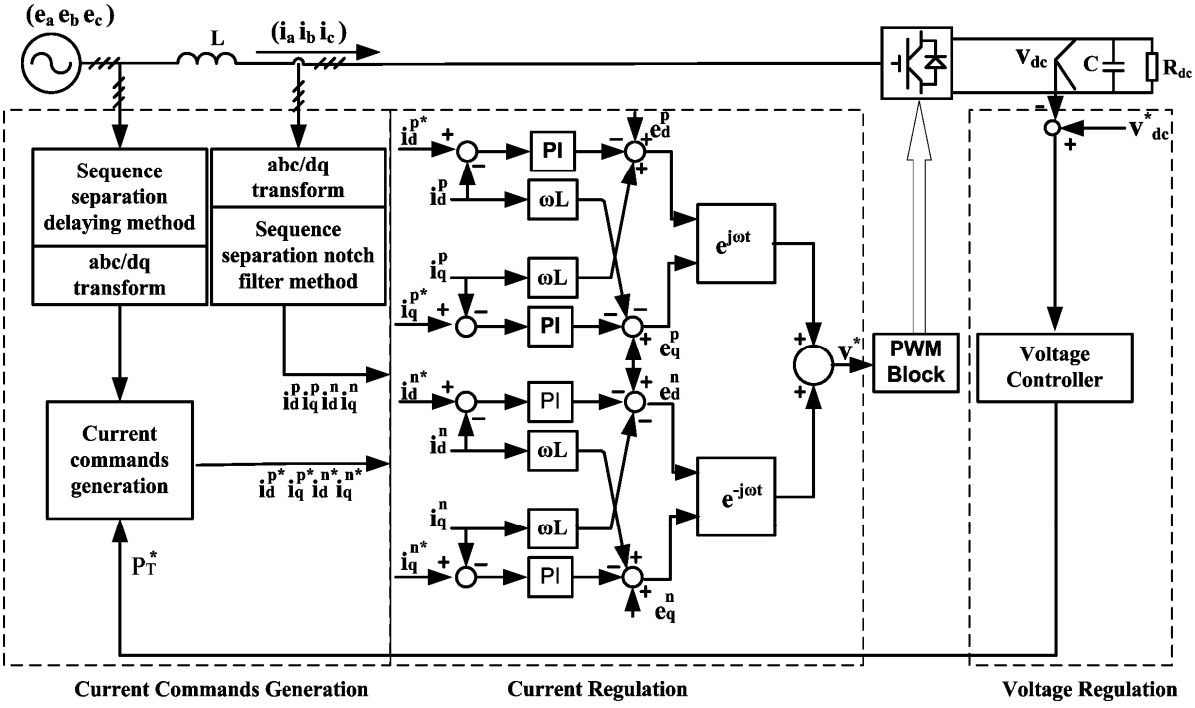


Fig. 4.5 Overall detailed control block diagram of the proposed scheme

and phase delays as mentioned in [73]. In [72], the amplitude and angle information in a single phase system and a three-phase four wire system has been obtained using only

two sampled values with a short data time window. However, as the relationships among three-phase variables are neglected [73], the scheme may not be applicable to a three-phase three wire system. Song *et al.* [73] proposed instantaneous phase angle detection method under unbalanced conditions using the weighted least-squares estimation method. The sequential components may also be obtained without almost a delay using the method in [73]. However, the method needs complex algorithms and is not simple to implement. This scheme can be adopted if accurate instantaneous sequential components detection is absolutely necessary. Notch filter method proposed in [50] again by Song *et al.* is a fast and simple though relatively inaccurate method to extract the sequential components. It has been also successfully used to obtain the sequential components of the line currents in [49, 50].

In the control scheme shown in Fig. 4.5, sequential components of both supply voltages and line currents are needed to be separated. The sequential components of supply voltages are necessary for calculation of current commands in the feed-forward loop whereas the sequential components of line currents are necessary for separation of positive- and negative-sequences of the *d*-axis and *q*-axis actual current components in the feedback loop. Therefore, the main requirement for voltage sequential components separation is accuracy. On the other hand, the main requirement for current sequential components separation is speed of response.

Time delaying method proposed in [51] is an effective method to extract the sequential components without steady-state error. However, in carrying out this separation, a time delay of at most one-third of the fundamental period will be

introduced. Such a time delay will cause instability if the method is employed in the current feedback loops to separate the positive and negative *d* and *q* components of the actual line current. On the other hand, the notch filter method proposed in [49] is a fast and simple though relatively inaccurate method to extract the sequential components. However, if this method is used in the current commands generation loops, inaccuracy of the current commands may occur. Therefore, in our scheme, instead of using one single sequence components separation scheme to carry out both separations, the delaying method is used for accurately calculating the sequence components of the supply voltage in the feed-forward loop whereas the notch filter method is used to determine in real-time the sequential current components in the feedback loop.

4.2.4 Theoretical vector power factor with the output power control method

The vector power factor is defined in [7] as follows.

$$P_{FV} = \frac{P}{S_V}, \tag{4.21}$$

where S_V is the vector apparent power with $S_V = |P+jQ|$. Variable P is the total active power and variable Q is the total reactive power. The total active power and total reactive power at the supply input terminals of the rectifier with instantaneous reactive power regulation scheme are given by

$$\begin{cases} P_{in} = \frac{3}{2} e^p i^p \cos(\theta_e^p - \theta_i^p) + \frac{3}{2} e^n i^n \cos(\theta_e^n - \theta_i^n) \\ \overline{q}_{in} = -\frac{3}{2} e^p i^p \sin(\theta_e^p - \theta_i^p) + \frac{3}{2} e^n i^n \sin(\theta_e^n - \theta_i^n) \end{cases}, \tag{4.22}$$

As mentioned earlier, positive sequence triangle and negative sequence triangle are geometrically similar as shown in Fig. 4.4. Thus, the following relationship can be shown to be true.

$$\theta_e^p - \theta_i^p = \theta_i^n - \theta_e^n + \pi \tag{4.23.a}$$

Accordingly, following relationships hold

$$\begin{cases} \cos(\theta_e^p - \theta_i^p) = -\cos(\theta_e^n - \theta_i^n) \\ \sin(\theta_e^p - \theta_i^p) = \sin(\theta_e^n - \theta_i^n) \end{cases} \tag{4.23.b}$$

The vector power factor for the output power control scheme proposed earlier can be obtained by substituting (4.22) and (4.23.b) into (4.21):

$$P_{FV} = \cos(\theta_e^p - \theta_i^p) \tag{4.24}$$

The (vector) power factors obtained with the IPC method in [48] and [49] and the POPC method in [51] and [52] are both always unity. With the proposed OPC method, on the other hand, the vector power factor equals $\cos(\theta_e^p - \theta_i^p)$ and is not unity on account of the reactive power consumed by the inductors. As may be seen from Fig. 4.4, this factor will depend on the value of the inductances and will typically be very nearly unity. For example, even if we consider that the voltage drop across the inductor is equal to a high value of 10% of the phase voltage, it can be shown that

$$\cos(\theta_e^p - \theta_i^p) = 0.995, \tag{4.25}$$

which is almost unity. Thus, the power factor obtained with the output power control method is very high.

4.3 Experimental results

The proposed control scheme was implemented on a dSPACE DSP system (DS1104), which uses a floating processor MPC8240 as the main processor, and a TMS320F240 motion control DSP as an interface with the power converter. Experimental verification was done on a 1 kW PWM rectifier built for this purpose. The system parameters are: L = 4.15 mH, R = 0.27 Ω, C = 136 μF, R_{dc} = 45 Ω and f = 10 kHz for both switching frequency and sampling frequency. The supply frequency was 50 Hz and the *dc* output voltage was regulated at 200 V for both balanced and unbalanced cases. The control scheme shown in Fig. 4.5 was employed. In the current controller design, the resistance of the inductors, R, was also taken into account. The PI parameters for the current loop were designed such that the bandwidth of the current control loop was 400 Hz which is high enough for *d*- and *q*-axes currents regulation. The proportional gain and the integral gain were chosen to be 10.4 and 678, respectively. The supply voltages and the line currents in two of the three phases were measured in the experimental set up. The delaying method was used to obtain the sequence components of the supply voltage for calculating the current commands while a faster notch filter based approach was employed to determine the current sequence components from line currents for use in the current feedback loops.

The experimental waveforms under balanced conditions with the proposed control scheme are shown in Fig. 4.6. The three-phase supply voltage was set as 60V (RMS). Fig. 4.6 shows the *dc* output voltage v_{dc} and the three line currents i_a, i_b and i_c. As shown in the figure, the three-phase currents are balanced and the output voltage is almost

ripple-free. The measured total harmonic distortion (THD) for the three line currents are 2.3%, 2.15%, 2.4%, respectively. The maximum peak to peak ripple voltage in the *dc* output voltage measured in the experiment results was 2V. As expected, in the balanced case, the line currents were found to be in phase with the corresponding phase voltages as also shown in Fig. 4.7. Thus, the experimental results establish that the proposed method works very well under normal balanced supply voltage conditions.

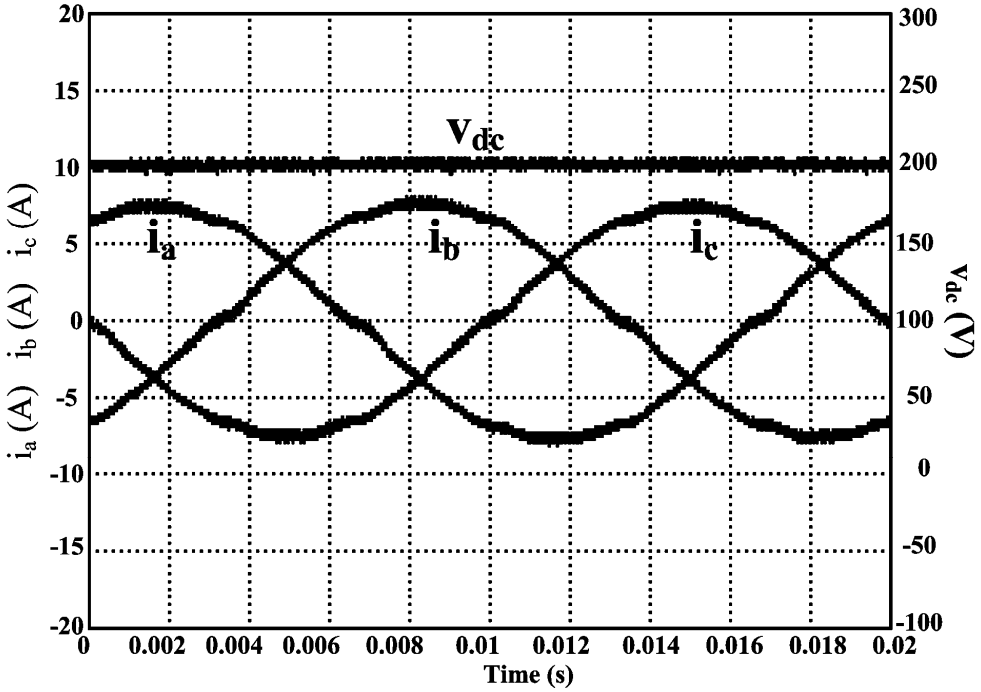


Fig. 4.6 Experimental waveforms of three-phase currents and *dc* output voltage under balanced supply - Proposed output power control method

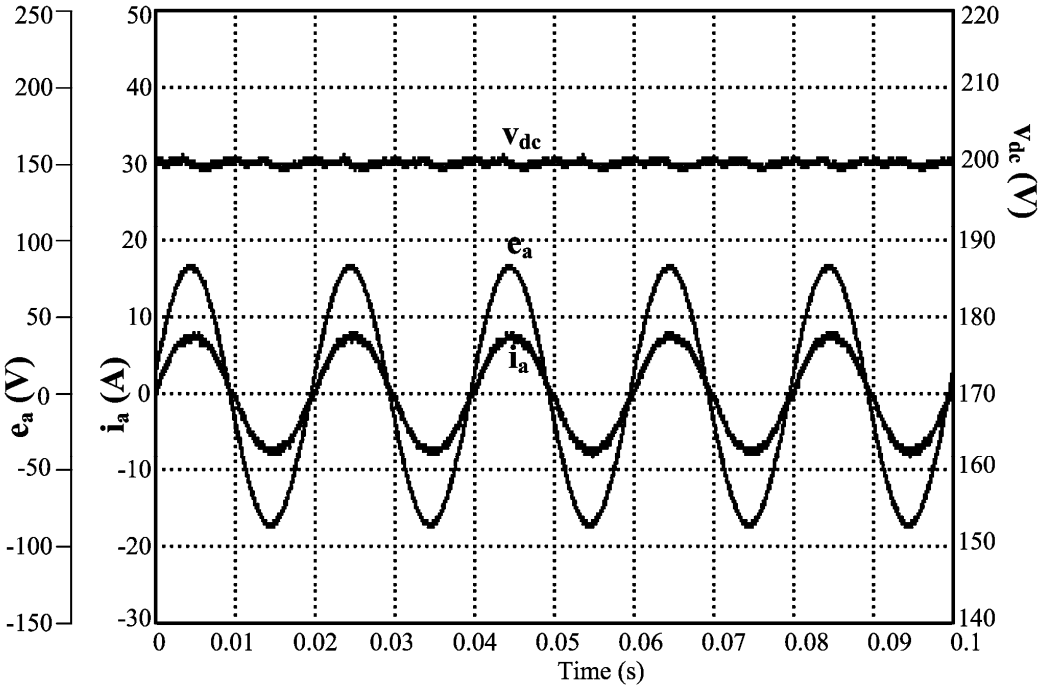


Fig. 4.7 Experimental waveforms of a-phase current, a-phase supply voltage and zoomed *dc* output voltage under balanced supply - Proposed output power control method

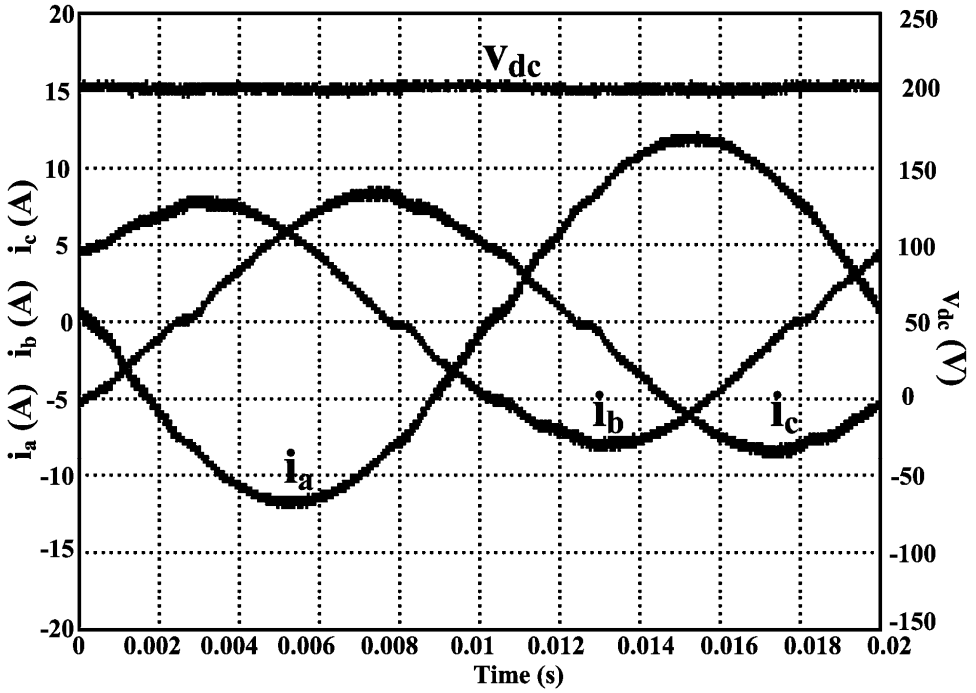


Fig. 4.8 Experimental waveforms of three-phase currents and *dc* output voltage under unbalanced supply - Proposed output power control method

The experimental results under unbalanced conditions with the proposed method are shown in Fig 4.8. The supply voltages for the experiments were set at $42\sqrt{2}\sin(\omega t + 355^\circ)$ V, $75\sqrt{2}\sin(\omega t + 236^\circ)$ V and $66\sqrt{2}\sin(\omega t + 90^\circ)$ V. These values correspond to a positive sequence voltage of around 60 V (RMS) at a phase of -13^o and a negative sequence voltage of around 20 V (RMS) at a phase of 148^o, resulting in an unbalance ratio of around 33% (negative sequence voltage magnitude to positive sequence voltage magnitude). The current waveforms, though unbalanced as expected, are nearly sinusoidal, while the *dc* output voltage is nearly constant with low ripple. The measured THD for the three line currents were 2.02%, 4.95%, 4.95%, respectively. The maximum peak to peak ripple voltage in the output voltage measured in the experiment results was 4.2 V. The *dc* output voltage should theoretically be ripple-free. The voltage ripple on the *dc* output voltage can be attributed to the switching action as well as the presence of ESR of the *dc* capacitor. It is not easy to directly calculate VPF value from (4.22) as fairly involved computations on variables (θ_e^p θ_i^p) are required. The VPF was calculated using (4.17.f) to be 0.992, which is close to unity.

Fig. 4.9 shows transient responses of three-phase currents and *dc* output voltage under the same unbalanced operating conditions with the proposed method for a step change in the load from 90Ω to 60Ω and back to 90Ω. Fig.4.10 shows the experimental waveforms of the three-phase currents and the *dc* output voltage under step change from normal balanced operating condition to unbalanced operating conditions. Here, the three-phase supply voltage was changed in a step fashion from 60V (RMS) each phase under balanced operating conditions to $42\sqrt{2}\sin(\omega t + 355^\circ)$ V, $75\sqrt{2}\sin(\omega t + 236^\circ)$ V

and $66\sqrt{2}\sin(\omega t + 90^\circ)$ V under unbalanced operating conditions. A 1500VA/phase *ac* power supply/analyzer equipment (HP 6834B) was used to produce this voltage step change. It can be seen from Fig. 4.9 and Fig. 4.10 that both the responses for step changes in loads and the transition from normal to unbalanced grid operation are quite fast and very smooth.

Thus, the experimental results clearly show that the main objectives of the proposed scheme have been achieved - sinusoidal line currents, constant *dc* power transfer to the *dc* side resulting in low *dc* output voltage ripple, near unity vector input power factor and ability to handle transient situations - all under unbalanced supply voltage conditions.

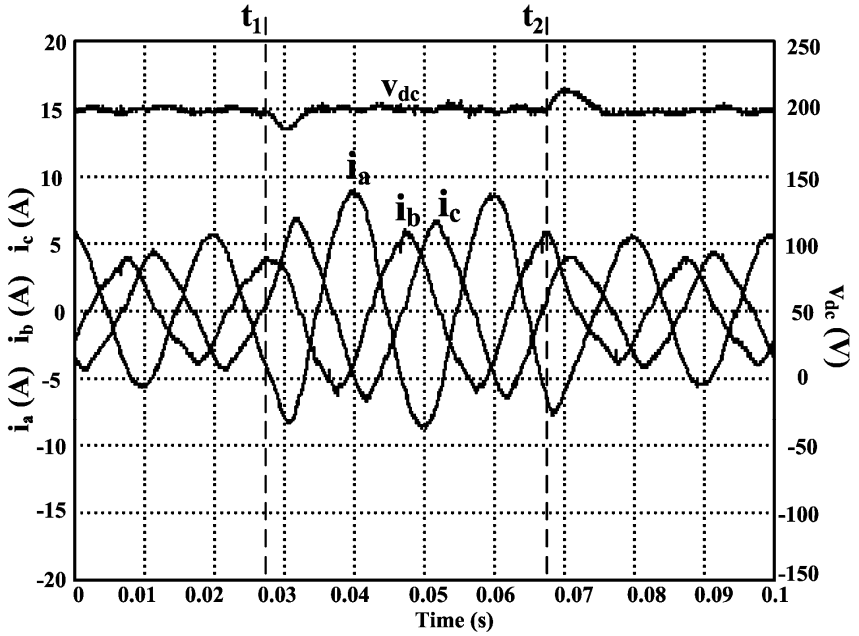


Fig. 4.9 Experimental waveforms of three-phase currents and *dc* output voltage under unbalanced operating conditions for a step change in load from 90Ω to 60Ω and back to 90Ω

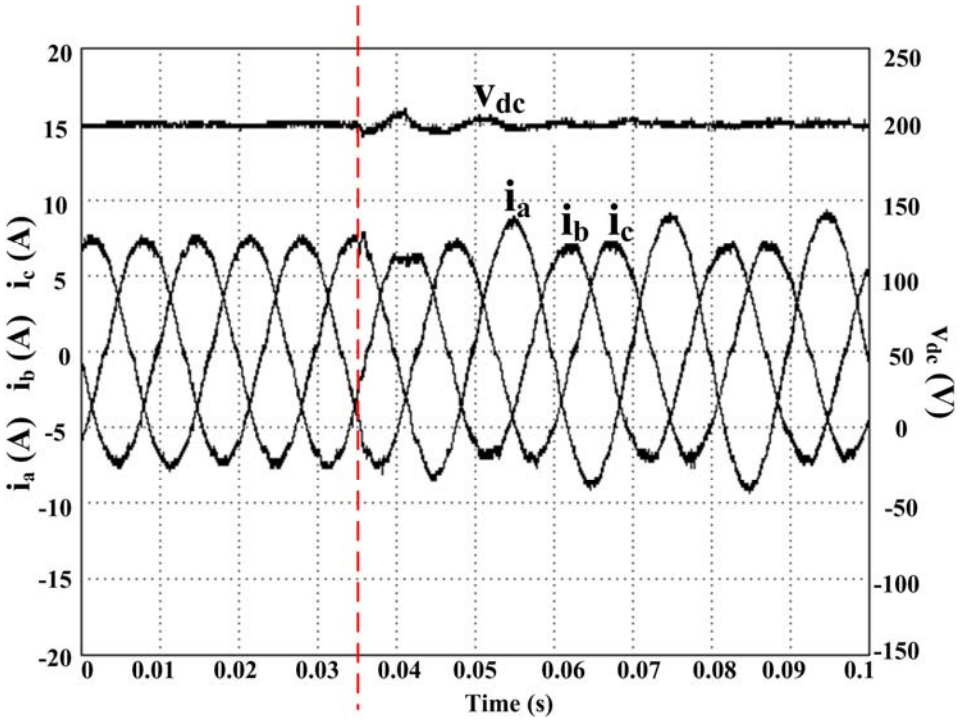


Fig. 4.10 Experimental waveforms of three-phase currents and *dc* output voltage under a step change of supply voltage from normal balanced operating conditions to unbalanced operating conditions

4.4 Conclusions

An output power control method was proposed in this chapter to improve both the input and output performance of a PWM rectifier system under unbalanced operating conditions. With the proposed method, simple closed form solutions for the current commands are obtained while maintaining a desired constant *dc* output voltage under steady-state. Experimental results obtained with a 1 kW laboratory prototype have verified the effectiveness of the proposed output power control method.

However, the power factor is not directly regulated in this method. It is found that even though the obtained vector power factor with the output power control method is very high, it is still not unity. As partial output power control method can theoretically achieve both *dc* output voltage regulation and unity power factor operation, further

investigations were carried out to find out the possible reasons for the poor performance for this method reported in the literature. The results of these investigations are reported in the next chapter.

CHAPTER 5

IMPLEMENTATION ISSUES IN PARTIAL OUTPUT POWER CONTROL STRATEGY

5.0 Introduction

The output power control (OPC) method proposed in Chapter 4 can provide very good input and output performance simultaneously for a PWM rectifier system under unbalanced operating conditions. However, in this method, as pointed out in Section 4.2.4, the power factor is not directly regulated. It is found that even though the obtained vector power factor (VPF) with the OPC method is very high, it is still not unity.

Unity power factor operation can be theoretically achieved by maintaining zero reactive power at supply input terminals instead of at the rectifier bridge input terminals. This results in the method previously proposed in [52]. In this method, the active power (constant portion plus the ripple portion) is regulated at the rectifier bridge input terminals whereas the average reactive power is regulated at the supply input terminals. As the power quantities are partially regulated at the output terminals, this method has been named here as *partial output power control* (POPC) method. This control method can, in principle, maintain nearly constant *dc* output voltage and sinusoidal line currents at unity VPF as desired.

However, as mentioned in Chapter 4, the experimental results provided in [52] show a considerable second harmonic ripple and also an observable steady-state error in

the *dc* output voltage when operating with a low 15% magnitude imbalance in one of the phases. Simulations and experimental results carried out as part of the current work (shown in the latter part of the present chapter) have also confirmed the existence of this problem.

This chapter presents the results obtained from the investigations carried out with the aim of overcoming the performance limitations observed with the POPC method. In the implementation of the POPC method, the rectifier input voltage is estimated through the use of dc output voltage and switch control signals. As will be shown in this chapter, such an approach introduces an additional feedback loop in the system. Essentially, the effect of the additional loop on the performance is not known. It is suspected, however, that this additional unintended feedback loop is the root cause of the POPC scheme's poor performance.

However, difficulties were encountered in carrying out theoretical investigations of the POPC method in order to resolve this problem. Hence, the issue of estimating the rectifier bridge input voltage was first studied with regard to the simpler OPC method proposed in Chapter 4.

As may be seen from (4.13), the bridge rectifier input voltages are required to be known in the case of the OPC method also. However, in Chapter 4, this issue is bypassed through the use of the fact that the positive sequence triangle and the negative sequence triangle in the phasor diagram (Fig. 4.4) are geometrically similar. This leads to the current references for the OPC being determined by (4.19), which requires only the *ac* input voltages to be known. In the case of the POPC scheme, the positive

sequence and the negative sequence triangles are not similar (see Fig. 6.4) and hence this approach can not be taken.

In order to investigate the issues with regard to the estimation of the bridge rectifier input voltage, two additional implementations of the OPC scheme are introduced and investigated. The first method is through the estimation of the rectifier bridge input terminal voltage by using the *dc* output voltage together with switching function signals. This approach is similar to that in [52] for the POPC method. This method of estimating the bridge input voltage has been named 'Estimation Method 1'. It is shown that using Estimation Method 1 results in an unintended, additional feedback loop in the compensated system (see Fig. 5.1 - Fig. 5.3) in the OPC scheme and this largely degrades the robustness of the system stability. Next, the bridge input voltage was estimated ('Estimation Method 2') by using the *ac* input voltage together with the inductor voltage drop. It is shown that this method of implementing the OPC scheme has largely improved the robustness of the system stability.

This result suggests that the reason for the poor performance in the case of the POPC method may also be linked, in a similar manner, to the manner in which the rectifier bridge input terminal voltages are estimated. Based on this insight, the POPC method was implemented with the rectifier bridge input voltage being determined by Estimation Method 2 instead of the earlier Estimation Method 1. The performance of the POPC method was significantly improved with this implementation as verified using both simulation and experimental approaches.

5.1 Analysis of different implementation methods of the OPC method

In this section, two additional implementation methods of the OPC method proposed in Chapter 4 are presented. These two methods involve different ways of estimating the bridge rectifier input voltage. The resulting system stabilities are also analyzed.

5.1.1 Background

It was noted that in Chapter 4, the current commands can be expressed as a function of rectifier bridge input voltages (4.13) as given below.

$$\begin{bmatrix} i_d^{p*} \\ i_q^{p*} \\ i_d^{n*} \\ i_q^{n*} \end{bmatrix} = \frac{2P_T^*}{3D} \begin{bmatrix} v_d^p \\ v_q^p \\ -v_d^n \\ -v_q^n \end{bmatrix}, \tag{5.1}$$

However, as discussed in Chapter 4, the rectifier bridge input voltages are not smooth but contain a very large switching ripple due to the operation of the switches in the rectifier. Also, in order to implement the dual current control scheme for the inner current loop as in [49], the input supply voltages are required to be measured (see Fig. 4.5). Therefore, direct relationship between current references and supply input voltages has been established in Chapter. 4.

Due to this, the current commands are directly calculated from supply input voltage (4.19) in Chapter 4.

$$\begin{cases} i_d^{p*} = k_2 \cdot e_d^p + k_1^2 \omega L \cdot e_q^p \\ i_q^{p*} = k_2 \cdot e_q^p - k_1^2 \omega L \cdot e_d^p \\ i_d^{n*} = -k_2 \cdot e_d^n - k_1^2 \omega L \cdot e_q^n \\ i_q^{n*} = -k_2 \cdot e_q^n + k_1^2 \omega L \cdot e_d^n \end{cases}, \tag{5.2}$$

with $k_1^2 = (1 - \sqrt{1 - 4\omega^2 L^2 k_2^2}) \big/ 2\omega^2 L^2$ and $k_2 = 2P_T^* / 3[(e^p)^2 - (e^n)^2]$.

Thus the current references of the proposed OPC method in (5.2) require only the supply input voltages to be sensed. This is a consequence of the simple geometrical relationship that exists between the line currents, supply input voltages and rectifier bridge input voltages as illustrated in Fig. 4.4. In this way, the requirement of estimating rectifier bridge voltages is totally avoided.

The POPC method also requires the rectifier bridge voltage to be sensed. However, in this case, simple geometrical relationship does not exist between currents, supply input voltages and rectifier bridge input voltages. The positive sequential triangle is not geometrically similar to the negative sequential triangle. Thus, the methods used in Chapter 4 can not be adopted directly in the case of POPC method.

In the following subsection, instead of calculating current commands using (4.19) & (5.2), two additional methods for calculating the rectifier bridge input voltages will be introduced and analyzed.

5.1.2 Estimation of the rectifier bridge input voltages

The rectifier bridge input voltage signals can be estimated either from output *dc* voltage together with switch functions (Estimation Method 1) or supply input voltages

together with inductor voltages (Estimation Method 2).

When Estimation Method 1 is used, the rectifier bridge input voltages can be obtained by using (2.2) of Chapter 2.

$$\bar{v}_m = \frac{(\bar{u}+1)\cdot v_{dc}}{2} \tag{5.3}$$

Here, $\bar{u} = [u_a \quad u_b \quad u_c]^T$ are the averaged switching functions in *a-b-c* frame. Also, $\bar{v}_m = [v_{am} \quad v_{bm} \quad v_{cm}]^T$, $\bar{v}_n = \bar{v}_m + v_{mn}$ and $v_{mn} = -\frac{1}{3}(v_{am} + v_{bm} + v_{cm})$ with $e_{an} + e_{bn} + e_{cn} = 0$.

The rectifier bridge input voltages in both the positive- and negative- sequences synchronously rotating frame can be obtained using the transformation (see (B.5), (B.8) and (B.10)) presented in Appendix B and can expressed as follows.

$$\begin{cases} v_d^p = u_d^p \frac{v_{dc}}{2} \\ v_q^p = u_q^p \frac{v_{dc}}{2} \\ v_d^n = u_d^n \frac{v_{dc}}{2} \\ v_q^n = u_q^n \frac{v_{dc}}{2} \end{cases} \tag{5.4}$$

Ignoring the dead time effect and voltage drop in the switching devices, $[v_d^p \; v_q^p \; v_d^n \; v_q^n]$ can be replaced by $[v_d^{p*} \; v_q^{p*} \; v_d^{n*} \; v_q^{n*}]$ which are the control signals to the rectifier, as shown in Fig. 5.1.

When Estimation Method 2 is used, the rectifier bridge input voltages can be reconstructed as given below.

$$\begin{cases} v_d^p = e_d^p + \omega L i_q^p \\ v_q^p = e_q^p - \omega L i_d^p \\ v_d^n = e_d^n - \omega L i_q^n \\ v_q^n = e_q^n + \omega L i_d^n \end{cases} \tag{5.5}$$

Here, the voltage drops in the parasitic resistors of the inductors are neglected. Instead of using (5.2) for current reference calculation, (5.4) or (5.5) can be substituted into (5.1) to generate current reference signals.

5.1.3 Implementation of OPC method using Estimation Method 1

In this subsection, the implementation of the OPC method by using Estimation Method 1 will be investigated. In particular, the introduction of an extra loop in the generation of current commands will be studied and its influence on the overall system stability robustness investigated.

5.1.3.1 Simplification of the subsystem

Fig. 5.1 illustrates the detailed closed-loop subsystem for a PWM rectifier in the positive sequence SRF with the OPC method. This subsystem is slightly different from the one shown in Fig. 4.5 as discussed below.

In the actual implementation, the *d*-axis and *q*-axis control signals were transformed into *a*-*b*-*c* frame to generate the three-phase PWM control signals. The three-phase currents regulated by these PWM signals are then transformed from *a*-*b*-*c* frame back to *d*-*q* frame as shown in Fig. 4.5. In the present analysis, the *abc*-*dq* transformation and the subsequent inverse *abc*-*dq* transformation are omitted in the modeling as they effectively cancel each other.

The PWM rectifier is modeled in the independent positive- and negative- sequence SRFs as shown in Fig. 5.1. The control signals (v_d^{p*}, v_q^{p*}) have twofold functions. One of the functions is to generate the switching function signals for controlling the rectifier bridge. The other function is to calculate current reference as follows:

$$i_d^{p*} = kv_d^{p*} \quad \text{and} \quad i_q^{p*} = kv_q^{p*}, \tag{5.6}$$

where $k=2P^*_T/3D$ with $D = [(v_d^p)^2 + (v_q^p)^2 - (v_d^n)^2 - (v_q^n)^2] = (v^p)^2 - (v^n)^2$. Here, P^*_T denotes the power reference at the rectifier bridge terminal. This reference is the output of the voltage loop controller not shown in Fig. 5.1.

The control signals (v_d^{p*}, v_q^{p*}) and the controlled positive sequence rectifier bridge input voltages (v_d^p, v_q^p) are assumed to be equal to each other as indicated in Fig. 5.1 by the rectangles marked with dashed lines. Here, $G_i(s)$ is the system transfer function with $G_i(s) = 1/(Ls+R)$ and $G_c(s)$ is the current controller transfer function with $G_c(s) = k_p + k_i/s$.

Please note in Fig.5.1 that there are two closed loops in one subsystem, e.g., *d*-axis positive sequence SRF system: the basic feedback control loop and the additional unintended positive feedback loop. The basic feedback control loop starts with the error signal feeding to the current controller $G_c(s)$ and also includes the PWM unit and the plant $G_i(s)$. The additional unintended positive feedback loop refers to the current reference generation loop. Here, the current reference is obtained from the control signals (v_d^{p*}, v_q^{p*}).

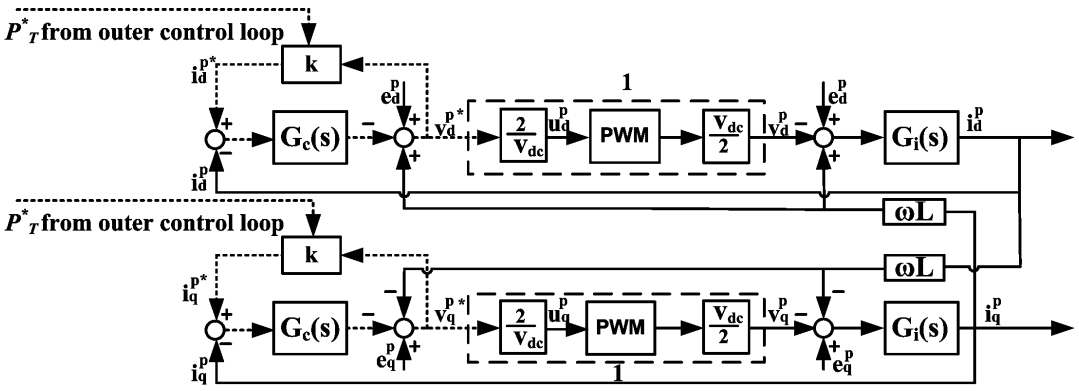


Fig. 5.1 Detailed closed-loop subsystem for a PWM rectifier in the positive sequence SRF - OPC scheme using Estimation Method 1

As shown in Fig. 5.1, the control signals v_d^{p*} and v_q^{p*} can be written as follows

$$\begin{cases} v_d^{p*} = e_d^p + \omega L i_q^p - (k_p + \dfrac{k_i}{s})(i_d^{p*} - i_d^p) \\ v_q^{p*} = e_q^p - \omega L i_d^p - (k_p + \dfrac{k_i}{s})(i_q^{p*} - i_q^p) \end{cases} . \tag{5.7}$$

On the other hand, the currents can be obtained from Fig. 5.1 as given below.

$$\begin{cases} i_d^p = \dfrac{e_d^p + \omega L i_q^p - v_d^p}{Ls + R} \\ i_q^p = \dfrac{e_q^p - \omega L i_d^p - v_q^p}{Ls + R} \end{cases} \tag{5.8}$$

The supply voltages and the coupling terms from *d*-axis or *q*-axis in the model can be cancelled out by the decoupling control and feed-forward control in the control signals given in (5.7).

By substituting (5.7) into (5.8) and replacing $G_i(s) = 1/(Ls+R)$ and $G_c(s) = k_p + k_i/s$ with $k_p = 2\pi fL$ and $k_i = 2\pi fR$ in both equations, we have

$$\begin{cases} \dfrac{i_d^{p*}}{i_d^p} = \dfrac{G_c(s)G_i(s)}{1+G_c(s)G_i(s)} = T(s) \\ \dfrac{i_q^{p*}}{i_q^p} = \dfrac{G_c(s)G_i(s)}{1+G_c(s)G_i(s)} = T(s) \end{cases} \tag{5.9}$$

The closed-loop loop-transfer function is *T(s)* which can be written as $T(s) = \dfrac{G_c(s)G_i(s)}{1+G_c(s)G_i(s)} = \dfrac{1}{\tau s+1}$ with $\tau=1/2\pi f$. Here, variable f denotes the cut-off frequency of the current controller.

Based on the above, the subsystem shown in Fig. 5.1 can be simplified further into Fig. 5.2. In Fig. 5.2, control signals (v_d^{p*} v_q^{p*}) constructed based on (5.7) are used for current reference generation.

Please note that the basic control loop in Fig. 5.2 starts with the current error signals and includes controller $G_c(s)$ and plant $G_i(s)$. The additional unintended feedback loop due to current reference generation shows up in Fig. 5.2 also.

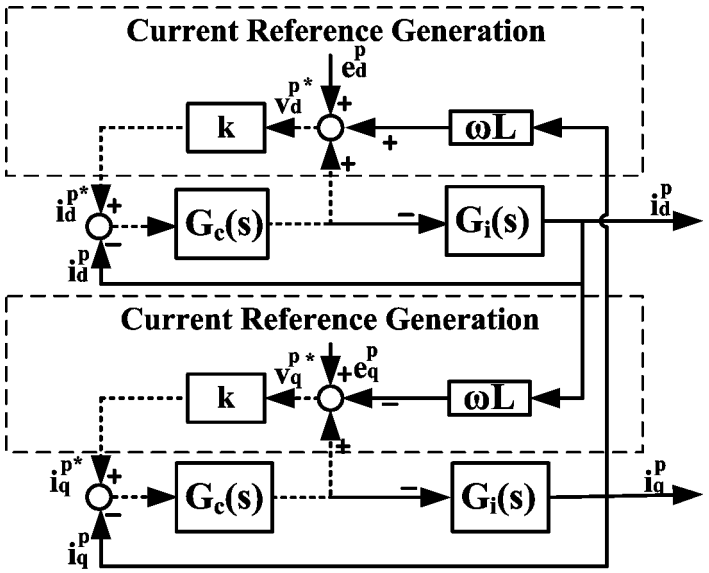


Fig. 5.2 Simplified closed-loop subsystem for a PWM rectifier in the positive sequence SRF – OPC scheme using Estimation Method 1

5.1.3.2 Stability analysis

The loop-transfer function for the basic closed loop system shown in Fig. 5.2 is given in (5.9). With the given control parameters (k_p and k_i), the system loop-transfer function is reduced to a stable first order linear system as discussed in the Section 5.1.3.1. Therefore, we can conclude that the basic control loop is stable.

Next, the stability due to the additional unintended feedback loop is analyzed. As mentioned earlier, with the OPC method, current commands can be expressed by the sequential components of the rectifier bridge input voltages as given in (5.6). As the parameter k has a non-linear relationship with rectifier bridge input voltage and the information about the structure of the input uncertainty is available, it is considered as a structured uncertainty for convenience (see appendix F). Therefore, ideas of uncertainty and stablility robustness theory are used to assess the robustness of the system stablility in face of this uncentainty. In Appendix F, the basic concepts behind uncertainty and stablility robustness are introduced.

To facilitate the stability robustness analysis, the compensated system with uncertainty shown in Fig. 5.2 is redrawn as shown in Fig. 5.3. This is a standard representation for robust stability condition formulation as shown in Fig. F.2 in Appendix F. Please note that the additional feedback loop still appears in the standard representation as shown in Fig. 5.3.

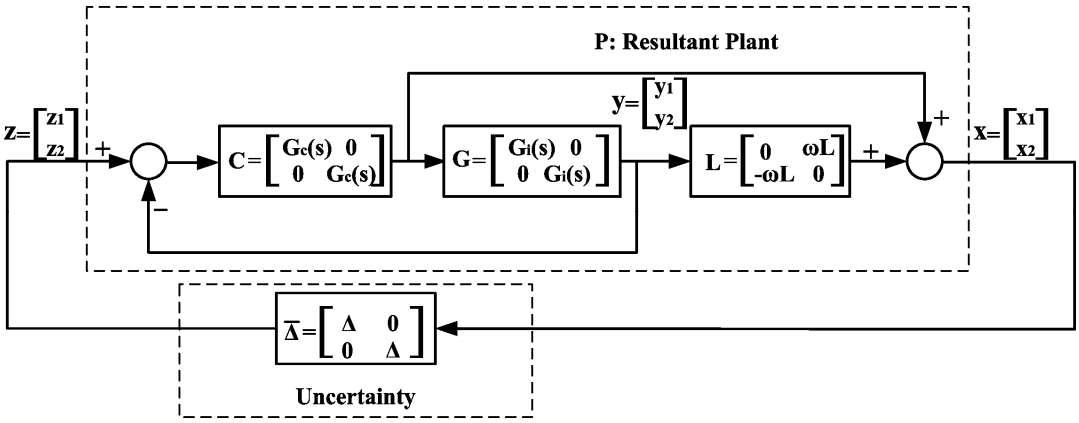


Fig. 5.3 Standard system used to formulate stability condition – OPC scheme using Estimation Method 1

Please note that the *d*-axis and *q*-axis supply input voltages in positive sequence synchronously rotating frame (e_d^p, e_q^p) in Fig. 5.2 have been removed in Fig.5.3 as they do not affect system stability robustness. In Fig 5.3, vector *y* denotes *d*-axis and *q*-axis actual currents in positive sequence SRF (i_d^p, i_q^p), vector *x* denote inputs to uncertainty and vector *z* denote outputs of the uncertainty.

The uncertainty Δ shown in Fig. 5.3 can be expressed with a normalized $\tilde{\Delta}$ as given below:

$$\Delta = K\tilde{\Delta}, \tag{5.10}$$

where $K = \begin{bmatrix} k & 0 \\ 0 & k \end{bmatrix}$ and $\left\|\tilde{\Delta}\right\|_\infty \le 1$. Variable *k* has been defined in (5.6).

Based on the stability robustness theorem, the compensated system will remain stable for all $\Delta \in BD_1$ (Appendix F) if and only if

$$\left\|K\right\|_\infty \le \frac{1}{\left\|P\right\|_\infty} \tag{5.11}$$

Next the singular value of the resultant plant P will be calculated. From Fig. 5.3, the following relationship can be derived.

$$\begin{cases} G \cdot C \cdot [z - y] = y \\ L \cdot y + C \cdot [z - y] = x \end{cases} \tag{5.12}$$

where $G = \begin{bmatrix} G_i(s) & 0 \\ 0 & G_i(s) \end{bmatrix}, C = \begin{bmatrix} G_c(s) & 0 \\ 0 & G_c(s) \end{bmatrix}$ and $L = \begin{bmatrix} 0 & \omega L \\ -\omega L & 0 \end{bmatrix}$.

The relationship between inputs to uncertainty x and outputs to uncertainty z is derived based on (5.12) as shown below.

$$P \cdot z = x \tag{5.13}$$

with $P = [L \cdot G + I] \cdot [C \cdot G + I]^{-1} C$.

The singular value of P is calculated as $\|P\|_u = 10.24$. Here, the uncertainty has been normalized with $\Delta = K\tilde{\Delta}$. Based on the stability robustness theorem, the compensated system remains stable for all $\Delta \in BD_1$ if and only if

$$K_\infty < \frac{1}{\|P\|_\infty} = 0.0976 \tag{5.14}$$

The Matlab M-file used to calculate the singular values of P is given in Appendix F.

Therefore, the system with the OPC method using Estimation Method 1 is robustly stable in the face of uncertainty Δ with the condition $k \le 0.0976$ satisfied.

5.1.4 Implementation of the OPC method using Estimation Method 2

The detailed closed-loop subsystem for a PWM rectifier in the positive sequence

SRF with Estimation Method 2 can be illustrated by Fig. 5.4. The *abc-dq* transformation and the subsequent inverse *abc-dq* transformation are omitted as discussed in Section 5.1.3.1 and the closed-loop subsystem can be simplified as in Fig. 5.5. Using Estimation Method 2, the additional feedback loop is absent from Fig. 5.4 and Fig. 5.5.

Here, $G_c(s)$ and $G_i(s)$ have the same meanings as those shown in Fig. 5.1 and Fig. 5.2. As the coupling terms and supply voltages in the system model shown in Fig. 5.4 can be directly cancelled by the decoupling control and feed forward control terms in the dual controller, these terms have been ignored in Fig. 5.5. Parameter *k* is again treated as uncertainty.

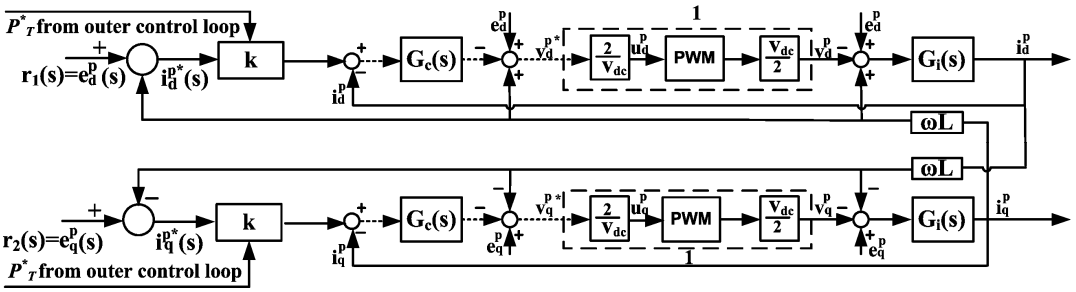


Fig. 5.4 Detailed closed-loop subsystem for a PWM rectifier in the positive sequence SRF − OPC scheme using Estimation Method 2

To facilitate stability robustness analysis, the compensated system with uncertainty shown in Fig. 5.5 is redrawn as shown in Fig. 5.6. This is again the standard representation for robust stability condition formulation as shown in Fig. F.2 in Appendix F. Once again, the *d*-axis and *q*-axis supply input voltages in the positive sequence synchronously rotating frame (e_d^p, e_q^p) in Fig. 5.5 have been neglected as they do not affect system stability robustness. Here, vector *y* denotes *d*-axis and *q*-axis actual currents in positive sequence synchronously rotating frame (i_d^p, i_q^p), vector *x* denotes inputs to uncertainty and vector *z* denotes outputs to uncertainty as before.

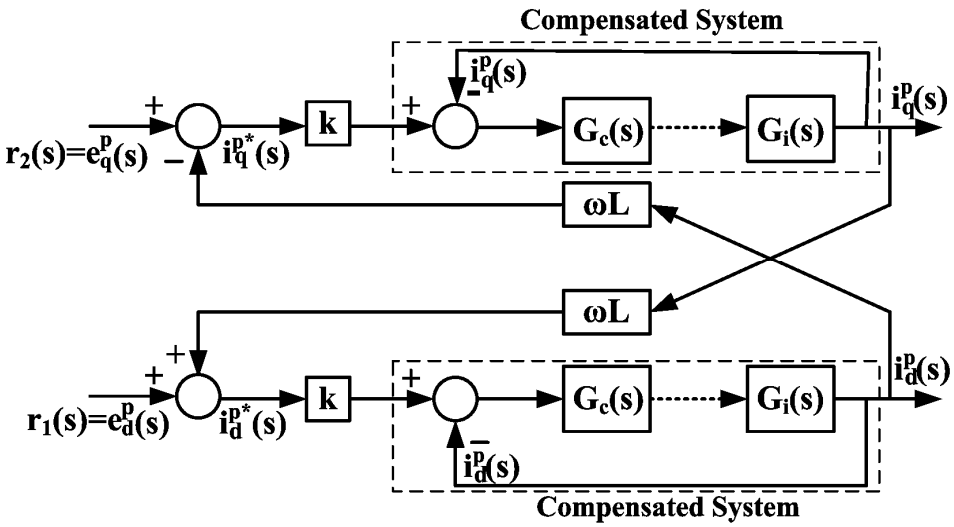


Fig. 5.5 Simplified control subsystem for a PWM rectifier in the positive sequence SRF – OPC scheme using Estimation Method 2

From Fig. 5.6, the relationship between inputs to uncertainty x and outputs to uncertainty z is

$$P' \cdot z = x \tag{5.15}$$

with $P' = T' \cdot L$ and $T' = \begin{bmatrix} T & 0 \\ 0 & T \end{bmatrix}$ where $T(s) = \dfrac{G_c(s)G_i(s)}{1+G_c(s)G_i(s)} = \dfrac{1}{\tau s+1}$.

The calculated structured singular value of P' is 1.3038. Here, the uncertainty has been normalized with $\Delta = K\tilde{\Delta}$ as discussed in Section 5.1.3. Based on the stability robustness theorem, the compensated system remains stable for all $\Delta \in BD_1$ if and only

$$K_\infty < \frac{1}{\|P'\|_\infty} = 0.767$$

(5.16)

The Matlab M-file used to calculate singular values of P' is given in Appendix F.

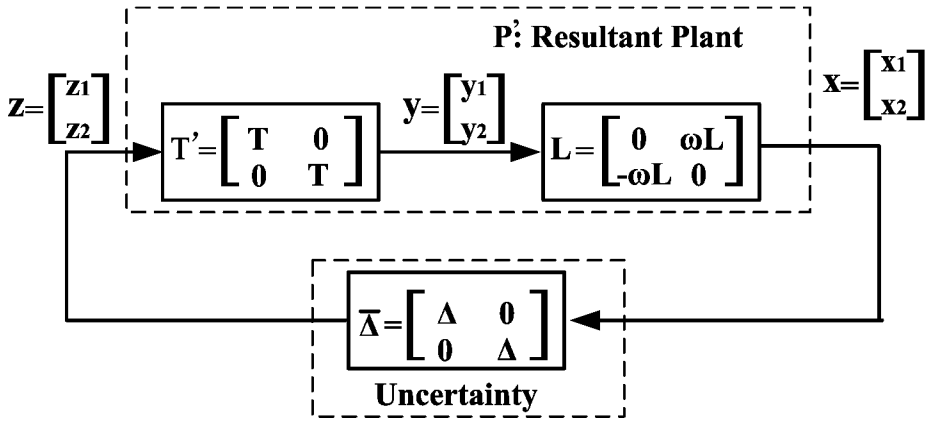


Fig. 5.6 The feedback loop of Fig. 5.5 redrawn to formulate stability condition – OPC scheme using Estimation Method 2

Therefore, the system with the OPC method using Estimation Method 2 is robustly stable in the face of uncertainty Δ with $k \le 0.767$.

5.1.5 Discussion on parameter *k*

As mentioned earlier, with the OPC method, current commands can be expressed by the sequential components of the rectifier bridge input voltages as given in (5.6). As the parameter k has a non-linear relationship with rectifier bridge input voltage, it has been considered as an uncertainty for convenience in the analyses presented before.

In the OPC method, k is a non-linear function of v^p and v^n as indicated in (5.6). Next, the expression for k is determined. Equations (4.14) and (4.15) give

$$\frac{v^p}{e^p} = \frac{k_1}{k} = \cos(\theta_e^p - \theta_v^p) \tag{5.17}$$

Substituting (5.17) and (4.17.d&e) into (4.17.f), variable k can be expressed as given below.

$$k = \frac{k_2}{\cos^2(\theta_e^p - \theta_i^p)} = \frac{k_2}{(1+\sqrt{1-4\omega^2 L^2 k_2^2})} \tag{5.18}$$

with $k_2 = 2p_T^* / 3[(e^p)^2 - (e^n)^2] = 2p_T^* / 3(e^p)^2(1-\mu^2)$ and $\cos(\theta_e^p - \theta_v^p) = \frac{k_2}{k_1}$ where $k_1^2 = (1-\sqrt{1-4\omega^2 L^2 k_2^2}) / 2\omega^2 L^2$.

It can be seen from (5.18) that the value of the parameter *k* is linked to the active power to be delivered, the degree of imbalance μ and the reactive power consumed which is determined by $\cos(\theta_e^p - \theta_i^p)$ in the OPC method. It can be concluded from (5.18) that the higher the degree of imbalance in the supply voltage and the greater the active power to be delivered the larger will be the value of parameter *k*. However, to maintain the robust stability of the plant shown in Fig. 5.3 and Fig. 5.6, the values of *k* should be less than the value indicated in (5.14) and (5.16). Therefore, the robustness stability of the compensated system is determined by the operating conditions. However, it is worth noting that the allowable value of *k* with Estimation Method 2 is 7.86 times of the allowable value of *k* with Estimation Method 1. Therefore, with Estimation Method 2, better stability robustness can be achieved for the compensated system than that with Estimation Method 1. This can be illustrated by the following example.

Let us consider the operating condition used in Chapter 4 as an example. The imbalance voltages used in the experiment in Chapter 4 are $e^p = 60\sqrt{2}$ and $e^n = 20\sqrt{2}$ which results in an unbalance ratio (negative sequence voltage magnitude to positive sequence voltage magnitude) of around 33%. Also, the rectifier bridge input terminal power is given by $p_T^* = 933W$ with 5% parasitic loss due to switching loss and

resistive loss in the circuit. With these assumptions, using (5.18), it is found that k is equal to 0.101. Therefore, the system with the OPC method using Estimation Method 1 is not robustly stable in the face of uncertainty Δ under the above operating condition. On the other hand, the system with the OPC method using Estimation Method 2 is robustly stable in the face of uncertainty Δ under the same operating condition.

As mentioned earlier, better stability robustness can be achieved for the resultant system with Estimation Method 2 than with Estimation Method 1. As pointed out earlier, in Fig. 5.3, besides the current control loop, an additional closed-loop exists, which uses the control output as a feedback signal for current reference generation. Poor stability robustness could very probably be attributed to this additional unintended feedback closed-loop. This feedback loop from the control output is absent in the case of Estimation Method 2 (Fig. 5.6) as mentioned earlier.

5.1.6 Simulation verification

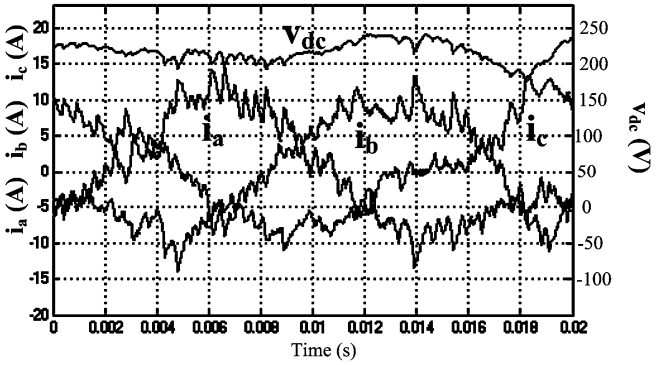


Fig. 5.7 Simulation waveforms with unbalanced supply voltage - OPC scheme using Estimation Method 1

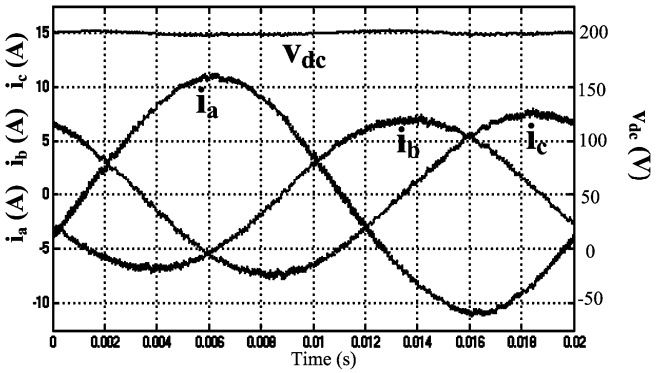


Fig. 5.8 Simulation waveforms with unbalanced supply voltage - OPC scheme using Estimation Method 2

Fig. 5.7 and Fig. 5.8 show the simulated results for the OPC method under unbalanced conditions using Estimation Method 1 and Estimation Method 2, respectively. As expected, the simulation results obtained with Estimation Method 1 (Fig. 5.7) are not stable even though it is bounded. The bounded signal in an unstable system might be due to the nonlinear nature of system and bounded control input, e.g., the output of PWM is always within range of -1 and 1. On the other hand, the simulation results with Estimation Method 2 (Fig. 5.8) are stable with high performance on both the input side and the output side.

5.1.7 Comments on OPC implementation methods

As discussed in Section 5.1.2, there are three implementation methods for the OPC scheme.

In the first method, which was the one adopted in Chapter 4, the OPC scheme is implemented using (5.2); this requires only the supply input voltages to be sensed and hence, the current reference generation/calculation does not involve any signals from the current control loop. Therefore, there is no uncertainty and stablility robustness issues in this implementation.

On the other hand, both the implementations using Estimation Method 1 and Estimation Method 2 have used signals from the current control loop. In Estimation Method 1, the signals from the control output have been used for current reference calculation. Thus, in the implementation with Estimation Method 1, an additional feedback-loop exists which may be accountable for limited stability robustness range.

In the implementation with Estimation Method 2, the system exhibits better robustness of stability in the face of uncertainty compared to the implementation with Estimation Method 1.

5.2 Investigation of the reason for the poor performance of the POPC method [52]

As mentioned earlier, the POPC method can theoretically achieve unity power factor operation and excellent *dc* output voltage regulation. However, the experimental results obtained with this method in literature [52] show large values of steady-state error and second order harmonic in the *dc* output voltage. In this subsection, the possible reason for this poor performance of the POPC method will be investigated.

5.2.1 Introduction of the POPC method

The power condition equations for the POPC method are given in (4.7). Substituting expressions of the positive- and negative- sequence voltage and current vectors into (4.7) and using instantaneous reactive power definition detailed in the Appendix E, we have

$$\begin{bmatrix} \frac{2}{3}\overline{p}_{in} \\ \frac{2}{3}\overline{q}_{in} \\ \frac{2}{3}p_{Tc} \\ \frac{2}{3}p_{Ts} \end{bmatrix} = \begin{bmatrix} \frac{2}{3}P_{in}^{*} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} e_d^p & e_q^p & e_d^n & e_q^n \\ e_q^p & -e_d^p & -e_q^n & e_d^n \\ v_d^n & v_q^n & v_d^p & v_q^p \\ v_q^n & -v_d^n & -v_q^p & v_d^p \end{bmatrix} \begin{bmatrix} i_d^p \\ i_q^p \\ i_d^n \\ i_q^n \end{bmatrix} \tag{5.19}$$

The resulting solutions are

$$\begin{bmatrix} i_d^p \\ i_q^p \\ i_d^n \\ i_q^n \end{bmatrix} = \frac{2p_{in}^{*}}{3|A|} \begin{bmatrix} e_d^p (v^p)^2 - e_q^n (v_d^n v_q^p + v_d^p v_q^n) + e_d^n (v_q^p v_q^n - v_d^n v_d^p) \\ e_q^p (v^p)^2 - e_q^n (v_q^n v_q^p - v_d^p v_d^n) - e_d^n (v_d^p v_q^n + v_d^n v_q^p) \\ -e_q^p (v_d^n v_q^p + v_d^p v_q^n) + e_d^p (v_q^n v_q^p - v_d^p v_d^n) + e_d^n (v^n)^2 \\ -e_q^p (v_q^p v_q^n - v_d^n v_d^p) - e_d^p (v_q^n v_d^p + v_q^p v_d^n) + e_q^n (v^n)^2 \end{bmatrix}, \tag{5.20}$$

where

$$|A| = (e^p)^2 (v^p)^2 + (e^n)^2 (v^n)^2 - 2(e_q^n e_d^p + e_q^p e_d^n)(v_q^n v_d^p + v_q^p v_d^n) + 2(v_q^p v_q^n - v_d^n v_d^p)(e_d^n e_d^p - e_q^n e_q^p)$$

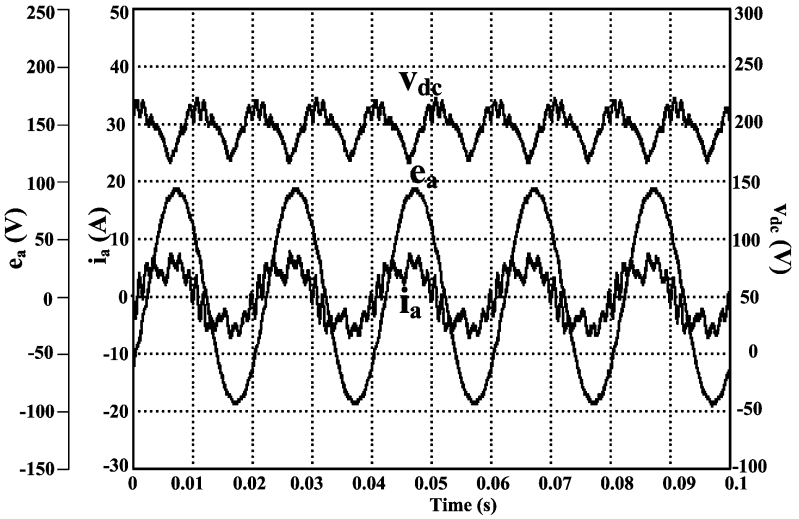


Fig. 5.9 Experimental steady-state waveforms under unbalanced supply voltage: a-phase current, a-phase supply voltage and *dc* output voltage under unbalanced condition – POPC method with implementation as in [52] (Estimation Method 1)

Eq. (5.20), which has been developed in [52], provides a closed-loop solution to the POPC method which avoids the implementation difficulties faced when the non-linear power equations are solved iteratively in real-time [51] to obtain the current references.

Although, as mentioned earlier, the control method outlined in [52] can, in principle, eliminate ripple on the *dc* output voltage, in practice, the performance was not as good as expected. Experimental waveforms which illustrate this are given in Fig. 5.9. This figure shows the input voltage, input current and *dc* output voltage waveforms from our experimental set-up with the current commands being generated using the scheme in [52]. The test conditions were the same as in Fig. 4.8. The unbalance conditions are more severe than those used in [52]. Considerable second harmonic ripple and also steady-state error may be seen in the *dc* output voltage waveform, confirming the poor results reported in [52].

5.2.2 Investigation of the reason for poor performance

The control system block diagram for the POPC control method used in [52] is redrawn in Fig. 5.10. To generate current commands, both sequential components of the supply input voltage and rectifier bridge input voltage are required. As shown in Fig. 5.10, instead of a simple current control loop, the rectifier bridge input voltages obtained from the control signals (Estimation Method 1) form an additional closed-loop (see dashed line). The investigations carried out in Section 5.1 with regard to the OPC method suggest that this additional loop may lead to poor stability robustness of the overall closed-loop system in the POPC case also, thereby accounting for the poor performance obtained in the experimental results with the POPC strategy.

5.2.3 Difficulty in analyzing the effect of the extra loop on the overall closed-loop system behavior

The effect of the extra loop presented in Fig. 5.10 on the overall closed-loop system behavior could, in principle, be studied using the same analysis method discussed in Sec. 5.1. However, the current commands given in (5.20) are constructed partially from the rectifier bridge input voltages and partially from supply input voltage and have highly non-linear relationship with the rectifier bridge input voltages. This non-linear relationship between current commands and

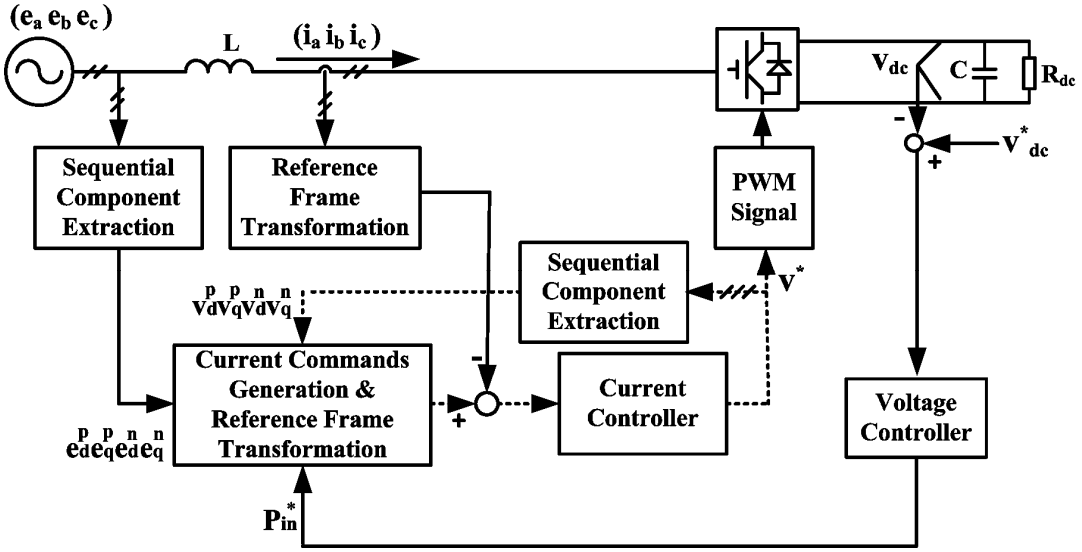


Fig. 5.10 Control system block diagram for the partial output power control method [52] (Estimation method 1)

the rectifier bridge input voltages makes it difficult to analyze the effect of the extra loop on the overall closed-loop system behavior in this case as has been done in Sec 5.1 for the OPC method.

With the OPC method, the current commands are proportional to only the rectifier bridge input voltages as presented in (4.13). This is reproduced below.

$$\begin{bmatrix} i_d^{p*} \\ i_q^{p*} \\ i_d^{n*} \\ i_q^{n*} \end{bmatrix} = \frac{2P_T^*}{3D} \begin{bmatrix} v_d^p \\ v_q^p \\ -v_d^n \\ -v_q^n \end{bmatrix}. \tag{5.21}$$

Here, the current commands are completely generated from the additional loop (see dashed line) in Fig. 5.10 if the OPC method is implemented using Estimation Method 1. Thus, this scheme can reflect the worst effect on the closed-loop behavior caused by the additional feedback loop.

In this Chapter, the investigation result obtained with the OPC method is directly extended to the POPC method. The detailed analysis of the effect of the extra loop on the overall closed-loop system behavior in the case of the POPC scheme is suggested as a possible future research work.

5.3 Improved realization of the POPC Method

Based on the discussion in Section 5.2 for the POPC method, we can conjecture that the poor performance of the POPC [52] may be due to the use of control signals to construct the rectifier bridge input voltage signals introducing an additional feedback loop in the closed-loop system.

Also, based on the analysis in Section 5.1, for the OPC method at least, using Estimation Method 2, the resultant system has better robustness stability. This finding suggests a possible solution for improved realization of the POPC method.

In the POPC scheme, instead of using Estimation Method 1, the current commands can be calculated using Estimation Method 2.

The effectiveness of this solution will be verified by both simulation and experiment results.

5.4 Simulation and experimental verification

In this section, both simulation and experimental results with the POPC method using both Estimation Methods 1 and 2 are presented and discussed.

The control block diagram of the proposed scheme is again shown in Fig. 4.5. The voltage controller and current controllers are the same as used in the OPC method. The sequence separation methods for current and supply input voltages are the same as explained in section 4.2.3. The current commands are calculated based on (5.20). The rectifier bridge input voltages are constructed by both Estimation Method 1 and Estimation Method 2.

The system parameters are: L = 4.15 mH, R = 0.27 Ω, C = 136 μF, R_{dc} = 45 Ω and f = 10 kHz for both switching frequency and sampling frequency. The supply frequency was 50 Hz and the *dc* output voltage was regulated at 200 V for both unbalanced cases. The proposed control scheme was simulated using Matlab 6.5 and Simulink and was also implemented on a dSPACE DSP system (DS1104). The supply voltages for the simulation were set at $44\sqrt{2}\sin(\omega t + 355^\circ)$ V, $75\sqrt{2}\sin(\omega t + 236^\circ)$ V and $66\sqrt{2}\sin(\omega t + 90^\circ)$ V.

Fig. 5.11 and Fig. 5.12 show the simulated and experimental results for the POPC method under unbalanced conditions using Estimation Method 1. As expected, both *dc* output voltage and line currents are poorly regulated. Considerable second harmonic

ripple and also steady-state error can be seen in the *dc* output voltage waveform, confirming the results reported in [52]. Though the simulated and experimental results are similar, they are not exactly the same. This is likely due to that the initial conditions for both cases are not the same.

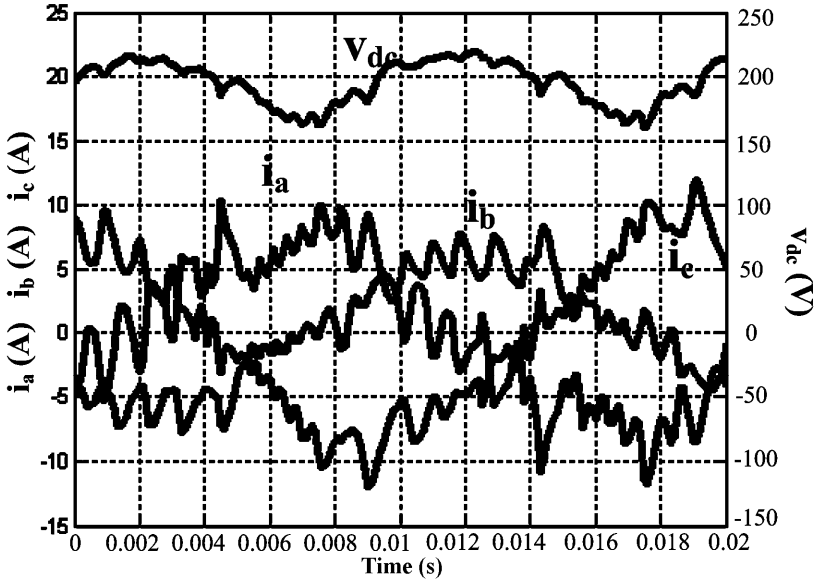


Fig. 5.11 Simulated waveforms for unbalanced supply voltage – POPC scheme using Estimation Method 1

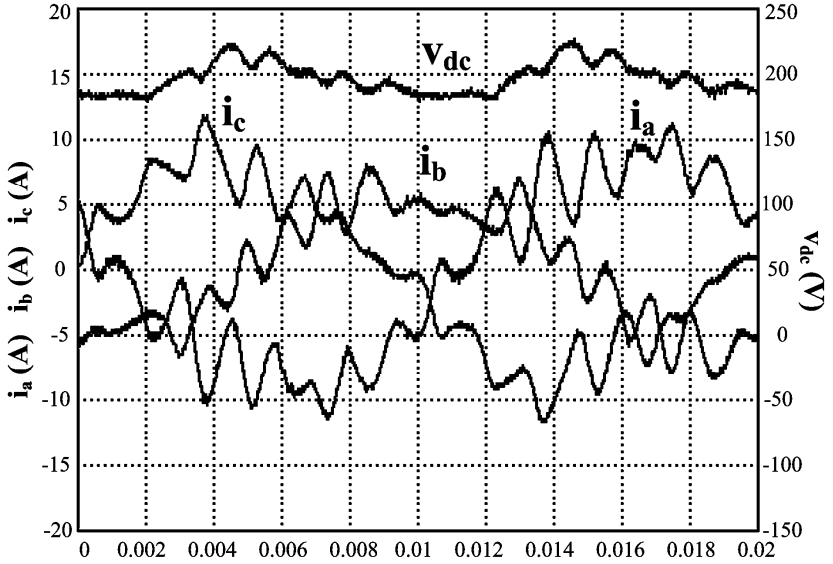


Fig. 5.12 Experimental waveforms for unbalanced supply voltage – POPC scheme using Estimation Method 1

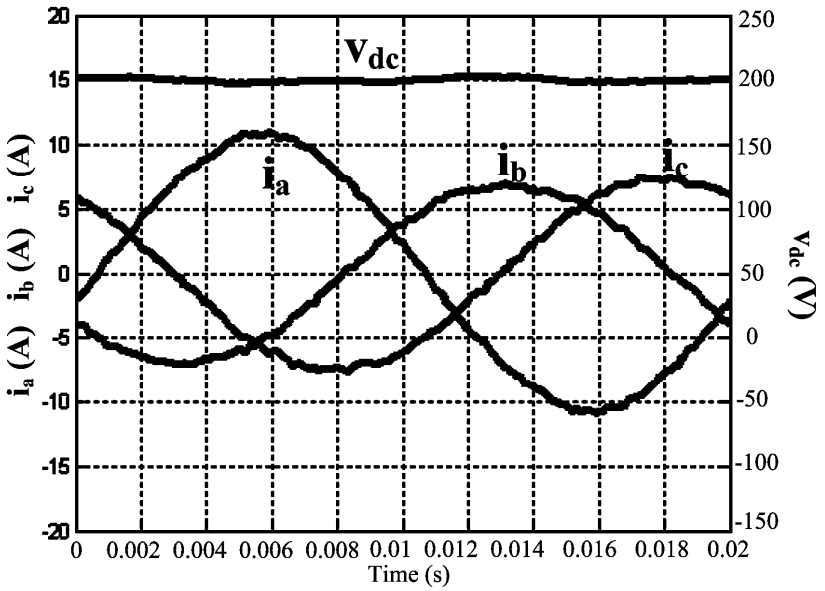


Fig. 5.13 Simulated waveforms for unbalanced supply voltage – POPC scheme using Estimation Method 2

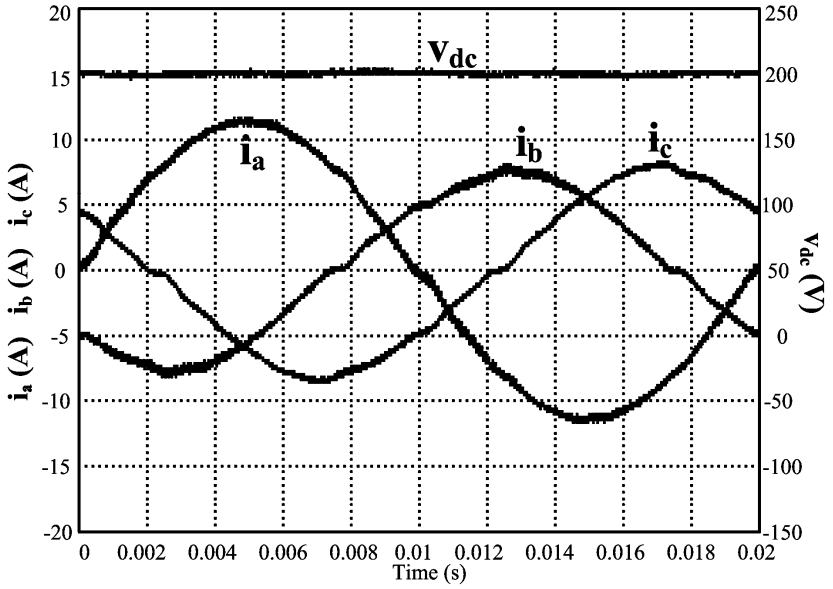


Fig. 5.14 Experimental waveforms for unbalanced supply voltage – POPC scheme using Estimation Method 2

Fig. 5.13 and Fig. 5.14 show the simulated and experimental results for the POPC method under unbalanced conditions using Estimation Method 2. The current waveforms, though unbalanced as expected, are nearly sinusoidal, while the *dc* output

voltage is nearly constant with low ripple. The measured THD for the three line currents were 1.99%, 4.8%, 4.88%, respectively. The maximum peak to peak ripple voltage in the output voltage was 4V. Both the simulation and experimental results show the effectiveness of the realization of the POPC method with Estimation Method 2.

As mentioned earlier, the POPC method can provide constant *dc* output voltage and unity vector power factor operation simultaneously. Due to implementation problem, the advantage of this method was not fully realized in the previous literature. In the present research, through a slight modification in the implementation, the strength of the POPC method has been realized.

As can be seen from Fig. 5.13 and Fig. 5.14, the *dc* output voltage obtained with the POPC method are constant. On the other hand, as the average reactive power is regulated to zero, the vector power factor is unity. Fig. 5.15~5.17 shows three-phase current and their corresponding voltage of a PWM rectifier with the POPC method under unity vector power factor operation respectively. As shown in Fig. 5.15, a-phase current is almost in phase with a-phase voltage. However, b phase current and c phase current are not in phase with their corresponding voltages. As shown in Fig. 5.16 and 5.17, the b phase current has a lead relationship with the b-phase voltage whereas the c-phase current has a lag relationship with the c-phase voltage. This is a consequence of the fact that reactive powers are allowed to flow among the three phases under unity vector power factor operation as long as the sum of the reactive powers in the three phases is zero. Thus, vector power factor may be over-optimistic in evaluating the power flow condition. In a balanced system, when currents are aligned to their corresponding voltage, reactive power across each phase becomes zero. However, it was found that

neither was the phase current in phase with its corresponding supply voltage nor they have the same amplitudes under unbalanced supply voltages from experimental results shown in Fig 5.15 ~ 5.17 obtained under unity vector power factor operation.

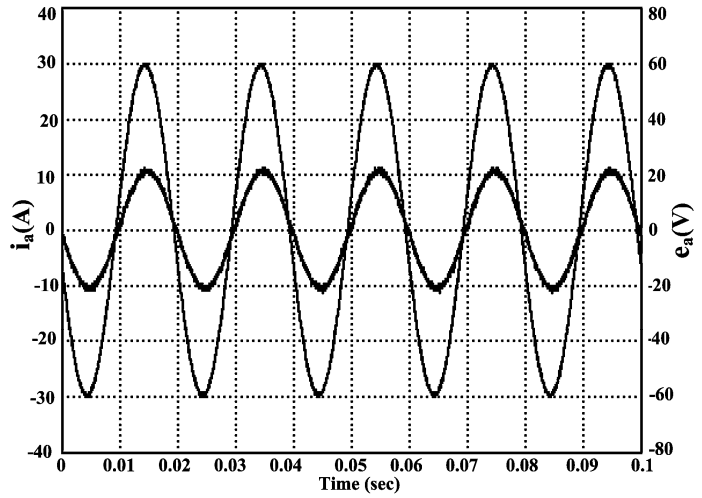


Fig. 5.15 Experiment results for a-phase current and a-phase voltage under unbalanced condition

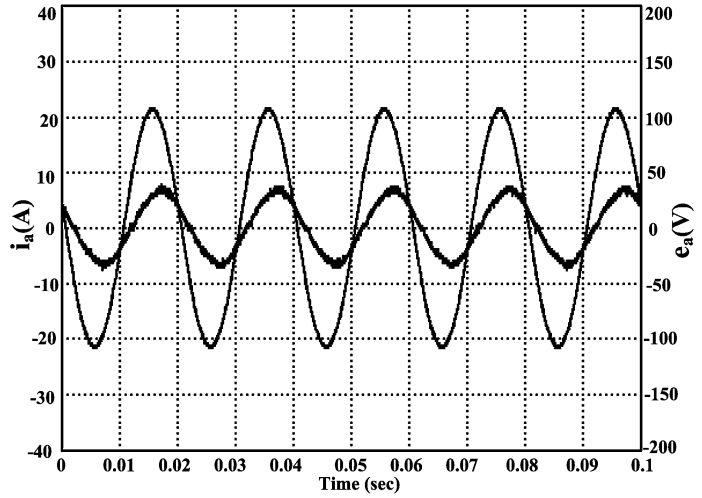


Fig. 5.16 Experiment results for b-phase current and b-phase voltage under unbalanced condition

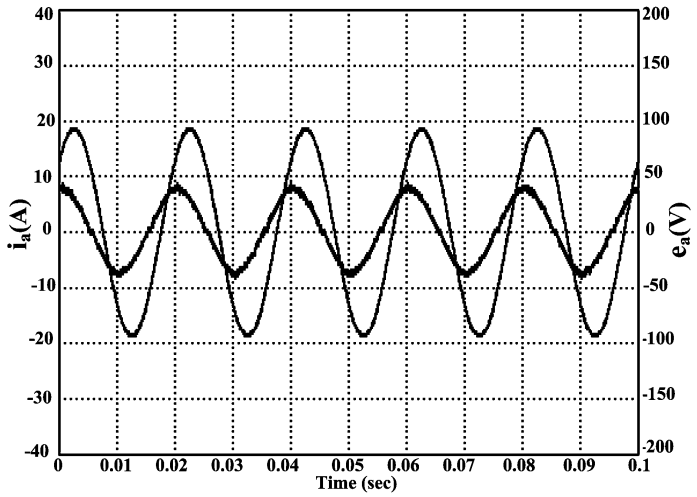


Fig. 5.17 Experiment results for c-phase current and c-phase voltage under unbalanced condition

5.5 Discussion

With the Estimation Method 2, the POPC can achieve high performance in both input and output sides for the above operating conditions. However, as discussed in Section 5.3, it is difficult to theoretically analyze the POPC with stability robustness theory as used in the OPC method. Therefore, we have yet to determine the stability robustness range of the POPC method.

To fully explore the strength of the POPC method, more research should be done to find a proper realization of the POPC method and also to explore the stability robustness range of the method with Estimation Method 2.

5.6 Conclusions

Different implementation methods of the OPC scheme have been analyzed in this chapter. It has been found that Estimation Method 1 results in an additional loop which largely degrades system stability. On the other hand, Estimation Method 2 largely improves system stability.

The reason for poor performance obtained with the POPC method was then investigated. Based on the insight gained with the OPC method, it was suggested that the use of Estimation Method 1 may be the cause of the poor performance obtained with POPC method also. An improved implementation of the POPC method based on Estimation Method 2 was carried out. With this change in the control scheme, the POPC method was shown to provide sinusoidal line current, constant *dc* output voltage and unity vector power factor operation.

It was found that even under unity vector power factor, the line current is not in phase with its corresponding supply voltage. Thus, the power flow condition under supply imbalance should be fairly evaluated. This issue will be addressed in Chapter 6.

CHAPTER 6

PERFORMANCE ASSESSMENT OF POWER REGULATION SCHEMES FOR UNBALANCED SUPPLY CONDITIONS

6.0 Introduction

In Chapter 5, an improved realization of the partial output power control (POPC) method has been proposed. With the proposed realization, the POPC method can provide nearly constant *dc* output voltage and unity vector power factor (VPF) operation. However, it was found that the resultant phase current is not in phase with its corresponding supply voltage even under unity VPF operation. As imbalance degrades the efficiency of power transmission just as reactive power does [5-7], the performance evaluation of the different control schemes must be based on an appropriate definition of power factor, taking into account degradation in power transfer performance due to supply imbalance also besides reactive power drawn by a load.

In this chapter, two different power factor definitions, viz., vector power factor (VPF) and effective power factor (EPF) are first defined and discussed. Typically, in PWM rectifier research so far in literature [48-52], the concept of VPF has been utilized. That has been the approach followed in the present work so far. In this chapter, it is shown that the alternative concept of 'effective power factor' results in a better

evaluation of the power transfer performance of a given PWM rectifier control method under unbalanced supply conditions.

Following this, the performances of the different control methods previously introduced in Chapters 4 and 5 are compared. In particular, the discussion will be focused on the power factor achieved with different schemes based on the two different power factor definitions.

The number of PWM rectifier control methods evaluated under unbalanced supply operation in this chapter is four. Besides the three 'power oriented' control methods investigated earlier, an additional control method, called 'voltage oriented control' (VOC) method for the three phase PWM rectifier is introduced and investigated in this chapter. This latter method has the potential to achieve high power factor operation. It is based on the simple idea of extending a straightforward voltage oriented control method for the balanced supply input case [43, 57] to the unbalanced supply case also.

The remaining methods discussed are the three power oriented control methods which have been introduced and discussed earlier in Chapters 2 and 4，5. They are 1) the input power control (IPC) method, 2) the partial output power control (POPC) method and 3) the output power control (OPC) method. Of these three, IPC and POPC are existing methods, while OPC is a new control method introduced in Chapter 4 of this thesis. Also, in order to implement the POPC scheme, estimation of the bridge rectifier terminal voltages is required. As discussed in Chapter 5, in the case of the OPC method, Estimation Method 2 has the potential to achieve a wider range of stablility robustness in the face of uncertainty compared to Estimation Method 1. It has also been

experimentally shown in Chapter 5 that stable operation can be obtained for the POPC method with Estimation Method 2. Hence, in the present chapter Estimation Method 2 is used in the implementation of the POPC scheme.

The achievable VPF and EPF of the four power regulation methods are first obtained with theoretical analysis. The expressions of the achievable VPF and EPF are verified through simulations. The performances of these four control methods are then evaluated in terms of the EPF obtained, current THDs and peak-peak *dc* output voltage. It is found that the OPC method and the POPC method (with the suggested modification) provide optimal performances.

However, as mentioned in Chapter 5, the stability robustness of the realization of the POPC method is yet to be theoretically proven. Due to this, in situations where both high input side and output side performances are required, the OPC method may be a better choice for controlling the three phase PWM rectifier.

6.1 Discussion on power factor definitions

The power factor definition used so far in earlier chapters and in much of the literature in the area of three phase PWM rectifiers is based on the concept of 'vector power factor' (VPF) [7], which is defined as follows:

$$P_{FV} = \frac{P}{S_V}, \tag{6.1}$$

where S_V is the 'vector apparent power' with

$$S_V = |P + jQ|. \tag{6.2}$$

Here, P is the total active power with

$$P = P_a + P_b + P_c = P^P + P^n + P^0. \tag{6.3}$$

The variables P_a, P_b and P_c are the active power components in the three phases and P^p, P^n and P^0 are the positive-, negative-, and zero-sequence active power components, respectively.

Likewise, Q is the total reactive power with

$$Q = Q_a + Q_b + Q_c = Q^P + Q^n + Q^0. \tag{6.4}$$

Here, the variables Q_a, Q_b, and Q_c are the reactive power components in the three phases and Q^p, Q^n and Q^0 are the positive-, the negative-, and zero-sequence reactive power components, respectively.

Greater details on the definitions of P_a, P_b, P_c and Q_a, Q_b, Q_c are given in Appendix E.

In a balanced system, when currents are aligned to their corresponding voltages, reactive power in each phase becomes zero. Therefore, unity VPF operation results in minimum power loss operation as the RMS value of the current is minimized under such balanced operation.

On the other hand, in an unbalanced system, it has been shown in the experimental results obtained in Chapter 5 that the phase current is not in phase with its corresponding supply voltage. In addition, the phase currents have different amplitudes while the operation results in zero average reactive power and unity VPF operation. In this case, even though the reactive power in each phase is not zero any more, the VPF definition

treats the three-phase reactive power as a whole. Thus, the reactive currents are allowed to flow in the three individual phases under unity VPF so long as the sum of the three-phase reactive powers ($Q = Q_a + Q_b + Q_c$) is zero. Thus, unity VPF operation can be achieved even with reactive currents flowing in individual phases under unbalanced supply conditions.

Table 6.1 shows the voltages and currents in a hypothetical system with imbalances in both input voltages and currents. Two different conditions of operation have been considered. Here, the active power transferred is targeted to be 900W and the supply voltages are set at $42\sqrt{2}\sin(\omega t + 355^\circ)$ V, $75\sqrt{2}\sin(\omega t + 236^\circ)$ V and $66\sqrt{2}\sin(\omega t + 90^\circ)$ V. These voltage values are the same as those used in the experiments in Chapters 4 and 5 and they correspond to a positive sequence voltage of around 60 V (RMS) at a phase of -13^o and a negative sequence voltage of around 20 V (RMS) at a phase of 148^o as indicated in Chapter 4. Two sets of system operating conditions are considered (Cond. 1 & Cond. 2) with different phase currents.

Incidentally, the three currents for Cond. 1 are based on the VOC method, which is introduced later in this chapter, and the currents for Cond. 2 are based on the IPC method. The fact that the currents indicated here are obtained using these methods, however, is not relevant to the present discussion on power factor definitions.

Table 6.2 shows the values of power and the reactive power in the three phases, a, b & c and the corresponding positive- negative- and zero- sequence values under the two conditions. These values have been calculated using the system data in Table 6.1. It may be noted that the net active power, as per (6.3), is the same in both cases (≈ 900 W)

Using the power and reactive power values calculated in Table 6.2 and using (6.1) ~ (6.4), the VPFs for the two conditions have been computed (Table 6.3). As may be noticed in Table 6.2, under Cond. 1, the three reactive powers are individually near zero while under Cond. 2, they are not. However, the net three phase reactive power Q (see Table 6.3) is nearly zero under both conditions, resulting in near unity VPF in both cases.

TABLE 6.1 UNBALANCED POWER FLOW CONDITIONS WITH SUPPLY VOLTAGE IMBALANCE

	a-phase		b-phase		c-phase	
	e_a (RMS, V)	i_a (RMS, A)	e_b (RMS, V)	i_b (RMS, A)	e_c (RMS, V)	i_c (RMS, A)
Cond. 1	42∠355°	3.12∠-4°	75∠236°	5.73∠-123°	66∠90°	5.1∠-270°
Cond. 2	42∠355°	7.42∠-18°	75∠236°	4.38∠-149°	66∠90°	5.59∠126°

TABLE 6.2 ACTIVE AND REACTIVE POWER VALUES FOR THE SYSTEMS IN TABLE 6.1

	a-phase		b-phase		c-phase		pos. sequence		neg. sequence		zero sequence	
	P_a (W)	Q_a (VAR)	P_b (W)	Q_b (VAR)	P_c (W)	Q_c (VAR)	P^p (W)	Q^p (VAR)	P^n (W)	Q^n (VAR)	P^0 (W)	Q^0 (VAR)
Cond. 1	131	-2.3	430	-7.5	337	0	810	0	90	0	0	0
Cond. 2	304	70	298	139	298	-216	1012	0	-112	0	0	0

This anomalous situation can be avoided by the use of the concept 'effective apparent power'. Ref. [7] defines effective apparent power as the maximum active power that can be transmitted under a virtual, balanced, poly-phase system that has potentially the same power losses as the actual unbalanced system.

The equivalent balanced voltage (e_e) and current (i_e) may be defined as follows:

$$e_e = \frac{1}{\sqrt{2}}\sqrt{(e^p)^2 + (e^n)^2} \tag{6.5}$$

$$i_e = \frac{1}{\sqrt{2}}\sqrt{(i^p)^2 + (i^n)^2} \tag{6.6}$$

Here, e^p, e^n, i^p and i^n refer to the peak values of the positive and negative sequence

phase voltages and currents. The equivalent voltage e_e and equivalent current i_e have been defined in (6.5) and (6.6) in such a way as to potentially have the same impact on the power system losses as the actual voltages and currents.

The three-phase effective apparent power is then given by

$$S_e = 3e_e i_e \tag{6.7}$$

Using the above defined effective apparent power, the 'effective power factor' (EPF) can be defined [7] as

$$P_{FE} = \frac{P}{S_e}. \tag{6.8}$$

TABLE 6.3 DETERMINATION OF POWER FACTOR VALUES USING DATA IN TABLE 6.1 AND TABLE 6.2

	Vector Power Factor				Effective Power Factor							
	P (W)	Q (Var)	S_V (VA)	VPF	e^p (V)	e^n (V)	e_e (V)	i^p (A)	i^n (A)	i_e (A)	S_e (VA)	EPF
Cond. 1	898	-9.8	898	0.999	84.84	28.3	63.3	6.36	2.12	4.75	901	0.99
Cond. 2	900	-7	900.02	0.997	84.84	28.3	63.3	7.95	2.65	5.93	1126	0.79

Table 6.3 also contains the values of effective power factors calculated for the two conditions discussed before. It may be noted from Table 6.3 that the effective equivalent current i_e and hence the effective apparent power S_e are larger under Cond. 2 than under Cond. 1. This accurately reflects the fact that the reactive power in the individual phases is non-zero under Cond. 2. Consequently, the EPF for Cond. 2 is lower which again accurately reflects the true power flow condition.

Thus, the EPF is a candidate to practically and realistically evaluate the power flow condition under unbalanced operation. In the following sections, EPF will be used as an index to evaluate power flow conditions in the PWM rectifier system.

6.2 Power regulation methods for unbalanced supply operation

In this section, the different power regulation methods for operation under unbalanced power supply conditions are discussed and brought under a common approach. As mentioned earlier, a new VOC method is first introduced. This simple method may be viewed as a direct extension of the VOC method for a balanced system [43, 57] to the case of unbalanced input supply. Following this, the three power-oriented control methods discussed earlier in Chapters 4 and 5 and reported in literature [49, 51~52] are again presented here under a common frame work. This then sets the stage for the investigation into the achievable power factor with the different methods in Section 6.3.

6.2.1 Voltage-oriented control (VOC) method

A simple control [43, 57] for unity power factor operation applicable when the PWM rectifier system operates under balanced supply will be to keep the individual phase currents to be in phase with the corresponding voltages while controlling the current magnitude to be proportional to the corresponding voltage. With such a control scheme, the PWM rectifier can provide constant *dc* output voltage while drawing balanced sinusoidal line currents at a unity power factor (both VPF and EPF) in a balanced system. This control method is termed as 'voltage-oriented control' method [43].

The above scheme may be directly extended to an unbalanced system by making

the positive sequence current proportional to and in phase with the positive sequence voltage and likewise making the negative sequence current proportional to and in phase with the negative sequence voltage.

$$\vec{i}^{\,p} = k\vec{e}^{\,p} \text{ and } \vec{i}^{\,n} = k\vec{e}^{\,n} \tag{6.9}$$

Here, the variable k is constant. The corresponding phasor diagram is shown in Fig. 6.1.

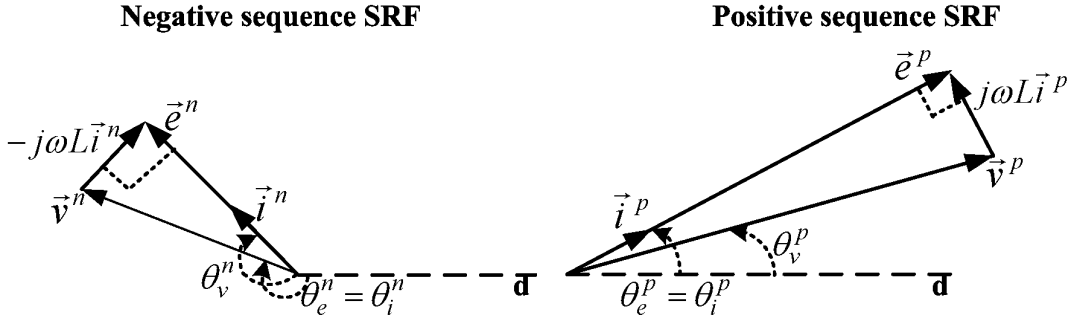


Fig. 6.1 Phasor diagram for the voltage-oriented control method

The following equations are based on (4.11a) & (4.11b).

$$P_{in} = \frac{3}{2}e^p i^p \cos(\theta_e^p - \theta_i^p) + \frac{3}{2}e^n i^n \cos(\theta_e^n - \theta_i^n), \tag{6.10.a}$$

$$P_{inc} = \frac{3}{2}e^p i^n \cos(\theta_e^p + \theta_i^n) + \frac{3}{2}e^n i^p \cos(\theta_e^n + \theta_i^p), \tag{6.10.b}$$

$$P_{ins} = -\frac{3}{2}e^p i^n \sin(\theta_e^p + \theta_i^n) - \frac{3}{2}e^n i^p \sin(\theta_e^n + \theta_i^p). \tag{6.10.c}$$

$$q_{in} = \frac{3}{2}e^p i^p \sin(\theta_e^p - \theta_i^p) - \frac{3}{2}e^n i^n \sin(\theta_e^n - \theta_i^n) \tag{6.10.d}$$

Eqs. (6.10.a~6.10.c) are the components of the instantaneous input active power in (4.11.a) and (6.10.d) is the average reactive power in (4.11.b). This has been calculated by considering the instantaneous reactive power based on instantaneous reactive power

theory (Appendix E) and then averaging the same over a line cycle.

With the current commands given by (6.9),

$$\theta_e^p = \theta_i^p \quad \text{and} \quad \theta_e^n = \theta_i^n . \tag{6.11}$$

Therefore, the equations (6.10.a~d) can be simplified as follows.

$$P_{in} = \frac{3}{2} k[(e^p)^2 + (e^n)^2] \tag{6.12.a}$$

$$P_{inc} = 3ke^p e^n \cos(\theta_e^p + \theta_e^n) \tag{6.12.b}$$

$$P_{ins} = 3ke^p e^n \sin(\theta_e^p + \theta_e^n) \tag{6.12.c}$$

$$q_{in} = 0 \tag{6.12.d}$$

For a given average active power P_{in}, the variable k can be written as

$$k = \frac{2P_{in}}{3[(e^p)^2 + (e^n)^2]} \tag{6.13}$$

Under balanced supply conditions, the voltage e^n is equal to zero and hence the power ripple (with cosine and sine components P_{inc} and P_{ins}) at the supply input terminals are also zero. However, with an unbalanced supply, these ripple power components are no longer zero. Therefore, with the VOC method, a substantial second-order ripple will occur on the output side. This will be shown later to occur in the experimental results obtained with this scheme.

As will be discussed later, this scheme manages to achieve the highest effective power factor. However, the substantial second order ripple with this scheme is a major disadvantage of this scheme.

6.2.2 Power oriented control methods

The instantaneous power balance on the *ac* side gives rise to the condition shown in (4.5) which is reproduced below (see Fig. 4.1).

$$p_{in} = p_T + p_L \tag{6.14}$$

In a balanced system with three-phase balanced line currents, the net instantaneous power in the inductors, p_L, is zero. However, in an unbalanced system, p_L is no longer zero and will contain ripple power. Each term in (6.14) has three parts as indicated below when both the line currents and supply voltages are unbalanced but sinusoidal.

$$p_z = P_z + P_{zc}\cos 2\omega t + P_{zs}\sin 2\omega t \tag{6.15}$$

Here P_z is the constant portion of the instantaneous power p_z and P_{zc}, P_{zs} are the coefficients of the second order harmonic power ripple varying as $cos2\omega t$ and $sin2\omega t$ respectively. Subscript z in (6.15) can denote the symbols '*in*', '*T*', and '*L*' present in (6.14).

To control the power flow in a PWM rectifier, the average active power, the average reactive power and the instantaneous power ripple become concerns of interest at either supply input terminals (AA' in Fig. 4.1) or rectifier bridge input terminals (BB' in Fig. 4.1). If both supply voltages and line currents are unbalanced but sinusoidal, the instantaneous power at AA' or BB' is given as follows based on the power definition in [69].

$$p_z = x_a i_a + x_b i_b + x_c i_c = \frac{3}{2}(x_\alpha i_\alpha + x_\beta i_\beta) = \frac{3}{2}\mathrm{Re}((\vec{x}_s^{\,p} + \vec{x}_s^{\,n})(\vec{i}_s^{\,p} + \vec{i}_s^{\,n})^*) \tag{6.16}$$

Here, variables i_a, i_b, i_c represent instantaneous input currents and x_a, x_b, x_c represent instantaneous voltages with x denoting either the input supply voltage or the rectifier bridge input voltage (averaged over a switching cycle). Variables x_α, x_β and i_α, i_β are α-axis and β-axis voltages and α-axis and β-axis currents, respectively. Variables $\vec{x}_s^{\,p}$ and $\vec{i}_s^{\,p}$ denote the positive sequence voltage and current vectors in the SF with

$$\vec{x}_s^{\,p} = x^p e^{j(\omega t+\theta_x^p)} = (x_d^p + jx_q^p)e^{j\omega t} \quad \text{and} \tag{6.17.a}$$

$$\vec{i}_s^{\,p} = i^p e^{-j(\omega t+\theta_i^p)} = (i_d^p + ji_q^p)e^{j\omega t}. \tag{6.17.b}$$

Variables $\vec{x}_s^{\,n}$ and $\vec{i}_s^{\,n}$ denote the negative sequence voltage and current vectors in SF with

$$\vec{x}_s^{\,n} = x^n e^{-j(\omega t+\theta_x^n)} = (x_d^n + jx_q^n)e^{-j\omega t} \quad \text{and} \tag{6.18.a}$$

$$\vec{i}_s^{\,n} = i^n e^{-j(\omega t+\theta_i^n)} = (i_d^n + ji_q^n)e^{-j\omega t}. \tag{6.18.b}$$

Substituting expressions of the positive- and negative- sequence voltage and current vectors (6.17~6.18) into (6.14), we have

$$\begin{bmatrix} \frac{2}{3}P_z \\ \frac{2}{3}P_{zc} \\ \frac{2}{3}P_{zs} \\ \frac{2}{3}q_z \end{bmatrix} = \begin{bmatrix} x_d^p & x_q^p & x_d^n & x_q^n \\ x_q^n & -x_d^n & -x_q^p & x_d^p \\ x_d^n & x_q^n & x_d^p & x_q^p \\ x_q^p & -x_d^p & -x_q^n & x_d^n \end{bmatrix} \begin{bmatrix} i_d^{p*} \\ i_q^{p*} \\ i_d^{n*} \\ i_q^{n*} \end{bmatrix} = \begin{bmatrix} \frac{2}{3}P_z \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{6.19}$$

The first equation in (6.19) determines the active power delivered at the terminal z.

The second and third equations in (6.19) are normally used to nullify the power ripple or output current ripple of the terminal *z*. The fourth equation is employed to regulate the average reactive power at the given terminal. The current commands can be obtained in general by solving (6.19). Eq. (6.19) allows us to view the different power-oriented control methods within a common framework.

Next we will briefly review the different power-oriented control methods in light of the equation (6.19).

Note:

The second and third voltage equations in the matrix of (6.19) can be easily replaced by switching functions *u* (i.e., ($u_d^p \quad u_q^p \quad u_d^n \quad u_q^n$)) due to the relationship $x=uv_{dc}/2$. In this case, the power variables on the left hand of (6.19) will be changed into output current variables. In other words, instead of using *x* as the variables in the matrix of (6.19), switching functions *u* can be used to ensure a constant *dc* output current. The changes do not appear to offer any significant additional advantages. Such methods are essentially the same as the power regulation schemes discussed here and hence they are not further addressed here.

6.2.2.1 Input power control (IPC) method

The IPC method is obtained with *z* denoting supply input terminals (AA') in Fig. 4.1. The ripple power P_{inc} and P_{ins} are nullified at the supply input terminals thus ensuring a constant instantaneous supply input power. The average reactive power is regulated to zero at the supply input terminals to obtain unity VPF operation. The current commands satisfying the above conditions can be found and can be written as

follows [49].

$$\begin{bmatrix} i_d^{p*} \\ i_q^{p*} \\ i_d^{n*} \\ i_q^{n*} \end{bmatrix} = \frac{2P_{in}}{3D} \begin{bmatrix} e_d^p \\ e_q^p \\ -e_d^n \\ -e_q^n \end{bmatrix} \tag{6.20}$$

Here $D = \left[(e_d^p)^2 + (e_q^p)^2 - (e_d^n)^2 - (e_q^n)^2 \right] = (e^p)^2 - (e^n)^2$.

The phasor diagram for this scheme is shown in Fig. 6.2. It may be noticed in the diagram that the current i^p is in phase with the supply input voltage e^p whereas the current i^n is out of phase with the supply input voltage e^n. Therefore, the positive sequential triangle is geometrically similar to the negative sequential triangle.

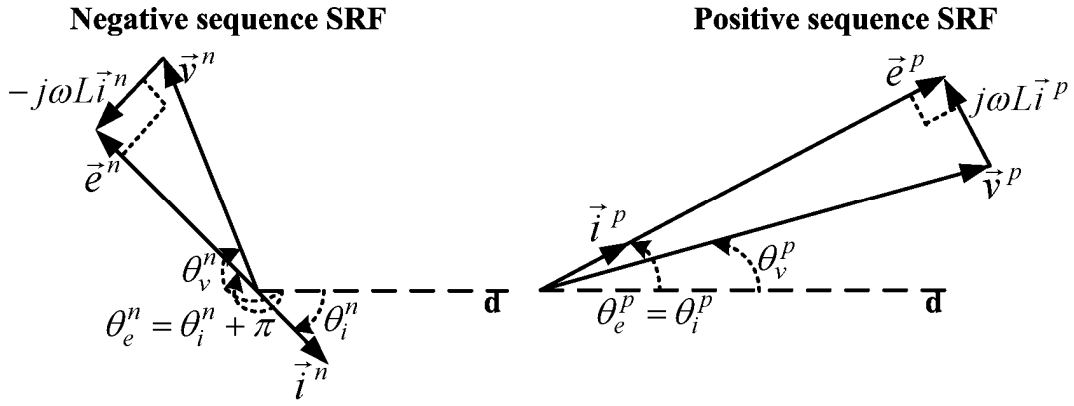


Fig. 6.2 Phasor diagram of the input power control method

The output power of the rectifier (p_{dc}) will be equal to the power at the rectifier input terminals (p_T) if the switch losses are ignored. This power will not be constant because of the non-zero instantaneous power ($P_{Lc,}$ P_{Ls}) in the inductor as mentioned earlier.

6.2.2.2 Output power control (OPC) method

To overcome the ripple output power problem with the IPC scheme, Chapter 4 had proposed and investigated the OPC scheme. In this scheme, z in (6.19) denotes the rectifier input terminals (BB') in Fig. 4.1. By this, the ripple power is nullified at the rectifier bridge input terminals leading to constant output power (assuming constant rectifier losses). The current commands satisfying the above conditions can be found in (4.19).

$$\begin{cases} i_d^{p*} = k_2 \cdot e_d^p + k_1^2 \omega L \cdot e_q^p \\ i_q^{p*} = k_2 \cdot e_q^p - k_1^2 \omega L \cdot e_d^p \\ i_d^{n*} = -k_2 \cdot e_d^n - k_1^2 \omega L \cdot e_q^n \\ i_q^{n*} = -k_2 \cdot e_q^n + k_1^2 \omega L \cdot e_d^n \end{cases}, \tag{6.21}$$

The phasor diagram is shown in Fig. 6.3. It may be noticed that here the current i^p is in phase with the rectifier input voltage v^p whereas the current i^n is out of phase with the rectifier input voltage v^n. Therefore, once again, the positive sequence triangle is geometrically similar to negative sequence triangle.

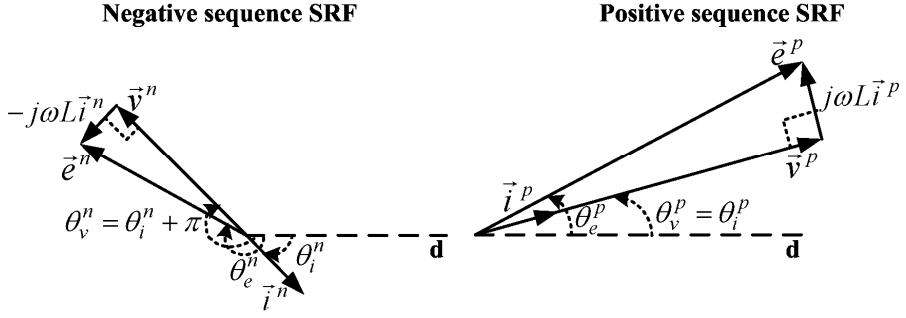


Fig. 6.3 Phasor diagram of the output power control method

The output regulation scheme does effectively eliminate the ripple at the *dc* side. However, the reactive power at the supply input terminals is not directly addressed as discussed in Chapter 4.

6.2.2.3 Partial output power control (POPC) method

It may be noted that the terminal *z* for each of the four power condition equations in (6.19) does not remain the same. This allows one to develop to more control methods using (6.19). One effective option is the POPC method discussed in detail in Chapter 5. Here, the 1st and the 4th equations are satisfied at the supply input terminals (AA'), allowing the required input power to be delivered and eliminating the reactive power. The 2nd and the 3rd equations are then satisfied at the rectifier input terminals (BB') which ensures delivery of ripple free constant power to the output side. The power condition equation based on (6.19) is given below.

$$\begin{bmatrix} \frac{2}{3}P_{in} \\ \frac{2}{3}P_{Tc} \\ \frac{2}{3}P_{Ts} \\ \frac{2}{3}q_{in} \end{bmatrix} = \begin{bmatrix} e_d^p & e_q^p & e_d^n & e_q^n \\ v_q^n & -v_d^n & -v_q^p & v_d^p \\ v_d^n & v_q^n & v_d^p & v_q^p \\ e_q^p & -e_d^p & -e_q^n & e_d^n \end{bmatrix} \begin{bmatrix} i_d^{p*} \\ i_q^{p*} \\ i_d^{n*} \\ i_q^{n*} \end{bmatrix} = \begin{bmatrix} \frac{2}{3}P_T \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{6.22}$$

Another alternative would be a control scheme in which the 1st and the 4th equation are satisfied at the rectifier input terminals and the 2nd and the 3rd equations are satisfied at the supply input terminals. While this may be possible, the resulting scheme will neither result in constant, ripple free, output power nor in zero reactive power at the supply input terminals. Since the scheme does not appear to have any significant merits, this was not pursued in this work.

The phasor diagram of the POPC scheme is shown in Fig. 6.4. As shown in Fig 6.4, the positive sequence current is not in phase with either voltage at the supply input or

voltage at the rectifier input terminals. Likewise, the negative sequence current is also not in phase/out of phase with either voltage at the supply input or voltage at the rectifier input terminals. Therefore, the positive sequence triangle is not geometrically similar to the negative sequence triangle in this case. Due to this, it may not be possible to use supply input voltage to replace rectifier input terminal voltage as has been done in OPC (see Section 4.2.2).

The solution to (6.22) is given below.

$$\begin{bmatrix} i_d^{p*} \\ i_q^{p*} \\ i_d^{n*} \\ i_q^{n*} \end{bmatrix} = \frac{2p_{in}^*}{3|A|} \begin{bmatrix} e_d^p (v^p)^2 - e_q^n (v_d^n v_q^p + v_d^p v_q^n) + e_d^n (v_q^p v_q^n - v_d^n v_d^p) \\ e_q^p (v^p)^2 - e_q^n (v_q^n v_q^p - v_d^p v_d^n) - e_d^n (v_d^p v_q^n + v_d^n v_q^p) \\ -e_q^p (v_d^n v_q^p + v_d^p v_q^n) + e_d^p (v_q^n v_q^p - v_d^p v_d^n) + e_d^n (v^n)^2 \\ -e_q^p (v_q^p v_q^n - v_d^n v_d^p) - e_d^p (v_q^n v_d^p + v_q^p v_d^n) + e_q^n (v^n)^2 \end{bmatrix} , \quad (6.23)$$

where

$$|A| = (e^p)^2 (v^p)^2 + (e^n)^2 (v^n)^2 - 2(e_q^n e_d^p + e_q^p e_d^n)(v_q^n v_d^p + v_q^p v_d^n) + 2(v_q^p v_q^n - v_d^n v_d^p)(e_d^n e_d^p - e_q^n e_q^p)$$

This is the control implemented in [51]. In Chapter 5 this control was implemented based on an improved implementation method using Estimation Method 2.

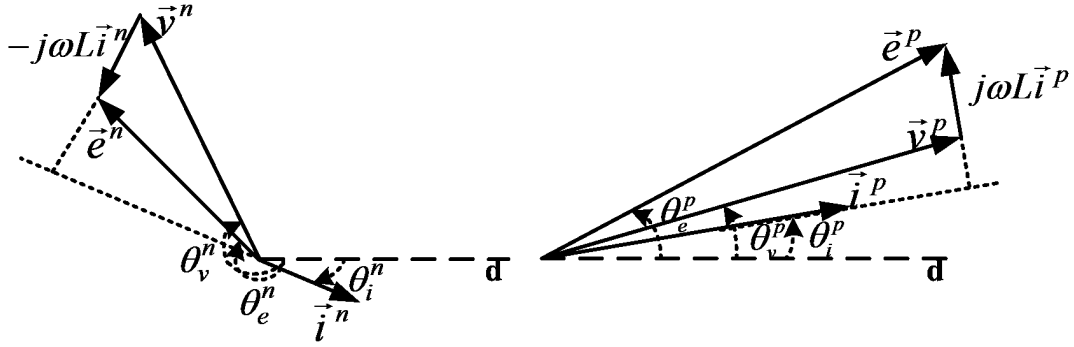


Fig. 6.4 Phasor diagram of the partial output power control method

All of the reported power regulation methods, namely, the IPC method, the OPC method, and the POPC method, can improve both the input side performance and the

output side performance substantially. In the next section, the performances obtainable with these three methods will be compared.

6.3 Investigation of achievable power factor

In this section, the achievable power factors at both the rectifier supply input terminals and the rectifier bridge input terminals are investigated.

6.3.1 Average active and reactive power

The average power across the supply input terminals has been given in (4.22) and reproduced below.

$$P_{in} = \frac{3}{2} e^p i^p \cos(\theta_e^p - \theta_i^p) + \frac{3}{2} e^n i^n \cos(\theta_e^n - \theta_i^n) \tag{6.24}$$

The instantaneous reactive power at the supply input terminals can be expressed as follows.

$$q_{in} = -\frac{3}{2} e^p i^p \sin(\theta_e^p - \theta_i^p) + \frac{3}{2} e^n i^n \sin(\theta_e^n - \theta_i^n) \tag{6.25}$$

These equations will be used in determining the power factors.

6.3.2 Nullifying power ripple

Let us consider the general case of nullifying the ripple active power across a selected set of terminals. To carry out this nullification, the coefficients of *sin (2ωt)* and *cos (2ωt)* of (6.15) should be made zero as follows.

$$p_z = P_z + P_{zc} \cos 2\omega t + P_{zs} \sin 2\omega t \tag{6.26}$$

with

$$P_{zc} = \frac{3}{2}(x^p i^n \cos(\theta_x^p + \theta_i^n) + x^n i^p \cos(\theta_x^n + \theta_i^p)) = 0 \tag{6.27.a}$$

$$P_{zs} = \frac{3}{2}(x^p i^n \sin(\theta_x^p + \theta_i^n) + x^n i^p \sin(\theta_x^n + \theta_i^p)) = 0 \tag{6.27.b}$$

Here, depending on whether z denotes supply input terminals or bridge input terminals, the symbol x can denote either supply input voltage or rectifier bridge input voltage.

Eq. (6.27) can be further simplified as shown below.

$$\begin{cases} \dfrac{i^p}{x^p} = \dfrac{i^n}{x^n} = k_x \\ \theta_x^p - \theta_i^p = \theta_x^n - \theta_i^n \pm n\pi \qquad n = 1,3,5... \end{cases} \tag{6.28}$$

Eq. (6.28) shows the current condition that must be satisfied by all power-oriented control methods discussed in Section 6.2.

6.3.3 Nullifying power ripple at the supply input terminals

In the following discussion, the power ripple is assumed to be nullified at the supply input terminals. Variable x in (6.28) will denote input supply voltage in this case. Substituting (6.28) into (6.24), the constant part of the power, the equivalent current and the effective apparent power S_e at the supply input terminals can be written as shown below.

$$i_e = \frac{k_1}{\sqrt{2}}\sqrt{(e^p)^2 + (e^n)^2} \tag{6.29}$$

$$S_e = 3e_e i_e = \frac{3}{2} k_1((e^p)^2 + (e^n)^2) \tag{6.30}$$

$$P_{in} = \frac{3}{2} k_1[(e^p)^2 - (e^n)^2]\cos(\theta_e^p - \theta_i^p) \tag{6.31}$$

It can be deduced from (6.29) and (6.30) that both the equivalent current and the effective apparent power reach their minimum values when the value of the variable k_1 is minimized.

For a given active power P_{in} and supply voltage (e^p, e^n), k_1 reaches its minimum value if and only if the condition

$$\theta_i^p = \theta_e^p \tag{6.32}$$

is satisfied based on (6.31).

Therefore, the resultant minimum value of variable k_1 is

$$k_1 = \frac{2p_{in}}{3[(e^p)^2 - (e^n)^2]} \tag{6.33}$$

With the minimum k_1, the amplitudes of i^p and i^n reach their minimum values based on (6.28). With minimum input current values, the effective apparent power S_e (6.30) reaches its minimum value for the given supply input voltage and active power. Therefore, we infer that the resultant EPF is maximum when constant power is delivered across the supply input terminals.

$$P_{FE} = \frac{\frac{3}{2} k_1[(e^p)^2 - (e^n)^2]}{\frac{3}{2} k_1((e^p)^2 + (e^n)^2)} = \frac{1-\mu^2}{1+\mu^2} \tag{6.34}$$

Here $\mu=e^n/e^p$.

Next, the achievable VPF when nullifying power ripple at the supply input terminals is investigated.

With the condition $\theta_i^p = \theta_e^p$ and also the condition given in the second equation in (6.28), it can be deduced that zero average reactive power operation is achieved based on (6.25). This, in turn, provides unity VPF operation based on (6.2).

Eq. (6.28), (6.32) and (6.33) result in the same control algorithm as the IPC scheme (see Section 6.2.2.1). Therefore, the above analysis indicates that the input power control method (IPC) theoretically yields the best EPF and unity VPF while maintaining constant power delivery to the output side among the power regulation schemes which aim to nullify the power ripple at the input supply terminals. Eq. (6.34) allows us to estimate the value of this effective power factor. It may be noted that the achievable EPF is directly linked to the degree of supply imbalance μ.

6.3.4 Nullifying power ripple at the rectifier bridge input terminals

This has been carried out in both the OPC and the POPC schemes. Variable x will denote the rectifier bridge input voltage in this case. Substituting (6.28) into (6.24), the constant part of the power at the rectifier bridge input terminals can be written as shown below.

$$P_T = \frac{3}{2}k[(v^p)^2 - (v^n)^2]\cos(\theta_v^p - \theta_i^p) \tag{6.35}$$

As the average active power stored in three-phase inductor is zero, the constant part of the power at the rectifier bridge input terminals is equal to the constant part of the

power at the supply input terminals which gives the following relationship.

$$P_T = P_{in} = \frac{3}{2} e^p i^p \cos(\theta_e^p - \theta_i^p) + \frac{3}{2} e^n i^n \cos(\theta_e^n - \theta_i^n) \tag{6.36}$$

As both the VPF and the EPF should be evaluated at the supply input terminal, it may not be possible in the cases of OPC and POPC to find the best obtainable power factor with the help of (6.28) as was done in the case of the IPC method.

Next, the VPFs and the EPFs obtainable with the OPC and POPC schemes are discussed and evaluated.

The actual VPFs achieved in the case of the OPC and POPC methods are dependent on the 4th equation in (6.19) which determines the amount of reactive power across the selected terminals.

The VPF for both the OPC and the POPC schemes can be obtained based on (6.1). With the OPC method, the obtained VPF can be further simplified as

$$P_{FV} = \frac{P_{in}}{\sqrt{P_{in}^2 + \bar{q}_{in}^2}} = \cos(\theta_e^p - \theta_i^n) \tag{6.37}$$

The derivation of (6.37) has been given in Section 4.2.4 of Chapter 4.

On the other hand, the theoretical VPF with the POPC method is unity as we are controlling the average input reactive power (q_{in}) to be zero in this method.

The EPF with both the OPC and the POPC schemes can be obtained based on (6.8). Substituting (6.36) and (6.28) into (6.8), the EPF with the OPC and the POPC schemes can be expressed as given below.

$$P_{FE} = \frac{P_{in}}{S_e} = \frac{P_T}{S_e} = \frac{\frac{3}{2}k[(v^p)^2 - (v^n)^2]\cos(\theta_v^p - \theta_i^p)}{\frac{3}{2}\sqrt{(i^p)^2 + (i^n)^2}\sqrt{(e^p)^2 + (e^n)^2}}$$
$$= \frac{[(v^p)^2 - (v^n)^2]\cos(\theta_v^p - \theta_i^p)}{\sqrt{(v^p)^2 + (v^n)^2}\sqrt{(e^p)^2 + (e^n)^2}} \quad (6.38)$$

Here, assuming inductor loss to be zero $P_{in} = P_T$. With the OPC scheme, the EPF expression in (6.38) can be further simplified using this assumption $P_{in} = P_T$ as shown below.

With the relationship $\cos(\theta_e^p - \theta_i^p) = -\cos(\theta_e^n - \theta_i^n)$ given in (4.23.b), the average input active power is

$$P_{in} = \frac{3}{2}(e^p i^p - e^n i^n)\cos(\theta_e^p - \theta_i^p) \quad (6.40)$$

Using the relationship $\frac{e^n}{e^p} = \frac{i^n}{i^p}$ given in (4.15), the EPF expression for the OPC case can be obtained as given below.

$$P_{FE} = \frac{P_{in}}{S_e} = \frac{\frac{3}{2}(e^p i^p - e^n i^n)\cos(\theta_e^p - \theta_i^p)}{\frac{3}{2}\sqrt{(i^p)^2 + (i^n)^2}\sqrt{(e^p)^2 + (e^n)^2}}$$
$$= \frac{1-\mu^2}{1+\mu^2}\cos(\theta_e^p - \theta_i^p) \quad (6.41)$$
$$= \frac{1-\mu^2}{1+\mu^2}P_{FV}$$

Here $\mu = e^n / e^p$ specifies the extent of imbalance.

It can be seen from (6.41) that the obtained EPF with the OPC scheme is related to

the imbalance ratio μ of the supply input voltage as well as the obtained VPF value (= P_{FV}).

It was found difficult to simplify the EPF expression given in (6.38) in a similar manner for the POPC scheme as the positive sequence triangle is not geometrically similar to the negative sequence triangle in this scheme as discussed in Section 6.2.2.3. Furthermore, eq. (6.38) does not give much insight into the determining factors of the EPF value as does (6.41) for the OPC case. In addition, it was found that it is not straightforward to evaluate the POPC scheme's EPF with (6.38) because additional computations are needed to calculate the values of the variables (θ_v^p θ_i^p). These computations are not necessary for the actual control scheme implementation.

Due to these reasons, it was found more convenient to use directly the EPF definition given in (6.8) and use simulation data to evaluate the EPF value in the case of the POPC scheme.

The VPF and EPF values obtained with the OPC and POPC schemes are summarized in Table 6.4.

6.3.5 Power factor with the voltage-oriented control method

As indicated in (6.13.d), for the VOC scheme, the average reactive power is zero. This indicates that the VPF value will be unity.

$$P_{FV} = \frac{P}{S_V} = 1 \tag{6.42}$$

As may be noticed from the discussions in Sections 6.3.3 and 6.3.4, the effective power factors for the IPC, OPC and the POPC methods are all not unity. From the

analysis of the VOC scheme in Section 6.2.1, the effective power can be determined as follows:

$$P_{FE} = \frac{P}{S_e} = \frac{\frac{3}{2}k[(e^p)^2 + (e^n)^2]}{\frac{3}{2}\sqrt{(e^p)^2 + (e^n)^2}\sqrt{(i^p)^2 + (i^n)^2}} = 1 \tag{6.43}$$

The EPF in this case is unity, thereby indicating that this method can theoretically provide the best input side performance, with in-phase currents and unity EPF, for a three phase PWM rectifier operating under unbalanced supply conditions. But the presence of the large output side ripple makes the method impractical for most cases except those where a large output voltage ripple can be tolerated.

6.3.6 Evaluation of achievable power factors

To evaluate the power flow conditions with the different control methods, the VPF and EPF values of the schemes have been calculated and are summarized in Table 6.4.

It can be seen from Table 6.4 that except the OPC scheme, all the other three schemes can achieve unity VPF operation. Even in the case of the OPC scheme, as discussed in Section 4.2.4, the power factor obtained with the OPC method will be almost unity. Therefore, unity or near unity VPF can be achieved with all of the four control schemes.

As can be seen in Table 6.4, with the VOC method, the achievable EPF is unity, the highest value possible. In the case of the IPC method, the achievable EPF is less than unity and will depend on the degree of imbalance in the supply voltage. This value is the best achievable value while delivering ripple free power to the output side. In the case of

the OPC method, the achievable EPF is less than unity and will depend on both the degree of imbalance in the supply voltage and the achievable VPF. As discussed earlier, in the case of the POPC method, the expression of the EPF does not give much insight into the determining factors **o**f the EPF value.

In summary, Table 6.4 shows the theoretical achievable power factor values with the VOC and the IPC schemes, while in the case of the OPC scheme, the expression given shows the factors that determine the achievable EPF. However, the theoretical expression for EPF in the case of POPC does not give much insight.

Though Table 6.4 provides the expressions for the power factor values, still it is not easy to compute the theoretical power factor values (both VPF and EPF for the OPC scheme and EPF for the POPC scheme) using these expressions from the measured variables. This is because, as stated in Section 6.3.4 and Section 4.3, the values of variables (θ_e^p θ_i^p) required for the OPC scheme and the values of variables (θ_v^p θ_i^p) needed for the POPC scheme require fairly involved computations.

On the other hand, it is more convenient to use the vector power factor and effective power factor definitions given in (6.1) and (6.8) for power factor calculation. Therefore, it is suggested that the power factor computations are carried out by performing system simulations and then using the original definitions for calculations.

Here, the power factor computations are carried out in two ways. In both ways, system simulations are performed first. In the first method, the data from the simulations are used in the original power factor definitions given in (6.1) and (6.8) to evaluate the power factor values (Table 6.5). In the second method, the data from simulations are

used in the expressions in Table 6.4 in order to evaluate the power factor values (Table 6.6). In this manner, the results of the theoretical analysis presented in Table 6.4 are verified.

The system parameters used in the simulations were L = 4 mH and R_{dc} = 45 Ω. The power reference used for the calculations was set as 889W ($=v_{dc}^2/R_{dc}$) with v_{dc}=200V. In the simulation, the supply voltages were set at $42\sqrt{2}\sin(\omega t+355^\circ)$ V, $75\sqrt{2}\sin(\omega t+236^\circ)$ V and $66\sqrt{2}\sin(\omega t+90^\circ)$ V and the current references were calculated using (6.9), (6.20), (6.21) and (6.23). With the current references and the supply input voltages, the resulting active power, reactive power, vector apparent power and effective apparent power can be obtained from the simulation results. The power factors are then calculated based on (6.1) and (6.8). Table 6.5 summarizes the power factor values which were obtained using the original definition given in (6.1) and (6.8).

Next the power factor values are calculated using the expressions derived for them which are given in Table 6.4. Here, besides current references calculated using (6.9), (6.20), (6.21) and (6.23), additional data such as angles of supply voltages, current and rectifier bridge input terminal voltages were all obtained from simulation results. The extent of imbalance μ is 0.33. The positive sequence angles for supply voltage θ_e^p and supply current θ_i^p for the OPC method are -13^o and -19.7^o. Therefore, the calculated the VPF and the EPF values of the OPC method are 0.993 and 0.795. Likewise, the positive sequence angle for rectifier bridge terminal voltage θ_v^p and supply current θ_i^p for the POPC method are -19.6^o and -14.2^o. The amplitude of the supple voltage (e^p e^n) and

rectifier bridge terminal voltage (v^p v^n) are 84.84V, 28.28V, 85.12V and 27.8V. Using the EPF expression of the POPC method, the EPF value of the POPC method is 0.8089. Table 6.5 summarizes the above power factor values which were obtained using the VPF and EPF expression given in Table 6.4.

It can be seen from Table 6.5 and Table 6.6 that the obtained VPF and EPF values for all the control schemes are almost the same which verifies the correctness of the VPF and EPF expressions given in Table 6.4. It can be also seen from Table 6.5 and Table 6.6 that the values of VPF for the VOC scheme, the IPC scheme and the POPC scheme are unity. As expected, the EPF value with the VOC scheme was unity. Correspondingly, the equivalent RMS current value of the VOC method is also the lowest for this scheme. The three power control methods all have similar equivalent RMS currents and EPF values, with the POPC method providing the best EPF value among the three schemes.

TABLE 6.4 CALCULATED VPF AND EPF VALUES

	VOC scheme	IPC scheme	OPC scheme	POPC scheme
VPF	1	1	$\cos(\theta_e^p - \theta_i^p)$	1
EPF	1	$\frac{1-\mu^2}{1+\mu^2}$	$\frac{1-\mu^2}{1+\mu^2}\cos(\theta_e^p - \theta_i^p)$	$\frac{[(v^p)^2-(v^n)^2]\cos(\theta_v^p - \theta_i^p)}{\sqrt{(v^p)^2+(v^n)^2}\sqrt{(e^p)^2+(e^n)^2}}$

TABLE 6.5 SIMULATION BASED COMPARISON OF POWER FACTORS WITH DIFFERENT CONTROL METHODS USING ORIGINAL POWER FACTOR DEFINITIONS

	VOC scheme	IPC scheme	OPC scheme	POPC scheme
i_a(RMS)	3.083	7.333	7.454	7.327
i_b(RMS)	5.648	4.333	4.76	4.705
i_c(RMS)	4.947	5.512	5.113	5.068
Equivalent RMS current (A)	4.686	5.858	5.898	5.817
P_{in}	889	889	889	889
Q_{in}	0	0	-104.9	0
S_V	889	889	895.2	889
VPF	1	1	0.993	1
S_E	889.05	1111.2	1119	1099.7
EPF	1	0.8	0.795	0.8084

TABLE 6.6 SIMULATION BASED COMPARISON OF POWER FACTORS WITH DIFFERENT CONTROL METHODS USING EQUATIONS GIVEN IN TABLE 6.4

	VOC scheme	IPC scheme	OPC scheme	POPC scheme
VPF	1	1	0.993	1
EPF	1	0.8	0.795	0.8089

In the next section, the experimental results with all of the different control methods will be presented and their relative performances discussed. As indicated earlier in Section 6.1, the concept of VPF is useful in assessing potential system power losses associated with reactive power alone whereas the concept of EPF is useful in assessing potential system power losses due to both reactive power and supply voltage imbalance. Due to the greater generality of the EPF concept, only EPF will be calculated to evaluate power flow condition in the experimental results.

6.4 Experimental results with the different control methods

In Chapters 4 & 5, the experimental implementation of the IPC method, the OPC method and the POPC method have all been discussed and a few basic results have been presented. In this section, their detailed performances are all presented and evaluated. The VOC scheme was also implemented and included in this comparison since this is the only scheme capable of achieving unity EPF under unbalanced operating conditions.

The overall control scheme and the voltage loop PI control parameters used were the same for each of these methods; the only difference was in the current-commands generation law employed. To calculate the current-commands, (6.9) was used in the VOC scheme, (6.20) in the IPC scheme, (6.21) in the OPC scheme and (6.22) in the POPC scheme. The dual current control scheme presented earlier in Sec. 4.2.3 has been adopted for current control in all the cases. The detailed control block diagram has been shown earlier in Fig. 4.5. The supply voltages for the experiments were again set at $42\sqrt{2}\sin(\omega t + 355^\circ)$ V, $75\sqrt{2}\sin(\omega t + 236^\circ)$ V and $66\sqrt{2}\sin(\omega t + 90^\circ)$ V as in Chapters 4 and 5.

The experimental waveforms of the *dc* output voltage, the three-phase currents, the input power and the output power with the VOC scheme are shown in Fig. 6.5. Here, the input power was calculated using the measured three-phase currents and three-phase voltages using

$$p_{in} = e_a \cdot i_a + e_b \cdot i_b + e_c \cdot i_c . \tag{6.44}$$

The output power was calculated using the measured *dc* output voltage and *dc*

output current with

$$p_{dc} = v_{dc} \cdot i_{dc} . \tag{6.45}$$

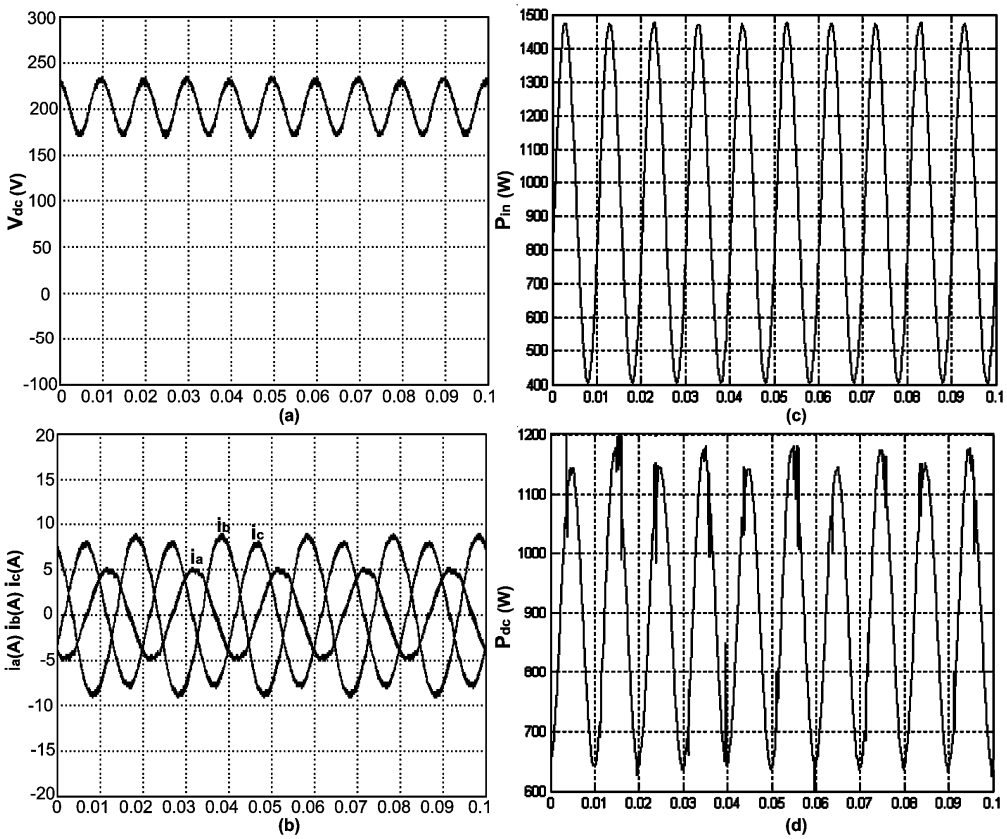


Fig. 6.5 Experimental waveforms with unbalanced supply: (a) output voltage (b) three-phase currents (c) input power (d) output power – the VOC method

The same approach was used for input power and output power calculations for all the control methods.

As shown in Fig. 6.5(b), the three-phase currents are sinusoidal but unbalanced. In this method, the amplitudes of three-phase currents are proportional to their corresponding voltages with no phase shifts between currents and the corresponding voltages. As expected, there is a very substantial second harmonic ripple in the *dc* output voltage, the input power and the output power.

The waveforms with the IPC method are shown in Fig. 6.6. As discussed earlier in Chapter 2, in the IPC method, the ripple power in the inductors is ignored, and this results in ripple power appearing on the *dc* side causing an even harmonic ripple in the *dc* output voltage which can be seen from 6.6(a).

Contrary to expectations, the input power in Fig. 6.6(c) is not in fact constant with the input power control method. Instead, the input power is also seen to have a large ripple. This phenomenon may be explained as follows.

The large output power ripple results in a ripple in the *dc* output voltage, which in turn causes a ripple to appear in the output of the voltage controller, which is the input power command signal P_{in}^{*} in this case. Thus, the reference value of P_{in}^{*} itself is not constant and the current commands calculated with this P_{in}^{*} will not also be constant under steady-state as expected. Even though the input power control method aims to draw constant input power from the *ac* supply, the ripple in P_{in}^{*} prevents this from being achieved (see Fig. 6.6(c)). Thus, neither a constant input power nor a constant output power is maintained in this scheme, in practice. One can mitigate this problem by using a large *dc* output capacitor. As an example, a relatively large capacitance (2200 μF) has been employed in [49]. Alternatively, the voltage controller can be made very slow in order to reduce the ripple in P_{in}^{*}. However, either of the approaches will result in a very slow voltage loop performance and undermine the intrinsic advantage of a PWM rectifier.

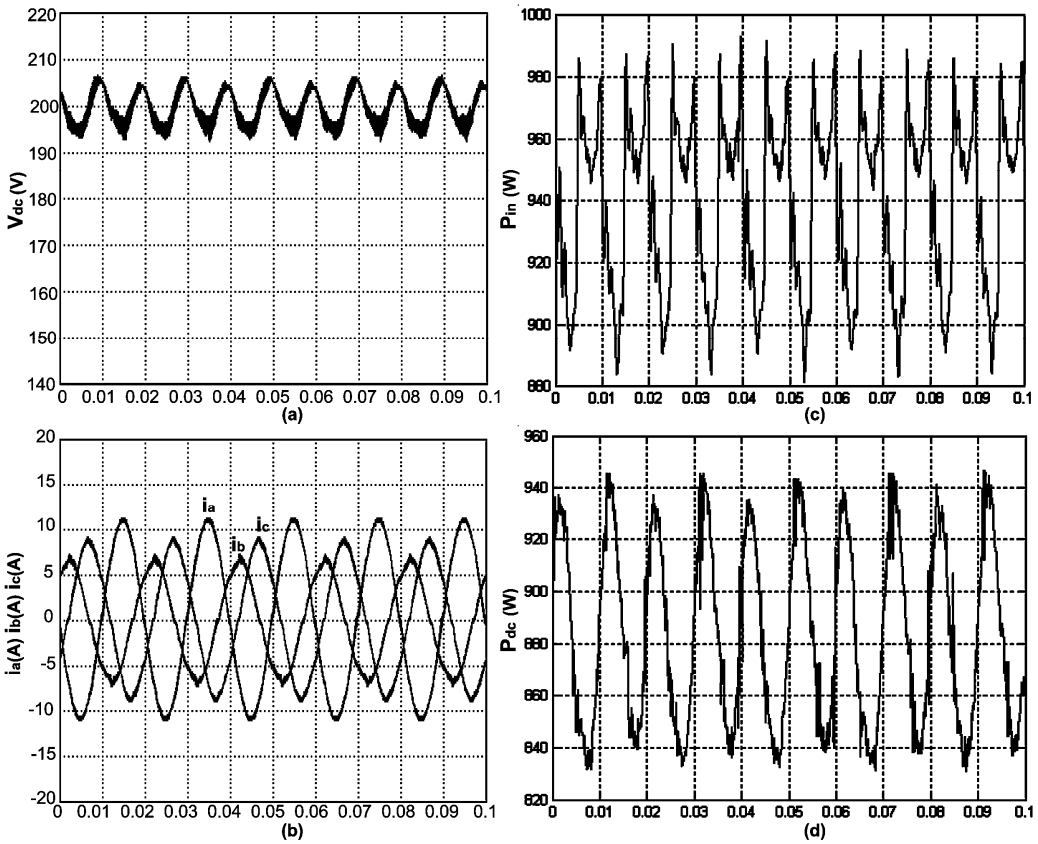


Fig. 6.6 Experimental waveforms with unbalanced supply: (a) output voltage (b) three-phase currents (c) input power (d) output power –the IPC method

The waveforms with the POPC and the OPC methods are shown in Fig. 6.7 and Fig. 6.8, respectively. As shown in Figs. 6.7(c) & 6.8(c), the instantaneous input power with either of the output power control methods is not constant but has a second harmonic component at 100 Hz. However, the corresponding *dc* power (Fig. 6.7(d) & Fig. 6.8(d)) and the *dc* output voltage (Fig. 6.7(a) & Fig. 6.8(d)) are both nearly constant, as would be expected in methods aiming to nullify ripple power at the rectifier bridge input terminals.

The peak to peak ripple in the *dc* output voltage, the measured THDs of the three-phase line currents, and the experimental EPF values obtained with these control methods are summarized in Table 6.7. The EPF values were calculated using (6.8).

Among these control methods, the VOC method, as expected, provides excellent input side performance with a high EPF value (0.955 against the theoretical value of unity) and good input current quality. The equivalent input RMS current is only 5.158 A, which is the lowest among all of the control methods studied. However, as expected, the output performance is very poor as can been seen from Fig. 6.5 (b) and also Table 6.7 (output ripple voltage). This makes the method not practically useful except in those few applications where input side performance is paramount and such large output power and voltage ripple can be tolerated.

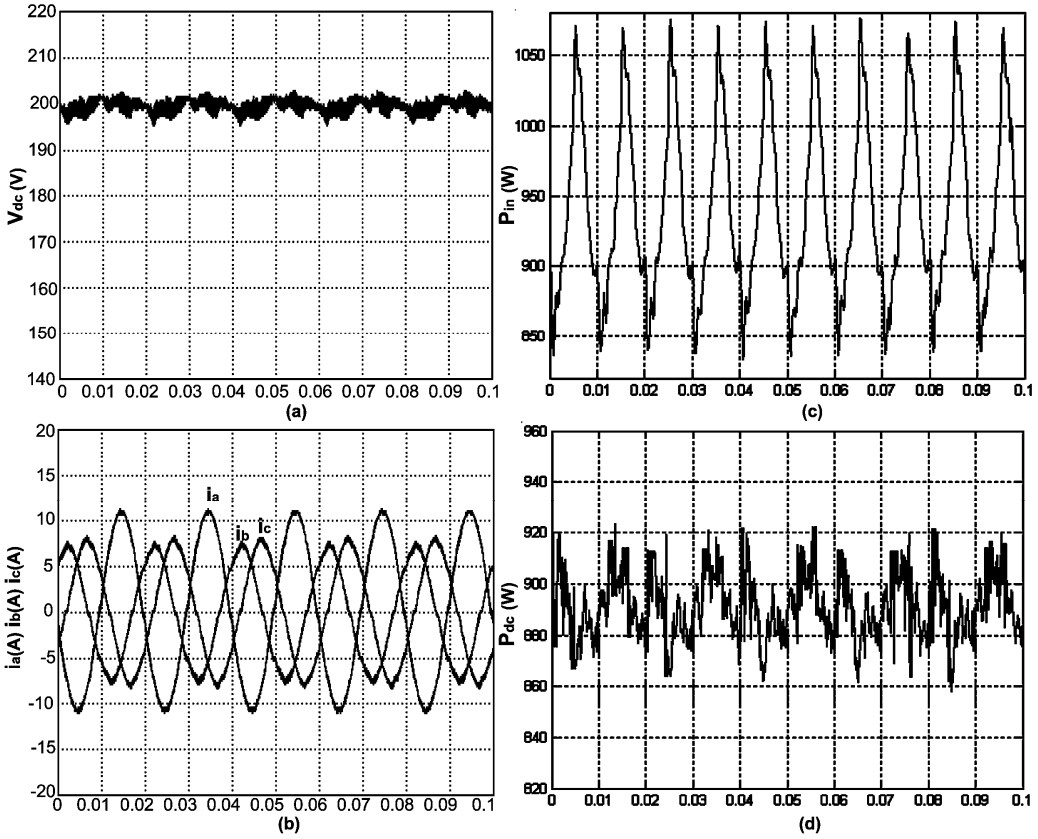


Fig. 6.7 Experimental waveforms with unbalanced supply: (a) output voltage (b) three-phase currents (c) input power (d) output power – the POPC method (with Estimation Method 2)

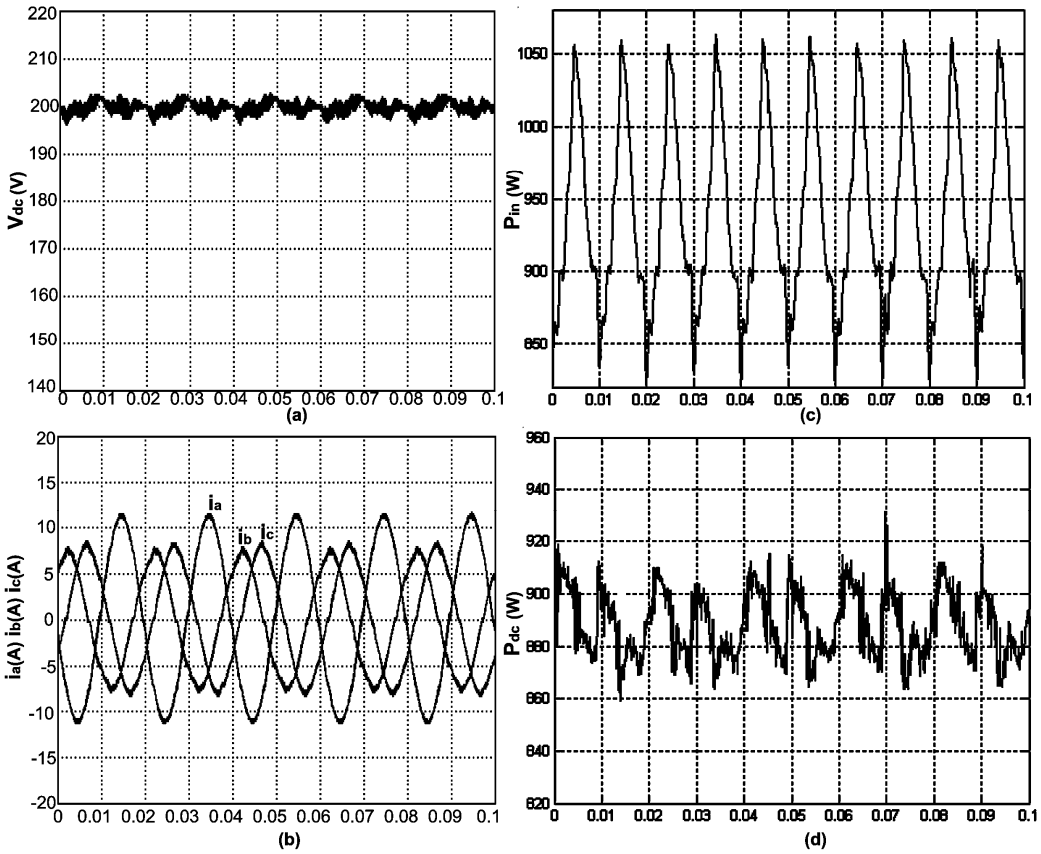


Fig. 6.8 Experimental waveforms with unbalanced supply: (a) output voltage (b) three-phase currents (c) input power (d) output power – the OPC method

TABLE 6.7 EXPERIMENTAL PERFORMANCE WITH DIFFERENT CONTROL SCHEMES

		VOC scheme	IPC scheme	OPC scheme	POPC scheme
p-p ripple of *dc* output voltage (V)		59.4	10.6	3.72	4.0
THDs of currents	a-ph	3.99%	2.18%	2.02%	1.99%
	b-ph	3.55%	4.9%	4.95%	4.8%
	c-ph	3.74%	5.01%	4.95%	4.88%
RMS values of currents	a-ph	3.463	7.692	7.819	7.618
	b-ph	6.198	4.62	5.114	5.047
	c-ph	5.424	5.946	5.443	5.384
Equivalent RMS current (A)		5.158	6.215	6.243	6.124
EPF		0.955	0.796	0.792	0.806

On the other hand, the POPC method and the OPC method can provide similar input and output side performances. Even though both the OPC method and the POPC method can provide the same output side performances theoretically, the peak to peak voltage ripple on the *dc* output voltage with the OPC method is slightly smaller than that

with the POPC method. This may be attributed to the fact that the current commands calculated with measured supply voltages in the OPC method are likely to be more accurate than the current commands calculated with the estimated values of rectifier bridge input voltages in the POPC method. The POPC method (with the Estimation Method 2) provides the best input side performance with the lowest effective RMS current and the highest EPF among three power regulation methods. However, as may be seen from Table 6.7, the differences among the three power-oriented control methods with regard to the input side performance are quite small.

In addition, as discussed in Chapter 5, the stability robustness range for the POPC method with Estimation Method 2 has not been investigated. This somewhat reduces the confidence level in the usage of the POPC method for different input supply and load conditions. On the other hand, the OPC method as implemented in Chaper 4 does not possess any stability robustness issues as discussed in Chapter 5. Therefore, the OPC method is a better choice currently for achieving high performance on both input and output sides under unbalanced operating condition.

It may be noted from results given in Table 6.7 that with the dual current control scheme adopted, the distortions of the line currents become high when the amplitudes of the currents are small. Excellent input side performance includes achieving high quality sinusoidal input currents. This leads to the work on high performance *ac* current tracking schemes which aim to improve the quality of the input current waveforms particularly at low current magnitudes discussed in Chapter 7.

TABLE 6.8 COMPARISON OF DIFFERENT POWER REGULATION SCHEMES

	IPC scheme [47], [48]	OPC scheme (Chapter 4)	POPC scheme [50], [51] with Estimation Method 2 (Chapter 5)
Power condition equations	$\begin{cases} \overline{p}_{in} = P_{in}^{*} \\ \tilde{p}_{in} = 0 \\ \overline{q}_{in} = 0 \end{cases}$	$\begin{cases} \overline{p}_{T} = P_{T}^{*} \\ \tilde{p}_{T} = 0 \\ \overline{q}_{T} = 0 \end{cases}$	$\begin{cases} \overline{p}_{in} = P_{in}^{*} \\ \tilde{p}_{T} = 0 \\ \overline{q}_{in} = 0 \end{cases}$
Input Performance	Difficult to achieve excellent input side performance practically. Input current distortion if output is tightly regulated.	Excellent input side performance with nearly optimal EPF and nearly unity VPF. Performance practically achievable.	Practically the best input side performance with the best achievable EPF and unity VPF.
Output performance	Large second harmonic ripple on the *dc* side requiring a large output capacitor.	Low ripple in the *dc* output voltage	Low ripple in the *dc* output voltage
Realization issues	Only supply voltage needed for current reference generation and no realization issue.	Only supply voltage needed for current reference generation and no realization issue.	The rectifier bridge terminal voltage needed to be estimated for current reference generation. Stability robustness over the range of operation for the Estimation Method 2 implementation to be established.

Table 6.8 provides a summary of the salient features of the three power-oriented control methods and compares their relative merits. As may be noticed, overall, both the OPC method and the POPC method have the important merits of low output *dc* voltage ripple and sinusoidal *ac* input current waveforms with high EPF values. The stability robustness range of the POPC method with Estimation Method 2 implementation is yet to be established.

6.5 Conclusions

In this chapter, the performances of the various power regulation methods for the PWM rectifier under unbalanced operation have been compared. The concept of EPF

available in literature was introduced and shown to be superior in evaluating the input side performances of the PWM rectifier under unbalanced supply. Besides the three power regulation methods (IPC, OPC and POPC), a new VOC method capable of excellent input side performance was also introduced. The four control schemes were evaluated by comparing both input side and output side performances. The values of the THDs of the input currents, the peak-to-peak ripple of the *dc* output voltage and the EPF values were all used in this evaluation. It was found that both the output power control method and the partial output power control method can provide excellent input side and output side performances. However, the stability robustness range of the POPC method with Estimation Method 2 implementation is yet to be established. Due to this, it is suggested that the OPC method is currently a better choice.

With the dual current control scheme adopted for current control, the distortion in the line currents is seen to become high when the amplitudes of the currents are small. In order to improve the input side performance with regard to the quality of the input current, current tracking schemes capable of achieving low input side current distortion are investigated in the next chapter.

CHAPTER 7
CURRENT TRACKING SCHEMES FOR THE THREE-PHASE BOOST-TYPE PWM RECTIFIER

7.0 Introduction

Under unbalanced supply voltages, the line current magnitudes and phase will have to be adjusted such that constant instantaneous power is transferred to the *dc* side in order to achieve good output performance. According to symmetrical component theory, this will result in unbalanced *ac* line currents which have both positive and negative sequence components.

The dual current controller has been implemented [49] to regulate positive sequence currents in positive sequence SRF and negative sequence currents in negative sequence SRF separately. Such a dual current controller has been used in the present work so far in Chapters 4, 5 & 6. Such a control scheme does simplify the tracking problem to a pure *dc* command regulation problem. However, the scheme requires four separate PI current controllers besides feed forward and decoupling elements. In addition, in order to regulate positive- and negative-sequence components separately, sequence component extracting filters are required to be employed which undermine the overall regulator bandwidths and stability margins [52]. It was also found in the experimental results given in Table 6.6 of Chapter 6 that the distortion of the line currents becomes very high when the amplitudes of the currents are small.

On the other hand, it is noted that both positive- and negative- sequence components become 50 Hz *ac* terms in the stationary frame (SF) of reference. If the currents are controlled in SF, the control task becomes a 50Hz *ac* command tracking problem under unbalanced supply operation. Only two current controllers will be required and extraction of sequence components will also not be needed. Thus, it would be advantageous to develop a high performance *ac* tracking controller in SF which can achieve zero steady-state error while tracking the input currents according to the desired 50 Hz waveforms.

Recently, an *ac* current tracking controller, called P+Resonant control, has become popular and has been successfully applied to current control in a three-phase PWM rectifier [74, 75]. The controller can theoretically provide infinite gain at the line frequency which allows it to minimize steady-state tracking error of *ac* reference signals.

It was mentioned in Chapter 2 that the integral variable structure control (IVSC) has the potential merits of both zero steady-state error operation offered by traditional integral control and robustness to parameter variation and system disturbances offered by variable structure control (VSC). Thus, it is also a good candidate for implementing the tracking current controller for the PWM rectifier.

Likewise, it was also mentioned in Chapter 2 that the iterative learning control (ILC) based hybrid current control has the merits of both fast dynamic response due to the inclusion of the conventional feedback controller and high precision tracking

ability due to the inclusion of the learning controller. Thus, this control approach also has the potential for implementation as the high performance tracking controller in a PWM rectifier system.

Therefore, both integral variable structure control (IVSC) and iterative learning control based hybrid current control (Hybrid ILC) have the potential to provide the required high *ac* current tracking performance during both steady-state and transient operations. Thus, the aim of the present chapter is to apply the IVSC and the Hybrid ILC based *ac* current control to a three-phase PWM rectifier system and then to evaluate their performances with the P+Resonant controller (P+RC) as the benchmark controller. Comparison is also made with the dual PI current controller (DPIC) presented in Chapter 4 as it has been widely used in research on PWM rectifiers under unbalanced operating conditions.

The organization of this chapter is as follows. Firstly, the system model of a PWM rectifier is presented in the α-β stationary frame using voltage equations, transfer functions and sampled-data state space model. Thereafter, the three *ac* current tracking control schemes: P+RC scheme, IVSC scheme, Hybrid ILC scheme are introduced and their design methods presented.

Experimental results with the proposed control techniques and the bench mark controllers conducted on a 1 kW laboratory prototype PWM rectifier are then presented and discussed. To evaluate the performance with these current control schemes, experiments are first carried out with only the current loop closed and then

with both the current loop and the voltage loop closed. The experimental results show that the Hybrid ILC scheme provides the best steady-state performance among these controllers with good transient performance. Therefore, detailed experimental results of the proposed Hybrid ILC scheme are presented to show the effectiveness of this current control approach.

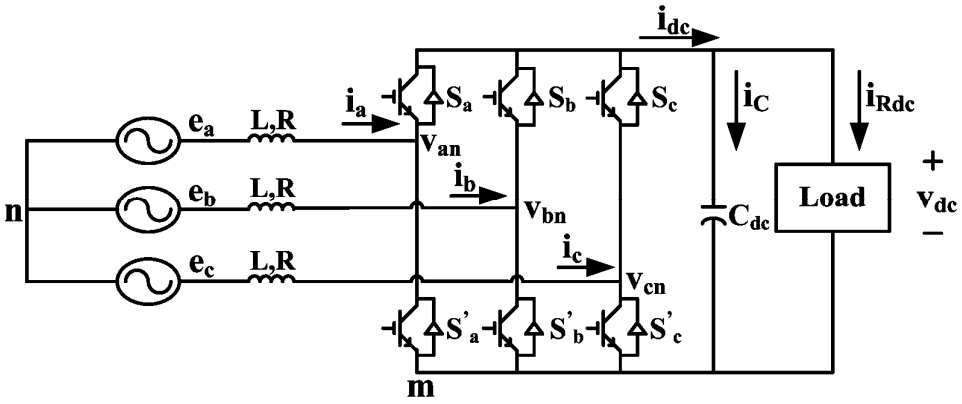


Fig. 7.1 Structure of a three-phase boost-type PWM rectifier

7.1 System model of a PWM rectifier

The voltage-source type PWM rectifier is shown in Fig. 7.1. Here, e_a, e_b, and e_c represent the source voltages and i_a, i_b, and i_c represent the input currents. Parameters L and R are the inductance and parasitic resistance values of the synchronous inductance. As mentioned in Chapter 2 Section 2.1.2, the system equations of a three-phase PWM rectifier in the *a-b-c* frame can be converted into a decoupled system through *a-b-c* to *α-β* transformation as follows:

$$\begin{cases} L\dfrac{di_\alpha}{dt} = e_\alpha - Ri_\alpha - u_\alpha \dfrac{v_{dc}}{2} \\ L\dfrac{di_\beta}{dt} = e_\beta - Ri_\beta - u_\beta \dfrac{v_{dc}}{2} \end{cases}, \tag{7.1}$$

where i_α , i_β and e_α , e_β are the α-axis and β-axis currents and voltages, respectively. Variables u_α and u_β are the α-axis and β-axis control efforts, respectively, and v_{dc} denotes the *dc* output voltage.

7.1.1 Transfer function of current loop

The system equation relating the input current and the control effort can be written as

$$i_{\alpha,\beta}(s) = -\frac{v_{dc}/2}{Ls+R} \times u_{\alpha,\beta}(s) + \frac{e_{\alpha,\beta}}{Ls+R} = G(s) \times u_{\alpha,\beta}(s) + D(s) \tag{7.2}$$

Here, $G(s) = \frac{v_{dc}/2}{Ls+R}$ is the system transfer function. The *dc* output voltage v_{dc} is assumed to be constant. The function *D(s)* is dependent on the system input voltage and can be viewed as the system disturbance.

The corresponding transfer functions *G(z)* and *D(z)* in *z*-domain can be found using *z*-transformation.

7.1.2 Sampled-data state space model

The sampled-data state equations can be obtained from (7.1) as follows:

$$i_s(k+1) = a \cdot i_s(k) + b \cdot (e_s(k) - \frac{v_{dc}}{2} u_s(k)) \quad , \tag{7.3}$$

where $a = \exp(-\frac{R}{L} T_s)$, $b = \frac{1-a}{R}$ with T_s being the switching/sampling period and s could represent α or β.

Defining $\tilde{i}_s(k) = i_s(k) - i_s^*(k)$, the error equations in discrete-time system can be written as:

$$\tilde{i}_s(k+1) = a \cdot \tilde{i}_s(k) + b \cdot e_s(k) - i_s^*(k+1) + a \cdot i_s^*(k) - \frac{v_{dc}}{2} \cdot b \cdot u_s(k), \tag{7.4}$$

where $i_s^*(k)$ is the reference current, $\tilde{i}_s(k)$ is the error between the actual and reference currents and s could represent α or β.

It has been shown in [79, 80] that variable structure control will result in steady-state error in the sliding mode dynamics. Therefore, the concept of integral augmentation borrowed from linear control theory has been introduced in variable structure control [79] to minimize steady-state error. In order to do this, let us define an additional state as follows:

$$z_s(k+1) = z_s(k) + T_s \cdot \tilde{i}_s(k), \tag{7.5}$$

where $z_s(k+1)$ is the integration of $\tilde{i}_s(k)$ and s could represent α or β.

The state space representation with integral augmentation is then given by

$$\begin{bmatrix} z_s(k+1) \\ \tilde{i}_s(k+1) \end{bmatrix} = \begin{bmatrix} 1 & T_s \\ 0 & a \end{bmatrix} \begin{bmatrix} z_s(k) \\ \tilde{i}_s(k) \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{v_{dc}}{2} b \end{bmatrix} u_s(k) + \begin{bmatrix} 0 \\ d_s(k) \end{bmatrix}, \tag{7.6}$$

Here, terms $d_s(k)$ (= $b \cdot e_s(k) - i_s^*(k+1) + a \cdot i_s^*(k)$) depend on the system input voltages and on the change in reference currents. These terms can be viewed as disturbances on the system.

Eq (7.6) will be used later for the design of the integral variable structure control.

7.1.3 Current control structure in stationary frame

Fig. 7.2 illustrates the structural diagram of the current loop of the PWM

rectifier system. As shown in Fig. 7.2, the amplitudes of the control signals u_α and u_β are limited to ±1 by a saturation unit. The control signals are then 'amplified' by the PWM rectifier to control the line current. The current controller unit could be the P + Resonant controller (P+RC), the integral variable structure controller (IVSC) or the ILC based hybrid current controller (Hybrid ILC).

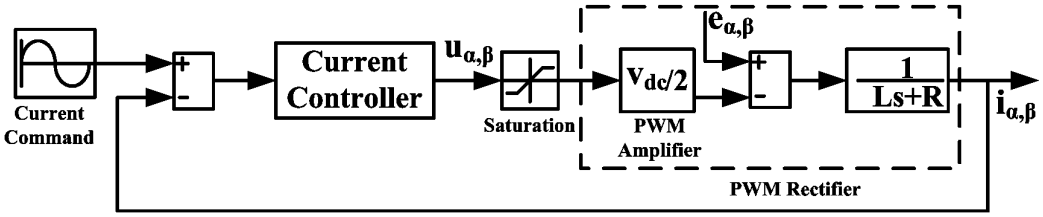


Fig. 7.2 Structure of the current loop of the PWM rectifier system

7.2 P + Resonant control (P+RC) current tracking scheme

In this section, the P + RC scheme will be introduced.

7.2.1 Introduction to P + Resonant controller [74, 75]

Proportional integral (PI) compensators are widely used in many *dc* regulation systems because of their ability to provide theoretically infinite gain at zero frequency. The PI controller has an *s*-plane transfer function of

$$H_{dc}(s) = K_p + \frac{K_I}{s}, \tag{7.7}$$

where K_p and K_I are the proportional gain and integral gain, respectively.

However, a simple PI controller suffers from steady-state error problem [74, 75] when tracking periodic *ac* signals. This is because the PI controller can not provide

infinite gain at the frequency of the *ac* signal. On the other hand, if a controller provides infinite gain at the tracking frequency of interest, say, f_o, then zero steady-state tracking error can be achieved for a signal with frequency of f_o. A P + Resonant controller is such a compensator which can provide infinite gain at the resonant frequency. The P + Resonant controller is derived based on *ac* regulator theory developed in carrier servo-control systems [74, 75]. The principle is to transform the desired *dc* compensation network into an equivalent *ac* compensation network, so that it has the same frequency response characteristic as the *dc* compensation network in the bandwidth of concern. The shifting of the frequency range of the PI controller by a frequency ω_o can be done by the following transformation [75].

$$H_{ac}(s) = H_{dc}(\frac{s^2 + \omega_o^2}{2s}) \tag{7.8}$$

The ideal P + Resonant controller is then obtained by substituting (7.8) into (7.7).

$$H_{ac}(s) = K_p + \frac{2K_I s}{s^2 + \omega_o^2} \tag{7.9}$$

Under ideal conditions, the controller will provide infinite gain at the resonant frequency.

7.2.2 Practical implementation

Practically, it is not possible to realize an ideal *dc* integrator in the case of a PI

controller due to the limited finite precision in digital systems and the finite amplifier gain in analog systems. A low-pass transfer function can be used to approximate a PI controller [74, 75].

$$H_{dc}(s) = K_p + \frac{K_I}{s + \omega_c} \tag{7.10}$$

Here ω_c is the lower breakpoint frequency of the *dc* transfer function.

Likewise, a practical P+Resonant controller will not realize the ideal resonant function indicated in (7.9). Substituting (7.8) into (7.10) [74, 75], we can obtain the transfer function of a practical P+Resonant compensator as

$$H_{ac}(s) = K_p + \frac{2K_I s}{s^2 + 2\omega_c s + \omega_o^2} \tag{7.11}$$

Essentially, the practical P+Resonant controller will incorporate a damped resonant function rather than an ideal resonant function.

Fig. 7. 3 shows the Bode plots of the loop transfer functions for a PWM rectifier system obtained a) with only a proportional controller, b) with an ideal P + Resonant regulator and c) lastly with a practical (damped) P + Resonant regulator. The plots show the effect of the resonant regulator on the frequency response of the loop transfer function and also the effect due to damping in the P+Resonant controller on the loop transfer function. It can be seen from Fig. 7.3 that the resonant regulator only contributes to the frequency response around the resonant frequency due to its narrow band frequency response. The proportional control determines the frequency

response at frequencies other than the resonant frequency. It can be seen from Fig. 7.3 that both the ideal and the practical resonant controller introduce a phase shift around the resonant frequency, which reduces the phase margin at the resonant frequency. However, the phase shift of the damped resonant controller has less effect on stability of the system than that of the ideal resonant controller.

Based on the above discussion, a simple design procedure for the P + Resonant controller can be implemented as follows. Firstly, the proportional gain is chosen such that the system remains stable and can provide a reasonable transient response. Thereafter, the resonant regulator is designed to minimize steady-state error.

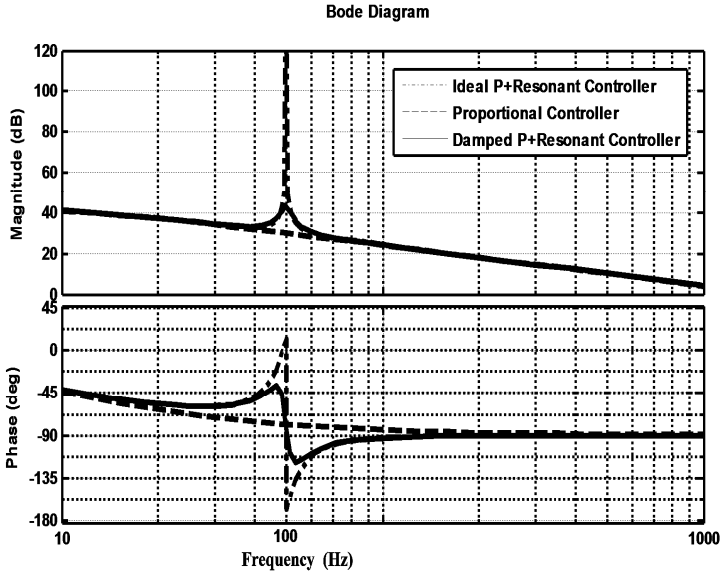


Fig. 7.3 Frequency responses of loop transfer function with only a proportional controller, with an ideal P + Resonant Controller and with a damped P + Resonant controller with a resonant gain K_i=15

Next the method for designing the resonant regulator will be investigated.

The gain at the resonant frequency ω_0 is given by

$$H_{ac}(j\omega_o) = \frac{j2K_I\omega_o}{-\omega_o^2 + j2\omega_c\omega_o + \omega_o^2} = \frac{K_I}{\omega_c} \tag{7.12}$$

With $K_I=1$ and ω_c varied from 0.1 to 10 and 100, the Bode plots of resonant control are given in Fig. 7.4. From (7.12), we conclude that varying ω_c results in the change of the value of the resonant peak. Thus, as illustrated in Fig. 7.4, very high gain can be obtained at the resonant frequency only with a very small value of ω_c. With such a small ω_c value, if the operating frequency has a slight shift from the designed resonant frequency, then a large attenuation of the amplitude of the frequency response will occur [74, 75]. The high gain benefit of the resonant regulator at the tracking frequency will no longer exist. Thus, the P + Resonant regulator can be sensitive to frequency variations, particularly with low damping ratios.

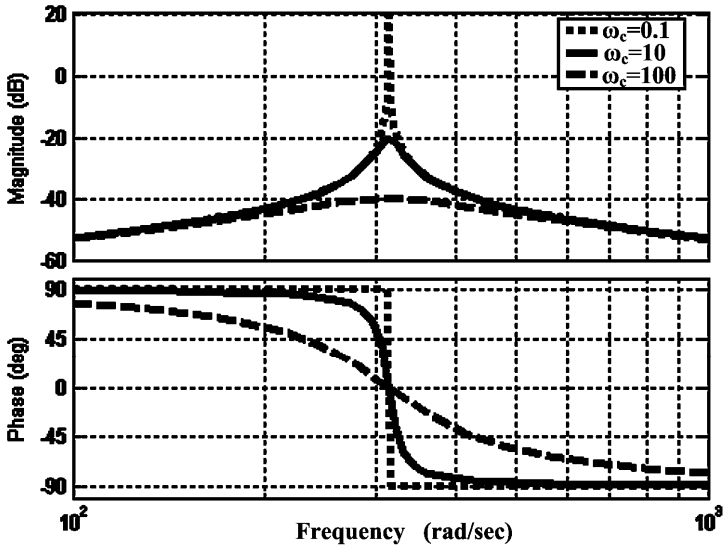


Fig. 7.4 Frequency response of the resonant term for variation in ω_c and $K_I=1$.

The sensitivity to frequency variation of the resonant regulator can be reduced

by increasing the gain of regulator K_I [74，75]. By doing this, the magnitude response of the regulator can be uniformly increased around resonant frequency while its shape will not be affected.

However, if the gain K_I of the regulator is made very large, then the gain cross-over frequency of the system will be significantly increased [96]. The upper value of the parameter K_i is thus limited by considerations of system stability. Thus, there is a trade-off between the phase margin achieved and the robustness to line frequency variations. Both Bode plots and root locus can be used to assess the stability of system using the P + resonant controller [96].

In summary, with a smaller value of ω_c, larger gain at the resonant frequency can be obtained with a given value of K_I. A larger value of K_I, within stability limit, can enhance the robustness of P + Resonant controller to frequency variations.

7.3 Integral variable structure control (IVSC) current tracking scheme

Variable structure control has been widely used in control applications, since it can provide high robustness in the face of system uncertainties and disturbance. The concept of the variable structure control is to formulate a variable structure control law such that the system state is forced to certain pre-defined surface, called sliding surface, and it is forced to stay there by appropriate switching of the control structure [76~83]. However, for a first order system, variable structure control will result in steady-state error in the sliding mode dynamics [95]. On the other hand, integral

variable structure control is a variable structure control with integral augmented switching surface [79]. Integral augmentation is introduced to alleviate steady state error in the quasi-sliding mode.

7.3.1 Controller design

Normally, the design procedure of variable structure control includes selecting sliding surface, verifying sliding mode existence and stability analysis. With a reaching law approach [76], a reaching law is specified such that the existence and stability of IVSC are satisfied.

- ***Choice of switching surface***

The **P-I** type switching surface is selected as:

$$\sigma_s(k) = \tilde{i}_s(k) + \lambda z_s(k) \quad s = \alpha, \beta \tag{7.13}$$

where $\sigma_s(k)$ is the switching surface and λ is the integral gain.

- ***Reaching law***

A convenient reaching law for a discrete system is specified as [77]:

$$\sigma_s(k+1) - \sigma_s(k) = -qT_s\sigma_s(k) - \varepsilon T_s \operatorname{sgn}(\sigma_s(k))$$

$$\varepsilon > 0, q > 0, 1 - qT_s > 0, s = \alpha, \beta \tag{7.14}$$

where $\operatorname{sgn}(\sigma_s(k)) = \begin{cases} 1 & if \quad \sigma > 0 \\ -1 & if \quad \sigma < 0 \end{cases}$

- ***Stability and existence of sliding mode***

The existence and stability of the IVSC can be guaranteed if

$$\left[\sigma_s(k+1)-\sigma_s(k)\right]\sigma_s(k)<0 \tag{7.15}$$

With (7.14), this condition can be satisfied easily as follows.

$$\left[\sigma_s(k+1)-\sigma_s(k)\right]\sigma_s(k)=-qT\sigma_s^2(k)-\varepsilon T\sigma_s(k)\,\mathrm{sgn}(\sigma_s(k))<0 \tag{7.16}$$

- ***Control law***

Substituting (7.6) and (7.13) into (7.14), the control law is obtained as:

$$u_s(k)=\left[(\lambda T-1+a)\tilde{i}_s(k)+d_s(k)+qT\sigma_s(k)+\varepsilon T\,\mathrm{sgn}(\sigma_s(k)/\Phi)\right]\Big/\, b\cdot\frac{v_{dc}}{2}\quad s=\alpha,\beta \tag{7.17}$$

with $d_{\alpha,\beta}(k)=b\cdot e_{\alpha,\beta}(k)-i^*_{\alpha,\beta}(k+1)+a\cdot i^*_{\alpha,\beta}(k)$.

7.3.2 The quasi-sliding mode

The ideal quasi-sliding mode satisfies:

$$\sigma_s(k+1)=\sigma_s(k)=0\quad s=\alpha,\beta\quad k=0,1,2,\cdots \tag{7.18}$$

While on the quasi-sliding surface, the dynamics of the system is reduced to

$$\tilde{i}_s(k+1)=(1-\lambda T)\cdot\tilde{i}_s(k)\quad s=\alpha,\beta \tag{7.19}$$

Speed of error convergence is determined by λ. With $0<\lambda T<1$, the quasi-sliding mode is stable and the error will converge to zero in finite time.

7.3.3 The quasi-sliding mode band

With the above design, a desired state trajectory of a discrete variable structure system should have the following attributes [76]:

1. Starting from any initial state, the trajectory will move monotonically toward the switching plane and cross it in finite time.

2. Once the trajectory has crossed the switching plane the first time, it will cross the plane again in every successive sampling period, resulting in a zigzag motion about the switching plane.

3. The size of each successive zigzagging step is non-increasing and trajectory stays within a specified band.

The first attribute forms the discrete-time reaching condition and the last two attributes form the basis in defining the quasi sliding mode for discrete variable structure control system. With a reaching law approach [76], the above attributes are always satisfied.

Based on the second attribute, the signs of $\sigma_s(k+1)$ and $\sigma_s(k)$ must be opposite to each other. Eq. (7.14) can be written as given below.

$$\sigma_s(k+1) = (1-qT)\sigma_s(k) - \varepsilon T \operatorname{sgn}(\sigma_s(k)) \qquad 1-qT > 0 \tag{7.20}$$

The sign of the first right-hand term is the same as the sign of $\sigma_s(k)$. In addition, the sign of sgn ($\sigma_s(k)$) is the same as that of $\sigma_s(k)$. Thus, as the signs of $\sigma_s(k+1)$ is opposite to that of $\sigma_s(k)$, the following condition is satisfied.

$$\left|(1-qT)\sigma_s(k)\right| < \left|\varepsilon T \operatorname{sgn}(\sigma_s(k))\right| \tag{7.21}$$

That is

$$\left|\sigma_s(k)\right| < \frac{\varepsilon T}{1-qT} \tag{7.22}$$

The width of the quasi-sliding mode band can be conveniently calculated based on (7.22). It is clear that the width of the sliding mode band decreases with increasing sampling frequency.

7.3.4 Chattering reduction

However, as the discontinuity in the control (7.17) gives rise to chatter in the system, the switching function should be replaced by a continuous approximation using a boundary layer technique [81]. A narrow boundary layer is introduced near the sliding surface so as to smoothen out the control behavior. In this way, the signum function is replaced by saturation function.

$$sat(\sigma_s/\Phi) = \begin{cases} \sigma_s/\Phi & \left|\sigma_s/\Phi\right| < 1 \\ \mathrm{sgn}(\sigma_s/\Phi) & \left|\sigma_s/\Phi\right| \geq 1 \end{cases} s = \alpha, \beta \tag{7.23}$$

Here Φ is the thickness of the boundary layer.

It is clear that outside the boundary layer, the saturation function and the signum function provide equivalent control efforts, while within the boundary layer the control law given by (7.17) becomes a smoothly varying function; the feedback action provided by the discontinuous control is reduced which degrades control precision. Thus there is a trade-off between control precision and reduction of chattering.

7.3.5 Choice of parameters

In conclusion, the control law given in (7.17) can be written in the following form.

$$u_s(k) = u_{eq}(k) + k_1\sigma(k) + k_2 sat(\frac{\sigma(k)}{\Phi}) \tag{7.24}$$

with $u_{eq}(k) = \frac{2\left[(\lambda T - 1 + a)\tilde{i}_s(k) + d_s(k)\right]}{b \cdot v_{dc}}$, $k_1 = \frac{2qT}{b \cdot v_{dc}}$ and $k_2 = \frac{2\varepsilon T}{b \cdot v_{dc}}$. Here v_{dc} is treated as constant.

The first term on the right hand side of (7.24) is used to cancel the known dynamics and keep the trajectory on the quasi sliding mode. As can be seen from (7.19), the choice of parameter λ will determine sliding mode stability and the speed of error convergence.

The second term on the right hand side of (7.24) forces the trajectory to approach the sliding mode surface. Once trajectory is on the sliding mode surface, the effect of the second term is attenuated as the value of $\sigma(k)$ becomes quite small. Therefore, a large value of k_1 (q) will accelerate the process of approaching the sliding mode surface.

The third term on the right hand of (7.24) will cancel out any unknown dynamics and disturbances. As seen from (7.22), a small value of k_2 (ε) will result in a narrow quasi-sliding mode band. However, the value of k_2 (ε) should be large enough to overcome unknown dynamics and disturbances. Thus, a suitable value for k_2 (ε) and a small boundary layer Φ are desired to facilitate global attractiveness of

the sliding surface and result in small steady state error.

In summary, the choice of parameter λ will determine sliding mode stability and the speed of error convergence. The choice of parameter q will determine the process of approaching the sliding mode surface. The choice of parameter ε and boundary layer Φ will determine steady state error. The parameters λ, q, ε and Φ are chosen based on guideline given here and further refined during experiments to obtain optimal performance.

7.4 Hybrid Iterative learning controller (Hybrid ILC) current tracking scheme

7.4.1 Iterative learning control – an introduction

The idea of iterative learning control (ILC) [84] is to use the information of the preceding cycle to improve the control performance of the present cycle. ILC differs from most of the existing control methods in the sense that it computes/ generates the present cycle control effort based on the error and control input signals of the preceding cycle directly.

We consider a simple P- type learning update rule

$$u_{i+1}(k) = u_i(k) + k_{ILC} \times e_i(k), \tag{7.25}$$

where $u_{i+1}(k)$ and $u_i(k)$ are the control efforts given to the system at the (i+1) th and i th iteration cycle respectively and $e_i(k)$ is the tracking error at the i th iteration

cycle. Here, parameter k_{ILC} is the learning gain, subscript i denotes i th repetition and letter k denotes the k th sampling action.

According to (7.25), ILC computes the present cycle control effort by utilizing the experience gained from repeated executions of the same operation [86]. The above ILC update law can be illustrated by taking its z-transform in the repetition domain as follows.

$$u_i(z) = \frac{k_{ILC}}{z-1} \times e_i(z) \tag{7.26}$$

Eq. (7.26) shows that the control effort at the ith iteration simply becomes the learning gain times the sum over all previous repetitions of the errors observed at the time kth interval which corresponds to applying integral control concepts in the repetition domain. Thus, one can refer to this learning law as integral based ILC [86]. This highlights the underlying philosophy of ILC.

To discover the learning process in the frequency domain, let us take the z-transform of (7.25) in the sampling sequence domain which produces

$$u_{i+1}(z) = u_i(z) + k_{ILC} \times e_i(z). \tag{7.27}$$

Supposing $G(z)$ is the plant transfer function and $r(z)$ is the reference which is the same for each repetition, then the output $y(z)$ is given by

$$y_i(z) = G(z) \times u_i(z) \tag{7.28}$$

Combining these equations, it can be shown that the error propagation equation is

$$e_{i+1}(z) = [1 - k_{ILC} \times G(z)] \times e_i(z). \tag{7.29}$$

Here, *e(z)* is error between reference and output.

By setting $z = e^{j\omega T_s}$, where T_s is the sampling interval, the steady-state frequency response can be obtained. Thus, the amplitude of the steady-state frequency component of the error $\left|e_i(e^{j\omega T_s})\right|$ at frequency ω satisfies

$$\left|e_{i+1}(e^{j\omega T_s})\right| = \left|1 - k_{ILC} \times G(e^{j\omega T_s})\right| \times \left|e_i(e^{j\omega T_s})\right| \tag{7.30}$$

The error will decay cycle by cycle if

$$\left|1 - k_{ILC} \times G(e^{j\omega T_s})\right| < 1 \tag{7.31}$$

If this inequality (7.31) is satisfied for all ω then monotonic decay of the tracking error to zero can be achieved. The absolute value term on the left hand side of (7.31) is the 'error decay factor'. The amplitude of the error component at any frequency ω is multiplied by this factor in each repetition; thus, this factor determines the convergence speed of the tracking error.

Thus, by choosing the learning gain k_{ILC} in (7.31) in such a way that the locus of vector $k_{ILC} \times G(e^{j\omega Ts})$ does not exceed the unit circle centered at 1 as ω is increased from 0 to Nyquist frequency (equal to half of sampling frequency), monotonic convergence of error will be guaranteed.

7.4.2 Hybrid ILC current control scheme

It should be noted that the ILC forms its control effort by learning from the experience of the preceding cycle. As the present activities of a PWM rectifier are

not monitored, a fast transient response to a sudden change can not be expected. Hence, to obtain a reasonable dynamic response, a feedback controller is also required. A hybrid current control scheme which consists of a feedback controller together with a plug-in type iterative learning controller for a PWM rectifier is shown in Fig. 7.5. Here, *r(k)* is the current command and $e_{i+1}(k)$ is the tracking error during the (*i+1*)th repetition cycle. The periodic disturbances, caused by the *ac* sinusoidal supply voltage and by the *ac* load current are denoted by *d(k)*. The linear feedback controller provides the major part of the control effort during any transient operation, such as under load change or supply voltage change. As the system enters steady-state, the ILC takes over the control effort and tries to reduce the steady-state tracking error from cycle to cycle.

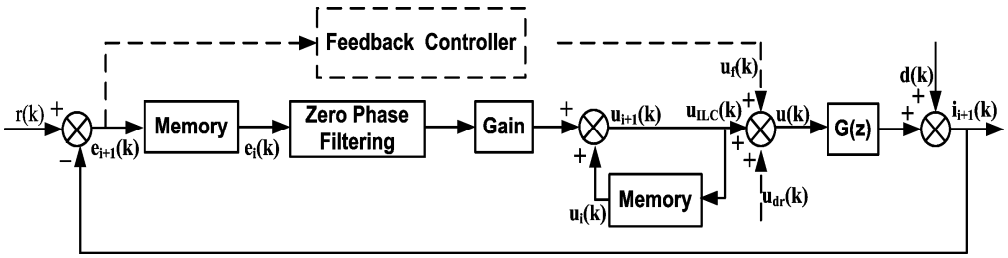


Fig. 7.5 Block diagram of the Hybrid ILC controller for a PWM rectifier system

The overall control law is given by

$$u(z) = u_{ILC}(z) + u_f(z) + u_{dr}(z), \tag{7.32}$$

where the control effort $u_{ILC}(z)$ denotes the feed forward control effort provided by ILC, the control effort $u_f(z)$ denotes the feedback control effort and the control effort $u_{dr}(z)$ denotes the feed forward control effort which is used to reject the disturbance caused by *d (z)*.

The relationship between the present cycle error and the preceding cycle error can be obtained as given below.

$$e_{i+1}(z) = [1 - \frac{k_{ILC} \times G(z)}{1 + G_c(z) \times G(z)}] \times e_i(z) \tag{7.33}$$

Here, $G_c(z)$ is the transfer function of the feedback controller, variable $e_{i+1}(z)$ is the present cycle error and variable $e_i(z)$ is the previous cycle error. In Fig. 7.5, variable $u_{dr}(z)$ is the feed forward controller used to reject the disturbance $d(z)$.

By setting $z = e^{j\omega T_s}$, the error convergence equation can be written as:

$$e_{i+1}(e^{j\omega T_s}) = [1 - \frac{k_{ILC} G(e^{j\omega T_s})}{1 + G_c(e^{j\omega T_s}) G(e^{j\omega T_s})}] e_i(e^{j\omega T_s}) \tag{7.34}$$

The speed of error decay is determined by the error decay factor $\left|1 - \frac{k_{ILC} G(e^{j\omega T_s})}{1 + G_c(e^{j\omega T_s}) G(e^{j\omega T_s})}\right|$. If parameter k_{ILC} is selected such that the gain of $\frac{k_{ILC} G(e^{j\omega T_s})}{1 + G_c(e^{j\omega T_s}) G(e^{j\omega T_s})}$ is much close to unity, very fast error decay can be expected. The term $\frac{k_{ILC} G(e^{j\omega T_s})}{1 + G_c(e^{j\omega T_s}) G(e^{j\omega T_s})}$ can be divided into two parts as follows:

$$\frac{k_{ILC} G(e^{j\omega T_s})}{1 + G_c(e^{j\omega T_s}) G(e^{j\omega T_s})} = T(e^{j\omega T_s}) \times \frac{k_{ILC}}{G_c(e^{j\omega T_s})} \tag{7.35}$$

with $T(e^{j\omega T_s}) = \frac{G_c(e^{j\omega T_s}) G(e^{j\omega T_s})}{1 + G_c(e^{j\omega T_s}) G(e^{j\omega T_s})}$.

Here, the first part $T(e^{j\omega Ts})$ is the system closed loop transfer function when using feedback controller only. Normally, it is designed to have unity gain at low

frequency. Thus, if the second part $\frac{k_{ILC}}{G_c(e^{j\omega T_s})}$ also has unity gain, then fast error decay can be obtained. In the present work, the feedback control is chosen as a simple proportional controller. Therefore, if the gain of k_{ILC} is made equal to the proportional gain, P, then the error decay factor will approach unity at low frequency.

7.4.3 Practical implementation issues

As mentioned earlier, the learning control law in (7.25) can be viewed as an integral control applied in the repetition domain. As anti-windup integration action is required in the integral control, some measures should also be taken to ensure long term stability and monotonic decrease of the tracking error.

As discussed in Sections 7.4.1 and 7.4.3, the error convergence condition can be easily satisfied by choosing a proper learning gain k_{ILC}. However, in practice, it is unlikely that there is any one learning gain that would satisfy the convergence condition for each frequency. This is because in a practical system there will always exist parasitic poles which will force the trajectory outside the unit circle at higher frequencies. Due to the uncertainties in the modeling of the PWM rectifier, a simple ILC would unavoidably result in an unstable system. A phenomenon that was commonly observed in our experimental set-up is that the error would appear to converge to zero very nicely at the beginning of the operation, but later the error would start to grow and the system would become unstable.

There are several ways to cope with this problem. A great deal of effort has been devoted by other researchers to the practical implementation issues in an ILC system [85-91]. A recent successful application of ILC and Hybrid ILC for inverter voltage control has been presented in [91]. The approach followed in the present work and presented below is largely based on [91].

- ***Zero phase filtering***

As the learning process is unforgiving, the ILC will keep working on any small error even if the error is small enough to be neglected from an engineering point of view [86]. If the error occurs at frequencies without extra phase margin, divergence of error will eventually happen. It would be advisable if the learning process is cut off for frequencies outside of the unit circle. One way to achieve this is to make use of zero phase low pass filtering to filter the high frequency components.

There are several ways to design such a zero-phase low pass filtering [90] and [91]. The design procedure provided in [91] is applicable to the present system also.

According to [91], to construct the zero phase filter, a zero-phase non-causal filter $F_1(z)$ and a high-frequency attenuation filter $F_2(z)$ are required. Therefore, the complete filter Φ (z) is

$$\Phi(z) = F_1(z)F_2(z) \tag{7.36}$$

In the design of ZPF, choosing a suitable cutoff frequency is vital. A simple method to determine this value is to use an experimental approach. One can begin with a high cutoff frequency, and if the error does not converge, then the cutoff

frequency is slightly reduced until error converges.

- ***Forgetting factor***

In a practical implementation, the forgetting factor α is selected as a small positive constant to enhance the robustness of the ILC against noise, initialization error and variations in system dynamics. Reference [80] gives the requirement of α according to measurement noise level. It is shown that the presence of measurement noise can render the system unstable with too small a value of α. On the other hand, a large value of α will cause high steady-state tracking error. Therefore, a compromise is needed between robustness and tracking performance of the ILC in choosing α.

- ***Linear phase lead compensation***

A time advance unit advances control effort by m sampling intervals in next iterative period, to compensate for the phase lag of the PWM rectifier. Due to the time-delay of a fundamental cycle introduced before starting the tracking, it is possible to use a non-causal filter and the time advance unit [83].

- ***Practical learning law***

The resultant learning law of the ILC is given by

$$u_{i+1}(z) = (1-\alpha)u_i(z) + k_{ILC}z^{-m}\Phi(z)e_i(z), \tag{7.37}$$

where $\Phi(z)$ is the zero phase low pass filter to be designed, α is the forgetting factor and z^{-m} is the linear phase lead compensation (time advance) unit.

7.5 The design of current controllers

In this section, the three current tracking schemes for the PWM rectifier system are designed in the SF based on the methods discussed in earlier sections. In order to perform a fair comparison, the control parameters of the three controllers are further adjusted experimentally to obtain optimal experimental performance.

7.5.1 Design of P + Resonant controller

As mentioned earlier, the resonant regulator only contributes to the frequency response around the resonant frequency. Therefore, the current controller with proportional control only is first designed to achieve reasonable transient response. Thus, the resonant controller is used as a plug in type controller to eliminate steady-state tracking error.

It can be seen from the model given in (7.1) that the supply voltages are the major disturbances to the system. To reject the disturbance, these measured voltages transformed into SF will be used as a feedforward disturbance rejection control u_{dr}.

$$u_{dr} = \frac{2e_s}{v_{dc}} \quad s = \alpha, \beta \tag{7.38}$$

Eq. (7.2) gives transfer function of current loop. Based on the system parameters given in Table I, the transfer function *G(s)* in (7.2) can be discretized as follows.

$$G(z) = \frac{2.402}{z - 0.9935} \tag{7.39}$$

With feedback controller u_f and disturbance rejection term u_{dr} employed, the resulting closed loop transfer function is

$$T(z) = \frac{PG(z)}{1+PG(z)} = \frac{2.402P}{z-0.9935+2.402P}, \tag{7.40}$$

where P is the proportion gain.

In principle, it should be easy to design the proportional gain for the first order system given in (7.40). One way is to choose the P value to be equal to 0.414, so as to place the pole of $T(z)$ at the origin to achieve deadbeat control. However, it was found during experimental work that the theoretically designed proportional gain could not maintain stable operation. This may be attributed to parameter variations in the resistance and inductance values and to a time delay of 1.5 T_s that was found to be inherent in the dSpace experimental system, which is discussed further in Appendix F. Experimentally, a proportional gain of 0.21 was found to result in a stable system and also give a good transient response.

Following this, the resonant component of the controller was designed to provide sufficiently large loop gain amplification at the line frequency. To ensure long term stability, an anti-windup action was introduced to reset the resonant control when it is saturated as suggested in [74]. The control parameters (see (7.11)) used in the experiment were $k_p = P = 0.21$, $k_i = 150$, $\omega_c = 0.1$ and $\omega_o = 100\pi$.

With this design, the bandwidth of current loop was around 800 Hz. It must be noted that this bandwidth is twice that obtained in the case of dual current controller in Chapter 4. The reason for this higher bandwidth can be attributed to the avoiding

of sequence separation and sequence component extracting filters in the current feedback path due to the control being carried out the α-β stationary frame.

7.5.2 Design of integral variable structure control

The control parameters λ, q, ε, T and Φ in the control law (7.24) have to be determined. As both the sampling frequency and the switching frequency are 10 *kHz*, the value of control parameter T was set to 1e-4s. As mentioned in Section 7.3.5, the choice of parameter λ will determine the sliding mode stability and the speed of error convergence. The value of parameter λ should be within a range of [0 10000] as indicated in (7.19). A larger value of parameter λ will result in a faster error reduction. However, as there is a time delay of 1.5 T_s that was found to be inherent in the dSpace experimental system as discussed in the Appendix F, the value of parameter λ can not be chosen too large. Otherwise, the sliding mode stability is deteriorated. In the experimental work, the value of parameter λ was chosen as 2000 using a trial and error approach.

As mentioned in Section 7.3.5, the choice of parameter q will determine the speed with which the trajectory approaches the sliding mode surface. The value of parameter q should be within a range of [0 10000] as indicated in (7.20). However, it was found in our experiment that with increasing q, the steady-state error also increases. In the experiment, the value of parameter q was chosen as 2000 using again a trial and error approach.

The choice of parameters ε and Φ will determine the amplitude of the steady

state error as discussed in Section 7.3.5. A value of 500 and a value of 0.5 were experimentally chosen for parameter ε and parameter Φ, respectively, to achieve a narrow quasi-sliding mode band and at the same time to overcome unknown disturbance and reduce chattering.

In summary, the control parameters used in the experimental work were as follows:

λ=2000, q=2000, ε=500, T=1e-4 and Φ=0.5.

7.5.3 Design of the Hybrid ILC current controller

As shown in Fig. 7.5, the overall controller includes three parts: the feedback controller u_f, the iterative learning controller u_{ILC} and the feed-forward controller u_{dr} for disturbance rejection purposes. All these controllers were implemented in the stationary frame.

Here, the disturbance rejection controller u_{dr} with $u_{dr} = 2e_{\alpha,\beta}/ v_{dc}$ is used to cancel out disturbance $d(s)$ shown in (7.2). The proportional control is used as the feedback controller. The design procedure adopted for this feedback controller was the same as that of the proportional controller in the P + Resonant controller. The proportional gain was once again chosen based on experimental approach to be 0.21. With such a proportional gain, the bandwidth of the system with proportional controller together with the disturbance rejection controller is close to 800 Hz.

Next the ILC controller was designed. Based on the ILC control law given in

(7.37), four design steps are involved, names, the determination of learning gain, zero phase filter, forgetting factor and the time advance unit.

As shown in (7.35), the error convergence speed is determined by two terms. The first term *T(z)* is the closed loop transfer function given in (7.40) designed to have unity gain at low frequency. Therefore, the gain of second part $\frac{k_{ILC}}{P}$ will determine the speed of the error convergence. In our experiment, the learning gain is chosen as 0.105 such that error converges at a rate of $(0.5)^{n}$.

In the design of the zero phase filter, the determination of the cutoff frequency of the filter is vital to the success of the design. Here, the cutoff frequency was obtained by using a trial and error approach. As the *ac* current to be controlled has a fundamental frequency of 50 Hz. A zero phase filter with a cutoff frequency of 500 Hz was chosen as below.

$$F(z) = \frac{z^7 + 8z^6 + 28z^5 + 56z^4 + 86z^3 + 112z^2 + 141z + 156}{1024} + \frac{141z^{-1} + 112z^{-2} + 86z^{-3} + 56z^{-4} + 28z^{-5} + 8z^{-6} + z^{-7}}{1024} \tag{7.41}$$

However, it was found experimentally that the error could not converge. A zero phase filter with a slightly reduced cutoff frequency was then chosen and tried out. This process was repeated until the error converged. Eventually, the following zero phase filter was designed to cut off the learning of the ILC at about 391 Hz such that a stable system is obtained.

$$F(z)=\frac{z^8+4z^7+8z^6+12z^5+16z^4+20z^3+24z^2+28z+30}{1024}+\frac{28z^{-1}+24z^{-2}+20z^{-3}+16z^{-4}+12z^{-5}+8z^{-6}+4z^{-7}+z^{-8}}{1024} \tag{7.42}$$

with $F_1(z)=\dfrac{z^4+2+z^{-4}}{4}$ and

$$F_2(z)=\frac{z^4+4z^3+8z^2+12z+14+12z^{-1}+8z^{-2}+4z^{-3}+z^{-4}}{64}$$

As the proposed method is implemented in a dSPACE DSP system (DS1104) using PWM technique, a time delay of 1.5 times the sampling period time was found to be introduced during experiments (see Appendix F). Therefore, to compensate for ths time delay, the time advance unit was set to 2. In addition, a forgetting factor of 0.01 was chosen to enhance the robustness of ILC controller.

The resultant learning law of the ILC used in the experimental work is given by

$$u_{i+1}(z)=0.99u_i(z)+0.105z^{-2}F_1(z)F_2(z)e_i(z) \tag{7.43}$$

7.6 Experimental comparison of current controllers

In this section, the experimental results with the three tracking current controllers and the dual current controller are presented and their performances are compared.

7.6.1 Current control with voltage loop open

As the purpose here was to evaluate the effectiveness of the current controllers, the voltage regulation loop was kept open for each of the four current control schemes. Tests were carried out under both balanced and unbalanced supply

conditions. The structure of the current control loop is illustrated as Fig. 7.2. The output power control method detailed in Chapter 4 with a given power reference has been employed as the current generation law for both balanced and unbalanced operating conditions. The power reference was set around 900 W. This resulted in a set of current commands such that the *dc* output voltage was around 200 V. The specifications of the experimental set-up are given in Table I. The same 1 kW prototype experimental system that was used in other experimental work was used here.

TABLE 7.1 EXPERIMENTAL SYSTEM PARAMETERS

Inductance	4.15 mH
Line resistor	0.27 Ω
dc output voltage	200 V
dc output capacitor	136 μF
Load	90 Ω
Switching Frequency	10 k*Hz*

The three-phase input supply voltage was kept at 60V (RMS) for the balanced operating condition. The supply voltages for the experiments under unbalanced conditions were set at $42\sqrt{2}\sin(\omega t + 355^\circ)$, $75\sqrt{2}\sin(\omega t + 236^\circ)$ and $66\sqrt{2}\sin(\omega t + 90^\circ)$. These values correspond to a positive sequence voltage of around 60 V (RMS) at a phase of -13^o and a negative sequence voltage of around 20 V (RMS) at a phase of 148^o. The THDs of the three-phase currents obtained with the four current controllers have been tabulated in Table II. It may be noted that the lowest THD values can be achieved under both balanced and unbalanced conditions with the Hybrid ILC scheme.

TABLE 7.2 EXPERIMENTAL TOTAL HARMONIC DISTORTION RESULTS – WITH ONLY CURRENT CONTROLLER

	Balanced Condition				Unbalanced Condition			
	DPIC	P+RC	IVSC	Hybrid ILC	DPIC	P+RC	IVSC	Hybrid ILC
i_a (THD %)	3.75	3.84	4.81	0.9	2.76	2.49	2.94	1.38
i_b(THD %)	3.79	3.74	4.49	0.86	7.43	5.56	5.82	1.45
i_c(THD %)	3.77	3.82	4.77	1.01	7.19	5.17	5.78	1.94

On the other hand, both the P + Resonant controller and the dual current controller provide similar steady-state performances especially under balanced operating conditions. This phenomenon may be explained as follows.

The working principle of both the dual current controller and the P + Resonant current controller is to provide relatively high gain at the frequency of interest. For the dual current controller, the frequency of interest (in the SRF) is *dc* (zero frequency). Therefore, the PI controller can provide a relatively high gain at that frequency. For the P + resonant current controller, the frequency of interest is 50 Hz and the resonant regulator will provide high amplification at that frequency. The ideal P + Resonant current controller has been obtained by shifting s to the frequency ω_o with the following transformation.

$$H_{ac}(s) = H_{dc}(\frac{s^2 + \omega_o^2}{2s}) \tag{7.44}$$

Here, $H_{dc}(\,)$ is transfer function of PI controller.

Therefore, the P+Resonant current controller is an extension to the stationary frame of the PI current controller used in the synchronous rotating frame to the stationary frame. This may be the reason why both controllers provide similar

steady-state performances.

However, it may be also noted that the IVSC has the largest THD values for the input currents under balanced conditions among the four current controllers. This could be attributed to the sensitivity of the integral variable structure control to the inherent time delay of 1.5 T_s in the dSpace experimental system used. This time delay can be addressed [97, 98] to enhance performance of IVSC. Compared to the IVSC current controller, the Hybrid ILC and P+RC controllers appear to be more robust to the existence of time delay in the experimental set-up.

It is worth noting that the current controllers (P+RC, IVSC and Hybrid ILC) implemented in the stationary frame are superior to the dual PI current controller implemented in the synchronously rotating frame in many aspects. First of all, only two current controllers are required when the current controllers are implemented in the stationary frame. Secondly, sequence separation and sequence component extracting filters in the current feedback path are avoided. The sequence component extracting filters are sensitive to noise disturbances particularly when the amplitude of the current is small. Very likely, this is the reason for the high THDs of the *b*-phase and *c*-phase currents obtained with dual current control scheme under unbalanced operating conditions. Lastly, as indicated in Sec. 7.5.1, the bandwidths of both the P + Resonant and the Hybrid ILC controllers can be made much higher (in this case double) than that of the dual current controller due to the absence of the sequence separation and sequence component extracting filters in the current

feedback path. A faster current loop makes it possible to have a faster voltage loop controller, in turn.

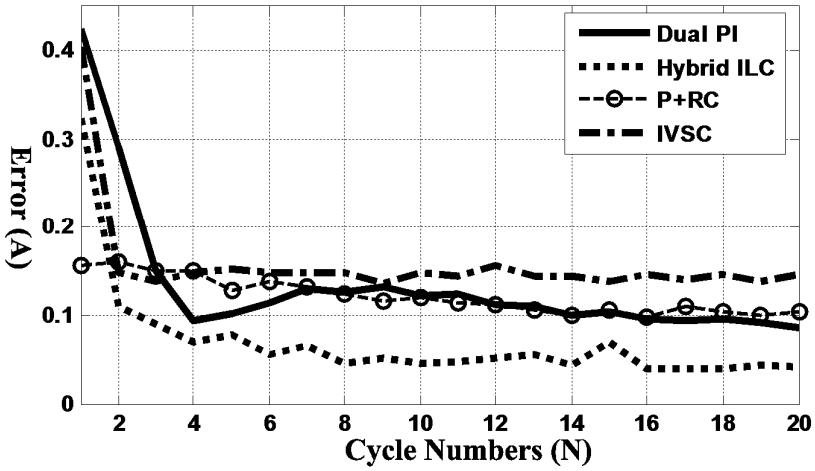


Fig. 7.6 Tracking error in a-phase RMS current with different current controllers for a step change in current commands from 4.2 A to 2.4 A

Next, the transient responses with the three tracking current controllers were experimentally compared. Fig. 7.6 shows the tracking error of the *a*-phase RMS current for a step change in current commands from 4.2 A to 2.4 A when connected to a 90 Ω *dc* load with the different current controllers. As shown in Fig. 7.6, the Hybrid ILC current controller has the smallest error among the three current controllers.

The steady-state performances of the different control methods can also be judged from Fig. 7.6. When the system enters steady-state operation, (after about 6 fundamental cycles in Fig. 7.6), it can be noted that the Hybrid ILC current controller has the smallest error steady-state error whereas ILVC current controller has the highest error steady-state error. The current error with the proposed Hybrid ILC controller settles down to a low value after 2 fundamental cycles. The P + Resonant

current controller has the fastest dynamic response for the current tracking among these current controllers. The error is very close to the final value in the first cycle itself.

While the Hybrid ILC controller does not match the dynamic performance of the P+RC current controller, it still has a satisfactory performance during transient conditions. As mentioned earlier, in the first fundamental cycle after a sudden change in the current command, only the proportional feedback controller reacts to the change. The ILC controller begins to react after one fundamental cycle. This accounts for the slower transient response with the proposed hybrid ILC controller compared to the P + Resonant controller.

7.6.2 With both current and voltage loops closed

- ***Voltage loop controller***

Operating a PWM rectifier with current mode control simplifies the dynamics of the *dc* output voltage to that of a current-fed resistor-capacitor load. The voltage loop controller used in the 'current mode control' scheme in Chapter 3 was adopted here. The current to output voltage transfer function is $F_{vi}(s)$ given in Table 3.4 of Chapter 3. A three-pole one-zero compensator was used here. The poles of the compensator were located at 0 rad/s for tight *dc* regulation, 2928 rad/s to compensate the effect of the RHP zero and 12900 rad/s to cancel out the effect of ESR, respectively, and the zero was placed at 327 rad/s to compensate for the pole due to the output filter circuit in the transfer function $F_{vi}(s)$ given in Table 3.4 of Chapter 3.

The *dc* gain of the controller was set at 35.1. The cross-over frequency is 80Hz and the phase margin achieved is 70.5^{o} as mentioned in Chapter 3.

As the overall bandwidth of the voltage loop is 80 Hz, the voltage controller is not suitable for the system with dual current controller wherein the overall bandwidth of current loop is only 400 Hz (see Section 4.3). Therefore, for comparison of the closed loop operation, only the three current tracking schemes are utilized.

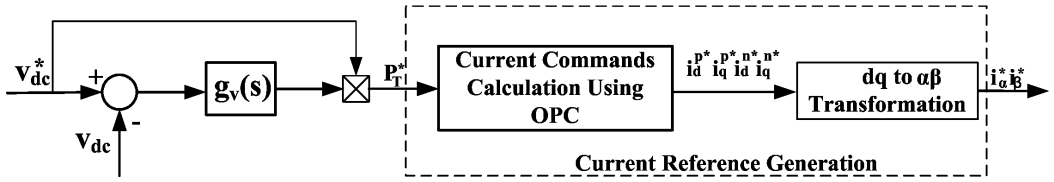


Fig. 7.7 Schematic diagram for current reference generation with both voltage and current control loops closed.

- ***Current reference generation***

It may be noted that the voltage loop controller designed in Chapter 3 can not be directly used to control the PWM rectifier with unbalanced supply. A current reference generation unit should be inserted between the voltage controller presented in Fig. 3.13 of Chapter 3 and the current controller given in Fig. 7.2 as illustrated in Fig. 7.7.

The power reference was generated by multiplying the output of voltage controller with *dc* output voltage reference. Then the output power control method presented in Chapter 4 was employed to generate the current commands in the *d-q* SRF frame. The generated current commands were then transformed into *α-β* stationary frame as shown in Fig. 7.7 and used as current commands inputs shown in

Fig. 7.2.

- ***Current loop controller***

The structural diagram of the current loop of the PWM rectifier system is given in Fig. 7.2. The current controller unit could be the P+Resonant controller, the integral variable structure control or the ILC based hybrid current controller as mentioned in Section 7.1.3.

TABLE 7.3 EXPERIMENTAL TOTAL HARMONIC DISTORTION RESULTS – CLOSED LOOP VOLTAGE CONTROL OPERATION

	Balanced Condition			Unbalanced Condition		
	P+RC	IVSC	Hybrid ILC	P+RC	IVSC	Hybrid ILC
i_a (THD %)	4.07	5.35	1.43	3.37	3.05	1.91
i_b(THD %)	4.35	5.14	0.75	6.05	6.08	1.32
i_c(THD %)	4.03	4.94	1.28	6.35	6.5	2.13

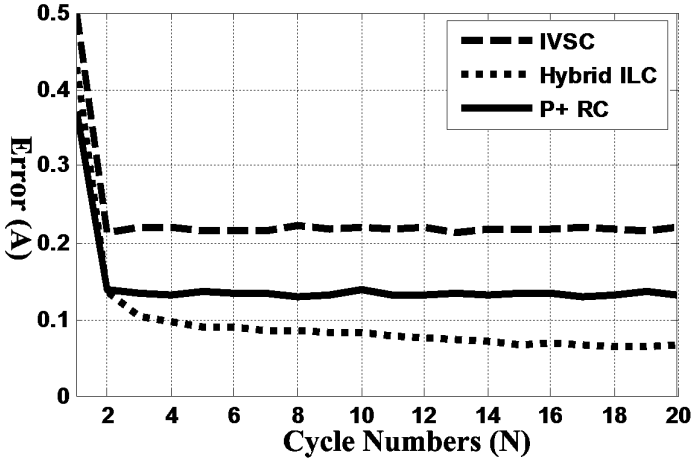


Fig. 7.8 Tracking errors in a-phase current (RMS value) with the three current controllers for a step change in *dc* output voltage reference from 175 V to 225 V

The supply voltages used for both balanced and unbalanced operations are the same as the ones used before in Sec. 7.6.1. The experimental THDs are summarized in Table III. From Table III, it is noted that once again the lowest *THD*s of the input

currents can be achieved under both balanced and unbalanced conditions with the Hybrid ILC current controller.

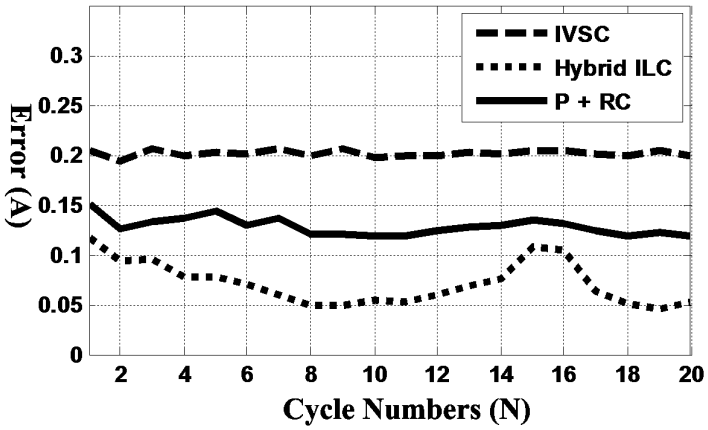


Fig. 7.9 Tracking errors in a-phase currents with the three current controllers for a step change in load from 90 Ω to 60Ω

Fig. 7.8 shows the tracking errors of the *a*-phase current (RMS value) for a step change in *dc* output voltage reference from 175 V to 225 V with 90 Ω *dc* load. As shown in Fig. 7.8, the Hybrid ILC scheme has the smallest errors for input current among the three current controllers. The current error with Hybrid ILC settles down to a low range after four fundamental cycles. Once again, the P+Resonant control scheme has the fastest dynamic response for current tracking among the three current controllers. Though not the fastest, the Hybrid ILC current controller also has satisfactory performance during transient operation. As mentioned earlier, during the first fundamental cycle after a sudden change in the *dc* output voltage reference, only the proportional feedback controller reacts to this change. The ILC controller begins to react only after one fundamental cycle accounting for the slower transient response with the proposed controller compared to the P + Resonant controller.

Fig. 7.9 shows the tracking errors of the *a*-phase RMS current for a step change in *dc* load from 90Ω to 60 Ω with the three different current controllers. It may be noted that the Hybrid ILC current controller again gives the best transient performance for a step load changes among the three methods. This is because a change in load does not change the required control effort much. Due to this, though the current changes, the high performance current tracking will not be affected during load induced transients.

It may be noted that both the steady-state and transient performance provided by IVSC current controller is not as good as P+RC and Hybrid ILC current controllers. As discussed in Section 7.6.1, this could be attributed to the sensitivity of the integral variable structure control to the inherent time delay of 1.5 T_s in the dSPACE experimental system. The implementation of the IVSC current controller with due consideration for this time delay is suggested as a future work to be performed in this area.

In conclusion, the Hybrid ILC current controller provides the best performance among the current controllers investigated with excellent steady-state performance and good transient performance. In the next subsection, more detailed experimental results will be presented and discussed with the Hybrid ILC current controller.

7.7 Detailed experimental results with Hybrid ILC current controller

In this section, detailed experimental results with the Hybrid ILC current

controller will be provided.

7.7.1 Steady-state operation

The three-phase input supply voltage is kept at 60V (RMS) as before for the balanced operating condition. Fig. 7.10 shows the reduction in current error on sudden application of the ILC controller. Initially, only the proportional feedback control is activated together with supply voltages being employed as a feed-forward signal to achieve disturbance rejection. There is a significant steady-state error as shown in Fig. 7.10. Subsequently, the ILC controller is brought in. It takes one fundamental period to gather the previous error and to form the ILC control effort. After it gets enough information, the ILC controller begins to function as shown in Fig. 7.10. It can be seen from Fig. 7.10 that the steady-state error has been dramatically minimized after about two or three fundamental cycles. This coincides with the theoretical expectation based on (7.35). The learning gain and proportional gain used here are 0.15 and 0.3, respectively, which result in an error convergence rate of $(0.5)^n$.

When the system enters steady-state, as mentioned earlier, the ILC reduces error from cycle to cycle. Fig. 7.11 shows one phase current and its corresponding error during steady-state operation. The steady state error is very low and largely within $\pm 0.1A$. The line current exhibits an extremely low THD of about 1.2 %. As discussed earlier, the likely cause of the small tracking error that still remains is the use of the forgetting factor in the learning law.

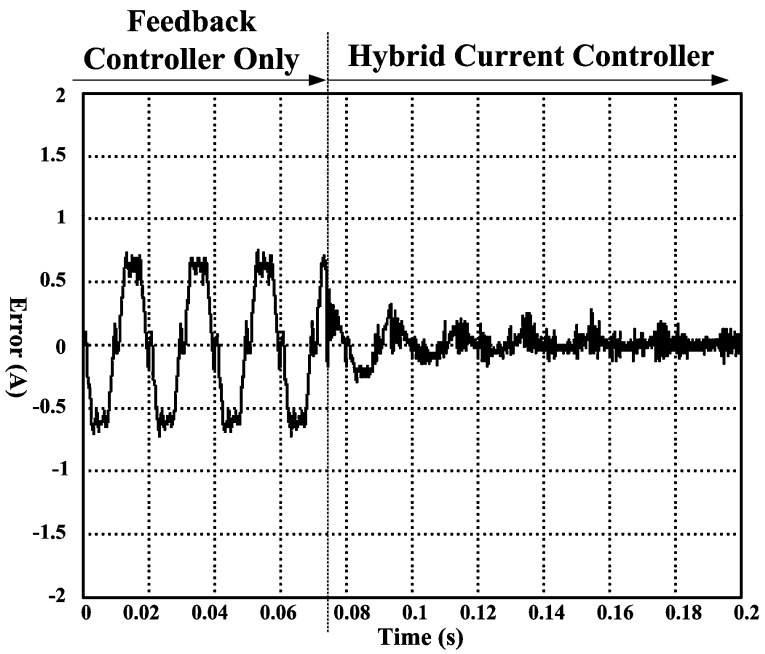


Fig. 7.10 Reduction in current tracking error on application of ILC – Hybrid ILC current controller

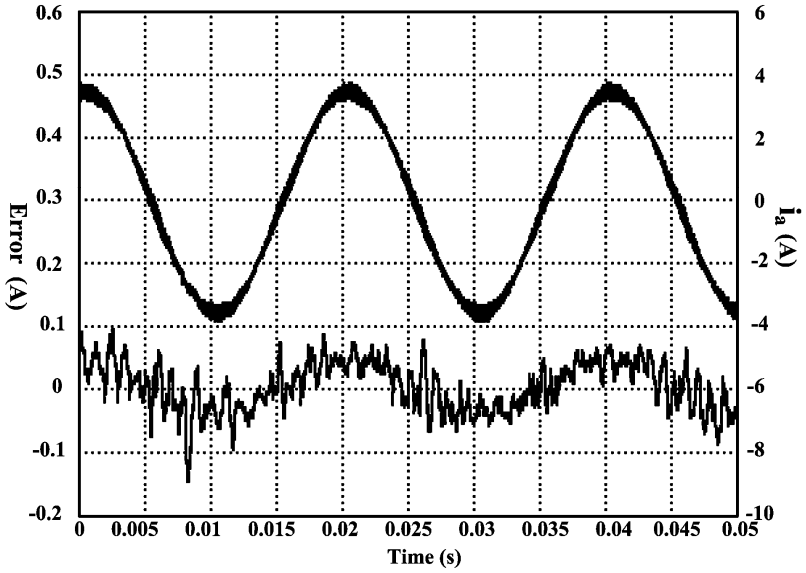


Fig. 7.11. Steady-state experimental result: a-phase current (scale: 2 A/div) and a-phase error (scale (0.1 A/div) – Hybrid ILC current controller

The experimental results under unbalanced conditions with the proposed method are shown in Fig. 7.12. The supply voltages for the experiments under unbalanced conditions were again set at $42\sqrt{2}\sin(\omega t + 355^\circ)$, $75\sqrt{2}\sin(\omega t + 236^\circ)$

and $66\sqrt{2}\sin(\omega t + 90^{\circ})$. As indicated before, these values correspond to a positive sequence voltage of around 60 V (RMS) at a phase of -13^{o} and a negative sequence voltage of around 20 V (RMS) at a phase of 148^{o}. The current waveforms are nearly sinusoidal, and the *dc* output voltage is nearly constant with low ripple. The measured THDs for the three line currents were 1.13%, 1.43%, 1.52%, respectively, which are very low.

Thus, it has been demonstrated that the proposed ILC based hybrid current controller can provide excellent steady-state performance for both balanced and unbalanced operation of the PWM rectifier.

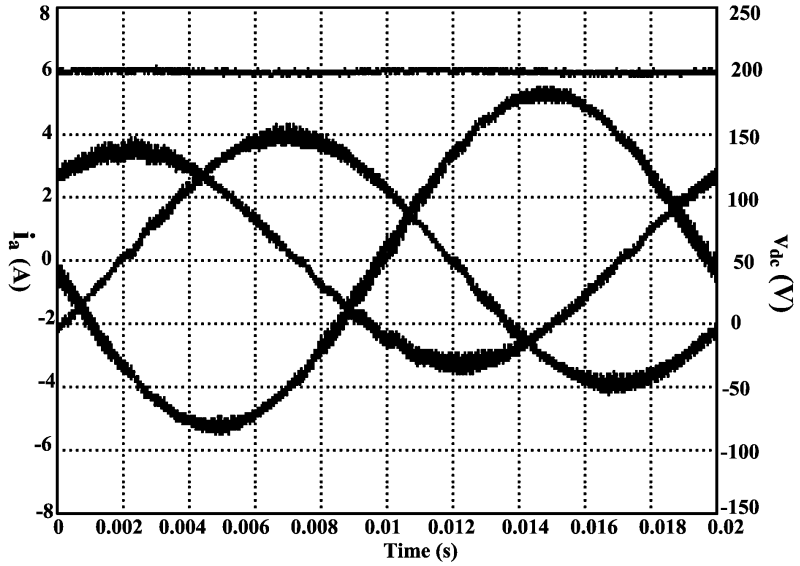


Fig. 7.12 Experimental waveforms for unbalanced supply voltages condition – Hybrid ILC current controller

7.7.2 Transient operation

The next three experiments have been carried out to examine the dynamic performance of the Hybrid ILC current controller. The first experiment (Fig. 7.13)

was conducted with only the current loop closed. The last two experiment results shown in Fig. 7.14 and Fig. 7.15 were obtained with both the voltage loop and current loop closed.

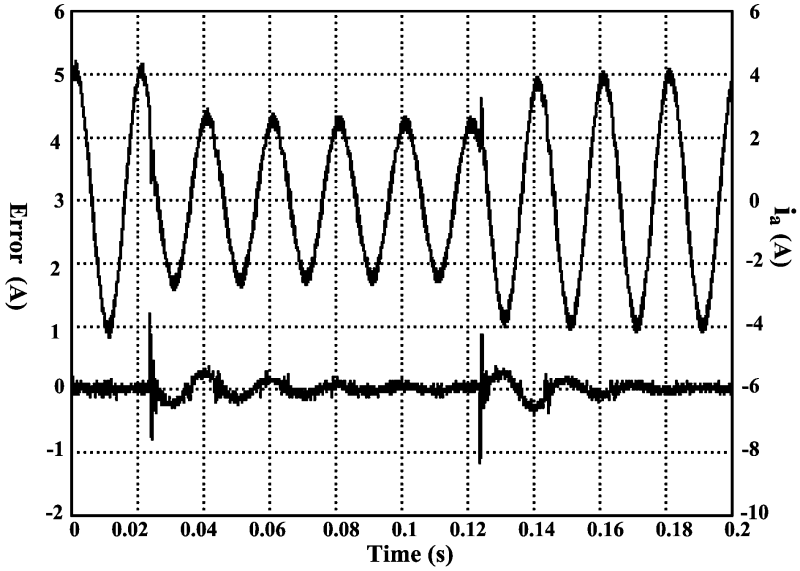


Fig. 7.13 Experimental transient responses for a step change in current reference from 4.2 A to 2.4 A and back to 4.2 A – Hybrid ILC current controller with only the current loop closed

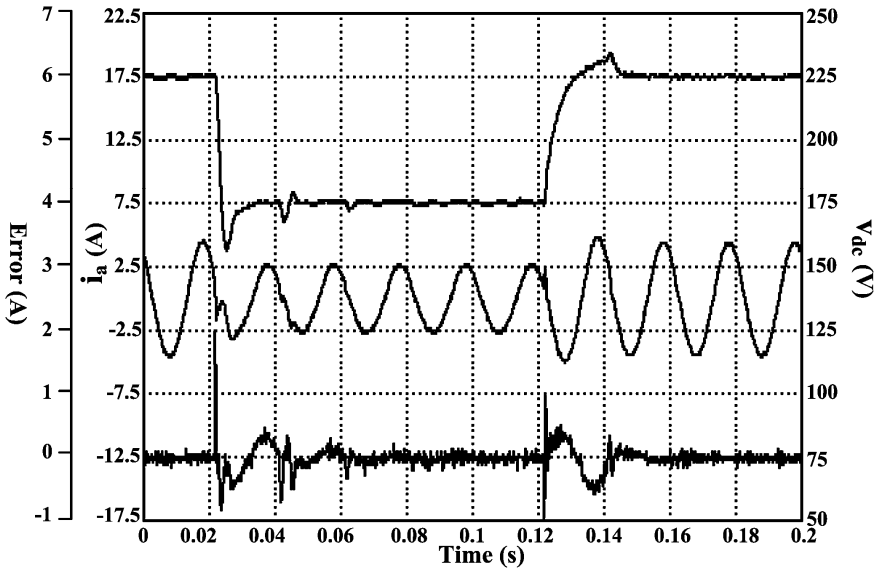


Fig. 7.14 Experimental transient response for a step change in *dc* output voltage reference from 225 V to 175 V and back to 225 V – Hybrid ILC current controller with both the voltage and current loops closed

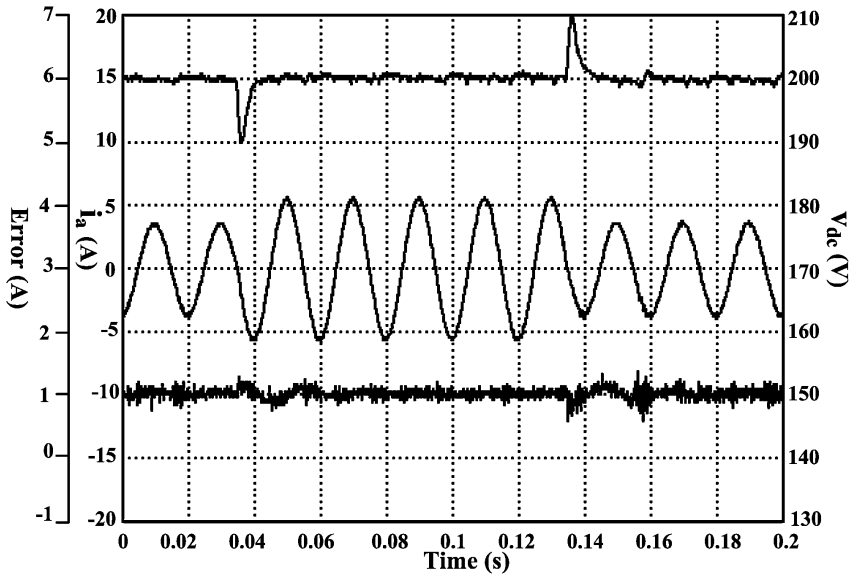


Fig. 7.15 Experimental transient response for a step change in load from 90 Ω to 60 Ω and back to 90 Ω – Hybrid ILC current controller with both the voltage and current loops closed

Fig. 7.13 shows the transient responses of the a-phase current and a-phase current error to changes in current command from 4.2 A to 2.4 A and then back to 4.2 A. As shown in the figure, the actual current tracks its reference effectively. It takes about two or three fundamental cycles for error convergence to be achieved.

Fig. 7.14 shows the transient responses of the *dc* output voltage, the a-phase current, and the a-phase error signal with the proposed Hybrid ILC current controller for a step change in the voltage reference from 225 V to 175 V and then back to 175 V with a load of 90Ω. During both the transitions, the change in current is quite abrupt and the tracking error also increases quite abruptly. At the transition, there is a notable spike in the current tracking error which is then rapidly reduced by the operation of the P-controller. In the first fundamental cycle after the step change in the *dc* output voltage, only the proportional controller responds to this sudden change. Thereafter, the ILC controller constructs its current effort based on this

particular cycle's error signal. After one fundamental cycle, the ILC starts to function effectively and reduces the tracking error monotonically.

Fig. 7.15 shows the transient responses of the *dc* output voltage, the a-phase current, and a-phase error signal with the proposed Hybrid ILC current controller to a change in load resistance from 90 Ω to 60 Ω and back to 90 Ω. The response times are around 0.5ms for both step decrease and step increase in load resistance. The undershoot and the overshoot in the *dc* output voltage during the two transient situations are both 10 V as may be observed in Fig. 7.15. The voltage responses during both load changes are quite fast. It is again noted that the tracking error for the current is quite small even during the instants when large step load change was introduced. The likely reason, as explained earlier, is that the control effort is unaffected by the changes in load. Thus, this transient performance is mainly determined by the voltage loop controller.

Thus, the experimental results show that the proposed Hybrid ILC current controller exhibits very good performance under both steady-state and transient operating conditions.

The switching frequency in our work has been kept at 10 kHz, which is a typical value for medium power (< 20 kW) rectifier applications. An issue of importance to a system designer is the relationship between switching frequency and control performance. This is beyond the scope of the present work and has not been investigated. However, it is worth noting that with a higher switching frequency, the

Hybrid ILC current controller's performance is likely to remain unaltered, while the performance of the integral variable structure control is likely to be improved further.

7.8 Conclusions

The following conclusions can be drawn from this chapter.

Two current tracking schemes based on integral variable structure control and iterative learning control were proposed in this chapter. The working principles and design issues were discussed in detail.

For comparison purposes, the widely used dual current controller and the recently developed P + Resonant current controller were also discussed and implemented.

Experimental results showed that the proposed Hybrid ILC current control can provide excellent steady-state performance and good transient performance suggesting that this is a promising technique for use with the PWM rectifier.

CHAPTER 8
CONCLUSIONS AND FUTURE WORK

8.0 Introduction

Though the PWM rectifier has become very popular in recent years in most three-phase *ac*-to-*dc* applications due to its several potential advantages, problems still remain with regard to its modeling and control as discussed in this thesis earlier. The aim of the research work reported in this thesis was to provide solutions to the problems associated with such a PWM rectifier system operating under both balanced and unbalanced supply voltage conditions. The problems identified and the key solutions proposed in this thesis fall under the following four categories:

- A control-oriented model is required in order to exploit the potential benefits of a PWM rectifier under balanced supply conditions. To meet this requirement, a dual SISO model for the PWM rectifier under balanced operating conditions has been proposed.

- The available power-oriented regulation techniques for ensuring that the salient advantages of a three phase PWM rectifier are retained even under unbalanced supply voltage conditions were found to fall short of expectations in their performances. A new ‘output power control’ (OPC) scheme capable of high input and output performance has been proposed. In addition, the reason for the existing ‘partial output power control (POPC) scheme’ not fulfilling its promise of good performance was investigated.

With the alternative implementation proposed in the present work, the existing POPC scheme was also shown to be capable of achieving excellent performance under unbalanced supply conditions.

- The commonly used measure of vector power factor (VPF) to account for the power factor of the load was found to be inadequate in accurately reflecting the power flow conditions under unbalanced operation. The alternative definition of effective power factor (EPF) was used to properly evaluate the performances obtained with four different power regulation schemes.

- In order for the PWM rectifier control techniques to function properly, the inner loop current control must be capable of excellent performance with sinusoidal input currents at the set values and fast dynamics. A hybrid iterative learning control (Hybrid ILC) was proposed and shown to be capable of near perfect tracking of the reference unbalanced currents.

8.1 PWM rectifier system under balanced supply

8.1.1 Development and verification of a dual SISO model

A dual SISO model for a three-phase PWM rectifier operating under balanced supply conditions at unity power factor was developed to give meaningful insights into the behavior of a PWM rectifier system and to facilitate the design of controllers. This work has been presented in Chapter 3.

With the proposed model, the *q*-axis model becomes a first order linear system determining the power factor regulation whereas the *d*-axis model becomes a second-order non-linear system determining the power delivery. The open loop characteristic of the *d*-axis model was investigated and verified through analysis, simulations and experiments in both frequency domain and time domain. The experimental results obtained in both time domain and frequency domain validate the proposed *d*-axis SISO model suggesting that the proposed dual SISO model, though simple, can indeed reflect accurately the characteristics of a three-phase PWM rectifier.

One of the advantages of the proposed equivalent *d*-axis SISO model is that the non-minimum phase feature associated with a three-phase PWM rectifier is simplified as a RHP zero appearing on the small-signal control-to-output transfer function. This allows the limit on the realizable closed-loop bandwidth of a PWM rectifier system imposed by the non-minimum phase feature to be accurately predicted by the knowledge of the location of the RHP zero. This, in turn, facilitates the design of the stable controllers for the system.

Besides, the proposed equivalent *d*-axis SISO model is found to be similar to the model of a traditional *dc-dc* boost converter. This finding opens possible avenues for controlling PWM rectifier systems by directly extending the well-developed control design and system analysis techniques of *dc-dc* converters to PWM rectifiers.

8.1.2 Voltage-mode and inner current loop based controllers

Voltage mode and inner current loop based control techniques, widely used in *dc* to *dc* converters, were then applied to the control of the PWM rectifier system based on the insight that both the *d*-axis model and its equivalent circuit of the PWM rectifier exhibit similarities to those of the *dc* to *dc* boost converter.

The steady-state and transient performances for step changes in output voltage reference, *dc* load, and supply voltage were experimentally investigated. Results show that both the voltage and the inner current loop based controllers yielded satisfactory performance with zero steady-state error and fast transient responses. The comparison results suggest that better performance can be achieved with the inner current loop based control scheme.

Successful implementation of both voltage mode and inner current loop based controllers further justify the validity of the proposed dual SISO model suggesting feasibility of controlling PWM rectifier systems with the well-developed control design and system analysis techniques of *dc*-*dc* converters.

8.2 PWM rectifier system under unbalanced supply

8.2.1 Proposal of an output power control (OPC) scheme

A control method for the three-phase PWM rectifier under unbalanced supply condition based on an output power control (OPC) strategy was proposed and evaluated in Chapter 4. In the proposed scheme, constant instantaneous power and

zero reactive power are both maintained at the rectifier bridge input terminals. The current commands are appropriately determined resulting in the ripple in the input power equaling the instantaneous power in the line inductances. Simple closed form solutions for the current commands have been obtained, which makes the scheme easily implementable. It was also established that though the power factor was not directly controlled, the resultant vector power factor with the proposed scheme was almost unity.

Experimental results with the proposed OPC scheme on a 1 kW laboratory prototype have been presented. It has been shown that, as expected, the system with the proposed control scheme exhibits both high input and output performances during both steady-state and transient operations. The proposed output OPC method fulfills all of the main objectives of a high performance PWM rectifier, viz., sinusoidal input currents with high power factor and ripple free *dc* output voltage, under unbalanced supply voltage conditions.

8.2.2 Improved realization of a partial output power control (POPC) scheme

Ref. [51] has proposed a control method for achieving the objectives of PWM rectifier control; this method has been named in the present work as ‘partial output power control (POPC) scheme. In Chapter 5, the reasons for the poor experimental results obtained in [52] with POPC have been investigated. In the POPC method, the rectifier bridge input voltages have been estimated by using the *dc* output voltage

together with switching function signals (‘Estimation Method 1’) and then used as known variables to construct current commands. This results in an additional feedback loop within the system, which is identified as the likely cause preventing the effective implementation of the POPC scheme. However, it was found difficult to perform a theoretical stability robustness analysis of the POPC scheme due to the scheme’s complexity.

An alternative way to estimate the rectifier bridge input voltages using the supply input voltage and line currents (‘Estimation Method 2’) was then investigated. This method has been used successfully in the proposed OPC method in Chapter 4.

It was found that in the OPC method also a similar additional feedback loop is formed if Estimation Method 1 is used. Theoretical stability robustness analyses were performed on the OPC method using both Estimation Method 1 and Estimation Method 2 for sensing the bridge rectifier input voltages. Based on the insight gained, it is conjectured that the reason for the poor experimental performance of the POPC method reported in literature is also due to the use of Estimation Method 1 and the resulting addition control loop.

Both simulations and experiments have been carried out for verifying the hypothesis. With the Estimation Method 2, the POPC method was shown to provide sinusoidal line currents, constant *dc* output voltage and unity vector power factor operation – high performance in both input side and output side. The problems which occurred with Estimation Method 1 were shown not to occur with the Estimation

Method 2.

8.2.3 Performance evaluation of power regulation schemes for unbalanced supply conditions

Although unity vector power factor (VPF) operation can be achieved with the POPC method, it was found from experimental results that the line currents are not in phase with their corresponding supply voltages. Thus, it appears that the vector power factor provides an over-optimistic estimation of the effectiveness of power transmission. This issue was investigated in Chapter 6.

It was established in Chapter 6 that the concept of EPF (Effective Power Factor) [7] accurately reflects the effects of both reactive power flow and supply imbalance on the power flow condition, unlike the concept of VPF which takes into account only the reactive power flow in the system. Due to this, in this thesis, EPF has been advocated to appropriately estimate power flow condition in a three phase PWM rectifier system.

Four power regulation schemes were then evaluated thoroughly for input side and output side performances. The schemes include a new voltage - oriented control method (VOC) and the three power-oriented control schemes discussed earlier.

The newly proposed VOC scheme is based on the simple idea of directly extending the voltage oriented control method for the balanced supply input case available in literature to the unbalanced supply case also. This new VOC scheme is included since it is the only method theoretically capable of achieving unity EPF

operation in addition to unity VPF operation. The three power-oriented schemes which were evaluated in Chapter 6 are the input power control (IPC) method, the output power control (OPC) method and the partial output power control (POPC) method (with Estimation Method 2), which have been introduced in earlier chapters.

A generalized, overall theoretical framework for a PWM rectifier operating under unbalanced supply conditions has been proposed for these three schemes in order to help in the reviewing and the understanding of the different power regulation methods under unbalanced supply conditions.

The achievable power factors (VPF and EPF) were theoretically assessed for the four power regulation schemes. The correctness of the obtained theoretical expressions of the achievable VPF and EPF were then verified by simulation results.

The experimental performance of these four control methods were evaluated in terms of the obtained EPF, current THDs and peak-peak *dc* output voltage. It was found that the VOC can provide good input performance. However, a second harmonics ripple will appear on the dc link voltage. It was also found that the OPC method and the POPC method provide high performances on both the input side and the output side.

However, further investigations into the stability robustness of the realization of the POPC scheme is required so as to fully explore the scheme's potential strengths and weaknesses. This has been suggested in Section 8.4 as one of the future research issues that need to be addressed in this area.

Based on the investigations in Chapter 6, it is concluded that the OPC method is capable of achieving high performance on the input side and output side and thus is a promising choice for the control of three phase PWM rectifier under unbalanced supply conditions.

8.3 Current Tracking Schemes

The experimental results under unbalanced supply operation presented in Chapter 6 utilized the widely used dual current control scheme for the inner current loops. In these results, it was found that the distortions in the line currents become large when the amplitudes of the currents are small. In order to improve the input side performance with regard to the quality of the input current, two current tracking schemes based on integral variable structure control and iterative learning control (named 'Hybrid ILC') were proposed in this thesis and investigated. For comparison purposes, the dual current controller and the recently developed P + Resonant current controller were also discussed and implemented.

Experimental tests of the current tracking schemes were conducted on a 1 kW laboratory prototype PWM rectifier. The tests were carried out with only the current loop closed first and then with both the current loop and the voltage loop closed for the four current controllers. It was found that the Hybrid ILC current controller provides the best performance among the four current controllers investigated with excellent steady-state performance and good transient performance. Contrary to expectations, the experimental results obtained with the IVSC current controller were

not as good as the P+RC and Hybrid ILC current controllers. This could be attributed to the sensitivity of the IVSC current controller to the inherent time delay of $1.5T_s$ in the dSPACE experimental system.

The relationship between switching frequency and control performance is beyond the scope of the present work and has not been investigated. However, it is worth noting that with a higher switching frequency, the Hybrid ILC current controller's performance is likely to remain unaltered, while the performance of the integral variable structure control is likely to be improved further.

Detailed experimental results of the proposed Hybrid ILC scheme were then presented to show the effectiveness of this current control approach.

This finding is of considerable importance because it suggests a promising control technique for controlling periodic currents commonly existing in power converters applications.

8.4 Future work

Some issues that can be considered for future research are given below.

8.4.1 Solutions to dynamic response problem due to RHP zero

Our work in this thesis has focused on the development of a simple control oriented model for operation under balanced supply conditions. In our study, large valued inductors were used so as to make the effect of RHP zero on the system performance significant. By a coincidence, this has resulted in the corner frequency

of resonant peak of the control to output transfer function being 110 Hz. This might excite power fluctuations with twice mains frequency under unbalanced conditions.

In general, a small value of inductor reduces the RHP zero effect while increasing the line current ripple. Further investigations on the optimum design of the inductor and its effect on system steady-state and dynamic performance need to be carried out.

8.4.2 PWM rectifier functioning as an active power filter

As a solution to harmonic pollution problems caused by non-linear loads on utility, active power filters have attracted considerable attention in the last two decades. By injecting the harmonic currents required by the non-linear load, only active currents are drawn from the utility by the load-active power filter combination.

Since a three-phase PWM rectifier has the same topology as an active power filter, it can function as an active power filter with the incorporation of suitable harmonic current detection technique and current tracking scheme. Some research [93] has been done on this topic so far. As the current controller's task is to track the high frequency harmonic current, future work may adapt the current tracking techniques investigated in the present work to the active filter application.

8.4.3 FPGA based implementation of PWM rectifier control to overcome time delay problem

In our research, the control schemes were realized using dSPACE DSP system (DS1104), which uses a floating processor MPC8240 as the main processor, and a TMS320F240 motion control DSP, as an interface with the power converter as mentioned earlier. However, it was found in the experiment that the system contains a time delay of 1.5 times sampling period (switching period) from sampling action to updating PWM signals action. Processing and calculation may account for this time delay. The presence of this time delay may also be attributed to the communication and interruption cooperation modes between slave DSP and main processor, because of manipulation of slave DSP as interface between the main processor MPC824 and the PWM rectifier system in the dSPACE system. Whatever the reason, due to the presence this time delay as well as parameter variations, the realizable closed-loop bandwidth of the system, which is already limited by the location of RHP zero will be reduced even further.

FPGA based implementations have been widely used in power converters to reduce computational time and cost. It is a promising avenue for real-time implementation of a PWM rectifier control system.

8.4.4 Further investigations into Power Regulation methods

With the improved implementation proposed in Chapter 5, the POPC method can provide high performances on both input and output sides under the certain

operating conditions. However, the improved implementation was obtained by directly applying the conclusions drawn from the OPC method to the POPC method. No theoretical basis was established with an analysis specifically for the POPC method. It is suggested that a stability analysis should be carried out for the POPC method.

As mentioned in Chapter 5, to fully explore the strength of the POPC method, more theoretical research should be done to find a proper realization technique for the POPC method including the exploration of the stability robustness range of the POPC method with Estimation Method 2.

In addition, the effect of mains voltage distortion and circuit parameter variations on the power regulation methods should be also investigated for a comprehensive analysis.

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Appendix A
Non-minimum Phase Feature in a PWM Rectifier

A.0 Introduction

The problems associated with a PWM rectifier under balanced supply voltages conditions are explored in this appendix. The discussion is based on the information in [26]. In both Chapter 2 and Chapter 3, it states that the three-phase PWM rectifier has a multi-input multi-output (MIMO) nonlinear structure with a non-minimum phase feature. Appendix A provides background information of non-minimum phase feature of a three-phase PWM rectifier for both Chapter 2 and Chapter3.

A.1 State-space-averaged model of a PWM rectifier system in SRF

The differential equations for a three-phase PWM rectifier in the *d-q* synchronously rotating frame (SRF) have been given in the Chapter 2 and are reproduced below.

$$\begin{aligned}
\frac{di_d}{dt} &= -\frac{Ri_d}{L} + \omega i_q + \frac{e_d}{L} - \frac{v_{dc}}{2L}u_d \\
\frac{di_q}{dt} &= -\frac{Ri_q}{L} - \omega i_d + \frac{e_q}{L} - \frac{v_{dc}}{2L}u_q \\
\frac{dv_{dc}}{dt} &= \frac{3}{4C}(u_d i_d + u_q i_q) - \frac{i_{Rdc}}{C}
\end{aligned} \tag{A.1}$$

Here, e_d, e_q, and i_d, i_q denote the *d*-axis and *q*-axis input voltages and input currents in the SRF and u_d, u_q are the *d*-axis and *q*-axis switching functions.

Although the model in SRF has the merits of dealing with only *dc* quantities, less control inputs/states and clearer physical insights into power factor management and power transfer capability compared to the model in the *a-b-c* natural frame, it suffers from multi-input multi-output (MIMO) non-linear structure and the presence of a non-minimum phase feature. These properties are obstacles in fully understanding the behavior of the three-phase PWM rectifier system; they also complicate the control design.

A.2 Presence of non-minimum phase feature in the system model

In a linear setting, non-minimum phase implies that the system has right half plane (RHP) zero(s). This notion has been extended to non-linear system by identifying the stability of the zero dynamics. The zero dynamics is defined as the internal dynamics of the system when the system outputs are maintained at their references by the control input.

A.2.1 Voltage control scheme

As the control objective is to regulate the *dc* output voltage and maintain unity power factor operation, it is natural to choose output variables as $y_{1=}$ [i_q, v_{dc}] and output references as [0, V_r]. To fulfill these control objectives, the control inputs are selected using input-output linearizing feedback [26] as follows:

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} 0 & -\frac{v_{dc}}{2L} \\ \frac{3i_d}{4C} & \frac{3i_q}{4C} \end{bmatrix}^{-1} \left(\begin{bmatrix} \omega i_d + \frac{R}{L} i_q - \frac{e_q}{L} \\ \frac{1}{C} i_{Rdc} \end{bmatrix} + v \right), \tag{A.2}$$

where v is the proportional feedback control with $v = \begin{bmatrix} k_1(0 - i_q) \\ k_2(V_r - v_{dc}) \end{bmatrix}$.

With control inputs given by (A.2), the internal dynamics becomes

$$\frac{di_d}{dt} = -\frac{R}{L} i_d + \frac{e_d}{L} - (\frac{R}{L} + k_1) \frac{i_q^2}{i_d} - \frac{2v_{dc} i_{Rdc}}{3Li_d} + \frac{2Ck_2 v_{dc}(V_r - v_{dc})}{3Li_d} + \frac{e_q i_q}{Li_d} \tag{A.3}$$

The zero dynamics can be obtained when i_q approaches zero and v_{dc} approaches V_r. The zero dynamics is given as follows:

$$\frac{di_d}{dt} = -\frac{R}{L} i_d + \frac{e_d}{L} - \frac{2V_r^2}{3LR_{dc} i_d}, \tag{A.4}$$

where $i_{Rdc} = \frac{V_r}{R_{dc}}$.

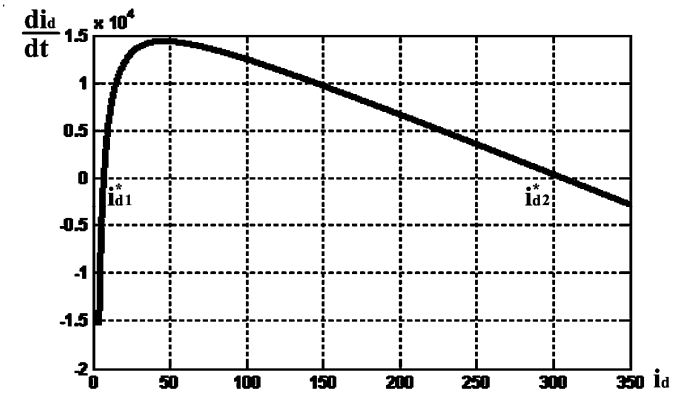

Fig.A.1 Phase trajectory of the zero dynamics of the voltage control scheme

Fig A.1 depicts phase trajectory of zero dynamics of the voltage control scheme. Here, the system parameters used to plot phase trajectory of the zero dynamics given

in Fig. A.1 are R=0.27Ω, L=4.15mH, V_r=200V, R_{dc}=45Ω and e_d= 60$\sqrt{2}$ V. As shown in Fig A.1, there are two equilibrium points i_{d1}^* and i_{d2}^*. At the first equilibrium point i_{d1}^*, the d-axis current has a reasonable amplitude. However, it is an unstable node, as once d-axis current deviates from the equilibrium point value of i_{d1}^*, it will never come back. On the other hand, the second equilibrium point is a stable node. However, the current drawn here is extremely large for the same power delivery, and hence this is not a practical operating point for the PWM rectifier. As the reasonable operating point (i_{d1}^*) does not provide stable operation based on the analysis of zero dynamics, we may claim that the system is of non-minimum phase with output y_1.

A.2.2 Current control scheme

Instead of using y_1 as the set of output variables, the set y_2 = [i_q, i_d] can be chosen as output and be regulated at their references [0 i_d^*] [26]. As before, to fulfill the control objectives, the control inputs are selected using input-output linearizing feedback as follows:

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} -\frac{v_{dc}}{2L} & 0 \\ 0 & -\frac{v_{dc}}{2L} \end{bmatrix}^{-1} \left(\begin{bmatrix} -\omega i_q + \frac{R}{L} i_d - \frac{e_d}{L} \\ \omega i_d + \frac{R}{L} i_q - \frac{e_q}{L} \end{bmatrix} + v' \right), \tag{A.5}$$

where v' is a proportional feedback control with $v' = \begin{bmatrix} k_3(i_d^* - i_d) \\ k_4(0 - i_q) \end{bmatrix}$.

The desired d-axis current command can be obtained from steady-state solution of the PWM rectifier given by (A.1) by setting v_{dc} as V_r and i_q to null. The current command is given below

$$I_d^* = \frac{1}{2}[\frac{e_d}{R} - \sqrt{(\frac{e_d}{R})^2 - \frac{8V_r^2}{3R}}] \tag{A.6}$$

However, due to parameter variations and parasitical losses, the ideal current command itself may not bring the *dc* output voltage to its reference. Therefore, error in the *dc* output voltage is feedback to adjust the current command as follows.

$$i_d^* = I_d^* + k_5(V_r - v_{dc}) \tag{A.7}$$

This is the case in the often used current mode control approach where the current command for the inner current control loop is generated by an outer voltage control loop.

The zero dynamics can be obtained when i_q approaches zero and i_d approaches I_d^*. The zero dynamics is given as follows:

$$\frac{dv_{dc}}{dt} = \frac{(V_r^2 - v_{dc}^2)}{CR_{dc}v_{dc}} - \frac{3LkI_d^*}{2Cv_{dc}}(V_r - v_{dc}), \tag{A.8}$$

where $k=k_3k_5$.

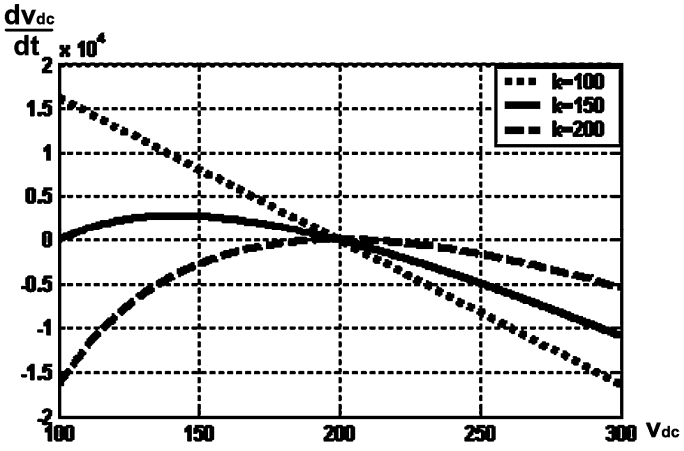

Fig. A.2 Phase trajectory of the zero dynamics of the current control scheme

Phase trajectory of the zero dynamics of current control scheme is shown in Fig. A.2. The stability of the zero dynamics is dependent on the chosen value of the parameter k. As shown in Fig. A.2, with increasing value of k, the zero dynamics becomes unstable. Fig. A.2 also illustrates that any attempt to speed up the control by increasing control gain will lead to unstable operation. Thus, we may claim that the system is of non-minimum phase with output vector y_2 also.

Thus, we can conclude that both the current control and the voltage control schemes may lead to unstable zero dynamics suggesting the existence of non-minimum phase property in a PWM rectifier system.

Appendix B
Model of a Three-Phase PWM Rectifier in an Unbalanced System and Separation of Sequential Components

B.0 Introduction

In this appendix, model of a three-phase PWM rectifier in an unbalanced system will be developed and the separation techniques adopted for sequential components in Chapter 4 will be explained. The organization of this appendix is as follows. In Section B.1, symmetrical components analysis of an unbalanced three-phase power system is first presented. In Section B.2 and B.3, space vector representation of three-phase unbalanced variables in both stationary frame and positive-, negative sequence synchronously rotating frame are derived. In Section B.4, the system model of three-phase PWM rectifier is given. In Section B.5, the separation techniques for the positive sequence components and the negative sequence components are explained. This model and the separation techniques presented in appendix B have been used in the Chapter 4, Chapter 5 and Chapter 6 for dual current control design and implementation.

B.1 Symmetrical components analysis of an unbalanced three-phase power system

In electrical engineering, the method of *symmetrical components* is used to simplify analysis of unbalanced three-phase power systems.

In our analysis, three-phase variables (x_a, x_b, x_c) of fundamental frequency are assumed to be unbalanced and sinusoidal. As *dc* side performance of an *ac-to-dc* power converter is not affected by the zero sequence components, they are not addressed in a three-phase PWM rectifier system.

According to symmetrical components theory, the unbalanced three-phase variables can be represented as the orthogonal sum of positive and negative sequence components as follows:

$$x_a = x_a^p + x_a^n = x^p \cos(\omega t + \theta_x^p) + x^n \cos(\omega t + \theta_x^n) = X_a \cos(\omega t + \theta_a) \quad \text{(B.1)}$$

$$x_b = x_b^p + x_b^n = x^p \cos(\omega t + \theta_x^p - 2\pi/3) + x^n \cos(\omega t + \theta_x^n + 2\pi/3) = X_b \cos(\omega t + \theta_b)$$

$$x_c = x_c^p + x_c^n = x^p \cos(\omega t + \theta_x^p + 2\pi/3) + x^n \cos(\omega t + \theta_x^n - 2\pi/3) = X_c \cos(\omega t + \theta_c) \ ,$$

where x_a^p , x_b^p , x_c^p and x_a^n , x_b^n , x_c^n are the three-phase positive and the negative sequence components, respectively. Also, x^p and x^n are the peak amplitudes of the positive and the negative sequence variables, respectively, θ_x^p and θ_x^n are the corresponding phase values and ω is the angular frequency of the power supply. Variables X_a, X_b, X_c are the peak amplitudes of the three-phase variables and variables θ_a, θ_b, θ_c are angles of three-phase variables.

The symmetrical components equations for the three-phase variables in matrix notation are

$$\begin{pmatrix} \tilde{x}_a^p \\ \tilde{x}_a^n \end{pmatrix} = \frac{1}{3} \begin{pmatrix} 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{pmatrix} \begin{pmatrix} \tilde{x}_a \\ \tilde{x}_b \\ \tilde{x}_c \end{pmatrix} \quad \text{(B.2)}$$

Here, $\tilde{x}_a$, $\tilde{x}_b$ and $\tilde{x}_c$ corresponds to phasors of three-phase variables (x_a, x_b, x_c)

with $\tilde{x}_a = X_a \angle \theta_a$, $\tilde{x}_b = X_b \angle \theta_b$ and $\tilde{x}_c = X_c \angle \theta_c$. Variables $\tilde{x}_a^p$ and $\tilde{x}_a^n$ correspond to phasors of *a*-phase positive- and negative- sequence components with $\tilde{x}_a^p = x^p \angle \theta_a^p$ and $\tilde{x}_a^n = x^n \angle \theta_a^n$.

The phasors of three-phase variables can be constructed by symmetrical components as follows.

$$\begin{pmatrix} \tilde{x}_a \\ \tilde{x}_b \\ \tilde{x}_c \end{pmatrix} = \begin{pmatrix} 1 & 1 \\ \alpha^2 & \alpha \\ \alpha & \alpha^2 \end{pmatrix} \begin{pmatrix} \tilde{x}_a^p \\ \tilde{x}_a^n \end{pmatrix} \tag{B.3}$$

B.2 Space vector representations in stationary frame

Space vectors are defined using the vector sum of instantaneous phase variables:

$$\vec{x}_s = \frac{2}{3}(x_a(t) + \alpha x_b(t) + \alpha^2 x_c(t)), \tag{B.4}$$

where $\alpha = e^{j\frac{2\pi}{3}} = \cos(\frac{2\pi}{3}) + j\sin(\frac{2\pi}{3})$, $\alpha^2 = e^{j\frac{4\pi}{3}} = \cos(\frac{4\pi}{3}) + j\sin(\frac{4\pi}{3})$ and $\vec{x}_s$ denotes a space vector of three-phase variable in SF.

The space vector at any time is the vector sum of contributions by phases *a*, *b*, *c*. Expressed in the orthogonal complex plane we can rewrite (B.4) as

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix}, \tag{B.5}$$

where x_α and x_β denote the *d*-axis component and the *q*-axis component in SF, respectively.

Using (B.4), (B.5) and by transforming (B.1) into stationary coordinates, we get

$$\vec{x}_s = \vec{x}_s^p + \vec{x}_s^n = x_\alpha + jx_\beta = x^p e^{j\omega t} e^{j\theta^p} + x^n e^{-j\omega t} e^{-j\theta^n} \tag{B.6}$$

As explained in Chapter 4, variables x_α and x_β are the projections of the space vector on the α-axis and β-axis, respectively. Variable $\vec{x}_s^p$ is the positive sequence space vector in SF with $\vec{x}_s^p = x^p e^{j(\omega t + \theta_x^p)}$ which is rotating counter-clockwise with a constant velocity ω and $\vec{x}_s^n$ is the negative sequence space vector in SF with $\vec{x}_s^n = x^n e^{-j(\omega t + \theta_x^n)}$ which is rotating clockwise with a constant velocity ω. Vector $\vec{x}^p$ is the positive sequence stationary vector in the positive sequence SRF with $\vec{x}^p = x_d^p + jx_q^p = x^p e^{j\theta_x^p}$ and $\vec{x}^n$ is the negative sequence stationary vector in the negative sequence SRF with $\vec{x}^n = x_d^n + jx_q^n = x^n e^{-j\theta_x^n}$. Vectors x_d^p and x_q^p are projections of the positive sequence components on the d-axis and q-axis, respectively. Likewise, x_d^n and x_q^n are the projections of the negative sequence components on the d-axis and q-axis, respectively.

From (B.6), it can be seen that the positive sequence components rotate anticlockwise whereas the negative sequence components rotate clockwise in stationary coordinates with identical rotating speeds.

B.3 Space vector representations in positive- and negative-sequence synchronously rotating frame

Positive synchronous reference frame is a coordinate system moving synchronously with the positive space vector. Space vector transformation law from the stationary frame to the positive synchronous coordinate system is given as

$$\vec{x}_{s\_pn}^p = \vec{x}_s e^{-j\omega t}, \tag{B.7}$$

where $\vec{x}^{p}_{s\_pn}$ denotes the vector in the positive sequence SRF with $\vec{x}^{p}_{s\_pn} = \vec{x}^{p} + e^{-j2\omega t}\vec{x}^{n} = x^{p}e^{j\theta^{p}} + x^{n}e^{-j2\omega t}e^{-j\theta^{n}}$ under unbalanced conditions. The positive synchronous reference coordinate is moving anticlockwise at fundamental speed ω.

Expressed in the orthogonal complex plane we can rewrite (B.7) as

$$\begin{bmatrix} x^{p}_{ds} \\ x^{p}_{qs} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x_{\alpha} \\ x_{\beta} \end{bmatrix}, \tag{B.8}$$

where x^{p}_{ds} and x^{p}_{qs} denote the *d*-axis component and the *q*-axis component in positive sequence SRF, respectively.

In similar fashion, negative synchronous reference frame is a coordinate system moving synchronously with the negative space vector. Space vector transformation law from the stationary frame to the negative synchronous coordinate system is given as

$$\vec{x}^{n}_{s\_pn} = \vec{x}_{s}e^{j\omega t}, \tag{B.9}$$

where $\vec{x}^{n}_{s\_pn}$ denotes the vector in the positive sequence SRF with $\vec{x}^{n}_{s\_pn} = e^{j2\omega t}\vec{x}^{p} + \vec{x}^{n} = x^{p}e^{j2\omega t}e^{j\theta^{p}} + x^{n}e^{-j\theta^{n}}$ under unbalanced conditions. The negative synchronous reference coordinate is moving clockwise at fundamental speed ω.

Expressed in the orthogonal complex plane we can rewrite (B.9) as

$$\begin{bmatrix} x^{n}_{ds} \\ x^{n}_{qs} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x_{\alpha} \\ x_{\beta} \end{bmatrix}, \tag{B.10}$$

where x_{ds}^n and x_{qs}^n denote the *d*-axis component and the *q*-axis component in negative sequence SRF, respectively.

B.4 System modeling in positive- and negative- sequence synchronously rotating frames

Since positive sequence commands become *dc* terms in the positive SRF and negative sequence commands likewise become *dc* terms in the negative SRF, the control problem will be changed from tracking type into regulation type, if the positive sequence commands are regulated in the positive SRF and the negative sequence commands are regulated in the negative SRF, respectively. It would then be advantageous to model the positive sequence components and the negative sequence components in their corresponding synchronous reference frames.

The unbalanced three-phase voltage vector can be represented as the orthogonal sum of positive and negative sequence components. The relationship among OF, SF and SRF descriptions of a variable can be written as

$$\vec{x}_s = e^{j\omega t}\vec{x}^p + e^{-j\omega t}\vec{x}^n = \frac{2}{3}(x_a + \alpha x_b + \alpha^2 x_c), \tag{B.11}$$

where $\vec{x}^p = \begin{bmatrix} x_d^p & x_q^p \end{bmatrix}^T$ denotes the positive vector in the positive sequence SRF, and $\vec{x}^n = \begin{bmatrix} x_d^n & x_q^n \end{bmatrix}^T$ denotes the negative vector in the negative sequence SRF.

The voltage equations on the *ac* side of the rectifier for both positive sequence and negative sequence in SF are given in (4.3) and (4.4). Using transformation given in (B.8) and (B.10), the resultant differential equations in both positive and negative SRF can be expressed as

$$\begin{cases} L\dfrac{di_d^p}{dt} = e_d^p - R\cdot i_d^p - u_d^p\cdot\dfrac{v_{dc}}{2} + \omega L i_q^p \\ L\dfrac{di_q^p}{dt} = e_q^p - R\cdot i_q^p - u_q^p\cdot\dfrac{v_{dc}}{2} - \omega L i_d^p \\ L\dfrac{di_d^n}{dt} = e_d^n - R\cdot i_d^n - u_d^n\cdot\dfrac{v_{dc}}{2} - \omega L i_q^n \\ L\dfrac{di_q^n}{dt} = e_q^n - R\cdot i_q^n - u_q^n\cdot\dfrac{v_{dc}}{2} + \omega L i_d^n \end{cases}, \tag{B.12}$$

where $x_d^p = x^p\cos\theta^p$, $x_q^p = x^p\sin\theta^p$, $x_d^n = x^n\cos\theta^n$ and $x_q^n = -x^n\sin\theta^n$.

Eq. (B.12) represents model for a PWM rectifier in an unbalanced system. This model has been used in Chapter 4~6 for dual current control design.

B.5 Separation of sequential components

The model given in (B.12) requires that the unbalanced three-phase variables are separated into positive and negative *d*- and *q*- components. A few methods have been proposed earlier to carry out this separation [49-51]. The method proposed in [51], called delaying method, is an effective method to extract the sequential components of the line voltage without steady-state error. However, the time delay in the scheme introduces a right-half plane zero based on Pade approximation and this makes the method not suitable for current regulator for stability consideration. Therefore, the notch filter approach proposed in [49] is used here to measure sequential components of line current for real-time feedback current controller. The delaying method and notch filter method are briefly explained here in order to make the design procedure complete.

B.5.1 Notch filter

In the positive synchronous rotating frame, the negative sequence components appear as second harmonic components and vice verse. A notch filter with a 100-Hz notch frequency is used in this method to remove the 100-Hz ripple in both the positive and negative synchronous rotating frames [49]. The transfer function of the notch filter used is given by

$$T(s) = \frac{s^2 + \omega_0^2}{s^2 + \omega_0 s / Q + \omega_0^2}, \tag{B.13}$$

where $Q = 10$ and $\omega_0 = 2\pi f = 628.2$.

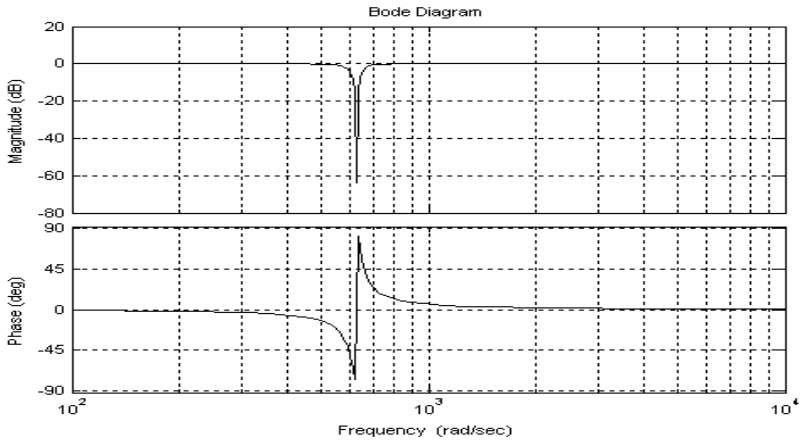

Fig.B.1 Bode diagram for notch filter with notch frequency 100-Hz

B.5.2 Delaying method

This method utilizes a fundamental characteristic of a balanced three-phase system, viz., a phase signal which is delayed by one-third or two-thirds of its period is identical with either of the two remaining phase signals depending on the phase order of the balanced system [8].

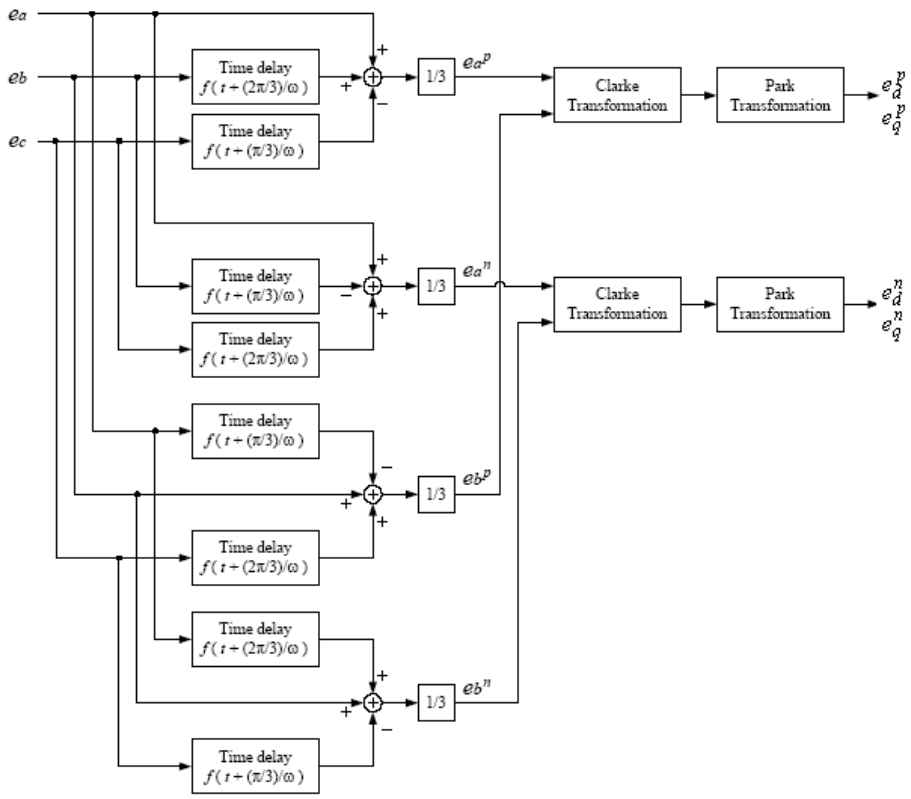

Fig. B.2 Block diagram showing the implementation of the delaying method of calculating symmetrical components in positive and negative sequence rotating frames

The positive and negative components of the each phase voltage can be given by:

$$\begin{cases} e_a^p(t) = \dfrac{1}{3}\left[e_a(t) + e_b(t+T/3) - e_c(t+T/6)\right] \\ e_a^n(t) = \dfrac{1}{3}\left[e_a(t) - e_b(t+T/6) + e_c(t+T/3)\right] \end{cases}$$

$$\begin{cases} e_b^p(t) = \dfrac{1}{3}\left[-e_a(t+T/6) + e_b(t) + e_c(t+T/3)\right] \\ e_b^n(t) = \dfrac{1}{3}\left[e_a(t+T/3) + e_b(t) - e_c(t+T/6)\right] \end{cases} \tag{B.14}$$

$$\begin{cases} e_c^p(t) = \dfrac{1}{3}\left[e_a(t+T/3) - e_b(t+T/6) + e_c(t)\right] \\ e_c^n(t) = \dfrac{1}{3}\left[-e_a(t+T/6) + e_b(t+T/3) + e_c(t)\right] \end{cases}$$

After obtaining positive and negative sequence components of each phase, we can calculate the symmetrical components in the positive and negative rotating frames based on (B.15)

$$\begin{cases} \vec{x}_s^{\,p} = \dfrac{2}{3} e^{j\omega t}(x_a^p + \alpha x_b^p + \alpha^2 x_c^p) \\ \vec{x}_s^{\,n} = \dfrac{2}{3} e^{-j\omega t}(x_a^n + \alpha x_b^n + \alpha^2 x_c^n) \end{cases} \tag{B.15}$$

According to (B.14), the delaying method requires a delay time of one-third of the period which is equal to 6.67ms in the case of supply frequency being 50Hz.

Appendix C
Small Signal Model for the *d*-Axis Dynamics

In this Appendix, open loop and closed-loop transfer functions of *d*-axis dynamics of a PWM rectifier are derived. These transfer functions have been summarized in Table 3.1 and Table 3.4 of Chapter 3. These transfer functions have been used for open loop characteristic verification and design of the voltage mode and inner current control based schemes.

C.0 Open loop transfer functions

The state-spaced averaged equations of the equivalent circuit shown in Fig. 3.4(b) can be written as

$$\begin{bmatrix} \dot{v}_{dc} \\ \dot{i}_d \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_{dc}C} & \frac{3}{4C}(1-d) \\ -\frac{(1-d)}{2L} & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} v_{dc} \\ i_d \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} e_d \,. \tag{C.1}$$

Ignoring the parasitic resistance *R*, the steady state solutions are obtained by equating the rate of change of the dynamic variables to zero.

$$\begin{bmatrix} -\frac{1}{R_{dc}C} & \frac{3}{4C}(1-d) \\ -\frac{(1-d)}{2L} & 0 \end{bmatrix} \begin{bmatrix} v_{dc} \\ i_d \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} e_d = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{C.2}$$

The average current and output voltage can be obtained from (C.2) as

$$V_{dc} = \frac{2E_d}{1-D} \quad \text{and} \quad I_d = \frac{8E_d}{3R_{dc}(1-D)^2} \tag{C.3}$$

Perturbations are introduced in the control inputs for obtaining the small signal model. Let the perturbed variables be

$$v_{dc} = V_{dc} + \hat{v}_{dc}, \tag{C.4.a}$$

$$i_d = I_d + \hat{i}_d, \tag{C.4.b}$$

$$d = D + \hat{d}, \quad \text{and} \tag{C.4.c}$$

$$e_d = E_d + \hat{e}_d. \tag{C.4.d}$$

Applying the perturbed variables to (C.1), removing the dc terms and neglecting the higher order nonlinear terms, the small-signal model can be obtained as follows.

$$\begin{bmatrix} \dot{\hat{v}}_{dc} \\ \dot{\hat{i}}_d \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_{dc}C} & \frac{3}{4C}(1-D) \\ -\frac{(1-D)}{2L} & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} \hat{v}_{dc} \\ \hat{i}_d \end{bmatrix} + \begin{bmatrix} -\frac{3}{4C} I_d \\ \frac{V_{dc}}{2L} \end{bmatrix} \hat{d} + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} \hat{e}_d \tag{C.5}$$

Substituting (C.3) into (C.5), we get

$$\dot{\hat{x}} = A\hat{x} + f\hat{d} + b\hat{e}_d, \tag{C.6}$$

where $\hat{x} = \begin{bmatrix} \hat{v}_{dc} & \hat{i}_d \end{bmatrix}^T$, $A = \begin{bmatrix} -\frac{1}{R_{dc}C} & \frac{3}{4C}(1-D) \\ -\frac{(1-D)}{2L} & -\frac{R}{L} \end{bmatrix}$, $f = \begin{bmatrix} -\frac{2E_d}{R_{dc}C(1-D)^2} \\ \frac{2E_d}{L(1-D)} \end{bmatrix}$ and $b = \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix}$.

Taking Laplace Transform, we have

$$(sI - A)\hat{x}(s) = f\hat{d}(s) + b\hat{e}_d(s) \tag{C.7}$$

The control gain functions are defined as

$$F_v(s) = \frac{\hat{v}_{dc}(s)}{\hat{d}(s)}\Big|_{\hat{e}_d=0} = [1 \quad 0](sI - A)^{-1} f \tag{C.8.a}$$

$$F_i(s) = \frac{\hat{i}_d(s)}{\hat{d}(s)}\Big|_{\hat{e}_d=0} = [0 \quad 1](sI - A)^{-1} f \tag{C.8.b}$$

The audio susceptibility function is defined as

$$F(s) = \frac{\hat{v}_{dc}(s)}{\hat{e}_d(s)}\Big|_{\hat{d}=0} = [1 \quad 0](sI - A)^{-1} b \tag{C.9}$$

The audio susceptibility of the converter quantifies the output response for input variations.

Neglecting the inductor parasitic resistance *R*, we can obtain the following expressions for the variations of the *dc* output voltage $\hat{v}_{dc}(s)$ and input current $\hat{i}_d(s)$ for perturbations in the duty cycle *d(s)*.

$$F_v(s) = \frac{\hat{v}_{dc}(s)}{\hat{d}(s)} = \frac{2e_d}{(1-D)^2} \frac{1 - \dfrac{8L}{3R_{dc}(1-D)^2} s}{1 + \dfrac{8L}{3R_{dc}(1-D)^2} s + \dfrac{8LC}{3(1-D)^2} s^2} \tag{C.10.a}$$

$$F_i(s) = \frac{\hat{i}_d(s)}{\hat{d}(s)} = \frac{16e_d}{3D^3 R_{dc}} \frac{1 + \dfrac{R_{dc}C}{2} s}{1 + \dfrac{8L}{3R_{dc}(1-D)^2} s + \dfrac{8LC}{3(1-D)^2} s^2} \tag{C.10.b}$$

The relationship between variation of the *dc* output voltage and variation of the *d*-axis current can be obtained from (C.10.a) and (C.10.b) as follows.

$$F_{vi}(s) = \frac{\hat{v}_{dc}(s)}{\hat{i}_d(s)} = \frac{3DR_{dc}}{8} \frac{1 - \dfrac{8L}{3R_{dc}D^2} s}{1 + \dfrac{R_{dc}C}{2} s} \tag{C.11}$$

The audio susceptibility function can be obtained after some algebraic manipulations as

$$F(s)=\frac{\hat{v}_{dc}(s)}{\hat{e}_d(s)}=\frac{2}{D}\frac{1}{1+\frac{8L}{3R_{dc}(1-D)^2}s+\frac{8LC}{3(1-D)^2}s^2} \tag{C.12}$$

The output impedance function is defined as:

$$Z_o(s)=\frac{\hat{v}_{dc}(s)}{\hat{i}_z(s)}\bigg|_{\hat{d}=0,\hat{e}_d=0} \tag{C.13}$$

Here, i_z is the output current. In the above derivation (C.10~C.12), the output current was viewed as a function of the *dc* output voltage with a known load resistance, R_{dc}. With the R_{dc} being treated as a known variable, the transfer functions obtained so far (C.10~ C.12) yield more accurate information. However, to obtain the output impedance transfer function, the load resistance can not be treated as being constant. Hence, in this case, the output current is treated as an independent variable and (C.1) becomes

$$\begin{bmatrix}\dot{v}_{dc}\\ \dot{i}_d\end{bmatrix}=\begin{bmatrix}0 & \frac{3}{4C}(1-d)\\ -\frac{(1-d)}{2L} & -\frac{R}{L}\end{bmatrix}\begin{bmatrix}v_{dc}\\ i_d\end{bmatrix}+\begin{bmatrix}0\\ \frac{1}{L}\end{bmatrix}e_d+\begin{bmatrix}-\frac{1}{C}\\ 0\end{bmatrix}i_z \tag{C.14}$$

This can be also written as

$$\dot{x}=A'x+be_d+mi_z \tag{C.15}$$

with $A'=\begin{bmatrix}0 & \frac{3}{4C}(1-d)\\ -\frac{(1-d)}{2L} & -\frac{R}{L}\end{bmatrix}$, $b=\begin{bmatrix}0\\ \frac{1}{L}\end{bmatrix}$ and $m=\begin{bmatrix}-\frac{1}{C}\\ 0\end{bmatrix}$.

Applying the perturbed variables to (C.14), removing the dc terms and neglecting the higher order nonlinear terms, and then taking Laplace Transform, we have

$$(sI - A')\hat{x}(s) = f\hat{d}(s) + b\hat{e}_d(s) + m\hat{i}_z(s) \tag{C.16}$$

After some algebraic manipulations, the output impedance can be found to be given by

$$Z_o(s) = \frac{\hat{v}_{dc}(s)}{\hat{i}_z(s)} = [1 \quad 0](sI - A')^{-1}m = -\frac{8L}{3D^2}\frac{s}{1 + \frac{8LC}{3(1-D)^2}s^2} \tag{C.17}$$

The equations given in (C.10.a) and (C.10.b) are the 'quasi open-loop' transfer functions of the three-phase PWM rectifier. They have been arrived at under the assumption that the de-coupling control given in (3.6) has been implemented and also that the *q*-axis current is being regulated to be zero.

The zero term in (C.10.a) and (C.11) is set to zero to obtain the location of the RHP zero.

$$1 - \frac{8L}{3R_{dc}(1-D)^2}s = 0 \tag{C.18}$$

The RHP zero is located at a frequency given by

$$f_z = \frac{3R_{dc}(1-D)^2}{16\pi L} = \frac{e_d}{2\pi L i_d} = \frac{3e_d^2}{4\pi L p_{dc}}. \tag{C.19}$$

The resonant corner frequency and the damping ratio can be calculated as

$$f_0 = \frac{1-D}{2\pi}\sqrt{\frac{3}{8LC}} \quad \text{and} \quad \varsigma = \frac{1}{2R_{dc}(1-D)}\sqrt{\frac{8L}{3C}}, \tag{C.20}$$

where f_0 is resonant corner frequency with $\omega_0=2\pi f_0$ and ς is damping ratio. Their values can be found by expressing the denominator of (C.10.b) in the standard form for a resonant term, $\omega_0^2+2\varsigma\omega_0 s+s^2$.

C.1 Closed loop transfer functions

When a closed loop compensator is added to the converter, the performance functions, namely, audio susceptibility and output impedance change. Under closed loop operation, the control input for the voltage mode controller is given by

$$d(s)=(v_{dc}^{*}(s)-v_{dc}(s))h_v(s) \tag{C.21}$$

With perturbations introduced in the control input *d*, *dc* output voltage v_{dc} and *dc* output voltage reference v_{dc}^{*}, the small signal expression for the control input of the voltage mode controller can be given as follows.

$$\begin{aligned}\hat{d}(s)&=-h_v(s)\hat{v}_{dc}(s)+h_v(s)\hat{v}_{dc}^{*}(s)=-\begin{bmatrix}h_v(s) & 0\end{bmatrix}\begin{bmatrix}\hat{v}_{dc}(s)\\ \hat{i}_d(s)\end{bmatrix}+\begin{bmatrix}h_v(s) & 0\end{bmatrix}\begin{bmatrix}\hat{v}_{dc}^{*}(s)\\ \hat{i}_d^{*}(s)\end{bmatrix}\\ &=-h(s)\hat{x}(s)+h_v(s)\hat{v}_{dc}^{*}(s)\end{aligned} \tag{C.22}$$

Likewise, under closed loop operation, the control input for the current mode controller is given by

$$d(s)=((v_{dc}^{*}(s)-v_{dc}(s))g_v(s)-i_d(s))g_i(s) \tag{C.23}$$

Again with perturbations introduced in the control input *d*, *dc* output voltage v_{dc} and *dc* output voltage reference, the small signal expression for the control input of the current mode controller can be obtained as given below.

$$\begin{aligned}\hat{d}(s) &= -g_v(s)g_i(s)\hat{v}_{dc}(s) - g_i(s)\hat{i}_d(s) + g_v(s)g_i(s)\hat{v}^*_{dc}(s) \\ &= -\begin{bmatrix} g_v(s)g_i(s) & g_i(s)\end{bmatrix}\begin{bmatrix}\hat{v}_{dc}(s) \\ \hat{i}_d(s)\end{bmatrix} + \begin{bmatrix} g_v(s)g_i(s) & 0\end{bmatrix}\begin{bmatrix}\hat{v}^*_{dc}(s) \\ \hat{i}^*_d(s)\end{bmatrix} + g_v(s)g_i(s)\hat{v}^*_{dc}(s) \\ &= -g(s)\hat{x}(s)\end{aligned} \tag{C.24}$$

Substituting (C.22) and (C.24) into (C.7), the closed loop small signal models with voltage mode and current mode controllers become

$$(sI - A + fh(s))\hat{x}(s) = b\hat{e}_d(s) + fh_v(s)\hat{v}^*_{dc}(s) \tag{C.25.a}$$

$$(sI - A + fg(s))\hat{x}(s) = b\hat{e}_d(s) + fg_v(s)g_i(s)\hat{v}^*_{dc}(s) \tag{C.25.b}$$

The closed loop transfer functions for both voltage and current mode controllers are defined as:

$$\left.\frac{\hat{v}_{dc}(s)}{\hat{v}^*_{dc}(s)}\right|_{\hat{d}=-h(s)\hat{x}(s),\hat{e}_d=0} = [1 \quad 0](sI - A + fh(s))^{-1} fh_v(s) \tag{C.26.a}$$

$$\left.\frac{\hat{v}_{dc}(s)}{\hat{v}^*_{dc}(s)}\right|_{\hat{d}=-g(s)\hat{x}(s),\hat{e}_d=0} = [1 \quad 0](sI - A + fh(s))^{-1} fg_v(s)g_i(s) \tag{C.26.b}$$

The above equations can be rewritten as

$$\begin{aligned}\left.\frac{\hat{v}_{dc}(s)}{\hat{v}^*_{dc}(s)}\right|_{\hat{d}=-h(s)\hat{x}(s),\hat{e}_d=0} &= [1 \quad 0](sI - A + fh(s))^{-1} fh_v(s) \\ &= [1 \quad 0](sI - A)^{-1}(sI - A)(sI - A + fh(s))^{-1} fh_v(s) \\ &= [1 \quad 0](sI - A)^{-1}\frac{(sI - A)}{sI - A + fh(s)} fh_v(s) \\ &= [1 \quad 0](sI - A)^{-1}\frac{fh_v(s)}{1 + [1 \quad 0]fh_v(s)/(sI - A)} \\ &= \frac{[1 \quad 0](sI - A)^{-1} fh_v(s)}{1 + [1 \quad 0](sI - A)^{-1} fh_v(s)} \\ &= \frac{F_v(s)h_v(s)}{1 + F_v(s)h_v(s)} \\ &= \frac{T_v(s)}{1 + T_v(s)}\end{aligned} \tag{C.27.a}$$

$$\left.\frac{\hat{v}_{dc}(s)}{\hat{v}^{*}_{dc}(s)}\right|_{\hat{d}=-g(s)\hat{x}(s),\hat{e}_d=0} = [1 \quad 0](sI-A+fg(s))^{-1} fg_v(s)g_i(s)$$

$$= [1 \quad 0](sI-A)^{-1}(sI-A)(sI-A+fg(s))^{-1} fg_v(s)g_i(s)$$

$$= [1 \quad 0](sI-A)^{-1}\frac{(sI-A)}{sI-A+fg(s)} fg_v(s)g_i(s)$$

$$= [1 \quad 0](sI-A)^{-1}\frac{fg_v(s)g_i(s)}{1+[1 \quad 0]fg_v(s)g_i(s)/(sI-A)+[0 \quad 1]fg_i(s)/(sI-A)} \quad \text{(C.27.b)}$$

$$= \frac{[1 \quad 0](sI-A)^{-1} fg_v(s)g_i(s)}{1+[1 \quad 0](sI-A)^{-1} fg_v(s)g_i(s)+[0 \quad 1](sI-A)^{-1} fg_i(s)}$$

$$= \frac{F_v(s)g_v(s)g_i(s)}{1+F_v(s)g_v(s)g_i(s)+F_i(s)g_i(s)}$$

$$= \frac{F_v(s)g_v(s)g_i(s)}{1+T_i(s)}$$

where $T_v(s)=F_v(s)h_v(s)$ and $T_i(s)=F_v(s)g_v(s)\ g_i(s)$.

The closed loop audio susceptibility functions for both voltage and current mode controllers are defined as:

$$F'(s) = \left.\frac{\hat{v}_{dc}(s)}{\hat{e}_d(s)}\right|_{\hat{d}=-h(s)\hat{x}(s),\hat{x}^{*}(s)=0} = [1 \quad 0](sI-A+fh(s))^{-1}b \quad \text{(C.28.a)}$$

$$F''(s) = \left.\frac{\hat{v}_{dc}(s)}{\hat{e}_d(s)}\right|_{\hat{d}=-g(s)\hat{x},\hat{x}^{*}(s)=0} = [1 \quad 0](sI-A+fg(s))^{-1}b \quad \text{(C.28.b)}$$

The above equations can be rewritten as

$$F'(s) = [1 \quad 0](sI-A+fh(s))^{-1}b = [1 \quad 0](sI-A)^{-1}(sI-A)(sI-A+fh(s))^{-1}b$$

$$= [1 \quad 0](sI-A)^{-1}\frac{(sI-A)}{sI-A+fh(s)}b$$

$$= [1 \quad 0](sI-A)^{-1}\frac{b}{1+[1 \quad 0]fh_v(s)/(sI-A)} \quad \text{(C.29.a)}$$

$$= \frac{[1 \quad 0](sI-A)^{-1}b}{1+[1 \quad 0](sI-A)^{-1} fh_v(s)} = \frac{F(s)}{1+F_v(s)h_v(s)}$$

$$= \frac{F(s)}{1+T_v(s)}$$

$$
\begin{aligned}
F''(s) &= [1 \quad 0](sI - A + fg(s))^{-1} b = [1 \quad 0](sI - A)^{-1}(sI - A)(sI - A + fg(s))^{-1} b \\
&= [1 \quad 0](sI - A)^{-1} \frac{(sI - A)}{sI - A + fg(s)} b = [1 \quad 0](sI - A)^{-1} \frac{b}{1 + fg(s)/(sI - A)} \\
&= \frac{[1 \quad 0](sI - A)^{-1} b}{1 + [0 \quad 1](sI - A)^{-1} f g_i(s) + [1 \quad 0](sI - A)^{-1} f g_v(s) g_i(s)} \\
&= \frac{F(s)}{1 + F_i(s) g_i(s) + F_v(s) g_v(s) g_i(s)} = \frac{F(s)}{1 + T_i(s)}
\end{aligned}
\tag{C.29.b}
$$

Similarly, to obtain the closed loop output impedance functions, substituting (C.22) and (C.24) into (C.16), the closed loop small signal models with voltage mode and current mode controllers become

$$(sI - A' + fh(s))\hat{x}(s) = b\hat{e}_d + m\hat{i}_z - fh(s)\hat{x}^*(s) \tag{C.30.a}$$

$$(sI - A' + fg(s))\hat{x}(s) = b\hat{e}_d + m\hat{i}_z - fg(s)\hat{x}^*(s) \tag{C.30.b}$$

The closed loop output impedance functions for both voltage and current mode controllers are defined as:

$$Z_o'(s) = \frac{\hat{v}_{dc}(s)}{\hat{i}_z(s)}\bigg|_{\hat{d}=-h(s)\hat{x},\hat{e}_d=0,\hat{x}^*(s)=0} = [1 \quad 0](sI - A' + fh(s))^{-1} m \tag{C.31.a}$$

$$Z_o''(s) = \frac{\hat{v}_{dc}(s)}{\hat{i}_z(s)}\bigg|_{\hat{d}=-g(s)\hat{x},\hat{e}_d=0,\hat{x}^*(s)=0} = [1 \quad 0](sI - A' + fg(s))^{-1} m \tag{C.31.b}$$

The above equations can be rewritten as

$$
\begin{aligned}
Z_o'(s) &= [1 \quad 0](sI - A' + fh(s))^{-1} m \\
&= [1 \quad 0](sI - A')^{-1}(sI - A')(sI - A' + fh(s))^{-1} m \\
&= [1 \quad 0](sI - A')^{-1} \frac{(sI - A')}{sI - A' + fh(s)} b \\
&= [1 \quad 0](sI - A')^{-1} \frac{m}{1 + [1 \quad 0] fh_v(s)/(sI - A')} \\
&= \frac{[1 \quad 0](sI - A')^{-1} b}{1 + [1 \quad 0](sI - A')^{-1} fh_v(s)} = \frac{Z_o(s)}{1 + F_v'(s)h_v(s)} \\
&= \frac{Z_o(s)}{1 + T_v'(s)}
\end{aligned}
\tag{C.32.a}
$$

$$
\begin{aligned}
Z_o''(s) &= [1 \quad 0](sI - A' + fg(s))^{-1} m \\
&= [1 \quad 0](sI - A')^{-1}(sI - A')(sI - A' + fg(s))^{-1} m \\
&= [1 \quad 0](sI - A')^{-1} \frac{(sI - A')}{sI - A' + fg(s)} b = [1 \quad 0](sI - A')^{-1} \frac{m}{1 + fg(s)/(sI - A')} \\
&= \frac{[1 \quad 0](sI - A')^{-1} m}{1 + [0 \quad 1](sI - A')^{-1} fg_i(s) + [1 \quad 0](sI - A')^{-1} fg_v(s) g_i(s)} \\
&= \frac{Z_o(s)}{1 + F_i'(s)g_i(s) + F_v'(s)g_v(s)g_i(s)} \\
&= \frac{Z_o(s)}{1 + T_i'(s)}
\end{aligned}
\tag{C.32.b}
$$

The main closed-loop transfer functions have been summarized in Table 3.4 of Chapter 3.

Appendix D
Measurement of Bode Plots in a dSPACE Controlled PWM Rectifier System

D.0 Introduction

As the *d*-axis equivalent circuit of a PWM rectifier does not independently exist in the experimental set-up, pre-controllers should be implemented to operate the three-phase PWM rectifier in a "quasi open-loop" mode as explained in Chapter 3.2.3. Once the equivalent *d*-axis SISO circuit is established, the variable *d* (u_{d2}) can be treated as the control input of the SISO system and either *dc* output voltage or *d*-axis current be treated as the outputs of the SISO system. In this appendix, the method of performing the gain phase measurement for the *d*-axis equivalent circuit of the PWM rectifier with a dSPACE controlled system that was adopted will be explained.

D.1 Measurement of open-loop bode plots

Fig. 3.5 illustrates the equivalent *d*-axis SISO system of a PWM rectifier that was realized. Fig. D.1 shows the diagram for the measurement of open loop Bode plots of the equivalent SISO system. To measure the open loop control-to-output Bode plots, a perturbation signal is introduced from a HP4194A gain-phase analyzer into the control input through an ADC (Analog to Digital Converter) unit of the dSPACE. With the added perturbation signal in the control signal, the perturbed *dc* output voltage $\hat{v}_{dc}$ and the perturbed *d*-axis current $\hat{i}_d$ can be obtained. The Bode plots of the control gains can be measured by using the perturbation signal from the HP4194A equipment

as the injected signal into the open-loop system and feeding it to the reference channel and by feeding the *dc* output voltage or the *d*-axis current to the test channel of the HP4194A equipment.

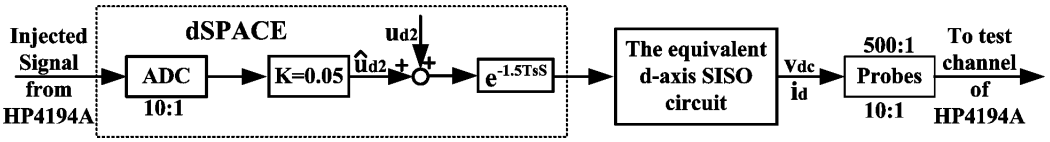

Fig. D.1 Diagram for measurement of open loop Bode plots of the equivalent SISO system

As shown in Fig. D.1, the perturbation signal is obtained from the ADC unit with a further attenuation in the dSPACE processor. By attenuating the injected signal in the dSPACE processor, the amplitude of the injected signal can be adjusted large enough to reduce the sampling error of the ADC unit. As the dSPACE contains an $1.5T_s$ (i.e., 1.5 x sampling period) time delay as detailed in the Appendix G, an extra phase lag will be introduced in the phase Bode plot as follows:

$$\theta = 1.5T_s \cdot 2\pi f \,, \tag{D.1}$$

where θ is the phase lag with the units of radians, T_s is sampling period with T_s=*0.0001* s and f is frequency.

The output signals of the system will be connected to the test channel of HP4914A through a current probe (for *d*-axis current) or differential probe (for output voltage). This allows the Bode Plots of the control gains to be obtained from the HP 4194A equipment. The raw Bode plots obtained from the HP4194A equipment should be reconstructed by applying both amplitude and phase compensations as explained in the previous paragraph. Taking the control-to-*dc* output voltage Bode plots as an

example, the measured control gain can be expressed as given below.

$$F_v'(s) = \frac{\hat{v}_{dc}/500}{200\hat{u}_{d2}} = F_v(s)/10000 \tag{D.2}$$

Thus, to reconstruct the Bode plots, the magnitude should be compensated according to (D.2). In addition to magnitude compensation, the phase should be also compensated based on (D.1). Thus, the control-to-dc output voltage Bode plots shown in Fig. 3.7 and the control-to-d axis current shown in Fig. 3.8 were obtained after applying the compensations as indicated in this section.

D.2 Measurement of loop transfer function Bode plots

The loop transfer function can be expressed as

$$T(s) = G(s)C(s), \tag{D.3}$$

where $G(s)$ denotes the system transfer function, such as $F_v(s)$ or $F_{vi}(s)$ and $C(s)$ denotes the corresponding controller transfer function.

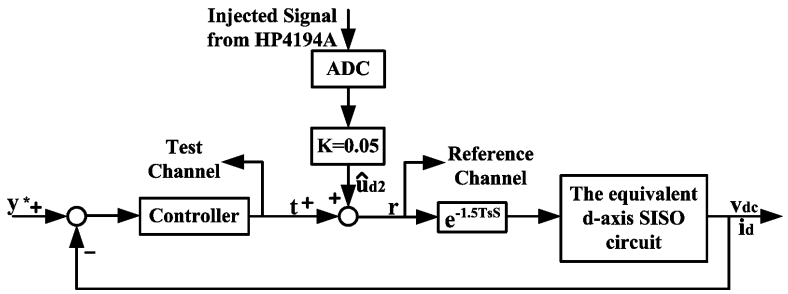

Fig. D.2 Diagram for the measurement of closed loop Bode plots of the equivalent SISO system

To measure loop transfer function Bode plots, the closed loop system including the measurement set-up was built as shown in Fig. D.2. The loop transfer function of the can then be obtained as follows.

$$T'(s) = \frac{\hat{r}}{\hat{t}} = -G(s)C(s)e^{-1.5T_s s} \tag{D.4}$$

To obtain the loop transfer function Bode plots from the measured Bode plots, magnitude compensation and phase compensation should be done as indicated earlier in Section D.1.

Appendix E
Power Definition in a Three-Phase Sinusoidal Unbalanced System

In this appendix, the definitions of power in *a-b-c* natural frame, *α-β* stationary frame and *d-q* synchronously rotating frame are presented. The instantaneous reactive power definition derived with vector calculation and the conventional reactive power definition derived with phasor calculation have been given and discussed. These power definitions have been used in Chapter 6 for power factor calculation.

E.1 Power definitions in *a-b-c* frame [5-7]

In an unbalanced system, the three currents, i_a, i_b and i_c, do not have equal magnitudes, nor, in general, are they shifted exactly with respect to each other.

The line-to-neutral voltages are as follows:

$$\begin{cases} v_a = \sqrt{2}V_{a\ln}\cos(\omega t + \alpha_a) \\ v_b = \sqrt{2}V_{b\ln}\cos(\omega t + \alpha_b - 120^o) \\ v_c = \sqrt{2}V_{c\ln}\cos(\omega t + \alpha_c + 120^o) \end{cases} \quad \text{(E.1)}$$

The line currents have similar expressions. They are as follows;

$$\begin{cases} i_a = \sqrt{2}I_{a\ln}\cos(\omega t + \beta_a) \\ i_b = \sqrt{2}I_{b\ln}\cos(\omega t + \beta_b - 120^o) \\ i_c = \sqrt{2}I_{c\ln}\cos(\omega t + \beta_c + 120^o) \end{cases} \quad \text{(E.2)}$$

Definition 1: Instantaneous power

$$p = v_a i_a + v_b i_b + v_c i_c \quad \text{(E.3)}$$

Definition 2: Active power (W)

$$P = \frac{1}{kT}\int_{\tau}^{\tau+kT} p dt \tag{E.4}$$

$P=P_a+ P_b+ P_c$

Here

$$P_a = \frac{1}{kT}\int_{\tau}^{\tau+kT} v_a i_a dt = V_{a\ln} I_a \cos\theta_a ;\ \theta_a = \alpha_a - \beta_a \tag{E.5}$$

$$P_b = \frac{1}{kT}\int_{\tau}^{\tau+kT} v_b i_b dt = V_{b\ln} I_b \cos\theta_b ;\ \theta_b = \alpha_b - \beta_b \tag{E.6}$$

$$P_c = \frac{1}{kT}\int_{\tau}^{\tau+kT} v_c i_c dt = V_{c\ln} I_c \cos\theta_c ;\ \theta_c = \alpha_c - \beta_c \tag{E.7}$$

P_a, P_b and P_c are phase active powers.

Definition 3: Reactive power (var)

The total reactive power Q is as follows:

$$Q=Q_a+ Q_b+ Q_c \tag{E.8}$$

With per phase reactive powers defined with the help of the following expressions:

$$Q_a = \frac{1}{kT}\int_{\tau}^{\tau+kT} i_a[\int v_a dt]dt = V_{a\ln} I_a \sin\theta_a ;\quad \theta_a = \alpha_a - \beta_a \tag{E.9}$$

$$Q_b = \frac{1}{kT}\int_{\tau}^{\tau+kT} i_b[\int v_b dt]dt = V_{b\ln} I_b \sin\theta_b ;\quad \theta_b = \alpha_b - \beta_b \tag{E.10}$$

$$Q_c = \frac{1}{kT}\int_{\tau}^{\tau+kT} i_c[\int v_c dt]dt = V_{c\ln} I_c \sin\theta_c ;\quad \theta_c = \alpha_c - \beta_c \tag{E.11}$$

E.2 Power definition in stationary frame

With the Clark transformation, $\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix}$, the variables

in a-b-c frame can be transformed into stationary frame.

E.2.1 Power definitions

Definition 1: Instantaneous active and reactive power

$$p = v_a i_a + v_b i_b + v_c i_c = \frac{3}{2}(v_\alpha i_\alpha + v_\beta i_\beta) \tag{E.12}$$

$$q = \frac{1}{\sqrt{3}}[(v_b - v_c)i_a + (v_c - v_a)i_b + (v_a - v_b)i_c] = \frac{3}{2}(v_\beta i_\alpha - v_\alpha i_\beta) \tag{E.13}$$

Definition 2: Average active power (W)

$$P = \frac{1}{kT}\int_{\tau}^{\tau+kT} p\,dt \tag{E.14}$$

Definition 3: Average reactive power (var)

$$Q = \frac{1}{kT}\int_{\tau}^{\tau+kT} q\,dt \tag{E.15}$$

E.2.2 Space vector expression of three-phase variables in stationary frame

As mentioned in Appendix B, the unbalanced three-phase variables can be represented as the orthogonal sum of positive and negative sequence components as (B.1) and be reproduced as follows.

$$\begin{cases} v_a = v_a^p + v_a^n = v^p \cos(\omega t + \theta_v^p) + v^n \cos(\omega t + \theta_v^n) \\ v_b = v_b^p + v_b^n = v^p \cos(\omega t + \theta_v^p - 120^o) + v^n \cos(\omega t + \theta_v^n + 120^o) \\ v_c = v_c^p + v_c^n = v^p \cos(\omega t + \theta_v^p + 120^o) + v^n \cos(\omega t + \theta_v^n - 120^o) \end{cases} \tag{E.16}$$

$$\begin{cases} i_a = i_a^p + i_a^n = i^p \cos(\omega t + \theta_i^p) + i^n \cos(\omega t + \theta_i^n) \\ i_b = i_b^p + i_b^n = i^p \cos(\omega t + \theta_i^p - 120^o) + i^n \cos(\omega t + \theta_i^n + 120^o) \\ i_c = i_c^p + i_c^n = i^p \cos(\omega t + \theta_i^p + 120^o) + i^n \cos(\omega t + \theta_i^n - 120^o) \end{cases} \tag{E.17}$$

Applying Clark transformation to (E.16), we have

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} v^p \cos(\omega t + \theta_v^p) + v^n \cos(\omega t + \theta_v^n) \\ v^p \sin(\omega t + \theta_v^p) - v^n \sin(\omega t + \theta_v^n) \end{bmatrix} \tag{E.18}$$

Forming the space vector with $v = v_\alpha + jv_\beta$, we have

$$v = v^p \cos(\omega t + \theta_v^p) + jv^p \sin(\omega t + \theta_v^p) + v^n \cos(\omega t + \theta_v^n) - jv^n \sin(\omega t + \theta_v^n)$$

$$= v^p e^{j(\omega t + \theta_v^p)} + v^n e^{-j(\omega t + \theta_v^n)} \tag{E.19}$$

Likewise, applying Clark transformation to (E.17) and forming the space vector with $i = i_\alpha + ji_\beta$, we have

$$i = i^p e^{j(\omega t + \theta_i^p)} + i^n e^{-j(\omega t + \theta_i^n)} \tag{E.20}$$

E.2.3 Power definition expressions in space vector formulation

The apparent power *S* is defined as

$$S = v \cdot i^* = \frac{3}{2}(v_\alpha i_\alpha + v_\beta i_\beta) + j\frac{3}{2}(v_\beta i_\alpha - v_\alpha i_\beta) \tag{E.21}$$

Substituting (E.19) and (E.20) into (E.21), we have

$$S = \frac{3}{2}(v^p e^{j(\omega t + \theta_v^p)} + v^n e^{-j(\omega t + \theta_v^n)})(i^p e^{j(\omega t + \theta_i^p)} + i^n e^{-j(\omega t + \theta_i^n)})^*$$

$$= \frac{3}{2}[v^p i^p e^{j(\theta_v^p - \theta_i^p)} + v^n i^n e^{-j(\theta_v^n - \theta_i^n)} + v^p i^n e^{j(2\omega t + \theta_v^p + \theta_i^n)} + v^n i^p e^{-j(2\omega t + \theta_v^n + \theta_i^p)}] \tag{E.22}$$

The average active power is

$$p = \frac{3}{2}v^p i^p \cos(\theta_v^p - \theta_i^p) + \frac{3}{2}v^n i^n \cos(\theta_v^n - \theta_i^n) \tag{E.23}$$

The average instantaneous reactive power is defined as

$$q = \frac{3}{2}v^p i^p \sin(\theta_v^p - \theta_i^p) - \frac{3}{2}v^n i^n \sin(\theta_v^n - \theta_i^n) = q^+ - q^- \tag{E.24}$$

with $q^+ = \frac{3}{2} v^p i^p \sin(\theta_v^p - \theta_i^p)$ and $q^- = \frac{3}{2} v^n i^n \sin(\theta_v^n - \theta_i^n)$.

E.3 Power definition expressions in synchronously rotating frame

The symmetrical components analysis for the three-phase variables in an unbalanced system was done in the Appendix B. The power can be expressed in the phasor form as given below.

$$s = \frac{1}{2}(\tilde{v}_a \tilde{i}_a^* + \tilde{v}_b \tilde{i}_b^* + \tilde{v}_c \tilde{i}_c^*)$$

$$= \frac{1}{2}[(\tilde{v}^p + \tilde{v}^n)(\tilde{i}^p + \tilde{i}^n)^* + (\alpha^2 \tilde{v}^p + \alpha \tilde{v}^n)(\alpha^2 \tilde{i}^p + \alpha \tilde{i}^n)^* + (\alpha \tilde{v}^p + \alpha^2 \tilde{v}^n)(\alpha \tilde{i}^p + \alpha^2 \tilde{i}^n)^*]$$

$$= \frac{3}{2}\tilde{v}^p(\tilde{i}^p)^* + \frac{3}{2}\tilde{v}^n(\tilde{i}^n)^* + \frac{1}{2}(1+\alpha+\alpha^2)\tilde{v}^p(\tilde{i}^n)^* + \frac{1}{2}(1+\alpha^2+\alpha)\tilde{v}^n(\tilde{i}^p)^*$$

$$= \frac{3}{2}\tilde{v}^p(\tilde{i}^p)^* + \frac{3}{2}\tilde{v}^n(\tilde{i}^n)^* \qquad \text{(E.25)}$$

Here, $\tilde{v}_a$, $\tilde{v}_b$, $\tilde{v}_c$ and $\tilde{i}_a$, $\tilde{i}_b$, $\tilde{i}_c$ corresponds to the phasors of three-phase voltages (v_a, v_b, v_c) and three-phase currents (i_a, i_b, i_c) with $\tilde{v}_a = V_a \angle \alpha_a$, $\tilde{v}_b = V_b \angle \alpha_b$, $\tilde{v}_c = V_c \angle \alpha_c$ and $\tilde{i}_a = I_a \angle \beta_a$, $\tilde{i}_b = I_b \angle \beta_b$, $\tilde{i}_c = I_c \angle \beta_c$. Variables V_a, V_b, V_c and variables I_a, I_b, I_c are the peak amplitudes of the three-phase voltages and currents and α_a, α_b, α_c and β_a, β_b, β_c are the angles of three-phase voltages and currents. Here, $\tilde{v}^p = v^p \angle \theta_v^p$, $\tilde{v}^n = v^n \angle \theta_v^n$ and $\tilde{i}^p = i^p \angle \theta_i^p$, $\tilde{i}^n = i^n \angle \theta_i^n$.

Therefore, the average active power is

$$p = \frac{3}{2} v^p i^p \cos(\theta_v^p - \theta_i^p) + \frac{3}{2} v^n i^n \cos(\theta_v^n - \theta_i^n) \qquad \text{(E.26)}$$

Conventional reactive power is defined as

$$q = \frac{3}{2} v^p i^p \sin(\theta_v^p - \theta_i^p) + \frac{3}{2} v^n i^n \sin(\theta_v^n - \theta_i^n) = q^+ + q^- \quad \text{(E.27)}$$

with $q^+ = \frac{3}{2} v^p i^p \sin(\theta_v^p - \theta_i^p)$ and $q^- = \frac{3}{2} v^n i^n \sin(\theta_v^n - \theta_i^n)$.

E.4 Discussion on Different Reactive Power Definitions in SRF

It is worth noting that the average reactive power definitions in (E.24) and (E.27) are different. The reason can be illustrated with the help of Fig. E.1.

The current and voltage expressions in the a-b-c natural frame with both positive and negative sequence components are given in (E.16) and (E.17). However, when currents and voltages are expressed as vectors with Clark transformation, the angle of the negative sequence component takes a positive direction as shown in the vector diagram given in Fig. E.1.a. This is different from the positive direction taken in the conventional reactive power definition which is shown in the phasor diagram given in Fig. E.1.b.

Thus differences exist in the orientation of the positive angle direction of the negative sequence component in the two cases. This results from the different negative sequence reactive power definitions adopted in the cases of the instantaneous reactive power definition approach (E.24) and the conventional reactive power definition approach (E.27). Thus, the differences do not really exist but are merely due to the different conventions adopted.

In the thesis, instantaneous reactive power definition has been adopted.

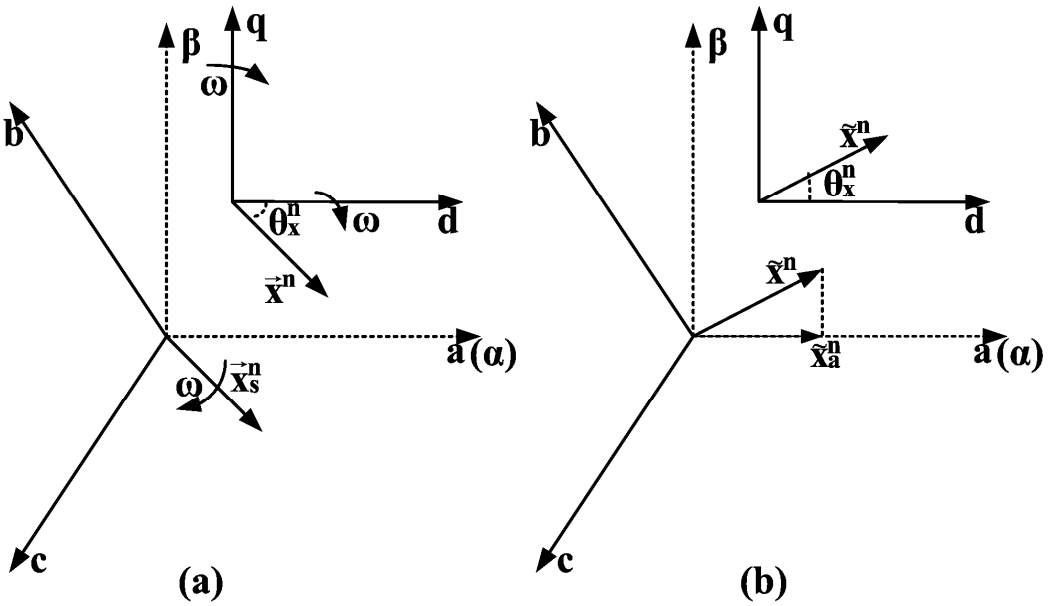

Fig. E.1 a) Vector diagram of a negative sequence component at t=0 in the instantaneous reactive power definition b) Vector diagram of a negative sequence component at t=0 in the conventional reactive power definition

Appendix F
Uncertainty and Stability Robustness

In this appendix, some basic concept of uncentainty and stablility robustness will be introduced [100]. This theory will be used in Charter 5 to evulate the stability robustness of the systems given in Fig. 5.3 and Fig. 5.6

F.1 Representation of uncertainty

The purpose in this analysis is to make explicit model of system uncertainties. Here, two kinds of uncertainties will be introduced. They are 'unstructured uncertainty' and 'structured uncertainty'.

Let $G_0(s)$ be a nominal transfer matrix, which is a best estimate, in some sense, of the true plant behavior. Let $G(s)$ denote the true transfer function matrix of the plant. The following are the three most commonly used unstructured uncertainty models:

Additive perturbation: $G(s) = G_0(s) + \Delta_a(s)$ (F.1)

Input multiplicative perturbation: $G(s) = G_0(s)(1 + \Delta_i(s))$ (F.2)

Output multiplicative perturbation: $G(s) = (1 + \Delta_o(s))G_0(s)$ (F.3)

The only restriction on the perturbation is on their 'size', which is measured by $\|\Delta\|_\infty$. Here, $\|\cdot\|_\infty$ is defined by $\|\cdot\|_\infty = \max_i |\Delta_i|$. If we want to make the size frequency-dependent we can set $\Delta = W_1\tilde{\Delta}W_2$, where *W1* and *W2* are minimum-phase transfer functions which serve as frequency-dependent wighting functions. In this case,

$\left\|\tilde{\Delta}\right\|_{\infty} \le 1$ is taken as being valid.

In practice both structured and unstructured information may be available about plant uncertainty.

The use of the unstructured description generally leads to conservative design because the system must perform satisfactorily for those perturbations which can never occur [100].

Structured uncertainty refers to the condition where the information about the structure of the input uncertainty is available. For example, the uncertainty has a block-diagonal structure, such as $\Delta = diag\{\Delta_{1,} \quad \Delta_{2,} \quad \cdots, \quad \Delta_{n}\}$.

In our work, a structured uncertainty has been used.

F.2 Description of the plant uncertainty

Let a plant have three sets of inputs and outputs.

1st set of inputs: all manipulated variables.

2nd set of inputs: all other external signals (disturbances/set points).

1st set of outputs: all measured variables for feedback.

2nd set of outputs: all other outputs whose behaviors are of interest.

The third set of inputs and outputs is novel and comes from uncertainty. We take each of the uncertainties in the plant outside the plant and assign it with one block. We collect all such blocks together as a special system. This special system is around

the plant and has a block-diagonal structure, with those blocks which have been pulled out from inside the plant being on the diagonal.

$$\Delta(s) = diag\{\Delta_1(s), \quad \Delta_2(s), \quad \cdots, \quad \Delta_n(s)\} \tag{F.4}$$

Here, Δ_i may be a scalar or a matrix. This can be illustrated as shown in Fig. F.1.

If the compensator is already known, we can form a single system representing the closed loop system consisting of *P* and *K*. Fig. F.2 shows a standard system for which we can formulate now robust stability condition.

The system shown in Fig. F.2 can be written in the matrix form:

$$\begin{bmatrix} y \\ x \end{bmatrix} = Q \begin{bmatrix} v \\ z \end{bmatrix} = \begin{bmatrix} Q_{11} & Q_{12} \\ Q_{21} & Q_{22} \end{bmatrix} \begin{bmatrix} v \\ z \end{bmatrix} \tag{F.5}$$

Here, *x* is input vector to uncertainty and *z* is output vector of uncertainty. Vector *v* is all manipulated variables and vector *y* is output whose behaviors are of interest.

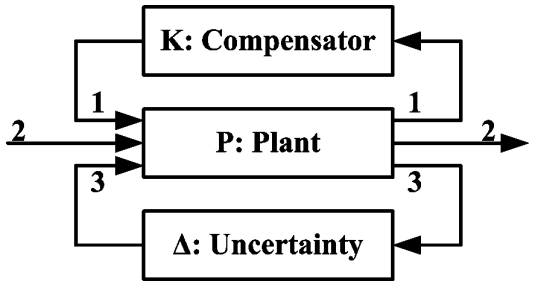

Fig. F.1 Standard representation of uncertainty

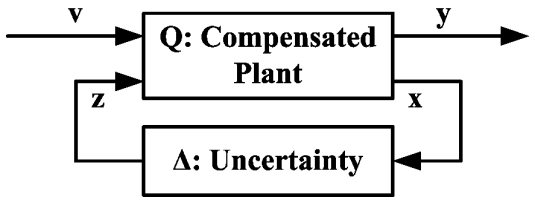

Fig. F.2 Standard representation for robust stability condition formulation

F.3 Robust stability for the SISO case

The property that the system remains stable in face of uncertainty is called the robust stability. The closed-loop system is said to be robustly stable if it remains stable for all Δ satisfying $|\Delta| < r$.

The robust stability condition for the compensated system given in Fig. F.2 is

$$\begin{cases} \left\|\tilde{Q}_{22}\right\|_\infty < 1 & if \left\|\tilde{\Delta}\right\|_\infty \le 1 \\ \left\|\tilde{Q}_{22}\right\|_\infty \le 1 & if \left\|\tilde{\Delta}\right\|_\infty < 1 \end{cases} \tag{F.6}$$

Here, Q_{22} can be obtained by removing the first set of inputs v and outputs y shown in Fig. F.2 with $Q_{22}=x/z$.

F.4 M-Files for singular value calculation for system shown in Fig. 5.3

The following code is used to calculated singular value of the resultant plant $P = [L \cdot G + I] \cdot [C \cdot G + I]^{-1} C$ shown in Fig. 5.3.

```
S = tf ('s');
f = 800*pi; Ls = 4.15e-3; Rs = 0.27; Kp = f*Ls; Ki = f*Rs;
L = [0 2*pi*50*Ls; -2*pi*50*Ls 0];
G = [1/(Ls*s+Rs) 0; 0 1/(Ls*s+Rs)];
C = [Kp+Ki/s 0; 0 Kp+Ki/s];
I = [1 0;0 1];
P = (L*G+I)*inv(C*G+I)*C;
P = ss(q);
A = P.a
B = P.b
C = P.c
D = P.d
G = pck(A,B,C)
omega = logspace(-2,5,200);
M_g = frsp(G,omega);
```

```
Deltaset = [2 0; 2 0];
[mubnds,rowd,sens,rowp,rowg] = mu(M_g, deltaset, 'c');
vplot ('liv, m', mubnds, 'b-');
muRP = sel(mubnds,':',1);
[pkvnorm(muRP)  1/pkvnorm(muRP)]
```

F.5 M-Files for singular value calculation for system shown in Fig. 5.6

The following code is used to calculated singular value of the compensated plant $P' = T' \cdot L$ given in Fig. 5.6.

```
s = tf('s');
f = 800*pi; L = 4.15e-3;R = 0.27; Kp = f*L; Ki = f*R;
W = [0.1 0; 0 0.1;];
K = [0 2*pi*50*L; -2*pi*50*L 0];
G = [1/(L*s+R) 0; 0 1/(L*s+R)];
C = [Kp+Ki/s 0; 0 Kp+Ki/s];
I = [1 0;0 1];
q = C*G*inv(C*G+I)*K*W;
P = ss(q);
A = P.a
B = P.b
C = P.c
D = P.d
G = pck(A,B,C)
omega = logspace(-2,5,200);
M_g = frsp(G,omega);
deltaset = [2 0;2 0];
[mubnds,rowd,sens,rowp,rowg] = mu(M_g,deltaset,'c');
vplot ('liv,m',mubnds,'b-');
muRP = sel(mubnds,':',1);
[pkvnorm(muRP)  1/pkvnorm(muRP)]
```

Appendix G
Time Delay in a dSPACE System

In a dSPACE controlled system, the three-phase PWM signal is generated by a slave DSP processor. Thus, it is necessary to synchronize PowerPC 603e microprocessor with the DSP subsystem by using a PWM generation interrupt from the Slave DSP.

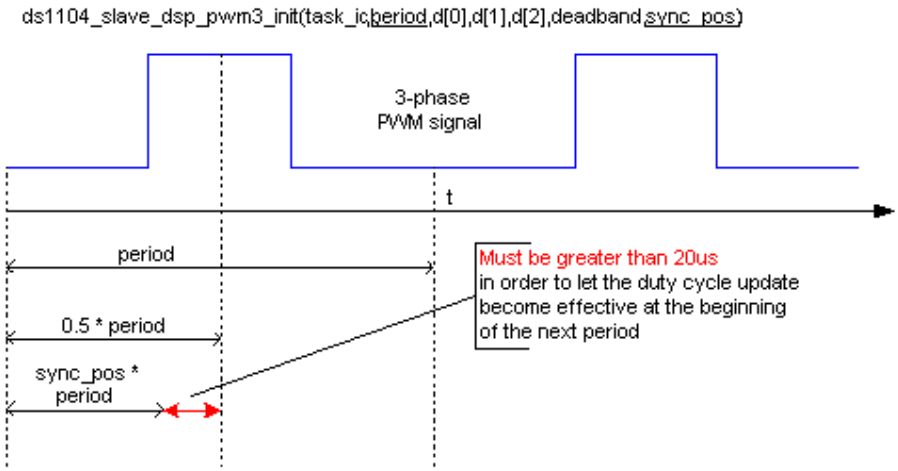

Fig. G.1 Diagram for the synchronization interrupt signal

Assuming that the PWM3 generation is performed, an interrupt can be generated by the slave DSP nearly at any time over the whole period. The position (interrupt alignment) of the generated interrupt must be within the range (0~1). This position is determined by the value of sync_pos parameter. The PWM generation interrupt can be used to sample and update the PWM signal.

If the PWM generation interrupt is used to update the PWM signal, the new duty cycle value must be transmitted from the Master PPC to the Slave DSP more than 20us before the center of the PWM period as shown in Fig. G.1. Under this condition,

the new duty cycle becomes effective at the beginning of the next period. If the new duty cycle value is transmitted to the slave DSP later, the change becomes effective at the beginning of the next second PWM period.

In our experiment, the sync_pos period was set to be 0.5 due to processing and calculation time. It was found in the experiment that the system contains a time delay of 1.5 times the sampling instant (switching period) from sampling action to the updating of the PWM signal as shown in Fig. G.2.

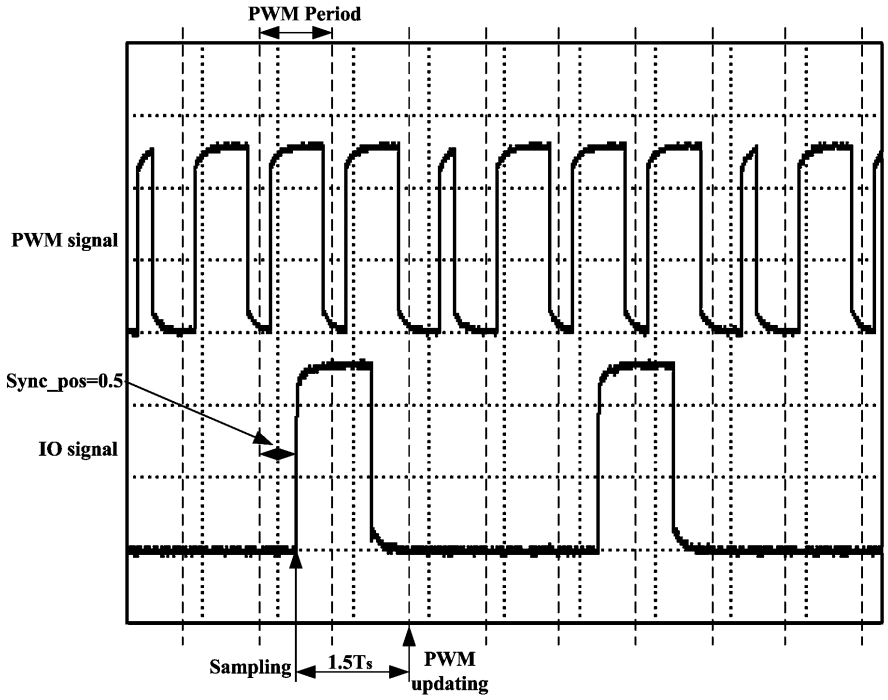

Fig. G.2 Experimental waveforms for a-phase PWM signal and IO signal

In this experiment, the IO unit was set to unity and a-phase duty ratio was updated from 0.7 to 0.2 at the same interrupt action. However, as shown in Fig. G.2, there was 1.5Ts time delay between IO signal updating and PWM signal updating.

The presence of time delay can be attributed to the communication and interruption cooperation modes between slave DSP and main processor. This time delay must be taken into account in evaluating the results obtained with the set-up as was the case in Appendix D.

Appendix H
Architecture of dSPACE DS1104

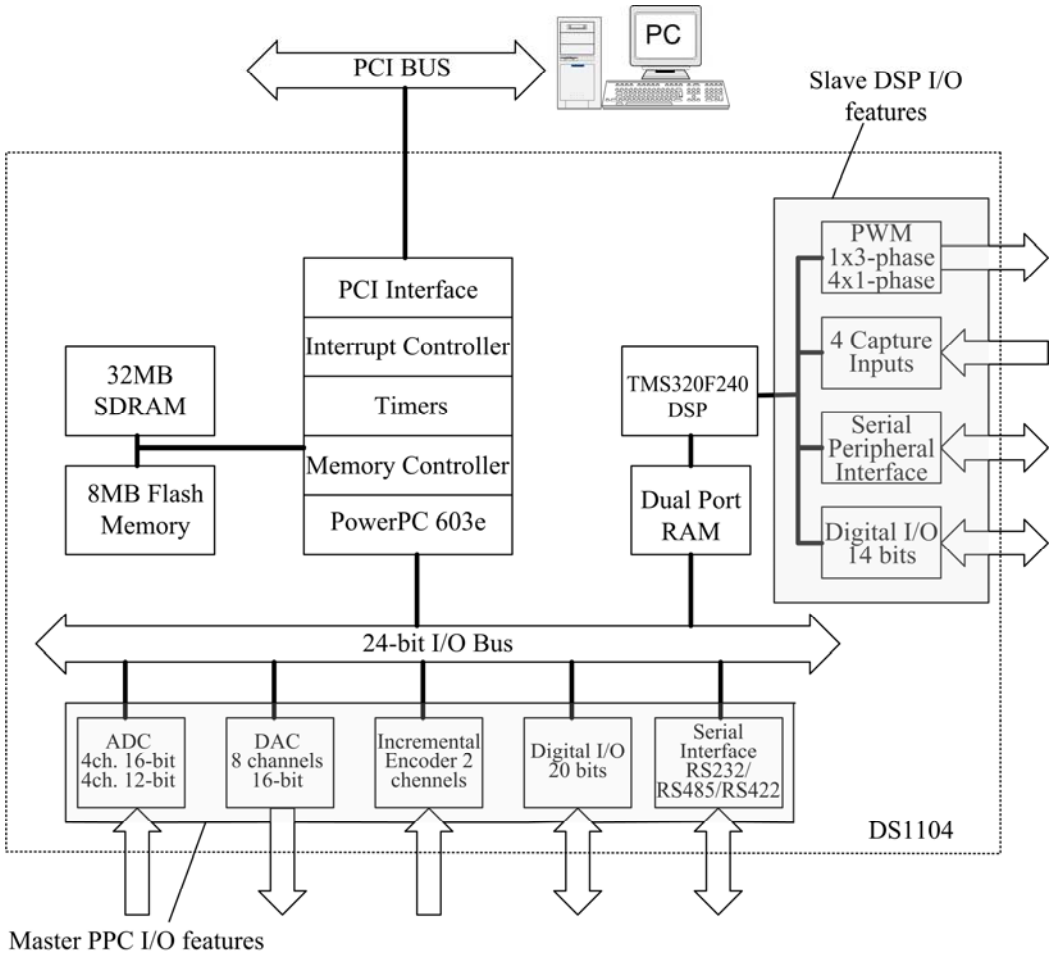

Fig.H.1 Architecture of the DSP DS1104 controller board

Fig.H.1 gives an overview of the architecture and the functional units of the DS1104. The DS1104 controller board provides the following features:

- Master Processor: PowerPC 603e microprocessor at 250MHz,16Kbyte L1 data cache, 16Kbyte L1 instruction cache;
- Slave DSP subsystem: a Texas Instruments TMS320F240 DSP at 20MHz

- 1 16bit A-D converter multiplexed to four channel, 4 parallel 12bit A-D converters
- 8 parallel 16bit D-A channels
- 20bit digital I/O
- 4 64bit timer