DEFECT ENGINEERING IN THE FORMATION OF ULTRA-SHALLOW JUNCTIONS FOR ADVANCED NANO-METAL-OXIDE-SEMICONDUCTOR TECHNOLOGY

YEONG SAI HOOI

NATIONAL UNIVERSITY OF SINGAPORE

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“Research serves to make building stones out of stumbling blocks.”

Arthur Dehon Little
(1863-1935)

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Abstract

The formation of ultra-shallow junctions (USJs) in silicon is demanded by progressive miniaturization of CMOS (Complimentary Metal-Oxide-Semiconductor) devices. The main objective of this work is to achieve highly doped and electrical activated USJs through defect engineering. Defects generated during processing can interact with doping ions causing anomalous phenomena such as transient enhanced diffusion (TED) and dopant-defect clustering, which are detrimental to the desired USJ properties. The primary study here is concerned with the investigation of co-implantation of C/F/N (Carbon/Fluorine/Nitrogen), advanced flash annealing scheme as well as surface state in effectively controlling dopant diffusion and defect distribution in the pre-amorphized B doped silicon substrate so as to exert control over the amount of dopants as well as their activity. We seek to achieve better physical understanding of the interactions between dopants and defects associated with the advanced USJ techniques, providing some insights for the optimization of USJs in the CMOS devices.

Summary

Formation of ultra-shallow junctions (USJs) poses one of the extremely difficult challenges in the CMOS (Complimentary Metal-Oxide-Semiconductor) device downscaling era. This can be attributed to the fact that, in addition to the shallower junction depth that is required to rival the short channel effect (SCE), high dopant activation and defect-free junctions are necessary to improve the transistor performance.

In this dissertation, a few advanced USJ formation techniques are investigated on the B (Boron) doped USJs associated with Ge pre-amorphizing implant (Ge-PAI). The primary aim is to fabricate USJs for the application in nano-CMOS devices through the understanding and maneuvering of dopant-defect interactions, known as defect engineering.

The first USJ technique being studied is the N co-implant on Ge-PAI B junctions. It is deduced that N atoms react with vacancy point defects and B atoms, to form NV (Nitrogen – Vacancy) clusters and B-N (Boron – Nitrogen) complexes during the solid-phase-epitaxy-regrowth (SPER) process. The effect of N co-implant on B can be optimized by carefully locating the N distributions. The optimized N co-implanted B USJs show superior R_s/X_j junction properties over the standard spike annealed junctions. Application in PMOS devices also reveals great reduction in SCE attributed to the suppression of B TED by the co-implanted N atoms.

The extensive study of C/F co-implant in Ge-PAI B/BF_2 junctions clearly indicates that C co-implant is more efficient than F co-implant towards the trapping of excess interstitials during SPER. Hence, the former has better inhibition of B TED

and dopant de-activation effect. The efficiency of the two co-implants is attributed to their different interstitial trapping pathways and amount of co-implanted atoms retained after annealing. The F doping in junctions either by F co-implant or F co-doing via BF_2 degrades the B activation though B-F paring. A direct comparison among the C, F and N co-implants reveals that the various co-implant species has their respective distinct advantages on the junction physical and electrical properties.

Flash lamp annealing (FLA) has been shown to be a great potential candidature for future dopant activation technique. However, residual end-of-range (EOR) defects upon FLA causing high junction leakage in devices. It is demonstrated that the EOR defects can be reduced by applying multiple-pulse FLA and pre-spike rapid thermal annealing (RTA) + FLA schemes. From the diode fabrication, it is found that the high junction leakage for the direct single pulse FLA can be significantly reduced by increasing the flash pulses or inserting pre-spike RTA prior to FLA. The underlying physical mechanisms have been studied and investigated by experiment and simulation.

As the devices is continue to shrink, the dopants are getting closer to the silicon surface. It is found that the surface chemical state has significant impact on B diffusion/activation and EOR defects in the junctions. This is attributed to the fact that dangling bonds at atomically clean surface open an alternative pathway for enhanced annihilation of excess interstitials compared to the conventional native oxide surface during the annealing. It reduces the concentration of excess silicon interstitials available in the junctions, thus minimizing the interactions between the B

and point defects. This eventually benefits the B TED and dopant deactivation towards the Ge-PAI B USJ formation.

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List of Abbreviations

4ppt	Four-Point-Probe
A/C	Amorphous/Crystalline
AFM	Atomic Force Microscopy
As	Arsenic
B	Boron
BIC/BICs	Boron Interstitial Cluster/s
B-N	Boron-Nitrogen
C	Carbon
CMOS	Complimentary Metal-Oxide-Semiconductor
C_{ov}	Overlap Capacitance
CVD	Chemical Vapour Deposition
EOR	End-of-range
F	Fluorine
FET	Field Effect Transistor
FLA	Flash Lamp Annealing
FV	Fluorine-Vacancy
Ge	Germanium
I	Interstitial
IC	Integrated Circuit
In	Indium
ITRS	International Technology Roadmap for Semiconductors
I-V	Current –Voltage
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
N	Nitrogen
NMOS	N-type Metal-Oxide-Semiconductor
N_s	Active Carrier Concentration
NV	Nitrogen-Vacancy
P	Phosphorus

PAI	Pre-Amorphizing Implant
PLAD	Plasma Doping
PMOS	P-type Metal-Oxide-Semiconductor
RHs	Hall Coefficient
R_s	Sheet Resistance
RSF	Relative Sensitivity Factor
RTA	Rapid Thermal Annealing
S/D	Source/Drain
Sb	Antimony
SCE	Short Channel Effect
Si	Silicon
SIMS	Secondary Ion Mass Spectroscopy
SOI	Silicon On Insulator
SPER	Solid-Phase-Epitaxy-Regrowth
SSI	Small Scale Integration
TCAD	Technology Computer Aided Design
TED	Transient Enhanced Diffusion
TEM	Transmission Electron Microscopy
ULSI	Ultra-Large Scale Integration
USJ/USJs	Ultra-Shallow Junction/s
V	Vacancy
VDP	Van der Pauw
V_H	Hall Voltage
VLSI	Very-Large Scale Integration
X_j	Junction Depth
XTEM	Cross-sectional Transmission Electron Microscopy

Chapter 1

Introduction

Since William Shockley, John Bardeen and Walter Brattain from Bell laboratories unveiled the first point contact transistor in 1948, a revolution change in microelectronics industry has witnessed the end of "vacuum tube" century [Bardeen et al., 1948]. The semiconductor industry has further developed at an astonishing pace after the invention of monolithic Integrated Circuit (IC) by Jack Kilby and Robert Noyce two years later, which has played an important role in human civilization by transforming the world into a technology era [Transistorized, 2007].

IC placed the previously separated transistors, resistors, capacitors and all the connecting wiring onto a single crystal semiconductor material. Starting with Small Scale Integration (SSI) with 1 to 100 devices to Very Large Scale Integration (VLSI) with 10^3 to 10^5 devices, we are presently in the era of Ultra Large Scale Integration (ULSI) with a count of 10^6 to 10^9 devices. Larger number of devices on a single chip is ever demanded for greater functionality and smaller electronic products. Thus, the major driving force for continue growth of the IC industry is the ability to "shrink" or "scale" the dimension of devices, which is the performance booster for higher speed and smaller power consumption.

Gordon Moore, a co-founder of Intel, tracked the history of the IC growth and predicted that "the number of transistors on an integrated circuit for minimum component cost doubles every 24 months" [Moore, 1965]. His statement is today's

well known Moore's law, which is thought to be the main guidance for future generations of ICs. It is due to this reason, semiconductor industry is making phenomenal growth and delivering exponential increase in the number of transistors integrated into single chip at lower cost (per transistor) over the last few decades. Figure 1.1 shows the actual number of components used to fabricate a whole range of Intel microprocessors produced from 1971 to 2007, following the trend predicted by Gordon Moore in 1965 [Moore's Law, 2007].

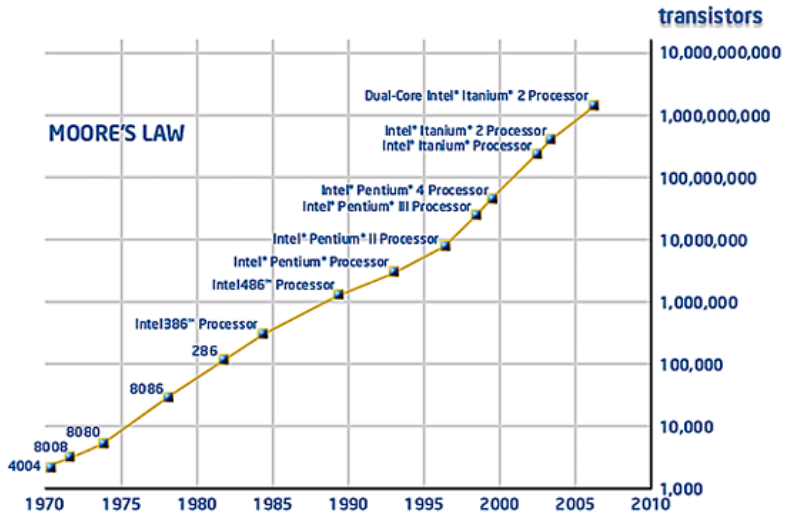


Figure 1.1: Actual number of components used to fabricate a whole range of Intel microprocessors produced from 1971 to 2007 [Moore's Law, 2007].

Keeping up with Moore's law is not an easy and trivial task, but it has been recognized as the "Golden" law in the IC industry. Over the years, great amount of efforts have been inputted and various innovative ideas have also been generated. The International Technology Roadmap of Semiconductor (ITRS) is one of the excellent examples. The ITRS is being established to provide the unified outline on device requirements and foreseen issues for device integration into the circuit level [ITRS,

2007]. It also serves as a communication platform among the global researchers, government organizations, industry manufacturers and suppliers to share and exchange their ideas and required supports to develop the more advanced and ever smaller transistors. Therefore, the ITRS roadmap has been successfully implemented for the past two decades to keep up with the pace of Moore's law. However, the guidelines set to increase the device numbers by scaling of both vertical and lateral dimensions of the transistors have become harder to achieve as it has approached the atomic level range. This has also alarmed the semiconductor community.

MOS (metal-oxide-semiconductor) devices associated circuits constitute approximately 90% of the semiconductor device market nowadays [Sze, 1998]. Among the various challenges in the ITRS roadmap, scaling down the dimension of transistors is one avenue to achieve faster devices with higher functionality while creating more densely pack circuits. However, the aggressive down scaling progress has aggravated the short channel effect (SCE) and thereby leading to the unfavorable degradation in the device performance. The SCE is more prevalent when the channel length is scaled down to the same order magnitude as the depletion width of S/D extension junction. This can be attributed to the 2 major physical phenomena, namely, (1) variation of threshold voltage as channel length is shortened and (2) restriction imposed on the electron drift characteristic in the channel region.

To resolve the SCE, formation of ultra-shallow junctions (USJs) in the S/D region, or more particularly the S/D extension, has been identified as one of the main roadblocks for device downscaling. Ever decreasing junction depth (X_j) and highly activated low sheet resistance (R_s) junctions in S/D extension junctions are desired to

sustain the scaling proportion of whole device. Unfortunately, the anomalous behaviors associated with the doping processes, such as transient enhanced diffusion (TED) and dopant clustering/de-activation, hinder the junction specifications required in the advanced devices [Cowern et al., 2000]. It has been the general consensus that the dopant anomalous phenomena are induced by the defects generated during doping steps, known as ion-implantation and post-implant thermal annealing.

Ion-implantation is a well-established process for the controlled doping in silicon substrate [Gibbons, 1972]. Due to its high reproducibility and precise control in dopant distribution and dose, it has been a preferred and industrial-oriented approach for junction doping and formation. However, extensive defects are induced during the implantation process. A subsequent thermal cycle (annealing) is necessary to electrically activate the doped atoms and repairing defects in the crystal body. It is during this thermal annealing process, transient enhanced diffusion (TED), dopant clustering/de-activation as well as evolution and dissolution of defects arise and thus leading to increase in final X_j or R_s that are undesired for USJ formation.

Generally, dopant diffusion/activation and removal of residual defects are the major factors to be considered in achieving optimum USJs. The complex interactions between the defects and dopants lead to a situation where trade-off has to be made to minimize dopant diffusion while sufficiently activating the implanted dopant as well as removing most of the defects to prevent junction leakage. For instance, one would wish to increase the annealing temperature to remove the implant defects, but the resulting dopant distribution profiles may diffuse to an extent that is unrealistic for USJ application. On the other hand, a lower anneal temperature could be used to

achieve shallower junctions; however, this might lead to the formation of high resistance and leaky junctions due to the lower dopant activation and the non-dissolvable remaining extended defects. In addition, the fraction of dopants being activated (R_s value) depends greatly on the dopant types and configurations of post-implant defects. Therefore, understanding of the defect evolution and defect-dopant interactions is very crucial as it affects the final properties and characteristics of USJs and subsequently to the device electrical performances.

1.1 Proposal Objectives

The primary goal of this thesis is to achieve highly doped and electrically activated USJs via the understanding and maneuvering of dopant-defect interactions, designated as defect engineering. This work revolves around the investigations of new USJ techniques, such as the co-implantation (C/F/N), advanced flash annealing and surface-defect engineering. To achieve the primary goal of this work, the studies will be carried out in 4 different main sections associated with their own specific objectives described as following:

(a) The Impact of Nitrogen Co-implant on Boron USJ Formation and Physical Understanding

The effect of N on B diffusion has been in controversy over the years. In this section, the impact of N co-implant towards the B USJ formation associated with preamorphization scheme will be explored. The objective is to find out the optimum N implant condition that could offer the most improved junction characteristics. In addition, understanding of the influence of co-implanted N atoms on the interactions

between dopants and defects is investigated. Finally, the competency of the junctions fabricated using the N co-implant will be reported.

(b) Understanding of Carbon/Fluorine Co-implant Effect on Boron USJ Formation

Although C/F co-implant is a well-established USJ technique, there are no available works which have compared the effectiveness between C and F co-implant on their respective junction stability coupled with the physical explanations. The other objective of this section is to expand the effect of C co-implant beyond the B atoms but also to the molecular BF_2 atoms, while it is also desired to have an idea on the F co-doping between the additional F co-implant and F doping via BF_2. Moving to the technological point of view, it is targeted to evaluate the potential of the various co-implanted junctions (C/F and N from previous chapter), in terms of their physical and electrical properties for the application in USJ fabrication.

(c) Understanding of Boron Junction in Preamorphized Silicon upon Optimized Flash Lamp Annealing

Flash lamp annealing (FLA) is an attractive advanced annealing technique for USJ fabrication. Although highly activated and nearly diffusionless junction is achievable by FLA, it leaves significant EOR defects around the amorphous/crystalline (a/c) interface induced by the pre-amorphizing implant (PAI). This results in high current leakage in the junctions. Hence, it is the primary purpose of this section to optimize the FLA with various possible schemes, for instance, multiple-pulse flash or combination of FLA with spike or soak RTA, to resolve the issue of residual defects remaining upon FLA. On top of that, it is also important to

understand the de-activation characteristic associated with the various proposed FLA schemes as well as their impact of the junction leakages. Simulation analysis on defect structure and defect evolution in the flash annealed B junctions is part of the interests in this chapter, so that a better physical picture for the dopant defect interactions during the FLA can be achieved.

(d) The Effect of Surface State on Boron Doped Pre-amorphization Junction for USJ Application

The properties of the semiconductor can be changed significantly by controlling the chemical state at the surface of the silicon substrate. In this section, the effect of surface state on B doped preamorphized junction will be explored. Part of this work seeks to investigate how the surface state could affect the B diffusion in junction and its influence towards the EOR defect evolution upon annealing. In addition, the junction stability under the different surface states is also one of the main concerns for USJ application. Finally, it is desirable to establish the theoretical explanations of surface effect on the USJ formation.

1.2 Organization of the Thesis

The thesis is outlined and organized with following chapters:

Chapter 1 delineates the background of the subject with a brief review of the semiconductor industry, along with challenges that hinder the progress of CMOS device scaling. It is then followed by highlighting the main motivations and the associated difficulties in USJ formation. The objectives and organization of the thesis are also included.

Chapter 2 covers the review of scientific findings and literature relevant to the defect engineering. Firstly, it presents the fundamental theories from MOS devices to USJ formation. This is followed by the review of various defect types that could be formed in the junction as well as the anomalous phenomenon in the USJ. Finally, various USJ techniques are briefly discussed in the later part of this survey to highlight both the advantages and disadvantages of each technique.

Chapter 3 describes experimental procedures and techniques used to process and characterize the samples in this work. Theories behind the major experimental techniques are also briefly elaborated.

Chapter 4 is dedicated to study the impact of N co-implant on B doped preamorphized junctions. It examines the effect of N distributions on B diffusion and activation in the junctions along with the proposal of possible involved mechanisms. Feasibility of the application of N co-implant for the USJ in PMOS devices is also reported.

Chapter 5 reports an extensive study on the C/F co-implant in the B/BF_2 doped preamorphized junctions subjected to isochronal soak annealing and spike annealing. It compares effectiveness of C/F co-doping in suppressing the junction de-activation behavior and B TED phenomena. The competency of the C, F and N co-implants for USJ application is also evaluated in the last section of the chapter.

Chapter 6 presents the study on the application of FLA in the B doped preamorphization junctions. Various FLA schemes are investigated in an attempt to reduce the residual defects in the PAI junctions. The impact of the various proposed schemes on junction stability and diode leakage is discussed. Lastly, the study also encompasses the simulation of some experimental results to complement the understanding on the effect of FLA on the B USJ formation.

Chapter 7 examines the effect of surface on B doped Ge pre-amorphized junctions. It reports that the B junction properties can be significantly affected by the surface state upon annealing. Similarly, the EOR defect evolution also responds to the different surface states. From the experimental results, a theoretical explanation is postulated for the effect of surface on the B USJ formation.

Chapter 8 concludes the major findings in this thesis in relation to the objectives in this work. Finally, it also provides some recommendations for future work.

Chapter 2

Literature Review

2.1 Introduction

This chapter serves as a brief review of literature and significant prior achievements which are related to this work. Since numerous studies have been performed so far, it is beyond the scope to cover all the details comprehensively. Instead, state-of-the-art and general insight to set up the background for this work will be described.

The main objective of this thesis is to fabricate ultra-shallow junctions (USJs) for the application in the future generation nano-MOS devices through defect engineering. Therefore, it will be appropriate to start with a description of the architecture of MOS devices. Issues on device scaling are discussed and the importance of USJ formation will be highlighted as well. In the following section, the discussion moves on to the generation, configuration and evolution of silicon defects. The associated mechanisms and other defect-induced phenomenon will be reviewed. The last part of the survey will focus on the current and developing techniques for USJ fabrication.

2.2 Architecture of Metal-Oxide-Semiconductor (MOS) Devices

Figure 2.1 shows the typical structure of metal-oxide-semiconductor field effect transistor (MOSFET). The basic components of this transistor include gate, gate insulator (gate dielectric), channel, source and drain junctions. To turn on the transistor, a bias voltage is applied to the gate (V_g). When the gate bias exceeds the threshold voltage (V_{th}), a conducting channel is formed in the silicon under the gate dielectric, connecting the source and drain junctions. Current flows from source to drain through this conducting channel as the voltage is applied (V_{ds} & V_{dd}). The device can be simply turned off by reducing the gate bias voltage below V_{th} [Sze, 2001].

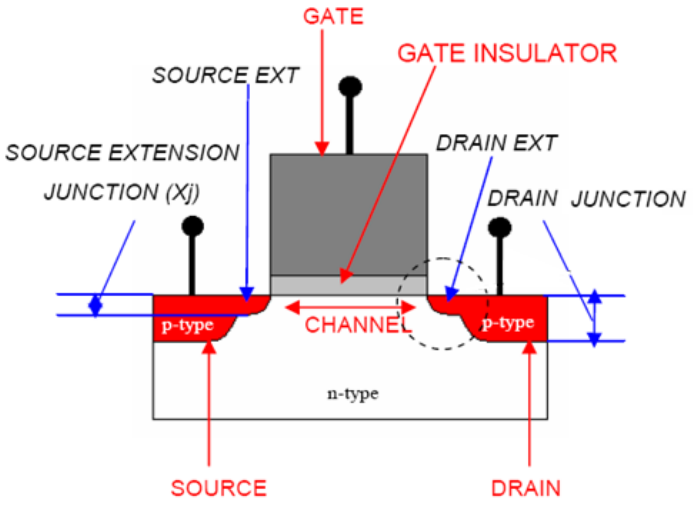


Figure 2.1: Schematic showing the typical structure of metal-oxide-semiconductor field effect transistor (MOSFET).

Over the years, transistor has gone through many advance developments, new features and changes are continuously being made. To fabricate a planar transistor,

the major processes include thin film deposition, etching, oxidation, ion implantation and diffusion. If we account each as single step, more than 300 processing steps are required to fabricate today's mainstream 90nm/65nm/45nm technology node MOSFET devices with physical channel length (gate length) approximately 40-60 nm [Thompson, 2002]. The transistor fabrication process will become even more complex in the future as further device performance improvement is ever desired.

2.3 Device Scaling and Challenges

In the past 40 years, it was realized that by simply scaling down the physical dimensions of transistor structure, improvements such as higher switching speed, lower power consumption and increase in device density per chip can be achieved. This has been used to fulfill the natural demand for faster, cheaper and more functional electronic IC requirements.

The phenomenon in transistor scaling was highlighted in 1965, when Gordon Moore observed an exponential growth in the quantity of transistor per chip since the invention of planar device. He predicted that "the number of components on a chip would double every two years" [Moore, 1965]. This predication has held not only as a guideline, but also as a challenge for device scaling in the IC industry. Keeping up with such a trend is not a trivial task. This has contributed to a cooperative effort from global industry manufacturers, governments, consortia as well as universities and colleges to outline the foreseen issues and problems associated with device scaling in an assessment map, called International Technology Roadmap for Semiconductors (ITRS) [ITRS, 2007].

Forward prediction of various device parameters down to year 2016 are listed in ITRS as the milestones for future device scaling. However, some of the predicted parameters are becoming harder to "scale". For instance, the switching speed of transistor is improved by compromising other device parameters such as current leakage. This indirectly suggests that major issues and problems are arising with the rapid scaling.

One of the most intensely studied issues is the scaling of gate dielectric thickness [Thompson, 2002]. Silicon dioxide (SiO_2) has been widely used for dielectric layer between the gate and channel in transistor. As the oxide thickness is thinned down to 1 nm, which is equivalent to 2-3 atomic layers, gate leakage current drastically increases. It leads to a serious problem in the stand-by power dissipation as well. It was suggested that integrating new materials with high dielectric constant (high-K) would help in reducing the leakage current [Plummer, 2000]. With a higher K value, the effective dielectric thickness can be increased to prevent the tunneling of carries through the gate insulator [Thompson et al., 1998]. For the cases of 65nm/45nm technology, SiON-based dielectric was used to relax the gate oxide thickness. This is basically achieved by maintaining the same equivalent electrical thickness via increasing its physical thickness. Similarly, other potential high-K materials such as hafnium oxide, zirconium oxide and rare earth elements oxide are c under active research and development for the application in future generation of devices below 32nm [Zeitzoff, 2001]. In year 2009, high-K dielectrics associated with metal gate has been initiated for the production of Intel 32nm chip [Packan, 2009].

Another scaling issue lies in the gate electrode of the transistor. The use of polysilicon gate is the key advance in today MOS technology, since it allows the self-alignment of source/drain junctions during the fabrication process, preventing any overlay errors by having the lithography step to define the source/drain regions. However, the pre-doping of polysilicon by ion-implantation in current technology becomes no longer reliable as the gate electrode is continuously scaled down. When gate voltage is applied to turn on the device, in the case of 90nm, a depletion layer is formed in the pre-doped polysilicon gate, adding about ~0.2 to 0.5 nm to the effective oxide thickness [Plummer, 2000]. Similarly, the same extent of degradation will result from the quantum mechanical effects as well. Considering the gate dielectric with approximately 1 nm, the effective oxide thickness could be doubled (~2nm). If the gate is further scaled down, the depletion phenomenon will become more apparent and seriously reduce the charge density in the channel region when the device is turned on and hence resulting in the degradation of transistor electrical performance. The application of metal gate electrode has proven to be the most practical solution, but it is associated with integration issues that require certain changes to the process. Nevertheless, successful metal gate integration with the high-K dielectric into modern device has been demonstrated in recent years [Datta et al., 2003, Tseng et al., 2004, 2005, Xiong et al., 2006].

In the MOS device scaling theory, the electric field or potential should be maintained in the device to gain the optimum performance enhancement. Device physical dimensions such as gate/channel length, gate oxide thickness, junction depth and others are to be scaled down by the same scaling factor. Unfortunately, this

cannot be attained because the scaling rate of gate dielectric thickness and source/drain junction depth could not follow the aggressive scaling in channel length. Therefore, the electric field lines have changed tremendously, resulting in a roll-off of the threshold voltage for the short-channel MOS device, known as short channel effect (SCE). The immediate drawback of SCE is the current leakage has become excessive and is being identified as one of the most important challenges in device scaling.

To minimize the SCE, one can reduce either the gate oxide thickness or reduce the junction depth. The issues related to gate oxide have been discussed above; aggressive reduction in junction depth, designated as ultra-shallow junction (USJ) formation, faces various major challenges over the years and it is the main focus of this thesis.

2.4 Ultra-shallow Junctions (USJs)

One main component in the MOS devices is the source/drain (S/D) regions [ITRS, 2007]. In modern high performance MOSFET technology, the S/D regions typically comprise of deep S/D junctions and shallower S/D extensions located at the 2 sides of the gate edge, as shown in figure 2.1. As the junctions become shallower, particularly in S/D extensions, suppression of SCE is more significant. It is also well recognized that there are other critical device parameters, directly and indirectly, are affected through the formation of USJs. The junction formation in current technology relies on the ion implantation and post-implant annealing to introduce the dopants into the substrate.

2.4.1 Ion Implantation

Ion implantation is a widely used technique to induce phase transformation, synthesis and structural modification of materials. It is also a well-established doping process for fabricating junctions due to the following reasons:

(1) Wide selection of beam sources (dopant species) with high purity.

(2) High precision in controlling the spatial location and concentration of implanted ions.

(3) Excellent reproducibility and uniformity.

(4) Flexible in the integration of new advance processes.

(5) Improved yield for devices/circuits.

During the ion implantation, the dopant ions are accelerated with a specific energy and directed into the substrate. Ions penetrate through the surface, colliding with lattice atoms before coming to rest at some depth after losing all their energy. Generally, there are two types of stopping interactions involved. One of them is nuclear stopping, where the impinging ions collide directly with the target atoms. The collisions are Coulomb elastic collision, with some of the energy is transferred from the incoming ions to the target atoms and the total momentum of the system is preserved. As opposed to this, the overall momentum is not conversed in electronic stopping, in which the impinging ions lose energy to the target electrons.

The stopping mechanisms determine the statistical distribution of the implanted dopant atoms. Figure 2.2 shows the simulation of the ion trajectories for 50 keV Boron (B) implanted into silicon substrate. It has been recognized that electronic stopping dominates low energy implant, while high energy implant is dominated by

the nuclear stopping mechanism which causes the host atoms to recoil leading to a subsequent nuclear collision cascades. An example of stopping power relative to the stopping energy is shown in figure 2.3.

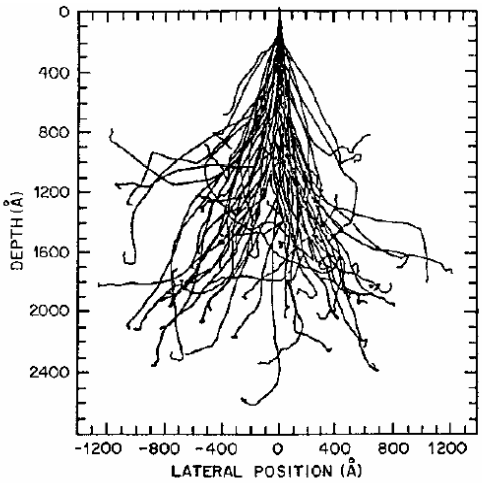


Figure 2.2: Monte Carlo simulation of the ion trajectories for 50 keV B implanted into silicon [Sze, 2001].

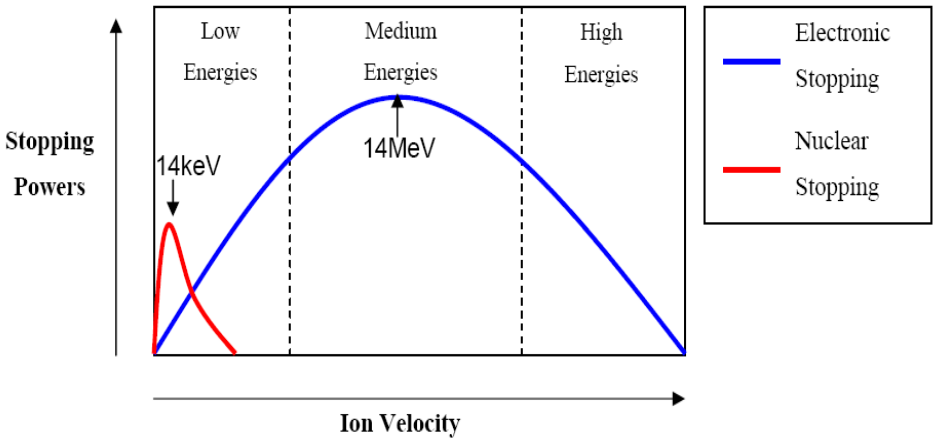


Figure 2.3: Relative amount of nuclear and electronic stopping power as a function of the ion velocity. The peaks in the stopping powers are indicated for silicon to be at ion energies of 14 keV and 14 MeV for nuclear and electronic stopping in silicon, respectively.

The minimum energy to displace a lattice atom from an impinging ion is around ~13 eV [Nastasi, 1996]. Typical ion implantation induces a series of cascade collisions and recoils in the silicon substrate, resulting in extensive damages to the crystal structure. In many instances, the as-implanted silicon damages, designated as defects, constitute of the silicon interstitials and vacancies (also known as Frenkel pairs). The defect configurations induced by implantation can range from isolated point defects, point defect clusters, amorphous pockets (surrounded by crystalline silicon) and to a continuous amorphous layer. It is thought that implantation is the origin of silicon defects, subsequently affecting the junction properties which inhibit the formation of USJs. Thus, the understanding of ion implantation induced damages/defects is very crucial.

The most direct method to fabricate USJs is by lowering the implant energy. In theory, the depth of implanted dopants is proportional to the energy of implantation. Shallower junctions can be fabricated by decreasing the ion beam energy to the lower range. However, there are challenges in continuously lowering the implantation energy. The throughput of the ion implantation processes will be significantly degraded when ion beam energy decreases, and such a process becomes extremely costly for manufacturing. In addition, to achieve a sub-keV low energy implant of light mass atoms, such as B for PMOS extension junctions, it requires the use of acceleration/deceleration mode which leads to unavoidable energy contamination and worse doping uniformity across the wafer.

In addition, another major drawback of ion implantation in silicon substrate is dopant channeling, resulting in the long dopant profile tail. This is attributed to the

incoming ions moving in the direction along with the crystal structure plane, where long range open space which serves like "channel" that the ions can travel without significant scattering. The channeling effect is pronounced for light dopant species, such as B and Phosphorus (P). It was found that such effect can be inhibited by tilting the substrate at certain angles; however, this approach offers marginal improvement in the ultra-low energy ion beam implantation. The channeling effect becomes even more significant when the junction requirement is scaled down to sub-50 nm range.

Pre-amorphizing implant (PAI) is adopted as a solution to prevent channeling in the advance technology junction. The technique uses higher mass dopant implantation to destroy the crystalline structure of the silicon substrate, generating a continuous amorphous silicon layer. Since the amorphous layer is a highly non-uniform lattice layer, ion channeling is greatly reduced [Jones el al., 1998, Foad et al., 1998].

For instance, BF_2 ion implantation is commonly used as it can induce amorphization during the implantation for de-channeling. Since it does not require additional pre-implant step (eg. Si/Ge implant), it is also known as self-amorphization. Due to its high atomic mass ratio (i.e 11-B to 49-BF_2), shallower B dopant profile would be obtained for BF_2 at the same implant energy of a typical implantation using B ions only. However, BF_2 doping has disadvantages due to the presence of Fluorine (F) atoms. The B-F pairing in the junction reduces the activation of B dopants and also the implanted F atoms at the gate (during the implantation to S/D regions) enhance the B penetration into the channel region which degrades the device performance [Aoyama et al., 1995].

Another favored technique in pre-amorphization is pre-implantation of heavy inert ions, such as Si or Ge, before doping of the desired ions. In this scheme, one would have the flexibility in choosing the amorphous layer thickness (defined by the heavy ion implant) regardless the depth of subsequent dopant implantation. A well defined and sharp transition between the amorphous and crystalline (a/c) interface can also be obtained. Unfortunately, this technique generates high concentration of silicon damages/defects beyond the a/c interface upon annealing. The silicon interstitials around the a/c interface will agglomerate into defect band during the dopant activation process, leading to various detrimental effects to the USJs.

2.4.2 Post-implant Annealing

One main disadvantage for ion implantation is the introduction of silicon damages/defects, which remain after the doping process. Since only a 13 eV is required displace the host silicon atom from its lattice site [Nastasi et al., 1996], even a very low energy ion beam implantation can easily destroy the silicon substrate to highly disordered structures. To form a conductive junction, subsequent thermal cycle, known as thermal annealing, is essential in the process to activate the implanted dopants as well as to repair the silicon lattice damages induced during the ion implantation.

The success of thermal annealing can be assessed by the fraction of dopant that is being electrically activated, which corresponds to the dopants at the substitutional lattice sites. It can be measured by the Hall effect measurement technique. However, a more common way to examine the effect of annealing is by

measuring the sheet resistance (R_s) of the implanted junction since R_s is inversely related to the dopant activation level. The R_s value can be used as an indirect method to indicate the extent of a junction is being activated during the anneal cycle.

The characteristics of thermal anneal process depend on the implanted dopant type, energy and dose. There is a clear distinction between a typical implantation, where the crystal silicon structure has been merely partially disordered; and PAI, where the silicon substrate is being amorphized by heavy ions. In the first case, the implanted area still remains as crystalline and exists together with interstitial and vacancy point defects or even point clusters which highly depend on the implantation conditions. As annealing proceeds, the interstitials and vacancies recombine, lattice repair occurs by the generation and diffusion of point defects. To remove all the implanted defects, activation energy of about 5 eV (equivalent to thermal energy at temperature of 900^{o}C) is necessary [Pichler, 2006]. The activation of implanted dopants is also taking place while the crystal lattice is being repaired. Incomplete thermal annealing will result in the reduction of the active dopant fraction.

For amorphized silicon, re-crystallization takes place during the initial stages of annealing where the re-growth proceeds via solid phase epitaxy re-growth (SPER). The a/c interface will move towards the surface, clearing all the defects and placing the dopants in the substitutional sites of the lattice. It has been reported that the re-growth velocity can vary with the presence of different types of ions and it was inferred as a result of the bond binding and breaking pathways during the re-crystallization [Pelaz et al., 2005]. The activation energy for SPER is about 2.3eV [Pichler, 2006], and it implies that damages/defects are easier to be repaired in the

amorphous layer. Nevertheless, it is worth mentioning that the excess of interstitials beyond a/c interface cannot be easily removed completely and will agglomerate into a defect band, designated as EOR defects. The EOR defects evolve to different types of defects and dissolve at extremely high anneal temperature or transform to more stable extended defects [Lindsay et al., 2002].

The major downside of thermal annealing in junction formation is the diffusion of dopant atoms and defect agglomeration. Thus, the anneal parameters - ramping-up, dwell period and ramping-down play significant roles. A number of groups have studied the effect of ramp rates on the diffusion and electrical activation of dopants during the annealing cycle [Agarwal et al., 1999, Mannino et al., 2001]. It was shown that by increasing the ramping rates, higher dopant activation while minimizing the dopant diffusion could be achieved [Larson, 2000]. However, it was later reported that very high ramp-up will saturate at a certain level, where it does not help in reducing junction depth or improving dopant activation further. In this case, it would rather delay the dopant diffusion effect in the ramp-down portion of the anneal cycle [Agarwal, 2000].

Similarly, various anneal schemes are being studied. Particularly, high peak temperature and very short dwell soaking time was shown to be beneficial for shallow junction formation. The theoretical basis for this trend is that activation energy of dopant diffusion is greater than that of defect reduction [Larson, 2000]. Thus, higher temperature provides greater efficiency to remove damage and activate the dopants, while the short soak time inhibits dopant diffusion, producing a highly activated shallow junction with minimum defects. Evolution of the anneal techniques can be

seen over the years, from the early furnace annealing to rapid thermal annealing and today commonly use of spike annealing. The differences of these anneal techniques basically lie in their respective anneal temperature profiles; for instance, the spike annealing has a ramp-up rate of 200 ~ 400^{o}C/s and soak time of 0 ~ 1s compared to typical RTA with 30 ~ 150^{o}C/s and 10 ~ 100s, respectively [Larson, 2000]. In addition, novel advance anneal schemes such as flash and laser annealing have been shown to be potential candidates to replace spike annealing for the USJ application in the future. However, it is found out that the thermal budget of laser/flash annealing is too low to repair the implant damage fully [Lerch et al., 2005, Lenoble, 2006]. Instead of switching from spike to flash/laser annealing directly, these advanced anneal techniques have been employed as additional post-annealing step to enhance the activation of the junctions. There are many on-going studies trying to evaluate and understand the evolution of damages/defects under these advanced anneal schemes for the application in advanced MOS devices.

2.5 Defects

The main process steps, both ion-implantation and thermal annealing, used in the fabrication of USJs have been introduced in the last section. Now we move on to the discussions of the generation, evolution and configuration of defects.

2.5.1 Origin of Defects

Ion implantation is the most favored doping technique used in junction formation due to its superior advantages as discussed in section 2.4.1. In a typical

implant, where the extent of implant damage is not high enough to disorder completely the periodicity of silicon crystal structure, this can be classified as the non-amorphizing implant. If the implant dose and energy are increased so that the surface crystalline region of the silicon substrate evolves to an amorphous phase, it is known as amorphizing implant. The benefits of amorphizing implant have been mentioned previously, and an excellent review of this technique has also been reported by Pelaz et al. [Pelaz et al., 2005]. The reason to define these two implants here is because the resulting defects are inherently different from each other, subsequently affecting the evolution pathways of the defects. Figure 2.4 shows schematically the difference between the non-amorphizing and amorphizing implants.

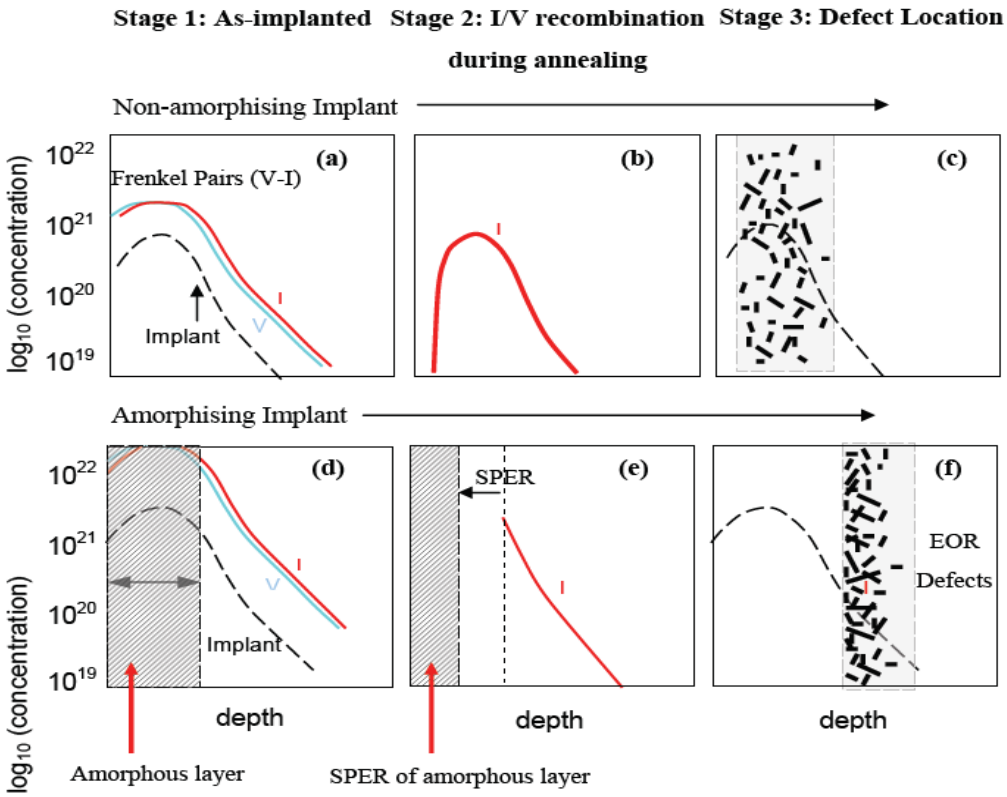


Figure 2.4: Schematic representation of a non-amorphizing implant and an amorphizing implant. The two sequences show essentially the main differences between the two implant regimes [Cowern, 2003].

In the non-amorphizing implant case, annealing the vacancies (V) and interstitials (I) (Frenkel pairs) generated by the implanted ions result in recombination, leaving a band of excess silicon interstitials. These excess of interstitials are resulted from the activation of implanted ions on to the substitutional lattice sites, roughly equal to the number of implanted ions (i.e there is one excess of silicon interstitial generated for every implanted impurity ion, it is known as the plus-one model [Giles, 1991]). The excess interstitials evolve into extended defects and distribute across the implanted dopant profiles.

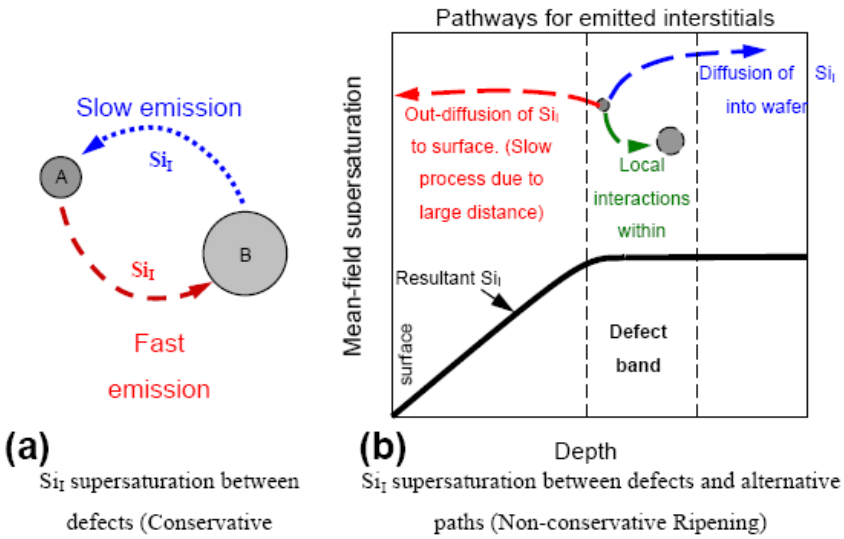
On the other hand, when a pre-amorphized substrate is annealed, the crystalline substrate beneath the amorphous region serves as a "seed" layer for re-growing the amorphous phase into a near perfect crystal [Olson et al., 1988]. No residual point defects are thought to remain in the amorphous region since all the disordered silicon atoms and dopants are placed into the lattice during the SPER. However, a supersaturated excess of interstitials will remain beyond the amorphous layer near the end of implant profile, known as end-of-range (EOR) defects. Since the rate of interstitial nucleation is far greater than that of SPER, this leaves a band of extended defects at the EOR region [Colombeau et al., 2004].

2.5.2 Evolution of Defects

Post-implantation annealing is a crucial process as it involves the evolution of defects that will affect the properties of the junction significantly. Interstitials and vacancies recombination associated with substitution of dopants into lattice sites will take place once the annealing is initiated, generating excess of silicon interstitials in

the implanted substrate (based on the plus-one model). The resulting supersaturation of silicon interstitials evolve into extended defects. The location and concentration of the interstitial supersaturation are implantation-dependent (either non-amorphizing or amorphizing), which also affecting the configuration and type of extended defects to be produced.

Extended defects grow in size and reduce their density, while the number of silicon atoms bound to the defects stays constant when the interstitial-defect agglomeration reach the stable state. This phenomenon has been interpreted as being an interchange of silicon atoms between defects of different sizes following an Ostwald ripening process [Colombeau et al., 2004]. The theory of Ostwald ripening [Ostwald, 1900] was formulated by Greenwood [Greenwood, 1956] and considerably extended by Lifshitz, Slyozov and Wagner, and the latter is known as LSW theory [Jain et al., 1978]. Figure 2-5(a) shows a schematic of the conservative Ostwald ripening process, where small defects interchange self-interstitials with larger defects. Figure 2-5(b) illustrates the more realistic process, taking into account the probability of free interstitials which can diffuse to the surface or into the bulk wafer. This occurrence is indicated by the decrease in interstitial supersaturation from the defect band to the surface. This means that there are many parameters which can affect how the defects evolve and dissolve. In general, the exact type of the predominant defects depends on ion dose, energy and annealing conditions. A “catalogue” exists where almost all of the possible defects found after a certain implantation and annealing combinations have also been reported [Jones et al., 1988a].



Si_I supersaturation between defects (Conservative)

Si_I supersaturation between defects and alternative paths (Non-conservative Ripening)

Figure 2.5: (a) Conservative Ostwald ripening; where the large defects grow at the cost of the smaller defects. (b) Non-conservative ripening; where alternative paths affect the ripening process.

2.5.3 Configuration of Defects

As the defects grow in size or change their crystallographic structure from one type to the next, their formation energy decreases. The formation energy of a defect is the energy required to add one extra atom to the defect. Figure 2.6(a) shows the formation energies calculated through a combination of theoretical [Cowern et al., 1999a, b] and experimental work [Colombeau, 2001]. This is a crucial result since the decrease in formation energy is the driving force for defect evolution upon annealing. The curve in figure 2.6(b) can be broken into three sections based on the defect states: (1) clusters, (2) {113}'s and (3) dislocation loops. The second Y axis shows the level of supersaturation of silicon interstitials decreasing as the defects evolve from clusters to loops. Figure 2.6(b) and figure 2.7 are the plan-view TEM micrographs of different extended defects formed after annealing and the description of each type of defects.

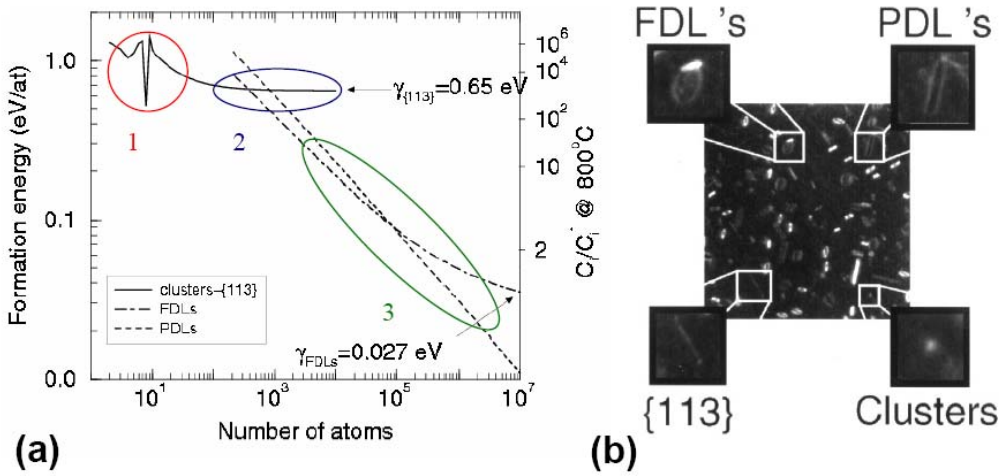


Figure 2.6: (a) Formation energy decreases as the defects evolve from clusters to loops: the driving force to the evolution. (b) TEM images of the actual defects [Cowern et al., 1999a, b].

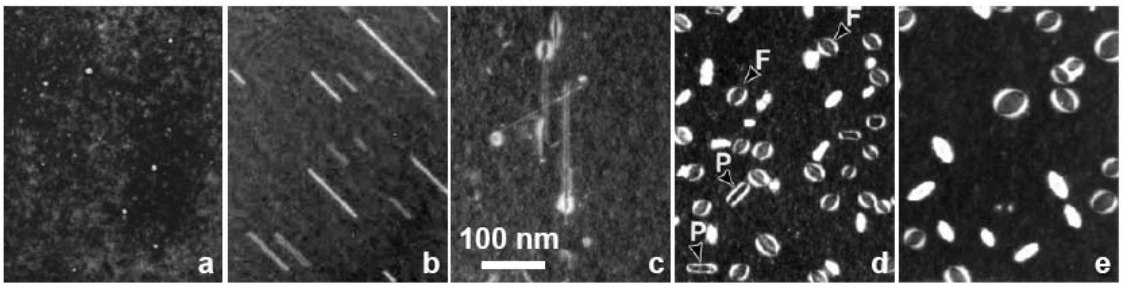


Figure 2.7: Different types of defects formed after annealing (a) clusters, (b) {113}'s, (c) transformation from {113}'s into dislocation loops, (d) PDL's and FDL's and (e) FDL's only [Claverie et al., 2002].

2.5.3.1 Clusters

Immediately following implantation and/or during the anneal ramp-up, most of the excess interstitials are stored as di-interstitials. Due to the Ostwald Ripening mechanism, they begin to cluster and then vary in size; it is thought that clusters of more than 20 atoms are similar to {113} defects [Claveria et al., 2003].

2.5.3.2 {113} Defects

(a) Rod-like {113} defects

Rod-like defects are assumed to be elongated planar {113} defects in the <110> direction (Figure 2.7(b)) [Claveria et al., 2003]. Eaglesham et al. showed [Eaglesham et al., 1994, 1995] that {113} defects are an important source of the interstitials in TED. In the experiment, a B delta-doped superlattice implanted with 40 keV silicon atoms was used to prove that the number of interstitials emitted by the defects is correlated with the flux of interstitials upon annealing, which is the main driving force for B TED.

Investigations by Zhang et al. showed that {113} defects are not the only source of interstitials behind TED and in fact there may be more than one source [Zhang et al., 1995]. This was evidenced by experiments by Eaglesham et al. with low B energy and dose showing that although TED was observed, TEM did not show the presence of {113} defects since they were below the detection limit.

Liu et al. confirmed Zhang's results and went on to show that for B implant energies above 10 keV {113} defects are seen by TEM and they actually enhance the already present B TED [Hodgson et al., 1984]. They concluded that the first source of TED is due to the formation and release of interstitials towards the surface from BI pairs. The second source is the dissolution of the {113} defects providing interstitials for the formation of mobile BI complexes.

(b) Zig-Zag {113}'s

Agarwal et al. found a different form of {113} defects known as "zigzag {113}'s" [Agarwal et al., 1997a]. These defects can be detected by high resolution cross-sectional TEM (in figure 2.8), are corrugated across their width and are more stable than ordinary {113} defects. They formed in the early stages of annealing (Ar ambient) after a 5 keV silicon implant with a dose of $3x10^{14}$ cm^{-2}. It is evident from these results that even at low implantation energies, the formation and dissolution of {113}-type defects will continue to modulate interstitial injection and TED.

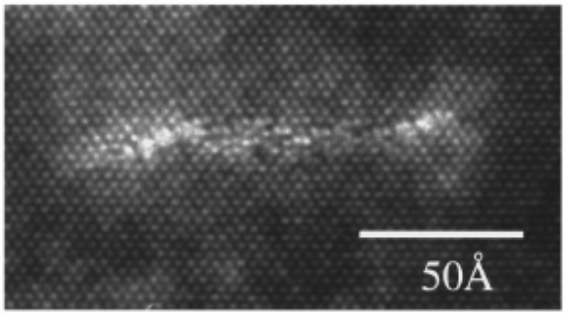


Figure 2.8: High resolution XTEM image of a zigzag {113} defect [Agarwal et al., 1997a].

2.5.3.3 Dislocation loops

There are two main types of dislocation loops, faulted and perfect. These dislocation loops have been found to be more stable than {113} defects, which formed after annealing on the implanted samples with a silicon dose of $2x10^{14}$ cm^{-2} and an energy of 100 keV [Claverie et al., 2003].

Perfect dislocation loops, Figure 2.7(d), are reported to be either elongated, near circular or hexagonal objects and have even once been referred to as

"Rectangular Elongated Defects" (REDs) [Claverie et al., 2002, Raman et al., 1999] These defects have been studied by Claverie at al. and were observed to be elongated with hexagonal shaped ends [Claverie et al., 2002, 2003].

Faulted dislocation loops, shown in figure 2.7(d) and (e), are interstitial in nature [Claverie et al., 2003] and survive at higher anneal temperatures [Claverie et al., 2000a]. They are also thought to have the same density of excess silicon atoms.

2.6 Challenges in USJs

Silicon damages/defects induced by ion implantation are known to interact with dopants, contributing to transient enhanced diffusion (TED) and clustering of dopants [Stolk et al., 1997]. These two behaviors have been well recognized as the underlying causes of increase in final junction depth (X_j) and sheet resistance (R_s) during the post-implantation annealing process. In addition, the non-dissolvable extended defects after thermal annealing have also been reported to cause high current leakage at the device level. Combining all these unfavorable effects, they become the major challenges to be tackled for the formation of nano-scale USJs in the advanced MOS devices.

2.6.1 Mechanisms of Dopant Diffusion in Silicon

Fick's law of diffusion is described as the macroscopic phenomena of dopant diffusion, which states that once a concentration gradient is established, ions diffuse

from a high to low concentration in proportion to their respective inherent diffusion coefficient. However, on top of the macroscopic diffusion characteristic, dopant diffusion in silicon is associated with a series of anomalous diffusion phenomena. Therefore, it is crucial to determine the mechanisms of how defects (interstitials/vacancies) interact with the dopants. Fahey et al, Bracht et. al. and Jain et. al. published comprehensive reviews on the mechanisms of dopant diffusion in silicon substrate [Fahey et al., 1989, Bracht, 2000, Jain et al., 2002].

The most commonly cited possible diffusion mechanisms of impurity dopant atoms in silicon are shown in figure 2-9, referring to Bracht's notation.

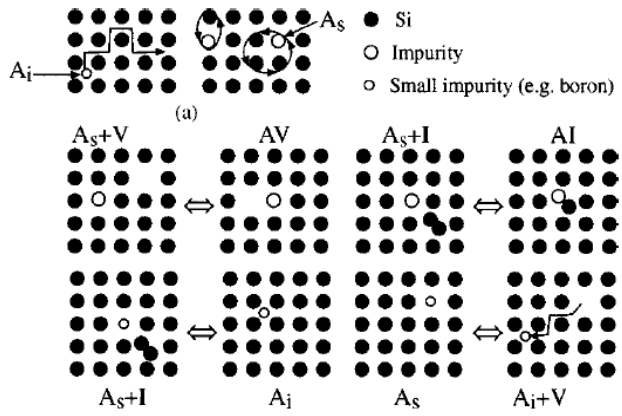


Figure 2.9: Schematic representation of (a) direct and (b) indirect diffusion mechanisms of an impurity atom A in a solid. V and I denote the vacancies and interstitials. Subscripts I and s indicate interstitial and substitutional positions of the foreign atoms. AV is the pair of A and V and AI the pair of A and I [Bracht, 2000].

The direct mechanism, shown in figure 2.9(a), involves no point defects. The dopants diffuse either via interstitial lattice or localized exchange between the interstitial and vacancy position. It requires very large activation energy, resulting in

diffusion at very small rate at which it cannot be observed in the experiments. In contrast, figure 2.9(b) refers to the indirect diffusion mechanism, in which the diffusion of dopants takes place with the help of point defects. In another words, the diffusion involves the reactions between the point defects and dopant atoms. The four common reactions are given below:

$$A_S + V \Longleftrightarrow AV \quad \text{Vacancy Mechanism} \quad (1)$$

$$A_S + I \Longleftrightarrow AI \quad \text{Interstitialcy Mechanism} \quad (2)$$

$$A_S + I \Longleftrightarrow A_i \quad \text{Kick Out Mechanism} \quad (3)$$

$$A_S \Longleftrightarrow A_i + V \quad \text{Dissociative Mechanism} \quad (4)$$

Here A stands for the dopants, subscripts s and i indicate substitutional and interstitial positions, while V and I are vacancies and interstitials. AV and AI are defect pairs of the corresponding point defects. For instance, the main governing diffusion mechanism for dopants such as B (Boron), P (Phosphorus), C (Carbon) and In (indium) are interstitialcy (2); whereas As (Arsenic) and Sb (Antimony) are thought to diffuse via vacancy (1). It is worth to mention that, in the boron case, kick out mechanism is also heavily involved in the diffusion. Therefore, reactions (2) and (3) are not explicitly defined for boron atoms, but it is generically termed as interstitial-mediated diffusion. This has been proven from the ab-initio calculations that more complex mechanisms are involved, representing at an interstitial driven process without explicitly phase out the configuration of defects as it diffuses [Jain et al., 2002]. Thus, a boron interstitial (BI) notation is commonly used. A similar situation also applies to other dopants, such as the vacancy-mediated diffusion of Arsenic dopants. The details of the absolute mechanisms for different dopants are

believed to be extremely complex; however, we should keep in mind that the four reactions shown in above play a dominant role for the diffusion of dopants in silicon.

2.6.2 Transient Enhanced Diffusion (TED)

TED is a phenomenon observed during the post-implantation annealing process. As described in the previous section, the diffusion of dopants is defect-mediated. Dopants would experience enhanced diffusion in the silicon with the presence of implanted-induced defects. Since B and P are interstitial-mediated diffusing dopants, they are susceptible to the TED during annealing due to the supersaturation of excess interstitials induced by implantation (based on the +1 model).

Hofker et al. showed that B has an anomalous diffusion effect in 1970s [Hofker et al., 1973]. The chemical dopant profiles after annealing at 800^{o}C for 35 minutes and 21 hours extracted from the Hofker's results are shown in figure 2.10. He realized that large supersaturation of point defects is the cause of the rapid diffusion in early part of the annealing and it will saturate over the time.

TED of dopants becomes widely recognized only when Michel et al. performed an extensive study on the annealing of B profiles over wider range of temperature and time, depicted in figure 2.11[Michel et al., 1987]. They showed the real extent of transient diffusion observed from the experiment, at which the TED decay time was shown to be around 45 minutes at 800^{o}C. It is found that the TED decay time is exponentially decreases to 1s at 1000^{o}C. In addition, it was verified that

the B enhanced diffusion is a "transient" behavior at which it saturates eventually across the time.

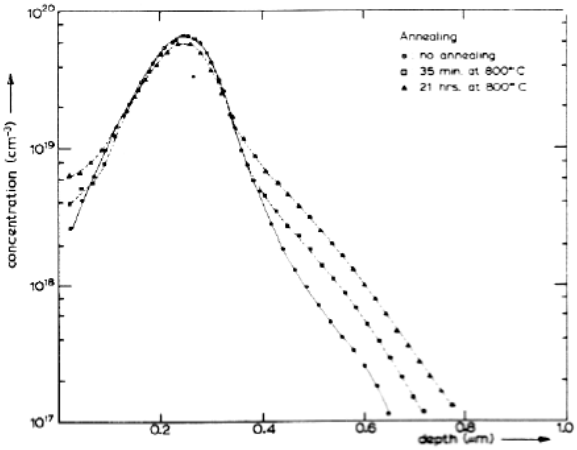


Figure 2.10: Hofket's original discovery of B anomalous diffusion, indicating a large amount of B diffusion at 800°C for 35mins which saturates over a longer time [Hofker et al., 1973].

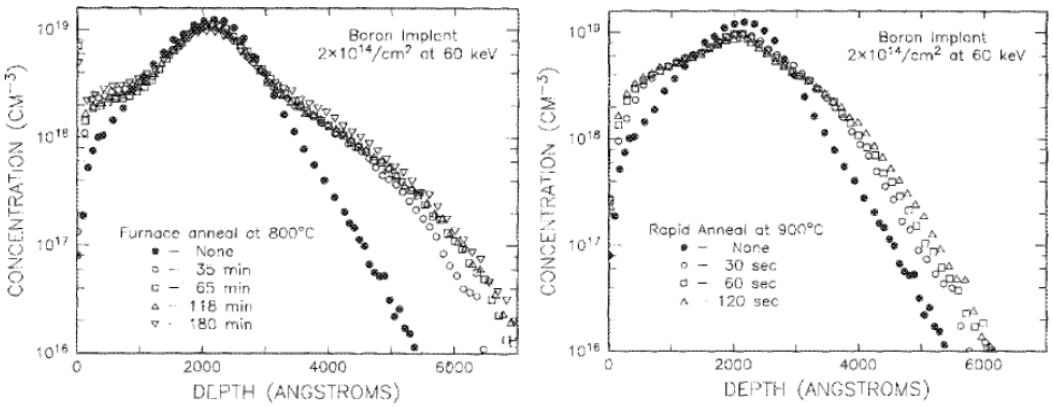


Figure 2.11: The isothermal study performed by Michel et al. with a 60 keV, 2×10^{14} cm^{-2} B implant, clearly showing what is now known as TED [Michel et al., 1987].

Eaglesham et al. and Cowern et al. discovered that the extended defects, ({113} defects) are indeed maintaining the supersaturation of interstitials by emitting the silicon atoms during the annealing [Eaglesham et al., 1994, Cowern et al, 1990]. It

was concluded that extended defects could be the driving force for anomalous diffusion which in turn prolongs the TED phenomenon.

The effects of implant energy were studied by Liu et al.; B was implanted at varying energies and then isothermally annealed. The results showed that as implant energy increased so did TED (also seen by Chao *et al.*), this was related to the release of silicon interstitials from {113} defects for energies >10 keV [Liu et al., 1997, Chao et al., 1996]. For the lower energy of 5 keV, B interstitial (BI) pairs are thought to be the cause of the TED, where the duration of the enhancement is less for the higher energies. Agarwal et al. studied the effect but for lower energies <5 keV, and found results similar to that of Liu [Agarwal et al., 1997b]. This was described as being due to the increased surface recombination of interstitials. As opposed to this, King et al. showed surface recombination does not play an important role in defect dissolution [King, 2003].

Another implantation effect on TED is the dopant dose. Cowern *et al.* showed that TED increased with dose, until it eventually saturated at higher doses [Cowern et al., 1990]. A similar effect was observed by Chao *et al.* [Chao et al., 1996]. In their study (shown in figure 2.12),they showed that in the lower dose range (e.g. $3x10^{14}$ cm^{-2} annealed at 900ºC) broadening of the dopant profiles increases with dose, but towards the highest dose ($5x10^{15}$ cm^{-2} annealed at 900ºC) the displacement decreases until it saturates. For the lower doses, the TED is attributed to the release of silicon interstitials from interstitial clusters formed during implantation which dissolve during annealing, and as the dose increases so does the size of these clusters [Michel, 1987]. However, when the dose is high enough to result in the formation of highly

stable clusters, then it will become a sink for interstitials which decreases the TED enhancement.

Lamrani et al. showed direct evidence of the recombination of silicon interstitial atoms at the surface [Lamrani et al., 2003]. They grew four B marker layers at different depths within a silicon substrate and implanted silicon to form a layer of extended defects on top of the second marker layer. It was shown that after annealing, TED was observed in the B marker layers. They also showed a gradient of the supersaturation of interstitials towards the surface as a result of the surface recombination of silicon interstitial atoms that escaped the defect region. This experiment suggests that substrate surface would be a good sink for implanted-induced interstitials.

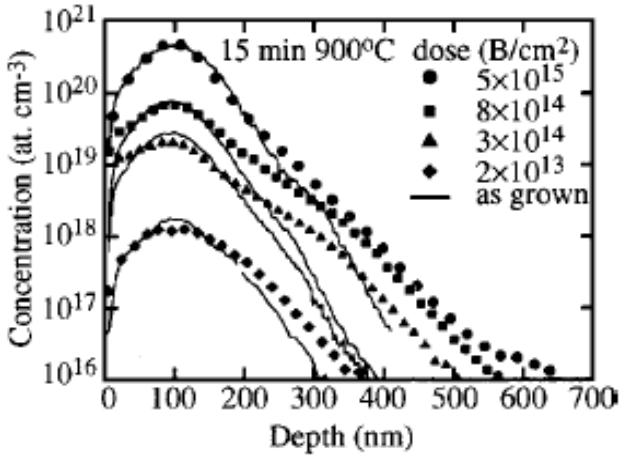


Figure 2.12: Implant dose dependent boron profiles, solid lines (as-implanted), symbols (900^{o}C 15 min annealing) [Cowern et al., 1990].

2.6.3 Dopant Activation and Clustering

In the new generation of devices, the requirements of USJs are not only restricted to the depth of junction, but also to the extent of the implanted dopant activation during the annealing process. As mentioned previously, the level of dopant activation can be indirectly indicated by the sheet resistance, R_s.

Generally, the junction depth can be related to the TED phenomenon; while the solid solubility was thought to be the main limiting factor for the level of dopant activation. Clustering of implanted dopants with defects results in a large fraction of dopants being electrically de-activated and simultaneously reduces its activation level well below the dopant solid solubility limit. Thus, it is essential to understand the clustering mechanism of dopants during the anneal process to optimize the R_s of the final junction.

Similar to the dopant diffusion mechanisms, the pathways involved in dopant clustering are complex. One of the reasons is that the dopant-defect clusters are generally very small and it is not possible to observe them in detail experimentally. In order to study these clusters, combination of indirect experimental information with modeling and simulation are necessary.

For the case of B, both experimental and theoretical work suggests that B atoms combine with interstitials to form boron-interstitial clusters (BICs). It is customary to represent the BICs composition in the form of B_mI_n, where m denotes the number of B atoms and n denotes the number of silicon interstitials in the clusters [Picher, 2006]. During the early stages of thermal annealing, interstitial

supersaturation is large, high interstitial content clusters (BI_2, B_2I_2, B_3I_3 ...) are easily formed near the Si surface, resulting in an immobile peak in dopant profile. On further annealing when the interstitial supersaturation reduces, large clusters will emit interstitials into the system and leave behind with the high B concentration clusters (B_3, B_4I, B_4 …). These B clusters are generally stable and will dissolve only after a long annealing is performed. Throughout the dissociation of BICs, the level of dopant activation is expected to increase, leading to reduction in R_s; however, this is offset by the TED of the B.

The immobile static peak (the BICs) near the surface region has caused some controversies in the literature. Hodgson *et al.* noticed this peak whilst annealing the B implanted silicon [Hodgson et al., 1984]. They observed that the tail of B profile diffused a lot faster than the peak close to surface and concluded that this was due to the B atoms occupying interstitial positions which allowed them to diffuse at low temperatures. Michel *et al.* showed similar diffusion results at which the B electrical activation can be improved by increasing the anneal temperature and the B atoms also behave in a similar way to the saturation of the anomalous diffusion [Michel et al., 1987]. Therefore, it was concluded that in the peak of B profile, the B atoms were inactive and its diffusion was due to dissolution of clusters of point defects rather than the diffusion of interstitial boron atoms. Holland *et al.* argued that the peak was due to active substitutional boron, but that the tail was due to interstitial B. Cowern *et al.* proposed that the static peak is associated with trapped non-substitutional B atoms and the diffused region is associated with electrically active substitutional B [Holland et al., 1988, Cowern et al., 1990].

Pelaz et al. used a combination of atomistic modeling and experimental observations to suggest a probable pathway for the BICs evolution, as shown in figure 2.13 [Pelaz et al., 1999]. The solid line suggests the evolution and dissolution path for the BICs based on a predominant high silicon interstitial content pathway. The proposed theory was supported by Mannino et al later by using an indirect experiment [Mannino et al., 2000]. A pre-doped B "box" shape marker layer grown by SPER was used as a detector for silicon implantation where the implanted ions are located at the left shoulder of the boron doped "box". During the annealing, the right shoulder of the box diffused due to TED as expected. However, the left site of the "box" profile was static due the B atoms being tied up in the form of BICs. Besides, theoretical studies of ab-initio calculations also support Pelaz's work [Pelaz et al., 1999].

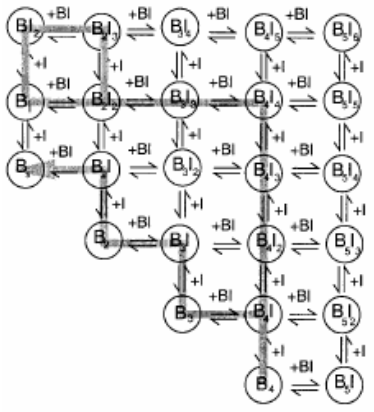


Figure 2.13: The reaction path suggested by Pelaz et al. for the formation of boron-interstitial clusters [Pelaz et al., 1999].

For other dopants such as As and P, their clustering mechanisms are via vacancy defects having configurations of As_nV_m and P_nV_m, respectively. It is noteworthy that the details regarding vacancy clusters have been obtained through

theoretical calculations and verified by simulation. However, the exact clustering pathways are not consensually well-established across the different dopant types.

2.7 Review of Various USJs Fabrication Techniques

The understanding of the underlying mechanisms and the effects of TED associated with dopant clustering are fairly important towards the formation of USJs. In this context, one would possibly optimize the properties of UJSs through the engineering of the implant generated-defects. In the following sections, the current status of USJ formation will be reviewed. Lenoable et al. published an excellent review on USJ formation techniques and the summary table from this article is being adapted here for the discussion, shown in figure 2.14 [Lenoble, 2006].

2.7.1 Standard Ion Implantation + Spike Annealing

The standard ion implantation combined with spike annealing has been used in the junction formation to sustain the downscaling of MOS device technology in last few decades. The success of this approach is due to its simplicity and flexibility. For instance, the desired shallow junction properties for device fabrication can be met by simply tuning the process parameters, such as implantation energy/dose and annealing temperature profile. However, the intrinsic limitation of low energy ion beam implantation (which has been discussed in section 2.4.1) prevents the as-implanted profile depth to go below 15 nm in the case of conventional B ions.

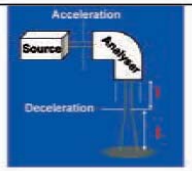
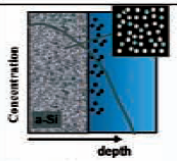
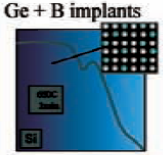
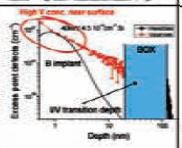
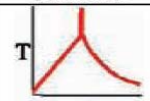
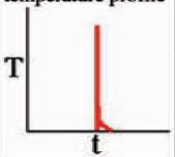
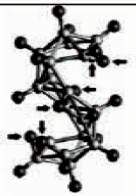
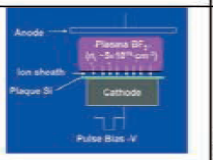
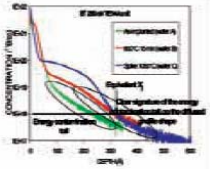
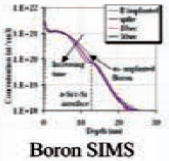
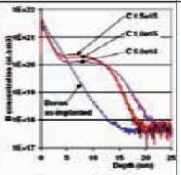
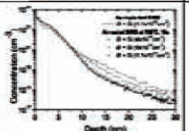
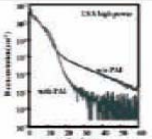
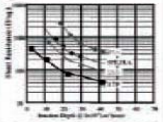
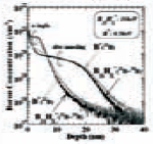
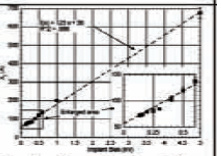
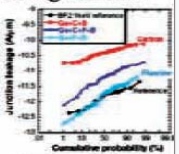
Process	ION IMPLANTATION	SPER	CO-IMPLANTS	VACANCY ENGINEERING	ADVANCED ANNEAL	CLUSTER IONS	PLAD
Description		 Ge + B implants  Anneal → crystal regrowth	Ge pre-amorphization + B or P + C + F implants	 Vacancy engineering schematic from [31]	 Flash anneal temperature profile  Laser anneal temperature profile	 Octadecaborane molecule ball and stick model. The dark spheres represent hydrogen atoms and the light spheres represent boron atoms [33]	
Results		 Boron SIMS profiles after SPER with self-amorphizing implants [13]	 Boron SMS profiles after annealing with C co-implants [11]	 Boron SIMS profiles after 700°C anneal [32]	 Boron SIMS profiles after LSA  R_s/X_j tradeoff [24]	 Boron SIMS profiles (as-implantd and annealed) B^+ vs $B_{18}H_x^+$ implants [33]	 As-implanted X_j vs bias  R_s/X_j after spike anneal
Advantages	Well-know technique Manufacturability control	Good R_s/X_j performance	Shallow X_j High activaton Standard ion implantation	Standard ion implantation Good R_s/X_j	Best R_s/X_j tradeoff	Standard ion implantation High throughput No X_j limitations	No X_j limitations Enhanced R_s/X_j No extended defects High throughput
Drawbacks	X_j limitations Low throughput for low-energy implants	Dopant deactivation Impact on dielectric reliability Extended defects distribution  picture from [13]	Cost (3 or 4 implants) Throughput Extended defects Leakage current:  data from [10]	Limited to SOI substrate Through the gate implants → dielectric reliability	New tool Circuit compatibility Residual defects  data from [30] Junction leakage Dielectric reliability	Specific ion source Impact of co-implanted hydrogen on NBTI? Impact on silicidation?	Technique and tool maturities Process control worse than standard implant process

Figure 2.14: Comparison of various USJs fabrication

Furthermore, significant B TED occurs during the spike annealing, and therefore the shallowest depth that can be achieved is around 20~25 nm, which only fulfils the up to the 90nm technology node MOS device.

2.7.2 Pre-amorphization Implant (PAI) and Solid Phase Epitaxial Re-growth (SPER)

Pre-amorphization implant (PAI) prior to doping and followed by solid phase epitaxial re-growth (SPER) is one of the favored techniques in today's USJ technology to avoid dopant channelling and to overcome the solid solubility limit of the dopant in crystalline silicon [Lindsay et al., 2002, 2003b]. Two pre-amorphization schemes have been commonly considered so far, (1) using inert ions such as Ge or Si for pre-amorphizing, and (2) using dopant as self-amorphizing.

One main disadvantage of this technique, however, is that it leaves a damage band just beyond the amorphous/crystalline (a/c) interface. Taking B dopant as an example, B-rich clusters form in the region of high B concentration near to the surface; and beyond the initial a/c interface the excess interstitials agglomerate into I-clusters, known as EOR defects, during the re-growth of the PAI layer. The interstitial supersaturation generated by the ripening and dissolution of EOR defects results in subsequent B TED and deactivation. In PAI USJs, the EOR defect band is located beyond the high-concentration B region, so that deactivation requires transport of interstitials from the EOR band towards the surface, forming the inactive BICs.

The physical basis for this technique is shown figure 2.15.

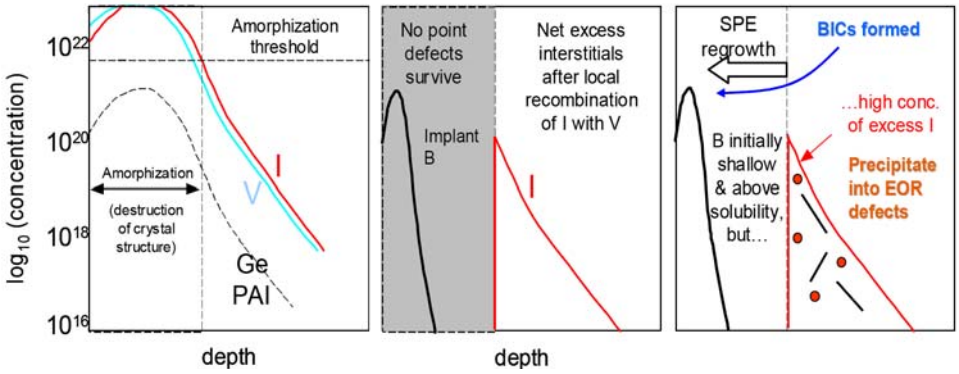


Figure 2.15: Schematic illustration of physics underlying for simulation of defect evolution and diffusion in the crystalline phase [Colombeau et al., 2004b].

The stability of the junction formed by this technique is of main concern since dopant deactivation arises upon subsequent thermal treatments (generally present after S/D junction formation). The deactivation phenomenon poses the main challenge in the device fabrication which imposes a very narrow thermal process window after the junction formation. Pawlak et al. reported the electrical and atomic stability of Ge-PAI B doped junction with its R_s as a function of isochronal annealing for this junction is shown in figure 2.16 [Pawlak et al., 2004]. The solid symbols demonstrate the effect of de-activation (increase in R_s) over varying amorphous thickness, while the open symbols represent the same conditions with additional F co-implant. It is also shown that when a pre-amorphized layer is just re-grown at low temperature (650^{o}C), high level of dopant activation is achieved and reflected by the low R_s value achieved. Applying a higher temperature treatment to the junctions causes the B to de-activate (increase in R_s), subsequently followed by a recovery in activation (reduce in R_s). These experimental observations are the result of interactions between the dopant atoms and silicon interstitials released from the EOR

region. This can be described in a physical picture. Upon annealing, the initial SPER process places the B atoms into the lattice sites, resulting in the formation of low R_s junction. At the same time, the excess of silicon interstitials at the EOR regions agglomerate into a band of extended defects. The further thermal cycle leads to the ripening-dissolution of the extended defects (interstitial clusters and {113} defects), causing a flux of interstitials flows towards the surface region which contains high concentration of B. The flux of interstitials will probably "kick out" some B atoms, and also interacts with B to form the BICs. Thereby, B deactivation is taking place which degrades the R_s of the junction (increase in R_s). Subsequently, the dissolution of BICs during extended thermal process leads to dopant activation recovery (lower in R_s) accompanied with the diffusion of B atoms (deeper X_j). The evolution pathway of this technique has been verified by quantitative modeling and simulation [Colombeau et al., 2004b]. In addition, the results shown by Pawlak et al. highlighted the dependence of dopant deactivation with respect to the depth of the amorphization in the substrate [Pawlak et al., 2004].

Another disadvantage of this technique lies in the residual extended defects located around the EOR region after being processed with thermal annealing. Lindsay et al. characterized the SPER junction device and showed strong degradation in current leakage attributed to the residual crystalline defects [Lindsay et al., 2004]. The residual 2D distributions of the extended defects induced by the Ge-PAI and SPER integration may also be very problematic to the gate dielectric reliability.

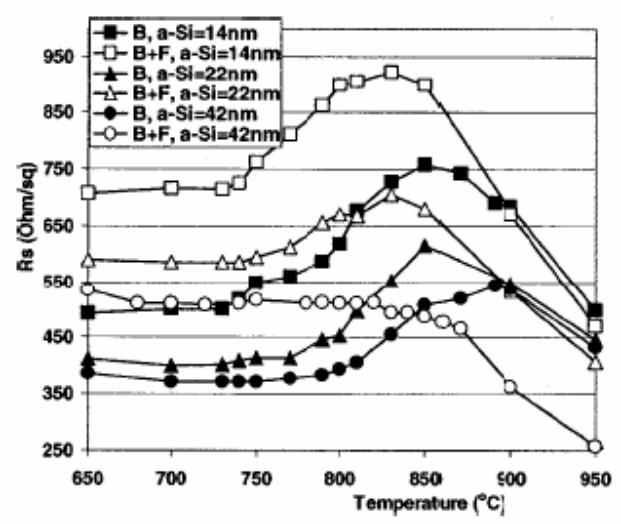


Figure 2.16: R_s as a function of 60s isochronal annealing from 650°C to 950°C. The solid symbols represent B implanted at 1.5 keV into varying amorphous layer thickness. Open symbols show the effect of 6 keV F co-implant [Pawlak et al., 2004].

2.7.3 Carbon/Fluorine (C/F) Co-implantation

The use of C and F co-implantation for USJ formation has been actively investigated recently. Significant improvements in reduced dopant diffusion and enhanced activation have been shown when the C/F co-implant is associated with pre-amorphizing implant (Ge or Si). Integration of such a technique in advanced MOS devices has been demonstrated to improve the short-channel effect and gain in device performance [Lenoble, 2006].

The basis of this technique is based on the SPER junction, where co-implant of C/F atoms is thought to be able to reduce the supersaturation of interstitials from the EOR defects (induced by PAI) towards the surface. The co-implanted impurity atoms trap or combine with the emitted silicon interstitials resulted from the

ripening/dissolution of extended defects during the thermal cycle. This was proven to be beneficial in suppressing the dopant de-activation that usually arises in the junction preceded with PAI.

B de-activation can be significantly reduced by optimizing the profile of F dopants in the amorphous layer (figure 2.16). It has been proposed that SPER of the amorphous layer enables the F atoms to form fluorine-vacancy (FV) clusters, which then traps the emitted interstitials from the EOR defect bands. There are also other experiments suggested that F atoms form B-F complex which can prevent boron diffusion and clustering with interstitials [Mokhberi et al., 2002a]. The B-F complex formation has been correlated to the degradation in R_s (increase in R_s value). More recent experimental data also showed the validity of the interstitial trapping mechanism by the FV clusters detected by the positron annihilation technique [Mubarek et al., 2004, Kham et al., 2005]. Cowern et al. used a combination of modeling and experimental results demonstrated that FV cluster is possibly induced and created during the SPER [Cowern et al., 2005a].

For the case of C, it has been well proven that it is a highly efficient medium in gettering of silicon interstitials and was even shown to inhibit the formation of extended defects [Wong et al., 1988, Souza et al., 2006]. However, it was determined that the C atoms must be initially located in the lattice substitutionally so that it can cluster with the silicon interstitials effectively, and hence suppressing the highly mobile BI pair formation (which is dominant mechanism in TED). Mirabella et al. suggested that high C concentration is required to restrict the left over silicon interstitials from the implantation [Mirabella et al., 2002]. Therefore, large amount of

silicon-carbon clusters are formed, which has been proven to have detrimental impact on junction current leakage in the devices. Furthermore, very high temperature annealing may lead to dissolution of these clusters, thereby the gain in TED suppression is significantly diminished [Ban et al., 1996].

C/F co-implant provides gains not only in junction depth but also to the electrical characteristics in terms of R_s value and dopant deactivation [Graoui et al., 2005]. Another important advantage of this technique is that it can extend the use of current equipment and processes. However, the physical limitation of lowering the ion beam energy of implantation is still a main issue for this technique, particularly when further scaling of ultra shallow junction is desired in the future technologies.

2.7.4 Vacancy Engineering

The main principle of vacancy engineering is to generate an excess of vacancies in the vicinity of the doping region via high energy co-implant process, typically preceding the desired dopant (B or P) implant. This technique differs from other competing approaches in that it eliminates the supersaturation of interstitials induced from dopant implantation via an interstitial-vacancy annihilation mechanism.

Raineri et al. studied the effects of high energy co-implant in relation to dopant enhanced diffusion [Raineri et al., 1991]. They applied a 1 MeV silicon co-implant followed by a B implant in bulk silicon substrate leading to the reduction in TED. Roth et al. and Venezia et al. used Silicon-On-Insulator (SOI) substrates to investigate a similar effect induced by high energy silicon co-implant. They studied

the origin of diffusion reduction by physically de-coupling the excess vacancies (near to surface) and interstitials rich (away from surface) regions (resulting from high energy co-implant) through what was thought as a diffusion barrier [Roth et al., 1997, Venezia et al., 1999]. Among their studies, the buried silicon oxide (BOX) layer in SOI structure was used to restrict the back diffusion of silicon interstitials to the top layer, leaving the top layer rich in vacancies, while majority of silicon interstitials are beneath the BOX layer. Much better B TED retardation was achieved as compared to the experiments performed by observed by Raineri et al. in bulk silicon substrate [Raineri et al., 1991]. An example (in figure 2.17) shows the simulated distribution of vacancies and interstitials after a 1 Mev, 1×10^{16} cm^{-2} silicon co-implant and annealing at 790^{o}C for 60s in the SOI substrate.

It was not until recently that vacancy engineering has been applied in the USJs. Shao et al. showed that not only improvement was observed in B TED, improvement in R_s was observed at low temperature annealing as well [Shao et al., 2004]. However, the resulting R_s was not able to rival with the current standard requirement. Vacancy engineering has also been examined by Larsen et al. and Saito et al. as highly efficient techniques in removing the EOR defects induced by PAI [Larsen et al., 1996, Saito et al., 1993].

To take the full advantage of this technique in SOI substrate, Smith et al. has recently proposed the use of vacancy generating implant to create rich vacancy concentrations in the active layer (the top silicon layer on BOX) [Cowern et al., 2005b]. It was indicated that the optimized high energy silicon co-implant has to avoid the full amorphization of the top silicon layer of SOI such that the highly

damage crystalline layer, rich in vacancies, remains as "seed" layer for SPER. The rich vacancy surface region is designed to annihilate the interstitial supersaturation induced by the subsequent low energy B implant. Excellent USJ characteristics were achieved such as "diffusionless" dopant profile and highly enhanced B activation level.

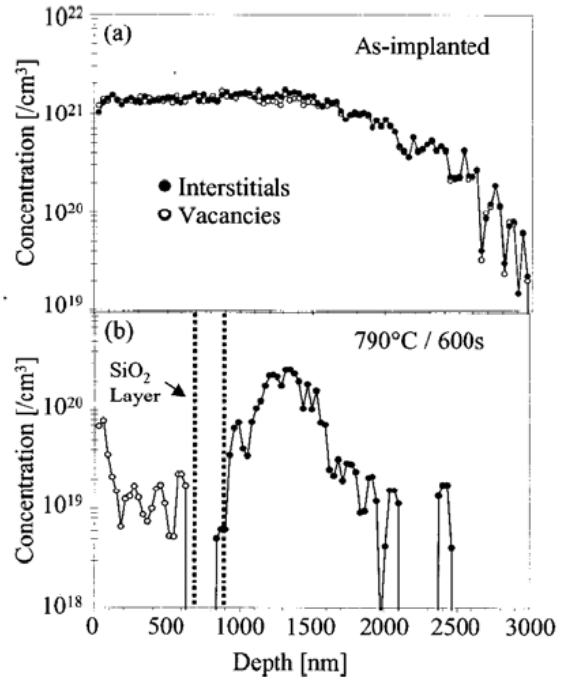


Figure 2.17: (a) Simulation of the interstitial and vacancy distribution created by a 1 MeV, $10^{16}cm^{-2}$ silicon implant. (b) Atomistic simulation of the defect distribution in part (a) after 790^{o}C anneal for 600s. Dashed line represents the position of the BOX [Venezia et al., 1999].

Therefore, optimized vacancy engineering is highly attractive since standard tools are sufficient to fabricate the USJs and no additional process step is involved. However, the reliability of the gate electrode and dielectric are affected since they are implanted with the high energy ions. So far this technique has not been

comprehensively demonstrated at the device level and it is also limited to SOI substrates [Lenoble, 2006].

2.7.5 Advanced Anneal Schemes

As it has been discussed in section 2.4.2, thermal annealing is applied to the implanted substrates for (a) repairing the defects created during the implantation and (b) activating the dopants for electrical conduction. It is during the thermal cycle that the excess defects evolve and the point defects interact with dopants resulting in undesired dopant enhanced diffusion and clustering.

The effect of anneal schemes has been extensively studied by a number of groups [Agarwal et al., 1999, Mannino et al., 2001]. It was shown that by increasing the peak annealing temperature, higher dopant solubility can be achieved while less transient phenomenon in dopant is observed. Another important feature was demonstrated on the ramping-rate, showing that faster ramp-up rate favors higher dopant activation and minimizes dopant diffusion. Generally, the principle of advanced annealing is based on the information and understanding acquired above. This can be seen from the transition of conventional spike annealing with soak time around 1s at maximum temperature, to 1ms for flash annealing and even shorter, (1μs) soak time, for laser annealing. In addition, both advanced anneal techniques use indefinite extreme rapid ramping rate, which is a few orders above the spike case. It is due to this ultra-short time high temperature scheme, the implant induced silicon interstitials saturate at very short times thus minimizing the point defect supersaturation and hence TED effect [Pelaz et al., 1999].

Excellent functional MOS devices with source/drain extension junctions activated with the advanced anneal techniques have been demonstrated in literature. However, it is difficult to integrate this method in the industrial process for some reasons. For instance, laser annealing imposes detrimental effects to the gate electrode [Okabayashi et al., 1980]. Cristiano also indicated that the thermal budget of advanced annealing is insufficient to remove the extended defects when amorphizing implants are associated in the junction [Cristiano, 2006]. Nevertheless, flash or laser is currently being used in the advanced technology process in complement with the spike annealing (additional thermal step on top of spike annealing) to enhance the dopant activation. In addition, due to the extreme high ramping rate properties, non-optimized flash/laser thermal profile will cause the substrates to experience highly thermal stress, and possibly leading to wafer warping or breaking during the processing [Wolf et al., 2000]. Careful optimization of laser or flash annealing condition is necessary for use in manufacturing production.

2.7.6 Cluster Ion Implantation

BF_2 cluster implantation has been used as one option to produce shallow junctions. Using this ion molecule as a doping source, the implantation energy can be relaxed up to 11/49 of the typical boron implant, which is scaled-up by the mass ratio of the molecule over the single boron atoms, M_{BF2}/M_B. Moreover, implantation of the heavy BF_2 cluster ions can result in self-amorphization at the surface of the substrate, and this is beneficial in suppressing the dopant tail channeling effect. The associated F was also shown to help in TED inhibition during the post-implant

annealing. But one of the main drawbacks is that the junction formed by BF_2 usually has high R_s due to retardation of dopant activation through the formation of B-F complexes [Colombeau et al., 2004]. Implanted profiles with depth less than 15 nm is inevitably the limitation of this ion source, where an acceleration/deceleration mode is required for implantation which inherently leads to undesired implant energy contamination.

Keeping in mind that those larger cluster ions will provide high mass ratio in relaxing the ion beam energy, $B_{10}H_{14}$ has been developed and used previously for shallow junctions. Unfortunately, the issues of stability, tuning procedure, and the dissociative nature of the ion, prevent this ion source to be considered seriously in manufacturing [Goto et al., 1996, Chong et al., 2000].

There has been renewed interest in using the $B_{18}H_{22}$ clusters ions recently after it was proven that the throughput of the beam has been greatly improved (scaled with equivalent beam current) [Jacobson, 2005]. As-implanted profiles with junction 10 nm are easily being fabricated without applying the acceleration/deceleration mode when performing the cluster implantation. The diffusion study showed that there is no particular impact of the co-implanted species in the post-annealed dopant profile and its electrical characteristics. In addition, fabricated devices with $B_{18}H_{22}$ implanted junctions revealed similar performance as compare to those obtained via B implants [Ishibasi et al. 2005]. However, no extensive study has been shown in the crystalline damages/defects generated by cluster ions. It is suspected that the resulting defects could be significantly different from the monomer dopant implants and this will impose detrimental effects to the junction electrical properties as well as the

contact formation process windows. Last but not least, considerations of ion beam tuning time, ion source lifetime, beam cleaning procedure, etc. should be carefully quantified.

2.7.7 Plasma Doping (PLAD)

Plasma doping (PLAD) or plasma immersion ion implantation has been studied extensively in late 1990s for the application in USJ formation [Felch et al., 1998]. The use of plasma in this doping technique enables an ultra-low energy implantation at a high beam current, leading to high doping dose rate and throughput. Junctions with high doping concentration and ultra-shallow profiles, in the region of sub-10 nm have been demonstrated. By using a BF_3 gas precursor, PLAD doping combining the spike can be used to fabricate advanced MOS devices at the 65 nm technology node [Lallement et al., 2004]. Lallement extends the application of PLAD association with advanced annealing, and his results revealed that extended defects induced by plasma doping can be removed by the thermal budget from both flash and laser annealing [Lallement, 2005]. The result was further verified by electrical junction study, in which same order of magnitude for junction current leakage was obtained as compared to the standard reference process. Plasma doping, however, suffers from energy and dose error due to the collisional charge exchange. The non-mass selective doping process can also induce ions and metal contaminants. Another main drawback is its restriction in normal angle doping, this prevents the plasma doping from the application in those implant steps which requires angle tilting, such as the Halo implant in the typical CMOS process flow. In addition, assessment of

process uniformity, reproducibility, dosimetry, multi-species/energy implants are also the main roadblocks for this doping technique.

2.8 Summary of Literature Study

The formation of USJs is one of the major barriers for device downscaling. It is now well-known that the typical doping process - ion implantation - induces silicon damages/defects which interact with dopant atoms during the thermal cycle (annealing). This causes the TED and clustering of dopants, inhibiting the formation of ultra shallow and highly active junctions. The configuration of defects and its evolution pathway play a significant role and it has been comprehensively described. Subsequently, the details of TED and the mechanisms involved in dopant activation and clustering have also been discussed to highlight the factors affecting these effects.

Lastly, different USJ fabrication techniques have been briefly reviewed. While these techniques have their own drawbacks as well, nevertheless, it is believed that these drawbacks are related to the defects induced during the processing of different approaches. In this work we seek to understand how the defects interact with dopants and use this information to optimize USJ fabrication techniques.

Chapter 3

Experimental Details and Techniques

3.1 Introduction

This chapter describes the experimental details used to obtain the data shown in subsequent chapters (Chapter 4 to 7). Procedures from the initial sample processing to physical and electrical characterizations are included. The theories behind the major experimental techniques are also briefly elaborated.

3.2 Sample processing and fabrication

3.2.1 Ion Implantation

Ion implantation is one of the key critical steps for impurity doping in semiconductor device processing and for sample fabrication. It offers great flexibility in the selection of the doping species as well as precise control in the spatial location and concentration of dopants, rendering ion implantation to be the method of choice in state-of-the-art CMOS integrated circuit fabrication. During the implantation, the desired doping atoms are ionized, accelerated in electric filed, mass analyzed and filtered before they penetrated into the silicon substrate. When entering the substrate material, the dopants will lose their momentum and energy before coming to rest at some depth through the interactions and collisions with host atoms of the target material. For instance, the crystalline nature of the silicon will be disturbed when dopants are implanted, causing damage or disorder in the silicon lattice in the form of

point defects (interstitials and vacancies). To achieve a conducting doped layer, a thermal treatment is required to return the crystal structure and activate the dopants by locating them into the substitutional sites in the crystalline silicon.

3.2.1(a) Ion Implanter

Ion implanter is traditionally classified based on the implant current or energy, such as Low-Current (LC), Medium-Current (MC), High-Current (HC), High-Energy (HE) and more recently the Ultra-Low-Energy (ULE) implanters. The LC implanters have beam current range less than 100 μA and are the early generation of implanters which are no longer used in production due to their low throughput. Under the optimum throughput, MC and HC implanters can offer a maximum implant energy between 200 and 400 keV, with dose range of 10^{10} ~ 10^{14} atoms/cm^2 for MC implanters whilst 10^{15} ~10^{16}atoms/cm^2 for HC implanters. HE implanters are systems used for deep energy well implant with the maximum singly charge ion energy can achieve higher than 1 MeV. On the other hand, the ULE implanters are designed for the USJ application purpose which offers single charged ion with energies as low as 100eV to a few keV.

The typical ion implanters generally consist of 4 components as depicted in figure 3.1, namely, (1) ion source chamber, (2) mass analyzing magnet, (3) acceleration / deceleration tube and (4) target chamber.

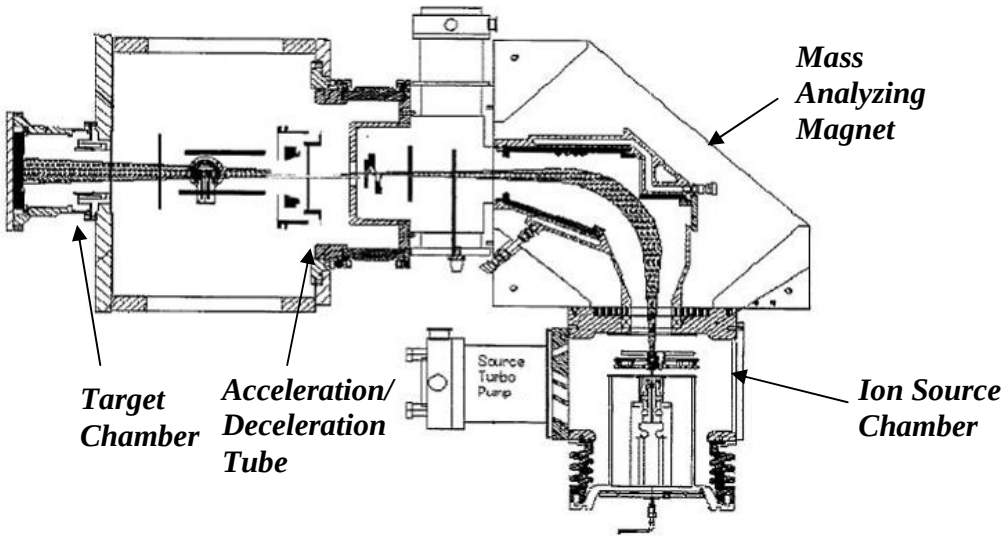


Figure 3.1: Schematic of a typical ion implanter with the main parts and components.

The ion implantation starts from the ion source chamber, where the ions of the desired element are produced from the gaseous or solid vapor source by sustaining the plasma. This is achieved by heating the tungsten filament through thermionic reaction, inducing electrons to drift through the source containing the desired atoms to be ionized. A potential is held at the end of the ion source chamber with an aperture to extract an ion beam with the desired ions.

Since the extracted ion beam will contain many species of ions, a mass analyzing magnet is used to filter the unwanted ions in the beam. Due to the varying charge to mass ratios, only desired ions are steered through the 90^{o} bend magnetic sector under the specified magnetic field.

After the mass selections, the ions are accelerated or decelerated under the influence of electric field to the desired velocity according to the implant energy. In some implanters, the ions are accelerated prior to the mass selection by magnetic field.

Also, deceleration mode is used for ultra low energy; however, it has been reported that the possibility of energy contamination is higher when deceleration is applied during the implantation [Yasunaga et al, 1999, Zhimin et al, 2003].

The ions eventually reach the target chamber, where the target substrate is mounted. The ions can be introduced into the substrate via electrostatic scan or mechanical scan. It is found that the mechanical mode offers better uniformity in doping with only 1% of variation. Parameters such as substrate temperature, tilt and twist angles can be adjusted in the target chamber.

The implantations in this work were performed by following 3 implanters:

(1) Varian VIISta 80HP high current ion implanter

(2) AMAT Quantum XR80 Leap high current ion implanter

(3) Axcellis GSD Ultra high current ion implanter

3.2.1(b) Ion Range Distributions

As mentioned earlier, the implanted ions penetrate into the target materials and lose energy while colliding and interacting with the host and neighboring atoms. These ions are indeed traversing in a random path but eventually resulting in spatial distribution of dopants depending on the ion species, energy and total dose. The total length of the ion trajectories in either lateral or vertical movement is defined as the range, R; while the average path of the implanted ions is called as the projected range, R_p. [use subscript for 'p'] The difference between the R and R_p of ions is illustrated in figure 3.2.

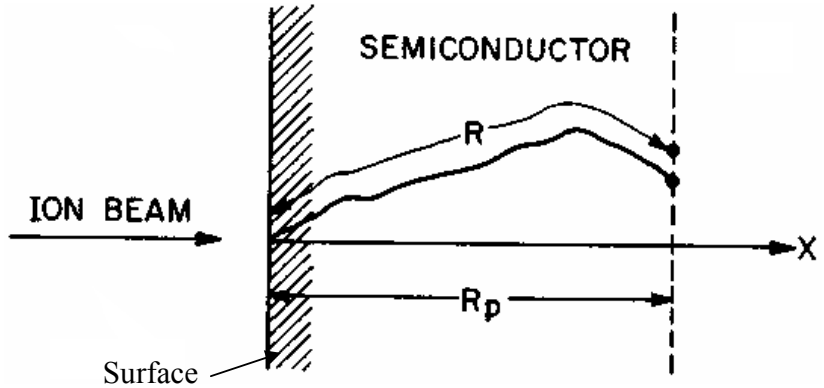


Figure 3.2: Schematic diagram showing the total path length (R) and projected range (R_p) of the implanted ions.

The distribution of implanted ions around the R_p can be approximated mathematically by Gaussian distributions with standard deviations of σ_P and σ_T which accounts both vertical and lateral motions of the ions respectively. The schematic of the Gaussian curve with the parameters are shown in figure 3.3.

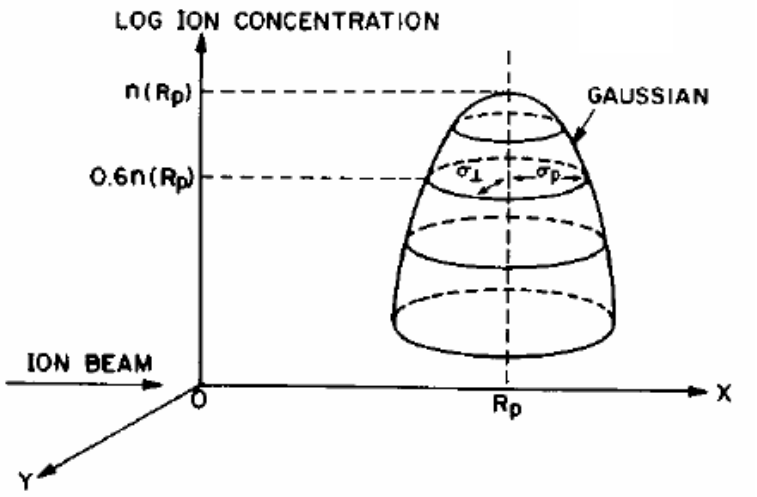


Figure 3.3: Schematic view of ion distribution representation in terms of Gaussian distribution and the associated parameters.

When the distribution of ion profile is far for any mask edge, the lateral motion in the y-axis can be neglected, and hence ion concentration at distance x from the surface can be expressed as:

$$n(x) = n_o \exp\left[\frac{-(x-R_P)^2}{2\sigma_P{}^2}\right] \qquad \text{Eq. 3-1}$$

where n_o is the peak concentration of the ions. If the total dose is Φ, then integrating equation 3.1 gives an expression for peak concentration (n_o):

$$n_o = \frac{\Phi}{\sqrt{2\pi}\sigma_p} \cong \frac{0.4\Phi}{\sigma_p} \qquad \text{Eq. 3-2}$$

Therefore, ion concentration in equation 3.1 can be evaluated when the total implanted dose is known:

$$n(x) = \frac{0.4\Phi}{\sigma_p} \exp\left[\frac{-(x-R_P)^2}{2\sigma_P{}^2}\right] \qquad \text{Eq. 3-3}$$

An arbitrary ion distribution can be characterized in terms of its moments. So far, two moments, both the projected range R_p and the standard deviation σ_P are used to approximate the ion profile with Gaussian curve. To have a more accurate estimation of ion profiles, it would be better to use a more distorted Gaussian distribution (Person IV), which uses 4 moments. For instance, the skewness and kurtosis are the additional moments used to account the asymmetry of the distribution, while the kurtosis is used to estimate the 'flatness' at the top of a distribution [Sze, 1998]. The approximation of the ion distribution is generally used to provide a quick prediction and insight of how the ion distributes in the material after implantation. However, a physical Secondary Ion Mass Spectroscopy (SIMS) characterization (to

be described in section 3.3.1) will be required and more appropriate if information about the actual ion distribution is highly desired.

3.2.2 Annealing

Annealing is a thermal process that serves to repair the damage resulted from ion implantation and to electrically activate the dopants in the crystalline structure. The non-repair implant damage would cause degradation in mobility and high current leakage, while a small dopant activation level would lead to a lower current conduction, affecting the off and on-current of the devices eventually. Therefore, the quality of the thermal annealing with appropriate thermal budget (combination of time and temperature) is very crucial in the device fabrication especially on the USJ formation. Three different types of annealing were employed here:

3.2.2(a) Soak Annealing

Soak annealing is used to study the junction stability in this thesis. Samples were isochronally annealed by Uniaxis Addax XM80 rapid thermal annealer (RTA) with the temperature ramp-up and ramp-down rates of 60^{o}C/s and 45^{o}C/s, respectively. The rapid heating is accomplished by two banks of halogen-quartz lamps above and beneath the quartz wafer holder, as illustrated in figure 3.5. The cooling process involving pumping of compressed air and supplying of cooling water that calculate around the anneal chamber.

A 8” inch blanket silicon wafer is used as a support to anneal the sample pieces. Prior to annealing, the chamber is pumped down to 1 mbar followed by

constant injection of nitrogen flow into the chamber, providing a clean and inert environment during the anneal cycle. This can also reduce the chances of sample oxidation due to the moisture.

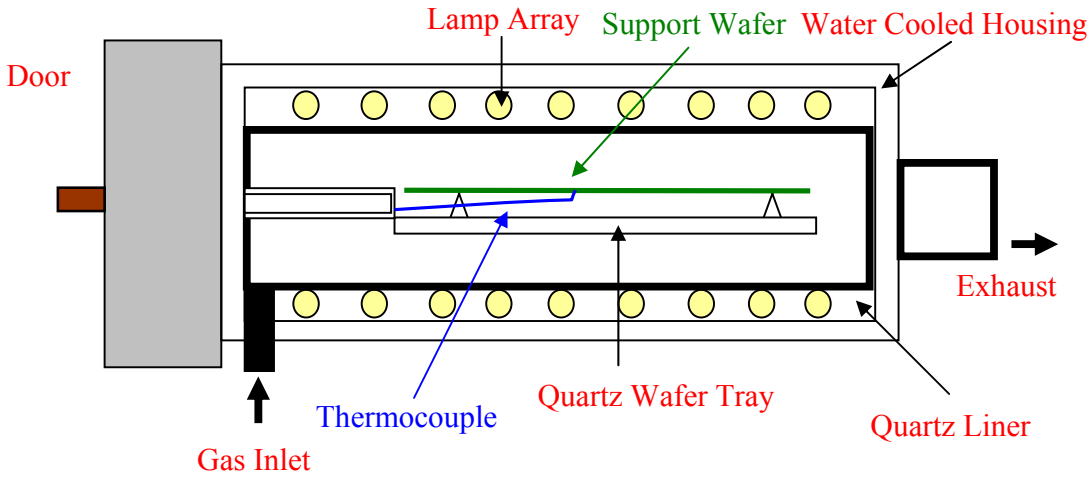


Figure 3.4: Schematic diagram of the Uniaxis Addax XM80 RTA chamber associated with all the key components.

The substrate temperature during the anneal cycle was measured and monitored by using the K-type thermocouple which is contacted underneath of the support wafer. A real-time feedback of the support wafer temperature to the RTA controller is used for the heating lamp power adjustment, so that the thermal cycle would be able to follow the pre-set desired anneal temperature and duration. To maintain the high repeatability of the annealing cycle, the thermocouple is changed in every 200 runs and the temperature calibration is performed once in every 3 months.

3.2.2(b) Spike Annealing

Spike annealing is a thermal process similar to the soak annealing since both of them are performed in the RTA system. However, spike annealing does not have a holding time at the peak temperature and it is associated with a much higher ramping-up rate, 100^{o}C/s ~ 400^{o}C/s. Therefore, it is a relatively low thermal budget process, which can reduce the TED effect and yet maintain the high dopant activation level in the junction attributed to its high peak temperature. Due to above benefits, the spike thermal cycle has been commonly in 0.13μm or more advanced technology node process flow.

In a typical spike annealing thermal profile, a pre-stabilization annealing is involved before its rapid ramp to the desired set point temperature. This is because a rapid heating with a large temperature gradient can cause wafer damage in the form of slip dislocations induced by the thermal stress. In addition, the uniformity of the doping across the whole wafer will also be degraded if thermal transient difference is too big. On the other hand, it has also been shown recently that ramp-down rate in spike annealing, typically between 70-90^{o}C/s, has limited the gain in further increase of ramping-up rate in the thermal profile [Agarwal et al, 1999]. Two RTA systems were used to perform the spike annealing for the samples in this work:

(1) Applied Vantage Radiance RTA system

The ramp-up rate for the pre-stabilization step was 60^{o}C/s. The pre-stabilization is performed at 650 °C for 10 s followed by a temperature spike with a ramp-up rate of 250^{o}C/ s. The peak temperature of the spike anneals was set to 1080 °C. The ramp-

down is 75°C/s. Annealing was performed in a chamber flushed with 100ppm oxygen in nitrogen ambient at atmospheric pressure.

(2) Mattson 3000 Plus RTA system

The ramp-up rate to the pre-stabilization step was 50 C/ s. The recipe includes pre-stabilization at 650 °C for 10 s followed by a temperature spike with a ramp-up rate set to 250°C/ s. The peak temperature of the spike anneals was 1080 °C. Annealing was also done in the 100ppm oxygen in nitrogen ambient at atmospheric pressure. The ramp-down is 75°C/s.

3.2.2(c) Flash Annealing

Flash lamp annealing (FLA) has been considered as one potential candidate in forming the USJ. This is because it can perform the thermal annealing in millisecond duration with extremely high temperature as compared to the conventional RTA soak and spike annealing [Yoo et al., 2005, Lerch et al., 2005]. In addition, FLA is a lamp based thermal process, the entire wafer can be annealed at the same time as compared to the raster scans is required to cover the whole wafer area used in laser annealing. Hence, FLA has absolute advantages in terms of better uniformity and higher productivity.

Flash annealing is typically carried out after a pre-stabilization thermal step similar to the case of spike annealing, avoiding the wafer deformity or defect introduction due to the excess thermal stress. In the initial phase of FLA cycle, the backside of the wafer is heated up to an intermediate temperature and held for a few tens of seconds. It is then followed by the exposure of front side of the wafer to the

flash or arc lamp to increase the substrate surface to a high temperature within milliseconds. The millisecond annealing is achieved by discharging a capacitor bank into the flash lamp [Jones et al., 2003, Jain et al., 2005]. Figure 3.5 shows the schematic of a FLA tool with a hot chuck used to heat-up the substrate up to the pre-stabilization temperature. Recently, a novel flash tool, known as flash-assisted RTP system, has also been developed. This tool combines both the spike and flash anneals into a single thermal cycle and was claimed to offer improved thermal budget for USJ formation.

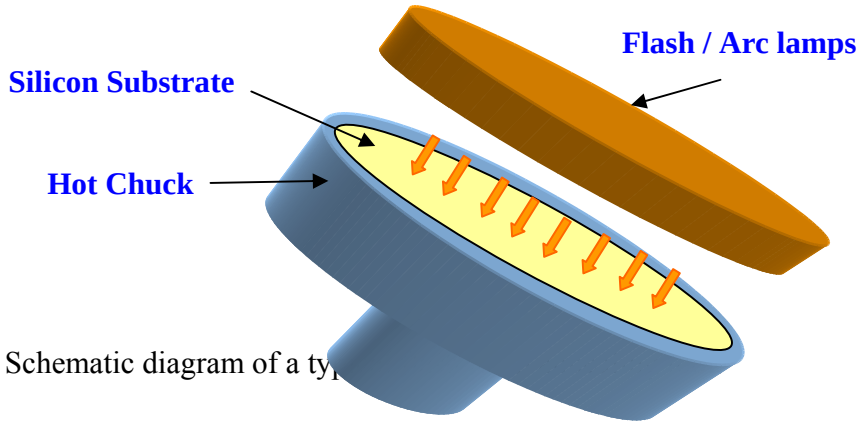


Figure 3.5: Schematic diagram of a ty

The flash annealing tool used in chapter 6 is Dainippon Screen LA-3000-F flash lamp annealer system. During the anneal process, the backside of the wafer was raised to the intermediate temperature of 500^{o}C using a hot chuck, while wafer surface was exposed to the Xenon flash pulse with an intensity of 26J/cm^{2} in the N_2 ambient. The peak wafer surface temperature under the flash pulse was estimated to be around 1150^{o}C ~ 1200^{o}C with a pulse duration of 0.8ms.

3.2.2(d) Ultra-High Vacuum(UHV) Soak Annealing

Ultra-high vacuum soak annealing was used to study the surface effect on the pre-amorphized B junction formation (described in Chapter 7). The annealing was carried out in an in-house built UHV chamber (in Roger Adams Laboratory at University of Illinois at Urbana Champaign – figure 3.6), which using Ta clips for resistive heating. Heating was performed in a turbo-molecularly pumped high vacuum chamber with a working pressure maintained around 10^{-8}~10^{-9}torr to prevent formation of native oxide and contamination of the surface. Temperature was monitored with a chromelalumel thermocouple spot welded to the Ta foil adjacent to the edge of the Si specimen, while the surface condition was measured by Auger electron spectroscopy (AES) which is attached to the chamber. The annealing conditions can be performed in the range of 500^{o}C to 1300^{o}C.

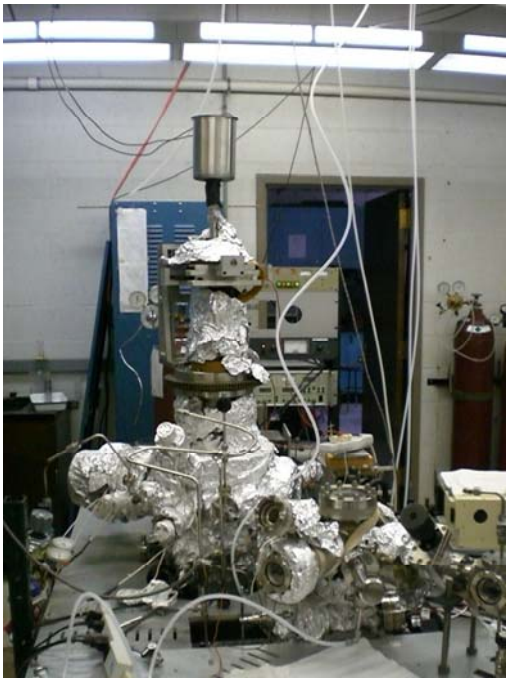


Figure 3.6: In-house built ultra-high vacuum chamber in Roger Adams Laboratory at University of Illinois at Urbana Champaign.

3.2.3 Diode and Transistor Fabrication

The p+/n diodes of some B doped junctions in this work are used to investigate their current leakage behavior at the reversed biased condition. The diodes were fabricated using a simple circular contact mask and lithography step to form the circular silicon islands which surrounded by SiO_2. Nickel silicidation (~10nm) was used to form the front contact of diode, whilst aluminum (~300nm) was deposited at the back of the subtracted to form the ohmic back contact. The schematic diagram of the diode layout is shown in figure 3.7.

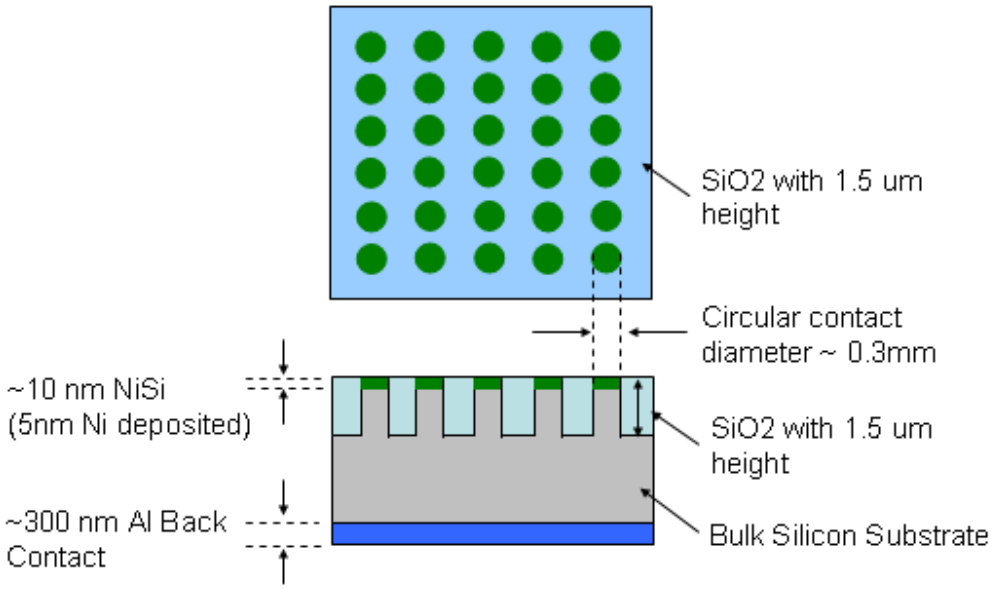


Figure 3.7: The top and cross-sectional view of the diode layout.

On the other hand, PMOS devices were employed in chapter 4 to study the impact of the proposed USJ on electrical performance. These transistors were fabricated by following to the 65nm high performance CMOS process flow.

3.3 Physical Characterizations

3.3.1 Secondary Ion Mass Spectrometry (SIMS)

Secondary Ion Mass Spectrometry (SIMS) is an analysis technique widely used to analyze the traces of elements in solid substrates. The SIMS technique can be generally classified to two major modes based on their sputtering rate, namely the static SIMS and dynamic SIMS. The static SIMS uses extremely slow sputtering rate, at which less than a tenth of an atomic monolayer is consumed during the entire analysis and is generally useful for identifying molecular species. On the other hand, dynamic SIMS is an analysis with sample surface continuously being sputtered away to generate changes of the ion count intensity as a function of depth, also designated as depth profiling. The latter is the SIMS technique which is extensively used in this thesis to gain more physical picture of the atomic information of the junction.

The basic principle of dynamic SIMS is an application of primary ion beam to bombard a sample surface, generating secondary ions analyzed by mass spectrometer in measuring its lateral distribution of elements in the samples. The primary beam energies are typically between 0.5 to 50 keV and directed to sample surface in the incident angle range of ~ 45^{o} to 90^{o}. When a surface receives the bombardment of ions, energy is transferred from the primary ions to the target atoms causing recoil of host atoms in a series of binary collisions. Fraction of the recoiled atoms may gain enough momentum to overcome the surface binding energy and sputter off from the surface along with electrons and photons. The sputtered particles, also known as secondary particles, can carry negative, positive or neutral charges. Figure 3.8 shows the schematic of the sputtering by primary beam and the generation of sputtered particles.

Among the sputtered particles, only the ionized state secondary particles are indeed involve in the mass spectrometry analysis. The ionization efficiency is also known as ion yield, defined as the fraction of sputtered atoms that become ionized. Ion yield can vary a few orders of magnitude with respect to the elements. It is also found that the ion yield is playing a key role if a good quality of depth profile can be obtained from the SIMS. One key factor affecting the ion yield is the primary ion species, typically consists of O2+, Cs+, Ar+, and Ga+. For instance, the O2+ offers better positive ion yields, while the Cs+ increases the yield of negative ions. Despite the beam species, optimization of other primary beam conditions such as beam energy, incident angle, etc, are also necessary for obtaining the optimum high resolution dopant profile. In addition, some of the instruments are also equipped with secondary ion post acceleration system for enhancing the electron multiplier signals at low primary ion energies used in the analysis of USJ.

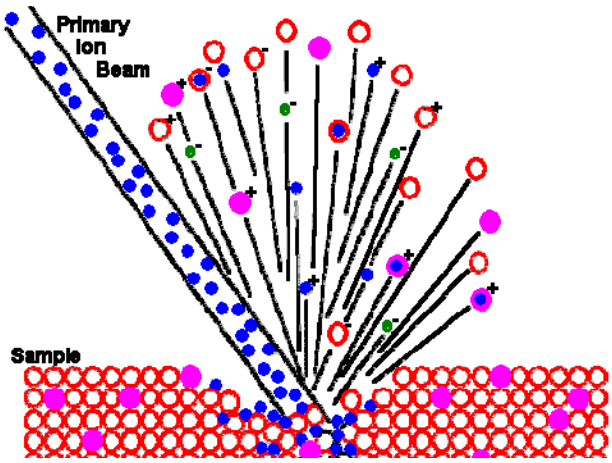


Figure 3.8 Schematic showing the sputtering of sample by primary beam associated with the generation of secondary particles.

Although SIMS is a high resolution technique which can provide a detection limit up to $1x10^{12}$~$1x10^{16}$ atoms/cm^3, there are certain effects induced during the analysis. It can lead to artifacts in the measured dopant distributions profile. Following are a few possible effects:

1) Elemental interference when an isotope of one element has the same nominal mass as an isotope of another. This results in higher concentration of the analyzed element than the real value in the sample.
2) Variation of sputtering rate in multilayer materials with different density. This leads to errors in the depth calibration.
3) Sample charging when a net electric current is buildup at the sample surface. It changes the energy distribution of the secondary ions and hence affects their transmission and detection by the mass spectrometer.
4) Mixing and redistribution of sputtered ions with the ions from underlying later, it causes inaccuracy of dopant concentration profiling across the depth.

Therefore, understanding of the sample nature and configuration are necessary prior to the analysis, so that precautionary steps can be taken care for choosing the optimum analyzing condition.

Figure 3.9(a) shows the raw data for the measurement of a boron implanted silicon at 1keV to a dose of 1×10^{15} cm^{-2}. The analysis uses the O2+ primary ion source at net energy of 500eV and measures the positive secondary ions (IE). During the analysis, the ion count rate of ^{11}B is monitored as a function of time.

To convert the time axis into depth, a profiler-meter was used to measure the crater depth by dragging a stylus across the crater and noting the vertical deflections

between the sputtered and non-sputtered region. Then the measured total depth is divided by the total sputter time to obtain the average sputter rate. Tencor Alpha-Step 500 profiler-meter was used throughout this thesis.

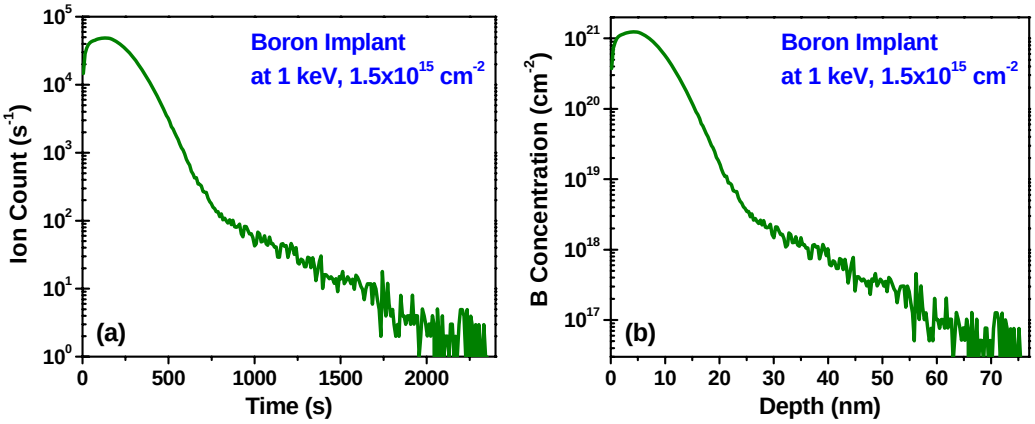


Figure 3.9 Example of B SIMS raw data conversion from (a) ion count/time dopant profile to (b) concentration/depth dopant profile using a constant sputter rate to determine the depth, and a RSF value to convert the secondary ion count to concentration.

The ion count in the vertical axis, is converted to the concentration (CE) by the Relative Sensitivity Factor (RSF) using the following expression:

$$C_E = RSF \times \frac{I_E}{I_{ME}} \qquad \text{Eq. 3-4}$$

$$RSF = C_{ER} \times \frac{I_R}{I_{MR}} \qquad \text{Eq. 3-5}$$

where RSF Relative sensitivity factor based on reference sample

I_E Secondary ion intensity for desired element E in analyzed sample

I_R Secondary ion intensity for E in reference sample

I_{ME} Secondary ion intensity for matrix element (Si) in analyzed sample

I_{MR} Secondary ion intensity for matrix element (Si) in reference sample

C_E Concentration of E in analyzed sample

C_R Concentration of E in reference sample (known)

In order to obtain a more accurate RSF value in this work, a reference sample with known atomic concentration was run prior to analysis, instead of referring to the standard RSF tables [Cameca, 2008]. This is because ion yield highly depends on the analyzed elements, the sputtering species and the sample matrix. For the case of B, an epitaxial grown uniform straight line B profile at 1.2×10^{19} atm/cm^{-3} was used, while as-implanted C/N/F profiles, with known implant dose, served as the standard for their respective annealed profiles. The standard sample was run once in every batch of samples to accommodate the errors due to the fluctuation of the beam condition. The calculated RSF value for the B profile in figure 3.9(a) is 1.28×10^{23} cm^{-3}, and the matrix current is (IME) is 3×10^{8} ions/s. With these values together with the average sputter rate calculated earlier, the ion count versus time plot can be converted to the dopant concentration profile as a function of depth illustrated in figure 3.9(b).

The SIMS analyses in this thesis were carried out with different machines. However, the analysis conditions, such as the ion beam species, ion beam energy, beam incident angle, scan area, etc were optimized according to the nature of the sample as well as the desired element for profile. The experimental samples were characterized in batches for comparison within a study topic to minimize errors. The SIMS tools used for this work are as following:

(1) Cameca IMS 6f at Physics Department, National University of Singapore

(2) Cameca IMS Wf / SC Ultra at Chartered Semiconductor Manufacturing, Singapore

(3) Cameca IMS 5f at Center for Microanalysis of Materials, University of Illinois At Urbana-Champaign

The details of analysis conditions will be specified in each chapter.

3.3.2 Transmission Electron Microscopy (TEM)

Transmission Electron Microcopy (TEM) is a powerful technique used to image the structures and materials in nano-range. The basic principal of TEM analysis is bringing a beam of accelerated electrons into focus, so that it can transmit through a sufficiently thin specimen. Part of the transmitted and forward scattered electrons may form the diffraction pattern based on the crystallography of the samples in the back of the focal plane and projected in the image plane. Bright field, dark field, and high resolution TEM (HRTEM) are the 3 different major imaging modes in TEM. Images formed with only the transmitted electrons are bright field images, while images formed with a specific diffracted beam are dark field images. HRTEM gives extremely high resolution down to ~0.08 nm, hence it can be used for interface analysis and the characterization of structural information on atomic size level.

In order to get a high quality image, sample preparation is a pivotal part of the TEM analysis. It is well-known that ever thinner TEM specimens are desired while keeping the damage to an absolute minimum to prevent any changes in its structure and chemistry. Generally, 50 ~ 100nm thick specimens would be considered as reasonable thickness for TEM electron beam to pass through. There are different methods for the TEM sample preparations, such as mechanical polishing (wedge and dimpling), chemical etching, microtome preparation and focused ion beam (FIB). The choice of preparation depends on the material characteristics and the information

desired. Both mechanical polishing and FIB are employed in this work to prepare the various TEM specimens.

In this thesis, the TEM analyses were carried out by JEOL 2100 TEM and Philips Tencai F20 TEM with 200keV acceleration voltage and 0.2 – 0.15nm focused spot size. The cross sectional image XTEM were performed under bright field with multiple beam mode, and used to characterize the extent of amorphization due to the implantation and the evolution of silicon damages/defects after thermal annealing.

3.3.3 Atomic Force Microscopy (AFM)

Atomic Force Microscopy (AFM) was used to scan for the surface morphology of the annealed samples. In chapter 7, for instance, AFM scans were performed to study the impact of surface treatment with HF solvent to remove the native oxide and thus creating the atomically clean surface. All the images were obtained under tapping mode by using a monolithic silicon tip and the scan rate set within 1.0 Hz to 1.8 Hz without inducing destructive friction forces. In addition to the topography image, vertical distance profile and root-mean-square (RMS) roughness value was obtained. For instance, the RMS roughness of a given area can also be estimated from:

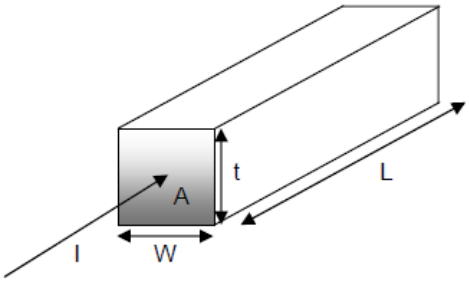
$$Ra = \frac{1}{L_x L_y} \int_0^{L_y} \int_0^{L_x} |F(x,y)| \, dx \, dy \qquad \text{Eq. 3-6}$$

where the L_x and L_y are the dimensions of the surface while F(x,y) represents the surface relative to the center plane. The machine employed was Nanoscope III Atomic Force Microscope provided by Veeco Metrology Group.

3.4 Electrical Characterizations

3.4.1 Four Point Probe Measurement (4PPT)

The resistivity is a key parameter for semiconductor material since it can be related directly to the impurity content or the conductivity of a thin film or bulk material. The resistivity (ρ) can be correlated to the resistance (R) of a uniformly doped block shown in figure 3.10 as following:



$$R = \frac{\rho \times L}{A} = \frac{\rho \times L}{W \times t}$$

Figure 3.10: Schematic of a uniformly doped block associated with the various dimensions. The equation of resistance (R) is shown on the right.

Since the dimensions of the sample is necessary to obtain the R, another parameter, known as sheet resistance R_s has been defined for the ease of representation, which requires the information of thickness only. The R_s of a sample is the R per unit square and inversely proportional to the thickness:

$$R_S = R \times \frac{W}{L} = \frac{\rho}{t} \qquad \text{Eq. 3-7}$$

where R_s Sheet resistance (Ω/)

R Sheet resistance (Ω)

ρ Resistivity (Ω-cm)

W Width (cm)

L Length (cm)

t Thickness (A)

Four point probe (4ppt) is a quick and simple technique widely used for measuring the sheet resistance of a sample. The configuration of a typical 4ppt is depicted in figure 3.11 with 4 needle probes and spacing S. Typically, I is the current carried through the outer of the two contacts (1 and 4) into the sample, whilst the V is potential difference measured across the inner contacts (2 and 3).

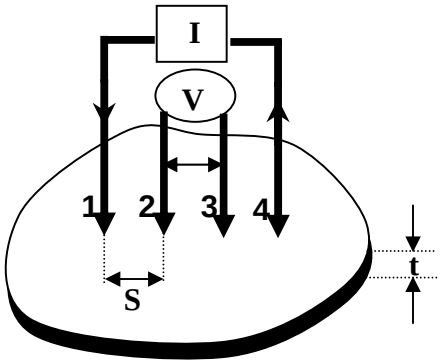


Figure 3.11: Schematic of the standard 4 point probe technique measuring the sheet resistance (R_s) of a semiconductor substrate with thickness "t".

The R_s value of the measured sample can be obtained with this equation:

$$R_S = \frac{\rho}{t} = C_{F1} C_{F2} \frac{V}{I} \qquad \text{Eq. 3-8}$$

where V Voltage across probe 1 and 3 (V)

I Current across probe 1 and 4 (A)

C_{F1} Correction factor 1 to account the geometry and size of the sample

C_{F2} Correction factor 2 to account t/s ratio dependency of the sample

It can be clearly noticed from the equation 3-8, the correction factors (C_{F1} and C_{F2}) are associated with the measured voltage and current to calculate R_s of the sample. C_{F1} is the factor that corrects geometry, shape and size of the sample and C_{F2} is a constant taking account of the correction for the ratio of sample thickness to

probe spacing. With the appropriate correction factor values, 4 ppt can be used to measure any sample with arbitrary dimensions. Nevertheless, R_s measurement can be further simplified with a constant correction factor value of 4.4515 (C_{F1} x C_{F2}) when probe spacing is much larger than doping thickness, S>>t ($t \leq 50$ nm) and size of the sample is reasonable big (>10 x 10 mm) [George Tech, 2008].

The instrument used in this work was the 100g light weighted probe head standard 4 ppt system with a probe spacing (S) of 1mm. For accurate reading the probe head was placed at the centre of sample with dimensions of 20 x 20mm. The absolute R_s for each sample is obtained by averaging the multiple measurements (>5 times). In some sample sets, the measurements were carried out with more than one 4ppt system at different laboratories to ascertain the error range.

3.4.2 Hall Effect Measurement

The Hall effect measurement has gained popularity for the electrical measurement of extrinsic semiconductor in recent years. This is because the Hall technique can be used to determine directly the free carrier type and density, electrical resistivity as well as the carrier mobility in the semiconductor materials.

The Hall effect is working with the basic physical principle of Lorentz force governed by following equation:

$$F = e (V_d \times B) \qquad \text{Eq. 3-9}$$

This force is experienced by the electron when moving along a direction perpendicular to an applied magnetic field. The electron will move in response to the force (F) with a drift velocity (V_d) under the effect of internal electric field.

Figure 3.12 shows a schematic of an n-type, bar-shaped semiconductor in the presence of a magnetic field B and current I being applied on it. The free carriers, electrons, move in the opposite direction of current flow subjected to a force to drift them towards the negative y-direction. This leads to an excess surface charge on the side of the sample, generating the voltage potential drops across the y-direction of the sample which is known as Hall voltage (V_H).

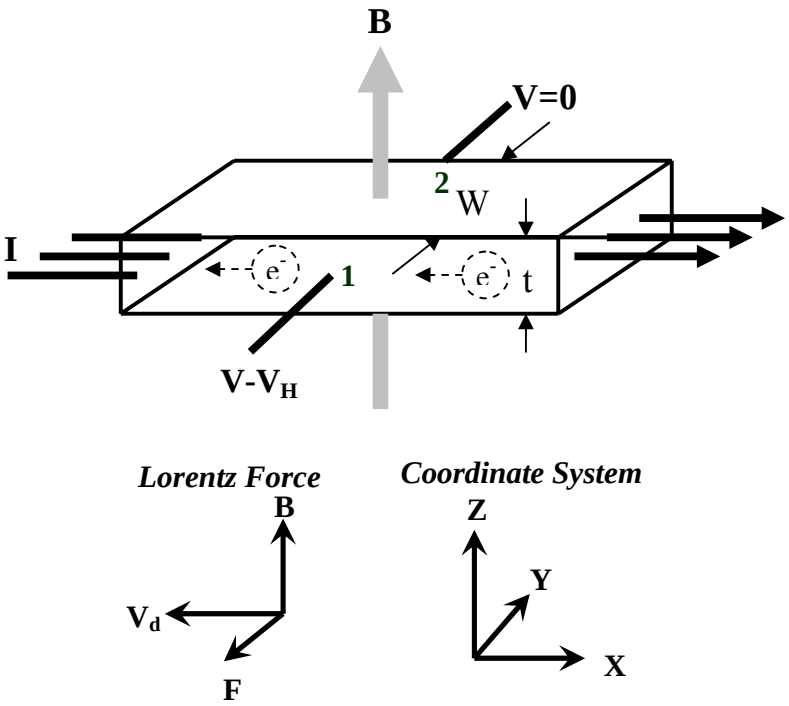


Figure 3.12: Schematic representation of the Hall effect on a bar-shaped n-type semiconductor with magnetic field (B) and current (I) being applied on it.

To calculate the sheet carrier concentration (N_s) and Hall mobility (μ_H), it is necessary to obtain the Hall coefficient (RHs) from the measured V_H. Following are the relations used:

$$RHs = \frac{V_H}{I \times B} \qquad \text{Eq. 3-10}$$

$$Ns = \frac{r}{q \times RHs} \quad \text{Eq. 3-11}$$

$$\mu_H = \frac{RHs}{Rs} \quad \text{Eq. 3-12}$$

$$\mu_C = \frac{\mu_C}{r} = \frac{RHs}{r \times Rs} \quad \text{Eq. 3-13}$$

where RHs Hall Coefficient (m^2C^{-1})

V_H Hall voltage (V)

I Applied current (A)

B Applied magnetic filed (T)

N_s Carrier density (at/cm^3)

r Hall scattering factor

q Elementary charge ($1.602\times10^{-19}C$)

μ_H Hall mobility ($cm^2V^{-1}s^{-1}$)

μ_C Conductivity mobility ($cm^2V^{-1}s^{-1}$)

R_s Sheet resistance (Ω/sq)

As shown in equation 3.11, a parameter "r" which is the Hall scattering factor is needed to be specified to determine the N_s value. This factor is to take in account the scattering of carriers caused by the magnetic field which involving complicated scattering mechanisms. In addition, the same scattering factor "r", is also used to convert the Hall mobility μ_H to the true conductivity mobility μ_C in the material in equation 3.13, due to the presence of magnetic field in the measurements. For a B concentration of $5x10^{17}cm^{-3}$ sample, r~0.8 has been reported and applied for the calculation [Collart et al., 1998]. In other studies, the value of r is tends to approach 1 for B concentration > $1x10^{18}cm^{-3}$ [Johansson et al., 1970, Mitchel et al., 1982]. Since

most of the samples in this work have concentrations a few orders higher than $1x10^{18}cm^{-3}$, a unity Hall scattering factor has been assumed.

On the other hand, sheet resistance R_s is also required to obtain prior to the calculation of mobility value. Instead of measuring it with 4ppt, the R_s can be obtained using the Van der Pauw technique directly with the Hall setup, at which four ohmic contacts being formed along the perimeter of the sample with arbitrary shape as illustrated in figure 3.13.

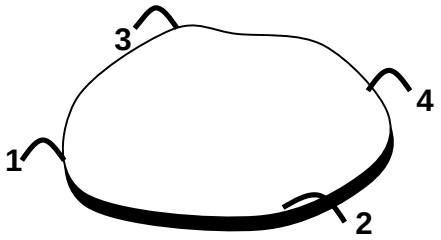


Figure 3.13: Schematic of an arbitrary shape sample with four contacts that satisfies the Van der Pauw requirements.

The R_s values can be measured by applying a current to 2 contacts and then noting a voltage across two others. The measurement is also repeated with switching the contacts to determine the R_s with following expression:

$$\exp\left(-\frac{\pi}{R_S}R_{34,21}\right)+\exp\left(-\frac{\pi}{R_S}R_{42,13}\right)=1 \qquad \text{Eq. 3-14}$$

which $R_{34,21}$ is determined by applying a current through contact 3 and out of contact 4 (I_{34}) and measuring the voltage across contacts 2 and 1 (V_{21}) and similar notation to $R_{42,13}$, can be expressed as following:

$$R_{34,21}=\frac{V_{21}}{I_{34}} \qquad R_{42,13}=\frac{V_{13}}{I_{42}} \qquad \textbf{Eq. 3-15}$$

If the sample has a line of symmetry through points 3 and 2 as then $R_{34,21}=R_{42,13}$, the R_s from equation 3.1 can be simplified to:

$$R_S = \frac{\pi}{\ln 2} R_{34,21} \qquad \text{Eq. 3-16}$$

When the above condition is not satisfied, the general expression for the R_s is in the form:

$$R_S = \frac{\pi}{\ln 2} \frac{R_{34,21} + R_{42,13}}{2} f \qquad \textbf{Eq. 3-17}$$

where f is a correction factor as a function of the ratio $Q = R_{34,21}/R_{42,13}$. The relation between f and Q for the Van der Paul technique can be found from the reported literature [Pauw, 1958, 1959]. In general, when Q > 1.5, it indicates that a non-uniform doped layer or poor ohmic contacts have been formed.

All the Hall effect measurements in this work were carried on the Accent HL5500 Hall system. The samples were prepared in square patterns with 1mm x 1mm in dimension, as illustrated in figure 3.14. Prior the contact formation, standard diluted HF cleaning is preformed to remove the native oxide. Eutectic InP was then used to form the ohmic contacts at the 4 corners of the square samples, for which these points were the locations where the probe needles landed.

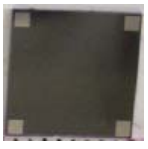


Figure 3.14: Example of the contact pattern on a sample used for Hall effect measurement.

During the characterization, the R_s and V_H are first measured by using the Van der Pauw technique, followed by the Hall measurements. To determine the R_s,

multiple measurements were performed for all permutations of the contacts, and the average value is used for the calculation of N_s. In any case, ohmic contact will be re-fabricated when the Q factor is larger than 1. In addition, the V_H were repeatedly measured with and without the presence of the magnetic field; the difference under these two modes will be subtracted from the real V_H to reduce the error induced by voltage misalignment. To reduce both the thermo-magnetic effects and photoconductive effects, the Hall measurements were conducted at a constant room temperature and dark environment.

3.4.3 Current Voltage (I-V) Measurements

The current-voltage (I-V) measurements were performed on the fabricated PMOS devices (chapter 4) and p+/n diodes (chapter 5 & 6) with the standard probe station.

In the PMOS devices analysis, probe station associated with HP 4145A semiconductor parameter analyzer and 4 high precision Source Measurement Units (SMUs) was used. The system is also coupled with microscope with a zooming option to ease the landing of probe needles on the gate, source and drain contacts of the devices. An automatic bias program was used to obtain the desired electrical parameters throughout the measurements in DC mode.

On the other hand, the p+/n diodes were measured on another instrument using the HP4156B semiconductor parameter analyzer. The biasing condition is between -3V and 3V with a sweeping rate of 0.01 V/s.

The above electrical measurements were performed under the room temperature ambient.

3.5 Monte Carlo Simulations

Monte Carlo (MC) simulations were performed to further understand and verify the hypothesis assumed in the flash annealing study (Chapter 6). In brief, the model is implemented in a non-lattice atomistic kinetic Monte Carlo simulator [Jaraiz et al., 2001], also known as Diffusion of Atomistic Defects Object-Oriented Simulator (DADOS).

It is based on ion-implant damage structures, designated as the amorphous pockets (I_nV_m) whereby the amorphous pocket re-crystallization rate is characterized by the effective size of the amorphous pocket. The damage model can nucleate from isolated IV pairs, I_2 and V_2, resulting in more complex amorphous pockets, I_nV_m, and further building up to amorphization. The self-consistent treatment of pure I, V clusters, and amorphous pockets I_nV_m allows for the model to account for the contribution of damage from point defects, amorphous pockets, and pure clusters.

In additional, physical modeling based on based on the latest data available from literature in terms of the Fermi-level effects [Bragado et al., 2005], damage evolution [Mok et al., 2005, Castrillo., 2005] ,dopants [Mok et al., 2006, Pinacho et al., 2006] and impurities [Pinacho et al., 2002], diffusion and clustering, and the interaction of interfaces [Rubio et al., 2002]. Calibration of the physical parameters is done with results from dedicated experiments, ranging from transmission electron microscopy (TEM) analyses, SIMS, and sheet-resistance measurements [Colombeau et al., 2006].

3.6 Summary

In summary, the details of sample fabrication and characterizations have been discussed and elaborated in this chapter. Brief descriptions on the theory of some physical and electrical characterizations are also included to provide the readers a quick insight and understanding of the major techniques. The more specific experimental details and variation in experimental procedures will be described in the subsequent chapters.

Chapter 4

The Impact of Nitrogen Co-implant on Boron USJ Formation and Physical Understanding

4.1 Introduction

Co-implantation of impurities into source/drain extension is an area which has gained intense interest since device improvement using this technique for USJ formation has been successfully demonstrated [Yamamoto et al., 2007, Tan et al., 2008]. Fluorine (F) and carbon (C) co-implant in Boron (B) doped preamorphized silicon is known to be able to reduce B transient enhanced diffusion (TED) and suppress dopant de-activation [Pawlak et al., 2006a, 2006b, Vanderpool et al., 2005, Graoui et al., 2005, Downey et al., 1998]. However, the application of nitrogen (N) as co-implant impurity for USJ formation is less established and the underlying physical mechanisms are not fully understood.

In the last few decades, in addition to the well-known effect of varying gate oxide growth, N co-implant has been shown to reduce B penetration into gate oxide due to the reduction of B diffusion in polysilicon [Liu et al., 1996, Kuroi et al., 1994]. Recently, N doped silicon layer was also developed to achieve the similar advantage, which is thought to be due to the suppression of B diffusion through Boron-Nitrogen (B-N) complex formation [Jalaert et al., 2001, Chao et al., 1996]. For the application

in junction formation, there has been controversy over the effect of N on B diffusion in silicon. Earlier, T. Murakami et al. reported that high dose N co-implant suppresses B TED [Murakami et al., 1997]. In contrast, another study claimed that B diffusivity is indeed enhanced by N co-doping in crystalline silicon [Dokumaci et al., 2000]. The former study speculated that high dose N co-implant induces end-of-range (EOR) defects, leading to reduction in B diffusion; while the latter work proposed that additional damage is introduced during the low dose non-amorphizing N implant, enhancing the dopant diffusion via the interaction with point defects. Some experiments also suggested that N atoms react with Vacancy (V) point defects to form the Nitrogen-Vacancy (NV) clusters in silicon and has been modeled for N diffusion study [Dokumaci et al., 2001, Adam et al., 2001]. It was proposed that the NV clusters can alter the B diffusion and activation, upon which device performance boost has been reported via N co-doping [Auriac et al., 2007]. Nevertheless, there is a lack of consensus on the different possible mechanisms involved in the USJ formation with N co-implantation.

In this chapter, an extensive experimental study on the impact of N co-implant in the Ge-PAI B junction is performed. The purpose of this work is to clarify and demonstrate the effect of N on B diffusion and activation associated with Ge-PAI for USJ application. Various physical mechanisms involved are discussed in terms of the interactions among the B dopants, co-implanted N atoms and the extended defects**,** to get a deeper understanding for the design and optimization of the source/drain extension for CMOS device fabrication.

4.2 Experimental Details

Czochralski grown 8-inch (100) n-type silicon wafers were subjected to preamorphization by performing a Ge ion implantation at 15 keV to a dose of 3×10^{14} $cm^{-2}$and subsequently with 1keV B to a dose of 1.5×10^{15} cm^{-2}. N co-implantation with energies of 2 keV, 6 keV and 25 keV to a same dose of 1×10^{15} cm^{-2} were performed on some wafers. In addition, 1/5 mass ratio is used convert the 1keV B to a 5 keV BF_2 with a dose of 1.5×10^{15} cm^{-2}, so that the both BF_2 and B have roughly similar initial B distribution profiles. The Ge and N implants were performed at 0^o tilt and 0^o twist angles, while B was implanted at 7^o tilt and 0^o twist angles to reduce the channeling effect in the tail of the profile. The thermal annealing was carried out in Uniaxis Addax XM80 RTA system under N2 ambient, with ramp-up and ramp-down rates of $60^oC/s$ and $45^oC/s$, respectively. The annealing conditions (temperature ranging from 650^oC to 1000^oC for 60s) were used to reveal junction stability through the dopant de/re-activation behavior. In addition, some wafers underwent spike annealing in Mattson 3000 Plus RTA system which is capable for higher ramp-up rate of $230^oC/s$ and ramp-down rate of $80^oC/s$ with peak temperature at 1080^oC. The spike annealing was performed with 100 ppm of oxygen to improve the uniformity across the whole wafer.

The dopant profiles were analyzed ex-situ by secondary ion mass spectrometry (SIMS) using a Cameca IMS 6f instrument. A primary beam of O2+ ions with a net energy of 0.5 keV at 56° incidence was scanned over an area of 250μm × 250μm for B profiling. The N distribution profiles were scanned via a primary Cs+ with a net energy of 2 keV at the same incident angle and scanning area.

The crater depth measurement was done using a Tencor Alpha-Step 500 profilometer. The sheet resistance (R_s) was measured by standard four point probe and verified by Van der Pauw measurements by Hall. Cross-sectional TEM (XTEM) was also performed to analyze the extent of amorphization and the Ge-PAI induced EOR defects.

4.3 The Impact of Nitrogen Co-implant on B Profiles

Figure 4.1(a) shows the SIMS profiles of B without co-implant, after thermal annealing at 4 different temperatures for 60s. The dopant profiles clearly show the B TED effect upon annealing. In addition, trapping of B atoms are visible beyond the former a/c interface with annealing temperatures of 700^{o}C and 750^{o}C. Upon increasing the anneal temperature to 900^{o}C, significant B diffusion occurs compared to that at 800^{o}C. This is possibly due to the dissolution of extended defects at 900^{o}C, resulting in emission of free Si interstitials which interact with B atoms and thus promoting the enhanced B diffusion.

Figure 4.1(b) presents the counterparts of B profiles where 6keV N has been co-implanted. The results clearly indicate that N atoms have significant effect on B profile broadening induced by the anomalous TED effect during thermal annealing. On top of the reduction in depth, one of the noticeable features shown is that the B trapping at EOR region becomes negligible for the cases below 800^{o}C. It is postulated that the EOR defects induced by the PAI could have been stabilized by the N atoms, and hence reducing the trapping of B atoms. For the cases of higher annealing

temperatures, the suppression of B TED in presence of N atoms is observed and associated with the improvement in junction abruptness.

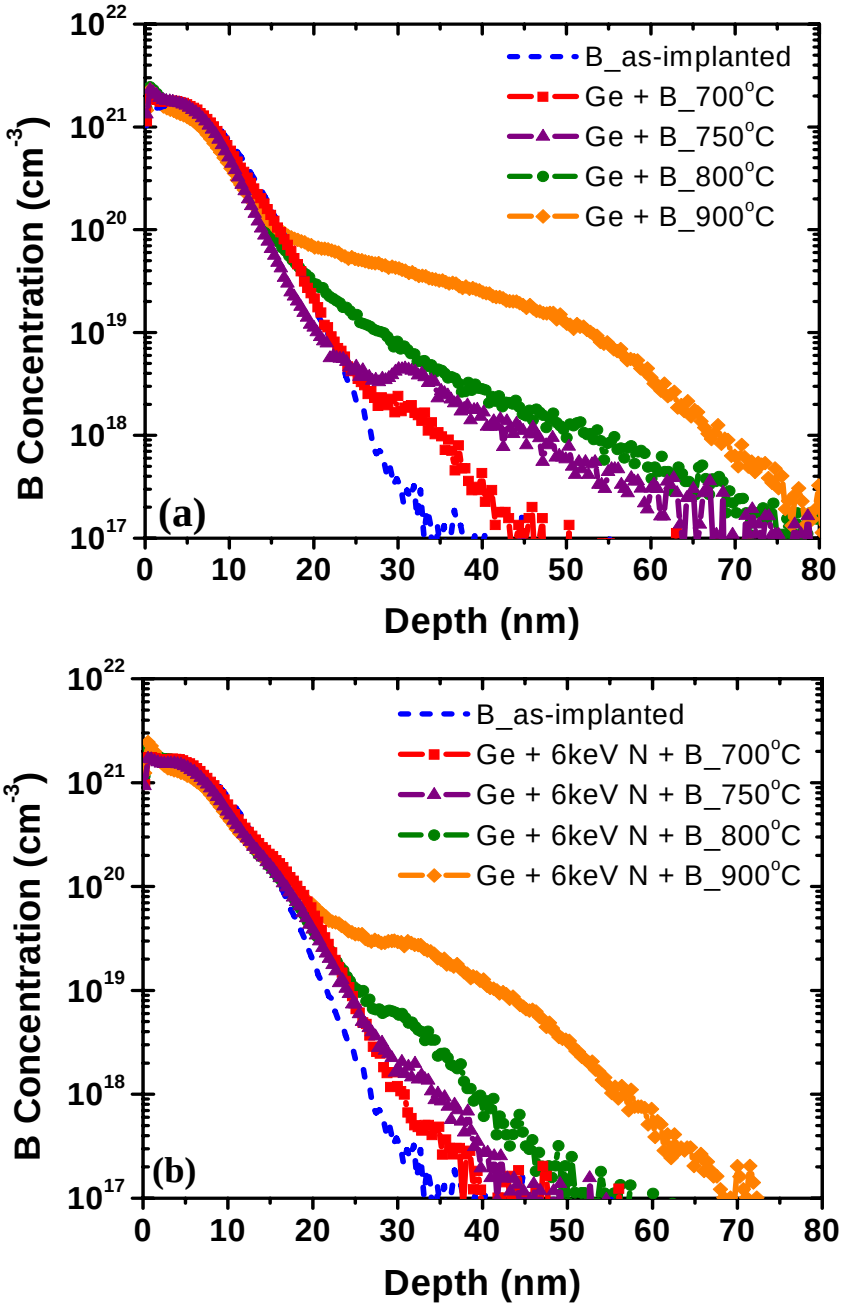


Figure 4.1: (a) SIMS profiles of 1 keV, 1.5×10^{15} cm^{-2} B implant, before and after RTA annealing at different temperatures: 700°C, 750°C, 800°C and 900°C for 60s. (b)

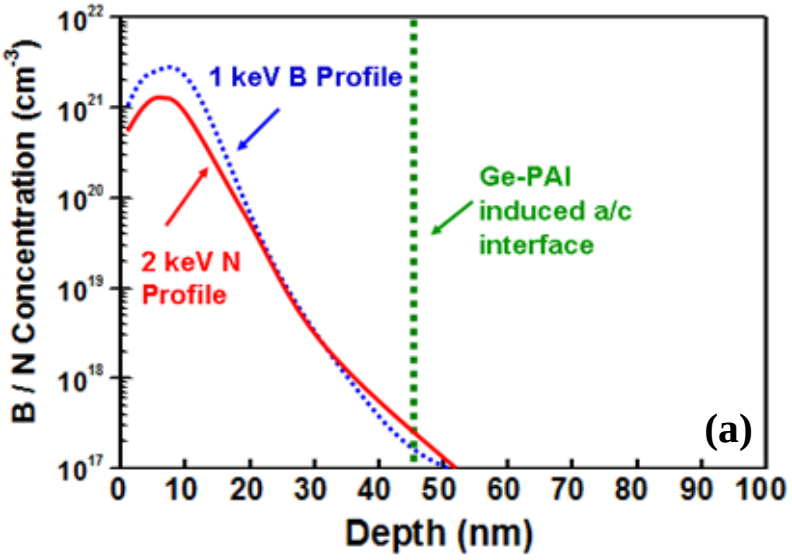
The corresponding profiles in the case where 6 keV, 1×10^{15} cm^{-2} N has been co-implanted and annealed at the same conditions.

Based on above observations, it is reasonable to deduce that additional dopant-defect interaction or pathway could have involved in the B doped layer when the N co-implant is implemented.

4.4 The Effect of Nitrogen Distribution on B Diffusion

4.4.1 The Initial As-implanted Conditions

To get a deeper understanding of the possible mechanisms, the diffusion and activation behaviors of B with three co-implant conditions are studied here. The three N implant energies were chosen so as to purposely to locate the N projected range (a) similar to the project range of the B implant, (b) between the peak B profile and the Ge-PAI induced amorphous/crystalline (a/c) interface and (c) well beyond the B profile and the Ge-PAI induced a/c interface. The 3 different experimental conditions are illustrated in figure 4.2.



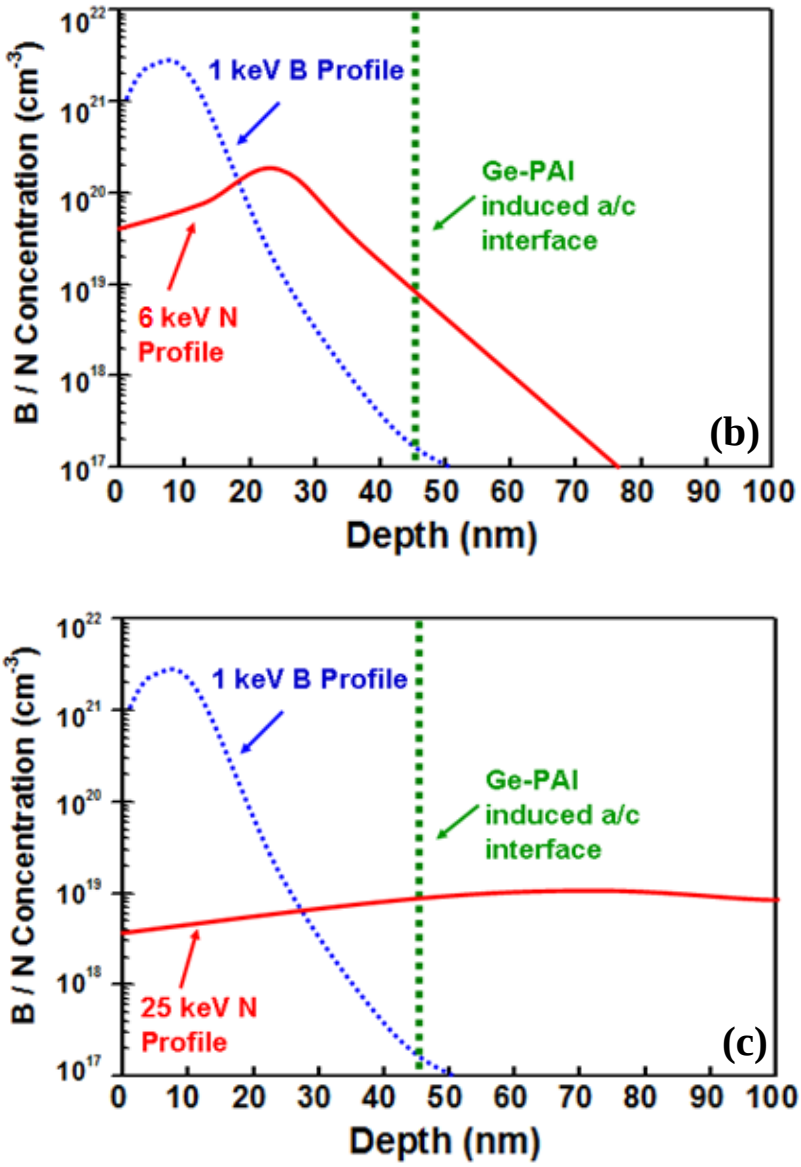


Figure 4.2: Schematic diagrams showing the 3 different experimental conditions with N co-implant, N profile is located (a) to have similar project range of the B profile, (b) between the peak B profile and the Ge-PAI induced a/c interface and (c) well beyond the B profile and the Ge-PAI induced a/c interface.

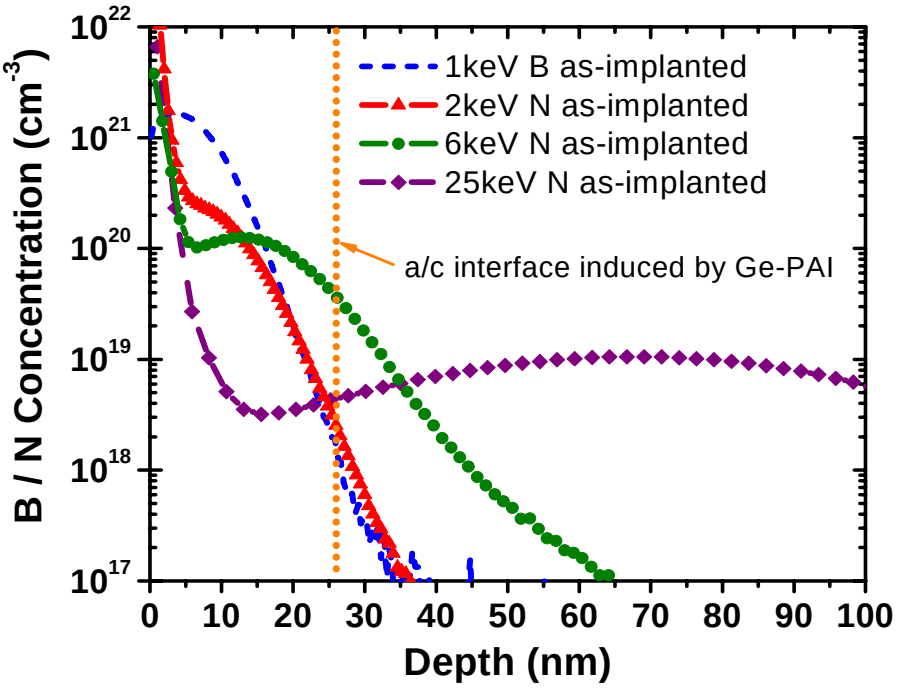


Figure 4.3: SIMS depth profiles for 1 keV B implant and the 2, 6, and 25 keV N implants used in used study. The depth of a/c interface induced by the prior 15 keV Ge-PAI is drawn with vertical dotted line for reference here.

The SIMS as-implanted B and N chemical dopant profiles are shown in figure 4.3, demonstrating that the actual N distributions are close to the target profiles. However, it is also observed that N atoms are significantly segregated near the first 3nm of surface; this is possibly an out-gassing effect of N during the implantation [Dokumaci et al., 2000, 2001]. Nevertheless, the extremely high N_2 concentration near to the surface (>20% of Si in absolute concentration) is possibly an artifact induced during the SIMS characterization.

Figure 4.4(a) shows the XTEM of the sample implanted with 15 keV Ge followed by the 1 keV B; the depth of the a/c interface is around ~26-27nm.

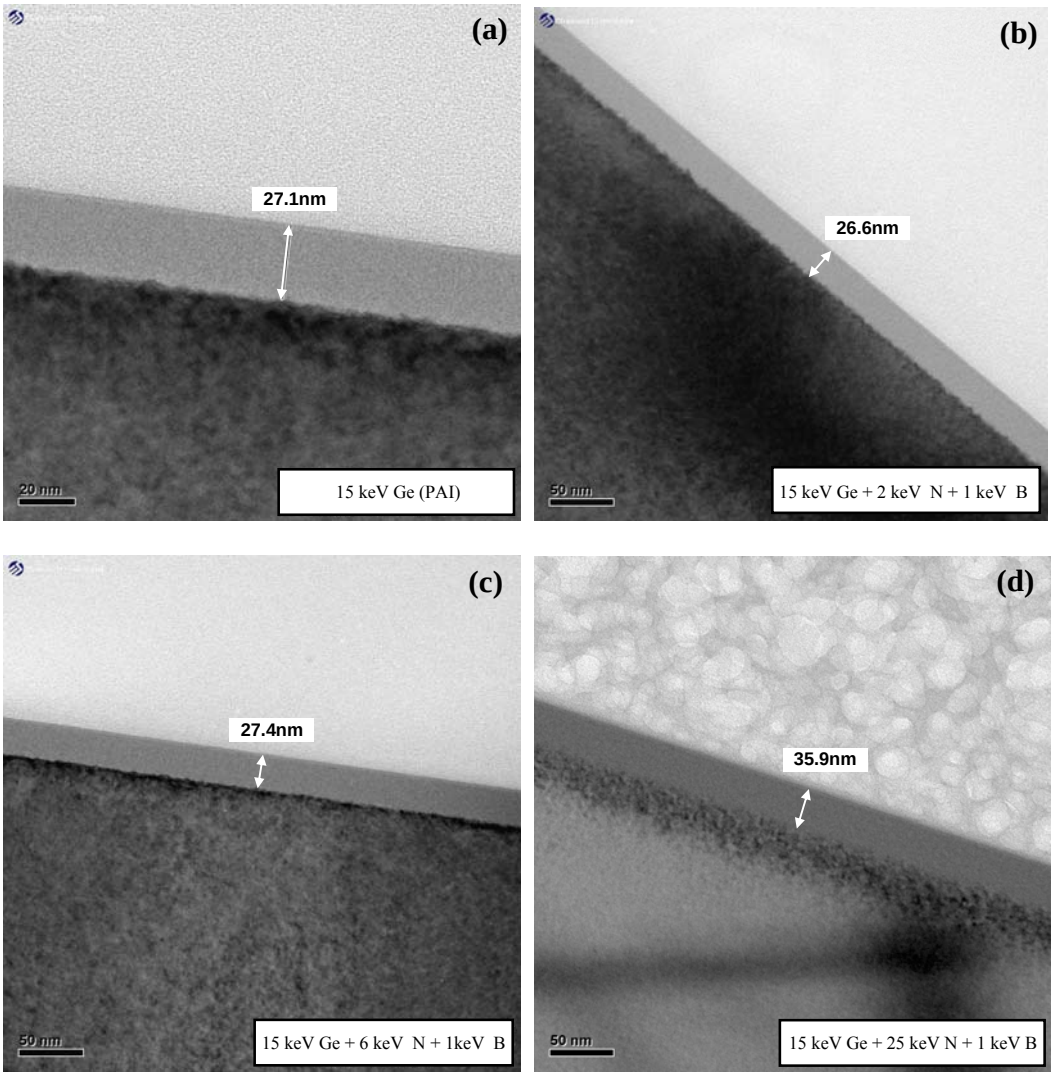


Figure 4.4 XTEM for the as-implanted samples with (a) 15 keV Ge + 1 keV B implant only, (b) 15 keV Ge + 2 keV N + 1 keV B, (c) 15 keV Ge + 6 keV N + 1 keV B and (d) 15 keV Ge + 25 keV N + 1 keV B.

Since B is well known as a low mass atomic element, the a/c interface is thus the result of the preamorphization effect induced by the Ge implant. Figure 4.4(b) and (c) reveal that the thickness of the amorphous layer remains unchanged (~26-27 nm) even after 2 keV or 6 keV of N was implanted after the Ge implant and prior to B implant. On the other hand, the 25 keV N implant causes an extension of the a/c

interface to a depth of around ~36nm (figure 4.4(d)). The a/c interface is very rough and ambiguous a/c transition is observed. The rough transition region is approximately ~30nm thick and is in the form of semi crystalline/amorphous phase.

4.4.2 De/re-activation of Boron with Nitrogen Co-implant (Isochronal Annealing)

Figure 4.5 shows the B de/re-activation characteristic performed by the R_s measurements on the isochronal RTA annealed samples with temperature ranging from 650°C to 1000°C for 60s. For the case of N-free samples (open square in figure), the data indicates an initial low R_s value at 650°C due to the high activation level being achieved after the SPER process.

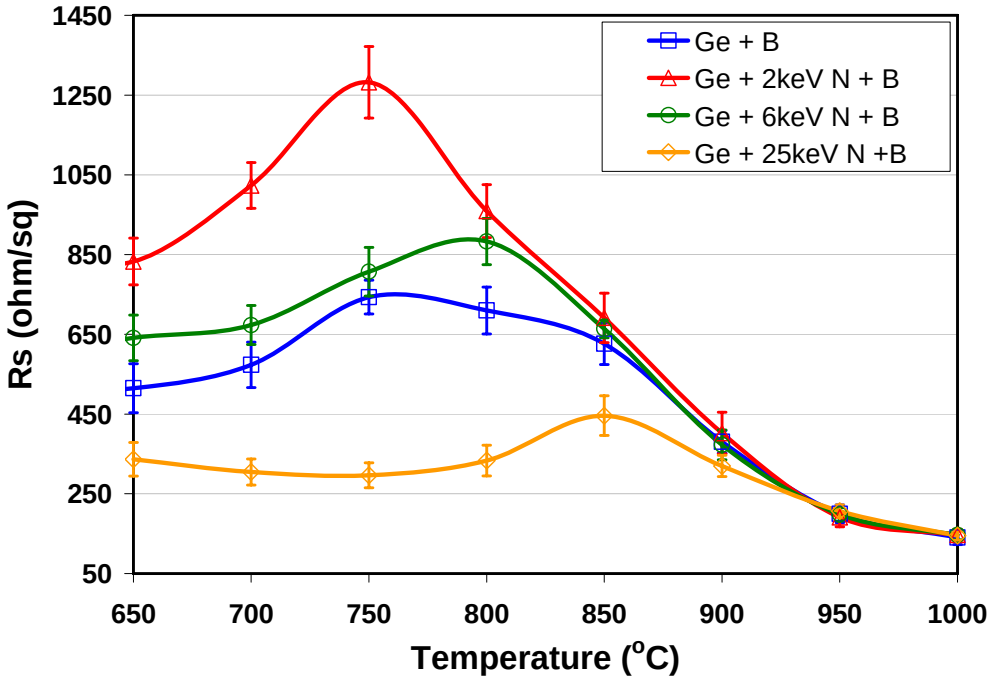


Figure 4.5: Sheet resistance value (R_s) as a function of 60s isochronal annealing temperature for the 1keV B implant with and without N co-implant at 2, 6 and 25 keV.

Following the increment in temperature, the R_s rises continuously before it starts to drop with further increase in temperature. This behavior is known as the "reverse annealing" effect and is generally observed in other B doped PAI studies [Seidel, 1983, Colombeau et al., 2004b]. It can be thought as an evolution event of the dopant-defect interactions which results in the change of junction sheet resistance [Claverie et al., 2000b].

In brief, the early low temperature annealing corresponds to the dopant activation during the SPER and recombination of the point defects (interstitial/vacancy) in the non-amorphized region, leaving a band of excess interstitials just below the amorphous-crystalline interface. With increasing annealing temperatures, these defects evolve from small interstitial clusters to extended defects (eg. {311} defects or dislocation loops) in the EOR region located around the as-implanted a/c interface. At the same time, interstitial point defects released from the EOR defects will diffuse to the B rich surface to form small, immobile, electrically-inactive boron interstitial clusters (BICs), thereby deactivating some of the electrically activated substitutional B atoms and degrading the junction R_s [Vanderpool et al., 2005]. The activation will be restored eventually when dissolution of BICs and B diffusion take place at a higher annealing temperatures, when the EOR extended defects are mostly or completely dissolved.

The de/re-activation of B associated with N co-implant at 3 different energies is also shown in the same figure. Interestingly, huge variations in terms of the R_s values are observed across the different N distributions. Unlike the gain in B diffusion suppression (shown in figure 4.1 (a) and (b)), the 6 keV N condition degrades the R_s

at the initial low annealing temperature of 650^{o}C. The consequence of higher R_s values in the 6 keV N co-implanted sample suggests that B would interact with the N atoms to produce B-N complexes [Chao et al, 1997, Bouridah et at, 2004]. Hence, B-N formation during the SPER reduces the B atoms being substituted into the lattice, leading to a lower electrical dopant activation level with larger R_s. This has been verified by a Hall effect measurement, and the results indicate that the sample co-implanted with 6 keV has its active carrier concentration (N_s) 18% lower (reducing from 5.90×10^{14} cm^{-2} [No N co-implant] o 4.84×10^{14} cm^{-2}[6 keV N]) than the B case without N co-implant.

Furthermore, by reducing N implant energy to 2keV, the profile overlaps between the distributions of B and N atoms increases (shown in figure 4.3). Similarly, the R_s increases further from ~650 to 850 ohm/sq, comparing to the case of 6keV N co-implant at annealing temperature of 650^{o}C. The huge jump in R_s, about 30%, further re-affirms that the possibly of B-N reaction induces de-activation during the process of SPER and can be correlated to the overlapping density between the B and N profiles. From Hall measurement, the N_s has dropped about ~ 20% (from 4.84×10^{14} cm^{-2} [6keV N] to 3.82×10^{14} cm^{-2} [2keV N]), which is less than the R_s percentage gain and found to be attributed to the degradation of mobility for the 2keV N case. As the temperature increases, the 2keV N co-doping reaches the highest R_s of ~1282 ohm/sq at 750^{o}C. This is followed by continuous R_s reduction up to 1000^{o}C.

Lastly, in the case of 25keV N, the deleterious increase of R_s attributed to B-N interactions is not expected due to the smaller overlapping fraction of B and N atoms as seen in figure 4.3. The results also show that the samples co-implanted with

25keV N has an overall lower R_s values across the various annealing temperatures, which is attributed to the increased B activation with the deeper amorphous layer in the sample, shown in figure 4.4(d) earlier. The deeper amorphization extent is believed to cause the R_s peak position shift to higher temperature at 850^{o}C.

To further quantify the extent of de-activation, R_s values are re-plotted in terms of the percentage change in R_s (normalized to their respective samples annealed at 650^{o}C) in figure 4.6. From this figure, one may conclude that the B deactivation is indeed reduced by the N co-implant. This can be noticed from the de-activation peaks across the 3 different co-implant cases. It has to be emphasized that 25 keV N co-implant further increases the amorphous region, which is unlike the outcomes of the 2 keV and 6 keV N co-implants where their amorphous layers are defined by the Ge-PAI at around ~26-27nm. A deeper amorphous layer thickness has been reported to decrease the amplitude as well as delay the maximum point of deactivation [Pawlak et al., 2006a]. Such an outcome is clearly seen in the de-activation curve of the 25 keV N co-implanted samples.

With the same amorphous layer thicknesses, the 6 keV N co-implant results in lower extent of peak deactivation percentage compared to both B only and 2 keV N co-implant conditions. The larger gain of deactivation suppression for 6keV N case can be indirectly deduced to be the result of silicon free-interstitials (released from the EOR region) trapping by the NV clusters formed between the peak of B profile and EOR region during the SPER. However, the effect of B-N complexes on B de-activation cannot be ruled out as well. This is particularly in the case of 2 keV N co-doping, where reduced dopant deactivation is also seen. Another significant feature is

their peak deactivation temperature; the lower peak temperature in the 2keV N case is possibly signifies the larger extent of interactions between the B and N atoms.

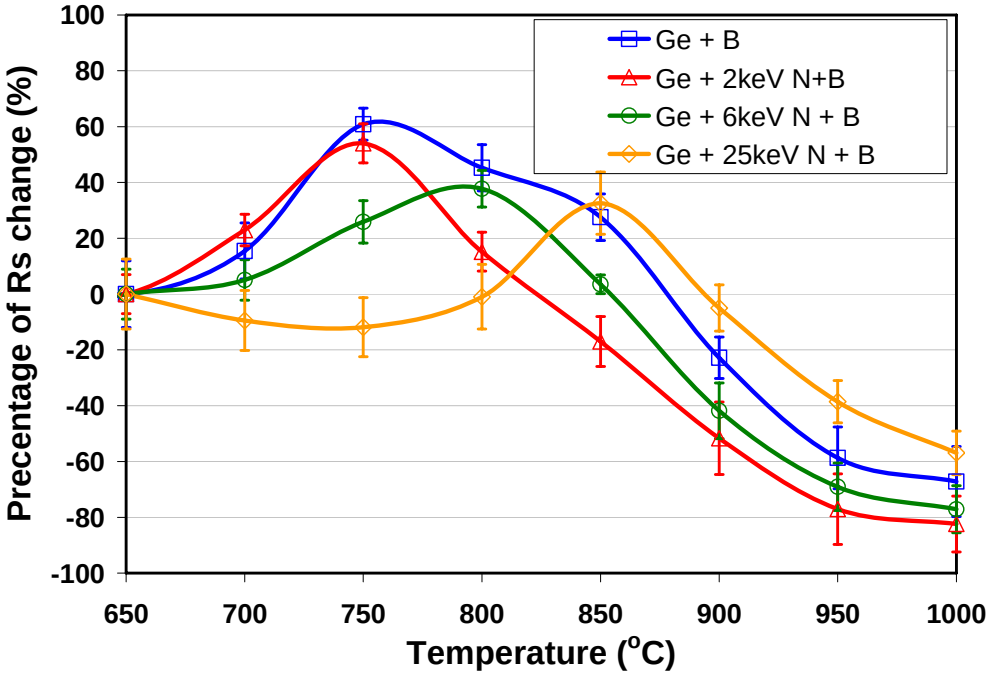


Figure 4.6: Percentage change of R_s (normalized with the R_s at 650°C) as a function of 60s isochronal annealing temperature for the 1keV B implant with and without N co-implant at 2, 6 and 25 keV.

4.4.3 Boron and Nitrogen Diffusion with Nitrogen Co-implant

(a) Boron Diffusion Profiles

Figure 4.7 depicts the various B profiles processed with RTA annealing at 700°C for 60s. The sample implanted with B only reveals a kink around the a/c interface and the dopants start to diffuse beyond this point. It is similar to the case when a 2keV N is co-implanted prior to the B. With a closer look it is found that its B concentration around the "kink" is lower. The N atoms are believed to have interacted with EOR defects thereby reducing the B trapping. Although the diffused B profile

with 25 keV N co-doping has a same junction depth as the B only case at a concentration of 1×10^{18} cm^{-3}, its kink level is about 2 orders higher (at 3×10^{18} cm^{-3}) and attributed to the effect of deeper amorphous layer induced by the high N implant energy at 25 keV. Since B has been previously shown to have larger diffusivity in the amorphous layer, the 25 keV N shows a deeper depth beyond its kink level at 3×10^{18} cm^{-3} but before the tail profile meeting up with the B only and 2keV N co-implanted B counterparts. Nevertheless, the 6 keV N co-implant shows an overall shallowest tail junction with a high kink B concentration at 2×10^{20} cm^{-3} even if its amorphous layer is similar to the B only case. This indirectly suggests that 6 keV N co-implant would have played a key role in suppressing the B diffusion.

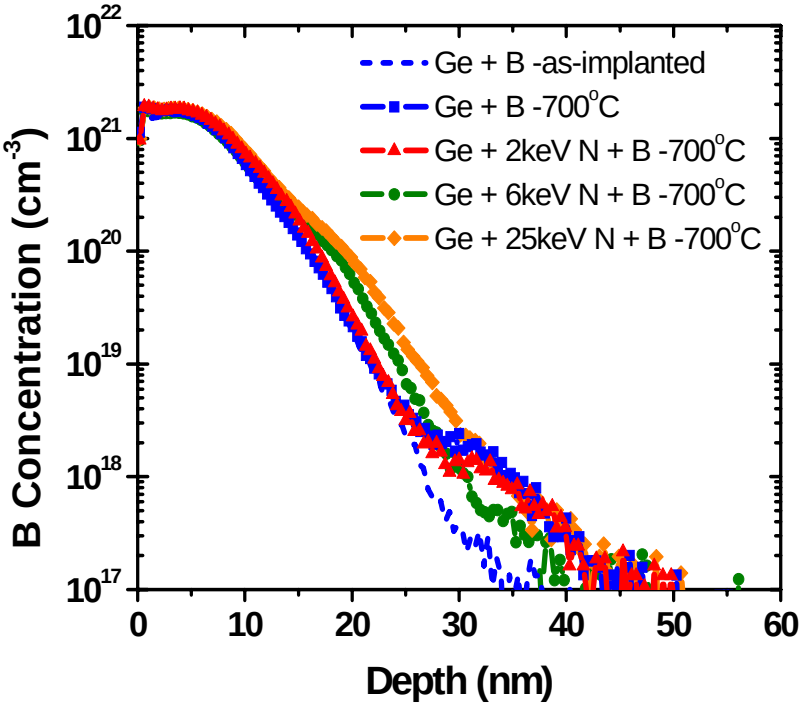


Figure 4.7: SIMS profiles of 1 keV B implant with and without N co-implant at 2, 6 and 25 keV after annealing at 700°C for 60s.

Figure 4.8 illustrates the impact of N co-implanted atoms on B diffusion when subjected to annealing at 800^{o}C. Unlike the profiles at 700^{o}C anneal, the diffused B profiles have kink level variations within half an order, providing an easier comparison for the B TED effect. The results clearly indicate that the effect of N on B diffusion can be significantly different by changing the distribution of N atoms. Both the 2keV and 6keV N co-implanted samples exhibit shallower junction depths than that of the B only case. It is hypothesized that one possible reason for the B diffusion reduction is the interactions of B with N atoms inhibiting the B-I reactions, at which the latter is responsible for the B TED effect. One should note that the de-activation due to B-N complex at low temperature (650^{o}C) is more extensive for the 2 keV N compared to the 6 keV N co-implant (higher R_s for 2keV N, shown in figure 4(b)). Therefore, the B TED suppression due to the B-N interactions is expected to be larger in the 2 keV N condition; however, the experimental SIMS profiles show a greater reduction in B diffusion for 6 keV N co-implant. Indeed, a similar better suppression in B TED with 6 keV N has been shown in the previous figure with RTA temperature of 700^{o}C. It is possible that the suppression of B TED is contributed by the enhanced effect of free-interstitial trapping by the NV clusters formed during the SPER of the amorphous layer. The silicon free-interstitials are released from the EOR defect band and this has been conventionally taken to be the root cause of B TED and deactivation. This is similar to what has been reported for F atoms in Ge-PAI silicon, where Fluorine-Vacancy clusters are formed during SPER [Colombeau et al., 2004a].

For a 25keV N co-implant, the improvement in final junction depth is almost negligible at this temperature. Although deeper B distribution has been observed

between the kink of the B profile at 2×10^{20} cm^{-3} and $1x10^{18}$ cm^{-3}, it eventually reaches the tail B profile similar to the N-free case. The suppression of B TED is not seen at this anneal condition when the N distribution is located well beyond the B profile. The results show that the two earlier proposed mechanisms - interstitial trapping by NV clusters as well as the B-N reactions for complex formation, are not significant when the N implant is increased to 25 keV. Besides, the B profiles associated with this N implant energy present a static "kink" at larger concentration ($8x10^{19}$ cm^{-3}), suggesting that higher dopant activation level has been achieved [Cowern et al., 2005a]. This is in agreement with the lower R_s value seen in figure 4.5 possibly contributed by the deepening of amorphization caused by high energy co-implantation of N atoms.

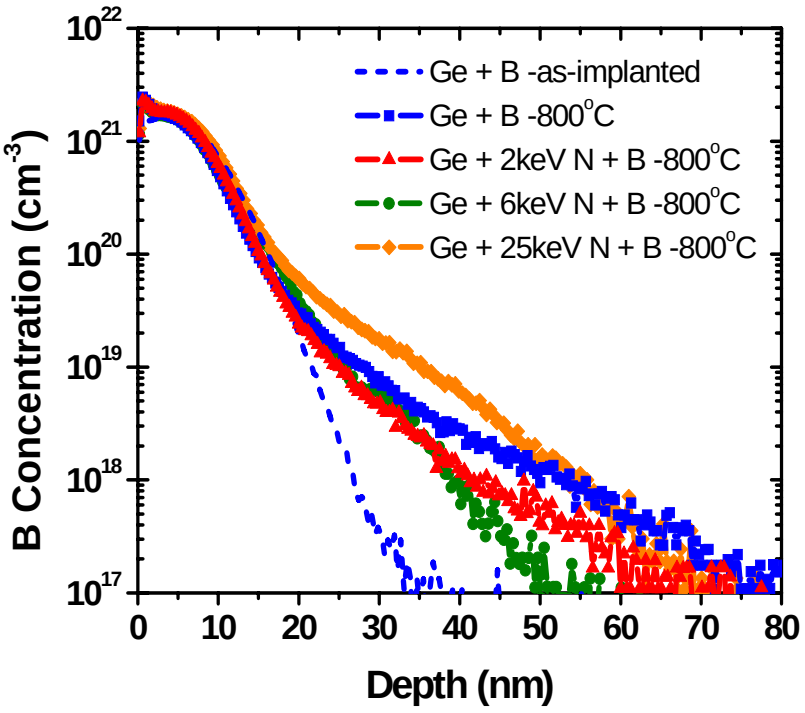


Figure 4.8: SIMS profiles of 1 keV B implant with and without N co-implant at 2, 6 and 25 keV after annealing at 800°C for 60s.

Figure 4.9 is another set of SIMS data demonstrating B profiles after annealing at 900°C for 60s.

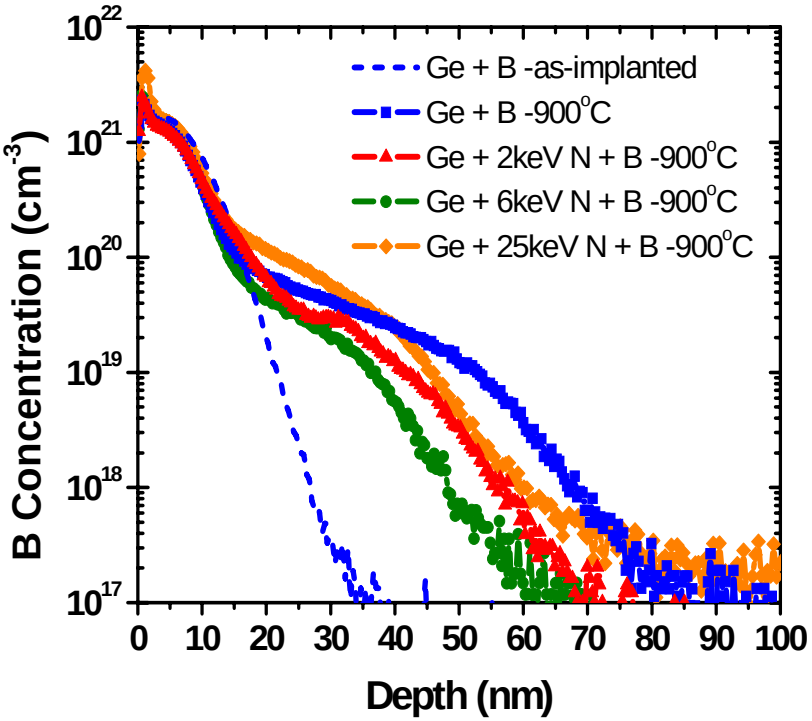


Figure 4.9: SIMS profiles of 1 keV B implant with and without N co-implant at 2, 6 and 25 keV after annealing at 900°C for 60s.

The relative effect of the N co-implant becomes clearer and re-affirms that the placement of N distribution with respect to the EOR region is playing a key role which eventually affects the junction depth. At the concentration level of 1×10^{18} cm^{-3}, the depth starting from shallowest to deepest are in the sequence of 6 keV N, 2keV N, 25 keV N and lastly followed N-free B doped samples. The B-N interactions are expected to take place mostly in the 2 keV implant, whilst it is expected to be smaller but up to certain extent in 6 keV N condition due to the overlapping between the implanted B and N distributions. The latter B condition shows better reduction in junction depth is consistent with the annealing temperatures of 700°C and 800°C,

implying that the 6 keV N co-implanted condition is more effective in interstitial trapping via NV clustering mechanism which takes place during the SPER.

For the 25 keV N co-implant on the other hand, the B profile shows a higher activation "kink" again thanks to its thicker amorphous layer, but it appears that a shallower junction results when compared to the control B case below the B concentration of 1×10^{19} cm^{-3}. Since the benefits of B-N complex and NV cluster formation on junction depth has not been illustrated in 700^{o}C and 800^{o}C for the 25 keV N, the reduced junction depth seen here could be related to the different level of dissolution of EOR extended defects at or above 900^{o}C, possibly influenced by the implanted N atoms. It is also possible that N on substitutional sites may trap interstitials becoming mobile/out-gassing resulting in less TED. Nevertheless, the impact of the variation in the extent of amorphization on defect evolution cannot be ruled out in this case as well.

(b) Nitrogen Diffusion Profiles

Figure 4.10 to 4.12 depict the as-implanted and diffused co-implanted N profiles at 800^{o}C and 900^{o}C for 60s. These annealed N profiles reveal the obvious nitrogen out-gassing effect. The amount of the retained N atoms is also reduced when the annealing temperature is raised to higher level regardless the N implant energy.

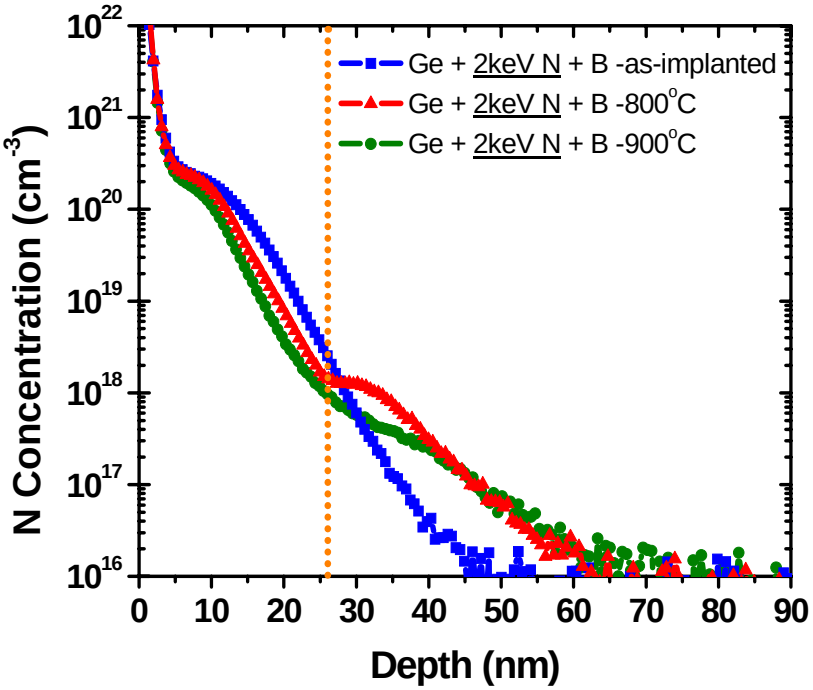


Figure 4.10: SIMS profiles of 2keV N co-implant before and after subjected to annealing at 800°C and 900°C for 60s.

In figure 4.10, the 2keV N annealed at 800°C reveals a minor peak corresponding to the N atom trapping beyond the a/c interface at around ~30-35nm. It is worth to mention that the B atom trapping at EOR defects usually would not survive but should be fully dissolved at this temperature level. The N trapping peak vanishes at 900°C, indicating that the extended defects at the EOR region would have dissolved and released the N atoms as well as the free silicon interstitials that significantly cause further B diffusion.

Figure 4.11 shows the 6 keV N profiles which were co-implanted prior the B doping. It can be observed the amount of retained N atoms is significantly reduced after annealing, and the retained N dose becomes even less when the temperature is increased from 800°C to 900°C. The severe N out-gassing effect also causes the N

distribution to be shallower than the as-implanted N distribution even when annealing is performed at a higher temperature.

In addition, it can be seen that the N trapping peak has shifted into the amorphous layer from the bulk crystalline region where the silicon interstitials conventionally agglomerate to form the EOR defects. EOR defects are generally known to grown upon coarsening and will reside both deeper and shallower around the a/c interface. Therefore, the N gettering to the evolving EOR defects might explain the peak shifting. In addition, this can be postulated as an evidence of N clustering, possibly in the form of NV clusters, during the SPER of the amorphous layer. As mentioned previously, the NV clusters would react with the Si interstitials emitted from the EOR and reduce the B-interstitial interactions. Therefore, a greater suppression of B TED is achieved with this N co-implant condition and results in shallowest B junction profile. Besides the shift in the N trapping peak, it is noticed that the N atoms were trapped at the high concentration range of 1×10^{19} cm^{-3} for 6 keV N compared to the 2keV which is only around the 1×10^{18} cm^{-3} range. Besides, the N trapping peak decreases to a lower concentration level when annealed at 900^{o}C but it still appears above the concentration of 1×10^{19} cm^{-3}, suggesting that N trapping mechanisms are significantly different between the 6 keV N and 2 keV N co-implant conditions.

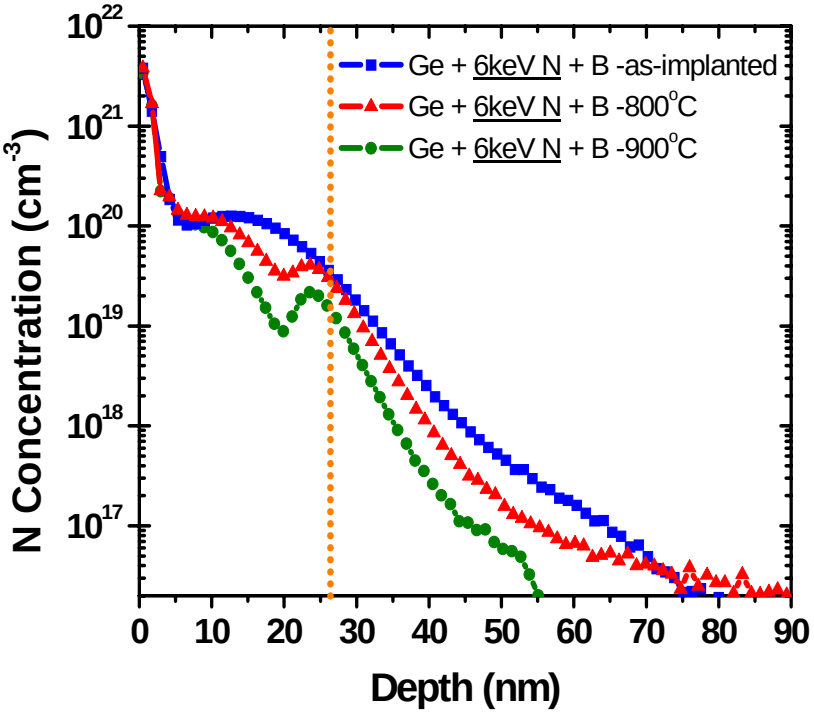


Figure 4.11: SIMS profile of 6 keV N implant before and after subjected to annealing at 800°C and 900°C for 60s.

For the case of 25 keV N co-implant (figure 4.12), N out-gassing is also clearly shown in the profile. Similar to the previous condition, more N atoms are lost at higher temperature and hence a narrower and shallower N distribution results at 900°C. However, the N atom trapping feature is not significantly demonstrated on the annealed profiles around the a/c interface either in the amorphous phase or the crystalline region shown in either 2keV or 6keV implants. Therefore, it is not surprising that the impact of 25keV N co-implant on B diffusion is not significant, owing to the much smaller overlapping region of their as-implanted distribution between B and N atoms.

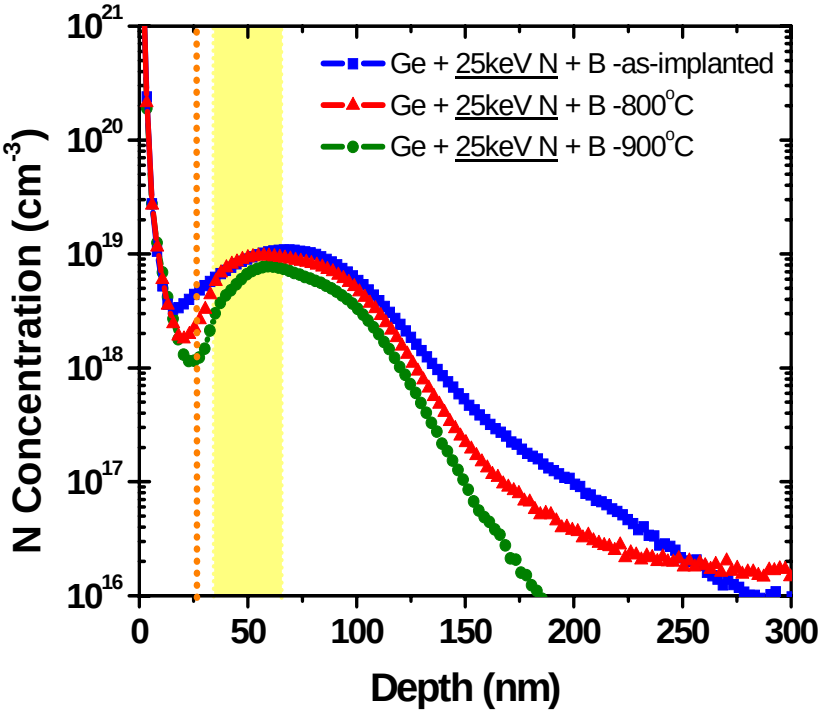


Figure 4.12: SIMS profiles of 25 keV N implant before and after subjected to annealing at 800°C and 900°C for 60s.

(c) EOR Defects

Figure 4.13 shows the XTEM of the various samples subjected to annealing at 650°C for 60s. The images confirm that full re-crystallization of the amorphous layer has taken place for all conditions, leaving an observable defect band at the EOR region.

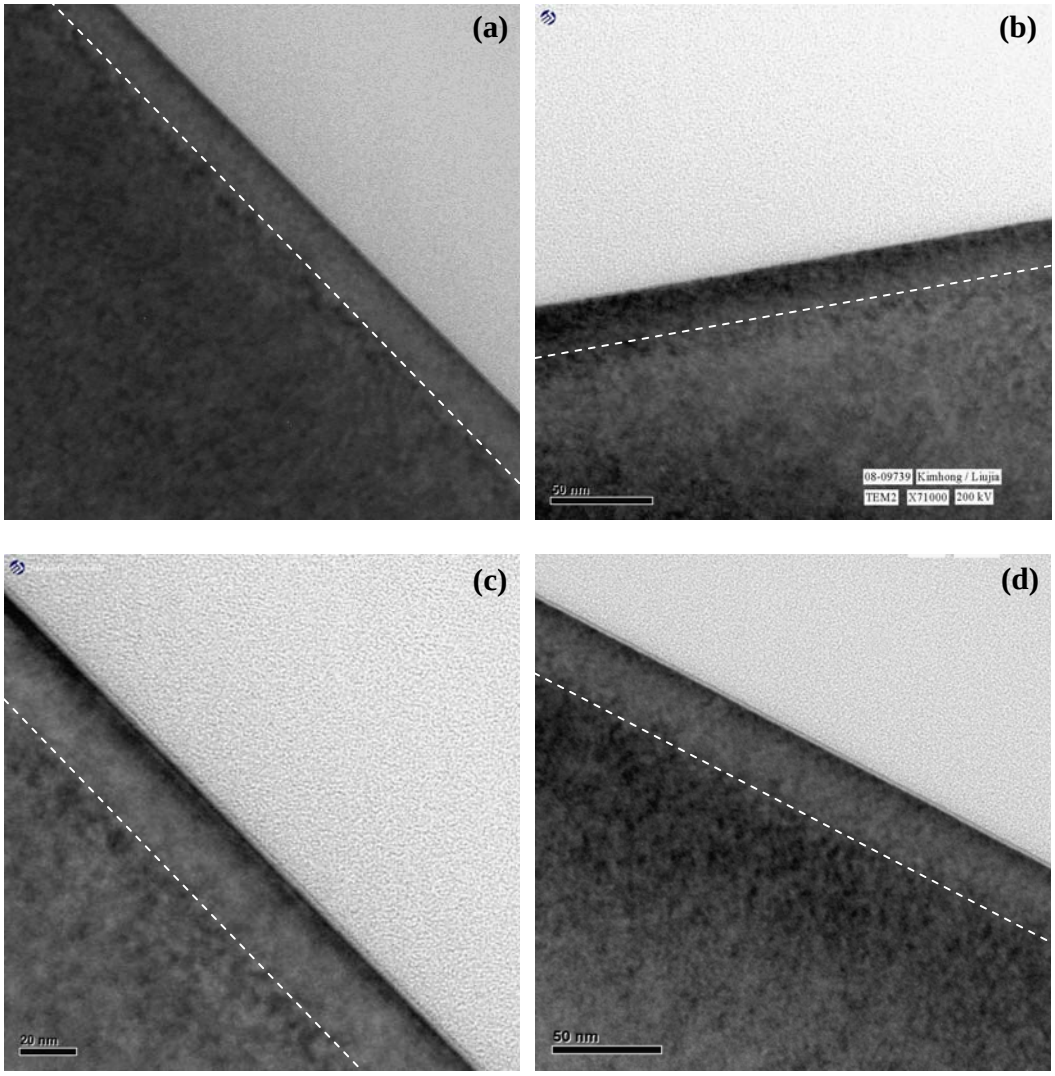


Figure 4.13: XTEM of the N co-implanted samples subjected to annealing at 650^{o}C for 60s. The implant conditions of various splits are: (a) 15 keV Ge + 1 keV B implant only, (b) 15 keV Ge + 2 keV N + 1 keV B, (c) 15 keV Ge + 6 keV N + 1 keV B and (d) 15 keV Ge + 25 keV N + 1 keV B. Dotted lines are drawn to show the a/c interfaces.

The location of the EOR defects band can be correlated to the a/c interface of the as-implanted samples. For instance, the defects for 2 keV N, 6 keV N and B only conditions lie below the depth of ~27-28nm, while it is extended to below ~35-36nm for the 25keV N co-implanted case. For an anneal temperature of 650^{o}C, the EOR

defects are expected to be in their early stage of evolution and the defects are not stable. Nevertheless, the amount of defects for the 2keV and 6 keV N is estimated to be less than the reference B only case upon close examination. This suggests that the EOR defect evolution has been affected by the N atoms. Conversely, the defect band in the 25 keV N is shown to have grown wider, which is believed to be due to the re-crystallization of the rough a/c transition layer (shown in figure 4.3(d)) induced by the high energy N co-implant.

To further investigate the defect structure, the XTEM images were performed on the samples with higher anneal temperature of 750^{o}C and these are shown in figure 4.14. In the N-free B sample, a great population of defects still remains below the a/c interface. Interestingly, figures 4.14(b) and (c) illustrate that the N co-implant at 2keV and 6keV N significantly reduces the defect density at the EOR region, which has already been observed after the annealing at 650^{o}C. In addition, it also complements the earlier SIMS results, in figure 4.1(a) and (b), with less B dopant trapping when a 6 keV N is co-implanted on the B doped samples at 750^{o}C. This is the strong evidence in support of the hypothesis that the N atoms may lead to the stabilization of EOR defects. It can be thought that the defects in the EOR regions have evolved into more stable extended defects in the presence of N atoms. However, it is also worth mentioning that the defect profile and density are not too different for the 2keV and 6keV N conditions as seen from their respective XTEM images. Therefore, it is believed that the impact of the stabilization of defect by N co-implant may be minimal in its contribution to the suppression of B diffusion and its deactivation

behavior. Nevertheless, more in-depth study is required to establish the effect of EOR defect stabilization by the N co-implant.

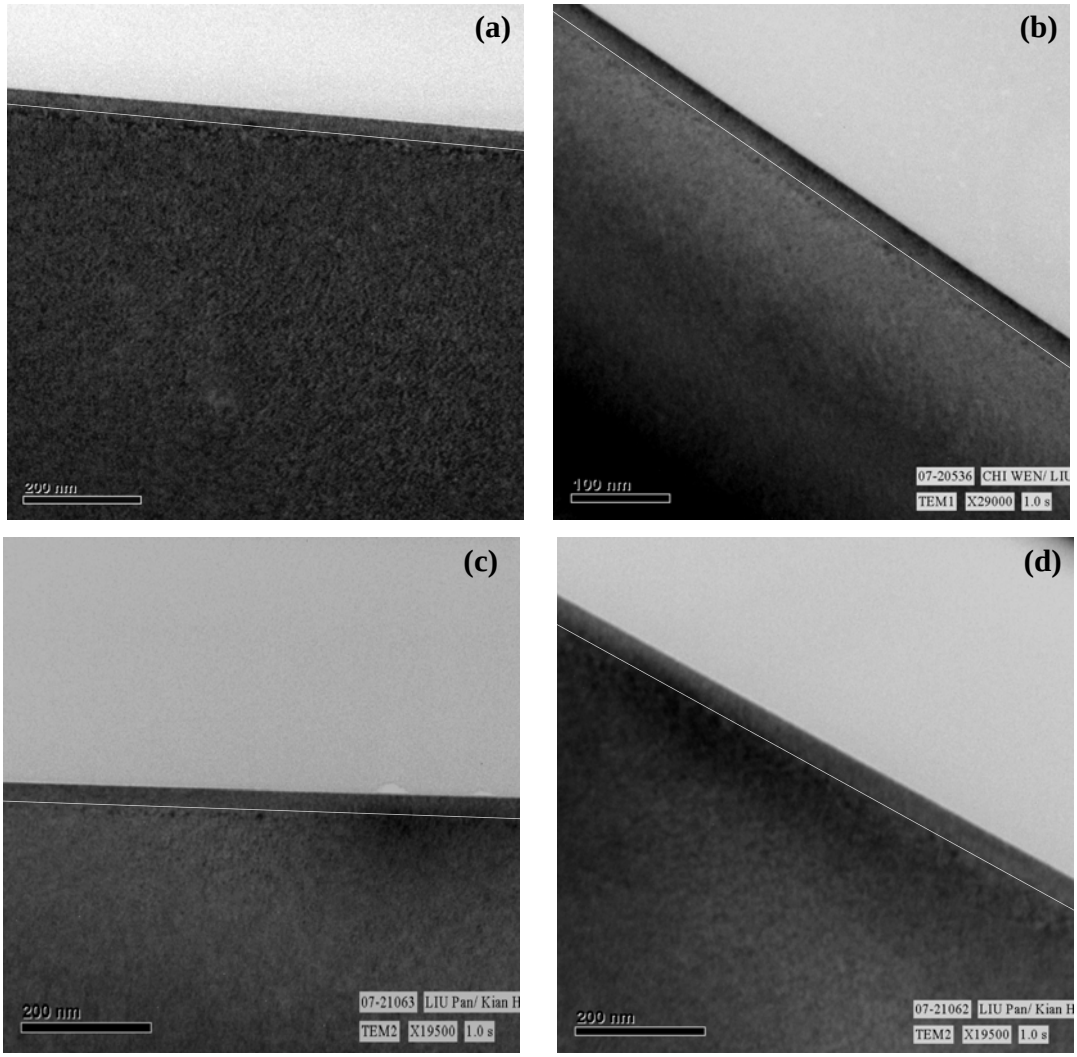


Figure 4.14: XTEM of the N co-implanted samples subjected to annealing at 750^{o}C for 60s. The implant conditions of various splits are: (a) 15 keV Ge + 1 keV B implant only, (b) 15 keV Ge + 2 keV N + 1 keV B, (c) 15 keV Ge + 6 keV N + 1 keV B and (d) 15 keV Ge + 25 keV N + 1 keV B. Dotted lines are drawn to show the a/c interfaces.

The sample co-implanted with 25keV N shows the EOR defect band located 10nm deeper than the others as shown in figure 6(d). Because of the additional

amorphization induced by the high energy N implant on top of the Ge-PAI, a wider defect band has resulted which is also seen after annealing at 650^{o}C. The additional amorphization causes lower R_s with no significant gain in B diffusion suppression compared to the N-free B control sample. The kinetics of the defect transformation could be changed since higher concentration of silicon interstitials are introduced into the EOR defect range due to deeper preamorphization effect induced by the high energy 25 keV N co-implant.

4.4.5 A Summary of the Effect of Nitrogen Distribution on Boron Diffusion

The results presented above have clearly demonstrated the effect of N co-implant on the diffusion and activation behaviors of B in Ge pre-amorphized silicon. The distribution of N atoms with respect to the B profile and EOR defect band is an important factor to determine final dopant profile and the electrical properties of silicon. As shown above, the R_s will be degraded through the interaction between the B and N atoms to produce the B-N complexes. Hence, the extent of the degradation is largely dependent on the overlapping density between the B and N profiles.

In additional, NV clusters are proposed to be formed during SPER, which would be able to trap the emitted silicon interstitials from EOR, indirectly suppressing the dopant deactivation to a certain extent. The hypothesis is proven through a combination of evidences from activation and diffusion results seen in figure 4.5-4.9. The efficiency of the free interstitial trapping can be enhanced not only by reducing the B-N complex formation to increase the chances for NV cluster

formation, but it is also necessary to locate the N atoms at a position which facilitates the formation of NV clusters and subsequently traps the interstitials released from the EOR region. Indeed, both of the involved mechanisms, NV clusters and B-N complexes, assist in suppressing the B TED and the latter pathway degrades the B activation level. Nevertheless, silicon trapping by NV clusters is believed to be dominant if the N distribution is optimized as seen in the 6keV N co-implant case.

There is also the possibility of EOR defect stabilization by N co-implant. For instance, inferences can be obtained from the SIMS profiles that the two lower energy N profiles (2keV and 6keV N co-implant) have stabilized the EOR defects. However, the TEM reveals no significant variations in terms of defect population between these two samples with the same anneal condition. In the case of 25 keV N co-implant, the density of the defects is found to be higher than the B only control case, but the observed minor TED suppression at high temperature can be possibly correlated to the change in defect kinetics at the EOR defect band due to the deeper amorphous layer.

4.5 The Impact of N Co-implant on B/BF_2 USJ upon Spike Annealing for USJ Applications

In order to study the applicability of N co-implant for the latest USJ technology, the impact of N co-implant has been investigated under spike annealing. Spike annealing is commonly used in standard device fabrication process (since 0.13 um technology node) with an extremely fast ramp-rate and a spike of peak temperature.

Figure 4.15 shows the B SIMS profiles of the samples with and without N co-implant subjected to spike annealing at 1080°C. Comparing to the B only profiles annealed at 900°C for 60s in figure 4.9, the spike annealed B profiles demonstrate shallower junction tails even though a higher peak temperature, 1080°C, was used. This is simply attributed to the smaller thermal budget of a spike annealing which possesses the faster ramp-rate and shorter peak temperature holding time. It has also been reported that higher the ramping rate could further reduce the dopant TED effect [Agarwal et al, 1999].

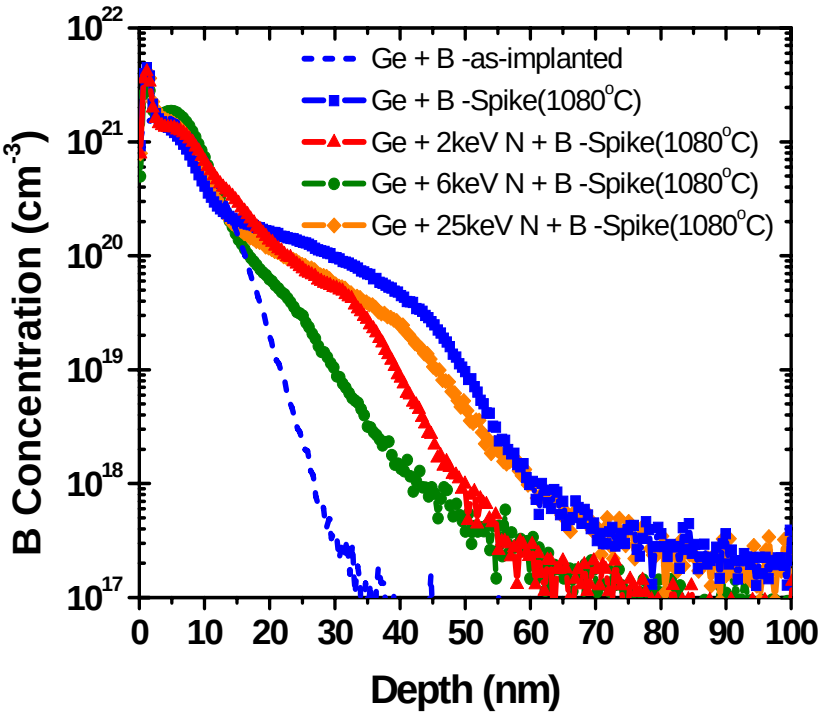


Figure 4.15: SIMS profiles of 1 keV B implant with and without N co-implant at 2, 6 and 25 keV subjected to spike annealing at 1080°C.

Although the depths of these junctions are different from those seen in figure 4.9, the spike annealed B profiles show very similar trends to the samples processed

with isochronal soak annealing under the influence of N co-implant. The 6keV N co-implant is among the most effective conditions in suppressing the B TED, resulting in the shallowest B profile followed by the 2keV and 25keV N co-doping conditions. The observation suggests that the mechanisms involved behind the impact of N co-implantation are similar to what has been demonstrated and shown regardless of the thermal budget. For instance, both the B-N complex and NV cluster formation during the SPER continue to be the key factors affecting the diffusion of B.

Figure 4.16 shows the SIMS profiles corresponding to 3 different co-implanted N atom distributions.

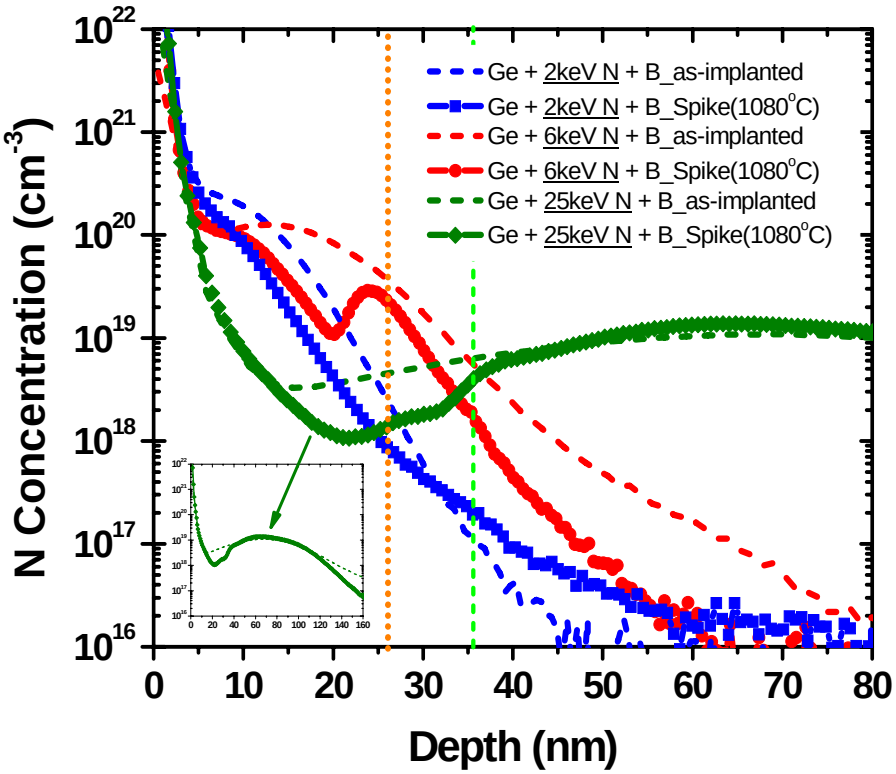


Figure 4.16: SIMS profiles of 2, 6 and 25 keV N implant before and after subjected to spike annealing at 1080°C.

There is a severe N out-gassing effect taking place during the annealing, resulting in smaller amount of N dose retained in silicon across the different N co-implant conditions. For the case of 2keV N, a N-trapping free profile is obtained with a smooth transition around the a/c interface, comparing to the earlier case where a clear dopant trapping peak is observed at 800^{o}C isochronal annealing for 60s (figure 4.11). This provides indirect evidence that the spike annealing could have dissolved most of defects at the EOR region.

A high concentration N trapping is clearly shown with the 6 keV N co-doping. The depth of the trapping peak is located before the a/c interface, which is nearly identical to the profiles obtained with 2 other anneal conditions (in figure 4.11). Therefore, the occurrence of the N trapping peak can be taken as evidence of the NV cluster formation during the spike annealing. The NV clusters are believed to have effectively reduced the silicon supersaturation by reacting with the emitted interstitials from the EOR region, and thus it further suppresses the B TED in the 6 keV N case during the annealing with respect to the 2 keV N co-implant.

With the 25 keV N co-doping, the spike annealing demonstrates N diffusion profile similar to the isochronal soak annealing. The inset in the figure 4.15 covers the whole distribution range of the as-implanted and annealed 25 keV B profiles. No significant feature has been observed from these profiles except the typical N out-gassing effect. Thus, it has the smallest effect on the B diffusion among the 3 N co-implant conditions.

BF_2 has often been used in manufacturing instead of B to increase the productivity due to its advantage of higher atomic mass. Hence, N co-implant was

also investigated to study its effect on the BF_2 implanted samples. Figure 4.17 shows the B profiles of the BF_2 with and without a 6 keV N co-implant processed with spike annealing at 1080°C. Compared to the B case, the BF_2 implant reveals a shallower junction profile under the same anneal condition. This has been generally reported and attributed to the retardation of B diffusion by the F atoms in the BF_2 species [Cowern et al., 2005a, 2005b, Boninelli et al., 2007, Downey et al., 1998]. A further B TED suppression has been observed when the 6 keV N co-implant is inserted prior to BF_2 implant.

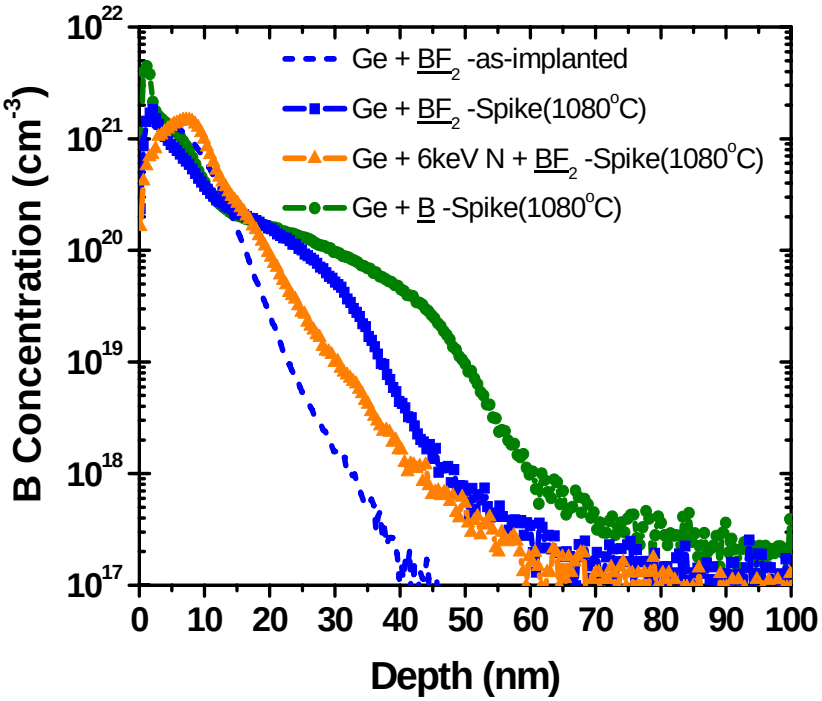


Figure 4.17: SIMS profiles of 5 keV BF_2 implant with and without N co-implant at 6 keV after spike annealing at 1080°C. The spike annealed B only profiles is also included for reference.

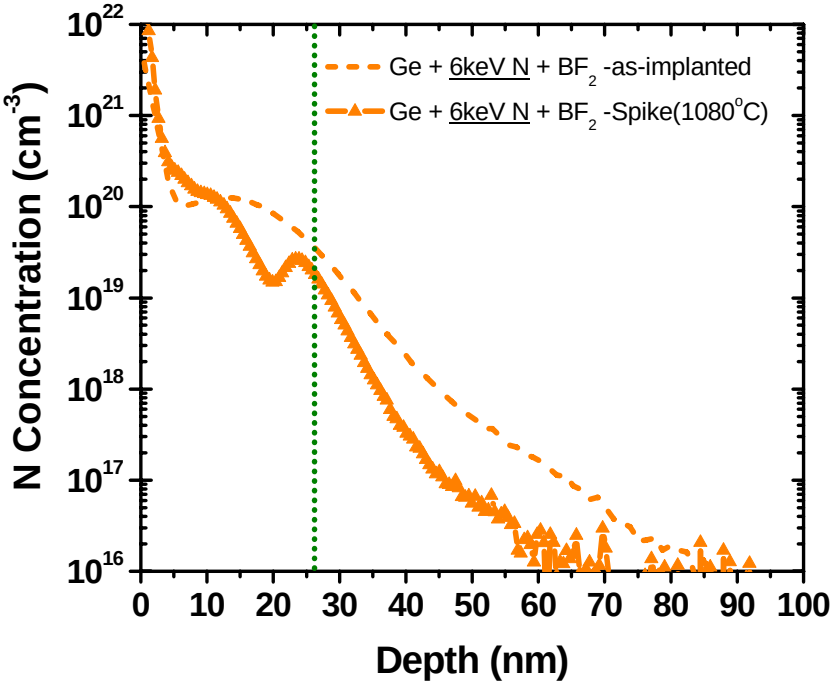


Figure 4.18: SIMS profiles of 6 keV N implant before and after subjected to spike annealing at 1080°C.

Referring to its N profile in figure 4.18, an identical N trapping peak is still remaining before the a/c interface when the N co-implanted sample is subjected to spike annealing. This re-affirms the existence of the proposed NV cluster formation mechanism although a more complex scenario could be involved with the F atoms from BF_2.

The R_s values of the above spike annealed samples are shown in figure 4.19. On the B doped sample, the two lower N implant energies (2keV & 6 keV) have higher R_s, while the 25 keV N case has lower R_s, comparing to the B only reference sample. Since it has been shown in the SIMS results (figure 4.15) that the B junction depths of 2keV and 6 keV N conditions have changed, the higher R_s values of these

two samples cannot be attributed directly to the result lower dopant activation but could be possibly due to their shallower junctions.

With a more in-depth analysis (shown in 4.15), it is found that 2 keV N has a final deeper doping than 6 keV N. Theoretically, assuming the same activation level, the deeper junction will contribute to the lower R_s value. However, since the 2 keV N co-implant shows higher R_s with a deeper junction depth, it is thereby deduced that the dopant activation level of the resulting junction is lower than the 6 keV N co-implant and attributed to the B activation restriction due to the B-N complex formation. The B-N complex formation is proposed to be the main driving force for the B TED reduction in the smallest N implant energy case (2keV N), which has been described above. For the 25 keV N, it is verified that the amorphous layer has been deepened by the N co-implant. Hence, the thicker amorphous region is recrystallized and goes through the SPER, which enhances the dopant activation level and lowers the R_s with respect to the reference B sample case.

The F atoms in BF_2 have retarded the B TED (shown in figure 4.17) resulting in a shallower B doped junction. In addition, it has also been reported that F may possibly interact with B for B-F pairing; therefore, this may account for the higher R_s for BF_2 than for the B doped samples. Similarly, the 6 keV N co-implant in the BF_2 sample has resulted further increase in R_s compared to that in the B only implanted sample.

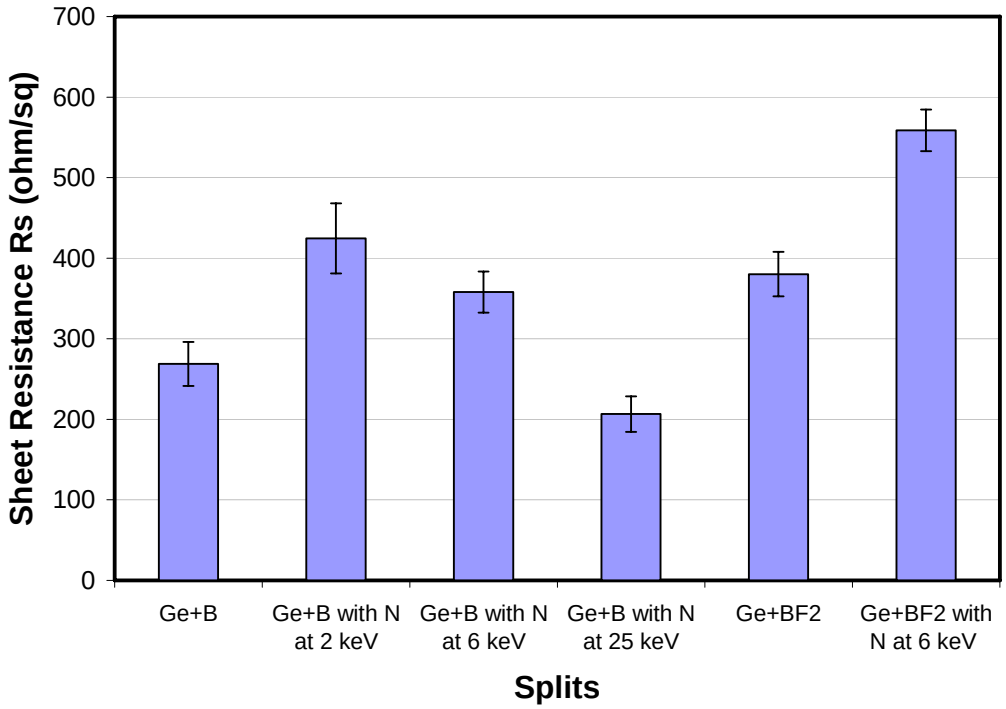


Figure 4.19: The sheet resistance (R_s) values of the Ge-PAI B/ BF_2 junctions with and without N co-implant when subjected to spike annealing at 1080^{o}C.

Indeed, the effect of N co-implant on the B junction formation cannot be easily evaluated based on a single junction parameter. For instance, some N co-implant conditions are effective in B TED suppression, but it increases the R_s of the resulting junction as shown above. In order to better quantify the effect of various N co-implant conditions, the results of the R_s as a function of junction depth (X_j) (at 5×10^{18} cm^{-3}, defined for 65nm technology and above, where this is the concentration level at which the acceptors is equaling to the donors) is plotted in figure 4.20. In addition, the universal R_s/X_j curve for B/BF_2 based on spike annealing, which obtained from the ITRS roadmap projection, is also inserted in same figure for comparison. The R_s/X_j universal curve represents how would the B/BF_2 responses to

the R_s at a particular depth junction or vice verse, when the B/BF_2 implant energy or spike anneal temperature are varied.

Both spike annealed B and BF_2 samples conform well with the universal R_s/X_j curve, suggesting that there is a physical dopant activation limitation with respect to the junction depth. Interestingly, it is observed that the data points can shift distinctly in different directions under the various N co-implant conditions. On the co-implanted B samples, one would observe that besides the 2keV N the other 2 conditions (2 keV and 25 keV) show favorable shift to the left of the curve. The unfavorable R_s/X_j behavior in the 2 keV N could probably attributed to the extensive B-N interactions during the junction formation, thus reducing dopant activation level significantly though a shallower junction can be achieved. The 6 keV N co-implanted B case can be considered as an optimum case, which can offer a junction with a slightly lower R_s and also a shallower junction depth which can rival the case of the BF_2 under the same spike anneal condition. Converse to the B implanted sample, the BF_2 co-implanted with the same 6 keV N atoms shows a significant reduction in junction depth but it causes extensive increase in R_s, eventually leading to an unfavorable shift in the universal curve. Lastly, the improvement in the R_s/X_j behavior of 25keV N with B case could be largely contributed by the higher extent of preamorphization induced by the high energy N co-implant, which is supported by the evidence illustrated in the previous sections.

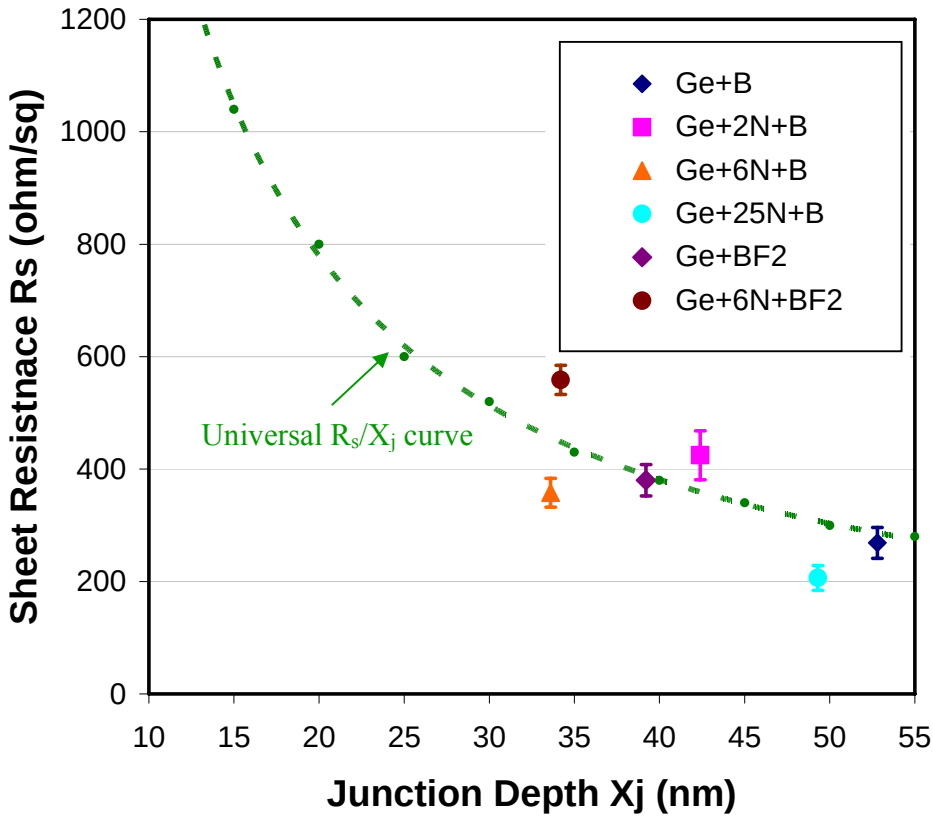


Figure 4.20: The sheet resistance (R_s) as a function junction depth X_j with data points extracted from the SIMS profiles and R_s data of the B/BF_2 samples with and without N co-implant subjected to spike annealing at 1080°C.

4.6 The Study of Nitrogen Co-implant on Electrical Device Performance

As shown in the R_s versus X_j plot of figure 4.20, the condition of N co-implant is playing an important role in determining junction performance. With a careful optimization, the N co-implant could offer improved junction characteristics. Nevertheless, to achieve a better insight and understanding of its impact on the device performance, it is necessary to integrate the optimized N co-doping condition into the device fabrication process.

For instance, both 6 keV and 25 keV N co-implant conditions contribute to favorable R_s/X_j characteristic. Among these two conditions, the 6 keV N case rivals the BF_2 sample with shallower junction depth associated with slightly improved R_s, which is unlike the 25 keV case resulting in a deeper junction. In addition, the 6 keV N does not cause any further amorphization and its diffused N profile has a similar depth of the BF_2. Therefore, this avoids the concern of gate dielectric punch-through in real devices which has been optimized with respect to the amorphization condition of the Ge-PAI. Based on the above considerations, the 6 keV N co-implant with B is used to dope the S/D extension compared with the typical optimized BF_2 S/D extension in standard 65 nm technology devices.

The fabrication of the PMOS follows a typical process flow as shown in figure 4.21.

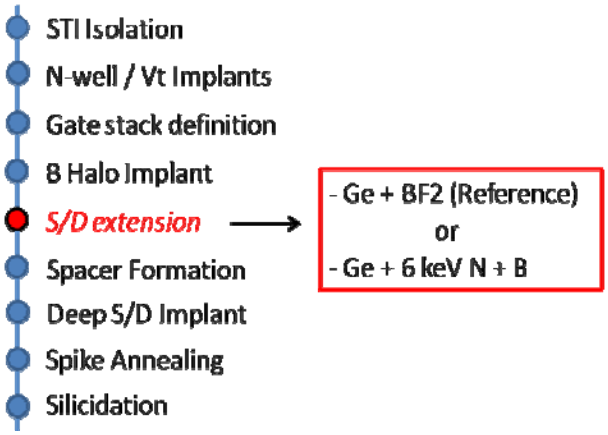


Figure 4.21: Fabrication flow chart of the PMOS transistors.

Ge preamorphization implant was done prior to the BF_2 and the 6 keV N with B implants in S/D extension. The implant energies and doses were same as the blanket study. The spike annealing thermal profile is similar to the condition used in

previous section. With the exception of the S/D extension implant, all other processing steps were kept the same for both of the device splits.

Figure 4.22 illustrates the I_{off} versus Ion behavior of the PMOS. Although the B with 6 keV N co-doping has superior junction properties in X_j and R_s than the BF_2, the fabricated devices with the S/D extension of 6 keV N co-implanted B show electrical performance degradation. The PMOS with N co-implant exhibits ~9% lower Ion at the fixed I_{off} level in the technology curve comparing to the BF_2 reference. The result depicts clearly that the benefits gained from N co-implantation shown earlier cannot be directly and easily translated to the device improvement.

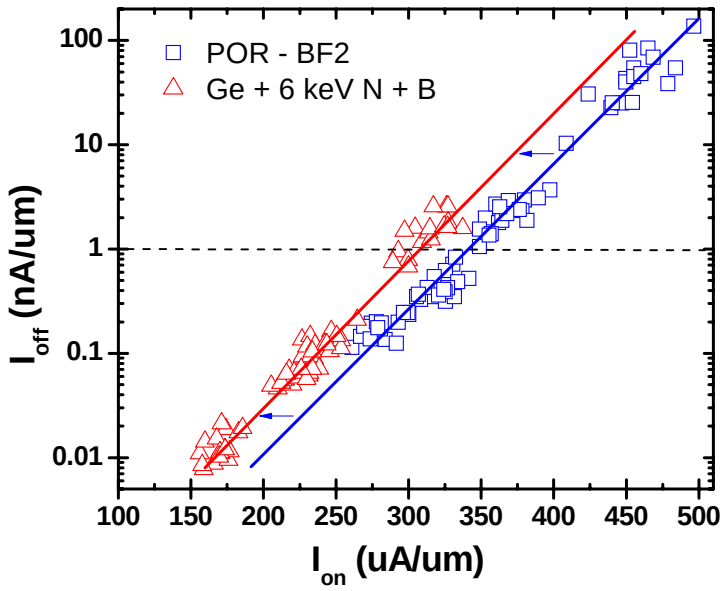


Figure 4.22: PMOS Ion versus I_{off} at V_{dd} of 1.0V. The 6 keV N + B device shows a 9% degradation in Ion at fixed 1nA/um I_{off} compared to the BF_2 reference device.

With a more detailed investigation into the device data, figure 4.23 illustrates that 6 keV N co-implant with B in S/D extension has resulted in a significant drop in overlap capacitance (C_{ov}). It is observed that the N co-implant split has a 15% lower

C_{ov} with respect to the reference device, which is believed to be the root cause for the 9% degradation in the Ion performance shown in the previous figure. The C_{ov} represents the gate overlap with the extension junction profile; hence it can be correlated to the extent of lateral diffusion of the S/D extension dopant profile. The sharp reduction in C_{ov} with the N co-doping split thus indicates that a much less diffused lateral profiles has been achieved compared to the pure BF_2 S/D extension. It is attributed to the B TED suppression in the presence of N, at which physically involving the dominant NV cluster mechanism with the 6 keV N co-implant described in the earlier sections. In addition, the reduction in lateral diffusion is also consistent with the reduction of vertical junction (ΔX_j) when 6 keV N co-implant is implemented in the blanket study shown in figure 4.20.

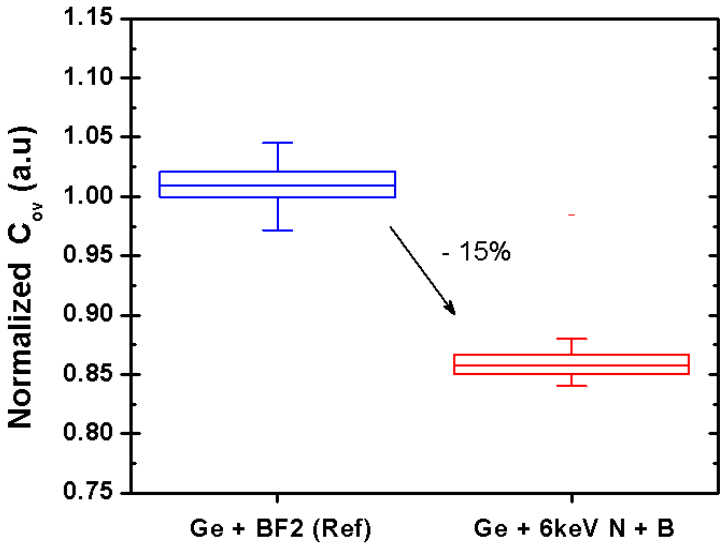


Figure 4.23: Overlap capacitance (C_{ov}) of the 2 device splits. The C_{ov} of device is reduced significantly when the 6 keV N with B is used in the S/D extension.

Figure 4.24 depicts the roll-off characteristic of PMOS for the 2 different splits. It can be seen that the Vt is shifted at the nominal device due to the change in

the B profile in the extension as a result of N co-doping. In addition, the 6 keV N implant does strongly improve the threshold voltage device control for the minimal gate length, leading to a smaller roll-off and a better short channel effect control.

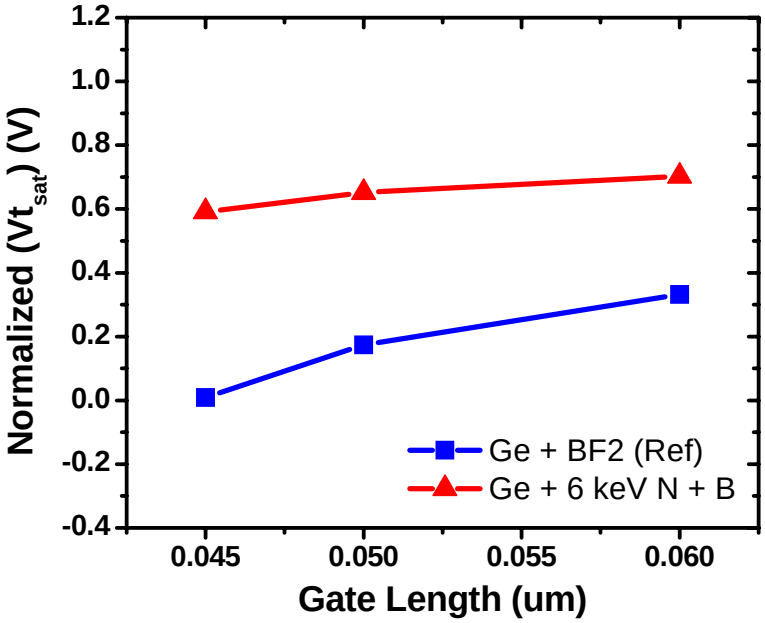


Figure 4.24: Vt_{sat} roll-off characteristic as a function of gate length, comparing devices with Ge + BF_2 (POR) to the Ge + 6 keV N + B S/D extensions.

So far, the device results shows no clear improvement in the I_{on}/I_{off} electrical performance by applying the optimized 6 keV N co-implant into the S/D extension of the transistor compared to the standard BF_2 reference. This can be simply explained by the serious degradation of other electrical parameters, in this case the huge C_{ov} reduction, which overrides the R_s/X_j advantages gained by the optimized N co-implant in the S/D extension junction. Despite the degradation in I_{on}/I_{off} performance, the significant C_{ov} reduction also signifies the gain in reduced lateral diffusion. On the other hand, the N split is shown to have helped in the roll-off behavior improvement

for the PMOS devices. Therefore, this shows a great extent of potential with N co-implant approach in achieving the reduced SCE devices. Nevertheless, more in-depth optimization effort, such as re-tuning the Halo and extension profile to bring back the similar Vt_{sat} and slight change in C_{ov} is necessary to reveal the effect of the N co-implant in PMOS devices.

4.7 Summary

In summary, a deeper physical understanding on the interactions among N atoms, dopants and extended defects has been obtained based on the impact of N co-implant on B diffusion and deactivation behaviors. Both the physical and electrical data confirm that the location of co-implanted N atoms with respect to B profile and EOR defect distribution plays a significant role towards the optimum USJ properties. The study from this chapter suggests that co-implanting N atoms with projected range located in between B profile and EOR defect distribution can offer the best optimum effect on the B TED and dopant de-activation suppression, as well as possibly affecting its EOR defect population. The potential of N co-implant for USJ fabrication in PMOS devices has also been studied and demonstrated in terms of the R_s/X_j performance as well as the reduction of lateral junction diffusion in the devices towards the better control in SCE.

Last but not least, this work has provided an insight, not all, but at least part of the clarifications on the effects and possible involved mechanisms of N co-implant in B USJ formation, which is currently lack of consensus view.

Chapter 5

Understanding of Carbon/Fluorine Co-implant Effect on Boron USJ Formation

5.1 Introduction

At present, co-implantation of impurities, such as Carbon (C) or Fluorine (F) atoms, in pre-amorphized substrates is of much interest since no complex or additional process is required [Augendre et al., 2006, Vanderpool et al., 2005, Graoui et al., 2005, Pawlak et al., 2006a]. In addition to the gain from TED reduction, suppression of dopant deactivation has also been successfully demonstrated, producing not only highly active but relatively stable shallow junctions [Pawlak et al., 2006b, Cowern et al., 2005a, 2005b]. The key principle that is exploited arises from the inhibition of interactions between dopants with the defects introduced by implantation in the presence of C/F atoms.

Various mechanisms involved in co-implantation have been proposed. In general, it is known that C forms carbon-interstitial clusters, C_mI_n [Mirabella et al., 2002], while F reacts with vacancy point defects and forms F_mV_n clusters, which are subsequently annihilated by interstitials from the end-of-range (EOR) to release the F atoms [Cowern et al., 2005a, Impellizzeri et al., 2004]. Thus, co-implanted C/F serve as sinks in different forms, but both employ the interstitial trapping mechanism which is a promising approach to eliminate TED of B. Though controversy has existed over

the years on the details of the clustering/reaction pathways, it has been clearly demonstrated that C/F co-implant could provide a significant physical and electrical improvement in USJ formation [Graoui et al., 2005, Pawlak et al., 2006a].

The incorporation of metal gate, high-k dielectric materials and strained silicon in sub-32 nm devices give rise to the concern of thermal stability [Kwong, 2005, Song et al., 2006]. Therefore, the junction stability associated with C/F co-implant is a key property that needs to be characterized for application in advanced devices. Besides, low temperature junction activation process may become one of the challenges in future USJ. A promising way to achieve this is to use the pre-amorphization and low temperature solid phase epitaxial re-growth (SPER) scheme. However, extensive residual defects form at the EOR region in this process. Therefore, C/F co-implant with low temperature annealing has become an important alternative because it has been shown previously that the co-implant scheme could help in removing extended defects [Simpson et al., 1995].

In this work, an extensive study of C/F co-implant for the formation of B USJ during isochronal soak annealing has been investigated. The obtained results are discussed in terms of the interactions among the dopants, defects and co-implanted impurities. Also, the effectiveness of C/F co-implant towards the suppression of B TED and de-activation in the B/BF_2 junctions are evaluated and discussed. For instance, the soak annealed dopant diffusion profiles from low to high temperatures are also compared to that obtained from spike annealing. Besides the B TED, junction electrical characteristics and low temperature post-annealing residual defects for the co-implanted junctions are of interest. Part of the results from the previous chapter on

N co-implant study will be used for comparison with the C/F co-implant in this chapter.

5.2 Experimental Details

Experiments were performed on 12 inch n-type, 300 mm, <100> Cz silicon wafers with resistivity of ~10-25 ohm.cm. All wafers were first pre-amorphized with Ge ions at energy of 15 keV to a dose of 3×10^{14} at/cm^2. This was followed by the implantation of C at energy of 4 keV or F at energy of 10 keV to the same dose of 1×10^{15} at/cm^2, and subsequently with B implanted at energy of 1 keV to a dose of 1.5×10^{15} at/cm^2. A second set of wafers was implanted with C at the previous condition followed by BF_2 implantation at energy of 5 keV to a dose of 1.5×10^{15} at/cm^2. The implant energy of BF_2 was chosen based on mass ratio between B and BF_2, 1/5 (~11/49) to produce as-implanted profile identical to the B 1 keV profile. All implants were performed at 0^o tilt and 0^o twist angles on Varian VIISta 80HP high current ion implanter.

The wafers were subsequently annealed for 60s by Uniaxis Addax XM80 RTA system for the isochronal annealing study, with temperature ranging from 650^{o}C to 1000^{o}C. The ramp-up and ramp-down rates are 60^{o}C/s and 45^{o}C/s, respectively. Spike annealing was performed at 1080^{o}C in Applied Vantage Radiance RTA system with the ramp-up and ramp-down rates of 250^{o}C/s and 75^{o}C/s, respectively.

The chemical dopant (B) and impurity (C/F) profiles were analyzed by secondary ion mass spectrometry (SIMS) using CAMECA IMS 6F/WF. Oxygen primary ions (O2+) with net energy at 500 eV were employed to scan the B profiles;

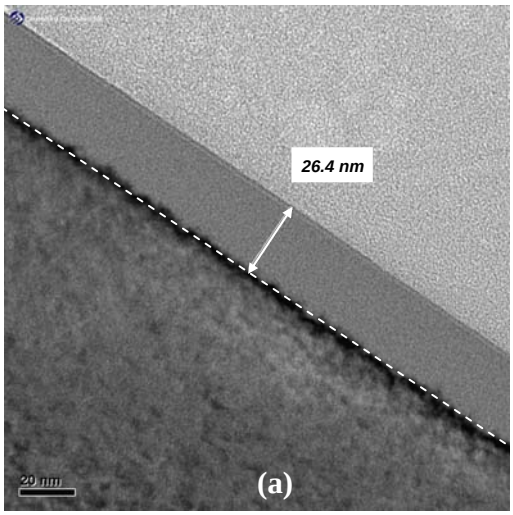
while Cesium (Cs+) primary ions with net energy at 3 keV were used for the C and F profiles. The incident angle for the primary ions were 56^{o} and scanned over an area of 250 μm × 250 μm. Sheet resistance (R_s) measurements were carried out on a standard four point probe and Hall Effect measurements were done using HL 5500 Accent equipment to obtain the active carrier concentration (N_s) and mobility (μ_s). Transmission electron microscopy (by JEOL 2100) was performed to analyze the extent of amorphization, and to investigate the evolution of EOR defects.

5.3 The Initial As-implanted Conditions

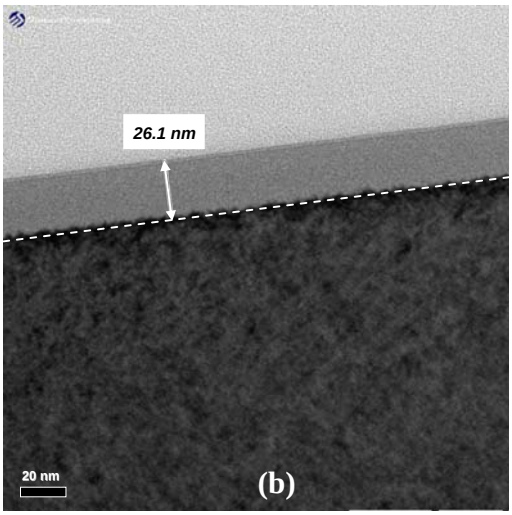
The dose and energy of C/F co-implant and amorphization schemes have been found to play significant roles in achieving optimum effect on B doped junctions [Graoui et al., 2005, Pawlak et al., 2006a]. In this work, C/F were co-implanted to the location approximately around the middle range in between B/BF_2 peak concentration and the preamorphized amorphous/crystalline (a/c) interface, below which is the location EOR defects upon annealing.

The amorphization depths were obtained and measured from XTEM micrographs. Figure 5.1(a) is the XTEM of the Ge + B sample with an amorphous layer approximately ~26 - 27 nm being induced by the Ge implant. When C is co-implanted, figure 5.1(b) shows its amorphous layer remains to be around the same thickness. Similar observations are also applied to the cases for Ge + BF_2 and Ge + C + BF_2, their amorphization extent are also approximately ~ 26 - 27 nm, which is defined by the Ge-PAI (shown in figure 5.1(d) and (e)). The amorphous thickness only varies for the case of F co-implant on B sample, figure 5.1(c) shows its

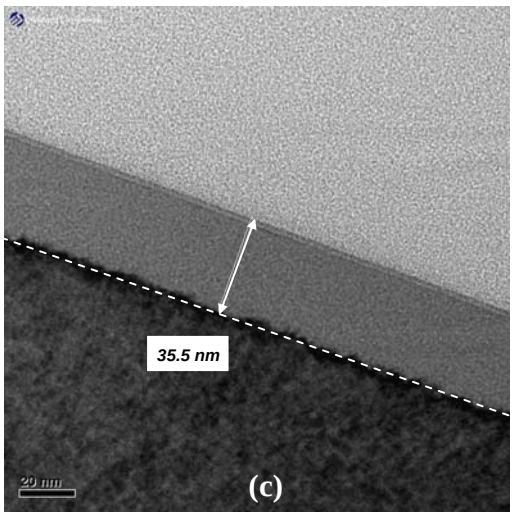
amorphous layer is increased to ~ 35 - 36 nm. It is attributed to the extension of amorphization induced by the F co-implant condition on top of the Ge-PAI.



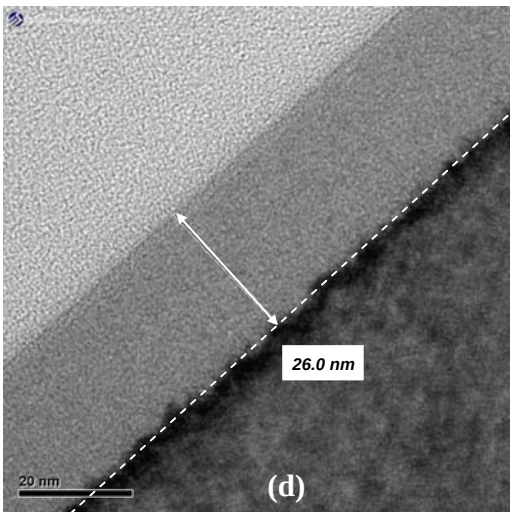
Ge + B



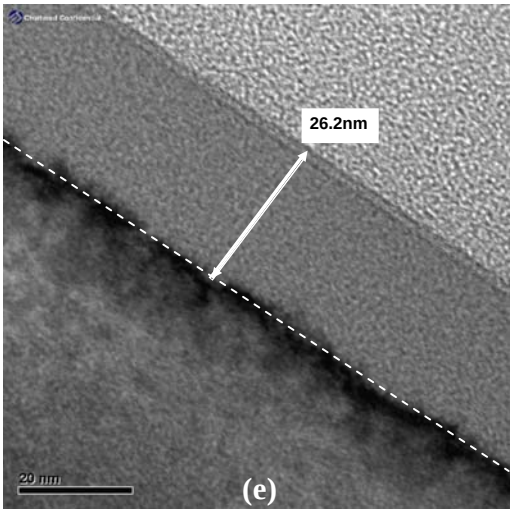
Ge + C + B



Ge + F + B



Ge + BF_2



Ge + C + BF_2

Figure 5.1: XTEM for the as-implanted samples with (a) Ge + B, (b) Ge + C + B, (c) Ge + F + B, (d) Ge + BF_2 and (e) Ge + C + BF_2.

The as-implanted profiles for the C on B/BF_2 and F on B are shown in figure 5.2(a) and 5.2(b), respectively. The depths of the amorphization obtained from XTEM are inserted in the figures for reference. Figure 5.2(a) reveals that the B and BF_2 implants have nearly identical B dopant distribution in high concentration portion within the amorphous layer after mass ratio conversion (~1/5) for the implant energy. However, dopant channeling can be seen for the small mass B implant in the bulk crystalline region beyond the a/c interface, which results in a deeper tail profile than the BF_2. Nevertheless, the results in the two figures clearly confirm that the projected range or peak concentration of the co-implant impurities, either the C or F atoms, is located between the peak of B profile and the distribution of EOR defects.

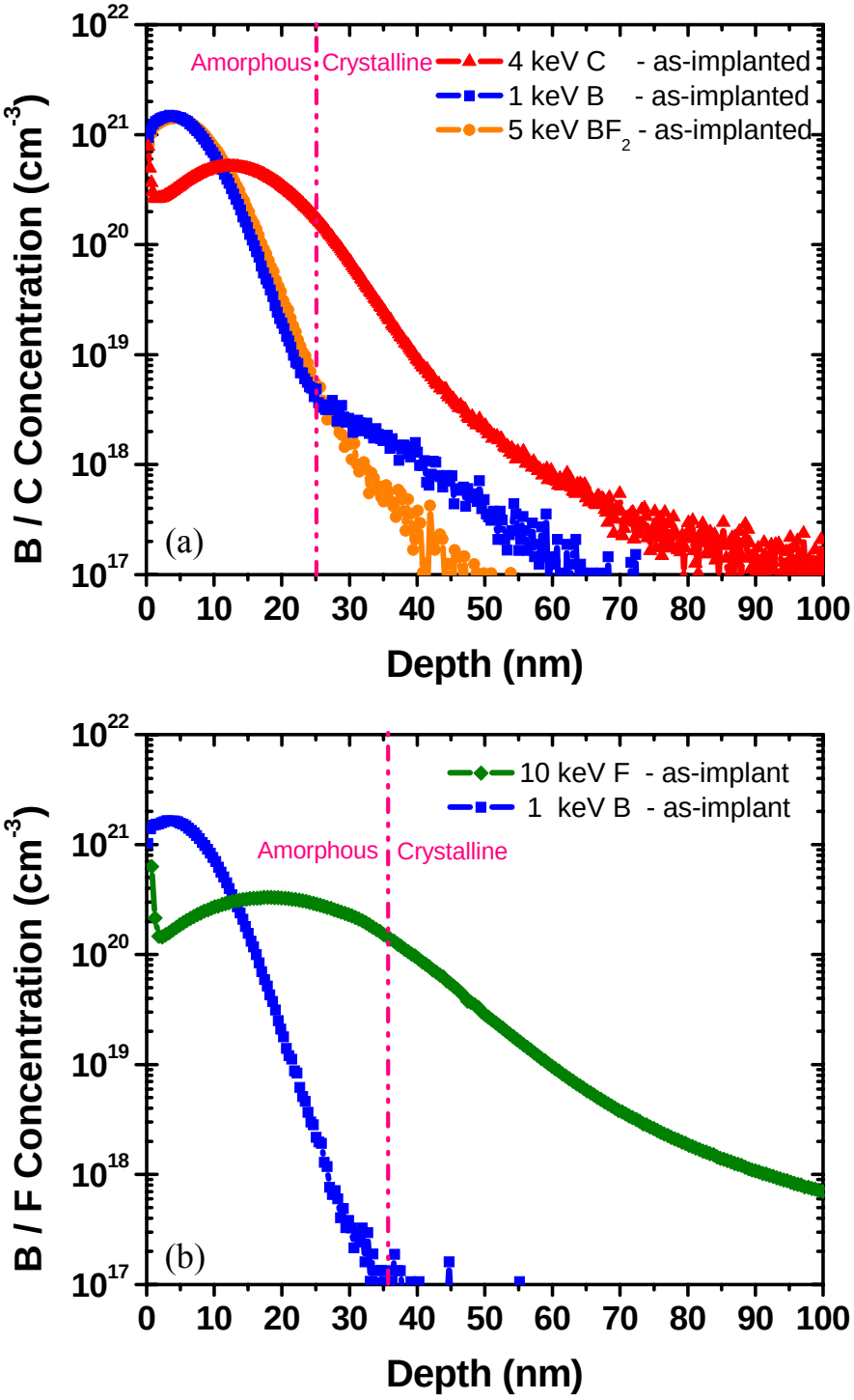


Figure 5.2: SIMS depth profiles for various as-implanted (a) 4 keV C / 1 keV B / 5 keV BF_2 and (b) 10 keV F / 1 keV B with 15 keV Ge-PAI.

5.4 Diffusion Anomalies

Figure 5.3(a) and (b) shows the various samples subjected to annealing at 750°C for 60s.

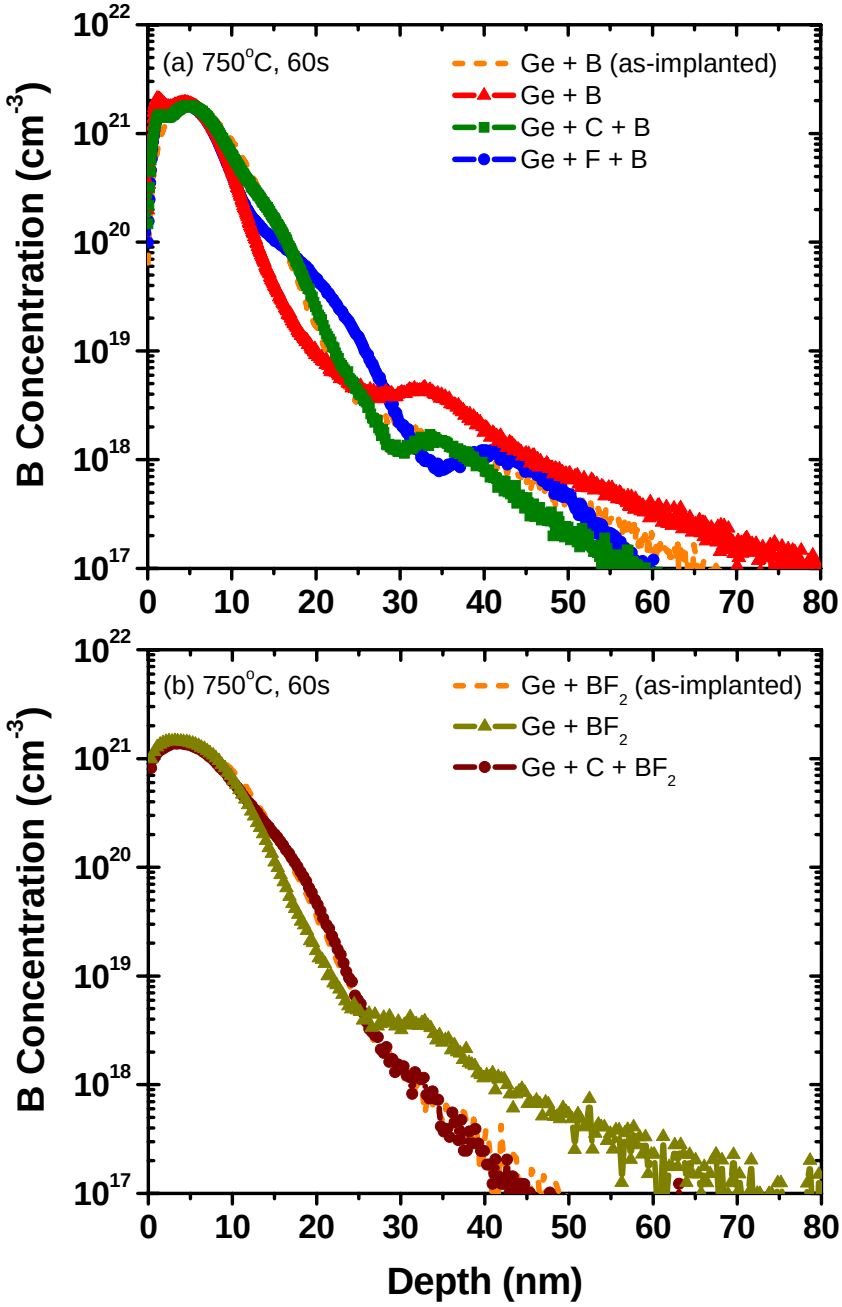


Figure 5.3: Comparison of B SIMS profiles showing the effect of (a) C/F co-implant on Ge + B and (b) C co-implant on Ge + BF_2, subjected to annealing at 750°C for 60s.

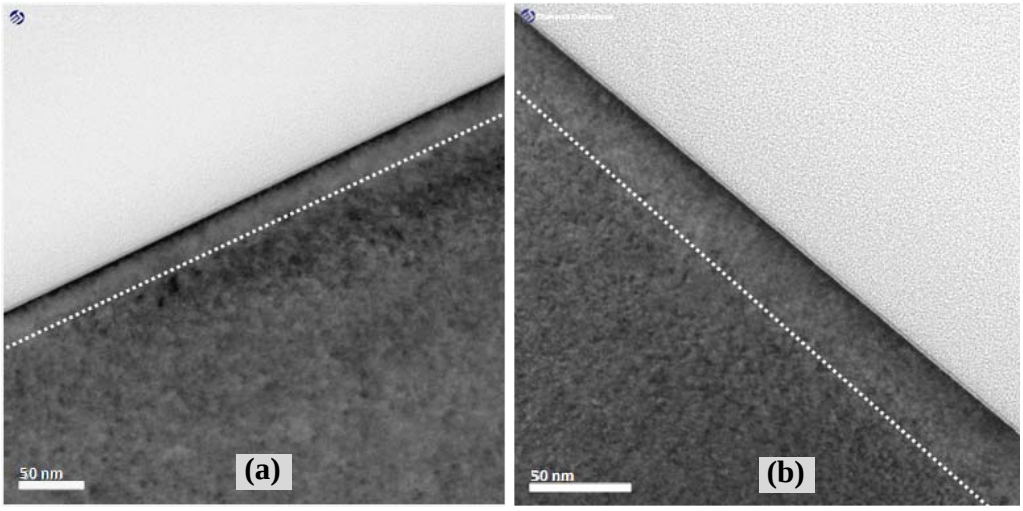
SPER of amorphous silicon with crystal seed layer beneath is reported to take place above 600^{o}C, hence the amorphous layers of these samples are expected to undergo the full re-crystallization and proceed with dopant activation at the same time [Colombeau et al., 2004b]. In the control Ge + B sample, the implanted B atoms show the well-known uphill diffusion phenomenon. The high B concentration portion (C_{boron}>5×10^{18}cm^{-3}) has moved towards the silicon surface, resulting in shallower profile than the as-implanted B [Duffy et al, 2003, Wang et al., 2001]. The underlying cause is attributed to the (a) inherent hopping characteristic of B and (b) the driving force induced by the emitted silicon interstitials from the EOR band towards the surface. Despite dopant uphill diffusion, a deeper tail profile at the low concentration region (C_{boron}<5×10^{18}cm^{-3}) is observed in the figure as a result of the interactions between B atoms and emitted silicon interstitials from EOR region, yielding the B TED phenomenon. Figure 5.3(b) shows the Ge + BF_2 reveals similar dopant surface directed movement and tail enhanced diffusion.

Interestingly, with C co-implanted and being positioned between peak of doping profile and EOR defect band, B uphill diffusion and TED diminish in both B (figure 5.3(a)) and BF_2 cases (figure 5.3(b)). The result suggests that the C atoms have reduced the interstitial flux induced by the emission of silicon interstitials from the EOR region, which prevent the interactions of the interstitials with the B atoms. For F co-implant prior to B doping (figure 5.3(a)), the diffusion of B in the tail is also suppressed at the anneal condition of 750^{o}C. Unlike the C co-doping, the broadening of B profile with respect to the as-implanted B distribution is observed between the 1×10^{18} cm^{-3} to 1×10^{20} cm^{-3}. This is attributed to the enhanced B diffusion in the

amorphous region or possibly the slower SPER in the presence of F atoms [Jacques et al., 2003, Duffy et al., 2004].

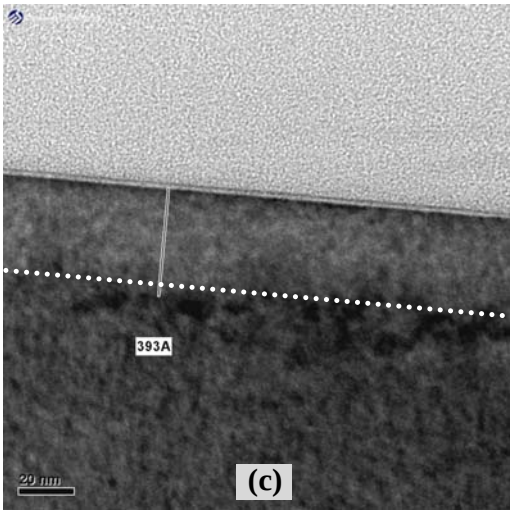
Another noticeable feature due to the pre-amorphization is the dopant trapping at the EOR defect band. The B trapping peak can be found in the Ge + B SIMS profile as illustrated in figure 5.3(a). The location is just below the a/c interface caused by Ge-PAI. The peak of the B trapping approaches a high concentration up to 5×10^{18} cm^{-3}.

Figure 5.4(a) shows the corresponding XTEM image with same anneal condition at 750^{o}C for 60s. A dark band, the EOR defect band, located directly below the a/c interface can be clearly observed. However, the EOR defects are not visible when C is added to the doping scheme in figure 5.4(b). Similarly, a smaller and lower dopant trapping peak (~1.5×10^{18} cm^{-3}) is observed in the B dopant profile of the same sample (Ge + C + B in figure 5.3(a)). Although it is not observable from the XTEM image above, it is possible that some smaller size defects still remain but are out of the detectable range of the microscopy. Nevertheless, with reference to both the TEM and SIMS, it can be clearly stated that the amount of extended defects can be significantly reduced by the C co-implant at low anneal temperature.



Ge + B

Ge + C + B



Ge + F + B

Figure 5.4: XTEM micrographs showing the annealed samples at 750^{o}C for 60s with (a) Ge + B has clear EOR defects, (b) Ge + C + B has no visible defects around the EOR region and (c) Ge + F + B has deeper and wider EOR defect band. Dotted lines are drawn to show the a/c interfaces.

The F co-implant shows a deeper depth of B trapping peak in figure 5.3(a). Its location is just right below the deeper a/c interface of the F co-doped as-implanted sample. XTEM image in figure 5.4(c) shows that the extended defects are still clearly

showing up with the F co-implant upon annealing though its B trapping peak concentration is at a similar level as the C co-implant.

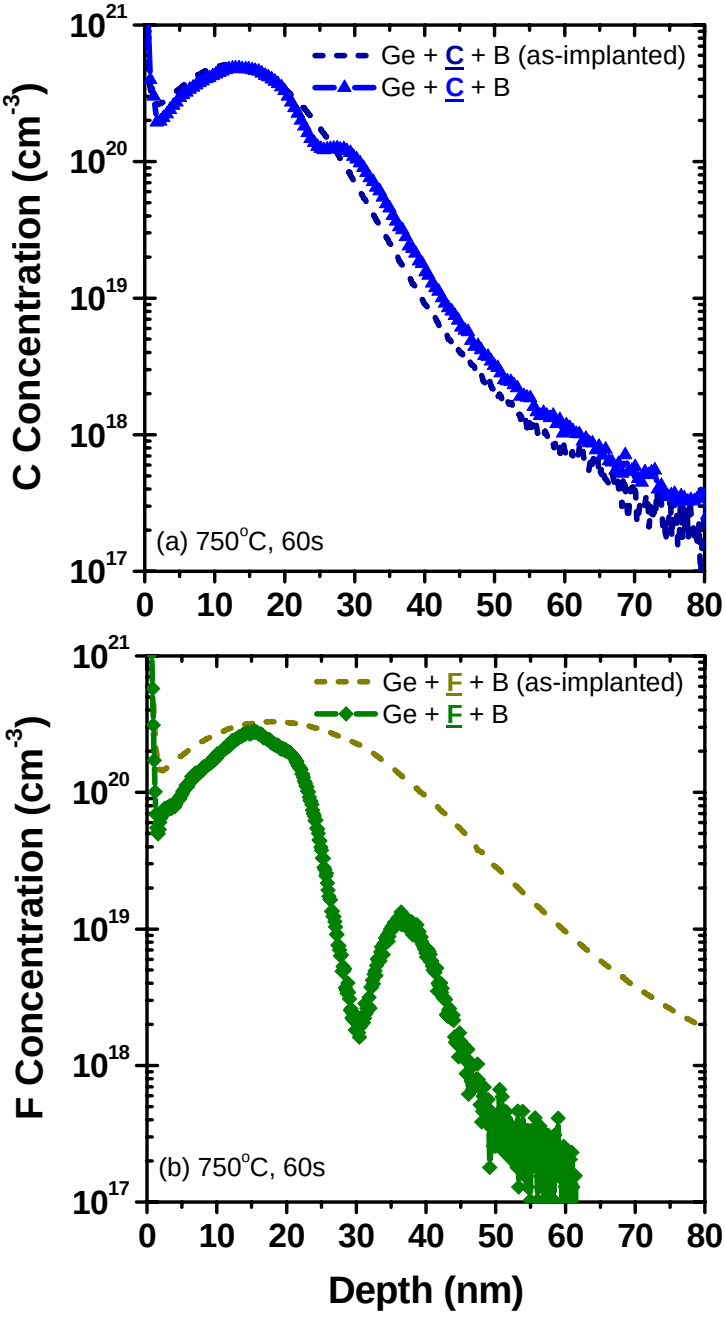


Figure 5.5: SIMS profiles of (a) C and (b) F co-implant on Ge + B samples before and after subjected to annealing at 750°C for 60s.

However, a much higher dopant out-diffusion is seen for the co-implanted F than the C atoms after annealing, as illustrated in their SIMS profiles shown in figure 5.5(a) and (b). In addition, the impurity trapping of peak C (at the depth of ~ 28 - 30 nm) is at a higher concentration than the F (at the depth of ~ 28 - 30 nm), suggesting that C atoms interact efficiently with the point defects at EOR region thereby suppressing the agglomeration of silicon interstitials into extended defects. This could be the possible reason to explain why the B trapping peak is at similar concentration level but showing significant higher density of EOR defects (figure 5.4(b) and (c)) in the case of F compared to the C co-implanted Ge + B sample.

For Ge + BF_2, the shape of the dopant trapping peak around the a/c interface is somewhat different from that observed in the Ge + B, with a smaller overall area. This result is mirrored by less significant EOR defect band seen from the XTEM (in figure 5.6(a)).

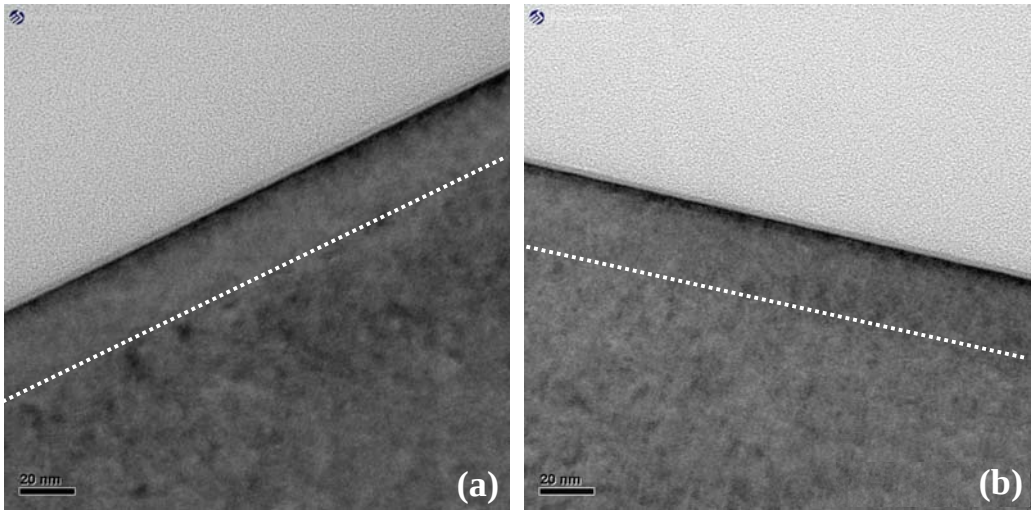


Figure 5.6: XTEM micrographs showing the annealed samples at 750^{o}C for 60s with (a) Ge + BF_2 has minor detectable defects at EOR defects and (b) Ge + C + BF_2 has no observable EOR defects formation. Dotted lines are drawn to show the a/c interfaces.

Since B profile of the annealed BF_2 with C co-doping overlaps with the B profile of the as-implanted Ge + BF_2, no kink or trapping peak can be traced; also a clean crystalline region is seen in XTEM micrograph (figure 5.6(b)). Once again, this agrees well with the result of the Ge + B, indicating that C could inhibit B trapping at the a/c interface and therefore leading to a reduction of extended defects at the same thermal budget.

For a higher thermal budget (850^{o}C for 60s), all the annealed B dopant profiles show no observable B dopant trapping around the a/c interface region (figure 5.7(a) and (b)), suggesting that the defects could have been dissolved and releasing silicon interstitials that causes B diffusion in the tail. Comparing to the B dopant profiles across the different splits, the reference Ge + B shows the deepest junction depth among all the splits due to the great extent of TED as a result of the interstitial emission from the EOR region. Slight reduction (~3 nm at 1×10^{18} cm^{-3}) in the B junction depth is seen with F co-implant. In contrast, the C atoms are more efficient in suppressing the B TED evidenced by the negligible dopant diffusion in the tail (at 1×10^{18} cm^{-3}) with respect to the as-implanted B profile.

A similar trend is also observed for BF_2, in which B TED of B in BF_2 is effectively suppressed when the C atoms are being located in the middle range between the peak of BF_2 and EOR defect band. Figure 5.7(b) illustrates that the non-diffuse B tail profile of BF_2 in the presence of C atoms (Ge + C + BF_2) after being subjected to annealing at 850^{o}C for 60s. On the other hand, without a C co-implant the B profile of the Ge + BF_2 split has diffused about ~12nm deeper (at 1×10^{18} cm^{-3}).

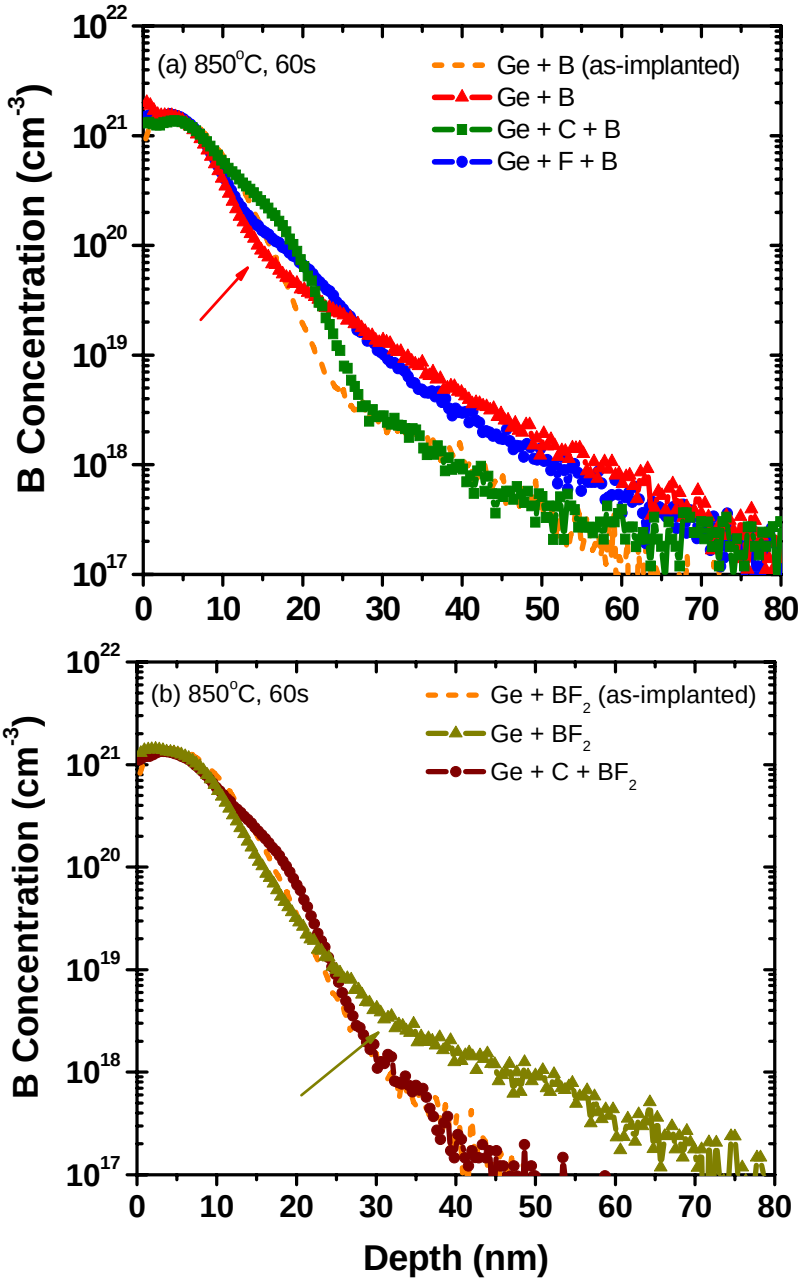


Figure 5.7: Comparison of B SIMS profiles showing impact of (a) C/F co-implant on Ge + B and (b) C co-implant on Ge + BF_2, annealed at 850°C for 60s.

In addition, the F atoms in the BF_2 are believed to have reduced the B activation level, as indicated by the "kink" in its diffusion profile. It is observed that the Ge + BF_2 reveal a B "kink" concentration level at least an order lower than that of

Ge + B and Ge + F + B (in figure 5.7(a)), respectively (Ge + BF_2 at ~5×10^{18} cm^{-3} versus Ge + B at ~5×10^{19} cm^{-3} and Ge + F + B at ~1.5×10^{20} cm^{-3}). This phenomenon has been deduced to be the result of B-F pairing reaction in BF_2 case limits the B activation during the thermal annealing [Colombeau et al., 2004a].

When moving from the soak annealing to the spike annealing at 1080°C, the impact of co-implant on B diffusion becomes more prevalent as seen from figures 5.8(a) and (b). Align with the two previous anneal conditions, a clear suppression on B TED exhibits in the C co-implanted B doped sample, whereas the addition of F co-implant contribute minor gain in junction depth reduction compared to their reference counterpart Ge + B case.

In the case of C co-implant, a plausible explanation for the ~15nm reduction in junction depth with respect to the annealed Ge + B profile (reference at 1×10^{18} cm^{-3}) is the effect of C atoms to trap the silicon interstitials released from the EOR defect upon the spike anneal process. This fits the C trapping mechanism [Moroz et al., 2005, Pawlak et al., 2006a], in which the co-implanted C atoms are placed into the lattice sites during the re-crystallization process, and later the substituted C atoms can effectively react with the emitted silicon interstitials and thereby leads to the formation C_mI_n clusters.

$$C_I + V \leftrightarrow C_S$$

$$C_S + I \leftrightarrow CI$$

$$CI + C_s \leftrightarrow C_2I \quad \ldots\ldots \quad C_mI_n$$

With that, the interactions between the B and Si interstitials are greatly minimized and the suppression of B TED can be effectively achieved. Another contribution to the change in junction depth could arise from the interactions between the C atoms with the EOR defects which later affect the evolution of extended defects. Such a postulation is deduced from the C trapping peak existance around the a/c interface in the C distribution profile seem in figure 5.9(a).

The slight shallower B profile with F co-implant condition is attributed to the F_mV_n clusters formation during the SPER of amorphous layer, acting as traps for interstitials in inhibiting B TED [Diebel et al., 2003].

$$F_I + V \leftrightarrow FV \ldots\ldots F_mV_n$$

$$F_mV_n + I \leftrightarrow F_mV_{n-1}$$

However, it is also suspected that the overlapping between the F and B atoms in their as-implanted profiles (shown in figure 5.2(b)) could result in B-F complex formation [Cowern et al., 2005a, 2005b]. This also slows down the B diffusion. Besides, it is noticed that a large fraction of F is lost after spike annealing due to the inherent F out-diffusion characteristic as shown in figure 5.9(b). Therefore, the co-implanted F atoms are deduced to be not as efficient as the C atoms in trapping the silicon interstitials emitted from the EOR defect band, and also in suppressing the B TED.

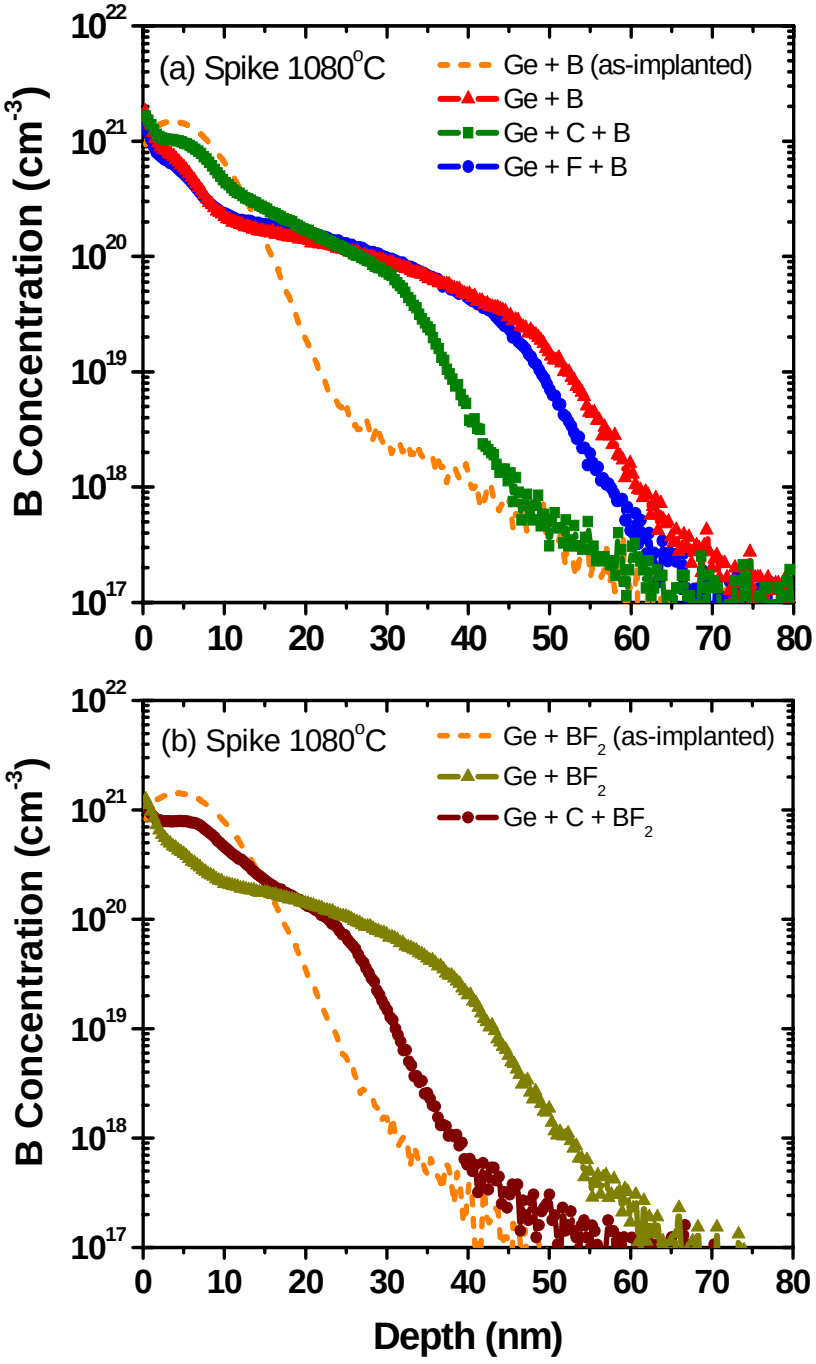


Figure 5.8: Comparison of B SIMS profiles showing impact of (a) C/F co-implant on Ge + B and (b) C co-implant on Ge + BF_2, after fast ramp-up spike annealing (1080°C).

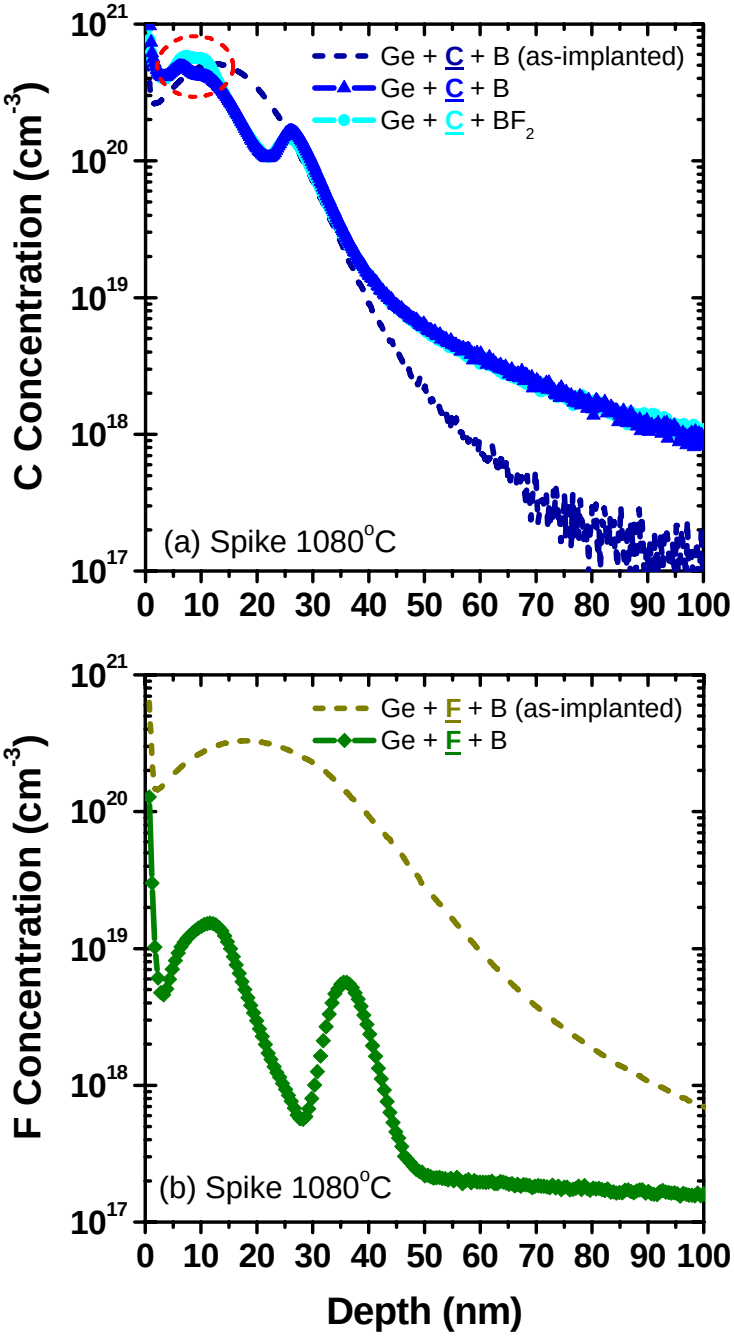


Figure 5.9: SIMS profiles for co-implanted (a) C atoms and (b) F atoms, before and after spike annealing (1080°C).

Figure 5.8 (b) on the other hand shows the various B diffusion profiles of BF_2 when subjected to the same spike annealing at 1080°C. Comparing the BF_2 diffusion

to their B-diffused counterparts in figure 5.8(a) without co-implant, it is seen that the B diffusion is also retarded by the F atoms in BF_2. A further shallower B junction profile is achieved when the C is co-implanted into BF_2. It only diffuses around 5 - 6 nm (reference at 1×10^{18} cm^{-3}) from the as-implanted BF_2 profile after spike annealing and it has the shallowest dopant distributions among all the different conditions illustrated in 5.8(a) and (b). The reduced profile broadening is attributed to the complex interactions of the point defects (interstitials, vacancies) not only with the dopant, but also with C and F atoms at the same time. In addition, it can be observed that there is a difference in the peak concentration of C atoms near to the surface from the C SIMS profiles of C between the Ge + C + B and Ge + C + BF_2 conditions in figure 5.9(a). This peak is around ~9 nm away from the surface and can be corresponded to the stable C_mI_n clusters formed during the spike annealing, suggesting that possibly more C-I reactions occur in the split of Ge + C + BF_2 and thus reducing the B-I interactions during the anneal process. Nevertheless, the role of F atoms from BF_2 should not be neglected for its contribution to the TED suppression. The details of the involved mechanism in the Ge + C + BF_2 are still not clearly understood and required further detail study.

5.5 Activation Anomalies

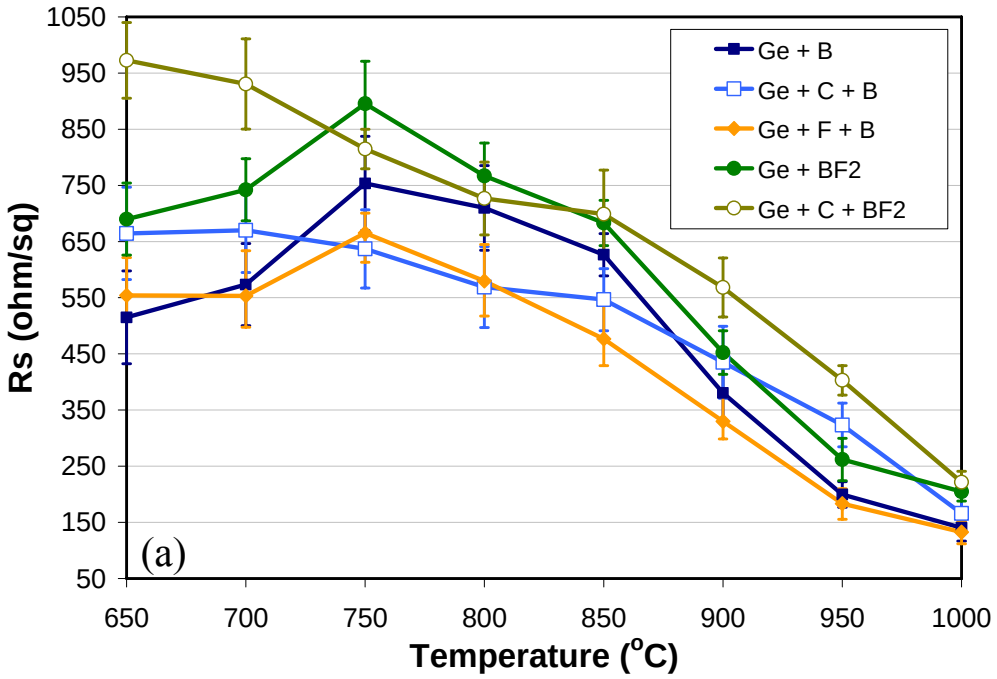
5.5.1 Isochronal Annealing

5.5.1(a) Sheet Resistance

The junction thermal stability evaluated based on de/re-activation studies were performed by isochronal annealing in the temperature range of 650^{o}C to 1000^{o}C for

60s. The obtained data were plotted in terms of R_s values versus the temperature as shown in figure 5.10(a).

The Ge + B (solid square) junction reveals the well known "reverse annealing" effect, in which the R_s is initially small and gradually rises until it reaches a maximum value before it decreases as the annealing temperature is further increased [Colombeau et al., 2004b]. This phenomenon can be described in a stepwise manner: a high level of B activation with low R_s is achieved once the amorphous layer is re-crystallized; this is then followed by nucleation of BICs in the near surface high B concentration region and driven by the interstitials released from EOR defects, resulting in the increase of R_s. The subsequent fall in R_s is a result of the slow process of BICs dissolution after the defects in the EOR band have fully dissolved or ripened into more stable extended defects. The maximum R_s value in the de/re-activation curve is generally defined as the peak deactivation.



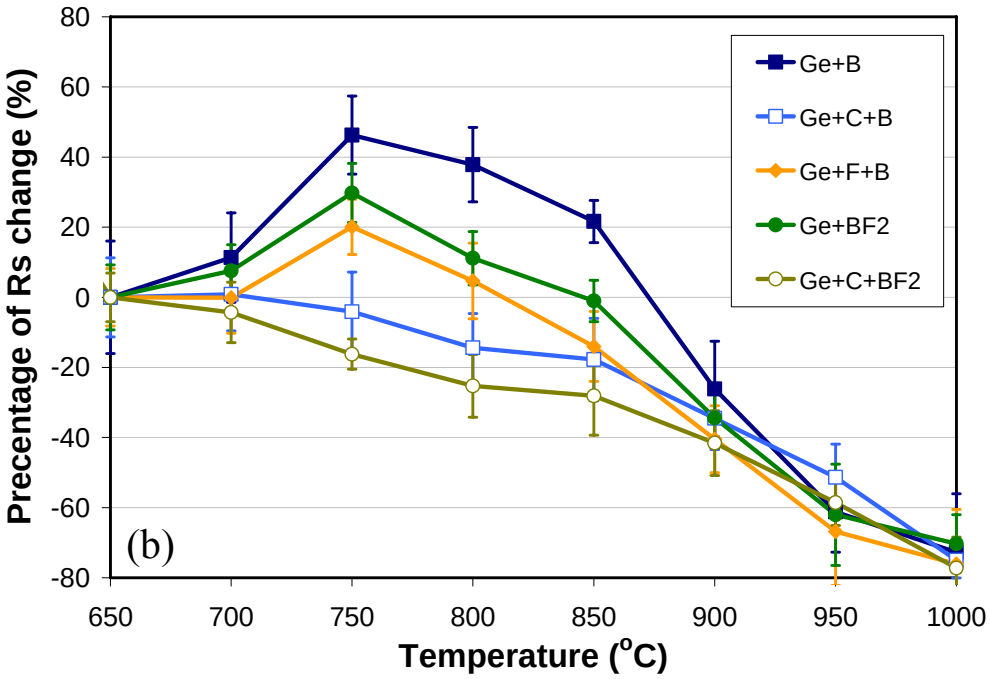


Figure 5.10: (a) Sheet resistance value (R_s) and (b) percentage change of R_s (normalized to the 650°C) as a function of isochronal annealing temperature for 60s to reveal the de/re-activation behavior of pre-amorphized B/ BF_2 junctions coupled with the C/F co-implant.

To further quantify the extent of de-activation, the percentage change of R_s with reference to the annealing temperature at 650°C is also shown in figure 5.10(b). It is observed that the deactivation of B with a typical Ge-PAI used in this study can reach as high as ~50% at the annealing temperature 750°C for 60s.

When C co-implant is incorporated, it is interesting to see that higher R_s value is obtained right after the SPER at 650°C in figure 5.10(a) (open squares). As the temperature is increased, R_s gradually deceases across the temperatures from 650°C up to 1000°C. Referring to figure 5.10(b), one can easily observes that the B deactivation is totally suppressed by C co-implant, leading to the inference that C

atoms can serve as an effective "block" for the back diffusion of interstitials from the EOR band towards the B active layer near the surface region. Hence, it avoids the deactivation of B atoms due to the formation of BICs. The "block" is established through a carbon clustering mechanism with the free silicon interstitials as described in previous section, suppressing the interactions between the backflow interstitials and activated B atoms [Mirabella et al., 2002].

For the F co-implant, as described early it is believed that the F_mV_n cluster formation and B-F pairing will take place during re-crystallization of the amorphous layer. The F_mV_n clusters are expected to be able to trap the released interstitials as the EOR defects evolve, while the B reacts with the F for B-F pairing at the high B concentration region [Diebel et al., 2003]. Referring to the R_s versus anneal temperature plot in figure 5.10(a) (solid diamond), dopant de-activation in Ge + F + B is noticeable and peaks at 750^{o}C. However, the magnitude of the de-activation peak is smaller and figure 5.10(b) indicates its maximum deactivation is reduced to approximately ~20% when comparing to the ~50% deactivation for Ge + B control sample. Despite B deactivation reduction is demonstrated by F co-implant, its reduction is indeed clearly less extensive than the C co-implant.

There are a few possible reasons: (1) higher retained dose for the C atoms than the F atoms upon annealing; (2) both F_mV_n cluster formation and B-F pairing are the indirect pathways in suppressing the B-I interactions. It would require, for instance, F to react with V point defects to form the F_mV_n clusters to trap the silicon interstitials emitted from EOR defects; while on the other hand the B-F pairing reduces the amount of initial active B available to be deactivated via BICs mechanism; (3) the

impact induced by extension of amorphization depth by the F co-implant on top of Ge-PAI. Nevertheless, it is worth to note that the free interstitial supersaturation from EOR defects to surface could be relatively lower with the deeper amorphization induced by the F co-implant, which generally results in smaller extent of dopant deactivation. This contradicts the observation of a worse deactivation suppression in comparison to C co-implant sample which has a shallower amorphization depth. Therefore, the prior two factors are more likely to responsible for the less effective deactivation inhibition of F co-implant.

In the Ge + BF_2 case, its curve (solid triangle) starts off with an R_s value which is generally above those of the Ge + B implant schemes (Ge + B, Ge + C + B and Ge + F + B) when annealed at 650^{o}C for 60s. This can be attributed to the large fraction of B atoms interacting with F atoms for B-F pairing during the SPER, thus resulting in lower initial dopant activation level comparing to the F-free B implanted samples [Colombeau et al., 2004a]. The existence of R_s peak at 750^{o}C in figure 5.10(a) indirectly reveals that the BF_2 with the Ge-PAI is still going through de-activation cycle. However, figure 5.10(b) shows that its ~30% deactivation is lower than the Ge + B. In addition, it is interesting to observe that the deactivation of Ge + BF_2 is about ~10% higher than the Ge + F + B, indicating the later is move effective in reducing the interactions of active B with the silicon interstitials during the dissolution of EOR defects possibly via the F_mV_n cluster-interstitial trapping mechanism. Since the F is implanted with the same energy and together with the B in the state of BF_2, the F atoms are basically overlapping completely with the B distributions. Therefore, the B-F pairing is expected to dominant over the F_mV_n

cluster formation in the BF_2 case, and this explain why the deactivation suppression of F in Ge + BF_2 is worse than the case where F atoms are co-implanted separately into the Ge + B sample.

The co-implantation of C into the BF_2 causes an undesired increase in R_s at the low annealing temperature starting at 650^{o}C (open circle) in figure 5.10(a). This is possibly due to the fact that only a smaller fraction of B is being electrically activated during the SPER process with the presence of C and F atoms at the same time. Although the detailed mechanism is not known, one postulation is that the B-F pairing could be enhanced with the presence of C doping and hence more electrically inactive B-F complexes exist in the early stages of the thermal cycle. Besides, it is also suspected that the activation of B could also be limited by the available lattice sides when C atoms are also competing for the active side during the SPER. Nevertheless, the R_s curve shows a similar monotonic reduction as the isochronal anneal temperature increases in figure 5.10(a). Furthermore when comparing the maximum deactivation at 750^{o}C with the Ge + BF_2 or Ge + B as references, it is found that the Ge + C + BF_2 has a negative de-activation percentage value in figure 5.10(b). This suggests that a further lowering of R_s value is achieved and confirming that the B de-activation process is totally being suppressed.

5.5.1(b) Active Carrier Concentration

Figure 5.11 is a graph showing the electrically active carrier concentration "N_s", also referred as activated B dose here, versus the annealing temperature for the various co-implanted B/ BF_2 splits.

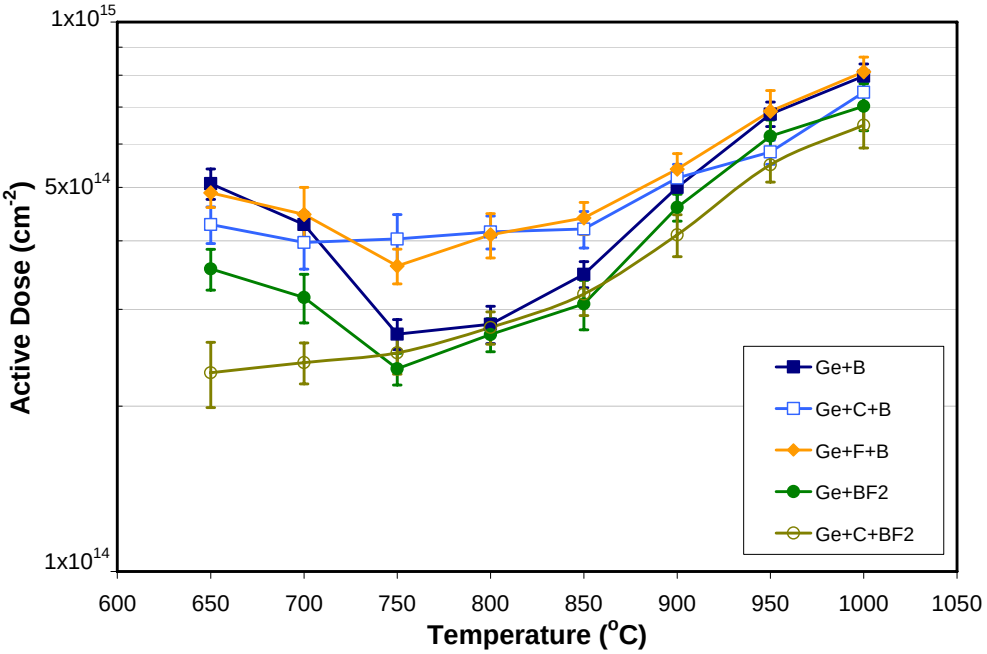


Figure 5.11: Active carrier concentration (N_s) as a function of isochronal annealing temperature for 60s to reveal the de/re-activation behavior of pre-amorphized B/ BF_2 junctions coupled with the C/F co-implant.

The Hall measurement results mirror and correlate the R_s measurements shown in figure 5.10(a) as expected. Although many similar features exhibit in these curves, a few points worth to be emphasized:

(1) It is clear from these data points that "reverse annealing" effect is taking place for the typical Ge + B junction with a trough at 750°C, which is the same temperature as the maximum R_s appears previously. This trend of N_s for Ge + B verifies the change of the R_s is not only due to variation in junction depth, however, is truly a de-activation (reduce in N_s) / re-activation (increase in N_s) process that due to the dopant-defect (interstitials) interactions during the evolution and dissolution of EOR defects as discussed earlier.

(2) Similar B de/re-activation cycle exhibits on the Ge + BF_2, but associated a smaller deactivation magnitude, due to the initial lower dopant activation as a result of B-F pairing explained above. In addition, the lower dopant activation also appears at 1000^{o}C, the BF_2 achieves ~47% activation comparing to ~53% eventual dopant activation for B case (B activation percentage is calculated based on the total implanted B dose).

(3) With C co-implant, B deactivation is clearly and effectively suppressed for the Ge-PAI B/BF_2 doped samples. It is also interesting to note that the initial B activation level at 650^{o}C is degraded by a factor of ~0.84 for Ge + C + B with respect to Ge + B, and further bigger degradation to ~0.65 for Ge + C + BF_2 with respect to Ge + BF_2. The results suggest that co-existence of C and F atoms in the junction could seriously restrict the activation of B during the SPER process. Besides, the degradation of total B activation in the presence of C persists up to 1000^{o}C.

(4) A smaller difference in the initial B activation level (at 650^{o}C) is observed between the Ge + B and Ge + F + B, indicating that F co-implant has less impact on the dopant activation during the SPER compared to the F co-doping in BF_2. Unlike the C co-implant, the B deactivation cannot be totally suppressed by the co-implanted F atoms, but it is clearly improved compared to the reference Ge + B case. In addition, the B activation level at 1000^{o}C is similar to the Ge + B reference, indicating the negligible effect of F co-implanted atoms.

5.5.1(c) Mobility

Although both of the R_s and N_s are presented above, it is important to have some insights on the variation of mobility during the annealing when co-implant is performed.

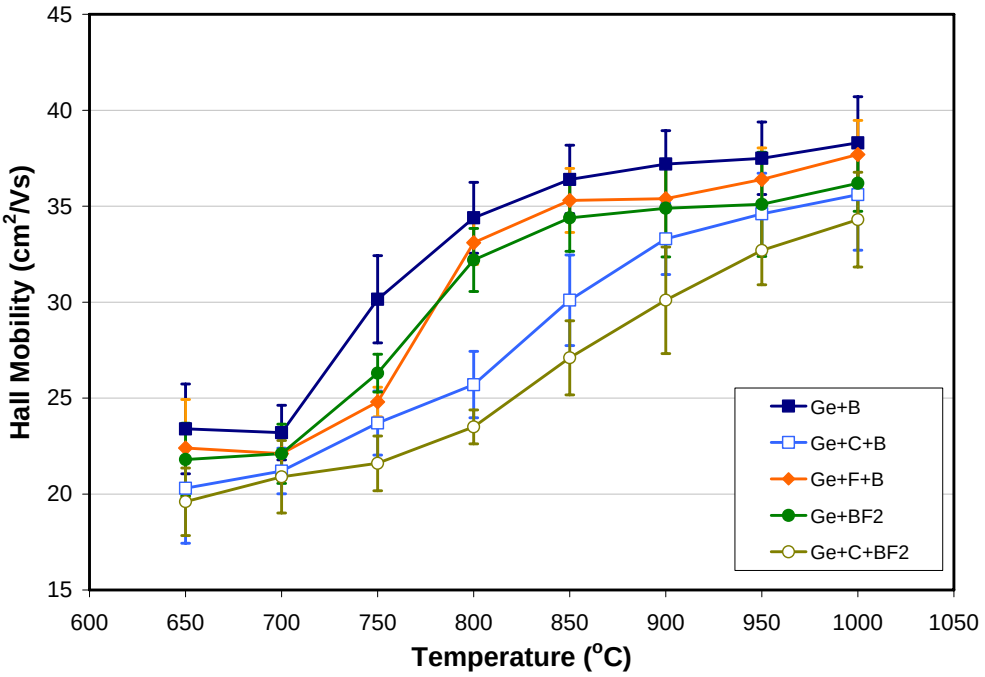


Figure 5.12: Mobility as a function of isochronal annealing temperature for 60s to reveal the de/re-activation behavior of pre-amorphized B/BF_2 junctions coupled with the C/F co-implant

The very first feature observed from figure 5.12 is that the reference Ge + B sample reveals relatively higher mobility values than the rest across the series of isochronal anneal temperatures. This can be thought as the result of co-doping in the B activated junction, increasing the ionized impurity scattering and thus causing the mobility to degrade. This is especially apparent to the Ge + C + BF_2 split, at which co-doping of C/F atoms at the same time leads to the lowest mobility values across

the anneal temperatures. On the other note, it is also observed that the mobility degradation is less extensive with the F co-implant comparing to the C co-implant, possibly due to the relatively smaller retention dose of F atoms after annealing which contributing less scattering sites.

The magnitude of the mobility is inversely proportional to active carrier density and also relates to the quality of the substrate. For the reference Ge + B sample, its mobility value at figure 5.12 shows initially low mobility values at 650^{o}C and 700^{o}C due to the existence of high level ionized impurity center, reflecting that high B activation has been achieved during the SPER process. Between 750^{o}C and 800^{o}C, the mobility is increasing rapidly and this correlates to a decrease in carrier density (less scattering centers) during the B deactivation cycle as shown in figure 5.9. A further annealing above 800^{o}C, B reactivation is initiated and induces more ionized impurity. However, removal of defects at higher temperature reduces the pathways for other scattering mechanisms. Therefore, this has resulted the mobility continues to rise but at a slower rate and eventually appears to saturate at higher temperatures.

Similar trend of mobility variation as a function anneal temperature is observed for the Ge + BF_2 and Ge + F + B, indicating that the "reverse annealing" effect is not able to be inhibited completely by the F co-doping. For the C co-implanted samples (Ge + C + B) on the other hand, the mobility shows more steady increment from 650^{o}C up to 800^{o}C opposes the typical rapid mobility increment in Ge + B reference, suggesting that the absence of B deactivation behavior. Correlate its mobility to the N_s plot, the gradual improvement of mobility values is also associated with the increment of B activation across the anneal temperatures. The

reduction of scattering effects from C atoms has largely contributed to the improvement in its mobility when C reacts with more interstitials to inhibit the dopant deactivation and TED. In combination with the better implant damage removal at higher temperature, it is therefore the mobility of C co-implanted samples is gradually improved. This mobility trend is not only applied to the C co-implant in Ge + B, but it also exhibits in the Ge + C + BF_2 case even though it has lower mobility values due to the F co-doping from BF_2.

5.5.2 The Effect of Carbon/Fluorine Co-implant on Junction Activation upon Spike Annealing

Figure 5.13 shows the R_s of the various B/BF_2 splits when subjected to spike annealing at 1080^{o}C.

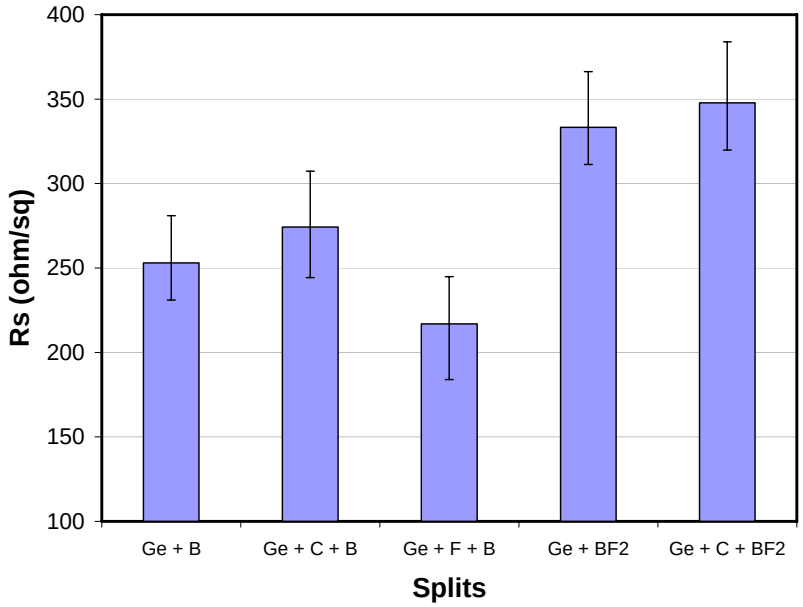


Figure 5.13: The sheet resistance (R_s) values of the Ge-PAI B/ BF_2 junctions with and without C/F co-implant when subjected to spike annealing at 1080^{o}C.

As opposed to the early illustration on the TED reduction by C/F co-implant, only F co-implant split exhibits the lower R_s value with respect to the Ge + B reference counterpart. Conversely, the co-doped F atoms in BF_2 are detrimental to the activation of junction due to the B-F pairing effect as described above, leading to increase R_s by 80 ohm/sq with respect to the F-free B only implanted sample. In addition, the R_s values of both Ge + B and Ge + BF_2 junctions are also degraded in the presence of C co-implant.

Nevertheless, the R_s results presented in above figure may not be a great representation for the effect of co-implant on the USJ characteristic because the R_s value is correlated not only on the dopant activation level, but is also inversely proportional to junction depth. Therefore, a graph showing R_s versus junction depth (X_j) (at 5×10^{18}, defined for 65nm technology and below) is plotted in figure 5.14. To quantify and compare the quality of the fabricated junctions, the universal R_s/X_j curve for the typical spike annealed B/BF_2 junctions is drawn in the same plot.

As seen from the figure, it is no surprise to see that the reference Ge + B and Ge + BF_2 samples show no distinguishable deviation of their points from the universal R_s/X_j curve. It is clearly demonstrated that F in BF_2 could help in retarding the B diffusion in the Ge + BF_2, however, the compensation of a higher R_s for the resulting junction constraint the junction to out-perform the universal junction characteristic.

The F co-implant into Ge + B has early been demonstrated to exhibit lower R_s (figure 5.14) with a slightly shallower junction depth upon spike annealing, it is thus ascertaining its favorite left shift in figure 5.12. This observation indicates that the

properties of the junction can be engineered very differently with F co-doping, for instance, the doping of F atoms into junction is more superior with an optimized F co-implant rather than indirect F co-doping via BF_2 state.

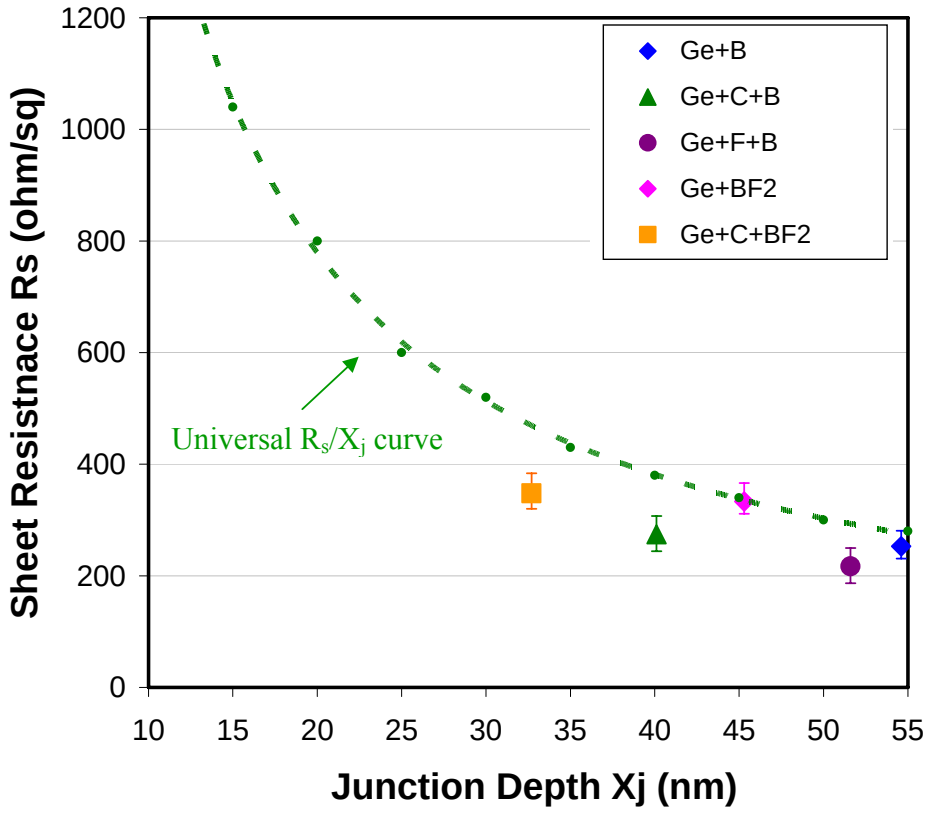


Figure 5.14: The sheet resistance (R_s) as a function junction depth X_j with data points extracted from the SIMS profiles and R_s data of the Ge + B samples associated with C/F/N co-implant subjected to spike annealing at 1080°C.

Although C co-implant has caused R_s degradation for the Ge + B/BF_2 in figure 5.11, it is interesting to observe that the corresponding junctions show favorable shift to the left of universal curve in figure 5.14. The Ge + C + B is demonstrated to provide a competitive junction which can rival with the Ge + BF_2 with smaller junction depth and R_s. On the other hand, C co-implanted Ge + BF_2 exhibits a further

shallower junction with appreciable increment in R_s that is well below the level defined by the R_s/X_j curve. The improvement of R_s/X_j behavior can be attributed to the extensive gain in the B TED suppression over the small degradation of dopant activation in the C co-implanted junction. In addition, by extending data points of the co-implanted samples vertically towards the R_s/X_j universal curve, one can possibly deduce that the C co-implant is benefiting the junction R_s reduction if the B/BF_2 junctions are fabricated at same junction depth.

5.6 Physical Interpretations of the Effect of Carbon/Fluorine on B/ BF_2 Junctions

The results above have demonstrated that C/F co-implant can significantly affect the dopant activation and diffusion of B/ BF_2 doped preamozphized junction. The theories and explanations behind the effects of co-implant were elaborated in terms of the anomalous diffusion and activation separately. The following discussion will interpret the observed results by correlating them together to give a better overall insight on how the junction characteristics would have changed in the presence of C/F co-implants.

During the SPER of the pre-amorphized layer, B-rich clusters form in the region of high B concentration, and the excess interstitials agglomerate into I-clusters beyond the initial a/c interface which leads to the formation of EOR defects [Colombeau et al., 2004b]. The driving force for B TED and de-activation is the interstitial supersaturation through the emission of interstitials towards the surface during the ripening and dissolution of EOR defects. In the typical USJ formed by pre-amorphization technique, the EOR defect band is located some distance beyond the

high-concentration B region, therefore the deactivation process requires transport of interstitials from the EOR band towards the surface, forming inactive BICs. Both the TED and dopant deactivation characteristics, induced by the dopant-defect interactions, are clearly demonstrated in the physical SIMS profiles and electrical measurements of the Ge + B reference in this work.

Among the different co-implant schemes, C co-implant indeed is shown to be more superior compared to F co-implant in terms of TED reduction and dopant clustering suppression, when the co-implanted atoms are located in the middle range of the peak B profile and the EOR region. One of the direct evidences is from their spike annealed C/F SIMS profiles, which is demonstrated that implanted C atoms are relatively stable as compared to the F atoms upon annealing, since a large fraction of the latter F atoms are out-diffused during the thermal annealing.

The C co-doping relies on the carbon-interstitial clustering, C_mI_n. Since, m is preferentially larger than n, and particularly C_2I is more favored, high C concentration is required to react with excess interstitials (at least two-folds) [Mirabella et al., 2002]. It is also generally thought that C must be placed into substitutional sites during the SPER to react with the emitted interstitials during the dissolution of EOR defects [Zechner et al., 2007]. A PAI associated C co-implant is therefore expected to be highly effective since it involves re-crystallization of shallow amorphous layer during the early stage of activation annealing. As shown in the B dopant profiles with C co-implant, B TED is greatly suppressed due to the interstitial trapping effect provided by the C atoms. Through the formation of C_mI_n clusters, the interactions between the B and silicon interstitials released from the EOR is greatly reduced with the clear

evidence from much shallower B profiles annealed either with soak or spike annealing. Likewise, negligible dopant deactivation is also seen from R_s versus isochronal anneal temperature plot, as a result of the suppression of B-interstitial clustering in the high B concentration region.

Another prevalent feature of C co-implant is its impact on the evolution of EOR defects. Based on the TEM micrograph and the observed dopant trapping at EOR region, it can be inferred that C would have helped in reducing the amount of EOR defects under the same anneal temperature with respect to the Ge + B reference case. One possible explanation is that the defect nucleation process has been disturbed by the presence of C atoms, leading to changes in the evolution of interstitial point defects at the EOR region or possibly faster dissolution of defects upon annealing. However, this would require further verification. The evidence of C atom interactions with interstitials in the EOR region is observed, at which a trapping peak is detected in the C profiles around the EOR region and is thought to be the stable C_mI_n clusters remain after spike annealing.

When F co-implant was performed prior to the B implant, the spike annealed profile of B atoms shows retardation in TED and is in agreement with the result shown previously by Graoui et al., in which the F atoms were positioned in between B profile and the a/c interface [Graoui et al., 2005]. It is thought that F_mV_n clusters are formed during SPER, which then can trap some of free interstitials flow towards surface during the dissolution of EOR defects, resulting in reduction in TED [Stolk et al., 1997]. But the possibly due to interactions of B and F atoms in their overlapped as-implanted distributions for B-F pairing should not be ruled out. Similarly to the

dopant deactivation inhibition observed in the isochronal annealing, in which the peak deactivation is still showing up at temperature around 750^{o}C for the sample with F co-implant. However, reduction of deactivation percentage by around 30% is observable. Recently, Cowern et al. reported a comprehensive study on the relevance of F location in relation to the B profile and the EOR defect bands, and proposed that dopant deactivation can be effectively inhibited if the range of F is optimized [Cowern et al., 2005a]. Nevertheless, it has been revealed in this study that the effectiveness of F co-implant is still lower than C co-implant when they were inserted in a similar relative location into the Ge + B junction.

With respect to the case which F atoms are co-doped together with B in the form of BF_2, the de/re-activation curve of the Ge + BF_2 shows a similar trend to the F+B case. However, the R_s values of Ge + BF_2 are significantly higher than both Ge + B and Ge + F + B cases, suggesting that F react with B easily to form B-F pairs due to its larger overlap between the B and F as-implanted distributions. The high R_s value is a result of dopant activation level lowering, which is also reflected in their SIMS profiles in their activation "kink" level shown upon low temperature annealing.

By using a similar C mechanism described for the Ge + C + B, advantages such as reduction of B TED, suppression of B deactivation/clustering as well as the EOR defects removal are also shown when C is co-implanted with BF_2. In particular, the shallowest dopant profile is obtained from the Ge + C + BF_2 case, suggesting that the gains are not only from C atoms alone, but through the combination with F atoms. However, deleterious impact on R_s due to the degradation of electrical activation is further magnified with the presence of C and F at the same time, resulting in a higher

series of R_s values at various annealed temperatures. The parallel interactions of C and F atoms with point defects involve complex mechanisms and the details are subjected to further investigation.

5.7 Comparison of Carbon/Fluorine/Nitrogen Co-implant on Boron Preamorphized Junctions

So far, the results presented are based on the C/F co-implant with their atoms located in between the peak of B profiles and the EOR defects. In previous chapter, N co-implant has also been demonstrated to offer optimum benefits with the similar relative location among the B, N, EOR defect distributions. Therefore, a quick comparison of the C/F/N co-implant in Ge + B would be necessary and critical to provide some insights of their effect on USJ formation, depicted in figure 5.15.

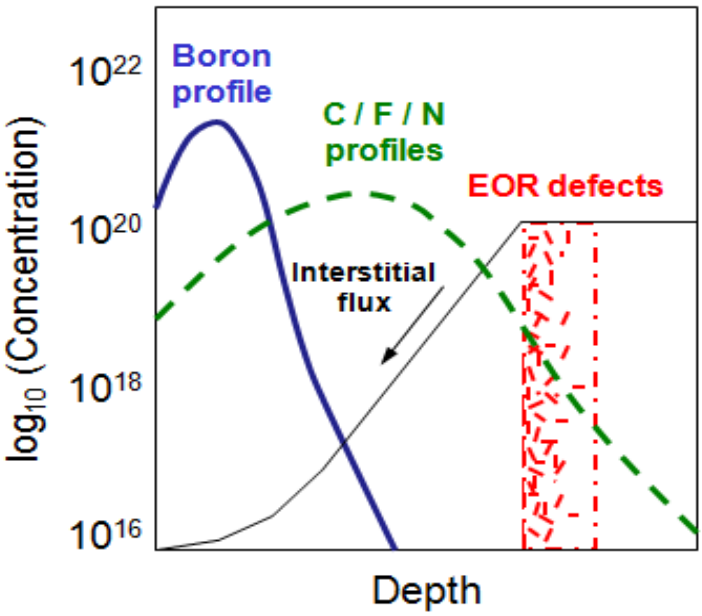


Figure 5.15: Schematic diagram showing the relative location among the boron profile, impurity distribution (C/F/N) and EOR defect range.

Figures 5.16 shows the various splits of B SIMS profiles subjected to spike annealing at 1080°C.

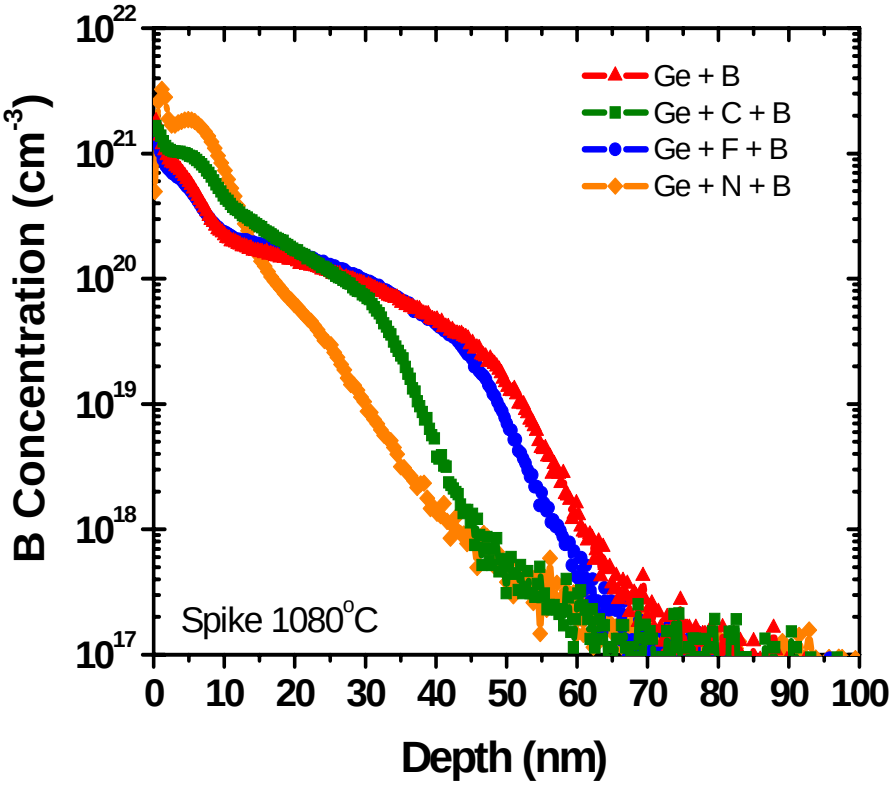


Figure 5.16: SIMS profiles of 1 keV B implant with and without C/F/N co-implant subjected to spike annealing at 1080°C.

The results clearly demonstrate that shallower B junctions are achievable with the C/F/N co-implant approach when compared to the typical Ge + B junction, attributing to the B TED suppression. As described in the various sections previously, the different co-implanted atoms have their individual mechanism inhibiting the interactions of B with interstitials. For instances, the C atoms interact with free interstitials through C_mI_n complex formation, while the F and N atoms would require to react with vacancy point defects to form the impurity-vacancy clusters (F_mV_n or N_nV_m) before it can annihilate the free interstitials. Therefore, the resulting B junction

depth can vary significantly as illustrated in figure 5.16. With reference to the concentration of 5×10^{18} cm^{-3} (the junction depth defined for 65nm technology and below), the sequence of the junction from deepest to shallowest is Ge + B, Ge + F + B, Ge + C + B and lastly the Ge + N + B (based on the optimum 6keV N co-implant). Nevertheless, the junction depth reduction shown here is not necessarily to serve as a benchmark of enhancement that is associated with co-implant towards the USJ junction properties. However, it would also require the evaluation of the dopant activation level in the particular junction if it is able to go beyond the electrical solubility limit set by B/BF_2 under spike annealing. Otherwise, one could achieve a similar shallow junction fabricated by co-implant by merely scaling down the implant energy or the spike anneal temperature.

Figure 5.17 presents state-of-the-art R_s/X_j plot for the samples co-implanted with C/F/N atoms in previous figures associated with their corresponding R_s values. Except the reference Ge + B, G + N + BF_2, all of the co-implant splits show improved R_s/X_j behavior by left shifting from the universal R_s/X_j curve. The results clearly illustrate that C/F/N co-implant would have helped in improving the junction R_s/X_j properties of the typical Ge + B represented by the universal curve.

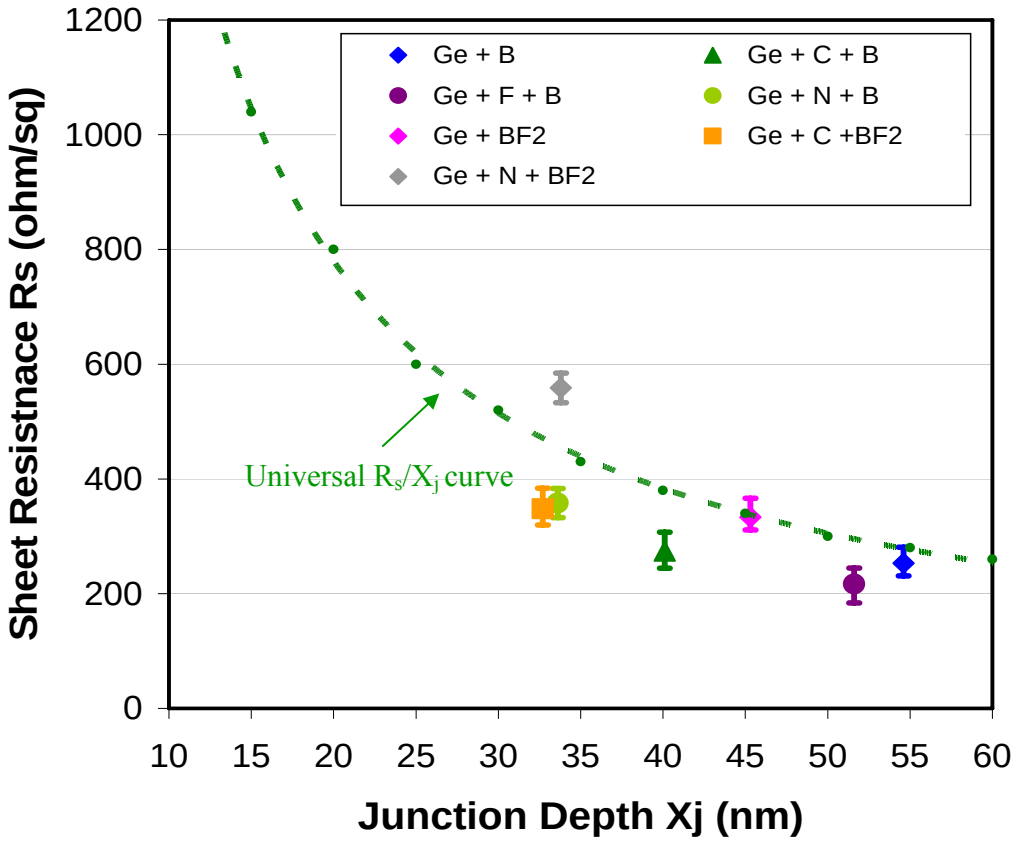


Figure 5.17: The sheet resistance (R_s) as a function of junction (X_j) with data points extracted from the SIMS profiles and R_s data of the B/BF_2 samples associated with C/F/N co-implant subjected to spike annealing at 1080°C.

To quantify the effectiveness of C/F/N for the Ge + B junction enhancement, the ratio between the R_s values of the actual C/F/N co-implanted junction and the R_s of same junction depth extracted from universal R_s/X_j is obtained and shown in table 5.1.

Comparing among the 3 different co-implants, the C co-implanted B shows the highest R_s gain by a factor of 1.39, suggesting that the R_s/X_j junction properties are improved the most with respect to C-free B/BF_2 cases. The effectiveness of enhancement is followed by the F co-implant with a factor of 1.35 and then the lowest

R_s improvement in N co-implant splits with a value of 1.27. This observation is contradicting to the largest gain in the TED suppression and its shallowest junction depth with N co-implant, depicting that the junction properties fabricated with co-implant should not be evaluated based on a single X_j parameter only.

	R_s measured from the co-implanted junction	**R_s extracted from universal R_s/X_j curve with same junction depth**	**R_s_extracted / R_s_measured**
Ge + C + B	274.3	380.5	***1.39***
Ge + F + B	216.9	293.4	***1.35***
Ge + N + B	358.2	456.5	***1.27***

Table 5.1: The sheet resistance (R_s) values of C/F/N co-implanted B preamorphization junctions and also the R_s extracted from R_s /X_j universal curve of B/BF_2 with the same junction depth.

On top of the R_s/X_j characteristic, it is also important to understand the stability of the junctions when the different types of atoms are co-implanted. Figure 5.18 is the de/re-activation study of different junction splits performed by isochronal annealing in the temperature range of 650^{o}C to 1000^{o}C for 60s.

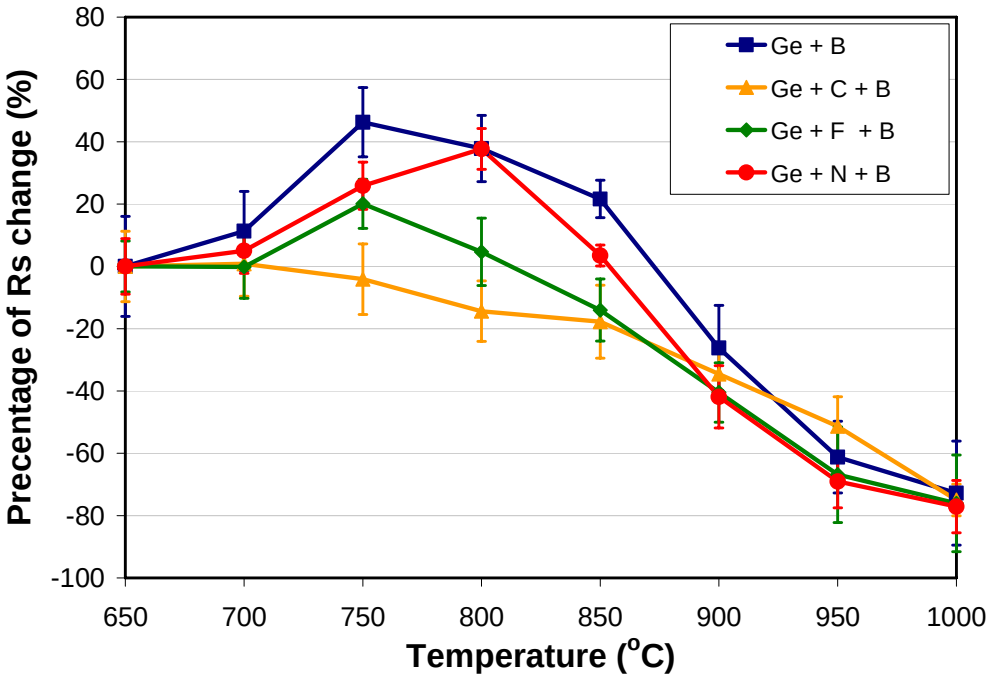


Figure 5.18: Percentage change of R_s (normalized to the 650°C) as a function of isochronal annealing temperature for 60s to reveal the de/re-activation behavior of preamorphized B junctions associated with the C/F/N co-implant.

As discussed earlier in section 5.5.1, C co-implant is shown to have a complete advantage over the F co-implant. One can clearly see that the typical B deactivation as a result of interstitial backflow from EOR region can be completely suppressed by C co-implant via the C_mI_n cluster formation upon annealing. Reduction in dopant deactivation on the other hand is seen for F co-implant, but the deactivation is still observable with a ~20% change of its R_s value, with respect to the ~50% deactivation in Ge + B junction. In the case of N co-implant, the B deactivation further increases to ~37%, proposing that the interstitial annihilation via the NV cluster is not as effective as the FV cluster exist in the F co-implant. The evidences and details of the various mechanisms have been discussed in the early section.

Another key parameter to study the electrical characteristic of USJ formation is the junction leakage. Figure 5.19 shows I-V behavior of the p+/n diodes fabricated using the C/F/N co-implanted Ge + B junctions shown in SIMS figure 5.16.

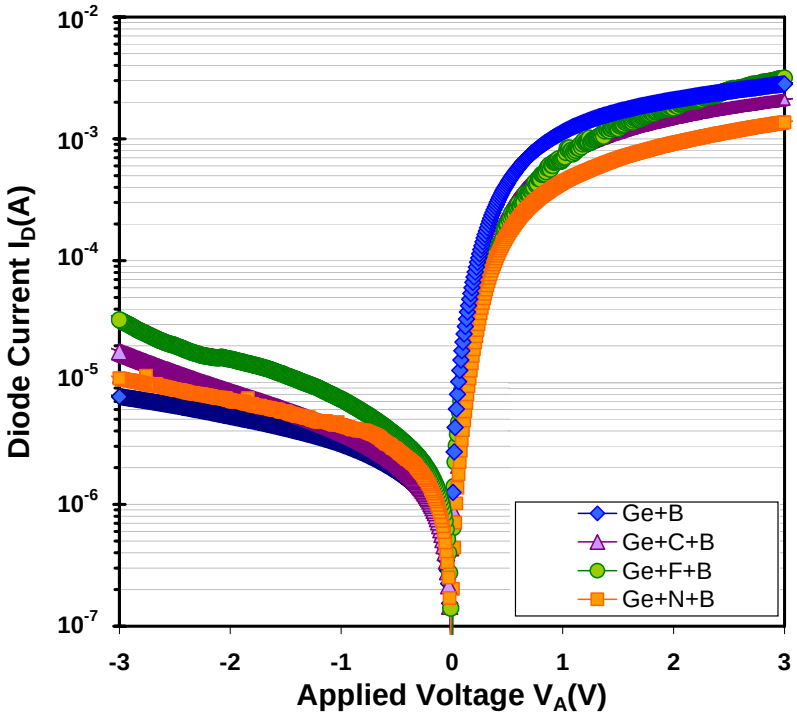


Figure 5.19: I-V characteristic of p+/n diodes fabricated with Ge + B junctions in n-type silicon and also associated with C/F/N co-implant subjected to spike annealing at 1080^{o}C.

Referring to the forward biased of the diodes, it is observed that the forward current varies with respect to the co-implants splits. At which the reference Ge + B shows the highest forward current, while the N co-implant B junction has the lowest on current when positively biased. With a more careful analysis, it is found that the forward current in the diodes can be correlated well to the R_s values of junctions

shown in figure 5.17 and hence attributed to the dopant activation effect on diode forward current.

Despite the variation in forward current, the diode leakage shows a very different pattern with respect to the co-implant species at the reversed biased regime. Although it is an unfavorable outcome, the results clearly indicate that all the co-implanted junctions reveal higher leakage level. For instance, the F co-implanted B junction shows up to around half an order higher in its current leakage as compared to the Ge + B reference. The leakage is demonstrated to be reduced with a C co-implant and further lowering on the current leakage is noticed when N co-implant is performed on the B junction. The different level of leakage in these diodes can be thought as an inherent doping effect of the various elemental atoms (C/F/N), or possibly, the impact of the different co-implant atoms towards the reparation of implant damages in junctions.

	Reference (Ge+B)	**C co-implant (Ge+C+B)**	**F co-implant (Ge+F+B)**	**N co-implant (Ge+N+B)**
R_s/ X_j Improvement	-	Most Improved	Improved	Least Improved
Junction stability	~ 50% Deactivation	Most Stable ~0% Deactivation	~20% Deactivation	~37% Deactivation
Junction leakage	-	Leaky, ~1.7x of reference	Most leaky, ~3x reference	Leaky, ~1.4x of reference

Table 5.2: A summary of the C/F/N co-implant effect on B USJ formation and its junction properties.

The overall effect of C/FN co-implant atoms on the B USJ formation and its junction properties is summarized in table 5.2 (previous page).

5.8 Summary

An extensive study on C/F co-implant in Ge-PAI B/BF_2 junction during soak annealing has been performed in comparison with the spike annealing. A physical description of dopant-defect interactions with the C/F co-implant scheme has been presented by correlating the B diffusion and activation behaviors.

The resulting junctions of the various co-implant schemes (C/F/N) associated with the similar relative distributions have been evaluated to provide a better insight on the effect of co-implant on the various junction characteristics towards the fabrication of USJ in the devices. The co-implanted C atoms interact with interstitials directly to form carbon-interstitial clusters (C_mI_n) and is the most effective co-implant species in improving the R_s/X_j junction behaviors as well as suppressing the B de-activation phenomenon in the Ge + B junctions. However, it increases the junction current leakage moderately. Both F/N co-implants, which employing the vacancy clusters (FV/NV) interstitial trapping mechanism, reveal a smaller but appreciable improvement in their R_s/X_j characteristics. The N co-implant is less efficient in dopant de-activation suppression, but it offers the lowest junction leakage among the various co-implant splits. The F co-implant has resulted in the largest current leakage.

In summary, there is no absolute advantage from one co-implant species. The use of the any co-implant approach for USJ formation in transistors requires the considerations on the needs of the devices (e.g low leakage, better SCE control).

Nevertheless, the observations and results obtained in this work can be served as an important reference.

Chapter 6

Understanding of Boron Junction in Preamorphized Silicon upon Optimized Flash Lamp Annealing

6.1 Introduction

Trade-off between the dopant diffusion and dopant activation limits the process window of the annealing thermal budget. Because of these constraints, conventional ion implantation coupled with spike RTA is no longer a feasible implementation in the sub-45nm devices [Feudel et al., 2006].

Formation of ultra-shallow and highly activated junction is ever desired and required for the future generation of CMOS. This can be achieved by maximizing the anneal temperature while reducing the anneal time. This explains the prevalent use of the spike RTA process with higher ramp-up rates of several hundred degrees per second in recent years, to reduce the overall thermal budget in the anneal cycle. However, it has been reported that when the ramp-up rate is too high, it will result in low uniformity and also possibly induce wafer deformity. This has attracted a lot of interests in the search for alternative thermal anneal techniques in recent years [Hill, 1983., Fiory et al., 1999, Mokhberi et al., 2002b].

Flash lamp annealing (FLA) has been proven to be a potential candidate as it offers the possibility of performing annealing in the millisecond range with high

temperature at lower thermal budget as compared to the conventional spike RTA process [Yoo et al., 2005, Lerch et al., 2005]. This technique uses an array of flash lamps which are energized to produce a pulse of intense light over short anneal times on the order of milliseconds. The very short pulse duration only heats up the near surface region of the silicon wafer, providing high meta-stable dopant activation, while the bulk of the substrate acts as a heat sink allowing for rapid conductive cooling, so that the near surface region quickly drops in temperature, preventing further dopant diffusion and possibility to result in diffusionless profile [Timans et al, 2006].

However, extensive silicon defects remain after FLA, leading to high current leakage at device level [Jones et al., 2003, Jain et al., 2005, Bayha et al., 2003]. Another concern of the residual silicon EOR defects is its impact on the junction stability, which is closely related to the dopant de-activation when the activated junction is subjected to post-thermal treatment, such as spacer formation and silicidation, in the typical MOS device process flow [Bayha et al., 2003, Sharp et al., 2006].

In this chapter, we investigate the characteristics of FLA on the USJ formed by Ge-PAI followed by low energy B ion implantation. Extensive study is performed on how to use the multiple-pulse FLA to optimize and improve the junction properties. Evaluation on junction stability and junction leakage when subjected to various flash anneal schemes is performed as well. Simulation study is also used to supplement the experimental results for the explanation of the operating physical mechanisms during the FLA process.

6.2 Experimental Details

Czochralski grown 12-inch (100) n-type silicon wafers were subjected to preamorphization by performing Ge ion implantation at 15 keV with a dose of 5×10^{14} cm^{-2} prior to the B implantation at 1 keV with a dose of 2×10^{15} cm^{-2}. Some of the wafers were processed with B implantation only. The front wafer surface was mounted facing the Xenon flash lamps with the backside exposed to the hot plate. The temperature of the wafer was raised using the hot plate to an intermediate temperature of 500°C before the flash lamps were triggered for irradiation. FLA was performed in N_2 ambient for 1, 3, and 6 pulses with the intensity of 26 J/cm^2 and pulse duration of 0.8 ms, respectively. At this FLA condition, the peak wafer temperature was estimated to be around 1150^{o}C ~ 1200^{o}C. One of the wafers was subjected to a 950^{o}C spike RTA to anneal out the EOR defects prior to FLA, and designated as pre-spike RTA flash annealing (or pre-spike RTA + FLA) in the subsequent sections. RTA isochronal annealing cycle was also applied on those Ge-PAI B junctions processed with different FLA schemes for the junction stability study. The isochronal annealing was performed with the temperature ranges from 600^{o}C to 1050^{o}C for 60s,

The dopant chemical profiles were analyzed ex-situ by secondary ion mass spectrometry (SIMS) using a Cameca IMS 6f instrument. A primary beam of O2+ ions with a net energy of 1 keV at 56° incidence was scanned over an area of 250μm × 250μm to characterize the B profiles. Crater depth was obtained by using Tencor Alpha-Step 500 profilometer. Sheet resistance (R_s) was measured by standard four point probe, whilst the active carrier concentration (N_s) and mobility were

characterized by Hall effect measurement assuming a unity Hall scattering factor. Cross-sectional TEM (XTEM) was performed to analyze the extent of amorphization and end-of-range (EOR) defect formation.

6.3 FLA on Crystalline (non-PAI) and Ge-PAI B Junctions

B junction formation was carried out in this section with the implementation of FLA on the non-PAI crystalline and Ge-PAI B doped silicon substrates. Figure 6.1 shows that the Ge-PAI has resulted in a continuous amorphous layer of approximately ~ 26 - 27 nm.

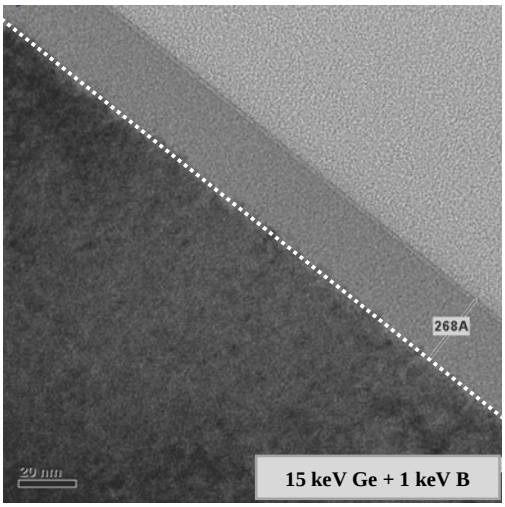


Figure 6.1: XTEM micrographs for the sample as-implanted with 15 keV, 5×10^{14} cm^{-2} Ge followed by 1 keV, 2×10^{15} cm^{-2} B.

Comparison of the R_s values for the various samples underwent 1, 3 and 6 pulses of FLA is illustrated in figure 6.2. It is observed that the non-PAI junctions (solid diamond) appear to have higher R_s than the samples with Ge-PAI (solid circle and open triangle). This is attributed to the solid phase epitaxial re-growth (SPER) of the amorphous layer in the Ge-PAI junctions, resulting in better B electrical

activation compared to the non-PAI counterparts regardless of the number of flash pulses.

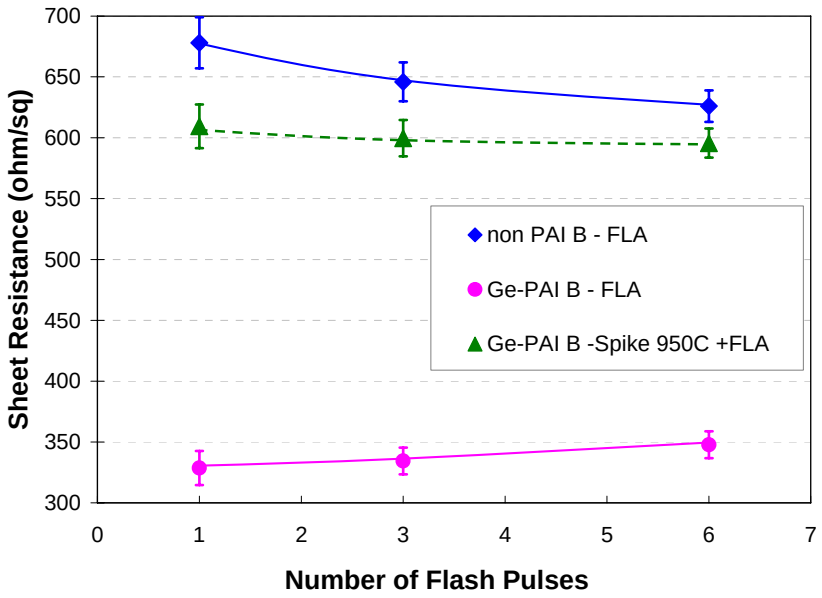


Figure 6.2: Sheet resistance as a function of the number of flash pulses for (a) non-Ge-PAI and Ge-PAI boron-doped samples, which annealed with (b) FLA and (c) pre-spike RTA 950^{o}C followed by FLA.

When multiple-pulse FLA is directly performed on the non-PAI and Ge-PAI samples (solid diamond versus solid circle), the measured R_s values exhibits the opposite trend. In the case of non-PAI, a continuous R_s reduction with the increase of flash pulses has been observed due to the enhanced thermal budget effect. However, it is interesting to see that the R_s characteristic of Ge-PAI junctions indeed increases with the number of FLA pulses being applied. It is well known that Ge-PAI introduces EOR defects around the a/c interface upon thermal annealing. The upward R_s trend in the latter case (Ge-PAI B) indirectly implies that the additional flash pulses may affect evolution of EOR defects and their interactions with dopants, subsequently change the junction activation property.

In addition of the direct FLA, the R_s of Ge-PAI samples subjected to a 950^{o}C pre-spike RTA prior to FLA is also included in figure 6.2 (open triangle). The pre-spike RTA step is inserted purposely aiming to dissolve or reduce the EOR defects. With further consideration, the Ge-PAI junction in this anneal sequence resembles to that of the non-PAI case with direct FLA (solid diamond) since the amorphous layer induced by Ge-PAI in the junction has been re-crystallized during the pre-spike RTA step, and thus the subsequent FLA is processed in a crystalline form. It is therefore to be expected that, Ge-PAI samples with pre-spike RTA flash scheme follow the trend of early non-PAI B junctions, where the R_s decreases with the number of flash pulses.

Interestingly, it is also noticed that the overall R_s level of the Ge-PAI B junctions subjected to pre-spike RTA followed by FLA is higher than those receiving the direct FLA Ge-PAI case (solid circle). The reason is due to the fact that the amorphous layer induced by the Ge implant was re-crystallized during a much slower ramping pace of the pre-spike RTA as compared the millisecond FLA. Therefore, it is thought that the ramping rate has profoundly affected the activation level of dopant during the SPER process. The observation is in agreement with the published findings, claiming that reduced boron-interstitial clustering and better dopant activation are achieved with the faster SPER when higher rate of ramping-up is applied in the thermal cycle [Sharp et al., 2006, Poon et al., 2008].

A brief summary up to this point is that the effect of FLA on the activation of Ge-PAI B doped samples, either by direct single/multiple-pulse FLA or pre-spike RTA + FLA, is not simply dependent on the magnitude of thermal budget. Rather, it involves the complex dopant-defect interaction mechanisms during the overall

thermal cycle. Therefore, it is essential to further understand and investigate the underlying involved physical mechanisms on the Ge-PAI samples.

Figure 6.3 (a) shows a clear defect band remains around the original a/c interface of the Ge-PAI samples when subjected to a single pulse of FLA. These defects are generally small and highly dense, possibly consisting of clusters and {113} defects.

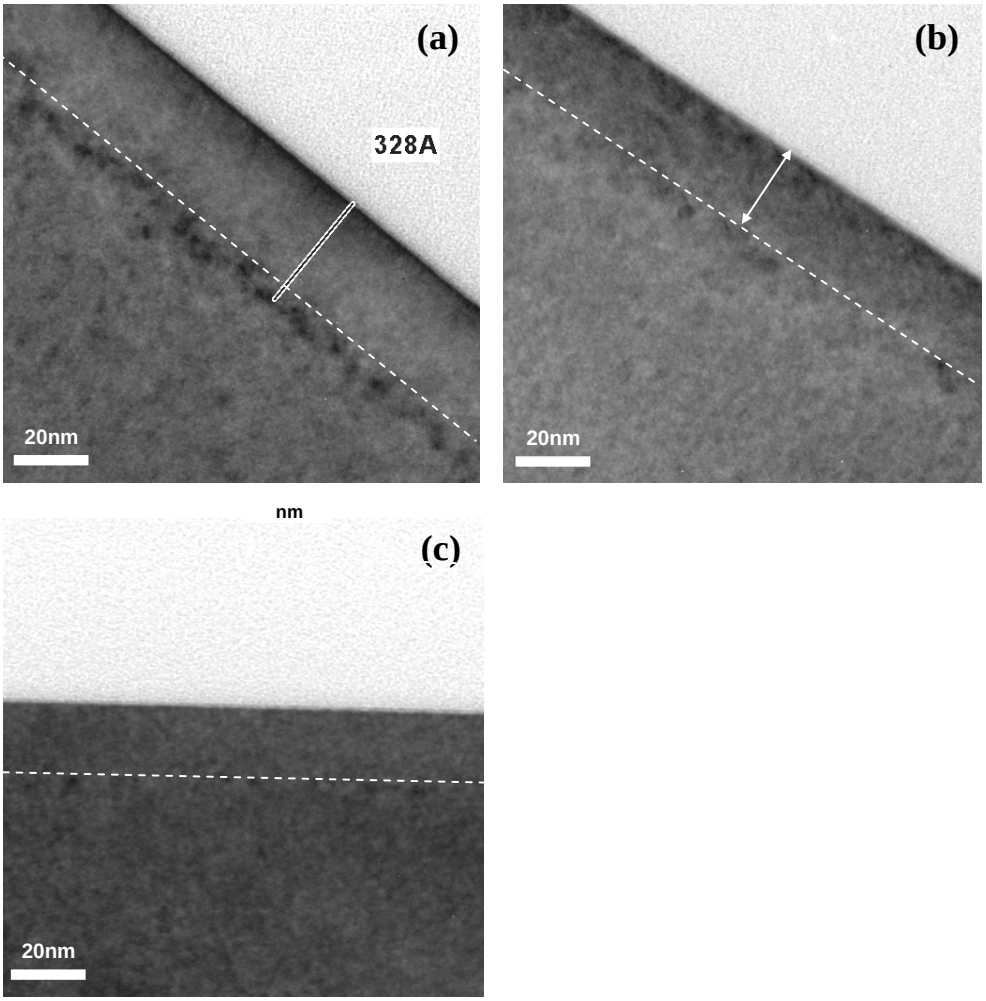
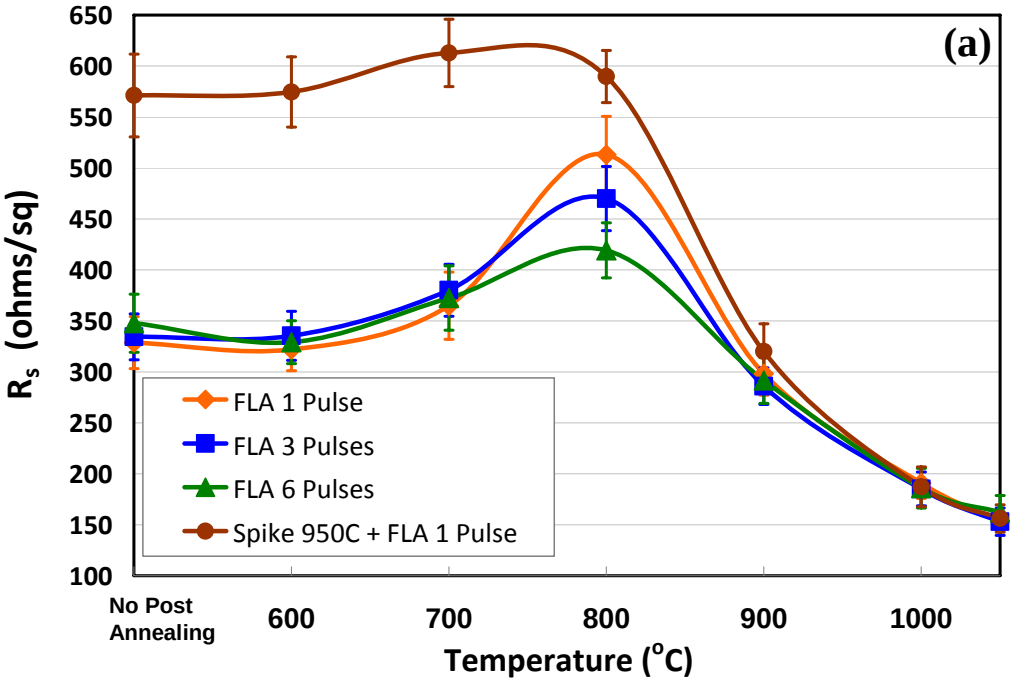


Figure 6.3: XTEM micrographs for the samples processed with FLA (a) 1 pulse, (b) 6 pulses and (c) 950^{o}C spike RTA + FLA. Dotted lines are drawn to show the a/c interfaces.

As the number of FLA is increased to 6 pulses, figure 6.3 (b) reveals that the defect density is greatly reduced. When pre-spike RTA at 950°C was applied followed by FLA, figure 6.3(c) clearly shows that great amount of the EOR defects has also been effectively reduced. However, non-significant traces of extended defects remain to be observable in the XTEM micrograph.

6.4 Junction Stability of Ge-PAI B Junctions with Various FLA Schemes

To evaluate the junction electrical stability, samples treated with 1, 3 and 6 pulses of FLA and those preceded with pre-spike RTA were subsequently annealed isochronally. Figure 6.4(a) shows the R_s values of the different samples after receiving a series of 60s isochronal post-annealing, ranging from 600°C to 1050°C.



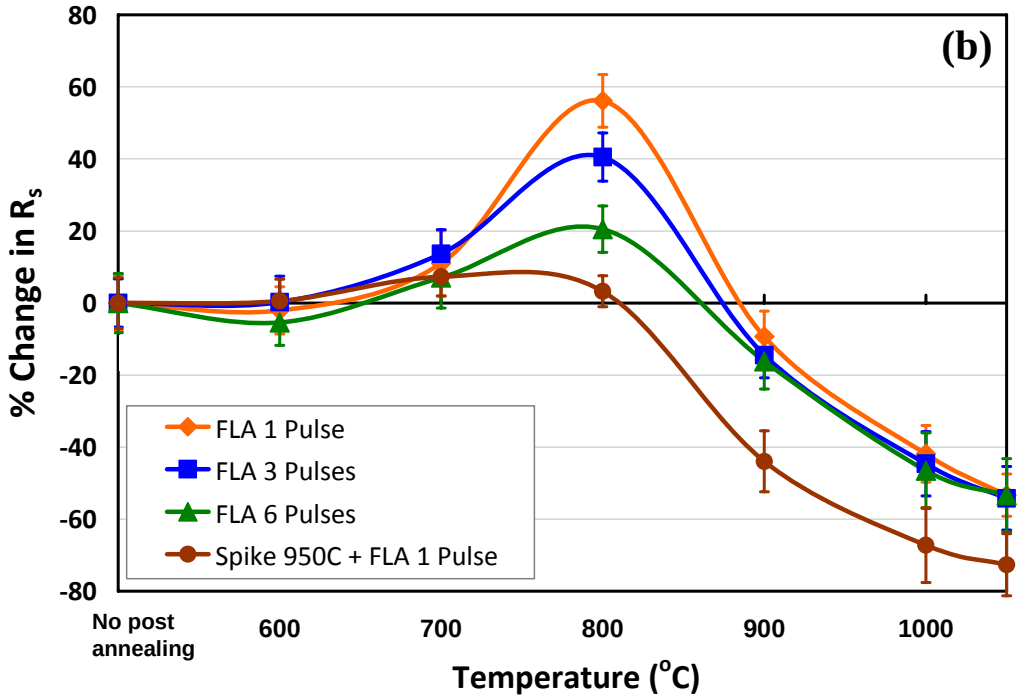


Figure 6.4: (a) Sheet resistance value (R_s) as a function of 60s isochronal annealing temperature. (b) Change of R_s as a function of 60s isochronal annealing temperature. The change of R_s is normalized to the as-flashed samples.

For single pulse FLA, there is no significant variation in the R_s as compared to the multiple-pulse FLA at post-annealing temperature of 600°C. The value of R_s increases above this temperature, suggesting that the dopants start to de-activate. The R_s peaks at 800°C. The observed de-activation behavior is due to the formation of inactive BICs induced by the backflow of the free interstitials from EOR defect band towards the surface during the post-RTA. Subsequently, the recovery of dopant activation is observed and inferred from the trend of reduction in R_s beyond the peak de-activation temperature. In addition, thermal diffusion at the higher temperature range also partially contributes to the continuous drop of R_s.

As the FLA is increased to 3 and 6 pulses, similar R_s variation curves are observed, whereby the dopants de-activate the most when the post-thermal treatment is performed at 800^{o}C. However, it is clearly seen that a lower peak R_s is obtained by increasing the number of FLA pulses. To further quantify the extent of de-activation, R_s values are re-plotted in terms of the percentage change in R_s (normalized to the as-flashed sample) in figure 6.4(b). For single pulse FLA, there is a 56% increment in the R_s value, and it decreases to 40.5% with 3 pulses and even further to 20.5% with 6 pulses of flash.

The de-activation characteristic of the pre-spike RTA flash scheme is almost negligible where only around 3% change in R_s is being observed. This can be directly correlated to the effective removal of EOR defects by pre-spike RTA (shown in figure 6.3(c)). Therefore, the supersaturation of interstitials from EOR region towards the surface is greatly decreased during the isochronal post-thermal annealing, which results in reduced dopant de-activation caused by the dopant-interstitial clustering. This finding is in agreement with the observation that incorporation of spike RTA prior to the FLA could overcome the residual defects and junction current leakage issues [Lindsay et al., 2003a]. Nevertheless, pre-spike RTA + FLA processed samples possess higher R_s either before or after isochronal post-annealing (up to 900^{o}C). It has no absolute advantage over the direct FLA (1, 3 or 6 pulses) in terms of dopant activation although the incorporation of pre-spike RTA is beneficial for dissolving the residual silicon defects.

Nevertheless, one may argue that the pre-stabilization thermal step during the flash cycle (as described in the experimental details) may induce the re-crystallization

of Ge-PAI amorphous layer through the SPER. This would render no difference between the direct FLA approach and the pre-spike RTA + FLA scheme, since the SPER are taking place with the lower ramping rate thermal step. To verify this, an XTEM was performed and is shown in figure 6.5.

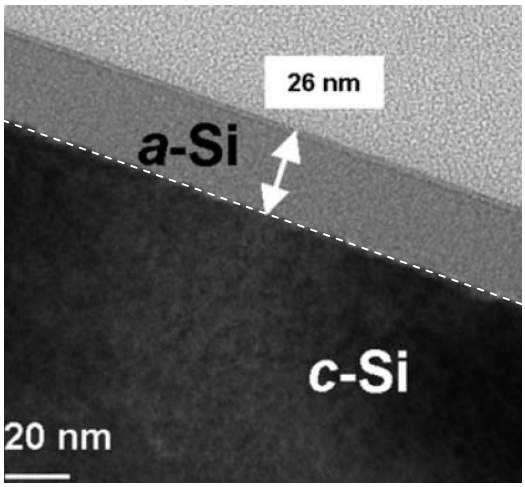


Figure 6.5: XTEM micrographs for the sample implanted with 15 keV, 5×10^{14} cm^{-2} Ge followed by 1 keV, 2×10^{15} cm^{-2} B and annealed at the intermediate temperature 600^{o}C without flash pulse.

It is found that the condition of 500^{o}C used for the intermediate pre-heating is not sufficient to cause the re-crystallization of the Ge implant induced surface amorphous layer. In this case, the SPER is taking place during the high temperature millisecond flash pulse, contributing to higher level of dopant solid solubility (lower R_s) in those samples undergoing the direct FLA scheme (1, 3 or 6 pulses). This is consistent with the published works, suggesting that short time, high temperature treatment with extremely rapid ramping rate could result in the faster SPER process, thereby leading to reduced dopant clustering and higher dopant activation [McCoy et al., 2004, Jain et al., 2004, Chao et al., 1997].

6.5 Dopant Activation of Ge-PAI Junctions with Various FLA Schemes

In this section, Hall effect measurements were performed on selected samples to extract both the active carrier concentration (N_s) and carrier mobility. The data of both as-flashed and 800°C post-annealed samples are shown in table 6.1.

Without any post-annealing (as-flashed), the pre-spike RTA + FLA sample exhibits lower N_s in comparison with those subjected to direct FLA with different number of pulses. However, its mobility has a reverse trend and shows greater mobility due to the lower ionized impurity scattering, possibly, as a result of better lattice repair by the pre-spike RTA step. The samples subjected single/multiple-pulse FLA have mobility values around ~20 cm^2/Vs.

Sample	Active Concentration (cm^{-2})			Mobility (cm^2/ V-s)	
	as-Flashed	Post-annealing 800°C	% Deactivation	as-Flashed	Post-annealing 800°C
Flash 1 Pulse	9.57×10^{14}	3.65×10^{14}	61.9%	20.0	34.2
Flash 3 Pulses	8.93×10^{14}	4.96×10^{14}	44.5%	20.9	32.9
Flash 6 Pulses	8.61×10^{14}	6.75×10^{14}	21.7%	21.5	29.5
Spike 950°C + Flash 1 Pulse	3.42×10^{14}	3.39×10^{14}	0.7%	30.7	32.8

Table 6.1: Hall effect measurements of samples with as-flashed conditions and subjected to post-annealing of 800°C for 60s (mean value).

In the cases where post-annealing at 800°C was carried out, it can be seen that the N_s drops across all the splits with respect to their own as-flashed counterparts.

This observation re-affirms that the increase of R_s at the same post-thermal temperature (800^{o}C) with respect to their as-flashed samples in figure 6.4 is not solely due to the change in mobility but also due to the reduction in the active dopant concentration. Furthermore, the de-activation percentage (normalized to the as-flashed sample) appears to be close to the percent change in R_s for the samples with different flash pulses, despite the variation in mobility that is being observed. For pre-spike RTA + FLA scheme, the reduction of N_s (~0.7%) seems to be lower than that in the R_s (~3.2%). It can be considered as the experimental errors or attributed to the more significant variation in its mobility values. Nevertheless, the changes of N_s and R_s values clearly indicate that the dopant de-activation is negligible when the pre-spike RTA is being applied.

6.6 SIMS Profiling of Ge-PAI Junctions upon Isochronal Post-annealing

Figure 6.6 to 6.8 shows the SIMS dopant distribution profiles under the various flash conditions followed by 3 different post-annealing temperatures. There is no major deviation in terms of the extent of diffusion for the as-flashed SIMS profiles among the various flash pulses. Thereby, 6 pulses as-flashed dopant profile is used as reference here.

After post-annealing at 700^{o}C (figure 6.6), the different B profiles subjected to various pulses of FLA show minimal dopant diffusion in the tail, and there is a noticeable kink at a depth of ~30 nm from the surface. The kink corresponds to the origin of EOR defect band, where the B atoms decorate the EOR defects during the

redistribution of dopants in the annealing process. From a careful analysis, it is clear that the kink after 6 pulses of FLA has a larger overall area than the 1 and 3 pulses of FLA. This implies that EOR defects initially consisting of small clusters or {113} defects may have transformed into the dislocation loops, bigger in size and more stable, thus trapping more B atoms around the EOR region [Mok et al., 2006]. This could be corresponded to the traces defects observed in figure 6.3(b) around the original PAI induced a/c interface. Since the dissolution of EOR defects for the pre-spike RTA happens before the FLA, a certain degree of diffusion in the low concentration tail profile is expected and B trapping is not being observed around the original a/c interface of pre-spike RTA + FLA sample.

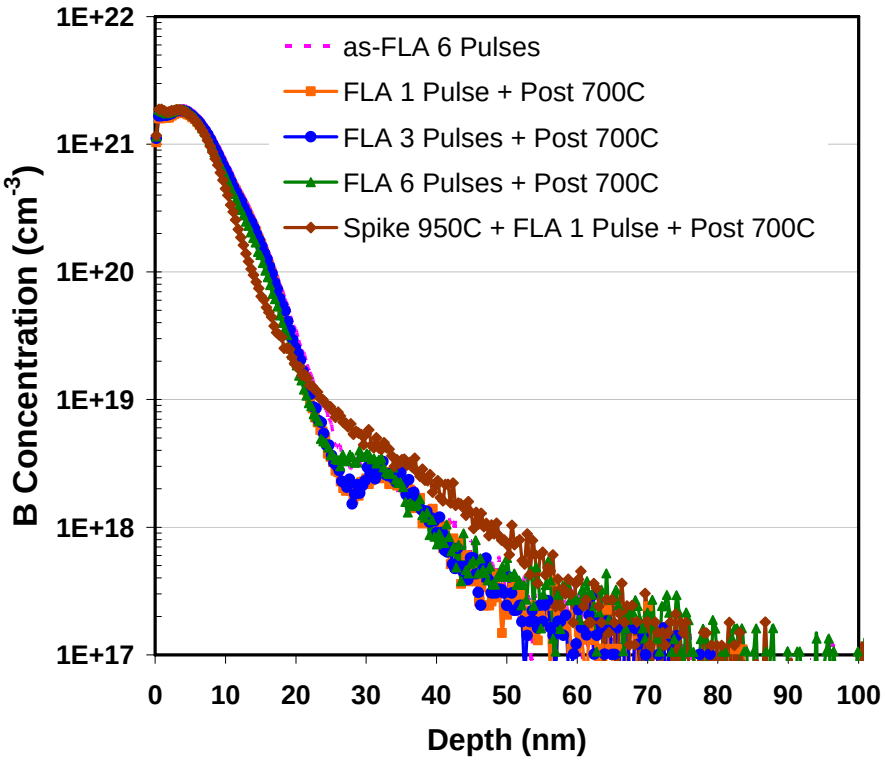


Figure 6.6: SIMS profiles of 1 keV B implant with prior 15keV Ge pre-amorphizing implant, after post-annealing at 700°C for 60s for the different flash annealing conditions.

When the temperature of post-annealing is increased to 800°C for 60s (figure 6.7), it is interesting to see that all the profiles with different flash schemes start to diffuse and arrive at similar junction depth.

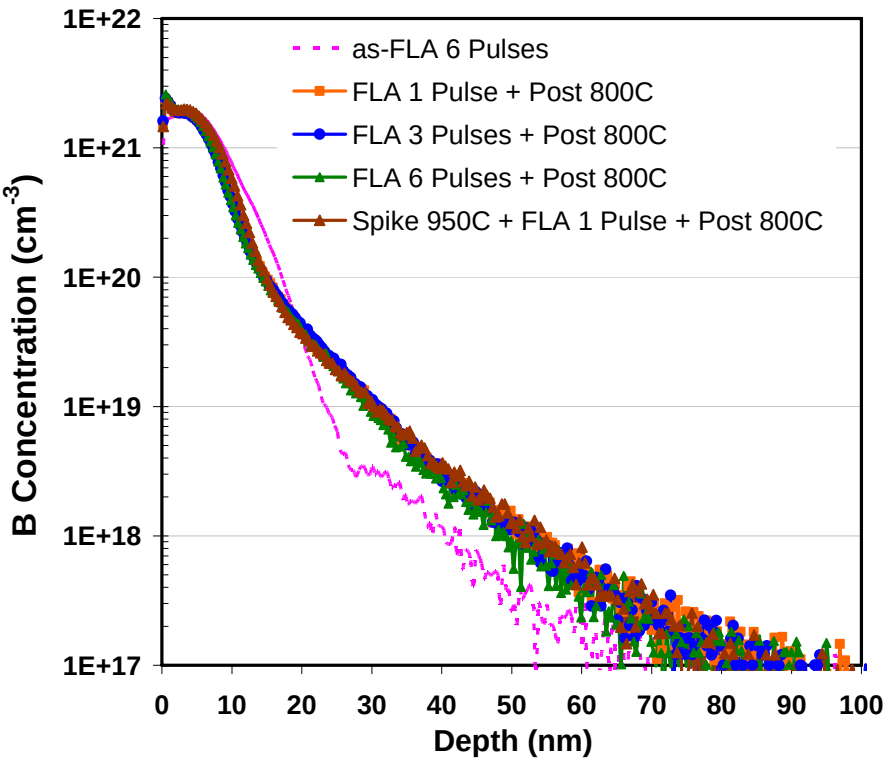


Figure 6.7: SIMS profiles of 1 keV B implant with prior 15keV Ge pre-amorphizing implant, after post-annealing at 800°C for 60s for the different flash annealing conditions.

The trapping of B atoms has diminished at the EOR region for the direct FLA with different pulses, which is presumably due to the dissolution of extended defects at this post-thermal anneal condition. It is also proposed that the level of silicon supersaturation is apparently much lower for the pre-spike RTA scheme. It can be inferred from the comparison of the diffusion length calculated by subtracting the junction depth at post-RTA temperatures from 800°C to the 700°C, where the

dopants diffuse less than 4 nm (at 1×10^{18} cm^{-3}) comparing to at least more than 8nm for the samples receiving 1, 3 or 6 pulses of FLA. In addition, it can be found that the 6 pulses of FLA provides the shallowest junction with a closer look at the tail of the B profiles, hinting that the possibility of variation in interstitial supersaturation when different number of flash pulse is applied.

Figure 6.8 shows another series of SIMS dopant profiles with a higher post-RTA temperature, 900°C for 60s. At this condition, the extended defects in EOR region is expected to have been completely dissolved.

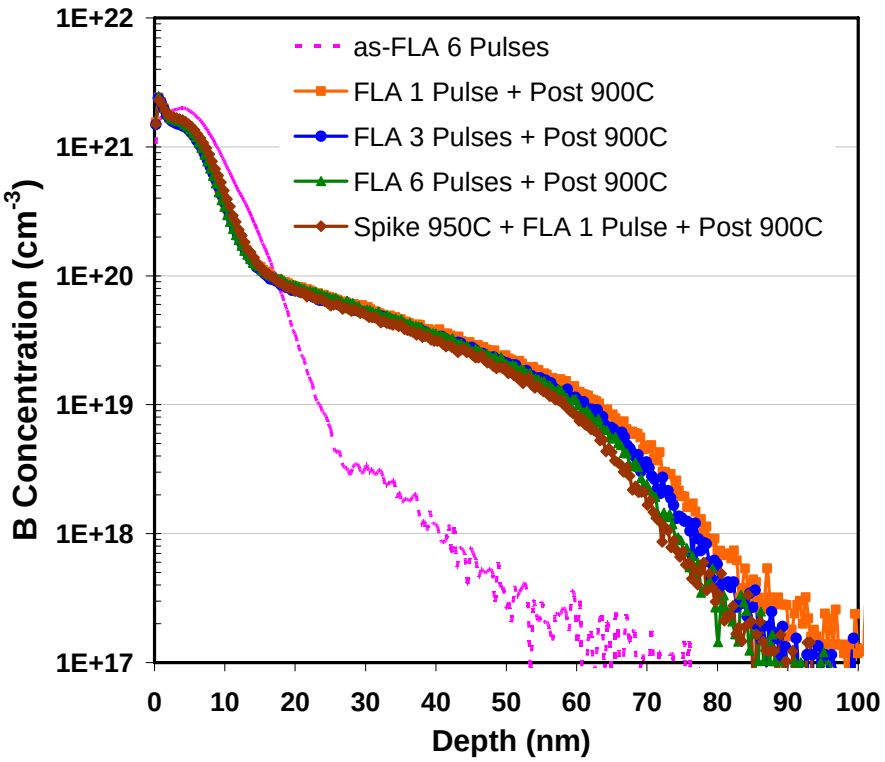


Figure 6.8: SIMS profiles of 1 keV B implant with prior 15keV Ge pre-amorphizing implant, after post-annealing at 900°C for 60s for the different flash annealing conditions.

Through the comparison of the diffusion depth among these profiles, one would able to quantify the relative magnitude of free interstitial supersaturation as

well as the B TED indirectly. It can be seen that the resulting junction depth is becoming shallower as the FLA pulse is increased from 1 to 3 and 6 pulses. The result validates the hypothesis that the interstitial supersaturation is decreased by increasing the number of FLA pulses, which possibly can be related to the reduction in defect density as well as transformation of small defects into more stable extended defects with the additional FLA pulse. Since the defect dissolution happens during the high temperature pre-spike RTA step, the supersaturation of silicon interstitials is expected to be at a lower level during its post-RTA. This explains the reason why the pre-spike RTA + FLA sample has the shortest diffusion length with the least B TED compared to the direct FLA scheme.

To provide a brief picture on what has been observed so far, figure 6.9 summarizes the junction depths of the Ge-PAI B doped samples based on the SIMS profiles with respect to the post-RTA temperatures.

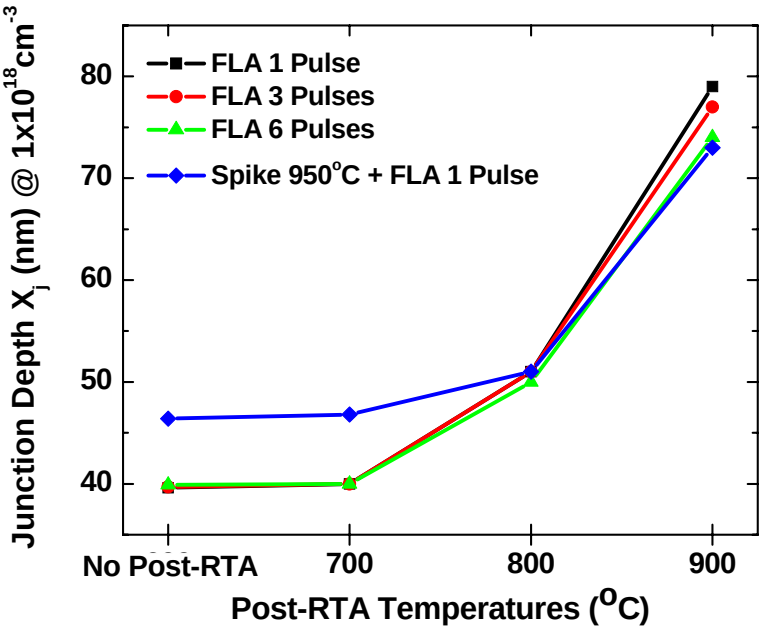


Figure 6.9: Junction depths of the Ge-PAI B doped samples subjected to the different FLA schemes plotted against the range of post-RTA temperatures.

Apparently, the post-RTA temperature of 700^{o}C does not lead to any significant B diffusion for the samples previously irradiated with the various FLA pulses. With this thermal budget, the defects at the EOR region go through the Ostwald ripening, building up the interstitial flux with respect to the surface or transforming smaller point defects into more stable extended defect state. As post-RTA is raised to higher temperatures, it is noticed that the junction depth and de-activation level (seen in figure 6.4) are significantly different across the samples which receive different number of flash pulses. This is attributed to the different level of silicon interstitial supersaturation among these samples during the dissolution of BICs and EOR defects, and hence results in different extent of B TED. For instance, as shown in XTEM early (figure 6.2), the density of defect can be reduced with the additional pulses of FLA. On this note, it is expected the initial interstitial supersaturation from the EOR region towards the surface is at a lower level for the sample processed with 6 pulses compared to 3 pulses and single pulse of FLA. Therefore, the peak de-activation level (in figure 6.4) and the TED effect seen at 900^{o}C (in figure 6.10), is getting smaller when the number of FLA pulses is increased.

On the other hand, the sample performed with the pre-spike RTA + FLA scheme has initially attained the larger junction depth due to the early interstitial supersaturation and dissolution of EOR defects prior to FLA. The evidence from XTEM (shown in figure 6.3(c)) reveals that the extended defects remaining with the pre-spike RTA flash scheme is clearly insignificant. Therefore, when the sample is subsequently processed with the post-RTA (shown in figure 6.10), the junction is relatively stable and associated with negligible B de-activation (shown in figure 6.4)

as a result of much lower silicon interstitial backflows from an EOR region. This also leads to an overall shortest diffusion length comparing to the direct FLA counterparts at the highest post-RTA temperature at 900°C.

6.7 Diode Leakage of Ge-PAI B Junctions with Various FLA Schemes

After the understanding of FLA effect on junction stability is being established, junction leakage characteristics of the p+/n diodes fabricated by various FLA schemes are investigated in this section. Figure 6.10 illustrates the I-V characteristics of the p+/n diodes.

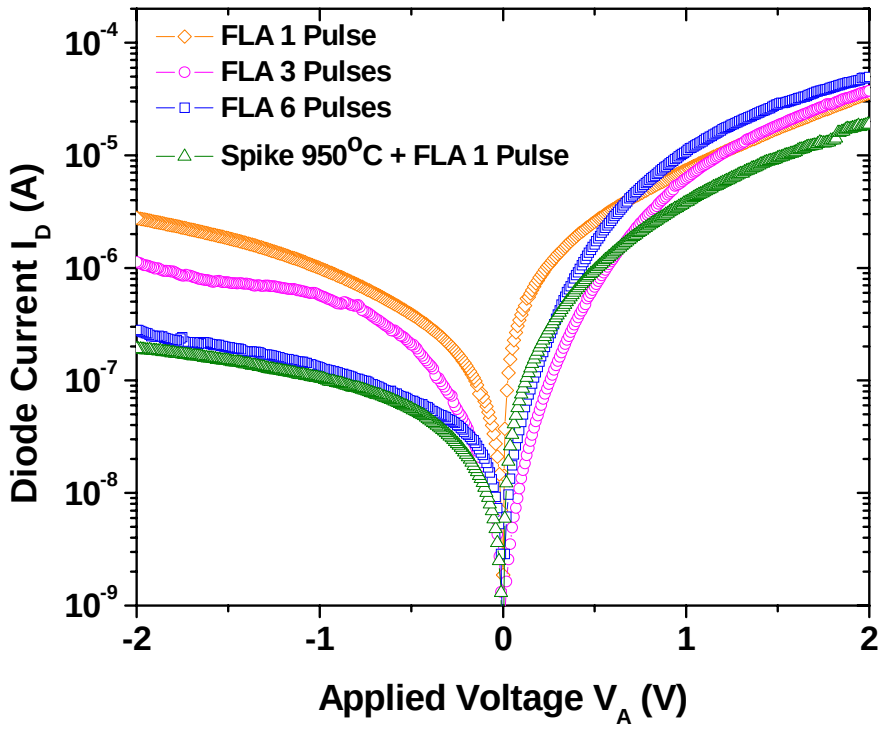


Figure 6.10: I-V characteristic of p+/n diodes (B junctions in n-type silicon) subjected to the FLA with (a) different number for flash pulses and (b) prior spike RTA schemes.

In the forward biased regime, it is observed that the 1, 3 and 6 pulses of direct FLA offer higher forward current comparing to its pre-spike RTA + FLA counterpart. This is consistent with earlier observation that higher dopant activation is achieved in the single/multiple-pulse FLA junction due to the much faster SPER process. However, it is also because of its extremely low thermal budget, the sample which received single pulse FLA displays the most leaky junction characteristic (referring to the diode current at -2V reversed biased) due to the presence of extensive non-dissolvable defects around the EOR region. Despite the inefficiency in the silicon defect removal, it is demonstrated that the leakage of the junctions can be improved gradually by having additional flash pulses. The sample subjected to 6 pulses of FLA is shown to have an order lower in its leakage current, closing to the level achieved by pre-spike RTA + FLA. This observation can be explained by the fact that pre-spike RTA treatment has effectively removed majority of EOR defects in the junction; while addition of FLA pulses (3 or 6 pulses of FLA) also aids in reducing the EOR defects and leads better lattice repairing. With the low concentration of residual defects present within the p+/n junctions, there are hence literally less alternative pathways of leakage for the current to flow.

6.8 Simulation of Ge-PAI Junctions with Single Pulse FLA and Pre-spike RTA + FLA Schemes

In this section, the focus is on the simulation of USJ formation process associated with the various FLA schemes, using an atomistic kinetic Monte Carlo simulator, known as DADOS (refer to section 3.5 for more details). The main

objection here is to investigate the evolution of residual implant-induced damage and junction stability after FLA processing in terms of diffusion, de-activation and re-activation of B upon subsequent isochronal thermal annealing. Simulations are also implemented to illustrate the underlying mechanisms involved in the pre-spike RTA followed by FLA.

The thermal profile used in the simulation of FLA process is shown in figure 6.11, where it can be clearly seen that FLA is in the regime of milli-second. Figure 6.12 shows the simulated cross-sectional TEM of the sample implanted with 15keV Ge with a dose of 5×10^{14} cm^{-2}, followed by 1keV B implantation with a dose of 2×10^{15} cm^{-2}. An amorphous layer of approximately ~27-28 nm is induced, which is closely similar to the experimental observation shown in figure 6.1.

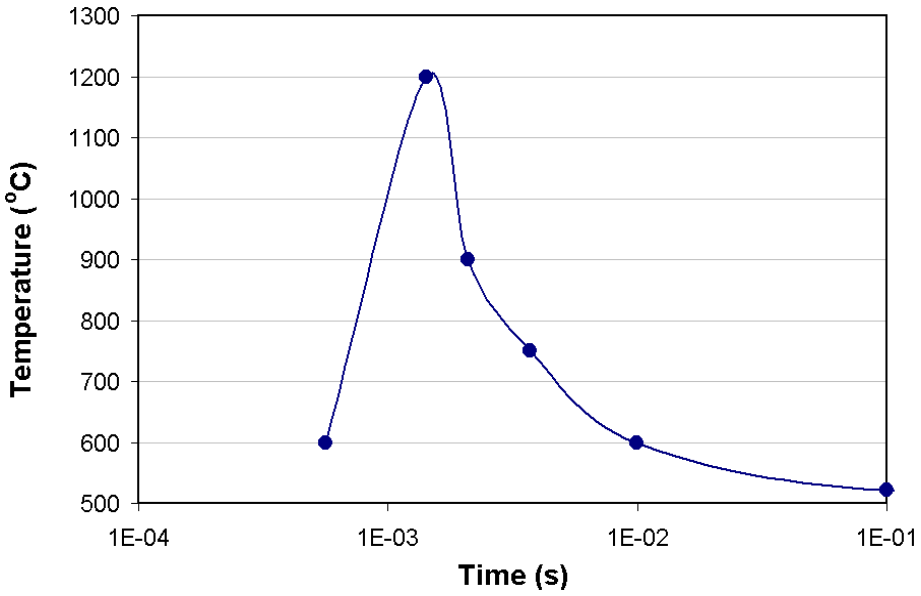


Figure 6.11: Temperature profile of the FLA process used in simulations.

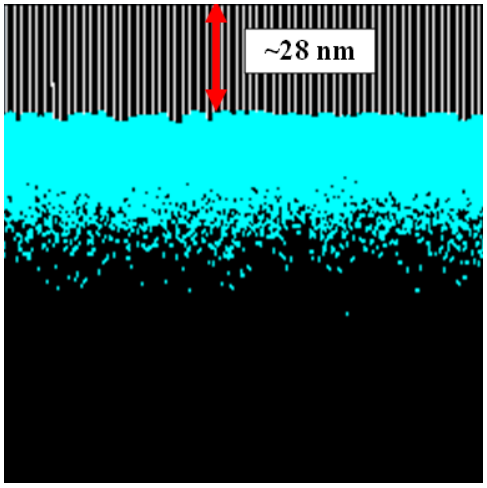


Figure 6.12: Simulation of the sample implanted with 15keV Ge with a dose of $5x10^{14}$ cm^{-2}, followed by 1keV B implantation with a dose of $2x10^{15}$ cm^{-2}, the resulted amorphous layer is around 28nm.

Subsequently, the single pulse FLA was simulated and reveals a clear defect band around the a/c interface. The simulated plan-view defect morphology is shown in figure 6.13. Analysis of the simulation results show that they consist mostly of small interstitial clusters and some extended {311} defects. It is noteworthy that for flash annealing, despite the very high temperature (1200^{o}C) reached, it does not fully dissolve the defects probably due to the extremely short thermal anneal duration [Lerch et al., 2005].

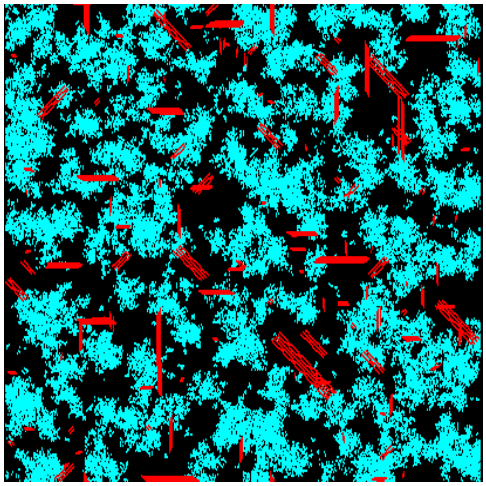


Figure 6.13: Simulated (100nm x 100nm) XTEM of the sample implanted with 15keV Ge with a dose of $5x10^{14}$ cm^{-2}, 1keV B implantation with a dose of $2x10^{15}$ cm^{-2}, followed by a flash anneal. Light blue defects represent small clusters and red defects are extended {311} defects.

On the other hand, figure 6.14 shows the simulation of the sample that was subjected to 950^{o}C pre-spike RTA. It is clearly shown that fewer defects remained with the addition of pre-spike RTA step, which is consistent with the observation from the XTEM shown in figure 6.3 of the early section. In addition, the defects remaining are more stable extended defects, like {311} defects and dislocation loops. Therefore, the simulated results clearly demonstrate that the additional thermal budget from the pre-spike RTA step has changed the emission of interstitials and subsequently the evolution of the extended defects.

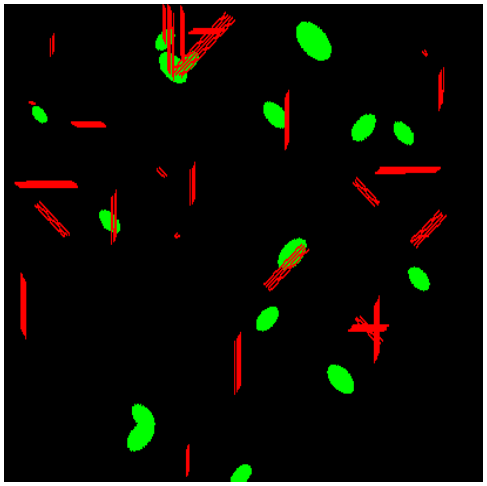


Figure 6.14: Simulated (100nm x 100nm) XTEM of the sample implanted with 15keV Ge with a dose of $5x10^{14}cm^{-2}$, 1keV B implantation with a dose of $2x10^{15}cm^{-2}$, followed by a 950^{o}C spike and a subsequent flash anneal. Red defects represent extended {311} defects and green defects represent the dislocation loops.

The different types of interstitial defects have different stabilities and contribute different interstitial supersaturation to the sample, resulting in different B diffusion. Although this has been experimentally shown in figure 6.6 to 6.8, simulations were carried out to verify the observations. Figure 6.15 shows the simulated dopant concentration profiles with single pulse of FLA and pre-spike RTA + FLA schemes at 2 different post-annealing temperatures. Figure 6.15 (a) shows the B concentration profiles at post-RTA of 700^{o}C. For the pre-spike RTA + FLA profile, the B has diffused most in the tail compared to the flash only profile. This is attributed to more of the defects have been annealed out during the spike RTA step for the pre-spike RTA flash sample compared to the sample which only receives single pulse of FLA. Since B undergoes interstitial-mediated diffusion, the defects annealed by the pre-spike RTA process would result in more B diffusion as shown in the obvious profile tail. Furthermore, in the near surface region, the pre-spike RTA

flash sample also shows B uphill diffusion due to the flux of interstitials from the EOR region diffusing to the surface. The trends comply with the early experimental SIMS shown in figure 6.6.

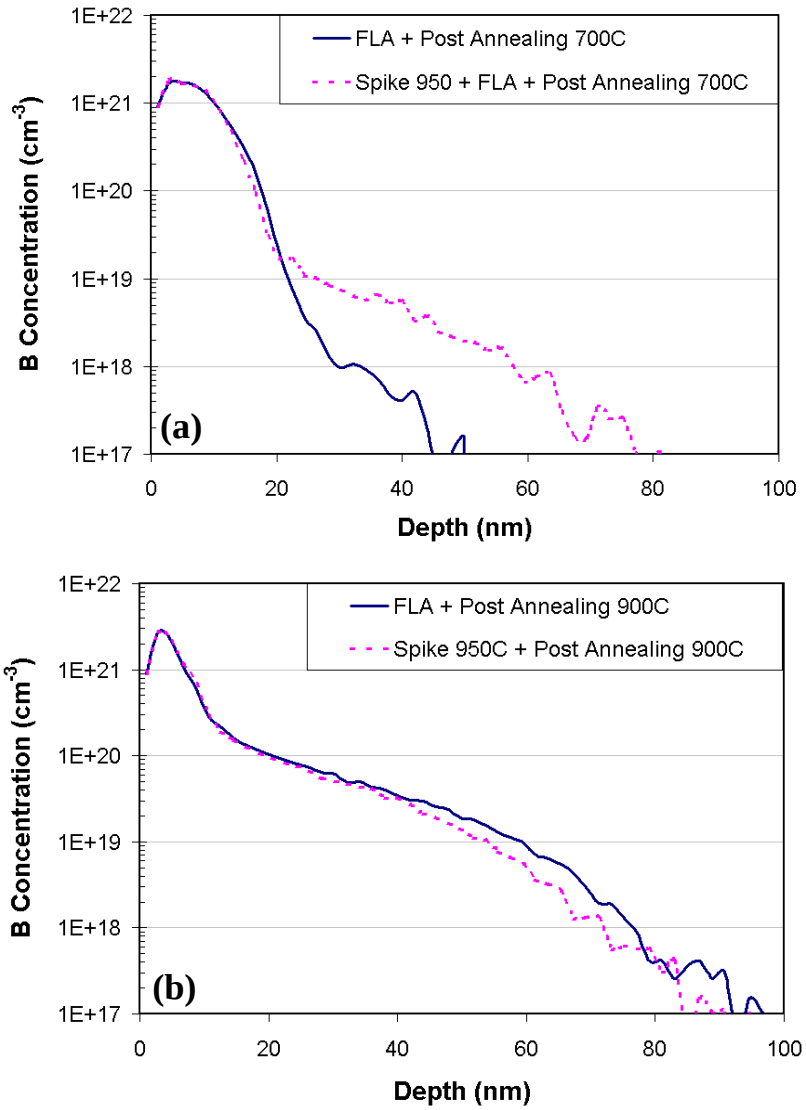


Figure 6.15 Simulated B concentration profiles after 15keV Ge with a dose of $5x10^{14}$ cm^{-2}, 1keV B implantation with a dose of $2x10^{15}$ cm^{-2}, subsequently either flash only annealed or 950°C pre-spike flash annealed, followed by (a) 60s, 700°C isochronal anneal (b) 60s, 900°C isochronal anneal.

Figure 6.15(b) shows the B concentration profiles post-annealed at 900^{o}C. In this case, the flash-annealed profile is more diffused instead comparing to the pre-spike RTA + FLA scheme. This key feature is also seen experimentally (figure 6.8). It is because for the pre-spike RTA followed by FLA, on top of the great amount of point defects has been effective reduced, the remaining defects are very stable dislocation loops (see Figure 6.14), leading to very low interstitial supersaturation and thereby resulting in less B diffusion. For the FLA only process, the defects do not nucleate in very stable dislocation loops after single pulse of FLA, so larger interstitial supersaturation would happen due to the higher silicon interstitial emission rate during the post-RTA.

In addition to the dopant concentration profiles, sheet resistance (R_s) was simulated as well to indicate its dopant activation, which is calculated by

$$R_s = \frac{1}{q\int_0^{x_j} \mu(x) C_B(x) dx}$$

where x_j is the junction depth, $C_B(x)$ the carrier concentration, $\mu(x)$ the concentration dependent hole mobility [Caughey et al., 1967], and q the electronic charge. Figure 6.16 shows the variation in sheet resistance as a function of annealing temperature, revealing the same trend as experimental results revealed in 6.4(b).

The simulation results clearly show that the pre-spike RTA + FLA offers a much more stable junctions than the flashed only sample; the difference in terms of de-activation level can be re-produced with respect to the experimental results. The detail description of the de/re-activation behavior has been illustrated in section 6.4.

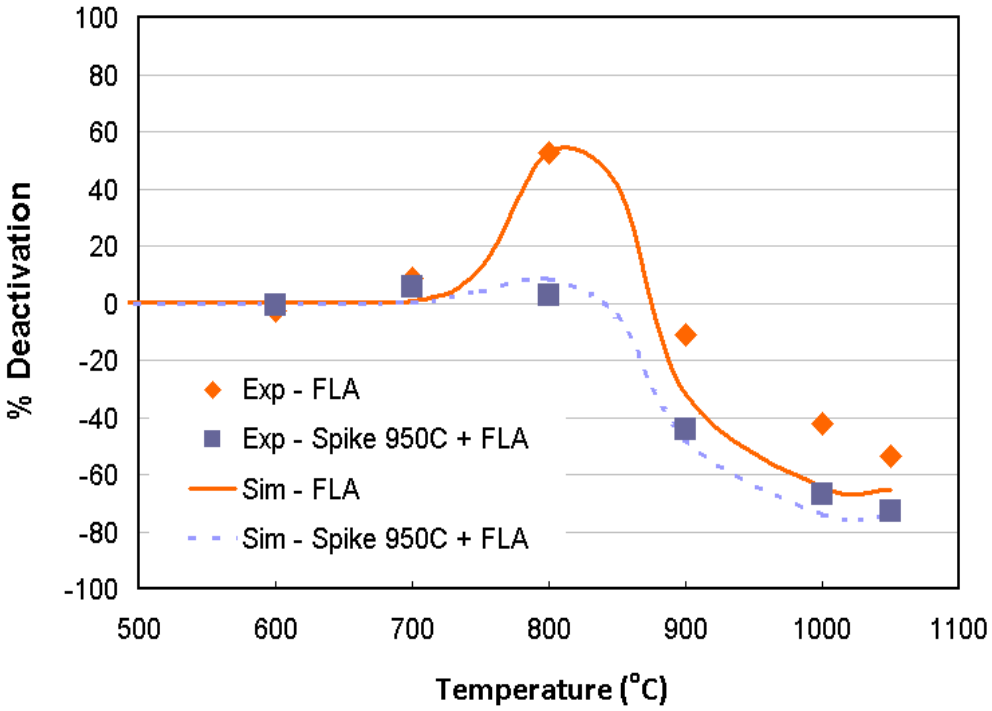


Figure 6.16: Percentage de-activation (measured by R_s and normalized to the post-annealing 600°C) as a function of annealing temperature, after 60s isochronal anneal following the flash-annealed or spike plus flash-annealed sample.

The thermal stability and evolution of the EOR defects can be more easily understood from the simulation as compared to the experiments. The total amount of interstitials and damage composition upon subsequent isochronal thermal anneals from 600°C to 1000°C were simulated. Figure 6.17(a) shows the total amount of interstitials retained in defects remaining as a function of annealing temperature, after 60s isochronal post-RTA. For the single pulse FLA sample, it is observed that it starts off with higher amount of damage, which completely dissolves by 800°C. However, the sample with pre-spike RTA followed by FLA starts off with less damage but persists up to 900°C.

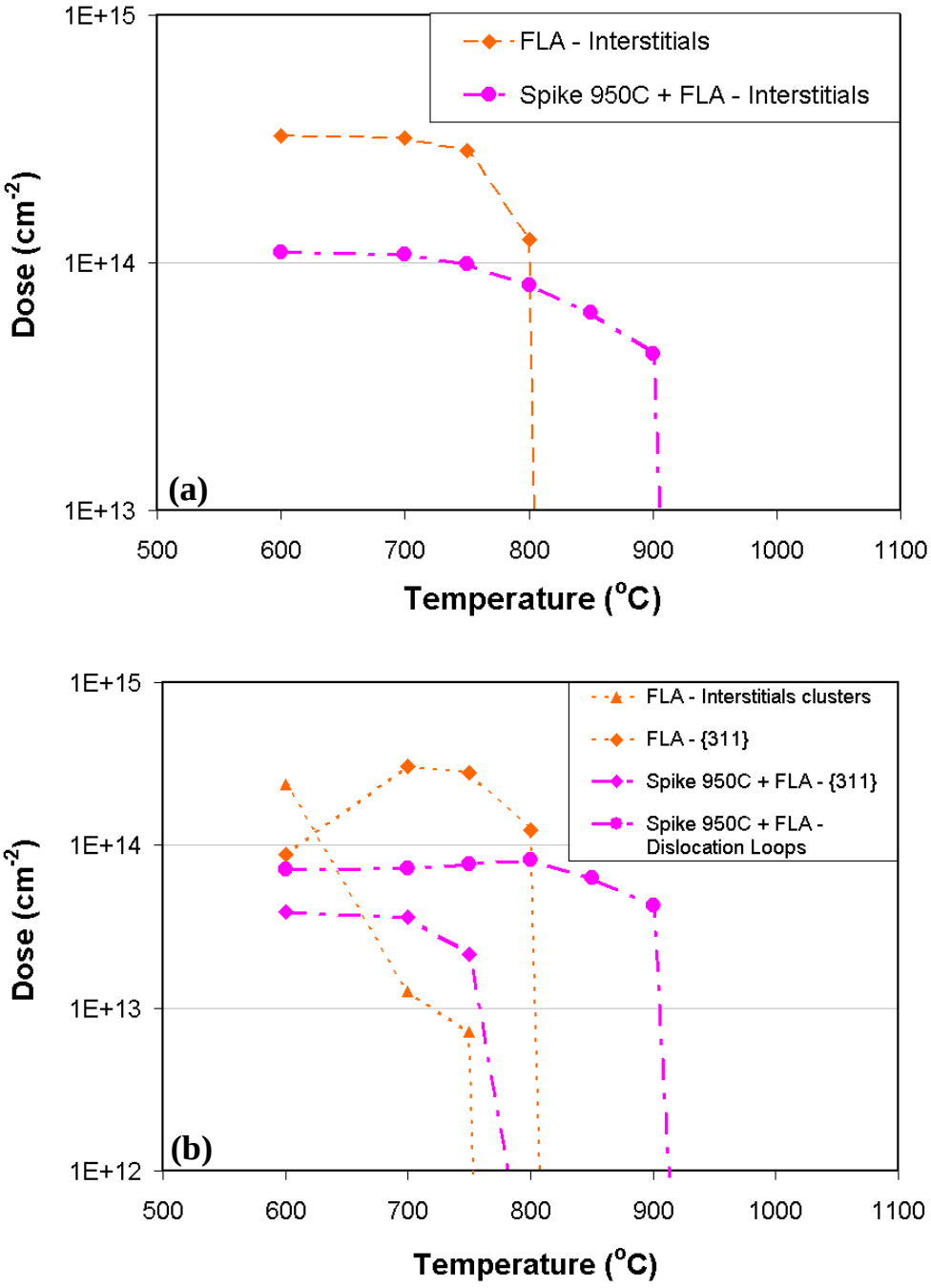


Figure 6.17: (a) Simulated total amount of interstitials after 60s isochronal anneal at various temperatures following the flash-annealed or spike plus flash-annealed sample. (b) Simulated total amount of interstitials and damage composition of the remaining interstitials after 60s isochronal anneal at various temperatures following the flash-annealed or spike plus flash-annealed sample.

Detailed analysis of the damage morphology can be seen from figure 6.17(b), which shows the simulated damage composition at different temperatures. The direct FLA sample with a 600^{o}C post-RTA consists mostly of small interstitial clusters and a small amount of {311} defects. The interstitial defects undergo Ostwald ripening whereby the less stable small clusters of interstitials dissolve and form more stable {311} defects. At 800^{o}C, both types of defects have completely dissolved. For the pre-spike RTA + FLA condition, simulations show that the dislocation loops have nucleated, and most of the interstitial defects are in dislocation loops, while some exist as {311} defects. The more stable dislocation loops remain and do not dissolve until the subsequent annealing temperature is more than 800^{o}C.

So far, simulations of dopant concentration profiles, dopant activation and damage remaining after post-RTA have been performed. The simulated results offer a clearer and more in-depth picture about the interactions between dopants and defects for FLA only and pre-spike RTA + FLA schemes. Schematic representations of the interstitial fluxes for the 2 different flash schemes are presented in figure 6.18.

For FLA only samples, dopant de-activation is observed as R_s increases with post-RTA temperature, up to a maximum at 800^{o}C, before dopant re-activation occurs followed by R_s rapidly decreasing (figure 6.16). The initial de-activation (increase in R_s) occurs during the ripening of EOR defects, which consisting mostly small interstitial clusters and less stable {311} defects (figure 6.13). The free interstitial point defects (released from the EOR) diffuse towards the B-rich surface, subsequently forming BICs, de-activating B in the process. It is because of its high density defects prior to post-RTA (figure 6.18), it leads to a greater interstitial flux

gradient from the EOR region towards the surface, driving more dopant de-activation via BICs and B TED when dopants are completely dissolved at post-RTA 900°C (figure 6.15 and 6.16). The subsequent dopant re-activation beyond 800°C, (decrease in sheet resistance) is due mainly to the dissolution of BICs in the absence of EOR defects.

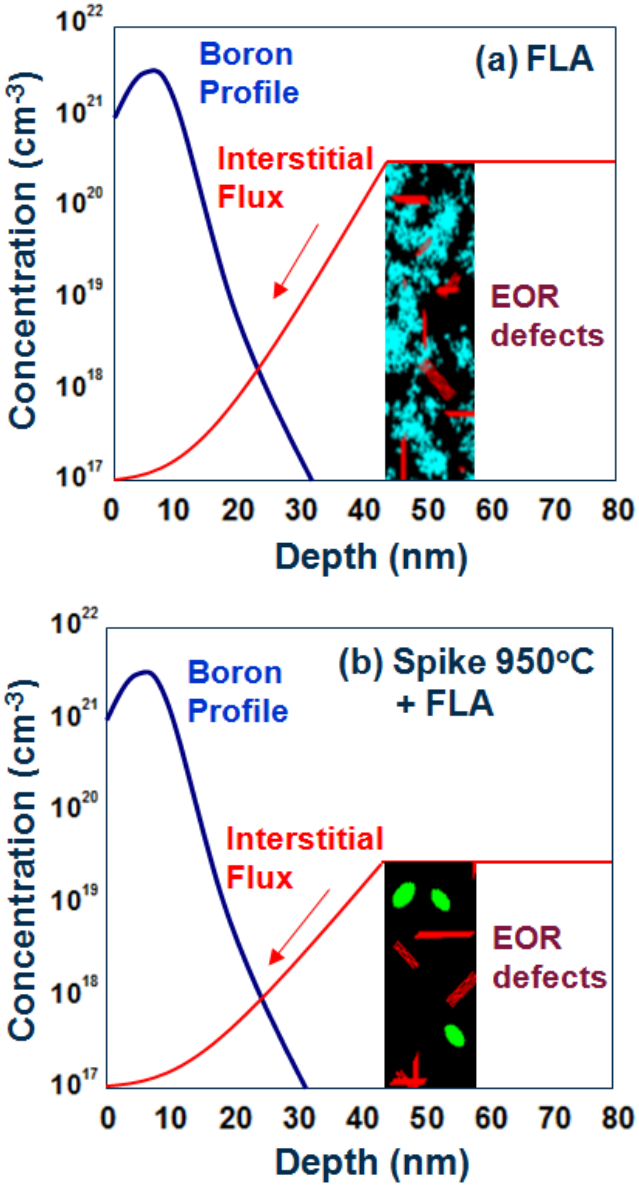


Figure 6.18: Schematic representation of the interstitial fluxes for (a) FLA and (b) pre-spike RTA + FLA schemes.

For the pre-spike RTA + FLA samples on the other hand, a great reduction of EOR defects is observed, attributing to the thermal effect of the pre-spike RTA prior to FLA (figure 6.14). There is only a slight de-activation at 800^{o}C, before the R_S decreases. This implies that there is a very small interstitial supersaturation up to 800^{o}C due to lower level of silicon interstitial emission, gaining from the reduced defect density and the formation of more stable extended defects during pre-spike RTA, demonstrated by simulations in figure 6.17(a) and (b) respectively. Moreover, it is possible that certain degree of de-activation process of the B has already occurred during the pre-spike RTA, so that there is little additional de-activation of B during the subsequent isochronal annealing. When the stable dislocation loops dissolve at 900^{o}C the supersaturation of interstitial occurs; however, the sample treated with pre-spike RTA remain to be shallower than the FLA only sample at post-RTA 900^{o}C, indicating its lower density of the extended defects. In addition, if the diffusion depth of B from 700^{o}C to 900^{o}C is taken into consideration, the reduction in B TED is very significant due to the much smaller initial interstitial gradient in the case of pre-spike RTA + FLA scheme (figure 6.18). Subsequent re-activation of B exists as a result to the dissolution of BICs at higher temperatures.

6.9 Summary

An in-depth study of Ge-PAI B junctions formed by various FLA schemes have been carried out. The results demonstrated that EOR defects can be reduced significantly by using multiple-pulse FLA or pre-spike RTA + FLA scheme. The pre-

spike RTA + FLA is shown to have better B de-activation suppression, but the multiple-pulse FLA scheme offers better activation in the preamorphized B doped junction. The junction leakage of single pulse FLA can be reduced by increasing the number of FLA pulses. With 6 pulses of FLA, junction leakage is reduced significantly associated with superior forward on current and able to match the leakage level achieved by the pre-spike RTA + FLA scheme. Therefore, the multiple-pulse FLA scheme has great potential for the application in actual devices.

In addition, it has also been demonstrated that the understanding of junction stability upon FLA can achieved via the defect evolution study complemented by kMC simulation. The simulated results have provided important insights on the damage morphology at different steps of the damage evolution in correlation to the B junction diffusion and activation.

In summary, a deeper physical understanding has been achieved on the USJ formation by the various optimized FLA conditions. The study has also proposed new FLA schemes which can reduce the junction leakage typically seen in the direct single pulse FLA processed B USJ.

Chapter 7

The Effect of Surface State on Boron Doped Pre-amorphization Junction for USJ application

7.1 Introduction

As CMOS evolves into sub-32 nm technology, the junction formation in the S/D extension region has become extremely ultra-shallow, which also means that the dopants are ever getting closer to the silicon surface. In this context, formation of ultra-shallow junctions (USJs) poses one of the major challenges. This is especially so for the PMOS where the conventional dopant, Boron, suffers from the transient enhanced diffusion (TED) and formation of electrically inactive boron-interstitial-clusters (BICs) [Stolk et al., 1997, Cowern et al., 1990]. These two anomalous behaviors have been well recognized as the underlying causes of increase in final junction depth (X_j) and sheet resistance (R_s) during the post-implantation annealing process.

Previous studies have reported that silicon surface is an efficient "sink" for the Si interstitial defects [Cowern et al., 1997]. Recently, Seebauer and coworkers have also shown by experiments [Seebauer et al., 2006, Zhang et al., 2006] and simulations [Krichenko et al., 2004a, 2004b], at which the silicon surface can be chemically manipulated in a controllable way to offer a particularly efficient pathway

for the annihilation of Si interstitials, leading to reduced diffusion and increased electrical activation of dopants upon annealing.

The manipulation seeks to create dangling bonds, to which Si interstitials can add with little activation barrier. Creation of an atomically clean surface leads to large numbers of dangling bonds, which act as a large sink that removes Si interstitials selectively over dopants in the interstitial sites. Such removal favorably impacts dopant TED and activation. Previous results pertained to crystalline silicon without PAI, however, the extension of these concepts to PAI-induced amorphous surfaces has remained unclear. Besides, the earlier works did not examine the most technologically problematic case of the boron dopant, and did not address EOR defect evolution.

The present study demonstrates experimentally that surface effects can also be exploited for B-implanted preamorphized silicon for USJ application. The main focus of this chapter is to investigate the interactions of surfaces, implanted dopants and the extended defects induced by PAI, involving the mechanism of interstitial insertion into the dangling bonds at the atomically clean surface.

7.2 Experimental Details

The experiments were performed on 8-inch <100>-oriented, Czochralski (CZ) grown, n-type silicon wafers with a resistivity of 6~9 ohm.cm. Ge was implanted at 15 keV to a dose of 3×10^{14} atoms/cm^2, resulting in the formation of a continuous amorphous layer at a depth approximately ~23-24 nm. The wafers were then implanted with boron at 500 eV to a dose of 1×10^{15} atoms/cm^2. All implants were

performed in single-quad mode at 0^o tilt and 0^o twist, and with native oxide thickness of 11±2Å covering the substrate surface. After implantation, some samples were pre-treated with 49% aqueous HF to remove the native oxide and thus create the atomically clean surfaces.

Annealing was carried out in an ultrahigh vacuum environment using Ta clips for resistive heating. The pressure in the chamber was maintained around 10^{-8}~10^{-9} torr during annealing to prevent formation of native oxide and contamination of the surface. In contrast, many RTA annealing studies reported in the literature have been performed in an inert N2 ambient at atmospheric pressure. Such environments was observed typically contain low, ill-defined levels of reactive gases such as oxygen or moisture [Gossman et al., 1995]. This is especially important since any form of adsorption may deactivate the dangling bonds at the atomically clean surface. The annealing conditions in this study were in the range of 700^{o}C to 950^{o}C for 60 minutes.

Dopant profiles were analyzed ex-situ with CAMECA 6f SIMS with oxygen source. A primary beam of O2+ ions with net energy of 0.5 keV or 1 keV at 56° incidence was scanned over an area of 250 x 250 μm^2 for B profiling. Sheet resistance (R_s) was measured by standard four point probe; while the active carrier concentration (N_s) was obtained from Hall measurement assuming a unity Hall scattering factor. Cross-sectional TEM (XTEM) was performed to analyze the extent of amorphization and the induced end-of-range (EOR) defects.

7.3 The Effect of Surface State on Boron Diffusion

Figure 7.1(a) shows the B diffusion profiles after annealing at 700°C for 60 minutes in ultra high vacuum chamber.

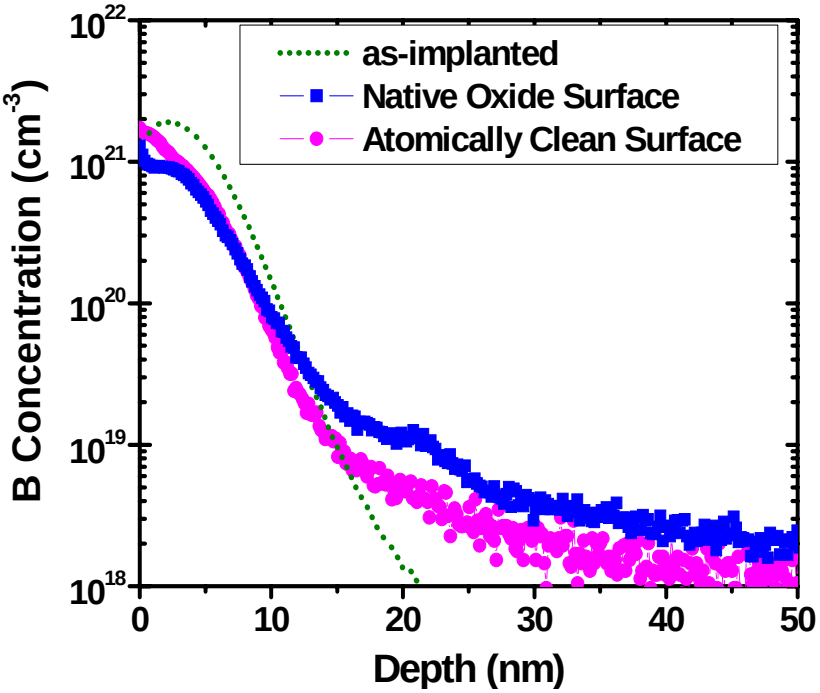


Figure 7.1: SIMS profiles of 500eV B implant after 15keV Ge pre-amorphizing implant, ultrahigh vacuum annealing was performed on native oxide and atomically clean surfaces at 700°C for 60 minutes.

Both the native oxide-covered and atomically clean surface samples exhibit surface-directed diffusion (boron uphill diffusion) at the high concentration portion of the B profiles. It is in agreement with the findings reported by Wang et al. and Duffy et al. [Duffy et al., 2003, Wang et al., 2001]. The phenomenon is attributed to the interstitial flux induced by the evolution of EOR defects located around the a/c interface during the annealing. The results show that clean surface sample has a dopant profile at which high B concentration region (<15 nm) diffuses more towards

the surface; while the native oxide sample on the other hand reveals that the tail of its B profile is diffusing deeper into the substrate. In addition, it is observed that there is a small trapping peak found at the depth of ~21-22 nm for the untreated native oxide surface sample. This B trapping peak is initiated from the decoration of B on the EOR defects and is an indirect indicator of the amount of defects remaining [Duffy et al, 2003, Cowern et al., 2003]. The disappearance of B trapping in the atomically clean surface state suggests that the complete or better dissolution of EOR defects in the sample.

Although it has been previously reported that silicon surface generally serves as a good sink for free interstitials, the efficiency of the interstitial annihilation between atomically clean and native oxide surface has not been identified. Based on above observations, one could possibly speculate that the defect annihilation at surface varies when its surface condition is changed. The interactions of dopants with silicon interstitials and the evolution of EOR defects may as well be affected.

Figure 7.2(a) and (b) show the corresponding SIMS profiles after annealing at 800^{o}C and 900^{o}C. Substantial TED diffusion is observed for both surface states due to the excess interstitials emitted from the EOR defects and dissolution of BICs at a higher thermal budget annealing [Stolk et al., 1997, Lindsay et al., 2002]. Nevertheless, the suppression of TED is becoming clearer, and junction depth has been reduced by approximately ~50 nm (at 800^{o}C) and ~70 nm (at 900^{o}C) at concentration of by 1×10^{18} cm^{-3} when comparing the native oxide to atomically clean surface. The junction abruptness is also improved together with the TED.

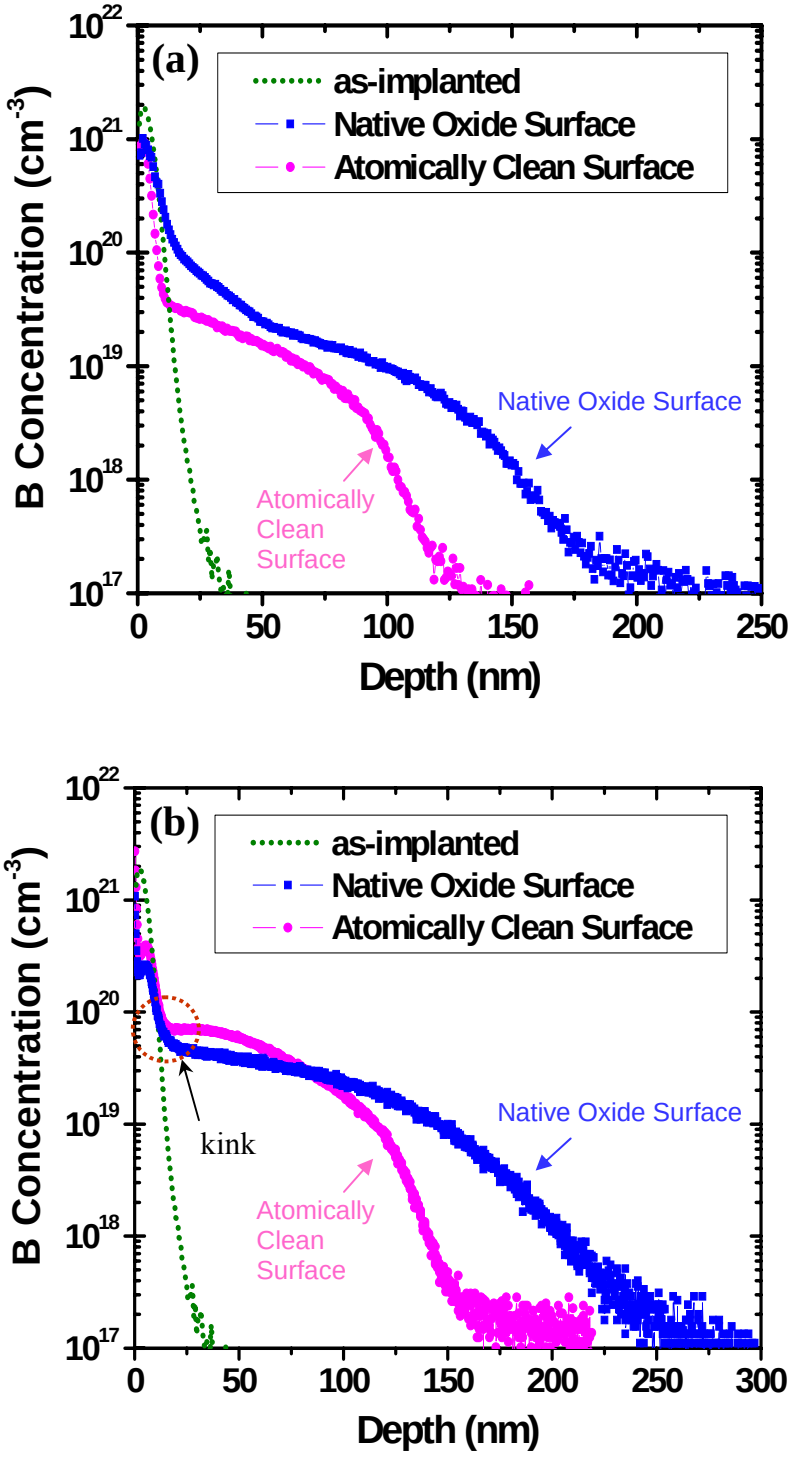


Figure 7.2: SIMS profiles of 500eV B implant after 15keV Ge pre-amorphizing implant, annealing was performed on native oxide and atomically clean surfaces at (a) 800°C and 900°C for 60 minutes.

Furthermore, it is worth to note that the "kink" concentration in the B profile of native oxide sample increases from ~5x10^{19} cm^{-3} to ~7.5x10^{19} cm^{-3} when subjected to vacuum annealing at 900^{o}C. The "kink" in the profile is generally known to signify the B concentration which starts to diffuse out of the initial implant distribution and subsequently being electrically activated. The difference in the "kink" concentration level suggests that the sample annealed under the atomically clean surface may have higher dopant activation level.

7.4 The Effect of Surface State on Boron Activation and Deactivation

7.4.1 Hall Effect Measurement

The samples from previous section were characterized by Hall effect measurement to study the electrical response of the B with respect to their surface states. Figures 7.3 shows the R_s and N_s obtained from Hall effect measurements. It is observed that the R_s measured for 700^{o}C shows a higher value for atomically clean surface; while reverse trend (lower R_s) is seen when moving to 800^{o}C and 900^{o}C. In term of N_s, as expected, an inverse relationship with the R_s is noticed. In particular, the reduction of R_s values, under the two higher anneal conditions (800^{o}C and 900^{o}C), can be clearly attributed to the improved B activation since the gain in the measured carrier mobility (shown in figure 7.4) is very small for the oxide-free clean surface and its B profiles are also shallower (shown in previous section). The conclusion of greater dopant activation is in agreement with the high B "kink" level at the 900^{o}C

SIMS profiles (shown in figure 7.2(b)), certifying that benefits of improved dopant activation and reduced TED can be obtained when the samples are annealed under the atomically clean surface condition.

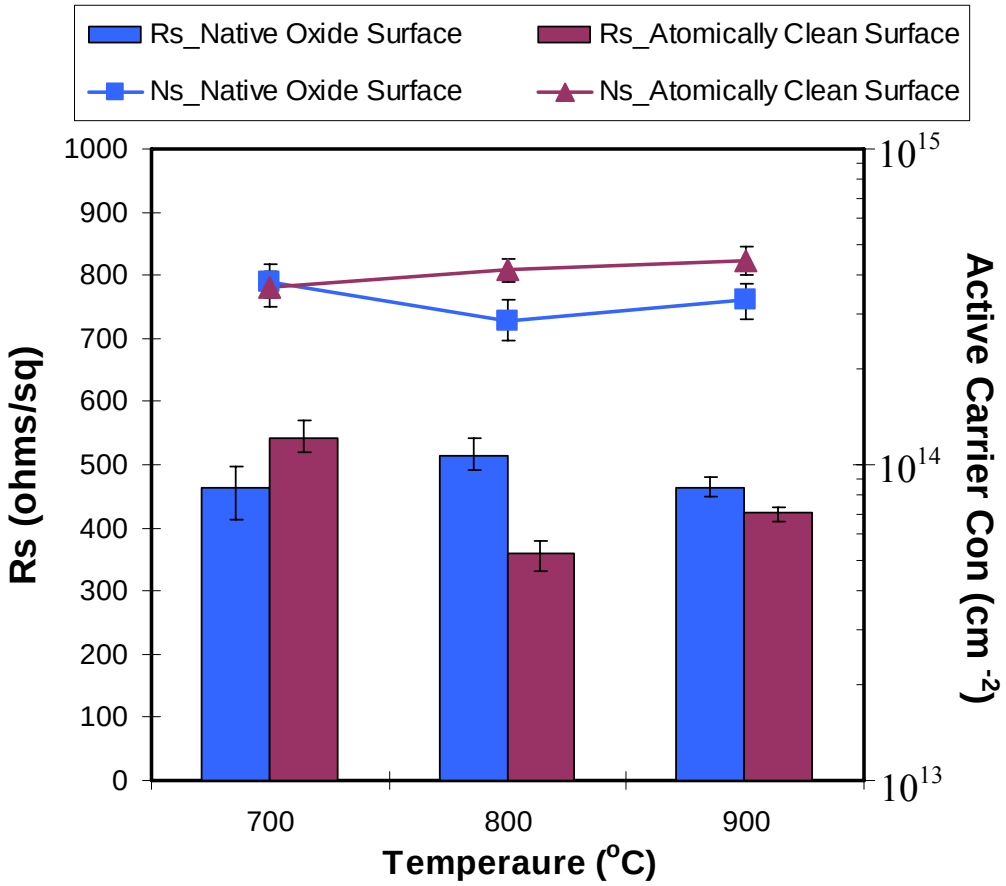


Figure 7.3: Sheet resistance (R_s) and active carrier concentration (N_s) of the native oxide and atomically clean surface samples subjected to ultrahigh vacuum annealing at 700°C, 800°C and 900°C for 60 minutes.

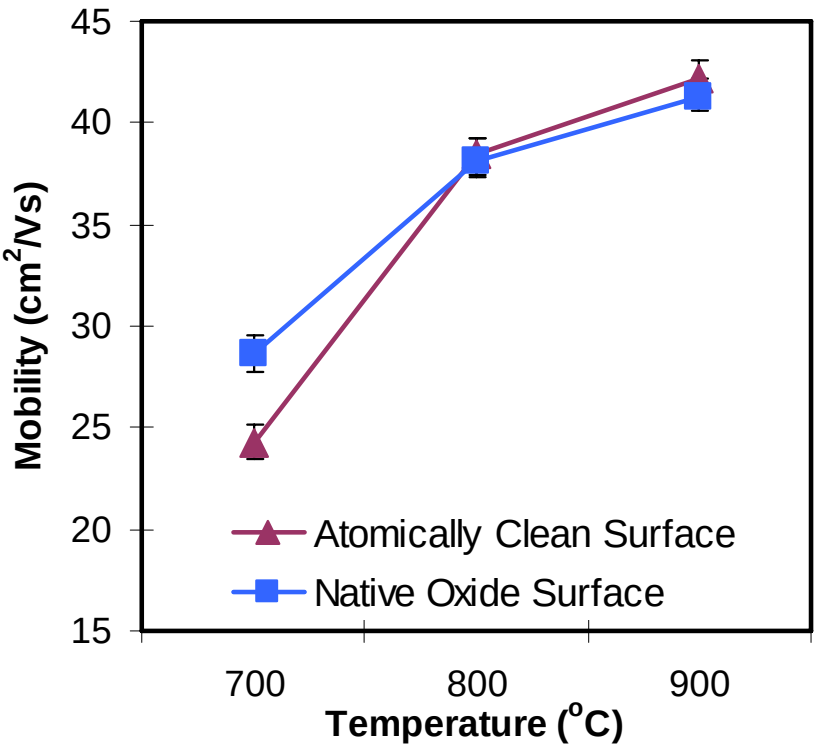


Figure 7.4: Mobility of the native oxide and atomically clean surface samples subjected to ultrahigh vacuum annealing at 700°C, 800°C and 900°C for 60 minutes.

Despite the fact that better activation has been demonstrated for the atomically clean surface above 800°C, it is essential to know why the oxide-free surface reveals higher R_s and lower level of N_s at the low annealing temperature of 700°C. With a closer look into the figure 7.3, it is noticed that the extent of R_s change (~14.8%) is not completely reflected by the slight difference in N_s (~3.9%), as the mobility of the clean surface case is significantly lower than the native oxide sample (~18.1%). The smaller N_s can be explained by a higher dopant loss when the native oxide is removed during the SPER process; while the significantly lower mobility value is possibly due to higher dopant segregation in the first 2-3 nm of surface as seen in figure 7.1. These segregated dopants are in the inactive states at the surface and could become the

scattering sites which substantially degrades the mobility. In other words, when atomically clean surface is subjected to a low temperature annealing at 700^{o}C, it undergoes the SPER process with minimum B diffusion, where it experiences dopant loss during this stage which leads to a slightly smaller in N_s. However, its higher R_s is believed to be dominant by the degradation of the mobility as a result of dopant segregation at the surface. Figure 7.4 shows that the mobility of the clean surface can be quickly recovered if the annealing temperature is increased, providing more thermal energy for dopant activation and lattice repair.

7.4.2 Isochronal Annealing

To further investigate the interactions of B dopants with defects, an electrical stability study with isochronal annealing was carried out. A series of samples were subjected to annealing at temperatures ranging from 700^{o}C to 950^{o}C for 60 minutes. For a surface with native oxide, figure 7.5 shows that R_s initially increases as the temperature progresses upward from 700^{o}C. R_s peaks at 850^{o}C, and decreases at higher temperatures. Such behavior can be explained by the evolution and ripening of EOR and BIC defects. Initial SPER occurs at 700°C and is completing by the end of the annealing. During SPER, dopant atoms move into electrically active substitutional sites in the crystal lattice, and excess interstitials nucleate into BICs and EOR defects. Annealing with temperatures up to 850°C releases free interstitials from the EOR defect band. The interstitials diffuse toward the B-rich region and interact with electrically active boron to form BICs in addition to those already present – a process that deactivates a large extent of the dopants. As the annealing temperature increases

further, the BICs dissolve leading to dopant re-activation together with a reduction in R_s. This behavior is generally well known as "reverse annealing", and observed in typical Ge-PAI B doped junctions [Colombeau et al., 2004b].

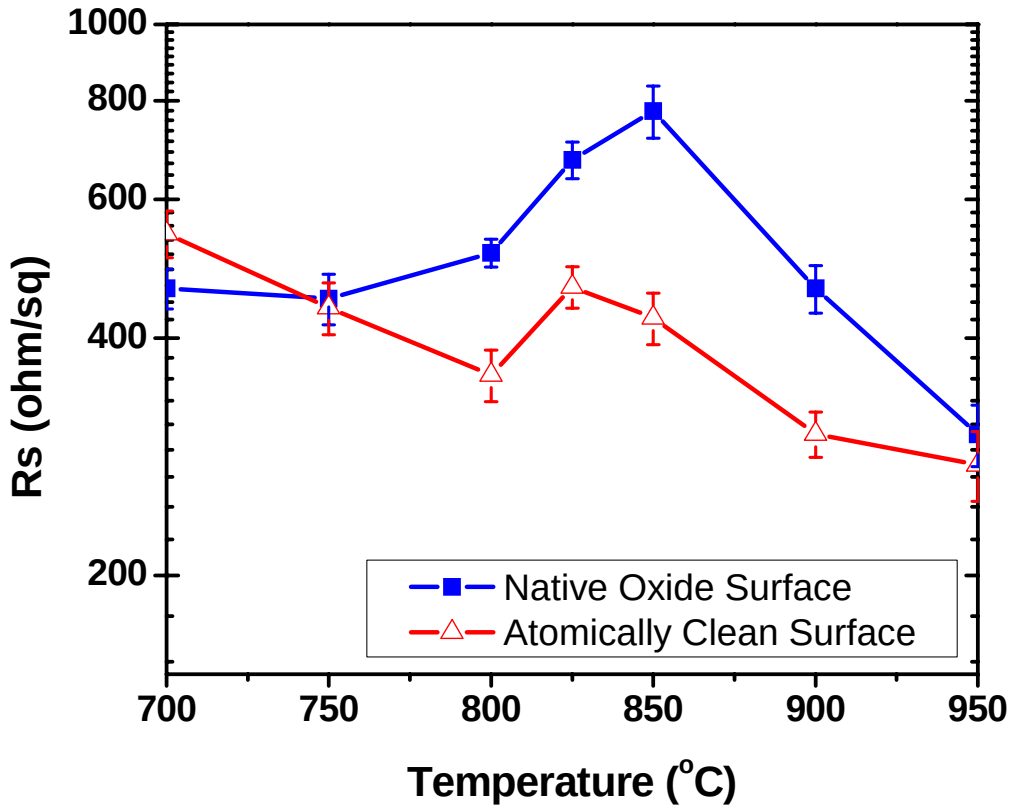


Figure 7.5: Sheet resistance (R_s) as a function isochronal annealing temperature. Squares represent the native oxide surface, and the triangles represent the atomically clean surface.

Interestingly, the result shows very different behavior for an atomically clean surface. The value of R_s at 700°C starts out higher than that of native oxide. This difference is possibly due to increased dopant loss and segregation at the surface as mentioned previous section (section 7.4.1) when the native oxide is removed, which agrees with the higher degree of B movement towards the surface as illustrated in the

SIMS profile of figure 7.1. At higher temperatures, however, R_s decreases continuously for the atomically clean surface until 800°C. R_s then peaks briefly at 825°C before continuing its downward trajectory. Thus, for the atomically clean surface "reverse annealing" is much less pronounced, yields a peak about 25°C lower in temperature, and leads to relatively lower R_s at most temperatures. The variation in deactivation level, particularly the lowering and shifting of R_s, is one key feature to indicate that the atomically clean surface sample experiences different dopant-defect interaction pathways, as well as possibly higher EOR defect dissolution rate during the thermal annealing.

7.5 The Effect of Surface on EOR Defects

To further investigate defect structure in the EOR region under 2 different surface states, the native oxide and atomically clean samples annealed at 750°C and 850°C were examined by XTEM.

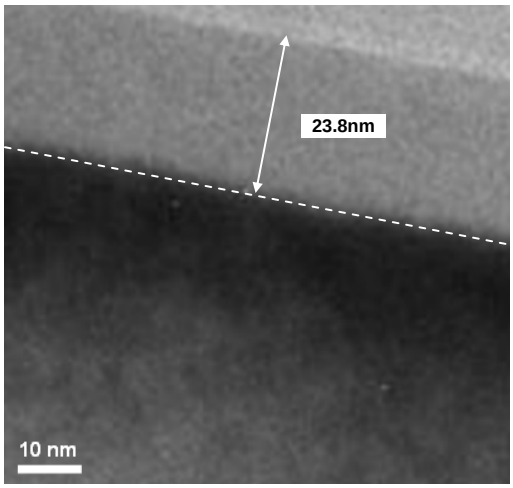


Figure 7.6: XTEM micrograph of the sample as-implanted with 15keV, 3×10^{14} cm^{-2} Ge followed by 500eV, 1×10^{15} cm^{-2} B.

Figure 7.6 shows a continuous amorphous layer of about 23-24 nm resulted from the 15 keV Ge and 500eV B implants prior to thermal annealing. A smooth and clear demarcation between the amorphous and crystalline phases is observed.

Figure 7.7(a) demonstrates the native oxide covered case, where a significant dark band remains around the previous a/c interface, corresponding to the EOR defects formed after the SPER of the amorphous layer at the anneal temperature of 750^{o}C. For the atomically clean surface depicted in figure 7.7(b), it does not show the presence of residual remaining EOR defects around the same location. Indeed, the results re-affirm the early prediction from SIMS measurements (as discussed in Chapter 7, section 3), the EOR defects in clean surface samples are mostly dissolved.

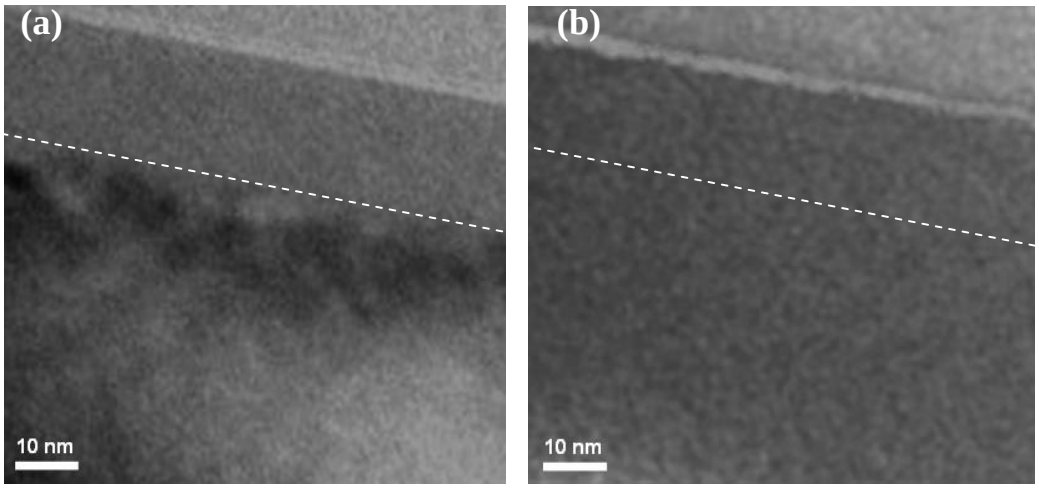


Figure 7.7: XTEM micrographs of (a) native oxide and (b) atomically clean surface samples after annealing at 750^{o}C for 60 minutes. Dotted lines are drawn to show the a/c interfaces.

Increasing the annealing temperature to 850^{o}C as illustrated in figure 7.8, the defects in the EOR region for the native oxide surface are still visible but they are clearly reduced as a result of dissolution of the extended defects at the higher anneal

temperature. The atomically clean surface sample on the other hand remains free of defects at the pre-annealing a/c interface. XTEM results are the strong evidence in supporting the hypothesis of the sink effect or interstitial annihilation efficiency is higher in the case of atomically clean surface, and which possibly promotes the EOR dissolutions rates subsequently.

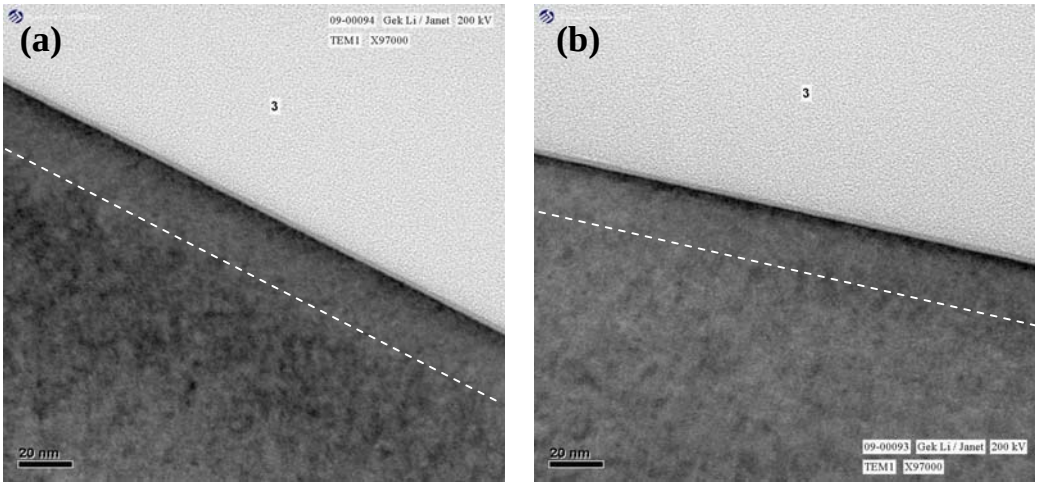


Figure 7.8: XTEM micrographs of (a) native oxide and (b) atomically clean surface samples after annealing at 850^{o}C for 60 minutes. Dotted lines are drawn to show the a/c interfaces.

7.6 The Effect of Surface State on Surface Morphology

As described in the experimental detail section, the atomically clean surface was prepared by the treatment of HF and it was then followed by thermal annealing cycle. Therefore, the surface condition of junction, particularly the morphology, could be a concern for USJ application in device. Figure 7.9 (a) to (d) show the 3 dimensional AFM images of the 2 different surface states subjected to thermal annealing of 750^{o}C for 60 minutes.

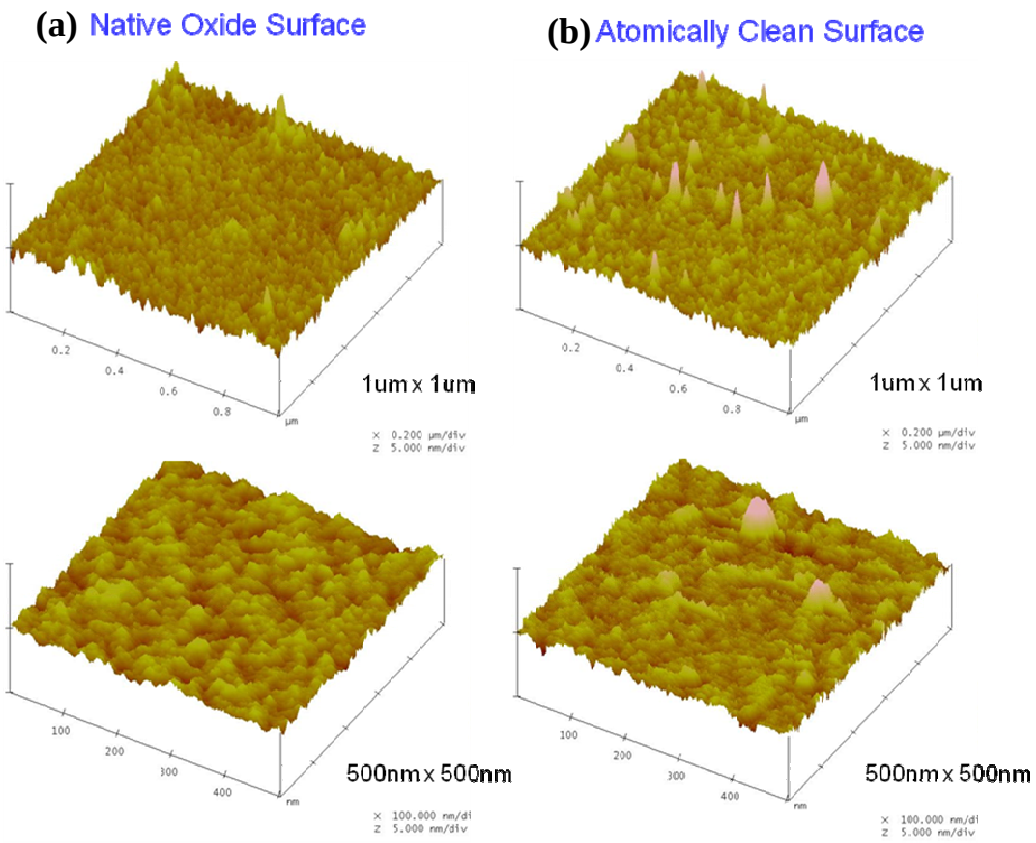


Figure 7.9: Top-view AFM scans of the (a) native oxide and (b) atomically clean surface samples subjected to vacuum annealing at 750^{o}C for 60 minutes. Two scanning dimensions were performed: the upper images are 1 µm × 1 µm and the lower images are 500 nm × 500 nm.

As observed from the scanned images, the native oxide-covered sample remains relatively smoother than the atomically clean sample. The root-mean-square roughness (RMS) of these samples is summarized in figure 7.9 with scanned area of 500nm×500nm and 1µm×1µm. It shows that the difference in RMS between the 2 surface states is within a 0.5nm range regardless of the variation in scanning dimension, suggesting that only minimum surface damage and reorganization were

caused during the HF treatment and after junction formation by ultra high vacuum annealing.

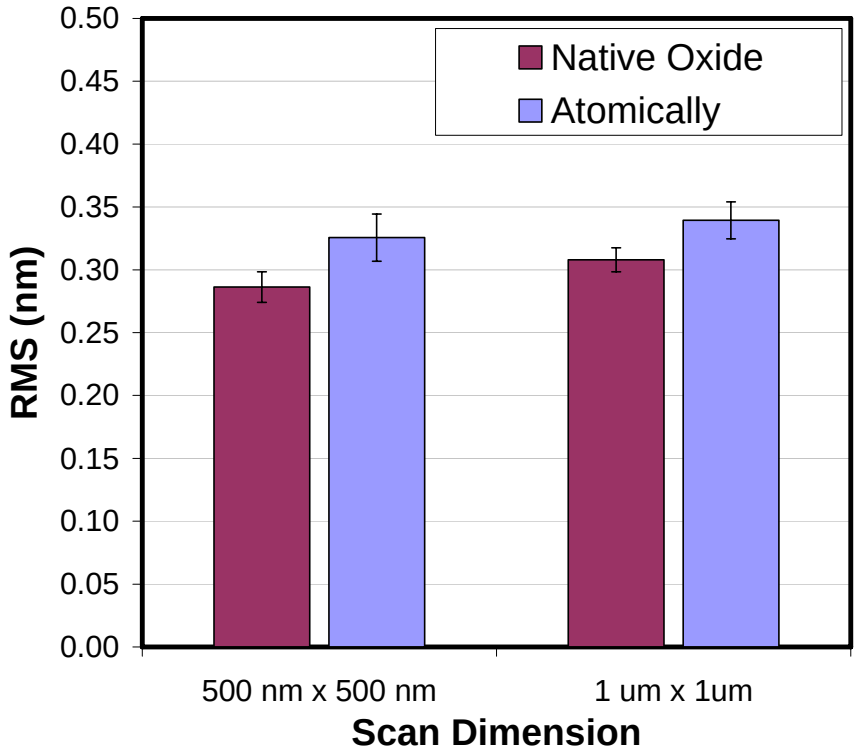


Figure 7.10: The root-mean-square roughness (RMS) extracted from the AFM images of the native oxide and atomically clean surface samples.

7.7 The Theory and Explanation of Surface State Effect on B Junction Formation

Based on the observations from above results, an overall picture and simple explanation of the surface effect on the Ge-PAI B junction formation is described below. Extended defects in the EOR region, induced by Ge-PAI, emit free Si interstitials during annealing process and the surface can serve as a sink for many of those free Si interstitials. Indeed, Cowern *et al.* have previously demonstrated that the

degree of interstitial supersaturation decreases significantly with respect to the depth from the EOR defects toward the surface, when an oxide is in place [Cowern et al., 1997]. In the atomically clean-surface case, it is shown in this work that the degree of supersaturation near the surface can be even lower than the oxide covered surface, because of the enhanced ability to annihilate interstitials at surface dangling bonds. Therefore, it results in a steeper supersaturation gradient from the EOR region towards the surface. A schematic representation of the scenario is proposed and shown in figure 7.11.

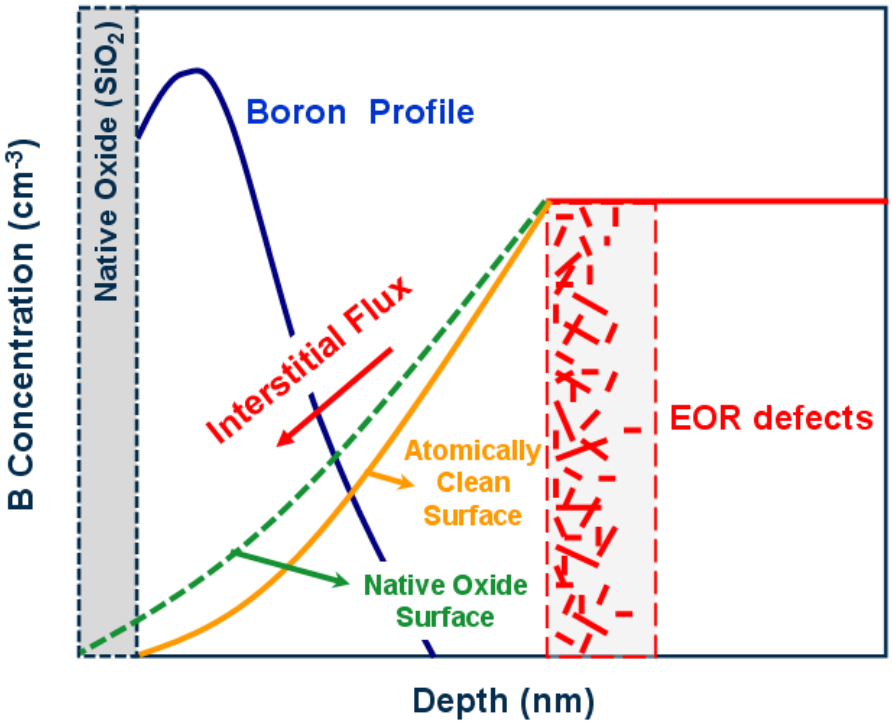


Figure 7.11: Schematic diagram showing the silicon interstitial supersaturation from EOR region towards surface. Atomically clean surface sample is proposed to have steeper supersaturation gradient than the native oxide surface case shown in figure.

The extra depletion of interstitials near the clean surface alters the way interstitials interact with dopant, leading to changes in the dopant profiles and its

activation/de-activation behavior. For instance, the extra depletion leads to a steeper concentration gradient of interstitials and a correspondingly stronger flux toward the clean surface during early stage of the SPER of the Ge-PAI junction. This is shown in the 700^{o}C annealing, at which larger extent of uphill B diffusion and B segregation have been observed (figure 7.1). Also, the higher rate of interstitial annihilation at the clean surface promotes higher EOR defect dissolution rates, resulting in smaller numbers and sizes of extended defects as seen from the XTEM results (figure 7.7 and 7.8). Therefore, it is expected the interactions of B with the interstitial are greatly reduced when B diffusion and extended defects dissolution is taking place at higher annealing temperature (>800^{o}C). Validation of such a hypothesis is evidenced by the significant suppression of B TED and improvement in dopant activation when the sample is annealed under the atomically clean surface state (figure 7.2 and 7.3).

7.8 Summary

In summary, the chemical state of surface is demonstrated to have a significant impact not only on dopant diffusion and activation, but also on the extended defects formation in the EOR region induced by Ge-PAI. The dangling bonds at atomically clean surface open a major alternative pathway for enhanced annihilation of excess interstitials during thermal annealing. This results in the change of dopant-defect interactions and EOR defect evolution behavior. The de/re-activation of the dopant is also shown to be strongly influenced by the surface conditions.

For the first time, we have shown that Ge-PAI B doped layer can be improved by surface state manipulation for USJ application, in terms of junction depth, dopant activation and extended defects removal.

Chapter 8

Conclusions and Recommendations for Further Works

8.1 Conclusions

Formation of USJs poses one of the extremely difficult challenges for the fabrication of advanced MOS devices as transistor scaling moves beyond to sub-50nm technology node. Lower sheet resistance, minimal residual defects and smaller junction depths are ever desired. However, the trade-off between anomalous diffusion and activation phenomena which are inherently associated with dopants upon thermal annealing is unavoidable [Lenoble, 2006]. For instance, the most common p-type dopant, B, suffers from TED, B interstitial clustering as well as dopant channeling effects. This pushes the physical limitation of B USJ which conventionally achieved by lowering implant energy or anneal temperature to the end.

One of the most common approaches to continue the B USJ scaling is the combination of PAI and SPER. Generally, inert atoms such as Ge/Si will be implanted prior to the B implant to induce a shallow amorphous layer. Subsequently, it is followed by the typical soak or spike annealing for dopant activation, at which the SPER of the amorphous layer takes place at the same time. This approach has been proven to resolve the issue of B channeling and it also offers the benefits in activation improvement and TED suppression. Although it has been able to sustain

the USJ formation in recent generations of devices, the junction instability and excessive junction leakage as a result of EOR defect formation induced by PAI are foreseen to be problematic. Furthermore, the SCE effect is going to exaggerate as the device scaling is continue, which set the requirements of USJs to become even more stringent and currently under scrutiny for new USJ formation techniques.

The main objective of this thesis is to achieve highly doped and electrical activated USJ through the understanding and maneuvering of the dopant-defect interactions, known as defect engineering. During the course of this work, USJ formation techniques such as C/F/N co-implantation, flash annealing and surface-defect engineering on preamorphized B doped junctions have been extensively investigated with respect to the objective. The following sections summarize and conclude the findings that have been achieved:

8.1.1 The Impact of Nitrogen Co-implant on Boron USJ Formation and Physical Understanding

N co-implant is one of the less established co-doping atoms as compared to the C/F co-implant. Over the years, the effect of N on B diffusion in silicon has been in controversy. On the other hand, N co-implant has not been studied in great details for the application in preamorphized B doped USJs.

Based on the findings from this work, it is found that co-implanting N atoms with projected range located in between B profile and EOR defect distribution can suppress B TED and dopant de-activation phenomenon, as well as possibly affecting EOR defect population. N atoms are believed to react with point defects and dopants, such as V and B atoms, to form the NV clusters and B-N complexes in the SPER

process. The NV clusters can trap the silicon interstitials emitted during the ripening and dissolution of EOR defects, suppressing the unfavorable anomalous B TED and BI clustering. Similarly, it is also found that B-N complex formation could indirect reduce BI interactions, but it restricts the B activation level in the junctions. Therefore, it is necessary to have dominant NV clustering effect over B-N complex formation during the SPER process for the optimum N co-implant effect, which is achievable via optimizing the location of N atom distribution. On the other hand, the defects in EOR region could have also been stabilized since variation in defect density has been observed, but its impact on B diffusion is deduced to be minimal.

In terms of technological application in CMOS devices, R_s and X_j behaviors of the N co-implanted junctions have been evaluated based on spike annealing. The distribution of the implanted N atoms remains a key factor to determine if the fabricated junctions would have superior R_s/X_j junction properties. The Ge-PAI B junction associated with the optimum N co-implant condition is shown to be able to rival the typical Ge-PAI BF_2 junctions with shallower junction depth and slightly lower R_s.

In addition, it has also been shown that the use of N co-implant with B for PMOS S/D extension has great potential in reducing the lateral junction diffusion as well as improving the SCE control in devices. However, the severe reduction in overlap capacitance for the N co-implant split in this study has caused degradation in the I_{on}/I_{off} performances with respect to the reference device. The degradation caused by the excessive overlap capacitance lowering can be fixed via further optimization and fine-tuning of other electrical parameters.

8.1.2 Understanding of Carbon/Fluorine Co-implant Effect on Boron USJ Formation

An extensive study on C/F co-implant in Ge-PAI B/BF_2 junctions upon soak annealing has been performed in comparison to the spike annealing. The desired effect mainly focuses on the B TED and dopant clustering/de-activation characteristics, which are induced by the backflow of silicon interstitials emitted from the EOR region during defect evolution.

The results have clearly shown that the C co-implant is more efficient in trapping the interstitials rather than the F co-implant, resulting in better inhibition of both B TED and dopant de-activation. For instance, C atoms interact with interstitials directly to form carbon-interstitial clusters, C_mI_n, whilst F atoms form F_mV_n clusters before subsequently react with the excess interstitials. The efficiency of the two different co-implant schemes could be possibly correlated to their respective individual interstitial trapping pathway. However, it has also been found that the amount of retained co-implanted atom dose upon annealing could play an important role, at which significantly higher dose retention has been observed for the C atoms as compared to the F atoms when subjected to the same thermal cycle.

On top of F co-implant, the F co-doping via BF_2 has degraded B activation in the junctions though B-F paring during the SPER process. The extent of B-F pairing is believed to be dependent on the overlapping density between initial B and F profiles introduced during the implantation. Nevertheless, B-F pairing has also been observed to have suppressed B TED and de-activation behaviors to a certain degree. The B activation degradation has become more prevalent when the C is co-implanted into the BF_2 junctions, producing the shallowest junctions among the various splits. It

is attributed to the complex interactions of the C and F co-doped atoms with the point defects and dopants during the anneal process.

In terms of R_s/X_j characteristics, the C/F co-implanted B/BF_2 junctions have shown superior advantages than their co-implant free B/BF_2 counterparts when subjected to the spike annealing. A direct comparison among the C, F and N co-implants in Ge + B (with similar relative distribution) reveals that each particular co-implant species has respective distinct advantages on their junction physical and electrical properties.

In a quick summary, the C co-implant is among the most effective co-implant species in improving the R_s/X_j junction behaviors as well as suppressing the B de-activation phenomenon, but it increases the junction current leakage moderately. Both F/N co-implants, which employing the vacancy clusters (FV/NV) interstitial trapping mechanism, reveal a smaller but appreciable improvement in their R_s/X_j characteristics. The N co-implant is less efficient in dopant de-activation suppression, but it offers the lowest junction leakage among the various co-implant splits. The F co-implant has resulted in the largest current leakage, which is approximately ~3x higher than the Ge + B reference junction.

8.1.3 Understanding of Boron Junction in Preamorphized Silicon upon Optimized Flash Lamp Annealing

The direct flash annealing has the advantage of its rapid milli-second temperature ramping-rate, where the instantaneous SPER of the amorphous layer occurs when PAI is coupled, leading to the formation of highly activated junctions

with minimum dopant diffusion. However, it is found that a great amount of residual EOR defects are remaining in the PAI junction that causes the high junction leakage.

The results from this work have demonstrated that EOR defects can be reduced significantly by using multiple-pulse FLA or pre-spike RTA + FLA scheme. The underlying physical mechanisms have been revealed and studied experimentally by post-RTA isochronal annealing, tracing the interactions between dopants and defects. The pre-spike RTA + FLA is shown to have better B de-activation suppression, but the multiple-pulse FLA scheme offers better activation in the preamorphized B doped junction. This is due to the higher dopant activation level achieved by the much faster SPER process in the junction by the direct FLA.

From the diode measurements, the results have shown that high junction leakage for single pulse FLA can be significantly reduced by increasing the number of FLA pulses. For instance, the leakage current has been observed to decrease by up to 1 order when 6 pulses of FLA are performed. Its leakage level is shown to be able to match with the leakage level achieved by the pre-spike RTA + FLA scheme and even associated with superior forward on current attributed to the better dopant activation with 6 pulses of FLA. Therefore, the multiple-pulse FLA scheme has great potential for the application in actual devices.

In the simulations, the stabilities of the different extended defects and their related interstitial supersaturations reproduce the same trend as observed in the experiment between the direct FLA and pre-spike RTA+FLA schemes. The simulated results have also provided important insights on the damage morphology at different steps of the damage evolution during the subsequent post-RTA isochronal annealing.

It has also confirmed and attributed that the better de-activation suppression for pre-spike RTA + FLA scheme is due to the very small interstitial supersaturation upon post-thermal treatment, which is gained from the better EOR defect dissolution during the pre-spike RTA step.

8.1.4 The Effect of Surface State on Boron Doped Pre-amorphization Junction for USJ Application

As the device scaling is continued, the dopants in the junctions are also getting closer to the silicon surface. Pervious works reported that silicon surface is an efficient "sink" for the silicon interstitials in the junctions, but the variation in the state of the silicon surface has not been greatly exploited.

In this work, the chemical state of surface has been demonstrated to have a significant impact not only on B diffusion and activation, but also on the extended defect formation in the EOR region of Ge-PAI junction. This is attributed to the dangling bonds at the atomically clean surface which open a major alternative pathway for enhanced annihilation of excess interstitials during thermal annealing. The excess interstitial supersaturation near the surface is lowered when free silicon dangling bonds are available on the atomically clean state, and hence resulting in a steeper supersaturation gradient from the EOR region towards the surface.

The extra depletion of interstitials in the clean surface has altered the way in which interstitials interacting with dopants due to the stronger interstitial flux, promoting higher dissolution rates of EOR defects during the early stage of SPER. Therefore, the density of EOR defects is reduced on the atomically clean surface samples upon the annealing. The interstitial annihilation at the clean surface will also

decrease the concentration of free silicon interstitials available in junctions, and thus suppressing the interactions between the B and interstitial point defects, which eventually benefiting the B TED and dopant de-activation in the Ge-PAI B doped junctions.

Overall Conclusion

Based on the various findings from this work, the physical understating of the dopant-defect interactions has been improved for the Ge-PAI B junctions associated with new USJ techniques. These results provide some general insights on the possible effects of the new USJ techniques along with some ideas on how to optimize USJs for the application in advanced MOS devices.

8.2 Recommendations for Future Work

Although several new findings and improvements to the existing knowledge base have been achieved on the new USJ formation techniques during the course of this work, there are certainly some areas and details are required to be done in order to acquire further understanding on the advanced USJ optimization. Following sections outline some of the possible avenues that could be followed on from this work:

8.2.1 Co-implantation

Chapter 4 and 5 have presented an extensive studies of the N/C/F co-implant effect on the Ge-PAI B/BF_2 junctions. The investigations focused on improving the USJ properties and to understand the interactions among dopants, defects and co-

implant atoms through a combination of the evidences obtained from doping profile, R_s and Hall measurement data. Although it has been qualitatively observed from XTEM that C/N co-implant offers better defect dissolution (around the EOR region) during the low temperature annealing, the results only provide the qualitatively observations, at which the information on the density and exact configuration was limited. Therefore, it is proposed that high resolution TEM with plan-view mode should be performed. In this case, the impact of co-implant on defect evolution can be further understood and quantitatively correlated to the defect size and density.

On the other hand, the C/N co-implant was also noticed to cause significant degradation in R_s for BF_2 but associated with better B TED inhibition. This is attributed to the complex interactions not only among the dopants, point defects and co-implanted atoms (C/F), but it is possible due to the competing interactions with F atoms which co-doped during the BF_2 implant. Hence, further experimental and modeling works are proposed to be carried out to acquire deeper understanding of the underlying pathways.

In chapter 5, a series of comparisons has been performed on the N/C/F co-implanted Ge + B junctions. Each co-implant species demonstrated their advantages in USJ properties, and also associated with their respective junction current leakage level based on diode measurements. Therefore, it would be interesting if device fabrication can be performed using the identical junction conditions and to study their impacts on device electrical performance. In this way, we could properly identify how the device characteristics would response to a particular set of USJ properties when impurity co-implantation is implemented.

8.2.2 Flash Annealing

The results from chapter 6 revealed that multiple-pulse flash annealing scheme can be used to reduce residual EOR defects which typically remain in the Ge + B junctions after a single pass of flash annealing. The junction leakage from the diode measurements showed that the current leakage level can be brought down to an order lower when single pulse of FLA is increased to 6 pulses. Hence, the multiple-pulse FLA scheme has great potential in offering highly activated B USJs with reduced residual defects for the application in PMOS devices. Trial-run on the device fabrication has been performed during the course of this work; however, it was not successfully done due to the wafer wrapping as a result the thermal stress built-up by 6 pulses FLA on the pattern device wafers. Therefore, further works on re-optimization of multiple-pulse FLA scheme, such as variation in flash pulse number or energy, should be done to find the suitable process windows for the device fabrication.

In addition, the FLA study in this work only involved the Ge + B junctions. It would be interesting to study the impact of advanced flash annealing on the C/N/F co-implanted junctions. The combination of these two USJ techniques could provide additional advantages for the USJ characteristics and its experimental study could also provide some new physical insights.

8.2.3 Surface-Defect Engineering

So far, the surface effect on dopant diffusion and activation has been established for B (in this work) and As dopants only [Vaidyanathan et al., 2006] Thus, it would be of great interest to extend this approach to other dopants, such as P as it

has high electrical solubility in silicon. P is an n-type dopant and exhibits interstitial-mediated diffusion, but inherently coupled with vacancy-mediated clustering mechanism. Therefore, enriching the silicon surface with active dangling bonds in the atomically clean state, could enhance excess interstitials insertion onto the surface. This is an attractive feature to suppress excessive dopant diffusion, which is generally known as the most serious problem for P atoms. In addition, the surface effect on the vacancy clustering mechanism has not been reposted before. Therefore, a general isochronal annealing study would provide new understanding on the interactions of vacancy-dopant clusters with the surface and excess interstitials.

Chapter 9

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Chapter 10

List of Publications

Publications related to this thesis

Journals

1. S. H. Yeong, B. Colombeau, K. R. C. Mok, F. Benistant, C. J. Liu, A. T. S, Wee, G. Dong, L. Chan, and M. P. Srinivasan, *"The Impact of Nitrogen Co-implantation on Boron Ultra-shallow Junction Formation and Underlying Physical Understanding"*, Materials Science and Engineering B: Solid-State Materials for Advanced Technology, v 154-155, n 1-3, p 43-48 (2008).

2. S. H. Yeong, B. Colombeau, K. R. C. Mok, , F. Benistant, C. J. Liu, A. T. S. Wee, L. Chan, A. Ramam, and M. P. Srinivasan, *"Understanding of Carbon/Fluorine Co-implant Effect on Boron-doped Junction Formed during Soak Annealing"*, Journal of the Electrochemical Society, v 155, n 2, p H69-H75 (2008).

3. S. H. Yeong, B. Colombeau, C. H. Poon, K. R. C. Mok, A. See, F. Benistant, D. X. M. Tan, K. L. Pey, C. M. Ng, L. Chan, and M. P. Srinivasan, *"Understanding of Boron Junction Stability in Pre-amorphized Silicon after Optimized Flash Annealing"*, Journal of the Electrochemical Society, v 155, n 7, p H508-12 (2008).

4. K. R. C. Mok , S. H. Yeong, B. Colombeau, F. Benistant, C. H. Poon, L. Chan, and M. P. Srinivasan, *"Experimental and Simulation Study of the Flash Lamp Annealing for Boron Ultra-shallow Junction Formation and its Stability"*, Materials Science and Engineering B: Solid-State Materials for Advanced Technology, v 154-155, n 1-3, p 14-19 (2008).

5. S. H. Yeong, M. P. Srinivasan, B. Colombeau, L. Chan, R. Akkipeddi, Charlotte T. M. Kwok, R. Vaidyanathan, and E. G. Seebauer, *"Defect Engineering by Surface Chemical State in Boron-doped Preamorphized Silicon"*, Applied Physics Letters, v 91, n 10, p 102112 (2007).

6. K. R. C. Mok, B. Colombeau, F. Benistant, R. S. Teo, S. H. Yeong, B. Yang, M. Jaraiz, and S.–F.S. Chui , *"Predictive Simulation of Advanced nano-CMOS Devices based on kMC Process Simulation"*, IEEE Transactions on Electron Devices, v 54, n 9, p 2155 (2007).

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1. S. H. Yeong, B. Colombeau, K. R. C. Mok, F. Benistant, L. Chan, and M. P. Srinivasan, *"Comparison of p+/n Junction Formation with Carbon/Fluorine/Nitrogen (C/F/N) co-implantation and the Underlying Physical Understanding"*, the 17th International Conference on Ion Implantation Technology at Monterey, California (2008).

2. S. H. Yeong, D. X. M. Tan ,B. Colombeau, C. H. Poon, K. R. C. Mok, A. See, F. Benistant., K. L. Pey, C.M. Ng, L. Chan, and M.P. Srinivasan, *"An Extensive Study on the Boron Junctions Formed by Optimized Pre-spike/Multiple-pulse Flash Lamp Annealing Schemes: Junction Formation, Stability and Leakage"*, the 17th International Conference on Ion Implantation Technology at Monterey, California (2008).

3. B. Colombeau, S. H. Yeong, D. X .M. Tan, A. J. Smith, R. M. Gwilliam, C. M. Ng, K. R. C. Mok, F. Benistant, and L. Chan, *"Ultra-Shallow Junction Formation – Physics and Advanced Technology"*, the 17th International Conference on Ion Implantation Technology at Monterey, California (2008). – *Invited Paper*

4. E. Seebauer, C. T. M. Kwok, R. Vaidyanathan, Y. Kondratenko, S. H. Yeong, M. P. Srinivasan, and B. Colombeau, *"Defect Engineering for Ultrashallow Junctions Using Surfaces"*, the 17th International Conference on Ion Implantation Technology at Monterey, California (2008).

5. B. Colombeau, K. R. C. Mok, S. H. Yeong, F. Benistant, M. Jaraiz, and S. Chui, *"Design and Optimization of nanoCMOS Devices using Predictive Atomistic Physics-based Process Modeling",* Extended Abstracts of the Seventh International Workshop on Junction Technology, p 17-22 (2007).

6. E. G. Seebauer, S. H. Yeong, M. P. Srinivasan, C. T. M. Kwok, R. Vaidyanathan, B. Colombeau, and L. Chan, *"Defect Engineering for Ultrashallow Junctions using*

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8. B. Colombeau, K. R. C. Mok, S. H. Yeong, B. Indajang, O. Tan, B. Yang, Y. Li, F . Benistant, M, Jaraiz, N. E. B. Cowern, and S. Chui, *"Design and Optimization of Nano-CMOS Devices using Predictive Atomistic Physics-based Process Modeling",* 2006 International Electron Devices Meeting, Technical Digest, p 381-4 (2006).

Other Publications

Journals

1. J. Smith, R. M. Gwilliam, V. Stolojan, A. P. Knights, P. G. Coleman, A. Kallis, and S. H. Yeong, "Enhancement of Phosphorus Activation in Vacancy Engineered Thin Silicon-on-insulator Substrates", Journal of Applied Physics, v106, n 10, p 103514 (2009).
2. S. H. Yeong, B. Colombeau, K. R. C. Mok, F. Benistant, L. Chan, and M. P. Srinivasan, *"Impact of Boron Halo on Phosphorus Junction Formation and Stability"*, Electrochemical and Solid-State Letters, v 11, n 7, p H179-H181 (2008).
3. D. X. M. Tan, K. L. Pey, K. K. Ong, B. Colombeau, C. M. Ng, S. H. Yeong, A. T. S. Wee, C. J. Liu, and X. C. Wang, *"Vacancy Engineering by Optimized Laser Irradiation in Boron-implanted, Preamorphized Silicon Substrate"*, Applied Physics Letters, v 92, n 20, p 203107-1-3 (2008).
4. M. Kah, A. J. Smith, J. J. Hamilton, J. Sharp, S. H. Yeong, B. Colombeau, R. Gwilliam, R. P. Webb, and K. J. Kirkby, *"Interaction of the End of Range Defect Band with the Upper Buried Oxide Interface for B and BF2 Implants in Si and Silicon on Insulator with and without Preamorphizing Implant"*, Journal of Vacuum

Science and Technology B: Microelectronics and Nanometer Structures, 26, 1, p 347-350 (2008).

Conferences

1. S. H. Yeong, D. X. M. Tan, B. Colombeau, L. Chan, K. L. Pey, J. P. Liu, and M. P. Srinivasan, *"Dopant Diffusion and Activation in SiGe/SiGeC Layers and the Incorporation of High Energy Silicon Co-implantation with RTA and Pulsed Laser Annealing"*, the 17th International Conference on Ion Implantation Technology at Monterey, California (2008).

2. J. Smith, S. H. Yeong, B. Colombeau, B. J. Sealy, and R. M. Gwilliam, *"The Formation of Ultra-Shallow Phosphorous Doped Layers Using Vacancy Engineering"*, the 17th International Conference on Ion Implantation Technology at Monterey, California (2008).

3. J. Smith, L. D. Antwis, S. H. Yeong, A. P. Knights, B. Colombeau, B. J. Sealy, and R. M. Gwilliam, *"Junction Leakage Analysis of Vacancy Engineered Ultra-shallow p-type Layers"*, the 17th International Conference on Ion Implantation Technology at Monterey, California (2008).

4. D. X. M. Tan, K. L. Pey, B. Colombeau, K. K. Ong, C. M. Ng, S. H. Yeong, A. T. S. Wee, and C. J. Liu, *"Advanced Defect Engineering in Pre-Amorphized Si Substrate with Laser Pre-Irradiation Optimization"*, the 17th International Conference on Ion Implantation Technology at Monterey, California (2008).

5. S. H. Yeong, B. Colombeau, F. Benistant, M. P. Srinivasan, C. P. A. Mulcahy, P.S. Lee, and L. Chan, *"Phosphorus Implant for S/D Extension Formation: Diffusion and Activation Study after Spacer and Spike Anneals",* 16th International Conference on Ion Implantation Technology 2006, France , AIP Conf. Proc., 866, 58 (2006).

6. B. Colombeau, S. H. Yeong, S. M. Pandey, F. Benistant, M. Jaraiz, and S. Chui, *"Coupling Advanced Atomistic Process and Device Modeling for Optimizing Future CMOS Devices",* 2006 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA) Proceeding, p 145-6 (2006).