DESIGN AND CHARACTERIZATION OF INTERPOSERS FOR HIGH-SPEED FINE-PITCH WAFER-LEVEL PACKAGED DEVICE TESTING

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To My Family

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Summary

In this thesis, novel designs of two unique interposers for the application of fine-pitch, high-speed wafer-level packaged device testing have been proposed and studied. An interposer is needed for the wafer level test because the fine pitch, high pin count, high density of Inputs/Outputs (I/Os) and vertical compliance requirements have to be accounted for. The interposer serves as the electromechanical interface between the signal generator or test processor and the device under test (DUT). Both of the designs were successfully characterized. One of proposed interposers is a MEMS based interposer using silicon as the substrate and the other is an elastomer interposer. The MEMS based interposer has special MEMS contacts to provide vertical compliance while the elastomer interposer has a special elastomer mesh structure to achieve that.

Both the interposers were designed with careful consideration of the limitations in electrical and mechanical aspects. To obtain better insight and appreciations of these interposers, electrical characterization were performed with the aid of a numerical solver (based on the finite element method). The possibility of optimizing the electrical high frequency response of both was examined and carried out. After detailed characterization had been made, the MEMS-based interposer was found to have limited bandwidth of 1 GHz and an insertion loss of 12 dB at 5 GHz, the target high-speed I/Os of the specifications. Therefore, it is not suited for the required wafer level packaged (WLP)

device test and was therefore not fabricated. In contrast, the characterization of the elastomer-based interposer shows good high frequency response and it meets nearly all the specifications required for the test. Therefore, a prototype of this interposer was fabricated. A functional test of this prototype interposer was successfully carried out. Measurements of the wafer-level packaged device using this interposer are compared to the simulation results. A simulation model for the test is made up of a series of cascaded models representing each components of the test, including the interposer, the wafer level packaging interconnects and the DUT. Each of these models is represented by either their simulated or measured S-parameters or an equivalent circuit. Without taking into the account of the reflections and discontinuities at the interfaces between these components in the overall cascaded test model and with assumption that the references at interfaces are aligned, a good degree of accuracy of the simulated model was achieved compared to the results of the measurements. This interposer shows a bandwidth of 5 GHz. Further parametric variation study of the interposer was attempted. Quantitative and qualitative studies showed that the most crucial part contributing to the signal degradation is the design of the printed circuit board (PCB) part of the interposer. 75 % of the loss of the overall test system is attributed to this board.

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Chapter 1

Introduction

An interposer is required for the electrical high speed testing of fine pitch wafer level packaged devices. It provides a solution to the required fine pitch, high density I/Os, high pin count and vertical compliance specifications of the test. This interposer is to serve as the electromechanical interface between the nano wafer level packaged (NWLP) device chip under test (DUT) and the automated test equipment (ATE). Two interposer designs have been proposed in this research work.

The first interposer is a MEMS-based interposer using silicon as substrate, while the second proposed interposer is an elastomer-based interposer. Mechanical and electrical constraints and limitations need to be taken care of in the design phase. In order to produce reliable electrical test results, signal integrity at high frequencies will be the most important issue to be investigated. The aim is to achieve minimum attenuation along the propagating signal transmission paths. Therefore, good characterization of these interposers are needed in order to accurately predict their high frequency performance.

1.1 Background

In today's cost-effective oriented microelectronics industry, unnecessary packaging cost can be avoided by rejecting defective components at as early stage as possible in a

production cycle. That is why complete direct current (DC), alternating current (AC), functional testing at wafer level are increasingly important.

As the semiconductor technology moves to the submicron regime, the requirements placed on the test probe cards have become increasingly stringent and challenging. Implementation of highly reliable, efficient and cost effective probe cards becomes more and more difficult with the conventional technology available because of the higher pin counts and density per die. The earliest epoxy ring probe card has the limitations of poor control over the interface's electrical environment and fragility. The membrane probe card shown in Figure 1.1 is an attempt to address these problems [21] [22]. It has many advantages over epoxy needle probe card such as lower parasitic inductance, controlled impedance tips, and improved mechanical reliability. However, it also has drawbacks because of the additional force delivery mechanism or air pressure needed to provide sufficient and uniform contacts. It is thermally mismatched and the contacts are also not independently compliant also. The epoxy ring probe cards and membrane probe cards are only capable of probing peripheral I/Os, which potentially limits the probing pin counts per die, and are not feasible for wafer level test which usually has area array pins.

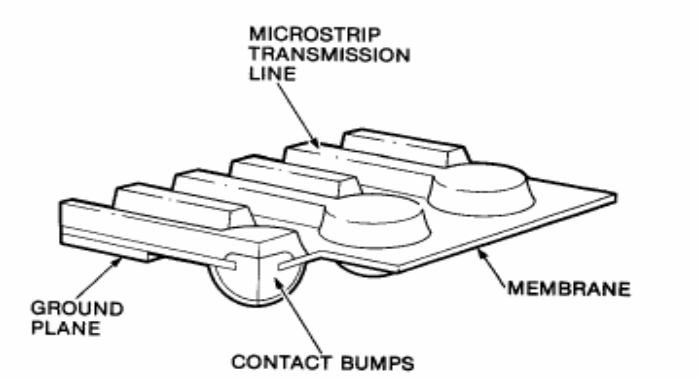


Figure 1.1: Membrane probe, Leslie and Matta, 1988

Various cantilever probe cards have been reported since 1989 [23] [24], but the impedance of the long cantilevered wires is high, resulting in unacceptable low bandwidth. It has difficulties keeping up with new trends in the chip industry. The Formfactor's Microsprings shown in Figure 1.2 successfully address problems of testing many chips in parallel [5], which was not previously achievable by using epoxy or membrane probe cards. It offers significant advantages over the other technologies, which results in low cost and high performance with a 175 μm pitch wafer probing solutions. A simple comparison among these available probing technologies is presented in Table 1.1.

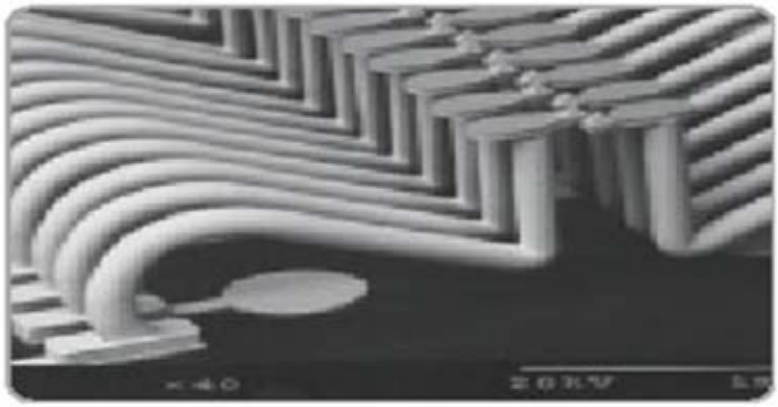


Figure 1.2: Formfactor's Microsprings contacts

Technology	Pitch	Frequency	Pins
Cantilever	L	L	M
Coaxial	M	H	L
MEMS	L	H	M
	L-low	**M-moderate**	**H-high**
pitch	**< 100 μm**	**100 – 1000 μm**	**> 1000 μm**
frequency	**< 2 GHz**	**2 – 5 GHz**	**> 5 GHz**
pin count	**100 - 500**	**500 - 1000**	**> 1000**

Table 1.1: Comparison of different probing technologies

In this research work, the two interposers presented have vertical through wafer and substrate interconnection and are capable of probing area array pins. They are thus applicable to very fine pitch and high frequency tests. Fine pitch wafer level packages are area array packages with extremely high pin density of 10000 pins/cm^2. They are targeted at high-end applications with electrical performance in the range of 5 to 10 GHz. The Wafer Level Packages (WLP) interconnects test is critical due to its mechanical and electrical constraints.

The motivation for developing an interposer to fit the purpose of high pin count and density wafer level test is to reduce the cost for testing. If this interposer is successfully

designed and implemented, it can fulfill the task of a wafer level test, replacing BI sockets, test sockets, handlers and trays with full wafer handling. Its compatibility with the traditional Printed Circuit Board (PCB) processing technology will lead to reduced spending on equipment, floor space, labor and other costs as well.

Another driving force behind this research work is that presently, using existing fine pitch probes, testing at wafer level has strict limitations on number of I/Os that can be tested concurrently. They are not good enough when the test structure is as small as 100um pitch and when the number of I/Os is large and the operating frequency is 5 GHz and beyond. For one of our target test specimens, the test chip of size 20 by 20 mm has 2256 I/Os, depopulated with 3 external rows – pitch 100 μm with three types of interconnects – bed of nails, stretched solder columns or solder balls as shown in Figure 1.3.

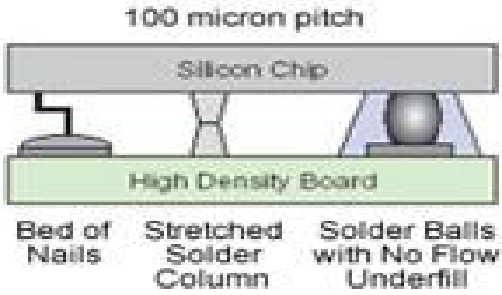


Figure 1.3: Interconnects for wafer level packaged device

The WLP testing involves three major components. First is the electronic circuits that create and detect the high frequency at which the device operates. Second is an interface which links the test circuit hardware to the device under test, which is the interposer. Thirdly we need a manual or an automated mechanism to align the leads of the WLP device under test and the test interposer. Figure 1.4 shows the concept of this kind of WLP test setup.

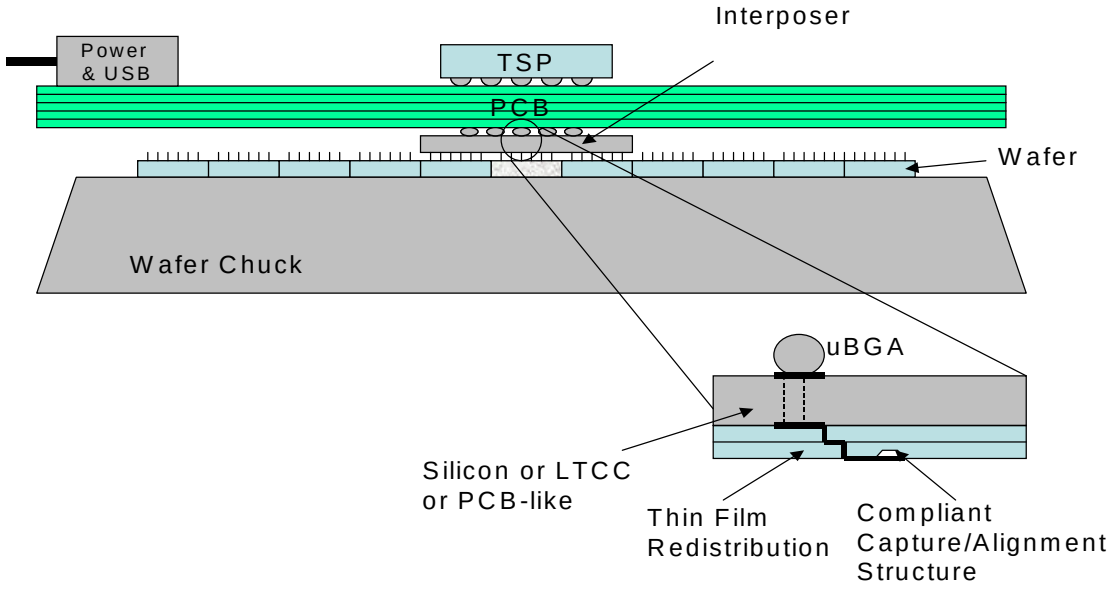


Figure 1.4: WLP test concept

The signal is generated by multiplexing a low frequency clock from an external RF source in a Programmable Gate Array (PGA) chip, designated as Test Support Processor (TSP). It is possible to concurrently perform high speed, fine pitch probing over large pin counts because many TSPs can be placed very close together. By keeping the signal source close to the probe, signal integrity can be preserved. The clock signal is input through the SMA connector. All test control signals are transmitted through the multi-pin connectors to the probe card where multiple TSPs are mounted. The USB and power connector are mounted on the probe card as well. The support logic chips surrounding the TSP will handle the clock distribution, timing generation, data multiplexing and driver/receiver buffering.

The interposer is the main focus of this research work. Having understood the mechanical and electrical constraints that the desired interposer will have, a careful design must be chosen for optimal high speed WLP test performance.

1.2 Project Objectives

The objectives of this research work are to design and characterize feasible interposers meeting the requirements for the application of specific high speed test of the fine pitch wafer level packaged devices with the target of preserving the signal integrity along the transmission path. Subsequently, it is to implement the optimal design of the interposer hardware and integrate it in the WLP test active circuits in order to establish measurements results and demonstrate functional test performance. The measurement results will serve as a good comparison to the simulations results as well.

The test specifications are as follows:

- Insertion Loss: 1-2 dB at 5 GHz
- High Speed I/O: 5 GHz
- High I/O Density: about 1000-10000 pins/cm^2
- Pitch: 100 μm
- Die Size: 20 mm x 20 mm
- Compliance (Vertical Displacement): 5 μm
- Max Temperature: 200 °C

1.3 Outline of Concept

In order to meet the specifications of the test as shown above, geometrical designs of the interposers were done by carefully considering the limitations of available processing technologies. Balancing between cost and effort required by selection of materials were important as well. It often involved a lot of trade-offs between mechanical and electrical

performance. However, meeting the requirements of being capable of probing area array pins and accommodating the DUT were the main concern. Another issue that needed to be addressed in the specifications was the compliancy. For probing area array pins simultaneously, it is important to have a mechanism to provide compliancy between the leads and interconnects of the wafer level packaged device. Therefore, in the two proposed designs, the compliant alignment issue was inherently taken into the consideration when designing the geometries.

Electrical modeling and characterization of the geometries were subsequently performed with the aid of commercial Computer Aided Design (CAD) software. Changes were often made during the simulations to achieve the best electrical performance. The repeated process of re-designing the geometrical properties of the interposer after a characterization exercise was essential to achieving optimal electrical performance. This process was the core research of this work with a lot of signal integrity issues needed to be addressed.

The simulations were done in an Electromagnetic (EM) full-wave solver, Ansoft's High Frequency Structure Simulator (HFSS), implementing Finite Element Method (FEM). The solver is capable of accurately predicting the high frequencies behavior of the 3D models. It has the capability of taking into account of all real-world effects that would have impact on the examined model under conditions prescribed by the user. Reliable simulations results could only be achieved with important information given or specified.

The optimal design was fabricated and underwent a functional test. Measurements results were obtained by using suitable instrumentations and tools. Comparisons between simulations and measurements were made to identify discrepancies in the frequency responses.

1.4 Thesis Layout

The layout of the thesis is as follows:

Chapter 2: A literature search was done to provide an overview of the probe cards technology and techniques. Some popular probing techniques are reviewed. A literature review on the signal integrity issue was also made. Signal integrity problems arising from transmission lines are studied.

Chapter 3: Design and characterization of the proposed MEMS based interposer using silicon as the substrate was done with modeling and simulation in order to optimize the design. Simulations results are analyzed and discussed at the end of the chapter.

Chapter 4: Design, fabrication and characterization of the proposed elastomer based interposer are presented together with detailed methodology on modeling. Simulation results and discussions are also included, followed by measurement results and a comparison to simulations results. Parametric variation study of the interposer is performed for the rest of the chapter.

Chapter 5: The limitations of the proposed interposer designs are discussed. Suggestions for possible improvements and future work conclude the thesis.

1.5 Original Contributions

In this project, the following original contributions have been made:

(i) A MEMS based interposer using silicon as the substrate for high speed fine pitch wafer level packaged devices test was designed. Electrical performance of the interposer was fully characterized. Detailed methodologies of modeling and optimization of signal integrity are presented together with simulations data. Guidelines on future developments of this proposed are also given.

(ii) An elastomer-based interposer for high-speed fine-pitch wafer-level packaged devices testing was designed and fabricated, and its high frequency response was successfully characterized. Modeling and optimization methods were examined and are presented. The fabricated interposer was functionally tested and measurements and simulations results are in good agreement. Future integration with test processors or full wafer testing can be achieved with provided results and insights.

Along the course of this research work, the following papers have been generated:

- Jimmy P.H. Tan, J. Jayabalan, M. Rotaru, M.K. Iyer, B.L. Ooi and M.S. Leong, "Test Bench Modeling and Characterization for Fine Pitch Wafer Level Packaged Devices," Electronics Packaging Technology Conference Proceedings, pp.502-505, December 2004.
- Jimmy P.H. Tan, C. Deng, S. Ang, H.H. Feng, A.A.O. Tay, M. Rotaru and D. Keezer, "A MEMS Based Interposer for Nano Wafer Level Packaging Test," Electronics Packaging Technology Conference Proceedings, pp.405-409, December 2003.

Chapter 2

Literature Review

2.1 Probe Cards Technology

Semiconductors go through many testing processes during their production. One such process is the testing of circuits in chips, which is an extremely important process for ensuring the product performance and quality. This process also makes up a large portion of production cost. Because of losses resulting from packaging faulty circuits, semiconductor circuits are preferably tested while they are in the form of wafers. For testing the circuits, an inspection tool called a ‘probe card’ is used. A probe card has many needles (contact probes) that come into contact with electrodes in a chip. Figure 2.1 shows the basic composition of a semiconductor testing system.

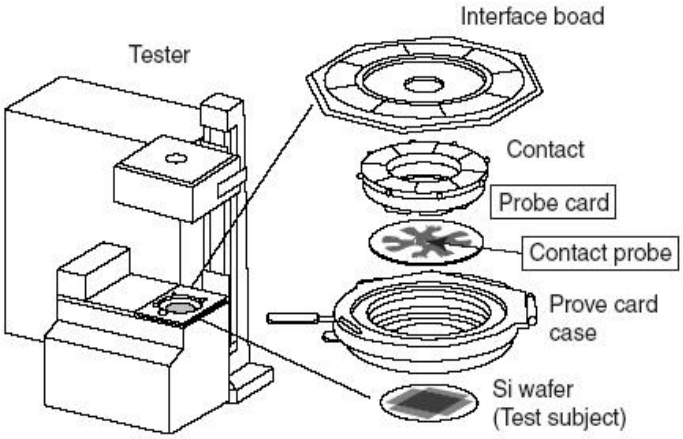


Figure 2.1: Composition of semiconductor test equipment (taken from [14] as reference)

In recent years, as mobile equipment such as cellular phones and PDAs become drastically downsized with higher performance, semiconductor devices are rapidly becoming more integrated. As a result of high integration, the pitches of electrode pads in chips are becoming smaller than 100 μm. In some devices, pad pitches are as small as 40 μm. The electrode pad layout is also becoming denser. In the past, the electrode pads were arranged linearly on the four corners of a chip. Now, the pads are arranged on the entire area of a chip. The operating speed (frequency) of devices often exceeds several hundred of MHz and has reached the GHz level. As a result, contact probes are required to be more minute and of shorter length. However, further miniaturization of contact probes is difficult with conventionally used machining techniques.

In wafer level testing, temporary electrical connections must be made between bond pads on the wafer and external testing circuitry. Traditionally, these connections are made using micro engineered tungsten needles. However, as the dimensions of dies shrink, the limit of this technology is being reached [25]. The international technology roadmap for semiconductors specifies that:

1. Individual probes apply contact forces less than 60 mN [26] to prevent damage to interconnect layers beneath pads.
2. The probe applies less than 40 kg total force to the wafer.
3. Probes provide contact resistances of less than 1 Ω.
4. Probes should require infrequent cleaning (200 - 2000 touchdowns before online cleaning [27]).
5. Probe cards provide electrical and mechanical compliance over a temperature range of -40 to +150 °C
6. Probes have bandwidths of up to 40 GHz for RF devices.
7. Probe cards provide contacts at fine pitches (25 microns or less) whilst maintaining high probe tip planarity (less than 15 microns [26])
8. Probe cards cover a large area (900 – 2000 mm^2) and provide high pin counts (600 – 19000)
9. The costs and times for manufacture and repair of the probe cards should be reduced.

Many different types of probe cards are manufactured, including epoxy, blade, vertical, array, multi-DUT, micro-spring, etc. Currently, the probe card industry is dominated by epoxy ring cantilever needles. There are many small suppliers but few large ones in this highly competitive environment. Emerging new technologies include vertical buckling beam, membrane, conglomerate bump, photolithography defined beams and others. Typical technical requirements can be broken down as follows:

- DC Electrical: Contact resistance, leakage, signal path resistance, probe current capacity, etc.

- AC Electrical: Bandwidth, capacitance, crosstalk, rise times, etc.
- Mechanical: Layout flexibility, alignment, planarity, contact force, pad size, pad pitch, etc.
- Other: Environment (temperature), pad damage, lifetime (number of touchdowns), cost, etc.

Probe card technology should therefore improve to take advantage of the test system improvements and increased performance of the devices. In general, the probe card should maintain the characteristic impedance of the test head, have a rise time faster than either the device or the tester, require little or no maintenance, have a long life cycle (greater than one million touchdowns), and keep pad damage to a minimum.

Packaging costs are increasing with the complexity of IC's. In addition, the high cost of packaging is necessitating AC testing at wafer level. In order to minimize these costs, complete AC, DC and functional testing at wafer level is becoming increasingly important. In today's market, the packaging of a device will cost more than the silicon, on which the device is implemented.

All of these factors (the higher densities, faster speeds and increased performance and elevated packaging costs) escalate the desire to improve probing at the wafer level and eliminate defective die before packaging. In order for this to occur, probe cards must offer enhanced electrical performance, higher densities and better reliability than those currently available.

2.1.1 Considerations for Probe Cards

Figure 2.2 and 2.3 reiterate the requirements for probe cards in term of mechanical and electrical aspects. These parameters are interactive, both in terms of how they are defined by the die to be probed and also with respect to the design details of the probe card. Electrical and mechanical interconnection of the probe card assembly, interface with the prober, and the ATE must be optimized. The probing environment, probe card life, and the maintenance process are also vital considerations.

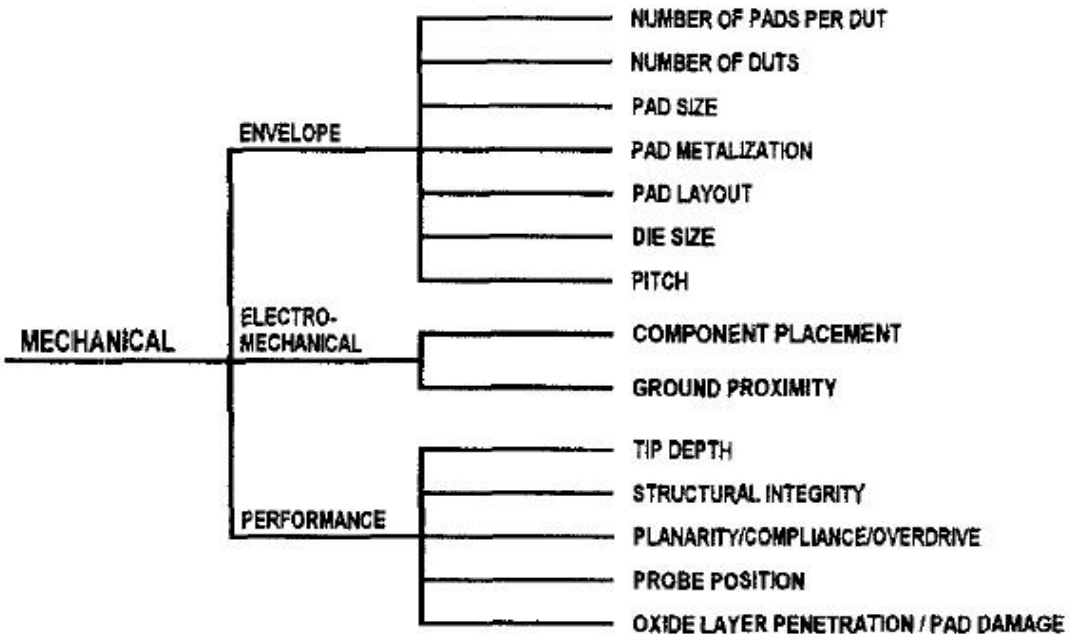


Figure 2.2: Mechanical requirements (taken from [11] as reference)

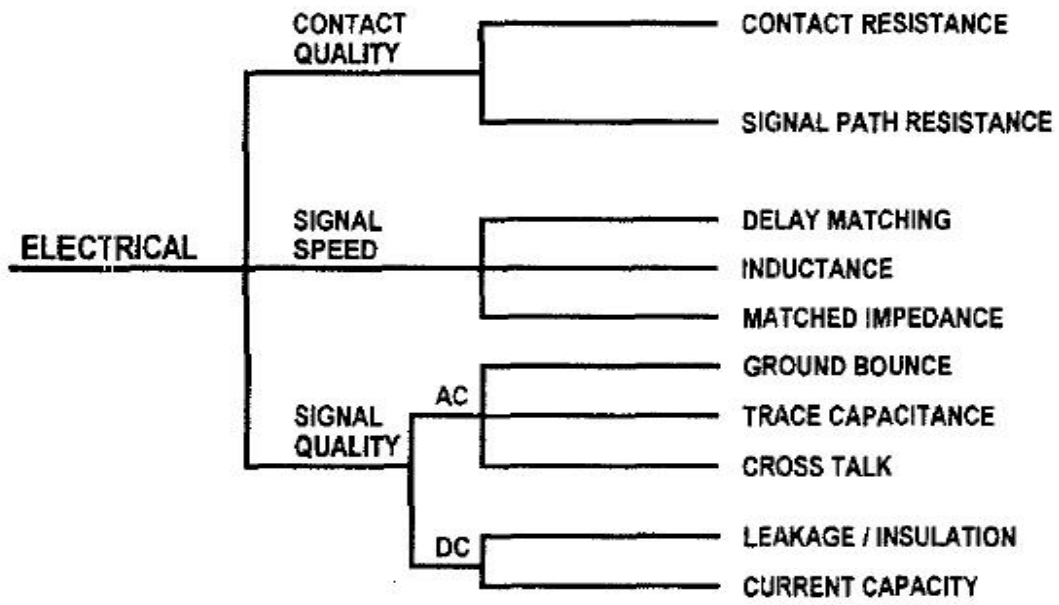


Figure 2.3: Electrical requirements (taken from [11] as reference)

Wafer integrity must be maintained through the probing process. Cost, serviceability, and delivery lead time are also very significant. Lastly, the probe card vendor's final test process and equipment must have proven compatibility with the customer's acceptance process and equipment. This is another vital requirement with increasing probe card sophistication and the availability of more sophisticated probe card analyzer test equipment.

The most common integrated circuit wafer has aluminum pads, which oxidize during fabrication. Aluminum oxide is an insulator. Unless the oxide is penetrated by the probe, good electrical connection is not possible. The ideal is to have no contact resistance between the probe and the wafer. Another type of wafer construction uses solder bumps to create the connection between the integrated circuit and the package. Probing bumps brings a different set of requirements compared to probing aluminum pads. Among other

things, the geometry is larger. Aluminum pads can have pitches that are less than 70 microns, whereas bumps have pitches typically greater than 200 microns. There are two categories of bumps: gold and various alloys of tin and lead. In some of these alloys, lead predominates and in others, eutectic as an example, tin predominates (63 % tin and 37 % lead). These metals require the probe to bump interaction to be optimized to yield effective contact resistance while minimizing pad damage. Reflowing the bumps usually follows probing to return the bumps to an optimum state for their intended packaging. However if no pad damage occurred during probing, then reflow would be unnecessary.

While these considerations address the impact of the probe on the device under test (the semiconductor die), multiple contact of the probe needle to the wafer impacts the probe material itself. In the case of the standard needle probing aluminum pads, the scrubbing action involved in obtaining penetration of the oxide creates the buildup of aluminum on the probe needle. This necessitates cleaning. Most cleaning processes wear the needles through sanding, thereby reducing their life.

To achieve uniform wear of the probe needles as well as uniform force on the die pads, the design of the probe card requires that a balanced contact force (BCF) be achieved by each needle as it scrubs the wafer. BCF is more difficult to obtain for tighter pitch, higher pin count applications. In this case, the ring design requires multiple layers of stacked needles to enable fan-out to prevent needle interaction. Each tier of needles is of different lengths because they are required to reach different distances from the probe card ring to the pads.

This is especially required for multi-DUT probing where the card may have six, or more rows, and each row of needles is of a different length; also the needles will be at different lengths and tapers or etches.

2.1.2 Epoxy Ring & Ceramic Blade Probe Cards

2.1.2.1 Epoxy Ring

The epoxy ring technology is engineered for applications that require high probe densities and high point counts. Probe counts as high as 2000 are not uncommon in some custom multi-DUT probe cards (see Figure 2.4). In the past, blade cards were the primary technology used in parametric testing, due to their relatively low cost and suitability for making low-level measurements. However, as the costs for low pin count epoxy cards have fallen and their leakage performance improved, epoxy cards are now often used in parametric testing. [13]

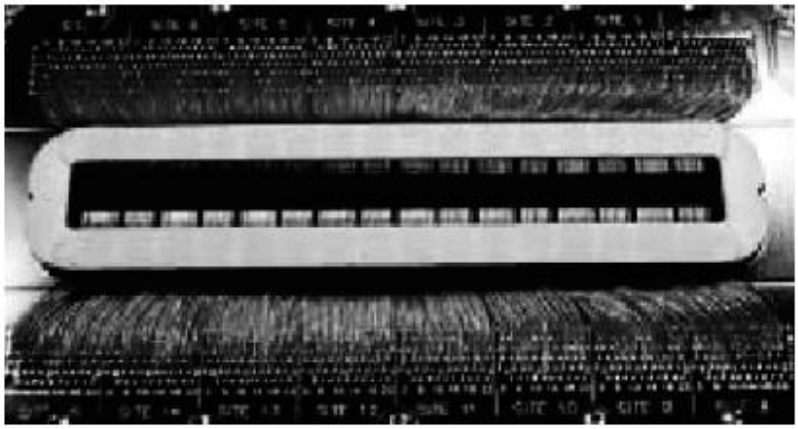


Figure 2.4: Multi-DUT memory probe card
(taken from [13] as reference)

Epoxy ring technology can be extended for low leakage, high frequency, and high temperature applications. The two major components of an epoxy card are the printed

circuit board (PCB) and the epoxy ring assembly. Figure 2.5 is a cross-section of a typical epoxy card PCB with the ring assembly attached.

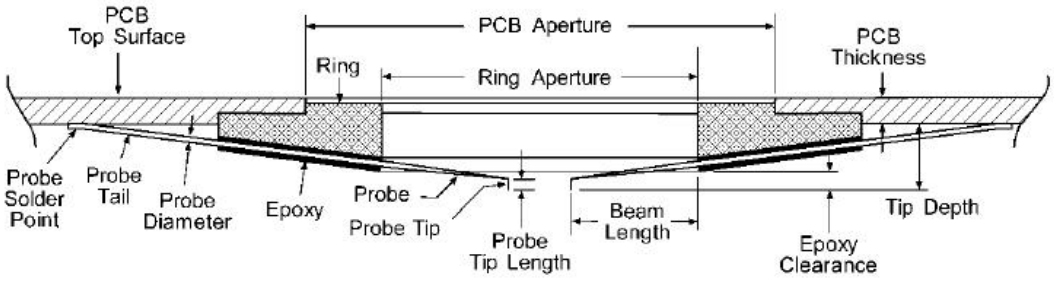


Figure 2.5: Epoxy card with ring assembly
(taken from [13] as reference)

The ring assembly is built by placing preformed probes into a plastic template. Holes corresponding to the pattern of the bond pads of the circuit to be tested are punched into the template. A ceramic or anodized aluminum ring is epoxied to the probes. The ring and epoxy hold the probes in their proper orientation permanently. The signal frequency of the DUT to be tested typically determines whether a ceramic or aluminum ring is used. Aluminum rings are often used in transmission line probe assemblies for high frequency applications (>2 GHz).

After the epoxy has cured, the completed assembly is glued to the PCB, and the probe tails are soldered to appropriate PCB solder points. At this point, user-specified, discrete components—capacitors, resistors, etc.—can be mounted on the PCB. The final steps in making an epoxy card include probe tip shaping, planarity, final alignment, and QA processes.

Probe card design parameters will vary, based on the IC fab's requirements for device size and shape, number of bond pads, signal characteristics, etc. The probe material used will depend on the test signal characteristics, contact resistance requirements, current carrying requirements, and bond pad material. The probe diameter and beam length are determined by the contact force requirements and current carrying requirements. PCB, tip depth, and epoxy clearance depend on the type of prober interface used. PCB, ring aperture size, and ring aperture shape are determined by the number of probes required and the size and shape of the device(s) being tested. The selection of PCB and ring material depends on probing temperature requirements.

2.1.2.2 Blade Cards

Blade card technology is engineered for applications that require low to moderate probe densities and low to moderate point counts (typically fewer than 80 probes). The technology can be extended for low leakage, high frequency, and high temperature applications. Figure 2.6 shows a cross-section of a blade card PCB with blades attached.

Unlike ceramic ring epoxy cards, a blade card has no ring assembly. Each probe is mounted on a separate blade, typically a thin, L-shaped piece of ceramic. These "blade probes" are individually soldered on to lands—special wide metalized patterns—on the top of the PCB.

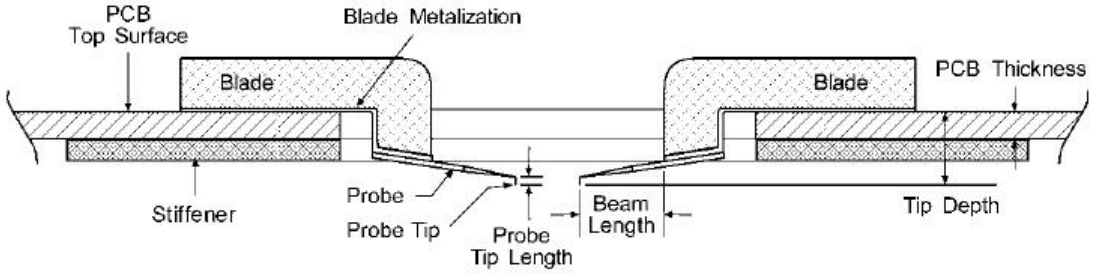


Figure 2.6: Blade probe card with blades attached
(taken from [13] as reference)

The most commonly seen blade card is the low leakage card shown in Figure 2.7. However, as Figure 2.8 illustrates, many different types and styles of ceramic blade cards are available.

Figure 2.7: Low leakage probe card
(taken from [13] as reference)

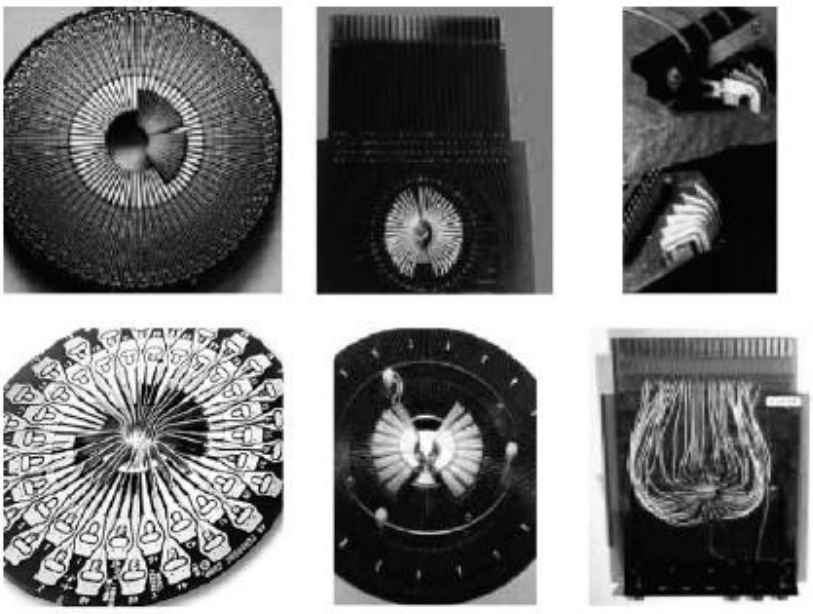


Figure 2.8: Different types of ceramic blade probe cards
(taken from [13] as reference)

The blade card building process starts with preparing the blade probes. Raw blades are metalized along the bottom edge, as shown in Figure 2.6. The probes are cut to the proper length and brazed or soldered—depending on probe material—onto the blades. Finally, the probe tips are bent to the proper angle, making sure that beam length and tip length are in accordance with the specifications.

The assembled blade probes are soldered on to the PCB, along with any user-specified discrete components, such as capacitors, resistors, etc. As with epoxy cards, the final manufacturing steps include probe tip shaping, planarity, final alignment, and quality assurance processes.

Blade card design parameters are similar to those for epoxy cards, with the exception of the blade. There are three main blade types and the most appropriate one for a specific

application will depend on test signal characteristics. A fourth type of blade is used as an edge sensor—this is a special configuration with two probes. Edge sensors are used to detect probe touchdown and help set vertical height, Z. However, due to improved probe technology, edge sensors are no longer as common as they once were. See Figure 2.9.

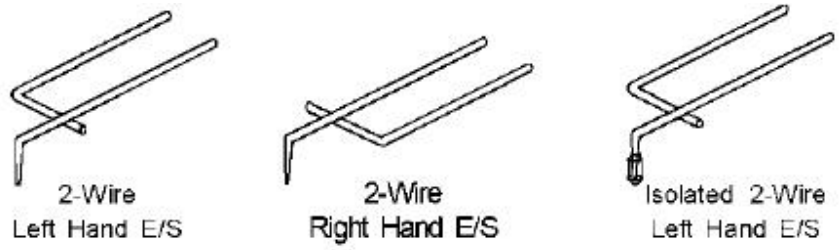


Figure 2.9: Edge sensor configurations
(taken from [13] as reference)

Ceramic blade probes offer superior mechanical stability and a high signal path integrity. With normal usage, ceramic blade probe cards rarely need re-planarization or alignment. The three most common types are the standard blade, microstrip blade, and the radial microstrip blade. See Figure 2.10.

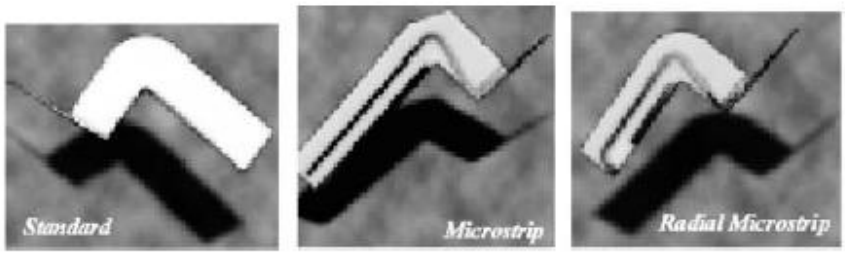


Figure 2.10: Ceramic blade types
(taken from [13] as reference)

Standard ceramic blade probes are used in applications that don't require a controlled impedance environment. Radial microstrip blades are designed for applications that require a controlled impedance environment, where the signal path connects directly to the PCB. Microstrip blade probes are meant for applications that require a controlled impedance environment, where the signal path connects directly to coaxial cable or other

types of transmission line. Microstrip and radial microstrip ceramic blade probes are well suited for high speed probing applications. The controlled impedance environment of probe cards built with these probe styles will support test speeds greater than 3 GHz.

Ceramic blade and the cantilever wire probe characteristics can be manipulated to optimize the performance of the probe for a given application or operating environment. The ceramic blade parameters which have the greatest effect on performance are the blade thickness, shank width, and shank depth. Refer to Figure 2.11. Increasing the thickness of the blade increases stability. Blade thickness is governed by the number of probes in the array and their proximity to each other. Varying the width of the blade shank increases or decreases the surface area where the blade is attached to the probe. This affects the flexibility of the wire probe and the contact force the probe introduces to the wafer bond pads.

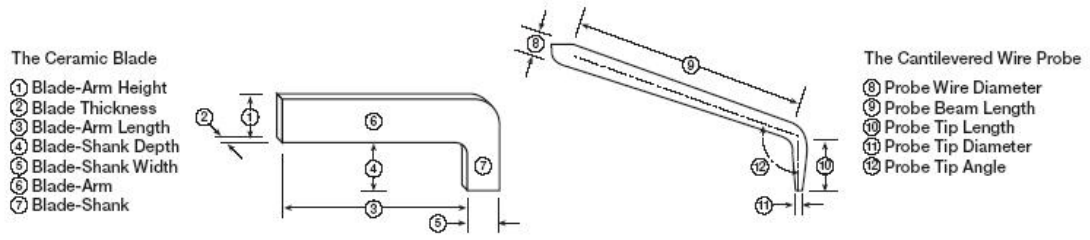


Figure 2.11: Ceramic blade probe geometries
(taken from [13] as reference)

The third variable parameter of the blade is the shank depth. Increasing the depth of the shank increases the distance between the probe card PCB and the wafer under test, which is especially important when testing in a hot chuck environment.

The cantilevered wire probe variations include differences in materials and physical characteristics. Wire diameter, beam length, and material are the primary factors influencing probe contact force and, consequently, scrub length. The probe wire diameter is directly proportional to the contact force. Beam length also influences the contact force, but the relationship is inversely proportional, so that increasing the beam length decreases contact force. The probe tip length and tip angle have a direct effect on scrub length. Longer probe tips are also used on high density probe cards, alternating with standard length tips to ensure proper clearance and signal isolation. The final parameter, probe tip diameter, must be selected to provide good contact force, yet ensure the entire scrub length fits well within the passivation opening.

2.1.2.3 Epoxy Ring Vs Ceramic Blade

Table 2.1 shows the comparison of the epoxy ring probe card technology to the ceramic blade probe card technology. The decision of which probe card technology to use will depend on the type of application.

	Epoxy Ring	Ceramic Blade
Multi-DUT	Very good	N/A
AC Electrical		
Bandwidth > 2 GHz	Needs work	Very good
Crosstalk	PCB layout dependent	PCB layout dependent
DC Electrical		
Inductance < 5 nH	Needs work	Good
Leakage	OK	Very good
Signal Path Resistance	PCB layout dependent	PCB layout dependent
Mechanical		
Planarity Compliance	Very good	Very good
Alignment Compliance	Very good	Very good
Min. Pad Pitch	50 mm	100 mm
Probe Density	> 2000 probes	< 88 probes
Scrub Aluminum Pad	Good	Good
Contact Force	Good	Good
Other		
Temperature	OK, requires custom > 100 °C	Best
Touchdowns > 250k	Very good	Good
Customer Repairability	OK	Better
Cost of Ownership	Good	Slightly better
Addition of Passives	OK	Very good

Table 2.1: Epoxy vs. blade comparison

2.1.3 Micro-spring Probe Card

FormFactor is the developer of the micro-spring probe card. MicroSpring^{TM} contact was introduced in 1995 [5]. The newest development was focused on the MicroSpringsII contact. Table 2.2 shows the comparison of these two contacts in term of general probe card requirements. Figure 2.12 shows what these two technologies have in common and what have been changed in the newest MicroSpringsII. [15]

	MicroSpring Contact	MicoSpringsII Contact
Fine Pitch Capability - down to 60 μm and below	No	Yes
Layout Flexibility - LOC, peripheral pads, staggered peripheral	No	Yes
Low TCOO - improved yield, low maintenance	Yes	Yes
Scalable for Multi-DUT Array Capability - 64 DUT memory and beyond, > 4 DUT logic	Yes	Yes
Low Probe Force - mean spring force < 1.5 gm/mil	Yes	Yes

Table 2.2: Comparison of two different micro-spring contacts

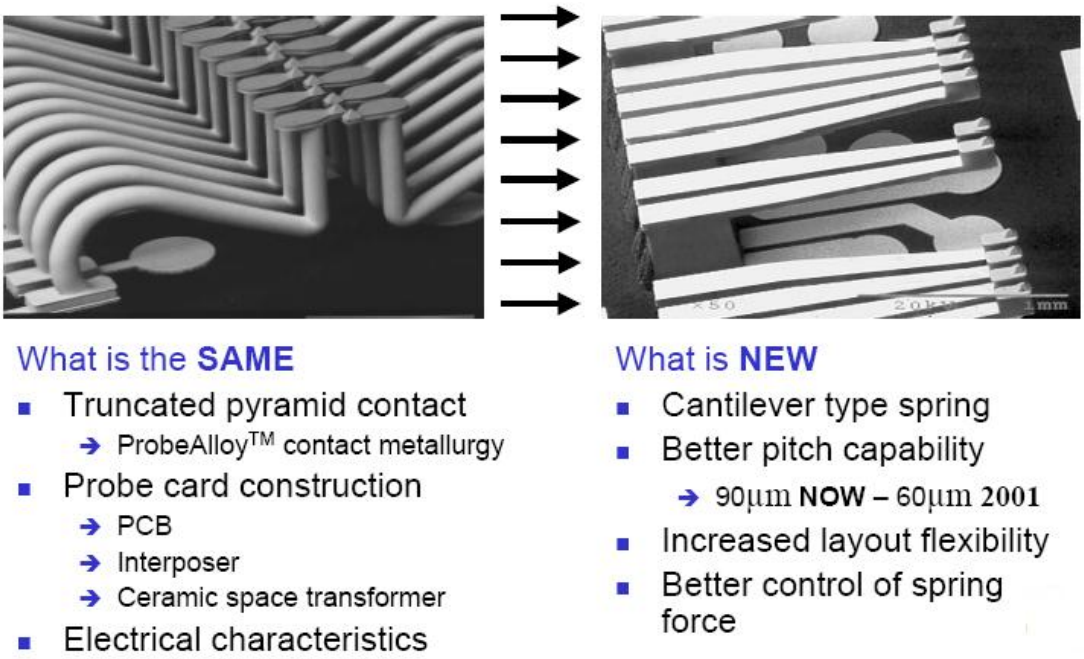


Figure 2.12: The changes on the new MicroSpringsII
(taken from [15] as reference)

As can be seen in Figure 2.12, the MicoSpringsII has the proven technology of the ProbeAlloy™ contact which is the truncated pyramid metal contact used in the MicroSpring™. It retains the advantages like low contact resistance, minimal cleaning required and long lifetime. During internal characterization, millions of touchdowns tests were performed. It is now available for fine pitch probing, parallel memory and logic test.

2.1.4 LIGA processed Micro Contact Probe

The Sumitomo Electric Industries, Ltd. (SEI) has studied the use of a high-precision micromachining technique called the LIGA process [14]. The LIGA process is a micromachining technique that uses synchrotron radiation (SR) X-ray lithography and plating (electroforming). Lithographic micromachining technology, which is the basis of LIGA process, allows mass-production of contact probes with only one radiation and enables production of plungers, springs, and supporting members all at once. SEI has also

developed a new electroforming material that can withstand the burn-in test and applied it to contact probes [1], [2].

2.1.4.1 Contact Probe Requirements

In order to absorb variations in the heights of test pieces (wafers and probe cards) caused by warping and bending and to generate contact loads, contact probes must have mechanical spring properties. Moreover, the probe material needs to have resistance against heat because probes must undergo measurements at a temperature of either 70 or 150 degrees C during the testing process. In addition, the probe material must satisfy the requirements shown in Table 2.3 so that the probes can be used for smaller pad pitches, area array layout, and high frequencies. As shown in Figure 2.13, conventional contact probe uses a coil spring and has a contacting projection (plunger) on its tip. Due to limitations of coil winding techniques and machining precision, the fabrication of contact probes less than 100 μm in outer diameter is extremely difficult. It is therefore difficult to apply the contact probes of conventional structures to the area array electrode layout of pitches less than 100 μm. Also, since the conventional contact probe structure is a made up of more than one parts, it is difficult to make its total length short. It can consequently only be applied to a limited range of high frequencies. In order to satisfy the required contact probe specifications shown in Table 2.3, a micro contact probe shown in Figure 2.14 was tested and developed.

Cross-section (width)	80 μm × 80 μm or less
Probe length	3 mm or less (2 nH @ 1 GHz)
Stroke	50 μm or less
Force (Load)	50 ~ 100 mN(Variation of force: ±20% or less)

Table 2.3: Requirements for micro contact probe

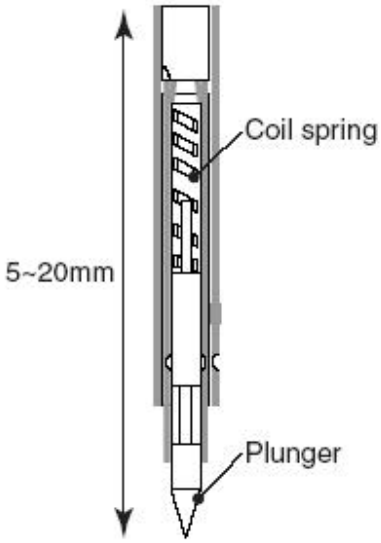


Figure 2.13: Structure of conventional contact probe

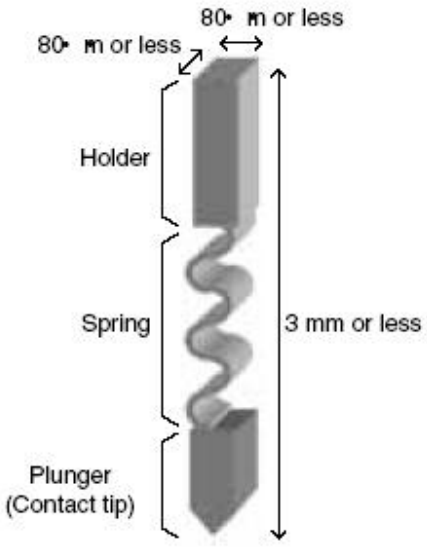


Figure 2.14: Basic structure of a micro contact probe

(taken from [14] as reference)

2.1.4.2 Fabrication Process

Figure 2.15 shows the micro contact probe fabrication method using LIGA process. The LIGA process makes use of X-ray's high permeability. It is possible to expose thick resist (maximum 1 mm in thickness) and fabricate thick mechanical structure. Moreover, because this process uses X-ray lithography, almost no diffraction of light occurs and therefore it is possible to transfer the mask pattern with high accuracy, allowing the fabrication of a mechanical structure with submicron-level accuracy. Other advantages of

the LIGA process include extremely high perpendicularity of side wall and surface smoothness (surface roughness Ra = 30 nm).

The mask pattern that determines the accuracy of the fabricated structure achieved ±0.3-0.4 μm (3 σ) dimensional accuracy in the entire mask area. After image development, the contact probe is fabricated by electroforming, using a substrate as the seed layer. Because electroforming may generate slight unevenness of thickness, uniformity in contact probe thickness is achieved by abrasion. The fabricated contact probe achieved dimensional accuracy of <±1 μm in plane and ±2 μm in thickness. The contact probe is then removed from the substrate.

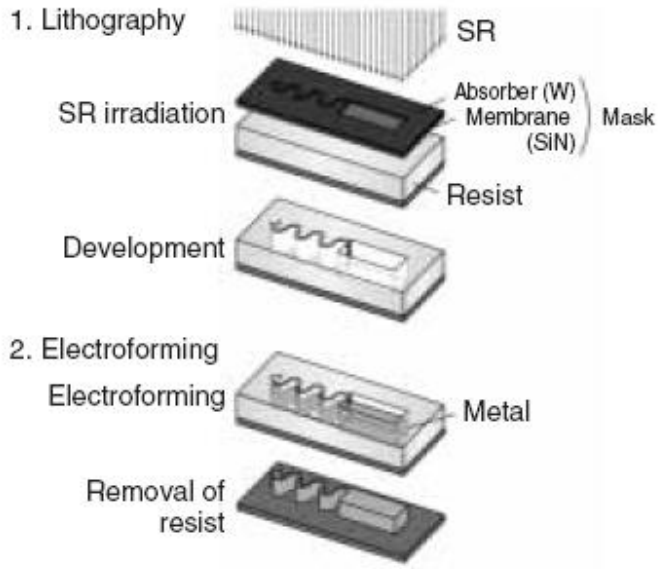


Figure 2.15: LIGA process
(taken from [14] as reference)

2.2 Signal Integrity

Testing semiconductors involves passing test signals from a tester through a distributed system of transmission lines (the test interface) to the device under test, a lumped-circuit

device (chip). For most electronic components, signal-integrity effects becomes significant at clock frequencies above about 100 MHz or rise times shorter than about 1 ns. This is called the high-frequency or high-speed regime. These terms refer to systems where the interconnects (for this case of semiconductors test, refer to the test interface) are no longer transparent to the signal and can seriously affect the electrical performance of the system if not properly taken account of. In this research work, a custom-made test interface, the interposer, will be designed and its high speed signal integrity closely examined.

Signal integrity refers, in its broadest sense, to all the problems that arise in high-speed products due to the interconnects. It is about how the electrical properties of the interconnects, interacting with the digital signal's voltage and current waveforms, can affect performance. Though signal integrity problems generally fall into three categories-- timing, noise and electromagnetic interference (EMI)-- most of the time, we are concerned about the noise issue. Reflections, ringing, cross talk, switching noise, ground bounce are all associated with noise. All of the signal integrity noise problems are related to the following four unique families of noise sources:

a. Signal quality of one net
b. Cross talk between two or more nets
c. Rail collapse in the power and ground distribution
d. EMI and radiation from the entire system

Table 2.4 gives the general guidelines in dealing with these four families of noise problems.

Noise Category	Design Principle
Signal Quality	Signals should see the same impedance through all interconnects
Cross Talk	Keep spacing of traces greater than a minimum value, minimize mutual inductance with non-ideal returns
Rail Collapse	Minimize the impedance of power/ground path and the delta I
EMI	Minimize bandwidth, minimize ground impedance, and shield

Table 2.4: General guidelines to minimize signal integrity problems

In this research work, as far as the proposed interposers are concerned, the most important signal integrity issue is the reflections. The cross talk is minimal, switching noise and other noise problems are not that critical.

The electrical description of every interconnect is based on three ideal lumped circuit elements (resistors, capacitors, and inductors) and one distributed element (a transmission line). The electrical properties of the interconnects are all due to the precise layout of the conductors and dielectrics and how they interact with the electric and magnetic fields of signals. Understanding the connection between geometry and electrical properties will give us insight into how signals are affected by the physical design of interconnects. The key to optimizing the physical design of a system for good signal integrity is to be able to accurately predict the electrical performance from the physical design and to efficiently optimize the physical design for a target electrical performance.

All the electrical properties of interconnects can be completely described by the application of Maxwell's Equations. These four equations describe how electric and magnetic fields interact with the boundaries (conductors and dielectrics) in some

geometry. Therefore, a numerical solver with capability of solving Maxwell's Equations is often used for characterization purpose.

2.2.1 Transmission Lines

In this research work on nano wafer level test (NWLP), most of the parts of the proposed interposers can be modeled as transmission lines. Knowledge of electrical properties of transmission lines is thus of critical importance in dealing with signal integrity problems of interposers. Fundamentally, a transmission line is composed of any two conductors that have length. A transmission line is used to transport a signal from one point to another. To distinguish the two conductors, one is referred to as the signal path and the other as the return path. A transmission line has two very important properties: a characteristic impedance and a time delay. Though in some cases electrical properties of an ideal transmission line can be approximated with combinations of inductors (L) and capacitors (C), the behavior of an ideal transmission line matches the actual, measured behavior of real interconnects much better and to much higher bandwidth than does an LC approximation. [28]

2.2.1.1 Return Path and Switching Reference Planes

Return path of a transmission line has to be design with as much care as the signal path to avoid undesirable noise problems. It is because it is preferable to have controlled impedance along the signal transmission path to avoid reflections. If the return path and signal path present a constant impedance that the signal "sees" while propagating, controlled impedance can be achieved.

In planar interconnects found in circuit boards, the return paths are usually designed as planes, as in multilayer boards. For a microstrip, there is one plane directly underneath the signal path and the return current is easy to identify. However, if there are additional planes in between the signal and return paths, switching reference planes can occur, which will introduce reflections. One important thing to note is that current will always distribute so as to minimize the impedance of the signal-return loop. Therefore, it has been showed that the impedance of a transmission line in a multilayer board will be dominated by the impedance between the signal line and the most adjacent planes, independent of which plane is actually connected to the driver's return path. To minimize the impedance between adjacent planes, a dielectric between the planes as thin as possible is used.

2.2.1.2 Reflections

If a signal is traveling down an interconnect and the instantaneous impedance the signal encounters a step changes, some of the signal will be reflected and some of the signal will continue down the line distorted. This principle is the driving force that creates most signal-quality problems on a single net. These reflections and distortions give rise to a degradation in signal quality. It looks like ringing in some cases. The undershoot, when the signal level drops, can make false triggering.

Reflections occur whenever the instantaneous impedance the signal sees changes. It can be at the ends of lines or wherever the topology of the line changes, such as at corners, vias, tees, connectors, and packages. By understanding the origin of these reflections and armed with tools to predict their magnitude, a design with acceptable system performance

can be engineered. For optimal signal quality, the goal in interconnect design is to keep the instantaneous impedance as constant as possible. First, this can be done by keeping the characteristic impedance of the line constant. Hence the growing importance of manufacturing controlled impedance boards. Minimizing stub lengths, using daisy chains rather than branches, and using point-to-point topology, are all methods to keep the instantaneous impedance constant. This can also be done by managing impedance changes with topology design and adding discrete resistors to maintain a constant instantaneous impedance for the signal.

2.2.1.3 Losses in Transmission Lines

There are five ways energy can be lost while the signal is propagating down a transmission line:

1. Radiative losses
2. Coupling to adjacent traces
3. Impedance missmatches
4. Conductor losses
5. Dielectric losses

While radiative loss is important when it comes to EMI, the amount of energy typically lost to radiation is very small compared to the other loss processes, and this loss mechanism will have no impact on lossy lines.

Coupling to adjacent traces (crosstalk) is important and can cause rise-time degradation. It involves the unwanted transfer of a signal from one net to an adjacent net and will occur between every pair of nets. Cross talk is related to the capacitive and inductive

coupling between two or more signal and return loops. It can often be large enough to cause problems. Minimum cross talk is achieved with a wide plane for the return path. In this case, the capacitive coupling is comparable to the inductive coupling and both terms must be taken into account. Cross talk is primarily due to the coupling from fringe fields. The most important way of decreasing cross talk is to space the signal paths further apart.

Impedance missmatches or discontinuities can cause reflections of the signal. The final two loss mechanisms represent the primary causes of attenuation in transmission lines. Conductor loss refers to energy lost in the conductors in both the signal and return paths. This is ultimately due to the series resistance of the conductors. The series resistance a signal sees in propagating along the signal and return paths is related to the conductors' bulk resistivity and the cross section through which the current propagates. At higher frequencies, the current will be using a thinner section of the conductor and the resistance will increase with frequency. This phenomenon is called "skin effect". Skin depth is driven by the need for the currents to take the path of the lowest impedance, which is dominated by the loop inductance at higher frequencies. This mechanism also causes the current in the return path to redistribute and change with frequency. At DC, the return current will be distributed all throughout the return plane. When in the skin-depth-limited regime, the current distribution in the return path will concentrate close to the signal path, near the surface, so as to minimize the loop inductance. Therefore, in short, the series resistance of the conductors in a transmission line will increase with increasing frequency.

Dielectric loss refers to energy lost in the dielectric due to a specific material property—the dissipation factor of the material. At high frequency, the dielectric losses are greater than the conductor losses and dominate. This is why the dissipation factor of the laminate materials is such an important property. Any two conductors can make up a capacitor. The current through an ideal capacitor, when filled with an ideal lossless dielectric, will be increased by a factor equal to the dielectric constant. All of the current will be exactly 90 degrees out of phase with the voltage, no power will be dissipated in the material, there is no dielectric loss. However, real dielectric materials have some resistivity associated with them. When a real dielectric is placed between the plates of a capacitor with a DC voltage across it, some DC current will flow. This is usually referred to as leakage current. It can be modeled as an ideal resistor. The leakage current is in phase with the voltage. This current will dissipate power in the material and contribute to loss.

2.3 Modeling Techniques

Modeling techniques used for electrical characterization can be done either in time or frequency domain. A 3D geometrical model or circuit model can be created to serve as accurate prediction of the response of the structure, circuit or device of interest. Most of the time, computer numerical solvers are used to analyze the created model. Depending on what kind of solver is used, different solution methods are implemented. Finite element method (FEM), method of moment (MOM) [30] and Finite Difference Time Domain (FDTD) [31] analysis are the most popular solving tools. Time domain or frequency domain analysis can be chosen as well to provide different perspectives. FEM and FDTD are methods based on solutions of Maxwell's equations in their differential form while MOM is solving the integral form. In general, FEM and FDTD

are highly efficient in solving complex geometries in inhomogeneous media, but not effective for solving open-region problems. MOM, on the other hand, is good for solving open radiation problems and planar layered structures, but faces problems when dealing with complex geometries and inhomogeneous media. Hence, FEM is often used to solve EM structures like waveguide, transmission line and cavities. In this research work, solver based on FEM method was used.[9]

High frequency simulation involves electromagnetic field and wave calculations in which the Maxwell equations are solved. In term of high frequency response, scattering parameters (S-parameters) serve as very good benchmark indicators to show insertion (transmission) loss and return (reflection) loss.

In this research work, high frequency S-parameter simulations were performed in frequency domain. The numerical solver used was Ansoft's High Frequency Structure Simulator (HFSS), which uses FEM to solve the full-wave 3D geometrical models.

Chapter 3

MEMS based Interposer using Silicon as Substrate

This chapter presents the design and characterization of a MEMS based interposer. The geometry of the interposer is described first. The interposer was designed to perform the test and burn-in task in wafer level packaged device as described in Chapter 1. It is created to meet the target specifications of the test. Fine pitch MEMS contact tips were built on one side of the interposer to provide compliance when they are connected to the DUT. Next, the electrical characterization of the interposer was carried out and examined carefully. The most crucial design part will be looked into and optimized after that.

3.1 Introduction

A MEMS based interposer using silicon as the substrate was designed. This interposer is similar to a conventional probe card, except for having vertically connected signal traces. It is designed to meet the requirement of fanning out the 100 μm pitch inputs/outputs (I/Os) to about 750 μm pitch pads, which are compatible with the traditional printed circuit board (PCB) processing technology. With self-aligned, z-axis compliant and good electrical contact features, the interposer serves as the electrical and mechanical interface between the device under test (DUT), and the test signal processor (TSP, the generator/receiver of the high speed signals). Due to the large number of I/Os on the nano

wafer level packaged (NWLP) devices (in the order of 10,000 to 200,000 I/Os per cm^2), it is anticipated that the interposer will need to have multi layers of metal and dielectric to fulfill the redistribution task. The developed interposer has three metal layers on top of the silicon substrate to serve as power plane, ground plane and signal trace layer, respectively. The overall test system schematic drawing can be seen in Figure 3.1. The top view of the proposed MEMS based interposer is shown in Figure 3.2. The dimension of the board is 25 mm by 25 mm. Its cross-section drawing is shown in Figure 3.3 with top part facing down. One side of the interposer has large pitch metal bump pads (750 μm pitch) for connection to the tester while another side has the fine pitch compliant structures (100 μm pitch) to make contact with the I/O pins on the NWLP wafers. When connected, the interposer will be mechanically aligned to the pads of the NWLP and to provide a temporary pressure contact for each electrical signal, including power and ground pins. Figure 3.4 shows the enlarged view of the layout of the compliant structure of the proposed interposer on the 100 μm pitch side.

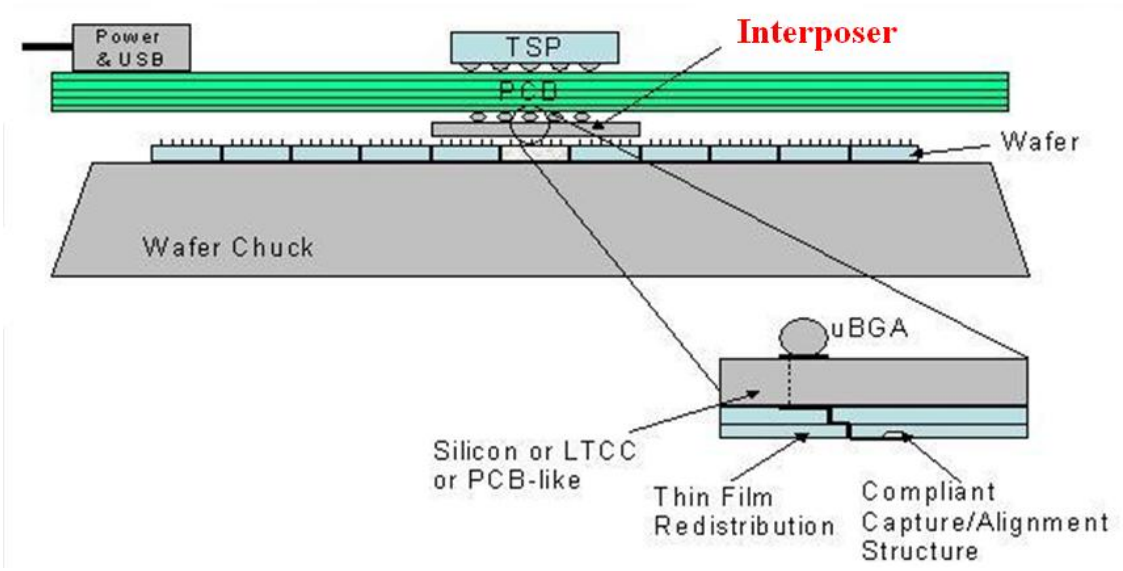


Figure 3.1: Interposer for NWLP DUT test

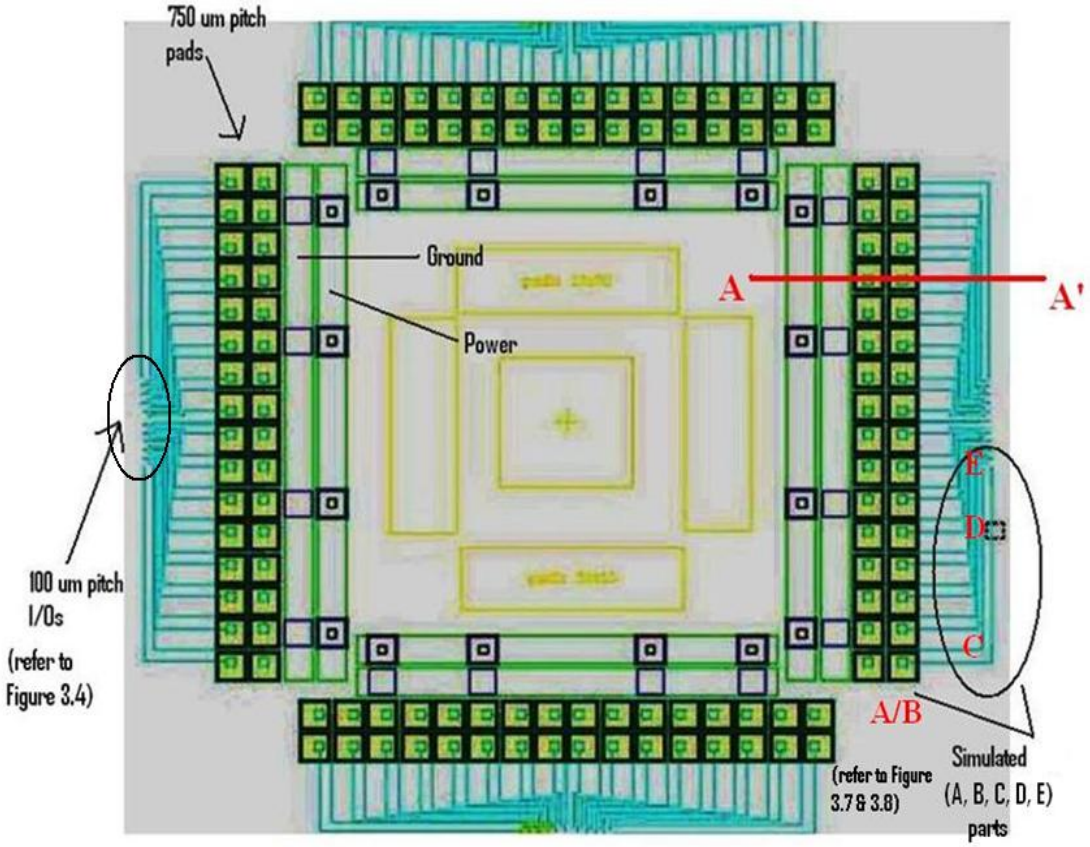


Figure 3.2: Top view of the proposed MEMS based interposer (25 mm X 25 mm)

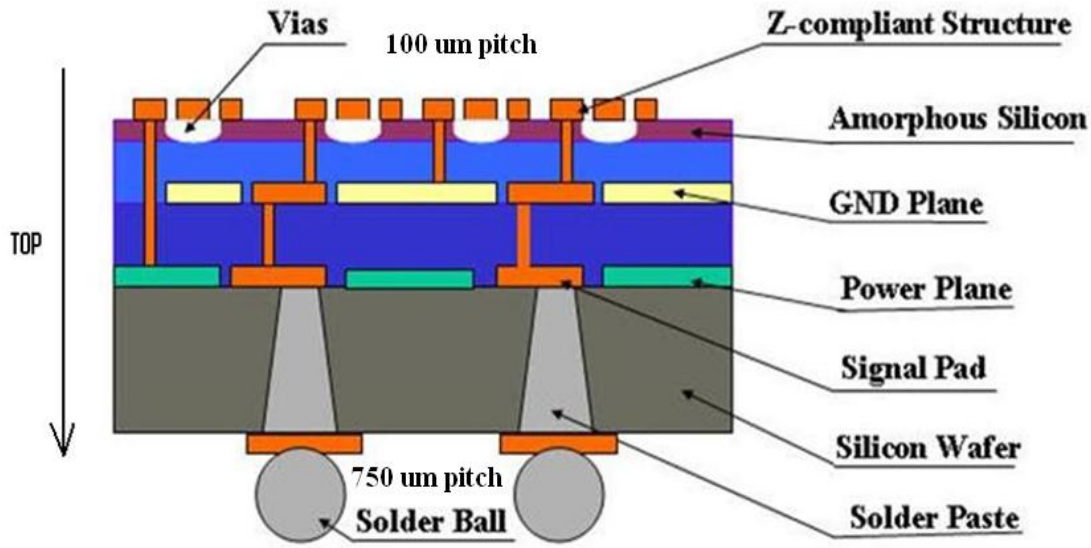


Figure 3.3: Cross sectional view (section AA' in Figure 3.2) of the proposed MEMS based interposer (top 750 μm pitch side facing down)

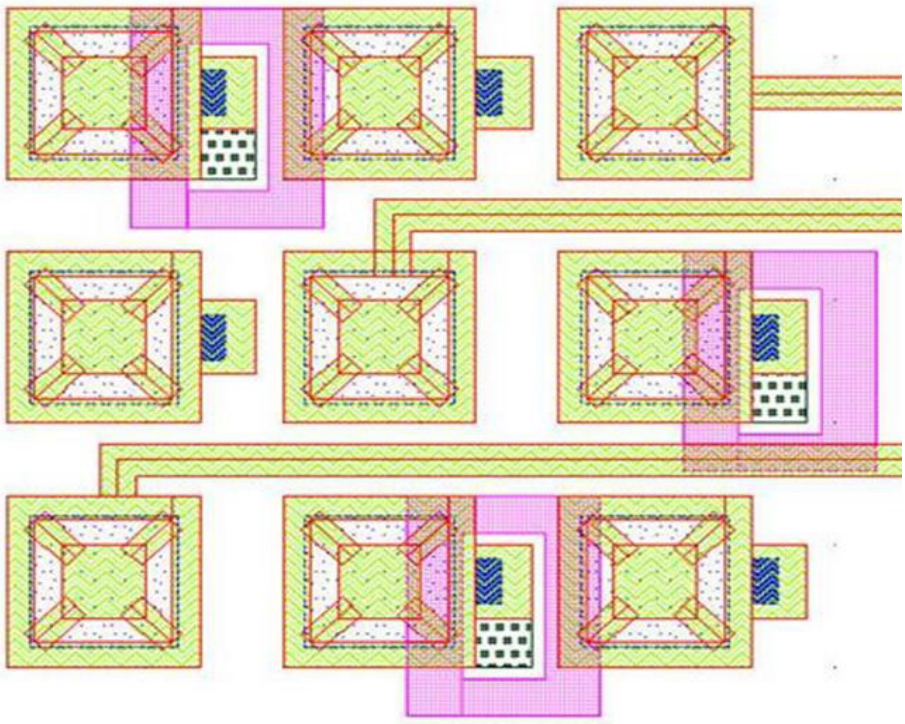


Figure 3.4: Enlarged view of the layout of the compliant structure of the proposed MEMS based interposer (100 μm pitch side in Figure 3.2)

The interposer was fabricated on a high resistivity silicon wafer substrate using semiconductor and micro-machining processes. The design of the interposer uses silicon as the substrate due to the availability of foundry resources and due to the ability to fabricate small features with the silicon process (50 um via diameters, 100 um pitch, etc). The interposer is CTE matched to that of the silicon wafer and is mounted to a conventional multilayer PCB, which further distributes the signals to pins or connectors that mate the test support processor (TSP). With the repeat of the TSP on a two-dimensional array, parallel test tasks can be completed simultaneously. It will dramatically increase the test throughput and reduce the test cost. A preliminary test vehicle Interposer with 180 I/Os was designed and fabricated.

3.2 Modeling and Simulation

In order to characterize the proposed MEMS-based interposer, an electromagnetic (EM) 3D model was created to capture the important features of the interposer. A commercial full wave solver implementing based on the finite element method (FEM). As shown in the bottom-right corner in Figure 3.2, the longest transmission path connecting the 750 μm pitch pad to the 100 μm pitch contact have been chosen to be modeled. The S-parameter simulations were performed in the frequency domain with a frequency sweep from 100 MHz to 10 GHz. Two-port simulations were setup, in which self calculated impedance waveport was excited on the 750 μm pitch pad and lumped point source port (port impedance was specified to be 50 Ω) was created on the 100 μm pitch contact. Boundary condition was made as a radiation box closely covering the model right on the edges of models.

The longest transmission path was chosen to provide the worst case response that could be found for this interposer. As described in Chapter 2, the designed interposers would mostly only have signal integrity issue in term of reflections, conductor and dielectric losses and longer the signal transmission path, the greater losses would be encountered in term of these loss mechanisms.

In addition, the interposer structure geometry and the material selections are optimized through this electrical modeling. The electrical performance improvement is obtained through a combination of low loss materials (BCB, SiO2) in between the build-up layers. The build-up layers have signal transmission through coplanar waveguide structure on the top layer and stripline geometry on the intermediate layers between the power and ground planes. The build-up layers can be seen in cross sectional view in Figure 3.5.

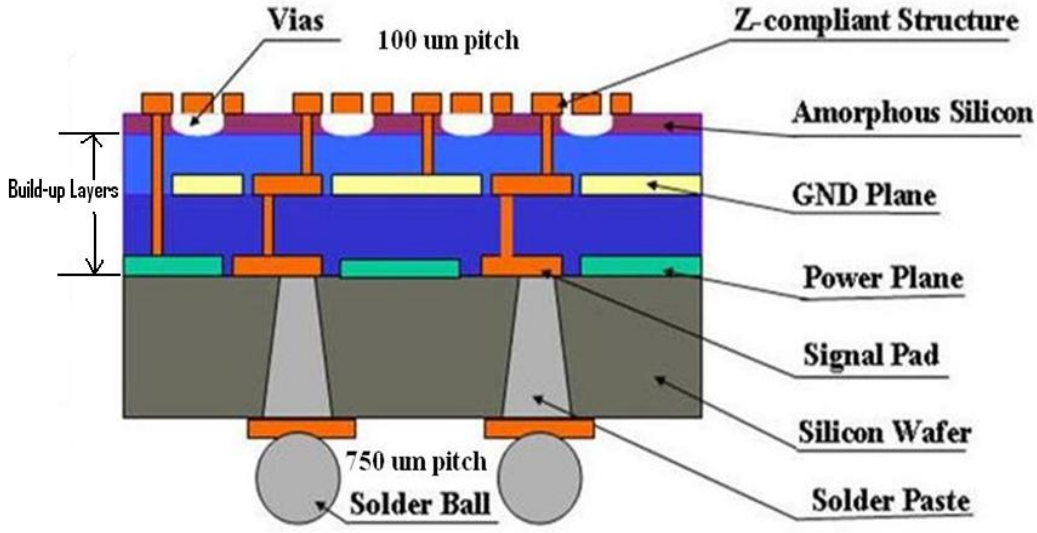


Figure 3.5: Cross sectional view of the proposed MEMS based interposer showing the build-up layers

3.2.1 Results Analysis

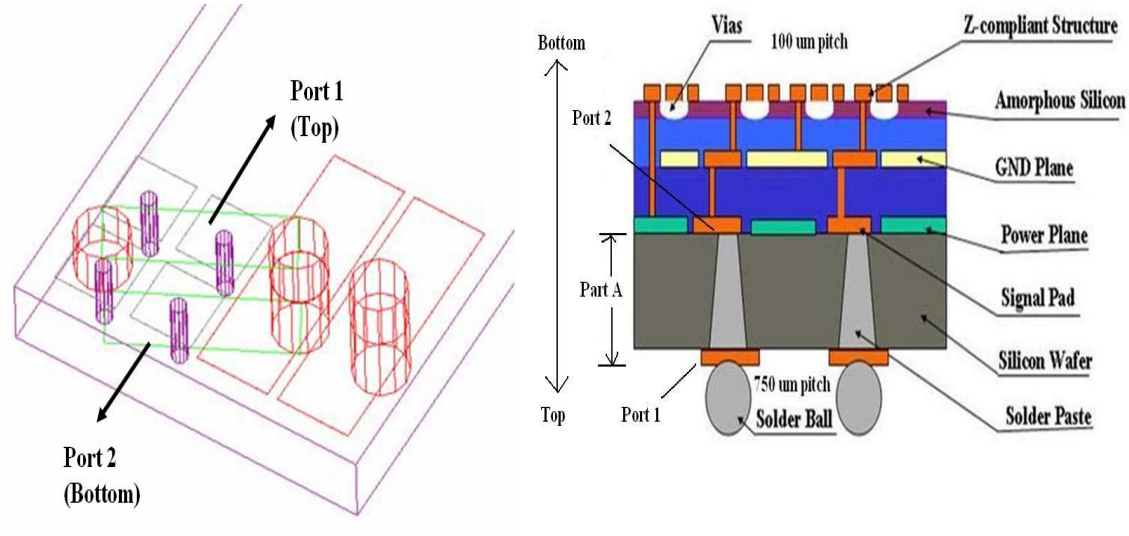
The created structure of the model (750 μm pitch/Port 1 to 100 μm pitch/Port 2 in the bottom-right corner of the interposer) was simulated and Figure 3.6 shows the overall response of the proposed MEMS based interposer.

Figure 3.6: The overall response of the proposed MEMS based interposer

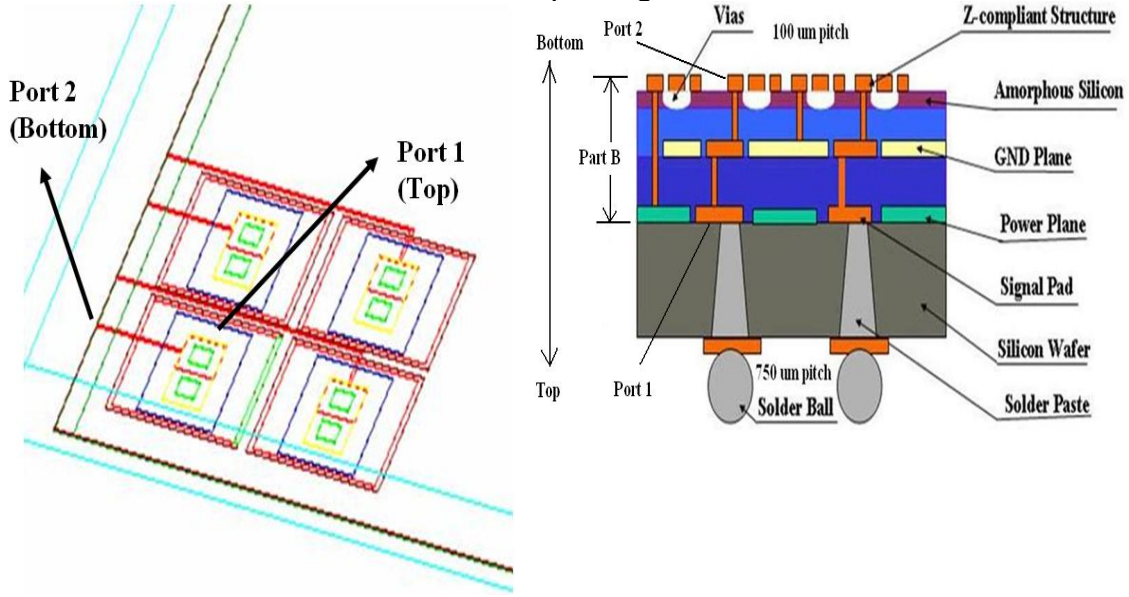
As can be seen from the Figure 3.6, the frequency response of this proposed interposer is very lossy within the frequencies of interest, it encounters 12 dB of insertion loss (designed value is 1 to 2 dB of loss) at 5 GHz, the target I/O speed. It has a -3 dB bandwidth of about 1 GHz, indicating this to be a poor candidate for the test and burn-in task of NWLP test.

To further investigate the structure, the model of the interposer was split into five parts bearing different features. These five parts were then simulated separately and examined. These five parts are presented in Figure 3.6, in which Part A and Part B make up the main parts of the interposer where Part A is carrying the 750 μm pitch inputs which are going

to be connected to the TSP and Part B is the build-up layers. Part C, D and E are the remaining parts that carry the signal to the 100 μm pitch I/Os. They are essentially transmission lines. Figure 3.7 shows where the models Part A and Part B were by relating them to cross sectional view of the interposer. The same have been done for Part C, Part D and Part E as well in Figure 3.8.



Part A model and its corresponding cross sectional view



Part B model and its corresponding cross sectional view

Figure 3.7: Part A and Part B of the interposer (reference can be seen in Figure 3.2)

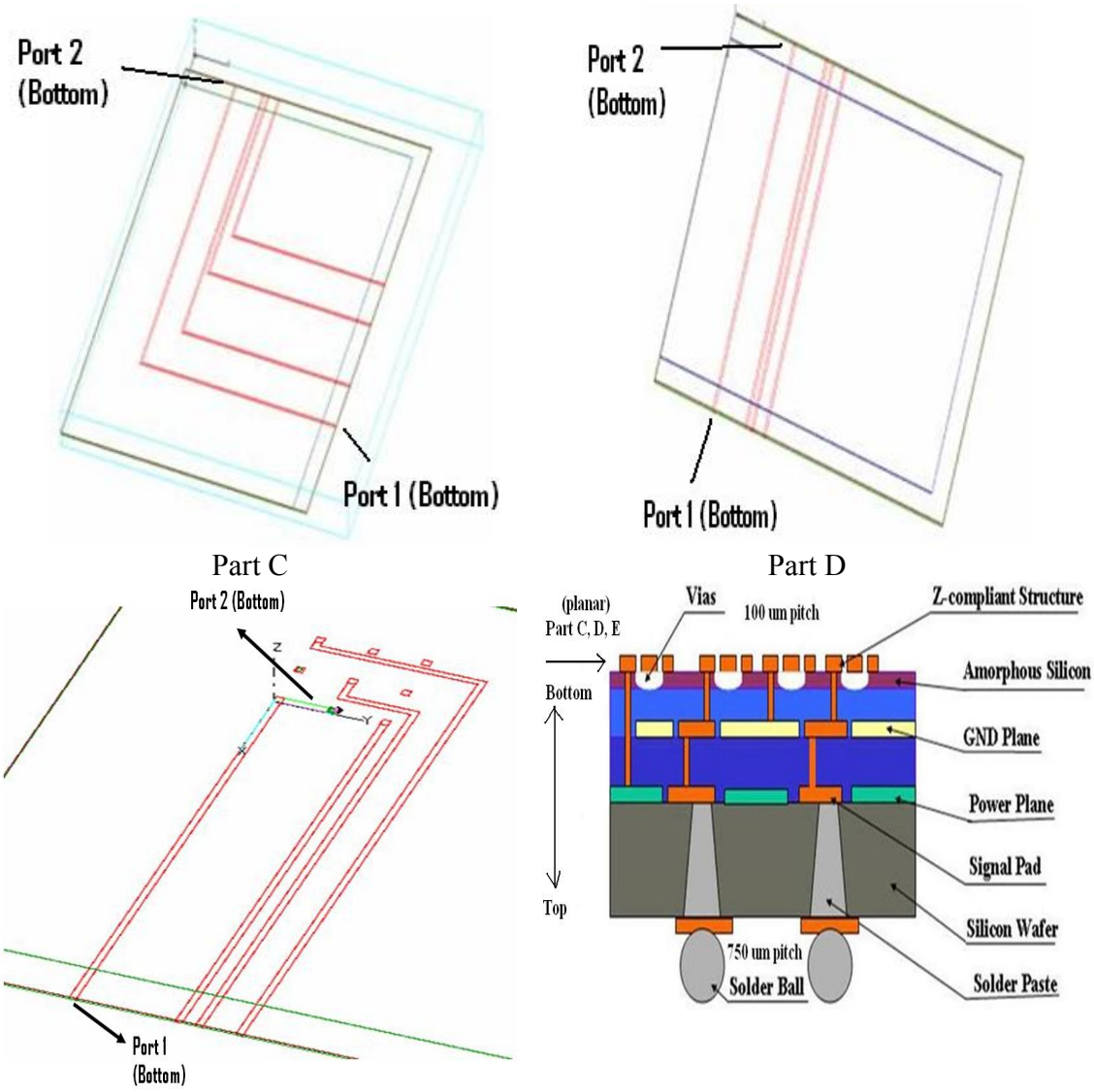
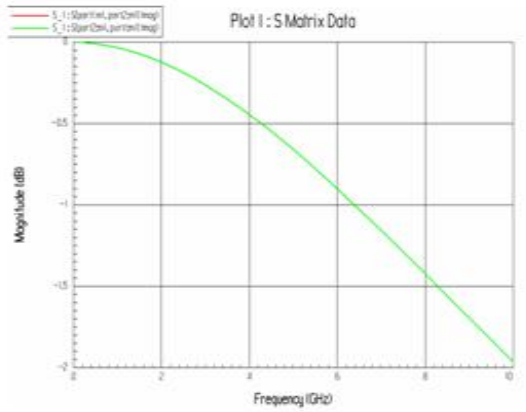


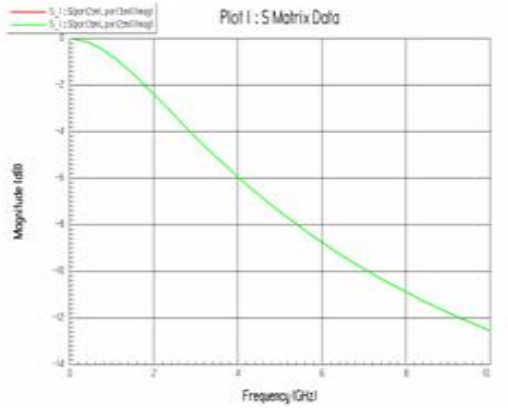
Figure 3.8: Part C, D, E models and cross sectional showing where they are (reference can be seen in Figure 3.2)

By following the excitation ports in each of the models shown in Figure 3.7 and Figure 3.8, a complete signal transmission path can be seen in which for Part A and Part B the signal is coming from the top to the bottom layer, whereas for Part C, Part D and Part E, the signal is traveling in the planar direction in the bottom layer.

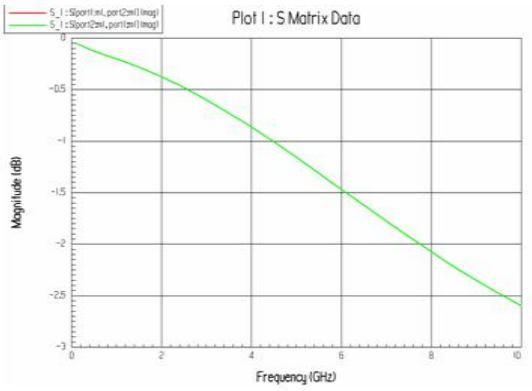
From the cross sectional view of the interposer, it can be seen that as the signal propagate through the build-up layers (Part B in Figure 3.7), there will be discontinuity due the two reference planes, power and ground. Hence, two set of simulations were done and studied with one using the power as the return path and another using the ground as the return path. Results of these are presented in Figure 3.9 and 3.10 respectively.



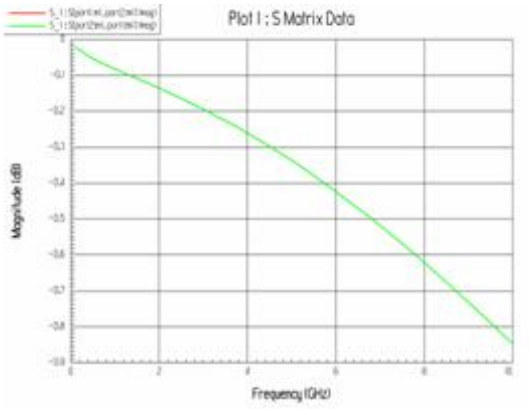
S21 of Part A



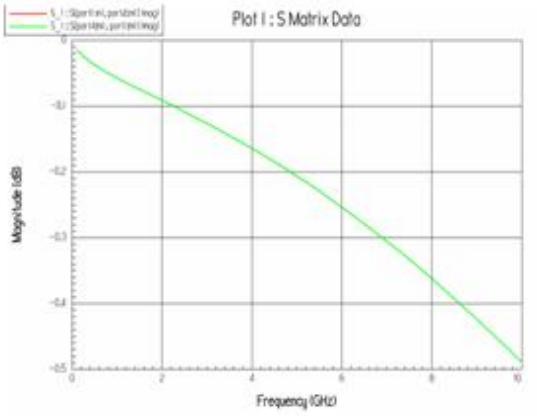
S21 of Part B



S21 of Part C

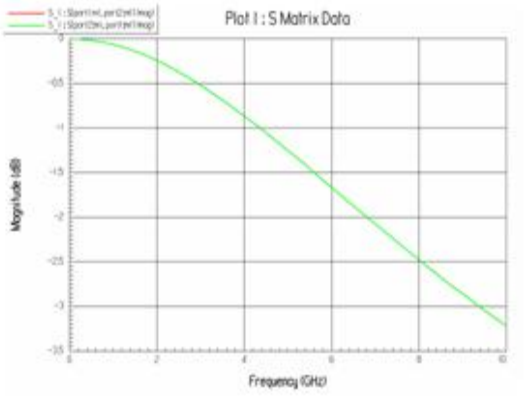


S21 of Part D

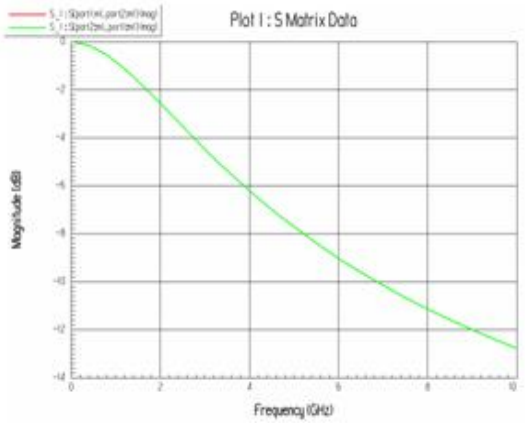


S21 of Part E

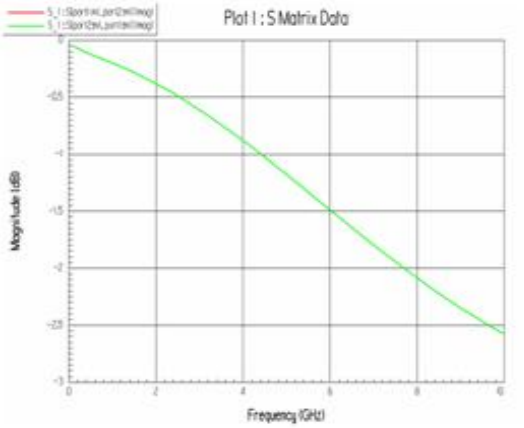
Figure 3.9: S21s of the five parts (signal–power)



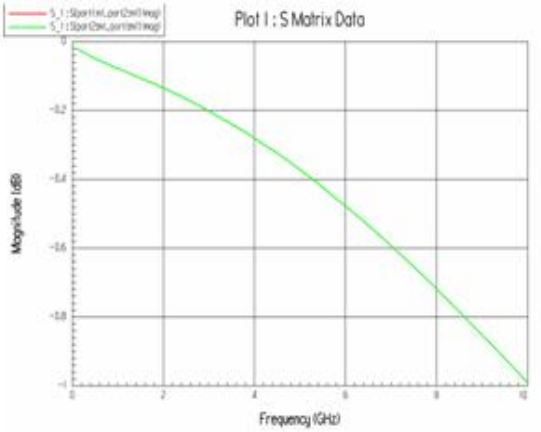
S21 of Part A



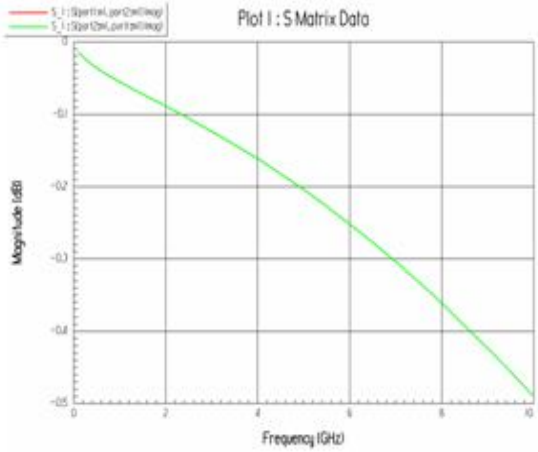
S21 of Part B



S21 of Part C



S21 of Part D



S21 of Part E

Figure 3.10: S21s of the five parts (signal-ground)

In Figure 3.9, with reference made to the power plane, the insertion loss, S21, for every each of the models is getting greater as the frequency increases. The insertion losses for them at 10 GHz are tabulated in Table 3.1.

Model	Insertion Loss, S21 at 10 GHz (dB)
Part A	2
Part B	12.2
Part C	2.6
Part D	0.85
Part E	0.5

Table 3.1: Insertion loss for models at 10 GHz when reference was power plane

Similarly, from Figure 3.10, with the reference made to the ground plane instead, the S21 insertion loss for every each of the models is getting worse as the frequency increases. Their values at 10 GHz are given in Table 3.2.

Model	Insertion Loss, S21 at 10 GHz (dB)
Part A	3.2
Part B	13
Part C	2.6
Part D	1
Part E	0.5

Table 3.2: Insertion loss for models at 10 GHz when reference was ground plane

It can be readily seen that Part B has significantly worse frequency response comparing to the rest of the models. It is mainly because the build-up layers of Part B would introduce switching reference to the propagating signal and it has a far more complicated structure than the rest of the parts of the interposer. The likelihood of reflections and capacitive parasitic would appear to be higher for Part B.

To examine these losses in the full interposer model perspective, these calculated S-parameter sets were cascaded in the HP Advanced Design System (ADS) as shown in Figure 3.11. Figure 3.12 shows the comparisons between the overall signal-power transmission loss and the overall signal-ground transmission loss.

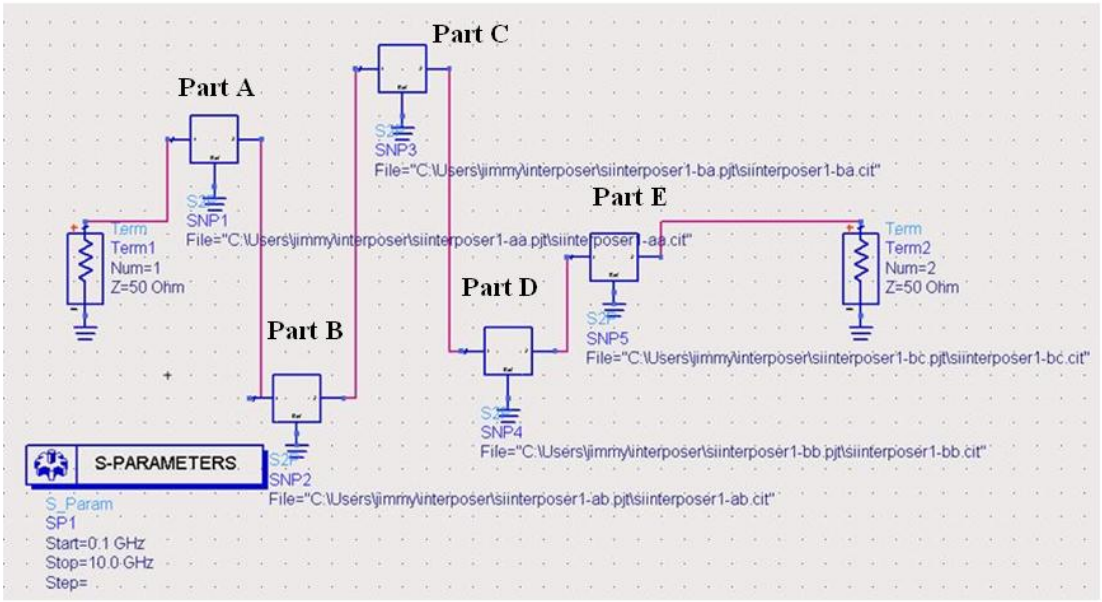


Figure 3.11: Five parts cascaded in ADS

Figure 3.12: Comparisons of the complete signal path transmission loss of signal-power to signal-ground

3.2.1.1 Optimization

Since Part B was found to be the one with the worst frequency response, optimization was attempted to improve the signal integrity. Three aspects of the Part B can be the cause for the high losses. The first is the material used for the dielectric (Figure 3.13) in between the build-up layers and its thickness which are responsible for the dielectric loss encountered.

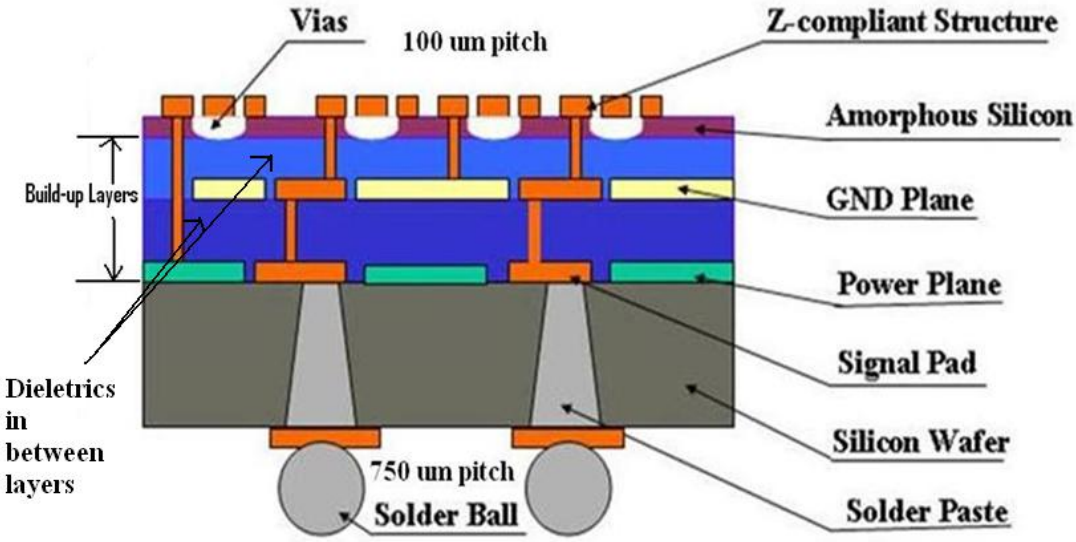


Figure 3.13: Dielectrics in between the build-up layers

The following figures present the effect of the dielectric constant and thickness of the built-up layers. Comparing BCB (dielectric constant, K = 2.6) with SiO_2 (K = 4) in Figure 3.14 and Figure 3.15, it was found that when used at a lower frequency, a higher K value material (SiO_2) is preferable. On the other hand, low K material should be used in higher frequency applications, as can be seen from the figures. Dielectric material thickness also has a great impact on the signal loss, as can be seen from Figure 3.14 and 3.16, when the thickness of the dielectric material increases, the signal transmission

improves. These results show that the choice of the material for the build up layers should be done with care.

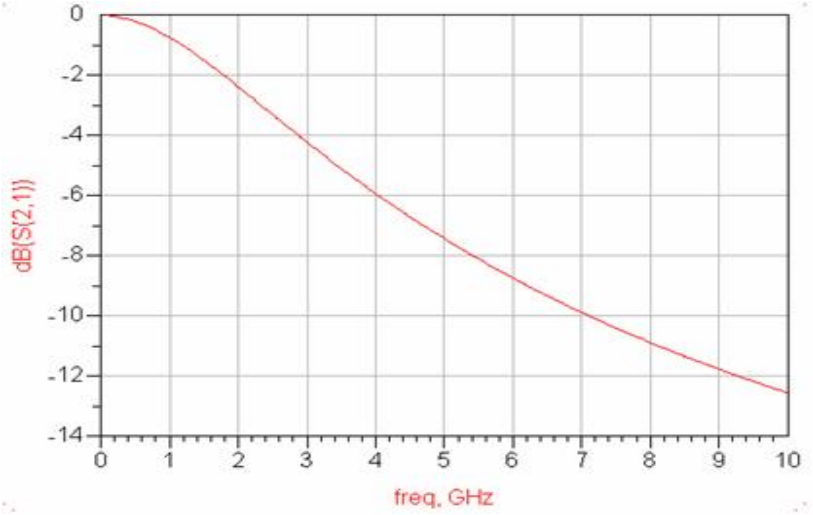


Figure 3.14: Insertion loss for Part B
(BCB as dielectric, thickness 2 μm)

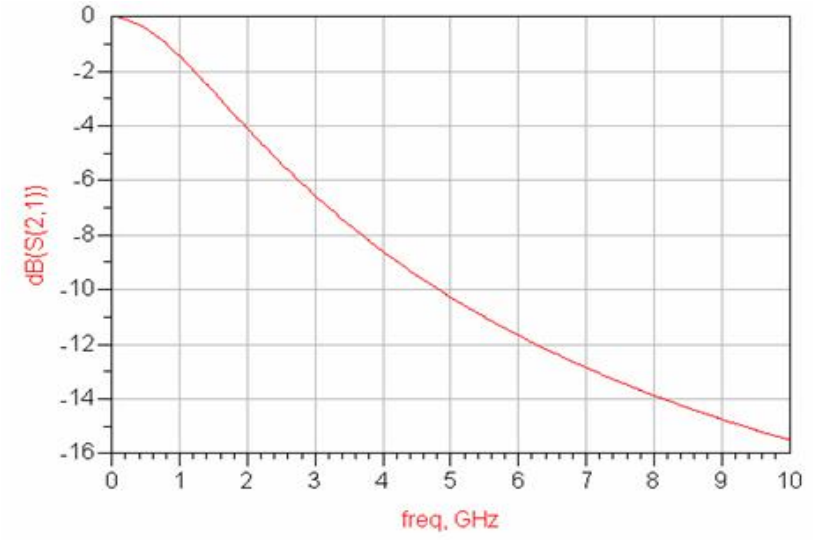


Figure 3.15: Insertion loss for Part B
(SiO_2 as dielectric, thickness 2 μm)

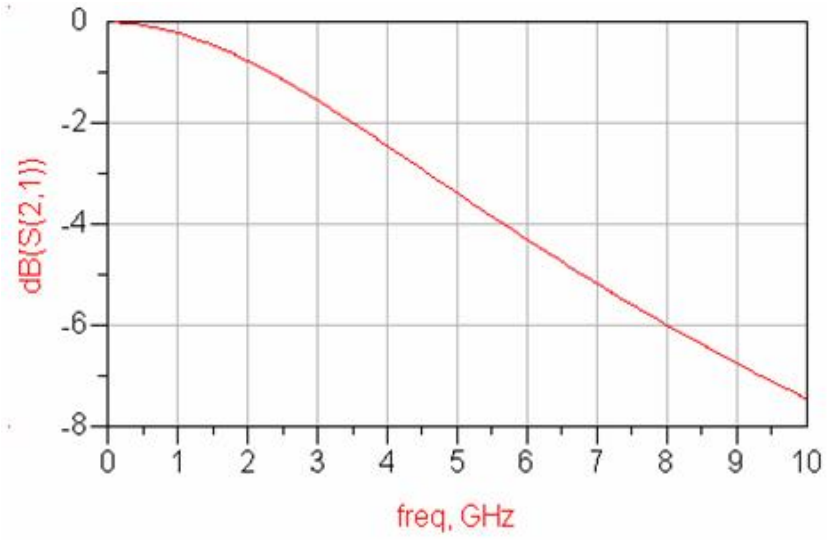


Figure 3.16: Insertion loss for Part B
(BCB as dielectric, thickness 4 μm)

The second cause of the losses are that the power and ground planes in between the layers are introducing discontinuities, which give rise to reflections. To show how badly this is affecting the signal, Figure 3.17 shows the response of Part B with one of the reference planes is taken away. The response as shown has improved drastically with only about 0.48 dB of insertion loss at 10 GHz in contrast to the previous 13 dB.

Figure 3.17: S21 of Part B with one of the reference planes taken (BCB as dielectric, thickness 4.9 μm)

The third cause is that the parasitic capacitive between layers of the pads and the planes are seriously affecting the signal integrity of the structure. Therefore, in order to optimize the performance of the structure, these capacitive effects could be kept in the minimum with proper cut-out between the planes to reduce the overlapping area that they could have. Figure 3.18 shows the comparison between initial design and optimized design. The capacitive effects have been minimized in the optimized design as can be noted from the fact that the electric field between the layers has been greatly reduced. The insertion loss of the optimized design is presented in Figure 3.19.

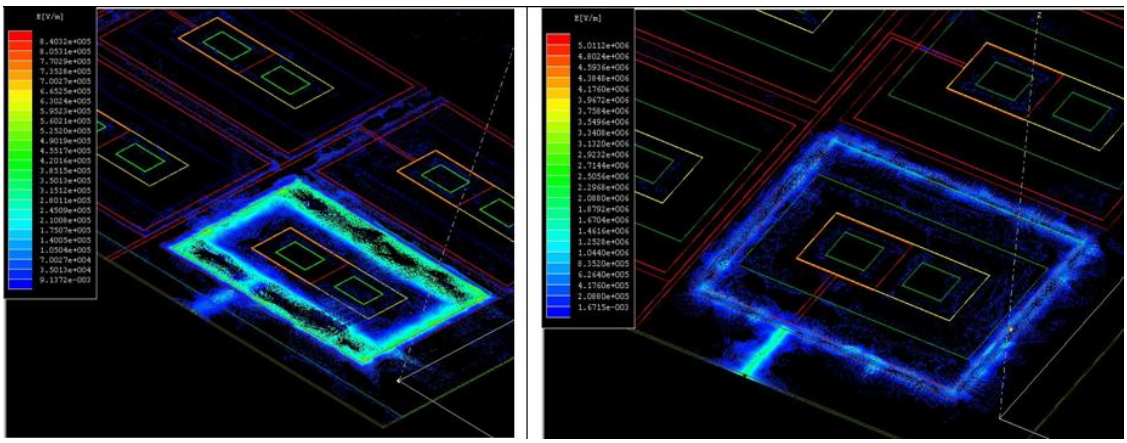


Figure 3.18: Comparison of capacitive parasitics of Part B between initial design (left) and optimized design (right)

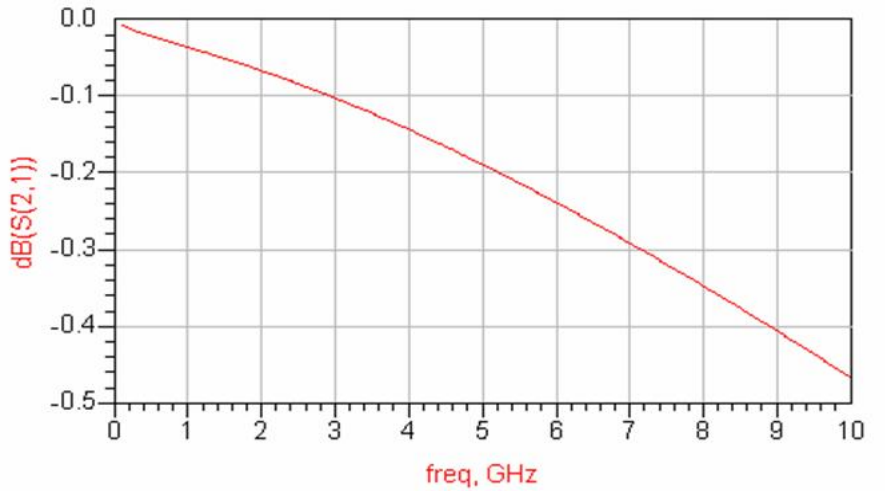


Figure 3.19: The much improved response of the optimized design of Part B

3.3 Summary and Discussions

Electrical characterization of the MEMS based interposer using silicon as the substrate has been done through modeling and simulation. Studies were done in order to understand the signal propagation and transmission losses. Optimization of the design focused on the build-up layers structure was carried out successfully with significant improvements. However, the optimization was done without considering the actual real world limitations. The proposed design of the interposer can sometimes not be changed arbitrarily in order to optimize the electrical high speed performance. This is due to the limitations of the processing and fabrication technology of existing facilities. It is simply not feasible to fabricate it. However, based on the simulation results, with a proper choice of materials and access to better process facilities, the requirements of NWLP test and burn-in can be met by this proposed MEMS-based interposer concept. In other words, if better compromise between the mechanical and electrical requirements can be made, implementation of this concept of interposer would be feasible.

Chapter 4

Elastomer based Interposer

Having studied the characteristic of the proposed MEMS based interposer mentioned in the previous chapter, an alternative elastomer based interposer was designed and fabricated. By carefully adhering to design rules, this interposer is better suited for the technical requirements of high density I/Os and a fine pitch, wafer level packaged devices test. Similarly, it was designed to meet the specifications of the test. The unique part of this interposer is that there is an elastomer structure (called "trampoline") which provides the compliance needed for the test. Simulation results of the board part of the interposer will be presented. Later, the responses of the various parts of the test setup including the DUT structure and small interconnects mounted on the chip will be combined to present the overall test system response. This response will be compared to the measured response of the fabricated interposer to verify the accuracy of the simulated models. Next, some variations on the simulation will be performed for comparison. After that, parametric variation of the interposer will be studied. Various parts of the interposer structure are parametrically varied to improve the overall signal integrity.

4.1 Introduction

The design of an elastomer-based interposer was performed within the guidelines such as fine pitch, high density I/Os, compliance as mentioned in Chapter 1. The test concept is

shown in Figure 4.1 with detailed structure of the interposer omitted. It is also a cross sectional view of the test setup. Another cross sectional schematic view is given in Figure 4.2. The interposer is basically made up of 5 parts, the RF/SMA connectors on the top layer, the main board part (with controlled impedance traces on the top layer), the vias connecting to the bottom layer, the 100 pitch traces at the bottom layer connecting to the elastomer "trampoline" and lastly the trampoline that is going to be connected to the DUT. One complete signal traveling cycle looks like SMA connector—top layer trace (the main PCB interposer Board)—via—bottom layer short trace—trampoline—DUT—trampoline—bottom layer short trace—via—top layer trace—SMA connector, as shown in Figure 4.3. With proper press force applied, the DUT will be able to be connected to the interposer board structure.

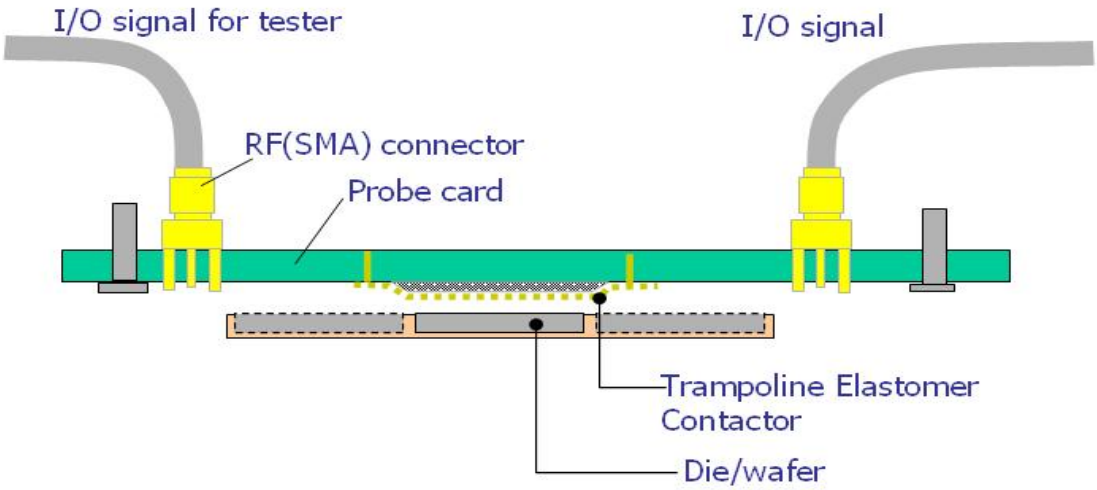
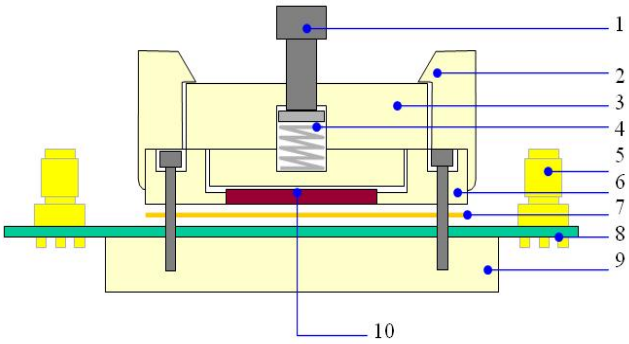


Figure 4.1: The test concept (cross sectional view)



PCB, mesh, socket and chip all contribute towards contact alignment. Manufacturing variations are compensated by offset in DUT dicing

	Parts name	Material
1	Pressure Adjust	Techtoron PPS
2	Screw Clamp lever	Techtoron PPS
3	Device press plate	Techtoron PPS
4	DUT press spring	
5	SMA RF connector	
6	Device Guide	Techtoron PPS
7	Trampoline Contactor	forming
8	PCB	BT Resin
9	Base Plate	Techtoron PPS
10	DUT	Wafer Level Package

Figure 4.2: Cross sectional schematic view of the test interposer

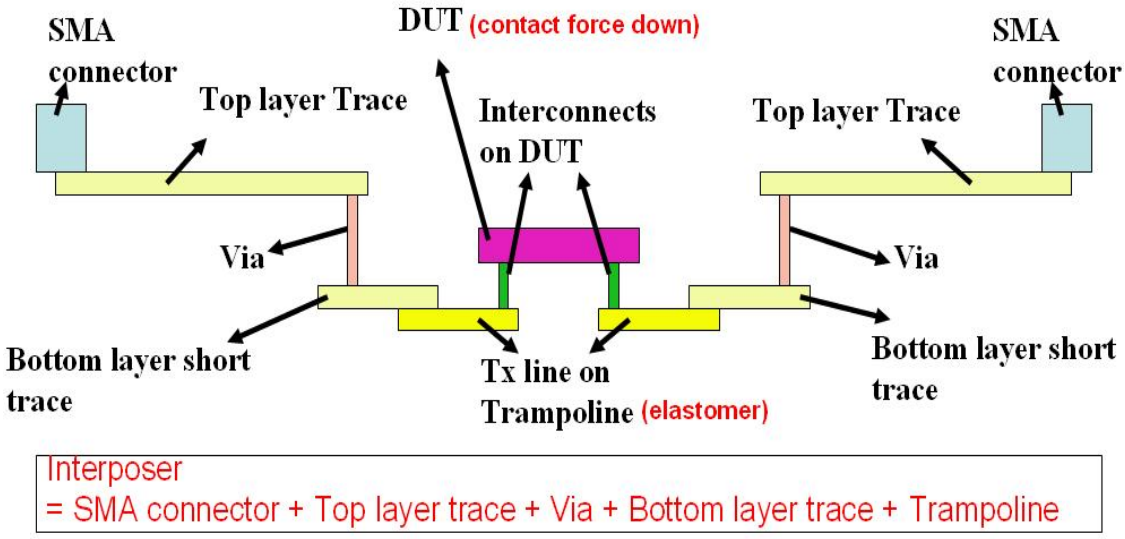


Figure 4.3: Cross sectional view showing the complete test signal transmission

To illustrate the geometry of the interposer, a 3D view of the fabricated prototype interposer is given in Figure 4.4. This prototype interposer is capable of probing 8 test lines concurrently. Four SMA connectors for two pairs of I/Os which send the signal in/out through the DUT (doing the wafer test) were mounted. In addition, two SMA connectors for a pair through line I/Os were mounted as well. Since this through line is

just a planar trace on the board top layer connecting two I/Os, measurement can be done through these through line I/Os to provide the loss information of the interposer board part alone without taking into account of the vias, the trampoline and the DUT. The SMA connectors used were 3.5 mm diameter SMA connectors. They are suitable for applications up to 18 GHz. Manual alignment of the DUT is done by the socket. It can be screwed to adjust the contact pressure. In addition, there are clamps to hold the socket cover in place as shown.

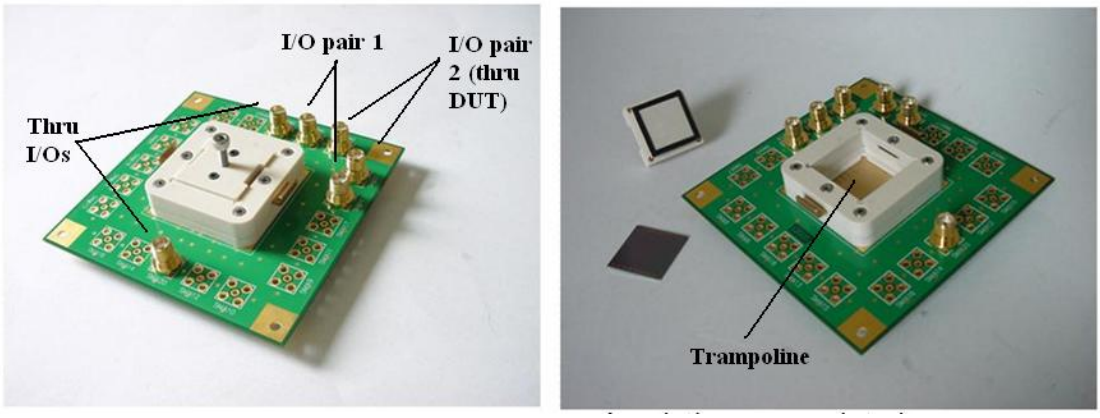


Figure 4.4: Fabricated prototype test socket

Signal from the tester passes through the RF connector, the board part of the interposer to the elastomer structure, the DUT and then to the output. Apart from the probe card board structure, this interposer is designed to have a special elastomer structure, called the "trampoline", which can provide compliancy during probing when it is pressed with proper force. It is basically an elastomer mesh cushion structure as shown in Figure 4.4. Close-up view of the trampoline is given in Figure 4.5. The elastomer mesh provides the vertical compliance needed while the copper weaved in between the mesh would provide the connection for the signal. Low K (2.86), low loss tangent (0.002) dielectric was used for this trampoline structure for efficient signal transmission. Copper metallization is

used as the probing contact due to its low contact resistance. The top view of the complete layout of the trampoline mesh is shown in Figure 4.6. As shown in Figure 4.6, there are 8 pairs of I/Os on the trampoline for the WLP test. The rest of the trampoline is mesh made up of woven copper traces.

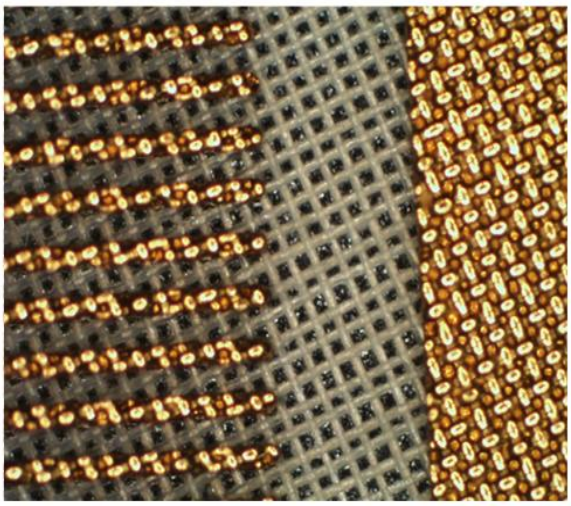


Figure 4.5: Close-up view of the trampoline

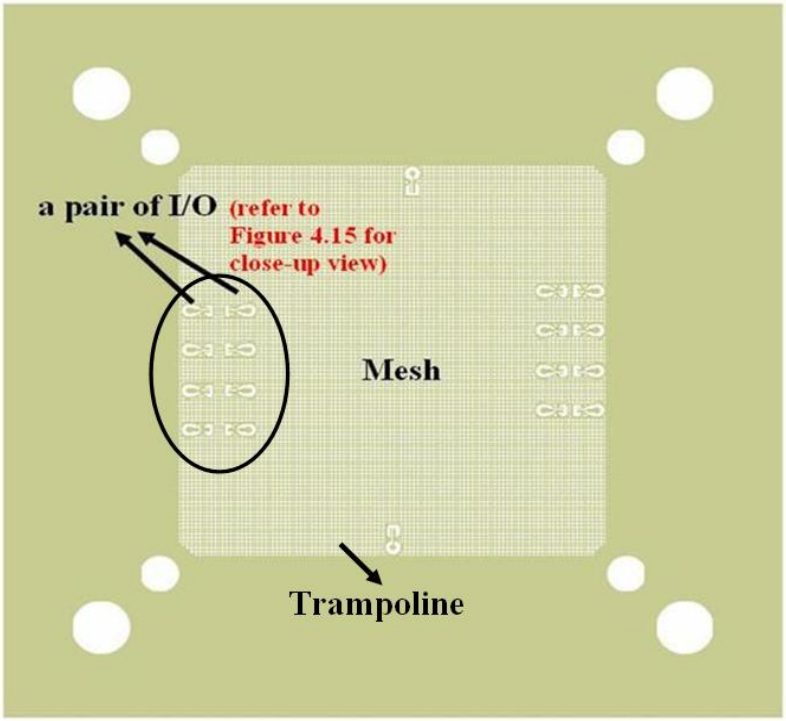
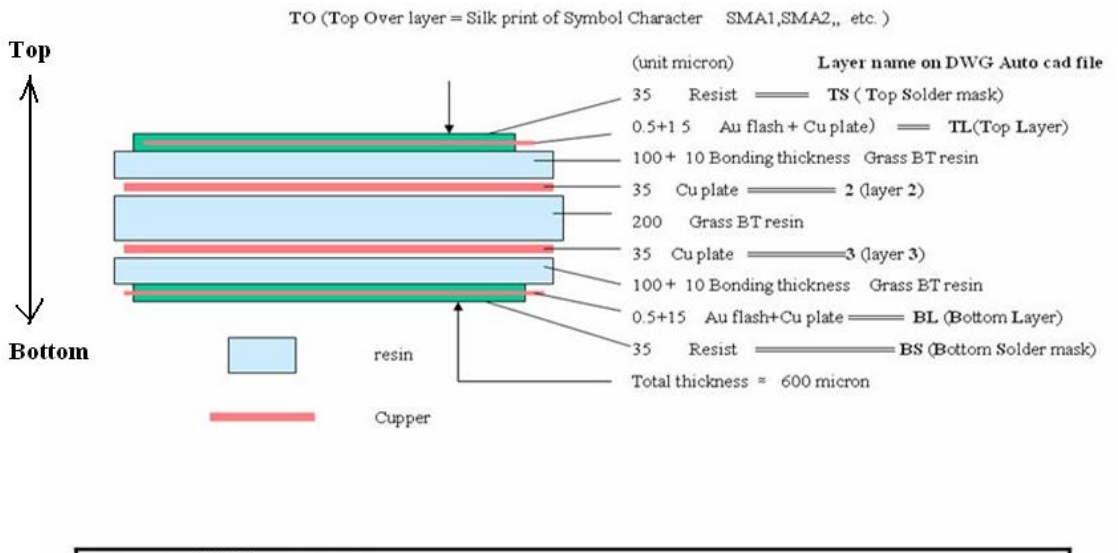


Figure 4.6: Top view of the complete layout of the trampoline

Cross sectional view in Figure 4.7 shows the thickness of each layers from top to bottom and the composition of the materials used in the design of the interposer. BT resin with dielectric constant of 4.4 was chosen to be the dielectric for better performance at high frequency.



Characteristic of PCB (Grass BT resin)							
ITEM	Tg (Deg.C)	Dielectric constant	Loss tan	Water absorption (%)	Max OP temp. (Deg.C)	Surface Resistance (Ohm)	B/Twist (N/mm)
CCL-H800	210	4.4	0.007 ±0,001	0.11	220	5x10e13-15	550

Figure 4.7: Cross sectional view of the interposer showing the thickness of the layers and the composition of the materials used

To further illustrate the physical design of the interposer, the top view of the layout of the elastomer interposer is presented in Figure 4.8. All the transmission line traces on the top layer are designed to be close to the controlled 50 Ω impedance microstrip lines. They have width of 200 μm and a distance of 110 μm to the return path underneath. The coplanar return path is 800 μm apart from the signal trace, hence the effect of coplanar grounding is not strong. Figure 4.9 shows the calculation of the designed value of close to 50 Ω characteristic impedance for the microstrip lines using the TXline from the Applied

Wave Research, Inc [32]. In addition, Figure 4.10 shows the top view of the top layer only with dimensions given.

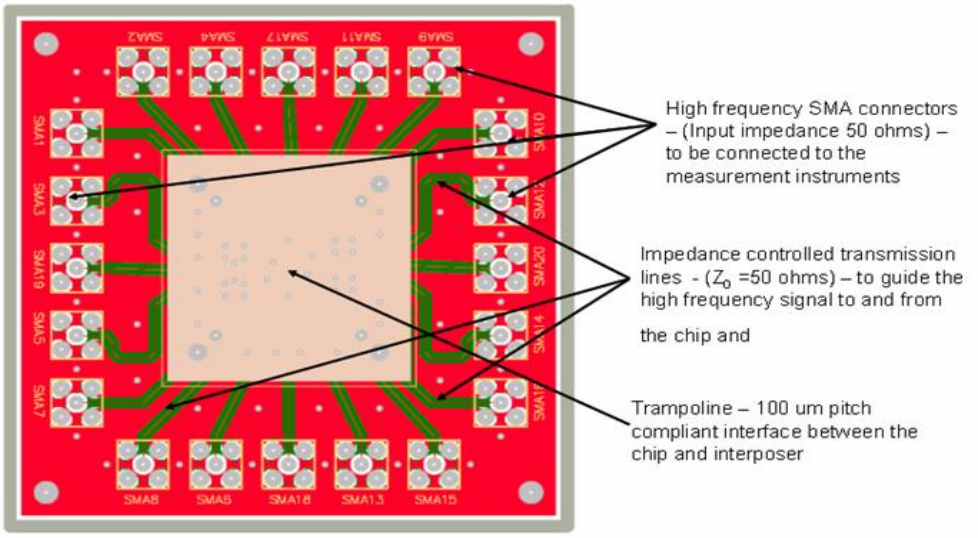


Figure 4.8: Top view showing the layout of the proposed elastomer interposer

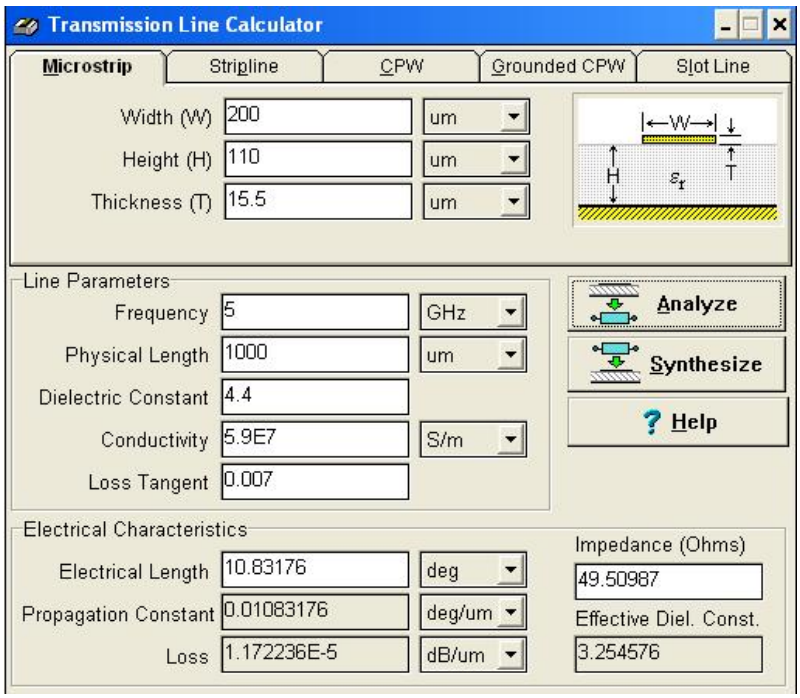


Figure 4.9: Characteristic impedance of the designed microstrip

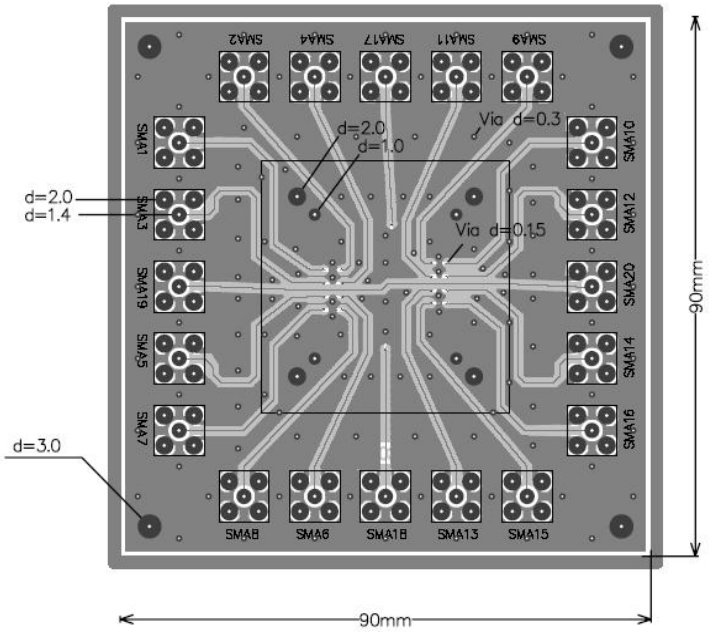


Figure 4.10: Top view of the top layer of the interposer showing dimensions

In contrast, the bottom layer with solder mask is shown in Figure 4.11. The eight 100 µm pitch openings are for the short traces on the bottom layer of the interposer. Signals travel to one end of these short traces through the vertical vias connected to the top layer traces, while the other end of these short traces form the probe contact to the DUT through the elastomer trampoline structure.

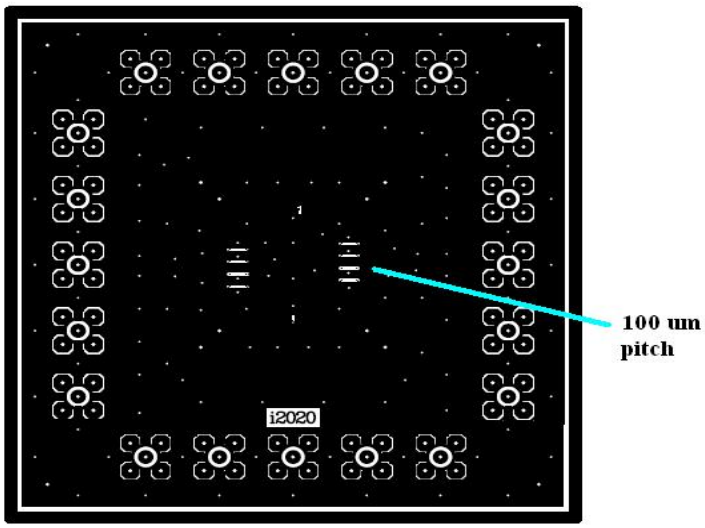


Figure 4.11: Bottom layer of the interposer showing the 100 µm pitch side

4.2 Modeling, Simulation and Measurement

A model which includes all the important features of the proposed elastomer interposer was created in the numerical solver. Two corner signal paths on the interposer as shown in Figure 4.10 have been chosen to do the EM high frequency full wave simulations. The frequency domain simulations were done as two-ports, in which ports excitations were set as wave ports with port impedance self calculated. The boundary condition was specified as a radiation box covering the model closely. The radiation boundary was created to let the radiated waves pass through the boundary undisrupted, since in real life, the interposer would be exposed in open space. A frequency sweep from 100 MHz to 10 GHz was performed to investigate the bandwidth of the interposer. The numerical solver uses finite element method (FEM) to solve the EM models.

Calculated S-parameters from the simulations which contained the information of insertion loss and reflection loss. These were analyzed to see how much attenuation was introduced by the structures. In the initial model, SMA connectors were not considered, but later models with SMA connectors were built to serve as comparisons to those without them. Figure 4.12 shows two 3D models constructed, one with the SMA connected and one without. Figure 4.13 shows some extra illustrations of the simulated model. Port 1 is a circular wave port on the edge of the SMA connector and port 2 is a rectangular wave port created at the bottom of the interposer where the vias connected short traces are.

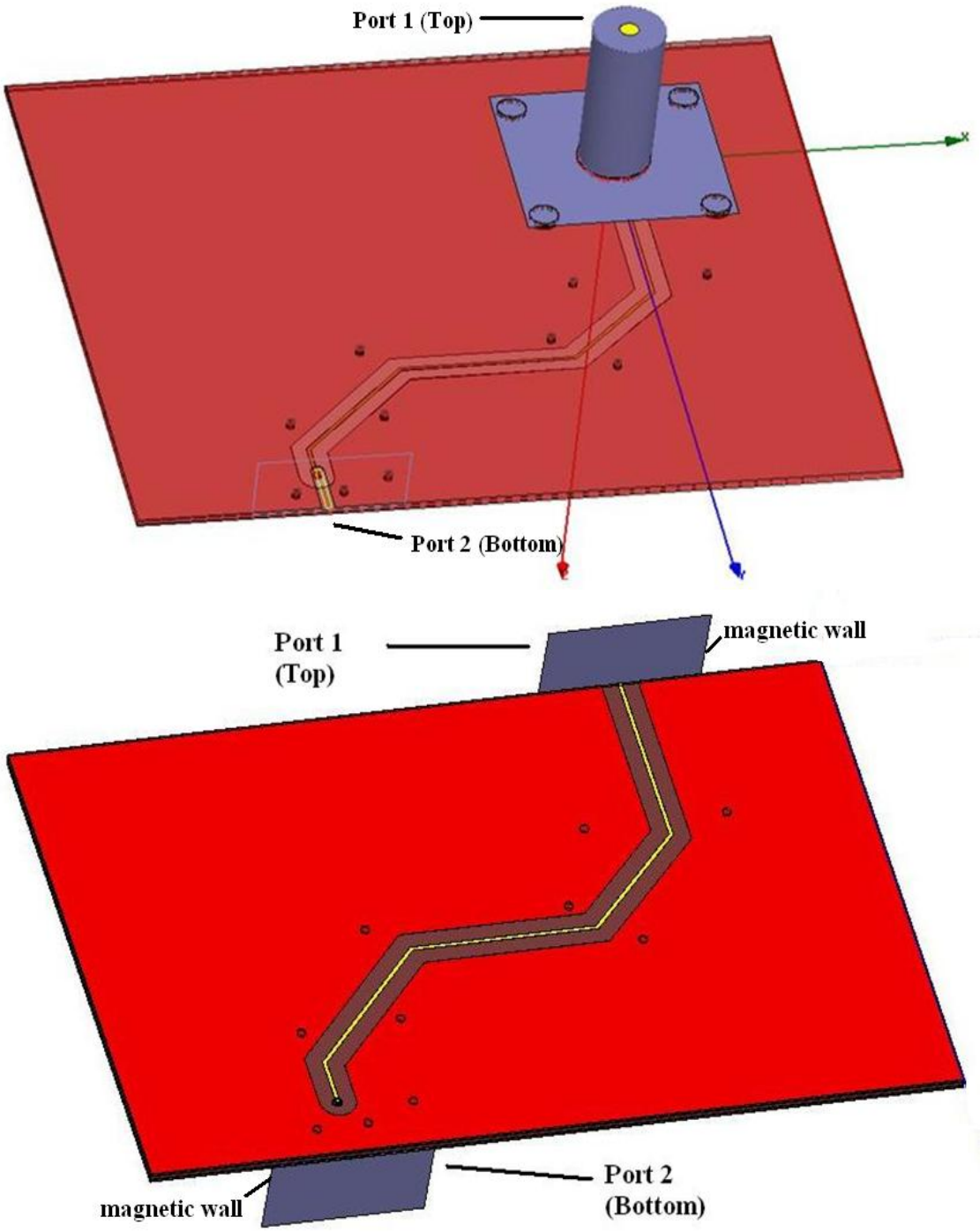
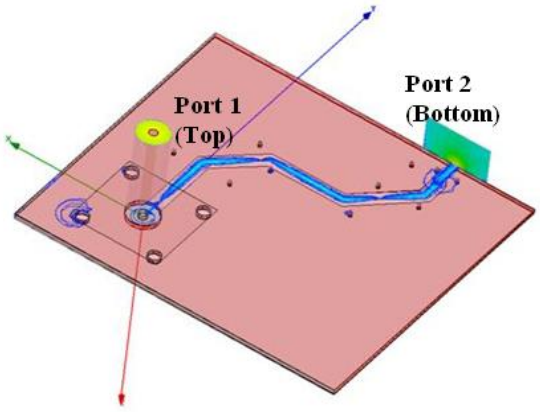
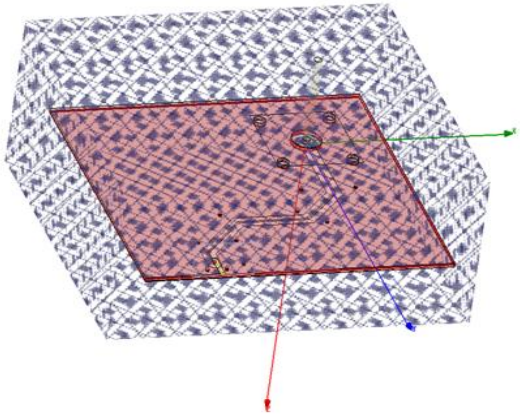


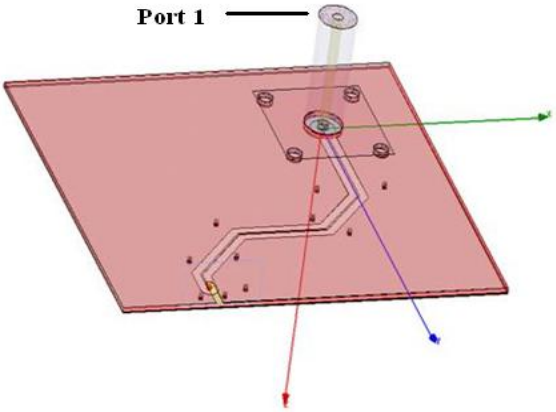
Figure 4.12: 3D models of the interposer with and without SMA connector showing excitation ports



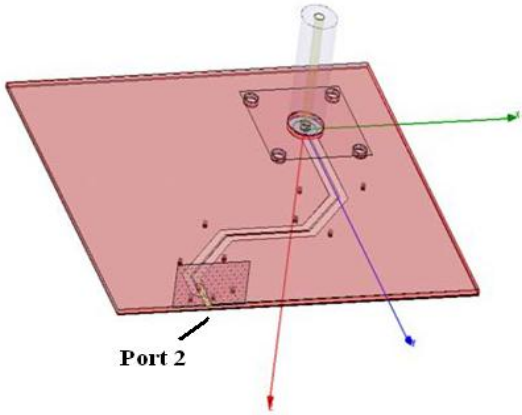
Model showing current density



Model showing boundary condition (radiation)



Model showing port 1



Model showing port 2

Figure 4.13: Simulated models

4.2.1 Results Analysis

A comparison of the S-parameters obtained using models with and without SMA connector (the models in Figure 4.12) is presented in Figure 4.14. It can be readily seen that the model without the SMA connector has insertion loss less than 2 dB up to 10 GHz while for the model with the SMA connector, it performs well up to about 7 GHz with a loss of 1.5 dB.

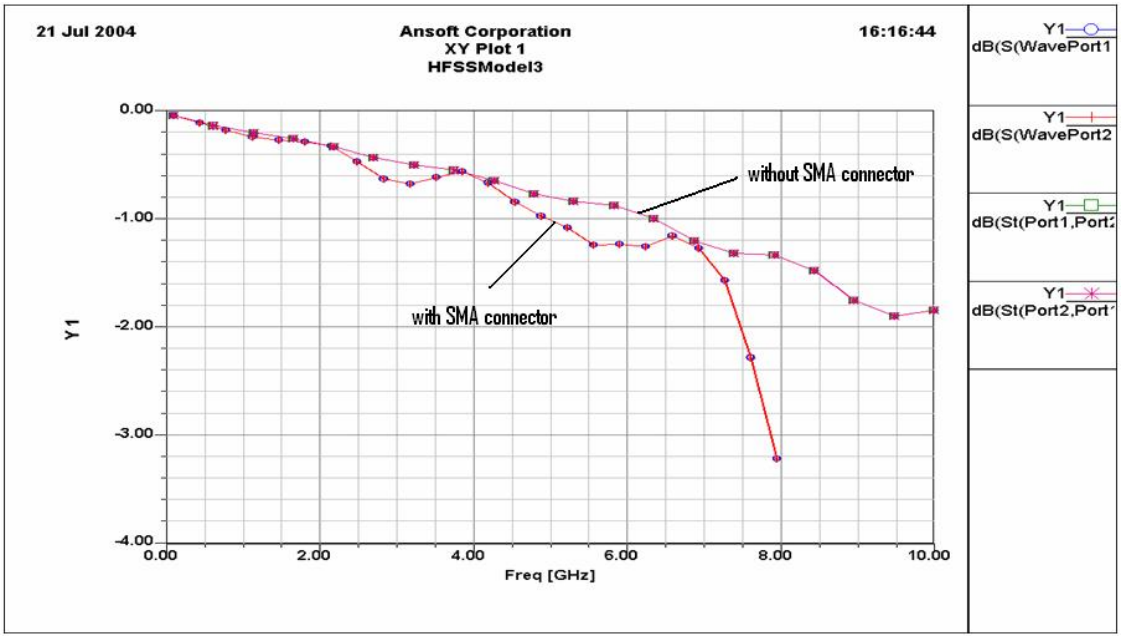


Figure 4.14: S21 comparison of interposer board part between with and without SMA connector

4.2.1.1 Trampoline

So far, the model only included the board part of the interposer (inclusive of the vias transition part and the bottom short traces) without the trampoline part. Thus, another model for the trampoline was created and is presented in Figure 4.15. Figure 4.16 shows the actual structure of this model. Similarly, 2-port frequency domain simulation was done for this model. The boundary condition was again specified as a radiation boundary. However, the excitation ports were created as lumped point sources, which required the port impedances to be specified. Port 1 and port 2 can be noted in Figure 4.15 as well.

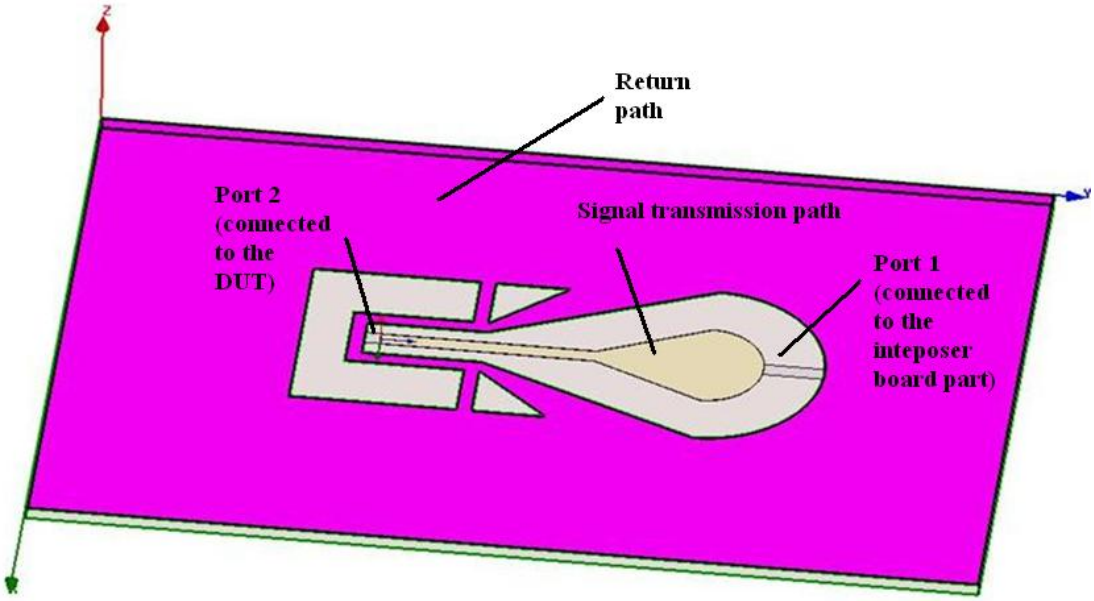


Figure 4.15: The model of the trampoline showing excitation ports

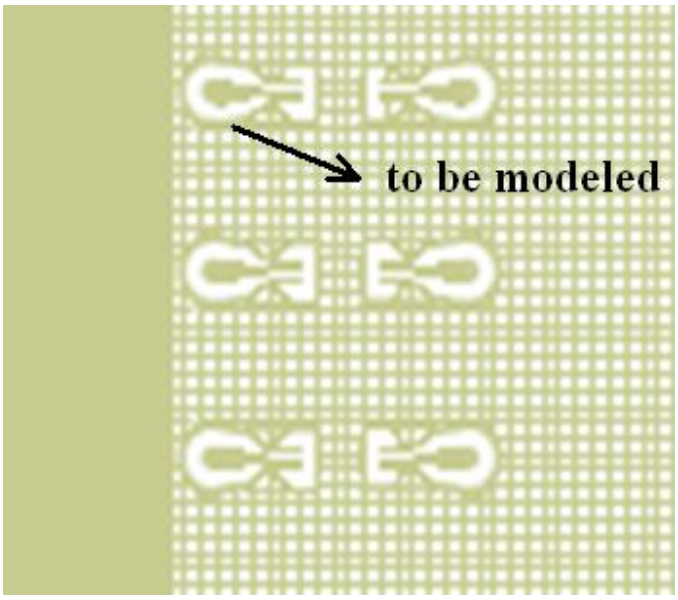


Figure 4.16: Actual layout view of the trampoline

4.2.1.2 DUT Test Structure

The test structure on the device under test (DUT) chip is a coplanar waveguide (CPW). It was created on high resistivity silicon of 2 kΩ-cm for low loss consideration. The chip has a pitch of 100 microns as presented in Figure 4.17. Initial 2-port S-parameter

measurements on the chip were done using vector network analyzer (VNA). The results are given in Figure 4.18. The frequency domain measurements were done with standard SOLT (short, open, load and thru) calibration. Alumina substrate was used for the calibration. The measurements were done in chip level with the reference close to the edge of the CPW line structure. 150 µm pitch GSG probes were used. These measurements show how much transmission loss the signal will experience when passing through the test structure.

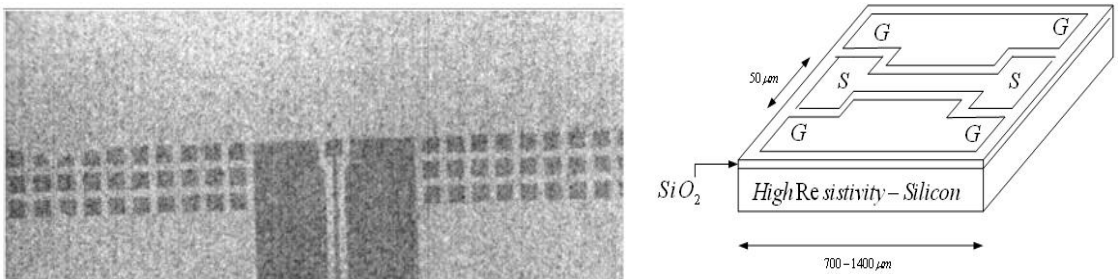


Figure 4.17: The DUT showing the CPW test structure

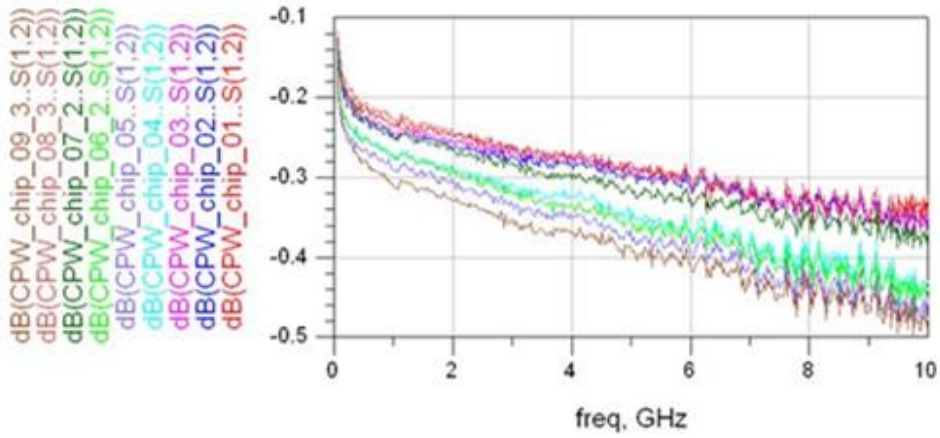


Figure 4.18: Transmission loss S21 of the DUT

4.2.1.3 Overall Test System

To fully demonstrate and investigate the overall system behavior (the complete signal transmission of the wafer level test using this proposed interposer), the response of the board and the trampoline parts of the interposer need to be combined in a system model with the response of the WLP interconnects mounting on the DUT and the response of the DUT itself. The full system model was implemented in ADS. The model was made up of black boxes containing simulated or measured data or an equivalent circuit model. The schematic of this system model is provided in Figure 4.19. As shown in the Figure 4.19, there are basically four components in this system model: the interposer board with SMA connectors (represented by simulated data), the trampoline contact (represented by simulated data), the interconnects on the DUT chip (represented by equivalent circuit model) and the DUT test structure (represented by measured data). Four port frequency domain (100 MHz to 10 GHz) S-parameter simulation was done using this system model to obtain the overall system performance. Interposer PCB board part with SMA connector and the elastomer trampoline structure simulated data was obtained by solving their simulation 3D models which have been shown above in Figure 4.12 and Figure 4.15 respectively. The measured data of the DUT test structure is also presented in Figure 4.18.

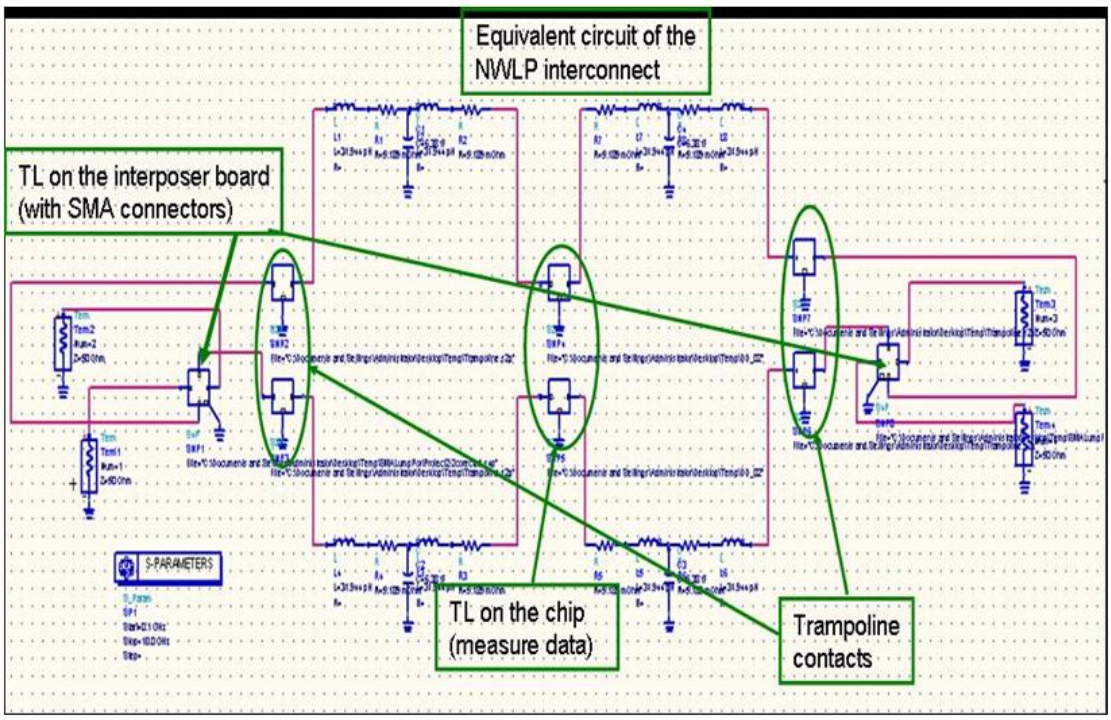
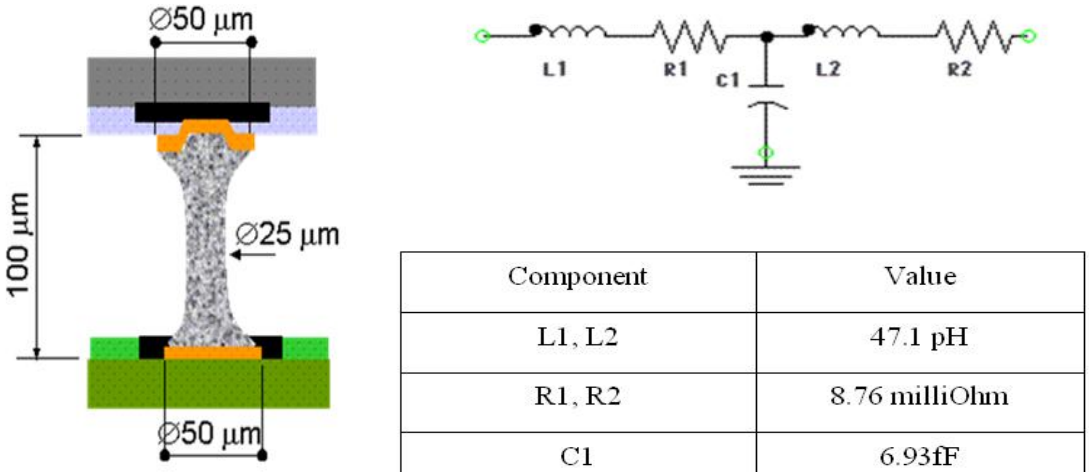


Figure 4.19: System model for the WLP test showing four sets of components (represented by either simulated data, measured data or equivalent model respectively)

Some variations were made to the system components to serve as comparison. First, there are two possible candidates for the interconnects created on the chip: one is the Bed of Nails (BON) interconnects and the other is the Stretched Solder Column (SC) interconnects. There are also two test structures on the DUT to be tested: one is a longer CPW and the other is shorter. Characterization of these interconnects and measurements of the DUT chip transmission lines were performed in advance. Modeling of the interconnects was done using a full-wave solver. Calculated S-parameters were used to extract the equivalent circuits which could accurately represent them. Figure 4.20 shows the model and the equivalent circuit representing the Stretched Solder Column interconnects.



Component	Value
L1, L2	47.1 pH
R1, R2	8.76 milliOhm
C1	6.93fF

Figure 4.20: Model and equivalent circuit for the Stretched Solder Column interconnect

From the equivalent circuit in Figure 4.20, the 2-port impedance matrix of this Stretched Solder Column can be given as:

$$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} Z_{L1} + Z_{R1} + Z_{C1} & Z_{C1} \\ Z_{C1} & Z_{L2} + Z_{R2} + Z_{C1} \end{bmatrix}$$

Figures 4.21—4.24 show comparisons of some variations on the setup of the system. In Figure 4.19, a 4-port simulation was examined. Hence the following figures show insertion losses S31 and S42. The simulations results were done only from the SMA connector to the DUT transmission, which means it only covers the first half of the system model in Figure 4.19 plus the DUT. Figure 4.21 gives the comparison of the response of different lengths of the transmission lines on the DUT using the Bed of Nails interconnects. Figure 4.22 shows the comparison of the response of different lengths of the transmission lines on the DUT using the Stretched Solder Column interconnects. It can be noted that the impact of these variations of the transmission lines on the overall system response is very small. This is mainly due to the fact that the difference in S21

between the two different lengths of CPW is very small compared to the overall response. Both of them are very short transmission lines compared to the complete signal transmission path of the test. Therefore, the impact of changing the fine pitch interconnects used on the chip is minimal.

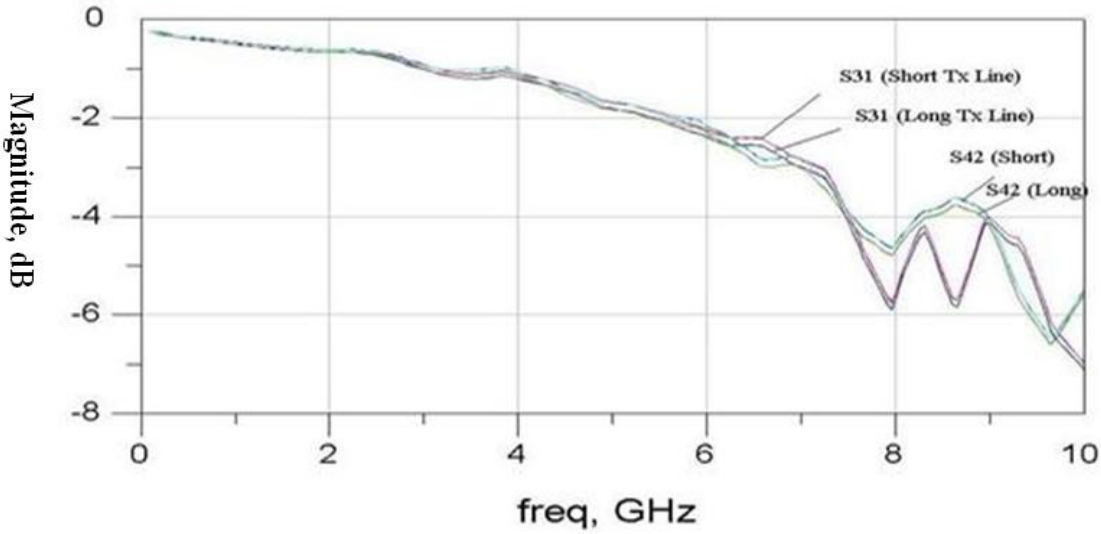


Figure 4.21: Insertion loss comparison of the system setup on different lengths of the CPW on the chip using BON as interconnects

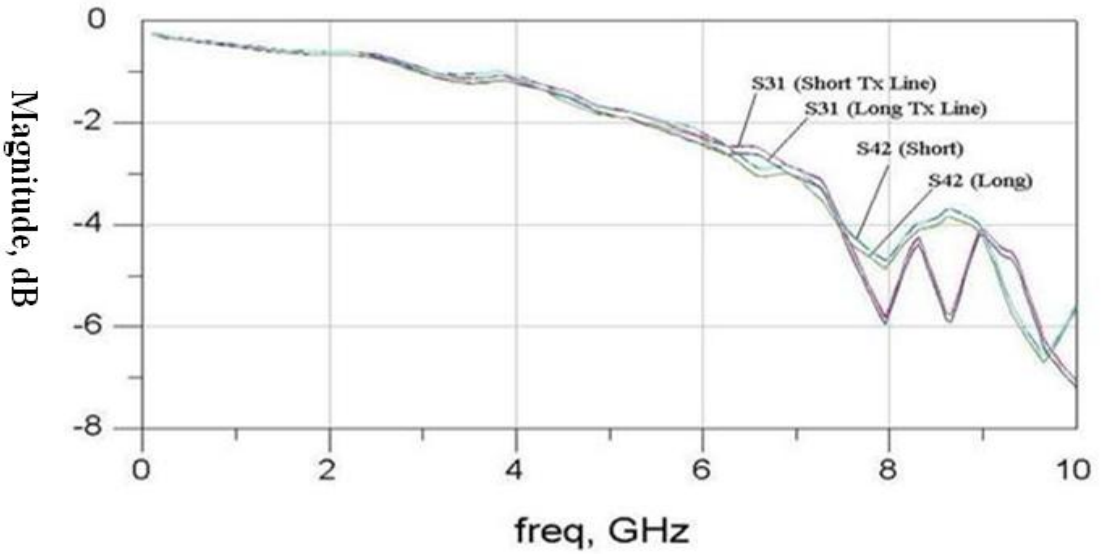


Figure 4.22: Insertion loss comparison of the system setup on different lengths of the CPW on the chip using SC as interconnects

The other variation studied involved the type of interconnects used on the chip. Figure 4.23 shows the comparison of different types of interconnects used in the system using the short CPW transmission line on the chip. Figure 4.24 shows the comparison of different types of interconnects used on the chip using the long CPW transmission line on the chip. It can again be seen that the choice of interconnect type used on the chip has little impact on the overall system performance. These interconnect structures mounted on the chip contribute little loss compared to the overall loss due to their relative small size.

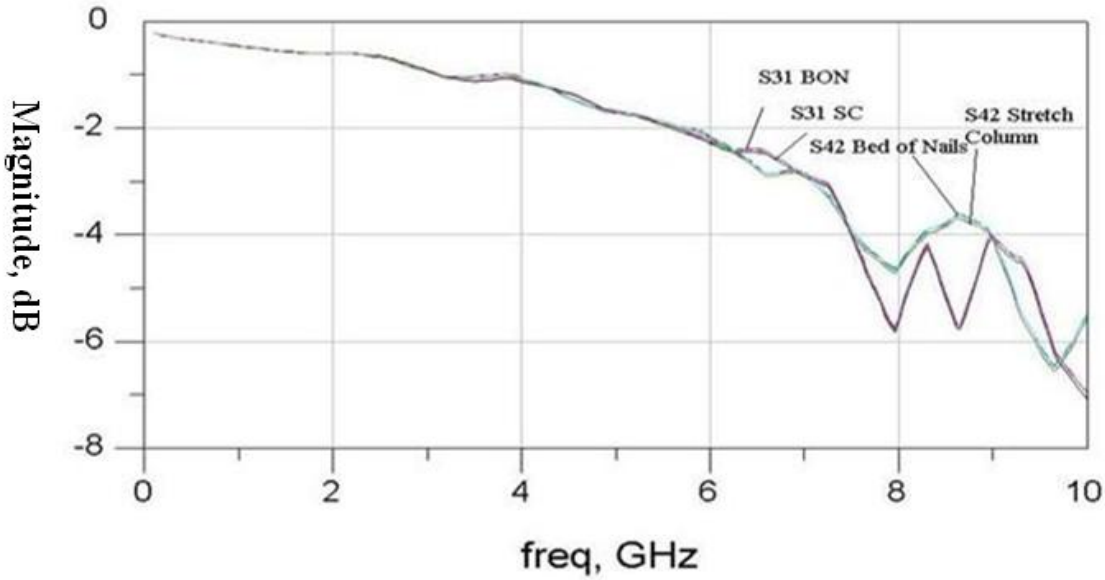


Figure 4.23: Insertion loss comparison of the system setup on different type of interconnects mounting on the chip while using the short CPW on the chip

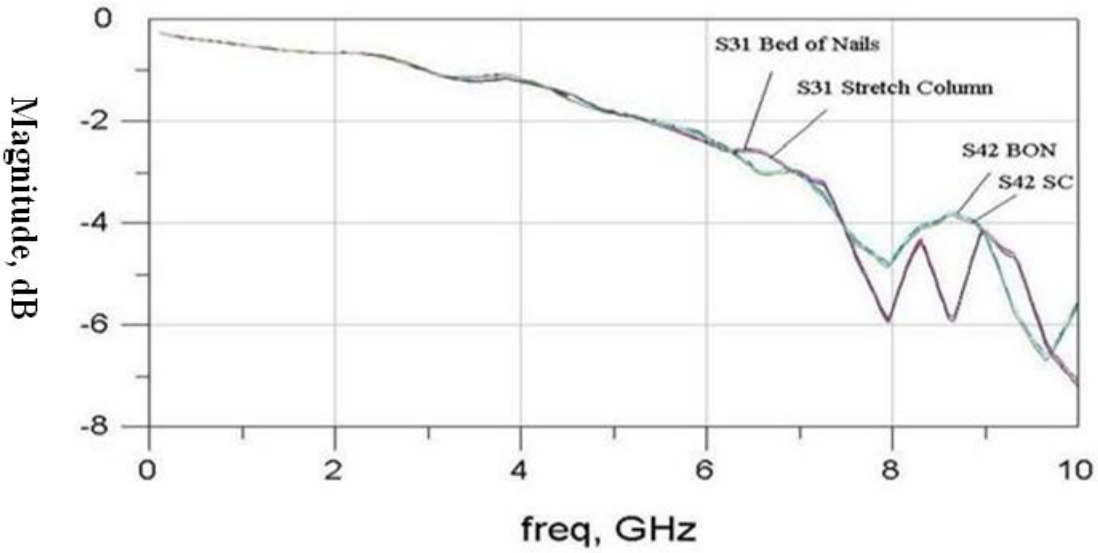


Figure 4.24: Insertion loss comparison of the system setup on different type of interconnects mounting on the chip while using the long CPW on the chip

Generally, all of these figures above show similar response in which this system model (SMA connector to DUT) has a bandwidth of 7 GHz. Beyond this frequency, the system would become lossy, which at 10 GHz, insertion loss of about 7 dB could be expected. Lastly, Figure 4.25 shows the return losses of this system model. They provide similar information in term of frequency responses as the insertion losses above, as can be seen, after 7 GHz, return losses are getting increasingly smaller (except for a dip at around 9 GHz) indicating more and more signals are reflected back.

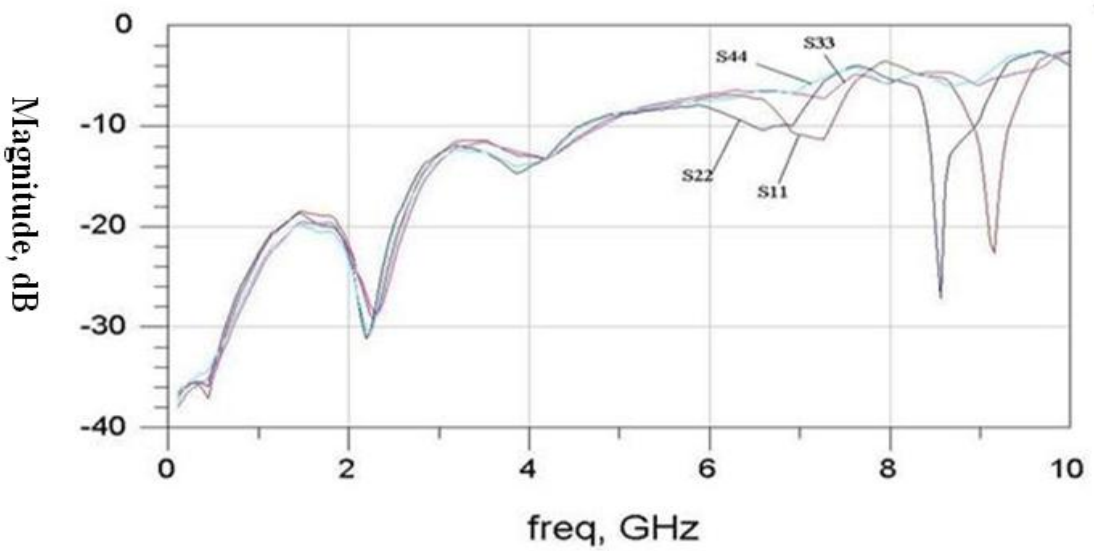


Figure 4.25: Return losses of the overall system of WLP test using the proposed elastomer based interposer

4.2.2 Measurements

Using a fabricated interposer, a functional WLP test was carried out. A vector network analyzer (VNA) HP 8750 was used for the frequency domain measurement from 35 MHz (the lower bound of VNA 8750) to 10 GHz. Measuring probes (diameter of 3.5 mm) were connected to the SMA connectors of the interposer through cables. Standard SOLT calibration was done with a 3.5 mm calibration kit.

Measurement results served as very good comparisons for the simulated data. The accuracy of the simulation models created could also be examined. There were some important assumptions made in the simulation test model. Since the overall test model is made up of cascaded models representing each of the components, the reflections and discontinuities between the interfaces of each component were not taken into consideration. In addition, it was assumed that the references of these components are aligned. Figure 4.26 shows the magnitude and phase of the insertion loss of the simulations and measurements. Only two ports were excited for the full system model,

since, as previously indicated, S31 and S42 do not differ significantly from each other.

Figure 4.27 shows the magnitude and phase of the return loss.

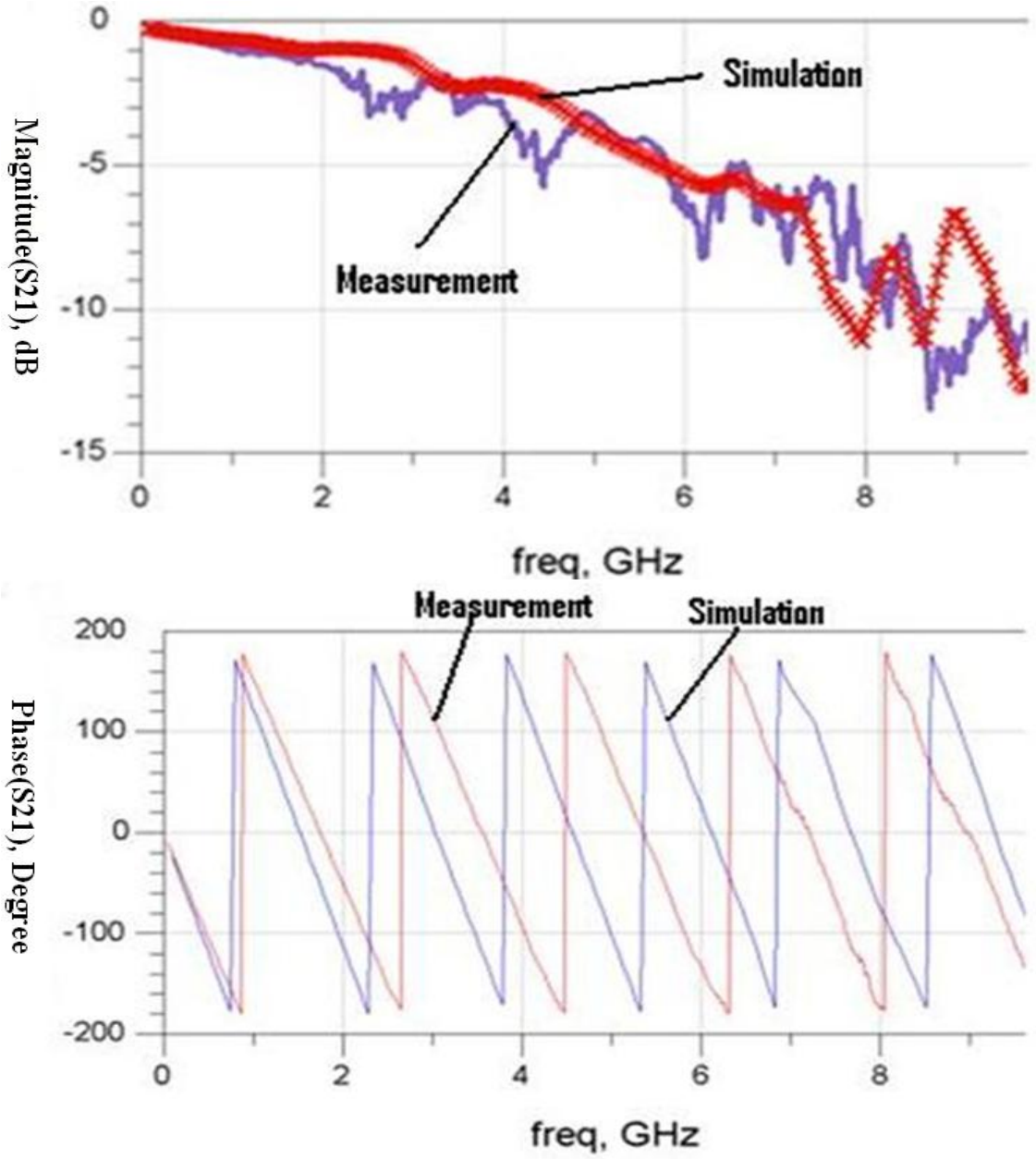


Figure 4.26: Magnitude and phase of the insertion loss comparisons between simulations and measurements results

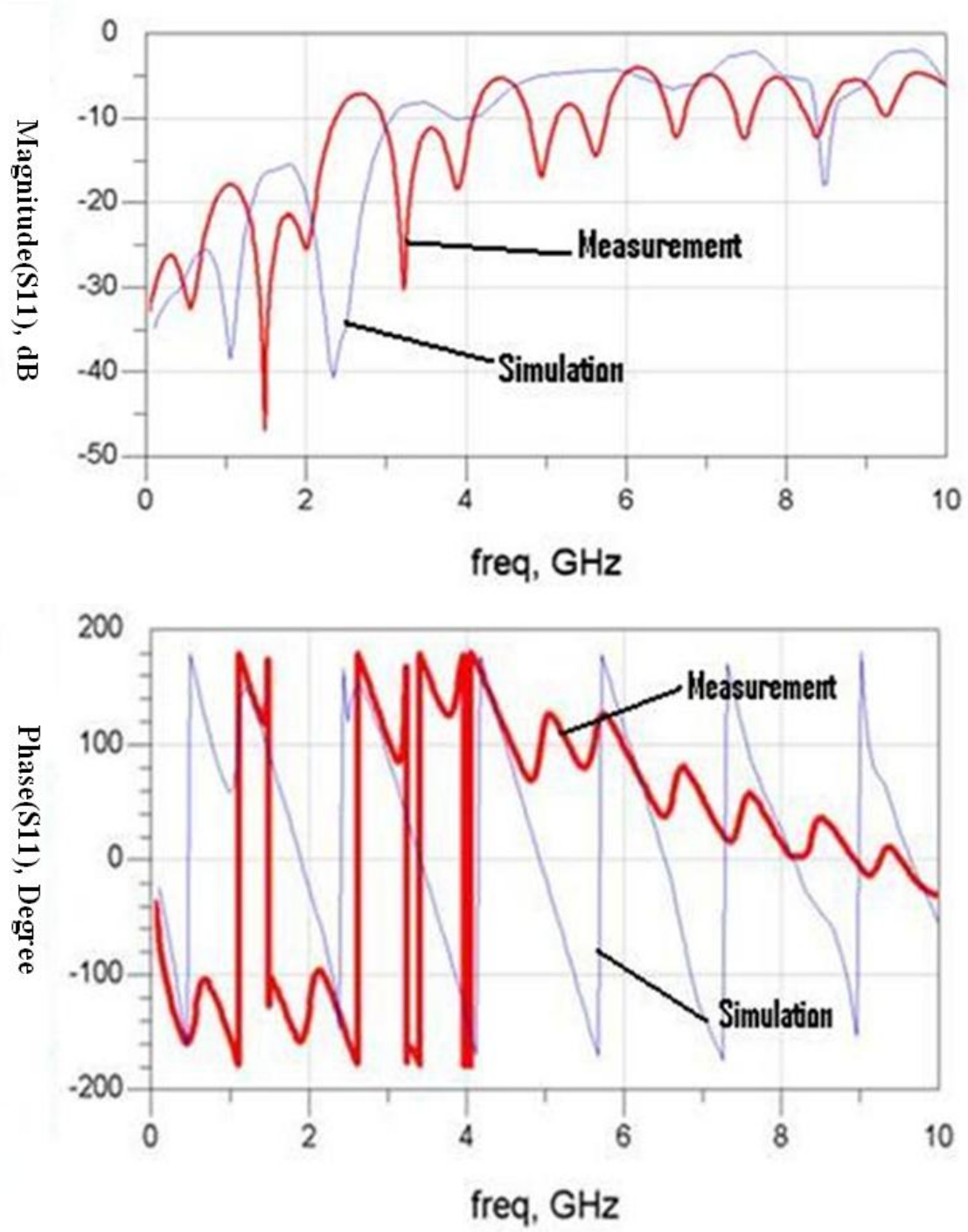


Figure 4.27: Magnitude and phase of the return loss comparisons between simulations and measurements results

As can be seen in Figure 4.26, in term of the assumptions made above, good agreement between the simulation and measurement results for the magnitude of the insertion loss is found. This shows the model created can accurately be used to predict the frequency response of the actual system. It also shows that the bandwidth of the full test system is about 5 GHz for both the actual physical system and the simulation system model. It shows that the proposed interposer meets almost all the specifications of the WLP test, except that at the target 5 GHz frequency, there is about 3 dB of insertion loss where 1-2 dB is desired.

However, some discrepancies are noted as well. A return loss of 15 dB was noted for the measurements but 5dB for the simulation system model. There are also some discrepancies of spikes and dips in the return loss frequency response. These deviations were due to the fact that the actual measurement included some noise which was not accounted for in the simulation. Apart from that, phase differences (time delay) that can be noted in these figures are mainly due to the difference in the definition of reference planes for the measurements and simulations.

4.3 Parametric Variation Study

Parametric variation of the elastomer-based interposer was studied. As described right in the beginning of the introduction of this chapter, this interposer is made up of 5 parts: the RF/SMA connector, the top layer trace (main PCB board part), the via, the bottom layer short trace and the trampoline. Therefore, in order to optimize the overall response of the interposer, the initial original designs of these parts were parametrically varied and optimized separately.

The objective was to reduce the losses experienced by the signal by at least half of the previous shown in Figure 4.26. For example, to reduce the insertion loss of 3 dB to about 1.5 dB at 5 GHz. Generally, for the proposed structure of the interposer, losses experienced by the input signal can mostly be attributed to the reflections and impedance discontinuities of the signal path and the dielectric loss. Cross talk is minimal in this case, since the distance between adjacent signals paths were great enough.

4.3.1 Variation of the SMA Connector Transition Part

Most of the time, reflections are present at the transition part of the structure. The most notable transition between the SMA connectors and the interposer board was examined first. As can be seen in the Figure 4.28, the SMA connector is perpendicular to the board. With this kind of right angle transition for the signal path, it was thought that the reflection would be improved if co-planarity between the connectors and the board could be achieved instead. Thus, simulations were carried out with new co-planarity design modeling for this transition part.

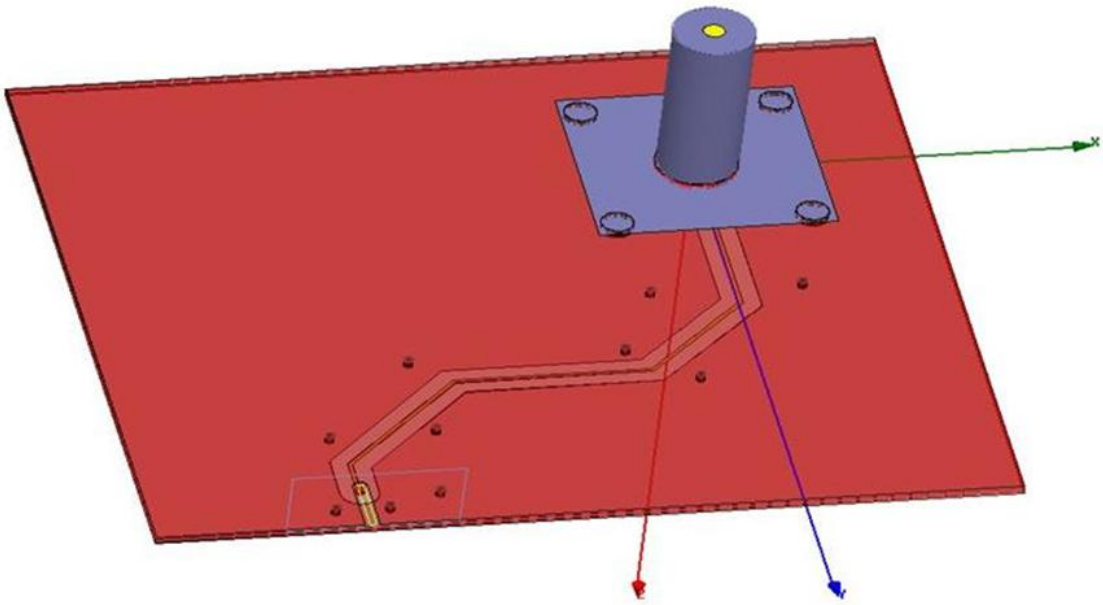


Figure 4.28: SMA connector perpendicular to the PCB board

In order to achieve co-planarity, a few different designs models for the transition were created. One of the main challenges here was to maintain the 50 Ohms impedance along the transition. Previously, the controlled impedance was achieved by having the coaxial structure along the transition.

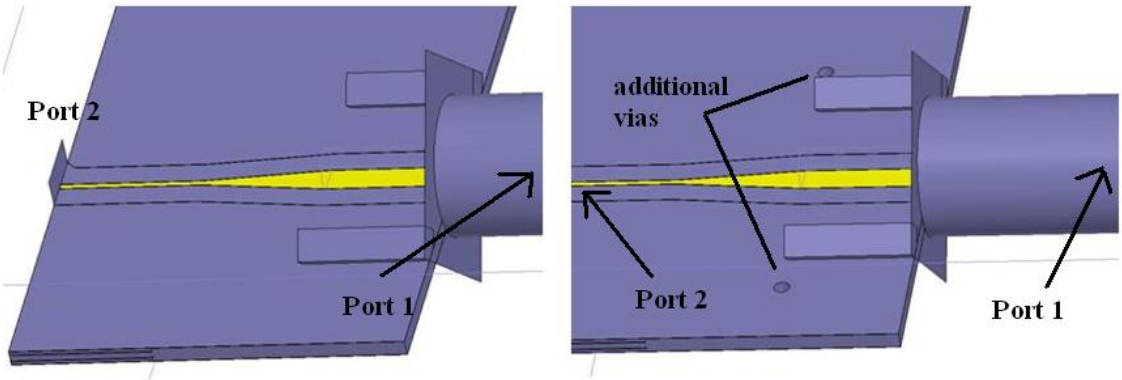


Figure 4.29: Tapered Design 1 & 2

The first two Tapered Design 1 and 2 are presented in Figure 4.29. It can be seen that the reference impedance was maintained by using coplanar waveguide (CPW) for the

transition. The difference between Tapered Design 1 and 2 are that there are two additional vias right beside the connector ground leads in Tapered Design 2. This was done to have a better guided return path for the signal. Unfortunately, simulated results showed S11 of 8 dB loss and S22 of 8 dB return loss at 6 GHz for both of the designs, indicating a considerable amount of reflections. For the following new designs, return losses S11 and S22 were studied to compare electrical performance of the different designs. In this Figure 4.29, one interesting fact is noted. For this CPW with ground design, the return path underneath showed greater influence than the coplanar return path due to the spacing. With 0.2 mm of width, the signal trace has a spacing of 0.8 mm between itself and the co-planar return path, but a mere 0.11 mm to the return path right below.

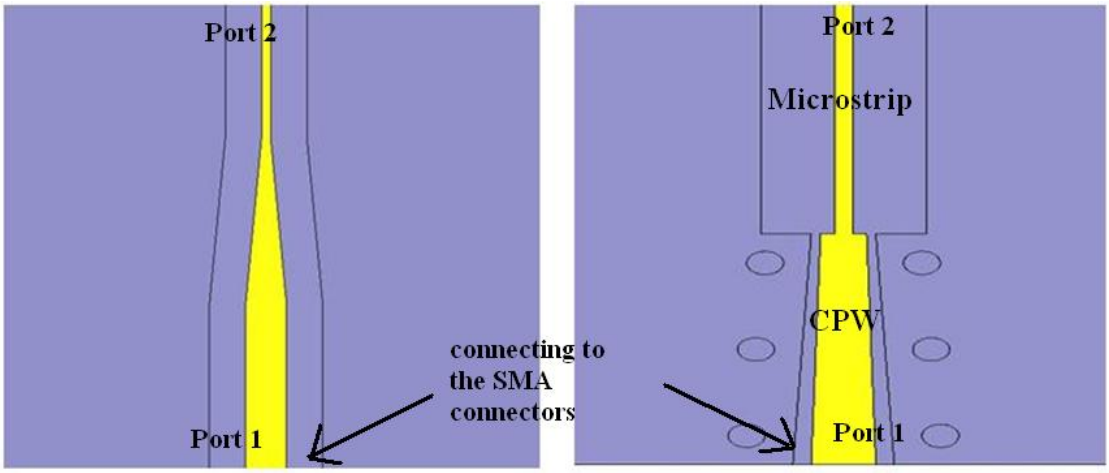


Figure 4.30: Tapered Design 3 and Step Design 1

Figure 4.30 shows the Tapered Design 3 and Step Design 1. By carefully examining the structure of Tapered Design 1, 2 and 3, it was realized that the CPW guided path needed for the transition was not achieved. The spacing between the signal and adjacent coplanar return paths on both sides was too great. Step Design 1 was designed with proper CPW

guided path implemented for the transition. The step transition was therefore tolerable, since the subsequent trace line was microstrip-like (spacing to both of coplanar return path was too great). Comparing results of these two designs in Figure 4.30, S11 improved from 11 dB of loss for the Tapered Design 3 to 27 dB for the Step Design 1. S22 improved from 12 dB of loss to 28 dB as well. However, these two simulations were done without considering the connectors first. Further studies on the step design with connector were done subsequently.

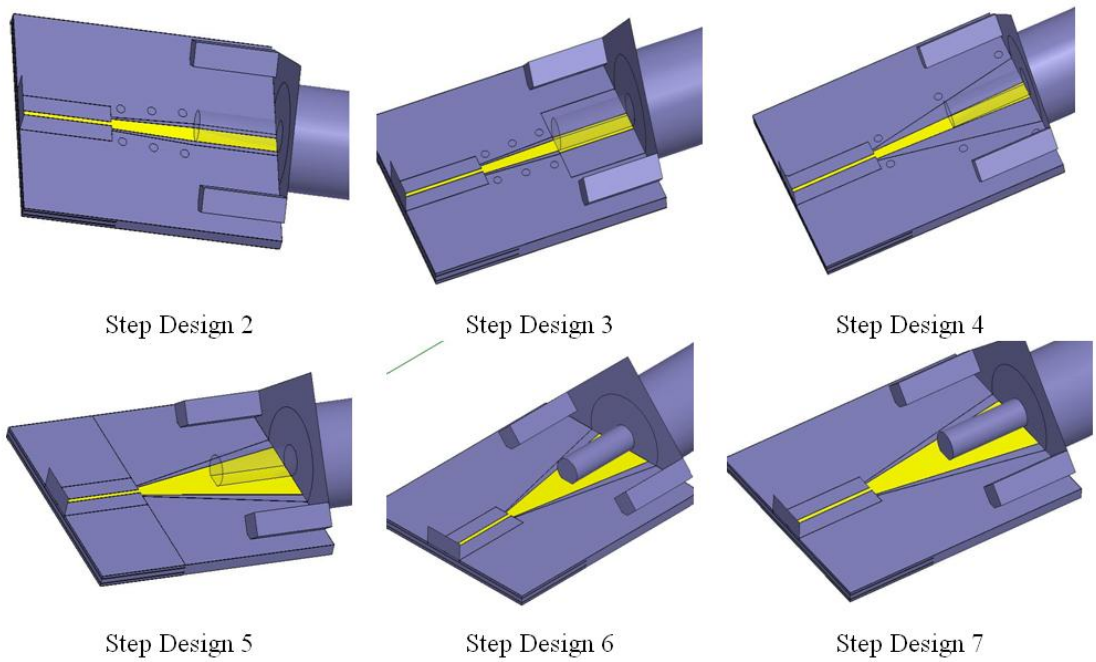


Figure 4.31: Various step designs with connectors

	S11 at 6 GHz (dB)	S22 at 6 GHz (dB)
Step Design 2	-10	-9
Step Design 3	-14.5	-13.2
Step Design 4	-13.3	-14
Step Design 5	-22	-20
Step Design 6	-29	-24
Step Design 7	-23	-20

Table 4.1: Simulated results for various step designs

Various step design models presented in Figure 4.31 were then created and simulated and their simulated results are listed in Table 4.1. Step Design 2 is actually an extension of Step Design 1, with an extended path to accommodate the signal lead of the connector. As can be seen in Table 4.1, once the connector was included, the reflections became considerably greater. Therefore, further research on the structure was done. As presented in Table 4.1, the Step Design 3 and 4 were not satisfactory. This is mainly due to the fact, again, that the co-planarity guided effect of the transition paths were not strong enough. The signal wave mode coming from the coaxial connector is perfect TEM (transverse electromagnetic). When it goes through the transition to the coplanar waveguide with ground structure, the traveling wave mode was to change to quasi-TEM. Hence, the wave has to be guided very carefully to the CPW with ground structure. It is only when the signal was properly guided by shortening the spacing between the signal and the return path on both sides of it, as in Step Design 5, 6 and 7, that satisfactory results were achieved. During this phase of design, limitations of the actual fabrication process had to be taken into consideration, such as the minimum spacing that can be achieved by the current technology while at the same time maintaining the 50 Ohms impedance level.

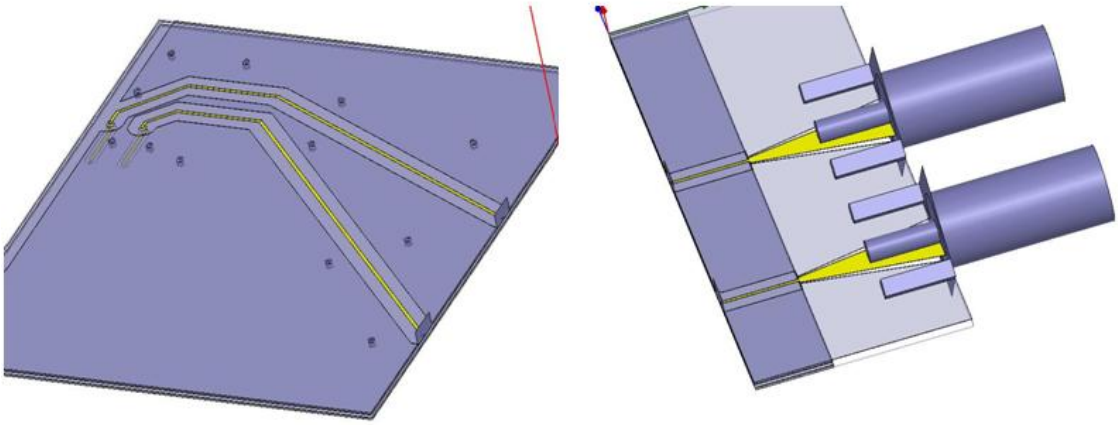


Figure 4.32: New design model for the interposer separated into two parts, the SMA connectors transition part and the rest of the structures of the interposer

Figure 4.32 shows the new design model of the interposer using the new SMA connector transition design. The best design was chosen with the lowest reflections. The model was split into two parts for faster simulation. The insertion loss comparisons between this new design and the old design are shown in Figure 4.33. It shows that this new co-planar design board actually has a slightly worse response compared the original old design. Comparing the old design to the new design without the connector part in Figure 4.33, it becomes apparent that the old SMA connector transition design with the right angle transition between the connector and the PCB board, has superior loss performance.

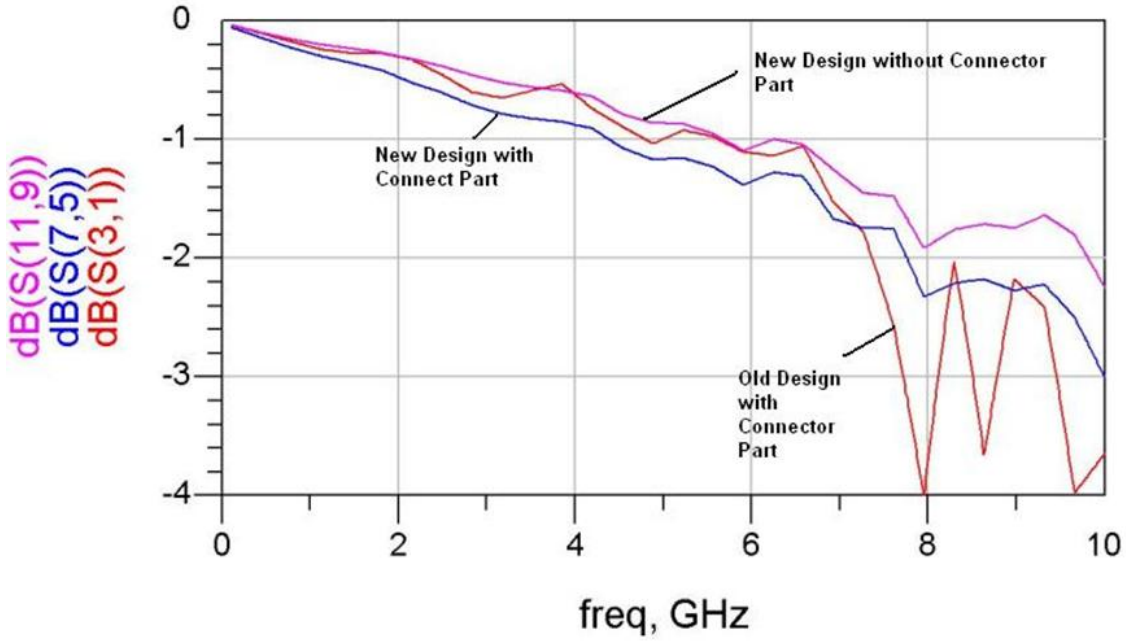


Figure 4.33: Insertion loss comparisons of new PCB board with/without connector design to old design

4.3.2 Variation of the Via Transition Part

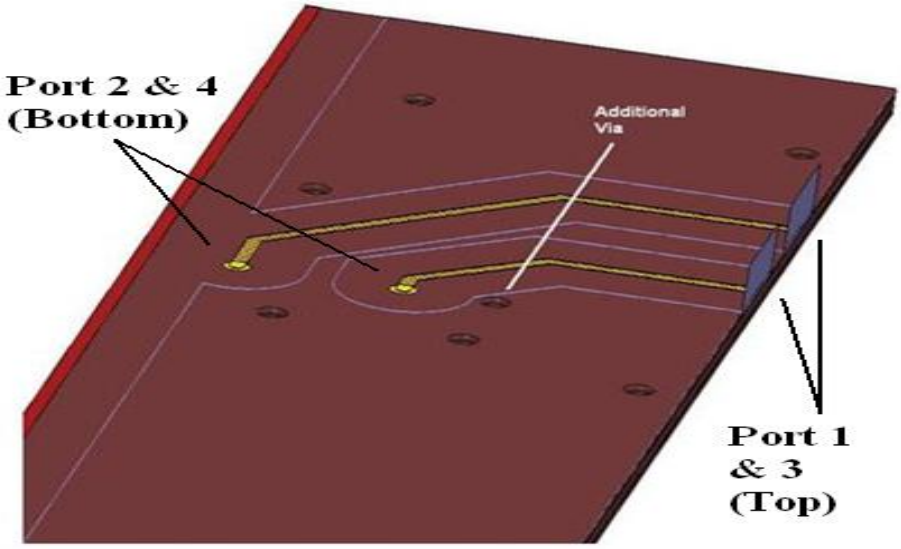


Figure 4.34: New Design 1 of the via transition part (one additional via added)

Next, variation of the via transition was attempted. This transition is bound to introduce some reflections due to the physical discontinuities. Figure 4.34 shows a new design

(New Design 1) of the via transition part. An additional via was created just beside the via transition. This additional via was created to join the four layers of metallization return path (top layer, two intermediate layers, bottom layer) as shown in Figure 4.7. Simulations were performed to see how much improvement could be obtained by joining these layers.

In addition, a second simulation model, New Design 2 was created. The model is presented in Figure 4.35. Comparing to the New Design 1, another three additional vias were introduced on the sides of the signal via transitions. The three new vias were used to join up the two intermediate return path layers only. By connecting the intermediate planes together, it was expected that the signal will "see" a more suitable impedance along the path and reduce the effect of discontinuities.

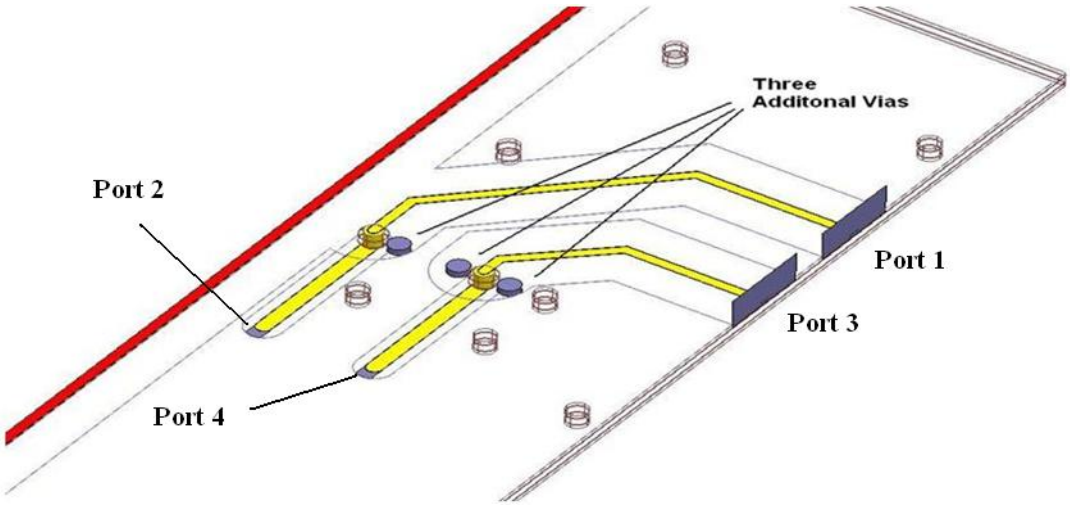


Figure 4.35: New Design 2 of the via transition

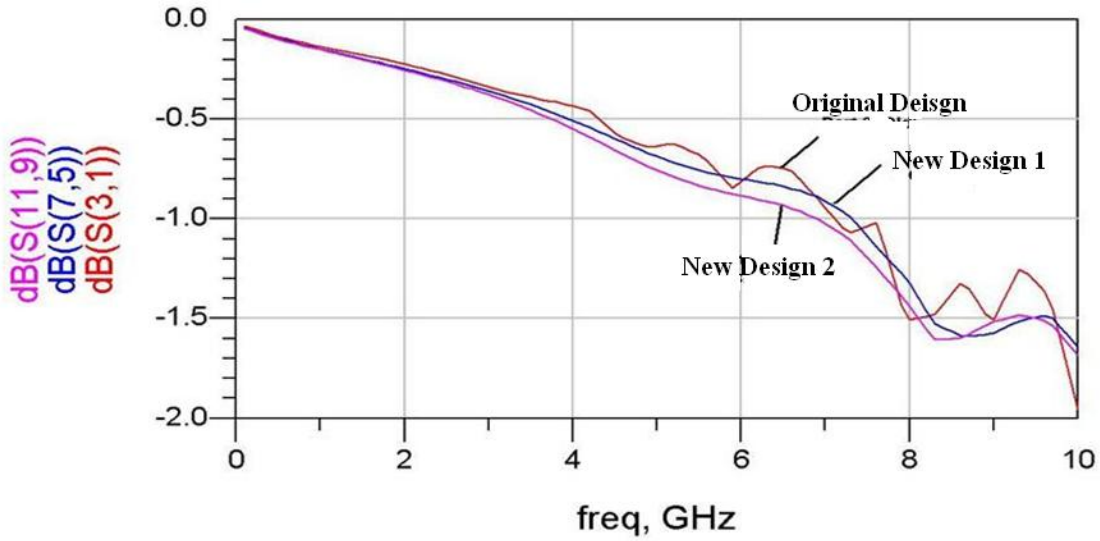


Figure 4.36: Insertion loss comparisons of different via transition part designs

The three models (original, New Design 1 and New Design 2) were then simulated. The results are given in Figure 4.36. Though in previous figures, four ports were excited, 2-port simulation results were given in this case. The other 2-port simulation results were found to be similar. It can be noted that the differences are minimal. It seemed that no significant improvement on signal integrity could be achieved without making great changes.

4.3.3 Variation of the Short Traces on the Bottom Layer

The short traces on the bottom layer of the interposer are to be connected to the trampoline structure. Some reflections could be present in this transition from the short traces to the trampoline if they are not impedance-matched.

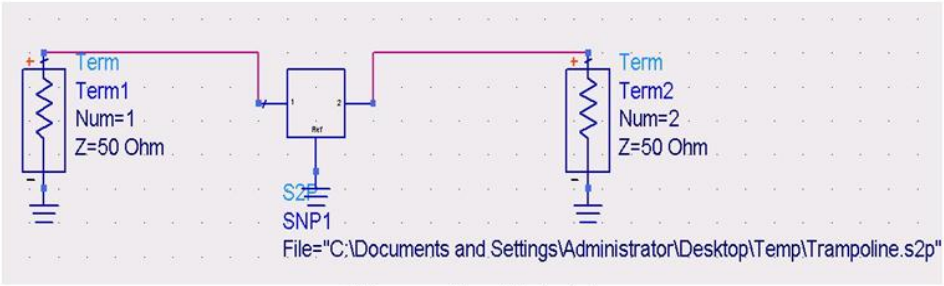
The first task was to find the impedance of the trampoline. After that, impedance of the short trace could be calculated as well. If these two impedance were found to be

mismatched, design of the short trace could be changed to minimize the signal reflections. Due to the limitations of the fabrication process, changes could only be made to the short traces, but not the trampoline. Thus, in order to study the electrical performance of the trampoline, extraction of the equivalent model of the trampoline would be useful. The trampoline structure was therefore analysed in a quasi-static numerical solver to extract the lumped RLC values. The extracted data is presented in Table 4.2.

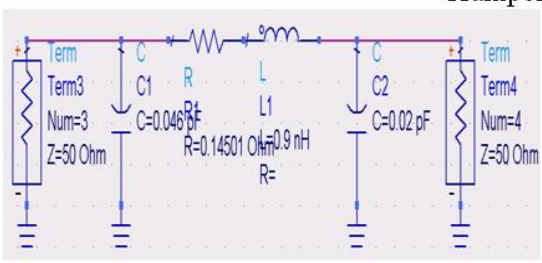
Capacitance		**Ground**	**Signal**
	Ground	0.13553 pF	- 0.043552 pF
	Signal	- 0.043552 pF	0.04673 pF
Inductance (DC)	0.92198 nH		
Inductance (AC)	0.91631 nH		
Resistance (DC)	0.14501 Ohms		
Resistance (AC)	0.038569 Ohms		

Table 4.2: RLC extraction of the trampoline (at 100 MHz)

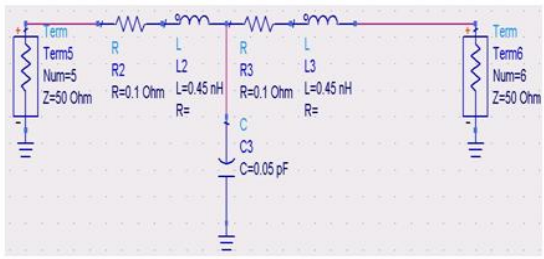
These lumped component values were used as starting values to build up an equivalent model for the trampoline. As such, two candidates, a Pi model and a T model, for the trampoline equivalent circuit were constructed and are presented in Figure 4.37. The response of the actual trampoline model in Figure 4.37 is represented by a data box carrying the simulated S-parameters taken from the full wave solver. The model of the trampoline for the full wave simulation was shown in Figure 4.15. The two excitation ports are point sources. Where specific port impedance had to be provided, a value of 50 Ω was set in the full wave simulation. Port definitions for the equivalent models shown in Figure 4.37 could consequently be set as S-parameter 50 Ω sources.



"Trampoline" Model



Equivalent Circuit 1



Equivalent Circuit 2

Figure 4.37: Trampoline model with two candidates for its equivalent circuit model (refer to Figure 4.15 for the ports notation)

The 2-port Z-parameter matrices for the Equivalent Circuit 1 (Pi Model) and the Equivalent Circuit 2 (T Model) in Figure 4.37 can be given as:

$$Z_{\Pi} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} Z_{C1} // (Z_{R1} + Z_{L1} + Z_{C2}) & \dfrac{Z_{C1} \bullet Z_{C2}}{Z_{C1} + Z_{R1} + Z_{L1} + Z_{C2}} \\ \dfrac{Z_{C1} \bullet Z_{C2}}{Z_{C1} + Z_{R1} + Z_{L1} + Z_{C2}} & Z_{C2} // (Z_{R1} + Z_{L1} + Z_{C1}) \end{bmatrix}$$

$$Z_{T} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} Z_{R2} + Z_{L2} + Z_{C3} & Z_{C3} \\ Z_{C3} & Z_{R3} + Z_{L3} + Z_{C3} \end{bmatrix}$$

respectively where $Z_A // Z_B = \dfrac{1}{\dfrac{1}{Z_A} + \dfrac{1}{Z_B}}$

A comparison of frequency response of these two equivalent circuit models to the actual trampoline response is shown in Figure 4.38.

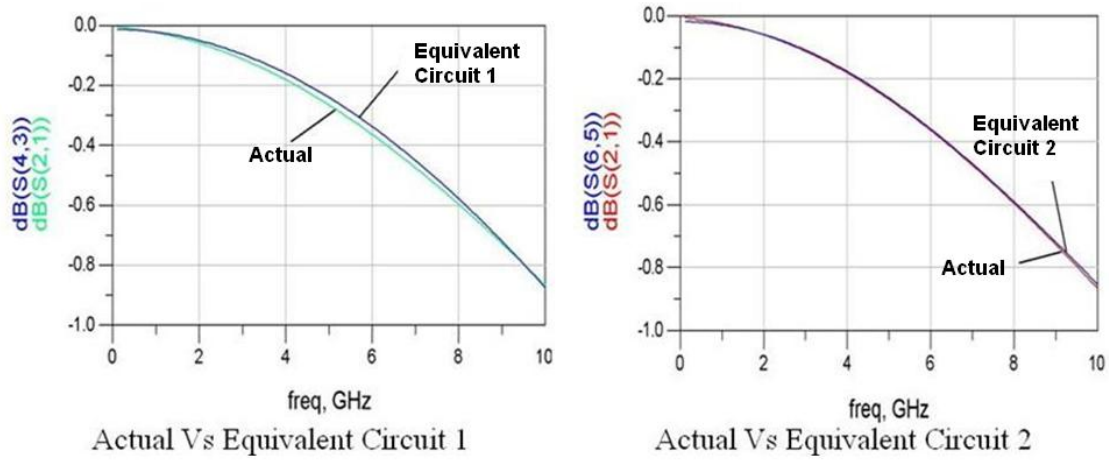
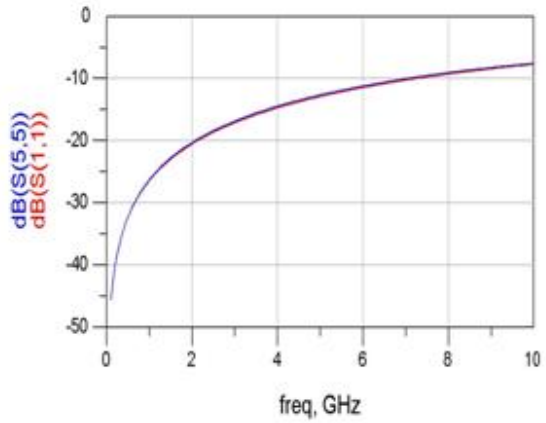
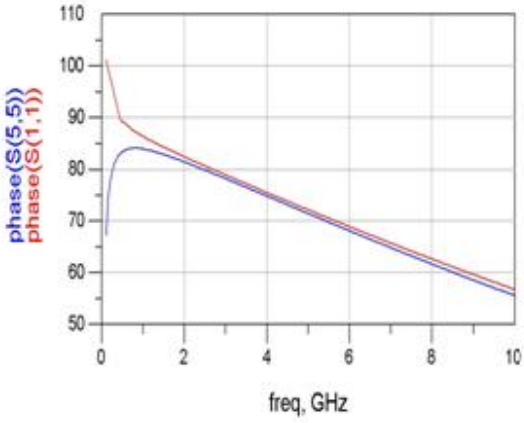


Figure 4.38: Comparisons of trampoline 3D model response to equivalent circuit models

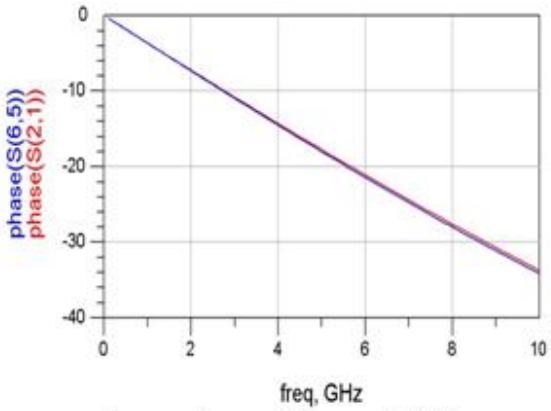
In Figure 4.38, it shows that the Equivalent Circuit 2, the T model, was a better choice. It matches the actual trampoline response closer. Further comparisons between this equivalent circuit model and the full wave simulation results (Actual) of the trampoline structure were examined. These are provided in Figure 4.39 and Figure 4.40. By looking at these comparisons, it is clear that the Equivalent Circuit 2 (the T model) is indeed a good model for the trampoline structure, since it matches all the full wave simulated responses except for a phase difference at the beginning of the frequency phase response. This is because of the difference in definitions of the ports between the HFSS model and the equivalent model (between Figure 4.15 and Figure 4.37). In Figure 4.40, port 2 was shorted to the ground to provide input impedance of the trampoline in frequency domain.



Comparison of S11



Comparison of Phase of S11



Comparison of Phase of S21

Figure 4.39: Responses comparisons of trampoline to equivalent model

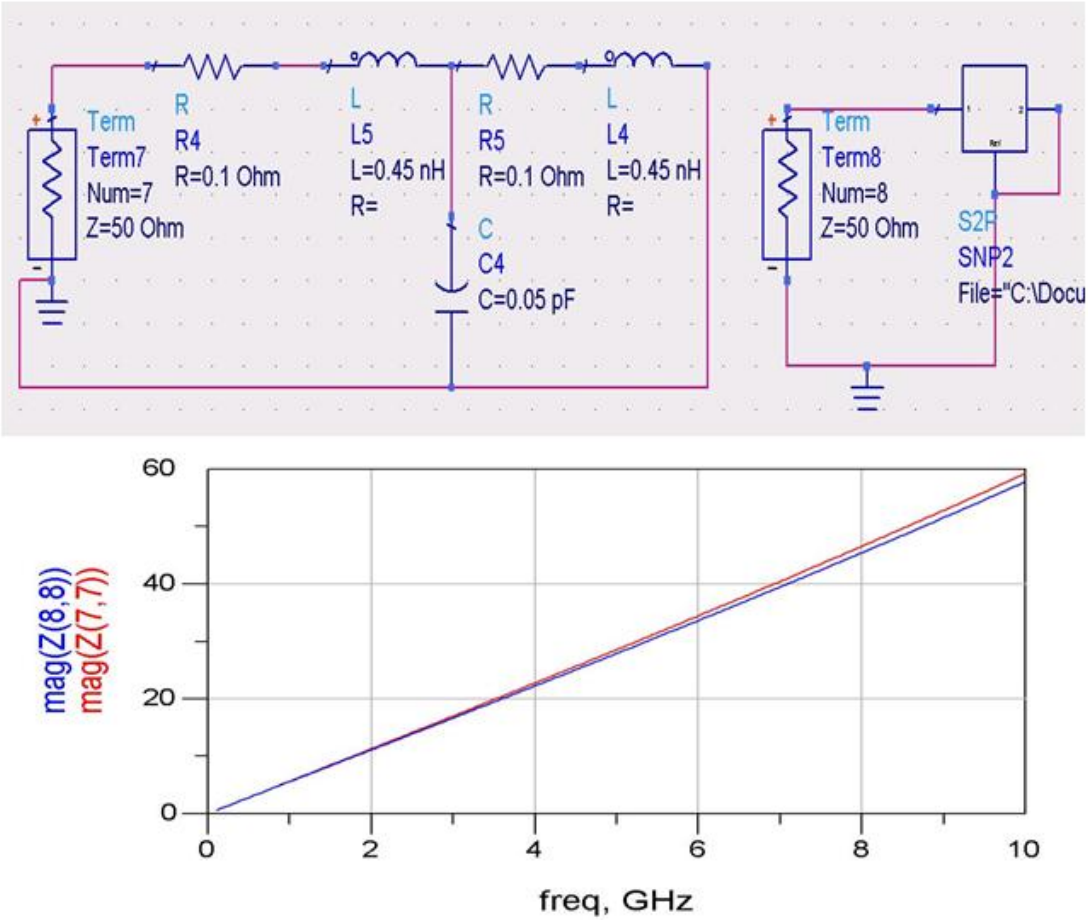


Figure 4.40: Comparison of magnitude of input impedance of trampoline to the equivalent circuit model

As depicted in Figure 4.40, the input impedance of this equivalent circuit for the trampoline can be given as:

$$Z_{11} = (Z_{R4} + Z_{L5}) + [(Z_{R5} + Z_{L4}) // Z_{C4}]$$

where $Z_A // Z_B = \dfrac{1}{\dfrac{1}{Z_A} + \dfrac{1}{Z_B}}$

Another objective of finding the equivalent circuit model for the trampoline structure was to have a better understanding of the parasitics of the structure, like the capacitance between the signal and return path.

With this equivalent circuit of the trampoline structure placed into the circuit model of the overall system of WLP test as shown in Figure 4.19, a parametric study on the values of the parasitics in the interposer structure could be performed. For example, by changing the value of the 0.05 pF capacitance formed between the signal and return path shown in the T equivalent circuit model in Figure 4.37, it could be observed whether the reflections are reduced. Quantitative studies were done and showed that if this capacitance is changed to 0.1 pF, the overall system response will improve (insertion loss reduces 0.5 dB at 5 GHz; reduces 1 dB at 10 GHz). If this is changed to 0.01 pF, the overall response will get worse (loss increases 0.5 dB at 5 GHz; loss increases 1 dB at 10 GHz).

For values for the capacitance greater than 0.05 pF, the transition from the short transmission line of the board to the trampoline structure was found to be better matched. However, this value could not be increased indefinitely, since when a value of 1 pF for the capacitance was reached, the overall system response collapsed and became very lossy at frequencies greater than 6 GHz. These effects of changing the input capacitance values are shown in Figure 4.41.

It was hence observed that signal, coming from the short transmission line of the board traveling towards the trampoline structure, is seeing an input capacitance value lying between 0.1 pF and 1 pF. Verification of this can be done readily with simple calculation by using equation:

$$C_L = 83\frac{(E_r)^{0.5}}{Z_o} \text{ pF/inch}$$

E_r (relative permittivity) is 4.4 for the BT Glass Resin, from the geometry of the short transmission line (microstrip), the characteristic impedance of the short transmission line, $Z_{o,}$ is 39 Ohms. Thus, C_L is calculated to be 4.464 pF/inch. The short transmission line has a length of 0.12205 inches, so that the overall capacitance would be 0.545 pF for this short transmission line section. When the input capacitance value of the trampoline as seen by the signal connecting to the short transmission line closer is 0.545 pF, better matching will be achieved.

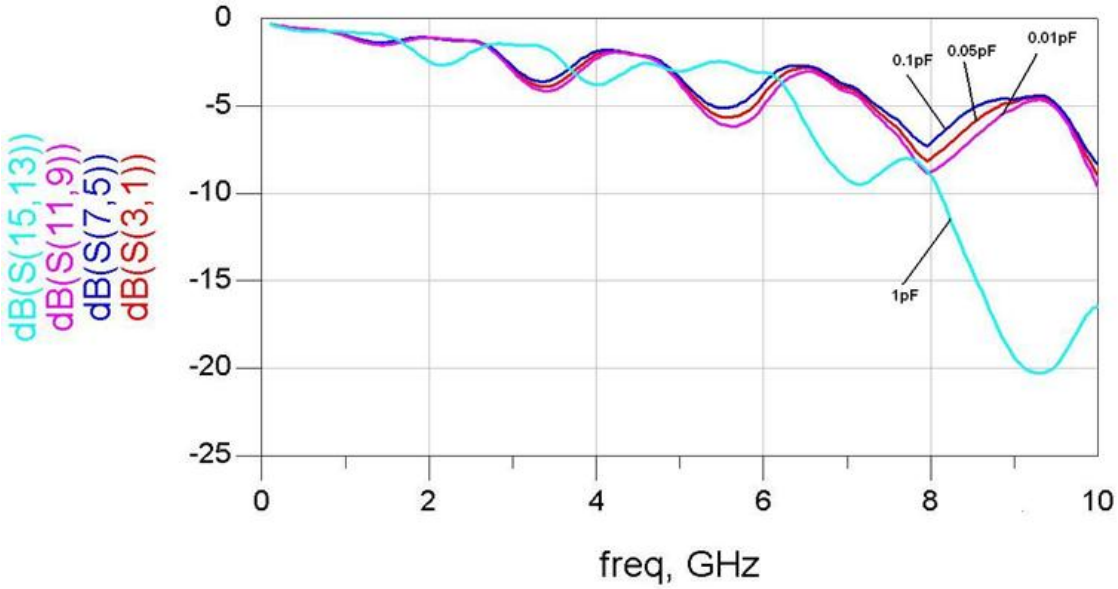


Figure 4.41: Impact on overall system insertion loss with changes made on the capacitance in the equivalent circuit model of trampoline

However, as mentioned above, changes could only be made to the short traces. The objective here was to match the impedance as seen from the trampoline's point of view as close as possible. Since it is known that the trampoline has a capacitance to ground of 0.05 pF, we tried to match that by tapering the short transmission line.

Tapering was done in order to achieve slow and gradual changes to the impedance. Two tapered designs were attempted. In the first, Design 1, the short trace was tapered from a width of 300 μm to a width of 50 μm at the connecting end to the "trampoline". In the second, Design 2, the trace was tapered from a width of 300 μm to a width of 150 μm at the connecting end to the trampoline. These two models are shown in Figure 4.42.

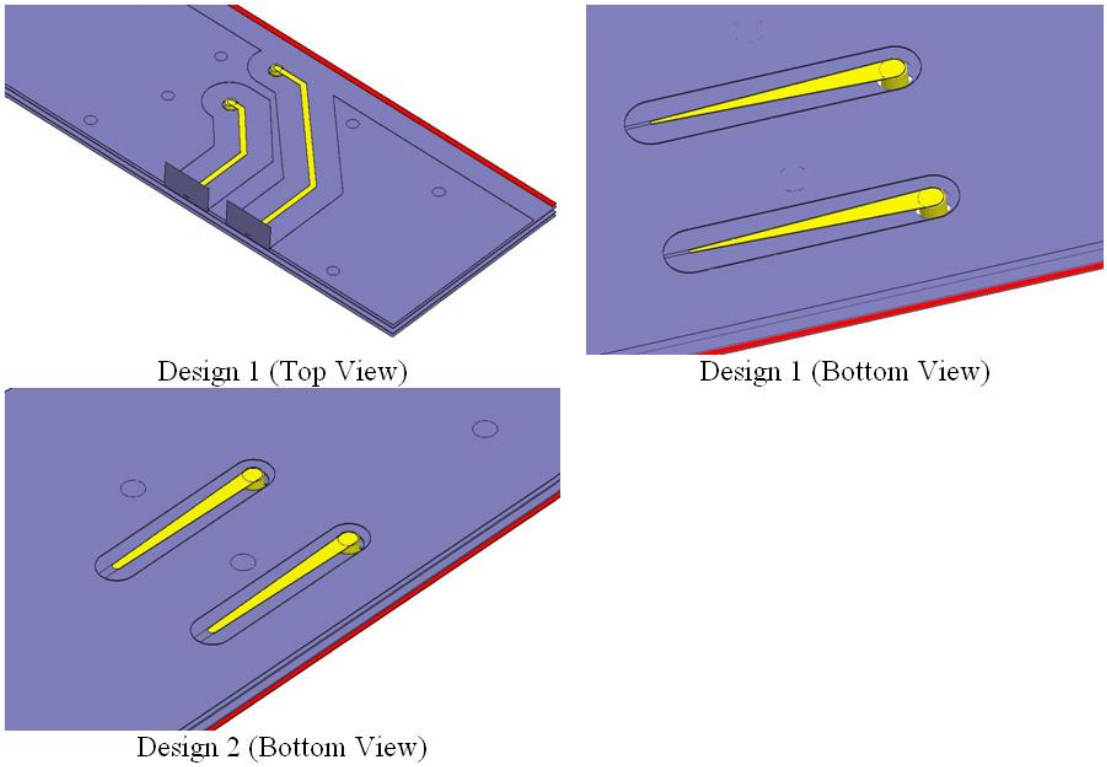


Figure 4.42: Two designs of the tapered short traces (reference can be seen in Figure 4.12)

The simulations results compared to the original are presented in Figure 4.43. As can be seen from the figure, no significant improvement was achieved by making changes to the short traces on the bottom layer of the interposer.

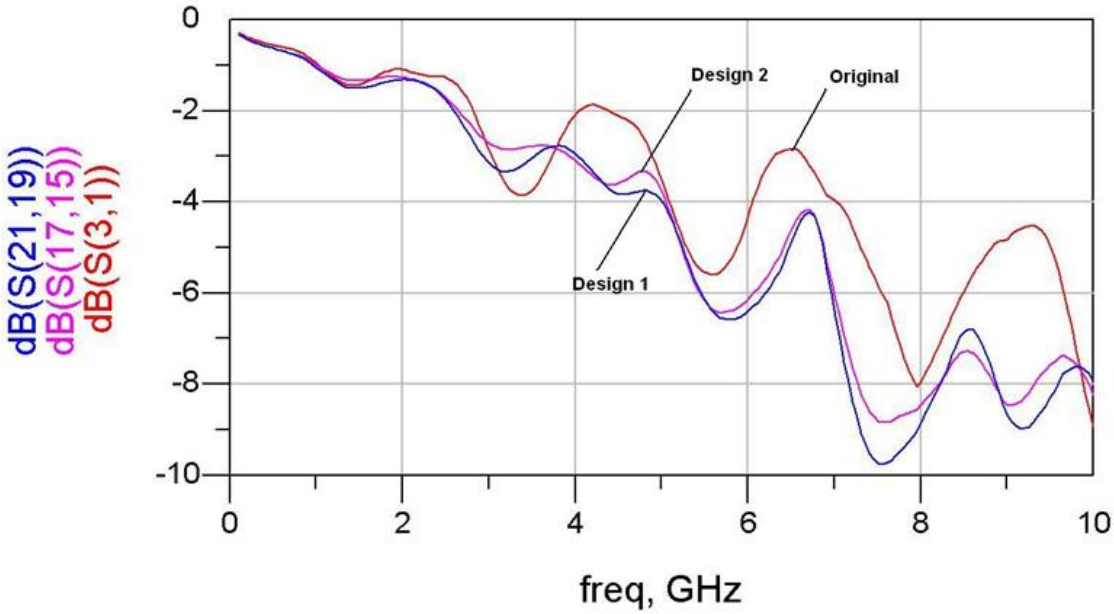


Figure 4.43: Comparisons for responses of different designs on the short traces

4.3.4 Variation of the PCB Board Part

The last part to be optimized was the PCB board of the interposer. There are only long transmission lines on the PCB board. A simulation was done to do a comparison. The response of the original interposer structure with vertical SMA connectors was compared to the new design as shown in Figure 4.31, which has coplanar SMA connectors. An additional response was added to the comparison, being the response of the new design shown in Figure 4.32 with the via transition and the bottom layer short traces taken away (only the coplanar SMA connector and the board part are left). This comparison is shown in Figure 4.44.

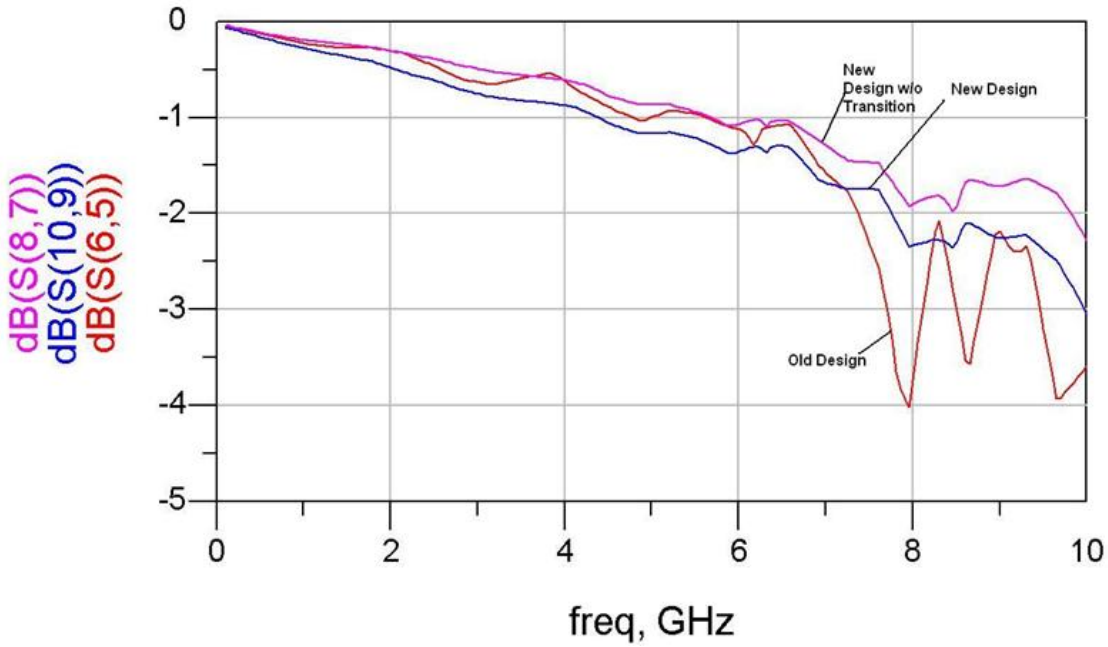


Figure 4.44: Comparison of old (original), new coplanar SMA connector design and the new coplanar SMA connector design without the via transition and the bottom layer short traces parts

As shown in Figure 4.44, the new coplanar design has a slightly worse insertion loss response than the original design, meaning that the new coplanar SMA connector would introduce only a small amount of loss. Similarly, when this new coplanar SMA connector design is compared to the same design, but without the via transition and the bottom layer short traces part, the difference is only about 0.3 dB. Combining these two findings, it was found that the three parts (SMA connector, via transition and bottom layer short traces) of the interposer do not have much impact on the overall loss mechanism. This indicates that the most dominant loss contributor is the main PCB board part with the long transmission line.

Emphasis should therefore be given to shortening these top layer transmission lines to reduce the loss experienced along these traces. An effort was made to effectively reduce

the overall size of the interposer by shortening the top layer signal traces. Figure 4.45 shows the original and shortened models. As presented in Figure 4.45, the shortened version of the interposer model has been split into two parts, the PCB board part with SMA connector and the via transition part with the bottom layer short traces part.

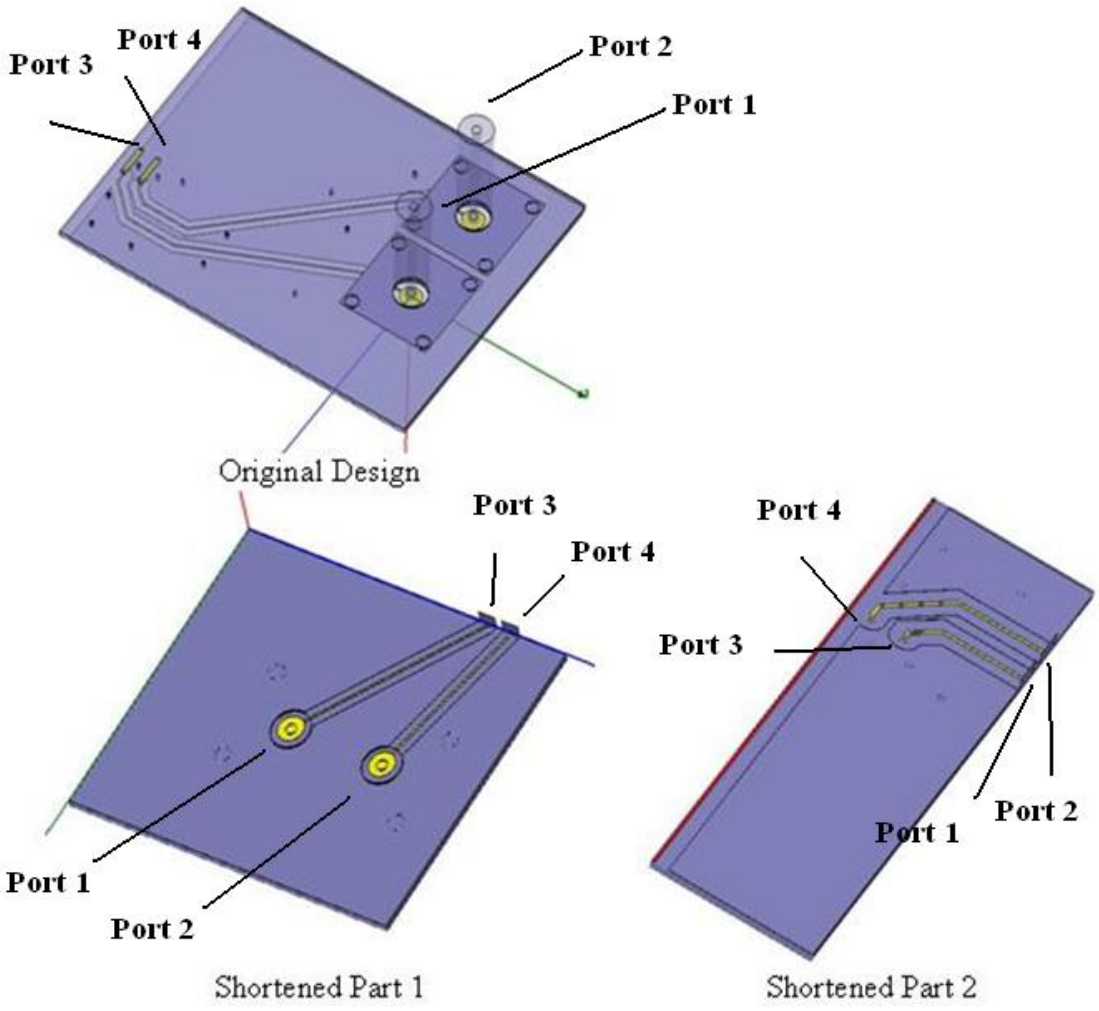


Figure 4.45: Original and shortened model

As shown in Figure 4.45, four port simulation was done. Figure 4.46 and Figure 4.47 show the insertion loss S31 and S42 respectively of the shortened version compared to the original. These two figures are superimposed in Figure 4.48, but without the SMA connector part.

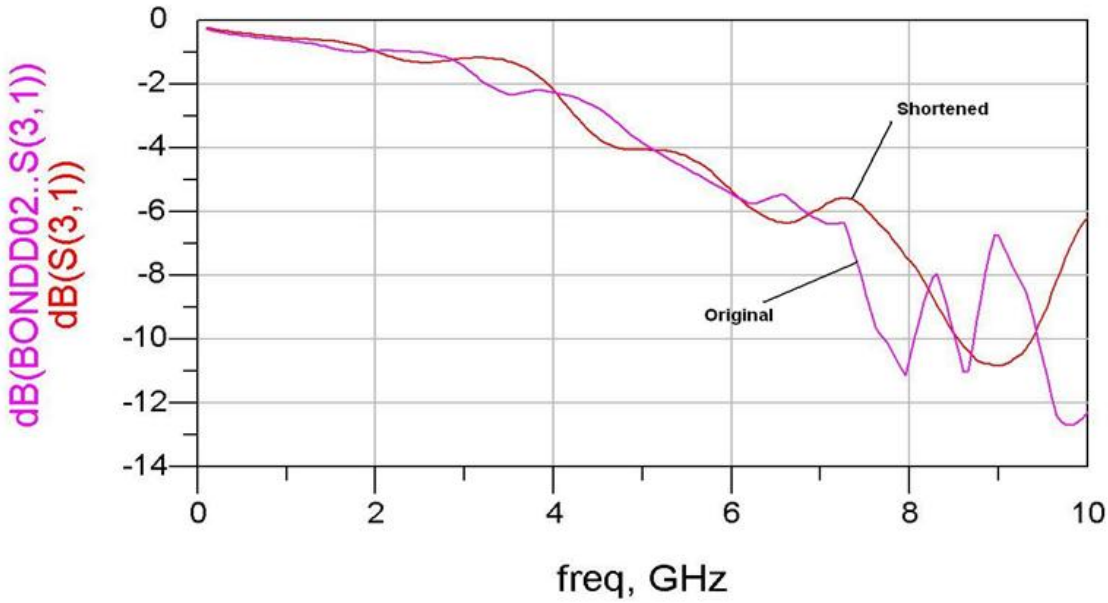


Figure 4.46: Insertion loss S31 comparison between original and shortened versions of the interposer

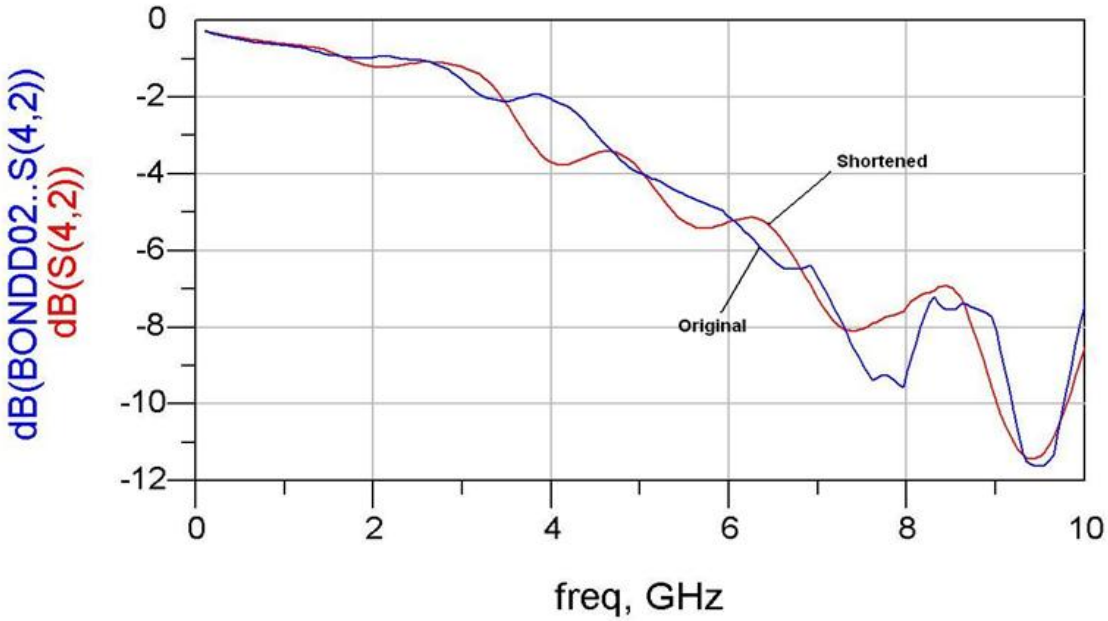


Figure 4.47: Insertion loss S42 comparison between original and shortened versions of the interposer

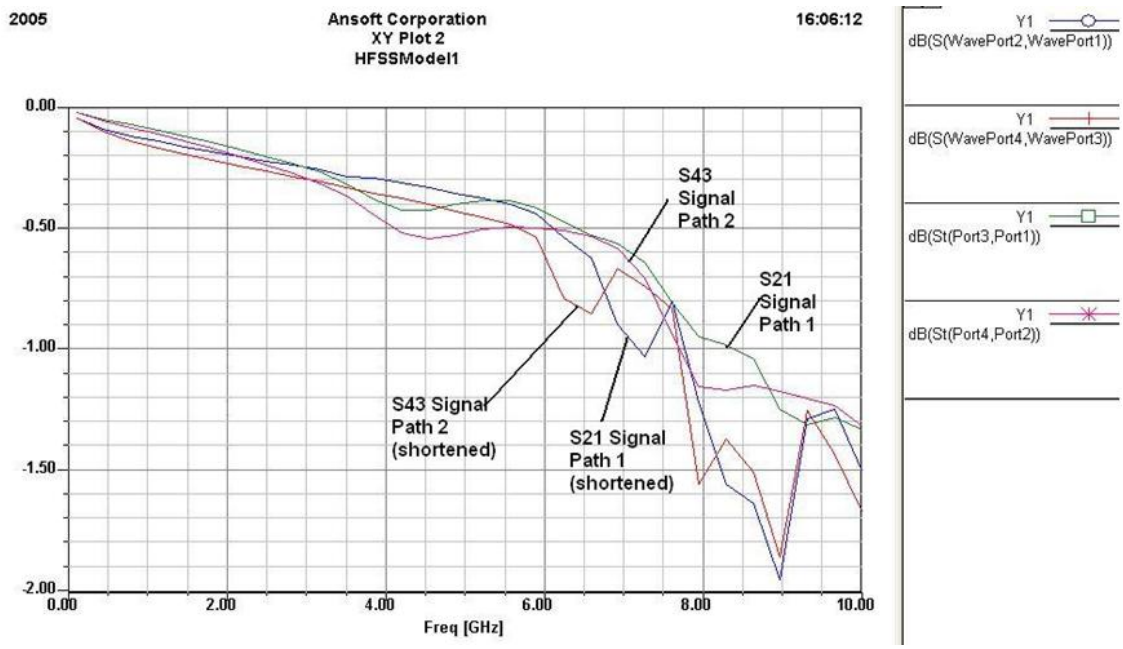


Figure 4.48: Comparison for responses of original and shortened board size of the interposer excluding the connector part

It can be readily seen that, from these three figures, minimizing the overall interposer structure was not useful. The deviations on the insertion loss are not significant. This might be due to the fact that the interposer board size has not been minimized enough. However, that was the smallest size that could be achieved, with enough space to fit in the plastic clamp structure. There is a minimum feasible size of the interposer that can be fabricated.

Finally, 2-port frequency domain measurements were carried out once again to verify that board size is the dominant loss contributor. These results are presented in Figure 4.49. The measurement was done up to 20 GHz. The interposer board response was obtained by measuring the through line on the top layer of the board as described in Figure 4.4. The other response was done in the system level, completing an I/O signal traveling trip

through the DUT. By making this comparison, it was obvious that the response of the board part of the interposer alone would make up about 75 % of the total overall loss.

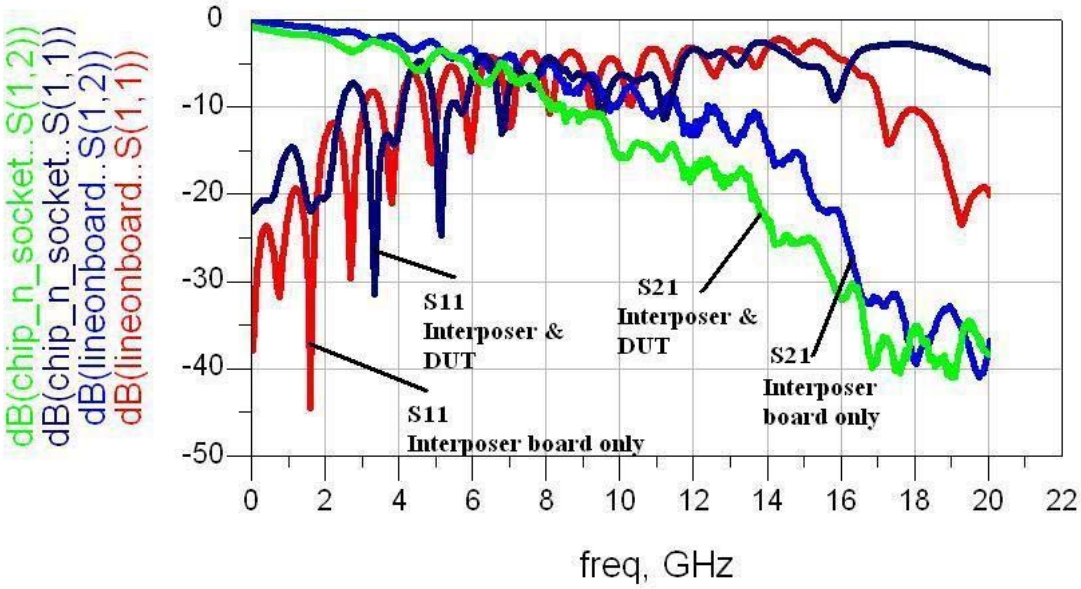


Figure 4.49: Insertion and return losses comparisons between interposer &DUT to interposer board only

4.4 Summary and Discussions

An elastomer-based interposer was successfully designed, fabricated and characterized. Good electrical performance up to a frequency of 5 GHz was achieved. Methodology of modeling the interposer was proposed and the interposer was analyzed by calculating the S-parameters. The simulation results show relatively agreement with the measurement results performed on the fabricated interposer although some disparities in the phase response due to differences in the phase reference were observed. A functional test of the fabricated interposer was carried out successfully.

The design meets the specifications. Possibilities of optimizing the performance of the interposer were carefully examined. It was found that the PCB board of the interposer has a major signal integrity issue that needs to be addressed if any enhancement of the performance were to be achieved. The PCB board was found to be making up about 75 % of the overall system loss. Shortening the overall size of the board of the interposer appeared to be one of the most essential ways of improving the high frequency response. Unfortunately, limitations on processing restricted significant improvement in this manner, since there is a limit on how small the board of the interposer could be processed. If existing limitations on fabrication could be overcome, a significant improvement on the high frequency response is anticipated. Substituting the BT resin substrate with another low loss material may also provide better high speed performance.

Chapter 5

Conclusions and Recommendations for Future Works

5.1 Conclusions

In this thesis, two novel interposers for the task of fine pitch, high speed wafer level packaged device test were designed and characterized. The elastomer-based interposer was successfully fabricated. It has a novel elastomer structure offering an innovative way of providing z-direction compliance during probing. Proper and careful design of the layout of controlled impedance lines was shown to have good high speed response which met the specification of the test. Simulations and measured data both verified the usefulness of this proposed interposer with a bandwidth of 5 GHz. Beyond this, signal degradation gets increasingly greater and reach 13 dB at 10 GHz. A functional test for this interposer was also performed. Possibilities of enhancing the high frequency response were explored. It was found and verified through simulations and measurements that the PCB board part of interposer suffers the most severe loss compared. The loss incurred on the PCB board part makes up about 75 % of the total test system loss. A viable solution of this can only be achieved through minimizing the size of the board of the interposer. However, limitation on the physical size of the board that can be

manufactured must be overcome before significant improvement of high speed response can be achieved.

In contrast to the elastomer interposer mentioned above, the MEMS-based interposer was found not to be a good candidate for the WLP (wafer level packaging) test. Novelty of the design of this interposer lies in the use of unique MEMS contacts to provide the vertical compliance during wafer probing proposed. Geometrically, it meets the fine pitch, high density and high pin count requirements of the test. However, after proper electrical characterization of the interposer had been done, it was observed that this interposer has severe signal integrity issue that needed to be addressed for high frequency application. It has bandwidth of only 1 GHz and encounters 20 dB of loss at 10 GHz. Optimizations through variations on the design were explored, but due to the constraints of material properties and fabrication limitations, this interposer could not be realized.

5.2 Recommendations for Future Works

A high-speed testing interface for WLP of 100 microns pitch is feasible and can be realized, but the work is far from being done. Further developments on this work could include:

1. Using the current prototype interposer, work on integrating it with the test support processor (TSP) and performing functional testing of the WLP chips could be considered. Prospective test vehicles together with a proper test strategy have been suggested [3].

2. Demonstrating the elastomer interposer concept for a full wafer testing. Full installation of Stretched Solder Column or Bed of Nails interconnects mounted on top of the complete wafer can be implemented. One of the challenges would be to ensure minimum defects of this large amount of interconnects. High density and fine pitch probing could then be demonstrated with elastomer interposer capable of accommodating all these interconnects concurrently.
3. Smaller board size of the prototype interposer could be achieved coupled with better material selection of the dielectrics substrate used. Brand new topology of the layout on the top layer traces might be needed to create controlled impedance lines. Potential candidates could be Teflon and high density dielectrics.
4. For the MEMS based interposer, better compromise on mechanical and electrical aspects could be made. The idea of having MEMS contacts for the compliance is worthwhile to explore further. A new design consisting most of the important features of this interposer could be explored and characterized. It can then be fabricated and undergo functional testing.
5. New modeling techniques and methodologies for modeling these interposers could be explored in order to produce simulation results with good accuracy. Test models that can incorporate all the reflections and discontinuities between the interfaces of the components parts of the test setup would be most useful.

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