# LOW POWER LOW NOISE ANALOG FRONT-END IC DESIGN FOR BIOMEDICAL SENSOR INTERFACE

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*"Few people are successful unless a lot of other people want them to be"*

— Charles Brower

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# SUMMARY

In the ageing society, the focus of the future healthcare services is moving from treatment to prevention. The traditional hospital-centric medical system lacks the resources and flexibility to adapt to the desired transformation. Wearable health monitoring system is a possible solution to build the prevention-oriented, consumer-driven model for future healthcare system. This calls for the development of the intelligent biomedical sensor nodes for continuous health monitoring. This thesis presents the design of the low power low noise analog front-end IC for biomedical sensor interface.

Power consumption is one of the most important considerations in wearable biomedical sensor interface design. In this research, we have developed a cross-domain optimization technique that balances the power consumption between analog and digital blocks. The technique was applied to the design of several sensor interface chips, which include a 445nW fully integrated programmable ECG chip, a 32-channel 22μW implantable EEG chip and a 16-channel 60μW neural recording chip. The outstanding performances of these chips verify the developed algorithm successfully, which provides an effective and optimal approach to achieve high power efficiency for biomedical sensor interface design.

In the design of biomedical sensor interface, the input referred noise of the front-end amplifier must be as low as possible in order to detect the weak biopotential signals. The trade-off between noise and power becomes very important. Based on the

proposed cross-domain power optimization technique, low noise front-end amplifiers developed in this design achieve low noise efficiency factor (NEF) from 2.16 to 3.26, which are among the lowest numbers reported to date. MOS-bipolar active pseudo-resistor structure has been widely adopted in biomedical amplifiers to realize the ultra low high-pass cut-off frequency. The existing pseudo-resistor structure exhibits unbalanced electrical property and induces serious DC level shift, which make it not suitable for low voltage operation. A fully balanced tunable pseudo-resistor structure was proposed in this project. Employing the proposed pseudo-resistor, the amplifier achieved a THD of 0.6% at rail-to-rail output swing, providing a reliable solution for low voltage operation.

Multi-channel recording is essential for many biomedical applications. A large number of recording channels impose more rigid requirement for chip area. An innovative system architecture was proposed, which solved the dilemma among the system bandwidth, input referred noise and chip area. Employing the proposed system architecture, more than 50% chip area was saved compared to the existing design. Furthermore, this system architecture facilitates the system power optimization. The average power per channel of this design is only 3% of the recently published multi-channel recording IC.

All of the presented designs were fabricated and their functionalities were verified by the measurement results. The performances of these prototypes were reported in Journal of Solid-State Circuits (JSSC), International Solid-State Circuits Conference (ISSCC) 2010, Custom Integrated Circuits Conference (CICC) 2009, and Symposium on VLSI Circuits 2008, etc.

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# LIST OF ABBREVIATIONS

| | |
|---|---|
| AAP | Axon Action Potential |
| ADC | Analog to Digital Converter |
| BJT | Bipolar Junction Transistors |
| CMRR | Common Mode Rejection Ratio |
| ECG | Electrocardiograph |
| EEG | Electroencephalograph |
| EMG | Electromyography |
| EOG | Electrooculography |
| LSB | Least Significant Bit |
| NEF | Noise Efficiency Factor |
| OTA | Operational Transconductance Amplifier |
| PGA | Programmable Gain Amplifier |
| PSRR | Power Supply Rejection Ratio |
| SAR | Successive Approximation Register |
| SNR | Signal to Noise Ratio |
| S/H | Sample and Hold |
| TB-FEA | Tunable Bandwidth Front-End Amplifier |
| THD | Total Harmonic Distortion |
| WBAN | Wireless Body Area Network |

# CHAPTER 1

# INTRODUCTION

## 1.1 Background

With the development of the modern society, people become more and more health conscious. The focus of the future health services will be more in prevention rather than treatment. However, the traditional healthcare system requires patients to visit hospital on a regular basis for early detection of diseases, as hospitals and physicians are the major sources of medical diagnosis and treatment. This kind of hospital-centric healthcare system faces many difficulties to facilitate the prevention oriented healthcare model [1]. First of all, the increase in the ageing population demands larger number of physicians, nurses and medical appliances. Some may need twenty-four hour constant medical support, resulting in overcrowding and bed blocking in hospital. Second, patients with chronic disease such as hypertension, diabetes and heart disease may need to record their health condition everyday for more effective treatment. Going to hospital frequently obviously brings many inconveniences such as time wasting on travelling and queuing. Third, the self-inflicted diseases caused by improper diet, inadequate exercise and other unhealthy habits are increasing, especially among the young generation working under high pressure. This situation calls for continuous medical monitoring to keep people aware of health condition and guide one's diet and lifestyle to prevent these diseases, rather than seeking treatment after a symptom develops. In addition, people desire improved healthcare quality with

lower cost. Therefore, there is an increasing demand for more efficient and responsive individual-centric healthcare services [2].

Wearable health monitoring devices integrated into a telemedicine system is a possible solution to build the prevention-oriented, consumer-driven model for healthcare system. Wireless transmission of the recorded biomedical signals is necessary, as unwieldy wires between sensors and processing unit will severely limit the patient's movement and level of comfort, especially for diagnosis requiring long time continuous recording. The converging of bioengineering, nanotechnologies, computers, and communications opens the door for integration of biomedical sensor devices, signal processing unit, and wireless communication channel into a single chip, which leads to the introduction of wearable wireless biomedical sensor devices. A collection of these wearable wireless biomedical sensor devices forms the base of a wireless body area network (WBAN). WBAN together with the personal sever and remote healthcare servers form the complete wireless health monitoring system.

The general overview of the wireless health monitoring system architecture is shown in Figure 1.1 [3]. There are basically three levels in the overall system. The first level consists of a set of intelligent physiological sensors depending on the end-user application, such as ECG sensor, blood pressure sensor, motion sensor, etc [4]. The interested biological signals are captured by these sensors and converted to digital format for easy processing in the later stages. Through WBAN, these sensors are interfaced to standard wireless platforms that provide computational, storage and communication capabilities. The network nodes of WBAN continuously collect and process the raw data from these sensors, store them locally, and send them

periodically to the personal server, which is the second level of the wireless health monitoring system.

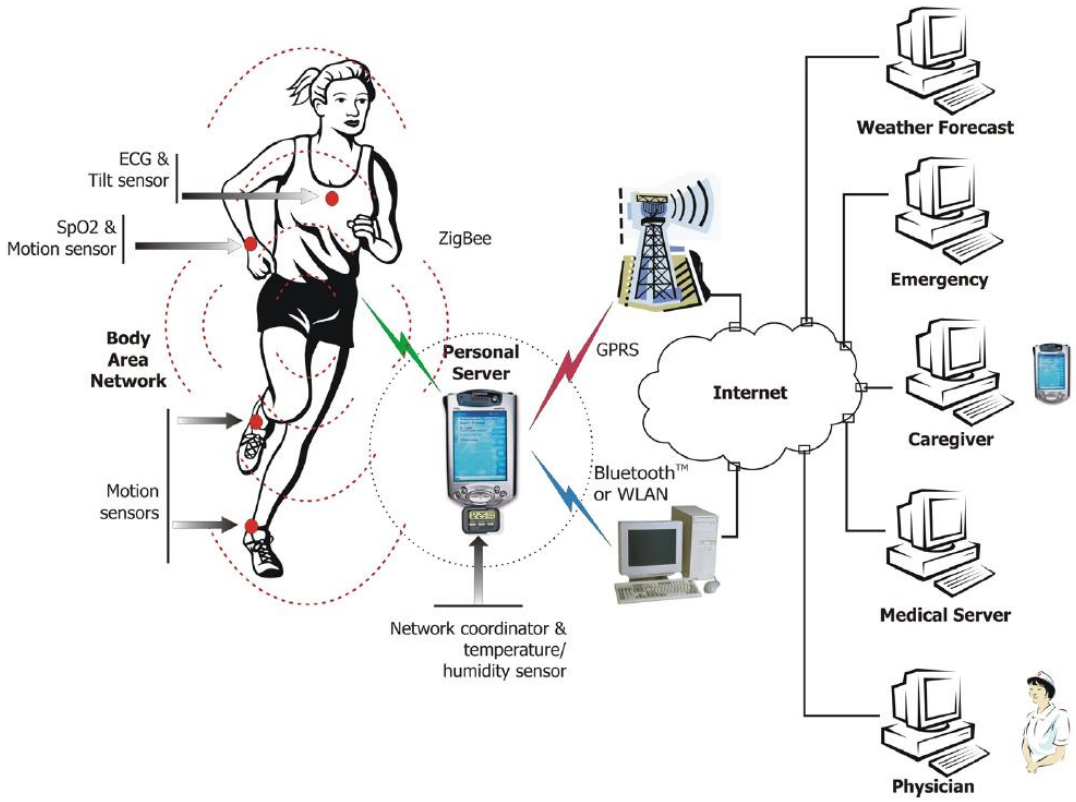


Figure 1.1. Generalized overview of the wireless wearable health monitoring system architecture [3].

The personal server is usually run on a PDA, or a cell phone, or a personal computer. The main function of the personal server is to receive and process biological data from the intelligent sensors. It also acts as a controller to configure and monitor the WBAN nodes and integrate the data from various physiological sensors for better insight into the user's health condition. Some simple decisions can be made by the personal server and early warning or guidance may be generated based on the processing results. Another function of the personal server is to communicate with the remote upper-level healthcare services using internet services.

The top level in the system is the healthcare provider, which collects data automatically from individual patient. The information of each patient is processed, analyzed and integrated into a patient's medical record. Medical professionals can monitor the health condition of the patient and issue recommendations based on the collected biological data. If the received data indicates an imminent medical condition, emergency service will be activated for immediate treatment. Another benefit is that the stored data can be used for research purpose without spending any time on collecting samples.

## 1.2 Motivation

As stated in the background section, the wireless health monitoring system makes the prevention-oriented, consumer-driven healthcare model possible. The physiological sensors of WBAN provide continuous monitoring of the patient's vital signals at home. Seamless connections between patients and doctors are built, and timely feedback on patients' health condition can be provided to aid the early detection of abnormal conditions. The healthcare services available online reduces unnecessary duplicate examinations and waiting queues at hospital and the physicians delivery their professional advices at the point of need. This kind of healthcare system gives great benefit and convenience to doctors, patients with chronic diseases, elderly people and rehabilitant. Young people can also employ the WBAN of physiological sensors to monitor their health condition and use the widely available medical information online to alter their unhealthy lifestyle and diet. The WBAN of physiological sensors integrated into the telemedicine has the potential to provide higher quality healthcare with less medical cost, hence to improve the quality of life.

It is envisaged that the WBAN will revolutionize the hospital, homecare, and personal health systems and establish a prevention-oriented, consumer-driven model for health care. These advantages of the WBAN motivate researchers world-wide to develop the wireless health monitoring system.

## 1.3 Research Objectives and Contributions

One of the most challenging tasks to develop the wireless health monitoring system is the physiological sensor design. To be worn everyday, these sensors must be designed to provide greatest comfort to the wearers. Since the target users are not limited to stationary patients in hospital beds, the sensors should be designed with light weight and compact size to minimize its effect on people's daily life. As a result, battery operation is necessary and ultra low power design is critical to lengthen the battery lifetime. Meanwhile, these sensors might be worn in the unconstrained ambulatory environment, hence high detection accuracies and stable performances are very important. One essential module in these physiological sensors is the sensor interface IC. It is responsible for the amplification, filtering and digitization of the captured biological signals before further digital signal processing works. The performance of the overall system relies on the performance of the sensor interface IC since it locates at the most front end of the system.

### 1.3.1 Research Objectives

The objective of this project is to develop the analog front-end circuits for the biomedical sensor interface to improve its performance and comfort for person under monitoring. The primary goals of this project include the followings:

A. To develop the low power system architecture for the analog front-end circuits of the biomedical sensor interface IC. Power distribution among each functional block should be carefully plotted to achieve high power efficiency. The total power dissipation of the overall system should be within 1 μW under battery supply.

B. To design each individual circuit block for the low noise, low power analog front-end to achieve the functions of amplification and filtering. The performance of each module needs to meet the design requirements according to different applications. They may include front-end amplifier, programmable gain amplifier (PGA), filters, and reference generator.

C. The overall system is required to take as small area as possible. Full integration of the overall system is necessary and any external components should be avoided to minimize the size of the physiological sensors.

D. To develop multi-channel analog front-end for certain applications such as EEG and neural recordings. The area and power consumption constraints of each channel are more rigid than single channel design since integration of a large number of channels increases power and area significantly.

### 1.3.2 Research Contributions

The ultra low power system architecture for the sensor interface IC was developed in this research work. The power consumption of each individual circuit block was investigated and minimal power consumption for the overall system was realized. A generalized cross-domain technique was established, which could be applied to any biomedical sensor interface designs to achieve optimal system power consumption. The developed prototype based on the proposed system architecture achieves minimum power consumption of 450nW under 1V supply, which is one of the chips with lowest power consumption reported to date.

Pseudo-resistors based on active devices are widely used in the design of sensor interface IC to achieve ultra low high-pass cut-off frequency with minimum silicon area. However, the existing pseudo-resistor structure exhibits unsymmetrical property and induces unavoidable DC level shift, which make it not suitable for low voltage operation. The second contribution of this thesis is the development of fully balanced tunable pseudo-resistor structure. Employing the proposed pseudo-resistors, the analog front-end achieves less than 0.6% distortion at rail-to-rail output swing, making it the optimum selection for low voltage operation.

The third contribution of this thesis is the low noise, low power front-end amplifiers design. The method of achieving optimal noise to power trade-off is presented. The front-end amplifier reaches a noise efficiency factor (NEF) of 2.24, which is the lowest value reported to date, indicating the optimum noise to power trade-off of the amplifier.

The conventional PGA using switches to connect or disconnect the feedback elements from the feedback loop introduces additional zero-pole pair at low frequency band. A new flip-over-capacitor scheme is developed for the PGA, which eliminates the zero-pole pair and corrects the gain error at low frequency.

For multi-channel biomedical signal recording chip, the area consumption of each individual channel is crucial to minimize the total area of the overall system. An innovative system architecture is proposed, which eliminates the large Miller compensation capacitor in the narrow bandwidth front-end amplifier and achieves more than 50% area saving compared to the existing system. Meanwhile, the proposed system architecture facilitates the system power optimization, where 97% power saving is achieve compared to the current multi-channel design.

## 1.4 List of Publications

Listed below are publications generated from this project.

[1] Xiaodan Zou, Xiaoyuan Xu, Libin Yao, and Yong Lian, "A 1-V 450-nW Fully Integrated Programmable Biomedical Sensor Interface Chip," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 1067-1077, Apr. 2009.

[2] Xiaodan Zou, Xiaoyuan Xu, Yong Lian, and Yuanjin Zheng, "A Low Power Sensor Interface IC for Wearable Wireless Biomedical Devices," *the ICST 2nd International Conference on Body Area Networks*, Jun. 2007.

[3] Lim, E.C.M, Xiaodan Zou, Yuanjin Zheng, and Jun Tan, "Design of Low-Power Low-Voltage Biomedical Amplifier for Electrocardiogram Signal Recording",

*IEEE Biomedical Circuits and Systems Conference (BioCAS2007)*, Nov. 2007, pp. 191-194.

[4] Xiaodan Zou, Xiaoyuan Xu, Jun Tan, Libin Yao, and Yong Lian, "A 1-V 1.1-μW Sensor Interface IC for Wearable Biomedical Devices," *International Symposium on Circuits and Systems (ISCAS 2008)*, May 2008, pp. 2725-2728.

[5] Xiaoyuan Xu, Xiaodan Zou, Libin Yao, and Yong Lian, "A 1-V 450-nW Fully Integrated Biomedical Sensor Interface System," *2008 Symposium on VLSI Circuits*, Jun. 2008, pp. 78-79.

[6] M. Cassim Munshi, Xiaoyuan Xu, Xiaodan Zou, Edward Soetiono, Chang Sheng Teo, and Yong Lian, "Wireless ECG Plaster for Body Sensor Network," *5th International Workshop on Wearable and Implantable Body Sensor Networks (BSN 2008)*, Jun. 2008, pp. 310-313.

[7] Yong Lian and Xiaodan Zou, "Towards Self-Powered Wireless Biomedical Sensor Devices," *9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT 2008)*, Oct. 2008, pp. 1556 – 1559.

[8] Wen-Sin Liew, Xiaodan Zou, Libin Yao, and Yong Lian, "A 1-V 60-μW 16-Channel Interface Chip for Implantable Neural Recording," *IEEE Custom Integrated Circuits Conference(CICC2009)*, Sep. 2009, pp. 507-510.

[9] Xiaodan Zou, Wen-Sin Liew, Libin Yao, and Yong Lian, "A 1V 22μW 32-Channel Implantable EEG Recording IC*," IEEE International Solid-State Circuits Conference (ISSCC2010)*, Feb. 2010.

[10] Chacko John Deepu, Xiaoyuan Xu, Xiaodan Zou, Libin Yao, and Yong Lian, "An ECG-on Chip for Wearable Cardiac Monitoring Devices," *IEEE International Symposium on Electronic Design, Test & Applications*, Jan. 2010.

[11] Xiaodan Zou, Xiaoyuan Xu, Libin Yao, and Yong Lian, a book chapter "The Optimal Design of Low Power Biomedical Sensor Interface," in "*Integrated Microsystems: Mechanical, Photonic and Biological Interfaces*", pending for publication.

## 1.5 Organization of the Thesis

The rest of this thesis is organized as follows.

**Chapter 2:** This chapter gives a literature review of the previous works on biomedical sensor interface IC. The general design considerations for biomedical sensor interface IC are included and the related designs are studied.

**Chapter 3:** This chapter presents the analog front-end sensor interface design for ECG recordings, including the development of the low power system architecture and the detailed circuit description for each individual functional block. The detailed operation of the proposed tunable pseudo-resistor structure and the approaches to achieve optimum noise to power trade-off for the front-end amplifier are introduced in this chapter.

**Chapter 4:** 32-channel sensor interface design for EEG recordings is elaborated in this chapter. Innovative system architecture is proposed to minimize the chip area while maintaining the low power consumption. Different design considerations and specifications are applied according to the characterization of the EEG signal. A front-end amplifier with improved noise performance is employed in this design.

**Chapter 5:** This chapter provides the detailed circuit design of sensor interface IC for neural recording application. Since the frequency band of neural signals can reach as high as 10 kHz, the design focus is shifted to minimization of the thermal noise of the

front-end amplifier. Front-end amplifier structure with higher transconductance efficiency is adopted in this design.

**Chapter 6:** This chapter summarizes the thesis and draws the conclusions. Future works for the design of the low noise low power biomedical sensor interface IC are given and discussed here, including the impedance measurement circuit, driven right leg (DRL) circuits, and integration of the complete system.

# CHAPTER 2

# LITERATURE REVIEW

## 2.1 The Biopotential Signals

Biopotential signals are produced by the electrochemical activities of a certain class of cells, which are know as excitable cells that exist in nervous, muscular or glandular tissue. The cell membranes are selectively permeable to ions and control what enters and exits the cells. Biopotential is the difference in charge across the surface of the cell membranes due to the concentration gradient of ions. This phenomenon is the result of the voltage- and time-dependent and selective permeability of the cell membranes to those specific ions, notably $Na^+$ and $K^+$ [5]. Movement of these ions across the cell membranes causes an electric current to travel along the membranes. In order to measure and record the potentials and currents in the excitable cells, biopotential electrodes provide the interface between the human body and electronic measurement devices, and convert the biological information into measurable and quantifiable electrical signals.

The amplitude and frequency properties of some commonly used biopotential signals are displayed in Figure 2.1 [5]. EOG is the electrooculography, a technique for measuring the resting potential of the retina. Its main applications are in ophthalmological diagnosis and in recording eye movements. EEG refers to the electroencephalography. It is the recording of electrical activity along the scalp produced by the firing of neurons within the brain, and the main diagnostic

applications of EEG are epilepsy, coma, encephalopathies and brain death. ECG is the electrocardiography, the recording of the electrical activity of the heart and is widely used for heart diseases diagnosis. EMG refers to electromyography, a technique for evaluating and recording the activation signal of muscles. The recorded signals can be analyzed in order to detect medical abnormalities or analyze the biomechanics of human or animal movement. AAP is the axon action potential, which is known as the pulse-like waves of voltage that travel along the axons of neurons, and can be widely applied for the studies of neurons activities. It is clear from Figure 2.1 that most of these biopotential signals appear in the low frequency range with small amplitude. This common property of the biopotential signals gives many constraints to the design of the biomedical sensor node, leaving great challenges to the IC designers.

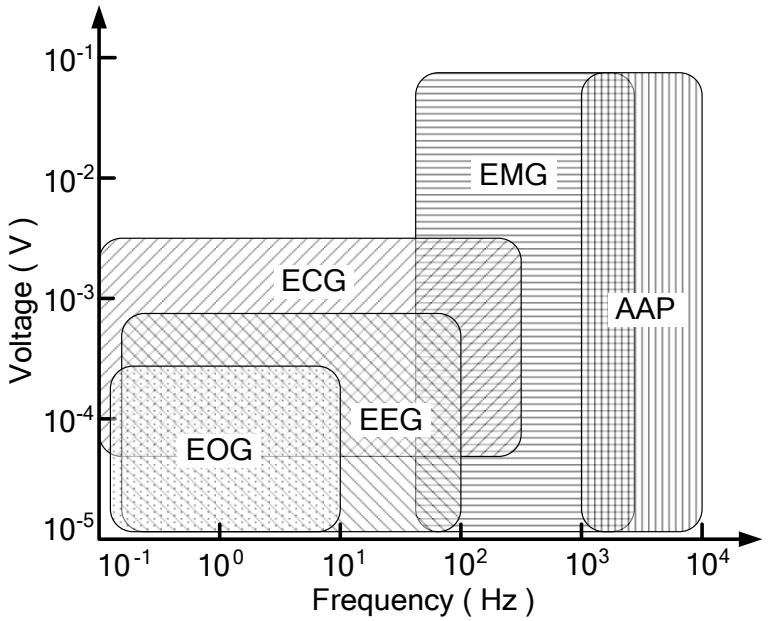


Figure 2.1 Voltage and frequency ranges of some common physiological signals.

## 2.2 General Design Requirements

The biomedical sensor node comes just after the biopotential electrodes and is in charge of the amplification, filtering, digitization and transmission of the acquired biopotential signals. One of the most important parts in the biopotential sensor node is the analog front-end circuits, where the acquired biopotential signals are amplified and filtered for further processing. It locates at the most front-end of the WBAN and plays a very important role in the overall system. There are many strict requirements for the design of the analog front-end circuits. First of all, the main challenge is associated with the nature of biopotential signals. The amplitudes of these signals are in the order of tens of μV to tens of mV and the frequencies span from DC to a few kHz, as illustrated in Figure 2.1. To capture such weak signals, the input referred noise of the analog front-end amplifier is a very critical parameter, especially in the low frequency range, where minimizing the flicker noise becomes an important work. Furthermore, a good analog front-end design needs to be able to accommodate the high dynamic range of different biopotential signals, where fully programmable bandwidth and gain may be necessary. Besides, the biological signals captured from the electrodes are usually accompanied by high DC component, which is resulted from the electrode-skin interface. Hence, a high-pass filter will be necessary, whose cut-off frequency can be adjusted to sub 1 Hz to keep the low frequency component of the biopotential signals undistorted. In addition, small size and light weight are the constant requirements for portable or implantable devices. Compact size calls for a fully integrated system. To further minimize the volume of the device, single battery supply is required, or even battery-less operation is desirable, especially for the implantable devices, where the energy may be collected from human body or the

environment. Thus low voltage operation is an essential requirement, where the whole system needs to be able to function properly at 1 V supply or even lower. Meanwhile, to lengthen the battery lifetime and protect the contact tissue from over heating, ultra low power consumption is also a very important benchmark for the biopotential sensor node. It is especially crucial for multi-channel applications, where slightly higher power consumption for an individual channel design will result in much more heat dissipation if hundreds of channels are implemented. This calls for carefully planned system architecture to balance the trade off between the power consumption and system performance.

## 2.3 Biomedical Sensor Interface IC Design

In recent years, the implementation of the biomedical signal acquisition system and design of each individual functional block have been intensively studied. As stated in the previous section, due to the common characteristics of most biopotential signals, the design requirements for different biopotential applications are quite similar, such as low noise signal conditioning, ultra low power consumption, compact chip size, etc. The general design strategies for biomedical sensor interface IC are investigated and summarized in the following sections.

### 2.3.1 System Structure

In order to minimize the power consumption and chip area of the biomedical sensor interface chip, the system architecture must be carefully plotted. The basic and essential functions of a typical biomedical sensor interface system are amplification,

low-pass filter, high-pass filter and digitization. While these functional blocks can be realized by separated modules, it is preferred to integrate as many functions as possible into a single block to conserve power. Currently, the widely used strategy is to embed the low-pass and high-pass function into the low noise front-end amplifier [6-14]. This method helps to achieve minimum number of active blocks and leads to very compact and neat system structure. One design reported by H. Wu [15] realizes these essential functions with one front-end amplifier and one ADC as shown in Figure 2.2, which consumes only 2.3μW total power. However, without comprehensive analysis and careful partitioning of the overall system's power consumption, the power efficiency of such compact system structure may be quite low [16, 17]. The detailed analysis and development of the power efficiency system architecture for biomedical sensor interface IC will be covered in the next chapter.

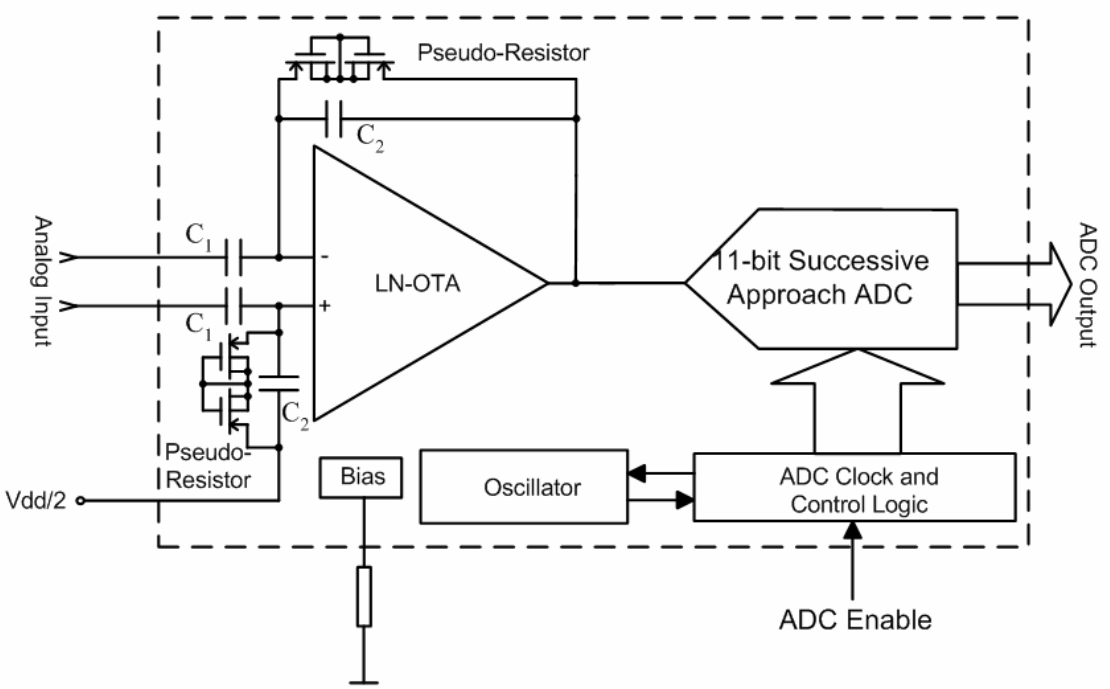


Figure 2.2 Schematic of the system architecture proposed by H. Wu.

To enhance the versatility of the system, tunable bandwidth and adjustable gain functions are implemented in most biomedical sensor interface IC [6-8, 18-20]. Due to the weak amplitude of most biopotential signals, one-stage amplification is usually not able to provide high enough gain for the overall system. As a result, a second stage amplifier is frequently adopted in the system to obtain sufficient gain and high dynamic range [6-8, 18, 19, 21-27]. The adjustable gain function is usually realized by the second stage amplifier, providing an overall system gain ranging from several hundred to few thousand, in order to accommodate the large dynamic range of the biopotential signals. Some designs facilitate gain tuning at the first stage front-end amplifier to realize multi-functional block [11]. However, such structure will lead to inconsistent system bandwidth when gain is changed, because of the constant gain-bandwidth product of the front-end amplifier. Tunable low-pass corner frequency of the system is implemented either at the first stage front-end amplifier, or at the second stage programmable gain amplifier (PGA) [8, 19, 21, 26]. Some reported designs have the feature of variable high-pass corner frequency [7, 8, 28, 29], This function helps to precisely set the high-pass cutoff frequency, keeping the useful biomedical signals in very low frequency band undistorted and shortening the start-up time of the front-end amplifier.

Since the frequency range of the biopotential signal is very low, usually from sub-one hertz to hundreds of hertz, the flicker noise presented in the CMOS devices will degrade the detection of the weak biomedical signals. To remove the flicker noise in the low frequency band, chopper stabilization topology is usually employed [21, 26, 30-37], and the typical system structure adopting chopper amplifier is show in Figure 2.3. This approach is especially popular for very weak biomedical signal acquisition

systems, such as EEG monitoring system [18, 19, 38-41]. However, the design complexity of the chopper stabilized instrumentation amplifier is relatively high, due to the introduction of the modulator and demodulator circuits. Meanwhile, the mid-band gain of the instrumentation amplifier should be high enough at the modulation frequency, which is decided by the corner frequency of the flicker noise, and usually appears at several kHz. This requires relatively wide bandwidth for the amplifier and may increase the power consumption of the amplifier considerably. In addition, a low pass filter is essential after the demodulator block in order to remove the residual voltage spikes, leading to additional power consumption of the overall system. As a result, chopper stabilization scheme is seldom adopted in the monitoring systems dedicated for relatively large amplitude signals or relatively high frequency signals, such as ECG or neural signals [6-8, 11, 15, 28, 42-46].

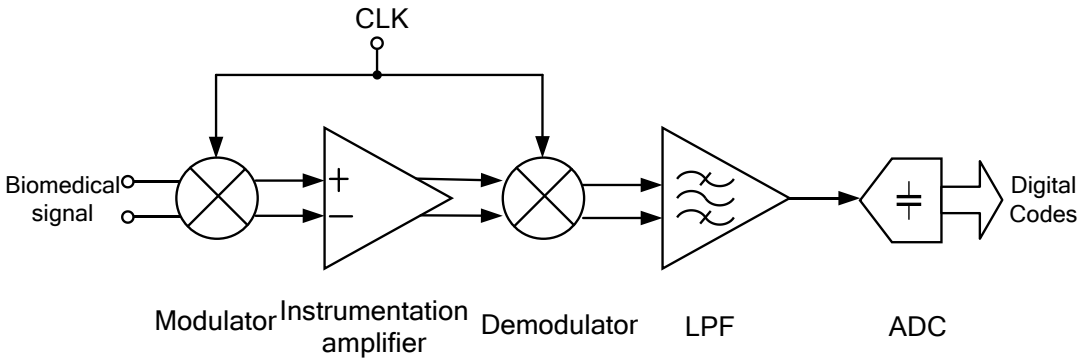


Figure 2.3 A typical system architecture with chopper stabilized instrumentation amplifier.

The above mentioned system structure is mainly for single channel biomedical signal monitoring. However, for some kind of biomedical signals, such as EEG or neural signal, it is necessary to observe multi-channel waveforms and their correlations for both diagnosis and research purposes. This calls for multi-channel analog front-end sensor interface IC design. For EEG recordings, relatively less number of channels are

required [47, 48], and the currently reported designs usually have 32 channels or less [8, 18, 19, 49-52]. However, a large number of channels are required for neural signal recordings. R. R. Harrison has reported a wireless neural recording system with 100 electrodes [7, 53]. F. Heer and M. Chae have both published a design with 128-channel microelectrode array for neural networks [7, 28]. The currently reported neural recording system with highest electrode density is 256 channels, which is developed by J. N. Y. Aziz [6]. The design requirements for multi-channel biomedical sensor interface IC are even more crucial compared to single channel design. First of all, the power consumption of each channel must be optimized to minimum. Otherwise, a slightly higher power for each channel may result in remarkable increase of the overall power consumption and damage the tissue around the recording chip. Besides this, chip area requirement has imposed another constraint to multi-channel system, which is especially important for implantable design. Hence, minimize the chip area is much more essential now. The conventional system structure of multi-channel biomedical sensor interface IC is shown in Figure 2.4. The first stage is a low noise front-end amplifier with band-pass function for signal conditioning, followed by a second stage amplifier for further gain boosting. After that, the multi-channel biopotential signals will pass through an analog multiplexer before the digitization. Some designs do data compression on-chip in order to reduce the size of the data [6, 8, 29, 54, 55]. However, this may result in losing of useful data and is not preferred by doctors [56]. Some designs employ the chopper stabilization topology for the first stage amplifier. This is especially popular for scalp EEG detection [18, 19, 38]. This is because the EEG signal has relatively small amplitude and occupies quite lower frequency band, from 0.16Hz to about 100Hz [47, 48], making the removal of flicker noise more important.

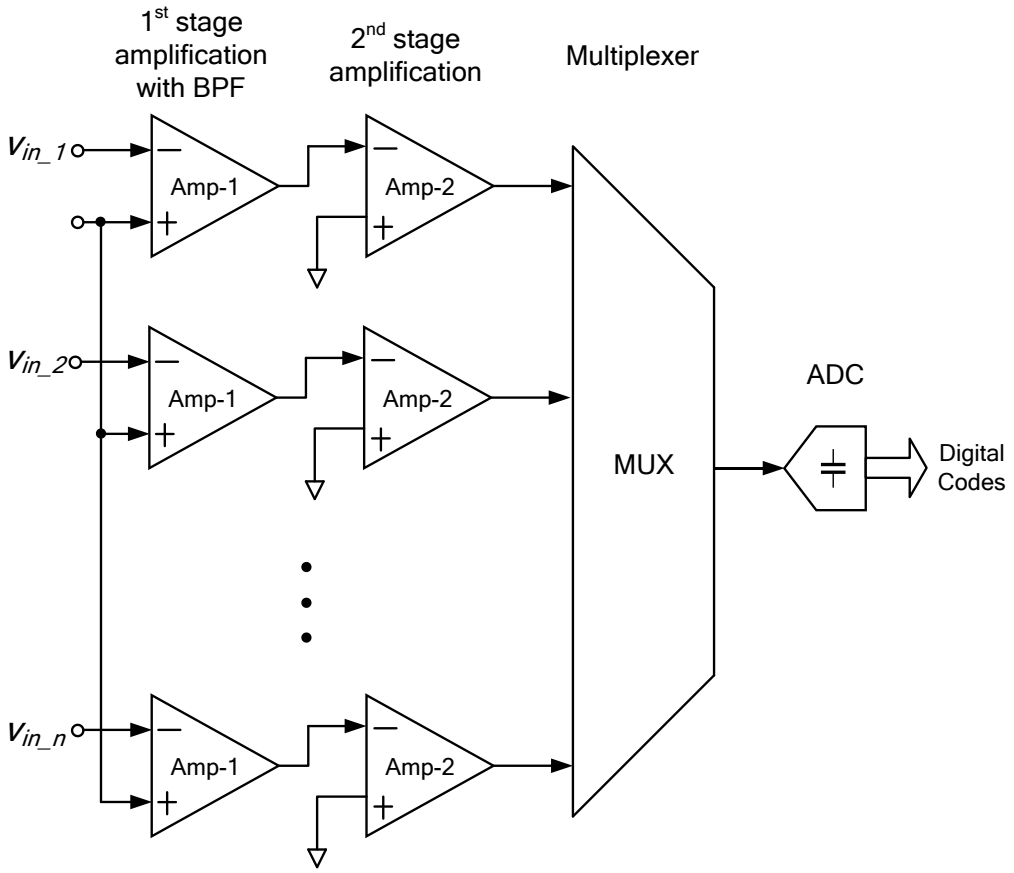


Figure 2.4 Conventional system architecture for multi-channel biomedical sensor interface IC.

### 2.3.2 Low Noise Front-End Amplifier Design

The low noise front-end amplifier is one of the most important modules in the biomedical sensor interface IC, as it comes at the most front-end of the system and most of the system parameters depend on the performance of the front-end amplifier. First of all, the noise performance of the front-end amplifier determines the detection accuracy of the overall system. Minimizing the input referred noise of the front-end amplifier is very critical, which usually requires high quiescent current. On the other hand, the tight power budget may limit the current allocated to the front-end amplifier. As a result, achieving optimum noise to power trade-off for the front-end amplifier

becomes more and more important. To increase the current efficiency of the amplifier, subthreshold operation of the input pair transistor is adopted [12, 57-59], where the transconductance $g_m$ is proportional to the drain current. This is preferred compared to the saturation operation of the input transistors where $g_m$ is proportional to the square root of the drain current, resulting in lower power efficiency.

Another approach employs both NMOS and PMOS transistors as the input pair of the operational transconductance amplifier (OTA) to reduce the input referred noise [42, 60, 61]. One example circuit is illustrated in Figure 2.5 [42]. By doing so, the input transconductance becomes ($g_{mn}$+$g_{mp}$), where $g_{mn}$ and $g_{mp}$ are the transconductance of the NMOS and PMOS input transistors, respectively. This will reduce the thermal noise floor by approximately half and thus suppress the input referred noise. This amplifier structure is especially preferred for relatively wideband applications, such as neural signal recordings, as the thermal noise is the major contributor of the total input referred noise. However, one drawback of the existing design is that, the quiescent current of the published OTA structure depends on the supply voltage and process variation seriously. As illustrated in Figure 2.5, the PMOS and NMOS current source/sink of the OTA is not biased by a fixed reference voltage. The total bias current of the OTA is decided by the voltage overdrive ($v_{gs}$ - $V_{th}$) and aspect ratio of both NMOS and PMOS tail transistors. Any voltage variation of the power supply will completely impose to the $v_{gs}$ of both NMOS and PMOS tail transistors and thereby change the quiescent current of the OTA significantly. As a result, such structure is not suitable for battery operation, as the supply voltage of battery will not remain constant through its entire lifetime. In addition, the transistor threshold voltage of the fabricated chip may be different with the simulated level due to the process

variation. This will also contribute to the variation of the OTA current. The changing of the bias current of the OTA will result in many undesirable outcomes, such as increased noise level, more power consumption, reduced open loop gain, etc.

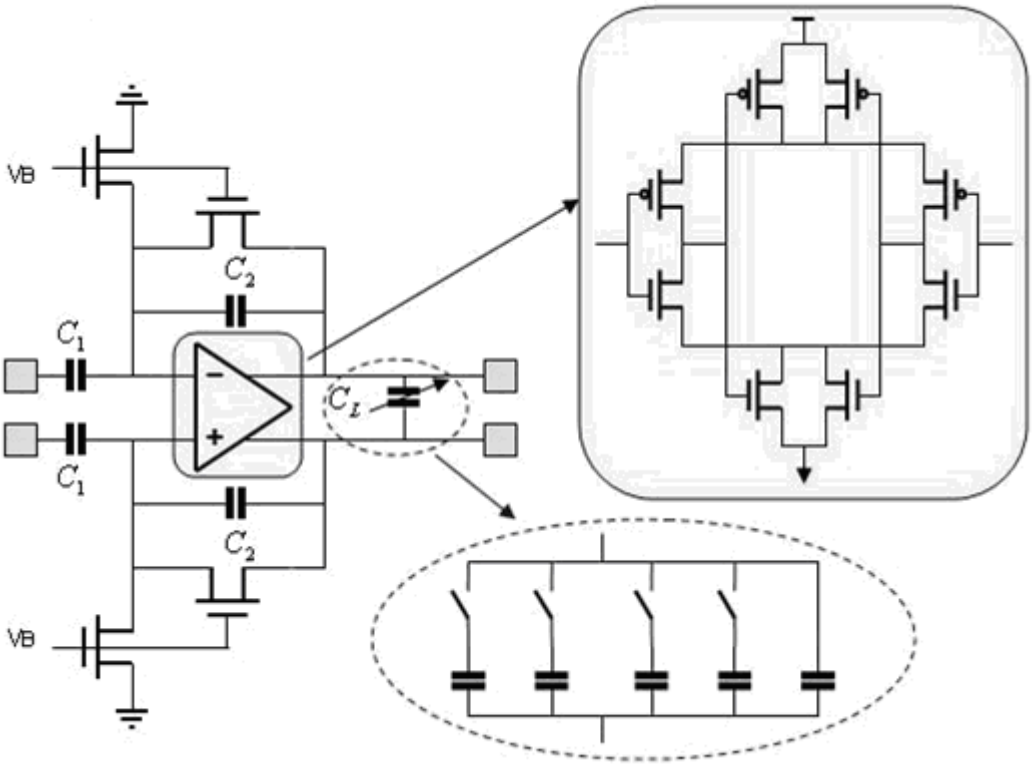


Figure 2.5 Schematic of the amplifier structure proposed by M. Chae.

Besides amplification of the biopotential signals and suppression of the input referred noise, another important function of the front-end amplifier is signal conditioning as band-pass filter is usually embedded into the front-end amplifier to conserve power. One big challenge for the design of the band-pass filter is the realization of the ultra low high-pass -3dB frequency (sub-1Hz) to reject the DC component and low frequency artifacts while keeping the useful biomedical signals undistorted. In order to get such low cut-off frequency, large capacitor or resistor is required, and it is impractical to implement it on-chip using passive component due to the silicon area limitation. The easiest and most direct way to realize the high-pass function is using

external capacitors [21, 62]. However this approach will increase the design cost, and result in bulky devices, which is not suitable for portable or implantable applications. One approach reported by T. Denison, where the high-pass filtering characteristic of the instrumentation amplifier is achieved and tuned using switched capacitor method [31, 63]. This technique is helpful to realize fully integrated system, but it requires additional control clocks and the switching switches lead to poor noise figure and high power consumption. An effective way to achieve ultra low cut-off frequency is first proposed by R. R. Harrison [12], where a huge resistance value in the range of $10^{12}\Omega$ can be achieved with negligible silicon area by employing a MOS-bipolar pseudo-resistor structure. The schematic of the proposed low noise amplifier and the simulated resistance values of the pseudo-resistor are shown in Figure 2.6 and Figure 2.7, respectively.

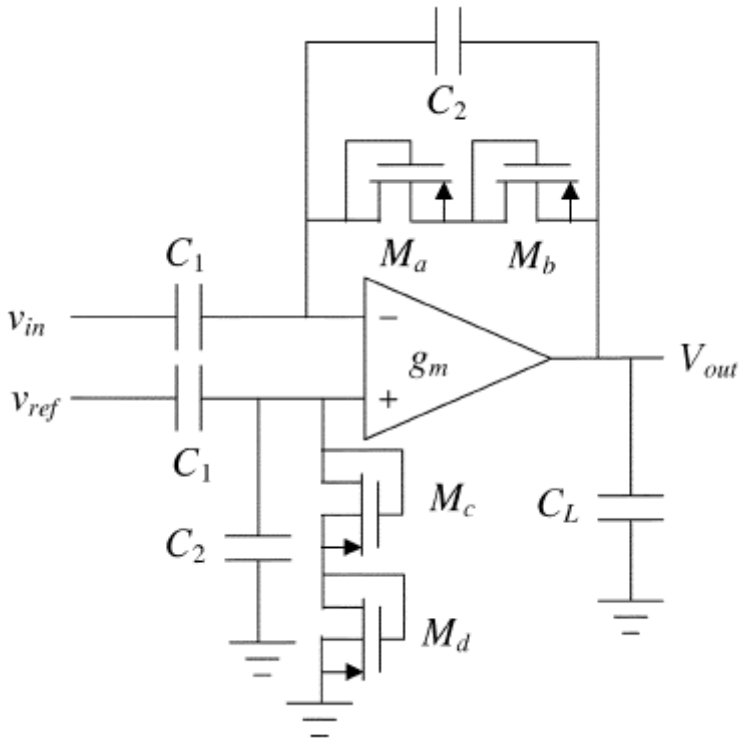


Figure 2.6 Schematic of the low noise amplifier proposed by R. R. Harrison [12].

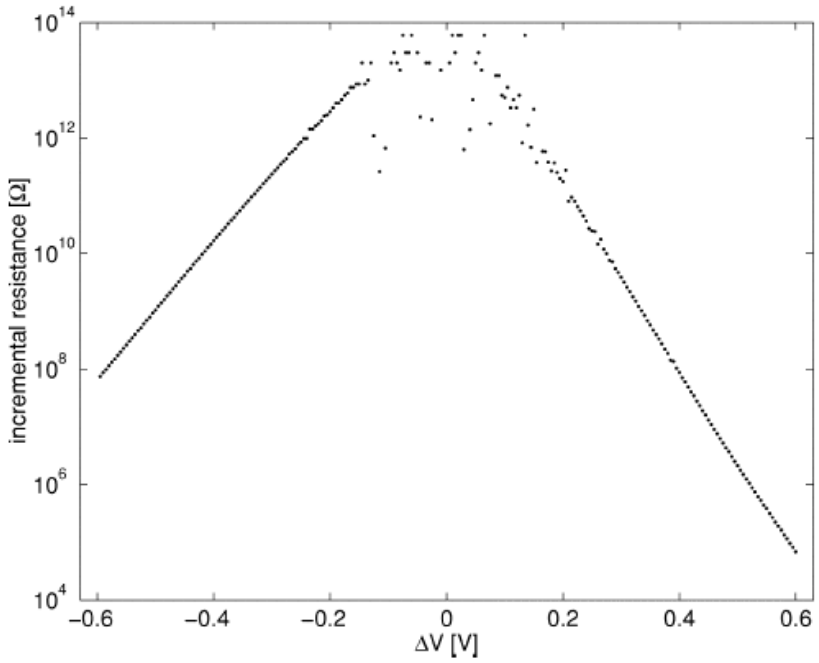


Figure 2.7 Simulation results of the pseudo-resistor proposed by R. R. Harrison [12].

Capacitive feedback topology is adopted by the low noise front-end amplifier to minimize the power consumption and noise figure. The mid-band gain of the amplifier is decided by the capacitance ratio $C_1/C_2$. The pseudo-resistor is composed of two diode-connected PMOS transistors in series as shown in Figure 2.6. The simulated equivalent resistance as illustrated in Figure 2.7 is greater than $10^{12}\Omega$ when the voltage across it is small. That is to say, a smaller capacitance in the range of few pF is sufficient to realize a sub 1Hz cut-off frequency. Since it has many advantages, such as low power, low noise, small area, full integration, easy to implement, etc, this capacitive feedback with pseudo-resistor structure is widely adopted in the design of the biomedical sensor interface IC [7, 8, 10, 15, 28, 29, 43, 64-68]. However, most of these published designs use relatively high power supply of above 3V. This is because the proposed pseudo-resistor is a nonlinear component, which will result in unexpected DC level shift and decreased dynamic range of the amplifier. This property is especially obvious when tunable resistance is realized by directly changing

the gate voltage of the PMOS transistors [7, 28, 29, 65, 69]. While high supply voltage may be tolerant of such drawback, this active resistor structure is not suitable for low voltage operation below 1.5V, as rail-to-rail output range is required for the front-end amplifier to enhance the dynamic range of the system. The design published by H. Wu improves the original pseudo-resistor structure by connecting the two diode-connected PMOS transistors symmetrically and achieves impressive result [15]. However, this is only applicable to the high-pass filter with fixed -3dB frequency. The need for programmable high-pass cut-off frequency calls for a tunable pseudo-resistor structure with small signal distortion. This thesis includes the development and analysis of such tunable pseudo-resistor structure in Chapter 3.

The low-pass cut-off frequency of the amplifier is determined by the dominant pole of the OTA. In order to expand the application of the amplifier to many different types of biopotential signals, the corner frequency of the low-pass filter is usually designed with reconfigurable property. One commonly used method to adjust the bandwidth of the amplifier is to change the capacitive load of the amplifier [7, 18, 19, 21, 42]. However, this method gives no power saving when the system works in narrow bandwidth mode, resulting in lower power efficiency. Another way to change the bandwidth of the amplifier is by tuning the biasing current of the OTA input stage [8, 29]. Such an approach helps to preserve the high power efficiency of the system, since the power consumption will decrease with the decrease of the system bandwidth.

The gain of the front-end amplifier is usually designed according to the amplitude of the target signal, input referred noise requirement, silicon area consumption, etc. If a large gain of more than 100 is required, two-stage amplification is necessary, as it is

not practical to implement using single amplifier due to the large silicon area consumption. The system gain of the currently published designs is from about several hundred to several thousand, and the gain of the front-end amplifier is usually set at 100 or below. For the second stage amplification, it is commonly realized by a programmable gain amplifier (PGA) to enhance the dynamic range of the system. Capacitive feedback is also widely applied here to conserve power and the gain is usually adjusted by changing the feedback factor [6, 8, 11, 18, 21].

### 2.3.3 Technology Selection

CMOS technology is very attractive for the implementation of biomedical sensor interface system due to its low current consumption capability, dense integration, wide availability and low cost [22]. However, most of the biopotential signals occupy very low frequency band, hence the flicker noise presented in CMOS devices considerably limits the detection of weak biopotential signals in the low frequency range [70]. In addition, the relative small transconductance of MOS transistors and threshold voltage variation from device to device often result in poor input offset and inferior common mode rejection ratio (CMRR). These limitations give CMOS IC designers great challenges and only a careful full-customized design can overcome these difficulties.

# CHAPTER 3

# DESIGN OF ANALOG FRONT-END IC FOR ECG RECORDINGS

## 3.1 Design Considerations

Electrocardiogram (ECG) is a test that measures the electrical activities of the heart. The information obtained from an ECG can be used to discover many different types of heart disease. This chapter describes the design of the sensor interface IC for ECG monitoring. The amplitude of the ECG signal is varying from patient to patient and depends on the position of the recording leads. Typically, it can be in the range of 80μV-2mV [46], which is relatively large among the various biopotential signals, such that a moderate gain will be sufficient. The bandwidth of the system will depend on its application, such as QRS detection or diagnostic purpose. In general, the useful signal components reside in the 0.67 to 40Hz bandwidth for standard ECGs and up to 300Hz to 1kHz for pacemaker detection [71]. The input referred noise of the system should be designed as small as possible based on the given power budget. The key design target for the ECG recording amplifier is listed in Table 1

Table 1. Design target for the ECG recording front-end circuits.

| Specification | Value | Remarks |
|---|---|---|
| Supply voltage | 1V | 0.35μm CMOS process |
| Supply current | < 1μA | System total current |
| Amplifier current | < 500nA | Front-end amplifier only |

| | | |
|---|---|---|
| Gain | 200~1000 | Programmable gain |
| Input referred noise | $< 3\,\mu V_{rms}$ | Integrated in the signal band |
| High-pass corner frequency | < 0.5Hz | No external components |
| Low-pass corner frequency | 30~300Hz | Programmable bandwidth |
| CMRR | > 60dB | In the signal band |
| THD | < 1% | @ 80% output swing |

## 3.2 System Architecture

In portable or implantable biomedical systems where power consumption is of primary concern, it is necessary to reduce the number of active building blocks and maximize the power efficiencies of each block. On the system level, this is accomplished by packing as many signal processing functions as possible into one active block while incorporating power management into the design. In addition, full integration of the biomedical signal acquisition chip is necessary to minimize the chip size. On the other hand, there are trade-offs between power consumption and system requirements such as noise figure and amplifier bandwidth. To achieve lower power consumption for given specifications, the system architecture should be carefully designed. A typical biomedical signal acquisition circuit includes a low noise front-end amplifier, a band-pass filter and an ADC. To reduce power, it is a common practice to embed the band-pass function into the front-end amplifier. Besides these, having a programmable gain is essential in order to enhance the dynamic range of input signals. For the ADC, successive approximation register (SAR) ADC is a good candidate due to its low power characteristics [15, 55, 64].

### 3.2.1 Analog Front-end Design

It is well known that the system's overall performance depends largely on the performance of the analog front-end. Full utilization of the tight power budget requires that a large portion of the total power is allocated to the analog front-end. This ensures optimal system performance. In a traditional sensor interface design, there are two essential circuit blocks, i.e. front-end amplifier and ADC. The front-end amplifier usually integrates with a band-pass filter to minimize the number of active components. Capacitive feedback topology is widely adopted for the band-pass filter in most biomedical applications [11, 12, 15, 43] to achieve low power and low noise figure. The cutoff frequencies of the band-pass filter are designed according to the frequency characteristics of the target biomedical signals. To block the DC offset and low frequency interferences in physiological signals, a pseudo-resistor based active filter is implemented to achieve the ultra low cut-off frequency of the high-pass function and full integration [11, 12, 15, 43]. The low-pass cut-off frequency of the band-pass filter is implemented by the dominant pole of the front-end amplifier. This compact system requires minimum number of active circuit blocks. However, we find that this conventional system level approach does not necessarily lead to optimal power efficiency [16, 17, 72]. Problem is induced when the front-end amplifier needs to directly drive the sampling capacitor of the SAR ADC with acceptable sampling error [15]. To illustrate this, we assume that the effect of higher frequency poles/zeros in the front-end amplifier is negligible. Because of relatively low frequencies and small amplitudes of biomedical signals, the linear settling process of the front-end amplifier is dominant in the amplifier dynamic transition. Therefore, we further assume that the amplifier output goes through a first-order linear settling without

slewing in each sampling period as illustrated in Figure 3.1.

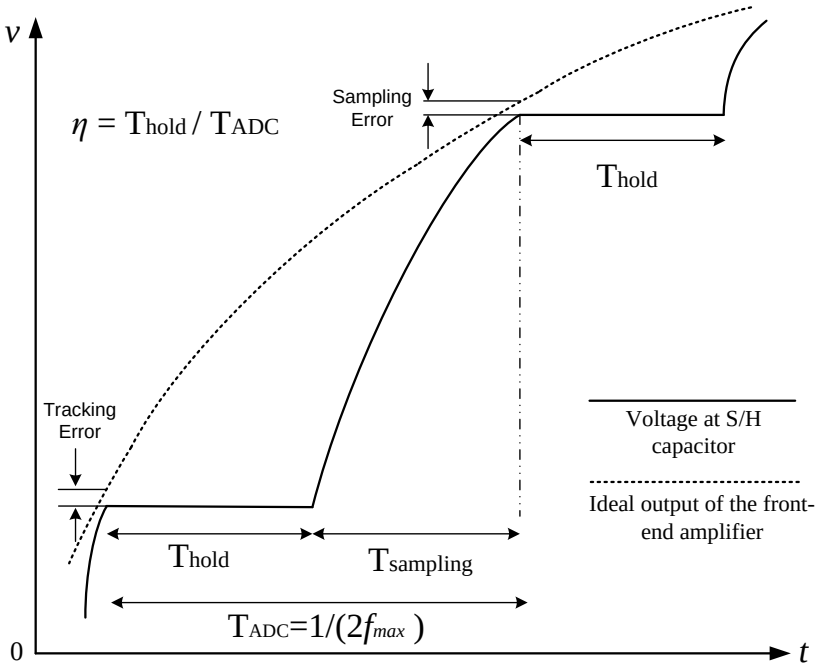


Figure 3.1 Tracking error of the system.

In order to suppress the sampling error within ½ LSB (least significant bit) of ADC, the sampling error of the sample and hold (S/H) circuit need to fulfill the following equation for an n-bit ADC and rail-to-rail swing output,

$$e_{sampling} = \left|\frac{dv_{out}}{dt}\right|_{\max} \cdot t_{hold} \cdot e^{-t_{sampling}/\tau} < \frac{1}{2} \cdot \frac{|v_{out}|_{\max}}{2^n}, \quad (1)$$

where $v_{out}$ is the output of the amplifier, $t_{hold}$ is the holding time of ADC where analog to digital conversion is carried out, $t_{sampling}$ is the sampling time interval of the amplifier, $\tau$ is the time constant of the amplifier and $n$ is the resolution of the ADC. The time constant $\tau$ is determined by the -3dB bandwidth of the front-end amplifier $f_{-3dB}$, which is designed to be equal to the maximum frequency of the target biological signal $f_{signal}$ in this single amplifier structure. Therefore, the time constant $\tau$ can be expressed by Eq. (2),

$$\tau = \frac{1}{2\pi f_{signal}}. \tag{2}$$

$f_{signal}$ is around few hundred hertz in most applications. Consequently, the time constant τ of the amplifier is quite large. Eq. (1) now can be written as

$$e_{sampling} = \left|\frac{dv_{out}}{dt}\right|_{\max} \cdot t_{hold} \cdot e^{-2\pi \cdot t_{sampling} \cdot f_{signal}} < \frac{1}{2} \cdot \frac{\left|v_{out}\right|_{\max}}{2^n}. \tag{3}$$

In order to achieve an acceptable tracking error, the sampling time $t_{sampling}$ must be increased due to the narrow signal bandwidth according to Eq. (3). As a result, $t_{hold}$ is inevitably shortened as it has the following relationship with $t_{sampling}$,

$$t_{hold} = T_{ADC} - t_{sampling}, \tag{4}$$

where $T_{ADC}$ is the time interval for ADC to finish one complete conversion cycle, and it is determined by the maximum frequency of the target signal. For Nyquist rate sampling,

$$T_{ADC} = \frac{1}{2 f_{signal}}. \tag{5}$$

The reduced holding time results in an excessively high conversion speed of the ADC [15]. $f_{CLK}$, which is the minimum clock frequency required by *n*-bit conversion for the ADC, can be estimated using Eq. (6),

$$f_{CLK} = \frac{n}{t_{hold}}. \tag{6}$$

A high value of $f_{CLK}$ results in excessive power consumption by the clock and timing sequence generation modules. As a result, for a sensor interface IC consisting of a

single amplifier with 200Hz bandwidth and a 10-bit ADC, nearly 70% of the total power is consumed by the ADC as shown by simulation results due to the excessively high clock frequency. Clearly, such a single amplifier system structure has large room for improvement in terms of power efficiency.

The main reason for the high conversion speed of the ADC is that the S/H capacitor of the SAR ADC is driven directly by the front-end amplifier, whose bandwidth is designed according to the target biomedical signal. The discussion above suggests that the S/H sampling time should be independent of the application bandwidth. This leads to the proposed system architecture as depicted in Figure 3.2 (the bootstrapped switch and ADC were developed by other team member) [16, 17]. The first block is the low noise front-end amplifier with band-pass function. It is then followed by a second stage amplifier, which isolates the front-end amplifier from the ADC. The settling dynamic of the sampling capacitor now depends on the bandwidth of the second stage amplifier, which is independent of the application bandwidth and can be designed with wider bandwidth to meet the settling requirement, so that the holding time constraint of the ADC is relaxed significantly. A slower clock of tens of kilo-hertz is thus sufficient for an ADC with a sampling rate of 1kS/s, and the power saved from the reduction of ADC clock frequency outweighs the additional power required by the second stage amplifier. By adopting this twin amplifiers architecture, the power distributions for each block can be fully optimized according to the design specifications. Detailed optimization strategy will be described in the next section. Another advantage of this system structure is that the programmable gain function is easily integrated into the second stage amplifier, leaving the front-end amplifier with lower complexity and robust performance. This also ensures consistent system

bandwidth for different gain settings. In the single amplifier approach, the bandwidth and gain tuning features are implemented within one closed-loop amplifier [11]. The fixed gain-bandwidth product suggests that bandwidth adjustment modifies the gain and vice versa. This issue does not exist in the proposed architecture.

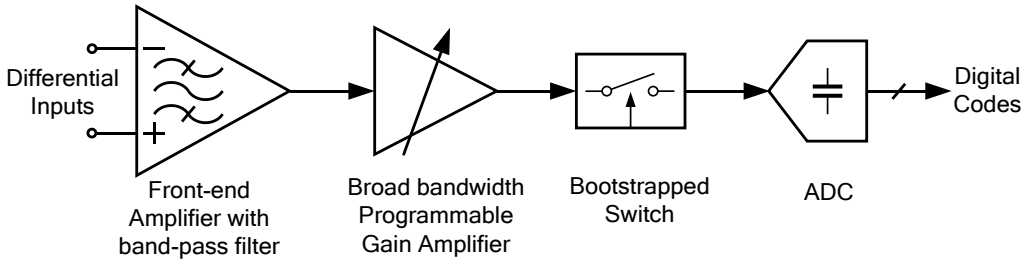


Figure 3.2 Proposed system architecture of the sensor interface.

### 3.2.2 Optimal System Power Partition

Further investigation on the proposed system architecture helps to determine the optimal partitioning of gain, bandwidth and power along the signal path to achieve the best power efficiency, which has never been done in the literatures. The overall gain is set by the amplitude of the physiological signal and the power supply voltage. For example, in a 1V supply ECG monitoring system, the required gain varies from 200 to 1000 corresponding to possible ECG amplitudes of 1~5mV. Generally, the gain of the programmable gain amplifier (PGA) $G_{PGA}$ should be at least one order of magnitude smaller than that of the front-end amplifier to ease its power and noise requirements. Hence, a gain of 100 is reasonable for the front-end amplifier. Since most physiological signals appear in the low frequency band, the bandwidth requirement of the front-end amplifier is realized easily and gives no burden to the tight power budget. As a result, the power consumption of the front-end amplifier is limited by the

input referred noise requirement only, which is relatively fixed for a given biomedical application. Hence, to minimize the power consumption of the front-end amplifier is to realize optimal noise to power trade-off.

In the proposed system architecture, the PGA acts as the driver of the S/H circuit, where broad bandwidth is essential to achieve acceptable sampling error within a relatively short sampling time. The $f_{signal}$ in Eq. (3) now should be replaced by the PGA bandwidth $f_{-3dB}$ as the driver of the S/H circuit is now the PGA and it is not related to the signal bandwidth anymore. Substituting Eq. (4) and Eq. (5) into Eq. (3), we get the following expression,

$$e_{sampling} = \left|\frac{dv_{out}}{dt}\right|_{\max} \cdot t_{hold} \cdot e^{-\pi \cdot \frac{1-2 \cdot t_{hold} \cdot f_{signal}}{f_{signal}} \cdot f_{-3dB}} < \frac{1}{2} \cdot \frac{\left|v_{out}\right|_{\max}}{2^n} . \qquad (7)$$

The $f_{signal}$ and ADC resolution $n$ are almost fixed for ECG application. For a rail-to-rail swing output signal $v_{out}$, Eq. (7) shows that the minimum bandwidth of PGA $f_{-3dB}$ is determined by the ADC holding time $t_{hold}$, which is the key factor that affects the system power consumption. For example, a shorter holding time results in a higher clock frequency according to Eq. (6), as well as higher current dissipation for the ADC. On the other hand, a shorter holding time implies a longer sampling time according to Eq. (4). As a result, the bandwidth requirement of the PGA is relaxed and less current is needed for the PGA. Hence, the length of the holding time affects the power consumptions of both the PGA and the ADC. Therefore, achieving minimum power consumption for the overall system means finding the optimal holding time for the S/H circuits.

For low voltage and low noise circuit designs, the input pair transistors of the amplifier usually operate in the weak inversion region to maximize the current efficiency. Their transconductances $g_m$ are evaluated by

$$g_{m.PGA} = \frac{I_{PGA}}{NV_T}, \tag{8}$$

where $I_{PGA}$ is the current drawn by the PGA, the subthreshold swing parameter $N$ is a process-related constant and $V_T$ is the thermal voltage. This can further be related to the PGA current by

$$I_{PGA} = NV_T g_{m,PGA} = 2\pi NV_T C_C G_{PGA} f_{-3dB}, \tag{9}$$

where $C_C$ is the Miller compensation capacitance of PGA. Assuming that the output of the PGA is a rail-to-rail sinusoid $A \cdot \sin(2\pi f_{signal} t)$, $f_{-3dB}$ can be derived from Eq. (7), i.e.,

$$e_{sampling} = \left| \frac{d(A \cdot \sin(2\pi f_{signal} t))}{dt} \right|_{\max} \cdot t_{hold} \cdot e^{-\pi \cdot \frac{1-2 \cdot t_{hold} \cdot f_{signal}}{f_{signal}} \cdot f_{-3dB}} < \frac{1}{2} \cdot \frac{2A}{2^n}.$$

We obtain the expression for $f_{-3dB}$,

$$f_{-3dB} = \frac{1}{2\pi \cdot \tau} > \frac{\ln(2^{n+1} \cdot \pi \cdot f_{signal} \cdot t_{hold})}{\pi(1 - 2 \cdot f_{signal} \cdot t_{hold})} \cdot f_{signal}. \tag{10}$$

Therefore, the current dissipated by PGA can be estimated by Eq. (11),

$$I_{PGA} = 2\pi NV_T C_C G_{PGA} \frac{\ln(2^{n+1} \cdot \pi \cdot f_{signal} \cdot t_{hold})}{\pi(1 - 2 \cdot f_{signal} \cdot t_{hold})} \cdot f_{signal}. \tag{11}$$

The current drawn by the clock and timing sequence generation modules $I_{CLK}$ can be estimated by Eq. (12),

$$I_{CLK} = C_{load} \cdot {V_{DD}}^2 \cdot f_{CLK} = C_{load} \cdot {V_{DD}}^2 \cdot \frac{n}{t_{hold}}, \tag{12}$$

where $C_{load}$ is the digital load capacitance and *VDD* is the supply voltage. To explore the relationship between total current dissipation and holding time $t_{hold}$ intuitively, $I_{PGA}$ and $I_{CLK}$ can be plotted by varying $t_{hold}$ while keeping the other parameters fixed. To simplify the analysis, $t_{hold}$ is normalized to $T_{ADC}$ and a new parameter $\eta$ was introduced, as defined in Eq. (12),

$$\eta = \frac{t_{hold}}{T_{ADC}} = \frac{t_{hold}}{t_{hold} + t_{sampling}} = 2 f_{signal} \cdot t_{hold}. \tag{13}$$

$\eta$ describes the ratio of holding period in each conversion cycle. A larger $\eta$ means longer holding time and lower ADC conversion rate, but requires much wider PGA bandwidth. Now Eq. (10), Eq. (11) and Eq. (12) can be simplified as

$$f_{-3dB} = \frac{1}{2\pi \cdot \tau} > \frac{\ln(2^n \cdot \pi \cdot \eta)}{\pi(1-\eta)} \cdot f_{signal}, \tag{14}$$

$$I_{PGA} = 2\pi N V_T C_C G_{PGA} \frac{\ln(2^n \cdot \pi \cdot \eta)}{\pi(1-\eta)} \cdot f_{signal}, \tag{15}$$

$$I_{CLK} = C_{load} \cdot {V_{DD}}^2 \cdot f_{CLK} = C_{load} \cdot {V_{DD}}^2 \cdot \frac{2 \cdot n \cdot f_{signal}}{\eta}. \tag{16}$$

To optimize the system power consumption now is to find the optimal value of $\eta$ so that the sum of $I_{PGA}$ and $I_{CLK}$ reaches its minimum. Figure 3.3 plots $I_{PGA}$, $I_{CLK}$ and the sum of the two against $\eta$. From Figure 3.3 it is clear that the minimum total current occurs when $\eta$ is approximately 0.8. With this $\eta$, the optimal power and bandwidth partitioning is achieved.

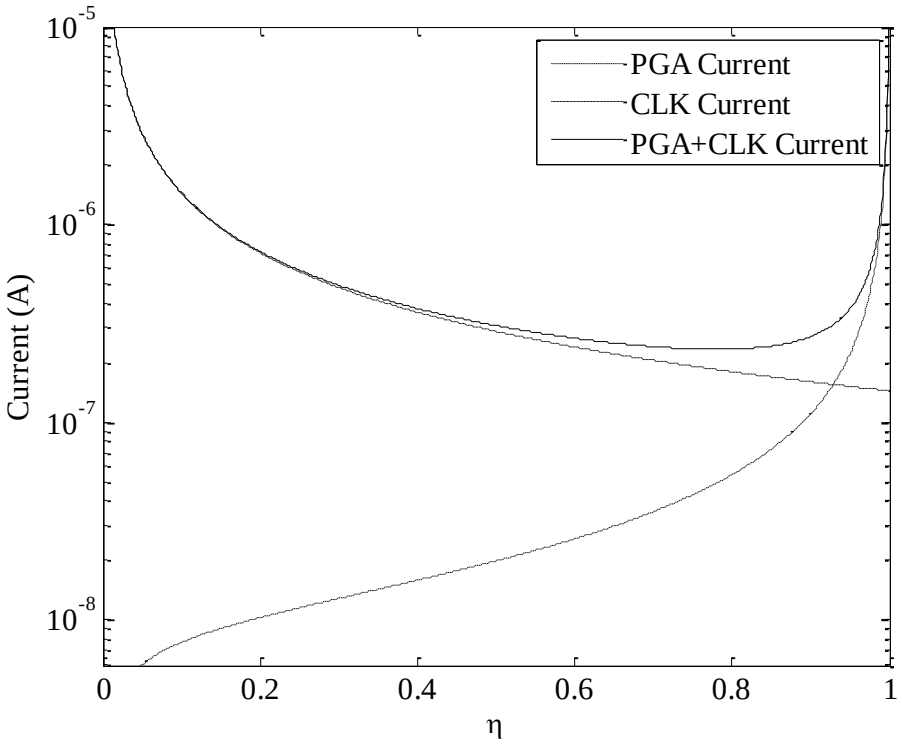


Figure 3.3 Current consumptions of circuit blocks versus $\eta$.

## 3.3 Analog Front-End IC Dedicated for ECG Recordings

This section describes the detailed circuit implementations of the analog front-end circuits dedicated for ECG recordings. It is the first version of the fabricated chips and only the basic functions of an ECG device are realized. The bandwidth and gain of the system are designed with fixed values. The major focus of this design is to minimize the power consumption of each individual module and achieve optimum noise to power trade-off.

### 3.3.1 Circuit Implementations

#### *3.3.1.1 Low Noise Front-End Amplifier*

The front-end amplifier is one of the most critical modules in the biomedical signals recording system. In order to maximize the power efficiency, the band-pass filter is usually integrated into the low noise front-end amplifier. Capacitive feedback is widely adopted in the biomedical amplifiers [11, 12, 15, 43], since it has the advantage of both low power consumption and low noise figure, which are two crucial requirements for biomedical sensor interface design. Figure 3.4 shows the schematic of the low noise front-end amplifier employed in this design.

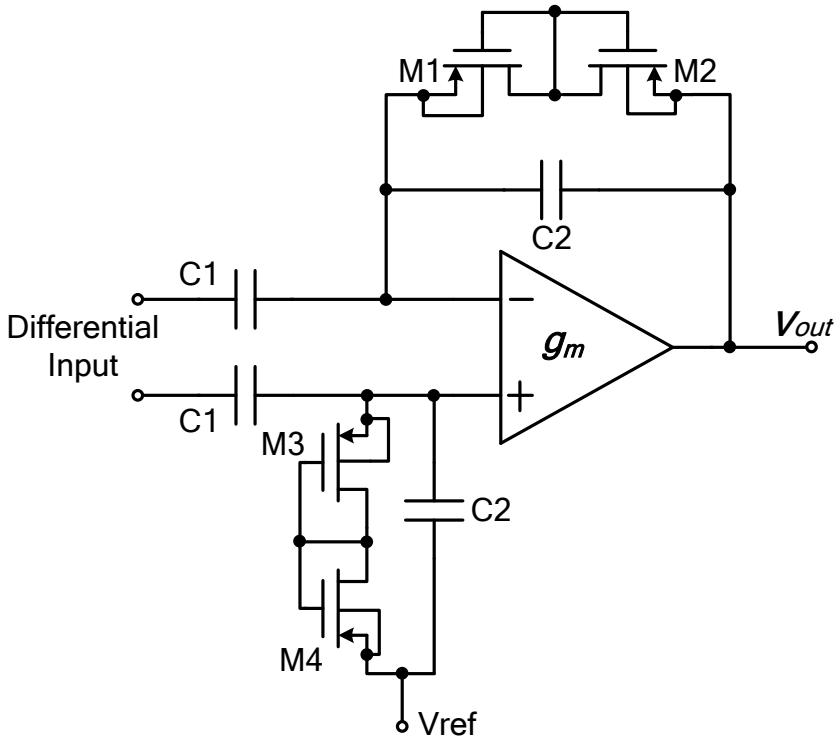


Figure 3.4. Schematic of the low noise front-end amplifier for ECG recordings.

To effectively reject the large DC component, a high-pass filter is built into the front-end amplifier. To minimize the number of external components, pseudo-resistors are usually employed together with the capacitive feedback to achieve a high-pass feature [11, 12, 15-17, 43]. The conventional pseudo-resistor usually consists of two PMOS transistors connected serially, providing ultra high resistance in the order of $10^{12}\Omega$ when the voltage across them is small. Thereby, only a small capacitance in the order of Pico farad is required to achieve a below 1Hz high-pass corner frequency. The implementation of the pseudo-resistors realizes full integration of the overall system and reduces the size of the portable devices significantly. The pseudo-resistors implemented in this design are fully symmetric in term of both geography and electric property, which provide same resistance values when the voltage across them is the same in amplitude but opposite in polarity. This connection topology ensures less signal distortion and enhances the dynamic range of the front-end amplifier. The

detailed analysis of the performance of the fully balanced pseudo-resistors will be given in Section 3.4.

The high-pass corner frequency of the close loop amplifier can be estimated by the following expression,

$$f_{-3dB,high-pass} = \frac{1}{2\pi \cdot R_{eq} \cdot C_2}, \tag{17}$$

where $R_{eq}$ is the equivalent resistance of the pseudo-resistor composed by $M_1$ and $M_2$, or $M_3$ and $M_4$. The value of $R_{eq}$ is usually in the range of $10^{12}\,\Omega$, therefore the high-pass corner frequency appears below 1Hz and the DC component in the biological signals can be rejected effectively. The output DC voltage is regulated by the $V_{ref}$ through the ultra high resistance pseudo-resistors in the feedback loop. In order to facilitate the maximum output swing, the DC levels of the OTA input and output are set in the middle of the supply rail through the external control voltage $V_{ref}$.

The mid-band gain of the front-end amplifier is determined by the capacitance ratio,

$$A_M = \frac{C_1}{C_2}. \tag{18}$$

The low-pass corner frequency of the TB-FEA is determined by the unity gain bandwidth of the operational transconductance amplifier (OTA) according to the following equation,

$$f_{-3dB,low-pass} = \frac{f_{unity,OTA}}{2\pi \cdot A_M} = \frac{g_{m1,2}}{2\pi \cdot C_{C,OTA} \cdot A_M}, \tag{19}$$

where $f_{unity,OTA}$ is the unity gain frequency of the OTA, $g_{m1,2}$ is the transconductance of the OTA input pair transistors, and $C_{C,OTA}$ is the Miller compensation capacitance of the OTA.

*Low Noise Operational Transconductance Amplifier (OTA) Design*

Figure 3.5 shows the schematic of the low noise OTA employed in the front-end amplifier. In order to achieve high enough open loop gain and rail-to-rail output swing, a two stage Miller compensation OTA is implemented. The OTA incorporates a push-pull output scheme by adopting $M_{10}$ and $C_2$ [73]. Transistor $M_{10}$ acts as pseudo-resistors which operate in deep triode region and provide large resistance values in the order of $10^{12}\Omega$. Under DC operation, there is no current flowing through $M_{10}$, resulting in the same DC voltages at the gates of $M_9$ and $M_7$. Under AC operation, the voltage variation at the gate of $M_8$ is transferred to the gate of $M_9$ since $C_2$ cannot charge or discharge quickly enough through $M_{10}$ due to its huge resistances. The combination of $C_2$ and $M_{10}$ enables class AB operation and provides very high settling speed while consuming less quiescent current. The capacitance of $C_2$ should be designed much larger than the gate capacitance of $M_9$ ($C_{gs9}$), otherwise $C_2$ and $C_{gs9}$ act as a voltage divider and remarkable portion of the voltage variation at the output node of the first stage is across $C_2$. That is to say, if we assume the voltage variation at the gate of $M_8$ is $v_i$, the voltage variation at the gate of $M_9$ is also $v_i$ ideally. However, if we take $C_{gs9}$ into consideration, the voltage variation at the gate of $M_9$ will be $v_i \, C_2/(C_2+C_{gs9})$. If $C_2$ is comparable with $C_{gs9}$ or smaller than $C_{gs9}$, the voltage variation at the gate of $M_9$ is almost halved or even smaller. This will make the gate voltage variation of $M_9$ only a small fraction of $v_i$ and greatly degrade the performance of the push-pull output stage.

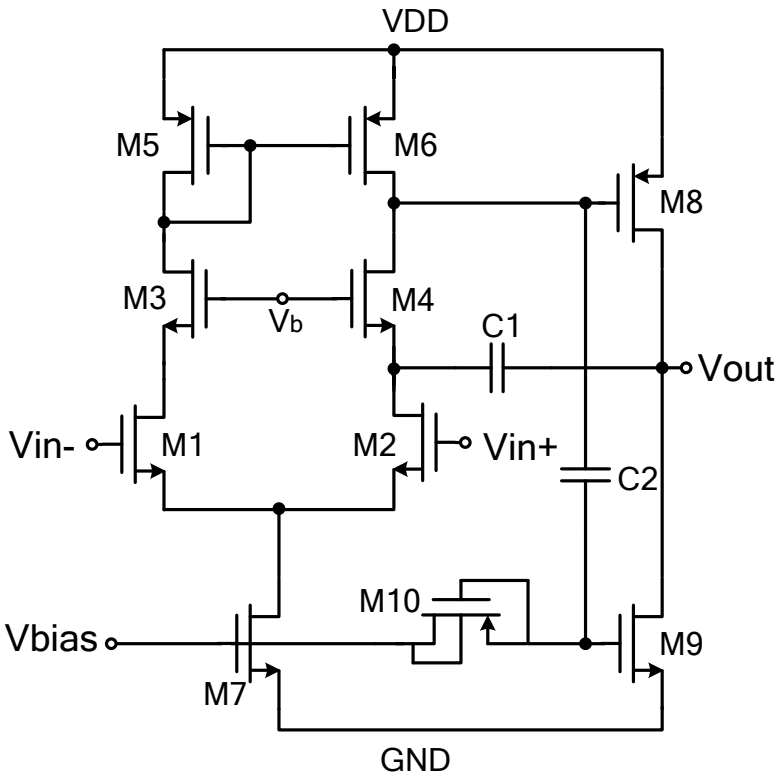


Figure 3.5. Schematic of the OTA used in the front-end amplifier for ECG recordings.

Compared to the conventional class AB structure, this push-pull output stage scheme is even more effective on power saving, since its slew rate is not limited by the quiescent current of the OTA and the driving capability of the OTA is greatly enhanced. More importantly, the equivalent class AB output stage reduces the thermal noise contributed by the output stage, since both transistors $M_8$ and $M_9$ participate in the signal amplification, leading to an improved performance of the front-end amplifier.

For the conventional two-stage Miller compensation OTA, there is no cascade transistor $M_3$ and $M_4$. The feed-forward path generated by the compensation capacitor $C_1$ introduces a right half plane zero which degrades the phase margin of the OTA.

Usually a compensation resistor is used in serial with $C_1$ to push the right half plane zero to a higher frequency or cancel the right half plane zero with non-dominant pole. The value of the compensation resistor is chosen according to the following equation,

$$R_{comp} = \frac{1}{g_{m8} + g_{m9}} \left( \frac{C_L + C_1}{C_1} \right), \tag{20}$$

where $C_L$ is the load capacitance of the OTA. The transconductances of $M_8$ and $M_9$ are in the order of $10^{-6}$. As a result, the required compensation resistor is in the order of $10^6\Omega$. This induces the difficulty that precise resistance value for the present CMOS technology is not available now. Also, the silicon area limitation induces another problem. The other way to cancel the right hand plane zero is using MOS resistor for $R_{comp}$. However, the MOS resistor needs additional circuit to bias and accurate bias is difficult to achieve, resulting in power consumption penalty and increasing the complexity of the OTA. Moreover, in analog domain, complete pole-zero cancellation is very difficult to achieve. Closely spaced pole and zero may not be detected from AC analysis and doublet will be resulted.

In order to avoid the large compensation resistor without affecting the phase margin of the OTA, two transistors $M_3$ and $M_4$ are employed in this design as shown in Figure 3.5 [74]. The right half plane zero can be derived with the aid of the simplified small signal diagram shown in Figure 3.6.

$$g_{m4} V_Y \cdot r_{o6} = V_X$$
$$g_{m9} V_X + g_{m8} V_X = V_Y \cdot sC_1$$

$$\Rightarrow s = (g_{m4} r_{06}) \left( \frac{g_{m8} + g_{m9}}{C_1} \right), \tag{21}$$

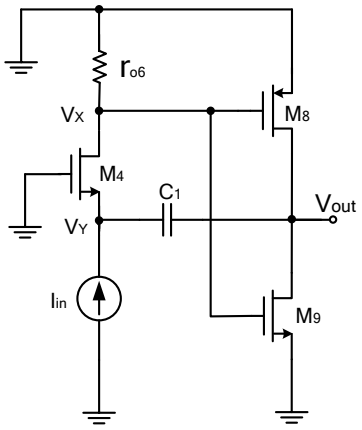


Figure 3.6 Simplified small signal diagram for right half plane zero derivation.

Now the right half plane zero has a much greater magnitude than the original zero of $(g_{m8}+g_{m9})/C_1$, while the dominant pole of the OTA remains the same. Besides the elimination of the compensation resistor, the insertion of $M_3$ and $M_4$ brings the additional benefit of boosting the voltage gain of the first stage. The overall gain expression of the OTA is

$$A_v = g_{m1,2}(g_{m3,4}r_{o3}r_{o1} \parallel r_{o5})(g_{m8} + g_{m9})(r_{o8} \parallel r_{o9}) . \tag{22}$$

It is well known that the input referred noise of the overall system relies on the noise performance of the front-end amplifier, thus minimizing the noise figure is one of the most important tasks in the design of the OTA. The input referred noise contributed by each transistor is calculated as follow:

i) M1 & M2:

$$\overline{v_{n1,2}^{\,2}} = 2 \times 4kT \frac{2}{3} \frac{1}{g_{m1,2}};$$

ii) M3 & M4:

$$\overline{v_{n3,4}^{\,2}} = 2 \times 4kT \frac{2}{3} \frac{g_{m3,4}}{(1 + g_{m3,4}r_{o1})^2 g_{m1,2}^{\,2}};$$

iii) M5 & M6:

$$\overline{v_{n5,6}^{\ 2}} = 2 \times 4kT \frac{2}{3} \frac{g_{m5,6}}{g_{m1,2}^{\ 2}};$$

iv) M8:

$$\overline{v_{n8}^{\ 2}} = 4kT \frac{2}{3} \frac{g_{m8}}{[(g_{m1,2} R_{out1}(g_{m8} + g_{m9})]^2}, \text{ where } R_{out1} = g_{m3,4} r_{o3} r_{o1} \parallel r_{o5};$$

v) M9:

$$\overline{v_{n9}^{\ 2}} = 4kT \frac{2}{3} \frac{g_{m9}}{[(g_{m1,2} R_{out1}(g_{m8} + g_{m9})]^2}, \text{ where } R_{out1} = g_{m3,4} r_{o3} r_{o1} \parallel r_{o5}.$$

So the total input referred noise at DC is the sum of the above individual terms applying superposition theorem.

$$\overline{V_{n,total}^{\ 2}} = \frac{16}{3} kT \frac{1}{g_{m1,2}} \left[ 1 + \frac{g_{m3,4}}{(1 + g_{m3,4} r_{o1}) g_{m1,2}} + \frac{g_{m5,6}}{g_{m1,2}} \right] + \frac{8}{3} kT \frac{1}{(g_{m8} + g_{m9})(g_{m1,2} R_{out1})^2}. \quad (23)$$

It is obvious that $g_{m1,2}$ plays the most important role in minimizing the input referred noise. Larger input transconductance gives lower input referred noise. The most direct and simple way to increase $g_{m1,2}$ is to increase the bias current in the input stage. However, in low power design, it may not be efficient to boost transconductance by a large current. Maximizing the current efficiency becomes the key factor in the optimization of noise-to-power trade-off. Thus a high efficiency of transconductance, which is defined by $g_m/I_d$ (where $I_d$ is the drain current of the transistor), is necessary for low voltage low noise circuits. Highest efficiency of transconductance appears at weak inversion region, where

$$\left(\frac{g_m}{I_d}\right)_{WI} = \frac{I_d \big/ NV_T}{I_d} = \frac{1}{NV_T}. \quad (24)$$

$N$ is the subthreshold swing parameter and $V_T$ is the thermal voltage. It is almost a constant for a specific process technology. In strong inversion region, the efficiency of transconductance can be estimated by the following equation,

$$(\frac{g_m}{I_d})_{SI} = \frac{\sqrt{2\mu C_{OX}\frac{W}{L}I_d}}{I_d} = \frac{\sqrt{2\mu C_{OX}\frac{W}{L}}}{\sqrt{I_d}}. \quad (25)$$

It reveals that a high drain current results in low efficiency of transconductance. Figure 3.7 plots the efficiency of transconductance and transconductance vs. inversion coefficient. Inversion coefficient is a parameter directly related to the drain current of the transistor and is defined by

$$IC = \frac{I_d}{I_S(W/L)}, \quad (26)$$

where $I_S$ here is a process dependent current. In order to achieve the goals of low input referred noise and low power consumption at the same time, we need to get a high transconductance while maintaining relatively high efficiency of transconductance. According to Figure 3.7, it would be better for the operation status of the input transistors to fall into the rolling off region of the efficiency of transconductance curve, where both transconductance and efficiency of transconductance have relatively high values. We set the target power consumption of the overall system to be within 1 μW, so each input transistor gets maximum 150nA bias current. Under these constraints, the input pair is designed with a high transconductance efficiency of about 30, where the transconductance is maximized within the power limit and the noise to power trade-off is improved. A further improvement in the input referred noise is from the class AB output stage as the

transconductance of the output stage increases from $g_{m8}$ in the common source configuration to ($g_{m8}$ + $g_{m9}$) in the push pull output scheme.

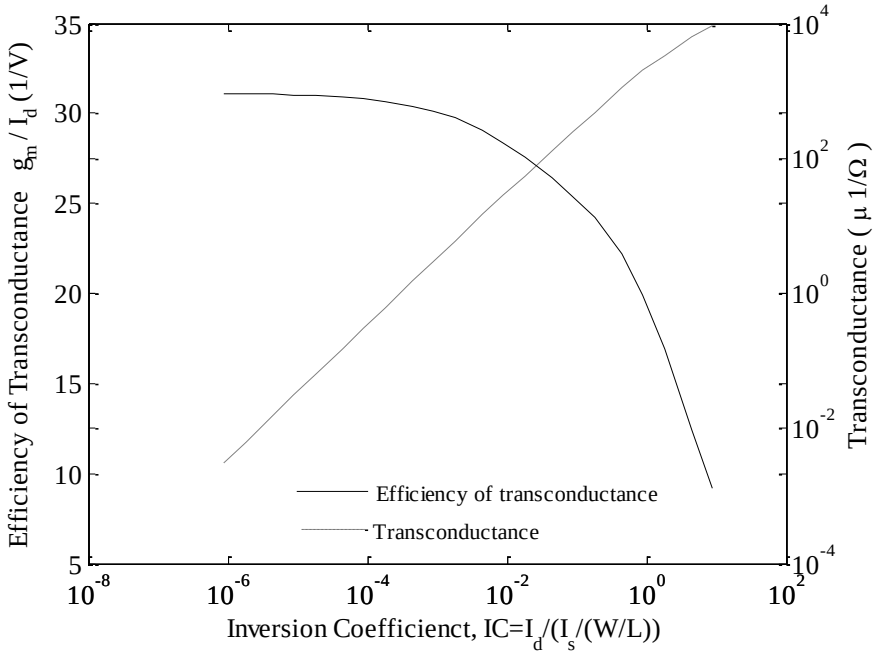


Figure 3.7 Efficiency of transconductance vs. inversion coefficient for input pair of the OTA.

It is well known that the PMOS transistor has better noise performance than NMOS. Thus it should be used as input differential pair [74-78]. However, in the target 0.35 μm CMOS process, the threshold voltage of PMOS transistor is higher than NMOS transistor for about 0.15V, which is a substantial quantity in the low supply voltage design. Moreover, the input transistors are operating at subthreshold region where the drain current depends on the gate voltage exponentially. This makes the voltage headroom even more critical. As a result, the use of PMOS transistors is very difficult due to its high threshold voltage and thus NMOS transistors are chosen for the input pair in this design. The flicker noise is suppressed by choosing large gate area for the input transistors, with an aspect ratio of $W/L$=1040/3 for $M_1$ and $M_2$.

#### *3.3.1.2 Low Gain Buffer*

As discussed in the previous section, a second stage is necessary to isolate the front-end amplifier and the S/H circuits. In this design, a broad bandwidth and high slew rate low gain buffer with gain of 2 is inserted to further amplify the ECG signal and drive the big capacitive load. Since the buffer follows the front-end amplifier where the signals have already been amplified, a large input swing for the buffer is required. For low supply voltage, designing OTA with high input swing and low signal distortion is a complicated and tough task. In order to avoid it, a close loop buffer is chosen as shown in Figure 3.8. A similar capacitance feedback as the front-end amplifier is adopted to conserve power and improve the noise figure. By employing such kind of feedback structure, both the positive and negative inputs of the OTA are virtual ground, such that the input swing requirement for the OTA is greatly relieved. The resistance provided by the pseudo-resistor here is larger than the one used in the front-end amplifier, in order to make sure that the high-pass function of the low gain buffer will not affect the high-pass corner frequency of the overall system. This is realized by using longer transistor length for the pseudo-resistor in the buffer.

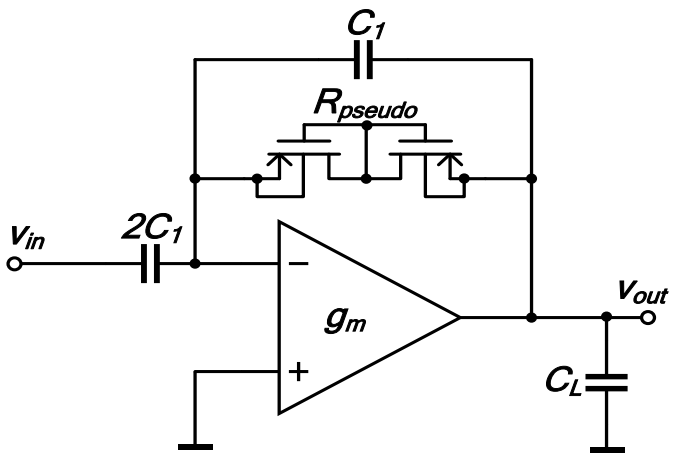


Figure 3.8. Schematic of the low gain buffer used in the ECG recording system.

The OTA of the buffer employs the similar structure with the one used in the front-end amplifier as shown in Figure 3.5, since it can provide high slew rate with very low quiescent current. In order to get wide bandwidth, which is determined by $g_{m1,2}/C_1$, the input stage of the OTA is biased with high quiescent current. On the other hand, the output stage also requires large current to push the secondary pole to high frequency. As a result, the bias currents for the OTA are evenly distributed between the input and output stages to obtain wide bandwidth and safe phase margin.

Since the output load of the buffer is the binary-weighted capacitor array of the ADC, which has an effective capacitance of 128pF in this design, a common practice is to set the dominant pole of the OTA at the output node in order to save power. However, the capacitor array is disconnected from the output node of the buffer during the holding time interval of ADC, which may lead to instability of the buffer during this time. As a result, it might take too long time for the buffer to return to normal operating condition at the beginning of the next sampling interval. To avoid this, the dominant pole of this OTA is set by the Miller compensation capacitor $C_1$, such that the buffer is always kept in stable working condition, regardless of the connection status of the capacitor array.

#### *3.3.1.3 Low Power Reference Generator*

The $V_{bias}$ in Figure 3.20 and Figure 3.25 is the same reference voltage and provided by a low power on-chip reference generator. Since most of the system parameters such as power consumption, noise figure and bandwidth depend on the $V_{bias}$, the reference generator is required to provide precise and stable reference voltage with low power

consumption to ensure robust system performance. The schematic of the reference generator is shown in Figure 3.9, where bipolar junction transistors (BJT) are adopted [74]. The OTA employed in the reference generator is to ensure that $V_X = V_Y$. Thus, the voltage drop across resistor $R$ is the difference between $V_{BE1}$ and $V_{BE2}$, where $V_{BE1}$ and $V_{BE2}$ is the base-emitter voltage of $Q_1$ and $Q_2$, respectively. $M_1$ and $M_2$ are two identical transistors and the current passing through them is derived as follow.

$$I_E \approx I_S A_Q \exp\left(\frac{I_E}{I_S}\right) \Rightarrow V_{BE} = V_T \ln\left(\frac{I_E}{I_S A_Q}\right), \tag{27}$$

$$I_{D1} = I_{D2} = \frac{V_Y - V_{BE2}}{R} = \frac{V_{BE1} - V_{BE2}}{R} = \frac{V_T \ln m}{R}, \tag{28}$$

where $m = A_{Q2}/A_{Q1}$, and $A_{Q1}$ and $A_{Q2}$ are the emitter area of transistor $Q_1$ and $Q_2$. It is well know that resistors are area-consuming. In order to get a small reference current with relatively smaller $R$, $m$ is required to be as small as possible. However, this leads to a very low voltage difference across $R$ if both $R$ and $I_{D2}$ are small. Given $I_{D2}$ in nA range and $R$ in kΩ range, the resultant voltage across $R$ is only several mV or even lower. Problem arises when the offset voltage of the OTA presents. Now the reference current $I_{D1}$ or $I_{D2}$ is expressed by the following equation,

$$I_{D1} = I_{D2} = \frac{V_R \pm V_{OS}}{R}, \tag{29}$$

where $V_{OS}$ is the offset voltage of the OTA, and $V_R$ is the expected voltage difference across $R$ when $V_{OS} = 0$. It is obvious that the reference current will suffer from significant deviation if $V_R$ is comparable to $V_{OS}$. To minimize the negative effect of the offset voltage, $m$ of 2 is chosen and a large $R$ of 1.75 MΩ is selected to get a

reference current of 10nA. This results in relatively large voltage across *R* and making the reference current less sensitive to $V_{OS}$.

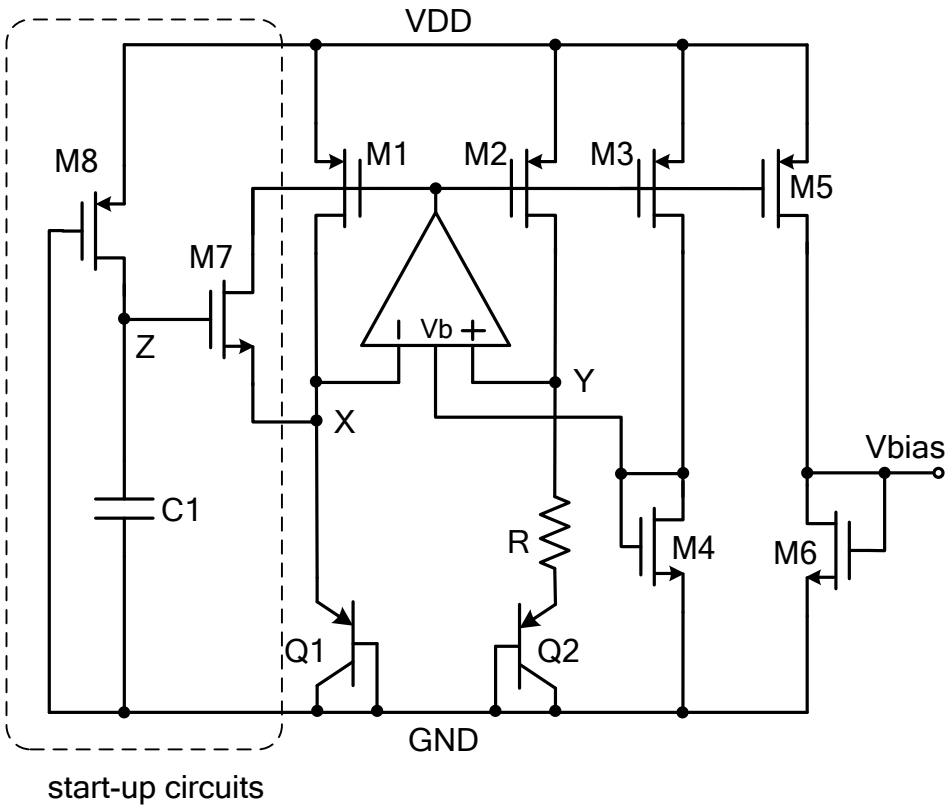


Figure 3.9 Schematic of the reference generator.

When the power supply is just applied, the voltage at gate of $M_1$ and $M_2$ could stick at VDD and the circuit cannot work properly. In order to pull the reference generator to normal working condition, a start-up circuit consisting of $M_7$, $M_8$ and $C_1$ are implemented as shown in Figure 3.9 [79]. $M_8$ is a PMOS transistor with gate connected to ground. It will charge up node Z to VDD during start-up since there is no path for DC current because of $C_1$. $M_7$ then will be turned on, injecting current to the circuit and pulling the gate voltage of $M_1$ and $M_2$ low. After the circuit enters normal working condition, the start-up circuit is turned off and no current is consumed by it.

The schematic of the OTA implemented in the reference generator is shown in Figure 3.10. A simple differential one stage OTA is chosen to conserve power and simplify the design. In order to minimize the offset voltage of the OTA, relatively large gate area is chosen for $M_1$ and $M_2$ and common-centroid layout topology is selected to achieve better transistor matching. Furthermore, $\frac{(W/L)_{3,4}}{I_{D3,4}}$ in Figure 3.10 is designed to equal to $\frac{(W/L)_{1,2}}{I_{D1,2}}$ in Figure 3.9 to further reduce the offset voltage. $V_b$ is the bias voltage provided by the reference generator itself and the total power of the OTA is 10nW under 1V supply.

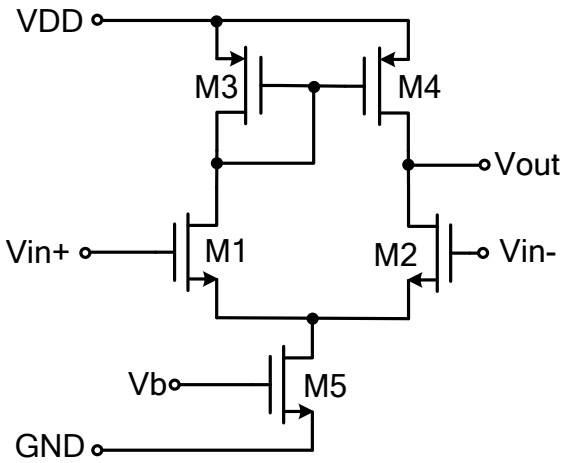


Figure 3.10. Schematic of the OTA adopted in the reference generator.

### 3.3.2 Measurement Results

The analog front-end system including the low noise front-end amplifier, the low gain buffer and the reference generator together with the SAR ADC (developed by the other group member) were fabricated in a standard 0.35μm 4M2P CMOS process with $V_{THN}+|V_{THP}|=1.15V$. Including the ADC, the chip occupies $1mm^2$ area excluding pads, where the analog front-end circuits take approximately half of the total area. The microphotograph of the prototype is shown in Figure 3.26. The top left part and top right part of the chip are the input capacitance of the low noise front-end amplifier. In order to minimize the noise interference from the digitization module, the noisy block such as oscillator was place far away from the analog modules. The capacitor array of the ADC was built on top of the n-type well, which is biased with VDD of the system and act as the guard ring of the analog part. The overall system was designed and tested under a 1V supply and the measurement results are summarized in the later part of this section.

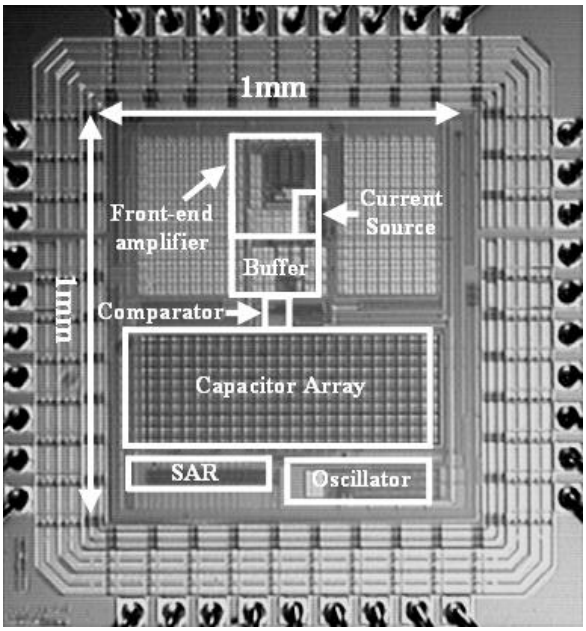


Figure 3.11. Die microphotograph of the ECG recording IC.

The frequency responses of the analog front-end circuits are shown in Figure 3.12. The gain of the front-end amplifier alone is measured to be 39.2dB, while for the overall system, the gain is 45.5dB including the low gain buffer. The -3dB corner frequencies of the system are 0.05Hz for high-pass function and 200Hz for low-pass function, which fulfill the bandwidth requirements for ECG recording system.

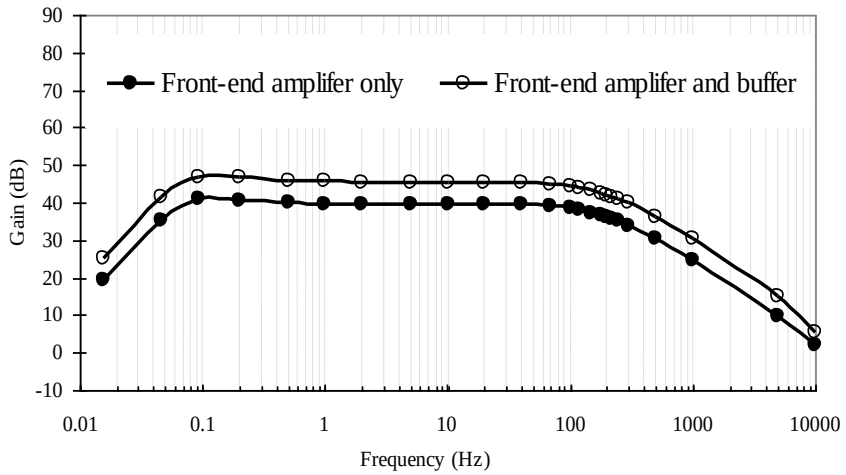


Figure 3.12. Measured frequency responses of the front-end amplifiers.

The input referred noise of the front-end amplifier is shown in Figure 3.13. 50Hz interference and its harmonics are observed, which is injected from the power line. Since very large gate area is selected for the input pair of the front-end amplifier, the flicker noise is effectively suppressed, where its corner frequency has been pushed to very low frequency range indicated in Figure 3.13. So the input referred noise of the system is dominant by the thermal noise. The *rms* value of the input referred noise is 2.1μV integrated from 0.05Hz to 200Hz.

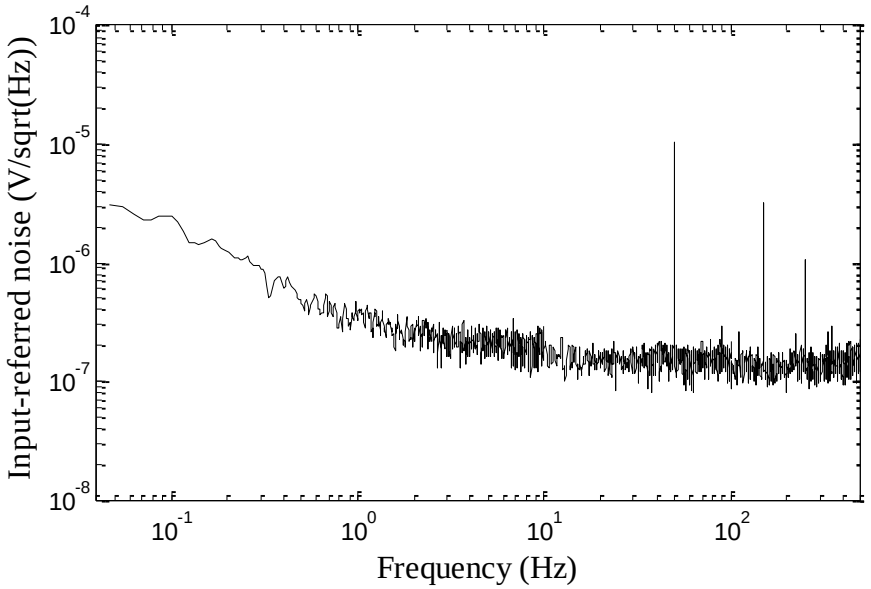


Figure 3.13. Measured input-referred noise of the front-end amplifier.

To measure the noise to power trade-off of the amplifier, the parameter NEF introduced in [80] is adopted. It is an evaluation of an amplifier noise performance taking its quiescent current and bandwidth into consideration and defined by

$$NEF = V_{rms,in}\sqrt{\frac{2 \cdot I_{total}}{\pi \cdot V_T \cdot 4kT \cdot BW}}, \tag{30}$$

where $V_{rms,in}$ is the *rms* value of the input referred noise, $I_{total}$ is the total supply current of the amplifier, $V_T$ is the thermal voltage, and $BW$ is the amplifier bandwidth in hertz. Lower NEF means better noise to power trade-off. The NEF of this design is 2.9, which is one of the lowest figures among these recently published results, indicating that the front-end amplifier achieves better trade-off between power and noise figure.

The performance of the developed system is summarized in Table 2. The total power consumption of the overall system including ADC is 1.1 μW only, with comparable or

better performance on various aspect of the system, showing fully optimized power efficient system architecture, promising long-term and continuous operations for biomedical sensor nodes.

Table 2. Performance comparison between the ECG recording chip and other recently published designs.

| **Parameter** | **Design in [12]** | **Design in [11]** | **Design in [15]** | **This work** |
|---|---|---|---|---|
| Supply voltage | ±2.5V | ±1.7V | 1V | 1V |
| Process technology | 1.5μm CMOS process | 1.5μm CMOS process | 0.35μm CMOS process | 0.35μm CMOS process |
| Current (front-end amplifier) | 16μA | 8μA | 330nA | 260nA |
| Midband gain | 39.5dB | 39.3dB/45.6dB | 40.2dB | 45.5dB |
| -3 dB Bandwidth | 0.025Hz~7.2kHz | 0.015~4 kHz (Tunable) | 0.003Hz~245Hz | 0.052Hz~200Hz |
| Input referred noise | 2.2μVrms (0.5Hz~50kHz) | 3.6μVrms (20Hz~10kHz) | 2.7μVrms (0.05Hz~250Hz) | 2.1μVrms (0.05Hz~200Hz) |
| Noise Efficiency Factor | 4 | 4.9 | 3.8 | 2.9 |
| Front-end amplifier THD | 1% (16.7mVpp input) | 1% (17.4mVpp input) | 0.053% (5 mVpp input) | 0.046% (7.5 mVpp input) |
| CMRR | ≥ 83dB (10Hz~5kHz) | N/A | 61 ~ 64dB (1Hz~250Hz) | > 67dB (Below 500Hz) |
| Total power consumption | 80μW (Amplifier only) | 27.2 μW (Amplifier only) | 2.3 μW | 1.1 μW |

The sensor interface IC was further tested to acquire ECG data from human volunteer, results being benchmarked with a commercially available ECG machine (Welch Allyn PC-Based Resting ECG). The two acquisition systems shared the same probe setup and the data streams were recorded at the same time frame with no post-acquisition processing. The input electrodes of the system were set as lead II configuration, where the negative input was placed on the right arm, and the positive input was placed on the left leg. This is the most useful lead for detecting cardiac arrhythmias and allows the best view of P and R waves. The recorded ECG signals are shown in Figure 3.14. It clearly displays the QRS, P and T waves of the ECG signals, providing steady and reliable performance for the ECG signal recordings.

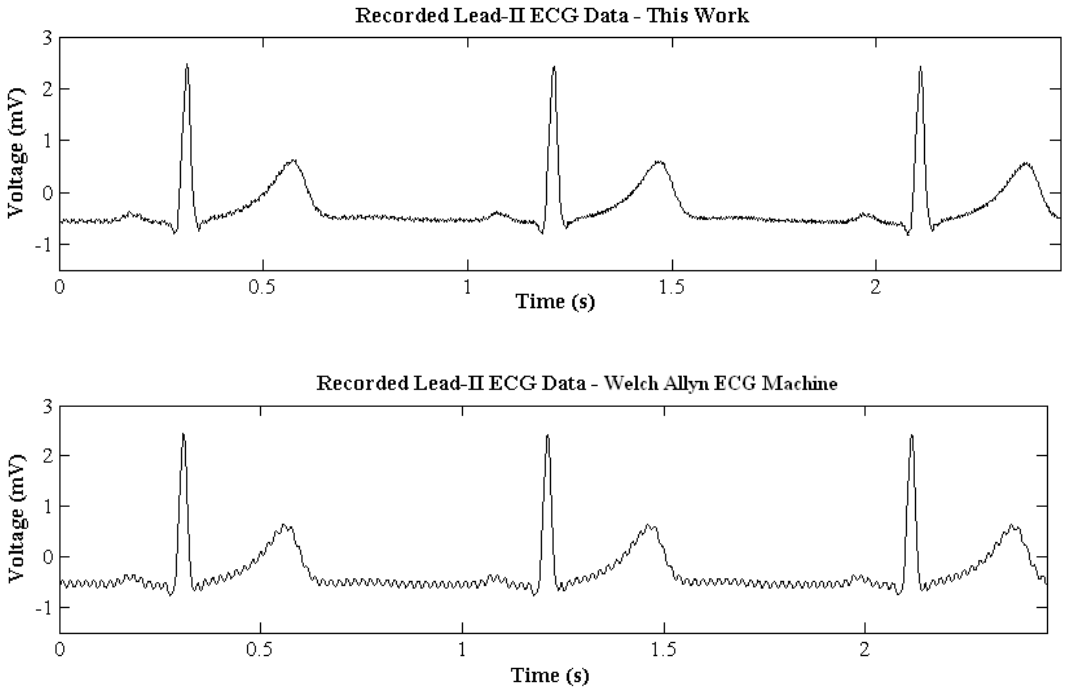


Figure 3.14. Recorded ECG streams by the developed chip and Welch Allyn ECG machine.

## 3.4 Fully Reconfigurable Analog Front-End IC

A fully configurable ECG recording device is usually preferred to fulfill different diagnostic and research purposes. For example, for heart rate measurement, we only need to detect the QRS signal and thus a low-pass filter with 30Hz bandwidth is enough. On the other hand, a thorough and accurate heart diagnosis requires recording of the detailed ECG signals, where a filter with 300Hz bandwidth may be necessary to keep the useful signal undistorted. Furthermore, the amplitude of the ECG signal falls in a quite wide range for different people, from about tens of μV to several mV. As a result, a programmable gain amplifier is needed to enhance the resolution of ECG signals with different amplitudes. In this section, a fully reconfigurable analog front-end IC for ECG recordings is presented, which can be tuned to fit various recording requirements and greatly facilitate the realization of multi-function ECG device.

### 3.4.1 Circuit Implementations

#### *3.4.1.1 Tunable Bandwidth Front-end Amplifier (TB-FEA)*

In order to record ECG signals for different applications, a low noise front-end amplifier with tunable bandwidth was designed. The proposed TB-FEA acts as a low noise amplifier as well as a reconfigurable band-pass filter. The schematic of the close loop TB-FEA is shown in Figure 3.15. It employs capacitance feedback topology and tunable pseudo-resistors to minimize both the power consumption and the noise figure. The high pass-corner frequency is tuned by changing the control voltage of the pseudo-resistors, which then changes the resistance values. The low-pass corner frequency of the front-end amplifier is adjusted by changing the bandwidth of the

OTA, which is realized by varying the transconductance of the OTA input transistors $g_{m1,2}$. Detailed description of the OTA operation will be presented in later section. The reference voltage $V_{ref}$ is fixed at half VDD to enhance the signal swing and minimize the signal distortion.

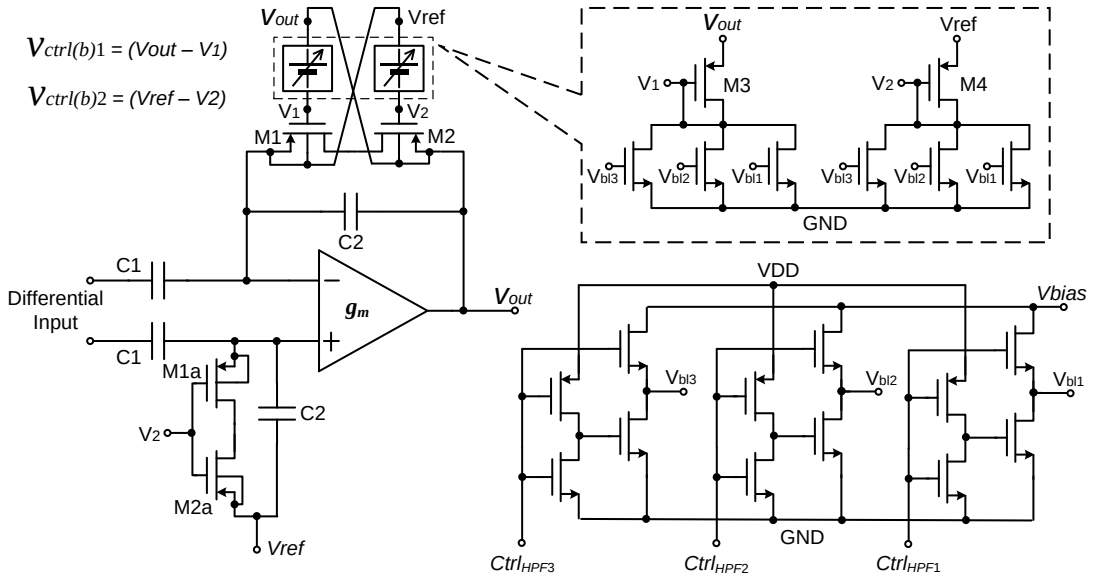


Figure 3.15 Schematic of the TB-FEA with balanced tunable pseudo-resistors.

## *A. Balanced Tunable Pseudo-Resistor*

In order to achieve programmable high-pass corner frequency for different applications, pseudo-resistors with reconfigurable resistances are demanded. The existing tunable pseudo-resistors are usually implemented by adjusting the gate voltage of the PMOS transistors [42, 43, 65], as shown in Figure 3.16. However, this kind of tunable pseudo-resistor exhibits asymmetric and nonlinear resistances when the voltage across the pseudo-resistor varies. This property is clearly demonstrated in Figure 3.17 where the voltage across the pseudo-resistor, ($v_b - v_a$), sweeps from −1V to 1V at different gate control voltages, $v_{ctrl(a)}$. The asymmetric resistance is due to the

fact that the PMOS transistors are in different operation conditions for different $v_b$. For example, when $v_b$ is greater than $v_{ctrl(a)}$, transistors $M_b$ and $M_a$ are entering subthreshold region or even completely switch on with $v_b$ increasing further more. Therefore, the generated resistance keeps decreasing in this range until $M_a$ and $M_b$ entering saturation region, where the resistance is nearly fixed with the increase of $v_b$. When $v_b$ is smaller than $v_{ctrl(a)}$, both transistors $M_a$ and $M_b$ are reverse biased. Hence, the simulated resistance is very high and almost remains unchanged with the decreasing of $v_b$. One point need to be mentioned that the simulations in Figure 3.17 are carried out without considering parasitic imperfections of the transistors, which may cause further unbalance of the existing pseudo-resistor structure.

The asymmetric resistances of the existing pseudo-resistors lead to unavoidable signal-dependent output shift as well as early clippings at one of the power rails as the signal level increases. This is the primary factor which limits the dynamic range in low-voltage circuits. The nonlinearity of the resistance, as perceived by signals sweeping over the slope of the curve in Figure 3.17, introduces additional distortions. Furthermore, the junction leakage current from n-type well to the substrate in the order of sub pA or larger may considerably bias the high impedance node $v_{bulk}$ and induce further unbalanced resistances of the pseudo-resistor. Due to these asymmetric and nonlinear characteristics, the existing pseudo-resistors are usually adopted for high supply voltage of 3V or higher [11, 42, 65].

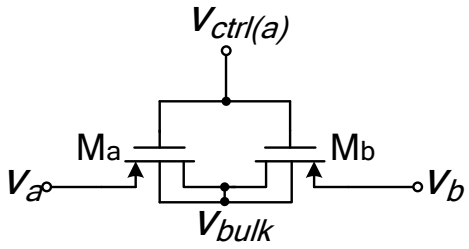


Figure 3.16 Schematic of the existing tunable pseudo-resistor.

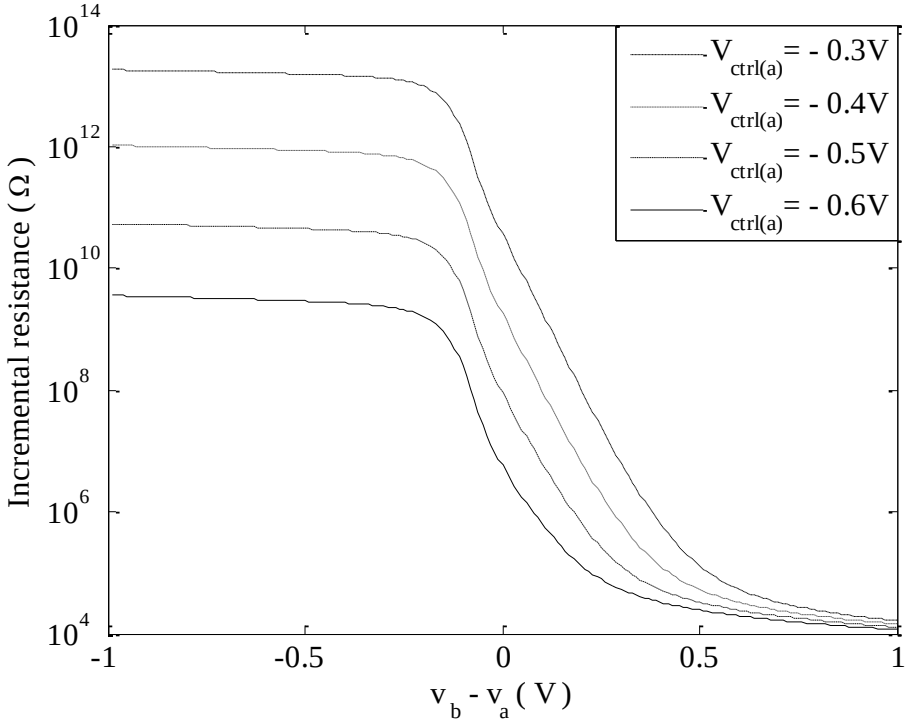


Figure 3.17 Simulated resistance of the existing tunable pseudo-resistor biased at $v_a$ = 0V and $v_b$ swept from –1V to 1V.

As the discussion stated above, the biasing configuration is very crucial for the development of fully balanced tunable pseudo-resistors. Besides ensuring topological and geometrical symmetry across the structure, it is required to source the control voltage $v_{ctrl(a)}$ solely from the local low-impedance nodes of the tunable pseudo-resistors. Furthermore, connecting the parasitic terminal $v_{bulk}$ of the PMOS transistors

to low-impedance node is also necessary to avoid the negative effect of the junction leakage current. Based on these design guidelines, a fully balanced tunable pseudo-resistor structure is proposed, as shown in Figure 3.18. The simulated resistances at different terminal voltages exhibit favorable symmetry, as illustrated in Figure 3.19. The plot is obtained by biasing the tunable pseudo-resistor at $v_a$ = 0V and sweeping $v_b$ from –1V to 1V. The two voltage drops $v_{ctrl(b)1}$ and $v_{ctrl(b)2}$ in Figure 3.18 are designed to be identical and they are equal to the $v_{ctrl(b)}$ Figure 3.19.

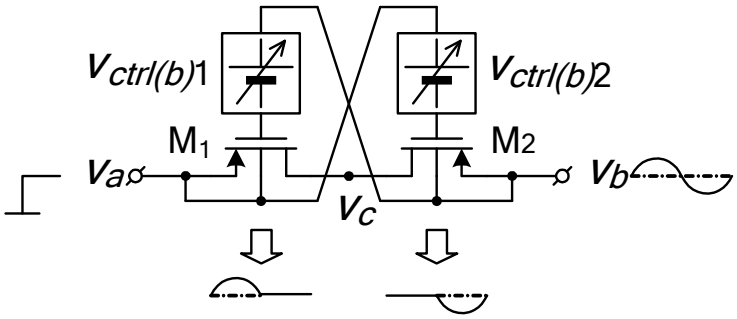


Figure 3.18 Schematic of the proposed tunable pseudo-resistor.

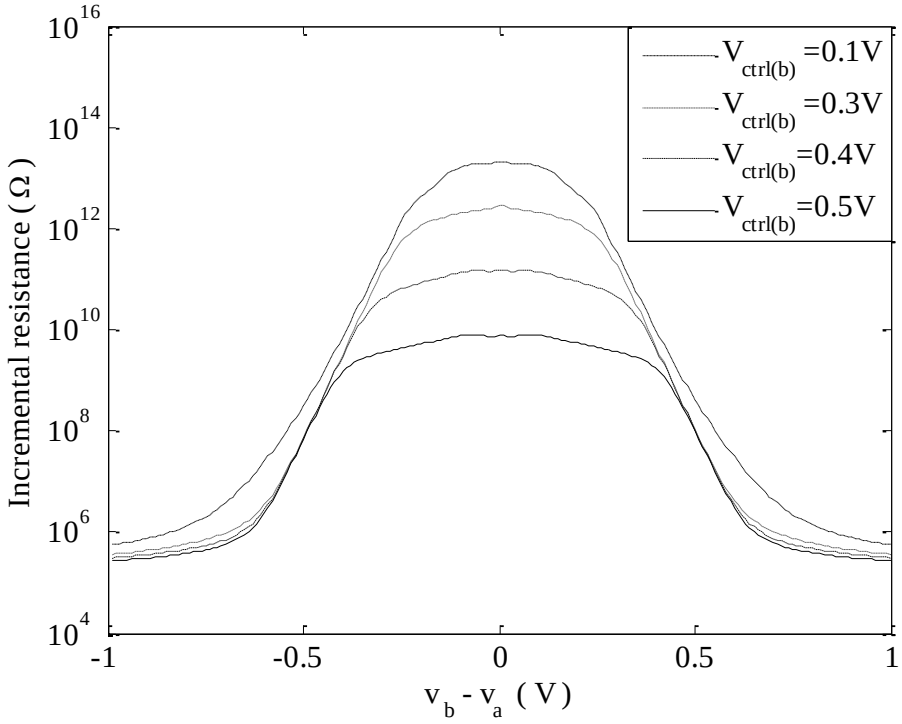


Figure 3.19 Simulated resistance of the proposed tunable pseudo-resistor.

The balanced property of the proposed tunable pseudo-resistor is explained by fixing $v_a$ at a reference voltage and applying a sine wave on top of the reference voltage to $v_b$. During the positive half cycle of the sine wave, the gate of $M_1$ and node $v_b$ are charged up, while the gate of $M_2$ and node $v_a$ remain virtually constant. During this period, the voltage at $v_b$ tends to turn on $M_2$ while keeping $M_1$ off, thereby the terminal voltage $v_b$-$v_a$ is applying to $M_1$ only. Conversely, during the negative half cycle, the gate voltage of $M_1$ is pulled down below the reference level and tends to turn on $M_1$, thereby the voltage swing is now left to the virtually shut $M_2$. Consequently, each transistor works as an active resistor for only half of each cycle.

The control voltages $v_{ctrl(b)1}$ and $v_{ctrl(b)2}$ in Figure 3.18 are formed by ($v_{out} - v_1$) and ($V_{ref}$ - $v_2$), respectively, as indicated in Figure 3.15. Their values are defined by the gate to source voltages ($v_{gs}$) of $M_3$ and $M_4$, respectively, which are in direct association with the drain currents of $M_3$ and $M_4$ (designed to be identical) and independent of $v_{out}$ and $V_{ref}$. Since $M_1$ and $M_2$ are turned on alternatively, $v_{ctrl(b)1}$ and $v_{ctrl(b)2}$ effectively set the $v_{gs}$ for $M_1$ and $M_2$. In this way, the resistance of pseudo-resistor is not affected by the change of $v_{out}$. To tune the resistance, 3-bit digital controlled current sources are used to adjust the current passing through $M_3$ and $M_4$ via $Ctrl_{HPF1}$ ~$Ctrl_{HPF3}$, which in turn determine the values of control voltages and set the high-pass corner frequency. Note that $V_{bias}$ is a fixed voltage reference provided by the internal reference generator. It is worth noting that the maximum voltage swing across the tunable pseudo-resistor should be kept small in order to avoid large changes in resistance. In our design, the expected output voltage falls into ±0.25V range, within which the generated resistances are almost constant and it is sufficient to meet the gain requirement.

*B. Low Noise Operational Transconductance Amplifier (OTA)*

Based on the capacitive feedback structure shown in Figure 3.15, the low-pass corner frequency of the TB-FEA is determined by the −3dB cut-off frequency of the OTA. There are two ways to change the bandwidth of the OTA: varying the load capacitance and adjusting the transconductance by means of changing the transistors bias current. However, as reported in [21], changing the capacitive load gives no DC current saving to narrow bandwidth applications. This makes the first method less attractive for low power design. The better approach to program the low-pass corner frequency is to control the bias current of the OTA.

Figure 3.20 shows the low noise OTA employing the structure of a typical two-stage Miller OTA in order to achieve sufficient gain and rail-to-rail output swing. It is improved based on the previous low noise OTA structure. The dominant pole of the OTA, which is the low-pass corner frequency of the TB-FEA, is adjusted by the 3-bit-controlled bias currents at both input and output stages through $V_{bh1}$ ~ $V_{bh3}$. It is realized by the 3-bit external control signals $Ctrl_{LPF1}$~ $Ctrl_{LPF3}$. For example, when $Ctrl_{LPF1}$ is set at "1", transistor $M_{11}$ is switched on and $V_{bh1}$ is now connected with $V_{bias}$. That is transistor $M_{7A}$ is now biased by the reference voltage $V_{bias}$. Otherwise, when $Ctrl_{LPF1}$ is set at "0", $V_{bh1}$ is pulled down to "0" and there is no current in $M_{7A}$. The $V_{bias}$ in Figure 3.20 is the same $V_{bias}$ as in Figure 3.15. The sum of the current flowing through $M_{7A,}$ $M_{7B}$ and $M_{7C}$ directly determines the transconductances of $M_1$ and $M_2$, subsequently sets the –3dB cutoff frequency of the OTA. Sizes of Transistors $M_{7A}$ ~ $M_{7C}$ were designed to be different and a variable bandwidth from 30Hz to 300Hz is realized. By adopting this approach, tens of nA current dissipation for the OTA is enough to achieve the minimum bandwidth requirement, and power efficiency

is improved significantly.

Similar push-pull output stage is employed for the OTA to enhance its driving capability and save power. The noise analysis of the OTA was already done in the previous section. The input referred noise is minimized according to the developed guidelines. To obtain optimum noise to power trade-off, the aspect ratio of the input pair in this design is the same as the previous design.

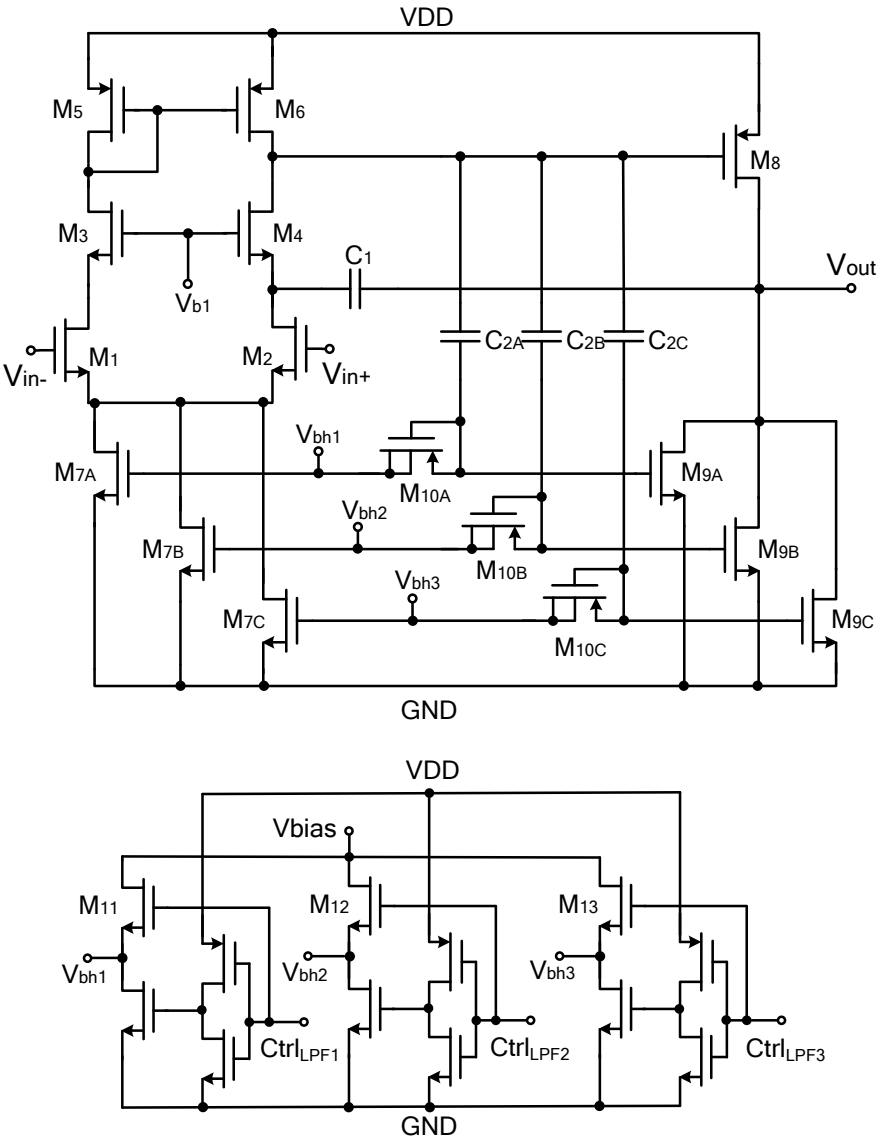


Figure 3.20 Schematic of the low noise tunable bandwidth OTA.

### *3.4.1.2 Programmable Gain Amplifier (PGA)*

To enhance the resolution of ECG signal with different amplitude, a PGA is introduced in the proposed architecture to regulate the gain and to drive the S/H circuit. The voltage gain of the PGA can be adjusted by varying its feedback factor. A common approach is to use a switch to connect or disconnect a feedback path from the loop, as illustrated in Figure 3.21 (a).

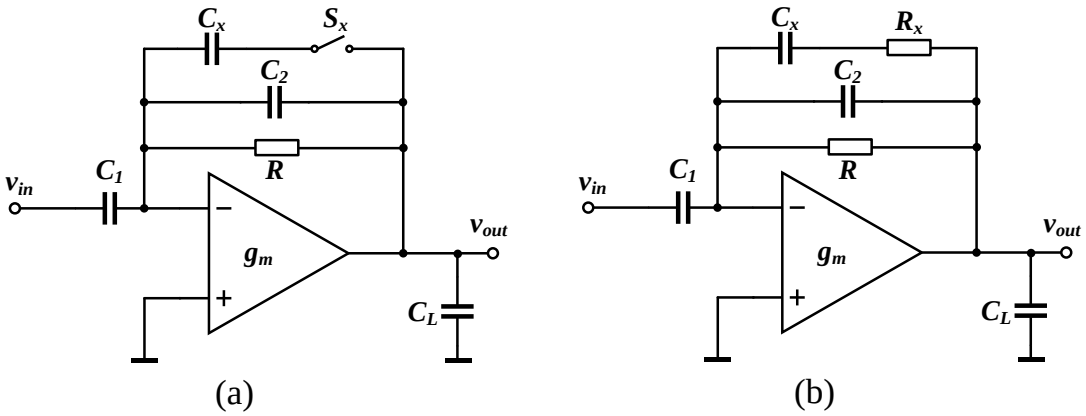


Figure 3.21 (a) Concept of the conventional PGA. (b) Equivalent circuit of the conventional PGA.

For an ideal switch $S_x$, its equivalent resistance is infinite when it is switched off and zero when it is switched on. However, in practice, the switch $S_x$ cannot be simply considered as open circuit or short circuit, especially in low voltage operation where the voltage overdrive for the transistor is relatively small. Instead, it is equivalent to a resistor $R_x$ connected with the capacitor $C_x$ serially, as illustrated in Figure 3.21 (b). As a result, this simple programmable gain scheme may not hold at very low frequency when the reactance of $C_x$ becomes comparable to the off-state resistance $R_x$

of the corresponding control switch. The close-loop gain can be estimated more precisely by the following equation,

$$G = \frac{C_1}{C_2} \bullet \frac{sC_xR_x + 1}{sC_xR_x + 1 + C_x/C_2}. \tag{31}$$

The equation above indicates that $R_x$ introduces an additional zero-pole pair, where

$$z = \frac{1}{C_xR_x}$$

and

$$p = \frac{1 + C_x/C_2}{C_xR_x}.$$

Since $C_x$ is comparable to $C_2$, the resultant zero-pole pair is non-overlapping but close to each other. If $S_x$ is switched on, $R_x$ is in the range of several kΩ, the resultant zero-pole pair appears at very high frequency and thus will not affect the frequency response of the PGA. However, if $S_x$ is in the off state, $R_x$ is approximately in the range of $10^{13}$Ω. Given $C_x$ in pF range, the zero-pole pair occurs around sub 1Hz to a few hertz. As a result, the frequency response is distorted with a small ripple in the low frequency range, interfering with the high-pass function of the TB-FEA.

To correct the signal distortion at low frequency, the "flip-over-capacitor" scheme is proposed as shown in Figure 3.22. There are two control switches $S_x$ and $\overline{S}_x$ associated with each flip-over-capacitor $C_x$, and the statuses of the two switches are always complementary. That is, $C_x$ is connected in parallel with either $C_1$ or $C_2$ according to the different gain settlings. In such a feedback scheme, $C_x$ functions either as a part of the input capacitor or as a part of the feedback capacitor according to the states of the two control switches. By doing so, the off-state resistance $R_x$ of the

corresponding switch is always excluded from the feedback loop and behaves only as a negligible load to the TB-FEA and the PGA as illustrated in Figure 3.23, posing no threat to the frequency response of the system. Two sets of $C_x$ are implemented in the PGA as shown in Figure 3.24. By flipping over each $C_x$ to either input or output node, four gain settings are achieved. The on-off states of $S_{x1}$ and $S_{x2}$ at different gain settings are listed in Table 3. The capacitance values of $C_1$, $C_2$, $C_{x1}$, and $C_{x2}$ are 8pF, 1pF, 2pF and 1pF, respectively. The four gain levels allow the system to handle input signals with amplitudes from several mV down to tens of μV, which satisfies the ECG recording requirement.

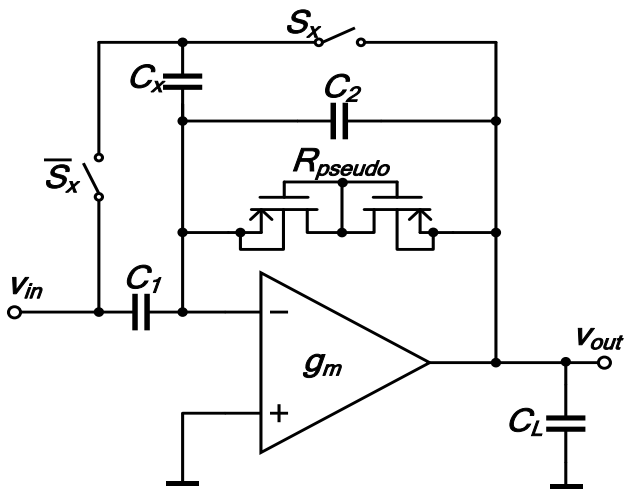


Figure 3.22 Concept of the proposed PGA with flip-over-capacitor.

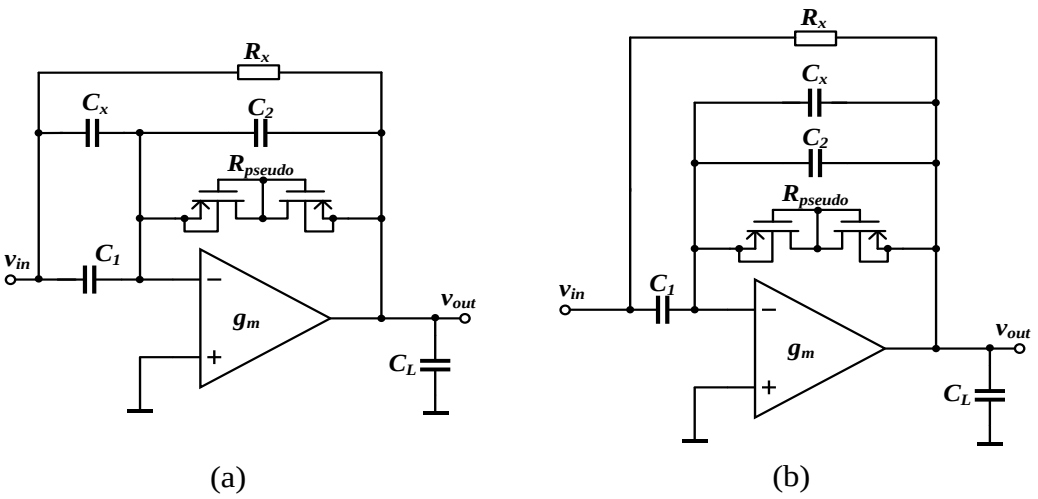


Figure 3.23. Equivalent circuit of the proposed PGA (a) when $C_x$ is flipped to input node and (b) when $C_x$ is flipped to output node.

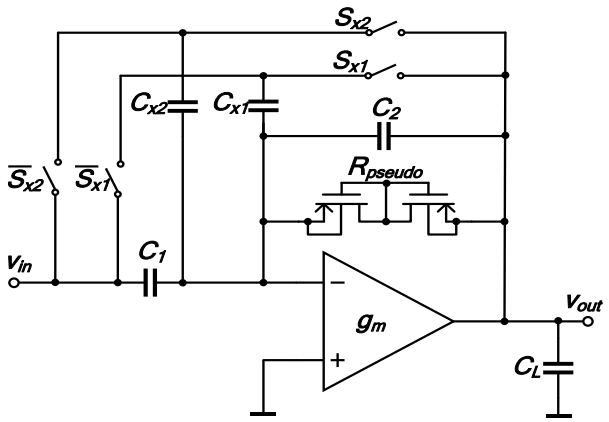


Figure 3.24 Schematic of the proposed PGA with flip-over-capacitor.

Table 3 Configuration of the control switches of PGA for each gain setting.

| Gain of PGA | $S_{x1}$ | $\overline{S}_{x1}$ | $S_{x2}$ | $\overline{S}_{x2}$ |
|---|---|---|---|---|
| 2 | ON | OFF | ON | OFF |
| 3 | ON | OFF | OFF | ON |
| 5 | OFF | ON | ON | OFF |
| 11 | OFF | ON | OFF | ON |

The DC biasing points of the PGA are regulated by a fully balanced pseudo-resistor with a fixed resistance. The reference voltage is set at half VDD to insure low signal distortion and high output swing. The resistance of the pseudo-resistor is designed to be large enough to ensure that the resultant high-pass corner frequency is lower than the lowest high-pass corner frequency of the TB-FEA. To ensure high driving capability, the OTA implemented in the PGA adopts a similar topology as the one in the TB-FEA as shown in Figure 3.25, since it can provide large slew rate with low power consumption.

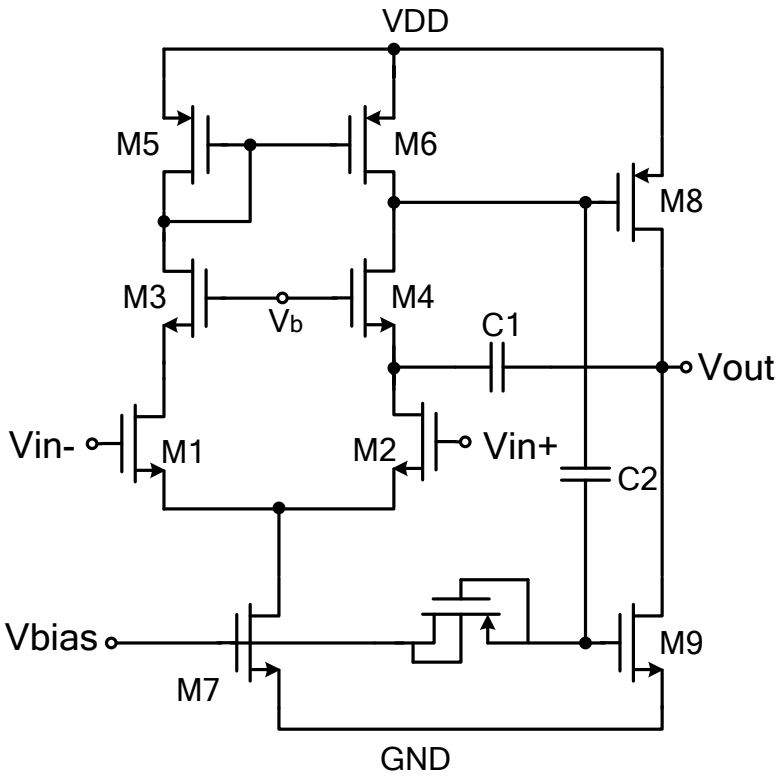


Figure 3.25. Schematic of the OTA adopted in PGA.

Since the bandwidth of the PGA is changed when different gain level is chosen due to the constant gain-bandwidth product, the bandwidth of the PGA is the narrowest when the voltage gain is set to 11. To ensure an acceptable tracking error for each

gain level, the minimum bandwidth requirement of the PGA is applied when the voltage gain is 11. Even though the bandwidth of the PGA varies, the bandwidth of the overall system still keeps constant as it is determined by the bandwidth of the TB-FEA, which is fixed and much narrower than the smallest bandwidth of the PGA. Based on Eq. (13), assuming the maximum signal frequency is 200Hz and $\eta$ is 0.8, the minimum bandwidth requirement for the PGA is 3.2kHz for a 12-bit ADC. To be conservative, the bandwidth of PGA at gain of 11 is designed to be greater than 5kHz for a reliable system performance.

### 3.4.2 Measurement Results

The analog front-end circuits including TB-FEA, PGA and reference generator were fabricated in a standard 0.35μm 4M2P CMOS process with $V_{THN}+|V_{THP}|=1.15V$. Together with the digitization module, the chip occupies 1-$mm^2$ area excluding pads, where the analog front-end circuits take approximately half of the total area. The micrograph of the prototype is shown in Figure 3.26. The system was designed and tested under a 1-V supply and the measurement results are summarized in the following sections.

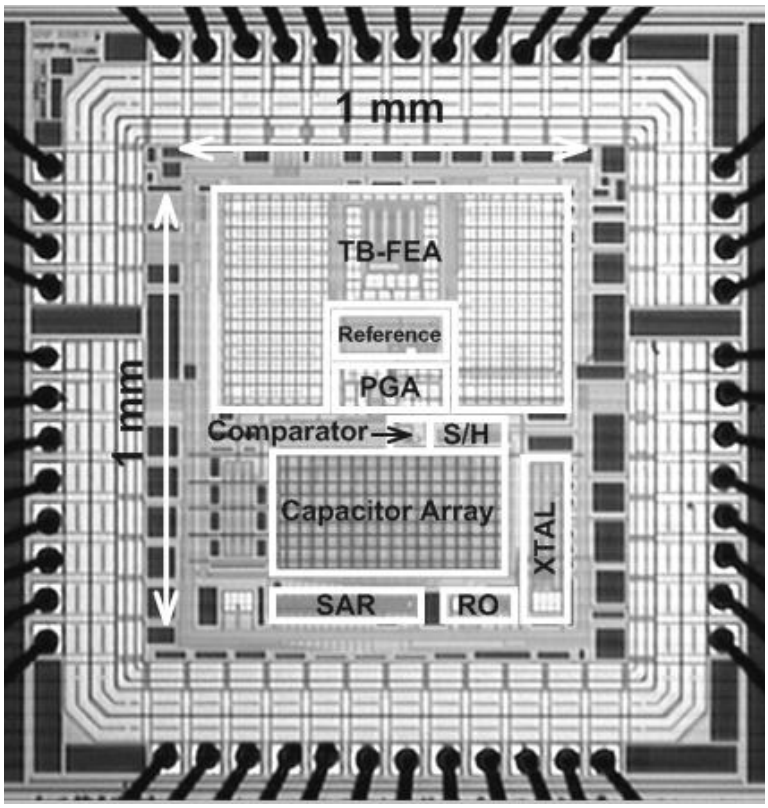


Figure 3.26 Microphotograph of the chip for ECG recording.

#### *3.4.2.1 Frequency Response*

The measured frequency responses of the TB-FEA are shown in Figure 3.27. It realizes a midband gain of 39.2dB with tunable bandwidth control, where the lower corner frequency can be adjusted from 4.5mHz to 3.6Hz and the upper corner frequency can be adjusted from 31Hz to 292Hz. The voltage gain of the system can be programmed by changing the gain of the PGA, where four level voltage gains of 45.6dB, 49dB, 53.5dB, and 60dB can be selected, as plotted in Figure 3.28. Since the current control approach was employed to tune the low-pass cut-off frequencies, the current dissipation of the TB-FEA reaches its minimum of 33nA when the narrowest bandwidth of 31Hz is selected and maximum of 337nA when the widest bandwidth of 292Hz is chosen. This tunable scheme improves the power efficiency effectively and makes the system suitable for portable/implantable devices with battery operation. The application of the developed prototype is not limited to continuous ECG recordings, but also can be extended to other biological signals acquisitions, such as audio signal, by tailoring the gain and bandwidth according to the specific recording requirements.

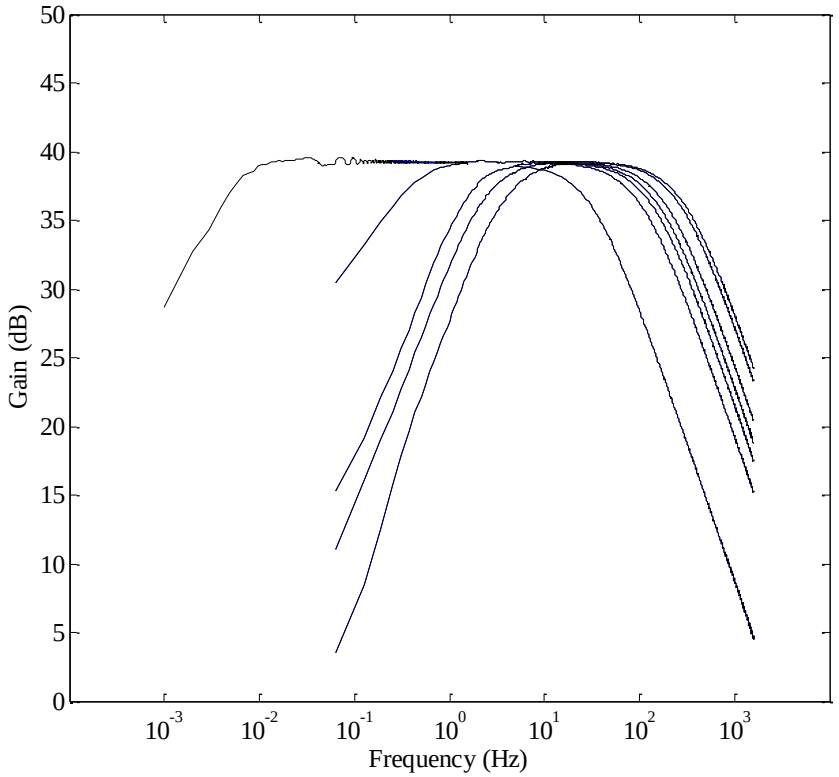


Figure 3.27 Frequency responses of the TB-FEA.

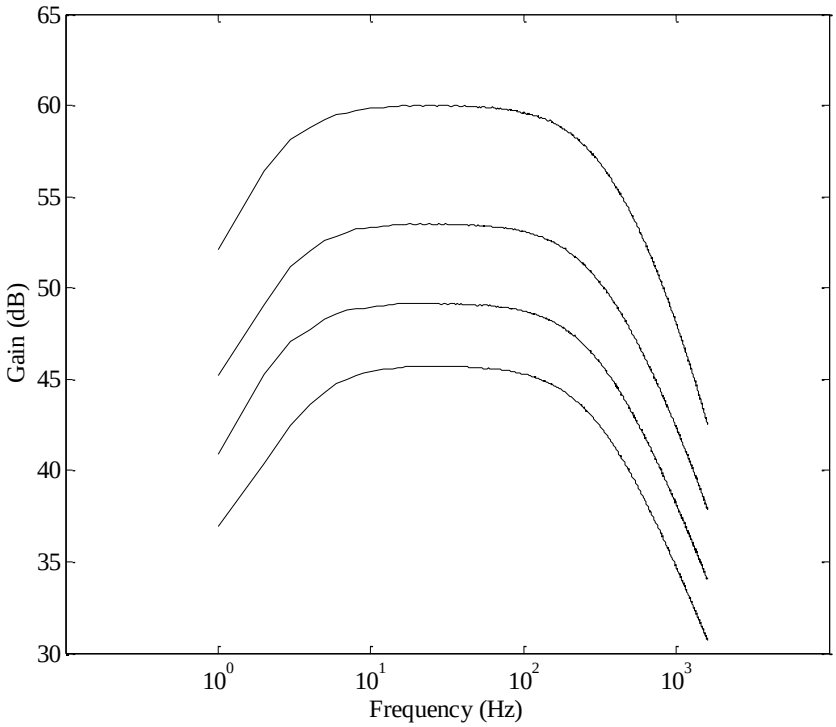


Figure 3.28 System gain adjustment with consistent bandwidth (one bandwidth setting is chosen for illustration).

#### *3.4.2.2 Input Referred Noise*

The input referred noise of the TB-FEA, measured using the Agilent Dynamic Signal Analyzer 35670A, with the maximum bandwidth is shown in Figure 3.29. The large gate area of the input transistors suppresses the flicker noise effectively, resulting in a low flicker noise corner frequency of several hertz. The thermal noise floor of the TB-FEA is around 120nV/√Hz, which is quite close to the simulation result. The *rms* value of the input referred noise can be obtained by integrating under the spectrum curve of the output noise to infinite and then dividing by the voltage gain of the amplifier. However, this method is impractical since it is difficult to plot the spectrum of the output noise to infinite frequency due to the limitations of the measurement instrument. Another approach to calculate the *rms* value of the input referred noise is integrating the spectrum curve of the input referred noise in Figure 3.29 across the equivalent noise bandwidth $f_{n,eq}$ given by

$$f_{n,eq} = \frac{\pi}{2} f_{-3dB,TB-FEA} \approx 460\text{Hz}. \tag{32}$$

The *rms* value of the input referred noise is 2.5 μV integrated from 0.05Hz to 460Hz.

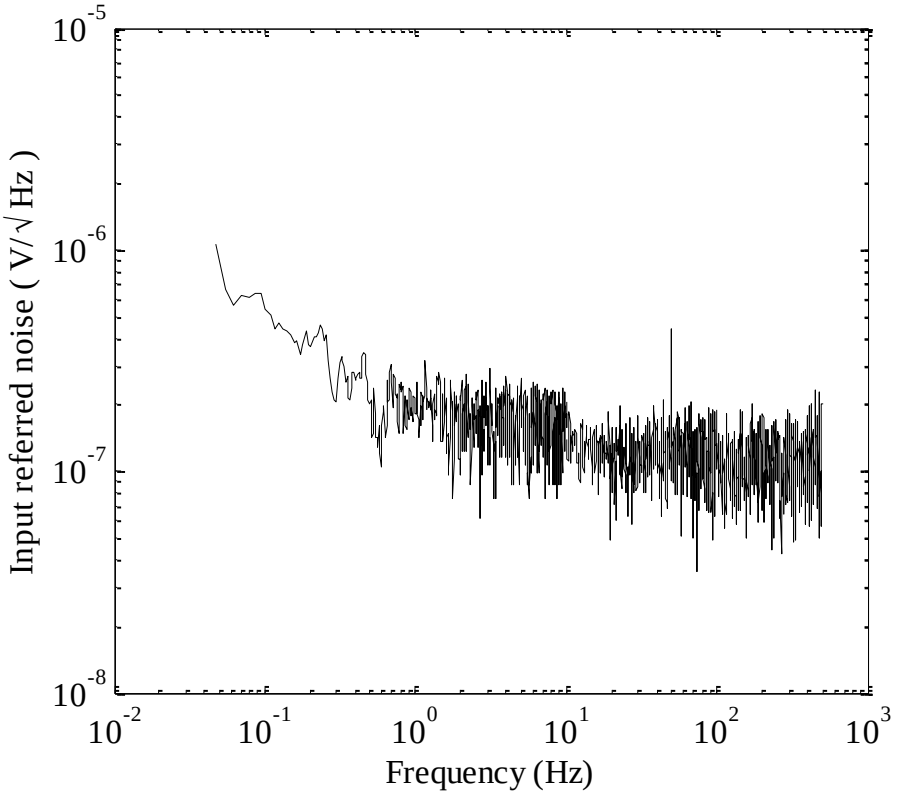


Figure 3.29 Input referred noise of the TB-FEA.

The parameter NEF is also adopted here to measure the noise to power trade-off of the TB-FEA. The state-of-the-art designs have demonstrated NEF in the range of 3.8 to 13 [11, 12, 15, 21, 31, 81]. Due to the high transconductance efficiency and large gate area of the input pair transistors, the NEF of this design reaches 3.26, which is among these lowest values published to date.

#### *3.4.2.3 Total Harmonic Distortion (THD)*

The THD was recorded using Agilent Dynamic Signal Analyzer 35670A with highest resolution setting, and the input signal was provided by ultra low distortion function generator (Stanford research systems, model DS360). The measured THD against the

output amplitude of the analog front-end for different high-pass cutoff frequencies is plotted in Figure 3.30. Since most of the signal degradation occurs at the tunable pseudo-resistors which have non-linear operation characteristic, the THD for different high-pass corner frequencies were tested. In Figure 3.30, the cutoff frequency for each curve from upper to lower is 3.6Hz, 2.2Hz, 1.4Hz, 0.25Hz, and 4.5mHz, respectively. It is seen that the maximum THD occurs when the high-pass corner frequency is set at 3.6Hz, where the resistance of the tunable pseudo-resistor reaches its minimum. The THD at this worst case is less than 0.6% even when the PGA approaches rail-to-rail output swing.

The excellent THD performance is a result of the balanced tunable pseudo-resistor that reduces the signal distortion in the feedback path. It is obvious from Figure 3.30 that the THD improves consistently when the high-pass cut-off frequency decreases. This is because with the increase of the tunable resistance, the feedback path is becoming dominated by the feedback capacitor, which was implemented by passive elements and has much better linearity than the non-linear tunable pseudo-resistor. For large resistance settings such as at 0.25Hz and 4.5mHz cut-off frequencies with the output amplitude smaller than 0.9V, most of the harmonic peaks are buried under the noise floor (around -85dB) and cannot be extracted. In this output range, the actual THD performance are expected to be better than the measured numbers since they are limited by the relatively high noise floor. So the result in Figure 3.30 is THD+noise curve, and the Y axis label should be THD+noise. However, it is not common to state THD+noise in %, so only THD is labeled in Figure 3.30. This leads to continuously decreasing THD readings in this output range due to the improved signal to noise ratio (SNR). Even though it is affected by the high noise floor, the THD performance is

still quite good compared to the state-of-the-art designs, especially for large output amplitude.

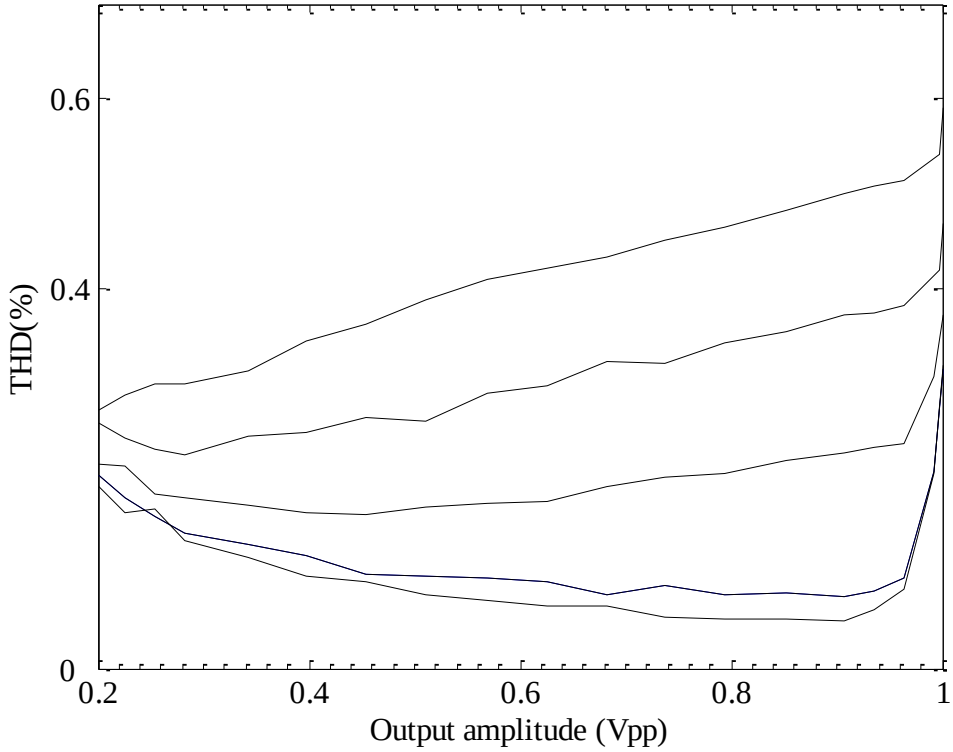


Figure 3.30 Total harmonic distortion of the analog font-end vs. output amplitude.

#### *3.4.2.4 System Benchmarks*

Table 4 summarizes the measured performance of the sensor interface chip. The proposed design shows improvements in various aspects. The TB-FEA achieves a NEF of 3.26, which is among the lowest values reported to date, indicating an optimum noise-to-power trade-off. Design in [43] achieves a slightly better NEF of 3.21 than the proposed design since it was fabricated using 0.5μm CMOS process,

which has better noise performance than 0.35μm CMOS process. Detailed explanations will be given in the next section.

Table 4. Performance comparison between the fully configurable ECG chip and other state-of-the-art designs.

| Parameter | Design in [11] | Design in [43] | Design in [15] | Design in [31] | This work |
|---|---|---|---|---|---|
| Supply Voltage | ±1.7V | 2.8V | 1V | 1.8 ~ 3.3V | 1V |
| Process Technology | 1.5μm CMOS | 0.5μm CMOS | 0.35μm CMOS | 0.8μm CMOS | 0.35μm CMOS |
| Current (TB-FEA) | 8μA | 743nA | 330nA | 1μA | 33~337nA |
| Midband Gain | 39.3/45.6dB | 40.9dB | 40.2dB | 41/50.5dB | 45.6/49/53.5/ 60dB |
| High-pass corner frequency | 0.015Hz ~700Hz | 0.392Hz (Tunable) | 0.003Hz (Fixed) | 0.05/0.4/2.5Hz | 4.5mHz~3.6Hz |
| Low-pass corner frequency | 40/400/3k/ 4k Hz | 295Hz (Tunable) | 245Hz (Fixed) | 120Hz (Fixed) | 31~292Hz |
| Input Referred Noise | 3.6μ$V_{rms}$ (20~10k Hz) | 1.66μ$V_{rms}$ (0.2~1k Hz) | 2.7μVrms (0.05~250Hz) | 0.95μ$V_{rms}$ (0.05~100Hz) | 2.5μ$V_{rms}$ (0.05~460Hz) |
| Noise Efficiency Factor | 4.9 | 3.21 | 3.8 | 4.6 | 3.26 |
| Output Swing @ 1% THD | ~ 48% Full Swing | ~ 29% Full Swing | ~ 85% Full Swing | 0.1% @5mV input | 100% Full Swing |
| CMRR | N/A | 66 dB (0.392~295Hz) | 64dB (1~250Hz) | 80dB/100dB | ≥ 71.2dB (≤300Hz) |
| PSRR | N/A | 75dB (392~295k Hz) | 62~63dB (1~250Hz) | N/A | ≥ 84dB (≤300Hz) |
| Total Power Consumption (with ADC) | 27.2 μW (Amplifier only) | 2.08μW (Amplifier only) | 2.3 μW | 2μW (Amplifier only) | 445nW~895nW |

To conserve power, different acquisition modes can be selected according to target applications. For example, the chip can operate in two modes in an ECG device. Under the narrowband mode for heart rate detection, the system bandwidth is set to 31Hz and the digitization module is set at low power less precise mode, the overall chip consumes only 445nA. Under the wideband mode for ECG data recording, the bandwidth is adjusted to 292Hz and a high precise crystal oscillator is used for the ADC, which increases the total current consumption to 895nA. The system power distributions among all these functional blocks for the two modes are shown in Figure 3.31.

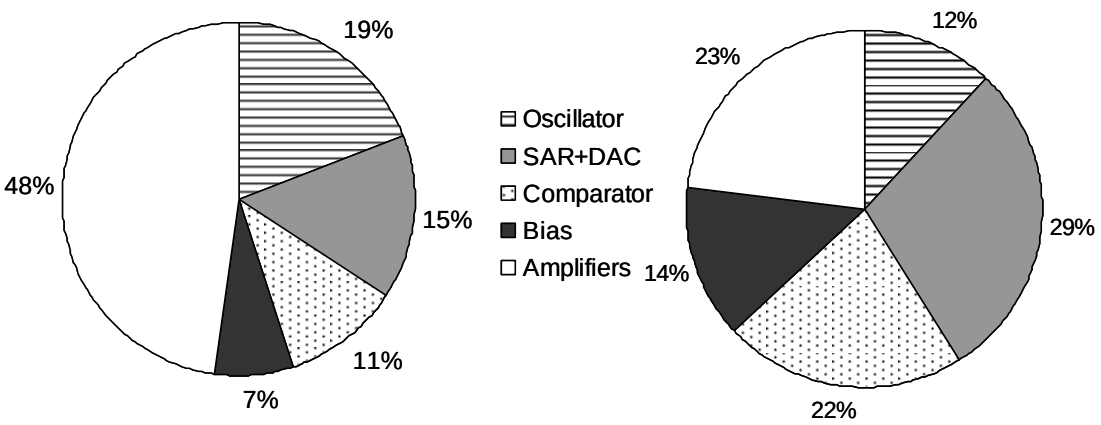


Figure 3.31 System power distributions for (a) wideband mode and (b) narrow band mode.

The flexible mode control scheme allows maximum utilization of the tight power budget in a wireless biomedical sensor node. The ultra low-power consumption of sub-μW for the overall system indicates a fully optimized system structure, which ensures the possibility of portable/implantable use and long term monitoring. To demonstrate the functionality of the chip, a human ECG signal captured using the developed prototype chip is shown in Figure 3.32. It is the recovered waveform after

ADC without any other additional filters. It shows the QRS, P and T waves clearly. The gain of the amplifier is set at 200 and the pass-band of the amplifier is from 4.5m Hz to 292 Hz. Standard Ag/AgCl monitoring electrodes with foam tape and sticky gel were used for the ECG signal acquisition.

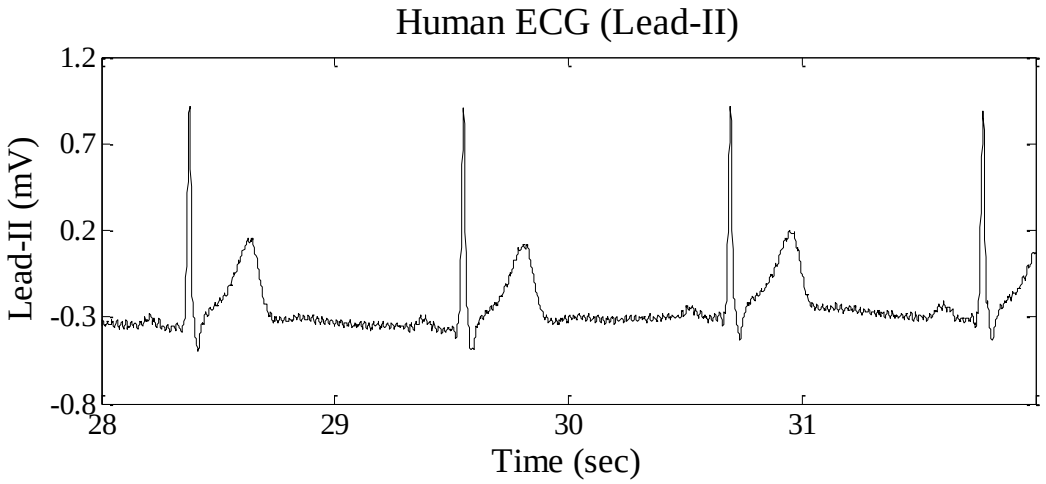


Figure 3.32 Recorded human ECG by the prototype chip.

## 3.5 Discussion on Technology Selection

### 3.5.1 Design Considerations

In order to investigate the performance of the amplifier with different process technologies, a low noise front-end amplifier was implemented using IBM 0.13μm CMOS process. Besides the issues existing in the 0.35μm process, there are many other design considerations that need to take care of for 0.13μm process technology. First of all, the degraded noise performance is one of the major concerns for 0.13μm technology, as the flicker noise of the CMOS devices will increase with the scaling down of the minimum transistor size. It has been reported that the flicker noise or 1/f noise spectrum is inversely proportional to $L_{g(min)}{}^3$, where $L_{g(min)}$ is the minimum drawn gate length of the process [82, 83]. Scaling down the $L_{g(min)}$ will greatly increase the flicker noise at low frequency band [84]. Meanwhile, there are studies showing that the use of nitrided oxides in the more advanced technologies will increase the flicker noise in MOSFETs through the introduction of interface traps [85-87]. In addition, as the thickness of the oxide layer decreases in 0.13μm technology, the direct tunneling current yields a non-negligible gate leakage current, which may further degrade the noise performances [88]. As a result, the significantly increased flicker noise in 0.13μm technology gives raise a great challenge to the low noise biomedical sensor interface circuits design. In order to compare the performance of this design to the one implemented using 0.35μm technology fairly, the chopper stabilized amplifier will not be adopted here, either. As a result, a larger gate area for the input pair transistors may be necessary to suppress the flicker noise.

For the implementation of the high-pass filter in the previous section, an ultra small control current is generated to control the pseudo-resistor and tune the high-pass corner frequency of the filter. However, the same design scheme may not hold for the 0.13μm process since the subthreshold leakage current increases significantly, which is larger than the control current of the pseudo-resistor. As a result, the ultra large resistance value is not achievable using the same biasing topology. This requires new biasing circuits in order to push the high-pass corner frequency below 1Hz.

With the decrease of the threshold voltages of 0.13μm process, the supply voltage needs to scale down in order to minimize the power consumption further more. In this design, the target supply voltage is set at 0.6V. However, the open loop gain of the amplifier reduces with the decrease of the supply voltage. When implementing in close loop configuration, the insufficient open loop gain will lead to inaccurate close loop gain and degraded performance of the front-end amplifier. Hence, gain boosting technique may need to apply to the front-end amplifier in order to achieve high enough open loop gain.

### 3.5.2 Circuits Implementation

Capacitive feedback and pseudo-resistors provide optimum solution for the low power low noise front-end amplifier design. This feedback topology is also adopted in this design. The schematic of the low noise front-end amplifier embedded with a band-pass filter is shown in Figure 3.33. The same tunable pseudo-resistor structure is employed to reject the DC component induced by the electrode-skin interface. In order to leave the low frequency component of the biological signal unaffected, the

corner frequency of the high-pass filter needs to be less than 1Hz. However, the subthreshold leakage current of the target 0.13μm technology is much larger, where the leakage current is greater than the control current of the pseudo-resistors. As a result, the previous biasing topology cannot achieve high enough resistance even when all the 3 bits high-pass control voltages $Ctrl_{HPF1}$ ~$Ctrl_{HPF3}$ at Figure 3.15 are set to low. According to the simulation, the minimum high-pass corner frequency appears at several hertz, and the ultra low cut-off frequency of sub-one hertz is not achievable using the existing biasing scheme.

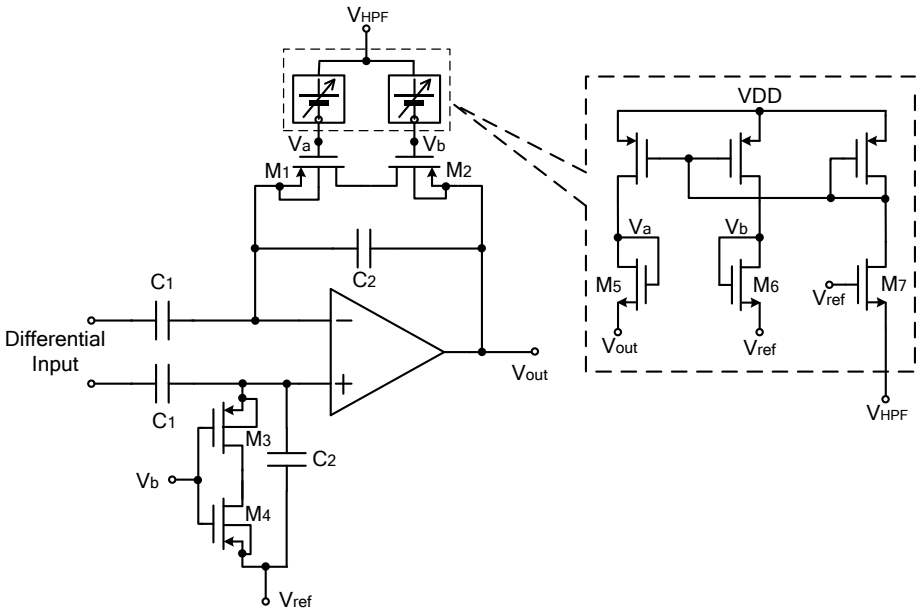


Figure 3.33 Schematic of the low noise front-end amplifier using 0.13μm technology.

According to the discussion above, the problem is due to the high subthreshold leakage current which overruns the control current of the pseudo-resistors. To solve this problem, a new biasing topology for the pseudo-resistors is proposed in this design, as shown in Figure 3.33. The P-type pseudo-resistors are biased by N-type transistors $M_5$ and $M_6$, thus the four pseudo-resistors $M_1$~$M_4$ are always reverse

biased. This will effectively reduce the leakage current and thus ultra high resistances are achievable. The high-pass corner frequency of the front-end amplifier is continuously tunable by changing the control voltage $V_{HPF}$. The gate voltage of transistor $M_7$ is fixed at $V_{ref}$, which is equal to half VDD. When $V_{HPF}$ is smaller than $V_{ref}$ and moving from $V_{ref}$ to 0V, transistor $M_7$ is forward biased and enters subthreshold or saturation region. The $v_{gs}$ of $M_5$ and $M_6$ increases due to the increasing current passing through them. The reverse bias voltage applied on these pseudo-resistors is equal to $v_{gs}$ of $M_5$ and $M_6$. As a result, a smaller $V_{HPF}$ will lead to further reverse bias of the pseudo-resistors and hence higher resistance value and lower high-pass corner frequency. When the control voltage $V_{HPF}$ is greater than $V_{ref}$, transistor $M_7$ is reverse biased, and $v_a \approx v_{out}$ and $v_b \approx V_{ref}$. The current passing through $M_5$ and $M_6$ now is only the leakage current and mainly depends on the aspect ratio of the two transistors. By doing so, transistor $M_7$ can be both forward and reverse biased by tuning $V_{HPF}$ from 0V to VDD, and thus the tunable range of the pseudo-resistors are enlarged. The smallest resistance value occurs when transistor $M_7$ is reversed biased. That is to say, the highest high-pass corner frequency depends on the leakage current of the 0.13μm technology. The simulation result indicates that the leakage current of the target technology allocates the high-pass corner frequency at several hertz. This gives the high-pass corner frequency an enough tunable range, so that the developed low noise amplifier satisfies the bandwidth requirement for ECG recordings and is capable to be reconfigured for different applications.

Besides the subthreshold leakage current, the pseudo-resistor faces another challenge. The leakage current is noticeable in 0.13μm technology and the junction leakage current induces unbalance to the pseudo-resistors. The unavoidable junction leakage

current leads to DC voltage shift at the output of the front-end amplifier for large amplitude output signals, even though fully balanced pseudo-resistor structure is employed. The THD performance is also degraded, especially for large output swing, which will induce higher junction leakage current. As a result, rail-to-rail output swing with less than 1% THD may not be possible. However, the THD performance is still competitive compared to the state-of-the-arts designs thanks to the proposed fully balanced pseudo-resistor topology.

In order to minimize the power consumption of the front-end amplifier, the target of the supply voltage is set at 0.6V in this design. Under such low supply voltage, it is difficult to get high enough open loop gain for the OTA. Besides, for low voltage design, rail-to-rail output swing is crucial for the front-end amplifier in order to enhance the dynamic range of the system. As a result, a two-stage Miller compensation OTA is employed in the front-end amplifier as illustrated in Figure 3.34. The first stage adopts cascaded transistors $M_3$ ~ $M_6$ to enhance the voltage gain. Besides this, further gain boosting technique is also adopted with a nested OTA, which is formed by transistors $M_{12}$ ~ $M_{16}$. The overall gain of the OTA can be estimated by the following equation,

$$A_v = g_{m1,2}\left[(1+A_1)g_{m3,4}r_{o3}r_{o1} \parallel g_{m,5,6}r_{o5}r_{o7}\right](g_{m10}+g_{m11})(r_{o10} \parallel r_{o11}). \quad (33)$$

$A_1$ here is the open loop gain of the nested OTA, which is expressed by the equation below,

$$A_1 = g_{m12,13}(r_{o12} \parallel r_{o14}). \quad (34)$$

It boosts the gain of the OTA by amplifying the output impedance of the first stage as indicated in Eq. (34). By doing so, the simulated open loop gain of the OTA is nearly 80dB, promising a reliable performance for the close loop amplifier. $C_1$ is the Miller compensation capacitor which determines the dominant pole of the OTA and thereby sets the -3dB low-pass corner frequency of the close loop amplifier. Similar push-pull output stage is employed to enhance the driving capability of the amplifier with minimum quiescent current.

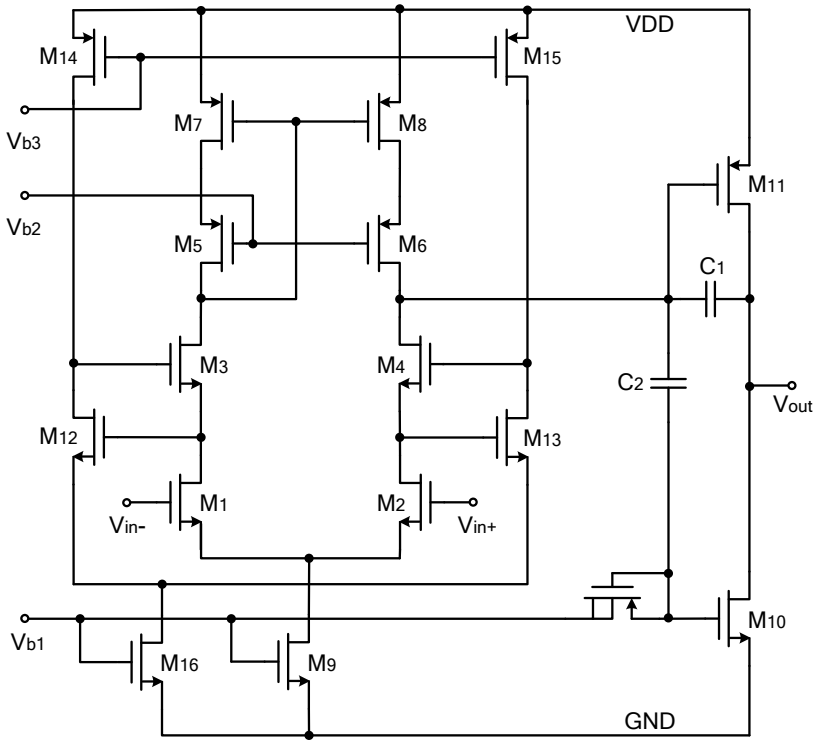


Figure 3.34 Schematic of the OTA implemented using 0.13μm technology.

To investigate the noise performance of the proposed OTA, the input referred thermal noise contributed by each transistor of the OTA is analyzed as follow:

vi) M1 & M2:

$$\overline{v_{n1,2}^{\ 2}} \approx 2 \times 4kT \frac{2}{3} \frac{1}{g_{m1,2}};$$

vii) M3 & M4:

$$\overline{v_{n3,4}^{\ 2}} \approx 2 \times 4kT \frac{2}{3} \frac{g_{m3,4}}{(1+g_{m3,4}r_{o1})^2 g_{m1,2}^{\ 2}};$$

viii) M5 & M6:

$$\overline{v_{n5,6}^{\ 2}} \approx 2 \times 4kT \frac{2}{3} \frac{g_{m5,6}}{(1+g_{m5,6}r_{o7})^2 g_{m1,2}^{\ 2}};$$

ix) M7 & M8:

$$\overline{v_{n7,8}^{\ 2}} \approx 2 \times 4kT \frac{2}{3} \frac{g_{m7,8}}{g_{m1,2}^{\ 2}};$$

x) M10:

$$\overline{v_{n10}^{\ 2}} \approx 4kT \frac{2}{3} \frac{g_{m10}}{[(g_{m1,2}R_{out1}(g_{m10}+g_{m11})]^2},$$

where $R_{out1} = (1+A)g_{m3,4}r_{o3}r_{o1} \parallel g_{m5,6}r_{o5}r_{o7}$;

xi) M11:

$$\overline{v_{n11}^{\ 2}} \approx 4kT \frac{2}{3} \frac{g_{m11}}{[(g_{m1,2}R_{out1}(g_{m10}+g_{m11})]^2},$$

where $R_{out1} = (1+A)g_{m3,4}r_{o3}r_{o1} \parallel g_{m5,6}r_{o5}r_{o7}$;

xii) M12&M13:

$$\overline{v_{n12,13}^{\ 2}} \approx 4kT \frac{2}{3} \frac{1}{g_{m13,14}(g_{m1,2}r_{o1})^2};$$

xiii) M14&M15:

$$\overline{v_{n14,15}^{\ 2}} \approx 4kT \frac{2}{3} \frac{g_{m14,15}}{(g_{m13,14}g_{m1,2}r_{o1})^2}.$$

The two current sinks $M_9$ and $M_{16}$ do not contribute any noise to the circuit theoretically. So the total input referred thermal noise of the OTA at DC is the sum of the above individual terms applying superposition theorem. From the above equations, we can see that most of the thermal noise comes from the input pair transistors $M_1$ and $M_2$. The noise contributed from $M_7$ and $M_8$ is also remarkable. The cascaded transistors, output stage and the nested OTA generate much smaller noise and their effect on the total noise performance can be neglected. Compared to the low noise OTA in Figure 3.20, the thermal noise performance of this OTA is not degraded much even though many transistors are added for gain boosting purpose. Maximizing the transconductance of the input pair is the most effective and straight way to minimize the input referred noise of the OTA. Meanwhile, the transconductances of the current sources $M_7$ and $M_8$ are designed as small as possible to further lower down the noise floor.

It is believed that PMOS devices exhibit less flicker noise than NMOS transistors. Nonetheless, this difference between PMOS and NMOS transistors is not consistently observed [89]. According to the preliminary simulation results, the PMOS transistors in this process technology do not have better flicker noise performance, but give higher thermal noise floor due to their weak transconductance. As a result, NMOS transistors input pair is still adopted in this design. The flicker noise of the OTA is suppressed by using large gate area for the input transistors and the current sources $M_7$ and $M_8$.

### 3.5.3 Measurement Results

The design was fabricated using IBM 0.13μm process and tested under 0.6V supply voltage. The threshold voltages of the CMOS and PMOS devices vary from 0.2V to 0.5V depending on the channel length of the transistors, where long channel devices possess lower threshold voltage according to the simulation results. In this design, relatively long channel transistors are adopted to minimize the flicker noise and transistors mismatch, thus that the threshold voltages of these transistors fall around 0.2V. The microphotograph of the chip is shown in Figure 3.35. The top layer of the layout was filled with dummy metals according to the process requirements. As a result, only capacitors can be seen from the microphotograph.

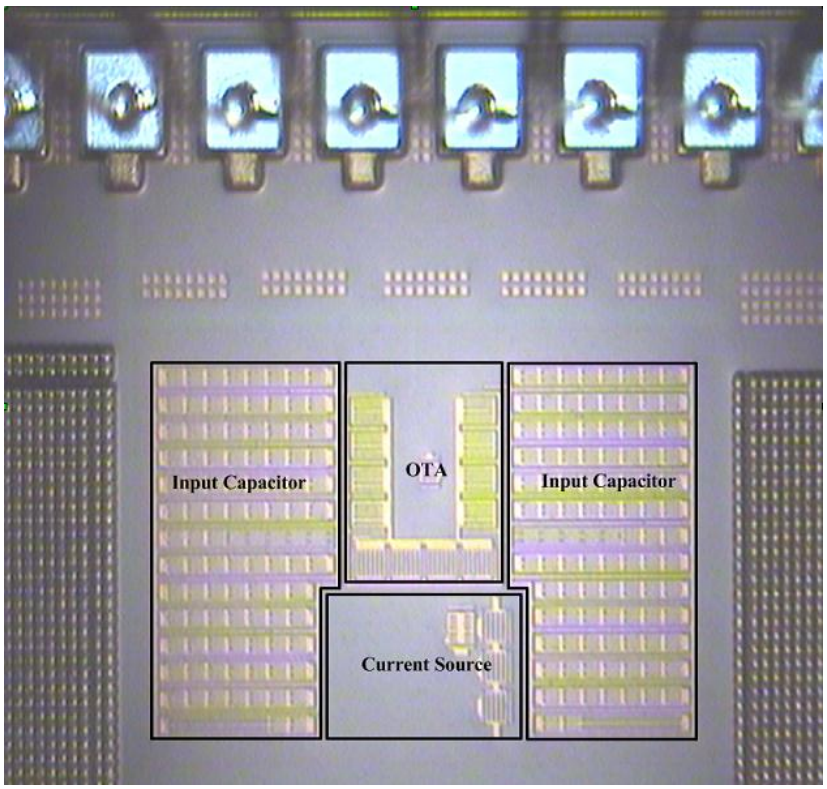


Figure 3.35 Microphotograph of the chip fabricated using 0.13μm technology.

The frequency responses of the front-end amplifier are shown in Figure 3.36. The mid-band gain of the low noise amplifier is about 39.6dB and the -3dB corner frequency of the high-pass filter is continuously tunable with the control voltage $V_{HPF}$ as shown in the plot. The lowest high-pass cut-off frequency appears at 0.03Hz when the pseudo-resistors are severely reverse biased. With the increase of the control voltage $V_{HPF}$, the high-pass corner frequency moves right and the highest -3dB frequency is approximately 4Hz, which is determined by the subthreshold leakage current of the process technology. This measurement result is consistent with the simulation result, and the tunable range of the high-pass corner frequency is broad enough for biomedical applications.

The measured low pass corner frequency of the front-end amplifier is approximately 250Hz, tailored for ECG recordings. In Figure 3.36, a little excursion of the low pass -3dB frequencies is observed for different $V_{HPF}$. This is because varying $V_{HPF}$ changes the DC current in the biasing circuits of the pseudo-resistors. Part of these biasing current is drawn from the output stage of the OTA as shown in Figure 3.33. Even though the biasing current of the pseudo-resistors are very tiny, it still alters the low pass corner frequency slightly due to the small quiescent current in the output stage of the OTA. However, the slight changes in the low pass corner frequency will not affect the performance of the low noise front-end amplifier and can be neglected.

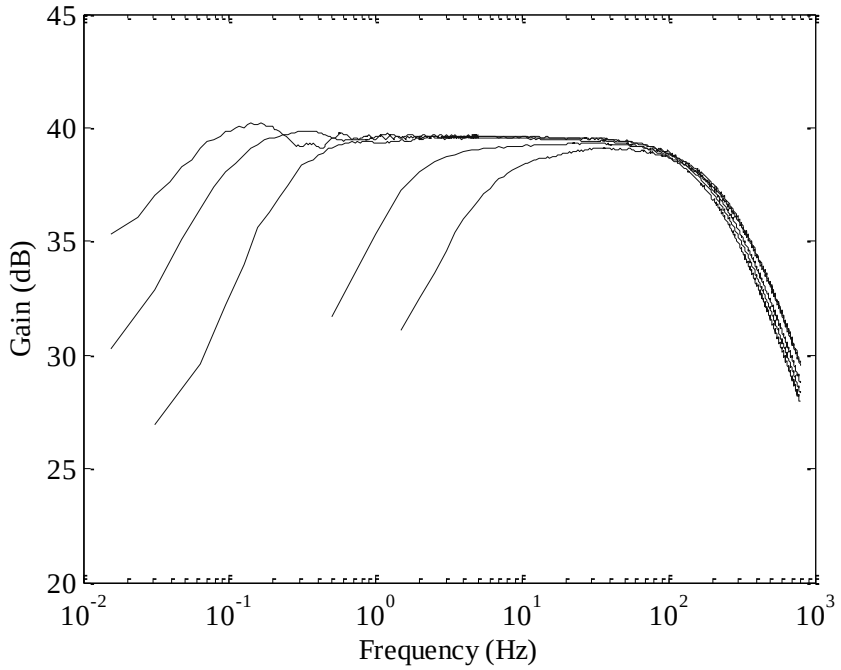


Figure 3.36 Frequency responses of the front-end amplifier fabricated using 0.13μm technology.

The input referred noise of the low noise amplifier is plotted in Figure 3.37. It is obvious that the flicker noise of the amplifier is dominant in the low frequency range, where the corner frequency of the flicker noise appears at about few hundred hertz, even though the input transistors of the amplifier were designed with very big gate area. This is because the thinner gate oxide in the 0.13μm technology increases the flicker noise. The *rms* value of the input referred noise is 2.73μV when integrated from 0.1Hz to 300Hz.

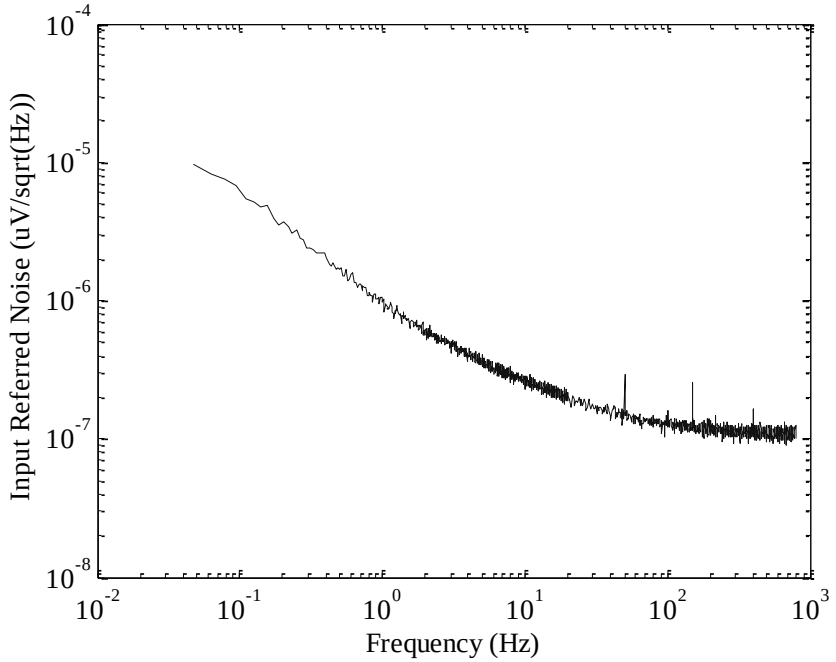


Figure 3.37 Input referred noise of the front-end amplifier fabricated using 0.13μm technology.

### 3.5.4 Comparison with design in 0.35μm technology

The performance of the low noise amplifier implemented using 0.13μm CMOS technology is compared with the one realized using 0.35μm CMOS technology. The performances of the two low noise front-end amplifiers are summarized in Table 5, named as Amplifier I for 0.35μm technology and Amplifier II for 0.13μm technology, respectively. Both of the two amplifiers were designed for ECG recordings, thus their gain and bandwidth are more or less the same. The biggest advantage of Amplifier II is that it is able to operate under lower supply voltage due to the lower threshold voltages of the transistors in 0.13μm CMOS technology. However, the noise figure of Amplifier II is higher than amplifier I even though more current was allocated to amplifier II. This is mainly because of the raised flicker noise corner frequency in

0.13μm CMOS technology. The degraded noise performance makes it not preferable for low noise amplifier design. One may note that the power supply rejection ratio (PSRR) of Amplifier II is much lower than Amplifier I. This is mainly caused by the outstanding short channel effect of the transistors in 0.13μm technology, where the drain current of the transistor changes remarkably with its drain-source voltage ($v_{ds}$). Although the overall performance of the 0.13μm design is not as good as the one built in 0.35μm technology, it is necessary to explore further on the designs with 0.13μm and below technologies if a system-on-chip wireless biomedical sensor is targeted.

Table 5. Performance summary of the low noise front-end amplifier implemented using 0.13μm technology.

| | Amplifier I | Amplifier II |
|---|---|---|
| Process technology | 0.35μm CMOS | 0.13μm CMOS |
| Supple voltage | 1V | 0.6V |
| Current dissipation | 337nA | 490nA |
| Midband gain | 45.6dB | 39.6dB |
| Lower -3dB frequency | 4.5mHz ~3.6Hz (Tunable) | 27mHz ~ 4Hz (Tunable) |
| Higher -3dB frequency | 31 ~ 292Hz | 250Hz |
| Input referred noise | 2.5μVrms (0.05 ~ 460Hz) | 2.73μVrms (0.1 ~ 300Hz) |
| NEF | 3.26 | 5.32 |
| THD | 0.06% (@ 25% output swing) | 0.1% ( @ 25% output swing) |
| CMRR | > 71.2dB | > 60dB |
| PSRR | > 84dB | > 42dB |
| Total power consumption | 337nW | 414nW |

# CHAPTER 4

# DESIGN OF ANALOG FRONT-END IC FOR EEG RECORDINGS

## 4.1 Design Considerations

An Electroencephalography (EEG) is a test that measures and records the electrical activities along the scalp produced by the firing of neurons within the brain [90]. EEG is the most useful and important test in confirming a diagnosis of epilepsy, as epileptic activity can create clear abnormalities on a standard EEG study [91]. Besides this, EEG is also applied in the diagnosis of comma, encephalopathies and brain death. A routine clinical EEG recording typically lasts 20-30 minutes. However, such an EEG recording may not be able to provide sufficient information in some situation, especially when it is necessary to record a patient while a seizure is occurring, as the recording of an actual seizure can give significantly better information for the diagnosis. In this case, the EEG of this patient needs to be constantly recorded for days or even weeks. As the traditional bulky and wiry device will give the patient under monitoring great inconvenience on daily life for such a long time monitoring, implantable intracranial EEG monitoring is needed. According to the international federation of clinical neurophysiology (IFCN) standards, at least 24 channels, and preferably 32 channels of recording EEG is necessary [48]. Meanwhile, the amplitude of the EEG signal is quite weak, typically in the range of 25-100 μV [5]. Thereby, a high voltage gain of 1000 and above is essential. These impose a strict power and area

requires to the design of the implantable EEG sensor interface IC. The design target of some key parameters for this EEG recording chip is summarized in Table 6.

Table 6 Design target for the EEG recording front-end circuits.

| Specification | Value | Remarks |
|---|---|---|
| Supply voltage | 1V | 0.35μm CMOS process |
| No. of channels | 32 | IFCN standards |
| Average current/channel | < 1μA | Including ADC |
| Amplifier current | < 400nA | Front-end amplifier only |
| Gain | 1000~5000 | Programmable gain |
| Input referred noise | < 1.5$\mu V_{rms}$ | Integrated in the signal band |
| High-pass corner frequency | < 0.5Hz | No external components |
| Low-pass corner frequency | 150Hz | Tunable |
| THD | < 1% | @ 80% output swing |
| Channel isolation | > 80dB | Adjacent channels |
| Average area per channel | < 0.4$mm^2$ | As small as possible |

## 4.2 System Architecture

According to the implant requirement in [38], the input referred noise for implantable EEG device is less than 1.5$\mu V_{rms}$. This figure is achievable with normal amplifier structure according to the previous experience, thus the chopper stabilized instrumentation amplifier [18, 38] is not employed in this design. Figure 4.1 shows the system architecture of the proposed chip (only the designs in the analog part are included in this project, the circuits from the multiplexer rightward were developed by

other team member). It consists of 32 analog front-end blocks, a 32-to-1 multiplexer, a 10-bit SAR ADC and a reference generator. Each of the analog front-end blocks was implemented using three cascaded stages. The first stage is a low noise front-end amplifier with integrated high-pass function. The second stage acts as a tunable low-pass filter while providing programmable gain. The last stage uses a wide bandwidth unity gain buffer with high slew rate to drive the multiplexer in order to achieve an acceptable tracking error. The proposed architecture differs from existing biomedical sensor interface chips in which single or twin-amplifier structure is commonly used to conserve power [15, 17, 92]. Fewer amplifiers do not necessarily lead to optimum design in terms of power and chip area, especially for multi-channel applications. In conventional biomedical systems, the low-pass function is usually integrated with the front-end amplifier [12, 17], and the -3dB corner frequency of the overall system is determined by

$$f_{-3dB} = \frac{g_m}{C_C \cdot A_V}, \tag{35}$$

where $g_m$ is the transconductance of the input pair, $C_C$ is the load capacitance or Miller compensation capacitance and $A_V$ is the midband gain of the front-end amplifier. Since the noise figure of the front-end amplifier is inversely proportional to $g_m$ of the input pair, a low noise floor requires a largest possible $g_m$. For a specific application, $A_V$ is relatively fixed according to the amplitude of the target signal and the supply voltage. As a result, a large $C_C$ is necessary if the low-pass corner frequency is set at several hundred hertz. For EEG recording, the cut-off frequency is less than 150Hz [38], which leads to a large compensation capacitance of tens of pF. These capacitors take up large silicon area for multi-channel design.

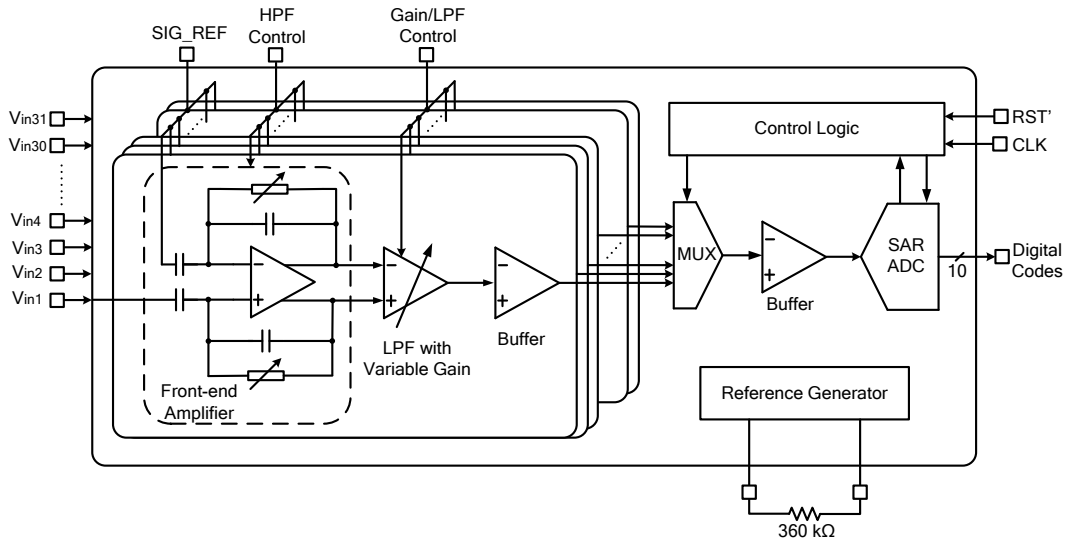


Figure 4.1 System architecture of the 32-channel EEG recording IC.

In the proposed system architecture, we avoid using large $C_C$ by separating the role of noise suppression and low-pass function. The first stage is dedicated to noise suppression which uses largest possible $g_m$ without a compensation capacitor. Its bandwidth may go as high as several kilo hertz due to the large $g_m$. However, this will not affect the performance of the overall system, as the low-pass filter is realized at the second stage, where its noise is insignificant to the overall system's noise figure. Thereby a small $g_m$ is adequate. As a result, the size of the compensation capacitor is reduced by 85% compared to the design in [17] and the total area of the overall system decreases significantly.

Another advantage of the proposed system architecture is its flexibility in balancing system performance and power efficiency. For example, almost all the current of the front-end amplifier is devoted to achieve low input referred noise, without worrying about other trade-offs, such as area, gain or bandwidth. While for the unity gain buffer, a wide bandwidth is implemented at lowest possible current to reduce the tracking

error without considering the gain requirement. In this way, each stage serves a particular purpose without compromising on other system parameters. This leads to better system partition and optimal power distribution.

## 4.3 Circuits Implementations

### 4.3.1 Low Noise Front-end Amplifier

The schematic of the low noise front-end amplifier is shown in Figure 4.3. It employs capacitance feedback and a fully differential OTA. Fully balanced tunable pseudo-resistors [17] were implemented in the feedback loop to achieve high dynamic range and low signal distortion. The high-pass corner frequency of the front-end amplifier is continuously tunable to meet the requirements of different applications. It is well known that capacitor is very area-consuming. For multi-channel design, the area of each individual circuit block becomes more and more critical in order to reduce the chip size and lower the cost of mass production. In order to minimize the total area of the overall system, the input capacitance of the front-end amplifier should be designed as small as possible. However, smaller capacitance may result in poor CMRR since it is difficult to get good matching of the positive and negative feedback paths during fabrication. Furthermore, the thermal noise floor of the amplifier will go up if the size of capacitor $C_1$ reduces, according to the following equation,

$$v_{in,amp} = v_{in,OTA} \cdot \left( \frac{C_1 + C_2 + C_{in}}{C_1} \right) = v_{in,OTA} \cdot \left( 1.01 + \frac{C_{in}}{C_1} \right). \quad (36)$$

$C_{in}$ is the input capacitance of the OTA, which is generated by the parasitic capacitance of the input pairs. According to Eq. (36), smaller $C_1$ will results in

degraded noise performance of the front-end amplifier. In this design, a capacitance of about 6pF is selected for $C_1$ to achieve better noise to area balance, thus that the silicon area of the overall system is relatively small while the input referred noise of the front-end amplifier is restricted to an acceptable level for EEG recordings. To improve the CMRR, the layout of the feedback network is carefully plotted and common-centriod layout scheme is applied to the input capacitors in order to improve the matching problem.

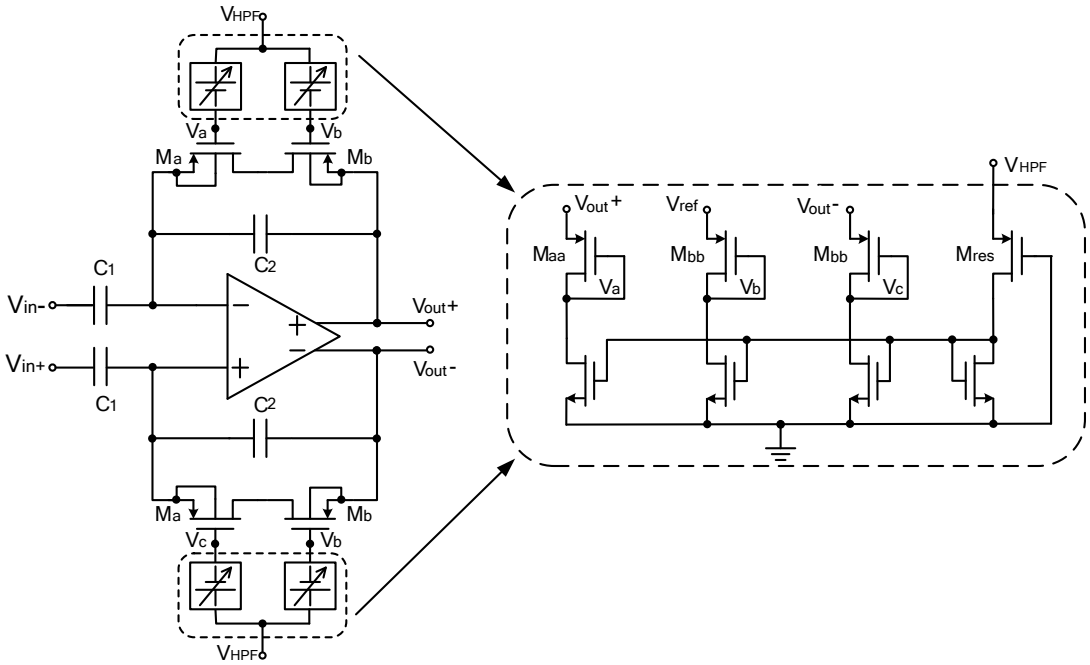


Figure 4.2 Schematic of the low noise front-end amplifier for EEG recordings.

The OTA employed in the low noise front-end amplifier is shown in Figure 4.3. In order to achieve better noise to power trade-off, both NMOS and PMOS transistors are employed as the input pairs of the OTA which increases $g_m$ and lowers the thermal noise floor. All 4 input transistors operate in sub-threshold region to achieve high transconductance efficiency ($g_m/I_d$). Flicker noise plays a very important role in the

total input referred noise for low frequency application. In this design, the flicker noise is suppressed by large gate area of the input transistors. However, increasing the size of the input transistors will give penalty to the thermal noise performance of the front-end amplifier. According to Eq. (36), large input transistor means large $C_{in}$ and thereby high thermal noise floor. This effect is prominent especially when the input capacitance $C_1$ is designed to be relatively small in order to get compact chip size. Even though flicker noise is the dominant factor for the total input referred noise in EEG recording applications, raising thermal noise level still degrades the noise figure remarkably. As a result, balancing the contributions from flicker noise and thermal noise becomes one of the most important tasks in the low noise front-end amplifier design. The input PMOS pair and NMOS pair are designed with W/L= 220/0.8 and 540/1.5, respectively, thus that the sum of the flicker noise and the thermal noise is minimized according to the simulation result.

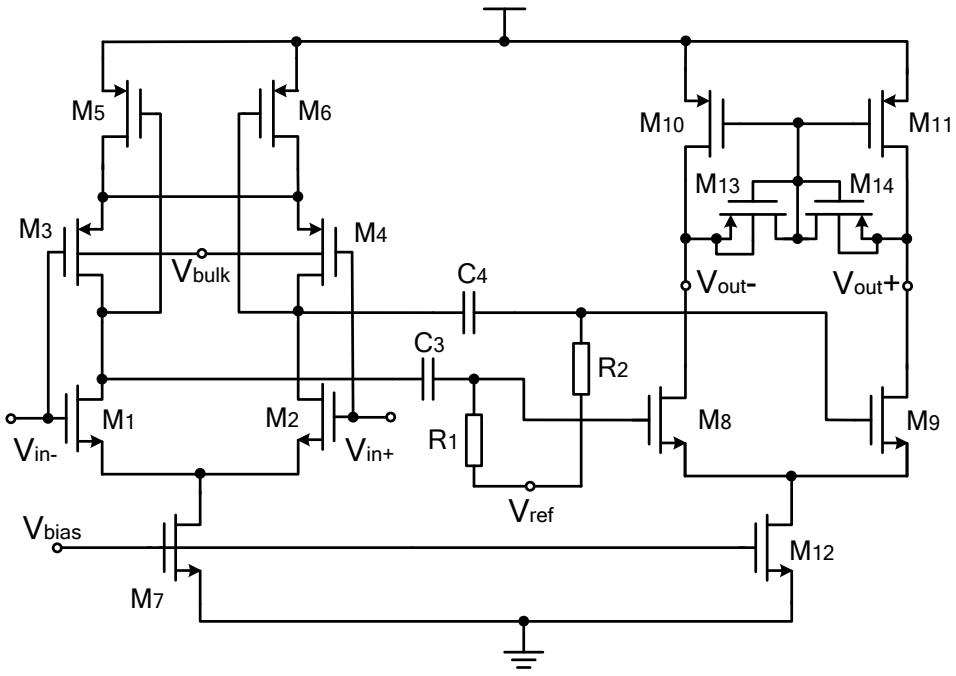


Figure 4.3 Schematic of the OTA adopted in the low noise front-end amplifier for EEG recordings.

The threshold voltage of the PMOS transistor is about 0.65V, which is too high to operate under 1V supply and may lead to malfunction of the front-end amplifier. To solve this problem, the bulks of $M_3$ and $M_4$ are biased externally, thus their threshold voltage can be tuned by changing the control voltage $V_{bulk}$. By forward biasing $M_3$ and $M_4$, their threshold voltages are lowered to a suitable level and much more voltage headroom are obtained for $M_5$ and $M_6$. $M_5$ and $M_6$ here act as the common mode feedback circuit, which set the output DC level of the first stage. The quiescent current of the OTA is well defined by the reference voltage $V_{bias}$, which is provided by an on-chip low power reference generator. This makes the DC biasing current of the OTA insensitive to the process variation and supply voltage. The common mode feedback of the output stage is realized by two pseudo-resistors $M_{13}$ and $M_{14}$. Their large resistances draw very little current at the output stage, hence a very small current is enough to support the output stage and further power saving is achieved. Meanwhile, small current at the output stage move the dominant pole of the OTA to left, and thus the phase margin of the OTA is improved and stability of the close loop amplifier is enhanced.

Even though ultra low power output stage is achieved using pseudo-resistors as common mode feedback circuit, there is a drawback for such kind of feedback topology. Proper working of the feedback circuit requires quiescent current in the output stage. Otherwise, it may lead to malfunction of the overall circuits. For example, when power is just applied to the circuits, the DC level of the output stage may stick at VDD or GND and there is no current in the output stage. The pseudo-resistor common mode feedback circuit will not be able to pull the circuit to proper operation condition. As a result, the OTA may not be able to start up and the circuit

will stay dead. To correct this problem, a DC rejection circuit between the first stage and the second stage of the OTA is inserted, which is composed by $R_1$, $R_2$, $C_3$ and $C_4$. They actually form a high-pass filter which cuts off the DC path in the OTA and effectively prevents the DC component from feeding back. The input common mode voltage of the second stage is provided by the external reference voltage $V_{ref}$, which is independent of the output common mode voltage of the first stage. By doing so, the output stage of the OTA is surely start-up during power on, leading to the output common mode voltage at normal working condition with the help of the pseudo-resistors $M_{13}$ and $M_{14}$. This common mode voltage will then be fed back to the first stage of the OTA via the feedback pseudo-resistors $M_a$ and $M_b$ in Figure 4.2, and the whole OTA circuits enter normal working condition. $R_1$ and $R_2$ are fixed resistance pseudo-resistors, which provide DC bias for $M_8$ and $M_9$. They have much higher resistance values than the ones generated by $M_a$ and $M_b$, to make sure that the high-pass corner frequency of the front-end amplifier will not be affected.

### 4.3.2 Auxiliary Circuits

The programmable gain amplifier is implemented at the second stage, where 2-bit control signal sets four gain levels. The same flip-over-capacitor feedback topology is employed for the gain tuning as the one shown in Figure 3.24. A Miller compensation OTA is adopted for the PGA as shown in Figure 4.4. $V_{LPF}$ controls the gate voltages of the current sink $M_5$ and $M_7$, thereby tune the quiescent current in the OTA. This adjusts the bandwidth of the OTA as well as the low-pass corner frequency of the PGA. Since both the low-pass corner frequency and the gain are controlled by the PGA, the different gain settings alter the –3dB bandwidth of the amplifier accordingly

due to the constant gain bandwidth product. Fortunately, this can be corrected by the tunable bandwidth feature, thus the bandwidth of the overall system remains consistent at different gain levels.

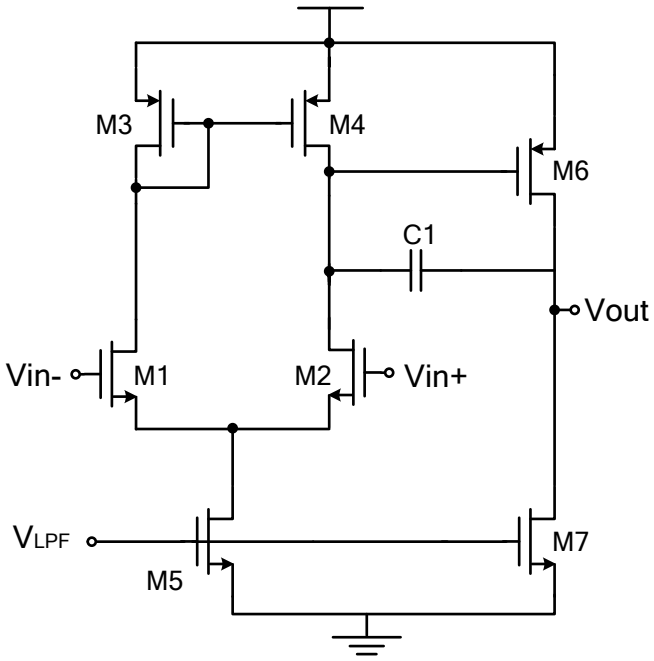


Figure 4.4 Schematic of the OTA adopted in the PGA for EEG recordings.

A buffer with broad bandwidth and high slew rate is necessary after the PGA to drive the S/H circuit of the ADC. The total gain contributed by the front-end amplifier and the PGA is high enough for EEG amplification. Thus a unity gain buffer is employed, where a broad bandwidth of tens of MHz can be achieved with less current. The buffer employs two-stage Miller compensation OTA with push-pull output stage to enhance the slew rate, as the one shown in Figure 3.25. Unity gain feedback may applied to the buffer to achieve gain of one and stable performance. However, unity gain feedback requires rail-to-rail input swing for the OTA, which is very difficult to implement, especially when low signal distortion is critical in low voltage applications. As a result, capacitive feedback is adopted as shown in Figure 4.5, where the negative and positive input of the OTA is virtual ground and no high swing

input OTA is needed. Balanced pseudo-resistor with fixed resistance is used in the buffer to provide DC bias and low distortion.

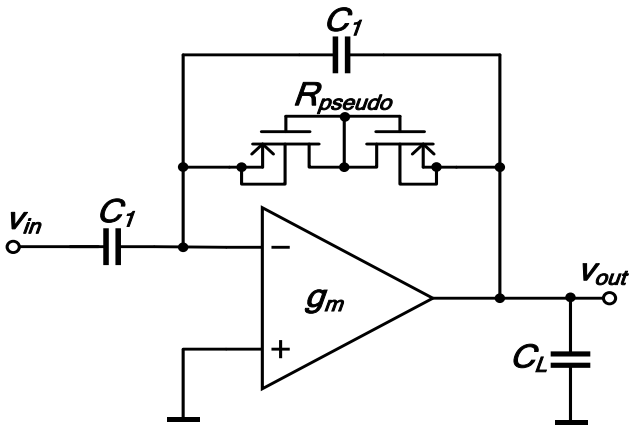


Figure 4.5 Schematic of the buffer in the neural recording system.

The required bandwidth of the buffer is calculated as follows.

$$\Delta V \times e^{-t/\tau} < \frac{1}{2^n \times 2},$$

$$-t \times 2\pi \times f < -\ln(2^n \times 2 \times \Delta V),$$

$$f > \frac{\ln(2^{n+1} \times \Delta V)}{2\pi \times t}, \tag{37}$$

where $f$ is the bandwidth of the buffer in hertz, $n$ is the resolution of the ADC, which is 10 in this design, $\Delta V$ is the sampling distance of the buffer and $t$ is the sampling time of the buffer. For 1V supply voltage, the maximum possible sampling distance of the buffer is 1V. The frequency band of the EEG signal is about 150Hz. For a 32-channel system, the minimum sampling frequency of the ADC is 150×2×32=9600(Hz). Assuming the sampling time of the buffer is one tenth of the ADC period for conservation estimation, $t$ is calculated to be about 10μs. So the minimums bandwidth of the buffer is calculated as follows,

$$f > \frac{\ln(2^{n+1} \times \Delta V)}{2\pi \times t} = \frac{\ln(2^{11} \times 1)}{2\pi \times 10 \times 10^{-6}} = 121k\,.$$

To ensure the fast settling of the buffer and reliable performance of the overall system, the bandwidth of the buffer is design to be more than 500kHz in this application.

In this design, the low-pass corner frequency is tuned at the gate of the current sink. A small circuit block is inserted between the external control pin and the gate of the current sink, as shown in Figure 4.6. By adopting such simple circuit, the sensitivity of the buffer bandwidth to the external control voltage is greatly reduced, as the aspect ratio of $M_{HPF}$ and $M_{11}$ are designed to be very small (smaller than 1), thus that the quiescent current in the circuit will not change dramatically with the change of the control voltage $V_{LPF2}$. This allows delicate tuning of the quiescent current in the buffer circuit, as well as the bandwidth of the buffer. Meanwhile, the insertion of such circuit effectively minimizes the external noise injected to the core circuits of this design.

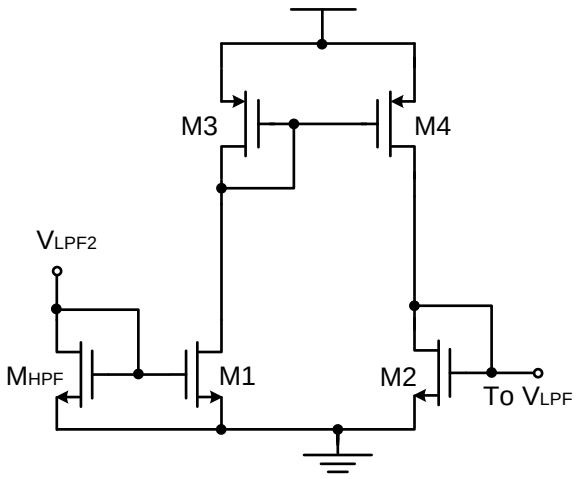


Figure 4.6 Schematic of the circuit used for the external control voltage.

## 4.4 Measurement Results

The prototype was fabricated in a standard 0.35μm 4M2P CMOS process with $V_{THN}+|V_{THP}|=1.15V$. The chip size is $1.8\times2.6mm^2$ excluding pads and the micrograph is shown in Figure 4.7. The input signals were fed into the system from the top and the bottom part, and the output signals of the analog front-end circuits went through the middle of the two symmetric blocks before entering the multiplexer located at the right part of the chip. The power supply and various control voltage pins are at the left hand side of the chip. Such floor plan separates weak input signals and large swing output singles, hence minimizes the channel cross talk. The overall system was designed and tested under 1V supply voltage and the system performance is summarized in the following sections.

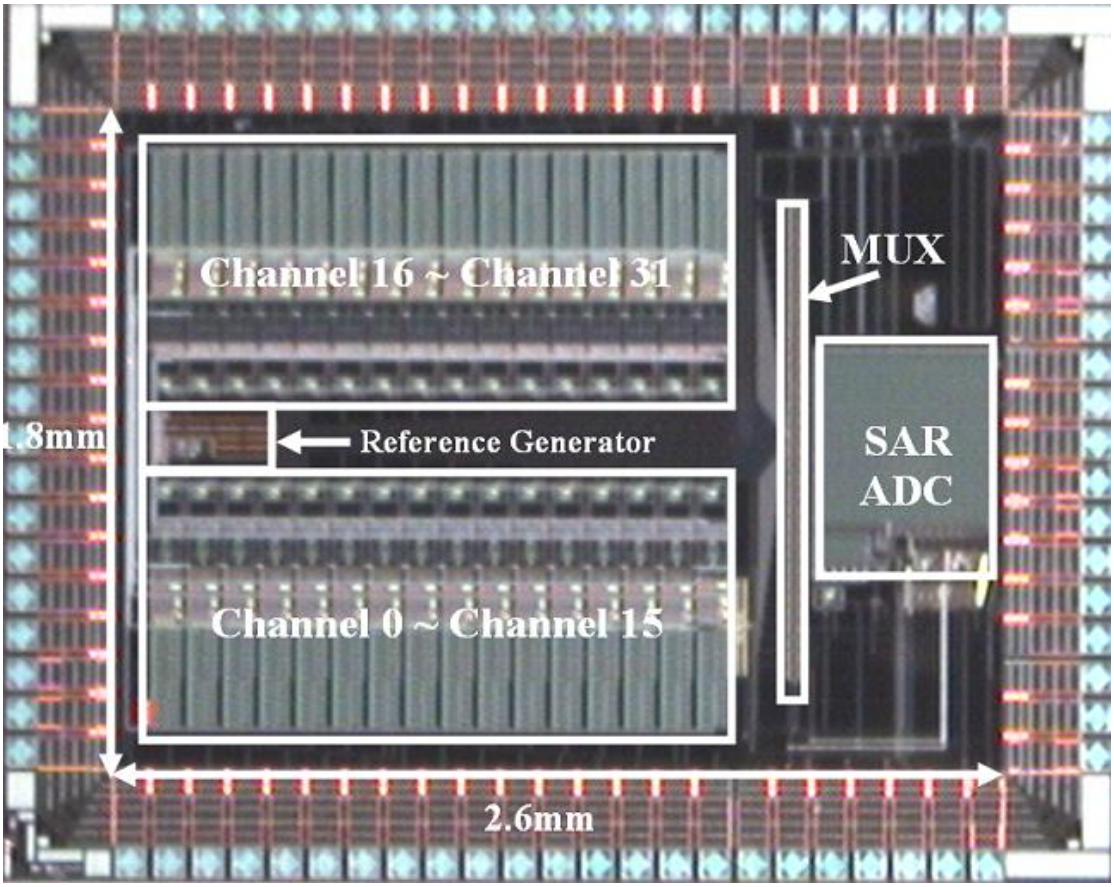


Figure 4.7 Microphotograph of the chip for EEG recordings.

### 4.4.1 Frequency Response

Figure 4.8 shows the frequency responses of the analog front-end. The figure was plotted by recording the signals at the output of the buffer using Agilent Dynamic Signal Analyzer 35670A. The high-pass corner frequency was tuned by changing the control voltage of the feedback pseudo-resistors, which thereby changes the resistance value. In Figure 4.8, the high-pass corner frequencies vary from about 0.2Hz to 10Hz by tuning the high-pass control voltage from 0.1V to 0.5V. In fact, according to the previous designs, it can be set at frequencies much smaller than 0.2Hz (refer to Figure 3.27), as the pseudo-resistors are able to provide resistance values in the range of $10^{15}\Omega$. However, it is not showed in Figure 4.8 as it requires very long time for the measurement equipment to collect enough number of points at such low frequency range. The low-pass corner frequency can be adjusted from about 30Hz to several kHz by changing the bandwidth control voltage of the PGA. In Figure 4.8, the control voltage $V_{LPF2}$ corresponding to the low-pass plot from left to right are 0.34V, 0.37V, 0.42V, 0.45V, and 0.5V, respectively. The maximum low-pass corner frequency is limited by the bandwidth of the front-end amplifier, which is about 4kHz according to the simulation result. By tuning both the high-pass and low-pass corner frequency, the application of the developed design is not limited to EEG acquisitions, and it can be configured to fit various biological signals recordings.

The gain adjustment of this design is displayed in Figure 4.9. There are four gain levels, which are 59dB, 61.5dB, 65.3dB and 70.8dB, respectively. In this plot, a slight variation on the high-pass corner frequency is observed for the highest gain configuration. This is because for the highest gain setting, all the non-fixed capacitors

in the feedback path of the PGA are flipped over to the input node, acting as the input capacitance. The feedback capacitance now is the smallest, and hence the high-pass corner frequency of the PGA moves right. This frequency is a little bit higher than the high-pass corner frequency of the front-end amplifier. As a result, the high-pass corner frequency of the overall system moves towards right slightly. However, from the plot of the frequency response, this small variation will not affect the performance of overall system much. This excursion can be corrected by resize the feedback pseudo-resistors of the PGA, i.e., decreasing the aspect ratio of the pseudo-resistors such that the highest high-pass corner frequency of the PGA is much smaller than the front-end amplifier. This will make sure that the PGA will not change the frequency response of the overall system and the high-pass corner frequency is only determined by the front-end amplifier itself.

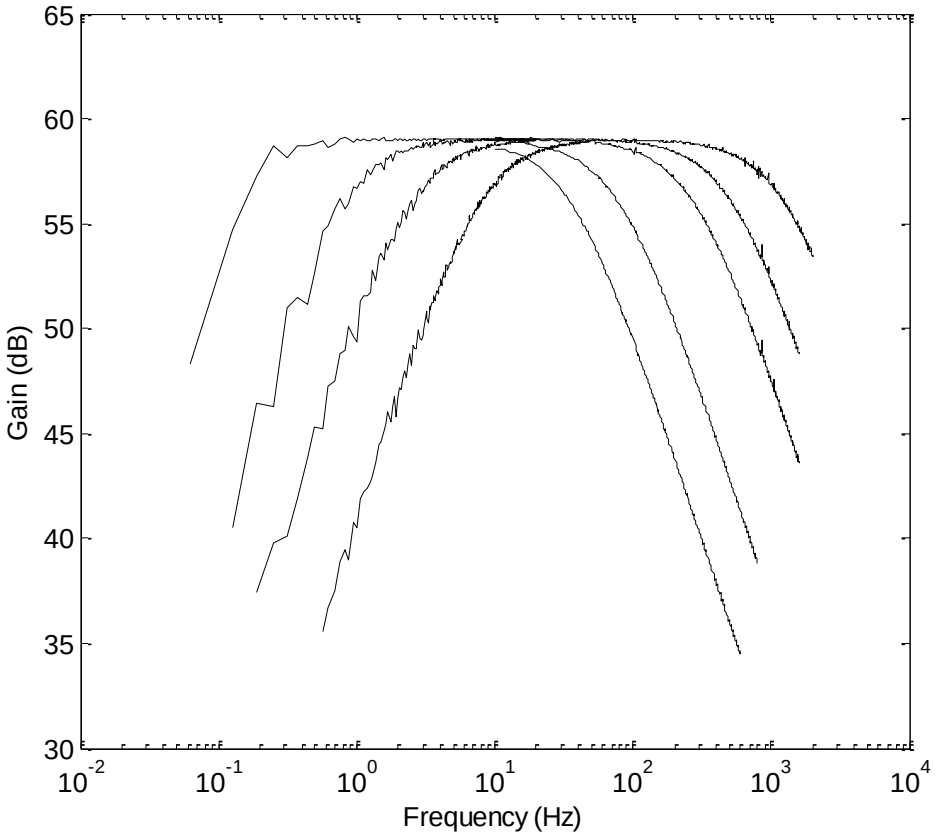


Figure 4.8 Frequency responses with tunable bandwidth for EEG recordings.

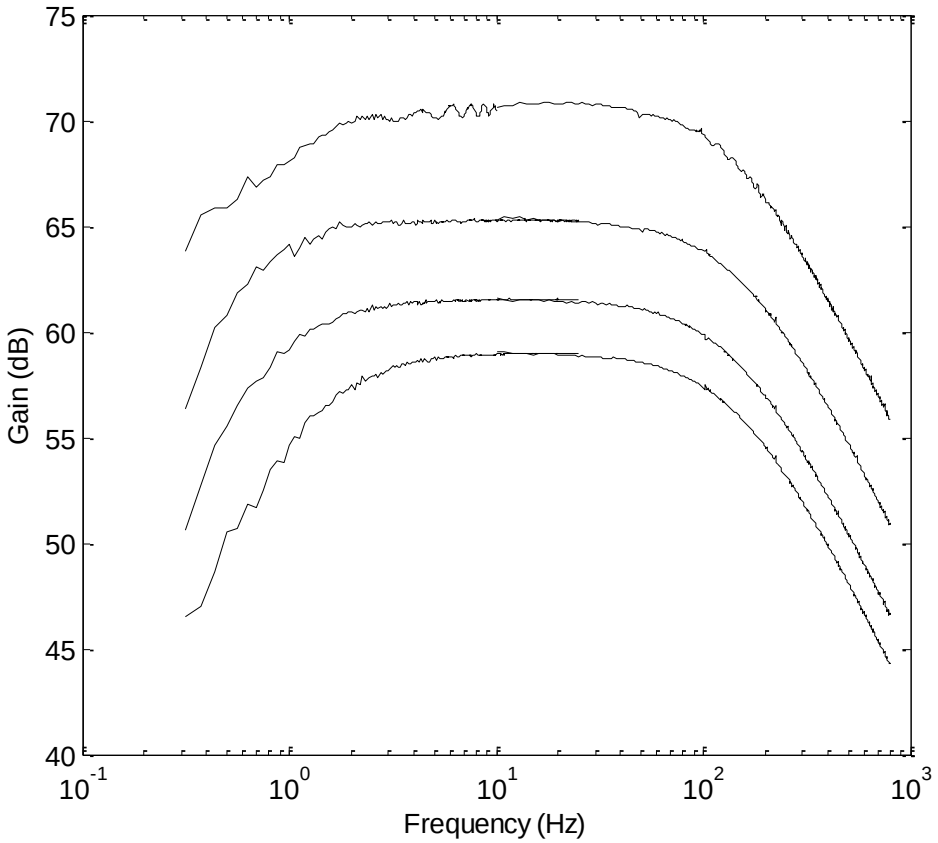


Figure 4.9 Frequency response with programmable gain for EEG recordings.

### 4.4.2 Input Referred Noise

The input referred noise of the analog front-end circuits is plotted in Figure 4.10 using Agilent Dynamic Signal Analyzer 35670A. It clearly shows that for low frequency application, the flicker noise is dominant. One may notice that the flicker noise corner frequency of this design is higher than the design dedicated for ECG recordings shown in Figure 3.29. This is because the gate area of the input transistors in this design is decreased in order to reduce the parasitic input capacitance and lower down the thermal noise floor. Figure 4.10 was plotted when the low-pass control voltage $V_{LPF2}$ was set at 0.45V, where the bandwidth of the system is 150Hz, and the gain

control voltage was set at 11, where the gain of the overall system is 70.8dB, and the high-pass control voltage was set at 0.1V, where the high-pass corner frequency appears at about 0.2Hz. The *rms* value of the input referred noise is 1.15μV, integrated from 0.5Hz to 150Hz. This satisfies the noise requirement for the implantable EEG devices.

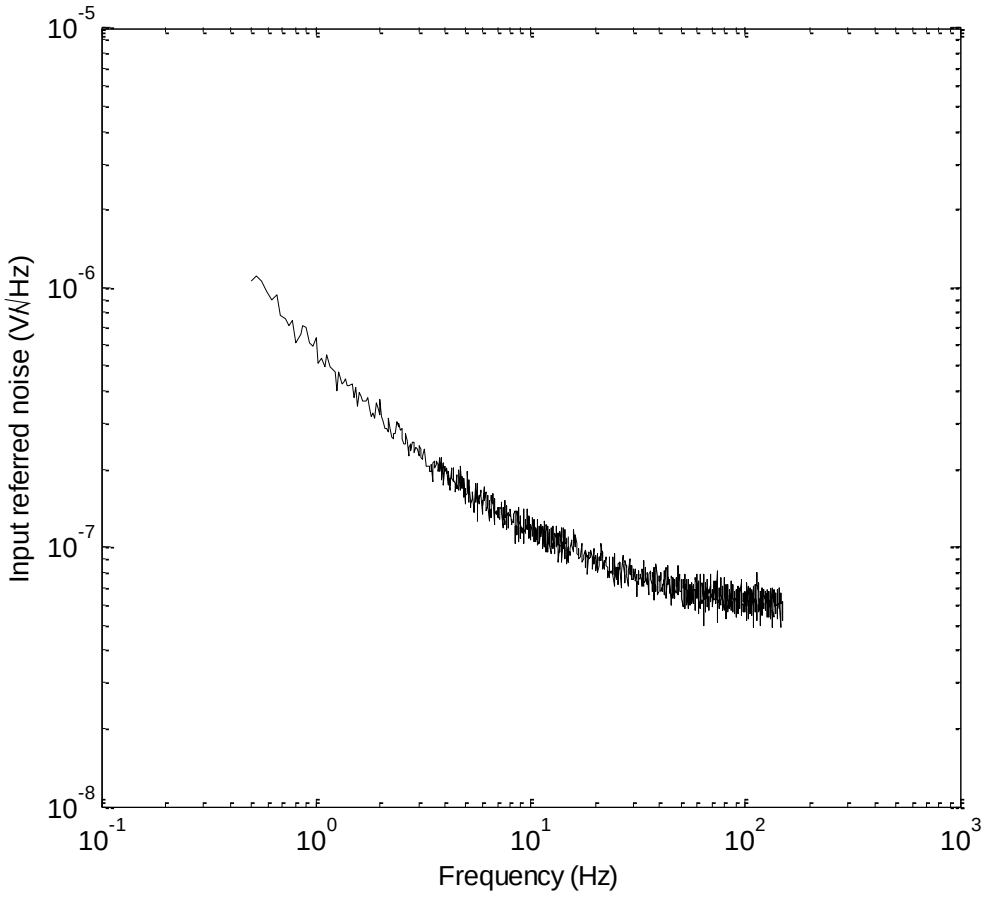


Figure 4.10 Input referred noise of the front-end amplifier for EEG recordings.

### 4.4.3 Total Harmonic Distortion

Figure 4.11 shows the THD vs. output amplitude of the analog front-end circuit. It was plotted by feeding a sine wave input from an ultra low distortion function generator (Stanford research systems, model DS360), and measuring the signal

distortion at buffer output using Agilent Dynamic Signal Analyzer 35670A. The results were recorded when the gain of the system was set at 70.8dB and the high-pass corner frequency was set at 0.2Hz. The THD readings for output amplitude less than 0.15V is not shown in the plot since the noise floor overrides the harmonic peaks and the readings do not reflect the THD performance of the system. The minimum THD reading appears at output amplitude of about 0.5V. After that, the THD increases with the increasing of the output amplitude. The 1% THD appears at output amplitude of about 0.9V. The THD performance of this design is worse than the previous designs for ECG recordings. The reason is that in this design, the analog front-end consists of 3 stages, where the signals experience more stages and thus more distortion. For large output amplitude of the analog front-end, the input amplitude of the third stage buffer is nearly rail-to-rail, and it is quite difficult to get low signal distortion for such large signal. Even though the THD performance of this design is degraded than the previous designs, it is still comparable with the recently published state-of-the-arts designs, making it an outstanding candidate for low noise low voltage biomedical sensor interface IC.

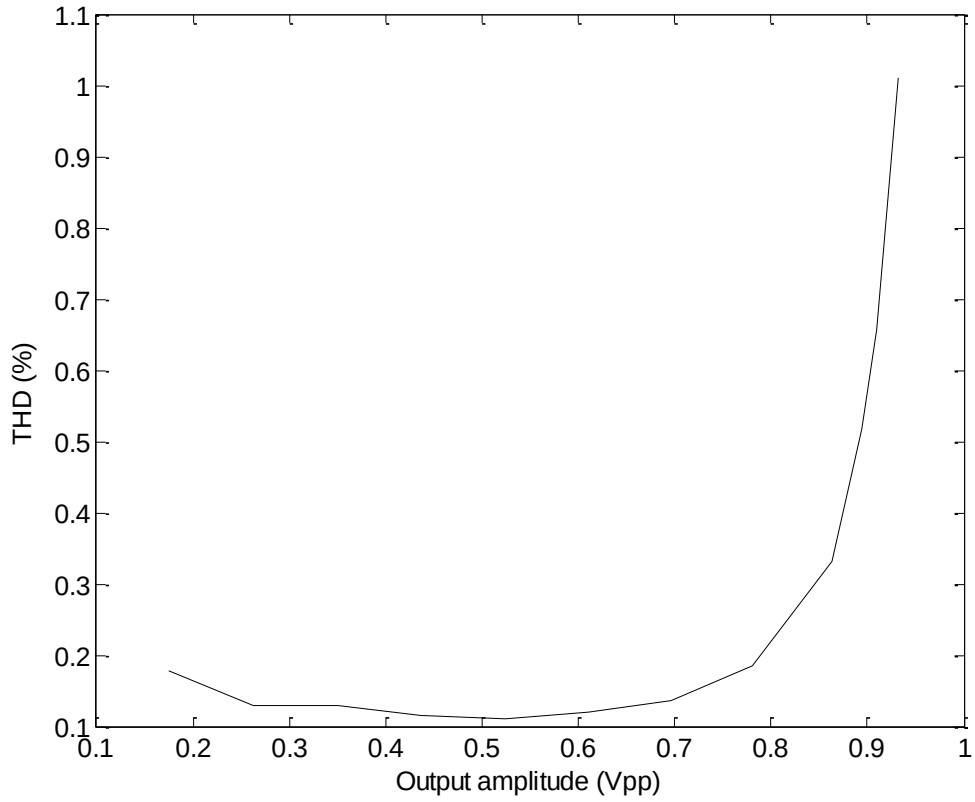


Figure 4.11 THD vs. output amplitude of the analog front-end for EEG recordings.

### 4.4.4 System Benchmarks

By employing the proposed 3-stage system architecture for the analog front-end circuits, more than 50% area saving is achieved compared to the recently published design [17]. The overall system consumes 22 µW, where 15.7 µW is dissipated by the 32-channel analog front-end. The average power per channel of the proposed chip is about 2.8% of the existing multi-channel design [18], indicating a power efficient system architecture. Table 7 summarizes the performance of the EEG chip and the comparison between this work and recently published state-of-the-arts designs is also provided. From Table 7 we can see that the performance of this design is better or comparable with the state-of-the-arts designs, especially on chip area and power

consumption. The front-end amplifier achieves a NEF of 2.24, which is the smallest among published designs, indicating an optimum trade-off between power consumption and noise figure. The relatively high noise figure of this design compared to [38] and [18] is due to the lack of chopper stabilization. However, an input referred noise of 1.15 μV still satisfies the application requirement. The channel isolation is measured by giving an input signal with specific frequency at one channel and recording the signal at the output of the adjacent channel. In fact, there is no signal with that specific frequency is observed at the output of the adjacent channel but only thermal noise. The reading shows a more than 85dB channel isolation as the channel cross-talk signals are buried under the noise floor. The CMRR of this work is only 83.2dB, which is much lower than the simulated result of 120dB. This is because the positive inputs of the 32 front-end amplifiers are tied together in order to save number of pins and chip area. This makes the positive and negative inputs of the front-end amplifiers not perfectly matched, resulting in degraded CMRR. Improvement on CMRR needs to be done in future designs.

Table 7 Performance comparison between the developed EEG recording chip and recently published state-of-the-arts designs.

| **Parameter** | **Design in [38]** | **Design in [18]** | **Design in [17]** | **This work** |
|---|---|---|---|---|
| **Supply voltage** | 1.8 V | 3 V | 1 V | 1 V |
| **Process technology** | 0.8 μm CMOS | 0.5 μm CMOS | 0.35 μm CMOS | 0.35 μm CMOS |
| **Current (front-end amplifier)** | 1.2 μA | 2.3 μA | 337nA | 385nA |
| **Midband gain** | 45.5dB | 72/75.6/81.6dB | 45.6/49/53.5/60 dB | 59/61.5/65.3/70 .8dB |
| **High-pass $f_{-3dB}$** | 0.5Hz | 0.1Hz | 0.5Hz (tunable) | 0.5Hz (tunable) |
| **Low-pass $f_{-3dB}$** | 250 | Digitally selectable | 292Hz (tunable) | 150Hz (tunable) |

| | | | | |
|---|---|---|---|---|
| **Input referred noise** | 0.93 μV (0.5~100Hz) | 0.57 μV (0.5~100Hz) | 2.5 μV (0.05~ 460Hz) | 1.15 μV (0.5~150Hz) |
| **NEF** | 4.9 | 4.1 | 3.26 | 2.24 |
| **CMRR** | 105dB | >120dB | 71.2dB | 83.2dB |
| **PSRR** | -- | 90dB | 84dB | 75dB |
| **THD** | -- | <1% (at 1.65$V_{pp}$ output swing) | <0.6% (at 1$V_{pp}$ output swing) | <1% (at 0.9$V_{pp}$ output swing) |
| **Channel isolation** | -- | -- | -- | > 85dB |
| **Total power** | 2.2 μW | 198 μW | 0.9 μW | 22 μW |
| **Number of channel** | 1 | 8 | 1 | 32 |
| **Average power per channel** | 2.2 μW (amplifier only) | 24.75 μW | 0.9 μW | 0.69 μW |
| **Area per channel (analog part)** | 1.4$mm^2$ [18] | 0.45$mm^2$ | 0.64$mm^2$ | 0.08$mm^2$ |

The developed prototype was further tested by acquiring the ECG signal from human volunteer. A total of 6-channel EEG signals were recorded as shown in Figure 4.12. All of the 6 electrodes were placed on forehead spreading to temple in a line, as we need to avoid the hairy part of the head, since the only available electrodes in the lab are the standard Ag/AgCl monitoring electrodes with foam tape and sticky gel (wet electrode). The data in Figure 4.12 was extracted from the ADC and these signal pulses were generated by eye blinking. The signal amplitude in the top two channels is relatively large, since these two channels were placed in the center of the forehead and close to the signal sources. The successful acquisition of the EEG signal demonstrates the functionality of the developed chip. Its ultra low power consumption and small chip area makes it an excellent candidate for the implantable low power EEG sensor interface IC.

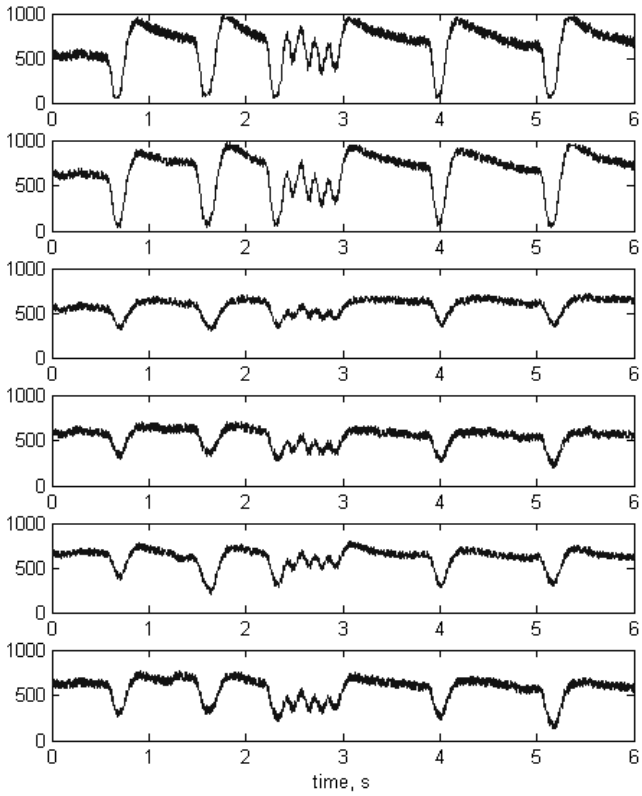


Figure 4.12 EEG signals captured by the developed chip during eye movement.

# CHAPTER 5

# DESIGN OF ANALOG FRONT-END IC FOR NEURAL RECORDINGS

## 5.1 Design Considerations

Simultaneous recording of neuropotentials over a large number of electrodes from the brain provides an effective way for neuroscientist and clinician to study the brain state dynamics and understand the nature of various neurophysiological behaviors. It has a wide range of applications, where the most exciting and hottest one currently is the development of brain controlled neural prostheses, which are controlled directly by thoughts. Recent clinical trials with paralyzed human volunteers have shown that it is possible to restore limb movement by such kind of neuroprosthetic devices [93-95]. This calls for the development of low power low voltage implantable integrated multi-channel neural recording interface. As the recording microsystem is implanted in the brain, the power density budget of the chip is very limited, in order to prevent the damage of the surrounding tissue due to the excessive heat dissipation [96]. Different from the previous ECG and EEG signals which occupy very low frequency band, the frequency range of the neural signal can spread up to several kilo Hz and a bandwidth of 5~10kHz is typically used for the neural signal amplification. The high-pass corner frequency of the amplifier is better designed with a tunable range of 1~300Hz, in order to be compatible for both extracellular neural signals and local field potentials (LFP) [7, 97]. The amplitude of neural signals from extracellular recording is relatively small, typically from 10-500 μV [43]. In order to obtain clean neural signal

recordings, the input referred noise of the front-end amplifier should be kept below the background noise of the recording site (5~10 μV) [56]. According to these characteristics of the neural signals, the design target of the analog front-end circuits for the sensor interface IC is listed in Table 8.

Table 8 Design target of the neural signal recording front-end circuits

| **Specification** | **Value** | **Remarks** |
|---|---|---|
| Supply voltage | 1V | 0.35 μm CMOS process |
| No. of channels | 16 | |
| Average current/channel | < 4 μA | Including current of ADC |
| Amplifier current | < 1.5 μA | Front-end amplifier only |
| Gain | 200~1000 | Programmable gain |
| Input referred noise | < 5 $\mu V_{rms}$ | Integrated in the signal band |
| High-pass corner frequency | 1~300Hz | No external components, tunable |
| Low-pass corner frequency | 8kHz | fixed |
| THD | < 1% | @ 80% output swing |
| Channel isolation | > 80dB | Adjacent channels |

## 5.2 System Architecture

The essential modules in a typical analog front-end of neural recording IC are amplifier and band-pass filter. Due to the small amplitude of the neural signals, a system gain of several hundred to few thousand is needed. Since the upper frequency bound of the neural signal is quite high, which is from 5kHz up to 10kHz, the bandwidth of the front-end amplifier is relatively high. Hence it may be possible for

the front-end amplifier to drive the S/H circuit itself and the second stage driving circuit can be eliminated. However, there are issues with single-amplifier approach. According to Eq. (14), assuming a maximum neural signal frequency of 8kHz with a moderate $\eta$ of 0.5 and a 10-bit ADC, the required minimum -3dB bandwidth of the driving circuit in a single channel design is

$$f_{-3dB} = \frac{1}{2\pi \cdot \tau} > \frac{\ln(2^n \cdot \pi \cdot \eta)}{\pi(1-\eta)} \cdot f_{signal} = 37.6kHz\,. \tag{38}$$

The resultant value is higher than the signal bandwidth of 8kHz, because of the high sampling speed of the ADC and shortened sampling time. For multi-channel design, the minimum $f_{-3dB}$ becomes much higher than 37.6kHz due to the further reduced sampling time. As a result, the proposed two-stage analog front-end architecture in the previous chapter is still necessary for neural recording sensor interface IC. Besides solving the driving problem, the two stage analog front-end makes the system partition easier compared to single amplifier based system. The first stage aims for low input referred noise with integrated band-pass function, without worrying about the gain adjustment and driving capability. In addition, the THD requirement is relaxed since the signal amplitude in this stage is relatively low. The second stage PGA is designed with high driving capability, and its bandwidth variation and noise figure have negligible effect on the overall system. Thus it is much easier to decide the circuit topologies and allocate the current dissipation of the analog front-end modules according to their different design requirements.

Effective and reliable neural research and diagnosis rely on multi-channel recordings. A complete 16-channel sensor interface system consists of a 16-channel analog front-end, a 16-to-1 multiplexer, an S/H switch and a 10-bit SAR ADC was designed. The

system architecture is shown in Figure 5.1 (the multiplexer and the SAR ADC were developed by other team member). The first stage is a low noise front-end amplifier integrated with a band-pass filter, providing a fixed gain of 100, which is selected to achieve both relatively small chip area and sufficient noise suppression. The second stage is a PGA with 4 gain settings to fulfill the system gain requirement. Meanwhile, the PGA is designed with wide bandwidth and high slew rate to enhance its driving capability. The multiplexer, S/H switch and the ADC are developed by another team member and will not be covered in this thesis.

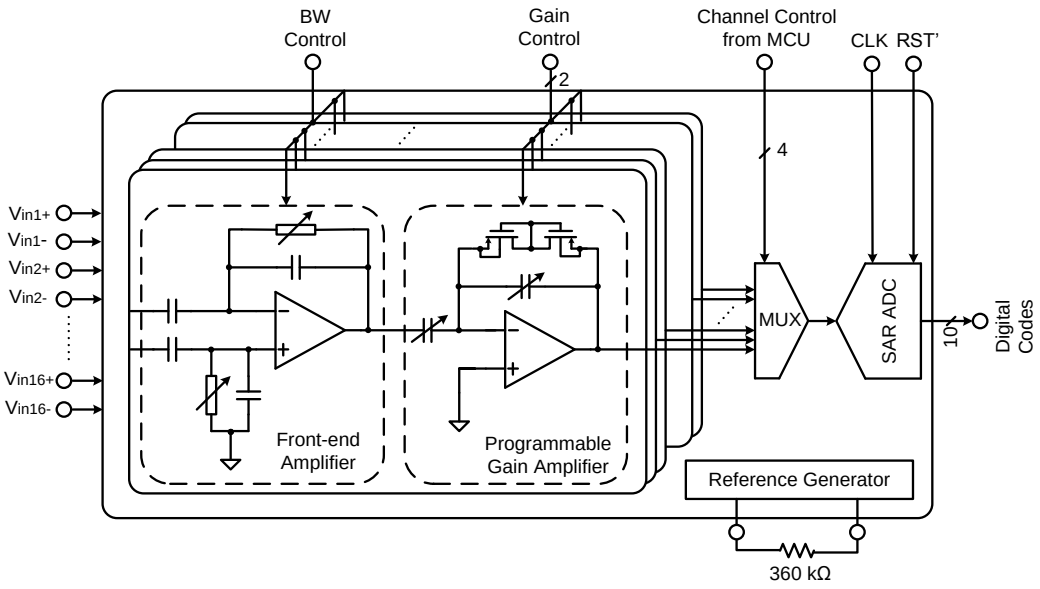


Figure 5.1 System architecture of the 16-channel neural recording IC.

## 5.3 Circuits Implementations

### 5.3.1 Low Noise Front-end Amplifier

The schematic of the front-end amplifier is shown in Figure 5.2. It adopts capacitive feedback for low power and low noise operation. Neural amplifier usually has

relatively wide bandwidth of several kHz, hence thermal noise is dominant and a slight rise of the thermal noise floor will increase the *rms* input referred noise remarkably. According to Eq. (36), smaller input capacitance will result in higher thermal noise floor. In order to ensure good matching and minimize the input referred noise, $C_1$ and $C_2$ are set to be 50pF and 500fF, respectively, where the total area of the overall system is still acceptable. The reference voltage $V_{ref}$ is fixed at half VDD to maximize the dynamic range of the front-end amplifier. The DC rejection of the front-end amplifier is provided by the fully balanced tunable pseudo-resistors $M_a$~$M_d$, so that it achieves high dynamic range and low signal distortion. By varying the control voltage $v_{res}$, the current passing through $M_{aa}$ and $M_{bb}$, as well as their gate to source voltages ($v_{gs}$) are changed. Thereby the resistances of the pseudo-resistors are tuned by $v_a$ and $v_b$, which in turn set the high-pass corner frequency of the front-end amplifier. The W/L ratio of $M_{res}$ is designed to be very small to make its current less sensitive to voltage change at $v_{res}$.

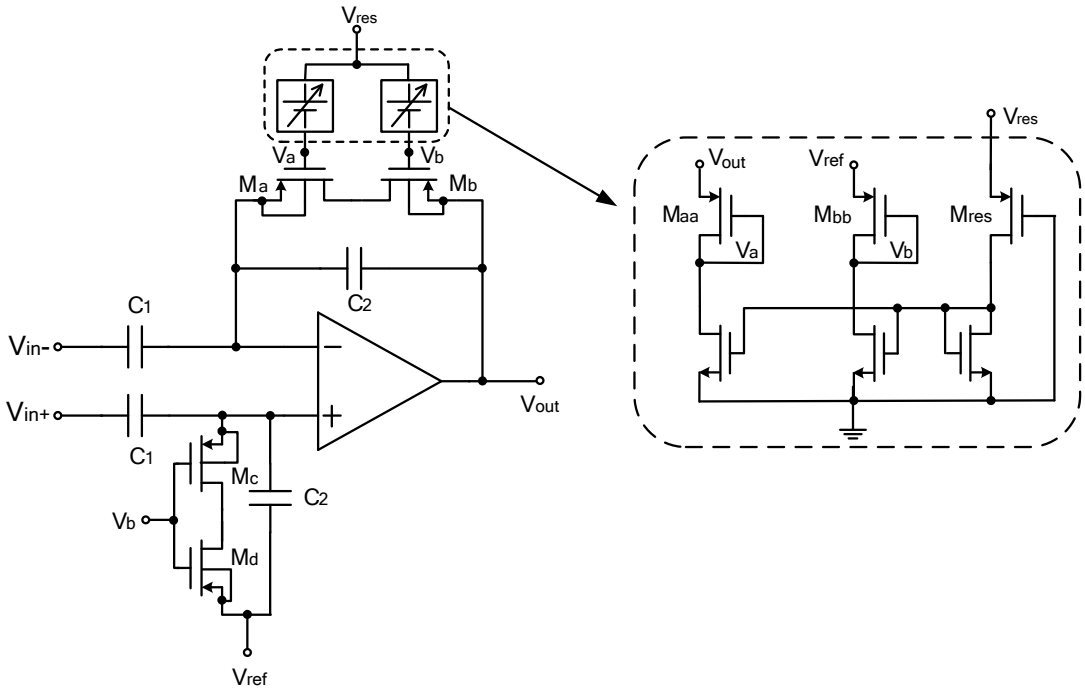


Figure 5.2 Schematic of the low noise front-end amplifier for neural recordings.

As shown in Figure 5.3, the OTA of the front-end amplifier adopts a two-stage Miller compensated topology. For neural recording applications, thermal noise is dominant. Thus, maximizing the transconductance of the input pair transistors within the tight power budget becomes more and more critical. To get better noise to power trade-off, both NMOS and PMOS transistors are employed as the input pairs of the OTA to increase the input transconductance and lower the thermal noise floor. All the 4 input transistors operate in sub-threshold region to achieve high transconductance efficiency ($g_m/I_d$). Meanwhile, more than 80% of the OTA power is distributed to the input stage for further noise reduction. The flicker noise of the OTA is suppressed by choosing large gate area for both PMOS and NMOS input pairs. Due to the high threshold voltage ($V_{th}$) of the PMOS transistors in 0.35μm CMOS technology, the bulks of transistor $M_3$ and $M_4$ are biased externally to lower their $V_{th}$ and increase the voltage headroom for $M_5$. The quiescent current of the OTA is well defined by the reference voltage $V_{bias}$, which is provided by the on-chip reference generator. This makes the DC biasing current of the OTA insensitive to the process variation and supply voltage, while in [42], the DC biasing current is greatly dependent on the supply voltage and the threshold voltages of both NMOS and PMOS tail transistors, where the total power consumption may significantly differ from the expected value, especially for multi-channel design. The penalty of the proposed approach is the degraded power supply rejection ratio (PSRR), which can be improved by good decoupling of the power lines and isolating the digital part from the analog circuits.

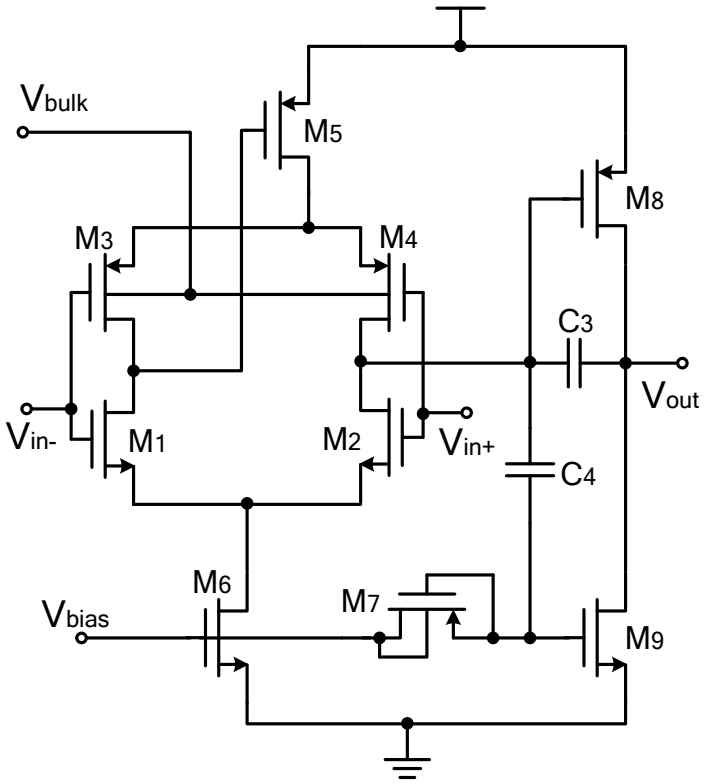


Figure 5.3 Schematic of the OTA adopted in the front-end amplifier for neural recordings.

The output stage of the OTA employs a push-pull topology [73]. Hence a small DC current at the output stage is able to support large amplitude and high frequency input signals. The savings in current from the output stage is added to the input stage to maximize the power efficiency. Besides this, the input referred noise contributed by the output stage is reduced under such push-pull scheme. $C_3$ is the Miller compensation capacitor that sets the dominant pole of the OTA, which in turn determines the low-pass corner frequency $f_{-3dB,LPF}$ of the front-end amplifier according to Eq. (38),

$$f_{-3dB,LPF} = \frac{g_{m,input}}{C_3} \times \frac{C_2}{C_1}, \tag{39}$$

where $f_{-3dB,LPF}$ is set at 8kHz for neural recording and $g_{m,input}$ is the input transconductance of the OTA.

### 5.3.2 Auxiliary Circuits

Following the front-end amplifier, it is a low power high output swing PGA. The neural signal is further amplified here before digitization. It employs the same flip-over-capacitor feedback as described in Figure 3.24 to avoid the low frequency zero-pole pair. Since the PGA also acts the driver of the following S/H circuit, a two stage OTA with push-pull output stage is implemented to enhance its driving capability, as shown in Figure 3.25.

A low power reference generator is also implemented to provide the reference current to the core circuits of this design. Similar circuit topology is adopted as the one in Figure 3.9, except that the resistor in this design is external. The reference current of this current source is increased to 50nA. This is because the current dissipations for both the front-end amplifier and the PGA in this design increase, which are in μA range, due to the relatively high bandwidth required by the neural signals recordings. A reference current of 50nA is suitable for easy and compact design while maintaining low power consumption of the reference generator.

## 5.4 Measurement Results

The chip prototype was fabricated in a standard 0.35μm 4M2P CMOS process with $V_{THN}+|V_{THP}|$=1.15V. The chip size including ADC is 2.5×3.3mm$^2$ excluding pads and the die photo is shown in Figure 5.4. The overall system was tested under 1V supply and consumes 60.3μW total power.

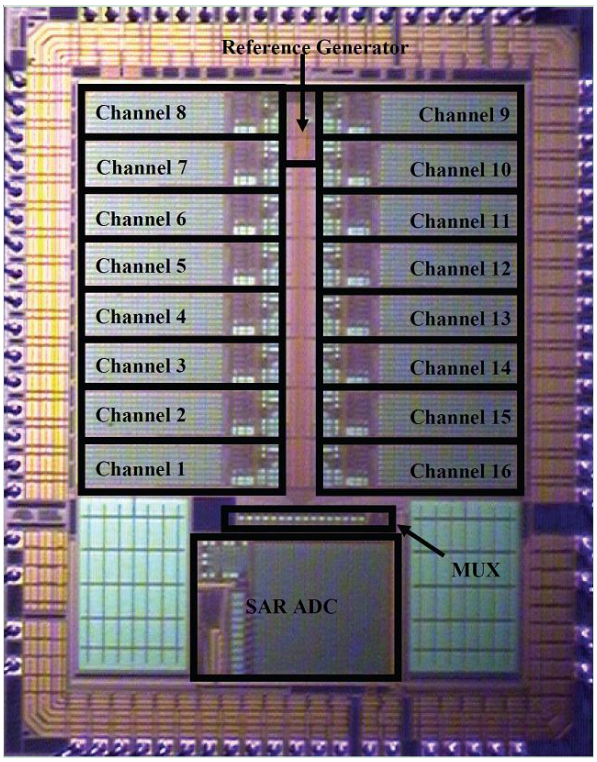


Figure 5.4 Microphotograph of the chip for neural recordings.

The measured frequency responses of the analog front-end using Agilent Dynamic Signal Analyzer 35670A is shown in Figure 5.5. The high-pass corner frequency of the front-end amplifier is continuously tunable from 0.23Hz to 217Hz by varying the control signal $v_{res}$ from 0.4V to 0.7V in 50mV steps. The measured low-pass corner frequency of the front-end amplifier is 7.8kHz which is approximately the same as the

design target. The programmable gain function is demonstrated in Figure 5.6. There are four gain levels which can be selected by 2-bit control signal. The gain of the analog front-end varies from about 200 to 1000, which satisfies the implantable requirement for neural recordings.

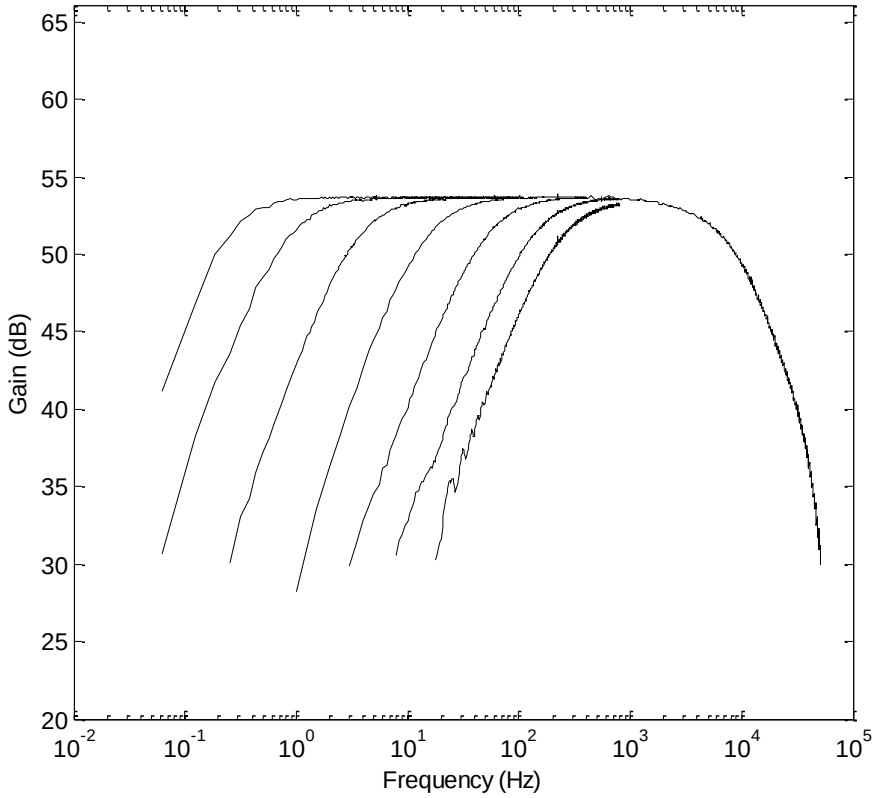


Figure 5.5 Frequency responses with tunable bandwidth for neural recordings.

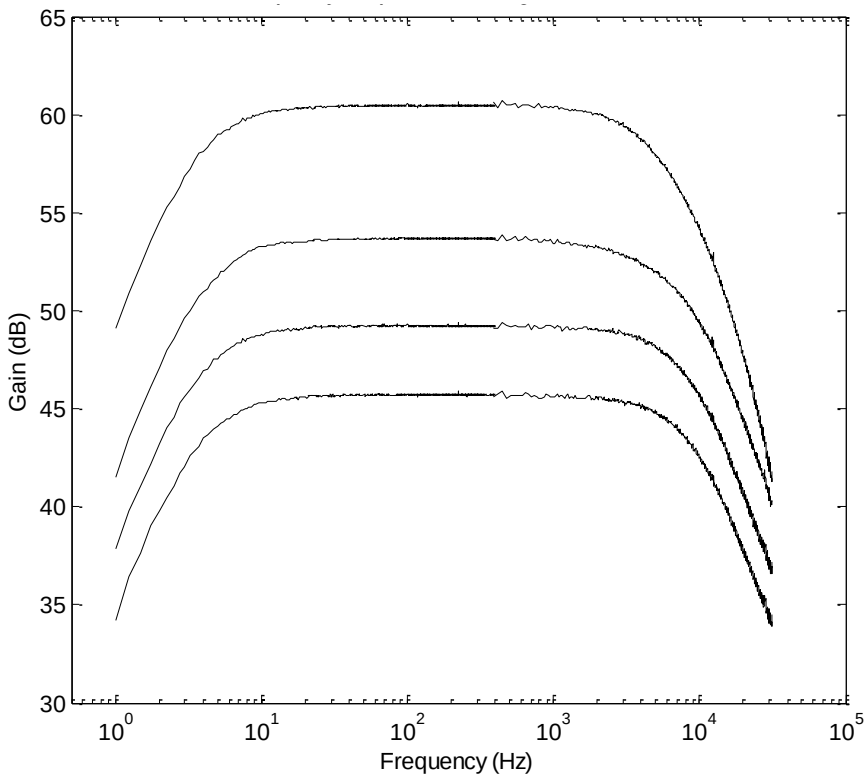


Figure 5.6 Frequency responses with programmable gain for neural recordings.

The input referred noise of the front-end amplifier was measured by connecting the differential inputs to ground and recording the output signal spectrum using Agilent Dynamic Signal Analyzer 35670A. The *rms* value of the input referred noise is 4.43 μV integrated from 1 Hz to 12 kHz, which is the effective noise bandwidth of the front-end amplifier. With the power consumption of 1.255 μW, the front-end amplifier achieves a NEF of 2.16, which is one of the lowest values among recently published neural recording ICs, indicating an optimum power to noise trade-off for the front-end amplifier.

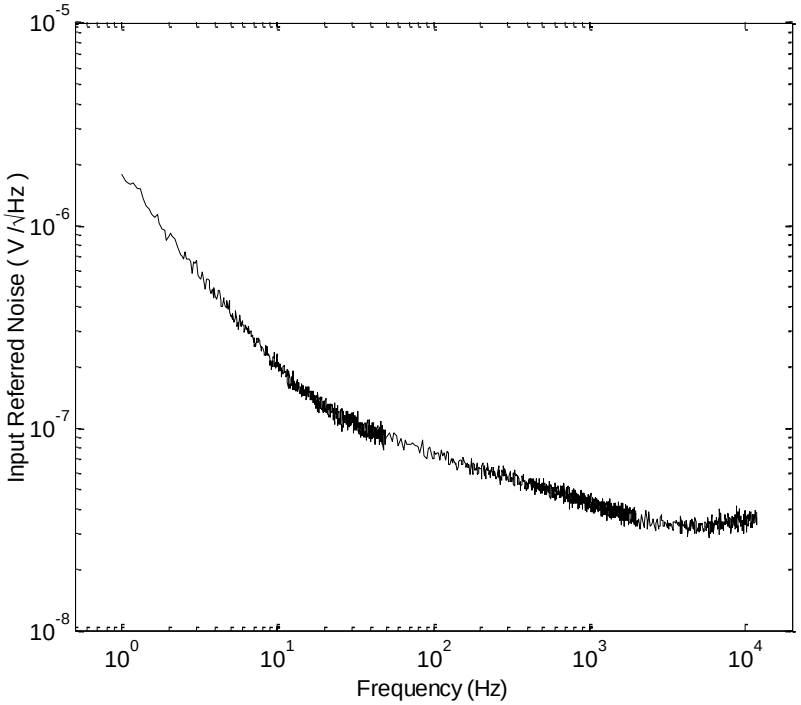


Figure 5.7 Input referred noise of the analog front-end circuits for neural recordings

The total harmonic distortion (THD) of the analog front-end is plotted in Figure 5.8. For output amplitudes smaller than 0.9V, most of the harmonic peaks are over-ridden by the noise floor. So the THD readings decreasing continuously in this range due to the increasing signal to noise ratio (SNR). That is to say the high THD at small output amplitude does not mean bad linearity of the amplifiers but is due to the noisy signal source. The THD is only 0.53% at rail-to-rail output swing, thanks to the two-stage analog front-end architecture and the fully balanced pseudo-resistors implemented in both the front-end amplifier and PGA.

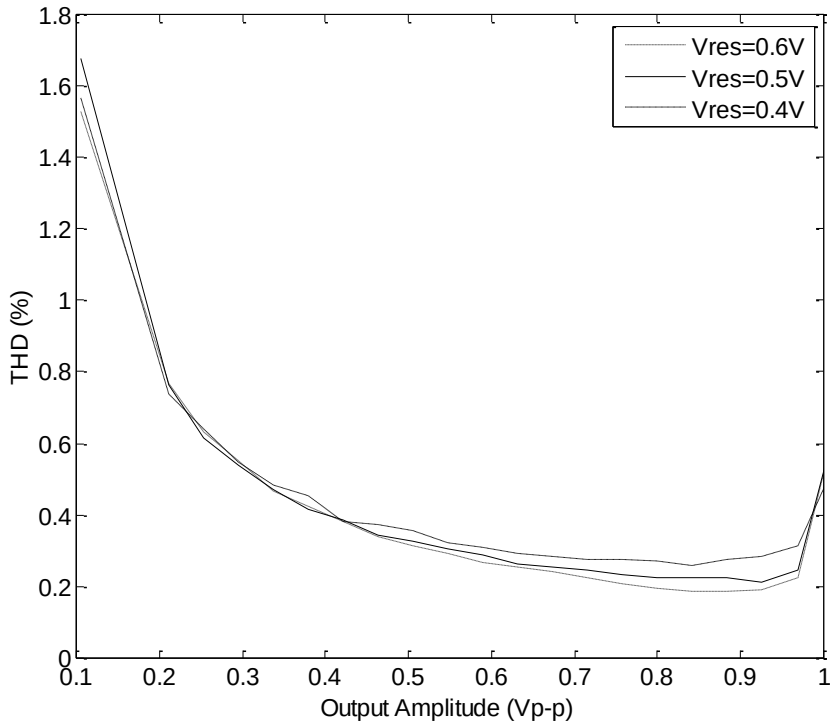


Figure 5.8 THD vs. output amplitude of the analog front-end circuits for neural recordings.

The detailed performance of the neural recoding IC and comparisons with other state-of-the-art designs are summarized in Table 9. The proposed design achieves minimum power consumption, which is more suitable for implantable neural recordings. The lowest NEF indicates an optimum noise to power trade-off of the front-end amplifier.

Table 9 Performance comparison of the neural recording chip with recently published state-of-the-art designs.

| Parameter | Design in [42] | Design in [18] | Design in [12] | This work |
|---|---|---|---|---|
| Supply voltage | ±1.65V | 3V | 3.3V | 1V |
| Process technology | 0.35 µm CMOS | 0.5 µm CMOS | 0.5 µm CMOS | 0.35 µm CMOS |
| Current ( front-end amplifier) | 2 µA | 2.3 µA | 12.8 µA | 1.255 µA |

| | | | | |
|---|---|---|---|---|
| Midband gain | 57 ~ 60dB (tunable) | 72 / 75.6 / 81.6dB | 60.1dB | 45.7 / 49.3/ 53.7 / 60.5dB |
| High-pass corner frequency | 0.1 ~ 200Hz (tunable) | 0.1Hz | 30 Hz ~1kHz (tunable) | 0.23 ~ 217Hz (tunable) |
| Low-pass corner frequency | 2k ~ 20kHz (Tunable) | Digitally selectable | 5kHz | 7.8kHz |
| Input referred noise | 4.9 μV | 0.57 μV ( 0.5 ~ 100Hz) | 5.1 μV | 4.43 μV (1Hz ~ 12kHz) |
| Noise efficiency factor | -- | 4.1 | -- | 2.16 |
| THD | -- | -- | -- | 0.53% (at full swing) |
| CMRR | 90dB | 120dB | -- | 58dB |
| PSRR | 80dB | 89dB | -- | 40dB |
| Average power per channel | 23.4 μW | 24.75 μW | ~ 142 μW | 3.77 μW |
| Total power ( amplifiers + ADC) | 3 mW (128 channels) | 198 μW (8 channels) | ~ 142 μW (1 channel) | 60.3 μW (16 channels) |

While working on the biological implantation for neural tests, the prototype was preliminarily tested to acquire eye blinking artifacts from human volunteer to demonstrate its functionality. Although the eye blinking artifacts exhibit lower frequency components, however its lower signal amplitude makes it a good candidate to benchmark the recording interface, especially for the noise performance. Figure 5.9 shows one of the eye blinking artifacts recordings. From the recording, it is clear that the recording interface has sufficient SNR to support neural signal acquisition. Standard Ag/AgCl monitoring electrodes with foam tape and sticky gel were used. Two electrodes were placed at the back of the ears, as the reference and ground of the

system, respectively. The other electrode was placed at the forehead as the input signal. During eye blinking, clear signal pulses were captured by the developed chip as displayed in Figure 5.9.

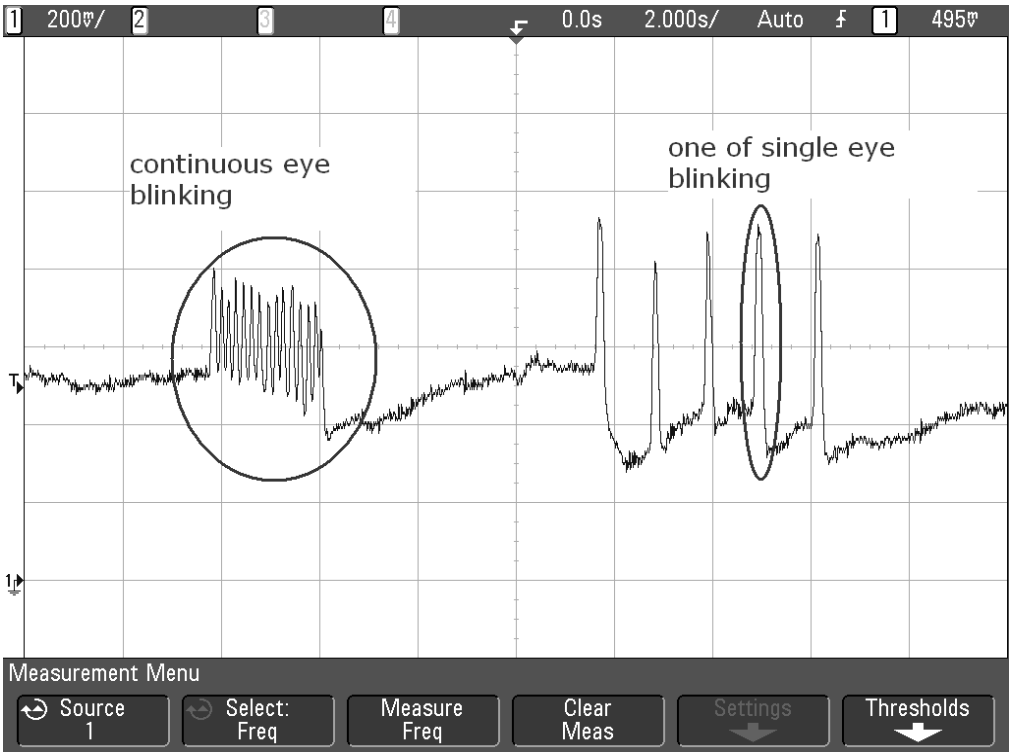


Figure 5.9 Eye blinking artifacts captured by the developed chip.

# CHAPTER 6

# CONCLUSION AND FUTURE WORKS

## 6.1 Conclusion

The realization of the WBAN system calls for the development of the low power low noise biomedical sensor interface IC. The work in this thesis covers the detailed implementation and optimization approaches for the low power low noise biomedical sensor interface IC design, including the development of the system architecture and each individual module. According to the different application requirements, prototypes for EEG, ECG and neural signal recordings were successfully fabricated and their functionalities were carefully verified.

A general guideline to optimize the total power consumption of the system is first proposed in this project. The relationship between the buffer bandwidth and the ADC holding time is investigated and analyzed, which has never been discussed in the literature before. By finding out the optimum holding time for the ADC S/H circuit, the minimum power consumption of the system can be achieved. Applying the developed guideline, the fabricated chip consumes only 445nW total power including ADC, which is one of the lowest values reported to date, indicating an optimum system design strategy for low power low noise biomedical sensor interface system.

In the low power low noise biomedical sensor interface IC design, pumping a large current to suppress the noise floor is not a proper approach. Optimizing noise to

power trade-off is becoming more and more important. In this project, the approach to achieve lowest NEF is discussed, which is realized by choosing the suitable operation region for the input pair transistors. Besides this, a low noise amplifier structure is proposed, which employs both NMOS and PMOS transistors as input pairs and reduces the thermal noise floor to almost half. Compared to the published structure whose power greatly depends on the supply voltage and process variation, the proposed circuit is much more reliable on both power consumption and performance, as its quiescent current is a well defined stable value. The NEFs of these developed low noise amplifiers are from 2.16 to 3.26, which are all among the lowest values published to date. In order to achieve ultra low cut-off frequency with minimum chip area, MOS-diode pseudo-resistor structure is widely employed. However, the existing pseudo-resistor exhibits unbalanced electrical property and induces unavoidable DC level shift, resulting in poor dynamic range in low voltage operation. A fully balanced tunable pseudo-resistor structure was proposed in this project. By using the proposed pseudo-resistor, the analog front-end achieves a THD of 0.6% at full output swing, providing a reliable and optimal solution for low voltage biomedical amplifier design. In addition, the technology selection for the implementation of the low noise amplifier is also discussed. A low noise amplifier was designed and fabricated using IBM 0.13μm process technology and the measurement results show that the advanced technology is not preferred for the low noise amplifier implementation, due to its higher flicker noise at low frequency. As a result, AMS 0.35μm process technology was chosen for the later designs, especially for those working at low frequency range of less than 1kHz.

Besides the restrict power consumption requirement, silicon area consumption is also a critical parameter for multi-channel designs. By moving the low-pass function in the system from the first stage to the second stage, the dilemma among the bandwidth requirement, input referred noise requirement and chip area is successfully eliminated. The fabricated 32-channel EEG sensor interface chip saves more than 50% silicon area compared to the existing designs. Furthermore, the proposed system architecture facilitates the power optimization of the individual functional block, where the average power per channel of the proposed chip is about 2.8% of the current-state-of-the-art multi-channel design.

The measurement results and comparisons with the currently published designs indicate that these developed low power low noise sensor interface prototypes are capable for biopotential signal acquisitions. They achieved better or comparable performance with much lower power consumption and smaller chip area, providing an optimum and robust solution for the low power low noise biomedical sensor interface design.

## 6.2 Future Works

The research conducted over the past four years focus on the design of the analog front-end circuits dedicated for biopotential signals acquisition. The proposed system realizes the basic and primary functions of signal amplification and conditioning. To improve the robustness and versatility of the system, some other secondary functions may be required, such as electrode impedance measurement, micro-controller, memory, and wireless transceiver. Furthermore, it may be necessary to integrate many

amplifiers with different functions into one single chip, such as ECG amplifier, blood pressure amplifier, temperature amplifier, accelerator amplifier, etc. By doing so, one sensor node will be able to manage different type of biopotential signals and meet various recording requirements of the person under monitoring. In summary, a system-on-chip solution for biomedical sensors is the next step forward.

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