FABRICATION AND CHARACTERISTICS OF HIGH-κ MIM CAPACITORS FOR HIGH PRECISION APPLICAITONS

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ABSTRACT

The Metal-Insulator-Metal (MIM) capacitor has been proposed as the next generation capacitors for precision Radio Frequency (RF) and Analog/Mixed-Signal (AMS) ICs applications, due to its advantages of depletion–free, high–conductance electrodes and minimized capacitance loss to Si substrate. Conventional dielectric materials for MIM capacitors, such as SiO_2, Si_3N_4, cannot satisfy the requirements of both high-quality and high-density MIM capacitors in the near future according to ITRS roadmap. The integration of high-κ materials to realize high capacitance density and low Voltage Coefficient of Capacitance (VCC) in a cost effective way is imperative.

In this thesis, a systematic research has been done for high-κ MIM capacitors using Sm_2O_3 dielectric as base dielectrics. Firstly, the electrical characteristics of Sm_2O_3 MIM capacitors with various Sm_2O_3 thicknesses are investigated, including voltage linearity and leakage current density. The physical characteristics of Sm_2O_3 based high-κ MIM capacitor is studied by using techniques such as Transmission Electron Microscopy (TEM), X-Ray Diffraction (XRD) and X-ray Photoelectron Spectroscopy (XPS), in which the dielectric constant, crystalline structure are examined.

Secondly, the effects of Plasma Treatments (PT) with O_2 and/or N_2 on the performance of MIM capacitors with Sm_2O_3 dielectric are investigated. It will be shown that plasma treatment after Sm_2O_3 dielectric formation can effectively reduce

both the quadratic and linear VCC, hysteresis. Also the leakage current density can be significantly improved. These results indicate that plasma treatment after dielectric formation is an effective way to improve the performance of high-κ dielectric MIM capacitors for precision circuit applications. The excellent electrical characteristics of Sm_2O_3 MIM capacitors indicate that it is a promising candidate for the application of high-κ dielectric MIM capacitors.

Thirdly, the MIM capacitors of Sm_2O_3 stacked with a thin SiO_2 layer to modulate the effective VCC are investigated. By using the "cancelling effect" of the positive quadratic VCC of Sm_2O_3 and the negative quadratic VCC of SiO_2, MIM capacitors with high capacitance density, low quadratic VCC and leakage current density are successfully demonstrated. Such "cancelling effect" of SiO_2 and Sm_2O_3 dielectrics can be further optimized to obtain higher capacitance density and near zero quadratic VCC.

Finally, a systematic study of the influence of metal electrodes on the performance of Sm_2O_3 MIM capacitors is performed. The improvement of electrical characteristics is demonstrated by using high work-function metal electrodes while low work-function metal electrodes show negative effects. The possible reasons of the interfacial layer formation are discussed.

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CHAPTER 1
INTRODUCTION

1.1. Radio Frequency and Analog/Mixed-Signal Technology

1.1.1. Background

Radio Frequency (RF) and Analog/Mixed-Signal (AMS) technologies show essential and critical technologies for many semiconductor and Integrated Circuits (ICs) products. Such technologies now serve the rapidly growing market of both internet and wireless communications, such as hand phones and other wireless devices. RF/AMS circuits process radio signals (analog signals) and digital data, some of which includes RF, analog, digital to analog and analog to digital conversions. These technologies depend on many materials and processing technologies, some of which are compatible with Complementary Metal Oxide Semiconductor (CMOS) processing and others are not, e.g., those compound semiconductors.

The drivers for most of RF/AMS products are cost, frequency bands, power consumption, functionality, size, production volume, standards and protocols. Considering these requirements and also being required to perform according to preset standard specifications, scaling transistor dimensions alone is insufficient for

these products. Therefore, a technology of "System-on-a-Chip (SoC)" to integrate the Digital Signal Processors (DSP) with other analog functions was developed. This technology can maintain a competitive edge for these RF/AMS products with comparable cost and performance.

1.1.2. On chip and Embedded Passives for RF and Analog Technology

Passive components include resistors, capacitors, inductors, varactors, transformers, and transmission lines. These components are frequently used for impedance matching, resonance circuits, filters, and bias circuits in Radio Frequency Integrated Circuits (RFICs). Unlike active devices such as Metal Oxide Semiconductor Field Emission Transistor (MOSFET) in the Ultra Large Scale Integrated circuit (ULSI) technology for digital CMOS ICs, the performance of many RF/AMS circuits are mainly determined by the performance of these passive elements. This is because that even in some RF circuits, the performance of RF/AMS CMOS transistors is usually good enough for most of the applications well beyond 10 GHz [1.1].

Integrating passives components into RF/AMS ICs has been now progressing in the era of SoC in order to realize RF/AMS CMOS technology with high performance and low cost, particularly for some consumer electronic devices. When incorporating such passives component into a standard CMOS process, some additional processing steps such as photolithography are needed. Moreover, new

materials such as using high-permittivity (κ) dielectrics may be also required to obtain better passive performance. This is because that these passive components, such as capacitors and inductors, usually occupy much more chip area than active devices. To obtain smaller die size, another optimization scheme or research should be performed to increase the capacitance density. This might be realized by extra process steps or adding process complexity such as introducing new materials or new device structures. The requirements for embedded passive components are the same to those of surface mount passive components. Embedded passives technologies involve additional material such as using high-κ dielectric for capacitors, resistive layer for resistors, and high permeability material for inductors.

1.2. Metal-Insulator-Metal Capacitors for Applications of RF and Analog ICs

Among these basic passive devices, capacitor is one of the essential elements, which are usually employed for decoupling, filtering and oscillating in the applications of RF/AMS ICs [1.2]. Conventional capacitors are Polysilicon-Insulator-Polysilicon (PIP) and MOS devices [1.3, 1.4]. However, polysilicon electrode has the unavoidable depletion effects and large sheet resistance, which cannot be accepted for the high precision requirements for scaled processing technologies [1.5, 1.6]. Therefore, a capacitor with metal electrodes, which is known as Metal-Insulator-Metal (MIM) capacitor, has been developed.

The key parameters of MIM capacitors for RF applications are capacitance

density, voltage linearity, leakage, matching and quality (*Q*) factor [1.1]. Higher capacitance density is required because of capacitor area scaling. The matching tolerances become smaller also due to the capacitance area scaling down. According to the International Technology Roadmap for Semiconductors 2007 (ITRS roadmap), the main requirements and specifications of short term and long term for MIM capacitors are summarized in Table 1.1 and Table 1.2, respectively, where aggressive projections have been extent to year 2022 with ever increased performance requirements. The detailed requirements will be presented in Chapter 2.

Table 1.1. On-Chip Passive Technology Requirements — Short-term.

Year of Production	2009	2010	2011	2012	2013	2014	2015
Metal-Insulator-metal Capacitor							
Density (fF/μm^2)	4	5	5	5	7	7	7
Voltage linearity (ppm/V^2)	<100	<100	<100	<100	<100	<100	<100
Leakage (A/cm^2)	<1e-8	<1e-8	<1e-8	<1e-8	<1e-8	<1e-8	<1e-8
σ Matching (%•μm)	0.5	0.5	0.4	0.4	0.3	0.3	0.3
Q (5GHz for 1pF)	>50	>50	>50	>50	>50	>50	>50
MOM Capacitor							
Density (fF/μm^2)	5.3	6.2	7.0	6.5	7.5	8.6	9.9
Voltage linearity (ppm/V^2)	<100	<100	<100	<100	<100	<100	<100
s Matching (% for 1pF)	<0.15	<0.15	<0.15	<0.15	<0.1	<0.1	<0.1

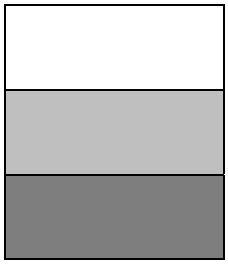
Table 1.2. On-Chip Passive Technology Requirements — Long-term.

Year of Production	2018	2020	2022
Metal-Insulator-metal Capacitor			
Density (fF/μm^2)	10	12	12
Voltage linearity (ppm/V^2)	<100	<100	<100
Leakage (A/cm^2)	<1e-8	<1e-8	<1e-8
σ Matching (%•μm)	0.2	0.2	0.2
Q (5GHz for 1pF)	>50	>50	>50
MOM Capacitor			
Density (fF/μm^2)	15.1	20.0	26.4
Voltage linearity (ppm/V^2)	<100	<100	<100
s Matching (% for 1pF)	<0.1	<0.08	<0.08

Manufacturable Solutions Exist, and are being optimized

Manufacturable Solutions are known

Manufacturable Solutions are no known



1.3. Thesis Outline and Contributions

In Chapter 2, the key parameters of MIM capacitors for high precision circuit applications are detailedly introduced and a systematic review of recent studies on

high-κ dielectric MIM capacitors is presented.

In Chapter 3, the electrical and physical characteristics of MIM capacitors with a single Sm_2O_3 dielectric have been systematically investigated. Moreover, the influence of plasma treatment on the performance of Sm_2O_3 MIM capacitors has been described. Plasma treatment in N_2 ambient after dielectric formation can be utilized to improve the performance of high-κ dielectric MIM capacitors.

In Chapter 4, the MIM capacitors of Sm_2O_3 stacked with a Physical Vapor Deposition (PVD) or a Plasma Enhanced Chemical Vapor Deposition **(**PECVD) SiO_2 layer have been fabricated and characterized. The application of using a thin SiO_2 layer to modulation the voltage linearity of whole dielectric stack is presented.

In Chapter 5, the influence of metal electrodes on the performance of Sm_2O_3 MIM capacitors has been systematically investigated. The improvement of electrical characteristics by using high work-function metal electrodes is presented.

Finally, Chapter 6 concludes with suggestions for future work based on the conclusion of this thesis.

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CHAPTER 2

LITERATURE AND TECHNOLIGY REVIEW

2.1. Metal-Insulator-Metal Capacitors

For the capacitors used in the applications of RF/AMS ICs, precision capacitance control within different bias voltage and temperature is required. Traditional Polysilicon-Insulator-Polysilicon (PIP) capacitors cannot be tolerated in RF/AMS ICs due to the undesirable depletion effects of polysilicon electrodes [2.1-2.4]. Although cross-coupled capacitors have been employed to alleviate the capacitance variation [2.1], the resistivity of capacitors is large, and quality factor (Q) is poor due to the excessive capacitance-loss to the substrate. Therefore, the requirement of capacitor electrodes with little or no depletion effects motives the employment of metal electrodes. It is generally known as Metal-Insulator-Metal (MIM) structures.

The MIM capacitor has been proposed as the next generation capacitor for RF/AMS ICs applications, due to its advantages of depletion–free, high–conductance electrodes and minimized capacitance loss to Si substrate [2.5-2.9]. Fig. 2.1 shows the typical schematic of MIM capacitor in the AlCu Back-End of Line (BEoL). There is a thin metal electrode inserted between the two metal layers. The conventional dielectrics used in industries are usually SiO_2 or Si_3N_4 which are

deposited by PECVD at the low-temperature process below 500 ^{o}C. The capacitors are usually done between the last top two metal layers so as to reduce the substrate coupling effect.

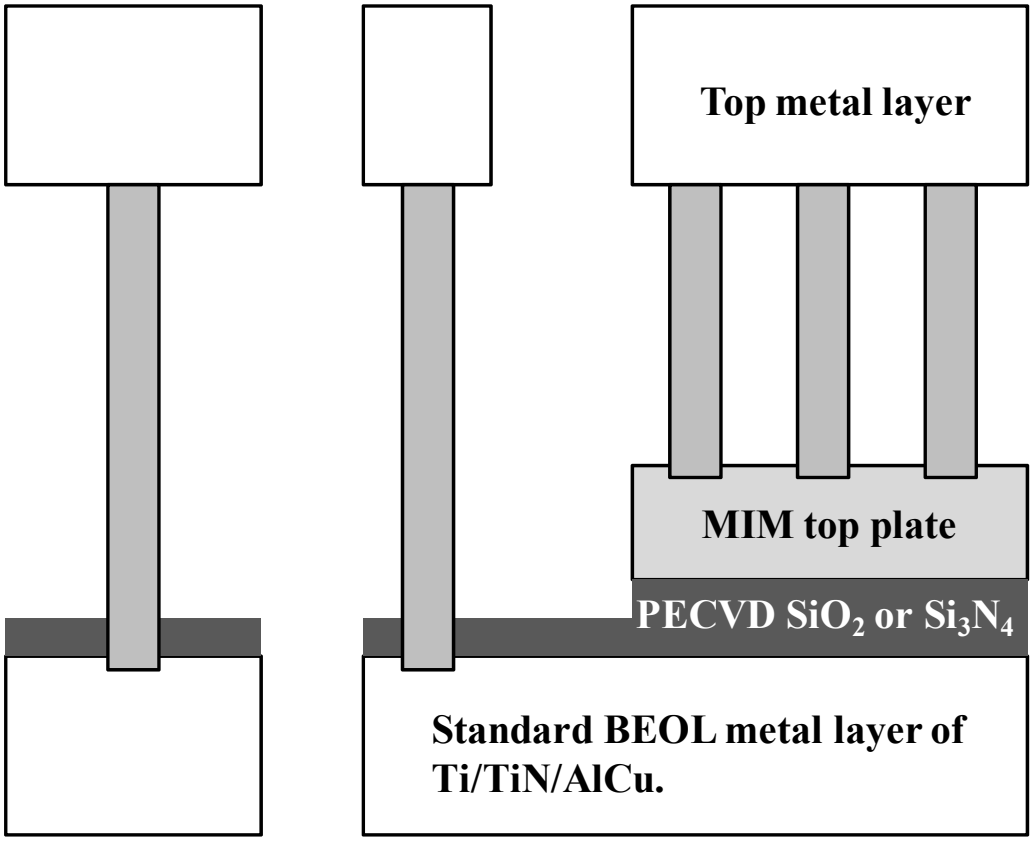

Fig. 2.1. Typical schematic of MIM capacitor used in the AlCu BEoL.

2.2. Parameters of MIM Capacitors for the Applications of RF/AMS ICs

The key parameters for MIM capacitors in the application of RF/AMS ICs are capacitance density, voltage linearity, leakage current density, matching and *Q* factor [2.10]. The details of specified requirements are list below:

(1) Capacitance density

Capacitance density is one of the essential issues of MIM capacitors because capacitors usually occupy much area in a chip. The areal percentage of capacitor significantly increases within the scaling down of ICs. To increase the capacitance per unit area can improve the capacitor integration and thus reduce the cost.

(2) Voltage linearity

The variation of capacitance with the applied voltage is known as the Voltage Coefficient of Capacitance (VCC), as shown in Fig. 2.2. The precision capacitance control needs small capacitance variation with the applied voltage varied.

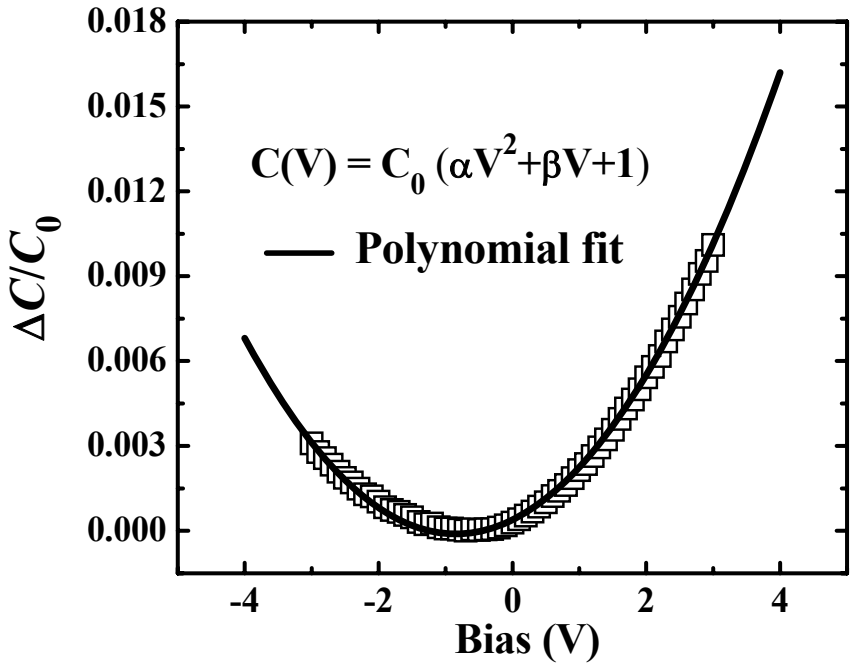

Figure 2.2. Polynomial fitting of a typical *C-V* curve. The fitting is performed from positive voltage to negative or reverse.

Usually VCC can be approximated by equation 2.1.

$$C(V) = C_0 (\alpha V^2 + \beta V + 1) \text{ [2.9]}, \qquad (2.1)$$

where V is the voltage applied between the electrodes of the capacitor, and C_0 is the capacitance at zero voltage. α, β are the quadratic and linear VCC, respectively. The quadratic VCC (α value) is critical for the dynamic range of analog circuit [2.10]. The linear VCC (β value) can be cancelled out by differential techniques such as cross-coupled arrangement [2.1].

(3) Temperature coefficient of capacitance (TCC)

The temperature coefficient of capacitance (TCC) is an important parameter of MIM capacitors as the actual device temperature during the circuit operation is usually much higher than room temperature and is usually expressed in ppm/ºC. TCC describes the maximum change in capacitance over a specified temperature range. TCC can be usually defined as:

$$TCC = \frac{10^6}{T}\frac{dC}{dT} ppm/^oC \text{ [2.11, 2.12]} \qquad (2.2)$$

TCC is usually positive because of the effect of larger inter-atomic space at higher temperature, which allows a larger dipole moment in the presence of an electric field [2.13, 2.14]. A TCC parameter which is under about 200 ppm/ºC is considered low.

(4) Leakage current density (*J*)

Leakage current density (*J*) is defined at room temperature and for the highest end of the supply voltage range for precision analog device. The requirement of low leakage current density is obvious.

(5) Quality factor (*Q*)

The quality factor (*Q*) is the reciprocal of the dissipation factor. If the mobile charges cannot respond enough to the changing fields or if there are resistive losses in the dielectric or capacitor electrodes, the current and voltage might deviate from the ideal value of 90^{o}. The difference of this angular and 90^{o} is called the loss angle (δ). The tangent of this loss angle is called the loss tangent (dissipation factor), and is zero for a capacitor that does not dissipate wasted energy.

Planar structures were usually implemented for MIM capacitors integrated in BEOL process, and positioning the capacitors beneath the final metal level could further minimize the loss to the substrate. Moreover, the fabrication of MIM capacitors needs to be compatible to the existing ULSI BEoL technology. That is, high quality dielectrics and electrodes have to be formed at a low temperature of ~400^{o}C which is limited by backend process.

2.3. Literature Review

As the continuous scaling down of CMOS technology, it is inevitable to increase the capacitance per unit area to save chip area, especially in the applications of RF/AMS ICs. Therefore, MIM capacitors draw great attentions among semiconductor industry companies in the very recent years. Conventional dielectric materials for MIM capacitors in current technology node, such as SiO_2, Si_3N_4, have been investigated and optimized to meet this requirement [2.6-2.10, 2.15, and 2.16]. Si_3N_4 has a higher dielectric permittivity (κ) of 7 as compared to that of SiO_2 (~3.9), which usually provides relatively higher capacitance density than SiO_2 MIM capacitors [2.17]. Much effort has been performed to improve the performance, including voltage linearity and breakdown field [2.18-2.21].

SiO_2 and Si_3N_4 MIM capacitors with excellent electrical performance have been successfully demonstrated in Al and Cu BEoL process. However, the capacitance density are low, usually ≤ 2 fF/μm^2 due to the small dielectric permittivity (κ) of SiO_2 (~3.9) and Si_3N_4 (~7). Although further reduced dielectric thicknesses of SiO_2 and Si_3N_4 can increase the capacitance density, it may offset leakage current, breakdown voltage, and voltage linearity properties. In short, the capacitance density of MIM capacitors using conventional SiO_2 and Si_3N_4 dielectrics cannot satisfy the requirements of both high-quality and high-density MIM capacitors in the near future according to ITRS roadmap [2.10]. The integration of new materials to realize high capacitance density and low VCC in a cost effective way is imperative.

Therefore, high-permittivity (κ) dielectrics have been introduced for MIM capacitors applications. These high-κ dielectrics are usually metal oxides, such as HfO_2, which have been developed for gate dielectrics of future node. The most important advantage of the high-k dielectrics rather than SiO_2 or Si_3N_4 is to provide a physically thicker film for leakage current reduction while improving the capacitance by higher permittivity, as described in equation 2-3,

$$EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} T_{high-k,phy} \qquad (2\text{-}3)$$

where EOT is the Equivalent Oxide Thickness of high-k dielectric, ε_{SiO2} and $\varepsilon_{high\text{-}k}$ are the permittivity of SiO_2 (3.9) and the high-k dielectrics, respectively, and $T_{\text{high-}k,\text{phy}}$ is the physical thickness of the high-k film.

In searching suitable high-κ dielectric materials for MIM capacitors, a simple criterion is high dielectric permittivity (κ) and high band-gap. The decrease of band-gap is usually coupled with the reduction of breakdown voltage for dielectric materials. Table 2.1 summarizes the experimental band gaps and dielectric permittivity for a compilation of a few potential high-κ dielectric candidates [2.22, 2.23].

The relationship of dielectric permittivity (κ) versus band-gap is summarized in Fig. 2.3 [2.22]. With the increasing of κ value for dielectrics, the band-gap is usually reduced.

Table 2.1. Comparison of dielectric permittivity, gap energy and for different high-κ dielectric candidates, including SiO_2 and Si_3N_4.

Material	Dielectric permittivity (κ)	Gap energy E_g (eV)
SiO_2	3.9	8.9
Si_3N_4	7	5.1
Al_2O_3	9	8.7
Y_2O_3	15	5.6
La_2O_3	30	4.3
Ta_2O_5	26	4.5
TiO_2	80	3.05
HfO_2	25	5.7
ZrO_2	25	7.8
$ZrSiO_4$	10 – 12	~6
$HfSiO_4$	~10	~6

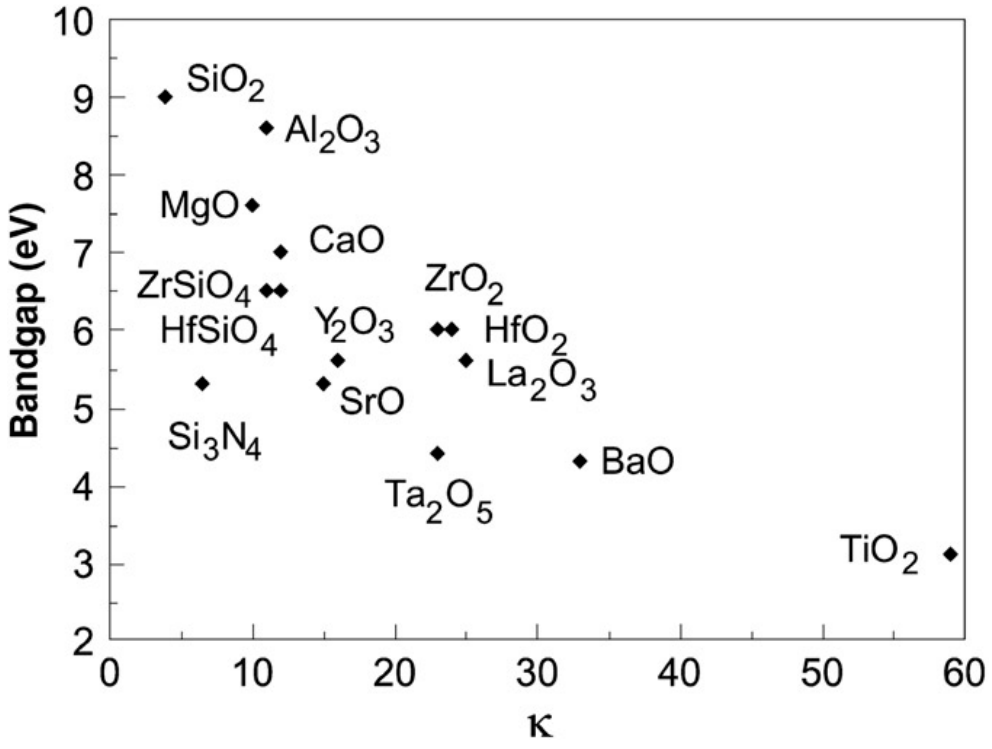

Figure 2.3. Dielectric permittivity κ versus band gap for oxides [2.22]. It is observed that dielectric with higher permittivity usually has lower band-gap.

Among these high-κ dielectrics, binary dielectrics such as Al_2O_3, HfO_2, and Ta_2O_5, are the most popular high-κ dielectrics studied in recent years to explore high capacitance density. Moreover, ternary or even fourfold metal oxides have been attempted to obtain higher capacitance density and high quality dielectrics. Furthermore, in order to reduce voltage linearity and leakage current density, the stacking of different high-κ dielectrics or a thin SiO_2 layer has been also fabricated and characterized.

However, these single or stacked high-κ dielectric MIM capacitors were often done with different unit capacitance, and thus these reported electrical characteristics, such as VCC, are at different frequencies, i.e., 100 kHz, 1 MHz, or even 1 GHz. It is difficult to compare and judge their performance.

2.3.1. Binary Metal Oxides

Binary metal oxides are known the most popular high-κ dielectrics investigated for future gate dielectrics. The application of these binary high-κ dielectrics in MIM capacitors has been demonstrated recently [2.22-2.25]. Al_2O_3 MIM capacitor has exhibited the great characteristics of low TCC, low loss tangent and small frequency dispersion [2.26, 2.27]. As the dielectric energy band-gap of Al_2O_3 is high (8.7 eV), it also gives rise to low leakage current density [2.23]. The capacitance of 5.2 $fF/\mu m^2$ and low leakage current density of 4.3×10^{-8} A/cm^2 at 1 V was demonstrated with sputter (PVD) Al_2O_3 [2.26]. The quadratic and linear VCC reported are 2051

ppm/V^2 and 1888 ppm/V at 1 MHz, respectively. However, its dielectric permittivity (~9) is pretty low, as compared to those of other high-κ dielectrics, such as Ta_2O_5 (~26) and HfO_2 (~25). This makes it less attractive to be employed in the application of high-κ dielectric MIM capacitors. Moreover, its voltage and temperature linearity are poor [2.28, 2.29].

Ta_2O_5 appears to be the candidate of MIM capacitor dielectrics since it has been used in DRAM for more than one decade. Ta_2O_5 can be deposited at temperature of low than 500 ^oC, which is suitable for MIM capacitors in the BEoL. Moreover, the dielectric permittivity of Ta_2O_5 (~26) is about 2 times higher than that of Al_2O_3 (~9). There are several deposition techniques available for this dielectric, such as Metal-Organic Chemical Vapor Deposition (MOCVD) [2.30], Atomic-Layer Deposition (ALD) [2.31], PECVD [2.32] [2.33], and Low Pressure Chemical Vapor Deposition (LPCVD) [2.33]. The best reported Ta_2O_5 MIM is with 4 fF/μm^2 of capacitance density, -9.9 [2.34] to 13 ppm/V^2 [2.28] of quadratic VCC and 106-84 ppm/^oC of TCC. However, its leakage current density at 3.3 V and 125 ^oC is about 5 $\times 10^{-5}$ A/cm^2, which is much larger than other high-κ dielectrics, such as Al_2O_3, HfO_2. The poor leakage performance makes it difficult to be accepted in the RF/AMS applications.

HfO_2 for gate dielectrics of Metal-Oxide-Semiconductor (MOS) devices has been widely studied. It has the advantages of high dielectric constant (~25), high heat of formation (271 Kcal/mol), and large band gap (5.7 eV) [2.22]. The excellent

thermal stability and high band gap make it a promising candidate for high-κ dielectric MIM capacitors. The reported capacitance density of HfO_2 MIM capacitor is varied from 5 to 13.7 fF/μm^2 by using ALD-deposited HfO_2 [2.35-2.37]. For the HfO_2 MIM capacitors with capacitance density of 5 fF/μm^2, the quadratic and linear VCC can reach 238 ppm/V^2 and 206 ppm/V, respectively, at the frequency of 1 MHz [2.35]. Another reported HfO_2 for MIM capacitor application were demonstrated by using a Pulsed-Laser Deposition (PLD) [2.36] and PVD methods [2.37].

Other binary metal oxides for high-κ MIM capacitors, such as Y_2O_3 [2.38], La_2O_3 [2.39] and TiO_2 [2.40], have been also fabricated and characterized to study the electrical characteristics in the applications of RF/AMS ICs. Their reported capacitance densities are 2.2, 9.2, and 28 fF/μm^2 for Y_2O_3, La_2O_3 and TiO_2 MIM capacitors, respectively. In these reports, their corresponding quadratic VCC are 110, 3000 and 5010 ppm/V^2, respectively.

Table 2.2 summarizes the electrical characteristics of binary high-κ dielectrics for MIM capacitors. The defaulted measured frequency is 100 kHz. Those un-reported characteristics are marked with "–".

Table 2.2. List of electrical characteristics of binary high-κ dielectric MIM capacitors reported recently.

	High-κ dielectric **Top/bottom metal**	**Cap. Density (fF/μm^2)**	**Leakage (A/cm^2)**	**Q.VCC** **α (ppm/V^2)**	**L.VCC** **β (ppm/V)**	**TCC** **(ppm/^{o}C)**
1	PVD Al_2O_3 [2.26] Al/ Pt	5.2	4.3×10^{-8}@ 1V	2051 @ 1 MHz	1888 @ 1 MHz	–

2	Al_2O_3 [2.34] TiN/ TiN	4	5×10^{-9}@ 3.3V, 125C	468	–	254
3	MOCVD Ta_2O_5 [2.34] TiN/ TiN	4	6×10^{-5}@ 3.3V, 125C	-9.9	–	106
4	MOCVD Ta_2O_5 [2.28] Cu/ Cu	4	5×10^{-5}@ 3.3V, 125C	13	25	84
5	MOCVD HfO_2 [2.34] TiN/ TiN	4	7×10^{-9}@ 3.3V, 125C	468	–	254
6	ALD HfO_2 [2.35] Ta/ Ta	13	1.55×10^{-6}@ 1V, 125C	5000	6000	–
7	ALD HfO_2 [2.35] Ta/ Ta	8	–	1800	4000	–
8	ALD HfO_2 [2.35] Ta/ Ta	5	–	700	2500	–
9	ALD HfO_2 [2.35] Ta/ Ta	13	–	800 @ 1 MHz	600 @ 1 MHz	–
10	ALD HfO_2 [2.35] Ta/ Ta	8	–	400 @ 1 MHz	110 @ 1 MHz	–
11	ALD HfO_2 [2.35] Ta/ Ta	5	–	238 @ 1 MHz	100 @ 1 MHz	–
12	PVD HfO_2 [2.37] Ta/ TaN	13.7	4×10^{-4}@ 3.3V, 125C	4631	-4843	135
13	MOCVD Y_2O_3 [2.38] TiN/ TiN	2.2	1×10^{-8}@ 10V	120	470	–
14	PVD La_2O_3 [2.39] Al/ Pt	9.2	$<1\times10^{-5}$@ -1V	~ 3000	~3000	347
15	PVD TiO_2 [2.40] Ir/ TaN	28	3×10^{-8}@ -1V	5010 @ 500 kHz	–	353

2.3.2. Ternary Metal Oxides and Above

The aforementioned binary metal oxides for high-κ dielectric MIM capacitors can obtain high capacitance density up to 28 fF/μm^2. However, the requirements for both small VCC and low leakage current density cannot be satisfied. Most of these high-κ dielectrics show large positive quadratic VCC, which cannot be accepted for precision analog circuit applications. Moreover, the improvement of the leakage current density is limited by the low band-gap, such as Ta_2O_5 (4.5 eV), TiO_2 (3.05 eV) [2.23]. Although Al_2O_3 has comparable band-gap (8.7 eV) with that of SiO_2 (8.9 eV), its dielectric permittivity is too low to obtain high capacitance density. Therefore, people have attempted to introduce other elements into binary metal oxides or combine these dielectrics to utilize their own advantages to improve voltage linearity and leakage current density.

The intermixing of HfO_2 and Al_2O_3 to form Hf-Al-O dielectrics is investigated for the merits of high permittivity of HfO_2 and high energy band-gap of Al_2O_3 [2.41]. The capacitance density of 3.5 fF/μm^2 and low quadratic VCC of 190 ppm/V^2 are obtained by varying the chemical composition of HfO_2 or Al_2O_3. Another way is to use lanthanide-doped HfO_2 to suppress leakage current density [2.37]. The reported leakage current density with the capacitance density of 13.3 fF/μm^2 for Hf-Tb-O MIM capacitors is successfully reduced from 4×10^{-4} A/cm^2 to 2×10^{-7} A/cm^2 at 3.3 V by doping 4% Tb into HfO_2. Other ternary metal oxides, such as TaZrO [2.42], SrTaO [2.43], and BiTaO [2.43], have also demonstrated low leakage current density.

Leakage current densities of lower than 1×10^{-8} A/cm^2 at 3 V were reported for SrTaO and BiTaO MIM capacitors by using Pt electrodes. However, Pt electrode is hard to be dry-etched as the by-product is nonvolatile.

To further increase the capacitance density, TiO_2 dielectric mixed with other high-κ dielectrics have been studied as TiO_2 has relatively high dielectric permittivity (~80) but with low energy band-gap [23]. $AlTiO_X$ MIM capacitor with high capacitance density of around 10 fF/μm^2 was reported [2.26]. However, the leakage current density is still poor. Other Ti doped metal oxides for MIM capacitors, such as $PrTi_XO_Y$ [2.44], TaTiO [2.45], TiHfO, [2.46], $Sm_2Ti_2O_7$ [2.47], $BaSm_2Ti_4O_{12}$ [2.47], and $SrTiO_3$ [2.48], can obtain high capacitance densities and relatively low leakage current densities as compared to that of TiO_2 MIM capacitors. For example, TaTiO MIM capacitor can demonstrate the capacitance density of 23 fF/μm^2 and leakage current density of 1×10^{-6} A/cm^2 at 1V. Although some performance improvement have been obtained by combining TiO_2 with other high-κ dielectrics, the leakage current density is still an issue due to the low band-gap of TiO_2.

The electrical characteristics of the ternary or above high-κ dielectrics have been summarized, as shown in Table 2.3. The defaulted measured frequency is 100 kHz. The “one side fit” means that the VCCs are extracted from *C-V* curves by data fitting at only one side, i.e., positive voltage side. Conventional data fitting for VCCs is done from positive to negative sides (or reverse). The results with “one side fit” are not comparable to those extracted at both sides.

Table 2.3. List of electrical characteristics of ternary and above high-κ MIM capacitors reported recently.

	High-κ dielectric **Top/bottom metal**	**Cap. Density ($fF/\mu m^2$)**	**Leakage (A/cm^2)**	**Q.VCC** **α (ppm/V^2)**	**L.VCC** **β (ppm/V)**	**TCC** **(ppm/°C)**
1	ALD HfAlO [2.41] Ta/ Ta	3.5	$<1.1\times10^{-6}$@ 3V	~190	~300	–
2	PVD Hf-Tb-O [2.37] Ta/ TaN	13.3	2×10^{-7}@ 3.3V	2667	332	–
3	TaZrO [2.42] TaN/ Ta	12	$<1\times10^{-8}$@ 1V	1236	–	240
4	SrTaO [2.43] Pt/ Pt	10	1×10^{-8}@ 3V	200 @ 1 MHz	300 @ 1 MHz	–
5	BiTaO [2.43] Pt/ Pt	10	1×10^{-8}@ 3V	300 @ 1 MHz	40 @ 1 MHz	–
6	PVD $AlTiO_X$ [2.26] Al/ Pt	10	1 @1V	–	–	–
7	PVD $PrTi_XO_Y$ [2.44] Al/ TiN	5	–	>1000 @ 1 MHz	–	–
8	PVD TaTiO [2.45] Al/ TaN	23	1.2×10^{-6}@ 1V	81 @ 1 GHz	98 @ 1 GHz	391 @1 MHz
9	PVD TiHfO [2.46] TaN/ Ni	10.8	9×10^{-9}@ 2V	447 One side fit	132	–
10	PVD TiHfO [2.46] TaN/ Al	10.6	2×10^{-7}@ 2V	935 One side fit	3620	–
11	$Sm_2Ti_2O_7$ [2.47] Pt/ Pt	4.84	1.63×10^{-9}@ 1V	-295	684	-136
12	$BaSm_2Ti_4O_{12}$ [2.47] Pt/ Pt	3.47	0.26×10^{-9}@ 2V	-89.3	-0.9	-122

13	$BaTi_4O_9$ [2.48] Pt/ Pt	4.58	1.07×10^{-9}@ 1V	-65.4	-44	126.6
14	PVD SrTiO3 [2.49] TaN/ TaN	28	3×10^{-8}@ 2V	589 One side fit	–	747

2.3.3. Stacked or Multi-layered Metal Oxides

Although by introducing another element into binary metal oxides can obtain some performance improvements, these achievements are not prominent to satisfy the ITRS's requirements of high capacitance density, low leakage current density and small voltage linearity. Most of these MIM capacitors with single high-κ dielectric are found to show large positive quadratic VCC. Recently, numerous attempts have been performed to engineer these dielectrics, such as bi-layer or multiple laminated dielectric structures, particularly for those binary metal oxides, to improve the leakage current density and voltage linearity.

The stacking of Ta_2O_5 with other high-κ dielectrics for MIM capacitors have been fabricated and characterized [2.28, 2.34, and 2.50]. This is because Ta_2O_5 dielectrics demonstrate excellent VCC characteristics and relative high dielectric permittivity but poor leakage current density. The capacitance density of 4.4 ~ 9.2 $fF/\mu m^2$ and leakage current density lower than 1×10^7 A/cm^2 for Ta_2O_5/Al_2O_3 MIM capacitors are demonstrated. The laminating of Ta_2O_5/Al_2O_3 or sandwiching of Ta_2O_5 between Al_2O_3 [2.50] can successfully reduce the leakage current density as Al_2O_3 can be an barrier for oxygen diffusion to bottom metal contact interface during

Ta_2O_5 deposition.

Moreover, $Ta_2O_5/Al_2O_3/Ta_2O_5$ and $Ta_2O_5/HfO_2/Ta_2O_5$ MIM capacitors [34] for MIM capacitors were recently investigated with the consideration of the excellent leakage current density of Al_2O_3 and HfO_2 dielectric layers. Furthermore, after NH_3 plasma treatment on the electrodes, both leakage current density and VCC can be significantly improved. This is possible due to the elimination of parasitic capacitors which originated from the depletion or defects between top/bottom electrodes and dielectrics. After NH_3 plasma treatment, the capacitance density of 4 $fF/\mu m^2$ and quadratic VCC of 16.9 ppm/V^2 for $Ta_2O_5/HfO_2/Ta_2O_5$ stacked MIM capacitor are demonstrated. The reported leakage current density is midrange between the single layer of Ta_2O_5 and HfO_2 MIM capacitors, $\sim 1\times10^{-7}$ A/cm^2 at voltage of 3.3 V and temperature of 125 ^oC.

A multiple laminated $Al_2O_3/HfO_2/Al_2O_3/HfO_2/Al_2O_3$ MIM capacitor with thicknesses of 1nm/5 nm/1 nm/5 nm/1 nm has been evaluated [2.51]. This dielectric stack aims to reduce the leakage current density via increasing the energy band-gap in the intermixed film after the addition of Al_2O_3 and improving the interface condition between electrodes and dielectrics. Another laminated $Al_2O_3/Pr_2O_3/Al_2O_3$ MIM capacitor for RF applications has been developed for the consideration of high band-gap of Al_2O_3 and large dielectric permittivity of Pr_2O_3 (15-30) [2.52]. This dielectric stack demonstrates the capacitance density of 5.7 $fF/\mu m^2$ and low leakage current density of 5×10^{-9} A/cm^2 at 1V.

Another well engineered high-κ dielectric stack is HfO_2/SiO_2 dielectric stack [2.53]. It makes use of the "cancelling effect" of negative quadratic VCC of SiO_2 and the large positive quadratic VCC of HfO_2 for RF MIM capacitors. Such compensation effect produced a MIM capacitor with the quadratic VCC of 14 ppm/V^2 and the capacitance density of 6 fF/μm^2. This excellent result demonstrates the realization of low quadratic VCC with high capacitance density. The electrical characteristics of these reported high-κ dielectric stacks for MIM capacitors are summarized in Table 2.4.

Table 2.4. List of electrical characteristics of stacked high-κ MIM capacitors reported.

	High-κ dielectric **Top/bottom metal**	**Cap. Density ($fF/\mu m^2$)**	**Leakage (A/cm^2)**	**Q.VCC** **α (ppm/V^2)**	**L.VCC** **β (ppm/V)**	**TCC** **(ppm/^oC)**
1	Ta_2O_5/Al_2O_3 [2.28] Cu/ Cu	3	~1×10^{-8}@ 3V	< 100	250	147
2	Ta_2O_5/Al_2O_3 [2.50] Ta/ Ta	9.2	~1×10^{-7}@ 3V	3580	2060	200
3	Ta_2O_5/Al_2O_3 [2.50] Ta/ Ta	4.4	~1×10^{-8}@ 1V	400	150	–
4	$Ta_2O_5/HfO_2/Ta_2O_5$ [2.34] TiN/ TiN	4	~1×10^{-7}@ 3.3V, 125C	16.9	5.2	–
5	$Al_2O_3/HfO_2/Al_2O_3$ [2.51] TaN/ TaN	12.8	~3.2×10^{-8}@ 3.3V	1990 @1 MHz	211	182
6	$Al_2O_3/HfO_2/Al_2O_3$ [2.51] TaN/ TaN	6	–	405 @1 MHz	-95	196
7	$Al_2O_3/HfO_2/Al_2O_3$ [2.51] TaN/ TaN	4	–	207 @1 MHz	-65	199

8	$Al_2O_3/Pr_2O_3/Al_2O_3$ [2.52] Au/ TiN	5.7	5×10^{-9}@ 1V	–	–	–
9	HfO_2/SiO_2 [2.53] TaN/ TaN	6	1×10^{-8}@ 3.3V	14	–	54

2.4. Summary

The single and stacked high-κ dielectric MIM capacitors have demonstrated much improvement in achieving high capacitance density, low leakage current density, and low voltage linearity. However, there are still areas need to be explored, especially on capacitance density and the quality of the interface between dielectrics and electrode. According to the requirements of ITRS 2007 [10], the capacitance density should be at least 5 and 7 fF/μm^2 through the year of 2010 and 2013 respectively and also keeping the quadratic VCC within the range of ±100 ppm/V^2. The solutions have not been found yet due to the large positive quadratic VCC of high-κ dielectrics, especially at high capacitance density. Although the stacking of HfO_2 with thin SiO_2 (having negative quadratic VCC) can obtain high capacitance density of up to 6 fF//μm^2, the further improvement of higher capacitance density is limited by the large quadratic VCC of HfO_2. It is essential to explore other suitable high-κ dielectrics which have lower quadratic VCC as compared to that of HfO_2 and high dielectric quality, especially at high capacitance density.

Not only the capacitance density, but also most high-κ materials are generally

more ionic due to the nature of metal oxides and more highly coordinated as compared to SiO_2 and Si_3N_4, the electrical characteristics are different from these amorphous dielectric films. The electrical performance is regarded to be dependent on the quality of the dielectrics and the dielectric/electrode interface. In addition, the high-κ dielectrics and dielectric stack are generally dispersive which leads to the frequency dependence (frequency dispersion) in VCC. This dispersive behavior is believed related to the existence of bulk-dielectric traps near the interface. Different traps might induce charges with different time constants and thus modulate capacitor charges at certain frequencies. When the applied frequency is high, VCC would be low since the induced charges are unable to follow the fast AC signal. Therefore, it is also essential to investigate the interface of the high-κ dielectric/electrode, especially the bottom electrode which would be exposed directly to dielectrics targets or the precursors during the dielectric deposition.

Moreover, the leakage current density is related to the interface and bulk-dielectric quality. The process temperature for MIM capacitors is limited by the temperature requirement of BEoL. Therefore, other treatments, such as post-deposition annealing and low temperature treatment, are needed to improve the dielectric quality and to suppress the leakage current density.

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CHAPTER 3

SAMARIUM OXIDE (Sm_2O_3) HIGH-κ DIELECTRIC FOR HIGH PERFORMANCE MIM CAPACITORS

3.1. Introduction

As discussed in Chapter 2, many high-κ dielectrics have been screened and investigated for MIM capacitors in the applications of RF/AMS ICs. High capacitance density can be realized by reducing the thickness and/or increasing the permittivity (κ) of the MIM dielectric materials. Moreover, some higher-κ dielectrics, such as TiO_2 [3.1], can demonstrate much higher capacitance density. However, leakage current density and reliability issues still limit thickness scaling of the MIM dielectrics. In addition, there are stringent requirements on the voltage coefficients of capacitance (VCC), including the quadratic VCC (α) and the linear VCC (β), for precision analog circuit applications.

According to the ITRS 2007 [3.2], the requirement for the capacitance density would be 7 fF/μm^2 by 2013 while the quadratic VCC should be kept within $\pm$100 ppm/V^2. The leakage current should be below 10^{-8} A/cm^2 at room temperature and at maximum supply voltage V_{DD}. Although the capacitance density and leakage current density can be tailored with different high-κ dielectrics in different combinations, most of these high-κ dielectrics are found to show large positive

quadratic VCC. This makes it difficult to achieve a high capacitance density while maintaining a quadratic VCC of less than ± 100 ppm/V^2 as the quadratic VCC usually increases with decreasing MIM dielectric thickness. Therefore, it is necessary to explore new high-κ dielectrics with smaller quadratic VCC and low leakage current density for future high-κ dielectric MIM capacitors.

Recently, lanthanoid oxides have been attracting people's attentions for high-κ dielectric applications in CMOS technology due to their high permittivity (κ) ranging from 10 to 30.5 and large energy band-gap [3.3-3.21]. These advantages make the potential using of lanthanoid oxides with high capacitance density and low leakage current density for high-κ dielectric MIM capacitors. Therefore, firstly, we have done a material screening by fabricating MIM capacitors with various lanthanoid oxides to explore the electrical and physical characteristics of lanthanoid oxides MIM capacitors in high precision applications. Among them, for the first time, we demonstrate the use of samarium oxide (Sm_2O_3) for high-κ dielectric MIM capacitors with a smaller quadratic VCC at a given high capacitance density, as compared to other high-κ dielectrics.

The MIM capacitors with a single Sm_2O_3 dielectric layer were fabricated and characterized in this chapter. The electrical characteristics of Sm_2O_3 MIM capacitors with various Sm_2O_3 thicknesses (various capacitance densities) are investigated for the first time, including the relationship of quadratic VCC and capacitance density, the dependence of quadratic VCC on frequency and the leakage current density.

Moreover, the physical characteristics of Sm_2O_3 MIM capacitors is studied by using techniques such as Transmission Electron Microscopy (TEM), X-Ray Diffraction (XRD) and X-ray Photoelectron Spectroscopy (XPS), in which the dielectric permittivity, crystalline structure, et,al, are examined. Furthermore, the effects of plasma treatments (PT) with O_2 and/or N_2 on the performance of MIM capacitors with Sm_2O_3 dielectric are investigated for the first time. It will be shown that plasma treatment on Sm_2O_3 dielectric in either O_2 or N_2 ambient can effectively reduce both the quadratic and linear VCC. The effects on leakage current density and hysteresis have been also evaluated.

3.2. Experiments

MIM capacitors were fabricated on Si wafers covered with a 400 nm thick thermally-grown SiO_2. A TaN/Ta layer as bottom electrode with the thickness of 50 nm/150 nm was deposited on the 400 nm thick SiO_2 layer by reactive sputtering in an Argon/Nitrogen (Ar/N_2) ambient. To form MIM capacitors with a single Sm_2O_3 dielectric, a Sm_2O_3 layer was directly deposited on the TaN bottom electrode by sputtering at room temperature in Ar ambient. The thickness of the Sm_2O_3 layer was controlled by adjusting the sputtering time. For the investigation of plasma treatment (PT) effects, plasma treatments were performed in N_2 or O_2 ambient by an Inductively Coupled Plasma (ICP) at different steps of the capacitor formation: after bottom electrode formation; after dielectric formation; or in both steps. Following

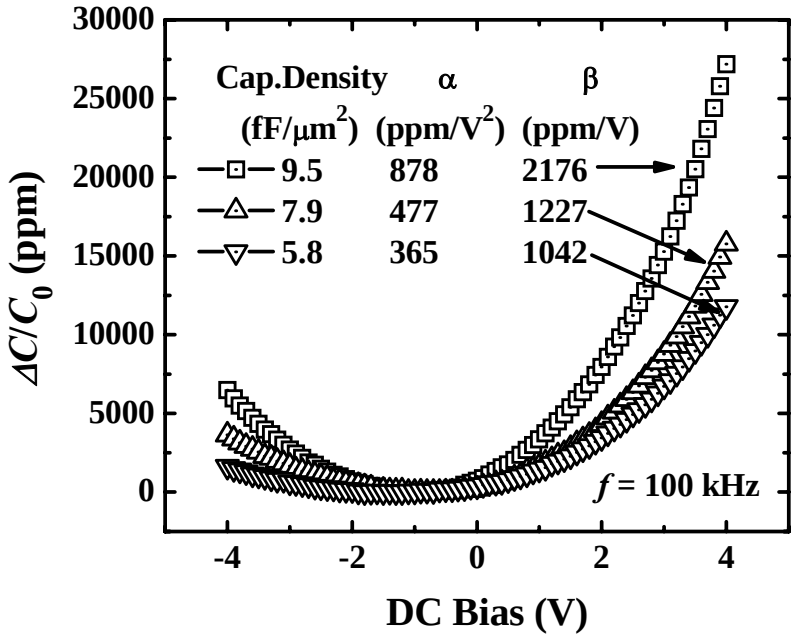
that, Post- Deposition Annealing (PDA) at 400 °C for 120 s in an N_2 ambient was then performed for all samples. Finally, a 150 nm thick top TaN layer was sputtered and patterned to form the top electrode.

Capacitance and leakage current were measured by using a HP4284A precision LCR meter and a HP4156A precision semiconductor parameter analyzer, respectively on 200×200 μm^2 capacitors.

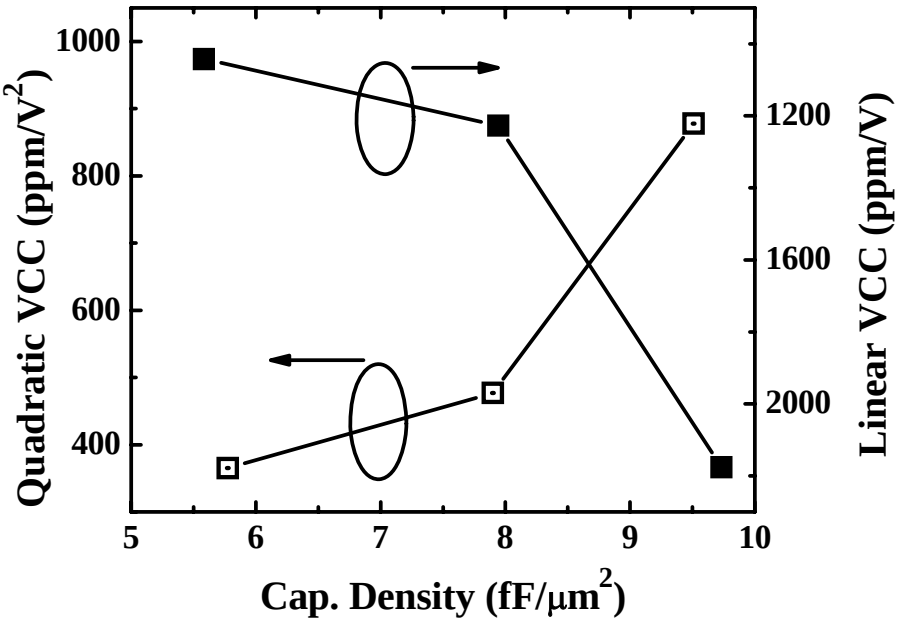
3.3. Properties of Sm_2O_3 High-κ Dielectric for the Applications of MIM Capacitors

3.3.1. Electrical Characteristics of Sm_2O_3 MIM Capacitors

Fig. 3.1 (a) shows the normalized capacitance ($\Delta C/C_0$) versus DC voltage of Sm_2O_3 MIM capacitors with the capacitance density of 9.5, 7.9, and 5.8 $fF/\mu m^2$, respectively. The capacitance is measured by sweeping the voltage from -4 to +4 V with a 0.1 V step at the frequency of 100 kHz. Note that these samples have not been performed any post deposition treatments except PDA. The quadratic VCC (α) and linear VCC (β) are extracted from the experimental *C-V* curves by using the equation of $C(V) = C_0(\alpha V^2+\beta V+1)$, which we have mentioned in Chapter 2. It is observed that both the quadratic VCC (α) and the linear VCC (β) decrease with decreasing the capacitance density. A quadratic VCC of lower than 500 ppm/V^2 with a high capacitance density of near 8 $fF/\mu m^2$ are demonstrated for MIM capacitors with a single Sm_2O_3 layer.



(a)



(b)

Figure 3.1. (a) Normalized capacitance ($\Delta C/C_0$) measured at 100 kHz for MIM capacitors with a single Sm_2O_3 dielectric layer with the capacitance density varied. By fitting a second-order polynomial equation to the experimental curves, the quadratic VCC (α) and the linear VCC (β) are obtained. **(b)** Summary of both quadratic VCC and linear VCC versus capacitance density.

The asymmetric experimental *C-V* curves are believed to be due to the different interfacial status at the interface of dielectric/bottom electrode and dielectric/top electrode, which have experienced different process, i.e., dielectric deposition at bottom electrode not at top electrode. This also causes large linear VCC (β). The relationship of the capacitance density versus both quadratic VCC and linear VCC of Sm_2O_3 MIM capacitors is summarized in Fig. 3.1 (b).

The obtained quadratic VCCs of Sm_2O_3 MIM capacitors are comparable or less than those reported high-κ dielectric MIM capacitors [3.22-3.30]. Fig. 3.2 compares the values of quadratic VCC of MIM capacitors with a Sm_2O_3 dielectric layer obtained in this work with other reports for binary high-κ dielectric MIM capacitors measured at 100 kHz.

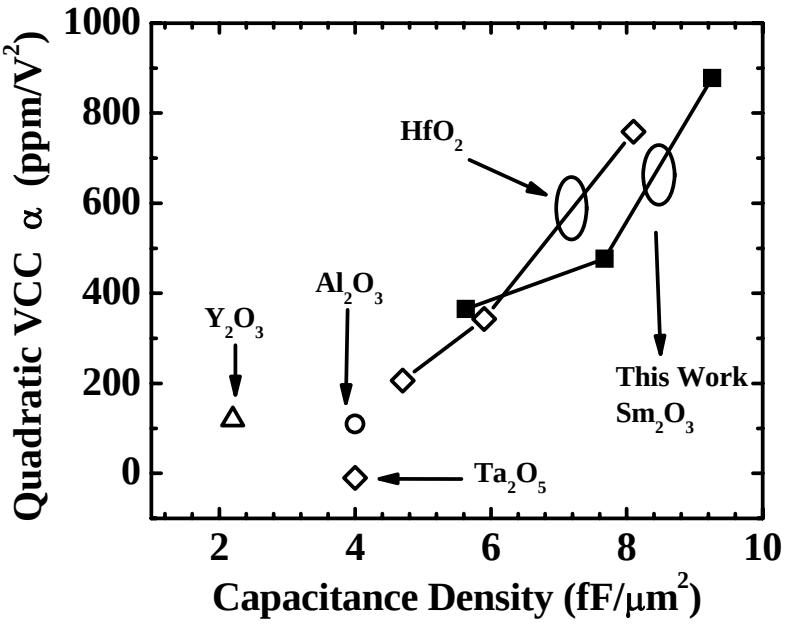
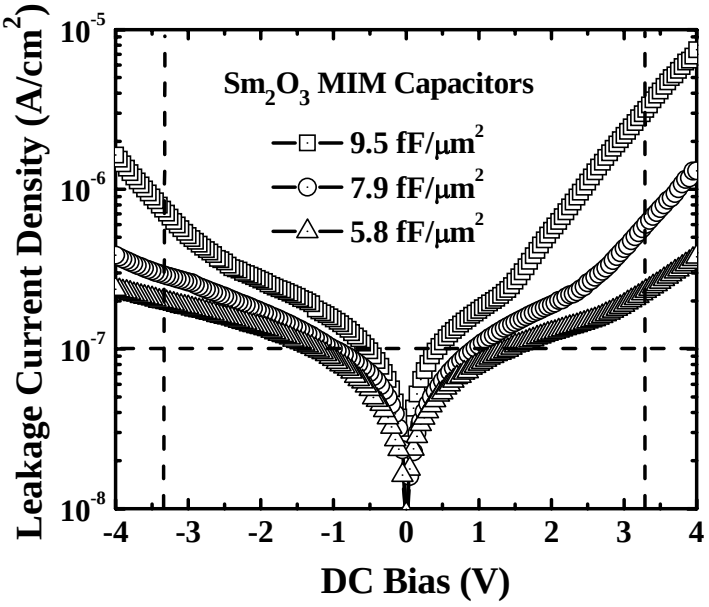


Figure 3.2. The values of quadratic VCC extracted from MIM capacitors with a single Sm_2O_3 dielectric layer in this work are compared with data published in the literature.

For a given capacitance density, MIM capacitors with a Sm_2O_3 dielectric are found to have smaller positive quadratic VCC than those of most of the other high-κ dielectrics. When compared with the extensively studied HfO_2, Sm_2O_3 shows a smaller quadratic VCC at the same capacitance density in the region where the capacitance density is larger than 6.5 fF/μm^2. This makes Sm_2O_3 a potential dielectric candidate for MIM capacitors in precision analog circuit applications.

Fig. 3.3 shows the dependence of leakage current density J on direct current bias voltages for Sm_2O_3 MIM capacitors with various capacitance densities at room temperature. The leakage current densities at both +3.3 V and –3.3 V are under 10^{-6} A/cm^2. The *J-V* curves are similar with the normalized *C-V* curves shown in Fig. 3.1 (a). As we have discussed before, the different interface quality causes asymmetric *C-V* curves and this also causes asymmetric *J-V* curves. The different interface quality of Sm_2O_3/TaN electrodes is believed due to different deposition process, i.e., bottom electrode experiences dielectric deposition and an additional PDA process.

The *J-V* curves show that at high bias region, the leakage current increases sensitively with increasing in the applied voltage. Fig. 3.4 plot ln(J/E) versus $E^{1/2}$ at different capacitance density for high positive bias. It is shown that at each capacitance density, the ln(J/E) value increases linearly with the increasing of $E^{1/2}$. The conduction process at high bias is likely dominated by Poole-Frenkel (P-F) emission. It is believed that the P-F emission is due to field-enhanced thermal excitation of trapped electrons.



(a)

Figure 3.3. *J-V* characteristics at room temperature of MIM capacitors with a single Sm_2O_3 dielectric layer at the capacitance of 9.5, 7.9, and 5.7 fF/μm^2, respectively. The *J-V* curve becomes asymmetric at higher DC bias, indicating that the MIM capacitor may have physically asymmetric, i.e. different electrode-dielectric interface quality for the bottom and top interfaces.

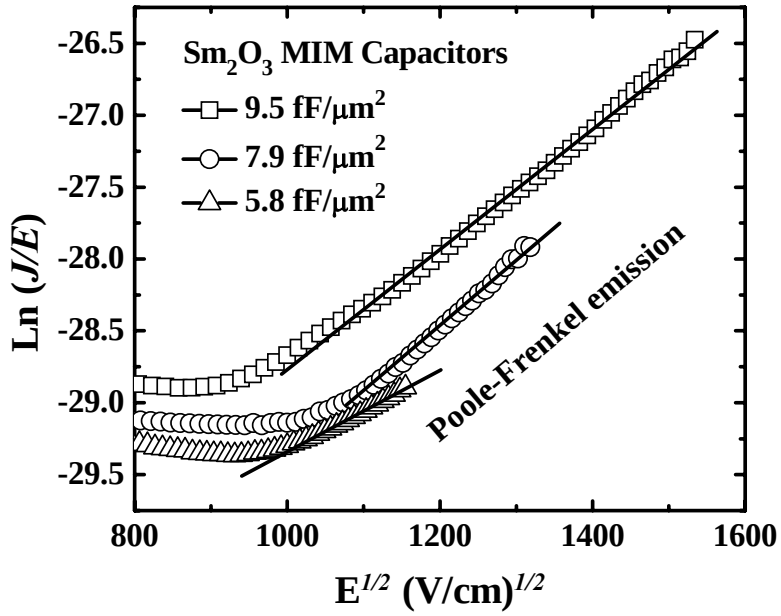


Figure 3.4. Plot of ln(*J*/*E*) versus $E^{1/2}$ of the capacitor with different capacitance density, together with the linear fitting for the leakage current at positive bias.

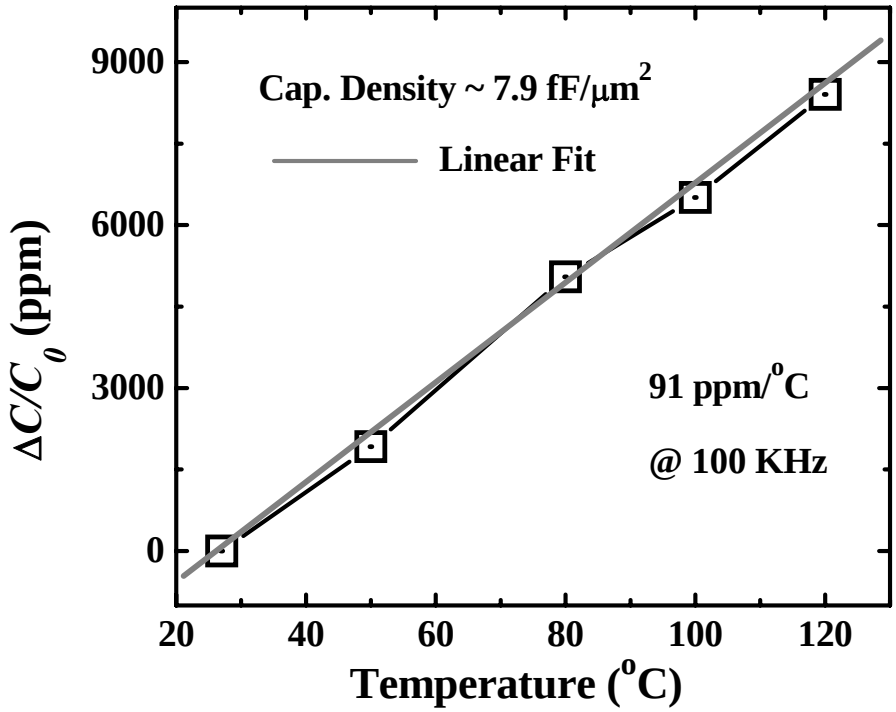


Figure 3.5. TCC characteristic of Sm_2O_3 MIM capacitors measured from 27 to 120 °C. The capacitance variation increases linearly with the increasing of the temperature.

Furthermore, the characteristic of temperature coefficient of capacitance (TCC) with a capacitance density of around 7.9 fF/μm^2 was studied with the temperature change from 27 to 120 °C, as shown in Fig. 3.5. Low TCC characteristic of 91 ppm/^{o}C are comparable or even smaller to those reported [3.25, 3.31].

3.3.2. Physical Characterization of Sm_2O_3 MIM Capacitors

Fig. 3.6 shows a cross-sectional transmission electron microscopy (TEM) image of the MIM capacitor with a single Sm_2O_3 dielectric without any post deposition treatment except PDA. This capacitor has a capacitance density of around 15.5 fF/μm^2 with a physical thickness of around 12.5 nm.

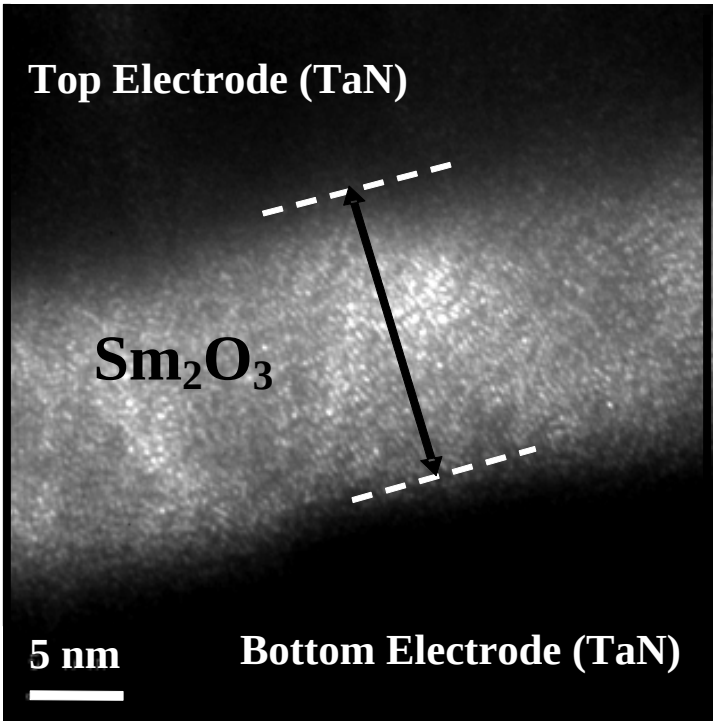


Figure 3.6. The TEM image of the MIM capacitor with a single Sm_2O_3 layer. It should be noted that the Sm_2O_3 layer is poly-crystalline.

The calculated dielectric permittivity of Sm_2O_3 is around 22, which is within the range of 10 to 30.5 as reported in the literature [3.11, 3.20 and 3.21]. The κ value of Sm_2O_3 is also comparable to that of the widely researched HfO_2 dielectric (22~25) [3.32].

The crystalline structure of the Sm_2O_3 dielectric has been investigated by using XRD, as shown in Fig. 3.7. A thick Sm_2O_3 (80 nm) film was deposited directly on a 200 nm thick TaN layer with as-deposited or annealing at the temperatures of 400 ^oC for 60 s before XRD analysis. The Sm_2O_3 film for analysis is thicker than the typical used Sm_2O_3 film for MIM capacitors.

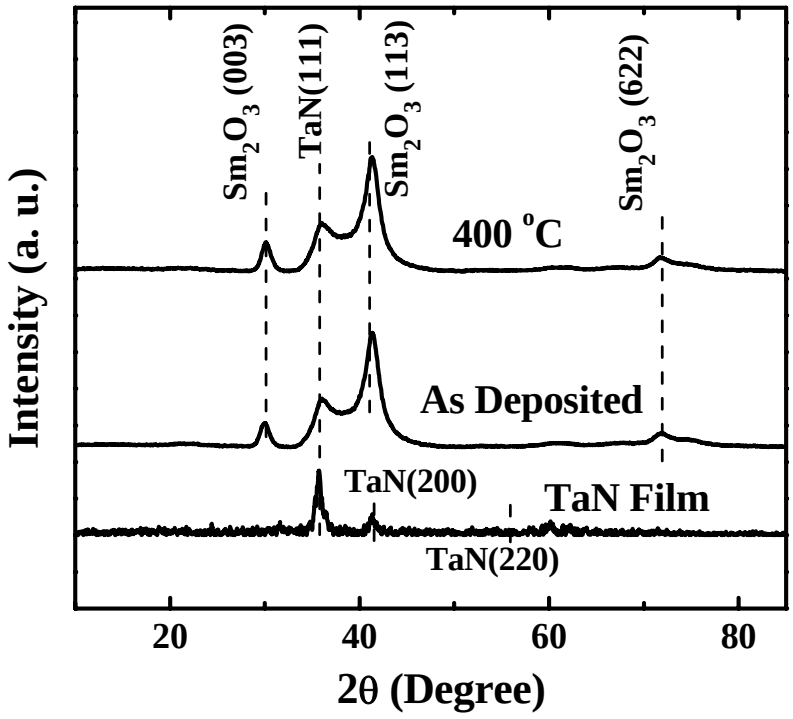


Figure 3.7. X-Ray Diffraction (XRD) spectra of as-deposited Sm_2O_3 dielectric on TaN, as well as Sm_2O_3/TaN after being annealed at 400 ºC for 60 s. XRD spectrum of an exposed TaN surface is also obtained. As-deposited Sm_2O_3 on TaN is shown to be likely poly-crystalline.

In the XRD result, it is shown that a bare TaN surface (prior to Sm_2O_3 deposition) is likely poly-crystalline. The as-deposited Sm_2O_3 film formed on the TaN surface is also poly-crystalline. In comparison with as-deposited film, the Sm_2O_3 peaks after being annealed at 400 ºC did not differ much, indicating the phase and composition were not affected by the temperature. The result of poly-crystalline of Sm_2O_3 film after being annealed at 400 ºC is consistent with the observation from the TEM image with a thinner film.

3.4. Performance Improvement of Sm_2O_3 MIM Capacitors by Using Plasma Treatment after Dielectric Formation

Due to the thermal budget limitation for the back-end CMOS process, the post deposition annealing (PDA) temperature should be kept below 400 ^oC. This is a limitation for forming high quality high-κ dielectrics with low leakage current density. In order to improve the quality of high-κ dielectrics, other post-deposition treatments with low thermal budget such as plasma treatment have been investigated [3.23, 3.33]. Results indicate that plasma treatment is promising for further investigation. It has also been demonstrated that Sm_2O_3 dielectric is an excellent candidate for high-κ MIM capacitors in precision analog circuit application. In this work, the effects of Plasma Treatments (PT) with O_2 and/or N_2 on the performance of MIM capacitors with Sm_2O_3 dielectric are investigated. Plasma treatment directly on Sm_2O_3 dielectric in either O_2 or N_2 ambient can effectively reduce both the quadratic and linear VCC. Furthermore, the leakage current density and hysteresis can be significantly improved.

3.4.1. Voltage Linearity

Fig. 3.8 shows the quadratic VCC versus capacitance density of Sm_2O_3 MIM capacitors with or without 2 minutes of PT after Sm_2O_3 dielectric formation. Effective quadratic VCC reduction can be obtained by using PT in either O_2 or N_2 ambient, especially PT in N_2 ambient.

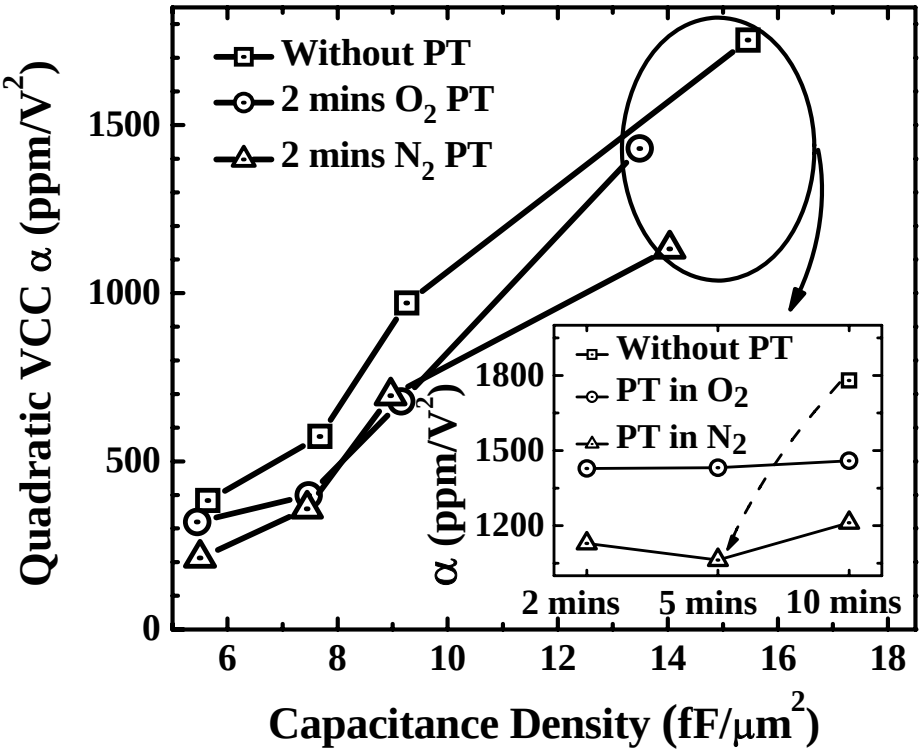
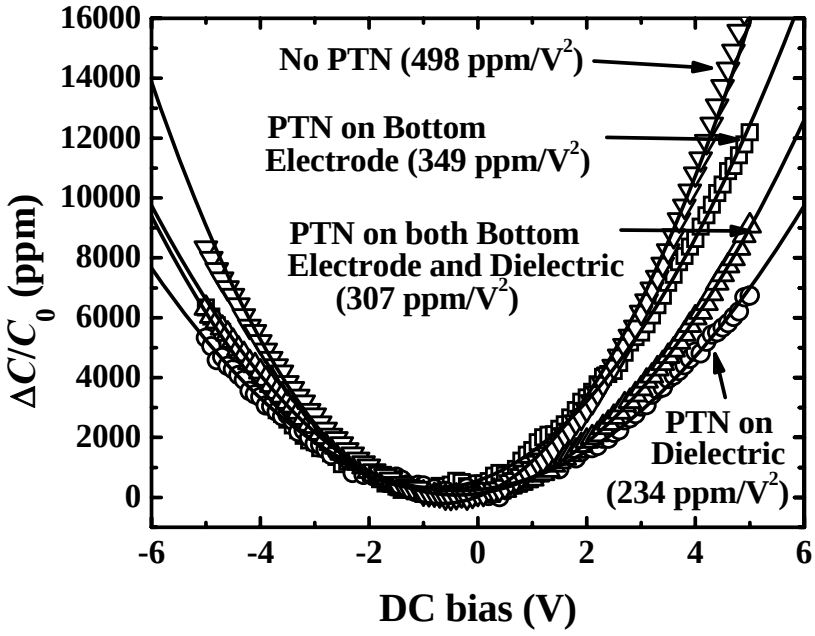
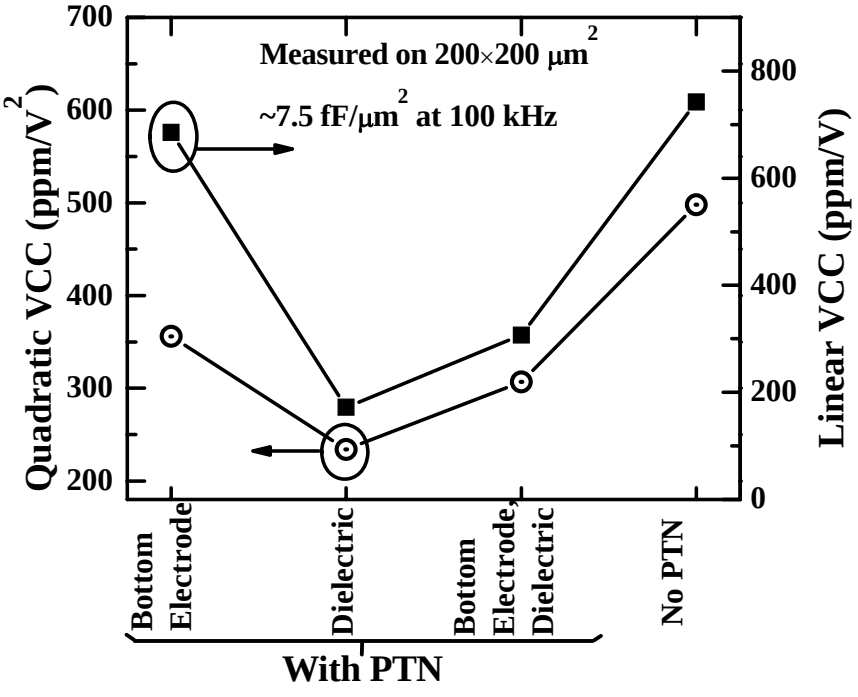


Figure 3.8. Quadratic VCC versus capacitance density of Sm_2O_3 MIM capacitors without or with plasma treatment (PT). The inset shows the influence of PT duration on the quadratic VCC.

For capacitors with high capacitance densities, the effect of post-dielectric plasma treatment on the quadratic VCC is compared in the inset of Fig. 3. 8. By adjusting the duration of the post-dielectric Plasma Treatment in N_2 ambient (PTN), an optimal quadratic VCC was obtained after a 5 minute treatment. PTN led to a minor change in the capacitance density (from 15.5 fF/μm^2 to 14.5 fF/μm^2), but significantly improved the quadratic VCC from ~1800 ppm/V^2 to 1100 ppm/V^2. PTN after Sm_2O_3 deposition is effective for reducing quadratic VCC. On the other hand, PT in O_2 ambient after Sm_2O_3 deposition did no change the quadratic VCC appreciably.



(a)



(b)

Figure 3.9. **(a)** Normalized *C-V* curves of Sm_2O_3 MIM capacitors with Plasma Treatment in N_2 (PTN) after bottom electrode formation, PTN after dielectric formation, PTN in both steps, and with no PTN. **(b)** Summary of the quadratic and linear VCC of Sm_2O_3 MIM capacitors after various PTN conditions. The best VCC values are obtained by using PTN after dielectric formation.

Recent report showed that plasma treatment (PT) performed on lower electrode in O_2 ambient, i.e. before dielectric formation, can improve both the quadratic VCC and leakage current density [3.33]. To investigate further, we examine the effects of PTN on Sm_2O_3 MIM capacitors by inserting the PTN process at various stages of the device fabrication: after bottom electrode formation, after dielectric formation, or after each of the two steps.

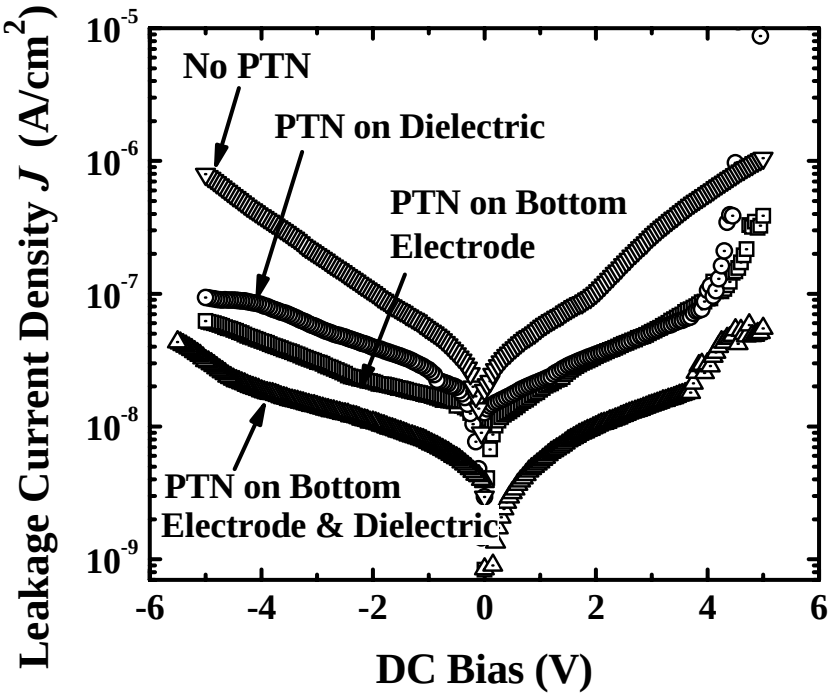
The normalized *C-V* curves of Sm_2O_3 MIM capacitors with PTN inserted at various stages of the process flow are shown in Fig. 3.9 (a). Note that there is a split in which PTN is performed only after dielectric formation, and a thick Sm_2O_3 layer (giving a capacitance density of ~7.5 fF/μm^2) was used for all the capacitors so that the effect on the bottom electrode is minimized. The VCC values were extracted from *C-V* data by a fit performed over a wide voltage range (-5 to +5 V). The capacitance densities of Sm_2O_3 MIM capacitors obtained are 7.85, 7.7, 7.35, and 7.76 fF/μm^2 for the capacitors with Plasma Treatment in N_2 (PTN) after bottom electrode formation, PTN after dielectric formation, and PTN after both bottom electrode formation and after dielectric formation, and with no PTN, respectively.

Fig. 3.9 (b) summarizes both the quadratic and linear VCC obtained. The quadratic VCC for a control capacitor without any PT is 498 ppm/V^2, and this is reduced to 234 ppm/V^2 with PTN performed after Sm_2O_3 deposition, and to 307 ppm/V^2 with PTN performed after bottom electrode as well as after Sm_2O_3 deposition. The linear VCC for a control capacitor without any plasma treatment is 742.3 ppm/V.

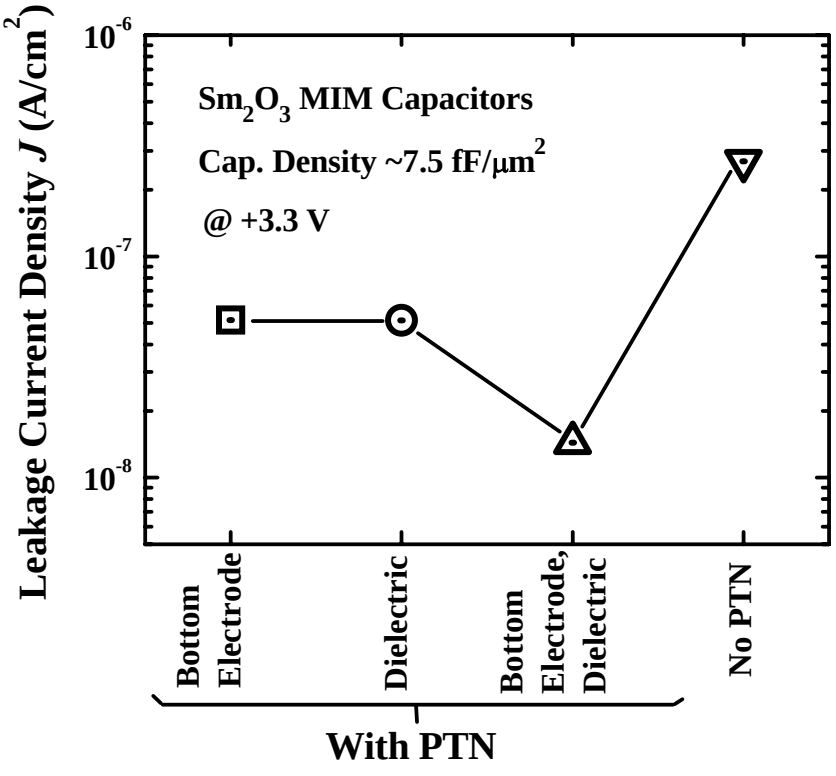
This is reduced to 172 ppm/V with PTN performed after Sm_2O_3 deposition, and to 308 ppm/V with PTN performed after bottom electrode as well as Sm_2O_3 deposition. This demonstrates that PTN after Sm_2O_3 formation can effectively improve the quality of Sm_2O_3 MIM capacitors and thus the VCC. The quadratic VCC of capacitors after PTN at both steps is slightly larger than that of capacitors with PTN after dielectric formation. This is possibly due to interfacial layer formation at the dielectric/bottom electrode interface after 2-step PTN, which also caused the capacitance density to be reduced to 7.35 $fF/\mu m^2$.

3.4.2. Leakage Current Density

The typical *J-V* curves of Sm_2O_3 MIM capacitors with different PTN conditions are shown in Fig. 3.10 (a). PTN generally reduces the leakage current density. The leakage current density values measured at +3.3 V for the various device splits are compared in Fig. 3.10 (b). As compared to capacitors without PTN, the leakage current density at +3.3 V is significantly reduced from 3.44×10^{-7} A/cm^2 to 6.05×10^{-8}, 5.79×10^{-8}, and 1.60×10^{-8} A/cm^2 for the capacitors with PTN after bottom electrode formation, after dielectric formation, and in both steps, respectively. Over one order leakage current density reduction is obtained by using PTN on both bottom electrode and dielectric



(a)



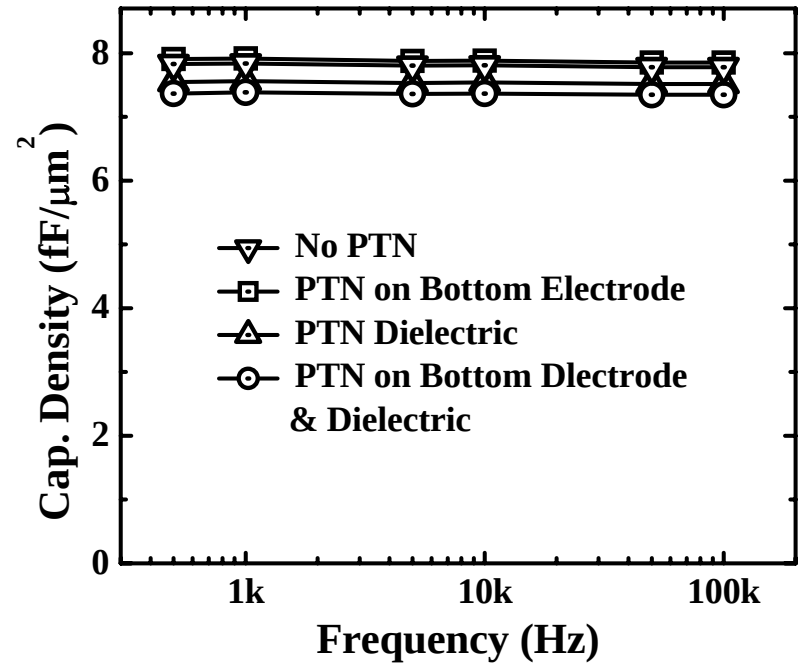
(b)

Figure 3.10. **(a)** The *J-V* curves of Sm_2O_3 MIM capacitors after different PTN. **(b)** Summary of the leakage current density *J* obtained at +3.3 V for MIM capacitors with Sm_2O_3 dielectric.

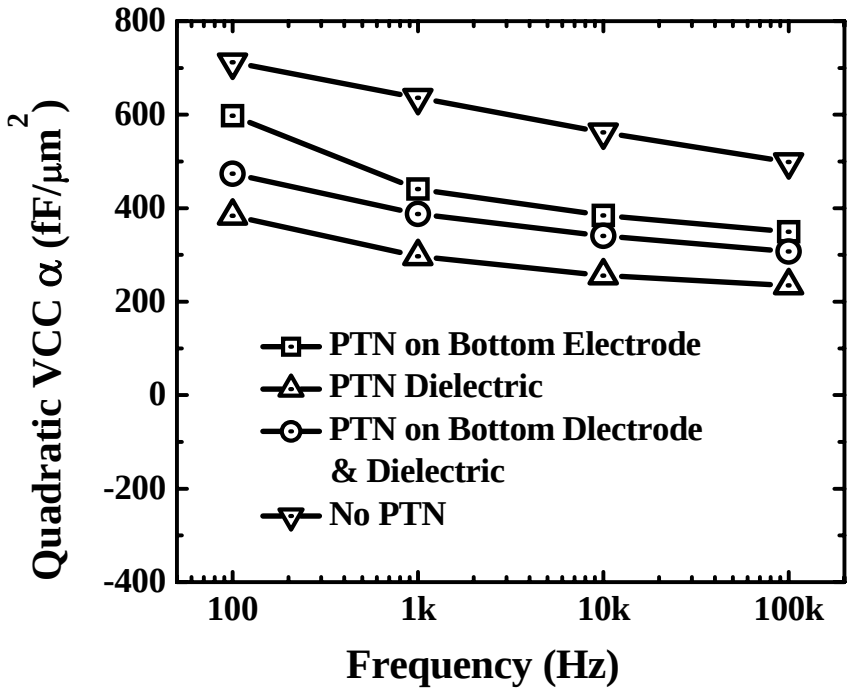
The result of leakage current density reduction demonstrates the significant performance improvement of Sm2O3 MIM capacitors by introducing PTN on Sm_2O_3 MIM capacitors. PTN should be performed after bottom electrode formation and after dielectric formation to achieve the largest leakage reduction of about one order of magnitude.

3.4.3. Frequency Dependence

The frequency dependence of the capacitance density and the quadratic VCC (α) are shown in Fig. 3.11 (a) & (b), respectively. A small amount of capacitance reduction for Sm_2O_3 MIM capacitors with or without PTN is found over the entire frequency range from 500 Hz to 100 kHz. The quadratic VCC decreases linearly with a logarithmic increase in frequency [Fig. 3.11 (b)]. At each frequency, the quadratic VCC of Sm_2O_3 MIM capacitors with PTN after dielectric deposition are smaller than that of with only PTN on bottom electrode and with no PTN. The slope of the quadratic VCC (α) versus log(*f*) is approximately constant for MIM capacitors with various PTN conditions. The frequency dependence of α can be explained as the change of relaxation time with different carrier mobility in the dielectric [3.34].



(a)



(b)

Figure 3.11. Frequency dispersion of the capacitance density **(a)** and the quadratic VCC **(b)** of Sm_2O_3 MIM capacitors with or without PTN. The capacitance density shows small dependence on the frequency while the quadratic VCC has a linear relationship with the frequency.

3.4.4. Hysteresis and TCC

The capacitance hysteresis of Sm_2O_3 MIM capacitors with different PTN conditions is summarized in Fig 3.12. C_{M+} and C_{M-} are the minimum values of the capacitance obtained by sweeping the Direct Current (DC) voltage from +4 to -4 V and from -4 to +4 V, respectively. It can be observed that low capacitance variation (<40 ppm) is obtained by performing PTN after dielectric formation.

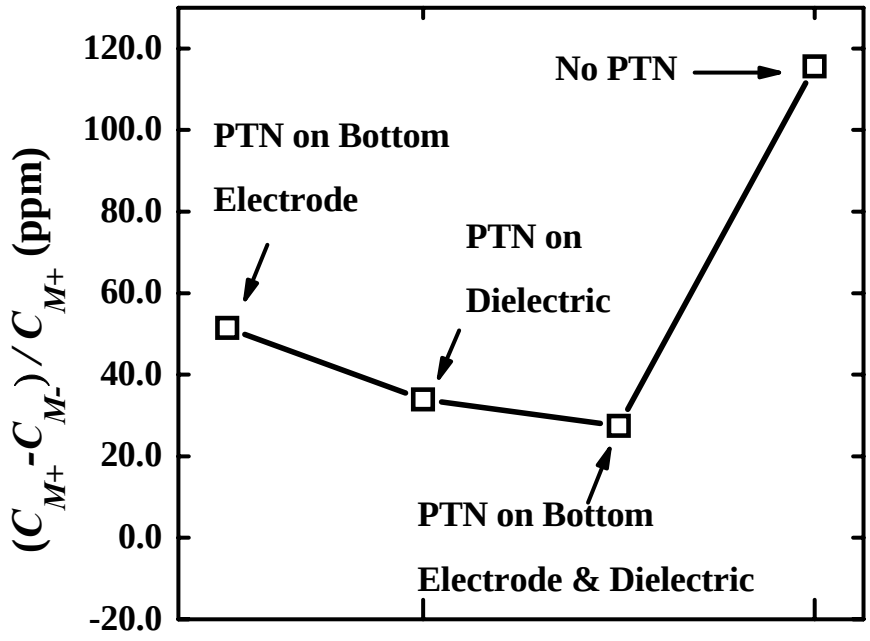


Figure 3.12. Hysteresis of the capacitance density of Sm_2O_3 MIM capacitors after various PTN conditions.

Fig. 3.13 depicts the temperature dependence of Sm_2O_3 MIM capacitors with different PTN. The extracted Temperature Coefficient of Capacitance (TCC) is 115, 90, and 74 ppm/^oC for the capacitors with PTN after bottom electrode formation, after dielectric formation, and in both steps, respectively. The TCC values of the

capacitors with PTN after dielectric formation is comparable or less than that with no PTN (91 ppm//^{o}C), indicating that PTN after dielectric formation does not deteriorate the TCC value.

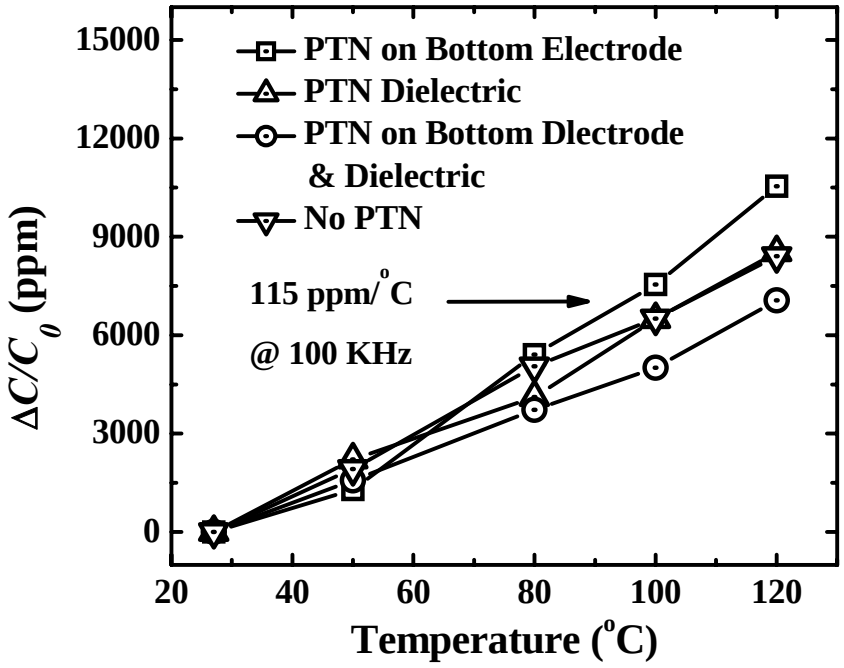
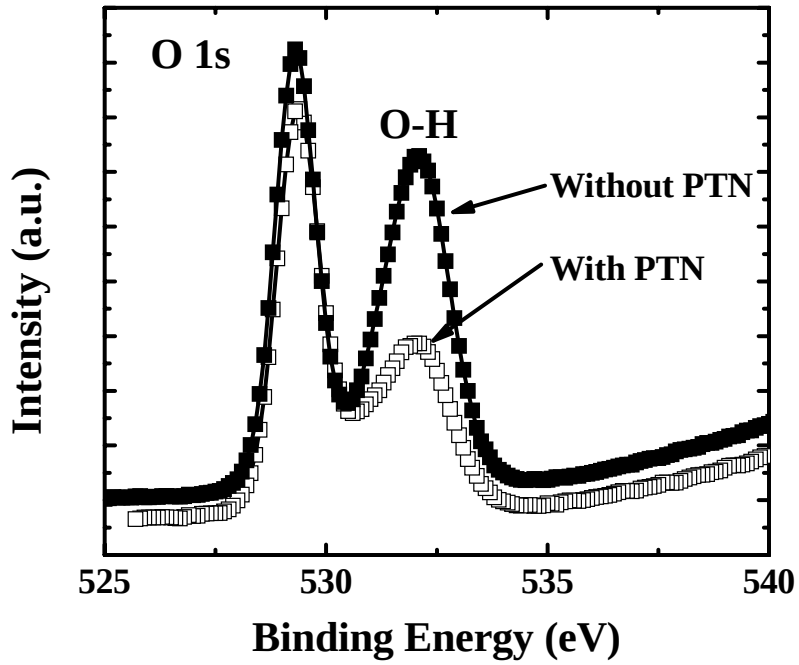
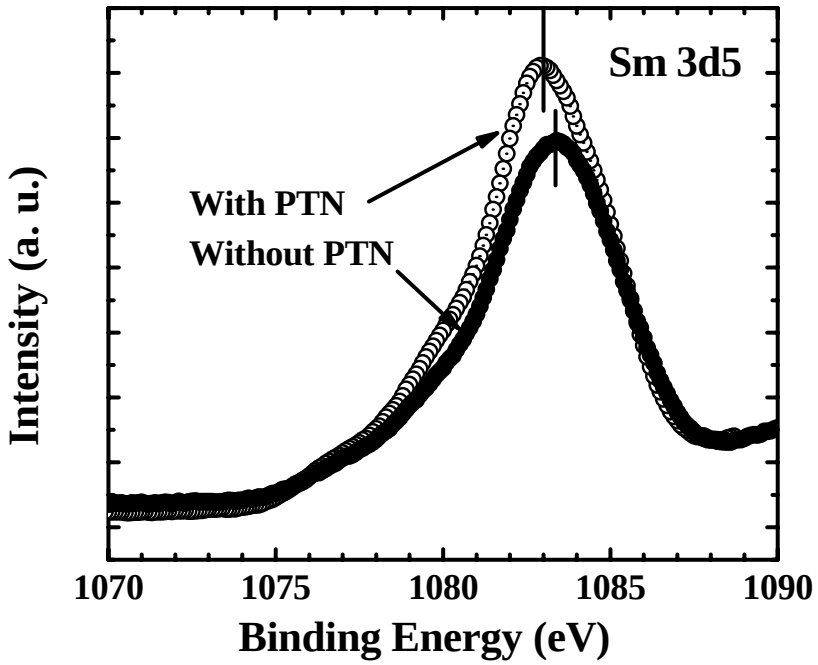


Figure 3.13. Temperature dependence of Sm_2O_3 MIM capacitors after various PTN conditions.

We performed further material analysis using cross-sectional TEM and XPS on the Sm_2O_3 MIM capacitors, as shown in Fig. 3.5 and Fig. 3.14 (a) & (b). The TEM photograph of Sm_2O_3 MIM without PTN [Fig. 3.5] shows that there is no obvious interfacial layer at Sm_2O_3/bottom electrode interface, which means that the large quadratic VCC is probably not contributed by interfacial layer effects [3.35]. The effective reduction of the VCC, leakage current densities, and hysteresis of capacitance is believed to be due to the improvement of dielectric quality by using plasma treatment after dielectric formation.



(a)



(b)

Figure 3.14. Bonding energy of O 1s **(a)** and Sm 3d5 **(b)** of Sm_2O_3 dielectric with or without PTN after Sm_2O_3 dielectric formation.

Fig. 14 (a) and (b) shows the O 1s and Sm 3d5 spectra of Sm_2O_3 after exposure to atmospheric air with or without PTN after dielectric formation. The hydroxide formation, revealed by the peak of O 1s near 534 eV, is effectively suppressed by the introduction of PTN on the dielectric. Moreover, the bonding energy of Sm 3d5 slightly shifts lower after PTN on the dielectric. This is probably due to the lower bonding energy of N 1s (around 400 eV) as compared to that of O 1s (around 533 eV). The larger improvement in VCC of Sm_2O_3 MIM capacitors using PT in N_2 ambient on dielectrics rather than using PT in O_2 ambient is probably due to the smaller electronegativity of N (3.04) as compared to that of O (3.44). The smaller difference in electronegativity between Sm (1.17) and N indicates a less polar bond between them which might have an influence on the VCC [3.36, 3.37].

3.5. Summary

MIM capacitors using Sm_2O_3 dielectric were first found to have lower quadratic VCC as compared to other high-κ dielectrics with the same capacitance density. The electrical and physical characteristics of MIM capacitors with a single Sm_2O_3 dielectric were systematically investigated in this chapter. The excellent electrical characteristics of Sm_2O_3 MIM capacitors indicate that it is a promising candidate for the application of high-κ dielectric MIM capacitors. Moreover, we have successfully demonstrated the performance improvement of plasma treatment on Sm_2O_3 MIM capacitors, including quadratic VCC, linear VCC, hysteresis and leakage

current density. By performing PTN after Sm_2O_3 dielectric formation, the effective quadratic VCC and linear VCC can be reduced from 498 ppm/V^2 to 234 ppm/V^2 and from 742.3 ppm/V to 172 ppm/V, respectively. In addition, more than one order of magnitude reduction in leakage current density at +3.3 V can be obtained by applying PTN at both steps. These results indicate that PTN after dielectric formation is an effective way to improve the performance of high-κ dielectric MIM capacitors for high precision applications.

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CHAPTER 4

Sm_2O_3/SiO_2 LAMINATED DIELECTRICS FOR MIM CAPACITORS IN PRECISION ANALOG CIRCUIT APPLICATIONS

4.1. Introduction

Sm_2O_3 dielectric has already demonstrated excellent electrical characteristics, including small quadratic VCC and low leakage current density, as shown in Chapter 2. Plasma treatment on Sm_2O_3 dielectrics can obtain significant reduction of quadratic VCC, linear VCC, hysteresis and leakage current density. However, the obtained capacitance density and corresponding quadratic VCC still cannot satisfy the specified requirements of MIM capacitors for precision analog circuit applications according to ITRS 2007 [4.1]. The requirement for the capacitance density should be 7 $fF/\mu m^2$ by 2013, while the quadratic VCC (α) should be kept below 100 ppm/V^2.

Recently, MIM capacitors with HfO_2/SiO_2 stack have been studied [4.2]. The compensation or 'cancelling effect' in the stack of HfO_2 (having positive α) and the thin SiO_2 (having negative α) can achieve reduction of the effective α value. According to the theory of "cancelling effect", the ratio of effective oxide thickness

(EOT) of each dielectric layer to the whole EOT of stacked dielectrics plays a significant role in determining the effective quadratic VCC value. For a dual layer dielectric stack, i.e. laminate structure, the relationship between the α value and the thicknesses (or EOT) of the dielectrics is given by equation 4.1:

$$\alpha = \delta_1^3 \alpha_1 + \delta_2^3 \alpha_2 ,$$

$$\delta_i = \frac{EOT_i}{EOT_{total}}, i = 1,2 \qquad (4.1)$$

EOT_i is the EOT of the i^{th} layer, and EOT_{total} is the EOT of the entire dielectric stack. The quadratic VCC (α) values of both dielectrics at each thickness are derived from the experimental data of MIM capacitors with a single high-κ layer or a single SiO_2 layer.

With "canceling effect", HfO_2/SiO_2 MIM capacitors with capacitance density of around 6 $fF/\mu m^2$ and α value of 14 ppm/V^2 have been successfully demonstrated. [4.2]. However, further improvement is limited by the large positive α value of HfO_2 dielectrics. There is a need for further material exploration. MIM capacitors with Sm_2O_3 dielectric, especially those with PTN, are found to show smaller positive quadratic VCC as compared to those with HfO_2 layer, as shown in Fig. 4.1. The smaller quadratic VCC of MIM capacitors with Sm_2O_3 dielectric as compared to that with HfO_2 dielectric implies that Sm_2O_3 is more suitable than HfO_2 for exploitation of the "cancelling effect" using SiO_2. In this section, Sm_2O_3 dielectric is laminated with SiO_2 dielectric of Physical Vapor Deposition (PVD) by sputtering or Plasma

Enhanced Chemical Vapor Deposition (PECVD) to modulate the effective quadratic VCC. Various thickness combinations of Sm_2O_3 and SiO_2 have been studied and analyzed.

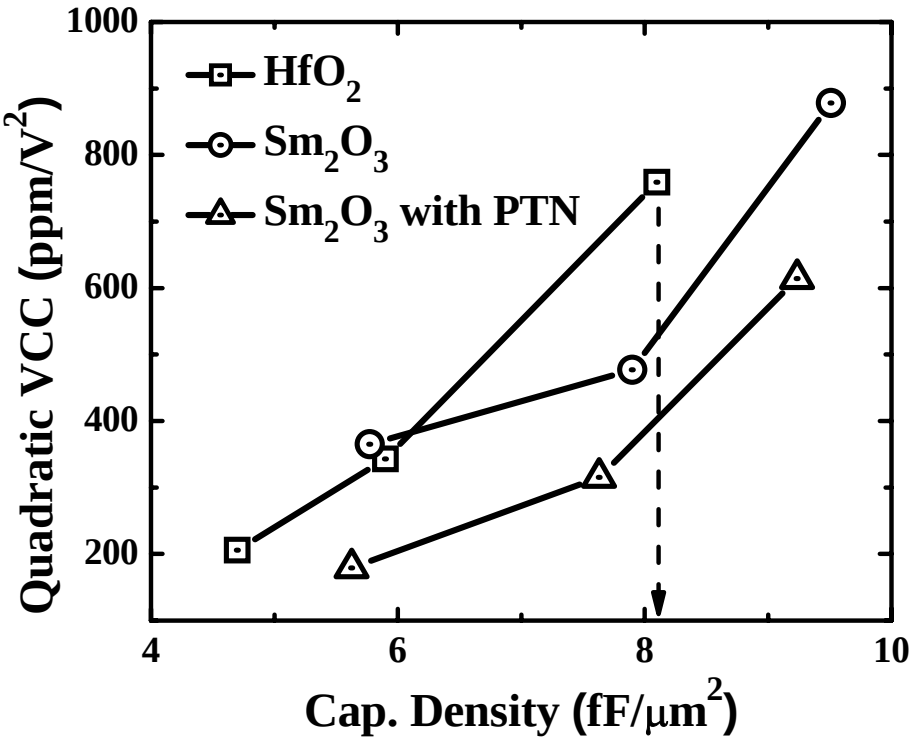


Fig. 4.1. Quadratic VCC (α value) versus capacitance density of HfO_2 and Sm_2O_3 (with or without PTN). Sm_2O_3 MIM with PTN on Sm_2O_3 dielectrics can obtain much lower quadratic VCC.

4.2. Sm_2O_3/PVD SiO_2 Laminated Dielectrics MIM Capacitors

4.2.1. Experiments

Both PVD SiO_2 and PVD SiO_2/Sm_2O_3 MIM capacitors are fabricated on Si wafers covered with a 400 nm thick thermal SiO_2. A 200 nm thick TaN layer was

deposited by sputtering in Ar/N_2 ambient as bottom electrode. For PVD SiO_2 MIM capacitors, the SiO_2 layer was deposited at room temperature by sputtering at RF power in Ar ambient. After PVD SiO_2 deposition, an optional plasma treatment in N_2 ambient (PTN) was performed to investigate the effect of PTN on PVD SiO_2 MIM capacitors. For PVD SiO_2/Sm_2O_3 MIM capacitors, Sm_2O_3 layer was first deposited directly on bottom TaN electrode by sputtering in Ar ambient and followed by PVD SiO_2 deposition. After Sm_2O_3 and SiO_2 dielectric deposition, a PTN was performed on the samples and followed by PDA at 400 ^oC for 60 ~ 120 s within N_2 ambient. After that, a 100 nm thick TaN was deposited and patterned to form the top electrode. Fig. 4.2 shows the schematic of PVD SiO_2/Sm_2O_3 MIM capacitors. The thicknesses of SiO_2 and Sm_2O_3 layers are adjusted by controlling the sputtering time.

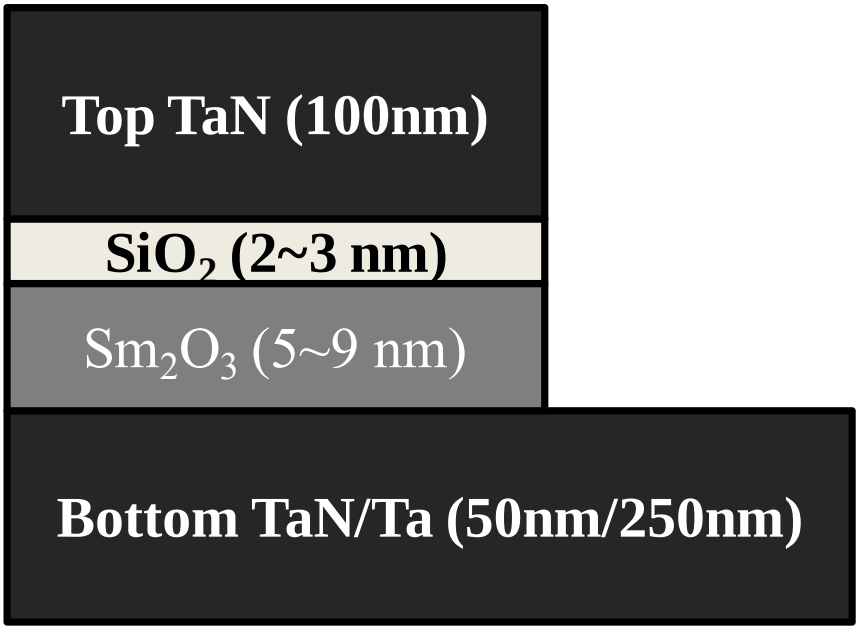
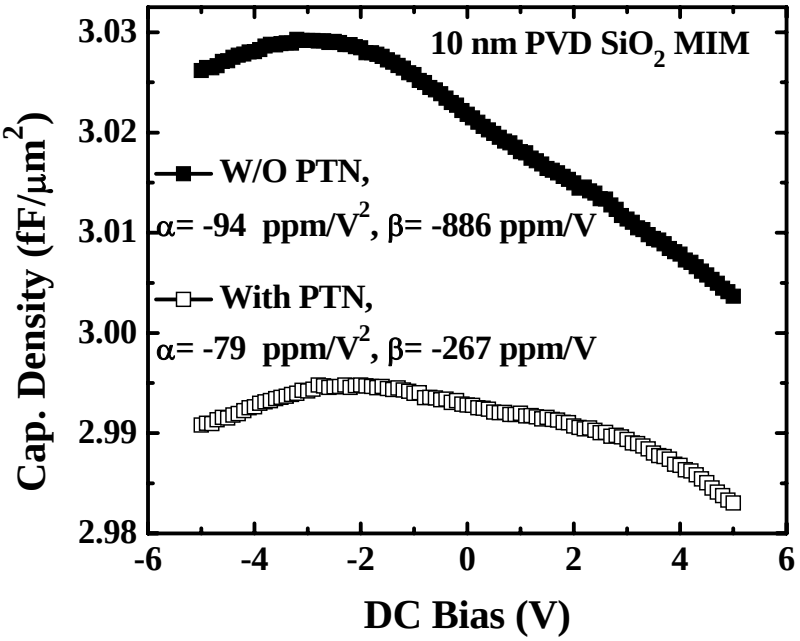


Figure 4.2. Schematic of PVD SiO_2/Sm_2O_3 MIM capacitors. Note that Sm_2O_3 layer was deposited prior to SiO_2 layer.

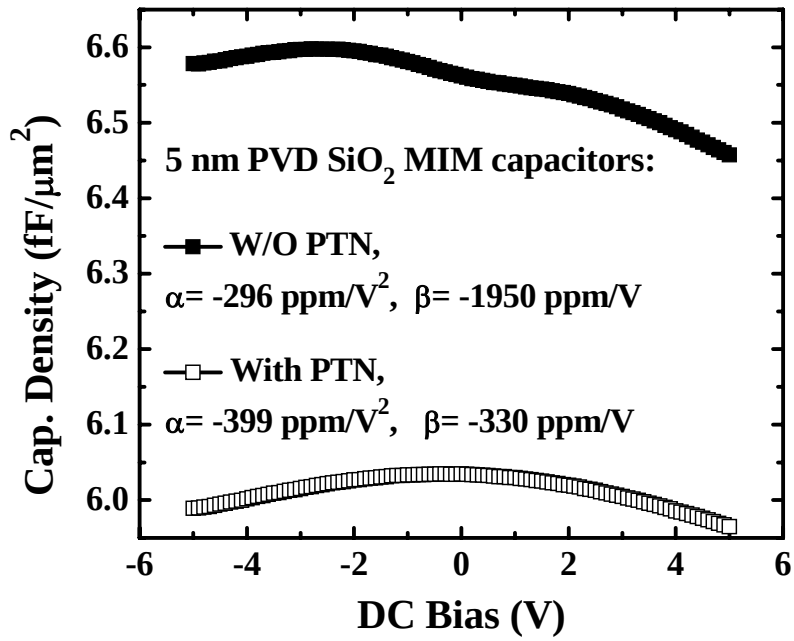
4.2.2. Electrical Characteristics

Fig 4.3 shows the typical *C-V* curves of PVD SiO_2 MIM capacitors with 10 nm and 5 nm thick SiO_2 measured at 100 kHz. The quadratic VCC (α) and linear VCC (β) were extracted by fitting the *C-V* curves with voltage ranging of +5 to –5 V. The quadratic VCC of PVD SiO_2 MIM capacitors with 10 nm and 5 nm thick SiO_2 shows negative value, which implies that it can be utilized to cancel the positive quadratic VCC of high-κ dielectric MIM capacitors. Form 10 nm SiO_2 MIM capacitors, the extracted effective quadratic VCC are -79 and -94 ppm/V^2 for the capacitors with and with no PTN on SiO_2, respectively.

For 5 nm thick SiO_2 MIM capacitors, the effective quadratic VCC can be reduced significantly from -296 to -399 ppm/V^2 by performing PTN on SiO_2 [Fig. 4.3(b)]. It is noticed that after PTN on SiO_2, the quadratic VCC of the capacitors with SiO_2 thicknesses at 5 nm and 10 nm shows different direction change. This is probably due to the asymmetric *C-V* curves of capacitors with no PTN. After PTN on SiO_2, the *C-V* curves of both of 5 nm and 10 nm SiO_2 MIM capacitors become symmetric, especially for capacitors with 5 nm thick SiO_2. The linear VCC (β) can be significantly reduced after plasma treatment.



(a)

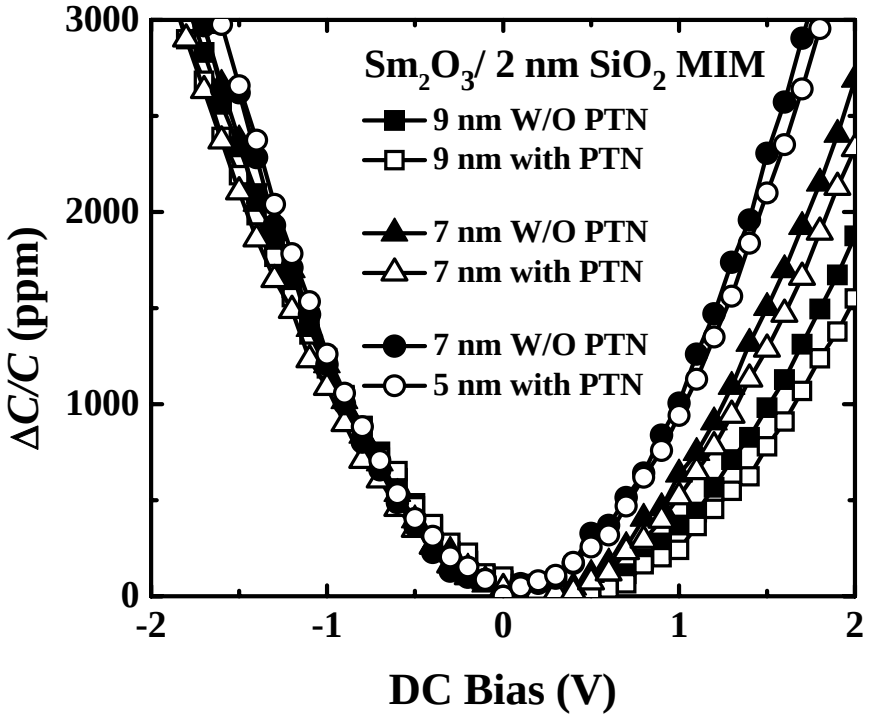


(b)

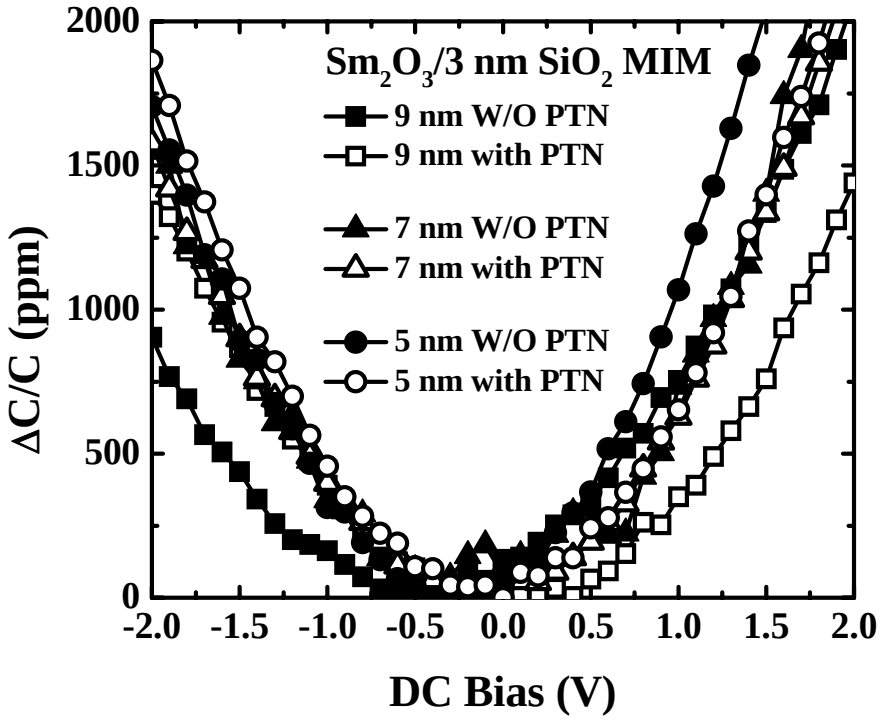
Figure 4.3. Typical C-V curves of PVD SiO_2 MIM capacitors with **(a)** 10 nm and **(b)** 5 nm sputtered SiO_2. PTN shows improvement on both quadratic VCC and linear VCC.

Fig. 4.4 shows the normalized *C-V* curves of Sm_2O_3/PVD SiO_2 MIM capacitors with SiO_2 thicknesses at 2 nm (a) and 3 nm (b), respectively. The thicknesses of Sm_2O_3 layer are at 5, 7 and 9 nm by controlling the deposition time. The quadratic VCC of Sm_2O_3/PVD SiO_2 MIM capacitors are modulated with the corresponding change of Sm_2O_3 (or SiO_2) thickness.

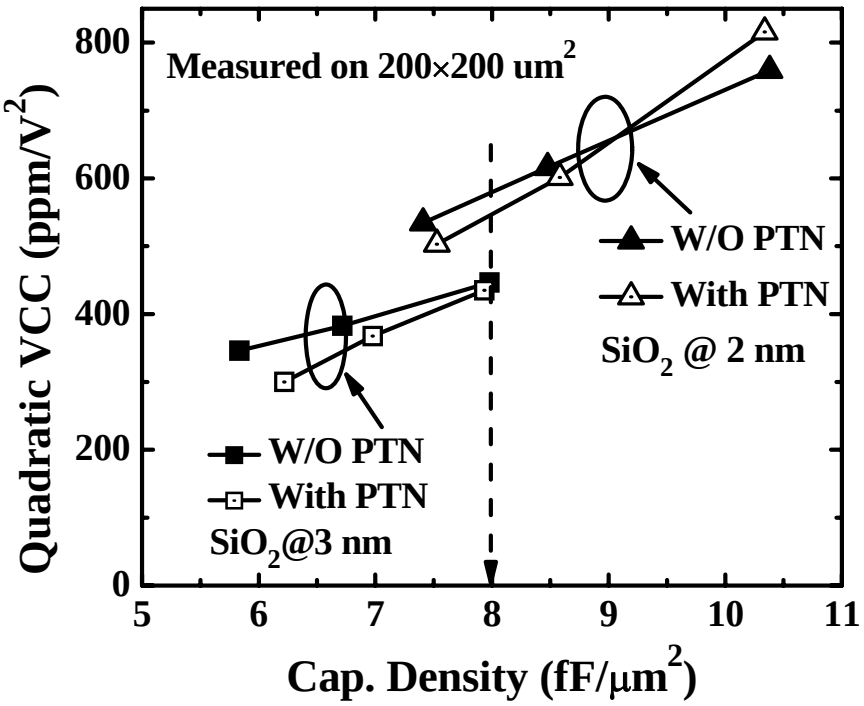
We have summarized the capacitance density versus quadratic VCC extracted from the normalized *C-V* curves, as shown in Fig. 4.4 (c). By decreasing the capacitance density, the quadratic VCC decrease slightly. The Sm_2O_3/PVD SiO_2 MIM capacitors with SiO_2 thickness at 3 nm can obtain quadratic VCC of 432 ppm/V^2 at 8 fF/μm^2 as compared to that of 574 ppm/V^2 of MIM capacitors with 2 nm thick SiO_2 at same capacitance density. The modulation of the effective quadratic VCC is the reason that the ratio of SiO_2 thickness to the whole dielectric stack increases when increasing the SiO_2 thickness. Therefore, the negative quadratic VCC of SiO_2 tunes the effective quadratic VCC of whole stack toward lower value. This result demonstrates the effective modulation of quadratic VCC by inserting a SiO_2 layer. Moreover, after PTN on dielectrics, the quadratic VCC can be tuned to more negative direction for the capacitors with 3 nm thick SiO_2. This is due to the reduction of the effective quadratic VCC of both Sm_2O_3 and PVD SiO_2 after PTN on dielectrics.


Sm2O3/ 2 nm SiO2 MIM
9 nm W/O PTN
9 nm with PTN
7 nm W/O PTN
7 nm with PTN
7 nm W/O PTN
5 nm with PTN
ΔC/C (ppm)
DC Bias (V)
3000
2000
1000
0
-2
-1
0
1
2

(a)


Sm2O3/3 nm SiO2 MIM
9 nm W/O PTN
9 nm with PTN
7 nm W/O PTN
7 nm with PTN
5 nm W/O PTN
5 nm with PTN
ΔC/C (ppm)
DC Bias (V)
2000
1500
1000
500
0
-2.0
-1.5
-1.0
-0.5
0.0
0.5
1.0
1.5
2.0

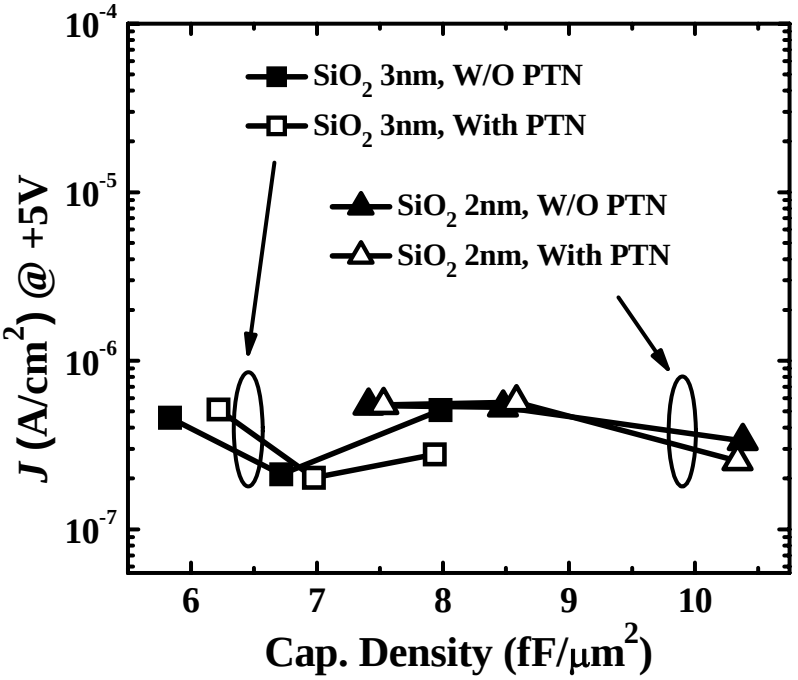
(b)



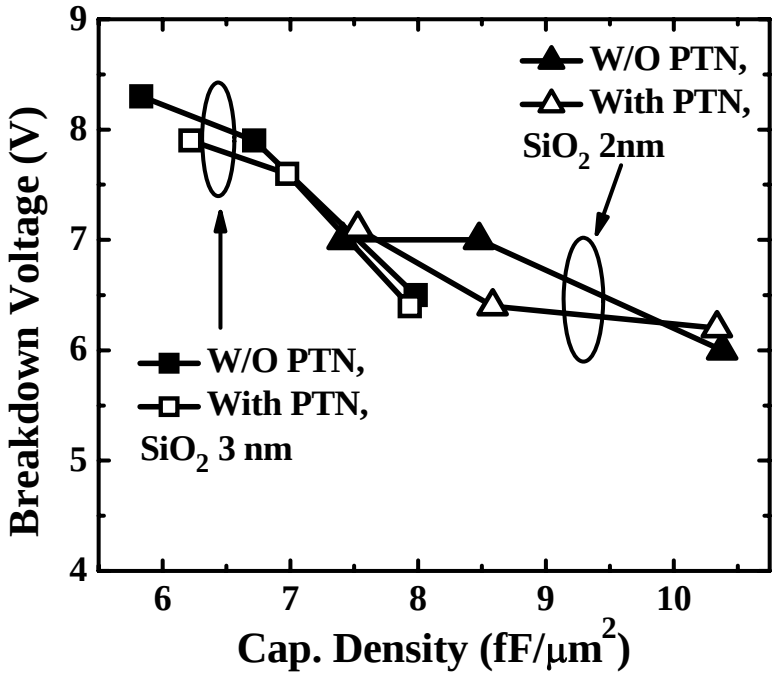
(c)

Figure 4.4. Normalized *C-V* curves of Sm_2O_3/PVD SiO_2 MIM capacitors with SiO_2 thicknesses at **(a)** 2 nm and **(b)** 3 nm. **(c)** Summary of capacitance density versus quadratic VCC. By increasing the thickness of SiO_2 from 2 nm to 3 nm, the effective quadratic VCC is modulated from 545 to 432 ppm/V^2 at the capacitance density at 8 fF/μm^2.

Fig 4.5 (a) and (b) summarize the electrical characteristics of the leakage current density (@+5 V) and breakdown voltage versus capacitance density, respectively. The leakage current densities are around 2×10^{-7} A/cm^2 at +3.3 V, which is comparable to that of MIM capacitors with a single Sm_2O_3 layer shown in Chapter 2. Plasma treatment shows no much improvement in the leakage current density and breakdown voltage. At each capacitance density, the leakage current density shows no much change. This might be the trap assistant tunneling in PVD SiO_2 as the quality of sputter SiO_2 is not good.



(a)



(b)

Figure 4.5. Summary of the electrical characteristics of **(a)** leakage current densities at +5 V and **(b)** breakdown voltage versus capacitance density.

In this work, MIM capacitors with Sm_2O_3/PVD SiO_2 laminated structure have been fabricated and characterized. The modulation of quadratic VCC of MIM capacitors by inserting a SiO_2 layer has been demonstrated. However, the modulation effect of PVD SiO_2 to the whole dielectric stack is not enough to satisfy the requirement of ITRS. Moreover, the quality of PVD SiO_2 is poor, which limits the performance of Sm_2O_3/PVD SiO_2 MIM capacitors. Therefore, a high quality SiO_2 with a larger quadratic VCC is needed.

4.3. Sm_2O_3/PECVD SiO_2 Laminated Dielectrics MIM Capacitors

The quality of SiO_2 layer is essential to determine the performance of MIM capacitors with Sm_2O_3/SiO_2 laminated dielectrics. Therefore, in this section, plasma enhanced chemical vapor deposition (PECVD) SiO_2 stacked with sputtered Sm_2O_3 high-κ dielectric for MIM capacitors was fabricated and characterized. The deposition temperature of PECVD SiO_2 is around 350^{o}C, which is under the temperature limitation of BEoL. As a result, at given quadratic VCC, Sm_2O_3/PECVD SiO_2 MIM capacitors with superior capacitance densities are successful demonstrated, in comparison to the HfO_2/SiO_2 stack.

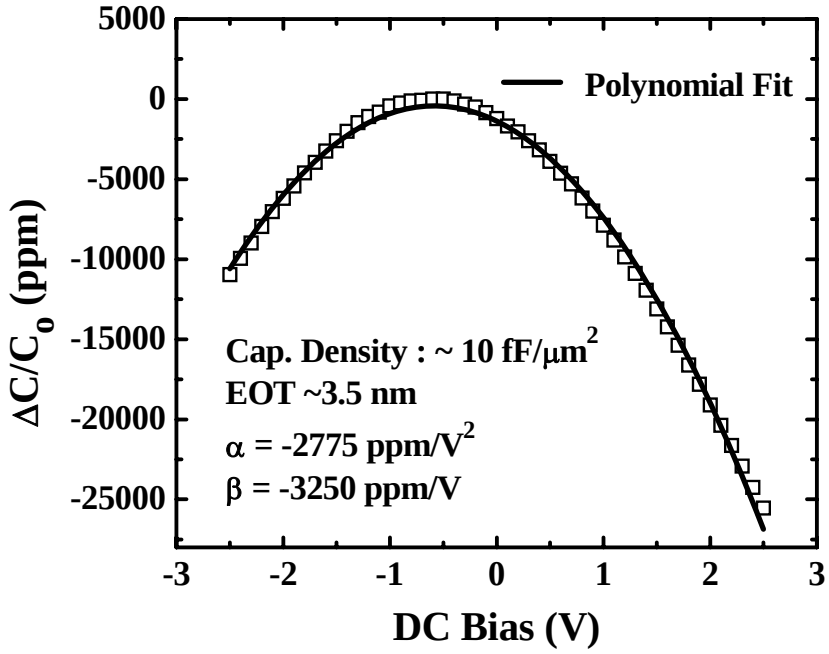
4.3.1. Experiments

PECVD SiO_2 was deposited directly on 200 nm thick TaN electrodes. For Sm_2O_3/PECVD SiO_2 MIM capacitors, PECVD SiO_2 was deposited with thickness

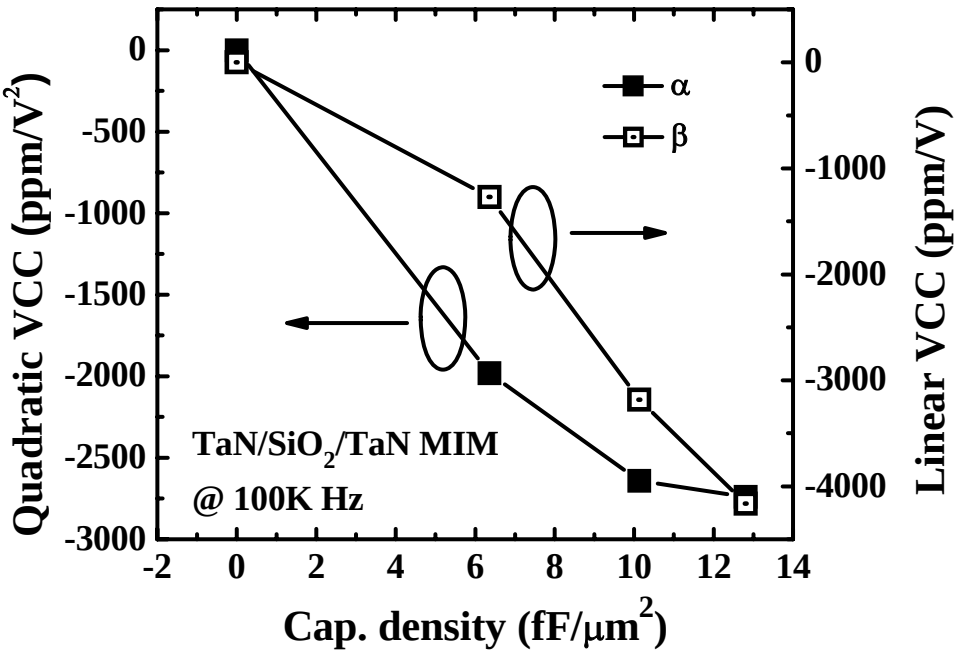
varying from 3 to 7 nm, and Sm_2O_3 was then deposited on PECVD SiO_2 with thicknesses varying form 6 nm to 10 nm. After dielectric deposition, a plasma treatment in N_2 ambient (PTN) was carried out. Post deposition annealing (PDA) at 400 °C for 120 s within N_2 ambient was then performed for all samples. Following that, a 100 nm thick top TaN layer was sputtered and patterned using lithography.

4.3.2. Electrical Characteristics of PECVD SiO_2 MIM Capacitors

Fig 4.6 (a) shows the *C-V* curves of PECVD SiO_2 MIM capacitors with a capacitance density of around 10 fF/μm^2. A large negative value of the quadratic VCC (~ - 2775 ppm/V^2) is obtained. This is much larger than those of PVD SiO_2 MIM capacitors. The large negative quadratic indicates that it is promising to be used to cancel the large quadratic VCC of Sm_2O_3 dielectrics. Moreover, PECVD SiO_2 MIM capacitors shows better asymmetric *C-V* curve as compared to PVD SiO_2 MIM capacitors and can be fitted well by using polynomial fitting. Fig 4.6 (b) summarizes both quadratic VCC (α) and linear VCC (β) versus capacitance density of the MIM capacitors with a single PECVD SiO_2 layer. The PECVD SiO_2 MIM capacitors with a capacitance density of 0 fF/μm^2 is assumed to have α and β with zero values. Both of the quadratic VCC and linear VCC are changed to more negative value by increasing the capacitance density.



(a)



(b)

Figure 4.6. (a) *C-V* curve of MIM capacitors with a single PECVD SiO_2 layer. **(b)** Summary of both quadratic and linear VCC versus the capacitance density.

According to the equation 4.1, the effective quadratic VCC (α) of the whole dielectric stack is determined by the thickness ratio of each dielectric to the whole stack and their corresponding α values. A simulation is first carried out to determine the relationship between the effective quadratic VCC (α) and the stacked dielectric thicknesses. Fig. 4.7 shows the relation between the quadratic VCC of a Sm_2O_3/SiO_2 stack and the thicknesses of each layer.

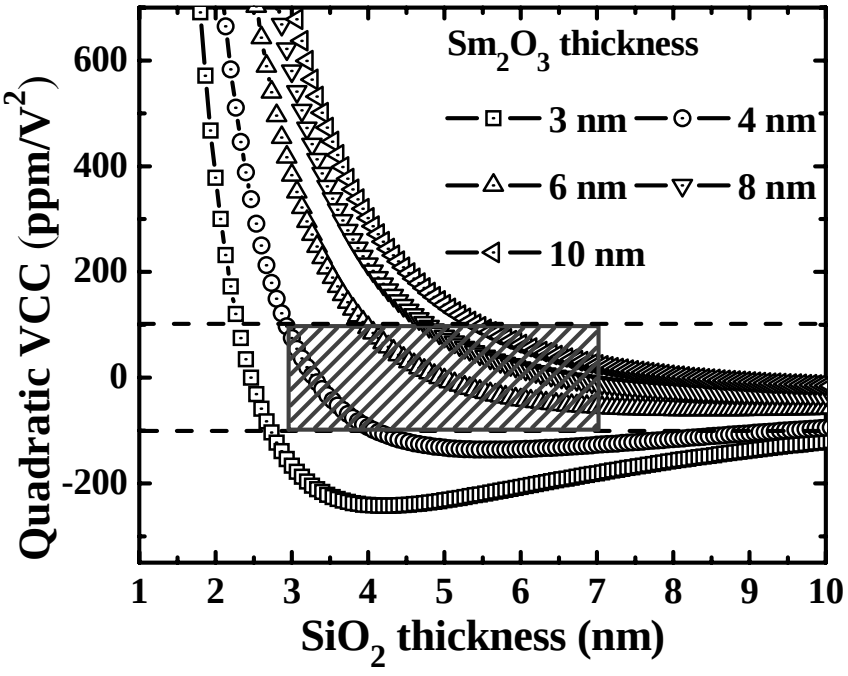


Figure 4.7. Simulated α versus SiO_2 thickness plot for different Sm_2O_3 thicknesses from 3 to 10 nm. The value of α should preferably be within the range of ±100 ppm/V^2, as indicated by the horizontal dashed lines. The quadratic VCC is sensitive to the thicknesses of both SiO_2 and Sm_2O_3.

The quadratic VCC (α) values of both dielectrics at each thickness are derived from data that obtained from MIM capacitors with a single Sm_2O_3 layer or a single PECVD SiO_2 layer. The region between the two dashed lines is where quadratic

VCC is within ±100 ppm/V^2. For a thinner Sm_2O_3 thickness, a more precise thickness control for SiO_2 is needed. It is shown that by controlling the Sm_2O_3 thickness in the range of 6 to 10 nm, the quadratic VCC can be modulated in the range of ±100 ppm/V^2. The simulation, nevertheless, ignores the process and structural differences between MIM capacitors with single layer and laminate dielectrics.

4.3.3. Electrical Characteristics of Sm_2O_3/PECVD SiO_2 MIM Capacitors

The split table for MIM capacitors with Sm_2O_3/PECVD SiO_2 laminated dielectrics is shown in Table 4.1. The thickness of PECVD SiO_2 and Sm_2O_3 is controlled by adjusting the deposition time.

Table 4.1. Split table for MIM capacitors with Sm_2O_3/SiO_2 laminate dielectric.

SiO_2 Thickness	Sm_2O_3 Thickness (PTN on Sm_2O_3)			
	6.5 nm	**7.5 nm**	**8.5 nm**	**10 nm**
3.0 nm	√	√	√	√
3.5 nm	√	√	√	√
4.0 nm	√	√	√	√
5.0 nm	√	√	√	√
7.0 nm	√	√	√	√

Fig. 4.8 depicts the TEM image of a Sm_2O_3/SiO_2 stack with their thicknesses at 7.5 nm/3.5 nm. The structure of TaN/Sm_2O_3/SiO_2/TaN MIM stack is successfully demonstrated.

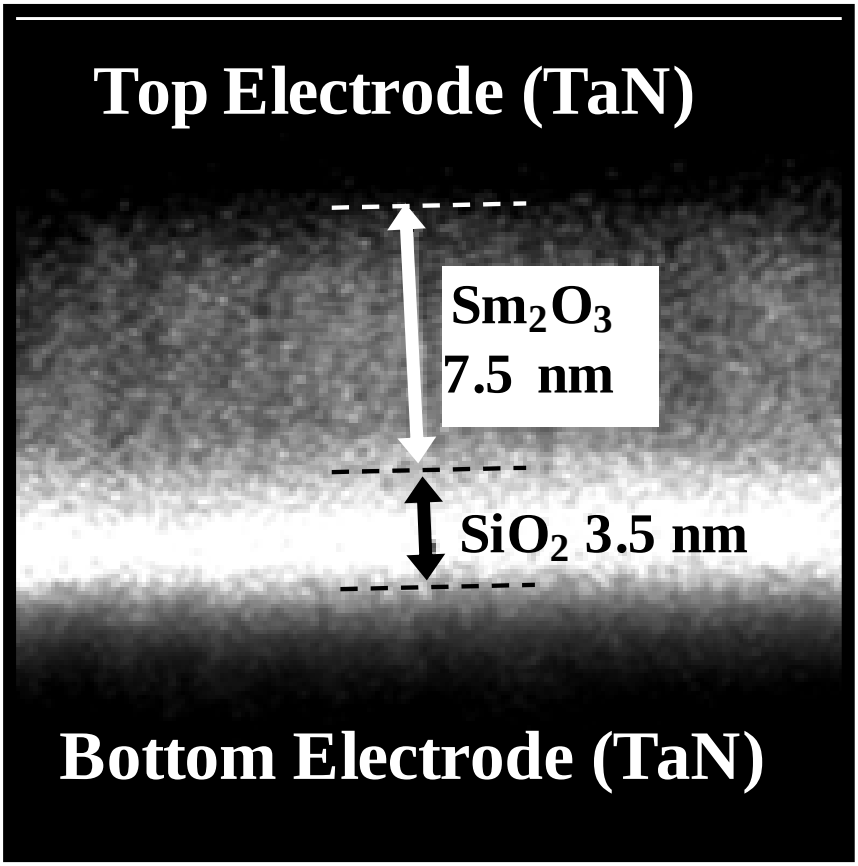


Figure 4.8. TEM image of Sm_2O_3/PECVD SiO_2 MIM capacitor.

Fig.4.9 shows the extracted effective oxide thickness (EOT) of Sm_2O_3/SiO_2 MIM capacitors versus the thickness of PECVD SiO_2. A linear relationship of the thickness of SiO_2 with EOT is observed, indicating that the physical thickness of deposited SiO_2 is well controlled.

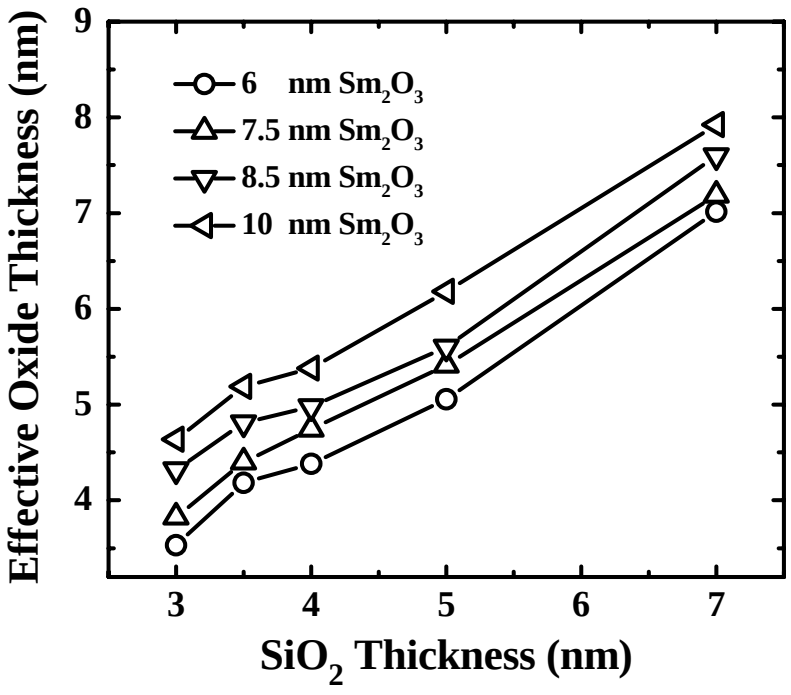


Figure 4.9. EOT versus SiO_2 thickness of Sm_2O_3/SiO_2 MIM capacitors with the Sm_2O_3 thickness at 6, 7.5, 8.5 and 10 nm, respectively.

Fig.4.10 shows the normalized *C-V* curves of Sm_2O_3/PECVD SiO_2 MIM capacitors with Sm_2O_3 thickness at 7.5 nm and SiO_2 thickness varying from 3 nm to 7 nm. The dark lines are *C-V* curves of Sm_2O_3 and SiO_2 MIM capacitors with comparable capacitance densities. Increasing the SiO_2 thickness can effectively modulate the effective quadratic VCC from positive to negative values. The quadratic VCC is effectively modulated with the introduction of SiO_2 under-layer. The experimental *C-V* curves with SiO_2 thickness varying from 3.5 nm to 5 nm are modulated in the region where their corresponding α values are within ±100 ppm/V^2. It can be observed that for larger SiO_2 thicknesses used, i.e., 5 nm and 7 nm thick SiO_2, the quadratic VCC actually turns negative. This is due to the large thickness ratio of SiO_2 to the whole dielectric stack.

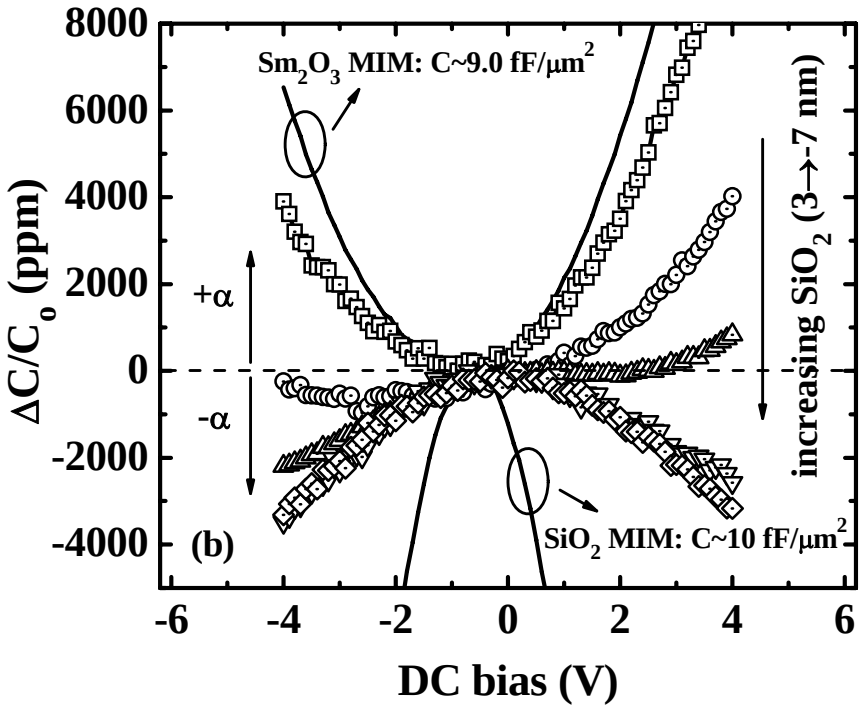
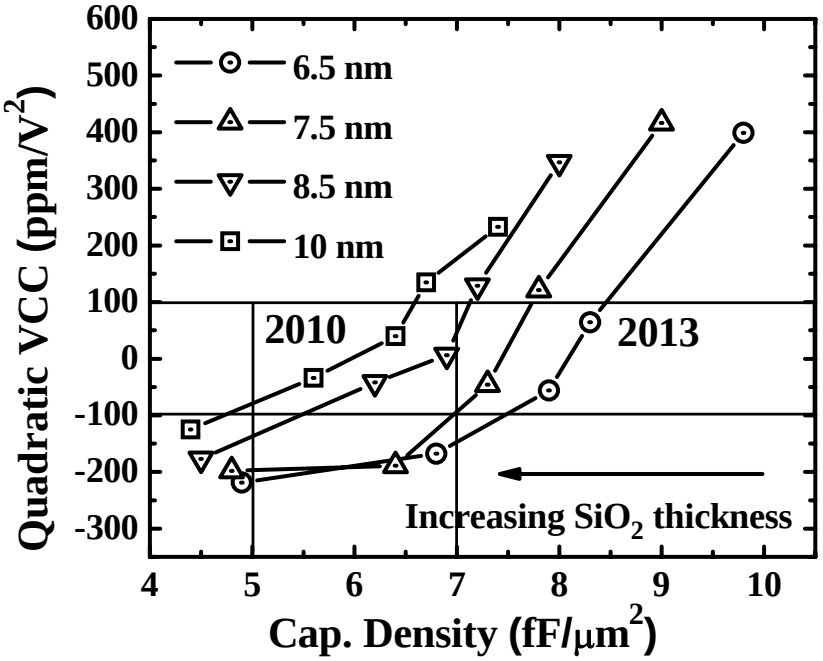
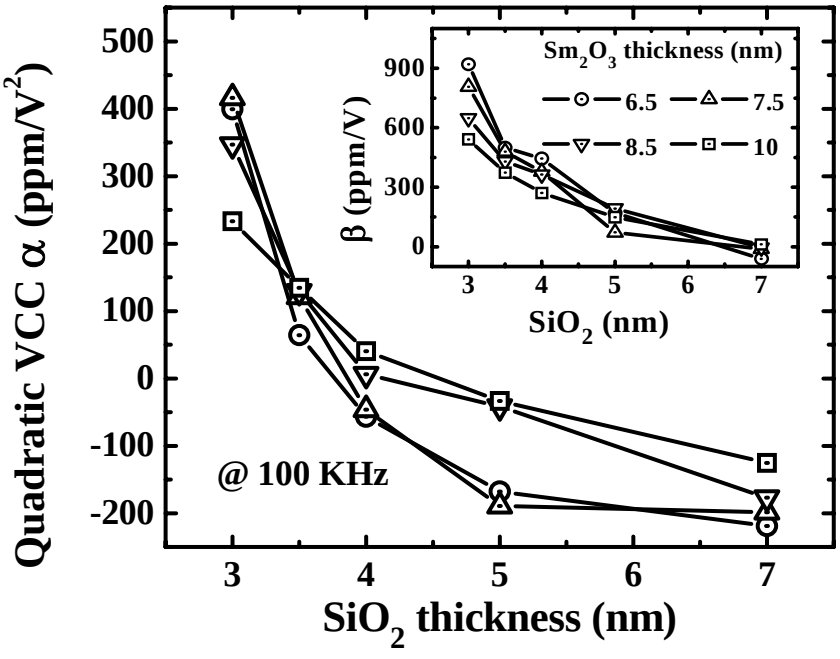


Figure 4.10. Normalized *C-V* curves of Sm_2O_3/SiO_2 MIM capacitors with SiO_2 thickness varying from 3, 3.5, 4, 5, to 7 nm, and Sm_2O_3 thicknesses being fixed at 7.5 nm. Sm_2O_3 and SiO_2 MIM with comparable capacitance densities are also included. The effective quadratic VCC (α value) is modulated from positive to negative values by increasing SiO_2 thickness.

Fig. 4.11(a) summarizes the obtained quadratic VCC (α) of Sm_2O_3/SiO_2 dielectric stacks versus varying SiO_2 thickness (from 3 nm to 7 nm) at different Sm_2O_3 thicknesses (6.5 nm, 7.5 nm, 8.5 and 10 nm). For each Sm_2O_3 thickness, the capacitance density of Sm_2O_3/SiO_2 MIM capacitors decreases with increasing SiO_2 thickness. Consequently, the quadratic VCC (α) of Sm_2O_3/SiO_2 MIM capacitors are effectively modulated from positive to negative values because of the increasing thickness (or EOT) ratio of SiO_2 layer to Sm_2O_3/SiO_2 dielectric stacks, as shown in Fig. 4.11(b). This result is similar to the aforementioned simulation result shown in Fig. 4.7.



(a)



(b)

Figure 4.11. (a) Quadratic VCC versus capacitance density and **(b)** quadratic VCC versus SiO_2 thickness (3 to 7 nm) for Sm_2O_3 thicknesses being varied (6.5, 7.5, 8.5, and 10 nm). Inset of **(b)** shows linear VCC versus SiO_2 thickness with varying the thickness of SiO_2 and Sm_2O_3. The linear VCC can be modulated to near zero by increasing the thickness of SiO_2.

High capacitance densities of above 7.3 fF/μm^2 and quadratic VCC within ±100 ppm/V^2 are successfully demonstrated with Sm_2O_3/SiO_2 thickness of 7.5 nm/4 nm, 6.5 nm/4 nm and 6.5 nm/3.5 nm, respectively. Moreover, from the change of α value with capacitance density, it is possible to achieve high capacitance density of over 8 fF/μm^2 and α of near zero ppm/V^2 by optimizing the ratio of SiO_2 thickness to whole thickness of the dielectric stack. The above experimental results satisfy the requirements of MIM capacitors for precision analog circuit applications until year 2013 [4.1]. Furthermore, the modulation of linear VCC (β) due to a varying SiO_2 thickness in a Sm_2O_3/SiO_2 dielectric stack is summarized in the inset of Fig. 4.11 (b). It is shown that the linear VCC can be also modulated by tuning the thickness of SiO_2. These results indicate the effective modulation of both quadratic and linear VCC of Sm_2O_3/SiO_2 MIM capacitors by inserting a thin PECVD SiO_2 layer.

Fig. 4.12 shows the frequency dispersion of the capacitance and the loss tangent of Sm_2O_3/SiO_2 MIM capacitors, with Sm_2O_3 being fixed at 7.5 nm and with SiO_2 thicknesses varying from 3 to 7 nm. Small capacitance variation is observed for these dielectric stacks. The loss tangent obtained at various frequencies is comparable to those reported [4.3, 4.4].

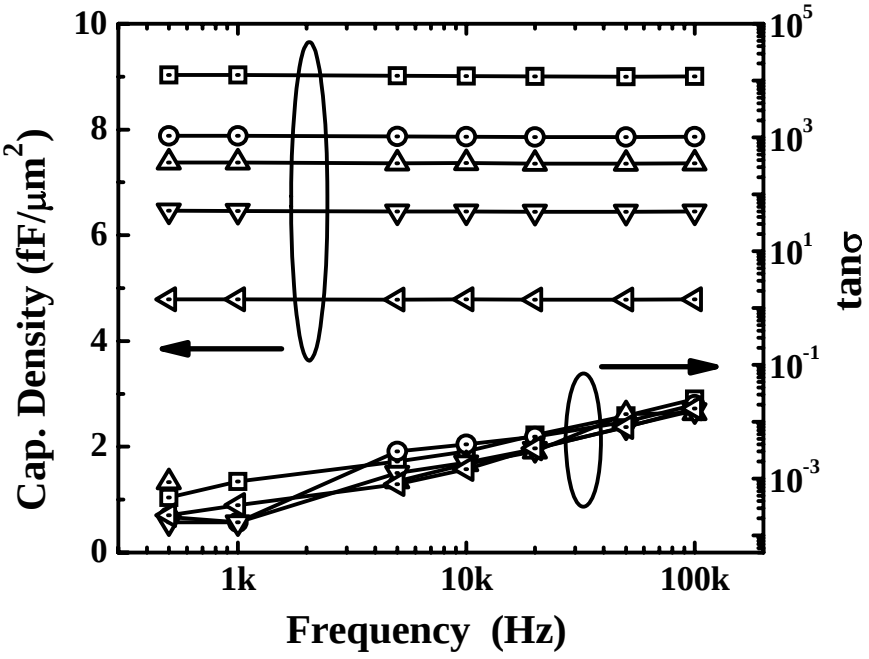


Figure 4.12. Frequency dispersion of the capacitance density and loss tangent of Sm_2O_3/SiO_2 MIM capacitors, with Sm_2O_3 being fixed at 7.5 nm while varying SiO_2 thickness from 3 to 7 nm.

Fig. 4.13 summarizes the leakage current densities of the capacitors with the Sm_2O_3 thickness (6.5, 7.5, 8.5 and 10 nm) and the SiO_2 thickness (3 to 7 nm) being varied. The typical *J-V* curves of the laminate MIM capacitors with three different thickness combinations are shown in the inset of Fig. 4.13. The leakage current density at +3.3 V are 1.86×10^{-7}, 1.03×10^{-7}, and 6.48×10^{-8} A/cm^2, respectively, for the splits with Sm_2O_3/SiO_2 thicknesses of 8.5 nm/3.5 nm, 6.5 nm/4.0 nm, and 8.5 nm/4.0 nm. Leakage current densities can be maintained at around 1.0×10^{-7} A/cm^2 at +3.3 V (room temperature) or even less. Furthermore, the breakdown field is about 6 MV/cm for the capacitors with SiO_2 thickness at 4 nm and Sm_2O_3 thickness at 6.5, 7.5 and 8.5 nm, as illustrated in the cumulative probability of breakdown field shown in Fig. 4.14. These results indicate the high quality of Sm_2O_3/SiO_2 dielectric stacks.

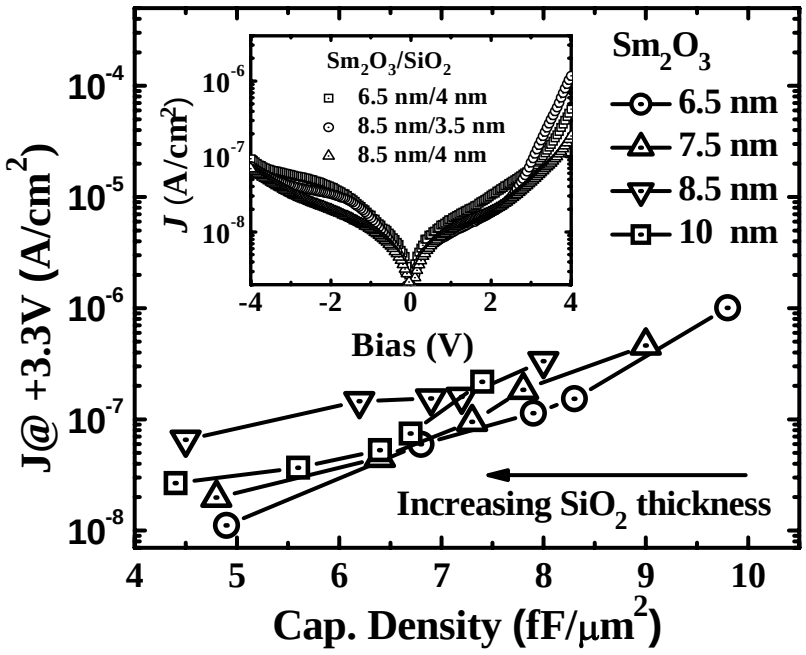


Figure 4.13. Summary of the leakage current densities of Sm_2O_3/SiO_2 MIM capacitors with various combinations of Sm_2O_3 (6.5, 7.5, 8.5, and 10 nm) and SiO_2 thicknesses. Inset shows the typical *J-V* curves

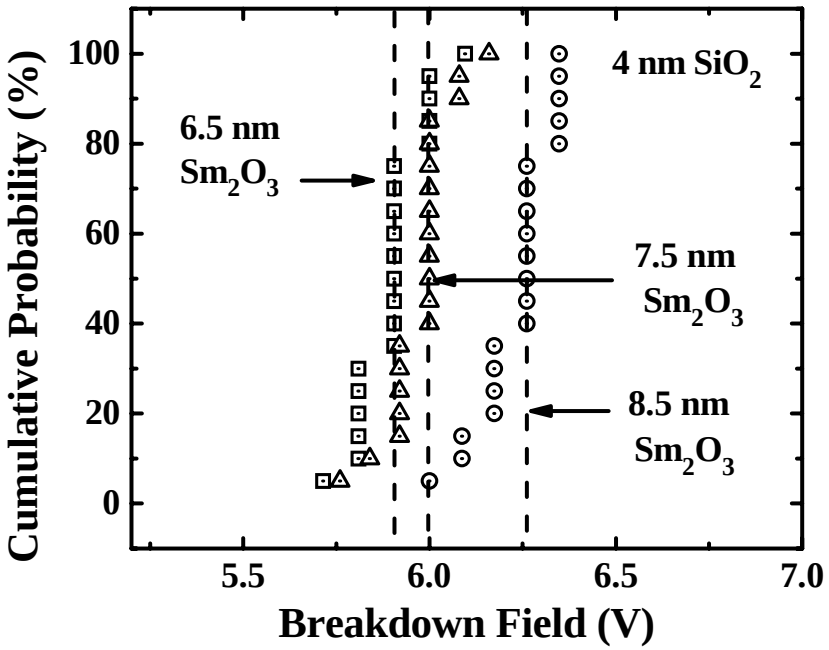


Figure 4.14. Cumulative probability of breakdown field of Sm_2O_3 MIM capacitors.

The temperature dependence of the *J-V* curves is shown in Fig. 4. 15. The *J-V* curves for the Sm_2O_3/SiO_2 laminate capacitors with Sm_2O_3 at 8.5 nm and SiO_2 at 3.5 nm are measured from room temperature to 120 °C. The asymmetric *J-V* characteristic of the capacitors is found for all temperatures. This is due to the asymmetric dielectric stacks and the different dielectric-electrode band offsets on the top and bottom electrodes [4.5]. The electron barrier between TaN and Sm_2O_3 is smaller than that at SiO_2/TaN interface. More of the electric field is dropped across the SiO_2 layer due to the differences in κ values and thicknesses.

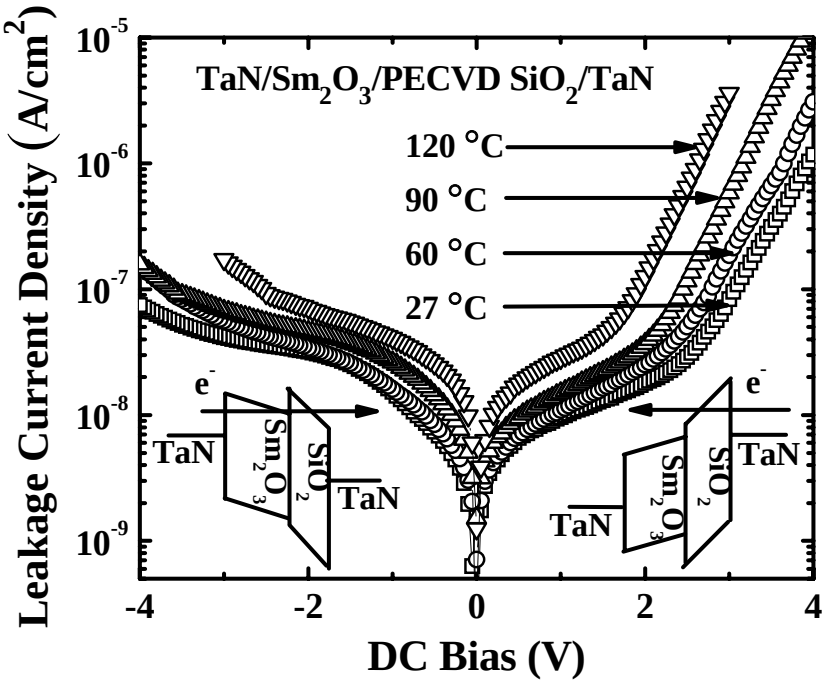


Figure 4.15. *J-V* curves of Sm_2O_3/SiO_2 capacitors with an 8.5 nm thick Sm_2O_3 and a 3.5 nm thick SiO_2 measured from 27 to 120 °C.

4.4. Summary

In this chapter, the MIM capacitors of Sm_2O_3 stacked with PVD and PECVD SiO_2 were investigated. Both of PVD and PECVD SiO_2 show negative quadratic VCC. Due to the small negative quadratic VCC of PVD SiO_2, the modulation of the effective quadratic VCC is not enough to meet the requirement of ITRS. On the contrary, by using PECVD SiO_2, we successfully demonstrate the stacked Sm_2O_3/ SiO_2 MIM capacitors with high capacitance densities (over 7.3 fF/cm^2), low quadratic VCCs (~-50 ppm/V^2), and low leakage current densities at +3.3 V (1×10^{-7} A/cm^2) by using the "cancelling effect" of SiO_2 and Sm_2O_3 dielectrics. Such "cancelling effect" of SiO_2 and Sm_2O_3 dielectrics can be further optimized to obtain higher capacitance density and near zero quadratic VCC. The characteristics of reported high capacitance density and low quadratic VCC satisfy the requirements of MIM capacitors in precision analog circuit applications till year 2013 according to ITRS 2007.

Reference:

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CHAPTER 5
INFLUENCE OF METAL ELECTRODES ON THE PERFORMANCE OF Sm_2O_3 MIM CAPACITORS

5.1. Introduction

MIM capacitors have been demonstrated high capacitance density by employing high-κ dielectrics [5.1-5.18]. The electrical characteristics of high-κ dielectrics for MIM capacitors in precision circuit applications have been reviewed in Chapter 2. By introducing other elements into binary metal oxides to form ternary or even fourfold metal oxides, the leakage current density and voltage linearity can be improved at a certain extent. Furthermore, the stacking of high-κ dielectrics with other dielectrics, especially with a thin SiO_2 layer which has a large negative quadratic VCC, can obtain significant reduction of quadratic VCC and also keep low leakage current density [5.12, 5.13].

These researches have been performed mainly on bulk dielectrics themselves. However, these reported high-κ MIM capacitors were fabricated on various metal electrodes, such as TiN [5.14, 5.15], TaN [5.11-5.13], Cu [5.16], and Pt [5.18]. Different electrical characteristics of the capacitors, including voltage linearity and leakage current density, have been reported by using different metal electrodes.

Recently, it is shown that by using a high work-function metal (Ni) to replace a low work-function metal (Al) as the top electrode can significantly improve the leakage current density [5.10]. These results indicate that the metal electrodes might influence significantly the performance of high-κ dielectric MIM capacitors. Therefore, it is necessary to investigate systematically the effect of different metal electrodes on high-κ MIM capacitors. In this chapter, Sm_2O_3 MIM capacitors with a series of metal electrodes, ranging from high work-function metals (Ni: 5.2 eV, Pt: 5.5 eV) [5.19] to low work-function metals (Al: 4.1 eV, HfN: 4.3 eV), have been fabricated and characterized. The results of electrical characteristics, including voltage linearity, leakage current density, temperature dependence of the capacitance, and hysteresis of the capacitance have been compared and analyzed with the capacitors with TaN electrodes.

5.2. Experiments

Sm_2O_3 MIM capacitors were fabricated on Si wafers covered with a 400 nm thick thermally-grown SiO_2. Various metal electrodes, such as Al, HfN, TaN, Ni, and Pt, with the thickness of 50, 150, 150, 50, and 50 nm were deposited by reactive sputtering in an Ar ambient (Al, Ni, and Pt) or Ar/N_2 ambient as bottom electrodes (HfN, TaN), respectively. For Al, Ni and Pt metals, a 150 nm TaN layer was deposited on the 400 nm thick SiO_2 layer as a buffer layer before metal deposition. After bottom electrode formation, a single Sm_2O_3 layer was directly deposited on the bottom electrodes by sputtering at room temperature in Ar ambient. The thickness of

the Sm_2O_3 layer was controlled by adjusting the sputtering time. Following that, Post-Deposition Annealing (PDA) at 400 °C for 120 s in an N_2 ambient was performed for all samples. After dielectric formation, corresponding metal electrodes (Al, HfN, TaN, and Ni,) were deposited on Sm_2O_3 dielectrics as top electrodes. For the capacitors with Al and Ni electrodes, a 100 nm TaN layer was deposited after Al and Ni deposition. For the capacitors with a Pt bottom electrode, a 150 nm thick TaN layer was sputtered as the top electrode due to the ease of etching TaN for electrode definition. The top electrodes for Al, HfN, and TaN were defined by lithography and dry-etching. For the capacitors with a Ni electrode, the top electrode was defined by lithography and wet-etched by using diluted HNO_3 (5%).

5.3. Properties of Sm_2O_3 MIM Capacitors with Different Metal Electrodes

5.3.1. Sm_2O_3 MIM Capacitors with High Work-Function Metal Electrodes

Fig 5.1 shows the normalized *C-V* curves of Sm_2O_3 MIM capacitors with metal electrodes of TaN, Ni and Pt respectively. It is observed that the capacitor with Pt bottom electrode has smaller capacitance variations with the voltage changing, as compared to those with TaN and Ni electrodes. Moreover, the capacitor with Pt bottom electrode shows more symmetric *C-V* curves, indicating less interfacial layer at the interface of dielectric/bottom electrode.

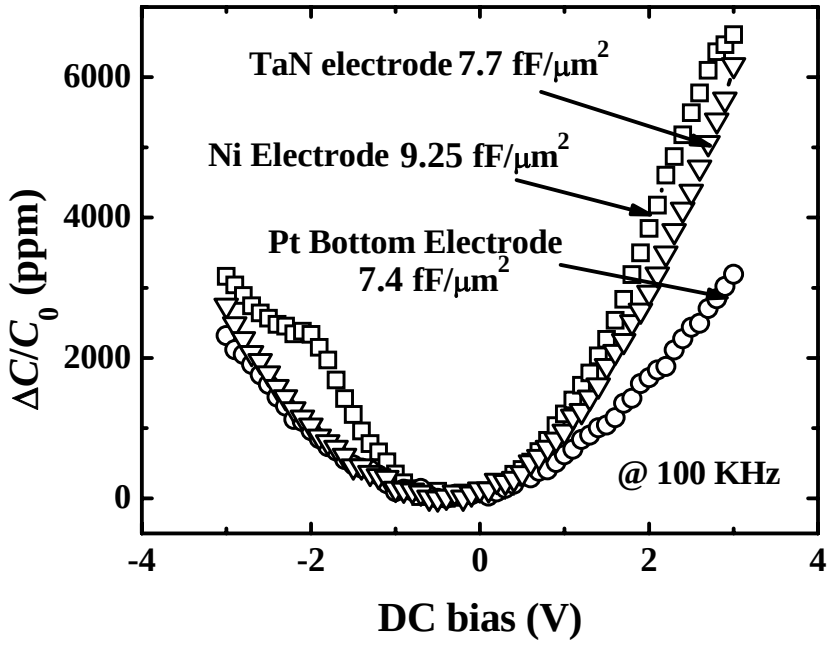
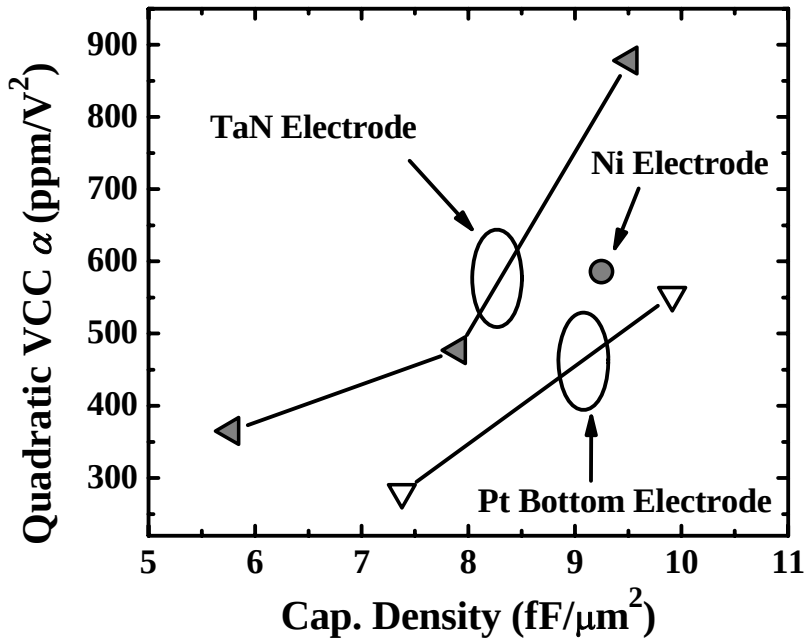
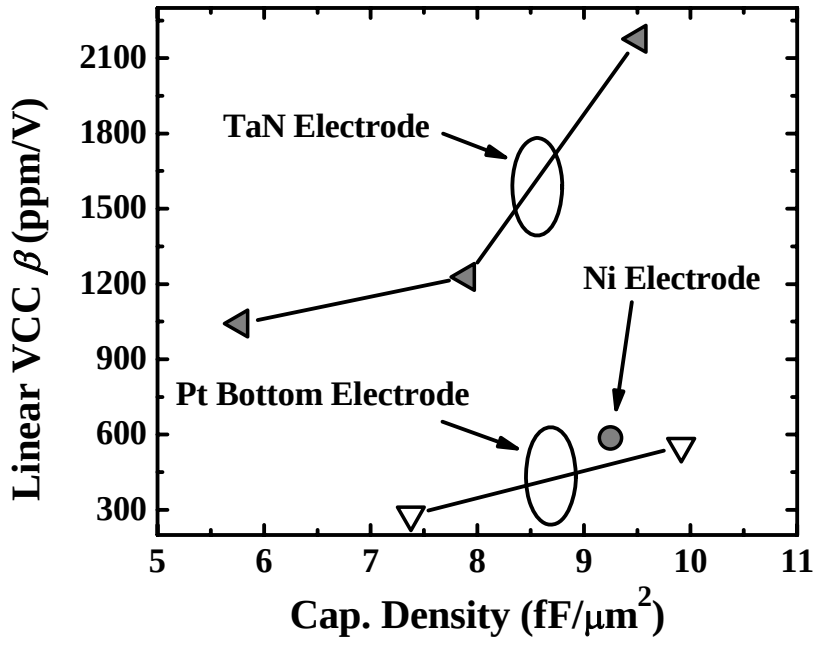


Figure 5.1. Normalized *C-V* curves of Sm_2O_3 MIM capacitors with TaN, Ni and Pt electrodes, respectively.

Fig 5.2 (a) & (b) compares the quadratic and linear VCC of Sm_2O_3 MIM capacitors with Ni and Pt electrodes and that with a TaN electrode. Low quadratic VCC values of 280 and 553 ppm/V^2 of the capacitors by using Pt as bottom electrodes are obtained, for the capacitance densities of 7.4 and 9.9 fF/μm^2 respectively. The obtained quadratic VCC is smaller than those of 477 and 586 ppm/V^2 for the capacitors by using TaN and Ni electrodes with the capacitance densities of 7.9 and 9.25 fF/μm^2, respectively. The result of quadratic VCC reduction is similar to [5.10], which shows that the reduction of the quadratic VCC from 953 to 447 ppm/V^2 by using Ni to replace Al as top electrodes. Moreover, the linear VCC can be also reduced by using Pt electrodes [Fig. 5.2 (b)]. This is probably due to the suppression of interface react during dielectric deposition and PDA.



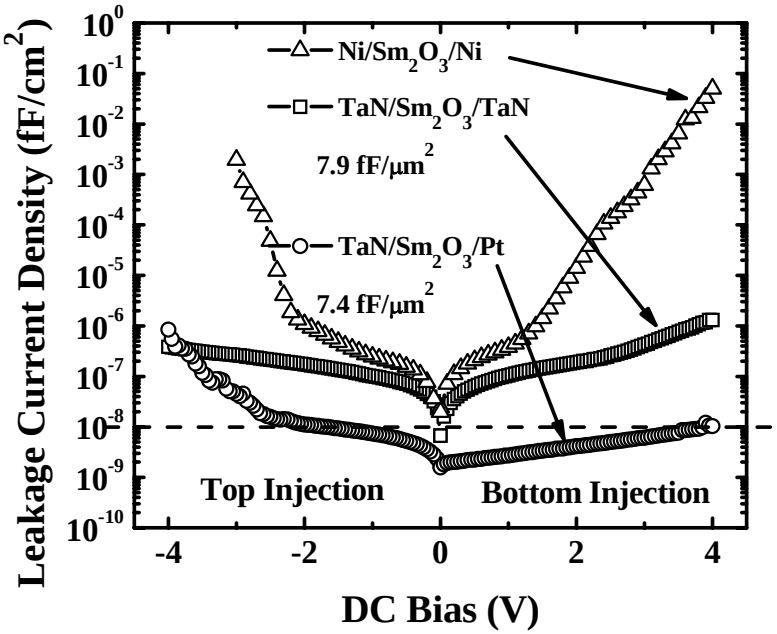
(a)



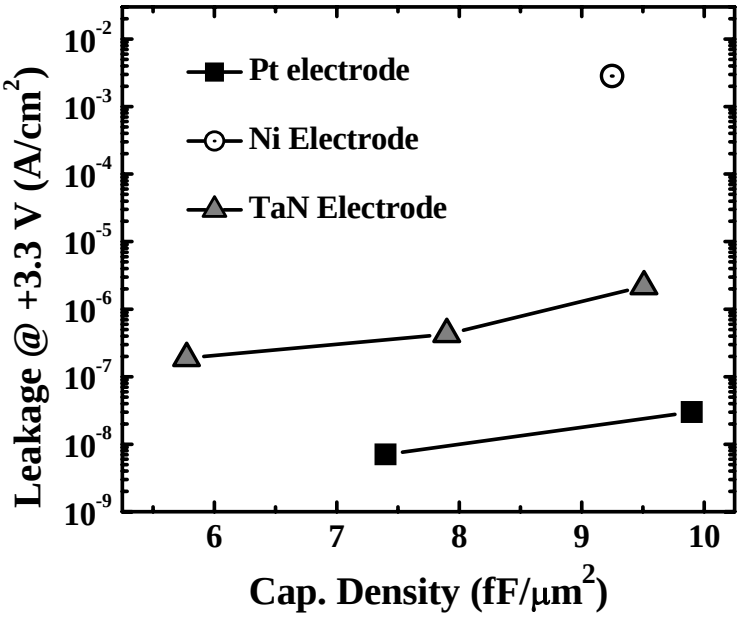
(b)

Figure 5.2. Summary of quadratic VCC **(a)** and linear VCC **(b)** of Sm_2O_3 with Ni, Pt and TaN bottom electrode. Both the quadratic and linear VCC can be reduced by using Pt electrodes.

The typical *J-V* characteristics of the capacitors by using TaN, Ni and Pt electrodes are plotted in Fig 5.3 (a). A significant reduction of the leakage current density is observed by using Pt metal electrodes, in comparison with those by using TaN and Ni electrodes. More than two orders of magnitude reduction in leakage current density is obtained by using Pt electrodes, especially at positive bias (bottom injection from Pt electrode). This result is similar to [5.10]. We believe that it is due to the larger conduction band offset of Pt with Sm_2O_3 and better interface of dielectric/Pt bottom electrode. The leakage at +3.3 V versus capacitance density is summarized in Fig. 5.3 (b). The obtained leakage current density at +3.3 V of the capacitors with Pt bottom electrode is around 7×10^{-9} A/cm^2, which satisfy the requirement of leakage current density according to ITRS 2007 [5.20].



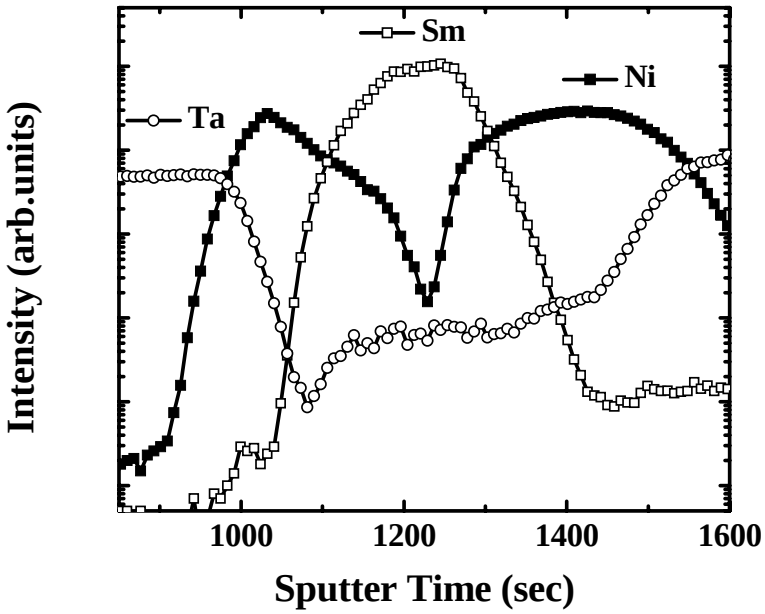
(a)



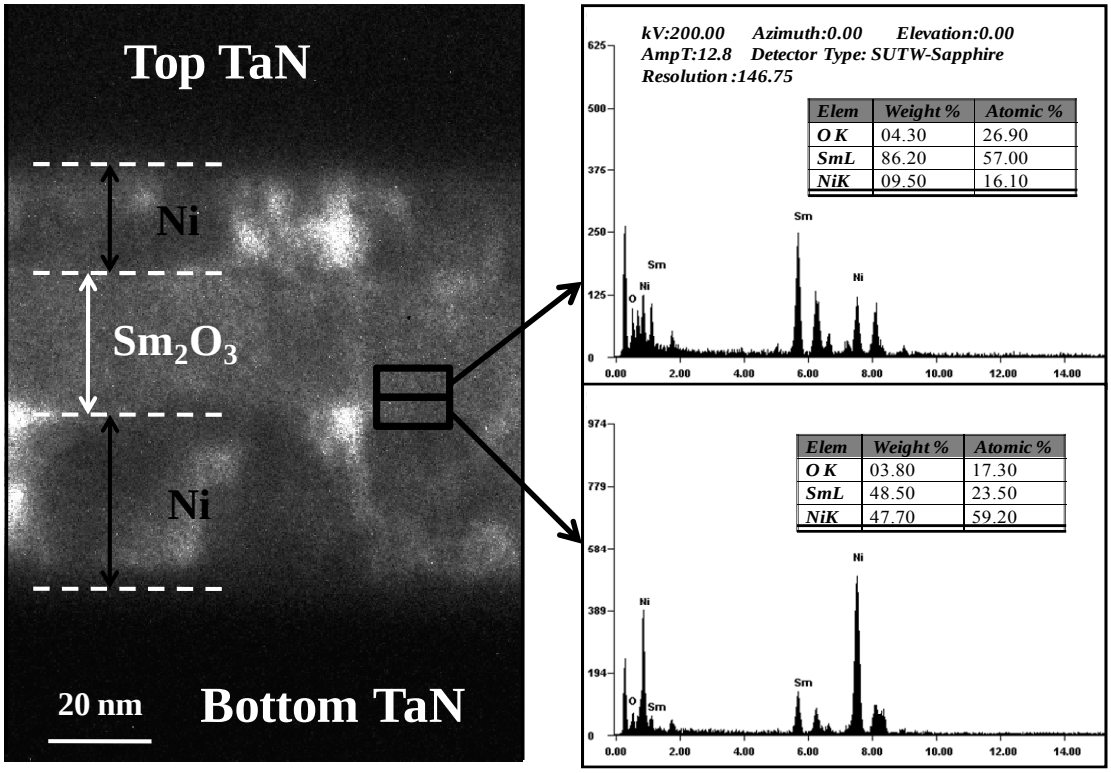
(b)

Figure 5.3. **(a)** *J-V* curves of Sm_2O_3 MIM capacitors with TaN, Ni, and Pt electrodes. Significantly leakage reduction of the capacitor by using Pt electrode can be obtained. **(b)** Summary of leakage at +3.3 V versus capacitance density.

Note that the capacitor with a Ni electrode exhibits high leakage current density. It is probably due to the inter-diffusion of Ni and Sm_2O_3 during post-deposition annealing (400 ^oC) and thus deteriorates the quality of dielectrics. To investigate further, we have done Secondary Ion Mass Spectrometry (SIMS) analysis and Energy Dispersive X-ray analysis (EDX) on this MIM structure, as shown in Fig 5.4 (a) and (b), respectively. The SIMS depth profile of TaN/Ni/Sm_2O_3/Ni/TaN structures shows a slightly diffusion of Sm and Ni at the bottom electrode. Furthermore, the EDX results illustrate the presence of both Ni and Sm elements at (or near) the interface of Sm_2O_3/bottom Ni electrode. The aforementioned results demonstrate the inter-diffusion of Ni and Sm elements at the interface of bottom electrode, and this is probably the reason of high leakage current density.



(a)



(b)

Figure 5.4. **(a)** SIMS depth profile of the Sm_2O_3 capacitor with TaN/Ni/Sm_2O_3/Ni/TaN structure. **(b)** EDX results of Ni/Sm_2O_3/Ni structures. The material study shows the inter-diffusion of Ni and Sm elements.

The hysteresis of the capacitance with different metal electrodes is summarized in Fig 5.5. C_{M+} and C_{M-} are the minimum values of the capacitance obtained by sweeping the DC voltage from +3 to -3 V and from -3 to +3 V, respectively. It can be observed that lower capacitance variation (~40 ppm) is obtained by using Pt and Ni metal electrodes, in comparison to that with a TaN electrode (117 ppm).

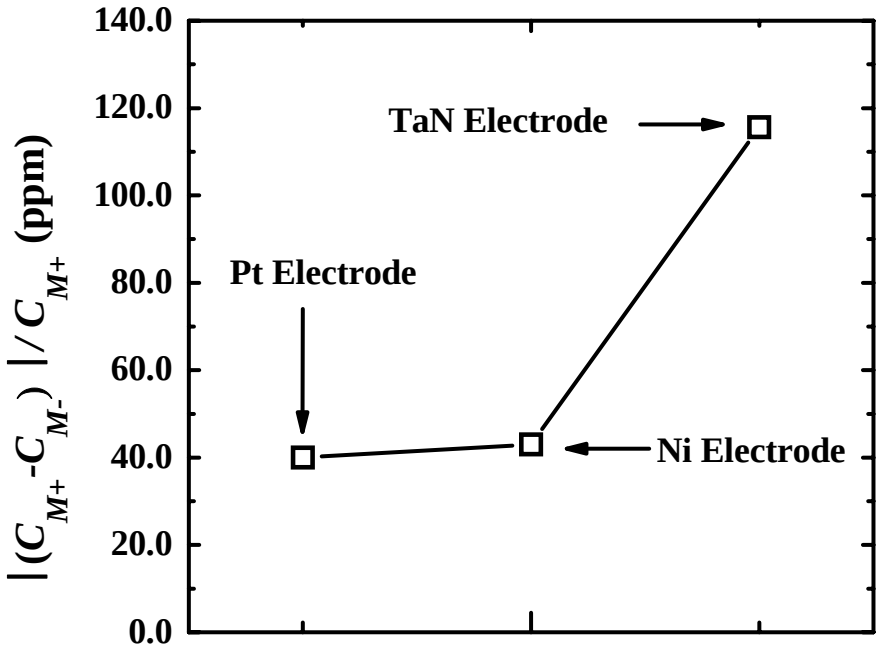


Figure 5.5. Comparison of the hysteresis of the capacitance density of Sm_2O_3 MIM capacitors with TaN, Ni and Pt electrodes, respectively.

The Sm_2O_3 MIM capacitors with Pt electrodes have been demonstrated excellent electrical characteristics, including small voltage linearity, low leakage current density, and small hysteresis of the capacitance, as compared to those with Ni and TaN electrodes. It is necessary to investigate the influence of Pt electrodes on the TCC characteristics. Fig. 5.6 compares the temperature dependence of the capacitance of

Sm_2O_3 MIM capacitors with TaN, Ni and Pt electrodes. The capacitance was measured at the frequency of 100 kHz with the temperature up to 120 ^oC. The extracted TCC of the capacitors with a Pt electrode is 49 ppm/^oC, which are much smaller than that of 94 ppm/^oC with a TaN electrode and 220 ppm/ ^oC with a Ni electrode, indicating that Pt electrode can significantly improve the TCC characteristics.

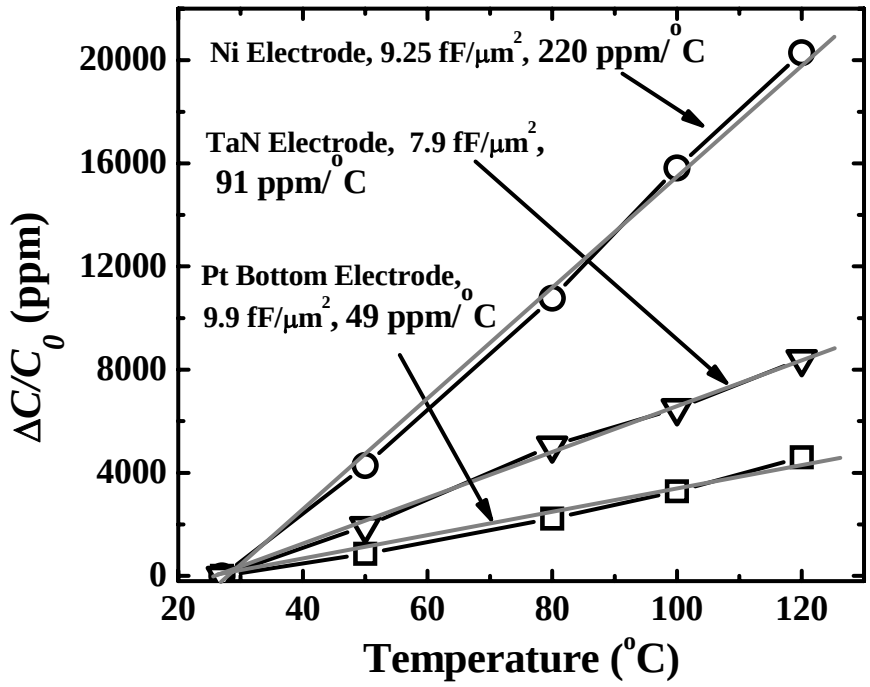


Figure 5.6. Comparison of the temperature dependence of the capacitance of Sm_2O_3 MIM capacitors with TaN, Ni and Pt electrodes, respectively.

The aforementioned results show that by employing Pt as bottom electrodes, the electrical characteristics can be significantly improved, including voltage linearity, leakage current density, TCC and hysteresis of capacitance. These improvements might be due to the high conduction band offset of dielectric/electrode and robust interface of dielectric/electrode as Pt is an inert metal electrode.

5.3.2. Sm_2O_3 MIM Capacitors with Low Work-Function Metal Electrodes

Fig 5.7 shows the normalized *C-V* curves of Sm_2O_3 MIM capacitors with Al, HfN and TaN electrodes. A high capacitance variation with the voltage of the capacitors with Al electrode is observed, as compared to that with a TaN electrode.

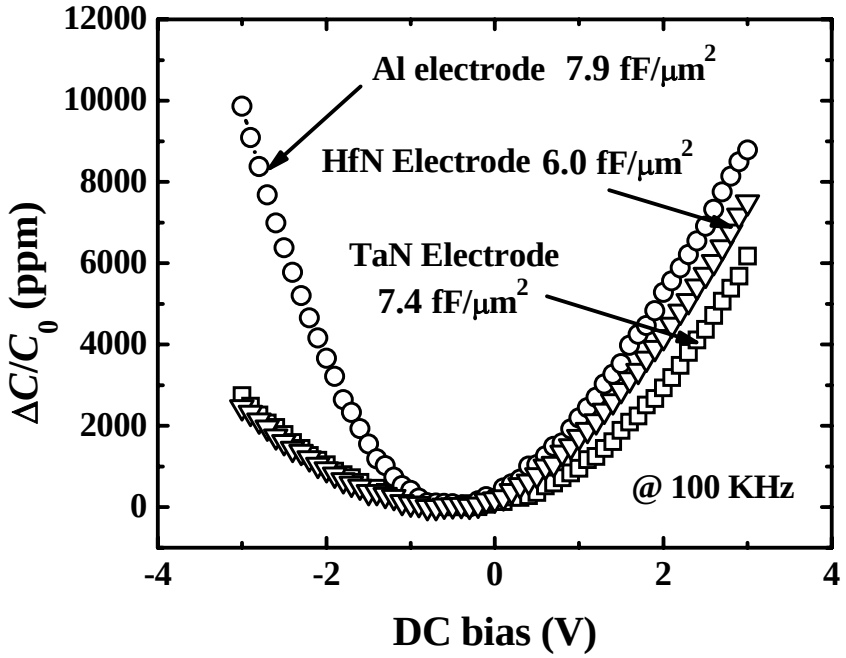
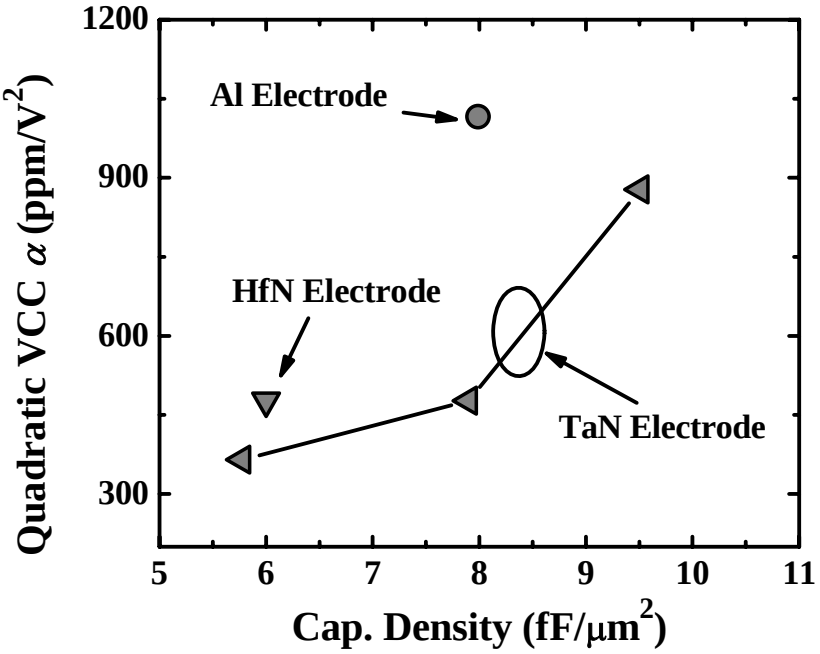
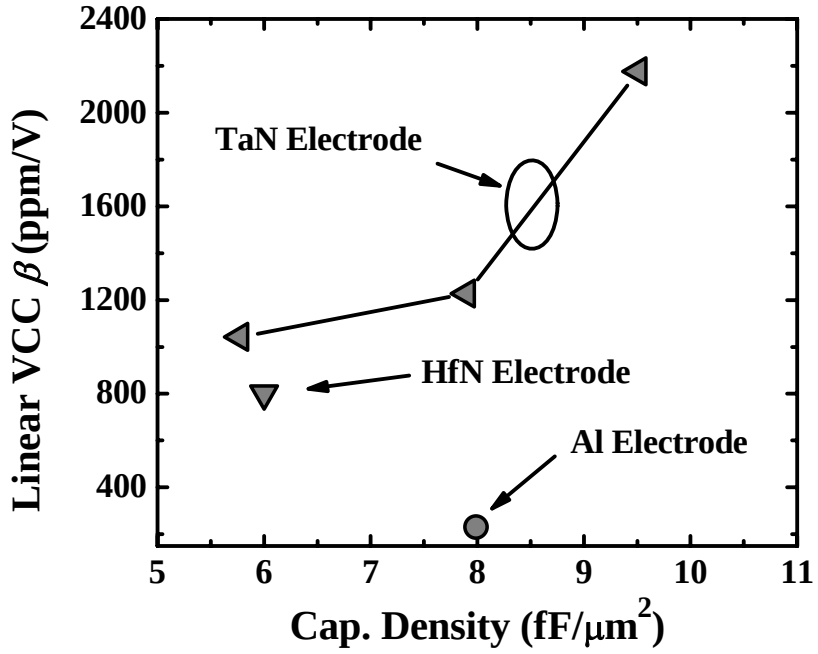


Figure 5.7. Normalized *C-V* curves of Sm_2O_3 MIM capacitors with Al, HfN, and TaN, electrodes, respectively.

The extracted quadratic VCC and linear VCC of the capacitors with Al, HfN, and TaN electrodes are summarized in Fig 5.8 (a) and (b), respectively. The capacitor with an Al electrode shows large quadratic VCC (1099 ppm/V^2), as compared to that with a TaN electrode (477 ppm/V^2 at 7.9 fF/μm^2), indicating that Al is not suitable to be the MIM electrodes. The linear VCC of the capacitors with HfN and TaN electrodes are larger than that with Al electrode. This might be due to the interfacial layer at the dielectric/bottom electrode.



(a)



(b)

Figure 5.8. Summary of quadratic VCC **(a)** and linear VCC **(b)** of Sm_2O_3 with Al, HfN and TaN bottom electrodes, respectively.

For the capacitors with an HfN electrode, the capacitance density is pretty low (~6 fF/μm^2), as compared to that with a TaN electrode (7.9 fF/μm^2). Note that the dielectric deposition time for the capacitors with HfN and TaN electrodes are the same. The dramatic reduction of the capacitance density implies that the interface of dielectric/electrode might suffer significant reaction during dielectric deposition and post-deposition annealing. To investigate the interface of dielectric/HfN electrode, we have done secondary ion mass spectrometry (SIMS) analysis on this MIM structure, as shown in Fig 5.9. The SIMS depth profile shows a smaller gradient of Hf elements at the right side (bottom HfN electrode) as compared to that at left side (top HfN electrode). This result imply that the interface reaction, i.e., Hf diffusion into Sm_2O_3 (oxidation of bottom HfN), occurs at the bottom HfN electrode during post deposition annealing.

To investigate further the interface of the dielectric/HfN electrode, we have also done TEM and EDX analysis on it, as shown in Fig 5.10 (a) and (b). From the TEM image, a 5 nm thick interfacial layer at the Sm_2O_3 dielectric/bottom HfN electrode can be clearly observed. This result is different from the TEM image of the Sm_2O_3 capacitor with a TaN electrode [Fig 3.6]. This interfacial layer is Hf-riched dielectric, i.e., Hf-Sm-O, as illustrated in Fig 5. 10 (b), indicating that the bottom HfN electrode is significantly oxidized during dielectric deposition and post deposition annealing. This interfacial layer is believed to result in the significant reduction of the capacitance density.

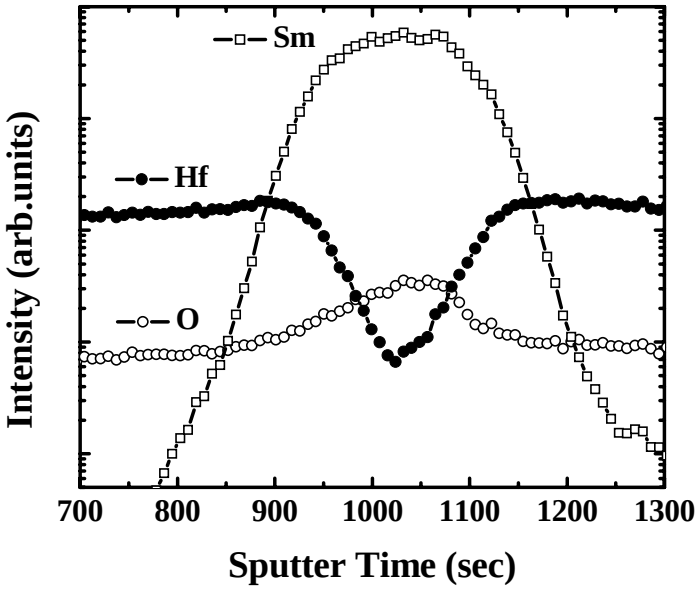


Figure 5.9. SIMS depth profile of the Sm_2O_3 capacitor with HfN electrodes.

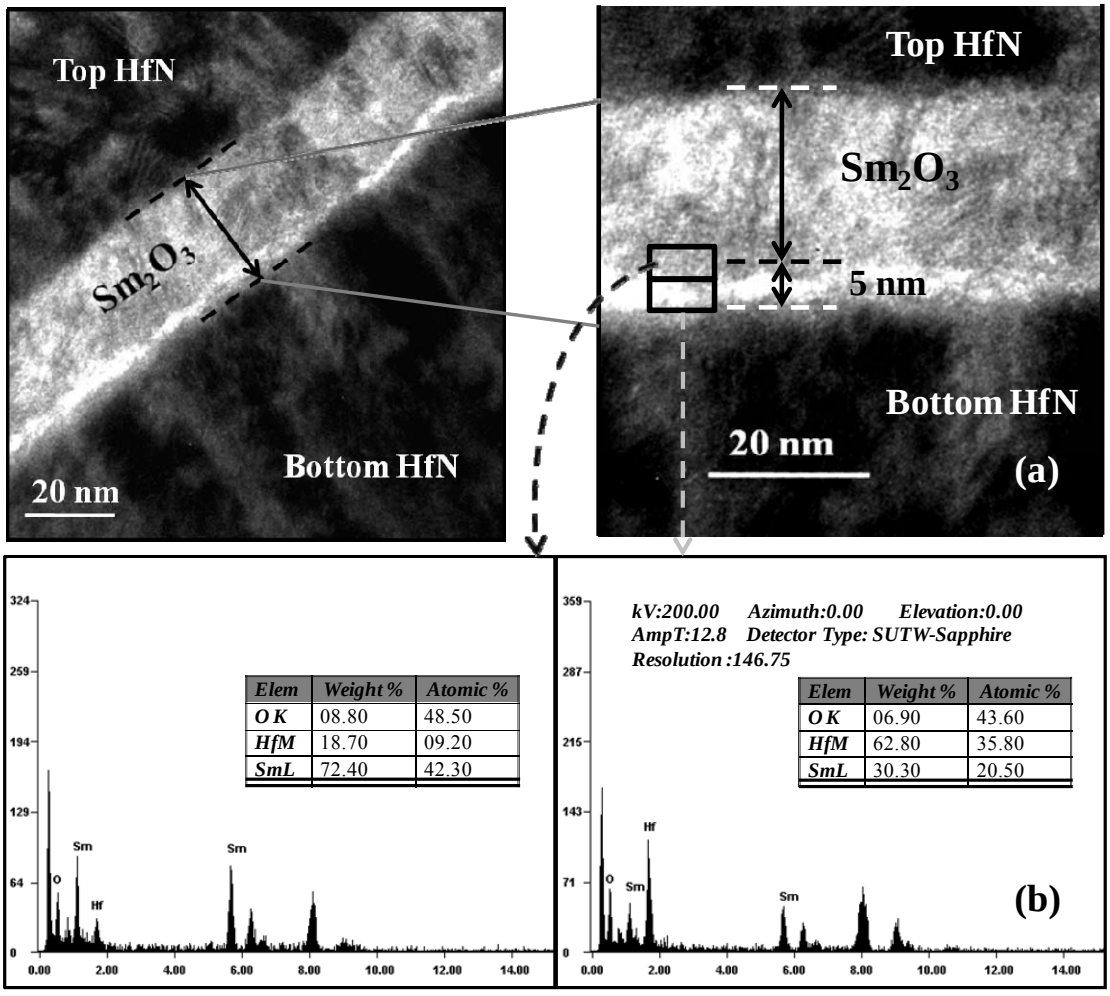
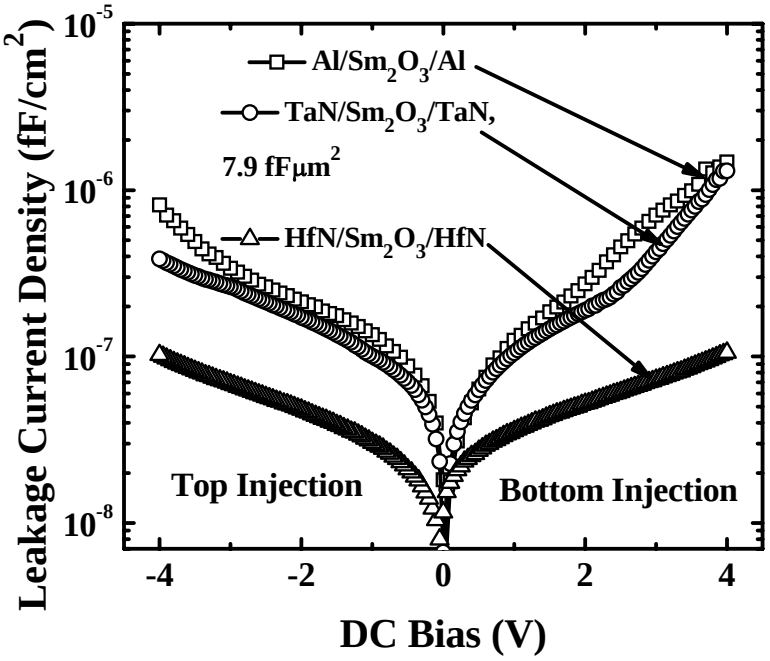
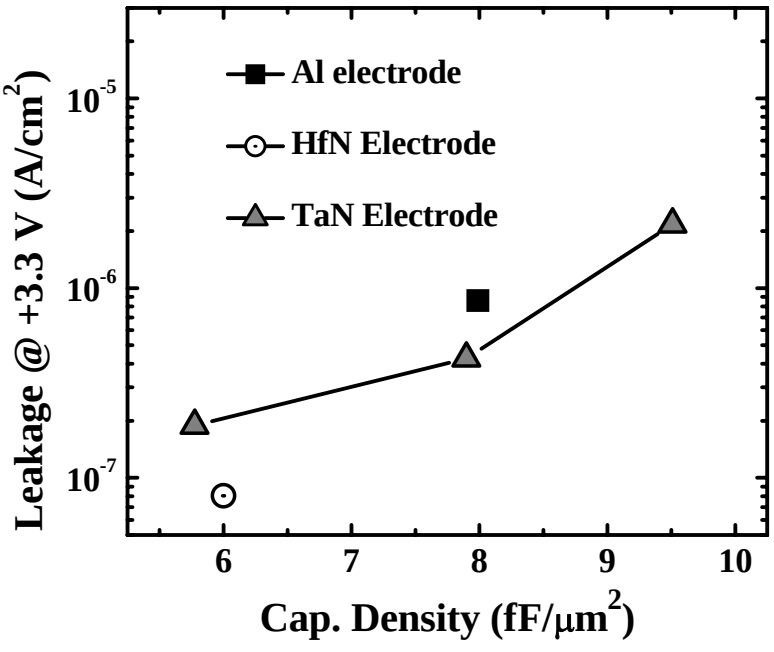


Figure 5.10. **(a)** TEM image and **(b)** EDX analysis of HfN/Sm_2O_3/HfN MIM capacitor.



(a)



(b)

Figure 5.11. **(a)** *J-V* curves of Sm_2O_3 MIM capacitors with Al, HfN, and TaN electrodes. **(b)** Summary of leakage @ +3.3 V versus capacitance density. The capacitor with an HfN electrode shows a smaller leakage current density.

The *J-V* characteristics of the capacitors with Al, HfN, and TaN electrodes are plotted in Fig 5.11 (a). The leakage current density at +3.3 V versus capacitance density is summarized in Fig 5.11 (b). The capacitor with an Al electrode shows larger leakage current density, as compared to that with a TaN electrode. On the contrary, the capacitor with an HfN electrode shows smaller leakage current density. We believe that this is because that the interface of dielectric/HfN is better than others, i.e., HfON might be better than TaON as Ta_2O_5 normally exhibit high leakage current density [5.16, 5.21] as compared to HfO_2.

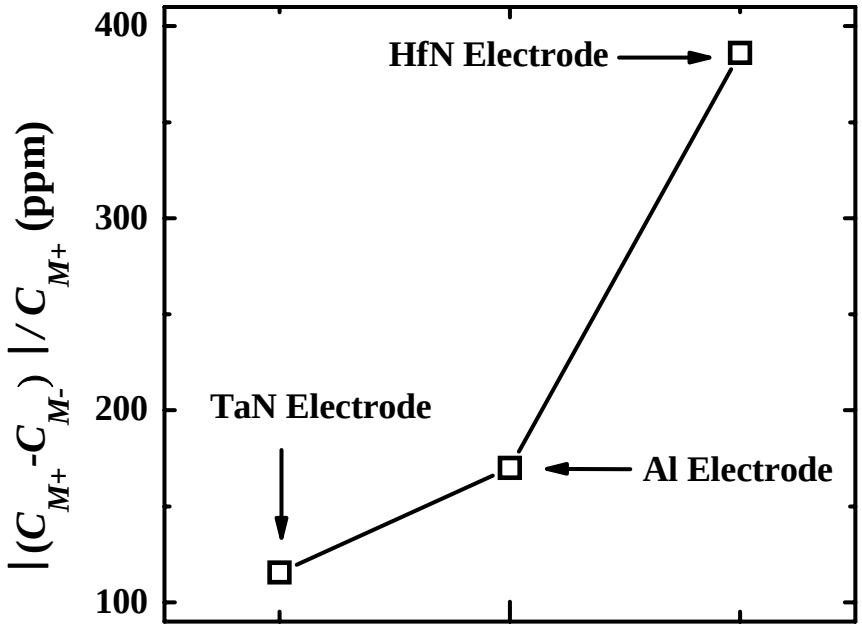


Figure 5.12. Comparison of the hysteresis of the capacitance density of Sm_2O_3 MIM capacitors with Al, HfN and TaN electrodes.

Fig 5.12 shows the hysteresis of the capacitance with Al, HfN, and TaN metal electrodes. The capacitors with Al and HfN metal electrodes show much large

capacitance variation (~386 ppm for HfN and 172 ppm for Al). The large hysteresis of the capacitors with an HfN electrode might be due to the traps in the interfacial layer at the dielectric/bottom HfN elelctrode.

Fig 5.13 compares the TCC characteristics of the capacitors with Al and TaN metal electrodes. Note that the data of the capacitors with an HfN electrode is not included. This is due to the influence of the interfacial layer at dielectric/bottom HfN electrode. When increasing the temperature, the bottom electrode become unstable and thus makes it hard to measure the capacitance. The extracted TCC characteristic of the capacitor with Al electrode is around 196 ppm/^{o}C, which is larger than that with TaN electrode, indicating that the Al electrode can be easier influenced by the temperature.

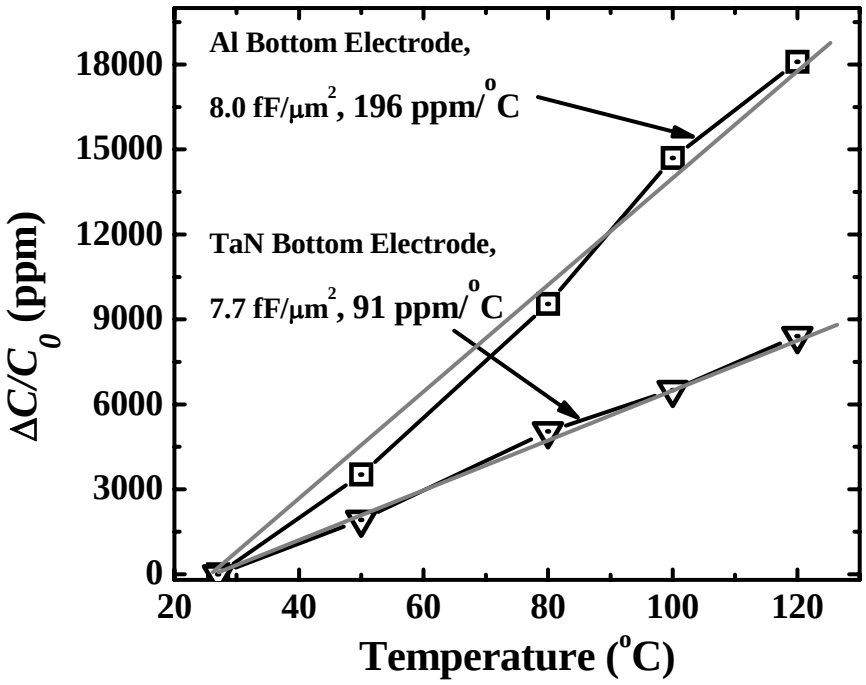


Figure 5.13. Comparison of the temperature dependence of the capacitance of Sm_2O_3 MIM capacitors with Al and TaN electrodes, respectively.

In short, the electrodes with low work-function show negative effects on the performance of Sm_2O_3 MIM capacitor, as compared to those with high work-function electrodes.

5.3. Summary

The influence of the metal electrodes on the performance of Sm_2O_3 MIM capacitors has been investigated. The metal electrodes with high work-function, such as Ni and Pt, can obtain small voltage linearity and hysteresis of the capacitance, in comparison with TaN electrodes. Moreover, by using Pt as bottom electrode, low leakage current density and small temperature dependence of the capacitance have been demonstrated. The promising results are believed to be due to the high conduction band offset of dielectric/electrode and excellent interface of dielectric/electrode. On the contrary, low work-function metals, such as Al and HfN, show the negative effects on the electrical characteristics of Sm_2O_3 MIM capacitors. The results and possible reason have been discussed in this chapter. The aforementioned results indicate a high work-function metal electrode with a robust interface at the dielectric/electrode is essential to improve the performance of high-κ MIM capacitors.

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CHAPTER 6

CONCLUSION AND FUTURE WORKS

6.1. Conclusion

In this thesis, a novel Sm_2O_3 based high-κ MIM capacitors for high precision applications have been fabricated and characterized. The properties of MIM capacitors with a single Sm_2O_3 layer and (or) stacked with a thin SiO_2 layer have been investigated systematically, including the electrical and physical characteristics. Moreover, the influence of the post deposition plasma treatment and the metal electrodes on the performance of Sm_2O_3 MIM capacitors has been studied. The important findings and conclusions obtained in the course of the studies can be summarized as the following:

1. The electrical and the physical characteristics of Sm_2O_3 MIM capacitors with various Sm_2O_3 capacitance densities are systematically investigated for the first time. The physical characteristics of Sm_2O_3 MIM capacitors are studied by using techniques such as TEM, XRD and XPS. The dielectric permittivity of Sm_2O_3 is calculated to be around 22, which is comparable to that of the widely studied HfO_2 dielectric. Sm_2O_3 dielectric has demonstrated excellent electrical characteristics, including small quadratic VCC, TCC and low leakage current

density. Sm_2O_3 dielectric is a promising candidate for the application of high-κ dielectric MIM capacitors in precision analog circuit applications.

2. The effects of plasma treatments with O_2 and/or N_2 on the performance of MIM capacitors with Sm_2O_3 dielectric have been investigated for the first time. We examine the effects of PTN on Sm_2O_3 MIM capacitors by inserting the PTN process at various stages of the device fabrication: after bottom electrode formation, after dielectric formation, or after each of the two steps. It is shown that plasma treatment in N_2 ambient after Sm_2O_3 dielectric formation can effectively improve the electrical characteristics, including the voltage linearity, hysteresis and leakage current density. PTN after dielectric formation is an effective way to improve the performance of high-κ dielectric MIM capacitors for precision analog circuit applications.

3. The MIM capacitors of Sm_2O_3 dielectric stacked with a thin PVD or PECVD SiO_2 layer have been investigated. The stacked Sm_2O_3/ PECVD SiO_2 MIM capacitors with high capacitance densities (over 7.3 fF/cm^2), low quadratic VCCs (~-50 ppm/V^2) and low leakage current densities at +3.3 V (1×10^{-7} A/cm^2) have been demonstrated by using the "cancelling effect" of SiO_2 (having negative quadratic VCC) and Sm_2O_3 dielectrics. Such "cancelling effect" of SiO_2 and Sm_2O_3 dielectrics can be further optimized to obtain higher capacitance density and near zero quadratic VCC. The characteristics of reported high capacitance density and low quadratic VCC satisfy the requirements of MIM capacitors in

precision analog circuit applications till year 2013 according to ITRS 2007.

4. The influence of metal electrodes on the performance of Sm_2O_3 MIM capacitors has been investigated systematically. High work-function metals are found to significantly improve the electrical characteristics of MIM capacitors, especially for Pt electrode, including voltage linearity, leakage current, hysteresis and TCC characteristics. By contraries, low work-function metals show negative effects on the electrical characteristics. These results indicate that the metal electrode influence significantly the performance of high-κ MIM capacitors. A metal electrode with a high work-function and good interface of dielectric/electrodes is much desirable.

6.2. Future Works

More detailed investigation and further exploration will be necessary to further optimize the process described in this thesis. It is suggested further studies on high-κ MIM capacitors for high precision applications should center on the improvement of the quality of dielectrics and the interface of dielectric/electrodes.

Due to the temperature limitation of thermal budget of BEOL, the post deposition treatments with low temperature is important to improve the quality of dielectrics. It has been demonstrated that PTN can improve the performance of MIM capacitors. This process needs to be further optimized and the effect of plasma

treatment is worthy to be analyzed.

The voltage linearity can be tailored by using a thin SiO_2 layer which has a large negative quadratic VCC. This method is effective to achieve a low quadratic VCC to meet the requirements of ITRS for MIM capacitors. However, the leakage current is still an issue due to the quality of the thin SiO_2 and high-κ dielectrics. Other dielectric deposition tools, such as atomic-layer deposition (ALD), can be utilized to improve dielectric quality.

It has been demonstrated that the metal electrodes influence significantly the performance of high-κ MIM capacitors. The quality of the interfacial layer at the dielectric/electrode is essential to improve the performance of high-κ MIM capacitors. Although Pt metal electrode can obtain excellent electrical characteristic, the economic issue makes it unacceptable in mass production. It is necessary to explore an economical inert metal with high work-function and a robust interface for the high-κ MIM capacitors.

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