LANTHANOID BASED MATERIALS IN ADVANCED CMOS TECHNOLOGY

CHEN JINGDE

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CHEN JINGDE

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ABSTRACT

Aggressive complementary metal-oxide-semiconductor (CMOS) scaling requires the development of new materials and device architectures. This dissertation focuses on introducing lanthanoid based materials into CMOS technology to address some of the new challenges in CMOS scaling.

The low work function lanthanoid silicides are potential candidates for N-type Schottky source/drain field-effect transistor (N-SSDT). Several lanthanoid elements, including Dy, Er, Tb and Yb, were investigated to form the self-aligned silicide (salicide) S/D for N-SSDT. The $YbSi_{2-x}$ has been found to be a very promising candidate for N-SSDT as it provides a high drive current with a very low leakage current. By addressing the compatibility issues of lanthanoid materials with conventional CMOS process, a low temperature, implantation free MOSFET process featuring a "hole spacer", Schottky barrier source/drain, high-κ dielectric and metal gate electrode was successfully developed.

The elimination of polysilicon gate depletion effect and reduction in gate leakage current are major advantages of metal gate/high-κ dielectric gate stack over conventional polysilicon/SiO(N) gate stack. However, achieving the desired effective metal gate work function Φ_m to meet threshold voltage requirements in future CMOS devices is one of the main hurdles for its implementation. We demonstrate two methods for tuning the metal gate work function towards the silicon conduction band edge. The first one is to incorporate ytterbium (Yb) into Ni fully-silicided (Ni-FUSI) gate. Yb has a low work function of 2.59 eV. During the silicidation process, Yb atoms accumulate at the $NiSi/SiO_2$ interface and achieved a FUSI gate Φ_m lowering of

about 0.3 to 0.5 eV. However, this method is less effective on high-κ dielectrics. The second method is to incorporate lanthanoid oxides into hafnium oxide gate dielectric. Conduction band-edge TaN gate Φ_m values of 4.1 to 4.24 eV were obtained by doping HfO_2 gate dielectric with Er_2O_3 and several other lanthanoid oxides. Interface dipole models were discussed to explain the effective gate Φ_m tunability.

After addressing the challenges active device, we explore the scaling down of metal-insulator-metal (MIM) capacitors by investigating a series of lanthanoid oxides as candidates for the insulator layer. MIM capacitors using Sm_2O_3 or Er_2O_3 dielectric material were found to have better voltage linearity as compared with other high-κ materials at the same capacitance density. Satisfactory leakage current and frequency dispersion properties indicate that both oxides are promising. It was found that both oxygen vacancy in the dielectric film and the interfacial layer at the high-κ/bottom electrode interface played an important role in the voltage linearity of the MIM stack. An innovative dielectric structure is developed by intentionally inserting a thin SiO_2 layer between the lanthanoid oxide and bottom electrode. We achieved high capacitance density (up to 8.5 fF/μm^2) with quadratic VCC lower than 100 ppm/V^2 by engineering the thickness ratio of high-κ to SiO_2 layers. This performance can meet the International Technology Roadmap for Semiconductors (ITRS) requirements in 2013 and indicates that MIM capacitors with high-κ/SiO_2 dielectric stack can be a long-term solution to RF and analog/mixed-signal capacitor technology.

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LIST OF SYMBOLS

Symbol	**Description**	**Unit**
C	Capacitance	fF/μm^2
C_{ox}	Capacitance of gate oxide	fF/μm^2
E_c	Si conduction band-edge	eV
E_F	Fermi-level energy	eV
E_v	Si valence band-edge	eV
E_{vac}	Vacuum level	eV
f	Frequency	Hz
I_D	Transistor drive current	A
J_G	Gate current density	A/cm^2
$m*$	Effective mass	kg
N_d	Doping concentration	cm^{-2}
Q_{ox}	Oxide fixed charge density	cm^{-2}
q	Electronic charge	C
t_{ox}	Dielectric physical thickness	nm
T_{ox}	Equivalent oxide thickness	nm
V_{ds}	Transistor drain voltage	V
V_{gs}	Gate voltage	V
V_{FB}	Flatband voltage	V
V_{th}	Threshold voltage	V
α	Quadratic voltage coefficient of capacitance	ppm/V^2
β	Linear voltage coefficient of capacitance	ppm/V
ε	Permittivity	F/cm^2
Φ_{bn}	Electron barrier height	eV
Φ_{bp}	Hole barrier height	eV
Φ_{Si}	Work function of Si substrate	eV

Φ_m	Work function of metal gate	eV
ρ	Resistivity	$\mu\Omega\cdot cm$
κ	Relative dielectric constant	none

Chapter 1

Introduction

As the author is typing this thesis, the ITRS (International Technology Roadmap for Semiconductors) Summer Public Conference is being held during SEMICON West. New materials and devices are being investigated to extend CMOS. In CMOS technology development, new materials, such as high-κ and low-κ dielectric, metal gate, stressors and new silicide materials have played and will continue to play an important role.

Lanthanoid elements and their compounds, which have widely been used in lasers, catalysts, magnets, glass and ceramics, are strategic materials for several major industry areas, including the military weapons. They have become more important in microelectronics as the demand for performance cannot be fulfilled by existing materials. This chapter would discuss the characteristics of lanthanoid elements and their potential to address the challenges in the silicon CMOS technology.

1.1 Lanthanoid Elements and Their Compounds

1.1.1 The Lanthanoid Series

Lanthanoid elements are the 15 elements of the Periodic Table (La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu) with the atomic numbers from 57 through 71 (Table 1.1). The lanthanoid series (Ln) is named after lanthanum. Lanthanoids are sometimes referred to as the "rare earths", which is used to describe all the lanthanoids together with scandium (Sc) and yttrium (Y). The use of this name is deprecated by International Union of Pure and Applied Chemistry (IUPAC), as they are neither rare in abundance nor "earths" (an obsolete term for water-insoluble oxides of electropositive metals incapable of being smelted into metal using late 18th century technology). These elements are in fact fairly abundant in nature, although rare as compared to the "common" earths such as lime or magnesia. IUPAC currently recommends the name *lanthanoid* rather than *lanthanide*, as the suffix "-ide" generally indicates negative ions whereas the suffix "-oid" indicates similarity to one of the members of the containing family of elements. In the older literature, the name *lanthanon* was often used.

Lanthanoids are chemically similar to each other and closely resemble the first element in the series - La. The lanthanoids occur as trivalent cations in nature except for cerium (Ce) and europium (Eu). An important feature is that they all have low work function, ranging from 2.59 eV (Yb) to 3.3 eV (La). The photoelectric work functions of all lanthanoid elements are listed in Table 1.1.

Table 1.1. List of lanthanoid elements, photoelectric work functions [2], and ionic radii of the trivalent lanthanoid ions [1].

Atomic No.	57	58	59	60	61	62	63	64
Symbol	La	Ce	Pr	Nd	Pm	Sm	Eu	Gd
Work function	3.3	2.7	2.7	3.3	-	3.2	2.54	3.07
Ln^{3+} radii (nm)	0.123	0.115	0.114	0.112	-	0.106	0.106	0.104
Atomic No.	65	66	67	68	69	70	71	
Name	Tb	Dy	Ho	Er	Tm	Yb	Lu	
Work function	3.09	3.09	3.09	3.12	3.12	2.59	3.15	
Ln^{3+} radii (nm)	0.100	0.099	0.098	0.096	0.094	0.093	0.092	

In the outer electronic configuration of the lanthanoid series, the $6s^2$ shell is always occupied, the $5d^1$ configuration appears in La, Ce, Gd and Lu, and then the $4f$ shell is progressively filled as the atomic number increases. The number of electrons in the $4f$ shell is therefore the distinctive characteristic of the lanthanoid elements. The $4f$ sub-shell lies inside the ion, shielded by the $5s^2$ and $5p^6$ closed sub-shells. The ionic radii of the lanthanoids decrease through the period - the so-called lanthanide contraction – from 0.123 nm in La to 0.092 nm in Lu [1].

1.1.2 Lanthanoid Silicides

Metal silicide thin films are commonly used in ohmic contacts, MOS gate electrodes, and silicidation of diffusion regions. Silicides of platinum (Pt), tungsten

(W), titanium (Ti), cobalt (Co), nickel (Ni), tantalum (Ta) and other metals have been heavily investigated, and some of them are now commonly used in manufacturing. The lanthanoid silicides are relatively new to CMOS processing technology, but their low work function and low Schottky barrier to the n-type silicon [3] have made them attractive in the development of new infrared detectors, work function tuning in FUSI metal gate [4] and Schottky source/drain transistors [5, 6].

The lanthanoid disilicides ($LnSi_2$) are a large group among the lanthanoid silicides. However, the perfect stoichiometry of 1:2 is not commonly seen in thin silicide films. The silicon atoms behave like interstitials and the silicon sublattice in the silicide usually contain vacancies. The actual compositions vary between 1:1.66 and 1:1.85, especially for heavy lanthanoid silicides from Gd to Lu [7-9]. Lanthanoid disilicides with silicon vacancies are usually denoted as $LnSi_{2-x}$.

The most common method for forming lanthanoid silicide thin films is by depositing a thin layer of the metal onto clean silicon surface by Physical Vapor Deposition (PVD), which includes e-beam evaporation and sputtering; the silicide is then formed by annealing either in furnace or in RTP. The reactions of lanthanoid silicides show remarkably different growth kinetics from those observed in the formation of other transition metal silicides. By annealing lanthanoid metal on Si substrates, it has been shown that Si atoms are the dominant diffusing species during the silicide formation [10, 11]. It is generally accepted that the mechanism of lanthanoid silicide thin film formation is dominated by nucleation phenomena. The solid state interactions between lanthanoid and silicon exhibit a critical temperature. Below the critical temperature, reactions are very sluggish; while above this temperature, reaction is fast. For La, it was found that although the reaction starts from as low as 200 ℃, the disilicide phase $LaSi_2$ does not form until 600 ℃ [12, 13].

This suggests an intermediate stage of formation of $LaSi_{2-x}$ [13]. As lanthanoid metals are chemically reactive, the oxidation of the lanthanoid elements must be prevented during the formation of silicides.

1.1.3 Lanthanoid Oxides

Lanthanoid metals react with oxygen vigorously and form oxides [14]. These oxides are thermally stable. In the solid state, the +3 oxidation state (Ln_2O_3) is generally the stable one for the lanthanoid elements in the solid state. This is advantageous because, when one element has more than one stable oxidation state, more than one stoichiometry is possible which, in turn, could lead to a complicated band structure [15]. Some lanthanoid elements are also stable in the oxidation state +2 (Sm, Eu, Tb, and Yb), and others in the oxidation state +4 (Ce, Pr, Tb) [16, 17]. Two issues of major concern in microelectronics are the dielectric constant (κ) and the energy gap (E_g).

The κ value of a dielectric is related to frequencies of its dominant infrared optical modes [18], which in turn are related to the crystalline structure. The κ value is higher for crystalline films with structures having the most intense absorption band at lower frequencies. Lanthanoid oxides with the same chemical composition but different crystal structures may have different dielectrics constants. For a insulator in microelectronic devices, larger energy gap is desired for larger capacitance density. The reported κ values of lanthanoid oxides are listed in Table 1.2. All the lanthanoid oxides are considered high-κ since their κ values are larger than that of SiO_2 (~3.9). The deviation of actual κ values of the same lanthanoid oxide but different sources are ascribed to deposition method, thickness, purity, oxygen vacancies and some other aspects [19-24].

Table 1.2. Summary of dielectric constant κ values of lanthanoid oxides.

Oxide	**κ (bulk)**	**κ (thin film)**
La_2O_3	30 [25]	19 [21], 23 [20], 30 [25]
Ce_2O_3	16.6	26 [24], 52 [19]
Pr_2O_3	14.9	15 [23], 30 [22]
Nd_2O_3	14.3-16	11.7 [26]
Sm_2O_3	-	10 [27], 30.5 [28]
Eu_2O_3	13.7	12 [29]
Gd_2O_3	13.6	16 [30] , 23 [31]
Tb_2O_3	13.3	-
Dy_2O_3	13.1	-
Ho_2O_3	13.1	-
Er_2O_3	13	7 – 14 [32]
Tm_2O_3	12.6	7 – 22 [33]
Yb_2O_3	12-13.4	12 , 14[20]
Lu_2O_3	12.5	11 [34]

κ values for the bulk dielectrics are from [35].

The energy gap (E_g) of the lanthanoid oxide series varies in a periodic way with the increasing atomic number. The optically measured E_g values shown in Fig. 1.1 show this trend. The electrically measured E_g values from high-temperature conductivity experiments [36] are also presented. The electrically measured energy gaps are lower than optically measured ones, but the two trends agree with each other. The oxide of La, Gd, and Lu have the largest E_g (~ 5.5 eV). Ce, Pr and Tb have significantly lower energy gaps (2.3 eV, 3.9 eV, and 3.8 eV, respectively). The periodic E_g values are believed to be due to the gradual increase of *f* shell electrons [36-38].

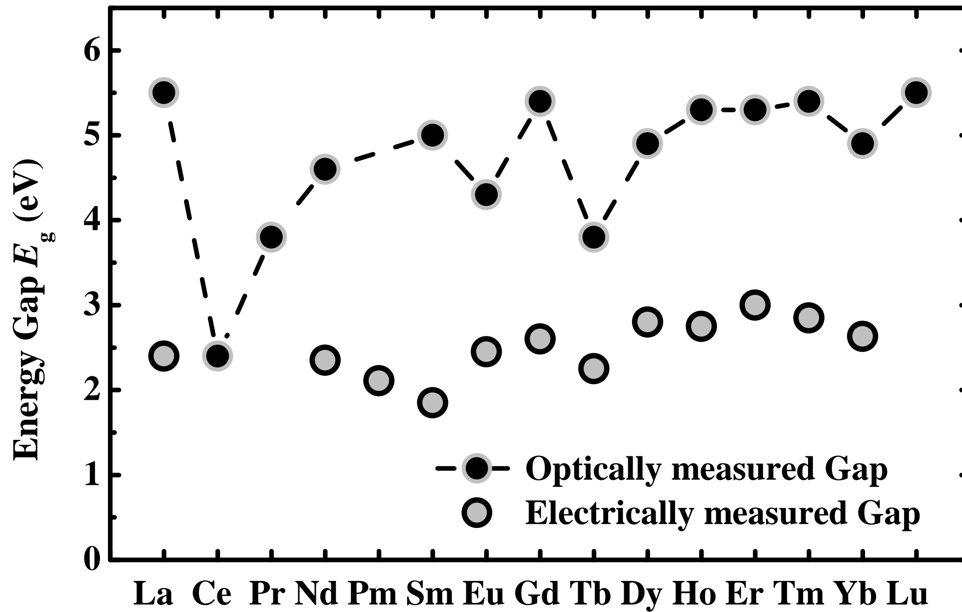

Fig. 1.1. Energy gap of Ln_2O_3 oxides. The optical gap data is from collected from [38]. The electrical gap derived from high temperature conductivity measurements are from [36].

Although lanthanoid oxides are thermally stable, they are known to react with water [39-41]. This reactivity decreases as the ionic radius of the lanthanoid element decreases [41]. This can be verified from the analysis of the XPS O 1*s* spectra. Special caution should be taken when handling lanthanoid oxides to reduce exposure to water or the moisture in air.

1.2 Integrated Circuit Scaling

1.2.1 Transistor Scaling

The exponential increase in transistor density IC [42] has lasted for half a century. This has been predominantly achieved through conventional transistor scaling based on the criteria proposed by Dennard *et al.* [43]. Since the 1970's, the minimum feature size of transistors was reduced by a factor ~0.7 times in successive complementary metal-oxide-semiconductor (CMOS) technology nodes every 18

months. The increase in packing density per unit chip area for state-of-the-art IC's has improved speed and functionality. The transistors per chip have been increasing from 10^3 in year 1972 to more than 10^9 in today's leading-edge technology, as shown in Fig. 1.2. However, as the technology advances into sub-32 nm regime, fundamental physical limitations of transistor scaling are met. Aggressively-scaled transistors lead to high leakage currents that lead to unacceptable power consumption and performance degradation. Hence, it is imperative to review these challenges and consider other alternative technological solutions for continued development in future generation nodes.

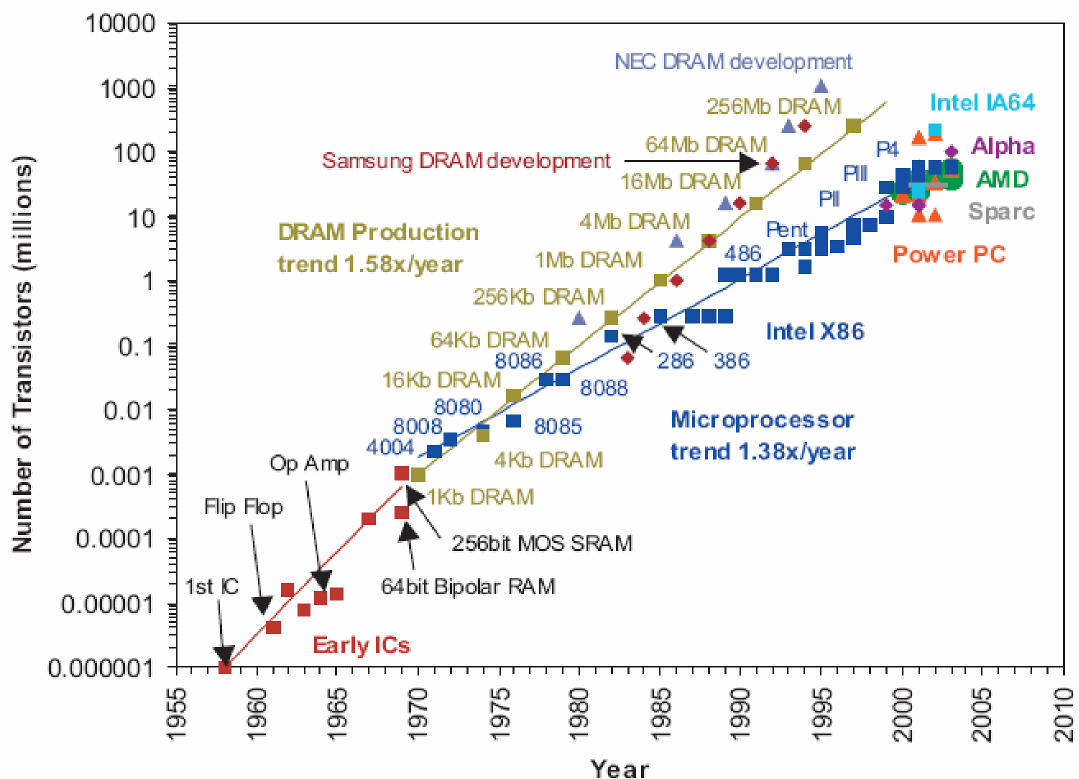

Fig. 1.2. The number of transistors on integrated circuits such as microprocessors and DRAM increases exponentially over the years [44].

Table 1.3. Specifications for the scaling of transistors, derived from *ITRS* 2008 [42]

Year of Production	**2007**	**2009**	**2011**	**2013**	**2015**
Technology node/ DRAM half Pitch (nm)	68	52	40	32	25
Physical gate length for MPU/ASIC (nm)	32	27	22	18	15
EOT for MPU (nm)	1.1	1	0.88	0.65	0.53
Gate leakage at 100°C for high performance (A/cm^2)	180	650	900	1100	1300
Metal gate work function for MPU/ASIC $\left\|E_{C,V} - \Phi_m\right\|$ (eV)	-	< 0.2	< 0.2	< 0.2	< 0.2
Channel doping for bulk (10^{18} cm^{-3})	3.70	4.71	3.77	5.40	7.19
Extension lateral abruptness for bulk (nm)	3.5	2.8	2.3	1.8	1.5
Contact X_j for bulk (nm)	35.2	29	24.7	19.8	16.9
Allowable junction leakage for MPU/ASIC (μA/μm)	0.06	0.25	0.71	0.64	0.72
Contact silicide sheet resistance for MPU (Ω/□)	-	-	-	7.4	8.7

The International Technology Roadmap for Semiconductors (ITRS) has been developed as a guideline to identify key technical requirements and imminent technological challenges faced by the semiconductor industry [42]. Table 1.3 shows some of the projected specifications for the scaling of transistors from 2007 to 2015. Short channel effect (SCE) can be suppressed by doping the channel heavily, but this leads to mobility degradation, high junction leakage and stochastic doping variations

which compromise the benefit from a shorter channel. Metal gate, high-κ dielectric and multi-gate transistors are proposed for stronger gate control. Ultra-shallow junctions and ultra-thin body fully depleted silicon-on-insulator (SOI) can effectively reduce the junction leakage and improve the subthreshold behavior.

A. Source/Drain Dopant and Contact

Ultra-shallow shallow junctions are required to suppress short channel effects. However a trade off exists between the sheet resistance, R_s and junction depth X_j. By reducing the thermal budget (e.g. the temperature and time) of the junction anneal, X_j can be lowered due to reduced diffusion. However, this normally deteriorates the activation of the implanted dopants, which increases R_s. The dose is already high. Increasing dose beyond the maximum solubility limit of depants does not help much. Therefore fabrication of ultra-shallow source/drain (S/D) with low series resistance is a bottleneck for future scaling of MOSFET.

Schottky barrier Source/Drain Transistor (SSDT) has been suggested as a potential solution to overcome this problem due to its abrupt silicide/Si interface and the low resistance of the silicide [6]. On top of that, it has also been reported that SSDT is able to suppress drain induced barrier lowering (DIBL) because of the fixed potential barrier at the source Schottky contact which offers an insensitive barrier to electric field from the drain and source [45, 46]. SSDT is also particularly attractive when a metal-gate/high-κ gate stack is employed as it avoids the use of a high–temperature annealing process required for activation of implanted S/D dopants. This eliminates thermal stability issues associated with high-κ gate stack. Lanthanoid elements, like other transition metals, form silicide when annealed with silicon. It is well known that the low work function metals such as lanthanoids usually have low

Schottky electron barrier height [47]. Lanthanoid silicides are potential candidates for N-type SSDT.

B.Gate Electrode

The polycrystalline silicon (poly-Si) depletion problem (Fig. 1.3) retards the scaling of the capacitance equivalent thickness (CET) of the gate stack in the inversion regime (CET_{inv}), which determines the drive current capability of MOSFET's [48]. The voltage drop across the gate depletion layer may lead to a reduction in the effective gate voltage and hence less inversion charges in the channel. Gate capacitance degradation due to the depletion of the doped poly-Si gate typically accounts for 0.4~0.5 nm in the CET_{inv} [49]. Therefore the performance improvement from the EOT reduction by using high-κ dielectric could be compromised by this poly-Si depletion problem. Although the depletion of poly-Si gate could be alleviated by using higher doping concentration in the n^+ and p^+ -doped poly-Si, dopant penetration (especially boron) could be another concern [50, 51]. Additionally, the continuous scaling in gate electrode thickness leads to high gate resistance for the poly-Si electrode, which would also degrade the over-all performance of transistors [52]. As a result, immense interests have been shown in metal gate technology.

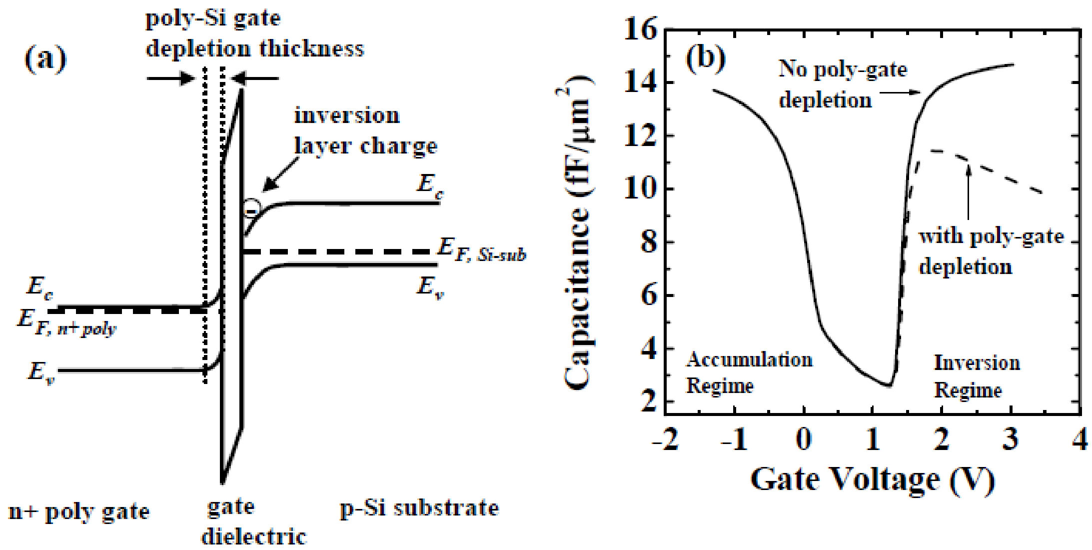

Fig. 1.3. (a) The energy band diagram of an NMOSFET showing the poly-Si gate depletion layer during inversion bias. (b) The capacitance-voltage plot depicts how the poly-Si gate depletion effect decreases the gate capacitance in the inversion regime. This figure is from reference [53].

Metal gate is expected to be introduced in the sub-45nm CMOS technology nodes to address the concerns associated with the poly-Si electrode. Fully-silicidation (FUSI) metal gate electrodes such as NiSi, $CoSi_2$ and $TiSi_2$ have been extensively studied due to the compatibility of FUSI process with CMOS process flow [54-56]. However, the optimization of the flatband and threshold voltage and the process integration for dual metal gate still need to be explored. Low work function lanthanoid elements are expected to be helpful in metal gate work function tuning.

C. Gate Dielectric

A direct method to control the short channel effect would be to reduce the gate dielectric thickness and to eliminate gate depletion to increase gate-to-channel capacitive coupling. At present, gate dielectric thickness has become so thin that gate leakage current densities due to direct tunneling of electrons are reaching unacceptable levels for logic technology, especially for high performance logic. High-

κ dielectrics have been proposed as an alternative to conventional silicon oxy-nitride dielectrics to suppress gate leakage, and the most promising candidate is hafnium-based dielectrics [25, 57]. The replacement of the conventional doped polysilicon gate with a metal gate electrode is also expected for integration with high-κ dielectrics. There has been a breakthrough in the implementation of metal gate/high-κ gate stack for CMOS devices in high volume production [58]. However, research on the flatband voltage modulation by high-κ material, physics at the high-k/Si interface, and gate stack reliability are still going on. The potential application of lanthanoid oxide as a high-κ dielectric will be discussed in Chapter 4.

1.2.2 Scaling of Integrated Passive Devices

The explosive growth of the wireless communications market has been served by radio frequency (RF)/mixed-signal (MS) chips, which includes RF, analog, analog-to-digital and digital-to-analog conversion, and a large number of mixed-signal chips. These chips deal with analog signals with high precision. On such circuits, passive devices usually occupy a large portion of the area. Therefore, scaling transistor dimensions alone is insufficient. However, passive devices for these applications have not shrunk in size as rapidly as active devices. Adding to the problem is the fact that increasing numbers of passive devices are required in modern wireless applications due to the larger fraction of analog signals involved [59].

Among the passive devices, capacitors occupy more area than the sum of the others, and they can be vastly affected by process engineering while the improvement in resistors and inductors are mainly done through design [60]. Fig. 1.4 shows the position of MIM capacitors in an mixed signal circuit. High capacitance density can be realized by reducing the thickness and/or increasing the permittivity κ of the MIM dielectric material.

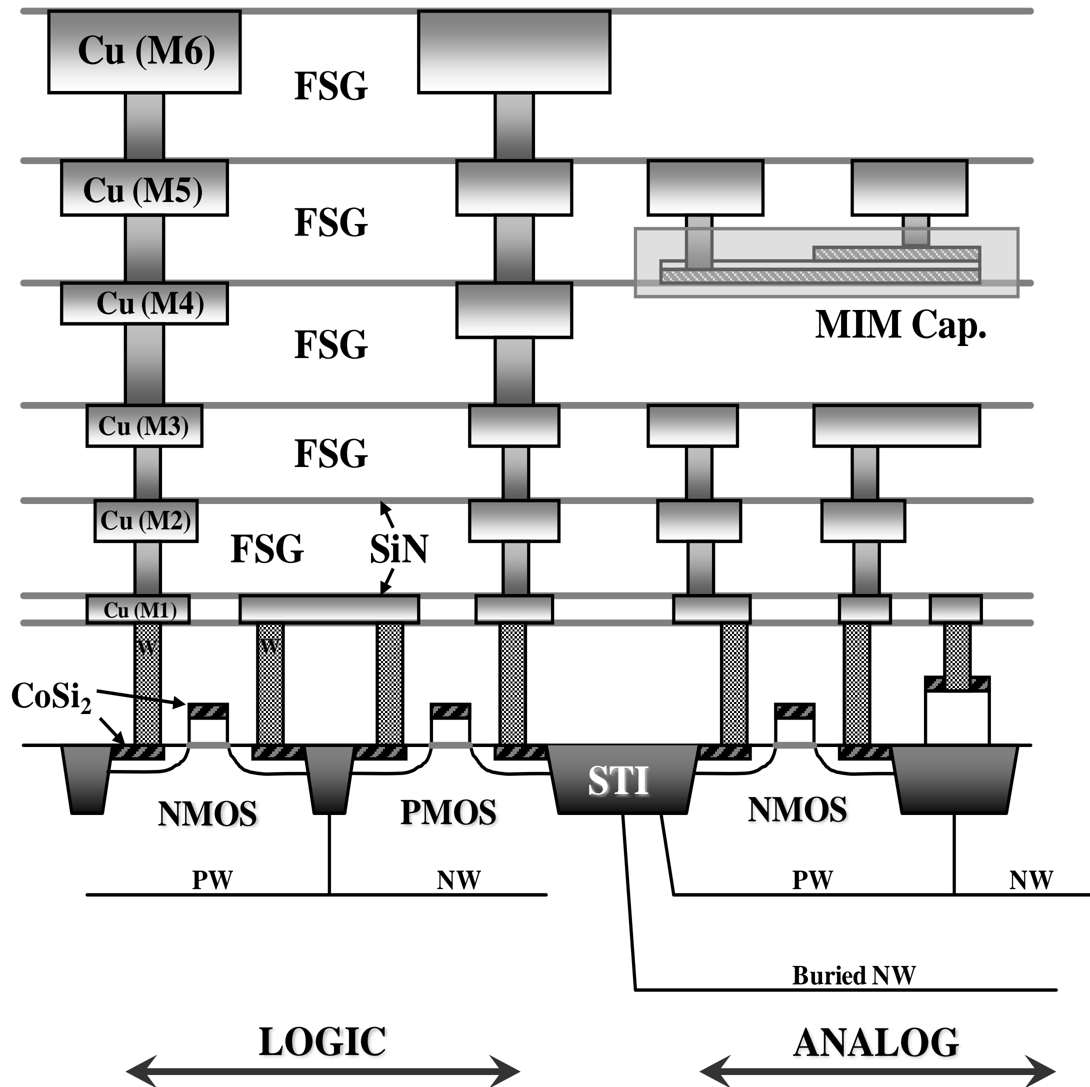

Fig. 1.4. Cross sectional view of digital-analog mixed-signal circuit, where MIM capacitor is integrated in the Cu back-end-of-the-line.

However, leakage current and reliability issues limit thickness scaling of the MIM dielectric. High-κ materials, which have been recently introduced to CMOS gate stack and DRAM cell [61], are also potential candidates for MIM dielectrics. However, other than the capacitance density, MIM capacitors for RF an MS circuits require special and stringent device specifications as shown in Table 1.4 [42]. For example, the voltage linearity requirement is 100 ppm/V^2 for precision RF/analog circuits, which is still a challenge for intensively studied high-κ materials such as HfO_2 [62, 63], Ta_2O_5 [64], and Al_2O_3 [65]. Much less progress has been done in

analog and RF circuit applications, where SiO_2 or Si_3N_4 based capacitors are still being used. Lanthanoid oxides, with κ values ranging from 7 to 30 (Table 1.2), are potential candidates for MIM applications. It has been reported that the voltage coefficient can be reduced by incorporating Tb, which is a lanthanoid element, into HfO_2 [66]. Tb_2O_3 itself was not studied because it is not an ideal high-κ material for its small energy gap (Fig. 1.1). Nevertheless, this thesis work shows that, at least some of the lanthanoid oxides might be suitable for realizing MIM capacitors with low VCC.

Table 1.4. Specifications for the scaling of MIM capacitors, derived from *ITRS* 2008 [42].

Year of Production	**2007**	**2009**	**2011**	**2013**	**2015**
Density (fF/μm^2)	2	4	5	7	7
Voltage linearity (ppm/V^2)	<100	<100	<100	<100	<100
Leakage (A/cm^2)	$<10^{-8}$	$<10^{-8}$	$<10^{-8}$	$<10^{-8}$	$<10^{-8}$
σ Matching (%·μm)	0.5	0.5	0.4	0.3	0.3
Q (5 GHz for 1pF)	>50	>50	>50	>50	>50

1.3 Objective of Research

The objective of this thesis is to explore novel lanthanoid based materials to address the challenges in the scaling down of CMOS transistors and MIM capacitors in modern silicon processing technology. Several areas, namely Schottky barrier source/drain transistor (SSDT), FUSI metal gate, high-κ dielectric for gate stack, and MIM capacitors with lanthanoid oxides have been extensively evaluated. This research contributes to the assessment of identification, and optimization of lanthanoid based materials for applications in advanced CMOS technology.

1.4 Thesis Organization

The main issues discussed in this thesis are documented in 4 chapters.

In **Chapter 2**, Schottky barrier source/drain transistor (SSDT) with $DySi_{2-x}$, $ErSi_{2-x}$, $TbSi_{2-x}$ and $YbSi_{2-x}$ as source/drain were investigated. The Schottky diode performance was studied by *J*-*V* measurements. The transistor characteristics were also compared. The process and integration issues are also discussed.

In **Chapter 3**, a novel Ni-FUSI gate work function tuning method using Yb-doped NiSi was demonstrated for the first time. Electrical and material analysis was conducted to ascertain the attractiveness of this Φ_m tuning technique. Additional insights were given for the application of the novel doping technique to attain band-edge Ni-FUSI gate Φ_m tunability in a gate-first process flow.

In **Chapter 4**, a comprehensive study of erbium (Er) doped HfO_2 for Φ_m tunability of TaN metal gate was performed. The dependence of metal gate Φ_m on the dosage of erbium was studied.

In **Chapter 5**, lanthanoid oxide based metal-insulator-metal capacitors for precision analog circuit were demonstrated for the first time.

Finally, the main contributions of this thesis are summarized in **Chapter 6**.

References

[1] Y. Sakabe, Y. Hamaji, H. Sano, and N. Wada, "Effects of rare-earth oxides on the reliability of X7R dielectrics," *Japanese Journal of Applied Physics. Pt. 1, Regular papers & short notes,* vol. 41, pp. 5668-5673, 2002.

[2] D. Lide, *CRC handbook of chemistry and physics: a ready-reference book of chemical and physical data*, CRC press, 2004.

[3] K. Tu and R. Thompson, "Low Schottky barrier of rare earth silicide on n-Si," *Applied Physics Letters,* vol. 38, pp. 626, 1981.

[4] J. Chen, H. Yu, M. Li, D. Kwong, M. van Dal, J. Kittl, A. Lauwers, P. Absil, M. Jurczak, and S. Biesemans, "Yb-doped Ni FUSI for the n-MOSFETs gate electrode application," *IEEE Electron Device Letters,* vol. 27, pp. 160-162, 2006.

[5] S. Zhu, H. Yu, J. Chen, S. Whang, J. Chen, C. Shen, C. Zhu, S. Lee, M. Li, and D. Chan, "Low temperature MOSFET technology with Schottky barrier source/drain, high-κ gate dielectric and metal gate electrode," *Solid State Electronics,* vol. 48, pp. 1987-1992, 2004.

[6] S. Zhu, J. Chen, M. Li, S. Lee, J. Singh, C. Zhu, A. Du, C. Tung, A. Chin, and D. Kwong, "N-type Schottky barrier source/drain MOSFET using ytterbium silicide," *IEEE Electron Device Letters,* vol. 25, pp. 565-567, 2004.

[7] R. Potttgen, R. Hoffmann, and D. Kubann, "The Binary Silicides Eu_5Si_3 and Yb_3Si_5-Synthesis, Crystal Structure, and Chemical Bonding," *Zeitschrift für anorganische und allgemeine Chemie,* vol. 624, pp. 945-951, 1999.

[8] S. Vandre, T. Kalka, C. Preinesberger, I. Manke, H. Eisele, M. Dähne-Prietsch, R. Meier, E. Weschke, and G. Kaindl, "Growth and electronic structure of dy silicide on Si (111)," *Applied Surface Science,* vol. 123, pp. 100-103, 1998.

[9] V. Koleshko, V. Belitsky, and A. Khodin, "Thin films of rare earth metal silicides," *Thin Solid Films,* vol. 141, pp. 277-285, 1986.

[10] J. Baglin and C. Petersson, "Diffusion marker experiments with rare earth silicides and germanides: Relative mobilities of the two atom species," *Journal of Applied Physics,* vol. 52, pp. 2841, 1981.

[11] A. Travlos, P. Aloupogiannis, G. Weber, and G. Robaye, "Diffusion marker experiments with rare earth silicides: The case of lutetium silicide," *Journal of Applied Physics,* vol. 70, pp. 7620, 1991.

[12] C. Hsu, Y. Wang, J. Hu, J. Ho, and J. Qian, "The effect of thermal treatment on the thin-film reaction of La, Ce, and Nd on silicon surfaces," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 7, pp. 3016, 1989.

[13] C. Hsu, J. Ho, J. Qian, Y. Wang, and Y. Wang, "Lanthanum Silicide Formation in Thin La--Si Multilayer Films," *Vacuum,* vol. 41, pp. 1425-1427, 1989.

[14] L. Eyring, *Synthesis of lanthanide and actinide compounds*, Netherland, 1991.

[15] G. Scarel, A. Svane, and M. Fanciulli, *Rare Earth Oxide Thin Films, Growth, Characterization, and Applications*, Springer, 2007.

[16] P. Villars and L. Calvert, *Pearson's Handbook of Crystallographic Data for Intermetallic Compounds*, American Society for Metals, 1991.

[17] J. Leger, N. Yacoubi, and J. Loriers, "Synthesis of rare earth monoxides," *Journal of Solid State Chemistry,* vol. 36, pp. 2, 1981.

[18] E. Bonera, G. Scarel, M. Fanciulli, P. Delugas, and V. Fiorentini, "Dielectric Properties of High- Oxides: Theory and Experiment for Lu_2O_3," *Physical Review Letters,* vol. 94, pp. 27602, 2005.

[19] Y. Nishikawa, T. Yamaguchi, M. Yoshiki, H. Satake, and N. Fukushima, "Interfacial properties of single-crystalline CeO high-κ gate dielectrics directly grown on Si (111)," *Applied Physics Letters,* vol. 81, pp. 4386, 2002.

[20] S. Ohmi, C. Kobayashi, I. Kashiwagi, C. Ohshima, H. Ishiwara, and H. Iwai, "Characterization of LaO and YbO Thin Films for High-k Gate Insulator Application," *Journal of The Electrochemical Society,* vol. 150, pp. F134, 2003.

[21] H. Yamada, T. Shimizu, A. Kurokawa, K. Ishii, and E. Suzuki, "MOCVD of high-dielectric-constant lanthanum oxide thin films," *Journal of The Electrochemical Society,* vol. 150, pp. G429, 2003.

[22] A. Fissel, H. Osten, and E. Bugiel, "Towards understanding epitaxial growth of alternative high-K dielectrics on Si (001): Application to praseodymium oxide," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 21, pp. 1765, 2003.

[23] K. Kukli, M. Ritala, T. Pilvi, T. Sajavaara, M. Leskela, A. Jones, H. Aspinall, D. Gilmer, and P. Tobin, "Evaluation of a praseodymium precursor for atomic layer deposition of oxide dielectric films," *Chem. Mater,* vol. 16, pp. 5162-5168, 2004.

[24] L. Tye, N. El Masry, T. Chikyow, P. McLarty, and S. Bedair, "Electrical characteristics of epitaxial CeO on Si (111)," *Applied Physics Letters,* vol. 65, pp. 3081, 1994.

[25] J. Robertson, "High dielectric constant gate oxides for metal oxide Si transistors," *Reports on Progress in Physics,* vol. 69, pp. 327-396, 2006.

[26] A. Dakhel, "Characterisation of Nd_2O_3 thick gate dielectric for silicon," *Physica Status Solidi (a),* vol. 201, pp745-755, 2004.

[27] J. Paivasaari, M. Putkonen, and L. Niinisto, "A comparative study on lanthanide oxide thin films grown by atomic layer deposition," *Thin Solid Films,* vol. 472, pp. 275-281, 2005.

[28] H. Yang, H. Wang, H. M. Luo, D. M. Feldmann, P. C. Dowden, R. F. DePaula, and Q. X. Jia, "Structural and dielectric properties of epitaxial Sm_2O_3 thin films," *Applied Physics Letters,* vol. 92, pp. 062905-3, 2008.

[29] M. Singh, K. Shalini, S. Shivashankar, G. Deepak, N. Bhat, and T. Shripathi, "Microstructure, crystallinity, and properties of low-pressure MOCVD-grown europium oxide films," *Materials Chemistry & Physics,* vol. 110, pp. 337-343, 2008.

[30] D. Landheer, J. Gupta, G. Sproule, J. McCaffrey, M. Graham, K. Yang, Z. Lu, and W. Lennard, "Characterization Of Gd_2O_3 Films Deposited On Si (100) By E-beam Evaporation From Pressed-Powder Targets," *Low and High Dielectric Constant Materials: Materials Science, Processing, and Reliability Issues: Proceedings of the Fifth International Symposium,* pp. 172-174, 2000.

[31] M. Singh, C. Thakur, K. Shalini, S. Banerjee, N. Bhat, and S. Shivashankar, "Structural, optical, and electrical characterization of gadolinium oxide films deposited by low-pressure metalorganic chemical vapor deposition," *Journal of Applied Physics,* vol. 96, pp. 5631, 2004.

[32] V. Mikhelashvili, G. Eisenstein, F. Edelman, R. Brener, N. Zakharov, and P. Werner, "Structural and electrical properties of electron beam gun evaporated Er_2O_3 insulator thin films," *Journal of Applied Physics,* vol. 95, pp. 613, 2004.

[33] T. Zdanowicz, "Preparation and some electrical properties of thulium oxide films," *Thin Solid Films,* vol. 58, pp. 390, 1979.

[34] S. Ohmi, M. Takeda, H. Ishiwara, and H. Iwai, "Semiconductor Devices, Materials, and Processing-Electrical Characteristics for Lu_2O_3 Thin Films Fabricated by E-Beam Deposition Method," *Journal of The Electrochemical Society,* vol. 151, pp. 279, 2004.

[35] R. Shannon, "Dielectric polarizabilities in oxides and fluorides," *Journal of Applied Physics,* vol. 73, pp. 348-366, 1993.

[36] H. Lal and K. Gaur, "Electrical conduction in non-metallic rare-earth solids," *Journal of Materials Science,* vol. 23, pp. 919-923, 1988.

[37] L. Petit, A. Svane, Z. Szotek, and W. Temmerman, "First-principles study of rare-earth oxides," *Physical Review B,* vol. 72, pp. 205118, 2005.

[38] A. V. Prokofiev, A. I. Shelykh, and B. T. Melekh, "Periodicity in the band gap variation of Ln_2X_3 (X = O, S, Se) in the lanthanide series," *Journal of Alloys and Compounds,* vol. 242, pp. 41-44, 1996.

[39] S. Guha, E. Cartier, M. Gribelyuk, N. Bojarczuk, and M. Copel, "Atomic beam deposition of lanthanum-and yttrium-based oxide thin films for gate dielectrics," *Applied Physics Letters,* vol. 77, p. 2710, 2000.

[40] Y. Zhao, M. Toyama, K. Kita, K. Kyuno, and A. Toriumi, "Moisture Absorption-Induced Permittivity Deterioration and Surface Roughness Enhancement of Lanthanum Oxide Films on Silicon," *Solid State Devices And Materials,* vol. 2005, pp. 546, 2005.

[41] S. Jeon and H. Hwang, "Effect of hygroscopic nature on the electrical characteristics of lanthanide oxides (Pr_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3)," *Journal of Applied Physics,* vol. 93, pp. 9, 2003.

[42] International Technology Roadmap for Semiconductors 2008, www.itrs.net.

[43] R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions " *IEEE Journal of Solid-State Circuits*, vol. 9, pp. 256-268, 1974.

[44] Source: *Intel Corporation*.

[45] J. Kedzierski, P. Xuan, E. H. Anderson, J. Bokor, T. J. King, and C. Hu, "Complementary silicide source/drain thin-body MOSFETs for the 20nm gate length regime," *Technical Digest - International Electron Devices Meeting,* pp. 57-59, 2000.

[46] M. Nishisaka, S. Matsumoto, and T. Asano, "Schottky source/drain SOI MOSFET with shallow doped-extension," *International Conference on Solid-State Devices and Materials,* pp. 586-587, 2002.

[47] R. T. Tung, "Electron transport at metal-semiconductor interfaces: General theory," *Physical Review B,* vol. 45, pp. 13509-13523, 1992.

[48] S. Wolf, *Silicon Processing for the VLSI Era, Volume 4-Deep-submicron process technology, chapter 15. Sunset Beach*, Lattice Press, 2002.

[49] H. Wong and S. Philip, "Beyond the conventional transistor," *IBM Journal of Research and Development,* vol. 46, pp. 133-168, 2002.

[50] T. Morimoto, H. Momose, Y. Ozawa, K. Yamabe, and H. Iwai, "Effects of boron penetration and resultant limitations in ultrathin pure-oxide and nitrided-oxide gate-films," 1990, pp. 429-432.

[51] K. Onishi, L. Kang, R. Choi, E. Dharmarajan, S. Gopalan, Y. Jeon, C. Kang, B. Lee, R. Nieh, and J. Lee, "Dopant penetration effects on polysilicon gate HfO_2 MOSFET's," *Symposium on VLSI Technology Tech. Dig,* pp. 131-132, 2001.

[52] H. Iwai, T. Ohguro, and S.-i. Ohmi, "NiSi salicide technology for scaled CMOS," *Microelectronic Engineering,* vol. 60, pp. 157-169, 2002.

[53] Y.-C. Yeo, T.-J. King, and C. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology," *Journal of Applied Physics,* vol. 92, pp. 7266-7271, 2002.

[54] W. Maszara, Z. Krivokapic, P. King, J. Goo, and M. Lin, "Transistors with dual work function metal gates by single full silicidation (FUSI) of polysilicon gates," *International Electron Devices Meeting Tech. Dig.*, pp. 367-370, 2002.

[55] B. Tavel, T. Skotnicki, G. Pares, N. Carriere, M. Rivoire, F. Leverd, C. Julien, J. Torres, and R. Pantel, "Totally Silicided ($CoSi_2$) Polysilicon: A Novel Approach to Very Low-Resistive Gate (~ 2Ω) Without Metal CMP Nor Etching," *International Electron Devices Meeting Tech. Dig.*, pp. 825-830, 2001.

[56] D. Yu, C. Wu, C. Huang, A. Chin, W. Chen, C. Zhu, M. Li, and D. Kwong, "Fully silicided NiSi and germanided NiGe dual gates on SiO/sub 2/n-and p-MOSFETs," *IEEE Electron Device Letters,* vol. 24, pp. 739-741, 2003.

[57] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," *Journal of Applied Physics,* vol. 89, pp. 5243-5275, 2001.

[58] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, and R. Chau, "A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," *International Electron Devices Meeting Tech. Dig.*, p. 247, 2007.

[59] R. Ulrich, W. Brown, S. Ang, F. Barlow, A. Elshabini, T. Lenihan, H. Naseem, D. Nelms, J. Parkerson, and L. Schaper, "Getting aggressive with passive devices," *IEEE Circuits and Devices Magazine,* vol. 16, pp. 16-25, 2000.

[60] J. Burghartz and B. Rejaei, "On the design of RF spiral inductors on silicon," *IEEE Transactions on Electron Devices,* vol. 50, pp. 718-729, 2003.

[61] D. Kik, K. Hong, K. Lee, J. Kim, H. Song, K. Park, J. Roh, H. Sohn, J. Kim, and S. Park, "Development of highly robust nano-mixed $Hf_xAl_yO_z$ dielectrics for TiN/$Hf_xAl_yO_z$/TiN capacitor applicable to 65 nm generation DRAMs," *Symposium on VLSI Technology Tech. Dig.,* pp. 126-127, 2004.

[62] H. Hu, C. Zhu, Y. Lu, M. Li, B. Cho, and W. Choi, "A high performance MIM capacitor using HfO_2 dielectrics," *IEEE Electron Device Letters,* vol. 23, pp. 514-516, 2002.

[63] X. Yu, C. Zhu, H. Hu, A. Chin, M. Li, B. Cho, D. Kwong, P. Foo, and M. Yu, "A high-density MIM capacitor (13 fF/μm^2) using ALD HfO_2 dielectrics," *IEEE Electron Device Letters,* vol. 24, pp. 63-65, 2003.

[64] T. Remmel, R. Ramprasad, and J. Walls, "Leakage behavior and reliability assessment of tantalum oxide dielectric MIM capacitors," *Reliability Physics Symposium Proceedings*, pp. 277-281, 2003.

[65] Y. L. Tu, H. L. Lin, L. L. Chao, D. Wu, C. S. Tsai, C. Wang, C. F. Huang, C. H. Lin, and J. Sun, "Characterization and Comparison of High-k Metal-Insulator-Metal (MiM) Capacitors in 0.13 m Cu BEOL for Mixed-Mode and RF Applications," *Symposium on VLSI Technology Tech. Dig.*, pp. 79-80, 2003.

[66] S. Kim, B. Cho, M. Li, C. Zhu, A. Chin, and D. Kwong, "HfO_2 and lanthanide-doped HfO_2 MIM capacitors for RF/mixed IC applications," *Symposium on VLSI Technology Tech. Dig.*, pp. 77-78, 2003.

Chapter 2

Schottky Barrier Source/Drain Field-Effect Transistor

2.1 Background and Theories

2.1.1 Motivation for Schottky Barrier Source/Drain Transistors

The series resistance contributed by ultra-shallow source/drain (S/D) junctions is a serious performance bottleneck for future CMOS transistor. The Schottky barrier Source/Drain field-effect Transistor (SSDT) architecture [1] has been proposed to overcome the series resistance problem of ultra-shallow source/drain (S/D) junctions in sub-50 nm MOSFETs [2-4], due to the abrupt silicide/Si interface and low resistance of silicide. SSDT is particularly attractive when a metal-gate/high-κ gate stack is employed, as it avoids the use of a high-temperature annealing process required for activation of implanted S/D dopants, hence, eliminating the thermal stability issues associated with high-κ gate stack [5]. Table 2.1 summarizes the features, advantages, and benefits of the SSDT technology.

Table 2.1. Summary of the features, advantages and benefits of the Schottky source/drain transistor technology.

Feature	**Advantage**	**Benefit**
2-3 fewer masks (S/D implant)	Simpler process	Lower cost, higher yield
Atomically abrupt junction	Scalability	Lower cost, higher speed, lower power
Low resistivity S/D contacts	Reduced parasitic series resistance	Higher speed, lower power
Low temperature S/D formation	Reduced thermal budget	Easier integration with high-κ dielectric, metal gates, strained Si, and other new materials
Lower channel implant concentration	Less channel impurity scattering	Higher effective carrier mobility
No shallow-implants	Simpler process	Lower cost
Schottky barrier at drain-to-body junction	Built-in barrier for drain-to-body leakage	Greater control of I_{off}, deeper S/D junctions allowed
Theoretical parasitic bipolar gain < 0.001	Elimination of latch-up, reduced soft-error rate	Simpler circuit design, improved IC reliability

Achieving low barrier height is a key issue for SSDT. P-channel SSDT (P-SSDT) with PtSi as Schottky S/D (hole barrier $\Phi_{bp} = 0.24 \sim 0.28\ eV$) has been fabricated with acceptable electrical performance with a I_{on}/I_{off} ratio of ~10^8 [6, 7] and a sub-threshold slope of 66 mV/decade [6]. However, the electrical performance of N-channel SSDT (N-SSDT) is still inferior mainly due to lack of suitable silicide material [4, 6, 8].

2.1.2 Schottky Barrier and Metal Work Function

The Schottky barrier (Φ_b) is the rectifying barrier for electrical conduction across the metal-semiconductor (MS) junction. It is of vital importance to the successful operation of Schottky diodes and SSDT. Ideally, Φ_b is equal to the difference between the metal work function Φ_b and the electron affinity of the semiconductor (Schottky-Mott theory) [9]. However, Fermi level pinning due to the large density of surface states present on the semiconductor surface makes Φ_b insensitive to the metal work function [10]. Fermi level pinning is closely related to the orientation/structure of the MS interface and the preparation of the semiconductor surface. Nevertheless, metals with lower work function have been found to have systematically lower Schottky barriers.

As discussed in Chapter 1, lanthanoids have lower photoelectric work function than most of the other transition metals. It is well known that the low work function metals usually have low Schottky electron barrier height [11]. In this chapter, we discuss the fabrication and characterization of SSDT with various lanthanoid silicides as S/D, namely $DySi_{2-x}$, $ErSi_{2-x}$, $TbSi_{2-x}$ and $YbSi_{2-x}$. The photoelectric work function of Dy, Er, Tb and Yb are 3.09 eV, 3.12 eV, 3.09 eV and 2.59 eV, respectively [12]. Yb silicide is expected to have a lower Schottky barrier height for electron.

2.1.3 Schottky Barrier Extraction

The Schottky barrier can be derived from current-voltage (*I-V*), current-temperature (*I-T*), capacitance-voltage (*C-V*), or photo current methods (*PC*) [13]. Any damage at the interface affects the *I-V* behavior because defects may act as recombination centers or intermediate states for trap-assisted tunneling currents. *C-V* measurements are less prone to such defects. However, defects can alter the space-

charge region width and hence the intercept voltage. Photocurrent measurement is less sensitive to such defects, and this method is judged to be most reliable [13]. Both the Schottky barrier height and the interfacial defects are important factors that affect the on-state current (I_{on}) and off-state current (I_{off}) of SSDT. As far as the SSDT performance is concerned, the *I-V* method is preferable for evaluation of the Schottky junction quality. We used both *I-V* and *C-V* methods to extract the barrier height. The *C-V* method used was the same as that discussed in [13]. For the *I-V* method, we employed a model to incorporate the series resistance to improve the accuracy, as discussed below.

The equivalent circuit of a real Schottky diode can be approximated as a perfect Schottky diode (no resistance), connected in series with a resistor. The series resistance comes from the top silicide and the silicon substrate. The thermionic current-voltage relationship of a Schottky barrier diode [14], neglecting series and shunt resistance, is given by

$$I = AA^{*}T^{2}\exp\left(\frac{-q\Phi_{b}}{kT}\right)\left(\exp\left(\frac{qV_{diode}}{nkT}\right)-1\right), \tag{2.1}$$

where A is the area of the Schottky junction, A^{*} is the Richardson constant, n is the ideality factor, T is the temperature (in Kelvin), q is the magnitude of electron charge (1.60×10^{-19} C), k is the Boltzmann's constant (8.61760×10^{-5} eV/K), and V_{diode} is the voltage drop on the Schottky barrier diode. For n-Si, $A^{*}=112\ \text{A/cm}^{2}\cdot\text{K}^{2}$,and for p-Si, $A^{*}=32\ \text{A/cm}^{2}\cdot\text{K}^{2}$ [15].

The voltage V_{R} across the resistor in series can be expressed as

$$V_{\text{R}} = V_{\text{bias}} - V_{\text{diode}}, \tag{2.2}$$

where

$$V_{\text{R}} = I\times R. \tag{2.3}$$

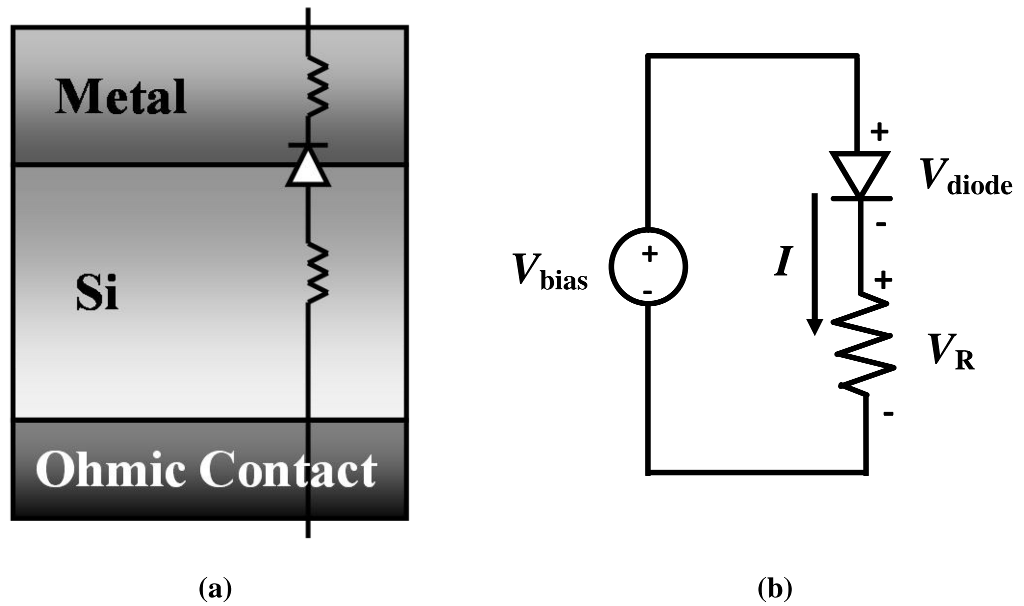

Fig. 2.1. (a) Schottky diode structure. (b) Equivalent circuit of Schottky diode. The resistances from the top electrode and bottom Si substrate are considered as one resistor.

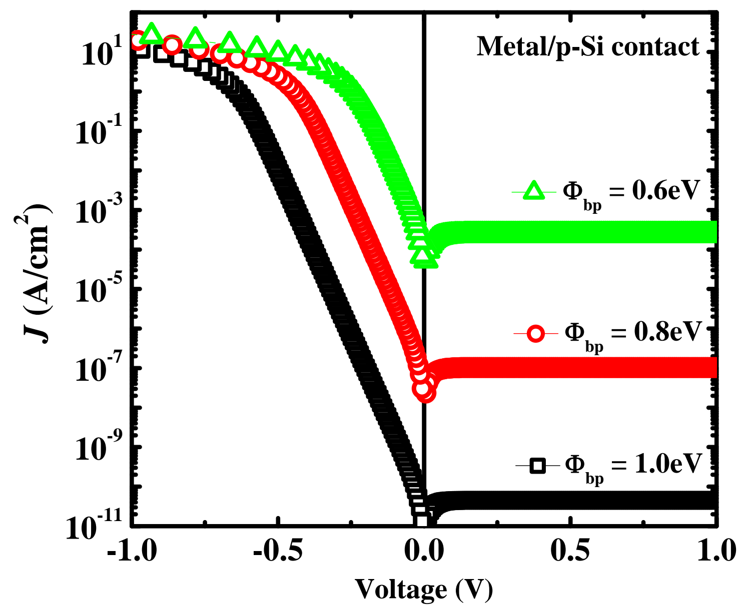

Fig. 2.2. Simulated *J-V* curves of metal/p-Si Schottky contact with an electron barrier of 0.6 eV, 0.8 eV and 1.0 eV. The series resistance is assumed to be 80 Ω.

Fig. 2.2 shows the simulated *J-V* curve of a Schottky junction in series with a 80-Ω resistor using Equation 2.1~2.3. For the reverse biased region (positive bias), the current is almost constant with increasing reverse bias voltage. The reverse current increases with decreasing electron barrier. For the forward bias region, the current increases linearly in the log scale at lower voltage, and the current reduces with the increase of electron barrier height. The slope at low negative bias is determined by the ideality factor n, but it changes at higher negative voltage region because of the series resistance. As the bias increases, the dynamic resistance of the Schottky barrier becomes smaller, and the series resistance becomes the dominant factor in the total resistance.

2.1.4 SSDT Structure and Principles of Operation

A comparison of schematic representation and operating principles of conventional N-MOSFET and N-SSDT devices is shown in Fig. 2.3. The principle innovation of SSDT is in the engineering of the source and drain electrodes. The conventional impurity-doped source/drain electrodes are entirely replaced by metal, which is typically self-aligned metal silicide (salicide). The different nature of the junction between the S/D regions and the semiconductor substrate leads to the different fundamental principles of operation.

For SSDT, the emitted current at the source is the sum of the current emission over the barrier and through the barrier. The thermal-emission current can be determined by classical thermal-emission (T-E) theory (equation 2.1).When a low electric field (E-field) is present at the source electrode, there is virtually no field-emission current. As the E-field increases at the source, the field emission current increases rapidly, while the thermal emission current remains approximately constant.

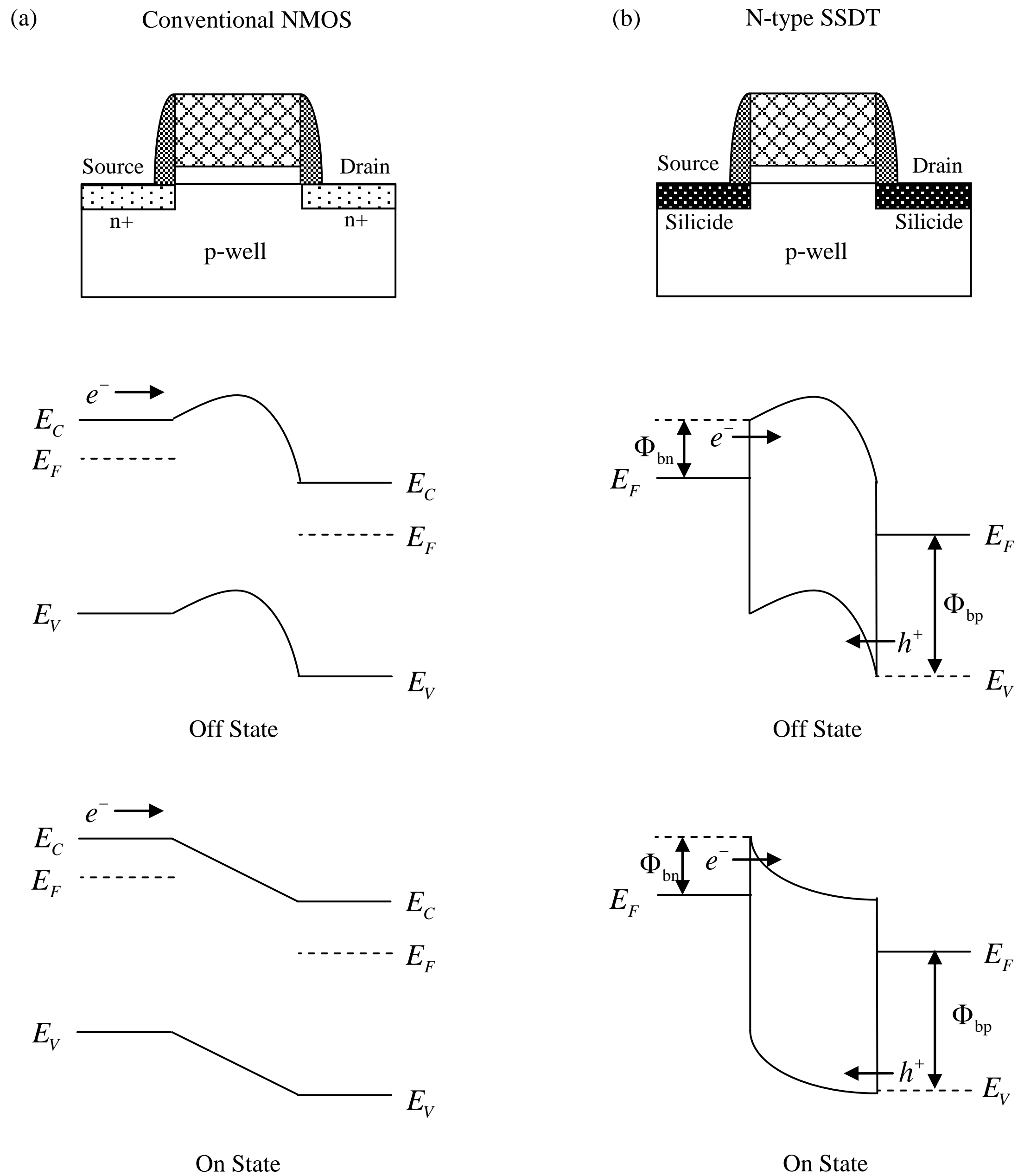

Fig. 2.3. Device architecture and band diagrams in off and on states for (a) conventional impurity-doped S/D NMOS device, and (b) SSDT device.

Similar to conventional CMOS devices, SSDT subthreshold leakage current is typically dominated by four components: 1) gate-induced drain-leakage current (I_{GIDL}); 2) junction leakage (I_{j}); 3) S/D thermal-emission leakage current (I_{th}); and 4) gate insulator leakage (I_{g}):

$$I_{\mathrm{off}} = I_{\mathrm{GIDL}} + I_{\mathrm{j}} + I_{\mathrm{th}} + I_{\mathrm{g}} \, . \tag{2.4}$$

The gate dielectric leakage is similar to conventional MOSFET, which is related to the thickness and other properties of the high-κ material. Junction leakage current (I_{j}) for an SSDT is caused by the reverse-biased Schottky diode at the drain electrode. This reverse leakage current is larger than the T-E model prediction because of the recombination and trap-assisted tunnel currents caused by the defects at the MS interface.

Fig. 2.3(b) (middle) illustrates the band diagram in the off state for an SSDT, with the drain biased at $V_{\mathrm{ds}} = V_{\mathrm{dd}}$, and $V_{\mathrm{gs}} = 0$. For n-type SSDT, I_{GIDL} is caused by the tunneling of holes through the relatively large but thin barrier at the drain side in the off state, which is a result of the close proximity of the drain to the gate. The Schottky barrier to holes (Φ_{bp}) can be approximated to the difference between the silicon band gap (E_{g}) and the electron barrier height (Φ_{bn}):

$$\Phi_{\mathrm{bp}} \approx E_{\mathrm{g}} - \Phi_{\mathrm{bn}} \, . \tag{2.5}$$

I_{GIDL} is strongly dependent on the width of the hole barrier. The barrier width is a function of E-field and potential profile near the drain area.

The most significant contribution to subthreshold leakage current is the source-to-drain thermal-emission leakage current (I_{th}). Due to the presence of Schottky barrier, SSDT have an intrinsic advantage in controlling I_{th} because the Schottky barrier plays the role of halo implant, without having to add any dopants to

the channel region. This leakage current is a function of both Φ_{bp} and channel length. I_{th} can be suppressed by a relatively low-concentration simple channel doping profile.

At on state, a strong electric field is present at the source electrode, virtually all of the source-emitted current is due to field emission of carriers that tunnel through the Schottky barrier. As the channel charge increases, the E-field at the source reduces due to charge screening effect, which in turn reduces the field-emitted current, until equilibrium is achieved. The physics and models for the on-state current are fundamentally different from those used in conventional MOSFET. There have been several approaches for estimating the field-emission tunnel current (J_{fe}) through the sharp triangular Schottky barrier at the source side which is shown in the on-state band diagram in Fig. 2.3(b) [17-22]. In general, the field emission current is sensitive to the Schottky barrier height [9]:

$$J_{fe} \sim \exp(\frac{-q\Phi_{bn}}{E_{00}}), \tag{2.6}$$

where $E_{00} \equiv \frac{q\hbar}{2}\sqrt{\frac{N_D}{\varepsilon_s m^*}}$. The field emission decreases exponentially with increasing electron barrier Φ_{bn}.

In summary, the for N-SSDT, the electron barrier Φ_{bn} should be kept as low as possible to obtain higher drive current, while the hole barrier Φ_{bp} must be large enough to suppress the off-state current. There are various reports discussing the optimal Schottky barrier height for SSDT to outperform the conventional MOSFET. J. Guo *et al.* claimed a zero or even negative barrier height is required for acceptable

performance [23], while M. Fritze *et al*. suggest that a sub-0.3-eV barrier would be good enough [24].

2.2 Process Development

2.2.1 Overview

The manufacturing process for SSDT requires fewer steps than conventional CMOS. The process starts with a standard STI or LOCOS for isolation, followed by well implants and channel implants. Gate stacks are then formed by either traditional dual-doped poly-Si/SiON stack or metal gate/high-κ dielectric stack. After gate etch, a thin (<10 nm) sidewall spacer is formed by oxide deposition and anisotropic etch. Low-dose implant is not needed to form lightly doped drain (LDD). The spacer thickness must be thin enough to avoid discontinuity between the S/D and channel, but not too thin to cause short-circuit between gate electrode and S/D. S/D extension and deep contact implants are also eliminated. Since different kinds of silicides are used for P-SSDT and N-SSDT, the silicide exclusion mask is used to form the two different S/D regions separately.

There are significant process advantages with SSDT technology. Firstly, the post-gate thermal budget is reduced. The maximum process temperature is less than 600 ℃ after gate formation. S/D implantation and deep ion implantation steps are eliminated and so are the high-temperature 900 - 1000 ℃ dopant activation anneals. This releases the thermal budget for metal gate and high-κ gate dielectric. Lower cost is also achieved by eliminating the implantation and spike annealing steps.

2.2.2 Integration Issues

Lanthanoids are all chemically reactive. This leads to several issues that need to be addressed for integration with conventional process.

Firstly, both lanthanoids and their silicides are chemically reactive to oxygen. Oxygen contamination not only increases the resistivity of lanthanoid silicides, but also degrades the Schottky barrier height. For $ErSi_{2-x}$ silicide, the electron barrier Φ_{bn} was reported to be 0.28 eV when it was grown in ultra-high-vacuum (UHV) condition [25]; however, it becomes higher for growth in normal vacuum as reported in another paper [26].

To study the effect of oxygen, we intentionally varied the process condition for $YbSi_{2-x}$. Fig. 2.4 shows the *I-V* curves of $YbSi_{2-x}$/Si where with Yb deposited at 2 mTorr and 4 mTorr in Ar ambient during sputtering whereas other processes were kept the same as will be discussed later in this chapter. O_2 contamination is always present in the N_2 and the chamber; the lower the total pressure, the lower the O_2 partial pressure in the chamber. The one deposited at a higher pressure shows a lower Schottky barrier and higher reverse leakage current, implying a degraded Schottky contact. Other factors, such as annealing temperature and pressure, silicon substrate doping concentration, and the different fitting techniques may also lead to discrepancies in barrier height values for different experiments. Strict process control, especially the oxygen contamination control is crucial for a high-quality Schottky junction. Very low barrier height (0.08 eV) of metal/n-Si contacts has been reported recently by surface passivation of a thin Se layer [27]. However, such method is infeasible for N-SSDT fabrication due to the requirement of self-aligned S/D formation.

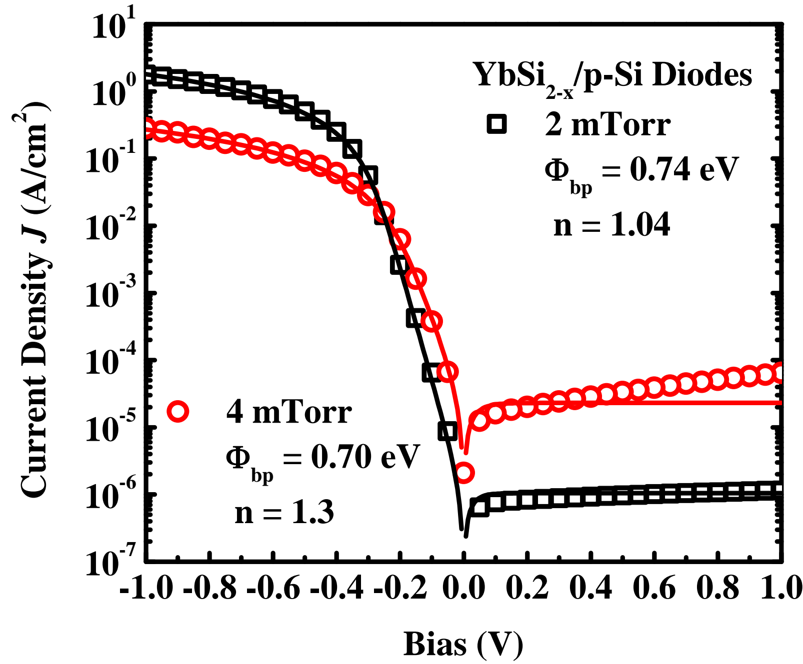

Fig. 2.4. *I-V* curves of $YbSi_{2-x}$/p-Si diodes, with Yb deposited at 2 mTorr and 4 mTorr.

To reduce the oxygen contamination, the background pressure of the sputter chamber was set to of 1×10^{-7} Torr before deposition. A relatively long burn-in step was performed on the lanthanoid targets prior to the sputtering process in order to remove possible surface moisture and oxides on the targets. The working pressure was set to 2 mTorr, which is the lowest according to the machine's specification.

The second problem is that the devices fabricated with SiO_2 spacer suffered from short-circuit between the gate and the source/drain. Fig. 2.5 shows the Scanning Electron Microscope (SEM) images of a transistor with poly-Si/SiO_2 gate, SiO_2 spacer and $YbSi_{2-x}$ S/D. Silicide bridging was observed at multiple locations along the gate side wall. This is similar to the reported TiSi bridging problem [28]. During the formation of lanthanoid or titanium silicides, the dominant diffusion species is silicon [26]. The out-diffusion of silicon grows along the gate side wall and causes short-circuit between the gate and source/drain. The bridging problem is less prominent for

NiSi and $CoSi_2$, since Ni and Co are the dominant diffusion species during the formation.

The third problem comes from the reaction between lanthanoid and SiO_2. The penetration of lanthanoid metals into SiO_2 at elevated temperature brings another major integration issue since it degrades isolations such as spacer and STI. 100 nm Yb was deposited on 400 nm SiO_2 with 100 nm HfN capping layer. The stack was annealed at multiple temperatures from 300 ℃ to 600 ℃ for silicidation. The capping HfN was then removed by DHF dipping and the unreacted Yb was removed by HNO_3. Discoloration was observed on the remaining surface of SiO_2, which is an evidence of chemical reaction between Yb and SiO_2 (Fig. 2.6). This is similar to the reaction between Tb and SiO_2 which is reported in [29].

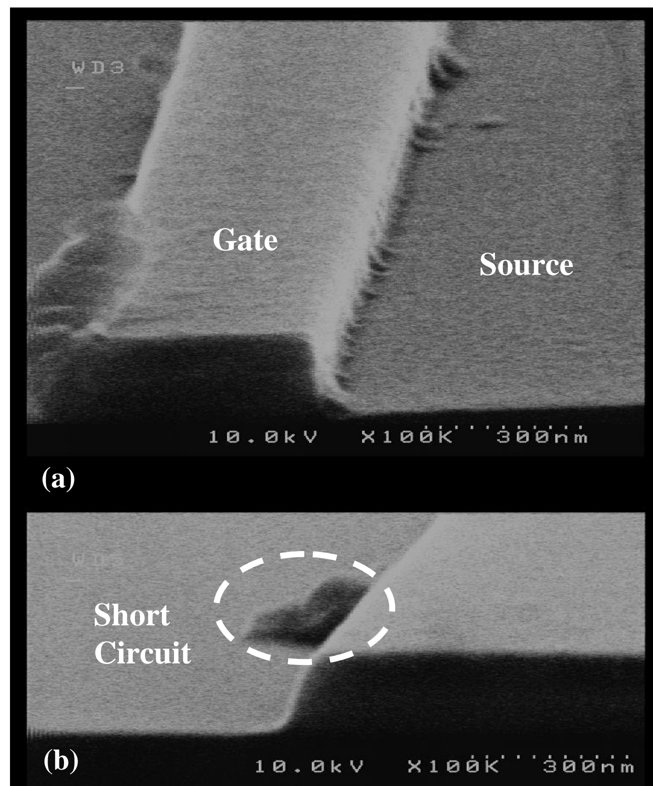

Fig. 2.5. (a) Scanning Electron Microscope (SEM) of a transistor with poly-Si/SiO_2 gate, SiO_2 spacer and $YbSi_{2-x}$ S/D. (b) SEM image zoomed in to one of the bridges between S/D and gate on the side wall.

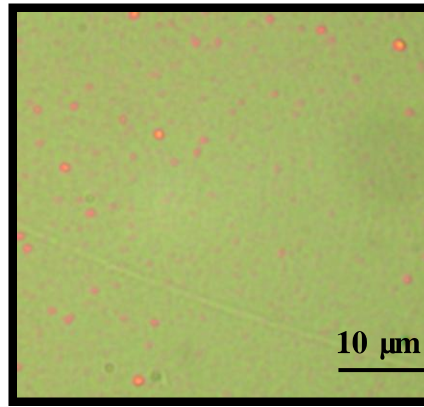

Fig 2.6. Optical microscopic image of SiO_2 surface after selective etch. Yb was first deposited on the SiO_2, annealed at 350 ℃ for 1 minute, and then removed by selective wet etch by 5% HNO_3.

2.2.3 SSDT device Fabrication

To prevent the issues discussed in Section 2.2.2, a one-mask transistor process featuring “hole spacer” was designed to fabricate N-SSDT. The top view of the layout is shown in Fig 2.7(a). The gate is all around the source in the top view, and the drain is all around the gate. The cross sectional schematic is illustrated in Fig. 2.7(b). The gate electrode contains two layers, HfN and TaN, whereby the hole spacer was formed on the side wall of HfN. Cross-section TEM of an SSDT device is shown in Fig. 2.7(c). The hole spacer is clearly visible on the image. Note that source/p-Si is a square shaped Schottky diode. The electrical characterization of Schottky diode in this chapter was conducted from the source/p-Si diodes.

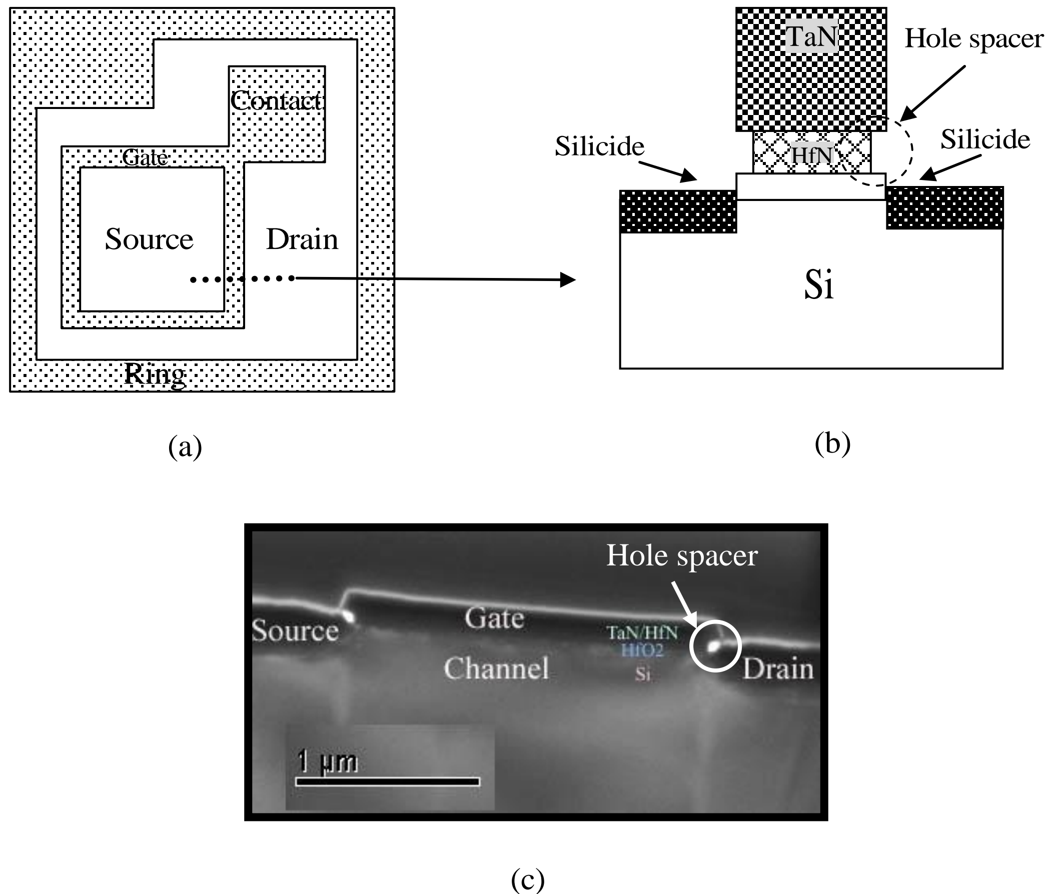

Fig. 2.7. (a) Top view schematic of a one-mask transistor. (b) Cross-section schematic of a one-mask transistor. (c) Cross-section TEM of a SSDT device of 2-μm gate length.

Figure 2.8 illustrates the process flow for the one-mask SSDT. N-type Si (100) wafers with resistivity of 4-8 Ω cm were used as the starting substrates. After a standard RCA clean and diluted HF (DHF) solution dipping, a ~6 nm HfO_2 film was deposited at 400 ℃ using $Hf[OC(CH_3)_3]_4$ and O_2 in a MOCVD system, followed by an in-situ post deposition annealing in N_2 ambient at 700 ℃ to improve the film quality. Then, a HfN (~50nm)/TaN(~100 nm) stack was deposited as a metal gate in a sputtering system with a base pressure of ~1.4×10^{-7} torr at room temperature, where TaN was used as a capping layer to reduce the sheet resistance (~10 Ω/sq). The wafers were patterned using standard photolithography and reactive ion etching (RIE)

procedures to etch the TaN/HfN/HfO_2 stack. The patterned wafers were then dipped in DHF to form a hole at the side wall on the HfN while the TaN on top remained intact; the native oxide in S/D region was removed at the same time. This hole served as isolation from the source/drain to the gate electrode. Immediately after the dipping, the wafers were loaded into the sputtering system again to deposit lanthanoid metal (~ 100 nm)/HfN(~100 nm) stack at 2 mTorr. The lanthanoid metals are Dy, Tb, Er and Yb. Silicidation was performed by rapid thermal anneal (RTA) at 600 ℃ for 1 minute in Ar ambient. Since the lanthanoid metals could be easily oxidized during ex-situ anneal, a capping layer of HfN was used to prevent lanthanoid metal oxidation during the annealing. HfN is a thermally stable material which could serve as an oxygen barrier in the gate stack to prevent the EOT increase during annealing [30]. Unreacted lanthanoid metal beneath the capping layer prevents HfN from participating in the silicidation process. Forming gas anneal (FGA) was done at 420 ℃ for 1 hour to improve the electrical and reliability characteristic of the HfO_2 dielectric. Finally, the HfN capping layer and the unreacted lanthanoid metal were removed by DHF (1%) and diluted HNO_3 (5%) solutions sequentially.

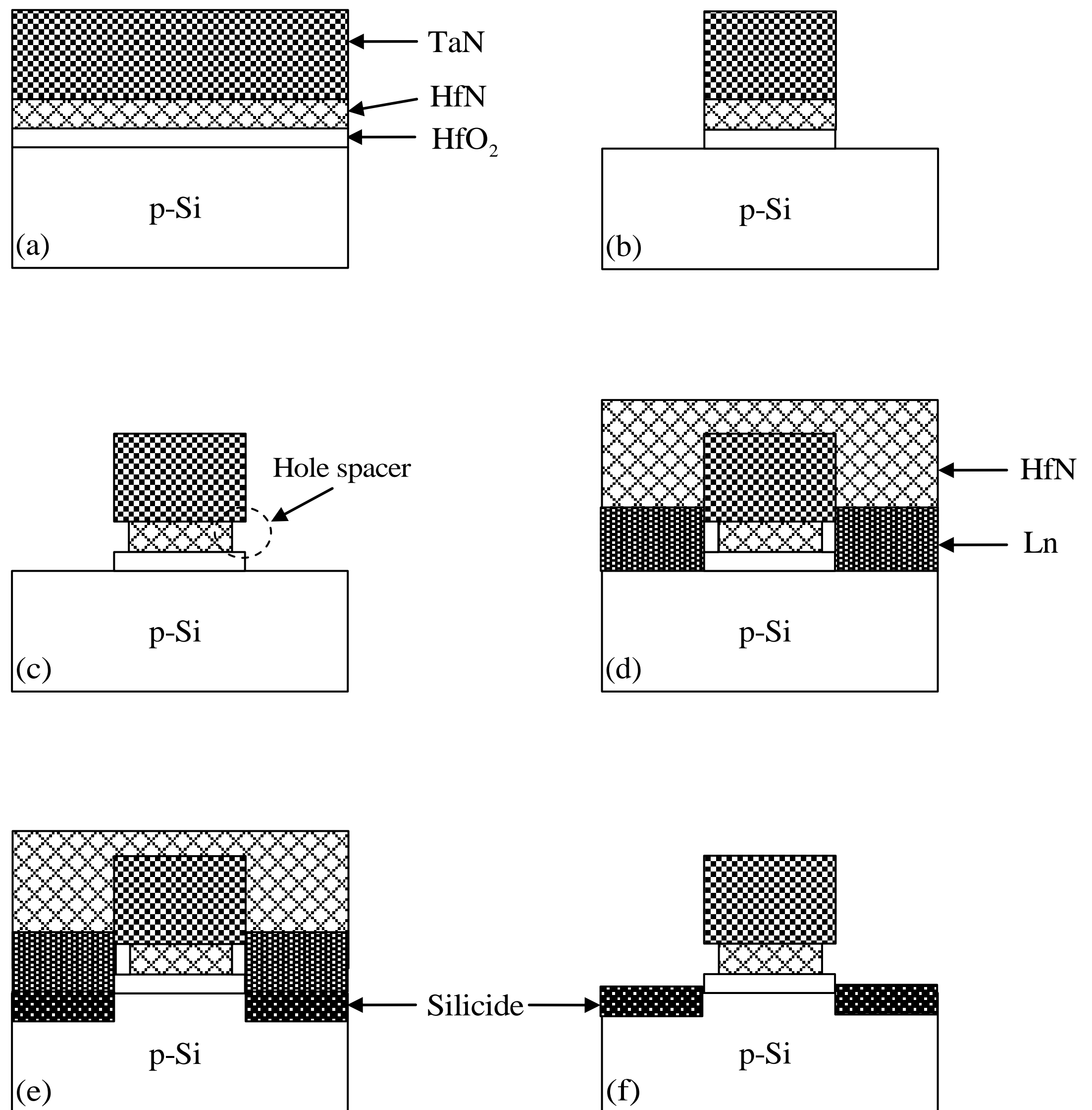

Fig. 2.8. Process flow of Schottky source/drain transistors. (a) Deposition of gate stack. (b) Patterning of gate stack. (c) DHF dip to remove the native oxide on source/drain region. A hole is formed on the side wall of HfN. (d) Deposition of lanthanoid metals (Dy, Er, Tb, or Yb), capped by HfN to prevent oxidation during silicidation. (e) Silicidation in RTP. (f) Selective etch of top HfN (by DHF) and un-reacted lanthanoid metal (by diluted HNO_3); lanthanoid silicide source/drain are intact.

2.3 Device Characterization and Analysis

2.3.1 Schottky Diode Characterization

Fig. 2.9 shows *I-V* curves of various lanthanoid silicide/p-Si(100) Schottky diodes. The Schottky hole barrier height (Φ_{bp}) and the ideality factor (*n*) were deduced by fitting with the thermal emission model taking consideration of the series resistance from the top contact, p-Si substrate, and bottom contact (Fig. 2.10). Among the four lanthanoid silicides, the $YbSi_{2-x}$/p-Si contact has the highest hole barrier height (Φ_{bp}) of 0.74eV, lowest reverse bias leakage current, and the best rectifying property with near unity ideality factor. Other diodes have significantly higher leakage current at reverse bias.

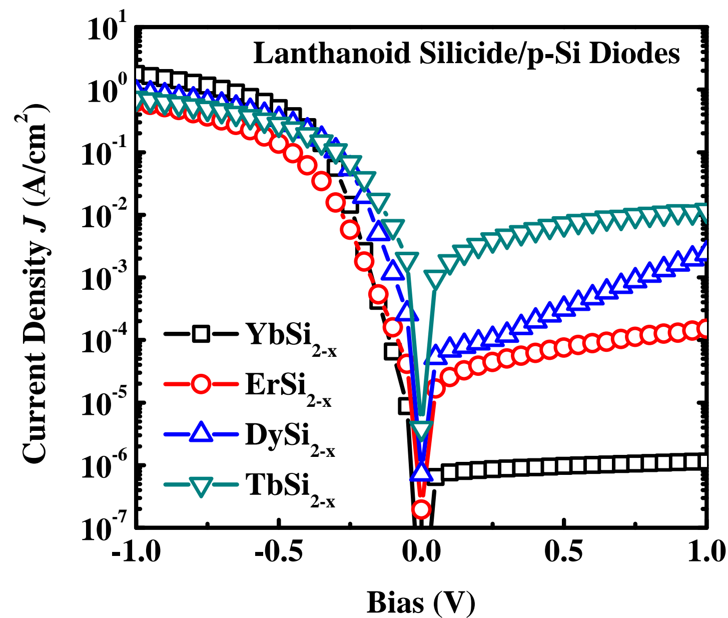

Fig. 2.9. Room temperature *I-V* curves of various $LnSi_{2-x}$/p-Si(100) diodes.

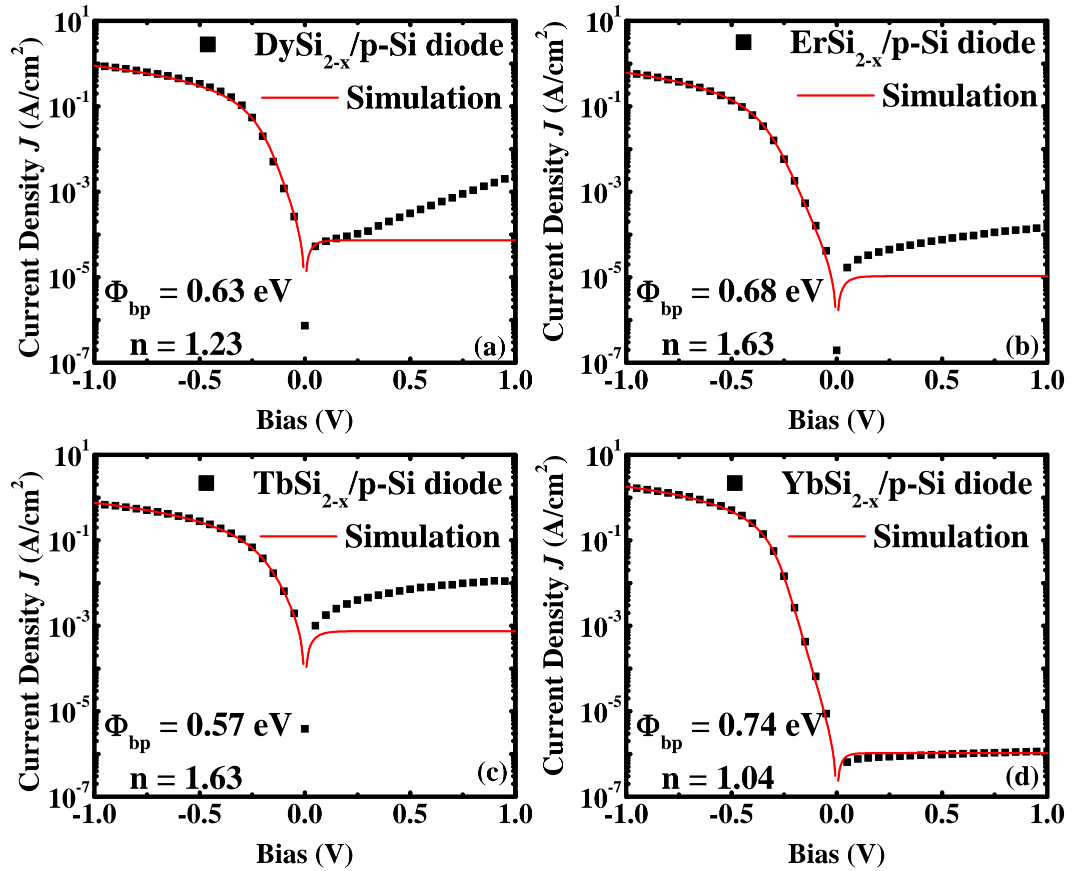

Fig. 2.10. Thermal emission model fitting of the *I-V* curves of Schottky diodes. (a) $DySi_{2-x}$/p-Si; (b) Er Si_{2-x}/p-Si; (c) Tb Si_{2-x}/p-Si; (d) $YbSi_{2-x}$/p-Si.

It is noticed that in Fig. 2.10, the measured reverse current is much higher than the simulated current, except for $YbSi_{2-x}$. There are several causes of the departure from the ideal behavior: 1) field dependence of the barrier height; 2) the effect of tunneling; 3) generation in the depletion region [16]. The defects and inhomogeneity at the silicide/Si interfaces lead to excessive tunneling and generation-recombination currents.

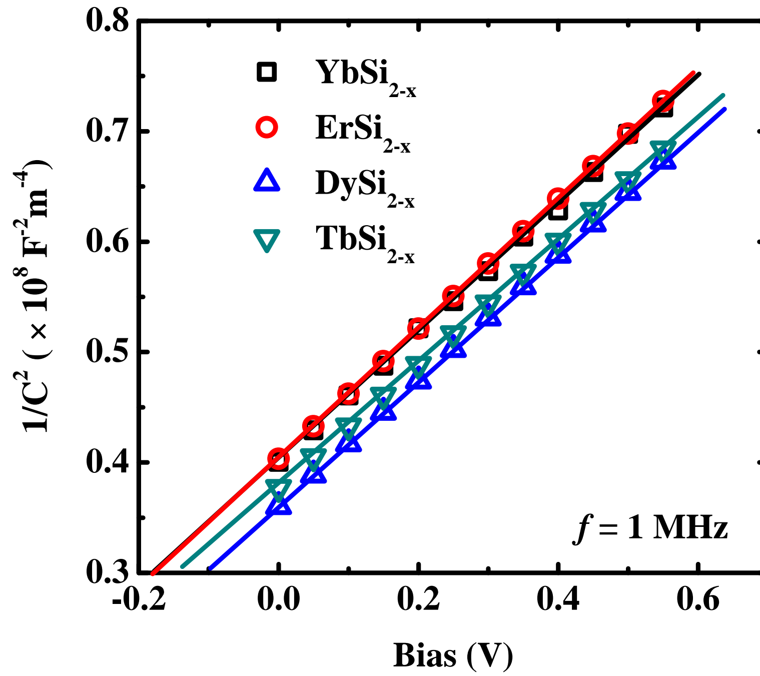

Fig. 2.11. Reverse bias *C-V* curves for $LnSi_{2-x}$/p-Si diodes.

The Schottky barrier heights were also derived from Capacitance-Voltage (*C-V*) measurement. A C^{-2} versus *V* plot of the $LnSi_{2-x}$/p-Si diodes is shown in Fig. 2.11. The barrier heights obtained are 0.83, 0.78, 0.87, and 0.88 eV, for $DySi_{2-x}$, $ErSi_{2-x}$, $TbSi_{2-x}$, and $YbSi_{2-x}$, respectively.

Deviation of ideality factor from unity and the large difference between the barrier heights derived from *I-V* and *C-V* measurements indicate un-negligible barrier height inhomogeneity [31]. The surfaces of $DySi_{2-x}$, $ErSi_{2-x}$ and $TbSi_{2-x}$ contain many square pits of micrometer size [Fig. 2.12(a)]; while there are no such pits on the surface of $YbSi_{2-x}$ [Fig. 2.12(b)]. Contamination at the metal/Si interface was suggested as the primary cause of surface pitting [32, 33].

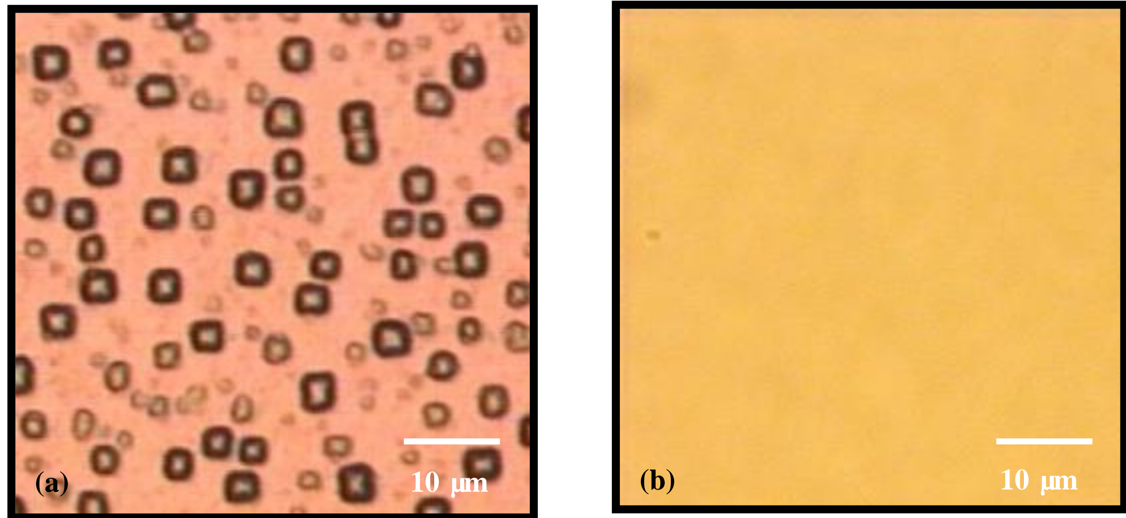

Fig. 2.12. Top view of (a) $DySi_{2-x}$ and (b) $YbSi_{2-x}$ as observed using an optical microscope.

It was reported that the surface pits may be reduced in density or eliminated entirely either through the use of a Si substrate surface prepared under UHV conditions prior to metal deposition, or by means of ion irradiation techniques [33]. Since all samples were prepared under the same condition, the better morphology of $YbSi_{2-x}$ suggests that ytterbium is less affected by the surface contamination.

Fig. 2.13 (top) shows the cross-sectional TEM image of the N-SSDT fabricated by the simplified one-mask process, a hole between the S/D and the gate acts as the sidewall spacer. Fig 2.13 (bottom) shows the high resolution image of the polycrystalline $YbSi_{2-x}$/Si(100) contact. The grain size of the polycrystalline $YbSi_{2-x}$ is about 5 ~ 10 nm and the grain growths approximately along Si [110] axis. The interface is abrupt, flat, and sharp, and leads to excellent electrical performance. Columnar growth, as in the cases of $DySi_{2-x}$, $ErSi_{2-x}$ and $TbSi_{2-x}$ was not found.

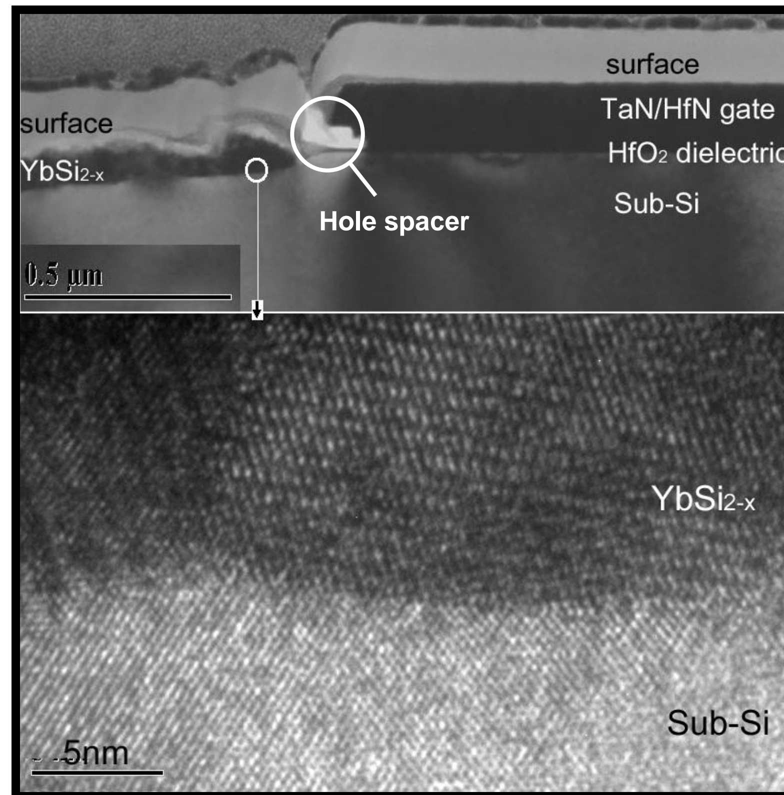

Fig. 2.13. (Top) Cross sectional TEM image of the N-SSDT with $YbSi_{2-x}$ source/drain fabricated by our simplified one-mask process. (Bottom) High resolution XTEM image of polycrystalline $YbSi_{2-x}$/Si(100) contact.

The formation of $YbSi_{2-x}$ was studied by XRD by analyzing samples annealed at different temperatures. From Fig. 2.14, it can be observed that silicide peaks do not show up until the annealing temperature reaches 300 ℃. $YbSi_{1.7}$ was formed at 300 ℃ and 350 ℃. The phase changes to $YbSi_{1.8}$ after 600 ℃ anneal. Higher concentration of Si means less Si vacancy, and that might have increased the uniformity of the Schottky contact. For Dy, Er, and Tb, The formed silicides were found to be $DySi_{1.7}$ and $ErSi_{1.7}$ due to the Si vacancy in the silicide thin film, which is consistent with the report in [4]. The formation of $YbSi_{1.8}$ with less Si vacancy is possibly due to the fact that ytterbium is less affected by the surface contamination, such as SiO_2. The small work function of Yb makes it chemically more active than the other three lanthanoid elements, and easier for it to overcome the SiO_2 layer and continue the reaction.

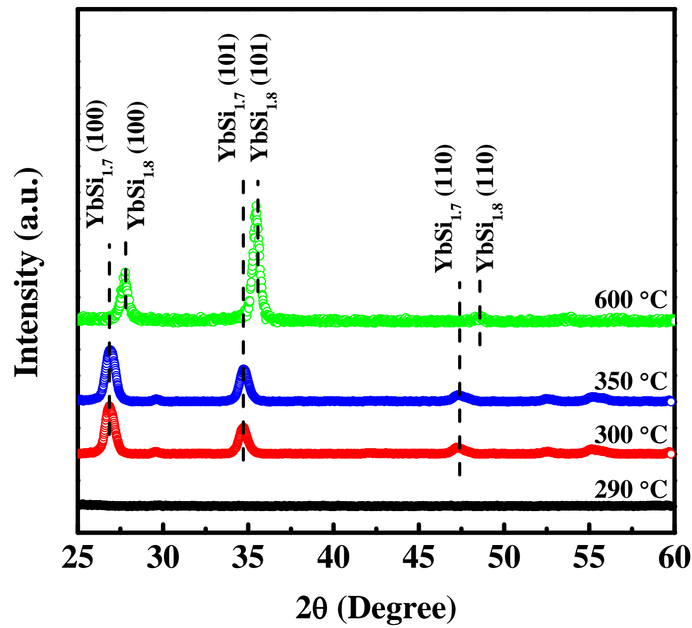

Fig. 2.14. X-ray diffraction (XRD) spectra of Yb silicide formed at different annealing conditions.

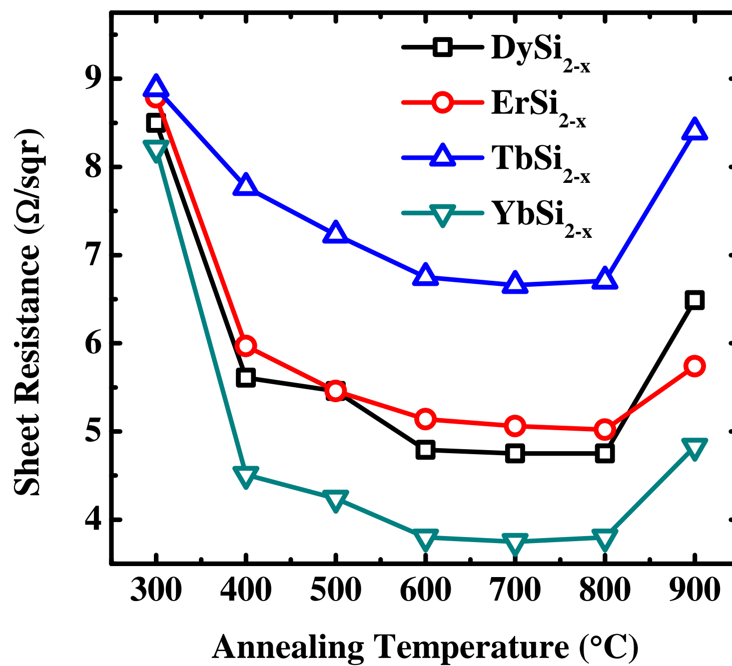

Fig. 2.15. Sheet resistance of lanthanoid silicides formed at different annealing conditions.

The sheet resistances of various lanthanoid silicides are studied in Fig. 2.15. The resistance reaches the minimum at around 600 ℃ for all of the four silicides, indicating the formation of a low resistance phase. $YbSi_{2-x}$ shows the smallest sheet resistance comparing to the other three for the temperature range from 300 ℃ to 900 ℃. The sheet resistance of $YbSi_{2-x}$ formed at 600 ℃ is ~3.8 Ω/sq. From the sheet resistance and the thickness of ~ 90 nm (measured by XTEM), the resistivity of $YbSi_{2-x}$ was calculated to be ~ 34 μΩ·cm.

2.3.2 Transistor Characterization

Fig. 2.16 shows the cross sectional TEM image of the HfN/HfO_2/p-Si gate stack. The HfO_2 has been partially crystallized. The interfaces between HfN/HfO_2 and HfO_2/p-Si are both well-defined. The *C-V* curve measured from the gate stack is shown in Fig. 2.17.

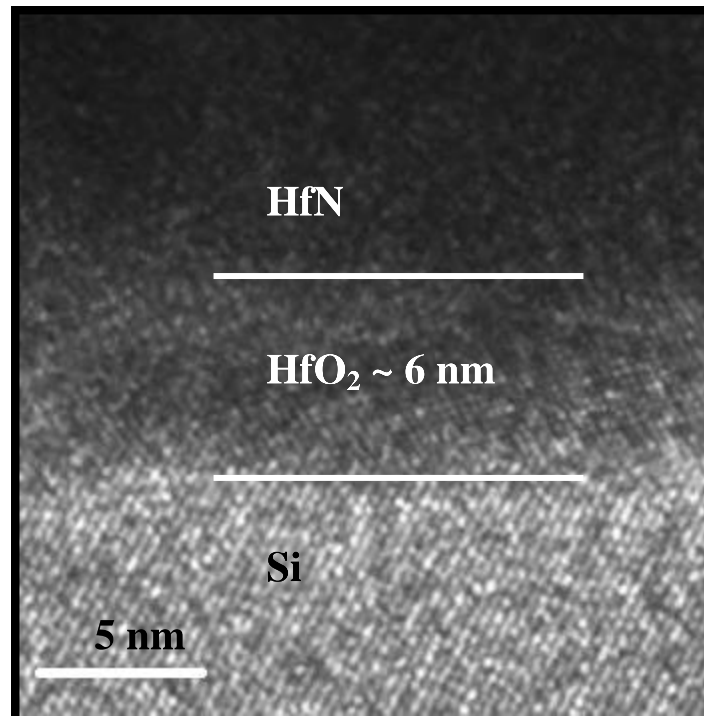

Fig. 2.16. High resolution TEM image of the HfN/HfO_2/p-Si gate stack, with 700 ℃ post-deposition anneal (PDA) and 420 ℃ forming gas anneal (FGA).

The effect oxide thickness (EOT) can be deduced by fitting the *C-V* curve from the quantum mechanical (QM) model with the measured curve. Fig. 2.18 shows the gate leakage current densities. A 1000 ℃ spike post metal anneal (PMA) was done to simulate the S/D activation. It is observed that after the PMA, the capacitance density drops significantly, causing the EOT to increase from 1.53 nm to 2.21 nm. This was due to the formation of a thick interfacial layer at the HfO_2/Si interface. However, the leakage current at positive bias increases despite of the increase in EOT due to the poor quality of the bottom interface after PMA. The benefit of the low temperature fabrication process to the high-κ dielectric has been reported by other authors [5].

Fig. 2.18(a) shows the I_{ds}-V_{gs} curves of N-SSDT with $YbSi_{2-x}$ source and drain. The gate length (L_g) is 4 μm and the gate width is 400 μm. The on/off ratio reaches 10^7 with a subthreshold swing of 75 mV/dec. For comparison, Fig. 2.18(b) shows the transfer characteristics of N-SSDT with the same device structure and technology, but different S/D silicides. It is clear that all other N-SSDTs exhibit higher off-state current, lower on-state current, smaller on/off ratio and larger subthreshold swing comparing to N-SSDT with $YbSi_{2-x}$. As the gate stacks are exactly the same, the large subthreshold swing for $DySi_{2-x}$, $ErSi_{2-x}$, and $TbSi_{2-x}$ are expected to be the result of large junction leakage caused by poor silicide/Si interface. This is consistent with the previous diode characterizations.

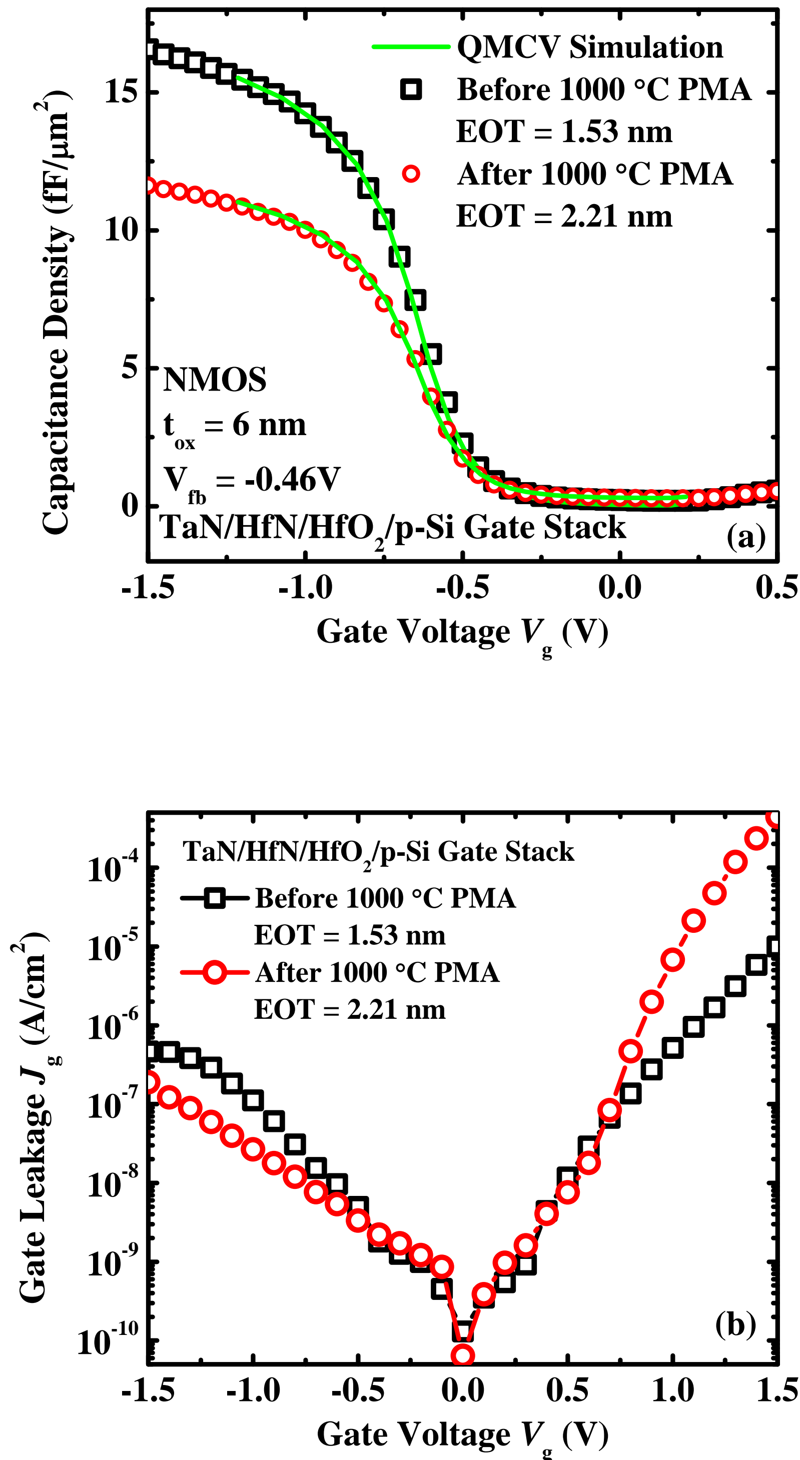

Fig. 2.17. (a) *C-V* and (b) *I-V* curves of the TaN/HfN/HfO_2/p-Si gate structure.

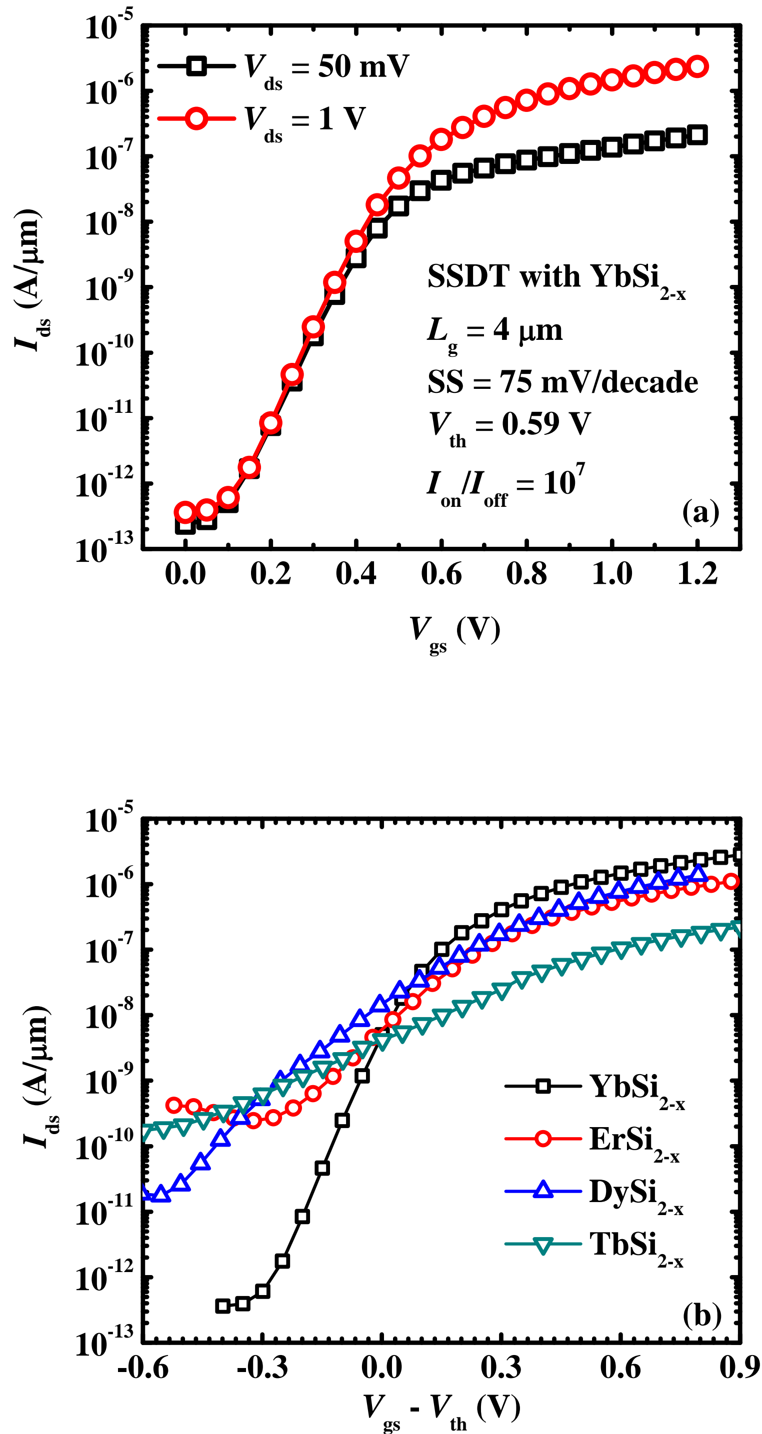

Fig. 2.18. (a) I_{ds}-V_{gs} characteristics of TaN/HfN/HfO_2 gated n-SSDT with $YbSi_{2-x}$. (b) I_{ds}-V_{gs} characteristics of TaN/HfN/HfO_2 gated n-SSDT with $DySi_{2-x}$, $ErSi_{2-x}$, $TbSi_{2-x}$, $YbSi_{2-x}$.

Fig. 2.19 shows the I_{ds}-V_{ds} curves of N-SSDT with $YbSi_{2-x}$ source/drain. A reasonable drive current of 7.5 μA/μm is achieved for a gate voltage of 1.5 V.

Table 2.2 summarizes the electrical characteristics of various lanthanoid silicide/p-Si (100) contacts formed by solid-state reaction and their corresponding N-SSDT properties. Due to the difficulty to measure a low electron Schottky barrier height Φ_{bn} directly, the high hole barrier height Φ_{bp} is measured and the electron barrier height is calculated according to the approximation of $\Phi_{bn} + \Phi_{bp} \cong E_g$ (silicon bandgap). Among all the four lanthanoid silicides, $YbSi_{2-x}$ exhibits the largest hole barrier, smallest electron barrier and reverse leakage current in contact with p-Si(100); it also shows the largest drive current and on/off ratio in N-SSDT.

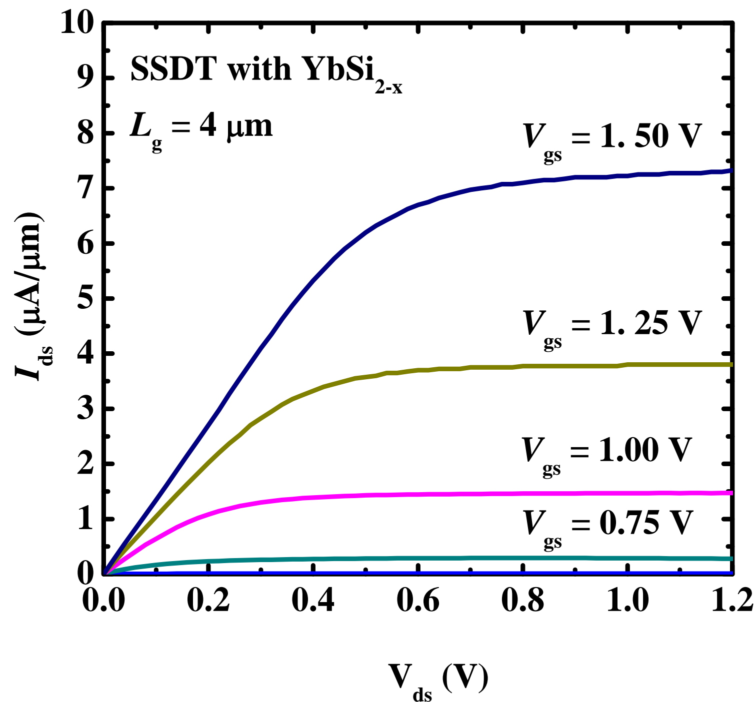

Fig. 2.19. I_{ds}-V_{ds} characteristics of $TaN/HfN/HfO_2$ gated n-SSDT with $YbSi_{2-x}$ source/drain.

Table 2.2. Electrical characteristics of various lanthanoid silicide/p-Si (100) contacts formed by solid-state reaction and their corresponding N-SSDT properties.

Silicide/p-Si (100) diode	**$ErSi_{2-x}$**	**$DySi_{2-x}$**	**$TbSi_{2-x}$**	**$YbSi_{2-x}$**
Hole barrier obtained by *I-V* measurement, Φ_{bp}^{IV} (eV)	0.68	0.63	0.57	0.74
Ideality factor in I-V, *n*	1.5	1.23	1.63	1.04
Hole Barrier obtained by *C-V* measurement, Φ_{bp}^{CV} (eV)	~ 0.78	~ 0.83	~ 0.87	~ 0.88
Averaged hole barrier $\Phi_{bp} = (\Phi_{bp}^{IV} + \Phi_{bp}^{CV})/2$ (eV)	0.73	0.73	0.72	0.81
Electron Barrier $\Phi_{bn} = 1.12 - \Phi_{bp}$ (eV)	0.39	0.39	0.40	0.31
Leakage @ 1V (A/cm^2)	1.5×10^{-4}	2.3×10^{-3}	1.2×10^{-2}	1.1×10^{-6}
N-SSDT (L_g = 4 μm)	**$ErSi_{2-x}$**	**$DySi_{2-x}$**	**$TbSi_{2-x}$**	**$YbSi_{2-x}$**
I_{on} / I_{off} ratio	10^3~10^4	10^4~10^5	10^3~10^4	~ 10^7
I_{ds} (μA/μm) @ $\lvert V_{ds} \rvert = V_{gs} - V_{th} = 1$(V)	~ 1.4	~ 2.5	~ 0.26	~ 3.4

2.4 Conclusion

In summary, new process technologies for SSDT were investigated. We addressed the compatibility issues of lanthanoid materials with conventional CMOS processing technology and developed a low temperature MOSFET process featuring a “hole spacer”, Schottky barrier source/drain, high-κ dielectric and metal gate electrode. Several lanthanoid elements, namely Dy, Er, Tb and Yb, were investigated to form silicide S/D for N-SSDT. The $YbSi_{2-x}$ has been found to be a very promising

candidate for N-SSDT as it provides a high drive current with a very low leakage current. It is probably due to the low electron barrier height of the $YbSi_{2-x}$/Si Schottky contact and smooth $YbSi_{2-x}$/Si interface. It can be concluded that $YbSi_{2-x}$ is a much better silicide material than the commonly used $ErSi_{2-x}$ and other lanthanoid silicides for N-SSDT. However, there are still major challenges integrating the lanthanoid silicide S/D with conventional CMOS processing technology because of their chemically reactive nature.

References:

[1] M. P. Lepselter and S. M. Sze, "SB-IGFET: An insulated-gate field-effect transistor using Schottky barrier contacts for source and drain," *Proc. IEEE,* vol. 56, pp. 1400-1402, 1968.

[2] M. Nishisaka, S. Matsumoto, and T. Asano, "Schottky source/drain SOI MOSFET with shallow doped-extension," *International Conference on Solid-State Devices and Materials Tech. Dig.,* pp. 586-587, 2002.

[3] H. C. Lin, M. F. Wang, F. J. Hou, H. N. Lin, C. Y. Lu, J. T. Liu, and T. Y. Huang, "High-performance p-channel Schottky-barrier SOI FinFET featuring self-aligned PtSi source/drain and electrical junctions," *IEEE Electron Device Letters,* vol. 24, pp. 102-104, 2003.

[4] J. Kedzierski, P. Xuan, E. H. Anderson, J. Bokor, T. J. King, and C. Hu, "Complementary silicide source/drain thin-body MOSFETs for the 20nm gate length regime," *International Electron Devices Meeting Tech. Dig.,* pp. 57-59, 2000.

[5] C. Kang, H. Cho, K. Onishi, R. Nieh, R. Choi, S. Gopalan, S. Krishnan, J. Han, and J. Lee, "Bonding states and electrical properties of ultrathin HfON gate dielectrics," *Applied Physics Letters,* vol. 81, p. 2593, 2002.

[6] S. Zhu, H. Yu, J. Chen, S. Whang, J. Chen, C. Shen, C. Zhu, S. Lee, M. Li, and D. Chan, "Low temperature MOSFET technology with Schottky barrier source/drain, high-K gate dielectric and metal gate electrode," *Solid State Electronics,* vol. 48, pp. 1987-1992, 2004.

[7] L. E. Calvet, H. Luebben, M. A. Reed, C. Wang, J. P. Snyder, and J. R. Tucker, "Suppression of leakage current in Schottky barrier metal-oxide-semiconductor field-effect transistors," *Journal of Applied Physics,* vol. 91, pp. 757-759, 2002.

[8] W. Saitoh, A. Itoh, S. Yamagami, and M. Asada, "Analysis of short-channel Schottky source/drain metal-oxide-semiconductor field-effect transistor on silicon-on-insulator substrate and demonstration of sub-50-nm n-type devices with metal gate," *Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers,* vol. 38, pp. 6226-6231, 1999.

[9] S. Sze, *Physics of Semiconductor Devices*, Willey, New York, 1981.

[10] R. Tung, "Formation of an electric dipole at metal-semiconductor interfaces," *Physical Review B,* vol. 64, pp. 205310, 2001.

[11] R. T. Tung, "Electron transport at metal-semiconductor interfaces: General theory," *Physical Review B,* vol. 45, pp. 13509-13523, 1992.

[12] H. Yu, J. Kang, C. Ren, J. Chen, Y. Hou, C. Shen, M. Li, D. Chan, K. Bera, and C. Tung, "Robust high-quality HfN-HfO_2 gate stack for advanced MOS device applications," *IEEE Electron Device Letters,* vol. 25, pp. 70-72, 2004.

[13] D. Schroder, *Semiconductor material and device characterization*, Wiley-interscience, 2006.

[14] R. T. Tung, "Recent advances in Schottky barrier concepts," *Materials Science and Engineering: R: Reports,* vol. 35, pp. 1-138, 2001.

[15] J. Andrews Jr and M. Lepselter, "Reverse current-voltage characteristics of metal silicide Schottky diodes," *IEEE Transactions on Electron Devices,* vol. 16, pp. 246-246, 1969.

[16] E. Rhoderick, "Metal-semiconductor contacts," *IEE Proceedings I, Communications, Speech and Vision,* vol. 129, pp. 124-132, 1982.

[17] R. Hattori, A. Nakae, and J. Shirafuji, "A new type of tunnel-effect transistor employing internal field emission of Schottky barrier junction," *Japanese Journal of Applied Physics Part 2 Letters,* vol. 31, pp. 1467-1467, 1992.

[18] R. Hattori and J. Shirafuji, "Numerical simulation of tunnel effect transistors employing internal field emission of Schottky barrier junction," *Japanese Journal of Applied Physics,* vol. 33, pp. 612-618, 1994.

[19] F. Padovani and R. Stratton, "Field and thermionic-field emission in Schottky barriers," *Solid-State Electron,* vol. 9, pp. 695-707, 1966.

[20] M. Ieong, P. Solomon, S. Laux, H. Wong, D. Chidambarrao, and H. IBM SRDC, "Comparison of raised and Schottky source/drain MOSFETs using anovel tunneling contact model," *International Electron Devices Meeting Tech. Dig.,* pp. 733-736, 1998.

[21] J. Knoch and J. Appenzeller, "Impact of the channel thickness on the performance of Schottky barrier metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters,* vol. 81, pp. 3082, 2002.

[22] B. Winstead and U. Ravaioli, "Simulation of Schottky barrier MOSFETs with a coupled quantum injection/Monte Carlo technique," *IEEE Transactions on Electron Devices,* vol. 47, pp. 1241-1246, 2000.

[23] J. Guo and M. Lundstrom, "A computational study of thin-body, double-gate, Schottky barrier MOSFETs," *IEEE Transactions on Electron Devices,* vol. 49, pp. 1897-1902, 2002.

[24] M. Fritze, C. Chen, S. Calawa, D. Yost, B. Wheeler, P. Wyatt, C. Keast, J. Snyder, and J. Larson, "High-speed Schottky-barrier pMOSFET with f_T= 280 GHz," *IEEE Electron Device Letters,* vol. 25, pp. 220-222, 2004.

[25] P. Muret, T. Nguyen Tan, N. Frangis, and J. Van Landuyt, "Unpinning of the Fermi level at erbium silicide/silicon interfaces," *Physical Review B,* vol. 56, pp. 9286-9289, 1997.

[26] K. Maex and M. Van Rossum, *Properties of metal silicides*, INSPEC, 1995.

[27] M. Tao, S. Agarwal, D. Udeshi, N. Basit, E. Maldonado, and W. P. Kirk, "Low Schottky barriers on n-type silicon (001)," *Applied Physics Letters,* vol. 83, pp. 2593-2595, 2003.

[28] L. Chen, *Silicide technology for integrated circuits*, The Institution of Engineering and Technology, 2004.

[29] G. Berning and H. Swart, "Multilayer formation during annealing of thin Tb layers on SiO_2 substrates," *Surface and Interface Analysis,* vol. 26, pp. 420-424, 1998.

[30] H. Y. Yu, H. F. Lim, J. H. Chen, M. F. Li, C. Zhu, C. H. Tung, A. Y. Du, W. D. Wang, D. Z. Chi, and D. L. Kwong, "Physical and electrical characteristics of HfN gate electrode for advanced MOS devices," *IEEE Electron Device Letters,* vol. 24, pp. 230-232, 2003.

[31] S. Zhu, R. L. Van Meirhaeghe, C. Detavernier, F. Cardon, G. P. Ru, X. P. Qu, and B. Z. Li, "Barrier height inhomogeneities of epitaxial $CoSi_2$ Schottky contacts on n-Si (100) and (111)," *Solid-State Electronics,* vol. 44, pp. 663-671, 2000.

[32] J. Knapp and S. Picraux, "Epitaxial growth of rare earth silicides on (111) Si," *Applied Physics Letters,* vol. 48, pp. 466, 1986.

[33] S. Lau, C. Pai, C. Wu, T. Kuech, and B. Liu, "Surface morphology of erbium silicide," *Applied Physics Letters,* vol. 41, pp. 77, 1982.

Chapter 3

Yb-Incorporated Ni FUSI for the N-MOSFETs Gate Electrode Application

3.1 Introduction

Metal gate is introduced in the sub-45nm CMOS technology nodes to eliminate the poly-Si gate depletion effect. Fully-silicidation (FUSI) metal gate electrodes such as NiSi, $CoSi_2$ and $TiSi_2$ have been extensively studied as an option for integrating metal gates in a CMOS process flow [1-3].

Ni FUSI technology has attracted considerable attention due to its compatibility with the conventional poly-Si technology [1, 2, 4-8], and due to demonstrated capability of work function modulation. The modulation of midgap NiSi gate work function Φ_m (4.65 $\pm$0.5 V) is highly desired to achieve low transistor threshold voltage, and various Φ_m tuning methods have been investigated [7, 9, 10]. Addition of dopants such as As and Sb may lower the work function, but at the expense of introducing adhesion issues that impact manufacturability [11]. Phase-controlled Ni-silicidation is another Φ_m tuning method and dual gate integration option. It employs different nickel silicide phases such as Ni-disilicide ($NiSi_2$), Ni-monosilicide (NiSi) or Ni-rich silicides (e.g. Ni_2Si, N_3iSi, or $Ni_{31}Si_{12}$) for Φ_m

tenability [9]. NiSi and Ni-rich silicides have been extensively researched upon for dual gate integration [12], as they are easier to be formed relative to $NiSi_2$. However, their small Φ_m tuning range of ~0.3 eV, is not sufficient for high performance CMOS applications.

As mentioned in Chapter 1, most lanthanoid elements exhibit low work function values (< 4.0 eV). It has been reported that the work function of TaN can be tuned to 4.2-4.3 eV by incorporating terbium and other lanthanoid elements [13, 14]. Incorporating lanthanoid elements in NiSi gate can potentially tune the work function toward the silicon band edge.

Yb is known for its low photoelectric work function of ~2.59 eV, which is even lower than most of other lanthanoid elements. A low electron barrier height (~0.31 eV) to silicon conduction band has been reported for Yb silicide in Chapter 2, outperforming Dy silicide, Er silicide and Tb silicide. In this chapter, Yb is used to modulate the work function of Ni FUSI. The effect of different Yb/Ni composition ratios was studied. By introducing Yb in Ni FUSI, we show that work function of Ni FUSI (on SiON dielectrics) could be tuned from ~4.72 eV to ~4.22 eV, which is suitable as a gate electrode for n-MOSFETs with V_{th} down to 0.2 V. A CMOS integration scheme is proposed to evaluate the process compatibility. The mechanism behind the work function tunability is discussed at the end of this chapter.

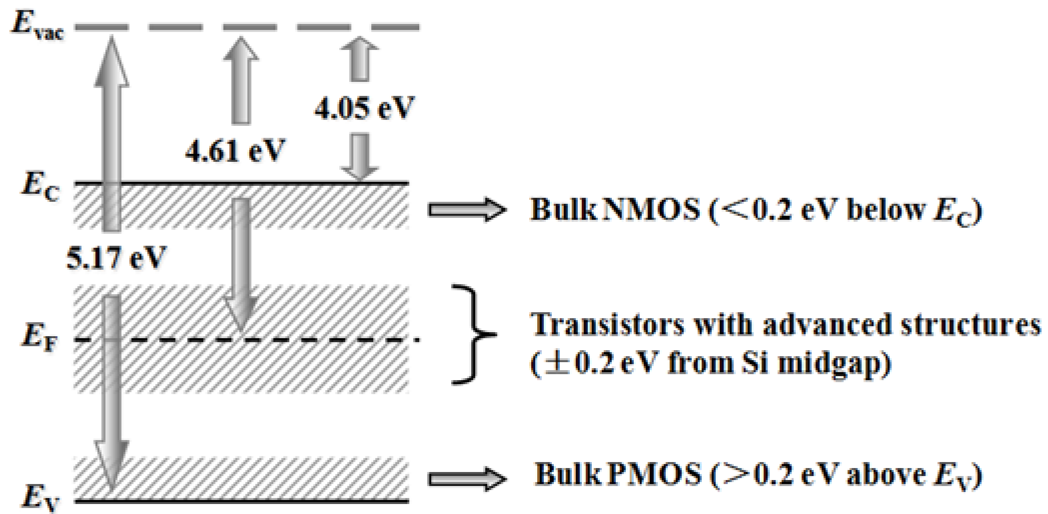

Fig. 3.1. Metal gate effective work function (Φ_m) requirements for both planar bulk transistors and ultra-thin body transistors.

3.2 Process Development

3.2.1 Process Flow for MOS Capacitors

Capacitors were fabricated on p-type Si substrate (with resistivity of 4-8 Ω-cm). SiO_2 was thermally grown and nitrogen was then incorporated to form SiON by decoupled plasma nitridation (DPN). This was followed by undoped poly-Si (~100 nm) deposition. After a dilute HF dip to remove native oxide on top of poly-Si, Ni-Yb was deposited by either co-sputtering or sequentially sputtering from Yb and Ni targets in Ar ambient. A working pressure of 2 mTorr and an Ar flow rate of 25 sccm were used for all Ni-Yb deposited by sputtering in this chapter. The back ground pressure in the sputter chamber was about 1×10^{-7} torr or less. A relatively long burn-in step was performed on the lanthanoid targets prior to the sputtering process in order to remove possible surface moisture and oxides on the targets. The ratio of Yb/Ni was controlled by adjusting the respective Yb and Ni deposition power and time. The four different thickness ratios of Yb/Ni are 1/40, 1/5, 1/3 and 1/2. The total metal thickness is kept at ~ 90 nm so that poly-Si could be completely silicided during the FUSI

process. The silicidation was done by one-step annealing in vacuum (5×10^{-6} Torr) at 400 ℃. Selective etch was then carried out to remove the remaining un-reacted Ni & Yb using dilute HNO_3 (5%). EOT and flat band voltage (V_{FB}) were obtained by fitting a simulated C-V that considered quantum mechanical effects. Ni FUSI control samples were made for comparison.

Capacitance-voltage (*C-V*) and current-voltage (*I-V*) characteristics were measured using a HP4284A LCR meter and HP4156A semiconductor parameter analyzer, respectively, on MOS capacitors with area of 100 × 100 μm^2. EOT and flat-band voltage (V_{FB}) were obtained by fitting the *C-V* curves with the theoretical ones, which take the quantum mechanical effect into account. Auger electron spectroscopy (AES), Rutherford backscattering spectrometry (RBS), secondary ion mass spectrometry (SIMS), X-ray photoelectron spectroscopy (XPS), X-ray diffraction (XRD) and high-resolution transmission electron microscopy (HRTEM) were also performed for material characterizations.

3.2.2 Thickness Ratio Control and Sputter Sequence for Yb/Ni

The thickness of Yb and Ni can be calculated from the desired thickness ratio of Yb/Ni since the total thickness is fixed at 90 nm. The deposition time for each material can be calculated as the deposition rate of each material at certain DC power is known. The detailed experimental splits and deposition time are shown in Table 2.1.

The sputter time of Yb is shorter than that of Ni. We have the following options for the deposition sequence of the two metals: 1) sputter Yb first, followed by Ni; 2) co-sputter Yb and Ni first, then close Yb and continue Ni sputtering; 3) sputter Ni first, then sputter Yb.

As discussed in Chapter 1, Si is the dominant diffusion species during $YbSi_{2-x}$ formation; while for NiSi formation, Ni is the dominant diffusion species [15]. If Ni is sputtered first (option 3), Ni would consume the Si first until Ni is depleted, if there is excess Si, Si would then diffuse up and react with Yb. In this case, Yb atoms would not be able to reach the electrode/SiON interface and there would be no work function tuning effect. In the case of option 2, during annealing, Si atoms diffuse up to form $YbSi_{2-x}$ and Ni atoms diffuse down to form Ni silicide; after Yb is fully consumed, Ni would continue to diffuse through the Yb silicide layer and form Ni silicide. During the Ni diffusion process, a small portion of Yb atoms are expected to be pushed down to the silicide/SiON interface, which is similar to dopant segregation phenomenon in Ni FUSI process. This was confirmed with SIMS analysis in the later part of the chapter. The case of option 1 should be similar to option 2; the only difference is just that the only Yb silicide is formed at the beginning of silicidation. One experimental split was prepared to compare the effect of sputter sequence.

Table 3.1. Experimental splits and deposition time for Yb-incorporated Ni FUSI capacitors. There are two options for the deposition sequence of Ni and Yb: (1) Yb first, Ni second; (2) cosputter Yb and Ni followed by Ni only.

No.	Thickness ratio Yb/Ni	DC power on Ni (Watt)	Ni sputter time (s)	DC power on Yb (Watt)	Yb sputter time (s)	Sequence Option
1	0	550	348	0	0	2
2	1/40	550	340	100	8	2
3	1/5	550	290	100	51	2
4	1/5	550	290	100	51	1
5	1/3	550	261	100	77	2
6	1/2	550	232	100	102	2

3.2.3 Silicidation Process Optimization

The nickel silicidation process had been extensively studied. However, for Yb-incorporated NiSi (NiYbSi), optimized process condition needed to be established through preliminary material and electrical characterization. Two major parameters during the rapid thermal annealing (RTP), pressure and temperature, were found to be critical.

NiSi and NiYbSi (Yb:Ni ~ 1:3) were formed by rapid thermal anneal (RTP) at 400 ℃ under 10 Torr or 5×10^{-6} Torr pressure in N_2 ambient. The *C-V* curves are plotted in Fig. 3.2. The curves for NiSi overlap with each other, implying that the pressure does not have much effect on the formation of pure NiSi. For NiYbSi, the sample annealed in high vacuum (5×10^{-6} Torr) has a similar capacitance density as the NiSi control, but the flatband voltage (V_{FB}) is shifted to the left. For NiYbSi annealed at a higher pressure (10 Torr), we observe a distorted *C-V* curve, where there are two regions in the accumulation region. This hump is unlikely due to interfacial states because of its large magnitude. It is due to the incomplete silicidation of the poly-silicon gate, which is confirmed by TEM image in Fig. 3.3.

Fig. 3.3 shows the cross sectional TEM image for the Ni FUSI and Yb-incorporated Ni FUSI capacitors annealed at a pressure of 10 Torr. For the case of pure NiSi, the poly-silicon gate is fully silicided. A relatively smooth and uniform interface is also observed at the NiSi/SiON interface. However for the Yb-incorporated Ni FUSI capacitors, a non-uniformly silicided poly-Si gate is observed. A region of ordered poly-Si structure is observed at the interface which suggests that undoped poly-Si is not fully silicided.

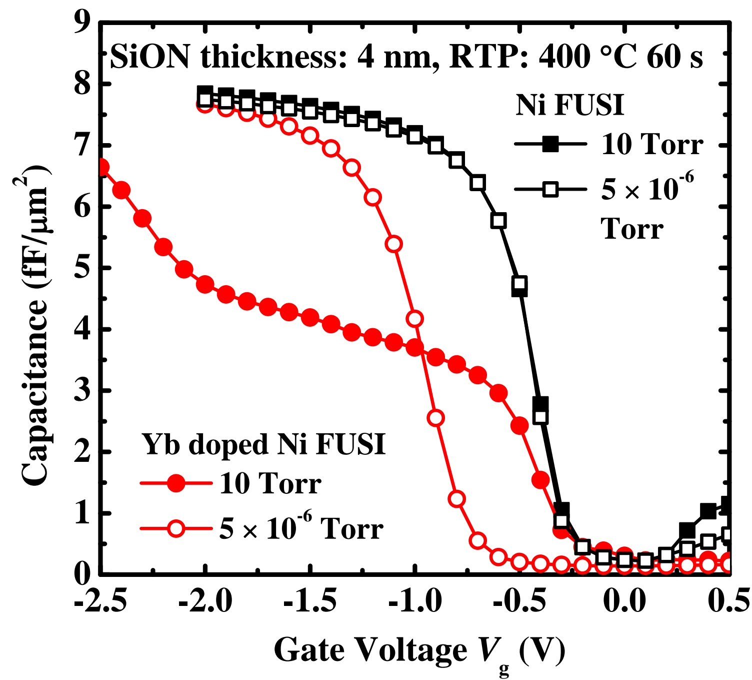

Fig. 3.2. The effect of different pressure during the silicidation process. The *C*-*V* curve of Yb-incorporated NiSi is distorted for the 10 Torr RTP pressue.

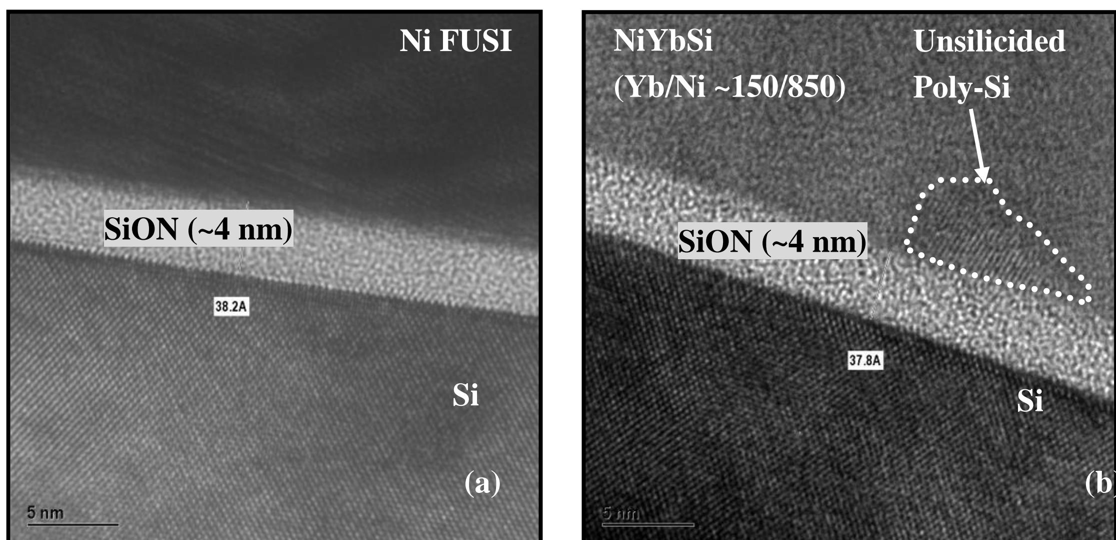

Fig. 3.3. High-resolution TEM results of (a) Ni FUSI and (b) Yb-incorporated Ni FUSI capacitors, annealed at a pressure of 10 Torr.

Temperature is another important parameter for the silicidation process. The criterion is to find the lowest temperature at which the poly-silicon gate can be fully silicided and maintain a low resistivity. Fig 3.4 shows the *C-V* curves of NiSi FUSI capacitors with silicidation temperature of 300 ℃, 400 ℃, and 500 ℃. The overlapping 400 ℃ and 500 ℃ curves exhibit similar EOT as the pure NiSi FUSI control. The distorted 300 ℃ curve shows lower capacitance density and high interfacial trap density, which implies that 300 ℃ is not high enough to fully convert the 90-nm thick poly-silicon into metal silicide. The optimal annealing temperature was determined to be 400 ℃.

Fig. 3.5 shows the phase transformation curve of NiSi and NiYbSi (Yb/Ni ~ 1/5 and 1/3 respectively). The total metal thickness is ~90 nm and poly gate thickness is ~100 nm before the annealing process, for all the three splits with different Yb concentrations. The annealing time for each point was ~30 s. The sheet resistance (R_s) of NiYbSi is lower than that of NiSi below 300 ℃. From 350 to 750 ℃, the resistivity decreases with the increase of Yb/Ni ratio, although the difference is small. NiYbSi has a small R_s of ~ 2 Ω/□ (Yb/Ni ~1:3), slightly lower than that of NiSi (~ 3 Ω/□). When the temperature rises to 800 ℃, the resistance of NiSi increases dramatically due to the formation of high-resistance phase, while the R_s of Yb-incorporated NiSi remains the same.

In summary, the optimized silicidation condition for NiYbSi is: 400 ℃, 5×10^{-6} Torr, 60 s, N_2 ambient.

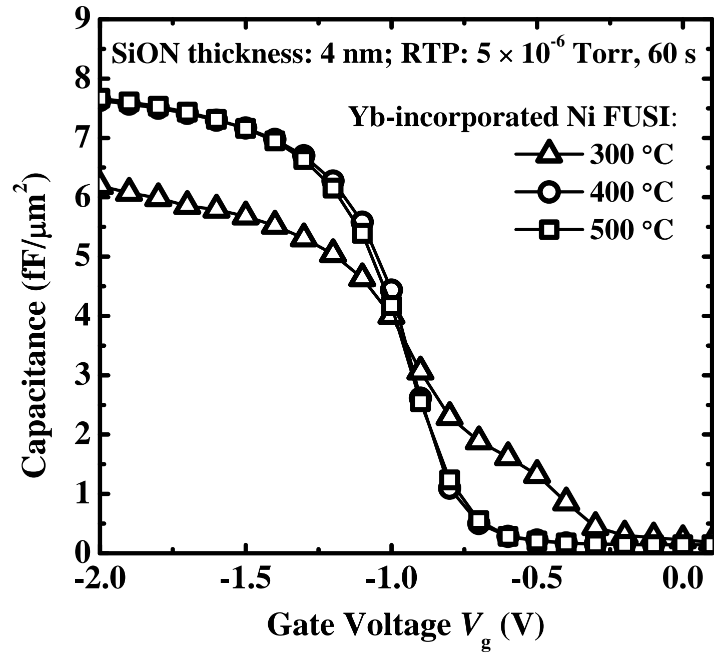

Fig. 3.4. The effect of different annealing or silicidation temperature.

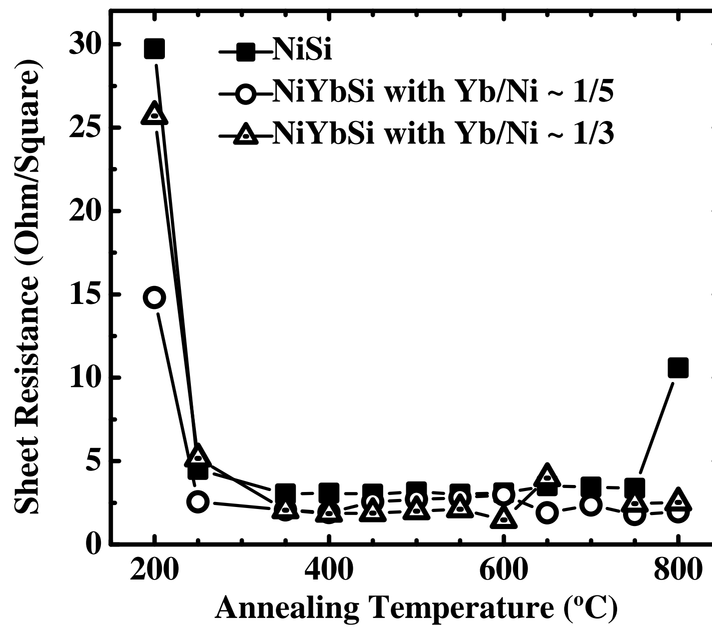

Fig. 3.5. Phase transformation curve for NiSi and NiYbSi (with Yb/Ni deposition ratio ~ 1/5 and 1/3 respectively).

3.3 Device Characterization and Analysis

3.3.1 Material Characterization

In Fig. 3.6(a), the cross sectional TEM micrograph shows that the bulk layer of Yb incorporated NiSi (with Yb/Ni ~1/3) is fully silicided (with a thickness of ~120 nm). It is also observed that there are two different layers in the NiYbSi: top and bottom. The Yb concentrations in the two different layers will be studied by AES, RBS and SIMS. Moreover, a smooth NiYbSi/SiON interface is observed from the XTEM [Fig. 3.6(b)]. An abrupt and smooth interface is found between NiYbSi and SiON. We did not observe any interface adhesion issues found in other reports when work function is modulated by dopants such as As or Sb [16].

Yb concentration in the NiYbSi top layer (Yb/Ni ~ 1/3) is ~12%, as determined by AES (Fig. 3.7).

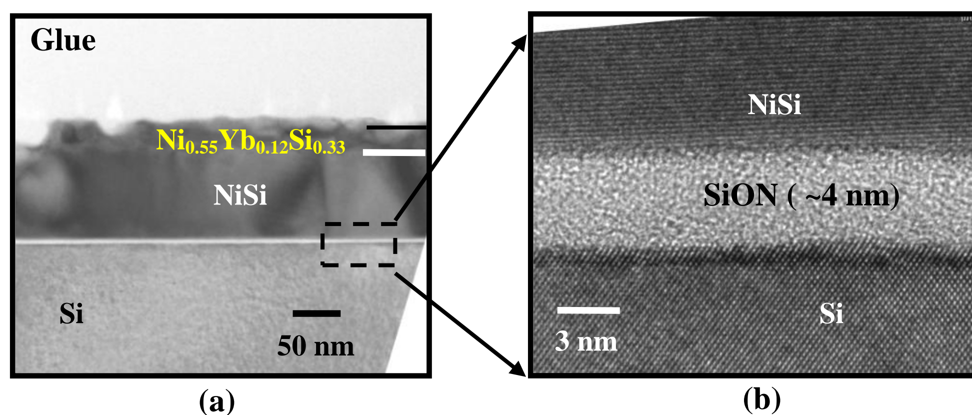

Fig. 3.6. XTEM shows that the bulk layer of NiYbSi (Yb/Ni ~ 1/3) is fully silicided, and the resulting silicide thickness is ~120 nm. Two different layers in the NiYbSi (corresponding to Figs. 3.2 & 3.3) are observed. A smooth NiYbSi/SiON interface is also revealed by XTEM.

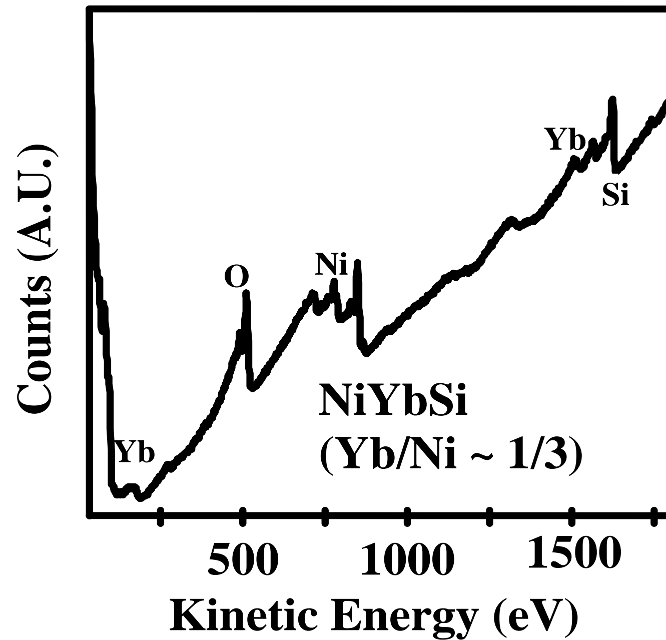

Fig. 3.7. Based on AES, composition of the top layer of NiYbSi (Yb/Ni ~ 1/3) is: $Ni_{0.55}Yb_{0.12}Si_{0.33}$.

Both SIMS (Fig. 3.8) and RBS (Fig. 3.9) analysis of the annealed samples imply that most of Yb in the Yb incorporated NiSi film (with Yb/Ni ~1/3, as defined by Yb/Ni deposition parameters) is distributed in a thin layer at the top surface. SIMS reveals that Yb is piling-up at the NiYbSi/SiON interface after silicidation process. This phenomenon leads to significant change in electrical characteristics. Yb signal cannot be detected by RBS in the bottom layer as the Yb concentration is below the RBS detection limit (< 1% in atomic concentration).

The resulting Yb distribution is correlated to the fact that the dominant diffusion species during the respective NiSi and Yb silicide formation are Ni and Si as discussed in section 3.2.2. Ta was reported to have a similar distribution in NiTaSi during the silicide formation [17].

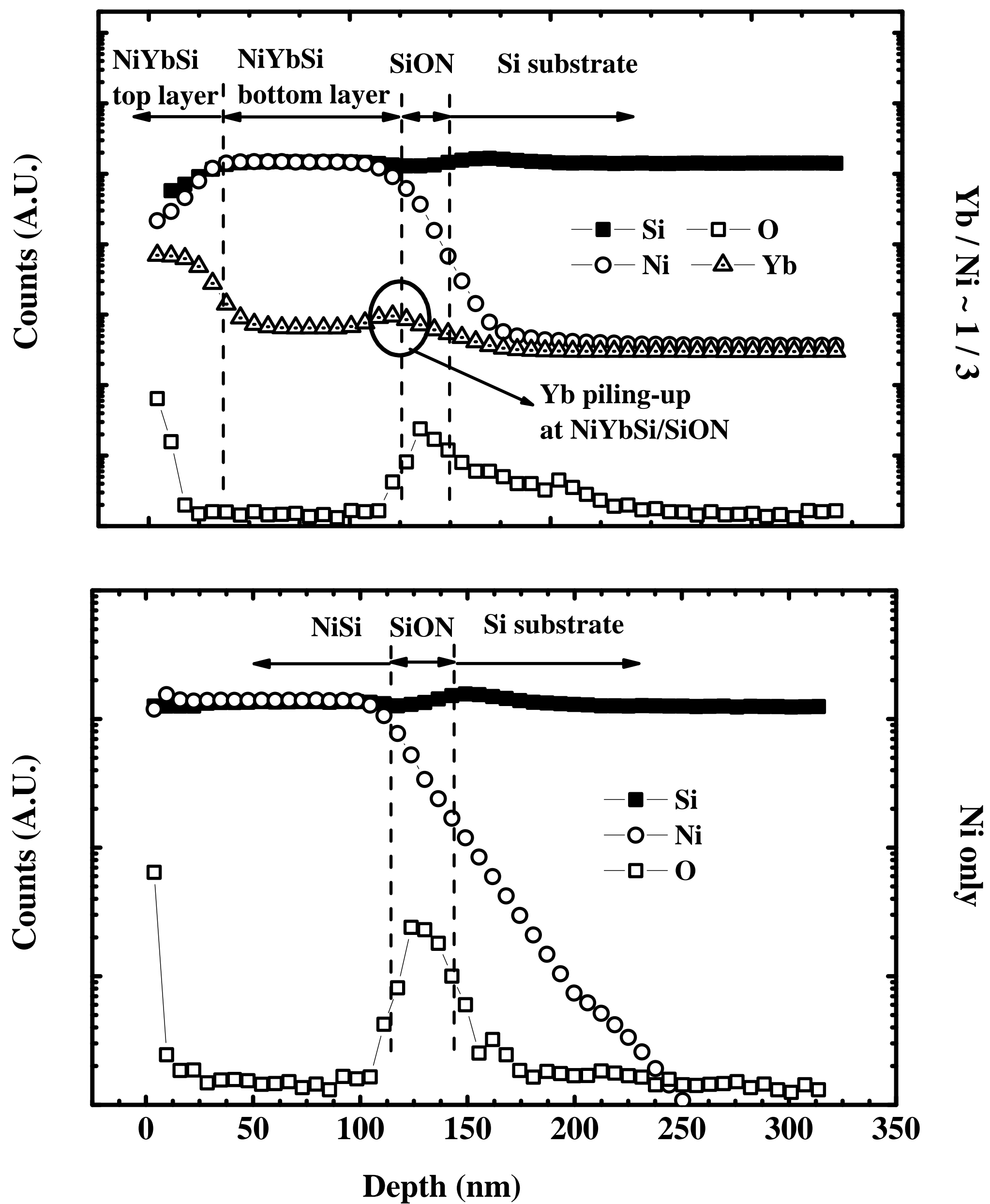

Fig. 3.8. SIMS spectra for NiSi and NiYbSi (Yb/Ni ~ 1/3) shows that Yb is mainly distributed at top layer of silicide. Pile-up of Yb at the NiYbSi/SiON interface is also observed.

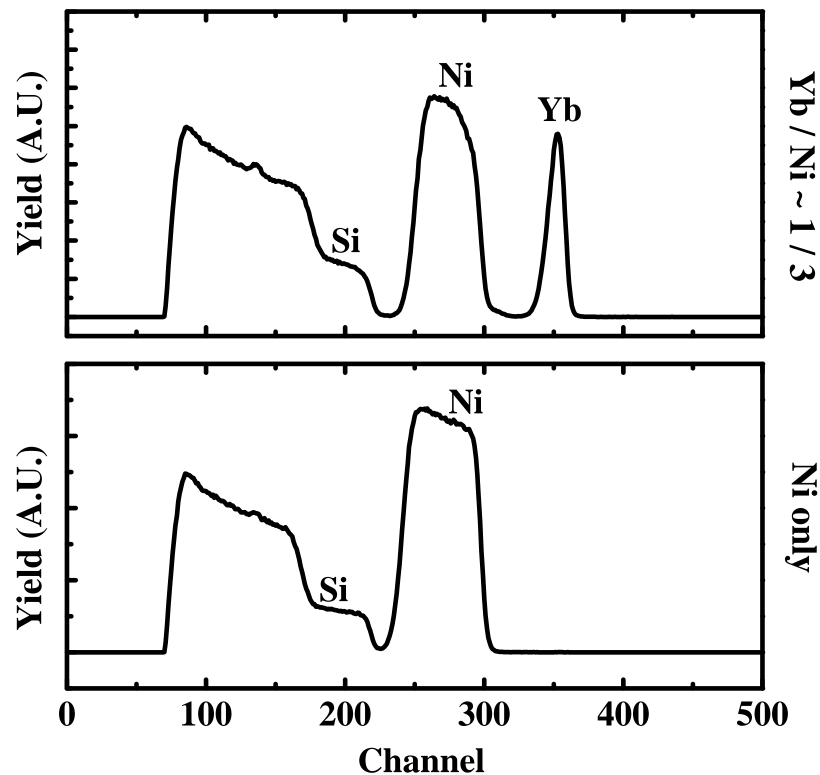

Fig. 3.9. RBS spectrum comparison between NiYbSi (Yb/Ni ~1/3) and NiSi. For Yb-incorporated NiSi, Yb is mainly distributed at top layer of silicide. Yb signal is not detected at the bottom layer probably due to its concentration is below the RBS detection limit (<1 at.%).

The phase control is important in Ni FUSI process. Fig. 3.10 shows XRD spectrums of NiYbSi with different Yb concentrations. The annealing condition is the optimized one discussed earlier in this chapter. It is found that from Ni silicide to Yb-incorprated Ni silicide (Yb/Ni ~1/5 and ~1/3 respectively), their corresponding phases transit from Ni rich Ni_2Si to Ni_3Si_2 and NiSi with increasing Yb content. It has been reported that the Ni silicide phase can be effectively controlled by the Ni/Si thickness ratio [16]. In this work, the deposited Ni is less in the Yb incorporated Ni silicide samples than in the pure NiSi sample and tend to form silicon rich Ni silicide. It was also reported that the resistivity of the silicide thin film increases with the Ni/Si ratio. This is consistent with the sheet resistance measurement (Fig. 3.5).

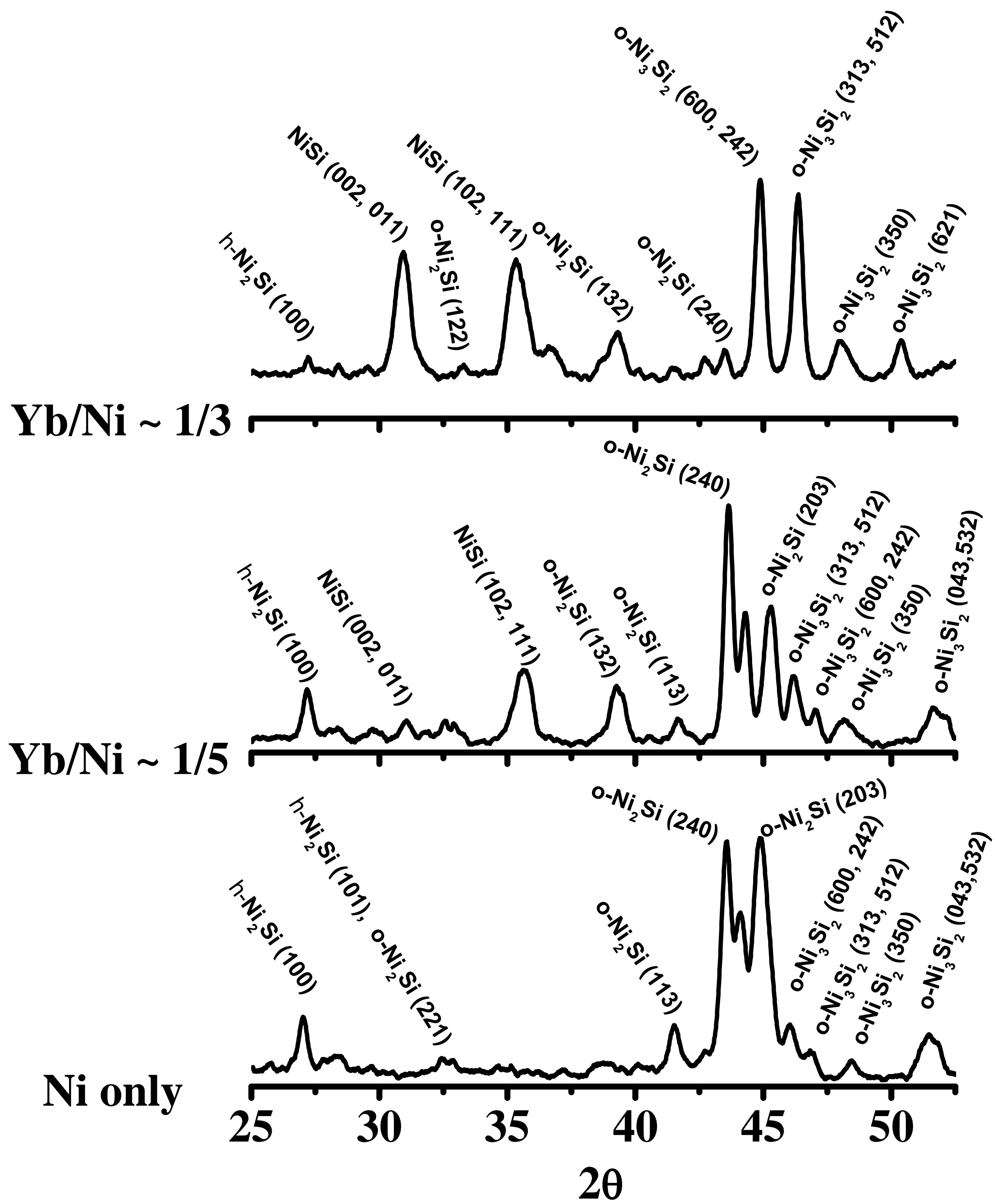

Fig. 3.10. XRD study reveal that from the NiSi to NiYbSi (Yb/Ni ~1/5 and ~1/3 respectively), the phase transits from Ni rich Ni_2Si to Ni_3Si_2 and NiSi.

3.3.2 Work Function Tunability

Fig. 3.11(a) shows the high-frequency *C-V* measurement for MOS capacitors with both NiYbSi (Yb/Ni ~ 1/3) and NiSi electrodes. NiYbSi (Yb/Ni~1/3) demonstrates a negative V_{FB} shift of about -500 mV compared to Ni FUSI, while the EOT values are the same. This significant V_{FB} shift is much larger than the 100 mV reported in [16], thus it cannot be attributed to the change of the phase of Ni silicide. Yb piling-up at the NiYbSi/SiON interface (Fig. 3.8) is believed to be responsible for the V_{FB} shift. The nice fitting between the measured and simulated C-V data for the capacitors suggests the negligible interface trap density D_{it} of the MOS capacitor devices.

The work function of all the experimental splits in this work were extracted from the V_{FB} vs. EOT plot which eliminates the contribution of oxide fixed charge to the V_{FB} of MOS capacitor to obtain the accurate work function. Fig. 3.11(b) shows an example of work function extraction for the case of Yb/Ni ~ 1/3, whose *C-V* is shown in Fig. 3.11(a). The extracted work function Φ_m is 4.22 eV, which is desirable for n-MOSFETs application.

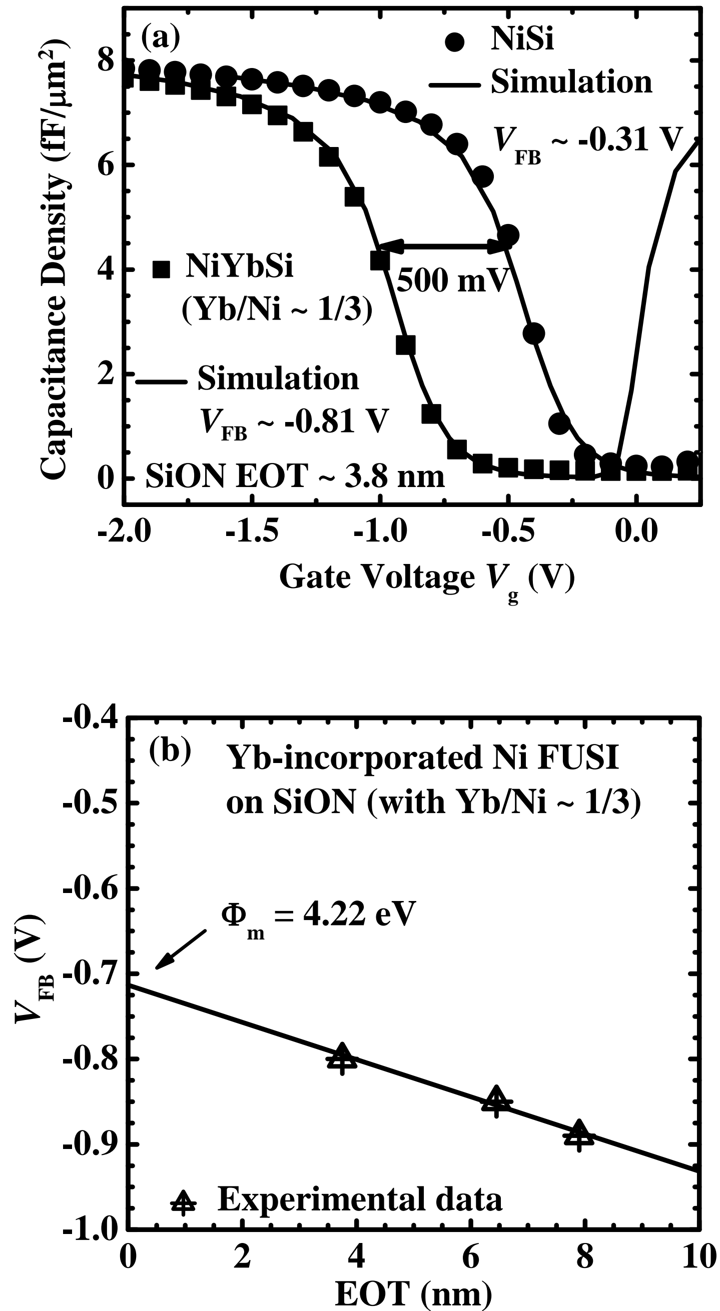

Fig. 3.11. (a) Measured and simulated C-V data for capacitors with NiYbSi (Yb/Ni ~1/3) and NiSi gate electrodes. Deposited SiON thickness is ~ 4nm. No change in EOT is observed with addition of Yb. (b) The plot of EOT vs. V_{FB} for the devices with NiYbSi (with Yb/Ni ~ 1/3) gate electrode. The work function extracted is 4.22 eV on SiON, fixed charge $Q_{ox} / q = 4.59 \times 10^{11}$ cm^{-2}.

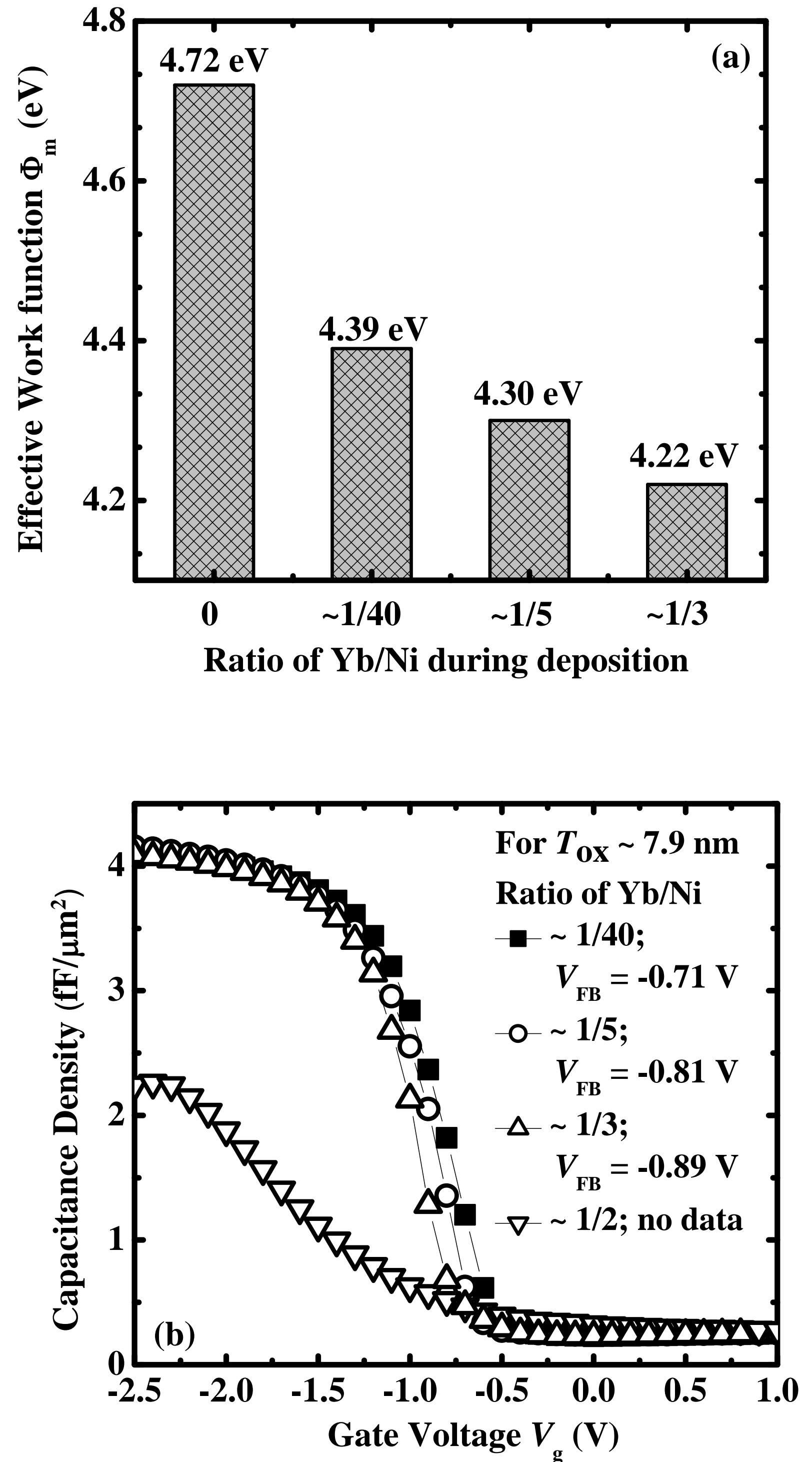

Fig. 3.12. (a) Work function of Yb-incorporated Ni FUSI is tunable by modifying Yb incorporation during deposition. (b) *C-V* plots of Yb incorporated Ni FUSI with different YB/Ni ratios. It is noted that excessive Yb might degrade the device dielectric (e.g. Yb/Ni ~1/2).

Using the same method, the Φ_m of other experimental splits were obtained as shown in Fig. 3.12. It was found that Φ_m of Yb incorporated NiSi could be tuned by

modifying the amount of Yb introduced during metal deposition, from 4.22 eV to 4.72 eV. Fig. 3.12(b) shows the gradual shift of flat band voltage by *C-V* plots. It is noted that for the case where Yb/Ni ~1/2, the curve is distorted due to large leakage current. Considering the reaction between Yb and SiO_2, which has been discussed in Chapter 2, this should be due to the degradation the SiON dielectric by excessive Yb.

The work function tunability is due to the low work function of Yb. With the increased Yb/Ni ratio, more Yb is piled up at the metal gate/SiON interface and lowers the Φ_m of NiYbSi alloy. The lowering of Φ_m leads to lowering of electron barrier between the gate electrode and dielectric as $\Phi_B = \Phi_m - E_{c,\,SiON}$. Excessive Yb at interface should be prevented to avoid degradation of the dielectric.

It is also interesting to know whether the sequence during the sputtering of the two metals would affect the outcome. Fig. 3.13 shows that the *C-V* characteristics from Yb incorporated Ni FUSI devices fabricated by two different methods are comparable, i.e., by co-sputter Ni and Yb or by sequential sputter Yb and Ni.

Another way to determine the flatband voltage makes use of the Fowler-Nordheim plot, which is a plot of ln (J_{FN}/E_{ox}^2) versus $1/E_{ox}$. The barrier height Φ_B between the electrode and dielectric can be obtained from the slope and intercept in the plot [19]. With Φ_B and the conduction band of the SiON dielectric, the work function of gate electrode can be easily obtained. To confirm the work function shift, we compare the F-N plot for the devices with NiSi and NiYbSi gate electrodes in Fig. 3.11. The work function difference obtained from this plot is about 0.54 eV, which is consistent with their *C-V* data.

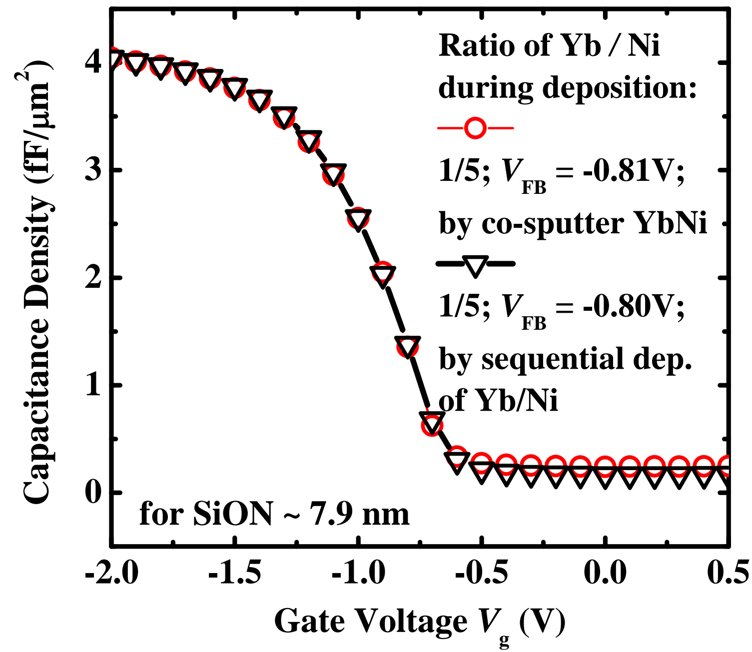

Fig. 3.13. *C-V* characteristics are comparable for Yb incorporated Ni FUSI devices fabricated by two different methods, co-sputter YbNi and sequential sputter Yb and Ni (Yb first).

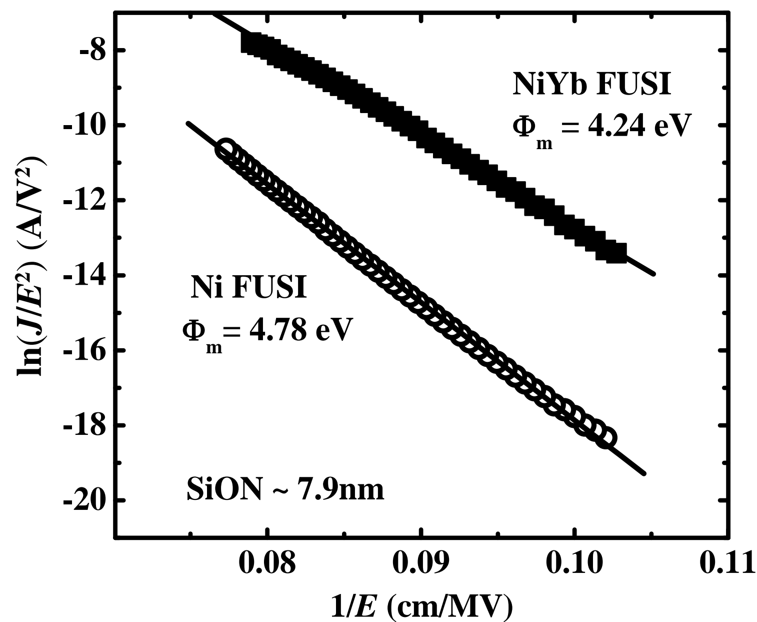

Fig. 3.14. FN plots for the devices with Ni FUSI and NiYb FUSI gate.

3.3.3 Reliability Assessments

Time zero break down (TZBD), charge trapping, and time dependant dielectrics breakdown (TDDB) characteristics (under gate injection, and constant voltage FN stress @ -6.5 V) of the devices with Yb incorporated Ni FUSI are shown in Figs. 3.15, 3.16 and 3.17 respectively, and are compared to those Ni FUSI devices.

The TZBD plot in Fig. 3.15(a) shows that with NiYbSi (Yb/Ni ~ 1/3), the break down voltage is statistically slightly increased with $V_g - V_{FB}$. This is probably due to the suppressed Ni diffusion into SiON gate dielectric as a result of the Yb piling up at the interface. Fig 3.15(b) shows a typical *J-V* sweep for the device with NiYbSi gate.

Fig. 3.16 shows the typical 'current density'-time characteristics for devices with NiYbSi and NiSi under constant voltage FN stress (gate injection). The higher FN current in NiYbSi devices is attributed to its lower electron barrier height as compared to that of NiSi gated devices.

Fig. 3.17 shows the TDDB measurement to access the time dependent reliability. It is seen that the Yb incorporated Ni FUSI devices show comparable reliability characteristics to Ni FUSI Breakdown time is slightly longer for NiSi gated MOS capacitors, but the difference is very small. It is seen that the Ni-Yb FUSI devices show comparable reliability characteristics to the Ni FUSI.

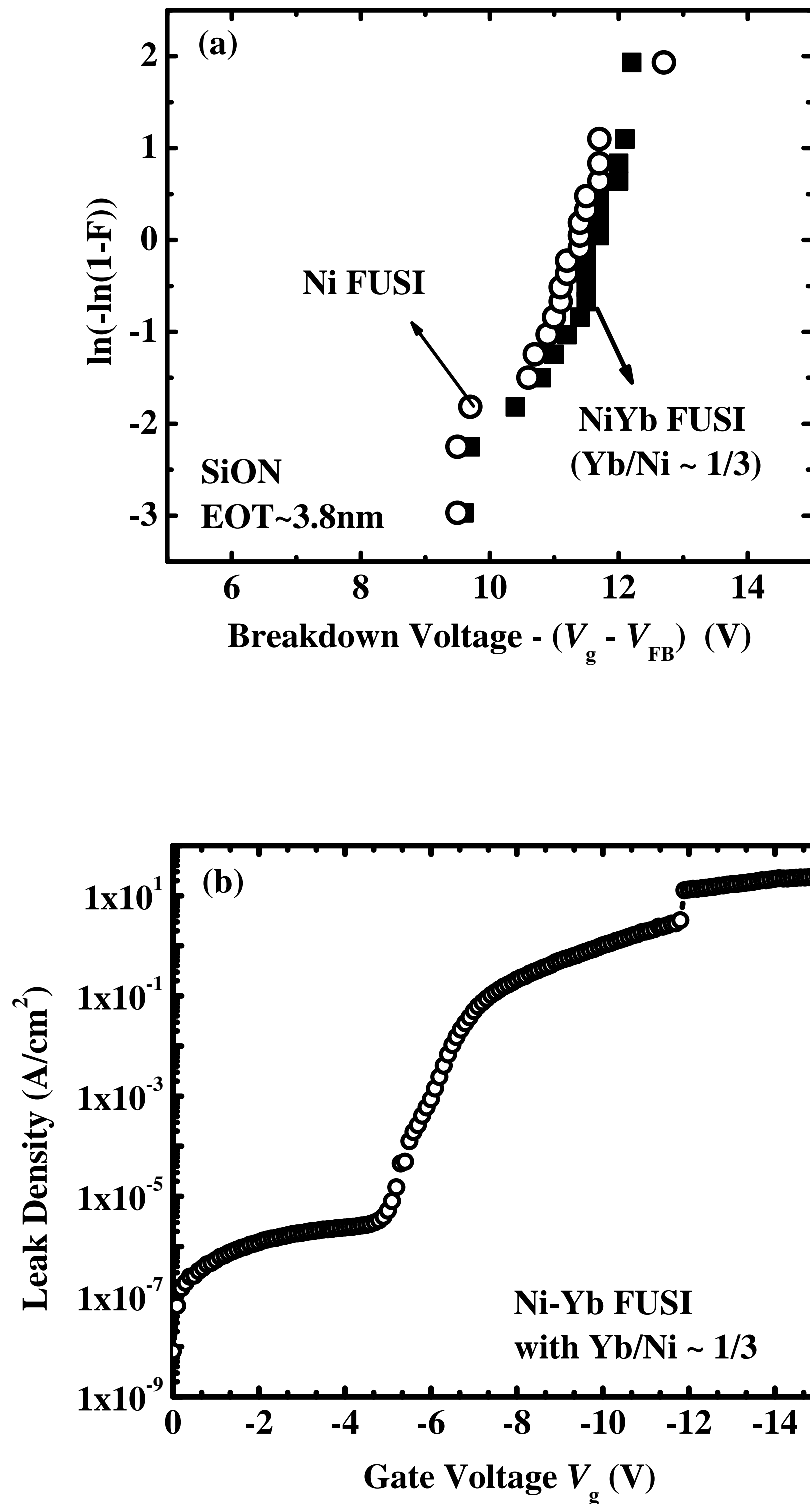

Fig. 3.15. (a) TZBD comparison between the devices with Ni FUSI and NiYb FUSI electrodes (on SiON dielectric). (b) A typical *J-V* sweep for the device with NiYbSi gate.

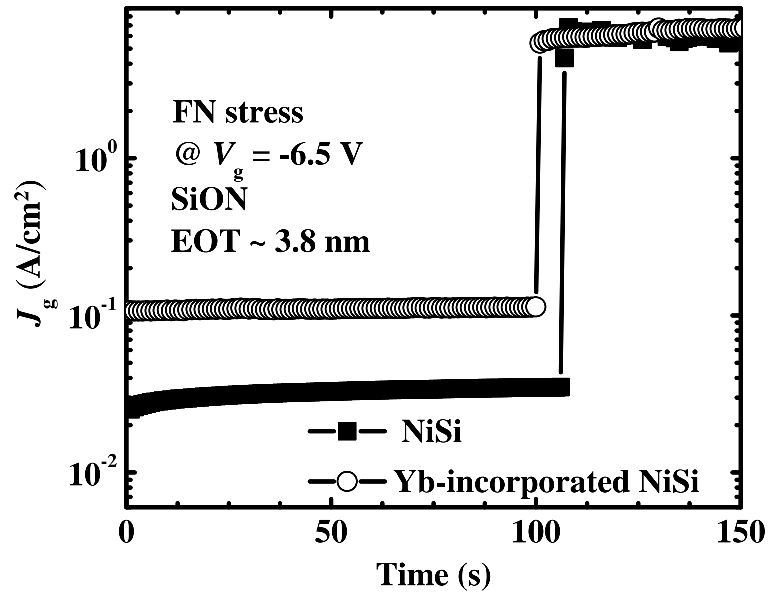

Fig. 3.16. 'Current density'-time characteristics for Ni FUSI and Yb-incorporated Ni FUSI devices under constant voltage FN stress (gate injection).

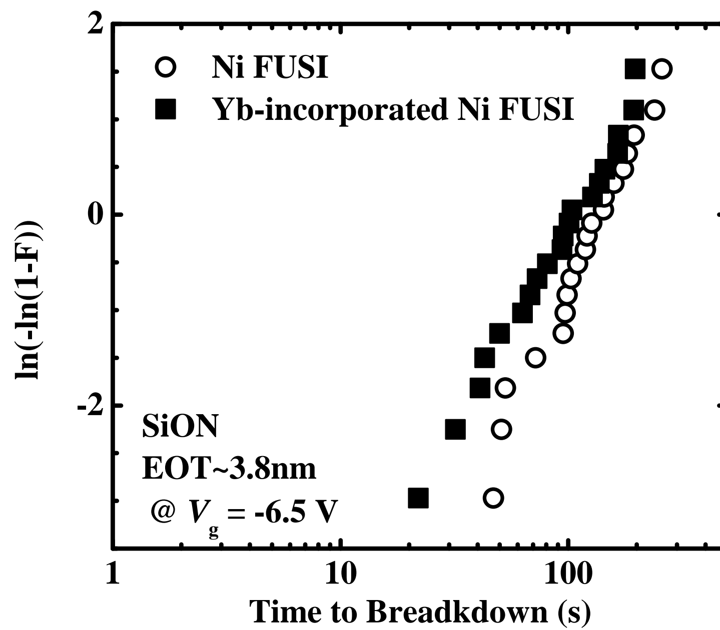

Fig. 3.17. TDDB (under gate injection and FN-CVS) comparison between the devices with NiYbSi and NiSi gate electrode (on SiON dielectric).

3.4 CMOS Integration Scheme

Integration of dual metal gate electrodes into the CMOS process is a major challenge for the development of metal gate technology. The criteria for ideal dual metal gate integration process include: 1) obtain dual work function for n-FET and p-FET respectively; 2) without any process-induced damages or reliability concerns to the gate oxide; and 3) compatibility to conventional process.

The FUSI gate process, where the conventional poly-Si gate is used as the bottom protective layer, is compatible with the conventional CMOS process flow. As illustrated in Fig. 3.18, a poly-Si gated CMOSFET is first fabricated using a conventional gate-first CMOS process. After source/drain silicidation, the devices are wrapped by the post-metal-dielectric (PMD). A planarization step is then performed using oxide CMP before the hard mask (HM) on top of poly-Si is exposed. Then the NMOS region (p-well) is covered by photo resist for protection. The hard mask is then etched away and the poly-Si gate in PMOS region is exposed. Then the metal (e.g. Pt) is deposited and annealed to FUSI the poly of p-FET. After removing the un-reacted metal, PMD is deposited again and polished by CMP. Photo resist is then applied and patterned to protect the p-FET region. The hard mask on n-FET is etched away to expose the poly-Si. Metal (e.g. Yb-incorporated Ni) is then deposited and annealed to form FUSI for n-FET. Residual metal is removed by selective etch.

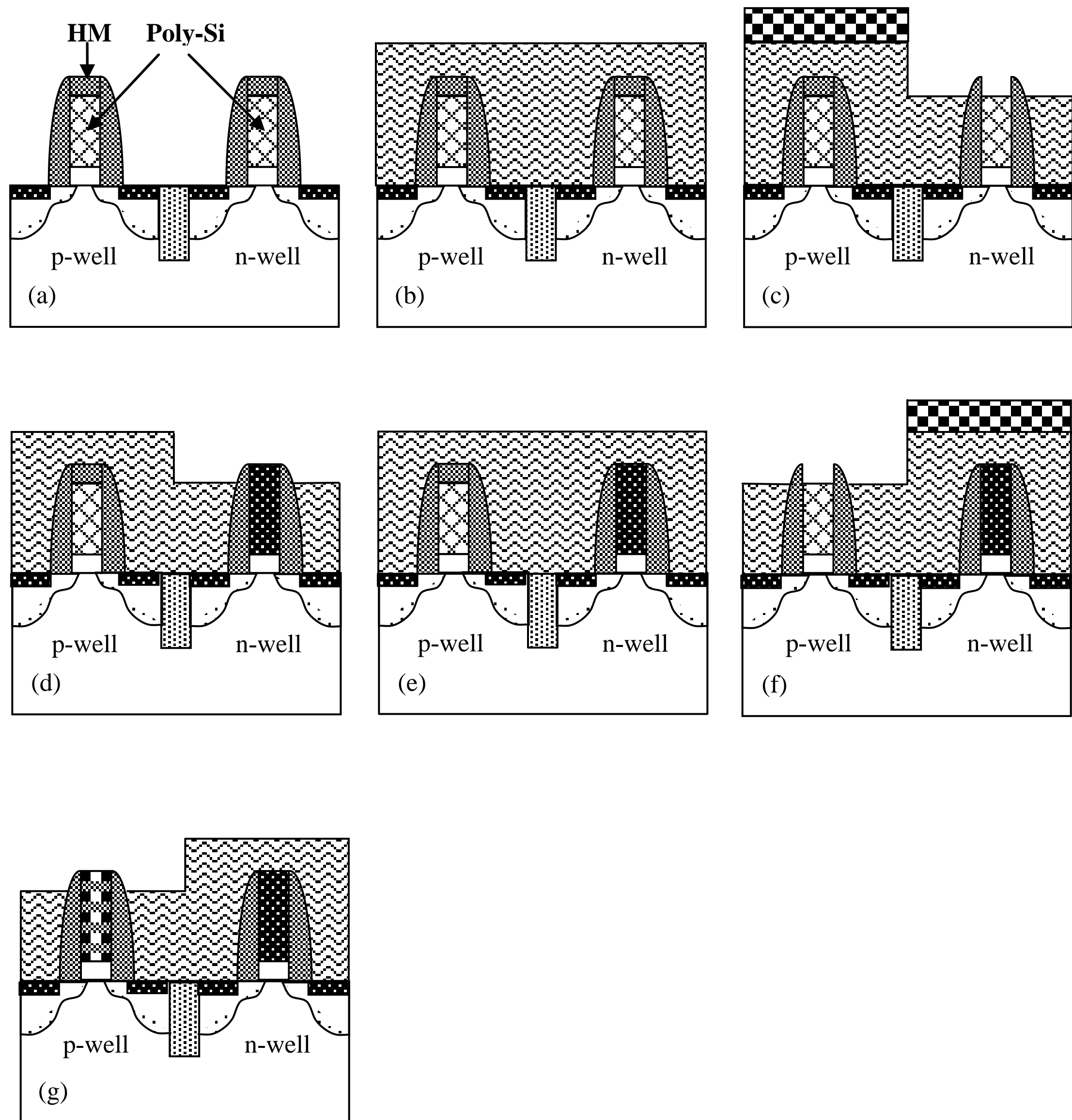

Fig. 3.18. Proposed CMOS integration scheme using Yb-incorporated Ni FUSI for n-FETs, and Pt FUSI for p-FETs. (a) CMOS fabrication conventionally using undoped poly-Si gate, after source/drain silicidation; (b) oxide reflow and chemical mechanical planarization (CMP); (c) lithography to mask n-FET region and etch the hard mask to expose the poly of p-FET and hard mask stripping; (d) photo resist strip and FUSI the poly-Si of p-FET (e.g. $PtSi_x$); (e) oxide reflow and CMP; (f) lithography to mask n-FET region and etch the hard mask to expose the poly of n-FET; (g) photo resist strip and FUSI the poly-Si of n-FET (e.g. Yb-incorporated Ni FUSI).

3.5 Investigation of Work Function Tuning Mechanism

When metal and dielectric are in contact, the interface states would be created and charge transfer could occur across these interface states, leading to the formation of a dipole layer which consequently results in Fermi level pinning (FLP) of metal gate work function [20, 21]. Metal induced gap states (MIGS) model, considering the interface dipole due to intrinsic interface states only, was developed by Robertson to predict the effective metal work function [22]:

$$\Phi_{m,eff} = S(\Phi_m - \Phi_{Si}) + \Phi_{Si}\,, \tag{3.1}$$

where S is the Schottky pinning parameter, which determines the strength of FLP effect. W. Monch found that the parameter of S empirically obeys the following equation [23]:

$$S = \frac{1}{1+0.1(\varepsilon_\infty - 1)^2}\,, \tag{3.2}$$

where ε_∞ stands for the electronic part of the dielectric constant. The smaller the S parameter for a material, the more effective this material is to pin the metal Fermi level. On a SiO_2 dielectric, the FLP effect would be negligible due to the large S value of 0.95. On the other hand, significant FLP would be expected on HfO_2 because the S values are as small as 0.52. Such a model has been successful in fitting experimental results in many metal-dielectric systems.

It is assumed in the MIGS model that metal-dielectric interface is perfect without any physical/chemical defects. However, extrinsic states created at the metal/dielectric interface are also found to be responsible for the instability of Φ_m instability under high temperature anneal [21].

To explore the work function tuning effect on high-κ dielectrics, we fabricated MOS capacitors with HfSiON high-κ dielectric and NiYbSi FUSI gate electrode. The process was exactly the same as MOS capacitors with SiON dielectric, except for the gate dielectric deposition step. Fig. 3.19 shows the high-frequency *C-V* measurement for MOS capacitors with HfSiON dielectric. The 3.5-nm EOT is comparable to that of the SiON capacitors shown in Fig. 3.11. The Yb/Ni is 1/3, which is the same as in Fig. 3.11(a). However, the Yb incoporated Ni FUSI demonstrates a negative V_{FB} shift of only ~ -100 mV on HfSiON dielectric. This V_{FB} shift is much smaller than the 500 mV for SiON. The MIGS model is able to attribute the small V_{FB} shift to the small S factor of high-κ dielectrics.

As shown in Fig. 3.19(b), from SiON to HfSiON dielectric, V_{FB} shift is negative for NiSi gate electrode, this can be explained by the MIGS model that high-κ materials usually suffer from FLP to the midgap of silicon due to large S value. However, the V_{FB} shift is positive for NiYbSi gate electrode; the opposite shift direction cannot be explained by MIGS model. Other mechanisms have to be taken into account.

The initial motivation to incorporate Yb into NiSi FUSI was to form NiYbSi of low work function. However, as discussed in the physical characterizations, most of Yb in the Yb incorporated NiSi film is distributed in a thin layer at the top surface. Only a small amount of Yb piles up at the NiYbSi/SiON interface after the silicidation process. It is unlikely that the small amount of Yb has changed the intrinsic metal work function of the NiSi electrode. As mentioned in section 3.3.2, this significant V_{FB} shift cannot be explained by the change of phase of Ni silicide either. It seems to be more related to the built-in potential at the NiYbSi/SiON interface.

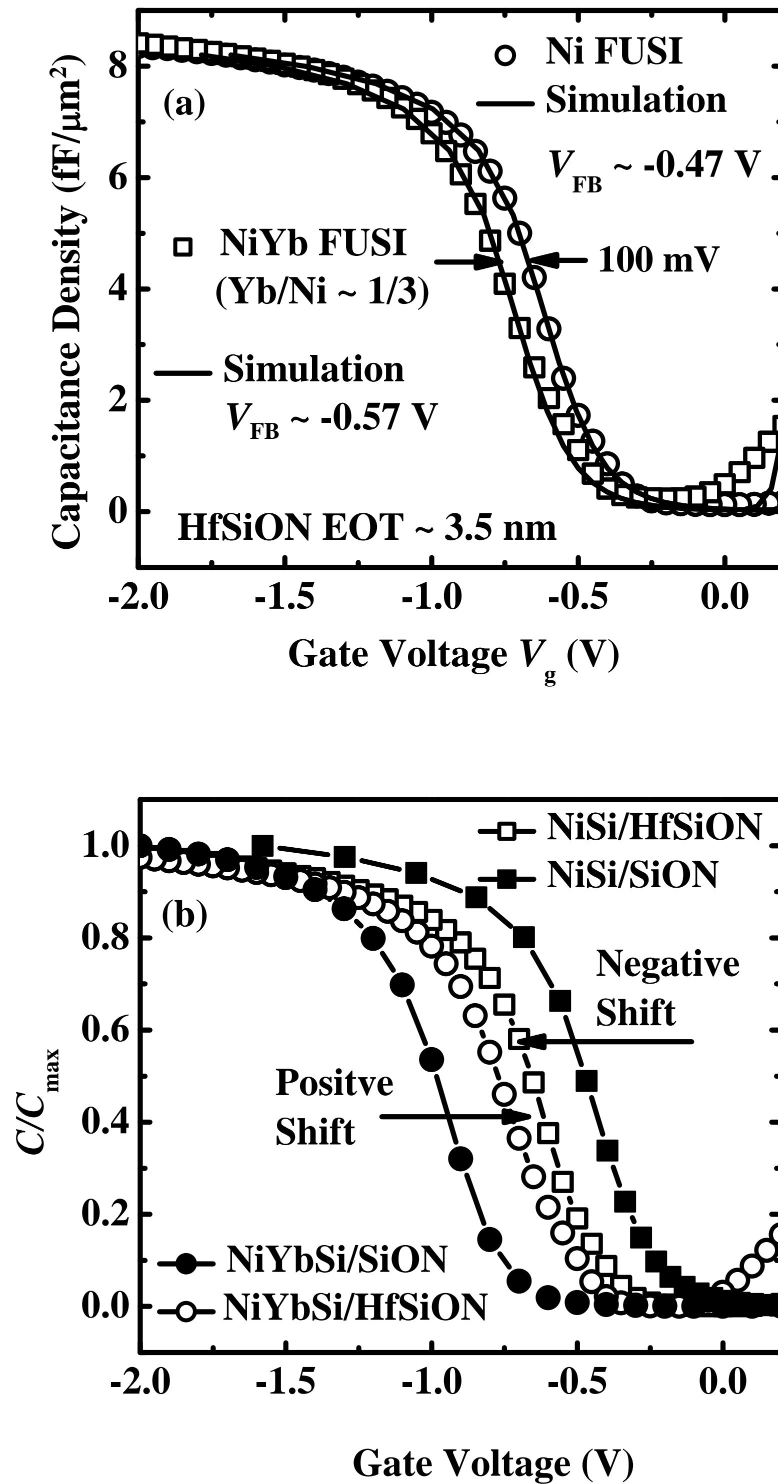

Fig. 3.19. (a) Measured and simulated *C-V* data for capacitors with Ni-Yb FUSI (Yb/Ni ~1/3) and Ni FUSI gate electrodes. The EOT of HfSiON is ~ 3.5nm. The V_{FB} shift is 0.1 V. (b) From SiON to HfSiON dielectric, V_{FB} shift is negative for NiSi gate electrode, and positive for NiYbSi gate electrode.

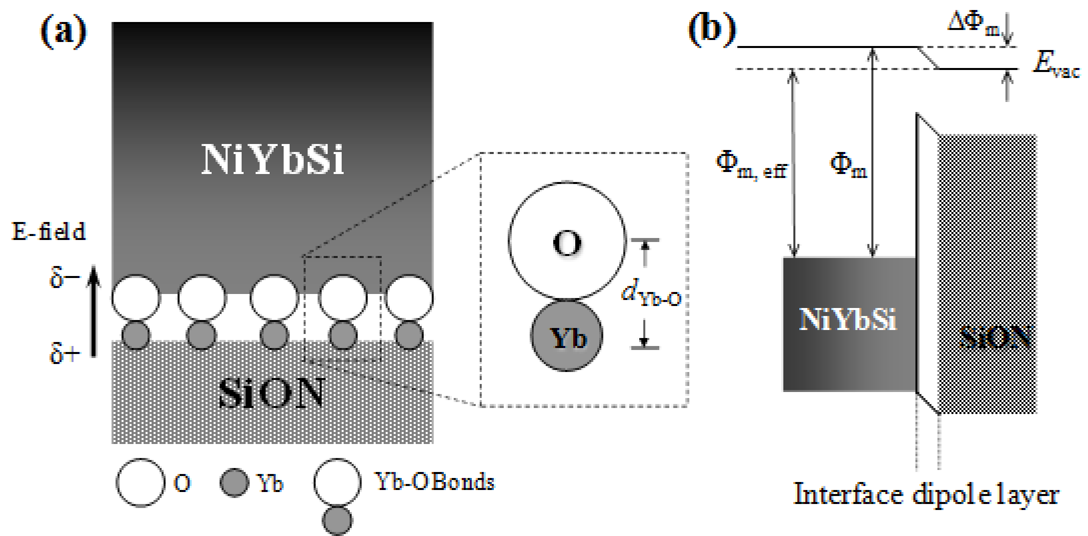

Fig. 3.20. (a) A schematic showing highly polarized Yb-O dipoles at the NiYbSi/SiON interface. (b)The Φ_m of NiYbSi is reduced due to the presence of dipole at the NiYbSi and SiON interface.

Lim et. al. proposed an interface dipole model to explain the work function tunability by inserting an ultra-thin rare earth dielectric interlayer between metal gate and SiO_2 [24]. According to the model, it was proposed that a highly polarized Ln-O dipole layer exists between the gate electrode and dielectric and this dipole layer creates a localized electric field that modulates the gate work function. The highly polarized Ln-O dipole originates from the high degree of polarization between lanthanoid and oxygen ions due to the large electronegativity difference between lanthanoid and oxygen ions. The amount of ionicity between Ln and O ions in an Ln-O-Si (or lanthanoid silicate) bonding is reported to be larger than that in a pure Ln-O (or Lanthanoid oxide) bonding [25]. The increase in Ln-O ionicity is accompanied by a corresponding increase in covalence between the Si and O ions in the lanthanoid silicate bond.

The segregated Yb atoms at the NiYbSi/SiO_2 interface can be the analogue of the rare earth dielectric interlayer in Lim's model. The segregated Yb reacts with SiON and form Yb-O-Si bond, which leads to highly polarized Yb-O bond pointing toward the gate electrode. Fig. 3.20 (a) and 3.20 (b) depict the interface dipole layer schematically, and highlight how the effective Φ_m is reduced by $\Delta\Phi_m$ in an energy diagram because of the dipole layer, respectively.

This model explains the positive V_{FB} shift direction from SiON to HfSiON for NiYbSi gated MOS capacitors shown in Fig. 3.19(b). For HfSiON dielectric, it is much more difficult to form Yb-O-Si bond at the interface than for SiON because of the existence of Hf-O-Si bond. Therefore, the density of highly polarized Yb-O bonds would be much lower and thus the V_{FB} shift is much smaller comparing to the case of SiON.

3.6 Conclusion

In summary, we successfully demonstrated a novel method to tune the work function of NiSi FUSI gate by incorporating ytterbium, which is a lanthanoid element. The silicide formation process was optimized and the material and electrical characteristics have been systematically studied. The results show that the work function of the Yb-incorporated Ni FUSI gate can be continuously tuned by varying the ytterbium concentration, and a work function value of 4.22 eV can be obtained, which meets the requirement for N-MOSFET. TZBD and TDDB studies showed comparable reliability performance to the conventional NiSi FUSI. A CMOS integration scheme is also proposed. Further investigation showed that this method is less effective on HfSiON high-κ dielectric. An interface dipole model was discussed to explain the work function tuning mechanism.

References

[1] W. Maszara, Z. Krivokapic, P. King, J. Goo, and M. Lin, "Transistors with dual work function metal gates by single full silicidation (FUSI) of polysilicon gates," *International Electron Devices Meeting Tech. Dig.*, pp. 367-370, 2002.

[2] B. Tavel, T. Skotnicki, G. Pares, N. Carriere, M. Rivoire, F. Leverd, C. Julien, J. Torres, and R. Pantel, "Totally Silicided ($CoSi_2$) Polysilicon: A Novel Approach to Very Low-Resistive Gate (~ 2Ω) Without Metal CMP Nor Etching," *International Electron Devices Meeting Tech. Dig.*, pp. 825-830, 2001.

[3] D. Yu, C. Wu, C. Huang, A. Chin, W. Chen, C. Zhu, M. Li, and D. Kwong, "Fully silicided NiSi and germanided NiGe dual gates on SiO_2 n-and p-MOSFETs," *IEEE Electron Device Letters,* vol. 24, pp. 739-741, 2003.

[4] K. Anil, A. Veloso, S. Kubicek, T. Schram, E. Augendre, J. de Marneffe, K. Devriendt, A. Lauwers, S. Brus, and K. Henson, "Demonstration of fully Ni-silicided metal gates on HfO_2 based high-κ gate dielectrics as a candidate for low power applications," *Symposium on VLSI Technology Tech. Dig.,* pp. 190-191, 2004.

[5] E. Gusev, C. Cabral Jr, B. Under, Y. Kim, K. Maitra, E. Carrier, H. Nayfeh, R. Amos, G. Biery, and N. Bojarczuk, "Advanced gate stacks with fully silicided (FUSI) gates and high-κ dielectrics: enhanced performance at reduced gate leakage," *International Electron Devices Meeting Tech. Dig.*, pp. 79-82, 2004.

[6] K. Hosaka, T. Kurahashi, K. Kawamura, T. Aoyama, Y. Mishima, K. Suzuki, and S. Sato, "A comprehensive study of fully-silicided gates to achieve wide-range work function differences (0.91 eV) for high-performance CMOS devices," *Symposium on VLSI Technology Tech. Dig.*, pp. 66-67, 2005.

[7] J. Kedzierski, D. Boyd, P. Ronsheim, S. Zafar, J. Newbury, J. Ott, C. Cabral Jr, M. Ieong, W. Haensch, and S. Res, "Threshold voltage control in NiSi-gated

MOSFETs through silicidation induced impurity segregation (SIIS)," *International Electron Devices Meeting Tech. Dig.*, pp. 13.3, 2003.

[8] M. Terai, K. Takahashi, K. Manabe, T. Hase, T. Ogura, M. Saitoh, T. Iwamoto, T. Tatsumi, and H. Watanabe, "Highly reliable HfSiON CMOSFET with phase controlled NiSi (NFET) and Ni_3Si (PFET) FUSI gate electrode," *Symposium on VLSI Technology Tech. Dig.*, pp. 68-69, 2005.

[9] K. Takahashi, K. Manabe, T. Ikarashi, N. Ikarashi, T. Hase, T. Yoshihara, H. Watanabe, T. Tatsumi, and Y. Mochizuki, "Dual workfunction Ni-silicide/HfSiON gate stacks by phase-controlled full-silicidation (PC-FUSI) technique for 45nm-node LSTP and LOP devices," *International Electron Devices Meeting Tech. Dig.,* pp. 91-94, 2004.

[10] Y. Kim, C. Cabral Jr, E. Gusev, R. Carruthers, L. Gignac, M. Gribelyuk, E. Cartier, S. Zafar, M. Copel, and V. Narayanan, "Systematic study of work function engineering and scavenging effect using NiSi alloy FUSI metal gates with advanced gate stacks," *International Electron Devices Meeting Tech. Dig.,* pp. 645-648, 2005.

[11] J. Kedzierski, D. Boyd, C. Cabral Jr, P. Ronsheim, S. Zafar, P. Kozlowski, J. Ott, and M. Ieong, "Threshold voltage control in NiSi-gated MOSFETs through SIIS," *IEEE Transactions on Electron Devices,* vol. 52, pp. 39-46, 2005.

[12] T. Hoffmann, A. Veloso, A. Lauwers, H. Yu, H. Tigelaar, M. Van Dal, T. Chiarella, C. Kerner, T. Kauerauf, and A. Shickova, "Ni-based FUSI gates: CMOS Integration for 45nm node and beyond," *International Electron Devices Meeting Tech. Dig.,* pp. 1-4, 2006.

[13] C. Ren, H. Yu, X. Wang, H. Ma, D. Chan, M. Li, Y. Yeo, C. Tung, N. Balasubramanian, and A. Huan, "Thermally robust $TaTb_xN$ metal gate

electrode for n-MOSFETs applications," *IEEE Electron Device Letters,* vol. 26, pp. 75-77, 2005.

[14] C. Ren, D. Chan, X. Wang, B. Faizhal, M. Li, Y. Yeo, A. Trigg, A. Agarwal, N. Balasubramanian, and J. Pan, "Physical and electrical properties of lanthanide-incorporated tantalum nitride for n-channel metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters,* vol. 87, pp. 073506, 2005.

[15] K. Maex and M. Van Rossum, *Properties of metal silicides*, INSPEC, 1995.

[16] J. Kittl, A. Veloso, A. Lauwers, K. Anil, C. Demeurisse, S. Kubicek, M. Niwa, M. van Dal, O. Richard, and M. Pawlak, "Scalability of Ni FUSI gate processes: Phase and V_t control to 30 nm gate lengths," *Symposium on VLSI Technology Tech. Dig.*, pp. 72-73, 2005.

[17] M. Sun, M. Kim, J. Ku, K. Roh, C. Kim, S. Youn, S. Jung, S. Choi, N. Lee, and H. Kang, "Thermally robust Ta-doped Ni SALICIDE process promising for sub-50 nm CMOSFETs," *Symposium on VLSI Technology Tech. Dig.*, pp. 81-82, 2003.

[18] S. Zhu, J. Chen, M. Li, S. Lee, J. Singh, C. Zhu, A. Du, C. Tung, A. Chin, and D. Kwong, "N-type Schottky barrier source/drain MOSFET using ytterbium silicide," *IEEE Electron Device Letters,* vol. 25, pp. 565-567, 2004.

[19] D. Schroder, *Semiconductor material and device characterization,* Wiley-interscience, 2006.

[20] Y. Yeo, T. King, and C. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology," *Journal of Applied Physics,* vol. 92, pp. 7266, 2002.

[21] H. Yu, C. Ren, Y. Yeo, J. Kang, X. Wang, H. Ma, M. Li, D. Chan, and D. Kwong, "Fermi pinning-induced thermal instability of metal-gate work functions," *IEEE Electron Device Letters,* vol. 25, pp. 337-339, 2004.

[22] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 18, pp. 1785, 2000.

[23] W. Monch, "Role of virtual gap states and defects in metal-semiconductor contacts," *Physical Review Letters,* vol. 58, pp. 1260-1263, 1987.

[24] A. Lim, R. Lee, G. Samudra, D. Kwong, and Y. Yeo, "Novel Rare-Earth Dielectric Interlayers for Wide NMOS Work-Function Tunability in Ni-FUSI Gates," *IEEE Transactions on Electron Devices,* vol. 55, pp. 2370-2377, 2008.

[25] M. J. Guittet, J. P. Crocombette, and M. Gautier-Soyer, “Bonding and XPS chemical shifts in $ZrSiO_4$ versus SiO_2 and ZrO_2: Charge transfer and electrostatic effects,” *Physical Review B*, vol. 63, 125117, 2001.

Chapter 4

Incorporation of Erbium in Hafnium Oxide Gate Dielectric for Metal Gate Work Function Engineering

4.1 Introduction

HfO_2 has been extensively investigated for replacing conventional SiO_2 and SiON gate dielectrics in MOSFETs [1]. One major problem for HfO_2 is the Fermi level pinning between the HfO_2 and a metal gate material [2, 3]. Due to Fermi level pinning, difficulties are faced in obtaining an effective work function of 4.1 eV in the metal/HfO_2 gate stack as required by NMOSFETs [4]. It was previously reported that incorporating La into HfO_2 could tune the work function of TaN metal gate from midgap to Si conduction band edge [5]. In this chapter, we incorporate other lanthanoid metals, namely Dy, Er, Tb and Yb, into HfO_2 to tune the work function of TaN gate. Among these dielectrics, HfErO was studied systematically. It is found that when the atomic ratio of Hf:Er is 7:3 (30% Er) in HfErO film, the effective work function of the TaN metal gate can be tuned to around 4.10 eV, without degrading oxide integrity even after high temperature anneal.

4.2 Experiment

MOS capacitors were fabricated on p-type (100) Si substrates with doping concentration of 6×10^{15} cm^{-3}. Field oxide of approximately 400 nm was thermally grown and subsequently patterned for active area definition. A standard pre-gate clean was performed prior to high-κ dielectric deposition. HfErO films with different Er concentration and thicknesses were deposited using DC magnetron sputtering from Hf and Er metal targets in Ar/O_2 ambient with low oxygen concentrations at room temperature. The composition of Er in HfErO films was controlled by the DC power ratio between Hf and Er targets during co-sputtering. The Er concentration is defined as Er/(Hf+Er) at.%. The dielectric thickness varies from 5 to 20 nm. *Ex-situ* post deposition anneal (PDA) in N_2 were then performed at 600^oC for 30 s with a small amount of O_2 to improve the high-κ film quality. The samples are then put into sputter system immediately (within 5 minutes) for gate electrode deposition, to minimize possible moisture absorption by lanthanoid oxides [6]. In addition, even though there was still some water absorbed during the device fabrication, it has been demonstrated that the absorbed moisture can be desorbed during annealed even at relatively low temperatures [7]. TaN gate electrodes (~150 nm) were deposited using reactive sputtering, and then patterned using a Cl_2-based etchant. After that, Post Metal Anneal (PMA) was done in N_2 ambient at various temperatures for thermal stability evaluation. Finally, all samples received back side Al metallization and 420 ℃ forming gas sintering.

The physical thickness of the films was determined by ellipsometer. The ratio of Er to (Hf + Er) in the HfErO films was determined to be 10%, 30% and 70% by X-ray photoelectron spectroscopy (XPS) using Er 3*d* and Hf 4*f* region on thick (80 nm) HfErO on Si. The interfacial layer were studied on thin (4 nm) HfErO on Si by XPS.

Capacitance-voltage (*C-V*) measurements were performed on MOS capacitors at a frequency of 100 kHz with a HP 4284A precision LCR meter. The equivalent oxide thickness (EOT) and flatband voltage (V_{FB}) were obtained by fitting the measured *C-V* curves with simulated *C-V* curves that account for quantum mechanical effects. Current-voltage (*I-V*) measurements were performed using a HP 4156A semiconductor parameter analyzer.

4.3 Results and Discussion

4.3.1 Physical Characterization

XPS spectra for Hf 4*f* and Er 4*d* are shown in Fig. 1. This analysis is done on 30 nm thick blank samples to minimize the interference from the substrate. It is observed that all the core level peak positions of Hf 4*f* and Er 4*d* experience a shift to lower binding energy with the increase of Er concentration in HfErO. These changes are similar to the XPS chemical shifts in $ZrSiO_4$ [8] and HfAlO [9]. The shift is due to the fact that Er is a more ionic cation than Hf in HfErO [10], and thus the charge transfer contribution changes with the increase of Er concentration [8-10].

Fig. 4.2(a) shows the O 1*s* energy-loss spectra, which are caused by the outgoing photoelectrons suffering inelastic losses to collective oscillations (plasmon) and single particle excitations (band to band transitions) [11]. The energy gap values for the dielectric materials can be determined by the onset of energy loss from the energy-loss spectra [11, 12]. . In each of the spectra in Fig. 4.2(a), the onset of the energy loss spectrum was defined by linearly extrapolating the segment of maximum negative slope to the background level. By this means, the energy gap value is measured to be 5.2 $\pm$0.1 eV for HfO_2, and 5.33 $\pm$0.1 eV for Er_2O_3. A linear change of energy gap value with the increase of Er concentration is observed in Fig. 4.2 (b).

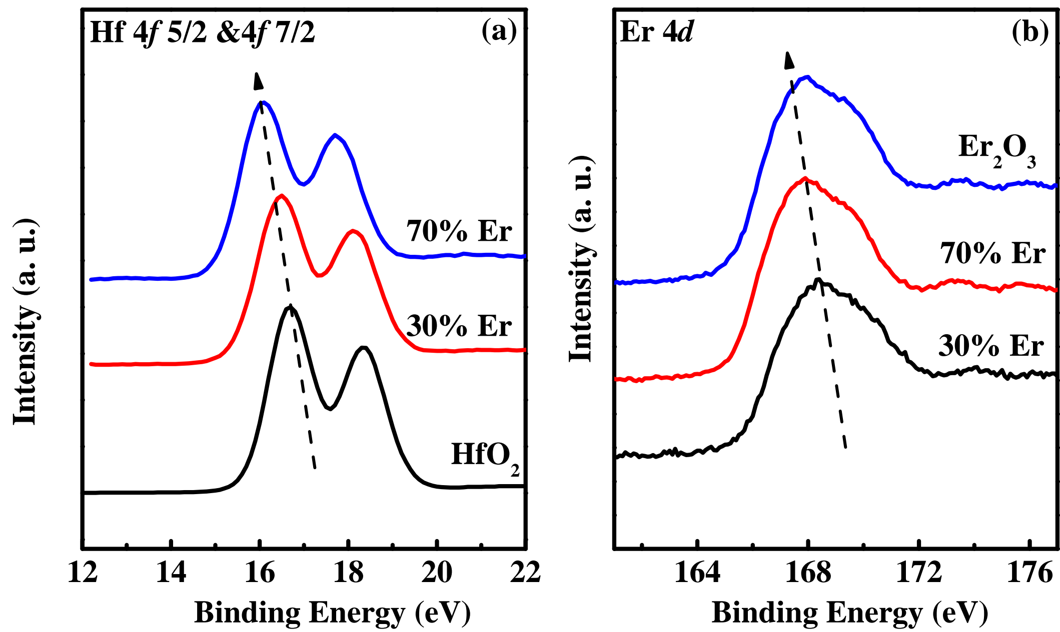

Fig. 4.1. XPS spectra for (a) Hf 4*f* core levels; (b) Er 4*d* core levels. The core level peak positions of Hf 4*f* and Er 4*d* shift continuously towards lower binding energy with increasing Er concentration.

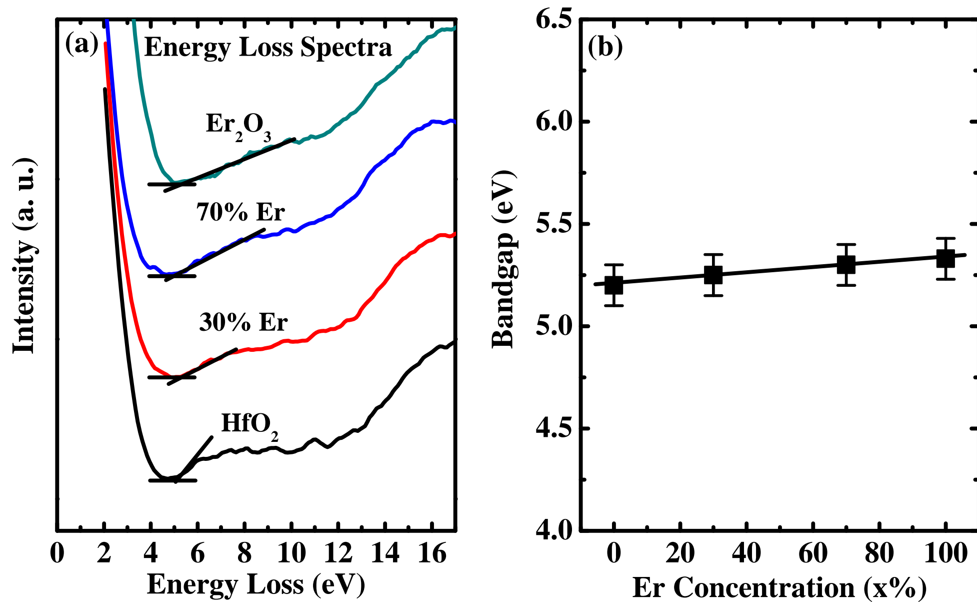

Fig. 4.2. (a) O 1*s* energy loss spectra for HfO_2, HfErO with 30% Er and 70% Er, and Er_2O_3 samples. The cross points (obtained by linearly extrapolating the segment of maximum negative slope to the base line) denote the energy gap E_g values. (b) Dependence of E_g on Er concentration. The solid line is obtained by linear-least-square fit of the data points.

Fig. 4.3 illustrates thermal stability by comparing the variation of EOT for TaN gated MOS capacitors with HfO_2 and HfErO after PMA at different temperatures.

The EOT values are averaged from 10 data points in each split. It was observed that the annealing temperature has more impact on EOT variation of HfO_2 film than that of HfErO films. This shows that HfErO has better thermal stability than HfO_2 in terms of EOT under high temperature anneal.

To study the interface between oxide and silicon substrate, we prepared 4-nm thick HfO_2 and HfErO films on silicon. Fig. 4.4 shows the XPS Si 2*s* spectra of HfO_2 and HfErO with various Er concentrations after 1000 ℃ PDA for 5 s. The two main peaks observed in the spectra can be attributed to the Si substrate (151.3 eV) and the interfacial layer (154.3 eV). The Si-O bonds in the interfacial layer indicate the existence of low-κ interfacial layer.

The reaction between Er_2O_3 thin film and silicon substrate has been reported [13]. The formation of Er silicide or Er–Si bonds can be understood by considering the fact of Er atoms diffusion toward the interface at high-temperature annealing, leading to the reaction of Er with Si. XPS studies confirm the existence of Er-O-Si bond (from erbium silicate) for HfErO on silicon substrate (Fig 4.5).

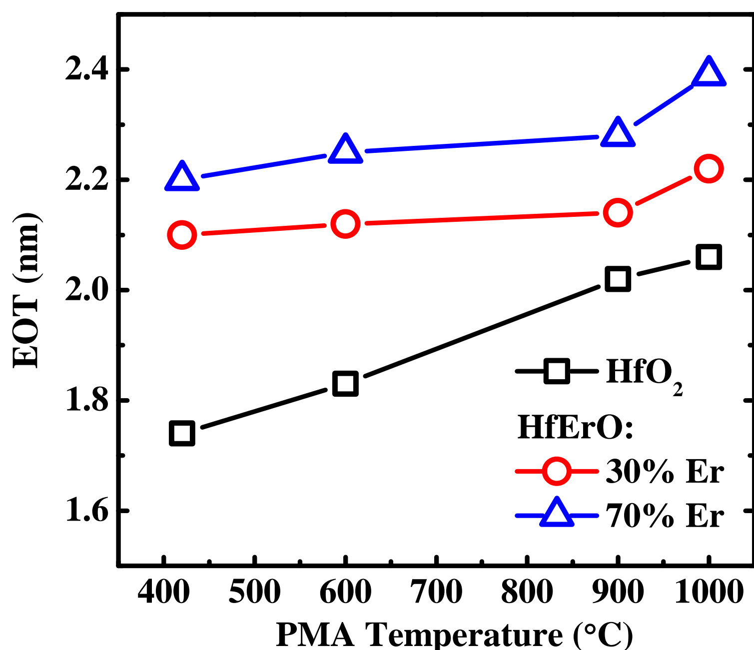

Fig. 4.3. EOT variation for TaN gated MOS capacitors with HfO_2 and HfErO dielectrics as a function of PMA temperatures, which indicates HfErO films have better thermal stability than HfO_2.

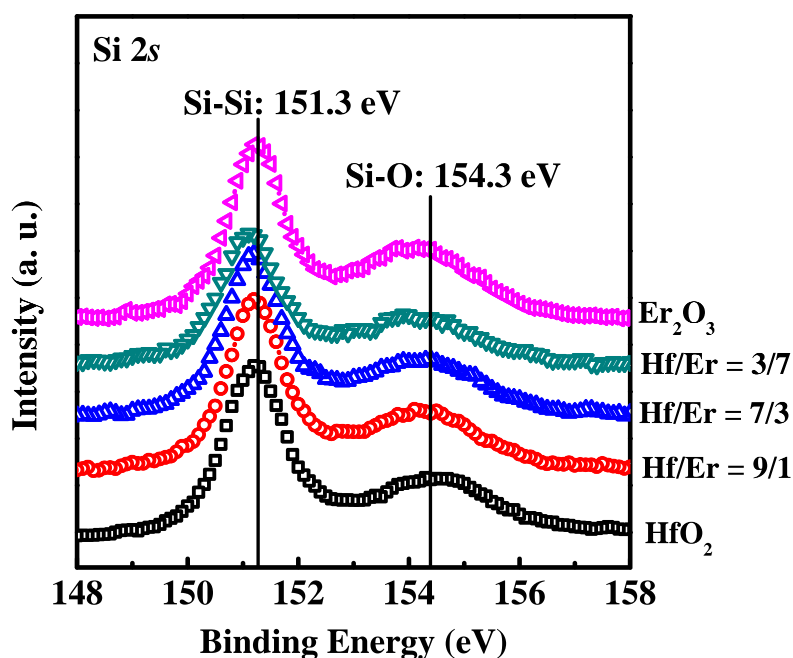

Fig. 4.4. XPS spectra for Si 2*s* core level taken from HfO_2, HfErO and Er_2O_3 after 600 ℃ PDA. The Si-O bond is found on all samples, indicating the existence of a low-κ interfacial layer between the deposited dielectric and silicon substrate.

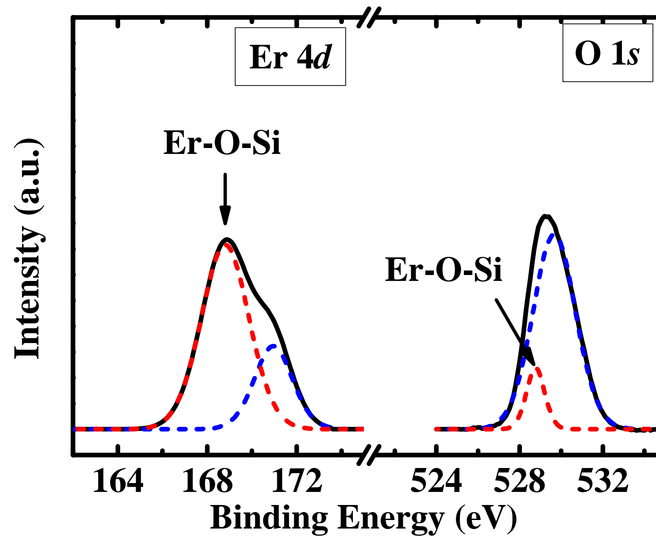

Fig. 4.5. Er core level and O 1*s* spectra for 4 nm HfErO (30% Er) deposited on silicon substrate. The PDA temperature was 600 ℃.

4.3.2 Electrical Characterization

Fig. 4.6 shows the normalized *C-V* curves for TaN gated capacitors with HfO_2 and HfErO gate dielectrics of different Er concentrations after forming gas anneal (FGA) at 420 ℃ only without PMA [Fig. 4.1(a)], and after PMA at 1000 ℃ for 5 seconds followed by FGA [Fig. 4.1(b)]. The thicknesses of the oxides are close to each other and range from 10 to 12 nm as measured by ellipsometer after deposition. For 420 ℃ PMA, the V_{FB} shift is 0.5 V and 0.66 V for 30% Er and 70% Er, respectively. For 1000 ℃ PMA, the V_{FB} shift is 0.38 V and 0.5 V for 30% Er and 70% Er, respectively. V_{FB} shift is observed for all HfErO samples at both temperatures compared to the control HfO_2 samples; while samples with 70% Er have larger V_{FB} shift than those with 30% Er at both temperatures. Therefore, it can be concluded that a higher Er concentration leads to a larger V_{FB} shift.

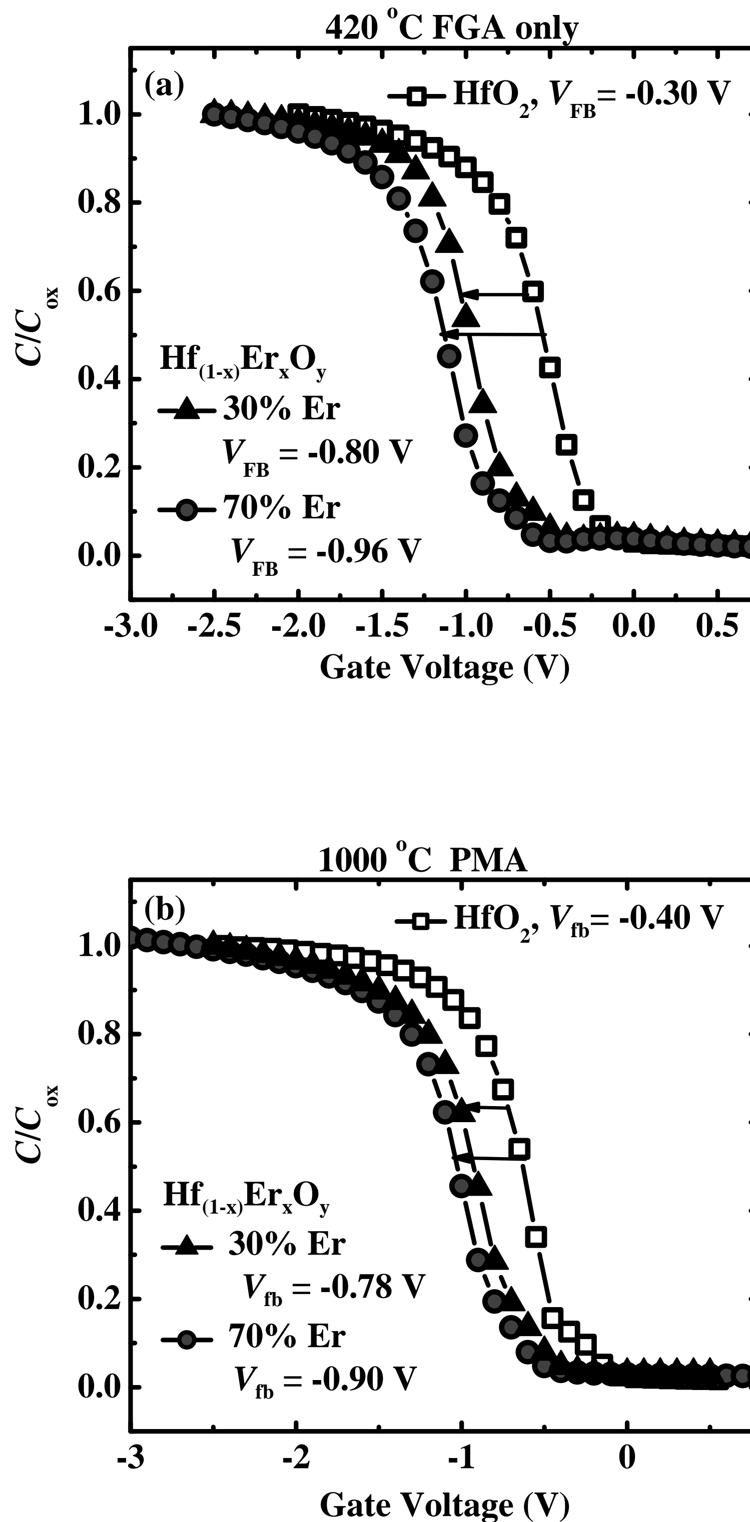

Fig. 4.6. (a) Typical *C-V* curves of capacitors with HfO_2 and HfErO (with 30% and 70% Er) gate dielectrics and TaN metal gate after 420 ℃ forming gas annealing. (b) Typical *C-V* curves of capacitors with HfO_2 and HfErO (with 30% and 70% Er) gate dielectrics and TaN metal gate after 1000˚C, 5 second annealing.

Fig. 4.7 shows the flatband voltage variation with PMA temperature. It is observed that after 1000˚C anneal, the difference in V_{FB} between HfErO and control is reduced for both Er concentrations, which is ascribed to the shift of V_{FB} towards the midgap. This can be explained by localized extrinsic states theory [4], which states that Fermi level pinning due to extrinsic states increases with annealing temperature. It is also observed that the ΔV_{FB} due to 1000˚C anneal, for HfO_2, HfErO (30% Er) and HfErO (70% Er) are -0.1 V, 0.02 V, and 0.06 V, respectively. The amount of ΔV_{FB} of both HfErO devices is smaller than that of HfO_2; yet HfErO (70% Er) has larger shift than HfErO (30% Er). This suggests the ratio of Hf and Er should be optimized to minimize the extrinsic states.

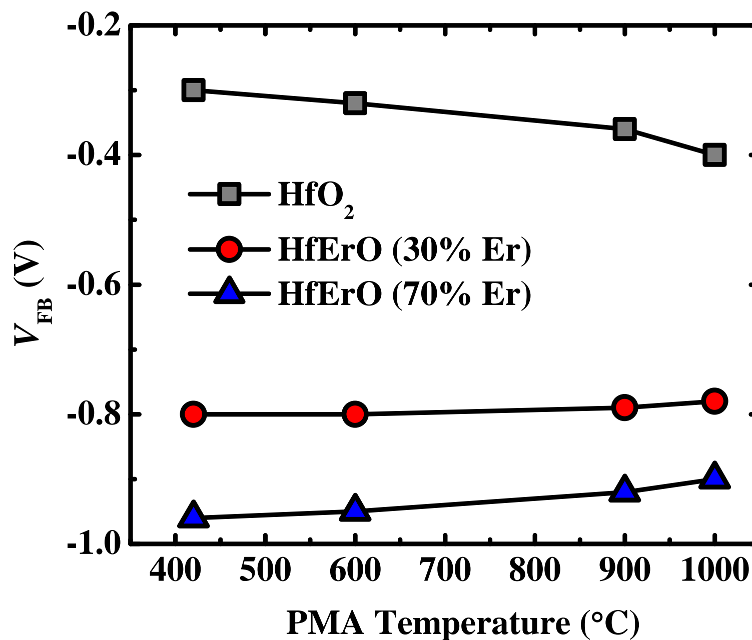

Fig. 4.7. Flatband voltage variation for TaN gated MOS capacitors with HfO_2 and HfErO dielectrics as a function of PMA temperature.

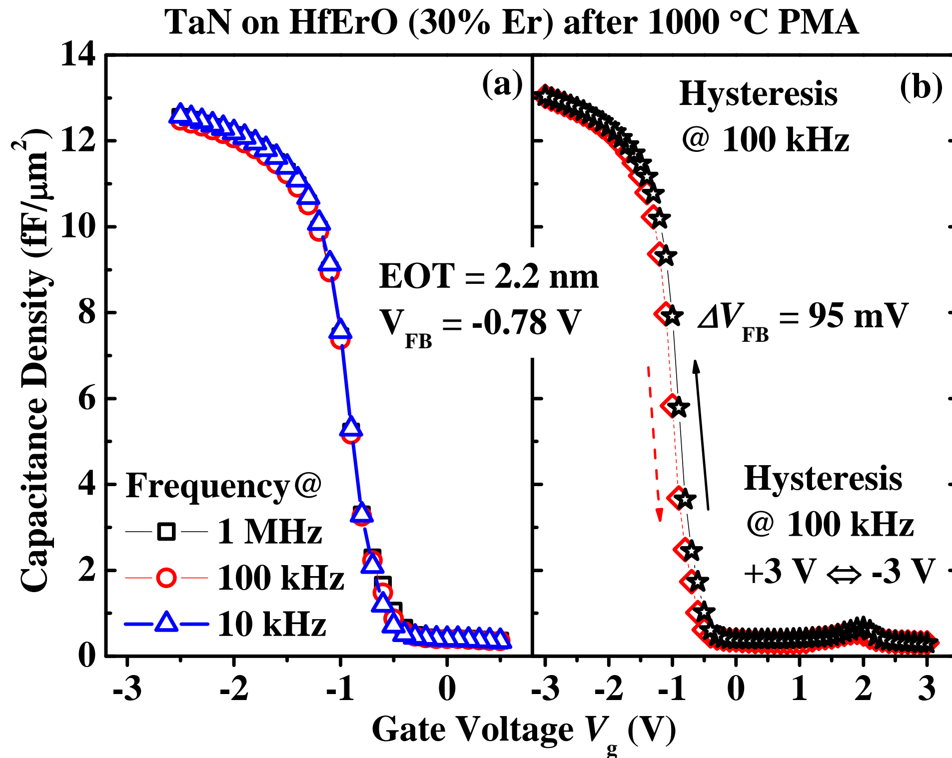

Fig. 4.8. (a) *C-V* curves of the HfErO with 30% Er measured at 10 kHz, 100 kHz and 1 MHz. (b) Hysteresis of MOS capacitors with HfErO (30% Er) dielectric after annealing at 1000 ℃ for 5 s.

Fig 4.8(a) shows the *C-V* curves of HfErO with 30% Er measured at 10 kHz, 100 kHz and 1 MHz. The small dispersion indicates the low interface trap density in the HfErO gate dielectric [14]. Fig 4.8(b) shows a hysteresis (~95 mV) for HfErO film (with 30% Er) after activation annealing at 1000 ℃ for 5 s. The hysteresis was quantified by the difference in V_{FB} during the voltage sweeps without delay time between ±3 V.

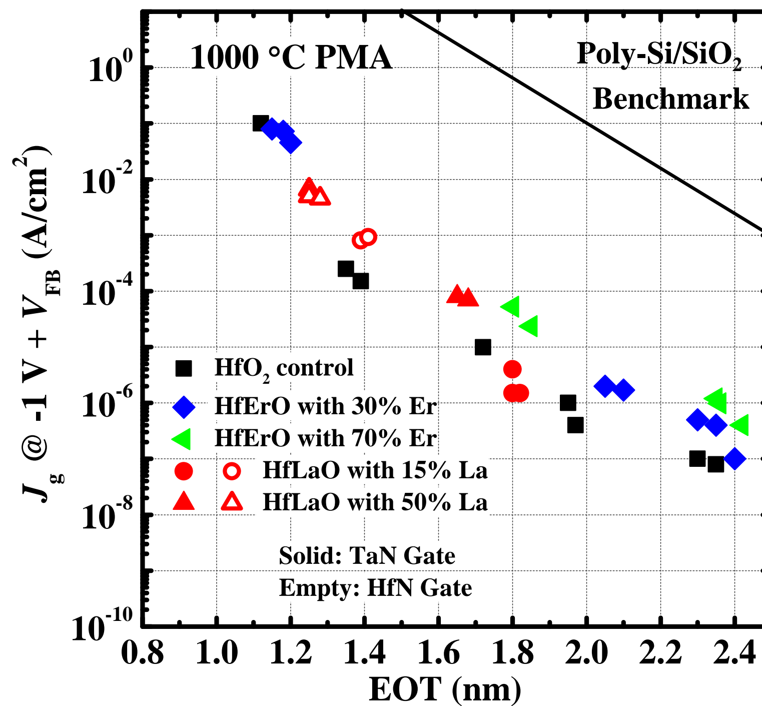

Fig. 4.9. The relationship between gate leakage current density and EOT for MOS capacitors with HfO_2, HfLaO and HfErO gate dielectrics and TaN or HfN metal gate. Compared with poly-Si/SiO_2 benchmark at the same EOT, HfErO provides ~4 orders reduction in gate leakage current. HfLaO data is from Ref. [5].

Fig. 4.9 shows that the gate leakage current densities of HfO_2, HfLaO and HfErO at different EOTs. HfLaO data is from a previously published paper [5], but the PMA was done at a lower temperature of 900˚C. The leakage current densities of HfErO locate on almost the same trend line as HfO_2 and HfLaO, and have around 4 orders reduction compared with poly-Si/SiO_2 benchmark, but they are slightly higher than that of HfO_2. It is shown in Fig. 4.4 and Fig. 4.5 that there is a substantial formation of silicate at the HfErO/Si interface, and the silicate interfacial layer increases leakage current density. This may have caused the increase of leakage current density compared to HfO_2 control.

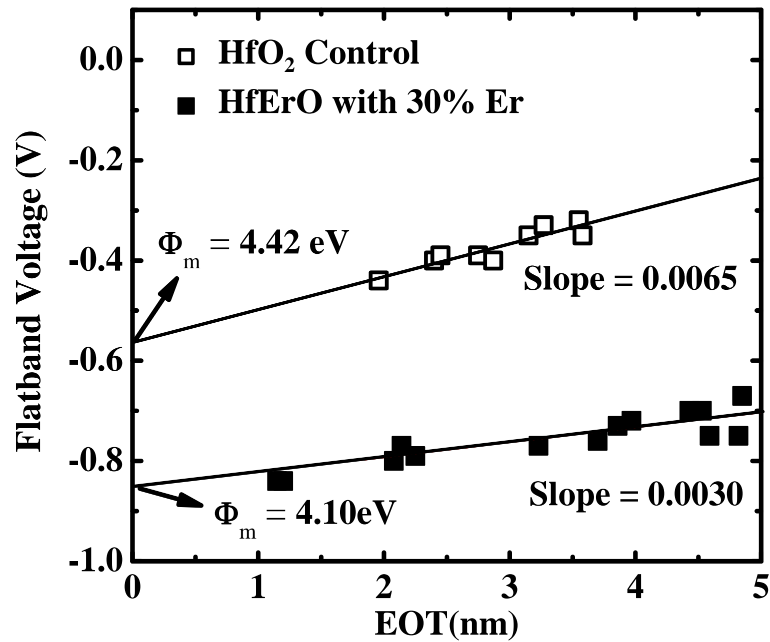

Fig. 4.10. V_{FB} vs. EOT plot was used to extract the modulated TaN Φ_m in TaN/HfO_2 or TaN/HfErO gate stack by eliminating the effect of fixed oxide charge. The PMA temperature was 1000˚C. The p-Si substrate doping was 6×10^{15} cm^{-3}.

Effective metal gate work function Φ_m was extracted from V_{FB} vs. EOT plot as shown in Fig. 4.3. The plot rules out the V_{FB} shift due to fixed charge in oxide. For HfErO with 30% Er after 1000 ℃ PMA, the extracted Φ_m is 4.1 eV, which meets the NMOS requirement. The slope for HfErO is smaller than that for HfO_2 control, which means that the fixed charge density in HfO_2 is reduced with the incorporation of Er. This is similar to the previous published work on HfLaO [5].

Fig. 4.11 shows the cumulative breakdown voltage of 10 nm HfErO with 30% Er. The breakdown voltage ranges from -5 V to -5.8 V. The increase of breakdown voltage with the increasing PMA temperature should be attributed to the growth of the interfacial layer, which increases the dielectric thickness and reduces the E-field. Tight V_{BD} distributions indicate good HfErO thickness uniformity.

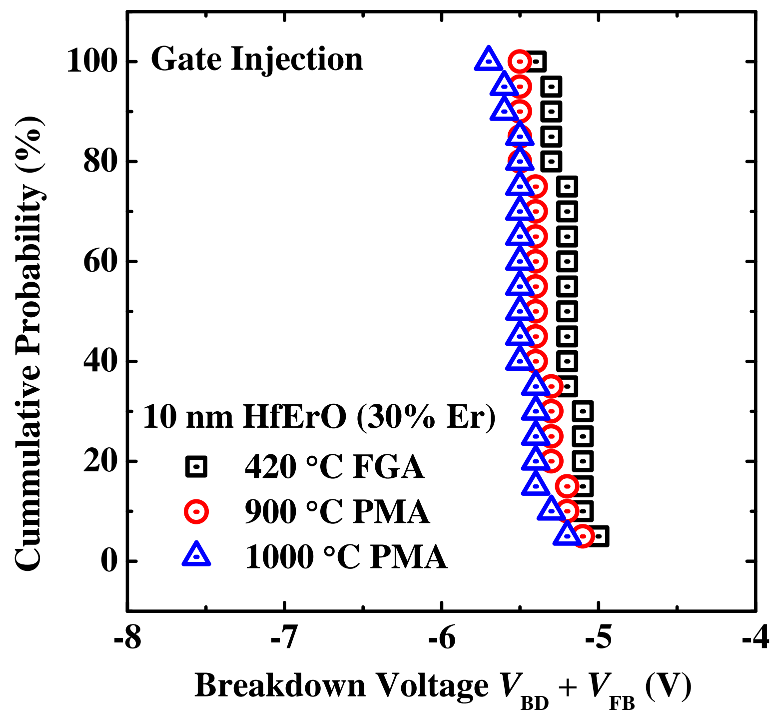

Fig. 4.11. Dependence of cumulative probability on breakdown voltage of TaN gated MOS capacitors with HfErO (30% Er).

4.3.3 Dipole Models for Metal Gate Work Function Tunability

As discussed in Chapter 3, interface dipoles induced by intrinsic or extrinsic states at the metal/dielectric interface, lead to shift of flatband voltage and effective gate work function. To provide guidance in choosing the right metal gate/high-κ stacks, Wang *et al.* further developed the interface dipole model by adding two factors, electronegativity and oxygen vacancy [15, 16]. Electronegativity is the tendency of an atom in a molecule to attract electrons to it. The atom with a higher electronegativity will always pull the electrons away from the atom that has a lower electronegativity. The difference in electronegativity defines the degree of electron shift. This effect is believed to be the main factor for n-type metal gates, such as TaN. Oxygen vacancy V_o in dielectric is also believed to induce electron transfer from V_o to the gate

electrode, which also leads to Fermi level pinning. This effect is obvious on p-type noble metals.

Er has an electronegativity of 1.24 on Pauling scale, which is lower than those of Hf (1.3) and Ta (1.5) [17]. Therefore, for the case of TaN gate, additional electrons transfer from HfO_2 to TaN through the dipole layer would be expected when Er atoms replace Hf atoms close to the interface due to the lower electronegativity of Er atoms. This effect compensates the original electron transfer from TaN to HfO_2 due to Fermi level pinning, resulting in partial release of Fermi level pinning and reduction of TaN effective work function. The corresponding energy band diagram for this case is shown in Fig. 4.12.

Recently, Toriumi and co-workers [18-20] showed by doing a series of alternate depositions that the determining interface in metal gate/high-κ/SiO_2 gate stack is not the upper oxide-gate interface but rather the lower high-κ/SiO_2 interface at the bottom of the stack. This applies to both La_2O_3 and Al_2O_3 capping layers. The effect might be due to the strong reaction of La_2O_3 and SiO_2 to form a silicate. Similarly, aluminates are formed by Al_2O_3. Although the La_2O_3 starts as a top layer, the free energy gain of forming the silicate drives diffusion to the bottom layer. However, the mechanism of the interface dipole was not clarified.

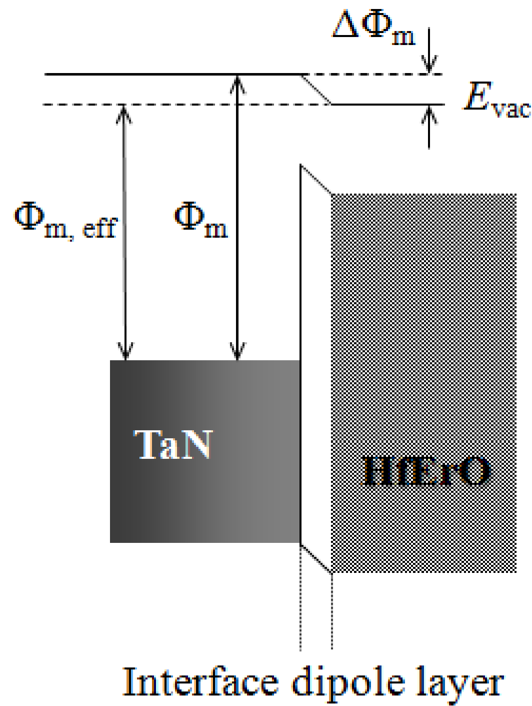

Fig. 4.12. The effect of an interface dipole layer on TaN Φ_m is illustrated in the energy band diagram. The Φ_m of TaN is reduced by $\Delta\Phi_m$ due to the presence of the interface dipole.

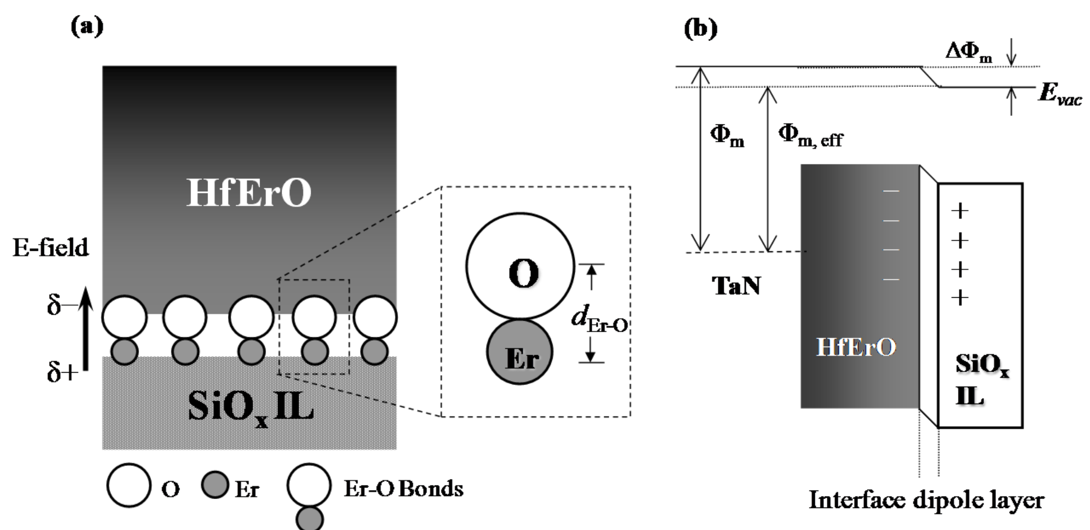

Fig. 4.13. (a) A schematic showing highly polarized Er-O dipoles at the HfErO/SiO_x interface. (b)The Φ_m of TaN is reduced due to the presence of dipole at the HfErO and SiO_x interface, which is different from Fig. 4.12.

The dipole layer at high-κ/SiO_2 interface is modeled by Lim *et al.* [21], as discussed in Chapter 3. This model can also be used to explain the shift of Φ_m of TaN/HfErO stack. Although there is no intentionally-grown SiO_2 below the HfErO, the oxygen rich PDA process could lead to formation of SiO_x inter-layer (IL) between HfErO and Si substrate. Er reacts with SiO_x and form highly polarized Er-O bond pointing toward the gate electrode. The existence of Si-O and Er-O-Si bonds has been confirmed by XPS studies (Fig. 4.4 and Fig. 4.5). Thus, a highly polarized Er-O dipole exists between the HfErO gate and SiO_x interfacial layer. This creates an electric field that modulates the gate work function, as illustrated in Fig. 4.13.

4.4 HfO_2 Incorporated with Other Lanthanoid Elements

Despite the different opinions on the location of the dipoles, the role of electronegativity is a key factor in all kinds of dipoles. Other lanthanoid elements, including Tb, Dy, and Yb, were incorporated into HfO_2 as gate dielectrics. All are lanthanoid elements sharing similar physical and chemical properties with Er. Normalized *C-V* curves for MOS capacitors with these dielectrics and TaN gate electrode are summarized in Fig. 4.14(a). The modulated Φ_m values are extracted from V_{FB}-EOT plots in Fig. 4.14(b). The results are summarized in Table 4.1. With the incorporation of these low electronegativity lanthanoid elements, V_{FB} for TaN/HfO_2 stack obviously shifts negatively and the Φ_m shifts to the silicon conduction band edge.

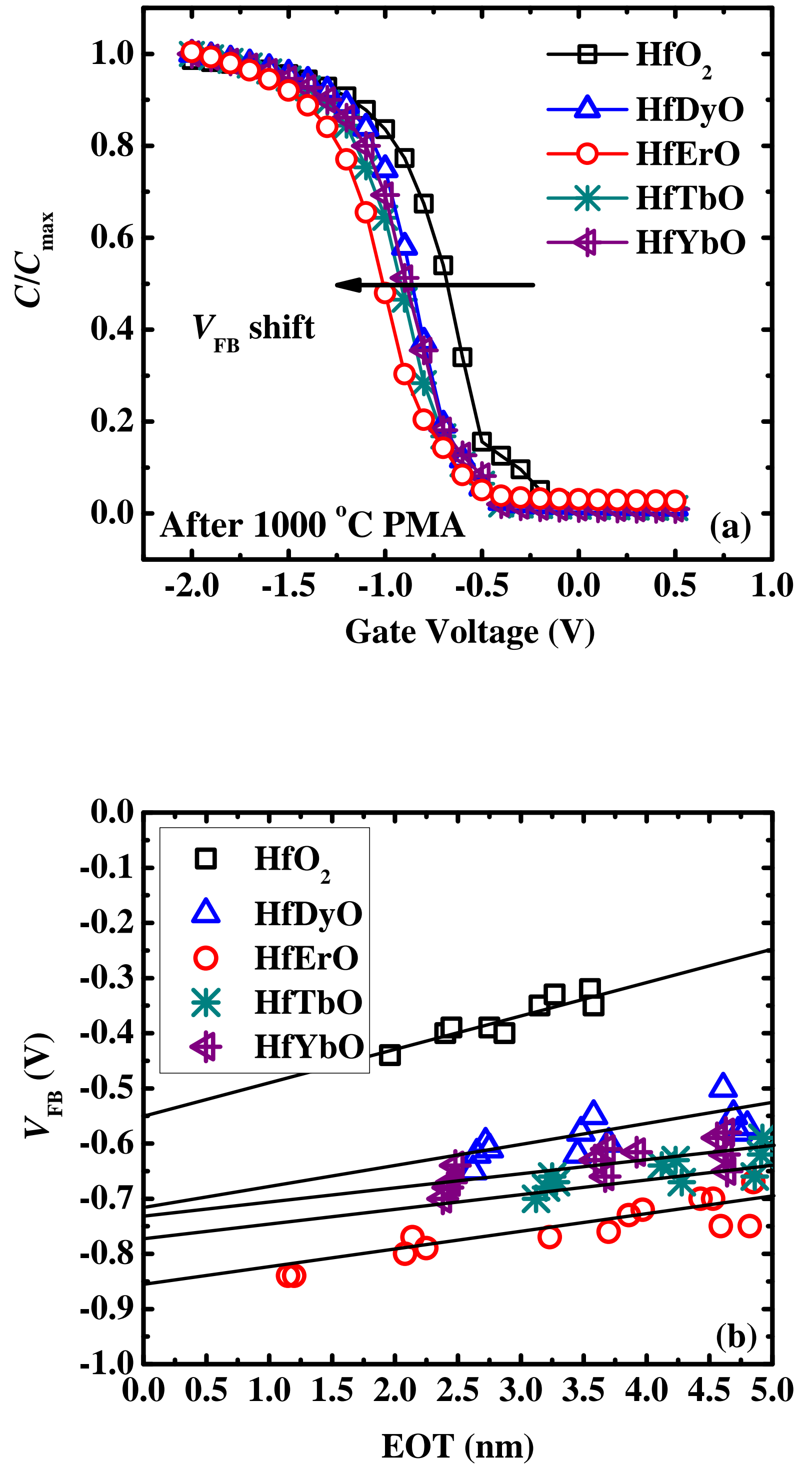

Fig. 4.14. (a) *C-V* curves of HfO_2 doped by Er_2O_3, Tb_2O_3, Yb_2O_3 and Dy_2O_3 after 1000 ℃ anneal. All curves show significant flatband voltage shift towards silicon conduction band. (b) V_{FB} versus EOT plot was used to extract the TaN Φ_m modulated by doping HfO_2 with by Er_2O_3, Tb_2O_3, Yb_2O_3 and Dy_2O_3.

Table 4.1. Summary of all lanthanoid elements incorporated into HfO_2 for metal gate work function tuning. All elements exhibit low electronegativities. The concentration of each element is derived from XPS measurements. The $\Phi_{m,\ eff}$ values are extracted from Fig. 4.14(b).

Incorporated Element	Er	Tb	Yb	Dy
Electronegativity	1.24	1.1	1.1	1.22
Concentration Ln/(Hf+Ln)	30%	27%	17%	21%
$\Phi_{m,\ eff}$ (eV)	4.10	4.18	4.22	4.24

4.5 Conclusion

In this chapter, a novel method of doping HfO_2 with Er_2O_3 to engineer the Φ_m of TaN metal gate was investigated. The doped Er_2O_3 enabled Si conduction band-edge modulation (4.1 eV) of midgap TaN Φ_m. Band edge Φ_m was retained even after high temperature anneal. A small EOT of 1.15 nm was achieved by HfErO (30% Er).

Er-O-Si Bonding confirmed the formation of erbium silicate at the high-κ/Si interface. Interfacial dipole models are investigated to interpret the significant work function shift. The modulation of TaN gate Φ_m was attributed to the dipole layers at both the TaN/HfErO and HfErO/Si interface. Similar results are obtained by doping HfO_2 doped by other lanthanoid metal oxides, namely Tb_2O_3, Dy_2O_3, and Yb_2O_3.

References:

[1] G. Wilk, R. Wallace, and J. Anthony, "High-κ gate dielectrics: Current status and materials properties considerations," *Journal of Applied Physics,* vol. 89, pp. 5243, 2001.

[2] S. Samavedam, L. La, P. Tobin, B. White, C. Hobbs, L. Fonseca, A. Demkov, J. Schaeffer, E. Luckowski, and A. Martinez, "Fermi level pinning with sub-monolayer MeO_x and metal gates," *International Electron Devices Meeting Tech. Dig.,* pp. 307-310, 2003.

[3] Y. Yeo, T. King, and C. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology," *Journal of Applied Physics,* vol. 92, pp. 7266, 2002.

[4] I. De, D. Johri, A. Srivastava, and C. Osburn, "Impact of gate workfunction on device performance at the 50 nm technology node," *Solid State Electronics,* vol. 44, pp. 1077-1080, 2000.

[5] X. Wang, M. Li, C. Ren, X. Yu, C. Shen, H. Ma, A. Chin, C. Zhu, J. Ning, and M. Yu, "Tuning effective metal gate work function by a novel gate dielectric HfLaO for nMOSFETs," *IEEE Electron Device Letters,* vol. 27, pp. 31, 2006.

[6] Y. Zhao, M. Toyama, K. Kita, K. Kyuno, and A. Toriumi, "Moisture-absorption-induced permittivity deterioration and surface roughness enhancement of lanthanum oxide films on silicon," *Applied Physics Letters,* vol. 88, pp. 072904, 2006.

[7] H. Watanabe, N. Ikarashi, and F. Ito, "La-silicate gate dielectrics fabricated by solid phase reaction between La metal and SiO_2 underlayers," *Applied Physics Letters,* vol. 83, pp. 3546, 2003.

[8] M. Guittet, J. Crocombette, and M. Gautier-Soyer, "Bonding and XPS chemical shifts in $ZrSiO_4$ versus SiO_2 and ZrO_2: Charge transfer and electrostatic effects," *Phys. Rev. B,* vol. 63, pp. 125117, 2001.

[9] H. Yu, M. Li, B. Cho, C. Yeo, M. Joo, D. Kwong, J. Pan, C. Ang, J. Zheng, and S. Ramanathan, "Energy gap and band alignment for $(HfO_2)_x(Al_2O_3)_{1-x}$ on (100) Si," *Applied Physics Letters,* vol. 81, pp. 376-378, 2002.

[10] G. Lucovsky, "Electronic structure of high-κ transition-metal and rare-earth gate dielectrics for aggressively-scaled silicon devices," *Proceedings of the International Workshop on Gate Insulator,* pp. 14-15, Tokyo, 2001.

[11] F. Bell and L. Ley, "Photoemission study of SiO_x (0 x 2) alloys," *Physical Review B,* vol. 37, pp. 8383-8393, 1988.

[12] H. Itokawa, T. Maruyama, S. Miyazaki, and M. Hirose, "Determination of Bandgap and Energy Band Alignment for High-Dielectric-Constant Gate Insulators Using High-Resolution X-ray Photoelectron Spectroscopy," *Extended Abstracts of the 1999 Int. conf. Solid State Devices and Materials*, pp. 158-159, 1999.

[13] T. Pan, C. Chen, W. Yeh, and S. Hou, "Structural and electrical characteristics of thin erbium oxide gate dielectrics," *Applied Physics Letters,* vol. 89, pp. 222912, 2006.

[14] G. Wilk and R. Wallace, "Electrical properties of hafnium silicate gate dielectrics deposited directly on silicon," *Applied Physics Letters,* vol. 74, pp. 2854, 1999.

[15] X. Wang, H. Yu, M. Li, C. Zhu, S. Biesemans, A. Chin, Y. Sun, Y. Feng, A. Lim, and Y. Yeo, "Wide V_{fb} and V_{th} tunability for metal-gated MOS devices with HfLaO gate dielectrics," *IEEE Electron Device Letters,* vol. 28, pp. 258-260, 2007.

[16] X. Wang, H. Yu, Y. Yeo, M. Li, S. Chang, H. Cho, S. Kubicek, D. Wouters, G. Groeseneken, and S. Biesemans, "Understanding and prediction of EWF modulation induced by various dopants in the gate stack for a gate-first

integration scheme," *Symposium on VLSI Technology Tech. Dig.*, pp. 162-163, 2008.

[17] D. Lide, "*CRC handbook of chemistry and physics: a ready-reference book of chemical and physical data,*" CRC press, 2004.

[18] K. Iwamoto, H. Ito, Y. Kamimuta, Y. Watanabe, W. Mizubayashi, S. Migita, Y. Morita, M. Takahashi, H. Ota, and T. Nabatame, "Re-examination of flat-band voltage shift for high-k MOS devices," *Symposium on VLSI Technology Tech. Dig.,* pp. 70-71, 2007.

[19] K. Iwamoto, Y. Kamimuta, A. Ogawa, Y. Watanabe, S. Migita, W. Mizubayashi, Y. Morita, M. Takahashi, H. Ota, and T. Nabatame, "Experimental evidence for the flatband voltage shift of high-k metal-oxide-semiconductor devices due to the dipole formation at the high-κ/SiO_2 interface," *Applied Physics Letters,* vol. 92, pp. 132907, 2008.

[20] A. Toriumi, K. Kita, K. Tomida, Y. Zhao, J. Widiez, T. Nabatame, H. Ota, and M. Hirose, "Materials science-based device performance engineering for metal gate high-κ CMOS," *International Electron Devices Meeting Tech. Dig.,* pp. 53-56, 2007.

[21] A. Lim, R. Lee, G. Samudra, D. Kwong, and Y. Yeo, "Novel Rare-Earth Dielectric Interlayers for Wide NMOS Work-Function Tunability in Ni-FUSI Gates," *IEEE Transactions on Electron Devices,* vol. 55, pp. 2370-2377, 2008.

Chapter 5

Lanthanoid Oxides for Precision RF/Analog MIM Capacitors

5.1 Introduction

Metal-Insulator-Metal (MIM) capacitors occupy substantial areas in integrated circuits for Radio-Frequency (RF) and analog/mixed-signal applications. With the rapid feature size reduction and increased levels of integration to reduce IC fabrication cost, MIM capacitors with higher capacitance densities are required. High capacitance density can be realized by reducing the thickness and/or increasing the permittivity κ of the MIM dielectric material. However, leakage current and reliability issues limit thickness scaling of the MIM dielectric. In addition, there are stringent requirements on the voltage coefficients of capacitance (VCC), including the quadratic VCC (α) and the linear VCC (β), for precision analog circuit applications. According to the International Technology Roadmap for Semiconductors (ITRS) [1], the capacitance density requirement would be 7 fF/μm^2 by 2013, and 10 fF/μm^2 by 2016, while the quadratic VCC should be kept below 100 ppm/V^2 and the leakage current should be below 10^{-8} A/cm^2 at room temperature and at maximum supply voltage V_{DD}. Thus the target is to achieve higher capacitance density while keeping

the VCC and leakage low. High-κ dielectrics have been investigated to replace the conventional SiO_2 and SiON in MIM capacitors. Many high-κ dielectrics, such as Ta_2O_5 [2], HfO_2 [3]-[4] , TiO_2 [5], Al_2O_3 [6], Y_2O_3 [7], as well as different combination of these dielectrics as sandwich or laminate structures, such as $Ta_2O_5/HfO_2/Ta_2O_5$ [8], $Al_2O_3/HfO_2/Al_2O_3$ [9], TaZrO [10], PrTiO [11] and HfTbO [12] have been explored to meet the capacitance density and leakage current density requirements. However, most of these high-*κ* dielectrics are found to have large positive quadratic VCCs. As the quadratic VCC usually increases with decreasing MIM dielectric thickness, it is difficult to increase the capacitance density while keeping the quadratic VCC less than 100 ppm/V^2. Recently, it was reported that adding Tb into HfO_2 could effectively reduce the quadratic VCC [12]. However, there has been little study on binary lanthanoid oxides for MIM capacitors.

In this chapter, we first did a material screening by fabricating MIM capacitors with various lanthanoid oxides, among which Sm_2O_3 and Er_2O_3 stand out as the best candidates. After that the physical and electrical properties of MIM capacitors with Sm_2O_3 and Er_2O_3 dielectrics were carried out systematically. Finally, we demonstrate the use of stacked Sm_2O_3/SiO_2 and Er_2O_3/SiO_2 as the MIM dielectric to further reduce the quadratic VCC to near zero while keeping the capacitance density high and the leakage current density low.

5.2 Device Fabrication and Material Screening

5.2.1 Device Fabrication

MIM capacitors were fabricated on Si wafers covered with a 500 nm thick thermally-grown SiO_2. A 200 nm thick TaN bottom electrode layer was then

deposited on the SiO_2 layer by reactive sputtering in an Argon/Nitrogen (Ar/N_2) ambient.

For MIM capacitors with a single-layer dielectric, a Sm_2O_3 film was directly deposited on the TaN bottom electrode with RF power applied on a Sm_2O_3 target at room temperature in Ar ambient. The thickness of the Sm_2O_3 layer deposited ranged from 10 to 30 nm. After dielectric deposition, N_2 plasma treatment was carried out. Post-dielectric deposition annealing (PDA) at 400 ℃ for 60 s within N_2 ambient (with some trace oxygen) was then performed for all samples. The trace oxygen came from the oxygen gas flow during the purging process in the RTP; the oxygen flow was stopped once the temperature started to ramp up.

While Sm_2O_3 was sputtered from the Sm_2O_3 target, Er_2O_3, Dy_2O_3, La_2O_3, Tb_2O_3, and Yb_2O_3 were sputtered from metal target by reactive sputtering in Ar/O_2 environment. This made it possible to manipulate the oxygen vacancy in the dielectric by controlling the Ar/O_2 gas flow. Two Ar/O_2 flow rate ratios (27:3 and 28:2) were used, while the total gas flow was fixed at 30 sccm. The PDA processes were all conducted at 400 ℃ for 60 s. For the ambient in the RTP chamber, other than trace oxygen, two other conditions were used besides the N_2 ambient with trace oxygen. One was pure N_2 without any O_2, the other was 95% N_2 with 5% O_2.

Following the oxide deposition and PDA, a 100 nm thick TaN top electrode layer was sputtered, and then patterned using lithography and dry-etch.

The MIM capacitors were characterized using transmission electron microscopy (TEM), X-ray diffraction (XRD), and X-ray photoelectron spectroscopy (XPS). Capacitance and leakage current were measured on 200×200 μm^2 capacitors using a HP4284A precision LCR meter and a HP4155B semiconductor parameter

analyzer, respectively. The leakage current was measured using long integration time (1 second) with a delay time of 1 second to obtain current in the steady state.

5.2.2 Material Screening

As discussed in the introduction, the target is to find materials with higher capacitance density but lower quadratic VCC. Fig. 5.1 summarizes the best quadratic VCC obtained for each oxide and plotted them versus capacitance density. The black line represents the highest capacitance density for a given α and is contributed by data points from Sm_2O_3 and Er_2O_3. MIM capacitors with Sm_2O_3 or Er_2O_3 dielectric have lowest α (positive) for a given capacitance density. Dy_2O_3 and Tb_2O_3 show small quadratic VCC close to that of Er_2O_3. Other oxides show much larger quadratic VCC which make them less preferable for RF/analog applications.

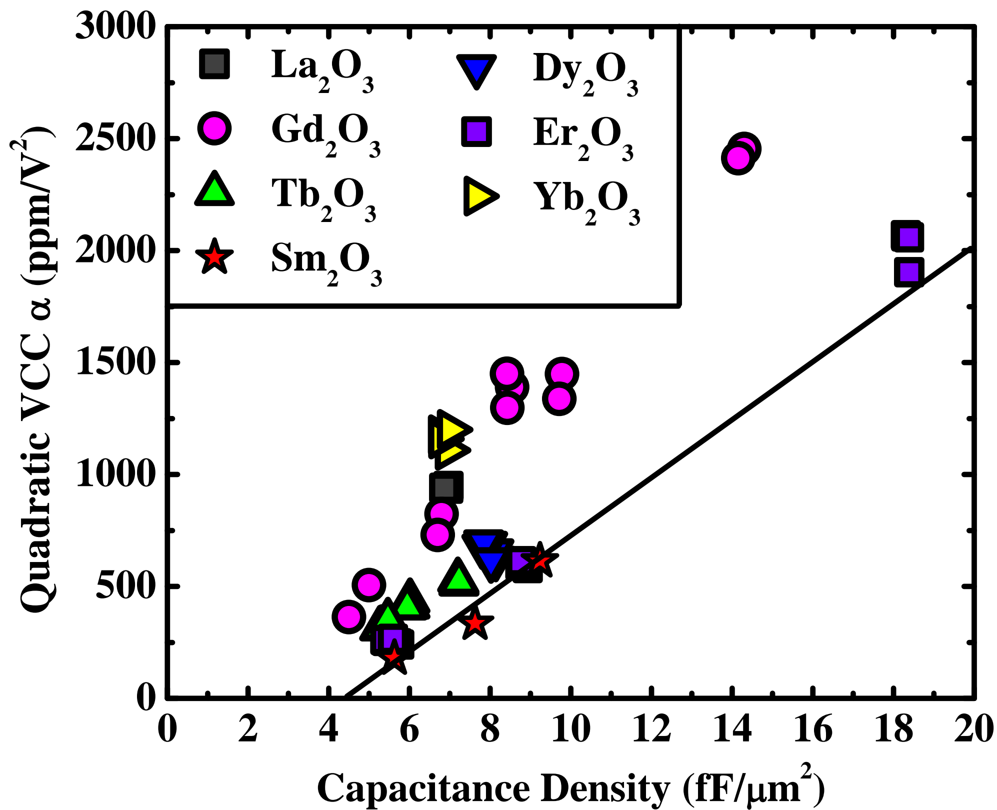

Fig. 5.1. Summary of quadratic VCC of MIM capacitors with various lanthanoid oxides, plotted versus capacitance density for all lanthanoid oxide MIM capacitors.

Fig. 5.2 compares the α of MIM capacitors with a Sm_2O_3 or Er_2O_3 dielectric layer obtained in this work with other high-κ MIM capacitor reports. At a given capacitance density, MIM capacitors with a Sm_2O_3 or Er_2O_3 dielectric are found to have smaller positive α than most of the other high-κ oxides, and have the lowest α among binary oxides. When compared with the extensively studied HfO_2, Sm_2O_3 has smaller α at the same capacitance density, especially in the region where the capacitance density is larger than 7 fF/μm^2. This makes Sm_2O_3 and Er_2O_3 potential candidates for MIM dielectric in precision analog circuit applications. The preliminary material screening show that Sm_2O_3 and Er_2O_3 are better than other lanthanoid oxides and other high-κ dielectrics in terms of voltage linearity and capacitance density.

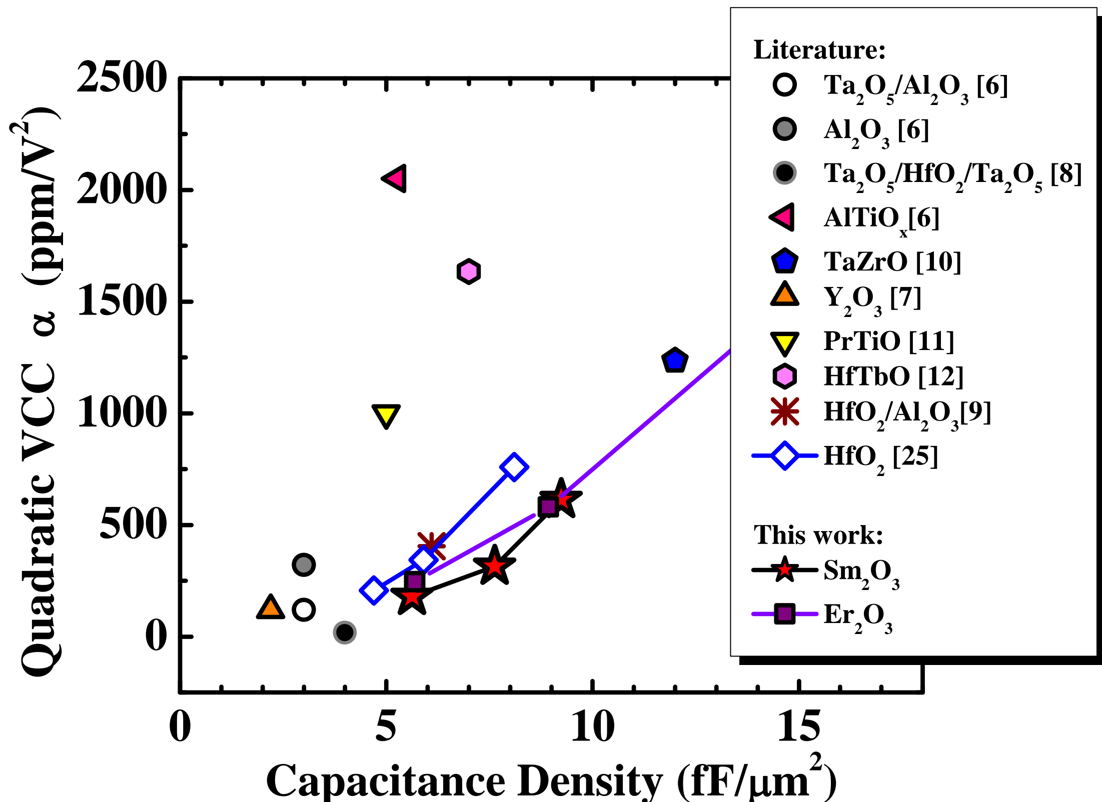

Fig. 5.2. The values of α extracted from MIM capacitors with a single Sm_2O_3 or Er_2O_3 dielectric layer in this work are compared with data published in the literature.

5.3 MIM Capacitors with a single layer Sm_2O_3 dielectric

5.3.1 Physical Characterization

Fig. 5.3 (a) shows a schematic of a MIM capacitor. TEM image in Fig. 5.3 (b) reveals the polycrystalline nature of the Sm_2O_3 layer in MIM capacitor with single layer dielectric. Considering the capacitance density of 13.5 fF/μm^2 and physical thickness of 12.5 nm from TEM, the dielectric constant κ of Sm_2O_3 is calculated to be 19.0. This is within the range of 10 to 30.5 as reported in the literature [13-15]. The κ value of Sm_2O_3 is also comparable to that of the widely researched HfO_2 (22~25) [16].

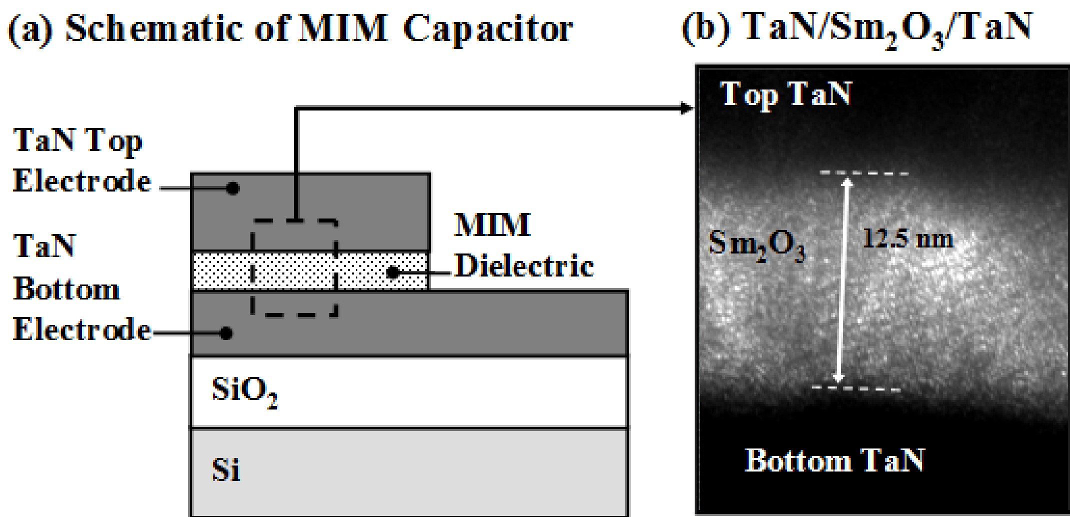

Fig. 5.3. (a) Schematic of Metal-Insulator-Metal (MIM) capacitor having top and bottom tantalum nitride (TaN) electrodes. (b) In one split, the MIM dielectric is a single Sm_2O_3 layer, as shown in the cross-sectional TEM image.

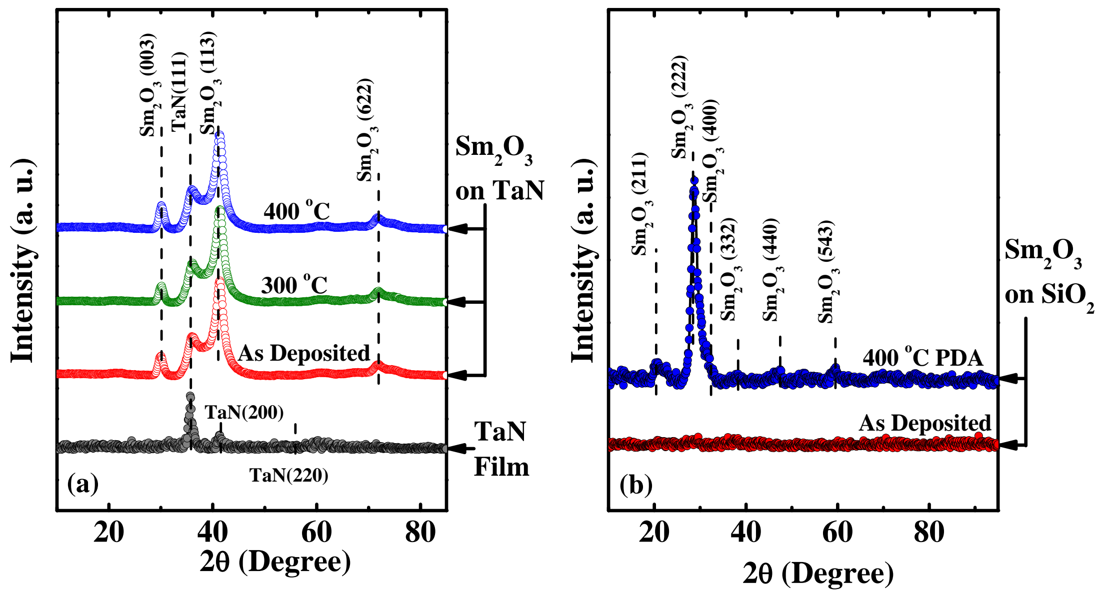

Fig. 5.4. (a) X-ray diffraction (XRD) spectra of as-deposited Sm_2O_3 on TaN, as well as Sm_2O_3/TaN stack after being annealed at 300 ℃ and 400 ℃. XRD spectrum of an exposed TaN surface is also obtained. As-deposited Sm_2O_3 on TaN is poly-crystalline. (b) XRD spectra of as-deposited Sm_2O_3 on SiO_2, as well as Sm_2O_3/SiO_2 stack after being annealed at 400 ℃. As-deposited Sm_2O_3 on SiO_2 is amorphous.

80 nm Sm_2O_3 films were prepared for analysis of the crystalline structure using XRD, and were either deposited directly on a 200 nm thick TaN [Fig. 5.4(a)] or on a 500 nm thick amorphous SiO_2 [Fig. 5.4(b)]. Annealing was done at various temperatures before XRD. In Fig. 5.4(a), an XRD plot obtained from a bare TaN surface prior to Sm_2O_3 deposition shows that the TaN film is poly-crystalline. The as-deposited Sm_2O_3 film formed on TaN is also poly-crystalline. After being annealed at 300 or at 400 ℃ [Fig. 5.4(a)], the Sm_2O_3 peaks did not differ much, indicating the phase and composition were not affected. On the other hand, Sm_2O_3 film was amorphous when it was first deposited on a SiO_2 surface [Fig. 5.4(b)]. The Sm_2O_3 film crystallized after being annealed at 400 ℃. The crystallization behavior of Sm_2O_3 appears to be dependent on the substrate material. While the Sm_2O_3 dielectric

thickness used in XRD analysis is thicker than those used in MIM capacitors, the observation of poly-crystalline nature of annealed Sm_2O_3 from XRD analysis is qualitatively consistent with TEM results obtained for thinner films (Fig. 5.3).

Next, we derive the energy band gap E_g of Sm_2O_3 from the O 1*s* energy-loss spectra of bulk Sm_2O_3 film [Fig. 5.5(a)] using the same approach as discussed in Chapter 4. The energy gap for Sm_2O_3 was obtained to be 5.20 $\pm$ 0.10 eV, which is consistent with previously reported value of 5.0 eV [17]. The E_g of Sm_2O_3 is seen to be comparable with other commonly used high-κ materials such as HfO_2 (5.25 eV) [18] and Gd_2O_3 (5.5 eV) [17].

The Schottky barrier for electrons Φ_{bn} evaluated at the interface between the MIM dielectric and an electrode, i.e. difference between the Fermi level of an electrode and the conduction band of a MIM dielectric, should preferably be large enough for suppression of leakage current. The value of Φ_{bp} can be derived from the measured dielectric band gap E_g and valence band offset Φ_{bp} using the relation $\Phi_{bn} = E_g - \Phi_{bp}$. The valence band offset of a thin heterostructure can be experimentally determined by a method in which the measured XPS valence band spectrum is deconvoluted into curves of the constituent materials that are separately observed[19, 20]. Fig. 5.5(b) and Fig. 5.5(c) show the deconvolution of the valence-band spectra for 5.0 nm-thick Sm_2O_3 on TaN and Pt, respectively. The results indicate that the barrier heights for holes are 2.64 eV for TaN, and 2.17 eV for Pt. Using these values and the measured Sm_2O_3 band gap of 5.20 eV, the electron barrier heights for TaN electrode and Pt electrode are determined to be 2.56 eV and 3.03 eV, respectively. Fig. 5.5(d) summarizes the results obtained. Considering TaN or Pt as possible electrode materials, the larger conduction band offset for a Pt electrode

suggests that the leakage current should be lower. In this work, we use TaN instead of Pt as the electrode due to the ease of etching TaN for electrode definition.

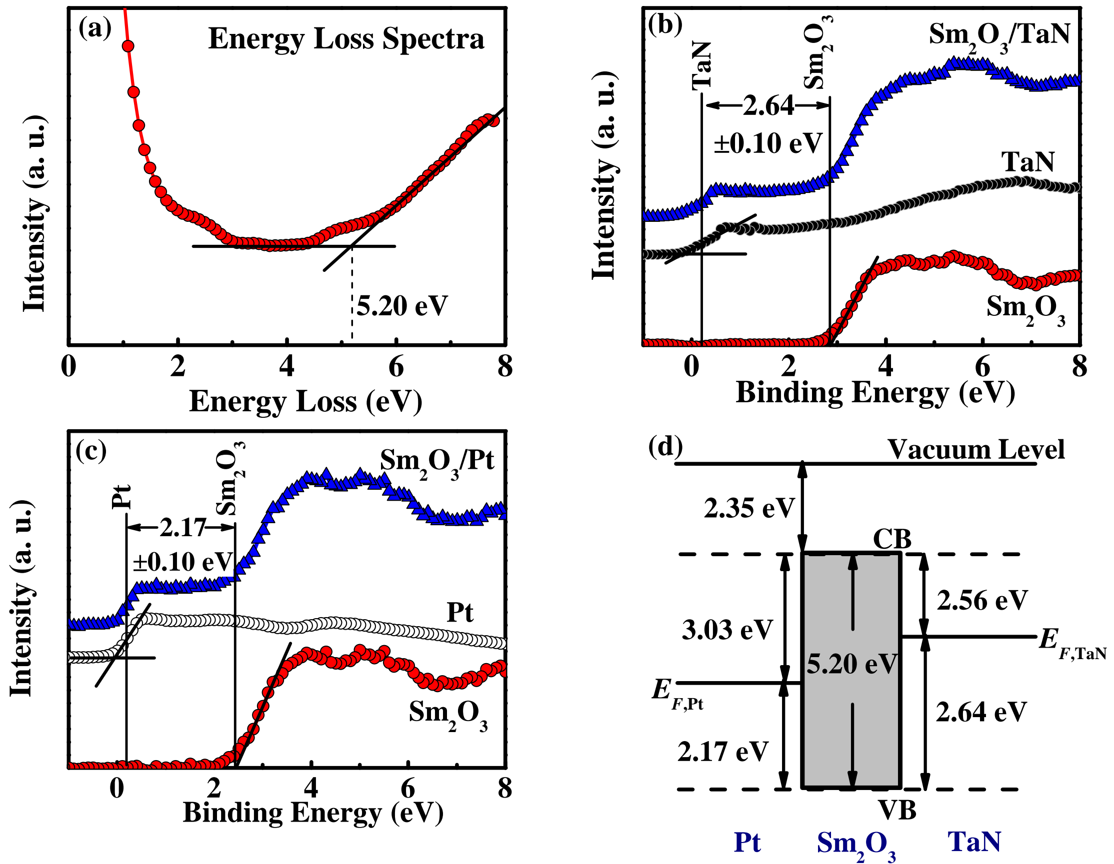

Fig. 5.5. (a) Oxygen (O) 1*s* energy-loss spectra obtained from bulk Sm_2O_3 which went through a 400 ℃ post-deposition anneal (PDA). The energy band gap of Sm_2O_3 is 5.20 eV. (b) Valence-band spectrum for Sm_2O_3/TaN and the deconvoluted spectra for thick Sm_2O_3 and TaN. (c) Valence-band spectrum for Sm_2O_3/Pt and the deconvoluted spectra for thick Sm_2O_3 and Pt. (d) Energy-band diagram showing the band alignment for Pt, Sm_2O_3, and TaN.

5.3.2 Electrical Characterization

VCCs are crucial parameters for MIM capacitor for analog applications, and can be obtained by fitting the measured data with a second order polynomial equation,

$$C(V) = C_0(\alpha V^2 + \beta V + 1), \tag{5.1}$$

where C_0 is the zero-bias capacitance, α is the quadratic voltage coefficient of capacitance, and β is the linear voltage coefficient of capacitance. Fig. 5.6(a) shows the bias-dependent normalized capacitance ($\Delta C/C_0$) fitted by eq. (5.1). The fitting procedure extracted the values of α and β. It is observed that both α and β decrease with increasing dielectric thickness. The dependence of $\Delta C/C_0$ on the electric field E is shown in Fig. 5.6(b). The curves roughly coincide for Sm_2O_3 dielectrics with various thicknesses.

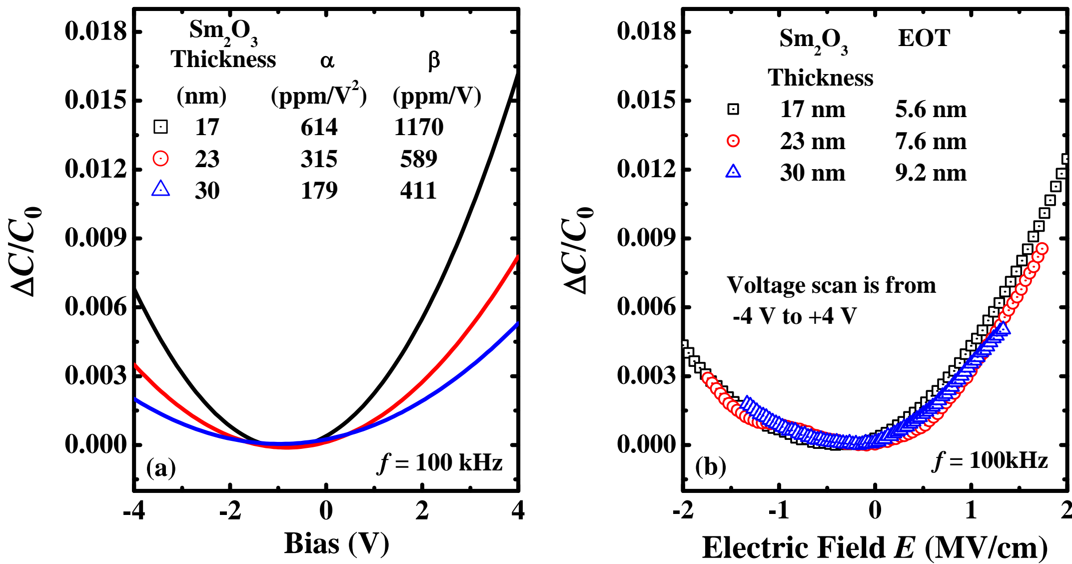

Fig. 5.6. (a) Voltage-dependant normalized capacitance ($\Delta C/C_0$) measured at 100 kHz for MIM capacitors with a single Sm_2O_3 dielectric layer having a thickness of 17 nm, 23 nm, or 30 nm. By fitting a second-order polynomial equation (solid lines) to the experimental data (plotted in symbols), the quadratic voltage coefficient of capacitance α and the linear voltage coefficient of capacitance β are obtained. (b) Plot of $\Delta C/C_0$ versus electric field E for the same MIM capacitors in (a).

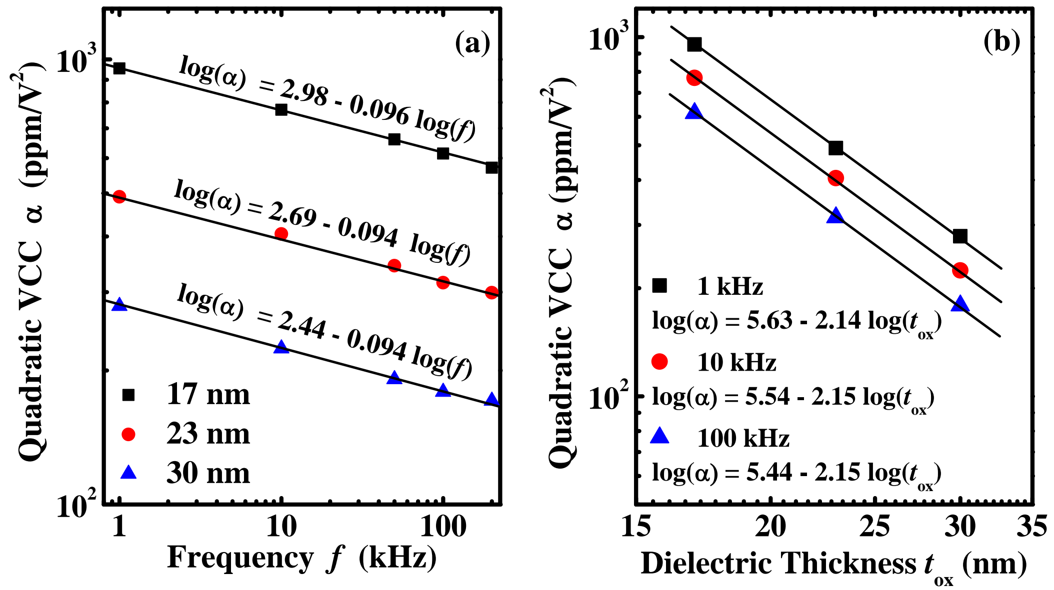

Fig. 5.7. **(a)** Frequency dependence of α for MIM capacitors with a single Sm_2O_3 dielectric layer having a thickness of 17 nm, 23 nm, and 30 nm. The straight lines are a linear fit to the data points on a log-log scale. (b) Thickness dependence of α at 1 kHz, 10 kHz, and 100 kHz with a linear fit (solid line) in log-log scale to experimental data (symbols).

The effect of the applied frequency f on α is shown in Fig. 5.7(a). The logarithm of α [i.e. log(α)] decreases linearly with a logarithmic increase in frequency. The slope of the log(α) versus log(f) is approximately constant for various MIM dielectric thicknesses. The frequency dependence of α can be explained as the change of relaxation time with different carrier mobility in insulator [21].

Furthermore, α is plotted against dielectric thickness in Fig. 5.7(b). α decreases linearly with increasing dielectric thickness t_{ox} on a log-log scale, exhibiting a similar slope at various applied frequencies. This reveals that the thickness dependence of α can be expressed as $\alpha \propto t_{ox}^{-2.15}$, which is consistent with Ref. [22]. Nonlinearities of MIM capacitors are typically quadratic in E-field, but the coefficient α is defined with respect to applied voltage. As a result, α should have a $1/t_{ox}^2$ dependence on the dielectric thickness [21]. Interfacial layer between the

electrode and dielectric, and the thickness dependence of refractive index both lead to imperfections in the $1/t_{ox}^2$ scaling factor [21].

Fig. 5.8 shows the leakage current density *J* for MIM capacitors having Sm_2O_3 dielectric with various thicknesses at room temperature. The leakage currents at +3.3 V and –3.3 V are above 10^{-7} A/cm^2. The *J-V* curve becomes asymmetric at higher bias, indicating that the capacitor may be physically asymmetric, i.e. electrode-dielectric interface quality is different for the bottom and top interfaces. It is conceivable that the bottom interface is of a poorer quality than the top interface, considering that plasma nitridation before PDA helped enhance the quality of top TaN-Sm_2O_3 interface and that the bottom Sm_2O_3-TaN interface experienced a higher thermal budget (e.g. an additional PDA at 400 ℃) which may lead to interfacial reaction. This possibly explains the higher leakage at large positive bias where electron injection occurs from the bottom electrode.

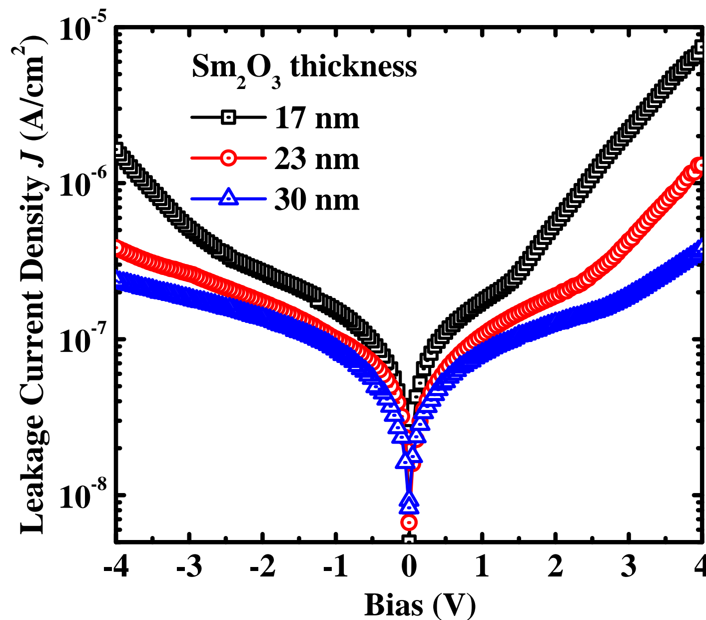

Fig. 5.8. Room temperature *J-V* characteristics of MIM capacitors with a single Sm_2O_3 dielectric layer having a thickness of 17 nm, 23 nm, and 30 nm.

5.4 MIM Capacitors with a single layer Er_2O_3 dielectric

5.4.1 Physical Characterization

Fig. 5.9(a) shows a cross-section of a typical MIM capacitor. A TEM image of a MIM capacitor with a single Er_2O_3 dielectric is shown in Fig. 5.9(b). It should be noted that the Er_2O_3 layer is poly-crystalline in Fig. 5.9(b). This capacitor has a capacitance density of 8.7 fF/μm^2. Together with the physical thickness from TEM, the dielectric constant of Er_2O_3 is calculated to be 19.7. The κ value of Er_2O_3 is slightly higher than that of Sm_2O_3 (19).

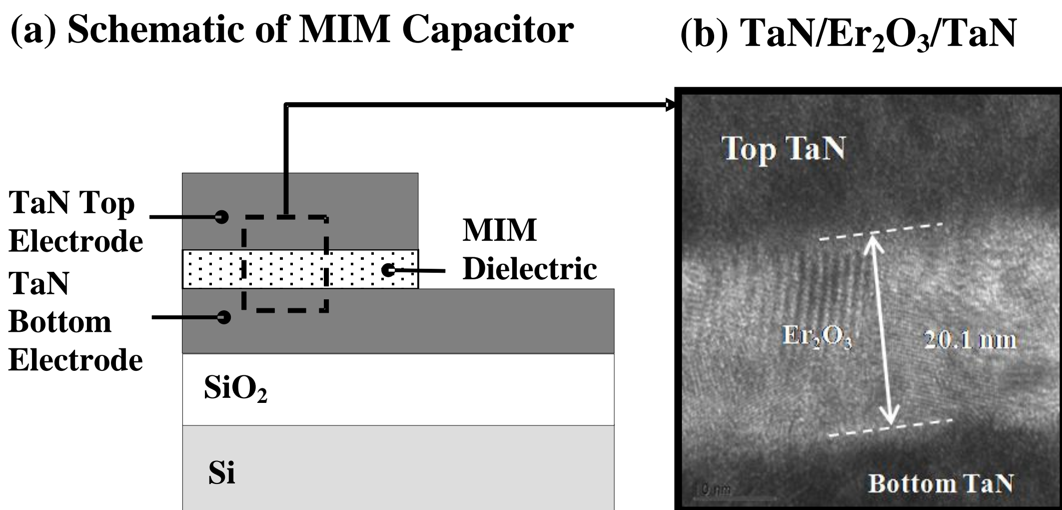

Fig. 5.9. (a) Schematic of Metal-Insulator-Metal (MIM) capacitor having top and bottom tantalum nitride (TaN) electrodes. (b) In one split, the MIM dielectric is a single Er_2O_3 layer, as shown in the cross-sectional transmission electron microscopy (TEM) image.

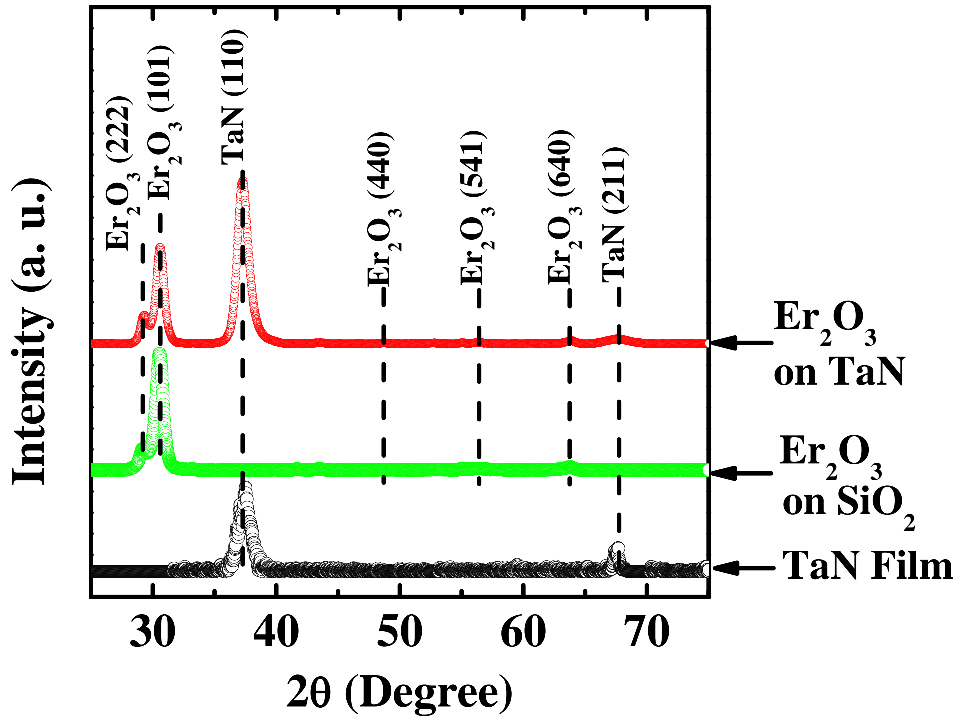

Fig. 5.10. XRD spectra of Er_2O_3 on SiO_2 and TaN, after being annealed at 400 ℃. XRD spectrum of an exposed TaN surface is also obtained. The Er_2O_3 films are polycrystalline.

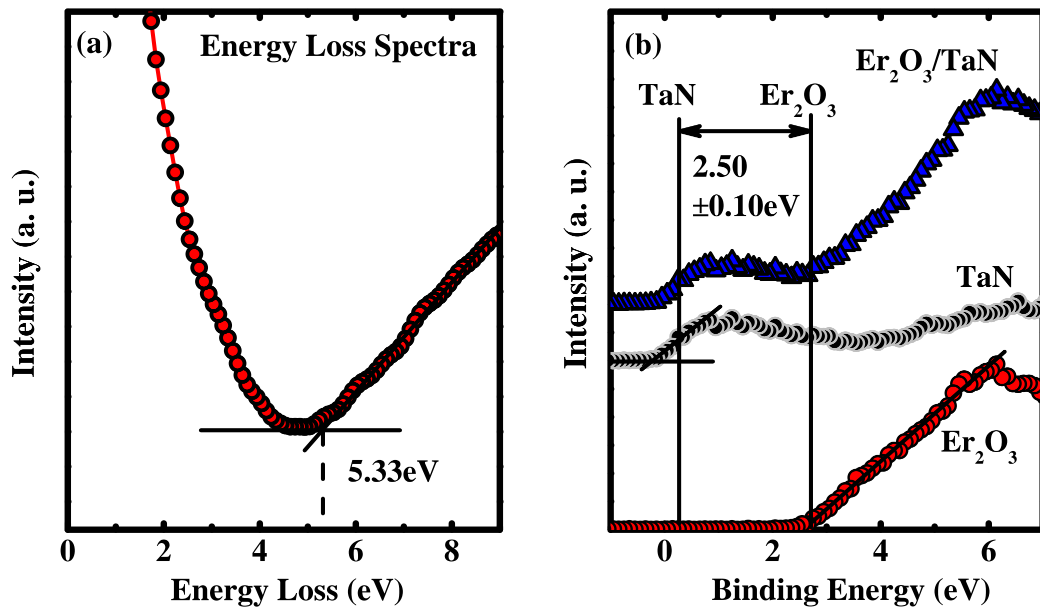

Fig. 5.11. (a) Oxygen (O) 1*s* energy-loss spectra obtained from bulk Er_2O_3 which went through a 400 ℃ post-deposition anneal (PDA). The energy band gap of Er_2O_3 is 5.33 eV. (b) Valence-band spectrum for Er_2O_3/TaN and the deconvoluted spectra for Er_2O_3 and TaN.

50 nm Er_2O_3 films were prepared for analysis of the crystalline structure using XRD as shown in Fig. 5.10. The 50 nm Er_2O_3 films were either deposited directly on a 200 nm thick TaN or on a 500 nm thick amorphous SiO_2, and annealed at 400 ℃ before XRD analysis. The Er_2O_3 peaks did not differ much for TaN and SiO_2 substrates, indicating the phase and composition were not affected by substrate materials.

Next, we derive the energy band gap E_g of Er_2O_3 from the O 1*s* energy-loss spectra of bulk Er_2O_3 film, as shown in Fig. 5.11(a). Taking the similar approach as in section 5.3.1, the energy gap for Er_2O_3 was obtained to be 5.33 $\pm$0.10 eV, which is consistent with a previously reported value of 4.9 to 5.5 eV [17]. The E_g of Er_2O_3 is seen to be comparable with other commonly used high-κ materials such as HfO_2 (5.25 eV) [18], Gd_2O_3 (5.5 eV) [17], and the previously discussed Sm_2O_3 (5.2 eV).

Φ_{bn} and Φ_{bp} are derived from XPS spectra. Fig. 5.11(b) shows the deconvolution of the valence-band spectra for 4.0 nm-thick Er_2O_3 on TaN. The results indicate that the barrier height for holes is 2.50 eV for TaN. Using this value and the measured Er_2O_3 band gap of 5.33 eV, the electron barrier height for TaN electrode is determined to be 2.83 eV.

5.4.2 Electrical Characterization

The ambient oxygen concentrations during the deposition and the PDA process were varied to find the optimal condition for Er_2O_3 formation. Fig. 5.12 shows the capacitance obtained at the different PDA conditions. For the capacitor with 10 nm Er_2O_3, the capacitance density drops significantly with increased O_2 flow in PDA process. However, the capacitance only drops slightly for 20 nm sample, and remains constant for the 30 nm one. The deceased capacitance with increased oxygen in the PDA ambient is possibly due to the oxidation of the bottom TaN electrode, which forms another layer of oxide and decreases the capacitance density. Thicker Er_2O_3 serves as an oxygen barrier for the bottom electrode.

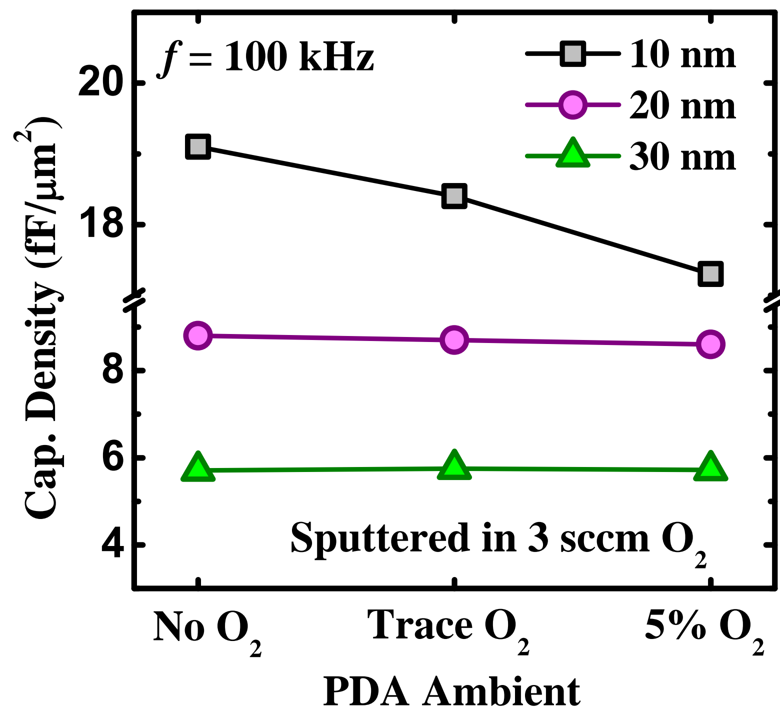

Fig. 5.12. The change of capacitance densities as a function of oxygen concentration in PDA ambient. The increased oxygen concentration has a larger impact on 10 nm Er_2O_3 than that on 20 nm and 30 nm Er_2O_3.

Fig. 5.13(a) demonstrates typical *C-V* curves of MIM capacitors with 10 nm Er_2O_3 deposited in 27-sccm Ar/3-sccm O_2. The quadratic VCC α and linear VCC β are extracted by equation (5.1). It is obvious that the split with Er_2O_3 annealed in trace O_2 has the smallest α. Furthermore, we plot α versus dielectric thickness in Fig. 5.13(b). It is found that α linearly decreases with increasing dielectric thickness t_{ox} on a log-log scale. The fitted slopes are all around 2. The slope (s) indicates that the thickness dependence of α can be expressed as $\alpha \propto t_{ox}^{s}$. The small difference between the slopes of the three PDA conditions are probably due to the interfacial layer between the electrode and dielectric, and different oxygen vacancy concentrations, which lead to imperfections in the $1/t_{ox}^{2}$ scaling factor [21].

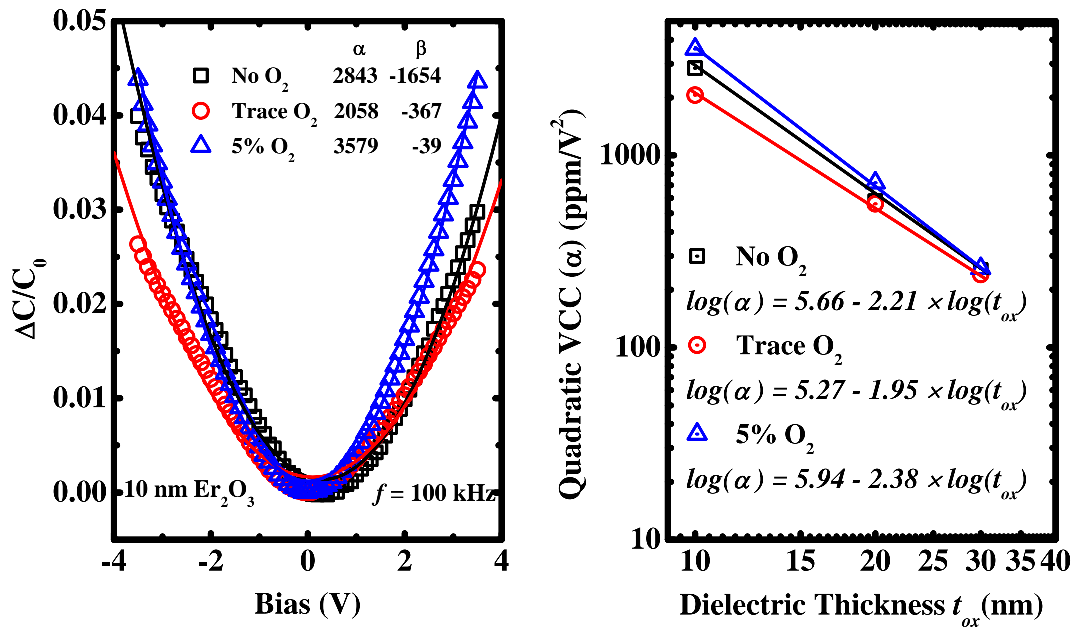

Fig. 5.13. (a) Voltage-dependant normalized capacitance ($\Delta C/C_0$) measured at 100 kHz for MIM capacitors with a single 10 nm Er_2O_3 dielectric layer annealed in different oxygen concentrations. By fitting a second-order polynomial equation (solid lines) to the experimental data (plotted in symbols), the quadratic voltage coefficient of capacitance α and the linear voltage coefficient of capacitance β are obtained. (b) Thickness dependence of α with a linear fit (solid line) in log-log scale to experimental data (symbols).

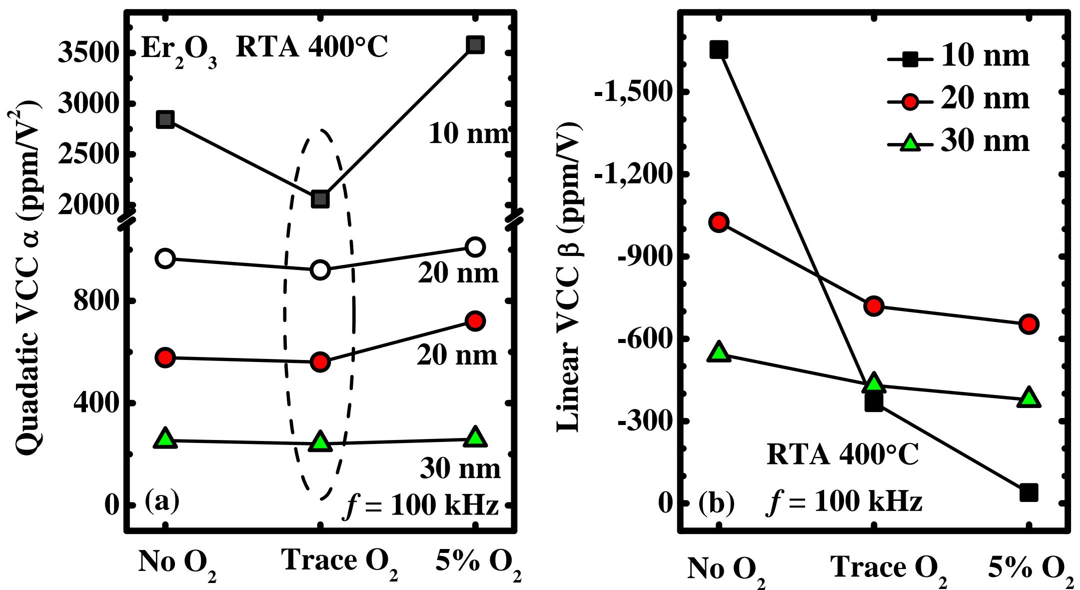

Fig. 5.14. (a) Quadratic VCC α as a function of oxygen concentration in PDA ambient. The solid symbols represent MIM capacitors with Er_2O_3 deposited in 27-sccm Ar/3-sccm O_2 during the PVD; the open symbols represent MIM capacitors with Er_2O_3 deposited in 28-sccm Ar/2-sccm O_2 during the PVD. (b) Linear VCC β as a function of oxygen concentration in PDA ambient.

Fig. 5.14(a) summarizes the change of α values obtained. The capacitor with Er_2O_3 sputtered in 28-sccm Ar/2-sccm O_2 exhibits significantly higher α comparing to that with Er_2O_3 sputtered in 3 sccm O_2, although their Er_2O_3 thicknesses and capacitance densities are almost the same. Lower concentration of O_2 during the deposition may have caused high density oxygen vacancies in the oxide, which was not effectively rehabilitated by the low temperature PDA process. For each thickness, capacitors annealed in trace O_2 ambient demonstrate smaller α than the other two PDA conditions. This effect is more pronounced on thinner Er_2O_3. This implies that a proper amount of O_2 must be present during the PDA process to maintain a small α, i.e., a small amount of O_2 in PDA process is helpful for higher quality Er_2O_3 with less trapping charges and defects; but excess O_2 increases the α. It is known that Ta_2O_5 has a large quadratic VCC [8]. The excess oxygen penetrates to the bottom electrode and

forms a thin Ta_2O_5 layer; the degraded interface leads to charge trapping and double layer-capacitance, and consequently increases α. Due to the large α value, we do not further characterize the samples deposited in 28-sccm Ar/2-sccm O_2 in the rest of the paper.

Linear VCC β values are summarized in Fig. 5.14(b). β is related to asymmetric device structure or process. β reduces with increased oxygen concentration during PDA. This is also related to the bottom interface. During the annealing, the oxygen penetrates from top surface of Er_2O_3 to the bottom interface. If there is not enough oxygen, the bottom interface would have more oxygen vacancies than the top surface. This effect is less pronounced for thicker oxides because oxygen has less influence on the bottom interface due to the thick oxide barrier.

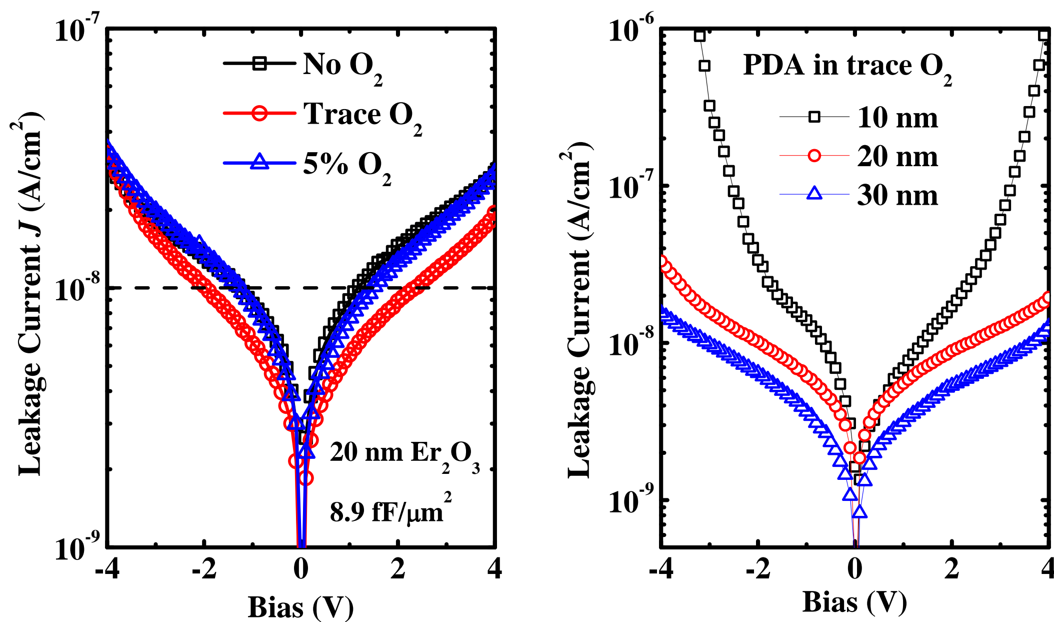

Fig. 5.15. (a) Effect of oxygen concentration during PDA on *J-V* characteristics of MIM capacitors with 20-nm single Er_2O_3 dielectric layer; (b) Comparison of *J-V* characteristics of MIM capacitors with a single Er_2O_3 dielectric layer having a thickness of 10, 20 and 30 nm with a PDA in trace oxygen.

Fig. 5.15(a) shows the dependence of leakage current density *J* on voltage at room temperature for MIM capacitors having 20-nm Er_2O_3 dielectric with various annealing conditions. *J* is at the order of 10^{-8} A/cm^2 at ±3.3 V bias for all the 3 different annealing conditions. The capacitor with Er_2O_3 annealed in trace O_2 during PDA has a smaller *J* than the other two. *J-V* curve becomes asymmetric at higher bias, indicating that the MIM capacitor is physically asymmetric, i.e. bottom and top interfaces are different. Fig. 5.15(b) shows the leakage current density for MIM capacitors with 10 nm, 20 nm and 30 nm Er_2O_3 deposited in 27-sccm Ar/3-sccm O_2 and annealed in trace O_2.

For application in precision analog circuits, quadratic VCC and leakage current are the two key factors and must be kept as small as possible. Considering the results discussed above, we decided the optimized process condition for Er_2O_3 deposition to be: 27-sccm Ar/3-sccm O_2 flow during reactive sputtering and trace O_2 in PDA process. The following characterizations were all performed on devices formed with this process condition.

Fig. 5.16 shows the capacitance densities and loss tangent (1/*Q* factor) of Er_2O_3 MIM capacitors, as a function of frequency measured at zero DC bias. The capacitance density almost remains the same for all the three thicknesses. This indicates that the cut-off frequency f_c is lower than 1 kHz at zero bias. The cut-off frequency f_c is related to the relaxation time of the dielectric [23, 24]. The loss tangent increases from ~10^{-4} at 1 kHz to ~10^{-2} at 100 kHz for all samples. A lower loss tangent is preferred for less energy loss.

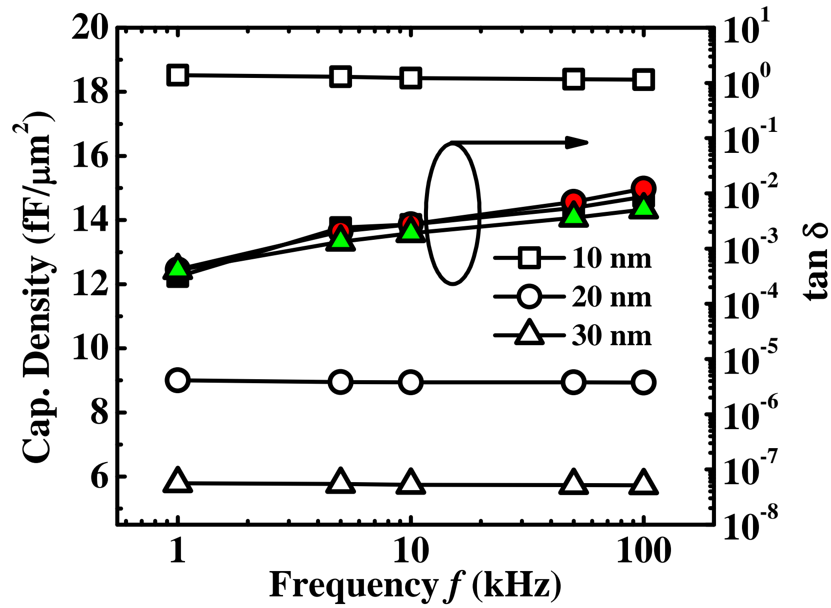

Fig. 5.16. Frequency dependence of capacitance density and frequency dispersion of loss tangent ($1/Q$ factor) for MIM capacitors with a single Er_2O_3 dielectric layer having a thickness of 10 nm, 20 nm, and 30 nm. The open symbols represents capacitance density; while the solid symbols represent the loss tangent.

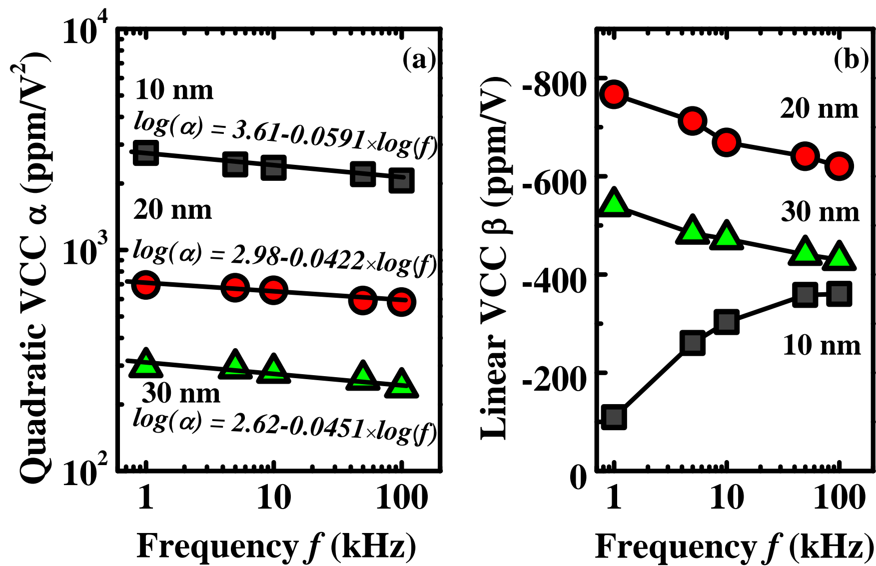

Fig. 5.17. (a) Frequency dependence of α for MIM capacitors with a single Er_2O_3 dielectric layer having a thickness of 10 nm, 20 nm, and 30 nm, annealed in trace O_2. The straight lines are a linear fit to the data points on a log-log scale. (b) Frequency dependence of β for MIM capacitors with a single Er_2O_3 dielectric layer having a thickness of 10 nm, 20 nm, and 30 nm, annealed in trace O_2.

The frequency dispersion of α and β are shown in Fig. 5.16. The logarithm of α [i.e. log(α)] decreases linearly with a logarithmic increase in frequency. The frequency dependence of α can be explained as the change of relaxation time with different carrier mobility in insulator [21]. The slope for 20 nm and 30 nm Er_2O_3 MIM capacitors are close to each other, but both are much smaller than that of the 10 nm one. The linear VCC (β) decreases with increasing frequency for 20 nm and 30 nm Er_2O_3 capacitors, but increases for the 10 nm split. The inconsistent behavior of the 10 nm sample should be due to the interfacial layer at the bottom interface.

5.5 Further Reduction of quadratic VCC by stacking with SiO_2

5.5.1 Device Structure and Cancelling Effect

Although Sm_2O_3 and Er_2O_3 show lower quadratic VCCs than most of other high-κ dielectrics, further improvement is needed to meet the requirement specified by ITRS (< 100). It has been demonstrated that VCC values can be actively engineered and virtually zero VCC can be achieved without a significant decrease of capacitance density, by using a stacked insulator structure of high-κ and SiO_2 dielectrics [25]. Such "canceling effect" was successfully demonstrated in HfO_2/SiO_2 MIM capacitors with a capacitance density of around 6 fF/μm^2 and a quadratic VCC α of 14 ppm/V^2 [25]. Fig. 5.18 shows the cross sectional schematics of an MIM capacitor with two layers of stacked dielectrics.

According to the theory of "cancelling effect", the ratio of EOT of each dielectric layer to the whole EOT of stacked dielectrics plays a significant role in determining the effective value of α [25]. For a dual layer dielectric stack, i.e. s

structure, the relationship between α and the thicknesses of the constituent dielectrics is given by [25]:

$$\alpha = \delta_1^3 \alpha_1 + \delta_2^3 \alpha_2 \quad (5.2)$$

$$\beta = \delta_1^2 \beta_1 + \delta_2^2 \beta_2 \quad (5.3)$$

$$\delta_i = \frac{EOT_i}{EOT_{total}}, i = 1, 2 \quad (5.4)$$

where EOT_i is the EOT of the ith layer, and EOT_{total} is the EOT of the entire dielectric stack. The α values of both dielectrics at each thickness are derived from data from MIM capacitors with a single Sm_2O_3 layer or a single SiO_2 layer. Simulation results showing the relation between α of a Sm_2O_3/SiO_2 stack with the thicknesses of each layer is given in Fig. 5.19. The region between the two dashed lines is where α is within ±100 ppm/V^2, a target for our MIM dielectric design. As the Sm_2O_3 layer thickness is reduced, the curve runs through the target region in Fig. 5.19 over a narrower range of SiO_2 thicknesses. If we use a thinner Sm_2O_3 layer, a more precise SiO_2 thickness control is needed to attain an α within ±100 ppm/V^2. The simulation, however, ignores process and structural differences between capacitors with single layer or laminate dielectrics. It only provides a rough guideline for thickness combinations (gray region) to be explored in the experiment.

During the fabrication of MIM capacitors with two layers of dielectrics, SiO_2 was deposited by Plasma-enhanced chemical vapor deposition (PECVD) on the bottom TaN at 350 ℃. The tool used for SiO_2 deposition was an Applied Materials Centura-5200. Other processes were the same as that of MIM capacitors with single layer dielectric discussed in section 5.2.1.

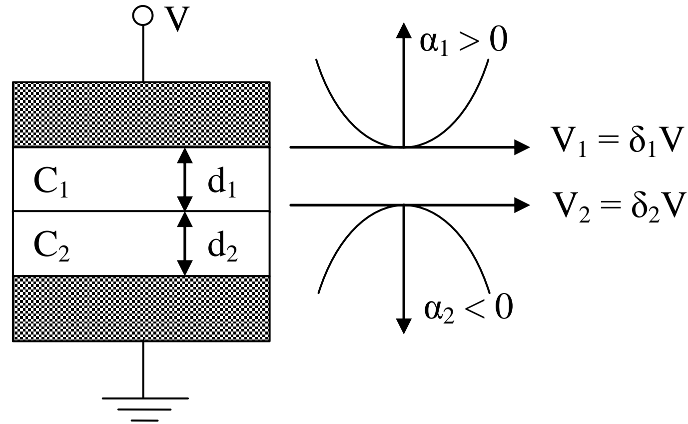

Fig. 5.18. Cross sectional schematics of an MIM capacitor with stacked dielectrics. When two different capacitors are connected in series, voltages divided in the stack decide the voltage linearity of the capacitance of the stack.

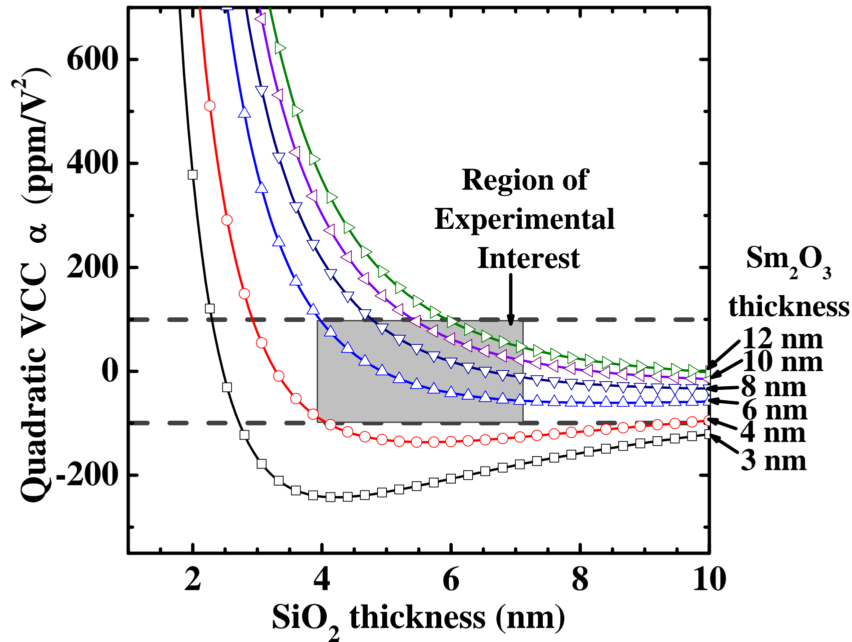

Fig. 5.19. Simulated α versus SiO_2 thickness plot for different Sm_2O_3 thicknesses from 3 to 12 nm. The value of α should preferably be within ±100 ppm/V^2, as indicated by the horizontal dashed lines. The choice of SiO_2 and Sm_2O_3 thicknesses should preferably be in the target region where α is small and relatively insensitive to a variation in the thickness of SiO_2. The gray region shows the range of thicknesses of SiO_2 and Sm_2O_3 to be selected in our experiment.

5.5.2 MIM Capacitors with Sm_2O_3/SiO_2 dielectric stack

MIM capacitors with Sm_2O_3/SiO_2 laminated dielectric having SiO_2 thickness varying from 2.8 to 7 nm and Sm_2O_3 thickness varying from 6.5 to 10 nm were fabricated to investigate the "cancelling effect" of SiO_2 (or Sm_2O_3) in Sm_2O_3/SiO_2. The split table is shown in Table 5.1, corresponding to the gray region in Fig. 5.19. Table 5.1 also shows the measured capacitance density of each split.

Fig. 5.20 shows the cross sectional TEM image of an MIM capacitor with Sm_2O_3 on top of SiO_2. Poly-crystalline Sm_2O_3 was formed on amorphous SiO_2. There is a 1.8 nm interfacial layer between SiO_2 and TaN electrode.

Fig. 5.21 shows the normalized *C-V* curves of the MIM capacitors with 8.5 nm thick Sm_2O_3 on various thicknesses of SiO_2 underlying layer. The quadratic VCC is improved with the introduction of SiO_2 under-layer. In fact, for larger SiO_2 thicknesses used, e.g. 7 nm, the quadratic VCC actually turns negative. The asymmetric *C-V* curves in Fig. 5.22 indicate a non-zero linear VCC β, and that is a direct consequence of the asymmetric device structure, which leads to different interface band alignments and trap densities at the top and the bottom electrode-dielectric interfaces of the MIM capacitor.

Table 5.1. Split table for MIM capacitors with Sm_2O_3-on-SiO_2 laminate dielectric, showing the thicknesses of Sm_2O_3 and SiO_2 used in each split and the capacitance density measured.

SiO_2	Sm_2O_3 Thickness			
Thickness	6.5 nm	7.5 nm	8.5 nm	10 nm
2.8 nm	9.8 fF/μm^2	9.0 fF/μm^2	8.0 fF/μm^2	7.4 fF/μm^2
3.5 nm	8.3 fF/μm^2	7.8 fF/μm^2	7.2 fF/μm^2	6.7 fF/μm^2
3.8 nm	7.9 fF/μm^2	7.3 fF/μm^2	6.9 fF/μm^2	6.4 fF/μm^2
4.8 nm	6.8 fF/μm^2	6.4 fF/μm^2	6.2 fF/μm^2	5.6 fF/μm^2
7.0 nm	4.9 fF/μm^2	4.8 fF/μm^2	4.5 fF/μm^2	4.4 fF/μm^2

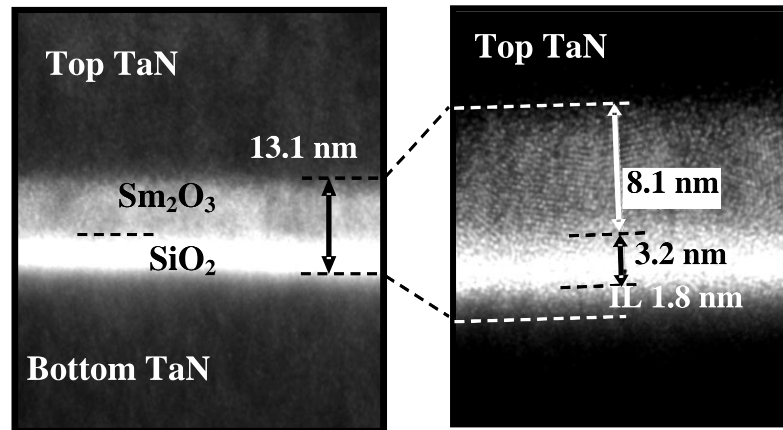

Fig. 5.20. The left figure shows a Sm_2O_3 layer formed on a SiO_2 layer as the dielectric in a MIM capacitor with TaN electrodes. A high resolution TEM image is given on the right, clearly showing the presence of an interfacial layer (IL) between SiO_2 and the TaN bottom electrode.

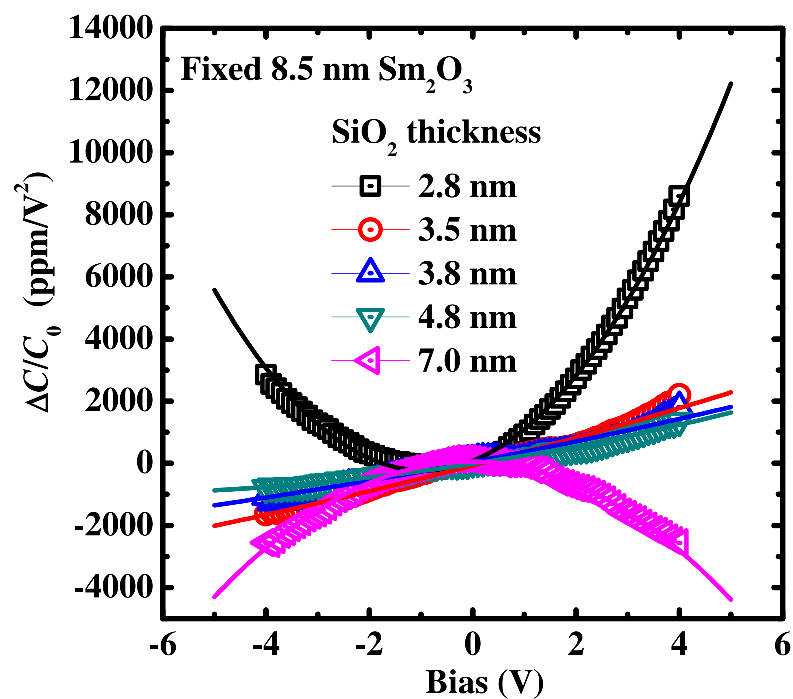

Fig. 5.21. Normalized *C-V* curves of Sm_2O_3/SiO_2 MIM capacitors with Sm_2O_3 fixed at 8.5 nm while varying SiO_2 thickness from 2.8 nm to 7 nm. Curvature of *C-V* curves changes from positive to negative as the SiO_2 thickness is increased.

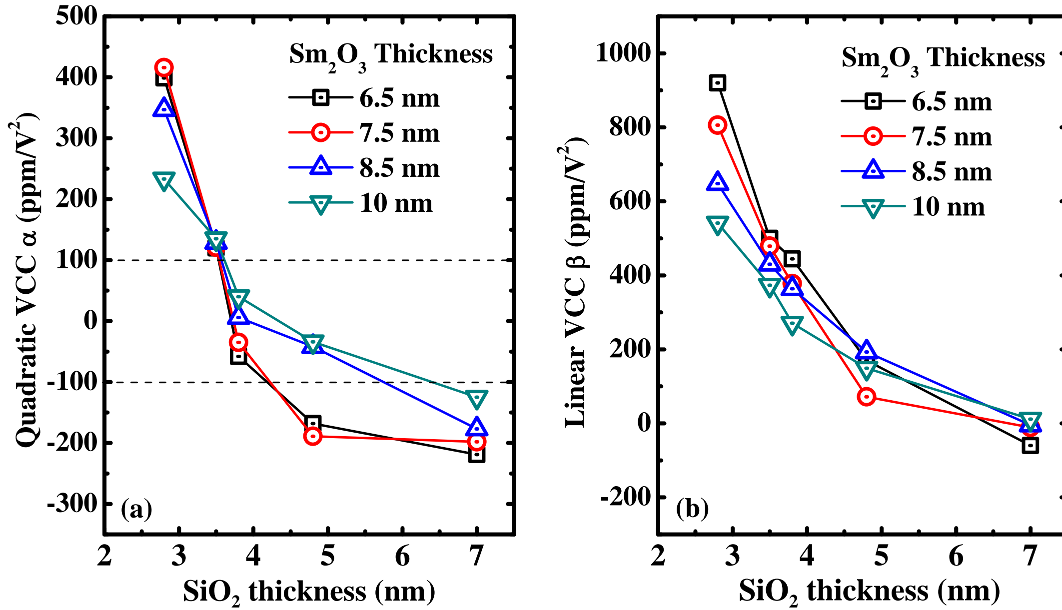

Fig. 5.22. (a) Quadratic VCC (α value) versus the thickness of SiO_2 with varying the thickness of SiO_2 and Sm_2O_3. (b) Linear VCC (β value) versus the thickness of SiO_2 with varying the thickness of SiO_2 and Sm_2O_3. Both α value and β value can be modulated by increasing the thickness of SiO_2 layer. Near zero α value can be obtained by optimizing the EOT ratio of SiO_2 to Sm_2O_3/SiO_2 stack.

Fig. 5.22(a) summarizes the measured α of Sm_2O_3/SiO_2 dielectric stacks versus varying SiO_2 thickness (from 2.8 nm to 7 nm) at different Sm_2O_3 thicknesses (6.5 nm, 7.5 nm, 8.5 nm and 10 nm). For each Sm_2O_3 thickness, the capacitance density of Sm_2O_3/SiO_2 MIM capacitors decreases with increasing SiO_2 thickness. Consequently, α is effectively modulated from positive to negative values because of the increasing of ratio of the SiO_2 thickness to the total thickness of the Sm_2O_3/SiO_2 stack. High capacitance densities of 7.3 fF/μm^2 and 7.9 fF/μm^2 with α of -46 ppm/V^2 and -56 ppm/V^2 were successfully demonstrated using Sm_2O_3/SiO_2 thickness of 6.5 nm/3.8 nm and 7.5 nm/3.8 nm, respectively. Furthermore, from the change of α with capacitance density, it is possible to achieve capacitance density of over 8 fF/μm^2 and α of near zero ppm/V^2 by optimizing the ratio of SiO_2 thickness to EOT of the dielectric stack. The above experimental results satisfy the requirements of MIM

capacitors for precision analog circuit applications until year 2013. The modulation of linear VCC β due to a varying SiO_2 thickness in a Sm_2O_3/SiO_2 dielectric is summarized in Fig. 5.22(b). β is reduced with an increase in the SiO_2 thickness.

The effect of the measurement frequency on α is depicted in Fig. 5.23. It can be observed that the logarithm of α [log(α)] decreases linearly with a logarithmic increase in frequency. This is similar to the behavior of MIM capacitors with a single Sm_2O_3 dielectric in Fig. 5.7(a).

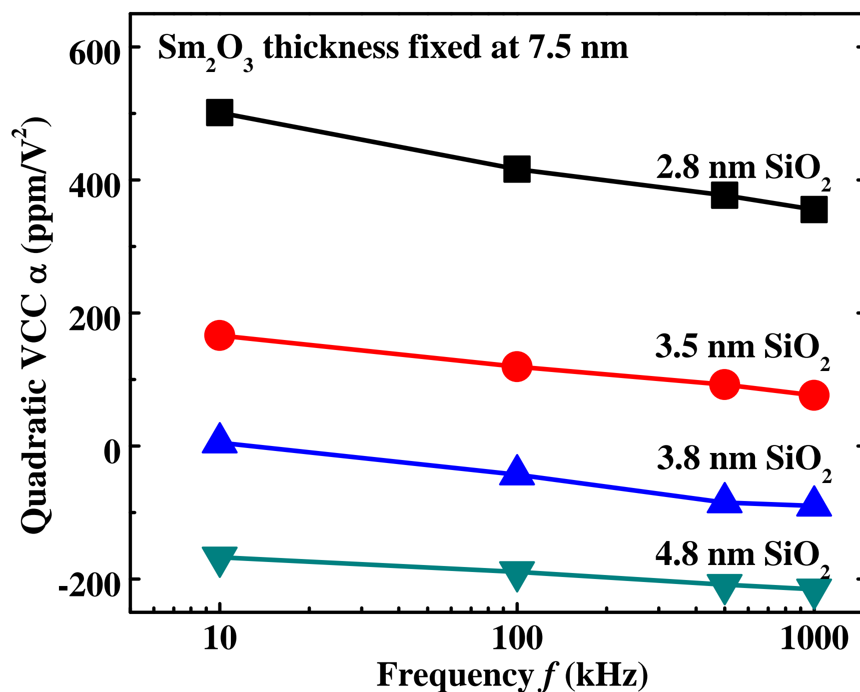

Fig. 5.23. Frequency dependence of α for the Sm_2O_3/SiO_2 MIM capacitors with Sm_2O_3 fixed at 7.5 nm while varying SiO_2 thickness from 2.8 nm to 4.8 nm.

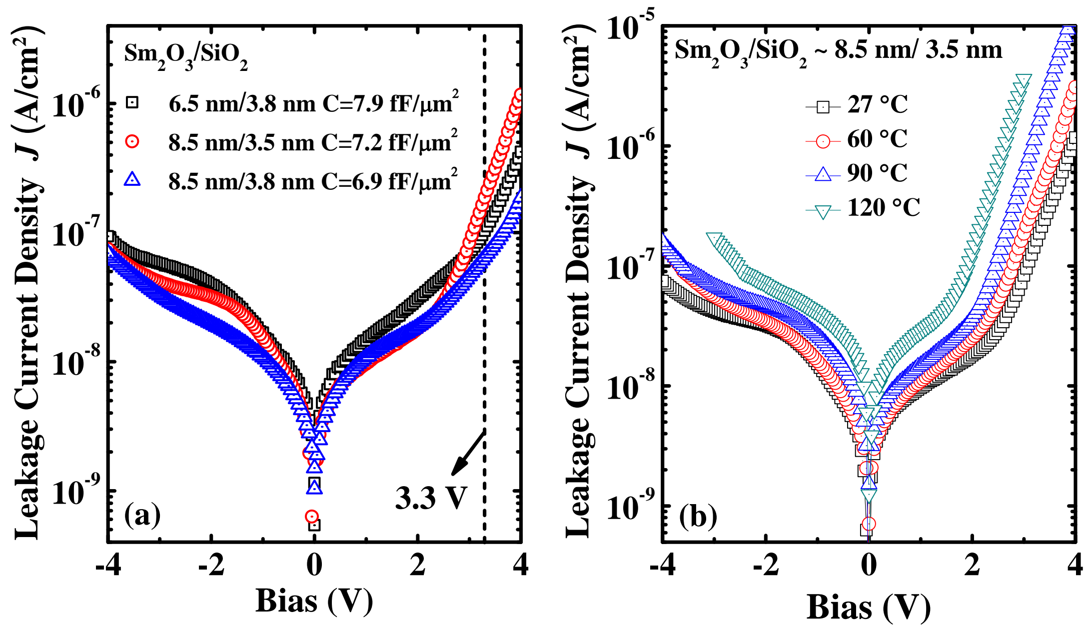

Fig. 5.24. (a) *J-V* characteristics of Sm_2O_3/SiO_2 MIM capacitors with 3 different thickness combinations at room temperature; (b) *J-V* characteristics of Sm_2O_3/SiO_2 MIM capacitors with 8.5 nm Sm_2O_3 and 3.5 nm SiO_2 measured at different temperatures (27-120 ℃).

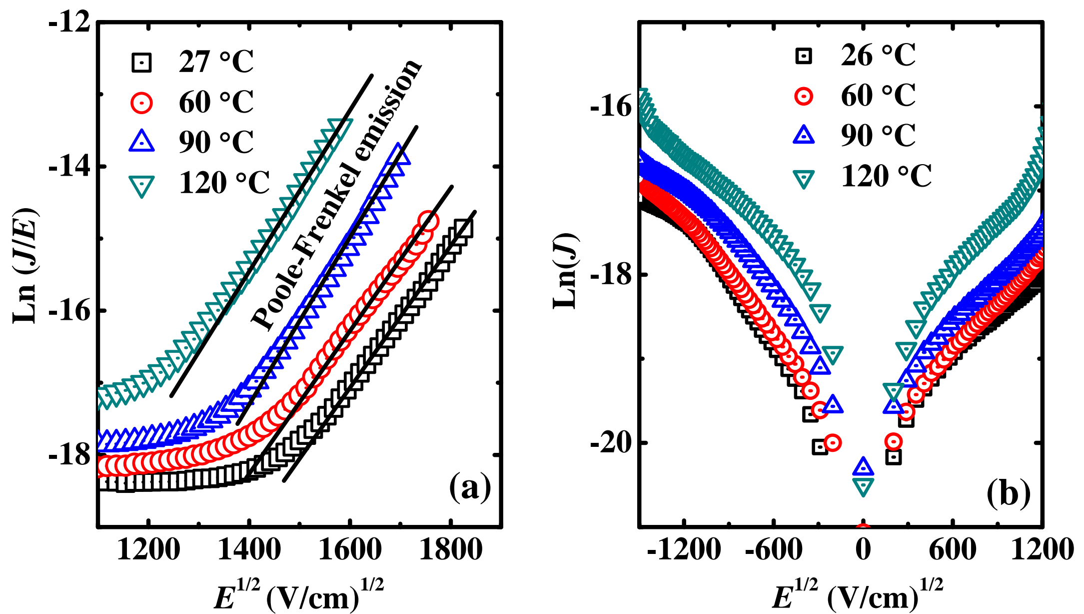

Fig. 5.25. (a) Plot of ln(*J*/*E*) versus $E^{1/2}$ as a function of temperature together with the linear fitting for the leakage current at high positive bias; (b) Plot of ln(*J*) versus $E^{1/2}$ as a function of temperature at low bias.

Fig. 5.24(a) shows the dependence of leakage on various Sm_2O_3/SiO_2 thickness combinations at room temperature. The leakage current density at 3.3 V are 1.86×10^{-7} A/cm^2, 1.03×10^{-7} A/cm^2, and 6.48×10^{-8} A/cm^2, for Sm_2O_3/SiO_2 thicknesses of 8.5 nm/3.5 nm, 6.5 nm/3.8 nm, and 8.5 nm/3.8 nm, respectively. Further evaluation of the leakage characteristics of the laminate MIM capacitors involves *J*-*V* characterization at the maximum operating temperature of 120 ℃. Fig. 5.25(b) shows the *J*-*V* curves for the laminate capacitors with 8.5 nm Sm_2O_3 on 3.5 nm SiO_2 measured from room temperature to 120 ℃.

The *J*-*V* characteristics exhibit two distinct regions under positive bias. One is the low bias region (typically from 0 to 2.5 V) where the leakage current increases gradually with the applied voltage; the other is the high bias region (> 2.5V) where the leakage current increases more sensitively with increase in the applied voltage. The phenomena reflect different current transport mechanisms. For the negative bias, the rapid increase in current with increasing voltage does not appear until -3.5 V. It is believed that the Poole-Frenkel (P-F) emission is due to field-enhanced thermal excitation of trapped electrons. The conduction process at high bias in Fig. 5.24 (a) is likely dominated by P-F emission. To further verify the possible effect, $\ln(J/E)$ versus $E^{1/2}$ is plotted in Fig. 5.25(a) at different temperatures for high positive bias. On the other hand, $\ln(J)$ versus $E^{1/2}$ is also plotted in Fig. 5.25(b) for both positive and negative biases. The leakage currents at low bias voltage show obvious temperature dependence, indicating that the leakage current at low electric field is likely due to Schottky emission.

The *J*-*V* curves in Fig. 5.24(b) are asymmetric at the measurement temperatures shown. This asymmetry in leakage current density may be contributed by interfacial charge which could be different for positive and negative biases. A

classic model to explain the current transport mechanism in a bilayer capacitor involves the Maxwell-Wagner polarization [26, 27]. This phenomenon occurs when a bias is applied across a capacitor with two dielectric layers having different conductivities, leading to a discontinuity in current densities at the interface of the two layers and interfacial charge accumulation until, in steady state, the same current density is established through both layers. Other than the interfacial charge, the space charge in the bulk of dielectric also affects the electric field in the capacitor dielectric layers [26]. The different barrier heights at top and bottom interfaces, may also contribute to different conductivities.

Fig. 5.26 plots the breakdown voltage distribution for various capacitors with different Sm_2O_3 thicknesses stacked on a 3.8 nm SiO_2. The median breakdown voltages of MIM capacitors with 6.5 nm, 7.5 nm, and 8.5 nm Sm_2O_3 are equal to 6.2 V, 7.0 V, and 7.5 V, respectively, i.e. the corresponding breakdown field is about 6 MV/cm.

The compensation effect is also found in Temperature Coefficient of Capacitance (TCC), which is another important parameter for precision MIM capacitors. The cancelling-out between positive value of TCC in Sm_2O_3 and negative TCC in SiO_2 is clearly seen in Fig. 5.27. The TCC values are 65 ppm/ ℃, 50 ppm/ ℃ and 28 ppm/ ℃ for for 8.5 nm, 7.5 nm and 6.5 nm Sm_2O_3 stacked with 3.5 nm SiO_2, respectively. These values are smaller than those reported for HfO_2/SiO_2 stack [25].

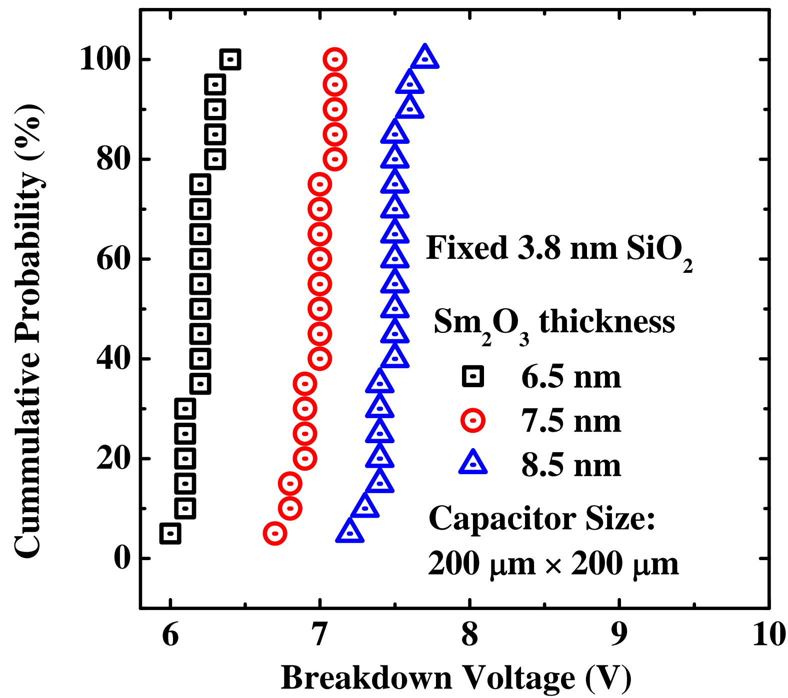

Fig. 5.26. Cumulative percentage for breakdown voltage of the MIM capacitors with various different Sm_2O_3 thicknesses formed on a 3.8 nm SiO_2 layer.

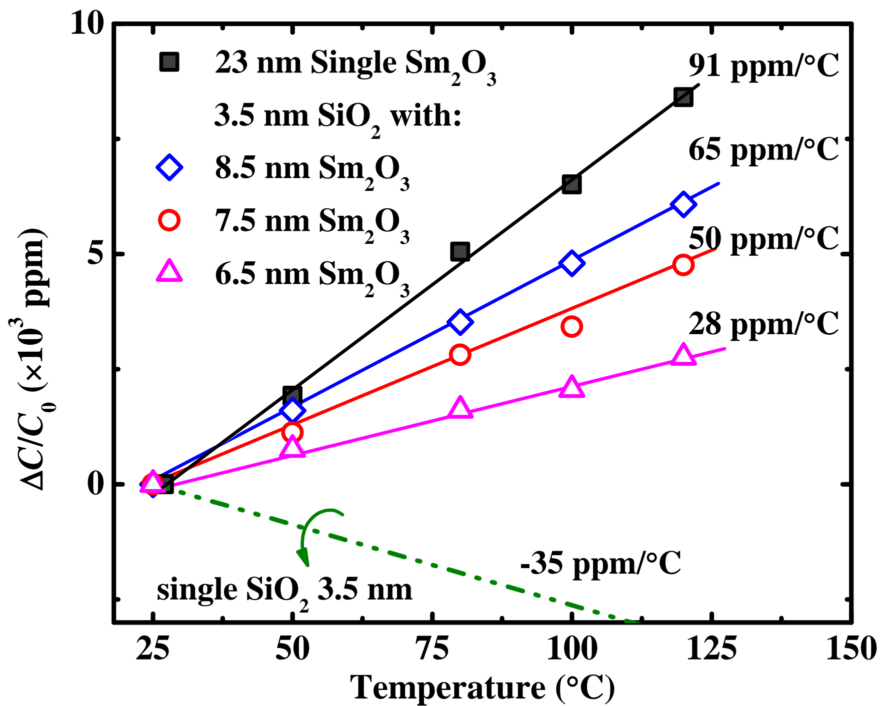

Fig. 5.27. Adding SiO_2 layer improves the TCC of Sm_2O_3 MIM capacitors by the canceling effect due to the negative TCC of SiO_2 MIM capacitors.

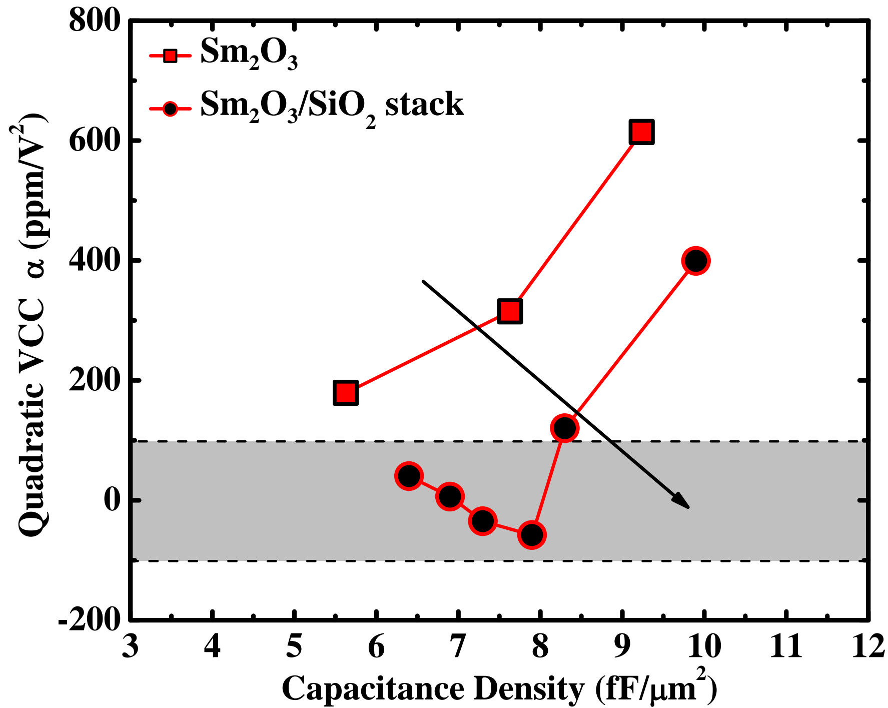

Fig. 5.28. A comparison of MIM capacitors with a single layer Sm_2O_3 dielectric and a Sm_2O_3/SiO_2 dielectric stack. The lowest values for α can be achieved at various capacitance densities by exploiting the canceling effect in the Sm_2O_3/SiO_2 dielectric stack.

Fig. 5.28 summarizes best values of α achieved at various capacitance densities in this experiment. By adding an underlying SiO_2 layer to Sm_2O_3, we shift α to smaller value, along with increased capacitance density.

5.5.3 MIM Capacitors with Er_2O_3/SiO_2 dielectric stack

MIM capacitors with Er_2O_3/SiO_2 laminated dielectric having fixed SiO_2 thickness of 3 nm and Sm_2O_3 thickness varying from 6 to 8 nm were fabricated to investigate the "cancelling effect" of SiO_2 (or Sm_2O_3) in Er_2O_3/SiO_2.

Fig. 5.29 shows the normalized *C-V* curves of the MIM capacitors with Er_2O_3/SiO_2 dielectric stacks, in comparison with MIM capacitors single layer Er_2O_3 or SiO_2. The quadratic VCC is significantly improved by the cancelling effect. With the

Er_2O_3 thickness increases from 6 nm to 8 nm, the quadratic VCC α increases from negative to positive. The smallest α is obtained with 7 nm Er_2O_3. The asymmetric *C-V* curves in Fig. 5.29 indicate a non-zero linear VCC β, and that is a direct consequence of the asymmetric device structure, which leads to different interface band alignments and trap densities at the top and the bottom electrode-dielectric interfaces of the MIM capacitor. The capacitance densities achieved are 7.95 fF/μm^2, 8,14 fF/μm^2 and 9.44 fF/μm^2 for 3 nm SiO_2 stacked with 8 nm, 7 nm and 6 nm Er_2O_3, respectively.

The effect of the measurement frequency on α is depicted in Fig. 5.30. The α decreases with a logarithmic increase in frequency. This is consistent with the behavior of MIM capacitors with stacked Sm_2O_3 /SiO_2 dielectric in Fig. 5.23.

Fig. 5.31 shows the leakage characteristics of the laminate MIM capacitors with three different thickness combinations at room temperature. The leakage current density at +3.3 V are 7.06×10^{-7} A/cm^2, 3.36×10^{-7} A/cm^2, and 1.62×10^{-7} A/cm^2, respectively, for the splits with Er_2O_3/SiO_2 thicknesses of 6 nm/3 nm, 7 nm/3 nm, and 8 nm/3 nm. The *J-V* curves are asymmetric for all the three splits. Due to the asymmetric structure, the charge trapping situations are different for positive and negative biases. This would affect the electric field distributions and consequently lead to different leakage current densities for positive and negative biases.

The cancelling-out between positive value of TCC in Er_2O_3 and negative TCC in SiO_2 is clearly seen in Fig. 5.32. The TCC values are 64 ppm/℃, 48 ppm/℃ and 35 ppm/℃ for for 8 nm, 7 nm and 6 nm Er_2O_3 stacked with 3 nm SiO_2, respectively. These values are smaller than those reported for HfO_2/SiO_2 stack [25], and the capacitance densities are higher.

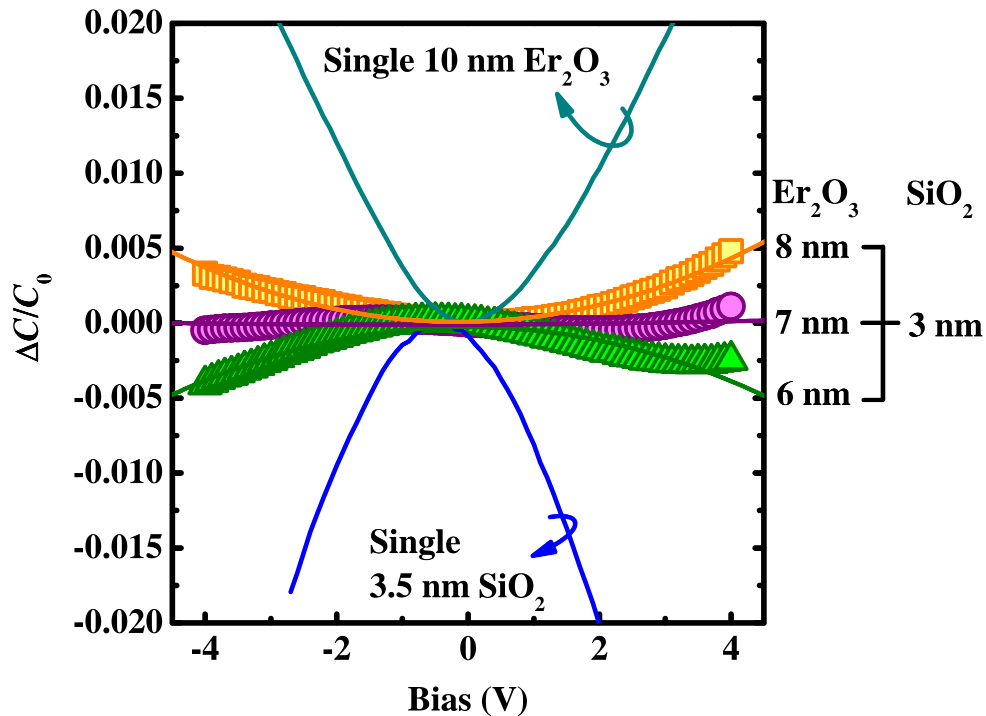

Fig. 5.29. Normalized *C-V* curves of Er_2O_3/SiO_2 stack MIM capacitors. Curvature of *C-V* curves changes from negative to positive as the Er_2O_3 thickness is increased.

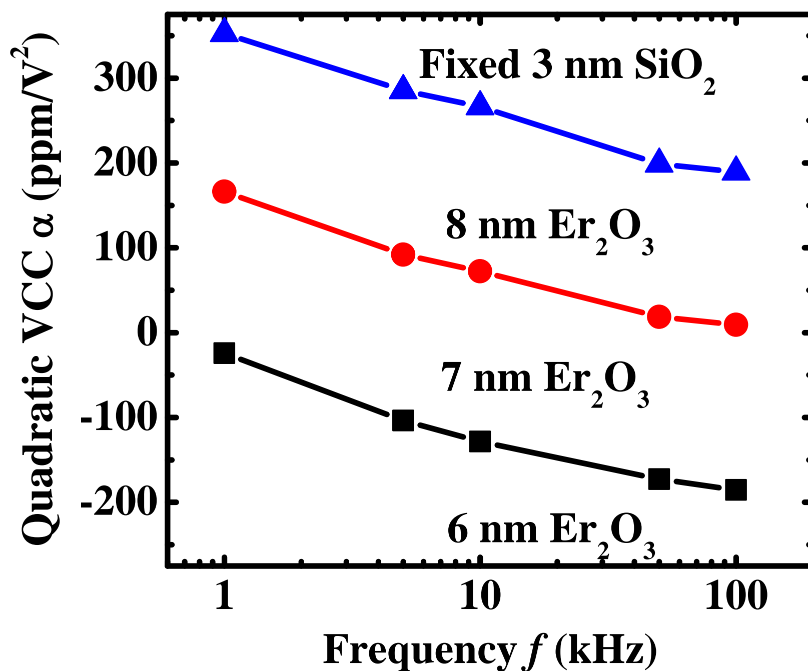

Fig. 5.30. Frequency dependence of α for MIM capacitors with different Er_2O_3/SiO_2 stacks.

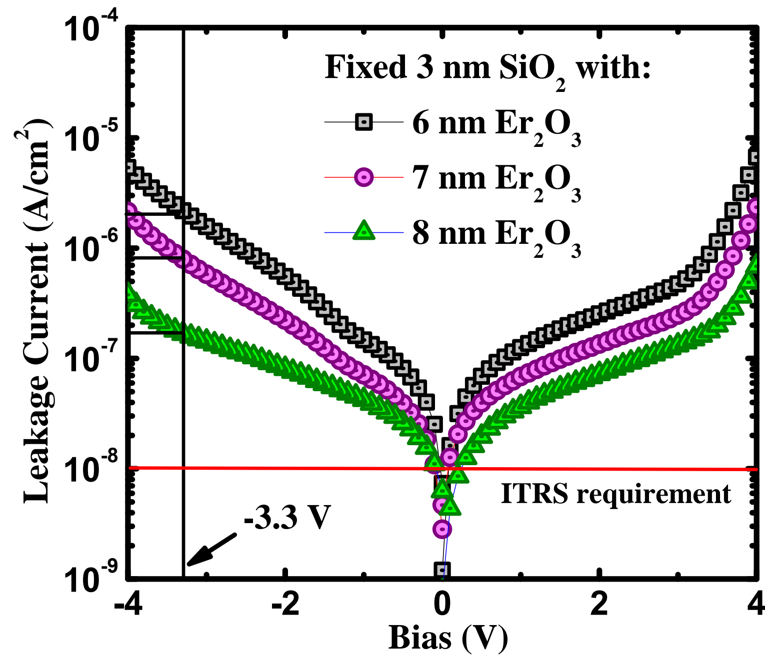

Fig. 5.31. *J-V* characteristic of Er_2O_3/SiO_2 MIM capacitors with 6, 7 and 8 nm Er_2O_3, stacked with 3 nm SiO_2.

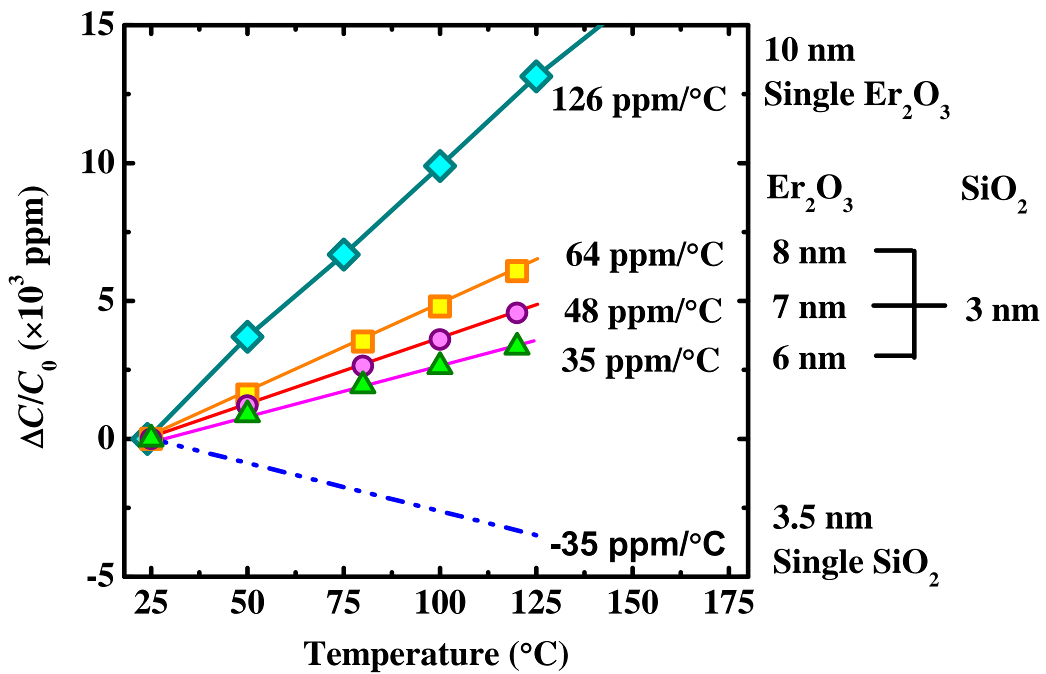

Fig. 5.32. Adding SiO_2 layer improves the TCC of Er_2O_3 MIM capacitors by the canceling effect due to the negative TCC of SiO_2 MIM capacitors.

The cumulative probability plots of breakdown voltage and breakdown field are indicated in Fig. 5.33 for single layer 10 nm Er_2O_3 and Er_2O_3/SiO_2 stacks. In case of 50% probability of failure, the breakdown field of MIM capacitors with single layer Er_2O_3 is 4.1 MV/cm, but increased to around 7 MV/cm after stacking with SiO_2.

Fig. 5.34 summarizes best values of α achieved at various capacitances for MIM capacitors with Er_2O_3/SiO_2 dielectric. By stacking Er_2O_3 with SiO_2, we shift α to smaller value, along with increased capacitance density, indicating higher capacitance density and lower α. With further optimization of the thicknesses of each oxide, even higher capacitance density is achievable at low quadratic VCC.

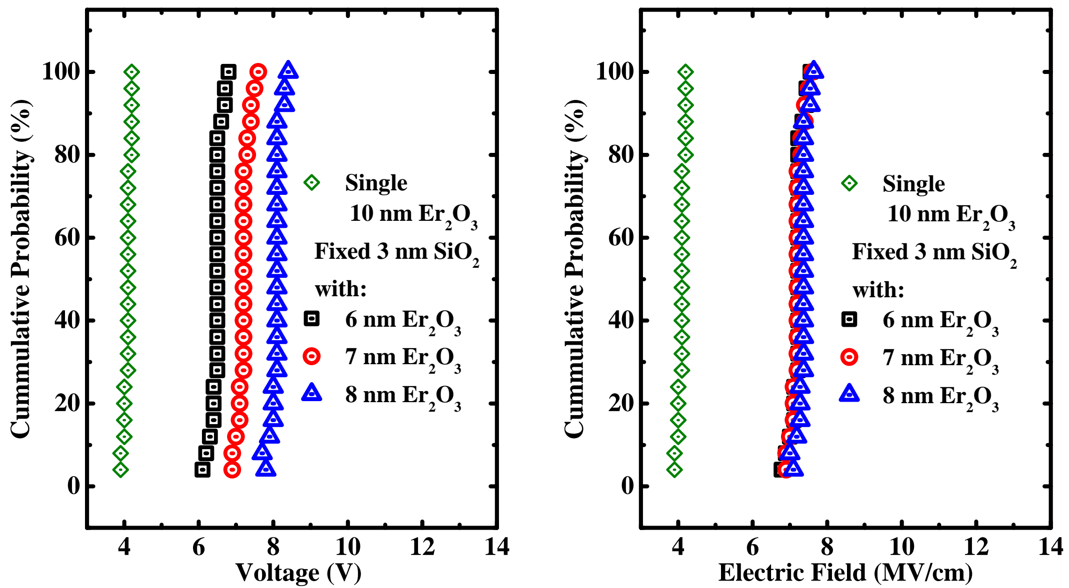

Fig. 5.33. Cumulative probability dependent on breakdown voltage and breakdown field of the MIM capacitors with single Er_2O_3 layer and Er_2O_3/SiO_2 stacks.

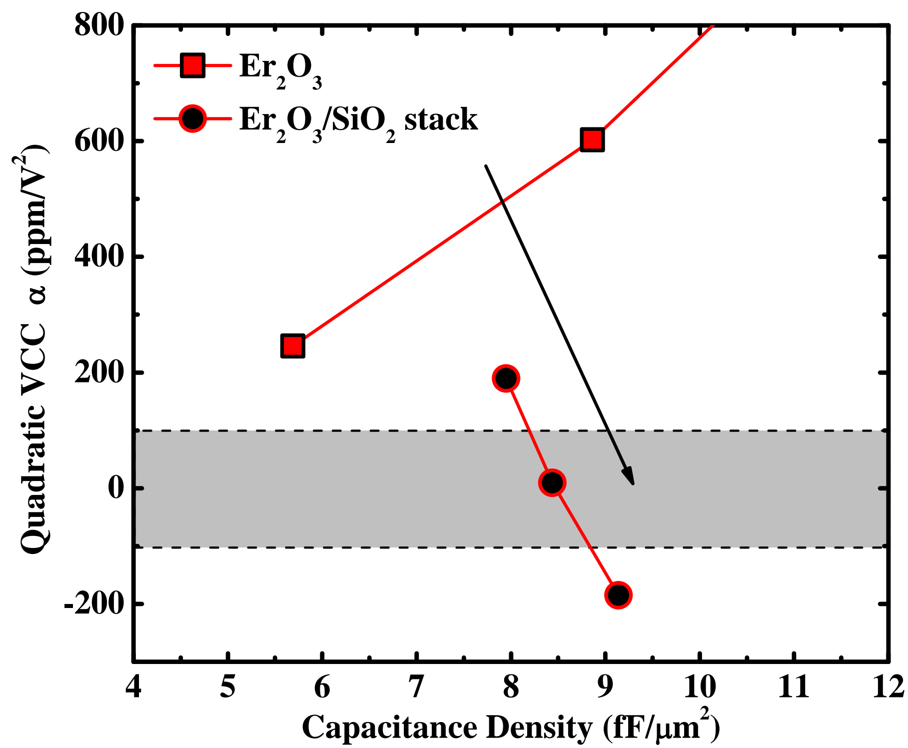

Fig. 5.34. A comparison of MIM capacitors with a single layer Er_2O_3 dielectric and a Er_2O_3/SiO_2 dielectric stack. The lowest values for α can be achieved at various capacitance densities by exploiting the canceling effect in the Er_2O_3/SiO_2 dielectric stack.

5.6 Summary

MIM capacitors using Sm_2O_3, Er_2O_3 were fabricated and characterized to utilize the cancelling effect for near-zero α and high capacitance density. MIM capacitors using Sm_2O_3 or Er_2O_3 dielectric material were found to have lower quadratic VCC as compared with other high-κ materials with the same capacitance density. Literature data and our experimental data on high-κ MIM capacitors are summarized in Table 5.2. In comparison with data in the literature, MIM capacitors with PVD Sm_2O_3 and Er_2O_3 dielectric show high capacitance density, low leakage current, low α, acceptable β and small TCC, suggesting its potential use in future RF and analog/mixed signal IC applications. Comparing Sm_2O_3 and Er_2O_3, Er_2O_3 has the advantage of lower leakage current, but the quadratic VCC and TCC values are slightly higher.

MIM capacitors with stacked dielectrics, namely Sm_2O_3/SiO_2 and Er_2O_3/SiO_2 were fabricated to further reduce the quadratic VCC by utilizing the cancelling effect.

Table 5.2. Comparison of DC performance of reported binary high-κ MIM capacitors

	Dielectrics	Cap. Density (fF/μm^2)	J_{leak} @ 1 V (A/cm^2)	J_{leak} @ 3.3 V (A/cm^2)	α @ 100kHz (ppm/V^2)	β @ 100kHz (ppm/V)	TCC
Reported High-κ MIM	Ta_2O_5 [8]	4	N/A	6×10^{-7}	-9.9	N/A	106
	Al_2O_3 [29]	5.2	4.3×10^{-8}	N/A	2051	1888	109~208
	ALD HfO_2 [4]	8	$\sim 4 \times 10^{-8}$	$\sim 6 \times 10^{-7}$	~1800	~4000	N/A
	PVD HfO_2 [12]	14	$\sim 3 \times 10^{-9}$	$\sim 8 \times 10^{-6}$	4631	-4843	135
	La_2O_3 [28]	9.2	$< 10^{-5}$	N/A	~3000	~3000	347
Our results	Er_2O_3	5.8	3.5×10^{-9}	6.4×10^{-9}	240	-430	178
	Er_2O_3	8.9	5.5×10^{-9}	1.4×10^{-8}	580	-620	170
	Er_2O_3	18.4	1.3×10^{-8}	4.9×10^{-7}	2000	-360	126
Our results	Sm_2O_3	5.6	8.1×10^{-8}	2.3×10^{-7}	179	411	99
	Sm_2O_3	7.6	1.1×10^{-7}	6.0×10^{-7}	315	589	91
	Sm_2O_3	9.2	1.7×10^{-7}	3.2×10^{-6}	614	1170	82

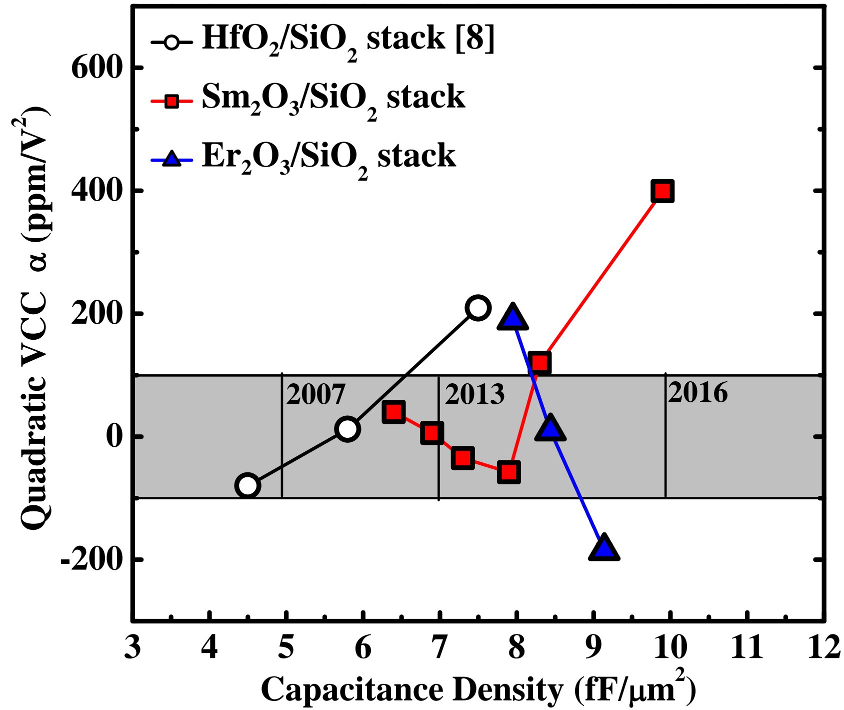

Fig. 5.35. A comparison of Sm_2O_3/SiO_2 and Er_2O_3/SiO_2 stacks with HfO_2/SiO_2 stack. Sm_2O_3/SiO_2 and Er_2O_3/SiO_2 stacks are better to meet the capacitance density requirements.

Fig. 5.35 summarizes best values of α achieved at various capacitance densities utilizing the cancelling effect when stacking with SiO_2. By replacing HfO_2 with Sm_2O_3 or Er_2O_3, we are able to achieve increased capacitance density while maintaining a near zero α value. With further optimization of the thicknesses of each oxide, even higher capacitance density is achievable at low quadratic VCC.

Capacitors with stacked dielectrics offers high capacitance density (up to 8.5 $fF/\mu m^2$) with quadratic VCC lower than 100 ppm/V^2, which meets the ITRS requirement in year 2013 [1]. The leakage current can be further reduced by using electrodes with higher work functions. These results support that high-κ/SiO_2 MIM capacitor can be a long-term solution to RF, analog/mixed-signal capacitor technology.

References:

[1] International Technology Roadmap for Semiconductors 2008, www.itrs.net.

[2] T. Remmel, R. Ramprasad, and J. Walls, "Leakage behavior and reliability assessment of tantalum oxide dielectric MIM capacitors," *Proceedings of the Reliability Physics Symposium*, pp. 277-281, 2003.

[3] H. Hu, C. Zhu, Y. Lu, M. Li, B. Cho, and W. Choi, "A high performance MIM capacitor using HfO_2 dielectrics," *IEEE Electron Device Letters,* vol. 23, pp. 514-516, 2002.

[4] X. Yu, C. Zhu, H. Hu, A. Chin, M. Li, B. Cho, D. Kwong, P. Foo, and M. Yu, "A high-density MIM capacitor (13 $fF/\mu m^2$) using ALD HfO_2 dielectrics," *IEEE Electron Device Letters,* vol. 24, pp. 63-65, 2003.

[5] C. H. Cheng, S. H. Lin, K. Y. Jhou, W. J. Chen, C. P. Chou, F. S. Yeh, J. Hu, M. Hwang, T. Arikado, S. P. McAlister, and A. Chin, "High Density and Low Leakage Current in TiO_2 MIM Capacitors Processed at 300 ℃," *Electron Device Letters, IEEE,* vol. 29, pp. 845-847, 2008.

[6] Y. L. Tu, H. L. Lin, L. L. Chao, D. Wu, C. S. Tsai, C. Wang, C. F. Huang, C. H. Lin, and J. Sun, "Characterization and Comparison of High-k Metal-Insulator-Metal (MiM) Capacitors in 0.13 m Cu BEOL for Mixed-Mode and RF Applications," *Symposium on VLSI Technology Tech. Dig.,* pp. 79-80, 2003.

[7] C. Durand, C. Vallee, V. Loup, O. Salicio, C. Dubourdieu, S. Blonkowski, M. Bonvalot, P. Holliger, and O. Joubert, "Metal-insulator-metal capacitors using Y_2O_3 dielectric grown by pulsed-injection plasma enhanced metalorganic chemical vapor deposition," *Journal of Vacuum Science and Technology A: Vacuum, Surfaces and Films,* vol. 22, pp. 655-660, 2004.

[8] Y.-K. Jeong, S.-J. Won, D.-J. Kwon, M.-W. Song, W.-H. Kim, M.-H. Park, J.-H. Jeong, H.-S. Oh, H.-K. Kang, and K.-P. Suh, "High quality high-k MIM

capacitor by Ta_2O_5/HfO_2/Ta_2O_5 multi-layered dielectric and NH_3 plasma interface treatments for mixed-signal/RF applications," *Symposium on VLSI Technology Tech. Dig.*, pp. 222-223, 2004.

[9] S.-J. Ding, H. Hu, C. Zhu, S. J. Kim, X. Yu, M.-F. Li, B. J. Cho, D. S. H. Chan, M. B. Yu, S. C. Rustagi, A. Chin, and D.-L. Kwong, "RF, DC, and reliability characteristics of ALD HfO_2-Al_2O_3 laminate MIM capacitors for Si RF IC applications," *IEEE Transactions on Electron Devices,* vol. 51, pp. 886-894, 2004.

[10] N. Inoue, H. Ohtake, I. Kume, N. Furutake, T. Onodera, S. Saito, A. Tanabe, M. Tagami, M. Tada, and Y. Hayashi, "High Performance High-κ MIM Capacitor with Plug-in Plate (PiP) for Power Delivery Line Hige-Speed MPUs," *Interconnect Technology Conference Proceedings*, pp. 63-65, 2006.

[11] C. Wenger, R. Sorge, T. Schroeder, A. Mane, G. Lippert, G. Lupina, J. Dabrowski, P. Zaumseil, and H. Muessig, "MIM capacitors using amorphous high-k $PrTi_xO_y$ dielectrics," *Microelectronic Engineering,* vol. 80, pp. 313-316, 2005.

[12] S. Kim, B. Cho, M. Li, C. Zhu, A. Chin, and D. Kwong, "HfO_2 and lanthanide-doped HfO_2 MIM capacitors for RF/mixed IC applications," *Symposium on VLSI Technology Tech. Dig.*, pp. 77-78, 2003.

[13] J. Paivasaari, M. Putkonen, and L. Niinisto, "A comparative study on lanthanide oxide thin films grown by atomic layer deposition," *Thin Solid Films,* vol. 472, pp. 275-281, 2005.

[14] S. Jeon, K. Im, H. Yang, H. Lee, H. Sim, S. Choi, T. Jang, and H. Hwang, "Excellent electrical characteristics of lanthanide (Pr, Nd, Sm, Gd, and Dy) oxide and lanthanide-doped oxide for MOS gate dielectric applications," *International Electron Devices Meeting Tech. Dig.*, pp. 471-474, 2001.

[15] H. Yang, H. Wang, H. M. Luo, D. M. Feldmann, P. C. Dowden, R. F. DePaula, and Q. X. Jia, "Structural and dielectric properties of epitaxial Sm2O3 thin films," *Applied Physics Letters,* vol. 92, pp. 062905-1, 2008.

[16] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-κ gate dielectrics: Current status and materials properties considerations," *Journal of Applied Physics,* vol. 89, pp. 5243-5275, 2001.

[17] A. V. Prokofiev, A. I. Shelykh, and B. T. Melekh, "Periodicity in the band gap variation of Ln_2X_3 (X = O, S, Se) in the lanthanide series," *Journal of Alloys and Compounds,* vol. 242, pp. 41-44, 1996.

[18] H. Yu, M. Li, B. Cho, C. Yeo, M. Joo, D. Kwong, J. Pan, C. Ang, J. Zheng, and S. Ramanathan, "Energy gap and band alignment for $(HfO_2)_x(Al_2O_3)_{1-x}$ on (100) Si," *Applied Physics Letters,* vol. 81, pp. 376-378, 2002.

[19] S. Miyazaki, "Photoemission study of energy-band alignments and gap-state density distributions for high-k gate dielectrics," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 19, pp. 2212, 2001.

[20] S. Toyoda, J. Okabayashi, H. Kumigashira, M. Oshima, K. Ono, M. Niwa, K. Usuda, and N. Hirashita, "Chemistry and band offsets of HfO_2 thin films on Si revealed by photoelectron spectroscopy and x-ray absorption spectroscopy," *Journal of electron spectroscopy and related phenomena,* vol. 137, pp. 141-144, 2004.

[21] C. Zhu, H. Hu, X. Yu, S. Kim, A. Chin, M. Li, B. Cho, and D. Kwong, "Voltage and temperature dependence of capacitance of high-κ HfO_2/MIM capacitors: a unified understanding and prediction," *International Electron Devices Meeting Tech. Dig.*, pp. 36-5, 2003.

[22] R. B. van Dover, R. M. Fleming, L. F. Schneemeyer, G. B. Alers, and D. J. Werder, "Advanced dielectrics for gate oxide, DRAM and rf capacitors," *International Electron Devices Meeting Tech. Dig.*, pp. 823-828, 1998.

[23] F. E. Kamel, P. Gonon, L. Ortega, F. Jomni, and B. Yangui, "Space charge limited transient currents and oxygen vacancy mobility in amorphous $BaTiO_3$ thin films," *Journal of Applied Physics,* vol. 99, pp. 094107, 2006.

[24] P. Gonon and C. Vallee, "Modeling of nonlinearities in the capacitance-voltage characteristics of high-k metal-insulator-metal capacitors," *Applied Physics Letters,* vol. 90, pp. 142906, 2007.

[25] S. Kim, B. Cho, M. Li, S. Ding, M. Yu, C. Zhu, A. Chin, and D. Kwong, "Engineering of voltage nonlinearity in high-κ MIM capacitor for analog/mixed-signal ICs," pp. 218-219, 2004.

[26] A. Von Hippel and S. Morgan, "Dielectrics and Waves," *Journal of The Electrochemical Society,* vol. 102, 1955.

[27] J. Jameson, P. Griffin, J. Plummer, and Y. Nishi, "Charge Trapping in High-κ Gate Stacks Due to the Bilayer Structure Itself," *IEEE Transactions on Electron Devices,* vol. 53, pp. 1858-1867, 2006.

[28] M. Y. Yang, D. S. Yu, and A. Chin, "High-Density RF MIM Capacitors Using High-k La_2O_3 Dielectrics," *Journal of The Electrochemical Society,* vol. 151, pp. F162-F165, 2004.

[29] S. Chen, C. Lai, A. Chin, J. Hsieh, and J. Liu, "High-density MIM capacitors using Al_2O_3 and $AlTiO_x$ dielectrics," *IEEE Electron Device Letters,* vol. 23, pp. 185-188, 2002.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

Lanthanoid elements are low work function metals and they form low work function silicides when anneal with silicon. Moreover, their oxides are thermally stable, featuring high dielectric constant (from 10 to 30), large band gap (from 2.4 eV to 5.5 eV). This thesis work has explored some of the possible applications of lanthanoid based materials in several areas of CMOS processing technology. The main contributions of this thesis are summarized below.

6.1.1 Schottky Barrier Source/Drain Field-Effect Transistor

In this chapter, we exploit SSDT using lanthanoid metal silicide to replace the traditional highly-doped source/drain. We developed a low temperature MOSFET process featuring a “hole spacer”, Schottky barrier source/drain, high-κ dielectric and metal gate electrode. Several lanthanoid elements, namely Dy, Er, Tb and Yb, were investigated to form silicide S/D for N-SSDT. The $YbSi_{2-x}$ has been found to be a very promising candidate for N-SSDT as it provides a high drive current with a very low leakage current. However, there are still major challenges integrating the

lanthanoid silicide S/D with conventional CMOS processing technology because of their chemically reactive nature.

6.1.2 Yb Doped Ni FUSI for the N-MOSFETs Gate Electrode Application

A novel Ni-FUSI gate tuning method using Yb-incorporated Ni FUSI was demonstrated for the first time. Electrical and material analysis was conducted to ascertain the attractiveness of this Φ_m tuning technique. By incorporating Yb, a FUSI gate Φ_m lowering of about 0.3 to 0.5 eV was achieved without compromising the gate integrity and capacitance density. The modulation of Ni-FUSI gate Φ_m was attributed to the presence of interfacial Yb-O dipoles. Additional insights were given for the application of the novel technique to attain band-edge Ni-FUSI gate Φ_m tunability in a gate-first process flow. It should be noted that the FUSI gate Φ_m lowering is not as effective on HfSiON as it is on SiON.

6.1.3 NMOS Compatible Work Function of TaN Metal Gate with Erbium Oxide Doped Hafnium Oxide Gate Dielectric

We exploit a novel method to engineer the Φ_m of TaN metal gate on HfO_2 dielectric to silicon conduction band edge. In this method, HfO_2 dielectric was doped with Er_2O_3, which enabled Si conduction band-edge modulation (4.1 eV) of midgap TaN Φ_m. Band edge Φ_m was retained even after high temperature anneal. A small EOT of 1.15 nm was achieved by HfErO (30% Er). The modulation of TaN gate Φ_m was attributed to the presence of interfacial Er-O dipoles at the high-κ/SiO_x-IL interface. Similar results are obtained by doping HfO_2 doped by other lanthanoid metal oxides, namely Tb_2O_3, Dy_2O_3, and Yb_2O_3. This result is noteworthy for attaining band-edge TaN gate Φ_m on high-κ dielectrics stacks.

6.1.4 Lanthanoid Oxides for Precision RF/analog MIM Capacitors

Lanthanoid oxide based metal-insulator-metal capacitors for precision analog circuit were demonstrated. From extensive material screening, Sm_2O_3 and Er_2O_3 are proved to be the most promising candidates among the 6 lanthanoid oxides investigated. In comparison with other high-κ materials reported in the literature, MIM capacitors with PVD Sm_2O_3 and Er_2O_3 dielectric show high capacitance density, low leakage current, low α, acceptable β and small TCC, suggesting its potential use in future RF and analog/mixed signal IC applications. MIM capacitors with laminated Sm_2O_3/SiO_2 and Er_2O_3/SiO_2 dielectric were fabricated and characterized to utilize the cancelling effect for near-zero α and high capacitance density. Capacitors with stacked dielectrics offers high capacitance density (up to 8.5 fF/μm^2) with quadratic VCC lower than 100 ppm/V^2. These results meet the ITRS requirement in year 2013 and support that high-κ/SiO_2 MIM capacitor can be a long-term solution to RF, analog/mixed-signal capacitor technology.

6.2 Suggestions for Future Work

The work presented in this thesis has been very exploratory and more detailed investigation and rigorous characterization will be necessary to evaluate the potential in applying these methods or concepts in coming technology nodes. Suggestions for future work will be directly or indirectly related to the work described earlier in this thesis.

With the emergence of ultra-thin body devices (e.g. FINFET, nanowire transistor), SSDT will be of greater importance. For ultra-thin body device, the gate has better control over the channel and leakage current paths are minimized, but

dopant concentration becomes harder to control. Self-aligned metal silicide source/drain would be a potential solution.

In source/drain engineering, T-FET is another attractive topic. The research is still at the earlystage. Due to its low drive current, it is more likely to be used in low power technology in the future.

In Chapter 3, NMOS Φ_m tunability of Ni-FUSI gate was limited due to the small amount of Yb atoms segregated at the interface. This problem could be improved by reducing the polysilicon gate height to facilitate the diffusion of Yb, or by implanting Yb atoms directly into the polysilicon. Moreover, the proposed dual gate integration scheme could be verified by using two different kinds of dopants in Ni FUSI for NMOS and PMOS metal gate Φ_m control. In Chapter 4, although all the four kinds of lanthanoid oxides have been experimentally proved to be able to modulate the TaN Φ_m towards the silicon conduction band edge, the effectiveness of each oxide dopant has not been quantitatively evaluated. It will be helpful to precisely control the dopant concentration for a fair comparison. A direct measurement of the momentum of the interface dipoles may be difficult but very helpful for understanding the mechanism.

For high precision capacitors, the specifications on capacitance density and voltage linearity have been met. However, they would be useful for the industry only when there are significant improvements in the leakage current issue. The large leakage can be reduced in several ways. One is to replace the electrode with inert materials with higher work function, e.g., Pt, Pd and Mo. However, inert metals usually have compatibility problems, especially during the etching process. There is still a need to improve the dielectric integrity of lanthanoid oxides without increasing

the thermal budget. As mentioned in Chapter 5, the Sm_2O_3 and Er_2O_3 formed are both polycrystalline. The leakage through grain boundaries may have contributed a substantial amount of leakage current. Adding foreign materials such as Al or Ta to lanthanoid oxides would be one of the process options to obtain amorphous film and reduce the; however, this may also worsen the voltage linearity of lanthanoid oxides.

Recently, resistive random-access memory (RRAM) has drawn much attention [3-5]. RRAM is a new non-volatile memory type, which bears some similarities to the phase change memory (PCRAM). The basic idea is that a dielectric, which is normally insulating, can be made to conduct through either a filamentary conduction path or an interface-type conducting path formed after application of a sufficiently high voltage. Recent studies have indicated that the electrochemical migration of oxygen vacancies in the vicinity of the interface could be one of the mechanisms that drive resistive switching [5]. Oxidative treatment of memory cells has been shown to change the resistive switching properties [5]. In Chapter 5, we have successfully engineered the voltage linearity of Er_2O_3 by manipulating the oxygen vacancies in the thin film. The same idea and device structure could be easily applied on RRAM studies by redesigning the oxide thickness and electrode materials.

References:

[1] M. Guillorn, J. Chang, A. Bryant, N. Fuller, O. Dokumaci, X. Wang, J. Newbury, K. Babich, J. Ott, and B. Haran, "FinFET performance advantage at 22nm: An AC perspective," *Symposium on VLSI Technology Tech. Dig.*, pp. 12-13, 2008.

[2] B. Haran, A. Kumar, L. Adam, J. Chang, V. Basker, S. Kanakasabapathy, D. Horak, S. Fan, J. Chen, and J. Faltermeier, "22 nm technology compatible fully functional 0.1 μm^2 6T-SRAM cell," *International Electron Devices Meeting Tech. Dig.*, pp. 1-4, 2008.

[3] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nature Materials,* vol. 6, pp. 833-840, 2007.

[4] C.-Y. Lin, C.-Y. Liu, C.-C. Lin, and T. Tseng, "Current status of resistive nonvolatile memories," *Journal of Electroceramics,* vol. 21, pp. 61-66, 2008.

[5] A. Sawa, "Resistive switching in transition metal oxides," *Materials Today,* vol. 11, pp. 28-36, 2008.

Appendix

A. LIST OF PUBLICATIONS

Journal Publications

[1]. S. Zhu, H. Yu, **J. Chen**, S. Whang, J. Chen, C. Shen, C. Zhu, S. Lee, M. Li, and D. Chan, "Low temperature MOSFET technology with Schottky barrier source/drain, high-κ gate dielectric and metal gate electrode," *Solid State Electronics,* vol. 48, pp. 1987-1992, 2004.

[2]. S. Zhu, **J. Chen**, M. Li, S. Lee, J. Singh, C. Zhu, A. Du, C. Tung, A. Chin, and D. Kwong, "N-type Schottky barrier source/drain MOSFET using ytterbium silicide," *IEEE Electron Device Letters,* vol. 25, pp. 565-567, 2004.

[3]. **J. Chen**, H. Yu, M. Li, D. Kwong, M. van Dal, J. Kittl, A. Lauwers, P. Absil, M. Jurczak, and S. Biesemans, "Yb-doped Ni FUSI for the n-MOSFETs gate electrode application," *IEEE Electron Device Letters,* vol. 27, pp. 160-162, 2006.

[4]. **J. Chen**, X. Wang, M. Li, S. Lee, M. Yu, C. Shen, and Y. Yeo, "NMOS compatible work function of TaN metal gate with erbium-oxide-Doped hafnium oxide gate dielectric," *IEEE Electron Device Letters,* vol. 28, pp. 862-864, 2007.

[5]. X. Wang, M. Li, H. Yu, J. Yang, **J. Chen**, C. Zhu, A. Du, W. Loh, S. Biesemans, and A. Chin, "Widely tunable work function TaN/Ru stacking layer on HfLaO gate dielectric," *IEEE Electron Device Letters,* vol. 29, pp. 50-53, 2008.

[6]. Jian-Jun Yang, **Jing-De Chen**, Rick Wise, Philipp Steinmann, Ming-Bin Yu, Dim-Lee Kwong, Ming-Fu Li, Yee-Chia Yeo, Chunxiang Zhu, "Effective Modulation of Quadratic Voltage Coefficient of Capacitance in MIM Capacitors Using Sm_2O_3/SiO_2 Dielectric Stack," *IEEE Electron Device Letters,* vol. 30, pp. 460-462, 2009.

[7]. **Jing-De Chen**, Jian-Jun Yang, Rick Wise, Philipp Steinmann, Ming-Bin Yu, Chunxiang Zhu , Yee-Chia Yeo. "Physical and Electrical Characterization of

Metal-Insulator-Metal Capacitors with Sm_2O_3 and Sm_2O_3/SiO_2 Laminate Dielectrics for Analog Circuit Applications," *IEEE Transaction on Electron Devices*, vol. 56, pp. 2683-2691, 2009.

[8]. Jian-Jun Yang, **Jing-De Chen**, Rick Wise, Philipp Steinmann, Yee-Chia Yeo, Chunxiang Zhu, "Performance Improvement of Sm_2O_3 MIM Capacitors by Using Plasma Treatment after Dielectric Formation,", *IEEE Electron Device Letters,* vol. 30, pp. 1033-1035, 2009.

Conference Publications

[9]. H. Yu, J. Kang, **J. Chen**, C. Ren, Y. Hou, S. Whang, M. Li, D. Chan, K. Bera, and C. Tung, "Thermally Robust High Quality HfN/HfO_2 Gate Stack for Advanced CMOS Devices," *International Electron Devices Meeting Tech. Dig.*, pp. 99-102, 2003.

[10]. H. Yu, **J. Chen**, M. Li, S. Lee, D. Kwong, M. van Dal, J. Kittl, A. Lauwers, E. Augendre, and S. Kubicek, "Modulation of the Ni FUSI workfunction by Yb doping: from midgap to n-type band-edge," *International Electron Devices Meeting Tech. Dig.*, pp. 630-633, 2005.

[11]. X. P. Wang, J. J. Yang, H. Y. Yu, M.-F. Li, **J. D. Chen**, R. L. Xie, C. X. Zhu, A. Y. Du, P. C. Lim, Andy Lim, Y. Y. Mi, Doreen M. Y. Lai, W. Y. Loh, S. Biesemans, G. Q. Lo, and D.-L. Kwong, "Practical Solutions to Enhance EWF Tunability of Ni FUSI Gates on HfO_2," *International Conference on Solid State Devices and Materials*, pp. 854-855, 2007.

[12]. X. P. Wang, M.-F. Li, H. Y. Yu, J. J. Yang, C. X. Zhu, W. S. Hwang, W. Y. Loh, A. Y. Du, **J. D. Chen**, Albert Chin, S. Biesemans, G. Q. Lo, and D.-L. Kwong, "Highly Manufacturable CMOSFETs with Single High-κ (HfLaO) and Dual Metal Gate Integration Process," in *International Conference on Solid State Devices and Materials Tech. Dig.*, 2007.

[13]. **Jingde Chen**, Andy Eu-Jin Lim, Lina Wei-Wei Fang, Yee-Chia Yeo, "Gate Work Function Engineering Using $Hf_{1-x}Er_xO_y$ and Band Alignment Studies

Using X-Ray Photoelectron Spectroscopy," *Materials Research Society Spring Meeting*, 2008.

[14]. **(Invited)** M.-F. Li, X. P. Wang, C. Shen, J. -J. Yang, **J.-D. Chen**, C.-X. Zhu and D.-M. Huang, "Some issues in advanced CMOS gate stack performance and reliability", *5th International Symposium on advanced gate stack technology*, 2008.

[15]. **Jing-De Chen**, Jian-Jun Yang, Rick Wise, Philipp Steinmann, Chunxiang Zhu and Yee.-Chia Yeo, "Lanthanoid metal oxide MIM capacitors for precision analog circuits: Material screening, process development, and characterization," *International Conference on Solid State Devices and Materials*, pp. 50-51, 2009.

[16]. Jian-Jun Yang, **Jing-De Chen**, Rick Wise, Philipp Steinmann, Ming-Bin Yu, Yee-Chia Yeo, Chunxiang Zhu, "Voltage Coefficient of Capacitance Modulation for Sm_2O_3/SiO_2 MIM Capacitors," *International Conference on Solid State Devices and Materials*, pp. 316-317, 2009.