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INVESTIGATION OF HIGH-Κ DIELECTRIC FILMS INCORPORATED WITH LANTHANUM AND THEIR APPLICATION IN FLASH MEMORY DEVICES

HE WEI

NATIONAL UNIVERSITY OF SINGAPORE

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INVESTIGATION OF HIGH-Κ DIELECTRIC FILMS INCORPORATED WITH LANTHANUM AND THEIR APPLICATION IN FLASH MEMORY DEVICES

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Abstract

The SONOS-type of flash memory is one of the promising candidates to replace the conventional floating-gate type flash memory to enable continued memory device down-sizing. For a typical SONOS-type flash memory, there is a tradeoff between data retention and operation speeds. In order to break this tradeoff, Al_2O_3 as a blocking oxide has been proposed and exhibits promising results. However, the permittivity of Al_2O_3 is not high (only around 9) and even higher permittivity dielectrics, such as $LaAlO_x$ and $HfLaO_x$, were investigated here to further improve the memory performance.

The lanthanum-incorporated dielectrics ($LaAlO_x$ and $HfLaO_x$) were deposited using the atomic layer deposition (ALD) method at 300ºC. The enhancement of deposition rate of La_2O_3 was observed when co-introducing the Hf or Al precursor into the process chamber to form $HfLaO_x$ or $LaAlO_x$, respectively. Overall, the ALD processes of both $HfLaO_x$ and $LaAlO_x$ showed good self-limiting behavior, good film uniformity, low carbon impurity and a strictly linear relationship between the film thickness and deposition cycles, indicating good ALD characteristics.

Both ALD $LaAlO_x$ and $HfLaO_x$ layers exhibited wide energy band gap and relatively large conduction band offset. $LaAlO_x$ films with a higher La percentage showed higher permittivity. The permittivity of amorphous $LaAlO_x$ films with 46% La was around 18 and these films could stand annealing temperature up to 850ºC. In

contrast, at low temperatures (~ 500ºC), $HfLaO_x$ with 8 at.% La would crystallize to a cubic-like phase and this phase has a much greater permittivity (~ 38) than that of amorphous or monoclinic phases (~ 20). This increase in permittivity resulted in a significant improvement in the overall leakage current. Moreover, the permittivities and leakage currents are dependant on annealing temperatures.

Both $LaAlO_x$ and $HfLaO_x$ were used as blocking oxides in nitride-based SONOS-type flash memories. In comparison with memory cells using Al_2O_3 blocking oxide, those with $LaAlO_x$ or $HfLaO_x$ blocking oxide exhibited improved memory characteristics, such as faster operation speeds, wider saturation window, and better time-to-breakdown (t_{BD}) reliability. Furthermore, memory cells with $LaAlO_x$ blocking oxide showed improved retention performance below 120ºC, which is similar to normal memory working temperature. On the other hand, memory cells using $HfLaO_x$ blocking oxide showed degraded retention performance due to their relatively low conduction band offset. By compiling above data retention results, it is found that the conduction band offset of blocking oxide over Si is required to be greater than 2.4 eV. However, few dielectrics can satisfy such requirement. In addition, by using the modified Yang's model, the trapping energy depth in nitride films was calculated to be ~ 0.7 eV below the nitride conduction band edge.

Overall, $LaAlO_x$ is a promising candidate as a blocking oxide to further boost the memory performances. And $HfLaO_x$, due to its improved permittivity under cubic phase, may be useful in other applications, e.g. in DRAMs.

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List of Symbols and Abbreviations

E_c	Conduction band edge
E_g	Energy band gap
E_{TA}	Trapping Energy
E_v	Valence band edge
J_g	Current density
k	Dielectric constant
t_{eq}	Equivalent oxide thickness
T_{ox}	Tunnel oxide
V_{fb}	Flat-band voltage
V_g	Gate voltage
V_{th}	Threshold voltage
ε_0	Permittivity in vacuum
ALD	Atomic layer deposition
CVD	Chemical vapor deposition
C-V	Capacitance-voltage
EOT	Equivalent oxide thickness
FGA	Forming gas anneal
FN tunneling	Fowler-Nordheim tunneling
HRTEM	High-resolution transmission electron microscopic
I-V	Current-voltage
MBE	Molecular beam epitaxy
MIM	Metal insulator metal
MOCVD	Metal-organic chemical vapor deposition
MOS	Metal oxide semiconductor
ONO	Oxide-nitride-oxide

PLD	Pulse laser deposition
PVD	Physical vapor deposition
RTP	Rapid thermal anneal
SONOS	Poly silicon-oxide-nitride-oxide-silicon memory
TMA	Trimethylaluminum
XPS	X-ray photoelectron spectroscopic
XRD	X-ray diffraction

Chapter 1 Introduction of Flash Memory and High-K Dielectrics

1.1 Overview

During the last decade, memory products have become a main growth engine for the semiconductor businesses owing to the huge demands from computers, mobile phones, digital cameras, and MP3 music players, etc [1]. The price of a bit of memory is ever-decreasing and the performance is ever-increasing. All of these successful achievements rely on the “scaling technology” which is primarily based on the shrinking of physical dimension of the MOSFET (metal-oxide-semiconductor field effect transistor). One of the great advantages of this “scaling technology” is that the device structures and memory structures undergo few changes during the scaling. The little changes in structures facilitate the integration of more transistors or memory cells in one chip, thus effectively enabling lower power consumption and lower manufacturing cost per die. This “scaling technology” follows the famous Moore’s Law, which predicted a constant growth rate of chip complexity (double the density every 3 years) in 1965 [2]. Moore’s prediction has been realized over the past 40 years in both memory and microprocessor products, as shown in Fig 1.1. The memory density has increased at an amazing speed and the number of memory cells per die doubled nearly every year, which is even greater than the prediction of Moore’s Law.

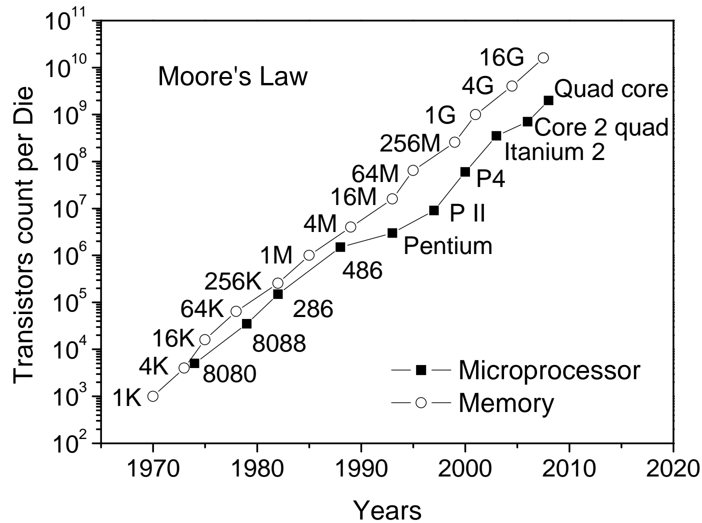

Fig. 1.1 The trend of ever-increasing number of transistors per die in microprocessor and memory products during the past 40 years [1]. This graph shows the device scaling basically follows Moore's Law.

Generally, memory products are divided into two branches, volatile memory and non-volatile memory. The volatile memory, such as SRAM (static random access memory) or DRAM (dynamic random access memory), loses the data contents when the power supply is turned off [3]. On the contrary, the non-volatile memory, such as EPROM (electrically programmable ROM), EEPROM (electrically erasable programmable ROM), or flash can keep the data content for a long duration even without the power supply [3]. Among the non-volatile memories, flash memory, a special EEPROM where the entire chip or an array is erased simultaneously, occupies the majority of market share due to its attractive compromise between cost and performance. In other words, the flash memory has the capability of electrical program and electrical erasure while using the smallest cell size [4].

At present, flash memory utilizes electron charges stored in a floating gate to

accomplish non-volatile data storage [4]. The floating gate is usually made of polysilicon (polycrystalline silicon) and is sandwiched by dielectric layers. The bottom layer adjacent to the silicon substrate is called tunnel oxide. The upper layer adjacent to the ploysilicon control gate is called inter-poly dielectric (IPD) [4]. A cross-sectional view of floating-gate type flash memory is illustrated in Fig 1.2. The charges stored inside the floating gate determine the threshold voltage, and thus impacts the source-to-drain current. By sensing the source-to-drain current, the memory status of the device can be detected [4].

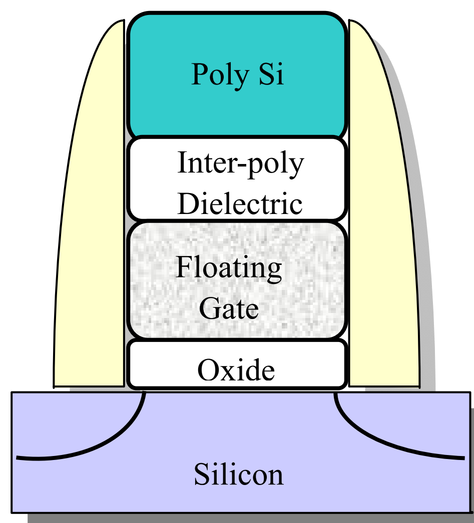

Fig. 1.2 A structure illustration of the floating-gate flash memory. The charges are stored inside the floating gate which is sandwiched between the inter-poly dielectric and bottom oxide.

Floating-gate type flash memory has been successfully developed during the last two decades [1]. However, it is facing severe challenges as the semiconductor industry enters the 45-nm technology node. Besides the common challenges faced by CMOS transistors (such as nano-dimension patterning, strong short channel effect,

and wide spread-out of process variation, etc.), floating-gate type flash memory also faces other special challenges. First, both tunnel oxide (T_{ox}) and inter-poly dielectric (IPD), using conventional SiO_2 and Si_3N_4 films, have reached their thickness scaling limit of 8 nm and 12 nm, respectively [4, 5]. This requires the introduction of high κ dielectrics to continue the scaling with decreased leakage current and maintain a reasonable coupling ratio (~ 0.7) of control-gate (CG) to floating-gate (FG) [5]. However, the introduction of high κ dielectrics may cause reliability issues [5]. The second problem is the strong cell-to-cell interference due to the scaling-down of the distance between floating gates, which also causes a concern of reliability [6]. Lastly, the most fundamental issue in floating-gate type flash memory is the significant reduction in the electron numbers during further scaling. For 30-nm gate length devices, the electron number is expected to be less than 100 for a threshold shift of 6 V. In order to achieve the 10-years data retention, a maximum of 10 electrons are allowed being loss within 10 years. Such low electron loss tolerance has set a big challenge for better achievement of data retention and endurance [1, 6-8]. In summary, all these challenges imply that it is difficult to continue the scaling of floating-gate type flash memory without performance degradation, thus a new type of non-volatile memory is needed.

1.2 Nitride-based SONOS-type Flash Memory

1.2.1 Overview of Non-volatile Memory Candidates

To replace the floating-gate type flash memory, several types of non-volatile

memories have been proposed, such as nitride-based poly silicon-oxide-nitride-oxide-silicon (SONOS-type) flash memory, phase-change random access memory (PCRAM), ferroelectric random access memory (FeRAM), magnetic random access memory (MRAM), etc [5]. The characteristics of non-volatile memory candidates are summarized in Table 1.1.

	SONOS flash memory	FeRAM memory	MRAM memory	PCRAM memory
Operational mechanism	Electronic charge	Polarization	Magneto-resistance	Phase resistance
Cell size per bit / F^2	1~3.3*	15	20	4
Program endurance	10^5	10^{14}	10^{16}	10^{10}
Read	Non-destructive	Destructive	Non-destructive	Non-destructive
Read voltage	2 V	1.2 V	3.3 V	0.4 V
Program voltage	6~15 V	1.2 V	3.3 V	1 V
Program speed	1 – 1000 µs	80 ns	25 ns	<500 ns
Erase speed	1 – 100 ms	80 ns	25 ns	<500 ns
Read speed	60 ns	80 ns	30 ns	50 ns
Block erase	Yes	No	No	No
New materials	No	Yes	Yes	Yes
Multi-bit storage	Yes	No	No	Yes
cost per bit	Low / high	High	High	Medium
Retention (years)	10 - 20	10	> 10	> 10
Technology issues	Endurance; high voltage; gate length scale	Cell size scalability	Write current; disturbance; cell size scaling	Thermal; cross talk; multi-bit

Table 1.1 A comparison of the characteristics of the non-volatile memories [3, 5, 9, 10]. The characteristics of the SONOS-type flash memory combine the parameters for both NOR-type and NAND-type memory cells.

Based on the information in Table 1.1, it is obvious that none of the four non-volatile memory candidates succeeds in all characteristics, but all of them have key advancements in at least some of the important areas. MRAM offers the fastest operation speed, the longest "life span" and the highest programming endurance [9]. While PCRAM offers the best scaling capability and the lowest programming/reading voltages [9]. FeRAM has a relatively fast operation speed, low energy consumption and high program-erase endurance [3]. Besides, FeRAM is not a perfect non-volatile memory because it is a destructive read-out technology, so every read is accompanied by a write to restore the data [3]. Compared to others, SONOS-type flash memory possesses several advantages.

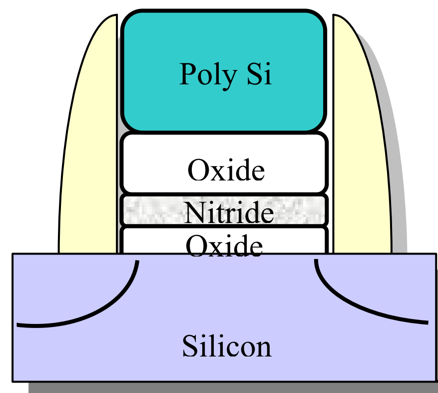

Fig. 1.3 A structure illustration of the nitride-based SONOS-type flash memory. The charges are locally trapped inside the nitride film and immobile.

Firstly, SONOS-type flash memory can achieve the highest chip density because it consists of only one transistor, as shown in Fig. 1.3, thus lower cost per bit [5]. The SONOS memory cell is a simple MOSFET cell, except that a silicon nitride trapping layer is inserted between the dielectrics. In comparison, other types of

non-volatile memories consist of more than one transistor. A FeRAM, MRAM or PCRAM cell generally has one transistor and one capacitor, one transistor and one magnetic tunnel junction, or one bipolar junction transistor and one resistor, respectively [10]. Therefore, their processes are more complicated than SONOS-type flash memory. Secondly, SONOS-type flash memory can implement multi-bit-per-cell storage scheme easily [4]. By controlling the amount of charges stored in nitride trapping layer, four or eight distinct states of threshold voltages can be achieved within a single cell, which corresponds to two-bit-per-cell or three-bit-per-cell memory [7]. The multi-bit storage scheme enhances the memory capacity significantly without increasing process steps, thus reducing the memory cost per bit dramatically. Besides, it is worth to note that PCRAM is also capable of two-bit-per-cell storing scheme but encounters huge challenges in implementing three-bit-per-cell storing scheme [5]. Thirdly, SiO_2 and Si_3N_4 used in SONOS-type flash memory are commonly used in conventional CMOS processes [4]. This enables the fabrication process of SONOS memory compatible with current CMOS processes, and especially suitable for embedded memory applications. In contrast, new materials used in other non-volatile memories (like $PbZr_{0.52}Ti_{0.48}O_3$ in FeRAM, $CoFe/AlO_x/NiFe$ in MRAM, $Ge_2Sb_2Te_5$ in PCRAM) are not fully compatible with conventional CMOS processes [3, 9]. Lastly, the capability of block erasure in SONOS-type flash memory makes the entire array to be erased quickly and simultaneously like a flash (so called "flash" memory) [4]. This simultaneous erasure compensates the disadvantage of slow erasing speed of SONOS-type flash memory

and makes it an edge in large-scale data storage application [4].

In addition, compared with conventional floating-gate type flash memory, nitride-based SONOS-type flash memory has an advancement of storing more electrons, making further scaling possible [1]. Furthermore, due to the localized-charge-storing mechanism, the nitride-based SONOS-type flash memory is free from cell-to-cell interference and more tolerant of dielectric defects [6].

In short, all of these advantages make the nitride-based SONOS-type flash memory a strong candidate to replace the conventional floating-gate type flash memory. Of course, SONOS-type flash memory also faces several challenges in data retention and endurance which will be discussed later in this chapter.

1.2.2 A Brief Review of SONOS-type Flash Memory

The poly silicon-oxide-nitride-oxide-silicon (SONOS) memory is a multi-dielectric device consisting of three layers. The middle layer - silicon nitride - acts as trapping layer holding charges. Unlike traditional floating-gate type flash memory, the charges stored in nitride layer are immobile and distributed discretely. These discrete charges are responsible for the threshold voltage shift. In order to retain these charges for long duration and be free from external disturbance, the nitride layer is sandwiched by two oxide layers, as shown in Fig. 1.3. Similarly to floating-gate type flash memory, the bottom oxide layer adjacent to the silicon substrate, called tunnel oxide, permits the transfer of charges from the silicon

substrate to nitride trapping layer by tunneling mechanism [11]. The top oxide layer isolating the gate electrode from nitride layer, called blocking oxide, was introduced in 1980s to allow the further thickness scaling of the nitride layer from 25 nm to 5 nm and allow lower programming voltages [11].

For the traditional nitride-based SONOS memory cells, the tunnel oxide was normally set to 1 to 2 nm to achieve a fast erase speed [12]. However, such thin layer significantly changes leakage due to the direct tunneling mechanism, thereby, resulting in poor data retention over time [1, 13]. On the other hand, if the tunnel oxide is increased to 4 nm to achieve good data retention, the SONOS memory cell will encounter some problems, such as slow erasure and even early erasing saturation leading to smaller operation window [14]. In order to solve this quandary, different methods have been investigated, such as band engineering SONOS (BE-SONOS) [15-17], using high-κ dielectric in blocking oxide layer or trapping layer [14, 17-21], atomic ratio tuning between Si and N in trapping layer [22, 23], etc.

Band engineering SONOS (BE-SONOS), first proposed by H.L. Lue *et al.*, uses triple layers of ultra-thin oxide-nitride-oxide (ONO) to replace single layer tunnel oxide (SiO_2) [15]. Because of the conduction band offset between oxide and nitride, the ONO tunnel oxide structure allows different tunneling distance under different situation. For example, under the situation of data retention, the charge will tunnel through all three layers before escaping away because of the low electric field on gate stack; on the other hand, under the situation of memory programming or

erasing, high electric field results in strong band bending thus short tunneling distance (probably only the single layer). Therefore, both good retention and high operation speed can be easily achieved [15, 24]. Another method named as TANOS (TaN-Al_2O_3-nitride-oxide-silicon), proposed by C. H. Lee *et al.*, used a high κ layer of Al_2O_3 as blocking oxide and high work function TaN as metal gate [21]. The TANOS structure cells have a higher electric field in tunnel oxide, but a lower electric field in blocking oxide compared to conventional SONOS cells, therefore, enabling higher programming speed and lower programming voltages [20, 21]. Similarly, due to the scaling limit of physical thickness of 4 nm for nitride layer [25], some groups used high κ dielectrics (such as $HfSiO_x$, $HfAlO_x$ Al_2O_3, HfON or HfO_2) as trapping layer to achieve higher electric field in tunnel oxide, resulting in higher programming / erasing speed [18, 19, 26-28]. But the trapping mechanism in these new dielectrics is believed to be much different from silicon nitride, thus requiring further investigations [18, 26]. Simultaneously, some other groups were still focusing on nitride trapping layer and have achieved improved data retention by simply varying nitrogen or hydrogen concentrations [29-31]. It was found that the reduced hydrogen concentration (lower density of Si-H bond) in nitride film could improve the data retention [29]. Besides, D.S. Golubović *et al.* reported that lower nitrogen concentration in nitride film could result in wider memory window, better cycling endurance, improved erase-state retention but degraded program-state retention [30]. The author further mentioned that modifying the nitride film from nitrogen-rich to silicon-rich would increase hole trap energy level but reduce electron trap energy

level [30]. Similar deduction was also reported by T.H. Kim *et al.* that the silicon-rich nitride film has larger trap density in shallow energy level than stoichiometric silicon nitride film [31].

1.2.3 Using High-κ Dielectric to Improve Memory Performance

Among the above methods, using high-κ Al_2O_3 as blocking oxide (TANOS) is believed to be the most successful method and has been widely used in other methods, like the BE-SONOS method [17], the nitride layer engineering method [22], the evolved 3-D structure method (FinFET) [32], etc.

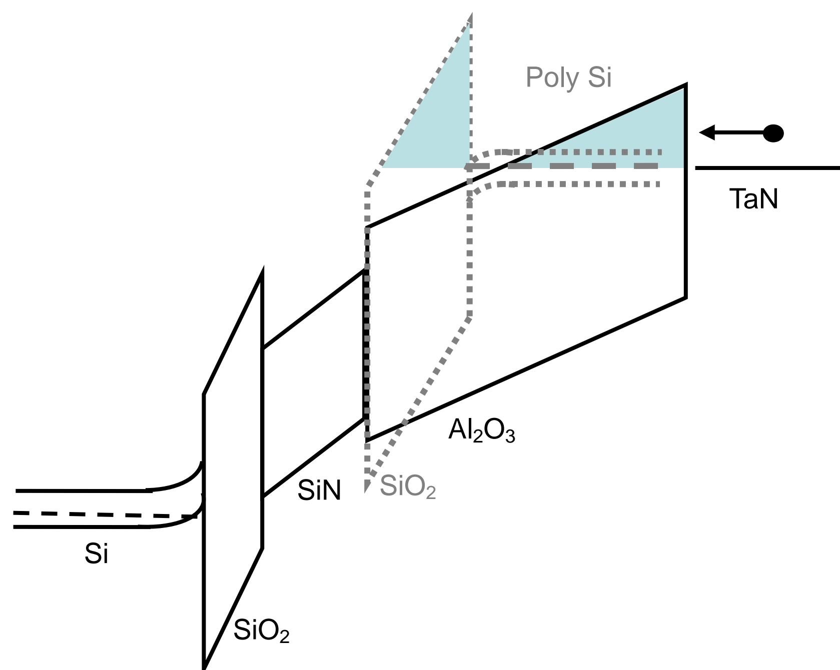

Fig. 1.4 A comparison of the energy band diagram between conventional SONOS memory cell (dashed line) and TANOS memory cell (solid line) under the erase operation. The TANOS memory cell exhibits longer electron tunneling distance, leading to higher programming / erasing speed due to the lower back-tunneling current.

The energy band structure of TANOS under the erase operation is illustrated in Fig. 1.3. The band structure of the conventional SONOS cell is also plotted as dashed lines as a comparison. For an easy illustration, both Al_2O_3 and SiO_2 are set to the same equivalent oxide thickness (EOT). Because of the higher dielectric constant, Al_2O_3 blocking oxide layer has a thicker physical thickness, thus a smaller electric field compared with SiO_2 blocking oxide layer under the same voltage stress. Although having a relative smaller energy band-gap, Al_2O_3 still has a lower tunneling probability (longer electron tunneling distance) than SiO_2, which is shown as the shadow area in Fig. 1.4. This lower tunneling current through Al_2O_3 blocking oxide layer in TANOS cells provides faster programming / erasing speed and lower programming voltage compared with conventional SONOS cells [20]. Furthermore, TaN has a relatively higher work function than n^+ polysilicon. Thus the electron barrier offset between TaN gate and blocking oxide becomes larger. The larger barrier offset will further reduce the back-tunneling electron current during erasure, therefore, increases the erase speed and suppresses the erase saturation [21, 24].

A significantly improved performance is achieved when using Al_2O_3 instead of SiO_2 as a blocking oxide [21]. But the κ value of Al_2O_3 is only about 9, which is relatively low compared to other high-κ dielectric candidates [33]. Thus, it is possible to further improve the nitride-based SONOS-type memory performance if even higher κ dielectric is used as blocking oxide. However, few papers have explored this possibility. With a κ value of 12, hafnium silicate was investigated by Erlbacher *et al.* as a blocking oxide [34]. The author showed improved erasing speed and a much

better time-to-breakdown reliability. However, the memory cells exhibited initial decay of flat-band voltage and data retention degradation [34]. In order to improve the data retention, the author further suggested reducing the physical thickness of hafnium silicate [34], which is contrary to original goal. Another high-κ dielectric HfAlO (κ~15) was also investigated by Wang *et al.* as both blocking oxide and tunnel oxide while with HfSiO as a trapping layer [27]. The author showed high erasing speed and good data retention [27]. But it was hard to evaluate the effect of each single layer because too many new materials were used at the same time.

In this study, we explored the possibility of using high-κ dielectrics as blocking oxide to further improve the programming/erasing speed as well as the memory data retention.

1.3 Lanthanum-incorporated High-κ Dielectrics

Over the past decade, many high-κ dielectrics have been investigated, such as Al_2O_3, ZrO_2, Y_2O_3, TiO_2, La_2O_3, Ta_2O_5, HfO_2, $SrTiO_3$ and $Ba_xSr_{1-x}TiO_3$, etc. In order to find suitable high-κ dielectrics for memory application, it is necessary to know the key characteristics of high-κ dielectrics and the requirements from memory cells first.

1.3.1 Dielectric Parameters for the Selection of High-κ Thin Film

As for the thin film dielectric evaluation, the key parameters have been suggested by Wilk *et al*, such as dielectric constant, band gap, band alignment,

thermodynamic stability, film morphology (crystal and amorphous phases), defects, reliability, etc. [35]

Dielectric constant of a material, also named as its relative permittivity, is defined as

$$\kappa = \varepsilon_r / \varepsilon_0 \tag{1-1}$$

where ε_r is the static permittivity of the material, and ε_0 is the permittivity of free space where $\varepsilon_0 = 8.854\times10^{-12}$ F/m. Using the dielectric constant, the capacitance of a parallel-gate-electrode capacitor is expressed as

$$C = \frac{\kappa\varepsilon_0 A}{t_{ox}} \tag{1-2}$$

where C is the capacitance of the capacitor, A is the area of overlap of gate electrodes, and t_{ox} is the physical thickness between the two electrodes. The equation (1-2) shows that the capacitance can remain unchanged with a thicker physical thickness by using a higher κ dielectric. Thus, hopefully, the physically thicker film will result in a lower leakage current and thereby improve the device reliability.

When replacing the oxide with a new high-κ dielectric, it is convenient to use the term of "equivalent oxide thickness" (EOT) to monitor the "electrical thickness" of the new high-κ dielectric. The equivalent oxide thickness (t_{eq}) is defined as the thickness of SiO_2 needed to maintain the same capacitance density as the high-κ material has in a capacitor. It is given by

$$t_{eq} = \frac{\kappa_{OX}}{\kappa_{high-\kappa}} t_{high-\kappa} \tag{1-3}$$

where κ_{OX} and $\kappa_{high-\kappa}$ is the dielectric constant of the SiO_2 (~3.9) and the replaced

high-κ dielectric, respectively, and $t_{high\text{-}\kappa}$ is the physical thickness of the replaced high-κ dielectric.

Ideally, a high-κ dielectric with higher κ value and wider band gap (E_g) is desired. However, this is impossible in reality since there is a tradeoff between the κ value and the energy band gap, as shown in Fig. 1.5 [36]. Generally, the energy band gap decreases as the κ value increases. This relationship implies that there is no ideal dielectric with both a wide band gap and a high κ value.

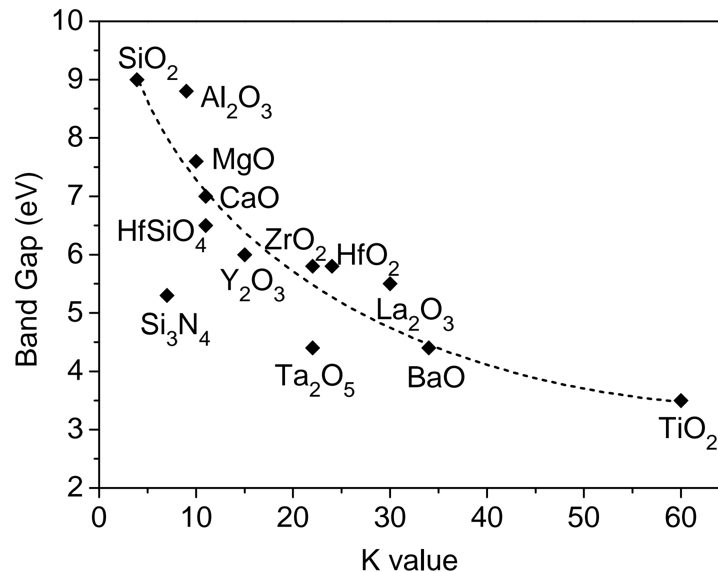

Fig. 1.5 An overview of dielectric constant (κ value) versus energy band gap. It implies a general rule of tradeoff between the κ value and the energy band gap [36].

Besides the band gap (E_g), the band alignment between the dielectric and semiconductor substrate or metal gate is another key parameter in dielectric evaluation. As an example, Figure 1.6 schematically shows the conduction band offset (ΔE_c) and valence band offset (ΔE_v) against silicon when aligning oxide and silicon

together. The conduction band offset (ΔE_c) and valence band offset (ΔE_v) against silicon are key parameters in determining the electron and the hole current, respectively. Normally, the electron current has an exponential relationship with the barrier offset, as expressed in the formulas of Schottky emission, Frenkel-poole emission and tunneling emission [37].

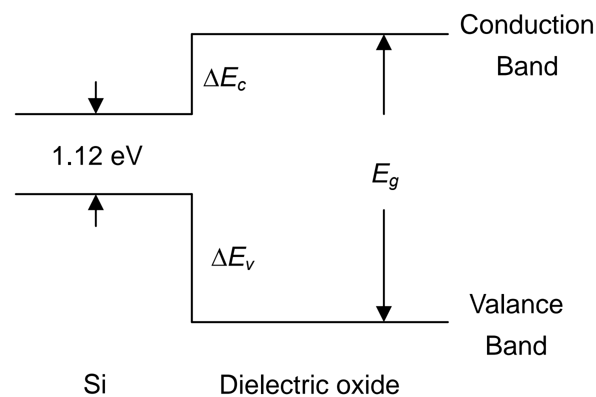

Fig. 1.6 A schematic of conduction band offset (ΔE_c) and valence band offset (ΔE_v) of a dielectric oxide over silicon. Higher ΔE_c and higher ΔE_v are desired to achieve the smaller leakage current.

The gate-first process scheme requires the gate dielectric to withstand the high temperature anneal. This annealing temperature is typically greater than 900ºC. The purpose of this anneal is to activate the source-drain dopants. Under such high temperatures, most high-κ dielectrics would change their phases from amorphous to poly crystalline. It is generally believed that the formation of crystalline phase in a thick high-κ dielectric would degrade the leakage current due to possible leakage route through the grain boundaries [35].

In addition, unlike in SiO_2, the bonds in high-κ dielectric oxides cannot relax

easily, which results in a high concentration of intrinsic defects [38]. The research of these intrinsic defects is still ongoing and there remain a lot of debates. Generally, it is believed that most of these defects in high-κ dielectrics origin from imprecise stoichiometry, disorder of atoms, impurities, dislocation at grain boundaries, dipoles or unwanted bonds at the interface [35, 38]. These defects would act as the charge center and lead to an increase of leakage current, a shift of threshold voltage, a decrease of lifespan or even an earlier electrical breakdown [38]. The quantity of these defects can be partially reflected by the hysteresis of the capacitance-voltage (*C-V*) curves. Furthermore, these defects and reliability in high-κ dielectric films are also highly dependent on the deposition method and post deposition annealing treatments. The reliability is normally characterized by the methods of stress-induced leakage current (SILC), bias temperature instability (BTI), time-dependent dielectric breakdown (TDDB), and mean time to failure (MTF), etc.

1.3.2 Lanthanum-incorporated High-κ Dielectrics: $LaAlO_x$ and $HfLaO_x$

In nitride-based SONOS-type flash memory, a suitable blocking oxide candidate should have high enough electron and hole barriers to retain charges inside the nitride film for a long time. The electron or hole barrier over silicon is required to be larger than 1 eV [35]. Because there is a trade-off relationship between κ value and energy band-gap, as shown in Fig. 1.5, high-κ dielectrics with a κ value in the range of 15 to 30 is mostly preferred. In addition, the gate-first process scheme requires dielectrics that can withstand high source-drain temperature anneal.

Taking process requirements (such as water nonreactive) and conduction band offset requirement (1 eV over Si conduction band edge) into consideration, possible candidates from periodic table are narrowed down to Al_2O_3, Y_2O_3, HfO_2, ZrO_2, La_2O_3 and other lanthanides oxide (such as Pr_2O_3, Gd_2O_3, Lu_2O_3, etc.). However, all these oxides have their own predominant disadvantages, such as a relatively low κ value (9 to 15) for Al_2O_3, Y_2O_3 and Lu_2O_3, low crystallization temperatures for ZrO_2 and HfO_2, and strong hygroscopic property for lanthanides oxides. In order to minimize these undesirable properties, ternary dielectrics were proposed, such as $HfSiO_x$, $ZrSiO_x$, $HfAlO_x$, $LaAlO_x$, $HfLaO_x$, etc. In this way, the ternary dielectric can, normally, inherit the desirable properties from two dielectric oxides, while simultaneously minimize their undesirable properties. For example, it is reported that $HfSiO_x$ has the properties of a large energy band gap, a high κ value (~10 to 15), improved crystallization temperature up to 900ºC, and improved reliability, etc.

Among these ternary dielectrics, lanthanum-incorporated high-κ dielectrics ($LaAlO_x$ and $HfLaO_x$) provide high κ values ranging from 13 to 33 [39-45]. And their conduction band offsets over silicon are reported to be greater than 1.5 eV [46-48]. Moreover, the stoichiometric $LaAlO_3$ and $HfLaO_3$ can remain amorphous phase up to 850 ºC [41-43, 49, 50]. These properties meet the requirement for memory application to a great extent. It was also reported that, with the incorporation of lanthanum, the reliability of dielectrics can be greatly improved [51, 52]. Furthermore, according to the simulation results, lanthanum-incorporated dielectric films offer the lowest leakage current compared to other high-κ dielectrics [53]. Therefore, lanthanum-

incorporated high-κ dielectrics ($LaAlO_x$ and $HfLaO_x$) were chosen to be targeted as blocking oxide in SONOS-type flash memory in this study.

1.3.3 Current Developments of $LaAlO_x$ and $HfLaO_x$ Dielectrics

$LaAlO_x$ and $HfLaO_x$ have been widely studied as possible candidates to replace SiO_2 as the gate dielectric.

A. Literature Review of $LaAlO_x$

The dielectric constant (κ) of $LaAlO_x$ films varied from 13 to 33 in different papers. In the study by R. Devine, a κ value of 14 was reported for both amorphous and poly-crystalline $LaAlO_x$ using sputter method [40]. Similar κ value of 14 and 13 were also reported for films deposited using MBE or ALD method by Vellianitis *et al.* and Lim *et al.*, respectively [39, 54]. In contrast, , Park *et al.* reported a κ value of 24 when using the same MBE deposition method [55]. An even higher κ value of 33 was reported by Shi *et al.* for amorphous $LaAlO_xN_y$ ($y = 0.4$) using the pulse laser deposition (PLD) method [42]. However, such high κ value has not been repeated by any other groups so far.

The optical energy band gap of $LaAlO_3$ was reported by Cicerrella *et al.* to be 5.84 eV and 6.33 eV for thinner and thicker films, respectively, using spectroscopic ellipsometry [56]. Using the XPS method, a higher value of the energy band gap (6.5 eV) of $LaAlO_3$ was reported by Suzuki *et al*. In addition, the conduction band offset

and valence band offset against Si were measured to be 2.4 eV and 3.0 eV, respectively [46]. For single crystalline $LaAlO_3$, similar band offsets were reported by Mi *et al.* [47]. Moreover, the large values of band offset against silicon of $LaAlO_3$ have a great impact on leakage current. The leakage current flowing through $LaAlO_3$ film, reported by Goldenblum *et al.*, was found to fit the space charge limited (SCL) current behavior very well [57]. That is, the square root of the leakage current had a linear relationship with the applied voltage. The space charges caused by impurities inside $LaAlO_3$ were suggested to be located near the Si band edge [57].

The reported temperature for the onset of $LaAlO_3$ crystallization ranged from 850ºC to 1000ºC. It was found that $LaAlO_3$ films deposited by the CVD method had a slightly lower crystallization temperature than the ones deposited by the PVD method. Shao *et al.* and Gaskell *et al.* both reported that $LaAlO_3$ films deposited by using MOCVD and ALD would remain amorphous after annealing at 850ºC [43, 49]. However, LaAlO films deposited by using the PVD method like sputter or MBE can remain amorphous after annealing at even higher temperature, such as 935ºC or 1000ºC [50, 58].

Different annealing conditions were investigated in order to improve the film quality,. Miotti *et al.* and Edon *et al.* both reported that thermal annealing at 600ºC under O_2 ambient on $LaAlO_3$ films would result in better electrical characteristics as compared to films annealed in an N_2 ambient [59, 60]. However, the side effect of high temperature anneal under O_2 ambient will form a much thick interfacial layer

which is undesired. Besmehn *et al.* revealed that the constitution of interfacial layer changed from SiO_x to La-Al-Si-O at 500ºC anneal [61]. In contrast, Clémer *et al.* reported that the SiO_x interfacial layer only existed at 800ºC anneal, and the transition of SiO_x interfacial layer to La-Al-Si-O interfacial layer occurred at 930ºC [62]. In addition, a high temperature anneal would not only result in the interfacial layer transformation, but also atomic migration. When film was annealed at 800ºC for 60 s, reported by Miotti *et al.,* Si atom migrated from substrate into sputtered $LaAlO_3$ film and this migration could be greatly suppressed by thermal nitridation of $LaAlO_3$ using NH_3 [59]. The suppression of atomic migration were also reported by Sivasubramani *et al.* using plasma nitridation method [50].

The lattice mismatch is only 1.3% between crystalline $LaAlO_3$ and Si substrate. Theoretically, it is possible to epitaxially grow single crystalline $LaAlO_3$ on Si substrate. However, simulations revealed that a stable interface between stoichiometric $LaAlO_3$ and Si could not be obtained [63]. This conclusion was consistent with the experiment reports by Gaillard *et al.* [64]. In order to achieve epitaxial growth, a seed layer of $SrTiO_3$ or γ-Al_2O_3 was applied as a template between the $LaAlO_3$ and the Si substrate. By this way, the single-crystalline $LaAlO_3$ films were successfully deposited using molecular beam epitaxy (MBE) method [47, 65].

In comparison with La_2O_3, $LaAlO_x$ exhibited better hydroscopic property, lower leakage current and smaller *C-V* hysteresis [66, 67].

B. Literature Review of $HfLaO_x$

Compared to $LaAlO_x$, there are fewer reports on the $HfLaO_x$ dielectric. The reported dielectric constant of $HfLaO_x$ ranges from 18 to 23 for amorphous films and monoclinic crystal films [44, 45, 68]. However, when La percentage was 4%, a higher κ value of 28 for $HfLaO_x$ was reported by Yamamoto *et al.* [41]. Author attributed this increment of κ value to cubic crystal formation [41]. In addition, the energy band gap, valence band offset and conduction band offset of amorphous $Hf_2La_2O_7$ over Si was measured to be 5.6 eV, 2.4 eV and 2.1 eV, respectively, using XPS [48].

The crystallization temperature of amorphous $Hf_2La_2O_7$ was reported to be 900ºC [68, 69]. Furthermore, when La percentage decreased from 50% to 15%, the crystallization temperature dropped to 600ºC accordingly[69]. The relationship between crystallization temperature and La percentage was further summarized by Yamamoto *et al.* [41].

Using $Hf_2La_2O_7$ as gate dielectric, devices showed a leakage current of $J_g = 4 \times 10^{-8}$ A/cm^2 with an EOT of 18.7 Å at $V_g = V_{fb} - 1$ V, which was almost 2 orders smaller in magnitude than that of HfO_2 gate dielectric devices [70]. Furthermore, in comparison with HfO_2 gate dielectric, $Hf_2La_2O_7$ gate dielectric devices exhibited 5% to 10% higher electron mobility on Si at high electric field due to lower electron trapping defects [70]. Besides, using $HfLaO_x$ as gate dielectric, Wang *et al.* first reported that the effective work function of TaN metal gate could be tuned to the ideal Si conduction band edge, which was a great breakthrough of implementation of high-κ/metal gate scheme in CMOS devices [71]. The capability of work-function

tuning was due to the incorporation of lanthanum and this tuning behavior was further confirmed by Alshareef *et al.* [72].

In summary, $LaAlO_x$ and $HfLaO_x$ exhibit attractive characteristics in gate dielectric application. Furthermore, these characteristics (such as dielectric constant, crystallization temperature, interfacial quality) are dependent on process conditions, chemical precursors and deposition methods.

1.3.4 Using ALD $LaAlO_x$ and $HfLaO_x$ Dielectrics in Memory Application

As discussed just now, $LaAlO_x$ and $HfLaO_x$ have been widely investigated as gate dielectrics in CMOS devices and exhibit promising properties. However, few groups have investigated the possible application of $LaAlO_x$ and $HfLaO_x$ in SONOS-type flash memory. The requirements for gate dielectric application and memory application are quite different. Generally, the requirements for gate dielectric focus more on the leakage current at -1 V, *C-V* hysteresis, channel mobility, and even effective work function. In contrast, the requirements for flash memory application concentrate more on the leakage current under high voltage (such as 16 V or -20 V), cycling endurance, data retention, etc. Furthermore, the target EOT of dielectric in flash memory is usually around 4 nm, which is much greater than that of gate dielectric (~ 1 nm). In words, different application requires unique target investigation. Therefore, in this study, lanthanum-incorporated high-κ dielectric ($LaAlO_x$ and $HfLaO_x$) are investigated focusing on the SONOS-type flash memory application.

Generally, there are several methods to perform the high-κ dielectric deposition, such as sputtering, electron beam evaporation (e-beam), molecular beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD), and atomic layer deposition (ALD) [73]. Among these, ALD deposition method has the advantages of precise thickness control, excellent conformal step coverage, good film uniformity and relatively low deposition temperature, etc [73]. These advantages, especially the conformal step coverage, give the ALD method an edge in the integration of 3-D structures. Based on ITRS 2007, the integration of 3-D structure devices (such as double-gate structure, triple-gate structure, nano-wire structure, etc.) have been proposed to replace the planar devices in the year of 2020 due to the huge difficulties encountered by planar MOSFET in controlling short channel effects and channel dopant distributions [1, 5]. Further, some other special 3-D structures, such as recessed channel structure, have also been proposed to assist the aggressive scaling of multi-bits memory cells. The stored charges in these multi-bit memory cells are physically separated. [74]. In brief, all of these 3-D structure cells require a highly conformal thin film on geometry surface. Thus the ALD deposition method is needed to meet this requirement.

However, due to the low volatility of Lanthanum precursors, ALD of lanthanum-incorporated dielectrics has not been well studied [75]. Therefore, great effort had been made to achieve successful deposition of ALD dielectrics in this study.

1.4 Outline of the Thesis

As discussed above, nitride-based SONOS-type flash memory is a most promising candidate to replace the traditional floating-gate type flashed memory for continuous scaling-down of memory size. The performance of nitride-based SONOS-type flash memory has been greatly improved by using Al_2O_3 and TaN as the blocking oxide and gate electrode, respectively. However, the κ value of Al_2O_3 is only around 9, the dielectrics with even higher κ value are needed as blocking oxide to further improve memory performance. Among the high-κ dielectrics, lanthanum-incorporated dielectrics ($LaAlO_x$ and $HfLaO_x$) were chosen in this study due to its relatively high κ value, large conduction band offset and good thermal stability.

Lanthanum-incorporated high-κ dielectrics ($LaAlO_x$ and $HfLaO_x$) were deposited by ALD method. The ALD process conditions and special ALD behaviors of La_2O_3 will be discussed in Chapter 2. In the latter part of Chapter 2, the physical properties of the ALD films will be analyzed. The electrical properties of these ALD films ($LaAlO_x$ and $HfLaO_x$) will be investigate in depth in Chapter 3. Especially, great efforts will be focused on cubic-phase $HfLaO_x$, which provides highest κ values up to 38. Then, in Chapter 4, $LaAlO_x$ and $HfLaO_x$ will be evaluated as the blocking oxide in nitride-based memory cells. The performances of memory cells using $LaAlO_x$, $HfLaO_x$ or Al_2O_3 blocking oxides will be compared, including operation speeds, memory retention, reliability, and endurance, etc. In addition, the key factors of

retention performance will be analyzed, as well as the energy trapping depth in nitride film. Finally, main findings of this study will be summarized in Chapter 5, together with some suggestions for future study.

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Chapter 2 High-К Dielectrics Engineering by Atomic Layer Deposition (ALD)

2.1 Introduction

Atomic layer deposition (ALD), also called atomic layer epitaxy (ALE), is a gas phase thin film deposition method which can be regarded as a special modification of metal-organic chemical vapor deposition (MOCVD) [1]. Compared to MOCVD, ALD allows better thickness control, better uniformity and better conformality. The deposition mechanism behind these advantages will be introduced first, followed by a brief review of ALD precursors for Al_2O_3, HfO_2, and La_2O_3 deposition, respectively. After the specification of ALD process conditions, ALD of La_2O_3 will be investigated. Its special behavior of low deposition rate will be discussed. The possible root cause of low deposition rate of La_2O_3 will be investigated by comparing and analyzing the deposition behaviors between ALD La_2O_3 and ALD $HfLaO_x$. Subsequently, self-limiting characteristic, a special ALD behavior, will be examined for both $HfLaO_x$ and $LaAlO_x$ depositions. Lastly, the film properties of ALD lanthanum-incorporated dielectrics will be investigated, such as vertical uniformity and bottom interface. Furthermore, carbon impurity and silicon impurity inside the $HfLaO_x$ films will be analyzed.

2.1.2 Introduction of ALD Principles

An ALD process requires at least two different vapor-phase precursors. In contrast to normal MOCVD process where precursors are introduced into process chamber simultaneously, ALD process breaks the reaction into two half-reactions by leading precursors into process chamber in separate and alternate pulses. During the pulse flowing, the precursors are chemically adsorbed onto the substrate and react with surface groups. Between two adjacent precursor pulses, inert gas normally flows into ALD chamber to purge the precursor residuals and reactant molecules out [1]. Generally, one ALD cycle consists of a pulse of metal precursor and a pulse of oxidant.

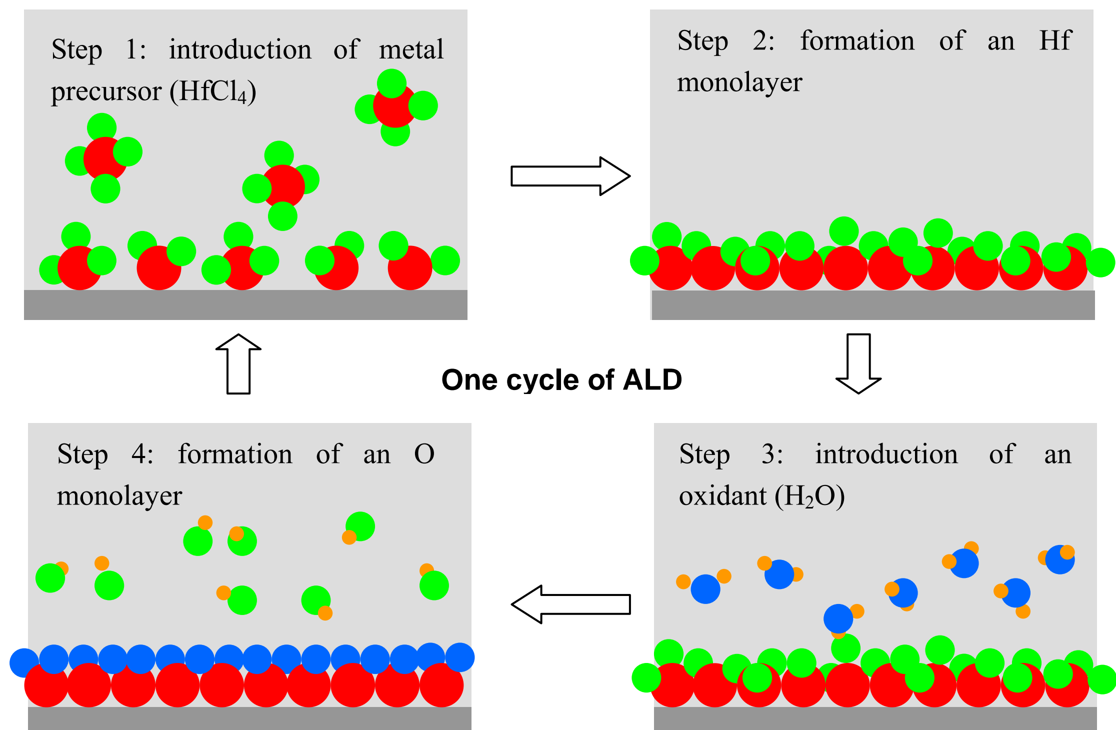

Fig. 2.1 A schematic illustration of an-ALD process cycle. By repeating the ALD cycle, the stoichiometric HfO_2 can be deposited.

A standard ALD process cycle can be divided into four steps [2], as schematically illustrated in Fig.2.1. Firstly, metal precursor molecules are chemically adsorbed onto the substrate surface during the metal precursor pulse. Secondly, the unadsorbed or unreacted metal precursor molecules are purged away by inert gas. Thirdly, oxidant precursor (H_2O) molecules are exposed to the substrate and react with metal precursor molecules forming desired metal oxide material by generating the volatile byproduct. Fourthly, the unreacted precursor residues and volatile byproducts are purged away by inert gas. Thus, by repeating the ALD cycles, thick films are deposited. Theoretically, one ALD cycle deposits a monolayer material. In practice, due to steric hindrances, one ALD cycle usually deposits only a fraction of a monolayer, like half monolayer.

Furthermore, as shown in step 1 and step 3 in Fig. 2.1, the precursor is reactively adsorbed onto the surface. After the precursor is exposed to a certain extent, all of the surface will be covered by the precursor, then reaction saturates and stops. This is called self-limiting reaction, which is one of the most important characteristics of ALD process [1]. To characterize the self-limiting behavior, a plot of pulse length *vs.* growth rate is usually used, as shown in Fig. 2.2. Here, the self-limiting behavior of HfO_2 deposition is used as an example. When pulse length of $HfCl_4$ precursor is greater than 0.4 s, growth rate of HfO_2 keeps constant and is independent on the precursor pulse length. This region is self-limiting region. With this wide region, the deposition rate can be maintained constantly in different cycles, resulting in a strict linear relationship between the film thickness and the numbers of growth cycle. Thus,

By simply varying the cycle numbers, film thickness can be easily and accurately controlled down to the atomic level [1]. Moreover, the reaction in step 1 and step 3 shown in Fig. 2.1 is a pure surface reaction. The pure surface reaction makes the deposition rate consistent everywhere across the wafer regardless of the surface morphology. Thus, almost perfect step coverage can be achieved. Furthermore, the surface reaction provides better control in dopant distribution [3].

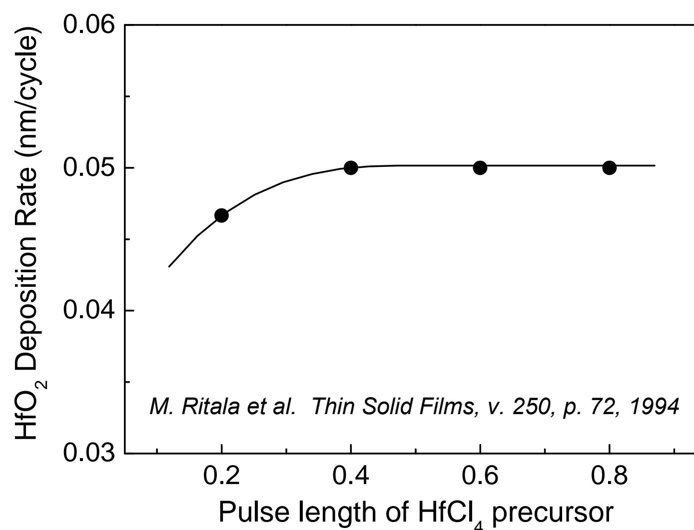

Fig. 2.2 A schematic illustration of self-limiting characteristic using ALD HfO_2 as an example [3]. When the pulse length is greater than 0.4 s, the deposition rate is independent of the pulse length, which implies a wide process window to achieve the constant deposition rate.

In addition, the purge steps (step 2 and step 4 shown in Fig. 2.1) separate precursors into different pulses. Thus the precursors will never meet each other in the gas phase, which eliminate the gas-phase reaction. The elimination of gas-phase reaction greatly reduces the risk of particle formation in gas phase [3]. This is another advantage of ALD process.

2.1.2 A Brief Review of ALD Precursors

An excellent ALD process relies on the successful development of ALD precursors. A good ALD precursor, on one hand, should be highly volatile and thermally stable in gas-phase. On the other hand, the precursor should be aggressively reactive on the deposition surface to reach the self-limiting region quickly and generate inert volatile by-products [1].

The ALD precursors for aluminum oxide and hafnium oxide deposition have been successfully developed. The most popular precursor for aluminum oxide is trimethylaluminum (TMA). It was reported that it can produce high purity films of Al_2O_3 when using H_2O as oxidant [4, 5]. This high purity film contains less than 0.2 at. % of carbon impurity and 1 at. % of hydrogen impurity [6]. For ALD hafnium oxide, there are three popular candidates: hafnium chlorine ($HfCl_4$), tetrakis(ethylmethylamino)hafnium ($Hf(NEtMe)_4$) and bis(methylcyclopentadienyl)-methoxymethylhafnium ($MeCp_2Hf(OMe)Me$). $MeCp_2Hf(OMe)Me$ has high thermal stability and can be used at a high deposition temperature (up to 450ºC). Therefore, it can be used to produce a more uniform film on the geometry surfaces [7, 8]. The disadvantages of $MeCp_2Hf(OMe)Me$ is that it requires O_3 as the oxidant. $HfCl_4$ together with H_2O can also provide high quality HfO_2 with the lowest cost and the widest deposition temperature window of up to 750ºC [9-12]. However, the corrosive byproduct (HCl) would shorten the equipment lifetime [11]. Moreover, the chlorine impurity inside the film (~0.14 at. %) might cause reliability issues [11, 13].

Compared to above two precursors, $Hf(NEtMe)_4$ provides the highest vapor pressure and is most reactive towards a hydroxylated surface [8, 11, 14, 15]. It was reported that the HfO_2 film deposited at 250ºC using $Hf(NEtMe)_4$ contains around 0.3 - 0.6 at. % carbon impurity and 2 at. % hydrogen impurity [14, 15].

In contrast, only limited ALD precursors are available for lanthanum and they are not considered as ideal precursors due to their relative low volatility and high-binding constant [16, 17]. Nieminen et al. reported ALD La_2O_3 deposited using β-diketonate $La(thd)_3$ (thd=2,2,6,6-tetramethyl-3,5-heptanedione) and ozone [18]. However, this process yielded a relatively high concentration of carbon impurity (~ 3 at. %) in the deposited film. In order to improve the film quality, tris(N,N'-diisopropylacetamidinato)lanthanum, $La(iPrAMD)_3$, was proposed by Lim *et al.* as a La precursor to deposit LaAlO together with TMA and water as Al precursor and oxidant, respectively [19]. A non-self-limiting process was reported when depositing ALD La_2O_3. A few other groups used Tris(bistrimethylsilylamido)-lanthanum, $La[N(SiMe_3)_2]_3$, as the La precursor to deposit La_2O_3 together with H_2O as oxidant [20-22]. However, the deposited films contained a large amount of Si impurity (~ 8 at. %), which would degrade the dielectric constant [23]. Recently, attractive performance of ALD La_2O_3 was reported by using tris(i-propylcyclo-pentadienyl) lanthanum, $La(iPrCp)_3$, as the lanthanum precursor. The self-limiting behavior was observed and the carbon impurity was detected to be lower than 1 at. % [24].

2.3 Experiment Conditions

In this work, ALD process was performed in a Genus Lynx2 ALD reactor. $Hf(NEtMe)_4$, TMA, $La(iPrCp)_3$ and H_2O were selected as Hf precursor, Al precursor, La precursor and oxidant, respectively. The precursors of $La(iPrCp)_3$, $Hf(NEtMe)_4$, and TMA were all kept in stainless steel bubblers and maintained at 180ºC, 90ºC and room temperature, respectively. During the ALD deposition, N_2 was used as the precursor carrier gas; and the chamber base pressure was set to 200 mTorr. As mentioned before, a deposition cycle consists of a pulse of metal precursor supply and a pulse of oxidant supply. In between these two pulses, Ar gas was kept flowing for 3 - 8 sec to purge precursor residuals and reactant molecules away.

In addition, it is worth to note that, during our ALD deposition, there is a small gap between the top-surface of heater and the backside of wafer which sit on the lift pins. So the actual wafer temperature is expected to be lower than the set-point of the deposition temperature. Moreover, because of the hardware capability, the deposition temperature cannot be set to below 270ºC. Otherwise, the heater will be automatically tripped off due to the temperature instability.

2.4 ALD Process of Lanthanum-incorporated Dielectrics

A. Temperature Window for Al_2O_3 and HfO_2 Deposition

The deposition temperature for Al_2O_3 and HfO_2 deposition in our ALD system

were investigated first. The thicknesses were measured using ellipsometer. As shown in Fig. 2.3, when deposition temperature varied from 270ºC to 500ºC, the deposition rate of ALD Al_2O_3 exhibited a concave shape. The lowest deposition rate was ~ 0.45 Å per cycle at the temperature of 450ºC. When the temperature was below 450ºC, the deposition rate decreased as the temperature increased. On the other hand, when the deposition temperatures were greater than 450ºC, deposition rate trended up. This up-trend of deposition rate is believed to be caused by thermal decomposition of TMA. Thus, the temperature window for La_2O_3 is suggested to be from 270ºC to 450ºC in our ALD system.

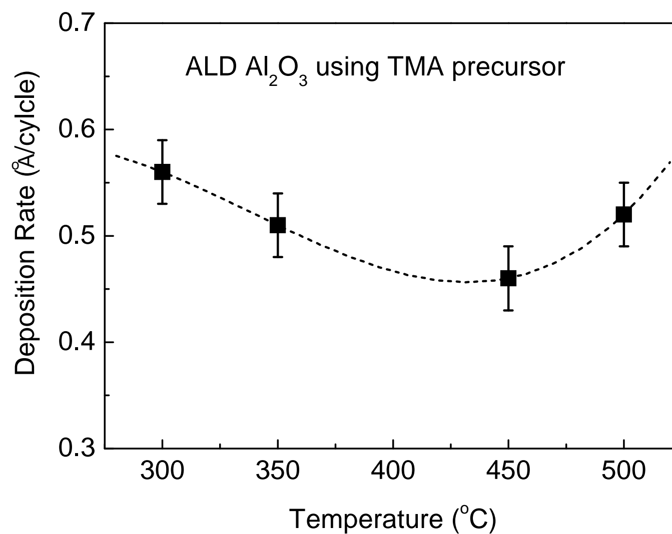

Fig. 2.3 The deposition rate of Al_2O_3 as a function of deposition temperatures. The deposition temperature for ALD Al_2O_3 is suggested to be below 450ºC.

The self-limiting characteristic of HfO_2 using $Hf(NEtMe)_4$ precursor is shown in Fig. 2.4. Under the deposition temperatures of 270ºC and 300ºC, the deposition rate of HfO_2 remained constant as $Hf(NEtMe)_4$ pulse length increased from 1 sec to 3 sec.

This implies a good self-limiting behaviour. However, when deposition temperature further increased to 350ºC, deposition rate increased as $Hf(NEtMe)_4$ pulse length increases. Again, this increase is caused by the thermal decomposition of $Hf(NEtMe)_4$ and indicates that self-limiting behaviour is ruined. Thus, the deposition temperature for HfO_2 deposition ranges from 270ºC to 300ºC in our ALD system. This temperature window is consistent with other reports [14].

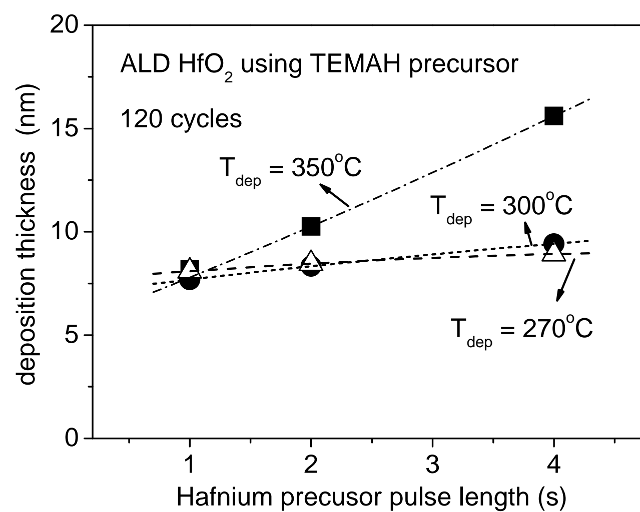

Fig. 2.4 The self-limiting characteristic of HfO_2 deposited using $Hf(NEtMe)_4$ precursor under various deposition temperatures. The deposition temperature is suggested to be below 350ºC.

B. Investigation of ALD La_2O_3 and ALD $HfLaO_x$

A suitable deposition temperature for La_2O_3 was also investigated. As shown in Fig. 2.5, when the deposition temperature varied from 280ºC to 480°C, the deposition rate of La_2O_3 decreased as temperature increased, then settled to a certain value when temperatures was above 360ºC. The flat deposition rate implies that the

thermal deposition does not occur even the temperature is further raised to 480ºC. It is worth to note that the thermal decomposition temperature of La(iPrCp)$_3$ is around 300ºC according to TGA data sheet from the precursor supplier [25]. This is not consistent with our experiment results of thermal stability up to 480ºC. Similar result of high thermal stability was also reported by another group [24]. More important, the deposition rate of La_2O_3, even at the temperature of 280ºC, was much lower than that of other ALD dielectrics (such as HfO_2). As shown in Fig. 2.6, the deposition rate of HfO_2 is 5 times greater than that of La_2O_3.

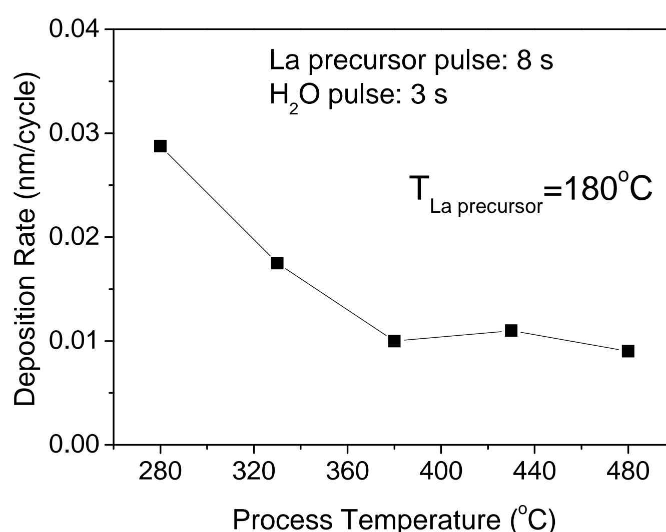

Fig. 2.5 The deposition rate of La_2O_3 as a function of deposition temperature. A 100 cycles of deposition was performed during evaluation. It shows that the deposition temperature for La_2O_3 can be raised up to 480ºC.

However, when the hafnium precursor, Hf(NEtMe)$_4$, or aluminum precursor, TMA, was used together with lanthanum precursor, La(iPrCp)$_3$, to co-deposit $HfLaO_x$ or $LaAlO_x$, respectively, significantly different deposition behaviors were observed. Figure 2.6 compares the film thickness as a function of deposition cycles for La_2O_3,

HfO_2 and $HfLaO_x$. The deposition temperatures were all set to 300ºC. For fair comparison, all deposition parameters remained unchanged. The recipes configuration was shown in Table 2.1. Here, one cycle of $HfLaO_x$ consists of one cycle of HfO_2 and one cycle of La_2O_3, that is two pulses of metal precursor (Hf pulse and La pulse) and two pulses of H_2O. The film thickness was measured by ellipsometer and confirmed by high resolution transmission electron microscopy (HRTEM).

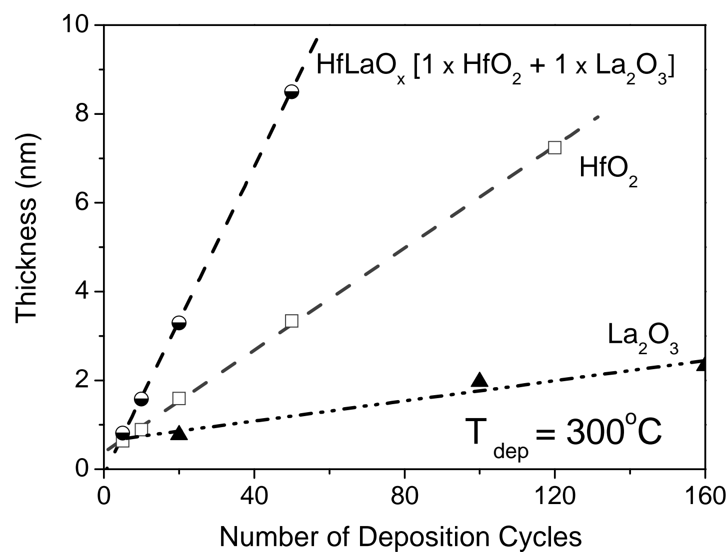

Fig. 2.6 Thicknesses of La_2O_3, HfO_2 and $HfLaO_x$ as a function of deposition cycles. The pulse length of La precursor, H_2O, Hf precursor and H_2O was set to 8 s, 3 s, 1 s and 0.5 s, respectively. The deposition rate of $HfLaO_x$ is much greater than the sum of the individual deposition rate of HfO_2 and La_2O_3, implying a reaction improvement.

	Hf pulse	purge	H_2O pulse	purge	La pulse	purge	H_2O pulse	purge
HfO_2	1	3	0.5	3	-	-	-	-
La_2O_3	-	-	-	-	8	8	3	5
$HfLaO_x$	1	3	0.5	3	8	8	3	5

Table 2.1 Recipes configuration of HfO_2, La_2O_3 and $HfLaO_x$. The unit of the number in the table is “second”.

As shown in Fig. 2.6, the film thickness of HfO_2 and $HfLaO_x$ are strictly proportional to the number of the deposition cycles, which is a typical characteristic of ALD process. And there was no incubation time for both HfO_2 and $HfLaO_x$. The deposition rate of HfO_2, La_2O_3 and $HfLaO_x$ was calculated to be around 0.6 Å, 0.15 Å and 1.4 Å per cycle, respectively. Among them, the deposition rate of La_2O_3 estimated by linear fitting may have some error because the deposited films were extremely thin. It is clear that the deposition rate of $HfLaO_x$ is much greater than the sum of the individual deposition rate of HfO_2 and La_2O_3, which means that one or both of the deposition rates increased in the co-deposition. Furthermore, XPS analysis showed that the atomic ratio of La / (La + Hf) in $HfLaO_x$ film was 0.81, which indicates that it is the deposition rate of La_2O_3 that is greatly enhanced.

C. Mechanism Investigation for Deposition Rate Enhancement

Further experiments were conducted to analyze the possible mechanisms behind this enhancement. First, the role of nucleation in ALD of La_2O_3 and $HfLaO_x$ was investigated. A few nanometer-thick seed layers of HfO_2, Al_2O_3, Si, Si_3N_4 and SiO_2 were deposited on silicon substrate, respectively, prior to La_2O_3 and $HfLaO_x$ depositions. After La_2O_3 and $HfLaO_x$ deposition, their physical thickness was measured using ellipsometer.

As summarized in Fig. 2.7, all the deposition rate of La_2O_3 on varied substrate surface remained constantly low, which was around 0.15 Å per cycle. In contrast, the deposition rate of $HfLaO_x$ was much higher (approximately 1.4 Å per cycle) on these varied substrates. Thus, the varied seed layers almost have no impact on deposition rate of La_2O_3 and $HfLaO_x$. Therefore, we deduce that the deposition rate enhancement in $HfLaO_x$ deposition is not due to the enhanced nucleation.

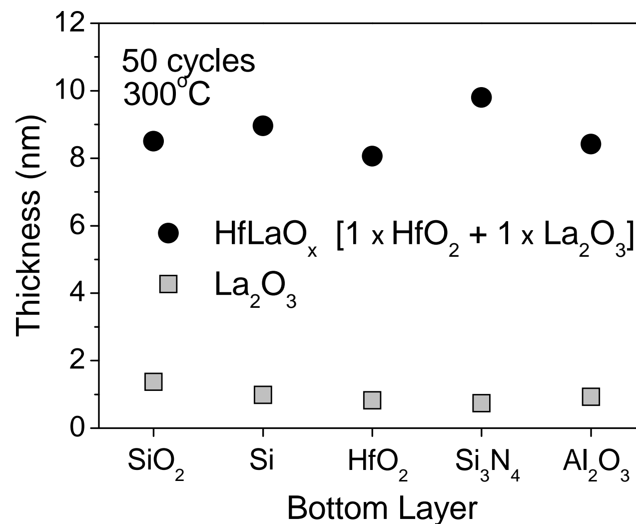

Fig. 2.7 Comparison of the deposition rate between $HfLaO_x$ and La_2O_3 on different seed layers. It shows that the deposition rate enhancement of $HfLaO_x$ is not related to the contacting substrate materials.

The deposition parameters of La_2O_3 were then further investigated. As shown in Fig. 2.8, the deposition rate of La_2O_3 increased dramatically as the increase of La precursor's pulse length and there was no trend of saturation. This is much different from the typical self-limiting graph mentioned in Fig. 2.2. Obviously, it is not ALD self-limiting behavior. Besides, it is interesting to notice that the deposition rates at 400ºC deposition temperature was lower than that at 300ºC deposition temperature for

the entire range of La pulse length. It implies that the increase of deposition rate with the increase of La pulse length is not due to the thermal decomposition, because the thermal decomposition would be more severe at higher temperature. In addition, poor thickness uniformity was observed when La pulse length was set to 15 sec. The thickness was 9.17 nm and 6.12 nm at the center and the edge, respectively, of a 6-inch wafer at 300°C deposition temperature.

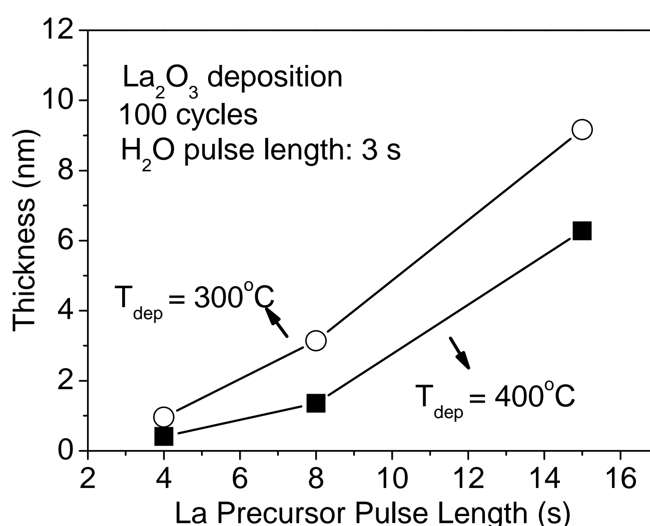

Fig. 2.8 The deposition rate of La_2O_3 as a function of La precursor pulse length at 300ºC and 400ºC, respectively. No self-limiting behavior was observed.

Figure 2.9 depicts that the deposition rate decreased as an increase of H_2O pulse length. This is again different from the usual behavior of the ALD process, which gives us a clue for finding out the mechanism of deposition rate enhancement for $HfLaO_x$. It is generally believed that longer H_2O pulse length generates more numbers of La-OH bonds on the surface. So it is postulated that more numbers of X-OH bonds on the surface would result in higher deposition rate in usual ALD

processes. However, it may have a different situation in La_2O_3 deposition. The formation of La-OH on the surface does not seem to promote La_2O_3 deposition, instead, inhibits further reaction.

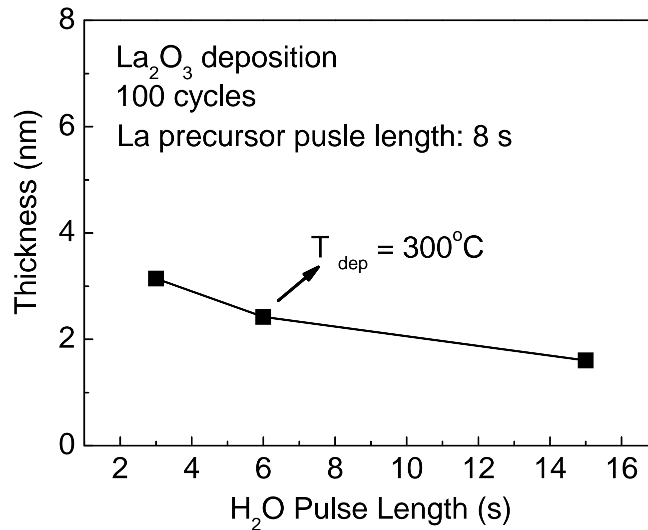

Fig. 2.9 The deposition rate of La_2O_3 as a function of H_2O pulse length, the deposition temperature was set to 300ºC. It is abnormal that deposition rate decreased with the increase of H_2O pulse length.

It is well known that La_2O_3 easily reacts with ambient moisture and turns to lanthanum hydroxide, $La(OH)_3$, which is chemically stable [17]. It is speculated that during the H_2O pulse, the La-OH forms on the surface and turns to $La(OH)_3$. This transition will be more prominent when the H_2O pulse length is longer. It is believed that the formation of $La(OH)_3$ on the surface will hinder further reaction with La precursor and thus results in decrease of deposition rate.

However, it is a different situation in $HfLaO_x$ alternate deposition. When the La precursor is flowing into ALD chamber, the wafer surface has been covered by

Hf-OH bonds. A reaction will definitely occur between the La precursor and Hf-OH. Thus, lanthanum can be successfully deposited on the surface. Besides, the presence of Hf element on the wafer surface helps to reduce the formation of $La(OH)_3$, which results in more dangling La-OH on the wafer surface. Similarly, when the Hf precursor is introduced into ALD chamber, it will react with the dangling La-OH on the surface. It is worth to note that the deposition rate of HfO_2 is still affected. In the case of HfLaO with 20% Hf/(Hf + La) atomic ratio, the deposition rate is 1.4 Å/cycle. Then, the deposition rate of hafnium oxide in 20% Hf-HfLaO deposition is calculated to be around 0.28 Å/cycle, which is much lower than that of pure HfO_2 deposition (0.6 Å/cycle). This difference is believed to be caused by the presence of $La(OH)_3$. Again, the reaction between $La(OH)_3$ and hafnium precursor will be hindered upon the formation of $La(OH)_3$ on the surface.

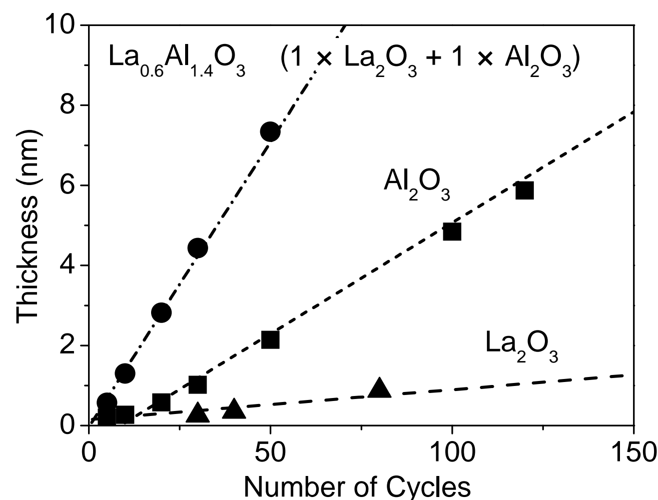

Fig. 2.10 Thicknesses of La_2O_3, Al_2O_3 and $LaAlO_x$ as a function of deposition cycles. The pulse length of La precursor, H_2O, Al precursor and H_2O was set to 8 s, 3 s, 0.2 s and 0.5 s, respectively. The deposition rate enhancement of $LaAlO_x$ was also observed.

Moreover, similar behavior of enhanced deposition rate was also observed in ALD $LaAlO_x$ upon the introduction of aluminum precursor (Trimethylaluminum, TMA). As shown in Fig. 2.10, similarly to $HfLaO_x$, under the same process conditions, the deposition rate of $LaAlO_x$ was also much higher than the sum of deposition rates of Al_2O_3 and La_2O_3. Besides, the film thicknesses of HfO_2 and $HfLaO_x$ were strictly proportional to the number of the deposition cycles. In addition, an incubation period at the beginning of ALD Al_2O_3 deposition was observed, which was also reported by other groups [26]. In contrast, there was almost no incubation period for ALD $LaAlO_x$ deposition.

D. Self-limiting Characteristic of $HfLaO_x$ and $LaAlO_x$

The self-limiting behavior of $HfLaO_x$ and $LaAlO_x$ were investigated. During the investigation, only the pulse lengths of La precursor and its immediate H_2O were varied; all other parameters, including hafnium precursor or aluminum precursor pulse length and their adjacent H_2O pulse length remained unchanged.

As shown in Fig. 2.11, when pulse lengths La precursor and H_2O were increased, the deposition rates of $HfLaO_x$ tended to be flat, indicating a self-limiting characteristic. And higher Hf:La pulsing ratios resulted in better self-limiting behavior. Besides, different composition ratios between Hf and La in $HfLaO_x$ could be obtained by controlling different Hf:La pulsing ratios. The atomic ratio of La/(La + Hf) was around 43% and 29% for the Hf:La pulsing ratio of 2:1 and 3:1, respectively. In addition, higher Hf:La pulse ratio resulted in better uniformity. The thickness

uniformity of 6-nm $HfLaO_x$ film with 29% La was 5.8% over 6 inch wafers, which was comparable to that of 6-nm HfO_2 film (~ 5.2%).

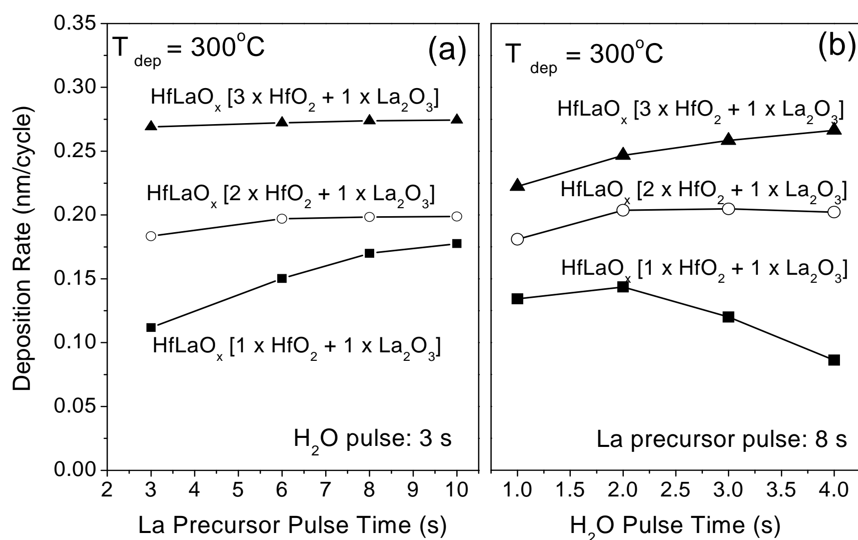

Fig. 2.11 Self-limiting characteristics of the $HfLaO_x$ films as a function of (a) La precursor pulse length and (b) H_2O pulse length. It was found that higher Hf:La pulsing ratio led to better self-limiting behavior.

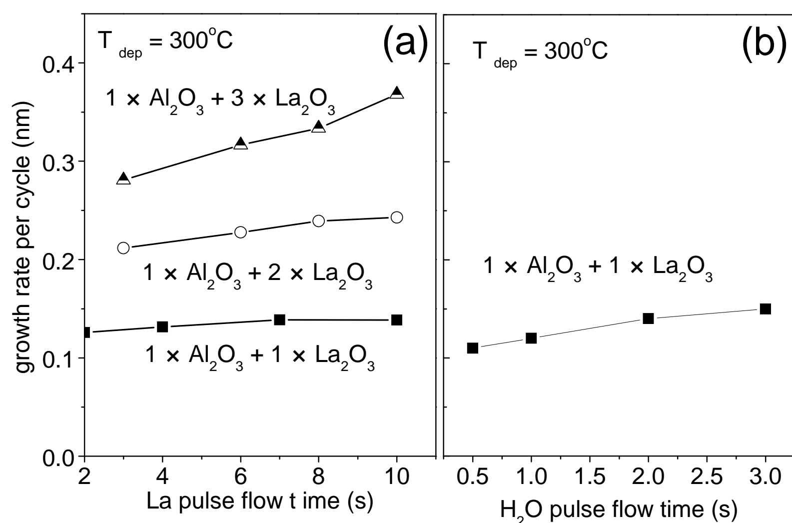

Fig. 2.12 Self-limiting characteristics of $LaAlO_x$ as a function of (a) La precursor pulse length and (b) H_2O pulse length. Higher number of Al:La pulsing ratio led to better self-limiting behavior.

Figure 2.12 shows the self-limiting characteristic of $LaAlO_x$. Similar to $HfLaO_x$, higher Al:La pulsing ratio resulted in better self-limiting behavior, as well as the film uniformity. The atomic ratio of La/(La + Al) was around 19%, 42% and 56% for the Al:La pulsing ratio of 1:1, 2:1 and 3:1, respectively.

In summary, upon the introduction of the hafnium precursor or aluminum precursor, the ALD process of La_2O_3 was significantly improved in terms of deposition rate, uniformity and self-limiting characteristic. By varying the La:Hf pulse ratio, the La concentration in $HfLaO_x$ and $LaAlO_x$ can be precisely controlled. Better uniformity and better self-limiting characteristics can also be achieved for $HfLaO_x$ and $LaAlO_x$ when Al or Hf percentage is high. In addition, except Al_2O_3 deposition, all ALD processes including HfO_2, $HfLaO_x$ and $LaAlO_x$ did not have the incubation time at the initial deposition stage.

2.5 Characterization of Deposited Film

There is a big concern about carbon impurity as for the ALD films deposited using metal-organic precursors. In order to get a more precise estimation of carbon impurity, $HfLaO_x$ film was analyzed using the TOF-SIMS (time of flight - secondary ion mass spectrometry) method. Because SIMS analysis is sensitive to matrix effects and there is no reference data for carbon impurity in metal oxides matrices, it is difficult to directly calculate the atomic percentage using the SIMS method [19]. To overcome this issue, a capping layer of ALD Al_2O_3 was deposited on top of the

$HfLaO_x$ at 300°C. The carbon impurity level of ALD Al_2O_3 deposited using TMA and water at 300 °C is known to be less than 0.2 at.%, which was detected by TOF-ERDA (time of flight-elastic recoil detection analysis) [6]. Thus, carbon impurity in $HfLaO_x$ can be estimated when using Al_2O_3 as a reference. As shown in Fig. 2.13, the carbon curve shows relatively low intensity at the bulk of the films but high intensity at the interface. This high intensity carbon impurity at interface is believed to be induced from the air when the samples were exposed to atmosphere. The intensity of the carbon curve in $HfLaO_x$ bulk film is almost 4 times higher than that in Al_2O_3 bulk film. Thus, the carbon percentage in 30% La-HfLaO was estimated to be less than 0.8 at.%.

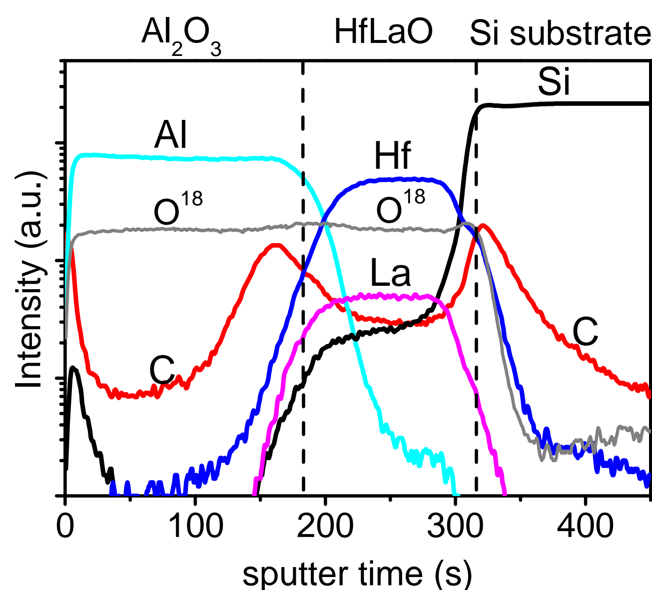

Fig. 2.13 The depth profile measured by the TOF-SIMS analysis for ALD Al_2O_3 / $HfLaO_x$ gate stack. All the curves have been normalized by the intensity of Gallium where Gallium was used as the primary ion source. The parallel lines between Hf and La elements indicated a uniform distribution in vertical direction. The carbon impurity and silicon impurity in $HfLaO_x$ were detected.

In addition, $HfLaO_x$ also exhibited a much higher silicon impurity than Al_2O_3. However, the source of these impurities in $HfLaO_x$ could not be determined thus far. In order to investigate the origin of carbon and silicon impurities, $HfLaO_x$ film capped with HfO_2 was fabricated for SIMS analysis, too. As shown in Fig. 2.14, $HfLaO_x$ showed a lower intensity of carbon impurity but higher intensity of silicon impurity than HfO_2, respectively. This indicates that the carbon impurity and silicon impurity possibly originated from the hafnium precursor and the La precursor, respectively. The carbon impurity in HfO_2 was estimated to be around 1.8 at.%. Silicon impurity in $HfLaO_x$ film is speculated to be introduced during the synthesis of La precursor because the La precursor source of $La(iPrCp)_3$ does not contain silicon element.

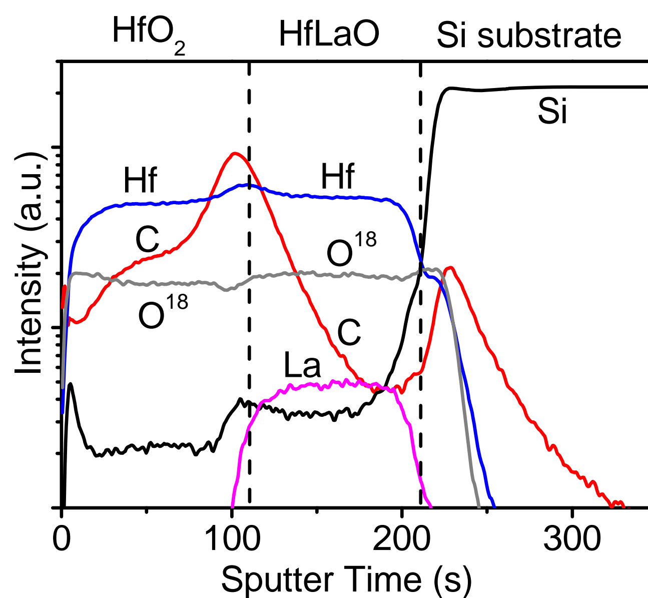

Fig. 2.14 The depth profile measured by the TOF-SIMS method for ALD HfO_2 / $HfLaO_x$ gate stack. All the curves have been normalized with the intensity of Gallium. The carbon impurity and silicon impurity in $HfLaO_x$ films is lower and higher than that of in HfO_2, respectively.

In addition, both Fig. 2.13 and Fig. 2.14 exhibit nearly flat intensity curves for Hf and La elements in depth profile from the top surface to the bottom interface. The constant composition ratio between Hf and La elements implies a uniform distribution of elements throughout the deposited film in the vertical direction.

The high-resolution transmission electron microscopy (HRTEM) was performed for an as-deposited $HfLaO_x$ film. As shown in Fig. 2.5, the as-deposited $HfLaO_x$ shows an amorphous structure and a flat top surface. Besides, a sharp interface transaction between $HfLaO_x$ and silicon substrate was also observed.

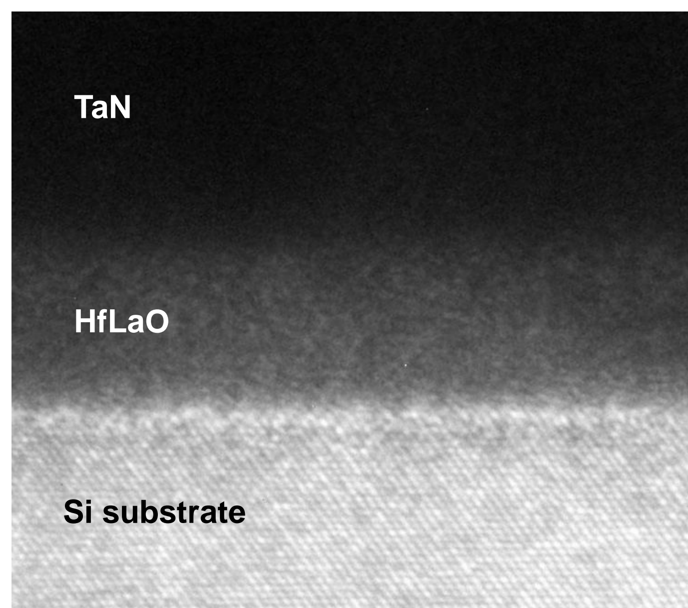

Fig. 2.15 TEM image of ALD $HfLaO_x$ film growth at 300°C. An amorphous film with smooth surface was observed.

2.6 Summary

Deposition process and film characteristics of ALD $HfLaO_x$ and $LaAlO_x$ dielectrics have been described. Significant enhancement of growth rate of La_2O_3 was observed when Hf precursor or Al precursor was introduced to form $HfLaO_x$ or $LaAlO_x$. A reason for this growth rate enhancement has been proposed. The self-limiting characteristic and film uniformity of $HfLaO_x$ and $LaAlO_x$ was found to be dependent on the Hf:La and Al:La pulse ratio, respectively. In addition, a uniform vertical distribution of elements together with a smooth and flat top surface was observed. Low carbon impurity was achieved and the carbon impurity was found to originate mainly from the Hf precursor. The silicon impurity, probably generated during the La precursor synthesis, was also detected inside the $HfLaO_x$ film.

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Chapter 3 Characteristics of Lanthanum-incorporated Dielectrics

3.1 Introduction

In the previous chapter, the lanthanum-incorporated dielectrics ($HfLaO_x$ and $LaAlO_x$) have been deposited successfully using the ALD method and exhibited good uniformity and low carbon impurity. The characteristics of ALD films have also been briefly explored. In this chapter, the physical and electrical characteristics of $HfLaO_x$ and $LaAlO_x$ will be further explored, including energy band structure, crystal structure, crystallization temperature, hygroscopic property, dielectric constant, as well as leakage current. With regards to electrical characteristics of $HfLaO_x$, this chapter will focus on 8% La-$HfLaO_x$ that can provide the highest permittivity (~ 38). The mechanism of such permittivity improvement will be investigated, as well as the effect of annealing temperatures. The optimum temperature window for achieving highest permittivity will be also suggested. Besides, the leakage currents of amorphous films and crystal films will be compared. In respect to $LaAlO_x$, the leakage currents of films deposited at different deposition temperatures will be firstly compared to find out the optimum deposition temperature. Afterwards, the crystallization temperature and phase separation of $LaAlO_x$ will also be investigated.

3.2 Experiments

A. Introduction of Process Flow and Characterization Tools

Using $HfLaO_x$ and $LaAlO_x$ as gate dielectrics, MOS devices were fabricated on p-type (100) Si substrates. First, field oxide with 400 nm was thermally grown in furnace. Subsequently, the field oxide was patterned and etched to open the active areas for gate stack growth. After a standard pre-gate cleaning process, ALD high-κ dielectrics ($HfLaO_x$ and $LaAlO_x$) were deposited. As discussed in the previous chapter, the deposition temperatures for HfO_2, Al_2O_3 and La_2O_3 range from 270ºC to 300ºC, from 270ºC to 450ºC and from 270º to 480ºC, respectively. In this experiment, the deposition temperature for $HfLaO_x$ deposition was fixed to 300ºC. In contrast, the deposition temperature for $LaAlO_x$ deposition varied from 270ºC to 450ºC. The optimum deposition temperature will be investigated in the later part of this chapter. After high-κ dielectric deposition, ex-situ post deposition anneal (PDA) was performed at 600°C for 30 s in N_2 ambient in order to improve the film quality. Subsequently, TaN was deposited as gate electrode by reactive sputtering from a Ta target in N_2 ambient. After gate stack patterning, rapid thermal annealing (RTA) treatment ranged from 600°C to 1000°C was performed in N_2 ambient for thermal stability evaluation. Finally, all samples received forming gas annealing (FGA) at 420°C for 30 min in N_2/H_2 ambient in Furnace.

In order to avoid any error in κ value estimation due to a low-κ interfacial

layer formation in MOS structure, metal-insulator-metal (MIM) capacitors were fabricated. On top of 400 nm field oxide, TaN was deposited as bottom and top electrodes by reactive sputtering from a Ta target in N_2 ambient. Between the two electrodes, ALD $HfLaO_x$ and $LaAlO_x$ films were deposited. After patterning, devices were treated with rapid thermal anneal (RTA) at various temperatures for 30 s in N_2 ambient under one atmospheric pressure, followed by a forming gas anneal at 420ºC for 30 min in N_2/H_2 ambient.

In this experiment, devices with an area of 0.01 × 0.01 cm^2 were used for current and capacitance determination, as well as κ value extraction. Current-voltage (*I*-*V*) and capacitance- voltage (*C*-*V*) was measured using a HP 4156A semiconductor parameter analyzer and HP 4284A precision LCR meter at a frequency of 100 kHz, respectively. A *C*-*V* simulator software tool written by UC Berkeley was used to extract the equivalent oxide thickness (EOT) and flat-band voltage (V_{fb}) of a MOS capacitor. During the EOT extraction, quantum mechanical correction was applied. In addition, the physical thicknesses of films were measured using SENTECH's spectroscopic ellipsometer SE800 and verified by high resolution transmission electron microscopic (HRTEM). X-ray photoelectron spectroscopy (XPS) was used to determine the energy band structure and the atomic percentage. Crystal structural analysis was performed with X-ray diffraction (XRD).

B. Methods for Electrical Performance Comparison

During the electrical performance evaluation, two methods are used for the

electrical performance comparison usually. The first one which is widely used is to compare the leakage current density at a defined voltage (J_g-EOT method). For illustration, $LaAlO_x$ with two different physical thicknesses in MIM structure was selected together with another sample of $HfLaO_x$, as shown in Fig. 3.1. The EOT of 10.6-nm $LaAlO_x$, 6.5-nm $LaAlO_x$ and 12.5-nm $HfLaO_x$ was extracted to be 2.13 nm, 1.33 nm and 1.6 nm, respectively. Figure 3.2(a) compares the current density at a voltage of - 3 V. The dashed line crossing two points of $LaAlO_x$ implies that two samples have the same performance. The fact that the point of $HfLaO_x$ locates below the dashed line indicates that $HfLaO_x$ film has better *I-V* performance than the $LaAlO_x$ films. In this J_g-EOT method, the defined voltage needs to be within a region which has the same dominant mechanism of leakage current for all the dielectrics to make comparisons meaningful [1]. For instance, the allowed voltage, marked as the shadowed area in Fig. 3.1, ranges from 2.5 V to 3.6 V. Another disadvantage of this method is that it requires at least two points from a certain dielectric with different EOTs. The other method is called the EOT normalization method. As shown in Fig. 3.2(b), the leakage current density is plotted against the voltage divided by EOT. It is obvious that the leakage current of $HfLaO_x$ is lower than that of $LaAlO_x$.

Compared with the J_g-EOT method, the EOT normalization method does not require comparison to be limited to a common voltage region, thus enabling the comparison among the dielectrics with large physical thickness variations. Furthermore, as evidence of leakage currents overlapping for $LaAlO_x$, one curve of leakage current is enough for comparison, therefore reducing the split samples.

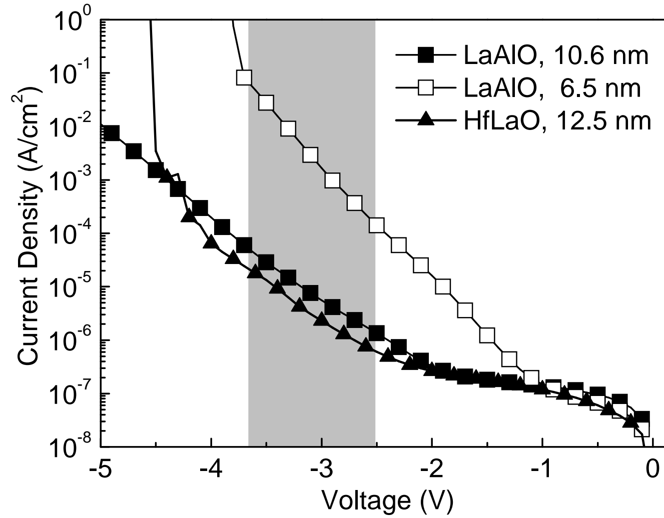

Fig. 3.1 The leakage current density as a function of voltage (*I-V*) for $LaAlO_x$ and $HfLaO_x$ films.

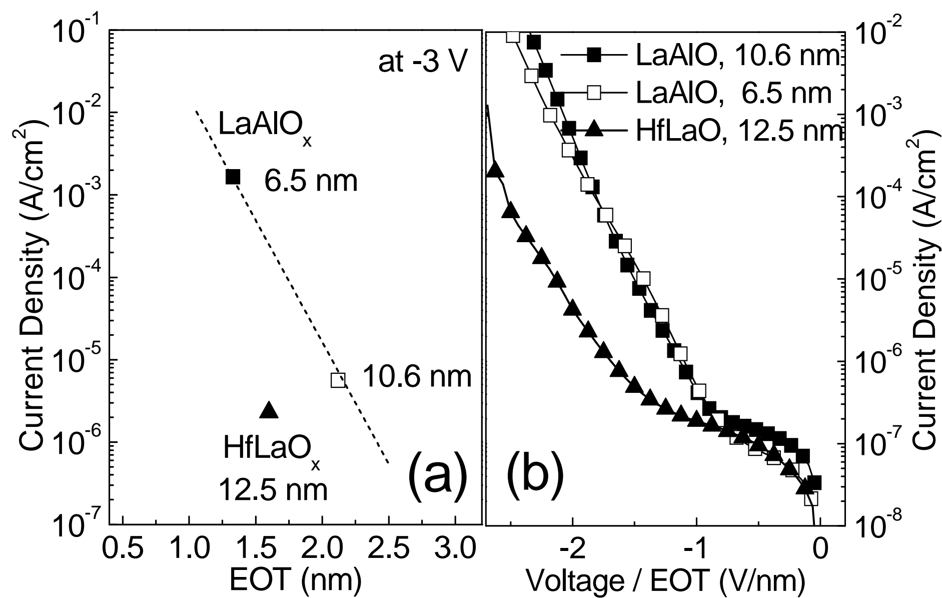

Fig. 3.2 A comparison of leakage current between $LaAlO_x$ and $HfLaO_x$ using (a) the J_g-EOT method and (b) the EOT normalization method. The EOT normalization method has the advantages of less split requirement for $LaAlO_x$ and more visual comparison among the dielectrics with large EOT variation. But the x-axis of the EOT normalization method does not have any physical meaning.

The disadvantage of the EOT normalization method is that the x-axis does not

have any physical meaning. In summary, J_g-EOT method and EOT normalization method can deliver the same information and both are used in this study.

3.3 Physical Characteristics of $HfLaO_x$ and $LaAlO_x$ Films

The material properties of $HfLaO_x$ and $LaAlO_x$ were investigated first, including their energy band structures, crystal structures, crystallization temperatures, and hygroscopic properties, etc.

A. Hygroscopic Property

The hygroscopic property of lanthanum-incorporated dielectrics was investigated using the XPS method.

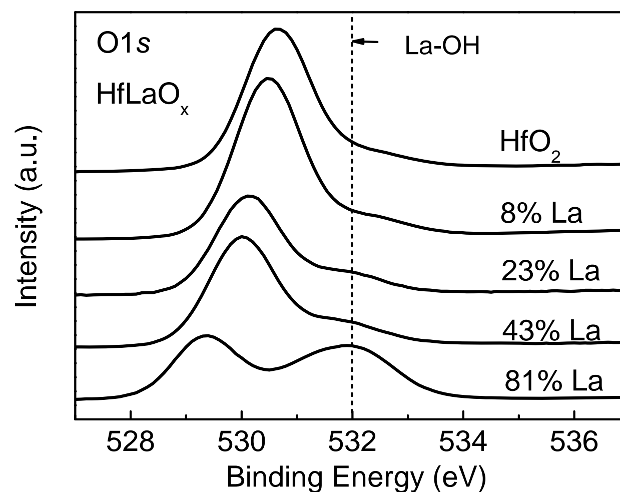

Fig. 3.3 The XPS spectra of O 1*s* core level of $HfLaO_x$ films with various La percentages. The La-OH bond is more obvious for the films with higher La percentage.

Figure 3.3 compiles the XPS O 1*s* core level spectrum taken from the $HfLaO_x$

films with different La percentages. The atomic ratios of La/(Hf + La) for 4 samples were 0% (pure HfO_2), 29%, 43% and 81%, respectively. Pure La_2O_3 samples were not prepared due to their extremely low deposition rate, as mentioned in the previous chapter. $HfLaO_x$ films were deposited on HF-last cleaned p-type Si (100) wafers. All spectra were calibrated against the adventitious carbon peak (C 1s: 285.0 eV).

In Fig. 3.3, the peak of O 1*s* spectra located at ~ 530.6 eV is attributed to the Hf-O bond [2]. As La percentage increases, O 1*s* core peak shifts toward a lower binding energy, which approaches the reported values of 529.1 eV for pure La_2O_3 films. The samples with high La percentage also show another additional peak locating at 531.8 eV. This additional peak corresponds to the La-OH bond [3-5]. The intensity of La-OH bonds becomes stronger as La percentage increases, indicating that higher La percentage in $HfLaO_x$ leads to a more serious hygroscopic issue.

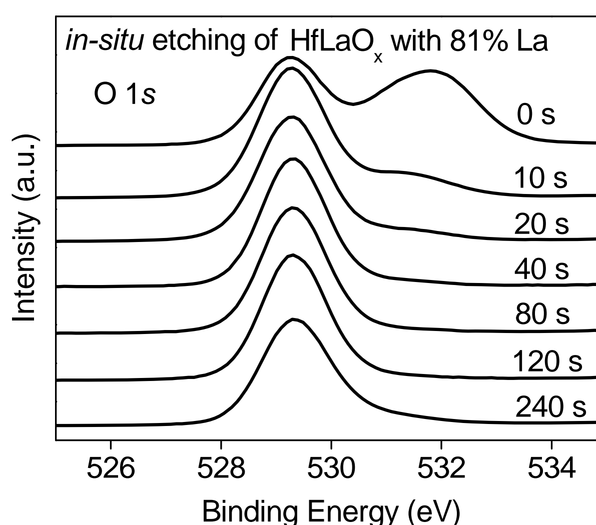

Fig. 3.4 The XPS spectra of O 1*s* core level for 81% La-$HfLaO_x$ with Ar *in-situ* etching. After 20 s *in-situ* etching, the La-OH bond cannot be detected.

The location of the absorbed moisture in $HfLaO_x$ films was also investigated. During the XPS measurement, the sample of 81% La-$HfLaO_x$ was etched *in-situ* using Ar plasma. As shown in Fig. 3.4 of the O 1*s* core level spectra, the intensity of La-OH peaks declines significantly after 10 s Ar *in-situ* etching and completely disappears after another 30 s etching. This indicates that the absorption of moisture mainly happens at the outer surface of the $HfLaO_x$ films.

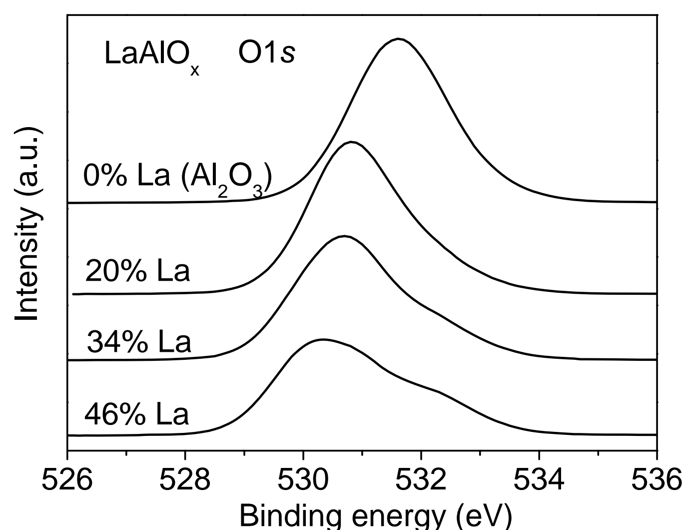

Fig. 3.5 The XPS spectra of O 1*s* core level of $LaAlO_x$ films. The La-OH bond located at 531.6 eV is more obvious for the films with higher La percentage.

$LaAlO_x$ films show similar hygroscopic property. Figure 3.5 compiles the spectra of O 1*s* core level for $LaAlO_x$ with 4 different La percentages. The La percentage in $LaAlO_x$ was 0% (Al_2O_3), 20%, 34% and 46%, respectively. As shown in Fig. 3.5, the spectra peak of O 1*s* located at ~ 531.6 eV is attributed to Al-O bonds [2]. As La concentration increases, O 1*s* core peak shifts toward lower binding energy. As in the case of $HfLaO_x$, an additional peak is shown up at 531.8 eV corresponding to

the La-OH bond which becomes more severe as the La percentage increases, implying stronger hygroscopic property for $LaAlO_x$ films with higher La percentages

B. Energy Band Structure

During the XPS measurement, when the photo-excited electrons are passing through a dielectric material, they experience inelastic energy losses. The inelastic energy loss is caused by plasmon or band-to-band excitation [6]. The energy loss caused by plasmon usually is observed at the lower kinetic energy region. This region is located at least 15 eV away from the core level peak or even more. Within the window of 15 eV, the spectra loss corresponds to band-to-band excitation. The onset of the spectra loss is the beginning of the band-to-band excitation.

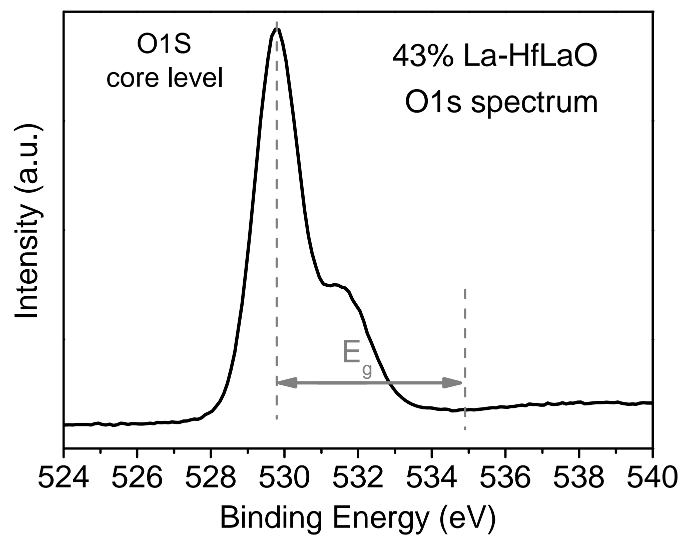

Fig. 3.6 An illustration of energy band gap extraction in O 1*s* spectrum. The energy band gap (E_g) refers to the difference between the O 1s core level and the onset of spectra loss.

The energy difference between the onset of the loss spectra and the core level

peak is defined as the energy band gap [6]. Therefore, the energy band gap (E_g) of dielectric materials can be determined using XPS method [6-8]. As illustrated in Fig. 3.6 of O 1*s* spectrum of 43% La-HfLaO, the core level peak of O 1*s* is located at 529.7 eV and the onset of the loss spectra is found to be at 535.0 eV. Thus, the energy band gap of 43% La-$HfLaO_x$ is calculated to be around 5.3 eV. The onset of the loss spectrum is actually determined in a magnified scale, as shown in Fig. 3.7.

In Fig. 3.7, the onset of the loss spectrum is the intercept of the background signal line and the linear curve derived from maximum spectral slope fitting. The peak value of O 1*s* core-level is set to zero in the new magnified graph. Thus, the value of intercept point corresponds to the value of energy band gap. As shown in Fig. 3.7, when La percentage increases from 0 to 81%, the energy band gap of $HfLaO_x$ increases from 4.9 eV to 5.7 eV accordingly.

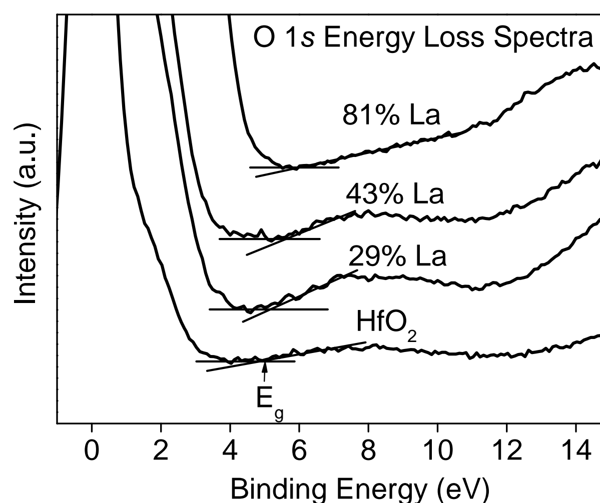

Fig. 3.7 O 1*s* energy-loss spectra for 15-nm $HfLaO_x$ films with different La percentages. The intercept points indicate the values of energy band gap (E_g). $HfLaO_x$ films with higher La percentage exhibit wider energy band gap.

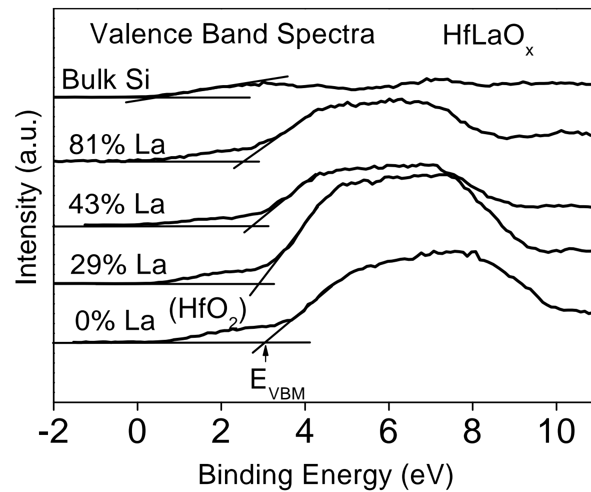

Fig. 3.8 The valence band spectra of bulk Si substrate and $HfLaO_x$ films (3-nm). $HfLaO_x$ films with higher La percentage shows smaller valence band offset over Si.

The valence band offset (ΔE_v) over Si can also be determined using the XPS method [2, 6, 8, 9]. In contrast to thick dielectric films (~ 15 nm) used for band gap determination, thin films of 3-nm-thick dielectrics were used for valence band edge determination. In this situation, the information from both thin films and silicon substrate can be obtained simultaneously during the XPS valence-band spectrum measurement [9]. By the deconvolution of the silicon contribution from the valence-band spectrum or by calculating the maximum energy (E_{VBM}), the valence band offset between silicon and thin film dielectric can be determined [2]. E_{VBM} can be extrapolated from the intersection point between the leading edge of the valence band spectrum and the baseline of the spectrum. After careful compensation of the charging effect, E_{VBM} of $HfLaO_x$ films and pure silicon substrate are shown in Fig. 3.8. The valence band offset is the difference between E_{VBM} of silicon and $HfLaO_x$. It is clear that the valence band offset decreases from 2.6 eV to 2.1 eV as La percentage increases from 0 to 81%.

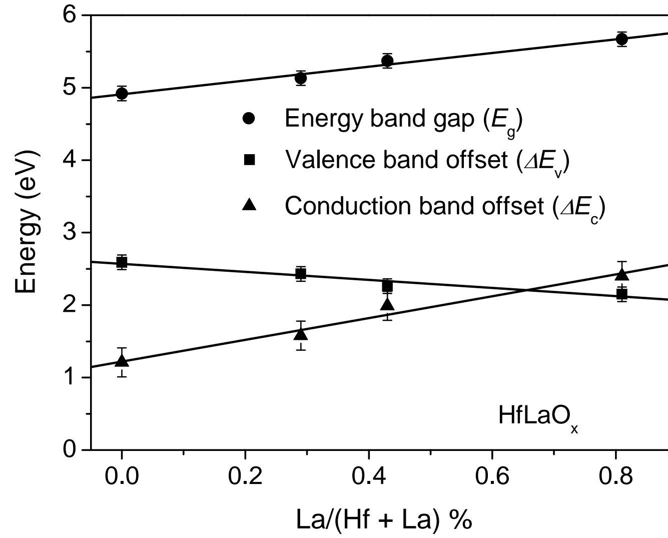

Fig. 3.9 A summary of energy band gap (E_g), valence band offset (ΔE_v) and conduction band offset (ΔE_c) of $HfLaO_x$ films as functions of La percentage. With incorporation of La into HfO_2, the E_g and ΔE_c are improved.

Using the results of energy band gap and valence band offset together with the silicon energy band gap of 1.12 eV, the conduction band offset (ΔE_c) of $HfLaO_x$ against silicon can be derived. The final results including the energy band gap (E_g), valence band offset (ΔE_v) and conduction band offset (ΔE_c) of $HfLaO_x$ as a function of La percentage are plotted together in Fig. 3.9. It clearly indicates that E_g, ΔE_c, and ΔE_v of $HfLaO_x$ changes almost linearly with the La percentage. Using the linear fitting, we can obtain the empirical relations as follows:

$$E_g = 4.9 + 0.9\beta \ (eV) \quad (1)$$

$$\Delta E_v = 2.6 - 0.5\beta \ (eV) \quad (2)$$

$$\Delta E_c = 1.2 + 1.5\beta \ (eV) \quad (3)$$

where β stands for atomic ratio of La/(Hf + La) in $HfLaO_x$. The relationship formulas tell us that $HfLaO_x$ provides higher conduction band offset and wider band gap as the

La percentage increases. When β is equal to 0.5, the values of E_g, ΔE_v and ΔE_c are 5.4 ± 0.1 eV, 2.3 ± 0.1 eV and 2.0 ± 0.2 eV, respectively. In above equations, it only considers system error from the XPS equipment. These values are consistent with the band structure of $Hf_2La_2O_7$, reported by Seguini *et al*, with E_g, ΔE_v and ΔE_c equal to 5.6 eV, 2.4 eV and 2.1 eV, respectively [10].

In addition, using the same methods, the energy band structure of 55% La-$LaAlO_x$ was also derived. The values of E_g, ΔE_v and ΔE_c are 6.5 ± 0.1 eV, 2.8 ± 0.1 eV and 2.6 ± 0.2 eV, respectively. These values are bigger than those of $HfLaO_x$.

C. Thermal Stability

The thermal stability of $HfLaO_x$ was investigated by using the XRD method.

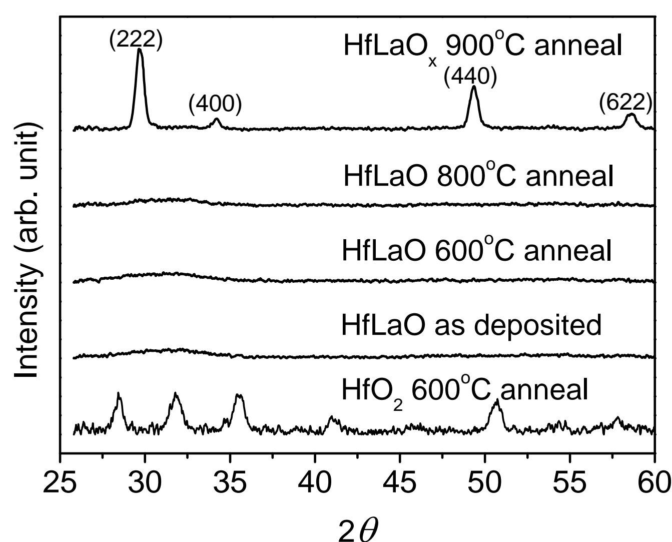

Fig. 3.10 The XRD spectra of 18-nm $HfLaO_x$ and HfO_2 films annealed at various temperatures. The atomic ratio of La/(La + Hf) was around 44%. The cubic phase spectra of $HfLaO_x$ (top curve) are observed that clearly distinguished it from the monoclinic phase of HfO_2 (bottom curve).

The ALD $HfLaO_x$ films with varying La percentage were deposited on top of 4000Å thermal oxide. Then these films were subjected to rapid thermal anneals (RTP) at different temperatures in a N_2 ambient for 30 sec. As shown in Fig. 3.10, the results show that 18-nm $HfLaO_x$ films remain amorphous up to 800ºC anneal and will crystallize to cubic-like structure after 900ºC anneal. This cubic-like structure is clearly distinguished from the monoclinic structure of HfO_2, as shown in the bottom of Fig. 3.10.

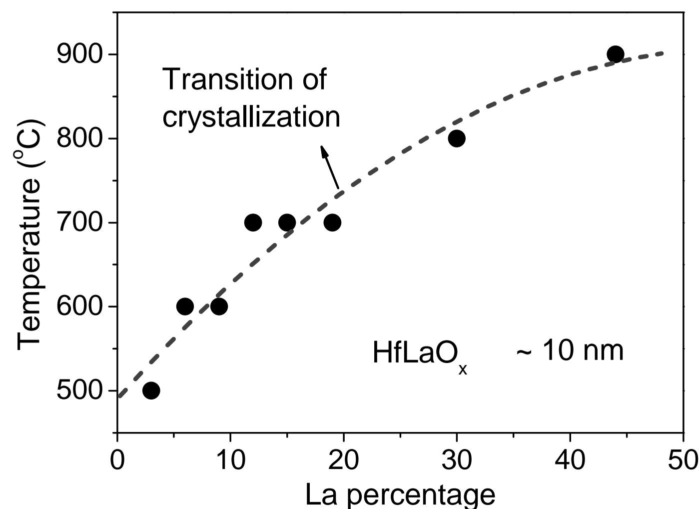

Fig. 3.11 The onset of the crystallization temperature as a function of La percentage for $HfLaO_x$ films. The $HfLaO_x$ films with higher La percentage exhibits higher crystallization temperature.

Furthermore, the transition of crystal structure from monoclinic to cubic-like for $HfLaO_x$ films was found to happen at 4% La doping condition. When La doping percentage in $HfLaO_x$ was greater than 4%, the peaks of cubic-like structure were clearly observed. Moreover, it was also found that the crystallization temperature varied with the La percentages. As shown in Fig. 3.11, when the La percentage

increases, the crystallization temperature increases.

Similar investigation of the thermal stability of 46% La-$LaAlO_x$ is shown in Fig. 3.12. It shows that $LaAlO_x$ remains amorphous after anneal at 900ºC. However, after anneal at 1050°C, the crystal peaks are observed. However, these crystal peaks are not consistent with the cubic-$LaAlO_3$ peaks, but are consistent with the monoclinic-La_2O_3 peaks. This implies that a phase separation may happen under this condition. Similar crystal peaks were also reported by Sivasubramani *et al* [11].

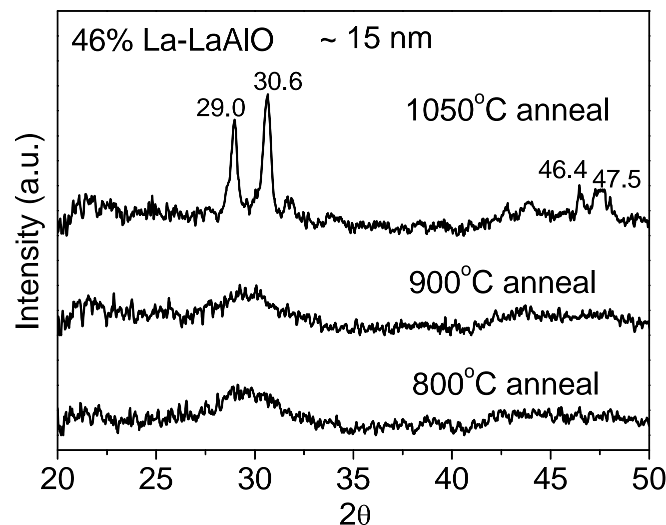

Fig. 3.12 The XRD spectra of $LaAlO_x$ films annealed at various temperatures. The spectra peaks of crystallized $LaAlO_x$ film cannot fit to cubic-$LaAlO_3$ peaks but to monoclinic- La_2O_3 peaks, indicating a phase separation.

3.4 Electrical Characteristics of $HfLaO_x$ Films

In order to check the basic electrical properties of $HfLaO_x$ films, metal-oxide-semiconductor (MOS) capacitor devices were prepared on p-type silicon substrate. Capacitive-voltage (*C-V*) cures were first measured. As shown in Fig. 3.13, the EOT

of as-deposited $HfLaO_x$ was measured to be 1.5 nm. After a 900ºC anneal, the EOT increased to 2.3 nm. The increase of EOT is attributed to low-κ dielectric formation at silicon interface. In addition, the *C-V* curves of both as-deposited and annealed samples exhibited sharp transition in the depletion region, indicating a high quality interface between the $HfLaO_x$ films and silicon substrate. Furthermore, both as-deposited and annealed samples had a flat band voltage (V_{fb}) of nearly -1 V. This large negative V_{fb} was also reported by Wang *et al* and was used to tune the effective work function of MOS gate stack [12]. This tuning capability is considered to be due to the oxygen-vacancy-related dipoles at the interface between $HfLaO_x$ and SiO_x thin films [13].

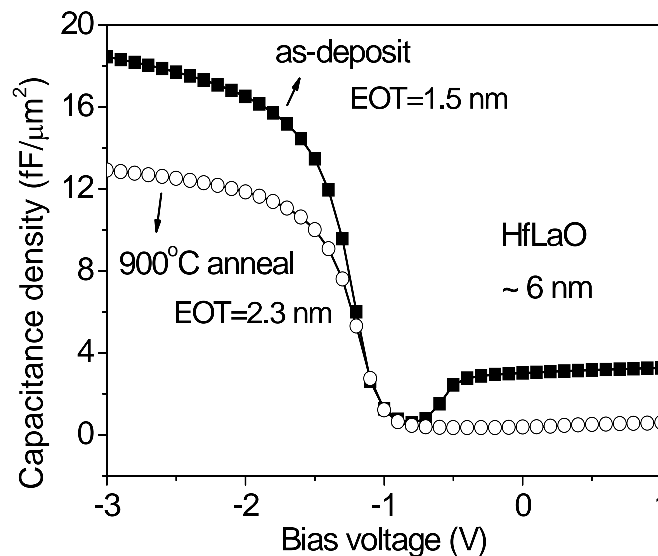

Fig. 3.13 The *C-V* characteristics of $HfLaO_x$ on p-type silicon substrate. A sharp transition at the depletion region is observed, implying a high quality interface.

The leakage current was evaluated in a MIM capacitor structure so as to minimize the disturbance from the presence of a low-κ interfacial layer. Both 18-nm

29% La-$HfLaO_x$ film and 18-nm HfO_2 (as control) film were deposited by ALD method. The EOT of $HfLaO_x$ and HfO_2 was calculated to be 3.07 nm and 4.11 nm, respectively. Even though the EOT value of $HfLaO_x$ is lower than that of HfO_2, the leakage current of $HfLaO_x$ is much lower than that of HfO_2 in both low and high electric fields after high temperature anneals, as shown in Fig. 3.14. As discussed earlier, $HfLaO_x$ films after anneal at 900ºC for 30 s will crystallize to a cubic-like structure. However, unlike HfO_2, the leakage current of $HfLaO_x$ showed almost no degradation after crystallization, even if annealed at 1050ºC for 10 s. This phenomenon of non-degradation after crystallization was also reported by Guha *et al* [14]. Furthermore, $HfLaO_x$ showed superior reliability characteristic. The breakdown field of crystallized $HfLaO_x$ film was much greater than that of crystallized HfO_2 film (4.2 MV/cm *vs.* 2.2 MV/cm).

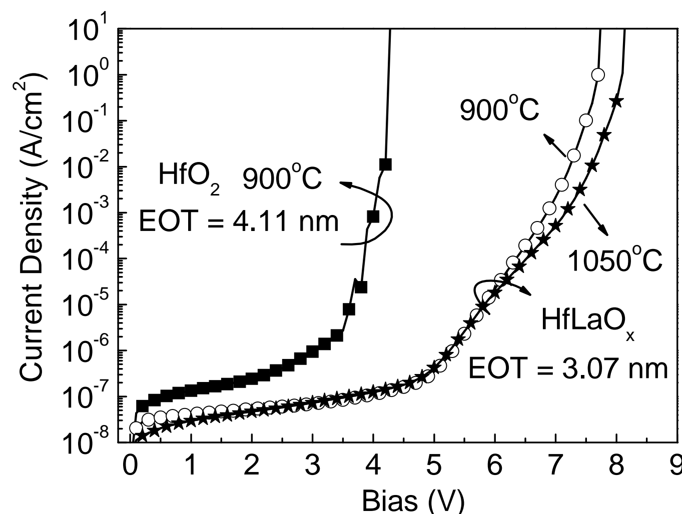

Fig. 3.14 Leakage current comparison between 29% La-$HfLaO_x$ films and HfO_2 film in MIM structures. The devices were annealed in a N_2 ambient at 900ºC for 30 sec or 1050ºC for 10 sec. The leakage currents of $HfLaO_x$ films did not exhibit any degradation after annealing at high temperatures.

In Fig. 3.14, the calculated κ value of $HfLaO_x$ film was greater than that of HfO_2 film (24 *vs.* 17). Furthermore, when the La percentage in $HfLaO_x$ films was varied, it was found that even higher κ values could be achieved. Fig. 3.15 compares the κ values of $HfLaO_x$ films with different La percentages before and after the crystallization. The annealing temperature here was 500ºC for 4% and 6% La samples, 600ºC for 8% and 12% La samples, and 700ºC for 16% and 22% La samples, respectively. Regardless of La percentages, the κ values of amorphous $HfLaO_x$ (as-deposited) were all around 23. In contrast, after crystallization, the κ values of $HfLaO_x$ could be as high as 38 when La percentage was around 8%. The dramatic increase of κ values after crystallization is believed to be due to the formation of cubic-like crystal phases.

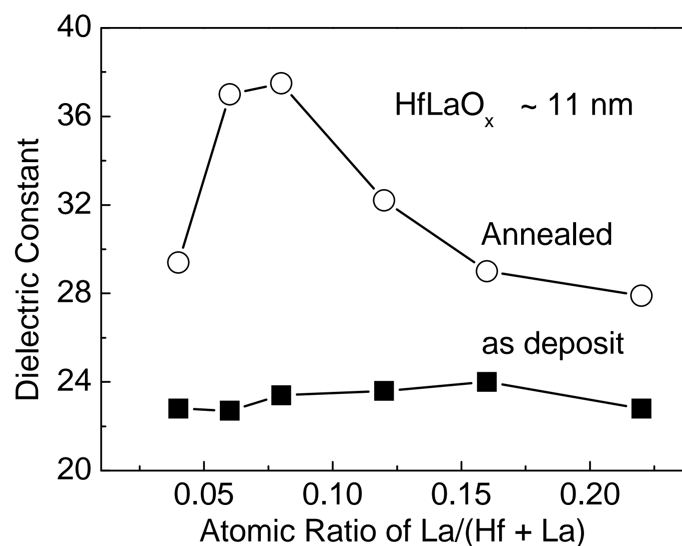

Fig. 3.15 Comparison of dielectric constant before and after anneals for $HfLaO_x$ films with different La percentages. The κ values of $HfLaO_x$ films increased dramatically after crystallization. The highest κ values can be as high as 38 when La percentage is in the range of 6% to 8% in $HfLaO_x$ films.

Similar phenomenon of κ value enhancement after crystallization from amorphous for hafnium-based dielectrics was also reported. The cubic-like or tetragonal-like crystal structure of hafnium-based dielectrics after high temperature treatment was obtained by using Si, Y, Dy, Gd, Er, or other dopants [15-20]. In order to achieve the optimum permittivity, different doping elements require different doping percentages [16]. Using an La dopant, the optimum doping percentage was reported to be around 4% and the highest κ value for La doped HfO_2 was only ~ 28 [20]. However, this reported κ value is much lower than the values we obtained (37.7 ± 1) and the optimum La doping percentage is also different (~ 8%). The inconsistency of κ values and optimum doping percentages may be caused by different deposition methods. The ALD process, used in this work, may have better control of the composition ratio, compared to the co-sputtering method used in previous works [20]. According to our experience, in order to achieve a low doping percentage (4% to 8%) during co-sputtering, the sputter power drawn for La target during co-sputtering is near the lower end range (~ 60 W). At this range, the output power is usually not stable. The fluctuation of the output power would result in composition variation. On the other hand, as shown in Fig. 3.15, the κ values of $HfLaO_x$ are much more sensitive to the La concentration when the atomic ratio of La/(La + Hf) ranges from 3% to 16%. Thus, a small composition variation of La in $HfLaO_x$ will result in a large difference in κ values. Moreover, our experiment also showed a κ value of 28 when La doping was 4%, which is the same as the report in Ref. [20]. Notably, the peak value of 38 is also the highest κ value reported in the

literatures for hafnium-based dielectrics.

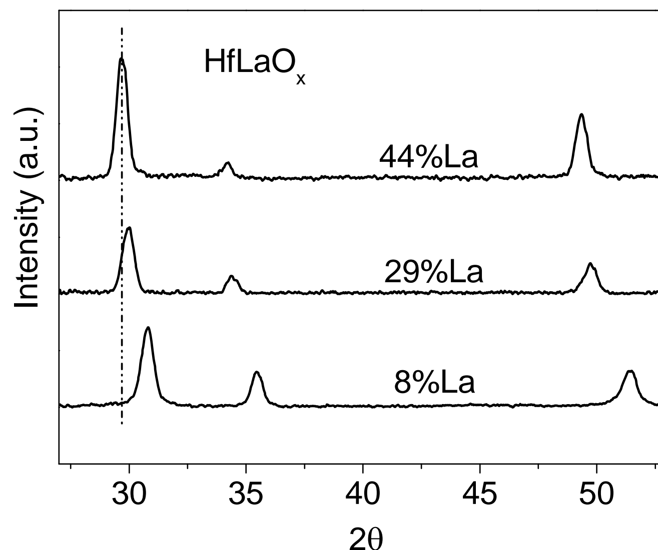

Fig. 3.16 The XRD spectra for crystallized $HfLaO_x$ films with various La percentages. With the increase of La percentage, the peaks of cubic phase shift toward lower incident angle, implying an increase of cubic crystal volume.

The reason for the variation of κ values with La percentages was also investigated. On one hand, when atomic ratio of La/(La + Hf) is below 6%, the κ value increases with the increase of La percentage. This region is believed to be a crystal-phase transaction region and contains both monoclinic phases and cubic phases. As monoclinic HfO_2 has a relatively lower κ value (~20), the overall κ value of $HfLaO_x$ would be decreased if the monoclinic phase exists. On the other hand, when the atomic ratio of La/(La + Hf) is greater than 8 percent, the κ value continuously decreases as the La percentage increases. The decrease of κ value is believed to be attributed to the different crystal volume, as evidenced in XRD results shown in Fig. 3.16. With the increase of La percentage, the cubic peaks shift toward

lower incident angle, implying an increase of the cubic crystal volume. The increase of the crystal volume would result in a decrease of κ value [18]. Extrapolating the decreasing trend shown in Fig. 3.15, the κ value of 50% La-$HfLaO_x$ is estimated to be 24, which is consistent with other reports showing that the κ value of pyrochlore $La_2Hf_2O_7$ is in the range of 18 to 25 [21-23]. In summary, 8% La-$HfLaO_x$ film is believed to be fully crystallized to a cubic-like structure containing minimum crystal volume, thereby exhibiting highest κ value.

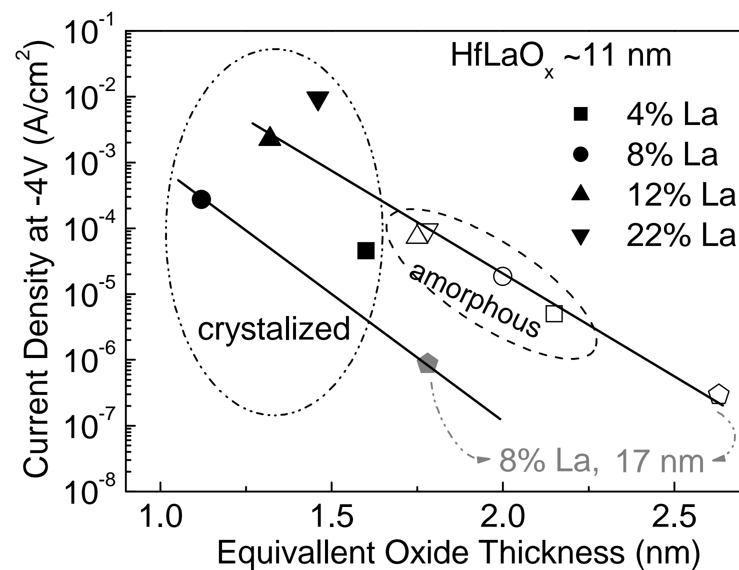

Fig. 3.17 The leakage current comparison of $HfLaO_x$ films with different La percentages. All the data points of leakage current were extracted at – 4 volts. Another leakage current of 17-nm-thick 8% La-$HfLaO_x$ film was also shown here to draw the reference line. Among all the films, crystallized 8% La-$HfLaO_x$ films exhibit the lowest leakage currents.

Figure 3.17 compares the leakage currents extracted from $HfLaO_x$ films with various La percentages before and after crystallization at - 4 volts. When $HfLaO_x$ films are in amorphous phase (as-deposited), these extracted points of leakage current

nearly fall on the same line. This implies that all amorphous $HfLaO_x$ exhibits the similar leakage current performance regardless of La percentages. In contrast, after crystallization, the leakage current varies. The annealing conditions are the same as that in Fig. 3.15. For a fixed physical thickness, leakage current increases after crystallization. However, thanks to the dramatic increase of the κ values, under the same EOT, crystallized $HfLaO_x$ films with 4%, 8% and 12% La show comparable or better leakage currents than amorphous films. Furthermore, among all the crystallized films, $HfLaO_x$ with 8% La exhibits the lowest leakage current.

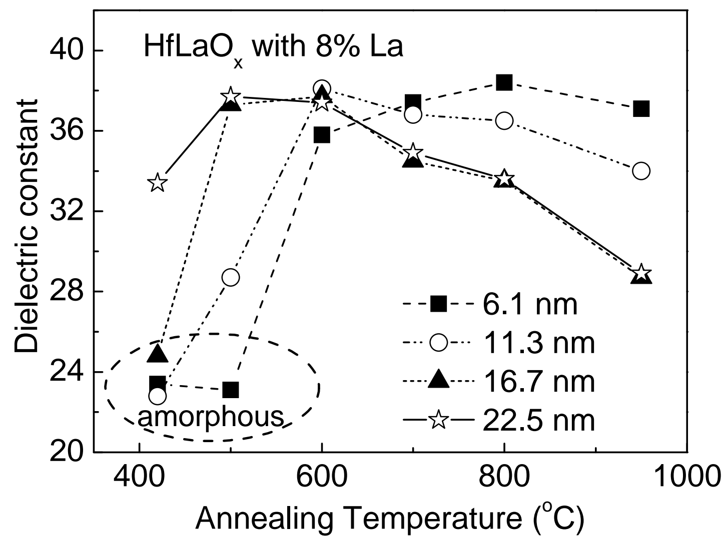

Fig. 3.18 The dielectric constant of 8% La-$HfLaO_x$ films with various thicknesses as a function of annealing temperatures. When the annealing temperature was far above the onset of the crystallization temperature, the κ values decreased.

Thermal stability of 8% La-$HfLaO_x$ films was investigated with various annealing temperatures. As shown in Fig. 3.18, there is a clear trend of the κ value decrease if the annealing temperature is too high. For instance, the κ value of 16.7-nm

8% La-$HfLaO_x$ decreases from 38 to 28 after anneal at 950ºC. Proper annealing temperature is required in order to achieve the highest permittivity. Moreover, this annealing temperature is also dependent on the physical thickness, i.e., 800ºC and 600ºC for 6.1 nm and 11.3 nm thick films, and 500ºC for both 16.7 nm and 22.5 nm thick films, respectively. Based on extracted κ values, the optimum ranges of annealing temperature are summarized in Fig. 3.19.

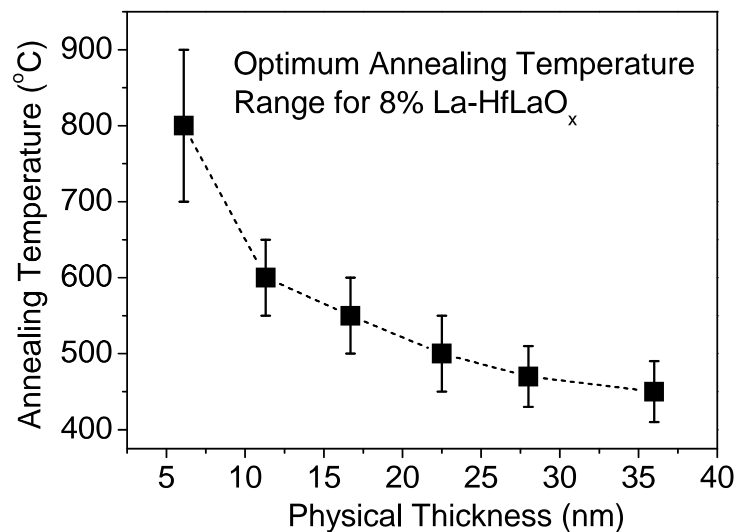

Fig. 3.19 A summary of annealing temperature needed to obtain the optimum film property for 8% La-$HfLaO_x$ films as a function of physical thicknesses. $HfLaO_x$ with thinner physical thickness require higher annealing temperatures.

It is also found that the thicker the $HfLaO_x$ film is, the faster permittivity drops. The reasons of permittivity dropping were investigated. The wafer of 8% La-$HfLaO_x$ was cut into many small pieces. These small samples were annealed at different temperatures and then were sent for the XRD analysis. As shown in Fig. 3.20, a new spectrum peak is observed at 31.5º when the annealing temperature is greater than

800ºC. This new peak corresponds to monoclinic-HfO_2, thereby resulting in overall permittivity drops. Furthermore, the cubic peaks also show a small shift towards a lower incident angle. As discussed in Fig. 3.16, this lower incident angle shift indicates a decrease of permittivity. In summary, both partial formation of the monoclinic phase and lower incident angle shift caused by high temperature anneals indicates a decrease of the overall κ value.

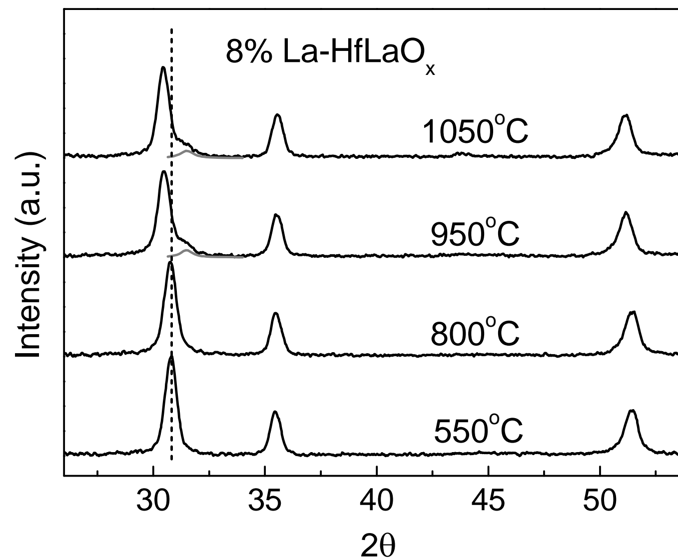

Fig. 3.20 The XRD spectra for 8% La-$HfLaO_x$ films with annealing at different temperatures. The main peak of cubic phase shifts to lower incident and a new small peak of monoclinic phase appear besides this main peak.

In addition, it is worth to note that the κ values cannot be extracted using the plot of EOT *vs*. physical thickness here, because the optimum annealing condition which provides the maximum κ value is different for different physical thicknesses of $HfLaO_x$ films and thus the plot of EOT *vs*. physical thickness at a given annealing temperature will not show a linear relationship. Therefore, in this work, the κ values

of 8% La-$HfLaO_x$ for different physical thickness were calculated out separately under each optimum annealing condition and they all show consistency of a value of 38. This value is further verified with 45-nm thick $HfLaO_x$ films.

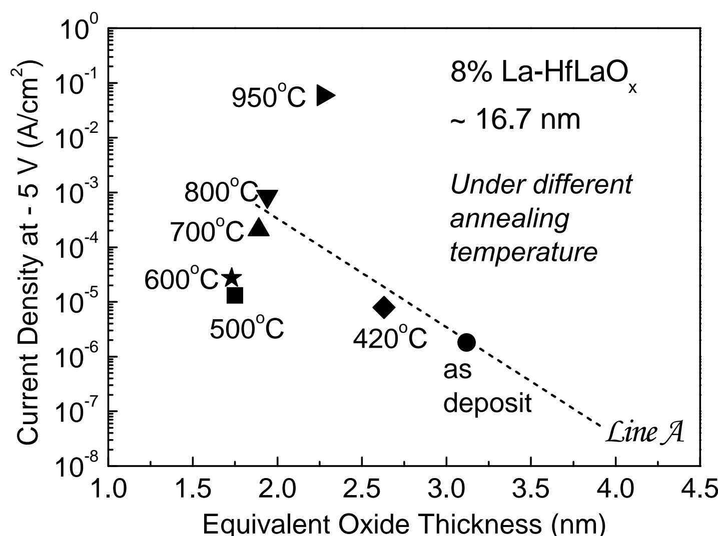

Fig. 3.21 Comparison of leakage currents of 8% La-$HfLaO_x$ films under different annealing temperatures. All the data points of leakage current are extracted – 5 volts. The dashed line (L*ine A*) is a reference line for the amorphous $HfLaO_x$ films (under as-deposited condition). When annealing temperature is 500ºC or 600ºC, the 8% La-$HfLaO_x$ films exhibits the lowest leakage current.

The extremely high temperature anneals not only degrade the permittivity, but also worsen the leakage current performance, as shown in Fig. 3.21. All the data points of leakage current are extracted from 8% La-$HfLaO_x$ film with various annealing temperatures at – 5 volts. It is clear that, for a 16-nm thick film, the lowest leakage current can only be obtained when the annealing temperature is in the range of 500ºC to 600ºC. If the annealing temperature is beyond this range, the leakage current degrades. The higher the annealing temperature is, the more the

leakage current degrades.

In conclusion, through cubic-structure formation, 8% La-$HfLaO_x$ film can exhibit the highest permittivity (~38) and best leakage current performance. These promising properties of $HfLaO_x$ may be useful in DRAM, RF IC or non-volatile memory applications.

3.5 Electrical Characteristics of $LaAlO_x$ Films

As discussed in the previous chapter, the deposition temperatures for Al_2O_3 and La_2O_3 ranges from 270ºC to 450ºC and from 270º to 480ºC, respectively. Thus, theoretically, a wide range of deposition temperatures from 300ºC to 450ºC can be used to deposit $LaAlO_x$ films. Here, under this wide temperature range, $LaAlO_x$ films were deposited as gate dielectrics in MOS capacitor structures. By evaluating the electrical performances of these MOS capacitors, an optimum deposition temperature can be obtained.

A large negative flat band voltage (V_{fb}) in *C-V* curve was observed for all $LaAlO_x$ films. As shown in Fig. 3.22, when annealing temperatures below 900ºC, these negative V_{fb} ranges from 0.4 V to 0.8 V, which are slightly smaller than that of $HfLaO_x$. Moreover, these negative V_{fb} in *C-V* curves were only observed from $HfLaO_x$ and $LaAlO_x$ gate dielectric MOS devices but not from HfO_2 or Al_2O_3 gate dielectric MOS devices. Thereby, it is deduced that this negative V_{fb} should be introduced by La atoms.

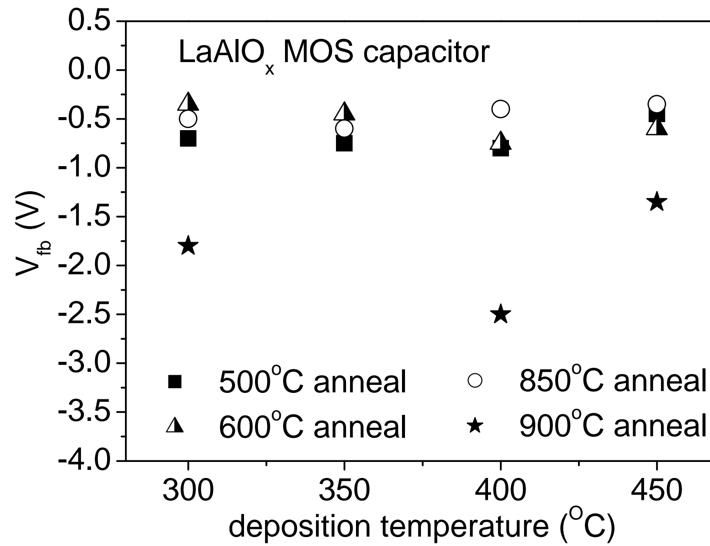

Fig. 3.22 The flat band voltage (V_{fb}) distribution for $LaAlO_x$ films deposited at various temperatures as a function of annealing temperatures. $LaAlO_x$ films with 900ºC anneal exhibit abnormal flat band voltage shift.

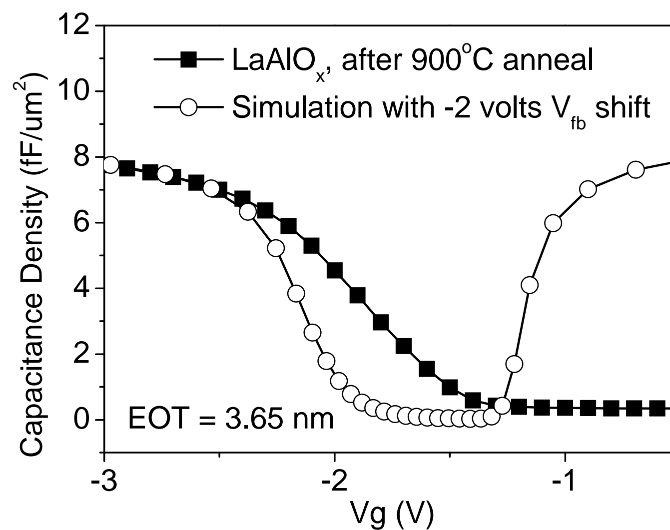

Fig. 3.23 A comparison of the *C-V* curves between 40% La-$LaAlO_x$ film and a simulated curve. The gentle slope of *C-V* curve at the depletion region indicates a large amount of traps at the silicon interface.

On the other hand, when the annealing temperature is greater than 900ºC, $LaAlO_x$ films exhibited a significant negative V_{fb} shift. This significant negative V_{fb}

shift was caused by *C-V* curve deformation. As shown in Fig. 3.23, there is a gentle slope at the depletion region in the *C-V* curve, which indicates a large amount of traps at the silicon interface. The interface traps are believed to be caused by the inter-diffusion between La and Si atoms. It was reported that a dramatic atom inter-diffusion would happen under high temperature anneal if La was directly contacting with silicon substrate [24]. Based on the observation of no gentle slop for annealed $HfLaO_x$ films in *C-V* curves, we suspect that the atomic inter-diffusion between La and silicon was further promoted by the phase separation, though the phase separation was not observed in XRD spectra at this temperature range but clearly shown after anneal 1050ºC. In addition, the *C-V* deformation resulted in a malfunction of $LaAlO_x$ devices, which was also reported by Triyoso *et al* when MOS devices were annealed at 850ºC or 900ºC [25].

The leakage current performances of $LaAlO_x$ at different annealing temperatures (550ºC and 850ºC) were compiled in Fig. 3.24 (a) and (b). No matter what the post deposition temperature is, all $LaAlO_x$ films have the similar leakage current performance except the film deposited at 450ºC. The degradation of leakage current of $LaAlO_x$ film deposited at 450ºC indicates high bulk trapping density. The high bulk trapping density is possibly caused by large amount of impurities generated from precursors due to thermal decomposition at 450ºC. In summary, based on the electrical results, the optimum temperature window for the deposition of ALD $LaAlO_x$ should be below 400ºC.

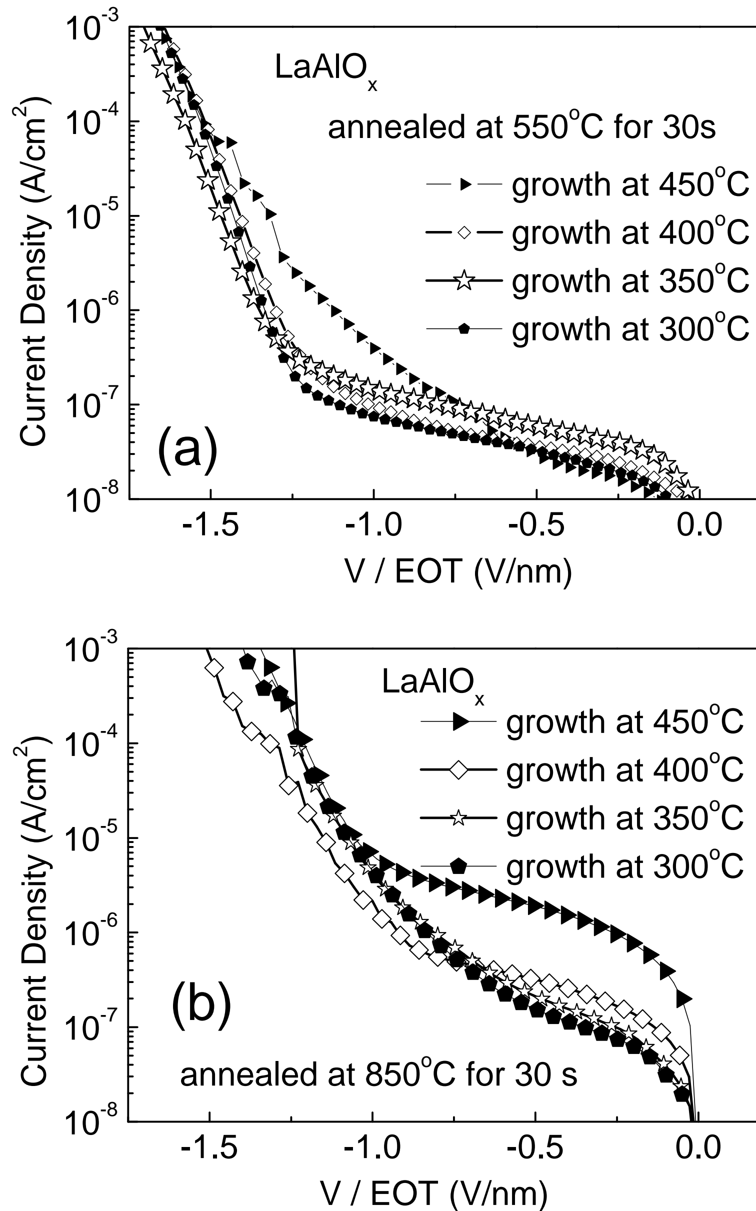

Fig. 3.24 Leakage current comparison for $LaAlO_x$ films deposited at various temperatures. All films were annealed at (a) 550ºC for 30s and (b) 850ºC for 30s under one atmospheric pressure in N_2 ambient. The $LaAlO_x$ films deposited at 450ºC exhibits a degraded leakage current, indicating the deposition temperature should be below 450ºC.

Moreover, as shown in Fig. 3.24, the $LaAlO_x$ films annealed at 850ºC exhibited worse leakage current performance than that annealed at 550ºC, especially at low electric field. These degradations are believed to be closely related to the thin

low-κ interfacial layer, which has a different value of conduction band offset. This thin low-κ interfacial layer plays an important role in determining the leakage current, which was discussed in depth in reference [26]. Another issue associated with the interfacial layer is the high defect density due to the non-stoichiometric formation during the initial deposition. These defects would assist the leakage current as a stepping-stone.

In addition, a permittivity of 17 was abstracted for 55% La-$LaAlO_x$ from MIM capacitor devices.

3.6 Summary

In this chapter, the material properties of $HfLaO_x$ and $LaAlO_x$ films have been discussed systematically. When La concentration is low, both $HfLaO_x$ and $LaAlO_x$ dielectrics exhibit good hygroscopic property. Besides, as La percentage increases, $HfLaO_x$ dielectrics exhibit wider energy band gaps, greater conduction band offsets over silicon, and higher crystallization temperatures. In contrast, for $LaAlO_x$ dielectrics, La percentage has hardly any impact on energy band gap, conduction band offset or crystallization temperature. It is also found that when the La percentage is around 8%, $HfLaO_x$ film exhibits highest dielectric constant (~38) and lowest leakage current after crystallizing to cubic-structure. In order to achieve such promising results, the annealing temperature needs to be carefully controlled as the optimum range of deposition temperature is dependant on the film thickness. Unlike the small range of deposition temperature (270ºC to 300ºC) for ALD $HfLaO_x$, $LaAlO_x$ can be

deposited at the temperature ranging from 300ºC to 400ºC. $LaAlO_x$ films can stand up to 850ºC anneal. However, if the annealing temperature is further increased to 900ºC, the phase separation may happen and the MOS devices show large defect density at the interface.

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Chapter 4 Evaluation of SONOS-type Memory Cells with Lanthanum-incorporated Dielectrics as Blocking Oxide

4.1 Introduction

In the previous chapter, the material properties of lanthanum-incorporated dielectrics ($LaAlO_x$ and $HfLaO_x$) have been investigated systematically. Both dielectrics exhibit wide energy band gaps, large conduction band offsets, good thermal stabilities and high κ values. Because of their promising material properties, in this chapter, both $LaAlO_x$ and $HfLaO_x$ dielectrics will be used as the blocking oxide in conventional SONOS-type flash memory. The electric field of blocking oxide or tunnel oxide will be deduced first to illustrate effects of integrating high-κ dielectrics. Based on the deduction, a rule of fair comparison among different memory cells will be given. Afterwards, the performance of memory cells using different dielectrics ($LaAlO_x$, $HfLaO_x$ and Al_2O_3) will be compared, such as programming / erasing speeds, data retention, cycling endurance, cell reliability, etc. Among them, the mechanism of data retention under different temperatures will be analyzed and the requirement of conduction band offset will be provided. Furthermore, based on the data retentions under elevated temperatures, the energy trapping depth in nitride film will be derived using the modified Yang's models.

4.1.1 Architecture of Flash Memory

There are several types of flash memory, NOR-type and NAND-type memories currently dominant the flash market. The circuit architecture of NOR flash memory and NAND flash memory are illustrated in Fig. 4.1 [1, 2]. The memory cells of NOR flash, shown in Fig. 4.1(a), are connected in parallel [1]. This parallel architecture enables random data access and a slightly faster read speed than NAND flash memory. With the advancement of easy code execution and low standby power, NOR flash memory is suitable for code storage, such as PDA or cell phone [2].

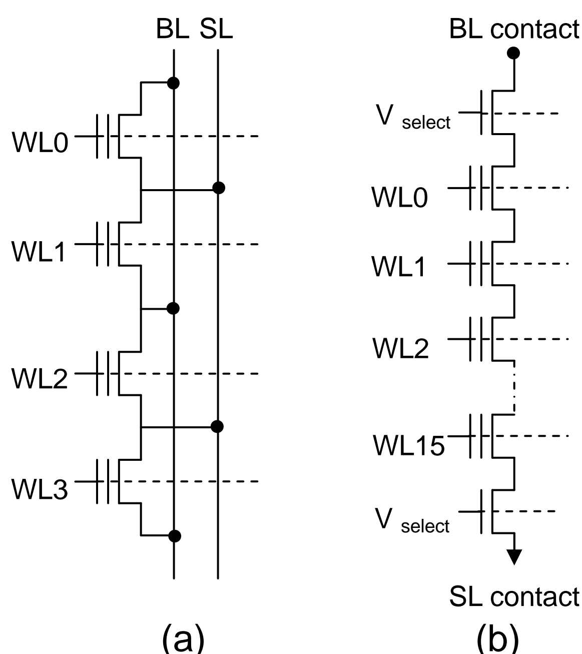

Fig. 4.1 A schematic illustration of typical circuit diagram of (a) NOR-type flash memory and (b) NAND-type flash memory. Here, BL, SL and WL refers to bit line, source line and word line, respectively [1]. Because of the series connection, NAND flash memory offers the highest integration density thus lowest cost-per-bit.

In contrast, the memory cells of NAND flash memory, shown in Fig. 4.1(b),

are connected in series and with selecting transistor at both ends [1]. This series architecture has the highest integration density due to the substantially reduced number of contacts. NAND flash memory can offer lowest cost-per-bit. Furthermore, compared to NOR flash memory, NAND flash memory exhibits faster programming / erasing speeds, lower active power and more tolerance to oxide defects due to the implementation of error code correction (ECC), thus is favored by the application of mass information storage, such as Flash drives, MP3 players, digital camera, etc.

Different programming/erasing schemes are used for different architectures. SONOS-type NOR flash uses hot hole injection (HHI) and channel hot electron (CHE) to erase or program the cells, respectively [2-4]. In contrast, SONOS-type NAND flash cells can only be programmed or erased using the Fowler-Nordheim (FN) tunneling method [2].

Because FN tunneling does not require high drain current and abrupt deep junction like CHE injection, NAND flash has a better endurance capability than NOR flash [5]. Furthermore, NAND flash can bear higher channel leakage current due to its series connection manner, thus enabling better scaling capability [5]. Thirdly, NOR flash encounters a special scaling challenge of resolution loss due to the mergence of source drain charges when gate length is further scaled down to below 100 nm, thus losing the capability of physical storage of 2-bit-per-cell [5-7].

In summary, because of above advancements, NAND-type SONOS cells are chosen to be the focus in this study.

4.1.2 Basic Operation of Memory Cell

The operation of memory cell is to remove (erase) or put (program) charges into the storage layer (e.g. silicon nitride trapping layer). There are several basic physical mechanisms involved in the operation of memory cells, such as channel hot electron (CHE) injection and Fowler-Nordheim (FN) tunneling, hot hole injection (HHI), band-to-band-tunneling hot hole (BTBTHH), trap assisted tunneling, etc. As this study focused on the NAND-type SONOS cell, the operations of NAND-type memory cells are illustrated, as shown in Fig. 4.2.

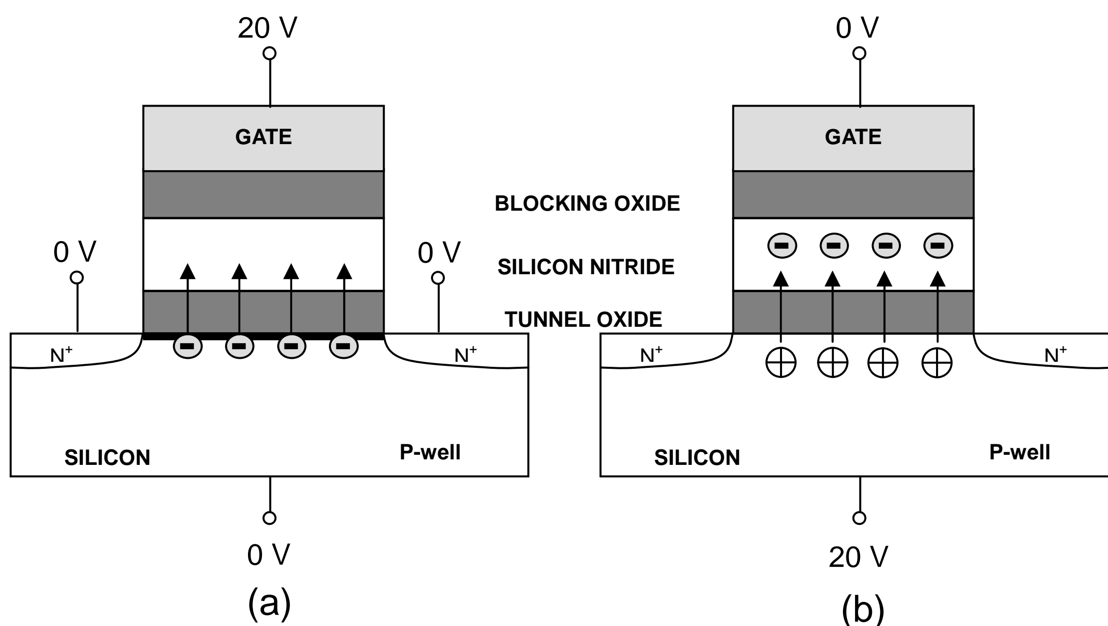

Fig. 4.2 A schematic illustration of NAND-type SONOS cell under (a) program and (b) erasure by Fowler-Nordheim tunneling [1].

For NAND-type flash, FN tunneling is used during the program by applying a high voltage (e.g. 20 V) to the gate while grounding the drain, source and bulk, as shown in Fig. 4.2(a) [1]. Thus, the electrons will be injected from the inversion layer

into the nitride trapping layer, inducing the threshold voltage shift from negative value (logic 1) to positive value (logic 0). One of the advantages of FN programming is that it generates a small programming current (< 1 nA) per cell. This results in lower active power than that from CHE injection method and allows batch program [1].

Cell erasure is also accomplished by FN tunneling for NAND-type memory cells by setting the P-well and the control gate of the memory cell to 20 V and 0 V, respectively, and keeping the source and the drain floating [1]. In such condition, the gate stack is stressed under a high reverse electric field. This reverse electric field will drive electrons out of nitride trapping layer or inject holes from accumulation channel into trapping layer, thus changing the threshold voltage from positive value (logic 0) to negative value (logic 1). Normally, the memory cell is over-erased to – 3 V deliberately to avoid any misoperation of the silicon channel [1].

During the read operation of NAND-type memory, a low voltage or 0 V is applied onto the gate of the selected memory cell, while a higher voltage of V_{read} (e.g. 4.5 V) is applied to other memory cells and selecting transistors in the same string. This will make these cells serving as transfer gates [1]. As a result, the state of memory cell can be detected by a sense amplifier, which is connected to the bit-line. Normally, a high bit-line current implies that memory cell is under depletion mode and a logic value 1 is stored, as illustrated in Fig. 4.3. Conversely, a low bit-line current implies that memory cell is under the enhancement mode and a logic value 0 is stored.

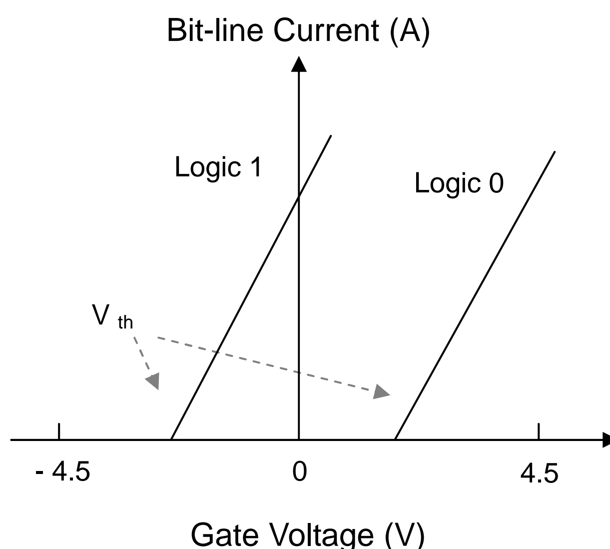

Fig. 4.3 An illustration of reading operation for NAND memory cell. Here, the bit line of the memory string is connected to a sense amplifier. By sensing the bit-line current, the status of memory cells can be detected.

4.1.3 Endurance and Data Retention

In most flash memories, the programming and erasing operations will generate stresses on the memory gate stack that eventually degrades the dielectrics and memory performances. In order to describe the capability of a memory cell to withstand these stresses, a term “endurance” is used [1]. Endurance is impacted by several factors, such as material property, deposition method, device geometry, cycling stress, program/erasure method, etc. Endurance test is used to verify whether the memory cell is still functional or not after a certain number of program-erasure cycles. Generally, after a large number of program-erasure cycles, the memory window becomes much smaller or shifts away from the original position [1]. Thus, the memory window is required to be maintained in a reliable range to avoid

information error. Normally, the number of program-erasure cycles used in semiconductor industry is in the range 20,000 to 100,000 [1].

Besides, the elapsed time between initial program and the first erroneous readout from the memory cell is called retention [1]. A typical requirement for retention time in industry is 10 years. The duration of 10-years retention test for natural decay is too long to monitor compared to human lifespan. In practice, the retention test is performed for several days or weeks under elevated temperature (e.g. 150ºC or 250ºC) to accelerate the charge loss [1]. However, the retention under high temperature is a big challenge, especially for nitride-based memory cells (SONOS). In order to reach fast operation speeds, the tunnel oxide of SONOS-type flash memory is usually thin, which is in the range of 1 to 3 nm. However, this thin tunnel oxide usually results in a retention degradation because of charge loss caused by direct tunneling. As a result, a tradeoff between the retention and the operation speeds exists [8]. A goal of our research was to push away this tradeoff by improving the operation speed without retention degradation.

In summary, both retention and endurance are important characteristics for memory cells because they indicate the lifespan of the memory cells. In the later part of this chapter, these two important characteristics for SONOS type flash memory will be deeply investigated.

4.2 Theoretical Considerations

Before the experiment, the electric field on tunnel oxide and blocking oxide was derived.

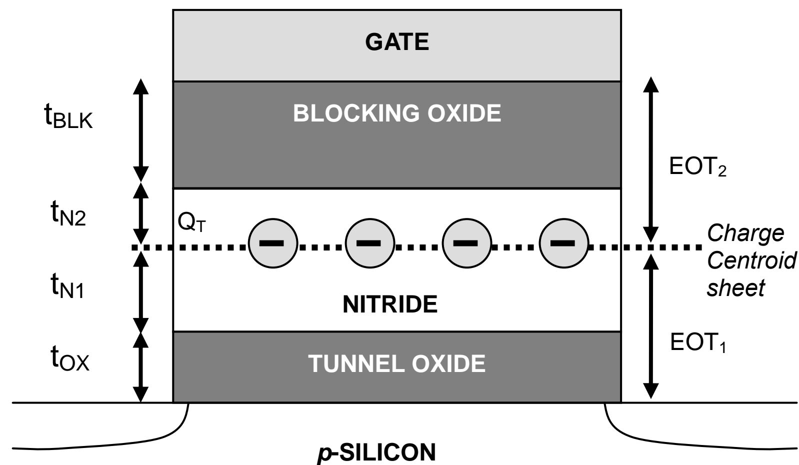

Fig. 4.4 A cross-section of SONOS structure with assumption of a sheet charge centroid in nitride; t_{OX}, t_{N1}, t_{N2} and t_{BLK} are the physical thickness of tunnel oxide, distance from charge centroid to tunnel oxide, distance from charge centroid to blocking oxide and physical thickness of locking oxide, respectively. The assumption of a charge centriod sheet greatly simplifies the analysis of electric field.

The vertical cross-section view of SONOS memory cell is illustrated in Fig. 4.4. The nitride trapping layer is sandwiched between the tunnel oxide (at bottom) and blocking oxide (on the top). During the programming / erasing operation, the nitride layer stores charges (Q_T) that are responsible for threshold voltage (V_{th}) shift. The charges inside the nitride film distribute uniformly in horizontal plane if Fowler-Norheim tunneling is used during program or erasure. On the other hand, the vertical distribution of charges is unknown. Regardless of the vertical distrubtion, the

charges that causing V_{th} shift can be regarded as a centroid sheet, as shown in Fig. 4.4. Thus, by using Gaussian equitation, V_{th} shift (ΔV_{th}) can be derived as

$$\Delta V_{th} = (\frac{t_{N2}}{\varepsilon_0 \varepsilon_{SiN} A} + \frac{t_{BLK}}{\varepsilon_0 \varepsilon_{BLK} A})Q_T \quad (1)$$

where t_{BLK} is the physical thickness of blocking oxide, t_{N1}, t_{N2} is the physical thickness from charge centroid to the tunnel oxide or to the blocking oxide, respectively, and ε_{SIN} and ε_{BLK} are the permittivity of the silicon nitride and the blocking oxide, respectively.

If we use EOT_1 and EOT_2 to represent the equivalent oxide thickness from charge centroid to the silicon surface or to the gate electrode, respectively, we have

$$EOT_1 = t_{N1} \frac{\varepsilon_{TOX}}{\varepsilon_{SIN}} + t_{TOX}$$

$$EOT_2 = (\frac{t_{N2}}{\varepsilon_{SiN}} + \frac{t_{BLK}}{\varepsilon_{BLK}})\varepsilon_{TOX}$$

where t_{TOX} is the physical thickness of tunnel oxide (SiO_2), ε_{TOX} is the permittivity of silicon dioxide. Hence, equation (1) can be simplified as

$$\Delta V_{th} = \frac{EOT_2}{\varepsilon_0 \varepsilon_{TOX} A} Q_T \quad (4)$$

Equation (4) indicates that the threshold voltage is determined by the electron charges (Q_T) and equivalent oxide thickness from the charge centroid to the top electrode.

Furthermore, based on above equations, the electric field in the tunnel oxide or the blocking oxide during programming or erasing operation can be derived as

$$E_{TOX} = \frac{V_g - \Delta V_{th} - \Phi_{MS} + \psi_s}{EOT_{total}} \quad (5)$$

$$E_{BLK} = \frac{\varepsilon_{TOX}}{\varepsilon_{BLK} EOT_{total}} (V_g + \frac{EOT_1}{EOT_2} V_{th} - \Phi_{MS} + \psi_s) \quad (6)$$

Where V_g is programming or erasing (P/E) voltage, Φ_{MS} is the work function difference between metal gate and silicon substrate, ψ_S is the surface potential, and EOT_{total} is the total EOT of the whole gate stack including tunnel oxide, nitride and blocking oxide. In a special case, when V_g is equal to zero, the equation (5) and (6) represent electric fields under the retention mode.

Equation (5) and (6) directly imply that, during the program, the increase of threshold voltage (V_{th}) will result in a decrease of E_{TOX} and a simultaneous increase of E_{BLK}. Both trends will ultimately lead to a state of programming saturation due to the equal current in the tunnel oxide and the blocking oxide. Besides, if V_g is changed from program to erasure, the voltage on tunnel oxide changes from $|V_g|$-$|V_{th}|$ to $|V_g|$+$|V_{th}|$. Thus the electrical filed in tunnel oxide during erasure is much higher than that during program. This high electric field during erasure will normally make the hole charges tunnel through the tunnel oxide then neutralize the trapped electrons in nitride layer, resulting in V_{th} shift back. On the other hand, this high electric field on tunnel oxide may also generate defects at tunnel oxide and silicon interface or even inside the bulk of tunnel oxide, which leads to endurance degradation and even early hard breakdown.

Secondly, equation (5) also implies that electric field in the tunnel oxide is determined by the threshold voltage shift, total gate stack EOT and the operation voltage, but not related to the charge distribution or κ values of the blocking oxide. This

gives us a guideline for fair comparison among memory cells if their blocking oxides are different. As long as the EOT of the blocking oxide remains constant during dielectric replacement, the electric field in the tunnel oxide can be maintained the same. Thus, any differences in memory performance would originate from the blocking oxide. In addition, in the case of retention evaluation, a fair comparison additionally requires the same initial ΔV_{th}.

Thirdly, with regard to the work function of the gate electrode, high work function (like IrO_2) is usually favored to reduce the back tunneling current from the electrode, thus enabling a fast erasure speed [9]. However, according to above equations, this high work function (Φ_{MS}) will lead to a larger electric field in blocking oxide during retention mode, which has a considerable impact on data retention.

4.3 Experiments

Nitride-based Flash memory transistor cells using $LaAlO_x$, $HfLaO_x$ and Al_2O_3 as blocking oxide were prepared. In order to minimize the disturbance of charge loss from tunnel oxide, a relative thick tunnel oxide (5-nm SiO_2) was thermally grown on a p-type Si substrate. On top of SiO_2, a 6-nm-thick LPCVD Si_3N_4 was deposited as charge trapping layer, followed by blocking oxide deposition. There are three different types of blocking oxides ($LaAlO_x$, $HfLaO_x$ and Al_2O_3) using atomic layer deposition (ALD) method. The ALD deposition parameters were all the same as that mentioned in Chapter 3 except the deposition temperatures were all fixed at 300ºC. The physical

thicknesses of these dielectrics were carefully defined to make the same gate-stack equivalent oxide thickness (EOT_{total}) for fair comparisons. On top of these ALD blocking oxides, a 150-nm-thick TaN was deposited by reactive sputtering to be the gate electrode. After gate stack patterning and S/D implantation with arsenic, samples were all annealed at 850°C for 30mins to activate the dopants. The annealing temperature of 850°C will avoid possible phase separation of $LaAlO_x$ film. In the end, a forming gas anneal was performed at 420°C for 30mins in a N_2/H_2 ambient.

In addition, the physical thickness of dielectrics was determined using the spectroscopic ellipsometer and verified by the high resolution transmission electron microscopy (HRTEM). The atomic ratio of ternary dielectrics was determined using the high resolution x-ray photoelectron spectroscopy (XPS). The threshold voltage (V_{th}) and capacitance-voltage (*C-V*) was measured using Agilent 4155C semiconductor parameter analyzer and Agilent 4284A precision LCR meter at a frequency of 100 kHz, respectively. During the program or erasure, the voltage pulse was generated using HP 8112A Programmable Pulse Generator.

The gate lengths of patterned SONOS memory cells were in the range of 4 ~ 20 μm. Because FN tunneling method was used to program or erase the memory cells, the variations of the gate lengths or device sizes have no impact on the device performances. The voltage configurations during program or erasure were the same as the illustration in Fig. 4.2. The state of a memory cell was detected by sweeping the gate voltage while maintaining the drain voltage at 0.2 V and grounding the source

and silicon substrate. In this thesis, the value of threshold (V_{th}) is defined to the point where the drain current is 1 μA.

In addition, the programming / erasing voltages and the initial ΔV_{th} during data retention test were kept the same to make fair comparisons.

4.4 Results and Discussion

4.4.1 LaAlO Memory Cells

The programming and erasing characteristics of memory cells with $LaAlO_x$ blocking oxide (LaAlO) and memory cells with Al_2O_3 blocking oxide (AlO) were investigated first. The physical thickness of $LaAlO_x$ and Al_2O_3 were 17 nm and 9 nm, respectively, and both memory cells exhibited the same equivalent oxide thickness (EOT_{total} = 12.2 nm). The atomic ratio of La/(La + Al) in $LaAlO_x$ film was around 55%. As shown in Fig. 4.5(a), under the same program voltage, the LaAlO devices show ~ 40% and 32% improvement in program speed and V_{th} saturation window, respectively. The program performance is improved by using $LaAlO_x$ as blocking oxide.

In contrast to different speeds in program, the erasing speeds were comparable between LaAlO and AlO, as shown in Fig. 4.5(b). The only difference is that AlO shows earlier breakdown than that of LaAlO. In addition, LaAlO did not show dielectric breakdown even if it reached erasing saturation under a stress voltage of - 22 V for 0.1 s. At this condition, V_{th} stabilized at -3 V.

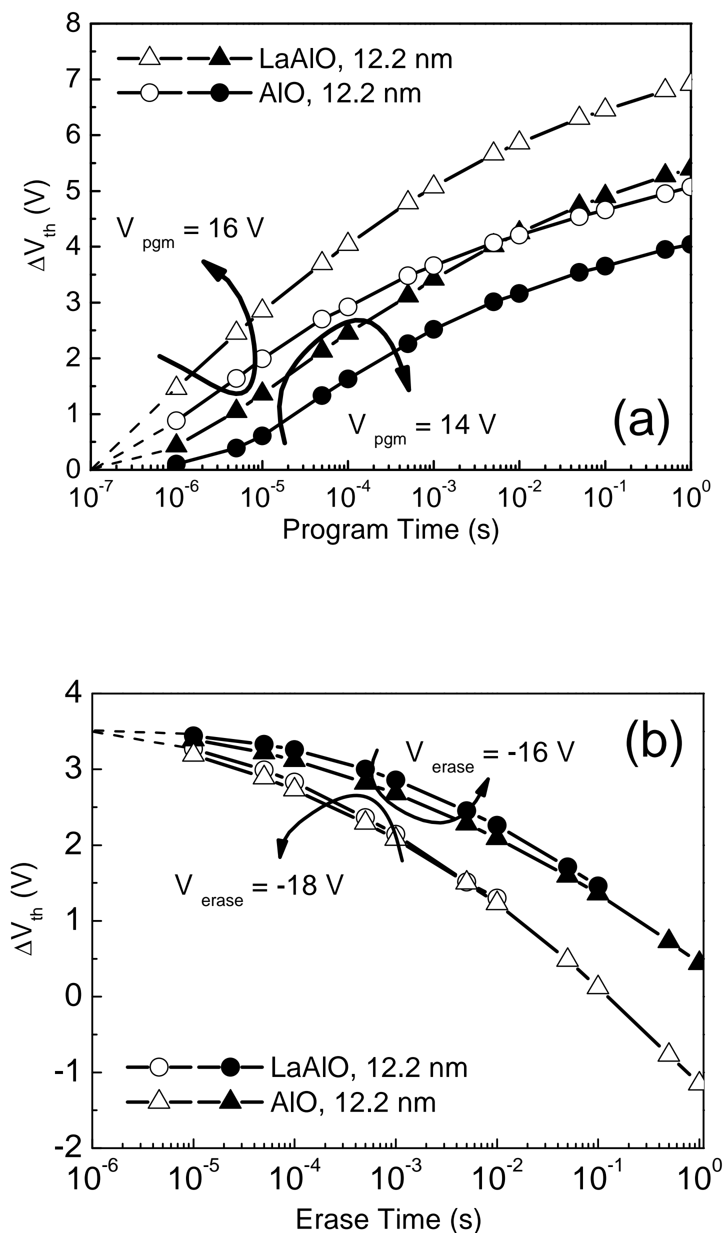

Fig. 4.5 A comparison of (a) Programming and (b) erasing characteristics between LaAlO and AlO memory cells. During the erasure, the initial V_{th} was set to 3.5 V. Compared with AlO memory cells, LaAlO memory cells showed faster programming speed and better performance of breakdown.

The fast programming speed in LaAlO devices, we believe, is due to less charging current through the blocking oxide. During program, the initial tunneling current through tunnel oxide would be the same for both types of memory cells

because of the same electric field. However, when program goes on, the less charge loss in LaAlO devices will result in a faster reduction of electric field across the tunnel oxide. This was evidenced by the smaller gate current in LaAlO devices during the program as shown in Fig. 4.6. The gate current of AlO devices was almost two times greater than that of LaAlO devices when the programming time was greater than 0.1 sec.

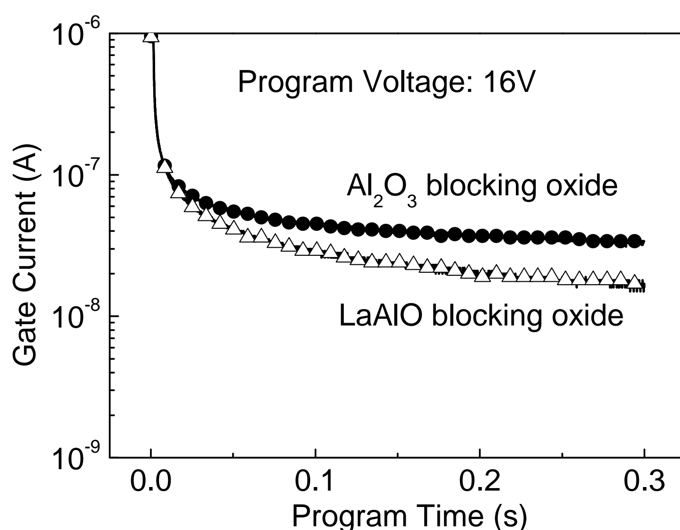

Fig. 4.6 A comparison of gate leakage current of memory cells during program. The lower current of LaAlO memory cell implies faster programming speed.

Reliability of memory gate stack was also investigated using TDDB (time dependent dielectric breakdown) test technique under negative gate biases. By applying constant negative voltage on memory cells, the memory cells were under the accumulation mode and electrons were injected from the gate electrode. Figure 4.7 shows that LaAlO cells are more robust to voltage stress. When the gate voltage was -21 V, the time to hard breakdown (t_{BD}) of LaAlO was almost 5 orders of magnitude

greater than that of AlO. Since LaAlO can stand for higher voltage than AlO, LaAlO can achieve faster erasing speed by using a higher erasure voltage than AlO.

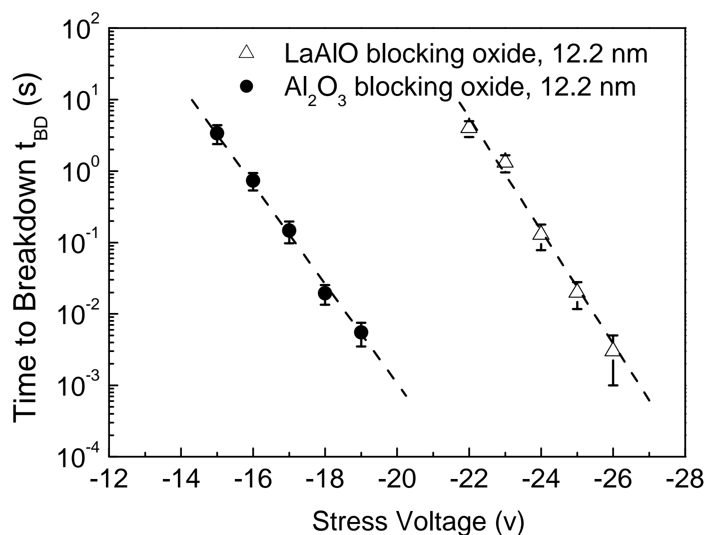

Fig. 4.7 A comparison of time-to-breakdown (hard breakdown) between LaAlO and AlO memory cells under a constant voltage stress. Memory cells with $LaAlO_x$ as blocking oxide exhibited much improved time-to-breakdown performance.

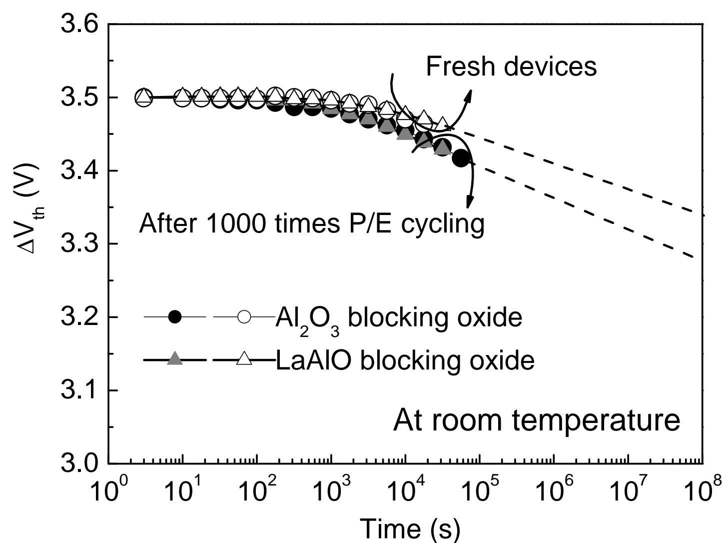

Fig. 4.8 Comparisons of data retention between LaAlO and AlO memory cells for both fresh and cycled devices. LaAlO and AlO memory cells showed almost the same retention performance at room temperature.

Data retention was also evaluated. During the evaluation, no external voltage was applied. For a fair comparison, the memory cells were programmed to the same initial V_{th} of 3.5 V. Besides, during the P/E cycles, the cycling window for both LaAlO and AlO was set to a small voltage (~1V) due to earlier breakdown of AlO. As shown in Fig. 4.8, no matter whether the memory cells are cycled for 1000 times or not, there is no difference in the data retentions between LaAlO and AlO at room temperature.

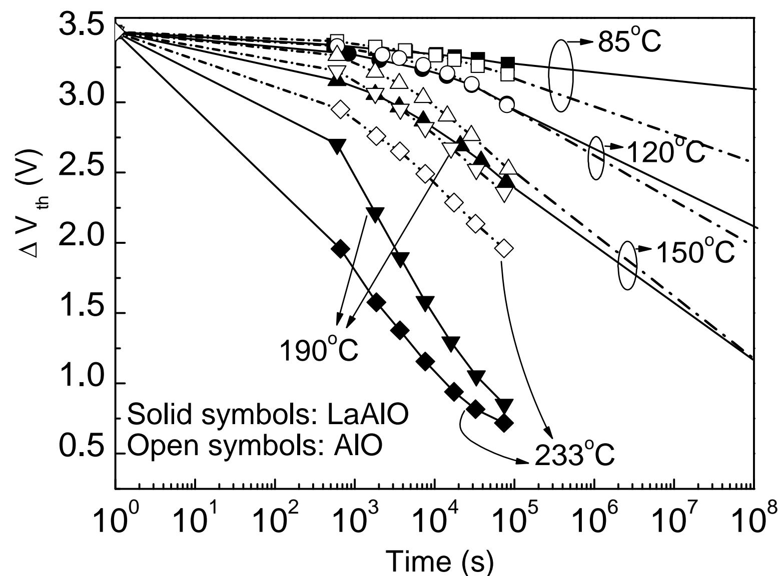

Fig. 4.9 Comparisons of data retention between LaAlO and AlO memory cells at various elevated temperatures**.** LaAlO memory cells showed improved data retention when baking temperature was below 150ºC but degraded retention performance at even higher baking temperatures.

Retention performance at elevated temperatures was also investigated. As shown in Fig. 4.9, when memory cells are evaluated at a temperature of 120ºC or below, especially at 85ºC, LaAlO shows better retention performance than AlO. However,

when the temperature is greater than 150ºC, the retention performance of AlO is much better. This discrepancy in data retention suggests a change of dominant charge-loss mechanisms at different temperatures.

For SONOS-type flash memory, the possible mechanisms of charge loss from nitride film has been identified to be trap-to-band tunneling, trap-to-trap tunneling, thermal emission, Poole-Frenkel emission or trap redistribution [10-12], as illustrated in Fig. 4.10.

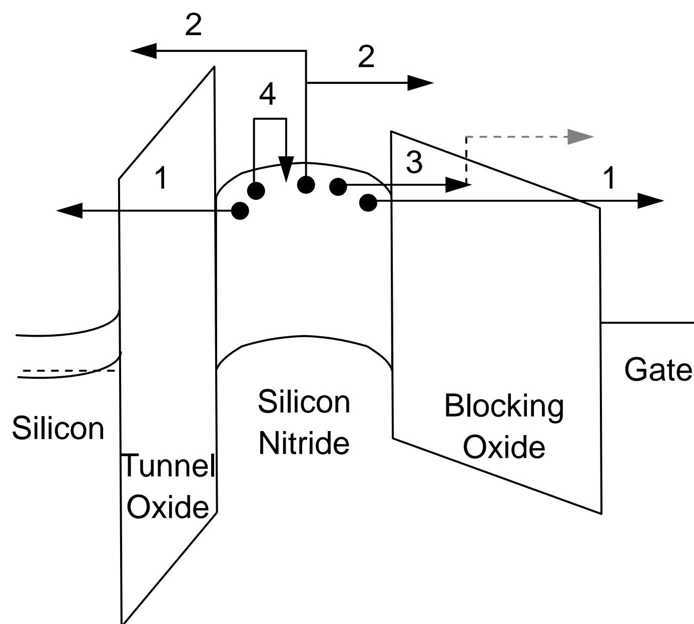

Fig. 4.10 An illustration of band diagram of a SONOS memory cell in excess electrons state under the retention mode. The electron loss mechanism is illustrated as: 1) trap-to-band tunneling, 2) thermal emission, 3) trap-to-trap tunneling, 4) Poole-Frenkel emission (including trap redistribution) [10-12]. Among them, thermal emission and trap-to-band tunneling are believed to be the dominant mechanisms of charge loss.

Among them, thermal emission and trap-to-band tunneling are believed to be the dominant mechanisms of charge loss [10, 11]. In our experiments, when temperature is below 120ºC, the better retention performance of LaAlO, we believe, is due to the longer tunneling distance, which suggests that the tunneling mechanism dominates the charge loss at this temperature range. However, when temperature is above 150ºC, the thermal emission mechanism dominates, and thus Al_2O_3 with a higher conduction band offset (~2.8 eV) exhibits better retention performance [13]. The conduction band offset of $LaAlO_x$ over Si is calculated to be around 2.6 eV from the XPS. In addition, when temperature is above 150ºC, it is also found that the retention performance is not sensitive to the physical thickness of $LaAlO_x$, again indicating that the thermal emission is the dominant mechanism at this temperature range.

In addition, we found that the data retention of memory cells was also affected by the programming voltage. As shown in Fig. 4.11 (a), the data retention of AlO is dependent on the program voltages. The higher the program voltage is, the worse the data retention exhibits. This behavior was also observed on LaAlO memory cells. As shown in Fig. 4.11(b), under the same gate stack EOT (EOT_{total}), the shift of data retention of AlO was bigger than that of LaAlO. This is believed to be related to the smaller physical thickness of Al_2O_3 blocking oxide (9 nm). However, when the physical thickness of Al_2O_3 was increased from 9 nm to 15 nm (the EOT_{total} increased from 12.2 nm to 15.0 nm), the shifts of data retention became much smaller and even could be neglected.

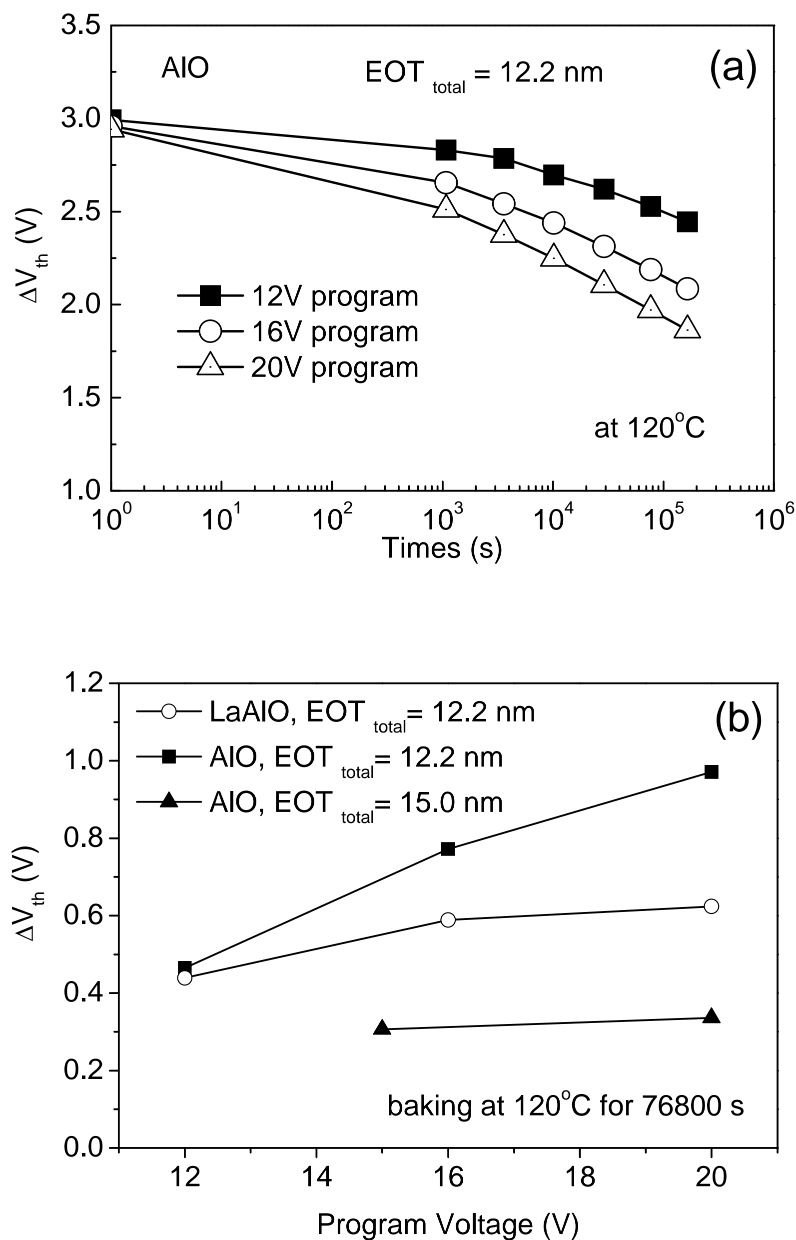

Fig. 4.11 (a) Dependence of AlO data retention on program voltage, (b) comparisons of V_{th} shift for AlO and LaAlO memory cells under various program voltages. The baking temperature was set to 120ºC during retention measurement. It shows that the higher program voltage would result in the worse data retention.

This retention shift caused by programming voltage is believed to be unrelated to oxide damage for two reasons. First, because the memory cell was only programmed or erased by several times, the damage could not be so significant. Second, a thicker

high-κ film should introduce more traps than thinner films theoretically, thus resulting in worse retention performance. However, this deduction is different from the observation shown in Fig. 4.11(b). Based on equation (6) discussed in chapter 4.2, we speculated that a higher programming voltage will cause the charge centroid to be closer to the blocking oxide. Let's assume that the charge centroid drifts up for a distance of Δx in the vertical direction in Si_3N_4 film. According to equation (6), we have:

$$\Delta E_{BLK} = \frac{\varepsilon_{TOX}}{\varepsilon_{BLK} EOT_{total}} \cdot \left(\frac{EOT_1 + \Delta x \frac{\varepsilon_{TOX}}{\varepsilon_{SiN}}}{EOT_2 - \Delta x \frac{\varepsilon_{TOX}}{\varepsilon_{SiN}}} - \frac{EOT_1}{EOT_2} \right) \cdot V_{th}$$

By simplifying the above formula, we can get:

$$\Delta E_{BLK} = \frac{\varepsilon_{TOX}}{\varepsilon_{BLK}} \cdot \left[\frac{1}{EOT_2 \cdot \left(\frac{\varepsilon_{SiN} EOT_2}{\varepsilon_{TOX} \Delta x} - 1 \right)} \right] \cdot V_{th}$$

For a thinner blocking oxide, EOT_2 will be smaller. According to derived equation above, the smaller EOT_2 will result in a greater change of the electric field on the blocking oxide. This higher electric field will lead to more charge loss through the blocking oxide layer. Therefore, the data retention for the memory cells with thinner blocking oxide is more sensitive to the charge centroid location, which is consistent with the observation shown in Fig. 4.11. In summary, we believe that the programming voltages will affect the location of the charge centriod in the vertical

direction in the Si_3N_4 film, which could explain the dependence of the data retention on the programming voltages.

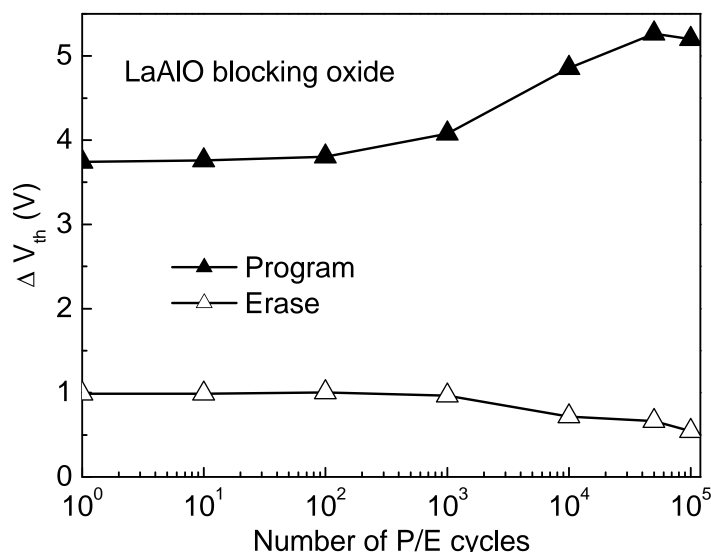

Fig. 4.12 Endurance of LaAlO memory cell with P/E cycles up to 100,000 times. The wider memory window was observed as the number of P/E cycles increased.

The test results of endurance of LaAlO cells are shown in Fig. 4.12. The endurance of AlO could not be obtained due to its earlier breakdown during the P/E cycles. It is found that, as the number of cycles increases, the subthreshold swing of LaAlO became larger, which is expected due to the interface damage during the cycling. It was also found that the V_{th} window turned wider as the erasure state continuously decreased. This behavior is on the contrary to the previous reports of narrowing V_{th} window behavior during endurance test [14].

In order to investigate this discrepancy, the changes of V_{th} during program and erasure of LaAlO memory cells before and after 100,000 P/E cycles were compared. As

shown in Fig. 4.13, the program speed of cycled memory cells is faster than that of fresh memory cells. Thus, the V_{th} of program state shift up during P/E cycles. On the other hand, during the erasure, the erasing speed of cycled memory cells is initially slower but later faster than the fresh cells when the erasing time is greater than 5 ms. Thus, the V_{th} of erasure state trends down.

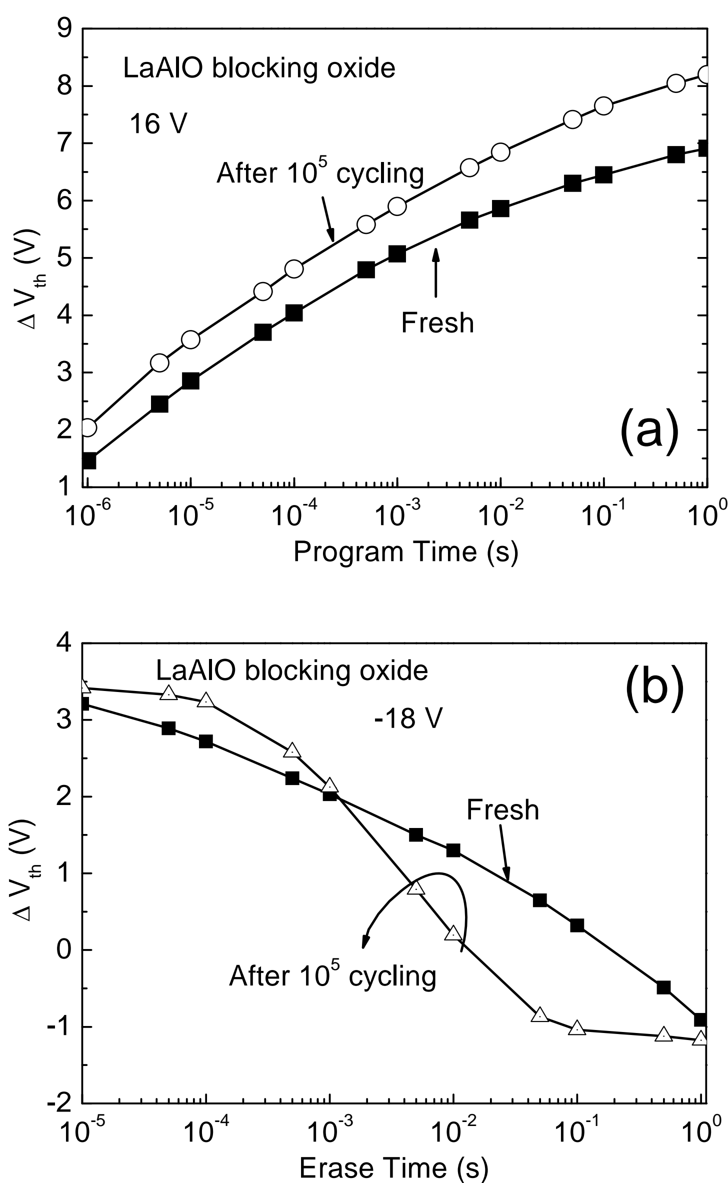

Fig. 4.13 A comparison of (a) programming and (b) erasing characteristics between the fresh and 100,000 times P/E cycled LaAlO memory cells.

This unusual behavior of V_{th} window narrowing is probably due to the presence of lanthanum in the blocking oxide. As discussed in Chapter 3, a vast negative flat-band voltage was observed when lanthanum was incorporated into the dielectrics. This vast negative flat-band voltage was widely believed to be due to the positive charges introduced by lanthanum element. By using such positive charges, the effective work function of nMOS transistors can be tuned to silicon conduction band edge [15, 16]. Similarly, we believe that the positive charges may also be accumulated in LaAlO films. Thus, these extra charges modify the programming and erasing behaviors.

4.4.2 HfLaO Memory Cells

$HfLaO_x$ films with different La percentages (30%, 54% and 82%) were evaluated as blocking oxide (HfLaO).

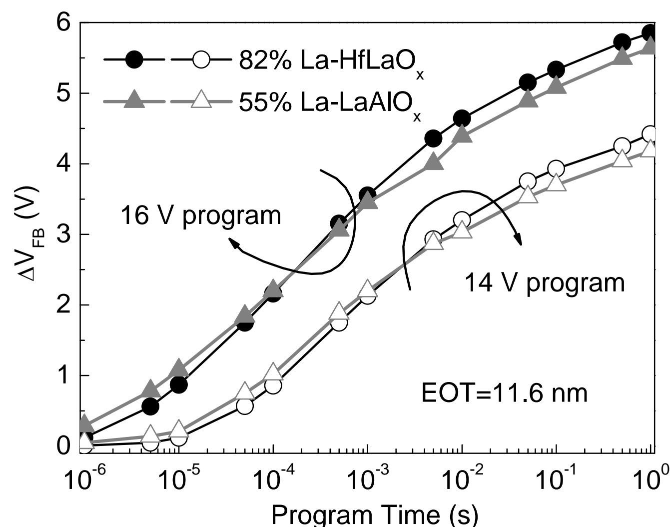

Fig. 4.14 A comparison of programming characteristics between HfLaO and LaAlO memory cells. The similar programming characteristics were observed.

Figure 4.14 compares the program characteristics of HfLaO, and LaAlO memory cells. Both types of memory cells had the same EOT_{total} (11.6 nm) and they showed comparable program speeds. Generally, HfLaO memory cells shows slightly wider V_{th} saturation window and more robustness to voltage stresses, which is attributed to the higher dielectric constant of $HfLaO_x$ (~22).

However, all HfLaO memory cells exhibited poor retention performance. Figure 4.15 compares the data retention of HfLaO and AlO memory cells at room temperature. It is obvious that the data retention of AlO memory cells is better than that of HfLaO memory cells. Furthermore, among HfLaO memory cells, the HfLaO blocking oxide with higher La percentage showed better data retention.

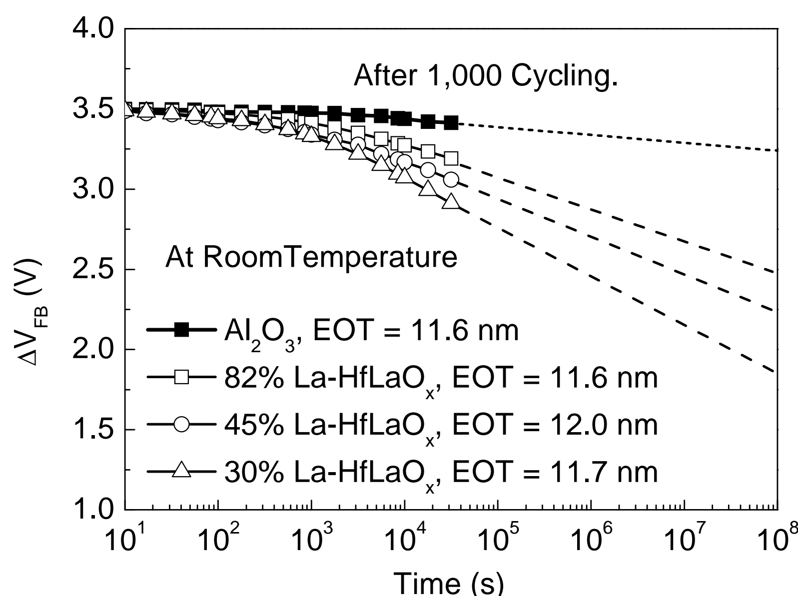

Fig. 4.15 Comparisons of data retention of HfLaO and AlO memory cells at room temperature. $HfLaO_x$ with higher La percentage exhibited worse data retention.

The dependence of data retention on La percentages is believed to be related to

the conduction band offset. The conduction band offset of Al_2O_3, $LaAlO_x$, and $HfLaO_x$ against Si are summarized in Fig. 4.16 [17, 18]. Among these dielectrics, Al_2O_3 has the highest conduction band offset, followed by $LaAlO_x$, then $HfLaO_x$. Among $HfLaO_x$ films, higher La percentage gives higher conduction band offset. This trend of conduction band offset is consistent with the trend of retention performance shown in Fig. 4.15, suggesting that the conduction band offset plays a key role in determining the data retention. It should be noted that the conduction band offset of Si_3N_4 against Si is 2.4 eV, which is lower than that of $LaAlO_x$ and Al_2O_3, but higher than that of $HfLaO_x$ dielectrics [19]. Thus, it is deduced that conduction band edge of replace blocking oxide is required to be greater than that of Si_3N_4.

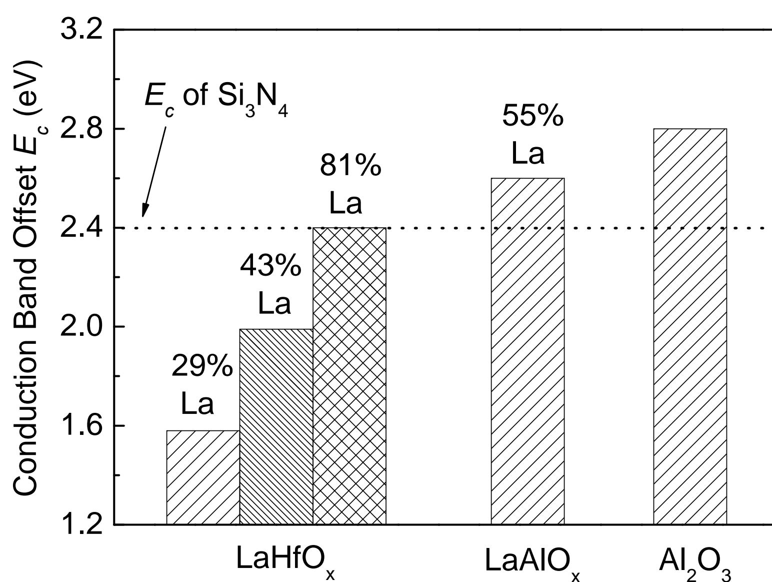

Fig. 4.16 Comparisons of conduction band edge of Al_2O_3, $HfLaO_x$ and $LaAlO_x$ films.

4.5 Charge Trapping Energy and Activation Energy

The performance of data retention is believed to be closely related to the charge trapping energy inside the nitride film. In order to calculate this trapping energy, several analytical retention models for SONOS-type flash memory cells at elevated temperatures have been proposed [10-12, 20]. By assuming a spatially uniform distribution of traps inside the nitride film, which can be true if FN tunneling is used to program or erase the memory cells, and considering the thermal excitation as the main charge loss mechanism at elevated temperatures, Yang and White derived an electron retention model to calculate trapping density in nitride film, $g(E_{TA})$, as a function of trapping energy, E_{TA}, for SONOS memory cells at high temperatures (>175ºC) [10]:

$$g(E_{TA}) = -0.435 \cdot \frac{\partial \Delta V_{th}}{\partial \log(t)} \cdot \frac{\varepsilon_0 \varepsilon_{SiO}}{q k_B T x_{SiN} (\frac{1}{2} EOT_{SiN} + EOT_{BLK})} \quad (7)$$

where t is the retention time, k_B is Boltzmann's constant, T is the absolute temperature (K), x_{SIN} is the physical thickness of nitride, EOT_{SIN} and EOT_{BLK} is equivalent oxide thickness of the nitride and the blocking oxide, respectively. E_{TA} is the maximum trapping energy (trapping depth) and is defined by P. J. McWhorter *et al*. as below [21]

$$E_{TA} = k_B T \ln(A T^2 t) \quad (8)$$

In equation (8), A is a constant given as [21]:

$$A = 2\sigma_n \sqrt{\frac{3k_B}{m^*}} \left[\frac{2\pi m^* k_B}{h^2} \right]^{3/2}$$

where σ_n is the trap capture cross-section, m^* is the effective electron mass in the nitride film and h is Plank's constant.

Using above equations and the data retentions taken at 175ºC, Yang and White showed the peak of trapping energy density distribution curve was located at 1.1 eV below the nitride conduction band edge [10]. However, this trapping density distribution curve is found to depend on the baking temperatures, thus resulting in different peak values. However, this is contrary to the expectation that the distribution curve of trapping energy should be constant for a certain memory cell. This expectation arises from an assumption during the equation (7) derivation that the emission sequence of charge traps followed a rule that the traps with shallower energy always emitted first and the traps with deeper energy remained unchanged. Therefore, the distribution of the trapping density would be constant and thus independent of the measurement temperatures. In order to solve this discrepancy, Kim *et al* modified the equation (8) by introducing a coefficient α as [20]

$$E_{TA} = k_B T \ln(\alpha \beta T^2 t) \quad (9)$$

where β is a coefficient of tunneling probability through the tunnel oxide or blocking oxide in considering of band-to-band tunneling and is defined as [20]:

$$\beta = \exp(-2\frac{t_{ox}}{\hbar}\sqrt{2qm_{ox}^* E_b})$$

where t_{ox} is the physical thickness of the tunnel oxide, m_{ox}^* is the tunneling effective

mass in SiO_2, and E_b is the barrier difference between the SiO_2 and the Si_3N_4. On the other hand, according to the emission rule mentioned above, coefficient α can be solved by convoluting of equation (9) at two different baking temperatures as [20]:

$$\alpha = (T_2^2 \beta t_2)^{[T2/(T1-T2)]} \Big/ (T_1^2 \beta t_1)^{[T1/(T1-T2)]}$$

By solving β and α, E_{TA} can be obtained. Using two types of memory cells with different tunnel oxide thicknesses and their retention data at 170ºC and 200ºC, Kim *et al* reported the peak of trapping density distribution curve was located at 1.2 eV [20]. However, during the calculation of coefficient β, it is inconvenient to obtain the exact value of the effective mass (m_{ox}^*) because this value was found to be process dependent and materials dependent. There were no consistent references about the effective mass in these new dielectrics, such as Al_2O_3 and $LaAlO_x$. Furthermore, it is difficult to extract the value from experiment's data.

In order to solve this difficulty of getting the exact value of effective mass, we further modified the equation (8) by using coefficient γ to replace coefficient α and β. Then the equation (8) is expressed as

$$E_{TA} = k_B T \ln(\gamma T^2 t) \qquad (10)$$

It is well-known that the tunneling current is not sensitive to the small change of the baking temperatures (from 180ºC to 250ºC). Thus, for a specified memory cell, the coefficient γ can be calculated by convoluting of equation (10) as

$$\gamma = (T_2^2 t_2)^{[T2/(T1-T2)]} / (T_1^2 t_1)^{[T1/(T1-T2)]} \tag{11}$$

Our modified equation does not require us to know the effect mass (m_{ox}^*) in new dielectrics during the calculation, thus it is more simple and accurate. Using the equations (7), (10) and (11) with data retentions taken at 190ºC and 233ºC, the trapping density as a function of trapping energy is plotted in Fig. 4.17.

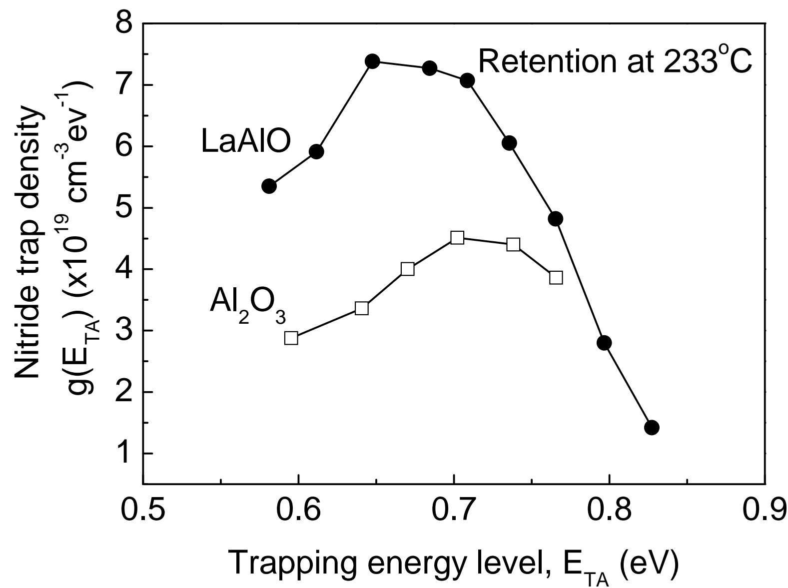

Fig. 4.17 Extracted value of nitride trapping density as a function of the trapping energy based on the data retentions of LaAlO and AlO memory cells at high temperatures. It shows that the trapping depth in nitride film is 0.6 to 0.75 eV below the nitride conduction band edge.

The trapping density distribution curves do not overlap each other between LaAlO and AlO devices because of the different rate of charge loss at high temperatures. The peaks of trapping density distribution for LaAlO and AlO memory cells are both located at 0.7 eV. As discussed before, the thermal excitation of LaAlO

memory cells is more dominant than that of AlO memory cells at 233ºC. This means LaAlO memory cells are more close to the presupposition of Yang's model. Thus, the trapping density curve of LaAlO should be more reliable. Therefore, the trapping energy depth in nitride film is extracted to range from 0.6 eV to 0.75 eV below the nitride conduction band edge. This range of nitride trapping depth is consistent with other groups' reports [22, 23].

The activation energy was also extracted from the shift of V_{th} using the retention data at various temperatures. Fig. 4.18 compiles the V_{th} shifts as a function of temperatures in Arrhenius plot. The activation energy of LaAlO memory cells is extracted to be 0.31 eV, which is higher than that of AlO memory cells (0.19 eV). The reason of higher activation energy of LaAlO is believed to be due to the thicker physical thickness. This result also indicate that the charge traps in LaAlO memory cells are more difficult to escape out, which is consistent with our observation of better retention of LaAlO at the lower temperature range (<120ºC). As we discuss previously, the charge loss at this range is dominated by tunneling mechanism. On the other hand, the impact of thermal emission also plays a role. By combining the tunneling effect and thermal emission effect, Frankel-Poole emission is used to derive the trapping energy depth. The trapping energy depth of nitride film is calculated to range from 0.53 eV to 0.65 eV below the nitride conduction band edge when varying the charge centroid from the nitride bottom to the nitride top surface. This range of trapping energy depth is comparable to the values calculated from our modified Yang's model.

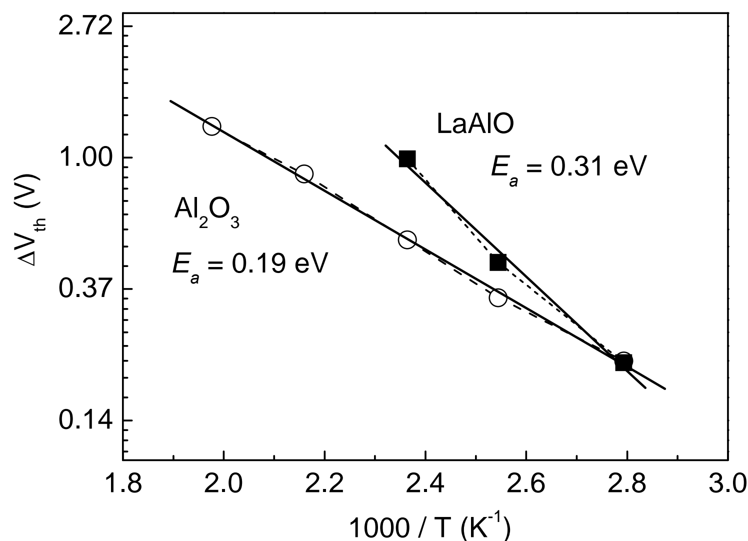

Fig. 4.18 Arrhenius plot of data retention as a function of temperatures for LaAlO and AlO memory cells. LaAlO memory cells exhibited greater activation energy.

In summary, the trapping energy depth in our nitride film is calculated to be within the range of 0.6 eV to 0.75 eV below the nitride conduction band edge, which is considered to be shallow traps. Therefore, it is no wonder that the retention performance is so sensitive to the value of conduction band offset of blocking oxide.

4.6 Conclusion

In summary, $LaAlO_x$ and $HfLaO_x$ have been systematically investigated for use as the blocking oxide in SONOS-type flash memory cells. Compared to AlO memory cells, both types of memory cells could provide faster program speed, wider saturation window, and improved breakdown characteristic. Furthermore, LaAlO memory cells show better retention performance than AlO memory cells when the temperature is below 120ºC, and especially at 85ºC. Therefore, if the device operation temperature is kept below 120ºC, $LaAlO_x$ will be a suitable candidate as the blocking oxide for further

performance improvement. On the other hand, $HfLaO_x$ shows bad retention performance due to the low conduction band offset of $HfLaO_x$ films. This is because the charges inside the nitride film are considered to be shallow traps. By using modified Yang's model, the trapping energy depth is calculated to range from 0.6 eV to 0.75 eV below the nitride conduction band edge.

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Chapter 5 Conclusion and Suggestions

5.1 Conclusion

In order to improve the performance of nitride-based SONOS-type flash memory, the role of lanthanum-incorporated high-κ dielectrics ($LaAlO_x$ and $HfLaO_x$) as a blocking oxide was investigated in this study, including the study of the deposition method, material characteristics, and memory characteristics.

Firstly, ALD deposition of $HfLaO_x$ and $LaAlO_x$ was studied. It was found that the deposition rate of La_2O_3 was greatly increased when an Hf or Al precursor was co-introduced into ALD chamber to form $HfLaO_x$ or $LaAlO_x$, respectively. The possible reason of this increased deposition rate is believed to be the suppression of lanthanum hydroxide formation. Both deposited $HfLaO_x$ and $LaAlO_x$ exhibited a strictly linear relationship between the film thickness and deposition cycles, suggesting a true ALD growth behavior. Another important ALD growth behavior – the self-limiting characteristic – was also observed. Higher cycle ratios of Hf:La or Al:La led to better self-limiting characteristics and better film uniformities (< 5%). In addition, the carbon impurities inside the deposited $HfLaO_x$ and $LaAlO_x$ film was found to be only 1 at.% and 0.6 at.%, respectively, indicating high quality ALD films.

The physical and electrical characteristics of ALD $HfLaO_x$ and $LaAlO_x$ have

been investigated. The crystallization temperature of $HfLaO_x$ increased as the La percentage increased. When La percentage was greater than 4%, $HfLaO_x$ crystallized to a cubic-like phase after annealing at high temperature. The permittivity of cubic-like phase $HfLaO_x$ was much higher than that of the dielectric in the amorphous or monoclinic phase. Especially when La doping percentage was around 8 at.%, the permittivity of crystallized $HfLaO_x$ can be as high as 38. This huge increase of permittivity benefited the overall leakage current performance. Under the same voltage stress, the leakage current was two orders of magnitude lower than that from the same EOT of amorphous film. Moreover, the annealing temperature needed to obtain optimum film property was dependant on the film thickness. Inadequate annealing temperature would decrease the permittivity. The decrease of permittivity is believed to be caused by the transformation of some cubic structures into monoclinic structures. In addition, $HfLaO_x$ films with higher La percentage showed higher conduction band offset and wider energy band gap.

In comparison with $HfLaO_x$, $LaAlO_x$ film exhibited a much higher conduction band offset and wider energy band gap. The permittivity of amorphous $LaAlO_x$ with 46% La was ~ 18. The amorphous films of $LaAlO_x$ could stand up to 850ºC anneal. Even higher annealing temperature would result in an interfacial layer with higher trapping density. This trapping interfacial layer is believed to be caused by phase separation. Using the XRD method, the phase separation of $LaAlO_x$ films was clearly observed when films were annealed at 1050ºC. In addition, ALD $LaAlO_x$ films deposited at 300ºC to 400ºC gave the optimum electrical performance.

Films of $LaAlO_x$ and $HfLaO_x$ were both applied in nitride-based SONOS-type flash memory as blocking oxides. In comparison with memory cells using Al_2O_3 as a blocking oxide (TANOS), both types of memory cells using $LaAlO_x$ and $HfLaO_x$ as blocking oxide exhibited higher program speed, wider saturation window, and improved time-to-breakdown (t_{BD}) characteristics. Furthermore, memory cells using $LaAlO_x$ blocking oxide showed much better retention performance than that of using Al_2O_3 blocking oxide when the baking temperature was below 120ºC, especially at 85ºC. Within this temperature range, the trap-to-band tunneling mechanism is believed to be the main charge loss mechanism. In most cases, the working temperature of memory cells is below 120ºC. Thus, $LaAlO_x$ will be a suitable candidate as blocking oxide to further boost the memory performance. In contrast to memory cells using $LaAlO_x$ blocking oxide, memory cells using $HfLaO_x$ blocking oxide showed bad retention performance due to the low conduction band offset of $HfLaO_x$ films. This is because the charges inside the nitride film are considered to be shallow traps. Using our modified Yang's model, the trapping energy depth was simulated to be 0.6 eV to 0.75 eV below the nitride conduction band edge. Furthermore, the conduction band edge of blocking oxide or tunnel oxide in nitride-based SONOS-type memory cells is needed to be greater than that of the nitride conduction band edge.

5.2 Suggestions for Future Work

In this study, many promising finding in regards to dielectrics and memory cells have been found and evaluated. However, there are still some issues to be overcome for

further performance improvement or eventual implementation in mass production.

First, our study showed that by using $LaAlO_x$ as a blocking oxide, an improved retention performance was achieved if the retention temperature was below 120ºC. On the other hand, if the retention temperature was greater than 120ºC, the retention degraded significantly due to the charge loss dominated by the thermal emission at high temperature. Thus, if we want to improve the retention performance at high temperature, the dielectrics with high conduction band offset will be needed. However, the dielectrics with such high conduction band offset are usually limited to SiO_2 and Al_2O_3, where the κ value is not high. So we proposed a double-layer structure to solve this quandary. One layer is desired to decrease tunneling probability by using an extreme high κ dielectric; the other layer is desired to minimize the charge loss caused by the thermal emission by using a high conduction band offset dielectric (like Al_2O_3). Besides the replacement of blocking oxide, another possible solution is to replace the nitride film with other types of trapping material with lower conduction band offset, such as HfO_2, AlGaN, etc [1, 2].

Second, the program-erase cycling endurance is always a big concern for SONOS-type flash memory. The P/E cycles results in a drift of threshold voltage for both program-state and erase-state. Normally, the threshold voltage of erase-state will trend up as the number of cycles increases [3]. However, our study showed a downward trend for erase-state when $LaAlO_x$ was used as blocking oxide. This downward trend is believed to be caused by the incorporation of lanthanum oxide. Thus, it is possible to

optimize the thickness of $LaAlO_x$ film or the concentration of incorporated lanthanum to flatten the erase-state trending. But, this only helps a little in improving the cycling endurance as the program-state still maintains an upward trending. Therefore, more efforts are needed to stabilize the program-state.

In addition, the etching of lanthanum-incorporated ternary dielectric is another challenging issue. In our experiment, we found the lanthanum-incorporated ternary dielectrics could only be etched away by wet chemical. But, the method of wet etching is not favored by industry, especially for small-size device patterning. In order to achieve a good etching profile, dry-etching method is required. However, dry etching of lanthanum is a big challenge when using conventional halogen gases because the compounds of halogen lanthanum are not easy to vaporize thus be purged away. Thus, a novel dry-etching process is needed for lanthanum-incorporated dielectrics.

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Appendix - List of Publications Related to This Thesis

A) Journals and Letters

1. ***Wei He***, Lu Zhang, Daniel S.H. Chan, and Byung-Jin Cho, "Cubic-Structured HfO_2 with Optimized Doping of Lanthanum for Higher Dielectric Constant", IEEE Electron Device Letters, v 30, n 6, 2009, p623-625

2. ***Wei He***, Jing Pu, Daniel S.H. Chan, and Byung-Jin Cho, "Performance Improvement for SONOS-type Flash Memory Using Lanthanum Based High-κ Dielectric as Blocking Oxide", IEEE Transactions on Electron Devices, Vol. 56, No. 11, 2009

3. ***Wei He***, Daniel S.H. Chan, Sun-Jung Kim, Young-Sun Kim, Sung-Tae Kim, and Byung-Jin Cho "Process and material properties of $HfLaO_x$ prepared by atomic layer deposition Source" *Journal of the Electrochemical Society*, v 155, n 10, , 2008, p G189-G193

4. Lu Zhang, ***Wei He***; Daniel S.H. Chan; Byung-Jin Cho, "Multi-layer high-κ interpoly dielectric for floating gate flash memory devices", Solid-State Electronics, v 52, n 4, April, 2008, p 564-570

B) Conference and workshop proceedings

1. ***W. He***, S. -J. Kim, Y. -S. Kim, B. J. Cho, "Electrical and Physical Properties of ALD HfLaO for CMOS Device Application". Material Research Society 2008 Spring Meeting, Symposium H, pp. 121.

2. ***Wei He***, Daniel S.H. Chan, and Byung-Jin Cho, "SONOS Type Memory Cell with ALD LaAlO Blocking Oxide for High Speed Operation". International Conference on Solid-State and Integrated Circuits Technology Proceedings, ICSICT, p835-838, 2008.

3. L. Zhang, ***W. He***, D. S. H. Chen, and B. J. Cho, "A Systematic Study of High-κ Interpoly Dielectric Structures for Floating Gate Flash Memory Devices". Proceedings on IEEE 2nd International Conference on Memory Technology and Design (2007), 223-226. Publication Number: 0354408

4. (Invited) B. J. Cho and ***W. He***, "ALD of HfLaO and AlLaO for Flash Memory Device Application", Proceedings on the 4th Korean ALD Workshop, pp. 99 – 115, Seoul, Korea, May 2008.