
# MULTIBIT DELTA SIGMA MODULATOR WITH NOISE SHAPING DYNAMIC ELEMENT MATCHING

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# Abstract

An xDSL (digital subscriber line) system requires a highly linear signal chain because the discrete multi-tone (DMT) modulation scheme is used. Thus the Delta-sigma modulators (ΔΣMs) in the xDSL receiver must have high-resolution and high-linearity as well. A multi-bit ΔΣM is preferred to fulfill these requirements. In practice, however, due to the device mismatch, the multi-bit digital-to-analog converter (DAC) in the feedback path of the ΔΣM, which is nonlinear, degrades the Spurious Free Dynamic Range (SFDR) of the ΔΣM. Dynamic element matching (DEM) techniques have been used to improve the linearity of the DAC. However, most of the existing DEM techniques reduce the spurious tones by spreading them over wide spectrum, resulting in an increased noise floor which degrades the SNR of the ΔΣM. In this way, there is a trade-off between SFDR and SNR.

This work proposes a new noise shaping DEM (NS-DEM) technique in an attempt to eliminate the trade-off between the SFDR and SNR of the ΔΣM with the existing DEM. The proposed NS-DEM can be incorporated into most of the existing DEM algorithms and provides noise shaping to the DAC noise while removing the nonlinearity error from the DAC. The proposed NS-DEM is analyzed, evaluated together with a lowpass multi-bit ΔΣM in behavior Matlab simulation, and verified in experiment, in which a dithered DAC employing NS-DEM is realized in a 0.35-μm CMOS process. The test result shows the first-order highpass noise shaping to the DAC noise. Furthermalre a $5^{th}$-order multi-bit lowpass ΔΣM with NS-DEM is realized in a 0.35-μm CMOS and achieves 94dB SFDR and 78dB DR in 2.2MHz BW and meets the ADSL2+ specifications.

# Acknowledgement

I am greatly indebted to Associated Professor Yong Ping Xu, my Ph.D advisor. I can never thank him enough for his unwavering support in various aspects during my five years' study at the National University of Singapore. Without his patience, professional expertise, and constructive and exhaustive suggestion for further revision, my Ph.D dissertation would not appear in its current form. I am grateful to all the professors whose intellectually-stimulating modules have inspired me a lot. My thanks also go to my classmates and friends for their companionship and intellectual sparkles. Among them, I would like to especially thank He Lin, who unreservedly exchanged his smart ideas with me and whose optimistic personality made me realize the importance of perseverance and the spirit of never giving-up even at the last moment. I also hope to thank all the lab assistants, who helped me for every small project. Last but not the least; I owe my gratitude to my family members, who had witnessed the development of my Ph.D project on a daily basis. My parents, though quite traumatized by the Sichuan Earthquake in their old age, encouraged me to finish my Ph.D dissertation and were ready to offer any kind of help they could afford. My wife Yan Du, the anchor of my life, also enthusiastically supported my study in a meticulous way while launching a blossoming career of her own.

# Table of Contents

# List of Figures

# List of Tables

# List of Acronyms

| | |
|---|---|
| ADC: | Analog-to-Digital Converter |
| ADSL: | Asymmetric Digital Subscriber Line |
| Bi-DWA: | Bi-Directional DWA |
| BW: | Bandwidth |
| CT: | Continuous-Time |
| CMFB: | Common-Mode Feedback |
| DAC: | Digital-to-Analog Converter |
| DEM: | Dynamic Element Matching |
| DFF: | D Flip Flop |
| DMT: | Discrete Multi-Tone |
| DSL: | Digital Subscriber Line |
| DT: | Discrete-Time |
| DWA: | Data Weighted Averaging |
| ΔΣM: | Delta-Sigma Modulator |
| DSP: | Digital Signal Processing |
| FF: | Feed-Forward |
| FS: | Full Scale |
| HPF: | High-Pass Filter |
| IDWA: | Incremental DWA |
| IIR: | Infinite Impulse Response |
| LSB: | Least Significant Bit |
| MSB: | Most Significant Bit |
| NS-DEM: | Noise-Shaping DEM |
| NS-DWA: | Noise Shaping DWA |
| NS-DTS: | Noise Shaping Dithered Tree Structure |
| NS-RAND: | Noise-Shaping Randomization |
| NS-PDWA: | Noise Shaping PDWA |
| NS-TS: | Noise Shaping Tree Structure |
| NTF: | Noise Transfer Function |
| OSR: | Oversampling Ratio |
| PDWA: | Partitioned DWA |
| RDWA: | Rotated DWA |
| PN: | Pseudo Noise |
| PSD: | Power Spectrum Density |
| PsDWA: | Pseudo DWA |
| RnDWA: | Randomized DWA |
| SFDR: | Spurious Free Dynamic Range |
| SNDR: | Signal-to-Noise and Distortion Ratio |
| SNR: | Signal-to-Noise Ratio |
| SQNR: | Signal-to-Quantization Noise Ratio |
| SC: | Switched-Capacitor |
| STF: | Signal Transfer Function |

# Chapter 1 Introduction

In the past decade, digital signal processing (DSP) capability in electronics has increased significantly, thanks to the fast growing integrated circuit technologies. As a result, the signal is preferred to be processed in the digital domain. However, the real world is analog in nature, in order to take the advantage of digital signal processing, the analog variables or signals around us need to be digitized first before they can be further processed in the digital domain. The device that performs digitization is analog-to-digital converters (ADCs), which encode the analog signal to a digital form. Nowadays, the ADCs are used in many electronic devices, such as hand phones, digital videos, digital cameras, and telephone modems. The requirements on ADC performance are application specific. Some required high resolution, while the others need wide bandwidth. Ideally an ADC should be able to perform A-to-D conversion without introducing any distortion to the original analog signal.

Many different types of ADCs have been proposed and reported for various applications. Among them, delta-sigma ADCs are able to achieve high resolution with less stringent requirement on the component mismatch. This is realized through the combination of oversampling and quantization noise spectrum shaping. The delta sigma ADCs have been widely used today in the applications that require medium to high resolution and low to medium bandwidth. In some applications, such as audio and xDSL (digital subscriber line) systems, in addition to the high resolution that is measured by its signal-to-noise ratio (SNR) of the ADC, high linearity is also required, which is measured by its spurious free dynamic range (SFDR). In xDSL, discrete multi-tone (DMT) modulation scheme is used and the DMT signal requires a highly

linear signal chain because any nonlinearity in the chain will incur the inter-modulation distortion which overlaps the sub-carries, badly interfering the sub-channels' signal. Thus the ADC in the xDSL receiver must be of high-resolution and high-linearity. So does in the high fidelity or hi-fi sound reproduction systems.

The single-bit delta-sigma ADC has a very good linearity performance with a simple structure, but the sampling frequency of the single-bit delta-sigma ADC is usually high in order to achieve high resolution. Multi-bit delta-sigma ADC, on the other hand, has inherent low quantization noise and hence low oversampling ratio can be employed to achieve the same resolution as compared to the single-bit architecture. Another advantage of the multi-bit quantization is that it offers good stability since the gain of the quantizer is well defined.

In practice, however, due to the device and component mismatch, the digital-to-analog converter (DAC) in the feedback path of the delta-sigma modulator is inherently nonlinear. As the DAC nonlinearity error cannot be suppressed by the loop filter, it distorts the input signal and degrades the linearity or SFDR of the delta-sigma ADC. Due to this reason, the advantages gained from the multi-bit quantization may be compromised by the non-idealities of the DAC.

Figure 1 shows the block diagram of a typical multi-bit delta-sigma modulator (ΔΣM). The multi-level quantizer output directly feeds back to the analog input through a multibit DAC. Any nonlinearity error from the multibit DAC is directly added to the summation node. This error, together with the input signal, will pass the ΔΣM without any suppression and directly affect the linearity of the ΔΣM.

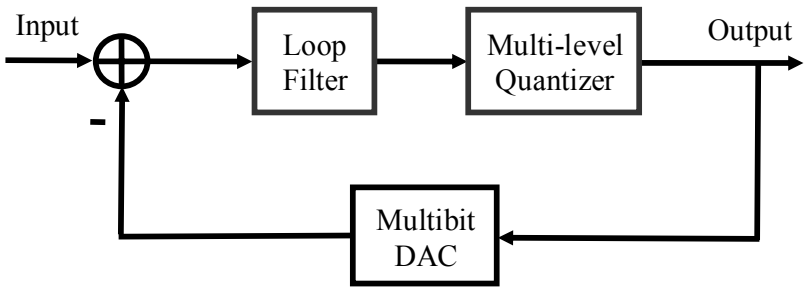


Figure 1. Block diagram of a typical multi-bit ΔΣM.

The most commonly used technique to reduce the nonlinear effects of DAC is the dynamic element matching (DEM). Figure 2 depicts the block diagram of a multi-bit ΔΣM with DEM. DEM randomly accesses the different DAC unit element and breaks the static nonlinear error. Most of the existing DEM techniques reduce the spurious tones by spreading them over wide spectrum, resulting in an increase of the noise floor. In other words, most of the existing DEM techniques trade SNR for SFDR or linearity.

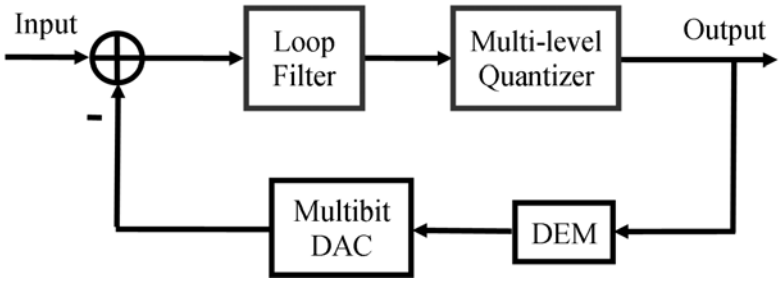


Figure 2. Block diagram of a multi-bit ΔΣM with DEM.

## 1.1 Motivation

The research in this thesis is aimed to develop a wideband lowpass multi-bit ΔΣM with high resolution and linearity. The targeted application is xDSL receivers. The research will particularly focus on how to reduce the DAC nonlinearity error and improve the linearity of the multi-bit ΔΣM.

## 1.2 Thesis Outline

The rest of the thesis is organized as follows. Chapter 2 introduces the fundamentals of ΔΣM. Chapter 3 reviews the prior scholarship on DEM. Chapter 4 proposes NS-DEM and evaluates its performance. Chapter 5 describes the design and measurement results of the ΔΣM that employs NS-DEM. Chapter 6 summarizes the original contribution of the research and suggests possible future work.

# Chapter 2 Delta-Sigma Modulation

This chapter introduces the different modulator structures and dynamic element matching (DEM), and reviews the previous works on DEM with an analysis of their limitation.

## 2.1 Quatization noise shaping technique

A/D conversion samples the input analog signal in time and quantizes it in magnitude. The conversion process has four steps, which is shown in Figure 3: anti-aliasing filtering, sampling and holding, and quantization.

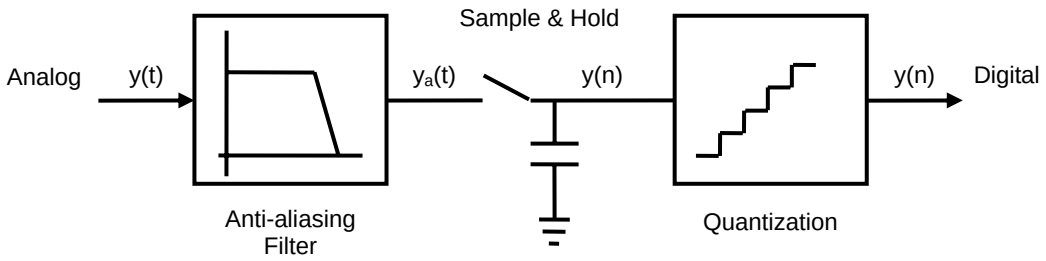


Figure 3. The conversion process of Nyquist-rate A/D converter.

### 2.1.1 Anti-aliasing

The analog signal goes through a lowpass anti-aliasing filter, which removes the signal components above half of the sampling frequency. Otherwise, high frequency components will be folded into the baseband and corrupt the in-band signal as soon as the signal is sampled.

### 2.1.2 Oversampling

Oversampling Ratio (OSR) is the ratio of the sampling frequency to the

Nyquist-rate. If the input signal bandwidth is $[0, f_B]$, OSR is defined as

$$OSR = f_s / 2f_B . \quad (1)$$

OSR is also defined as the sampling frequency over two times of the signal bandwidth (BW), for bandpass oversampling ADC,

$$OSR = f_s / 2BW . \quad (2)$$

Nyquist sampling rate is two times of the signal bandwidth. Generally in practice, to alleviate the constraints on anti-aliasing filters, OSR should be greater than one. OSR of the Nyquist-rate A/D converter is slightly higher than one and the digital output rate equals the sampling rate. For the oversampling A/D converter, OSR is much higher than the Nyquist rate and digital filter is used to decimate the high-rate bit stream to Nyquist rate and remove the out-of-band quantization noise.

As the sampling frequency is much higher than Nyquist rate, the constraints on anti-aliasing filter is alleviated. The sharp cut-off filter is not need to remove the out-of-band quantization noise, which makes it much easier to implement the filter on-chip.

## 2.1.3 Quantization noise

### 2.1.3.1 Quantization noise in Nyquist-rate ADC

When an analog signal is sampled and held, it is converted to digital value by a quantizer. This process is called quantization. Figure 4 shows the block diagram of the quantization in an N-bit A/D converter [2], where $B_{out}$ is the digital output word, while $V_{in}$ is the analog input signal and $V_{ref}$ is the reference signal. $b_n$ and $b_1$ represent the least significant bit (LSB) and most significant bit (MSB), respectively.

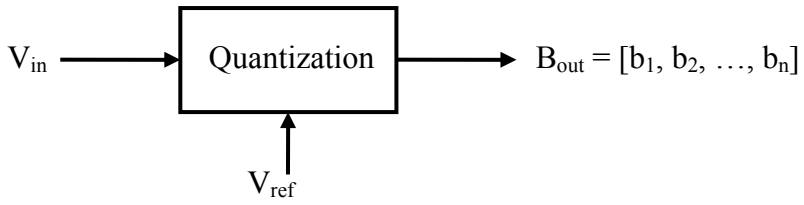


Figure 4. Block diagram of quantization in an N-bit ADC.

$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + ... + b_n 2^{-n}) = V_{in} + e \tag{3}$$

where $-V_{LSB}/2 \leq e \leq V_{LSB}/2$, $e$ is quantization error. It's difficult to analyze the quantization error due to its non-linearity and signal dependence. However, the quantization error can be approximated to an additive white noise and analyzed with statistical methods, if the following conditions are satisfied [3] [4]:

1) The input signal never overloads the quantizer.
2) The quantizer has a large number of quantization levels.
3) The input signal is active over many quantization levels.
4) The joint probability density of any two quantizer input samples is smooth.

Then the analysis is simplified. With the additive white noise assumption, the non-linear quantizer can be modeled as a linear system shown in Figure 5.

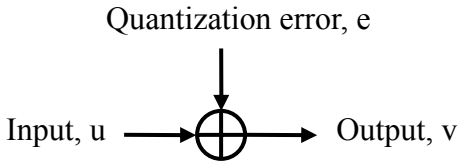


Figure 5. Linear model for quantization.

The output v is a combination of the analog input $u$ and uncorrelated white quantization noise $e$

$$v = u + e. \tag{4}$$

This additive white noise assumption is never precise because the quantization error is correlated with input signal and is too complex to be expressed analytically. However, in most cases, this linear model gives us reasonable predictions in analyzing the performance of a quantizer.

With the additive white noise assumption, if the quantization step is defined as Δ, the power of quantization error can be expressed as [2]

$$e^2 = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12}. \tag{5}$$

With a sampling frequency of $f_s$, the quantization noise will alias into the band of $[0, f_s/2]$. The spectral density of the sampled quantization noise is given by

$$E(f) = \sqrt{\frac{e^2}{f_s/2}} = e\sqrt{\frac{2}{f_s}}. \tag{6}$$

For a sinusoidal input signal with a full-scale magnitude of $V_{FS}$, the ac power of the sinusoidal input signal is $V_{FS}^2/8$. For $2^N >> 1$, the LSB is

$$1LSB = \frac{V_{FS}}{2^N - 1} \approx \frac{V_{FS}}{2^N} = \Delta, \tag{7}$$

where N is the bit number of the quantizer.

The SQNR (Signal-to-Quantization Noise Ratio), the ratio of signal power to the power of in-band noise, is given by

$$SQNR = 10\log_{10}\left(\frac{V_{ref}^2/8}{\Delta^2/12}\right) = 6.02N + 1.76dB. \tag{8}$$

**2.1.3.2 Quantization noise in oversampling ADC**

Oversampling A/D converter can achieve higher resolution than Nyquist-rate A/D converter. The in-band noise of an A/D converter is

$$n_{ib} = \int_0^{f_B} E^2(f)df = e^2 \frac{2f_B}{f_s}. \quad (9)$$

where E(*f*) is the spectrum density of the quantization noise.

For a Nyquist-rate ADC, $f_s=2f_B$, thus $n_{ib} = e^2$.

For an oversampling ADC,

$$n_{ib} = e^2 \frac{2f_B}{f_s} = \frac{e^2}{OSR} = \frac{\Delta^2}{12OSR}. \quad (10)$$

The Eq. (10) shows that the in-band noise can be reduced by increasing OSR. By doubling of OSR, the in-band noise power can be reduced by 3dB, which is equivalent to a half bit.

However, this SQNR improvement is not so significant. A noise-shaping technique should be employed to further improve the in-band SQNR. The noise-shaping technique shapes the quantization noise out of the band of interest. The oversampling A/D converter using the noise-shaping technique is called ΔΣADC.

### 2.1.3.3 Noise-shaping technique of ΔΣM

ΔΣM was first proposed by Inose and Yasuda in 1962 [5]. ΔΣM uses the feedback to improve the effective resolution of a coarse quantizer. Figure 6 illustrates the block diagram of a ΔΣM.

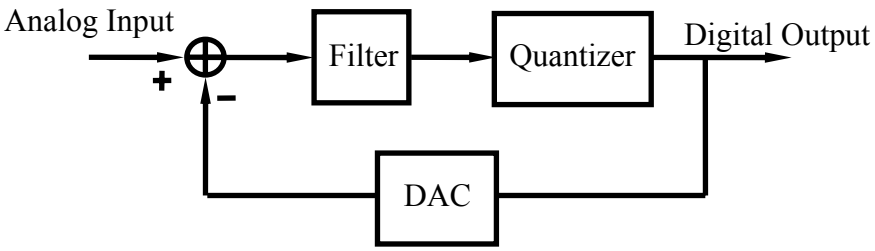


Figure 6. ΔΣM block diagram.

A ΔΣM consists of a loop filter, a quantizer, and a DAC in the feedback loop. The ΔΣM modulates the analog input signal into a digital sequence, which matches the analog input very well within the interested frequency band. The loop filter with the feedback structure shapes the quantization noise out of the signal band. Therefore, ΔΣM has the high in-band resolution.

By applying the linear model of the quantizer discussed in Section 2.1.3.1, a linear model of the ΔΣM is shown in Figure 7. *H(z)* is the transfer function of the loop filter in the *Z*-domain.

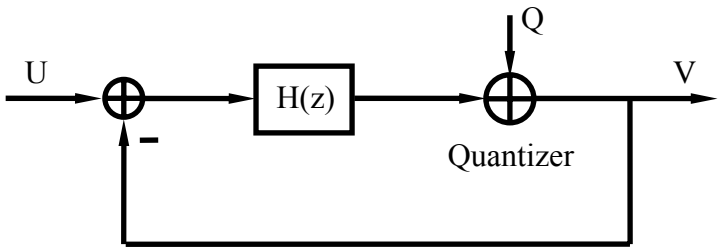


Figure 7. Linear model of ΔΣM.

The quantization noise is an additive white noise and independent of input signal, *U*, in the linear model. Then, the output of the modulator can be formulated as

$$V(z) = STF(z) \cdot U(z) + NTF(z) \cdot Q(z), \tag{11}$$

where the signal transfer function is

$$STF = \frac{H(z)}{1 + H(z)}; \tag{12}$$

and the noise transfer function is

$$NTF = \frac{1}{1 + H(z)}. \tag{13}$$

The poles of *H(z)* are also the zeros of *NTF* as indicated by Eq. (13). At the frequencies which satisfy $H(z) \gg 1$, $y(z) \approx x(z)$. It means that at these frequencies the signal goes through the loop while the quantization noise is shaped away from these frequencies. Such a technique that shapes the spectrum of the noise is called noise shaping.

For the 1st-order lowpass ΔΣM, in which H(z)=1/(z-1), the in-band noise can be calculated as follows:

$$\begin{aligned} e_{ib}{}^2 &= \int_0^{f_b} e^2(f)\left|\frac{z-1}{z}\right|^2 df \\ &= \int_0^{f_b} \frac{e^2}{f_s/2}\left|1-z^{-1}\right|^2 df \\ &= \int_0^{f_b} \frac{\Delta^2/12}{f_s/2}\left|1-e^{-j\omega T_s}\right|^2 df \\ &= \int_0^{f_b} \frac{\Delta^2/6}{f_s}(2-2\cos\frac{2\pi f}{f_s})df \\ &= \frac{\Delta^2}{12}\frac{\pi^2}{3}\frac{1}{OSR^3} \end{aligned} \quad (14)$$

,

where $f_B$ is the signal bandwidth (BW) and approximating $f \ll f_s$ and $\sin(\pi f/f_s) \approx \pi f/f_s$.

Obviously, doubling of OSR leads to SQNR 9dB improvement, equivalent to 1.5bit. The increase is much higher than that of the oversampling converter without noise-shaping as suggested by Eq. (10). Therefore, high OSR is desirable in ΔΣM as shown in Eq. (14).

Figure 8 shows a complete block diagram of baseband ΔΣ ADC. The ΔΣ ADC consists of a ΔΣM and a digital decimation filter. The decimation filter filters out the out-of-band quantization noise and decimates the high-rate bit stream into Nyquist rate data.

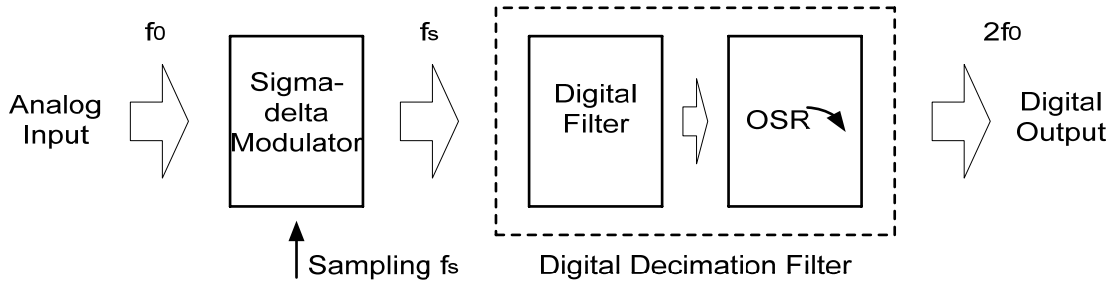


Figure 8. Structure of baseband ΔΣ A/D converter.

## 2.2 Delta-Sigma Modulator

### 2.2.1 High-order Delta-Sigma Modulator

In the previous section, the noise transfer function has been reviewed. Generally speaking, the order of the modulator is the order of its noise transfer function. High-order modulators result in more aggressive noise-shaping. For the L-order lowpass ΔΣM $H(z)=1/(z-1)^L$, the SQNR can be calculated as follows:

$$\begin{aligned} SQNR &= 10\log(2^{2N}\cdot\frac{3}{2}\cdot\frac{2L+1}{\pi^{2L}}\cdot OSR^{2L+1}) \\ &\approx 6.02N+1.76-10\log(\frac{2L+1}{\pi^{2L}})+(2L+1)10\log(OSR) \end{aligned} \tag{15}$$

It shows that, for an Lth-order lowpass modulator, (*6L+3*) dB SQNR can be improved when doubling the OSR [6].

One method to realize high order ΔΣM is to directly use high order filters and only one quantizer in the forward path of the modulator loop. This architecture is called single-stage ΔΣM. Figure 9 shows a $2^{nd}$-order single-stage lowpass ΔΣM [7]. The single-stage ΔΣM with a loop filter higher two order is not unconditionally stable.

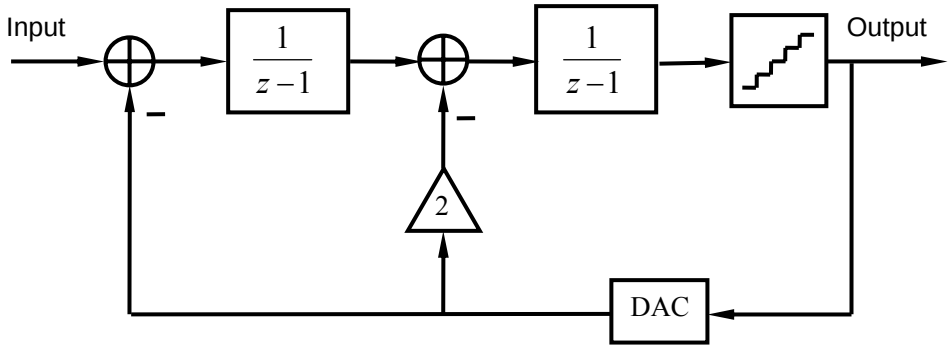


Figure 9. 2nd-order single-stage lowpass ΔΣM.

The other method is to use multi-stage structure (typically called MASH, for multi-stage noise-shaping [8]). Figure 10 shows a second-order lowpass MASH ΔΣM [7]. The output can be expressed as

$$V(z) = U(z) + (1 - z^{-1})^2 \cdot Q(z) . \tag{15}$$

The 1st-order shaped quantization noise from the first stage is offset by the second stage and 2nd-order noise-shaping is achieved. In theory, the structure can be extended to high-order noise-shaping with unconditional stability becasuse each 1st-order stage is unconditionally stable. However, mismatches between components in the stages result in imperfect noise cancellation [9].

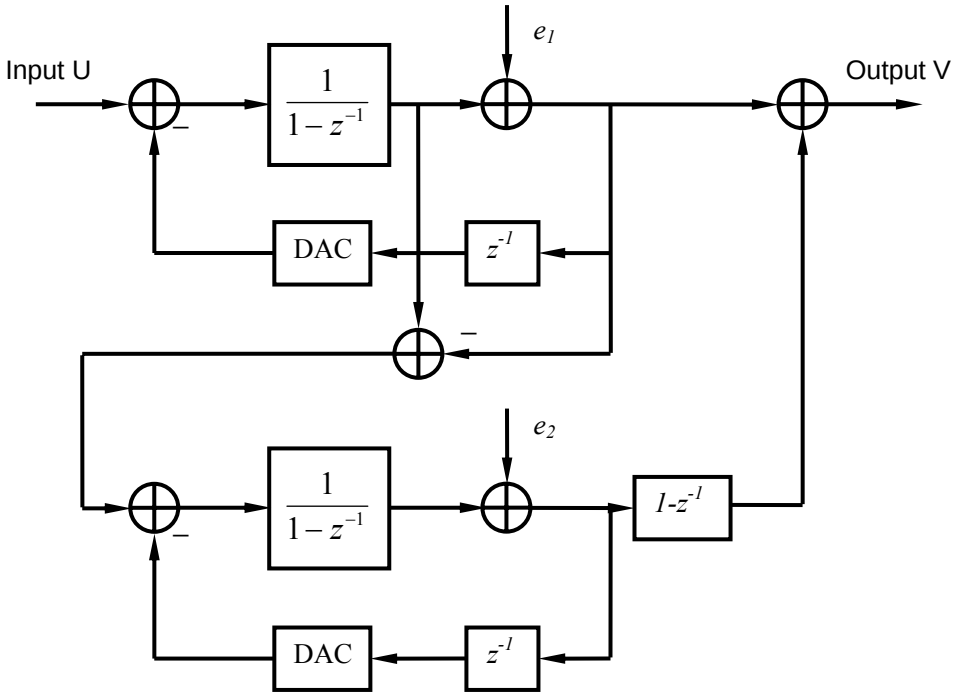


Figure 10. 2nd-order lowpass MASH ΔΣM.

### 2.2.2 Continuous-time v.s. Discrete-time

Discrete-Time (DT) ΔΣM refers to the ΔΣM which is mostly implemented with discrete-time switched-capacitor circuit [10] [11]. If the loop filter is realized with Continuous-Time (CT) circuit, such as *RC* or $G_mC$ form, the modulator is called continuous-time ΔΣM. As a result of different types of loop filter, the sampler position and the operation of the feedback DAC are different from each other. The sampler of DT is at the front end of the ΔΣM's loop filter, while the CT ΔΣM samples the signal at the quantizer. The DAC of CT ΔΣM output is the continuous-time analog signal, while it is the discrete-time analog signal in the DT ΔΣM.

DT ΔΣMs have robust performance and can be easily analyzed in Z-domain [11]. More aggressive noise shaping can be achieved by DT ΔΣM rather than CT ΔΣM. Implemented by Switched-Capacitor (SC) technique, the coefficients (capacitor ratios) of the loop filter can be precisely defined. But the operating frequency of ΔΣM is

limited by the settling time of the circuit. This makes the discrete-time ΔΣM unable to process high-frequency signals and also limits the maximum OSR that can be achieved in practice. The sampling frequency of most reported discrete-time ΔΣMs are below 200MHz.

Not constrained by the settling time problem, continuous-time ΔΣMs are suitable for high-speed applications. The continuous-time modulators also have the advantage of inherent anti-aliasing [13], which alleviates the constraints on the anti-aliasing filter. However, the CT ΔΣM is more sensitive to the clock jitter than the DT ΔΣM.

### 2.2.3 Feed-forward v.s. Feedback

For the loop filter in ΔΣM, there are mainly two structures, namely feed-forward and feedback. The feed-forward structure of the filter has only one feedback branch, while the feed back one has more than one branch.

Feed-forward structure is usually preferred in latest designs due to its two advantages over the feedback one. One is that the internal node of the feed-forward filter is scaled down compared with the feedback one [14]. This allows the design of the filter's building block, such as the OTA, to be relaxed. Large dynamic range is no longer needed. Other requirements for the OTA, such as power consumption, gain, and transistor size, can also be relaxed to some degree.

The other advantage is that the noises at the internal nodes of the filter can be attenuated by the gain of the preceding blocks [15].

### 2.2.4 Multi-bit v.s. Single-bit

ΔΣM can use single-bit quantizer to take advantage of its good linearity, but the ΔΣM with one-bit quantizer is likely to have idle tones and stability problem. In most of the latest published designs, multi-bit quantizer is used to increase the resolution

and improve the stability, especially for the high-order modulators. However, the main drawback of multi-bit ΔΣM comes from the nonlinear multi-bit feedback DAC.

Due to the device mismatch, there is nonlinearity in monolithic digital-to-analog converters (DAC). To put it another way, the transfer characteristic from digital to analog domain is nonlinear. Such nonlinearity errors cause distortion in the analog signal and degrade the performance of the DAC. This nonlinearity, together with other noises, such as the thermal noise, is generated inherently by the DAC. In multi-bit ΔΣM, the digitized signal needs to be converted back to analog domain in the feedback path through an internal DAC and subsequently subtracted from the input signal. If the feedback signal contains noise, it will degrade the performance of the ΔΣM as the noise from the internal DAC directly passed through the ΔΣM without being suppressed. Thus, the advantage gained from multi-bit quantization cannot be attained.

### 2.2.5 DAC Linearity Issue

An ideal DAC converts a sequence of digital codes to the same sequence of values represented by analog signals (typically currents or voltages). In practice, the DAC introduces errors that cause the value of analog signal to differ from the ideal values that correspond to the input digital codes. This conversion error makes the DAC nonlinear and hence gives rise to the signal distortion which degrades the overall ΔΣM performance.

To improve the linearity of the multibit DAC, some techniques have been proposed in previous works. They pertain to three categories, the calibration approach, the dual-quantization technique, and Dynamic Element Matching (DEM) technique.

#### 2.2.5.1 Calibration Technique

In the calibration technique, the DAC unit element can be calibrated in the analog

domain. Different methods can be employed, depending on the implementation of the DAC. Resistor elements can be laser-trimmed in the fabrication, but this requires a high cost. Current cells can be trimmed by changing the gate voltage of the transistor [16] or by combining coarse DAC with a fine DAC for calibration [17]. Capacitor can be calibrated by switching on or off small additional capacitors [18]. In general, this method incurs additional cost to the chip fabrication. In addition, both factory-trimming and calibration at startup may also suffer from the element matching variations due to age and temperature. Although this problem can be solved by periodical or continuous background calibration, the circuit complexity and cost are greatly increased [19].

The DAC calibration performs not only in the analog domain but also in the digital domain. Figure 11 shows the ΔΣM with the digital correction circuit [20] [21]. The digital correction circuit uses M-bit digital signal to accurately represent the N-bit DAC analog output. M is much larger than N to get more accurate digital correction result. In the conventional ΔΣM, the N-bit DAC output spectrum should match the input spectrum. Therefore, the M-bit digital correction output will match the input spectrum more accurately than the N-bit output of the ADC.

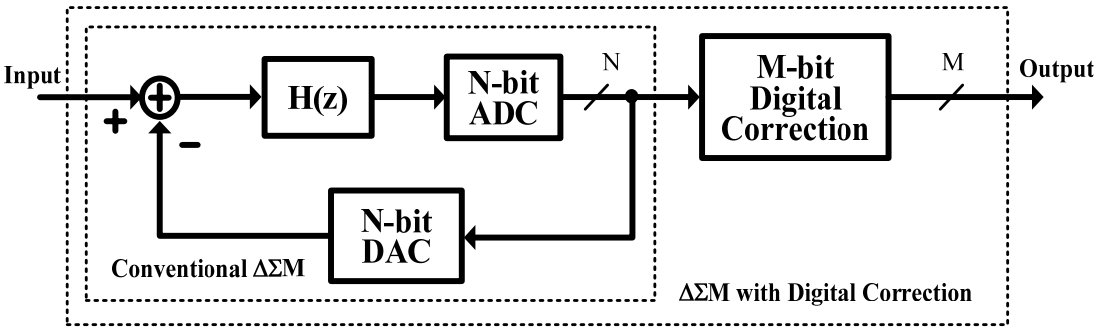


Figure 11. ΔΣM with digital correction.

#### 2.2.5.2 Dual-Quantization Technique

The dual-quantization technique can suppress the DAC nonlinearity in the ΔΣM. This technique combined single and multi-bit quantization in one converter. The 1-bit DAC converted the output of the single-bit quantizater and feedback to the input of the ΔΣM. The single and multi-bit quantizer outputs were combined together as the final output of the ΔΣM. Thus the basic idea was to combine the virtues of the reduced quantization noise of the multi-bit quantization and the intrinsic linearity of the single-bit DAC. The Leslie-Singh architecture [22], the single-loop dual-quantization architecture [23] [24] and the cascaded dual-quantization architecture [25] [26] [27] [28] were proposed. Figure 12 shows the architecture of a 2$^{nd}$-order single-loop dual-quantization ΔΣM.

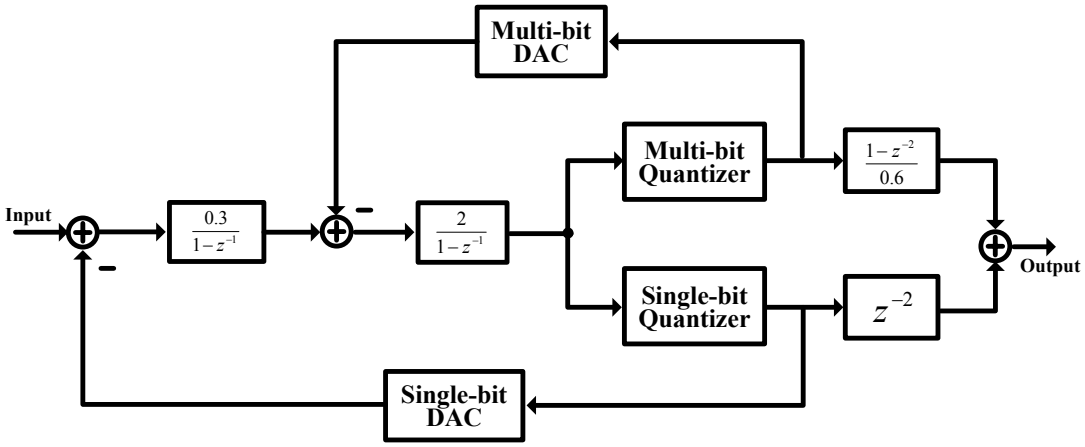


Figure 12. A single-loop dual-quantization ΔΣM architecture.

The main benefit of this architecture is the increased performance over a single-bit design without the stringent linear requirement for the multi-bit feedback DAC. Although this topology needs a multi-bit DAC in the feedback loop, the influence of non-linearity is reduced by the gain of the preceding integrators. However, the dual-quantization ΔΣM architecture is not a full multi-bit structure after all and the performance of these three architectures is significantly worse than a full multi-bit

structure [29]. The noise from the single-bit quantizer is offset by the digital filter followed by the quantizers. However, the noise cancellation by the digital filters is not complete if the integrator of the ΔΣM has any non-ideality, so the noise leakage is another drawback of the dual-quantization ΔΣM architecture.

#### 2.2.5.3 DEM

The third technique is based on Dynamic Element Matching (DEM). With DEM, excellent integral and differential linearity can be achieved, while only modest matching of the components is required. The DEM technique has been employed to reduce the internal DAC nonliearity error in the ΔΣM, albeit it was first introduced to improve the DAC accuracy [30] [31] [32] [33]. In the next Chapter, Various DEM techniques will be reviewed in details.

# Chapter 3 Dynamic Element Matching

Instead of reducing the power of the conversion error, the DEM techniques fransform the distribution of the error power to a random, wide-band, or even spectrally shaped noise, thus filtering a large amount of the out-of-band error out.

## 3.1 DEM Principle

The principle of DEM is illustrated in Figure 13. The thermalmeter internal DAC with DEM technique usually consists of two parts: a parallel unit-element digital to analog conversion structure and an element selection logic, which shuffles and selects the DAC corresponding unit-elements, of which the input is thermalmeter-code. In a conventional DAC without DEM, each of these lines controls one specific unit element of the DAC. Due to fabrication process variations, the values of these unit elements will not be equal and the DAC will introduce nonlinearity errors. This mismatch among the unit-elements plays a large part in the nonlinearity conversion error. The resulted noise, denoted by “mismatch noise”, is dependent on the element selection. The basic idea of the DEM technique is to use certain element selection algorithm to manipulate the power spectrum of the mismatch noise.

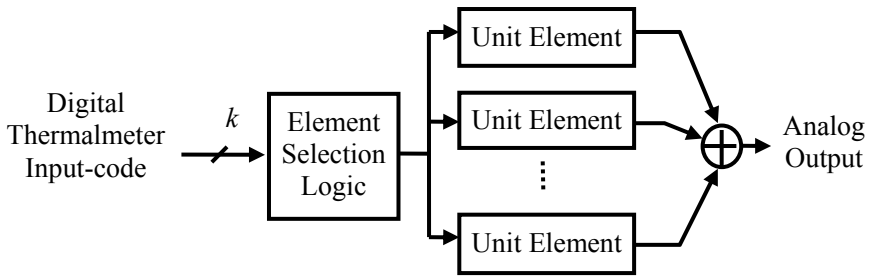


Figure 13. The DEM principle.

When DEM is employed, this one-to-one correspondence is interrupted by the element selection block. Hence, the element selecting block selects different unit

elements to represent a certain input code. Instead of having a fixed error for this certain input code, in each clock period a time-varying error signal will occur, because some of the unit elements have a positive contribution to the error, while the others have a negative contribution. The element selection logic makes this time-varying error introduced by DAC to be zero in average over multiple clock periods. The averaged output now approaches the ideal output. In other words, the errors due to component mismatch are whitened in a wide frequency band or moved out of signal band. Therefore, the error falls outside the signal band and can be removed by filter, when the DAC is over sampled [34]. The averaged output is a few orders of magnitude better than the accuracy of an individual unit element [35]. The output spectrums of the modulator without and with DEM are shown in Figure 14 in the grey and black color.

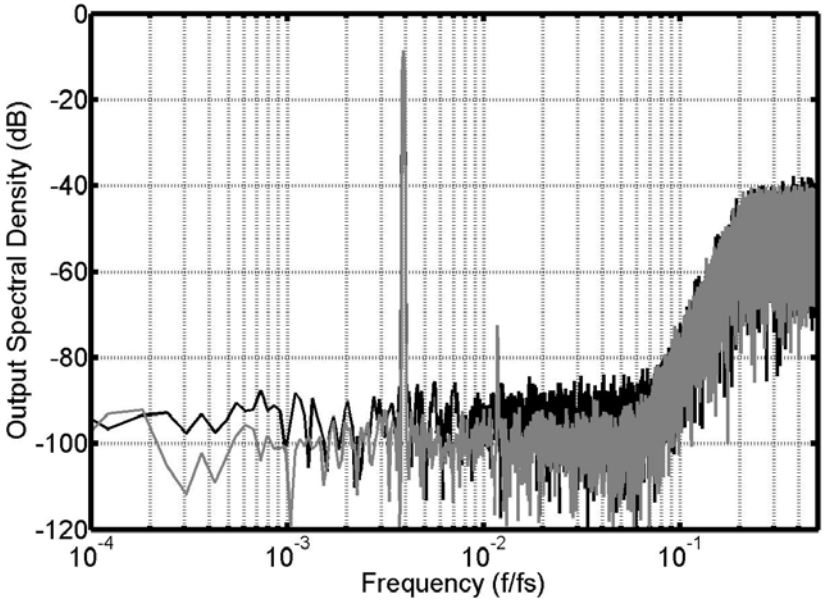


Figure 14. ΔΣM's output PSD with and without DEM.

The advantage of DEM is that, in contrast to calibration techniques that require an exact measurement of each unit element to compensate for the errors, it doesn't require the knowledge of the actual mismatch of the unit elements. Therefore, DEM is less sensitive to matching variation due to age and temperature.

## 3.2 Three widely used DEMs

In this section, three widely used categories of DEMs, namely randomization, DWA (data weighted averaging) and tree-structure, are reviewed and evaluated with a $5^{th}$-order 4-bit lowpass ΔΣM in Matlab using a Delta-Sigma toolbox[35]. The zeros of $NTF_Q$ are set at DC. Assumed to be thermalmeter coded, the DAC nonlinearity is added as follows. The unit element value is randomly generated with 0.5% standard deviation. The in-band noise floor of the ΔΣM is dominated by DAC noise; the quantization noise is well below the DAC noise floor; and kT/C noise is not included in the simulation. In all cases, the OSR is fixed at 16 in calculating the SNDR. The evaluation is done using by Matlab simulation. The signal-to-noise and distortion ratio (SNDR) and Spurious Free Dynamic Range (SFDR) are used as the benchmarks for the system performance comparison. SFDR indicates the linearity performance of the ΔΣM.

### 3.2.1 Randomization

The decoder with dynamic element randomization algorithm is sometimes called "randomizer". It picks up the elements randomly to represent a particular digital input. The goal of this approach is to convert the mismatch noise from a static nonlinear error to a dynamic wide band "white" noise, which can be partially removed by filtering in an over-sampling converter. With ideal randomization, a mismatch noise becomes a white-noise signal with a mean value of zero.

ΔΣM employing the DAC with DEM was first reported in [37][38]. A three-stage eight-line butterfly randomizer is used to randomly select unit elements. The dc-error and harmonic distortion components in this modulator are spread across the frequency band. Thus the tone related noise power is reduced, but the noise floor is increased.

The advantage of using DEM DAC in ΔΣM is that the Signal-to-Noise-and-Distortion Ratio (SNDR) is improved while the Signal-to-Noise Ratio (SNR) is degraded due to the increased noise floor. In the behavior simulation, the DAC unit elements are randomly selected. Figure 15 shows the ΔΣM's output PSD (Power Spectrum Density) with Randomization DEM. Figure 16 and Figure 17 show the SNDR and SFDR of the ΔΣM with Randomization DEM respectively. The ΔΣM is quite linear and there is no obvious tones and harmonic, because SFDR and SNDR are very linear with respect to the input level.

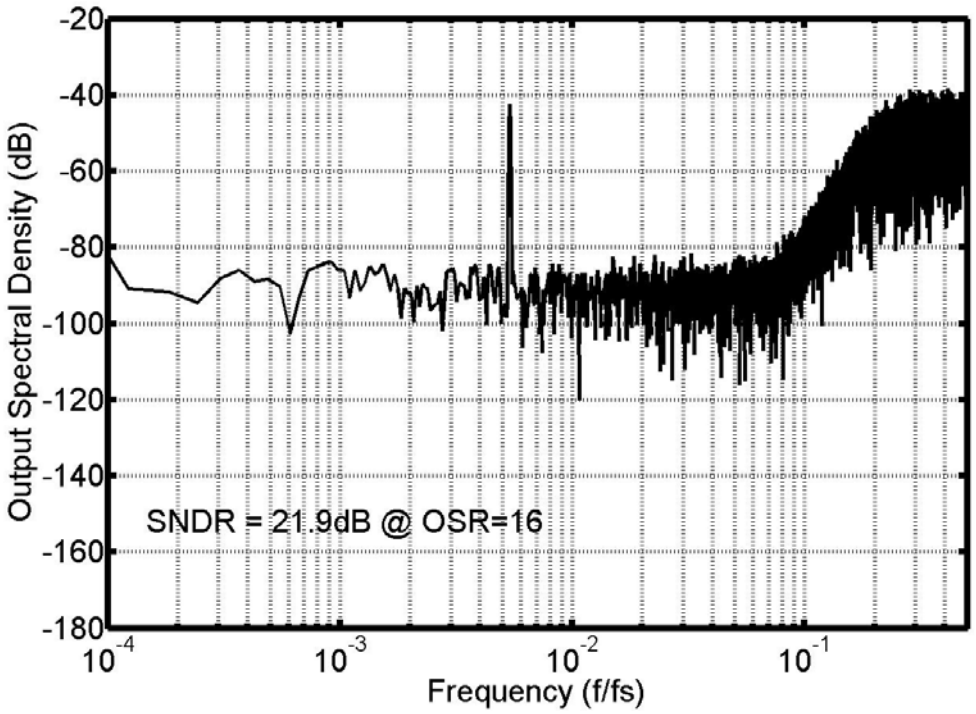


Figure 15. ΔΣM's output PSD with Randomization DEM.

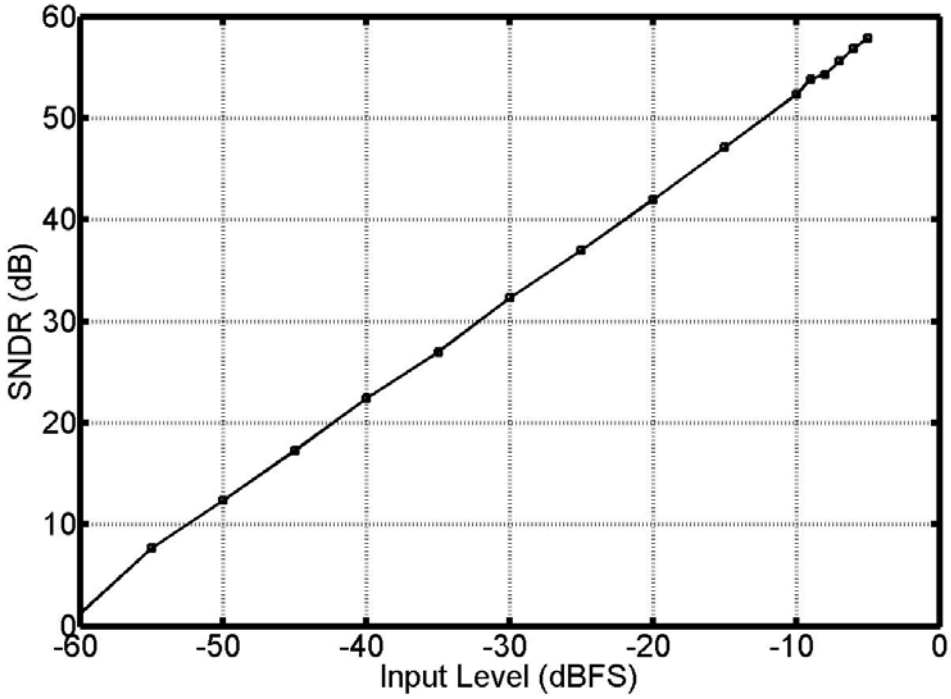


Figure 16. SNDR of the ΔΣM with Randomization DEM.

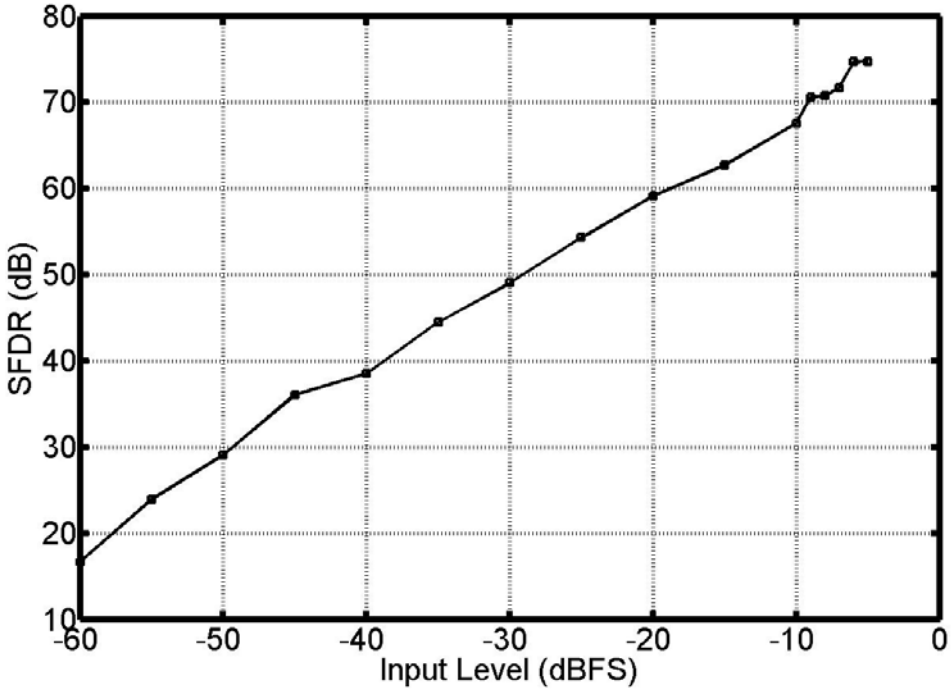


Figure 17. SFDR of the ΔΣM with Randomization DEM.

### 3.2.2 Data Weighted Averaging

Another most widely used algorithm for DEM is the Data Weighted Averaging (DWA) [34]. The basic concept of DWA is to guarantee that each of the elements is used with equal probability for each digital input code. This is realized by sequentially selecting elements, beginning with the next available unused element. The operation principle is illustrated in Figure 18. K[n] denotes the DAC input at clock cycle n. In the 1st clock twelve unit elements are selected. Then in the next clock the elements are selected from the first unused, that is the 13th element. If the last element is selected, DWA will start to select the 1st one again. The DAC unit elements are selected in rotation.

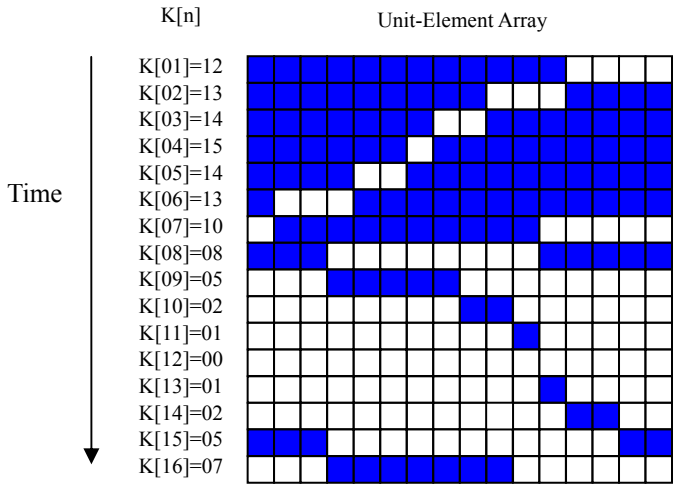


Figure 18. The DWA operation principle

The averaging of the element access rate is controlled entirely by the input data sequence. That is why this algorithm is referred to as “data weighted averaging”, denoted by “DWA”. With DWA, no unit-element is selected in an inordinate number of times even in a short time interval. For the constant input, this means that in the shortest time, every element can be selected once to represent the particular input code. Due to the equalized element access rate, the operation points can be symmetric

around the respective point on the characteristic line within the shortest time period. The symmetry means that the nonlinearity error is averaged out. For a better illustration, an M-element DAC is analyzed. When the input code is K, it takes only (M/K) uses of that particular code, and all unit-elements can be used once and (M/K) operation points are located symmetrically around the characteristic line. When M and K are relatively prime, it then needs M uses to equalize each element's access times. When M and K have common factors, the required number of uses will be smaller.

When the digital input is not constant, the analysis becomes complicated. The points on the characteristic line can be considered as $KI_a$, where K is the represented digital code and $I_a$ is the average value of the unit-elements. The non-linearity error can be expressed in terms of the deviation between the average value $I_a$ and the actual value of each element. The sum of such deviations is zero. Therefore, when all unit-elements are used once, the resulted nonlinearity error at that point is zero. With the effect of DWA algorithm, the access times of each element can be equalized in the shortest time period. This ensures that the nonlinearity errors are sum to zero quickly.

Under the same conditions, the randomization algorithm can not guarantee that the nonlinearity error can be averaged out in a short period due to its arbitrary element selection. The short error averaging-out period makes the mismatch noise move to high frequencies. Hence, the mismatch noise in the signal-band is relatively smaller in a low-pass DAC with DWA algorithm compared with that with the randomization algorithm. It has been proven analytically that DWA provides first-order shaping of the DAC mismatch error [39][40].

For the DAC with DWA algorithm, the error averaging-out period depends on the input data. Usually the input data is not constant, so the error averaging period is not fixed. This may move the distortion to the lower frequency domain. These tones result

from the limited cycles which excite the DAC with essentially unchanging periodic signals [34]. The SFDR may be degraded in the signal band. Figure 19 shows the ΔΣM's output PSD with DWA. Figure 20 and Figure 21 show the SNDR and SFDR of the ΔΣM with DWA respectively. SFDR drops when the input signal level is higher than -40dBFS, which means DWA does cause in-band tones problem.

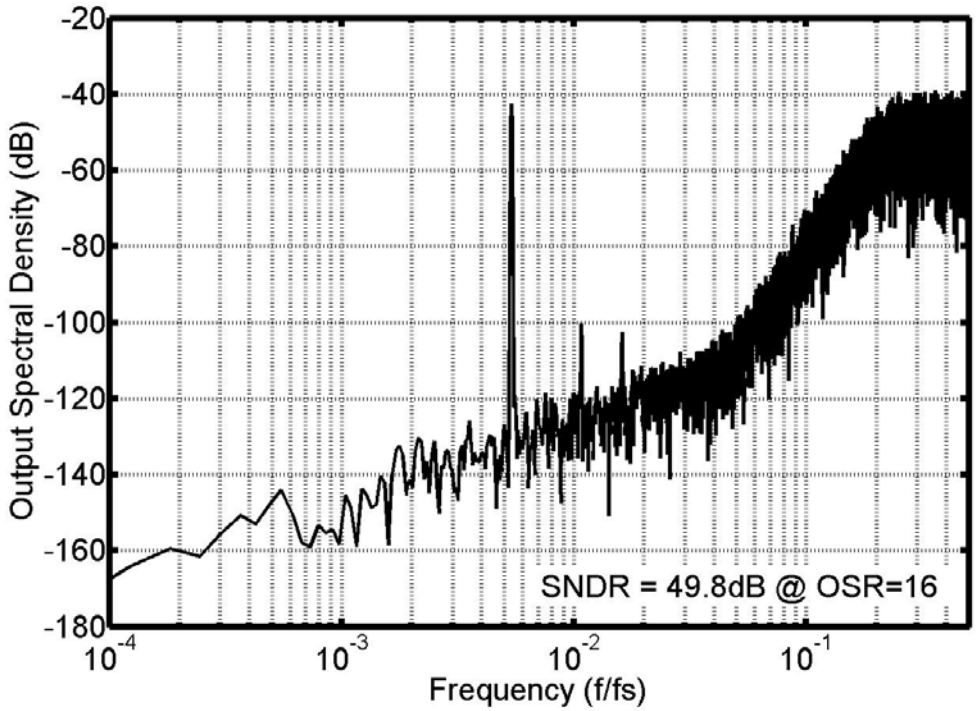


Figure 19. ΔΣM's output PSD with DWA.

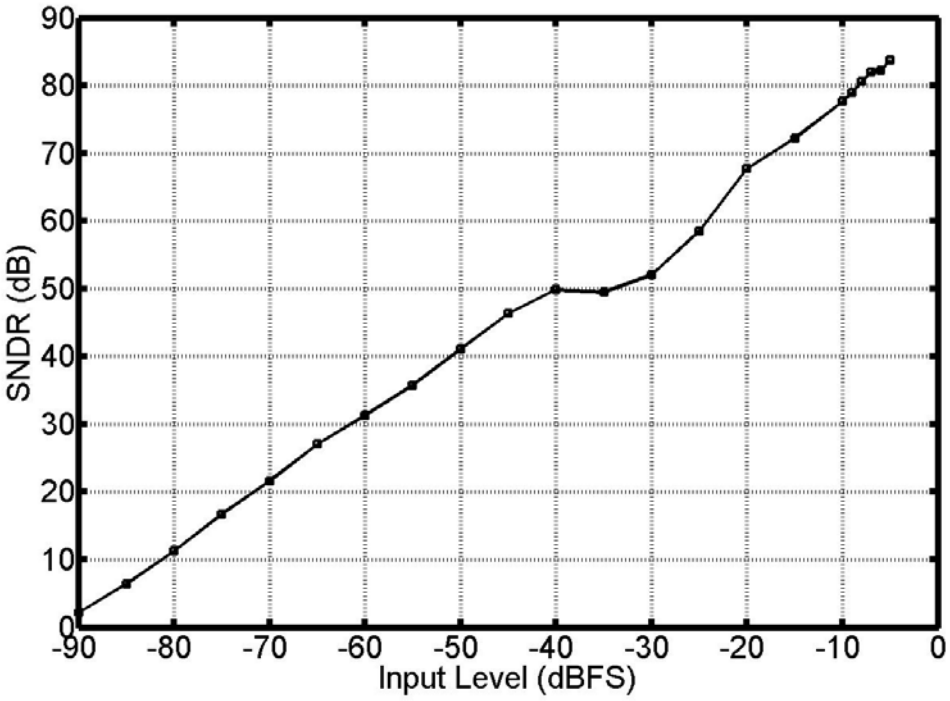


Figure 20. SNDR of the ΔΣM with DWA.

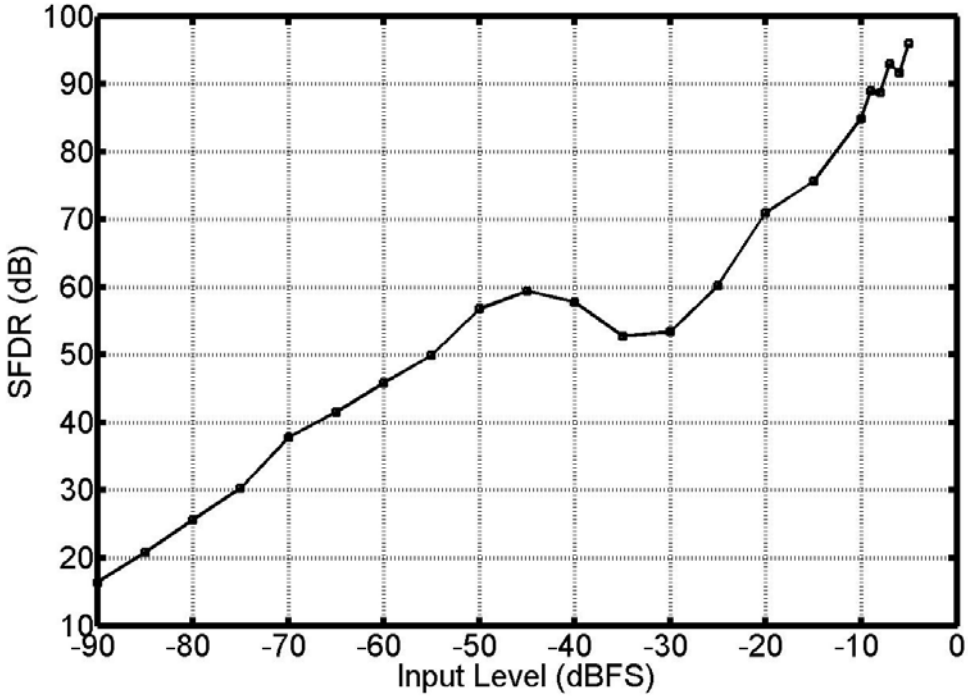


Figure 21. SFDR of the ΔΣM with DWA.

This limitation can be overcome by dithering at the input of the DAC to whiten

the inband tones [34]. However, the added dither result in stability issue and does contribute additional noise power to the signal band. To reduce the in-band tones of DWA, modified DWA algorithms are consequently reported in previous works.

### 3.2.3 Modified Data Weighted Averaging

The modified DWA algorithms, such as Partitioned DWA (PDWA) [41], Bi-Directional DWA (Bi-DWA) [42], Rotated DWA (RDWA) [43][44], Incremental DWA (IDWA) [45][46][47], Randomized DWA (RnDWA)[48][49] and Pseudo DWA (PsDWA) [50], have been reported to eliminate the in-band tones.

#### 3.2.3.1 Partitioned Data Weighted Averaging

PDWA splits the DAC into two identical parts with each employing the conventional DWA algorithm. In each DWA, a pointer always points to the first unused unit element. Selected in rotation, the DAC unit elements can be used at the maximum possible rate and each element is used by the same number of times, thus ensures that the errors introduced by the DAC quickly average to zero. PDWA algorithm reduces the in-band tones that are generated by the DWA, but the noise floor of DAC is increased in the signal band and SNR is sacrificed. Figure 22 shows the ΔΣM's output PSD with PDWA. Figure 23 and Figure 24 show the SNDR and SFDR of the ΔΣM with PDWA respectively. The ΔΣM with PDWA is quite linear as shown in Figure 23 and Figure 24.

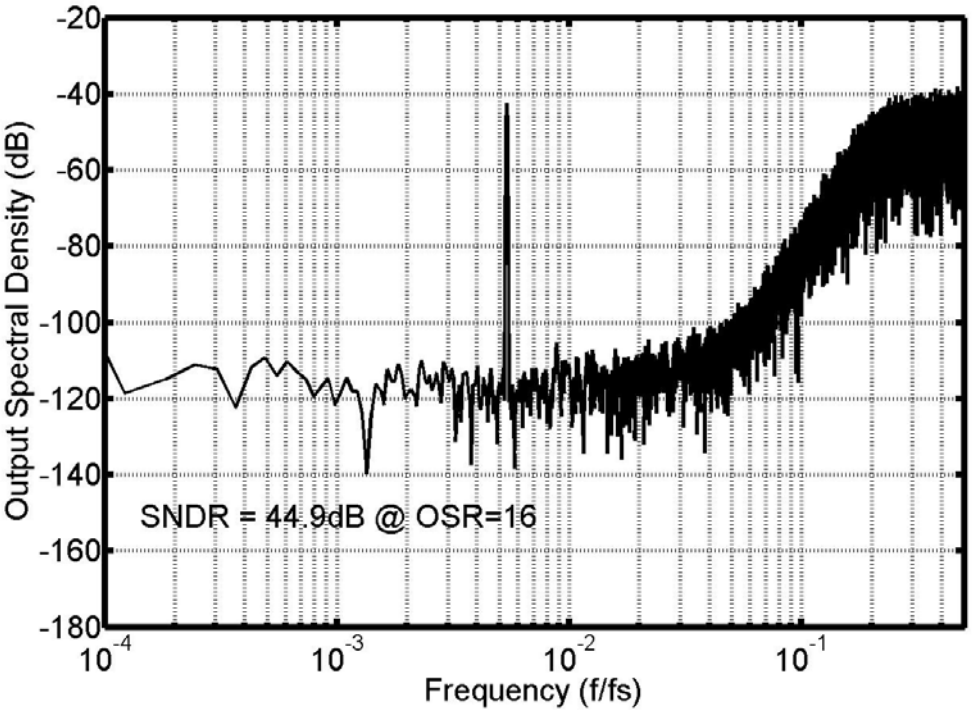


Figure 22. ΔΣM's output PSD with PDWA.

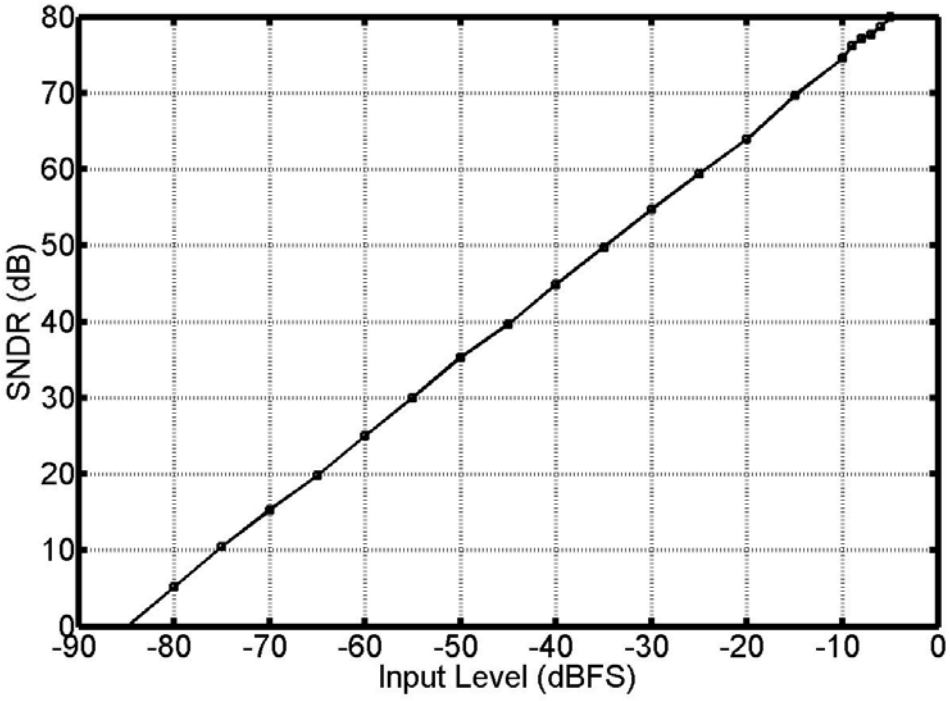


Figure 23. SNDR of the ΔΣM with PDWA.

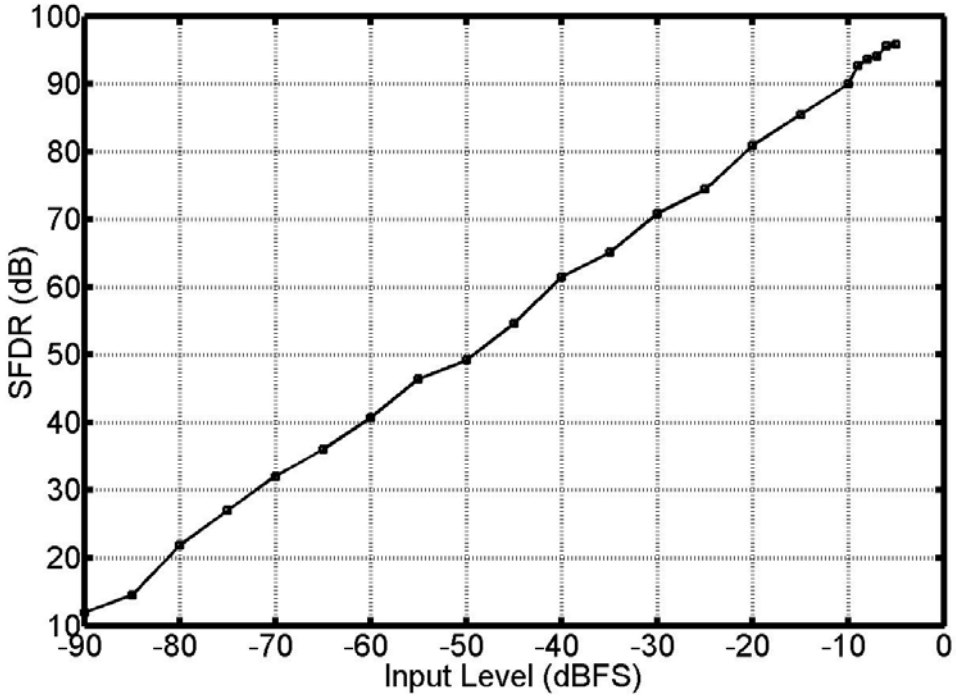


Figure 24. SFDR of the ΔΣM with PDWA.

#### 3.2.3.2 Bi-directional Data Weighted Averaging

The Bi-DWA (Bi-directional DWA) uses two pointers: one for the even clock cycles and one for the odd. While in the even clock cycles, one pointer rotates the used elements in one direction, in the odd clock cycles the other pointer rotates in the opposite direction. The operation principle is illustrated in Figure 25. Compared to DWA, the implementation requires more hardware since the barrel-shifter should be able to shift in two directions and an extra pointer register is needed. Bi-DWA can achieve better SFDR than DWA, but at the cost of increased in-band noise, that causes worse SNR. Figure 26 shows the ΔΣM's output PSD with Bi-DWA. Figure 27 and Figure 28 show the SNDR and SFDR of the ΔΣM with Bi-DWA respectively. The ΔΣM with Bi-DWA is also linear as shown in Figure 27 and Figure 28, but the noise floor of ΔΣM with Bi-DWA is 5dB higher than the one with PDWA.

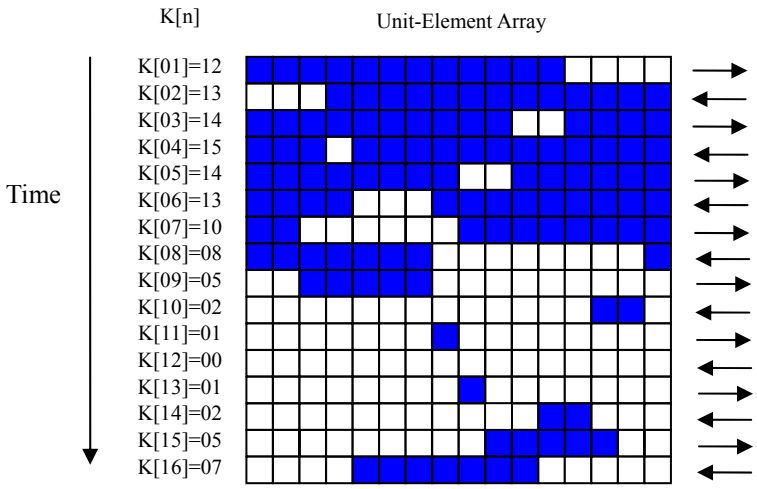


Figure 25. The Bi-DWA operation principle.

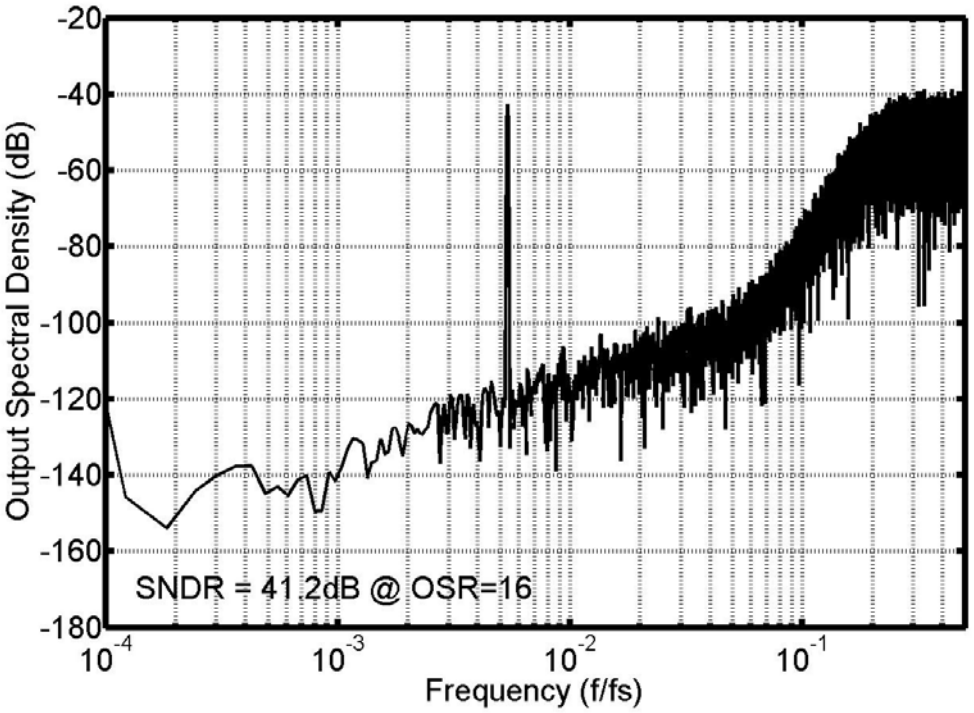


Figure 26. ΔΣM's output PSD with Bi-DWA.

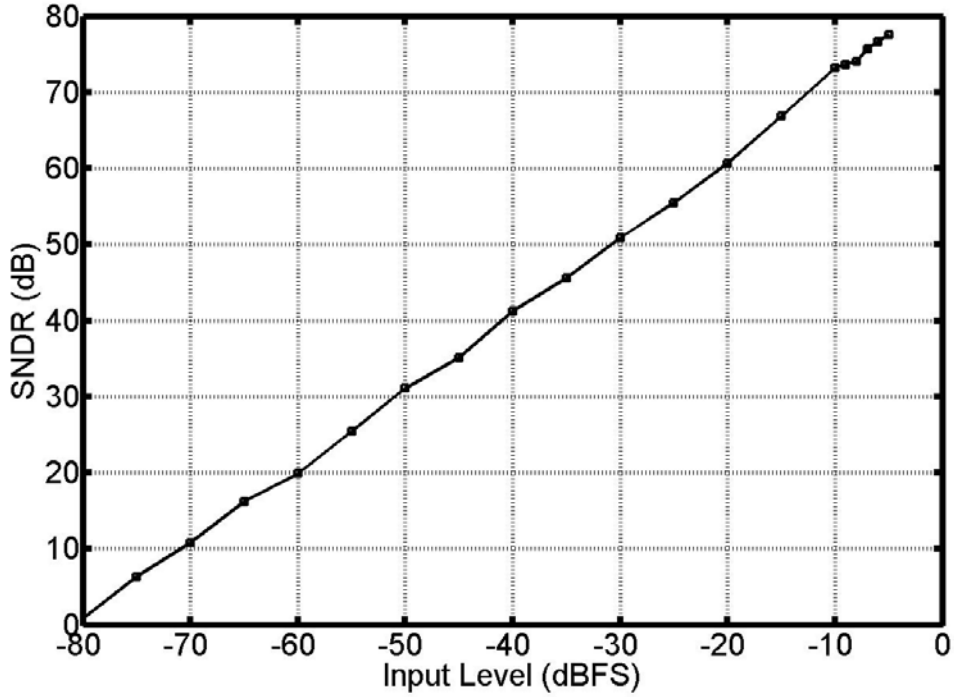


Figure 27. SNDR of the ΔΣM with Bi-DWA.

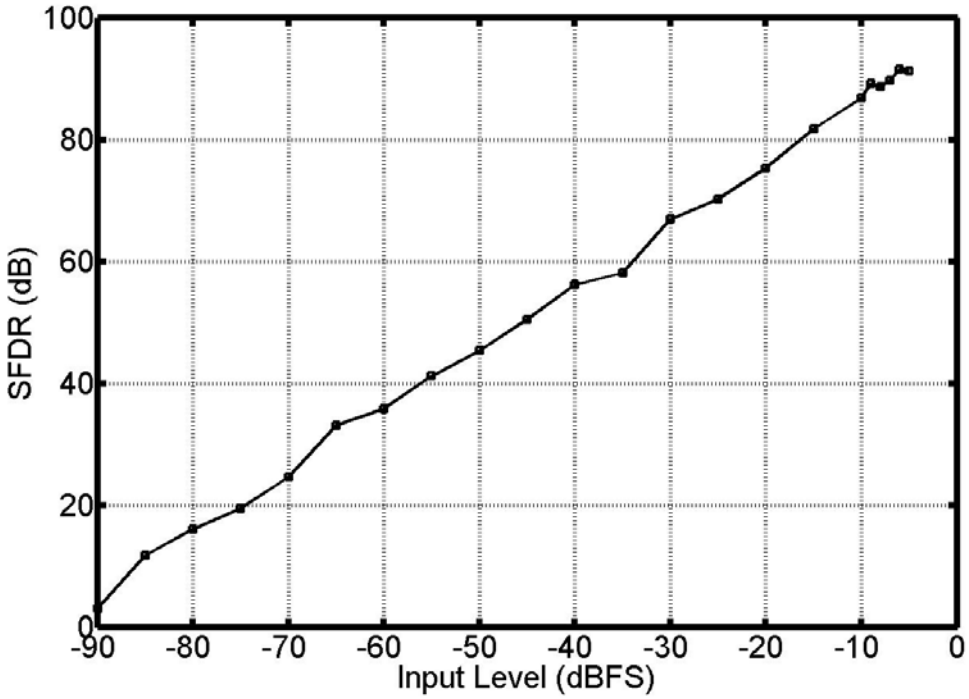


Figure 28. SFDR of the ΔΣM with Bi-DWA.

#### 3.2.3.3 Incremental Data Weighted Averaging

In the IDWA, *m* extra unit elements are added to the DAC as such that during every clock cycle at least *m* unit elements are not used. In this method, the SFDR drop in DWA can be recovered to some degree; however, a drop in SFDR curve may still occur for larger input amplitudes. This shows that the location of the tones is not accurately controlled by this algorithm and in-band tomes can still occur[50]. Figure 29 shows the ΔΣM's output PSD with IDWA with m equal to 9. Figure 30 and Figure 31 show the SNDR and SFDR of the ΔΣM with IDWA respectively. The ΔΣM with IDWA is not linear and there are in-band tones as shown in Figure 31, although the noise floor of ΔΣM with IDWA is 5dB lower than the one with PDWA.

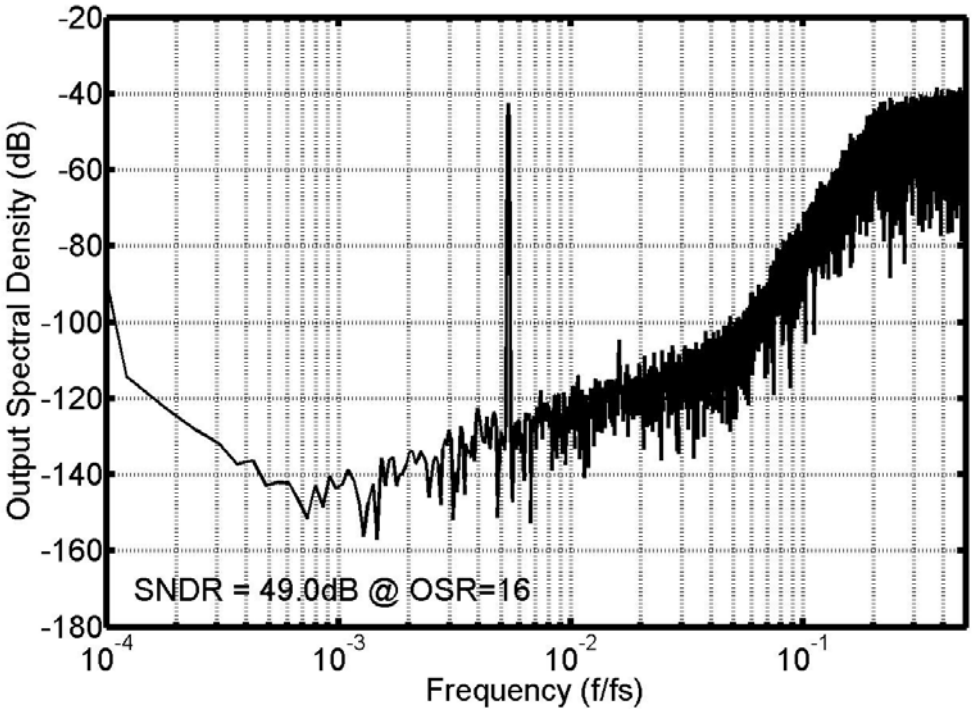


Figure 29. ΔΣM's output PSD with IDWA with m equal to 9.

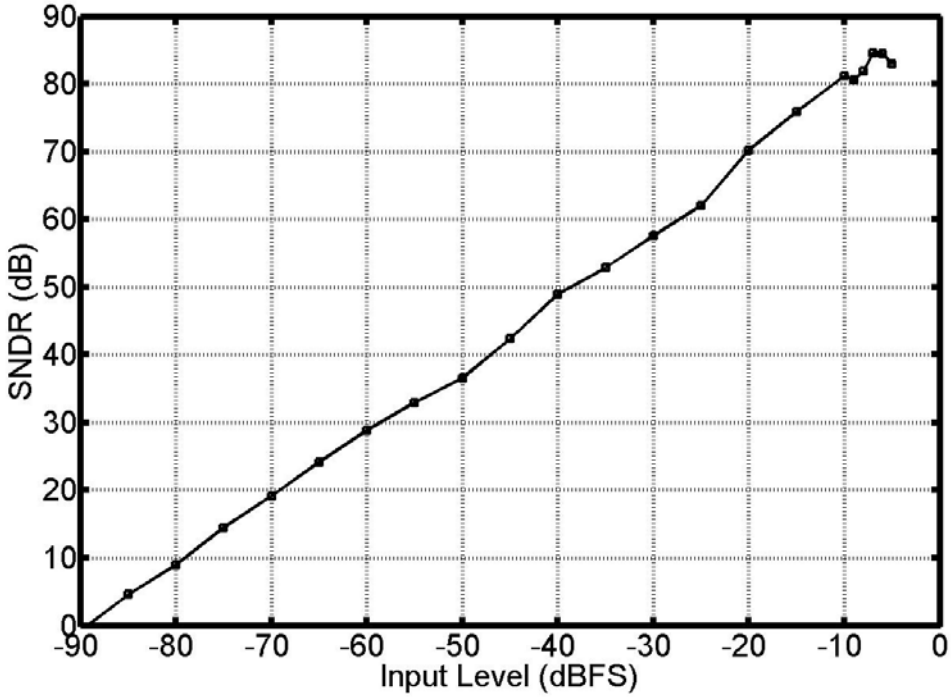


Figure 30. SNDR of the ΔΣM with IDWA.

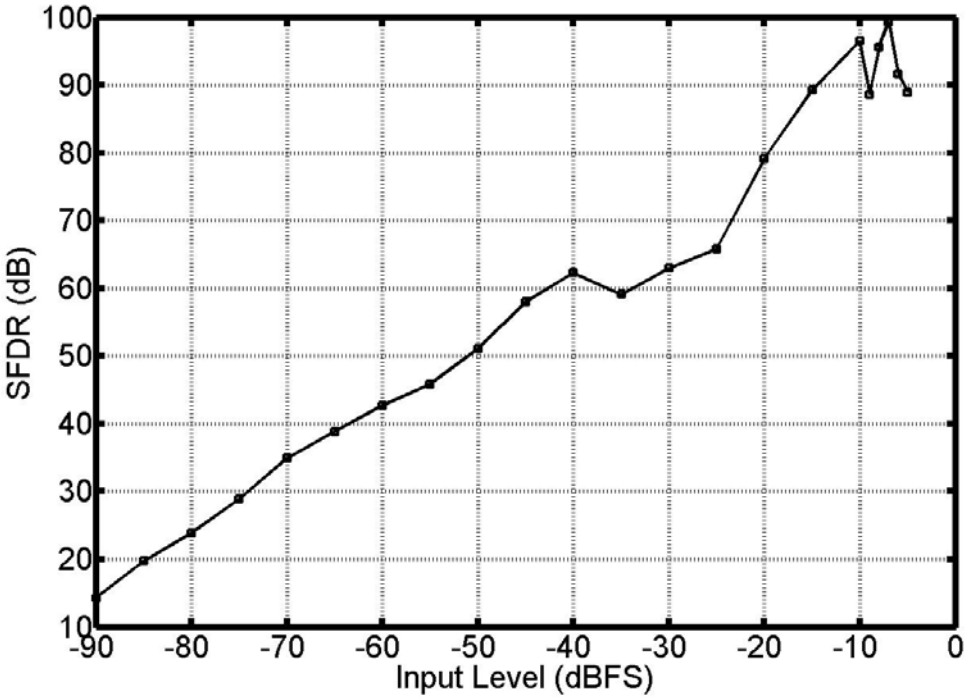


Figure 31. SFDR of the ΔΣM with IDWA.

#### 3.2.3.4 Rotated Data Weighted Averaging

In the RDWA (Rotated Data Weighted Averaging), the element access cycles rotate through the elements just like DWA, but occasionally changes the sequence of the elements. This operation can remove the tones; however, the sequence cannot be changed frequently; otherwise the performance will be degraded. The hardware implementation for this method is more complex.

#### 3.2.3.5 Randomized Data Weighted Averaging

The RnDWA (Randomized Data Weighted Averaging) operates as follows. Randomly selecting the elements among those that have not yet been used, RnDWA will begin the random selection again if all of the elements are used before. Obviously, the hardware implementation for this method is much more complex, although it can remove all of the tones.

#### 3.2.3.6 Pseudo Data Weighted Averaging

PsDWA (Pseudo Data Weighted Averaging) operation is essentially like the conventional DWA, which uses a pointer to "point" at the first unused element. PsDWA modifies the DWA scheme by periodically inverting the LSB of the pointer for DAC element selection. Thus, in every N clock cycle, a DAC element is periodically either reselected or skipped depending on whether the previous DAC input code was odd or even.

PsDWA breaks the cyclic nature of the element-selection process and, reduces the tone behavior; however, the inband noise is increased and SNDR is degraded [50]. Figure 32 shows the ΔΣM's output PSD with PsDWA with N equal to 256. Figure 33 and Figure 34 show the SNDR and SFDR of the ΔΣM with PsDWA respectively. There are no obvious in-band tones in the ΔΣM with PsDWA as shown in Figure 34, but the

noise floor is 10dB higher than the ΔΣM with PDWA.

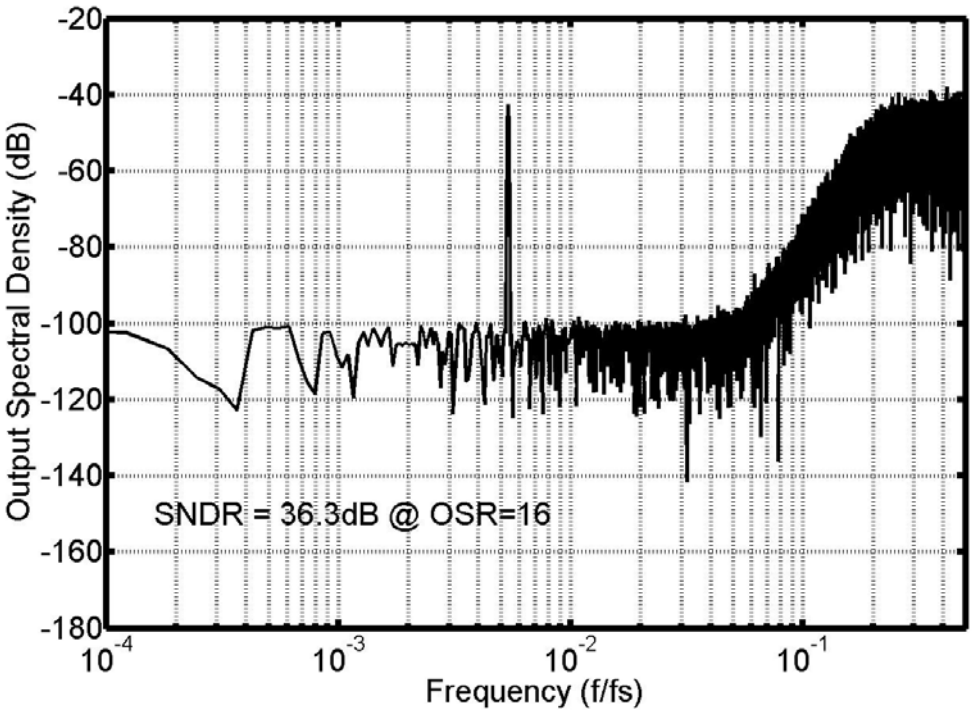


Figure 32. ΔΣM's output PSD with PsDWA with N equal to 256.

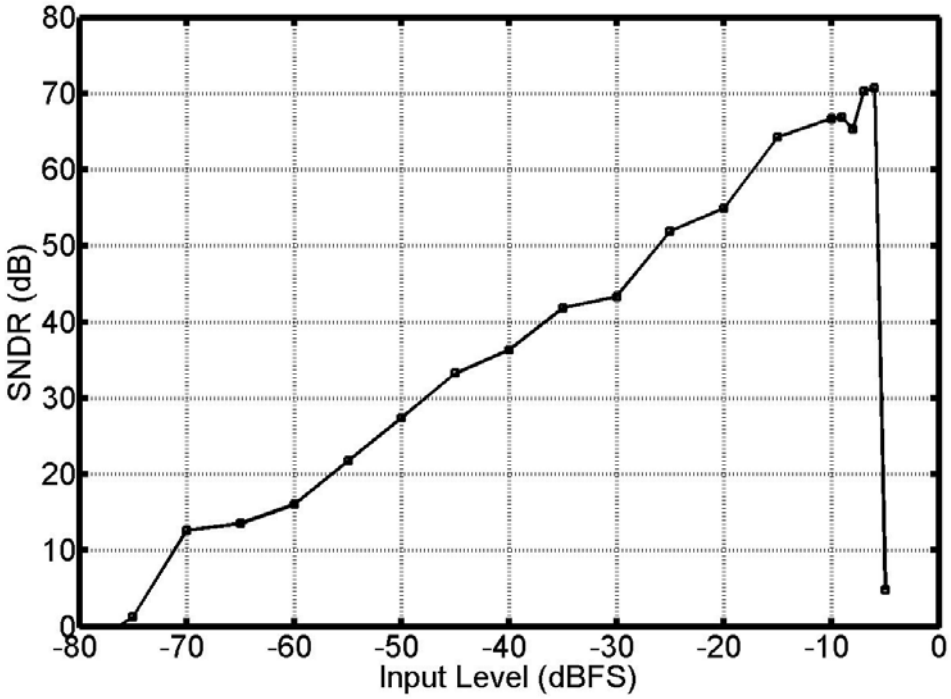


Figure 33. SNDR of the ΔΣM with PsDWA.

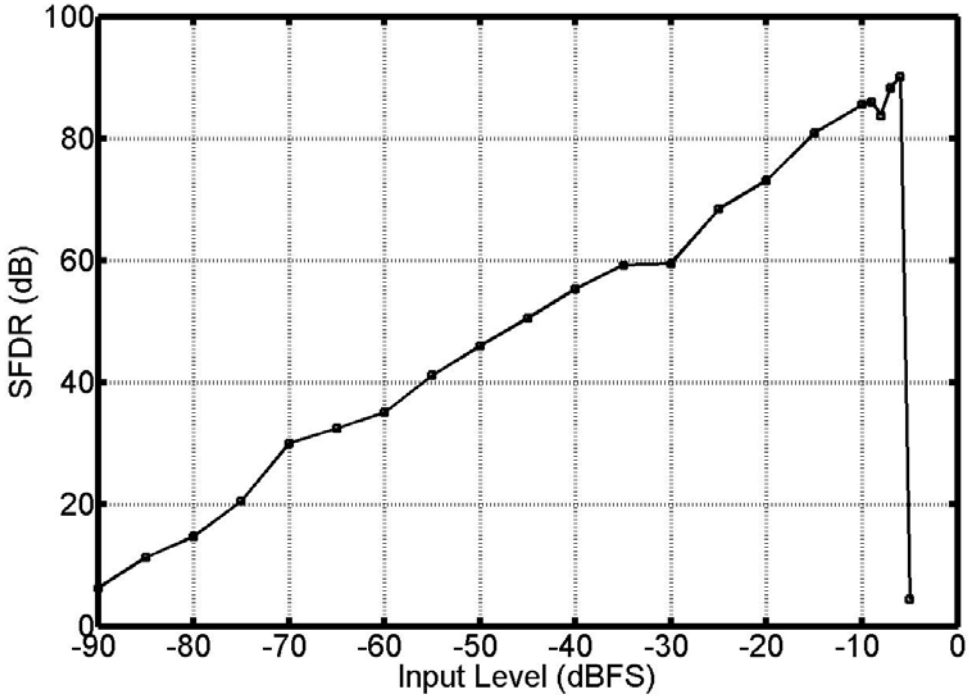


Figure 34. SFDR of the ΔΣM with PsDWA.

### 3.2.4 Tree-structure DEMs

Another DEM algorithm uses a tree-structure to perform the shuffling operation of the selected unit elements of DAC. This tree-structure was originally proposed in [51] and further detailed in [52] [53] [54]. The tree-structure for a DAC consists of $2^k$ unit elements and a "tree" shape switching network which is formed by $2^k$-1 sub switching blocks and used to select these unit elements, as shown in Figure 35. Each sub switching block can include a highpass noise shaping function, which generates the control signal for the subsequent switching blocks in the network. Therefore, differently shaped DAC errors can be achieved by employing different highpass noise shaping function, such as first- and second-order noise shaping.

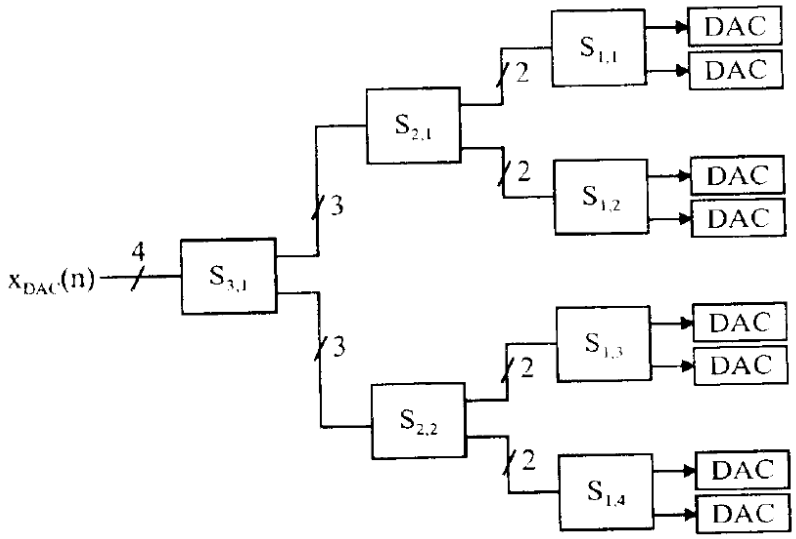


Figure 35. Tree-structure DEM.

The second-order noise shaping also in [52] can be overloaded for large input signals. When overload occurs, second-order noise-shaped DAC can no longer be obtained. The first-order noise shaping DEM introduces less hardware and propagation delay, but suffering less signal-to-noise plus distortion ratio (SNDR) compared with the second order's one. The first-order noise shaping with the tree-structure in [52] shows comparable performance as the DWA [29] and tends to generate in-band tones as well as DWA. However, DWA is preferred due to the less complex hardware requirements. Figure 36 shows the ΔΣM's output PSD with the tree-structure DEM. Figure 37 and Figure 38 show the SNDR and SFDR of the ΔΣM with the tree-structure DEM respectively. The in-band tones exit in the ΔΣM with the tree-structure DEM as shown in Figure 38.

The white dithering technique [52] [55] [56] is employed to reduce the tones, but it has to increase the DAC noise floor. Figure 39 shows the ΔΣM's output PSD with the dithered tree-structure DEM. Figure 40 and Figure 41 show the SNDR and SFDR of the ΔΣM with the dithered tree-structure DEM respectively. There are still some small in-band tones in the ΔΣM with the dithered tree-structure DEM as shown in

Figure 41. Recently, a high-pass dithering technique [57] provides better SNR performance than the conventional white dithering, but the noise floor is still higher than the original tree-structure DEM.

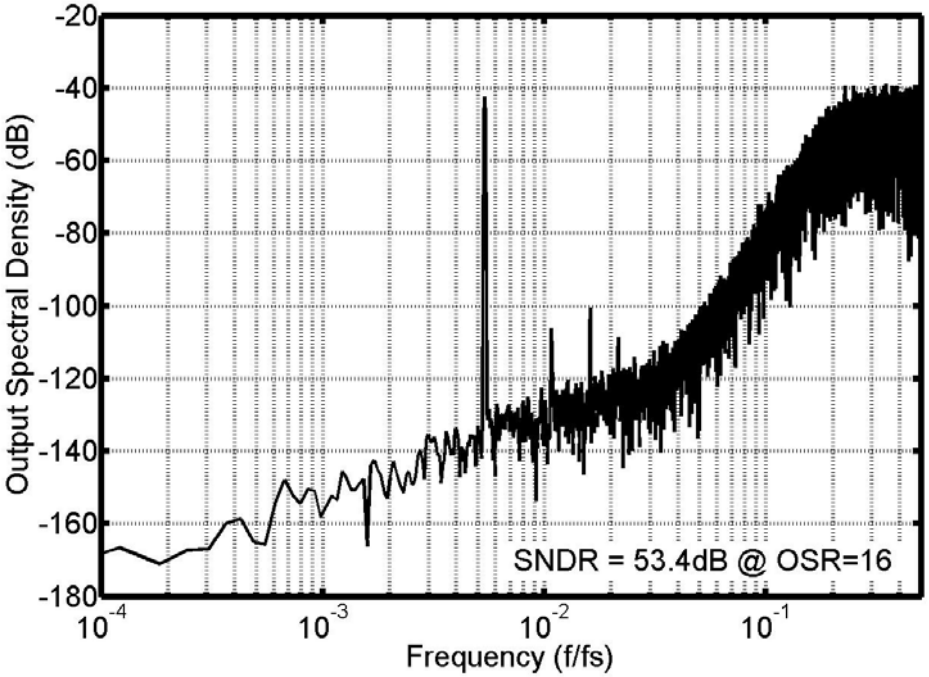


Figure 36. ΔΣM's output PSD with tree-structure DEM.

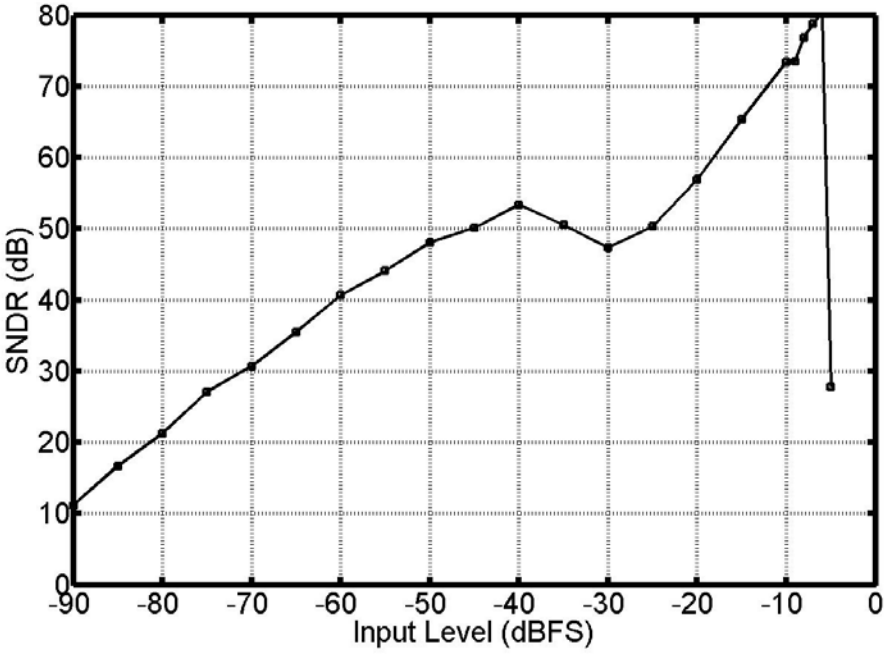


Figure 37. SNDR of the ΔΣM with tree-structure DEM.

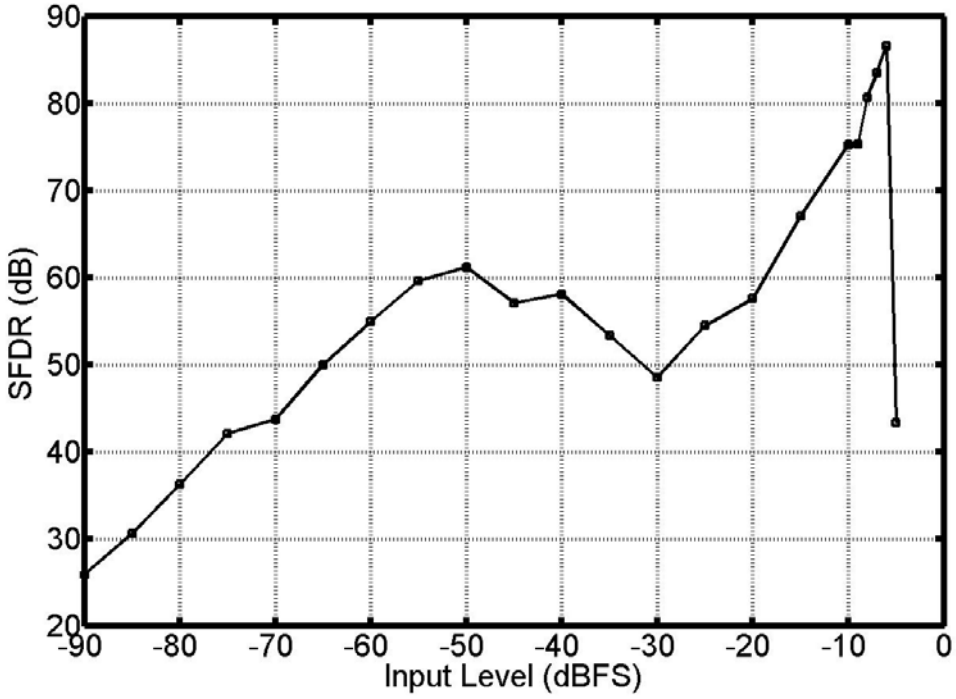


Figure 38. SFDR of the ΔΣM with tree-structure DEM.

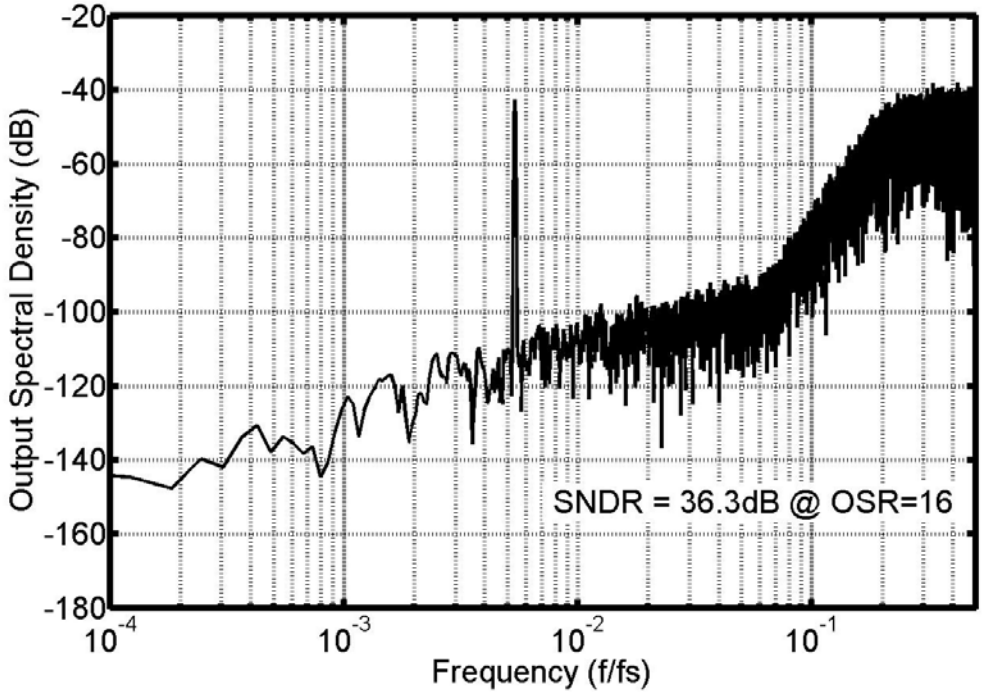


Figure 39. ΔΣM's output PSD with dithered tree-structure DEM.

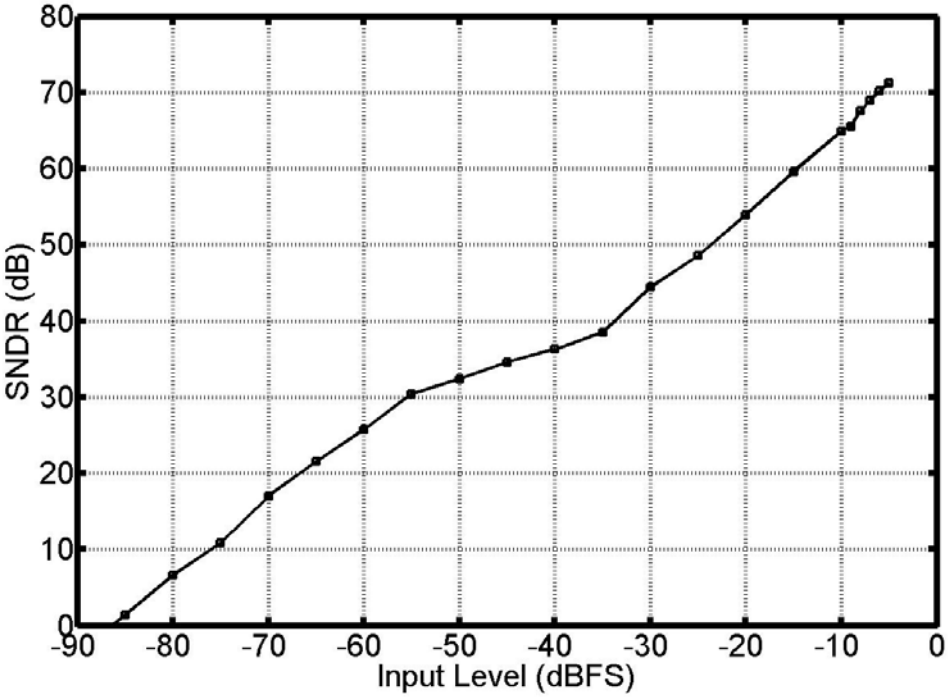


Figure 40. SNDR of the ΔΣM with dithered tree-structure DEM.

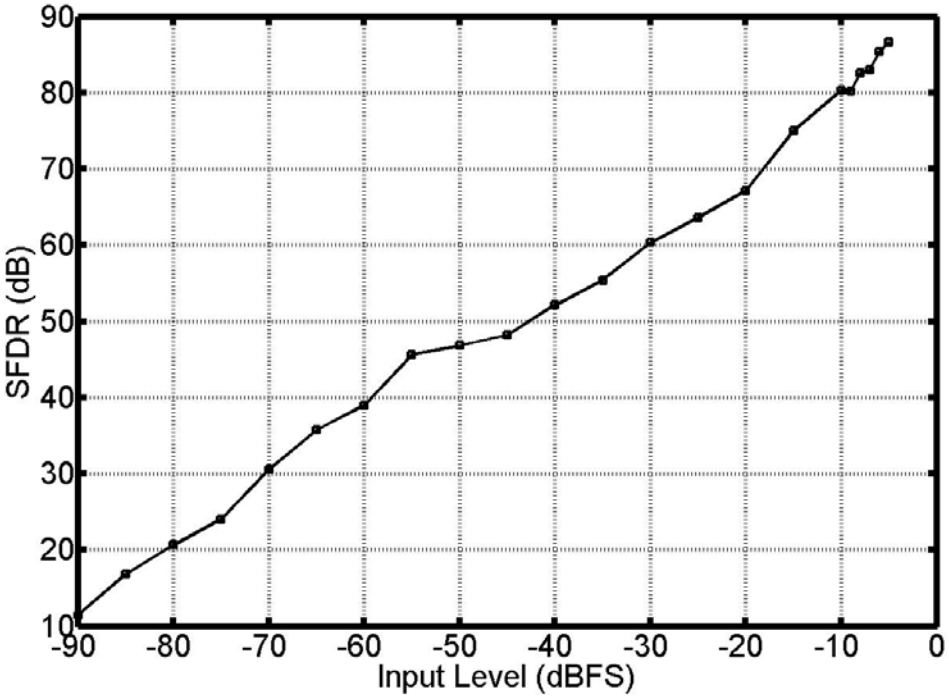


Figure 41. SFDR of the ΔΣM with dithered tree-structure DEM.

## 3.3 Summary

Among most of the existing DEMs, DWA seems to offer a good performance where DAC mismatch error is first-order shaped. Due to the simplicity of the algorithm, little digital hardware is required and it is suitable for high speed converter. A drawback of DWA is the input signal dependant SFDR. Although the modified DWA algorithms are reported to reduce the in-band tones of DWA, the SNR degradation or notable tone problems still remain.

In summary, most existing DEM techniques reduce the spurious tones by spreading them over wide spectrum. As a result, the tone energy is reduced, but the noise floor is increased. In other words, it trades SNR for SFDR. Table 1 shows the performance comparison of those widely used DEM. PDWA obtains the best compromise, namely the highest resolution without any visible tones.

Table 1. Performance comparison of the widely used DEM

| DEM | Peak SNDR (dB) | SFDR (dB) @ -40dBFS | Linearity over -90 to 0dBFS |
|---|---|---|---|
| Rand | 58 | 39 | No Visible Tones |
| DWA | 85 | 58 | Visible Tones |
| PDWA | 81 | 62 | No Visible Tones |
| Bi-DWA | 78 | 58 | No Visible Tones |
| IDWA | 85 | 62 | Visible Tones |
| PsDWA | 70 | 56 | No Visible Tones |

| | | | |
|---|---|---|---|
| Tree-structure | 80 | 58 | Visible Tones |
| Dithered Tree-structure | 71 | 52 | Visible Tones |

# Chapter 4 Noise Shaping Dynamic Element Matching

Most of the existing DEM techniques reduce the spurious tones of the DAC by spreading them over wide spectrum. As a result, the tone energy is reduced, but the noise floor is increased. In other words, it trades SNR for SFDR. This chapter proposes the noise-shaping DEM (NS-DEM), a new technique that aims to eliminate the trade-off between SNR and SFDR, The concept of NS-DEM is introduced and analyzed first, and then evaluated with several existing DEMs by the behavioral simulations.

Figure 42 shows the block diagram of a typical multi-bit ΔΣM with DEM. And Figure 43 shows a linear model of the multi-bit ΔΣM.

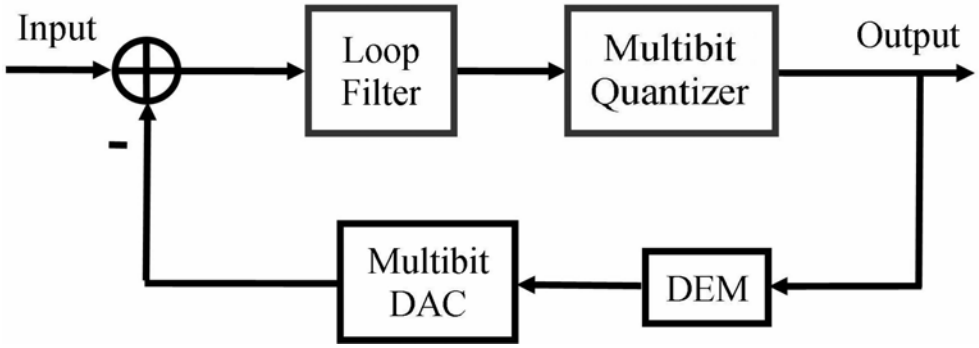


Figure 42. Typical Multi-bit ΔΣM with DEM.

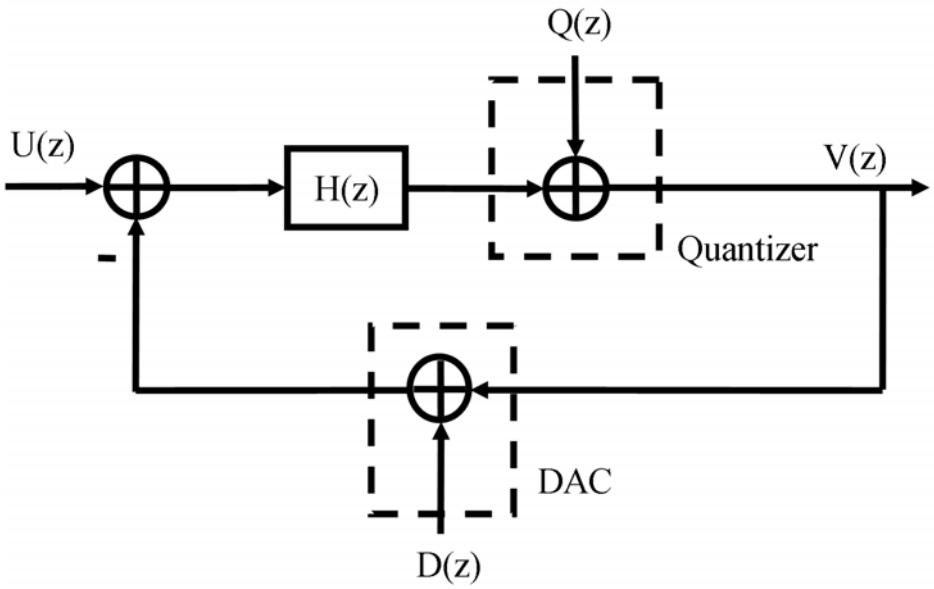


Figure 43. Linear model of multi-bit ΔΣM.

For the sake of simplicity, if assuming the DEM ideally randomizes the nonlinear DAC unit elements, the inherent DAC noise is modeled by an additive noise D(z). Since the output of the DAC is directly subtracted from the input signal, the DAC noise, D(z), should have the same transfer function as the input signal, U(z). The output of ΔΣM can be expressed as

$$V(z) = \frac{H(z)}{1+H(z)}U(z) + \frac{1}{1+H(z)}Q(z) - \frac{H(z)}{1+H(z)}D(z) \tag{16}$$

and the DAC noise transfer function is

$$H_d(z) = \frac{V(z)}{D(z)} = \frac{-H(z)}{1+H(z)} \tag{17}$$

which is exactly the same as the signal transfer function except the negative sign. This implies that the DAC noise directly passes through the ΔΣM without being suppressed and hence can degrade the performance of the ΔΣM, thus nullifying the advantage achieved from the multi-bit quantizer. As discussed in the previous Chapter, DEM is used to enhance the linearity of DAC; however, most existing DEMs sacrifice the

DAC SNR to obtain better SFDR.

## 4.1 Proposed NS-DEM Architecture

Figure 44 shows the block diagram of the proposed multi-bit ΔΣM with NS-DEM [58][59]. Its linear model is presented in Figure 45 where the DAC error is modeled by an additive noise, D(z).

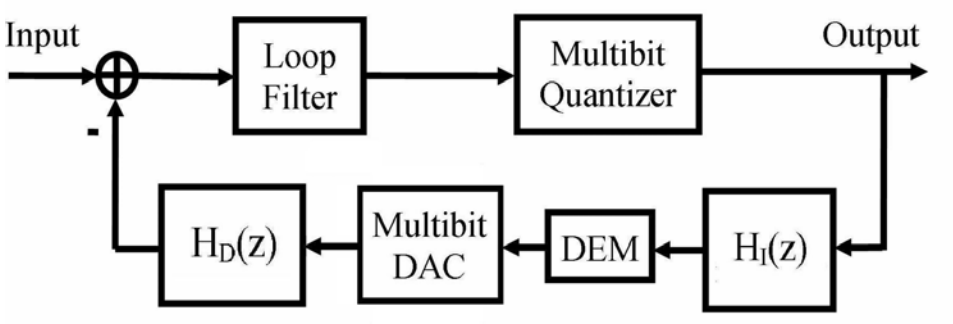


Figure 44. Block diagram of the proposed multi-bit ΔΣM with NS-DEM.

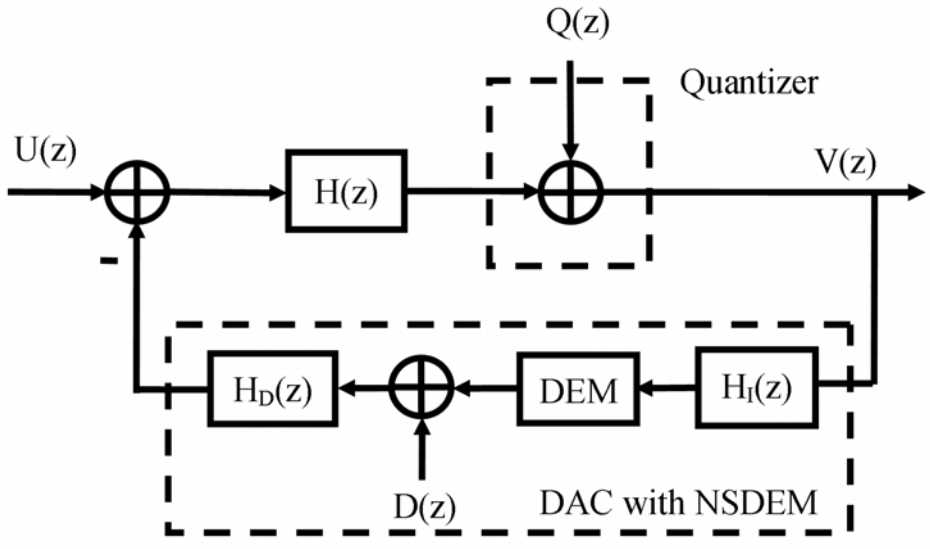


Figure 45. Linear Model of proposed multi-bit ΔΣM with NS-DEM.

Compared with the existing multi-bit ΔΣMs with DEM only, in NS-DEM, two additional signal processing blocks, $H_D(z)$ and $H_I(z)$, are inserted before DEM and after the DAC respectively. $H_I(z)$ counteracts $H_D(z)$ so that the feedback signal from the quantizer can not be affected when received at the input of the ΔΣM. The signal

transfer function (STF), quantization noise transfer function ($NTF_Q$), and DAC noise transfer function ($NTF_D$) can be written as

$$STF = \frac{V(z)}{U(z)} = \frac{H(z)}{1 + H(z)H_I(z)H_D(z)} \tag{18}$$

$$NTF_Q = \frac{V(z)}{Q(z)} = \frac{1}{1 + H(z)H_I(z)H_D(z)} \tag{19}$$

$$NTF_D = \frac{V(z)}{D(z)} = -\frac{H(z)H_D(z)}{1 + H(z)H_I(z)H_D(z)}. \tag{20}$$

Since $H_I(z)$ counteracts $H_D(z)$, they offset each other, that is, $H_I(z)H_D(z)=1$. The signal and quantization noise transfer functions (first two equations) are not affected and they remain the same as those from the conventional ΔΣM, while the DAC noise transfer function becomes

$$NTF_D = \frac{V(z)}{D(z)} = \frac{-H(z)}{1 + H(z)} H_D(z). \tag{21}$$

The DAC noise is modified or shaped by $H_D(z)$. Obviously, the zero(s) should be within the signal band in order to shape the DAC noise out of signal band. In principle, $H_I(z)$ and $H_D(z)$ are not only in the 1st-order, but also in the higher order. But for simplicity, only 1st-order $H_I(z)$ and $H_D(z)$ for the lowpass ΔΣM are discussed in the following.

### 4.1.1 1st-Order NS-DEM for Lowpass ΔΣM

For a lowpass ΔΣM with the 1st-order NS-DEM, $H_D(z)$ can be simply a differentiator, which moves the in-band noise to the high frequencies and provides a first-order shaping to the DAC noise, D(z). Thus $H_D(z)$ can be written as

$$H_D(z) = 1 - z^{-1}. \tag{22}$$

Consequently, $H_I(z)$ should be an accumulator whose transfer function is

$$H_I(z) = \frac{1}{1 - z^{-1}}. \tag{23}$$

Thus according to the Eq. (22) and (23), Figure 46 shows the block diagram of NS-DEM for lowpass ΔΣM.

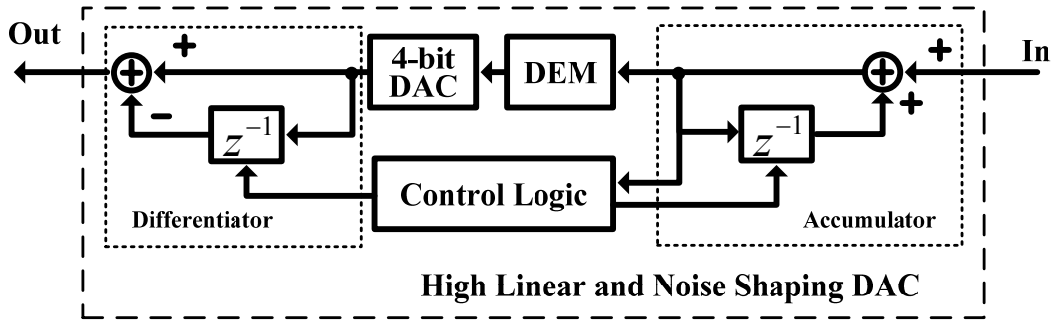


Figure 46. The block diagram of NS-DEM for the lowpass ΔΣM.

If the accumulator and the differentiator are perfect, the DAC SNR improvement bound is theoretically formulated as follows. The DAC thermal noise is not considered in the formulation.

Supposing that the DAC error is already converted into the white noise by an ideal randomization DEM, the in-band DAC noise power is

$$P_n = P \cdot 2f_0 / f_s = P / OSR, \tag{24}$$

where $P$ is the total DAC noise power over $f_s/2$, $f_0$ is the signal bandwidth, $f_s$ is the sampling frequency, and OSR is the oversampling ratio. With the first-order noise shaping provided by the differentiator or $H_D(z)$, the in-band noise power becomes

$$P_n' = \int_0^{f_0} P\left|1 - e^{-j2\pi f_0 / f_s}\right|^2 df = \int_0^{f_0} P\left|2\sin(\pi f_0 / f_s)\right|^2 df \approx P\frac{\pi^2}{3} / OSR^3, \tag{25}$$

provided $f_0 << f_s$. Similar to the first-order ΔΣM, the SNR improvement of the multi-bit DAC with NS-DEM over the DAC with randomization DEM is

$$\Delta SNR(dB) = 20\log(OSR) + 10\log(3/\pi^2) \approx 20\log(OSR) - 5.17 \qquad (26)$$

Figure 47 shows the SNR improvement with different OSR. For the DEM block in the NS-DEM, since its role is to break the tones and spread the energy to the entire spectrum, most of the existing DEM techniques can be employed.

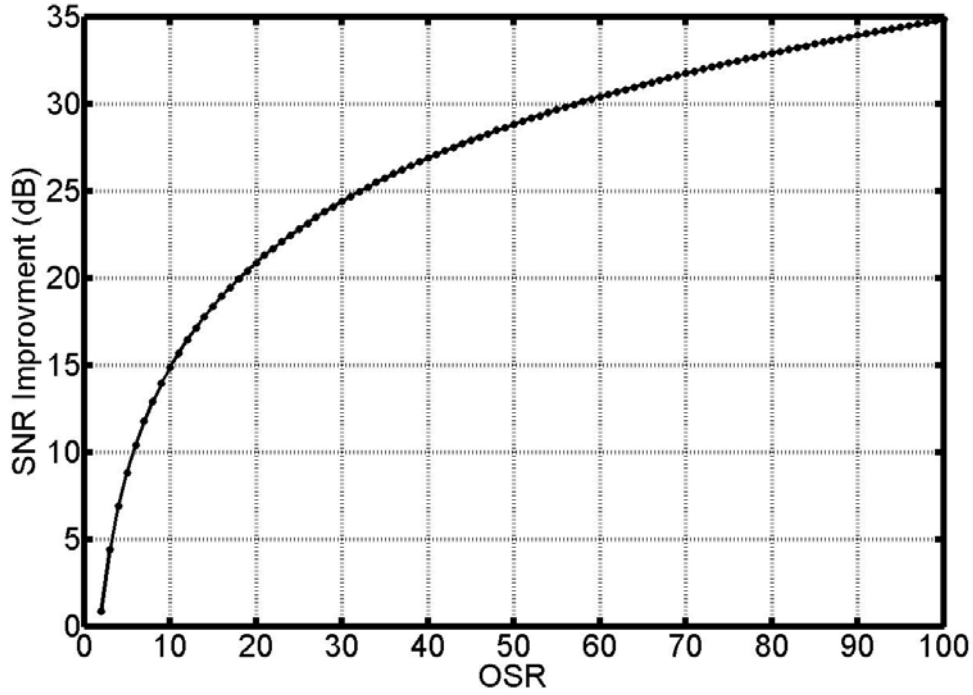


Figure 47. SNR Improvement v.s. Different OSR.

### 4.1.2 NS-DEM for Bandpass ΔΣM

For bandpass ΔΣM, $H_D(z)$ and HI(z) are more complicated. $H_D(z)$'s zero should be located in the signal band to shape the DAC noise. And $H_I(z)$ is $1/H_D(z)$ to make sure $H_D(z)H_I(z)=1$. However the implementation may not be simple for this case. For the bandpass ΔΣM whose sampling frequency equals to 4 times of signal center frequency, $f_s = 4f_0$, the transfer function can be attained by substituting z by $-z^2$ for $H_D(z)$ and $H_I(z)$ in the above mentioned low-pass ΔΣM. The resulting $H_D(z)$ and $H_I(z)$ are given below.

$$H_I(z) = \frac{1}{1+z^{-2}} \tag{27}$$

$$H_D(z) = 1+z^{-2} \tag{28}$$

### 4.1.3 Accumulator Overflowing

In the above formulation, the accumulator in NS-DEM is assumed to have infinite length and therefore there is no overflow. However, in practice, the length of the accumulator is always limited. The accumulator is thus prone to overflow when the input signal is at a strong level or low frequency. When the overflowing occurs, an overflow flag will be detected by the control block as shown in Figure 46, and a reset signal is immediately sent to the registers of the accumulator and the differentiator. Once registers are reset to zero, the differentiator and accumulator do not function at all in that clock cycle. The adder in the accumulator and the subtractor in the differentiator will always add and subtract "zero", as shown in Figure 48. The DEM in NS-DEM still operates as usual while both the differentiator and the accumulator are bypassed at the same time. In next clock cycle, the differentiator and accumulator start to work again if overflow doesn't happen.

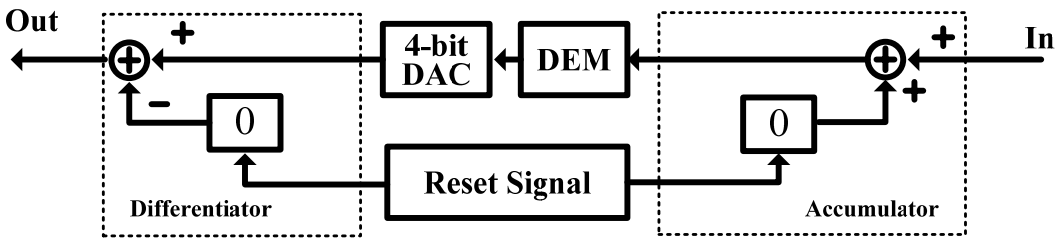


Figure 48. Accumulator and Differentiator are reset by the control logic.

However, the overflowing of the accumulator would impair the noise shaping performance of the NS-DEM. The noise shaping benefits of the NS-DEM would

gradually disappear when the overflowing happens more frequently. In the extreme case, the accumulator and the differentiator are reset in every clock cycle. When NS-DEM overflows, DEM still shuffles the DAC unit elements as usual and also the operation of the ΔΣM is not affected.

### 4.1.4 Nonideal differentiator

In NS-DEM, the noise shaping of DAC noise relies on the cancellation of transfer functions of the differentiator and accumulator, i.e. $H_I(z)$ and $H_D(z)$ as indicated in (20). Since they are respectively realized in the analog and digital domain, exact cancellation cannot be expected. This is mainly due to the analog differentiator in which the OTA has finite gain and settling error. However, it can be shown that the error of $H_D(z)$ caused by the finite gain appears as a scaling factor to the ideal $H_D(z)$, that is,

$$H_{D,non-ideal}(z) = \frac{1}{1+(1+\alpha)/A}\alpha(1-z^{-1}) = \frac{H_D(z)}{1+(1+\alpha)/A} \qquad (29)$$

where A is the DC gain of the OTA, α is the gain of the differentiator, set by $\alpha = 16C_{du} / C_f$ and $H_D(z) = \alpha(1-z^{-1})$, the ideal differentiator transfer function.

The DAC noise transfer function is therefore different from the ideal one due to the mismatch. As a result, the DAC noise shaping effect might be affected as well.

$$\frac{NTF_D^{ideal}}{NTF_D^{non-ideal}} = \frac{-\dfrac{H(z)H_D(z)}{1+H(z)H_I(z)H_D(z)}}{-\dfrac{H(z)H_{D,non-ideal}(z)}{1+H(z)H_I(z)H_{D,non-ideal}(z)}}$$
$$= \frac{\dfrac{H(z)}{1+\alpha H(z)}}{\dfrac{H(z)}{1+\alpha\beta H(z)}\cdot\beta} \qquad (30)$$
$$= \frac{\dfrac{1}{H(z)\beta}+\alpha}{\dfrac{1}{H(z)}+\alpha}$$

In the above equation, $\beta=1/[1+(1+\alpha)/A]$, $H_I(z)=1/(1-z^{-1})$, and H(z) is the transfer function of the loop filter. $NTF_D^{ideal}$ and $NTF_D^{non\text{-}ideal}$ are the ideal and non-ideal DAC noise transfer functions respectively. In the in-band signal frequency range, the loop filter's gain |H(z)| and OTA's DC gain are high, and $\alpha$ is one. The ratio in Eq (30) is slightly greater than one, which means the DAC noise shaping performance is not degraded but even slightly better. Therefore, assuming the DAC noise dominant the noise floor, SNR is not impaired but improved by $1/\beta^2$, as shown below. However, the scaling factor $\beta$ will reduce the feedback signal amplitude and thus cause the modulator unstable if $\beta$ is much smaller than one.

$$\frac{SNR^{ideal}}{SNR^{non-ideal}} = \left| \frac{\dfrac{U(z)\cdot STF^{ideal}}{Q(z)\cdot NTF_Q^{ideal} + D(z)\cdot NTF_D^{ideal}}}{\dfrac{U(z)\cdot STF^{non-ideal}}{Q(z)\cdot NTF_Q^{non-ideal} + D(z)\cdot NTF_D^{non-ideal}}} \right|^2$$

$$\approx \left| \frac{STF^{ideal}}{STF^{non-ideal}} \cdot \frac{NTF_D^{non-ideal}}{NTF_D^{ideal}} \right|^2 \tag{31}$$

$$= \left| \frac{\dfrac{H(z)}{1+H(z)H_I(z)H_D(z)}}{\dfrac{H(z)}{1+H(z)H_I(z)H_{D,non-ideal}(z)}} \cdot \frac{-\dfrac{H(z)H_{D,non-ideal}(z)}{1+H(z)H_I(z)H_{D,non-ideal}(z)}}{-\dfrac{H(z)H_D(z)}{1+H(z)H_I(z)H_D(z)}} \right|^2$$

$$= \beta^2$$

Since the differentiator is actually incorporated into the first stage of the loop filter in our design, the differentiator shares the same OTA with the loop filter. Thus although the lower OTA gain in the differentiator will result in the better SNR, the OTA gain for the loop filter is 1000 (60dB) without degrading the ΔΣM's performance.

## 4.2 Behavioral Verification

The NS-DEM technique is evaluated in a 5$^{th}$-order 4-bit quantization lowpass ΔΣM employing five existing DEM techniques, namely, randomization [59], DWA [34], PDWA, tree-structure DEM and dithered tree-structure DEM respectively. The architecture of the ΔΣM is illustrated in Figure 49. The 5$^{th}$-order lowpass ΔΣM used in the simulation is generated from the Delta-Sigma toolbox in MATLAB [60]. All the zeros of the NTF (noise transfer function) are at DC. The signal-to-noise and distortion ratio (SNDR) and spurious free dynamic range (SFDR) are used as the benchmarks for the system performance comparison. The evaluations are done in Matlab. The DAC nonlinearity is added as follows. The 4-bit DAC is assumed to be thermalmeter coded. The unit element value is randomly generated with a specified standard deviation (1%). Thus the quantization noise is well below the DAC noise. The in-band noise floor of

the ΔΣM is dominated by DAC noise not considering kT/C noise. In all cases, the OSR is fixed at 16 in calculating the SNDR. Thus the normalized signal bandwidth (BW) is 0.03125·*f*s. In the previous simulation, a standard deviation of 1% for the DAC unit elements is assumed.

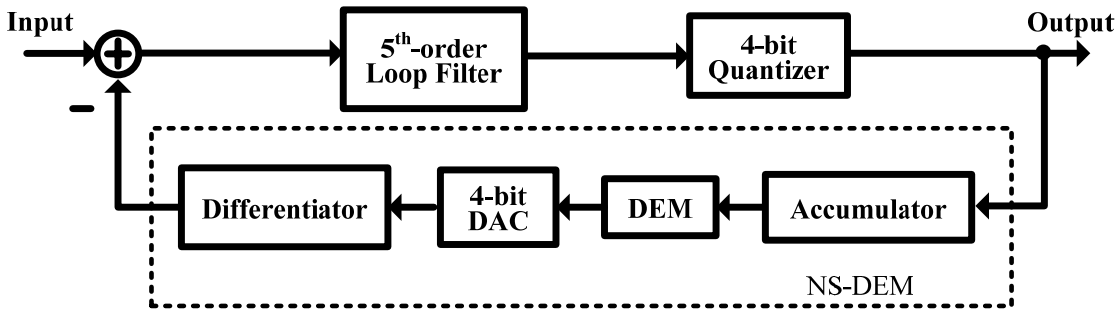


Figure 49. Block diagram of a 5th-order 4-bit quantization ΔΣM with NS-DEM.

In the following sub-sections, for each NS-DEM configuration, the linearity and resolution performance for each NS-DEM is presented. We will compare SNDR and SFDR of the ΔΣMs by employing existing DEMs that are with and without the proposed noise shaping, where the input signal is -40dBFS and 10/2048·*f*s. The ΔΣM used in the analysis is a 5th-order ΔΣM with 4-bit quantization.

### 4.2.1 NS-RAND

The NS-DEM that employs randomization for its DEM is referred to as noise shaping randomization, or NS-RAND hereafter. When NS-RAND is employed, it provides the first-order noise shaping to the noise floor and hence improves the SNDR. Figure 50 shows the ΔΣM's output power spectrum density (PSD) with Randomization and NS-RAND. The input signal frequency is 10/2048·*f*s. The plot shows that with NS-DEM, the ΔΣM's output SNDR, without distortion, is improved by 17dB, similar to that predicted in Eq. (26). Both of the DAC's and accumulator's resolution in the NS-RAND are 4-bit in the simulation.

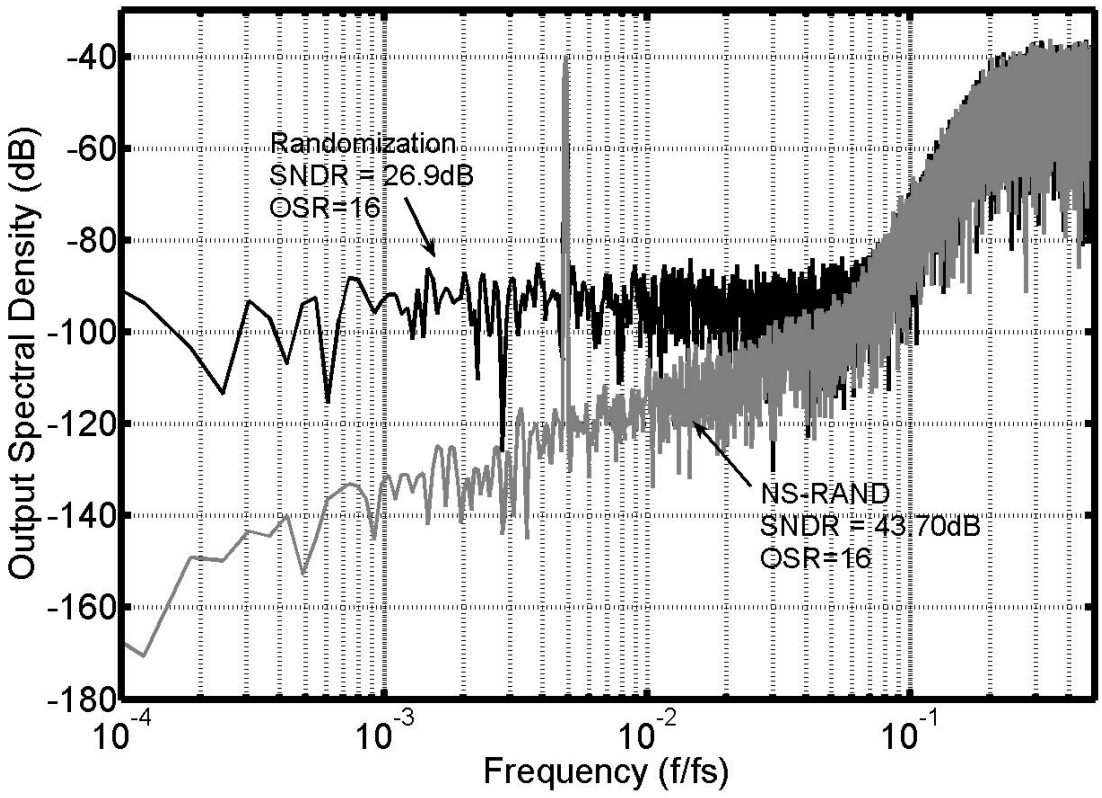


Figure 50. The 5th-order 4-bit quantization ΔΣM's output PSD with Randomization and NS-RAND.

Figure 51 shows that an improvement of about 20dB in SNDR can be obtained with NS-RAND over the normal randomization DEM at low input signal level. This is the same as predicted in Eq. (26), $\Delta SNR=20\log_{10}(OSR)-5.17=19dB$ at OSR=16. The SNDR and SNR have the same value, because the DAC with ideal randomization DEM is free of in-band tones.

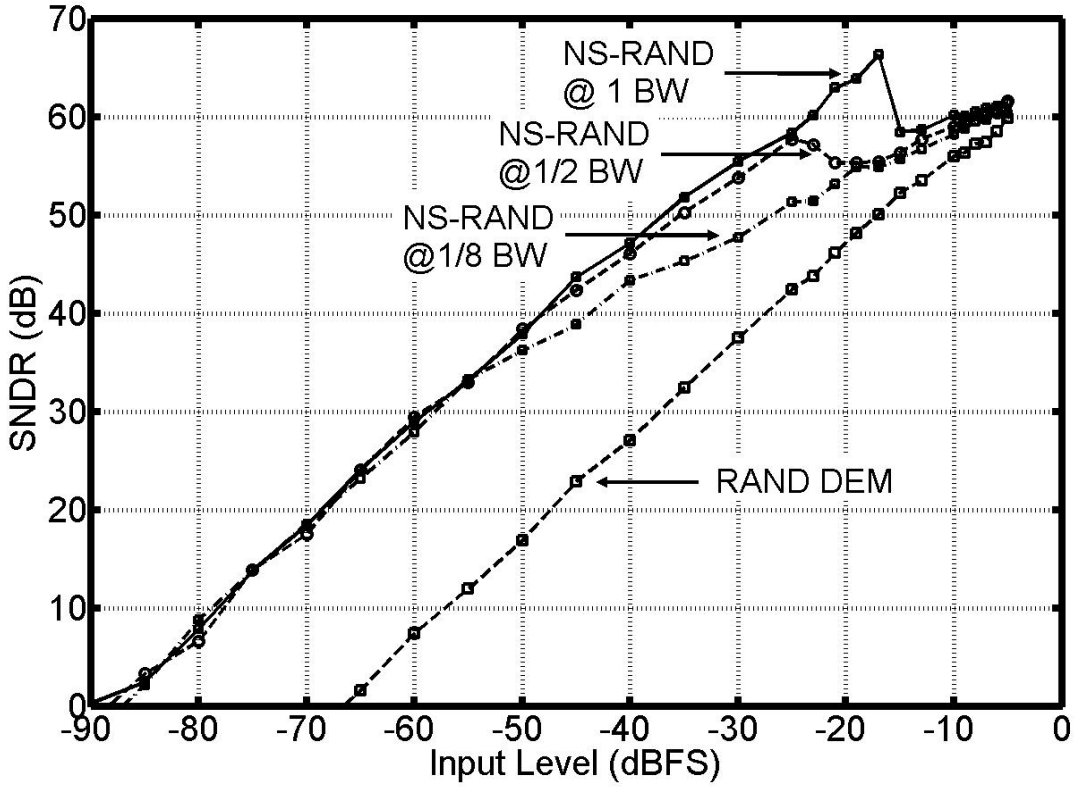


Figure 51. SNDR of the 5$^{th}$-order 4-bit quantization ΔΣM with NS-RAND at different frequencies of the input signal.

For the case of the input signal frequency at 1/8 BW, when the input signal level is higher than 40dBFS, the accumulator in NS-DEM starts overflowing and results in an increase of DAC noise floor to increase. Thus the SNDR of the ΔΣM with NS-RAND starts to drop gradually and eventually is almost equal to the value with randomization DEM when the input level reaches -5dBFS. At this input level, the accumulator and the differentiator are always reset. NS-DEM operates like normal DEM and thus their performances are the same.

The overflow of the NS-DEM will impair the noise shaping performance in some degree depending on how frequently the overflowing happens. The more frequently it takes place, the higher the DAC noise floor.

The higher frequency the input signal is, the less the accumulator of the NS-DEM

is prone to happen. As shown in Figure 51, the performance of the ΔΣM with the input signal at 1 BW, in terms of the peak SNR, is better than those with the input signal at 1/8 and 1/2 BW. The ΔΣM with the higher frequency of the input signal can obtain better performance because the accumulator in the NS-DEM is less prone to overflow with higher frequency of the input signal.

Figure 52 shows the SFDR of the 5$^{th}$-order 4-bit lowpass ΔΣM with NS-RAND and randomization DEM. The SFDR of the ΔΣM with NS-RAND also drops like SNDR due to the increased DAC noise floor.

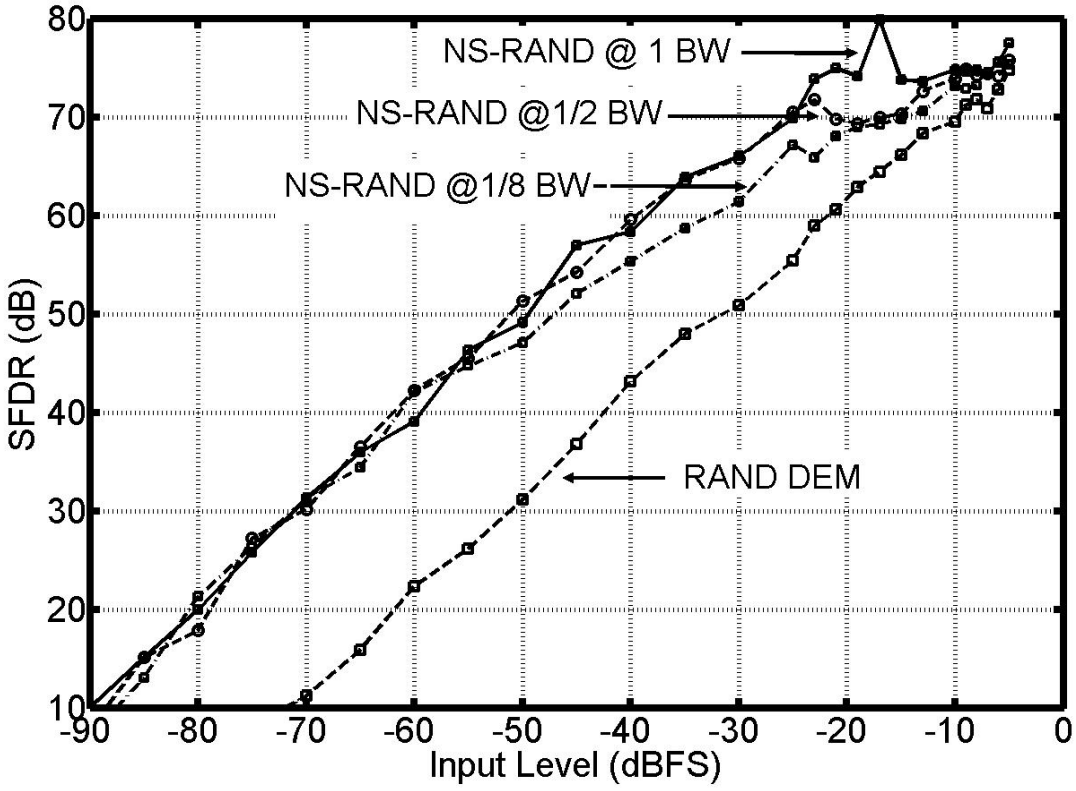


Figure 52. SFDR of the 5$^{th}$-order 4-bit lowpass ΔΣM with NS-RAND at different frequencies of the input signal

### 4.2.2 ΔΣM with Noise Shaping DWA

DWA algorithm is widely employed because it is easy to implement and shape the

DAC mismatch noise in the first-order. The drawback of DWA is the occurrence of the in-band tones, dependent on the amplitude and frequency of the input signal. When the NS-DWA (Noise Shaping DWA) is applied, the DAC noise floor is lower than the DWA's due to the introduced noise shaping of the differentiator, as shown in Figure 53. Figure 53 indicates that NS-DEM (NS-DWA) can not eliminate the tones generated by DEM (DWA), where the input signal's frequency is 10/2048·*f*s.

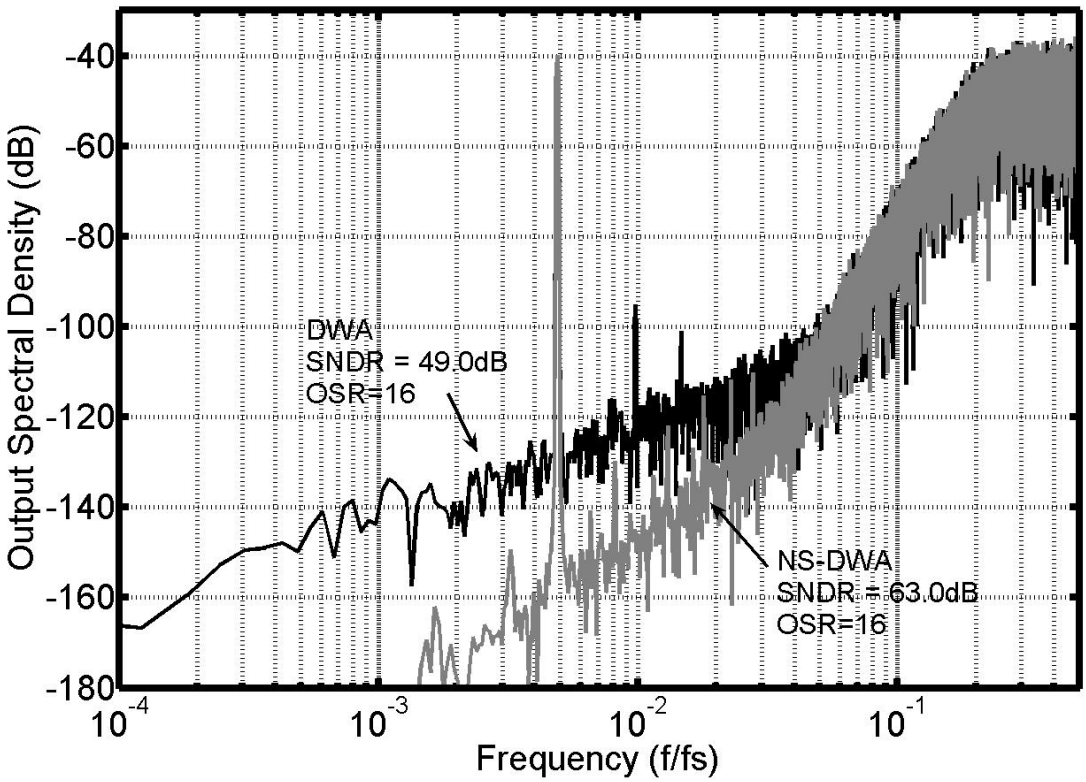


Figure 53. ΔΣM's output PSD with DWA and NS-DWA.

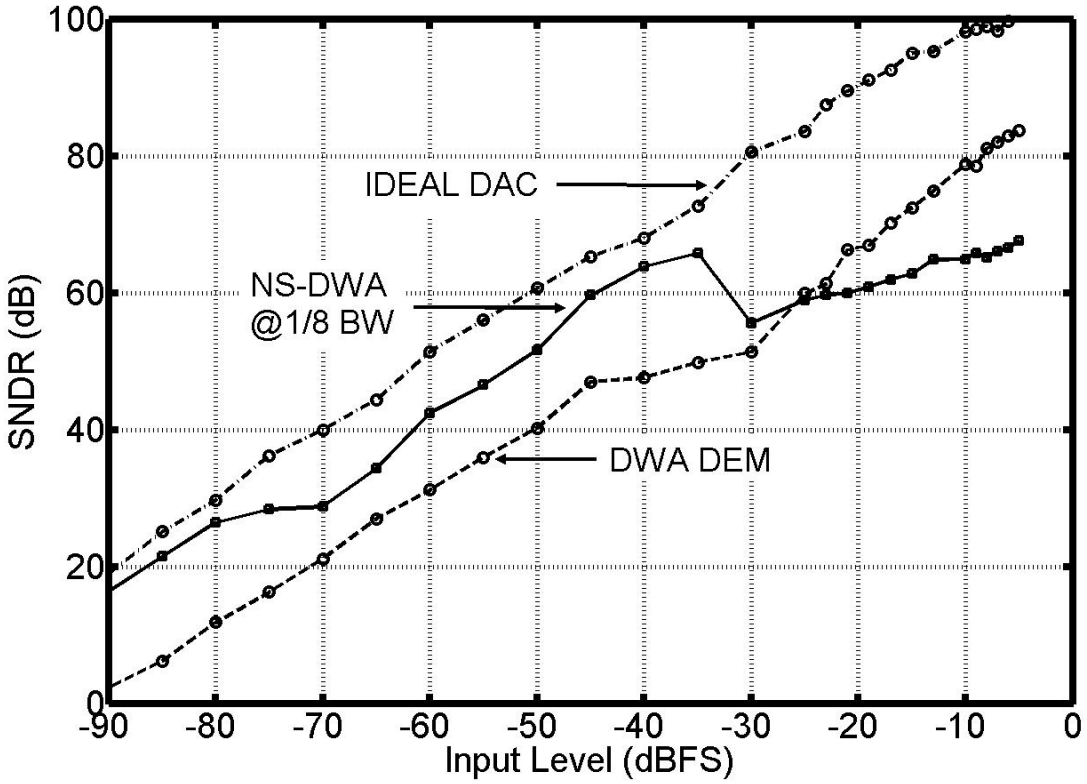


Figure 54. SNDR of the 5th-order 4-bit lowpass ΔΣM with NS-DWA, DWA and ideal DAC.

Figure 54 shows the SNDR of the 5th-order 4-bit lowpass ΔΣM with NS-DWA, DWA and ideal DAC, where the input signal is at 1/8 normalized BW. When the input level is low and the noise shaping is effective, the in-band noise floor is lower than DWA. Figure 55 shows the SFDR of the 5th-order 4-bit lowpass ΔΣM with NS-DWA, DWA and ideal DAC.

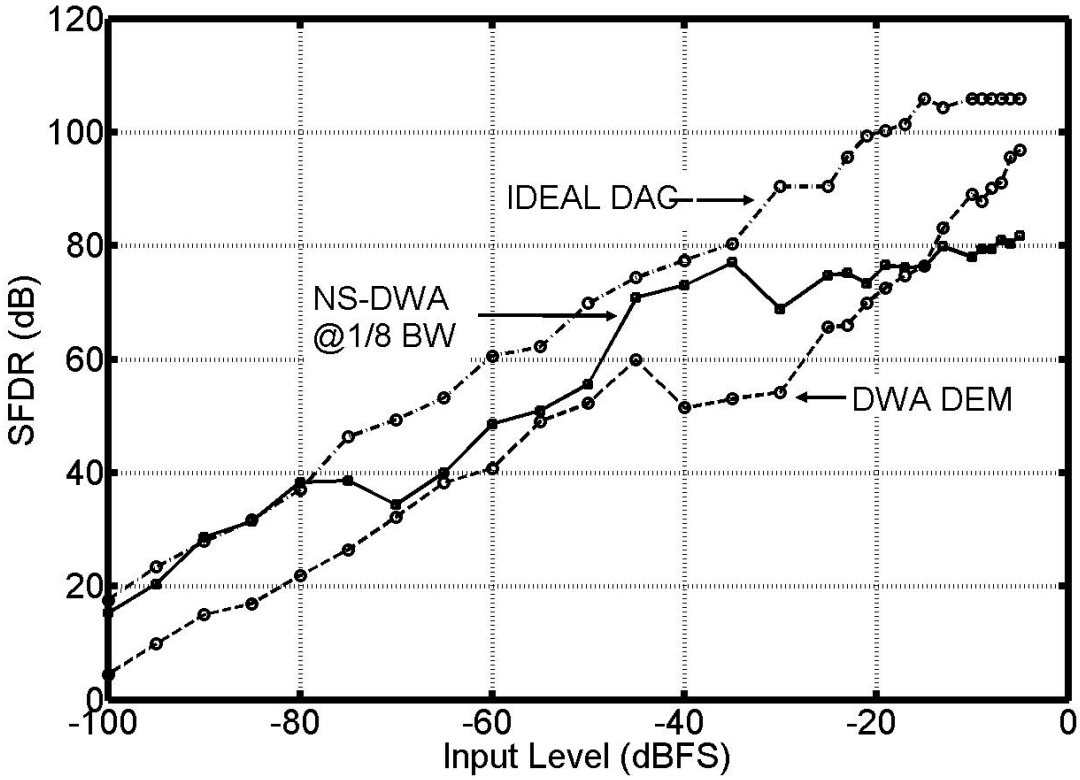


Figure 55. SFDR of the 5th-order 4-bit lowpass ΔΣM with NS-DWA, DWA and ideal DAC.

At high input signal level, the SNDR and SFDR degradation is due to the occurrence of the NS-DWA overflowing at high input level. Unlike NS-RAND, whose peak SNDR is the same with the randomization DEM's, the peak SNDR of NS-DWA is less than the DWA's. The NS-DWA overflowing and resetting impair the DWA's first order noise shaping to some degree. The noise floor is higher than DWA's at high input level.

In order to rescue the SNDR drop at high input level, the accumulator and the differentiator can be always disabled when the overflowing happens frequently. In other words, NS-DWA is switched to DWA mode. Therefore, the performance of NS-DWA is the same with DWA's at high input level. With this switching function of NS-DWA, the SNDR and SFDR of the lowpass ΔΣM are respectively shown in Figure

56 and Figure 57. The input signal at the different frequencies also results in the different SNDR and SFDR performance. Figure 58 and Figure 59 show the SNDR and SFDR of the lowpass ΔΣM with NS-DWA, where the frequency of the input signal are at 1/8, 1/2 and 1 normalized BW.

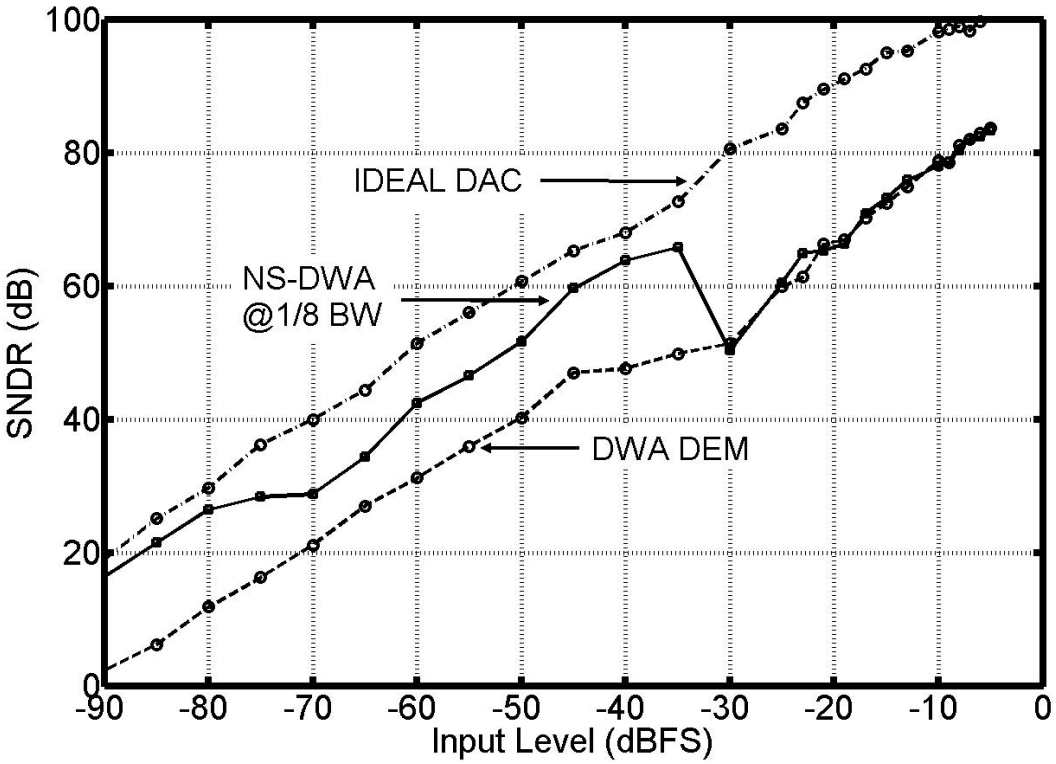


Figure 56. SNDR of the 5th-order 4-bit lowpass ΔΣM with switched NS-DWA, DWA and ideal DAC.

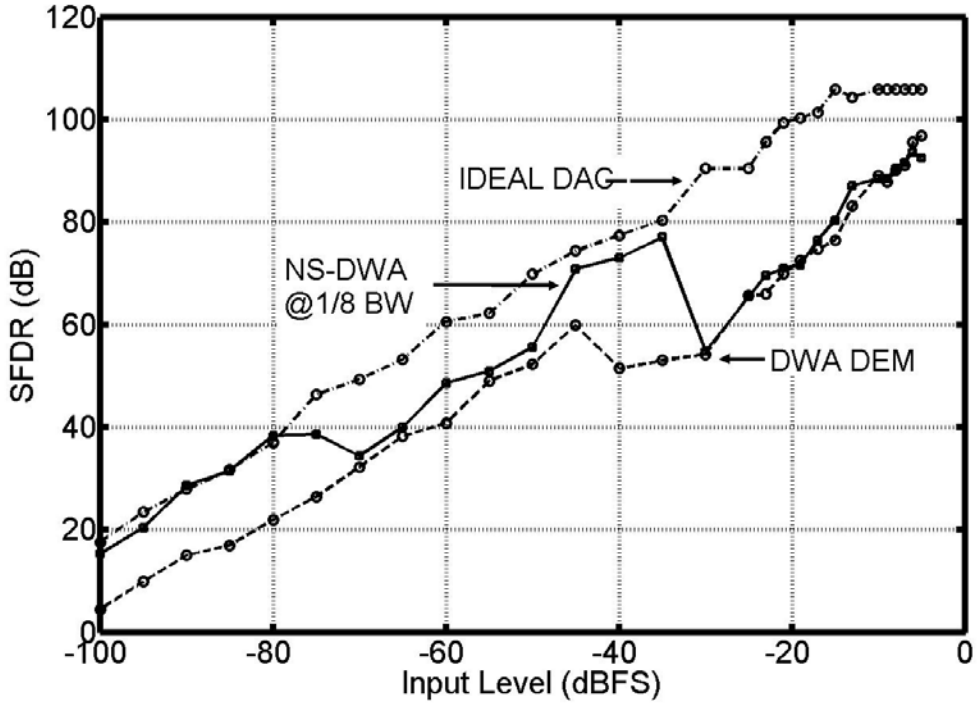


Figure 57. SFDR of the 5th-order 4-bit lowpass ΔΣM with switched NS-DWA, DWA and ideal DAC.

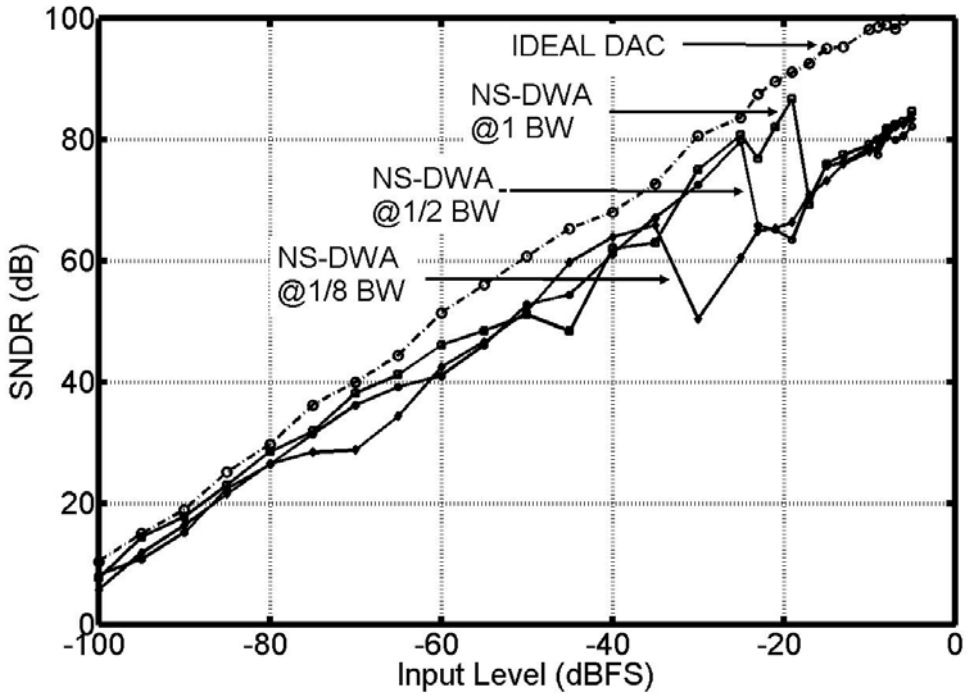


Figure 58. SNDR of the 5th-order 4-bit lowpass ΔΣM with NS-DWA at different frequencies of the input signal.

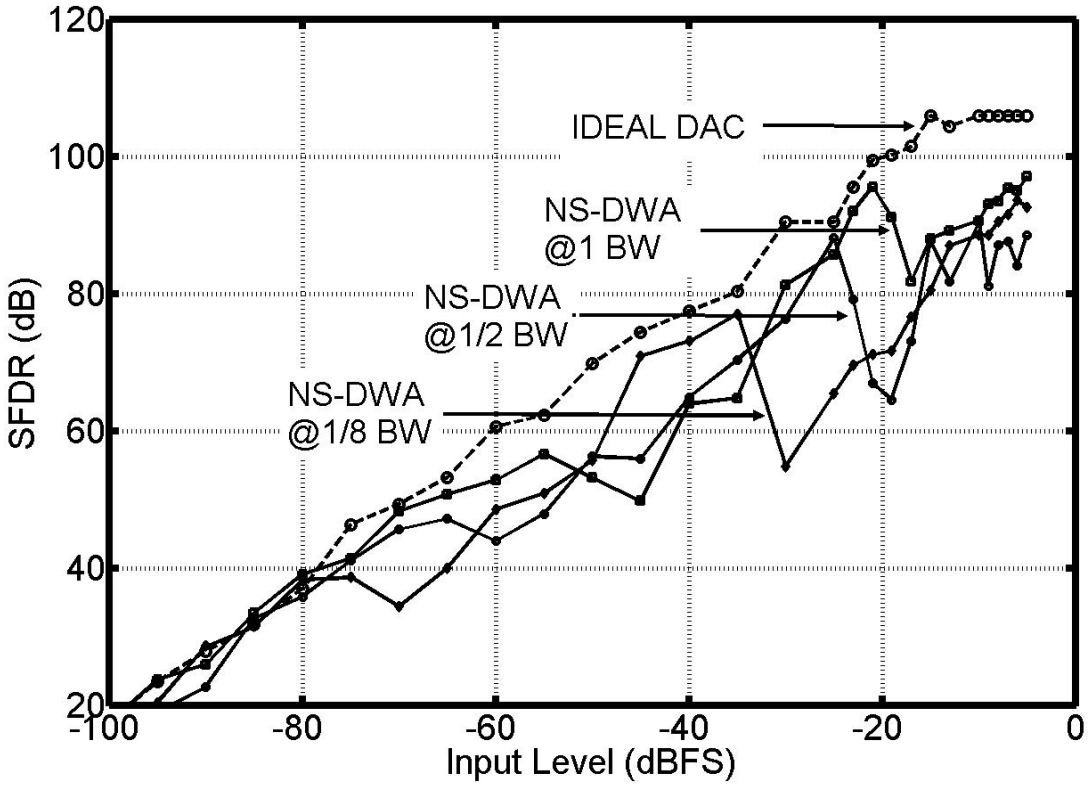


Figure 59. SFDR of the 5th-order 4-bit lowpass ΔΣM with NS-DWA at different frequencies of the input signal.

The performance of ΔΣM also depends on the internal DAC's resolution. Figure 60 shows that 6-b DAC is the best, because the peak SNDR is the highest. The input signal's frequency is fixed at 1/2 BW in the simulation. Although 6-b DAC performs better than the 4-b DAC does, the circuit scale of the 6-b DAC is four times of the 4-b one. Therefore, there is a trade-off between the performance and the hardware complexity. In a later implementation, a 4-b DAC is used in the experiment.

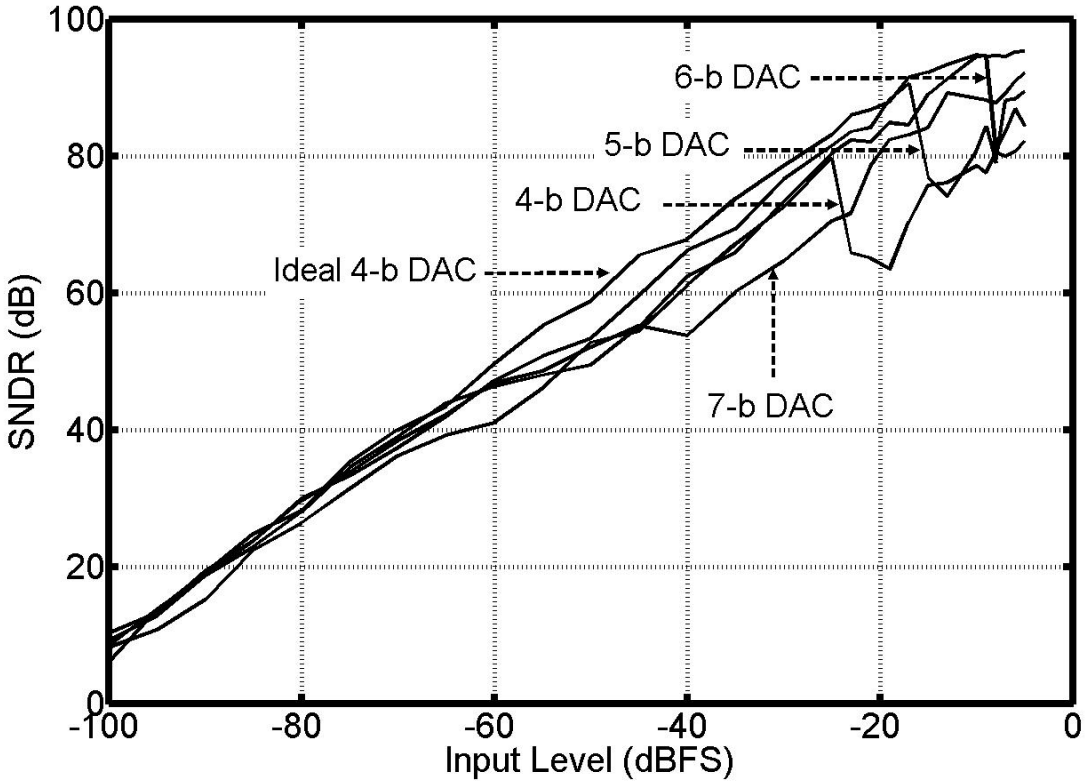


Figure 60. SNDR of the 5th-order 4-bit lowpass ΔΣM with NS-DWA at different DAC's resolution.

### 4.2.3 ΔΣM with Noise Shaping PDWA

PDWA (Partitioned DWA) algorithm is already discussed in the pervious chapter. PDWA reduces the in-band tones that are generated by the DWA. At the same time, the noise floor of DAC is increased in the signal band and SNDR is sacrificed. However, with the proposed NS-PDWA (Noise Shaping PDWA), the loss of SNDR, due to the increased in-band noise floor in PDWA, can be partly recovered by the first order noise shaping. Figure 61 shows ΔΣM's output PSD with PDWA and NS-PDWA. The input signal is -40dBFS and at 10/2048·*f*s. The noise floor of the ΔΣM with NS-PDWA is 1st order shaped and there is no obvious tone.

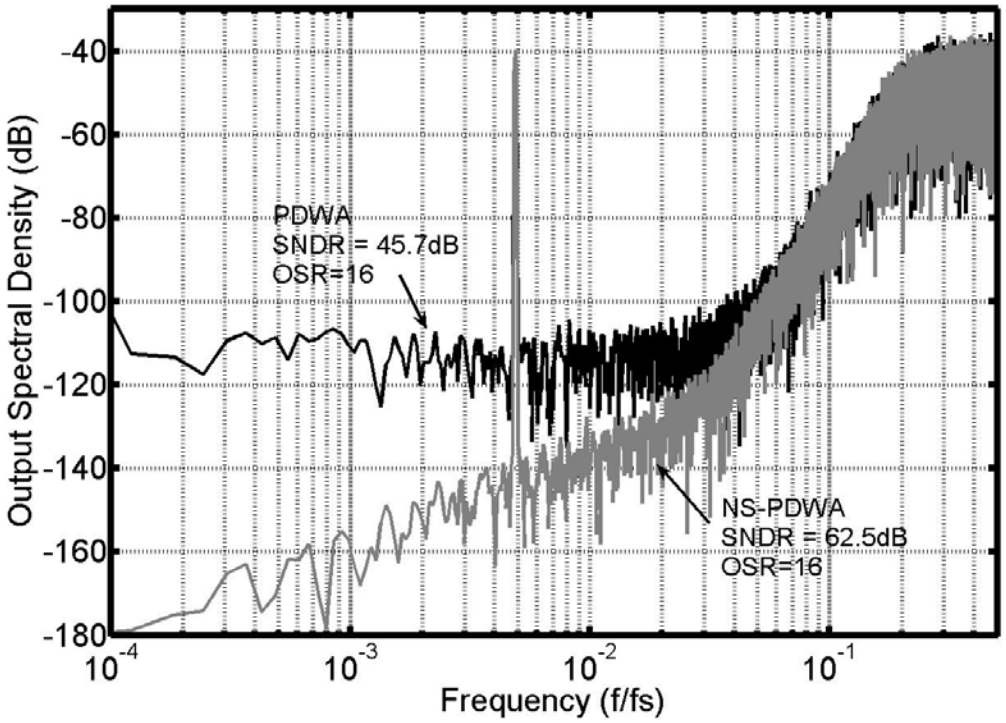


Figure 61. ΔΣM's output PSD with PDWA and NS-PDWA.

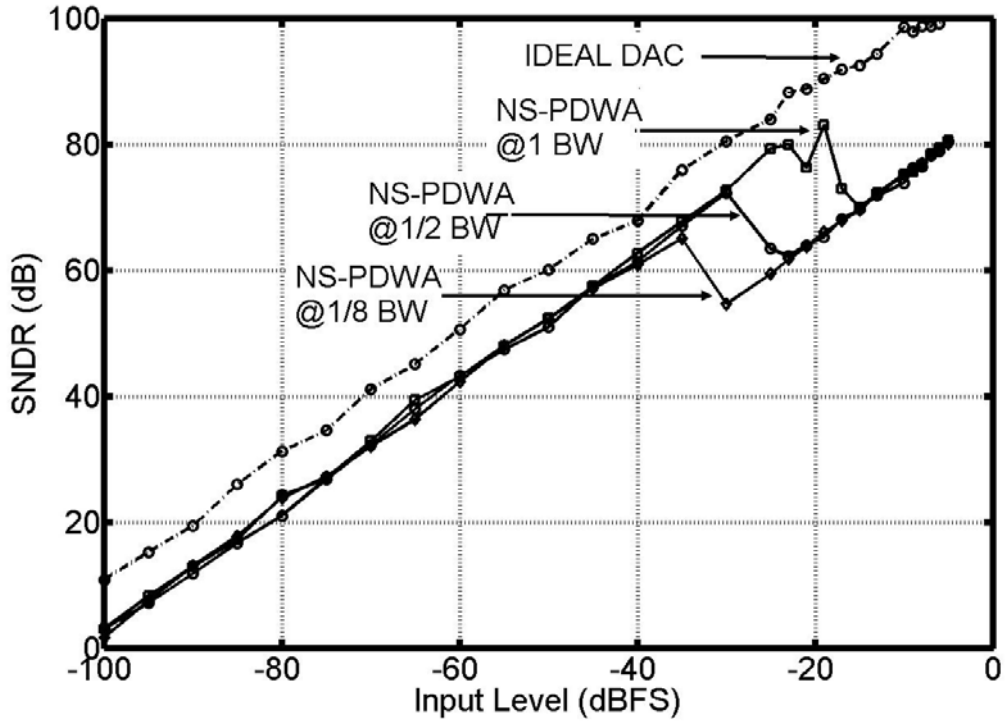


Figure 62. SNDR of the 5th-order 4-bit lowpass ΔΣM with NS-PDWA at different frequencies of the input signal.

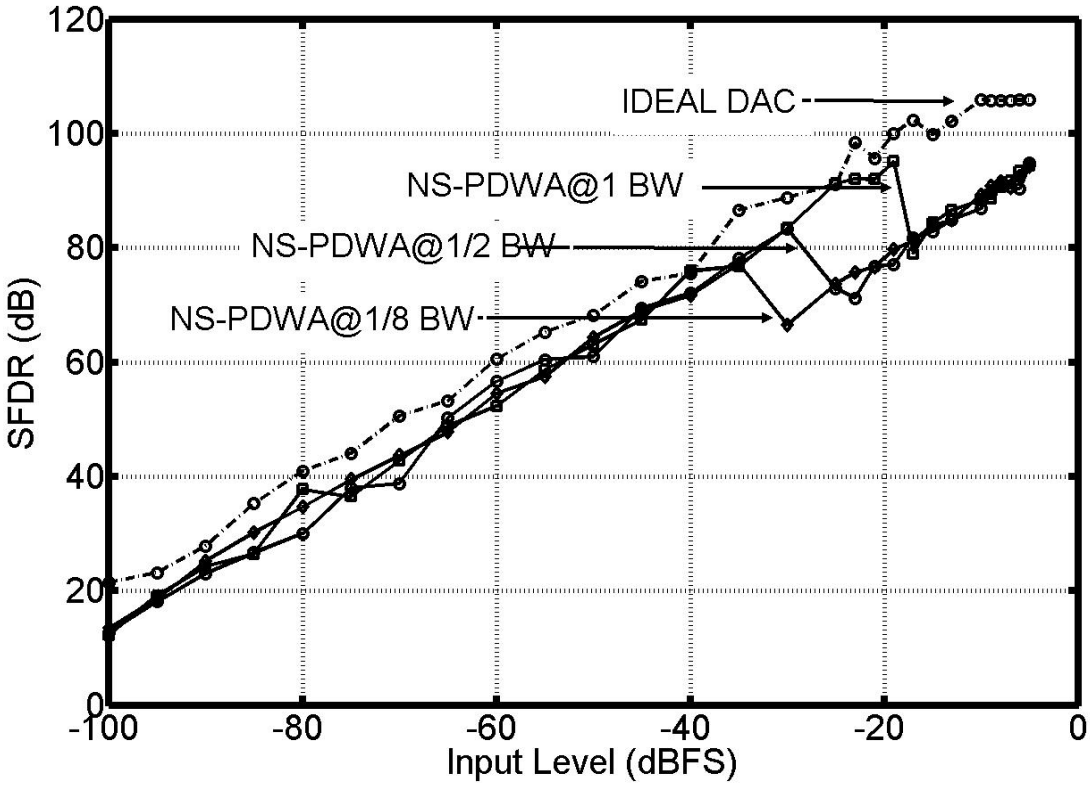


Figure 63. SFDR of the 5th-order 4-bit lowpass ΔΣM with NS-PDWA at different frequencies of the input signal.

Figure 62 and Figure 63 respectively demonstrate that the SNDR and SFDR of the 5th-order 4-bit lowpass ΔΣM with NS-PDWA at different frequencies of the input signal. In the above simulation of the noise shaping function in the NS-PDWA is disabled when the accumulator overflowing happens frequently.

The performance of ΔΣM also depends on the internal DAC's resolution. Figure 64 shows that 7-b DAC can obtain the best performance, because the peak SNDR is highest. The input signal's frequency is fixed at 1/2 BW in the simulation. Although the ΔΣM with a 7-b DAC can have the best performance, the hardware complexity in the implementation has to be considered. Therefore, a 4-b DAC with NS-PDWA is adopted in the later experiment of the 5th-order 4-bit lowpass ΔΣM because of its highest efficiency in the hardware.

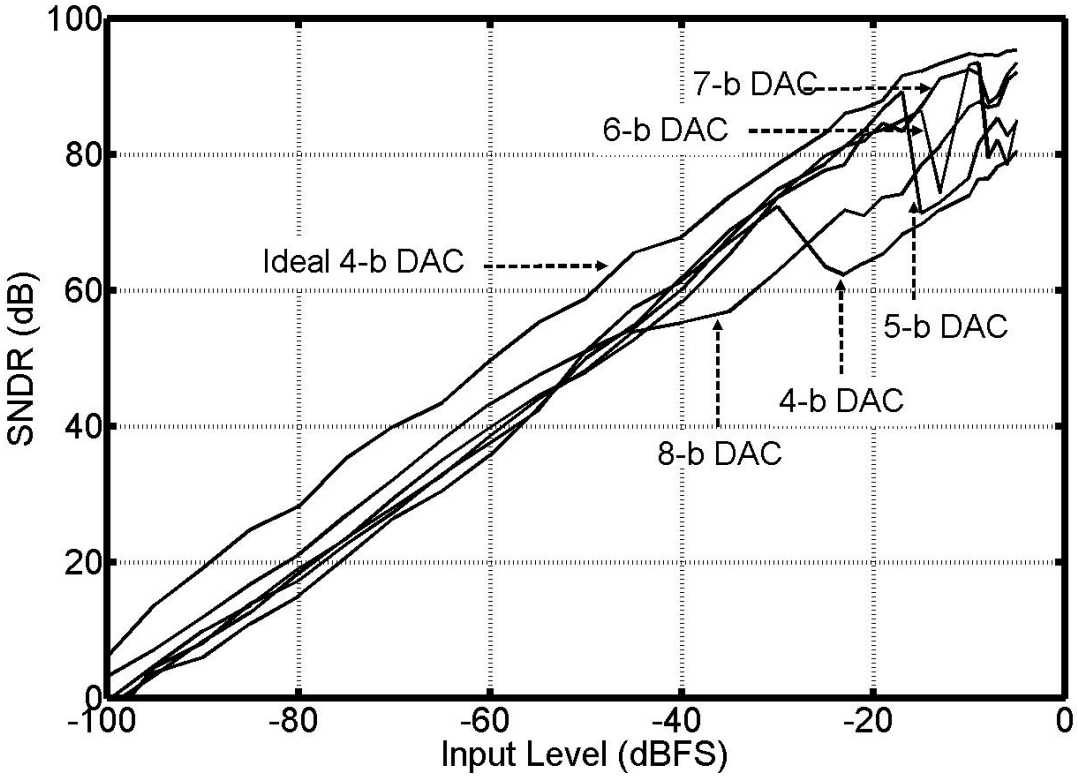


Figure 64. SNDR of the 5th-order 4-bit lowpass ΔΣM with NS-PDWA at different DAC's resolution.

### 4.2.4 ΔΣM with Noise Shaping Tree-structure DEM

The tree-structure DEM algorithm has already been discussed in the pervious chapter. Tree-structure DEM can also spectrally shape the DAC mismatch noise in the 1st or the 2nd order. Demonstrating the comparable performance with the DWA, the tree-structure DEM with the first order shaping has in-band tones problem as in DWA. The tree-structure with 2nd order noise shaping certainly calls for more hardware. Figure 65 shows the ΔΣM's output PSD with Tree-structure and NS-TS (Noise Shaping Tree-Structure). The input signal is -40dBFS and at 10/2048·$f_S$.

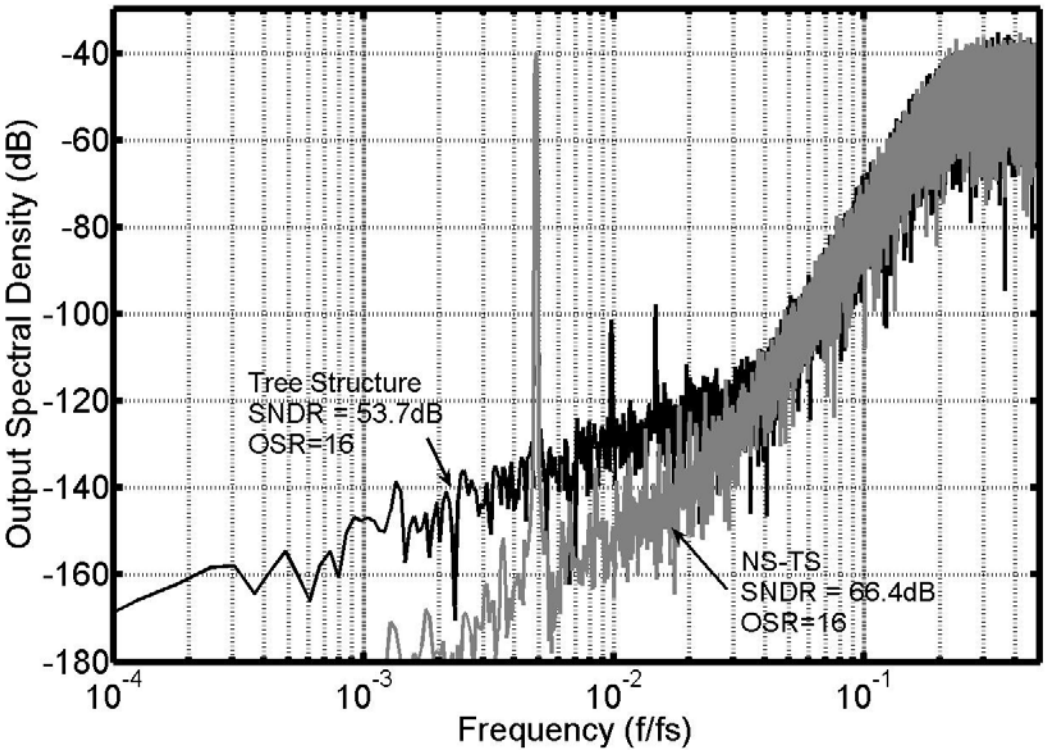


Figure 65. ΔΣM's output PSD with Tree-structure and NS-TS.

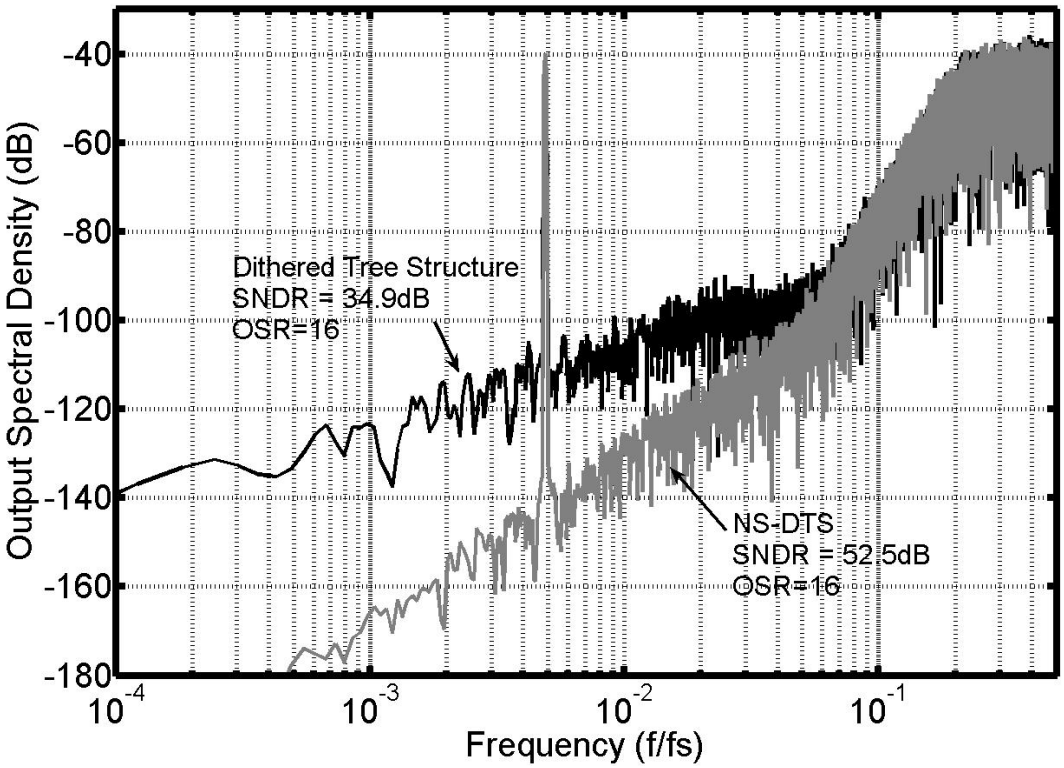


Figure 66. ΔΣM's output PSD with Dithered Tree-structure and NS-DTS.

The white dithering technique is employed to reduce the tones, but it has to increases the DAC noise floor. Figure 66 shows the ΔΣM's output PSD with Dithered Tree-structure and NS-DTS (Noise Shaping Tree-structure).

### 4.2.5 Summary

Table 2 summarizes the performance comparison of the ΔΣM with different DEMs and NS-DEMs. Among them, the NS-PDWA has the best performance. PDWA has the best compromise between resolution and linearity, as argued in the conclusion of Chapter 3. The ΔΣM with PDWA has the highest SNDR without obvious tones. Therefore, NS-PDWA adds an additional 1$^{st}$-order noise shaping benefit.

Table 2. Performance comparison between DEMs and NS-DEMs

| DEM/NS-DEM | SNDR (dB) | SFDR (dB) |
|---|---|---|
| Rand/NS-Rand | 26.9/43.7 | 44.1/57.4 |
| Tree-structure/NS-TS | 53.1/59.2 | 56.3/67.7 |
| Dithered Tree/NS-DTS | 34.9/52.5 | 50/64 |
| DWA/NS-DWA | 50/63 | 55.1/70.1 |
| PDWA/NS-PDWA | 44.6/62.9 | 70/90 |

In summary, although only five DEM algorithms were analyzed here with NS-DEM, the proposed NS-DEM should in principle work with any DEM algorithm. The advantage of NS-DEM is that the DAC linearity can be improved without sacrificing the SNR of ΔΣM.

The size of the accumulator and the DAC in NS-DEM are the same and could be

higher than the resolution of the quantizer. The accumulator is less prone to overflow when its length is longer, and hence less degradation in peak SNDR. However, the performance of the ΔΣM would drop, if the DAC size is higher than 6-bit in NS-DWA or 7-bit in NS-PDWA. It is because the rotation of the DAC unit element by DWA and PDWA is less efficient if more DAC elements are involved. It was theoretically proved in [39]. Figure 67 shows the SNDR of the 5$^{th}$-order 4-bit lowpass ΔΣM with PDWA and the different DAC. The SNDR performance of the ΔΣM with 8-bit DAC is lower than the one with 4-bit DAC. Considering that the DAC with higher resolution suffers more hardware penalty, 4-bit DAC is preferred.

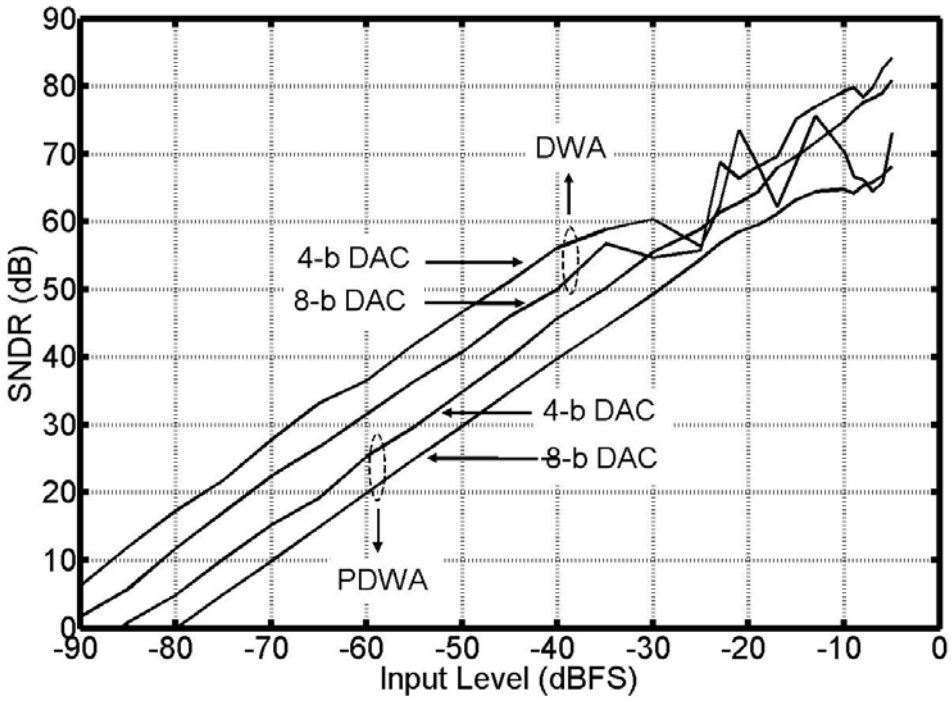


Figure 67. SNDR of the 5$^{th}$-order 4-bit lowpass ΔΣM with DWA, PDWA and the different DAC.

## 4.3 Implementation and Experiment

As explained in the previous chapter, the multi-bit modulator has several

advantages, such as the reduced quantization noise, the enhanced modulator stability and the relaxed settling requirement. However, the multi-bit DAC in the modulator will cause the linearity problem. The proposed NSDEM can improve the DAC linearity and resolution. To further validate the proposed noise shaping technique, an effective 5-bit DAC with a dither is implemented in a 0.35-μm CMOS process. The 3-bit dither is to mimic the noise floor and nonlinearity errors of non-ideal DAC with DEM. As shown in Figure 68, the two most significant bits of the PN (pseudo noise) code generator have 4 and 5 stages. This implies that PN codes are only pseudo-random and their periods are $2^4$-1 and $2^5$-1 clock cycles. Therefore, the tones resulted from the pseudo-random dither can be generated.

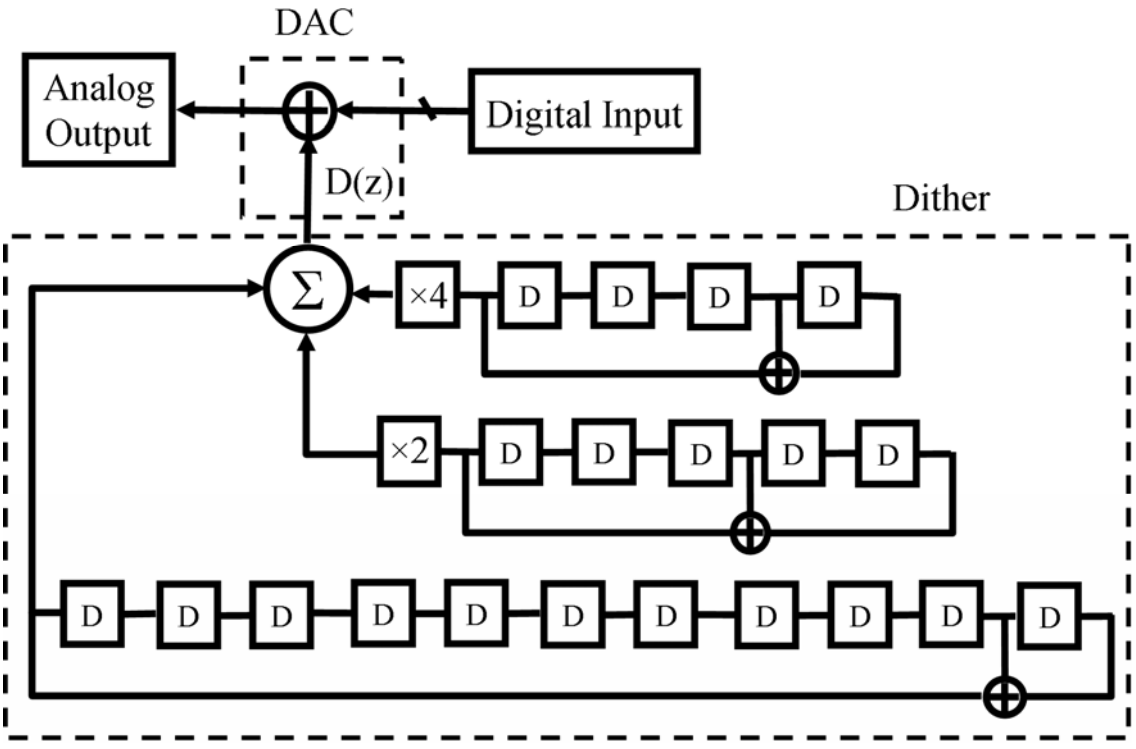


Figure 68. Dithered DAC in experiment

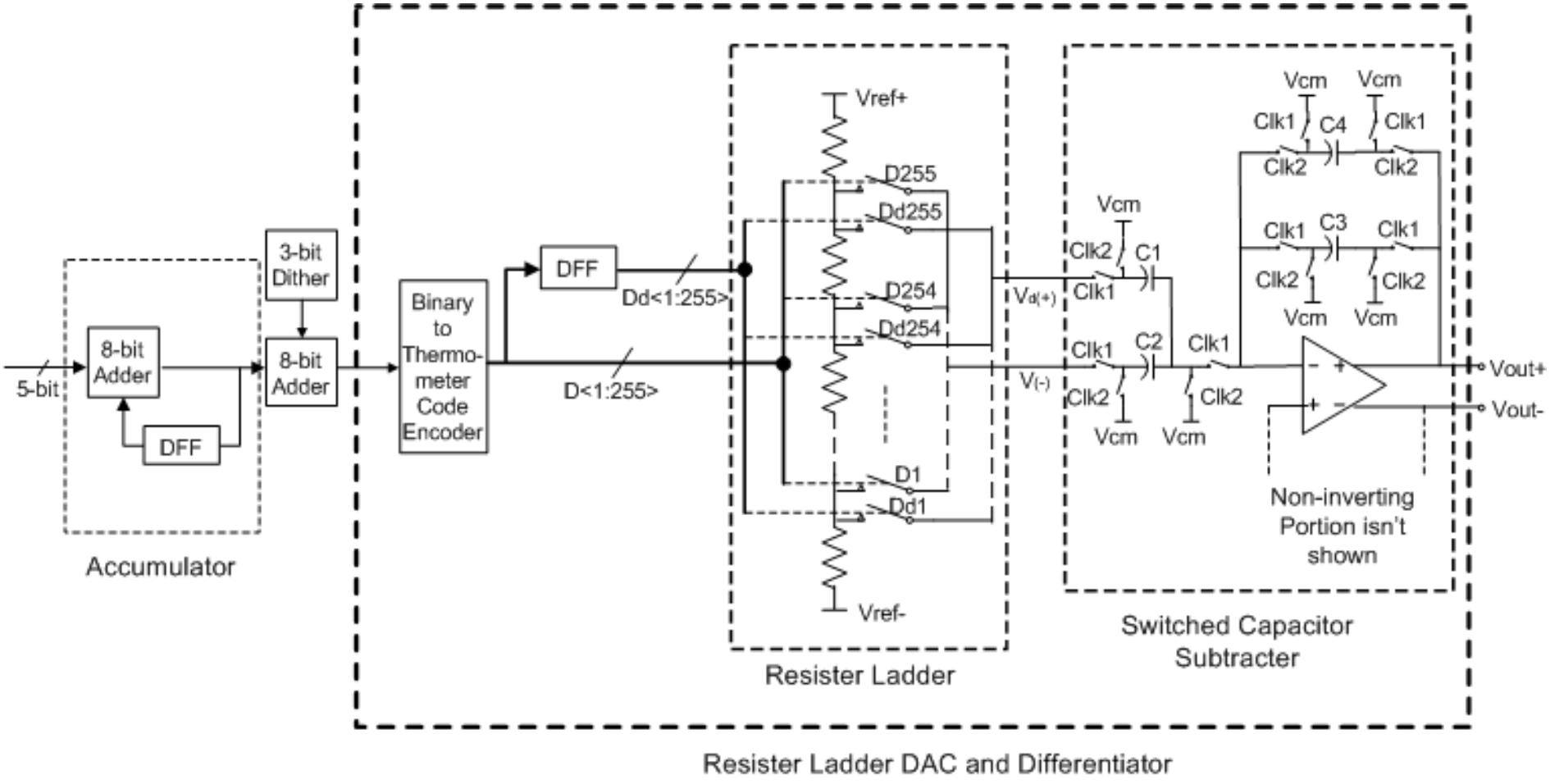


Figure 69. Schematic of the dithered DAC with the proposed noise shaping technique

Figure 69 depicts the resistor string DAC together with the accumulator, the differentiator and the dither. For the sake of simplicity, only the inverting portion is shown, although the circuit is fully differential. Since Differentiator is in the analog domain, it is combined with the DAC. The 5-bit input represents the output from a 5-bit quantizer in the delta-sigma modulator. An 8-bit accumulator is used to accommodate large signal. The accumulator will be reset to zero if it overflows. Consequently, the internal DAC employing NS-DEM should also be 8 bit to avoid the truncation. Although large accumulator is preferred, trade-off should be considered among performance, silicon area, and power consumption.

### 4.3.1 Accumulator

The implementation of accumulator is straightforward. $H_I(z)$ is realized by a 8-bit accumulator as indicated in Figure 69. The register, realized by D type Flip Flop (DFF), is limited to 8-bit. When the accumulator overflows, the register (DFF) in the accumulator is automatically reset to zero.

### 4.3.2 DAC and Differentiator

As indicated in Figure 69, a simple resistor ladder DAC is used, where the analog output is determined by the input digital signal that controls the switches. In our design, to facilitate the differentiation, a different switching scheme is adopted. There are two control signals; one is delayed by a clock cycle which the other is not. In Figure 69, Dd<1:255> is the control signal delayed by one clock cycle with respect to D<1:255>. There are two fully differential analog outputs, $V_d(+)$ and V(-) as indicated in Figure 69, controlled by Dd<1:255> and D<1:255> respectively. Among them, $V_d(+)$ is the delayed signal. Both are fed to a switch-capacitor (SC) subtractor. During Clk1, $V_d(-)$ should be subtracted from V(-).

Since $V_d(+)$ and $V_d(-)$ are fully differential signals and $V_d(+) = -V_d(-)$ with reference to the common-mode level, instead of subtracting Vd(-) from V(-), Vd(+) is added to V(-), thus realizing the differentiation.

In the SC subtractor, the opamp is the conventional telescopic type using the resistive sensing CMFB (common-mode feedback) circuit. Clk1 and Clk2 are two non-overlapping clock signals. Clk1 is the subtract mode and Clk2 is the reset mode. A small capacitor, C4, is used to avoid the opamp being open loop.

### 4.3.3 Measurement Result

The dithered DAC chip is fabricated in a 0.35-μm standard CMOS process and packaged in a 48-pin DIL package. The test setup is given in Figure 70. The analog sinusoid input signal is digitized by a 5-bit ideal ADC in Maltab and loaded in a pattern generator in the logic analyzer (HP 1661EP) and used as the input signal to DAC. The Agilent dynamic signal analyzer 35670A is used to measure the output PSD (Power Spectrum Density). To make comparison between the conventional DAC and the one with proposed noise-shaping, several control signals were provided on chip. By switching on and off these control signals, the proposed noise shaping can be switched on and off accordingly.

Figure 71a shows the output spectrum when dither is on and the noise shaping is off. The noise floor is relatively flat, showing the pseudo-white noise generated by dither. The appearance of the tones is due to the pseudo-random generator as explained in the previous section. Figure 71b shows the output spectrum of the dithered DAC with the proposed NS-DEM. The noise shaping effect can be clearly seen. A zoom-in view of Figure 71b is produced in Figure 71c where it shows that the dithered DAC noise floor is shaped by NS-DEM with a slop of 18dB/decade.This is slightly less than the ideal first-order shaping, 20dB/decade, due to the non-ideal subtractor. Figure 72 is

the die microphotograph. The active chip area is 2.0mm×2.5mm and measured power consumption is 15mW. Table 3 summarizes the testing results.

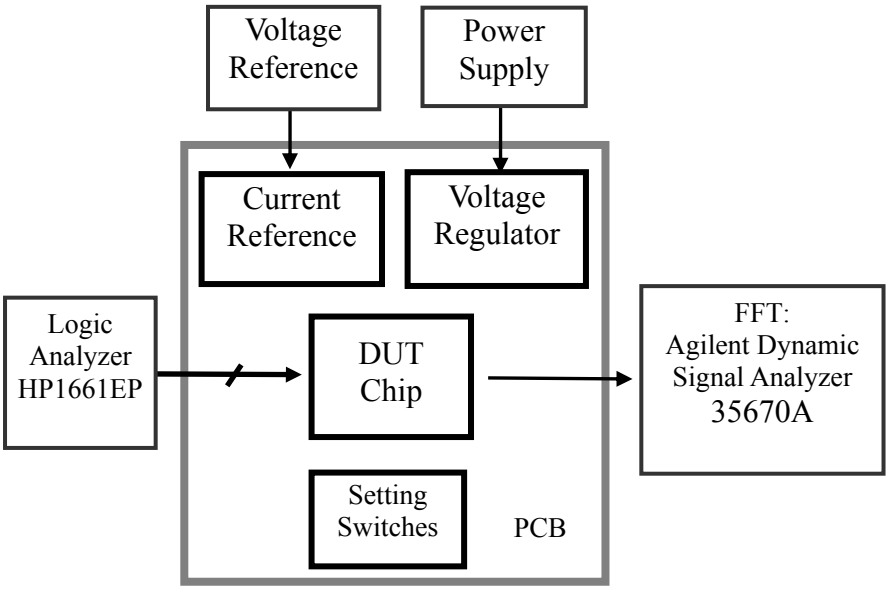


Figure 70. Testing Schematic

## 4.4 Summary

A new noise shaping DEM technique (NS-DEM) has been proposed to reduce the inherent DAC noise in multi-bit ΔΣM. NS-DEM can work with most existing DEM techniques although only five typical DEM algorithms are demonstrated in a $5^{th}$-order 5-bit lowpass ΔΣM. The behavioural simulation illustrates that NS-PDWA gives the best performance, yielding a 20dB SNDR improvement over the PDWA alone.

The proposed NS-DEM has also been experimentally demonstrated in a dithered DAC, fabricated in a 0.35-μm CMOS process. The first-order noise shaping has been observed in the measurement and the result validates the proposed concept. The proposed NS-DEM technique is especially suitable for the implementation of high-performance multi-bit ΔΣM.

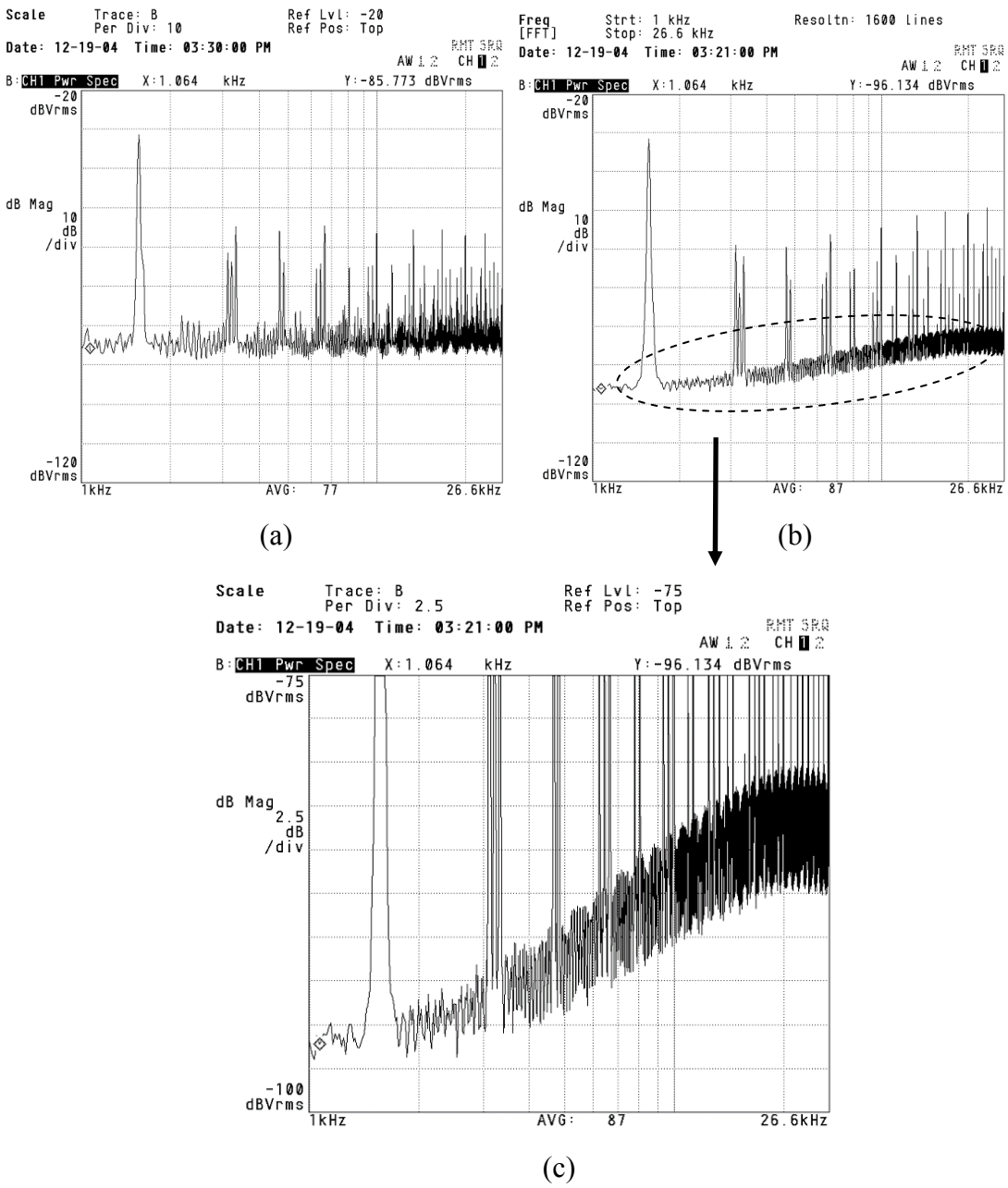


Figure 71. Measured output spectrum of the dithered DAC (a) with dither only; (b) with the dither and NS-DEM; (c) zoom-in view of (b).

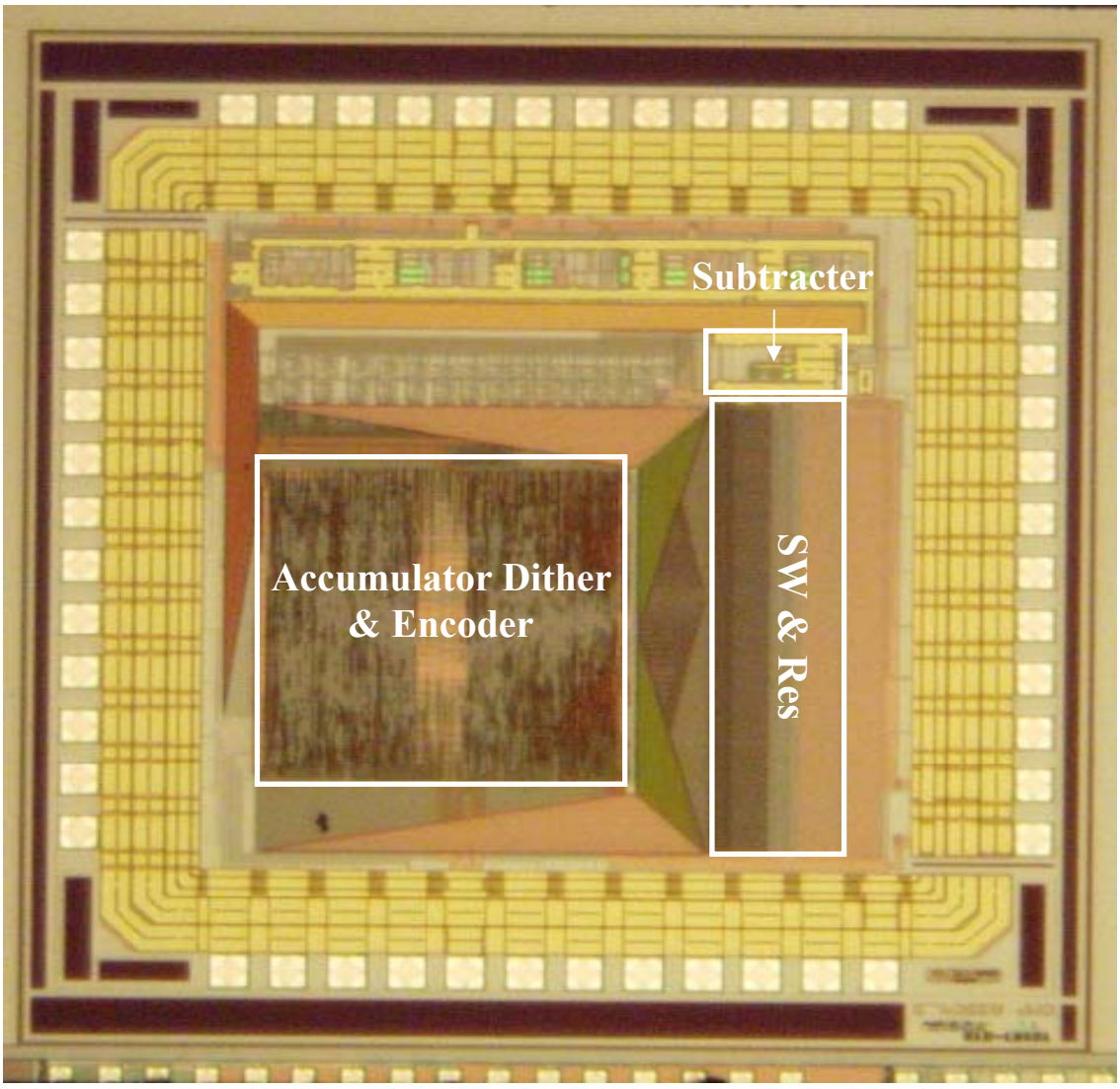


Figure 72. Die microphotograph

Table 3. Summary of Measurement Results

| Parameters | Measured Results |
|---|---|
| Data & Clk Rate | 50 KSample/s |
| Active Chip Area | 2.0mm×2.5mm |
| Power consumption | 15mW |
| Dither to DAC | 3 bit |
| DAC resolution | 5 bit |
| Noise shaping | 18dB/decade |
| Technology | AMS 0.35-µm CMOS |
| Power Supply | 3.3 V |

# Chapter 5 Delta-Sigma Modulator Design

To further evaluate NS-DEM, a 5th-order 4-b quantization lowpass ΔΣM with NS-PDWA is implemented in a 0.35-μm CMOS process. This chapter describes the design of the ΔΣM which is targeted for the ADSL2+ application. The top-down design methodology, from the system specification to the transistor level implementation, is adopted.

## 5.1 ADSL (Asymmetric Digital Subscriber Line)

ADSL (Asymmetric Digital Subscriber Line) is a form of DSL, a data communication technology that enables faster data transmission over copper telephone lines than a conventional voice band modem can provide. It does this by utilizing frequencies that are not used by a voice telephone call. A splitter allows a single telephone connection to be used for both ADSL service and voice calls at the same time. Because phone lines vary in quality and were not originally engineered with ADSL, it can only be used over short distances, typically less than 3 miles (5 km).

Figure 73 shows the spectrum of ADSL system [29]. ADSL uses two separate frequency bands, referred to as the upstream and downstream bands. The upstream band is used for communication from the end user to the telephone central office. The downstream band is used for communicating from the central office to the end user. With standard ADSL, the band from 26 kHz to 138 kHz is used for upstream communication, while 138 kHz – 1104 kHz is used for downstream communication. Each of these is further divided into smaller frequency channels of 4.3125 KHz. These tones are QAM modulated and individually optimized as a function of the channel

quality (SNR of the channel). During initial training, the ADSL modem tests available channels that have an acceptable signal-to-noise ratio. The distance from the telephone exchange, noise on the copper wire or interference from AM radio stations may introduce errors on some frequencies. By keeping the channels small, a high error rate on one frequency would not render the line unusable. If the channel quality is too low, that tone will not be used. The channel will not be used, merely resulting in reduced throughput on the ADSL connection. The maximum variation of all used tone's signal strength is limited to 3dB [61]. More detailed information on ADSL can found in [61][62][63][64].

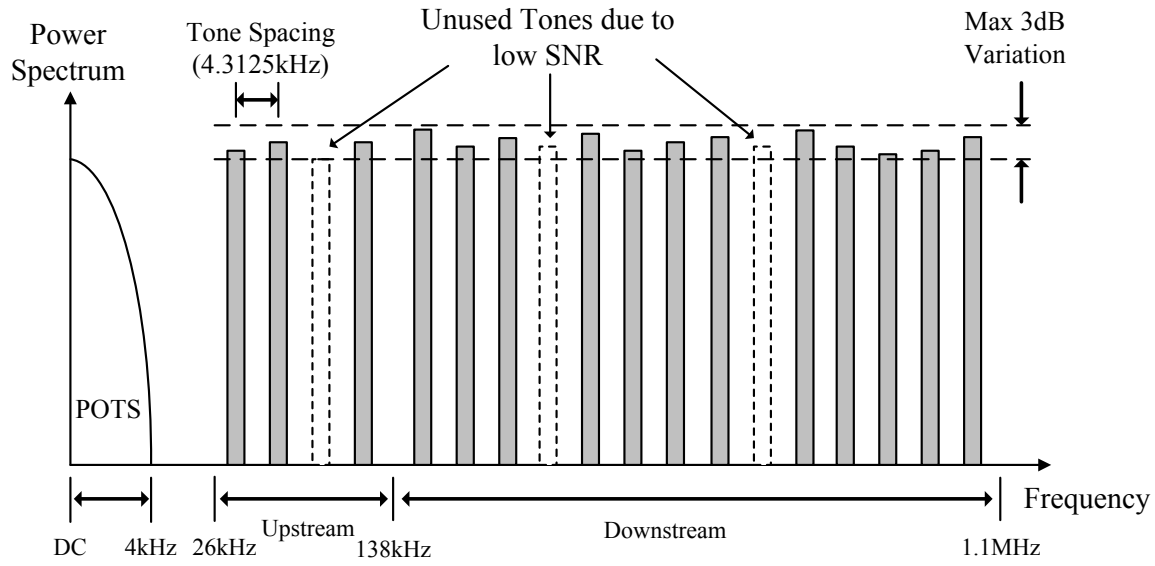


Figure 73. Spectrum of ADSL system

A simplified block diagram of ADSL modem is shown in Figure 74 [29]. In the front end of the ADSL, a high-pass filter (HPF) is used to filter out the low frequency POTS spectrum. The following hybrid is to separate the strong transmitted signals from the weak received signal and thus prevent saturation of the receive path. The HPF in the receiver path further reduces the out-of-band signals such as the echo from the transmitted signal. After the removal of the strong echo signal by the HPF, a VGA with

a typical gain range of 27dB is used to amplify the filtered signal in order to ensure that it optimally fits in with the input dynamic range of the ADC, which is preceded by an anti-alias filter. Finally, an FFT, demapper and decoder are used to extract the data bits. The ADSL modem requires the ADC resolution above 12b [29].

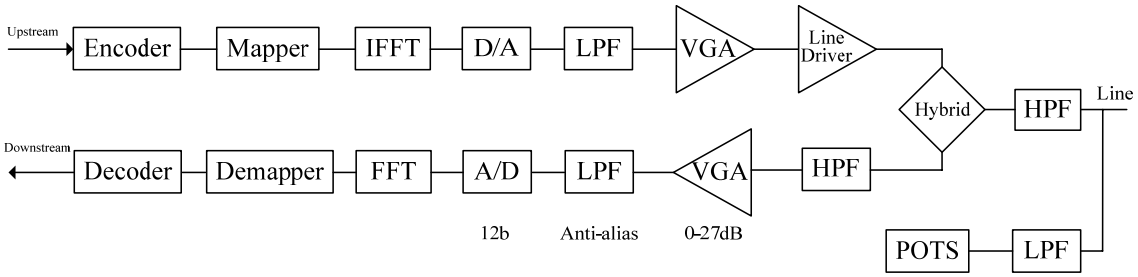


Figure 74. Block diagram of ADSL modem

ADSL2+ is an upgraded ADSL technology, which is the same as ADSL except its capability of doubling the frequency band of typical ADSL connections from 1.1 MHz to 2.2 MHz. The typical downstream data spectrum of ADSL2+ is from 138 kHz to 2.2MHz, unlike the one of ADSL that is from 138kHz to 1.1MHz.

The 12b ADC digitizes the received data in the downstream. Besides the high SNR requirement, the xDSL also puts high requirement on the the spurious free dynamic range (SFDR). In xDSL, discrete multi-tone (DMT) modulation scheme is used and the DMT signal requires a highly linear signal chain because any nonlinearity in the chain will introduce the inter-modulation distortion that overlaps the sub-carries, badly interfering the sub-channels' signal. Thus the ADC in an xDSL receiver has to be of high-resolution and high-linearity. Delta-sigma modulators (ΔΣMs) are regarded as a good candidate for such applications. To fulfill this requirement, most of the recently published discrete-time (DT) ΔΣMs employ multi-bit quantization to reduce the sampling frequency.

## 5.2 Architecture Design

Due to the demands for high data rate, xDSL has pushed the signal BW from 1.1MHz for ADSL (Asymmetric Digital Subscriber Line) to 12.5MHz for VDSL (Very-High-Bit-Rate Digital Subscriber Line). The over-sampling ratio (OSR) is usually squeezed in the range of 8-16 to relax the requirements on the speed of the OTA and the settling of the switch-capacitor circuit. Considering this, 8x OSR is chosen for the ΔΣM in this design, so that this design can be easily applied to wider signal BW application, such as VDSL. With the bandwidth of 2.2MHz for ADSL2+ application, the sampling clock frequency is 35.2MHz.

To meet 12b to 14b resolution requirement, the order of the filter and the quantizer resolution have to be determined. Theoretically, the higher the values of these two parameters, the better the ΔΣM performance for a given bandwidth. However, in practice, the circuit complexity, power consumption, and chip area have to be considered as well. To determine these two system-level parameters, MATLAB with a Delta-Sigma toolbox [66] is used for the simulation. The maximum out-of-band gain of the noise transfer function (NTF) is set to 6 to ensure the stability. 10dB margin is added to the signal-to-quantization-noise ratio (SQNR) to ensure that the quantization error is well below the thermal noise of the switches and the MOS device.

Three different options are explored and the results are shown in Table 4. Considering the ΔΣM performance, circuit complexity, power consumption, and chip area, option 1, that is, an 8x OSR $5^{th}$-order 4-b quantization single loop feed-forward (FF) switch-capacitor filter architecture, is chosen with ADSL2+ as the targeted application.

Table 4. SQNR vs. ΔΣM Architecture

| Option | OSR | Filter's Order | Quantization | Peak SQNR |
|---|---|---|---|---|
| 1 | 8 | 5 | 4-b | 90dB |
| 2 | 8 | 6 | 3-b | 85dB |
| 3 | 8 | 4 | 5-b | 89dB |

The detail of the ΔΣM architecture is given in Figure 75. In our design, Partitioned Data Weighted Averaging (PDWA) [67] is chosen to realize the DEM. PDWA is evolved from Data Weighted Averaging (DWA) [67] and can effectively reduce the in-band tones resulted from DWA with less SNR degradation. In NS-DEM, the PDWA reduces the spurious tones caused by DAC nonlinearity, while the differentiator, $H_D(z)$, provides a first-order noise shaping to the noise floor of the DAC and removes the noise out of signal band, resulting in the improvements on both SFDR and SNR. The NS-DEM that employs PDWA for its DEM is referred to as noise shaping PDWA, or NS-PDWA hereafter.

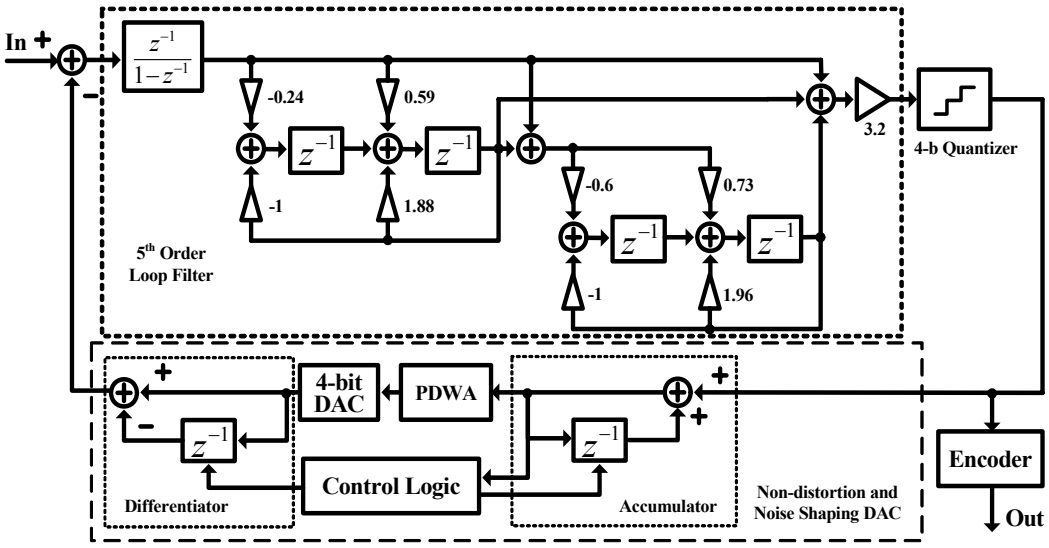


Figure 75. Proposed 5th order 4-b quantization ΔΣM employing NS-PDWA.

The single loop structure is adopted in this paper because the coefficient variations of up to 20% and large integrator leakage can still be tolerated without a noticeable loss of the performance in the ΔΣM. The feed-forward (FF) loop filter topology generally has better suppression of the disturbances generated at the loop filter internal nodes than the feedback (FB) one [15]. Also the output swings of the FF filter internal integrators are less than those of the FB [14]. As shown in Figure 75, the loop filter has an integrator at in the front, followed by two second-order infinite impulse response (IIR) blocks[67]. The ΔΣM has only one global feedback path. The low output swings of the internal blocks relax the requirement for OTA. The zeros of noise transfer function or the poles of the filter are spread over the signal band to make better quantization noise suppression.

## 5.3 Behavior Verification

Figure 76 shows the 262,144 points FFT plot of the output spectrum with NS-PDWA and PDWA respectively in the MATLAB simulation. Evidently the noise floor is lowered when the NS-PDWA is on and the total in-band noise is reduced by 10.2dB. The noise floor is mainly limited by quantization noise since the DAC noise is shaped out of signal band. The input signal locates at $f$s·11/2048. In the simulations, a standard deviation of 0.5% is assumed for the mismatch of the DAC unit elements, which is a typical mismatch of 1pF metal-wall capacitors in the advanced full digital process [67].

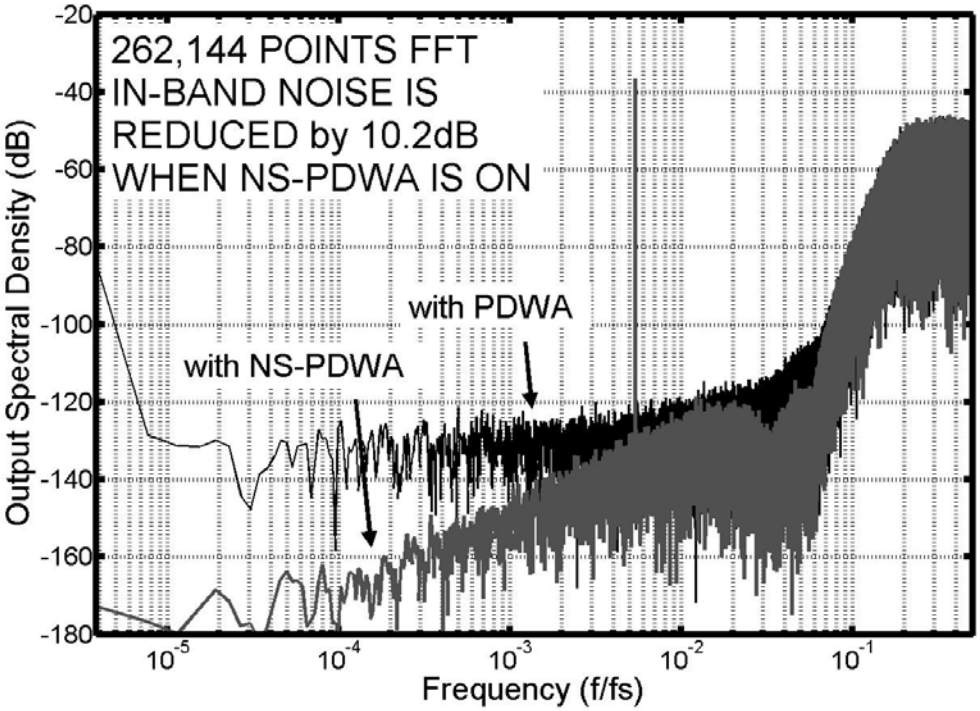


Figure 76. Spectrum Plots of the ΔΣM employing NS-PDWA and PDWA with 0.5% DAC mismatch.

Figure 77 shows the comparison of SNDR plots for the ΔΣM with NS-PDWA, PDWA and ideal DAC, respectively. The SFDR between NS-PDWA and PDWA are similar because PDWA has effectively suppressed the tones below the noise floor. However, the SNDR with NS-PDWA is improved by around 10dB compared to the one with PDWA alone when the input signal level is less than -20dBFS. For the input signal above -20dBFS, the SNDR drops to that of PDWA. This is due to the accumulator's overflow and the disabled noise shaping.

As discussed previously, ADSL divides the frequency band into subcarriers. Each of these subcarriers is individually QAM modulated with a variable number of data bits (2… 15 bits) dependent on the SNR of the channel [61]. The higher the SNR, the more the number of data bits. Thus the improved SNR of the ΔΣM with NS-PDWA

produces higher throughput in the ADSL connection.

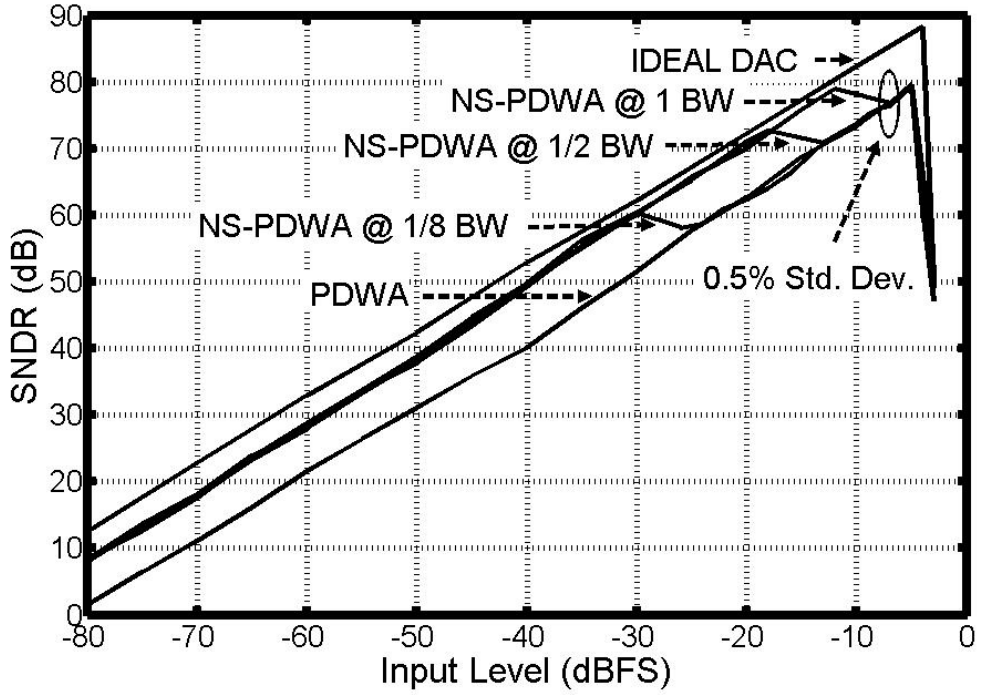


Figure 77. SNDR plots for ΔΣMs employing ideal DAC, NS-PDWA and PDWA, respectively, with 0.5% DAC mismatch

## 5.4 Implementation and Verification

Figure 78 shows the circuit-level implementation of the proposed 5$^{th}$-order 4-b quantization lowpass ΔΣM employing NS-PDWA. The 5$^{th}$-order loop filter is realized with a 5-stage switched-capacitor circuit followed by an amplification stage to boost the signal amplitude. The quantizer is a 4-b flash ADC with thermalmeter coded output that drives the NS-PDWA block consisting of a 4-b accumulator, PDWA, and a differentiator, which is incorporated into the 4-bit DAC. The output of the ΔΣM, taken after the encoder, is in binary format.

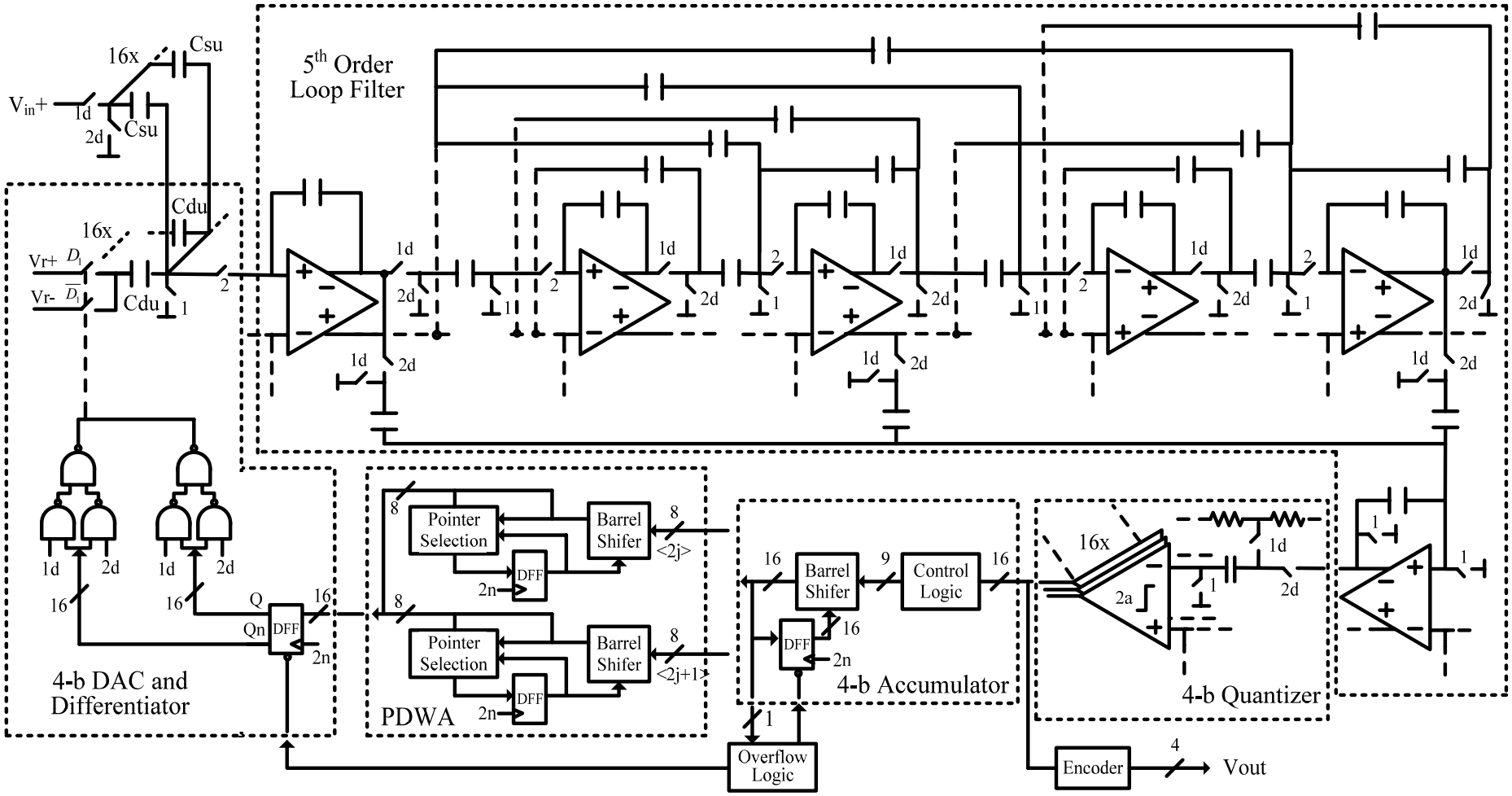


Figure 78. Schematic of the 5th order 4-b quantization ΔΣM employing NS-PDWA (only single-ended loop filter is shown).

### 5.4.1 Methodology

Due to the complexity of the system and the involvement of both analog and digital circuit, a top-down mixed-signal circuit design methodology is adopted. The design tools used in this work are CADENCE and MATLAB.

Firstly, the entire ΔΣM is constructed in the schematic level by substituting the OTAs and quantizer with their ideal analog behavioral models and NS-PDWA with its behavioral model in Verilog HDL, respectively. The specifications of these models are based on the predictions from previous MATLAB simulation. The switches and capacitors are in the transistor level. The ΔΣM is then simulated by "SpectreVerilog", a mixed-signal simulator from CADENCE. The output data is captured and further processed by FFT analysis in MATLAB. This exercise verifies the topology of the ΔΣM and the structure of the loop filter, as well as the rough performance of the ΔΣM. This ΔΣM is also used as a test platform for the subsequent verifications described below.

The second step is to realize each individual block to the transistor or gate level. Whenever a block is completed at either schematic- or layout-level, it replaces its behavioral model in the above mentioned ΔΣM test platform and is re-simulated to ensure the correct functionality and specifications of the ΔΣM. In this way, the simulation time can be greatly shortened. In the mixed-signal simulation, the interface properties between analog and digital circuit, such as the rising time, falling time, and high/low threshold, are set manually according to the values extracted from transistor-level simulation using SPECTRE.

When all the sub-blocks are replaced by their respective transistor level circuits, the entire ΔΣM takes too long to get enough output data points for the FFT analysis.

Our approach is to first make sure that the post-layout timing of digital NS-PDWA block meet the specifications and then replace the digital block with its behavioral model in the overall ΔΣM simulation. The analog sub-blocks are in transistor level. In doing so, the simulation time is manageable. Figure 79 shows the block diagram of the top-down design methodology of the ΔΣM.

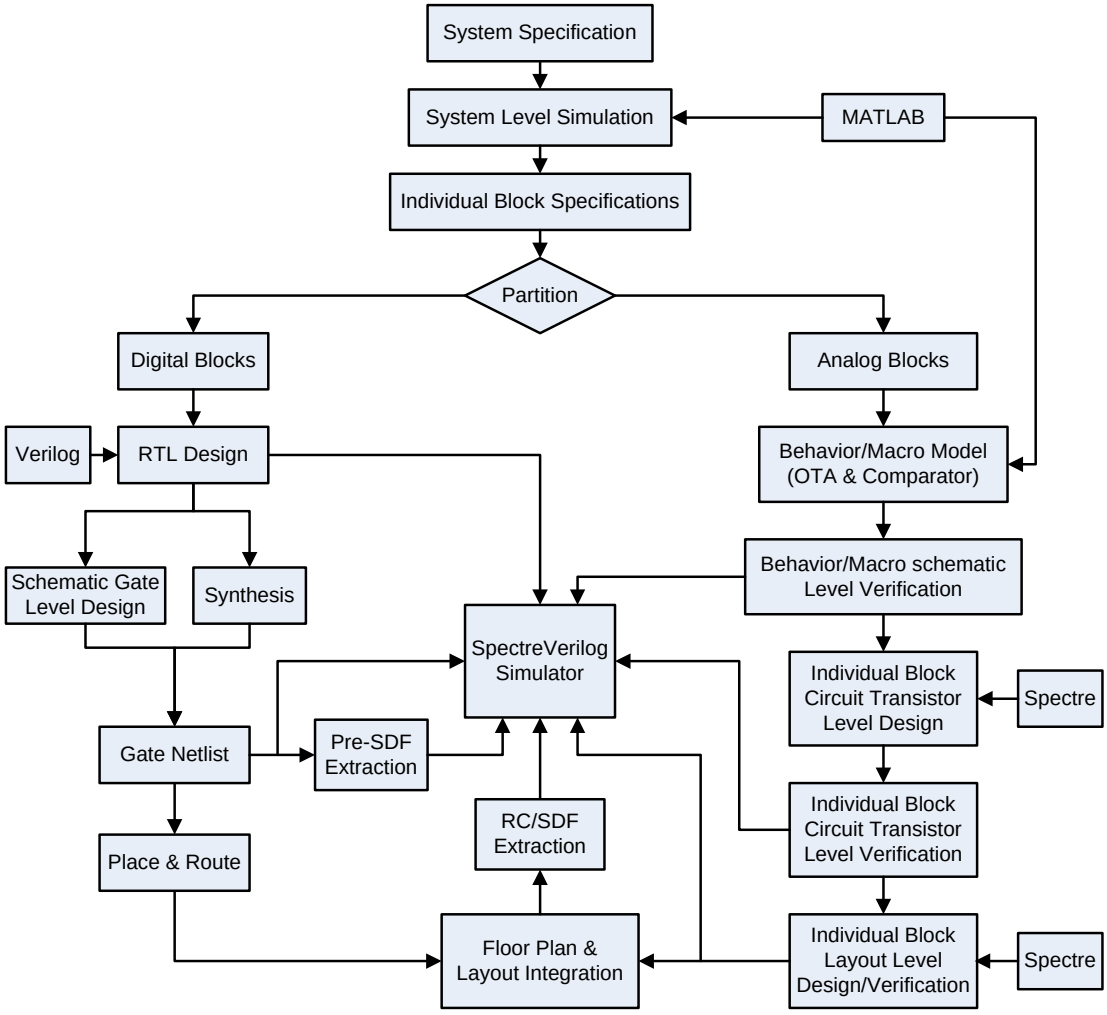


Figure 79. Block diagram of the top-down design methodology

## 5.4.2 NS-PDWA

As shown in Figure 78, NS-PDWA consists of PDWA, accumulator and differentiator. These three blocks are designed as follows, with the mismatch between the accumulator and differentiator discussed as well.

#### 5.4.2.1 Accumulator

The 4-b accumulator is implemented by a DFF register and a thermalmeter-code adder. Since the 4-b DAC is controlled by a thermalmeter-code and the output of the quantizer is also thermalmeter-code, the thermalmeter-code accumulator is therefore designed to avoid the conversions between the thermalmeter- and binary-code. Since the differential architecture is used throughout the entire ΔΣM and the quantizer has a signed output, a signed adder is used to perform addition and subtraction.

The 16-b thermalmeter coded flash quantizer's output is fed into the shifter based accumulator as shown in Figure 78. Figure 80 shows the complete block diagram of the shifter based accumulator. The proposed thermalmeter-coder adder is realized by a barrel shifter, control logic, and a DFF register. The control logic consists of the word wrap logic and 1-of-N converter modules.

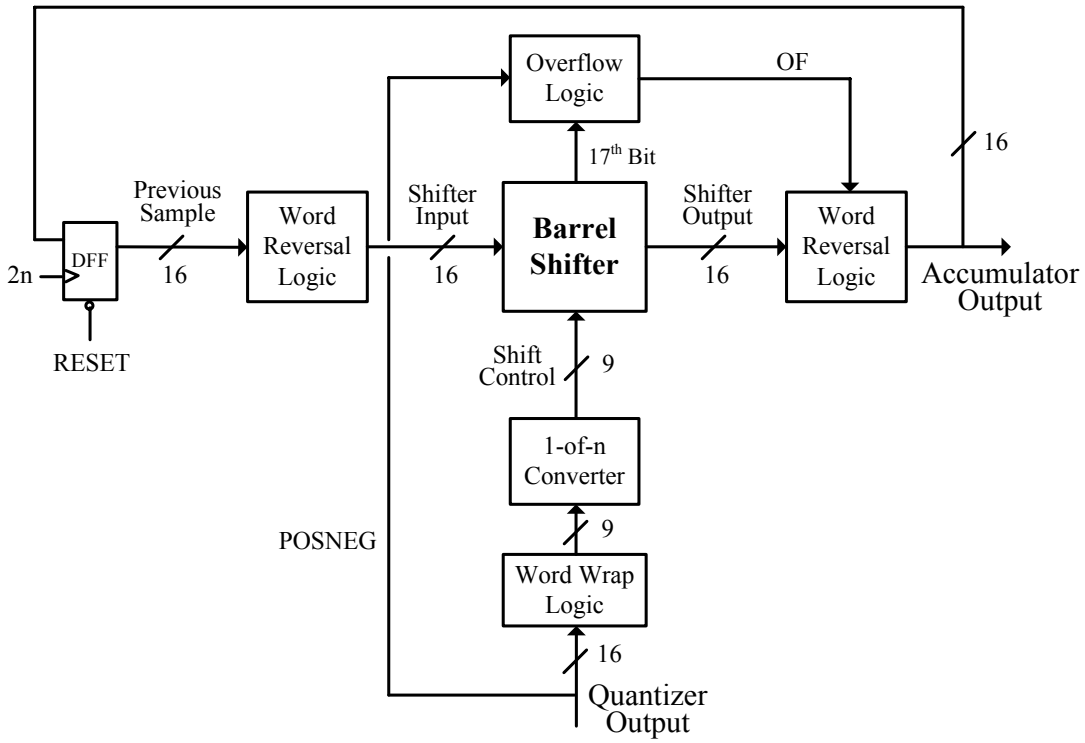


Figure 80. Block diagram of the shifter based accumulator

In the thermalmeter code domain, adding or subtracting involves a left or right

shift operation of the data word respectively. If "2" is to be added to or subtracted from the previous data registered, this registered data will be left or right shifted by two positions and the positions left will be filled by two "1s" or "0s" respectively.

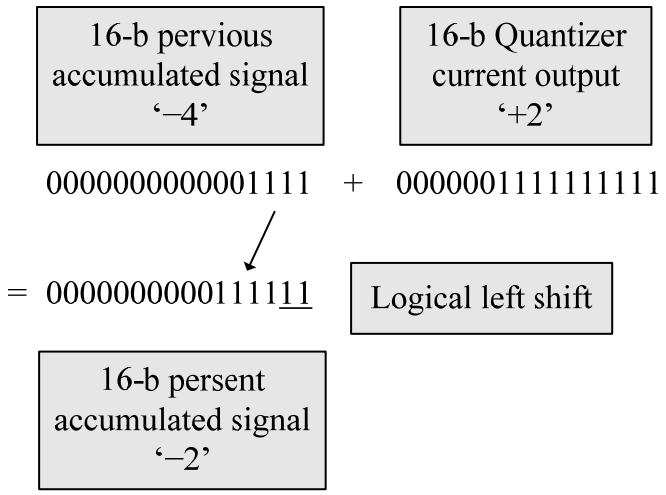


Figure 81. Example of an addition operation

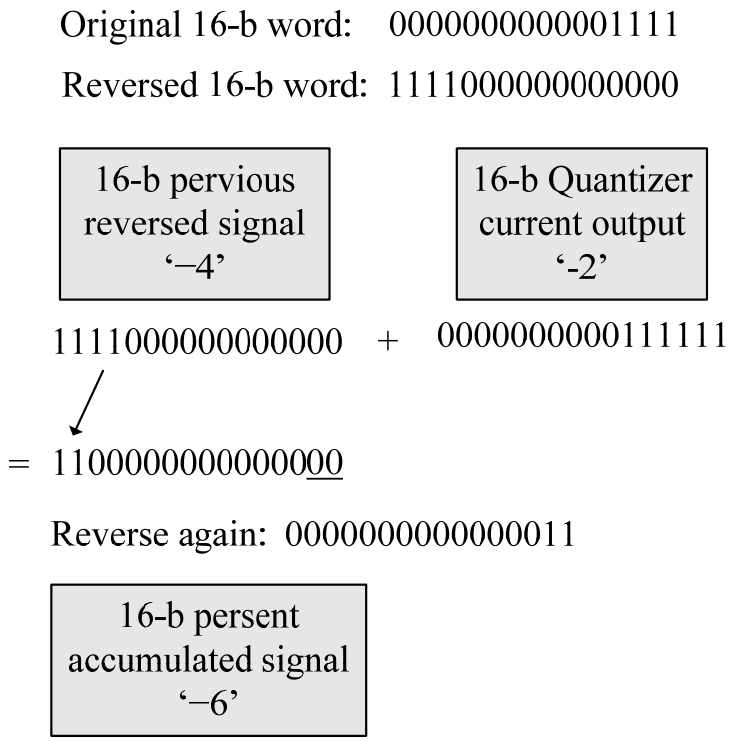


Figure 82. Example of a subtraction operation

For the addition operation, the 16-b PREVIOUS SAMPLE is left-shifted by the value determined by the 16-b input control signal (QUANTIZER OUTPUT). In the example shown in Figure 81, the operation includes shifting in '1's at the least significant bits (LSB).

For the subtraction operation, PREVIOUS SAMPLE is first reversed and a left shift is carried out. The word is then reversed back. The entire operation in Figure 82 is equivalent to right-shifting the 16-b word by 2-bits. Although this method is involves 2 extra steps, functionally only a left-shift operation would need to be implemented in hardware, and subtraction involves shifting in '0's at the LSBs.

Table 5 shows the complete truth table of shifter control logic of the accumulator. The shifter control logic takes in 16-b thermalmeter code from the quantizer and converts it to 9-b 1-of-N code SHIFT CONTROL (2nd and 4th column respectively in Table 5) for the barrel shifter.

Table 5. Truth Table of Shifter Control Logic

| **Addition Value** | **QUANTIZER OUTPUT** | **WORDWRAP OUTPUT** | **SHIFT CONTROL** | **Shift Value** |
|---|---|---|---|---|
| -8 | 0000000000000000 | 111111111 | 100000000 | 8 |
| -7 | 0000000000000001 | 011111111 | 010000000 | 7 |
| -6 | 0000000000000011 | 001111111 | 001000000 | 6 |
| -5 | 0000000000000111 | 000111111 | 000100000 | 5 |
| -4 | 0000000000001111 | 000011111 | 000010000 | 4 |

| | | | | |
|---|---|---|---|---|
| -3 | 0000000000011111 | 000001111 | 000001000 | 3 |
| -2 | 0000000000111111 | 000000111 | 000000100 | 2 |
| -1 | 0000000001111111 | 000000011 | 000000010 | 1 |
| 0 | 0000000011111111 | 000000001 | 000000001 | 0 |
| +1 | 0000000111111111 | 000000011 | 000000010 | 1 |
| +2 | 0000001111111111 | 000000111 | 000000100 | 2 |
| +3 | 0000011111111111 | 000001111 | 000001000 | 3 |
| +4 | 0000111111111111 | 000011111 | 000010000 | 4 |
| +5 | 0001111111111111 | 000111111 | 000100000 | 5 |
| +6 | 0011111111111111 | 001111111 | 001000000 | 6 |
| +7 | 0111111111111111 | 011111111 | 010000000 | 7 |
| +8 | 1111111111111111 | 111111111 | 100000000 | 8 |

It was noted that the digital accumulator can overflow in both directions – positive overflow may occur at an addition operation and negative overflow at a subtraction operation. Therefore, an overflow detection and reset circuitry is used. When a positive overflow occurs during addition, a '1' value will shift out to the 'overflow bit' ($17^{th}$ BIT in Figure 80), which is the bit immediately after the most significant bit (MSB) of the word being shifted. When a negative overflow occurs

during subtraction, it is a '0' value that will be shifted to the 17th BIT in the barrel shifter. If there is no overflow, 17th BIT will be '0' and '1' for addition and subtraction respectively after shifting. When the thermalmeter code adder overflows, OF will be '1' and the QUANTIZER OUTPUT will pass straight through to the output.

The advantage of using a barrel shifter is that ideally the 16-b signal has to pass through at most one transmission gate when shifted. Hence, the propagation delay is independent of shifter value or shifter size. Another benefit is that the shifter control signal is in 1-of-N code, and can be converted from thermalmeter code without incurring much delay.

#### 5.4.2.2 PDWA

As shown in Figure 78, PDWA splits the DAC into two identical parts with each employing the conventional DWA algorithm. Each DWA is realized by a barrel shifter and a pointer selection logic block. The one of the DWA implementation is shown in Figure 83. The pointer, registered in DFF, is delayed for one clock and ready for the next data cycle. This pointer always points to the first unused unit element. The pointer selection logic implementation for DWA is shown in Figure 84.

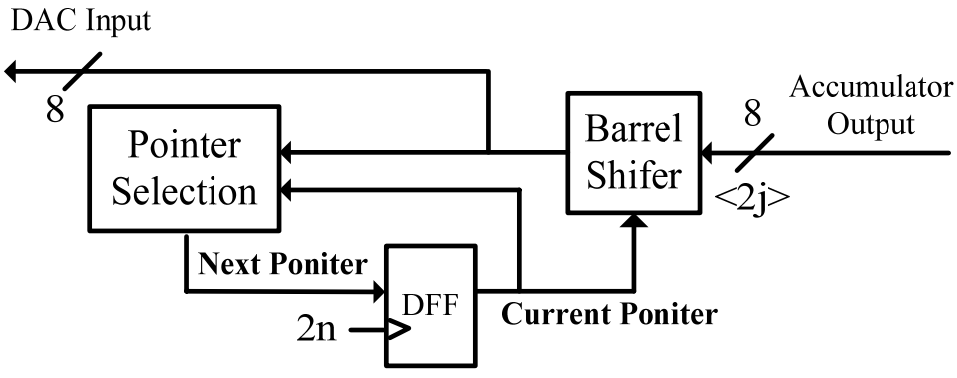


Figure 83. Block diagram of the DWA implementation

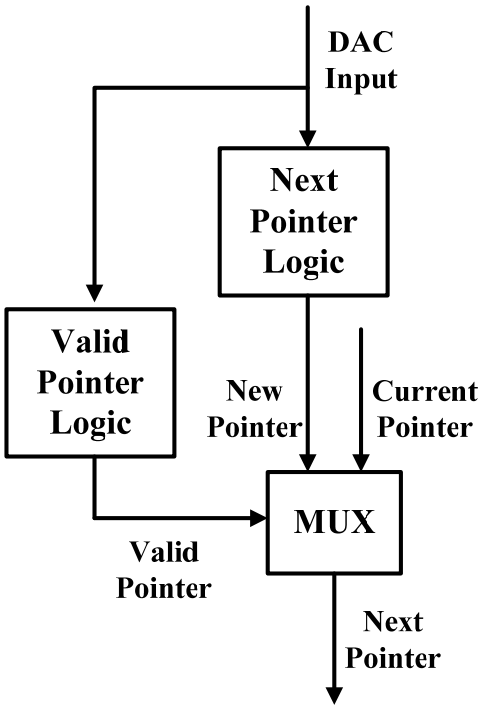


Figure 84. Block diagram of the pointer selection logic implementation for DWA

Table 6. The function of the next pointer logic

| | |
|---|---|
| DAC INPUT: | (MSB) 1 1 0 0 0 0 1 1 (LSB) |
| Next POINTER: | 0 0 0 0 0 1 0 0 |
| DAC INPUT: | 1 1 1 1 1 1 0 0 |
| Next POINTER: | 0 0 0 0 0 0 0 1 |

Table 6 demonstrates the function of the next pointer logic for the DWA algorithm. The next pointer can be identified by picking out "1-0" transitions in the rotated word (DAC Input), as shown in Table 6. The output of the next pointer logic can be expressed as

$$NextPTR = \overline{HigherBit} \bullet LowerBit = \overline{HigherBit \oplus \overline{LowerBit}} \quad (32)$$

There are two permutations of the DAC INPUT for which the next pointer logic fails to evaluate NEXT POINTER – when all the bits of the input word are '0's or when all are '1's. In such cases, NEXT POINTER should have the same value as CURRENT POINTER – the pointer does not shift in that time sample. The valid pointer logic evaluates whether DAC INPUT is either one of these 2 permutations. VALID POINTER is an internal flag which signals the validity of NEW POINTER (evaluated by next pointer logic).

The DAC unit elements are selected in rotation. Thus all the elements can be used at the maximum possible rate and each element is used by the same number of times. This ensures that the errors introduced by the DAC quickly average to zero. PDWA algorithm reduces the in-band tones that are generated by the DWA, but the noise floor of DAC is increased in the signal band and SNR is sacrificed. With NS-PDWA, the loss of SNR due to the increased in-band noise floor in PDWA can be partially recovered by the first-order noise shaping.

#### 5.4.2.3 Differentiator

The differentiator is incorporated into the DAC and the first stage of the filter without incurring any analog extra circuitry. For the sake of simplicity, only one side of the differential circuit is shown in Figure 85. The 4-b thermalmeter-coded DAC is implemented by 16 $C_{du}$ and 32 switches controlled by $D_1$ to $D_{16}$ with external references. The input signal is sampled on the input capacitor array, $C_{su}$, while the output of the DAC is held on the DAC capacitor array, $C_{du}$.

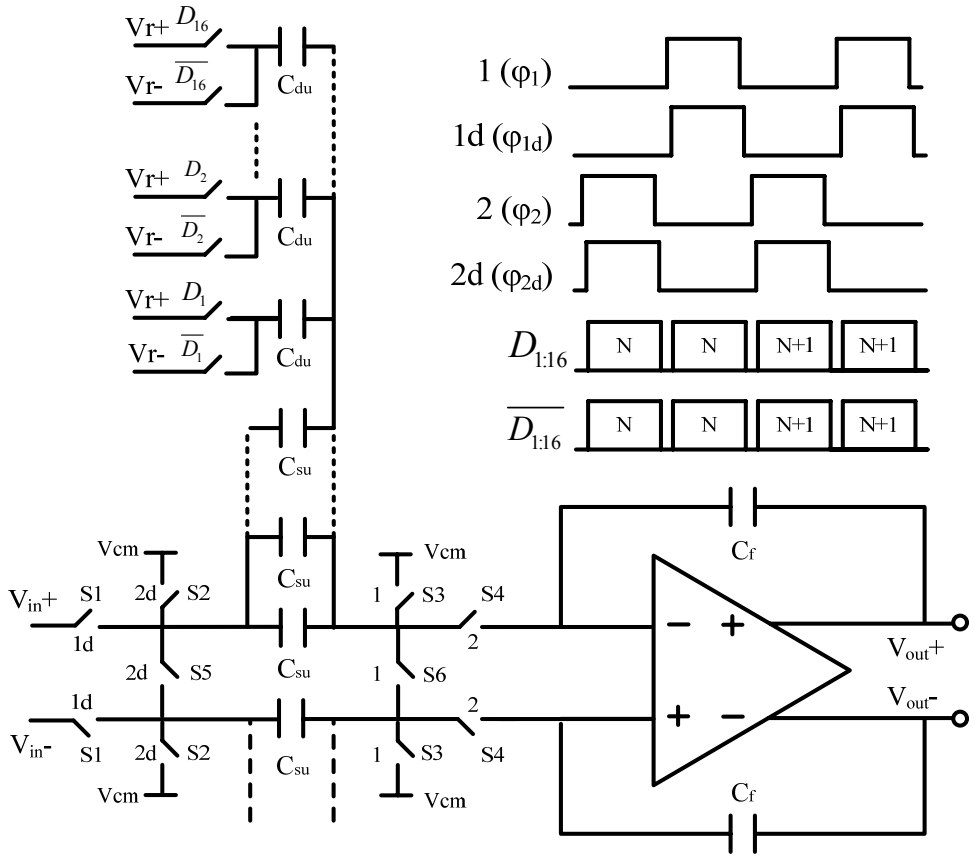


Figure 85. The 1st stage of filter and the differentiator (only single end is shown)

When $\phi 1=1$, $\phi 2=0$, $D_{1:16}=D(N)$, the charge on the input and DAC capacitors are

$$Q_{in} = 16 \cdot C_{su} V_{in}, \tag{33}$$

$$Q_{DAC} = 2 \cdot D(N) C_{du} V_r, \tag{34}$$

where $V_{in}=V_{in+} - V_{in-}$, $V_r=V_{r+} - V_{r-}$, $-8 \le D(N) \le 8$ is the 4-b DAC input at time N. In the sampling phase when $\varphi_1$ is high shown in Figure 86, the output of the DAC, namely $Q_{DAC}$, is held on the DAC capacitor array ($C_{du}$) and the input signal is sampled on the input capacitor array ($C_{su}$).

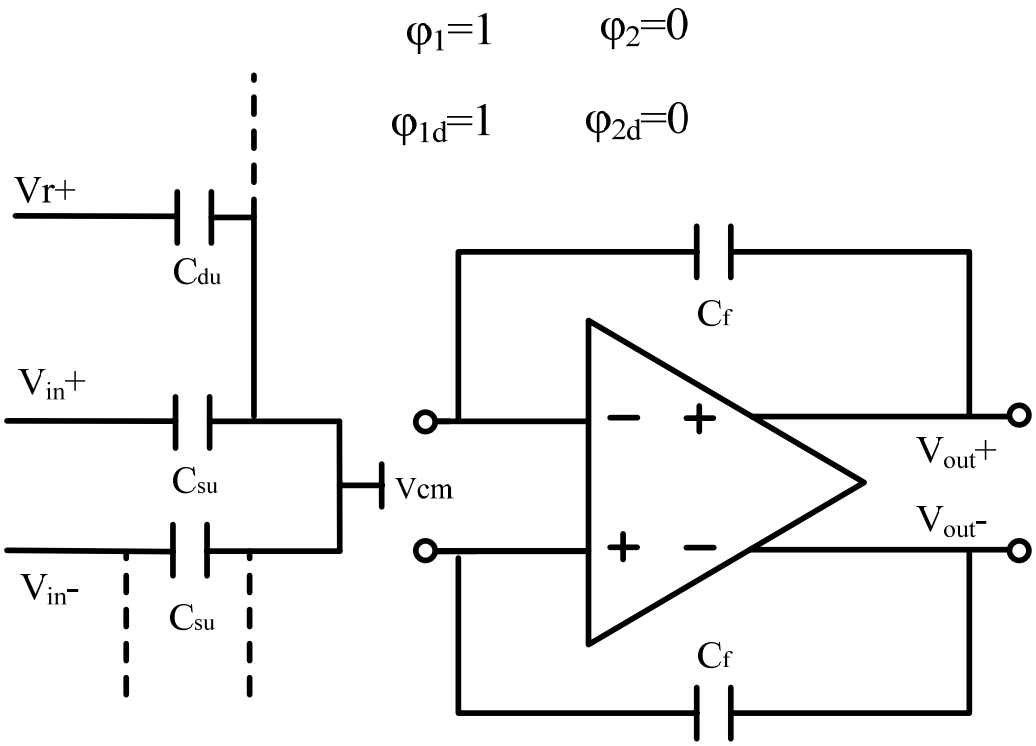


Figure 86. The 1st stage of filter and the differentiator in the sampling phase.

When $\phi 1=0$, $\phi 2=1$, $D_{1:16}=D(N+1)$, the charge on the input and DAC capacitor becomes

$$Q_{in} = 0, \tag{35}$$

$$Q_{DAC} = 2 \cdot D(N+1) C_{du} V_r, \tag{36}$$

where $-8 \le D(N+1) \le 8$ is the 4-b DAC input at time N+1.

During the integrating phase ($\varphi_2$ is high) shown in Figure 87, the new DAC output automatically subtracts the previous output. In other words, only the charge difference between the present and previous output on the DAC capacitor array ($C_{du}$) is transferred to the integrating capacitor, $C_f$.

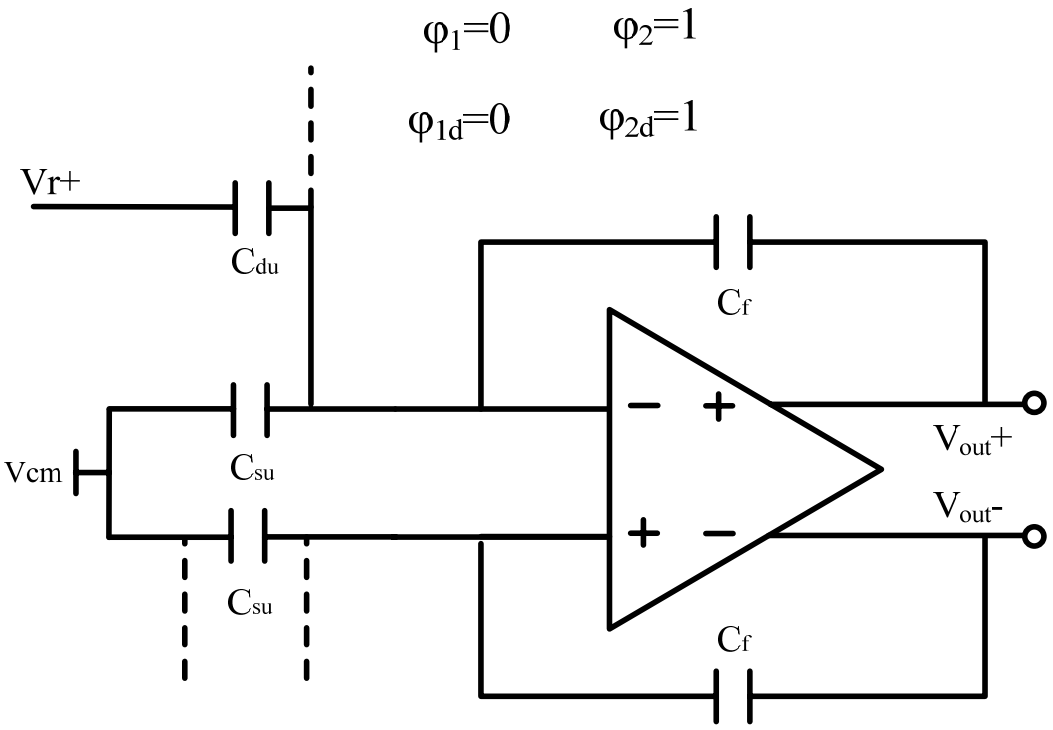


Figure 87. The 1st stage of filter and the differentiator in the sampling phase.

The quantitative analysis is as follows. The charge conservation requires

$$\Delta Q_{C_f} = \Delta Q_{in} + \Delta Q_{DAC}. \tag{37}$$

Therefore, the ideal variation of the differential integrator output Vout, at the end of the $\phi 2$ at time N+1, is given by

$$V_{out}(N+1) - V_{out}(N) = \frac{16 \cdot C_{su} V_{in} + 2 \cdot [D(N+1) - D(N)] \cdot C_{du} V_r}{C_f}. \tag{38}$$

The noise shaping or differentiation is realized as Eq (38) shows. The DAC output at time (N+1), $2 \cdot D(N+1) C_{du} V_r$, is substrated by the previous one, $2 \cdot D(N) C_{du} V_r$ at the end of the $\phi 2$ at time (N+1). Thus, the DAC output differentiation operation is realized. The nonlinearity of the DAC occurs when the reference in the DAC is sampled onto the capacitors that are mismatched, that is, during $\phi 1$ and $\phi 2$. The differentiation only happens in the following process, that is, during $\phi 2$. In fact, the mismatch is already

randomized by the DEM at the input of the DAC.

And, the *kT/C* noise from the switches and the thermal noise from the references are also sampled on the DAC capacitor. Therefore the thermal noise is differentiated during the above operation and shaped out of the signal band, so the proposed NS-DEM has the added benefit of DAC inherent thermal noise shaping.

### 5.4.3 Loop Filter

The key design issues in the loop filter are the OTA gain, namely the settling of the switched-capacitor circuit and the input-referred noise that has great impact on the performance of the ΔΣM. The OTA gain is determined by a behavioral simulation, which indicates that the OTA dc gain should be higher than 40dB to ensure the SNR of the ΔΣM above 86dB, as shown in Figure 88. Although the requirement for the OTA dc gain is not so stringent in terms of SNDR, the input-referred noise and tones generated by the 1$^{st}$ OTA should be well below the noise floor of the ΔΣM in order to meet the SNR and SFDR requirements. In this design, a conventional telescopic OTA shown in Figure 89 is employed with switched-capacitor common-mode feed back (CMFB) circuit. This highly efficient telescopic OTA is used for the first five stages of the loop filter to minimize the current consumption while achieving high speed. The dc gain of the OTA in the first stage is about 67dB. The internal node swing of the loop filter is relative small and suitable for the telescopic OTA. To restore the signal level at the input of quantizer, a folded cascade OTA with large output swing is used in the last stage.

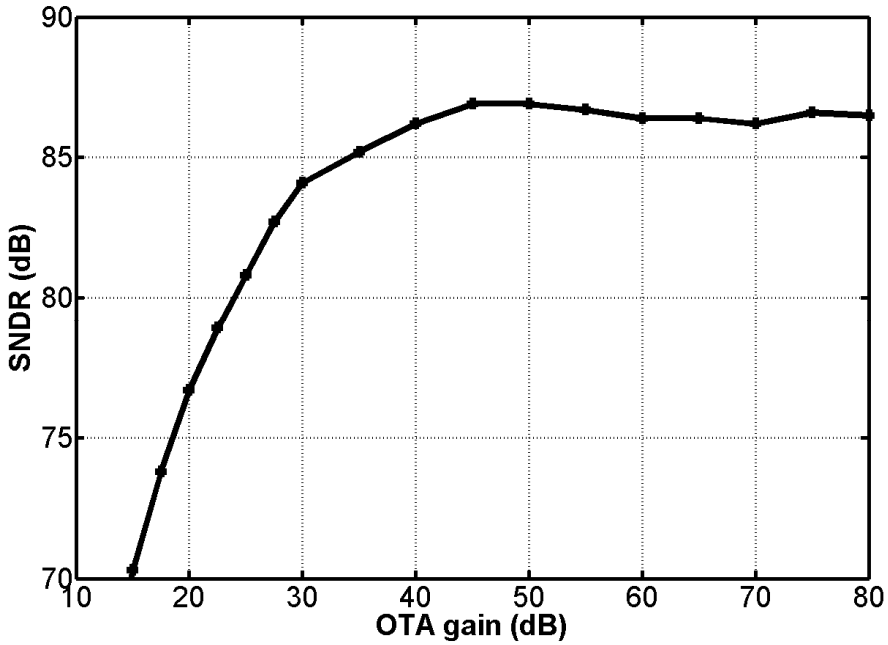


Figure 88. SNDR versus OTA dc gain

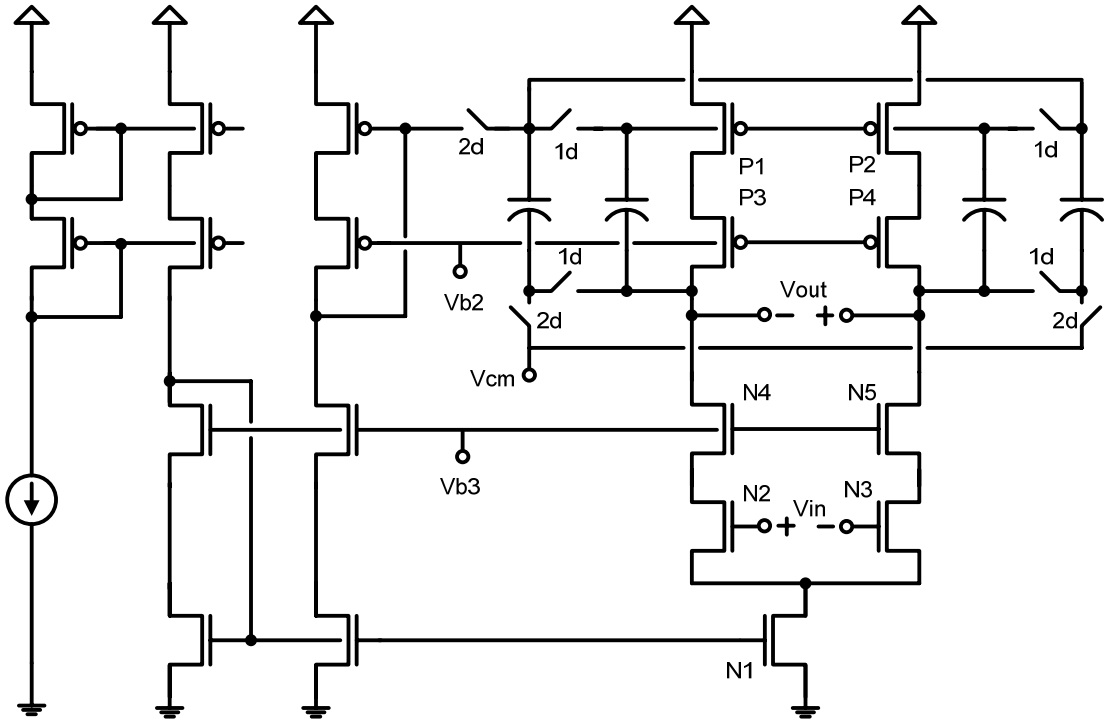


Figure 89. Employed telescopic OTA with switched-capacitor CMFB circuit

## 5.4.4 Front-End Integrator Design

The front-end integrator is the most critical part of the ΔΣM. The noise issue is

characterized as follows. The input-referred noise at the front-end of the ΔΣM mainly consists of the *kT/C* noise from the switches, the quantization noise of the ΔΣM, the transistor noise of the first OTA, and the thermal noise of the DAC voltage reference. Since the full scale of the input signal (differential) is 5V and the ΔΣM is stable for the input signal up to -3dB of the $V_{FS}$, the full scale signal power is

$$P_s = \frac{(\frac{5}{2} \cdot 10^{-3/20})^2}{2} = 1.566\ (V^2) \tag{39}$$

In order to achieve 80dB SNR performance, the total noise should be

$$P_n = P_s \cdot 10^{-80/10} = 1.566 \times 10^{-8}\ (V^2) \tag{40}$$

In line with the behavior simulation result, the quantization noise power of the ΔΣM is -90dB lower than the full scale single power.

$$P_{Quan} = P_s \cdot 10^{-90/10} = 1.566 \times 10^{-9}\ (V^2) \tag{41}$$

Figure 90 shows the input-referred transistor noise ($V/\sqrt{Hz}$) of the first OTA by the CADENCE Spectre simulation result. Figure 90 also shows that the flicker noise corner frequency is about 1MHz. The flicker noise dominates the transistor noise contribution in the signal BW, and the integrate the noise in Figure 90 over the frequency band. The total the input-referred transistor noise of the first OTA from 100Hz to 2.2MHz (the signal band for ADSL2+) is 14 μV as shown in Figure 91. The noise aliasing effect due to the sampling is not considered here because the flicker noise dominates the transistor noise. Thus the input-referred transistor noise power of the first OTA is roughly

$$P_{transistor} = \int_{f=100Hz}^{2.2MHz} V_{transistor\_noise}^2 df = (14\mu V)^2 \approx 0.02 \times 10^{-8}\ (V^2) \tag{42}$$

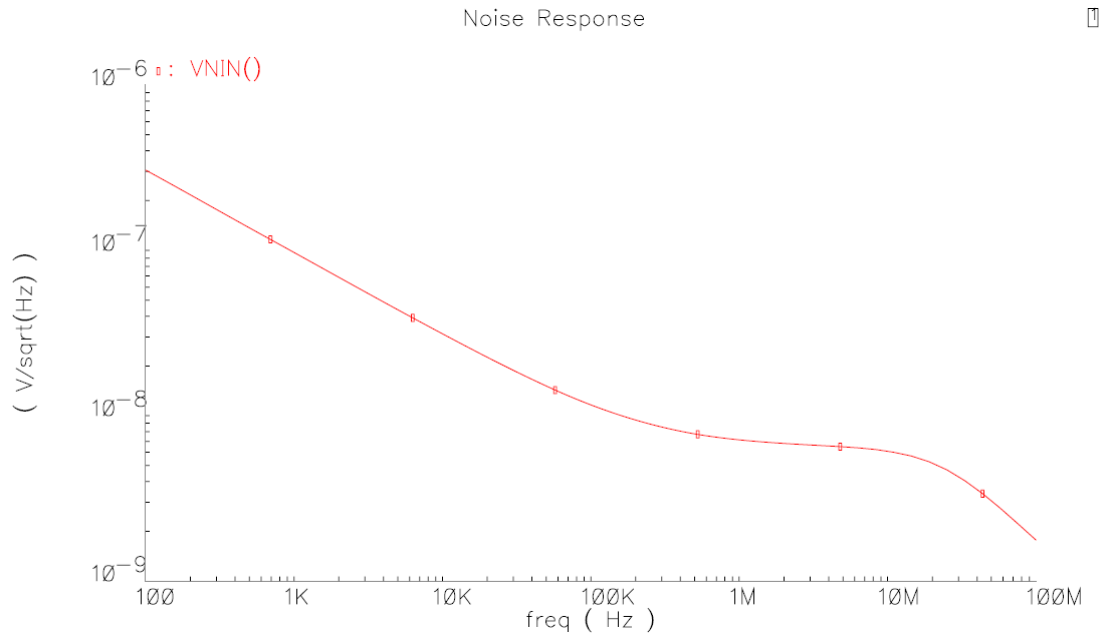


Figure 90. Input-referred transistor noise of the first OTA

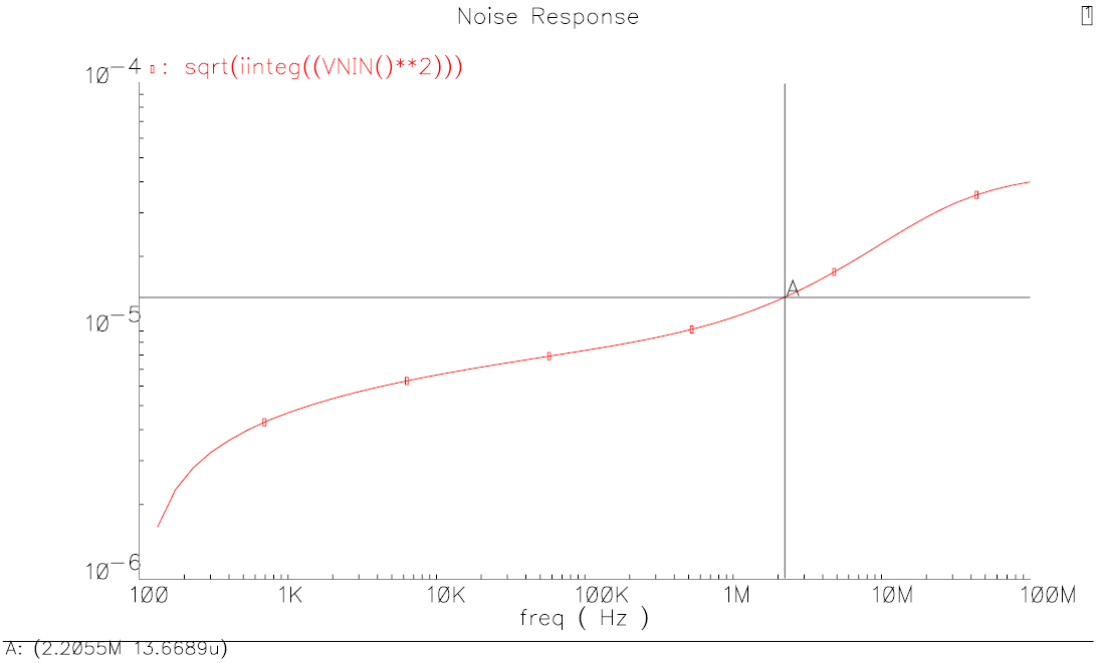


Figure 91. Integration of the input-referred transistor noise of the first OTA over the frequency band.

The *kT/C* noise from the switches is estimated as follows. Because the switch noise from DAC can be shaped out of the signal band as argued in the pervious chapter, only the noise from the switch for the input signal sampling will be discussed in the

following sections. Thus, the total input-referred *kT/C* noise power at the input of the first OTA is [10]

$$P_{kT\_in\_ref} = \frac{4kT}{16C_{su}} \tag{43}$$

where $k = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant and T is the absolute temperature.

The DAC mismatch noise and the thermal noise from the DAC voltage reference are also shaped out of the signal band by NS-DEM. The $C_{su}$ is calculated as follows.

$$\begin{aligned} P_n &= P_{Quan} + P_{transistor} + P_{kT\_in\_ref} \\ &= 1.566 \times 10^{-9} + 0.02 \times 10^{-8} + \frac{4kT}{16C_{su}} \\ &= 1.566 \times 10^{-8} \end{aligned} \tag{44}$$

By solving the above equation, $C_{su} = 63\ fF$. Thus, the total input capacitor $C_{in} = 16C_{su} \approx$ 1pF and the feedback capacitor $C_f = 1$ pF. Also the DAC capacitor $C_{du} = 63\ fF$.

### 5.4.5 Capacitor Matching Requirement

The DAC capacitors $C_{du}$ are random values whose standard formulation is

$$\sigma = \frac{A_C}{\sqrt{WL}} \tag{45}$$

where Ac is the process dependant matching parameter, W and L are the nominal width and length of the capacitor respectively.

To simulate the influence of the capacitor mismatch on the performance of the ΔΣM, the DAC capacitor values are given in a normal distribution with given σ. In the chosen CMOS process, the poly capacitor, $C_{du} = 63\ fF$, has $\sigma = 0.00118$. The simulation in Matlab shows that the peak SNR and SFDR are about 76dB and 90dB with such capacitor mismatch if without any DEM. The peak SNR and SFDR would be about 81dB and 110dB with PDWA in operation.

### 5.4.6 OTA Speed Requirement

The OTA is working in two different configurations, the sampling and integrating phases. The most critical phase is the integrating phase in terms of speed, $\phi1 = 0$ and $\phi2 = 1$ shown in Figure 87. In the integrating phase, $C_{su}$ connects the input of the OTA and increases the effective load of the OTA. The stringent settling requirement of the OTA should meet that the settling error $e_{settle}$, the ratio of which to the output step response $V_o^{\infty}$, should less than half LSB of the ΔΣM,

$$\frac{e_{settle}}{V_o^{\infty}} < \frac{2^{-n}}{2} \tag{46}$$

where n is the number of bit of the ΔΣM's resolution. The step response of the integrator goes into the slewing mode at first. After a while, the OTA operates in the settling modes. Assuming 1st order settling behavior of the OTA, the output of the OTA behaves in an exponential waveform with a time constant $\tau_{settle}$.

$$\tau_{settle} < \frac{C_{effective\_load}}{g_m} \tag{47}$$

where $g_m$ is the transconductance of the input transistor of the OTA and [69]

$$C_{effective\_load} = (C_s + C_g) + C_o + \frac{C_o(C_s + C_g)}{C_f} + g_m R_{sw} C_s \tag{48}$$

$C_s = 16(C_{su} + C_{du})$, $C_g$ is the parasitic capacitance at the input transistor's gate in which $C_{gs}$ is dominant; $C_o$ is capacitive load at the output of the OTA; $C_f$ is the feedback capacitor and $R_{sw}$ is the switch resistance. If not considering the slewing of the OTA, the settling error $e_{settle}$ is also given by

$$e_{settle} = V_o^{\infty} e^{-\frac{T_{settle}}{\tau_{settle}}} \tag{49}$$

where $T_{settle}$ is the duration time of the integration. Given the parameters n, $C_s$, $C_g$, $C_o$, $C_f$, $R_{sw}$, and $T_{settle}$, one can roughly estimate the $g_m$ of the input transistor through the above equations to meet the required resolution.

The non-zero switch resistance impairs the settling speed, according to Eq (47) and (48). To reduce the switch resistance, the aspect ratio of the MOS transistor has to be increased and the minimal length of the transistor is employed. However, the clock feedthrough, charge injection, and the parasitic capacitance increase with the size of the switch and may degrade the ΔΣM's performance. To reduce the on-resistance of the switches, two additional large switches, S5 and S6 [41] shown in Figure 85, are added to accelerate the settling of the differential signal. Switch S2 and S3 are responsible for the settling of the common mode signal, so their size can be minimized since the common mode signal varies little. Compared with the design in which switches S2 and S3 have large aspect ratio and settle both common-mode and differential signals, the use of S5 and S6 allows the equivalent on resistance to be halved in the differential signal path.

The current consumption of the first OTA is 3mA. The transistor sizes of the telescopic OTA (Figure 89) are listed in Table 7.

Table 7. Transistor and Cap Size of the first telescopic OTA

| Transistor | W (μm) | L (μm) |
|---|---|---|
| N1 | 1288 | 1 |
| N2, N3 | 2560 | 0.35 |
| N4, N5 | 1280 | 0.35 |

| | | |
|---|---|---|
| P1, P2 | 1000 | 0.35 |
| P3, P4 | 1000 | 1.15 |
| Csu, Cdu | 63*f*F | |
| Cf | 1pF | |

### 5.4.7 Quantizer

The quanizer is realized by a 4-b flash ADC with 16 identical comparators and the poly resistor string reference as shown in Figure 92. The full scale differential signal is 5V. Although the non-idealities of quantizer, such as offset and hysteresis of the comparators, can be suppressed by the loop filter in the same way as it is for the quantization noise, the ΔΣM still has certain tolerance to these non-idealities. Behavioral simulation in MATLAB shows that standard deviation of the comparator input offset should be less than 10% of the LSB of the quantizer (17mV) to make SNDR degradation less than 2dB. Similar requirement is also applied to the hysteresis of the comparator. The schematic of the comparator is shown in Figure 92. The input transistors, M1 and M2, are properly sized to minimize the offset and the input parasitic capacitance. M5 and M6 are minimized to reduce the parasitic capacitance at the output node and thus speed up the regeneration speed. M9 is turned off slightly earlier than clock 2d so that the regeneration would not be affected by the charge injection and clock feedthrough from the switches at the input of the quantizer as shown in Figure 92.

Figure 93 shows the transfer characteristic of the comparator with the offset and hystereis errors. At first, a ramping signal with positive slope from low to high level

feeds into the comparator and the comparator output is reversed at $V_{in} = V_L$. Similarly, the omparator output is reversed at $V_{in} = V_H$, when the input signal ramps from high to low level. The hysteresis of the comparator is defined by $V_{hys} = V_H - V_L$. The offset of the comparator is $V_{offset} = (V_H - V_L)/2$. The Monte-Carlo simulation results demonstrate the statistical characteristic of the $V_H$ and $V_L$ in Figure 94 and Figure 95. The Monte-Carlo simulation is done in CADENCE "Spectre" and the number of samples N is 100. The average and the standard deviation of $V_H$ ($V_L$) are 0.18mV (0.12mV) and 3mV (3mV) respectively. The mean comparator offset is 0.15mV with 3mV standard deviation.

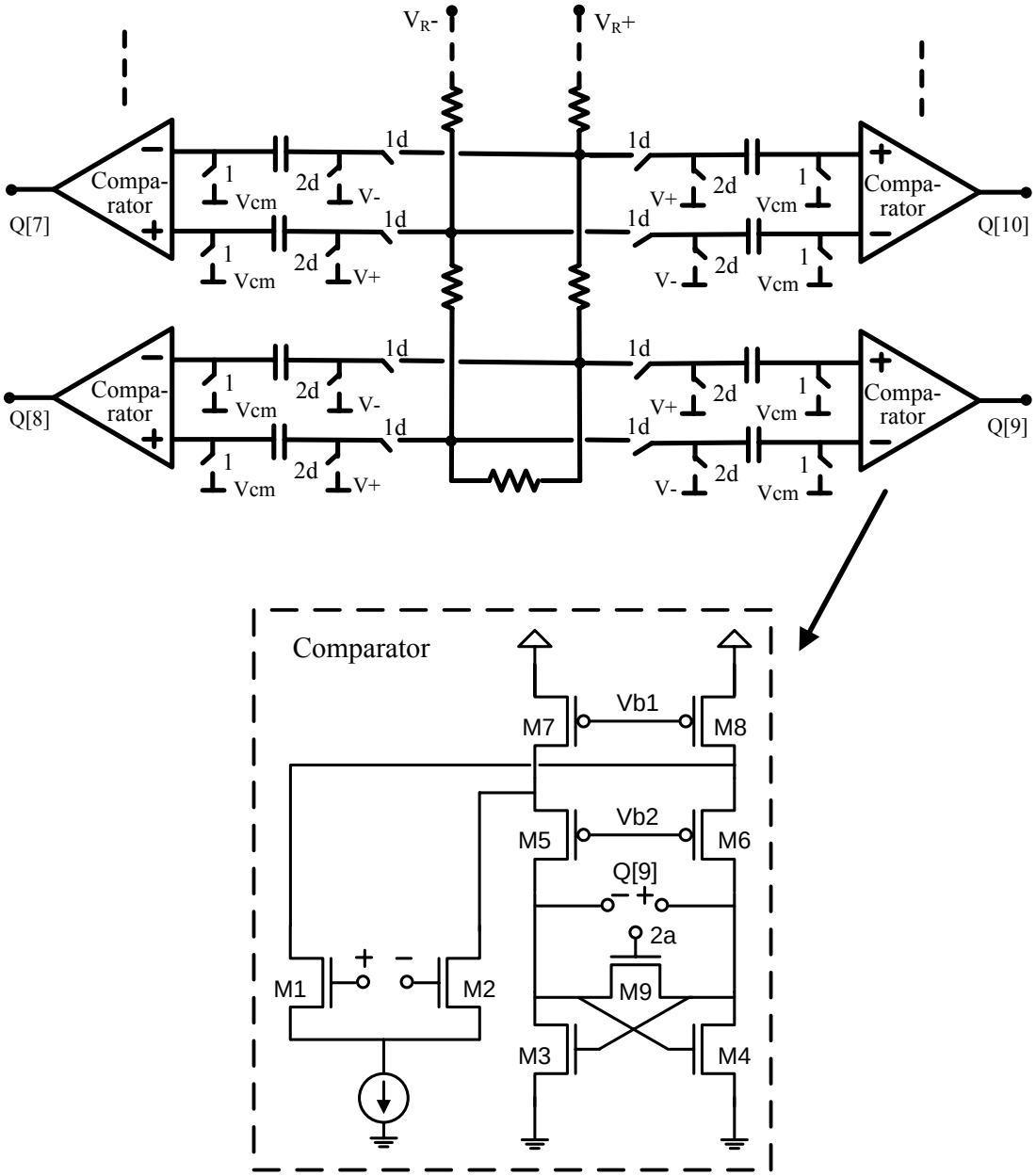


Figure 92. Quantizer schematic

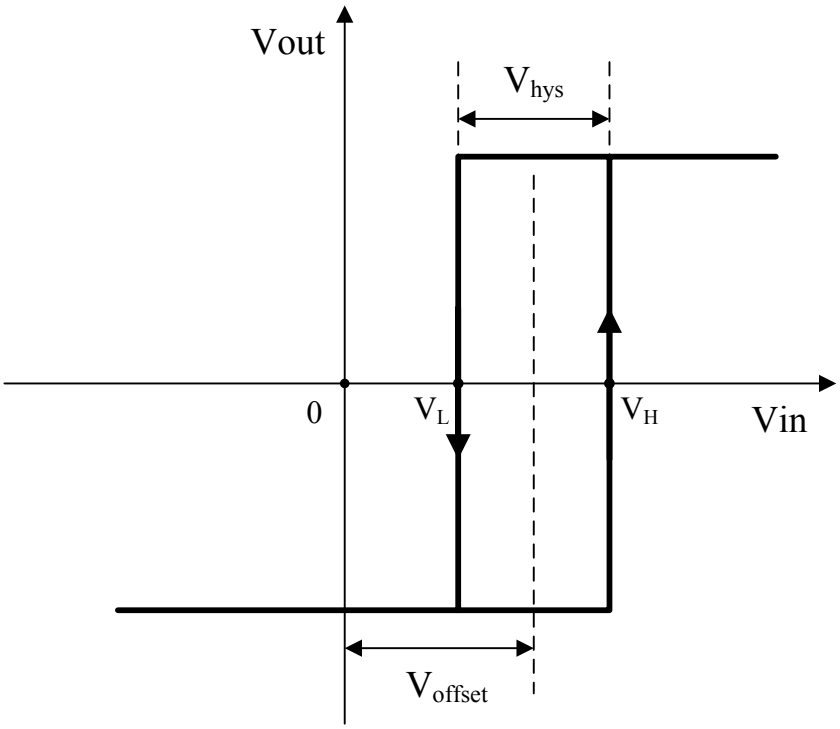


Figure 93. Transfer characteristic of the comparator with offset and hysteresis

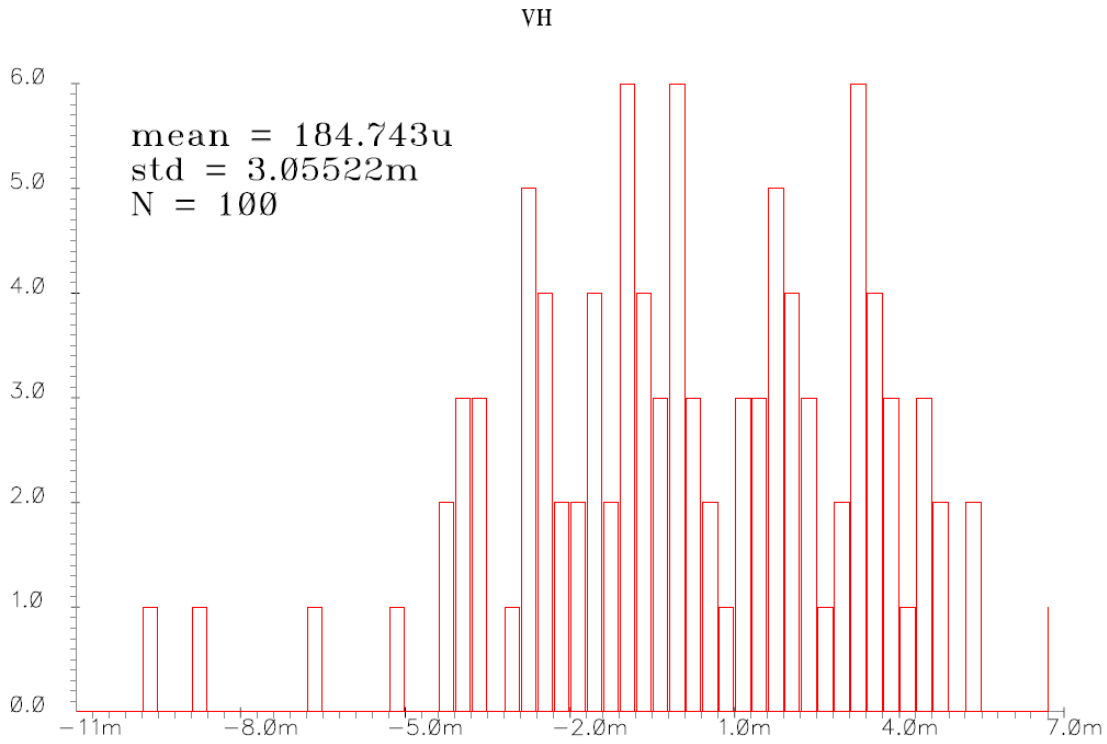


Figure 94. Monte-Carlo Simulation result of $V_H$

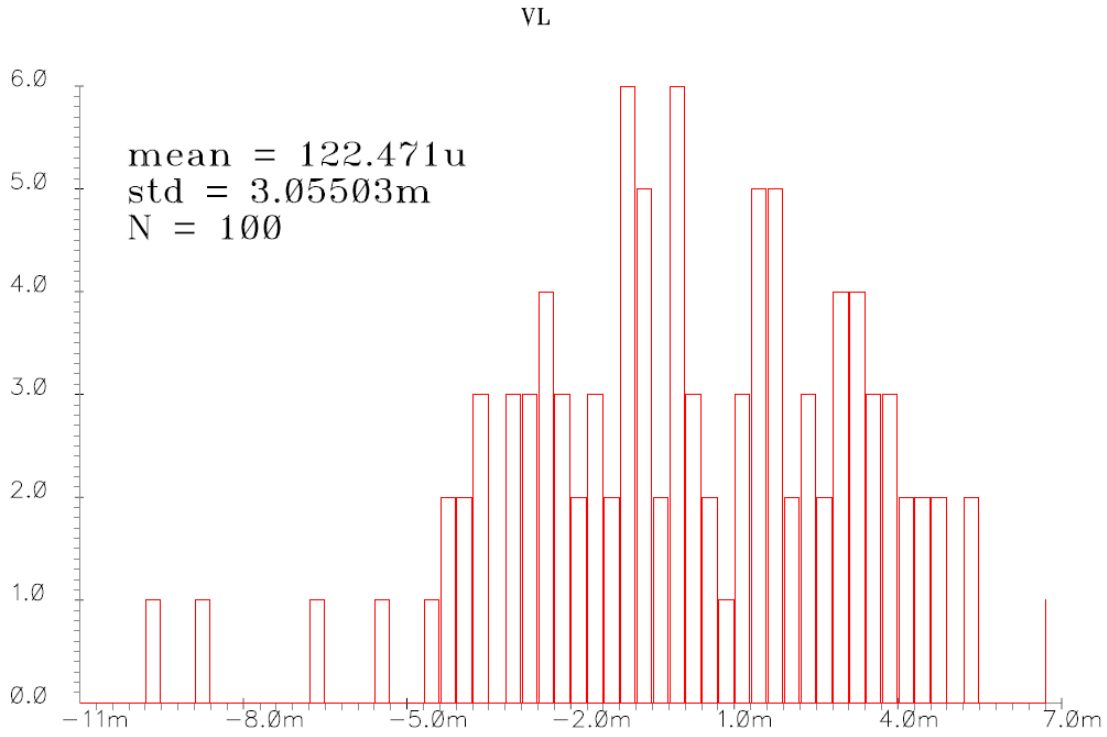


Figure 95. Monte-Carlo Simulation result of $V_L$

### 5.4.8 Schematic Simulation Result

According to the previous methodology, the entire ΔΣM is verified in CADENCE by "SpectreVerilog" simulator. The analog part is constructed on the transistor level, while the digital part is replaced by the behavioral model in the mixed-signal simulation. The transient output of the ΔΣM is captured and is further analyzed by FFT in MATLAB. Finally, the simulation result is shown in Figure 96 and Figure 97. Figure 96 shows the output spectrum of the ΔΣM with 82dB SNDR in the signal tone testing. The noise floor is limited by the quantization noise. Figure 97 shows the output spectrum of the ΔΣM in the two tones testing. There is no obvious intermediation tone in Figure 97.

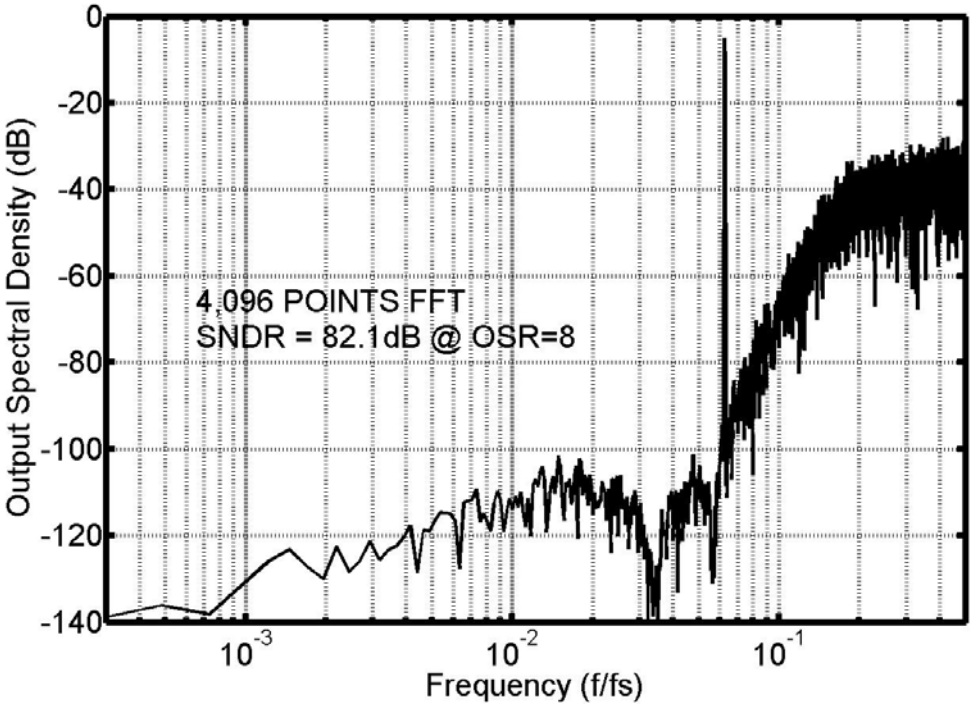


Figure 96. Output spectrums in the signal tone testing

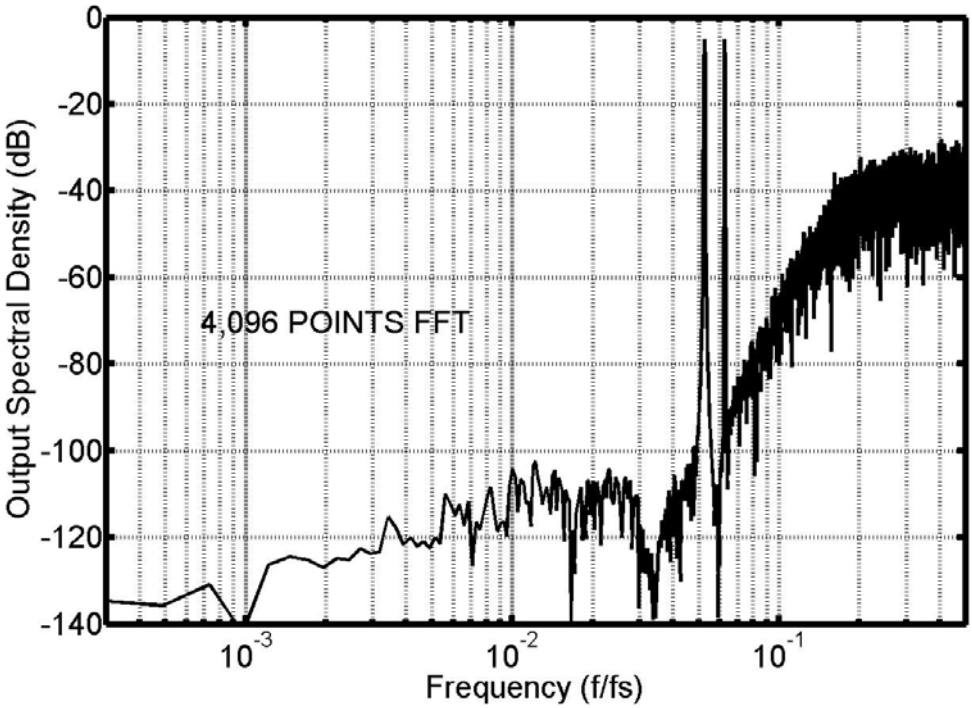


Figure 97. Output spectrums in the two tones testing

## 5.5 Experiment

This section describes the chip evaluation and presents the test results, as well as the test results.

### 5.5.1 Experiment Setting

The ΔΣM chip is fabricated in a 0.35-μm CMOS process and mounted in a ceramic CQFP 48-pin package. The test setup is given in Figure 98. An ultra low distortion function generator DS 360 is used to provide the input signal to the ΔΣM under test. The output data stream is captured by an Agilent logic analyzer 16801A and further processed by FFT analysis in MATLAB. The ΔΣM is clocked at 35.2MHz. With 8x OSR, the signal bandwidth is 2.2MHz. To make comparison between PDWA and NS-PDWA, a control signal was provided on chip. By switching on and off the control signal, the proposed noise shaping can be switched on and off accordingly.

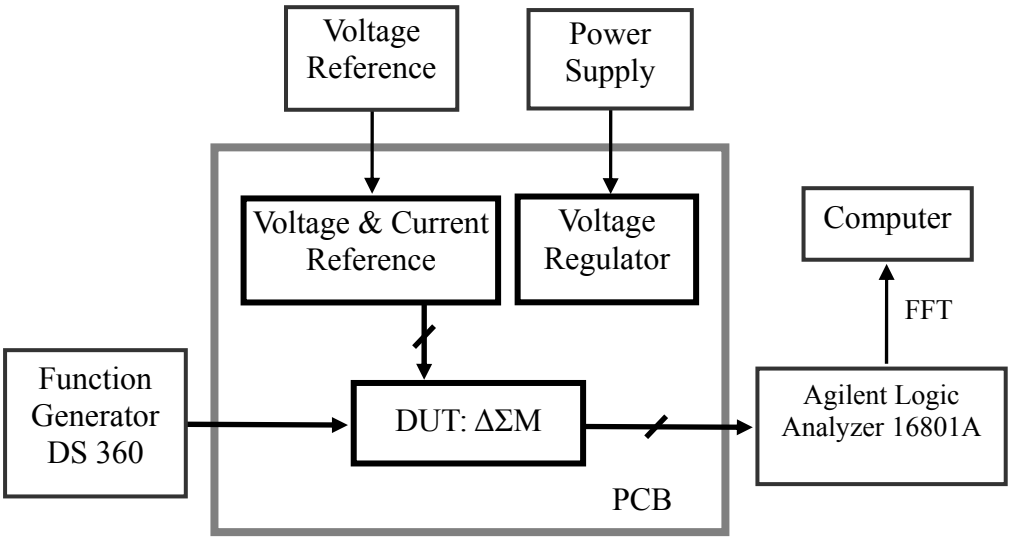


Figure 98. Testing Schematic

### 5.5.2 Experiment Result

The measurements are done with NS-PDWA on. Figure 99 shows the output spectrum with input sinusoidal signal at 189.06 kHz and -12dB below the full

reference scale ($5V_{p-p}$). The measured SFDR is 94dB and there is no obvious harmonic distortion. The DSM is also measured with NS-PDWA off. There is still no obvious harmonic and tones in the measured output spectrum. The reason is that the linearity of the DAC is higher than 94dB even without PDWA, which is also the same with that estimated in Section 5.4.5. Figure 100 shows the 65,536 points FFT plots of the output spectrum with NS-PDWA and without input signal.

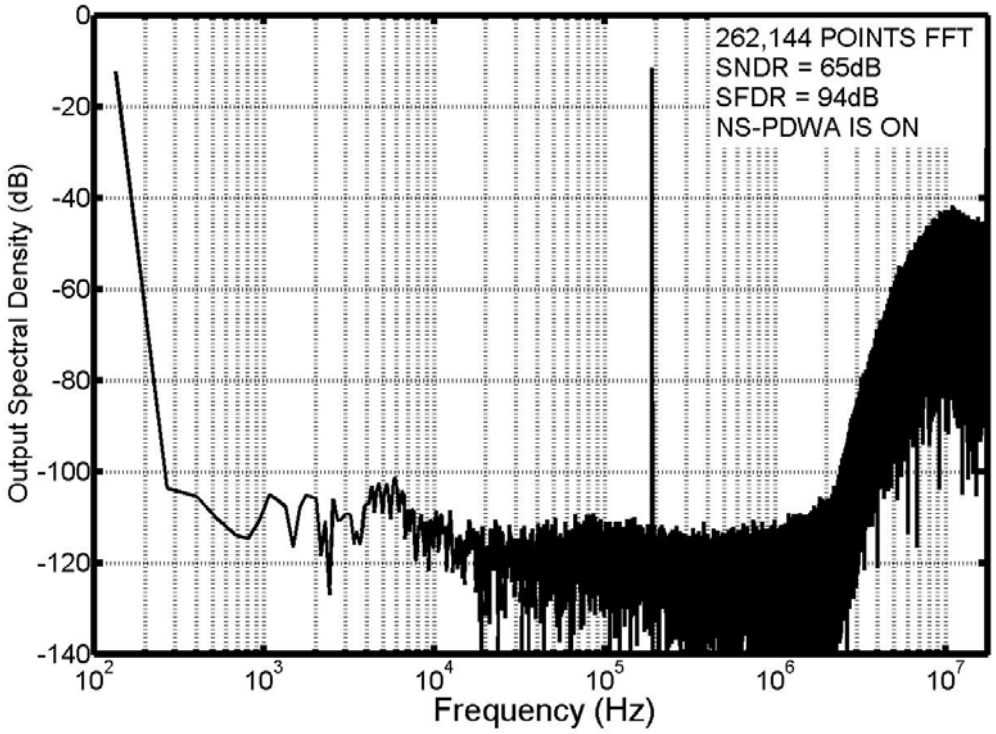


Figure 99. Measured output spectrum with NS-PDWA and input signal.

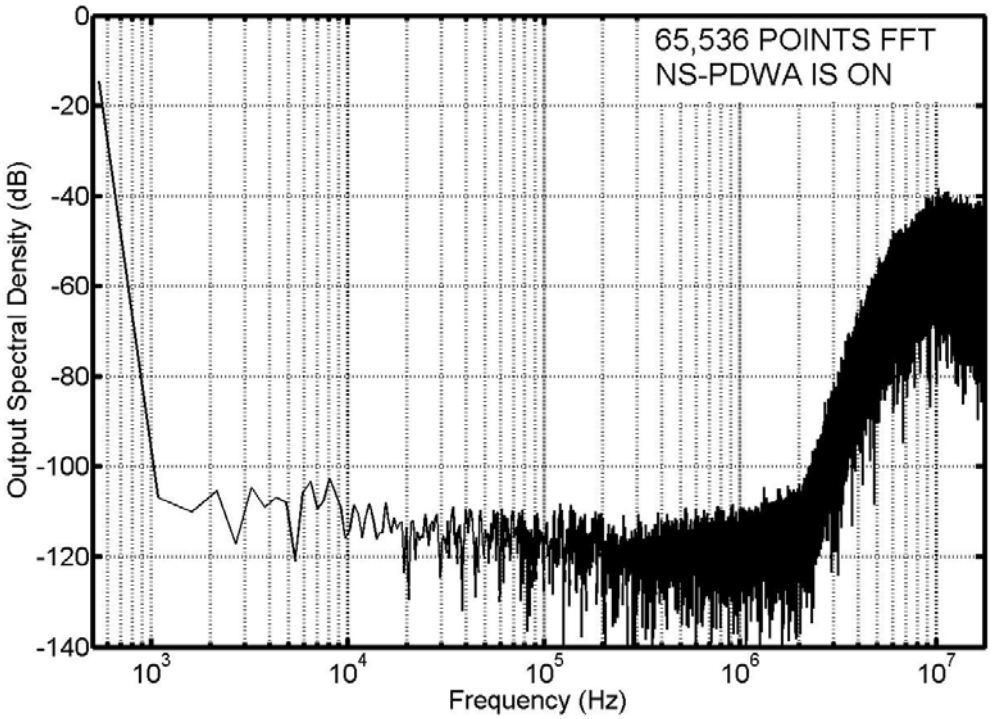


Figure 100. Measured output spectrum with NS-PDWA and zero input signal.

The harmonic distortion starts to show up when the input signal amplitude approaches the full scale. This is evident in the SNDR, SNR and SFDR plots, given in Figure 101. The degradations of peak SFDR and SNDR at high input level are mainly due to the input switch sampling distortion. This is because, if the degradation of SFDR is due to the nonlinearity or tones from DAC, PDWA would remove these tones, but would cause the noise floor to rise when NS-PDWA is not in action. However, this is not observed during the test. That implies the matching of the testing sample is good enough. The tone appears at high input level due to the nonlinear input sampling switch not the DAC mismatch no matter PDWA on or off. Figure 102 and Figure 103 show the measured output spectrum with PDWA on and off respectively, where the input sinusoidal signal is at 189.06 kHz and -9dB below the full reference scale. The SNDR doesn't drop at high input level, unlike the drop due to the accumulator's overflow in the behavior simulation, because the noise floor is limited by the *kT/C*

noise and the mismatch noise is relatively small.

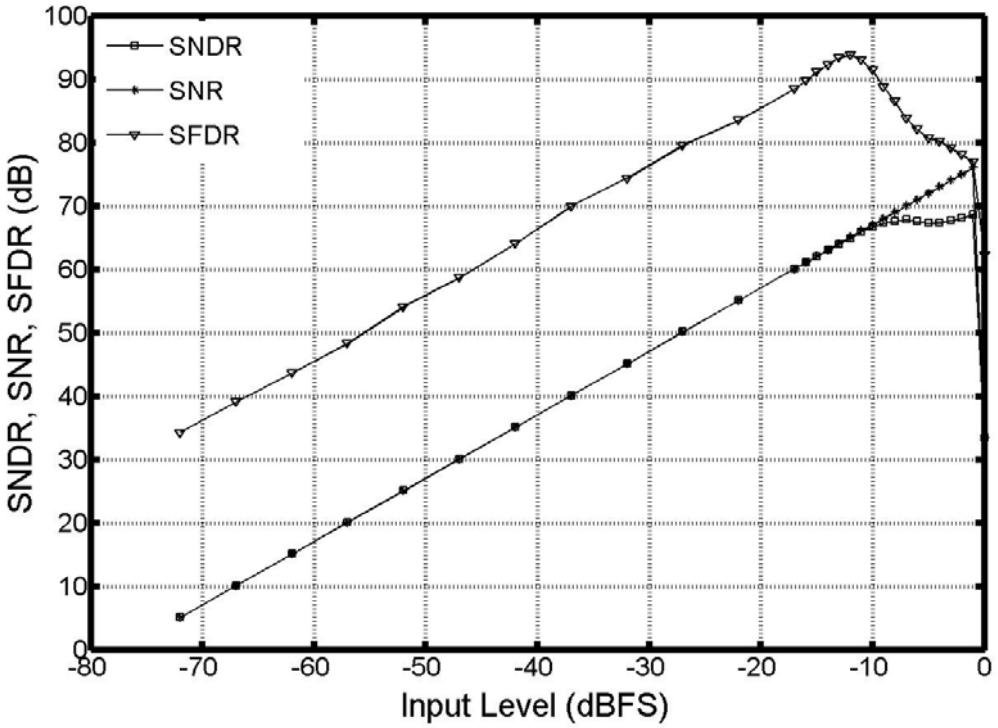


Figure 101. Measured SNDR, SNR and SFDR

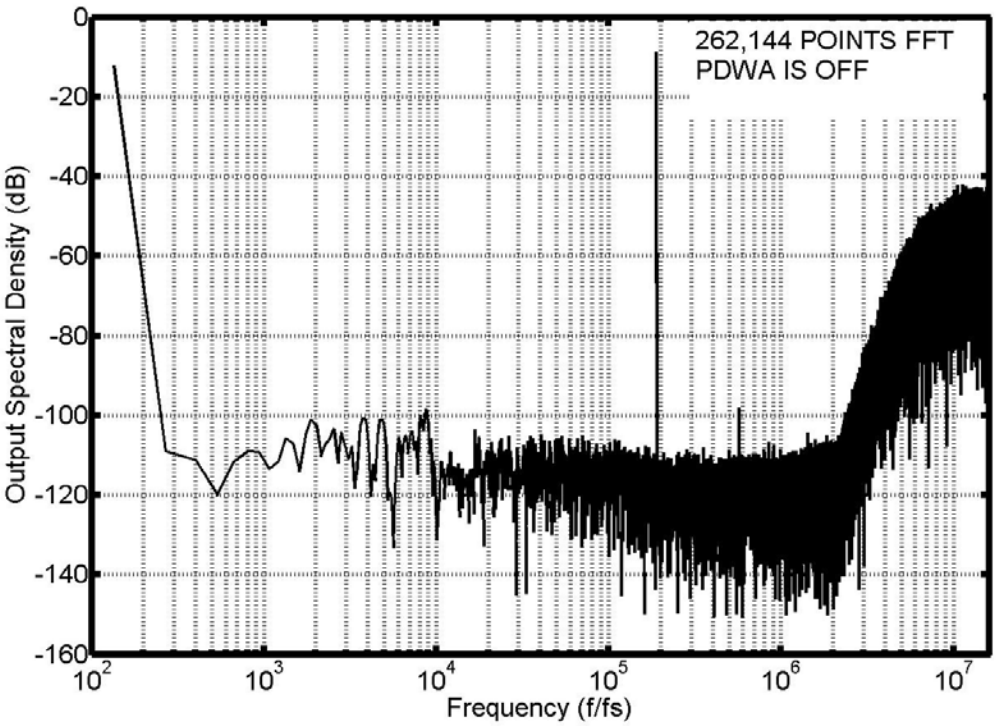


Figure 102. Measured output spectrum with PDWA off and input signal.

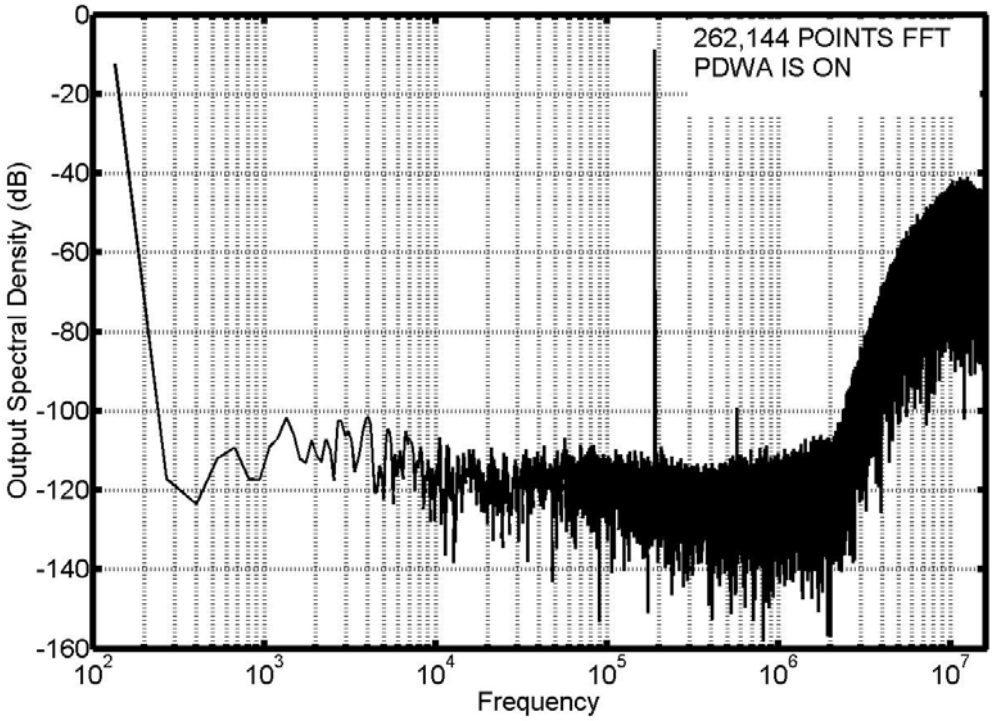


Figure 103. Measured output spectrum with PDWA on and input signal.

The measured DR is 78dB, and the peak SNR and SNDR are 77dB and 69dB respectively. The differential FS (Full Scale) input is $5V_{p\text{-}p}$. The power consumption is 62mW under a 3.3V supply voltage. The performance is summarized in Table 8 and the chip microphotograph is shown in Figure 104. The core chip area is $1.5\text{x}1.3\text{mm}^2$.

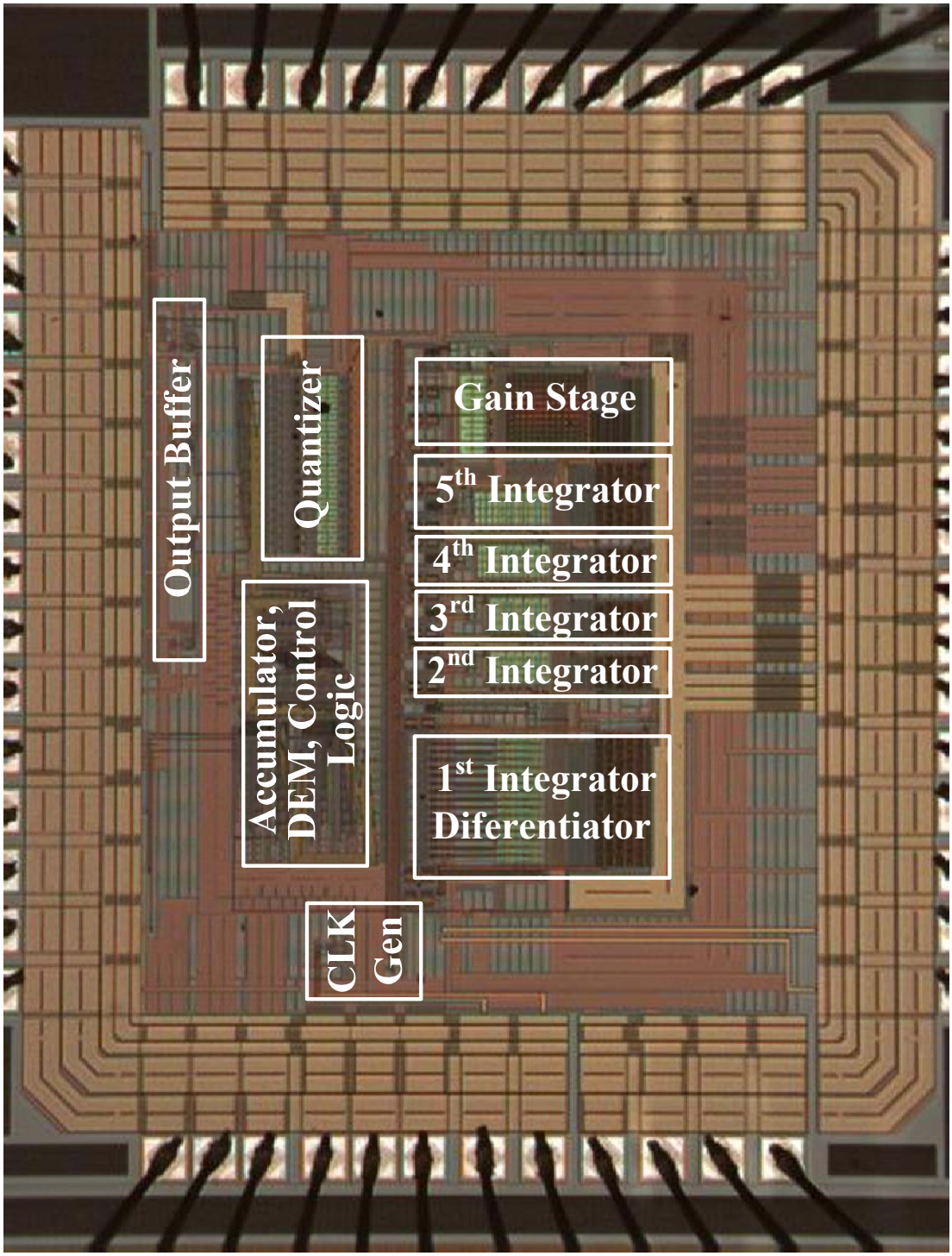


Figure 104. Die microphotograph

Table 8. Performance Summary

| PARAMETER | VALUE |
|---|---|
| Signal Bandwidth | 2.2MHz |
| Clock Frequency | 35.2MHz |
| Oversampling Ratio | 8 |
| SFDR | 94dB |
| Dynamic Range | 78dB |
| Peak SNR | 77dB |
| Peak SNDR | 69dB |
| Input Range | $5V_{pp}$ (differential) |
| Core Area | $1.5x1.3mm^2$ |
| Total Power Consumption | 62mW |
| Power Supply Voltage | 3.3V |
| Technology | 0.35µm CMOS |

# Chapter 6 Conclusions and Future Work

## 6.1 Conclusion

In this thesis, an NS-DEM technique has been proposed to improve the linearity of the multi-bit ΔΣM. NS-DEM works with most existing DEM techniques and provides further spectral noise-shaping to the DAC errors. The proposed technique eliminates the trade off between SNR and SFDR in most existing DEM techniques,

The NS-DEM is analyzed and evaluated in the behavior simulation and has shown an improvement in both SFDR and the SNR. The NS-DEM is more effective at low input signal level or signal with less dc component, while less effective at large input amplitude. . This is because of the overflow of the accumulator, which impair the noise shaping performance of the NS-DEM and result in the SNR degradation at high input signal level and low frequency signal.

The noise shaping concept of the NS-DEM is first experimentally demonstrated in a dithered noise shaping DAC in a 0.35-μm CMOS technology. The first-order noise shaping has been observed in the measurement.

The NS-DEM has also been employed in a lowpass $5^{th}$-order 4-bit quantization ΔΣM emplying NS-PDWA, which is aimed for ADSL2+ application. The fabricated ΔΣM chip is fully operational and achieves 94dB for SFDR and 78dB for DR in 2.2MHz BW, which meets the specification intended for ADSL2+ application.

## 6.2 Original Contribution

- A new noise shaping dynamic element matching (NS-DEM) technique for improving the DAC linearity. Unlike most of the existing DEM techniques that trade SNR for SFDR, the NS-DEM improves both SFDR and SNR of the

DAC.

- NS-DEM technique is validated with 5 existing widely used DEM algorithms. In principle, it can work with any DEM algorithms.
- A 5-bit DAC with the NS-DEM (dither) in 0.35 μm CMOS technology.
- A lowpass $5^{th}$-order 4-bit quantization ΔΣM employing NS-DEM (PDWA) in 0.35 μm CMOS technology.
- The concept of a bandpass ΔΣM employing NS-DEM.
- The incorporation of the differentiator into the first-stage loop filter in a lowpass ΔΣM without incurring any additional analog circuit.
- An accumulator realized by a register and a proposed new adder based on the thermalmeter code.

## 6.3 Future Work

In this design, it has been noted that tones come out when a large input signal is distorted by the input switch. Therefore, some solutions, such as bootstrapping, can be employed to remove this limitation, making the ΔΣM more linear over the whole input level. One of the common solutions is to use the bootstrapped circuit to ensure the constant Vgs.

Due to the reduced supply voltage and increased signal bandwidth, the continuous-time ΔΣM becomes more favorable nowadays. .The proposed NS-DEM may be further employed in continuous-time ΔΣMs where the DAC nonliearity is also a threat. .

Since the overflow is a major concern in NS-DEMS, the input-referred offset and 1/f noise of the whole ΔΣM should be minimized. Therefore, some techniques, such as auto-zero and chopper, may be employed to minimize the in-band offset and 1/f noise.

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