SIGMA-DELTA CLASS D AUDIO POWER AMPLIFIER

IN CMOS TECHNOLOGY

PAN JUNLE

(B.Eng.(Hons.).NUS)

A THESIS SUBMITTED

FOR THE DEGREE OF MASTER OF ENGINEERING
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2009

ACKNOWLEDGEMENT

I would like to express my sincere appreciation and utmost gratitude to my project supervisors, Assistant Professor Yao Libin and Associate Professor Lian Yong, for their invaluable advice, guidance, patience, encouragement and support throughout the duration of this project. I am extremely grateful for all the time they spent helping me with my problems and pointing me to the right direction.

CONTENTS

ACKNOWLEDGEMENTS …… i

TABLE OF CONTENTS……...……ii

SUMMARY ……..…… vii

LIST OF TABLES …….. viii

LIST OF FIGURES ……. ix

LIST OF SYMBOLS AND ABBREVIATIONS …… xiv

CHAPTER 1 INTRODUCTION ……..…….……..1

1.1 Background ……..……1

1.2 Objective ……. .2

1.3 Project Flow ……..……..…... 3

1.4 Thesis organization and Publication……4

CHAPTER 2 BACKGROUND OF CLASS D POWER AMPLIFIER …..… 5

2.1 Background of Audio Power Amplifier ……..…….5

2.1.1 Linear Amplifier …….....……6

2.1.2 Switching Amplifier ……..….. 9

2.2 Performance Metrics for Audio Power Amplifier ……...……...… 12

2.2.1 Power Efficiency(η) ……. 12

2.2.2 Dynamic Range (DR) ……...…… 12

2.2.3 Total Harmonic Distortion (THD) ……..…….13

2.2.4 Signal to Noise Ratio (SNR) …… 14

2.2.5 Power Supply Rejection Ratio (PSRR) ……14

2.3 Conclusion ……..…..... 15

CHAPTER 3 ARCHITECTURAL DESIGN ……....…..…. .16

3.1 General Achitecture of Class D Amplifier ……...…...…….. 16

3.2 Signal modulation scheme ……..…..…… 19

3.2.1 Pulse Width Modulation ……...…… 20

3.2.2 Sigma Delta Modulation ……...…… 22

3.3 Architectural of output stage ……..…….. .24

3.3.1 Half bridge output …… .25

3.3.2 Full H bridge output …….…… ..27

3.3.3 Dead time and distortion ……..…… ...30

3.4 Three-level switching scheme for SDM ……....…..…… ...35

3.5 PSRR and Feedback Topology ……..……...…….… ...39

3.6 Overall architectural design …….…….... ...43

CHAPTER 4: SIGMA-DELTA MODULATOR DESIGN ……..……44

4.1 Basis of Sigma-Delta Modulator ……. 45

4.2 System level design……...……50

4.2.1 System Level Design Parameters ……... 50

4.2.1.1 Modulator Architecture ……...…….. .50

4.2.1.2 Oversampling Ratio ……... 52

4.2.1.3 Loop Coefficient …… 53

4.2.1.4 Order of Loop Filter ……..….. .53

4.2.1.5 Number of bit for quantizer …….…….. .54

4.2.2 Stability analysis of single loop SD modulator ……..….. 56

4.2.3 Fully feed-forward topology ……..……. 60

4.2.4 System parameters optimization ……. 67

4.2.4.1 Architecture of SD Modulator ……..…….. 67

4.2.4.2 Order of Loop Filter and OSR ……..…….. 68

4.2.4.3 Loop Coefficient Optimization …… ……. 72

4.2.4.4 OTA Gain …… ……. .75

4.2.4.5 Effect of OTA Offset …… …… 78

4.2.4.6 Overall System Level SD Design …… …… …….…. 82

4.3 Circuit Implementation …… …… …….……. ……... 83

4.3.1 OTA Design …….…….…….…….. 85

4.3.2 Comparator and 1.5-bit quantizer design ……..…… 92

4.3.3 Sampler Design ……..……. .95

4.3.4 Non-overlap Clock generator design ……...……. .97

4.3.5 Feed Forward Summing Design ……...……. 99

4.3.6 Feedback and Vref generation.....100

CHAPTER 5: OUTPUT STAGE DESIGN ……102

5.1 Full H-bridge Output …….……...….…….102

5.2 Gate Driving Circuit ……..……..……106

5.3 Output LPF ……...….. 110

CHAPTER 6: MEASUREMENT RESULTS……113

6.1 H-bridge output waveform comparison (simulation) ……..…..117

6.2 Output waveform ……...……119

6.3 THD+N performance ……..... 123

6.4 Output Dynamic Range …… 126

6.5 PSRR …… 127

6.6 Overall power efficiency …….……. 129

6.7 Conclusion …….…….…….. 131

CHAPTER 7: CONCLUSION ……...…..135

REFERENCE……..136

APPENDIX……..…141

Summary

A one-channel high power efficiency Class D audio power amplifier utilizing full-feedforward Sigma-Delta topology is introduced. Compared to conventional structure, the power efficiency of this design is improved by using a novel three-level switching scheme which greatly reduces the switching activity of the modulator output and the power transistors, especially when the input power is small.

The main building blocks of this Class D power amplifier are high-linear single loop full-feedforward Sigma-Delta modulator, power transistors driving circuit and full H-bridge output stage. The output signal of the full H-bridge is directly feedback to the Sigma-Delta modulator which improved the PSRR of the power amplifier.

This design is realized in 0.35μm CMOS technology. The power transistors and the Sigma-Delta modulator are integrated in a single chip which has 3.97 mm^2 active area. The testing results show that the power efficiency for low input power is truly improved by using new switching scheme. The operational power supply for this design is ranged from 2.5 V to 4.5 V. With 3.3 V power supply, the THD reaches 0.0817% at 0.1 W output power and the PSRR is 64.8 dB. With 4 Ohm load, the maximum power efficiency is 80%.

LIST OF TABLES

Table 1.1: Design Specifications**.....3**

Table 4.1: Calculated SRN of 1-bit quantization ideal SD modulator [Pel97] **….. 69**

Table 4.2: SNR performance of stable 2nd to 4th order conventional SD modulator with optimized loop coefficient [Pel97] **…….....….. 70**

Table 4.3: SNR performance of 2nd to 4th order fully feed forward SD modulator with optimized loop coefficient [Yao05] **……...……..…….. 71**

Table 4.4: Output states of the 1.5-bit quantizer **……..……..…….. 95**

Table 5.1: Components value for the LPF **……...…….…… 112**

Table 6.1: Summary of measurement results **…….…..……..131**

Table 6.2 Performance Comparison**.....134**

LIST OF FIGURES

Fig 2.1.1a: Class A amplifier ..…… 7

Fig 2.1.1b: A single Class B element ……...7

Fig 2.1.1c: Class B push-pull amplifier …….……..8

Fig 2.1.2: Power efficiency of Class D VS. Class AB ……..……..11

Fig 3.1: Block diagram of a Class D amplifier ……..…..……. 16

Fig 3.2: Typical PWM input and output signal …….....20

Fig 3.3: Typical output waveform of two-level quantization SD modulator 22

Fig 3.4 Half bridge output circuit …….……..…..…..25

Fig 3.5: Supply voltage pumping effect …….…...…….....27

Fig 3.6: Differential output stage and its LC LPF ……..…...…...27

Fig 3.7: Local current loop to prevent pumping effect ……..…...……...29

Fig 3.8: Dead time of output control signal ……...……..30

Fig 3.9: Current flow in full H bridge …… 32

Fig 3.10: H-bridge output voltage and load current of 1-bit SD modulator..... 36

Fig 3.11: H-bridge output voltage and load current of 1.5-bit SD modulator…..37

Fig 3.12 Normalized switching activity of 1 bit and 1.5 bit SD modulator at different output power …….....…… 38

Fig 3.13: Linear model for open loop class D amplifier ……... 39

Fig 3.14: Linear model for class D amplifier with feedback …….……40

Fig 3.15(a): Model of SDM class D amplifier with feedback from quantizer…. 41

Fig 3.15(b): Model of SDM class D amplifier with feedback from H bridge 42

Fig 3.16: Block diagram of proposed class D amplifier ……...… 43

Fig 4.1: Structure of simplest single loop 1st order SD modulator ……..…...45

Fig 4.2: Noise Injection model for 1st order conventional SD modulator ….....46

Fig 4.3: Frequency response of SD modulator due to Noise shaping ……....…. 47

Fig 4.4: Conventional 2nd order single loop SD modulator ……..…...… 48

Fig 4.5: Quantization noise in Nyquist rate sampling and oversampling …..... 49

Fig 4.6: A 4th order cascaded 2-1-1 SD modulator [Yao05] ……...… 52

Fig 4.7: Variable gain linear model for SD modulator …….....57

Fig 4.8: Root locus of the poles for 3rd order conventional SD modulator…. 58

Fig 4.9: 1st order single loop fully feed forward SD modulator ……..... 60

Fig 4.10a: Integrators output of 4th order conventional SD modulator.....65

Fig 4.10b: Integrators output of 4th order fully feed forward SD modulator.....65

Fig 4.11: A 3rd order fully feed forward SD modulator ……..…..…66

Fig 4.12: SNR vs OSR for the proposed 4th order modulator ……..……..…..72

Fig 4.13: Contour plot of SNR with a1 and a2 as sweeping variable …….…..73

Fig 4.14a: PSD of 4th order conventional SD modulator with non-linear OTA, Ao=40dB ……..……..……. 76

Fig 4.14b: PSD of 4th order fully feed forward SD modulator with non-linear OTA, Ao=40dB …….....……...…….. 76

Fig 4.15: SNR performance base on OTA gain for proposed SD modulator…...78

Fig 4.16a: Effect of 1st stage OTA offset alone ……....…… .80

Fig 4.16b: Effect of 2nd stage OTA offset alone ……....…….…...80

Fig 4.17: Overall architectural of proposed 4th order fully feed forward SD modulator with a 1.5-bit quantizer 82

Fig 4.18: Circuit implementation of proposed 4th order fully feed forward SD modulator …….....……..… 84

Fig 4.19: Schematic design of the single stage telescopic OTA ……...… 87

Fig 4.20: AC response of 1st stage OTA with 16pF loading capacitance ……... 90

Fig 4.21: Switch-capacitor CMFB ……...….. 91

Fig 4.22: Schematic of regenerative latch comparator. ……..…. 92

Fig 4.23: 1.5-bit quantizer …….…… 94

Fig 4.23a: Schematic of sampler.....95

Fig 4.23b: equivalent circuit at sampling phase …….....…..…… 95

Fig 4.24: Clock generator …….……..…. 98

Fig 4.25: Output of clock generator …….…..……. 98

Fig 4.26: Summing point of the feed forward path …….…..…… 99

Fig 4.27: Reference voltage generation circuit.. …….....…….100

Fig 5.1: Output stage of class D amplifier: Gate Driver, H-Bridge and LPF ……..…… 102

Fig 5.2: Test bench for extraction of on-resistance …….…….……... 106

Fig 5.3: structure of gate driver …….…….. .107

Fig 5.4: Differential version of LC LPF for Class D amplifier …….……..… 110

Fig 6.1: Die Photo …….……. 113

Fig 6.2: Photo of Testing PCB ……...…..……. 114

Fig 6.3: Schematic of testing PCB ……...…...…….. 116

Fig 6.4: Output pulse train with 1-bit SD modulator at high output power …….....…….…… 117

Fig 6.5: Output pulse train with 1.5-bit SD modulator at high output power …….……. 117

Fig 6.6: Output pulse train with 1-bit SD modulator at low output power …….……. 118

Fig 6.7: Output pulse train with 1.5-bit SD modulator at low output power …….…….....…… 118

Fig 6.8: Output waveform of H-bridge without load ……... 119

Fig 6.9: Output waveform of LC LPF without load ……...… 120

Fig 6.10: Output waveform of H-bridge with 4 Ohm load …….……. 121

Fig 6.11: Output waveform of LC LPF with 4 Ohm load ……...…… 121

Fig 6.12: Output spectrum of LPF with 4 Ohm load at 0.16FS output power …….....…… 124

Fig 6.13: THD+N VS Output power of designed class D amplifier ……...… 124

Fig 6.14: THD+N VS input frequency of designed class D amplifier ….....… 125

Fig 6.15: Noise floor of LPF output within audio band …….…..... 126

Fig 6.16: Output power spectrum with 101Hz supply noise …….....….. 128

Fig 6.16: Power efficiency with 4 Ohm load @ 3.3V supply …….…...…..….. 129

Fig 6.17: Power efficiency VS output power in Reference [Axh07].....132

Fig 6.18: Power efficiency VS output power in Reference [Cho06].....133

LIST OF SYMBOLS AND ABBREVIATIONS

K	Boltzmann's Constant, 1.38 x 10^{-23} m^2 kg s^{-2} K^{-1}
T	Absolute Temperature, 273K
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DC	Direct Current
FFT	Fast Fourier Transform
NMOS	N-channel MOS
NTF	Noise Transfer Function
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PMOS	P-channel MOS
PSD	Power Spectral Density
PSRR	Power supply rejection ratio
PWM	Pulse Width Modulation
RF	Radio Frequency
SNR	Signal-to-Noise Ratio
VLSI	Very Large Scale Integrated Circuit
SD	Sigma-Delta

Chapter 1: Introduction

1.1 Background

Portable audio electronic devices such as mobile phone, MP3 player, have grown in popularity. They employ a power amplifier to drive a small loud speaker. Since these portable devices are powered by batteries and the power consumption of the audio system is significant to the total power consumption of devices, a highly efficient power amplifier with low power dissipation and low distortion is required [Kyo08]. The class D power audio amplifier provides a good solution in term of power efficiency. Compared to traditional class AB audio power amplifier, whose maximum power efficiency is around 60%, the class D power amplifier nowadays achieves much higher power efficiency. The theoretical maximum efficiency of a class D amplifier is 100%, but practically achievable is 90% at high output power [Axh07]. High power efficiency of class D power amplifier effectively reduces the supply current requirement so that the operation time of batteries is longer. Besides that, high power efficiency implies that less power is dissipated on the power amplifier itself. This greatly relaxes the thermal problem commonly found in power

amplifier. The bulky heat sink for power amplifier can even be eliminated to further reduce the size of the portable devices [Dap00]. These two advantages of class D audio power amplifier make it widely used for portable audio application.

The major drawback of class D power amplifier is its higher distortion level compared to other type of power amplifier. Apart from distortion, electromagnetic interface (EMI) caused by high frequency switching operation is another problem [Ber03]. Therefore, to design a class D audio power amplifier which produces good quality sound with high efficiency is a big challenge.

1.2 Objective

The main objective of this project is to design a 1-channel class D audio power amplifier using full-feedfoward Sigma Delta modulator using 0.35 μm CMOS technology with 3.3 V power supply. The design aims to maximize the power efficiency with low distortion and high PSRR. The load for this design is a 4Ω or 8Ω resistive load. Table 1.1 shows the design specifications for this project:

Table 1.1: Design Specifications

Power Supply	3.3V
Quiescent Current	<10mA
Load	4Ω or 8Ω
Dynamic Range	>90dB
Maximum Output Power	1W
PSRR	>60dB
THD+N	<0.1%
Maximum Power Efficiency	>80%
Active area	As small as possible

The design is done in Cadence EDA environment. This design is fabricated for the evaluation of the chip performance. Apart from the design of IC chip, testing PCB and the output filter for the class D power amplifier are also designed for the testing purpose in this project.

1.3 Project Flow

This research project can be separated into four stages. The first stage is paper research. The most recently published papers on class D power amplifier are studied in order to get a clear view on the research work done in this area. The second stage is the system level design. In this stage, the architecture of the power amplifier and the specifications of building blocks are determined. A single-stage 4th-order fully feedforward Sigma-Delta modulator is adopted to modulate the input signal. The third stage is transistor level schematic and layout design with simulation verification. Corner simulation and Monte Carlo simulation are carried out in this stage to ensure

that the design is able to work properly with process variations in fabrication. The last stage is the design of testing PCB and evaluation of the fabricated IC chip. In this stage, the performance of the designed class D power amplifier is extracted and compared with other designs.

1.4 Thesis organization and publication

This thesis is presented in seven chapters. Chapter 1 shows the motivation of this project and defines design specifications. Chapter 2 introduces the background knowledge of audio power amplifiers and the performance metrics. Chapter 3, 4 and 5 are the main body of this thesis. They include the details of system level design, block level design and transistor level design. Chapter 6 presents the details of sample chips measurement and the performances comparison between this design and other designs in recent publications. Chapter 7 gives brief conclusion of this project and suggests the direction of further improvement of the design.

This design had been published in International SoC conference 2008, Busan, South Korea. The publication list is shown in Appendix.

Chapter 2:
Background of Class D Power Amplifier

In this chapter, a short introduction of different types of power amplifier architectures and their trade-offs is discussed. Several general performance parameters are introduced and followed by the basic background knowledge about the class D power amplifier.

2.1 Background of Audio Power Amplifier

Audio power amplifier is an electronic device that produces high-power replication of low-power audio signal to deliver driving power for loudspeakers. Generally power amplifier can be classified into two categories: linear amplifier and switching amplifier.

2.1.1 Linear Amplifier

Class A, Class B and Class AB power amplifiers are the commonly used linear power amplifiers. The output devices of a linear amplifier are operating at linear region for bipolar junction transistors or saturation region for CMOS transistors. They act as active resistors to regulate the power delivery to loads.

In Class A amplifier, the output devices are continuously conducting for the entire cycle. This avoids turning the output on and off and hence Class A amplifier has very high linearity. However, since the output devices are always conducting current even if there is no input at all, power is wasted and this results in very low power efficiency. The power efficiency of Class A amplifier is typically from 5% to 25%. Inefficiency of Class A amplifier introduces serious problems that limit its usage as audio amplifier although it delivers best sound quality. First of all, its low power efficiency results in very high heat dissipation on the amplifier itself when large output power if required. Huge and expensive heat sink is needed. Secondly a powerful power supply is also required in order to drive a Class A amplifier.

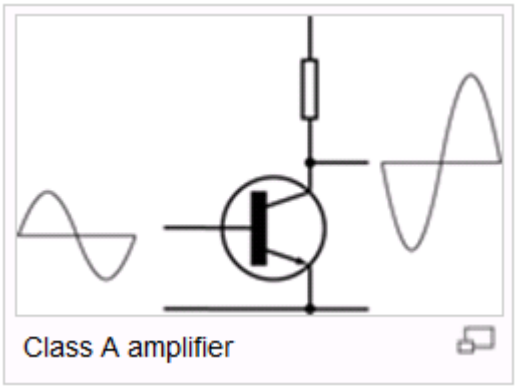

Fig 2.1.1a: Class A amplifier

In Class B amplifier, one output element only conducts half of the input wave cycle. Therefore, its power efficiency is greatly improved compared with Class A amplifier. Theoretically, Class B amplifier has maximum power efficiency up to 78.5%. However, there is trade-off between linearity and power efficiency. Since one output element only conducts in one half cycle and completely off in another half cycle, it creates large amount of distortion. Class B amplifier with single amplifying element is hardly found in application.

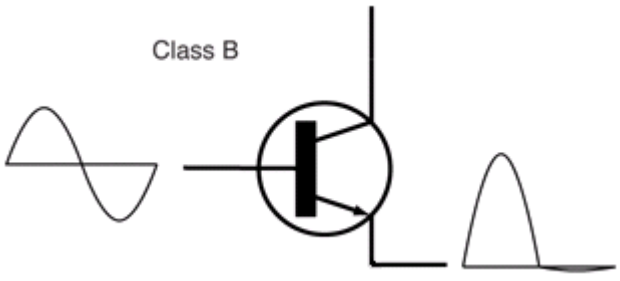

Fig 2.1.1b: A single Class B element

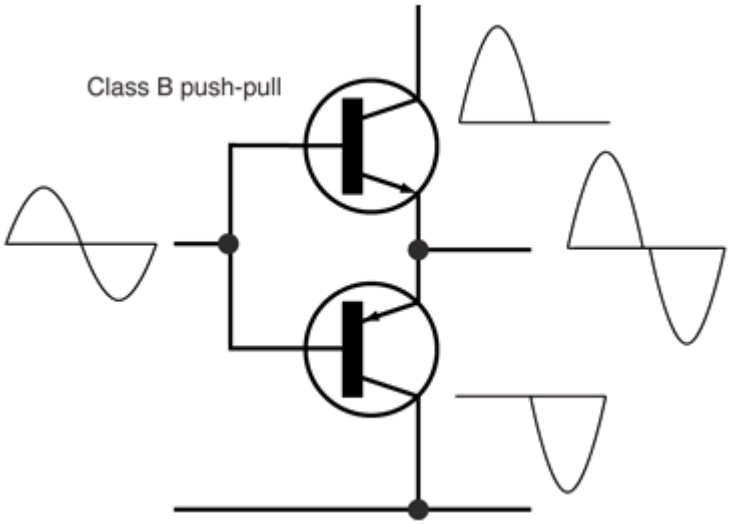

Fig 2.1.1c: Class B push-pull amplifier

In practical, the push-pull arrangement is commonly used in constructing Class B amplifier. Two Class B elements work together to form a complementary pair. Each amplifies one half of the input wave cycle and then combines them in the output to generate a full cycle output waveform. Although this architecture performs much better than the single Class B element, it suffers from crossover distortion. This refers to the small mismatch at the crossover point between the two halves of the output signal. This distortion reduces the linearity of the Class B push-pull amplifier. Many attempts have been made to reduce the crossover distortion. One is to bias the output elements to avoid completely turn-off when they're not in use, which is known as Class AB operation.

Strictly speaking, Class AB amplifier is not a separate class. It is the combination of Class A and Class B. Each output element in Class AB conducts current more than 50% and less than 100% of input wave cycle, which depending on the biasing of the output devices. Class AB is a good compromise between power efficiency and linearity and it is widely used for audio amplifier.

In general, linear amplifiers have high linearity and low distortion in term of performance. Apart from that, gain of linear amplifiers is constant and it is not a function of supply voltage. Hence, their power supply rejection ratio (PSRR) is also high. However, the power efficiency of linear amplifiers is usually low, which is about 50% typically. Low power efficiency makes it unsuitable to be used in batteries-driven portable electronic devices.

2.1.2 Switching Amplifier

Most of time, the switching amplifier refers to Class D amplifier. Its operation is very different from linear amplifiers: The output devices of Class D amplifier operate as switches which are turned completely “on” or completely “off”, making their resistance either zero or infinity in ideal case. The output devices are almost not losing any power by operating in this way: when the devices are complete “on”, the

voltage difference across them is zero; when the devices are complete “off”, the current flows through them is zero. Since the power dissipated in the output device is the product of the voltage difference and current flow, ideally, the power dissipated in devices is zero no matter in “on” state or in “off” state. Therefore, the power efficiency of Class D amplifier is 100% theoretically.

However, in reality the power efficiency of Class D amplifier can never reach 100%. This is because there is no ideal switch in practice. The small on-resistance at “on” state and non-infinite resistance at “off” state of the switch dissipates power on the switch itself. Besides the imperfection of the output devices, high frequency switching of the output devices also causes power loss. In real switching process, the output devices cannot be turned “on” or “off” immediately. There is transition time between “on” and “off”. During the transition period, neither the current flow nor the voltage difference of the output devices is zero, and hence power is dissipated on the devices. Furthermore, in order to reduce the on-resistance of the output devices, the size of the output devices is usually large. This introduces large parasitic capacitance to the output devices. In the switching process, high frequency charging and discharging of the parasitic capacitance waste power. These power losses related to switching process is named switching loss. It cannot be neglected if the switching

frequency is high. Last but not least, the power consumed by signal processing unit and gate driving unit of Class D amplifier further reduce its power efficiency.

In practice, the power efficiency of CMOS Class D audio power amplifier is typically 75% to 90%. High power efficiency implies less heat dissipation on the amplifier and less current requirement. Therefore, the power supply and heat sink requirements are relaxed for Class D amplifier. This helps to reduce the cost and device size. Furthermore, high power efficiency also helps to extend batteries life. Hence, compared to linear power amplifier, Class D amplifier is far more suitable to be used in portable electronic devices such as PDA, MP3 player and notebook.

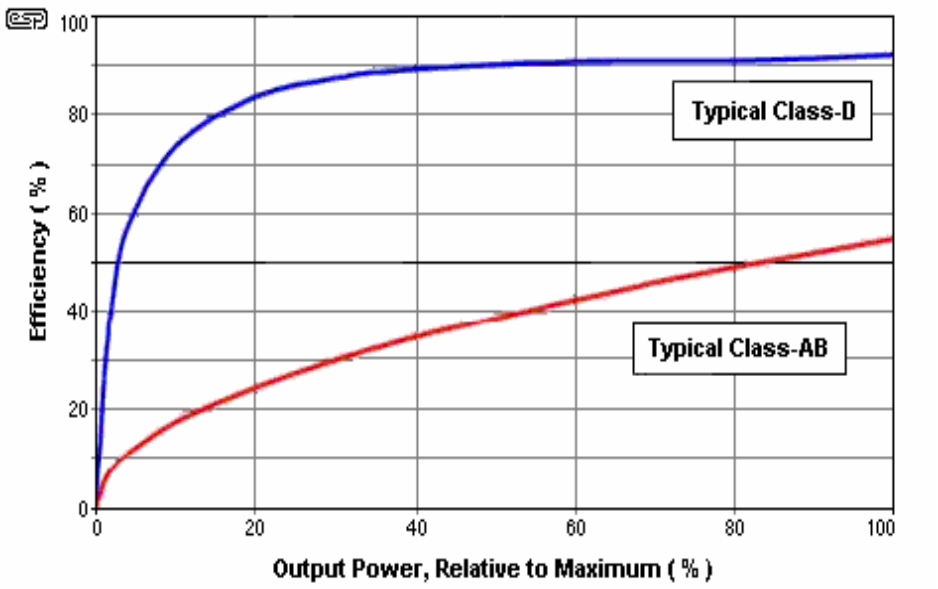

Fig2.1.2: Power efficiency of Class D VS. Class AB [int]

2.2 Performance Metrics for Audio Power Amplifier

The performance of audio power amplifier can be identified by some parameters, for example THD, PSRR, power efficiency and etc. The system parameters below are some of the most important ones.

2.2.1 Power Efficiency (η)

Power efficiency is the ratio of the power delivered to load and the total power delivered by the power supply. To maximise the power efficiency is always one of the design targets regardless of type of the power amplifier.

$$\eta = \frac{P_{out}}{P_{total}} \times 100\% = \frac{V_{out\_rms}^2 / R_L}{I_{total\_avg} \times V_{dd}} \times 100\% \qquad \text{(Equation 2.1)}$$

2.2.2 Dynamic Range (DR)

The dynamic range is specified as the ratio of the rms value of largest possible undistorted sinusoidal signal to the rms value of noise amplitude. The higher the

dynamic range, the better the amplifier performances. One can calculate the dynamic range of an amplifier by the following equation:

$$DR = 20 \times \log_{10} \frac{V_{O\max\_rms}}{V_{noise\_rms}} \qquad \text{(Equation 2.2)}$$

2.2.3 Total Harmonic Distortion (THD)

THD is a measurement of linearity of a system. A non-linear system adds harmonic of original frequencies to introduce distortion to the signal. For audio amplifier, THD should be kept as low as possible so that it can reproduce good sound quality. The following equation shows the calculation of THD commonly for audio specification (percentage THD) :

$$THD = \sqrt{\frac{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \cdots + V_{hn}^2}{V_{signal}^2}} \times 100\% \qquad \text{(Equation 2.3)}$$

2.2.4 Signal to Noise Ratio (SNR)

SNR is the measurement that compares the signal level to the background noise level. It is defined as the ratio of the output signal power to the noise power within the bandwidth of interest. SNR can be calculated by the following equation:

$$SNR = 20 \times \log_{10} \frac{V_{signal\_rms}}{V_{noise\_rms}} \qquad \text{(Equation 2.4)}$$

2.2.5 Power Supply Rejection Ratio (PSRR)

PSRR describes the ability of a device to reject noise from power supply. The definition of PSRR is the ratio of the change in supply voltage to the corresponding change in output voltage of the device. PSRR varies in different frequency and generally it tends to worsen with increasing frequency. Ideal amplifier has infinite PSRR.

$$PSRR = 20 \times \log_{10} \frac{\Delta V_{dd\_rms}}{\Delta V_{out\_rms}} \qquad \text{Equation (2.5)}$$

2.3 Conclusion

In this chapter, the basis of Class D power amplifier is presented. It operates very differently from a linear amplifier. Using switching mode of the output device, Class D amplifier can achieve very high power efficiency, which is the main advantage for this type of amplifiers. Besides the Class D amplifier, other types of amplifier such as Class A, Class B amplifiers are briefly introduced in order to visualize the basic differences between switching amplifiers and linear amplifiers.

Chapter 3:
Architectural Design

Due to the switching nature of class D power amplifier, its structure is very different from conventional linear amplifier. The input signal must be modulated into switch control signal before it processes to output stage. In this chapter, the general architectural design of class D amplifier is discussed. An appropriate architecture of each building block is chosen and presented in the second half of this chapter.

3.1 General Architecture of Class D Amplifier

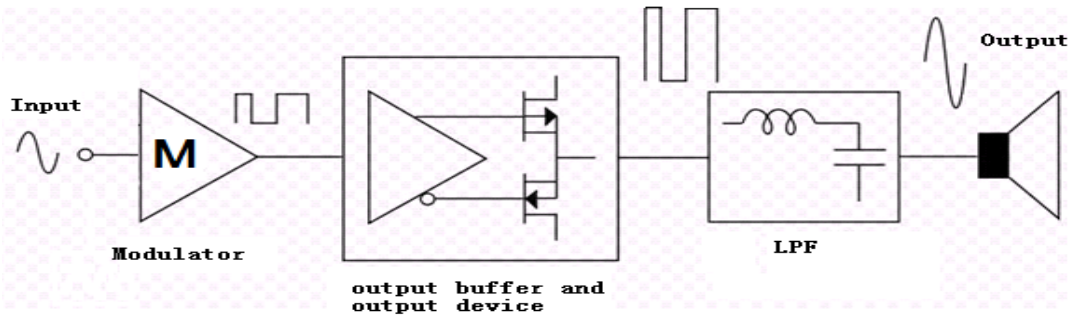

Fig3.1: Block diagram of a Class D amplifier

The above figure shows the general block diagram of a Class D amplifier. There are four main building blocks: signal modulator, output buffer, output devices (switches) and low pass filter (LPF).

The signal modulator is in charge of converting analog input signal into sequence of pulse. This pulse at modulator output is the digital representation of the analog input signal: its average value is directly proportional to the amplitude of the input signal at that time. In order to get an accurate estimation of the input signal, the frequency of pulse must be much higher than the bandwidth of the input signal. The pulse train from signal modulator is fed into the output buffer to generate the output switch control signal to regulate the power deliver to the loads.

The output buffer between the signal modulator and output devices is used for driving the output devices and introducing dead time. The output devices of solid-state Class D amplifier are usually power transistors which are very large in size. The purpose is to reduce the on-resistance to improve the power efficiency. Hence, the input capacitance of the output device is quite large due to its large size. In order to charge and discharge the input capacitance of the output device very fast to reduce the transition time, the output buffer between signal modulator and output power transistors is required. Besides to provide driving power to the gates, output buffer play a role in controlling the dead time to prevent shoot through current at output stage.

As mention above, the output device of a Class D power amplifier is usually half-bridge or full H-bridge. They consist of CMOS power transistors and work as switches to supply large current to drive Low Pass Filter (LPF) and speaker. The output signal from the H-bridge is high power pulse train. Unwanted spectral components of this pulse train, for example, the pulse frequency and its harmonics, must be removed by a passive low pass filter to reconstruct the input analog signal. This filter is usually made with (theoretically) lossless components like inductors and capacitors in order to maintain efficiency.

3.2 Signal modulation scheme

As shown in the previous section, the input audio signal needs to be converted into switch control signal to regulate the output power transistors to deliver current. This job is done with signal modulator. Although there are many ways to implement signal modulator for class D amplifier, the fundamental principle is the same: to encode information of audio input signal into a pulse stream. The spectrum of modulator output contains both high frequency pulse information and input audio signal content. Generally speaking, those modulation techniques produce bit stream that its pulse width or the pulse frequency is directly proportional to the instantaneous input amplitude. The most common modulation schemes used in class D amplifier are Pulse Width Modulation (PWM) and Sigma Delta Modulation (SDM). SDM technique is adopted in this project.

3.2.1 Pulse Width Modulation

As its name states, the pulse width of PWM modulator output is varying with the amplitude of the input signal. This can be achieved by comparing the input signal to a sawtooth waveform which is running at much higher frequency than the signal band [Kyo08]. Usually the sawtooth waveform has fixed carrier frequency. The pulse train produced by PWM modulator also runs in this carrier frequency. The figure below illustrates the idea of PWM clearly.

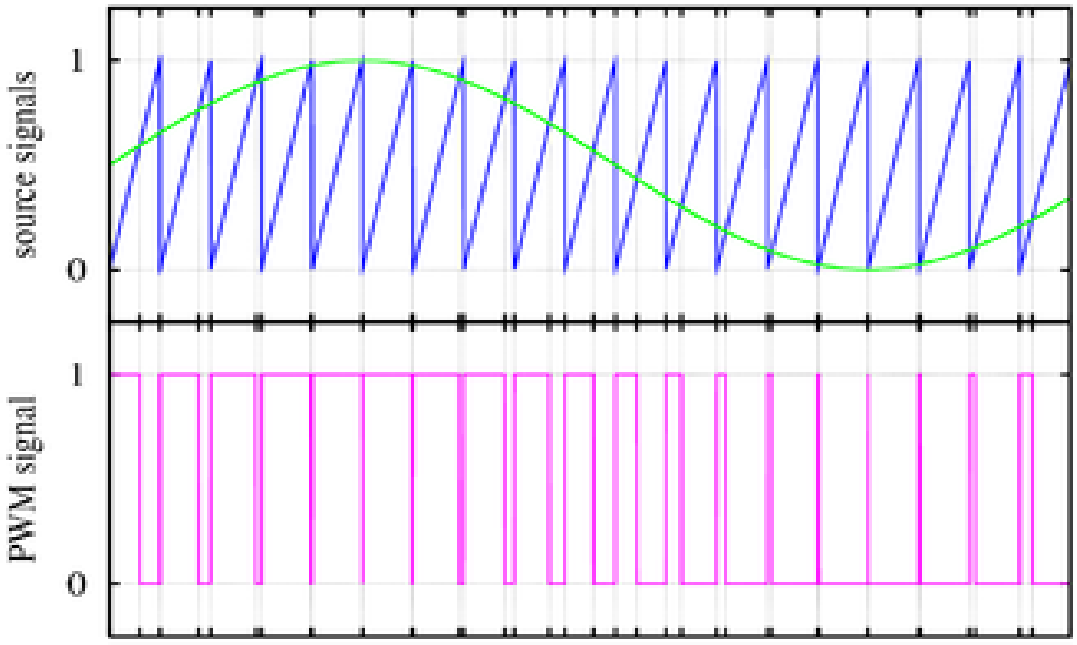

Fig3.2: Typical PWM input and output signal

If the audio input signal (green wave) level is higher than the sawtooth signal (blue wave) level, the output of PWM modulator is at high state, and visa versa. We

can see that the frequency of PWM signal is constant, but its duty cycle is changing with the input signal amplitude.

Some attractive features of PWM make it popular in class D amplifier design. Firstly, it can achieve above 100 dB signal-to-noise ratio (SNR) at audio band with as low as hundreds of kHz carrier frequency [Gaa05]. The low carrier frequency implies less power loss due to switching activity. Secondly, PWM modulator is stable at very high percentage of modulation [Gaa05]. This allows PWM to have high output power.

Unfortunately, there are some undesirable features of PWM modulator. First of all, as we can see from figure 3.2, the PWM signal has constant carrier frequency. This introduces concentrated high power peak at carrier frequency in spectrum. Its harmonics produce EMI with the AM radio band. Secondly, PWM process inherently adds distortion in many modulation schemes [Nie97]. One more problem is that when the input signal level is very low, the duty cycle of the PWM signal is very small for high percentage of modulation [Nie97]. It is clearly shown in figure 3.2. This very short pulse width creates problems in gate driving circuit design: if they do not have enough driving capability, they cannot switch fully on output power transistor to reproduce the short pulse. Therefore, full modulation is usually not achievable for PWM base class D amplifier which limits maximum output power of amplifier.

3.2.2 Sigma Delta Modulation

Compare to PWM, SDM encode input audio signal into steam of pulse in different way: instead of changing the duty cycle of pulse train in carrier frequency, SDM varies pulse density according to the input. The number of pulses in a time window is directly proportional to the average value of the input audio signal level at that instant. Therefore, SDM is a kind of Pulse Density Modulation. The typical output waveform of conventional two-level quantization SD modulator is below:

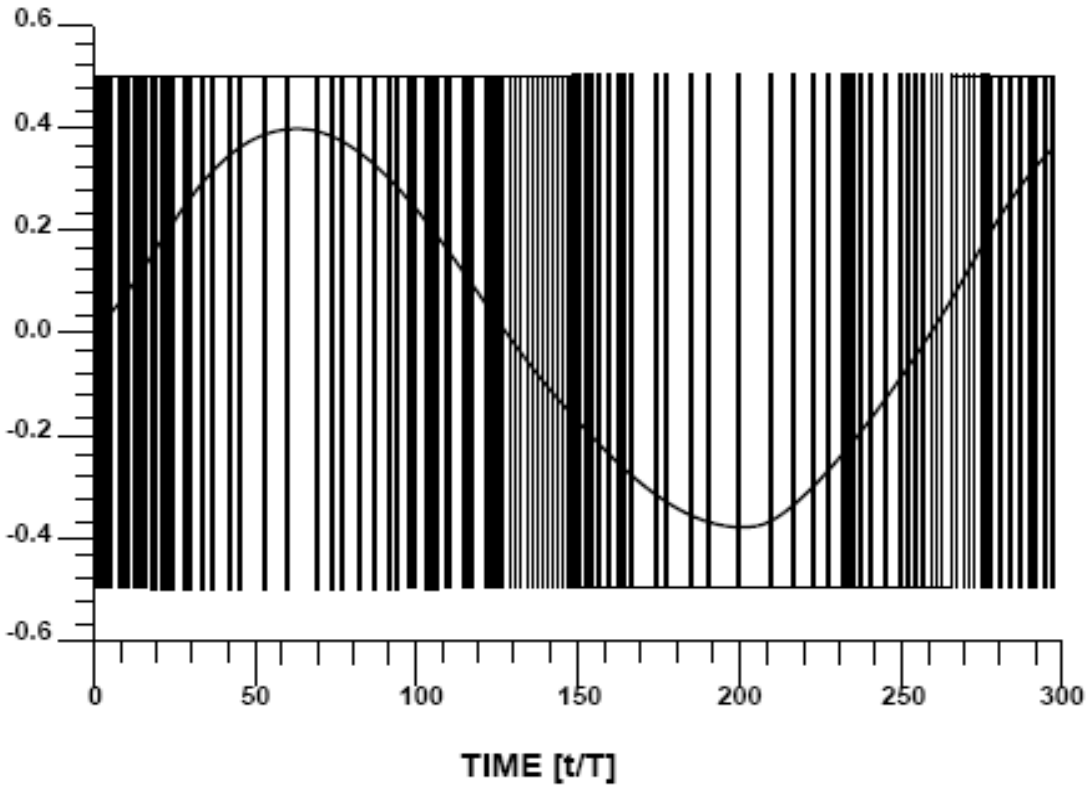

Fig3.3: Typical output waveform of two-level quantization SD modulator

Figure 3.3 clearly shows that the pulse density of the modulator output is directly proportional to the amplitude of the input signal. SM modulator makes a rough evaluation of input signal. The mean output value is equal to the mean input value.

From the above output waveform of SD modulator we can notice some of its interesting characteristics. First of all, its individual pulse width is fixed. This avoids short pulse width problem that imposed by PWM and relaxes the design requirement of gate driving circuit. Secondly, we can see that in time domain the SD modulator output is no longer running at a fixed frequency. It is varying with the input signal. Translate this into frequency domain imply that the high frequency energy in SDM is distributed over a wide range of frequency. This is an advantageous feature over PWM as there is no more concentrated tones at carrier frequency and its harmonics, which is able to reduce the EMI problem.

Apart from the characteristics stated above, there are two important features that make SDM attractive. They are Oversampling and Noise Shaping: Oversampling helps to reduce the quantization noise level while Noise Shaping helps to push in band noise out of band of interest so that the in band noise reduce further. These two features allow SDM to achieve high SNR within band of interest.

Since SD modulator is used in this class D amplifier design, more detail on SDM and the structure of SD modulator will be covered in next chapter.

3.3 Architectural of output stage

There are two commonly used output architecture for class D power amplifier: Half bridge circuit and full bridge circuit. Half bridge is the single ended output version while full H bridge is a differential implementation of the output power transistors. Each implementation has its pros and cons. In brief, half bridge is potentially simpler to implement while full H bridge has better audio performance. Apart from the output stage topology, the impact of dead time introduced by gate control circuit is also discussed in this section.

3.3.1 Half bridge output

The figure below shows a general half bridge circuit:

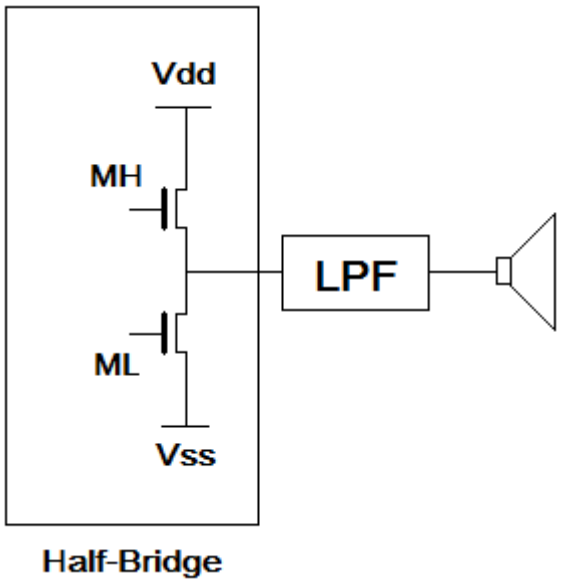

Fig3.4 Half bridge output circuit

MH and ML are the power transistors to deliver power. When MH turns on, charge is injected into LPF and speaker; when ML turns on, LPF is discharged and the voltage level at the LPF output is reduced. MH and ML are never turn on simultaneously to prevent creating low impedance path between Vdd and Vss.

Half bridge architecture is simpler than full bridge architecture. And it has the same functionality as the full bridge output. However, two disadvantages of half bridge structure limit its usage in class D amplifier:

- Half bridge structure can be powered by bipolar power supplies or single power supplies. However, with single power supplies, a harmful dc bias voltage which is half of Vdd is imposed across the speaker. It creates power loss so that degrades the efficiency of the amplifier. Therefore, this undesirable dc biasing voltage should be removed by inserting a large dc blocking capacitor in between the half bridge circuit and speaker. By doing this, the output filter becomes more bulky and costly.

- Half bridge also suffers from supply voltage pumping effect. Due to the single ended structure, the energy flowing in the output stage is bidirectional. The energy stored in the inductor of output LPF is kicked back into power supply bus. This introduces power supply noise which degrades the performance of class D amplifier. The voltage level of these spikes can be reduced by adding large decoupling capacitor in between Vdd and Vss. This also increases the cost of amplifier. The figure below shows how this pumping effect occurs:

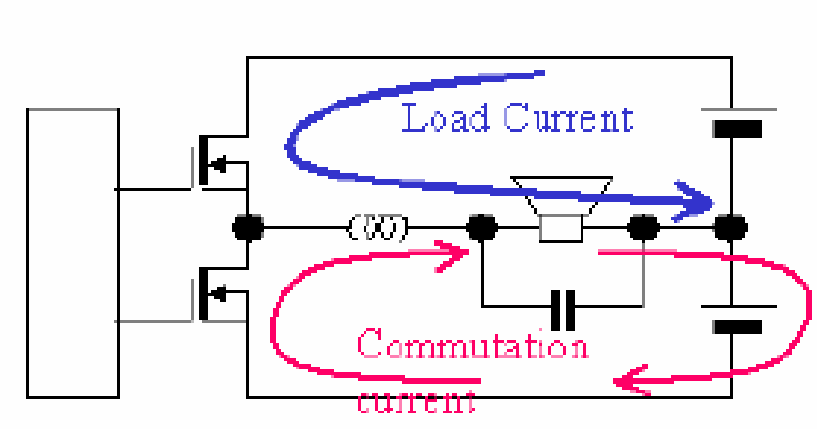

Fig3.5: Supply voltage pumping effect

As the single ended output version, half bridge circuit is simpler to build. However, due to its inferior performance compare to full H bridge, it is not widely used in class D amplifier design.

3.3.2 Full H bridge output

Full H bridge structure is the differential ended version of the output stage. The following figure show a full H bridge circuit.

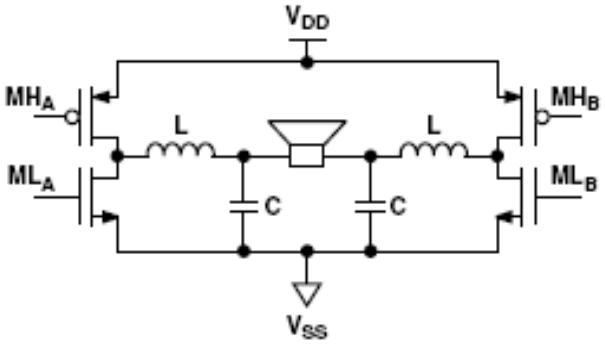

Fig3.6: Differential output stage and its LC LPF

In one time period, MHa and MLb turn on at the same time while the other two are in off state, current flows from Vdd to Vss and delivers power to the speaker. In another time period, MHb and MLa turn on to deliver power.

The full H bridge consists of two half bridge. Hence more components are needed to construct this circuit and its LPF. Although the cost to build full H bridge is higher, it is still much more popular than half bridge due to its superior audio performance:

- First of all, unlike single ended version, full bridge does not suffer from supply voltage pumping effect. This is because the inductor current flowing into one of the half bridge flows out from the other one due to the complementary switching operation of these two half bridge. Therefore, no energy is pumped back into the power supply. Since the gain of class D amplifier is directly proportional to the supply bus voltage, reducing fluctuation in supply voltage implies less distortion introduced in the output signal. The following diagram shows how full H bridge is immune to supply voltage pumping effect:

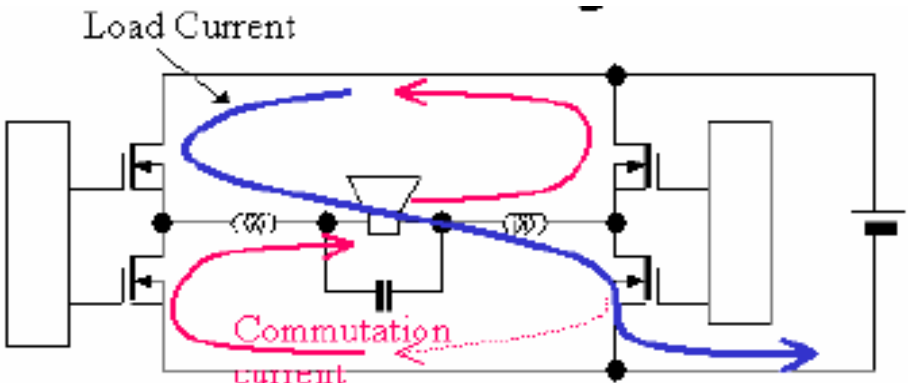

Fig3.7: Local current loop to prevent pumping effect

- Due to the differential operation, full H bridge topology inherently eliminates even orders harmonic distortion as well as harmful dc biasing offset [Axh07]. Hence, full H bridge usually runs with single power supply without the dc blocking capacitor.

- With the same power supply voltage, the output signal swing of full H bridge topology is two times compares to the single ended implementation. Since power=V^2, the full bridge structure is able to deliver four times output power of half bridge, which is especially valuable in low voltage design [Axh07].

- Another important feature of full H bridge is that 3 level switching operation can be implemented. This switching scheme effectively reduces the differential EMI and the switching activity of the output power transistors.

Since three levels switching operation is one of the most important of this class D amplifier design, full H bridge output stage topology is adopted in this design project.

3.3.3 Dead time and distortion

The purpose of introducing dead time for output stage control signal is to prevent both PMOS and NMOS of the output power transistors turn on during the transition period. Due to power efficiency requirement, the power transistors have low resistance in order to reduce conduction loss. Simultaneously turning on high side and low side power transistors create a low impedance path that shorts Vdd and Vss directly. This introduces a very large short circuit current which adds on to power loss, and more importantly, the reliability issue on output stage.

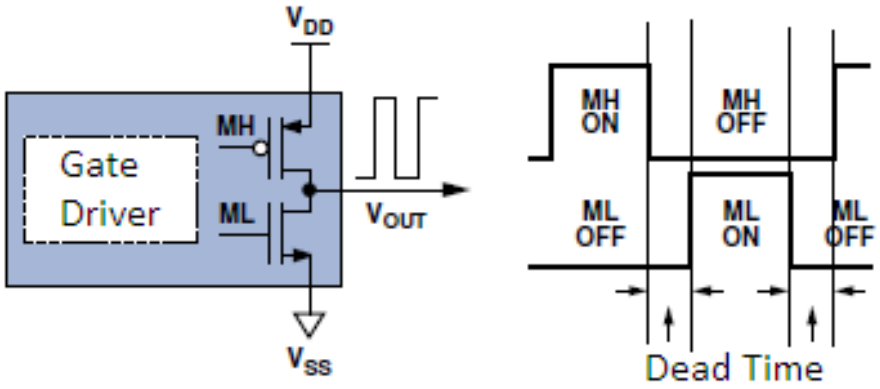

Fig3.8: Dead time of output control signal

The above figure shows how dead time, or non-overlapping time, works on the output stage. During the dead time period, both MH and ML are turned off. This operation ensures that one switch starts to turn on only after the other one has been completely turned off. Therefore, there is no low impedance path between Vdd and Vss at any time so that no shoot through current is formed. The voltage across the load depends on the direction and magnitude of the load current during the dead time period [Mos99].

Although the dead time of switching control helps to improve the power efficiency of the amplifier and addresses reliability issue, it also introduces switching timing error in gate control signal at the same time. Since this timing error is the main cause of the nonlinearity, dead time has significant contribution to the distortion of class D amplifier [Mos99]. Next figure shows the mechanism of timing error induced by the dead time. The diodes in this figure are body diodes of the output power transistors. The blue line shows the load current path during conduction period while the red line shows the load current path during the dead time period.

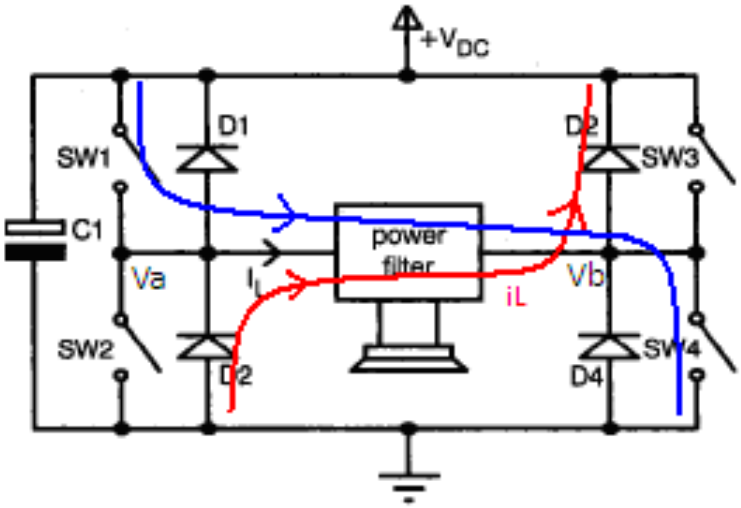

Fig3.9: Current flow in full H bridge

The operation of full H bridge can be categorized into two regions: the single directional output current operation region and bidirectional output current operation region. When the output current is larger than the LPF inductor ripple current, the output current flows in single direction within one whole period and it is in single directional output current operation region. When the output current is smaller than the inductor ripple current, the output current flows in positive direction in on-time period and it flows in negative direction in off-time period. The full bridge is in bidirectional output current operation region.

During the conduction period of positive single directional output current operation region, SW1 and SW4 turn on. The left side full bridge output Va is at high voltage level. Load current flows from Vdd to ground through SW1 and SW4. Since

the output current is larger than the inductor ripple current, it is still flowing in the same direction during the dead time period due to the inductor of LPF. The output current flows from ground to Vdd through the body diodes of SW2 and SW3 as all switches are turned off in this particular period. D2 and D3 conduct and so that node Va is connected to ground. Hence, Va is low during dead time. In another word, the voltage level of left half bridge output node goes low at the instant when SW1 is turned off. In summary, for positive single directional output current operation region, the output voltage only follows the SW1 switching signal from the gate driving stage. Since on-time from modulator is equal to on-time + dead time from gate driver, the on-time of H bridge is shortened by one dead time compare to the correct on-time from modulator. This timing error lowers the gain of class D amplifier. The situation is the same for negative direction output current operation region.

In the bidirectional output current operation region, since the load current is lower than the inductor ripple current, the output current of H bridge returns to zero during the dead time. All the switches and body diodes are in off mode and so that the output node of H bridge is floating and Va is undetermined in this particular period. For simplicity, we can consider that the Va in dead time has the same voltage level before the dead time. In this case, at the instant when SW1 is turned off, node Va is floating

and it is in high voltage level since Va is high before SW1 turned off. Therefore, the on-time of the H bridge is on-time of SW1 from gate signal plus the dead time, which is the same as the correct on-time from the modulator. In summary, dead time does not add timing error in bidirectional output current operation region and hence, no variation in the gain of class D amplifier.

Since the output current magnitude is dependent on the audio input signal, operation region of the full bridge output is changing from time to time. As the gain is different for each operation region, the output waveform will be distorted. The gain error is directly proportional to the timing error introduced by the gate driving stage, reducing the dead time decreases the timing error so that the distortion decreases at the same time. Therefore, the dead time should be minimized in order to get good sound quality.

3.4 Three level switching scheme for SDM

1 bit quantizer is widely used in SD modulator design due to the simplicity and linearity. It uses 1 bit digital to analog converter (DAC) to implement the feedback. Since the nonlinearity of DAC directly add to the input, and this nonlinearity is not able to be suppressed by the loop filter, the nonlinearity of DAC introduces distortion to the output signal without attenuation. Therefore, the linearity of feedback DAC is very important in SD modulator design. Single bit quantization SD modulator is inherently linear as it only has two output levels and two points define a straight line, and hence it is widely used in design.

However, from figure 3.3, we can notice an interesting phenomenon for 1-bit sigma-delta modulator is that the output switching activity is very high when the input amplitude is small. This is due to the high quantization noise of single bit SD modulator, which makes the output switching frequently between state 1 and state -1 so that its average value is small. This degrades the power efficiency of the class D amplifier for low output power due to high switching loss. Furthermore, because of fully differential switching operation of each half bridge, there is always a conduction current flowing in the output stage. Figure 3.10 in the next page shows the voltage at the output nodes, Va and Vb, of each half bridge and the conduction current flowing

into the load. Va and Vb are always in complementary and only two differential operating states exist, which means current is always flowing between this two nodes. Output current is positive at state 1, while it is negative at state -1. This continuous conduction current induced conduction loss of full bridge output and therefore further degrades the power efficiency.

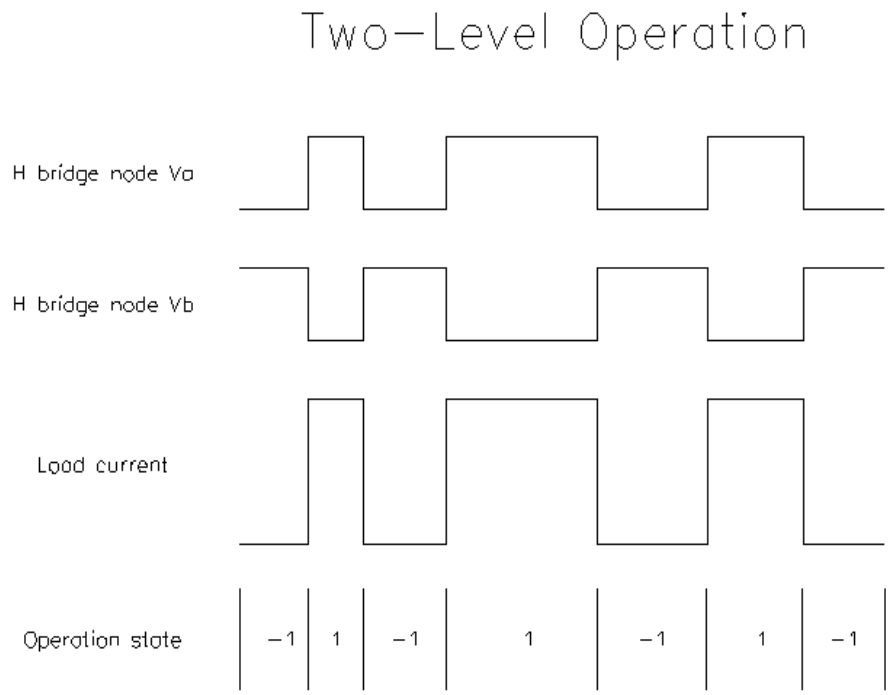

Fig3.10: H-bridge output voltage and load current of 1-bit SD modulator

In this design, 1.5 bit quantization SD modulator is adopted and three-level switching scheme is used. Compare to conventional binary switching operation which only processes state 1 and state -1, three-level switching scheme brings in one more state: the state 0. At state 1 and -1, two half bridge outputs Va and Vb are opposite,

while at state 0, two half bridge outputs have the same polarity, either both are at Vdd or both are at ground. This common mode state is used in conjunction with two differential states to produce three-state modulation. The differential input to the LPF of the output stage is positive, zero and negative in three different states. The output voltage of each half bridge and the output current are shown in figure 3.11. At state 0, the output stage current is zero since both Va and Vb are at voltage low. Instead of keep providing current to the load in binary switching scheme, the full H bridge only provides current to the load when it is needed. This greatly reduces the conduction loss due to the imperfect switches.

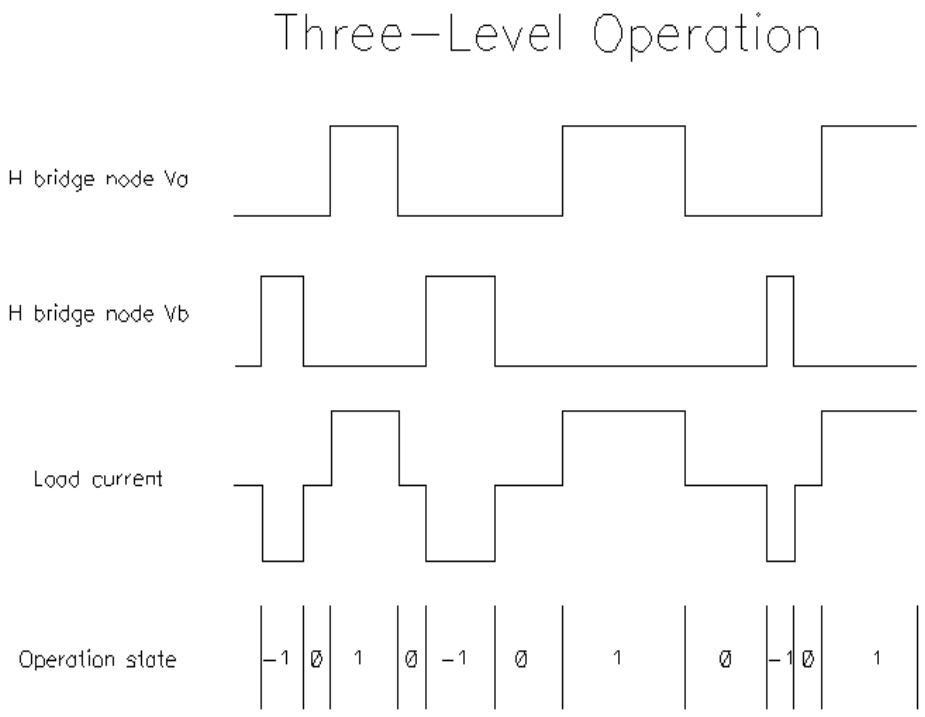

Fig3.11: H-bridge output voltage and load current of 1.5-bit SD modulator

One more advantage of 1.5 bit quantization is that instead of switching frequently between state 1 and state -1 to deliver low output power, the 1.5 bit quantization modulator outputs higher density of state 0 to represent low output power. This prevents high switching activity for low input amplitude and further improves the power efficiency of the amplifier. Figure 3.12 shows the normalized switching activity of the 1 bit SD modulator and 1.5 bit SD modulator with different output power simulated in MatLab:

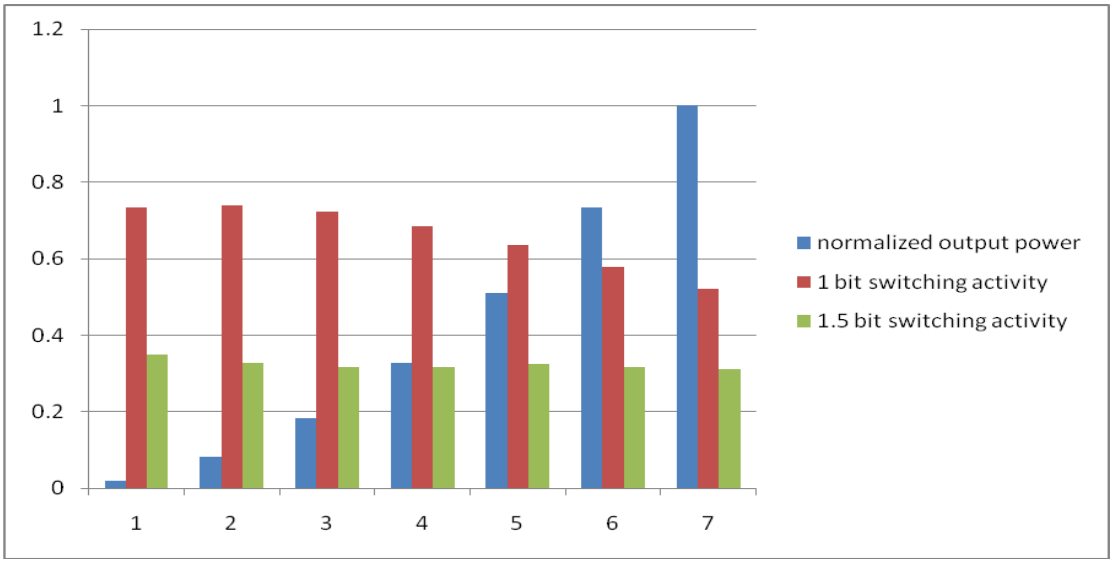

Fig3.12 Normalized switching activity of 1 bit and 1.5 bit SD modulator at different output power

It is obvious that the switching activity of the full H bridge driven by 1.5 bit SD modulator is lower than the one driven by 1 bit SD modulator, especially when the output power is small. Decrease in differential switching also helps to reduce differential EMI.

3.5 PSRR and Feedback Topology

One of the major drawbacks of class D power amplifier is the poor Power Supply Rejection Ratio (PSRR) [Put03]. Since the output stage is a full H bridge or a half bridge for class D amplifier, the output transistors connecting the power supplies to the LPF which is a very low impedance path. The fluctuation in power supplies bus is directly coupled to the load with very little attenuation. Hence, there is almost no rejection for the power supply noise for the open loop class D amplifier and the PSRR is very low [Put03]. This means a very stable and clean power supply is required to drive the open loop class D amplifier. Furthermore, since the gain of class D amplifier is directly proportional to the bus voltage, variation in bus voltage change the gain of the amplifier which results in distortion at the output. This further degrades the performance of class D amplifier. Figure 3.13 depicts the simplest linear model for an open loop class D amplifier:

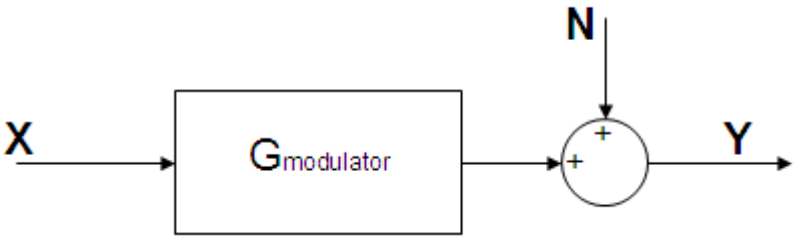

Fig3.13: Linear model for open loop class D amplifier

Where X is the input, Y is the output and N is only considering the power supply noise. The power supply noise transfer function is unity which implies 0 dB PSRR. Although the LPF is able to reject the supply noise outside the signal band, all the noise within audio frequency is passed through and affects the sound quality.

One way to address this issue is to use feedback with high loop gain. This helps to improve PSRR of the amplifier greatly. Besides that, it also attenuates the distortion caused by the bus voltage variation. With this negative feedback, the voltage fluctuation in power supplies is suppressed by the loop filter. Figure 3.14 shows the linear model with feedback.

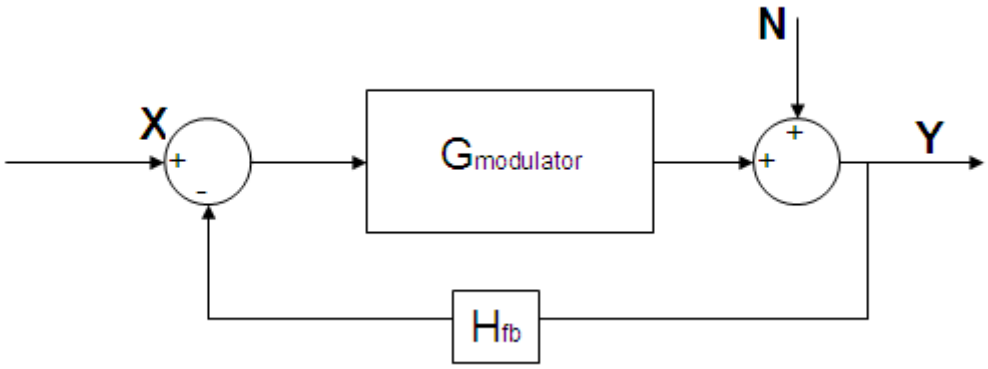

Fig3.14: Linear model for class D amplifier with feedback

Consider N as the power supplies noise, the noise transfer function is:

$$H_N = \frac{1}{G_{modulator} \cdot H_{fb} + 1} \qquad \text{(Equation 3.1)}$$

We can see that the supplies noise is suppressed by the loop gain of the filter. If the loop gain is very large within the audio band, which is the case in SD modulator class D amplifier, the noise will be attenuated greatly. Hence, the PSRR of the amplifier is improved.

SD modulator is used in this design. It is a feedback system which suppresses the quantization noise. If we adjust the feedback loop so that to include the power supplies noise, the PSRR of the whole system will be improved a lot. This concept is illustrated in figure 3.15(a) and 3.15(b).

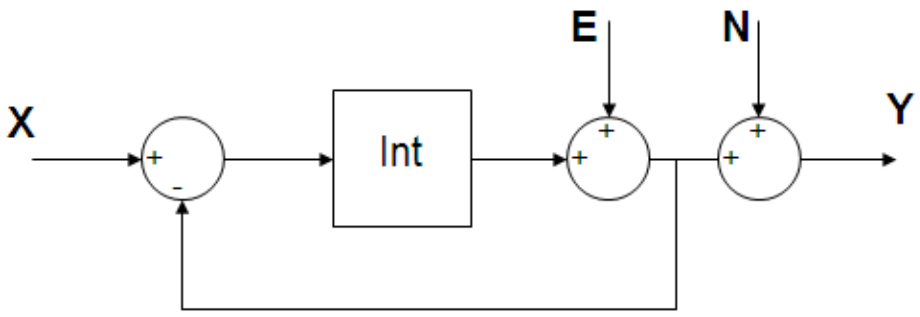

Fig3.15(a): Model of SDM class D amplifier with feedback from quantizer

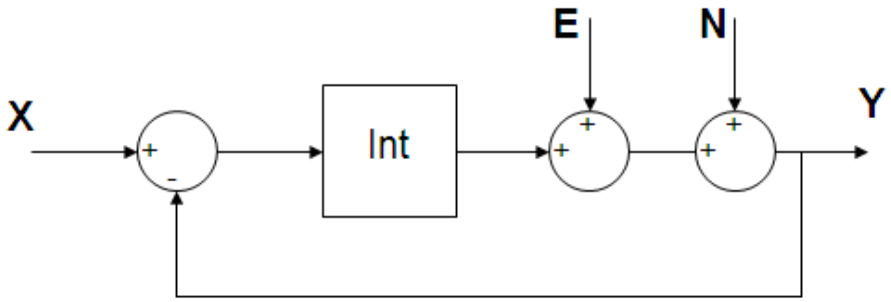

Fig3.15(b): Model of SDM class D amplifier with feedback from H bridge

E is the quantization noise and N is the power supplies noise. By shifting the feedback point from quantizer of SD modulator to the H bridge output of class D amplifier can include both the quantization noise and power supplies noise. This feedback topology guarantees the design to be able to achieve high PSRR.

3.6 Overall architectural design

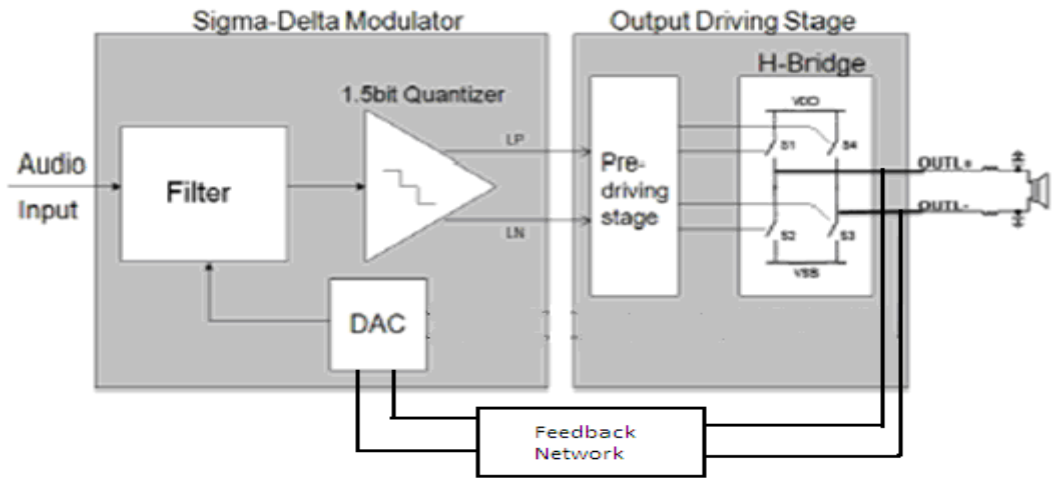

Fig3.16: Block diagram of proposed class D amplifier

Figure 3.16 depicts the proposed overall architectural design for this class D amplifier. Those blocks in gray areas are the on-chip components. A 1.5 bit SD modulator is used in this design to reduce the switching loss and conduction loss. A full H-bridge output stage helps to deliver more power and to eliminate the 2nd order harmonic distortion. The output of full H-bridge is fed back directly to the input of the modulator to improve PSRR of the class D amplifier. A zero-dead-time gate driving circuit is used in this design to minimize the distortion introduced by timing error. The gate driving circuit is designed in a way that the transition time for the gate control signal is very short to minimize the short circuit conduction loss. Due to low cut-off frequency, the lossless LC LPF is not able to be integrated onto the chip and it is built on the testing PCB.

Chapter 4:
Sigma-Delta Modulator Design

Signal modulator is the most important building block for a class D power amplifier. Pulse width modulation scheme and sigma-delta modulation scheme are commonly used for the signal modulator design. In this design, a three-level-quantization SD modulation scheme is chosen. The oversampling and noise shaping features of SD modulator helps to improve performance of class D amplifier.

The design details of the SD modulator for this project are discussed in this chapter. It consists of three major parts. In the first part, the basic principle of SD modulation is introduced and its main features are discussed. In the second part, the system level design of the SD modulator is cover. The system parameters and the architecture of the SD modulator are determined in this part. The system level design is mainly done by doing behavioural simulation in MatLab. The circuit implementation of the SD modulator and the transistor-level design of its building blocks are covered in the last part.

4.1 Basis of Sigma-Delta Modulator

Before going into the detail discussion of SD modulator design, a brief introduction on conventional SD modulation is given for better understanding.

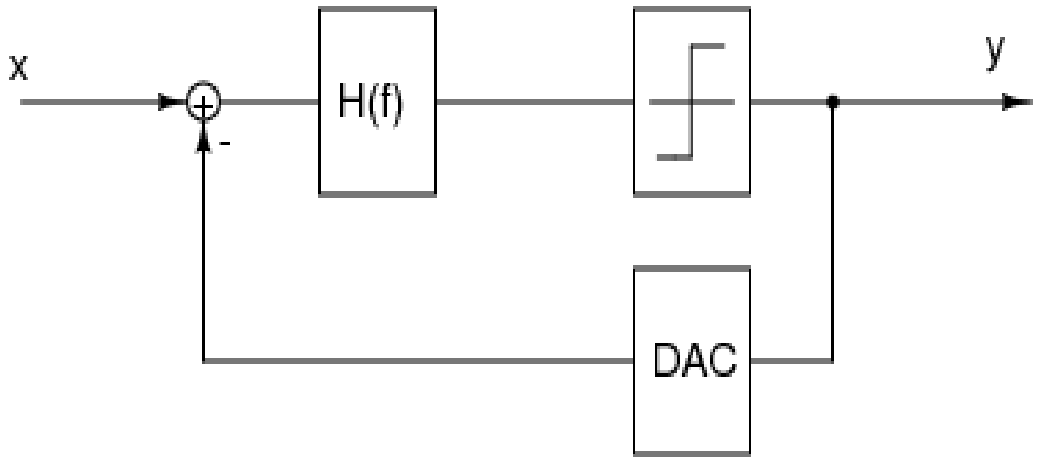

Fig 4.1: Structure of simplest single loop 1st order SD modulatorf

Figure 4.1 shows the simplest conventional sigma-delta modulator. It is configured as a closed loop using negative feedback, and has the noise-shaping property that removes the nonlinear components within the signal band [Kyo08]. The analog input, X, is fed to an integrator, and the output of the integrator is fed to a quantizer (A/D converter). The output of the modulator, Y, is converted back to analog signal by DAC and subtracted from the analog input. This feedback forces the

output of modulator, Y, tracks closely to the analog input signal, X, and so that the average value of the quantized signal is equal to the average value of input signal.

In order to study how the SD modulator process signal and noise, the linear model for conventional 1st order SD modulator needs to be built. The tricky part on building up this linear model is the existence of quantizer, which is a non-linear element. Since the output bitstream of the modulator contains the average input value, this bitstream can be seen as the combination of input and large magnitude noise. Therefore, the quantizer can be modelled as a signal source which adds noise to the input. Here is the linear model for the conventional 1st order SD modulator.

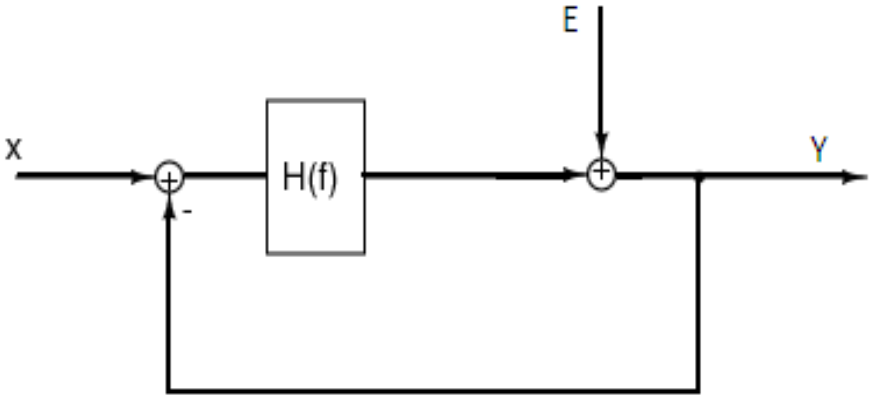

Fig 4.2: Noise Injection model for 1st order conventional SD modulator

The signal transfer function and noise transfer function for this conventional sigma-delta modulator are shown below:

Signal transfer function: $S_{(f)} = \frac{H_{(f)}}{1 + H_{(f)}}$ (Equation 4.1)

Noise transfer function: $N_{(f)} = \frac{1}{1 + H_{(f)}}$ (Equation 4.2)

If H(f) is chosen to have high magnitude within the signal band, it is clear that S(f) becomes close to unity while N(f) become very small within band of interest. The SD modulator can be seen as a band pass filter for signal X and band stop filter for noise E. However, the noise outside the signal band is not reduced by the feedback system as the loop gain outside the signal band is small. For class D amplifier application, the out-of-band noise can be filter out by the LPF at the output stage.

This is the noise shaping feature of sigma-delta modulation. It can reduce the in band noise and hence, improve the SNR in the signal band. The following figure illustrates this concept.

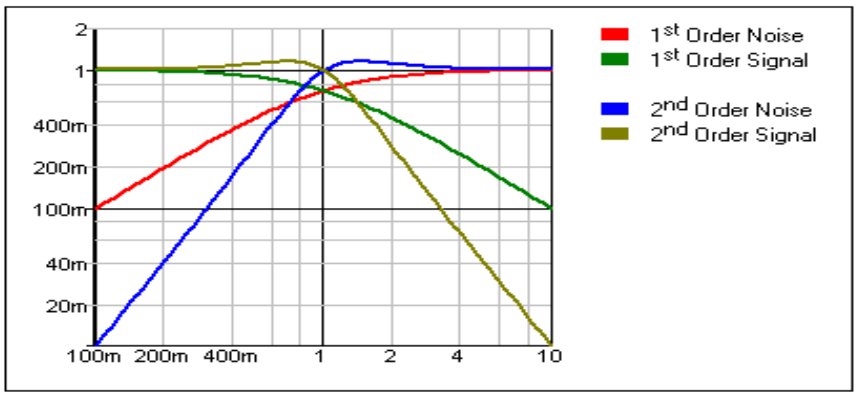

Fig 4.3: Frequency response of SD modulator due to Noise shaping

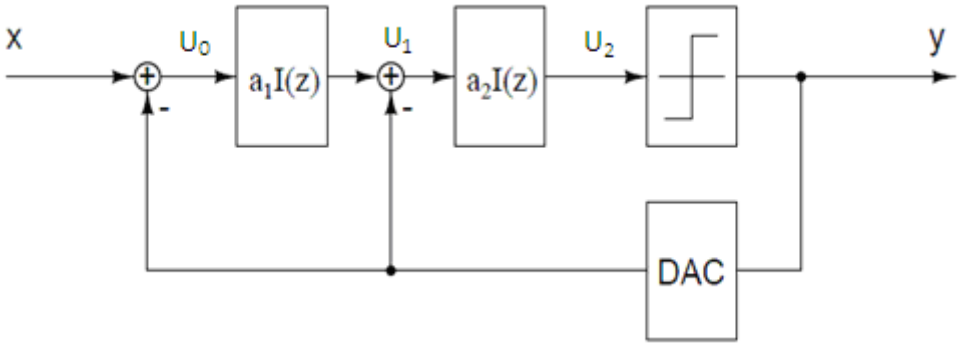

Fig 4.4: Conventional 2nd order single loop SD modulator

The 2nd order SD modulator contains two integrators inside the loop. The noise shaping is more aggressive if the orders of the loop filter increase. As we can see from figure 4.3, the 2nd order loop has steeper slop at the low frequency. This implies that the 2nd order loop have better noise rejection ability and so that its output has higher SNR than the one produced by 1st order loop filter.

Another important feature of sigma-delta modulator is oversampling. In order to prevent anti-aliasing, signal is usually sampled in its Nyquist rate. If the sampling rate is higher than the signal's Nyquist rate, it is called oversampling. If the maximum signal bandwidth is f_o and the sampling rate is f_s, the oversampling ratio can be calculated by:

$$OSR = f_s \big/ 2 f_o \qquad \text{(Equation 4.3)}$$

The advantage of oversampling is that it uniformly distributes the quantization noise across fs rather than fo. This reduces the quantization noise level according to the OSR. The plot below explains this concept:

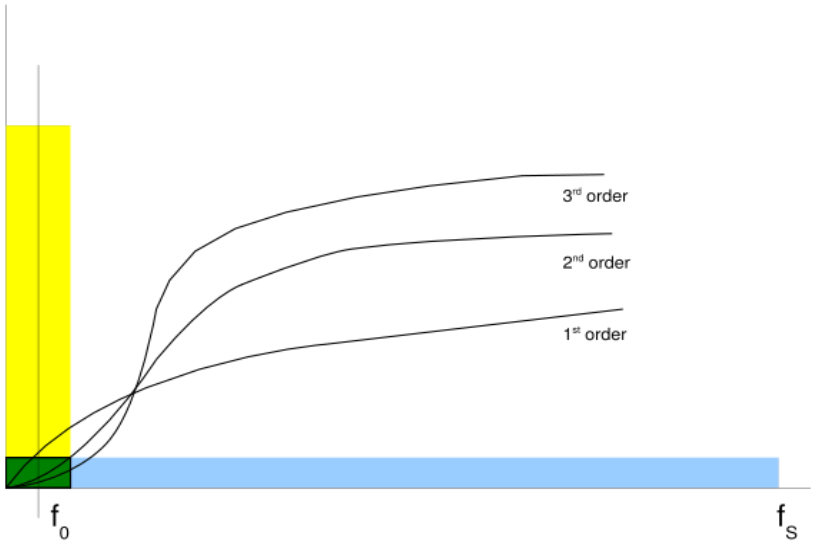

Fig 4.5: Quantization noise in Nyquist rate sampling and oversampling

The total quantization noise is the same for both in a Nyquist converter (in yellow) and in an oversampling converter (in blue), but it is distributed over a larger spectrum. The quantization noise level for the oversampling converter is 1/OSR of the quantization noise level for the Nyquist converter. Therefore, the higher the oversampling ratio, the better the SNR performance. The curves in figure 4.5 shows the noise shaping ability of 1st , 2nd and 3rd order SD modulator respectively.

4.2 Sigma-Delta Modulator System Level Design

System level design is important science optimization in block level help to relax the constrains in circuit level design. In this section, system level issues are covered, includes SD modulator topology selection, stability issue and system level parameters optimization. Besides that, a novel SD modulator topology is introduced and its advantages over conventional topology are discussed in this section.

4.2.1 System level Design parameters

In this section, the major design parameters in system level are briefly introduced and the design strategy is also discussed.

4.2.1.1 Modulator architecture

Generally speaking there are two types of SD modulator architectures: single loop SD modulators and cascaded SD modulators.

As the name stated, the single loop architecture consists of only one single SD loop in the modulator. It is the simpler and easier-to-build architecture since the building blocks requirement is relaxed comparing to cascaded architecture, especially

the gain of the OTAs. The major drawbacks of single loop architecture are its weaker noise shaping ability and its instability. A high order single loop SD modulator tends to suffer from oscillation when the input signal level is large.

The cascaded architecture consists of cascading several single loop SD modulators. Fig 4.6 shows an example of a 4^{th} order cascaded SD topology. Theoretically, orders of single loop SD modulator used for cascading is not restricted. However, low order of SD modulator is used in each cascade stage in practice for stability purpose. The main advantages of cascaded architecture are the high linearity and good stability. With proper design, a cascaded SD modulator can have high order loop filter yet remains stable. Therefore, it can achieve higher SNR than single loop architecture. However, due to noise leakage problem of cascaded architecture, requirement of the building blocks is very high. Since finite OTA dc gain, settling error of integrator and mismatch of loop coefficient are the main causes of noise leakage, very high OTA dc gain is require.

Since the cascaded architecture is highly sensitive to the nonlinearity of building blocks, its implementation is very difficult. And hence, the single loop architecture is adopted in this design project.

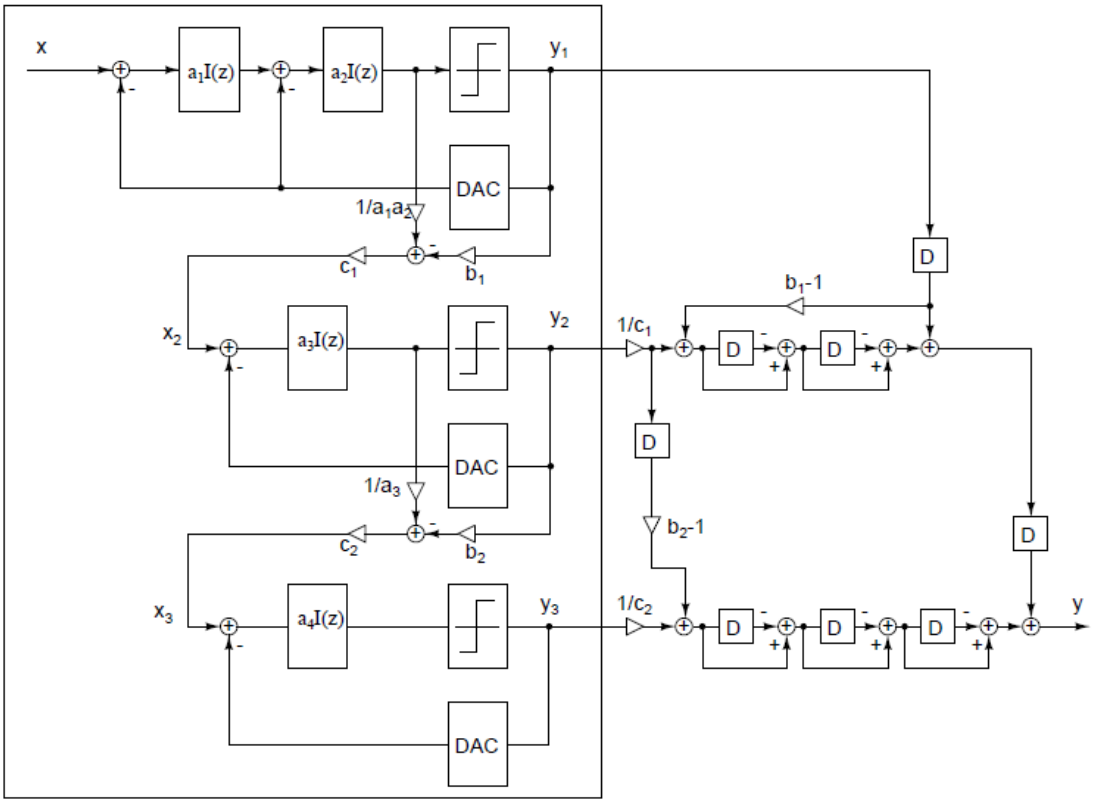

Fig 4.6: A 4th order cascaded 2-1-1 SD modulator [Yao05]

4.2.1.2 Oversampling ratio

Section4.1 shows that higher oversampling ratio (OSR) results in lower quantization noise level. SNR of a SD modulator can be increased by using higher OSR. For a Nth order SD modulator, doubling of OSR results in (0.5+N) bit increase in SNR. Unfortunately, speed limitation of circuit implementation does not allow OSR going too high. In practice, lower OSR is preferred to achieve the same

modulator performance. This is because reducing OSR helps to relax the speed requirement of the circuit and helps to decrease the switching activity of class D amplifier output stage.

4.2.1.3 Loop coefficient

The stability issue of single loop SD modulator which is greater then 2nd order is addressed by the loop coefficient of the loop filter. Increase in loop coefficient results in more aggressive noise shaping and hence, better SNR in signal band. However, large loop coefficient make the loop filter become more prone to instability. Therefore, there is a trade-off between the linearity performance and stability when choosing the loop coefficient. A balance between SNR and stability is needed for the optimization of loop coefficient.

4.2.1.4 Order of loop filter

Order of loop filter can be increased by inserting integrator into the forward path of the loop. As shown in Fig 4.5, noise shaping ability increases when the order of

loop filter is getting higher. Hence, higher order loop filter helps SD modulator to get better SNR performance. However, the stability becomes the major concern for high order single loop SD modulator. The loop coefficient should be reduced to maintain the stability of the modulator when the order of loop filter increases. Since SNR performance decreases when the loop coefficient reduced, further increase in the order will not gain much increase in SNR if the order of the loop filter is already high. In summary, the SNR performance of a single loop SD modulator is limited by the stability requirement. In practice, the loop filter of SD modulator is usually 3^{rd} order to 5^{th} order.

4.2.1.5 Number of bit for quantizer

Single bit quantizer is very popular in the SD modulator design because of the intrinsic linearity of single bit DAC in the feedback path. Nevertheless, the amplitude of quantization noise is large due to single bit quantization. This results in some problems like low SNR, high internal signal swing and more prone to instability comparing to the one using multi-bit quantizer.

By employing multi-bit quantizer, the SD modulator can have better loop stability due to its lower amplitude of quantization noise. Therefore, the order of loop filter can be increased and larger loop coefficient can be used. As a result, the SNR performance of multi-bit quantization SD modulator is superior than single-bit quantization SD modulator provided the linearity of multi-bit DAC in the feedback path is very high. However, designing a highly linear multi-bit DAC is not an easy task. Although there are many linearization techniques for DAC design, they have some drawbacks and greatly increase the complexity of design. More importantly, since the multi-bit DAC is at the feedback path, its nonlinearity can not be suppressed by the loop filter but just added to the output directly.

In this project, a 1.5-bit quantizer is adopted for the SD modulator design as the three-level-switching scheme is used for the full H-bridge output stage.

4.2.2 Stability analysis of single loop SD modulator

Since SD modulator is a feedback system, stability issue is one of the potential problems that need to be addressed in system level design. In previous analysis, we know that increasing the order of the loop filter can enhance the noise shaping ability and so that the modulator can achieve higher in band SNR. However, the single loop SD modulator structure is prone to instability if the order of the loop filter is greater than two [Can85]. And the modulator tends to be more unstable if the order of the loop filter increase.

In order to analyse the stability of the SD modulator, an appropriate linear model needs to be built. It is not an easy task as SD modulator is a highly nonlinear system due to the existence of quantizer. The noise injection linear model used in section 4.1 models the quantizer by a linearized gain stage with an additive noise source to represent the distortion component introduce by the quantizer. Although this linear model can predict the noise shaping of the modulator, it provides insufficient information to analyze the stability of SD modulator. Therefore, a more versatile model needs to be used for the stability analysis.

In this chapter, the variable gain linear model is employed for stability analysis. In this model, the nonlinear quantizer is modelled as a linear gain stage with arbitrary gain value which is depending on the input and output value of the quantizer [Bai94].

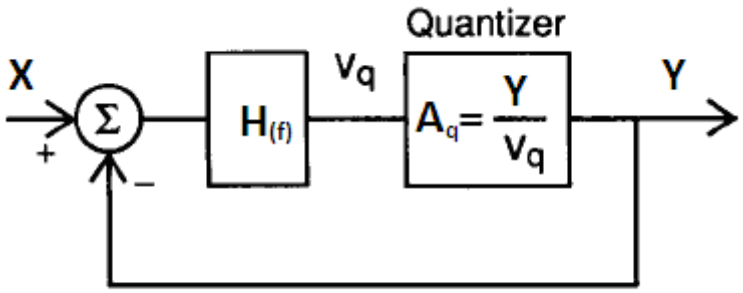

Fig 4.7: Variable gain linear model for SD modulator

Fig 4.7 shows the variable gain linear model. Vq and Y are the input and output of quantizer respectively. Aq is the variable quantizer gain which solely depends on the instantaneous value of Y and Vq. Since the quantizer output Y only has two voltage levels: voltage high or voltage low, Aq is small if the amplitude of Vq is large, and vice versa. Modelling the quantizer in this way allows root locus techniques to be applies in investigating system stability. The root moves along the locus as the linearized quantizer gain change. If the gain falls into the locus segment that is outside the unit cycle, the system becomes unstable. As a result, signal input level tends to be large due to feedback. The transfer function of variable gain model is:

$$\frac{Y_{(s)}}{X_{(s)}} = \frac{A_q \bullet H_{(s)}}{1 + A_q \bullet H_{(s)}} \qquad \text{(Equation 4.4)}$$

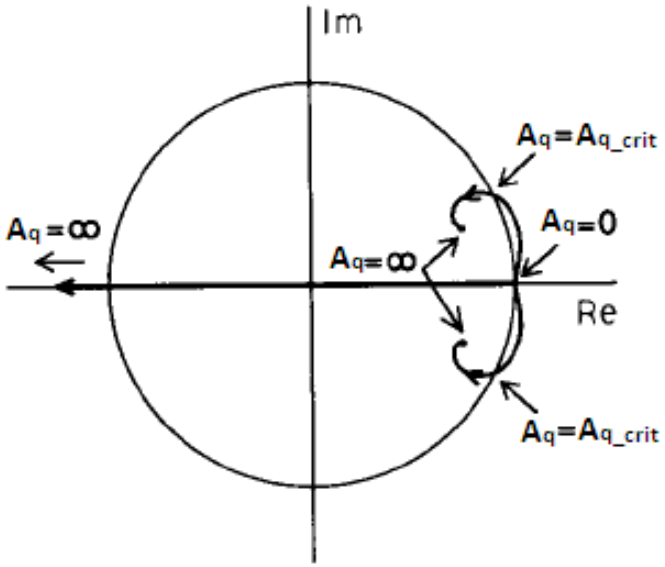

Fig 4.8: Root locus of the poles for 3rd order conventional SD modulator

Fig 4.8 shows the root locus for 3rd order modulator with loop coefficient [0.25 0.5 1] [Bai94]. The poles of the system move due to the quantizer gain Aq. There are two locus need to be analysis separately. For the one along Real axis, the pole of system goes outside the unit cycle when Aq goes to infinity. That means the system becomes unstable and the signal level in the modulator will increase. As the quantizer input level increases, Aq will decrease. This will drift this pole back within the unit cycle and the system stability is restored. Therefore, the system is stable if the quantizer gain is very large.

For the 2nd locus, this pair of complex poles are within the unit cycle when the quantizer gain is very large. However, as Aq decrease to a critical point, Aq_crit, the poles move outside the unit cycle. The system becomes unstable and the quantizer input level is getting larger and larger. The increase in quantizer input further reduces the quantizer gain, and the roots move along the locus outside the unit cycle instead of moving back inside. Hence, if the quantizer gain is smaller than Aq_crit, the system becomes unstable. In another word, the modulator becomes unstable when the quantizer input level is very large.

This stability analysis gives insight that how to make SD modulator stable. Generally speaking, the system becomes unstable if the internal signal level becomes too large. Another thing to mention here is that if the loop coefficient decrease or the integrator delay reduces, the value of Aq_crit also reduces. This implies the loop filter can accommodate larger internal signal and thus the modulator becomes more stable.

4.2.3 Fully feed-forward topology

Feed forward is another type of control system comparing to feedback. Feed forward control is an open loop system which applies the compensation control signal directly to the controller before error appears. Hence, it controls the system before the output making error. However, the compensation control signal of a feedback loop is based on error signal, which means feedback loop controls the system after making error. Therefore, feed forward control is much faster than the feedback control. Nevertheless, due to the "open loop" nature of feed forward control, it is not able to tell if the output produces error. This is the major drawback of feed forward control. To overcome this problem, feedforward-feedback combination control system is developed. The feed forward path helps system to react fast while the feedback loop can correct the residual error which is not compensated by the feed forward control.

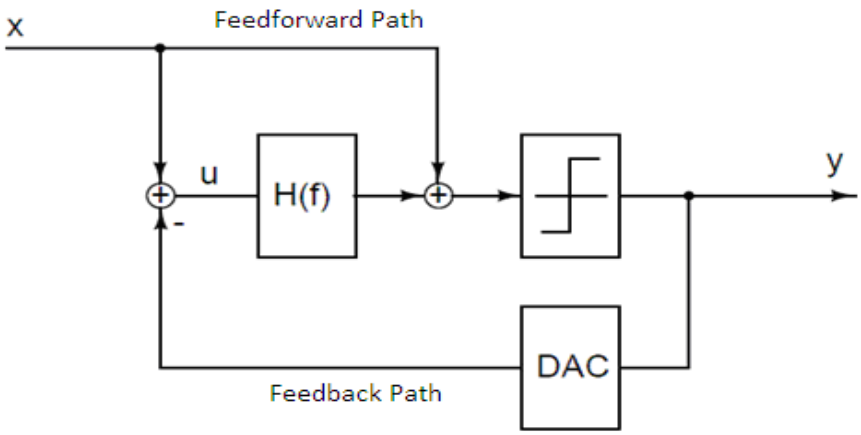

Fig 4.9: 1st order single loop fully feed forward SD modulator

Figure 4.6 shows a 1st order single loop fully feed forward SD modulator. It is a feedforward-feedback combination control system. The feed forward topology has the main advantages of conventional SD modulator: oversampling and noise shaping. It has some unique characteristics. Equation 4.5 and 4.6 are the signal transfer function and noise transfer function for this single loop feed forward SD modulator:

$$\text{Signal transfer function: } S_{(f)} = 1 \qquad \text{(Equation 4.5)}$$

$$\text{Noise transfer function: } N_{(f)} = \frac{1}{1 + H_{(f)}} \qquad \text{(Equation 4.6)}$$

The noise transfer function of fully feed forward topology is identical to that of conventional SD modulator, which implies that it has the same noise shaping ability as the conventional structure. More interestingly, the signal transfer function for the feed forward SD modulator is unity. It does not contain any terms related with H(f). This unity signal transfer function means that the non-linearity of the building blocks will not contaminate the input signal [Kyo08]. Therefore, the harmonic distortion introduced by the non-linearity of the loop filter is significantly reduced comparing to conventional SD modulator.

This unity signal transfer function feature is attractive in design. Since the effect of nonlinearity of the building blocks in feed forward is not as significant as in conventional topology, the design requirements for each building block is relaxed [Sil01][Gha06]. This means lower OTA gain can be used in design which makes design much easer.

Another major different between fully feed forward topology and conventional topology SD modulator is the input signal of the loop filter, U. Although the input signal of the loop filter is different between the modulator input and modulator output feedback signal for both feed forward topology and conventional topology, the signal contain of U is different for these two topologies due to the delay of the integrators in the loop filter. For the conventional SD modulator, the modulator input signal, X, needs to go through the integrators in the loop filter to reach the quantizer. Due to the integrators delay, the modulator output, Y, is the delayed version of the modulator input, X. For example, the Fig. 4.4 shows a conventional 2nd order SD modulator. The signal U2 at the quantizer input has two integrators delay comparing to X. According to the signal and noise transfer function of conventional SD modulator in Equation 4.1 and Equation 4.2, the quantizer input can be written as:

$$U_{(f)} = X_{(f)} - Y_{(f)} \quad \text{and} \quad Y_{(f)} = S_{(f)} \bullet X_{(f)} + E_{(f)} \bullet N_{(f)}$$

$$U_{(f)} = (1 - S_{(f)}) \bullet X_{(f)} - N_{(f)} \bullet E_{(f)}$$

$$U_{(f)} = \frac{1}{1 + H_{(f)}} \bullet X_{(f)} - N_{(f)} \bullet E_{(f)} \qquad \text{(Equation 4.7)}$$

Equation 4.7 clearly shows that the input signal of loop filter contains both the quantization error and the high pass version of the modulation input signal, X. This high pass version of X is restored to its full amplitude by the integrators in the loop [Sil01], which makes the internal signal swings in the loop filter to be high. This high internal signal swing reduces the overload level of the modulator and makes the modulator more susceptible to instability.

For the fully feed forward topology, due to the existence of feed forward path, the modulator input signal, X, is brought to quantizer input directly instead of passing through the integrators. Therefore, the output signal, Y, has no delay [Sil01]. Hence, the input and output of the modulator can cancel out at the input of loop filter. There is no high pass version of X in the error signal U.

The following paragraph derives the input signal of the loop filter, U, for fully feed forward SD modulator.

$$Y_{(f)} = S_{(f)} \bullet X_{(f)} + E_{(f)} \bullet N_{(f)} \quad \text{and} \quad S_{(f)} = 1$$

$$Y_{(f)} = X_{(f)} + E_{(f)} \bullet N_{(f)}$$

$$U_{(f)} = X_{(f)} - Y_{(f)} = -E_{(f)} \bullet N_{(f)} \qquad \text{(Equation 4.8)}$$

(Equation 4.8) demonstrates that due to the unity signal transfer function, the input signal of the loop filter, U, only contains quantization error. Therefore, the loop filter only processes the quantization noise, which is much smaller in amplitude comparing to the modulation input signal. This features helps to reduce the internal signal swing of the loop filter, which implies that the harmonic distortion generated inside the loop filter can be reduce. Smaller internal signal swing relaxed the output swing requirements of the integrators, which makes the design of building blocks much easier. Besides that, since the loop filter input signal, U, does not contain the modulator input, X, the signal X does not pass through the loop filter and so that the signal X will not be distorted by the nonlinearity of the building blocks in the loop filter.

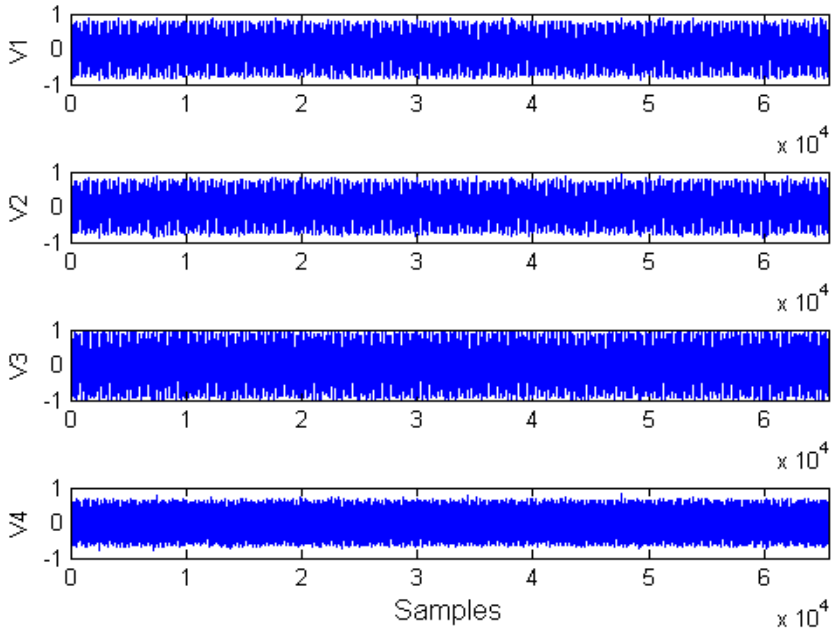

Fig 4.10a: Integrators output of 4th order conventional SD modulator

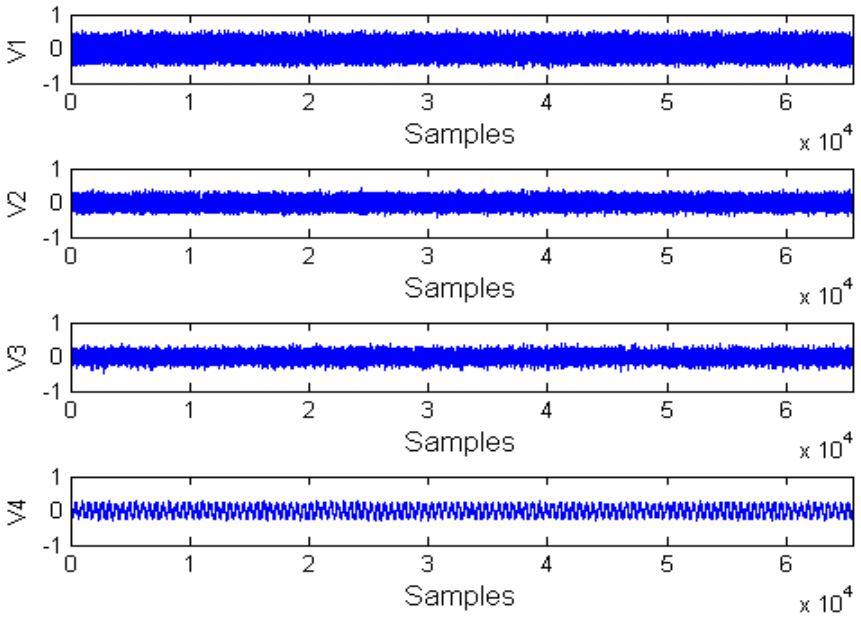

Fig 4.10b: Integrators output of 4th order fully feed forward SD modulator

The behavioural simulations of integrators output swing in MatLab are shown in Fig 4.10a and Fig 4.10b. V1, V2, V3, V4 represent the output signals of 1st to 4th integrator respectively. These two plots verify that the internal swing of fully feed forward topology is smaller than that of conventional topology with same number of bit of quantization. Furthermore, since there is no delay between the input X and output Y of the fully feed forward topology SD modulator, according to the analysis in section 4.2.2, it is more stable than the SD modulator using conventional topology.

The order of fully feed forward SD modulator can be increased by adding integrator and feed forward path into the loop filter. Fig 4.11 shows the block diagram of a 3rd order fully feed forward SD modulator. Each integrator output in the loop filter is fed forward directly to the quantizer by the feed forward coefficient [c].

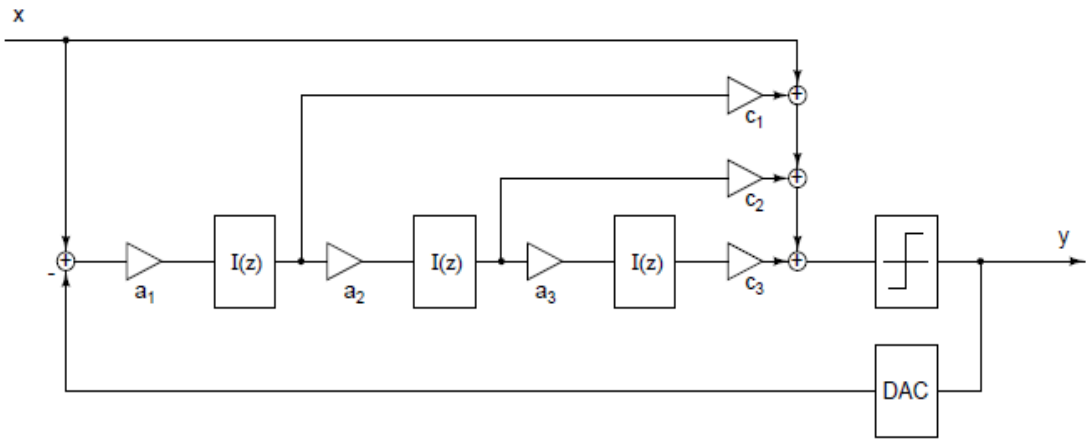

Fig 4.11: A 3rd order fully feed forward SD modulator

4.2.4 System parameters optimization

System parameters including OTA gain, value of loop coefficient, OSR and etc will be determined in this section. The optimization process is done by behavioural simulations in MatLab base on the appropriate linear model of the SD modulator.

4.2.4.1 Architecture of SD modulator

The analysis of fully feed forward topology in previous section reveals that it has several attractive features over conventional topology:

- Linearity of modulator is less sensitive to the nonlinearity of building blocks of loop filter due to unity signal transfer function. Design requirement is relaxed greatly

- Better stability comparing to conventional topology since there is no delay between input and output of the modulator

- Smaller internal signal swing as the loop filter processes quantization noise only. This further improves the stability of the modulator and reduces the output swing requirement of OTA.

- Improved the dynamic range of the modulator as the overload level increased due to the smaller internal signal swing.

- The only DAC feedback path reduces the design complexity of the modulator.

Due to these advantageous features, a single loop fully feed forward topology with a 1.5-bit quantizer is used in this design project. The order of loop filter and the OSR will be determined in next section.

4.2.4.2 Order of loop filter and OSR

Although 1st order modulator is intrinsically stable, it is hardly used in design because of its poor SNR performance and the existence of idle tone in spectrum. Practically, 2^{nd} to 4^{th} order SD modulator is more popular. Further increase in order above fourth order will not gain much in SNR performance due to the application of

smaller loop coefficient for stability. Therefore, the performance of 2^{nd}, 3^{rd} and 4^{th} order conventional and feed forward SD modulator is investigated in this section.

First of all, the calculated SNR performance of 1-bit quantization ideal SD modulator is presented in Table 4.1 [Pel97].

Table 4.1: Calculated SRN of 1-bit quantization ideal SD modulator [Pel97]

Order	2nd		3rd		4th	
OSR	SNR	OL	SNR	OL	SNR	OL
16	37	1	53	1	68	1
32	52	1	74	1	95	1
64	67	1	95	1	122	1
128	82	1	116	1	149	1

OL column shows the overload level of SD modulator. In this ideal case, all integrators coefficient in the loop filter are 1. According to this table, in order to achieve dynamic range over 90 dB, a 3^{rd} order loop filter with 64 and above OSR or a 4^{th} order loop filter with 32 and above OSR can be used. However, the SNR performance is lower than the ideal situation in reality, especially when the order increases. For the sake of stability, integrators coefficient must be less than 1 and hence SNR performance reduces. Table 4.2 shows the SNR performance with optimized loop coefficient for stable 2^{nd} to 4^{th} order conventional single loop SD

modulator from [Pel97]. The values in brackets are the difference between real stable modulator performance and the ideal performance.

Table 4.2: SNR performance of stable 2nd to 4th order conventional SD modulator with optimized loop coefficient [Pel97]

Order	2nd		3rd		4th	
Coefficient	a=[0.5, 0.5]		a=[0.2, 0.5, 0.5]		a=[0.2, 0.2, 0.5, 0.5]	
OSR	SNR	OL	SNR	OL	SNR	OL
16	35(-2)	0.7	38(-15)	0.6	34(-34)	0.6
32	50(-2)	0.7	60(-16)	0.55	67(-28)	0.6
64	66(-1)	0.7	80(-15)	0.55	91(-31)	0.55
128	80(-2)	0.65	105(-11)	0.55	123(-26)	0.55

As shown in table 4.2, the noise shaping drops a lot after introducing loop coefficient for stability purpose. Only the 3^{rd} order modulator with 128 OSR and 4^{th} order modulator with 64 or 128 OSR are able to achieve required SNR performance with the stated loop coefficient.

Although the data in Table 4.1 and Table 4.2 show the SNR performance of conventional topology SD modulator, they truly reflects the SNR performance of fully feed forward topology SD modulator with same order and same OSR setting since the noise transfer functions for these two topology are identical. The data shown in [Yao05] verifies the above statement.

Table 4.3: SNR performance of 2nd to 4th order fully feed forward SD modulator with optimized loop coefficient [Yao05]

Order	2nd		3rd		4th	
Coefficient	a=[0.3, 0.7] c=[2, 1]		a=[0.1, 0.3, 0.2] c=[1, 1, 1]		a=[0.2, 0.4, 0.1, 0.1] c=[1, 1, 1, 2]	
OSR	SNR	OL	SNR	OL	SNR	OL
16	45	0.95	41	0.85	22	0.9
32	62	0.9	63	0.8	63	0.85
64	78	0.9	86	0.8	95	0.75
128	102	0.9	109	0.8	125	0.75

As we can see, the data for SNR in Table 4.2 and Table 4.3 are pretty much the same for 3rd and 4th order loop filter. These two tables also show the overload level of SD modulator with different topologies. It is very obvious that the fully feed forward offers much higher overload level. This is helpful in obtaining better dynamic range performance for the modulator.

The SNR performance shown in these three tables is simulated under no-noise condition. Unfortunately, noise exists everywhere in real world and it does affect the modulator performance in great extent. The existence of unavoidable noise such as input signal noise, thermal noise and flicker noise further reduces the SNR performance of SD modulator. There is a reduction of a few dB to tens of dB in SNR according to noise condition. Therefore, in order to meet the design requirement, 4th

order loop filter with 128 OSR, who offers more than 100dB SNR, is used in this project for a safe design.

Fig 4.12 shows the SNR vs OSR plot for the proposed 4th order fully feed forward SD modulator with 1.5-bit quantization and optimized loop coefficients.

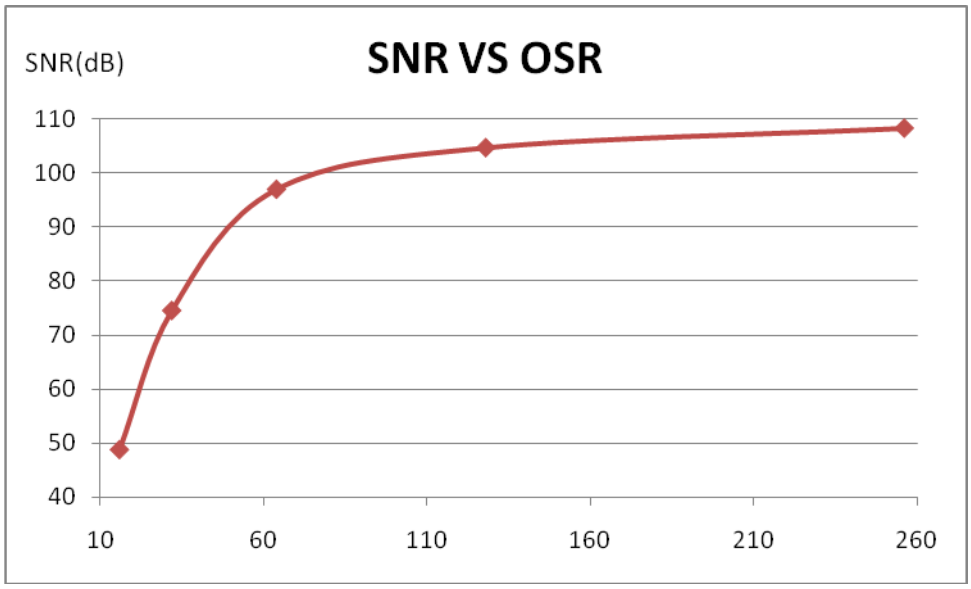

Fig 4.12: SNR vs OSR for the proposed 4th order modulator

4.2.4.3 Loop Coefficient optimization

Optimization of loop coefficients for a 4th order fully feed forward SD modulator is a very tedious work because there are 4 integrator coefficients and 4 feed forward gain coefficients in this system. Furthermore, as SD modulator is a strong non-linear system, analytical tools are not suitable for its loop coefficients optimization. The

simplest way to do the optimization is running extensive behavioural simulation to extract the SD modulator performance under different coefficient setting. After that, the combination that produces best performance is chosen to be the optimized loop coefficients.

The tedious part of this method is that it is not possible to sweep all eight variables at the same time. In each simulation cycle, only two variables are swept while the other six variables are fixed. After that the contour plot of the output data is constructed which reveals the region of coefficients that produces peak SNR performance. By repeating this simulation cycle with different sweeping variables, the optimized loop coefficients can be obtained.

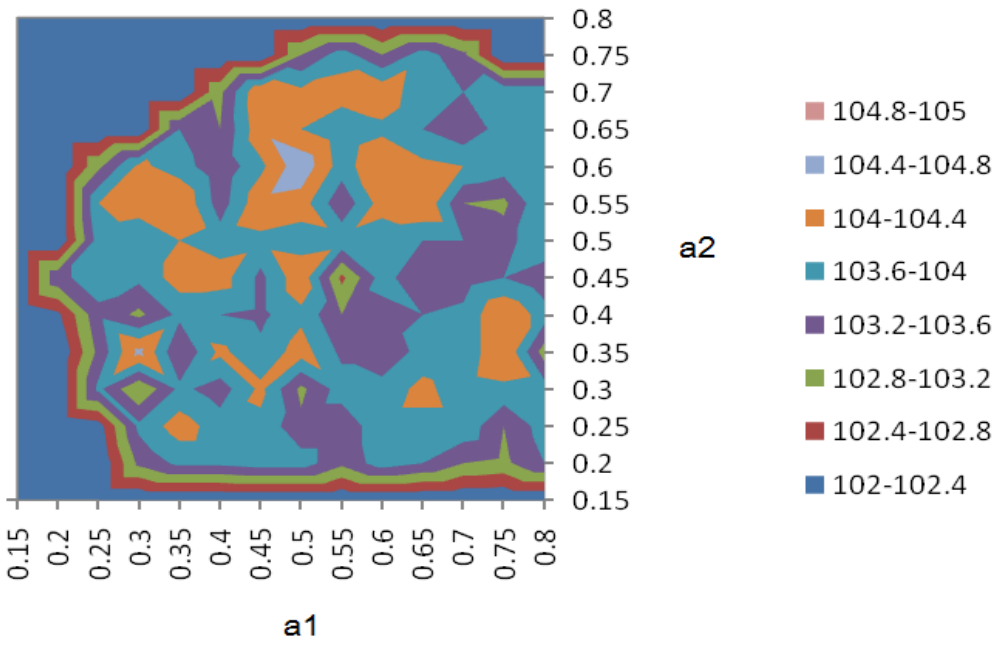

Fig 4.13: Contour plot of SNR with a1 and a2 as sweeping variable

Fig 4.12 shows the result of one of these simulation cycles. Those areas with 0 SNR is the unstable region which should be avoid in design. For this SNR contour plot, two integrator coefficients (a1, a2) are swept and feed forward coefficient (c1, c2, c3, c4) is fixed to (2, 2, 1, 1) while the other two integrator coefficients (a3, a4) is fixed to (0.5, 0.1). It is clearly seen that peak SNR occurs at the region where (a1, a2) = (0.5, 0.6) and hence a1 = 0.5 and a2 = 0.6 is chosen to be the optimum coefficient.

The optimized loop coefficients:

(a1, a2, a3, a4) = (0.5, 0.6, 0.5, 0.1)

(c1, c2, c3, c4) = (2, 2, 1, 1)

4.2.4.4 OTA gain

Operational Transconductance Amplifier (OTA) is the most important building block of SD modulator. The magnitude and linearity of the OTA gain determines the overall performance of the SD modulator. Hence it is necessary to determine the OTA gain requirement base on the noise shaping capability and linearity specification of the SD modulator before proceed to circuit level design.

The gain of a real OTA is not constant over entire input range. The gain variation introduces harmonic distortion to the input signal. To investigate the effect of non-linearity OTA gain, a non-linear model is built and behavioural simulation is carried out base on this. According to the definition of harmonic distortion, the input dependant OTA gain can be written as [San99]:

$$A = A_o(1 + 4hd_2 \cdot v_i + 12hd_3 v_i^2)$$

$$A \approx A_o(1 + \frac{4hd_2 \cdot v_o}{A_o} + \frac{12hd_3 v_o^2}{A_o}) \qquad \text{(Equation 4.9)}$$

Where A_o is the small signal DC gain of OTA; v_o and v_i are the input and output respectively. By applying this output dependant OTA gain instead of constant OTA gain in the SD linear model, the non-linear effect of SD modulator can be

obtained in behavioural simulation. Fig 4.13a and Fig 4.13b shows output spectrum of conventional SD modulator and fully feed forward SD modulator with non-linear OTA respectively [Yao05].

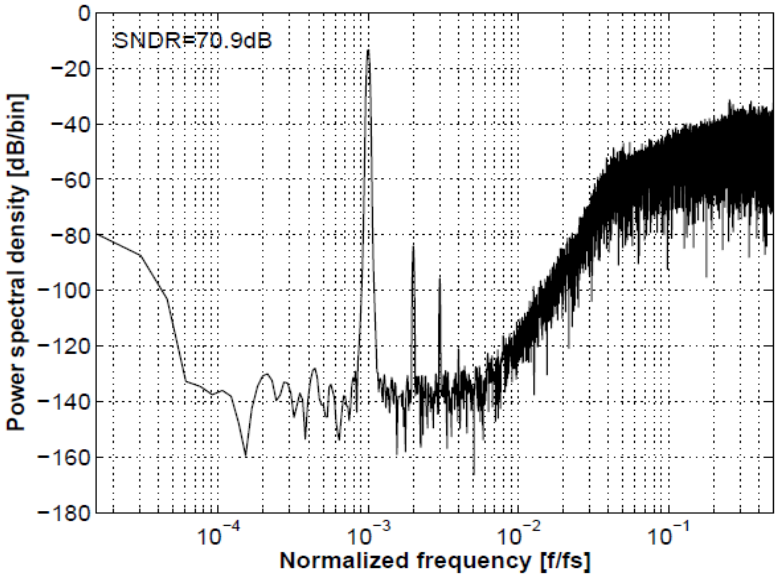

Fig 4.14a: PSD of 4th order conventional SD modulator with non-linear OTA, Ao=40dB

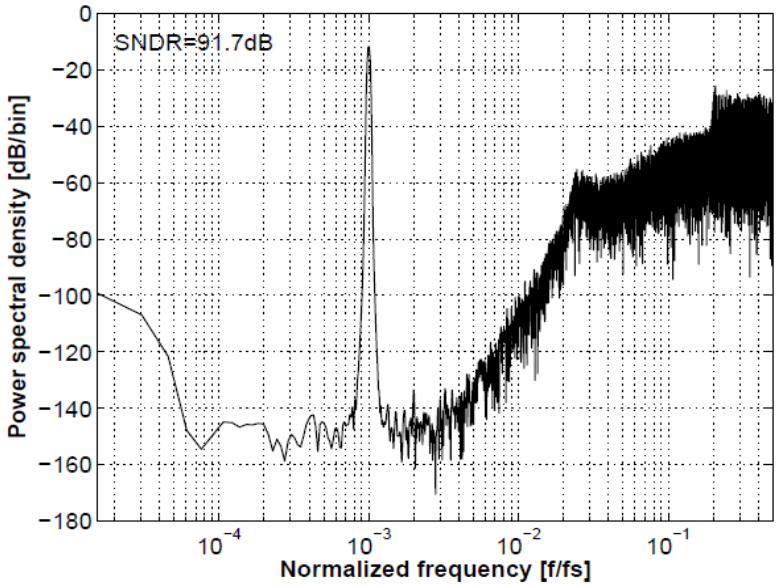

Fig 4.14b: PSD of 4th order fully feed forward SD modulator with non-linear OTA, Ao=40dB

With the same degree of non-linearity and small signal DC gain of the OTA, the conventional SD modulator shows a much higher harmonic distortion at the output comparing to the feed forward SD modulator. This is because the input signal passes through the loop filter and is distorted by the non-linear OTA. Therefore, the gain requirement of OTA for conventional SD modulator is mainly determined by the harmonic distortion criteria rather than the noise shaping capability. According to Equation 4.9, the harmonic distortion can be suppressed by improving the small signal DC gain of the OTA. Hence, in order to get a high linear conventional SD modulator, very high gain OTA is required, usually more than 60 dB [Mar99].

Thanks for the unity signal transfer function, the SD modulator with fully feed forward topology does not suffer from non-linear gain OTA. Harmonic distortion is hardly seen in Fig 4.14b. Therefore, the OTA gain for feed forward SD modulator is only determined by the noise shaping capability. The following figure shows the dependence of noise shaping of SD modulator on OTA gain.

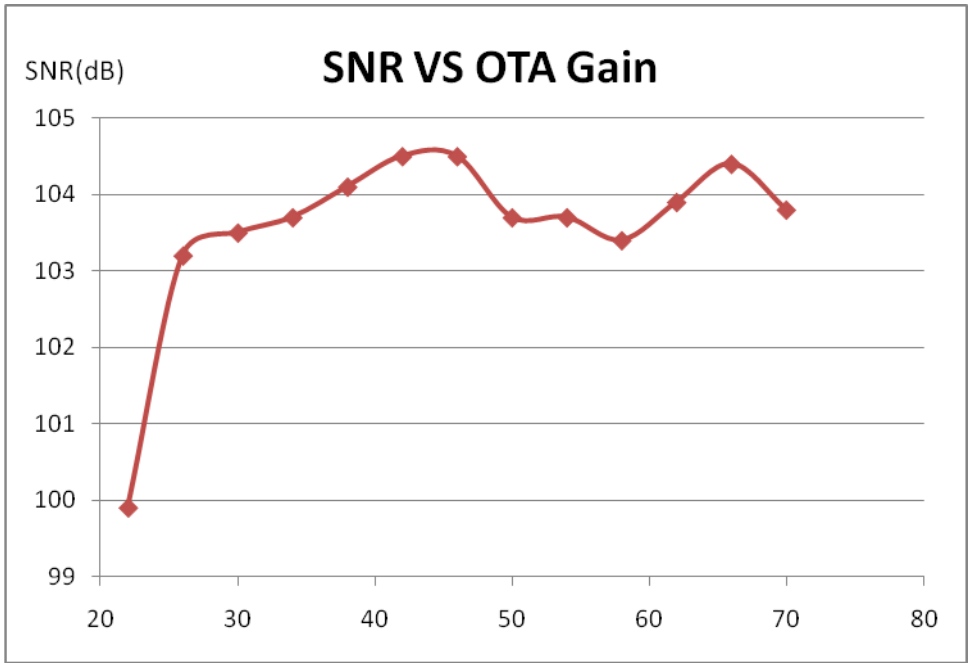

Fig 4.15: SNR performance base on OTA gain for proposed SD modulator

From Fig 4.15, we can conclude that the OTA gain of 30dB is sufficient for noise shaping alone. Thus, the minimum OTA gain requirement for this design is 30dB.

4.2.4.5 Effect of OTA offset

Offset in OTA is unavoidable in design. It acts as a dc biasing voltage at the OTA input which affects the output of SD modulator. In this section, the effect of OTA offset is briefly discussed. The offset of OTA can be categorized into systematic offset and random offset. The systematic offset is caused by design carelessness, which can be eliminated. The random offset is due to the process variation and

mismatch in fabrication process, which can only be minimized but cannot be eliminated.

The offset of OTA at the 1st stage integrator can be seen as adding a constant dc biasing voltage directly to the input signal. It introduces a dc tone to the output spectrum without any attenuation. The offset of OTA at the 2nd stage integrator is attenuated by the OTA gain of 1st stage integrator if seeing it at the input of loop filter. Therefore, the effect of offset of OTA at 2nd stage on modulator output is much smaller than that of the 1st stage. And the effect of offset of 3rd stage OTA, 4th stage OTA and quantizer can be ignored as they are greatly attenuated by the open loop gain of 1st and 2nd stage OTA.

Since offset acts just like a constant dc biasing voltage at the OTA input, it does not add any harmonic and noise. The linearity and noise shaping capability of SD modulator is not affected by the existence of OTA offset.

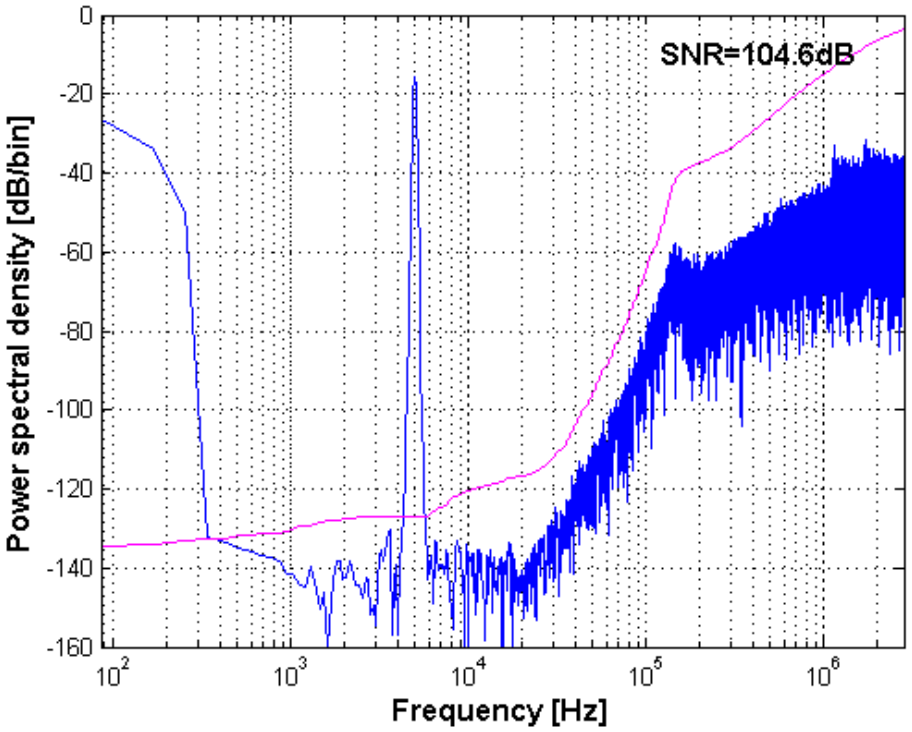

Fig 4.16a: Effect of 1st stage OTA offset alone

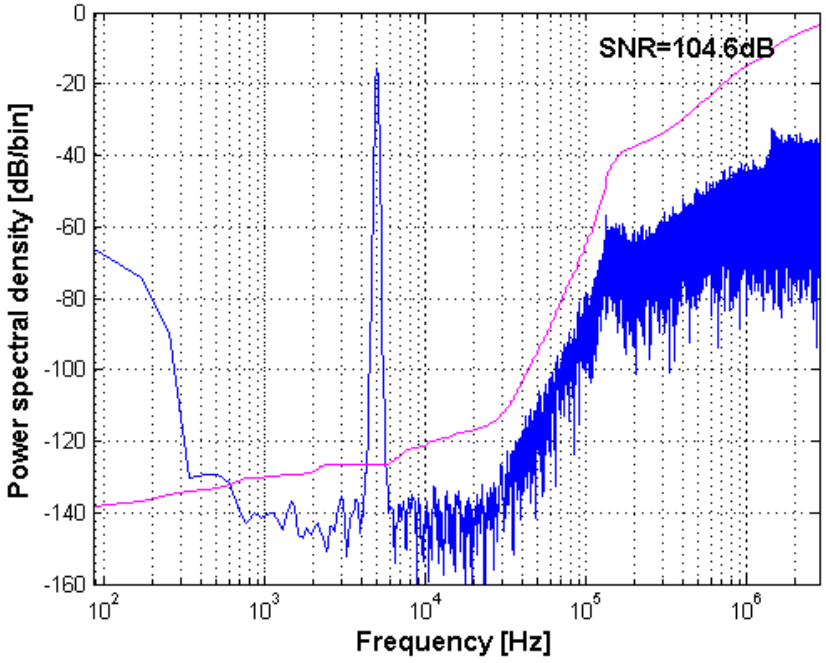

Fig 4.16b: Effect of 2nd stage OTA offset alone

Fig 4.16a and Fig 4.16b shows the effect of OTA offset in 1st and 2nd stage integrator on SD modulator output spectrum respectively. Although the offset value is the same for these two simulations, the dc power in Fig 4.16b due to 2^{nd} stage OTA offset alone is 40 dB less than that in Fig 4.16a. This is because it is attenuated by 40 dB OTA gain in the 1^{st} stage.

Since the offset of OTA introduces dc power, which reduces the power efficiency, it should be minimized in design. From the above analysis, we conclude that the gain and offset of 1^{st} OTA dominates this effect. Therefore, the 1^{st} stage OTA is the more important one which requires large dc gain and small offset.

4.2.4.6 Overall system level SD design

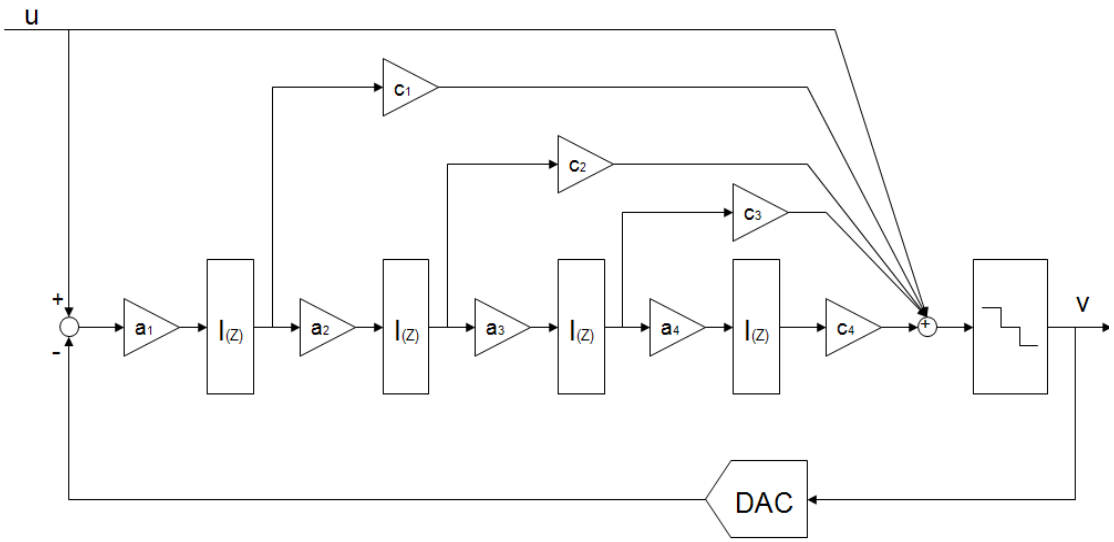

Fig 4.17: Overall architectural of proposed 4th order fully feed forward SD modulator with a 1.5-bit quantizer

Fig 4.17 shows the overall architectural design of proposed SD modulator in this project. It consists of a single loop fully feed forward 4th order loop filter and a 1.5-bit quantizer. The optimized loop coefficients are (a1, a2, a3, a4) = (0.5, 0.6, 0.5, 0.1) and (c1, c2, c3, c4) = (2, 2, 1, 1). The OTA gain of each stage is fixed to be 40 dB.

4.3 Circuit Implementation

Base on analysis tools and behavioural simulations, most of the system parameters and some of the building blocks specifications are determined in the system level design. It is the time to proceed to realize the proposed SD modulator in real electronic circuit. Transistor level circuit implementation of the proposed SD modulator is presented in this section.

Fig 4.18 in the next page shows the entire SD modulator circuit implementation. The signal path in this circuit is differential. This helps to reduce even order of harmonic distortion and to improve common noise rejection. The integrators in the loop filter are realized in switch-capacitor topology. The discrete time (DT) integrator has better noise immunity. More importantly, it is less affected by the process variation and hence, it has better accuracy than that of continuous time integrator.

The circuit implementation of those building blocks in Fig 4.18 such as OTA, quantizer and feed forward summing mechanism is discussed in detail. Some transistor level simulation results are also shown to verify the performance of the building blocks.

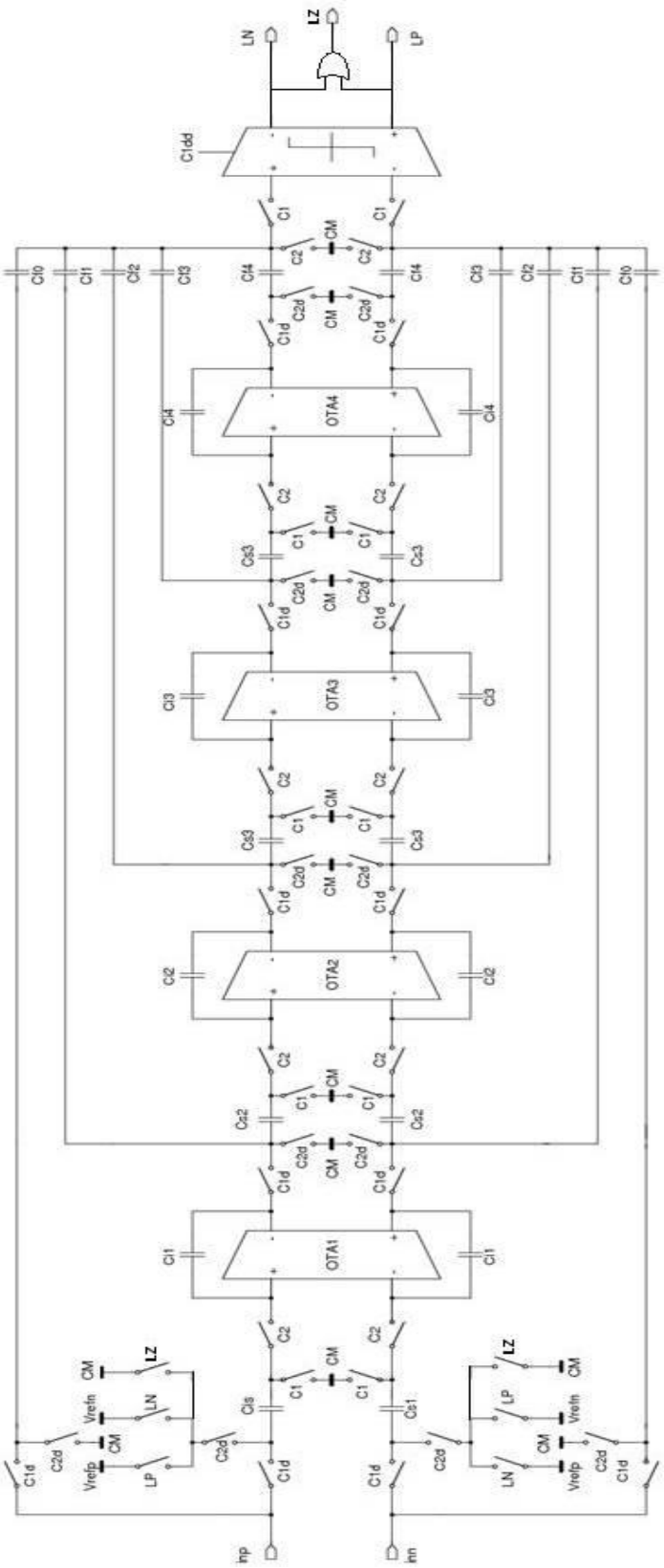

Fig 4.18: Circuit implementation of proposed 4th order fully feed forward SD modulator

4.3.1 OTA design

Being the major building block of the modulator, the performance of OTA dominates the overall performance of the SD modulator, especially the 1st stage OTA. They are also the major power consuming block in the loop filter.

The 1st stage OTA design is critical. Base on the analysis in last section, the non-idealities of 1st stage OTA directly reflects on the modulator output and hence, high gain and low random offset are required. The design requirement of OTA for the following stages can be relaxed. In order to save the power consumption and chip area, the biasing current and transistor size are scaled down accordingly. The design detail in this part is mainly for the 1st stage OTA.

According to section 4.2.4.4, the minimum gain of OTA is 30dB for the fully feed forward SD modulator. However, the dc gain of 1st stage OTA should be higher than the minimum value in order to have better suppression for the non-idealities of the following stage OTAs. Besides that, the process variation in fabrication may introduce a few dB drops in the worst corner. Thus, the 1st stage OTA should have voltage gain in between 50 dB to 60 dB.

Since the internal signal swing is small, the output swing requirement of the OTA is reduced. One of the best topologies to implement high gain and low output swing application with small drain current is the telescopic OTA. A single stage telescopic OTA is able to deliver voltage gain higher than 50 dB. Besides that, a single stage OTA is more stable and no dedicated compensation circuit required. This greatly reduces the design complexity and area consumption.

The bandwidth of OTA is determined by the settling speed. The OTA output must be settled well within one clock cycle in order to have good accuracy. Since a single stage OTA can be approximated to be a first order system, its settling time only depends on the GBW. In order to reduce the settling error for the 1st stage OTA, its GBW is set to be about ten times of the sampling clock. As the maximum OSR for this design is 128, the maximum sampling frequency is 5.6 Mhz. GBW around 60 MHz is sufficient for the settling of OTA.

The list below is the design target of 1st stage OTA:

- DC gain: above 50 dB
- GBW: above 60 Mhz
- PM: above 60 degree

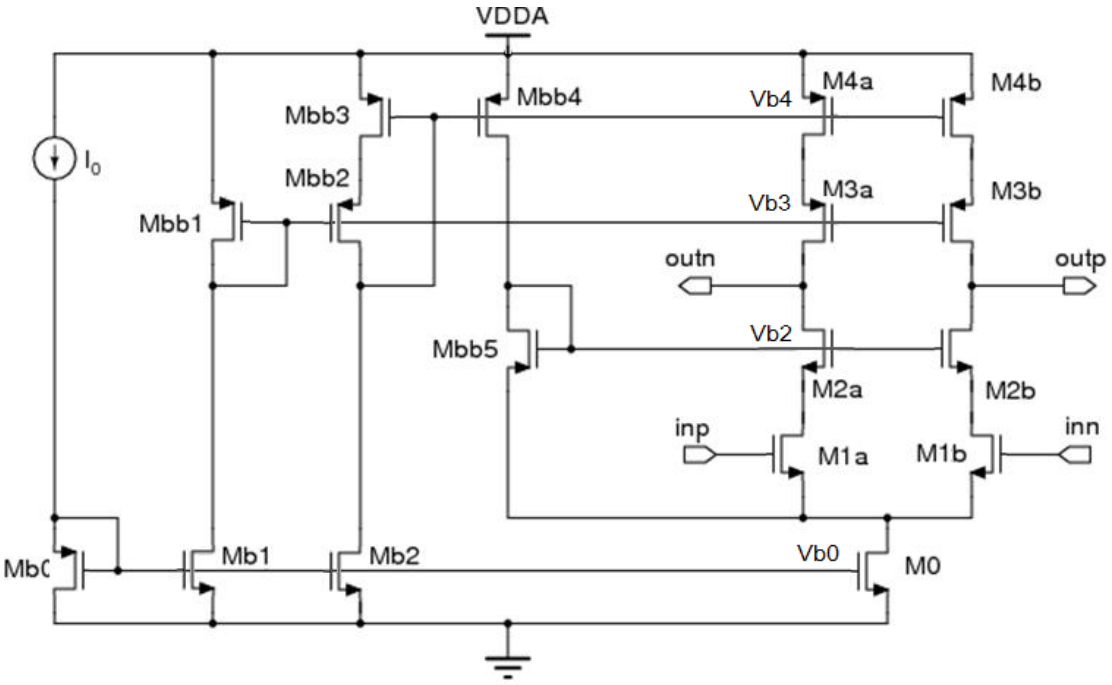

Fig 4.19: Schematic design of the single stage telescopic OTA

Fig 4.19 shows the schematic design of the telescopic OTA. The left hand side is the biasing circuit that provides biasing voltage to transistor M0, M2, M3 and M4 while the right hand side is the core of the telescopic OTA. The biasing voltages Vb0, Vb2, Vb3 and Vb4 are set to ensure that all the transistor in the telescopic core are in saturation during normal working condition. Besides that, they are optimized to maximize the output swing of the OTA:

$$V_{b4} = V_{dd} - \left(V_{th4} + V_{dsat4}\right)$$

$$V_{b3} = V_{dd} - \left(V_{th3} + V_{dsat3} + V_{dsat4}\right)$$

$$V_{b2} = V_{in\_cm} - V_{gs1} + V_{dsat1} + V_{th2} + V_{dsat2}$$

With the above biasing voltage, the output common mode range can be determined:

$$V_{out\_cm(\max)} = V_{b3} + V_{gs3} - V_{dsat3} \approx V_{dd} - V_{dsat4} - V_{dsat3}$$

$$V_{out\_cm(\min)} = V_{b2} - V_{gs2} + V_{dsat2} = V_{in\_cm} - V_{th1} + V_{dsat2} \quad \text{(Equation 4.10)}$$

From Equation 4.10, we notice that the output common mode voltage can be set to slightly lower than the input common mode voltage if V_{th1} is greater than V_{dsat2}. This allows the output common mode voltage to be the same as input common mode voltage in the design, which eliminates the voltage shifter in between two integrators and reduces error and design complexity. For simplicity, output common mode and input common mode voltage is set to be half of power supply voltage.

The gain of the OTA is determined by the transconductance of the input pair (g_{m1}) and r_o of loading transistors. Since r_o is proportional to the channel length, large channel length is used for those loading transistors.

$$A_{dc} \approx g_{m1} \cdot r_o^2 \quad \text{(Equation 4.11)}$$

The speed of a telescopic OTA is dominated by g_{m1} and the output load capacitance (C_{load}).

$$GBW \approx \frac{g_{m1}}{C_{load}} \qquad \text{(Equation 4.12)}$$

Besides that, the tail current of differential pair should be high enough to meet the slewing requirement of the output. This is because the loading capacitance is in the range of 10pF, large charging and discharging current is needed to make the load capacitor voltage to be settled in a short time.

The dominant pole of the OTA is at the output node and the non-dominant pole is at the source terminal of M2. Since the loading capacitance is much larger than M2 gate-source parasitic capacitance, these two poles are separated far enough to keep the OTA in stable. Fig 4.20 is the AC response of the 1st stage OTA. It shows that its dc gain is 53.2 dB, GBW is 72.6 MHz and phase margin is 66.7 degree under typical corner (temperature=50 C, process corner=typical mid, vdd=3.3 V).

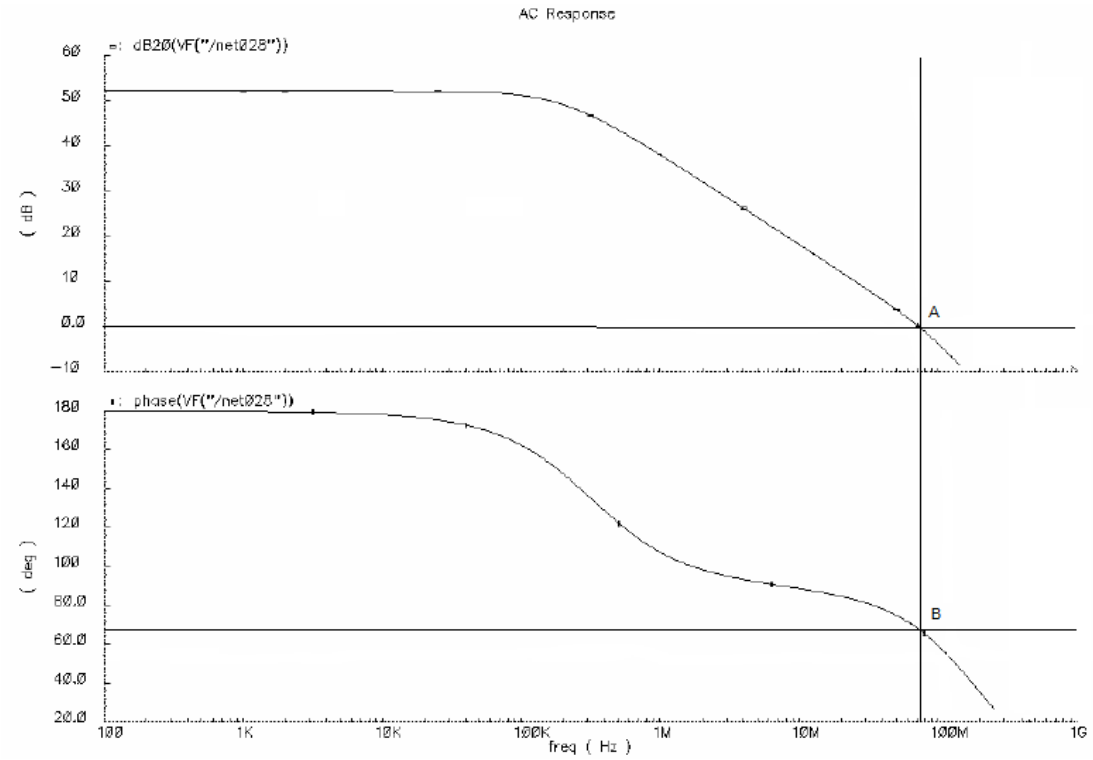

Fig 4.20: AC response of 1st stage OTA with 16pF loading capacitance

The offset of OTA is dominated by the mismatch and process variation of the input pair. Therefore, a very large size input transistor is used and special layout technique is applied in order to reduce the random offset voltage. According to Monte Carlo simulation of 100 samples, 3-sigma value of input offset is only 2.47 mV for the 1st stage.

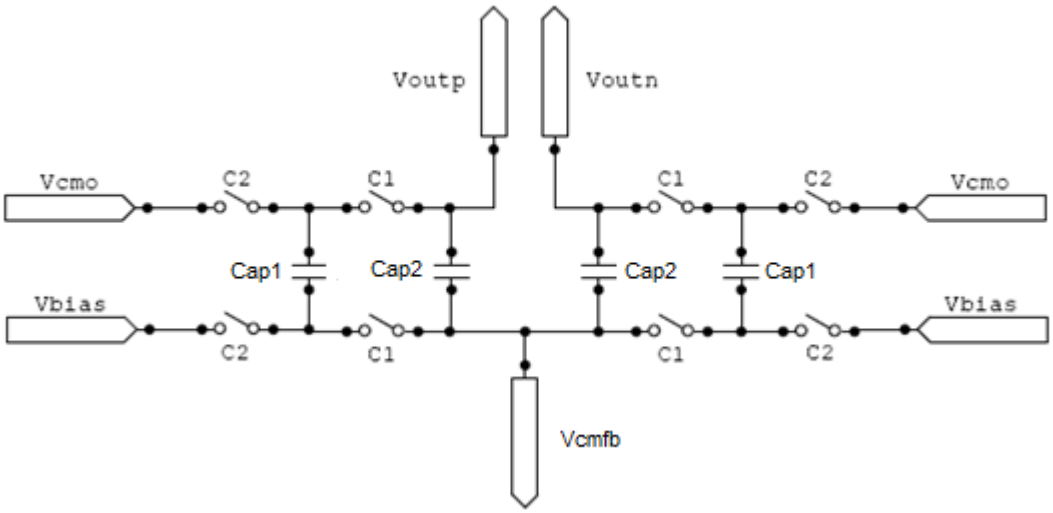

Fig 4.21: Switch-capacitor CMFB

Switch-capacitor common mode feedback (CMFB) is chosen for the OTA dui to its simplicity and its power efficiency [Kyo08]. Fig 4.21 shows the switch-capacitor CMFB circuit implementation. When C2 is on, the voltage difference between Vcmo and Vbias is store in Cap1. When C1 is on, charge sharing between Cap1 and Cap2 occurs and Vcmfb voltage is adjusted. Vcmfb voltage becomes stable only the following two conditions are met:

$$(Voutp + Voutn) / 2 = Vcmo$$

$$Vcmfb = Vbias$$

4.3.2 Comparator and 1.5-bit quantizer design

The comparator is the building block of 1.5-bit quantizer. In this project, a high speed cross-couple regenerative dynamic latch is used. Fig 4.22 shows the schematic design of the comparator.

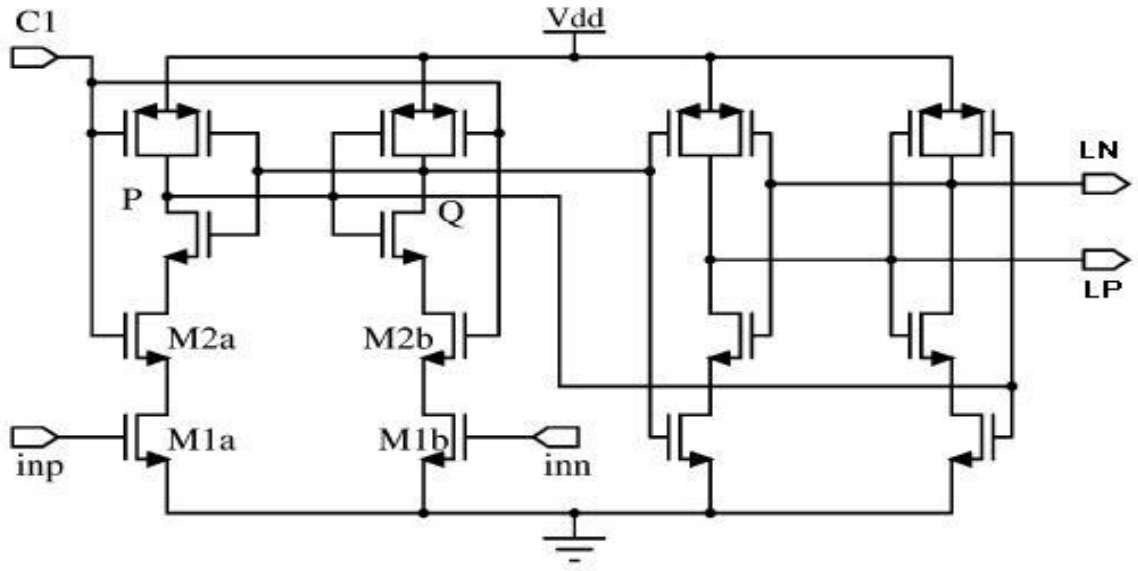

Fig 4.22: Schematic of regenerative latch comparator.

The left hand side of the schematic is the regenerative latch. It is a fully dynamic latch without dc biasing current. Two back-to-back connected inverters form a regenerative cell. Any charge imbalance at node P and Q initializes regenerative process and the output will reach to the stable point very fast. The right hand side of the schematic is the SR latch. It is also a fully dynamic circuit. It holds the regenerative latch output within one clock cycle and so that the comparator output does not return to zero at the

reset phase of regenerative latch. Thus, the SR latch helps to reduce the switching activity. Since this comparator is consists of two fully dynamic circuit, it consume very small power.

This comparator only needs one clock. When the clock is low, M2 is off. The regeneration node P and Q is charged to V_{dd}. When the clock goes up, M2 turns on and the regenerative process starts. The charge stored in node P and Q flow through M2 and M1 to the ground. If the gate voltages of M1 input pair are different, the branch with higher input voltage allows higher current flows so that the voltage at the corresponding regenerative node drops faster. The voltage imbalance at the regenerative node initiates the regeneration process of the cross-couple latch.

The reset speed and regenerate speed of this comparator is proportional to $e^{t/\tau}$. The maximum speed is approximately given by:

$$f_{\max} = \frac{g_{m1}}{2\pi \cdot C_p} \qquad \text{(Equation 4.13)}$$

Where C_p is the parasitic capacitance at node P and node Q. In order to have high regenerative speed, the transistors size in the latch cannot be large.

One important advantage of this comparator topology is low kick back noise. As the input pair is not directly connected to the regenerative node, the kickback noise is much smaller. Besides that, the voltage change at the drain terminals of two input pair has same polarity and similar amplitude. Therefore the kickback noise is a common mode disturbance which can be suppressed by the preceding fully differential circuit. Reduction in kick back noise helps to improve the accuracy of comparator.

Generally speaking, the offset of fully dynamic regenerative latch is usually pretty large. It can reach more than 100mV. Fortunately, the offset requirement is very relaxed due to the feedback as well as the attenuation of the preceding stage OTAs. Behavioural simulation verifies this conclusion. Therefore, no much attention is paid on the offset of the comparator.

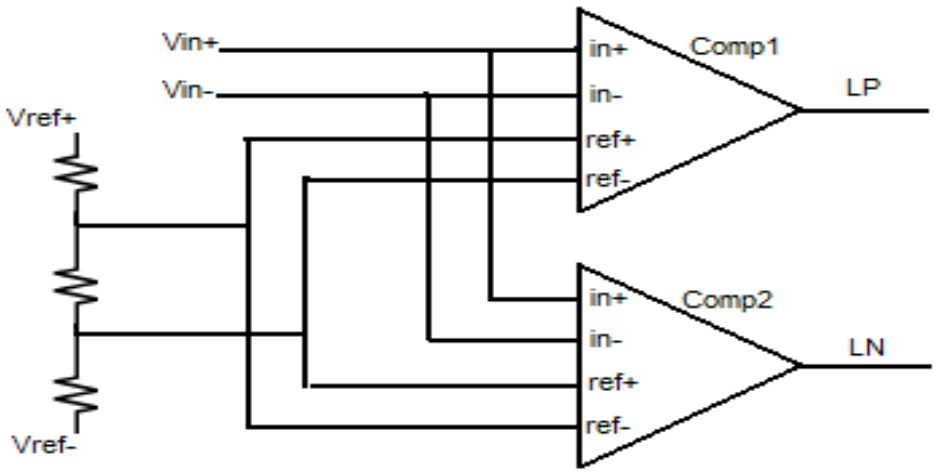

Fig 4.23: 1.5-bit quantizer

Fig 4.23 shows the block diagram of the three-level quantizer. It consists of two comparators. The reference is generated by a resister ladder. In fact, this 1.5-bit quantizer is a very simple and low resolution flash ADC. There are only three output states for this quantizer:

Table 4.4: Output states of the 1.5-bit quantizer

State	LP	LN
1	High	Low
0	High	High
-1	Low	High

4.3.3 Sampler design

The simplest switch-capacitor sampler is used in this design. Fig 4.24a and Fig 4.24b show the sampler circuit and the equivalent circuit during the sampling phase.

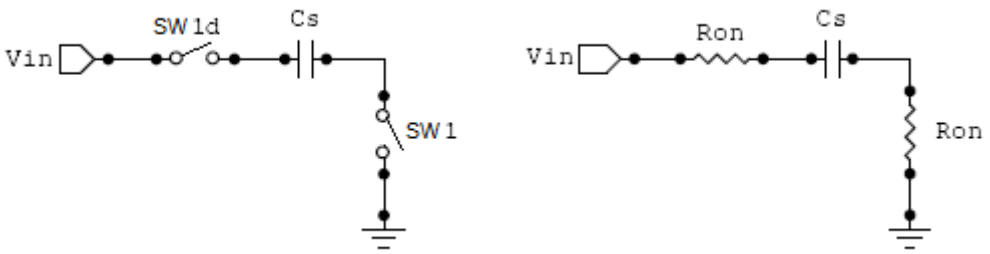

Fig 4.23a: Schematic of sampler; Fig 4.23b: equivalent circuit at sampling phase

During the sampling phase, switch SW1 turns on first and follow by SW1d. Vin is stored in the sampling capacitor Cs. Due to the non-ideal switches of SW1 and SW1d are used, RC time constant is formed by the Ron of the switches and the sampling capacitor.

Time required for 99% settling of a RC circuit is:

$$T_{on} = 4.6\tau$$

if the clock has 50% duty cycle:

$$\frac{1}{2 \cdot f_s} = 4.6 \cdot R_{on}C_s$$

$$R_{on}C_s = \frac{1}{9.2 \cdot f_s} \qquad \text{(Equation 4.14)}$$

The capacitance of Cs depends on the thermal noise level of the modulator. The behavioural simulation shows that a 6 pF sampling capacitor gives SNR larger than 100 dB for 128 OSR. Since the process variation of poly-cap is around +-5%, a 30% safety factor is given and hence, the sampling capacitance in this design is 8 pF.

Base on Equation 4.14 and Cs = 8 pF and fs = 5.6 MHz. Ron value can be obtain and the switches size can be estimated. It is worth to mention two major causes that introduce sampling error apart from sampler speed. The first one is the input

depend Ron of the switch. Since Ron is a function of Vgs of pass transistor, Ron is not constant for different input voltage. For the constant Vg, the Ron increases if the input level increases. This input dependent Ron results in non-linear sampler.

The second non-ideal effect is the charge injection of the switch at on and off. During the turn-on time of the switch, charge is drawn from the surrounding circuit to form the conduction channel under the gate; while during the turn-off time, conduction channel under gate is eliminated and the charge is distributed to the surrounding circuit. Charge injection adds constant amount of charge to the sampling capacitor regarding to the size of the switch if the input level is unchanged. There are some charge-injection-cancellation techniques that can effectively reduce the sampling error due to charge injection.

4.3.4 Non-overlap Clock generator design

Two non-overlap clock signals are required for sampling and integration phase for the integrator. Fig 4.24 shows the schematic of the clock generator.

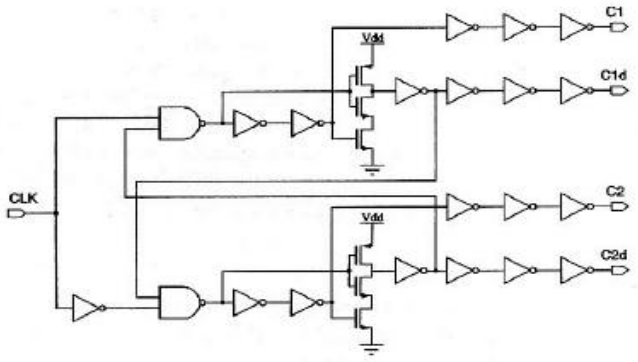

Fig 4.24: Clock generator

An external clock is fed into the clock generator and four clock signals are generated. C1 turns on after C1d and it turns off before C1d. C2 turns on after C2d and it turns off before C2d. Since C1 is the sampling phase while C2 is the integration phase, C1 and C1d do not overlap with C2 and C2d at any time instant. Fig 4.25 shows the output of the clock generator.

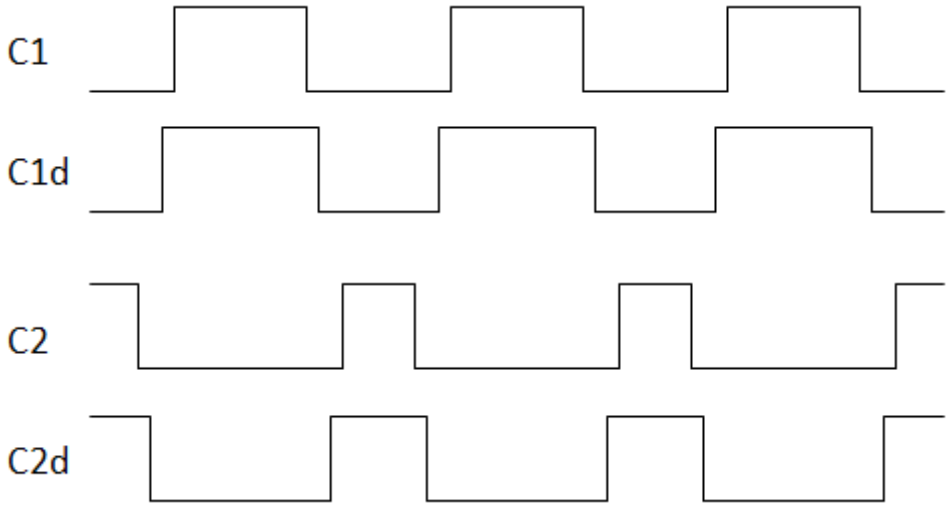

Fig 4.25: Output of clock generator

4.3.5 Feed forward summing design

There is a summing point where all the feedforward branches signals are summed together in a fully feed forward SD modulator. The summation is implemented by a switch-capacitor network shown in Fig 4.26 in the next page.

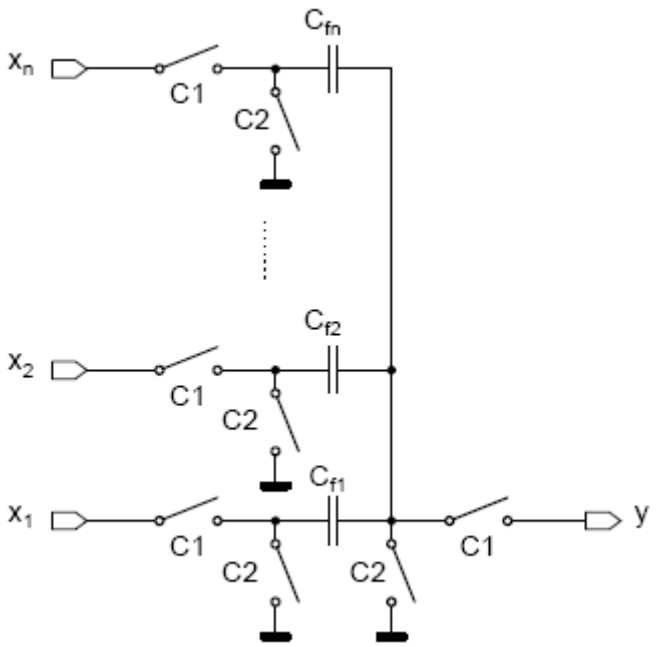

Fig 4.26: Summing point of the feed forward path

At phase C2, all summer capacitors are discharged. The charge stored in the capacitors is zero. At phase C1, summer output a valid result at Y. The transfer function of this summer is derived below:

$$(y-x_1)\cdot C_{f1}+(y-x_2)\cdot C_{f2}+\cdots+(y-x_n)\cdot C_{fn}=0$$

$$y\cdot(C_{f1}+C_{f2}+\cdots+C_{fn})=x_1\cdot C_{f1}+x_2\cdot C_{f2}+\cdots+x_n\cdot C_{fn}$$

$$y\cdot C_{unit}\cdot(\alpha_{f1}+\alpha_{f2}+\cdots+\alpha_{fn})=C_{unit}\cdot(x_1\cdot\alpha_{f1}+x_2\cdot\alpha_{f2}+\cdots+x_n\cdot\alpha_{fn})$$

$$y=\frac{C_{unit}\bullet\sum_{i=1}^{n}x_i\cdot\alpha_{fi}}{C_{unit}\bullet\sum_{i=1}^{n}\alpha_{fi}} \qquad \text{(Equation 4.15)}$$

Where α_{fi} is the loop coefficient for each feed forward path.

4.3.6 Feedback and Vref generation

Due to the fully differential architecture of the SD modulator, two reference voltages are required in this design, namely Vrefp and Vrefn (refer to Fig 4.18). These two references are generated by the feedback network from the H-bridge output. Fig 4.27 shows the configuration of the reference voltage generation circuit.

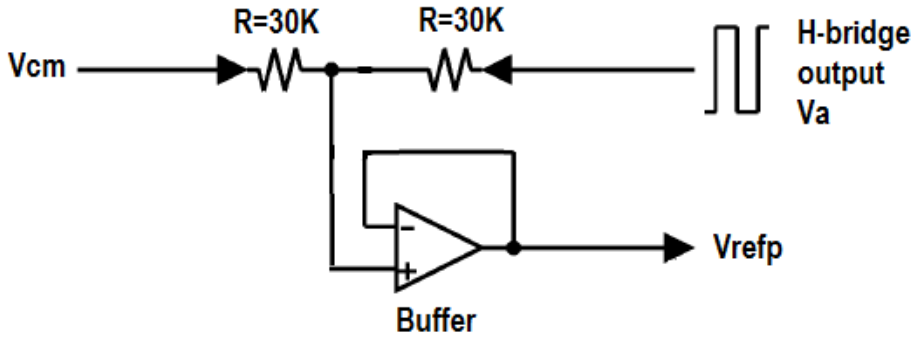

Fig 4.27: Reference voltage generation circuit

The other voltage reference is also generated by the same circuit by tapping the feedback point from H-bridge output Vb.

According to discussion in section 3.5, the gain of class D amplifier decreases if the H-bridge supply voltage decreases. From Fig 4.27 we observed that Vrefp also decreases when H-bridge supply voltage decreases. Decreasing in reference voltage results in increasing in degree of modulation and hence the gain of class D amplifier increases. Therefore, this feedback network helps to compensate the gain error due to the variation of H-bridge supply voltage so that the low frequency PSRR is improved.

Chapter 5:
Output Stage Design

The output stage of class D amplifier is in charge of delivering power to the load. It consists of gate driving circuit, full H-bridge output and the off-chip LPF. The design details of these building blocks are covered in this chapter.

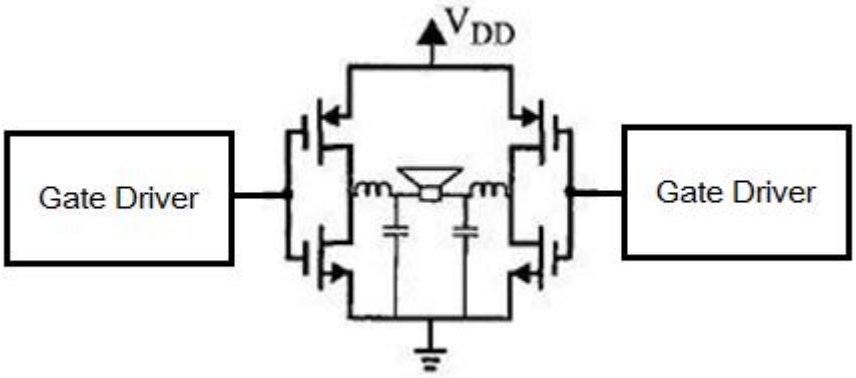

Fig 5.1: Output stage of class D amplifier: Gate Driver, H-Bridge and LPF

5.1 Full H-bridge output

Base on the discussion in chapter 3, the full H-bridge output is superior in term of performance comparing to the half bridge output. It is used in this design. Since high power rating and low on-resistance are required for the output transistors, their size is

generally very large, usually consumes more than half of the whole class D amplifier chip.

Power transistor in output stage acts as a switch which is controlled by the SD modulator. If it is ideal, there will be no power loss in the output stage. Unfortunately, the existence of on-resistance during conduction period and parasitic capacitance of the power transistor limits the power efficiency of the class D amplifier. Hence, the output stage must be properly designed in order to optimize the overall power efficiency.

There are three types of power loss in class D amplifier: switching loss, conduction loss and short-circuit current loss. Two of these power losses are only introduced by the H-bridge output stage: short-circuit current loss and conduction loss which are related to the on-resistance of the power transistors. Besides that, since the output transistor size is very large, its parasitic capacitance is also large. According to Equation 5.1, the switching loss of the output stage is large. In fact, the major switching loss of the overall system is contributed by the H-bridge output stage. Since all three types of power loss in class D amplifier are dominated by the output stage, the overall power efficiency of the class D amplifier is determined by this output stage.

Power loss in class D amplifier:

(1) Switching Loss: $P_{sw} = \alpha f_s C_p V_{dd}^2$ (Equation 5.1)

(2) Conduction Loss: $P_{cond} = \frac{1}{T}\int_0^T i_L(t)^2 R_{on} dt \approx \frac{R_{on}}{R_L} \times P_{out}$ (Equation 5.2)

(3) Short circuit Loss: $P_{sc} = I_{mean} \times V_{dd}$ (Equation 5.3)

- **Sizing of output power transistor**

The output transistor size is chosen to optimize power dissipation base on input signal condition. In order to increase the maximum output power and reduce the conduction loss, according to Equation 5.2, the on resistance of the output transistor must be small. This ensures that the voltage drop across source-drain of the output transistor is small. Base on Equation 5.4 the on-resistance can only be reduced by increasing W/L ratio of the output transistor because μC_{ox} is process parameter and $(V_{GS} - V_{th})$ is a constant.

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_{th})} \quad \text{(Equation 5.4)}$$

Lowering of R_{on} results in large size of output transistor which contributes significant gate capacitance. This leads to large switching loss. Therefore, sizing of

output power transistor is a trade-off between conduction loss and switching loss. Since conduction loss dominates power dissipation and efficiency at high output level while switching loss dominates at low output level, output transistor size is also determined by the application. In this design, the target of maximum power efficiency is around 80%. Since the maximum power efficiency is dominated by conduction loss, transistor size is optimized base on on-resistance requirement.

Assume 80% of power loss at very high output level is contributed by the conduction loss of the switches, for a class D amplifier with 85% maximum power efficiency and 1W maximum output power, the power loss due to conduction is 140mW. Base on Equation 5.2, $(R_{onp} + R_{onn}) \approx 0.56\Omega$ for a 4 Ω load. In order to have similar rising and falling time of the output waveform, the on-resistance for NMOS and PMOS switch should be the same.

The on-resistance is extracted by doing transistor level simulation. Fig 5.2 is the setup for extraction of R_{on}. The ratio of voltage difference between R_L and source-drain gives exact value of R_{on}.

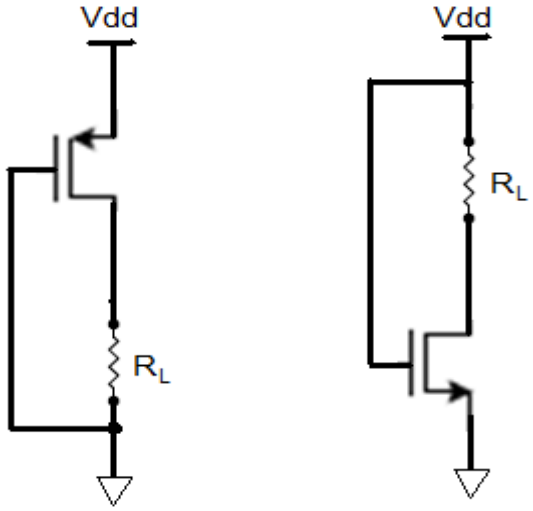

Fig 5.2: Test bench for extraction of on-resistance

Base on the simulation:

NMOS switch: (W/L) = 10500 with $R_{onn} = 0.257\Omega$

PMOS switch: (W/L) = 32000 with $R_{onp} = 0.286\Omega$

Minimum channel length is used for those four output transistors.

5.2 Gate driving circuit

Since the output transistor size is very large for this design, a buffer is necessary in between the SD modulator and full H-bridge output. The buffer provides sufficient current to drive the large parasitic capacitance of output transistors. Generally, this buffer is realized by inverter chain.

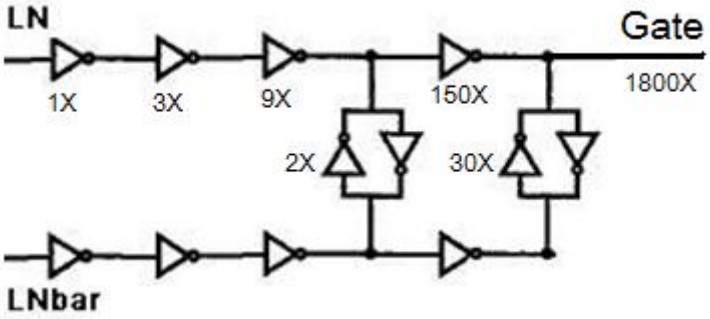

Fig 5.3: structure of gate driver

Fig 5.3 shows the structure of the gate driving circuit. It is an inverter chain with weak cross-coupled inverters. The number in the figure indicates the size of each inverter in the chain. Due to the existence of cross-coupled inverter, the design process of this gate driving buffer is different from the conventional inverter chain. Extensive transistor level simulation has been done to determine the size of those weak cross-coupled inverter.

The transition time of the gate terminal of output transistor is optimized in this design. According to Equation 5.3, short-circuit current loss of the output stage can be minimized by reducing the average short-circuit current. Decreasing the transition time of the gate control signal effectively reduce the average short-circuit current. This is the main reason for adding these weak cross-coupled inverters into the inverter chain. The feed-forward provided by the cross-coupled inverters helps to minimize the signal skew of the gate control signal [Jor03]. Besides that, the falling time and

rising time of the gate control signal is optimized to be the same by fine tuning the transistor ratio of inverters to ensure low distortion of the gate driving circuit.

The rising time and falling time of the gate driver output with output transistor as load is extracted by transistor level simulation in typical corner:

Average 90% rising time of NMOS switch: 236ps

Average 90% falling time of NMOS switch: 241ps

Average 90% rising time of PMOS switch: 247ps

Average 90% falling time of PMOS switch: 253ps

Since the transition time of the gate control signal is very short, the average short-circuit current is sufficiently low. According to the transient simulation on H-bridge, although the instantaneous peak short circuit current is huge, which is around 1.5A and has sinusoidal shape, the short circuit current conduction time is very short, which is less than 100 ps. The average short circuit current can be calculated by Equation 5.5:

$$I_{sc\_rms} = \frac{I_{sc\_peak}}{\sqrt{2}} \times T_{conduct} \times f_{clk} \times \alpha \qquad \text{(Equation 5.5)}$$

Where I_{sc_rms} is the average short circuit current; I_{sc_peak} is the instantaneous peak short circuit current; $T_{conduct}$ is the short circuit conduction time; f_{clk} is the system clock frequency; α is the switching activity of the output stage. According to simulation and system setting, the exact value for each variable can be obtained:

I_{sc_peak} = 1.5 A

$T_{conduct}$ = 100 ps

f_{clk} = 5.6 Mhz

α = 1 (for worst case analysis, in real situation α is much smaller than 1)

The average short circuit current is calculated to be 0.594 mA for worst case scenario. In real situation, due to the adoption of 3-level switching SD modulator, the switching activity is greatly reduced and is much smaller than 1. Hence the real case average short circuit current is much less than the calculated value. Since the average short circuit current is small, no deadtime control circuit is required. This improves the THD performance; simplifies the gate driver design and reduces the power consumption of the gate driver.

5.3 Output LPF

The output waveform of the full H-bridge of a class D amplifier is high frequency square wave which containing audio signal information. A low pass filter (LPF) is required at the class D output stage to remove the unwanted high frequency component to restore the audio signal. Although all type of LPF can be used for this purpose, a LPF constructed by lossless component is preferred due to better power efficiency. Generally speaking, a LC LPF is a good choice for the class D amplifier output.

The output LPF for this design is the most commonly used second order LC low pass filter. A differential version of the LC LPF used because of the full H-bridge output stage. Since inductor and capacitor are lossless components, this LC LPF does not consume any power. Fig 5.4 shows the LPF with speaker. The speaker works as load to damp the circuit's inherent resonance.

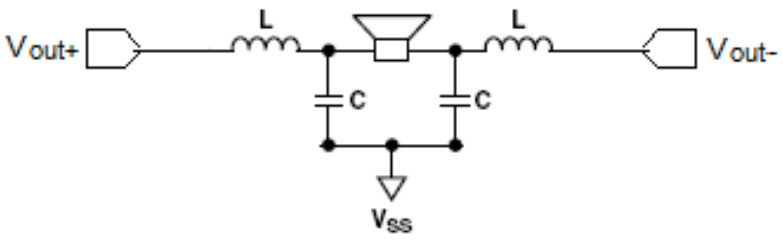

Fig 5.4: Differential version of LC LPF for Class D amplifier

Due to the oversampling nature of SD modulator, the pulse frequency is much higher than the audio frequency. In this design, a 64 or 128 OSR is used, which implies that the pulse frequency is at MHz range. More importantly, the high frequency power of SD modulator output is spread over a large frequency range in its output spectrum instead of a concentrated single tone. It is easier to be removed by the LPF. Therefore, although the second order LC LPF has finite attenuation in its stop band, the high frequency power remains in the filtered signal is unnoticeable as high frequency power is spread and it is very far from the audio signal band.

The LC filter in Fig 5.4 has flat frequency response in the audio band with 0 dB gain. Its attenuation after cut-off frequency is 40 dB/decade. Those two capacitors connected to ground provide low impedance path to ground for high frequency signal. The cut-off frequency of the LPF is normally set slightly higher than the audio bandwidth, usually between 30 kHz to 50 kHz.

$$L = \frac{R_L}{2\pi \cdot f_c} \qquad \text{(Equation 5.6)}$$

$$C = \frac{1}{(2\pi \cdot f_c)^2 \cdot L} \qquad \text{(Equation 5.7)}$$

$$Q = R_L \sqrt{\frac{C}{2L}} \qquad \text{(Equation 5.8)}$$

f_c is the desired cut-off frequency and R_L is the impedance of the speaker. Base on Equation 5.5 and 5.6, the inductance and capacitance value of the LC LPF can be obtained if speaker impedance and cut-off frequency are known. Q is the quality factor of a filter which is the ratio of the centre frequency to the filter bandwidth. A low Q produces an over damped curve and a high Q produces an under damped curve. The Q value for the output filter should be in the range of 0.6 to 0.8 to avoid underdamped or overdamped behaviour.

For a 4Ω speaker and 40 kHz cut-off frequency, desired L and C value is calculated and shown in table 5.1.

Table 5.1: Components value for the LPF

L (μH)	C (μF)	Q	R_L (Ω)	f_c (kHz)
15	1	0.73	4	42.44

As shown in table 5.1, the inductance and capacitance value of the LPF is too large to be integrated in the chip. Off-chip LPF is used in this design.

Chapter 6:
Measurement Results

The class D audio power amplifier designed in this project is fabricated in 0.35 μm CMOS technology. Fig 6.1 is the die photo of the fabricated chip. DIP44 packaging is used for the chip. Due to large output current requirement, several output pads are assigned to the PVSS, PVDD and H-bridge output to increase the current rating and reduce the parasitic resistance. A dedicated testing PCB is designed in Protel to estimate the performance of the class D amplifier design. Fig 6.2 shows the testing board including the DIP44 chip and the LC LPF.

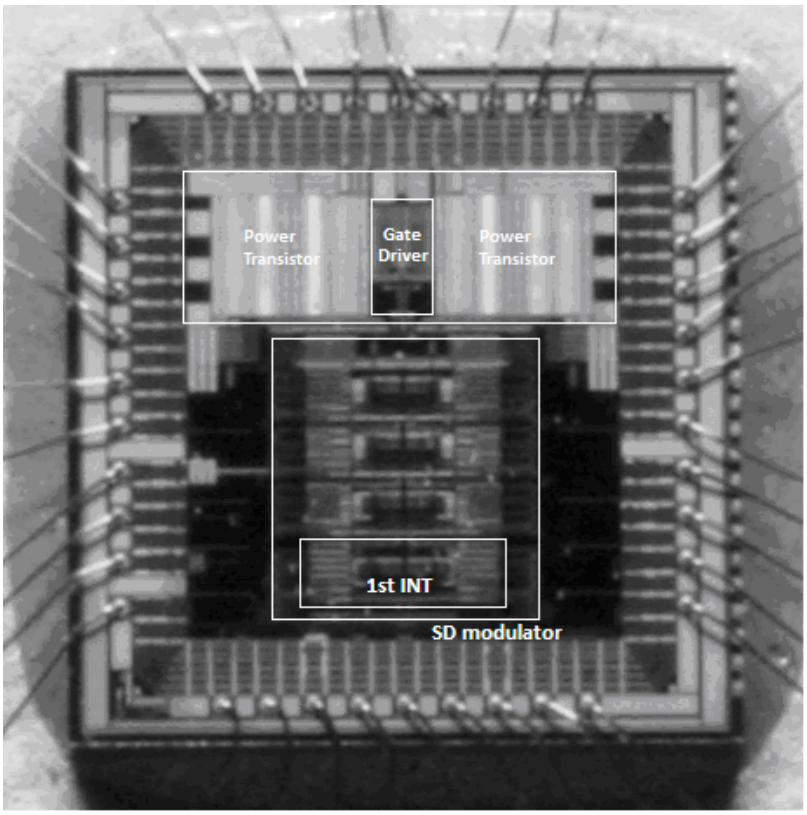

Fig 6.1: Die Photo

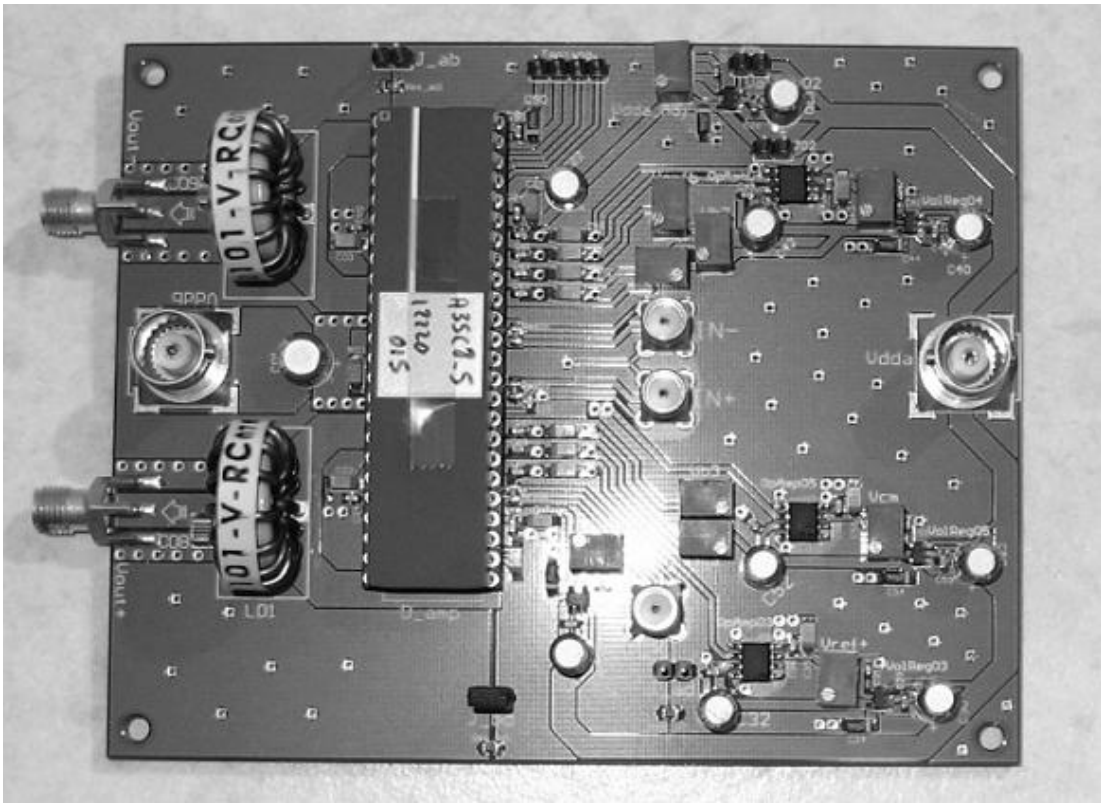

Fig 6.2: Photo of Testing PCB

The design of testing PCB is very important as it largely affects the testing results. Several LDOs (Low Dropout Voltage Regulator) are used in this test board to provide current with constant voltage. A lot of decoupling capacitors are connected to the power supply bus and constant voltage input in order to get clean and stable dc voltage. These decoupling capacitors are placed very close to the chip to reduce the path length and its parasitic inductance. This gives better filtering effect. A 50 Ω resistor is connected in between the input gate and the ground to maximize the power transfer from signal source to the input port. Very large track size and equal track length is used for the connection between the H-bridge output port and the LC LPF in

order to introduce balanced parasitic inductance, capacitance and resistance. Each pair of differential input tracks has identical geometrical structure. They also have equal track size and track length. Since the output of H-bridge is a high power high frequency pulse train, it will couple with other signals through the parasitic of the board and contaminate these signals. This greatly degrades the measurement results. Therefore, all sensitive signal tracks are shielded by guard ring connected to ground to reject the on-board high frequency noise. Ground plane is used in this testing board. This ensures all the signals has shortest path to assess ground. Apart from that, ground plane also provides shielding effect to improve the EMI performance of the class D amplifier. The test setup is placed in a metal box during testing in order to minimize noise injected from environment, especially the 50Hz noise which is in the audio band.

The schematic design of the testing PCB is shown in Fig 6.3 in next page. The output signal from LPF is measured by the oscilloscope and dynamic signal analyzer to evaluate the performance of this design. The average output current is recorded in different input signal level to estimate the output power and the overall power efficiency of this class D amplifier.

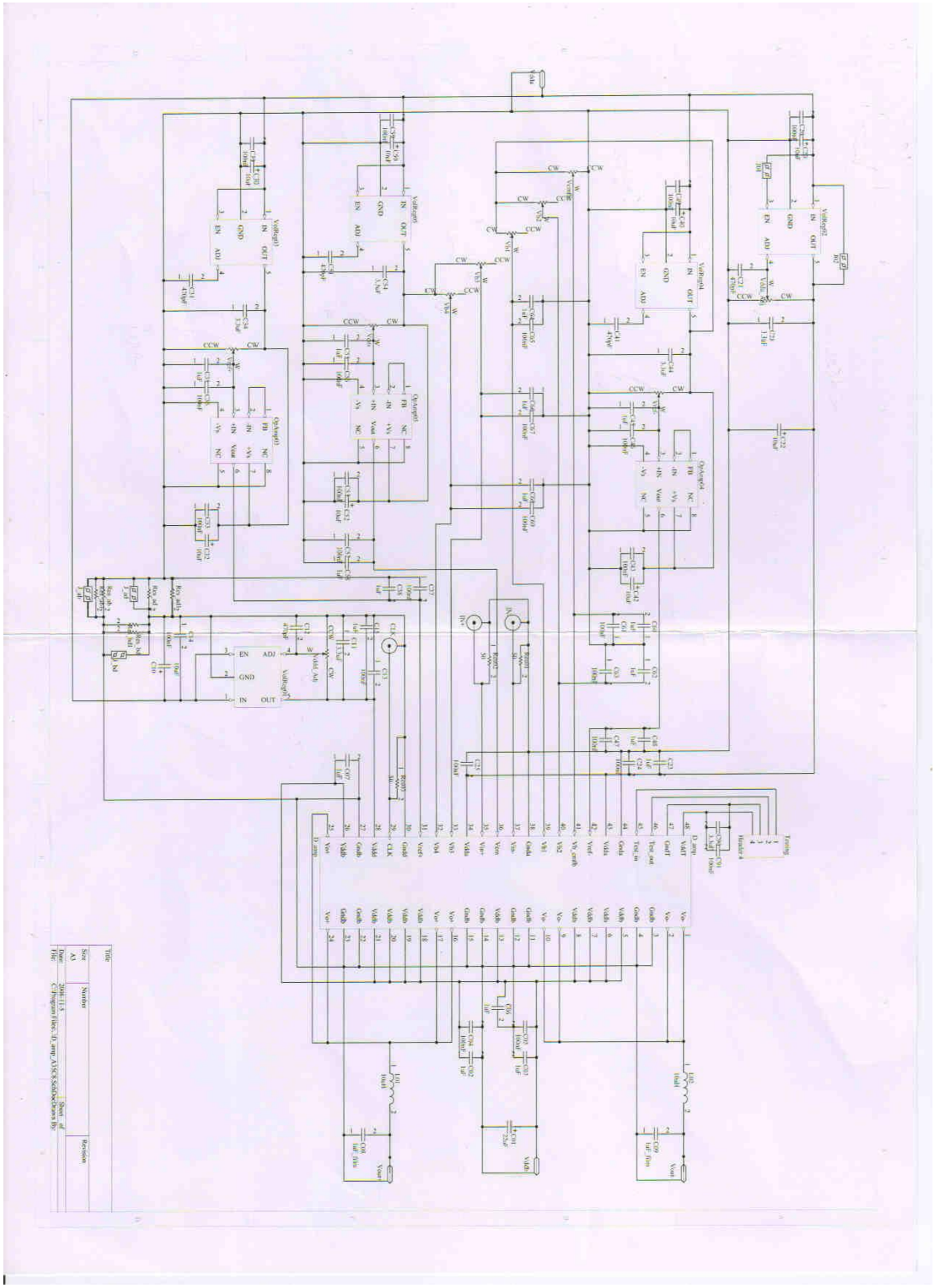

Fig 6.3: Schematic of testing PCB

6.1 H-Bridge output waveform comparison (simulation)

The following figures show the simulation results of output pulse train from H-bridge output stage with 1-bit and 1.5-bit quantization SD modulators in high output power and low output power respectively.

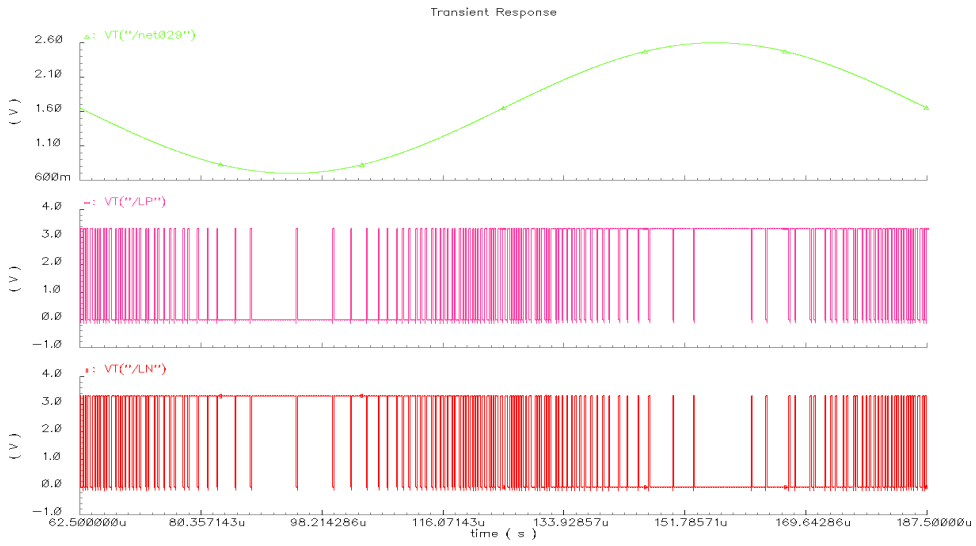

Fig 6.4: Output pulse train with 1-bit SD modulator at high output power

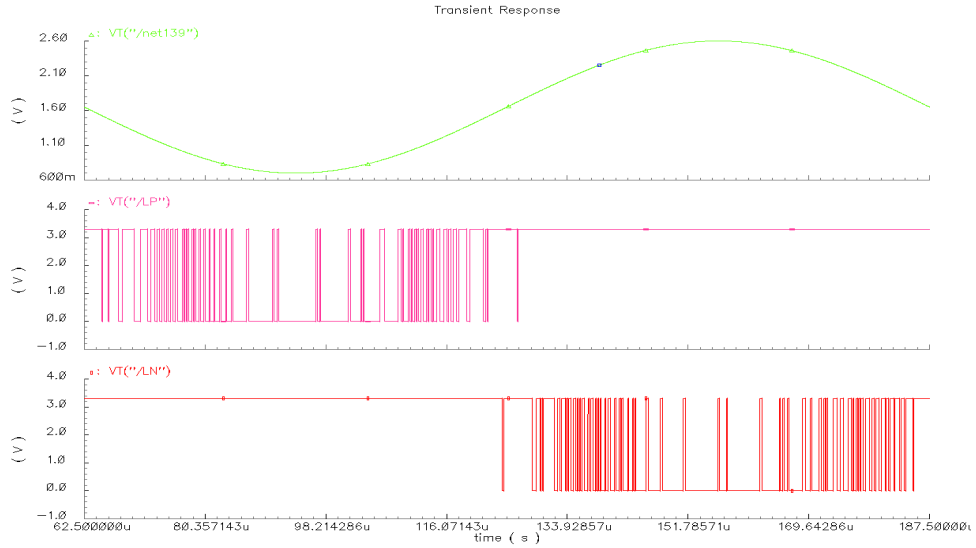

Fig 6.5: Output pulse train with 1.5-bit SD modulator at high output power

Fig 6.6: Output pulse train with 1-bit SD modulator at low output power

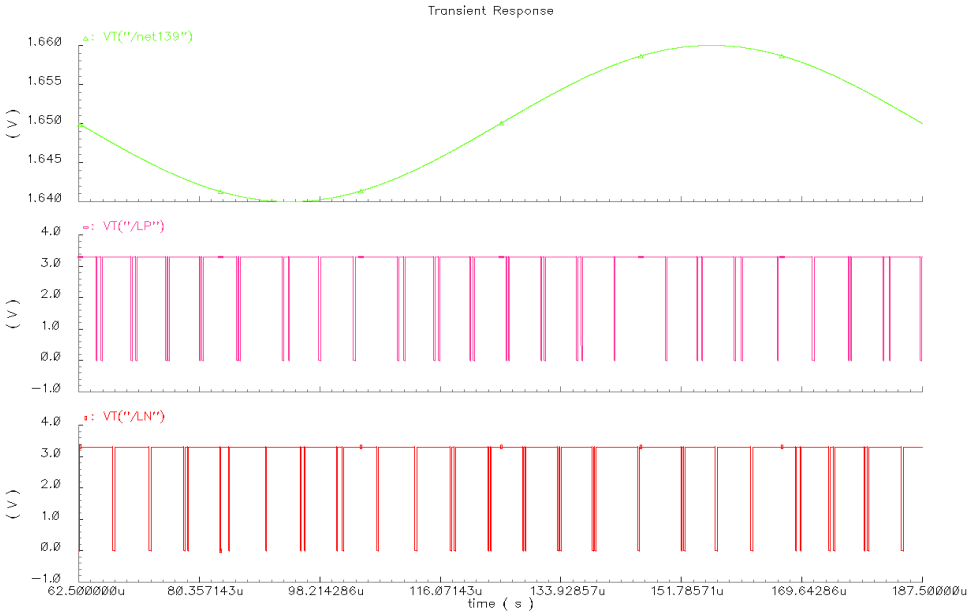

Fig 6.7: Output pulse train with 1.5-bit SD modulator at low output power

From these simulation results, one can confidently conclude that the switching activity of 1.5-bit quantizer SD modulator output is much lower than that of 1-bit quantizer SD modulator output, especially when the output power is low.

6.2 Output waveform

The output waveform of H-bridge output and LPF output are captured by oscilloscope. These output waveforms measured with and without a 4 Ω pure resistive load are shown in Fig 6.8 to Fig 6.11 in below.

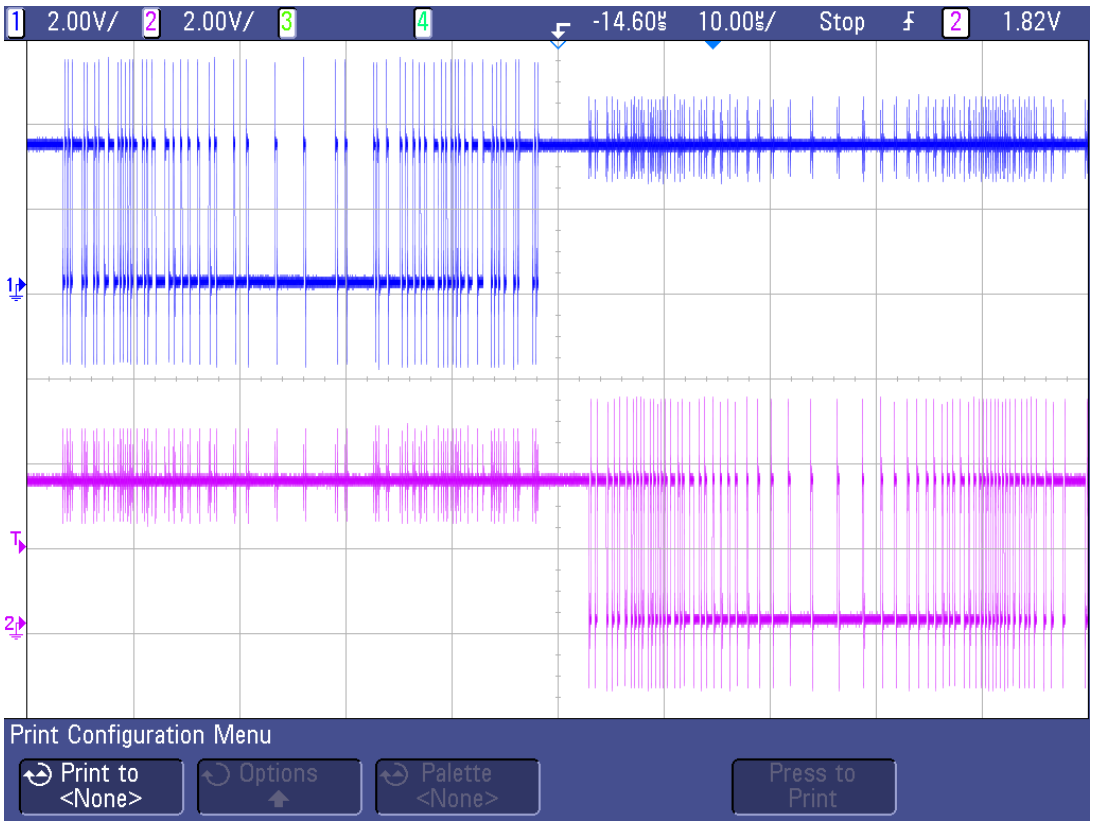

Fig 6.8: Output waveform of H-bridge without load

Fig 6.8 is the H-bridge output waveform without load when the input is a sinusoidal wave with high amplitude. It shows that the density of the output state varies with the input level. The output pattern is matched with the simulation result in Fig 6.5. The spikes in the output are due to the existence of parasitic inductance of the power supply bus. Very fast transition time of gate control signal for the output transistor induces a very fast changing output current. Since the inductor voltage is proportional to the gradient of output current, steep current slope makes the parasitic inductor voltage very high at the transition time, which eventually appears as spikes in the power supply bus.

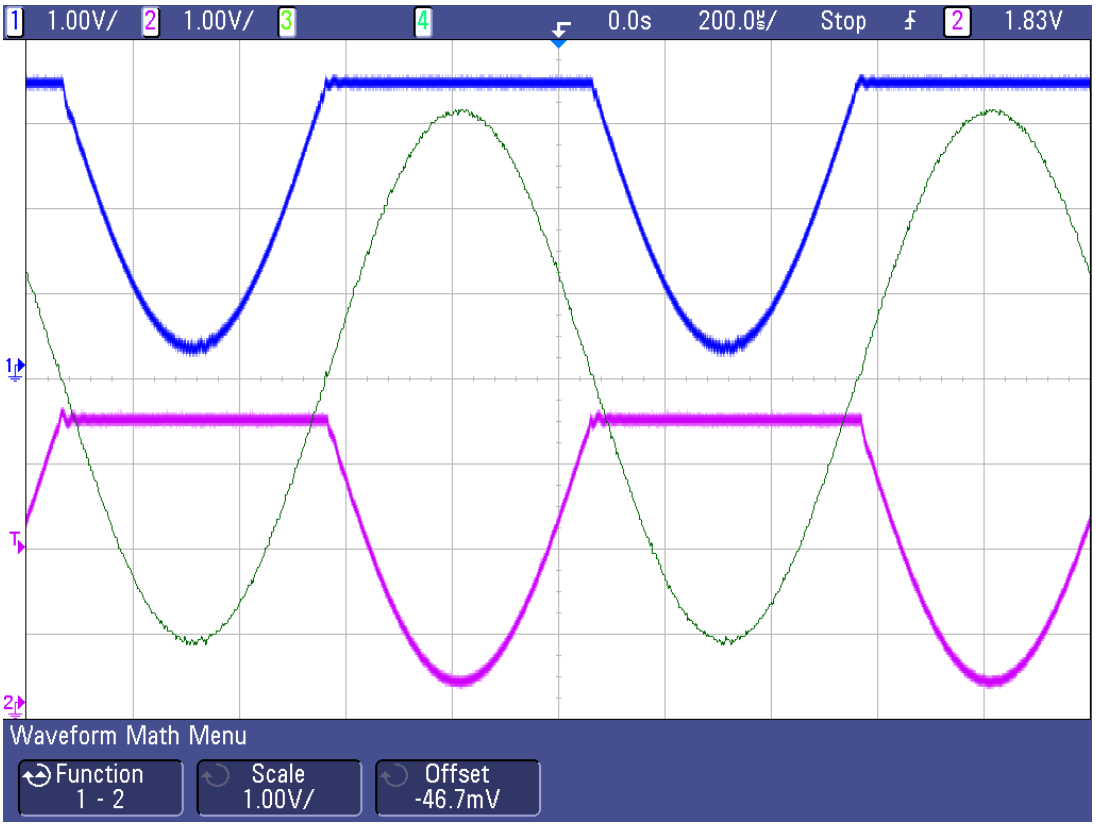

Fig 6.9: Output waveform of LC LPF without load

The blue and pink curves in Fig 6.9 are the signal waveforms from two output ports of differential LPF while the green curve is the signal waveform of differential output of LPF. It can be seen that the differential output from LPF is a sinusoidal wave with little distortion.

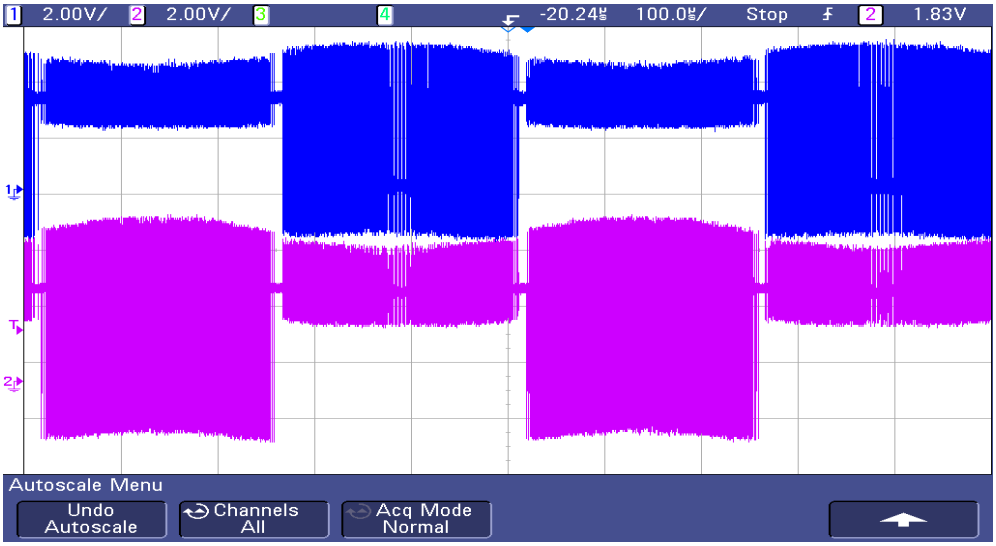

Fig 6.10: Output waveform of H-bridge with 4 Ohm load

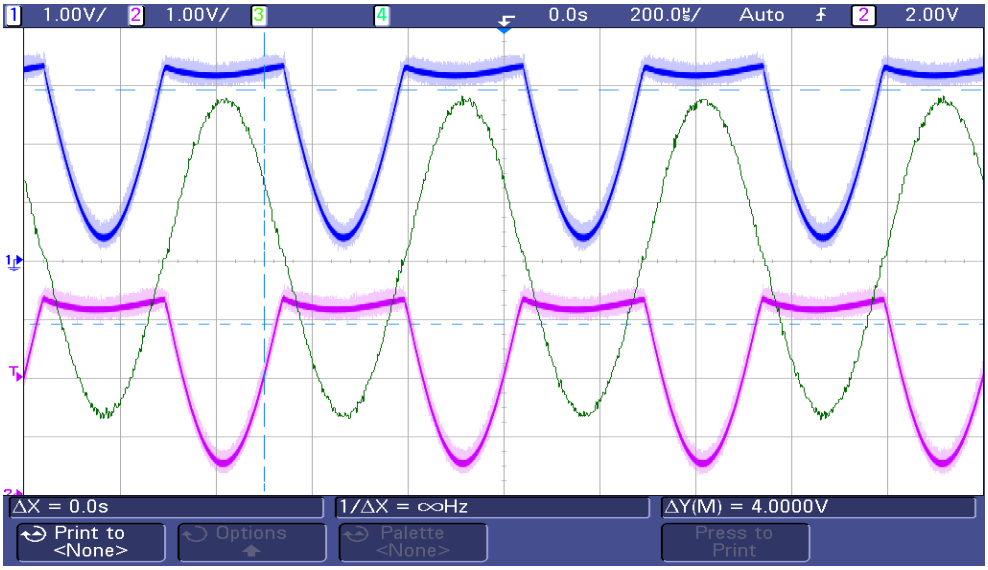

Fig 6.11: Output waveform of LC LPF with 4 Ohm load

Fig 6.10 and 6.11 show the signal waveform of H-bridge output and LPF output with a 4 Ω resistive load. They are slightly different from those without load. There is a very slight “amplitude modulation” type pattern at the H-bridge output waveform and a bend-down at the LPF output wave form. This phenomenon happens due to the existence of on-resistance of the power transistor during turn-on time. When the output current increase, current flows through the power transistor also increase and thus the voltage drop between source-drain of the transistor increase at the same time. Therefore, unlike the case without load, the H-bridge output can never reach Vdd or ground if there is an output current. Since the frequency of this “amplitude modulation” pattern is identical with the input audio signal and its magnitude is directly proportional to the input signal level, the distortion caused by the on-resistance induced “amplitude modulation” pattern is very low. According to [men00], the distortion introduced by this effect is less than 0.01%. The dynamic performance testing results verify this statement.

From these captured output waveforms, we can conclude that the class D audio amplifier designed in this project is functioning well. Its detail performances such as linearity, dynamic range, power supply rejection ration and overall power efficiency are evaluated in the later part of this chapter.

6.3 THD+N performance

Linearity is one of the most important indicators that evaluate the performance of an audio amplifier. The amplifier with high linearity gives high quality of sound. THD+N (Total harmonic distortion plus noise) measures linearity as well as the noise performance of an amplifier. It is the ratio between total power of harmonic distortion plus noise power within the audio band and the signal power.

Dynamic signal analyzer is utilized for the THD+N analysis. The differential output signal of LPF is captured and Fast Fourier Transform (FFT) is applied to the collected data. Signal in time domain is converted into frequency domain inside the dynamic signal analyzer and output power spectrum is produced by this process. The power of signal and its distortion at different frequency can be viewed in the output power spectrum. Fig 6.12 in next page shows the output spectrum at 0.16 of full scale output power with 2 kHz input signal.

After that, the data calculated by the dynamic signal analyzer is imported into MatLab. Total signal power and total noise and distortion power can be obtained from the output spectrum data. Hence, THD+N value can be calculated. The THD+N

performance over different output power with 2 kHz input frequency of the designed class D amplifier is shown in Fig 6.13.

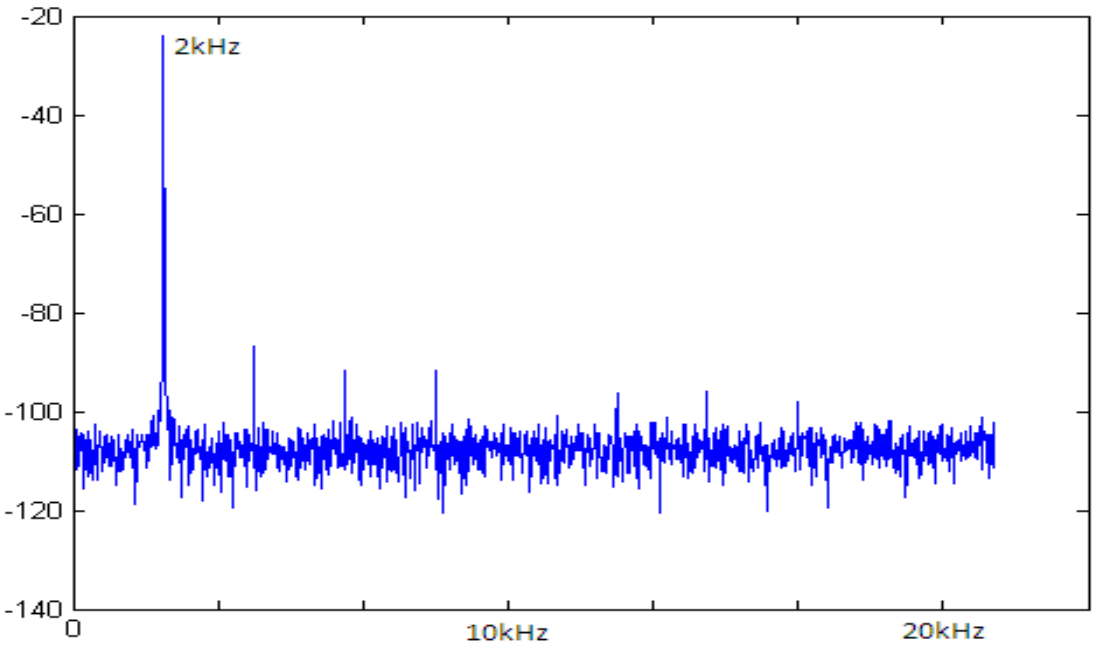

Fig 6.12: Output spectrum of LPF with 4 Ohm load at 0.16FS output power

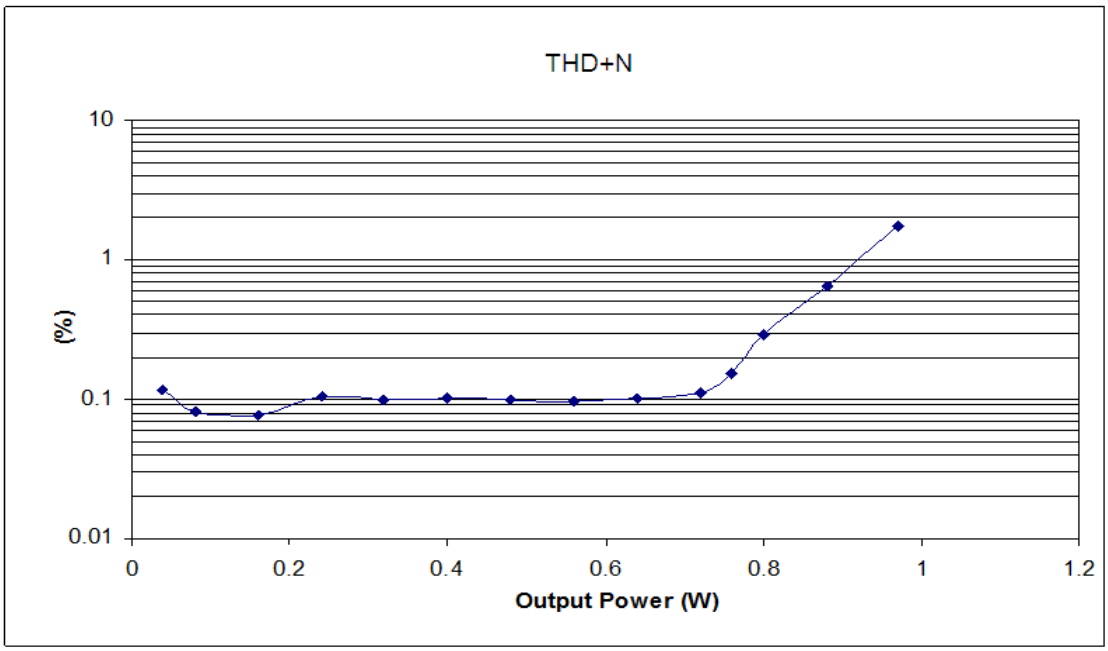

Fig 6.13: THD VS Output power of designed class D amplifier with 2 kHz input

As shown in Fig 6.13, the lowest THD+N is less than 0.08% located at very low output power around 0.1 W to 0.2 W. THD+N of this design is pretty constant around 0.1% across wide range of output power, from 0.1 W to 0.75 W. After 0.75 W the output distortion starts to increase as the output signal is approaching to saturation. The maximum output power is 0.97 W with 1.732% THD+N. The SFDR performance is determined by the signal power and 2nd harmonic power. It is in between -65dB to -70 dB and pretty constant for the output range where THD+N is 0.1%.

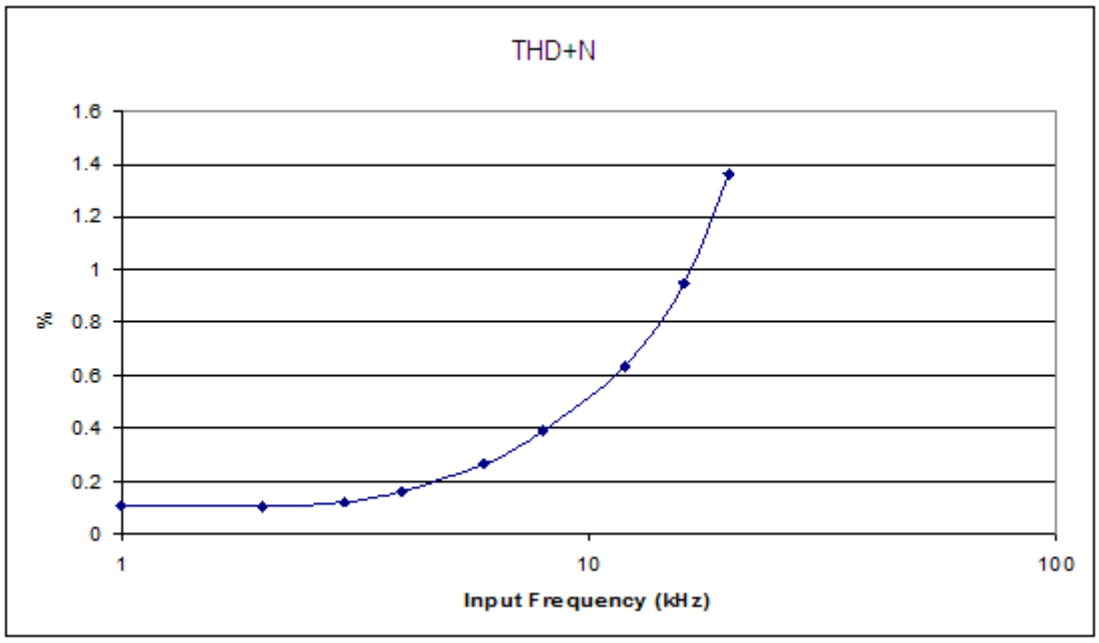

Fig 6.14: THD VS input frequency of designed class D amplifier

Fig 6.14 shows the linearity of the class D amplifier at different audio input frequency. The THD+N is around 0.1% and it is quite constant at low input frequency from 1 kHz to 3 kHz. The linearity is getting poor when the input frequency increases.

6.4 Output Dynamic Range

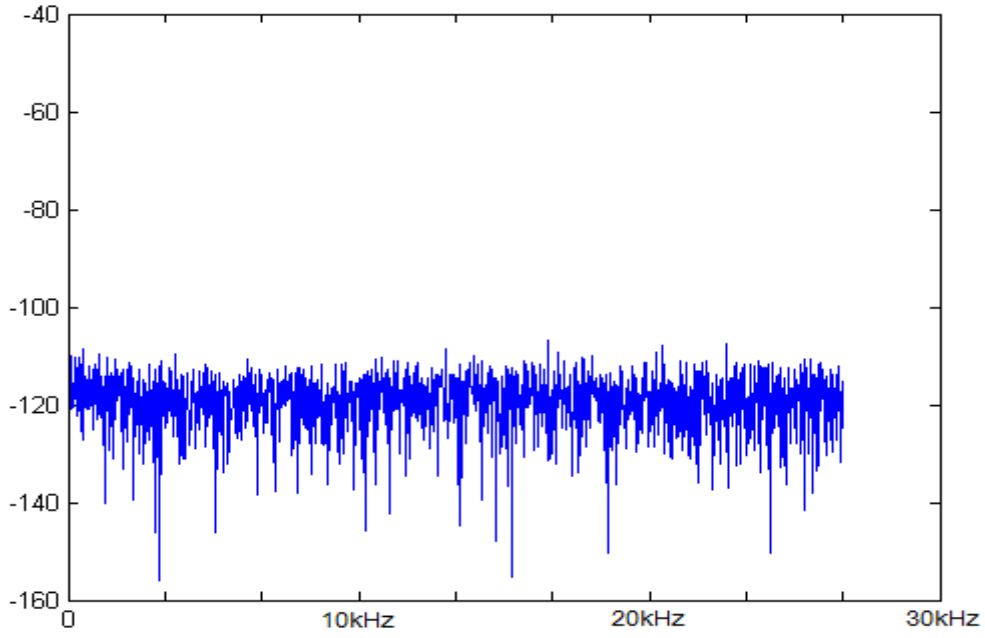

Fig 6.15: Noise floor of LPF output within audio band

Output dynamic range is the range between smallest and largest output level:

$$DR = 20 \times \log_{10} \frac{V_{O\max\_rms}}{V_{O\min\_rms}} \qquad \text{(Equation 6.1)}$$

The lower limit of useful signal is the output noise level while the upper limit of useful signal is the undistorted maximum output level. It can be seen that from Fig 6.15, the noise floor of the LPF output is at -110dB. The measured maximum achievable undistorted output power is at -16dB. Therefore, the output dynamic range of this class D amplifier is 94dB.

6.5 PSRR

Power supply rejection ratio (PSRR) is another important performance meter of audio amplifier. It measures the output signal dependency on the power supply voltage. Large PSRR is desired for audio amplifier. Audiophile-grade sound quality criteria for PSRR requirement is PSRR > 60 dB.

All the linear audio power amplifiers have high PSRR. However, the PSRR for a class D amplifier is small due to the low impedance path from power supply to the H-bridge output. The PSRR issue in this design is addressed by applying negative feedback from H-bridge output to the loop filter input. The effect of power supply variation is suppressed by the loop filter and hence, PSRR increase.

In the PSRR measurement, a 101 Hz sinusoidal with 3.3 V DC voltage waveform power supply is used for H-bridge output stage. A 1 kHz, 0.1 of full scale sinusoidal is applied to the amplifier input. The voltage supply ripple measured at H-bridge power input pin is 400 mV peak-to-peak. The output signal is analyzed by dynamic signal analyzer. The signal power shown at 101 Hz frequency in output power spectrum is obtained and compared with the 101 Hz signal amplitude at the power supply bus. The ratio between these two signals power is the PSRR of the class D

amplifier, as shown in Equation 6.2. Choosing 101 Hz frequency is because the power supply noise in real life is usually from 100 Hz to 120 Hz [Cha08].

$$PSRR = \frac{P_{vdd@101Hz}}{P_{out@101Hz}} \qquad \text{(Equation 6.2)}$$

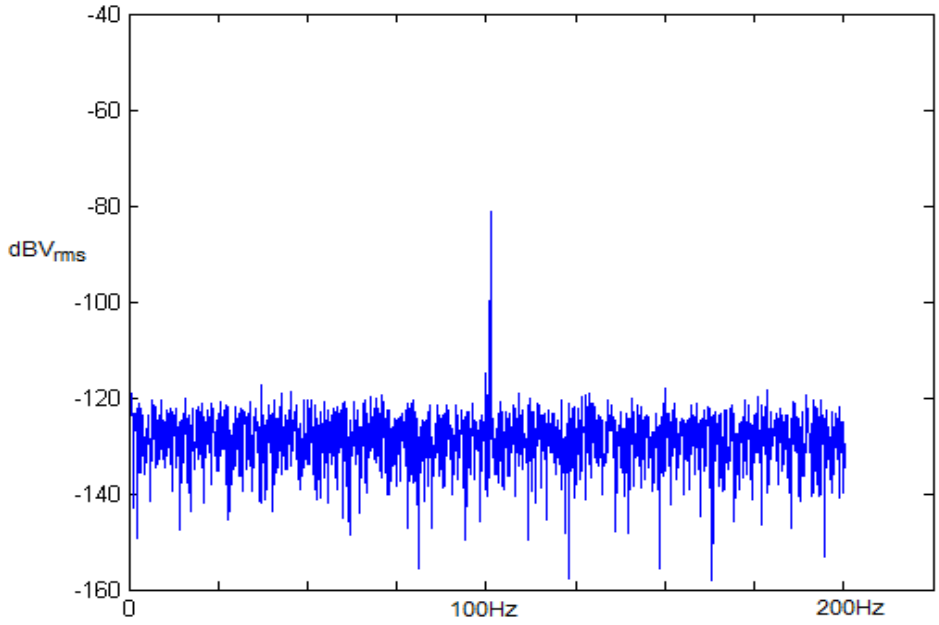

Fig 6.16: Output power spectrum with 101Hz supply noise

As shown in Fig 6.16, the output power at 101 Hz is -81.8 dBVrms. A 400 mV peak-to-peak sinusoidal wave has -16.99 dBVrms. Therefore, the PSRR can be calculated as:

PSRR= -16.99 – (-81.8) = 64.81 dB

The PSRR value for this class D amplifier is 64.81 dB.

6.6 Overall power efficiency

Power efficiency is the ratio between output power and total input power. Total power input power includes output power, power consumed by SD modulator and other circuit, power loss due to switching, conduction and short-circuit. In this testing, the sinusoidal output voltage waveform is captured and the average value of total input current is read from digital multi meter. The output power and input power can be calculated by:

$$P_{out} = \frac{V_{out\_rms}^2}{R_L} \qquad \text{(Equation 6.3)}$$

$$P_{in} = I_{tot\_avg} \times V_{dd} \qquad \text{(Equation 6.4)}$$

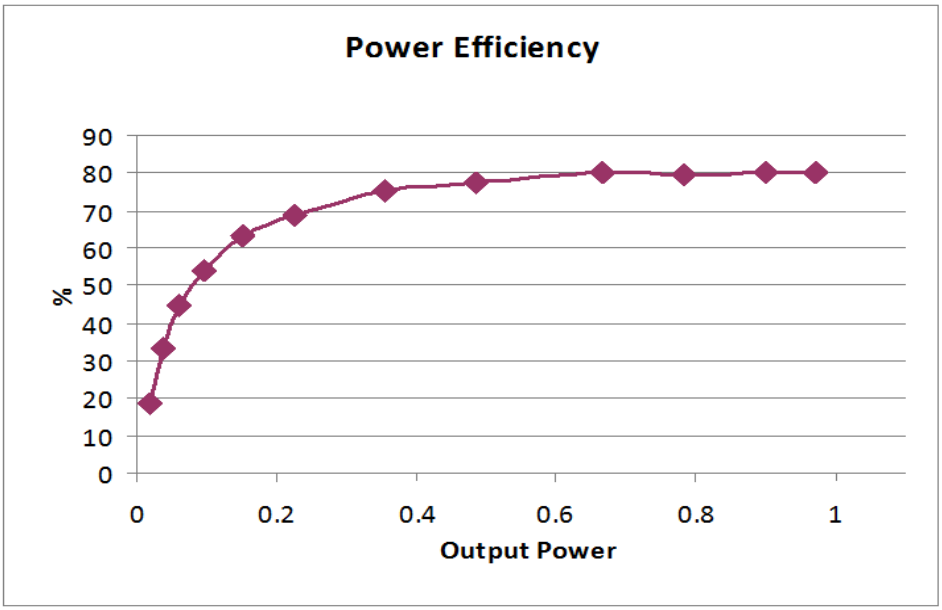

Fig 6.16: Power efficiency with 4 Ohm load @ 3.3V supply

Fig 6.16 shows the power efficiency of this class D amplifier at different output power. Its maximum power efficiency is 80% when the output power is high. This value is smaller than the design value. The main reason is the on-resistance of power transistor measured in real chip is about 10% to 20% higher than that in the transistor level simulation. This is probably due to process variation in fabrication such as shifting of transistor threshold voltage. It is not surprised that the power efficiency at low output power is low. This is because the SD modulator and gate driver dissipate constant power regardless of the output power. Their percentage increases if the output power drops.

6.7 Conclusion

The class D amplifier design is fabricated and a testing PCB is built. Three sample chips are tested. They have very close performance in different aspects. This shows the robustness of the design. Real testing data show that most of the performances of the chip meet the design specifications. The power efficiency meets the design specification marginally and the maximum output power is slightly lower than the specification. Table 6.1 summarizes the performance of the tested chip and the initial design specifications.

Table 6.1: Summary of measurement results

	Design Spec	Measurement
Power Supply Range	3.3 V	2.4 V to 4.5 V
Load	4 Ω to 8 Ω	4 Ω
Quiescent Current	<10 mA	5.56 mA
Dynamic Range	>90 dB	94 dB
PSRR @ 101Hz	>60 dB	64.8 dB
THD+N @ 0.1W	<0.1%	0.0817%
THD+N @ 0.97 W (Max Output Power)	-	1.732%
Output power @ 1% THD	-	0.924 W
Maximum Output Power	1W	0.97W
Maximum Power Efficiency	>80%	80%
Active area	-	3.97 mm^2

The main advantage of this Class D amplifier design is that it achieves high power efficiency even at low output power. In Fig 6.16 we can see that this design has 65% power efficiency at 20% of full output power. And the power efficiency reaches the maximum at around 50% of full output power. This result is better than recent Class D amplifier research works in 0.35 um technology and in 3.3 V power supply domain. Fig 6.17 and Fig 6.18 show the power efficiency of the Class D amplifier designs in [Axh07] and [Cho06], which are fabricated in 0.35 um CMOS technology and powered by 3.3 V supply. Although both papers claim that the maximum power efficiency for the designs are around 80%, their power efficiency at low output power are lower than this design.

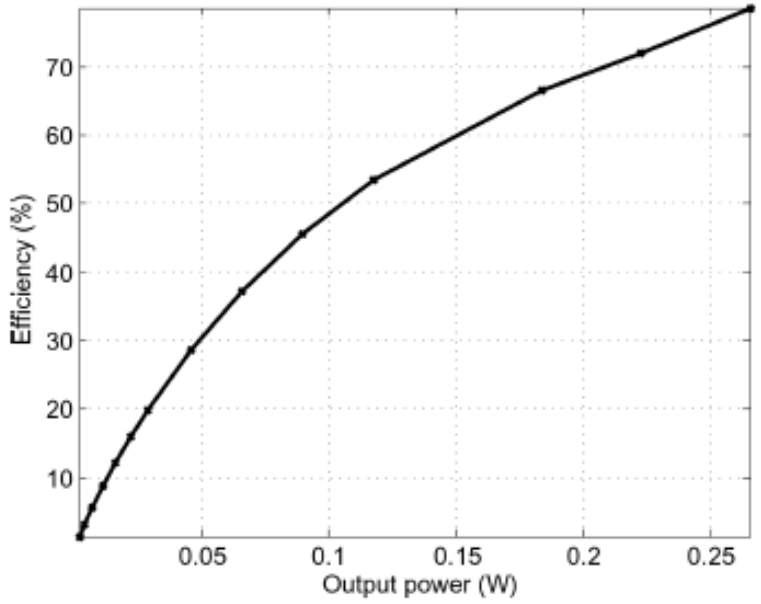

Fig 6.17: Power efficiency VS output power in Reference [Axh07]

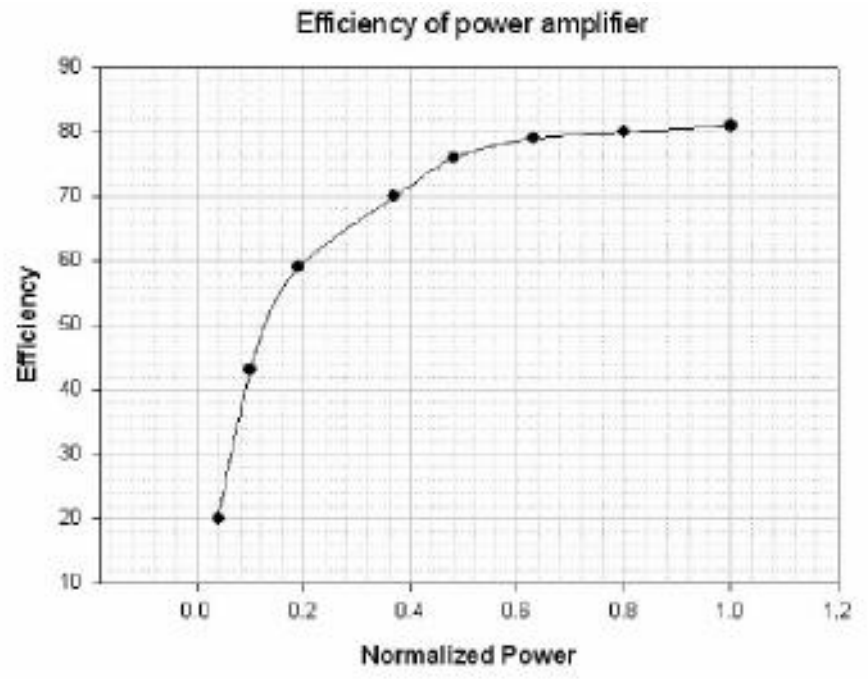

Fig 6.18: Power efficiency VS output power in Reference [Cho06]

High power efficiency in low output power is very important for portable audio application. The probability of portable audio devices running in low and mid output power is higher than the probability of portable audio devices running in high output power. High power efficiency in low output power allows portable audio devices have better batteries life time. This advantage of this design is mainly due to the adoption of 3-level switching scheme in SD modulator design. It greatly reduces the switching activity of the H-bridge output stage, especially at low output power (refer to Fig 3.12). Since the switching loss is the main power loss at low output power, reducing switching activity effectively reduce the switching loss and hence the power efficiency at low output power is improved.

Table 6.2 summarizes and compares the performances of this design and the state-of-the-art class D amplifier designs in order to have a clearer view on how this research work is done.

Table 6.2: Performance Comparison

Reference/ Year	Process/ supply	Active area (mm sqrt)	Output load (Ω)	Max output power (W)	Efficiency (%)	Min THD+N (%)
[Var03]/2003	0.18um/1.8V	0.3	4.3	-	76	0.07
[Kao06]/2006	0.35um/1.5V	-	600	-	90	0.27
[Kyo08]/2008	0.18um/3V	1.6	32	-	77	0.022
[Gro08]/2008	65nm/2.65V	0.278	8	0.53	76	0.025
[Axh07]/2007	0.35um/3.3V	2.88	16	0.25	76	0.5
[Kin08]/2008	0.35um/3.3V	2.55	7.5	1	80	0.15
This Work	0.35um/3.3V	3.97	4	0.97	80	0.082

The performance of Class D amplifiers vary from applications, technology, power supply voltage, power consumption, and etc. It is very difficult to make a fair comparison across them. Each design has its pros and cons. Compare to other designs listed in table 6.2, the design in this research work has high output power and high efficiency with moderate THD+N performance. However, its active area is largest mainly due to the lowest output load. The class D amplifier design in this research work demonstrates overall good performance compared to other designs.

Chapter 7: Conclusion

The research work on class D audio power amplifier design in 0.35 um CMOS technology is presented in this thesis. The background knowledge of class D amplifier is introduced in the first two chapters. System level design and circuit level design process of the SD modulator and output stage are discussed in chapter 3 and chapter 4. Three sample chips are tested and the testing results have been presented in the last chapter. The testing results show that this class D power amplifier design is robust and it meets most of the design specifications.

- **Suggestion of future work**

  Continuous time (CT) integrator can be used for 1st stage. This allows analog feedback directly from the H-bridge. By doing this, the feedback loop not only improves the PSRR, but also suppresses the distortion due to on-resistance of power transistor, timing error and errors due to process mismatch in the loop. Due to analog feedback from H-bridge, distortion introduced by deadtime can be suppressed. It is adviced to add a deadtime controller in the gate driving circuit. This can further increase the power efficiency of the class D amplifier.

Reference

[Nie97] K. Nielsen, “A review and comparison of pulsewidth modulation (PWM) methods for analog and digital input switching power amplifiers.” Presented at 102nd AES Convention, Munich, Germany, Mar 1997.

[Mos99] I.D. Mosely, P.H. Mellor and C.M. Bingham, “Effect of dead time on harmonic distortion in class-D audio power amplifiers”, Electronics Letters, 10th June 1999, Vol.35 No.12.

[Put03] B. Putzey, “Digital Audio’s Final Frontier,” IEEE spectrum, Vol. 40, pp.34-41, March 2003.

[Pel97] Peluso, V.; Marques, A.; Steyaert, M.; Sansen, W. “Optimal parameters for single loop ΔΣ modulators” Circuits and Systems, 1997, ISCAS '97. Proceedings of 1997 IEEE International Symposium on Volume 1, 9-12 June 1997 Page(s):57 - 60 vol.1

[Bai94] Baird, R.T.; Fiez, T.S. “Stability analysis of high-order delta-sigma modulation for ADC's” Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions Volume 41, Issue 1, Jan. 1994 Page(s):59 – 62

[Sil01] J. Silva, U. Moon, J. Steensgaard and G.C. Temes. “Wideband low-distortion delta-sigma ADC topology” Electronics Letters 7th June 2001 Vol.37 No.12

[Can85] J.C.Candy, “A use of double integration in sigma delta modulation”, IEEE Trans. Commun, Vol. COM-33, No.3, Mar 1985, pp. 249-258

[Yao05] Libin Yao, Low-Power Low-Voltage Sigma-Delta A/D Converters In Deep Submicron CMOS, PhD thesis, Leuven, 2005

[San99] W. Sansen, “Distortion in elementary transistor circuits”, IEEE Transactions on Circuits and Systems—Part II: Analog and Digital Signal Processing, 46:315 – 325, March 1999.

[Mar99] A. Marques, High Speed CMOS Data Converters, Ph.D. thesis, ESAT–MICAS, K.U.Leuven, Belgium, 1999.

[Jor03] Jorge Varona, Anas A, Hamoui, Ken Martin; “A Low-Voltage Fully-Monolithic Delta-Sigma Based Class-D Audio Amplifier”

[Men00] Meng-Tong Tan; Hock-Chuan Chua; Bah-Hwee Gwee; Chang, J.S.; “An investigation on the parameters affecting total harmonic distortion in class D amplifiers” Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on Volume 4, 28-31 May 2000 Page(s):193 - 196 vol.4

[Kyo08] Kyoungsik Kang; Jeongjin Roh; Youngkil Choi; Hyungdong Roh; Hyunsuk Nam; Songjun Lee; “Class-D Audio Amplifier Using 1-Bit Fourth-Order Delta-Sigma Modulation “; Circuits and Systems II: Express Briefs, IEEE Transactions on Volume: 55 , Issue: 8; Publication Year: 2008 , Page(s): 728 – 732

[Axh07] Axholt, A.; Oredsson, F.; Petersson, T.; Wernehag, J.; Sjoland, H.; “A 0.25W fully integrated class-D audio power amplifier in 0.35μm CMOS”; Norchip, 2007; Publication Year: 2007 , Page(s): 1 – 4

[Dap00] D. Dapkus, “Class-D audio power amplifiers: An overview,” Consumer Electronics (ICCE) 2000, pp.400-401

[Ber03] M. Berkhout, “An integrated 200-W class-D audio amplifier,” IEEE Journal of Solid-State Circuit, 2003, 38, (7), pp.1198-1206

[Cha08] T. Ge and J.S.Chang, “Modeling and technique to improve PSRR and PS-IMD in analog PWM class D amplifiers,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 55, no. 6, pp. 512-516, Jun. 2008

[Var03] J. Varona, A. A. Hamoui, and K. Martin, “A low-voltage fully-monolithic delta-sigma based Class-D audio amplifier,” in Proc. Eur. Solid-State Circuits Conf. (ESSCIRC), Sep. 2003, pp. 545-548

[Kao06] C. H. Kao, W. P. Lin, and W. C. Chen, “High efficiency and low distortion switching power amplifier for hearing aids,” Proc. IEE Circuits, Devices Syst., vol. 153, no. 2, pp. 143-147, Apr. 2006

[Gro08] Groeneweg. W. H., “Analog signal processing for a class D audio amplifier in 65 nm CMOS technology,” Solid-State Circuits Conf. 2008 (ESSCIRC), 34th Eur, pp. 322-325

[Kin08] Kin-Keung Lee, Yelin Wang, Qingyuan Zhang, Sjoland. H, “A 1W Class-D Audio Power Amplifier in a 0.35um CMOS Process,” Norchip 2008, pp. 172-175

[Gaa05] E. Gaalaas, B. Y. Liu, N. Nishimura, R. Adams, and K. Sweetland, “Integrated stereo ΔΣ class D amplifier,” IEEE J. Solid-State Circuits, vol. 40, no. 12, pp.2388-2397, Dec. 2005

[Gha06] A. Gharbiya and D. A. Johns, “On the implementation of input-feed-forward delta-sigma modulators,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 6, pp. 453-457. Jun. 2006

[Cho06] Choi, B.K.; Hong, Y.U.; Kwak, T.W.; Lee, M.C.; Cho, G.H.; “High-frequency switching class-D power amplifier for portable sound applications,” Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE, 2006, pp. 1-4

Appendix

Publication List

Pan Junle, Yao Libin and Lian Yong; “A Sigma-Delta Class D Audio Power Amplifier in 0.35μm CMOS Technology” ISOCC 2008 Nov.