DEVELOPMENT AND CHARACTERIZATION OF

HIGH-K DIELECTRIC/GERMANIUM GATE STACK

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To Guo Qian

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ABSTRACT

Scaling of the gate stack has been a key to enhancing the performance of complementary metal-oxide-semiconductor (CMOS) field-effect transistors (FETs) of the past 40 years. However, as the metal-oxide-semiconductor field-effect transistors (MOSFET) continues to scale down to tens of nanometers, Si/SiO_2 based device is approaching its fundamental limits, the motivation for alternative gate stacks has increased considerably. High-k/Ge gate stack is very promising for future nanoscale devices because it improves the device performance in terms of both drive current and power consumption. The most important technical issue for high-k/Ge MOSFET technology is the passivation of the Ge surface.

In this study, two approaches to improve the high-k/Ge interface qualities were investigated. The first approach was using pre-gate surface passivation for high-k/Ge gate stack. Two pre-gate surface passivation techniques were investigated. The first one was the sulfur passivation. We found that the Ge diffusion was suppressed by introducing sulfur atoms at high-k/Ge interface, due to less GeO_x ($x < 2$) formation, and consequently, the interface trap density (D_{it}) was significantly reduced. However, device with sulfur passivation presented a large amount of hysteresis. The second one was silicon nitride passivation by SiH_4-NH_3 treatment. This was an improved version of Si passivation. We found that ultrathin silicon nitride layer was more effective to suppress the Ge diffusion

than ultrathin Si layer. Moreover, the unexpected positive threshold voltage shift was also eliminated by using silicon nitride passivation, which was attributed to the suppressing of interfacial dipole formation.

The second approach to improve the high-k/Ge interface quality is to adopt proper post-gate treatment processes. For the first time, we proposed and demonstrated a post-gate CF_4 plasma treatment process to incorporate fluorine (F) into high-k/Ge gate stacks. We found that F tends to segregate at high-k/Ge interface upon thermal annealing and both the interface quality and high-k bulk quality were significantly improved by F incorporation. This was attributed to the Ge-F and Hf-F bonds formation at interface and in the bulk high-k, respectively. The post-gate treatment was found to be compatible with pre-gate surface passivation. By applying both techniques on high-k/Ge gate stack, the optimum interface quality was able to be achieved.

Variable rise/fall time charge pumping method was also used to characterize the interface properties of Ge MOSFETs. We found that F passivation was capable to reduce interface traps that located in the both bottom half and upper half of the Ge bandgap. It was also observed that D_{it} distribution in Si passivated Ge MOSFETs was asymmetric with much higher density in the upper half of the Ge bandgap. Those traps can act as Coulomb scattering centers when the MOSFETs operate under inversion, which can be possible cause of severe electron mobility degradation for Ge nMOSFETs.

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List of Symbols

χ	Electron affinity of a semiconductor
ε_0	Permittivity of free space
ϕ	Electron barrier height
μ_e	Mobility of electron
μ_{eff}	Effective mobility
μ_h	Mobility of hole
σ_n	Capture cross section area of electron
σ_p	Capture cross section area of hole
ω	Angular frequency
ΔV	Frequency dependent flat-band voltage shift
A	Area
a	Lattice constant
C	Capacitance
C_{gb}	Gate to substrate capacitance per unit area
C_{gc}	Gate to channel capacitance per unit area
C_{inv}	Gate to channel capacitance under inversion per unit area
C_{min}	Minimum capacitance of a MOS capacitor
D_{it}	Density of interface states
E_c	Conduction band edge
E_{eff}	Vertical effective electric field in a MOSFET channel
$E_{em.e}$	Electron emission energy level
$E_{em.h}$	Hole emission energy level
E_F	Fermi level of a semiconductor
E_g	Energy bandgap of a semiconductor
E_i	Intrinsic Fermi level of a semiconductor

E_v	Valence band edge
f	Frequency
G_m	Transconductance of a MOSFET
G_p	Equivalent parallel conductance of an MOS capacitor
I_{cp}	Charge pumping current
I_d	Current through the drain
I_g	Leakage current through the gate electrode
I_{off}	Drain leakage when the MOSFET is off
I_{on}	Channel saturation current when the MOSFET is on
J	Current density
J_g	Gate leakage current density
k	Dielectric constant (relative permittivity)
k_{Ge}	Dielectric constant of Ge (relative permittivity)
$k_{high\text{-}k}$	Dielectric constant of high permittivity dielectric (relative permittivity)
k_{SiO_2}	Dielectric constant of SiO_2 (relative permittivity)
L	Gate length of a MOSFET
N_c	Effective density of states in the conduction band
n_i	Intrinsic carrier concentration in a semiconductor
$N_{scatter}$	Interface scattering density
N_{sub}	Substrate doping concentration
N_v	Effective density of states in the valence band
q	Electronic charge
Q_b	Depletion charge in the bulk per unit area
Q_{cp}	Recombined charge per cycle in the charge pumping measurement
Q_i	Inversion charge in the channel per unit area
R	Resistance
R_s	Series resistance

$t_{high\text{-}k}$	Physical thickness of high permittivity dielectric
t_{inv}	Capacitance equivalent oxide thickness in inversion
T_{m}	Melting point
T_p	Period of the gate pulse
t_f	Fall time of the gate pulse signal
t_{ox}	Equivalent oxide thickness
t_{poly}	Equivalent oxide thickness due to poly depletion effect
t_{qm}	Equivalent oxide thickness due to quantum mechanical effect of channel
t_r	Rise time of the gate pulse signal
V_{a}	Amplitude of gate pulse
V_{d}	Drain voltage
V_{dd}	Positive supply voltage
V_{ds}	Drain-source bias
V_{fb}	Flat band voltage
V_{g}	Gate voltage
V_{ox}	Voltage dropped on oxide
V_{th}	Threshold voltage
W	Gate width of a MOSFET
X	Reactance
x_{j}	Junction depth
Z	Impedance

List of Abbreviations

ALD	Atomic layer deposition
C-V	Capacitance — voltage characteristic
CET	Capacitance equivalent oxide thickness
CMOS	Complementary metal-oxide-semiconductor device
CP	Charge pumping
CVD	Chemical vapor depostition
DI	Deionized
EOT	Equivalent oxide thickness
FGA	Forming gas annealing
FUSI	Full silicidation
G_m-V_g	Transconductance-gate voltage characteristic
GOI	Germanium on insulator
HFCV	High frequency capacitance-voltage characteristic
I_d-V_d	Drain current — drain voltage characteristic
I_d-V_g	Drain current — gate voltage characteristic
IC	Integrated circuit
ICP	Inductively coupled plasma
IL	Interfacial layer
ITRS	International Technology Roadmap for Semiconductors
J-V	Leakage current-voltage characteristic
J_g-V_g	Gate leakage current-gate voltage characteristic
LCR	Inductance (L), Capacitance (C), and Resistance (R)
MOCVD	Metalorganic chemical vapor deposition
MOS	Metal-oxide-semiconductor device, usually the MOS capacitor
MOSFET	Metal-oxide-semiconductor field-effect transistor

nMOS	n-type MOS device
nMOSFET	n-type channel MOSFET
PDA	Post deposition annealing
PMA	Post metal annealing
pMOS	p-type MOS device
pMOSFET	p-type channel MOSFET
PVD	Physical vapor deposition
QMCV	Quantum mechanical capacitance voltage
RF	Radio frequency
RTP	Rapid thermal processing
S/D	Source drain
SIMS	Secondary ion mass spectroscope
SS	Substreshold swing
UHV	Ultra high vacuum
UTB	Ultrathin body
UV	Ultraviolet
XPS	X-ray photoelectron spectroscopy
XTEM	Cross-section transmission electron microscopy

Chapter 1

Introduction

1.1. Challenges of MOSFETs scaling and possible solutions

The success of the semiconductor industry relies on the continuous improvement of integrated circuit (IC) performance by reducing the dimensions of the key component of these circuits: the metal-oxide-semiconductor field effect transistor (MOSFET). Indeed, the reduction of device dimensions, or scaling, allows the integration of a higher density of transistors on a chip, enabling higher switching speed and reduced costs. The scaling of MOSFET device was originally predicted by Intel co-founder Gordon E. Moore, in 1965 [1]. Moore's law describes a long term trend in the history of computing hardware, in which the number of transistors that can be placed inexpensively on an integrated circuit has doubled approximately every two years[*]. The key concept of the MOSFET scaling proposed by Dennard *et al.* in 1974 [2] is that various structure and electrical parameters of MOSFET (such as gate length, gate width, gate thickness and power supply voltage) should be scaled in concert, which guarantees the reduction in device dimensions without compromising the current-voltage characteristics. However, as the MOSFET continues to scale down to tens of nanometers, this conventional device scaling

[*]Although originally calculated as a doubling every year [1], Moore later refined the period to two years. It is often incorrectly quoted as a doubling of transistors every 18 months, as David House, an Intel Executive, gave that period to chip performance increase. The actual period was about 20 months.

scheme has confronted the difficulty that the three main indexes associated with MOSFET performance: short-channel effects, on current (I_{on}) and power consumption have the tradeoff relationships between each other, owing to several physical and essential limitations directly related to the device miniaturization (e.g. to maintain the I_{on} scaling, SiO_xN_y with equivalent oxide thickness (EOT) ~ 1 nm has to be used for 45 nm node technology, but this will cause greater power consumption in terms of high gate leakage current). The schematic diagram of this tradeoff relationship is shown in Fig. 1.1 [3].

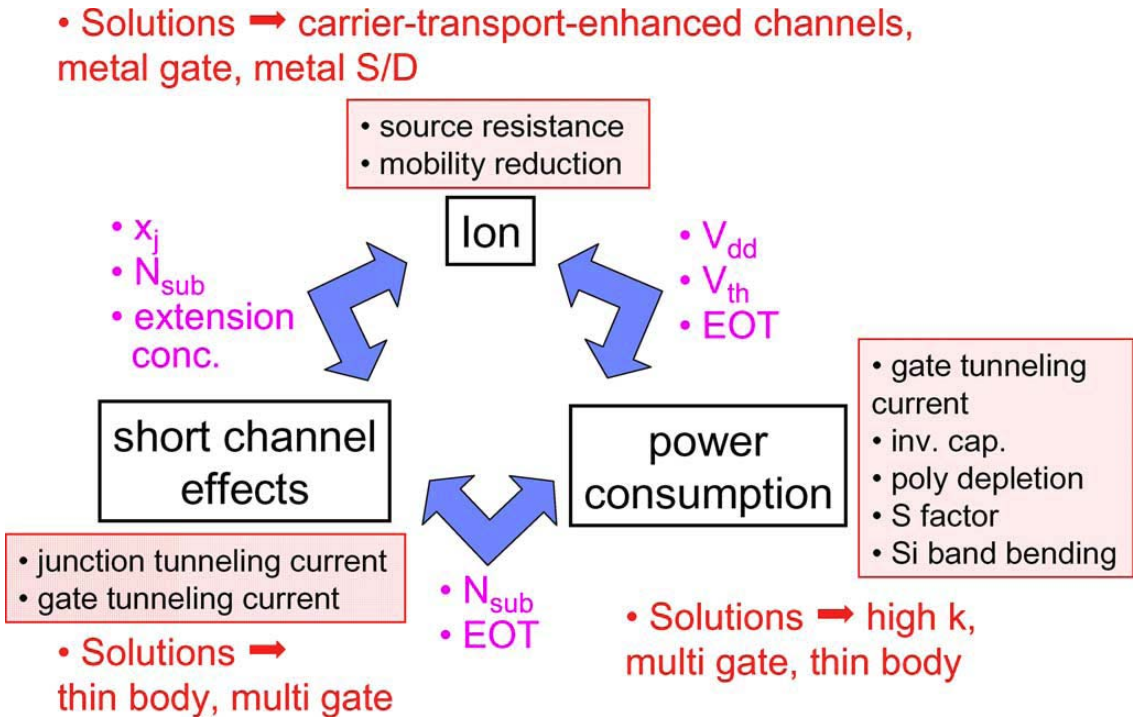

Fig. 1.1. Tradeoff factors among short-channel effects, on current (I_{on}) and power consumption under simple device scaling and possible solutions to mitigate the relationship. Critical device or physical parameters to provide the tradeoff, such as power-supply voltage V_{dd} and threshold voltage V_{th}, are shown between the two indexes, and also, the physical mechanisms causing the tradeoffs are shown inside the boxes [3].

Consequently, to continue the MOSFET scaling in the future, novel device technologies or new materials that simultaneously satisfy the high performance and low

power consumption under healthy device characteristics against these physical limitations are strongly desired to overcome these challenges or to mitigate these stringent constraints in the tradeoff relations. A group of these novel device technologies or new materials have been proposed to solve the ultimate scaling issues for future MOSFET, including high-k/metal-gate, high carrier mobility or high carrier velocity channels, ultrathin-body (UTB) structures, multigate structures, and metal source/drain, which are called the technology boosters in the International Technology Roadmap for Semiconductors (ITRS) [4]. The basic principle of these technology boosters is to boost or improve a specific device parameter like the gate leakage current, mobility, short-channel effects, and so on.

In this thesis, we focus on the gate stack engineering, because gate stack technology is the key driver for MOSFET scaling. The advanced gate stacks must fulfill both requirements of low power consumption and high performance. Therefore, the introduction of high-k materials for gate dielectrics and high carrier mobility material for channels is of paramount importance.

1.2. High-k gate dielectrics

1.2.1 Limits of SiO_2 scaling

The excellent material and electrical properties of thermal SiO_2 allowed the successful scaling of Si-based MOSFETs in the twentieth century. Properly working MOSFETs with SiO_2 gate layer as thin as 1.5 nm has been reported [5, 6]. However, further scaling of SiO_2 gate layer thickness is problematic. The first problem is the

concern of high leakage current flowing through the metal-oxide-semiconductor (MOS) structure. For the ultrathin SiO_2 gate layer (< 3 nm), charge carriers can flow through the gate dielectric by the direct tunneling mechanism [7] as illustrated in Fig. 1.2 [8]. It has been shown that the tunneling probability increases exponentially as the thickness of the SiO_2 layer decreases [7, 9]. As shown in the Fig. 1.2, the leakage current density exceeds 100 A/cm^2 at V_{ox} = 1V in a 1 nm thick SiO_2 layer (V_{ox} is the potential drop across the dielectric layer). It also can be seen from this figure that the SiO_2 layer thickness scaling is limited by the leakage current specifications from ITRS. SiO_2 gate dielectric is not suitable for 80 nm technology and below because the EOT requirement of 80 nm node and below is less than 1.4 nm for high performance logic and 1.7 nm for low operating power and the leakage current densities of the SiO_2 layers with those thickness will exceed the maximum leakage current specifications.

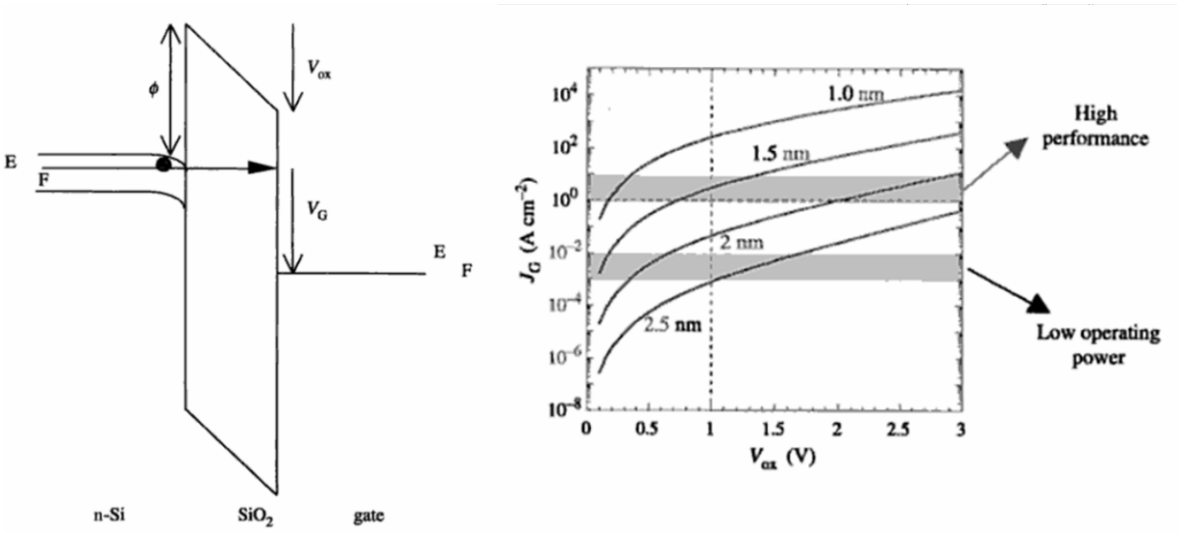

Fig. 1.2. (Left) Schematic energy band diagram of an n-Si/SiO_2/metal gate structure, illustrating direct tunneling of electrons from the Si substrate to the gate. ϕ is the energy barrier height at the Si/SiO_2 interface, V_{ox}, the potential drop in the SiO_2 layer and V_G, the applied gate voltage. (Right) Simulated tunneling current through a MOS as a function of the potential drop in the gate oxide, V_{ox}, for different SiO_2 gate layer thickness. Shaded areas represent the maximum leakage current specified by the ITRS for high performance and low operating power application, respectively.

Another issue arising from SiO_2 scaling is boron penetration through the gate dielectric. Upon thermal annealing, the boron from heavily doped poly-silicon gate can easily diffuse through the thin SiO_2 layer into substrate. This will cause unexpected threshold voltage shift and reliability issues [10]. Actually, to tackle the gate leakage and boron penetration issues, in most aggressive high performance technologies, SiO_xN_y is used as gate dielectric. SiO_xN_y has a dielectric constant ~7, which is higher than SiO_2, thus a larger physical thickness is allowed to achieve the same EOT. In addition, introduction of nitrogen into SiO_2 greatly reduces the boron diffusion benefited from the Si-O-N networking bonds formed in SiO_xN_y [11]. In this case, SiO_xN_y dielectric layer with EOT as thin as 1.1 nm still exhibits acceptable leakage current and amount of boron penetration, extending the scaling limit to 45 nm technology node. However, for sub-45 nm technologies, SiO_xN_y will not be used as gate dielectric since sub-1 nm EOT is necessarily required and SiO_xN_y can no longer fulfill the gate leakage requirement.

1.2.2 Alternative gate dielectrics

The MOS structure actually behaves like parallel plate capacitors. The capacitance density at strong inversion C_{inv} is given by

$$C_{inv} = \frac{k_{SiO_2}\varepsilon_0}{t_{inv}} \tag{1.1}$$

where k_{SiO_2} is the relative dielectric constant of SiO_2 (k_{SiO_2} = 3.9), ε_0 is the permittivity of free space (8.85×10^{-12} Fm^{-1}) and t_{inv} is the capacitance equivalent oxide thickness (CET) of the gate oxide. Higher C_{inv} value enables the MOS structure to have more inversion carriers in the channel at the given gate voltage, and thus increases the drive current of

MOSFETs. According to equation (1.1), to increase C_{inv}, we should decrease the t_{inv}. The t_{inv} consists of three components and can be expressed as

$$t_{inv} = t_{poly} + t_{ox} + t_{qm} \tag{1.2}$$

t_{poly} is the thickness contributing by poly-Si depletion effect, t_{ox} is the equivalent oxide thickness (EOT) of the gate dielectric*, and t_{qm} is the thickness attributed to quantum mechanical effect of carriers in the channel. t_{poly} could be reduced by replacing the poly-Si gate with metal gate, which is not the focus of this study. t_{qm} is an intrinsic mechanism and cannot be eliminated. The most effective way to reduce the t_{inv} is to decease t_{ox} (EOT). For the past several decades, the gate oxide thickness has been scaled down from hundred nm to now about ~ 1 nm. As pointed out in section 1.2.1, SiO_2 or SiO_xN_y has reached to its scaling limits. To further decrease the EOT while maintaining the gate leakage current of MOS structure, an insulator with a higher dielectric constant than SiO_2 (high-k material) with larger physical thickness should be used. The increased physical thickness can also solve the boron penetration problem and improve the gate dielectric reliability. As an example, using ZrO_2 as gate dielectric (k_{high-k}~20) would allow us to use a 5.1 nm thick layer in order to achieve an EOT of 1 nm*.

A lot of research efforts have been made on high-k gate dielectrics for the potential replacement of SiO_2 in advance CMOS technologies. The material that could be

*The EOT (t_{ox}) of a material is defined as the thickness of the SiO_2 layer that would be required to achieve the same capacitance density as the high-k material in consideration. EOT is given by $t_{ox} = t_{high-k} \times k_{SiO_2} / k_{high-k}$, where t_{high-k} and k_{high-k} are the physical thickness and relative dielectric constant of high-k dielectric, respectively.

the good candidate needs to satisfy a long list of requirements [12], e.g.:

- The relative dielectric constant of the material should be somewhere between 10 and 30. Dielectrics with higher k value will give rise to fringe fields from the gate to the drain or source and these fields can degrade short channel performances.
- The dielectric material must be an insulator with a band gap greater than 5 eV and the band offsets with silicon must be sufficient. Generally, increasing dielectric constant leads to lower conduction and valence band offset for materials in contact with silicon, and there is an inverse relationship between dielectric constant and the band gap. To prevent conduction by Schottky emission of electrons or holes into their respective bands, i.e. reduce leakage currents, the barrier at each band must be greater than 1 eV.
- Low density of intrinsic defects at the Si/dielectric interface and in the bulk of the material, providing high mobility of charge carriers in the channel and sufficient gate dielectric life time.
- Good thermal stability in contact with Si, preventing the formation of a thick SiO_x interfacial layer or silicide layers.

Table 1.1 lists the key characteristics of a wide variety of potential high-k gate dielectrics together with SiO_2 and Si_3N_4 for comparison. It can be seen that HfO_2 and $LaAlO_3$ meet most of the criteria listed above, such as k value, band offsets and good thermal stability. Indeed, the materials that received by far the most attention as alternative gate dielectrics are Hf-based, either HfO_2 or (nitrided) $HfSiO_x$ over a broad compositional range. The Intel's 45 nm technology microprocessor has already adopted Hf-based high-k dielectrics as gate insulator. Since Hf-based gate dielectrics have already

been demonstrated to be a very important high-k material for Si-based MOS devices. In this thesis, we will still focus on Hf-based high-k gate dielectrics for advanced gate stack application with alternative channel material.

Table 1.1. Key characteristics of a wide variety of gate dielectrics on Si [13-16].

Dielectric	**k value**	**Bandgap (eV)**	**Conduction band offset (eV)**	**Valence band offset (eV)**	**Thermal stability on silicon**
SiO_2	3.9	9.0	3.2	4.7	> 1050°C
Si_3N_4	7	5.3	2.4	1.8	> 1050°C
Al_2O_3	9	8.8	2.8	4.9	~ 1000°C
HfO_2	25	5.8	1.4	3.3	~ 950°C
$HfSiO_4$	11	6.5	1.8	3.6	> 900°C
La_2O_3	30	6.0	2.3	2.6	-
a-$LaAlO_3$	30	5.6	1.8	2.7	~ 1000°C
Ta_2O_5	22	4.4	0.35	2.95	Not stable
TiO_2	80	3.5	0	2.4	-
Y_2O_3	15	6.0	2.3	2.3	Silicate formation
ZrO_2	25	5.8	1.5	3.2	Forms silicides

1.3. Ge MOSFETs

Replacing the SiO_xN_y with high-k material mainly solve the high power consumption issue in MOSFET scaling, however, as mentioned earlier, the new technology node also needs increased I_{on} for higher performance. Stress-induced improvement of device performance has been widely reported. However, the mobility enhancement by strain is subject to limitation [17]. Furthermore, as the transistor size

becomes small enough (gate length < 20 nm), ballistic transport will become the dominant carrier transport mechanism. The transistor speed is no longer determined by the saturation velocity but the injection velocity at the source region, which is proportional to the mobility. Therefore, a MOSFET with high-k gate dielectrics and high mobility channel materials is a good option for future nanoelectronic devices.

Table 1.2. Material properties of alternative channel materials [18, 19].

	Ge	**Si**	**GaAs**	**InSb**	**InP**
Bandgap, E_g (eV)	0.66	1.12	1.42	0.17	1.35
Breakdown field (MV/cm)	0.1	0.3	0.06	0.001	0.5
Electron affinity, χ (eV)	4.05	4.0	4.07	4.59	4.38
Hole mobility, μ_h ($cm^2/V \cdot s$)	1900	450	400	1250	150
Electron mobility, μ_e ($cm^2/V \cdot s$)	3900	1500	8500	80000	4600
Effective density of states in valence band, N_v (cm^{-3})	6.0×10^{18}	1.04×10^{19}	7.0×10^{18}	7.3×10^{18}	1.1×10^{19}
Effective density of states in conduction band, N_c (cm^{-3})	1.04×10^{19}	2.8×10^{19}	4.7×10^{17}	4.2×10^{16}	5.7×10^{17}
Lattice constant, a (nm)	0.565	0.543	0.565	0.648	0.587
Dielectric constant, k	16	11.9	13.1	17.7	12.4
Thermal conductivity (W/cm·k)	0.58	1.3	0.55	0.18	0.68
Melting point, T_m (^oC)	937	1412	1240	527	1060

Table 1.2 lists the key material characteristics of Si, Ge and main III-V semiconductors. Among these materials, Ge offers the greatest potential for future CMOS application. Because it is the only material that provides higher mobility for both hole and electron with appropriate bandgap, breakdown field, thermal conductivity and melting point. In particular, the bulk hole mobility of Ge is the highest of all Group IV and III-V semiconductor materials. As shown later, it has actually been demonstrated that

unstrained Ge pMOSFETs can provide 3 times hole mobility against the Si universal hole mobility. Furthermore, Ge based MOS devices have shown to be compatible with strain technology for both nMOSFET [20] and pMOSFET [3] . It is found that the hole mobility enhancement of as high as ten is obtained by combing both Ge channel (GOI with 93% Ge content) and compressive strain [3]. Thus, Ge-channel MOSFETs have been regarded as one of the most promising channel materials for high speed application.

However, the current performance of Ge nMOSFETs is too poor to reach the level for the 22 nm node in the ITRS. Therefore, it maybe useful to investigate the feasibility of III-V MOSFETs because the enhancement factor of the bulk electron mobility against Si can amount to 3-50 for III-V semiconductors. However, it is easier to fabricate MOSFETs in Ge than in III-V materials since the surface passivation of III-V semiconductor is more challenging. Ge also has a larger density of states in the conduction band than III-V materials, which is another advantage for achieving a large drive current. It is suspected that the low mobility of Ge nMOSFETs is mainly attributed to the high density of interface traps of the gate stacks [21]. So Ge is also a potential nMOSFETs candidate if significant improvement of the interface quality can be achieved.

To realize the Ge-based CMOS technologies, there are a few issues to be solved, which are listed below [3]:

(1) High-k gate insulator formation with high quality interface and small EOT.

(2) High-quality Ge or GOI channel layer formation.

(3) Formation of low resistivity source/drain junctions.

(4) Improvement of poor performance of Ge nMOSFETs

(5) Reduction in large off state leakage current (I_{off}) due to smaller bandgap

(6) Appropriate CMOS structures and integration technologies.

In this thesis, we will focus on the issue (1). This is because in order to realize the desired high mobility Ge CMOS for sub-22 nm nodes, a viable high-k gate stack on Ge must at least have a low density of interface traps and small EOT.

1.4. Current status of Ge channel MOS devices with high-k dielectrics

Due to the water soluble nature of amorphous GeO_2, the early works mainly used germanium oxynitride as gate dielectrics. Rosenberg and Martin reported this kind of Ge pMOSFETs in 1988 [22]. Some subsequent result was reported from the same research group with improved hole mobility of 1050 $cm^2/V{\cdot}s$ [23]. Further progress was made by Ransom *et al.* with both n-channel and p-channel MOSFETs together in 1991 [24]. A gate-self-aligned process flow was used in this paper, which is very close to contemporary device fabrication flow already. Both n- and p-channel mobilties obtained from long channel device characteristics were greater than 1000 $cm^2/V{\cdot}s$, which are much higher than the mobility obtained from Si devices. In 2002, effective hole mobility measured by split *C-V* method was reported by Shang *et al*. with GeON dielectrics that was less than 10 nm thick [25]. Over 40% hole mobility enhancement is obtained over the Si control and a subthreshold slope less than 100 mV/dec was demonstrated. Although these results are encouraging, the equivalent oxide thicknesses are all too large to meet the ITRS requirement. Chui *et al.* studied the scalability of Ge oxynitride

dielectrics for MOS applications [26]. They found that GeON was not suitable for highly scaled MOSFET application (EOT < 2 nm) due to the high leakage current density.

In order to meet the gate leakage requirement, high-k dielectrics must be implemented on Ge substrate. In 2002, Chui *et al.* demonstrated Ge MOS capacitors with ZrO_2 gate dielectrics for the first time [27]. The gate dielectric was formed by UHV sputtering of ~ 20-30 Å Zr films on the Ge surface followed by *in-situ* UV ozone oxidation at room temperature. EOT as low as 5~8 Å and *C-V* hysteresis as small as 16 mV were achieved. The group further reported the Ge pMOSFETs with such high-k dielectrics with peak hole mobility as high as 313 $cm^2/V \cdot s$ [28]. However, the gate leakage currents for their samples were quite high and prevented the extraction of other device characteristics like interface states density. Kim *et al*. further investigated the ZrO_2/Ge gate stack, which was formed by atomic layer deposition (ALD) [29]. Large frequency dispersion and hysteresis were presented in the *C-V* characteristics, which was ascribed to poor interface quality.

Although introduction of high-k gate dielectrics enabled the scaling of EOT, the interface quality is poor when high-k dielectrics directly deposited on the Ge substrate. For ZrO_2/Ge gate stack, the poor interface quality was believed to originated from either the large areal density of interfacial dislocations due to the relatively large lattice mismatch or because of a very high density of interface states due to intrinsic differences in bonding coordination across the chemically-abrupt ZrO_2/Ge interface [29]. For the HfO_2/Ge gate stack, it was reported that a significant amount of germanium was found

inside HfO_2 film deposited by metalorganic chemical vapor deposition (MOCVD) [30]. Similar Ge incorporation was also observed in physical vapor deposition (PVD) HfO_2 on Ge substrate after high-temperature annealing [31]. There are several possible mechanisms causing the Ge diffusion into HfO_2. Zhang *et al*. believed that the fast germanium diffusion in dielectrics is probably due to its higher self-diffusivity coefficient compared to Si [31]. Kita *et al.* suggested that the diffusion might be attributed to the desorption of Ge-riched volatile Hf-Ge-O [32]. Whereas some other studies speculated that the formation of volatile GeO at HfO_2/Ge interface caused the diffusion [33]. The Ge diffusion into high-k dielectrics can cause significant degradation of interface quality and device performance. The high-k/Ge MOS characteristics tend to deteriorate when high-k/Ge is treated with thermal processes above 500 °C [34]. Such deterioration can be attributed to the fact that Ge-O bonds inevitably exist at the interface between Ge and high-k dielectrics.

The poor interface quality of high-k/Ge gate stack becomes the most challenging issue for the Ge MOSFETs. Many efforts have been made to improve the interface quality between high-k and Ge. In 2003, Bai *et al*. used an RTP NH_3 annealing before HfO_2 gate dielectric deposition for Ge MOS capacitors [35]. XTEM picture revealed that an ultra-thin interfacial layer (~8Å) was formed between the HfO_2 and Ge, which was believed to be the Ge oxynitride. By using the NH_3 passivation, electrical characteristics such as EOT, gate leakage current, hysteresis and D_{it} were significantly improved. The Ge pMOSFETs with such NH_3 treatment and HfO_2 gate dielectrics were further made by Ritenour *et al*. [36]. These devices exhibited sub-90 mV/decade substreshold swing and

low gate leakage current. An 1.8 X enhancement of hole mobility was achieved compared to Si control wafers. Van Elshocht *et al*. [30] and Lu *et al.* [33] investigated the Ge diffusion for MOS capacitors with NH_3 treatment. It was found that there was much less Ge diffusion for samples with NH_3 treatment compared to samples without NH_3 treatment.

The physical characteristics of NH_3 annealing was investigated by Wu *et al*. [37]. High resolution XPS study showed that GeO_xN_y is formed during NH_3 annealing. The concentrations of oxygen and nitrogen were quantified to be about 0.83:0.17. Although high purity NH_3 gas (99.999%) was used in the experiment, the concentration of oxygen in Ge oxynitride was very high. They author suspected that the oxygen was introduced by the NH_3 gas source since the main impurity was O_2, H_2O and H_2. The results also implied that Ge was much easier to be oxidized than nitrified. Gusev *et al*. further studied the microstructure of HfO_2 gate dielectric deposited on Ge [38]. It was found that the lack of an interlayer enables quisiepitaxial growth of HfO_2 on the Ge surface after wet chemical treatment whereas a nitrided interface (grown by thermal oxynitridation in NH_3) resulted in an amorphous HfO_2. Nitrided interfaces produced much better quality stacks.

Besides thermal NH_3 annealing, other techniques have also been reported to form the Ge oxynitride interlayer. Chen *et al*. reported an alternative surface nitridation technique by exposing the Ge substrate to an atomic N beam from a remote RF source at 350^{o}C to 600^{o}C [39]. Nuclear reaction analysis of nitride Ge substrate showed a nitrogen

surface density of 2.3×10^{15} cm^{-2}, translating to a substrate coverage of 3 to 4 monolayers. The surface nitridation was found to be effective to reduce EOT and *C-V* hysteresis for HfO_2 gated MOS capacitors. On the other hand, the nitridation also introduced a negative flatband voltage shift ~ 0.7 V, indicating of positive charge introduction or the incorporation of a charge dipole. Although improved electrical characteristics were obtained by surface nitridation, the D_{it} was still found to be high (~ 6×10^{12} $eV^{-1}cm^{-2}$) near the mid-gap using high-frequency/low-frequency method. The author also reported Al_2O_3 gated Ge MOS capacitor with surface nitridation. Interestingly, much lower D_{it} was found compared to HfO_2 gated samples, at the expense of increase in EOT and gate leakage current. To further minimize the GeO_x ($x<2$) component and increase N incorporation in the Ge oxynitride interlayer, a wet-NO oxidation was proposed by Xu *et al*. [40]. The mechanisms involved probably lie in the hydrolysable property of GeO_x in water-containing atmosphere.

Some groups of researchers also tried to fabricate Ge MOS structures with pure germanium nitride (Ge_3N_4). Because it is believed that the unstable GeO_x component can degrade the interface quality and high oxygen concentration may also lead to partially crystallization of Ge oxynitride films [37]. However, most of the films obtained through thermal nitridation were Ge oxynitride. Oxygen incorporation in these films was unavoidable, attributed to native oxide or residual oxygen in the reactor or oxygen impurities in the gas sources. Maeda *et al*. presented a demonstration of pure nitridation of clean Ge substrate using a plasma process at low temperatures [41]. The surface cleaning of Ge substrate and subsequent nitridation were performed in the same chamber.

In situ physical characteristics showed that oxygen was not present in these germanium nitride films. They also managed to fabricated the Ge MOS capacitors with EOT as low as 1.23 nm. These devices exhibited good high-frequency *C-V* characteristics but the gate leakage current is substantially high due to the fact that Ge_3N_4 was not a high-k material. The same group of researchers further optimized the process conditions and they found the smoothest interface and surface can be achieved in the Ge_3N_4 films grown at 100^oC [42]. It was also pointed out that the top surface of Ge_3N_4 films was oxidized easily once the Ge_3N_4 films were exposed to air. The similar phenomenon was also reported by Kutsuki *et al*. [43]. They found that humidity in the air accelerated the degradation of Ge_3N_4 layers and that under 80% humidity condition, most of the Ge-N bonds converted to Ge-O bonds. Therefore it is essential to take the best care of moisture in the fabrication of Ge MOS devices with Ge_3N_4 insulator or passivation layer. Maeda *et al*. further demonstrated HfO_2 gated Ge MOS capacitors with pure Ge_3N_4 interfacial layers [44]. The gate stack exhibited excellent interface quality with minimum $D_{it} \sim 1.8\times10^{11}cm^{-2}eV^{-1}$. It was noteworthy that D_{it} increased exponentially as the energy approached to the midgap. The thermal stability of the high-k gate stack was also improved with Ge_3N_4 interfacial layer. However, there is no report on transistor performance in that paper.

As mentioned earlier, pure Ge_3N_4 is hard to form on Ge surface due to two reasons. The first is that it is difficult to avoid residual oxygen content inside the process chamber or at Ge surface. The second is that Ge is much easier to be oxidized than nitrided [37]. Thus, some other groups of researchers tried to use metal nitride or metal oxynitride passivation layer to minimize the GeO_x ($x<2$) content at high-k/Ge surface.

Gao *et al*. demonstrated a surface passivation using AlN_x film for HfO_2 gated Ge MOS capacitors [45]. The AlN_x layer was deposited by reactive sputtering of Al target in N_2/Ar ambient. For comparison, they also fabricated Ge MOS capacitors with thermal NH_3 treatment. Interestingly, the author found that the intensity of GeO_2 peak increased significantly after HfO_2 deposition for sample with surface nitridation, indicating that most of the GeO_x component was formed at interface during the HfO_2 deposition process. Whereas for devices with AlN_x passivation, the GeO_x component was reduced because AlN_x acted as a better oxygen diffusion barrier. The electrical characteristics and thermal stability was also improved for device with AlN_x passivation. Kim *et al*. further made both n and p channel Ge MOSFETs with AlN_x or Hf_3N_4 passivation layer deposited by ALD [46]. Good *C-V* characteristics were achieved with EOT as low as 0.8 nm. However, the devices exhibited quite high interface states. The mobility for pMOSFETs was only slightly higher than Si hole universal and mobility for nMOSFETs was much lower than Si electron universal. It can be seen that although metal nitride passivation layer acts as a better oxygen barrier, but the high D_{it} seems to an intrinsic problem that limits its implementation for MOSFETs fabrication. Some recent works presented another TaO_xN_y passivation layer, formed either by plasma enhanced ALD [47] or reactive sputtering (with PDA) [48]. TaO_xN_y interlayer was demonstrated to be a good diffusion barrier between high-k and Ge. Electrical characteristics like EOT, hysteresis and D_{it} were improved. D_{it} value was lower than MOS capacitors with AlN_x or Hf_3N_4 interlayer reported earlier. A peak hole mobility of 225 $cm^2/V{\cdot}s$ was demonstrated for Ge pMOSFETs with TaO_xN_y interlayer, which was about ~1.7 X enhancement over Si hole universal.

By now, we have reviewed a few nitride based Ge surface passivation techniques. By forming Ge oxynitride, Ge_3N_4, metal nitride or metal oxynitride interlayer, high-k gated Ge MOS devices showed improved electrical characteristics such as EOT, gate leakage current, *C-V* characteristics and D_{it}. The improvements are attributed to less Ge diffusion into high-k dielectrics by reducing the amounts of GeO_x ($x<2$) formation at interface. High-k gated Ge pMOSFETs with enhanced hole mobility (as high as a 1.8X Si universal) have been demonstrated whereas electron mobility of Ge nMOSFETs is very poor.

Besides the nitride based surface passivation techniques, another alternative passivation process-Si passivation was proposed and demonstrated on HfO_2 gated Ge MOS capacitors by Wu *et al*. in 2004 [49]. Two important criteria were pointed out for an effective Si passivation: (1) Si must completely cover the Ge surface and Ge surface should be free of germanium oxide; (2) The Si passivation layer should be thin enough and consumed during the subsequent high-k deposition so that the MOSFET channel is still kept in Ge. XPS studies showed that Ge-O bonds were greatly reduced by Si passivation and Si cap layers were totally oxidized after HfO_2 deposition. Very good *C-V* characteristics were achieved with EOT as low as 13.5Å and gate leakage current as low as 1.16×10^{-5} A/cm^2@ 1V. Wu *et al*. further demonstrated TaN/HfO_2/Ge pMOSFETs with Si passivation [50]. TEM picture showed that a thin amorphous interfacial layer was obtained after Si passivation. Ge pMOSFETs with NH_3 treatment were also fabricated for comparison. The author found that devices with Si passivation exhibited lower gate leakage current and better thermal stability. The improvements were believed to be

resulted from the significant suppression of unstable germanium oxide formed at interface, as well as the uniform amorphous interfacial layer after the silicon passivation process. The peak hole mobility for NH_3 treated and Si passivated MOSFETs were 79.9 $cm^2/V{\cdot}s$ and 194.1 $cm^2/V{\cdot}s$, respectively. The author further optimized the Si passivation process by tuning the Si interlayer and HfO_2 thickness [51]. It was found that by increasing the Si cap thickness and decreasing the HfO_2 thickness, better *C-V* characteristics and interface quality were achieved. This is because increasing the amount of Si would reduce the amount of GeO_x ($x<2$) at the interface and hence, lead to fewer interface traps. At the same time, increasing HfO_2 thickness tends to consume more Si, and more GeO_x might form, resulting in worse interface quality. A much higher hole mobility with peak ~ 240 $cm^2/V{\cdot}s$ was achieved by optimizing the ratio between HfO_2 and Si. Ge nMOSFETs were also reported with peak electron mobility ~ 215 $cm^2/V{\cdot}s$, which was still much lower than Si electron universal.

In 2006, Zimmerman *et al*. demonstrated HfO_2 gated Ge pMOSFETs with Si passivation fabricated with a Si-compatible process flow using 200 mm (100) Ge-on-Si wafers [52]. Approximately a 3X mobility enhancement was observed compared to Si hole universal with EOT ~ 1.2 nm. Short channel devices were also fabricated using the same process flow. Correcting for R_s, the peak field effective mobilities extacted for even the shortest devices (L_g ~ 0.125 μm) remained above 300 $cm^2/V{\cdot}s$. Joshi *et al*. also reported high mobility (~ 3X Si) Ge pMOSFETs using direct SiO_x passivation [53]. Highly scaled sub-100 nm Ge pMOSFETs with Si passivation were also demonstrated [54, 55]. Similar to Wu's finding [51], it was also found that the interface quality was

improved with increasing Si cap thickness. Mitard *et al*. further observed that Ge could diffuse into Si and this Ge incorporation in Si could give strong impact on electrical performance. A low temperature Si layer deposition at 350^{o}C was proposed to solve this issue [54].

The principles of both nitride based passivation and Si passivation actually are quite similar. Both passivation techniques improve the gate stack quality by reducing the volatile GeO_x ($x<2$) formation at high-k/Ge interface and suppress the Ge diffusion into high-k dielectrics.

As in the case of SiO_2 with Si, GeO_2 is still believed to be the ideal passivating layer for Ge. Unlike the Ge sub-oxide (GeO_x), GeO_2 is not a volatile material and thus has the potential to act as a dielectric material. In 2007, Takahashi *et al*. investigated the possibility of using GeO_2 as a gate dielectric for Ge MOS devices [56]. They firstly studied the GeO_2/Ge interface kinetics by annealing the stack at different temperatures. It was observed that GeO_2 reacted with Ge forming volatile GeO which desorbs above 500-600^{o}C. It can be easily expected that GeO desorption should degrade the dielectric film and interface characteristics. Therefore, a Ni-FUSI cap layer, which acted as part of gate electrode, was implemented on GeO_2/Ge stack to suppress the GeO desorption. Surprisingly, very good *C-V* characteristics were achieved. Both Ge p- and n- channel MOSFETs were fabricated using Ni-FUSI/GeO_2/Ge gate stack. Recorded hole mobility ~ 370 cm^2/V·s with S/D resistance correction was obtained for pMOSFETs whereas ~ 270 cm^2/V·s without S/D resistance correction was obtained for nMOSFETs. Matsubara *et al*.

further investigated the interface quality of GeO_2/Ge using low temperature conductance method [57]. It was found that very promising interface quality could be obtained for GeO_2/Ge interface with D_{it} as low as 9.3×10^{10} $cm^{-2}eV^{-1}$, which was approaching to SiO_2/Si standard. The same group further presented very high hole mobility (> 400 $cm^2/V \cdot s$) Ge pMOSFETs with this GeO_2 dielectric layer capped with SiO or Al_2O_3 [58]. However, the physical thickness of their gate stack was quite large (> 40 nm).

To fabricate high quality GeO_2 on Ge surface, the process temperature and pressure is also very important. To minimize the GeO desorption and achieving good stoichiometry, Kuzum *et al*. proposed an ozone oxidization method to grow high quality GeO_2 at lower temperatures because ozone is more reactive than oxygen [59]. Lee *et al*. demonstrated another approach by using thermal oxidation in high pressure oxygen without any capping layer [60]. Because of higher oxygen pressure, a net process of Ge oxidization took place, rather than decomposition of GeO_2 into GeO. Moreover, by increasing the O_2 pressure at GeO_2/Ge interface, the GeO pressure was decreased. As a result, much better GeO_2 quality was obtained compared to GeO_2 grown by normal thermal oxidation process. By using this two methods, recently, recorded high electron mobility for Ge nMOSFETs have been demonstrated, which are higher than Si universal electron mobility [61, 62]. However, the gate oxide thickness is large for those devices, which has not met the requirement of small EOT for future nanoscale transistors.

Due to the fact that GeO_2 is a low-k material, although GeO_2/Ge exhibits excellent interface quality with low D_{it}, stoichiometric GeO_2 still cannot serve on its own

as a gate dielectric for aggressive scaled Ge MOSFETs where sub 1-nm EOT is required with a minimum gate leakage current. Therefore, capping the GeO_2 with a high-k dielectric offers the potential to improve the gate stack insulating properties and scalability. HfO_2 gated Ge MOS capacitors with thermal GeO_2 passivation layer was demonstrated by Delabie *et al*. [63]. EOT was successfully scaled down to 1.5 nm. The devices exhibited very good *C-V* characteristics with $D_{it} \sim 3\times10^{11}$ $cm^{-2}eV^{-1}$, which was slightly higher than pure GeO_2/Ge gate stack [57]. Tsipas *et al*. investigated the ZrO_2/GeO_2/Ge gate stack and it was found that Ge presence within ZrO_2 was beneficial in stabilizing the zirconia tetragonal phase, which was accompanied by a high-k value of around 44 [64]. Such a high value is desirable for further EOT scaling down. It can be seen that GeO_2 passivation is benefical for high-k gated Ge MOS capacitors. However, there is still no reports for high-k gated Ge MOSFETs with GeO_2 passivation.

By now, we have reviewed three major surface passivation techniques to obtain high quality high-k/Ge gate stacks. They are surface nitridation, Si passivation and GeO_2 passivation. We have also shown that minimizing the GeO_x ($x<2$) components at high-k/Ge interface is very important to achieve good interface quality since GeO_x is unstable and volatile which will cause severe Ge diffusion into high-k dielectrics. With the surface passivation layer, D_{it} is significantly reduced for high-k gated Ge MOS devices, although it is still higher than that of high-k/Si interface. High-k gated Ge pMOSFETs with 3X enhancement in hole mobility has been demonstrated. However, there is still no successful report on high-k gated Ge nMOSFETs achieving greater electron mobility than Si.

1.5 Thesis outline and original contributions

In chapter 2, an alternative surface passivation technique other than using nitride, Si or GeO_2 is studied. The technique is called sulfur passivation as a pre-gate $(NH_4)_2S$ solution treatment is done before the high-k deposition. In this chapter, the effects of the sulfur passivation are investigated in detail through both physical and electrical characterizations. The impact on gate stack thermal stability is also studied.

In chapter 3, an improved version of Si passivation is proposed and demonstrated. As discussed in section 1.4, the effectiveness of Si passivation highly depends on the Si interlayer thickness and ultrathin Si layer can not effectively suppress the Ge diffusion. In this work, we incorporate nitrogen into the ultrathin Si layer and find that the ultrathin Si_xN_y layer is more capable to suppress Ge diffusion and better electrical performance is achieved. The use of Si_xN_y interlayer also addresses the unexpected positive V_{th} shift issue for Si passivation.

In the literature, extensive studies have been made to explore the pre-gate treatments for high-k/Ge gate stack. In chapter 4, for the first time, the concept of the post-gate treatment is proposed for high-k/Ge gate stack. F incorporation is demonstrated on high-k/Ge gate stack through post gate CF_4 plasma treatment. The interface quality of high-k/Ge gate stack is greatly improved by F passivation.

In chapter 5, we further demonstrate this post gate treatment concept on thermal GeO_2 passivated Ge pMOSFETs with HfO_2 gate dielectric. Record high hole mobility >

3X Si hole universal is achieved with EOT as low as 1 nm. Variable rise/fall time charge pumping method is also used to study the interface quality of Ge MOSFETs.

In chapter 6, we implement the variable rise/fall time charge pumping method to study the energy distribution characteristics of HfO_2 gated Ge MOSFETs. The cause of the poor electron mobility for Ge nMOSFETs with Si passivation is pointed out.

Finally, the thesis is completed with conclusions and suggested future works in Chapter 7.

References:

[1] G. E. Moore, "Cramming more components onto integrated circuits (Reprinted from Electronics, pg 114-117, April 19, 1965)," *Proceedings of the IEEE,* vol. 86, pp. 82-85, Jan 1998.

[2] R. H. Dennard, F. F. Gaensslen, N.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of Solid-State Circuits,* vol. 9, pp. 256- 268, Oct 1974.

[3] S. Takagi, T. Irisawa, T. Tezuka, T. Numata, S. Nakaharai, N. Hirashita, Y. Moriyama, K. Usuda, E. Toyoda, S. Dissanayake, M. Shichijo, R. Nakane, S. Sugahara, M. Takenaka, and N. Sugiyama, "Carrier-transport-enhanced channel CMOS for improved power consumption and performance," *IEEE Transactions on Electron Devices,* vol. 55, pp. 21-39, Jan 2008.

[4] *International Technology Roadmap for Semiconductors (ITRS),* [Online]. Available: http://public.itrs.net/.

[5] G. Timp, J. Bude, K. K. Bourdelle, J. Garno, A. Ghetti, H. Gossmann, M. Green, G. Forsyth, Y. Kim, R. Kleiman, F. Klemens, A. Kornblit, C. Lochstampfor, W. Mansfield, S. Moccio, T. Sorsch, D. M. Tennant, W. Timp, and R. Tung, "The ballistic nano-transistor," in *IEEE International Electron Devices Meeting*, Washington, DC, 1999, pp. 55-58.

[6] R. Chau, J. Kavalieros, B. Roberds, R. Schenker, D. Lionberger, D. Barlage, B. Doyle, R. Arghavani, A. Murthy, and G. Dewey, "30 nm physical gate length CMOS transistors with 1.0 ps n-MOS and 1.7 ps p-MOS gate delays," in *IEEE International Electron Devices Meeting*, San Francisco, CA 2000, pp. 45-48.

[7] A. T. Fromhold, *Quantum Mechanics for Applied Physics and Engineering*: (New York: Dover), 1981.

[8] M. Houssa, *High-k Gate Dielectrics*: IOP, 2004.

[9] M. Depas, B. Vermeire, P. W. Mertens, R. L. Vanmeirhaeghe, and M. M. Heyns, "Determination of tunnelling parameters in ultra-thin oxide layer poly-Si/SiO_2/Si structures," *Solid-State Electronics,* vol. 38, pp. 1465-1471, Aug 1995.

[10] M. Cao, P. V. Voorde, M. Cox, and W. Greene, "Boron diffusion and penetration in ultrathin oxide with poly-Si gate," *IEEE Electron Device Letters,* vol. 19, pp. 291-293, Aug 1998.

[11] T. Sasaki, K. Kuwazawa, K. Tanaka, J. Kato, and D. L. Kwong, "Engineering of nitrogen profile in an ultrathin gate insulator to improve transistor performance and NBTI," *IEEE Electron Device Letters,* vol. 24, pp. 150-152, Mar 2003.

[12] M. Houssa, L. Pantisano, L. A. Ragnarsson, R. Degraeve, T. Schram, G. Pourtois, S. De Gendt, G. Groeseneken, and M. M. Heyns, "Electrical properties of high-k gate dielectrics: Challenges, current issues, and possible solutions," *Materials Science & Engineering R-Reports,* vol. 51, pp. 37-85, Apr 2006.

[13] X. H. Cheng, Z. R. Song, J. Jiang, Y. H. Yu, W. W. Yang, and D. S. Shen, "Study of HfSiO film prepared by electron beam evaporation for high-k gate dielectric applications," *Applied Surface Science,* vol. 252, pp. 8073-8076, Sep 2006.

[14] S. Pelloquin, L. Becerra, G. Saint-Girons, C. Plossu, N. Baboux, D. Albertini, G. Grenet, and G. Hollinger, "Molecular beam deposition of $LaAlO_3$ on silicon for sub-22 nm CMOS technological nodes: Towards a perfect control of the oxide/silicon heterointerface," *Microelectronic Engineering,* vol. 86, pp. 1686-1688, Jun 28-Jul 07 2009.

[15] J. Robertson, "High dielectric constant oxides," *European Physical Journal-Applied Physics,* vol. 28, pp. 265-291, Dec 2004.

[16] H. S. P. Wong, "Beyond the conventional transistor," *IBM Journal of Research and Development,* vol. 46, pp. 133-168, Mar-May 2002.

[17] S. Takagi, T. Mizuno, T. Tezuka, N. Sugiyama, T. Numata, K. Usuda, Y. Moriyama, S. Nakaharai, J. Koga, A. Tanabe, N. Hirashita, and T. Maeda, "Channel structure design, fabrication and carrier transport properties of strained-Si/SiGe-On-Insulator (strained-SOI) MOSFETs," in *IEEE International Electron Devices Meeting*, Washington, D.C., 2003, pp. 57-60.

[18] Y. Kamata, "High-k/Ge MOSFETs for future nanoelectronics," *Materials Today,* vol. 11, pp. 30-38, Jan-Feb 2008.

[19] B. H. Lee, J. Oh, H. H. Tseng, R. Jammy, and H. Huff, "Gate stack technology for nanoscale devices," *Materials Today,* vol. 9, pp. 32-40, Jun 2006.

[20] M. Kobayashi, T. Irisawa, B. M. Kope, Y. Sun, K. Saraswat, H. S. P. Wong, P. Pianetta, and Y. Nishi, "High Quality GeO_2/Ge Interface Formed by SPA Radical Oxidation and Uniaxial Stress Engineering for High Performance Ge NMOSFETs," in *2009 Symposium on Vlsi Technology, Digest of Technical Papers*, 2009, pp. 76-77.

[21] K. Martens, B. De Jaeger, R. Bonzom, J. Van Steenbergen, M. Meuris, G. Groeseneken, and H. Maes, "New interface state density extraction method applicable to peaked and high-density distributions for Ge MOSFET development," *IEEE Electron Device Letters,* vol. 27, pp. 405-408, May 2006.

[22] J. J. Rosenberg and S. C. Martin, "Self-aligned germanium MOSFET's using a nitrided native oxide gate insulator," *IEEE Electron Device Letters,* vol. 9, pp. 639-640, Dec 1988.

[23] S. C. Martin, L. M. Hitt, and J. J. Rosenberg, "Germanium p-Channel MOSFET's with high channel mobility, transconductance, and k-value," *IEEE Transactions on Electron Devices,* vol. 36, pp. 2629-2630, Nov 1989.

[24] C. M. Ransom, T. N. Jackson, and J. F. Degelormo, "Gate-self-aligned n-channel and p-channel germanium MOSFET's," *IEEE Transactions on Electron Devices,* vol. 38, pp. 2695-2695, Dec 1991.

[25] H. L. Shang, H. Okorn-Schmidt, K. K. Chan, M. Copel, J. A. Ott, P. M. Kozlowski, S. E. Steen, S. A. Cordes, H. S. P. Wong, E. C. Jones, and W. E. Haensch, "High mobility p-

channel germanium MOSFETs with a thin Ge oxynitride gate dielectric," in *IEEE International Electron Devices Meeting*, San Francisco, Ca, 2002, pp. 441-444.

[26] C. O. Chui, F. Ito, and K. C. Saraswat, "Scalability and electrical properties of germanium oxynitride MOS dielectrics," *IEEE Electron Device Letters,* vol. 25, pp. 613-615, Sep 2004.

[27] C. O. Chui, S. Ramanathan, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "Germanium MOS capacitors incorporating ultrathin high-k gate dielectric," *IEEE Electron Device Letters,* vol. 23, pp. 473-475, Aug 2002.

[28] C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "A Sub-400 degrees C germanium MOSFET technology with high-k dielectric and metal gate," in *IEEE International Electron Devices Meeting*, San Francisco, Ca, 2002, pp. 437-440.

[29] H. Kim, C. O. Chui, K. C. Saraswat, and P. C. McIntyre, "Local epitaxial growth of ZrO_2 on Ge(100) substrates by atomic layer epitaxy," *Applied Physics Letters,* vol. 83, pp. 2647-2649, Sep 2003.

[30] S. Van Elshocht, B. Brijs, M. Caymax, T. Conard, T. Chiarella, S. De Gendt, B. De Jaeger, S. Kubicek, M. Meuris, B. Onsia, O. Richard, I. Teerlinck, J. Van Steenbergen, C. Zhao, and M. Heyns, "Deposition of HfO_2 on germanium and the impact of surface pretreatments," *Applied Physics Letters,* vol. 85, pp. 3824-3826, Oct 2004.

[31] Q. C. Zhang, N. Wu, D. M. Y. Lai, Y. Nikolai, L. K. Bera, and C. X. Zhu, "Germanium incorporation in HfO_2 dielectric on germanium substrate," *Journal of the Electrochemical Society,* vol. 153, pp. G207-G210, 2006.

[32] K. Kita, K. Kyuno, and A. Toriumi, "Growth mechanism difference of sputtered HfO_2 on Ge and on Si," *Applied Physics Letters,* vol. 85, pp. 52-54, Jul 2004.

[33] N. Lu, W. Bai, A. Ramirez, C. Mouli, A. Ritenour, M. L. Lee, D. Antoniadis, and D. L. Kwong, "Ge diffusion in Ge metal oxide semiconductor with chemical vapor deposition HfO_2 dielectric," *Applied Physics Letters,* vol. 87, 051922, Aug 2005.

[34] K. Kita, H. Nomura, and T. Nishimura, "Impact of Dielectric Material Selection on Electrical Characteristics of High-k/Ge Devices," *Electrochemical Society Transactions,* vol. 3, pp. 71-78, 2006.

[35] W. P. Bai, N. Lu, J. Liu, A. Ramirez, D. L. Kwong, D. Wristers, A. Ritenour, L. Lee, and D. Antoniadis, "Ge MOS Characteristics with CVD HfO_2 Gate Dielectrics and TaN Gate Electrode," in *VLSI Symposium Technology Digest*, 2003, pp. 121-122.

[36] A. Ritenour, S. Yu, M. L. Lee, N. Lu, W. Bai, A. Pitera, E. A. Fitzgerald, D. L. Kwong, and D. A. Antoniadis, "Epitaxial strained germanium p-MOSFETs with HfO_2 gate dielectric and TaN gate electrode," in *IEEE International Electron Devices Meeting*, Washington, D.C., 2003, pp. 433-436.

[37] N. Wu, Q. C. Zhang, C. X. Zhu, C. C. Yeo, S. J. Whang, D. S. H. Chan, M. F. Li, B. J. Cho, A. Chin, D. L. Kwong, A. Y. Du, C. H. Tung, and N. Balasubramanian, "Effect of

surface NH_3 anneal on the physical and electrical properties of HfO_2 films on Ge substrate," *Applied Physics Letters,* vol. 84, pp. 3741-3743, May 2004.

[38] E. P. Gusev, H. Shang, M. Copel, M. Gribelyuk, C. D'Emic, P. Kozlowski, and T. Zabel, "Microstructure and thermal stability of HfO_2 gate dielectric deposited on Ge(100)," *Applied Physics Letters,* vol. 85, pp. 2334-2336, Sep 2004.

[39] J. J. H. Chen, N. A. Bojarczuk, H. L. Shang, M. Copel, J. B. Hannon, J. Karasinski, E. Preisler, S. K. Banerjee, and S. Guha, "Ultrathin Al_2O_3 and HfO_2 gate dielectrics on surface-nitrided Ge," *IEEE Transactions on Electron Devices,* vol. 51, pp. 1441-1447, Sep 2004.

[40] J. P. Xu, P. T. Lai, C. X. Li, X. Zou, and C. L. Chan, "Improved electrical properties of germanium MOS capacitors with gate dielectric grown in Wet-NO ambient," *IEEE Electron Device Letters,* vol. 27, pp. 439-441, Jun 2006.

[41] T. Maeda, T. Yasuda, M. Nishizawa, N. R. Miyata, Y. Morita, and S. Takagi, "Ge metal-insulator-semiconductor structures with Ge_3N_4 dielectrics by direct nitridation of Ge substrates," *Applied Physics Letters,* vol. 85, pp. 3181-3183, Oct 2004.

[42] T. Maeda, T. Yasuda, M. Nishizawa, N. Miyata, Y. Morita, and S. Takagi, "Pure germanium nitride formation by atomic nitrogen radicals for application to Ge metal-insulator-semiconductor structures," *Journal of Applied Physics,* vol. 100, 014101, Jul 2006.

[43] K. Kutsuki, G. Okamoto, T. Hosoi, T. Shimura, and H. Watanabe, "Humidity-dependent stability of amorphous germanium nitrides fabricated by plasma nitridation," *Applied Physics Letters,* vol. 91, 163501, Oct 2007.

[44] T. Maeda, M. Nishizawa, Y. Morita, and S. Takagi, "Role of germanium nitride interfacial layers in HfO_2/germanium nitride/germanium metal-insulator-semiconductor structures," *Applied Physics Letters,* vol. 90, 072911, Feb 2007.

[45] F. Gao, S. J. Lee, J. S. Pan, L. J. Tang, and D. L. Kwong, "Surface passivation using ultrathin AlN_x film for Ge-metal-oxide-semiconductor devices with hafnium oxide gate dielectric," *Applied Physics Letters,* vol. 86,113501, Mar 2005.

[46] K. H. Kim, R. G. Gordon, A. Ritenour, and D. A. Antoniadis, "Atomic layer deposition of insulating nitride interfacial layers for germanium metal oxide semiconductor field effect transistors with high-k oxide/tungsten nitride gate stacks," *Applied Physics Letters,* vol. 90, 212104, May 2007.

[47] T. Sugawara, Y. Oshima, R. Sreenivasan, and P. C. McIntyre, "Electrical properties of germanium/metal-oxide gate stacks with atomic layer deposition grown hafnium-dioxide and plasma-synthesized interface layers," *Applied Physics Letters,* vol. 90, 112912, Mar 2007.

[48] J. P. Xu, X. F. Zhang, C. X. Li, P. I. Lai, and C. L. Chan, "Improved electrical properties of Ge p-MOSFET with HfO_2 gate dielectric by using TaO_xN_y interlayer," *IEEE Electron Device Letters,* vol. 29, pp. 1155-1158, Oct 2008.

[49] N. Wu, Q. C. Zhang, C. X. Zhu, D. S. H. Chan, M. F. Li, N. Balasubramanian, A. Chin, and D. L. Kwong, "Alternative surface passivation on germanium for metal-oxide-semiconductor applications with high-k gate dielectric," *Applied Physics Letters,* vol. 85, pp. 4127-4129, Nov 2004.

[50] N. Wu, Q. C. Zhang, C. X. Zhu, D. S. H. Chan, A. Y. Du, N. Balasubramanian, M. F. Li, A. Chin, J. K. O. Sin, and D. L. Kwong, "A TaN-HfO_2-Ge pMOSFET with novel SiH_4 surface passivation," *IEEE Electron Device Letters,* vol. 25, pp. 631-633, Sep 2004.

[51] N. Wu, Q. C. Zhang, N. Balasubramanian, D. S. H. Chan, and C. X. Zhu, "Characteristics of self-aligned gate-first Ge p- and n-channel MOSFETs using CVD HfO_2 gate dielectric and Si surface passivation," *IEEE Transactions on Electron Devices,* vol. 54, pp. 733-741, Apr 2007.

[52] P. Zimmerman, G. Nicholas, B. De Jaeger, B. Kaczer, A. Stesmans, L. A. Ragnarsson, D. P. Brunco, F. E. Leys, M. Caymax, G. Winderickx, K. Opsomer, M. Meuris, and M. M. Heyns, "High performance Ge pMOS devices using a Si-compatible process flow," in *IEEE International Electron Devices Meeting*, San Francisco, CA, 2006, pp. 390-393.

[53] S. Joshi, C. Krug, D. Heh, H. J. Na, H. R. Harris, J. W. Oh, P. D. Kirsch, P. Majhi, B. H. Lee, H. H. Tseng, R. Jammy, J. C. Lee, and S. K. Banerjee, "Improved Ge surface passivation with ultrathin SiO_x enabling high-mobility surface channel pMOSFETs featuring a HfSiO/WN gate stack," *IEEE Electron Device Letters,* vol. 28, pp. 308-311, Apr 2007.

[54] J. Mitard, B. De Jaeger, F. E. Leys, G. Hellings, K. Martens, G. Eneman, D. P. Brunco, R. Loo, J. C. Lin, D. Shamiryan, T. Vandeweyer, G. Winderickx, E. Vrancken, C. H. Yu, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, and M. M. Heyns, "Record I_{ON}/I_{OFF} performance for 65nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability," in *IEEE International Electron Devices Meeting*, San Francisco, CA, 2008, pp. 873-876.

[55] T. Yamamoto, Y. Yamashita, M. Harada, N. Taoka, K. Ikeda, K. Suzuki, O. Kiso, N. Sugiyama, and S. Takagi, "High Performance 60 nm Gate Length Germanium p-MOSFETs with Ni Germanide Metal Source/Drain," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 1041-1043.

[56] T. Takahashi, T. Nishimura, L. Chen, S. Sakata, K. Kita, and A. Toriumi, "Proof of Ge-interfacing concepts for metal/high-k/Ge CMOS Ge-intimate material selection and interface conscious process flow," in *IEEE International Electron Devices Meeting*, Washington, DC, 2007, pp. 697-700.

[57] H. Matsubara, T. Sasada, M. Takenaka, and S. Takagi, "Evidence of low interface trap density in GeO_2/Ge metal-oxide-semiconductor structures fabricated by thermal oxidation," *Applied Physics Letters,* vol. 93, 032104, Jul 2008.

[58] Y. Nakakita, R. Nakane, T. Sasada, H. Matsubara, M. Takenaka, and S. Takagi, "Interface-controlled Self-Align Source/Drain Ge pMOSFETs Using Thermally-Oxidized GeO_2 Interfacial Layers," in *IEEE International Electron Devices Meeting*, San Francisco, CA, 2008, pp. 877-880.

[59] D. Kuzum, T. Krishnamohan, A. J. Pethe, A. K. Okyay, Y. Oshima, Y. Sun, J. P. McVittie, P. A. Pianetta, P. C. McIntyre, and K. C. Saraswat, "Ge-interface engineering with ozone oxidation for low interface-state density," *IEEE Electron Device Letters,* vol. 29, pp. 328-330, Apr 2008.

[60] C. H. Lee, T. Nishimura, K. Nagashio, K. Kita, and A. Toriumi, "Reaction Kinetics Control on Thermal Oxidation Process of Ge in High Pressure Oxygen," in *International Conference on Solid State Devices and Materials*, Tsukuba, JAPAN, 2008, pp. 16-17.

[61] D. Kuzum, T. Krishnamohan, A. Nainani, Y. Sun, P. A. Pianetta, H. S. P. Wong, and K. C. Saraswat, "Experimental Demonstration of High Mobility Ge NMOS," in *2009 IEEE International Electron Devices Meeting*, 2009, pp. 420-423.

[62] C. H. Lee, T. Nishimura, N. Saido, K. Nagashio, K. Kita, and A. Toriumi, "Record-high Electron Mobility in Ge n-MOSFETs exceeding Si Universality," in *2009 IEEE International Electron Devices Meeting*, 2009, pp. 424-427.

[63] A. Delabie, F. Bellenger, M. Houssa, T. Conard, S. Van Elshocht, M. Caymax, M. Heyns, and M. Meuris, "Effective electrical passivation of Ge(100) for high-k gate dielectric layers using germanium oxide," *Applied Physics Letters,* vol. 91, 082904, Aug 2007.

[64] P. Tsipas, S. N. Volkos, A. Sotiropoulos, S. F. Galata, G. Mavrou, D. Tsoutsou, Y. Panayiotatos, A. Dimoulas, C. Marchiori, and J. Fompeyrine, "Germanium-induced stabilization of a very high-k zirconia phase in ZrO_2/GeO_2 gate stacks," *Applied Physics Letters,* vol. 93, 082904, Aug 2008.

Chapter 2

Effects of Sulfur Passivation on High-k/Ge Gate Stack

As mentioned in the previous chapter, to have a high quality high-k gate stack on Ge substrate, minimizing the GeO_x ($x < 2$) at the surface between the high-k and substrate is a critical issue, because volatile germanium monoxide formation at interface can lead serious Ge out diffusion, resulting poor interface quality. To minimize the GeO_x, Ge surface passivation is needed before gate stack formation. In literature, a few surface passivation techniques have been systematically studied, including nitride based passivation, Si passivation and GeO_2 passivation. Recently, Martin M. Frank *et al* [1] reported another surface passivation technique - sulfur passivation, which has also been demonstrated to be useful for MOS capacitors made on III-V substrate [2]. It was found that interface state density is lower than NH_3 nitridation passivated samples. However, the gate stack in that paper did not go through any high temperature annealing (e.g. >400°C). Also, there is no report on electrical properties like equivalent oxide thickness (EOT) and gate leakage current. In this chapter, we investigate the effects of sulfur passivation on Ge MOS capacitors in a more detailed manner to fill in the gap in literature about sulfur passivation. Both physical and electrical characteristics will be studied and gate stack thermal stability will also be examined.

2.1. Experiments

The starting wafers for the experiment were n-type Ge wafers (Sb doped, resistivity = 0.04-0.08Ωcm). The native oxide was removed by a cyclic rinsing between deionized (DI) water and diluted HF [3]. After that, the substrates were immersed into 20% aqueous $(NH_4)_2S$ solution for 30 min at room temperature, followed by a water rinse and a N_2 blow dry. Control samples with only HF cyclic rinsing were also prepared. After that, HfON was then formed on both types of samples by HfON deposition with reactive sputtering and post deposition annealing in an N_2 ambient at 500°C for 1 min (the residual oxygen concentration < 5ppm). A 150nm TaN gate electrode was then sputtered, and followed by lithography and dry etching processes. Post metal annealing (PMA) at different temperatures was then performed for thermal stability investigation. The final step was forming gas anneal in $H_2 + N_2$ ambient at 420ºC for 2 hours. High-resolution *ex situ* x-ray photoelectron spectroscopy (XPS) analysis was performed with standard Al x-ray source. Secondary ion mass spectroscope (SIMS) analysis was used to study the Ge profile in the gate stack. Capacitance-voltage (*C*-*V*) and leakage current-voltage (*J*-*V*) characteristics were measured by an Agilent 4284A LCR meter and a HP4156A semiconductor parameter analyzer, respectively.

2.2. Results and Discussions

To confirm the S incorporation after the $(NH_4)_2S$ treatment, XPS data of S 2p signal is measured and shown in Fig.2.1. The peak (~162eV) of the S 2p signal indicates that S was introduced on the Ge surface after $(NH_4)_2S$ treatment. The N 1s spectra shown

in Fig. 2.2 shows that N would not be introduced on the Ge surface by the $(NH_4)_2S$ treatment.

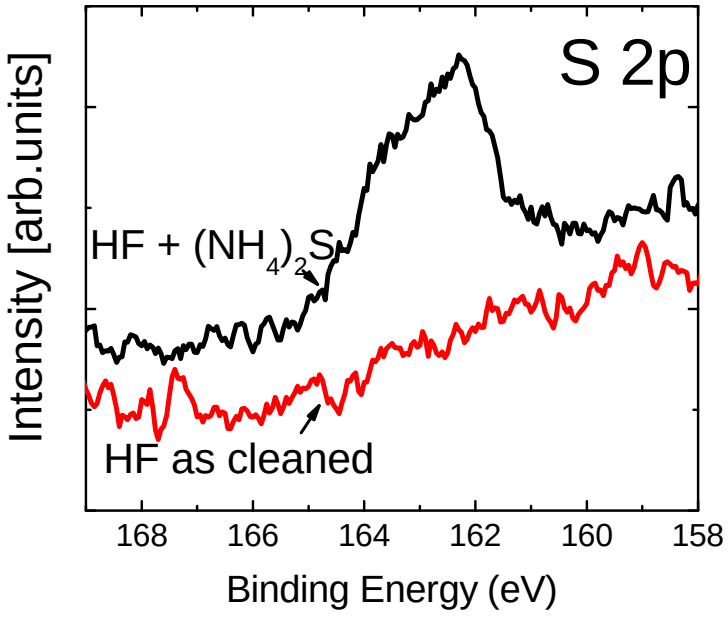

Fig. 2.1. XPS data in S 2p region from Ge(100) substrates after only HF clean or after HF + $(NH_4)_2S$ treatment.

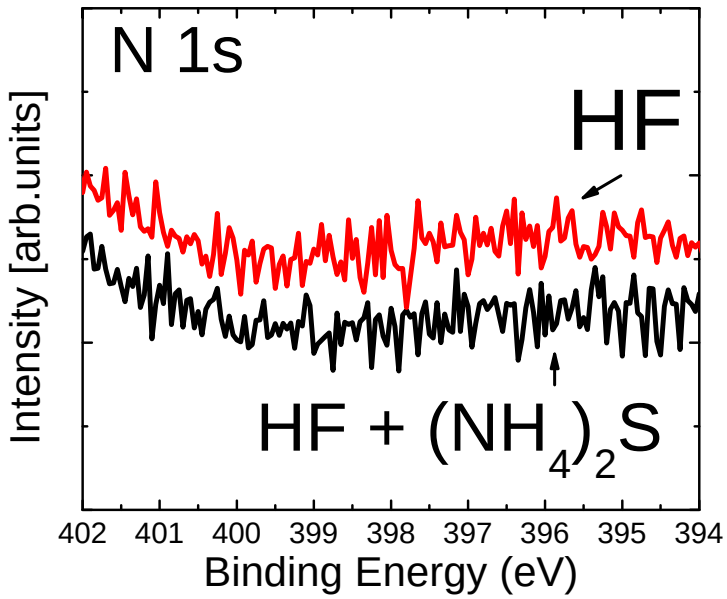

Fig. 2.2. XPS data in N 1s region from Ge(100) substrates after only HF clean or after HF + $(NH_4)_2S$ treatment.

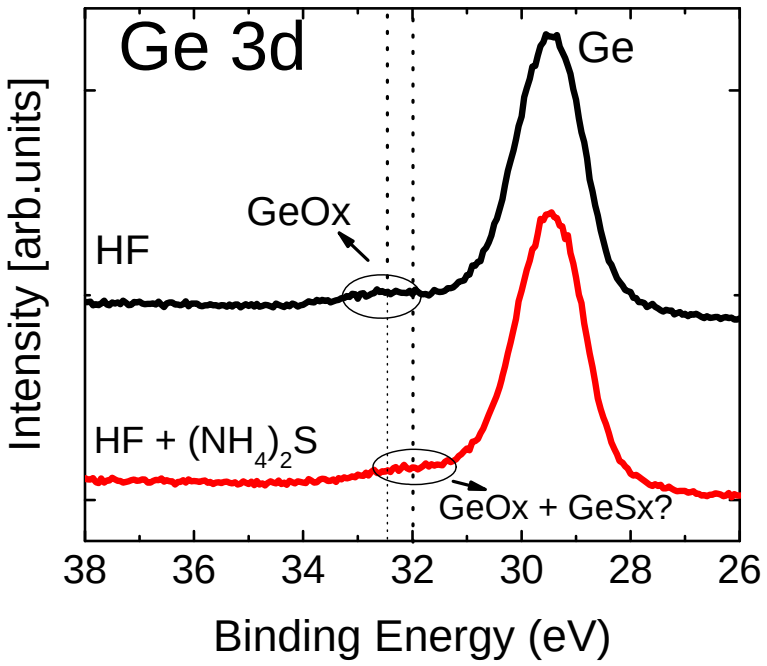

Fig. 2.3. XPS data in Ge 3d region from Ge(100) substrates after only HF clean or after HF + $(NH_4)_2S$ treatment.

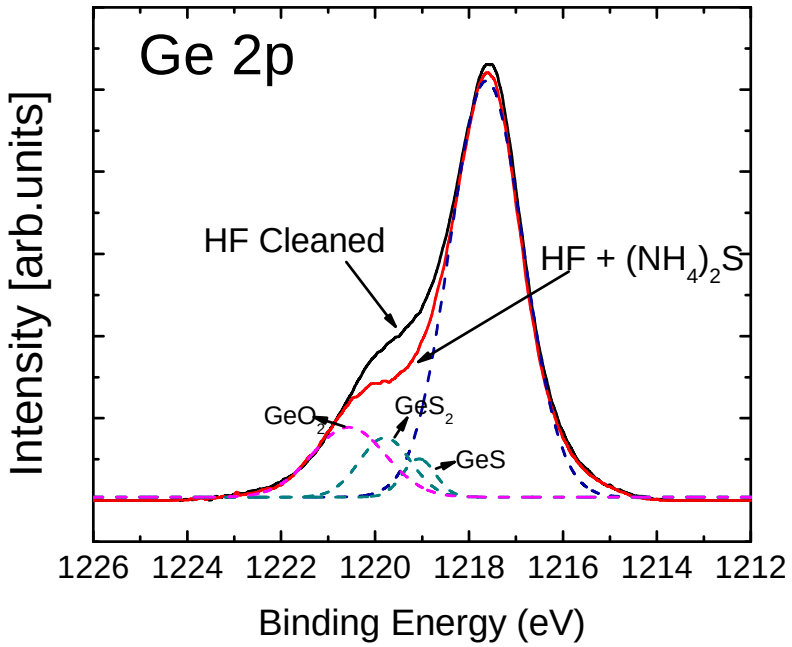

Fig. 2.4. XPS data in Ge 2p region from Ge(100) substrates after only HF clean or after HF + $(NH_4)_2S$ treatment. The dot lines are deconvoluted peaks for sample with $(NH_4)_2S$ treatment.

The XPS data in the Ge 3d signal is shown in Fig.2.3, which demonstrates that both HF-cleaned surface and $(NH_4)_2S$-treated surface are predominantly composed of metallic Ge (~29.7eV) [4] from the substrate. For the samples only cleaned by HF, there is a small peak (signal from 32 to 33eV) which represents GeO_x ($x \leq 2$) [4]. For the samples treated by $(NH_4)_2S$, it is found that this peak shifts to the right slightly (signal from 31.5 to 32.5eV) towards the Ge metallic peak, possibly it is because the Ge-S peak (29.5 to 30.5eV) [4] overlaps with GeO_2 peak (~32.5eV) [4].

To further investigate the surface chemical states after the pre-gate cleaning/treatment, the Ge 2p core level spectrum is shown in Fig.2.4. The main peak located at 1217.6eV is attributed to metallic Ge spectrum from the substrate. The shoulder, for the samples only cleaned by HF, ranging from 1219 to 1221eV, is attributed to GeO_x ($x \leq 2$) bonds [4], which are believed to be introduced during the sample transportation [5]. For the sample treated by $(NH_4)_2S$, the shoulder is smaller. Considering the possible bonds that the Ge atoms may have, it is reasonable to infer that the shoulder after the $(NH_4)_2S$ treatment consists of two types of Ge bonds: Ge-O and Ge-S. Because the shoulder of the $(NH_4)_2S$ treated substrate consists of both Ge-O and Ge-S and the size of the shoulder is smaller than the control sample, the $(NH_4)_2S$ treatment can reduce Ge-O bonds on the surface. From XPS curve fitting results, the total Ge-O bonds are reduced from 34.6% to 14.7%.

The interface state density was measured using frequency-dependent conductance method. The value of D_{it} was extracted according to $D_{it} = 2.5(G_p/\omega)|_{max}/qA$, where

$(G_p/\omega)|_{max}$ is the peak loss value, q is the electronic charge and A is the area. For the samples with $(NH_4)_2S$ treatment and 450°C PMA, D_{it} of 4.8 $\times 10^{11}$ cm^{-2} eV^{-1} at midgap is obtained, which is lower than those reported using surface nitridation [1, 5]; while for the samples without $(NH_4)_2S$ treatment, D_{it} is 1.4$\times$ 10^{12} cm^{-2} eV^{-1}. The improved interface properties in S-treated samples can be possibly explained as the GeOS interfacial layer which may suppress the Ge out-diffusion due to less Ge-O bonds, providing more stable interface properties. On the other hand, for the samples without S passivation, the surface consists of GeO_x and it may enhance Ge out-diffusion [6] and results in poor interface property. To prove this hypothesis, SIMS was performed on HfON/Ge samples. Fig.2.5 shows the Ge depth profiles for samples with or without $(NH_4)_2S$ treatment, it can be seen that more Ge out-diffusion was detected for samples without $(NH_4)_2S$ treatment, while samples with $(NH_4)_2S$ treatment show sharper Ge profiles.

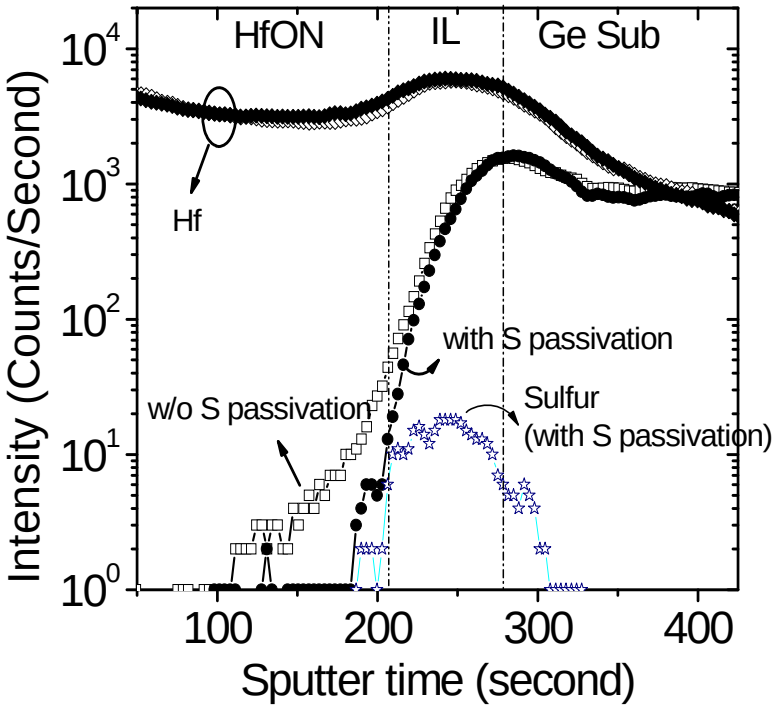

Fig. 2.5. SIMS profiles for HfON/Ge gate stack after 500°C PDA in N_2 ambient for 30s.

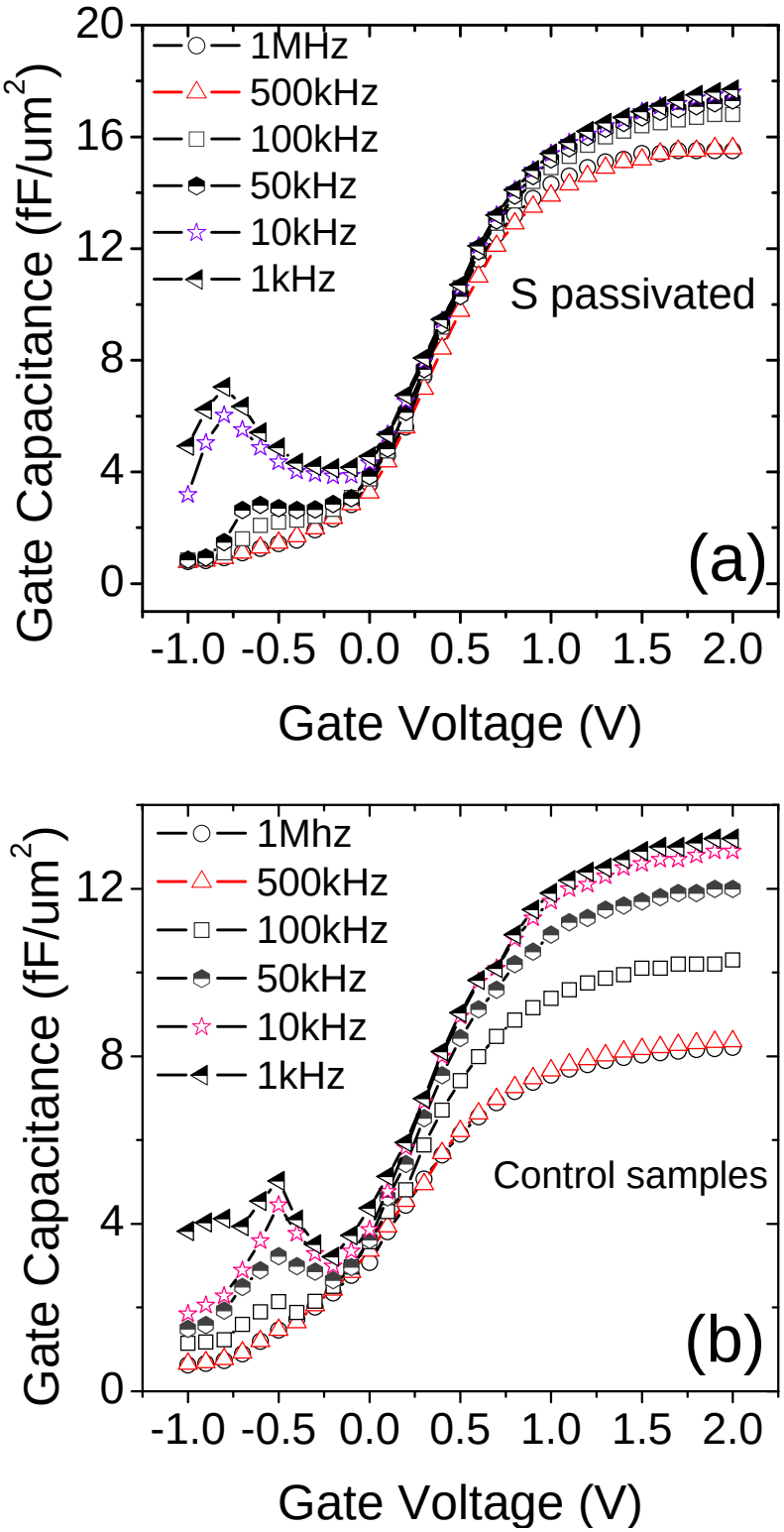

Fig. 2.6. Capacitance-Voltage characteristics of TaN/HfON/Ge capacitors (a) with $(NH_4)_2S$ treatment, (b) without $(NH_4)_2S$ treatment, after a 550°C PMA, in N_2 ambient for 30s.

To understand the thermal stability of S passivation, PMA at different temperature was carried out for samples with and without S passivation. Fig.2.6(a) shows the *C-V* characteristics of the TaN/HfON/Ge MOS capacitors with $(NH_4)_2S$ treatment after 550°C PMA at N_2 ambient for 30s. For comparison, *C-V* characteristics of the Ge MOS capacitor without $(NH_4)_2S$ treatment are plotted in Fig.2.6(b). The frequency dispersion phenomenon in accumulation region at positive gate bias is observed for both samples. The frequency dispersion is possibly attributed to HfO_xN_y bulk traps, because there always would be some bulk traps in high-k gate dielectric. It is also observed that the frequency dispersion is less evident for samples with S passivation. This can be attributed to series resistance [7]. In parallel model, the series resistance R_s is assumed to be negligible compared to the impedance of C/G_p, and is omitted. If this assumption holds valid, parallel model can, in principle, measure *C-V* curves accurately for pretty leaky samples, because the effect of leakage current (G_p) is taken care of. However, when the series resistance is significant, the error involved with neglecting R_s, which is determined by comparing R_s against the magnitude of impedance $|Z| = \sqrt{R^2 + X^2}$, where $R = R_s + \frac{G_p}{G_p{}^2 + \omega^2 C^2}$, $X = -\frac{\omega C}{G_p{}^2 + \omega^2 C^2}$, will increase at higher gate voltage (accumulation region) and at higher measuring frequency, because R_s would be coming close to |Z| in value when the gate leakage (G_p) or frequency (ω) increases. This is why we usually observe the frequency dispersion for the accumulation capacitance as shown in the Fig. 2.7 and 2.8, which are taken from other papers [7, 8]. On the other hand, the frequency dispersion of samples without S passivation is much larger, which could not be

contributed to series resistance induced frequency dispersion alone and may be contributed to additional traps from interface or bulk.

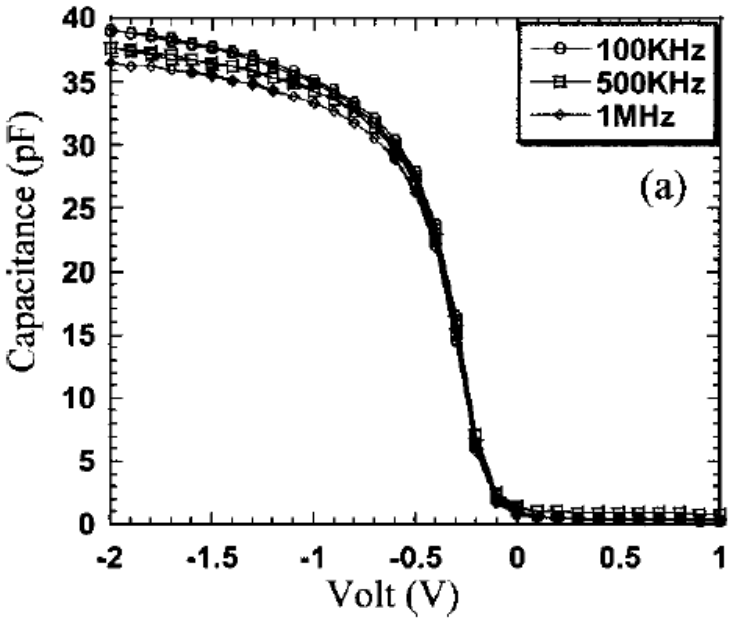

Fig. 2.7. Capacitance–voltage curves measured at 100 kHz, 500 kHz, and 1 MHz for (a) zirconia grown by ozone oxidation [8].

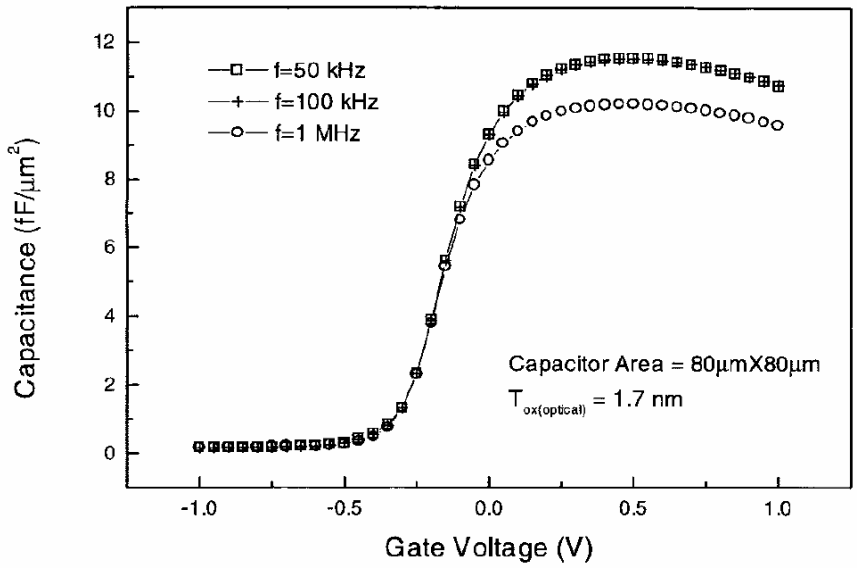

Fig. 2.8. High-frequency *C-V* measurement of MOS capacitor at 50 kHz (square), 100 kHz (cross), and 1 MHz (circle). *C-V* characteristics depend on frequency in the parallel circuit model [7].

To evaluate the quality of the bulk HfO_xN_y, TaN/HfO_xN_y/Si gate stack was also fabricated and the frequency dispersion curves are plotted in Fig. 2.9, it can be seen that the frequency dispersion at accumulation region is small and similar to that of samples with S passivation, which indicates the bulk traps in the HfO_xN_y itself are not severe. The large frequency dispersion of samples without S passivation should be contributed to the Ge out-diffusion. This out-diffusion may degrade both the interface quality and high-k dielectric quality near the interface, which is the source of the large frequency dispersion. The frequency dispersion in inversion may be attributed to the diffusion of impurities from dielectric into substrate which could increase minority carrier generation [9, 10], or perhaps, to the interaction of interface slow states [9].

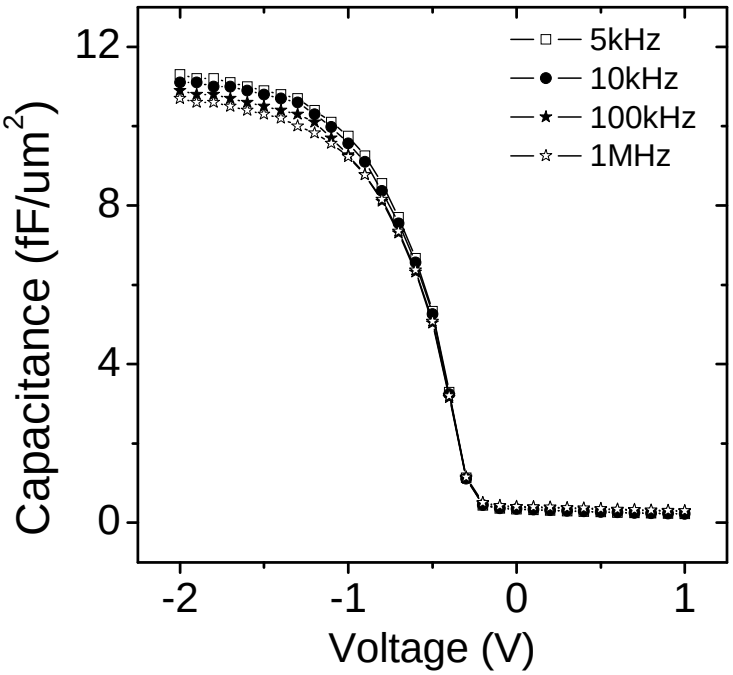

Fig. 2.9. Frequency dispersion characteristics of TaN/HfON/Si capacitors. The dispersion at accumulation region is attributed to the parasitic resistance.

EOT values for the samples were extracted by fitting the *C-V* data, using low frequency curves (1 kHz) in accumulation which are the least affected by shunt resistance

[7], while taking into account the quantum confinement effects. The results are summarized in Fig.2.10. It can be seen that samples with S passivation have a thinner EOT, which indicates a larger k value of dielectric or the thinner interfacial layer than those without S passivation. The decrease of EOT values after higher temperature PMA (550°C) is due to the high-k densification. Further, D_{it} values for the samples with different surface treatments and different PMA temperatures were extracted. The D_{it} degrades significantly ($D_{it} \sim 3\times 10^{12}$ cm^{-2} eV^{-1}) for the samples without S passivation after PMA increased to 550°C, while it shows little difference for the sample with S passivation after 550°C PMA ($D_{it} \sim 5.0\times 10^{11}$ cm^{-2} eV^{-1}). The D_{it} values of samples without S passivation increase after higher temperature PMA is due to more Ge out-diffusion at Ge/high-k interface [11]. Thus, S passivation improves the thermal stability of Ge gate stack.

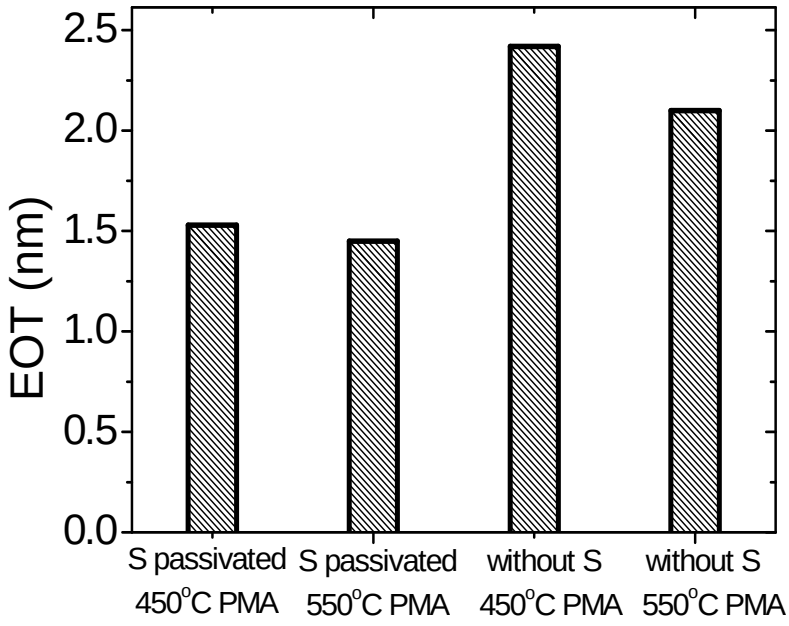

Fig. 2.10. EOT values with different surface treatment and post metal annealing temperatures. Sulfur passivated samples show about 0.7nm thinner EOT.

Fig.2.11 shows the gate leakage current density as a function of EOT together with published data [3, 5, 9, 10, 12]. Fig.2.12 shows the typical J_g-V_g curves of Ge MOS capacitors with different surface treatments or PMA temperatures. Both samples with S passivation or without have low gate leakage current densities about 1×10^{-6}A/cm^2@V_g-V_{fb}=1V. Though samples without S passivation have larger EOT values, this does not improve the gate leakage current. This may due to the poor quality of germanium oxide interfacial layer. It was also found that the gate leakage current decreases and the distribution become more uniform, after the higher temperature (550°C) annealing, especially for the sulfur passivated samples as shown in Fig.2.13. This is because higher temperature annealing can densify the gate dielectric and reduce the bulk traps in the gate oxide as well as weak points. The improvement in gate leakage after higher temperature annealing is less effective for samples without S passivation because of more Ge out-diffusion at elevated temperature.

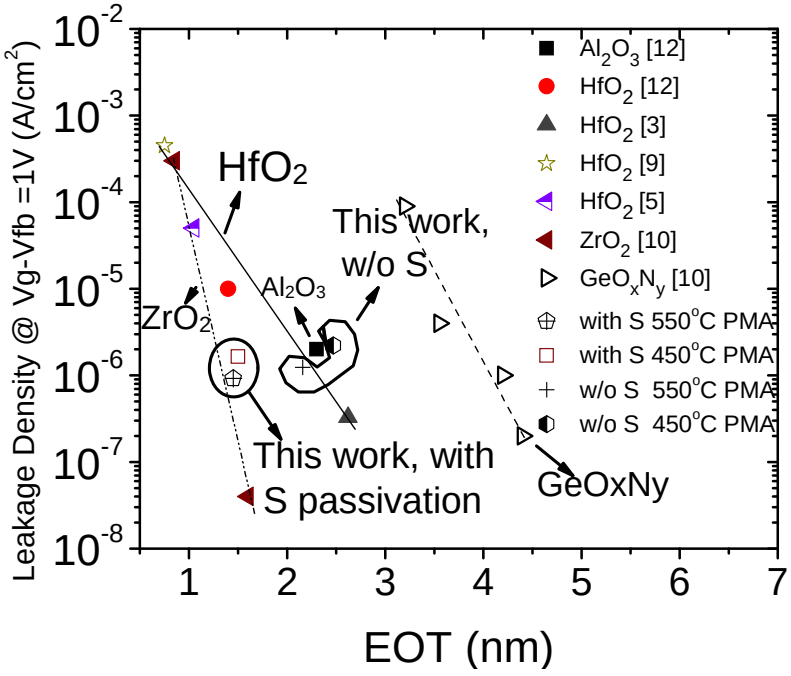

Fig. 2.11. Gate leakage current density as a function of EOT with different surface treatment and PMA temperatures together with published data.

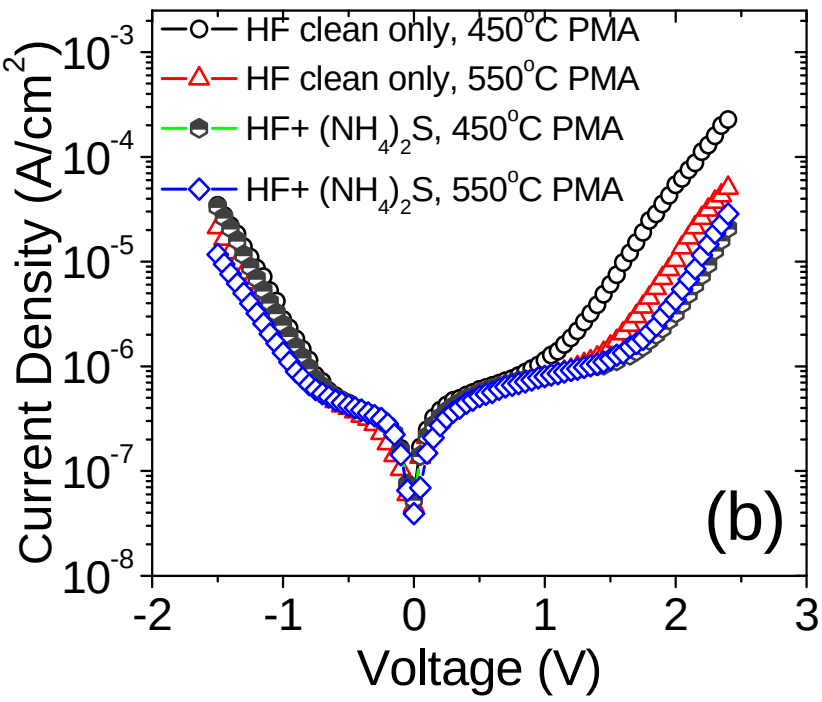

Fig. 2.12. Typical Ig-Vg curves of Ge MOS Capacitors with different surface treatment and PMA temperatures.

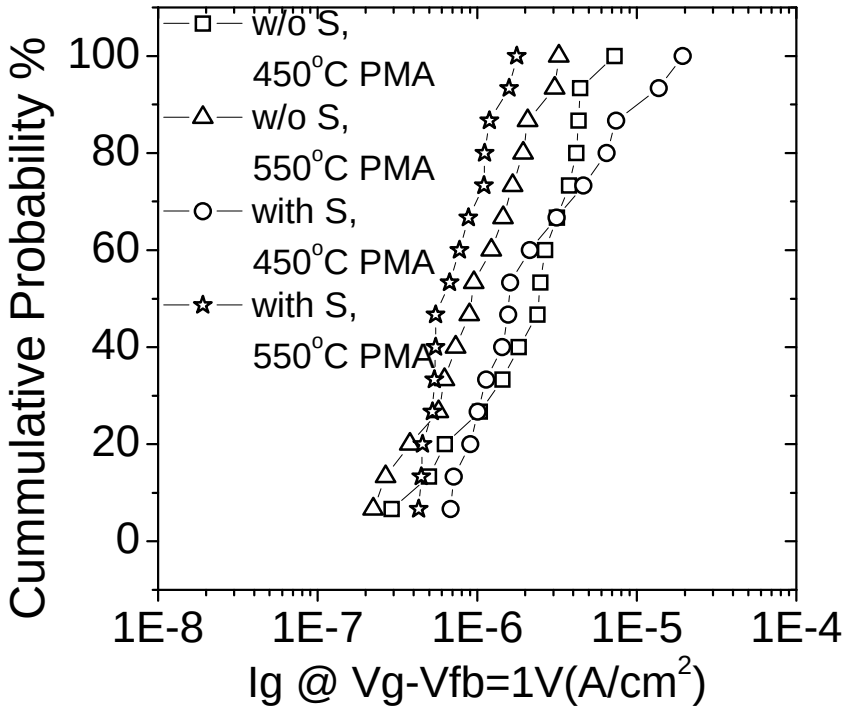

Fig. 2.13. Cumulative probability of leakage current densities of Ge MOS capacitors with different surface treatments and PMA temperatures.

Compared to devices with surface nitridation or Si passivation reported in literature, Ge MOS capacitors with S passivation exhibit comparable or less interface states density (NH_3 nitridation: $1.6\times10^{12}cm^{-2}eV^{-1}$[13], wet No nitridation: $5\times10^{11}cm^{-2}eV^{-1}$ [14], Si passivatio: $\sim4\times10^{11}cm^{-2}eV^{-1}$[13]) and good thermal stability. However, a large hysteresis of flat band voltage (> 800 mV) is present when gate voltage is swept from inversion to accumulation and back to inversion. The presence of larger hysteresis for S passivated samples is also reported in Ref [1] and this is possibly because of the lack of a wide band gap interfacial layer, or due to trapping in the GeOS.

2.3. Conclusions

The effects of the sulfur passivation of Ge using $(NH_4)_2S$ have been investigated. It is found that $(NH_4)_2S$ treatment can reduce the interface state density and improve the electrical properties in terms of EOT and gate leakage current. Moreover, it is found that samples with $(NH_4)_2S$ treatment shows better thermal stability at high-k/Ge interface. This is due to less Ge out diffusion into high-k dielectric by suppressing the germanium monoxide formation at high-k/Ge interface. On the other hand, the large *C-V* hysteresis is observed for Ge MOS capacitors with S passivation and this drawback may limit its application in real high performance Ge MOSFETs fabrication.

References:

[1] M. M. Frank, S. J. Koester, M. Copel, J. A. Ott, V. K. Paruchuri, H. L. Shang, and R. Loesing, "Hafnium oxide gate dielectrics on sulfur-passivated germanium," *Applied Physics Letters,* vol. 89, 112905, Sep 2006.

[2] T. Ohno, "Sulfur passivation of GaAs surfaces," *Physical Review B,* vol. 44, p. 6306, 1991.

[3] C. O. Chui, H. Kim, P. C. McIntyre, and K. C. Saraswat, "Atomic layer deposition of high-k dielectric for germanium MOS applications-substrate surface preparation," *IEEE Electron Device Letters,* vol. 25, pp. 274-276, May 2004.

[4] *NIST X-ray Photoelectron Specroscopy Database, NIST Standard Reference Database 20, Version 3.3 (Web Version).*

[5] N. Wu, Q. C. Zhang, C. X. Zhu, C. C. Yeo, S. J. Whang, D. S. H. Chan, M. F. Li, B. J. Cho, A. Chin, D. L. Kwong, A. Y. Du, C. H. Tung, and N. Balasubramanian, "Effect of surface NH_3 anneal on the physical and electrical properties of HfO_2 films on Ge substrate," *Applied Physics Letters,* vol. 84, pp. 3741-3743, May 2004.

[6] N. Lu, W. Bai, A. Ramirez, C. Mouli, A. Ritenour, M. L. Lee, D. Antoniadis, and D. L. Kwong, "Ge diffusion in Ge metal oxide semiconductor with chemical vapor deposition HfO_2 dielectric," *Applied Physics Letters,* vol. 87, 051922, Aug 2005.

[7] K. J. Yang and C. M. Hu, "MOS capacitance measurements for high-leakage thin dielectrics," *IEEE Transactions on Electron Devices,* vol. 46, pp. 1500-1501, Jul 1999.

[8] S. Ramanathan, D. A. Muller, G. D. Wilk, C. M. Park, and P. C. McIntyre, "Effect of oxygen stoichiometry on the electrical properties of zirconia gate dielectrics," *Applied Physics Letters,* vol. 79, pp. 3311-3313, Nov 2001.

[9] A. Dimoulas, G. Mavrou, G. Vellianitis, E. Evangelou, N. Boukos, M. Houssa, and M. Caymax, "HfO_2 high-k gate dielectrics on Ge(100) by atomic oxygen beam deposition," *Applied Physics Letters,* vol. 86, 032908, Jan 2005.

[10] C. O. Chui, H. Kim, D. Chi, P. C. McIntyre, and K. C. Saraswat, "Nanoscale germanium MOS dielectrics - Part II: High-k gate dielectrics," *IEEE Transactions on Electron Devices,* vol. 53, pp. 1509-1516, Jul 2006.

[11] Q. C. Zhang, N. Wu, D. M. Y. Lai, Y. Nikolai, L. K. Bera, and C. X. Zhu, "Germanium incorporation in HfO_2 dielectric on germanium substrate," *Journal of the Electrochemical Society,* vol. 153, pp. G207-G210, 2006.

[12] J. J. H. Chen, N. A. Bojarczuk, H. L. Shang, M. Copel, J. B. Hannon, J. Karasinski, E. Preisler, S. K. Banerjee, and S. Guha, "Ultrathin Al_2O_3 and HfO_2 gate dielectrics on surface-nitrided Ge," *IEEE Transactions on Electron Devices,* vol. 51, pp. 1441-1447, Sep 2004.

[13] N. Wu, Q.Zhang, N. Balasubramanian, D. S. H. Chan, C. Zhu, "Characteristics of self-aligned gate-first Ge p- and n-channel MOSFETs using CVD HfO_2 gate dielectric and Si

surface passivation", *IEEE Transactions on Electron Devices*, vol. 54, pp. 733-741, Apr 2007.

[14] J. P. Xu, P. T. Lai, C. X. Li, X. Zou, C. L. Chan, "Improved electrical properties of germanium MOS capacitors with gate dielectric grown in wet-NO ambient", *IEEE Electron Device Letters*, vol. 27, pp. 439-441, June 2006.

Chapter 3

Effects of Silicon Nitride Passivation on High-k/Ge Gate Stack

It is now clear that Ge p-type MOSFETs (pMOSFETs) with excellent performance can be achieved through various careful surface passivation process [1-11]. Among those surface passivation techniques, silicon (Si) passivation attracts many interest [1, 2, 6-8, 12, 13] because of easier process integration with current Si platform. However, a number of issues remain unsolved for Si passivation, such as unexpected positive shift in threshold voltage (V_{th}) for Ge pMOSFETs [1, 2]. Also, the Si cap layer thickness gives strong impacts on device performance [6-8]. The Ge out-diffusion is still found to be serious and an ultrathin Si layer (<5 monolayer) can not adequately passivate the Ge [8], possibly because the fully oxidization of the Si passivation layer and subsequent formation of volatile GeO at SiO_x/Ge interface, which takes place when Si passivation layer is thin and the thickness ratio between HfO_2 and Si is large [6, 8]. This limits the process window and equivalent oxide thickness (EOT) scaling capability. In this chapter, a novel silicon nitride (SN) passivation by SiH_4-NH_3 treatment is proposed and demonstrated for Ge MOS devices. Compared to Si passivation layer, SN layer is more effective to suppress the Ge out diffusion, resulting improved interface quality and electrical characteristics. In addition, SN passivation also eliminates the unexpected positive shift in V_{th}. This is explained by the suppression of the interfacial dipoles formation.

3.1. Experiments

The starting wafers are N-type Ge with (100) orientation. After HF dilution (1:50) and DI water cyclic rinsing [14], an ultrathin SN passivation layer ~6Å was deposited on Ge by SiH_4-NH_3 treatment carried out at 400^oC under a process pressure of 5 torr (the flow rates of SiH_4, NH_3, and N_2 were 60, 60, and 250 sccm, respectively), as described in [15], followed by in-situ deposition of an HfO_2 layer of 11.5 nm by metal organic chemical vapor deposition (MOCVD) at 400^oC. Control sample was made with 6Å Si cap by SiH_4 treatment as described in [13] at a reduced temperature of 400^oC and an HfO_2 layer of the same thickness. Post deposition annealing (PDA) at 500^oC in N_2 ambient for 60 sec was performed for both samples, After that, a 130 nm TaN gate electrode was sputtered and followed by lithography and dry etching. The source/drain was formed by boron implantation (15 keV, 1E15 cm^{-2}) and Al metal contact.

3.2. Physical effects of silicon nitride passivation

After SiH_4 or SiH_4-NH_3 treatment, some Ge samples were sent to ex-situ high resolution XPS measurements immediately (within 5 min, but the samples were still exposed to air). Fig. 3.1 (a) compares the Ge2p spectra between the two samples. A shoulder located around 1220 eV is observed for the sample with Si passivation, which is due to the Ge-O bond formation [16]. Why the Ge surface became oxidized even capped with a Si layer? This is because the Si cap layer can be easily oxidized when it is exposed to the oxidized ambient (e.g. air, or CVD HfO_2 process). Thus we can see that ultrathin Si layer can not effectively passivate Ge, since oxidized ambient is inevitable during the gate dielectric deposition process and volatile GeO can be formed once the Si cap layer is

fully oxidized. For the sample with SN passivation, nitrogen peak is clearly observed as shown in Fig. 3.1(b). The shoulder in Fig. 3.1(a) is less evident, suggesting that SN cap layer acts as a better barrier against oxygen.

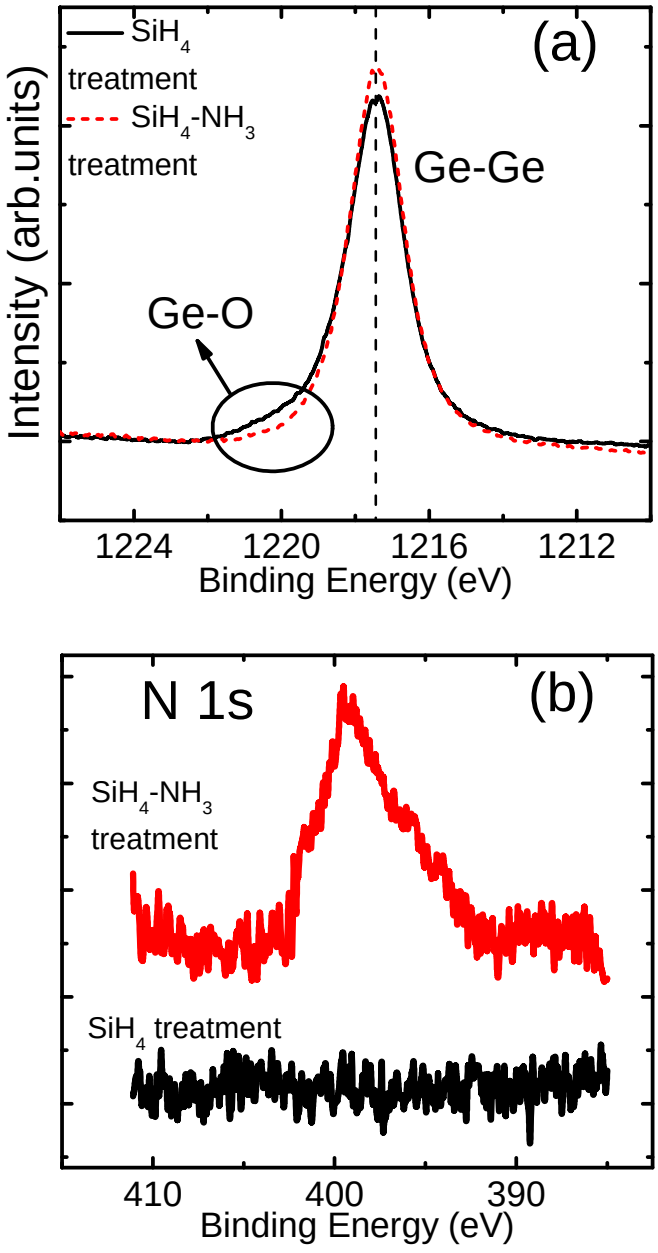

Fig. 3.1.(a) High resolution XPS data in (a) Ge 2p and (b) N 1s for Ge wafers after SiH_4 or SiH_4-NH_3 treatment. Ultrathin (~6Å) Si passivation layer by SiH_4 treatment can not adequately prevent GeO_x formation at Ge surface when sample is exposed to oxidized ambient (e.g. air).

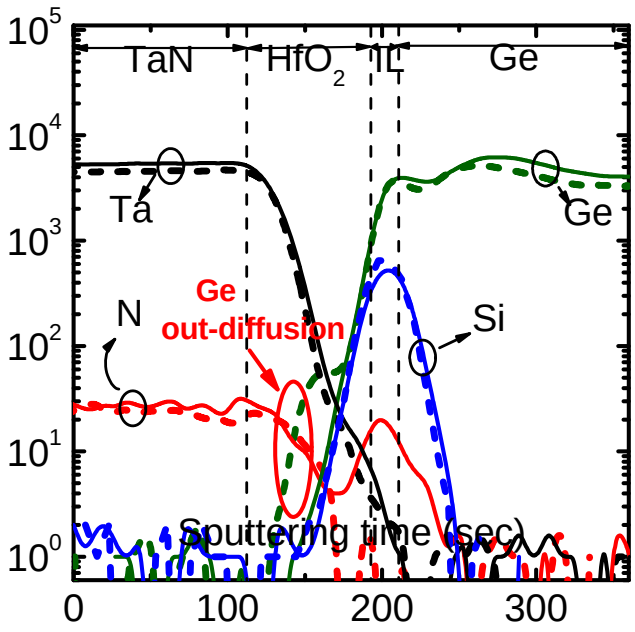

Fig. 3.2. SIMS profiles for HfO_2 gated Ge MOS capacitors with Si passivation (dash) and silicon nitride (SN) passivation (solid). Red: N. Blue: Si. Green: Ge. Ta: Black.

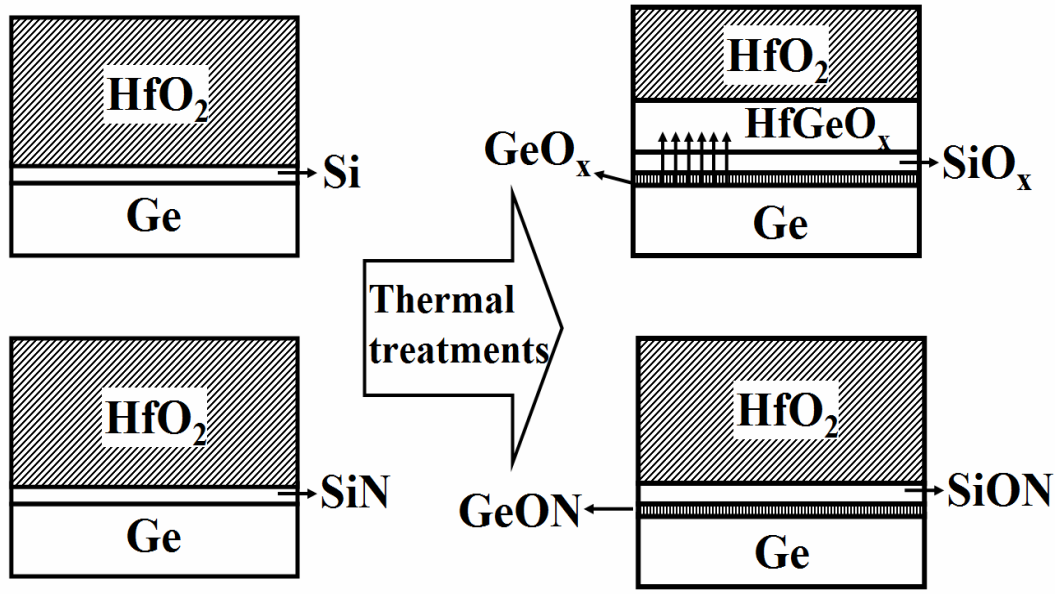

Fig. 3.3. Schematic illustration of better passivation effects by silicon nitride layer. After thermal treatments, ultrathin Si layer can be oxidized, especially when HfO_2 thickness is large and subsequently, volatile GeO could be formed and results serious Ge out-diffusion. Introduction of N can suppress volatile GeO formation at high-k/Ge interface.

Suppressing the GeO formation at interface is critically important to minimize the Ge out diffusion into the high-k gate dielectrics. Fig. 3.2 shows the SIMS profiles for TaN/HfO_2 gated Ge MOS capacitors with Si or SN passivation. The Si peaks are similar for both samples. For the sample with SN passivation, an additional N peak is observed at the interface. It is found that sample with SN passivation exhibits much less Ge out diffusion into the high-k dielectrics. As illustrated in Fig. 3.3, the ultrathin Si layer could be easily oxidized during the HfO_2 deposition and annealing [6] and the volatile GeO can be formed subsequently, which leads a significant Ge diffusion for sample with Si passivation [17]. On the other hand, SN is less easily to be oxidized because Si-N bond (~4.88 eV) is stronger than Si-Si bond (~3.37 eV) [18]. Also, the N incorporation at the interface can turn any volatile GeO_x to more stable GeO_xN_y. Therefore, much less Ge out diffusion is observed for sample with SN passivation.

Recently, it has been reported that area density difference of oxygen atoms forces the oxygen atom to move from higher density materials to lower density one [19]. At the high-k/SiO_2 interface, the common atom for both materials is oxygen. Thus, the oxygen atom should self-adjust the bonding characteristics at the interface. The oxygen atom density difference forces the oxygen atom to move from one to another oxide at the interface, resulting in an oxygen vacancy and excess oxygen formation in the respective side. It is considered that the increase of structural energy at the hetero-interface would be relaxed by such “dipole” formation, although the dipole formation increases the electronic energy. This is understandable by considering that the total energy composed of electronic and structural components should be minimized to stabilize the interface.

This model also explains why the dipole is not formed on SiNx, where the oxygen self-adjustment is not expected to occur [19]. In case of HfO_2 and SiO_2, the oxygen is transferred from HfO_2 to SiO_2. The self-adjustment of oxygen atoms causes the dipole formation and positive V_{th} shift [1, 2]. This is also consistent with the observation of positive flat band voltage (V_{fb}) shift for sample with Si passivation as shown in Fig. 3.6 (a). On the other hand, in the case of SN, the oxygen self-adjustment is not expected to occur [19]. Therefore the dipole is not formed on SN and unexpected positive V_{th} shift can be eliminated for sample with SN passivation.

Fig. 3.4 shows the summary of dipole formation for various high-k oxides [19]. The oxygen can be transferred from left to right among those oxides due to the area density difference of oxygen atoms. As illustrated in Fig. 3.5(a), once the Si cap layer is fully oxidized, the oxygen will tend to transfer from HfO_2 to SiO_2 and to GeO_x. The transfer of oxygen from high-k to Ge may further enhance the Ge out-diffusion. The oxygen self-adjustment behavior between HfO_2 and SN is less evident. This may also help to minimize the Ge out-diffusion. According to the Fig. 3.4, if the interfacial layer between the HfO_2 and Ge is Y_2O_3, Lu_2O_3, La_2O_3 or SrO, the direction of oxygen transfer will be opposite to the SiO_2 case and doesn't favor the Ge out-diffusion as shown in Fig. 3.5(b). This is possibly why recently it has been reported that interfacial layer containing La [20], Y [21] or Sr [10] greatly improves the interface quality.

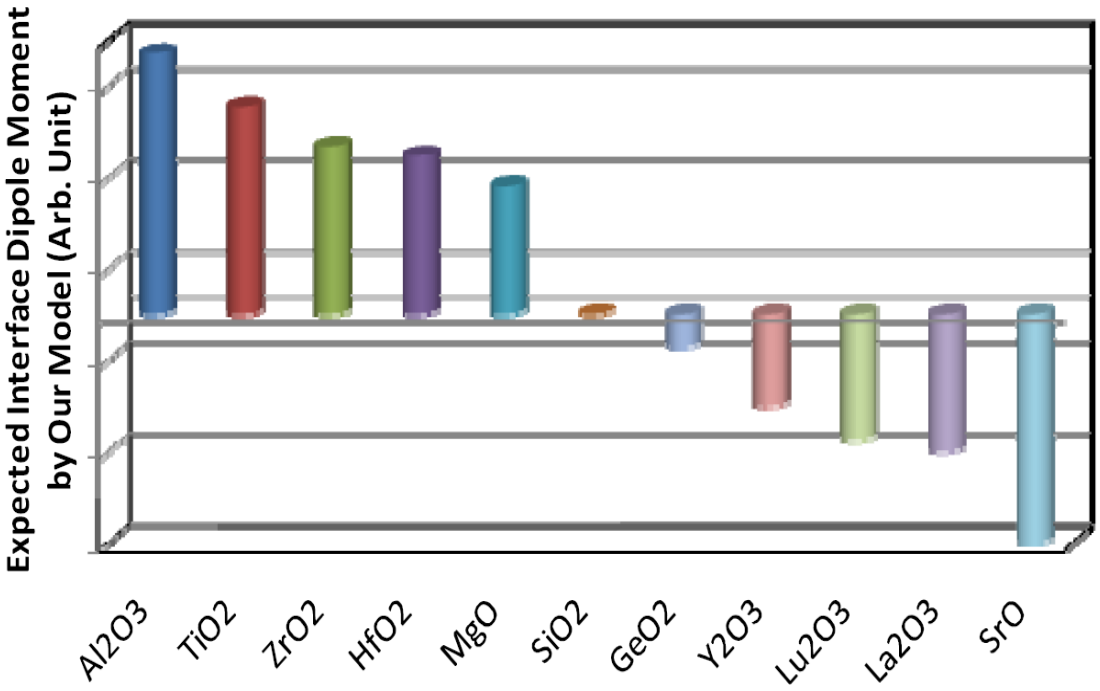

Fig. 3.4. Summary of the dipole moment formed at high-k/SiO_2 interface predicted by our model, for various high-k candidates including GeO_2. The dipole direction to increase *VFB* is represented as a positive direction [19].

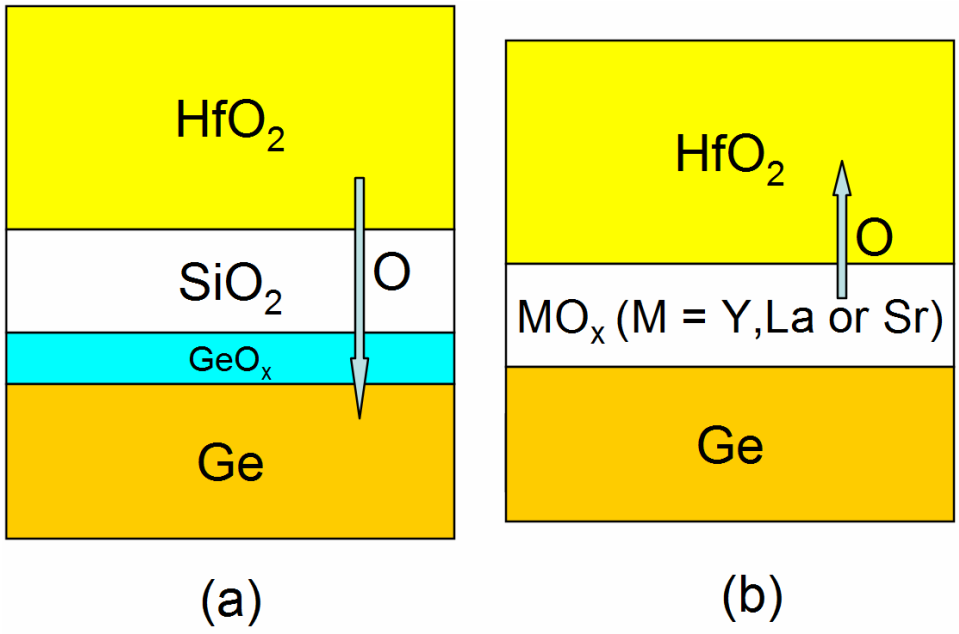

Fig. 3.5. Oxygen transfer direction for (a)$HfO_2/SiO_2/GeO_x$/Ge gate stack and (b)HfO_2/MO_x/Ge gate stack (M = Y, La or Sr).

3.3. Electrical effects of silicon nitride passivation

Fig. 3.6 compares the *C-V* characteristics between the MOS capacitors with Si passivation and SN passivation. MOS capacitors with Si passivation exhibit very serious frequency dispersion phenomenon. The weak inversion response [22] is clearly observable at measuring frequency as high as 100 kHz. The *C-V* curves are also severely stretched out from ideal *C-V* curves. MOS capacitors with silicon nitride passivation exhibit much better *C-V* characteristics than that with Si passivation. The weak inversion

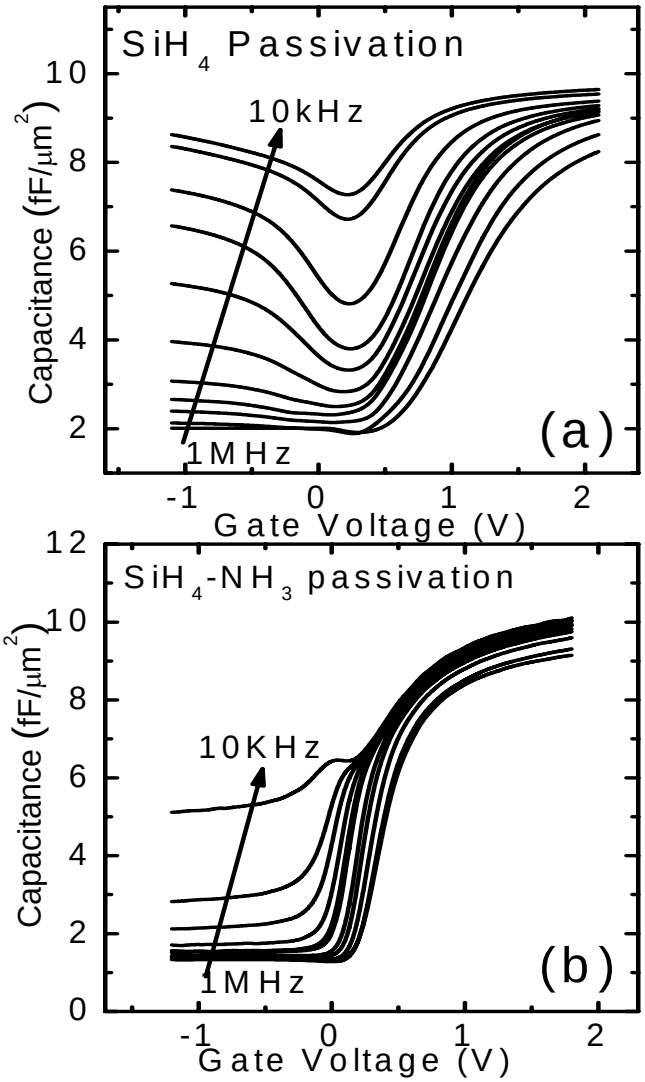

Fig. 3.6. *C-V* characteristics of HfO_2 gated Ge MIS capacitors with (a) Si passivation and (b) SN passivation measured at 1MHz, 800kHz, 500kHz, 300kHz, 200kHz, 100kHz, 80kHz, 50kHz, 30kHz, 20kHz and 10kHz.

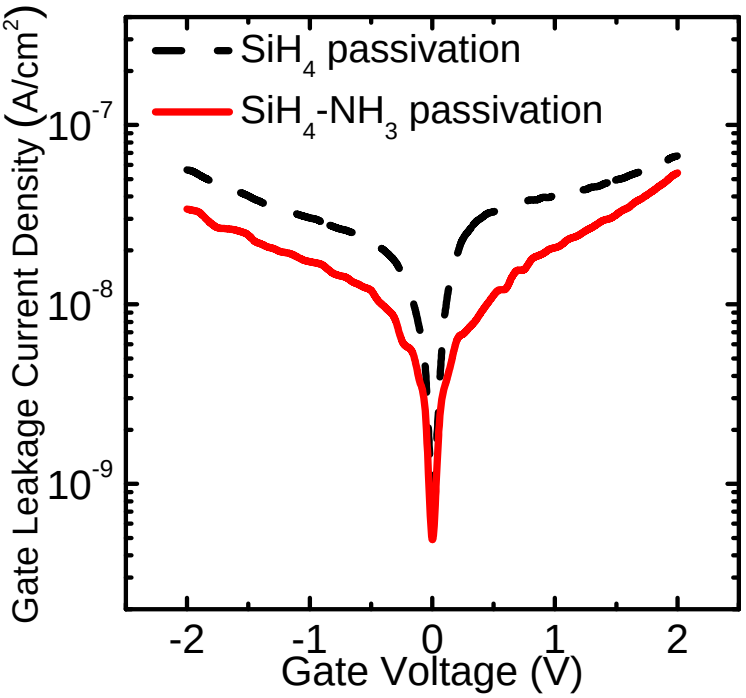

Fig. 3.7. Gate leakage current densiy for samples with Si passivation and SN passivation. Smaller J_g is observed for devices with SN passivation.

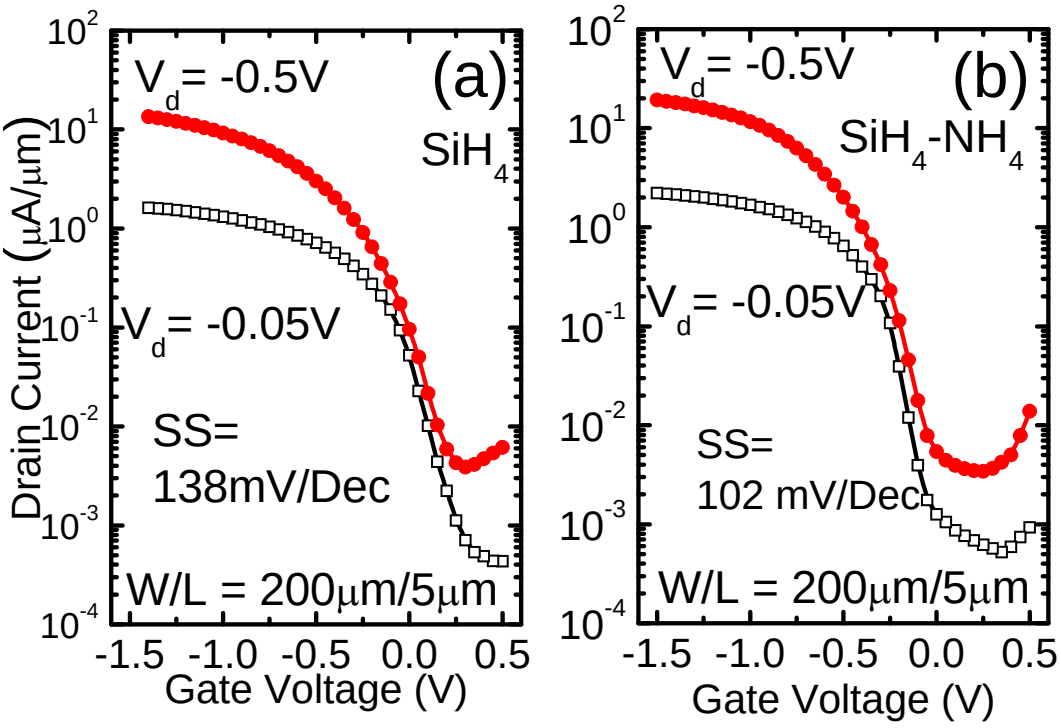

Fig. 3.8. Well-behaved I_d-V_g characteristics for Ge pMOSFETs (L = 5 μm) with (a) Si passvation and (b) SN passivation.

response becomes clear only when the measuring frequency is lower than 20 kHz and there are also much less stretch-outs in *C-V* slopes, indicating a much lower interface trap density. EOT values were extracted by fitting the *C-V* data using lower frequency curves (10 kHz) in accumulation which are the least affected by series resistance [23] and it was found that MOS capacitors with silicon nitride passivation have slightly smaller EOT values (2.95 nm) than that with silicon passivation (3.03 nm). The leakage current densities are plotted in Fig. 3.7 and it can be seen that MOS capacitors with SN passivation layer exhibit smaller gate leakage current than that with Si passivation, probably due to less trap assisted tunneling.

Fig. 3.8 shows the I_d-V_g characteristics. Samples with SN passivation exhibit higher drain current and smaller sub-threshold swing (SS). The positive shift of V_{th} for sample with Si passivation is due to the dipole formation at interface. Interface qualities were further characterized by variable rise/fall time charge pumping method, which will be further discussed in detail in Chapter 5. Samples with Si passivation exhibit higher charge pumping currents than that of samples with SN passivation at any rise/fall time condition, indicating higher interface trap density as shown in Fig. 3.9. The mean interface trap density (D_{it}) was extracted by plotting I_{cp} / f as function of $\ln(t_r \times t_f)^{1/2}$ [24] as shown in Fig. 3.10, where I_{cp} is the charge pumping current, f is the frequency, t_r and t_f is the rise time and fall time, respectively. The mean D_{it} is 4.85×10^{12} $cm^{-2}eV^{-1}$ for sample with Si passivation and 8.73×10^{11} $cm^{-2}eV^{-1}$ for sample with SN passivation. It can be seen that minimizing the unstable GeO_x formation at high-k/Ge interface is very important to achieve low D_{it}.

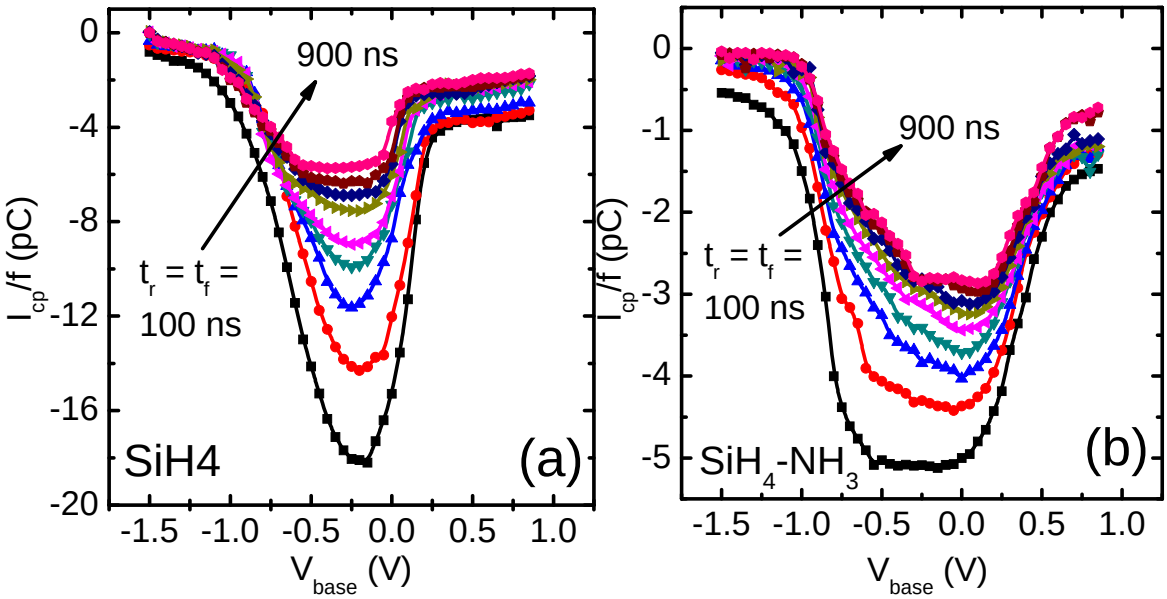

Fig. 3.9. Rise and fall time dependence of charge pumping (CP) currents (t_r = t_f = 100, 200, 300, 400, 500, 600, 700, 800, and 900 ns) for samples with (a) Si passivation and (b) SN passivation. The area is 14400μm^2, amplitude is 1V and frequency is 200 kHz.

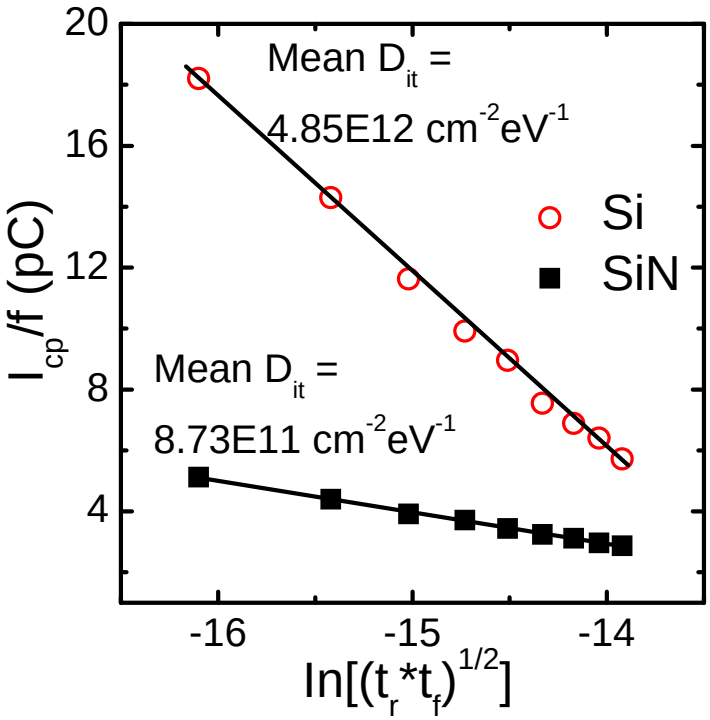

Fig. 3.10. Q_{cp}(= I_{cp}/f) as a function of $\ln(t_r \times t_f)^{1/2}$ that provides the mean D_{it} for samples with Si or SN passivation.

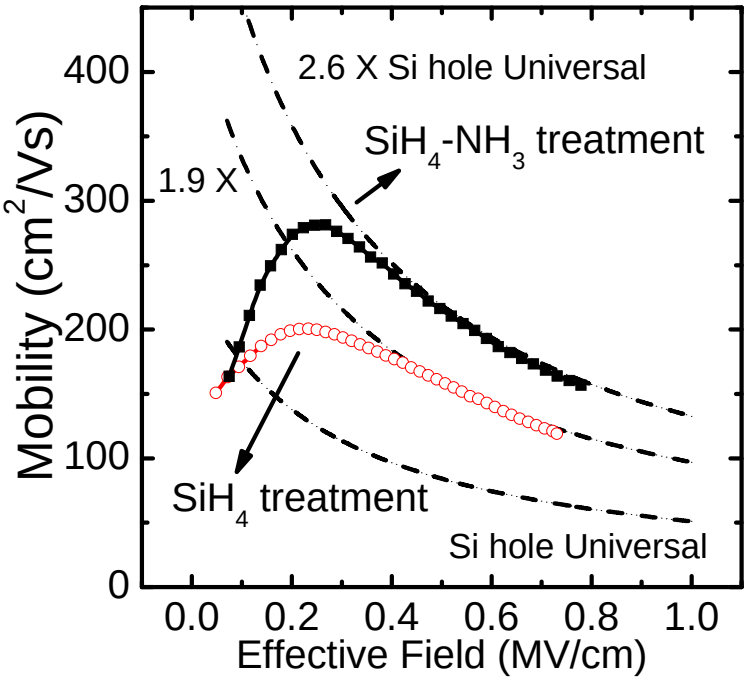

Fig. 3.11. Hole mobility as a function of vertical effective vertical field for Ge pMOSFETs (L = 5μm) with Si or SN passivation.

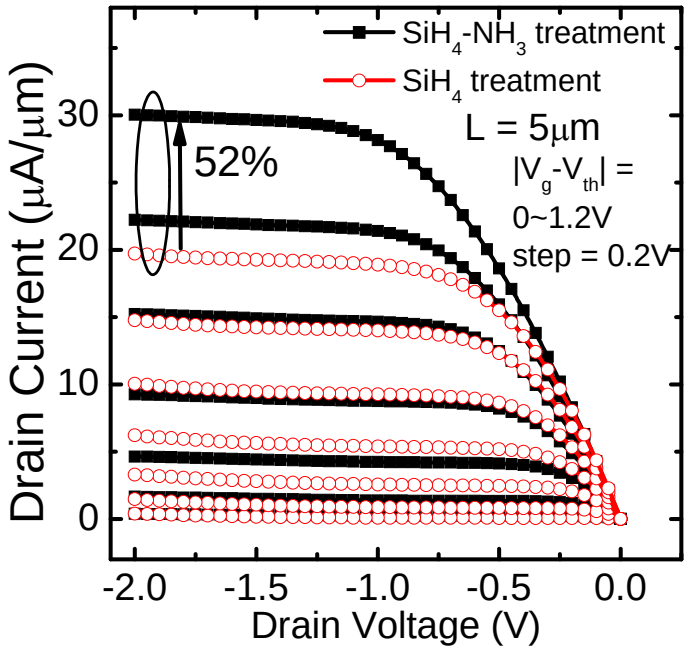

Fig. 3.12. I_d-V_d for Ge pMOSFETs (L = 5 μm). About 52% enhanced drive current is obtained for SN passivated device at V_g-V_t = -1.2V and V_d= -2V.

The hole mobility as a function of vertical effective field is plotted in Fig. 3.11 by split *C-V* method. The effective channel electrical fields were estimated by

$$E_{eff} = \frac{Q_b + nQ_i}{k_{Ge}\varepsilon_0}$$

where k_{Ge} is the Ge dielectric constant, ε_0 is the permittivity of vacuum. The value of "*n*" that offers the universal relationship should be determined experimentally by comparing the mobilities on the different impurity concentrations. For Si, systematic studies have been done and $n = \frac{1}{3}$ has been clarified [25]. However, for Ge, there is no such detail study to explore the correct "*n*" value yet except [7]: they have investigated the Ge pMOSFETs with different impurity concentration and they found that by choosing $n = \frac{1}{3}$, the mobility in moderately high field region fall on a single curve, i.e. the universality is obtained. So we believe n = 1/3 is still a reasonable value for Ge pMOSFETs. About 2.6 × Si universal hole mobility is achieved for sample with SN passivation, which is 40% higher than that with Si passivation. Fig. 3.12 shows the output characteristics, sample with SN passivation shows ~50% higher drain current at V_d = 2 V and V_g-V_t = -1.2 V.

3.4. Conclusions

An alternative surface passivation technique using SN by SiH_4-NH_3 treatment has been demonstrated on HfO_2 gated Ge MOS devices. By suppressing the interface dipole formation, SN passivation layer eliminates the positive V_{th} shift problem of Si passivation. Compared to Si passivation, SN passivation is also demonstrated to be more effective to

suppress the Ge out-diffusion into HfO_2. It improves the electrical characteristics like *C-V* frequency dispersion, gate leakage and mobility. SN passivation offers bigger process window than Si passivation and can be a promising technique for high-k/Ge gate stack.

References:

[1] P. Zimmerman, G. Nicholas, B. De Jaeger, B. Kaczer, A. Stesmans, L. A. Ragnarsson, D. P. Brunco, F. E. Leys, M. Caymax, G. Winderickx, K. Opsomer, M. Meuris, and M. M. Heyns, "High performance Ge pMOS devices using a Si-compatible process flow," in *IEEE International Electron Devices Meeting*, San Francisco, CA, 2006, pp. 390-393.

[2] S. Joshi, C. Krug, D. Heh, H. J. Na, H. R. Harris, J. W. Oh, P. D. Kirsch, P. Majhi, B. H. Lee, H. H. Tseng, R. Jammy, J. C. Lee, and S. K. Banerjee, "Improved Ge surface passivation with ultrathin SiO_x enabling high-mobility surface channel pMOSFETs featuring a HfSiO/WN gate stack," *IEEE Electron Device Letters,* vol. 28, pp. 308-311, Apr 2007.

[3] D. Kuzum, A. J. Pethe, T. Krishnamohan, Y. Oshima, S. Yun, J. P. McVittie, P. A. Pianetta, P. C. McLntyre, and K. C. Saraswat, "Interface-Engineered Ge (100) and (111), N- and P-FETs with High Mobility," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 723-726.

[4] G. Nicholas, B. De Jaeger, D. P. Brunco, P. Zimmerman, G. Eneman, K. Martens, M. Meuris, and M. M. Heyns, "High-performance deep submicron Ge pMOSFETs with halo implants," *IEEE Transactions on Electron Devices,* vol. 54, pp. 2503-2511, Sep 2007.

[5] T. Takahashi, T. Nishimura, L. Chen, S. Sakata, K. Kita, and A. Toriumi, "Proof of Ge-interfacing concepts for metal/high-k/Ge CMOS Ge-intimate material selection and interface conscious process flow," in *IEEE International Electron Devices Meeting*, Washington, DC, 2007, pp. 697-700.

[6] N. Wu, Q. C. Zhang, N. Balasubramanian, D. S. H. Chan, and C. X. Zhu, "Characteristics of self-aligned gate-first Ge p- and n-channel MOSFETs using CVD HfO_2 gate dielectric and Si surface passivation," *IEEE Transactions on Electron Devices,* vol. 54, pp. 733-741, Apr 2007.

[7] T. Yamamoto, Y. Yamashita, M. Harada, N. Taoka, K. Ikeda, K. Suzuki, O. Kiso, N. Sugiyama, and S. Takagi, "High Performance 60 nm Gate Length Germanium p-MOSFETs with Ni Germanide Metal Source/Drain," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 1041-1043.

[8] J. Mitard, B. De Jaeger, F. E. Leys, G. Hellings, K. Martens, G. Eneman, D. P. Brunco, R. Loo, J. C. Lin, D. Shamiryan, T. Vandeweyer, G. Winderickx, E. Vrancken, C. H. Yu, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, and M. M. Heyns, "Record I_{ON}/I_{OFF} performance for 65nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability," in *IEEE International Electron Devices Meeting*, San Francisco, CA, 2008, pp. 873-876.

[9] Y. Nakakita, R. Nakane, T. Sasada, H. Matsubara, M. Takenaka, and S. Takagi, "Interface-controlled Self-Align Source/Drain Ge pMOSFETs Using Thermally-Oxidized GeO_2 Interfacial Layers," in *IEEE International Electron Devices Meeting*, San Francisco, CA, 2008, pp. 877-880.

[10] Y. Kamata, A. Takashima, Y. Kamimuta, and T. Tezuka, "New approach to form EOT-scalable gate stack with strontium germanide interlayer for high-k/Ge MISFETs," in *VLSI Technology, 2009 Symposium on*, 2009, pp. 78-79.

[11] D. Kuzum, A. J. Pethe, T. Krishnamohan, and K. C. Saraswat, "Ge (100) and (111) N- and P-FETs With High Mobility and Low-T Mobility Characterization," *IEEE Transactions on Electron Devices,* vol. 56, pp. 648-655, Apr 2009.

[12] N. Wu, Q. C. Zhang, C. X. Zhu, D. S. H. Chan, A. Y. Du, N. Balasubramanian, M. F. Li, A. Chin, J. K. O. Sin, and D. L. Kwong, "A TaN-HfO_2-Ge pMOSFET with novel SiH_4 surface passivation," *IEEE Electron Device Letters,* vol. 25, pp. 631-633, Sep 2004.

[13] N. Wu, Q. C. Zhang, C. X. Zhu, D. S. H. Chan, M. F. Li, N. Balasubramanian, A. Chin, and D. L. Kwong, "Alternative surface passivation on germanium for metal-oxide-semiconductor applications with high-k gate dielectric," *Applied Physics Letters,* vol. 85, pp. 4127-4129, Nov 2004.

[14] C. O. Chui, H. Kim, P. C. McIntyre, and K. C. Saraswat, "Atomic layer deposition of high-k dielectric for germanium MOS applications-substrate surface preparation," *IEEE Electron Device Letters,* vol. 25, pp. 274-276, May 2004.

[15] H. C. Chin, M. Zhu, X. K. Liu, H. K. Lee, L. P. Shi, L. S. Tan, and Y. C. Yeo, "Silane-Ammonia Surface Passivation for Gallium Arsenide Surface-Channel n-MOSFETs," *IEEE Electron Device Letters,* vol. 30, pp. 110-112, Feb 2009.

[16] N. Wu, Q. C. Zhang, C. X. Zhu, C. C. Yeo, S. J. Whang, D. S. H. Chan, M. F. Li, B. J. Cho, A. Chin, D. L. Kwong, A. Y. Du, C. H. Tung, and N. Balasubramanian, "Effect of surface NH_3 anneal on the physical and electrical properties of HfO_2 films on Ge substrate," *Applied Physics Letters,* vol. 84, pp. 3741-3743, May 2004.

[17] K. Kita, S. Suzuki, H. Nomura, T. Takahashi, T. Nishimura, and A. Toriumi, "Direct evidence of GeO volatilization from GeO_2/Ge and impact of its suppression on GeO_2/Ge metal-insulator-semiconductor characteristics," in *International Conference on Solid State Devices and Materials*, Tsukuba, JAPAN, 2007, pp. 2349-2353.

[18] CRC Handbook of Physics and Chemistry (2003).

[19] K. Kita and A. Toriumi, "Intrinsic Origin of Electric Dipoles Formed at High-k/SiO_2 Interface," in *IEEE International Electron Devices Meeting*, San Francisco, CA, 2008, pp. 29-32.

[20] G. Mavrou, S. Galata, P. Tsipas, A. Sotiropoulos, Y. Panayiotatos, A. Dimoulas, E. K. Evangelou, J. W. Seo, and C. Dieker, "Electrical properties of La_2O_3 and HfO_2/La_2O_3 gate dielectrics for germanium metal-oxide-semiconductor devices," *Journal of Applied Physics,* vol. 103, 014506, 2008.

[21] C. X. Li and P. T. Lai, "Wide-bandgap high-k Y_2O_3 as passivating interlayer for enhancing the electrical properties and high-field reliability of n-Ge metal-oxide-semiconductor capacitors with high-k HfTiO gate dielectric," *Applied Physics Letters,* vol. 95, 022910, 2009.

[22] K. Martens, C. O. Chui, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, M. M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, "On the correct extraction of interface trap density of MOS devices with high-mobility semiconductor substrates," *IEEE Transactions on Electron Devices,* vol. 55, pp. 547-556, Feb 2008.

[23] K. J. Yang and C. M. Hu, "MOS capacitance measurements for high-leakage thin dielectrics," *IEEE Transactions on Electron Devices,* vol. 46, pp. 1500-1501, Jul 1999.

[24] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. Dekeersmaecker, "A Reliable Approach to Charge-pumping Measurements in MOS-Transistors " *IEEE Transactions on Electron Devices,* vol. 31, pp. 42-53, 1984.

[25] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFETs.1. Effects of substrate impurity concentration," *IEEE Transactions on Electron Devices,* vol. 41, pp. 2357-2362, Dec 1994.

Chapter 4

High-k Gate Stack on Germanium Substrate with Fluorine Incorporation

It is already known that the most critical challenge for building high quality high-k gate stack on Ge substrate is to improve the interface quality. Over the past few years, various pre-gate surface passivation techniques, such as surface nitridation [1-4], Si passivation [5, 6], sulfur passivation [7], metal nitride passivation [8], TaO_xN_y passivation [9, 10] and GeO_2 passivation [11] have been demonstrated on high-k/Ge MOS devices. These surface passivation techniques can either reduce the interface state densities or suppress the Ge out-diffusion into the high-k dielectrics. However, even with the careful surface passivation, the D_{it} of high-k/Ge gate stack is still much higher than that of high-k/Si gate stack. Do we have any technique to further optimize the interface quality, besides the surface passivation?

4.1. Principle and criteria of post gate treatment

Generally speaking, two possible ways exist to improve the HfO_2/Ge gate stack quality as shown in Fig. 4.1. The first way is to implement the careful surface passivation process on Ge substrate before the high-k gate stack formation, which is referred as "pre-gate surface passivation". This has already been discussed in details in previous chapters.

The other way is to explore further passivation process after the high-k gate stack formation, which is referred as "post-gate treatments".

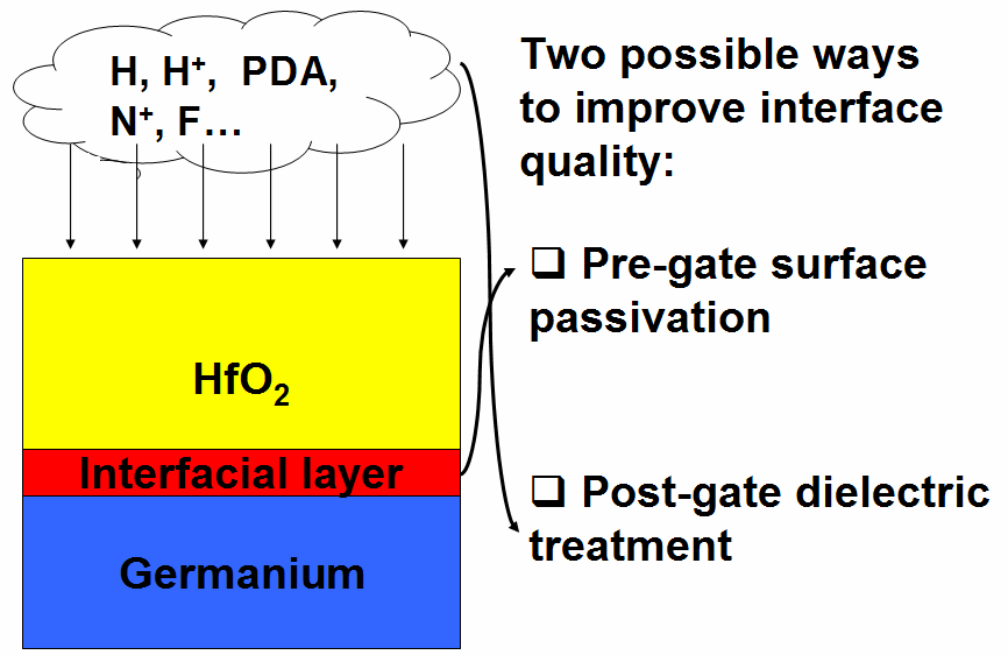

Fig. 4.1. Concept of interface engineering processes: Pre-gate passivation and Post-gate dielectric treatment.

One of the most important post-gate treatments is hydrogen passivation by forming gas annealing (FGA). It is an effective technique to passivate SiO_2/Si interface by forming the Si-H bonds. The D_{it} can be reduced as low as to the order of 10^{10} $cm^{-2}eV^{-1}$. However, for the MOS devices on Ge substrates, some studies have reported that FGA can improve electrical characteristics of Ge MOS capacitors [3], whereas other studies suggested that FGA might not be an effective passivation technique for Ge acceptor states or dangling bonds [12-14]. Atomic H^+ was reported to be more effective to passivate Ge but it is still sensitive to the process conditions (like temperature or metal electrode) [15].

Another important post-gate treatment is post deposition annealing (PDA), which is usually applied for high-k/Si gate stack. A PDA at ~ 700^{o}C can be used to repair high-k bulk defects. However, for the Ge devices, PDA higher than 550^{o}C will usually degrade the Ge gate stack quality because high temperature annealing can lead more GeO_x formation and Ge out diffusion.

Thus, we can see that currently there is no existing good post gate treatment for Ge based devices, left behind a large amount of unpassivated interface traps and bulk defects, which will degrade the device performance and reliability. An alternative post gate treatment is needed for Ge devices and it must satisfy the two important criteria. First, it must be a low temperature process ($\leq$ 500^{o}C) to avoid Ge out diffusion. Second, it must be capable to passivate both interface traps and bulk defects at the same time.

To meet the criteria, we proposed an alternative post gate treatment: fluorine (F) passivation. Firstly, F passivation could be a low temperature process since F can be introduced into the gate stack by either ion implantation or plasma treatment. Secondly, F is expected to be capable to passivate both interface traps and bulk defects. For passivating interface traps, F should be much more effective than H, because F has much higher binding energy with Ge (5.04eV) compared to Ge-H (< 3.34eV) bond [16]. In the case of bulk traps, F is also an excellent passivant, which has been demonstrated in high-k/Si gate stack [17-20]. In this study, F was introduced into the high-k/Ge gate stack by CF_4 plasma treatment as illustrated by Fig. 4.2. The gate stack is treated in an inductively coupled plasma (ICP) chamber with CF_4 gas mixed with a little amount of

O_2, so that unwanted carbon byproduct can react with oxygen and form volatile CO_2 as shown in Fig. 4.2 (a). By subsequent annealing steps, F will diffuse through the gate stack and various passivating processes will take place. It will repair the bulk defects in the HfO_2, especially those oxygen vacancies [21]. It will also passivate the interface traps like Ge dangling bonds. By forming Ge-F bonds, there are also less Ge-O bonds formation as shown in Fig. 4.2 (b).

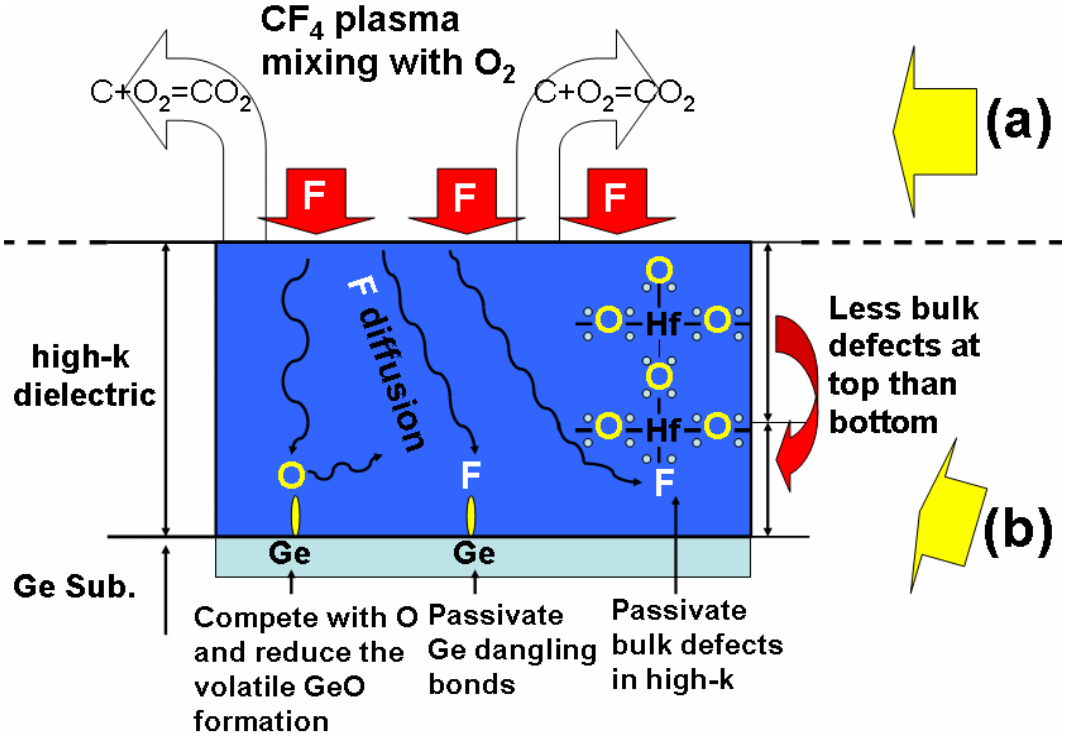

Fig. 4.2. (a) F incorporation to high-k dielectric during CF_4-plasma treatment. (b) Various mechanisms that can take place during the subsequent PDA or S/D activation annealing process for devices with CF_4-plasma treatment.

4.2 Effects of F incorporation without pre-gate surface passivation

4.2.1 Experiment

The starting wafers for the experiments were n-type Ge (100) wafers (Sb doped, resistivity ~0.13-0.14 Ωcm). The native oxide (GeO_x) was removed by a cyclic rinsing between deionized (DI) water and diluted HF. After that, an HfO_2 layer about 9.6 nm

thick was deposited by sputtering of hafnium oxide target. *To study the effects of F alone*, no pre-gate surface passivation other than cyclic rinsing was used before HfO_2 deposition. After the gate dielectric deposition, some samples were treated by CF_4 plasma (rf power of 20 W) in an ICP chamber with a pressure of 100 mTorr at 25^{o}C. The flow rate of CF_4 is 50 sccm. To avoid possible carbon byproduct deposition onto the gate stack, O_2 with a flow rate of 5 sccm was also introduced into the plasma. Post deposition annealing (PDA) was then performed for both CF_4-plasma treated samples and control samples (without CF_4 plasma treatment) at 500°C in a N_2 ambient for 30s. After that, a 150 nm TaN gate electrode was sputtered, and followed by lithography and dry etching. Post metal annealing (PMA) at 450°C, in a N_2 ambient for 1 min was then performed, and finally, a 150 nm Al was deposited on the bottom of Ge substrates for the ohmic contact.

4.2.2 Results and Discussions

To obtain the depth-dependent chemical information, SIMS analysis for both samples with and without CF_4-plasma treatment have been recorded and shown in Fig. 4.3. To avoid using high energy sputtering in SIMS which will cause artifact, samples with thin TaN gate electrode was used for the SIMS analysis. It can be seen that fluorine is introduced into the gate stack after the CF_4-plasma treatment and subsequent annealing (PDA and PMA) steps. The fluorine concentration is peaked at the bottom half of the HfO_2 near the HfO_2/Ge interface. This is because the density of defective bonds at the bottom half of the HfO_2 near HfO_2/Ge interface are much higher due to a sudden structural transition at the interface, and theoretical studies [21, 22] showed that F could passivate the gap state of the oxygen vacancy in HfO_2. Also, F should be a good passivant for

defects at Ge surface because it is the only element that is more electronegative than O and its bond length is similar. Therefore F is expected to segregate near high-k/Ge interface.

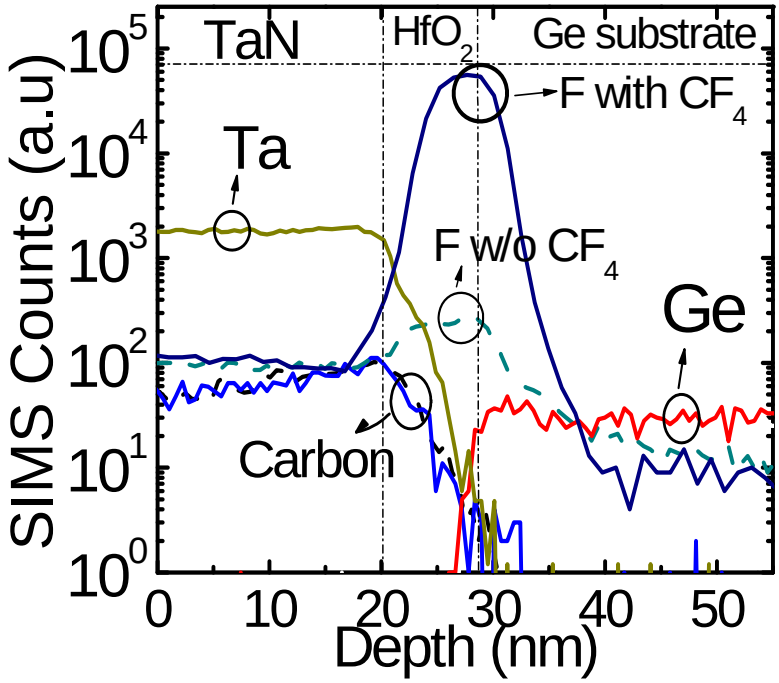

Fig. 4.3. SIMS depth profile for samples with and without CF_4-plasma treatment. F was incorporated in the bulk high-k dielectric and high-k/Ge interface.

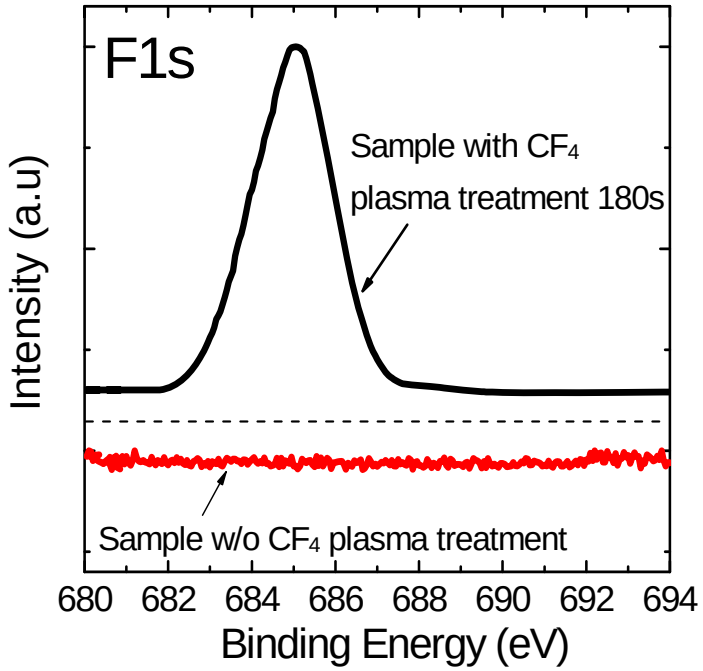

Fig. 4.4. F 1s XPS spectrum for samples with and without CF_4-plasma treatment on HfO_2/Ge gate stack.

The elevated F count at TaN/HfO_2 interface for untreated sample is possibly due to higher F sputter yield in the HfO_2. Further, the carbon (C) distributions for both CF_4 treated and untreated samples are almost the same, indicating that C would not be introduced into gate stack by the CF_4-plasma treatment. F 1s XPS spectra in Fig. 4.4 show that F is incorporated into HfO_2 for samples with CF_4 treatment. The peak located at ~ 685 eV corresponds to the F bonds in bulk HfO_2 [23].

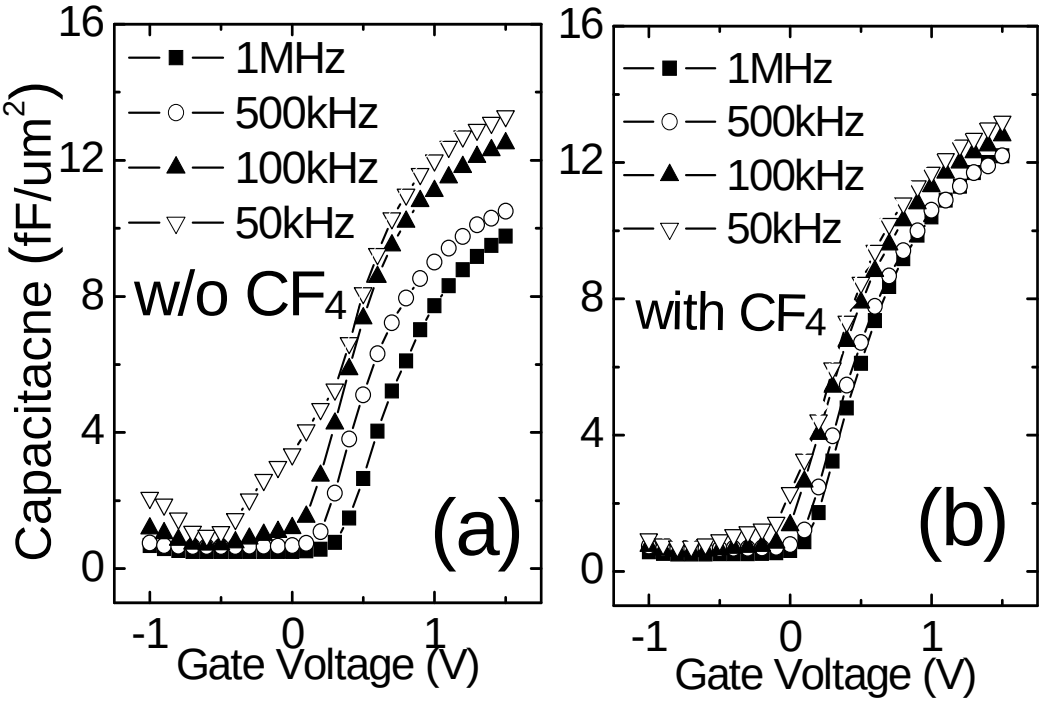

Fig. 4.5. *C-V* frequency dispersion characteristics for samples (a): without CF_4-plasma treatment and (b): with CF_4-plasma treatment.

Fig. 4.5 (a) and (b) show the *C-V* characteristics of MOS capacitors without and with CF_4-plasma treatment, respectively. CF_4 treated samples have smaller frequency dependent flat-band voltage shift (ΔV) (< 0.2 V) between 1 MHz and 50 kHz than samples without CF_4 treatment (~ 0.5 V). The frequency dependent flat-band voltage shift is a direct result of interface states [24]. Particularly for the PMOS capacitors, the V_{fb} shift at

different frequency can be explained by the high D_{it} located in the upper half of band gap, which will be further discussed in Chapter 6. The frequency dispersion in accumulation capacitance is possibly attributed to the series and shunt resistance [25]. Meanwhile, compared to the CF_4 treated samples, the kink in the *C-V* curves for samples without CF_4 plasma treatment is clearly visible at 50 kHz, which has been assigned to the larger density of interface defects [26]. The improved interface quality by CF_4 treatment is attributed to the dangling bonds passivation by forming Ge-F bonds at high-k/Ge interface.

Fig. 4.6 shows the gate leakage characteristics of both samples with and without CF_4-plasma treatment. It is noticed that samples with CF_4-plasma treatment exhibit lower leakage currents at low electrical fields (small positive gate voltage V_g) in the accumulation region. This is due to the reduced trap assisted tunneling, because incorporation of F at high-k/Ge interface can effectively reduce the interface traps (D_{it}), also, F incorporation into HfO_2 can reduce bulk traps of high-k dielectric by forming Hf-F bonds, which has been reported in other studies as well. When the electrical field becomes higher ($V_g > 3V$), the leakage currents of both samples become almost the same. This is because when gate voltage increases, Fowler-Nordheim tunneling would become dominant; the gate leakage is then mainly depending on the dielectric thickness and the conduction band offset. In addition, a two-stage breakdown characteristic is observed for samples without CF_4-plasma treatment, this may be due to the poor quality of interfacial layer at high-k/Ge interface. On the other hand, for the samples with CF_4-plasma

treatment, single stage breakdown is observed and the breakdown voltage is slightly higher.

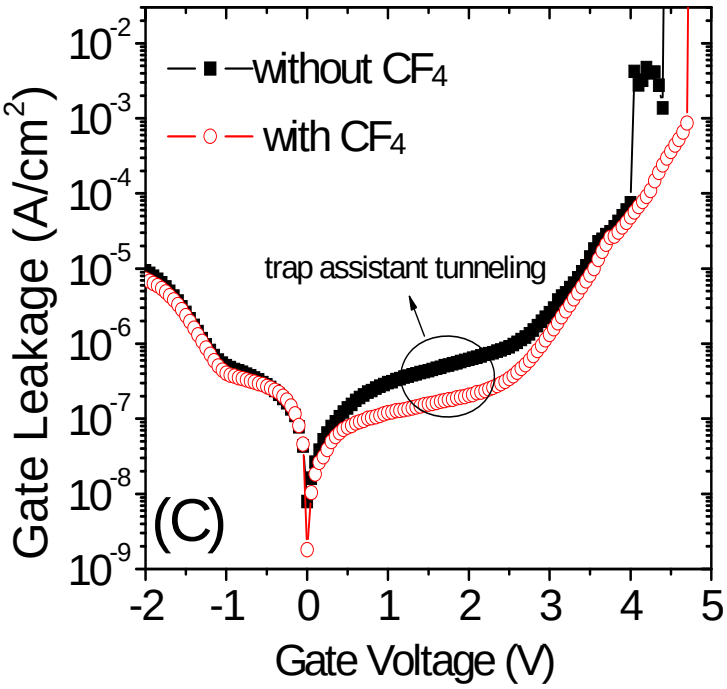

Fig. 4.6. I_g-V_g characteristics for samples with and without CF_4-plasma treatment.

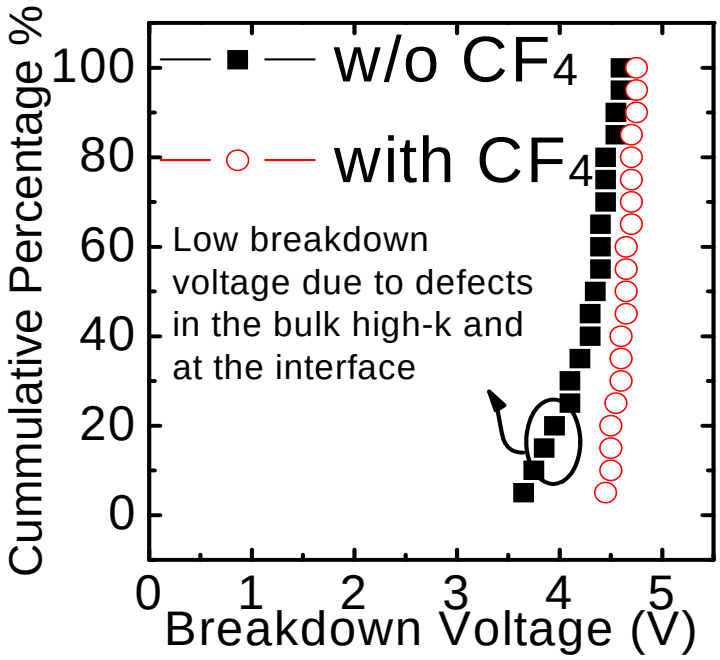

Fig. 4.7. Cumulative probability of breakdown voltages for samples with and without CF_4-plasma treatment.

To further study the CF_4-plasma treatment on the breakdown characteristics, cumulative probability of hard breakdown voltages is potted in Fig. 4.7. It is found that samples with CF_4-plasma treatment have more uniform breakdown distributions and higher breakdown voltages. Breakdown at low voltage (<4V) is observed for samples without CF_4-plasma treatment, which is due to high densities of interface and bulk traps that could lead a leakage path through the gate dielectric at lower gate voltage.

4.2.3 Summary

F passivation of high-k/Ge gate stack has been proposed and demonstrated for the first time. Ge MOS capacitors using HfO_2 gate dielectric and TaN gate electrode were fabricated without any pre-gate surface passivation process. SIMS and XPS results show that F is successfully incorporated into HfO_2 gate dielectric and high-k/Ge interface through a post gate CF_4 plasma treatment process without any carbon byproduct deposition. Compared to the control samples, samples with F incorporation exhibit much better *C-V* characteristics, which is due to lower interface state density. This is attributed to F passivation at high-k/Ge interface by forming Ge-F bonds. In addition, samples with F incorporation also show smaller gate leakage currents at low electrical fields in the accumulation region and have improved breakdown characteristics. This is because F incorporation can also effectively reduce bulk traps in the high-k dielectric by forming Hf-F bonds.

4.3 Effects of F incorporation with Si pre-gate surface passivation

F incorporation has been demonstrated to be useful for HfO_2 gated Ge MOS device without any pre-gate surface passivation. However, the interface quality is still far from satisfactory because the GeO can easily formed at HfO_2/Ge interface if no passivation layer is applied. To further improve the interface quality, pre-gate surface passivation is necessary. Therefore, it is very important to know whether this post gate F treatment process is compatible with pre-gate surface passivation. Among various pre-gate surface passivation techniques, Si passivation is the most promising one. High mobility pMOSFETs and transistors with small gate length have been achieved with Si passivation [6, 27]. Thus, we choose to investigate the effects of F passivation for HfO_2 gate Ge MOS devices with Si surface passivation.

4.3.1 Experiment

The starting wafers were n-type Ge (100) wafers. After cyclic rinsing between deionized (DI) water and diluted HF, Si surface passivation (SP) was carried out for some Ge substrates by annealing the samples in SiH_4 ambient with N_2 as the carrier gas at 5 torr, 450^{o}C. After that, an HfO_2 layer of about 6.5 nm was deposited to keep the EOT the same with the previous samples. An optimized CF_4 plasma (rf power of 10 W, flow rate of CF_4 100 sccm, flow rate of O_2 10 sccm) treatment for different duration in an ICP chamber with pressure of 100 mTorr at 25^{o}C was carried out for some samples. The remaining processes were the same as described in section 4.2.1 for Ge MOS capacitors. Ge pMOSFETs were also fabricated by an additional boron implantation (1E15 cm^{-2}, 15 keV).

4.3.2 Results and discussions

After SP and CF_4 treatment, almost ideal *C-V* shape is achieved as shown in Fig. 4.8. Fig. 4.9(a) and (b) compare the *C-V* characteristics for SP samples without CF_4 treatment and with CF_4 treatment for 3 min, respectively. Samples with SP show smaller ΔV as compared to samples without SP (Fig. 4.5), and ΔV further decreases with increasing CF_4 treatment time as shown in Fig. 4.10 and finally, almost frequency dispersion free *C-V* characteristics is achieved after 3 min CF_4 treatment. The elimination of such behavior suggests that a good interface quality is achieved by both CF_4 treatment and thin Si passivation layer.

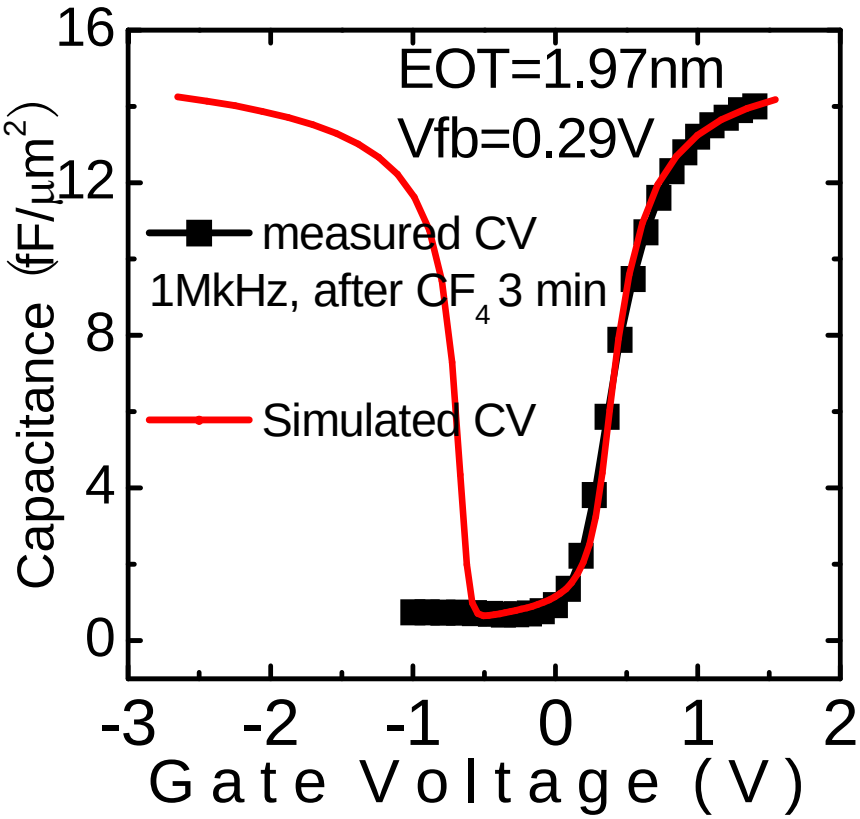

Fig. 4.8. Samples with both Si passivation and CF_4-plasma treatment show excellent high frequency *C-V* characteristics.

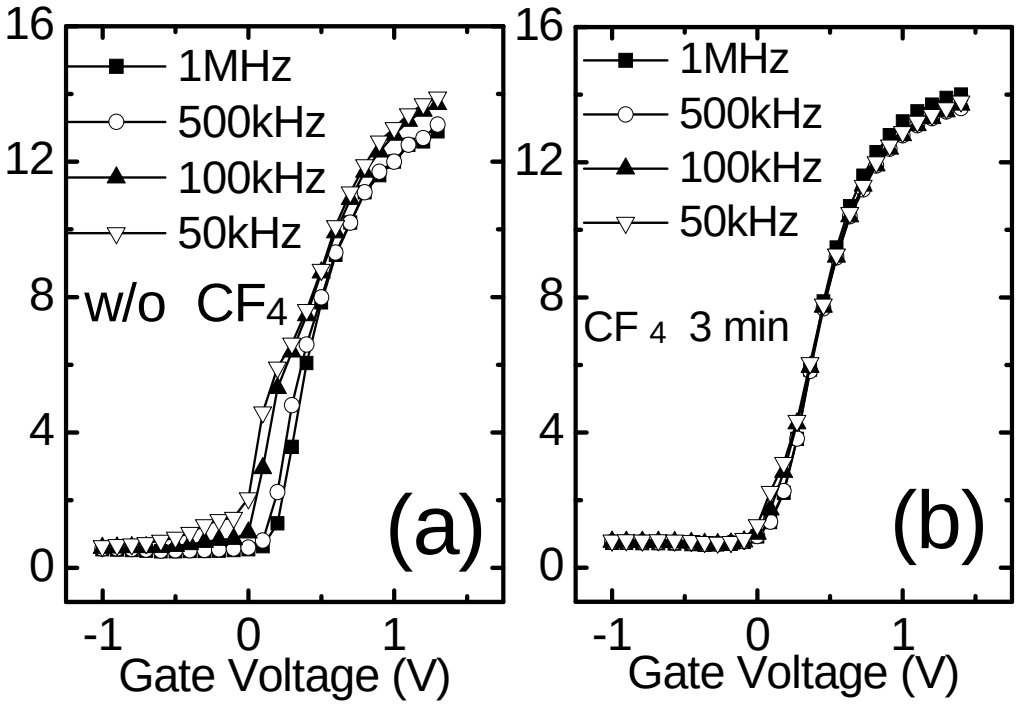

Fig. 4.9. *C-V* frequency dispersion characteristics for SP samples (a) without CF_4-plasma treatment and (b) with CF_4-plasma treatment for 3 min. Both frequency-dependent ΔV_{fb} and stretch-out disappear for CF_4 treated samples.

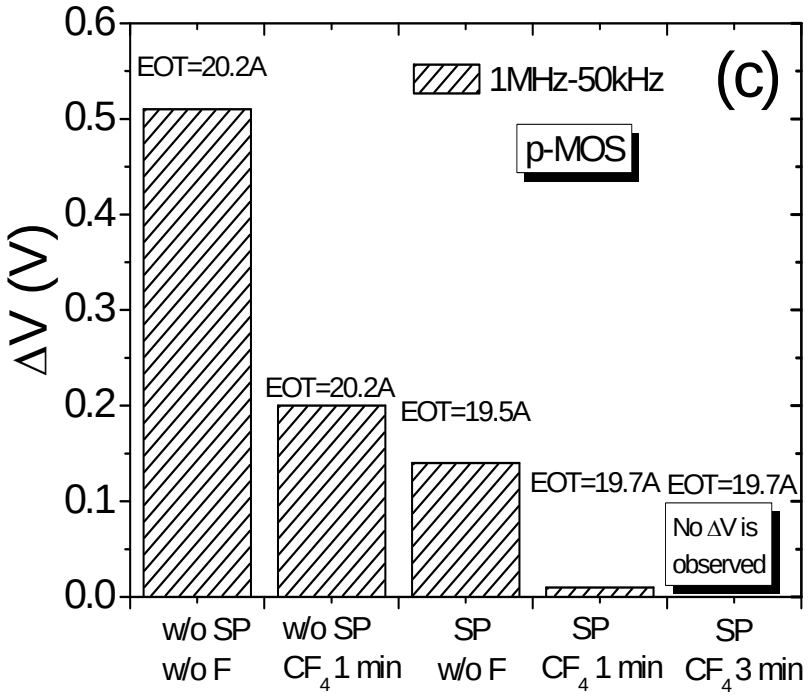

Fig. 4.10. Comparison of frequency dependent flat band voltage shift for samples with different pre-gate or post-gate treatment conditions.

Interface state density D_{it} was measured using the frequency-dependent conductance method. A series of ac conductance measurements was performed as a function of frequency. Fig. 4.11 shows the typical measured frequency dependencies of G_p/ω for various gate voltages for samples with SP. It can be seen that the peaks of the G_p/ω plot for each gate voltages are clearly distinguished and the amplitude of the peak is a strong function of gate voltages. The value of D_{it} was extracted according to $D_{it} = 2.5 (G_p/\omega)|_{max}/qA$, where $(G_p/\omega)|_{max}$ is the peak loss value, q is the electronic charge and A is the area. The extracted D_{it} was plotted as a function of energy relative to the valence band edge in Fig. 4.12. For SP samples without F passivation, the minimum D_{it} is 2.76×10^{12} $cm^{-2}eV^{-1}$, whereas for SP samples with 3 min treatment, the minimum D_{it} is reduced to 4.85×10^{11} $cm^{-2}eV^{-1}$. This suggests that the F post gate treatment is very effective to passivate the defect states at high-k/Ge interface. In addition, a significant reduction in D_{it} of upper half of the energy band is noticed after CF_4-plasma treatment for 1 min. This trend is consistent with observation that frequency dependent flat-band voltage dispersion (ΔV) is much less for CF_4-plasma treated samples.

Table 4.1 summarize the D_{it}, EOT, hysteresis and gate leakage current for the all kinds of MOS capacitors mentioned in this chapter. The EOT values for all the samples are almost the same. F incorporation will not change the EOT value significantly. Samples with SP shows much smaller D_{it} and hysteresis than samples without SP, indicating that surface passivation is still very important. For both samples without SP and with SP, D_{it}, hysteresis and leakage current density are greatly reduced with F passivation, suggesting that post-gate CF_4 treatment is an effective technique to improve

both interface and bulk quality and it is also compatible with pre-gate surface passivation process.

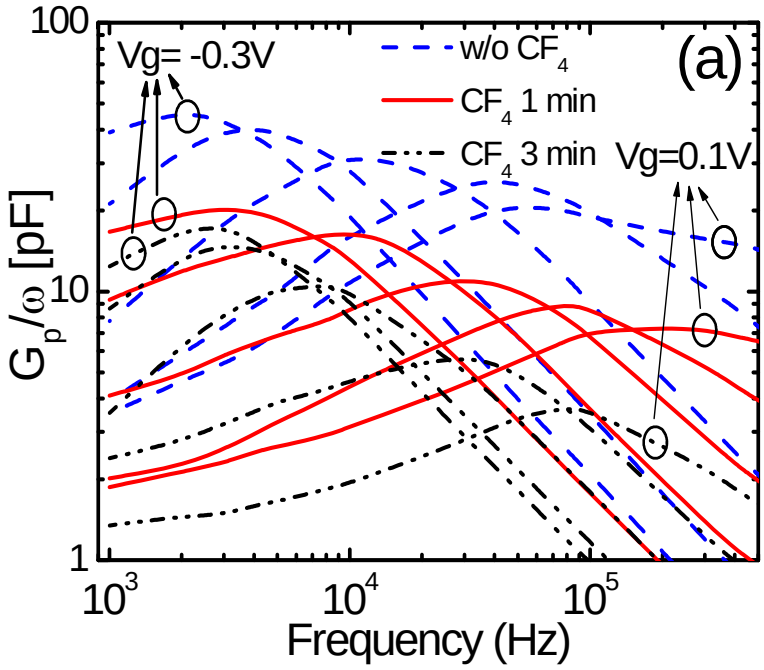

Fig. 4.11. Frequency dependent conductance G_p/ω for a series of gate voltages for SP samples w/o F treatment, with F treatment for 1 min, and with F treatment for min, respectively.

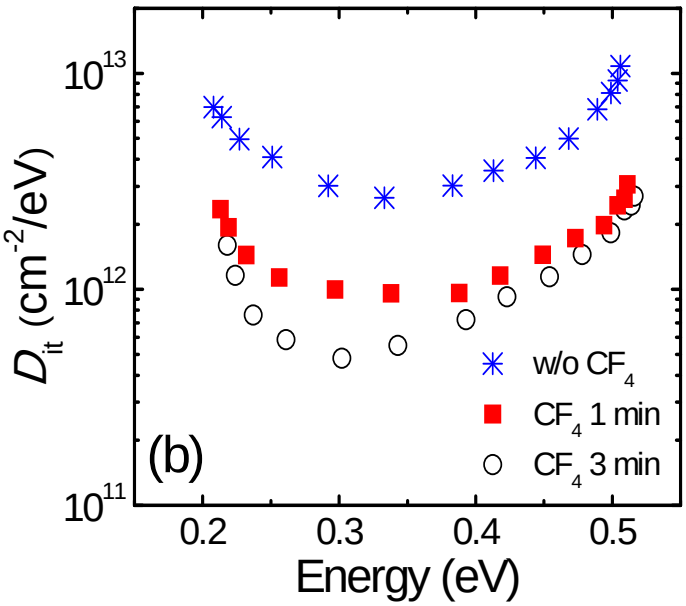

Fig. 4.12. Plot of D_{it} vs energy relative to the valence band edge for samples w/o CF_4 treatment, with CF_4 treatment for 1- and 3- min, respectively. Interface quality is greatly improved after CF_4-plasma treatment.

Table 4.1. Comparison of D_{it}, EOT, hysteresis and gate leakage current for Ge capacitors with different pre-gate or post-gate treatment conditions.

Samples	CF_4-plasma treatment duration (s)	D_{it} ($eV^{-1}cm^{-2}$)	EOT (Å)	Hysteresis (mV)	J_g at V_g=1V (Acm^{-2})
w/o Si passivation HfO_2 9.6 nm	0	6.09×10^{12}	20.2	450	3.01×10^{-7}
w/o Si passivation HfO_2 9.6 nm	60	2.61×10^{12}	20.2	220	1.21×10^{-7}
with Si passivation HfO_2 6.5 nm	0	2.76×10^{12}	19.5	50	1.72×10^{-7}
with Si passivation HfO_2 6.5 nm	60	9.57×10^{11}	19.7	negligible	1.38×10^{-7}
with Si passivation HfO_2 6.5 nm	180	4.85×10^{11}	19.7	negligible	1.36×10^{-7}

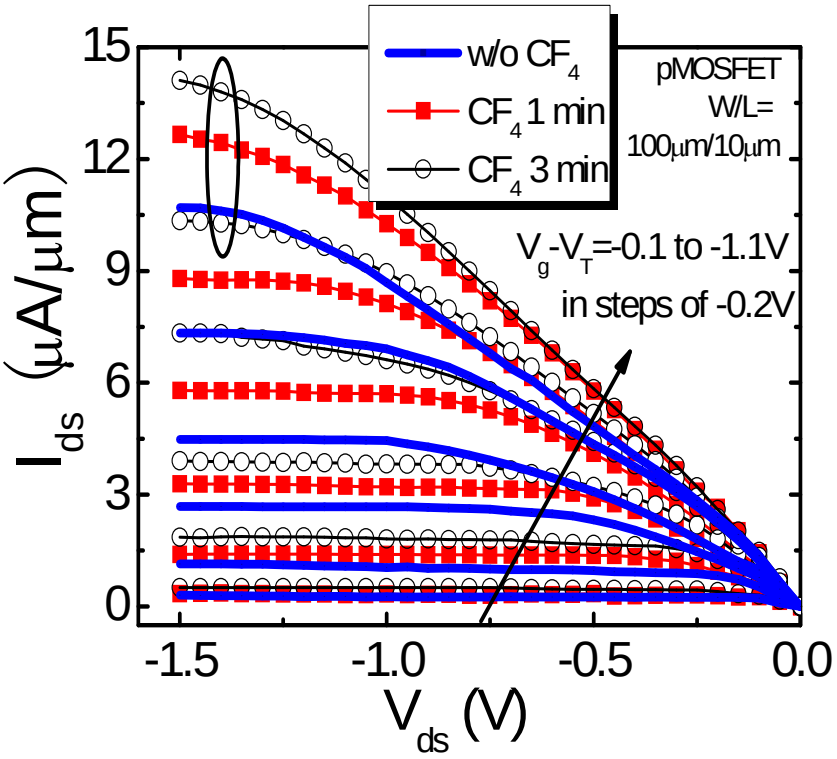

Fig. 4.13. Output characteristics for Ge pMOSFETs with Si passivation and CF_4-plasma treatment for different duration. Enhanced drive currents were achieved after CF_4 plasma-treatment.

I_d-V_d characteristics show that SP devices with CF_4 plasma treatment have higher drive current as shown in Fig. 4.13. Effective hole mobility was extracted using split *C-V* method and shown in Fig. 4.14. Compared to SP devices without CF_4 treatment, peak hole mobility is enhanced by 15.6% and 30%, high field mobility is enhanced by 13.4% and 21.9% for 1- and 3- min CF_4 treatment, respectively. A high peak hole mobility of 293 $cm^2/V{\cdot}s$ at effective vertical field of 0.19 MV/cm is obtained for 3 min treatment, without correction of parasitic resistance, and is about 376 $cm^2/V{\cdot}s$ with the correction. This is one of the highest reported record mobility values [6, 28, 29] for unstrained Ge pMOSFETs.

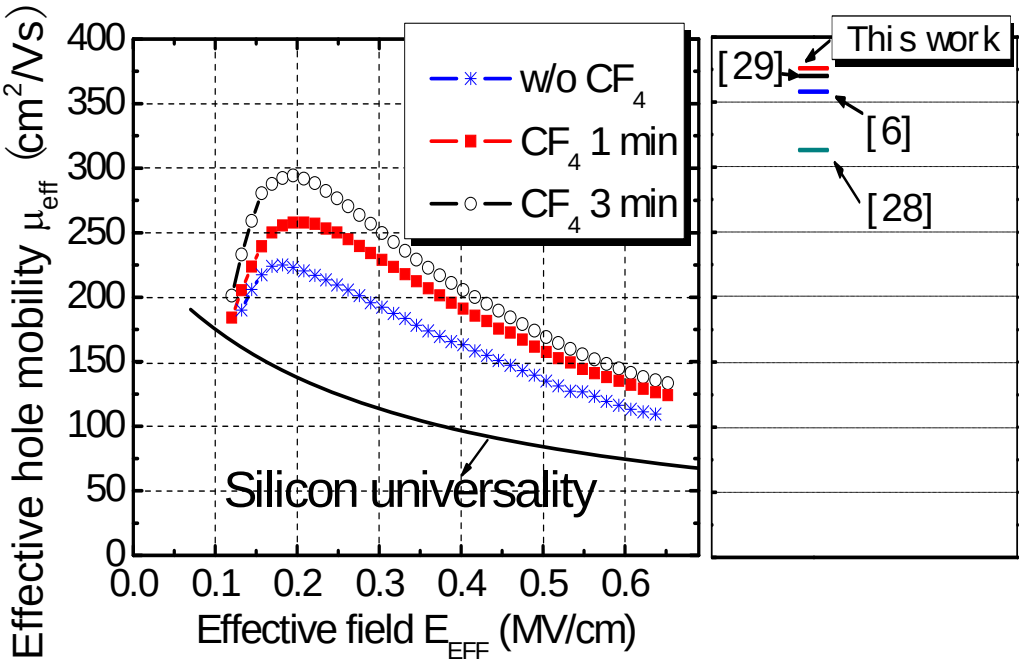

Fig. 4.14. *Left*: effective hole mobility in Ge pMOSFETs versus effective field for silicon passivated devices with different CF_4 treatment conditions without correction. *Right*: peak μ_{eff} after correction together with other reported data [6, 28, 29].

4.4 Conclusions

Pre-gate surface passivation techniques have been extensively studied in the past few years. By inserting an interfacial layer between high-k and Ge, interface quality is

greatly improved. However, compared to SiO_2/Si interface, this is still far from satifactory. To further optimize the interface quality, an additional post gate treatment process must be introduced. FGA and PDA are not effective for Ge based devices. Thus we proposed and demonstrated a low temperature CF_4 plasma treatment that introduced F into the high-k/Ge gate stack. By forming the Ge-F and Hf-F bonds, the D_{it} and high-k bulk defects are significantly reduced. Post gate F treatment is also compatible with pre-gate surface passivation. We demonstrated that an additional CF_4 plasma treatment process for samples with Si pre-gate passivation could further reduce the D_{it} and increase the mobility.

References :

[1] J. J. H. Chen, N. A. Bojarczuk, H. L. Shang, M. Copel, J. B. Hannon, J. Karasinski, E. Preisler, S. K. Banerjee, and S. Guha, "Ultrathin Al_2O_3 and HfO_2 gate dielectrics on surface-nitrided Ge," *IEEE Transactions on Electron Devices,* vol. 51, pp. 1441-1447, Sep 2004.

[2] C. O. Chui, H. Kim, P. C. McIntyre, and K. C. Saraswat, "Atomic layer deposition of high-k dielectric for germanium MOS applications-substrate surface preparation," *IEEE Electron Device Letters,* vol. 25, pp. 274-276, May 2004.

[3] T. Maeda, M. Nishizawa, Y. Morita, and S. Takagi, "Role of germanium nitride interfacial layers in HfO_2/germanium nitride/germanium metal-insulator-semiconductor structures," *Applied Physics Letters,* vol. 90, 072911, Feb 2007.

[4] N. Wu, Q. C. Zhang, C. X. Zhu, C. C. Yeo, S. J. Whang, D. S. H. Chan, M. F. Li, B. J. Cho, A. Chin, D. L. Kwong, A. Y. Du, C. H. Tung, and N. Balasubramanian, "Effect of surface NH_3 anneal on the physical and electrical properties of HfO_2 films on Ge substrate," *Applied Physics Letters,* vol. 84, pp. 3741-3743, May 2004.

[5] N. Wu, Q. C. Zhang, C. X. Zhu, D. S. H. Chan, M. F. Li, N. Balasubramanian, A. Chin, and D. L. Kwong, "Alternative surface passivation on germanium for metal-oxide-semiconductor applications with high-k gate dielectric," *Applied Physics Letters,* vol. 85, pp. 4127-4129, Nov 2004.

[6] P. Zimmerman, G. Nicholas, B. De Jaeger, B. Kaczer, A. Stesmans, L. A. Ragnarsson, D. P. Brunco, F. E. Leys, M. Caymax, G. Winderickx, K. Opsomer, M. Meuris, and M. M. Heyns, "High performance Ge pMOS devices using a Si-compatible process flow," in *IEEE International Electron Devices Meeting*, San Francisco, CA, 2006, pp. 390-393.

[7] M. M. Frank, S. J. Koester, M. Copel, J. A. Ott, V. K. Paruchuri, H. L. Shang, and R. Loesing, "Hafnium oxide gate dielectrics on sulfur-passivated germanium," *Applied Physics Letters,* vol. 89, 112905, Sep 2006.

[8] K. H. Kim, R. G. Gordon, A. Ritenour, and D. A. Antoniadis, "Atomic layer deposition of insulating nitride interfacial layers for germanium metal oxide semiconductor field effect transistors with high-k oxide/tungsten nitride gate stacks," *Applied Physics Letters,* vol. 90, 212104, May 2007.

[9] T. Sugawara, Y. Oshima, R. Sreenivasan, and P. C. McIntyre, "Electrical properties of germanium/metal-oxide gate stacks with atomic layer deposition grown hafnium-dioxide and plasma-synthesized interface layers," *Applied Physics Letters,* vol. 90, 112912, Mar 2007.

[10] X. F. Zhang, J. P. Xu, C. X. Li, P. T. Lai, C. L. Chan, and J. G. Guan, "Improved electrical properties of Ge metal-oxide-semiconductor capacitor with HfTa-based gate dielectric by using TaO_xN_y interlayer," *Applied Physics Letters,* vol. 92, 262902, Jun 2008.

[11] A. Delabie, F. Bellenger, M. Houssa, T. Conard, S. Van Elshocht, M. Caymax, M. Heyns, and M. Meuris, "Effective electrical passivation of Ge(100) for high-k gate dielectric layers using germanium oxide," *Applied Physics Letters,* vol. 91, 082904, Aug 2007.

[12] V. V. Afanas'ev, Y. G. Fedorenko, and A. Stesmans, "Interface traps and dangling-bond defects in (100)Ge/HfO_2," *Applied Physics Letters,* vol. 87, 032107, Jul 2005.

[13] C. O. Chui, H. Kim, D. Chi, P. C. McIntyre, and K. C. Saraswat, "Nanoscale germanium MOS dielectrics - Part II: High-k gate dielectrics," *IEEE Transactions on Electron Devices,* vol. 53, pp. 1509-1516, Jul 2006.

[14] J. R. Weber, A. Janotti, P. Rinke, and C. G. V. de Walle, "Dangling-bond defects and hydrogen passivation in germanium," *Applied Physics Letters,* vol. 91, 142101, Oct 2007.

[15] H. Matsubara, T. Sasada, M. Takenaka, and S. Takagi, "Evidence of low interface trap density in GeO_2/Ge metal-oxide-semiconductor structures fabricated by thermal oxidation," *Applied Physics Letters,* vol. 93, 032104, Jul 2008.

[16] CRC Handbook of Physics and Chemistry (2003).

[17] C. S. Lai, W. C. Wu, J. C. Wang, and T. Chao, "Characterization of CF_4-plasma fluorinated HfO_2 gate dielectrics with TaN metal gate," *Applied Physics Letters,* vol. 86, 222905, May 2005.

[18] K. I. Seo, R. Sreenivasan, P. C. McIntyre, and K. C. Saraswat, "Improvement in high-k (HfO_2/SiO_2) reliability by incorporation of fluorine," in *IEEE International Electron Devices Meeting*, Washington, DC, 2005, pp. 429-432.

[19] H. H. Tseng, P. J. Tobin, E. A. Hebert, S. Kalpat, M. E. Ramon, L. Fonseca, Z. X. Jiang, J. K. Schaeffer, R. I. Hegde, D. H. Triyoso, D. C. Gilmer, W. J. Taylor, C. C. Capasso, O. Adetutu, D. Sing, J. Conner, E. Luckowski, B. W. Chan, A. Haggag, S. Backer, R. Noble, M. Jahanbani, Y. H. Chiu, and B. E. White, "Defect passivation with fluorine in a Ta_xC_y/High-k gate stack for enhanced device threshold voltage stability and performance," in *IEEE International Electron Devices Meeting*, Washington, DC, 2005, pp. 713-716.

[20] W. C. Wu, C. S. Lai, S. C. Lee, M. W. Ma, T. S. Chao, J. C. Wang, C. W. Hsu, P. C. Chou, J. H. Chen, K. H. Kao, W. C. Lo, T. Y. Lu, L. L. Tay, and N. Rowell, "Fluorinated HfO_2 Gate Dielectrics Engineering for CMOS by pre- and post-CF_4 Plasma Passivation," in *IEEE International Electron Devices Meeting*, San Francisco, CA, 2008, pp. 405-408.

[21] K. Tse and J. Robertson, "Defect passivation in HfO_2 gate oxide by fluorine," *Applied Physics Letters,* vol. 89, 142914, Oct 2006.

[22] Q. Q. Sun, W. Chen, S. J. Ding, M. Xu, H. L. Lu, H. C. Lindh-Rengifo, D. W. Zhang, and L. K. Wang, "Comparative study of passivation mechanism of oxygen vacancy with fluorine in HfO_2 and $HfSiO_4$," *Applied Physics Letters,* vol. 90, 142904, Apr 2007.

[23] K. I. Seo, R. Sreenivasan, P. C. McIntyre, and K. C. Saraswat, "Improvement in high-k (HfO_2/SiO_2) reliability by incorporation of fluorine," *IEEE Electron Device Letters,* vol. 27, pp. 821-823, Oct 2006.

[24] J. Reed, Z. Fan, G. B. Gao, A. Botchkarev, and H. Morkoc, "GaAs metal-insulator-semiconductor capacitors and high transconductance metal-insulator-semiconductor field-effect transistors," *Applied Physics Letters,* vol. 64, pp. 2706-2708, May 1994.

[25] K. J. Yang and C. M. Hu, "MOS capacitance measurements for high-leakage thin dielectrics," *IEEE Transactions on Electron Devices,* vol. 46, pp. 1500-1501, Jul 1999.

[26] M. Houssa, T. Conard, F. Bellenger, G. Mavrou, Y. Panayiotatos, A. Sotiropoulos, A. Dimoulas, M. Meuris, M. Caymax, and M. M. Heyns, "Electrical properties of atomic-beam deposited $GeO_{1-x}N_x/HfO_2$ gate stacks on Ge," *Journal of the Electrochemical Society,* vol. 153, pp. G1112-G1116, 2006.

[27] J. Mitard, B. De Jaeger, F. E. Leys, G. Hellings, K. Martens, G. Eneman, D. P. Brunco, R. Loo, J. C. Lin, D. Shamiryan, T. Vandeweyer, G. Winderickx, E. Vrancken, C. H. Yu, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, and M. M. Heyns, "Record I_{ON}/I_{OFF} performance for 65nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability," in *IEEE International Electron Devices Meeting*, San Francisco, CA, 2008, pp. 873-876.

[28] C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "A Sub-400 degrees C germanium MOSFET technology with high-k dielectric and metal gate," in *IEEE International Electron Devices Meeting*, San Francisco, Ca, 2002, pp. 437-440.

[29] T. Takahashi, T. Nishimura, L. Chen, S. Sakata, K. Kita, and A. Toriumi, "Proof of Ge-interfacing concepts for metal/high-k/Ge CMOS Ge-intimate material selection and interface conscious process flow," in *IEEE International Electron Devices Meeting*, Washington, DC, 2007, pp. 697-700.

Chapter 5

Interface Engineered High Mobility High-k/Ge pMOSFETs with 1 nm Equivalent Oxide Thickness

Development of high-k/Ge gate stack with high quality interface and small equivalent oxide thickness (EOT) is essential for Ge to be used as an alternative high mobility channel material for future technology nodes. Over the past few years, various pre-gate surface passivation techniques have been developed to improve high-k/Ge interface quality and recently, GeO_2 as a native oxide layer, formed by either thermal growth [1-3], rf-sputtering [4, 5], or ozone oxidation [6, 7] is of particularly interest as it may be the most natural material to passivate Ge surface. Unlike Ge monoxide (GeO), GeO_2 is not volatile, so a high quality GeO_2 may act as a perfect interfacial layer. Interface trap density as low as ~ 3×10^{11} $cm^{-2}eV^{-1}$ and 7.5 $\times10^{10}$ $cm^{-2}eV^{-1}$ have been reported for MOS capacitors with $HfO_2/GeO_2/Ge$ [2, 6] and GeO_2/Ge [3] gate stack, respectively. A high peak hole mobility of 367 $cm^2/$ V·s has been demonstrated for Ge pMOSFETs with $FUSI/GeO_2/Ge$ gate stack [5]. However, there is still no reports on high-k gated Ge MOSFETs with GeO_2 passivation layer.

Besides pre-gate surface passivation, another alternative approach to further improve the high-k/Ge gate stack quality is to adopt appropriate post gate dielectric (post-gate) treatment processes. In the last chapter, we have already demonstrated that post gate F treatment can effectively reduce both interface states and high-k bulk traps. In this

study, firstly, we apply this technique to GeO_2 passivated samples with HfO_2 gate dielectrics. In addition to F incorporation, the effects of forming gas annealing (FGA) are also investigated. Secondly, high mobility Ge pMOSFETs with 1 nm EOT are successfully demonstrated with GeO_2 passivation layer and optimized post gate treatment processes. Finally, variable rise and fall time charge pumping procedure, as described in [8], is applied to investigate the interface properties for Ge MOSFETs.

5.1 Effects of F incorporation and FGA on TaN/HfO_2/GeO_2/Ge MOS Capacitors

5.1.1 Experiments

Firstly, we employ the surface GeO_2 passivation to HfO_2 gated Ge MOS capacitors and investigate the impacts of post-gate treatment including F incorporation and FGA. The starting wafers were n-type Ge wafers (Sb doped ~ 1.5 to 2×10^{16} cm^{-3}, R= 0.13-0.14 Ωcm). The native oxide was removed by a cyclic rinsing between deionized water and HF dilution (1: 50). A thin germanium oxide layer about 2 nm was then thermally grown on germanium substrates at 400°C. Higher temperature oxidation was not used to avoid possible decomposition of GeO_2 and desorption of GeO (GeO desorbs at 420°C) [9], and the oxidation temperature of 400°C was chosen because it has been reported that Ge oxidation at 400°C results in lowest D_{it} [6]. To minimize the air exposure to the GeO_2, the samples were then immediately transferred to the ALD load-lock chamber. A HfO_2 layer of 4.5 nm was deposited at 300°C in the ALD reactor using Hfi_4 (TEMAHf) precursor and H_2O. After the gate dielectric deposition, three different post-gate treatments schemes have been made as described in Fig, 5.1 (b) (c) and (d). The CF_4 plasma treatment condition has been described in last chapter. FGA condition was 350°C for 1 hour in H_2 + N_2 ambient. All samples had been processed with post

deposition annealing (PDA) at 500°C in N_2 ambient for 30 sec. A TaN layer of 150 nm thick was sputtered as the gate electrode and an Al layer of 100 nm was then deposited on the bottom of Ge substrates for ohmic contact.

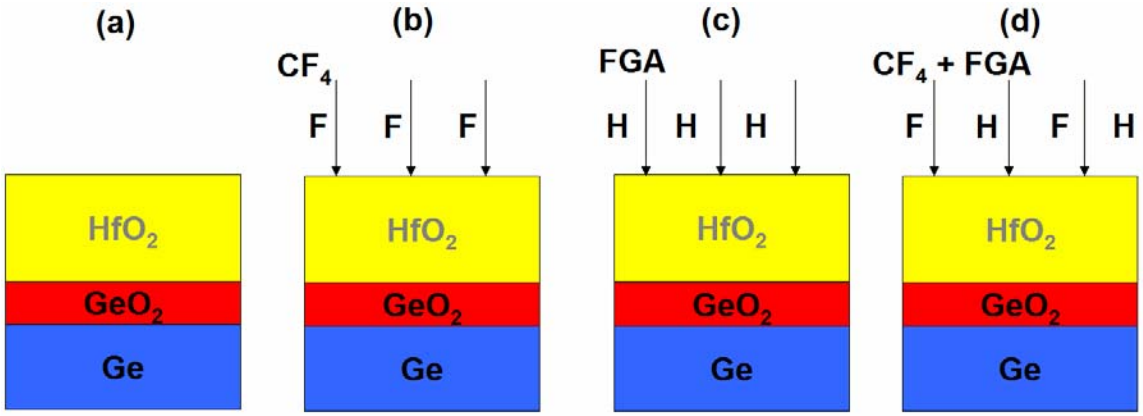

Fig. 5.1. Splits for post gate treatments scheme for TaN/HfO_2/GeO_2/Ge MOS capacitors.

5.1.2 Results and Discussions

After growing a thin germanium oxide, some samples were immediately sent for XPS analysis (within 5 min) to avoid the moisture effect on germanium oxide. Fig. 5.2 shows the angle-resolved XPS Ge 3d spectra. The difference between the binding energy of germanium oxide and substrate peaks is 3.3 eV for both 30° and 90° takeoff angles, indicating Ge^{4+} is present at both GeO_2 surface and near the GeO_2/Ge interface [10]. No significant components of germanium suboxides were detected, suggesting that our GeO_2 prepared by thermal growth at 400°C is with good quality. Fig. 5.3 confirms the F incorporation into TaN/HfO_2/GeO_2/Ge gate stack by CF_4 plasma treatment. The oxygen peaks for both samples with and without CF_4 plasma treatment are almost the same, indicating that the effects of CF_4 plasma treatment are mainly due to the F incorporation.

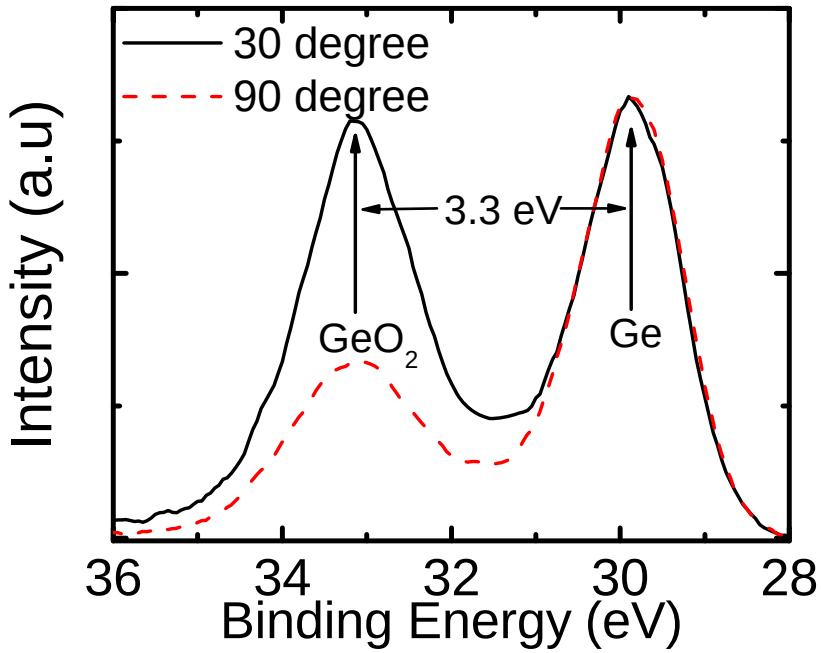

Fig. 5.2. Angle resolved XPS Ge 3d spectra for germanium samples after the thermal oxidation at 400°C. The thickness of GeO_2 is about 2 nm.

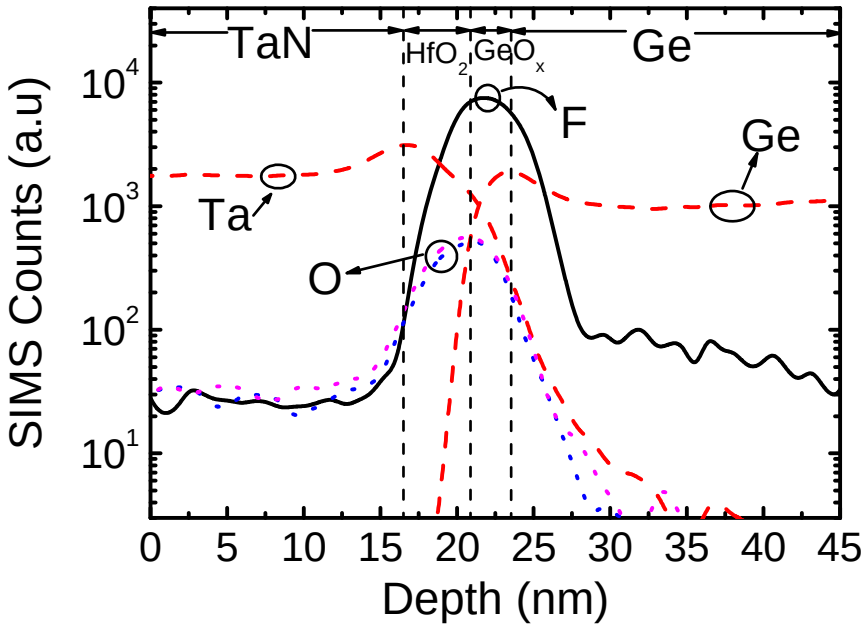

Fig. 5.3. SIMS profiles for $TaN/HfO_2/GeO_x/Ge$ gate stack after PDA and FGA. The oxygen profiles are taken for both samples with and without CF_4 plasma treatment process. Other curves are taken from CF_4 treated samples.

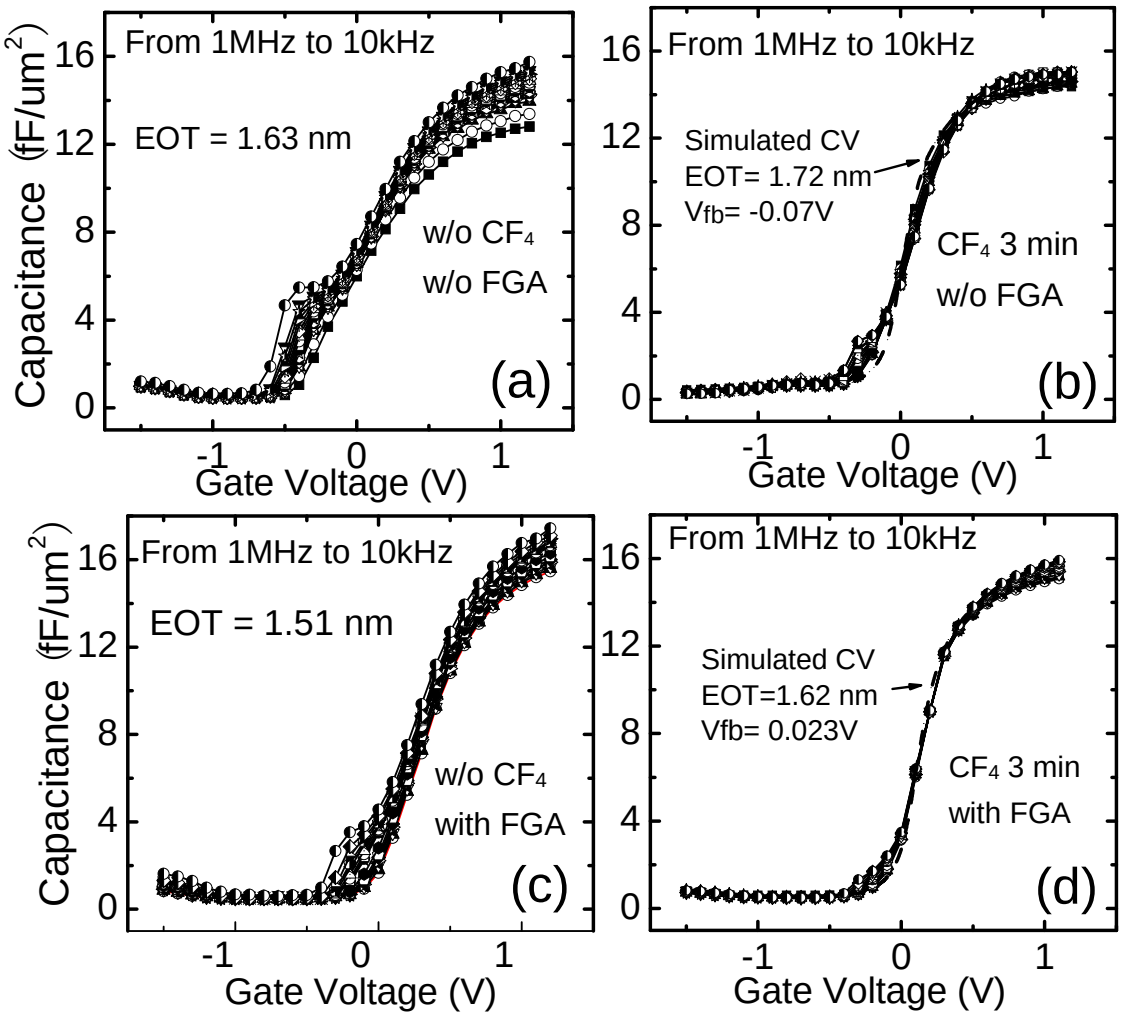

Fig. 5.4. Capacitance-voltage characteristics of TaN/HfO_2/GeO_x/Ge gate stacks (~ 2 nm GeO_2 and 4.5 nm HfO_2) measured at 1Mhz, 900kHz, 800kHz,…, 200kHz, 100kHz, 90kHz, 80kHz,…, 20kHz and 10kHz (a) with neither CF_4 plasma treatment nor FGA; (b) with CF_4 plasma treatment for 3 min but without FGA; (c) without CF_4 plasma treatment but with FGA; (d) with both CF_4 plasma treatment and FGA.

Fig. 5.4 shows the *C-V* frequency dispersion characteristics of TaN/HfO_2/GeO_2/Ge MOS capacitors with different post-gate treatments (CF_4 plasma treatment or FGA). For the samples with neither CF_4 plasma treatment nor FGA (split a), besides the observation of large kinks and significant *C-V* stretch-out, which is attributed to high density of interface traps near midgap (~3 $\times 10^{12}$ $eV^{-1}cm^{-2}$ estimated from

conductance method), a significant frequency dependent flat band voltage shift (ΔV) ~ 100 mV is also present between 1MHz and 10 kHz *C-V* curves, which is the direct result of interface states [11]. Particularly for the PMOS capacitors, ΔV is the indication of weak Fermi-level pinning in the upper half of Ge bandgap [12, 13]. In other words, this indicates a high density of interface traps locates in the upper half of the Ge bandgap. For the samples with only CF_4 treatment for 3 min (split b) [Fig. 5.1(b)], the size of the kinks becomes much smaller and no evidence of ΔV is observed. Also, *C-V* curves with various frequencies exhibit much less stretch-out behaviors. This is attributed to reduced interface states through the F passivation for both interface states at midgap and upper half of the bandgap.

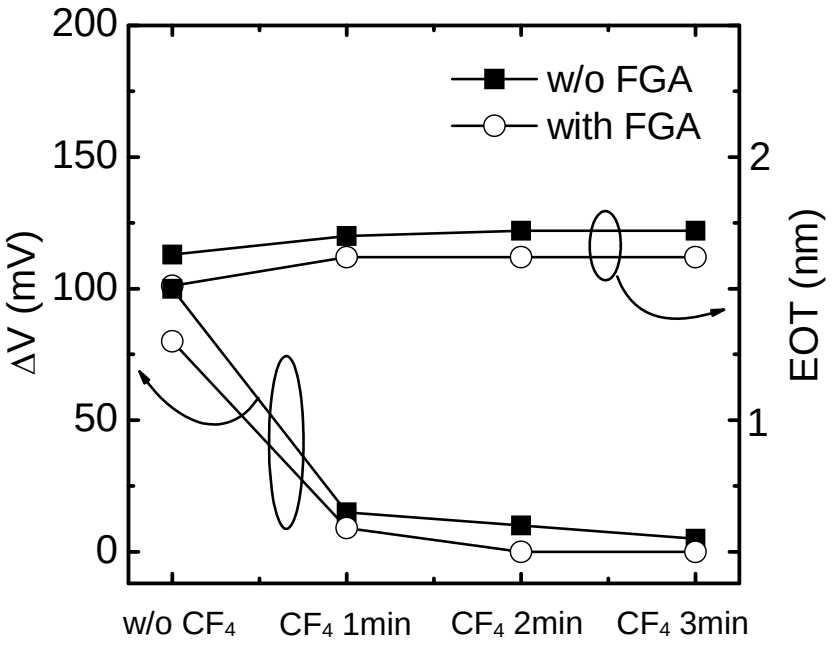

Fig. 5.5. Frequency dependent flat band voltage shifts (ΔV) and Equivalent oxide thickness (EOT) for samples both with and without FGA of different CF_4 treatment conditions.

Fig. 5.4 (c) and (d) shows the *C-V* frequency dispersion characteristics for samples with FGA. It can be seen that *C-V* stretch-outs and size of the kinks become

smaller and almost diminish for samples with 3 min CF_4 treatment. However, the reduction of frequency dependent flat band voltage shift after FGA is not so pronounced compared to 1 min CF_4 plasma treatment, as shown in Fig 5.5. This indicates that FGA is useful to passivate the interface states but not so effective to reduce D_{it} in the upper half of the bandgap. In addition, positive flat band voltage shifts are observed after either CF_4 treatment or FGA. This is possibly attributed to the reduction of positive fixed charges by F or H passivation, respectively.

Berkeley quantum mechanical capacitance voltage (QMCV) simulation code modified for Ge was used to estimate gate stack equivalent oxide thickness (EOT) by fitting the *C-V* data using lower frequency curves (10 kHz) in accumulation which are the least affected by series or shunt resistance [14] and are summarized in Fig. 5.5. It can be seen that F incorporation will not cause any significant EOT change (~ 1 Å EOT increment). The decrease of EOT values (~ 1Å) after FGA is due to the high-k densification. The total EOT value is about 1.5 to 1.6 nm for HfO_2/GeO_2 dual layer. Therefore the EOT contribution is about 0.7 nm from GeO_2, assuming EOT contribution is about 0.9 nm for 4.5 nm HfO_2. The relative dielectric constant of GeO_2 is thus about 11, which is consistent with value (~ 7 to 12) reported in Ref [15].

Gate leakage currents of Ge MOS capacitors are shown in Fig. 5.6. Low leakage currents of order of 10^{-7} to 10^{-6} A/cm^2 are observed for all the samples at 1 V gate voltage, indicating good gate dielectrics (HfO_2/GeO_2 dual layer) quality. Samples with F incorporation show smaller leakage current in the accumulation region. This is possibly

due to lower trap assisted tunneling. It should also be noted that samples with F incorporation have about 1 Å thicker EOT.

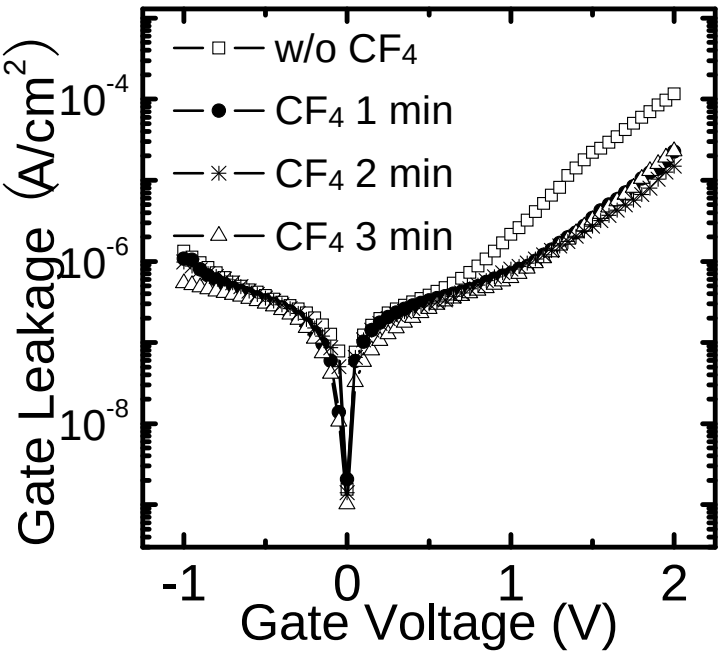

Fig. 5.6. I_g-V_g characteristics for forming gas annealed samples with different CF_4 plasma treatment conditions.

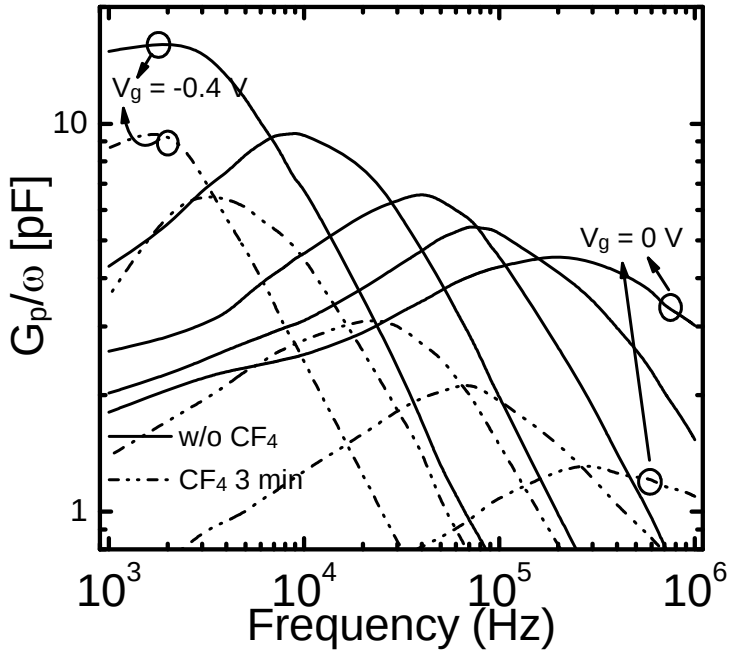

Fig. 5.7. Typical frequency dependent conductance G_p/ω for a series of gate voltage for forming gas annealed samples without CF_4 plasma treatment and samples with CF_4 plasma treatment for 3 min.

Finally, D_{it} was measured using frequency dependent conductance method. A series of ac conductance measurements was performed as a function of frequency. Fig. 5.7 shows the typical measured frequency dependencies of G_p/ω for various gate voltages for samples with FGA. The peaks of G_p/ω for each gate voltages are clearly distinguished and the amplitude of the peak is a strong function of gate voltages. Fig. 5.8 is the plot of the extracted D_{it} values at midgap. A low D_{it} value of 6.33×10^{11} $cm^{-2}eV^{-1}$ is observed for samples without CF_4 treatment and D_{it} further decreases as CF_4 treatment duration increases. The D_{it} value as low as 2.02×10^{11} $cm^{-2}eV^{-1}$ is achieved for samples with 3 min CF_4 treatment and FGA, approaching the state-of-the-art metal-gate/HfO_2/SiO_x/Si gate stacks (typically mid to high 10^{10} $cm^{-2}eV^{-1}$).

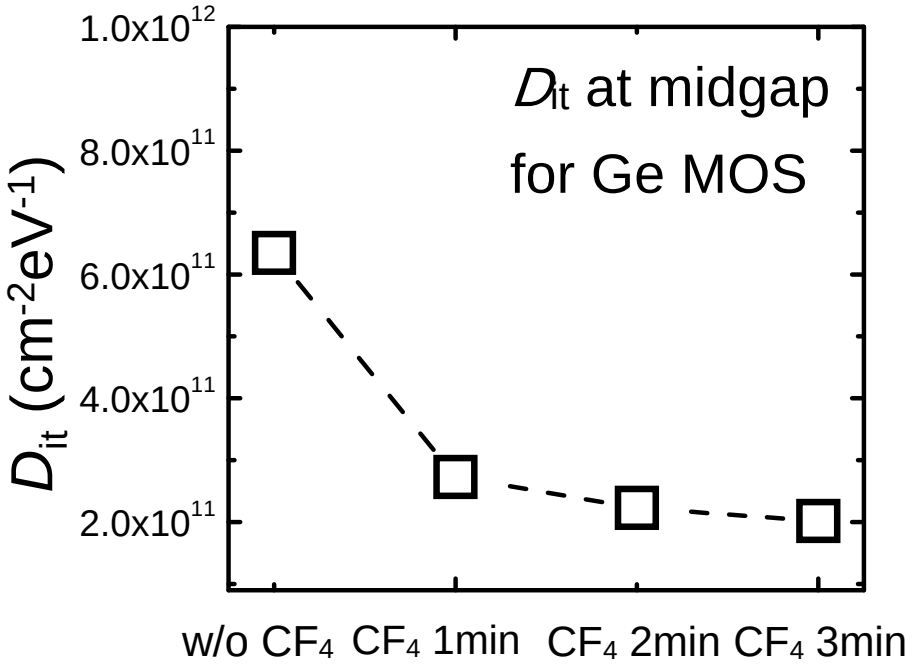

Fig. 5.8. Extracted midgap D_{it} for FGA annealed samples with different F treatment condition.

5.1.3 Summary

GeO_2 is an effective passivation layer for high-k/Ge gate stack. By controlling the growing condition, GeO_2 with good stoichiometry can be achieved with little volatile GeO_x ($x < 2$) component. TaN/HfO_2/GeO_2/Ge gate stack with small leakage current and low D_{it} have been demonstrated. Furthermore, the effects of two post-gate passivation techniques including CF_4-plasma treatment and FGA on high-k/Ge gate stack have been investigated. Both treatments can improve the interface quality, where the F incorporation is more effective to reduce the frequency dependent flat band voltage shift. By combining F incorporation and FGA, excellent electrical characteristics with negligible *C-V* stretch-out and frequency dispersion are achieved. The interface trap density of TaN/HfO_2/GeO_2/Ge MOS structure is as low as 2.02×10^{11} $cm^{-2}eV^{-1}$ at the minimum.

5.2 Ge pMOSFETs with 1 nm EOT

5.2.1 Devices performance of Ge pMOSFETs

Based on the MOS capacitor results in the previous section, optimized interface engineering techniques including GeO_2 pre-gate surface passivation, post-gate F incorporation and FGA were implemented to fabricate Ge pMOSFETs (N-type Ge wafers with (100) orientation were used here). Also, to achieve more aggressive scaling on EOT, thinner GeO_2 (~1 nm) and HfO_2 (~3.5 nm) layers were used as the gate dielectrics. The devices were implanted with Boron (1×10^{15} cm^{-2}, 15 keV, 7° tilted) to form the source/drain (S/D). After FGA at 350°C for 2 hours, contact metal (Al) was deposited and patterned.

Fig. 5.9 shows the split *C-V* curves obtained for a 200 μm × 10 μm pMOSFET device. EOT was extracted using a Ge-based *C-V* simulator considering the quantum mechanical effect and is about 10 Å. Fig. 5.10 shows the gate leakage current density as a function of EOT together with published data [16-20]. The gate leakage current density of the HfO_2/GeO_2 dual dielectric layer is of many orders of magnitude lower than the leakage currents of Ge MOS capacitors with GeO_xN_y as gate dielectrics. In addition, although the *k*-value of GeO_2 is relatively low, the HfO_2/GeO_2 dual layer exhibits similar gate leakage current density as the MOS capacitors with HfO_2 or HfON gate dielectrics, indicating good gate stack quality. The gate leakage current of ZrO_2 is slightly lower than that of HfO_2, which is possibly attributed to less interfacial layer formation [17, 21].

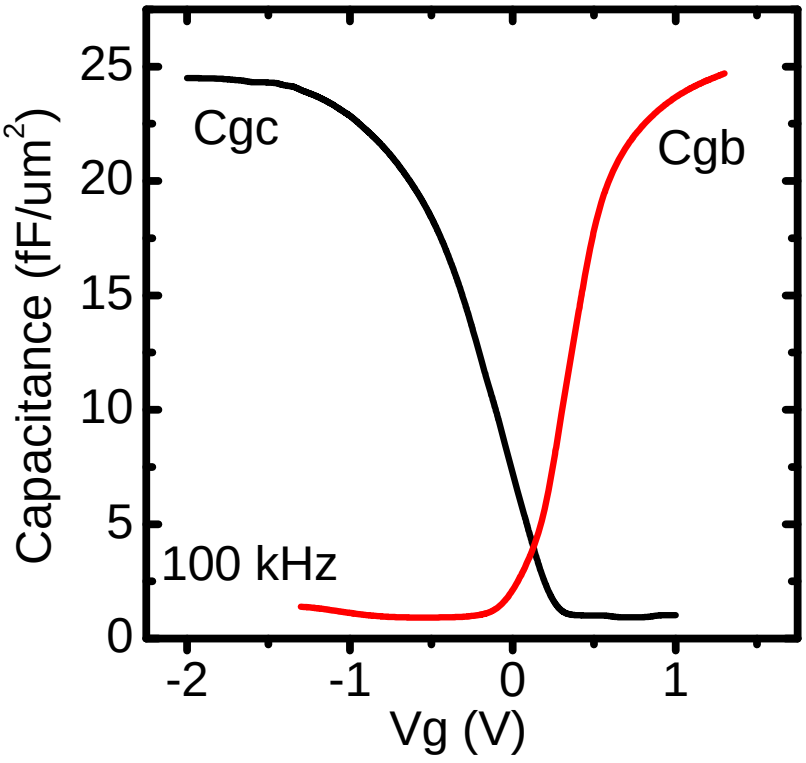

Fig. 5.9. Split *C-V* obtained for a 200μm × 10μm pMOSFET.

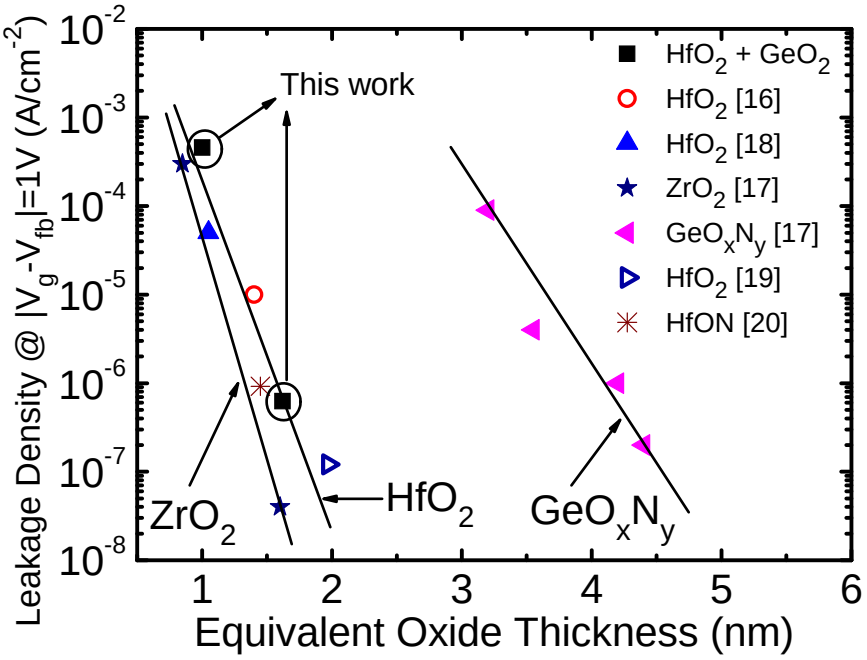

Fig. 5.10. Gate-leakage-current density as a function of EOT together with published data.

The linear I_d-V_g curves for the same 200 μm × 10 μm pMOSFETs are shown in Fig. 5.11. The device with F incorporation exhibits enhanced drain-current and transconductance G_m. Mobility as a function of vertical effective field is extracted using split *C-V* method and plotted in Fig. 5.12(a). Compared with the devices with only FGA, devices with F incorporation exhibit about 12% and 17% higher peak and high field hole mobility, respectively. This is ascribed to the better interface quality after the F passivation. Peak hole mobility of 396 $cm^2/V{\cdot}s$ at a vertical effective field of 0.178 MV/cm is achieved for devices with both F incorporation and FGA, which is better than previous recorded values for unstrained Ge transistors as shown in Fig. 5.12(b) [5, 22, 23]; whereas devices with only GeO_2 surface passivation and FGA show comparable mobility as the previous recorded values achieved by using either Si passivation [23] or GeO_2 as gate dielectric [5]. A three times the universal hole mobility for SiO_2/Si is maintained for

the vertical fields up to 0.9 MV/cm, which is the region of interest for highly scaled transistors.

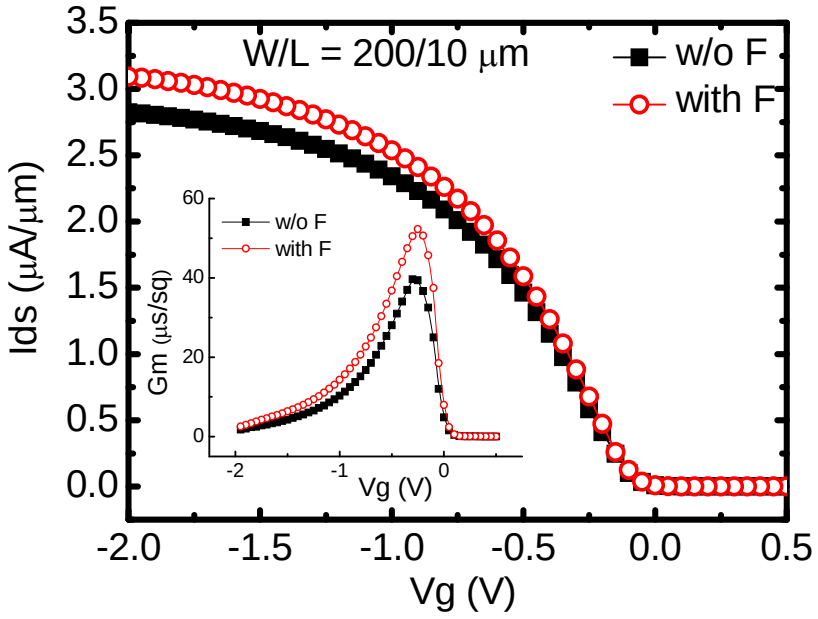

Fig. 5.11. Linear I_d-V_g and G_m-V_g obtained for 200μm × 10μm pMOSFETs. Device with F incorporation shows higher I_d and G_m.

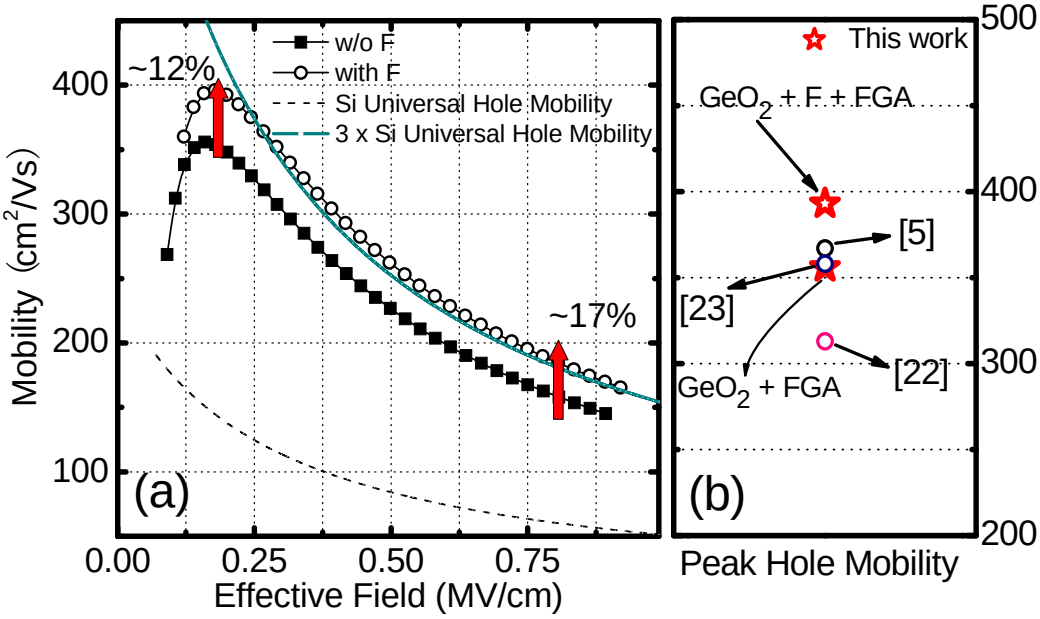

Fig. 5.12. Hole mobility as a function of vertical effective field for 200μm × 10μm pMOSFETs, with and without F incorporation. The mobility enhancement is maintained for large field. Right figure shows the comparison of peak hole mobility with previous reported record values [5, 22, 23].

The I_{on}/I_{off} ratio for F incorporated samples is about 1.2×10^3 as shown in Fig. 5.13 (This ratio is much smaller than the state-of-the-art MOSFETs made on Si substrate due to smaller bandgap of Ge), which is similar to the reported Ge pMOSFETs made on pure Ge substrate [7, 24, 25]. The I_{on}/I_{off} can be improved if careful implantations are used [26]. A smaller sub-threshold swing (85 mV/dec) is observed with F incorporation, suggesting the better interface quality, which is consistent with the previous MOS capacitor and mobility results. Fig. 5.14 shows the well-behaved output characteristics of the 200 μm × 10 μm pMOSFET devices, with flat drain-current in the saturation region. The Ge pMOSFETs with F incorporation show an ~18% improved drain-current over the ones without F passivation under the same overdrive of gate bias in the saturation region. A drive-current of 37.8 μA/μm at $V_g - V_t = -1.2V$ is obtained for devices with F incorporation.

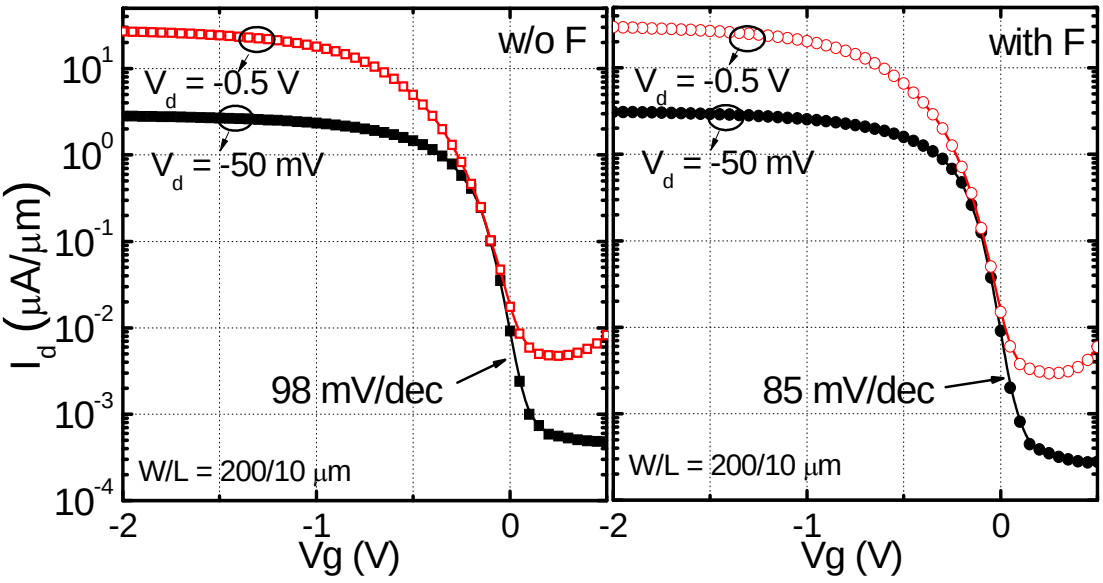

Fig. 5.13. Well behaved I_d-V_g characteristics for the 200μm × 10μm pMOSFETs with and without F incorporation. Devices with GeO_2 passivation and Forming gas annealing (FGA) show SS about 98mV/dec, while devices with GeO_2 passivation and both post-gate treatments including CF_4 plasma treatment and FGA exhibit smaller SS about 85mV/dec, indicating better interface quality.

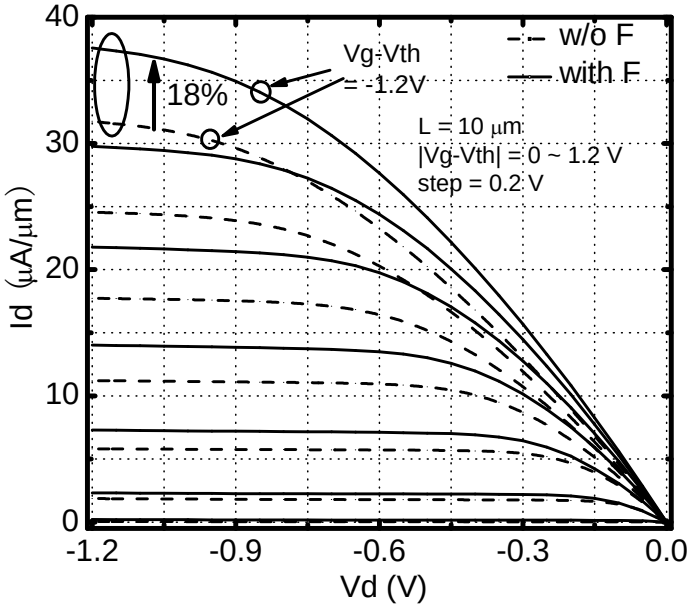

Fig. 5.14. I_d-V_d for 200μm × 10μm pMOSFETs. About 18% Enhanced drive current is obtained after F incorporation. Drive current is 37.8 μA/μm at $V_g - V_t = V_d = -1.2V$. This is the highest record drive current published for unstrained Ge devices to date.

Fig. 5.15 plots the total resistance as a function of gate length for three different gate bias voltages. The S/D series resistance was estimated to be about 10 Ω for the 200 μm gate width (i. e. ~ 2000 Ωμm). The measured S/D resistance and I_{on}/I_{off} ratio are also consistent with the junction leakage characteristics as shown in the right figure in Fig. 5.15. Note that S/D resistance for our devices is much higher than those of state-of-the-art devices with silicide S/D. Even better drive current performance can be obtained through careful S/D engineering to minimize the S/D resistance [27, 28]. In the literature, high mobility Ge pMOFESTs with high-k gate dielectric can be achieved through a few alternative pre-gate and post-gate treatment processes or combinations: (1) Si passivation (SiH_4 treatment, epitaxial Si on Ge or SiO_x directly on Ge) [23, 24]; (2) GeO_2 passivation (thermal oxidation or direct sputter GeO_2 on Ge [5]); (3) H_2 or H^+ annealing [23] and (4) F incorporation as discussed in Chapter 4. Our results indicate that native Ge oxide

passivation layer seems more beneficial for high-performance Ge MOSFETs than Si passivation and a combination of GeO_2 passivation, hydrogen passivation and F incorporation, will achieve even more superior device performance.

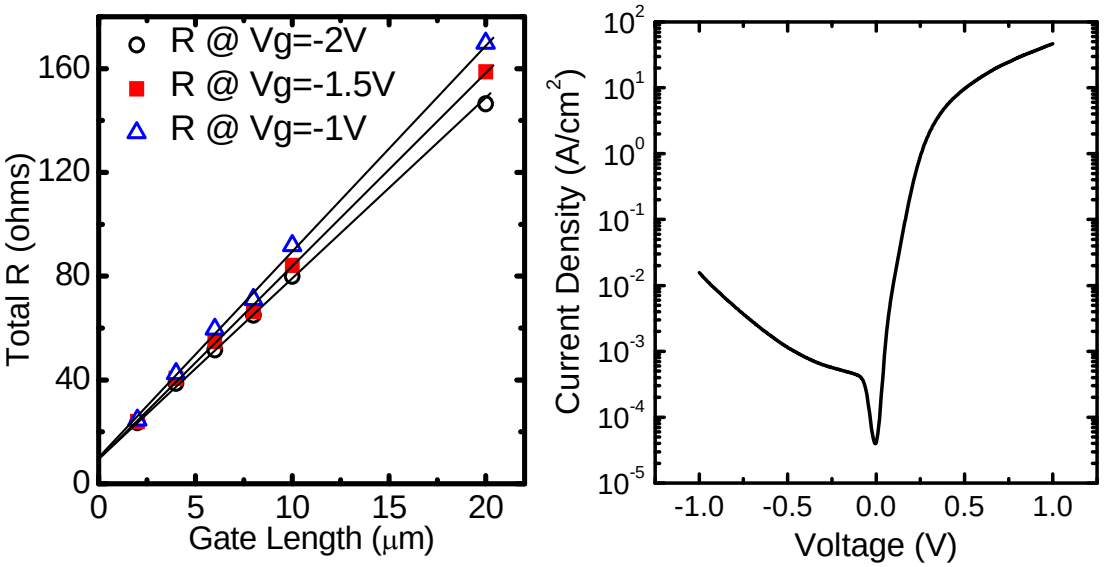

Fig. 5.15. Left: Series resistance R_s for the Al contacted Source/Drain extracted from the total resistance vs. gate length at V_g = -2V, -1.5V and -1V for 200μm width devices. Right: Junction leakage characteristics.

5.2.2 Interface Characterization

Direct characterization of interface property for Ge MOSFETs is critically important for better understanding the effects of interface engineering processes. Charge pumping has been demonstrated to be a powerful tool to characterize the interface trap density with high accuracy and sensitivity for MOSFETs. The basic setup for the charge pumping measurement, as introduced by Brugler and Jespers [29] is illustrated in Fig. 5.16. When the transistor is pulsed into inversion, surface become deeply depleted and electrons flow from S/D to channel region and some of them will be captured by surface states as shown in Fig. 5.17(a). When the gate pulse is driving the surface back into accumulation, the mobile charges drift back to S/D, but the charges trapped in the surface

states will recombine with the majority carriers from the substrate and give rise to a net flow of negative charge into substrate as shown in Fig. 5.17(b), which is so called the CP effect. By measuring this substrate current, an estimate of the mean value of the interface-state density over the energy range swept by the gate pulse can be obtained.

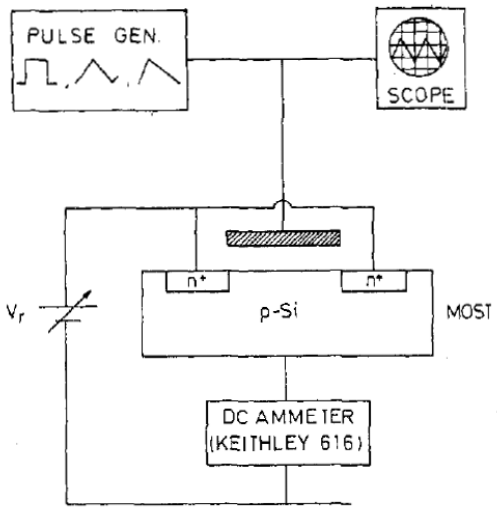

Fig. 5.16. Basic experimental set-up for charge pumping measurement [8].

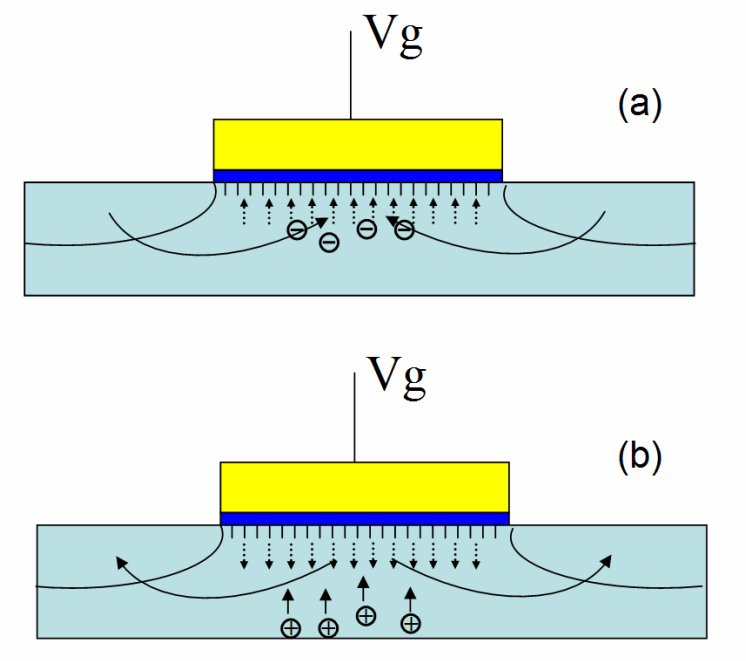

Fig. 5.17. Illustration of charge pumping effects by varying the V_g on a MOSFET.

In this section, the charge pumping measurements were performed with S/D grounded while sweeping the base level of a constant-amplitude (V_a) gate pulse at the frequency of 200 kHz. The definition of rise time (t_r) and fall time (t_f) for the trapezoidal pulse is shown in Fig. 5.18. Variable rise/fall time CP method as described in [8] is implemented to characterize the mean D_{it} of Ge pMOSFETs and the energy distributions of interface traps.

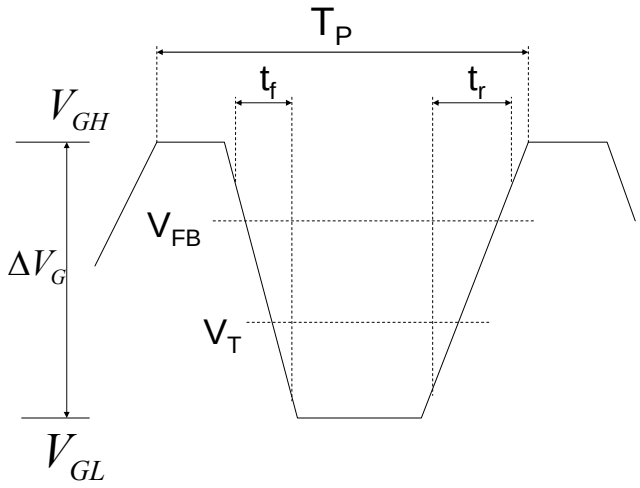

Fig. 5.18. Waveform applied at the gate when performing charge pumping.

Fig. 5.19 illustrated how the D_{it} and energy distributions of D_{it} are related to the rise and fall time of gate pulse. During the fall time t_f, electrons trapped in the surface states will also have chance to emit to the conduction band. Those electrons will not recombine with majority carrier later. Therefore, the longer the t_f is, the smaller the I_{cp}. The I_{cp} will have a large dependency with t_f if D_{it} in the upper half of the bandgap is high. Similarly, the longer the t_r is, the smaller the I_{cp}. The I_{cp} will have a large dependency with t_r if D_{it} in the bottom half of the bandgap is high.

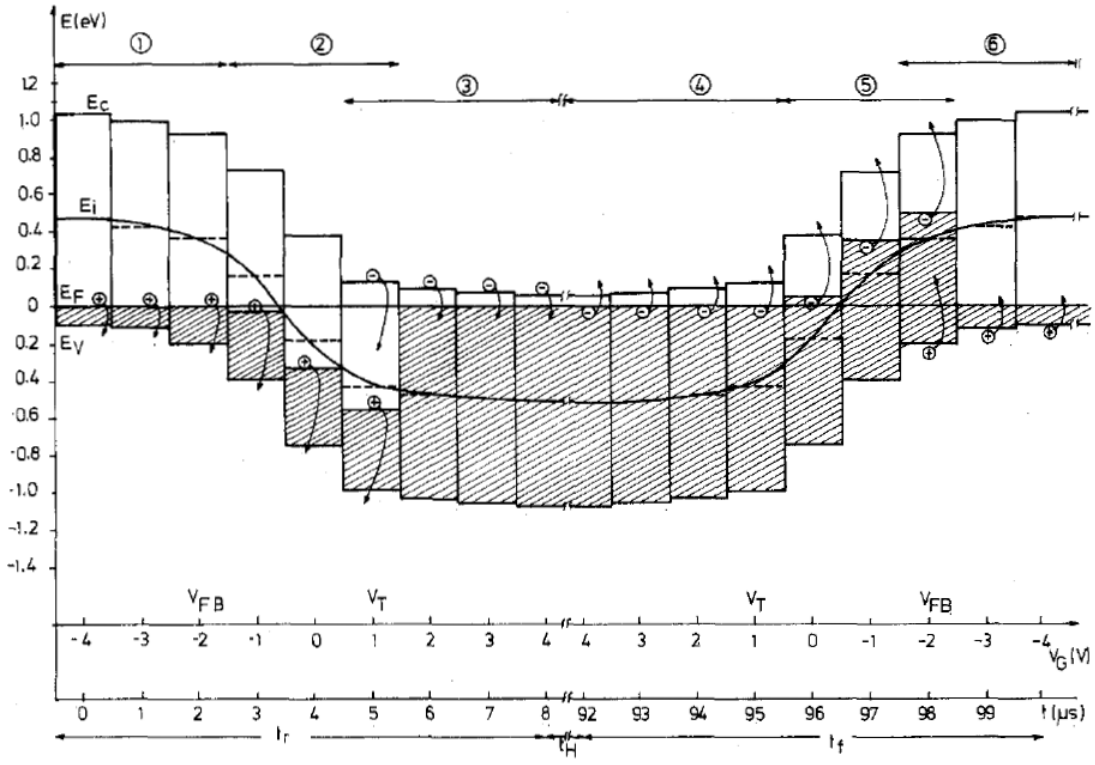

Fig. 5.19. Different processes occurring during one cycle of the gate pulse *(T_p* = 100 us), using the energy-band diagrams (the Fermi level is used as the zero reference level) [8]:
1) steady-state emission of holes to valence band (towards the substrate)
2) nonsteady-state emission of holes to valence band (towards the substrate)
3) trapping of electrons (from source and drain);
4) steady-state emission of electrons to conduction band (towards source and drain)
5) nonsteady-state emission of electrons to conduction band (towards source and drain)
6) trapping of holes (from substrate).

Table 5.1 shows the equations used for analyzing CP data with trapezoidal pulse waveform in this experiment. Fig. 5.20 shows a typical rise/fall time dependence of charge pumping currents (I_{cp}) for samples with and without F incorporation. Samples without F incorporation exhibit higher charge pumping currents than that for samples with F incorporation at any rise/fall time condition, indicating higher interface trap density. Fig. 5.21 shows the plot of $I_{\rm cp}$ as a function of $\ln(t_r \cdot t_f)^{1/2}$. The mean value of $D_{\rm it}$

was extracted to be 3.07×10^{12} $cm^{-2}eV^{-1}$ for samples without F and 9.55×10^{11} $cm^{-2}eV^{-1}$ for samples with F incorporation. With the F incorporation, about three times reduction for D_{it} is achieved.

Table 5.1. Equations used for analyzing CP data with trapezoidal pulse waveform [8].

1. $\frac{Icp}{f} = 2qD_{it}AkT\left\{\ln\sqrt{t_r t_f} + \ln\left(\frac{\lvert V_{fb}-V_t\rvert}{\lvert V_a\rvert}V_{th}n_i\sqrt{\sigma_n\sigma_p}\right)\right\}$
2. $E_{em.e} - E_i = -kT\ln(V_{th}n_i\sigma_n\frac{\lvert V_{fb}-V_t\rvert}{V_a}t_f + e^{(E_i-E_{f.inv})/kT})$
3. $E_{em.h} - E_i = +kT\ln(V_{th}n_i\sigma_p\frac{\lvert V_{fb}-V_t\rvert}{V_a}t_r + e^{(-E_i+E_{f.acc})/kT})$
4. $D_{it}(E_2) = -\frac{t_f}{qAkTf}\frac{dI_{cp}}{dt_f}$.....($t_r$ constant)
5. $D_{it}(E_1) = -\frac{t_r}{qAkTf}\frac{dI_{cp}}{dt_r}$.....($t_f$ constant)

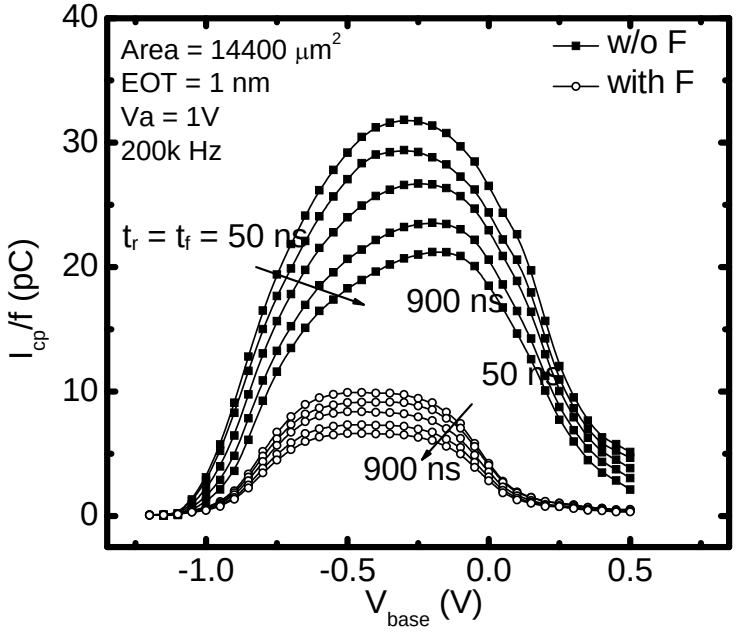

Fig. 5.20. Rise/fall time dependence of CP current ($t_r = t_f$ = 50, 100, 200, 500, 900 ns) for Ge pMOSFETs with or without F incorporation.

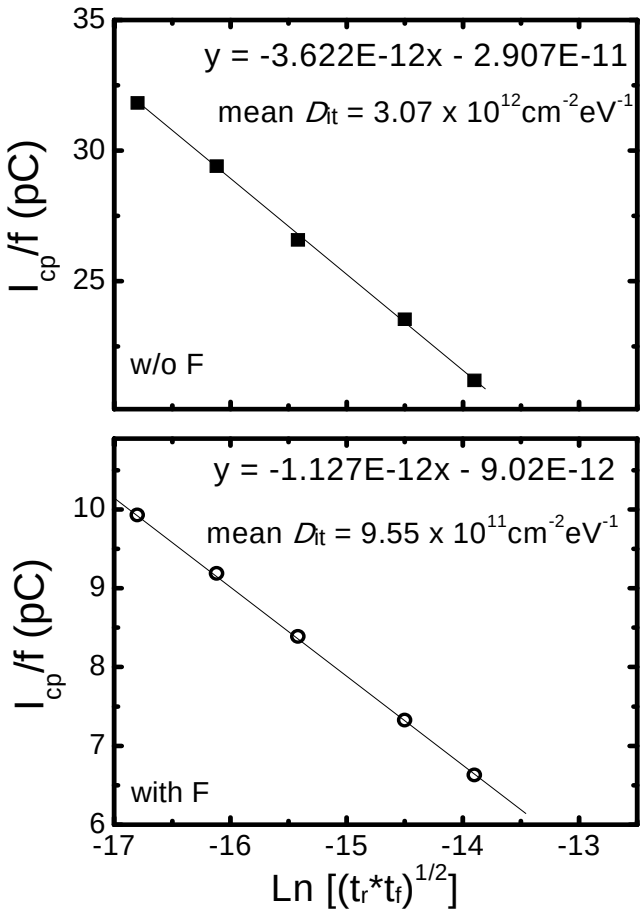

Fig. 5.21. Q_{cp} (= I_{cp}/f) as a function of $\ln(t_r \cdot t_f)^{1/2}$ provides the mean D_{it} for samples without F incorporation is about 3.07 × 10^{12} cm^{-2}eV^{-1} and for samples with F incorporation is about 9.55×10^{11} cm^{-2}eV^{-1}, respectively.

The energy distribution of D_{it} is further investigated by using variable t_r and t_f. By changing t_f while keeping t_r constant, the energy is gradually swept through electron emission energy level ($E_{em.e}$) above midgap. Likewise, by changing t_r while keeping t_f constant, the energy is gradually swept through hole emission energy level ($E_{em.h}$) below midgap [8]. Fig. 5.22 demonstrates strong dependence of I_{cp} on both rise and fall time, indicating high D_{it} is present in both upper and lower half of Ge bandgap for samples without F incorporation. Whereas for samples with F incorporation, the dependence of I_{cp} on rise and fall time is much weaker as shown in Fig. 5.23, implying the D_{it} in both upper

and lower half of the Ge bandgap becomes lower. Fig. 5.24 shows the density of interface traps as function of energy in the Ge bandgap as extracted from the data in Fig. 5.22 and 5.23 using equation 2-5 in Table 5.1, assuming that the change of the time in the trapezoidal waveform for upper and lower levels does not impact the I_{cp}. Room-temperature charge pumping data do not allow us to obtain D_{it} closer to the band edges due to the thermal emission, but the trend is obvious that D_{it} is significantly reduced in both upper and lower half of the Ge bandgap after the F incorporation.

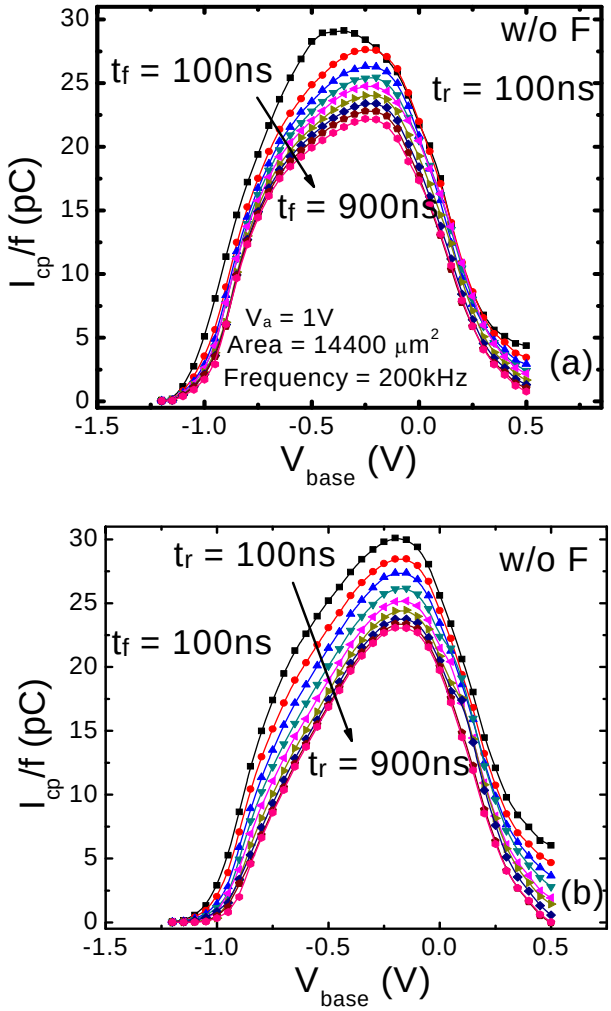

Fig. 5.22. (a) Fall time dependence of CP current curves for fixed rise time of 100 ns to measure the D_{it} distribution in the upper half of the Ge bandgap. (b) Rise time dependence of CP current curves for fixed fall time of 100 ns to measure the D_{it} distribution in the lower half of the Ge bandgap for samples without F incorporation.

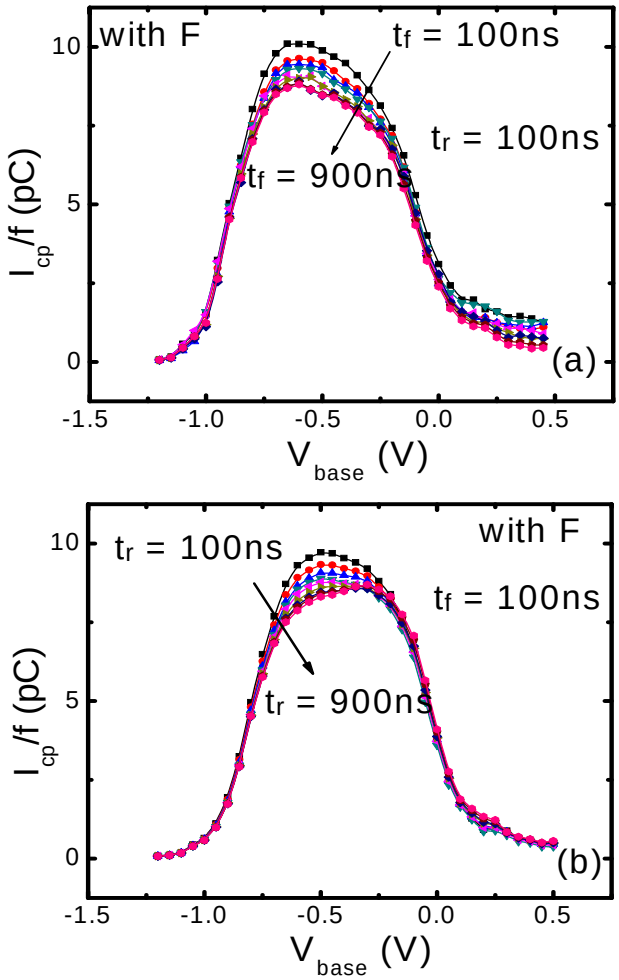

Fig. 5.23. (a) Fall time dependence of CP current curves for fixed rise time of 100 ns to measure the D_{it} distribution in the upper half of the Ge bandgap. (b) Rise time dependence of CP current curves for fixed fall time of 100 ns to measure the D_{it} distribution in the lower half of the Ge bandgap for samples with F incorporation.

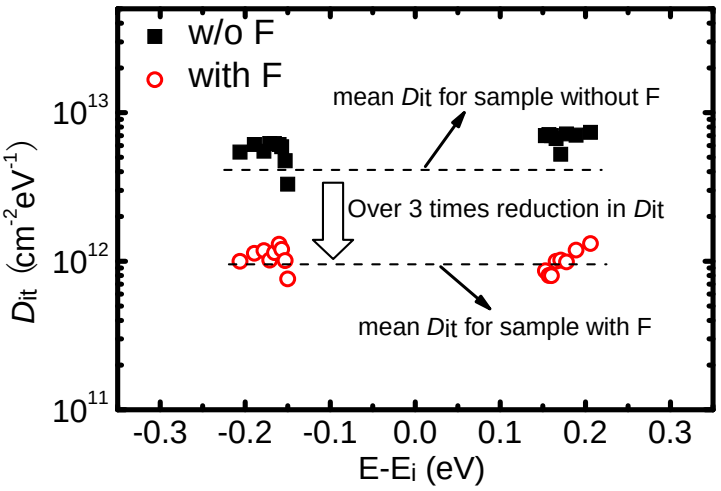

Fig. 5.24. Energy distribution of D_{it} as determined by rise/fall time dependence of I_{cp}.

5.2.3 Discussions

Recently, it was reported that GeO_2/Ge MOS capacitor fabricated using direct thermal oxidation and post H^+ annealing could achieve very low D_{it} even in both upper and lower half of Ge bandgap (< 10^{12} $cm^{-2}eV^{-1}$) [3]. However, in the HfO_2 gated Ge MOS capacitors, first principle simulation [30, 31] show that the formation of the Ge-Hf bonds due to the fivefold coordination of Hf in the GeO_x matrix will generate defect levels in the upper half of Ge bandgap. This is consistent with the high D_{it} (~ 5×10^{12} $cm^{-2}eV^{-1}$) observed in the upper half of Ge bandgap for our devices without F incorporation. When the F is introduced into the gate stack, formation of the Hf-F or Ge-F bonds as illustrated in Fig. 5.25 will hinder the Ge-Hf bonds formation, thus a significant reduction of D_{it} is observed in the upper half of Ge bandgap (~ 1.2 $\times10^{12}$ $cm^{-2}eV^{-1}$). This result is consistent with the observation that negligible ΔV is present in *C-V* characteristics of MOS capacitors with CF_4 plasma treatment as shown in Fig. 5.4.

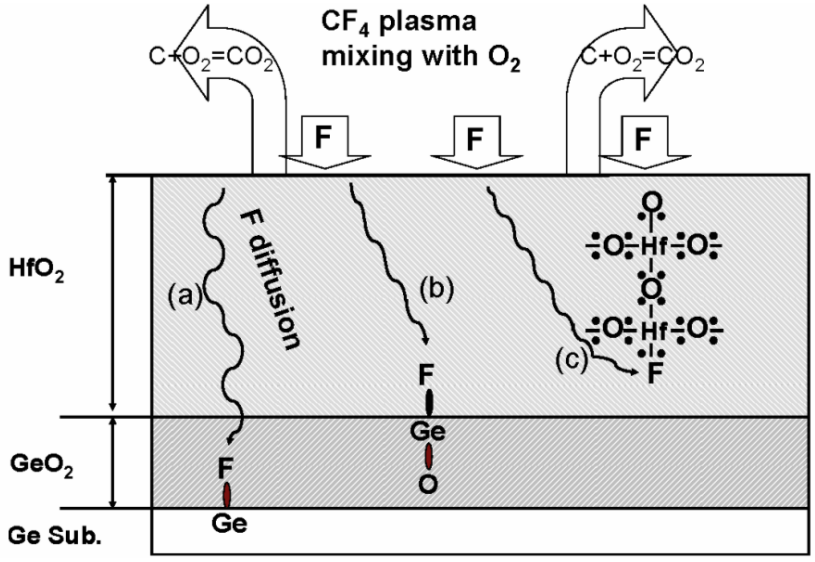

Fig. 5.25. F incorporation into high-k/Ge gate stack and various possible passivation mechanism during subsequent annealing steps: (a) passivation of interface traps at GeO_2/Ge interface by forming Ge-F; (b) passivation of interface traps at HfO_2/GeO_2 interface; (c) passivation of HfO_2 bulk traps by forming Hf-F.

5.3 Conclusions

In conclusions, the effects of post-gate F treatment on GeO_2 passivated MOS devices have been extensively studied. The F incorporation improves the electrical characteristics such as frequency dispersion and *C-V* stretch-out and reduces the interface trap density. Excellent electrical characteristics with negligible *C-V* stretch-out and frequency dispersion are achieved for TaN/HfO_2/GeO_x/Ge MOS structure with D_{it} as low as 2.02 $\times 10^{11}$ $cm^{-2}eV^{-1}$. Ge pMOSFETs have been fabricated using TaN/HfO_2/GeO_x/Ge gate stack with EOT ~ 1 nm without any degradation in gate leakage currents. About three time the SiO_2/Si universal hole mobility at vertical effective field up to 0.9 MV/cm have been achieved. A high drain current for unstrained Ge of 37.8 μA/μm at $V_g - V_t = V_d = -1.2V$ is presented for a channel length of 10 μm. The interface quality of Ge MOSFETs has been further investigated using variable rise and fall time charge pumping method. D_{it} in both upper and lower half of the Ge bandgap has been significantly reduced with F incorporation, thanks to the effective passivation of interface defects by F incorporation.

References:

[1] V. V. Afanas'ev, A. Stesmans, A. Delabie, F. Bellenger, M. Houssa, and M. Meuris, "Electronic structure of GeO_2-passivated interfaces of (100)Ge with Al_2O_3 and HfO_2," *Applied Physics Letters,* vol. 92, 022109, Jan 2008.

[2] A. Delabie, F. Bellenger, M. Houssa, T. Conard, S. Van Elshocht, M. Caymax, M. Heyns, and M. Meuris, "Effective electrical passivation of Ge(100) for high-k gate dielectric layers using germanium oxide," *Applied Physics Letters,* vol. 91, 082904, Aug 2007.

[3] H. Matsubara, T. Sasada, M. Takenaka, and S. Takagi, "Evidence of low interface trap density in GeO_2/Ge metal-oxide-semiconductor structures fabricated by thermal oxidation," *Applied Physics Letters,* vol. 93, 032104, Jul 2008.

[4] K. Kita, S. Suzuki, H. Nomura, T. Takahashi, T. Nishimura, and A. Toriumi, "Direct evidence of GeO volatilization from GeO_2/Ge and impact of its suppression on GeO_2/Ge metal-insulator-semiconductor characteristics," in *International Conference on Solid State Devices and Materials*, Tsukuba, JAPAN, 2007, pp. 2349-2353.

[5] T. Takahashi, T. Nishimura, L. Chen, S. Sakata, K. Kita, and A. Toriumi, "Proof of Ge-interfacing concepts for metal/high-k/Ge CMOS Ge-intimate material selection and interface conscious process flow," in *IEEE International Electron Devices Meeting*, Washington, DC, 2007, pp. 697-700.

[6] D. Kuzum, T. Krishnamohan, A. J. Pethe, A. K. Okyay, Y. Oshima, Y. Sun, J. P. McVittie, P. A. Pianetta, P. C. McIntyre, and K. C. Saraswat, "Ge-interface engineering with ozone oxidation for low interface-state density," *IEEE Electron Device Letters,* vol. 29, pp. 328-330, Apr 2008.

[7] D. Kuzum, A. J. Pethe, T. Krishnamohan, Y. Oshima, Y. Sun, J. P. McVittie, P. A. Pianetta, P. C. McIntyre, and K. C. Saraswat, "Interface-engineered Ge (100) and (111), N- and P-FETs with high mobility," in *IEEE International Electron Devices Meeting*, Washington, DC, 2007, pp. 723-726.

[8] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. Dekeersmaecker, "A Reliable Approach to Charge-pumping Measurements in MOS-Transistors " *IEEE Transactions on Electron Devices,* vol. 31, pp. 42-53, 1984.

[9] K. Prabhakaran, F. Maeda, Y. Watanabe, and T. Ogino, "Distinctly different thermal decomposition pathways of ultrathin oxide layer on Ge and Si surfaces," *Applied Physics Letters,* vol. 76, pp. 2244-2246, Apr 2000.

[10] K. Prabhakaran and T. Ogino, "Oxidation of Ge(100) and Ge(111) surfaces - an UPS and XPS study," *Surface Science,* vol. 325, pp. 263-271, Mar 1995.

[11] J. Reed, Z. Fan, G. B. Gao, A. Botchkarev, and H. Morkoc, "GaAs metal-insulator-semiconductor capacitors and high transconductance metal-insulator-semiconductor field-effect transistors," *Applied Physics Letters,* vol. 64, pp. 2706-2708, May 1994.

[12] K. Martens, B. De Jaeger, R. Bonzom, J. Van Steenbergen, M. Meuris, G. Groeseneken, and H. Maes, "New interface state density extraction method applicable to peaked and

high-density distributions for Ge MOSFET development," *IEEE Electron Device Letters,* vol. 27, pp. 405-408, May 2006.

[13] K. Martens, W. Wang, K. De Keersmaecker, G. Borghs, G. Groeseneken, and H. Maes, "Impact of weak Fermi-level pinning on the correct interpretation of III-V MOS C-V and G-V characteristics," *Microelectronic Engineering,* vol. 84, pp. 2146-2149 2007.

[14] K. J. Yang and C. M. Hu, "MOS capacitance measurements for high-leakage thin dielectrics," *IEEE Transactions on Electron Devices,* vol. 46, pp. 1500-1501, Jul 1999.

[15] Y. Kamata, "High-k/Ge MOSFETs for future nanoelectronics," *Materials Today,* vol. 11, pp. 30-38, Jan-Feb 2008.

[16] J. J. H. Chen, N. A. Bojarczuk, H. L. Shang, M. Copel, J. B. Hannon, J. Karasinski, E. Preisler, S. K. Banerjee, and S. Guha, "Ultrathin Al_2O_3 and HfO_2 gate dielectrics on surface-nitrided Ge," *IEEE Transactions on Electron Devices,* vol. 51, pp. 1441-1447, Sep 2004.

[17] C. O. Chui, H. Kim, D. Chi, P. C. McIntyre, and K. C. Saraswat, "Nanoscale germanium MOS dielectrics - Part II: High-k gate dielectrics," *IEEE Transactions on Electron Devices,* vol. 53, pp. 1509-1516, Jul 2006.

[18] N. Wu, Q. C. Zhang, C. X. Zhu, C. C. Yeo, S. J. Whang, D. S. H. Chan, M. F. Li, B. J. Cho, A. Chin, D. L. Kwong, A. Y. Du, C. H. Tung, and N. Balasubramanian, "Effect of surface NH_3 anneal on the physical and electrical properties of HfO_2 films on Ge substrate," *Applied Physics Letters,* vol. 84, pp. 3741-3743, May 2004.

[19] R. L. Xie, M. B. Yu, M. Y. Lai, L. Chan, and C. X. Zhu, "High-k gate stack on germanium substrate with fluorine incorporation," *Applied Physics Letters,* vol. 92, 163505, Apr 2008.

[20] R. L. Xie and C. X. Zhu, "Effects of sulfur passivation on germanium MOS capacitors with HfON gate dielectric," *IEEE Electron Device Letters,* vol. 28, pp. 976-979, Nov 2007.

[21] Y. Kamata, Y. Kamimuta, T. Ino, and A. Nishiyama, "Direct comparison of ZrO_2 and HfO_2 on Ge substrate in terms of the realization of ultrathin high-k gate stacks," *Japanese Journal of Applied Physics Part 1-Regular Papers Brief Communications & Review Papers,* vol. 44, pp. 2323-2329, Apr 2005.

[22] C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "A Sub-400 degrees C germanium MOSFET technology with high-k dielectric and metal gate," in *IEEE International Electron Devices Meeting*, San Francisco, Ca, 2002, pp. 437-440.

[23] P. Zimmerman, G. Nicholas, B. De Jaeger, B. Kaczer, A. Stesmans, L. A. Ragnarsson, D. P. Brunco, F. E. Leys, M. Caymax, G. Winderickx, K. Opsomer, M. Meuris, and M. M. Heyns, "High performance Ge pMOS devices using a Si-compatible process flow," in *IEEE International Electron Devices Meeting*, San Francisco, CA, 2006, pp. 390-393.

[24] S. Joshi, C. Krug, D. Heh, H. J. Na, H. R. Harris, J. W. Oh, P. D. Kirsch, P. Majhi, B. H. Lee, H. H. Tseng, R. Jammy, J. C. Lee, and S. K. Banerjee, "Improved Ge surface passivation with ultrathin SiO_x enabling high-mobility surface channel pMOSFETs featuring a HfSiO/WN gate stack," *IEEE Electron Device Letters,* vol. 28, pp. 308-311, Apr 2007.

[25] Y. Nakakita, R. Nakane, T. Sasada, H. Matsubara, M. Takenaka, and S. Takagi, "Interface-controlled Self-Align Source/Drain Ge pMOSFETs Using Thermally-Oxidized GeO_2 Interfacial Layers," in *IEEE International Electron Devices Meeting*, San Francisco, CA, 2008, pp. 877-880.

[26] G. Nicholas, B. De Jaeger, D. P. Brunco, P. Zimmerman, G. Eneman, K. Martens, M. Meuris, and M. M. Heyns, "High-performance deep submicron Ge pMOSFETs with halo implants," *IEEE Transactions on Electron Devices,* vol. 54, pp. 2503-2511, Sep 2007.

[27] Y. L. Chao and J. C. S. Woo, "Source/drain engineering for parasitic resistance reduction for germanium p-MOSFETs," *IEEE Transactions on Electron Devices,* vol. 54, pp. 2750-2755, Oct 2007.

[28] R. Li, S. J. Lee, H. B. Yao, D. Z. Chi, M. B. Yu, and D. L. Kwong, "Pt-germanide Schottky source/drain germanium p-MOSFET with HfO_2 gate dielectric and TaN gate electrode," *IEEE Electron Device Letters,* vol. 27, pp. 476-478, Jun 2006.

[29] P. G. A. J. J. S . Brugler, "Charge pumping in MOS devices," *IEEE Transactions on Electron Devices,* vol. ED-16, pp. 297-302, 1969.

[30] M. Houssa, G. Pourtois, M. Caymax, M. Meuris, and M. M. Heyns, "Electronic properties of (100)Ge/Ge(Hf)O_2 interfaces: A first-principles study," *Surface Science,* vol. 602, pp. L25-L28, Feb 2008.

[31] M. Houssa, G. Pourtois, M. Caymax, M. Meuris, and M. M. Heyns, "First-principles study of the structural and electronic properties of (100)Ge/Ge(M)O_2 interfaces (M=Al, La, or Hf)," *Applied Physics Letters,* vol. 92, 242101, Jun 2008.

Chapter 6

Energy Distribution of Interface Traps in Germanium Metal-Oxide-Semiconductor Field Effect Transistors with HfO_2 Gate Dielectrics and Its Impact on Mobility

Over the past few years, Ge high-k gated p-channel MOSFETs with various surface passivation techniques have been demonstrated with improved hole mobility over SiO_2/Si system [1-6]. About three times peak hole mobility over SiO_2/Si universal mobility have been achieved by several groups using either Si passivation [2, 4, 6] or using GeO_2 as gate dielectrics [3]. On the other hand, n-channel Ge MOSFETs with high-k gate dielectrics still show much lower electron mobility than SiO_2/Si universal [3, 7-10]. The causes of this severe mobility degradation for n-channel Ge MOSFETs are still not fully understood, but in order to realize the desired high mobility n-channel Ge MOSFETs, it is clear that a viable high-k gate stack on Ge must at least have a low density of interface traps. So far, a clear correlation between the interface trap density and inversion layer mobility for n-channel Ge MOSFETs has not been necessarily observed. For example, in Ref [7] and [10], no information on interface trap density was given; in Ref [3], a good interface quality was reported with highest recorded hole mobility, however the Ge nMOSFETs still exhibit low electron mobility and in Ref [9], a relatively low interface trap density (D_{it}) value of $4.5\times10^{11}cm^{-2}eV^{-1}$ was reported for Ge nMOSFETs, but electron mobility with less than half of SiO_2/Si universal was observed.

One possible explanation is that although D_{it} is relatively low at midgap of germanium, a high density of interface traps might be present in the upper half of the Ge bandgap near the conduction band, behave like Coulomb scattering centers when the device is under strong inversion as shown in Fig. 6.1. This kind of asymmetric D_{it} distribution for high-k/Ge interface has been reported based on Ge MOS capacitors by using conductance method under low temperatures [11]. However, there is still no direct evidence on the interface trap distributions for Ge MOSFETs under room temperature. Charge pumping (CP) has been demonstrated to be a powerful tool to characterize the D_{it} with high accuracy and sensitivity for MOSFETS [12]. In this study, we apply the variable rise and fall time CP procedure, as described in Section 5.2.3, to study the energy distribution of interface trap density in HfO_2 gated Ge MOSFET with Si passivation. The results are complementarily verified with *C-V* characteristics of Ge MOS capacitors, mobility extraction and mobility simulation of Ge MOSFETs.

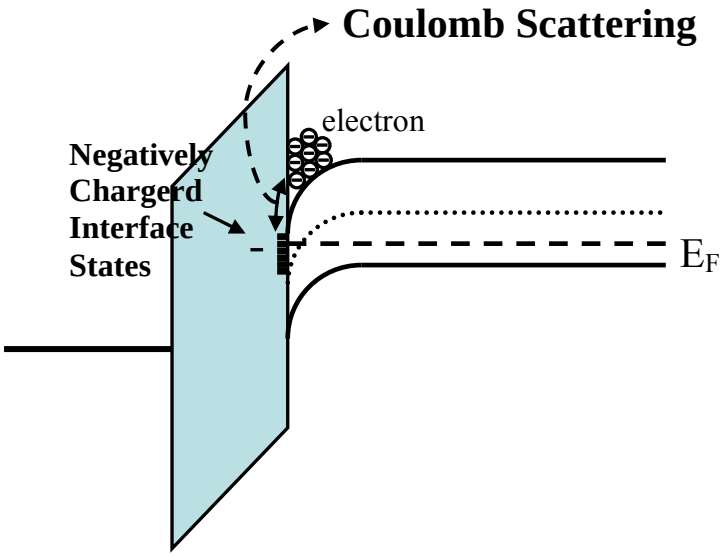

Fig. 6.1. Schematic illustration of n-channel electron mobility degradation by Coulomb Scattering.

6.1 Experiments

The starting Ge wafers are either Sb-doped n-type (100) wafers (0.04-0.08 Ω·cm) or Ga-doped p-type (100) wafers (0.09-0.18 Ω·cm). The wafers were firstly cleaned using diluted HF (1:50) and rinsed in de-ionized water, and then were subject to different surface passivations. The silicon passivation (SP) was carried out by annealing in SiH_4 [9]. The surface nitridation (SN) was carried out in NH_3 ambient under 20 Torr at 600 ºC for 30 sec [13]. HfO_2 was then deposited in a metal organic chemical vapor deposition (MOCVD) chamber in N_2+O_2 ambient and with Hf tert-butoxide as the precursor at temperature of 400°C for both SP and SN samples. After post deposition annealing (PDA) in N_2 at 500 ºC, TaN was reactively sputtered at room temperature, and then patterned by conventional lithography and Cl_2-based plasma etching. The transistor devices were implanted either with boron ($1x10^{15}$ cm^{-2} @ 20 keV) or with phosphorus ($1x10^{15}$ cm^{-2} @ 20 keV). The pMOSFETs source/drain (S/D) activation was carried out under 500^{o}C for 1 min and nMOSFETs S/D was activated using laser annealing described in [10]. Finally, forming gas annealing at 350^{o}C for one hour was carried out as the last step in device fabrication. Current-voltage (*I*-*V*) and Capacitance-voltage (*C*-*V*) characteristics were measured by a HP4196 semiconductor parameter analyzer and an Agilent 4284 LCR meter, respectively. The interface characteristics were analyzed by charge pumping measurements with source/drain grounded while sweeping the base level of a constant-amplitude gate pulse at frequency of 100 kHz.

6.2 Results and Discussions

CP measurement was carried out on HfO_2 gated Ge MOSFETs with SP. The energy distribution of D_{it} is obtained by using variable t_f and t_r as described in Section 5.2.3. By changing t_f while keeping t_r constant, the energy is gradually swept through electron emission energy level ($E_{em,e}$) above midgap. Likewise, by changing t_r while keeping t_f constant, the energy is gradually swept through hole emission energy level ($E_{em,h}$) below midgap. It should be noted that the interfacial layer between high-k gate stack and Ge is quite complicated and the interface traps measured here include all electrically active defects or charge centers that can respond to charge pumping signals.

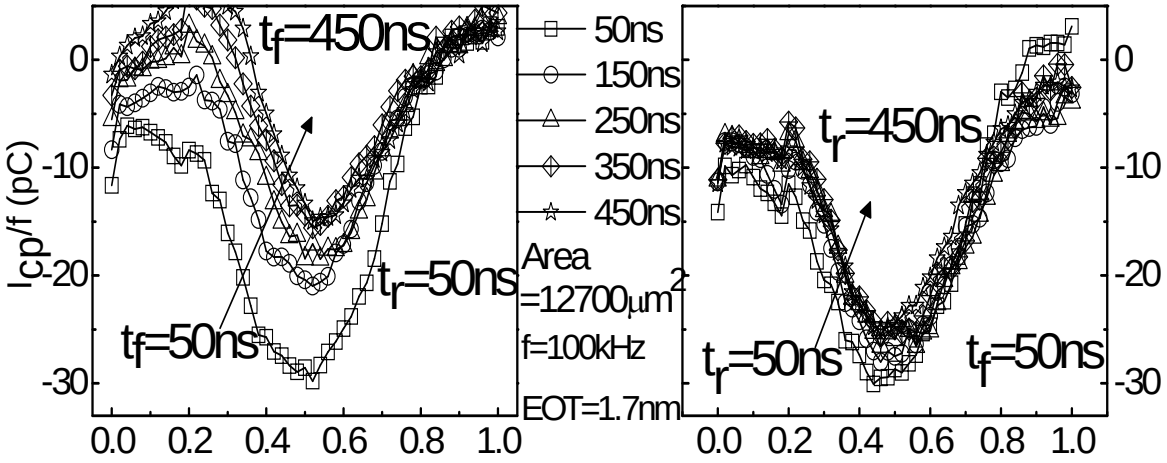

Fig. 6.2. (a) Strong fall-time dependence of charge pumping currents from 50 ns to 450 ns for fixed rise time of 50 ns; (b) Relatively week rise-time dependence of charge pumping currents from 50 ns to 450 ns for fixed fall-time of 50 ns.

Fig. 6.2(a) demonstrates a strong dependence of I_{cp} on the fall time by varying the fall time and keeping the rise time constant. This indicates that the density of interface traps in the upper half of the bandgap is high. On the other hand, Fig. 6.2(b) shows a relatively weak dependence of I_{cp} on rise time while keeping the fall time constant, indicating that density of interface traps in the lower half of the bandgap is lower. Fig. 6.3

shows the density of interface traps as a function of energy in the Ge bandgap as extracted from data in Fig. 6.2(a) and (b).

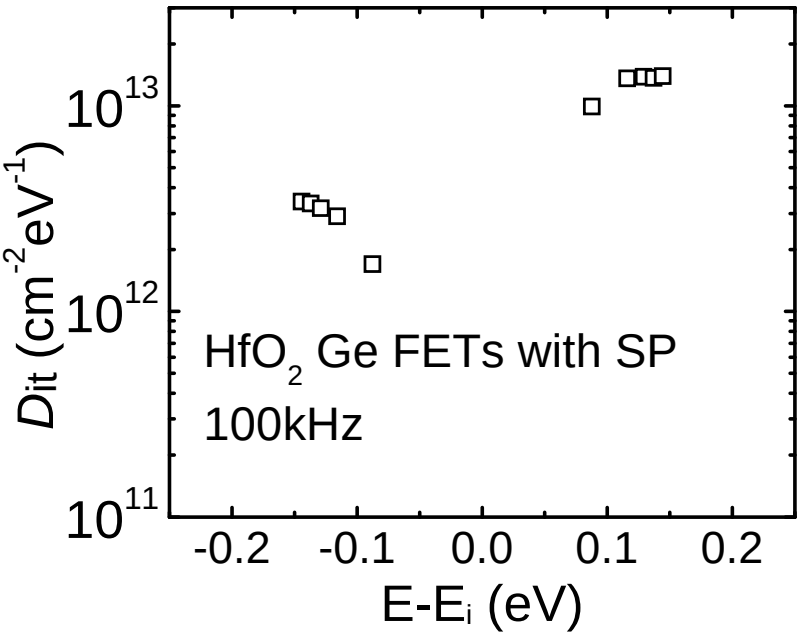

Fig. 6.3. Energy distribution of interface traps in HfO_2 gated Ge MOSFETs as determined by rise/fall time dependence of charge pumping currents under room temperature.

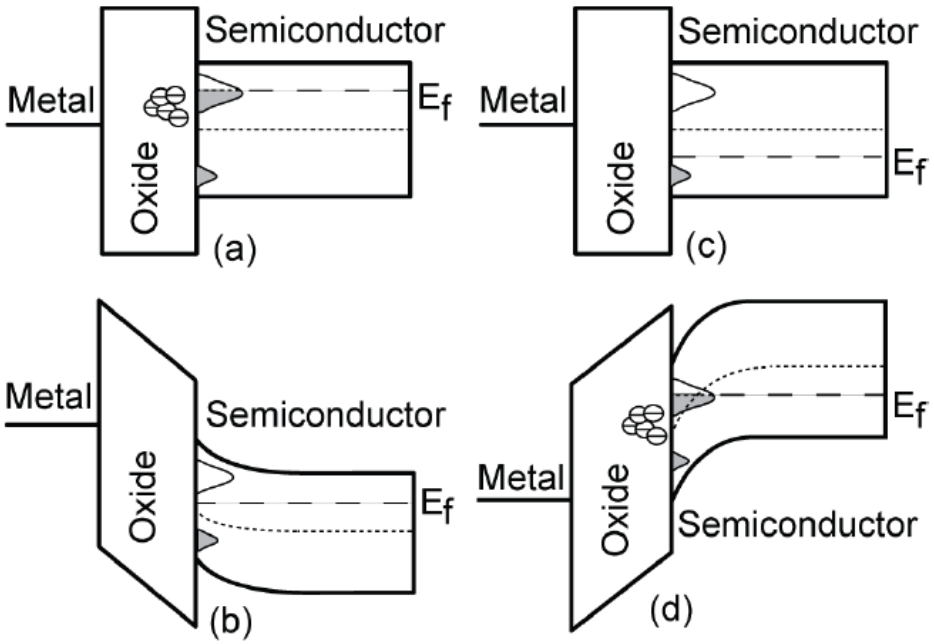

Fig. 6.4. Energy band diagrams of MOS system with asymmetrical distribution of interface trap density along the bandgap. (a) p-MOS under flat-band; (b) p-MOS near weak inversion; (c) n-MOS under flat-band; (d) n-MOS near strong inversion.

This asymmetric D_{it} distribution is consistent with the *C-V* characteristics for both Ge nMOS and pMOS capacitors with different surface passivation techniques and can be explained by a simple model illustrated in Fig. 6.4. Fig. 6.5 shows the high frequency *C-V* characteristics for Ge capacitors with SN or SP. For pMOS capacitors in Fig. 6.5 (a), both capacitors with SN and SP exhibit frequency dependent flat band voltage shift (~0.4 V for SN devices and 50 mV for SP device), which is usually observed in Ge or GaAs MOS capacitors [11, 14]. This is the direct result of interface states [14]. Especially for pMOS capacitors, this phenomenon is the indication of the weak Fermi-level pinning near the conduction band [11, 15]. Fig. 6.4 (a) and (b) show the p-MOS capacitor under flat-band and weak inversion, respectively. At high frequency (100 kHz), the high density interface traps in the upper half of band gap lead to a positive *C-V* shift because of filling of acceptor-like interface states when V_g is increasing; when the frequency decreases (10 kHz), some of the traps can respond to the gate voltage and contribute an additional capacitance, giving an illusion that V_{fb} shifts towards the negative direction.

As for the case of n-MOS in Fig. 6.5(b), no frequency dependent flat band voltage shift is observed for both SN and SP devices, this is because when the Fermi level is swept from the edge of valence band towards the mid-gap, the majority interface states (above the mid-gap) are above the Fermi level and do not contribute to the capacitance so that the capacitance is independent of measurement frequency as shown in Fig. 6.4(c) and (d). However, both abnormal inversion capacitance for SN device and kinks for SP device are observed. This is caused by the interface traps located at upper half of the germanium bandgap. When the Fermi level crosses the mid-gap and approaches the

upper half of the interface states (inversion), these interface states can lead to a large kink in the *C-V* curves (the SN capacitor case). A higher positive gate bias (>2V) would be needed to fill up states below the Fermi level before C_{min} is observed. For SP devices with better interface quality, D_{it} in the upper half of the bandgap will still lead to kinks where the sizes are frequency dependent.

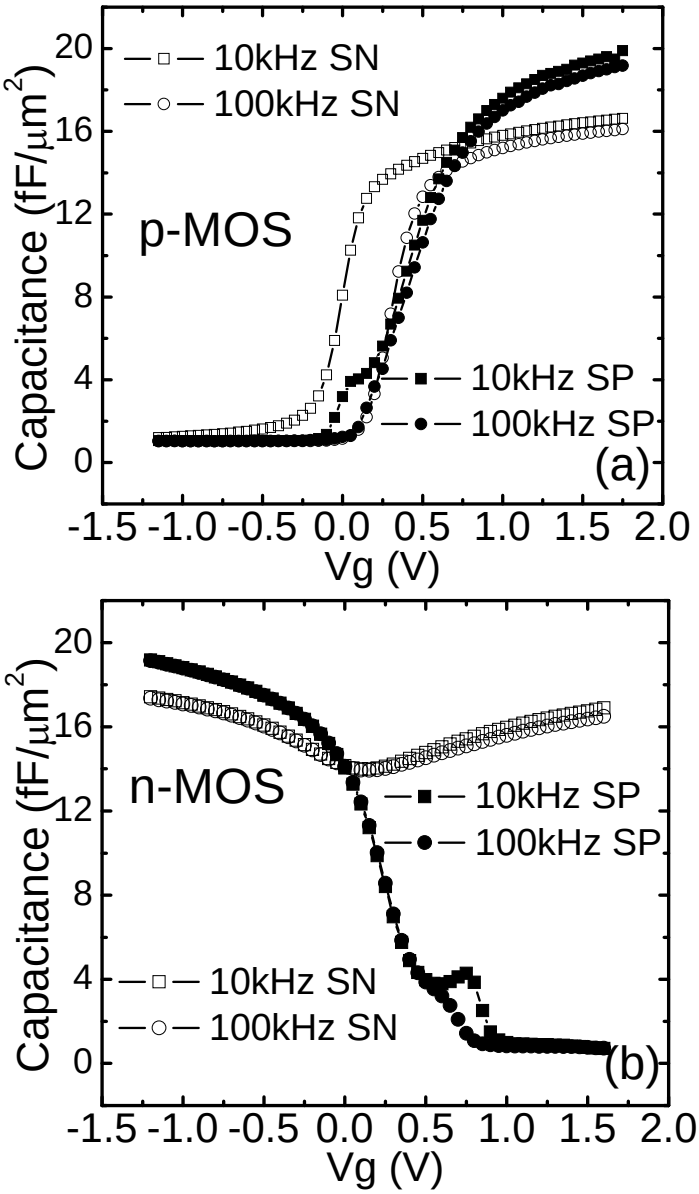

Fig. 6.5. (a) High Frequency Capacitance-Voltage (HFCV) characteristics of TaN/HfO_2/Ge p-MOS capacitors with surface nitridation (SN) or silicon passivation (SP); (b) HFCV characteristics of TaN/HfO_2/Ge n-MOS capacitors with SN or SP.

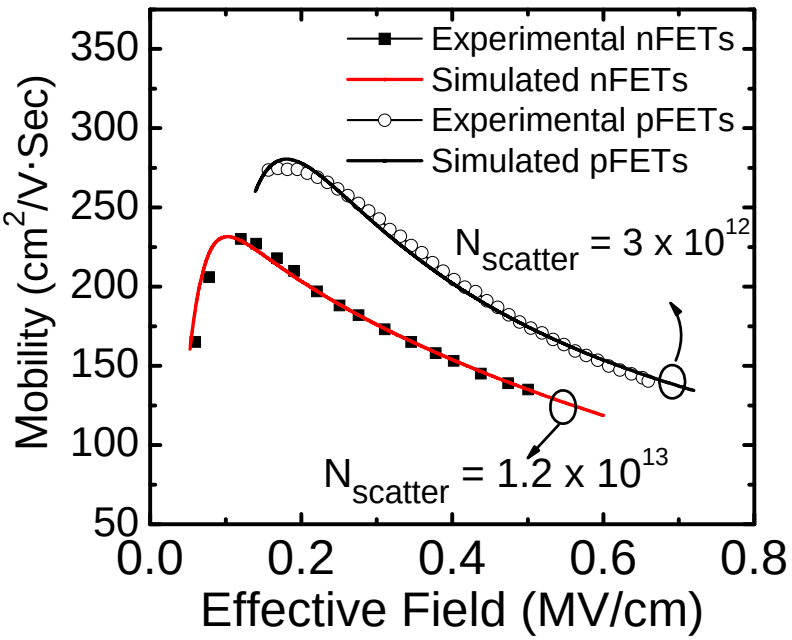

Fig. 6.6. Effective carrier mobility of HfO_2 Ge MOSFETs with SP together with simulation results.

The extracted hole and electron mobility in HfO_2 Ge MOSFETs with SP using split *C-V* technique is plotted in Fig. 6.6 together with simulated mobility data by assuming the interface scattering density is equivalent to the interface trap density. Here the NCSU Mob2d Program [16] is used to simulate the mobility with corresponding parameters modified to Ge. The hole mobility is about twice of Si hole universal (with peak mobility ~ 270 $cm^2/V \cdot s$) whereas the electron mobility (with peak mobility ~ 230 $cm^2/V \cdot s$) is less than half of Si electron universal. The low electron mobility and high hole mobility can be explained consistently by the higher interface trap density in the upper half of the bandgap than that in the lower half of bandgap. These interface traps with high D_{it} value located near the conduction band are acceptor-like traps. For nMOSFET in the inversion, these interface traps are occupied by electrons and become negative charge centers. Thus, we can expect that the Coulomb scatterings due to these

charge centers at or near the high-k/Ge interface, play a significant role for the severe electron mobility degradation for germanium nMOSFETs, especially at low and mid effective field. To minimize the electron mobility degradation in germanium nMOSFET, carefully interface engineering should be performed to reduce the high D_{it} near the conduction band edge.

6.3 Conclusions

In conclusion, asymmetric energy distribution of D_{it} in Ge MOSFETs is revealed by using variable rise and fall time CP method at room temperature. This result is consistent with *C-V* characteristics in Ge MOS capacitors as well as mobility extraction and simulation results for Ge MOSFETs. Both SP and SN could not adequately enhance the Ge nMOSFETs performance. Alternative passivation technique which can significantly reduce the interface traps at upper half of the Ge bandgap should be explored to achieve improved performance for Ge nMOSFETs.

References:

[1] C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "A Sub-400 degrees C germanium MOSFET technology with high-k dielectric and metal gate," in *IEEE International Electron Devices Meeting*, San Francisco, Ca, 2002, pp. 437-440.

[2] S. Joshi, C. Krug, D. Heh, H. J. Na, H. R. Harris, J. W. Oh, P. D. Kirsch, P. Majhi, B. H. Lee, H. H. Tseng, R. Jammy, J. C. Lee, and S. K. Banerjee, "Improved Ge surface passivation with ultrathin SiO_x enabling high-mobility surface channel pMOSFETs featuring a HfSiO/WN gate stack," *IEEE Electron Device Letters,* vol. 28, pp. 308-311, Apr 2007.

[3] T. Takahashi, T. Nishimura, L. Chen, S. Sakata, K. Kita, and A. Toriumi, "Proof of Ge-interfacing concepts for metal/high-k/Ge CMOS Ge-intimate material selection and interface conscious process flow," in *IEEE International Electron Devices Meeting*, Washington, DC, 2007, pp. 697-700.

[4] N. Taoka, M. Harada, Y. Yamashita, T. Yamamoto, N. Sugiyama, and S. I. Takagi, "Effects of Si passivation on Ge metal-insulator-semiconductor interface properties and inversion-layer hole mobility," *Applied Physics Letters,* vol. 92, 113511, Mar 2008.

[5] N. Wu, Q. C. Zhang, C. X. Zhu, D. S. H. Chan, A. Y. Du, N. Balasubramanian, M. F. Li, A. Chin, J. K. O. Sin, and D. L. Kwong, "A TaN-HfO_2-Ge pMOSFET with novel SiH_4 surface passivation," *IEEE Electron Device Letters,* vol. 25, pp. 631-633, Sep 2004.

[6] P. Zimmerman, G. Nicholas, B. De Jaeger, B. Kaczer, A. Stesmans, L. A. Ragnarsson, D. P. Brunco, F. E. Leys, M. Caymax, G. Winderickx, K. Opsomer, M. Meuris, and M. M. Heyns, "High performance Ge pMOS devices using a Si-compatible process flow," in *IEEE International Electron Devices Meeting*, San Francisco, CA, 2006, pp. 390-393.

[7] W. P. Bai, N. Lu, A. Ritenour, M. L. Lee, D. A. Antoniadis, and D. L. Kwong, "Ge n-MOSFETs on lightly doped substrates with high-k dielectric and TaN gate," *IEEE Electron Device Letters,* vol. 27, pp. 175-178, Mar 2006.

[8] H. L. Shang, K. L. Lee, P. Kozlowski, C. D'Emic, I. Babich, E. Sikorski, M. K. Ieong, H. S. P. Wong, K. Guarini, and N. Haensch, "Self-aligned n-channel germanium MOSFETs with a thin Ge oxynitride gate dielectric and tungsten gate," *IEEE Electron Device Letters,* vol. 25, pp. 135-137, Mar 2004.

[9] N. Wu, Q. C. Zhang, N. Balasubramanian, D. S. H. Chan, and C. X. Zhu, "Characteristics of self-aligned gate-first Ge p- and n-channel MOSFETs using CVD HfO_2 gate dielectric and Si surface passivation," *IEEE Transactions on Electron Devices,* vol. 54, pp. 733-741, Apr 2007.

[10] Q. C. Zhang, J. D. Huang, N. Wu, G. X. Chen, M. H. Hong, L. K. Bera, and C. X. Zhu, "Drive-current enhancement in Ge n-channel MOSFET using laser annealing for source/drain activation," *IEEE Electron Device Letters,* vol. 27, pp. 728-730, Sep 2006.

[11] K. Martens, B. De Jaeger, R. Bonzom, J. Van Steenbergen, M. Meuris, G. Groeseneken, and H. Maes, "New interface state density extraction method applicable to peaked and

high-density distributions for Ge MOSFET development," *IEEE Electron Device Letters,* vol. 27, pp. 405-408, May 2006.

[12] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. Dekeersmaecker, "A Reliable Approach to Charge-pumping Measurements in MOS-Transistors " *IEEE Transactions on Electron Devices,* vol. 31, pp. 42-53, 1984.

[13] N. Wu, Q. C. Zhang, C. X. Zhu, C. C. Yeo, S. J. Whang, D. S. H. Chan, M. F. Li, B. J. Cho, A. Chin, D. L. Kwong, A. Y. Du, C. H. Tung, and N. Balasubramanian, "Effect of surface NH_3 anneal on the physical and electrical properties of HfO_2 films on Ge substrate," *Applied Physics Letters,* vol. 84, pp. 3741-3743, May 2004.

[14] J. Reed, Z. Fan, G. B. Gao, A. Botchkarev, and H. Morkoc, "GaAs metal-insulator-semiconductor capacitors and high transconductance metal-insulator-semiconductor field-effect transistors," *Applied Physics Letters,* vol. 64, pp. 2706-2708, May 1994.

[15] K. Martens, W. Wang, K. De Keersmaecker, G. Borghs, G. Groeseneken, and H. Maes, "Impact of weak Fermi-level pinning on the correct interpretation of III-V MOS C-V and G-V characteristics," *Microelectronic Engineering,* vol. 84, pp. 2146-2149 2007.

[16] J. R. Hauser and K. Ahmed, *"Characterization of ultrathin oxide using electrical C–V and I–V measurements," in Characterization and Metrology for ULSI Technology*: Woodbury, NY, AIP, pp.235–239, 1998.

Chapter 7

Conclusions and Recommendations

7.1. Conclusions

High-k gate stack on high mobility channel materials enables the possibility of further MOSFETs scaling into sub-22 nm regime. Ge-channel MOSFETs have the greatest potential for integration into Si CMOS technology of all the alternative semiconductor materials. This study focused on the gate stack engineering for a Ge MOSFETs with high-k gate dielectrics, specially, the Hf-based high-k gate dielectrics.

In the literature, extensive researches have been made to improve the high-k/Ge interface quality. It is commonly agreed that surface passivation process is the key step to achieve the good interface quality. Nitride based passivation, Si passivation and GeO_2 passivation have been widely reported. By using these surface passivation techniques, electrical parameters of Ge MOSFETs, such as D_{it}, gate leakage current, EOT and mobility can be improved. However, tradeoff relationships usually exist between these parameters and none of those surface passivation techniques can offer the ideal gate stack quality to date (e.g. increase the Si passivation layer thickness can increase mobility, but EOT is also increased; pure GeO_2 can offer very low D_{it} with high EOT, high-k gate dielectric with thin GeO_2 passivation layer can decrease the EOT, but D_{it} also increases).

In the first half of this thesis (chapter 2 and 3), we still focused on the surface passivation techniques for high-k/Ge gate stack. An alternative sulfur (S) passivation was firstly investigated. It was found that $(NH_4)_2S$ treatment can reduce the D_{it} and improve the electrical properties in terms of EOT and gate leakage current. Moreover, it was found that samples with $(NH_4)_2S$ treatment shows better thermal stability at high-k/Ge interface. This is due to less Ge diffusion into high-k dielectric by suppressing the germanium monoxide formation at high-k/Ge interface, which was confirmed by XPS and SIMS studies. However, large *C-V* hysteresis was observed for Ge MOS capacitors with S passivation, which maybe the intrinsic problem for S passivation that limits its application in real high performance Ge MOSFETs fabrications. Another surface passivation technique we have proposed is silicon nitride (SN) passivation. This is a modified version from Si passivation and achieved by using a SiH_4-NH_3 treatment. It is known that the Si interlayer thickness gives strong impact on device performance. The ultrathin Si layer cannot effectively suppress the Ge diffusion, which results degraded performance. Compared to ultrathin Si passivation (~6 Å), ultrathin SN passivation was demonstrated to be more effective to suppress the Ge out-diffusion into HfO_2. It improved the electrical characteristics like *C-V* frequency dispersion, gate leakage and mobility. Therefore SN passivation offers bigger process window than Si passivation and can be a promising technique for high-k/Ge gate stack. Moreover, by suppressing the interface dipole formation, SN passivation layer eliminates the positive V_{th} shift problem of Si passivation. The only drawback of SN passivation is the possible mobility degradation due to the nitrogen involvement near the channel. The pMOSFETs mobility we obtained in this study was ~2.6X Si hole universal mobility for SN passivated devices,

which is less than reported ~3X Si hole universal mobility achieved by using a relatively thicker Si layer [1].

In the second half of this thesis (chapter 4 and 5), we tried to look beyond the "pre-gate" surface passivation. In the Si based MOS device technologies, one of the most important defects at the (100)Si/SiO_2 interface, the P_{b0} centre (trivalent Si dangling bond), can be passivated very effectively after post-metallization anneals performed in a hydrogen containing ambient. However, for Ge devices, it has been pointed out that hydrogen passivation of acceptor states or dangling bonds is ineffective. Moreover, due to the lower processing temperature for Ge devices, there are significant bulk defects in high-k dielectrics, especially near high-k/Ge interface and these defects may be the cause for mobility degradation and bias temperature instability. Thus a "post-gate" treatment with lower thermal budget is proposed. In this study, we employed the post-gate CF_4 plasma treatment process to incorporated F into the high-k/Ge gate stack. By optimizing the power, gas flow rates between CF_4 and O_2, and subsequent post deposition annealing conditions, F was effectively introduced into the gate stack without any carbon byproduct deposition. The effects of F incorporation were firstly investigated on Ge MOS capacitors without any pre-gate surface passivation. Electrical characteristics such as frequency dispersion, interface state density, gate leakage current, and breakdown voltage were greatly improved. This is attributed to the Ge-F and Hf-F bonds formation at high-k/Ge interface and in the bulk HfO_2 gate dielectric, respectively. However, the D_{it} was still as high as the order of 10^{12} $cm^{-2}eV^{-1}$, suggesting that ideal interface quality can not be achieved by simple post-gate treatment alone. Therefore,

both pre-gate surface passivation and post-gate treatment were implemented for HfO_2 gate Ge MOS devices. F incorporation combined with Si passivation was studied. It was observed that interface quality was improved after Si passivation, compared to samples without any surface passivation, and even better gate stack quality was achieved of D_{it} as low as 4.85×10^{11} $cm^{-2}eV^{-1}$ without any *C-V* dispersion or hysteresis after the F incorporation. This suggested that post-gate F passivation is also compatible with pre-gate surface passivation and it can be a candidate for Ge-based MOS devices, playing a similar role as forming gas annealing in Si-based MOSFETs.

The effects of F incorporation and hydrogen annealing were further compared based on the HfO_2 gated MOS capacitors with thermal GeO_2 passivation. Here the GeO_2 passivation was used because currently it is widely believed that this native oxide layer could offer the best interface quality. Our results revealed that both F incorporation and hydrogen passivation can improve the *C-V* characteristics of Ge MOS capacitors. However, compared to H passivation, F was more effective to reduce the frequency dependent flat band voltage shift ΔV, which is a sign of high density of interface states locating in the upper half of the Ge bandgap. By combining the GeO_2 passivation and both post gate treatments, excellent electrical characteristics with negligible *C-V* stretch-out and frequency dispersion were achieved. The D_{it} of $TaN/HfO_2/GeO_2/Ge$ MOS structure was as low as 2.02×10^{11} $cm^{-2}eV^{-1}$ at the minimum with EOT ~ 1.5 nm and J_g less than 10^{-6} A/cm^2 at 1V. Knowing that this combined interface engineering scheme can provide excellent interface quality, we further made Ge pMOSFETs with scaled EOT~ 1nm (by using thinner GeO_2 passivation layer and HfO_2). Excellent performance was achieved

with drive current as high as 37.8 μA/μm at V_g-V_t=V_d=-1.2V for a 10 μm L_g devices and record high hole mobility with peak up to 396 $cm^2/V \cdot s$. This was the first report for high-k gated Ge MOSFETs with GeO_2 passivation. Variable rise/fall time charge pumping method was further applied to study the interface trap characteristics and a significant D_{it} reduction in both upper and lower half of bandgap was observed with F incorporation. This result is consistent with the observation that negligible ΔV is present in *C-V* characteristics of MOS capacitors with CF_4 plasma treatment.

In the last, we further applied this variable rise/fall time charge pumping method to study the energy distribution of interface traps for Ge MOSFETs with Si passivation. A strong dependence of charge pumping current on the fall time was observed when rise time was fixed to a constant value, suggesting a high density of interface states was present in the upper half of the Ge bandgap. As a result, the inversion-layer electron mobility of Ge n-channel MOSFETs was significantly degraded by the Coulomb scatterings. This asymmetric energy distribution of D_{it} in Ge MOSFETs was further verified by the *C-V* characteristics in Ge MOS capacitors as well as mobility extraction and simulation results. This may clarified the cause of widely reported low electron mobility of Ge nMOSFETs made using either Si passivation or nitride based passivation.

7.2 Recommendations for future work

1) Different high-k dielectrics. So far, all our studies that have been done are based on Hf-based high-k gate dielectrics. This may not be the most compatible dielectric material for Ge substrate. Recently some research groups have suggested that $LaYO_3$ or $LaAlO_3$

is more compatible with Ge than HfO_2 [2, 3]. High-k/Ge gate stack with even better interface quality might be obtained by choosing proper high-k dielectric together with proper pre-gate and post-gate treatments.

2) Ge nMOSFETs. Although high mobility Ge nMOSFETs fail to be achieved with nitride based surface passivation and Si passivation, the recent popular GeO_2 native oxide layer may fulfill the job. Especially, some groups reported that high pressure oxygen thermal oxidation [4] or ozone oxidization [5] can further improve the GeO_2/Ge interface quality. Our results also revealed that F incorporation can reduce the D_{it} in both upper and lower half of the bandgap. Thus, it is possible to realize Ge nMOSFETs with higher electron mobility than Si if D_{it} can be significantly reduced by using these alternative passivation methods.

3) Gate stack threshold voltage control and reliability. As high-k/metal gate is used for Ge MOSFETs, workfunction engineering of gate electrode and study of oxide fixed charge or interfacial dipoles are also very important. Since Ge bandgap is smaller than Si, also, the gate stack maybe more complicate than high-k/Si system, the resultant V_{th} for MOS devices also can be complex. Experiments should be done to clarify the V_{th} dependence for different high-k/metal gate combination with different passivation schemes.

Besides the electrical performance of Ge MOSFETs, the reliability characteristics such as gate oxide breakdown, bias temperature instability are also very important issues to investigate. From our preliminary study [6], we find that BTI characteristic of Ge based

devices is worse than Si. The V_{th} shift is highly depending on the passivation methods. More studies should be done to clarify the root cause of the degradation, and give guidelines on how to improve the device reliability.

References:

[1] N. Taoka, M. Harada, Y. Yamashita, T. Yamamoto, N. Sugiyama, and S. I. Takagi, "Effects of Si passivation on Ge metal-insulator-semiconductor interface properties and inversion-layer hole mobility," *Applied Physics Letters,* vol. 92, 113511, Mar 2008.

[2] Y. Kamata, A. Takashima, Y. Kamimuta, and T. Tezuka, "New approach to form EOT-scalable gate stack with strontium germanide interlayer for high-k/Ge MISFETs," in *VLSI Technology, 2009 Symposium on*, 2009, pp. 78-79.

[3] K. Kita, T. Takahashi, H. Nomura, S. Suzuki, T. Nishimura, and A. Toriumi, "Control of high-k/germanium interface properties through selection of high-k materials and suppression of GeO volatilization," *Applied Surface Science,* vol. 254, pp. 6100-6105, Nov 12-14 2008.

[4] C. H. Lee, T. Nishimura, K. Nagashio, K. Kita, and A. Toriumi, "Reaction Kinetics Control on Thermal Oxidation Process of Ge in High Pressure Oxygen," in *International Conference on Solid State Devices and Materials*, Tsukuba, JAPAN, 2008, pp. 16-17.

[5] D. Kuzum, T. Krishnamohan, A. J. Pethe, A. K. Okyay, Y. Oshima, Y. Sun, J. P. McVittie, P. A. Pianetta, P. C. McIntyre, and K. C. Saraswat, "Ge-interface engineering with ozone oxidation for low interface-state density," *IEEE Electron Device Letters,* vol. 29, pp. 328-330, Apr 2008.

[6] R. L. Xie, T. H. Phung, M. B. Yu, and C. X. Zhu, "Effective Surface Passivation by Novel SiH_4-NH_3 Treatment and BTI Characteristics on Interface-Engineered High-Mobility HfO2-Gated Ge pMOSFETs," *Ieee Transactions on Electron Devices,* vol. 57, pp. 1399-1407, Jun 2010.

Appendix

The C program for charge pumping configuration:

Charge pumping measurement requires fine tuning of the following measurement parameters: pulse frequency, pulse height, sweeping range, leading and falling edges of the pulses, integration time, number of data for averaging, etc. The transistor should also be isolated properly (by the guard ring). The following *setupCP()* is the C program to program Agilent 4155C + 41501B for charge pumping measurement.

```
/* Measurement Unit Definition:
SMU1 – Gate
SMU2 – Source
SMU3 – Drain
SMU4 – Bulk (Substrate)
VSU1– Guard ring
*/

#define V_GAURD -0.2   //Apply voltage to the guard ring for isolation (accumulation)

#define CP_POINTS 39       //Number of data points in a Icp curve
#define CP_STEP 0.05       //Step range per data
#define CP_BASE -1.5       //Pulse base
#define CP_AMPLITUDE  1.0
#define CP_PULSE (CP_BASE+CP_AMPLITUDE)

#define CP_AV 12           //Averaging data
#define CP_TW 5e-6         //Charge Pumping pulse width
#define CP_TL 1e-7         //Charge Pumping leading edge
#define CP_TT 1e-7         //Charge Pumping trailing edge
#define CP_TP 1e-5         //Charge Pumping pulse period

ViStatus setupCP()         //ChargePumping Program
{
        ViStatus ViErr;
        char cmd[1000];
        double base=CP_BASE;
        double pulse=CP_PULSE;
        int i;
```

```
ViErrChk(Write(resource415x, "ST 3\n", 10));       //store program in memory block 3
ViErrChk(Write(resource415x, "FMT 2,0\n", 10)); //output data format: ASCII without header

sprintf(cmd, "AV, %d\n", CP_AV);                    //compile a command
ViErrChk(Write(resource415x, cmd, 10));             //number of averaging data

ViErrChk(Write(resource415x, "WM 1\n", 10));   //sweep abort condition & post sweep condition
ViErrChk(Write(resource415x, "SIT 3, 1", 10));   //set integration time: long=1sec
ViErrChk(Write(resource415x, "SLI 2", 10));       //select integration time: med
ViErrChk(Write(resource415x, "MM 1,4,2,3\n", 10));  //set SPOT measurement unit: SMU4(Ib),
SMU2(Is), SMU3(Id)

ViErrChk(Write(resource415x, "SSP 0, 2\n", 10));  //select PGU input to output channel
ViErrChk(Write(resource415x, "CN 2,3,4,21,27\n", 10)); //channel enable (SMU1,2,3,4, VSU1,
PGU1)
ViErrChk(Write(resource415x, "DV 2, 0, 0,    0.01\n", 10)); //set SMU2(Vs) const voltage=0
ViErrChk(Write(resource415x, "DV 3, 0, 0,    0.01\n", 10)); //set SMU3(Vd) const voltage=0
ViErrChk(Write(resource415x, "DV 4, 0, 0,    0.01\n", 10)); //set SMU4(Vb) const voltage=0

sprintf(cmd, "DV 21, 0, %f\n", V_GAURD);      //compile a command
ViErrChk(Write(resource415x, cmd, 10));         //force VSU1, auto range, voltage=0,
compliance=0.01A
ViErrChk(Write(resource415x, "RI 3, 11\n", 10));  //set SMU3 measurement range
mode=1nA~Autorange
ViErrChk(Write(resource415x, "PT 0, 03", 10)); //hold time=0, pulse width=0.3
ViErrChk(Write(resource415x, "POR 27, 0\n", 10)); //set PGU output impedance=low

        for (i=0; i<CP_POINTS; i++){
                Fmt(cmd,"%s<SPG  27, 2, %f, %f, 0, %f[e],%f[e],%f[e],%f[e],65535\n", base,
pulse, CP_TW,CP_TL,CP_TT,CP_TP);

        ViErrChk(Write(resource415x, cmd, 10));
        ViErrChk(Write(resource415x, "SRP\n", 10));              //force pulse output
        ViErrChk(Write(resource415x, "XE\n", 10));               //trigger measurement
        ViErrChk(Write(resource415x, "SPP\n", 10));              //stop pulse output
                base+=CP_STEP;
                pulse+=CP_STEP;
        }
        ViErrChk(Write(resource415x, "SLI 1", 10));          //select integration time=short
        ViErrChk(Write(resource415x, "CL\n", 10));           //switch OFF and disable channels
        ViErrChk(Write(resource415x, "SSP 0, 1\n", 10));   //select SMU to output channel
        ViErrChk(Write(resource415x, "END\n", 10));
Error:
   return ViErr;
}
```

LIST OF PUBLICATIONS

Conferences:

1. **Ruilong Xie**, Thanh Hoa Phung, Wei He, Zhiqiang Sun, Mingbin Yu, Zhiyuan Cheng, Chunxiang Zhu, "High mobility high-k/Ge pMOSFETs with 1 nm EOT -New concept on interface engineering and interface characterization", ***International Electron Devices Meeting (IEDM) 2008***, pp. 393-396.

2. **Ruilong Xie**, Weiming Chen, Mingbin Yu, Oh Sue Ann, Tripathy, S, Chunxiang Zhu, **"**Low temperature poly-germanium growth process on insulating substrate using palladium-induced lateral crystallization", ***9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT), 2008***, pp. 792-795.

3. **(Invited Paper) Ruilong Xie** and Chunxiang Zhu, "Interface Engineering for high-k/Ge gate stack", ***9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT), 2008***, pp. 1252-1255.

4. **Ruilong Xie**, Wei He, Mingbin Yu, Chunxiang Zhu, "High-k Gated Germanium Metal-Oxide-Semiconductor Capacitors with GeO_2 Surface Passivation and Fluorine Incorporation", ***International conference on solid state devices and materials (SSDM)***, pp. 10-11, 2008.

5. **Ruilong Xie** and Chunxiang Zhu, "Effects of Sulfur Passivation on Ge MOS Capacitors with High-k Gate Dielectric", ***International conference on solid state devices and materials (SSDM)***, pp.28-29, 2007.

6. **(Invited Paper) Ruilong Xie** and Chunxiang Zhu, "Development and Characterization of High-k Gate Stack for Ge MOSFETs", ***ECS Transactions***, Vol. 19, Issue. 2, pp. 537-561, 2009.

7. **Ruilong Xie**, Nan Wu, Chen Shen, Chunxiang Zhu, "Asymmetric Energy Distribution of Interface Traps in Germanium MOSFETs with HfO_2 Gate Dielectric", ***ECS Transactions***, Vol. 16, Issue. 10, pp. 175-180, 2008.

8. **Ruilong Xie**, Zhiqiang Sun, Mingbin Yu, Meiying Lai, Lap Chan, Chunxiang Zhu, "Enhanced Performance for Ge MOS Devices with High-k Gate Dielectrics through a Novel Post-gate CF_4-plasma Treatment Process", ***ECS Transactions***, Vol. 16, Issue. 10, pp. 707-716, 2008.

Journals:

9. **Ruilong Xie**, Thanh Hoa Phung, Mingbin Yu, Chunxiang Zhu, "Effective Surface Passivation by Novel SiH_4-NH_3 Treatment and BTI Characteristics on Interface Engineered High Mobility HfO_2 Gated Ge pMOSFETs", ***IEEE Transactions on Electron Devices***, Vol. 57, Issue, 6, pp. 1399-1407, 2010.

10. **Ruilong Xie**, Thanh Hoa Phung, Wei He, Mingbin Yu, Chunxiang Zhu, "Interface-Engineered High-Mobility High-k/Ge pMOSFETs With 1-nm Equivalent Oxide Thickness", ***IEEE Transactions on Electron Devices***, Vol. 56, Issue, 6, pp. 1330-1337, 2009.

11. **Ruilong Xie**, Thanh Hoa Phung, Mingbin Yu, Sue Ann Oh, Sudhiranjan Tripathy, Chunxiang Zhu, "Palladium-Induced Lateral Crystallization of Amorphous-Germanium Thin Film on Insulating Substrate", ***Electrochemical and Solid-State Letters***, Vol. 12, Issue. 7, pp. H266-H268, 2009.

12. **Ruilong Xie**, Nan Wu, Chen Shen, Chunxiang Zhu, "Energy Distribution of Interface Traps in Germanium Metal-Oxide-Semiconductor Field Effect Transistors with HfO_2 Gate Dielectric and Its Impact on Mobility", ***Applied Physics Letters***, Vol. 93, Issue. 8, 083510, 2008.

13. **Ruilong Xie**, Wei He, Mingbin Yu, Chunxiang Zhu, "Effects of Fluorine Incorporation and Forming Gas Annealing on High-k Gated Germanium Metal-Oxide-Semiconductor with GeO_2 Surface Passivation", ***Applied Physics Letters***, Vol. 93, Issue. 7, 073504, 2008.

14. **Ruilong Xie**, Mingbin Yu, Mei Ying Lai, Lap Chan, Chunxiang Zhu, "High-*k* gate stack on germanium substrate with fluorine incorporation", ***Applied Physics Letters***, Vol. 92, Issue. 16, 163505, 2008.

15. **Ruilong Xie** and Chunxiang Zhu**, "**Effects of Sulfur Passivation on Germanium MOS Capacitors With HfON Gate Dielectric", ***IEEE Electron Device Letters***, Vol. 28, Issue. 11, pp. 976-979, 2007.

Other publications:

16. X.P. Wang, J.J. Yang, H.Y. Yu, M.-F. Li, J.D. Chen, **R.L. Xie**, C.X. Zhu, A.Y. Du, P.C. Lim, Andy Lim, Y.Y. Mi, Doreen M.Y. Lai, W.Y. Loh, S. Biesemans, G.Q. Lo, D.-L. Kwong, "Practical Solutions to Enhance EWF Tunability of Ni FUSI Gates on

HfO_2", ***International conference on solid state devices and materials (SSDM)***, pp.854-855, 2007.

17. Thanh Hoa Phung, **Ruilong Xie**, Sudhiranjan Tripathy, Mingbin Yu and Chunxiang Zhu, "Low Temperature (375°C) Metal Induced Lateral Crystallization (MILC) of $Si_{1-x}Ge_x$ ($0 \leq x \leq 1$) using Silicide/Germanide Forming Metals (Ni, Pd and Co)", ***International conference on solid state devices and materials (SSDM)***, pp.172-173, 2009.

18. Thanh Hoa Phung, **Ruilong Xie**, Sudhiranjan Tripathy, Mingbin Yu and Chunxiang Zhu, "Low Temperature Metal Induced Lateral Crystallization of Ge using Germanide Forming Metals", ***Journal of Electrochemical Society***, vol. 157, issue. 2, pp. H208-H213, 2010.

19. Thanh Hoa Phung, **Ruilong Xie**, Sudhiranjan Tripathy, Mingbin Yu and Chunxiang Zhu, "Low Temperature Metal-Induced Lateral Crystallization of $Si_{1-x}Ge_x$ Using Silicide/Germanide-Forming-Metals", ***Japanese Journal of Applied Physics***, vol. 49, issue. 4, special issue. Part 2 Sp. Iss. SI, Article number. 04DH10, 2010.