ADDRESSING PERFORMANCE BOTTLENECKS FOR TOP-DOWN ENGINEERED NANOWIRE TRANSISTORS

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Summary

The continuous advancement has allowed CMOS technology to meet the demands of higher device density, faster clock rate and lower power consumption. However, as the scaling dimensions shrink down to the sub-100 nm regime, immense physical challenges make the use of conventional scaling techniques alone insufficient. Novel one-dimensional (1D) structures such as semiconductor nanowires (NWs) are considered to be promising structures for nanoscale devices and circuits. In this thesis, several approaches have been investigated in order to address the performance bottlenecks and to further enhance the performance of semiconductor nanowire devices.

In this work, Ge rich nanowire transistors are demonstrated with metal gate/high-k gate stack. Using the pattern size dependent Ge condensation technique, lateral hetero-structure Ge nanowire transistors are found to have higher drive current compared to the conventional homo-structure planar devices. Lower backscattering ratio is obtained in this Ge rich nanowire structure.

In a cost-effective approach for SiGe nanowire integration, the SiGe core/shell nanowire devices are fabricated on bulk Si substrate. Due to the lattice mismatch between SiGe core and Si shell, the SiGe core channel is under compressive stress, which improves the hole mobility due to hole effective mass reduction. With the surface passivation effect of the Si shell, the interface between the channel and dielectric is greatly improved.

The parasitic source and drain (S/D) resistances in extremely scaled Gate-All-Around (GAA) nanowire devices can pathologically limit the device drive current performance. Superior drive current was achieved in short gate length GAA nanowire

devices by utilizing metallic nanowire contacts. The parasitic S/D extension resistance was reduced significantly by using the ultra-thin Ni silicidation technique.

It is necessary to set the transistor threshold voltages correctly for both n and pFETs for nanowire circuit integrations. Dopant segregated FUSI GAA structure was demonstrated with successful dual work function implementation, achieving symmetrical threshold voltages (±0.3V). Good inverter transfer characteristics and relatively low ring oscillator delay are observed.

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List of Symbols

Symbol	Description	Unit
C	Capacitance	$fF/\mu m^2$
C_{ox}	Capacitance of gate oxide	$fF/\mu m^2$
E_c	Si conduction band-edge	eV
E_F	Fermi-level energy	eV
$E_{F,\ n+\ poly}$	Fermi-level energy of n+ poly-Si gate	eV
$E_{F,\ Si\text{-}sub}$	Fermi-level energy of Si substrate	eV
E_{Fi}	Intrinsic Si Fermi-level energy	eV
E_v	Si valence band-edge	eV
E_{vac}	Vacuum level	eV
G_m	Transconductance	S
I_{DS}	Drain current (per unit width)	A/μm
I_{Dsat}	Drain saturation current (per unit width)	A/μm
I_{off}	Off state current (per unit width)	A/μm
I_{on}	On state current (per unit width)	A/μm
I_D	Transistor drive current	A
μ_{eff}	Effective mobility	$cm^2/V\text{-}s$
N_A	Substrate doping concentration atoms	$/cm^3$
t_d	Circuit delay	s
V_{FB}	Flatband voltage	V
V_{DS}	Drain voltage	V
V_{GS}	Gate voltage	V
V_{DD}	Supply Voltage	V
V_T	Threshold voltage (Extracted at maximum transconductance)	V
$V_{T,lin}$	Linear threshold voltage (Extracted in linear regime at low V_{DS})	V
$V_{T,sat}$	Saturation threshold voltage (Extracted in saturation regime at high V_{DS})	V
Lg	Gate length	nm
J	Gate current density	A/cm^2
Q_f	Oxide fixed charge density	cm^{-2}
Q_d	Depletion layer charge in channel region	C/cm^2
N_d	Doping concentration	cm^{-2}
q	Electronic charge	C
T_{ox}	Equivalent oxide thickness	nm
W	Transistor gate width	μm
ε_{Si}	Permittivity of silicon	F/cm^2
ε_{SiO2}	Permittivity of silicon oxide	F/cm^2

Φ_{Si}	Work function of Si substrate	eV
Φ_{m}	Work function of metal gate	eV

List of Abbreviations

AFM	atomic force microscopy
ALCVD	atomic-layer chemical vapor deposition
ALD	atomic-layer deposition
BOX	buried oxide
BTI	bias-temperature-instability
CMOS	complimentary metal-oxide-semiconductor
CVD	chemical vapour deposition
CET	capacitance equivalent thickness
C-V	capacitance-voltage
CVS	constant-voltage scaling constant-voltage stress
CD	critical dimensions
DIBL	drain induced barrier lowering
DG	double-gate
DHF	diluted hydrofluoric (acid)
DIBL	drain-induced barrier lowering
EDX	energy dispersive X-ray
EELS	electron energy loss spectroscopy
EOT	equivalent oxide thickness
EWF	effective work function
ESL	etch-stop-layer
FFT	fast fourier transform
FUSI	fully-silicided (metal gate)
F-N	fowler-nordheim (tunnelling)
FGA	forming-gas annealing
GAA	gate-all-around
GIDL	gate-induced-drain leakage
HK	high-κ (dielectric)
HM	hard-mask
HP	high-performance
HRTEM	high-resolution transmission electron microscopy
ITRS	international technology roadmap for semiconductors
IC	integrated circuits
I-V	current-voltage
LSTP	low-standby-power
LPCVD	low pressure chemical vapour deposition
MEMS	Micro-Electro-Mechanical Systems
MG	metal gate
MOCVD	metal-organic chemical vapor deposition
MOSFET	metal-oxide-semiconductor field effect transistor
NW	nanowire
PDA	post-deposition-annealing
PMA	post-metal-annealing
PMD	post-metal-dielectric
PR	photoresist
PVD	physical vapor deposition
PECVD	plasma enhanced chemical vapour deposition
RTA	rapid thermal annealing

RF	radio-frequency
RTA	rapid thermal annealing
RIE	reactive ion etching
SBH	schottky barrier height
SC-1	standard cleaning-1 ($NH_4OH+H_2O_2+H_2O$) solution
S/D	source/drain
SIIS	silicidation induced impurity segregation
SS	subthreshold swing
SSDOI	strained-Si directly on insulator
SSOI	strained-Si on insulator
STI	shallow trench isolation
SCE	short channel effects
S/D	source / drain
SDE	source drain extension
SEM	scanning electron microscopy
SOI	silicon-on-insulator
STI	shallow trench isolation
SGNW	SiGe nanowire
TCAD	technology computer aided design
TEM	transmission electron microscopy
UHV	ultra high vacuum
UTB	ultra thin body
UTBSOI	ultra-thin-body silicon-on-insulator
UV	ultraviolet
WF	work function
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
XTEM	cross-sectional transmission electron microscope

CHAPTER 1

1. INTRODUCTION

1.1 Overview for CMOS Scaling

Since the transistor's invention in the early 1960s [1, 2], silicon (Si)-based microelectronic devices have been widely used in every aspect of our daily life. Driven by the demand of high speed, power and density, researchers have put much effort into CMOS device performance scaling. The behavior of CMOS device technology scaling follows the well-known Moore's law, which predicts that the number of transistors per integrated circuit would double approximately every ~ 18 months.

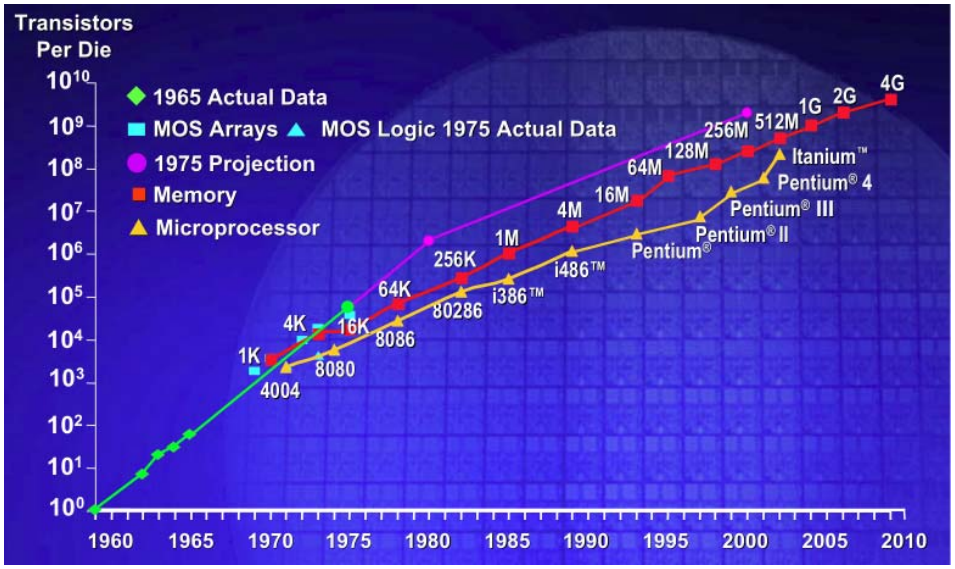


Fig. 1.1: Moore's law for memory chips and microprocessors plotted on a semi-logarithmic scale, the uppermost curve is the Moore projection based on data up to 1975 at Intel Corporation.

In order to meet the International Technology Roadmap for Semiconductors (ITRS) requirements for each technology node, traditional CMOS development during

the past decades revolves around the size reduction of transistors, and is commonly termed “scaling”. The conventional path of scaling is characterized by the adjustment of key parameters of the transistor with each technology node, such as reducing the gate dielectric thickness, reducing the gate length, and increasing the channel doping [3-8]. One of the most important purposes for the scaling is to reduce the transistor switching time [9]. With the continuous scaling of CMOS technology, the planar Si-CMOS devices encounter more and more challenges in fulfilling the ITRS road map and to keep in step with Moore’s law. Moreover, major issues have arisen which limit the Si-CMOS transistor’s potential for continued scaling.

In this chapter, various ways to improve the transistor switching speed, and to maintain the desired transistor performance, will be discussed in general, followed by a brief overview of the objectives and organization of the thesis.

1.2 Why Nanowire Transistors?

The scaling activities have continued since the invention of the Field Effect Transistor (FET). Since the early years, there have not been major changes in the physical structure, which is still planar, and with a SiO_2 gate dielectric. The scaling is focused on the reduction in both channel length and gate dielectric thickness. However, the planar device architecture with conventional materials is now gradually approaching its physical limitations. As the gate length and gate dielectric thickness have been reduced, the use of poly-silicon as the gate material results in an increasingly pronounced poly depletion effect [10-14]. There is also dopant penetration from the gate [15-21], which degrades the gate electrostatic control over the channel and increases the gate dielectric leakage. Furthermore, the channel mobility is reduced due to high vertical electric field as a result of thinner gate dielectric thickness [22, 23]. Moreover, as the gate leakage increases, the

power consumption of the transistor increases dramatically [24, 25]. These issues result in a trade-off between the transistor's performance and the scaling requirement, which defeats the main purpose of scaling. Thus, innovative device structures or novel materials are required to address these problems.

1.2.1 Innovation on Architecture and Material

During the past few decades, many engineers have put great effort in the scaling of the transistor and it has been observed that there are several device architectures which can help to improve MOSFET performance. Besides the conventional planar bulk metal-oxide semiconductor field effect transistor (MOSFET), there are also fully depleted silicon-on-insulator (FD-SOI) MOSFET [26-33], and multiple gate transistors [e.g., fin field effect transistor structures (Fin-FET)] [34-45]. The ITRS is entering a new era as the industry begins to address the theoretical limits of CMOS scaling. Basically, they are divided into two categories: novel material exploration and novel structural inventions to replace the conventional planar transistors.

Using high-permittivity (κ) dielectrics to replace SiO_2 or SiON on the Si-based transistors would be a potential solution for further scaling of the gate stack in the MOSFET [46-54]. The advantage of high-k material as gate dielectric is that it can greatly improve the gate leakage problems over the SiO_2 dielectric for thin EOT conditions. Many high-k materials have been investigated, amongst which Hf-based ones have shown great potential.

The incorporation of strain engineering in the Si-based channel has greatly enhanced the channel mobility. There are two methods to introduce stain into the channel of MOSFET. One approach is utilizing process induced strain technologies [55-60], which is also termed local strain methodology, to enhance the channel mobility. This

involves using ways to introduce local strain into the channel using process techniques such as Si_3N_4 stress liners [61, 62], embedded source/drain (S/D) stressors [63-66], S/D silicidation induced strain [67], strain induced by the formation of shallow trench isolation (STI) [68, 69]and so on. Another approach is to use global strain techniques. The channel is directly formed on the strained film such as strained SiGe on relaxed Si substrate [70], strained-Si on insulator (SSOI) [71, 72]. The presence of strain will alter the conduction or valence band structure, reducing the effective mass of carriers, thus enhancing the channel mobility. Introducing higher carrier mobility materials such as Ge, III-V has also significantly improved transistor performance [73, 74]. By utilizing thin SOI substrates, the parasitic capacitance has been shown to reduce dramatically, further improving the speed of the transistors.

The invention and utilization of novel device structures have been shown to improve transistor performance. The multiple gate transistor exhibits better gate electrostatic control over conventional planar transistors, which revolutionizes the current CMOS technologies. Examples of multiple gate transistors include double gated FinFET, π-gated, and Ω-gated FETs. In the tri-gate structure, gate coupling is greatly improved by its special geometry, so as to reduce short channel effects. The multiple gate structure takes advantage of the thin body effect (like UTBSOI) as well as the improvement in gate electrostatic control due to gate geometry. The Gate-All-Around (GAA) structure with an ultra narrow nanowire channel body represents the ultimate multiple gate structure for obtain excellent short channel immunity and a large drive current [75]. This satisfies the ITRS requirement as shown in Fig. 1.2.

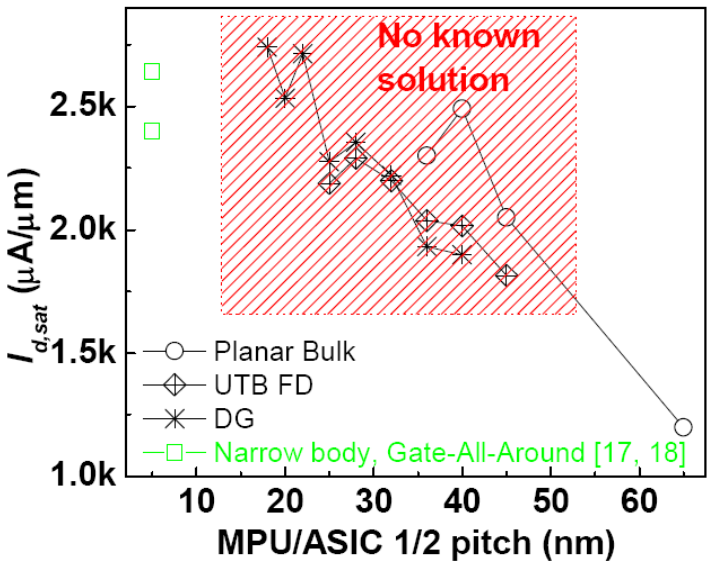


Fig. 1.2: 2006 The ITRS 2006 N-MOSFET $I_{d,sat}$ requirements for various MOSFET structures.

1.2.2 GAA Nanowire FETs

Fig. 1.3 illustrates the device structure evolution history, from the conventional bulk Si with top gate, followed by the tri-gate structure for better gate controllability and subsequently, fully depleted narrow nanowire channel with gate-all-around structure for even better gate control and suppression of short channel effects. This GAA structure shows great potential for the continued scaling of CMOS transistor performance.

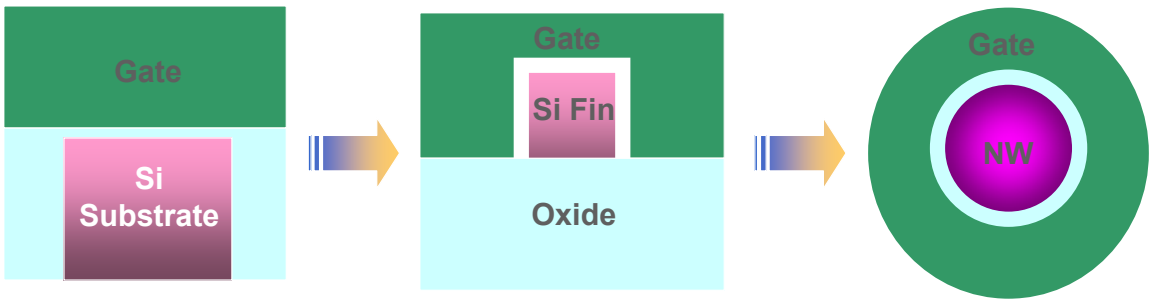


Fig. 1.3: Schematics of devices structure evolution from conventional planar transistors to the tri-gate structure and then the GAA nanowire structure.

Nanowire Field Effect Transistors (FET) have been fabricated by several different approaches. It can be divided into two major approaches: top-down approaches [75] and bottom-up approaches [76] which will be discussed in detail in the following chapter. From the process integration point of view, the top-down approach for the nanowire transistors fabrication is compatible with conventional CMOS processes, allowing for eventual nanowire circuit implementation. Superior short channel control with SS~60mV/dec and DIBL<20 mV/V were obtained for such top-down GAA Si NW transistors. The NW devices exhibited I_{on}-I_{off} ratios larger than 10^5. The excellent device characteristics clearly indicate high potential for further CMOS scaling. However, although GAA NW FETs have several advantages compared to conventional planar FETs [7], there are several challenges in obtaining optimum performance from NW FETs. With the scaling of the GAA NW FETs, large series resistances due to the narrow nanowire S/D regions will limit the drive current performance for the ultra scaled nanowire FETs; the intrinsic nanowire channel body relies on correct work function of the gate stack for circuit implementations; higher mobility material is also desirable in order to improve the PMOS performance, and so on. It is indeed necessary to develop corresponding techniques to address these issues.

1.3 Objectives and Scope

As listed below, there are challenges in fabricating high performance nanowire transistors. The details of these challenges will be presented in Chapter 2.

(1) Low hole mobility for Si channel, limited reports on high mobility materials such as Ge or SiGe.

(2) Higher S/D series resistance, which limits NW transistor performance.

(3) Incorrect V_T value due to the intrinsic channel doping.

(4) Novel structural innovations to increase the current density.

The project aims to explore possible ways of eliminating the performance bottlenecks for top-down engineering nanowire transistors. This will be achieved in several sections as follows:

(1) Channel engineering exploration: utilization of high carrier mobility materials such as Ge/SiGe integrated on nanowire pFETs for high performance transistors applications.

(2) Novel low-cost SiGe nanowire-like transistors integrated on the bulk Si substrates will also be investigated.

(3) Source/Drain engineering exploration: utilization of metallic nanowire contact technology such as NiSi nanowire contacts integrated on ultra scaled nanowire nFETs will be investigated in order to achieve low series resistance.

(4) Gate stack threshold voltage (V_T) engineering exploration: utilization of FUSI gate electrodes such as a NiSi GAA FUSI structure will be explored in order to achieve dual gate work function CMOS nanowire circuits for LSTP applications.

The work carried out for this thesis is based on top-down engineering approaches. Bottom-up NW transistors will not be discussed in this thesis. Although some of the methodology is similar to that in other structures such as planar or FinFET devices, this work is mainly focused on the fabrication, characterization and discussion of nanowire transistors.

In the following chapter, a detailed literature review of the current reports on nanowire transistors will be presented. Some of the key issues of nanowire transistor engineering will also be discussed in detail.

1.4 Thesis Organization

The organization of the thesis is divided in the following chapters.

Chapter 2 gives a detailed literature review on nanowire formation and nanowire FET fabrication. It also reviews issues pertaining to the development of the nanowire transistors, highlighting the motivations behind this work. It covers the fabrication approaches of the nanowires which consists of bottom-up and top-down methods. This is followed by the discussion of the transistor technology development for the two kinds of approaches. In order to achieve high performance nanowire transistors, some issues which limit the performance of the nanowire transistors are identified. All the issues will be investigated and elaborated upon in the following chapters.

Chapter 3 discusses in detail the channel engineering exploratory work. It covers the investigations on the Ge rich (70%) nanowire transistors with HfO_2/TaN gate stack. In this chapter, the epitaxy of Ge film at low temperature will also be investigated; the SiGe film stress will be discussed for channel strain engineering. The backscattering characteristics of such devices will be included.

Chapter 4 continues the channel engineering exploratory work. It mainly focuses on the cost-effective SiGe/Si core/shell nanowire transistors integrated on bulk Si substrates. Both approaches in Chapter 3 and 4 are designed to improve the p-FET performance by taking advantage of the high carrier mobility of Ge.

Chapter 5 focuses on the S/D engineering techniques. In this chapter, ultra thin NiSi formation process will be discussed together with material characterization and analysis. For nanowire S/D engineering, the dopant profile and its impact on transistor performance will also be investigated. Extremely scaled nanowire transistors with 10 nm nanowire channels with 8 nm gates have been fabricated. The series resistance is greatly reduced by the thin NiSi metallic nanowire contacts on the source/drain extension regions.

Chapter 6 is about threshold voltage engineering in nanowire FETs. In order to obtain the desirable threshold voltage for the FETs with intrinsic nanowire channels, FUSI Gate-All-Around nanowire CMOS transistors are fabricated with dual gate work functions. With the correct threshold voltage, the nanowire circuit can be realized. In this chapter, the characteristics of the nanowire inverter and nanowire ring oscillator will also be presented.

Chapter 7 summarizes the major results and findings. It also offers some suggestions on future research based on the results of this thesis.

CHAPTER 2

2. LITERATURE REVIEW

2.1 Introduction

Nanowire FETs have attracted the attention of many researchers due to their inherently better electrostatic control and enhanced carrier transport properties. The Gate-All-Around structure is able to retain the charge-based FET structure while improving gate control and suppressing short-channel effects. As for the nanowire FETs, carrier transport becomes one dimensional due to its small channel volume. As the channel can be intrinsically doped, the columbic scattering effect is reduced compared to the planar transistor. The carrier transport in the nanowire transistor is nearly ballistic for ultra short gate length or in ideal case, which gives significantly higher carrier mobility. As the volume becomes small, quantum effects can be observed in nanowire transistors. At room and intermediate temperature nanowires show a field effect, while at low temperatures, current oscillations due to coulomb blockade dominate transport [77-82]. The GAA nanowire structure is a potential candidate for taking CMOS electronics to the end-of-the-Si-roadmap by scaling of the gate length along with the nanowire diameter.

In this chapter, various ways of nanowire synthesis will be presented in detail. This has been divided into two categories. After the discussion of the nanowire formation, the nanowire-based transistors will be discussed separately according to the different nanowire formation approaches. The development of nanowire (NW) FETs will be discussed together with the nanowire technology evolution. Finally, the technology issues will also be summarized.

2.2 Nanowire Synthesis

The nanowire transistor is a highly promising candidate for forming ultra scaled high performance transistors. However, unlike the conventional planar transistor channel, it is not as easy to form a nanowire transistor. Currently, there are various methods that have been developed to fabricate the nanowires. These can be grouped into two categories: bottom-up and top-down approaches.

2.2.1 Bottom-up Method

There is a variety of bottom-up methods for nanowire synthesis. In the bottom-up approaches, the nanowires are synthesized mainly using template-directed synthesis [83-86], growth from vapor phase [87-90], and self-assembly methods [91, 92]. These nanowires are then assembled to make devices or circuits on other substrates using unconventional (and non-CMOS compatible) alignment/placement techniques such as electric- [93]or magnetic-fields [94-96], fluid flow [97], AFM tips [98], and SNAP (Superlattice nanowire pattern transfer, e.g., via GaAs/AlGaAs and Pt-templates) [99, 100]. Currently some well developed nanowire growth mechanisms have been widely used for nanowire synthesis such as vapor-liquid-solid (VLS), solid-liquid-solid (SLS), supercritical fluid-liquid-solid (SFLS), supercritical fluid-solid-solid (SFSS), oxide assisted growth (OAG), electrochemical deposition and so on.

VLS growth mechanism was first reported by Wagner and Ellis in 1964. The VLS method is a catalyst-assisted growth process which uses metal nanoclusters or nanoparticles as a catalyst of seeds for the nanowire growth [101]. The size of the grown nanowire is controlled by the size of the starting nanoclusters or nanoparticles. Au is one of the most popular catalysts for the nanowire growth by VLS method. It has four main process stages during nanowire growth: (a) catalyst initiates alloying (b) liquid alloy (c)

nucleation/supersaturation (d) nanowire elongation. VLS method is likely to be the most extensively explored approach to form the single crystal nanowires.

In 1997, J. Westwater reported that the size and position of the Si nanowire grown by VLS method can be controlled by the condensation of Au and temperature, [102], and the diameter of the nanowire was controlled by the dose of Au. In the following year, Si nanowires down to 10 nm were successfully synthesized via the VLS method [103]. It has been reported that the width and morphology of the nanowire can be tuned through pressure and temperature. Au was deposited on the (100) Si substrate at room temperature and silane was used as a Si source in this method. At high temperature and low pressure, the grown Si nanowire is in the direction of <111>. This position and diameter controllable VLS method makes nanowire circuit integration more possible.

Wang et al. reported the synthesis of the Si nanowires by laser ablation. It was found that the Si oxide is more effective for Si nanowire formation then metal catalyst. A bulk Si quality nanowire with uniform size has been successfully formed [87]. Hwang et al. demonstrated the growth of the Si nanowire by a chemical vapor deposition method. By utilizing a gas mixture of SiH_4, HCl, H_2, at a temperature of 1223K, high quality Si nanowires were formed on Si, SiO_2, and Si_3N_4 substrate. As the filament temperature increased, the anisotropic growth of Si nanowire degrades due to high anisotropic charged Si clusters [104].

Cui et al. reported the formation of boron-doped and phosphorus doped silicon nanowires by the VLS method. It was observed that the doped nanowires behaved like ohmic contacts, and as the doping increased, the current increased [105]. The diode structures which consist of P-N type nanowires exhibited the same behavior as planar devices. Active bipolar transistors were also reported with the emitter current gain as high as 16.

In 2006, Banerjee et al. synthesized twin GaAs nanowires down to 10-40 nm by VLS methods [106]. The twin GaAs nanowires have been grown on (001) Si substrate in a MOCVD chamber. The structure of the grown GaAs nanowire is zinc-blende diamond cubic structure with the growth axis parallel to <111>. The nanowires tend to group together so as to form the hexagonal wurtzite structure.

Though the bottom-up approach has the potential of growing and integrating nanowires of different materials, fabricating nanowire superlattice [107], the technology to assemble the individual nanowires for actual device/circuit function is complicated. It thus appears to be far from being ready for manufacturing in the near future. Self-assembly inside lithographically defined patterns, however, can avoid the post growth placement issues. However, good device performance from these nanowires has yet to be demonstrated.

2.2.2 Top-down Method

In the top-down scheme, the patterns on the wafer are defined using a lithography process, transferred onto Si by etch and converted into nanowires mainly by self retarded oxidation [108-110], electrochemical size reduction [111-113] or wet trimming. Spacer lithography method has also been used to define nanowires [114-115]. Apart from the spacer technique, a recessed hard mask and trenching method has been documented by Suk et al. [116, 117]. Besides the above mentioned top-down methods, Eliboi et al. utilized a confined lateral selective epitaxial growth (CLSEG) method to fabricate Si nanowires down to ~40 nm in diameter [118]. Diffraction mask projection excimer laser ablation [119, 120] has also been used under this category to fabricate GaN nanowires. The top-down lithographic approach appears more realistic than the assembling of pre-grown nanowires as most of the involved fabrication steps are suitable for manufacturing and CMOS-compatible in materials, equipment, and processes. These “top-down”

approaches exhibited better control and reproducibility of the nanowires, indicating high potential for CMOS integration. Detailed reviews on various methods of "top-down" nanowire formation are presented as follows.

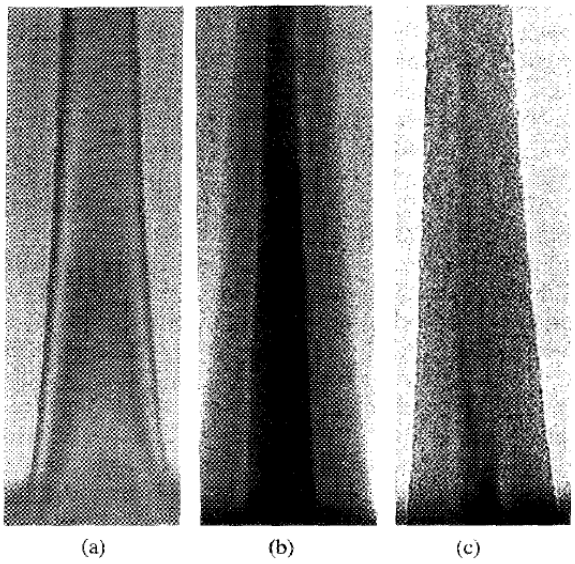


Fig. 2.1: TEM Micrographs of the bottom nonuniform portions of Si nano-columns going through (a) 0h, (b) 8h, and (c) 16h of dry oxidation at 850 º C. Enhanced oxidation rate near the bottom region where the diameter are larger is clearly evident [108].

The self-limiting oxidation method to form Si nanowires was first report by H.I. Liu in 1993. It has been reported that sub 10 nm nanowires were achieved with a tolerances of ±1 nm by the self-limiting oxidation method. In addition, it was also observed that the final size of the nanowire has a strong relationship with the oxidation temperature. Under dry oxidation of 800ºC and 850ºC, the final diameters of the nanowire are 11 nm and 6 nm. As the temperature increases, the final size of the nanowire shrinks. Fig. 2.1 shows the TEM images with different oxidation times. The self-limiting effect will disappear with even higher temperatures [108]. Later Liu also reported that the self-liming process will still be present as long as the temperature is below 950ºC. A 5 nm process controllable Si nanowire has been demonstrated and 2 nm Si nanowires with more than 100 to 1 aspect ratios have been reported. The possible reason for the self-

limiting process is due to highly stressed oxide, as a result of limited viscous flow at oxidation temperatures below 950ºC, slowing the oxidation rate of the remaining Si [109].

Prins, F. E investigated the thermal oxidation behavior of Si dots in 1999. Si dots sizes with 60 nm – 10 nm have been studied at 850ºC with different oxidation time. It further confirmed the self-limiting oxidation effect by observations that the oxidation rate decreases on the smaller structures of Si dots. It has been reported that the aspect ratio will change the shape of Si dots on the curved surface compared to the planar surface [121].

A CMOS compatible technique for silicon nanowire fabrication has been reported by Agarwal [122] et al in 2006. The silicon nanowires were formed by the combination of reactive ion etching and self-limiting oxidation process. The concept of modifying the cross sectional nanowire shape was also proposed. It has been observed that the height of the etched silicon fins determine the final number of nanowires formed (single nanowire or double nanowires). By using a high temperature annealing process, the triangular shaped nanowire can be converted to a circular shape. This top-down method can be used to realize the nanowire transistors, biosensors and in MEMS applications.

N. Singh et al. successfully fabricated nanowires with diameter down to 3 nm by this self-limiting oxidation methodology [75, 123]. The fabricated silicon nanowire is single crystalline as indicated in Fig. 2.2

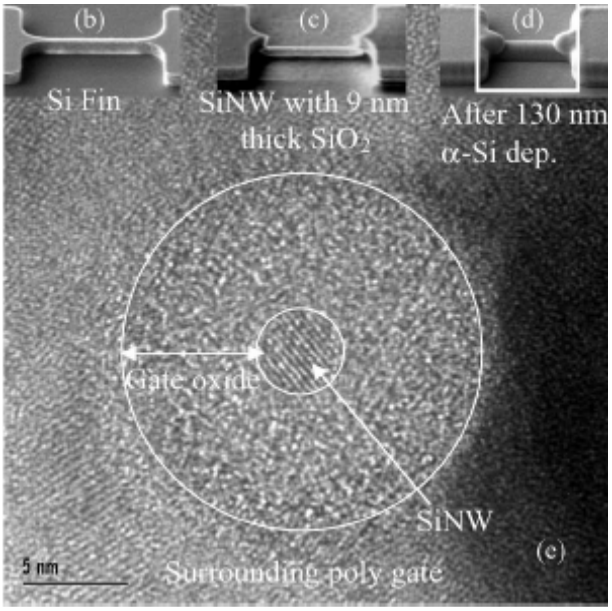


Fig. 2.2: (b) Tilt view SEM image of 1000-nm-long Si fins after top silicon etch processes. (c) SiNW after SiO_2 deposition. (d) SiNW after gate oxide and 130-nm α-Si deposition. (e) TEM image cross section of nanowire with a circular 4-nm-thick wire 9-nm oxide with full coverage by α-Si from all the sides. [123]

Kedzierski et al. reported the fabrication of horizontal single crystal Si nanowires down to 8 nm by the process combinations of fine line definition by lithography, metal lift-off process followed by plasma etch of Si [124]. By the low temperature self-limiting oxidation processes, sub 10 nm Si nanowires have been fabricated. It has been observed that shape of the nanowires would be non-circular. This is due to the different oxidation rate by different orientations.

Ra et al. reported another top-down approach for the sub 10 nm size nanowire formation. Two kinds of materials with different etching properties are needed for this lithography based nanowire formation. By selectively removing the sacrificial material while retaining the side wall spacers, nano-size patterned lines can be formed. In addition, the line width is no longer depended on the limitation of the lithography. Instead, it depends on the deposition thickness of the non-sacrificial material and final sidewall thickness [115].

2.3 Nanowire FETs

Si nanowire transistors provide many advantages compared to the conventional planar transistors. It has superior channel control due to the ultra narrow channel body. The nanowire channel exhibits fully depleted behavior which maintains a low off state current as the gate length is scaled down. Both kinds of approaches have been used to successfully demonstrate the nanowire-based transistors and have indicated better performance compared to other novel structures. The details will be discussed in the subsequent section.

2.3.1 Bottom-up Nanowire FETs

Cui et al. reported high performance nanowire transistors via bottom-up approaches [105]. By the successful control of p and n type doping, single crystal nanowire transistors were fabricated, which represents powerful building blocks for high performance nanoelectronics devices. Contacts, thermal annealing and surface passivation effects were investigated in this work. The results show that by introducing thermal annealing to passivate the oxide defects, the transconductance improved. Compared to state-of-the-art planar silicon devices, this novel nanowire field effect transistor shows substantial performance enhancement.

Si nanowire transistors down to 20 nm were fabricated with back gate structures by bottom-up approach [125]. Large on state current was obtained (10μA at V_D=1V) with gate length of 2 μm. High series resistance was observed with a measured value of 50kΩμm. The devices exhibited high ON/OFF ratio (>10^4). The measured mobility was comparable to that of planar Si transistors.

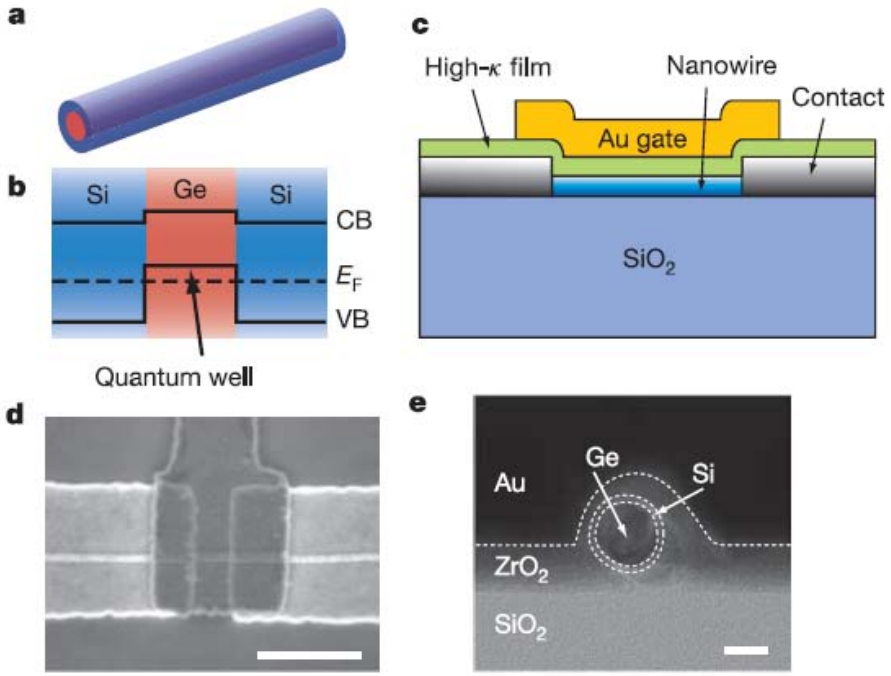


Fig. 2.3: (a) Schematic of a Ge/Si core/shell nanowire. (b) Cross-sectional diagram. (c) Schematic of the NWFET device with high-k dielectric layer and Au top gate. (d) Top-view SEM image of a typical device. The Au top gate overlaps with the Ni source/drain electrodes to ensure full coverage of the channel. (e) Cross-sectional TEM image of a device prepared using 7 nm ZrO_2 dielectric. Scale bar, 10 nm [127].

N and p type Ge nanowires are fabricated separately by VLS methods with Au as a catalyst. Ge field effect transistors were fabricated using this bottom-up method. Ge nanowire transistors exhibited high performance with on state current of 850 μA/μm and transconductance of 4.9μA/V [126]. Xiang et al. reported on novel Ge/Si heterostructures for high performance applications. Due to the valence band difference between Ge and Si material (Fig, 2.3), a quantum-well is formed in the Ge nanowire. The Ge/Si nanowire FETs were fabricated using a high-k film as the gate dielectric with an Au top gate. Superior on state current was obtained at 2.1mA/μm which is almost three or four times that of the conventional transistor [127].

One of the advantages of the bottom-up approach is that it is easy to form III-V nanowires by VLS method. It has been reported that n-InAs nanowire FETs have been fabricated and the DC characteristics have been investigated in detail. In that report,

transistors with dielectric thicknesses from 20 nm 90 nm were studied with the gate length changing from 1μm to 5μm. InAs nanowire FETs exhibited excellent drive current performance with a transconductance of up to 2 S/mm at room temperature. Good agreement was observed between the experimental results and modeling data [98].

Although there are some reports showing the excellent performance of bottom-up nanowire FETs, the bottom-up approach still has many unresolved issues such as the lack of arbitrary arrangement of nanowires, the control of the doping, the nanowire contact properties, the repeatability of the process and so on. Such problems make it very challenging for the nanowire circuit implementations using the bottom-up approach. A reproducible and CMOS compatible method is yet to be developed for NW circuit applications. On the other hand, NW FETs fabricated using top-down approaches with CMOS compatible process can meet such requirements. In the next section, a detailed review of the current top-down nanowire transistors will be discussed.

2.3.1 Top-down Nanowire FETs

With CMOS photolithography and self-limiting oxidation control, nanowire formation using such a top-down approach is appropriate for nanowire transistor and circuit implementations. In 2006, Navab et al. demonstrated ultra narrow p and n Gate-All-Around (GAA) Si nanowire transistors with diameters down to 5 nm [75]. It is a fully CMOS compatible process, with self-limiting oxidation process being utilized for nanowire formation. The I_{on} values were ~ 2400 μA/μm for the NMOS and ~ 1300 μA/μm for the PMOS, measured at V_D=1.2V. In addition, excellent SS ~ 60 mV/decade and DIBL ~ 6 mV/V were achieved, which indicates a better short channel immunity than conventional transistors. The nanowire transistors with nanowire channel in different crystal orientations were also investigated. Low temperature characterizations were performed down to 5K. Strong evidence of carrier confinement was observed in terms of

I_D-V_G oscillations and a shift in threshold voltage with Si NW diameter reduction. By utilizing the self-limiting oxidation process for nanowire formation, the size of the nanowire is easily controlled. Moreover, with this GAA gate structure, the gate electrostatic control was improved significantly, which makes the Si nanowire GAA transistors even more promising as the scaling of the CMOS transistors continues. However, since this demonstration was with a relatively larger gate length (L_G~350 nm), investigation for the ultra short channel operation (sub 100 nm) needs to be conducted. Furthermore, the devices had large micron-sized source/drain (S/D) pads with a thickness of ~120 nm in order to reduce the series resistance, which is undesirable for dense circuit integration. All the devices were fabricated on SOI substrates, which is costly. The cost issue is also a drawback for this top-down approach. In addition, the fabricated SiNWs with diameter down to 5 nm shows coulomb blockade oscillations at room temperature conditions [124, 128].

Theng, A.L. et al. reported a dual nanowire fabrication platform built on SOI substrate. The self-limiting oxidation technique was used for the nanowire formations. TaN metal gate was integrated on these dual nanowire structures. The dual nanowire devices exhibit excellent transfer characteristics with subthreshold slope of 65mV/dec and DIBL of 25mV/V [129]. This dual nanowire technique is able to boost the current density (footprint) without degrading the short channel effects.

In 2005, twin SiNW MOSFETs (TSNWFET) with diameters down to sub-10 nm were demonstrated on bulk Si substrates by Samsung Electronics. The gate length was scaled down to 30 nm. Superior drive current was obtained in their transistors, 2640 μA/μm and 1100 μA/μm for N and P FETs respectively, without short channel degradation. The hot carrier lifetime was studied and low gate induced leakage were achieved. In the following year, TiN gate TSNWFETs with even smaller gate lengths

down to 15 nm were demonstrated. The nanowire diameter was down to 4 nm, the calculated gate delay was within the ITRS requirements [104, 117]. This SiNW fabrication scheme is based on the bulk Si substrate so that the cost has been greatly reduced for the nanowire fabrication. However, using metal gate involves a complicated process for the metal gate formation step even for traditional planar transistors. Adopting such a scheme for the GAA NW structure would be even more challenging. A cost effective and less complex fabrication scheme is still desirable for NW transistor development. Besides, the large S/D pads are directly connected to the channel region, which takes up a larger footprint and limits the density of NW circuits formed using such transistors.

By utilizing S/D stressors, the performance of the nanowire transistors can be further enhanced. In 2007, Li, M et al. from Samsung Electronics reported a strained Si nanowire PMOSFETs with embedded SiGe (e-SG) source/drain stressors. An 85% enhancement was obtained from compressive stress induced by e-SG for PMOSFETs, and 80% improvement was achieved by using <110> orientation wafers [130].

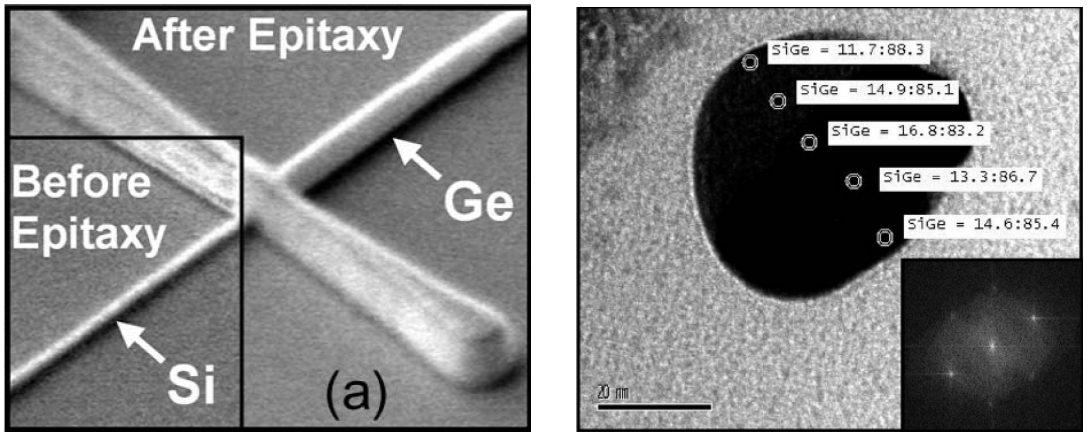


Fig. 2.4: (L) SEM images depicting a nanowire FET before and after Ge epitaxy to form the raised Ge S/D regions. (R) Cross-sectional TEM of MeltED Ge nanowire S/D regions [131].

Liow et al. reported on a pure germanium source/drain stressors technique to improve the PMOS nanowire transistors performances (Fig. 2.4). The smallest gate length achieved was 5 nm [132]. A laser-free Melt-Enhanced Dopant (MeltED) diffusion and Activation Technique was also used to form the Ge S/D stressors in the S/D regions of the NW-FETs which improved the drive current by ~125% [131, 133]. It was also observed that by using this MeltED technique, uniform dopant diffusion and incorporation can be achieved regardless of Ge thickness or S/D geometries.

SiGe nanowires FETs with high quality SiGe alloy nanowire channels have also been reported. Metal contacts were used as electrodes. Ge nanowires with different Ge concentrations (5%, 15%, 30%) were fabricated. SiGe (Ge~30%) shows high I_{on}/I_{off} ratios [134]. In the same year, the Institute of Microelectronics successfully integrated stacked arrays of SiGe nanowires with GAA structures. The transistors with the stacked SiGe nanowire arrays exhibited excellent SS~70 mV/dec, high I_{on}/I_{off} ratio and low leakage current properties [135]. Later on, both p and n SiGe nanowire FETs were demonstrated with high performance characteristics [136].

Tezuka et al. reported strained SiNW N-MOSFET and SiGe pMOSFETs fabricated on strained SOI substrate. Ge concentration of up to 70% was obtained in nanowires which were nearly cylindrical in shape. Effective mobility measurement revealed a 1.9 times enhancement for NMOSFET while a 1.6 times improvement was obtained for PMOSFET, when compared to unstrained SiNW MOSFETs [137].

Vertical silicon nanowires with GAA structure fabricated on bulk Si substrate with CMOS compatible process techniques have been reported [138]. Silicon pillars with high aspect ratio (up to 50:1) and diameter down to 20 nm were achieved in this work with the combination of lithography, dry-etching process and dry oxidation process. By employing a sacrificial oxide etchback technique, they were able to achieve surrounding

gate structures. The 150 nm gate length devices showed a drive current of 1mA/μm with nearly 10^7 I_{on}/I_{off} ratio and acceptable SS value [138]. This cost effective method can be considered to be one of the more promising techniques for next generation nanowire fabrication [138, 139].

Besides stand-alone nanowire transistor fabrication, Si nanowire inverters were also demonstrated in 2007 by top-down approaches. Sharp transfer characteristics were obtained with a low noise margin value. Matched p and n FETs were designed in order to get a symmetrical inverter performance. This circuit results for this unconventional structure indicates the start of a new and advance device generation [136, 138, 140, 141].

Nanowire devices were also demonstrated by other kinds of functional devices such as non-volatile memory devices and SRAM circuit devices [142-144]. In 2007, Samsung Electronics reported the GAA SONOS with ultra thin twin silicon nanowires for the first time [145]. Ultra fast program/erase (P/E) characteristics are observed. As the size of the nanowire decreased, a faster program speed was obtained.

2.4 Challenges of Nanowire Transistors

Currently, there are still some problems which limt the nanowire transistors and nanowire circuit performance. Further investigations and process developments are needed in order to solve these issues.

Recent nanowire research has mostly focused on Si NW transistor development. In order to achieve higher carrier mobility, it would be necessary to explore high mobility nanowire channel materials such as Ge or SiGe. There are few reports discussing the top-down approaches involving Ge or SiGe nanowires. Ge or SiGe nanowire transistors can take advantage of both high mobility and better short channel immunity, compared to

planar Si transistors. On the other hand, the dielectric interface with Ge/SiGe is not as ideal as that with Si. Thus, exploration on better interface formation between the Ge/SiGe nanowire and the dielectric is necessary. It is also known that as the Ge concentration increases, the carrier mobility improves. Existing techniques to obtain higher Ge concentration nanowires still face many challenges. Besides the issues above, a cost effective process is always desirable. Hence, it is desirable to develop a method to fabricate the Ge/SiGe nanowires on bulk Si substrate and thus, reduce the cost. The strain properties of nanowires and carrier backscattering characteristics of nanowire devices are also important aspects for further exploration.

As with conventional planar devices, gate/channel length scaling improves the performance of nanowire devices. As the nanowire channel length decreases, the external resistance becomes an increasingly dominant part of the total resistance, which limits the nanowire transistor drive current. The reduction of series resistance is also an important part for realizing ultra scaled NMOS transistors [146-148]. It would be even more crucial to obtain low series resistance for the nanowire transistor so that maximum benefits can be reaped. A possible way is by utilizing metallic nanowire S/D contacts formed using silicidation. For ultra scaled nanowire transistors, excessive lateral encroachment of the silicide would cause device shorts. A viable technique of forming the metallic nanowire contacts has not been reported yet.

Due to the extremely small dimensions of the nanowire channel, the channel doping is near intrinsic. Doped poly-Si gates have incorrect work-function values and set the V_T too low, resulting in high off state leakage currents. For circuit operation, it is desirable to obtain the correct threshold voltages in both n and pFETs. In 2006, S.D. Suk et al. from Samsung Electronics demonstrated the approach of adopting a single work-function mid-gap metal gate (TiN) nanowire transistors [116]. Nevertheless, this approach

sets the V_T too high (~0.47V) and is not optimum for high performance low voltage circuits. In order to achieve dual work-function for the CMOS FETs, very costly and complicated schemes are often required even for the planar transistors. Examples of these schemes involve poly etch back, different silicide phases or complicated masking steps [149-152]. However, such schemes pose even greater challenges if they are to be implemented on the gate all around nanowire structure. Dopant segregation during FUSI gate formation is another approach for the workfunction tuning [153]. It has been reported that during the Ni silicidation, the dopant will segregate towards the interface between the NiSi film and gate dielectric, providing a means of controlling the gate work function by controlling the dopant concentration prior to silicidation. The method is known as silicidation induced impurity segregation (SIIS) method [154, 155]. This method seems the most viable for GAA nanowire transistors, given its simplicity and effectiveness, and is hence explored in this thesis work.

In the following chapters, key performance bottlenecks for high performance nanowire transistors are addressed by employing novel solutions.

CHAPTER 3

3. CHANNEL ENGINEERING EXPLORATION (1) - Ge Rich Nanowire Hetero Transistors

3.1 Introduction

As discussed in Chapter 2, the GAA Nanowire transistor structure offers the best electrostatic control because the gate surrounds the channel body completely and shields the channel from the electric field lines originating from drain. Therefore, the GAA FET could possibly be the ultimate scaled MOS device architecture for high performance while maintaining low power dissipation.

Besides the architectural innovation, the present gate stack materials comprising thin SiO_2-dielectric/poly-Si electrode are also expected to be replaced by high-k dielectrics/metal gate in order to overcome the issues of high gate leakage and poly-depletion [156-158]. Moreover, Si channel material can be replaced with Ge, which provides ~3× higher intrinsic electron mobility and ~4× higher intrinsic hole mobility to that of Si due to lower effective mass of both electrons and holes [159-164]. Although the unstable nature and poor quality of GeO_2 is no longer a limitation in view of high-k and metal gate integration, the Ge surface gets oxidized easily to form GeO_x, leading to device degradation. Hence, effective surface passivation still remains a challenge. Producing SiGeOI or GOI wafers, which are required as substrates to fabricate Ge nanowire channels using the top-down method, is yet another challenge. In the past, various techniques such as smart-cut [165, 166], Liquid Phase Epitaxy [101, 167, 168], and Ge condensation [169-173] have been used to make such wafers. Cost-effectiveness,

process simplicity, throughput, possible integration into the Si based process flow, ease of control of the thickness of the GOI and low consumption of Ge material are the general requirements in the selection of these fabrication methods.

On Si/Ge nanowires devices, Al_2O_3/Ti [174, 175], HfO_2/Ti [176, 177], SiO_2/Cr [178], ZrO_2/Si (BG) , HfO_2 or ZrO_2/Cr [179] are some of the gate stack combinations already demonstrated. There are some expectations that using top-down fabrication methods, the combination of Si/SiGe/Ge GAA nanowire transistors with high-k/metal gate electrode will lead to the ultimate manufacturable CMOS device structure to replace the conventional planar architecture. SiGe/Ge nanowire transistors are supposed to perform even better.

In this chapter, the top-down integration approach of SiGe nanowire channel transistors is discussed. The epitaxial growth of SiGe film with different deposition thickness was explored. This was followed by the investigation of Ge condensation. Ge rich (70%) nanowire transistors with HfO_2/TaN gate stack were fabricated on SOI substrate. The crystalline structure and the strain properties were investigated in the high Ge concentration nanowire structures. DC characteristics of Ge rich nanowire exhibited enhancement comparing with planar transistors. The backscattering characteristics were also studied in the Ge rich nanowire devices.

In the work described in this chapter, I gratefully acknowledge the help of K.M. Hoe and C.H. Tung of the Institute of Microelectronics in the cross-sectional TEM imaging. Dr. S. Balakumar also gave valuable suggestions on the Ge condensation process. The use of the excellent facilities at IME is greatly appreciated. However, the ideas were conceived by me, and I have benefited through discussions with my mentors at IME, Dr. Navab Singh and Dr Patrick Lo. All the experiments were designed and executed by myself under the guidance of my mentors.

3.2 SiGe Growth and Ge Condensation

3.2.1 Review on the Ge Condensation Technique

Ge condensation technique has been introduced for SiGe nanowire fabrication. To grow SiGe layers on SOI wafer is a critical issue on the condensation part. The first epitaxy of $Si_{1-x}Ge_x$ layers was achieved using Molecular-Beam-epitaxy (MBE) [180, 181] and many universities still use MBE systems in research. As the thickness of the epitaxial layer is increased, there exists a maximum thickness, called the critical thickness, h_c, Defects such as misfit dislocations then begin to appear, which act to relieve the strain in the epitaxial film. A number of models have been developed to predict the critical thickness of the strained epitaxial layer. Van der Merwe [182] produced a thermodynamic equilibrium model by minimizing the total energy of a system with the generation of a periodic array of dislocations. This produced a critical thickness defined as:

$$h_c \approx \frac{19}{16\pi^2}\left(\frac{1+v}{1-v}\right)\left(\frac{b}{f}\right) \qquad (3.1)$$

where b is the slip distance which for misfit dislocations is the Burgers vector. For a bulk-silicon substrate b = 0.4 nm and more generally where f is the lattice constant of the relaxed substrate. This critical thickness is plotted in Fig. 3.1 and corresponds to the boundary between the stable and metastable regions.

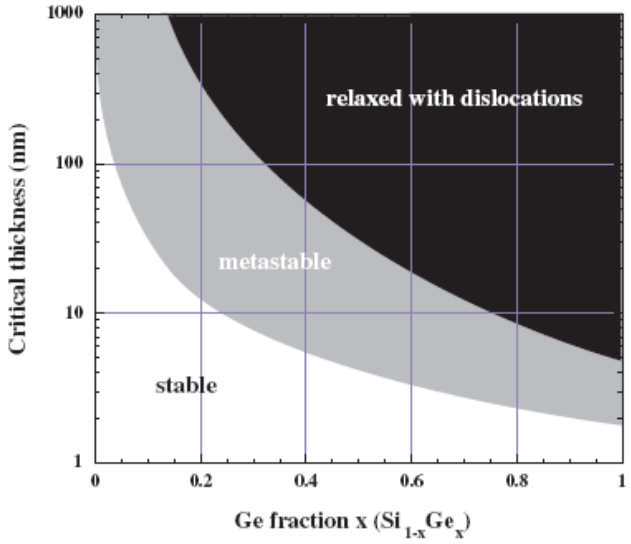


Fig. 3.1: Matthews and Blakeslee critical thickness plotted against germanium fraction for pseudomorphic $Si_{1-x}Ge_x$ layers grown on bulk (100) silicon. Also included a metastable curve for MBE growth at 550 ◦C [182].

Ge condensation technique was first introduced by Tezuka et al. [170, 172] in 2002 and has been intensively studied [136, 170, 172, 183-192]. The process is described as follows. First of all, an epitaxial SiGe layer is grown on a SOI wafer and then the wafer is subjected to oxidation in the furnace. During high temperature oxidation, Si is selectively oxidized because the formation energy of SiO_2 is much lower than that of GeO_2 (ΔG = -732kJ/mol for SiO_2 and ΔG = -376kJ/mol for GeO_2) and Ge atoms are rejected from the oxide layer and diffuse towards the substrate. The diffusion of Ge is then blocked by the buried oxide layer due to the small diffusion coefficient of Ge in oxide. Thus the Ge atoms are condensed and confined between the two oxide layers while the total number of Ge atoms is preserved. A diffusion model for oxidation of SiGe alloy has been proposed by Kilpatrick, Jaccodine and Thompson [193, 194], where the diffusion of oxygen and silicon atoms and crossover temperature are discussed in detail. After oxidation, the top thermal oxide layer can be removed by using hydrofluoric acid (HF) and the SGOI structure remains. The condensation process is illustrated in Fig. 3.2.

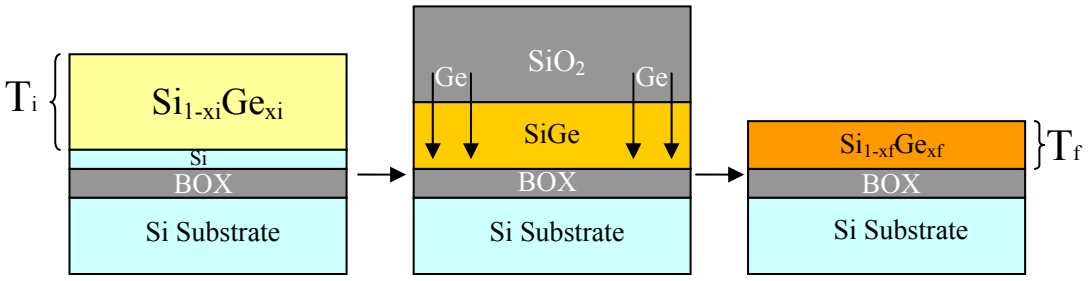


Fig. 3.2: Schematics illustrating the Ge condensation technique

The following relationship can be derived,

$$x_i T_i = x_f T_f \qquad (3.2)$$

Where x_i and T_i are the initial Ge concentration and SiGe thickness and x_f and T_f are the final Ge concentration and SiGe thickness, respectively. The desired Ge concentration and thickness can be easily achieved by adjusting initial Ge content, thickness and oxidation condition (such as time and temperature).

The challenges of Ge condensation technique include process condition optimization, Ge balling up issue due to high Ge content, amorphization due to oxidation at inappropriate temperatures, self limited oxidation behavior, SiGe melting due to the low melting point of Ge and Ge loss due to formation of volatile GeO.

3.2.2 Experiments on SiGe Growth and Ge Condensation

SiGe films with concentration of 15% and 25% were grown. Cold wall ultra-high vacuum chemical vapor deposition (UHV-CVD) system is used to form SiGe epitaxial layer at 580°C. For epitaxial process, a mixture of undiluted Si_2H_6 and Ar-diluted GeH_4 precursor gases was used for SiGe layer growth. Fig. 3.3, 3.4 show the DRSEM pictures after SiGe (25%) deposition with different deposition thicknesses.

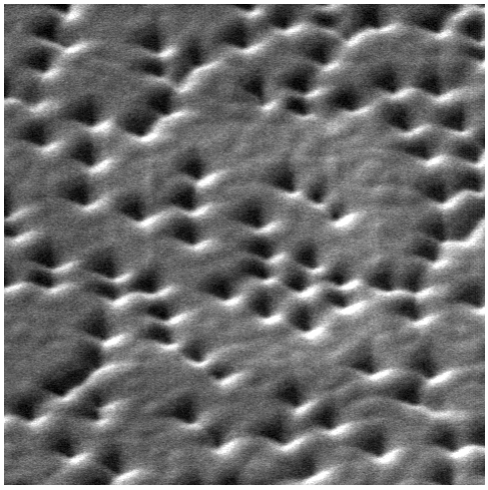


Fig. 3.3: 50nm SiGe 25%@ 580°C

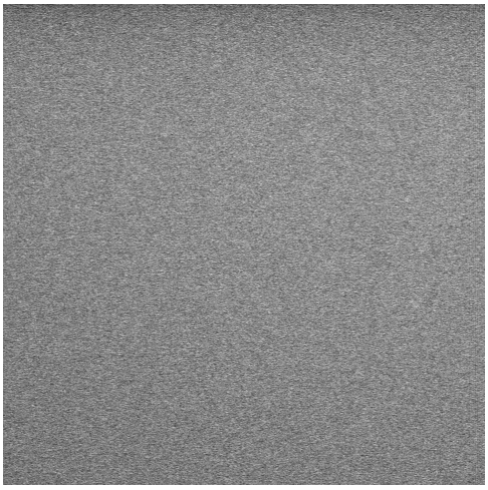


Fig. 3.4: 20nm SiGe 25%@ 580°C

As shown in Fig. 3.3, 3.4, 50nm SiGe with Ge 25%@ 580°C has poor surface morphology while the 20nm SiGe with Ge 25% @ 580°C layer shows smooth surface features. Some possible reasons are accounted below: (1) Native oxide formed after pre-epi clean cannot be fully removed by the ultra-high vacuum (UHV) anneal (UHV anneal volatilizes native oxide). (2) The temperature of 580°C for SiGe epitaxial process is a bit too high for 25% SiGe layer growth. (3) SOI defects are decorated by the epitaxial growth of 50nm SiGe layer. In order to solve this problem, some possible solutions have been used: (1) Use lower epi growth temperature (e.g. 500°C) (2) Reduce delay time between pre-epi clean and epitaxy growth and increase the temperature of the UHV anneal. (3) Lower the target SiGe epitaxial layer thickness or Ge% of SiGe layer. After optimizing these processes, two kinds of SiGe epitaxy layers have been used for SiGe nanowire fabrication. They are: (1) 40nm SiGe (25%) epitaxial growth at 580°C. (2) 140nm SiGe (15%) epitaxial growth at 580°C.

Cyclic oxidation and annealing method has been developed in order to get a uniform and less rough surface SGOI substrate. The Ge condensation process is divided into 3 steps: (1) 1050°C cyclic oxidation and anneal processes were performed to

condense the Ge into Si substrate. Annealing can make the Ge concentration more uniform. (2) Further condensation using the oxidation & annealing cycles at a relatively lower temperature (950°C) was carried out to obtain higher Ge content. (3) Low temperature annealing (750°C) was performed to get better surface morphology.

Fig. 3.5 shows the TEM picture for the SGOI substrate after condensation process, the starting SiGe layer is 40nm with Ge 25% on SOI substrate with top Si of 20 nm, after three-step condensation. Using EDX analysis, the Ge concentration across SiGe layer was found to be ~30%. Uniform Ge with 30% concentration layer with thickness of 525A has been achieved. After oxide strip, AFM surface analysis was performed on the SGOI substrate with scan size of 5μm, scan rate of 1.5Hz. As shown in Fig. 3.6, the RMS value of SGOI layer was 0.33nm which implies comparable surface smoothness with the bulk Si substrate. The image statistics data is shown in the box below the AFM image.

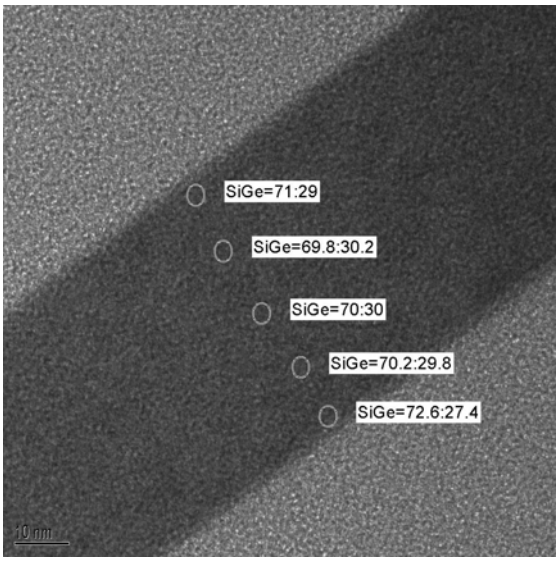


Fig. 3.5: TEM micrograph of SiGe layer after Ge condensation, a uniform SiGe layer was achieved by the cyclic oxidation and annealing steps.

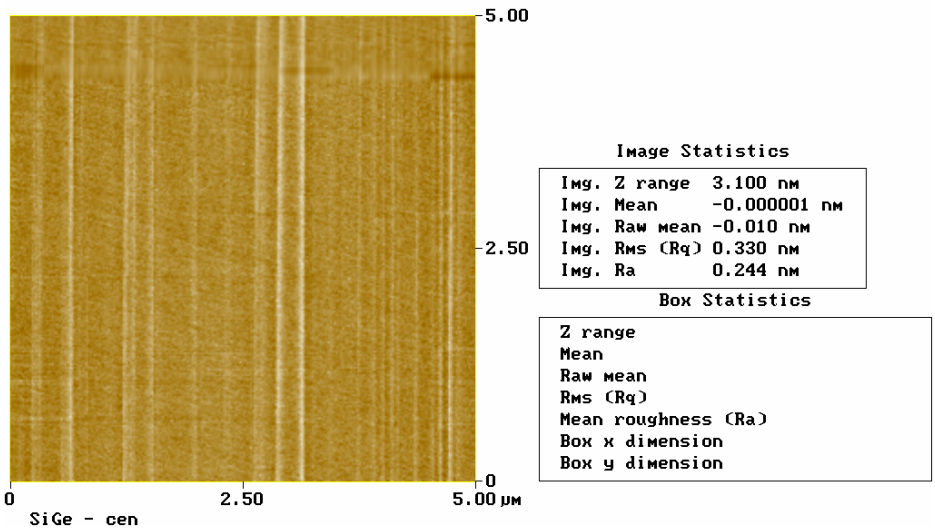


Fig. 3.6: AFM surface analysis of SiGe film after Ge condensation technique. Good surface morphology is obtained with RMS value~ 0.33 nm.

3.3 SiGe Nanowire Formation

As mentioned in chapter 1 and 2, CVD grown nanowires are generally randomly spread over the substrate, making it very difficult to use them in CMOS integration. A more compatible method is needed so as to get ordered nanowire placement. In our experiment, we have introduced a top-down approach for SiGe nanowire transistors fabrication with HfO_2/TaN gate. Process flow of SiGe nanowire fabrication is shown below: (with schematics for the key steps), the details will be discussed later.

- Thinning down of SOI (top Si thickness reduce to 200nm)

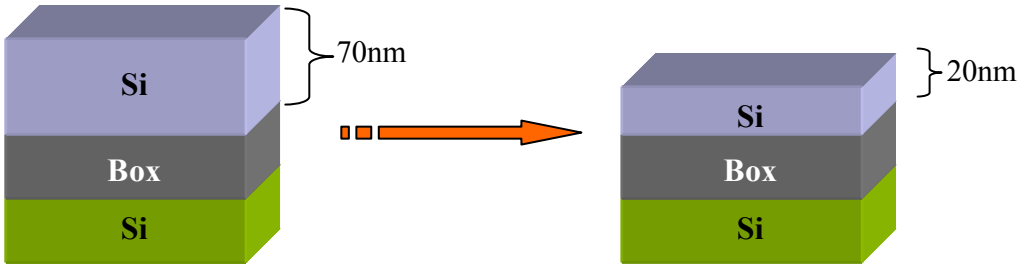


Fig. 3.7: Schematics illustrating of SOI thinning down process by dry oxidation process

- Epitaxy of SiGe layer on thin SOI substrate
- SiGe layer 1st condensation (Cyclic oxidation and annealing to form SGOI substrate). Details can be found in section 3.3.2.

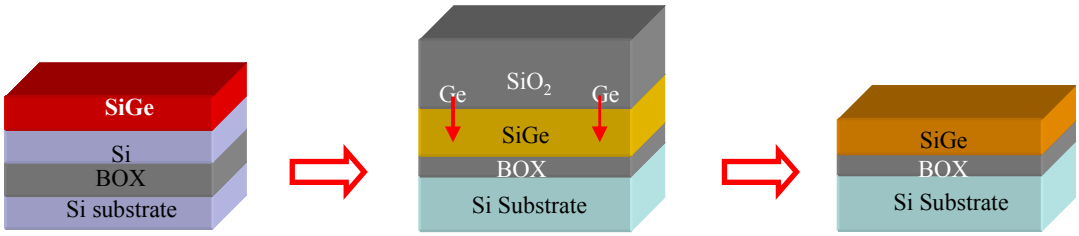


Fig. 3.8: Schematics illustrating Ge condensation process by the cyclic oxidation and annealing processes

- Fin definition. Fin structures were patterned using 248nm KrF lithography. Alternating phase shift mask was used to pattern ultra narrow (120 nm) fins. In order to get even smaller Critical Dimensions (CD) before SiGe nanowire oxidation, further photoresist trimming needs to be done by using oxygen plasma with RF bias to obtain a 40-60 nm fin. Fig. 3.9 shows the structure after SiGe fin formation. And the AA' plane denotes the cutting plane of the SiGe fin.

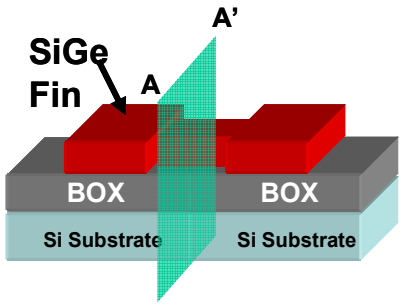


Fig. 3.9: Schematics after SiGe fin definitions. The AA' plane denotes the cutting plane of the SiGe fin cross-sections.

- Nanowire oxidation (2nd condensation). When fin width is trimmed down to 40-60 nm, an oxidation at 800-875°C is carried out. The fin area is then surrounded by thermal oxide. The following two figures show the cross section of the cutting plane AA'.

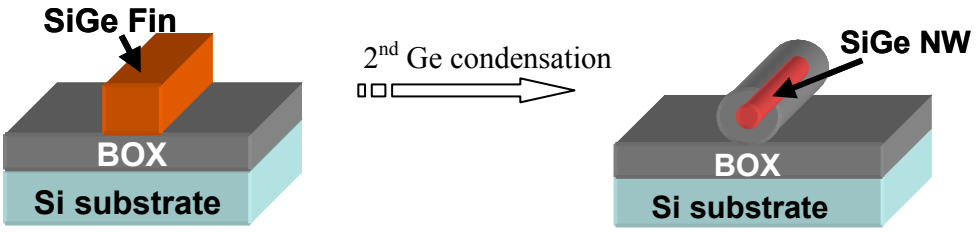


Fig. 3.10: Schematics illustrating the 2nd Ge condensation technique, after the 2nd Ge condensation technique, Ge rich nanowire formed.

- Oxide release in order to expose SiGe nanowire. Using HF wet etching process to remove the oxide at the fin area, a SiGe nanowire is formed.

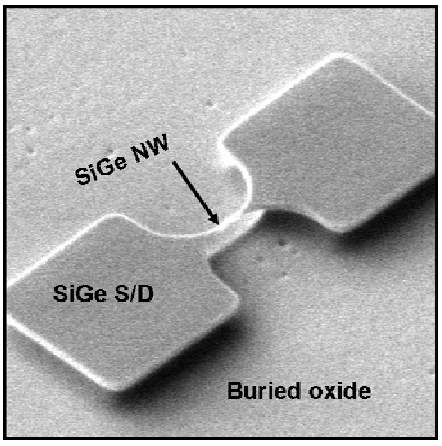


Fig. 3.11: SEM image after SiGe NW release processes.

- HfO_2/TaN gate-stack deposition
- Gate definition
- S/D implant and RTA activation
- PECVD SiO_2 deposition and metallization

By using this Ge condensation method, SiGe nanowire with different Ge concentration can be obtained. Fig. 3.12 is the TEM pictures after SiGe nanowire oxidation and formation. SiGe nanowires with 84.5% Ge, diameter 14.5nm and 21% Ge, 7.8nm diameter were formed respectively.

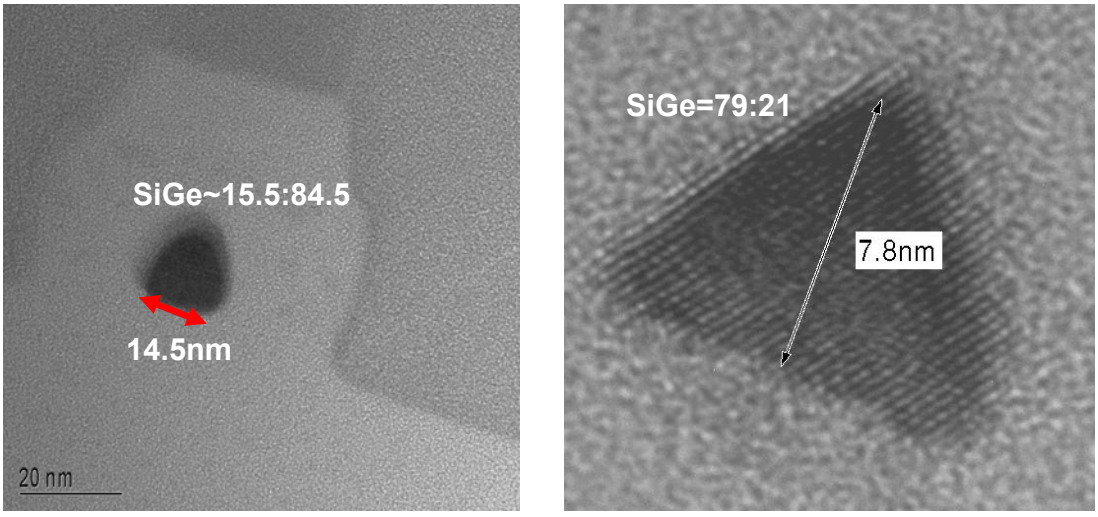


Fig. 3.12: TEM images after SiGe nanowire oxidation and formation. SiGe nanowires with diameter of 14.5nm, Ge%~84.5% and with diameter of 7.8 nm, Ge%~21% are formed respectively.

3.4 Ge Rich Nanowire FETs

3.4.1 Ge Rich Nanowire FETs Farication

SiGe NW (SGNW) PFETs with HfO_2/TaN gate stack fabricated using two-step Ge condensation have been reported [195]. Fig. 3.13 list the key steps for SGNW integration as discussed in previous session. The device fabrication process is described below.

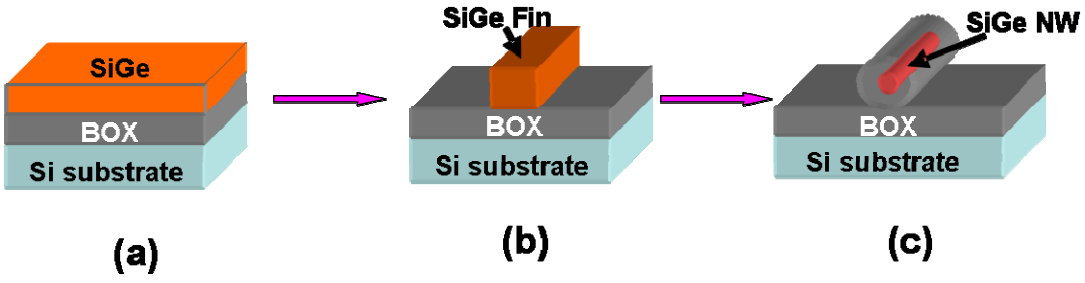


Fig. 3.13: Schematics illustration SiGe NW formation processes

P-type ($1\times10^{15}cm^{-2}$) SOI wafers with top Si thickness of 70nm was first thinned down to 20nm by dry oxidation process. Next, SiGe layer (25%) was epitaxially

deposited on the thin SOI substrate by UHVCVD at 580ºC. After SiGe layer growth, cyclic oxidation and annealing process (first condensation) was used to form a uniform SGOI substrate. Both high (950ºC) and low (750ºC) temperature process cycles were used for the first Ge condensation step. The lower oxidation and annealing cycle helps to improve the surface smoothness. Next, alternating phase-shift-mask lithography with KrF scanner was used for the SiGe fin patterning. SiGe Fin was further trimmed down to 40nm by O_2-plasma photoresist trimming and reactive ion etching processes. Fig. 3.13(b) shows the schematic view of the cross-section of SiGe fin structure. After fin pattern, SiGe fin was two-dimensionally condensed at 875° C (second condensation). This resulted Ge enrichment in the channel as well as the size reduction. After second condensation step, oxide-encapsulated [Ge]-rich SGNW was formed as shown in Fig. 3.13(c). Ge% of 70% was obtained by this two-step Ge condensation technique.

In order to improve the interface quality between SGNW and gate dielectric, after SiGe nanowire release, the SGNW surface was passivated with 2 nm Si epitaxial layer followed by ~8 nm HfO_2 and 75 nm TaN gate PVD deposition. The fabrication process was completed with gate patterning, BF_2 S/D implant, activation and metallization.

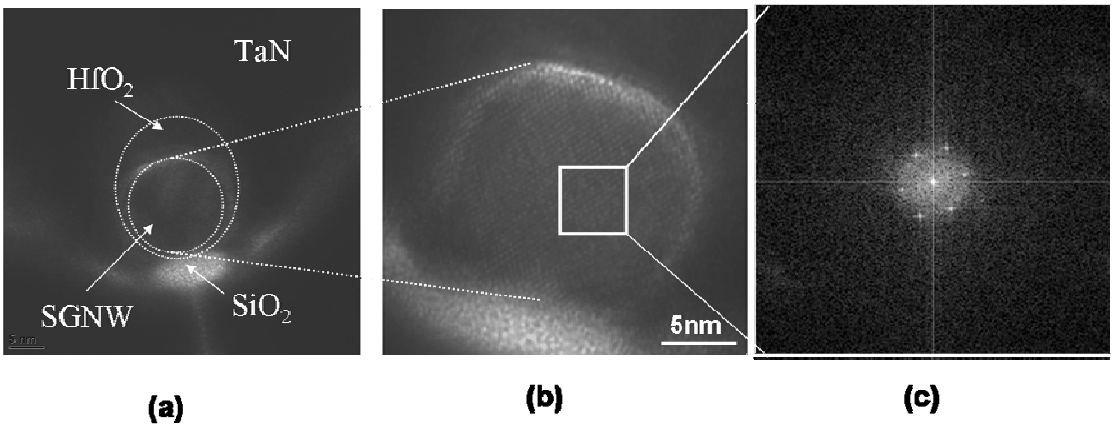


Fig. 3.14 (a) TEM image of channel cross-section, showing the SiGe (70%) nanowire with diameter of 12 nm and HfO_2/TaN gate stack. (b) HRTEM image of the SiGe nanowire, good crystalline structure can be seen clearly. (c) Reciprocal space diffractogram (FFT) analysis. Clear and sharp spots in the diffractogram implies defect free and crystalline SGNW formed by this two step process

Fig. 3.14 (a) is the TEM micrograph of the channel cross-section for a complete SGNW PFET device with HfO_2/TaN gate stack. The diameter of SGNW is 12nm, with Ge% up to 70% confirmed by EDX analysis. Due to the non-conformal nature for the PVD system, HfO_2 was found to be thicker on the top than the side walls, which results in a reduced overall physical thickness. The gate almost surrounded the channel. The HRTEM image for the SGNW channel is shown in Fig.3.14 (b). From the HRTEM image for the SGNW, good crystalline structure can be seen clearly. Thin Si (<2nm) passivation layer was formed covering SGNW in HRTEM image. Fig. 3.14 (c) shows the reciprocal space diffractogram (FFT) of SGNW. Clear and sharp spots in the diffractogram implies defect-free and crystalline SGNW formed by this two step process. Taking Si (111) lattice from substrate as a stress free reference, the nanowire was found to be under compressive strain (-0.63%).

3.4.2 Electrical Characteristics of SGNW FETs

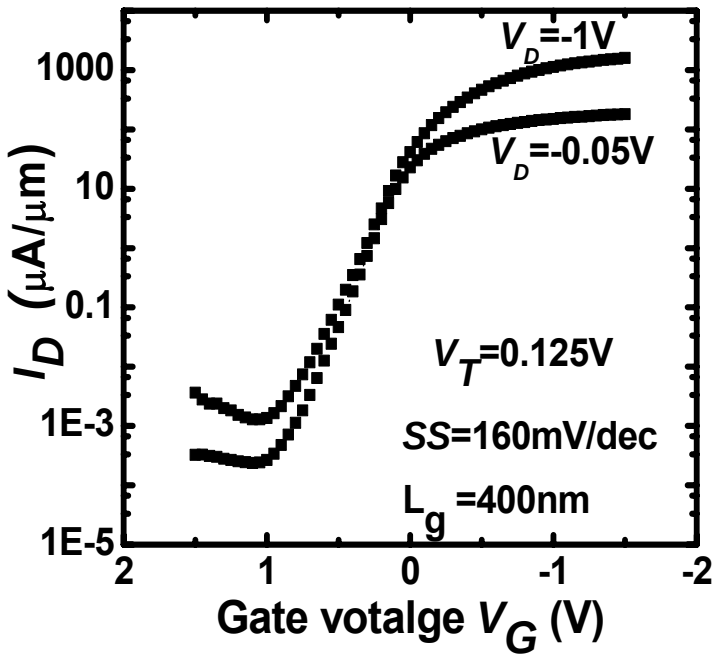


Fig. 3.15 I_D-V_G characteristics of SiGe NW device with NW diameter of 12nm, *Lg* - 400 nm, DIBL ~ 40mV/dec, I_{on}-I_{off} ~ 10^5

The I_D-V_G characteristics of the SiGe nanowire transistor with a gate length of 400 nm are shown in Fig. 3.15. The drain current was normalized by its diameter and the V_T was extracted to be ~0.125V. The subthreshold swing of this device is ~ 160 mV/dec. Acceptable subthreshold swings and drain-induced barrier lowering (DIBL) have been obtained for such SGNW devices due to the effective Si epitaxial surface passivation method. The SiGe nanowire device also shows good DIBL parameter of ~40 mV/V and an I_{on}-I_{off} ratio of 10^5. The I_D-V_D characteristics of the same device are shown in Fig. 3.16. The drive current at V_G-V_T = -1.0V is ~1000 μA/μm, which is exceptionally high for a long gate-length p-channel device.

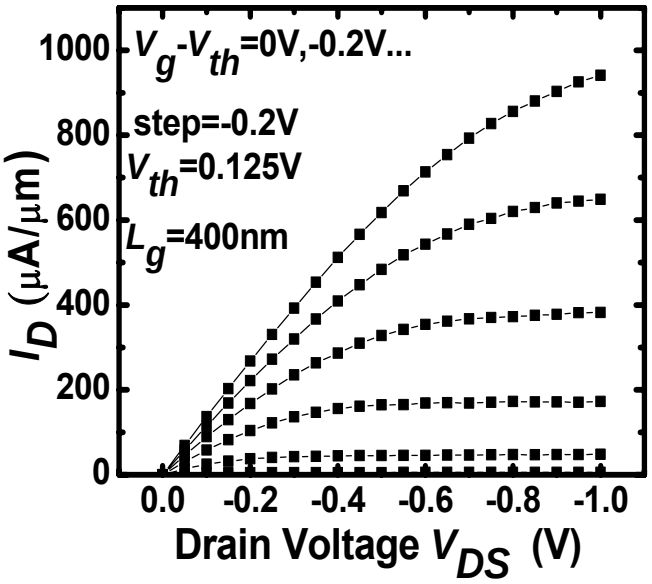


Fig. 3.16 I_D-V_D characteristics of the same device. Drive current is ~1000μA/μm @ V_G-V_T=-1.0V

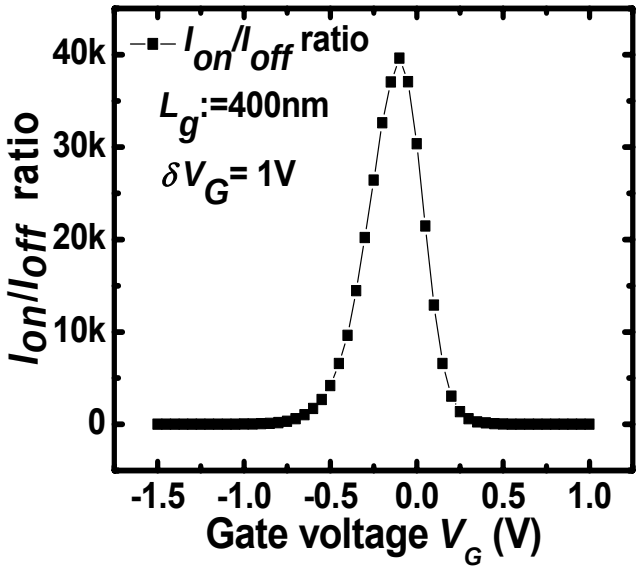


Fig. 3.17 I_{on}-I_{off} ratio for 400nm SiGe NW. (I_{on}-I_{off} ratio = I_D value@V_G+1V divided by that @V_G. V_G from -1.5V to 1V)

Fig. 3.17 plots the I_{on}-I_{off} ratio for L_G=400nm SiGe nanowire devices. This is the ratio of the drain current value at (V_G + 1.0 V) divided by that at V_G, as V_G moves from -1.5V to 1V. It can be seen that the I_{on}-I_{off} peak is >>10^4, suggesting good performance for such SiGe nanowire devices.

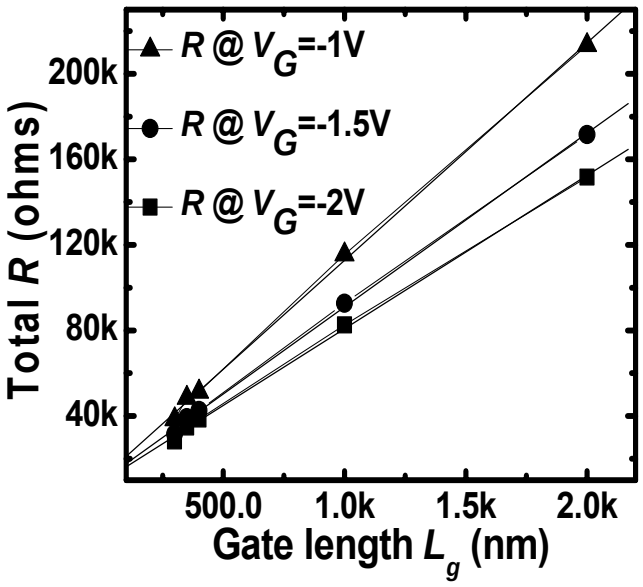


Fig. 3.18 Plot of resistance as a function of L_G @ V_G =-1V,-1.5V,-2V. The extracted series resistance is ~10kΩ

Fig.3.18 shows series resistance extraction using devices of different gate lengths biased in the linear region, estimating the absolute series resistance to be approximately ~10 kΩ. R total is extracted by the equation of $R_{Total} = \frac{V_D}{I_D} = \frac{0.05}{I_D}$. This corresponds to a value of 130 Ωμm if a nominal nanowire device width of 12 nm is assumed.

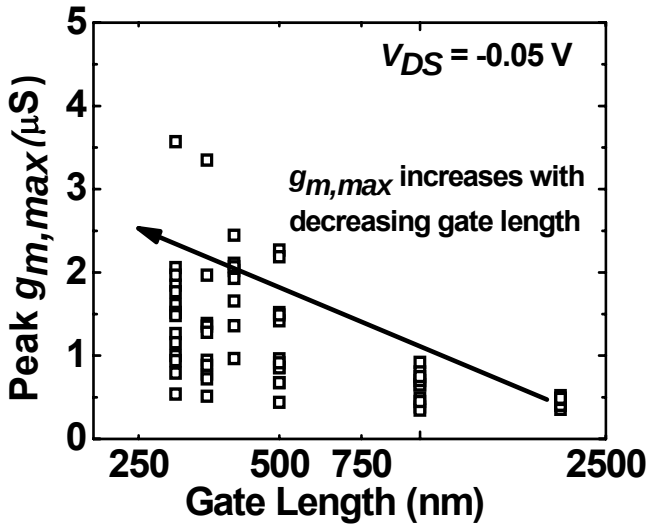


Fig. 3.19 Plot of g_m peak as a function of L_G. As L_G decreases, g_m peak increases.

Fig.3.19 plots the peak of linear transconductance for different gate lengths. The Gm is extracted by the equation of $Gm = \frac{dI_D}{dV_G}$. As the gate length decreases, the transconductance peak increases. Fig. 3.20 compares the drive current for different gate lengths. The drive current shows the same trend as the transconductance peak. For this first demonstration, all the fabricated SiGe NW devices are long channel devices. It is expected that the performance of these devices will improve further when gate lengths are scaled down.

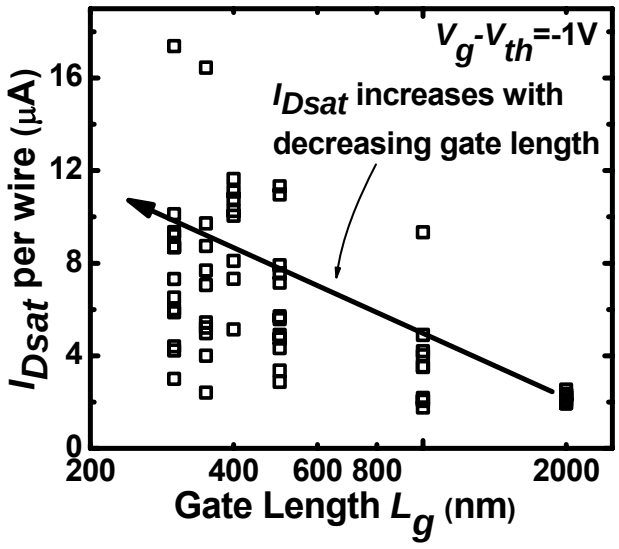


Fig. 3.20 Plot of I_{Dsat} per wire versus L_G. I_{Dsat} improves when L_G decreases.

3.4.3 Energy Band Diagram Investigation of SGNW

During the oxidation process (second Ge condensation), the pattern size and shape dependent Ge condensation takes place – a key process which converts the homogeneous structure (homo-structure) to a hetero-structure. In the narrow fins, the second condensation proceeded 2-dimensionally (almost from all 4 sides) as opposed to 1-dimensionally in the large S/D mesas (only from the top) as illustrated in Fig.3.21. This resulted in Ge enrichment within the channel, along with size reduction from 40 nm to 13 nm. The S/D regions maintained almost the same Ge concentration as obtained by the first condensation. Therefore, the second condensation step resulted in the formation of an oxide-encapsulated [Ge]-rich SiGe nanowire channel connected to lower Ge-content S/D regions as shown in Fig. 3.22. For comparison purpose, large channel width (W=1μm) planar devices were also fabricated on the same wafer. Due to large width, the impact of the second condensation on the channel region in planar devices was same as that on the S/D mesas (uniform Ge concentration of ~30% was obtained). Thus, a horizontal

heterojunction structure between Source-Channel-Drain (S-C-D) was formed for nanowires and a homo-junction was obtained in wide channel planar devices.

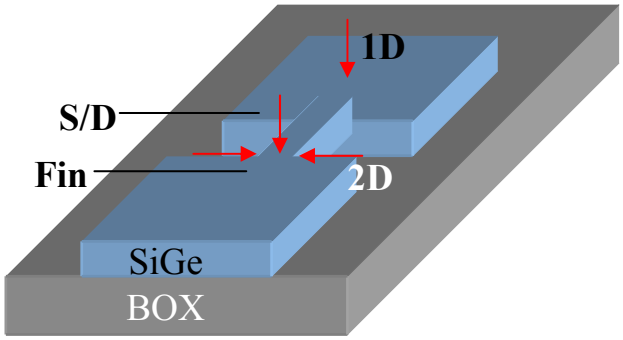


Fig. 3.21 Schematic illustrating pattern size dependent Ge condensation technique

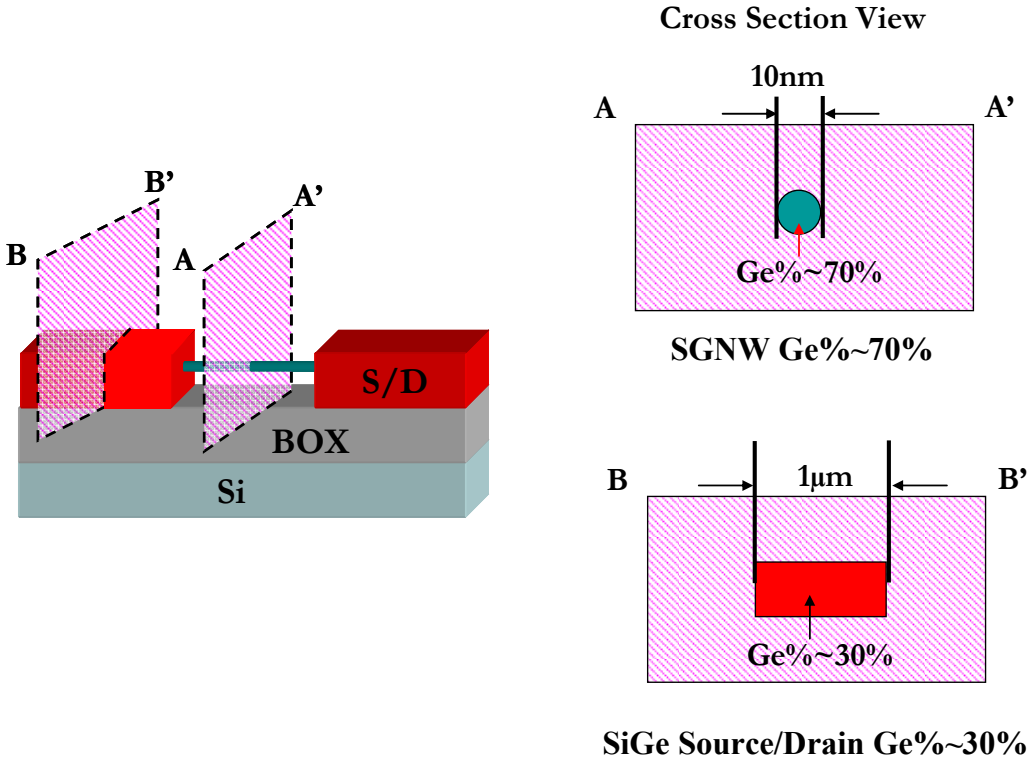


Fig. 3.22 Schematic illustrating Ge% difference between SiGe NW channel and source/drain area, thus forming the lateral heterostructure.

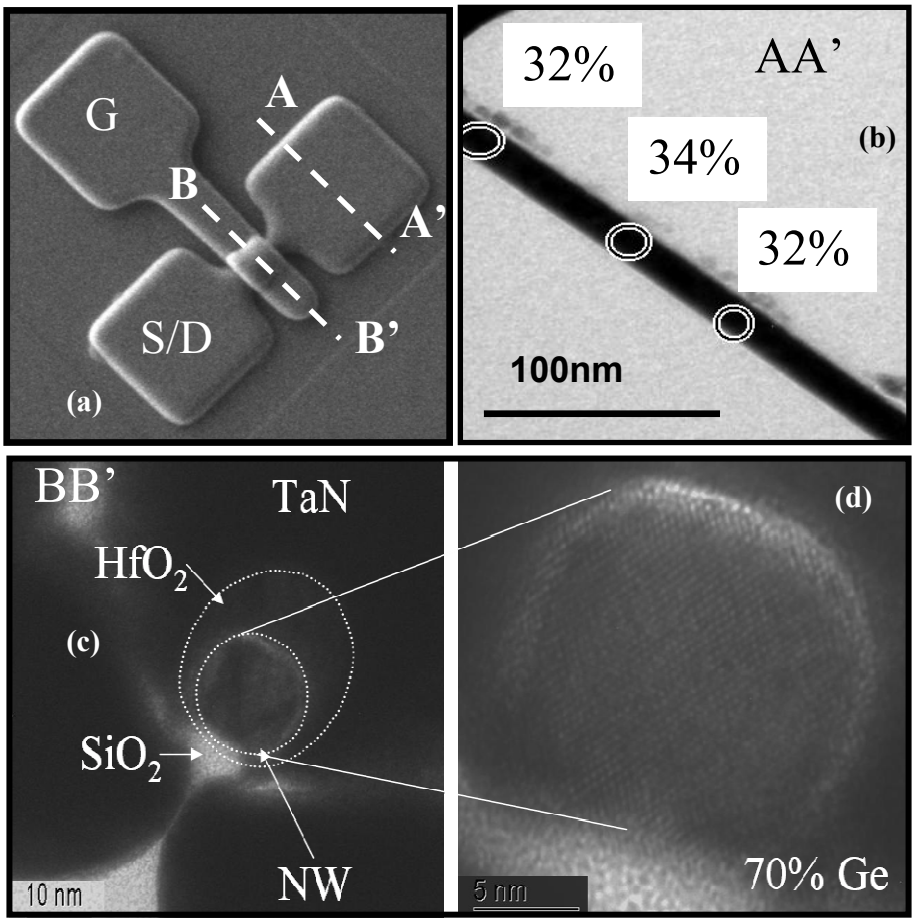
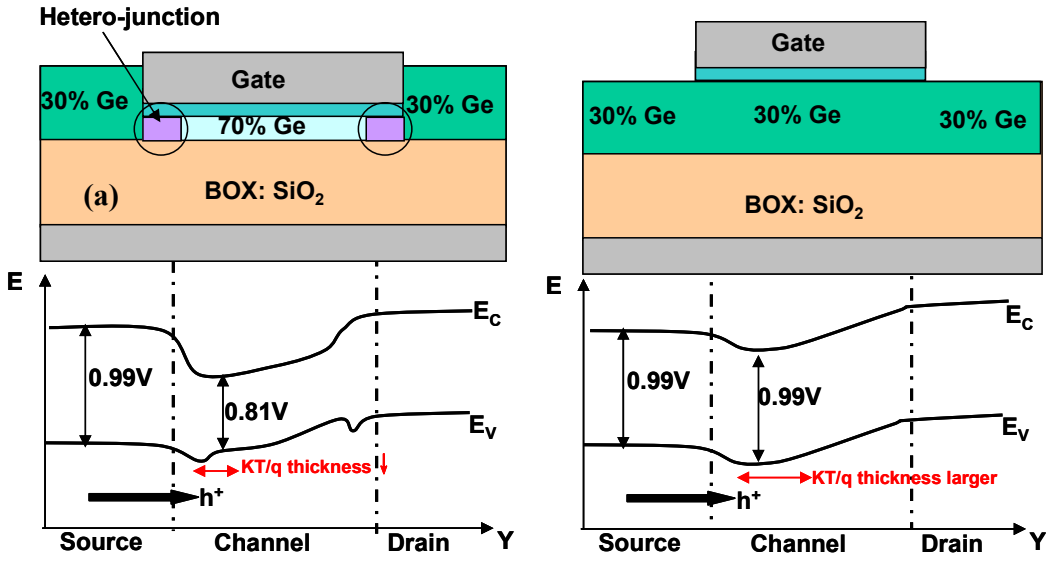


Fig. 3.23 (a) SEM image of a completed SGNW FETs with AA' and BB' representing two TEM cutting planes. (b) TEM image of S/D region for AA' cut. Ge concentration is around 30%. (c) TEM micrograph of cross-section (BB' cut) for SiGe NW channel, followed by the HfO_2 and TaN metal gate stack. The diameter of SiGe NW is 12nm. EDX showing Ge% in SiGe NW is 70%, and the HRTEM image of SiGe NW is showing on the right.

Fig. 3.23 (a) shows SEM image of a SGNW FET with gate and S/D regions indicated. AA' and BB' denoted TEM cutting planes for S/D regions and channel regions respectively. As shown in (b) the Ge concentration is ~30% in the S/D regions (AA' cut) due to one-dimensional Ge condensation. Fig. 3.23 (c) shows the cross-section TEM micrograph (BB' cut) of the SGNW channel regions. The SGNW, with a diameter of 12 nm, is covered by 8 nm-thick HfO_2 and 75 nm-thick TaN with some shadowing effect and thus forming Ω-shaped gate structure. The corresponding HRTEM image of the SGNW is

shown in Fig.3.23 (d). The SGNW is nearly circular with a Ge concentration of up to 70 %. Good crystalline structure of the nanowire indicates the effective suppression of defect formation by utilizing Ge condensation method with cyclic annealing.



(a) (b)

Fig. 3.24 Schematic view of SiGe NW devices with hetero-structure along channel direction. Ge concentration is modulating in S-C-D, where 30% Ge is in S/D while 70% in the channel area. The band diagram along the channel direction is shown below. As Ge% varies, the band gap changes from 0.99V (S/D) to 0.81V (Channel). This results valence band offset between source and channel, which reduces the KT/q layer thickness from source towards channel. Fig. 3.24 (b) Shows schematic view of homo-structure for comparison, the KT/q layer thickness is larger compared to hetero-structure devices.

Fig. 3.24 illustrates the band diagram along the channel direction, with the corresponding schematic view of the device structure on top, for both hetero-junction and homo-junction devices. As is shown in Fig. 3.24 (a), the band gap decreases significantly with higher Ge concentration as given by

$$E_g(alloy) = xEg_1 + (1-x)Eg_2 \qquad (3.3)$$

Without considering any strain effects inside the nanowire, the band gaps of $Si_{0.7}Ge_{0.3}$ and 70% $Si_{0.3}Ge_{0.7}$ band gap were calculated to be ~0.99V and ~0.81V respectively. In our

process, a non-abrupt hetero-junction with graded Ge concentration (indicated in the circle) is formed as a result of the curved S/D extensions and the channel regions due to corner round effect in the fin lithography. Although the hetero-structure is non-abrupt, the hole injection velocity from the source into the channel is expected to increase with the excess kinetic energy from the valence band offset. Furthermore, the decreased thickness of KT/q barrier layer from the channel to the source at a given gate overdrive voltage reduces the probability and proportion of carrier backscattering. For comparison, the schematic of the control planar device is also shown in Fig. 3.24 (b). Due to the uniform Ge concentration along the channel direction, the homo-structure has a constant band gap (0.99V) from source to channel region. Thus, a relatively larger KT/q thickness is observed.

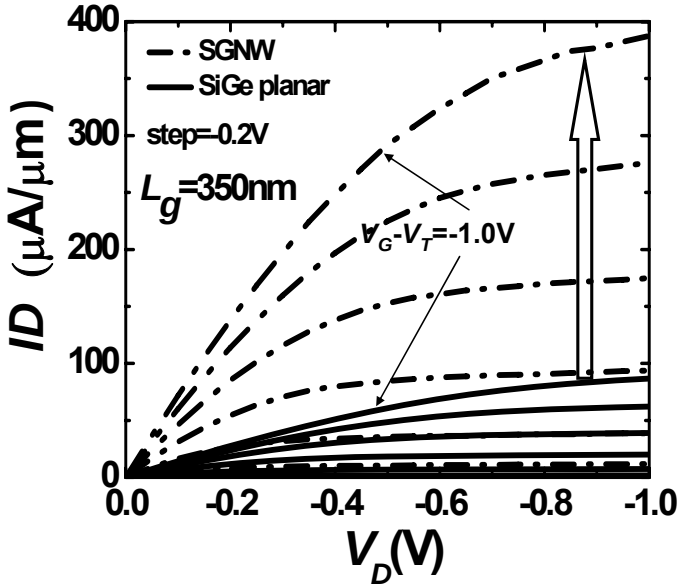


Fig. 3.25 I_D–V_D characteristics comparing the performance of hetero SGNW pFET (current normalized to perimeter) with planar homo SiGe channel (W = 1 μm) device. Drive current of SGNW device is 4.5× than that of planar devices.

Fig. 3.25 compares normalized I_D-V_D characteristics for SGNW and $Si_{0.7}Ge_{0.3}$ homo planar devices with gate lengths of 350nm. By using an even more conservative normalization method, i.e. the drain current of SGNW was normalized by its perimeter (assuming a GAA channel with surface inversion) while that of the planar device current

was normalized by channel width. The drive current of SGNW is ~4.5 times larger than planar devices. High drive current of SGNW implies large effective mobility for these strained Ge rich nanowire MOSFETs with lateral hetero-junction structure. Similarly, for planar devices fabricated on thin SGOI by local condensation technique with the Ge modulation from source to channel, Tezuka et. al. also reported ~10× enhancement in the mobility in SGOI channel [196-198]. A similar trend was found for transconductance– the peak Gm value in saturation as well in linear region for SGNW devices is 4.5× larger than planar devices in Fig. 3.26.

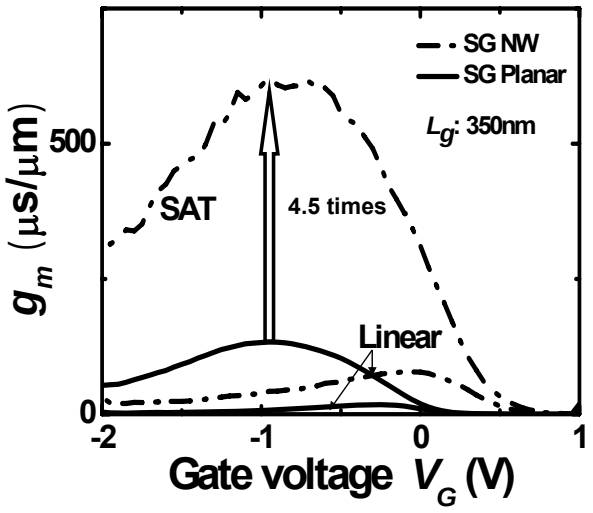


Fig. 3.26 G_m–V_G characteristics of hetero nanowire and homoplanar devices. Both saturation and linear G_m show 4.5 × enhancements for hetero nanowire device (normalized to perimeter) in comparison to homoplanar (normalized to W). Saturation G_m does not decrease too rapidly after the peak, which indicates that ON-state channel resistances dominate compared to the parasitic series resistances at lower gate overdrive voltages.

The enhancement in normalized current and G_m could be attributed to the following factors: firstly, better gate control has been achieved due to Ω-gated channel, increased carrier density due to volume inversion ; secondly, featuring horizontal hetero-junction between S-C-D, hole velocity is enhanced due to an excess kinetic energy which results from of the source to channel valence band offset ΔE_V; thirdly, Ge concentration

of SGNW channel is 70%, leading to larger hole mobility than the planar channel with lower Ge content; fourthly, lateral compressive strain (-0.6%) in the SGNW channel further increases the hole mobility; fifthly, the nanowire benefits from having a smaller EOT at the sidewalls due to the non-conformal nature of PVD dielectric deposition (However, EOT is thicker at the bottom due to residual buried Si dioxide); lastly, the nanowire device has a smaller access resistance due to the funnel-shaped extension regions. While another control homo-junction nanowire device with channel comprising $Si_{0.3}Ge_{0.7}$ would allow the heterojunction effect to be decoupled, this was omitted as fabricating the required device with exact Ge content and dimensions is too difficult. However, it is obvious that the large enhancement and high absolute drive current (for L_G=350 nm) observed is a result of compound effects and may not be attributed to the last two effects alone.

To investigate the hole injection enhancement due to the S-C-D hetero-structure, the channel backscattering coefficients for both SGNW and planar devices were extracted using a temperature-dependent model [199, 200].

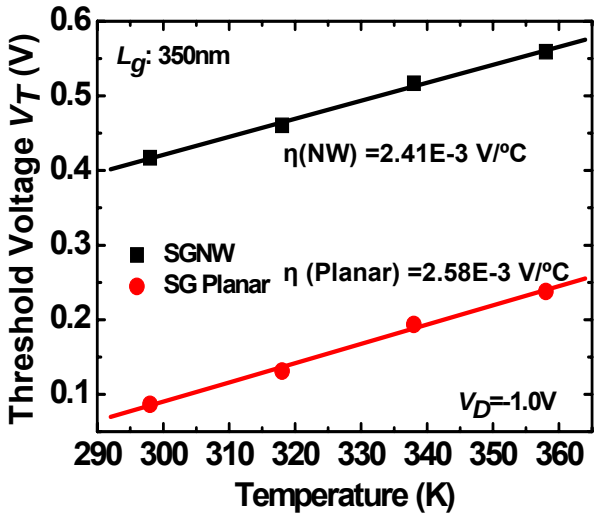


Fig. 3.27 Threshold voltage dependency with temperature for both SGNW and SG planar devices. Comparable η observed for two kinds of devices.

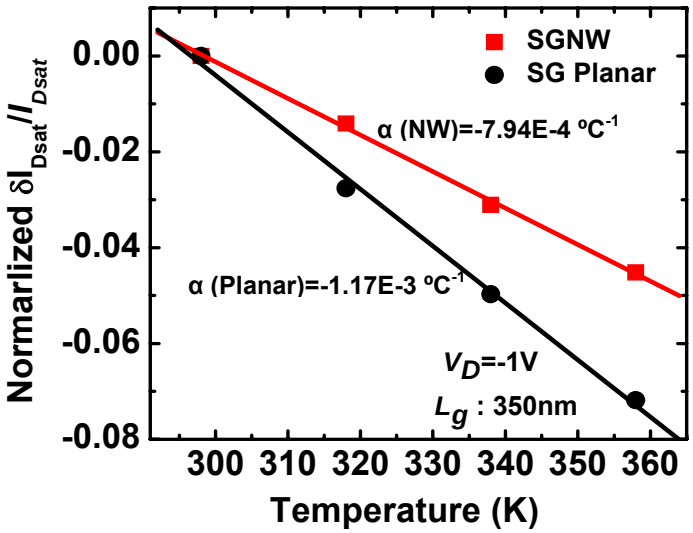


Fig. 3.28 Drive current changes with temperature for SGNW and planar devices at V_D=-1V. Temperature coefficient α of SGNW is 32% smaller than planar devices.

Fig. 3.27, 3.28 shows the temperature dependence of threshold voltage V_T, I_{Dsat} for both SGNW and planar devices with gate length of 350nm, respectively. η, α are the temperature coefficient of V_T, I_{Dsat} obtained from the gradient. There is not much difference on the threshold voltage with the temperatures as indicated in Fig. 3.27 while α of SGNW is ~32% smaller than that of the control planar device in Fig. 3.28.

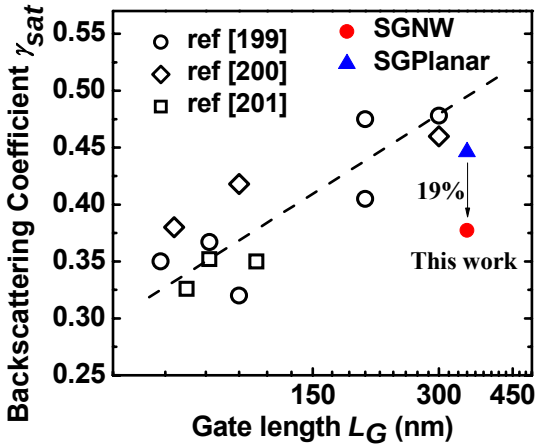


Fig. 3.29 Comparison of backscattering coefficient for this work and other work (ref [199-201]). γ_{sat} of SGNW was found far below the fitting line at the same gate length. And 19% reduction has been achieved for SGNW devices over planar devices.

Next, by using temperature dependent analytical model, backscattering coefficient was extracted. Fig. 3.29 plots the backscattering coefficient for both SGNW devices and homo-junction planar devices. The backscattering coefficients from other work are also shown for comparison. By linearly fitting the reference data and extrapolation towards longer gate length, it becomes obvious that the backscattering coefficient of the SGNW is far below the trend-line for the same gate length. Furthermore, the backscattering coefficient γsat of the SGNW is 19% lower than that of the control planar devices. This confirms that the hetero-structure SGNW indeed has enhanced hole injection due to the hole barrier KT/q layer thickness reduction as shown in Fig. 3.30.

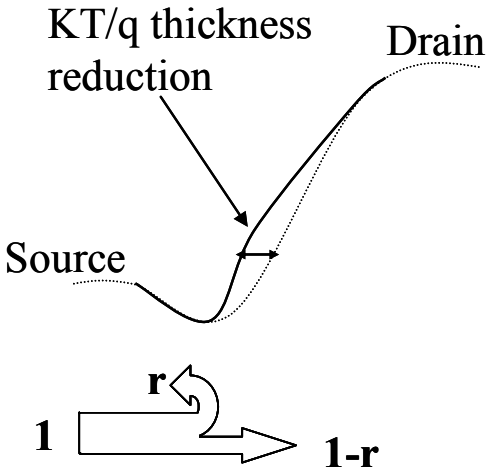


Fig. 3.30 Band diagram illustrates KT/q layer thickness reducing in 70% Ge channel of SGNW devices.

The solid line is corresponding to the hetero-structure while the dashed line is referring to the normal homo structure; for the same KT/q energy reduction, the hetero-structure exhibits barrier thickness lowering compared to the homo-structures. Besides the carrier injection investigation, channel mobility study can also be an important aspect for structure evaluation. However, in view of the reducing number of carriers (charge) in the channel or the reducing gate capacitance due to the small surface area of the nanowire

channel (CArea~ 3.14 x 350 nm ×13 nm), it is difficult to measure the gate capacitance using split C-V to extract the mobility of the SiGe nanowire. In fact, the nanowire channel capacitance is far smaller than the lower limit of any conventionally used standard ac bridge based instruments. Although it may not be very precise due to yield and variability issues, C-V measurements on multiple wire channel devices (500 to 1000 channels together) could have been a way out, but unfortunately, the mask used for fabricating these devices did not have such features. Use of the calculated capacitance value could have been another way but due to the involvement of high-k dielectric (precise k value unknown) and the rather complex Ω-shaped channel, the capacitance calculations might be far off from experimental value and thus lead to inaccuracies in mobility. To abstain from reporting inaccurate mobility numbers, we compared the linear transconductance to investigate the mobility difference between SGNW and planar devices as linear (low lateral field) transconductance which is directly proportional to mobility. It is found that the peak of linear G_m of SGNW is 4.5 times of that of planar devices. This enhancement is mainly attributed to two factors: First, with higher Ge concentration in the SGNW channel (70%) over planar channel (30%), hole mobility could be enhanced due to larger intrinsic hole mobility property of Ge. Besides, with the energy band modulation of SGNW, a valence band offset ΔE_V is formed from source to channel region which could further increase hole velocity due to the excess kinetic energy. Apart from these, there could also be some other factors accounting for the hole mobility enhancement of SGNW devices: Ω-shaped structure for better gate controllability; strain effect along the nanowire channel direction. Although it would be difficult to extract the mobility of the nanowire channel due to limitations in the measurement facilities and device layout designs, the mobility investigation of nanowire channel would be an interesting topic for future nano-scale devices explorations.

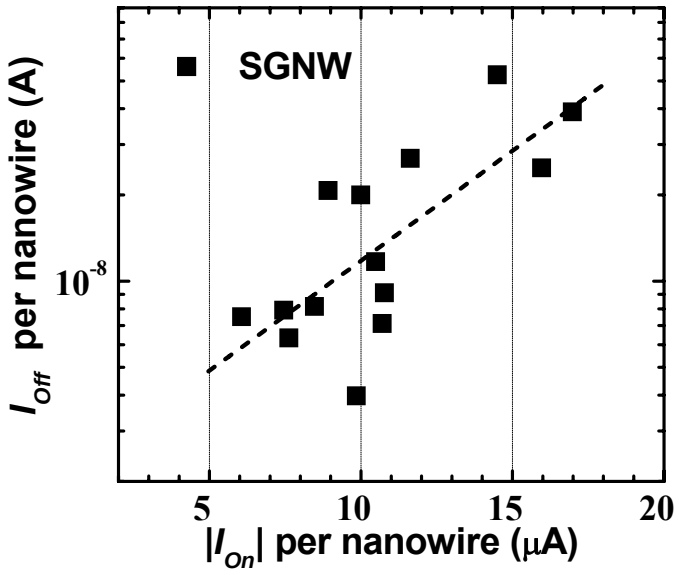


Fig. 3.31 I_{Off}–I_{On} plot for hetero SGNW devices (I_{Off} = I_{DS}@V_{GS} = +0.7 V, I_{On} = I_{DS}@V_{GS} = −0.7 V). A dashed line is linearly fitted to the data points. Improving process uniformity is likely to reduce the spread of data points.

The I_{Off}-I_{On} plot of the SGNW devices is shown in Fig. 3.31 (The selection of Vg to measure Ion and Ioff is dependent on the threshold voltages of the devices. The difference between Vg,on and Vg,off is dependent on the gate oxide thickness. Overall, the use of different Vg conditions for each chapter does not impact the validity of the results since the comparisons between experimental splits and control devices were only performed within each experiment using identical Vg conditions.). There is some spread in the data points which can be due to variability in threshold voltage, nanowire dimensions and Ge concentration. Improving the uniformity of lithographic fin widths, epitaxial SiGe thickness and concentration, and SOI thickness, is likely to reduce the variability in device performance.

3.5 Conclusion

In summary, Ge-rich (70%) strained SGNW was proposed and fabricated in this chapter. Pattern size dependent Ge condensation process was successfully developed to realize this structure with different Ge concentration in the channel and S/D regions. Significant improvement in G_m and drive current was observed compared to planar devices with uniform Ge%. Various possible factors for the enhanced performance were discussed. SGNW transistors were fabricated using a two-step pattern-size-dependent Ge condensation technique, which resulted in the formation of S-C-D hetero-structure. This reduced the hole KT/q barrier layer thickness from source to channel, which enhances the carrier injection from source to channel. This was confirmed by performing temperature dependent carrier backscattering characterization.

CHAPTER 4

4. CHANNEL ENGINEERING EXPLORATION (2) -SiGe/Si Core/Shell Nanowire FETs

4.1 Introduction

As discussed in previous chapter, the SiGe NW FETs as well as multi-stacked NW FETs are promising device architectures for high performance CMOS [134-137, 202] due to the better gate electrostatic control. Although higher hole mobility can be obtained from the SiGe channel, its gate oxide/SiGe interface exhibits a high interface trap density. To improve the interfacial quality between the SiGe channel and the gate dielectric, the incorporation of a thin Si capping layer can be a viable surface passivation method for the SiGe- and Ge-channel [203-208].

The SiGe/Si core/shell nanowire structure, thus, could be a promising candidate for high performance CMOS applications due to its better short channel control, lower interface trap density and higher hole mobility [209, 210]. Recently, SiGe NW transistors fabricated on SOI wafers by the Ge condensation method have been demonstrated using the top-down approach [195]. Nevertheless, SOI substrates are costly, prompting research efforts on integrating NW transistors on bulk Si substrates, which is, so far, limited to silicon nanowires [104, 116, 211]. A quantum confined SiGe nanowire channel covered with Si shell can be even promising for high performance pMOSFETs, which will take the advantages of both higher hole mobility and reduced interface traps.

In this chapter, uniaxially strained SiGe/Si core/shell p-MOSFETs were integrated on bulk Si substrates. In addition, the formation of a quantum confined SiGe nanowire channel device on bulk for high performance PMOSFETs was illustrated. Utilizing CMOS-compatible process, pFETs with nanowire like channels having ~12 nm SiGe NW core coated with a ~4 nm thick Si shell were fabricated with gate length down to 40 nm.

In the work described in this chapter, I gratefully acknowledge the help of P.C. Lim and S. Tripathy in XRD and UV Raman analysis. The use of the excellent facilities at IME is greatly appreciated. However, the ideas were conceived by me, and I have benefited through discussions with my mentors at IME, Dr. Navab Singh and Dr Patrick Lo. All the experiments were designed and executed by myself under the guidance of my mentors.

4.2 Device Fabrication

In this experiment, (100)-surface n^+ bulk Si wafers (ρ~0.001Ω.cm) with notches aligned to the <110> direction were used.

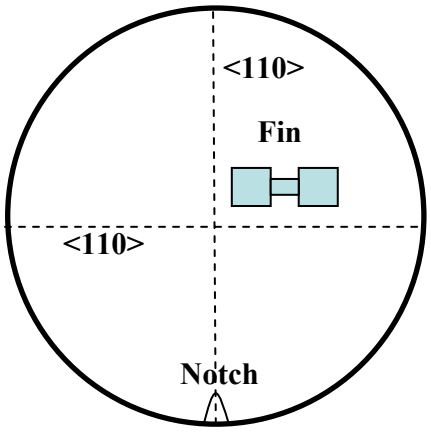


Fig. 4.1: Schematics illustrating the notch orientation and channel orientation fabricated in this work.

As illustrated in Fig. 4.1, the wafer we used is with a (100) surface and the notch indicating the <110> crystal orientation. The fins are etched perpendicular to the notch (indicated in the figures below), so the channel direction is <110> and the fin sidewalls orientation is (110). The key steps are schematically illustrated in Fig. 4.2

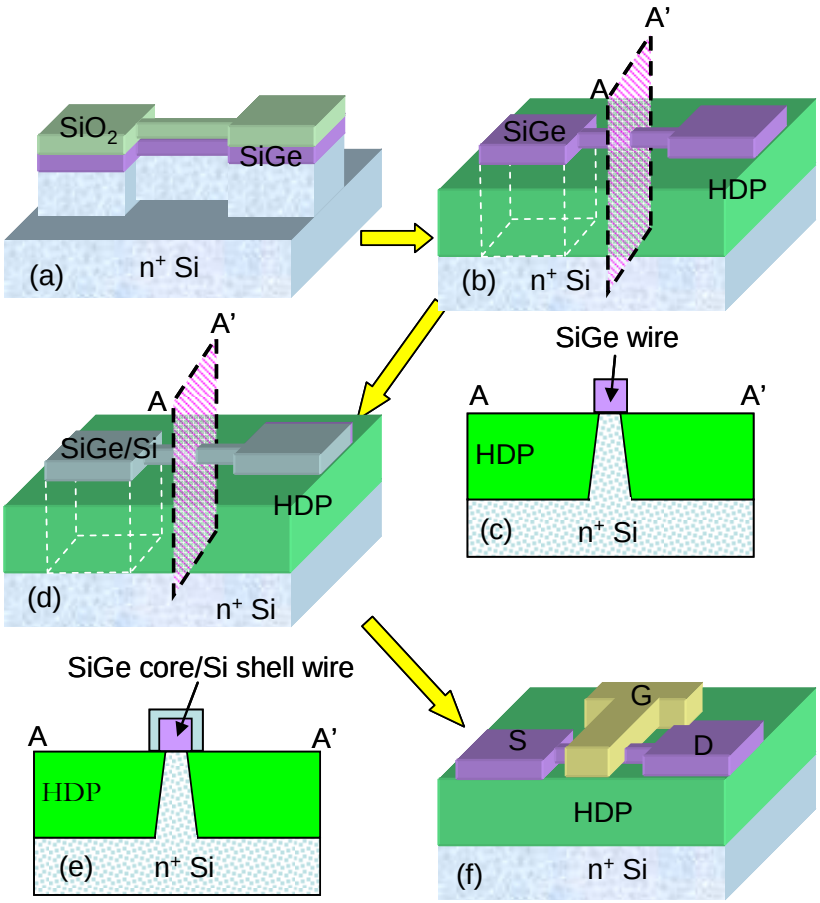


Fig. 4.2: Schematics of process flow illustrating the core/shell nanowire transistors fabrication.

After surface cleaning, a 25 nm thick $Si_{0.85}Ge_{0.15}$ was epitaxially deposited using an ultra-high vacuum chemical vapor deposition (UHVCVD) reactor at low temperature (~580ºC). For the control wafer, the epitaxial layer comprised 25 nm of Si instead. Both wafers went through the same processes subsequently. Epitaxy deposition was followed by 50 nm PECVD SiO_2 hard-mask deposition, high resolution patterning using alternating

phase shift mask with KrF (248 nm) lithography scanner, plasma photo-resist trimming, reactive ion etching of hard mask and hard-mask trimming processes to define fin patterns in hard-mask with critical dimensions about 12 nm. On the fabricated lines (length limited to channel length – small length) no obvious line edge and line width roughness were visible.

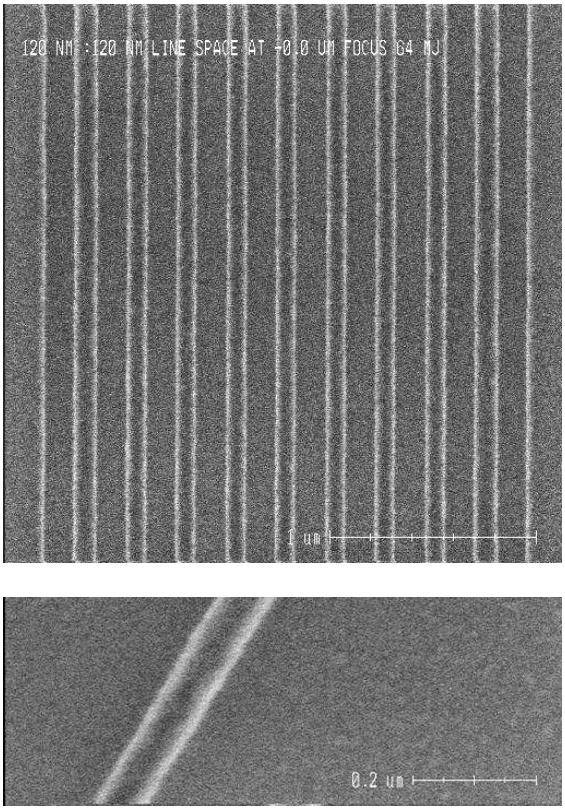


Fig. 4.3: Line/space patterns with printed line CD ~ 80 nm using alternating phase shift mask showing excellent line edge and line width uniformity. Bottom is a high zoom image taken at a rotation.

In fact not highlighted earlier, alternating phase shift mask was used to get very high resolution in patterning. The lithography process window was so large that with a thin high resolution resist layer (270 nm) we achieved lines almost free from line edge and line width roughness – shown in Fig.4.3. Both the photoresist trimming and hard-mask trimming processes have previously been observed to maintain or even slightly improve the edge and width roughness values.

The hard mask patterns were then transferred into wafer by etching 120 nm deep SiGe/Si using a plasma mixture of HBr and Cl_2 gases. SiGe and Si NW like structures were thus formed on different wafers on top of heavily doped silicon fins as shown in Fig. 4.2 (a). The wafers were then planarized using high density plasma (HDP) SiO_2 deposition and a time-controlled chemical mechanical polishing (CMP) process, leaving 500Å of oxide on top of wires. It was followed by recessing the HDP oxide in 1:25 DHF to selectively release the SiGe NWs out of oxide. The remaining HDP SiO_2 serves as the field isolation dielectric. The selective epitaxial growth of 6 nm Si as capping layer was then performed to passivate the surface of the SiGe NW channel, which effectively forms the SiGe/Si core/shell hetero-structure nanowire channel shown in Fig. 4.2 (d-e). The reference wafer was also processed through the Si-epitaxy process so that the physical channel thickness remains comparable. Fig. 4.4 illustrates the channel cross-section of the SiGe/Si core shell and Si reference device structure. The nanowire-like structure became SiGe core/Si shell one the SiGe wafer while remaining as pure silicon on the reference Si wafer. In both the cases device channels are physically connected on to the highly doped bottom substrate. The only difference between the SiGe and the reference Si wafer is the core channel's material (SiGe vs. Si).

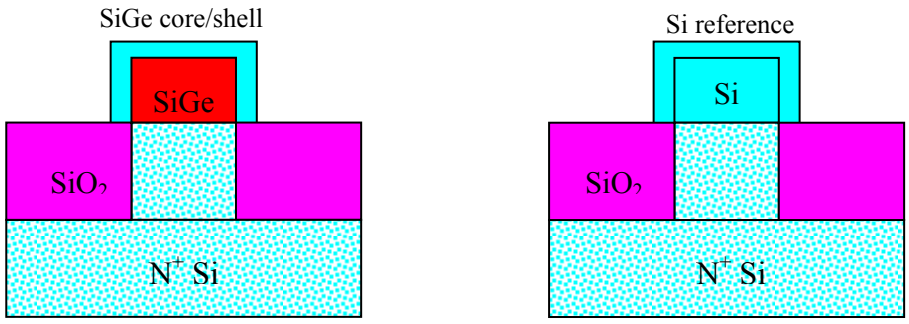


Fig. 4.4: Schematics illustrating the channel cross section. For the SiGe wafer, after Si epitaxy, a core/shell structure formed on top of the n^+ Si pillar while the reference wafer remains Si on top of n^+ Si pillar. The channel widths are comparable for two kinds of devices.

It is worth mentioning here, for a rectangular nanowire, with (110) sidewall surface orientation and (100) top surface orientation, the Si epitaxial growth rates will be different. The gate stack was formed with 4 nm SiO_2 thermally grown at 800ºC followed by 60 nm amorphous-Si deposition. Again, due to the difference in surface orientation, thermal oxide thickness will be slightly different. Nevertheless, the electrical effects are expected to be minimal. Next, gate lengths down to 40nm were defined using a similar scheme of patterning and trimming to that previously used to define the NWs. After LDD implantation (Boron: 6×10^{13} cm^{-2}), 40 nm wide nitride spacers were formed to protect the NW source/drain (S/D) extensions from silicidation, preventing excessive lateral silicide encroachment. This was followed by S/D implantation (Boron: $4\times10^{15}cm^{-2}$) and activation (~875ºC). The S/D germanium-silicidation process involved 4 nm of deposited Ni to form the $Ni_xSi_yGe_{1-x-y}$ salicide S/D contacts, which reduces the series resistances. The device fabrication was completed after pre-metal dielectric deposition, contact formation, and metallization processes.

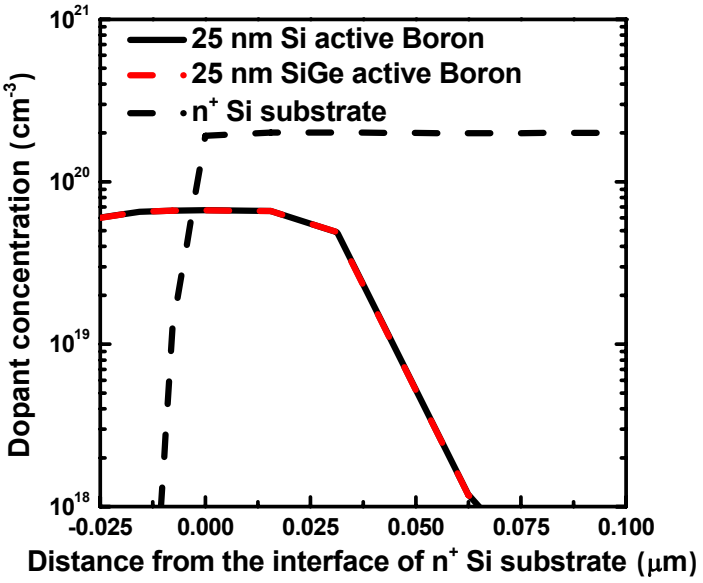


Fig. 4.5: TCAD simulations of the S/D implantation profile for SiGe and Si wafers separately. Comparable dopant concentration profile is observed.

It should be noted that the implantation profile may be slightly different between the SiGe and Si wafer although the same energy and dose were used. TCAD simulations to investigate the S/D implantation profile for SiGe and Si wafers separately. Both wafers received same implantation energy and dose condition ($2\times10^{15}cm^{-2}$). The dopant diffusion profile shown in Fig. 4.5 indicates that there is little difference between the doping profiles for SiGe and Si wafers. This is likely to be due to the low Ge concentration and low activation thermal budget.

4.3 Results and Discussions

4.3.1 SEM Analysis of Core/Shell NW Structures

Fig. 4.6 (a) shows a SEM image of a released SiGe NW with HDP oxide covering the field area. Selective epitaxial growth of Si was then performed to passivate the SiGe NW channel surface, forming the SiGe/Si core/shell heterostructure. Fig. 4.6 (b) shows the SEM micrograph after the gate etching process, which produced gate lengths down to 40 nm without parasitic gate stringers.

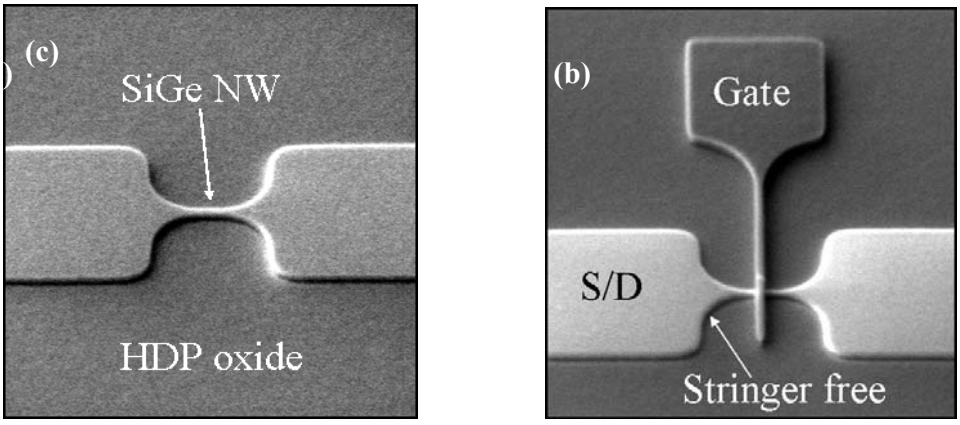


Fig. 4.6: (a) SEM image after CMP process & SiGe NW release (b) SEM image after gate pattern transfer. Gate lengths L_G down to ~40nm were formed. Parasitic gate stringers were removed. (c) SEM image of NW device after spacer formation. (d) SEM images after metal contact etching process.

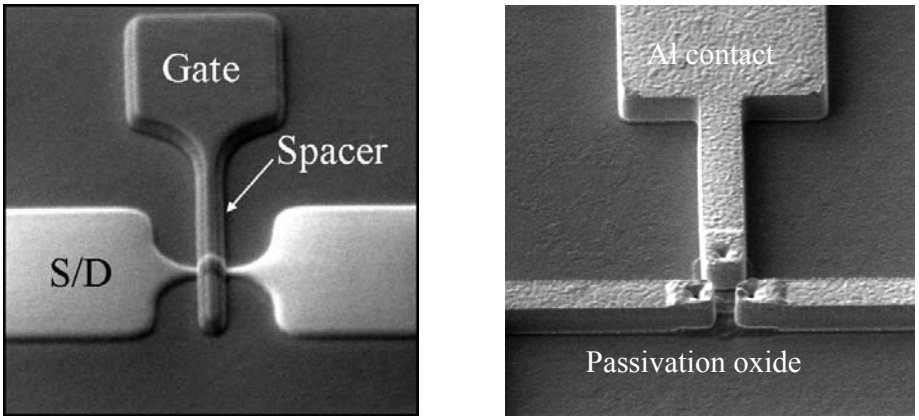


Fig. 4.6: (c) SEM image of NW device after spacer formation. (d) SEM images after metal contact etching process.

Fig. 4.6 (c) shows the SEM image after spacer formation prior to S/D silicidation. The 40 nm-wide nitride spacers protect the NW S/D extensions from silicidation, preventing excessive lateral silicide encroachment. Fig. 4.6 (d) shows the SEM image after contacts formations. Al contacts were used for the contact metal line in this work.

4.3.2 SiGe Epitaxy Film Study and Core/Shell Structure

Fig. 4.7 shows the (004) and (224) XRD reciprocal space maps of a SiGe/Si mesa region, revealing excellent alignment of the (15%) SiGe and Si intensity peaks. This illustrates lattice alignment across the heterojunction as a result of the pseudomorphic epitaxial growth. The high resolution XRD rocking curve in Fig. 4.8 shows well-defined SiGe peaks and indicates high SiGe crystalline quality.

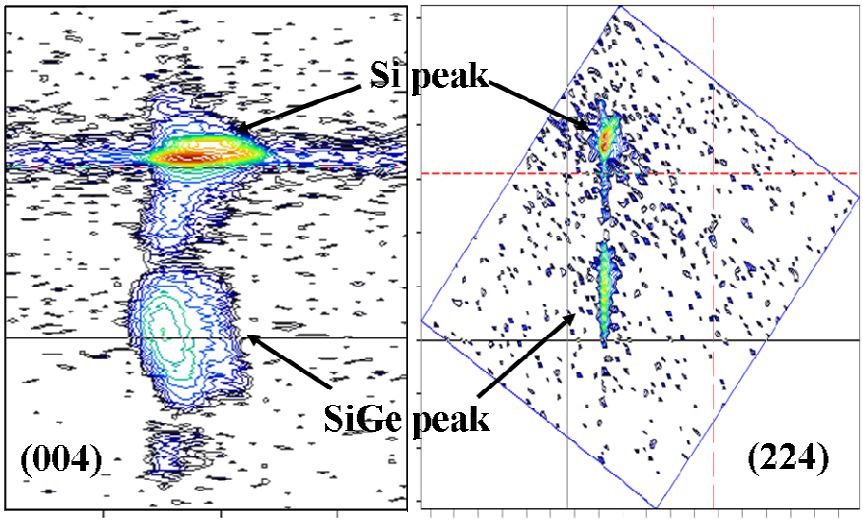


Fig. 4.7: (004) and (224) reciprocal space maps show excellent alignment between the SiGe and Si peaks, indicating pseudomorphic epitaxial growth. The SiGe film and the Si substrate have similar in-plane lattice constants.

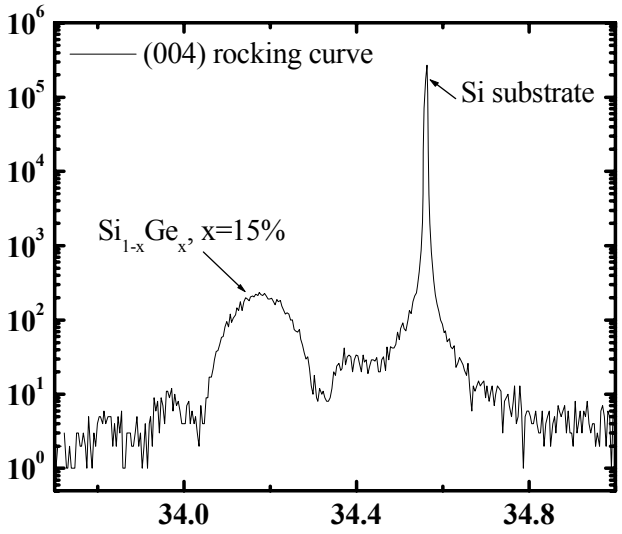


Fig. 4.8: High resolution XRD rocking curve shows excellent crystalline quality of 15% SiGe film grown pseudo-morphically on the bulk Si substrate.

UV Raman analysis was also performed on the thin SiGe film for strain metrology. The Raman peak for Si-Si in SiGe film, together with a reference Si-Si peak from a blanket Si wafer, is shown in Fig. 4.9.

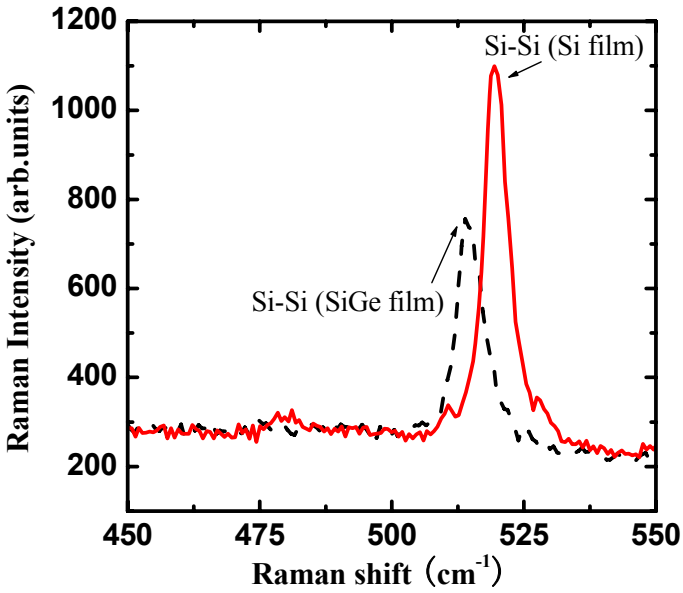


Fig. 4.9: High resolution XRD rocking curve shows excellent crystalline quality of 15% SiGe film grown pseudo-morphically on the bulk Si substrate.

The blue shift of the Si-Si peak ($514cm^{-1}$) is proportional to the compressive strain in SiGe film. The strain in the SiGe film was calculated to be -0.5% (compressive). When the SiGe NW is formed by the etch process, anisotropic strain relaxation results in a uniaxial compressive strain in the longitudinal direction, as opposed to biaxial strain, due to the small lateral dimension of the SiGe NWs [212, 213]. Uniaxial compressive strain causes valence band deformation, reduces the conductivity effective masses and enhances the hole mobility. Due to the core/shell structure, quantum confinement of holes in the SiGe NW channel helps to fully reap the mobility enhancement benefits.

4.3.3 TEM Analysis of the Core/Shell Structure

Fig. 4.10 is the cross-section TEM micrograph of the channel. The SiGe/Si core/shell heterostructure can clearly be seen in the high magnification view (inset). The 12 nm-wide SiGe core is covered by a 4 nm-thick Si shell, a 4 nm-thick SiO_2 gate oxide

and a 60 nm-thick poly-Si gate layer. HDP silicon oxide is used as the isolation dielectric. It is expected that further process development in etching process could form a floating body SiGe nanowire for gate all around structure.

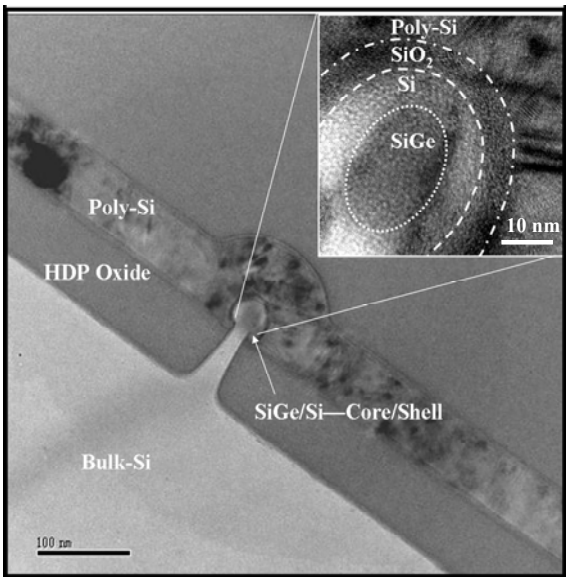


Fig. 4.10: TEM micrograph of channel cross-section with SiGe/Si Core/Shell.

4.3.4 Electrical Characteristics of the Core/Shell Structure

The I_D-V_G transfer characteristics of a SiGe/Si core/shell hetero-junction nanowire FET with a gate length of 40 nm are shown in Fig. 4.11. The drain current is normalized by the channel perimeter of ~78nm, i.e., (top surface 12 + 4 + 4 nm) + 2 × (sidewalls 25 + 4 nm). Low subthreshold swing of 128mV/decade confirms the effectiveness of the Si surface passivation for such SiGe channel devices. However, there might be still some Ge out-diffusion to the oxide interface which creates interface traps. The device also exhibits reasonable drain-induced barrier lowering (DIBL) of 148 mV/V. These parameters show good electrostatic control of the channel in spite of the short gate length and relatively thick gate oxide of 4 nm. Due to the valence band offsets between Si and SiGe, quantum confinement of holes is expected for the SiGe/Si core/shell hetero-structure channel

during FET operation. These parameters show that, in spite of the short gate length and relatively thick gate oxide of 4 nm, good electrostatic control of the channel was still maintained.

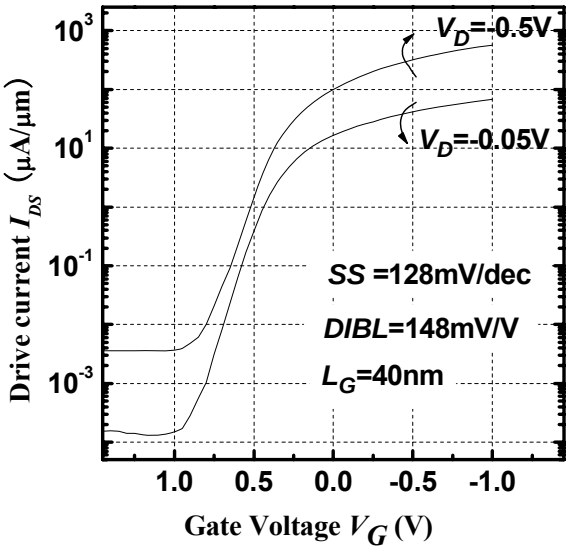


Fig. 4.11: I_D-V_G transfer characteristic of typical NW devices for gate length of 40 nm. Reasonable short channel control was maintained despite the thick gate oxide.

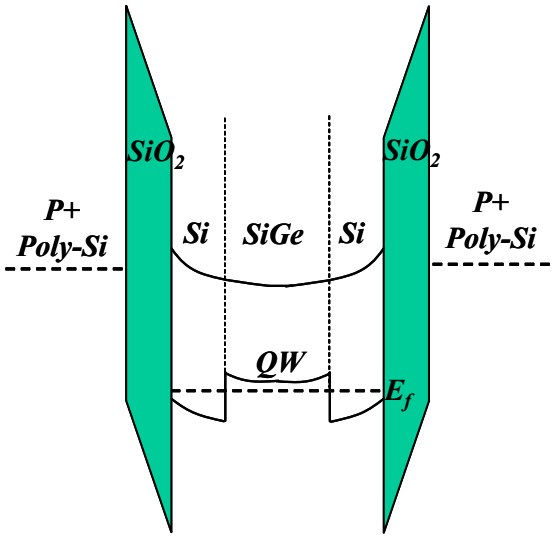


Fig. 4.12: Band diagram schematic (not to scale) of channel cross section of SiGe/Si Core/Shell structure. The hole quantum well (QW) in the strained SiGe region is illustrated.

Quantum confinement of holes is expected for the SiGe/Si core/shell heterostructure channel during FET operation. Fig. 4.12 shows a band diagram schematic

of the heterostructure nanowire channel, which schematically illustrates the cause of this quantum confinement as a result of the valence band offset. This valence band offset is due to the smaller intrinsic bandgap of the SiGe core. It is possible that the uniaxial strain-induced bandgap narrowing further contributes to the degree of valence band offset [214], making the quantum confinement even more pronounced.

The heterostructure NW FET is expected to exhibit two kinds of channel conducting mechanisms. Holes are largely confined to the SiGe core at low gate overdrive voltages. At higher gate overdrive voltages, surface inversion in the Si shell starts to occur. This existence of this effect is confirmed by the linear transconductance G_m plot as shown in Fig. 4.13. Two G_m peaks were observed, which concurs with similar observations made of SiGe quantum-well planar FETs in [215]. The first peak corresponds to conduction in the SiGe core while the second peak corresponds to surface conduction in the Si shell. It should be noted that the degree of quantum confinement can be adjusted by tuning the Ge concentration in the SiGe core.

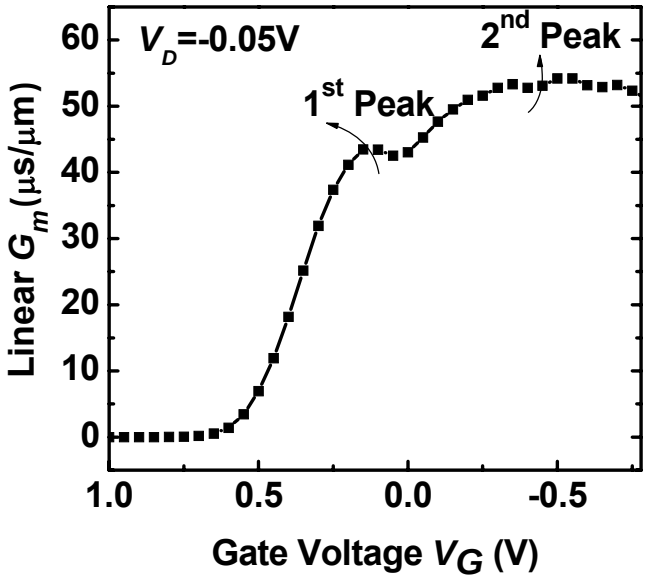


Fig. 4.13: Linear G_m characteristic shows two G_m peaks, which corresponds to SiGe (core) and Si (shell) channel conduction.

The I_D-V_D characteristics of the same device are shown in Fig. 4.14. The normalized drive current is ~167 μA/μm at V_G-V_T = -1.0V. The characteristics of Si reference control device are also presented in Fig. 4.14. A 15% I_{Dsat} enhancement is achieved over control Si reference devices. The high drive current is likely to be a result of the enhanced hole mobility in the uniaxially strained SiGe quantum well nanowire channel. There are two effects contributing the hole mobility enhancement: (1) 15% SiGe has a higher intrinsic hole mobility than Si, (2) Due to uniaxial compressive strain in the SiGe channel, the hole mobility will be enhanced further. However, it would be difficult to decouple the two effects.

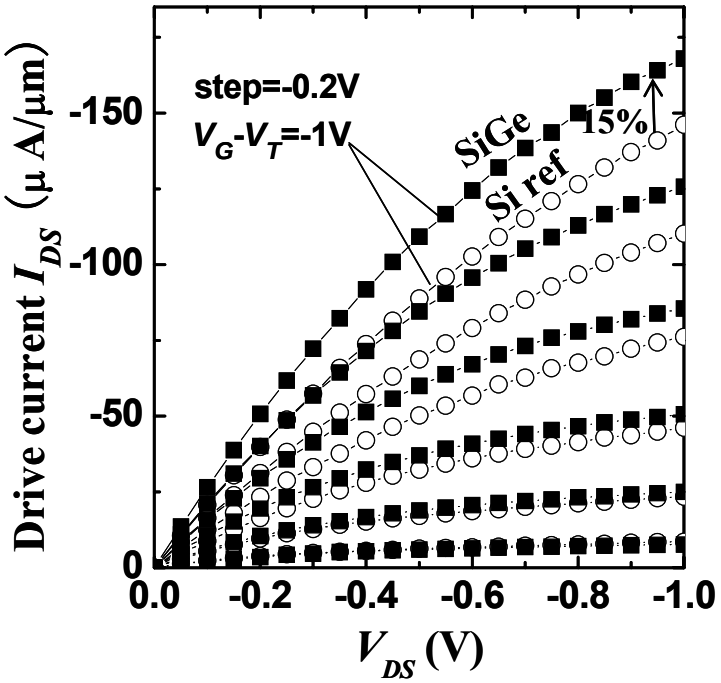


Fig. 4.14: I_D-V_D family of curves of the same device. The normalized drive current of Si/SiGe nanowire device is 167μA/μm at V_G-V_T=-1V. A 15% enhancement is observed for the core/shell devices compared to the Si reference devices.

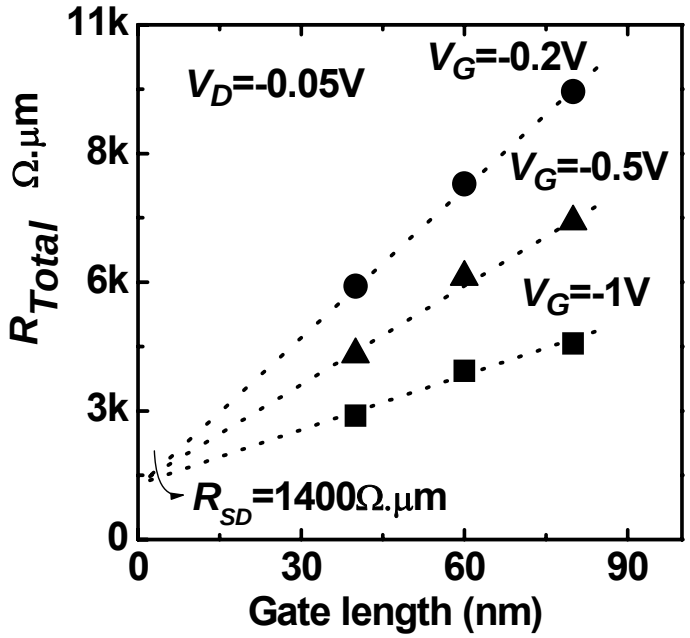


Fig. 4.15: Total resistance as a function of gate gate length for three gate bias voltages. S/D series resistance R_{SD} is estimated to be about 1400 Ωμm.

Fig. 4.15 plots the total resistance as a function of gate length for three gate bias voltages. The S/D series resistance was estimated to be about 1400 Ωμm, which is higher than that of state-of-the-art planar devices. It is likely that even better absolute drive current performance can be obtained through the careful optimization of the S/D extensions implants and the dopant profile engineering at the silicon-silicide interface.

4.3.4 Challenges of the Core/Shell Structure Process

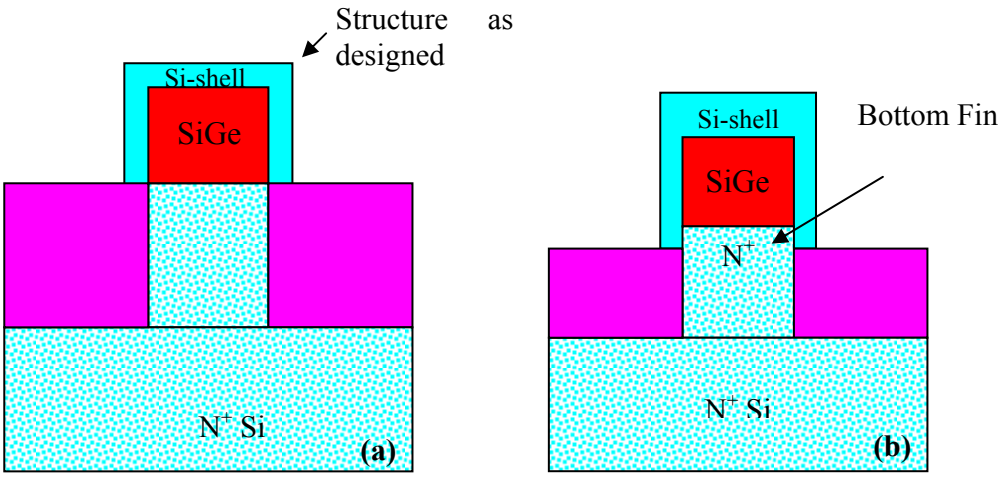


Fig. 4.16: (a) cross section of the core/shell structure as designed. (b) Cross section of the structure due to over etching process happened and bottom fin exposed.

Due to the non-uniformity of the process, there will be some process variations for the individual devices. Hence, there might be possible that the fabricated device structure would not be the same as the designed ones. As shown in Fig. 4.16 (a) is the cross section of the designed core/shell structure. Under the circumstance that there will be some over etching happening during the SiGe NW release process. The bottom Si fin would be exposed in a certain depth (<10nm), as indicated in Fig. 4.16 (b). We consider the width of the bottom Fin is ~10nm, however, even if this is the case, due to lack of gate controllability (fringing fields only) and high channel doping, this parasitic channel will have a much higher threshold voltage.

The doping concentration of the parasitic channel beneath the NW channel is estimated to be about 8×10^{19} cm^{-3} from the resistivity value. Based on the equation (4.1) for the channels with different channel doping, due to this high doping concentration, it was calculated that the threshold voltage of the parasitic channel will be much larger than 5 V. This means that for normal device operation, the parasitic channel will not be turned on and can be neglected.

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_s q N_a (2\Phi_F + V_{SB})}}{C_{ox}} \qquad (4.1)$$

Thus it would have a negligible contribution to the total device current during device operation. Even for the unlikely case that the parasitic channel inverts, it is unlikely that a distinct G_m peak corresponding to this inversion can be observed due to its minute current compared to the overall device current, unlike that for the Si shell's inversion.

4.4 Conclusions

Strained SiGe/Si core/shell NW pFETs with $Ni_xSi_yGe_{1-x-y}$ S/D contacts integrated on bulk Si substrates were demonstrated in this chapter. The width of the SiGe NW core is 12 nm with a Si shell of 4 nm. Good short channel performance has been achieved with low subthreshold swing (128 mV/dec) and DIBL, with drive currents of up to ~167 μA/μm. The fabrication scheme for the core/shell structure formation allows for further scalability by increasing the Ge concentration in the SiGe core during epitaxial growth, which can result in greater hole confinement and further improved hole mobility.

CHAPTER 5

5. SOURCE AND DRAIN ENGINEERING IN GAA NANOWIRE FETs FOR HIGH PERFORMANCE APPLICATION

5.1 Introduction

Gate-All-Around (GAA) silicon nanowire (SiNW) transistors are considered to be one of the most promising candidates for high performance and low power device applications owing to its superior short channel controllability [75, 116, 128, 142, 211, 216-218]. While electrostatic gate control improves as channel body dimension shrinks, high series resistance arises due to the narrow nanowire source and drain (S/D) regions, which pathologically limit the drive current performance [147, 148, 219-222]. In the ultra-short channel nanowire transistors, the adjoining source and drain regions - doped semiconductor nanowires which have comparatively large lengths, contribute significantly to the S/D series resistances, and form a large fraction of the total resistance.

In this chapter, the effect of parasitic series resistance on the performance of NW transistors is addressed. N-channel transistors were chosen as the test vehicles for this study since the impact of series resistance on n-channel transistors is greater than that on p-channel transistors. This is due to the higher electron mobility than hole mobility, which leads to a smaller channel resistance in the n-channel transistor. As such, the parasitic series resistance in the n-channel transistor is a larger fraction of the total resistance, making it a performance bottleneck for the n-channel transistor.

In order to obtain high performance in the ultra-short channel nanowire devices, silicide engineering on nanowire contacts in the S/D extension regions need to be optimized. However, the silicide formation for nanowire is a volume effect rather than a surface effect only, which leads to fast lateral silicidation effect and more substantial portion of the semiconductor nanowire being converted into metal silicide nanowire [223-225]. Unlike the conventional transistor silicidation processes, an optimized design of salicided nanowire contact for ultra scaled GAA FETs is yet to be demonstrated.

Fig. 5.1 shows the ratio of the external resistance over channel resistance at different technology node [226]. The historical ratio of the external resistance over channel resistance is 20%. R_{ext} is defined as the lumped external resistance component, and can be estimated from the linear region I_D-V_G characteristics at high gate overdrive voltages. $R_{channel}$ refers to the "on"-state channel resistance, and can be obtained by subtracting R_{ext} from the total resistance obtained at the corresponding gate voltage for "on"-state operation at each specific technology node. As the gate length scales, the channel resistance reduces significantly, thus the external resistance contribute large part on the total resistance which limits the drive current. It is necessary to reduce the external resistance for the nanowire transistor so as to improve the performance.

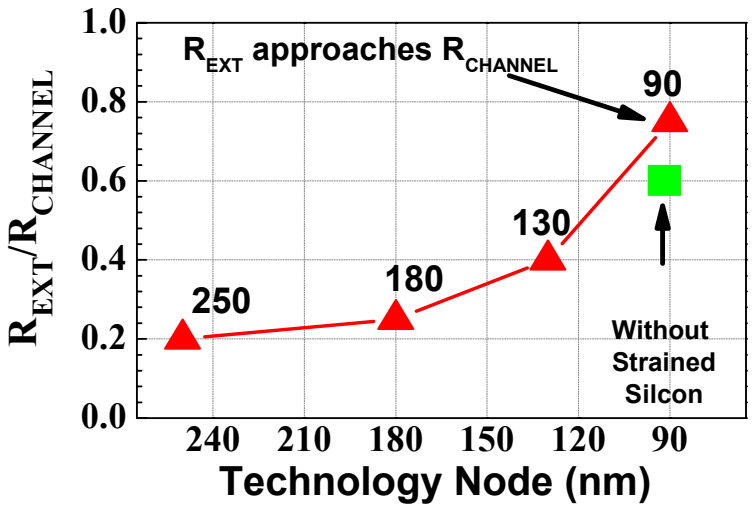


Fig. 5.1: Ratio of external resistance over channel resistance at different technology node. The historical ratio is 20%.

In this chapter, ultra-thin Ni silicide films of different Ni deposition thickness have been investigated for 10nm diameter nanowire devices. Low resistivity metallic nanowires source/drain (S/D) extensions has been demonstrated successfully for the first time with ultra scaled GAA FETs suitable for 22 nm technology node and below. Significant enhancement in drive current has been achieved for L_G = 8 nm Si GAA NW transistors with optimized NiSi nanowire contact.

In the work described in this chapter, I gratefully acknowledge the help of L. H. Tan of the Institute of Microelectronics in the cross-sectional TEM imaging. Dr. T. Y. Liow also gave valuable suggestions on the gate etching process. The use of the excellent facilities at IME is greatly appreciated. However, the ideas were conceived by me, and I have benefited through discussions with my mentors at IME, Dr. Navab Singh and Dr Patrick Lo. All the experiments were designed and executed by myself under the guidance of my mentors.

5.2 Material Investigation

The Ni silicidation process for nanowire transistors is a critical step. Deposition of a too thick Ni film can result in device shorts due to excessive lateral silicide encroachment [225, 227] while a too thin layer may not meet the high performance logic requirement as NiSi resistivity is a function of its thickness [228-230]. In this experiment, ultra-thin Ni films of 1 to 4 nm were deposited on Si substrates in a physical vapor deposition (PVD) system and annealed in a single wafer rapid thermal furnace to form Ni silicide films. For depositing ultra thin Ni films, we have utilized Anelva PVD system, which was designed specially for ultra thin film deposition. The deposition rate for Ni was about 1A/sec. Thus, a uniform Ni deposition layer can be obtained. In order to test the uniformity for the formed thin Ni_xSi_y film, we investigated the sheet resistance standard deviation value. The sheet resistance value we chose was the average value of 48 points across the wafer. The standard deviation value for the sheet resistance provides further information on the film uniformity. Even for the Ni deposition thickness of 1nm, 2nm, the deviation value for the sheet resistance of Ni_xSi_y film were 1.454% and 1,147% respectively, this confirmed the uniformity for the ultra thin Ni silicide film. Next, the silicidation process was performed at a slightly lower temperature and such agglomeration can be reduced. The formation temperature for our experiment is 400°C for 300 seconds.

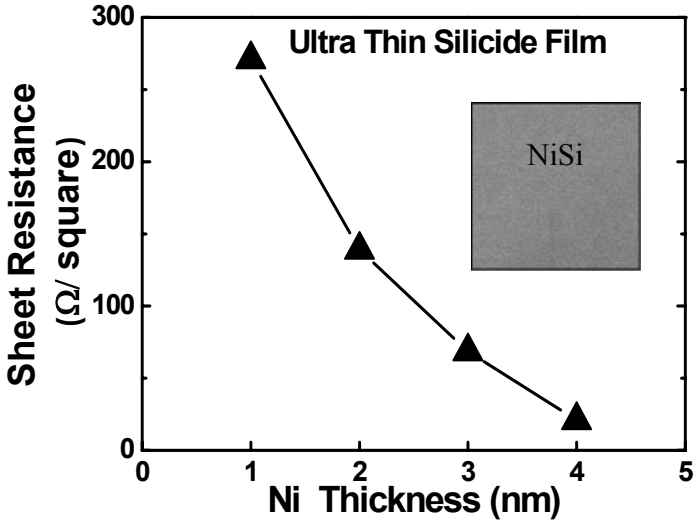


Fig. 5.2: Sheet resistance values as a function of deposited Ni thickness for ultra thin silicide film. The sheet resistance value chosen is the average value of 48 points across the wafer. Inset is the SEM images of the 4 nm Ni deposited NiSi film.

Sheet resistance drops significantly (from 270Ω/square to 20Ω/square) as Ni thickness increased from 1 nm to 4 nm as shown in Fig. 5.2. The inset is the SEM images of the Ni_xSi_y film. There is no agglomeration observed.

In order to extract the resistivity for the thin Ni_xSi_y film, we first performed TEM analysis for the 4 kinds of Ni deposition thickness to explore the thickness of the forming NiSi film. Through the absolute standard deviation value, it is expected that the formed NiSi film is uniform, thus the measured Ni_xSi_y film thickness can be used for the resistivity extraction.

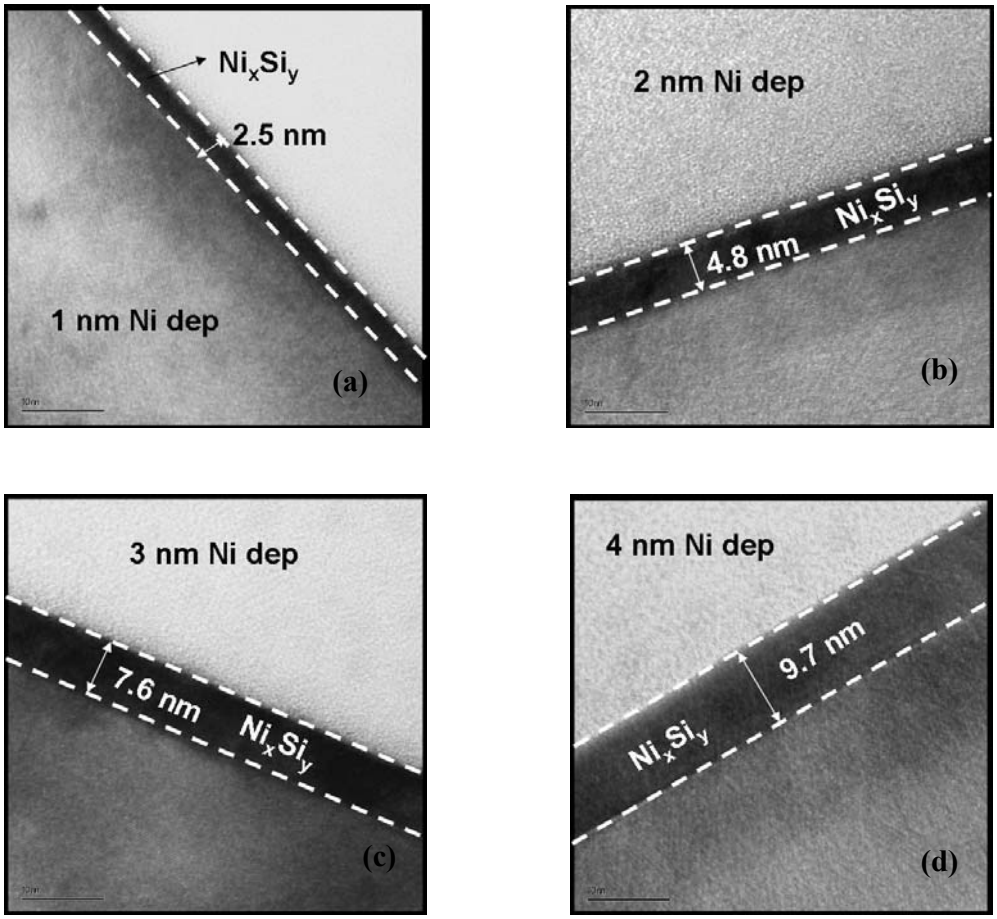


Fig. 5.3: HRTEM micrographs for the thin Ni_xSi_y film with Ni deposition thicknesses from 1 nm to 4 nm. The formed Ni_xSi_y thicknesses are indicated in the figures.

The samples with Ni deposited thickness of 1 nm, 2nm, 3nm, and 4 nm were performed for TEM analysis and the HRTEM images are shown in Fig.5.3 (a)-(d). The formed Ni silicide film thicknesses are 2.5nm, 4.8nm, 7.6nm, and 9.7nm.

Instead of using the same volume conversion assumption, we used the measured value for the resistivity extraction. The resistivity values versus NiSi thickness is plotted in Fig. 5.4 which is extended towards thicker film using ref. [231]. It was observed that the Ni silicide films corresponding to 4 nm Ni deposition thickness have resistivity values ~20 μΩ.cm which are higher, but close to that of thick NiSi films (T_{NiSi} >25nm). For silicide films corresponding to 1 to 3 nm of Ni deposition thickness, the resistivity values for all three thicknesses were above 60μΩ.cm.

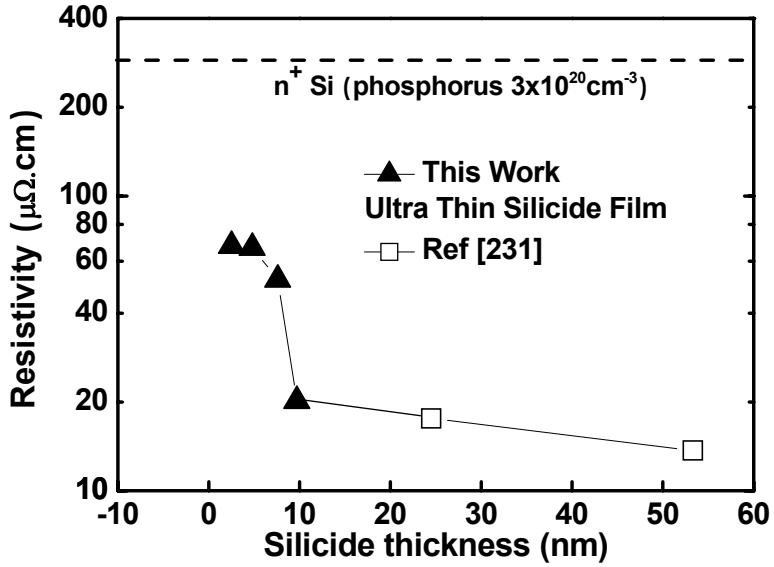


Fig. 5.4: Resistivity values as a function of silicide thickness which further expands of ref. [231] work (open symbols) to thinner silicide thickness region with highly doped Si as dashed line. The resistivity increases significantly when the silicide thickness is below 9.7nm.

For thin metal films, the increase in resistivity with decreasing film thickness has been attributed to thickness dependent surface scattering mechanisms such as electron-surface scattering, surface roughness induced scattering and grain boundary scattering [232-234]. This can possibly account for the increase in nickel silicide resistivity below a film thickness of 5 to 6 nm (~mean free path of electron in NiSi). Besides the surface scattering effect, there might also be other possible reasons for the high resistivity.

We did XRD phase analysis for these ultra-thin Ni_xSi_y films with Ni deposited thickness of 2 nm, 4 nm respectively. By utilizing GADDS (General Area Detector Diffraction System), with the incidence of 6º for 1800s wide-angle scan, the XRD results are showing in Fig. 5.5:

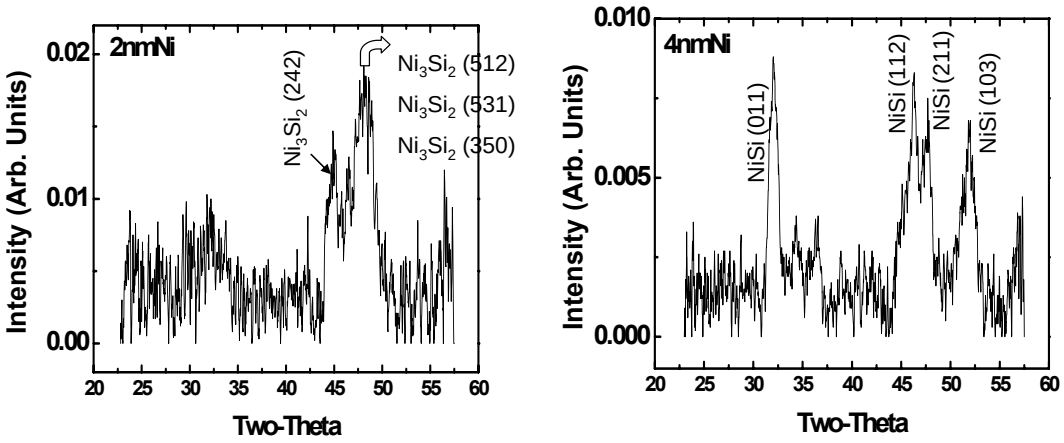


Fig. 5.5: XRD phase analysis for the ultra thin Ni_xSi_y film with Ni deposition thickness of 2 nm and 4 nm, respectively. The 2 nm Ni deposition thickness fits well with the Ni_3Si_2 phase (a) while the 4 nm Ni deposition thickness fits well with the NiSi phase (b).

Based on the XRD data, the 2 nm Ni thickness in Fig. 5.5 (a) fits well with the phase of Ni_3Si_2, which is indicated inside the figures, while the 4 nm in Fig. 5.5 (b) fits well with the phase of the NiSi. Thus, from the XRD, the phase difference could also be a possible reason accounting for the high resistivity. However, it should be noted that the thin film layer would suffer from strong mechanical stress, which can complicate the XRD analysis or affect the accuracy of the XRD analysis.

It is observed that such resistivity values are still much less than that of highly doped Si with phosphorus dopant $3\times 10^{20}cm^{-3}$ (dashed line in Fig. 5.4). Moreover, from the equation (4.1)

$$R = \rho \frac{l}{t_{NiSi} \cdot W} \qquad (5.1)$$

calculations show that even 4.8 nm of Ni_xSi_y film can theoretically reduce the series resistance contribution for 150 nm long nanowire S/D regions to less than 12kΩ for both sides, which is still acceptable for nanowire diameter scaling down to 5 nm. Due to the low resistivity value and thickness matching for nanowire diameter, in this work, 4 nm Ni was used to form metallic nanowire contacts.

In our experiment, all splits (control and NiSi S/D) underwent the same 950°C spike anneal after S/D implantation. Subsequently, the silicidation splits was silicided using 4 nm as deposited Ni thickness and annealed at 400°C in a single wafer rapid thermal furnace for 120s. The choice of this Ni thickness is thin enough to avoid "over-silicidation" of the nanowire S/D regions, which would otherwise result in excessive lateral silicide encroachment similar to that observed in [225].

We also performed high angle annular dark field STEM study on the ultra thin Ni_xSi_y film down to 2 nm which is from 1 nm Ni deposited film. Fig.5.6 shows an interesting phenomenon in which the lattice structure of the Si continues into the formed NiSi film, like a single crystalline structure. However, the properties of this thin NiSi film has not been investigated comprehensively, it need further detail exploration in order to understand the origin of this phenomenon.

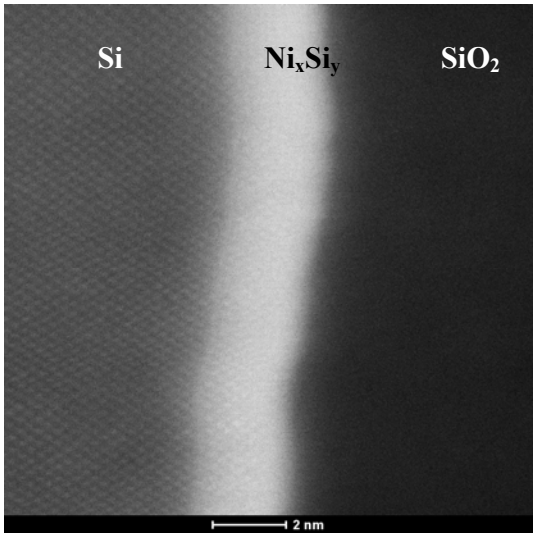


Fig. 5.6: STEM image of the ultra thin Ni_xSi_y formed from 1 nm Ni deposition thickness. The Si lattice structure keeps continuing towards the Ni_xSi_y film.

5.3 Device Fabrication

N-channel GAA SiNW transistors were fabricated similarly as reported in [75]. Firstly, thin down the SOI top Si thickness to 30 nm by dry oxidation process. Next, Si Fin structures down to 40nm are patterned on thin SOI wafers (Tsi=30nm) using deep UV lithography, trimming and etching processes. By thermal oxidation, nanowire diameters were further trimmed down to ~10nm. Fig. 5.7 (a) shows an SEM image of a released nanowire. Next, ~4nm grown SiO_2 was used as the gate dielectric followed by 60 nm poly-Si gate deposition, implantation, and activation. Poly-silicon gates down to less than 10nm were defined using a combination of photoresist trimming and gate hard mask wet trimming process. Fig. 5.7 (b) shows a SEM images after gate etching process. The arrows indicate the silicidation area and the circle suggests the metallic nanowire contact formation region.

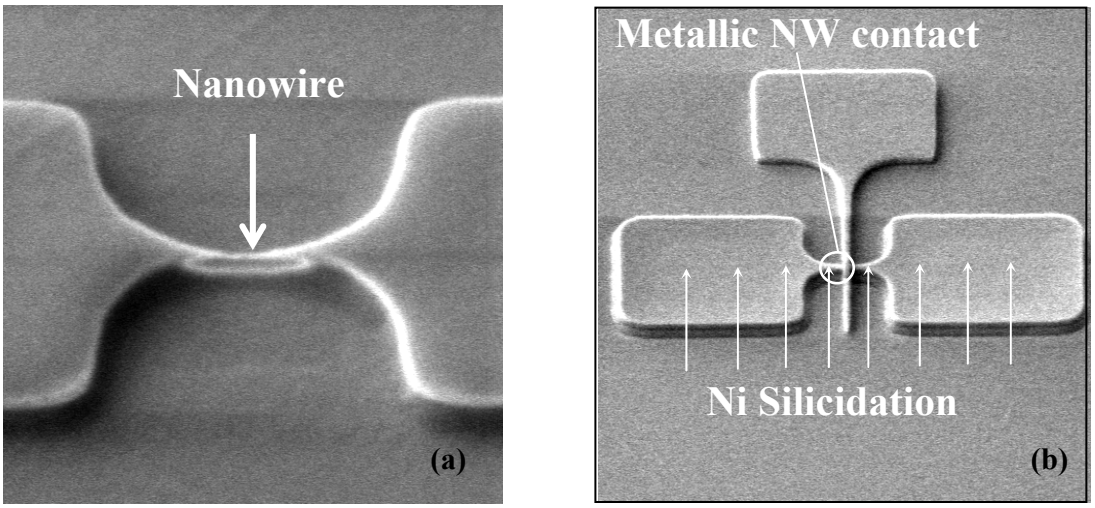


Fig. 5.7: (a) SEM image after Si NW release (b) SEM image after gate etch. Arrows indicate nanowire and pad Silicidation. The circle shows the nanowire contact regions.

After gate formation, LDD implantation (As: 3 $\times 10^{13}$ cm^{-2}) was performed after depositing a 10 nm-thick SiO_2 liner oxide offset for a slight gate under lap. Although the poly-silicon below the nanowire could not be etched completely and might results in large

overlap capacitance, the effective channel length controlled by etched gate length on top of the nanowire channel, could be achieved down to 8 nm. As shown in Fig. 5.8 the HRTEM image for planar transistors with the same gate length and pattern profile as the nanowire transistors. The smallest gate length achieved in this work is down to as small as 8 nm. The zoom out view of the HRTEM image is shown as the inset of Fig. 5.8. The linear oxide and spacer profile can be seen clearly with an Etch-Stop-Layer (ESL) of SiN covered on top of the gate region. The reasons for the ESL will be explained later.

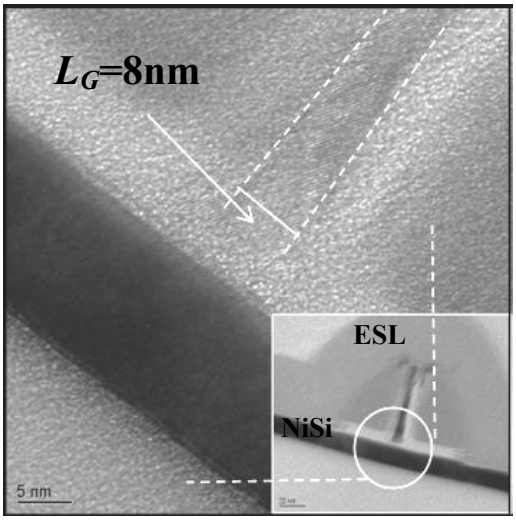


Fig. 5.8: HRTEM image of gate structure cross-section, gate length is ~8nm. Inset shows zoom out view of gate structure, with ESL as etching stop layer.

Next, 40 nm nitride was deposited for spacer formation, and followed by P^+ implant (P: $1\times10^{15}cm^{-2}$) as deep S/D implantation and spike anneal at 950 ºC. Low resistivity NiSi nanowire contacts to the nanowire S/D extensions were formed using an optimized silicidation process; for comparison, a control wafer was skipped this silicidation process. Further, 40 nm nitride layer was deposited as Contact-Etch-Stop-Layer (CESL) for ultra-thin S/D contact etching process. Process was completed by standard backend contact and metallization processes. Fig. 5.9 (a) is TEM micrograph of the channel cross section for a complete SiNW device with HRTEM image of nanowire shown in Fig. 5.9 (b). The 10 nm SiNW is surrounded by 4 nm SiO_2 followed by 60 nm

poly-Si. ESL is covered on top of the poly-Si gate stack which is served as etching stop layer for the ultra thin contact via etching process.

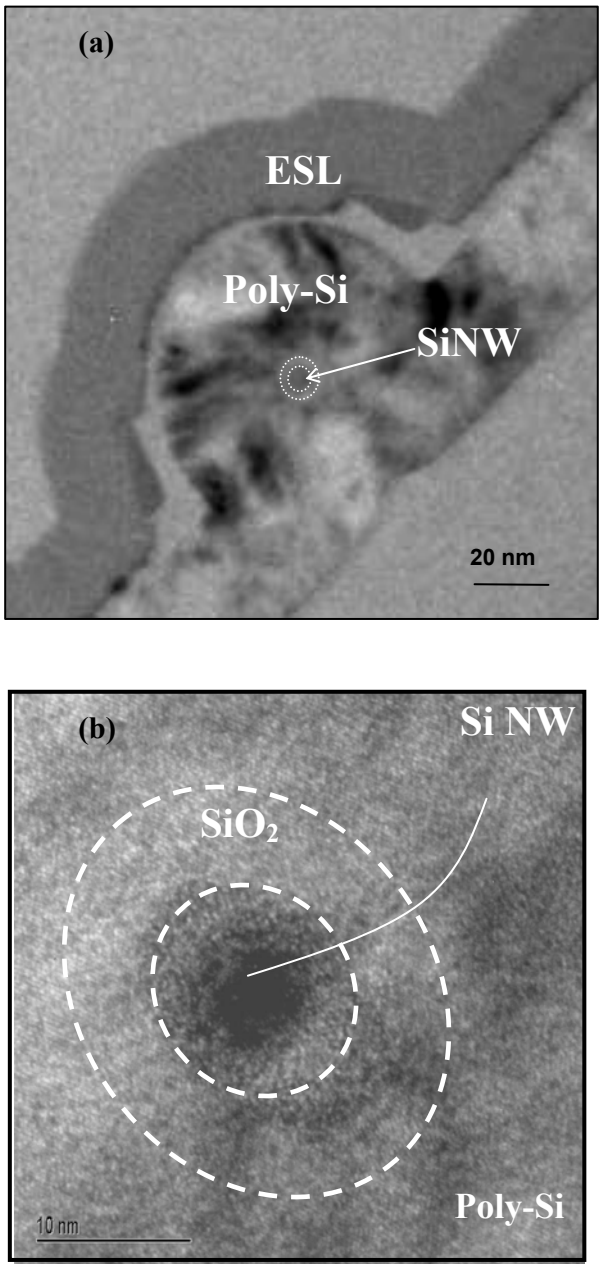


Fig. 5.9: (a) TEM micrograph of the channel cross-section. The GAA structure was successfully formed with 4 nm oxide and followed by the poly Si. ESL is covered on top of the poly Si gate stack. (b) HRTEM image of channel cross-section showing 10 nm SiNW surrounded by 4 nm oxide and followed by poly silicon.

5.4 Dopant Profile Optimizations

Besides sheet resistivity, contact resistivity is also an important parameter that requires careful optimization due to the extremely small contact area between the nanowire S/D extensions and the silicide. A high dopant concentration near the interface to the silicide is desirable, since this increases the tunneling current across the Schottky barrier, and will thus result in low contact resistivity. On the other hand, it is difficult to achieve highly doped nanowire S/D extensions without compromising short channel effects. For the devices in this work, the As^+ SDE implant was implanted after deposition of an offset SiO_2 liner for a slight gate-underlap. P^+ implant was employed after the formation of nitride spacers.

Experimentally finding the doping concentration in the SiNWs is a big challenge; conventional techniques such as SIMS can not be applied. Instead, we performed a TCAD simulation with the structure of 10 nm size nanowire source/drain extensions with the same gate pattern size. The nanowires received the same LDD and S/D implantation and activation condition as our devices. The simulation structure results are shown Fig. 5. 10. Fig. 5.10 (a) is the cross section of the gate profile and Fig. 5.10 (b) illustrate the 3-D doping concentration changing along the nanowire region. Different color stands for different dopant concentration.

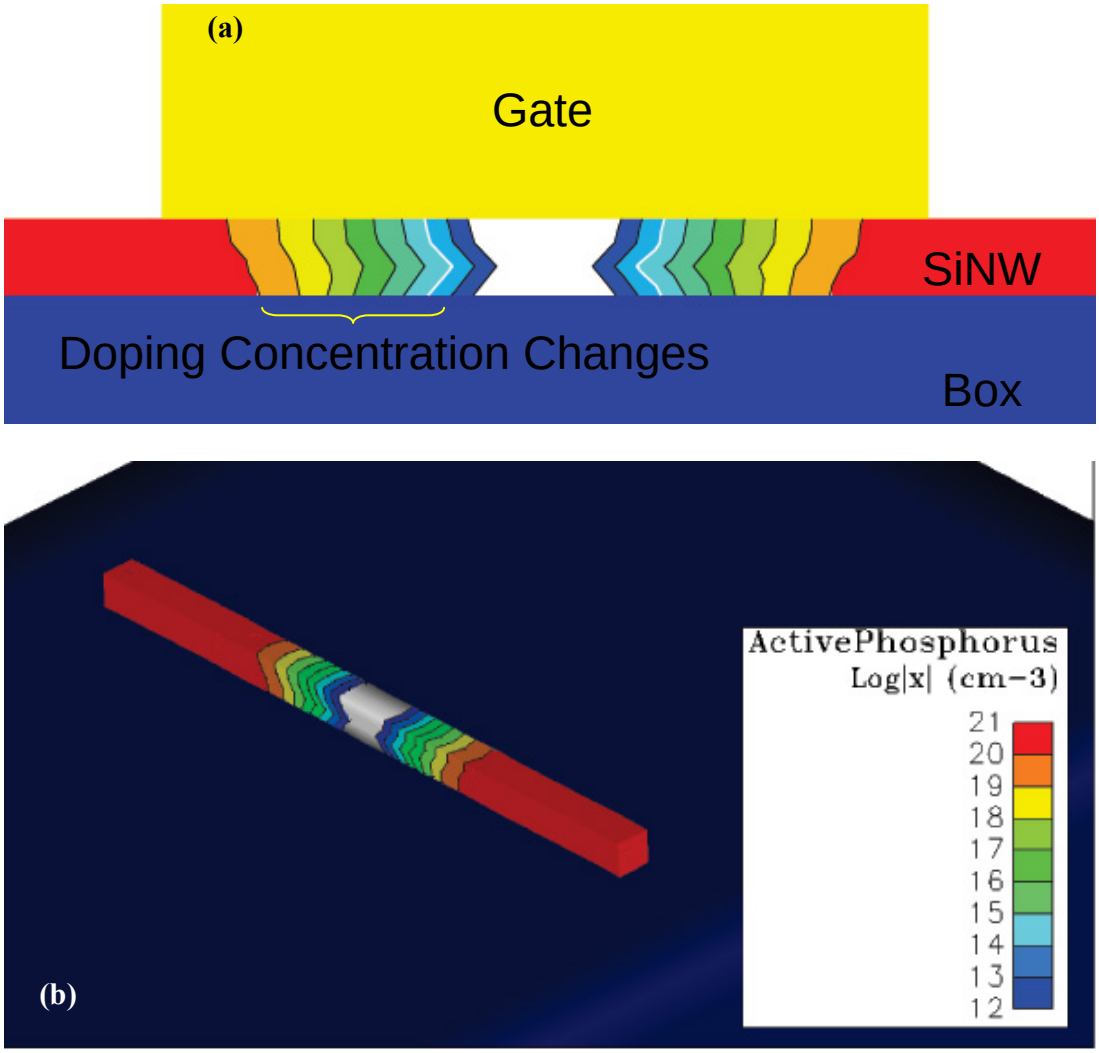


Fig. 5.10: (a) TCAD simulation for the gate profile with the structure of 10 nm size nanowire source/drain extensions with the same gate pattern size. (a) Doping concentration profile along the nanowire region with different color standing for different channel doping.

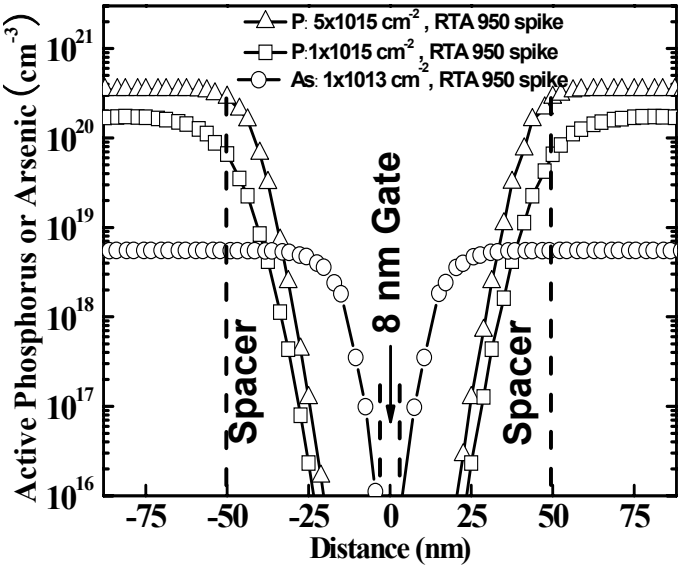


Fig. 5.11: Active dopant profile with different implant conditions. As LDD profile was also showing. 5×10^{15}cm^{-3} shows higher active dopant concentration and sharper profile.

We picked up the center of the nanowire to investigate the concentration inside the 10 nm size nanowires. Fig. 5.11 shows the simulated active dopant concentrations for 10 nm nanowire devices after S/D activation. Implanting P^+ at a dose of 5 x 10^{15} cm^{-2} results in significantly higher dopant concentration near the spacer edge than that obtained with implanting at a dose of 1 x 10^{15} cm^{-2}. This results in high dopant concentration at the semiconductor region near the silicide interface, which is crucial for ensuring a low contact resistivity.

The device splits are shown in Table 4.1. All splits received the same SDE implants. After nitride spacer formation, both the Control and split A received 1 x 10^{15} cm^{-2} P^+ implants while split B received 5 x 10^{15} cm^{-2} P^+ implants. All splits underwent the same 950˚C spike anneal. Subsequently, both splits A & B were silicided using 4 nm of deposited Ni. The choice of this Ni thickness is attributed to the low resistivity at this thickness. It is also thin enough to avoid "over-silicidation" of the nanowire S/D regions, which would otherwise result in excessive lateral silicide encroachment (Excessive

silicide encroachment can lead to Schottky transistor-like device behaviour or device shorts.).

Table 5.1: Split table for this work

samples	P dose (cm^{-2})	Silicidation
Control	1×10^{15}	×
A	1×10^{15}	4 nm Ni
B	5×10^{15}	4 nm Ni

5.5 Device Electrical Characteristics

5.5.1 I_D-V_G Curve and Series Resistance Investigations

The I_D-V_G characteristics for three splits are shown in Fig. 5.12. The gate length is 8 nm, which is the same pattern size as shown the inset of Fig. 5.8, and the drain current is normalized by the diamter (10nm). Comparable subthreshold swing (73mV/dec) and DIBL (28mV/V) parameters are observed for silicide and w/o silicide devices benifited by the GAA structure, while large drive current enhancement can be seen for silicide devices. By employing low resistivity metallic nanowire contacts (NiSi S/D extensions) technique, large drive current has been achieved without compromising short channel effects. By adopting higher S/D dopant concentration in order to increase the tunneling current, the drive current can be increased even higher.

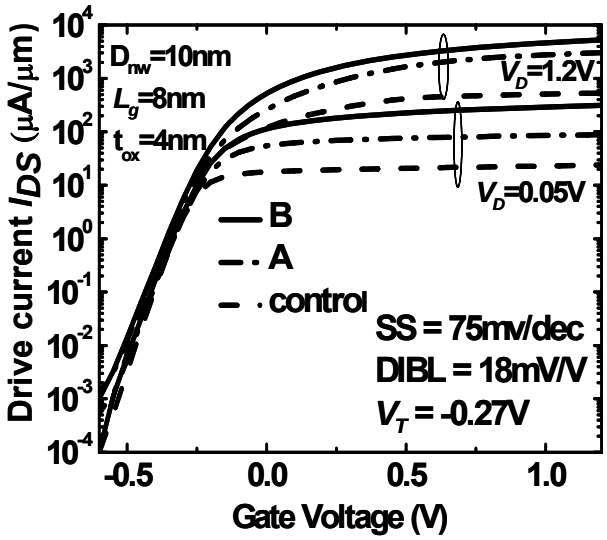


Fig. 5.12: showing DC characteristics comparison between the three splits. Large enhancement has been obtained on sample B. Highly doped S/D doping with metallic nanowire contacts.

Using the method of series resistance extraction described in ref. [147], Fig. 5.13 plots the series resistance R_{SD} exponential decay fitting at V_G=10V for the various splits. At low drain bias and high gate bias, the channel resistance diminishes asymptotically and R_{Tot} approaches the value of the parasitic S/D series resistances. It is observed that silicidation improves the series resistance tremendously.

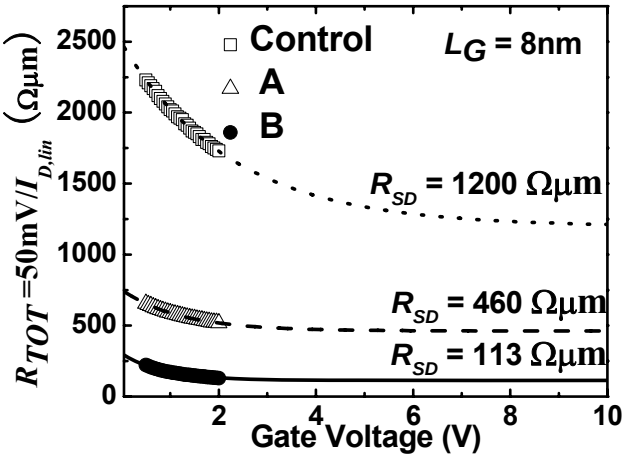


Fig. 5.13: R_{SD} resistance for control, split A, split B are 1200Ωμm, 460Ωμm & 113Ωμm, respectively. Metallic NW reduces R_{SD} significantly.

The series resistance of split B is also drastically improved over that of split A, which indicates that high S/D extension dopant concentration indeed helps to reduce the contact resistivity by lowering the Schottky barrier at the n^+-Si-NiSi junction.

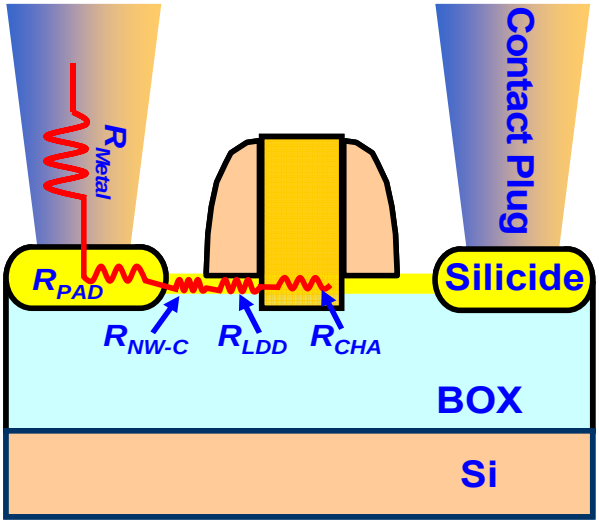


Fig. 5.14: Gate cross section illustrating the total resistance components for a typical nanowire transistor.

As illustrates in Fig. 5.14, the lumped total resistance of a silicided nanowire device (split A) is estimated to be 460 Ωμm. Its constituents are given by the following equation:

$$R_{total}=R_{channel}+R_{LDD}+R_{contact}(\text{silicide-silicon})+R_{silicide}+R_{contact\text{-}plug}+R_{metal\text{-}line} \qquad (4.2)$$

where the $R_{metal\text{-}line}$, $R_{contact\ plug}$ and $R_{silicide}$ component can be neglected for our devices having 1.0μm wide metal lines, 0.6μm x 0.6μm contact plugs and 1.0μm wide silicided S/D pads. Decoupling $R_{channel}$ using devices of different channel lengths, the $R_{LDD}+R_{contact}$(silicide-silicon) component for spits B is found to be around 113kΩ.μm. It suggests that R_{LDD} and $R_{contact}$(silicide-silicon) are the dominant resistance components in the total resistance of the nanowire devices. Thus, further I_{Dsat} performance enhancement

can be achieved through dopant concentration profile optimization in LDD regions, or by tuning of the barrier height at the silicide-silicon interface.

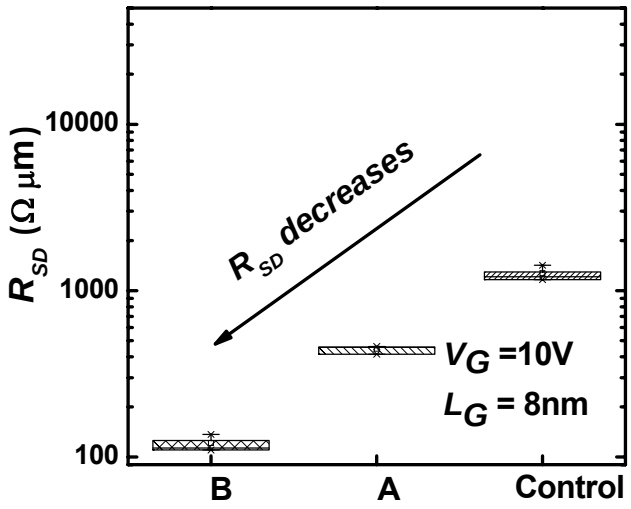


Fig. 5.15: Statistical R_{SD} extraction for three splits by exponential fitting @ V_G=10V. Splits B obtained the smallest series resistance among the three splits.

Statistical investigation was also performed to confirm the results. Fig. 5.15 shows the box plots of the fitted R_{SD} value for three splits which indicate the metallic nanowire contact with high dose deep SD doping (split B) obtain smallest R_{SD} value. This confirms that series resistance improvement via utilizing metallic nanowire contact technology.

5.5.2 I_{on}-I_{off} Characteristics Enhancement

The I_{on}-I_{off} plot for statistical analysis is shown in Fig. 5.16. (The selection of Vg to measure Ion and Ioff is dependent on the threshold voltages of the devices. The difference between Vg,on and Vg,off is dependent on the gate oxide thickness. Overall,

the use of different Vg conditions for each chapter does not impact the validity of the results since the comparisons between experimental splits and control devices were only performed within each experiment using identical Vg conditions.) At a fixed I_{Off} of 10 nA/μm, split A shows a 335% enhancement in I_{on} from 500 μA/μm to 2180 μA/μm. This highlights the importance of silicidation for improving nanowire drive current performance. Split B shows a further 43% enhancement in drive current than split A, giving a very high drive current of 3190 μA/μm for n-channel nanowire transistors at the same I_{Off}.

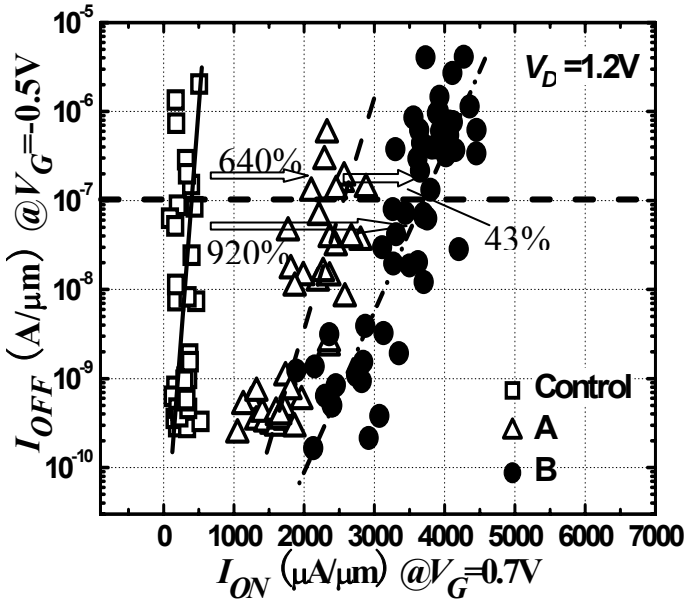


Fig. 5.16: Comparison of I_{off} versus I_{on} .Sample B shows large enhancement over control and sample A.

It is possible that the high deep S/D doping in split B can affect short channel control due to increased dopant diffusion into the channel regions. Fig. 5.17 plots I_{on} against subthreshold swing, which gives the dependence of I_{on} on the gate length. The enhancement in I_{on} with decreasing gate length is obvious in split B, as the total resistance is dominated by channel resistance. On the other extreme, I_{on} in the control does not show

a significant dependence on gate length as the current is suppressed due its high parasitic resistances. At a fixed SS value of 70 mV/dec, the enhancement in I_{on} are 280% and 600% for splits A and B respectively. This indicates that similarly large drive current enhancement can be obtained at the same effective channel length.

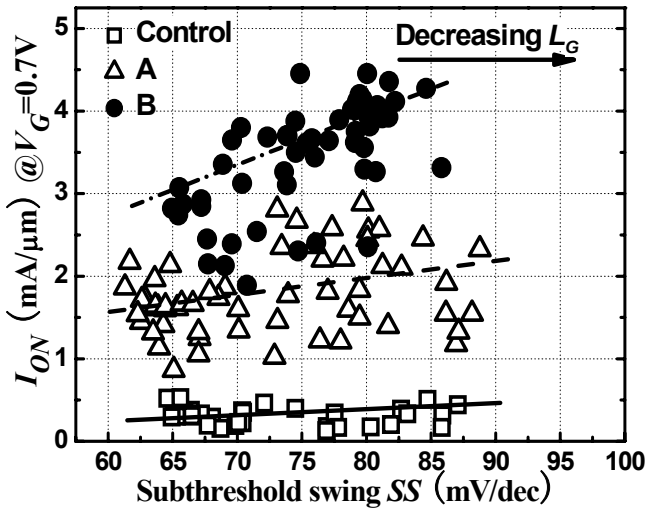


Fig. 5.17: Comparison of I_{on} versus SS. Sample B shows large improvement over control and sample A.

Fig. 5.18 plots I_{Off} against $V_{T,sat}$, which compares the severity of short channel effects for the various splits. Excellent matching at short gate lengths is observed, which confirms that no short channel degradation occurred in splits A and B as compared to control.

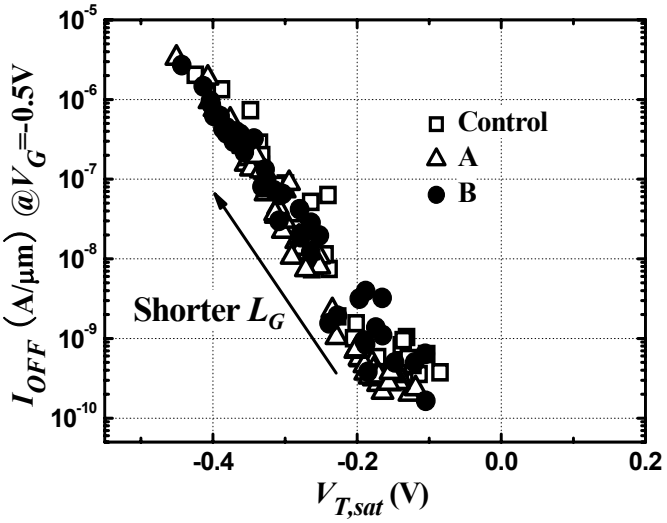


Fig. 5.18: Comparison of I_{Off} versus $V_{T,sat}$. No short channel degradation has been found on sample A and B compared to control.

Without comprising short channel performance, successful integration of low resistivity metallic contacts on GAA nanowire devices results in high drive current of 3740 μA/μm at a V_G - V_T = 1 V. A large enhancement in drive current has been achieved over control device shown in Fig.5.19.

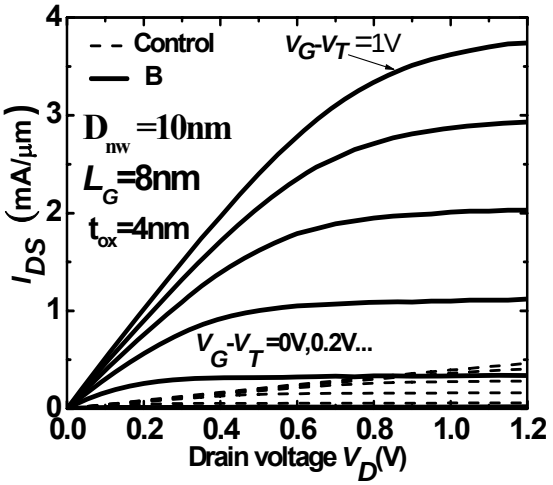


Fig. 5.19: I_D-V_D curve for control and split B. Large enhancement has been obtained on sample B. Drive current is 3740μA/μm@V_G-V_T=1V.

Table 5.2 summarizes and compares the key device parameters of this work with other prior work.

	This work	Ref [116]	Ref [128]	Ref [235]	Ref [218]
NW size radius (nm)	5	4	1.5	5	~5
Gate structure	GAA	GAA	GAA	Ωshape	GAA
Gate type	Poly Si	TiN	Poly Si	Poly Si	Poly Si
Dielectric	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2
Lg(nm)	8	15	350	10	130
tox/EOT (nm)	4	3.5	4	1.9	5
Vdd (V)	1.2	1.0	1.2	1	1.5
Ion (μA/μm)	3740	1440	2400	522	1039
Normalization	Diameter	Diameter	Diameter	---	Diameter
SS (mV/Dec)	75	72	60	75	72-74
DIBL (mV/V)	22	50	6	80	4~12
Ion/*Ioff*	$>10^7$	10^6	10^6	10^5	$>10^8$

5.5.3 Backscattering Study for High S/D dopant Split

Next, the split B are studied in greater detail, backscattering parameters in GAA nanowire transistors of such small gate lengths was extracted using a temperature-dependent model [199, 200]. The experimentally obtained results aid in the understanding of carrier transport characteristics in such devices. Fig. 5.20 shows backscattering ratio r_{sat} and ballistic efficiency B_{sat} extracted at various gate-overdrives for an 8 nm gate length split B GAA nanowire device.

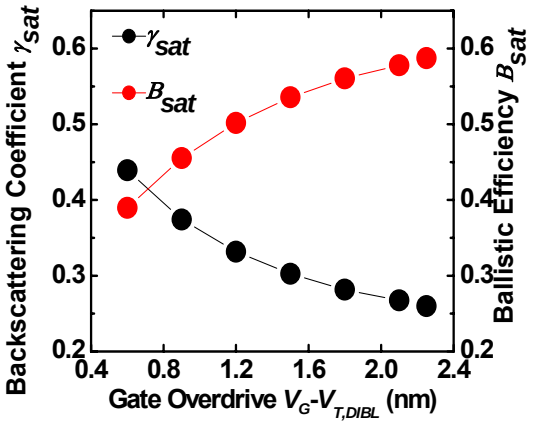


Fig. 5.20: Backscattering ratio r_{sat} and ballistic efficiency B_{sat} extracted at various gate overdrives. A minimum rsat of ~0.26 was obtained @ V_G-$V_{T,DIBL}$=2.25V.

A minimum r_{sat} of ~0.26 is obtained for such 8 nm gate length devices. Fig. 5.21 shows r_{sat} extracted for devices with different gate lengths. The low r_{sat} values obtained gives further evidence for the high performance in these devices. The results confirm that the probability of a carrier being backscattered also reduces as the gate lengths become smaller, indicating higher ballistic efficiency. It should be noted that in spite of the ultra-short channel lengths, corresponding B_{sat} values indicate that the devices still operate at a regime away from the ballistic limit. This concurs with reports for UTB-SOI double-gate devices for 10 nm gate lengths [236].

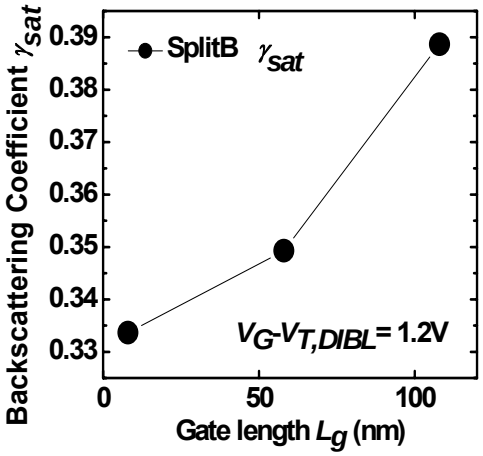


Fig. 5.21: Backscattering ratio r_{sat} extracted for various gate lengths at V_G-$V_{T,DIBL}$=1.2V. r_{sat} decreases (improves) as gate lengths are scaled down.

5.6 Conclusions

Nickel silicide resistivity values for ultra-thin films have been investigated for metallic nanowire contact application. Optimization of low resistance NiSi nanowire contacts integrated with GAA nanowire transistors using laterally encroaching NiSi junctions have been successfully demonstrated in this work. This resulted in an excellent I_{on} of ~3.75mA/μm at an I_{Off} of 100nA/μm. Backscattering results suggest that such high-performing GAA nanowire transistors with gate lengths down to 8 nm still operate at a regime away from the ballistic limit. Nevertheless, we demonstrate that effective short channel control, low channel and access resistances can be obtained in the GAA nanowire transistors down to 8 nm gate lengths. This resulted in very good I_{on}-I_{Off} performance as well as very small projected gate delays. The high absolute device performance obtained strongly suggests that low resistivity metallic nanowire contact technology is of great importance in realizing state-of-the-art nanowire devices.

CHAPTER 6

6. THRESHOLD VOLTAGE ENGINEERING OF GAA NANOWIRE FETs FOR CMOS CIRCUIT INTEGRATION

6.1 Introduction

Based on the understanding of the previous chapter, the Gate-All-Around (GAA) Si nanowire transistors exhibit excellent performance and short channel immunity with their superior gate electrostatistic control. [75, 116, 218, 237] Many technologies, such as the reduction of the series resistance in the source drain extensions using metallic nanowire contact technology [237], and mobility enhancement by strain incorporation into the Si nanowire [130-132, 137, 238], are being incorporated for further improving the performance of the nanowire transistors. However, in nanowire FETs the doped poly-Si gates set the V_T incorrectly as the channel dimension are in nanometer regime and operates at nearly intrinsic channel doping condition [116, 239]. Yeo et al. demonstrated the approach of introducing metal materials such as TiN gate to achieve desirable gate work-functions for CMOS transistor with the intrinsic nanowire channel [116]. Nevertheless, even for the planar transistors, costly and complicated metal gate schemes are often required [150, 155, 240-247]. A simple and cost effective metal gate scheme with desirable dual work functions [155, 248, 249] is therefore required for the integration of GAA NW FETs into circuits with correctly adjusted V_T.

In this chapter, we demonstrate, a cost effective GAA Si nanowire CMOS FETs with FUSI metal gate. Process simplicity is maintained for ease of integration. Using

work function optimization methodology via dopant segregation during Ni silicidation, dual work functions have been successfully obtained for this intrinsic Si nanowire channel. As a result, symmetrical V_T for N- (0.3V) and P- (-0.3V) FETs are achieved. Demonstration of excellent CMOS inverter transfer characteristics with desirable V_T of NW FETs indicates the suitability of GAA NiSi FUSI gate technology for LSTP circuit integrations.

In the work described in this chapter, I gratefully acknowledge the help of L.H. Tan of the Institute of Microelectronics in the cross-sectional TEM imaging. The use of the excellent facilities at IME is greatly appreciated. However, the ideas were conceived by me, and I have benefited through discussions with my mentors at IME, Dr. Navab Singh and Dr Patrick Lo. All the experiments were designed and executed by myself under the guidance of my mentors.

6.2 Device Fabrications with FUSI Gate

Fig.6.1 shows the schematics of the process flow, which illustrates the local Si nanowire release process by utilizing the reverse gate mask. Fig. 6.1-1 is the schematic after Si fin etching process; the detail has been reported in our previous work [75, 237] as well as in chapter 2. After the Si fin formation, dry oxidation self-limiting process at a temperature of 875°C was performed for 3.5 hours in order to form the Si nanowire down to sub 10 nm. Thus, the original Si fin structure was enwrapped by the SiO_2 layer as shown in Fig. 6.1-2. Next, 120A SiN layer was deposited on the top of the Si fin structure by LPCVD at 720°C. This SiN layer was served as an isolation layer to prevent the thermal oxide beneath the SiN layer being etched away by HF wet oxide etching process. Utilizing the reverse gate mask opened a 200 nm area across the fin structure. SiN layer

was etched away in the reverse gate regions, and left the Si nanowire encapsulated by thermal oxide (Fig. 6.1-3). As a result, only at the reverse gate open region, the SiN has been etched away, while the source/drain regions were still covered by the SiN layer. During oxide wet etching process by HF (1:25), Si nanowire was local released in the reverse gate region. Fig. 6.1-4 is the schematic after Si nanowire local release.

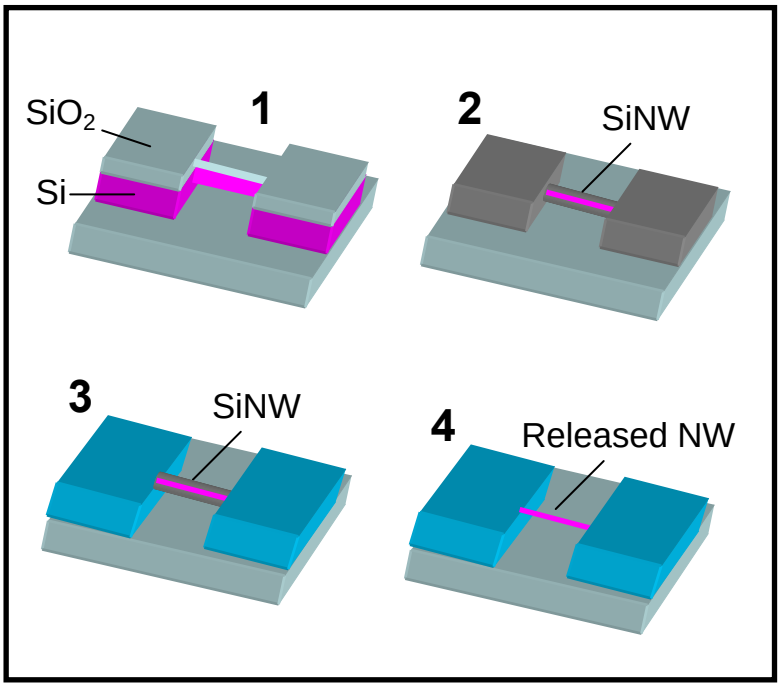


Fig. 6.1: Schematics illustrating the process flow for the nanowire local release by utilizing the reverse gate mask.

Fig.6.2 (a) is the SEM image after reverse gate mask etching process. SiN layer was etched away in the reverse gate open area, leaving Si NW covered by the thermal oxide. The reverse gate region was indicated in the figure. Fig. 6.2 (b) is the SEM image after Si nanowire local release. It is clearly seen that Si nanowire only released in the reverse gate region while other area (source/drain pad and field area) were covered by the SiN layer. Next, 50A thermal SiO_2 followed by the 500A α-Si deposition to form the gate stack. Three splits were fabricated in this work: split I is the poly-Si with poly-Si gate received Boron and phosphorus (3×10^{15} cm^{-2}) for gate implantation, and followed by the

gate implant activation. Split II is FUSI_Only which skiped this implantation step and instead, 500A Ni was deposited on top of poly-Si gate. After RTA soak anneal at 420ºC, a fully silicide GAA structure was formed. Split III is the Tuned_FUSI which received the same implantation and activation as split I while went through the nickel silicidation process to tune the work functions as same as split II.

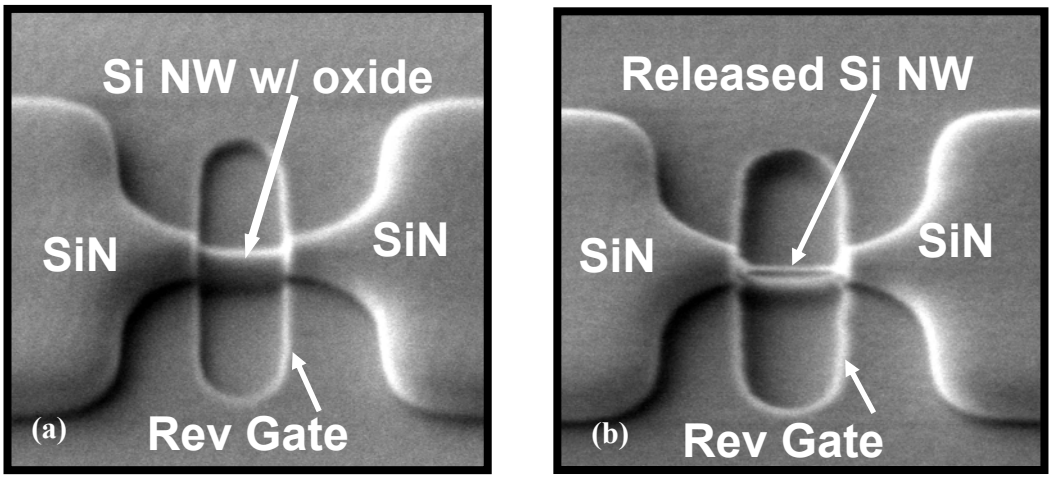


Fig. 6.2: (a) SEM image after reverse gate etching process. S/D regions are covered by the SiN layer. (b) SEM image after Si NW local release. Only the reverse gate region, the nanowire is fully released. S/D regions are protected by the SiN layer during local release.

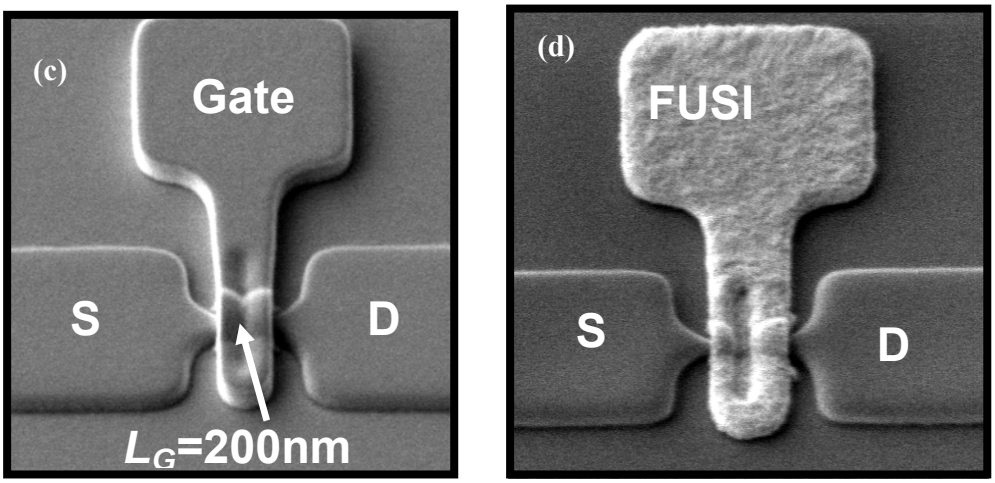


Fig. 6.2: (c) After gate pattern transfer. The gate length depends on the reverse mask, the L_G is 200nm. (d) FUSI device after gate FUSI process (RTA Soak anneal at 420°C). GAA FUSI gate formed with S/D region protected by SiN/oxide layer to prevent over-silicidation of the S/D regions.

Fig. 6.2(c) is the SEM image after gate etching process. The gate length fabricated in this work is 200 nm. The S/D and field oxide area are cover by the SiN hard mask, which prevent S/D region from siliciding during the gate slicidation process. Fig. 6.2 (d) is the SEM micrograph after FUSI gate formation. By employing the reverse gate mask scheme, the S/D regions were protected from silicidation by the SiN/oxide hard mask layer. The CMOS device fabrication was finished by the standard backend process.

Fig. 6.3 is the high angle annular dark field (HAADF) STEM investigation on channel cross section for the GAA structure. The homogeneously high intensity of the surrounding gate further confirms the full silicidation. The nanowire has an elliptical shape (about 7 nm by 4 nm), and is surrounded by 5 nm of SiO_2 and the NiSi FUSI metal gate.

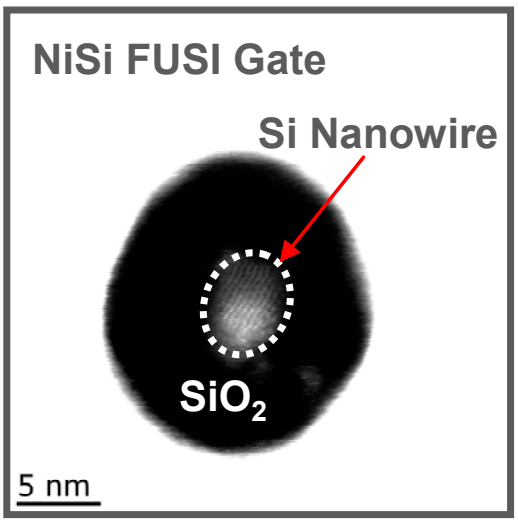


Fig. 6.3: HAADF STEM image of channel cross section. The homogeneously high intensity of the surrounding gate further confirms the full silicidation.

We also performed conventional TEM with EDX analysis of channel cross-section, shown in Fig. 6.4. The EDX analysis confirms the full silicidation of the poly-Si

gate, including the wrap-around regions underneath the nanowire channel. This confirms the true GAA NW FUSI metal gate structure. The ratio of Ni:Si is around 1:1 through this single metal annealing step for all regions measured around the gate films.

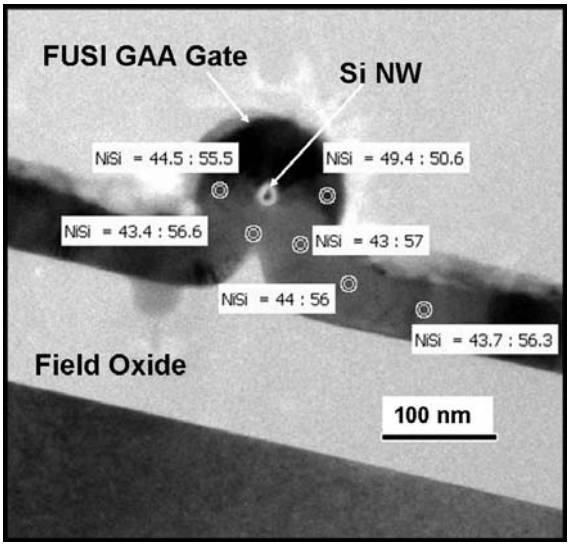


Fig. 6.4: TEM image of NW channel cross-section, showing the GAA FUSI NiSi gate. EDX analysis indicates that the Ni:Si ratio is close to 1:1. The wrap-around regions are also fully silicided.

6.3 Device Electrical Characteristics

6.3.1 GAA Single Metal FUSI Gates with Dual Tune-able Φ_m

Fig. 6.5 is the schematics illustrating the gate structure differences across the splits in this work. The conventional (a) Poly-Si received the gate dopant implantation ($3\times10^{15}cm^{-2}$). The (b) FUSI_Only skipped the gate dopant implantation step while Ni silicidation process was performed to form the FUSI GAA stack. The (c) Tuned_FUSI received the same amount of gate dopant as the Poly-Si gate stack and also underwent Ni

silicidation process. Details on the dopant type and dose can be found in Table 5.1. Gate doping dose for Poly-Si was adjusted to match that for Tuned_FUSI.

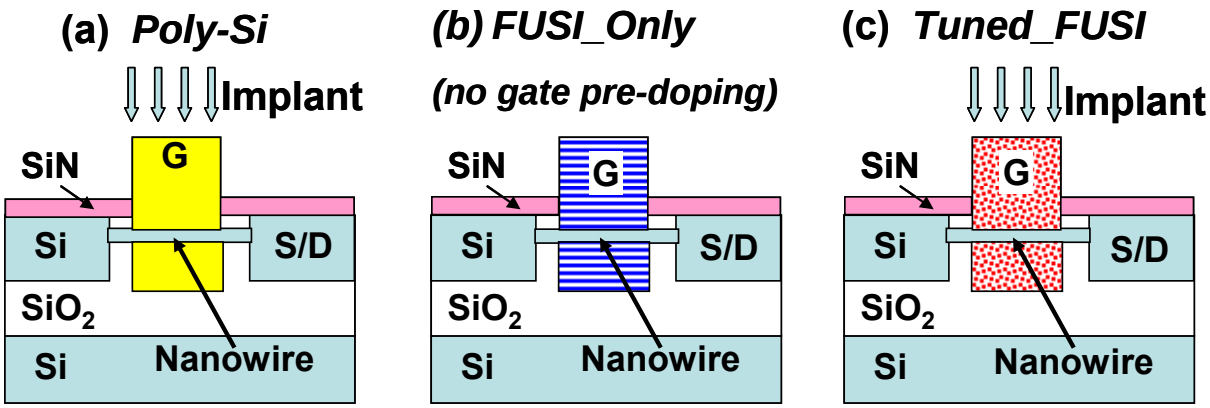


Fig. 6.5: Schematics showing the nanowire device splits. The control Split (a) is with conventional implantation-doped poly-Si gate stack. Split (b) has FUSI gate stack without any prior gate implantation step. Split (c) has FUSI gate with gate pre-doping via implantation for gate work-function tuning.

Table 6.1 : Splits of Gate Types and Doping

	Poly-Si	*FUSI_Only*	*Tuned_FUSI*
N-FETs	P, 3 x 10^{15}	N.A.	P, 3 x 10^{15} cm^{-2}
P-FETs	B, 3 x 10^{15} cm^{-2}	N.A.	B, 3 x 10^{15} cm^{-2}

The effects of the different gate electrodes on V_T, I_{Off} and I_{on} will be discussed with the group of NFETs and PFETs, respectively. By tuning the FUSI Φ_m using Phosphorus and Boron pre-doping of the poly-Si gates, optimum Φ_m were obtained, thereby setting the V_T values for both NFETs and PFETs correctly. Φ_m tune-ability can be

achieved by adjusting the pre-doping dose. More details on the physical mechanism can be found in [155].

The I_D-V_G transfer characteristics of the NMOS devices at a gate length of 200 nm are shown in Fig. 6.6. The parameters of each transistor are listed in the table 5.2. There is a positive shift with a V_T around 0.44V has been observed for the FUSI-only devices over poly-Si devices.

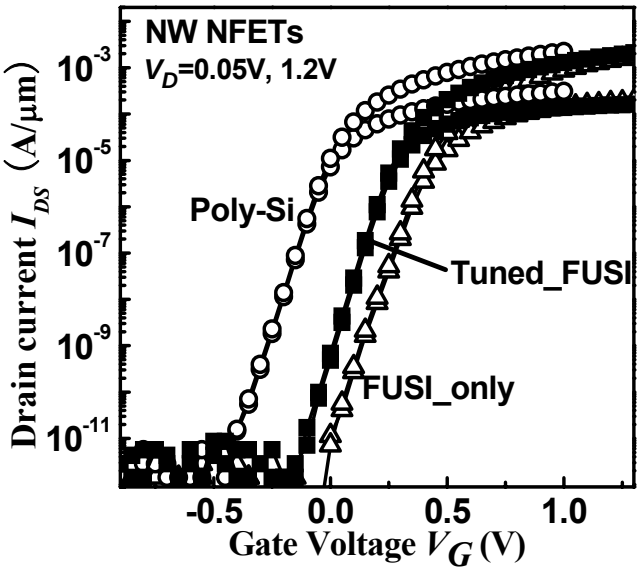


Fig. 6.6: I_D-V_G of NFETs. V_T successfully tuned by Phosphorus pre-doping before FUSI. There is no degradation in SS and DIBL observed.

Table 6.2 Parameters V_T, SS, DIBL for each split of NFETs

Parameter	V_T (V)	SS (mV/dec)	DIBL (mV/V)
Poly-Si	0.022	62	6
Tuned_FUSI	0.27	61	7
FUSI_Only	0.45	67	6

This is consistent with the difference between the Fermi-level for n^+ poly-Si gate (near conduction band) and NiSi metal gate (at mid-gap). As a result, the NiSi FUSI metal gate nanowire devices have higher V_T compared to the n^+ poly-Si gate devices. However, the FUSI_Only splits also set V_T incorrectly (i.e., too high V_T), which will result in lower saturation current at same gate voltage. By dopant segregation effect during gate silicidation process [155], the tuned-FUSI is able to set V_T correctly with excellent I_{off} and relative higher drive current. Thus it further confirms that the wrap-all-around FUSI gate has been successfully formed from the *I-V* characteristics and the tunable V_T was achieved by dopant implantation prior to the FUSI gate formation. Fig. 6.7 is the band diagram for different N gate types which illustrating the work function differences. The work function of NiSi is mid gap, and n^+ poly-Si is near the conduction band. With the n^+ dopant accumulating at the interface between the oxide and FUSI gate, the FUSI with gate dopant work function will be further moving upwards. As the gate doping increases, the work function is towards more to the conduction band so as to tuning the work function of the NMOS transistors.

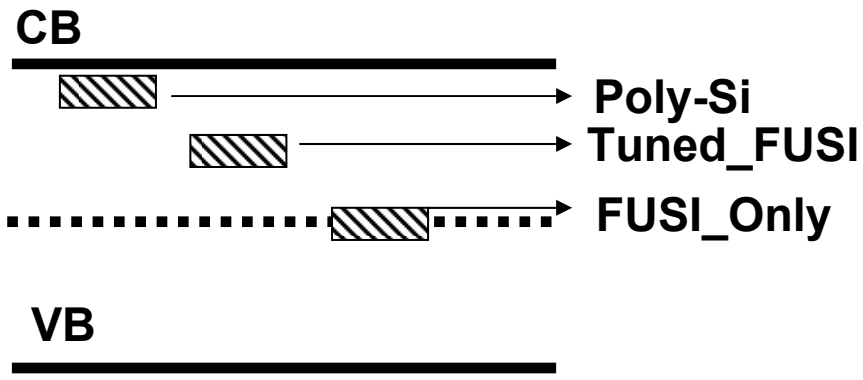


Fig. 6.7: Band diagram schematics illustrating the Fermi-Level difference among different gate stack material. (Not to scale).

The Tuned_FUSI split set the V_T aournd 0.27V. As the gate doping increases, the Fermi lever of NiSi FUSI film with gate implantation shift towards the conduction band,

which makes the threshold voltage even lower. This is consistent with the experimental result observed in Tuned_FUSI split. It can be further foreseen that if the gate dopant increases further, even lower threshold voltage can be obtained. This indicates large range of threshold voltage control is able to achieve by utilizing dopant segregation FUSI gate process. Besides, as shown in the table, all splits exhibit comparable DIBL and SS parameters, which could suggest that FUSI annealing process doesn't degrade channel control for the nanowire devices.

By the same train of the thought, PMOS FET was also investigated in this work. The I_D-V_G transfer characteristics of the PMOS at a gate length of 200 nm are shown in Fig. 6.8. The parameters of each transistor are listed in the table 5.3. There is a negative shift with a V_T around 0.65V for the FUSI-only devices over poly-Si devices.

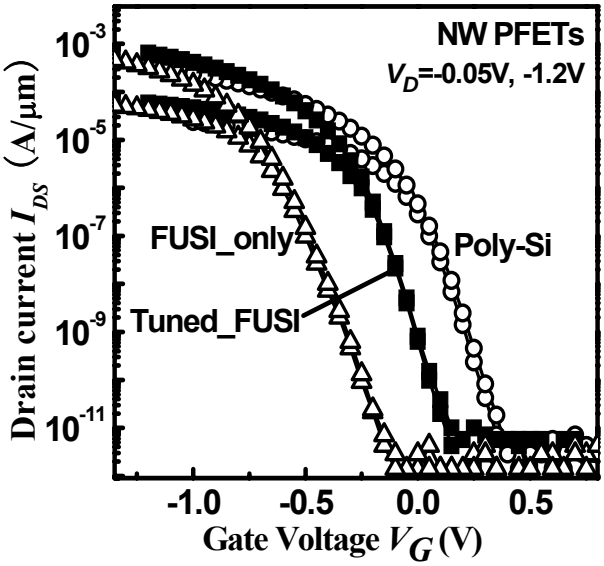


Fig. 6.8: I_D-V_G of PFETs. V_T successfully tuned by Phosphorus pre-doping before FUSI. There is no degradation in SS and DIBL observed.

Table 6.3 Parameters V_T, SS, DIBL for each split of PFETs

Parameter	V_T (V)	SS (mV/dec)	DIBL (mV/V)
Poly-Si	-0.029	70	14
FUSI($3\times10^{15}cm^{-2}$)	-0.26	70	6
FUSI_Only	-0.67	75	6

This is consistent with the difference between the Fermi-level for p^+ poly-Si gate (near valence band) and NiSi metal gate (at mid-gap). As a result, the NiSi FUSI metal gate nanowire devices have lower V_T compared to the p^+ poly-Si gate devices. The FUSI ($3\times10^{15}cm^{-2}$) split set the V_T aournd -0.26V. Fig. 6.9 is the band diagram for different N gate types which illustrating the work function differences. The work function of NiSi is mid gap, and p^+ poly-Si is near the valence band. With the p^+ dopant accumulating at the interface between the oxide and FUSI gate, the FUSI with gate dopant work function will be further moving upwards. As the gate doping increases, the work function is towards more to the conduction band so as to tuning the work function of the NMOS transistors. Again, as shown in the table, all splits exhibit comparable DIBL and SS parameters, which could suggest that FUSI annealing process doesn't degrade channel control for the nanowire devices.

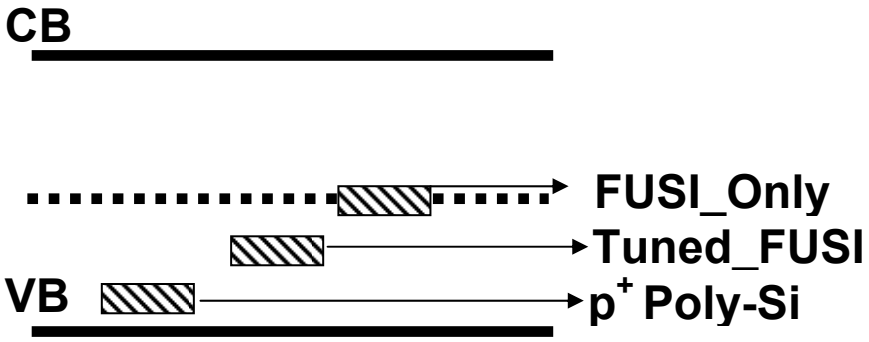


Fig. 6.9: Band diagram schematics illustrating the Fermi-Level difference among different gate stack material. (Not to scale).

6.3.2 Impact on Absolute V_T, I_{Off} and I_{on}, and on V_T

For NFETs, it is clear from the previous session discussion that Poly-Si and FUSI_Only NFETs have V_T that is too low and too high respectively. This is due to the Fermi level of the intrinsically doped channel and the incorrect gate Φ_m values of the n^+ poly-Si gate (conduction band-edge) and the NiSi FUSI gate (near mid-gap). As a result, the I_{Off} of the Poly-Si NFET is too high (Fig. 6.10), While the I_{Off} of the FUSI_Only and Tuned_FUSI NFETs are both desirably low. For the normal circuit implementation, it is necessary to obtain a higher drive current at a fix gate voltage supply (i. e. power supply). The Tuned_FUSI NFET has a 29% higher drive current, I_{on}, at V_{DD}=1.2V (Fig. 6.11). Fig. 6.11 further illustrates the large magnitude of I_{on} enhancement that can be obtained at lower V_{DD} for the same I_{Off}, emphasizing the importance of V_T tune-ability.

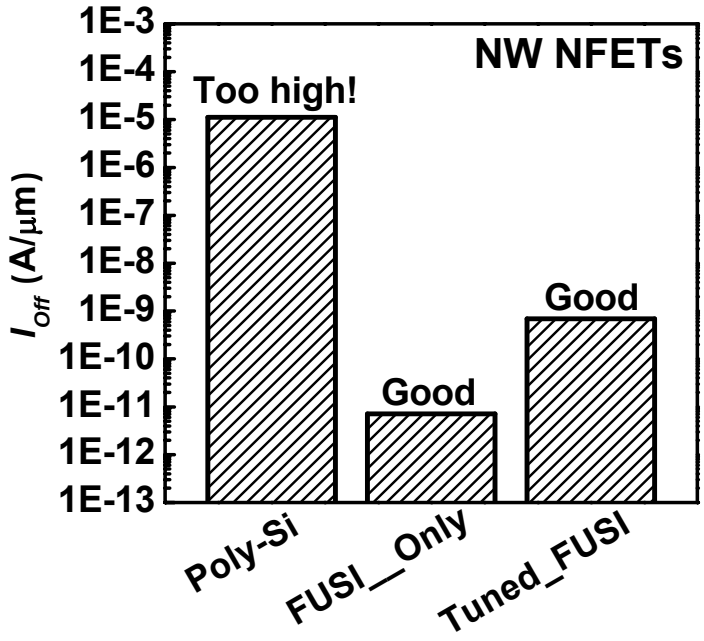


Fig. 6.10: I_{Off} of NFETs. Poly-Si gate NW NFET has I_{Off} that is too high. FUSI gate NW NFETs show excellent I_{Off} values. By tuning the V_T, the I_{Off} can be set at the designed value.

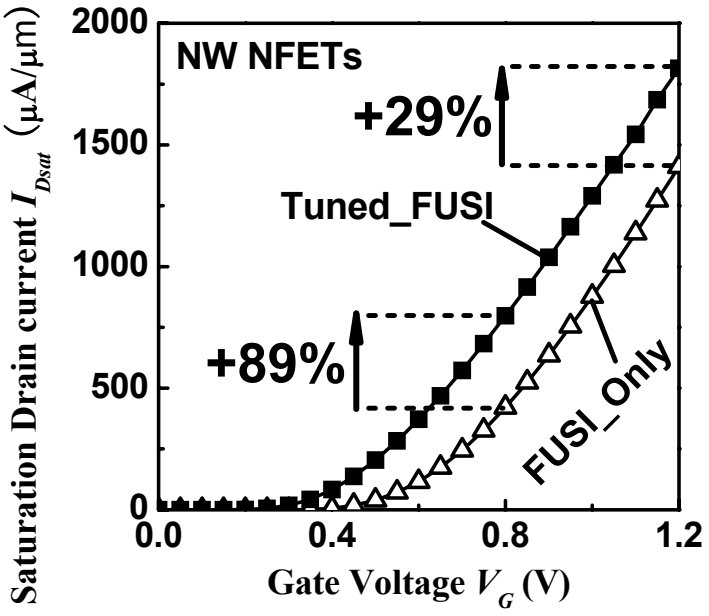


Fig. 6.11: I_{on} of Tuned_FUSI NFET is enhanced by 29% over FUSI_Only NFET at $V_G = V_{DD} = 1.2$ V. I_{on} enhancement is 89% at $V_G = 0.8$ V. This shows the importance of V_T tuning when V_{DD} is scaled down.

Following the same train of thought when going through, it can be seen that Boron pre-doping prior to gate silicidation sets the V_T correctly for PFETs, similar to what phosphorus pre-doping accomplished for NFETs. The I_{Off} of the Poly-Si PFET is too high (Fig. 6.12), While the I_{Off} of the FUSI_Only and Tuned_FUSI NFETs are both desirably low. The Tuned_FUSI NFET has a 105% higher drive current, I_{on}, at V_{DD}= -1.2V (Fig. 6.13). Fig. 6.13 further illustrates the large magnitude of I_{on} enhancement that can be obtained at lower V_{DD} for the same I_{Off}, emphasizing the importance of V_T tune-ability.

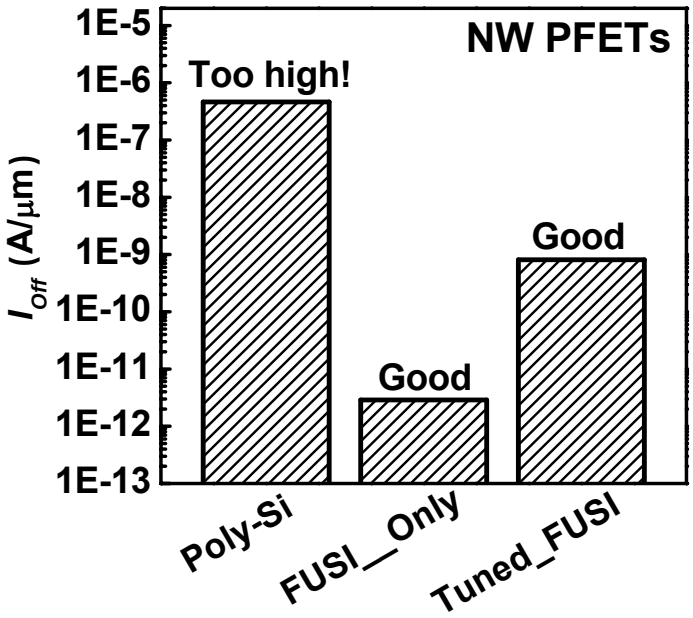


Fig. 6.12: I_{Off} of PFETs. Poly-Si gate NW PFET has I_{Off} that is too high. FUSI gate NW PFETs show excellent I_{Off} values. By tuning the V_T, the I_{Off} can be set at the designed value.

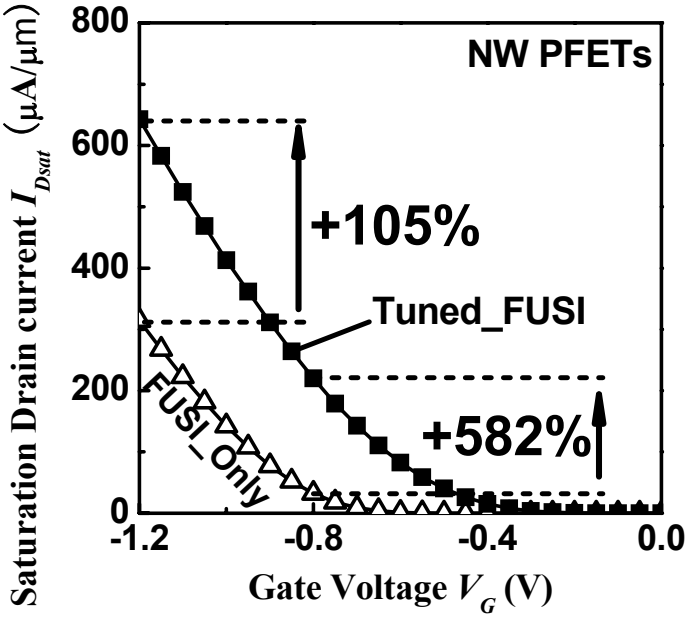


Fig. 6.13: I_{on} of Tuned_FUSI PFET is enhanced by 105% over FUSI_Only PFET at V_G = V_{DD} = -1.2 V. I_{on} enhancement is 582% at V_G = 0.8 V. This shows the importance of V_T tuning when V_{DD} is scaled down.

Statistically study was performed in order to confirm this threshould voltage tuning effect. Fig. 6.14 shows the cumulative distribution of V_T values for both NFETs (a) and PFETs (b), which statistically confirms the V_T tuning effects.

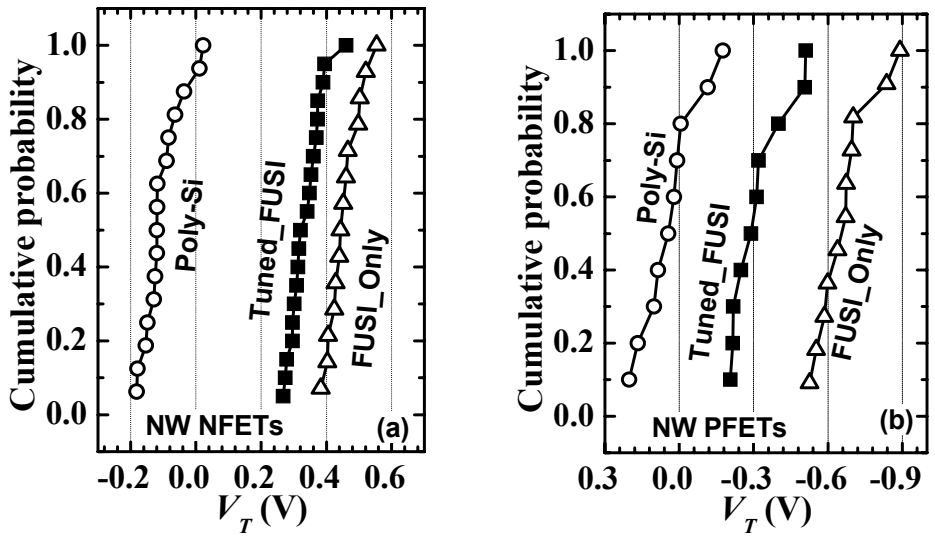


Fig. 6.14: Statistical plot of V_T for NW NFETs (a) and PFETs (b) clearly shows the V_T differences between splits. V_T extracted from linear I_D using max. G_m and tangent method.

V_T variation is an important determinant of device manufacturability. It is important that in the process of setting the gate Φ_m correctly, the Tuned_FUSI processes do not worsen V_T variation. Figs. 5.15 summarize the V_T data. Overall, the absolute standard deviation (σ) of the PFETs (all three splits) are larger than those of NFETs. However, since NFETs and PFETs are fabricated on the same wafers, T_{inv}, dielectric fixed charge and body thickness are unlikely to be the dominant sources of increased variation in the PFETs. It is possible that the source of the higher variation is due to higher variation in the S/D extension doping and series resistances of the PFETs. More importantly, for NFETs and PFETs, respectively, the standard deviations (σ) of V_T are

comparable across all three splits. This clearly indicates that the FUSI processes do not degrade the variation of the devices.

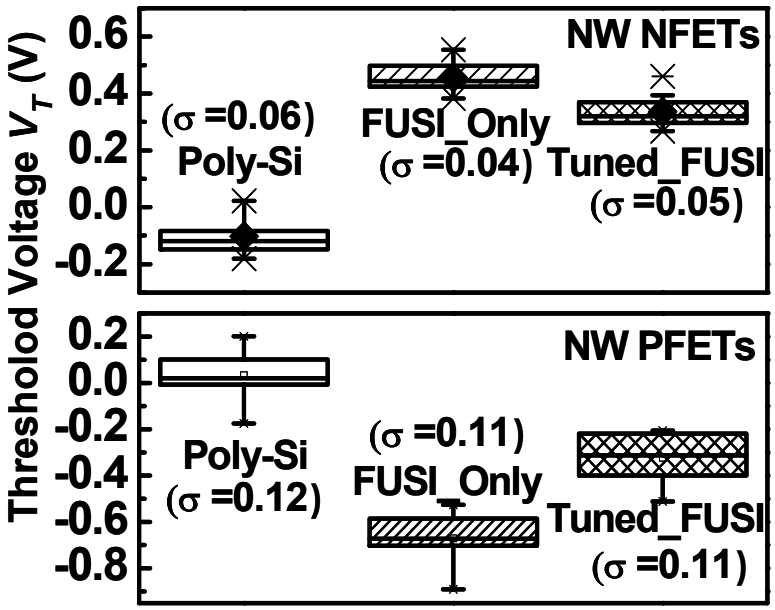


Fig. 6.15: Statistical plot of V_T for for all three splits. V_T was extracted from linear regime using max. G_m and tangent method. No degradation of V_T variation was observed.

As shown in the Fig. 6.15, the tuned-FUSI has obtained the desirable V_T and symmetrical V_{Ts} have been achieved at the same time through a single metal anneal step. This successful V_T tuning scheme will be suitable for the LSTP and circuit applications for intrinsic nanowire devices. An increase of ~0.5V is observed for FUSI-Only over Poly-Si split for both the N- and PFET devices. Summing together, |0.5V|+|-0.5V|=1V, which is nearly the band-gap of the bulk Si. Since both N- and P-FETs were formed in the same wafer and under the same condition, the FUSI gate work function should be the nominal value. The difference for the FUSI gate work function towards n^+ poly-Si sum it towards p+ poly-Si is ~ 1V.

Besides the threshold voltages statistical investigations, we also investigated the cumulative distributions of the subthreshold swing between the Poly-Si and Tuned_FUSI

splits. As shown in Fig. 6.16, both splits exhibit comparable SS value, which indicated that the FUSI gate process will not degrade the transistors performance.

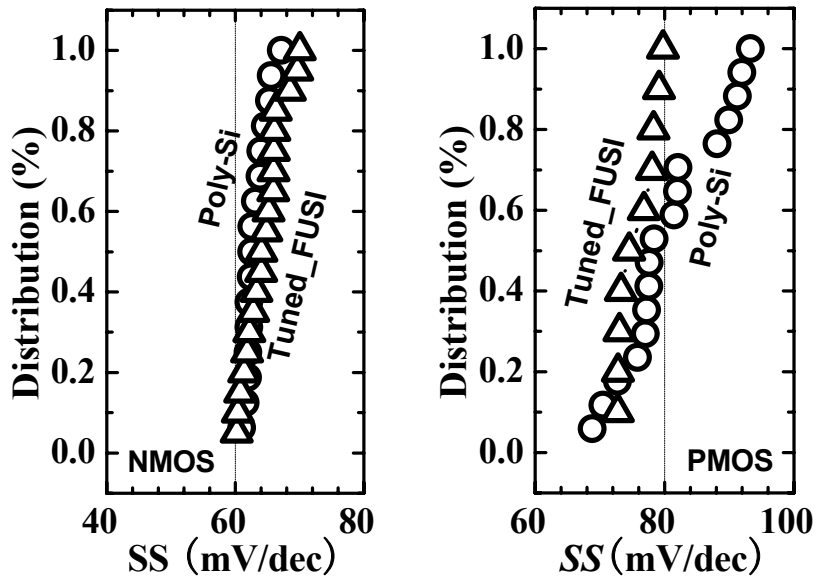


Fig. 6.16: Cumulative distribution of SS for Poly-Si and Tuned_FUSI splits. Both splits indicated comparable SS values.

6.3.3 Tuned_FUSI NW FETs Low Power CMOS Circuit Application

Fig. 6.17 shows the nearly symmetrical I_D-V_G transfer characteristics of the Tuned_FUSI N and P FETs, showing excellent SS and DIBL values. Stress effects help to reduce the I_{Dsat} performance gap between the NFET and PFETs which will be discussed later. At a gate overdrive of |1|V, the I_{Dsat} values for the Tuned_FUSI NFET and PFET are 1900 and 810 μA/μm respectively (Fig. 6.18), which is closer to 2:1 compared to the Poly-Si devices. The currents are normalized by the nanowire diameter of 7 nm. It is worth mentioning here that since the nanowire dimensions are comparable to the inversion layer thickness, normalization by the diameter may be more appropriate. This is also consistent with the normalization convention for other work on NW FETs [116, 128, 218].

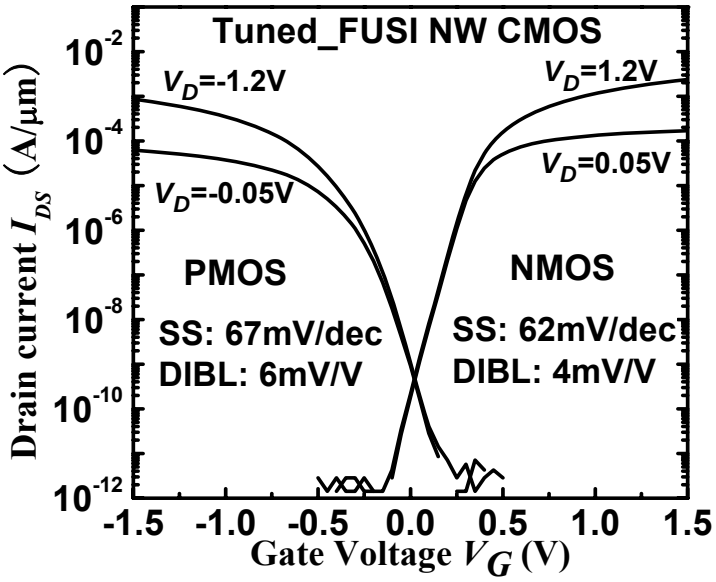


Fig. 6.17: I_D-V_G characteristics of Tuned_FUSI NW CMOS. Nearly symmetrical V_T achieved with comparable short channel control. The drain current is normalized by nanowire diameter ~7 nm.

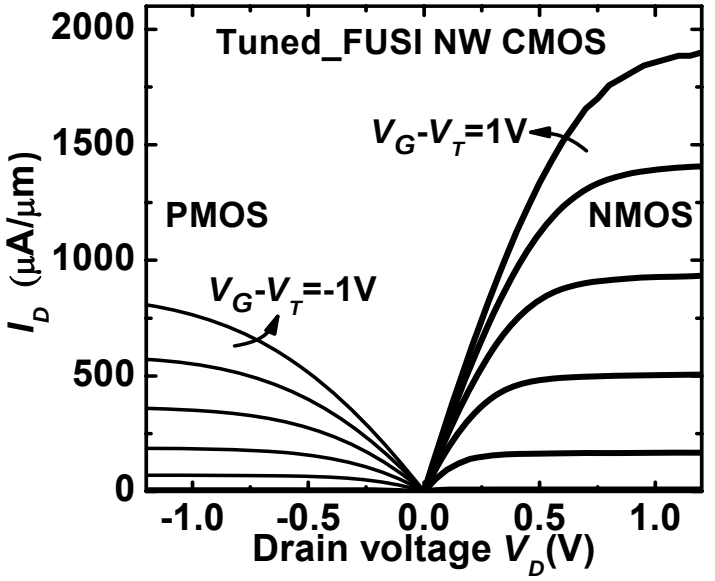


Fig. 6.18: I_D-V_D characteristics of Tuned_FUSI NW CMOS. The difference in drive current is attributed to electron and hole mobility differences and the higher series resistances in PFETs.

As mentioned in chapter 3, with the fewer carriers (charge) in the channel or the reducing gate capacitance due to the small surface area of the nanowire channel (C_{Area}~ 3.14 x 350 nm ×13 nm), it is difficult to measure the gate capacitance using split C-V to extract the mobility of the nanowire. The nanowire channel capacitance is far smaller than the lower limit of any conventionally used standard ac bridge based instruments. In order to capture the mobility of the nanowire channel, mobility testing structures with a maximum 1000 nanowires are fabricated on the same wafer, and C_{inv} was obtained from a test structure with 1000 nanowires. By the split C-V measure, the electron and hole mobility are able to be extracted. The measured peak electron mobility is 89% higher than the peak hole mobility (Fig. 6.19). At higher V_G-V_T, the hole mobility degrades less quickly than the electron mobility. This suggests that the performance gap between NFETs and PFETs will further narrow if T_{ox} scales down.

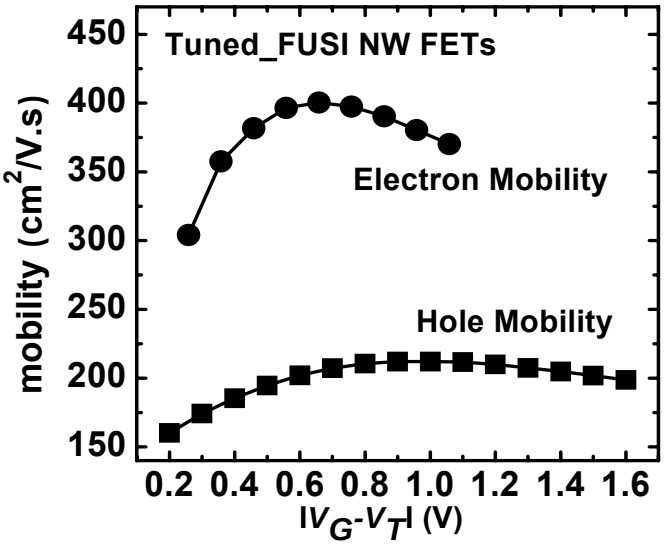


Fig. 6.19: Electron and hole mobility for Tuned_FUSI NW devices. C_{inv} was obtained from a test structure with 1000 nanowires. The peak electron mobility is 400 cm^2/V.s and hole peak mobility is 212 cm^2/V.s.

Next, I_{on}-I_{Off} characteristics are investigated for the Tuned_FUSI splits. (The selection of Vg to measure Ion and Ioff is dependent on the threshold voltages of the devices. The difference between Vg,on and Vg,off is dependent on the gate oxide thickness. Overall, the use of different Vg conditions for each chapter does not impact the validity of the results since the comparisons between experimental splits and control devices were only performed within each experiment using identical Vg conditions.) At an I_{Off} of 20 pA/μm, excellent I_{on} values of 1180 and 405 μA/μm are obtained for N and P FETs respectively (Figs. 6.20 and 6.21).

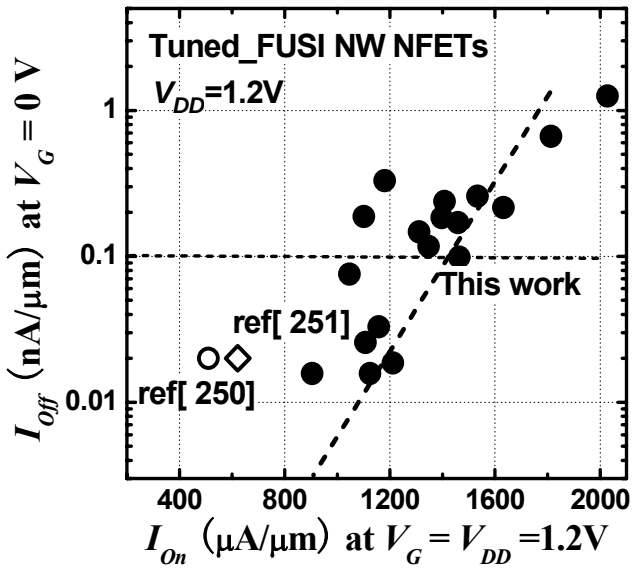


Fig. 6.20: I_{on}-I_{Off} plot of Tuned_FUSI NW NFETs. Significant enhancement obtained compared to LSTP benchmark work [250, 251]. At 20 pA/μm, the I_{on} is 1180 μA/μm.

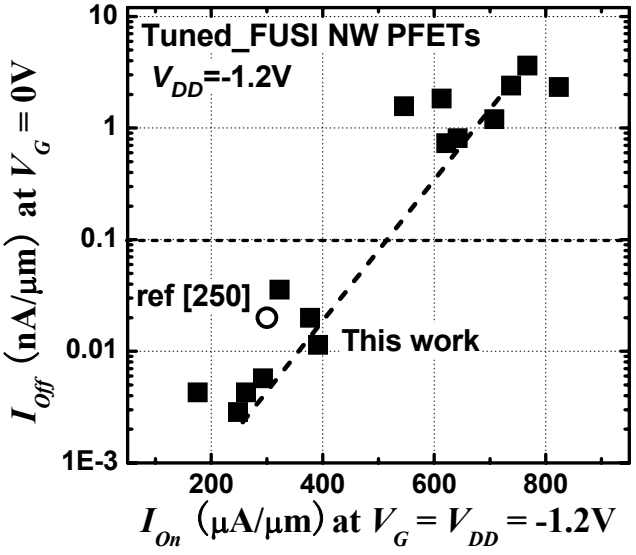


Fig. 6.21: I_{on}-I_{Off} plot of Tuned_FUSI NW PFETs. Significant enhancement obtained compared to LSTP benchmark work [250]. At 20 pA/μm, the I_{on} is 405μA/μm.

Dramatic I_{on} enhancement (especially for PFET) is expected with moderate T_{ox} reduction and aggressive L_G scaling, due to the excellent short channel control of the GAA NW structure.

Fig. 6.22 shows the transfer characteristics of Tuned-FUSI GAA NW inverters with symmetrical V_T. In order to compromise the mobility difference between n-FET and p-FETs, the design of the inverter P:N is 2 NWs:1 NW. Excellent noise margins has been achieved with NMH of 0.575V and NML is 0.408V. (V_{OH}=1.16V, V_{IH}=0.585V, V_{IL}=0.465V, V_{OL}=0.0569V). The transition voltage is nearly half value of the power supply voltage (V_{DD}/2), which implies the symmetrical threshold voltage of n-FETs and p-FETs. High inverter voltage gain was obtained for V_{DD} from 1.2V down to 0.6V (Fig. 23, Inset shows transfer characteristics), which reveals that such FUSI NW FETs has a possible potential for LSTP applications.

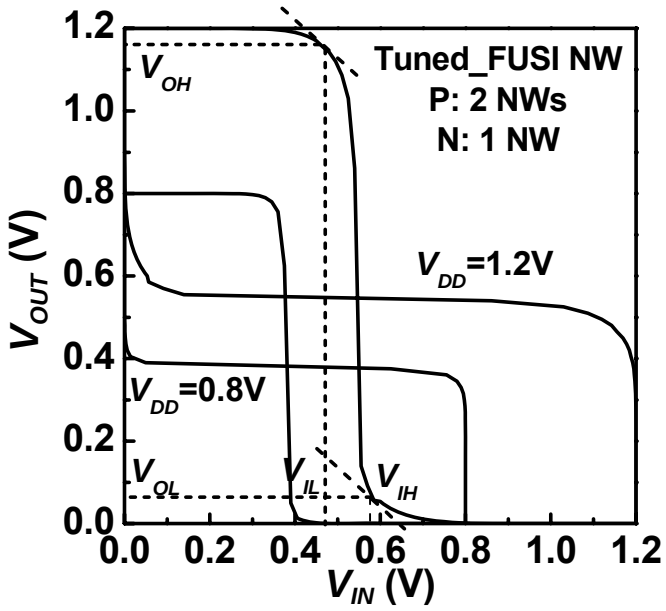


Fig. 6.22: Inverter transfer characteristics of Tuned_FUSI NWs. A sharp transfer obtained with excellent noise margin of NMH= 0.585V, NML= 0.407V at V_{DD}=1.2V.

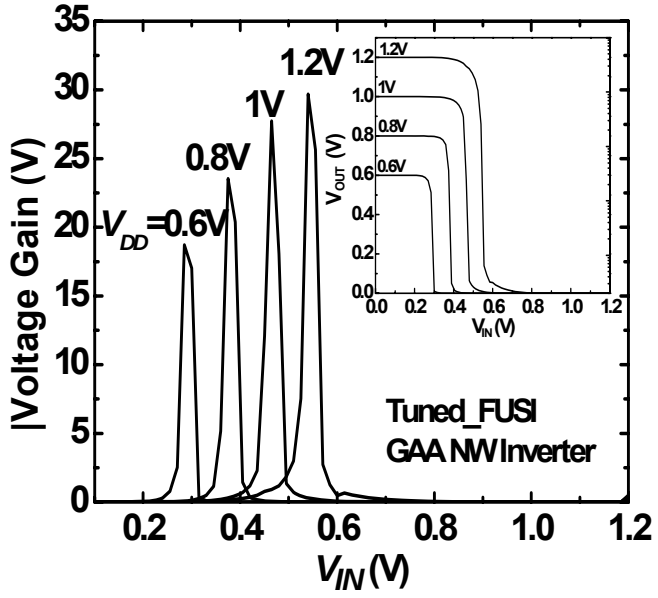


Fig. 6.23: Voltage gain characteristics of Tuned_FUSI NW Inverter at different V_{DD}. High inverter gain was obtained down to V_{DD}=0.6V, indicating the suitability of GAA NW inverters for low V_{DD} operation.

Besides the inverter nanowire circuit integration, ring oscillators with different stages are also fabricated in this work. Shown in Fig. 6.24, ring oscillator with the 101 stages exhibited 220 ps delay per stage at V_{DD} of 1.6V. Although the nanowire devices have relatively larger gate length, it can still obtain the reasonable stage delay.

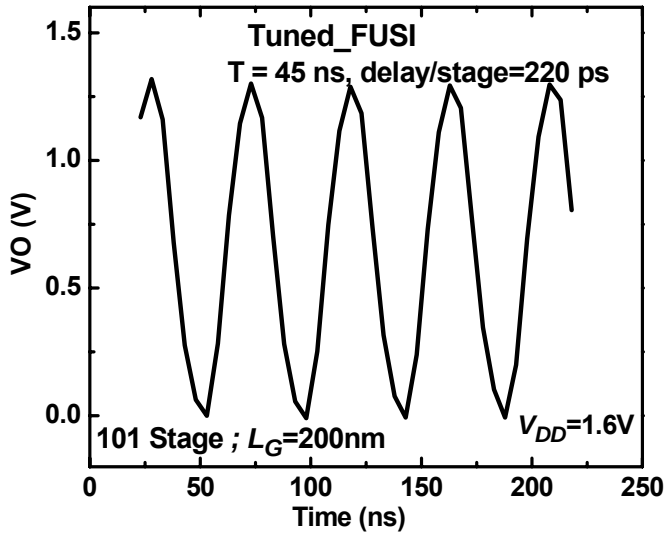


Fig. 6.24: Tuned_FUSI GAA NW ring oscillators output characteristics of 101 stages at power supply voltage of V_{DD}=1.6V. The per stage delay obtained is 220ps.

We also investigate the ring oscillator behavior at different power supply voltages. As shown in the Fig. 6.25, 6.26, as the power supply voltage increases, the output voltage magnitude of the ring oscillator increases. The gap between the power supply and output voltage is small when the power supply voltage reduced down to 0.8V. As the V_{DD} increases, it has been observed that the delay time reduces. At V_{DD} of 0.8V, the delay per stage is around 370 ps, which indicated potential for integration low standby power circuits applications.

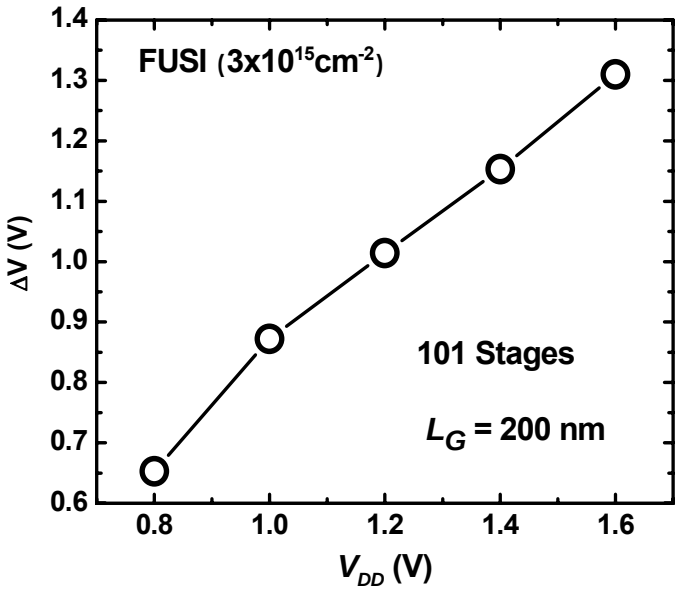


Fig. 6.25: Ring oscillator behavior at different power supply voltages. As V_{DD} decreases, the ΔV (magnitude of output voltage) drops.

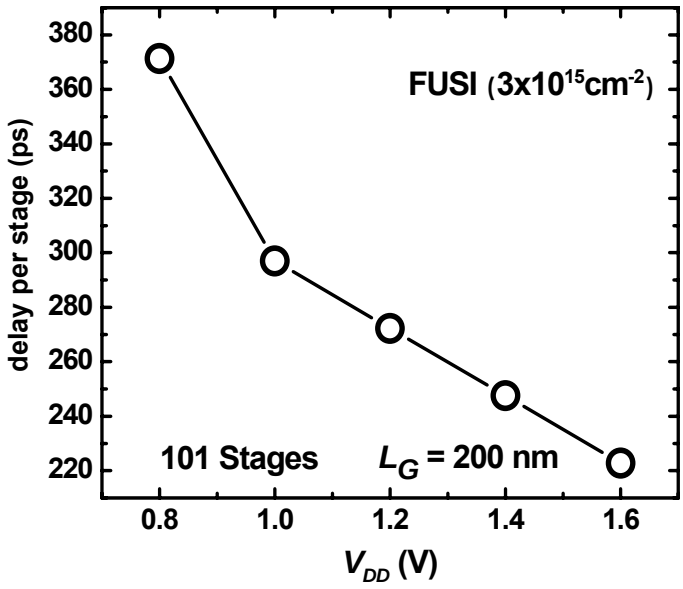


Fig. 6.26: Ring oscillator behavior at different power supply voltages. As V_{DD} decreases, the delay per stage increases.

6.3.4 FUSI Gate-Induced Stress Effects on Nanowire Channel

Due to the compliant nature of the narrow nanowires, stress in the gate electrode will be strongly coupled to the nanowire channel. NiSi has a tensile intrinsic film stress. As such, the FUSI gate electrode will exert a compressive stress on the nanowire channel in the <110> carrier transport direction (Fig. 6.27). This causes valence band deformation, reduces the hole conductivity mass and enhances the hole mobility in the FUSI gate NW PFETs over that of the poly-Si gate NW PFETs. Conversely, electron mobility is degraded by the compressive channel stress. Hence, it is important to examine the effect of gate-induced stress on device performance.

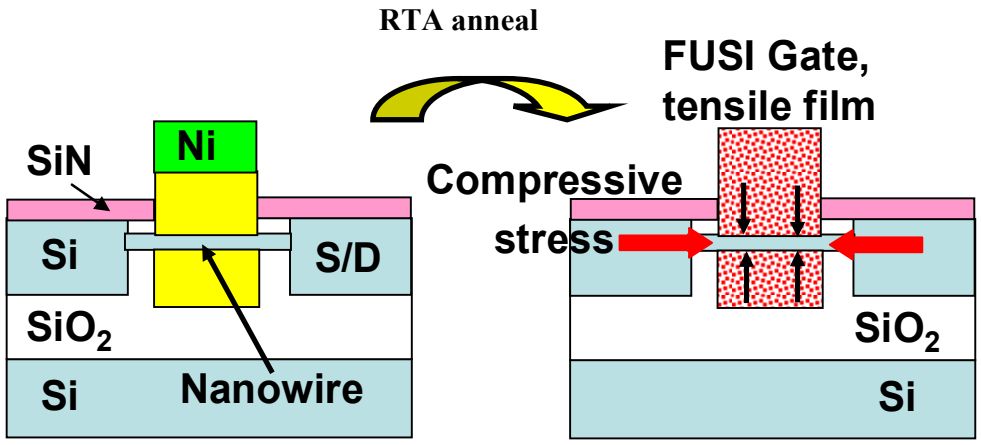


Fig. 6.27: Schematics of silicidation process. The tensile FUSI gate film induces compressive channel stress. All FUSI silicidation processes were performed at 420ºC. After FUSI, an additional split (FUSI_HT) went through a further stress-enhancing RTA anneal at 550ºC to increase the silicide stress, and its corresponding channel stress.

It has been reported that a post-silicidation anneal at temperatures above 500°C significantly increases NiSi film stress [252]. An additional FUSI gate wafer split (FUSI_HT), which includes an additional stress-enhancing anneal at 550°C, was also fabricated for comparisons.

The I_D-(V_G-V_T) transfer characteristics for FUSI_HT and poly-Si splits are shown in Fig.6.28 (NFETs) and Fig. 6.29 (PFETs). There is degradation in drive current for FUSI_HT compared over poly-Si splits (Fig. 6.28). The transconductance for both splits are shown in the inset. Due to the compressive channel strain, the electron mobility will degrade, and the transconductance of the FUSI_HT degrades accordingly for NFETs. On the other hand, the channel is under compressive stress and the hole mobility will increase, thus the drive current of FUSI_HT will be enhanced compared to the poly Si splits for PFETs (Fig. 6.29).

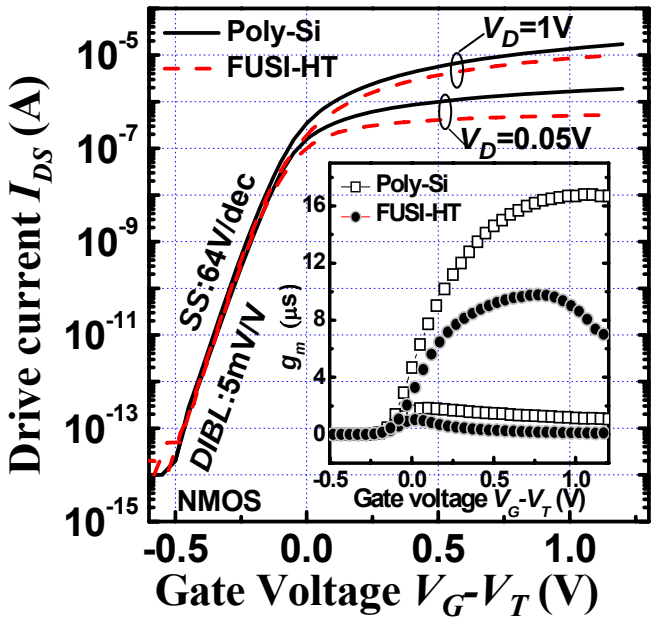


Fig. 6.28: *I-V* transfer characteristics of high stress FUSI split cover poly-Si split with the transconductance characteristics shown as inset. Due to the channel is under compressive strain, the performance of the FUSI_HT NFETs degrades.

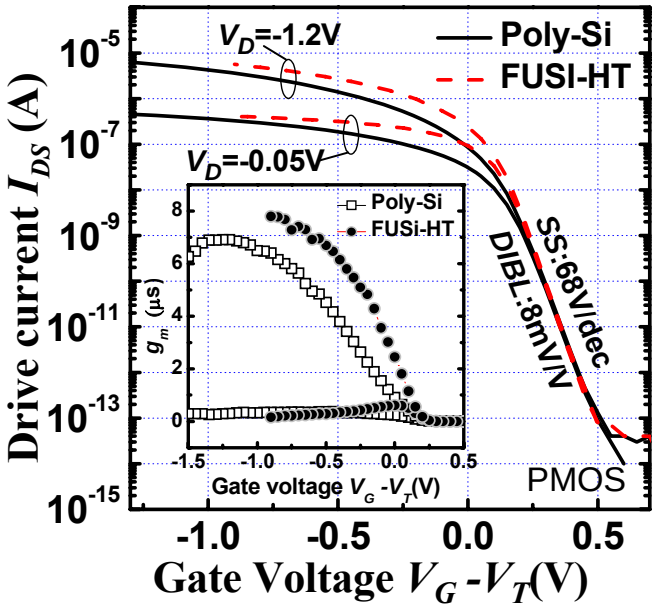


Fig. 6.29: *I-V* transfer characteristics of high stress FUSI split cover poly-Si split with the transconductance characteristics shown as inset. Due to the channel is under compressive strain, the performance of the FUSI_HT PFETs enhanced.

Peak linear transconductance $G_{m,lin}$ is related to the carrier mobility μ_{eff} and gate capacitance C_{ox}. By extracting $G_{m,lin}$, the μ_{eff} and C_{ox} changes due to the FUSI processes can be gauged. The FUSI_HT NFETs are degraded by 46% compared to Poly-Si NFETs shown in Fig. 6.30 (a). This is a combined result of both electron mobility degradation and C_{ox} increase. The FUSI_HT PFETs have enhanced $G_{m,lin}$ of 111%, which can be attributed to both stress-induced hole mobility enhancement and C_{ox} increase (elimination of poly-depletion in metal gate) (Fig. 6.30 (b)). The results confirm the immense impact of FUSI gate stress effects, which are exploited to reduce the performance gap between N and PFETs.

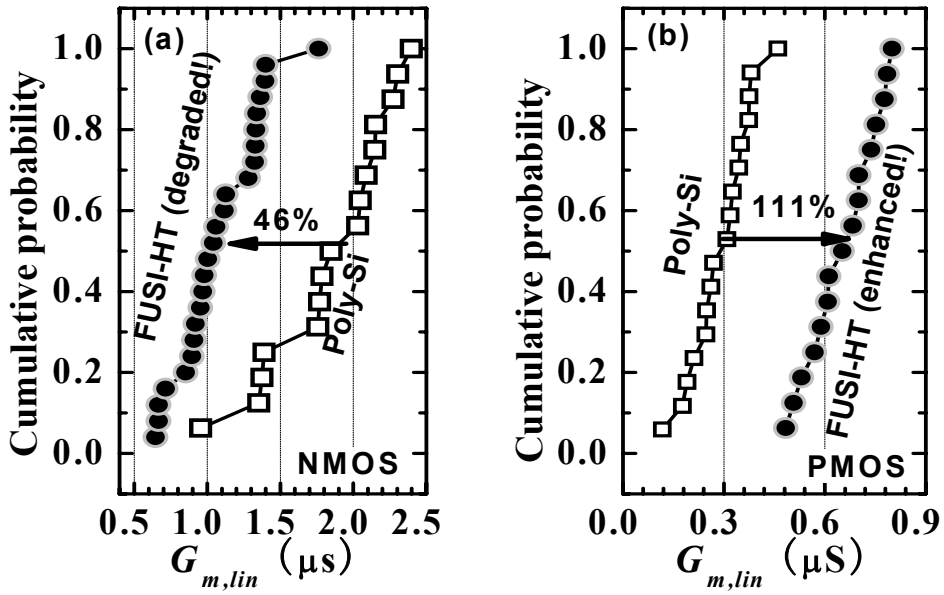


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Fig. 6.30: Cumulative distribution of peak g_m at linear region for both N and P FETs. Due to the gate-induced compressive channel stress, G_m of FUSI_HT is degraded for NFETs while enhanced for NW PFETs. For Tuned_FUSI no significant reduction was obtained for NW NFETs, while large enhancement was obtained for PFETs.

Statistical study plot of transconductance versus DIBL were shown in Fig.6.31. Comparable DIBL values are obtained for both FUSI_HT and Poly Si splits, which indicate that this high temperature anneal process will not degrade the short channel effects for nanowire transistors. Again, enhancement has been achieved for PFET while degradation was observed for NFETs. With the suitable optimization of the annealing steps, it is able to balance transistors performance between NFET and PFETs.

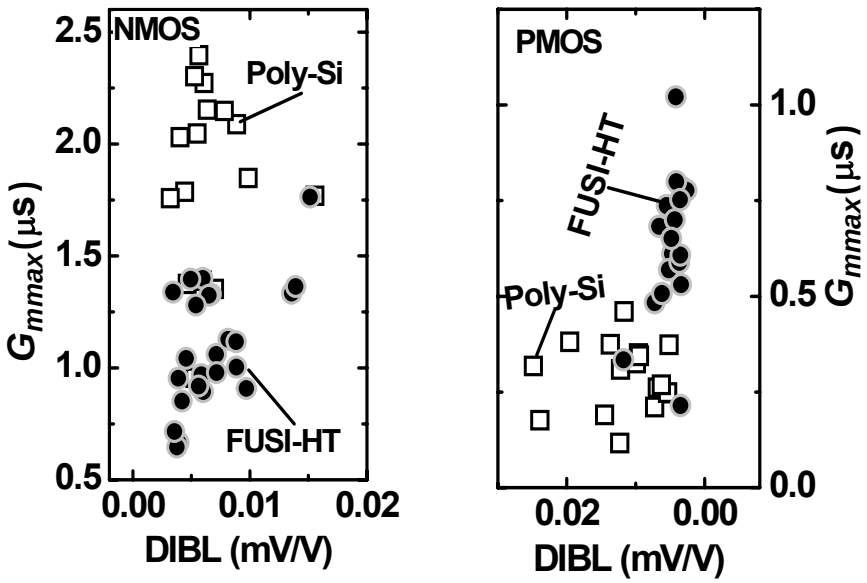

Fig. 6.31: Plot of G_{mmax} with DIBL for FUSI_HT and Poly Si. A clear enhancement is observed for PFETs while degradation for NFETs. Comparable DIBL indicated there is no short channel degradation occurred for the FUSI gate process.

6.4 Conclusions

In this chapter, GAA single metal FUSI gate nanowires CMOS FETs were successfully fabricated. Optimum CMOS V_T values were achieved using a simple and cost-effective metal gate process scheme with V_T tune-ability. Both *I-V* characteristics and EDX results confirmed the successful formation of the wrap-all-around FUSI metal gate. Symmetrical V_T (0.3V for n-FETs and -0.3V for p-FETs) has been obtained through the gate doping impurity segregation process. No degradation on the variation of V_T has been observed for this single metal FUSI gate process. It was shown that gate-induced stress effects help to narrow the performance gap between NFETs and PFETs by enhancing PFET performance greatly. This is helpful for building small-footprint balanced NW inverters. Excellent inverter transfer characteristics of FUSI GAA NW FETs and with the ring oscillator which exhibited 220ps per stage delay. This indicated high potential for LSTP circuit applications.

CHAPTER 7

7. CONCLUSION AND OUTLOOK

Nanowire technology and its applications have gained much attention in the engineering and scientific community over the past few decades. The nanowire transistors extend the CMOS roadmap beyond that which is possible with planar transistors. In order to boost the performance of nanowire transistors, several techniques for addressing the performance bottlenecks for top-down approach nanowire transistors were investigated in this work.

7.1 SiGe Nanowire Transistors with High-k/Metal Gate Integrations

Utilization of SiGe/Ge as channel materials dramatically enhanced transistor performance. SiGe/Ge has high carrier mobility compared to Si. As such, SiGe/Ge channel based nanowire transistors exhibit higher carrier velocity over Si channel based transistors. SiGe/Ge nanowire channel transistors show a large drive current enhancement (×4 times) over conventional Si channel transistors. In the work, the utilization of SiGe/Ge as the channel material was shown to enhance the performance as a result of enhanced carrier mobility. This indicates that replacing the channel material can be a viable method of improving the nanowire channel mobility.

In Chapter 3, SiGe nanowire transistors were successfully integrated on SOI substrates. The growth of the SiGe film was also investigated for reducing defect formation in the epitaxial film. In order to achieve higher Ge concentration within the Ge nanowire channel, the Ge condensation method was explored in this work. The cyclic oxidation and annealing processes were found to condense the Ge and at the same time

form a uniform SGOI film. By using this Ge condensation technique, Ge rich (70%) nanowire transistors with HfO_2/TaN gate stack were fabricated on SOI substrates. Using a two-step Ge condensation technique, a lateral hetero-structure from source-channel-drain transistors was formed. Such devices exhibited higher drive current properties compared to homo-junction devices, showing a reduced backscattering ratio. With further innovations on the channel material, nanowire PFETs with high hole mobility Ge channel are expected performed even better. This exploration on channel engineering provides a possible way of improving the mobility and performance of the nanowire transistors.

7.2 SiGe/Si Core/Shell transistors fabricated on Bulk Si substrate

Driven by the motivation of cost reduction, further work was done on SiGe channel nanowire transistors. It is desirable to develop a simple and cost effective way for SiGe nanowire transistor fabrication. The fabrication of nanowire transistors on bulk substrates is hence an attractive alternative.

In Chapter 4, the core/shell structure transistor was demonstrated, with the core/shell structure consisting of Ge core and Si shell respectively. In addition, due to the lattice constant mismatch between SiGe and Si, the SiGe/Si core shell nanowire structure showed strained-induced drive current improvements. A reasonable SS value was obtained as the Si shell served as an interfacial layer between SiGe and the SiO_2 gate dielectric. SiGe film strain was further studied in Chapter 4. The SiGe film strain was calculated to be -0.5% and is beneficial to the nanowire PMOS FETs. Double G_m peaks were observed, indicating two kinds of channel conductance mechanisms: SiGe core channel conduction and Si shell surface channel conduction. Further process optimization is expected to result in a fully wrap-around core/shell structure for even better performance.

7.3 Metallic NW S/D Contacts Technique for Ultra-Scaled GAA Si NW Transistors

As the gate length scales down, the channel resistance scales down correspondingly. At very short gate lengths, the source and drain extension resistance becomes a huge fraction of the total resistance. Since the dimension of the nanowire is small, the resistance of the nanowire contact region is also a significant portion. Therefore, the drive current performance of ultra-scaled GAA Si NW FETs is limited by the large parasitic resistances.

In Chapter 5, by utilizing the ultra-thin Ni silicidation technique, nanowire transistors with metallic nanowire S/D contacts were successfully fabricated. This significantly reduced the series resistances for the ultra-thin S/D nanowire transistors. Partially silicided Si nanowire contacts were able to reduce the series resistance significantly. The S/D extension resistance is reduced greatly by the proper optimization of the silicidation and junction profile. Therefore, high performance and high drive current was achieved in the ultra-scaled nanowire transistors. The drive current measured in 8 nm gate length Si nanowire transistors with Ni silicided S/D was as high as ~3.74 mA/μm. The data presented indicates that the metallic nanowire S/D technique has laid the foundation for high performance nanowire transistors.

7.4 GAA FUSI Structure with Dual Work Functions Si NW Transistors

Nanowire channels of small dimensions are typically intrinsically doped. This avoids the random dopant fluctuation effect and also improves mobility as a result of reduced coulombic scattering. However, this also means that using n^+ or p^+ poly-Si gate electrodes (band-edge work functions) will set the device threshold voltage incorrectly.

Without a correct threshold voltage and a means of tuning it, the implementation of nanowire circuits will be very challenging.

In Chapter 6, single metal FUSI gate nanowire transistors with gate silicidation induced dopant segregation was demonstrated. The desired V_T was obtained in the intrinsic Si nanowire transistors for both PMOS and NMOS. During the Ni silicidation process of the gate, the gate dopants were rejected from the silicidation film and segregated towards gate dielectric interface. The work function can be tuned by the concentration of the gate dopant impurity. By varying the gate dopant concentration, the work function can be controlled, so as to achieve the desired threshold voltage.

The FUSI induced dopant segregation effect has been used to successfully tune the nanowire gate work function. Thus, both PMOS and NMOS showed desirable and symmetrical threshold voltage values. Setting the V_T correctly results in very low off-state leakage due to the nanowire transistor's excellent subthreshold swing. This makes them suitable for low standby power applications.

7.5 Recommendations for Future Research

Nanowire transistor research is relatively new, which indicates that the technology is still being developed and explored. The research areas covered in this work is not exhaustive. However, it identifies several promising candidates to address specific important problems. Apart from this, there are also other problems regarding high performance nanowire devices which have yet to be fully solved. These other aspects should be studied for possible eventual adoption of high performance nanowire transistors by the semiconductor industry. These include:

(1) Novel silicidation material [253-255] which can be explored to reduce the series resistance such as Er, Pt. The nanowire structure for the nanowire silicidation can also be

an interesting area to study with regards to the resistivity property for nanostructures. Further high resolution TEM and material study such as EDX in this metallic nanowire region can be performed. The strain property in the metallic nanowires can also be studied, since the effect of silicide induced channel strain can affect the drive current performance.

(2) C-V measurements which can be carried out in order to investigate the intrinsic properties of nanowire transistors. Some possible gate interface traps and defects across the dielectric can be identified and quantified [256, 257]. The mobility of the carriers in the nanowire channel can also be extracted from the C-V curves. Low temperature measurements can also be carried out to analyze the low temperature carrier transport behavior [258].

(3) Strain engineering should also be explored in the nanowire transistors. SiGe/Ge S/D stressor can be a possible way to induce channel strain, while simultaneously reducing the S/D extension series resistance [130, 131]. The strain effects for the S/D stressors can be further investigated; and will provide a better comparison between nanowire channel devices and conventional devices. Gate electrode induced strain can also be carried out. The carrier mobility would change significantly according to the strain effect. Three-dimensional strain effects can be further evaluated so as to fully understand the effect of strain on such nanostructures.

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Appendix A: Publication List

Journal Publications

[1]. **Y. Jiang**, N. Singh, T. Y. Liow, W. Y. Loh, S. Balakumar, K. M. Hoe, C. H. Tung, V. Bliznetsov, S. C. Rustagi, G. Q. Lo, D. S. H. Chan and D. L. Kwong, "Ge-Rich (70%) SiGe Nanowire MOSFET Fabricated Using Pattern-Dependent Ge-Condensation Technique", ***IEEE Electron Device Letters***, v 29, n 6, June 2008, pp. 595-598.

[2]. **Y. Jiang**, T. Y. Liow, N. Singh, L.H. Tan, G. Q. Lo, D. S. H. Chan and D. L. Kwong, "Nickel Salicided Source/Drain Extensions for Performance Improvement in Ultra-Scaled (Sub 10nm) Si-nanowire Transistors", ***IEEE Electron Device Letters***, v 30, n 2, Feb. 2008, pp. 195-197.

[3]. **Y. Jiang**, N. Singh, T. Y. Liow, P. C. Lim, S. Tripathy, G. Q. Lo, D. S. H. Chan and D. L. Kwong, "Omega-Gate P-MOSFET with Nanowire-like SiGe/Si Core/Shell Channel", ***IEEE Electron Device Letters***, v 30, n 4, April. 2009, pp. 392-394.

[4]. **Y. Jiang**, N. Singh, T. Y. Liow, G. Q. Lo, D. S. H. Chan, and D. L. Kwong, "Reduced carrier backscattering in heterojunction SiGe nanowire channels", ***Applied Physics Letters,***, v 93, issue 25, 0003-6951, Dec. 2008.

[5]. **Y. Jiang**, T. Y. Liow, N. Singh, M. Bosman, A.L. Bleloch, L.H. Tan, G. Q. Lo, D. S. H. Chan and D. L. Kwong, "Intrinsic Si Nanowire CMOS Devices with FUSI Gate-All-Around Metal Gate Architecture", submitted to ***IEEE Trans. Electron Devices.*** to be submitted.

[6]. **Y. Jiang**, W. Y. Loh, D. S. H. Chan, Y. Z. Xiong, C. Ren, Y. F. Lim, G. Q. Lo, and D. L. Kwong, "Flicker-Noise and its Degradation Characteristics under Electrical Stress in MOSFETs with Thin Strained-Si/SiGe Dual-Quantum-Well", ***IEEE Electron Device Letters***, v 28, n 7, July 2007, pp. 603-605.

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Conference Publications

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Patents

[18]. **Y. Jiang**, N. Singh, S. Balakumar, G. Q. Lo, "High-speed nanowire semiconductor devices based on hetero-structure and formation",2007.