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SIMULATION OF SUPERJUNCTION MOSFET DEVICES

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NATIONAL UNIVERSITY OF SINGAPORE
2005

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ABSTRACT

Interdiffussion problem is unavoidable in superjunction device fabrication process. The practical superjunction device performance under interdiffusion influence is studied by extensive simulation and described in the thesis.

Partial SOI superjunction LDMOS structure is proposed in recent years in undergraduate projects. 3-D simulation by DAVINCI is done to study its performance. Simulation considers all the possible structure variations of the device such as p, n column width variation and gate structure variation. The performances under different structures are compared to select the best structure. Simulation results show that the performance of partial SOI device has broken the silicon limit. Finally, the detail process flow is proposed for the future fabrication.

Keywords: Superjunction devices, power devices, ideal silicon limit, interdiffusion, partial SOI superjunction LDMOS

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DECLARATION OF ORIGINAL CONTRIBUTIONS

The author would like to declare the original contributions based on the research as follows:

1. The practical superjunction performance under interdiffusion influence is investigated and described in chapter 3.

2. Simulation of partial oxide superjunction LDMOS structure is described in chapter 4.

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SUMMARY

The research work described in thesis is conducted around superjunction MOSFET devices. Two aspects of superjunction MOSFET devices are investigated through simulations. Firstly, the influence of interdiffusion on practical superjunction device performance is investigated. Based on extensive simulation results, the practical superjunction performance curves are arrived. In addition, some empirical equations such as concentration equation, specific on resistance equation are derived. The performance curves are compared with the theoretical superjunction curves to show the interdiffusion influence. The equations can give guidance in superjunction device design in practical conditions.

The second part of thesis presents results of detailed 3-D simulations of partial SOI superjunction LDMOS using DAVINCI, a 3-D simulator. The simulation work investigates the influence of the structure variations on the device performance. The structure variations include p, n column width variation and gate structure variation. The simulation results show that "all gate" structure with the smallest simulated n column width has the best performance compared with "trench gate" and "planar gate" structure. And the device performance has broken the silicon limit. To prepare for future fabrication, detailed process flow is proposed in the final part of thesis.

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LIST OF SYMBOLS

α	Ionization coefficient
L	Depletion length(μm)
N_D	Drift region concentration(cm^{-3})
V_{BR} or V_{br}	Breakdown voltage(V)
ε_s	Permittivity of Silicon
q	Elementary charge(C)
E	Electric field (V/cm)
R_{on}	On resistance(Ω)
R_{n+}	Source resistance(Ω)
R_{ch}	Channel resistance(Ω)
R_{acc}	Accumulation layer resistance(Ω)
R_{drift}	Drift region resistance(Ω)
R_{n+}'	Drain resistance (Ω)
$R_{on,sp}$	Specific on-resistance ($\Omega \cdot cm^{-2}$)
l_{drift}	Length of drift region (μm)
μ	Electron mobility($cm^2/V \cdot s$)
A	Cross-sectional area of current flow (cm^2)
N_A	Acceptor doping concentration(cm^{-3})
N_D	Donor doping concentration(cm^{-3})
E_y	The y component of the electrical field(V/cm)
E_0	Constant component of E_y(V/cm)
E_1	E_y - E_0 (V/cm)

V_B	The applied reverse voltage(V)
E_{1n}	The maximum value of E_1 along the middle of n column(V/cm)
E_{1p}	The maximum value of E_1 along the middle of p column(V/cm)
$V_{\substack{lateral \\ merge}}$	Lateral merge voltage of p, n column width(V)
N_{p^+}	Concentration in p+ region(cm^{-3})
x_n	The depletion depth in n column at $V_{\substack{lateral \\ merge}}$(μm)
E_C	The critical electrical field(V/cm)
E_{max}	Maximum electric field(V/cm)
w	P, n column width(μm)
E_A	Electrical field at p+/n junction (V/cm)
W_m	The column width at Merge point of practical concentration and ideal concentration(μm)
W_d	Depletion width(μm)
W_{padox}	Pad oxide thickness(μm)
$W_{nitride}$	Nitride thickness(μm)
W_{sideox}	Side wall oxide thickness(μm)
W_{si}	Deep trench silicon thickness(μm)
THW	Half width of total structure(μm)
HW_n'	Half width of n column before oxidation(μm)
HW_n	Half width of n column after oxidation(μm)
HW_p	Half width p column(μm)
HW_{dp}	Half width of deep trench(μm)
HW_{sh}	Half width of shallow trench(μm)

LIST OF ABBREVIATIONS

MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
DMOS	Double-diffusion MOS
LDMOS	Lateral DMOS
VDMOS	Vertical DMOS
UMOS	U-shaped trench Gate MOS
SOI	Silicon on Insulator
SJ	Superjunction
PSOI	Partial SOI
BOX	Buried oxide

Chapter 1

Introduction

Power devices are mainly used as power switches in various systems such as high voltage DC transmission, motor drive, transportation, induction heating and communications [1].

Power MOSFETs, which are based on the original field effect transistors introduced in 70s, are the most popular power device in today's era. The power MOSFET is a unipolar, majority carrier and voltage controlled transistor. It has the benefit of fast switching and simple gate drive circuitry. Therefore, it is suitable for high frequency integrated circuits.

Unfortunately, power MOSFETs have one major drawback — high on-state conduction loss. The device doping is limited by the requirement to support high breakdown voltage. The trade-off relationship between specific on-state resistance ($R_{on,sp}$) and breakdown voltage (V_{br}) has been defined as "silicon limit"[1][2], which shows a more than square relationship ($R_{on,sp} \sim V_{br}^{2.5}$). The relationship indicates that the on-resistance of power MOSFETs increases rapidly with the increase of breakdown voltage, which makes them only suitable for low voltage (<200V) applications.

A lot of effort has been put into the improvement of the performance of MOSFETs. Earlier effort can only make the performance of power MOSFETs as close as possible to the "silicon limit". Recently, some novel ideas have been proposed to overcome the "silicon limit" [3-11]. These ideas are based on modification of the one-type doped

drift region to add an opposite doped region to it. This kind of structure is defined as superjunction structure [2]. Devices based on superjunction structure have been fabricated and made commercially available [9].

1.1 History of superjunction device

The earliest superjunction concept appears at D.J.Coe's patent [3]. The superjunction device structure is shown in fig. 1.1[3]. The superjunction structure appears at the drift region, region 3. Region 3 comprises of first regions 11 of a first conductivity type (n-type) and second regions 12 of the opposite, second conductive type (p-type). Regions 11 are interleaved with regions 12. The existence of p-type region helps the depletion of the whole drift region. Thus, higher breakdown voltage can be achieved by this kind of structure.

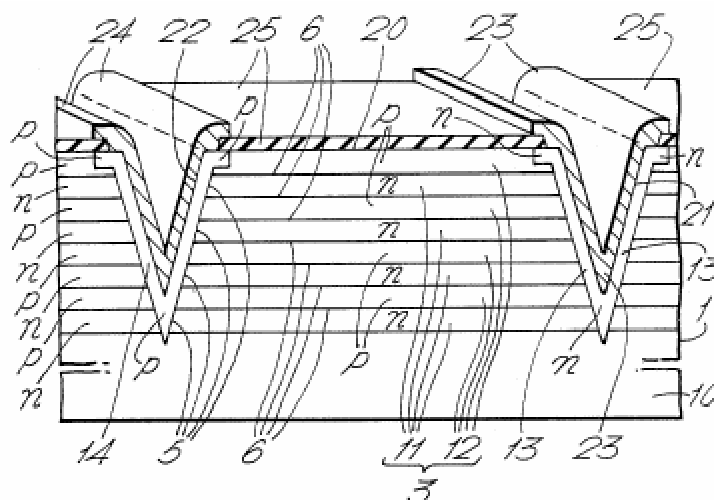
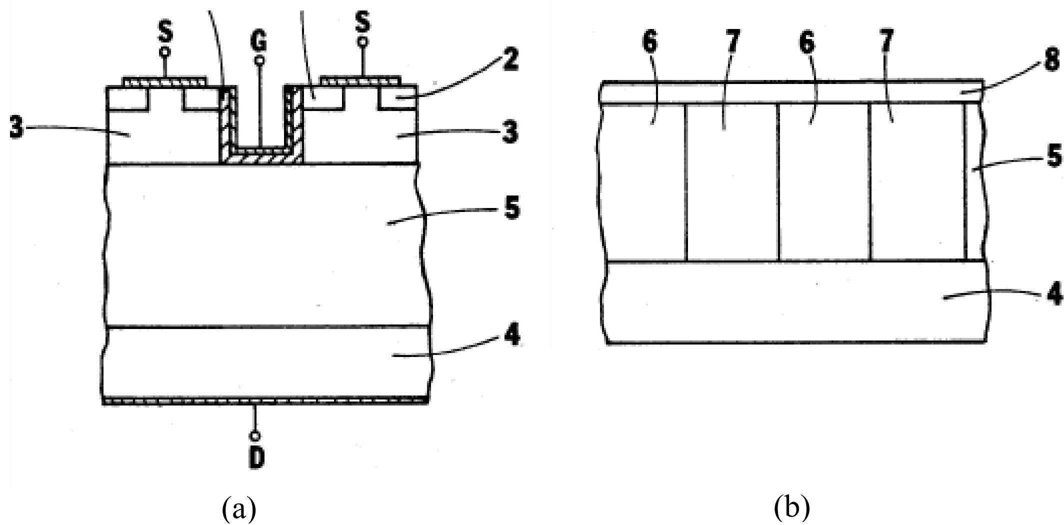


Fig. 1.1 Superjunction device structure extracted from [3]

Later on, the development of the concept is divided into two groups. One group is similar to the original concept to use the buried opposite doped region or floating opposite doped regions [4, 5]. The other group uses the alternatively stacked p, n region or multi-RESURF superjunction region as the drift region [6-11]. This kind of structure is shown in Fig. 1.2. Fig. 1.2(a) shows a vertical RMOS structure. The popular name for RMOS is UMOS. The drift region is region 5. Fig. 1.2(b) shows the drift region of the RMOS structure, which comprises of oppositely doped region 6(n-type) and region 7(p-type). Region 6 and region 7 are alternatively stacked; each n-type region is surrounded by the neighbor p-type regions and vice visa. Thus, when the drift region is fully depleted, the n-regions and the p-regions contribute charges with opposite signs, and the fields introduced by them cancel each other out for most part. This is called the charge compensation principle. Actually, the second group concept is widely recognized as the superjunction concept because the charge compensation principle is used in the device design, which is firstly proposed by X.-B. Chen's patent [6].

Although the devices discussed in these patents and papers are actually superjunction devices, the name of "superjunction" is firstly prominently proposed by T. Fujihira [2]. In this paper, a summary of various superjunction device structures are given and the general equation for superjunction device is derived for the first time. Later, other papers give some different superjunction equations. All these equations show a linear or slightly more than linear relationship between $R_{on,sp}$ and V_{br} [4][11]. Compared with the more than square relationship in "silicon limit", the performance of superjunction device has overcome the "silicon limit".



(a) (b)

Fig. 1.2 Superjunction RMOS device extracted from ref.6
(a)RMOS structure (b) drift region with superjunction structure of RMOS structure

In history, the development of the two kinds of superjunction devices – vertical devices and lateral devices is not parallel. Till now, most of the developed superjunction devices are vertical devices. Vertical superjunction devices are realized by various fabrication technologies such as COOLMOS™ technology, STM, VTR-DMOS and PFVDMOS etc.[9][12-16]. Due to the thermal process involved in fabrication, the dopant - interdiffusion problem is unavoidable in most of the fabrication technology. The interdiffusion between the p, n column of superjunction structure will affect the device performance. One part of the research work is to investigate the interdiffusion influence on practical superjunction device performance.

Recently, the superjunction concept is also used on lateral devices [11][17-22]. Some new concepts such as unbalanced superjunction structure, double gate, and SOI structure are proposed to improve the lateral superjunction device performance. The voltages of these lateral devices are in medium range - 120V or 150V. The research of

the lateral superjunction devices is still on simulation stage [11][17-22]. The few fabricated devices are on bulk wafer [22].

In this project, the performance of a partial SOI superjunction LDMOS at breakdown rating 120V is investigated through extensive simulation. Compared with previous lateral device, the device uses partial SOI technology and multi-gate structure to improve its performance. The fabrication probability of the device is also explored.

1.2 Objectives

This research is,

(a) To gain a thorough understanding of superjunction Theory;

(b) To investigate the practical superjunction performance under the interdiffusion influence;

(c) To simulate the performance of partial SOI superjunction LDMOS device at breakdown rating of 120V and develop a process flow based on current technology.

1.3 Thesis Outline

The thesis covers all the research work during the candidature, which include superjunction theory exploration, practical superjunction performance simulation, partial SOI superjunction LDMOS performance simulation and fabrication exploration.

The thesis is divided into six chapters:

Chapter 1 – The pros and cons of power MOSFETs are presented followed by the history of superjunction devices. The scope of the research work is presented afterwards.

Chapter 2 – The superjunction theory is reviewed and the superjunction device performance equation is derived based on the theory. The present state of the superjunction device development is provided. This chapter provides the theoretical basis of the whole research work.

Chapter 3 – Since the interdiffusion problem is unavoidable in the fabrication technology, the practical superjunction performance under interdiffusion influence is investigated based on extensive simulation work. The research work summarized in this chapter can give guidance for superjunction device design in practical condition.

Chapter 4 – The extensive simulation work of partial SOI superjunction LDMOS is summarized in this chapter. The device structure and operation is discussed in detail. Based on the proposed process steps, the simulation work is done to test its performance. The further improvement of device performance by changing gate structures are also discussed and tested by simulation.

Chapter 5 – The detailed process flow for all gate partial SOI superjunction LDMOS is proposed in this chapter. The process flow is illustrated by 3-D figures with detailed explanation.

Chapter 6 – This chapter gives the summary of the whole thesis.

Chapter 2

Superjunction (SJ) device theory and analyses

It has been mentioned in last chapter that the performance of conventional power MOSFETs is constrained by "silicon limit" [1] [2]. Many efforts have been put into improving the conventional device structure. Finally, the invention of superjunction structure greatly improved the device performance [3-11]. In this chapter, the analysis of conventional device is firstly provided with the emphasis on "silicon limit". Then, performance of superjunction device, which aims to break "silicon limit", is discussed in detail. Finally, the realization of superjunction structure in various devices is reviewed, and problems encountered are summarized.

2.1 Power MOSFETs Basics

The most popular structure of power MOSFETs is the DMOSFET structure shown in Fig. 2.1[1]. The device name is derived from the channel formation process, *double-diffusion* process. The difference between the vertical DMOSFET (VDMOS) and the lateral DMOSFET (LDMOS) is the current flow direction, which is also shown in Fig. 2.1.

As power switch in most of power applications, power MOSFET operates on two states - Off-state and On-state. By applying different control voltage on gate terminal, power MOSFET easily shifts between the two states. Using n-channel MOSFET as example, when the applied gate voltage is below threshold voltage, the device is in Off-state. As a switch, it is "open". Thus, in the Off-state, there will be a small leakage current through the device. If the applied voltage between drain and source is

too high, the device will breakdown and a large leakage current will pass through it. So, the blocking voltage of the device must be high enough for specific application. In the other case, when applied gate voltage is above the threshold voltage, an inverse channel will form below the gate for the device to conduct current. This is the On-state of power MOSFET and corresponding to the “close” state of a switch. In this state, forward current will pass through the power MOSFET and the voltage falling on it should be very small. The conduction loss of power MOSFET is decided by the resistance along the current path.

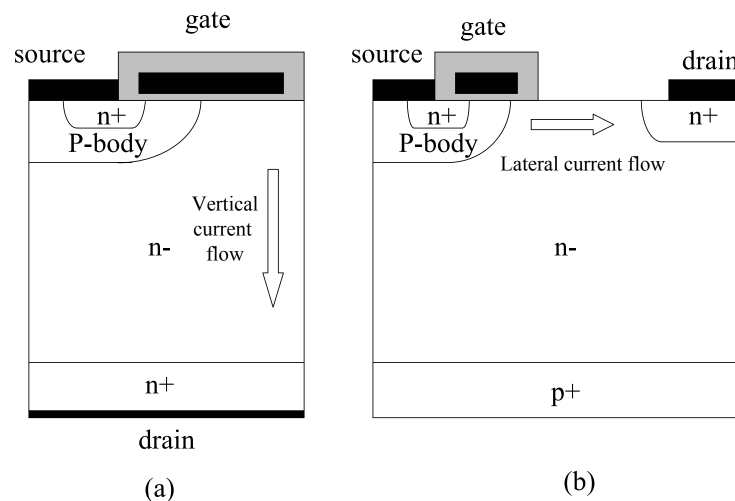


Fig. 2.1 Conventional power MOSFET structure (a) VDMOS structure (b) LDMOS structure

2.1.1 Off-state analysis

The most important parameter for Off-state is the breakdown voltage. During the Off-state operation, the applied reverse voltage is mainly supported by the junction between p-body an n-drift region for both VDMOS and LDMOS. Therefore, the DMOSFET structure can be simplified as a parallel-plane, abrupt p, n junction. The simplified structure, together with electrical field distribution is shown in Fig. 2.2.

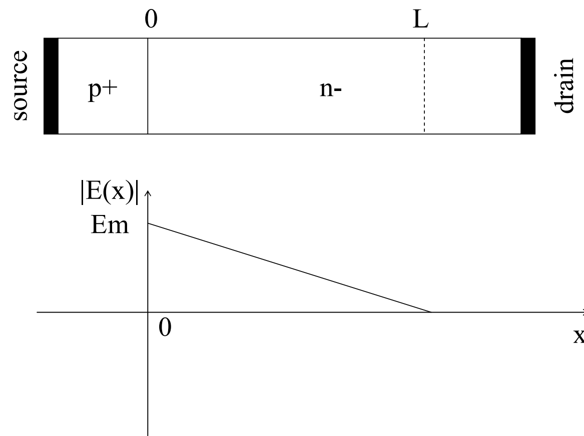


Fig. 2.2 Simplified Off-state structure and electrical field distribution

The applied reverse voltage is primarily distributed over the depletion region from x=0 to x=L. When the free carriers travel through the depletion region, they gain energy from the accelerating electrical field. They also collided with atoms in the lattice. When the applied voltage is increased, the electrical field in the depletion region increases and the free carriers will gain higher energy. If the free carriers gain enough high energy, they will ionize the lattice atoms during collide process. This is called impact ionization. The electron-hole pairs produced by impact ionization are also accelerated by the same electrical field to ionize other lattice atoms. So, the impact ionization is a multiplicative phenomenon that produces a cascade of mobile carriers. The device is considered to undergo avalanche breakdown when the rate of impact ionization approaches infinity. The avalanche breakdown can be identified by the condition that the ionization integral equals to one [1]. This condition can be expressed by:

$$\int_0^L \alpha \cdot dx = 1$$

(2.1)

where α is the ionization coefficient.

The ionization coefficient can be approximately expressed by electrical field *E*:

$$\alpha = 1.8 \times 10^{-35} \cdot E^{7}$$

(2.2)

To find out the relationship between breakdown voltage and various parameters of the device, Poisson's equation is solved. The equation in n- region is given by:

$$\frac{d^2V}{dx^2} = -\frac{dE}{dx} = -\frac{Q(x)}{\varepsilon_s} = -\frac{qN_D}{\varepsilon_s}$$

(2.3)

Combining the equation (2.3) with the boundary condition that the electrical field goes to zero at the depletion edge L provides the solution for electrical field:

$$E(x) = \frac{qN_D}{\varepsilon_S}(x - L)$$

(2.4)

Integrating the electrical field through the depletion region with boundary condition that potential is zero in the p+ region provides the potential distribution:

$$V(x) = \frac{qN_D}{\varepsilon_S}(Lx - \frac{x^2}{2})$$

(2.5)

Substituting electrical field distribution (2.4) to the ionization integral (2.1) and (2.2) gives:

$$\int_0^L 1.8 \times 10^{-35} \left[\frac{qN_D}{\varepsilon_s}(L - x) \right]^7 dx = 1$$

(2.6)

Solving above equation for the depletion length L gives:

$$L = 2.67 \times 10^{10} N_D^{-7/8}$$

(2.7)

Substituting equation (2.7) to (2.5), the breakdown voltage V_{BR} is expressed by drift region concentration N_D :

$$V_{BR} = 5.34 \times 10^{13} N_D^{-3/4}$$

(2.8)

Eliminating N_D from equations (2.7) and (2.8), the depletion length L can be expressed by breakdown voltage V_{BR} :

$$L = 2.58 \times 10^{-6} V_{BR}^{7/6}$$

(2.9)

2.1.2 On-state analysis

During on-state operation, the total resistance along the current flow path determines the voltage drop in the device. The various components of on-resistance are shown in Fig. 2.3.

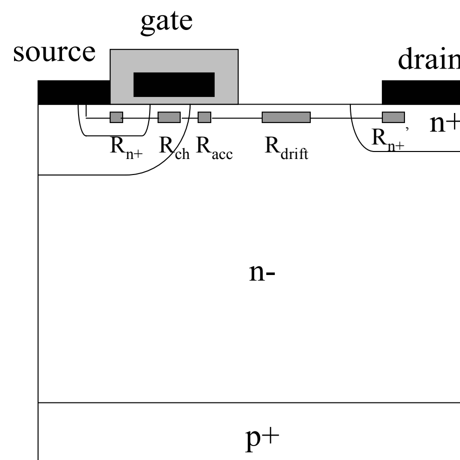


Fig. 2.3 Components of resistance within LDMOS structure on the current flow path

According to Fig. 2.3, on-state resistance of LDMOS can be given by:

$$R_{on} = R_{n+} + R_{ch} + R_{acc} + R_{drift} + R_{n+}^{'}$$

(2.10)

where R_{n+} represents source resistance; R_{ch} represents channel resistance; R_{acc} represents accumulation layer resistance below gate; R_{drift} represents drift region resistance; $R_{n+}^{'}$ represents drain resistance. Normally, the source and drain resistance can be neglected due to the high doping concentration of these regions. Accumulation resistance is also not so important because the overlap region between gate and drift region is very small. The channel resistance and drift region resistance compose of the major part of the total on-resistance. The relevant importance of these two components varies with breakdown voltage ratings. As the breakdown voltage increases, the drift region resistance becomes more and more important [1].

The specific on-resistance of drift region is calculated by:

$$R_{on,sp} = R_{on} \cdot A = \frac{l_{drift}}{q\mu N}$$

(2.11)

where A is the cross-sectional area of current flow.

By substituting equations (2.7) and (2.8) to above equation, the relationship between $R_{on,sp}$ and breakdown voltage is given by:

$$R_{on,sp} = 5.4 \times 10^{-9} \times V_{BR}^{\ 2.5}$$

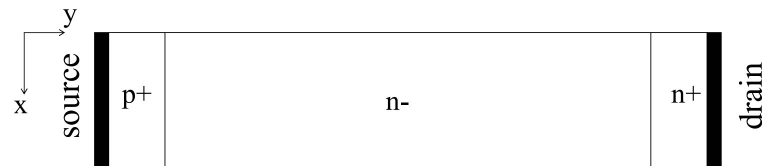
(2.12)

where $q = 1.60218 \times 10^{-19} C$ and $\mu = 1500$ cm^2/V-s are used in the calculation.

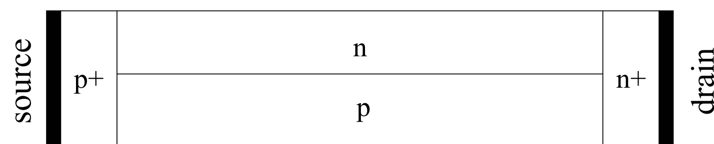
Equation (2.12) is called "silicon limit". This limit shows a more than square relationship between specific on resistance and breakdown voltage for conventional structure. In the following section, the performance of superjunction device will be analyzed. .

2.2 Superjunction Devices

Superjunction devices are designed to break the "silicon limit". The difference between conventional device structure and superjunction device structure is the drift region design. The two kinds of structures used in diode device are shown in Fig. 2.4.



(a) Conventional diode structure with n- drift region



(b) Superjunction diode structure with alternatively stacked p, n column as drift region

Fig. 2.4 Conventional diode structure compared with superjunction diode structure

It's easily noted from Fig. 2.4 that conventional drift region composes of one type epi-layer, either n or p, while the superjunction drift region is made up of two types oppositely doped, alternatively stacked epi-layer. Fig. 2.4 (b) shows an interdigitated p-n column structure, which is most commonly used. Other structures are also possible [23].

2.2.1 SJ characteristics at Off-state

(a) Comparison of breakdown with conventional device

To compare the Off-state performance of SJ device and conventional device, the two structures shown in Fig. 2.4 are used in Medici simulation to test the respective breakdown voltage. The n+, p+ contact region are heavily doped ($N_D=N_A=3\times10^{19}$ cm^{-3}), the n and p strips in superjunction structure, and n- layer of conventional structure are lightly doped ($N_D=N_A=3\times10^{15}$ cm^{-3}). The drift length is 15μm, and n+, p+ region are 2.5μm long. The drift region width is 5 μm. The simulation results show that the breakdown voltage for conventional drift region is 116V, and for superjunction drift region is 338V. It's obvious that by using superjunction structure in drift region, the device can sustain higher reverse voltage.

The improvement of breakdown voltage by using superjunction structure can be better understood through electrical field profiles. The electrical field distributions for the two structures are plotted in Fig. 2.5. As the structure in Fig. 2.4(a) is an effectively one-dimensional structure, there is no variation in the x direction. While, in Fig. 2.4(b), the structure is two dimensional, the electrical field has both x component and y component. For easy analysis, the electrical field is drawn along the outer edge of n

column. In this position, the electrical field only has y component due to the symmetric structure.

Fig. 2.5(a) shows that in conventional drift structure, the field profile is triangle shape, with constant slope and advancing towards drain contact as the voltage increases. In this structure, the depletion boundary moves gradually towards drain as voltage increases. For the superjunction structure, situation is totally different. The p+ region helps the depletion of n column; the n+ helps the depletion of p column; and most importantly p, n column helps the depletion of each other. So, the drift region is totally depleted at a relatively low voltage. After the fully depletion of the drift region, the field profile becomes rectangle shape and eventually moves up as voltage increases. Because the breakdown voltage is simply the area under the field profile when the maximum electrical field reaches critical value, the SJ structure certainly has higher breakdown voltage than conventional structure

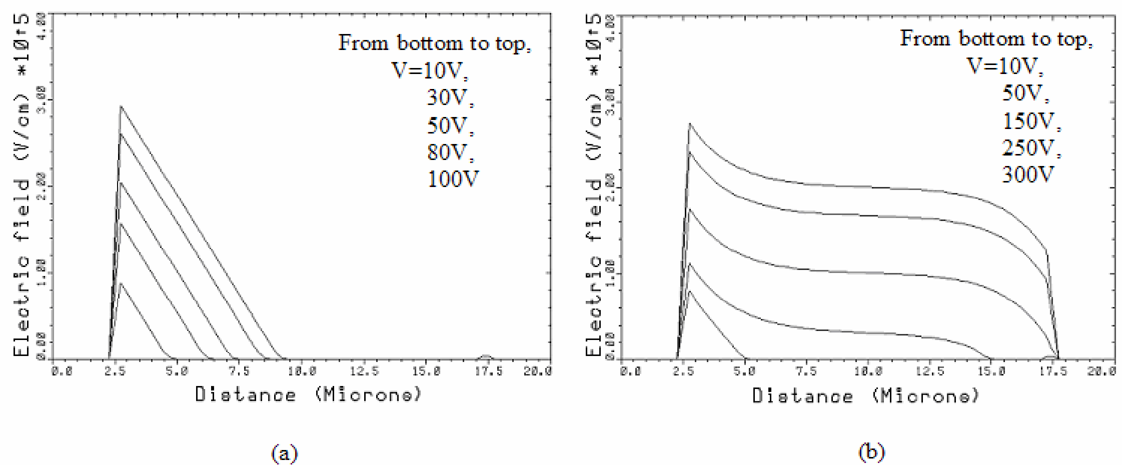


Fig. 2.5 Electrical field profiles in (a) conventional diode and (b) superjunction diode For the SJ diode, the field is plotted along the outer edge of n column

(b) Derivation of breakdown equation for SJ device

Since superjunction structure is two-dimensional (2-D) structure, 2-D Poisson equation should be solved to get the potential and electrical field equation. This has been done by several authors [24-27]. The solution of the y component of the electrical field E_y shows that it composes of two parts, one is a constant value E_0, the other is the E_1. E_0 is thought to be produced by the voltage applied and equal to that of a p^+-i-n^+ diode under the same reverse voltage. The equation of E_0 is given by:

$$E_0 = \frac{V_B}{L} \tag{2.13}$$

where V_B is the applied reverse voltage, L is the drift length.

The profile of E_1 is shown in Fig. 2.6. The maximum value of E_1 along the middle of n column is labeled as E_{1n}, along middle p column labeled as E_{1p}. E_1 is thought to be produced by the charge in the drift region. According to the charge compensation principle, most of the charge in p, n column is compensated by each other except some near charge the p+ and n+ contact. Therefore, E_1 is zero in most part of the drift region; only near p+, n+ contact there is peak value of E_1. Adding a constant value E_0 to the profile of E_1, the resulting profile E_y is very similar to the profile shown in Fig. 2.5(b).

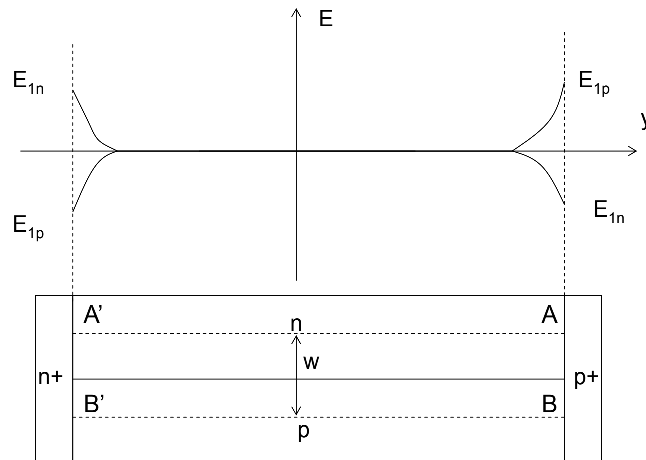


Fig. 2.6 Field profiles of E_1 along middle of n column (dash line) and along middle of p column (dash line)

It has been proved that the maximum electrical field appears at point A and B in Fig. 2.6, with the value of $E_0 + E_{1n}$ and $E_0 + E_{1p}$. The minimum electrical field appears at points A' and B' with the value of $E_0 - E_{1n}$ and $E_0 - E_{1p}$. Suppose the p, n column widths are equal, then $E_{1n} = E_{1p}$. The electrical field along the middle of n column is reproduced in Fig. 2.7 for the analysis of breakdown voltage. From Fig. 2.7, the optimum situation is that when breakdown occurs, the maximum electrical field $E_0 + E_{1n}$ reaches the critical electrical field, while the minimum electrical field $E_0 - E_{1n}$ is just zero. In other words, this condition means that when breakdown occurs, p, n column just fully depleted. At the optimum condition, E_0 and E_{1n} have the relationship: $E_0 = E_{1n} = E_C/2$, and breakdown voltage can be calculated by $E_0 \times L$ i.e. $\frac{E_C}{2} \times L$. The concentration satisfying this condition is the optimum concentration.

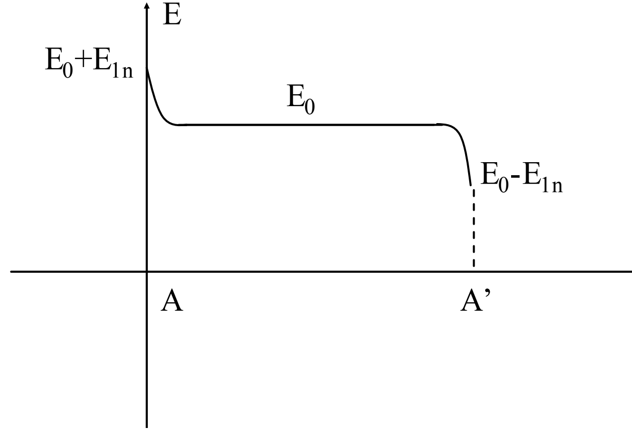


Fig. 2.7 Schematic electrical Field profile along middle of n column AA'

In the following, the maximum electrical field equation will be derived first to get the optimum concentration and breakdown voltage. For simplicity, the case that p, n column has same column width and same column concentration ($N_D = N_A = N$) is used in the derivation. Suppose before the fully depletion of p, n column, the electrical field only increases at the p+/n and n+/p junction. The lateral merge voltage $V_{\substack{lateral\\merge}}$ of p, n column is given by,

$$V_{\substack{lateral\\merge}} = \frac{qNw^2}{4\varepsilon_s} \tag{2.14}$$

At this voltage, the depletion depth in n column x_n is given by:

$$x_n = \left[\frac{2\varepsilon_s V_{\substack{lateral\\merge}} N_{p^+}}{q(N+N_{p^+})N}\right]^{1/2} \approx \frac{1}{\sqrt{2}}w$$

(2.15)

Then, the electrical field at p+/n junction before p, n column fully depletion E_A is arrived as:

$$E_A = x_n(\frac{qN}{\varepsilon_s}) = \frac{qN}{\sqrt{2}\varepsilon_s}w \qquad (2.16)$$

For the first order approximation, this field peak should be less than or equal to the critical electrical field, that is:

$$E_{\max} = E_A = E_C$$

(2.17)

where E_C is the critical electrical field, expressed as $Ec(N) = 4010N^{1/8}$.

Based on the expressions of E_A and E_C, the optimum column concentration is derived as:

$$N = 1.2 \times 10^{12} w^{-\frac{8}{7}} \qquad (2.18)$$

Equation (2.17) is obtained by substituting q=1.60218×10^{-19} C, ε_s=11.9×8.85×10^{-14} F/cm.

When the optimum concentration used in the SJ structure, the breakdown voltage can be expressed as following:

$$V_{BR} = E_0 \times L = \frac{E_C}{2} \times L = \frac{E_A}{2} \times L \qquad (2.19)$$

where L is the drift length.

Substituting equation (2.16) to (2.19), the breakdown voltage is expressed by device parameter:

$$V_{BR} = \frac{qN}{2\sqrt{2}\varepsilon_s}wL \qquad (2.20)$$

This equation is only applicable when the column concentration used is the optimum concentration. All the derived equations are first-order equations.

2.2.2 Specific on-resistance of SJ device

The relationship between $R_{on,sp}$ and V_{BR} for superjunction device is obtained by substituting equation (2.18) and (2.20) to the specific on-resistance definition equation (2.11):

$$R_{on,sp} = \frac{2 \times l_{drift}}{q\mu N} = \frac{2 \times \left(\frac{2\sqrt{2} \times \varepsilon_s \times V_{BR}}{qNw} \right)}{q\mu N} = \frac{4\sqrt{2} \times \varepsilon_s \times V_{BR}}{q^2 \mu N^2 w} = 0.107 w^{9/7} V_{BR}$$

(2.21)

where $R_{on,sp}$ is in unit of Ω-cm^2 ; w is in unit of cm; and V_{BR} is in unit of V.

Equation (2.21) is the ideal $R_{on,sp}$ vs V_{BR} relationship for superjunction devices. This is a linear relationship compared the more than square relationship for conventional device. To see clearly the superior performance of SJ device, the superjunction performance lines given by equation (2.21), together with the "ideal silicon limit" line expressed by equation (2.12), are shown in Fig 2.8. Fig. 2.8 shows that for breakdown voltage larger than 100V, superjunction devices have a lower specific resistance than the ideal silicon limit. This means that the silicon limit has been broken by the superjunction structure. The figure also shows that the higher breakdown voltage, the more prominent of the superjunction benefit.

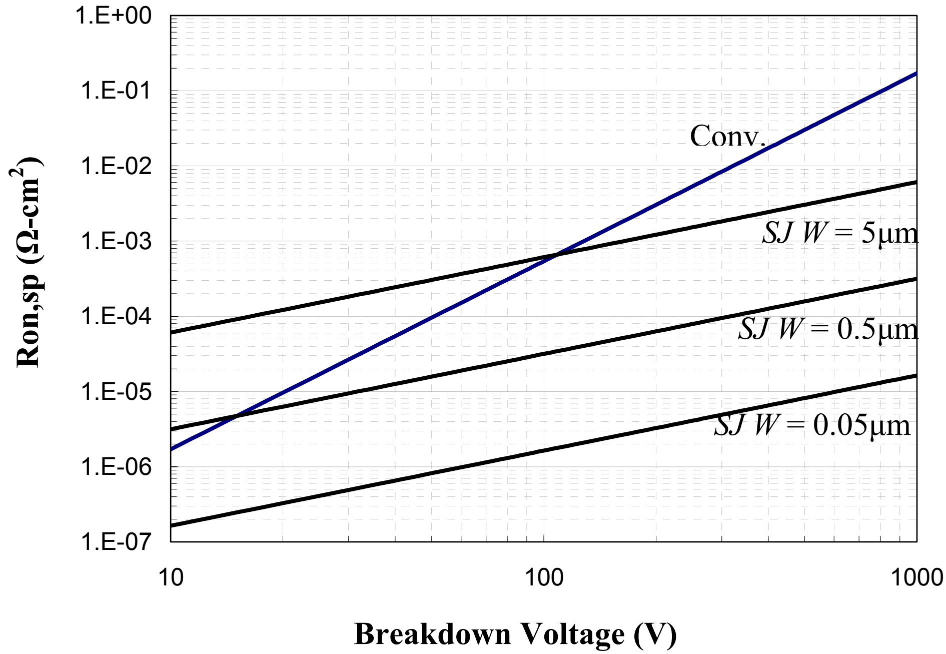


Fig. 2.8 Ideal $R_{on,\,sp}$ - V_{BR} performance comparison between conventional (CV) structure and superjunction(SJ) devices

2.3 Current state of superjunction device and technology

Superjunction concept is initially used in vertical devices. The reason is that the superiority of superjunction device is more prominent at high breakdown voltage and the whole wafer depth can be used to fabricate a vertical device to realize high breakdown voltage. While, for lateral device which is mainly used in medium or low breakdown voltage, it is not easy to achieve high breakdown voltage. Using superjunction structure in lateral device is still a new concept and the usage is limited at medium or low voltage range. Therefore, the fabrication technology of vertical SJ device is more mature than lateral SJ device. Till now, vertical SJ device has been made commercially available, while, lateral SJ device fabrication is still in research stage.

2.3.1 Vertical SJ devices

Most of fabricated SJ devices are vertical devices [9] [12-16]. There are many kinds of fabrication technology available which all have their pros and cons.

COOLMOS™ is the first commercially available superjunction device. The fabrication technology used is multiple deposition of epitaxial layers and subsequent implantation steps. This technology can achieve device performance of 3.5 Ω-mm^2@600V. The problem of the technology is that the resulted p, n column doping profile is not very satisfying. Along the drift region, p, n column shows radial profile due to limited number of epitaxial steps than can be employed. The interdiffusion between p, n column during driven-in process causes blur boundary between p, n column. Also the number of implantation masks needed to form p, n column profiles is a little large.

Compared with COOLMOS™ technology, Super Trench Power MOSFET (STM) uses trench etching and p, n tilt implantation to form p, n column doping profile. This technology only needs one additional mask over the conventional DMOS process [13, 14]. The device simulation results show it can achieve 5 mΩ-cm^2@ 300V. STM technology far surpasses conventional multi-epitaxy used in COOLMOS™ because it can realize very tight cell pitch, thus can achieve lower $R_{on,sp}$ [14].

Another similar fabrication technology is Vertical Deep Trench RESURF DMOS (VTR-DMOS) [15]. In this technology, a deep trench is etched to create vertical a sidewall, then highly doped p-poly is deposited along the sidewall to introduce solid boron source, finally boron diffuse into the sidewall to form p column. From

simulation results, VTR-DMOS shows a 5.5X improvement in $R_{on,sp}$ for breakdown voltage over 700V compared with conventional VDMOS.

A recent simple fabrication technology is Polysi Flanked VDMOS (PFVDMOS) [16]. This technology overcomes the interdiffusion problem between p, n column by introduce a thin layer oxide between them. The fabrication process is first growing n epi-layer, then etching it to leave space for p column. Next, dry oxidation is performed to form thin oxide layer. After removing the oxide on top and bottom part, a thin layer poly is deposited in the trench. To get uniform profile in p column, boron tilt implantation into the thin poly layer, poly refill and drive-in process are performed. This technology can produce rather uniform profile. In the p, n column formation process, only simple process steps such as etching, deposition, implantation and poly-fill are used.

2.3.2 Lateral SJ devices

Recently, SJ concept has been used in lateral MOSFET structure to improve it performance. Various structures have been proposed to achieve good performance [11] [17-22] [24, 28].

When lateral SJ structure was first proposed in 1998, it is called lateral 3-D RESURF device [11]. According to the author, the structure is based on the extension of RESURF concept to the third dimension. The lateral 3-D RESURF power MOSFET structure is shown in Fig. 2.9. After replacing conventional drift region to SJ structure, the breakdown voltage ability of the device has been greatly improved for the same

doping concentration due to the rectangular field distribution achieved by the SJ structure.

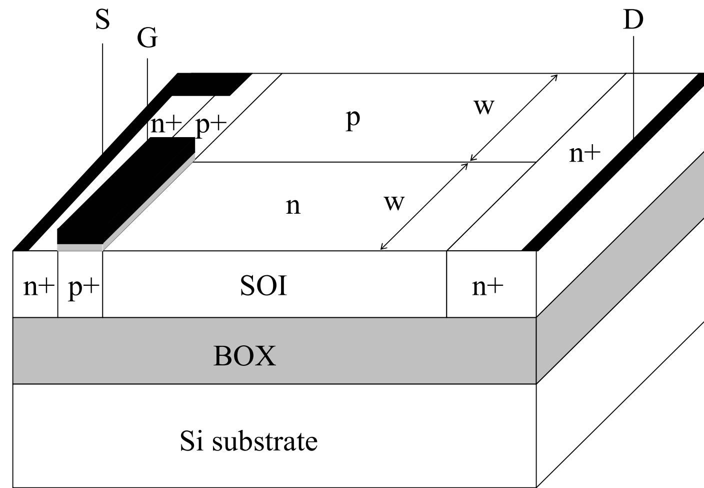


Fig. 2.9 The schematic view of lateral 3-D RESURF MOSFET

To further improve the specific on resistance, the same author proposed double gate structure [11]. Adding the second gate and p+ contact in the drain side, the p column can also be used to conduct current. Another variation of the structure is to use unbalanced SJ structure in drift region [17]. In the unbalanced structure, n column width eventually increases towards the drain end, while, p column width eventually decreases. This is to ensure that after p, n column fully depletion, the charge in n column will be greater than that in p column. Therefore, there is net charge increasing from source end to drain end. The net charge is similar to that produced by a linearly doping profile. This net charge is to counterbalance a layer of mobile charge on the surface of BOX, which is produced by field effect action across the SOI-BOX-substrate structure when a large reverse bias applied in the off-state. This mobile charge will affect the uniform distribution of the electrical field. After using the unbalanced SJ structure, the field distribution is very uniform and high breakdown

voltage can be achieved. To solve the same problem, another group proposed to use a different kind of substrate-sapphire [21]. The BOX and si-substrate in Fig. 2.9 are replaced by sapphire in the new structure. Without the SOI-BOX-substrate structure, the field effect action doesn't exist, so electrical field distribution is very uniform. Another benefit is that the sapphire has much better heat conduction ability than BOX-substrate structure.

The above devices are emphasis on the Off-state performance for high breakdown voltage. For medium level power applications, 120V interdigitated LDMOS (IDLDMOS) was proposed to have better performance than conventional LDMOS [18]. Device structure is similar to that in Fig. 2.9, with the only difference in channel formation process. The performance of the proposed structure can achieve 1.15 mΩ-cm^2 @124V, which is better than the performance of conventional LDMOS. A similar superjunction LDMOS structure was proposed to have breakdown voltage of 150V and specific on resistance 1.65 mΩ-cm^2[19]. The author emphasized on the fabrication aspect of the device. The fabrication steps, device layout design have been proposed and proved by the simulation.

The superjunction structure helps to increase the doping concentration of the n-drift layer, and lateral trench gate allows to increases channel area. If the two structures used in the same device, both the drift region resistance and channel resistance can be reduced. The structure is called lateral trench gate superjunction SOI-LDMOSFETs [20]. The device is aimed at breakdown voltage 120V and the specific resistance can be reduced to 60% of conventional SOI-LDMOSFETs.

Although superjunction LDMOS has been proved theoretically to have better performance than conventional LDMOS, the fabrication technology still needs to be

developed. Till now, only few structures are fabricated [22][28]. One fabricated device is on bulk silicon wafer [22]. First, n-drift region is formed by implanting high dose phosphorus to the lightly doped p-type substrate. Then, p-strip mask was patterned and the boron ions were implanted to form the p-strip region. The dosage used to form p-strip are several times higher than n-drift. The fabricated SJ-RESURF LDMOSFET has a performance of 3.53 Ω-mm^2 @ 335V.The on-resistance is 25% better than that of conventional structure. The other fabricated SJ LDMOS is on sapphire substrate using the 0.5µm CMOS/SOS technology [28]. The process includes three pairs of complementary LDD-CMOS transistors. Lateral isolation between devices is implemented using recessed LOCOS that extends down to sapphire substrate. The superjunction drift region is implemented by stacking alternating n and p-pillars made of layers corresponding to the channel regions of, respectively, PMOS and NMOS devices. The experimental breakdown voltage is 170V with the lateral electrical field of 17V/µm, which implies charge compensation. 3-D simulations predict silicon limit of conventional LDMOS can be broken when the aspect ratio of pillar height to width exceeds 1.2 µm /0.3µm.

2.4 Summary

In this chapter, the performance of conventional power MOSFET device is firstly analyzed with the emphasis on “silicon limit”. Then, the superjunction device is investigated in detail. The off-state performance of superjunction device is compared with that the conventional device to show its superiority. The off-state and on-state equations are derived based on electrical field analysis. Finally, the current status of superjunction device is reviewed, and problems encountered are summarized.

Chapter 3

Practical SJ performance under interdiffusion influence

Chapter 2 has summarized the current state of superjunction device and technology. Although superjunction device and technology have developed for many years, there are still some constrains existing in device structure or fabrication technology. Interdiffussion problem is one of the technology constrains. In this chapter, the interdiffusion problem is discussed and the study of practical superjunction device performance under given thermal cycles with the major consideration of interdiffusion is described.

3.1 Interdiffusion problem in current technology

Till now, most of the fabricated SJ devices are vertical devices. Few lateral SJ devices are fabricated. The available fabrication technologies for vertical SJ devices are

COOLMOS™ technology, STM, VTR-DMOS and PFVDMOS [9][12-16]. These technologies have been introduced in section 2.3.1 of chapter 2. Each technology has its own pros and cons.

To achieve the best performance in superjunction structure, precisely charge-balanced p and n voltage-sustaining columns must be formed to have exactly the same doping concentration and the same column width. However, to achieve ideal matching condition in practice is rather difficult, if not impossible. In addition, even if the doping of both p-n columns could be made equal, the quality of sidewall junction formed by the neighbouring p-n columns plays another important role to influence the breakdown voltage. This constraint becomes more dominant when p- and n-column widths get smaller for devices rated in lower voltage region, e.g. below 200 V. For a column width less than 3 μm, the approach of using multiple-layer epitaxial growth and implantation process [9] to form vertical p-n columns becomes unsuitable due to the constraints of multiple misalignments of masks, auto-doping in the epitaxial process and thermally-induced dopant inter-diffusion in annealing processes. Instead, the silicon trench and selective epitaxial growth processes can be used at a lower temperature to overcome the above-mentioned constraints [29-31].

However, other follow-on fabrication processes involving thermal cycles for MOSFET gate and source formation are always needed. These high temperature thermal cycles promote dopant inter-diffusion between non-ideal p-n columns and give rise to the formation of a wider dopant transition region between p-n columns, resulting in more non-uniform dopant distribution. The sidewall junction quality is thus worsened, and in turn, this lowers the achievable breakdown voltage of superjunction devices having narrow column width.

The dopant interdiffusion phenomenon is unavoidable in most of the fabrication technology such as COOLMOS™ technology, STM, VTR-DMOS. The PFVDMOS technology forms a thin oxide layer between p, n column to prevent the interdiffusion. The technology achieves the expected result. However, the interdiffusion influence on the SJ device performance is still needed to discover.

As part of the research work, the practical SJ performance under given process thermal cycles is investigated. When the process thermal cycles are fixed, the amount of interdiffusion caused by thermal cycles is fixed. The aim of the study is to find the influence of interdiffusion on the SJ device performance.

3.2 Practical SJ performance under given thermal cycles

3.2.1 Simulation methodology

To get the realistic SJ performance under given process thermal cycles, two vertical SJ MOSFET structure, DMOS and UMOS, are the used in the simulation. The schematic view of DMOS and UMOS structures are shown in Fig. 3.1 (a) and (b).

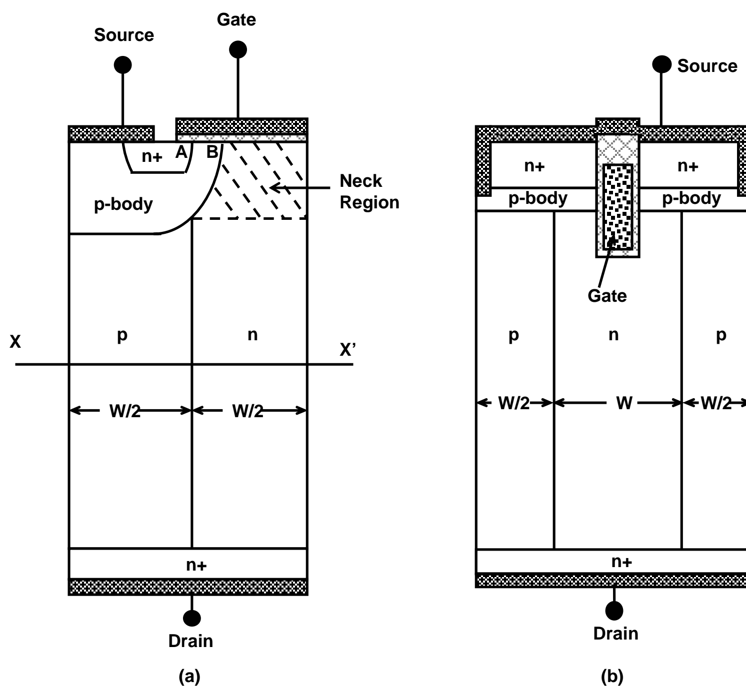


Fig. 3.1 The two vertical Superjunction power MOSFET structures
(a) SJ DMOS structure (b) SJ UMOS structure

The conducting n-column is set initially to have equal doping and width as the non-conducting p-column at the selective epitaxy growth stage then followed by all device thermal processes in order to find the optimum SJ device performance in practice. In process simulation, a silicon wafer of n-epitaxial layer grown on n^+ substrate is used. A trench is etched and p-column is grown by low-temperature (<550° C) selective epitaxy. The epitaxial layer now containing interdigitated p- and n-columns is further processed to form p-body, gate and source regions so as to complete the MOSFET structure. P-body and source regions are self-aligned to the gate edge to ensure fixed channel length for structural consistency for all cases in the investigation. The channel length is fixed at 0.3 μm. The right edge of source region, i.e. point A, is always aligned with the junction of p-n columns. The distance between p-body right edge, i.e. point B, and the p-n column junction is maintained at a reasonable distance, so that the neck region in DMOS structure will not be too small. The device geometries are summarised as following. The minimum source length is 0.5 μm, of which the overlap with gate oxide region is 0.1 μm. The column width varies from minimum of 1.3 μm to 9 μm at 0.1 μm step. No obvious degradation on breakdown voltage by the inter-column dopant diffusion in SJ structure was observed when the width is more than 9 μm in the simulated breakdown voltage range from 80V to 1000V. The neck length for DMOS is equal to half of the column width minus the channel length, i.e. it varies from 0.35 μm to 4.2 μm.

The epitaxial thickness is adjusted to the minimum for each specific breakdown voltage so that smallest achievable $R_{on,sp}$ is achieved. All essential thermal cycles such as gate oxide growth, n^+ source-drain anneals and p-body drive-in are included in TSUPREM [39] process simulation. The main thermal processes in MOSFET device

fabrication are listed in Table 3.1. The thermal budget shown in Table 3.1 is taken from previously optimized fabrication conditions in the run sheet, which is intended for a high voltage device. Compared with the thermal process in Table 3.1, the interdiffusion caused by p column epitaxy process can be neglected because the growth temperature is below 550° C.

To find the realistic and optimum SJ performance curve, the approach is to find the minimum $R_{on,sp}$ at various column width, doping concentration and drift length at each breakdown voltage. The simulation process was carried out in three nested loops, i.e. to determine these three optimal parameters at a particular breakdown voltage. A flow chart is given in Fig. 3.2 to illustrate the simulation methodology.

For each breakdown voltage, the column width (W) is set at the maximum value and the initial concentration (N) is set at 30% of the theoretical value of $N = 1.2 \times 10^{12} \times W^{-8/7}$ to start with the iterations. The drift region depth is set initially at a value by assuming uniform field of 10 V/µm over the drift length. The structure formed by the process simulation (TSUPREM) is imported into device simulation (MEDICI) [40] to simulate device performance. The iterations are to find the locally-optimal doping concentration first at each column width, and for all different column widths to determine the globally-optimal column width and doping concentration to yield the minimum $R_{on,sp}$ for a

Thermal process	Time (min)	Temperature (degree Celsius)
Gate oxide growth	76	1000
P-body driven-in	20	1100
Source/drain anneal	30	900

given breakdown voltage. For example, consider the case of column width W = 1.7 μm for device breakdown rating of 300 V. The calculated optimal concentration based on the ideal SJ theory for W = 1.7 μm is 2.44×10^{16} cm^{-3}. In practice, the optimal concentration is likely to be lower; hence, we start from the concentration of 8×10^{15} cm^{-3} (30% of ideal value). The concentration is gradually increased while the width W is fixed.

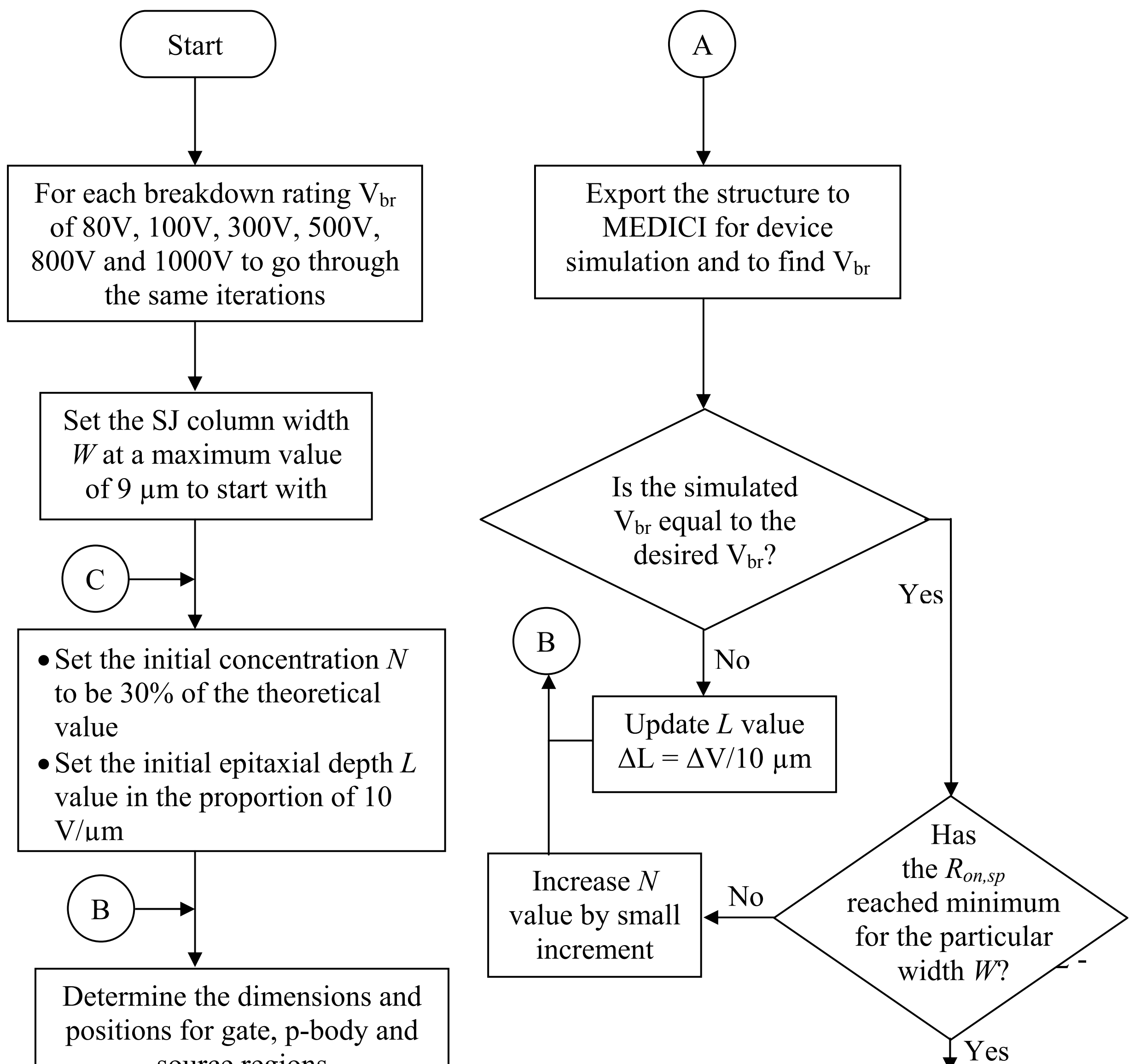


Fig. 3.2 Flow chart of simulation methodology

For each concentration, the drift length to sustain the expected breakdown voltage, i.e. 300 V, is adjusted accordingly. Then, the $R_{on,sp}$ is found with that concentration and epitaxial thickness. *W* is decided firstly because the initial value of *N* can be calculated based on it. *L* is decided finally because *W* and *N* have small influence on it. As can be seen in Fig. 3.3, under realistic process conditions, the increase in the doping concentration enables a lower $R_{on,sp}$ and the performance point moves towards the point Q where the optimal value is reached. This occurs at the concentration of 1.3×10^{16} cm^{-3}, a value below the theoretically calculated one mainly due to influence of dopant inter-diffusion. During thermal process, the substrate dopant may also out-diffuse into the epitaxial drift region. The out-diffusion phenomenon has been considered and included in the drift length adjustment, so that the drift length after thermal process is at the correct quantity to sustain the target voltage, i.e. 300 V in the current example.

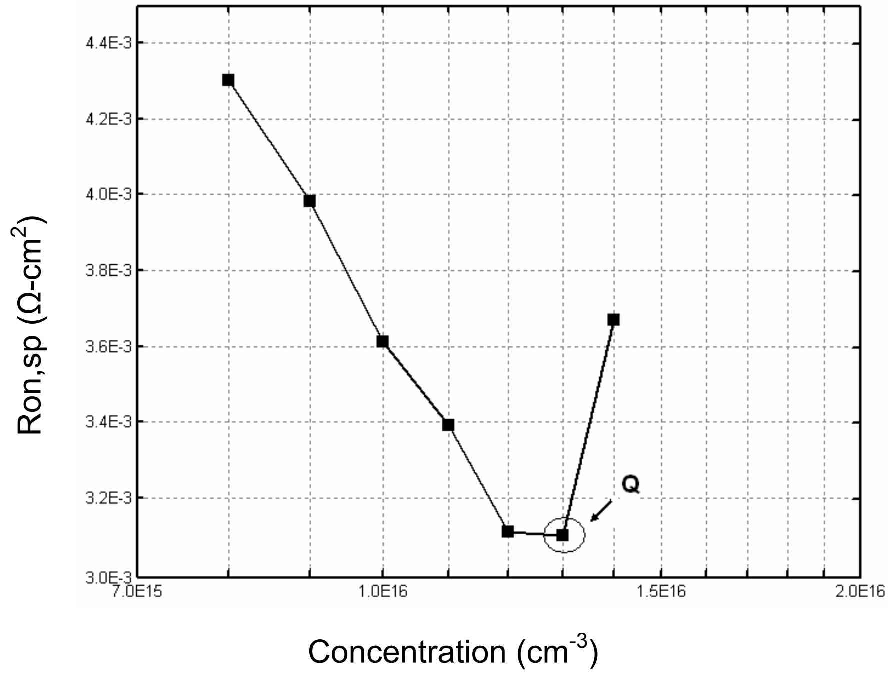


Fig. 3.3 The relationship between $R_{on,sp}$ and column doping concentration at the given breakdown voltage (300V) and column width (1.7μm). The optimum concentration for column width of 1.7 μm is 1.3×10^{16} cm^{-3}

For each column width, the optimal concentration and $R_{on,sp}$ to achieve a specific breakdown voltage can be found using the methodology described above. By observing $R_{on,sp}$ varying with changing W, the globally-optimal $R_{on,sp}$ can be found for a given breakdown voltage. For the breakdown voltage of 300 V, the $R_{on,sp}$ versus W curve is shown in Fig. 3.4. The optimal $R_{on,sp}$ at 300 V rating is 2.24×10^{-3} Ω-cm^2 at the column width of 2.3 μm. Hence, by following the same approach, it is now possible to find the globally-optimal $R_{on,sp}$ for each breakdown voltage. This has been done for breakdown voltages of 80 V, 100 V, 200 V, 300 V, 500 V, 800 V and 1000 V respectively.

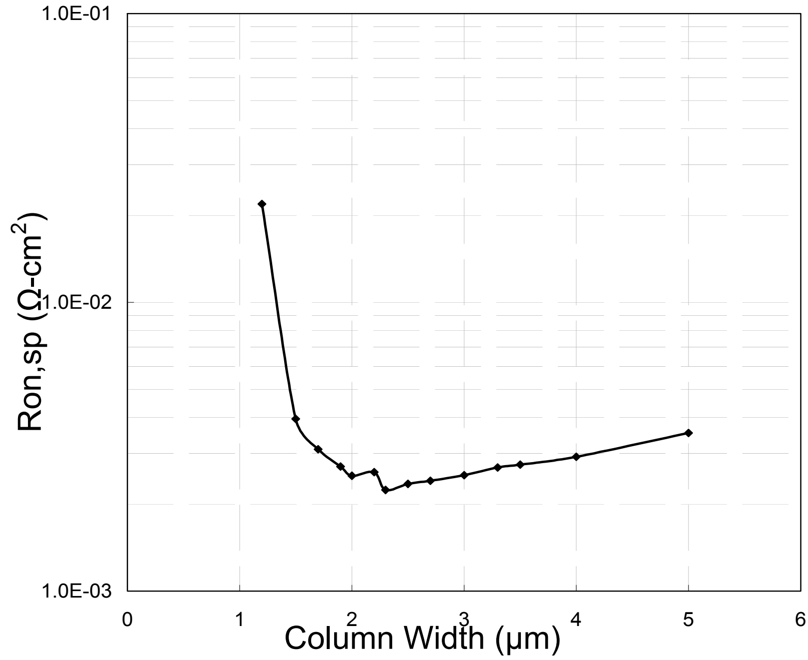


Fig. 3.4 The relationship between $R_{on,sp}$ and the column width at given breakdown voltage (300V). The optimal $R_{on,sp}$ at 300V is 2.24×10^{-3} Ω-cm^2 at column width W = 2.3 μm

3.2.2 The realistic optimum SJ performance curves

The realistic optimal SJ performance curves under inter-column diffusion influence for both DMOS and UMOS of minimum $R_{on,sp}$ versus V_{br} are shown in Fig. 3.5, together with the ideal silicon limit lines of conventional structure [1, 2] and ideal SJ performance lines for different column width W [2] and different Δ/L [32] where Δ is the hexagonal column width and L is the drift region depth as defined in [32]. Experimental data extracted from published work [4, 9, 13-15] are also labelled in Fig. 3.5. It is clearly shown that all the experimental data have a higher specific resistance above the realistic optimal SJ performance curves. With dopant inter-diffusion

included in practical process, the realistic optimal SJ performance curves are not linear in the log-log plane as ideal SJ performance lines. Compared with the ideal silicon limit line, when the breakdown voltage is below 80 V, the realistic $R_{on,sp}$ of SJ structure is worse than that of the ideal unipolar silicon limit.

3.2.3 The interdiffusion influence on breakdown voltage

To understand why the practical SJ curves become like this, the interdiffusion influence on breakdown voltage is studied.

To show the transition between ideal and realistic situation, the doping profiles changing from ideal case without thermal budget to the realistic case with full thermal budget are shown in Fig. 3.6. The simulated device is SJ VDMOS with column width of 2μm and ideal concentration of 2.03×10^{16} /cm^3. The doping profiles are cut along line X-X' as in Fig. 3.1(a). The dopant inter-diffusion creates a wider dopant transition region at p-n junction and it also alters the junction position away from its origin metallurgical position of equal p and n column widths.

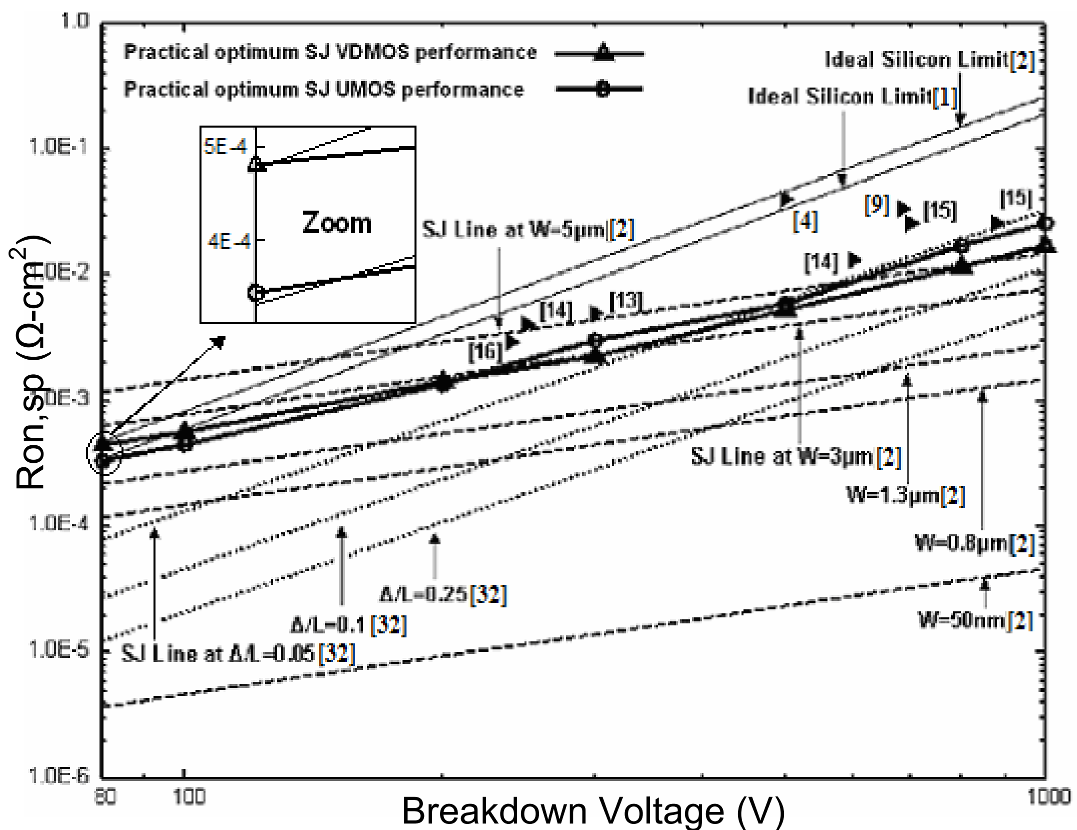


Fig. 3.5 The simulated practical optimum SJ performance curves (SJ DMOS and SJ UMOS) with dopant inter-diffusion included compared with the ideal SJ performance lines and the ideal silicon limit curves. A "zoom in" figure is added to show clearly the curves near 80V

By cutting the line along X-X', as shown in Fig. 3.1(a), perpendicular to the current flow, and integrating the doping concentration in p-column and n-column respectively, the difference between p-column doping integral Q_p and n-column doping integral Q_n can be found and is defined as one-dimensional (1-D) p-n doping integral imbalance. The two-dimensional (2-D) p-n doping imbalance is obtained by numerically integrating the 1-D p-n imbalance along the entire length of SJ column in the drift region. The results show that, for higher column concentration the imbalance of doping integral is more severe for a given thermal cycle. In turn, the sustainable voltage becomes lower. Hence, the column concentration is reduced in order to maintain the sustainable breakdown voltage.

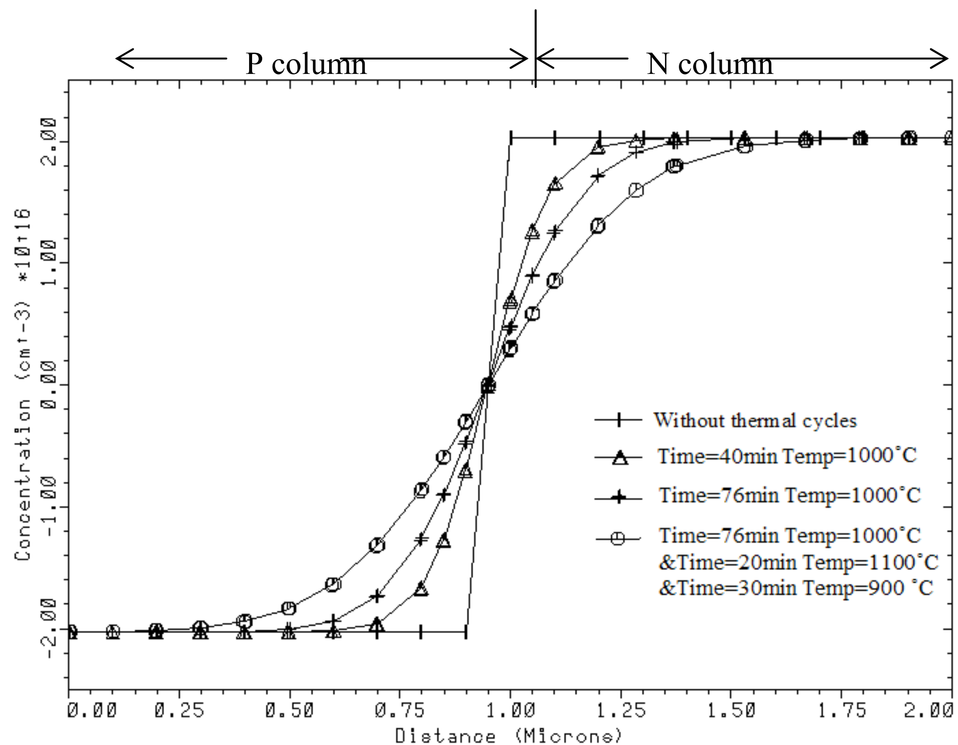


Fig. 3.6 The doping profiles changing from ideal case without thermal budget to the real case with full thermal budget. The thermal budgets for each doping profile are labelled in the figure. The simulated device is SJ VDMOS with column width of 2μm and ideal concentration of 2.03×10^{16} /cm^3. The doping profiles are cut along line X-X' in Fig. 3.1(a)

The realistic relationships between the optimal concentration and column width for breakdown voltages of 300 V, 500 V and 1000 V, together with theoretical concentration curve, are shown in Fig. 3.7. All three practical curves follow the same trend and deviate from the ideal curve when column width becomes small. To get an impression how much the realistic profile departs from ideal profile, the ideal profile without interdiffusion and the profile with ideal concentration and interdiffusion are compared to the realistic profile shown in Fig. 3.8. The three profiles are cut along line X-X' in Fig. 3.1(a). The data used in Fig. 3.8 are the ideal concentration (2.03×10^{16} /cm^3) and practical concentration (1.4×10^{16} /cm^3) for 300V device with the column width of 2μm, which can be found from Fig. 3.7. The breakdown voltages for the two cases with interdiffusion are also labeled.

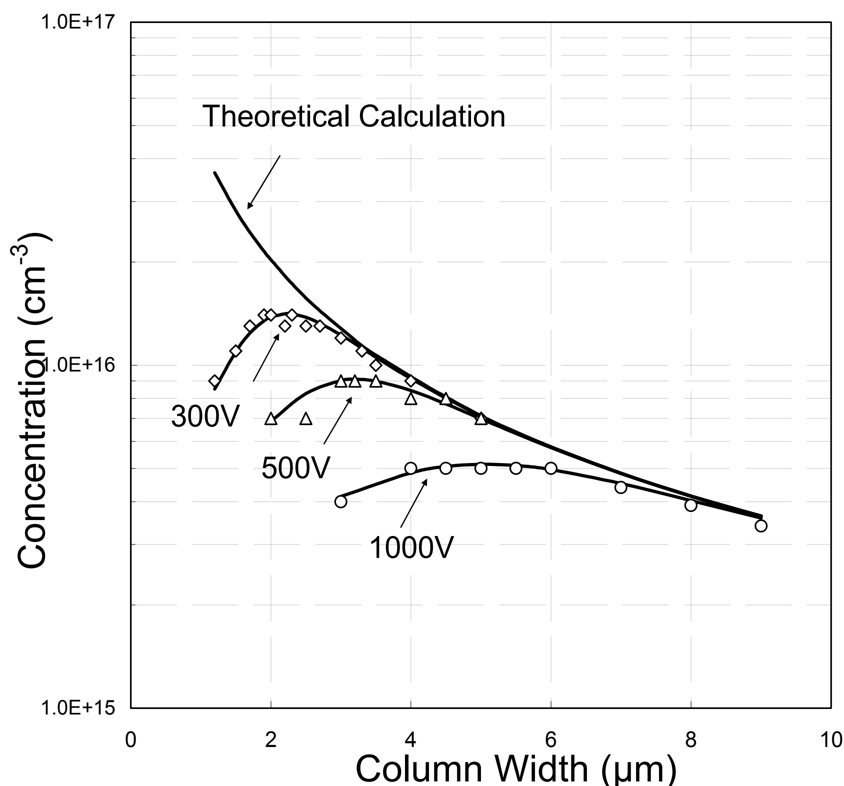


Fig. 3.7 The relationships between the simulated optimal concentration and column width at 300 V, 500 V and 1000 V along with and the ideal concentration curve which is calculated using equation $N = 1.2 \times 10^{12} \times W^{-8/7}$ are shown. For each breakdown voltage, the void markers represent the simulated data and the solid lines are the fitting curves calculated using the empirical equation (3.1)

To illustrate the phenomenon caused by doping integral imbalance, Fig. 3.9 shows the potential contours and depletion boundaries of two similar structures at breakdown. They have the same column width of 1.5 μm and epitaxial depth of 22 μm but with only the column dopant concentrations are different. The concentration in the structure of Fig. 3.9(a) is at the SJ theoretical value of 2.82×10^{16} /cm^3. The best acceptable concentration of 1.1×10^{16} /cm^3 under practical conditions is used in the second structure of Fig. 3.9(b). Simulated results indicate the breakdown voltages of 149.5 V for Structure 3.9(a) and 301.1 V for Structure 3.9(b).

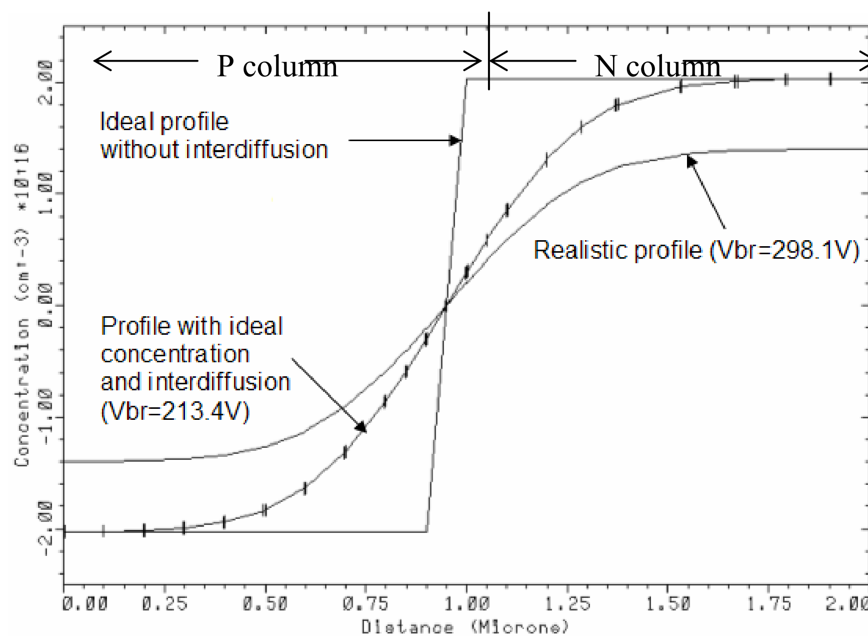


Fig. 3.8 The ideal profile without interdiffusion and the profile with ideal concentration and interdiffusion are compared to the realistic profile. The three profiles are cut along line X-X' in Fig. 3.1(a). The data used are the ideal concentration (2.03×10^{16} /cm^3) and practical concentration (1.4×10^{16} /cm^3) for 300V device with the column width of 2μm, which can be found from Fig. 3.7. The breakdown voltages for the two cases with interdiffusion are also labeled.

By observing the depletion boundaries (dash lines) in both structures, the lower breakdown is due to incomplete depletion of n-column. In Fig. 3.9(a), the n-column is not fully depleted at breakdown indicting that the SJ field action did not occur effectively. To study the relationship between p-n doping integral imbalance and incomplete column depletion, the depletion status of n-column, while p-column is just fully depleted, was investigated. The un-depleted n-column region is identified by depletion boundary given by simulation program MEDICI. The region is divided by the simulation mesh to small elements. By doing finite-element integration of doping manually, we can get the doing integration in the region. It was confirmed that the doping integral in the un-depleted n-column region is approximately equal to the 2-D p-n doping integral imbalance.

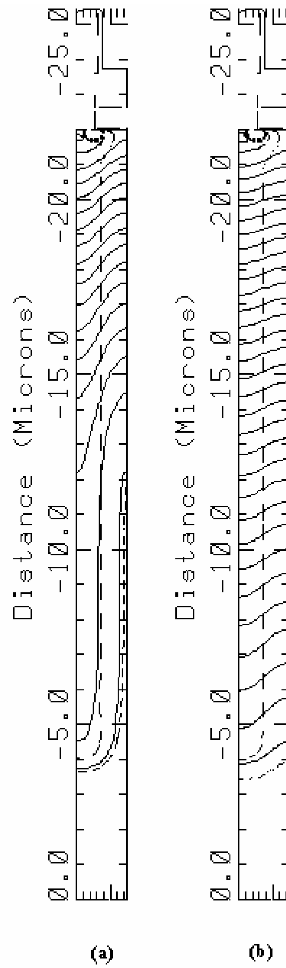
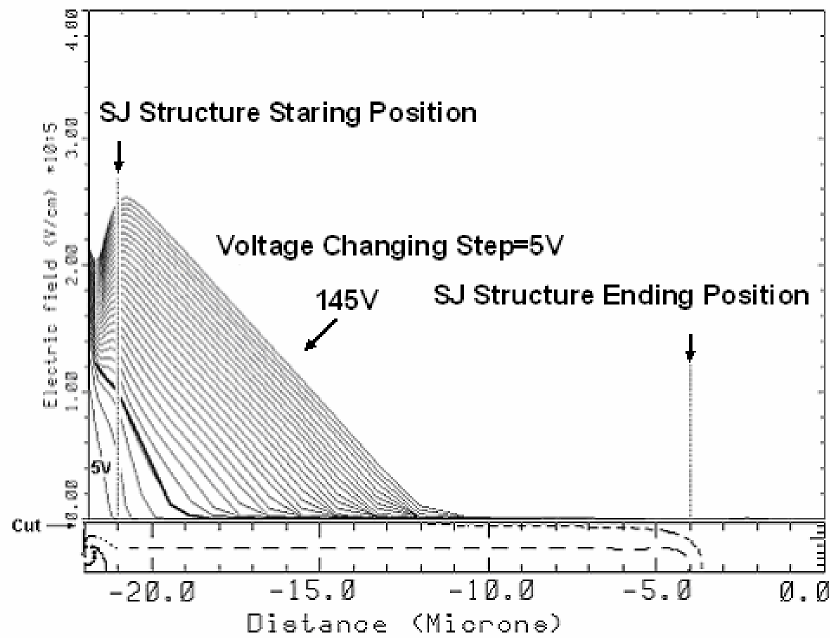
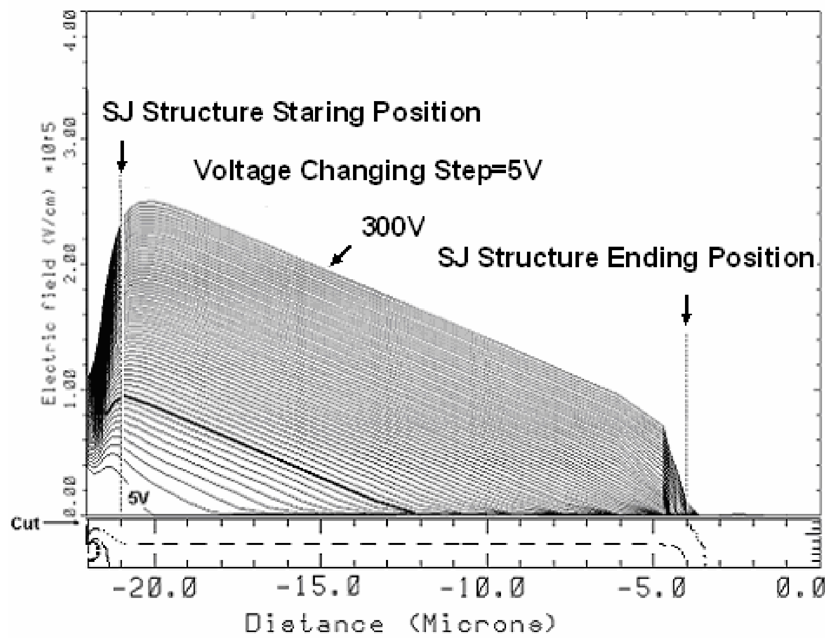


Fig. 3.9 For both structures, the solid lines are the potential contours and the dash lines are the depletion boundaries. Both structures have the same column width of 1.5 µm and epitaxial depth 22µm, only the column concentrations are different, namely (a) the theoretical concentration of $2.82 \times 10^{16}/cm^3$ with a breakdown voltage of 149.53V, and (b) the optimal concentration of $1.1 \times 10^{16}/cm^3$ with a breakdown voltage of 301.06V.

The influence of p-n doping integral imbalance can also be observed in the slope of electrical field (E-field) profiles. The E-field profiles in Fig. 3.10(a) and (b) are corresponding to the structures of Fig. 3.9(a) and (b). The E-field profiles are plotted along the cut at the centre of n-column along the drift region. The applied reverse voltage varies from 5 V to the respective breakdown voltages in a step of 5 V.



(a)



(b)

Fig. 3.10 The electric field profiles within n-column in (a) and (b) are corresponding to the structures in Fig. 3.7 (a) and (b). The cuts are at the centre of n-column with the applied blocking voltage changing in a step of 5V to the respective breakdown voltages. The E-field profile at which the p-column has just been fully depleted is marked by a darker line.

The particular E-field profile at the voltage while p-column is just fully depleted is marked with a darker line. The triangle-like shape of the E-field in Fig. 3.10(a)

indicates incomplete depletion of n-column caused by doping integral imbalance. The slope of E-field profile maintains approximately at the same value after p-column is fully depleted. Knowing the critical E-field is similar when column concentration varies in a limited range, the slope of E-field profile after p-column is fully depleted can be used as an index for breakdown voltage. The lower E-field slope indicates a better depletion of n-column and as a consequence higher breakdown voltage.

Simulation results indicate that the slope of the E-field profile is approximately proportional to the 2-D p-n doping integral imbalance at fixed column width. Fig. 3.11 shows the relationship between 2-D doping integral imbalance and the E-field slopes at 1.5 μm at different concentrations. 2-D doping integral imbalance is obtained by 1-D doping integral imbalance multiplied by drift length assuming 1-D doping integral

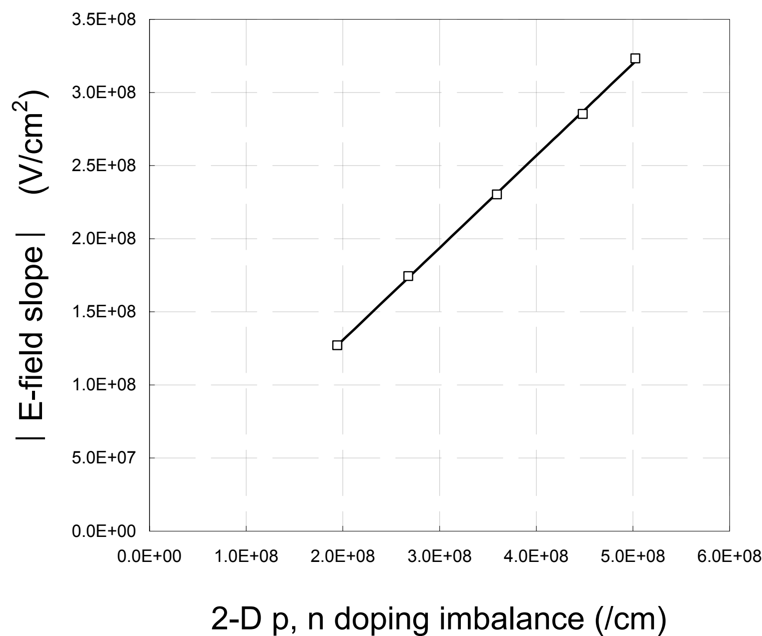


Fig. 3.11 The relationship between 2-D p-n doping integral imbalance and the E-field slopes

imbalance is constant along the drift region. 1-D doping integral imbalance is the difference between p column doping integral Q_p and n-column doping integral Q_n . Q_p and Q_n can be simulated by TSUPREM4.

With the above observations, the three realistic curves in Fig. 3.7 can be better explained. Take the 300 V curve as an example, at a critical E-field, the prospective slope of the E-field at breakdown can be identified at a certain value. At the same time, the actual E-field slope is known to be proportional to the 2-D p-n doping integral imbalance at a fixed column width. When the theoretical concentration corresponding to a smaller column width gets higher, the imbalance becomes worse. When the imbalance gets larger, the E-field slope gets steeper. To maintain the E-field slope for a specific breakdown voltage, the doping concentration needs to be reduced to lower the imbalance in order to maintain the full depletion in p-n columns.

3.2.4 Practical concentration equation

Fig. 3.7 shows the practical concentration deviates from theoretical concentration only when column width is small. As the column width increases, the practical concentration curve merges with the theoretical curve. The merger of the two curves shows that as column concentration decreases to a certain value and column width is large enough, the doping integral imbalance caused by inter-diffusion becomes unimportant and plays no role. The merger point of the practical curve and theoretical curve is dependent on the breakdown voltage rating. As the rating becomes higher, the merger point occurs at larger column width, i.e. lower concentration. Higher breakdown voltage corresponds to longer drift region depth, which will make 2-D doping integral imbalance higher. Hence, column concentration needs to be reduced in order to keep the 2-D doping integral imbalance low. The merger point can be empirically identified by the product of the breakdown voltage rating and the theoretical concentration. The product has a constant value of approximately 4×10^{18} V/cm^3 for ratings between 300V and 1000V as observed from the simulation results of a given thermal processes. It is recommended that this product is used to identify

the merger point on concentration-column width graph at a given breakdown voltage. The concentration in columns is lower than the one predicted by theoretical equation once the column width falls bellow that of the merger point. Hence a simple method to gauge onset of deviation from ideal concentration at different column width is possible. A simple empirical equation to fit all the curves in Fig. 3.7 was found. In this equation, realistic doping concentration *N* for a given breakdown rating based on actual given process is

$$N \approx \frac{1.2\times10^{12}\times W^{-\frac{8}{7}}}{1+\frac{3}{V_{br}^{\ 0.7}}\exp\left[-\frac{7(W-W_m)}{W_m}\right]} \tag{3.1}$$

where W_m is found from $1.2\times10^{12}\times W_m^{-\frac{8}{7}}\times V_{br}=4\times10^{18}$ as indicated earlier. The numerator of the equation (3.1) is the expression of theoretical concentration, and the denominator is introduced due to the inter-diffusion influence.

This proposed equation can be used to predict the behaviour of practical concentration for given thermal cycle in processing. Simulation has been done to test the sensitivity of the equation to particular thermal budget. The targeted breakdown voltage is 300V. To vary thermal budget, a drive-in process is followed after p-n column formation. The diffusion temperature is chosen at 1100˚C, as that in p-body drive-in. The diffusion times are chosen at 20min, 70min and 120min. The simulation shows that, for column width lower than 2μm, the practical optimum concentration doesn't change with different thermal cycles. For other column widths, the practical optimum concentration increases slightly as the diffusion time increases. For the extreme long diffusion time of 120min, the biggest increase is 7.69% of original value. This indicates that the practical optimum concentration *N* is only sensitive for lower thermal budget, where it actually improves. The coefficients in equation (3.1) are

clearly insensitive if thermal budget is increased. The equation applies to practical curves of V_{br} ratings from 300V to 1000V so that practical concentration and column width within this breakdown voltage range can be easily identified.

This equation is also useful in device design under known thermal cycles. For example, if a 400V breakdown rating power MOSFET device is required to have $R_{on,sp}$ as small as possible, the practical optimum concentration at different column width to sustain the breakdown voltage can be calculated from equation (3.1). Through which, a set of column widths is chosen and the corresponding column concentrations are calculated at these column widths to find the most suitable ones with lowest on-state resistance. The chosen column widths are 1.5μm, 2μm, 2.5μm, 3.5μm, 4μm and 4.5μm. The calculated practical column concentrations and theoretical column concentrations are listed in table 3.2. From Table 3.2, the optimum column width is found to be 2.5μm with concentration of 1.09×10^{16} /cm^3. Table 3.2 also shows that for column width larger than 3.7 μm, which is at the merger point (W_m) for 400V rating, the practical concentration and theoretical concentration are approximately equal. The drift region depth can be approximately estimated by the equation derived in Appendix A. The drift region depth is set to be 27μm for 400V devices by equation (A.5).

Table 3.2: The calculated practical concentration and the theoretical concentration for device breakdown rating of 400V

Column width(μm)	Practical conc.($/cm^3$)	Theoretical conc.($/cm^3$)
1.5	7.22E+15	2.81E+16
2	9.51E+15	2.02E+16
2.5	1.09E+16	1.57E+16
3	1.08E+16	1.27E+16
3.5	1.00E+16	1.07E+16
4	8.94E+15	9.17E+15
4.5	7.94E+15	8.02E+15

Two groups of devices were simulated with given thermal cycles. The two groups have the same drift region depth of 27μm, the column widths and concentration data obtained from Table 3.2. One group uses practical concentration and the other group uses theoretical concentration. After the same thermal cycles given by Table 3.1, the simulation results are shown in Fig. 3.12. Fig. 3.12 shows that breakdown voltages for the group with practical concentrations are always above 400V. While, the breakdown voltages for the other group increase as column width increases. When the column width is larger than W_m , the breakdown voltages can be over 400V. Fig. 3.12 has in effect proven the suitability and usefulness of equation (3.1). After the satisfaction of the breakdown voltage requirement, the minimum $R_{on,sp}$ requirement is met by choosing the device with the highest practical column concentration.

3.2.5 Practical SJ performance equation

Based on the practical concentration equation given in equation (3.1), the practical SJ performance equation is derived. The specific on-resistance of the drift region is given by

$$R_{on,sp} = \frac{l_{drift}}{q\mu(N/2)} \tag{3.2}$$

Equation (3.2) gives the drift region resistance of the SJ device. Due to the existence of neck region in SJ VDMOS, the mismatch between the simulated resistance and

derived one is visible. On the other hand, there is no neck region in SJ UMOS; the derived resistance is close to the simulated one.

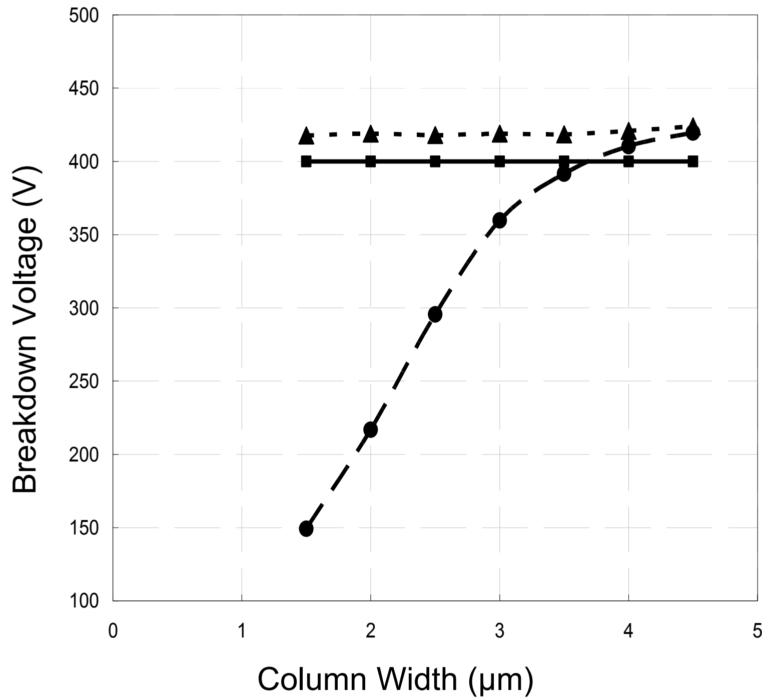


Fig. 3.12 The relationships between breakdown voltage and column widths for two groups of devices. The two groups have the same drift region length of 27μm and the same set of column widths. One group use the theoretical concentration, whose breakdown voltages are shown by dash lines and circles. The other group use the practical concentration, whose breakdown voltages are shown in dotted line and triangles. The expected breakdown voltages are shown in solid line and rectangles.

Substituting equations (3.2), (A.5) and constant values to above equation, equation (3.2) becomes

$$R_{on,sp} \approx 1.8\times 10^{-2} W^{8/7}\left\{1+\frac{3}{V_{br}^{\ 0.7}}\exp\left[-\frac{7(W-W_m)}{W_m}\right]\right\}V_{br}^{\ 7/6} \tag{3.3}$$

where $R_{on,sp}$ is in unit of Ω-cm^2; W in unit of cm; and V_{br} in unit of V.

Using equation (3.3), the practical SJ performance curves in the breakdown range of 300V-1000V for different column widths are plotted in Fig. 3.13. It shows that the cross-point of two curves corresponds to the situation that two different column widths have the same practical concentration for a certain breakdown voltage, which

is also shown in Fig.8. These curves show that the $R_{on,sp}$ doesn't necessarily decrease with a smaller column width in practical situation. There exists an optimum column width for each breakdown voltage. The column width corresponding to the lowest on-state specific resistance for a breakdown rating from the practical superjunction curves is the optimum column width. This qualitatively establishes that without appropriate charge compensation measure, such as precise corrective implantation, the SJ device performance will be strongly influenced by thermal cycles, especially at small column widths.

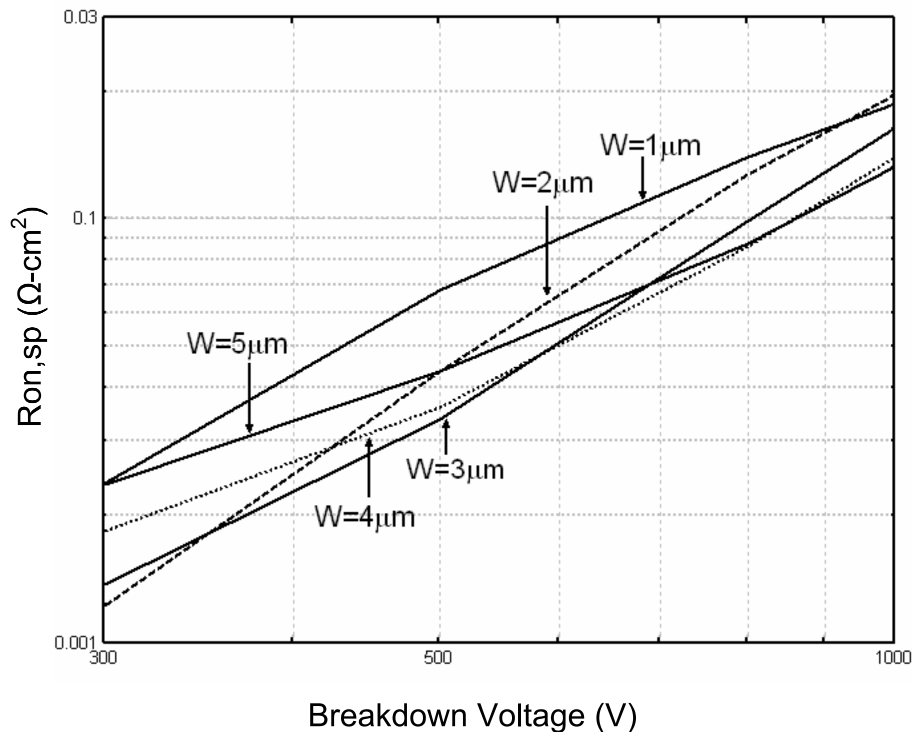


Fig. 3.13 Practical SJ performance curves under the thermal cycles given by table 3.1 at fixed column widths 1μm, 3μm and 5μm

3.3 Summary

In this chapter, the interdiffusion problem in current technology is discussed firstly. Then, the study of the interdiffusion influence on practical superjunction device

performance is discussed in detail. Through extensive simulation, the practical performance curves are arrived and compared with theoretical superjunction device curves and previous fabrication results. The analysis of interdiffusion influence on breakdown voltage is provided. Finally, the practical concentration equation and superjunction performance equation are derived, which can provide guidance for practical design.

Chapter 4

Partial SOI Superjunction LDMOS

The partial SOI superjunction LDMOS structure was previously proposed in university research projects. [33-35]. In these projects, the simulation work has been done to prove it has better performance than conventional LDMOS. However, the simulation work only focuses on simplified structures. In this thesis, the simulation is done by 3-D simulator DAVINCI in detail. Therefore, the structure variation is fully considered and specific parameters are given for fabrication purpose. In this chapter, firstly, device structure and operation is discussed in detail. Then, extensive simulation on device performance is summarized.

4.1 Review of partial SOI technology

The early partial SOI technology was used in CMOS/Bipolar technology [36, 37]. Take the CMOS device as example. In the device structure, the source/drain (SD) regions and part of the channel region adjacent to SD regions are formed on SOI film, while the middle part of the channel region is formed on the silicon bulk. The partial SOI structure is formed by the combination of selective epitaxial growth of silicon and a preferential polishing technique. The major benefits of the structure are as follows: (1) the parasitic capacitance, such as source-substrate, drain-substrate capacitance, is greatly reduced. (2) the isolation with peripheral device is realized by the partial SOI structure. (3) Compared with full SOI structure, the heat dissipations of the device is improved because middle part of the device is connected with bulk silicon.

In recent years, due to the application of LDMOS as RF amplifier, the partial SOI technology is used in the device structure to achieve high power added efficiency [38-40]. The new partial SOI formation technology is based on direct thermal oxide pinch-off.

The partial oxide platform is obtained by first forming a sequence of narrow deep trenches and then oxidizing the lower part of the trenches, shown in Fig. 4.1(a-c). The thickness of the oxide platform is not limited by normal thermal constrains. And, the oxide platform can be formed in any area of the device. The technology will be used in the proposed partial SOI superjunction LDMOS fabrication. The benefits of the technology are basically same as that mentioned before.

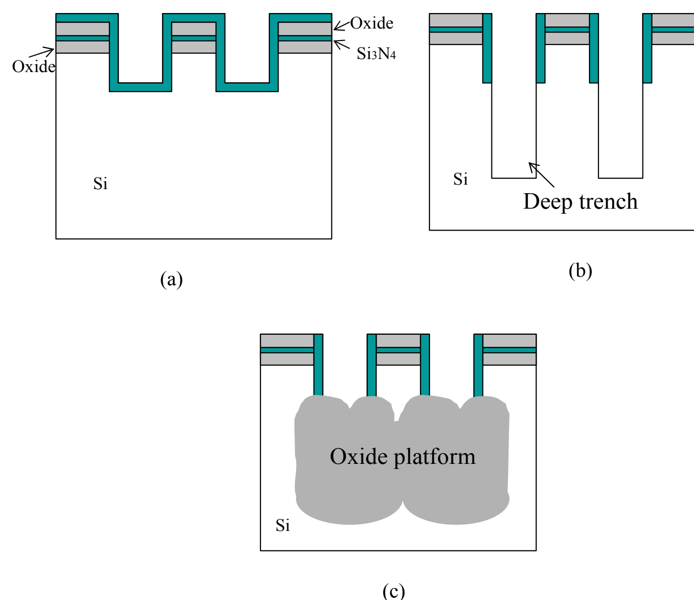


Fig. 4.1 Key process steps of the partial oxide platform formation (a) Shallow trench etch and oxidation mask formation (b) Deep trench formation (c) Oxide platform formation

Due the low parasitic capacitance in partial SOI device, it is also used as high speed power switches [41, 42]. The detailed studies of partial SOI device performance, especially breakdown performance have been done [43-45]. The study shows that if the silicon window is opened on the drain side, the breakdown voltage can very high

with a relative small oxide gap because the potential lines can spread in the substrate. If the silicon window is opened on the source side, the breakdown voltage is higher than that in the full SOI structure, but lower than in the JI case. And the breakdown voltage increases significantly with larger gap because more potential lines can be spread into the substrate.

4.2 Partial SOI Superjunction LDMOS

4.2.1 Structure

The partial SOI superjunction (PSOI SJ) LDMOS structure is shown in Fig. 4.2.

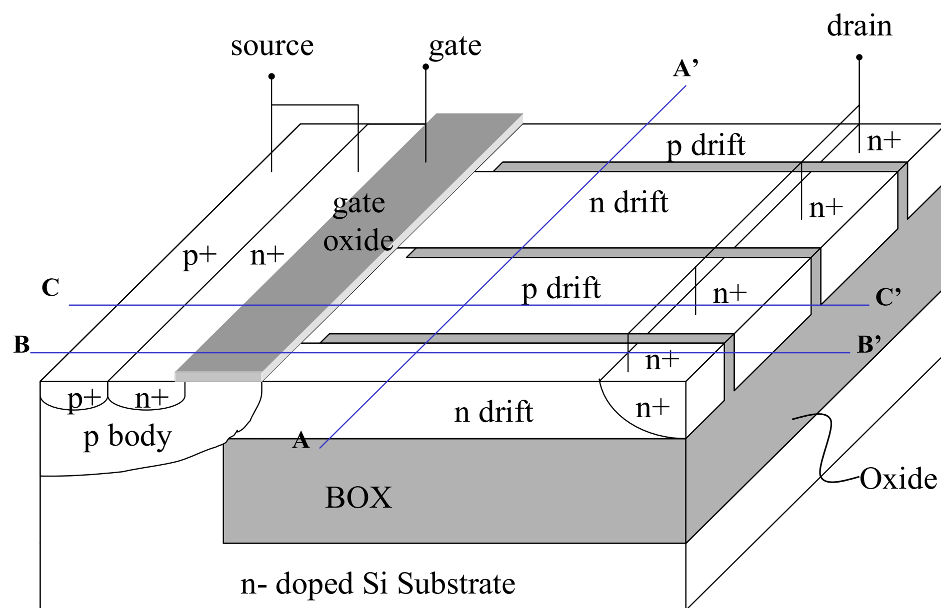


Fig. 4.2 Schematic structures PSOI SJ LDMOS

The partial SOI SJ LDMOS structure has several characteristics. First, the drift region of LDMOS structure is composed of alternatively stacked p and n columns, which is superjunction structure. Theoretical work has proved that the use of superjunction structure in LDMOS can improve it performance [11] [17-21] [28]. To solve the interdiffusion problem during the fabrication process, a thin oxide layer is

added between p, n column. Second, the buried oxide part (BOX) is only below the drain electrode. The benefit of partial SOI structure has been discussed in section 4.1.

4.2.2 Off-state and on-state Operation

The Off-state operation of the device is the same as that of superjunction device. The p column introduced in the drift region will help the depletion of n column. When the reverse voltage between drain (high voltage) and source (ground) increases, the depletion boundaries at n+ (drain)/p drift junction, p body (source)/ n drift junction and n drift/p drift junction extend in both sides. To ensure the depletion at the lateral n drift / p drift junction occurs properly with the added side wall oxide layer, the p drift must be electrically connected to the source by p-body and n drift must be electrically connected to drain. With proper p, n column concentration, the lateral depletion at the n drift / p drift junction will make the drift region fully depleted before the electrical field at n+ /p drift junction and p body / n drift junction reach the critical electrical field. After the fully depletion of drift region, the potential lines distribute uniform throughout the whole drift region, not concentrate around drain. Therefore, this structure can achieve higher breakdown voltage than that of conventional structure.

Since this is a lateral SJ structure, the substrate influence on the p, n columns depletion can't be ignored. This field action effect will introduce one kind of excess carriers in the drift region, which affect the charge balance. In the later simulation, the p column concentration is adjusted to count in the substrate effect. The substrate effect can only be included in 3-D simulation. 2-D simulation will ignore this effect; causing inaccuracy of the result. The breakdown voltage by 2-D simulation will be larger than that by 3-D.

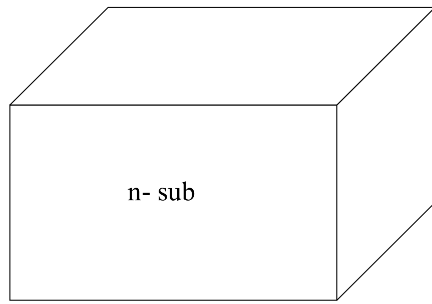
In the On-state, only n column can conduct current. The conduction area is only half of that of conventional device. However, the concentration of n column is at least one order higher than that of conventional one. From the specific on resistance definition equation (2.11), it is expected that the specific on resistance will be reduced to 5× lower than that of the conventional one. P column in on-state will cause some depletion in n-column. The effective current conductive area is reduced. 3-D simulation can include the p-column depletion effect while 2-D can't. The simulated current by 2-D is larger than that by 3-D.

4.2.3 Process steps

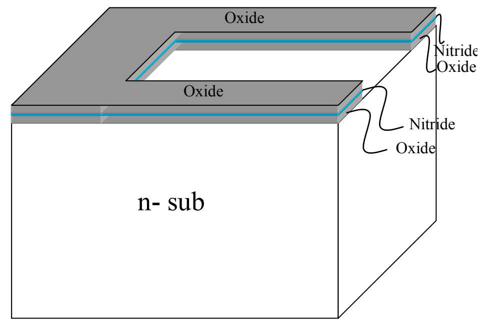
The process steps for the SJ LDMOS are divided to three parts: (1) partial SOI formation process, (2) p, n drift formation process and (3) MOSFET structure formation process. The three parts are in sequential order. Firstly, a thick buried oxide layer is formed below the drift region with process flow shown in Fig. 4.3. It is obtained by first forming a sequence of narrow deep trenches and then oxidizing the lower part of the trench to form thick layer of oxide. The starting wafer is lightly doped n-type or p-type bulk wafer. Suppose the wafer is n-type with concentration of 2×10^{15} cm^{-3} and thickness of 8μm. (Fig. 4.3a). After the wafer is ready, a serial of thermal oxidation, oxide deposition, nitride deposition are performed to form the oxide/nitride/oxide structure. Then, the three layer structure is etched according to the PSOI trench mask (Fig. 4.3b). After this, a 1.9 μm shallow silicon trench is etched in the n- wafer (Fig. 4.3c). Next, 60Å oxide is grown in the side wall and bottom of the shallow trench followed by nitride deposition on the exposed surface (Fig. 4.3d-e). After the performing anisotropic nitride and oxide etch, a 4.9 μm deep silicon trench is etched on the wafer (Fig. 4.3f-g). Till now, the shallow trench surface is totally

protected by oxide and nitride mask, and the deep silicon trench is ready for oxidation. Wet oxidation is performed to form the oxide platform (Fig. 4.3h). Secondly, p, n column is formed by implantation and drive-in process, shown in Fig. 4.4. After partial oxide formation, the oxide and nitride mask is removed followed by the phosphorous tilt implantation to form n column (Fig. 4.4 a-b). Then, about 500Å oxide is grown on all the surfaces, which will serve as sidewall oxide to prevent inter-diffusion between p, n columns (Fig. 4.4c).After the removal of oxide outside the drift region , a thin layer of poly-silicon is deposited in the trench followed with boron tilt implantation (Fig. 4.4d-f). After this, more poly silicon is deposited to fill up the trench (Fig. 4.4g). An oxide layer is deposited above the poly-silicon to prevent dopant out-diffusion, which is followed by a drive-in process for both p and n column formation (Fig. 4.4h). After the drive-in process, top oxide is removed and ploy planarization is performed to get the desired surface (Fig. 4.4i). Then, the oxide above the n drift region is removed to expose the n-drift region (Fig. 4.4j). Till now, the p, n column in the drift region is completely formed. Finally, the MOSFET structure is fabricated. The process steps are the same as those in the conventional MOS device fabrication, shown in Fig. 4.5. The gate oxide growth and gate poly deposition are the first two steps followed by gate poly pattern (Fig. 4.5a-c). Then, p-body is implanted and self-aligned to the gate followed by p-body drive-in (Fig. 4.5d). Next, Source and drain are implanted and annealed (Fig.4.5e). Finally, oxide is deposited and pattered on the device surface; aluminum contact is also deposited and patterned on the surface (Fig. 4.5f-g). After the passivation layer, the device fabrication is finished.

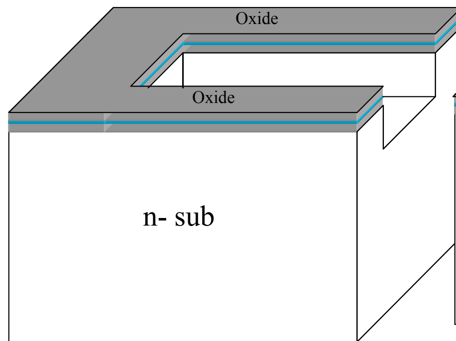
Fig. 4.5 shows the MOSFET structure formation process. Here the planar gate structure is used as example. If the trench gate or multi-gate is used in the structure, the process is more complex.



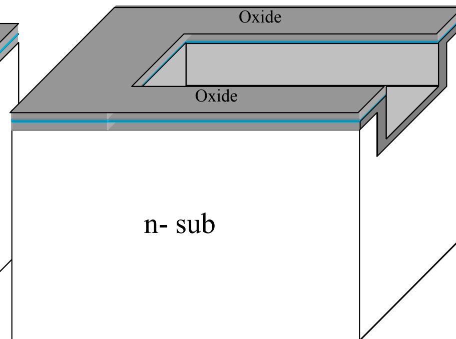
(a) Starting wafer



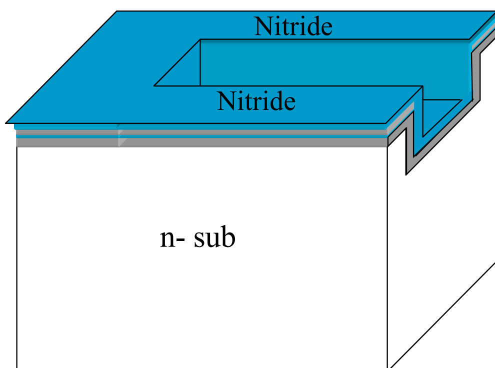
(b) Partial SOI trench Mask



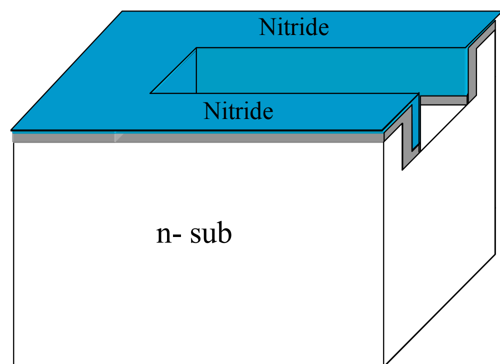
(c) 1.9µm shallow trench



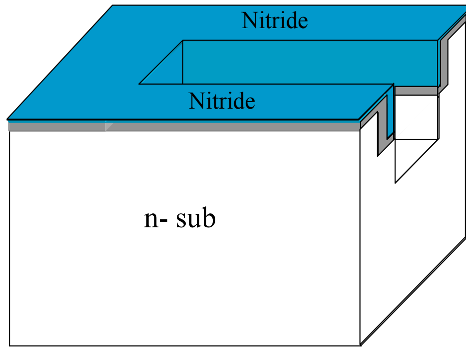
(d) Thin oxide growth
inside shallow trench



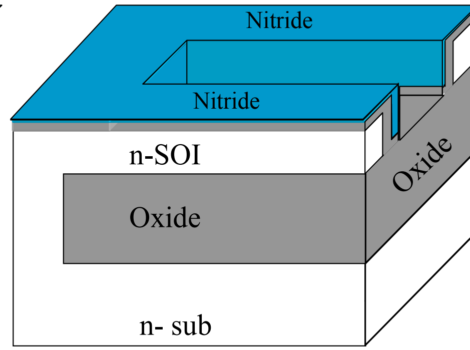
(e) Nitride deposition



(f) Anisotropic nitride and oxide etch

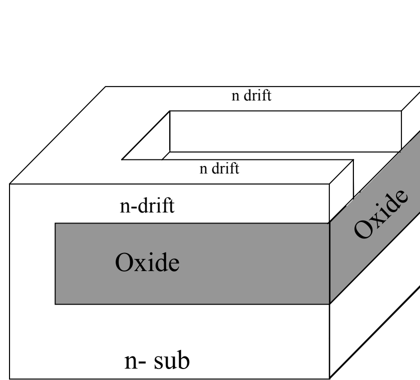


(g) Deep trench etch

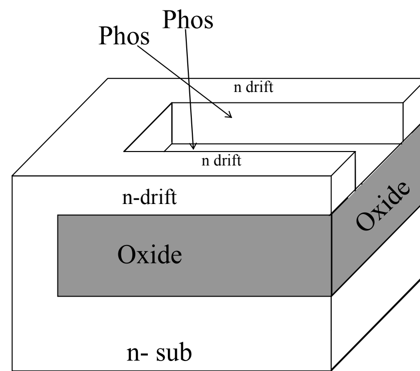


(h) Thermal oxide growth

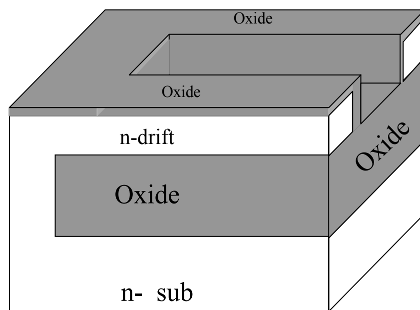
Fig. 4.3 Partial oxide formation process



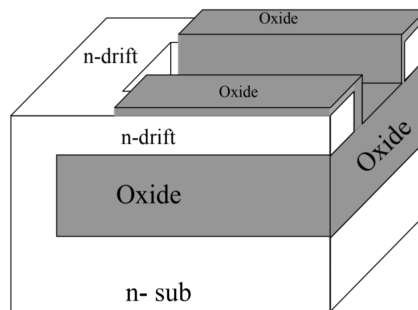
(a) Global oxide and nitride removal



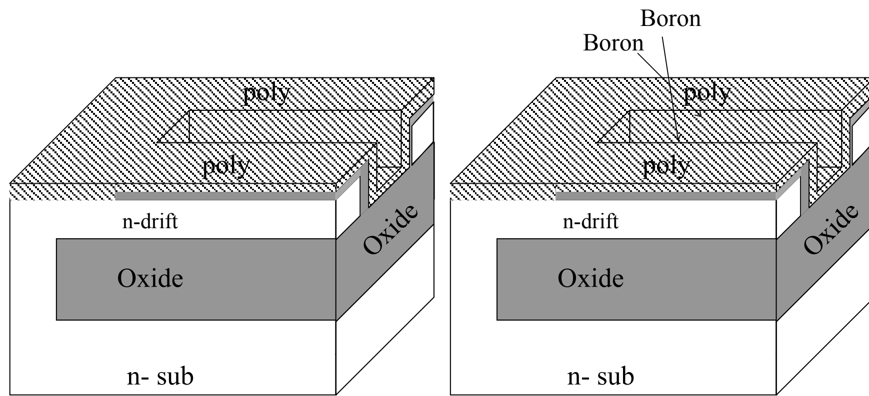
(b) Phosphorus tilt implantation



(c) Side wall oxide growth

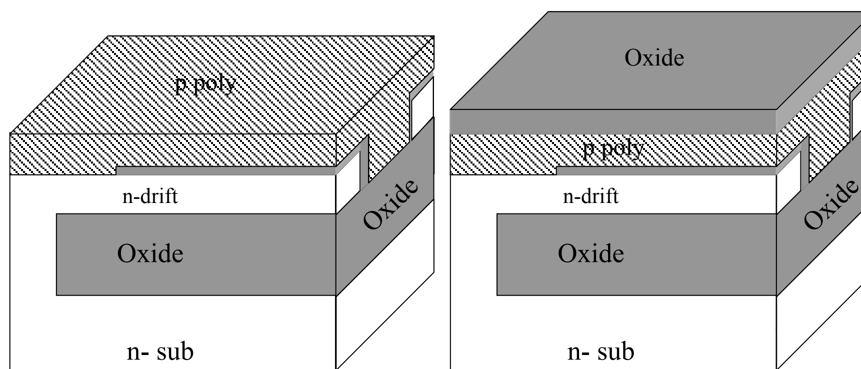


(d) Corner oxide removal



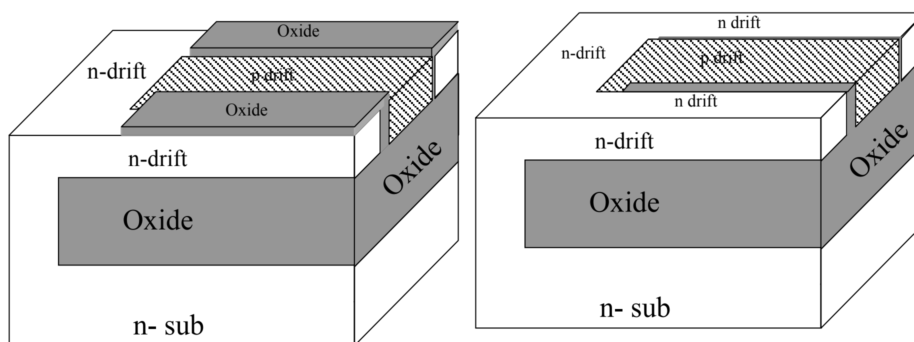
(e) Conformal poly deposition

(f) Boron tilt implantation



(g) Poly deposition to fill up the trench

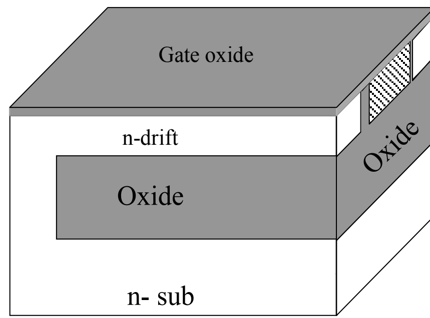
(h) Oxide deposition and p poly drive-in

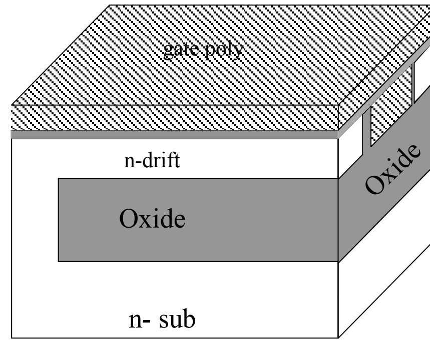


(i) Oxide removal and poly planarization

(j) the removal of oxide above the n-drift region

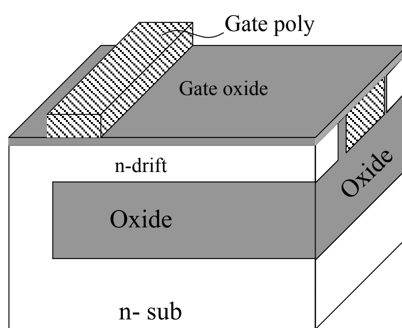
Fig. 4.4 P, n column formation process

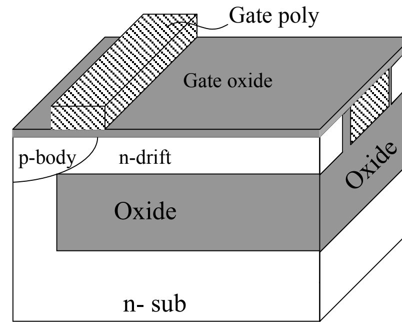




(a) Gate oxidation

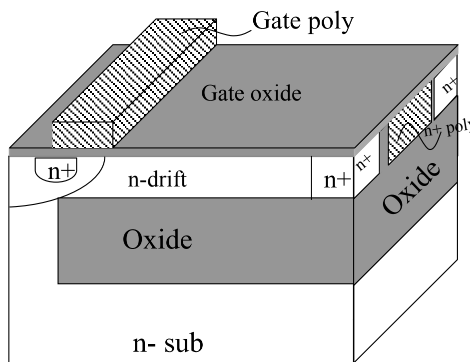
(b) Gate poly deposition

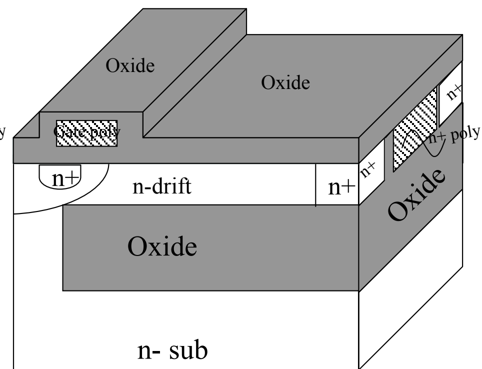




(c) Gate pattern

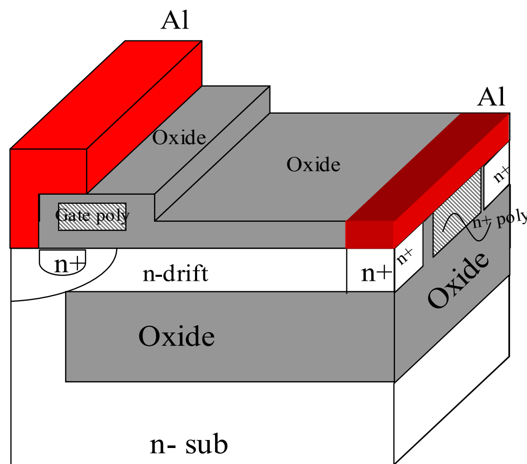
(d) P-body implantation and drive-in





(e) Source/drain implantation and annealing

(f) Plasma CVD Oxide
& BPSG Densification

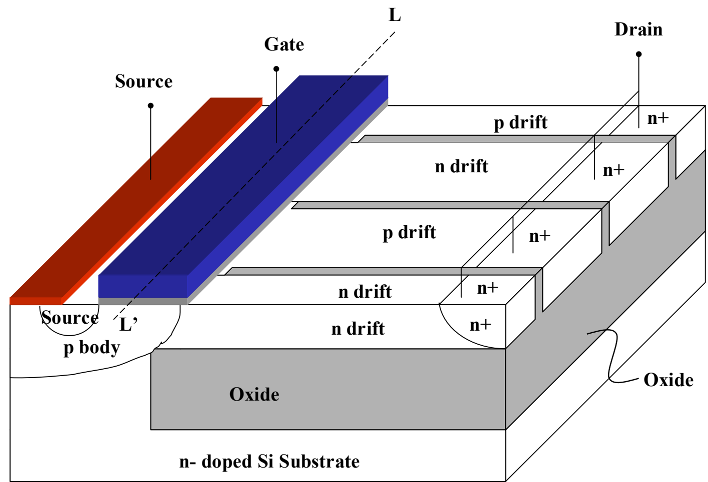


(g) Al Contact formation

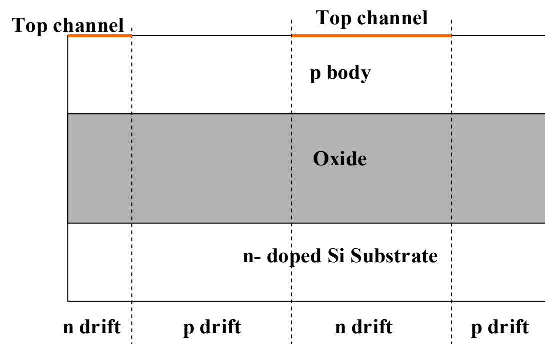
Fig. 4.5 MOSFET structure formation process

4.3 Gate variations of PSOI SJ LDMOS

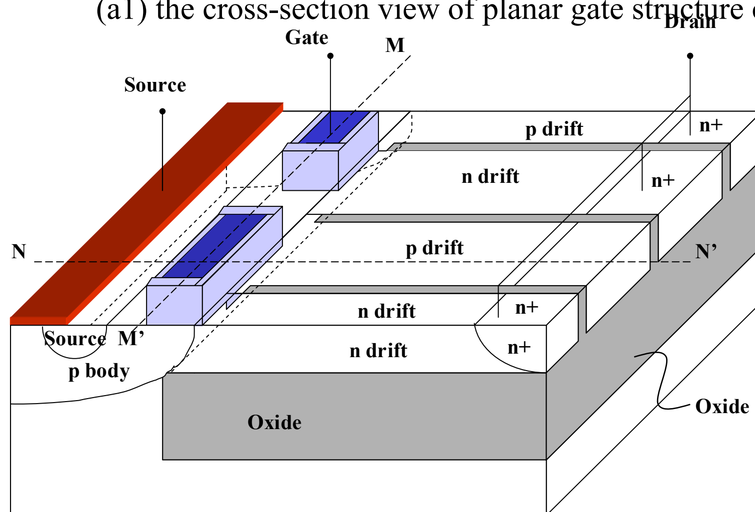
The device resistance can be further reduced by using different gate structures. Previously mentioned gate is planar gate. There is only one channel in the device. By using trench gate or all gate structure, the number of the device channel can be increased to 3 and 4. The increase of channel number can reduce the channel resistance, which still occupy a relatively bigger part in the total resistance of a superjunction device with breakdown voltage rating of 120V. The three kinds of gate structure, together with cross-section view, are shown in Fig. 4.6.



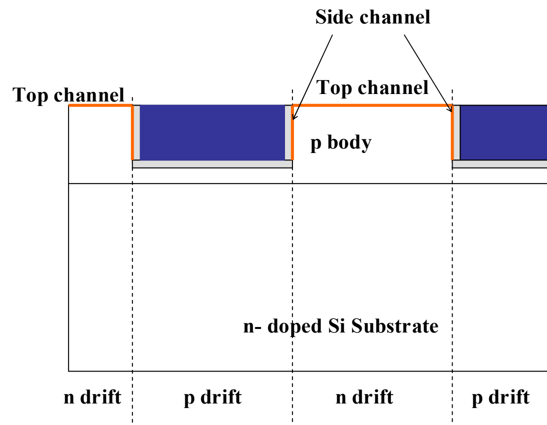
(a) Planar gate structure



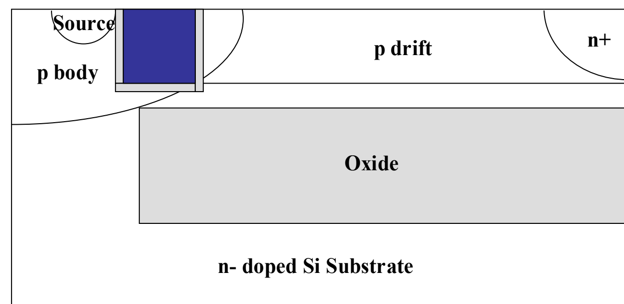
(a1) the cross-section view of planar gate structure cut along L-L'



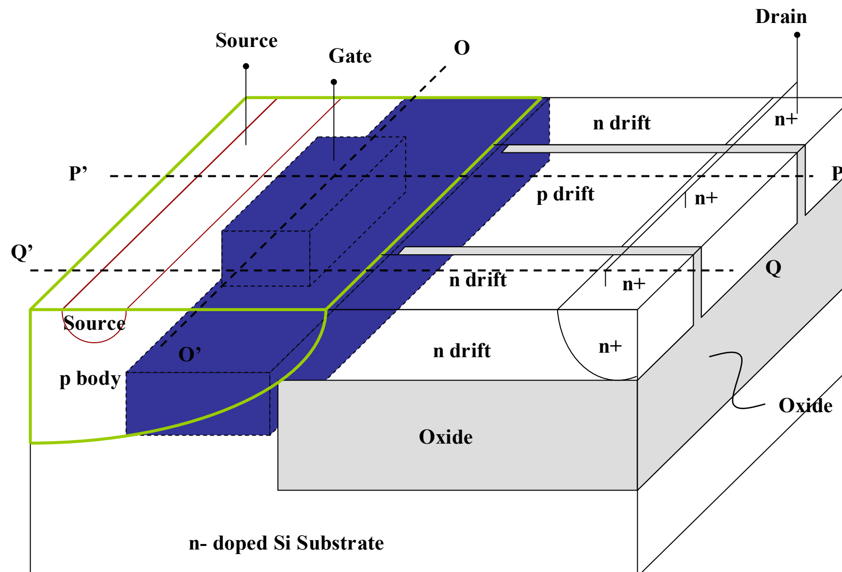
(b) Trench gate structure (top gate is not shown in the figure)



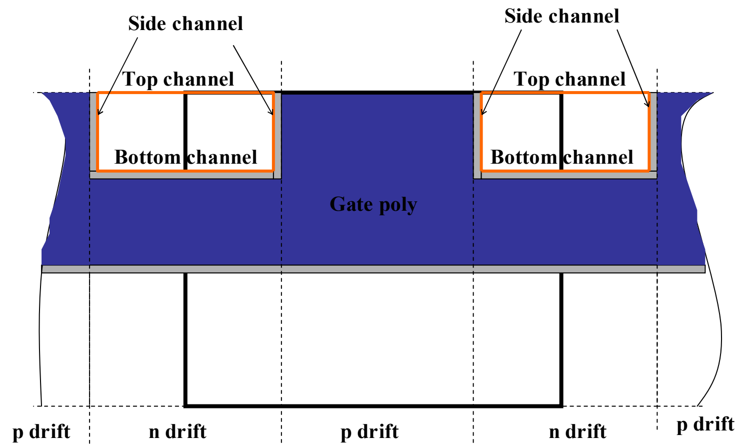
(b1) the cross-section view of trench gate cut along M-M’



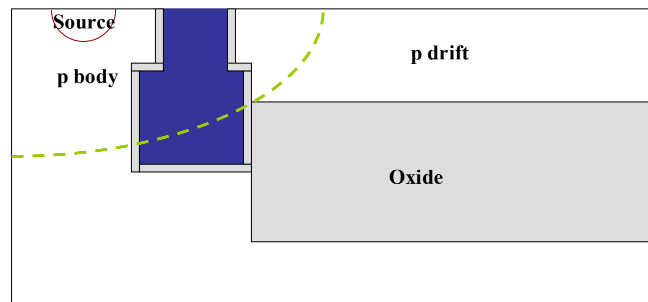
(b2) the cross-section view of trench gate cut along N-N’



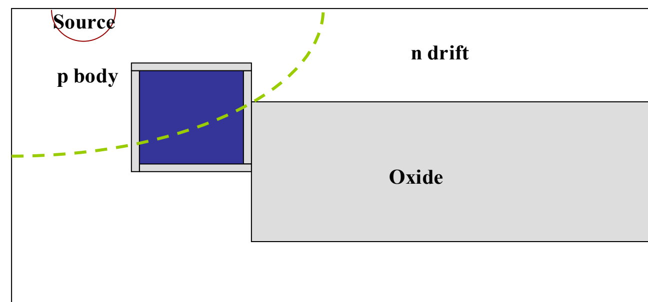
(c) All gate structure (top gate and gate oxide are not shown in the structure)



(c1) the cross-section view of all gate cut along O-O'



(c2) the cross-section view of all gate cut along P-P'



(c3) the cross-section view of all gate cut along P-P'

Fig. 4.6 The three kinds of gate structure and cross-section views (a) Planar gate structure (a1) the cross-section view of planar gate structure cut along L-L' (b) Trench gate structure (top gate is not shown in the figure) (b1) the cross-section view of trench gate cut along M-M' (b2) the cross-section view of trench gate cut along N-N' (c) All gate structure (top gate and gate oxide are not shown in the structure) (c1) the cross-section view of all gate cut along O-O' (c2) the cross-section view of all gate cut along P-P'(c3) the cross-section view of all gate cut along P-P'

The gate structure and channel position are clearly shown in Fig. 4.6. There is only one top gate and one top channel in planar gate device. In the trench gate device, there are two gates— top gate and trench gate. The trench gate is only inside the region

which is defined by the width p-drift. Due to the existence of trench gate, two side channels are added. The structure shown is deep trench device. In this structure, the trench depth is equal to or larger than the height of p, n drift. To ensure p body and p-drift contact properly, the right border of the trench must inside p-body to leave some space for p-body to contact with p-drift. The contact way between p-body and p-drift is clearly shown in Fig. 4.6 (b2). The other kind of trench gate structure is called shallow trench gate structure. In this structure, the trench gate is not deep enough to reach the bottom of p-body. The left part is for the dopant to diffuse through then connect with p-drift. The contact way between p-body and p-drift is different from the deep trench gate device. Not like Fig. 4.6(b2), the right border of the trench can be wider to touch the p-drift because the contact between p-body and p-drift is through lower part of p-body not the right part of p-body. The formation processes of deep trench and shallow trench device are also different. For deep trench device, the p-body must be formed before the gate formation. While, for shallow trench device the formation sequence between p-body and gate is not important. In the all gate structure shown in Fig. 4.6(c), only gate poly is there to show clearly the gate structure. The gate structure is formed by first etching a trench in the region which is aligned to the p-drift, then performing release etch through the trench to form the buried channel which is through the whole device width. After the gate poly is filled, the trench gate, buried gate and top gate comprise the all gate structure. The all gate structure produces four channels─ one top channel, two side channels and one bottom channel, when device is turned on. The channel structure is shown in Fig. 4.6(c1). The all gate structure can produce the maximum channel numbers in the structure. The gate structure in the region aligned to p-drift is shown in Fig. 4.6(c2). Both the trench gate and buried gate (wider gate) are there. It is better that the depth of the trench gate

equal to the p, n drift height. In this case, the side gate is the longest. The right border of the trench gate is not up to the p-drift to leave space for the p-body to contact with p-drift. The contact way is the same as the deep trench gate mentioned before. In the region aligned to the n-drift, there is only the buried gate, which is shown in Fig. 4.6(c3).

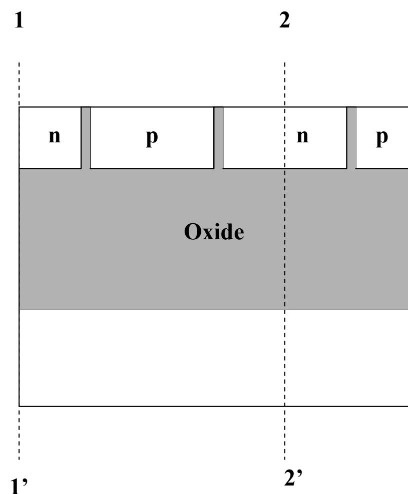
4.4 Simulation of PSOI SJ LDMOS

The simulation of the device is divided into two parts: process simulation and device simulation. Process simulation is to simulate the fabrication process to get the device structure, while, the device simulation is to simulate the electrical performance of device. PSOI SJ LDMOS, as a power switch, the main electrical characteristics are its Off-state breakdown voltage and on-state resistance. So, the device simulation is also divided into two parts: Off-state simulation and On-state simulation. The aim of device simulation is to check if the device performance has satisfied the required electrical characteristics. If not, the device parameters need to be changed to re-fabricate the device and re-check its characteristics until the device performance satisfies the requirement. Finally, the parameters need to be optimized to get optimum performance of the device. The final aim of the device simulation is to get the optimum process parameters for fabrication.

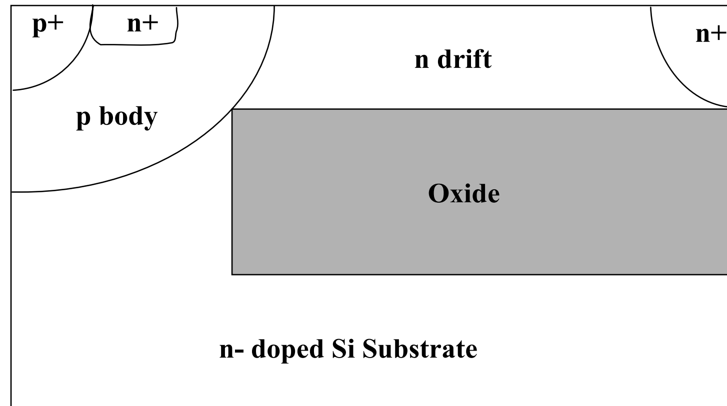
The Off-state breakdown voltage of the PSOI SJ LDMOS is designed to be 120V. The on-state resistance is expected to be lower than conventional structure due to the SJ structure.

4.4.1 Process simulation

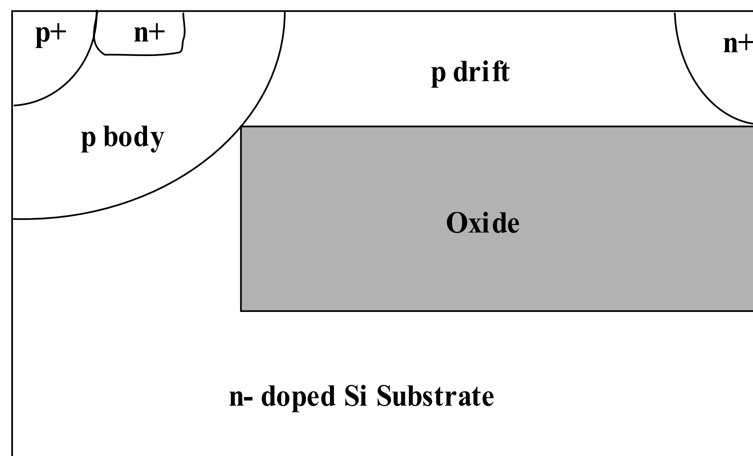
The process simulation will follow the process steps mentioned in section 4.3. The fabrication process is a truly 3-D process. Due to the software (TSUPREM4) limitation, the device is simulated by several cross-sections [46]. From Fig. 4.2, the cross-section cut along line A-A' is to simulate the partial oxide platform and p, n column formation process. The cross-sections cut along the lines B-B' and C-C' is used to simulate p-body and drain respectively. To simulate p-body and drain separately in n column and p column is aimed to get the better profiles. The three cross-sections are shown in Fig. 4.7. Cross-section A provides the detailed information about drift region. Cross-sections B and C give the profiles of p-body and drain.



(a) Cross-section A



(b) Cross-section B



(c) Cross-section C

Fig. 4.7 Cross-sections cut along (a) line A-A' (b) line B-B' and (c) line C-C'

To make the simulation result most close to the practical fabrication, the simulation models for each fabrication steps are carefully chosen. PD.TRANS model is used in the diffusion process to include the point-defect assistance effect. To accurately reflect the partial oxide shape and stress effect in the wafer, VISCOELA model, which will consider the viscous and elastic effects in the oxidation process, is used when forming partial oxide. In the ion implantation process, Monte Carlo model is used to the get the better dopant distribution profiles. In a word, the accurate numerical models, instead of approximate analytical models, are used in each process steps to get better simulation result.

There are some points needed to be noticed when simulating the three cross-sections.

(a) P, n column width

The simulation result of the cross-section A is shown in Fig. 4.8.

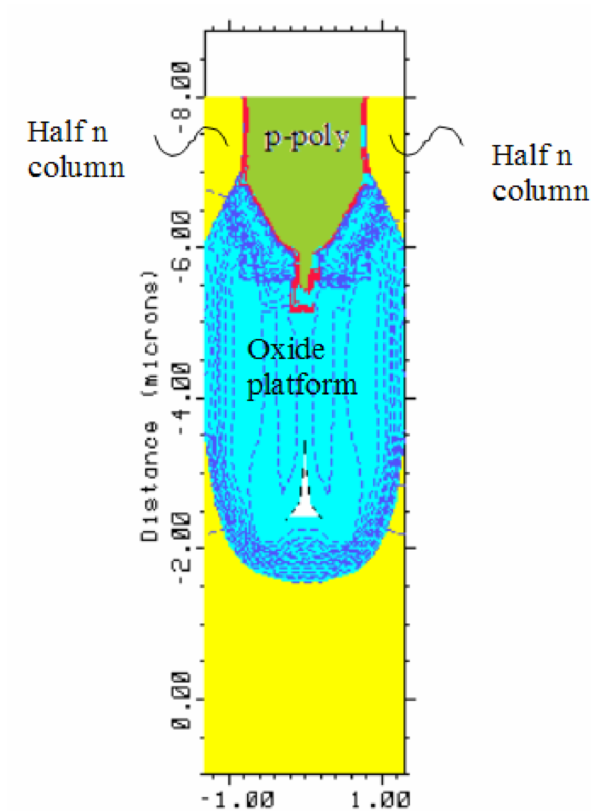


Fig. 4.8 Simulation result of cross-section A

Fig. 4.8 shows that the p column width is approximately equal to the shallow trench/ deep trench width, while n column width is approximately equal to the shallow trench/deep trench sidewall silicon width. To ensure the partial oxide can pinch-off both inside the deep silicon trench and inside the sidewall silicon, the trench width and sidewall silicon width should satisfy the thermal oxidation ratio. Therefore, the p n column width can't be equal, but constrained by the thermal oxidation ratio. Due to the minimum n column width is 0.6μm, the n column width is firstly decided as

0.6μm, 0.8μm and 1μm. Then, p column width is calculated according to the process steps given in Fig. 4.3 and Fig. 4.4. In the calculation, the sidewall oxide thickness, the oxide and nitride thickness in the shallow trench sidewall must be considered. The relationship between p, n column is not strictly proportional. The calculation process is given in Appendix B. The corresponding p column width is 1.03μm, 1.28μm and 1.5μm.

(b) P, n column concentration

After p, n column widths are decided; n column concentration can be calculated according to the equation $N = 1.2 \times 10^{12} w^{-\frac{8}{7}}$, given in chapter 2. The calculated n column concentration is not the optimum one. The optimum n column concentration is decided by a serial of 2-D simulations. The simulation structure is shown in Fig. 4.9. The 2-D structure is actually a diode structure. Compared with the Off-state structure, part of p+ is changed to n+ in the On-state structure, so that n column can conduct current when voltage applied. The structures with the same drift length but different n column concentration are tested for breakdown voltage and on-state resistance. For a certain structure, n column concentration is chosen around the calculated one, while p column concentration is calculated using the equation $W_n \cdot N_n = W_p \cdot N_p$, where W_n and W_p are the widths of n and p columns, N_n and N_p are the doping concentrations for n and p columns, respectively. After all the breakdown voltages and on-resistances are got, the figure of merit(FOM), which is defined as $V_{br}^2/R_{on,sp}$ is calculated for each structure. The structure with the maximum value of FOM is the optimum structure.

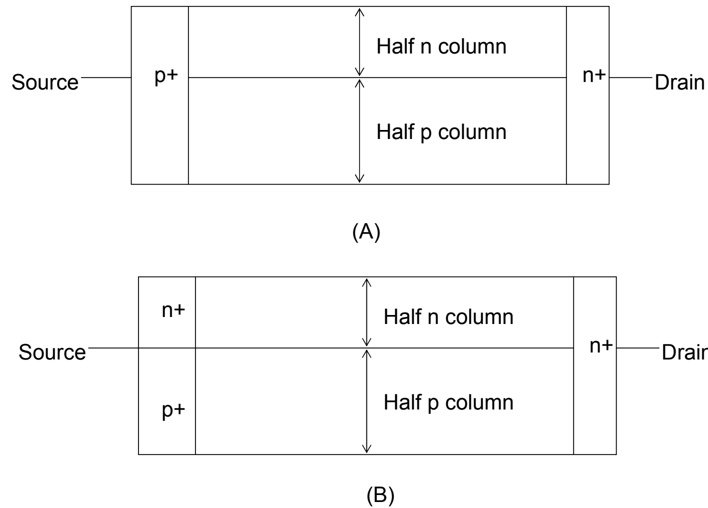


Fig. 4.9 2-D simulation structure (A) Off-state simulation structure (B) On-state simulation structure

The FOM figure is shown in Fig. 4.10. From Fig. 4.10, it is easy to know that the optimum n column concentration is $4.2\times10^{16}cm^{-3}$. The corresponding p column concentration is calculated to be 2.76×10^{16} cm^{-3} by using equation $W_n \cdot N_n = W_p \cdot N_p$.

The resulted n column concentration is right, but p column concentration has big error. This is due to the cross-sections of n column and p column are not rectangular, which is clearly shown in Fig. 4.8. The accurate value of p column concentration should be calculated by using the area ratio of the p, n column cross-sections. And the resulted p column concentration will be further adjusted through device simulation to get the final value.

During the fabrication of p, n column, it is required that the column concentration variation within the 10% of the required one in all the directions. This is the charge balance requirement. P column concentration is easier to be made uniform because the poly-silicon is used. N column concentration is hard to achieve uniform especially in the vertical direction. Fig. 4.8 shows that, in the vertical direction n column thickness is not uniform. It varies from 1.2µm to 1.8µm. To reduce the doping variation in the vertical direction, high energy implantation is used. For different

implantation angle, the implantation energy used is different. Due to the practical limitation of implantation energy to 250 Kev, the driven-in time is chosen to 300min for 1μm n column width device.

Although, the long diffusion time will cause substrate dopant out-diffusion, it is still used because non-uniform doping distribution will influence breakdown voltage seriously. Also, the dopant out-diffusion problem can be solved by choosing thicker wafer.

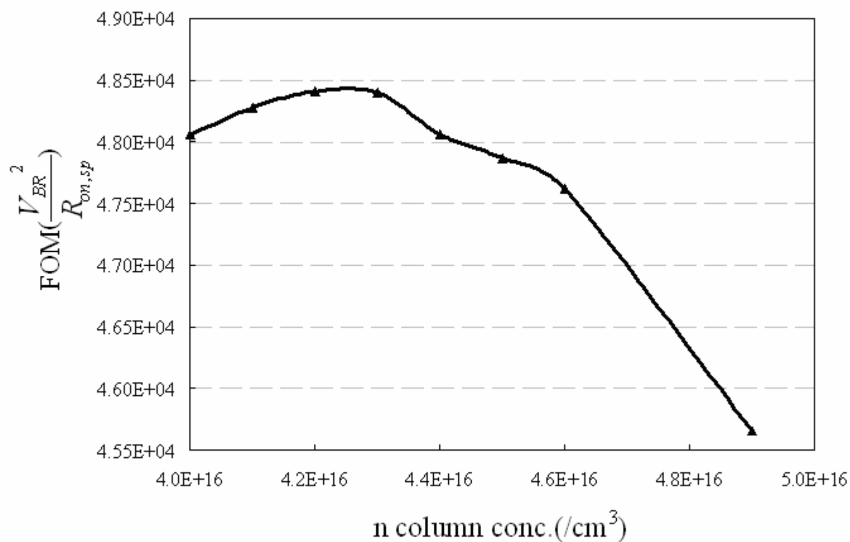
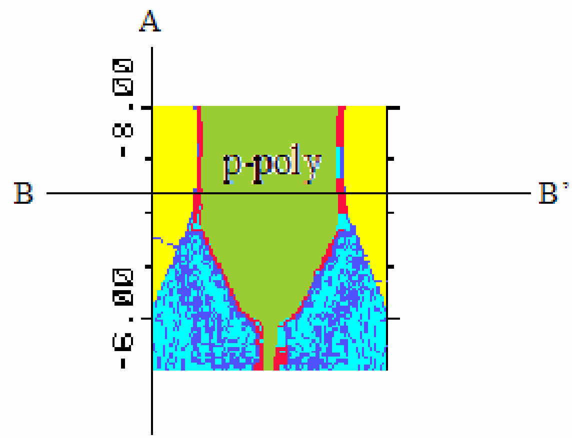
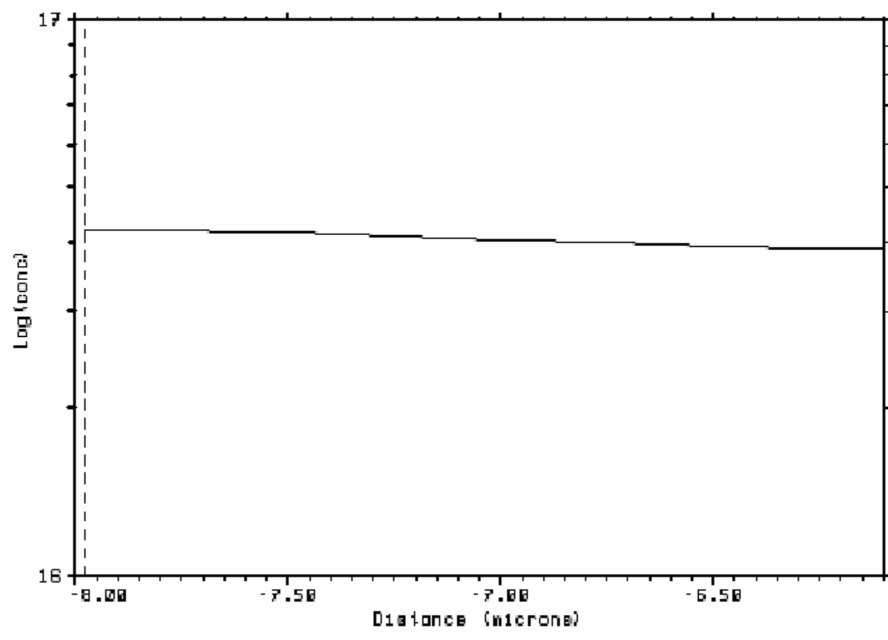


Fig. 4.10 The relationship between figure of merit and n column concentration with the drift length fixed

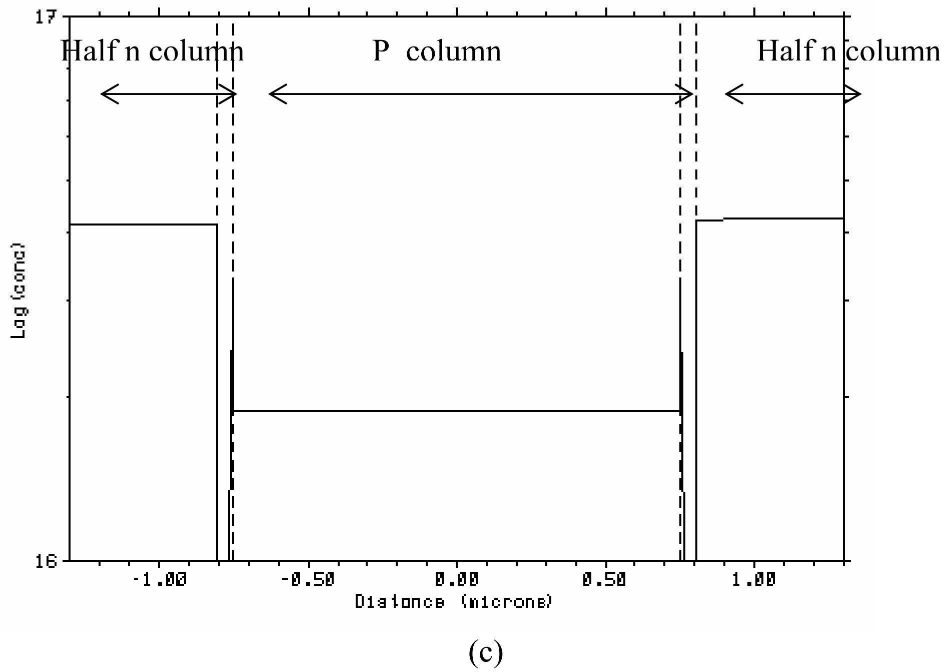
The doping profiles for the device with n column width of 1μm are shown in Fig. 4.11.



(a)



(b)



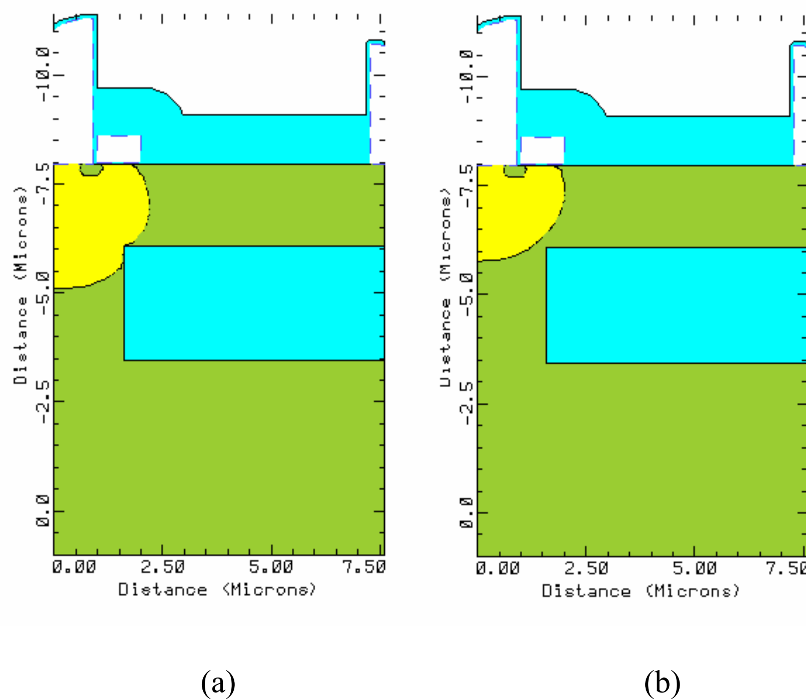
(c)

Fig. 4.11 (a) p,n column structure extracted from Fig. 4.7. (b) n column doping profile along the line A-A' in (a). (c) p, n column doping profile along the line B-B' in (a). The targeted n column concentration is $4.2\times10^{16}cm^{-3}$, and the targeted p column concentration is $1.87\times10^{16}cm^{-3}$.

Fig. 4.11 (a) shows the two cut lines A-A' and B-B' in the p, n column structure. In the line A-A', the n column thickness is maximum, and the n column concentration variation is maximum. The profile in this line is used to inspect the n column concentration. Fig. 4.11(b) shows the n column profile along this line. If the concentration in the profile varies within in 10% of the targeted concentration, the n column concentration is ok. In this example, the targeted n column concentration is $4.2\times10^{16}cm^{-3}$, the concentration should be in the range of $3.78\times10^{16}cm^{-3}$ ~ $4.62\times10^{16}cm^{-3}$. Fig. 4.11 (c) shows the doping profile cut along line B-B'. The profile shows that in the horizontal direction, the p, n column profiles are very uniform. The region inside the two adjacent dash lines is the sidewall oxide region. The targeted p column profile is 1.87×10^{16} cm^{-3}, which is the final value decided by device simulation.

(c) P-body and drain profiles

The purpose of the simulating cross-section B is to get the p-body doping profile. The simulation is done along the n-drift cross-section. In theory, the p-body should touch the buried oxide which is shown in Fig. 4.12(a). But, this will need very high implantation energy, which is not available in practical situation. So, the maximum available implantation energy 250V is used in the simulation and the threshold voltage is checked during the simulation process to ensure the implantation dose used is correct. The resulted figure is shown in Fig. 4.12(b).



(a) (b)

Fig. 4.12 (a) theoretically required p-body (b) achievable p-body by simulation

The drain profile is arrived by simulating cross-section C. The simulation is done along p column because the junction between drain and p column is important for the breakdown voltage. The implantation energy used is also the maximum available energy.

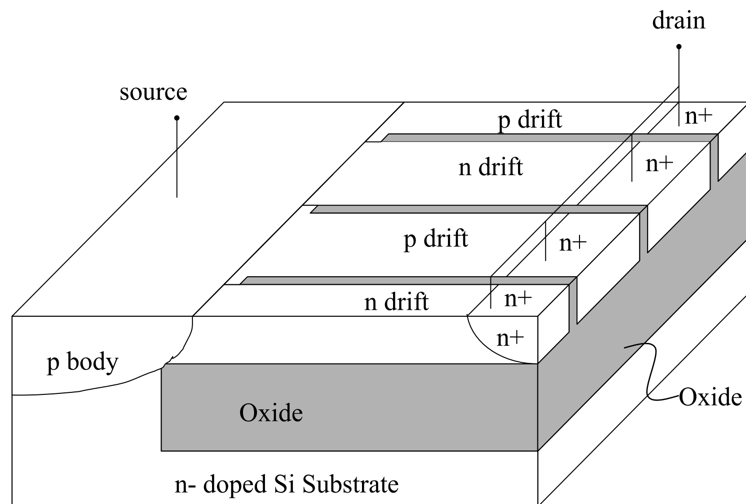
4.4.2 Planar gate device simulation

After the device is ‘fabricated’ by TSUPREM4, the resulted structure and doping profile are imported to device simulation program such as MEDICI, DAVINCI to get the electrical characteristics [47, 48]. Due to the 3-D structure of the device, DAVINCI is chosen as the simulation program. However, it is not a truly 3-D program. DAVINCI can only accept one cross-section from TSUPREM4, and the 3-D structure is formed by simply extending the cross-section in the third dimension.

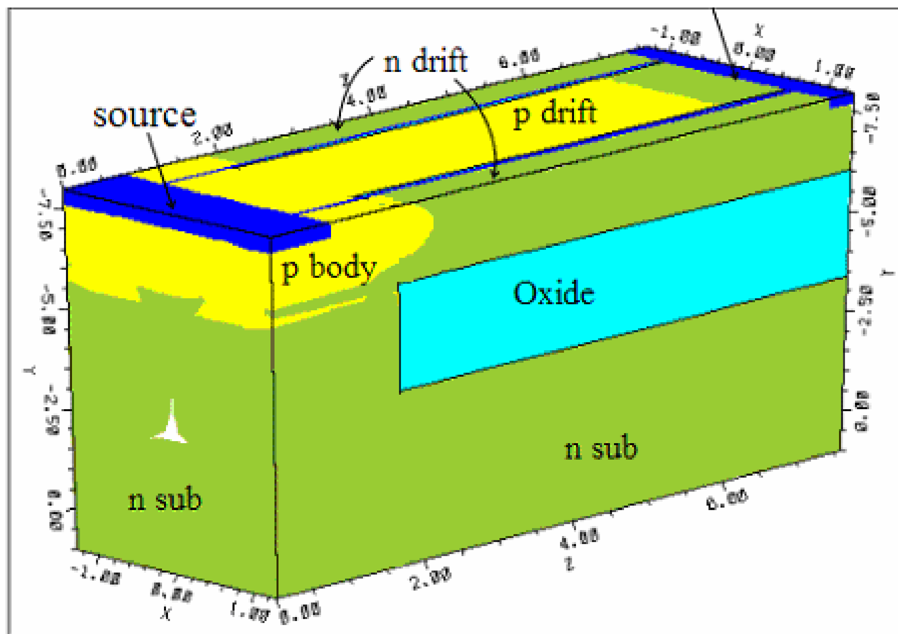
(a) Off-state simulation

Off-state simulation is to test the breakdown voltage of the device. The drift region structure is very important in deciding the breakdown voltage. So, the cross-section A shown in Fig. 4.8(a) is used as the imported plane. To use this cross-section ensures that the p, n column and buried oxide are formed by practical process steps. While, some relatively unimportant parts in deciding breakdown voltage such as p-body, drain are defined in the third dimension according to the profiles given by the simulation results of cross-sections B and C. Source and gate are neglected in testing Off-state breakdown voltage. The simulation structure is shown in Fig. 4.13.

The colors for different part in Fig. 4.13 (b) are different from the 2-D structure shown in Fig. 4.8. This is due to different program TSUPREM4, DAVINCI used. However, in the drift region of the structure, each cross-section perpendicular to the current flow direction is the same as the cross-section A shown in Fig. 4.8.



(a)



(b)

Fig. 4.13 (a) Schematic view of Off-state structure and (b) Off-state structure in Davinci

When breakdown occurs in the device, the leakage current arrives at 1E-9 Amps. The breakdown structure with equal potential line and impact ionization contour distribution is shown in Fig. 4.14. While, the parameters used in the structure and the breakdown data are shown in Table 4.1.

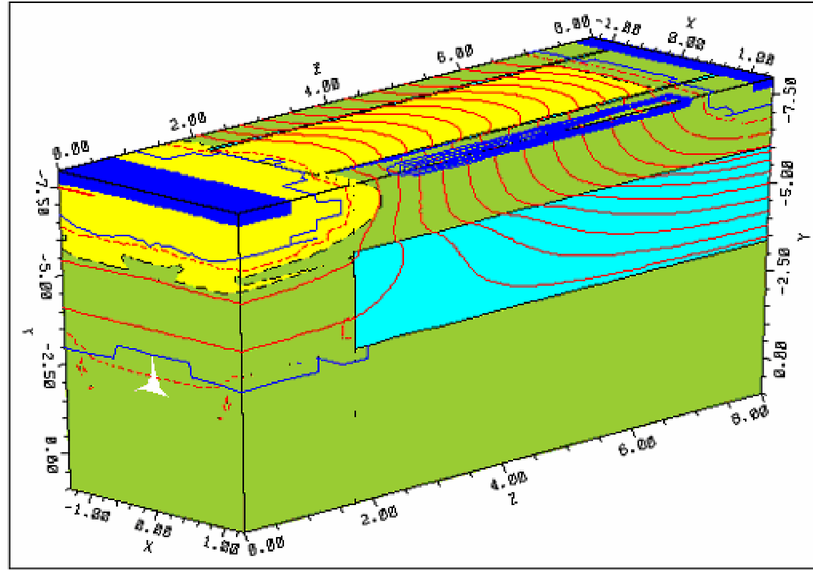


Fig. 4.14 The Off-state structure at breakdown. The breakdown voltage is 126V. The potential lines are red solid lines at 10V interval. The impact ionization contours are blue solid lines. The depletion boundary lines are red dashed lines.

Table 4.1 The parameters and breakdown voltage of the device shown in Fig. 4.13

N column width	P column width	N column conc.	P column conc.	Total length	Drift length	Vbr
0.98µm	1.50µm	4.20×10^{16} cm^{-3}	1.87×10^{16} cm^{-3}	8µm	5.5µm	128V

Fig. 4.14 shows that p, n columns are fully depleted, which can be observed from the red dashed depletion boundary lines. The potential lines are uniformly distributed in the drift region. Due to the thick oxide (about 4µm) used, the potential lines only distribute in the drift region and inside the buried oxide. No potential lines spread into the bulk. The impact ionization contours indicates that the breakdown occurs inside n column near the drain. The breakdown data also show that the breakdown position is near the surface.

In previous section, how to decide the p, n column widths and p, n column concentrations has been discussed. The optimum n column concentration can be

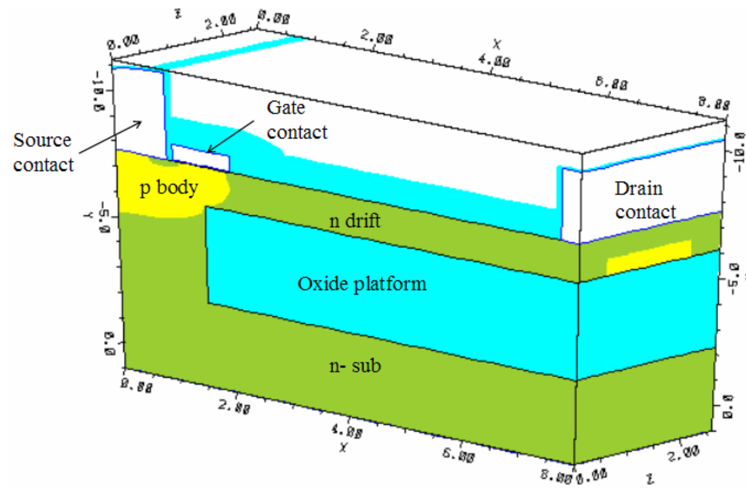
decided in advance, while, optimum p column concentration must be decided by the 3-D Off-state simulation.

Initial p column concentration can be calculated by the optimum n column concentration and the area ratio of p, n column cross-section. Then, by adjusting the p column implant dose in the process simulation to get the desired p column concentration. After this, the cross-section A is imported in DAVINCI to test the breakdown voltage. By observing the 3-D breakdown structure to decide p column concentration is too low or too high, then change p column implant dose in the process simulation again until the 3-D breakdown structure shows satisfying result such as p, n column depleted completely and potential lines distribute uniformly. Normally the calculated p column concentration is higher than the optimum one. By changing p column concentration to get the optimum the breakdown structure, the substrate assisted depletion effect or field action effect has been counted in.

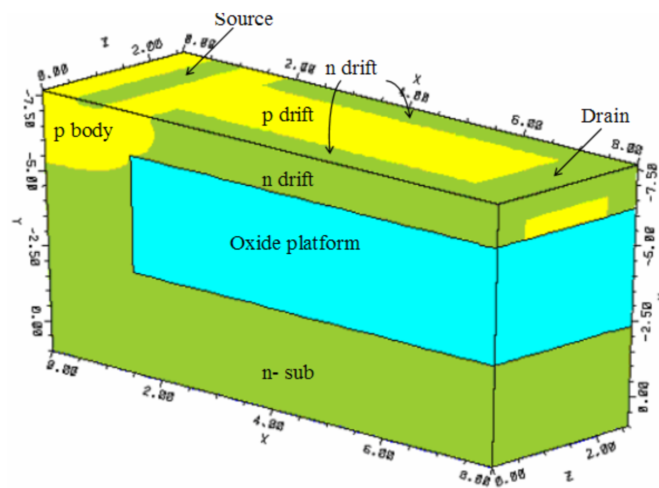
Other parameters such as drift length can be calculated in advance and adjusted through the 3-D Off-state simulation.

(b) On-state simulation

For planar gate device, the device structure is relatively easy to get in DAVINCI. The method is to import the cross-section B to DAVINCI. Then, define the p, n column in the third direction. The device structure in DAVINCI is shown in Fig. 4.15. Fig. 4.15(a) shows the On-state structure. The structure cut along certain Y plane to show p, n column is in Fig. 4.15 (b). In this structure, the p, n columns are defined by the author. The oxide platform is imported from cross-section B, not fabricated by process simulation.



(a)



(b)

Fig. 4.15 the On-state structure formed by importing cross-section B to DAVINCI (a) the whole structure (b) structure cut along certain Y plane to show p, n columns.

For the device with n column width of 1μm, the on-state performance data are shown in table 4.2. The structure shown in Fig. 4.15 is used in the simulation. The saturation current is measured when gate voltage is 20V. The on-resistance is measured when gate voltage is 20V and drain voltage is 0.5V. The specific on-resistance is calculated by the on-resistance multiplying the cross-section area of the drift region, which is perpendicular to the current direction. Different from the vertical device, the multiplied area is not the device surface area.

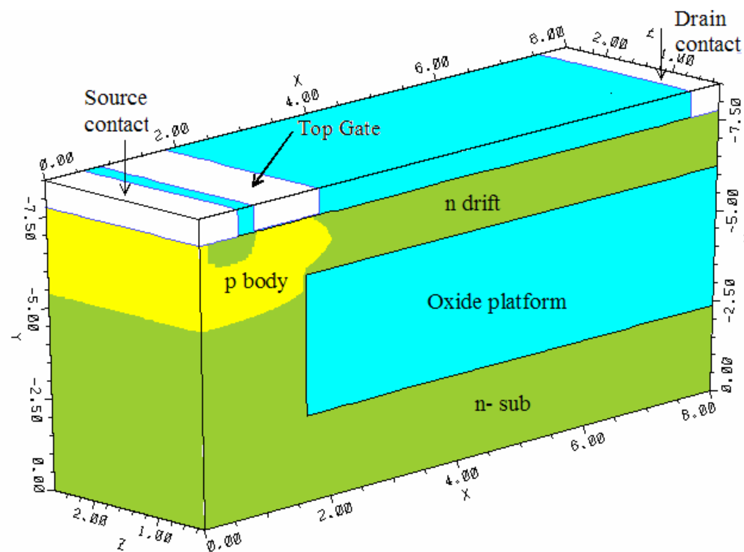
Table 4.2 The on-state performance data of the device with n column width of 1μm

Threshold voltage	Saturation current	On-resistance	Specific on-resistance
2.2V	4.43×10^{-4} A	11.3 KΩ	4.39×10^{-4} Ω-cm^2

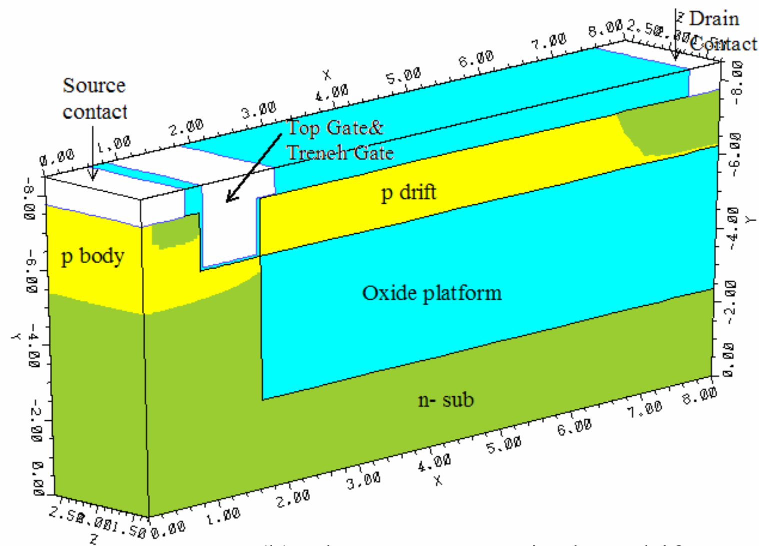
4.4.3 The 3-D simulation structures in DAVINCI

Previous simulations are about the planar gate structure. For trench gate and all gate structures, only on-state simulation is needed. This is because the gate structure has very little influence on the device breakdown voltage. And the previous Off-state simulation structure is without gate and source.

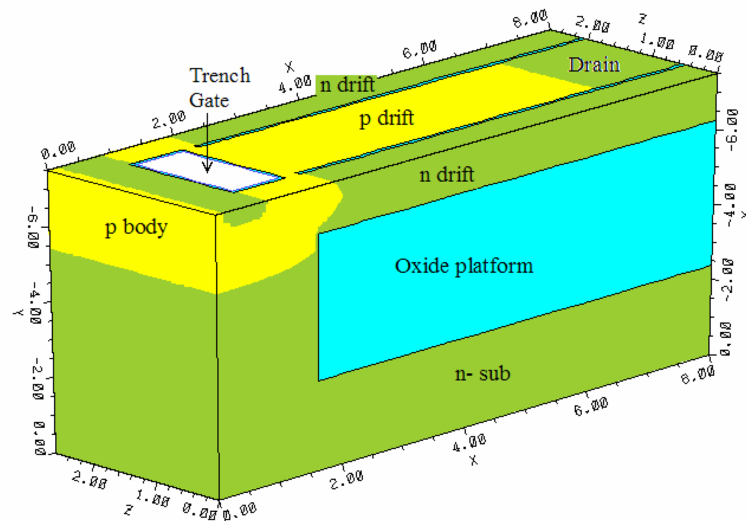
The trench gate on-state simulation structure is shown in Fig.4.16. The three cutting figures at different position clearly show the trench gate structure. The 3-D structure is totally defined in DAVINCI. The profile information is got from TSUPREM4 process simulation. Fig. 4.16 shows that the trench gate is aligned to the p-drift region.



(a)The structure cut in the n drift region



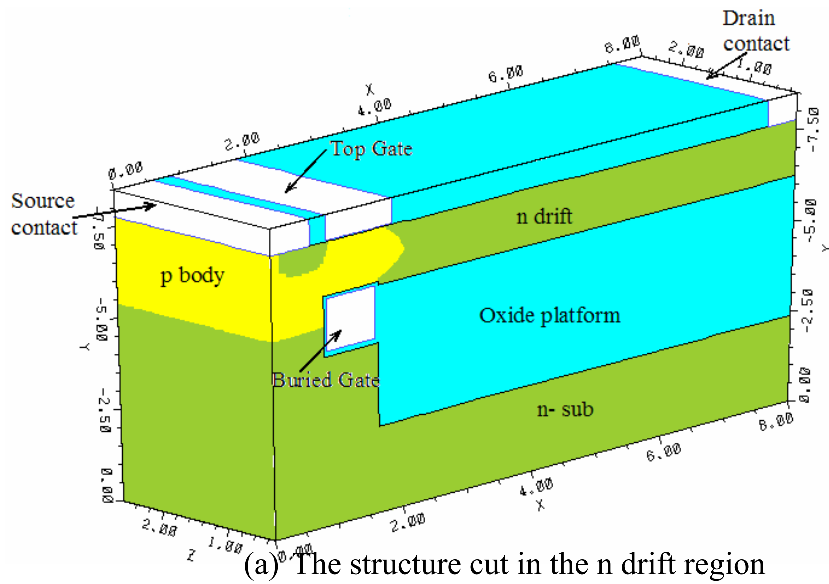
(b) The structure cut in the p drift



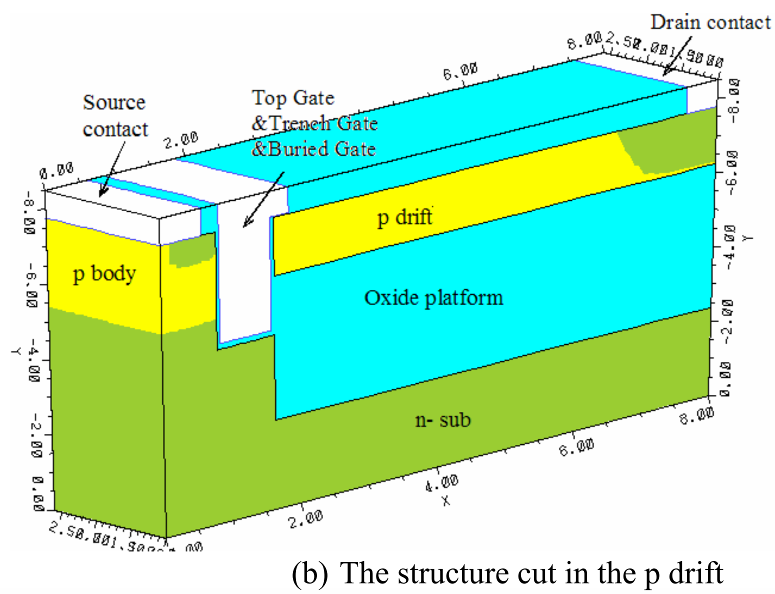
(c) The structure cut on the top

Fig. 4.16 The On-state simulation structure of the trench gate device (a) the structure cut in the n drift region (b) the structure cut in the p drift region (c) the structure cut at the top

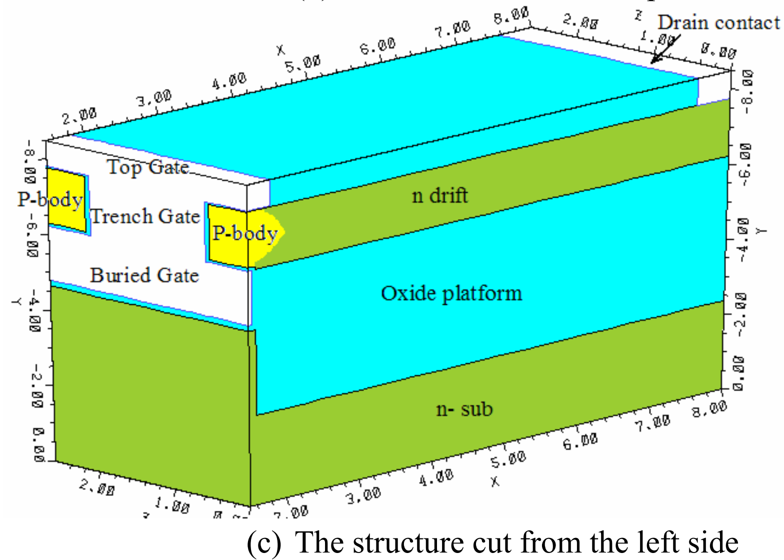
The all gate simulation structure is shown in Fig. 4.17.



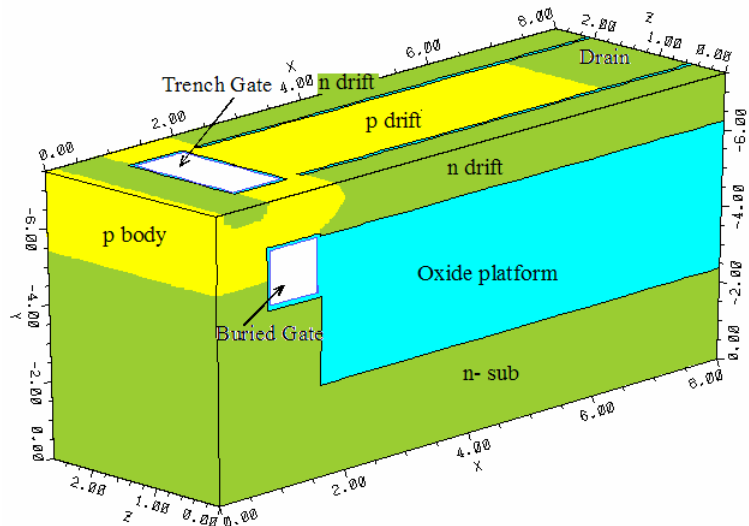
(a) The structure cut in the n drift region



(b) The structure cut in the p drift



(c) The structure cut from the left side



(d) The structure cut from the top

Fig. 4.17 The On-state simulation structure of the all gate device (a) the structure cut in the n drift region (b) the structure cut in the p drift region (c) the structure cut from the left side (d) the structure cut from the top

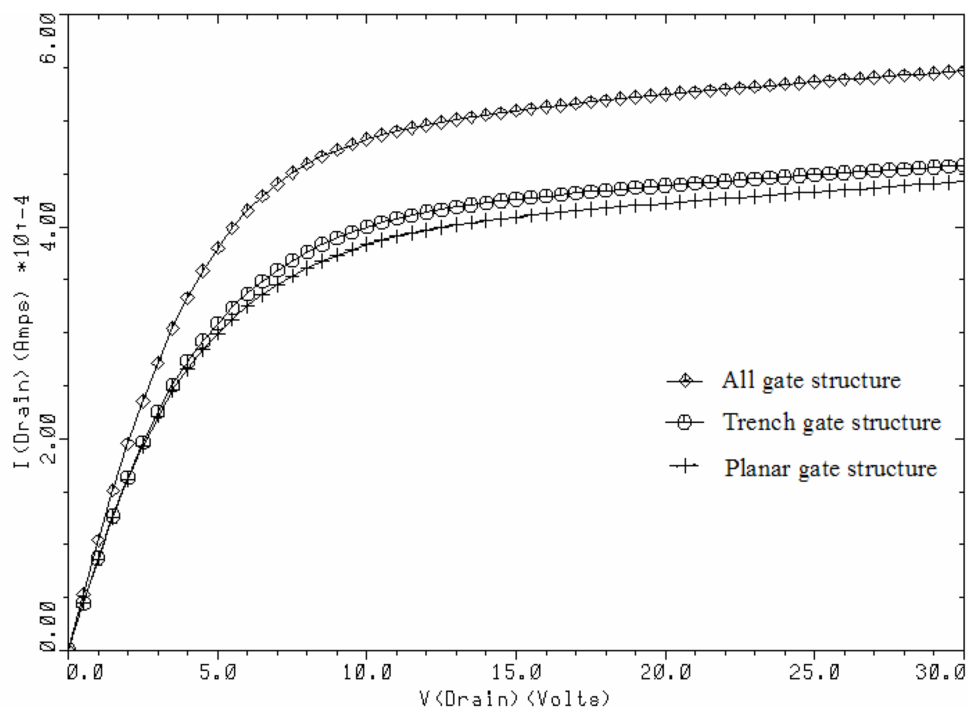
Due to the grid number limitation, all the structure is defined in the DAVINCI. From the structure cut in the n drift, only the top gate and buried gate can be seen. From the structure cut in the p drift, the top gate, trench gate and buried gate can be seen. From the structure cut in the left side, we can see the buried gate is connected together in the buried channel. The structure cut from the top shows the contact way between p-body and p-drift.

4.4.4 Summary of the simulation results

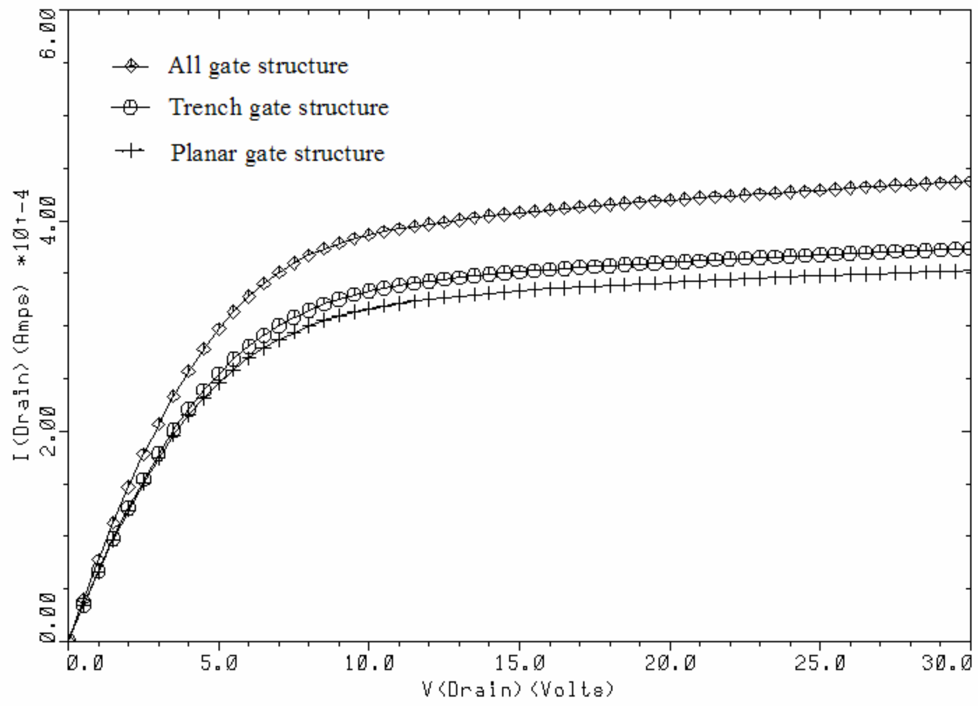
To compare the on-state performance fairly among the three kinds of gate structure, the three kinds of structures are completely defined in DAVINCI without TSUPREM4 importation. This is because the all gate structure is complex and has to be totally defined in DAVINCI. To make sure there are no other effects that affect the simulation result, the other two kinds of structures are also totally defined in DAVINCI. The structure definition includes the grid definition, different region definition and all kinds of profiles definition such as p, n column profile, source, drain

profile etc. The information needed for the structure definition is got from the TSUPREM4 process simulation.

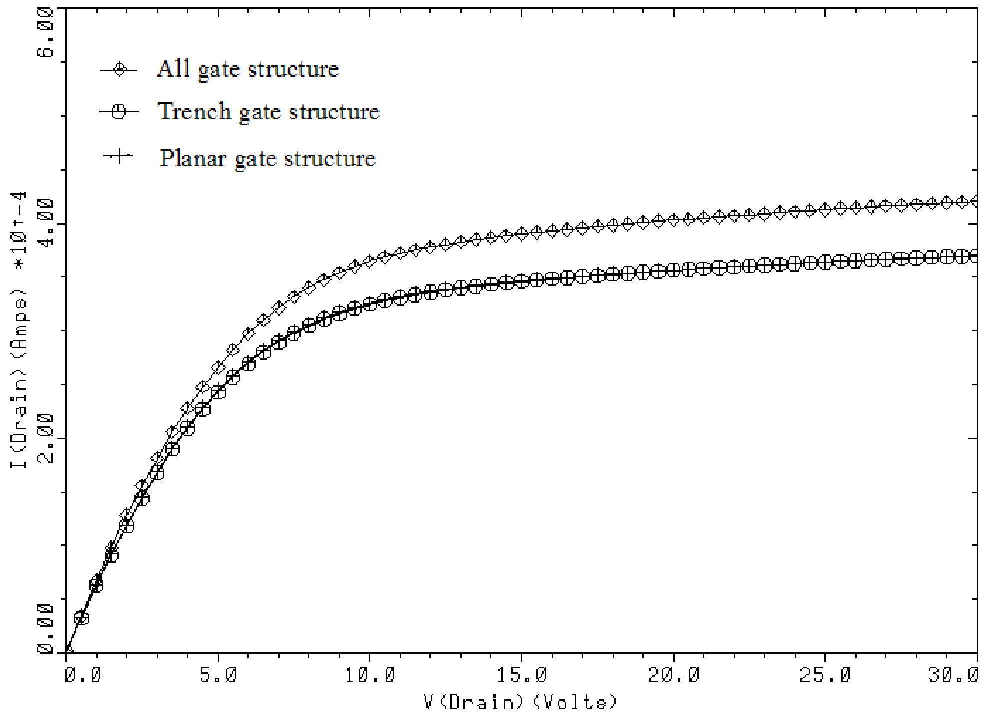
The on-state performance includes threshold voltage, specific on-resistance and saturation current. To compare the on-resistance and saturation current, the drain curves at gate voltage of 20V are drawn together in Fig. 4.18 for three kinds of gate structure. In Fig. 4.18(a), the n column width is fixed at 1μm, only gate structure has variations. In Fig. 4.18(b) and (c), the n column width is fixed at 0.8 μm and 0.6μm respectively. All the three figures show that the on-state performance of all gate structure is much better than that of other two kinds of structure. The on-state performance of trench gate structure and planar gate structure are relatively similar. In Fig. 4.18(c), the trench gate curve and planar gate curve almost overlap because the channel resistance occupies a very small part of the total resistance. The on-state performance data for the three cases are also in Table 4.3.



(a)



(b)



(c)

Fig. 4.18 The drain curves at gate voltage of 20V for three kinds of gate structures (a) for n column width of 1μm (b) for n column width of 0.8μm (c) for n column width of 0.6μm.

Table 4.3 The comparison of on-state performance data of devices with different gate variations and different n column widths

On state / N column width		Saturation current	On-resistance	Specific ON resistance
1μm	All gate	5.47×10^{-4} A	9.36 KΩ	3.63×10^{-4} Ω-cm^2
	Trench gate	4.58×10^{-4} A	11.2 KΩ	4.35×10^{-4} Ω-cm^2
	Planar gate	4.43×10^{-4} A	11.3 KΩ	4.39×10^{-4} Ω-cm^2
0.8μm	All gate	4.37×10^{-4} A	12.5 KΩ	4.11×10^{-4} Ω-cm^2
	Trench gate	3.73×10^{-4} A	14.5 KΩ	4.75×10^{-4} Ω-cm^2
	Planar gate	3.52×10^{-4} A	14.7 KΩ	4.82×10^{-4} Ω-cm^2
0.6μm	All gate	4.21×10^{-4} A	14.5 KΩ	3.75×10^{-4} Ω-cm^2
	Trench gate	3.70×10^{-4} A	15.5 KΩ	4.01×10^{-4} Ω-cm^2
	Planar gate	3.70×10^{-4} A	15.5 KΩ	4.01×10^{-4} Ω-cm^2

The data listed in the Table 4.3 show that for each fixed column width, the specific On-resistance of the all gate device is lower and has higher saturation current as compared to the devices with trench and planar gates. This is because for the devices with breakdown rating of 120V, the channel resistance occupies a comparatively big portion of the total resistance. All gate structure devices have four channels, which reduces the channel resistance and hence the total resistance decreases. For the planar and trench gate devices, the one and three channels present higher resistance as compared to all gate structures devices.

From the data in Table 4.3, as column width decreases, the specific On-resistance shows an increasing trend and saturation current shows a decreasing trend. It is expected that the specific On - resistance should increase with decreasing n column width because of higher n column concentration used. However on the other side, for narrower column width devices, in order to sustain the same breakdown voltage, larger drift length is needed. These two effects make the drift region resistance to

increase finally. So, narrower column devices show the poor performance compared with wider column width devices.

The performance data of the all gate devices with three different column widths are compared with the 'silicon limit' and ideal superjunction performance lines, which is shown in Fig. 4.19.

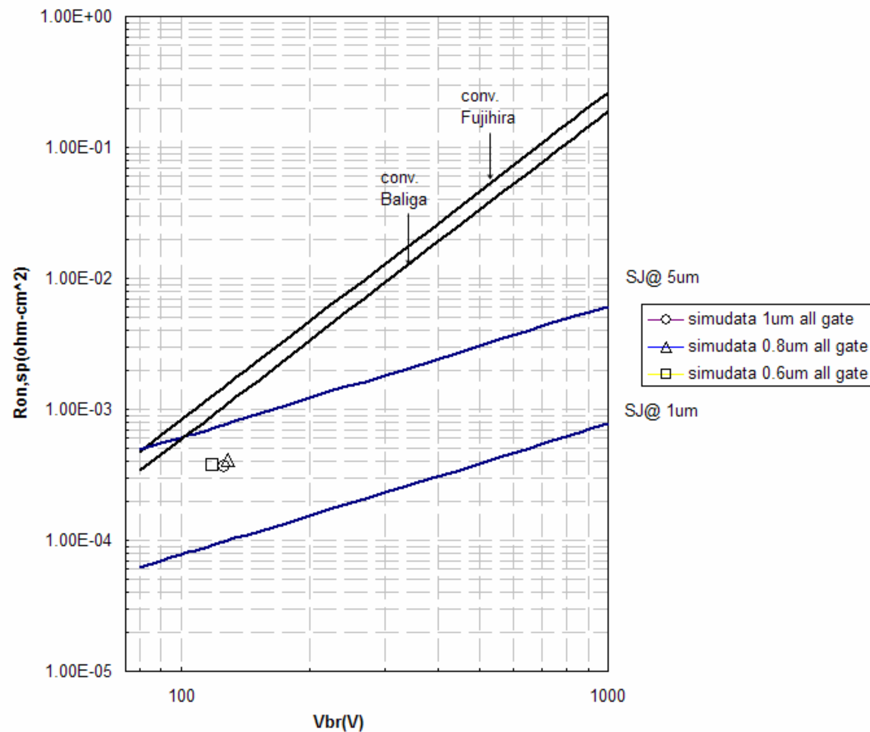


Fig. 4.19 The performance data of the all gate devices with different n column width 0.6μm, 0.8μm and 1μm compared with the conventional silicon limit lines and ideal SJ device lines at 5μm and 1μm. The two SJ lines are calculated by equation (2.21).

Fig. 4.19 shows all the simulated data are below the conventional device lines. This indicates that the device performance is much better than the conventional device. This is due to the superjunction structure used in the drift region and all gate structure used in the gate region. Compared with the superjunction lines, the simulated data are several times higher than the derived data when column width is 1μm. The big difference is due to the derived superjunction equation is for vertical superjunction

device. The current spreading effect in the lateral device, which will cause higher resistance, wasn't considered in the derivation.

4.5 Summary

In this chapter, firstly the partial SOI SJ LDMOS device structure, operation theory and possible process flow are discussed in detail. Then, the gate structure variations and the benefit of each gate structure are provided. Finally, the detailed simulation process and simulation results are provided. The simulation includes all the possible structure variations such as p,n column variation and gate structure variation. The results show that the device performance has broken the "silicon limit" and the "all gate" structure with minimum n column width can achieve the best performance result.

Chapter 5

Development of detailed process flow

Chapter 4 has given the detailed simulation information of the device. The simulation indicates that the device has superior performance compared with conventional device. Further, the proposed major process steps are expected to get good fabrication result. However, more detailed information is needed to guide the fabrication. In this chapter, the detailed process flow is described. The 3-D device structure figures are used to illustrate the fabrication process.

5.1 Practical process requirement

The technology limitations are different from one company to another. This requires us to do the investigation before process simulation. Only by knowing the technology limitations, we won't give wrong process parameters. The device is intended to be fabricated in IME, Singapore. The technology requirements are described as follows.

For the partial SOI formation process, the minimum achievable line width is 0.6μm. So, we can't expect to fabricate device with column width smaller than 0.6μm. When doing the optimization by reducing column width in the simulation, the column width can only be reduced to 0.6μm.

When doing the implantation, the maximum energy can be used is 250Kev. In the extreme case, the energy can be used is 280Kev. This constraint indicates that very deep p-body can't be fabricated in the practical case.

When doing the tilt implantation, the available implantation angles are 7° and 11°. The tilt implantation is needed to form the p, n columns. In the simulation, according

to the implantation angles, the proper implantation dose and energy should be given to get the desired p, n column concentration.

5.2 Detailed process flow for all gate structure

The all gate structure or multi-gate structure is the most sophisticated structure. The fabrication process for this structure is the most difficult one. Therefore, the detailed process flow for the fabrication of Multi-gate Partial SOI SJ LDMOS is described in the following. For better understanding, the process flow is divided into three parts. The three parts are: (1) partial SOI formation process (2) p, n columns formation process (3) multi-gate formation process. The three parts will be described separately with figure illustrations.

The partial SOI formation process is illustrated in Fig. 5.1(a-k). Fig. 5.1(a) demonstrates the starting wafer required for the formation of proposed device. The wafer substrate can be either lightly n doped or p doped. For both cases, doping concentration should be no higher than 1E17 cm^{-3}. It is expected to have the substrate concentration as low as possible. For p type substrate, this is easy to understand because n drift is formed by counter doping the substrate. For n type substrate, due to long thermal cycles needed in the process, high substrate concentration leads to non-uniform doping distribution. So, the initial high concentration is not helpful in the n drift formation. This is also the reason that bulk wafer instead of epi-wafer is used in the device formation. The substrate thickness is required to be more than 7 μm.

After the wafer is ready, a series of oxide and nitride deposition is performed in the wafer surface to form the oxide/nitride/oxide structure. Fig. 5.1(b) shows an initial oxide of 50nm is gown on the wafer surface followed by 5000 Å oxide deposition by LPCVD. Fig. 5.1(c) shows a 1500 Å nitride layer deposited in the oxide layer formed

in Fig. 5.1(b). In Fig. 5.1(d), by adding another 4000 Å oxide layer above the nitride, the oxide/nitride/oxide structure is formed.

In Fig. 5.1(e), the PSOI mask is applied and the oxide/nitride/oxide structure is etched according to the mask dimension. In designing of PSOI mask, several factors needed to be considered. First, the trench width variations should be considered to split the process steps. The real PSOI trench width is related to the trench width in Fig. 5.1(e), the thickness of sidewall Oxide layer grown in Fig. 5.1(g) and the thickness of sidewall Nitride layer deposited in Fig. 5.1(i). The dimensions of the trench part and non-trench part in the mask should follow certain relationship to make sure the thermal oxidation in Fig. 5.1(k) is performed properly.

According to the trench dimension defined by the oxide/nitride/oxide structure, a shallow trench of 1.9μm is etched in the silicon substrate, shown in Fig 5.1(f). P drift region will be formed inside the trench and trench sidewall silicon will be formed as n drift. The trench depth is roughly equal to the height of the p, n drift region. Considering the oxide encroachment from the bottom of the trench during thermal oxide growth shown in Fig. 5.1(k), the trench depth should be a little bigger than the height of p, n column.

Fig. 5.1(g) shows a thin layer of oxide 60 Å grown along the shallow trench. The thin oxide layer serves as pad oxide for the deposited nitride layer of 1000 Å in Fig. 5.1(h). Fig. 5.1(h) shows a nitride/oxide/nitride/oxide structure above the silicon around trench and nitride/oxide structure inside the trench. In Fig. 5.1(i), through anisotropic nitride and oxide etch the top two layers of nitride and oxide at the wafer surface are removed. Above the silicon around trench, only two layers of nitride and oxide left. Inside the trench, the original two layers nitride and oxide are removed, silicon surface is exposed. Most importantly, two layers of oxide and nitride are left in the

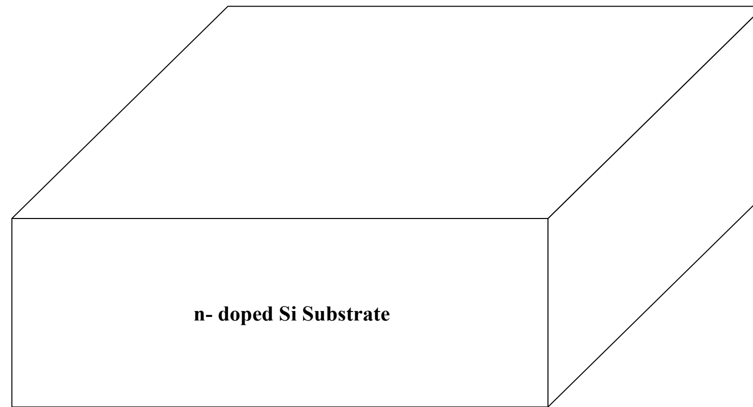
trench sidewall. The structure shows wafer surface around trench and trench side wall are protected by the oxide/ nitride structure. Only the trench bottom is exposed for further process.

In Fig. 5.1(j), a deep trench of 4.2 μm is etched along the shallow trench sidewall. The deep trench is etched to form the multiple silicon trench structure. From Fig. 5.1(j), it is clear that except the deep trench bottom and sidewall, other parts of the wafer surface are protected by the oxide/nitride structure. The structure is ready for thermal oxidation.

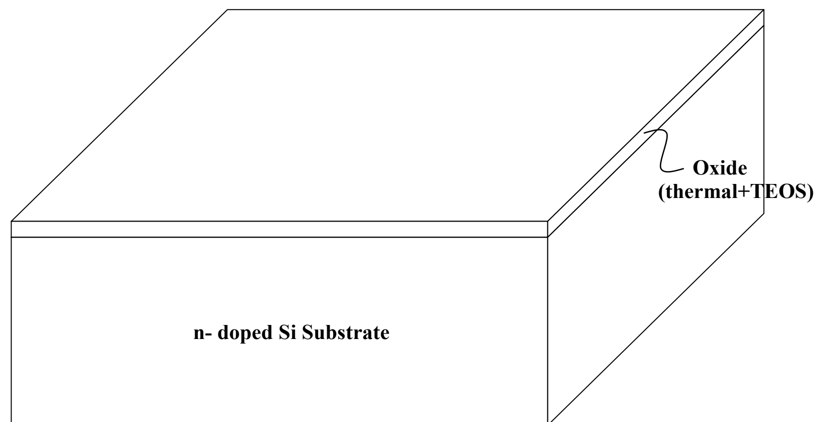
Fig. 5.1(k) shows the structure after thermal oxidation. In the real situation, the oxide profile is not rectangular. At the edge part, the oxide profile is round. The multiple silicon trench width and the width of the silicon between two adjacent trenches should follow the oxidation ratio to ensure that the oxide can pinch off in the middle silicon part. The deep trench width and middle silicon width are decided by the PSOI trench mask in Fig. 5.1(e) together with the shallow trench side wall oxide, nitride thickness. So, when PSOI mask is designed in Fig. 5.1(e), the thermal oxidation must be considered. During the step of PSOI growth in Fig. 5.1(k), Oxide must be guaranteed to entirely fill the PSOI region. That is, there is neither Silicon nor air hole left in PSOI region after Oxidation. Based on the process simulation, real fabrication on this part will find out the desired parameters for PSOI growth.

The figures from Fig. 5.1(a) to Fig. 5.1(k) show the PSOI formation process. Though these steps, the buried oxide platform is formed. Above this oxide platform, the drift region of the device, i.e. superjunction part will be formed and shown in the following figures. Fig. 5.1(a) to Fig. 5.1(k) provides an economic way to fabricate the buried oxide at desired thickness and desired position in the device structure. This is because the buried oxide thickness and position are only decided by the trench thickness and

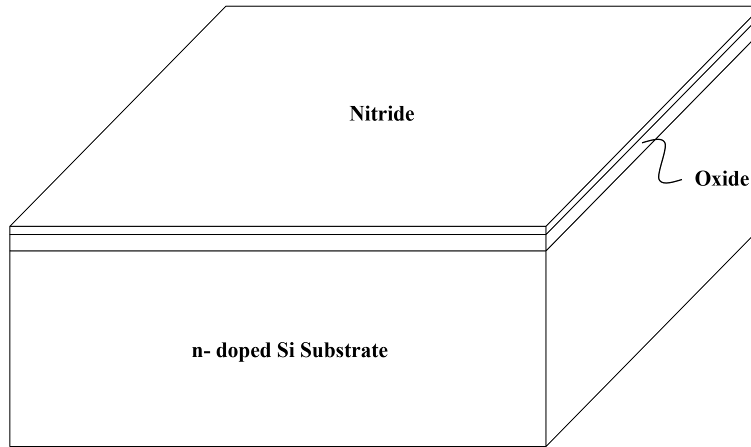
position. The multiple silicon trench method to form the buried oxide platform can easily be used in other device fabrication.



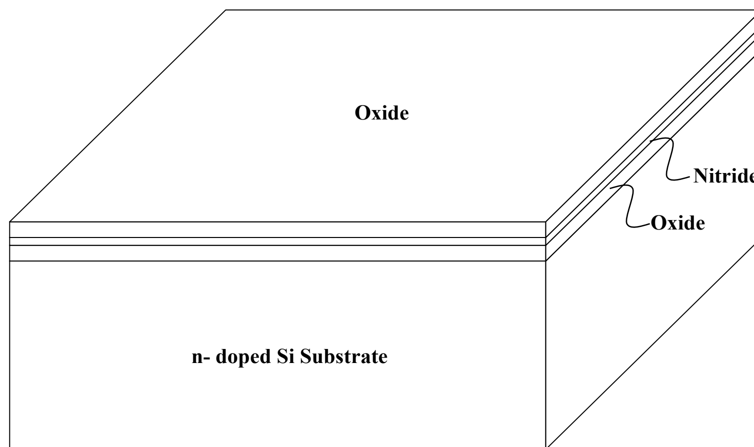
(a) Lot Start
Wafer Pre-treatment



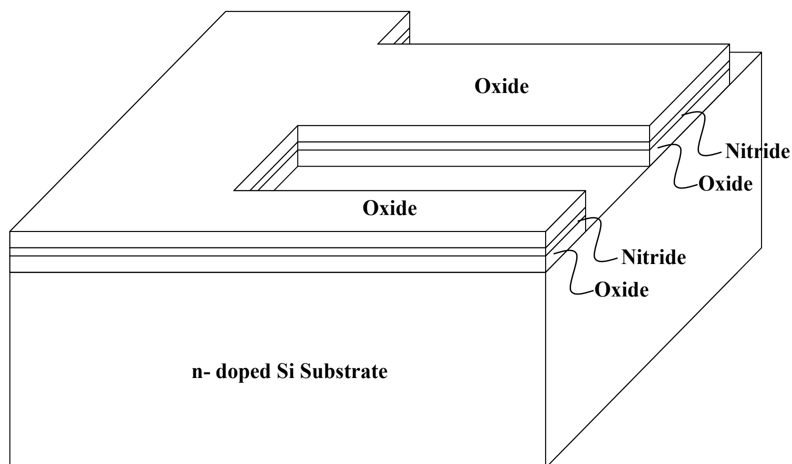
(b) Initial Oxidation 50nm
LPCVD_TEOS (5000 A)



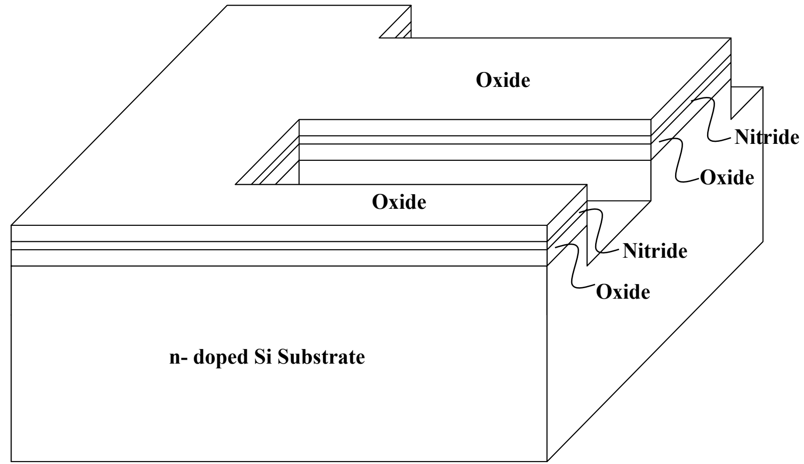
(c) Nitride Deposition (1500 A)



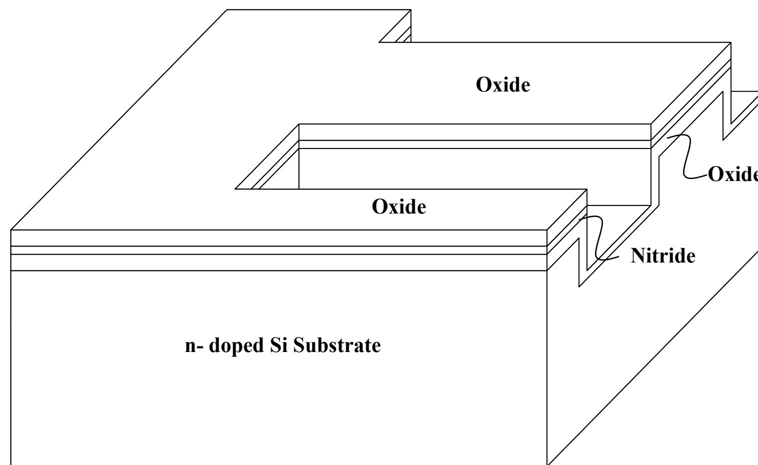
(d) LPCVD 4000A



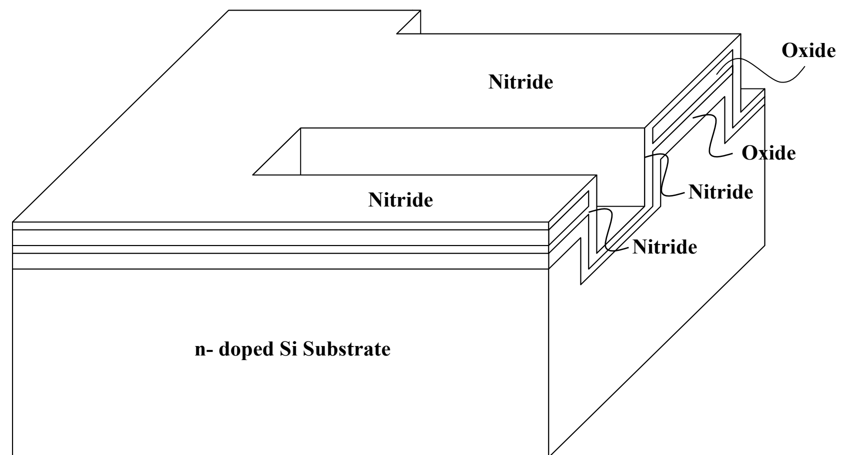
(e) **Mask 1:** Partial SOI trench Mask
Oxide/Nitride/Oxide Etch



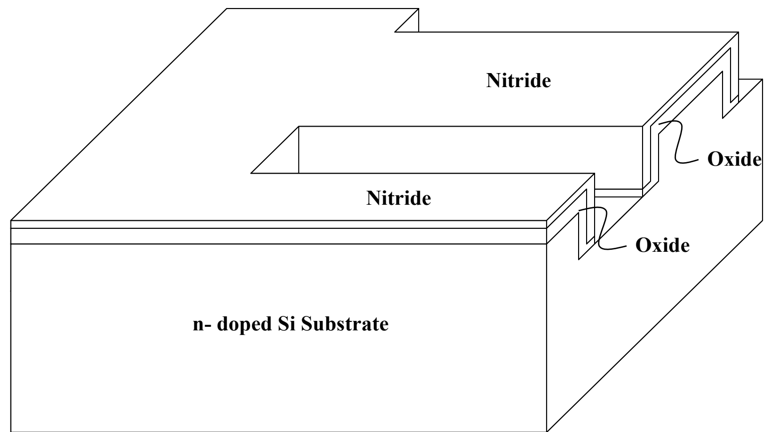
(f) Silicon Trench Etch (STS) 1.9um



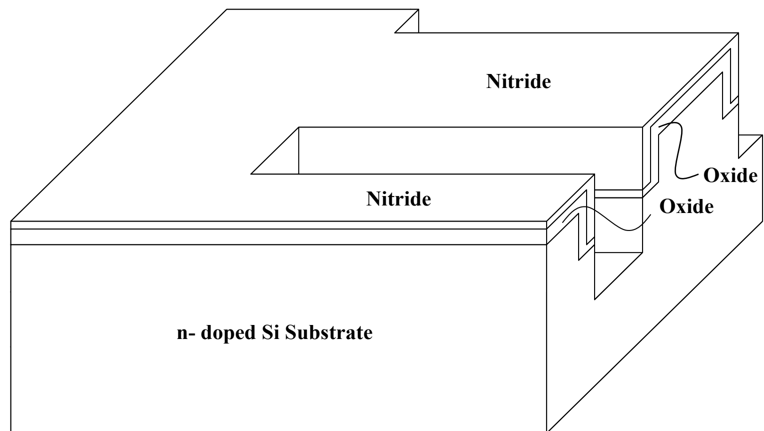
(g) Dry Oxidation 60A (Liner)



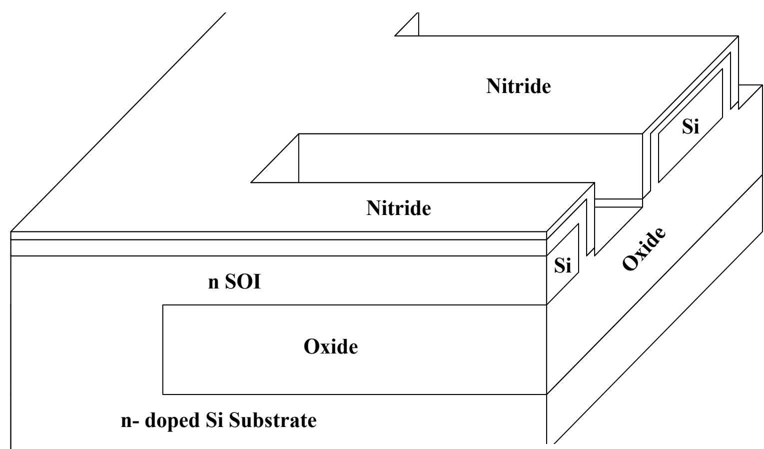
(h)Nitride Deposition_ 1000 A



(i) Anisotropic Vertical Nitride/Oxide Etch
(Remove the surface Nitride & Oxide only, to keep the sidewall Nitride & Oxide)



(j)Deep Silicon Trench Etch (4.2 um)



(k)Thermal P-SOI Growth
(The profile for P-SOI is round at the edges in real case)

Fig. 5.1 Partial SOI formation process

The PSOI formation process needs long thermal cycles. If an epitaxial wafer with the desired concentration is used in the beginning, the doping profile of the epi-layer

through long thermal cycles becomes very non-uniform. This non-uniform profile will greatly affect the superjunction performance. Therefore, in this device, low concentration bulk silicon wafer is used as the starting wafer. The doping profiles of p, n drift region are formed by dopant implantation and drive-in process. The p, n columns formation process is shown in Fig. 5.2.

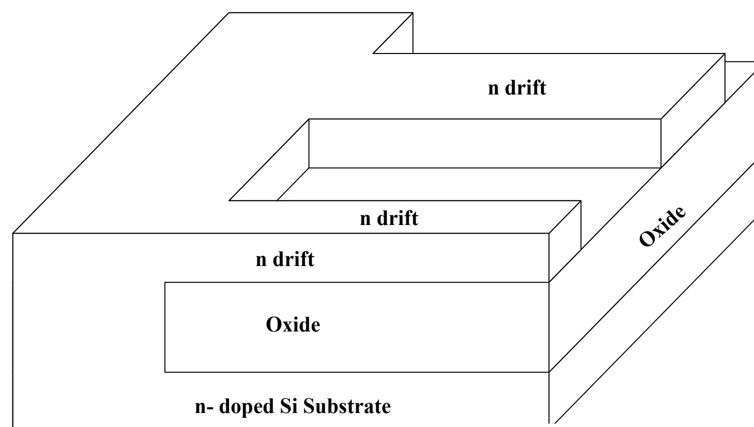
In Fig. 5.2(a), the protective nitride and oxide layer in the wafer surface is removed by global nitride and oxide removal. Then, the phosphorus tilt implantation is performed. The silicon part between the two adjacent shallow trenches will be formed as n drift region. Tilt implantation is used to ensure the shallow trench sidewall receive the dopant. This is helpful to get the uniform dopant distribution in the n drift region. After phosphorus tilt implantation, the drive-in process is not performed immediately. The drive-in process of n drift region will be performed together with the drive-in process of p drift region later.

In Fig. 5.2(b), a thin oxide layer of 500 Å is grown on the wafer surface. The thin oxide layer is aimed to prevent dopant interdiffusion between p, n column during various thermal cycles. In Fig. 5.2(c), an oxide removal mask is used to remove the oxide layer outside the drift region. The oxide removal mask is carefully designed to remove the oxide at the gate side. A small encroachment in the drift region is needed to remove sidewall oxide which is along the gate side. The p-body will be formed at the gate side and the p-drift will be formed in the trench. If the sidewall oxide along the gate side is not removed totally, the contact between p drift and p-body will be affected. This will influence the lateral depletion action between p, n column. With the sidewall oxide between p, n column, to ensure the proper depletion of p, n column, the p-drift must be electrically contacted with the source through p-body and the n-drift must be electrically contacted to the drain. On the other hand, in designing the

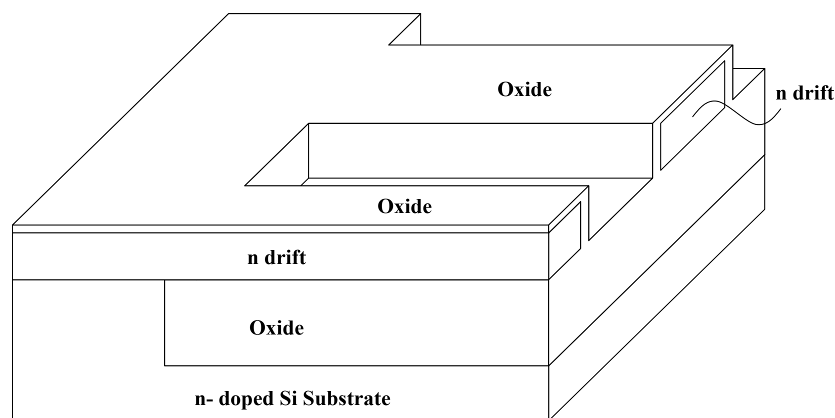
oxide removal mask, the encroachment in the drift side can't be too much. This is because in the area without oxide barrier, the dopant interdiffusion between p, n column is very serious. This may result in the degradation of superjunction structure on blocking voltage. Therefore, some variations in the mask layout design are helpful to judge the final device performance affected by this step.

After the process steps shown in Fig. 5.2(b) and Fig. 5.2(c), the n drift region is completely protected by the thin oxide layer. Fig. 5.2(d) shows a thin layer of polysilicon deposited on wafer surface followed by boron tilt implantation. In Fig. 5.2(e), another layer of polysilicon is deposited to fill up the trench. In Fig. 5.2(f), an oxide layer of 5000 Å is deposited on the polysilicon layer followed by drive-in process. The steps from Fig. 5.2(d) to Fig. 5.2(f) are aimed to form uniform doping profile in p column. The oxide layer above the polysilicon is to prevent dopant out-diffusion. The polysilicon layer is deposited by two steps. First deposition a thin layer and doing the implantation, then depositing another layer can make the dopant diffuse from the inside of polysilicon layer. This is helpful for the uniform dopant distribution of p column. The drive-in process is not only for the boron diffusion in the p column, also for the phosphorus diffusion in the n column. Previously in Fig. 5.2(a), only phosphorus implantation is performed without the drive-in process. Now in Fig. 5.2(f), the p, n column drive-in process is performed together. Fig. 5.2(f) shows that the thin oxide layer between n-drift and p-poly effectively prevents the dopant interdiffusion between them during the drive-in process. To get the desired the doping concentration in p, n column, the phosphorus and boron tilt implantation dose and angle should be carefully designed. The drive-in time should be designed long enough for the dopant uniform distribution in the p, n column.

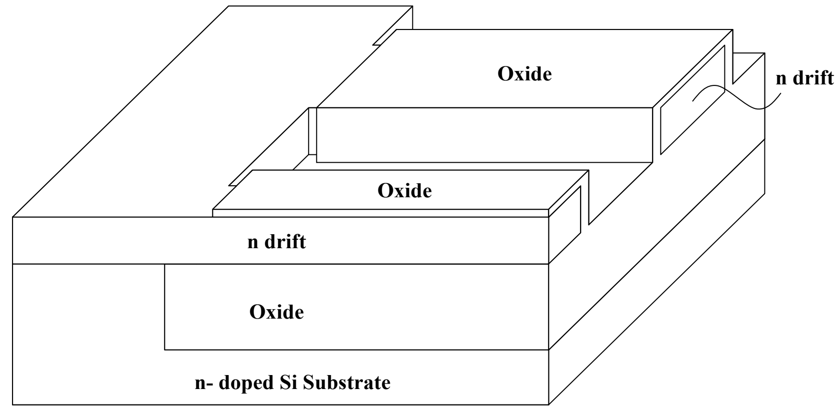
In Fig. 5.2(g), the deposited oxide layer is removed. The polysilicon layer is etched back for planarization. In Fig. 5.2(h), a field mask is added and the thin oxide layer above the n-drift region is removed. Only the thin sidewall oxide layer between p, n column is left. In Fig. 5.2(f), the thin oxide layer at the top of n-drift is needed because the deposited p-poly surrounds the n-drift. Now the p-poly is at the side of n-drift. The sidewall oxide layer is enough to prevent the interdiffusion between p, n drift during following thermal cycles.



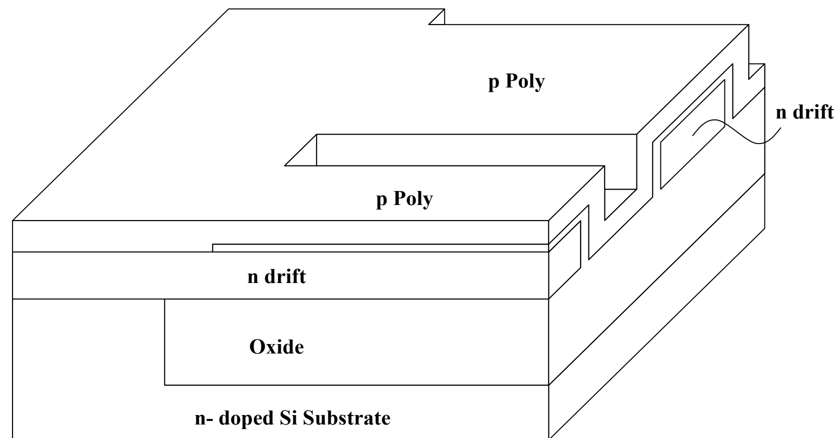
(a) Global Nitride & Oxide Removal
Phosphorus tilt implant



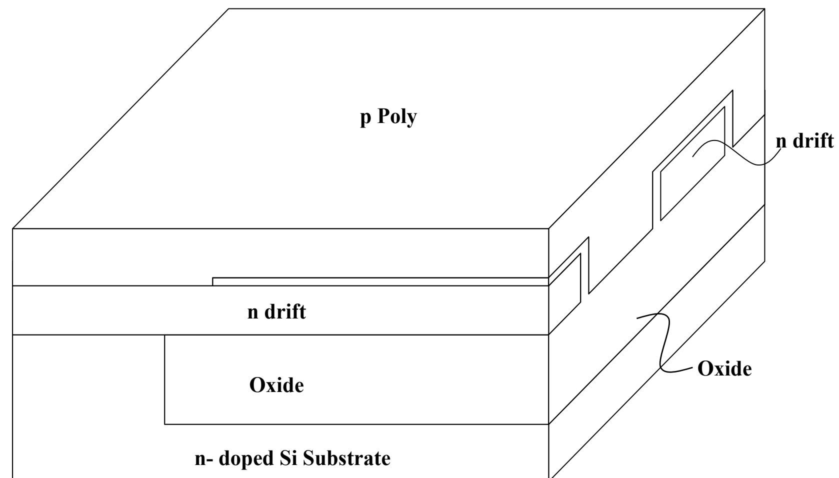
(b)Sidewall Oxide Growth 500A



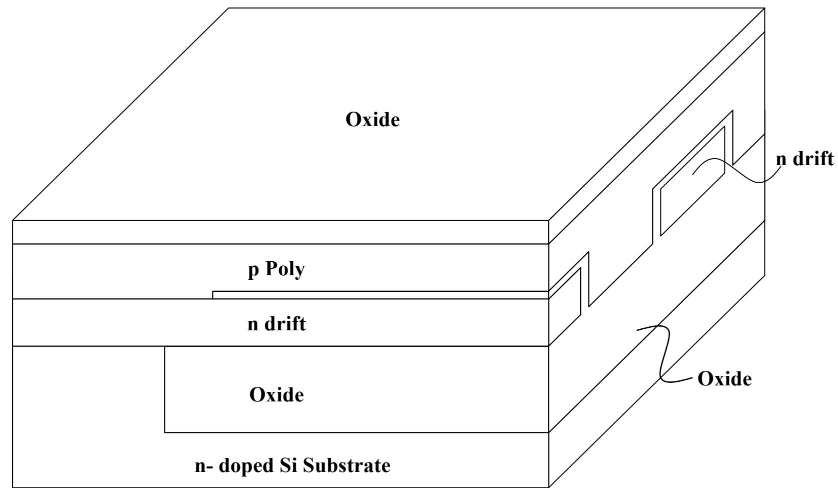
(c) **Mask 2:** Oxide Removal Mask
Corner Sidewall Etch



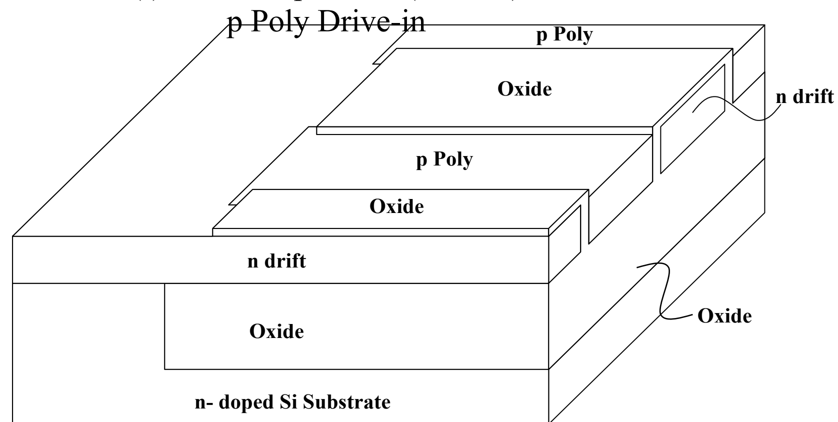
(d)Conformal Poly-Si Deposition
Boron Poly-Si Implant (tilted angle = $\pm 11^0$)



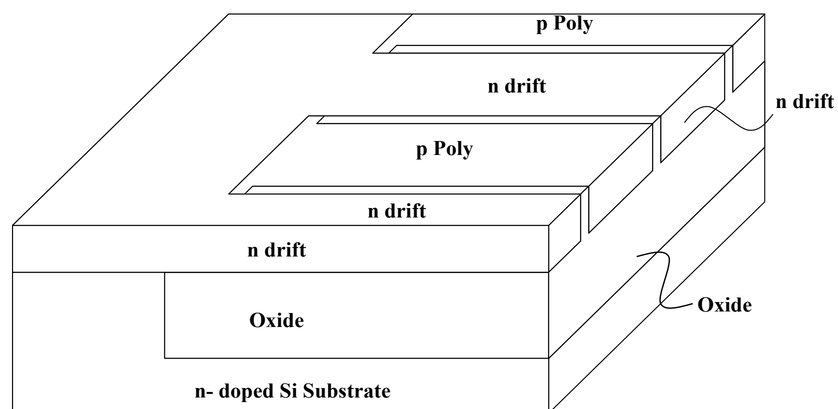
(e) Poly-Si Deposition



(f) Oxide Deposition (5000 A)
p Poly Drive-in



(g)Oxide Etch
Poly Etch back for Planarization



(h)**Mask 3:** Field Mask
Oxide Removal

Fig. 5.2 P, n column formation process

Fig. 5.2 shows the process steps of p, n column formation. In the following, the detail process sequences for multi-Gate structure formation are illustrated in Fig. 5.3.

For planar gate device and trench gate device, the partial SOI and p, n column formation process are all the same with multi-gate structure. That means the process steps shown in Figs. 5.1 and 5.2 are also applicable for planar gate and trench device. The different part in process steps for the three kinds of gate structures lies in the gate formation process. The most complicated gate formation process is for multi-gate formation. For planar gate and trench gate formation, the process steps can totally follow the conventional DMOS or UMOS formation process. For the multi-gate formation process, there is a little difference. Multi-gate formation process is a bit like UMOS formation process. The p-body is formed first followed by gate formation. P-body implantation and drive-in is shown in Fig. 5.3(a-b). In the lateral direction, it is required that the p-body is wider enough to touch p-poly. This makes p-body and p-column are electrical contacted. In the vertical direction, p-body is required to be deep enough to touch the PSOI oxide. If there is a gap between the p-body and PSOI oxide, at Off-state, the gap is hard to deplete. This will affect the breakdown voltage. Fig. 5.3(c) presents the device structure after Gate trench etching. Trench depth and trench width can vary according to later Silicon release etching. Normally, trench depth can be nearly equal to the thickness of Superjunction structure. The length of Gate trench is equal to the p column width of SJ structure. The Gate trench is aligned with p drift. The cross-section view cutting along AA' and BB' shown in Fig. 5.3(d). The distance between the edge of Gate trench and the left side of SJ p column is no less than 0.6 μm and large enough for Silicon release etching. It must guarantee that after Silicon release etching, there is at least a 0.2μm~0.3μm gap between Gate trench and PSOI to keep the electrical connection around Gate region, as shown in Fig. 5.3(k). The cross-section cutting along BB' shows the electrical contact way between p-body and p column.

Fig. 5.3(e) and Fig. 5.3(g) show the process steps needed for the sidewall protection during silicon release etching. Fig. 5.3(e) shows the 500 Å sacrificial oxide growth and removal followed by 400Å dry oxidation. The cross-section view after dry oxidation is shown in Fig. 5.3(f). Fig. 5.3(g) shows 500Å nitride deposition. The cross-section view after nitride deposition is shown in Fig. 5.3(h). After overall anisotropic nitride and oxide etching as in Fig. 5.3(i), only the sidewall nitride and oxide layers remain, as in the cross section view of Fig. 5.3(j).

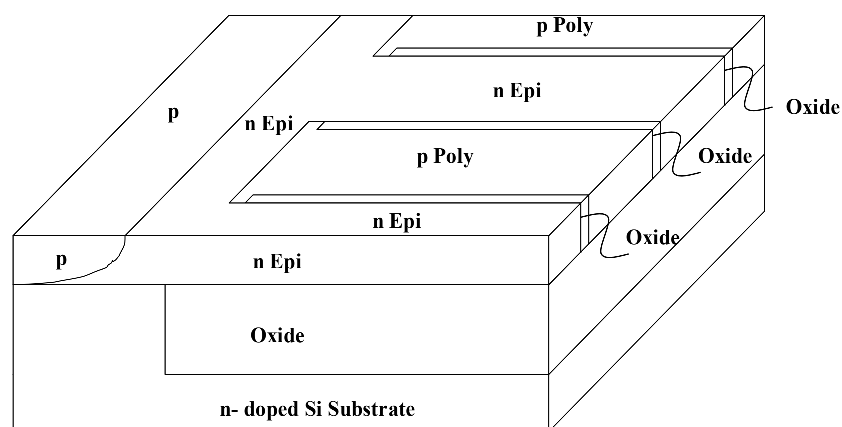
Fig. 5.3(k) shows the cross section view of the device after Silicon release etching. An entirely big Silicon cavity is formed underneath the Gate trench regions and beside the PSOI region. The size of the silicon cavity can be accurately controlled in real fabrication process by the recipe and etching time. It is expected that top boundary of the cavity is inside the p-body to ensure the bottom channel form properly.

Fig. 5.3(l) shows the device structure after the sidewall oxide and nitride removal. The cross-section view is shown in Fig. 5.3(m). In Fig. 5.3(n), the 400Å dry oxidation is performed at the entire exposed silicon surface to form gate oxide. The cross-section of Fig. 5.3(o) shows the gate oxide layer covers the exposed silicon surface including the inner surface of silicon cavity. Afterwards, Gate Poly-Si deposition is carried out to fill the silicon cavity and cover the thin oxide layer everywhere, as shown in Fig. 5.3(p) and Fig. 5.3(q). The Therefore, multiple Gate structure is achieved around the silicon region above the silicon cavity. In Fig. 5.3(q), the cross-section cut along MM' shows the silicon region above the silicon cavity is surrounded by gate oxide and gate poly. During the On-state, four channels will be formed inside the silicon region. One is on the top of the silicon region, the same as the channel in planar gate conventional MOSFET. The other three channels are at the side-walls and bottom of the silicon region. In the multi-gate structure device, the channel density is increased to four

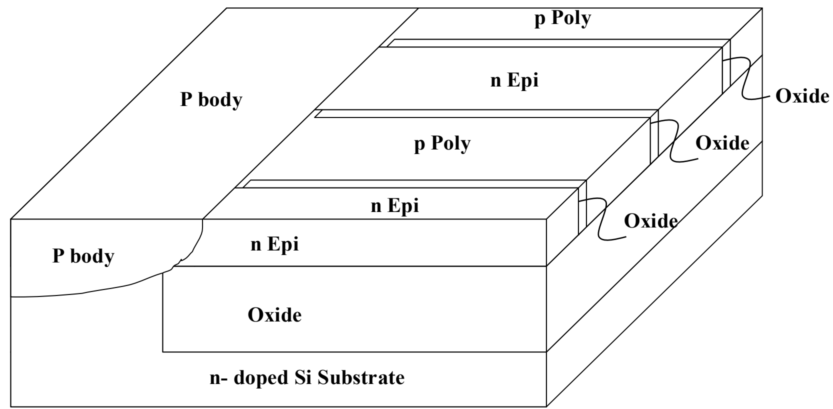
times of that in planar gate convention MOSFET. It is expected that the channel resistance is reduced in the new structure.

In Fig. 5.3(r), Gate Mask (Mask 6) defines the Gate region for Gate Poly-Si etching. So far the key parts of this invention including PSOI, Superjunction drift region and multiple Gate trench structures have been accomplished on the proposed device.

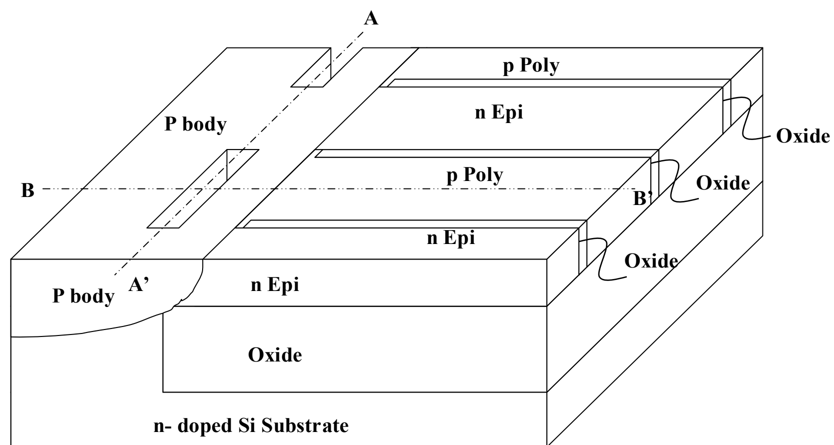
In the following, the source and drain are formed. The process is the same as that conventional MOSFET. The source implantation can also be performed just after p-body drive-in in the beginning. In Fig. 5.3(s), source and drain mask are used for source, drain implantation. P+ is implanted at the source side for the contact between source and p-body. In Fig. 5.3(t), source/drain annealing is performed to activate the dopant. Then, oxide is deposited and densified at the wafer surface. In Fig. 5.3(u), the contact mask is used to etch oxide and expose the silicon surface needed for source and drain electrode contact. AL is deposited on the wafer surface, shown in Fig. 5.3(v. In Fig. 5.3(w), metal mask is used to remove unnecessary AL and leave it only at the source and drain side. Finally, the passivation mask is used to deposit the passivation layer for the protection of the wafer surface.



(a) **Mask 4:** P-body Mask
P-body Implant & Resist Strip

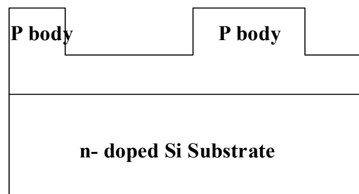


(b) P-body Drive-in

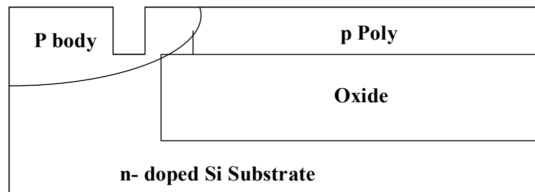


(c) **Mask 5:** All-Gate Trench Mask
Trench Etching & Resist Strip

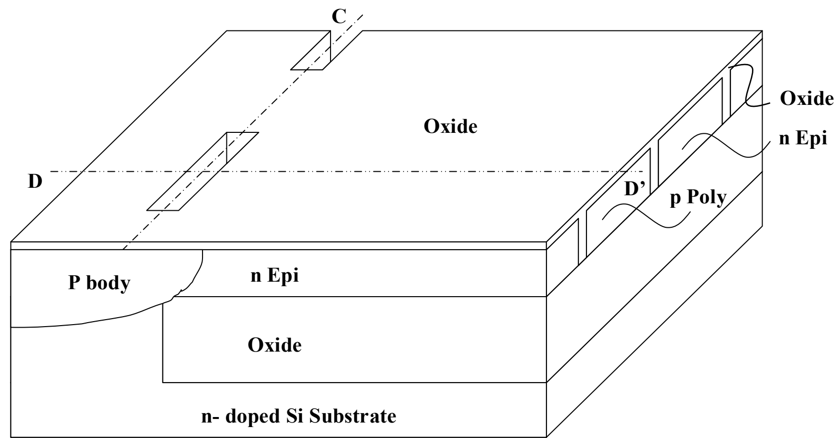
At AA':



At BB':

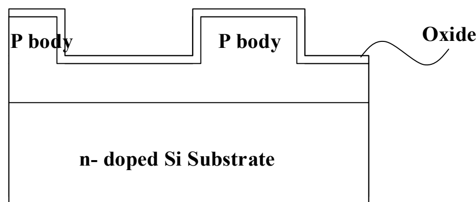


(d) Cross-section view of Fig. 5.3(c)

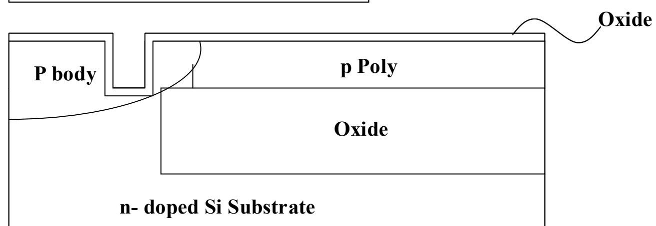


(e) SRO Growth_500A & Cleaning (Wet Etch)
Dry Oxidation (400A)

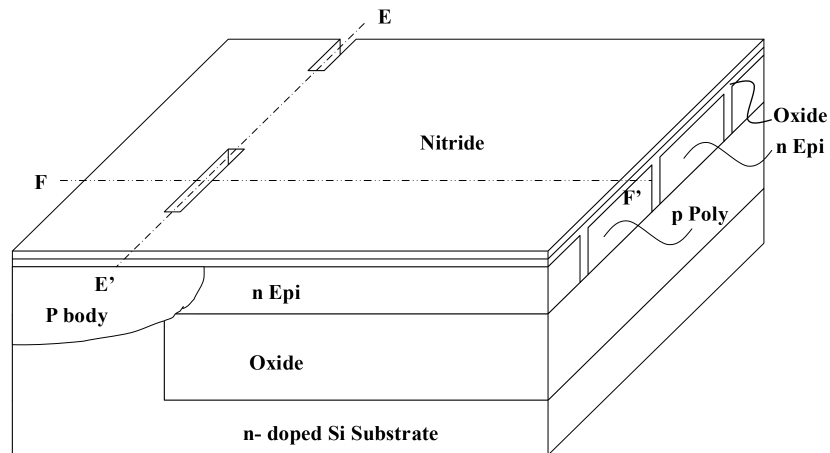
At CC':



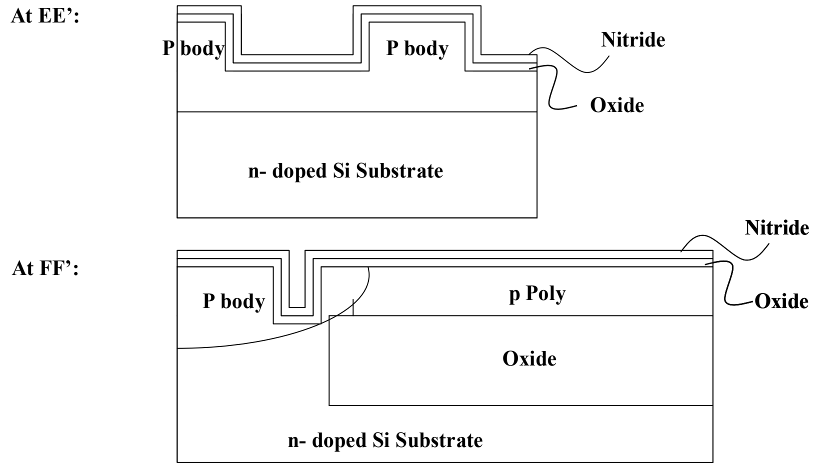
At DD':



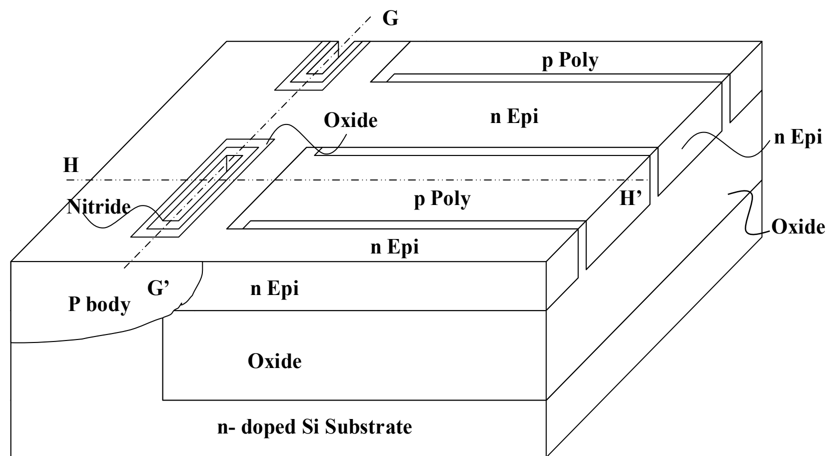
(f) Cross-section view of Fig. 5.3 (e)



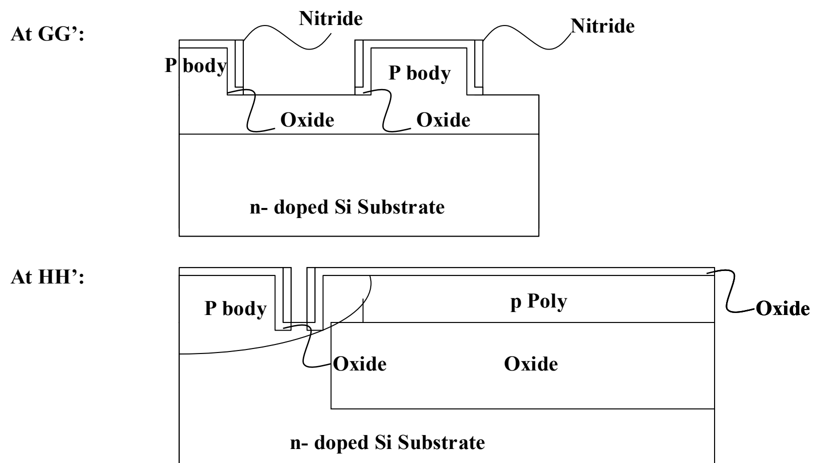
(g) Nitride Deposition_ 500 A



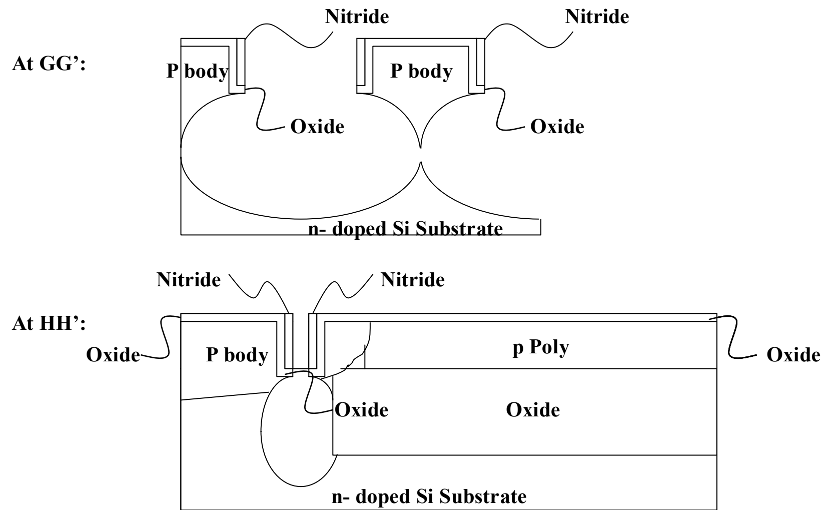
(h) Cross-section view of Fig. 5.3(g)



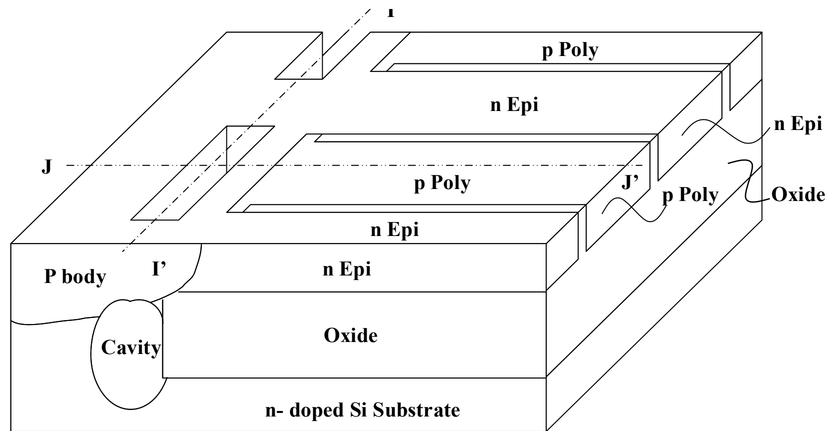
(i) Bottom Nitride & Oxide Removal



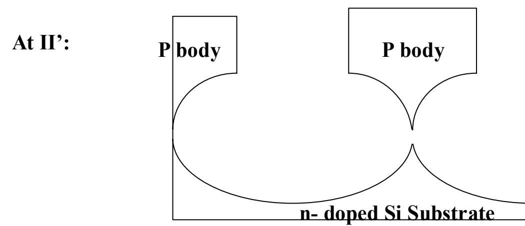
(j) Cross-section view of Fig. 5.3(i)

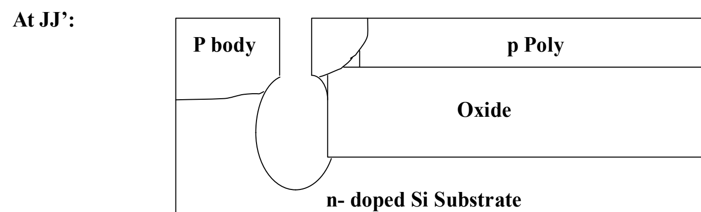


(k) Cross-section view of Fig. 5.3(i) after silicon release etching

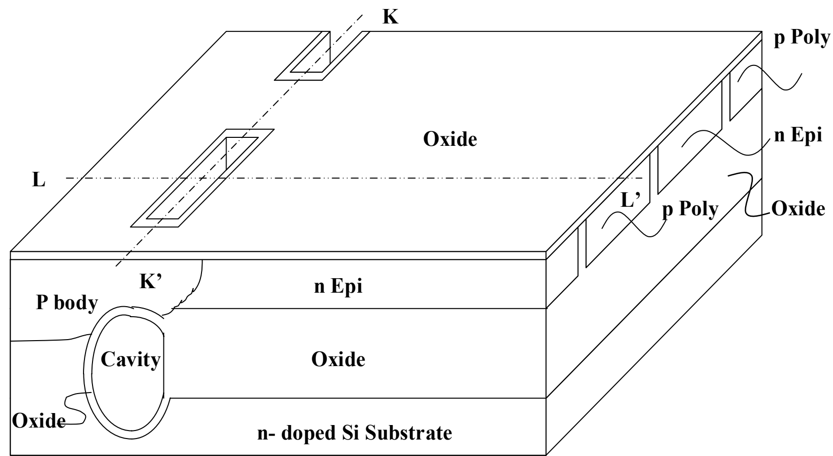


(l) Nitride & Oxide Removal



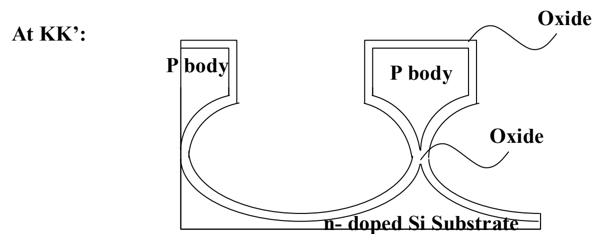


(m) Cross-section view of Fig. 5.3(l)

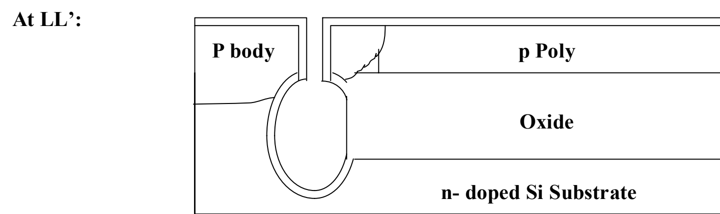


(n) Gate oxidation _400Å

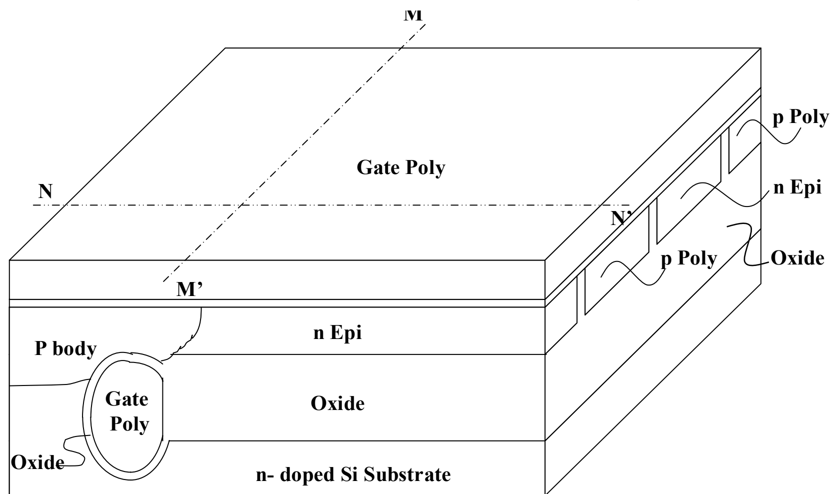
At KK':



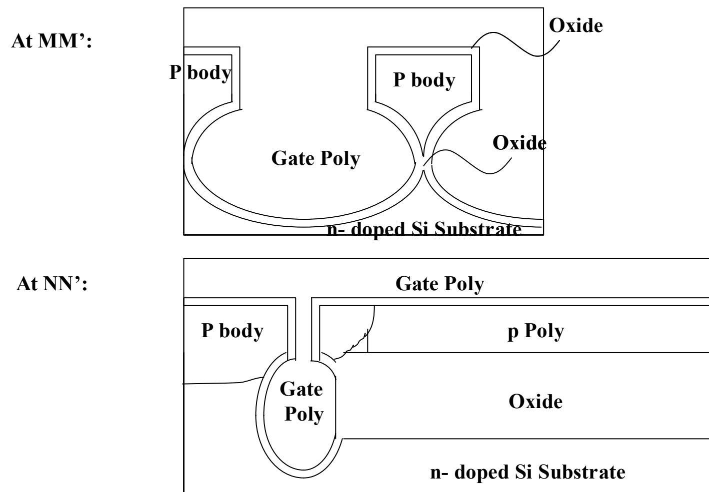
At LL':



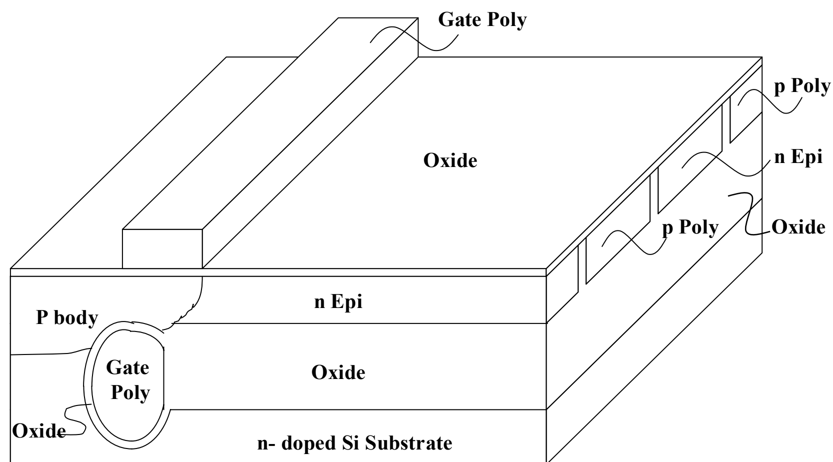
(o) Cross-section view of Fig. 5.3(n)



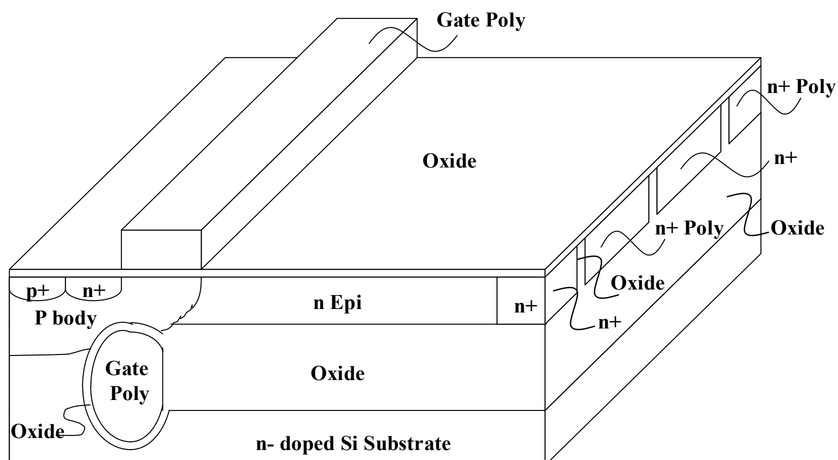
(p) Poly-Si Deposition & Poly-Si Dope



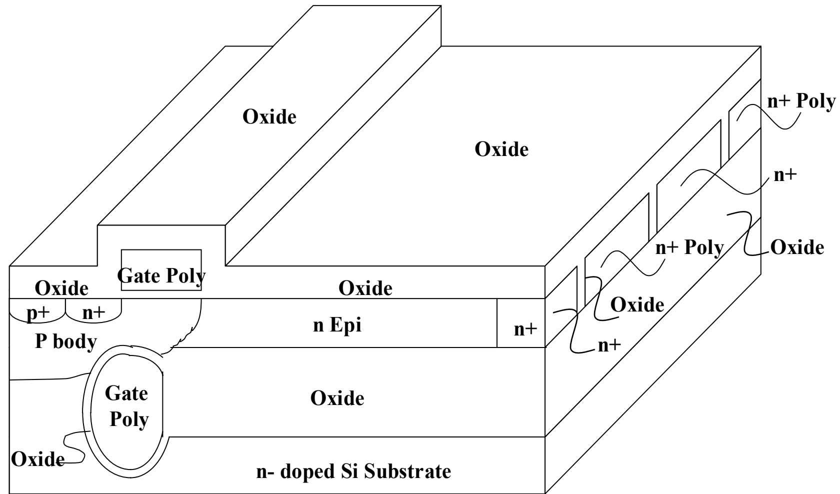
(p) Poly-Si Deposition & Poly-Si Dope



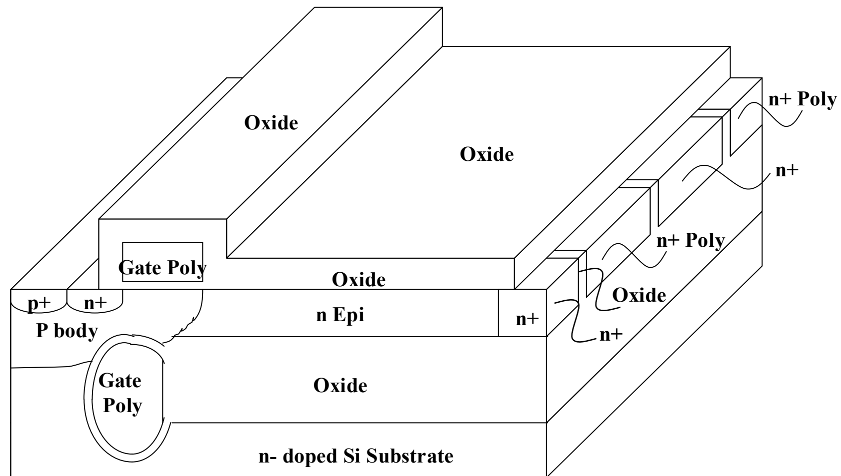
(q) **Mask 6:** Gate Mask
Gate Poly Etch & Resist Strip



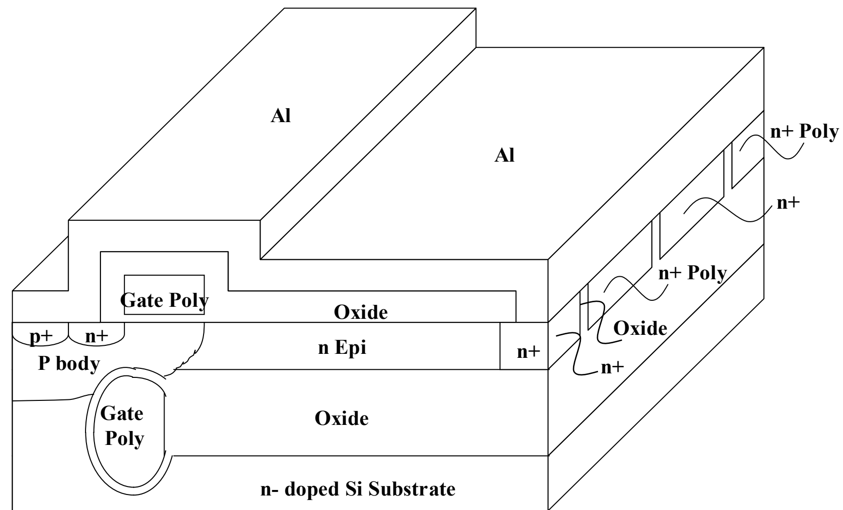
(r) **Mask 7: Source Mask** Source Implant & Resist Strip
Mask 8: Drain Mask Drain Implant & Resist Strip
Mask 9: P+ Imp Mask P+ Implant & Resist Strip



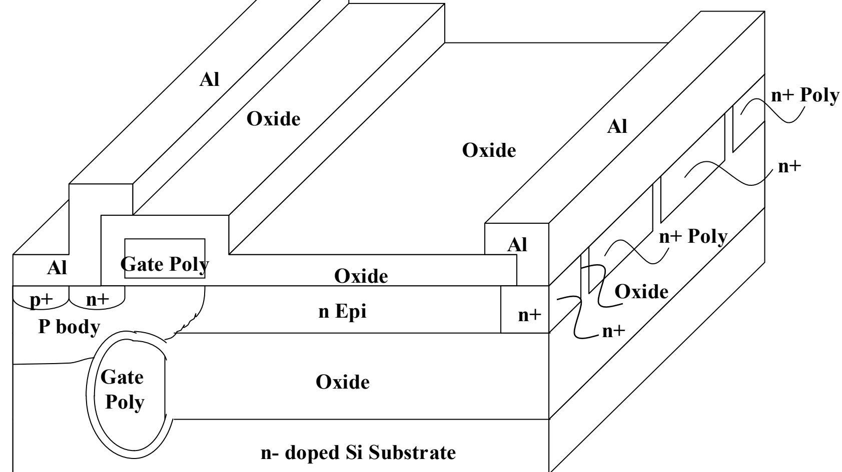
(s) S/D Annealing
Plasma CVD Oxide & BPSG Densification



(t) **Mask 10:** Contact Mask
Contact Slope Etch



(u) Si-AL PVD Deposition



(v) **Mask 11:** Metal Mask
Dry Etch & Resist Strip & Alloy

Fig. 5.3 Multi-gate formation process

5.3 Summary

This chapter provides detailed process flow of the partial SOI SJ LDMOS with "all gate" structure. The process flow is intended to be used for device fabrication in IME. This chapter starts with the discussion of fabrication condition limitations in IME. Then, the practical process flow is provided with detailed illustrations and explanations

Chapter 6

Conclusion

In this thesis, the research work is divided into two parts. One part is to study the influence of interdiffusion problem on superjunction device performance. The practical superjunction performance curves and equations are arrived based on extensive simulation work. The other part is to simulate the partial SOI superjunction LDMOS structures of three gate variants. The simulation work has proven that the device performance can break the silicon limit. The contents of each chapter are described in the following.

The superjunction theory is analyzed in chapter 2. The superjunction structure is to replace the conventional monotonically n- drift region to n-drift and p-drift alternatively stacked region. The inserted p-drift region can help the depletion of n-drift in the Off-state. So, to achieve the same breakdown voltage, the n-drift concentration can be improved greatly compared with conventional concentration. Although the current conduction area in On-state is reduced to half, the n column concentration can be improved to one order high and the on-resistance is reduced to approximately 5 times lower. The first order superjunction equation is derived to compare with the conventional equation. The relationship between specific on-resistance and breakdown voltage is reduced from over square for conventional devices to almost linear for superjunction devices. Although the concept is very attractive, its realization is not easy. Most fabricated superjunction devices are vertical

devices with relatively high voltage. For lateral superjunction devices, the research is still on the theoretical stage.

Chapter 3 summarized the investigation work on the practical superjunction device performance under given thermal cycles. Since the interdiffusion problem is unavoidable in superjunction device fabrication process, it is necessary to study its influence on the superjunction device performance. The practical superjunction performance lines under given process thermal cycles are arrived on the basis of simulation results. The practical concentration equation and superjunction equation are also derived based on the simulation results. These equations and curves can give guidance in the superjunction device design.

The detailed simulation of partial SOI superjunction LDMOS is summarized in chapter 4.

The partial SOI superjunction LDMOS combines the benefit of both superjunction device and partial SOI technology. In this chapter, firstly, the partial SOI technology is reviewed. Then, the device structure, operation and process flow are discussed. Finally the simulation method and results are discussed in detail. The on-state simulation results show that the all gate structure has the best on-state performance. Comparing simulation data of all gate devices with conventional and superjunction value, the device performance is much better than the conventional device but worse than the derived superjunction value. It's normal for the simulation value worse than the derived value because the derivation is only first order without the consideration of many effects. The comparison shows that the device performance can break the conventional silicon limit with the use of superjunction structure and all gate structure.

Chapter 5 is to give the detailed process flow for the all gate (multi-gate) partial SOI superjunction LDMOS with the consideration of practical process requirement. 3-D process figures are given with detailed description.

Due to the time constraint, the partial SOI superjunction LDMOS device has not been fabricated. The fabrication work can be done in the future.

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Appendix A

Drift length calculation of conventional device

The drift region depth of conventional vertical MOSFET device to sustain a certain breakdown voltage is derived thereafter. For one sided abrupt p, n junction, the depletion width in the lightly doped p side W_d and the maximum electrical field E_m in the p, n junction position are given by [2]

$$W_d = \sqrt{\frac{2\varepsilon_s V_{br}}{qN_A}}$$

(A.1)

$$E_m = \frac{qN_A}{\varepsilon_s} W_d$$

(A.2)

where V_{br} is the breakdown voltage; N_A is the doping concentration in the p side.

Eliminate concentration N_A from equations (A.1) and (A.2); the depletion width W_d is given by

$$W_d = \frac{2}{E_m} V_{br}$$

(A.3)

When breakdown occurs, the maximum electrical field E_m equals to the critical electrical field E_c. The critical electrical field is given by

$$E_c = E_0 V_{br}^{-\frac{1}{6}}$$

(A.4)

where $E_0 = 8\times10^5$ V/cm.

Substitute equation (A.4) to equation (A.3), the depletion width at breakdown is given by

$$W_d = \frac{2}{E_0} V_{br}^{\frac{7}{6}}$$

(A.5)

Equation (A.5) can be used to calculate the drift region depth at given breakdown voltage for conventional MOS device. The same equation is used to estimate the drift region depth for the superjunction device with the approximation on equal area relationship. For the same breakdown voltage, the electrical field profiles of superjunction device and conventional device are different in shape. The superjunction one has a rectangular-like shape, while the conventional one is triangle shape. If we put the two profiles (for different drift region doping concentrations) together on the same coordinate system, for most of cases the two curves cover approximately the same area, although not exactly the same under different column width and concentration of superjunction device. However, the approximate relationship is useful here for deriving the on-state specific resistance. Detailed description and analysis are found in reference [49].

Appendix B

P, n column width calculation

Fig. B.1 gives the calculation structure and Table 1 gives the physical meaning of the variables used in calculation.

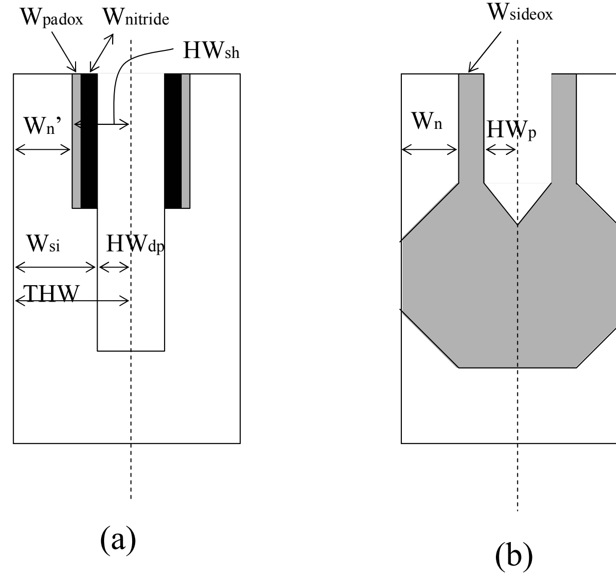

Fig. B.1 Schematic structures for calculation of p, n column width (a) before oxidation (b) after oxidation

Table B.1 Index Table for variables used

W_{padox}	pad oxide thickness	HW_n'	Half width of n column before oxidation
$W_{nitride}$	nitride thickness	HW_n	Half width of n column after oxidation
W_{sideox}	side wall oxide thickness	HW_p	Half width p column
W_{si}	deep trench silicon thickness	HW_{dp}	Half width of deep trench
THW	Half width of total structure	HW_{sh}	Half width of shallow trench

From Fig. B.1(a), following equations are given,

$$HW_n' = THW - HW_{sh} - 0.44 * W_{padox}$$

$$W_{si} = HW_n' + W_{nitride} + W_{padox}$$

$$HW_{dp} = W_{si} * 0.56/0.44$$

$$THW = HW_{dp} + W_{si}$$

From Fig. B.1 (b), following equations are given,

$HW_n = HW_n' - 0.44* W_{sideox}$

$HW_p = THW - HW_n - W_{sideox}$

If the process condition is given, $W_{padox,}$ $W_{nitride}$ and W_{sideox} are fixed. In my process condition, $W_{padox,}$ $W_{nitride}$ and W_{sideox} are respectively 0.0084um,0.05um,0.05um.

If required n column width is 0.8um, HW_n should be 0.4um.

Then, $HW_n' = HW_n + 0.44* W_{sideox}$ =0.4+0.44*0.0084=0.422um

$W_{si} = HW_n' + W_{nitride} + W_{padox}$ =0.422+0.05+0.0084=0.4804um

$HW_{dp} = W_{si}$ *0.56/0.44=0.4804*0.56/0.44= 0.6114um

$THW = HW_{dp} + W_{si}$ =0.6114+0.4804=1.0918um

$HW_p = THW - HW_n - W_{sideox}$ =1.0918-0.4-0.05=0.6418um

$HW_{sh} = HW_{dp} + W_{nitride} + W_{padox}$ =0.6114+0.05+0.0084=0.6698um

$W_p = HW_p$ *2= 0.6418*2=1.2836um

THW and HW_{sh} are needed for process simulation.

P column width W_p is needed for concentration calculation.

Appendix C

List of publication

1. Hanmei Zhong, Yung C Liang, Ganesh S Samudra and Xin Yang, “Practical superjunction MOSFET device performance under given process thermal cycles,” *Semicond. Sci. Technol. 19*, pp.987-996, August 2004.

Appendix D

List of simulation files

3-D all gate structure on-state simulation files for n column width of 1um:

```
TITLE DAVINCI PSOI SJ-LDMOS ON STATE DRAIN CHARACTERISTICS SIMULATION


$MESH IN.FILE=LDMOSZ.spu4 TSUPREM PROFILE
MESH

X.MESH NODE=1  LOCATION=0
X.MESH NODE=7  LOCATION=0.7
X.MESH NODE=12  LOCATION=0.9
X.MESH NODE=30 LOCATION=1.4
X.MESH NODE=33 LOCATION=1.5
X.MESH NODE=35 LOCATION=1.6
X.MESH NODE=48 LOCATION=2.5
X.MESH NODE=55 LOCATION=6.5
X.MESH NODE=65   LOCATION=8

Y.MESH NODE=1    LOCATION=-8.5
Y.MESH NODE=3   LOCATION=-7.83
Y.MESH NODE=5 LOCATION=-7.79
Y.MESH NODE=7  LOCATION=-6.35
Y.MESH NODE=10  LOCATION=-6.27
Y.MESH NODE=13    LOCATION=-5
Y.MESH NODE=15  LOCATION=-4.7
Y.MESH NODE=18  LOCATION=-2.42
Y.MESH NODE=21  LOCATION=0


Z.MESH NODE=1 LOCATION=0
Z.MESH NODE=5 LOCATION=0.4932
Z.MESH NODE=6 LOCATION=0.5496
Z.MESH NODE=16  LOCATION=2.0503
Z.MESH NODE=20  LOCATION=2.1067
Z.MESH NODE=24  LOCATION=2.5999


ELIMINATE COL Y.MIN=-4 X.MAX=2.5

REGION NAME=1 SILICON


REGION NAME=2 OXIDE X.MIN=1.6 X.MAX=8 Y.MIN=-6.27 Y.MAX=-2.42 Z.MIN=0
Z.MAX=2.5999

REGION NAME=2 OXIDE X.MIN=0 X.MAX=8  Y.MIN=-8.5 Y.MAX=-7.79 Z.MIN=0
Z.MAX=2.5999

$ pcolumn side oxide
REGION NAME=2 OXIDE X.MIN=0.7821 X.MAX=0.8248 Y.MIN=-8 Y.MAX=-4.7 Z.MIN=0.5496
Z.MAX=2.0503
REGION NAME=2 OXIDE X.MIN=1.56  X.MAX=1.6 Y.MIN=-8 Y.MAX=-4.7 Z.MIN=0.5496
Z.MAX=2.0503

$ oxide for p column
```

```
REGION NAME=2 OXIDE X.MIN=0.7821 X.MAX=1.6 Y.MIN=-7.79 Y.MAX=-4.7 Z.MIN=0.4932
Z.MAX=0.5496
REGION NAME=2 OXIDE X.MIN=0.7821 X.MAX=1.6 Y.MIN=-7.79 Y.MAX=-4.7 Z.MIN=2.0503
Z.MAX=2.1067

$bottom oxide
REGION NAME=2 OXIDE X.MIN=0.7821 X.MAX=1.6 Y.MIN=-4.9173 Y.MAX=-4.7 Z.MIN=0
Z.MAX=2.5999

$bot gate top oxide
REGION NAME=2 OXIDE X.MIN=0.7821 X.MAX=1.6 Y.MIN=-6.35   Y.MAX=-6.27 Z.MIN=0
Z.MAX=0.5496
REGION NAME=2 OXIDE X.MIN=0.7821 X.MAX=1.6 Y.MIN=-6.35   Y.MAX=-6.27
Z.MIN=2.0503 Z.MAX=2.5999

$n column side oxide
REGION NAME=2 OXIDE X.MIN=0.7821 X.MAX=0.8248 Y.MIN=-6.35   Y.MAX=-4.7 Z.MIN=0
Z.MAX=0.5496
REGION NAME=2 OXIDE X.MIN=0.7821 X.MAX=0.8248 Y.MIN=-6.35   Y.MAX=-4.7
Z.MIN=2.0503 Z.MAX=2.5999
REGION NAME=2 OXIDE X.MIN=1.56  X.MAX=1.6 Y.MIN=-6.35   Y.MAX=-4.7 Z.MIN=2.0503
Z.MAX=2.5999
REGION NAME=2 OXIDE X.MIN=1.56 X.MAX=1.6 Y.MIN=-6.35   Y.MAX=-4.7 Z.MIN=0
Z.MAX=0.5496

$ gate poly

$poly in p column buried gate &trench gate
REGION NAME=4 POLY   X.MIN=0.8248 X.MAX=1.56 Y.MIN=-7.83 Y.MAX=-4.9173
Z.MIN=0.5496 Z.MAX=2.0503

$poly in n column
$top gate
REGION NAME=4 POLY X.MIN=0.8248 X.MAX=1.8 Y.MIN=-8.5 Y.MAX=-7.83 Z.MIN=0
Z.MAX=2.5999

$buried gate
REGION NAME=4 POLY   X.MIN=0.8248 X.MAX=1.56 Y.MIN=-6.27 Y.MAX=-4.9173 Z.MIN=0
Z.MAX=2.5999


$side wall oxide
REGION NAME=2 OXIDE  X.MIN=1.8  Y.MIN=-7.8 Y.MAX=-6.7216  Z.MIN=0.4932
Z.MAX=0.5496
REGION NAME=2 OXIDE  X.MIN=1.8  Y.MIN=-7.8 Y.MAX=-6.7216  Z.MIN=2.0503
Z.MAX=2.1067

$GATE
ELECTRODE NAME=Gate region=4 VOID

$SOURCE
ELECTRODE NAME=Source X.MAX=0.6 Y.MAX=-7.79 VOID

$DRAIN
ELECTRODE NAME=Drain X.MIN=7.5 Y.MAX=-7.79 VOID

$ELECTRODE PREV NAME=Gate  ELIMINATE
$ELECTRODE NAME=Gate  region=4  VOID
```

```
PROFILE P-TYPE  X.MIN=1.6 X.MAX=8 Y.MIN=-7.82 Y.MAX=-6.27 Z.MIN=0.5496
Z.MAX=2.0503
+ UNIFORM N.PEAK=1.87E16

PROFILE N-TYPE X.MIN=1.6 X.MAX=8 Y.MIN=-7.82 Y.MAX=-6.27 Z.MIN=0 Z.MAX=0.4932
+ UNIFORM N.PEAK=4.2E16

PROFILE N-TYPE X.MIN=1.6 X.MAX=8 Y.MIN=-7.82 Y.MAX=-6.27 Z.MIN=2.1067
Z.MAX=2.5999
+ UNIFORM N.PEAK=4.2E16

PROFILE N-TYPE X.MIN=0 X.MAX=8 Y.MIN=-6.27 Y.MAX=0 Z.MIN=0 Z.MAX=2.5999
+ UNIFORM N.PEAK=2E15

$ Pbody

PROFILE P-TYPE N.PEAK=1.16E18 Y.DIRECT  Y.MIN=-7.2 Y.MAX=-7.1 Y.CHAR=0.6
+ X.MIN=0 X.MAX=0 X.CHAR=1.1

$ Source

PROFILE N-TYPE N.PEAK=2.34E20 Y.DIRECT Y.MIN=-7.7 Y.MAX=-7.7 Y.CHAR=0.1
+ X.MIN=0.5 X.MAX=0.5 X.CHAR=0.15

$ Drain
PROFILE N-TYPE N.PEAK=1E20 Y.DIRECT Y.MIN=-7.63 Y.MAX=-7.63 Y.CHAR=0.37
+ X.MIN=8 X.MAX=8 X.CHAR=0.5


PRINT POINTS


PLOT.1D DOPING X.START=4 X.END=4 Y.START=-7.5 Y.END=-7.5 Z.START=0 Z.END=2.538

PLOT.1D DOPING X.START=4 X.END=4 Y.START=-7.9 Y.END=-6.1 Z.START=1.2 Z.END=1.2

PLOT.3D   BOX  BOUNDFILL     CAM=(-100,-100,-100) GRID
PLOT.3D   BOX  BOUNDFILL     CAM=(-100,-100,-100) GRID
+ Z.MIN=0.3

PLOT.3D   BOX  BOUNDFILL     CAM=(-100,-100,-100) GRID
+ Z.MIN=1

PLOT.3D   BOX  BOUNDFILL     CAM=(-100,-100,-100) GRID
+ Z.MIN=1.3

PLOT.3D   BOX  BOUNDFILL     CAM=(-100,-100,-100) GRID
+ X.MIN=0.8

PLOT.3D   BOX  BOUNDFILL     CAM=(-100,-100,-100) GRID
+ X.MIN=1.2

PLOT.3D   BOX  BOUNDFILL     CAM=(-100,-100,-100) GRID
+ X.MIN=1.5
PLOT.3D   BOX  BOUNDFILL     CAM=(-100,-100,-100) GRID
+ Z.MIN=2.3


$STOP
```

```
$ Model Statement
MODELS          CONMOB          FLDMOB          CONSRH          AUGER BGN       SRFMOB2
SYMB   CARR=0
METHOD          ICCG    DAMPED

SOLVE  V(Gate)=0.0  V(Drain)=0.0            V(Source)=0.0

SYMB   CARR=1           NEWTON          ELECTRON

$ Gate characteristics simulation
$LOG    OUT.FILE=OBUMOSVthdat
$SOLVE          V(Drain)=0.1
$SOLVE          V(Gate)=0.2     ELEC=Gate       VSTEP=0.2       NSTEP=20
$PLOT.1D        Y.AX=I(Drain)   X.AX=V(Gate)    POINTS          COLOR=2
$+      PLOT.OUT=OBUMOSon1.ps DEVICE=L/POSTSCRIPT
$TITLE "Gate Curve"


$ Bias up the gate
SOLVE  ELEC=Gate        V(Gate)=2.0     VSTEP=2         NSTEP=9
        OUT.FILE=OBUMOSSOL02            SAVE.BIA

$ Drain characteristics simulation at Vg=20V
LOAD   IN.FILE=OBUMOSSOL11
LOG    OUT.FILE=OBUMOSD11
SOLVE  ELECTROD=Drain           v(Drain)=0      VSTEP=0.5       NSTEP=60

SAVE SOLUTION OUT.FILE=finalresult


$ Drain curve
PLOT.1D         IN.F=OBUMOSD11          X.AX=V(Drain)  Y.AX=I(Drain)   POIN
        TITLE="Drain curve"
$+      PLOT.OUT=OBUMOSon3.ps DEVICE=L/POSTSCRIPT




$ Drain characteristics simulation at other gate voltages
LOOP   STEPS=8
        ASSIGN          NAME=SFX        C.VAL=09        DEL=-1
        LOAD   IN.FILE="OBUMOSSOL"@SFX
        LOG    OUT.FILE="OBUMOSD"@SFX
        SOLVE  ELECTROD=Drain           V(Drain)=0      VSTEP=0.5       NSTEP=60
L.END

$ Drain curve
PLOT.1D         IN.F=OBUMOSD11          X.AX=V(Drain)  Y.AX=I(Drain)   POIN
        TITLE="Drain curve"
$+      PLOT.OUT=OBUMOSon3.ps DEVICE=L/POSTSCRIPT

LOOP   STEPS=8
        ASSIGN          NAME=SFX        C.VAL=09        DEL=-1
        PLOT.1D         IN.F="OBUMOSD"@SFX              X.AX=V(Drain)  Y.AX=I(Drain)
        POIN   UNCH
L.END
```