A VERY HIGH SPEED BANDPASS CONTINUOUS TIME SIGMA DELTA MODULATOR FOR RF RECEIVER FRONT END A/D CONVERSION

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Abstract

Directly sampling the Radio Frequency (RF) signal in the receiver front end moves the forthcoming Intermediate Frequency (IF) conversion, filtering, channel selection and In phase, Quadrature phase demodulation into the digital domain. Pushing more functions of the receiver into digital domain will tend to a system which is less complex, low distortion and more robust to temperature and process variation with reduced cost, size, weight and power dissipation. The above demands a very high speed Analog to Digital Converter (ADC) which would sample the signals directly at GHz with high linearity and dynamic range.

Though previously continuous-time bandpass Sigma Delta modulators were used for RF digitization, all of the reported work used RF bipolar transistors of SiGe HBT, AlGaAs/GaAs HBT or InP HBT in realizing the modulator. This limits the monolithic integration of the ADC and the digital signal processing modules (which are prevailingly designed in CMOS) on the same chip in a RF receiver. Hence this research thesis focuses on designing a very high frequency Sigma Delta modulator in CMOS technology. This is the first time that such a high frequency modulator is ever tried in CMOS.

A design and circuit implementation of a CMOS fourth-order continuous-time bandpass $f_s/4$ Sigma-Delta modulator is presented. The modulator uses fully differential multi feedback architecture. A novel way of realizing the feedback architecture in circuit in order to overcome the problem of loop delay in the modulator is proposed. Simulation results comparing the conventional architecture and the proposed one are also reported. To realize the bandpass filters, integrated LC resonators with active Q enhancement is

used. A very high frequency transconductor is used to driving the bandpass LC resonators. Dynamic comparators are used to quantize the signal and the output is shaped to a return to zero, half return to zero waveform. The feedback occurs in current domain with the current from the switched current source DACs and that from the transconductor.

The modulator, designed for 0.18µm/1.8V 1P6M CMOS process occupies a total area of 1.8mm^2 dissipating 290mW from a 1.8V power supply. At a sampling rate of 4GHz and a signal of 1GHz with 500 kHz bandwidth, the circuit achieves a peak Signal-to-Noise and Distortion Ratio (SNDR) of 40dB. With the proposed architecture the loop delay is keep below 3% of the clock period. The proposed architecture is also put under test for higher sampling frequencies to prove its stability.

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List of Abbreviations

ADC	Analog-to-Digital Converter
BJT	Bipolar Junction Transistor
CT	Continuous-Time
DAC	Digital-to-Analog Converter
ΣΔM	Sigma Delta Modulator
BP	Band Pass
LP	Low Pass
STF	Signal Transfer Function
NTF	Noise Transfer Function
HBT	Hetero-junction Bipolar transistor
OSR	Over Sampling Ratio
SNR	Signal to Noise Ratio
RMS	Root Mean Square
PDM	Pulse Density Modulation
DT	Discrete-Time
SC	Switched Capacitor
SNDR	Signal to Noise and Distortion Ratio
RZ	Return to Zero
HZ	Half return to Zero
NZ	Non return to Zero
DR	Dynamic Range
VHF	Very High Frequency
RF	Radio Frequency
IF	Intermediate Frequency
DSP	Digital Signal Processing
Gm-C	Transconductor-Capacitor
OPAMP	Operational Amplifier
Q	Quality factor
LO	Local Oscillator
CMOS	Complementary Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board

Chapter 1

Introduction

The Analog to Digital Converters (ADC) are well applied in many applications to function as converting an analog waveform into a digital waveform (digital codes) at particular sampling instances. The ADC is a key component in many electronic system, since by nature all waveforms exist inherently in analog domain while in electronic systems all computations are mainly carried out in digital domain which is a more robust, flexible and reliable domain for signal processing.

1.1 Role of ADC in Radio Receivers – Moving towards "Less Analog More Digital"

This thesis is much focused around the role of ADCs in radio receiver systems, which have become the part and parcel of everyday life. The position of ADC in a radio receiver is crucial in deciding whether a particular function of the receiver is to be implemented using analog or digital circuits. By studying the different radio receiver architectures the above fact becomes easier to understand.

1.1.1 Superheterodyne Receiver with baseband ADC

Traditional superheterodyne receiver architecture is shown in Fig. 1.1(a). The antenna signal is filtered by a wide bandpass filter and amplified by a low-noise amplifier. The desired Radio Frequency (RF) channel is selected by tuning the F_{LO} and mixing it down to a lower intermediate frequency (IF). The channel filter passes the desired IF channel

suppressing the adjacent channels by about 30-40dB. After amplification the signal is quadrature mixed into In-phase and Quadrature-phase channels at baseband, which is then anti-alias filtered and digitized. Further signal processing is done using Digital Signal Processing (DSP). Requirements for such baseband ADC regarding dynamic range, bandwidth and linearity are relaxed due to the filters which are preceding it. Sampling the baseband signal also leads to lower sampling rate, resulting in low power consumption.

1.1.2 Heterodyne receiver with IF digitizing ADC

The evolution of bandpass ADCs made them to be placed at a position closer to the antenna. An IF digitizing receiver is shown in Fig 1.1(b) where in, a bandpass wideband ADC sits well before the channel filter digitizing all the channels. The channel selection and quadrature modulation are implemented in DSP, with low-power consumption, prefect linearity and matching for excellent image rejection performance. Moreover IF ADC is insensitive to DC offset and low-frequency noise. But the lack of analog prefiltering by the channel filter and amplification by Variable Gain Amplifier (VGA) places a heavy linearity and dynamic range requirements on the IF ADC. The sampling rate is high due to IF digitization. This results in a systems that is less power efficient than a baseband ADC. Furthermore, the linearity and dynamic range requirements are more difficult to meet at higher frequencies [17].

1.1.3 RF digitization

The RF digitizing receiver which is in focus of current research and also in this thesis is shown in the Fig. 1.1(c). The only analog components are the RF bandpass filter and the Low Noise Amplifier (LNA). All the other functions namely the IF frequency translation,

channel filtering, and quadrature demodulation are done in DSP. This ADC should have a high dynamic range, high linearity and large bandwidth at RF frequencies. Since the sampling rate of the ADC is in GHz range the power consumption would be extremely heavy [13].

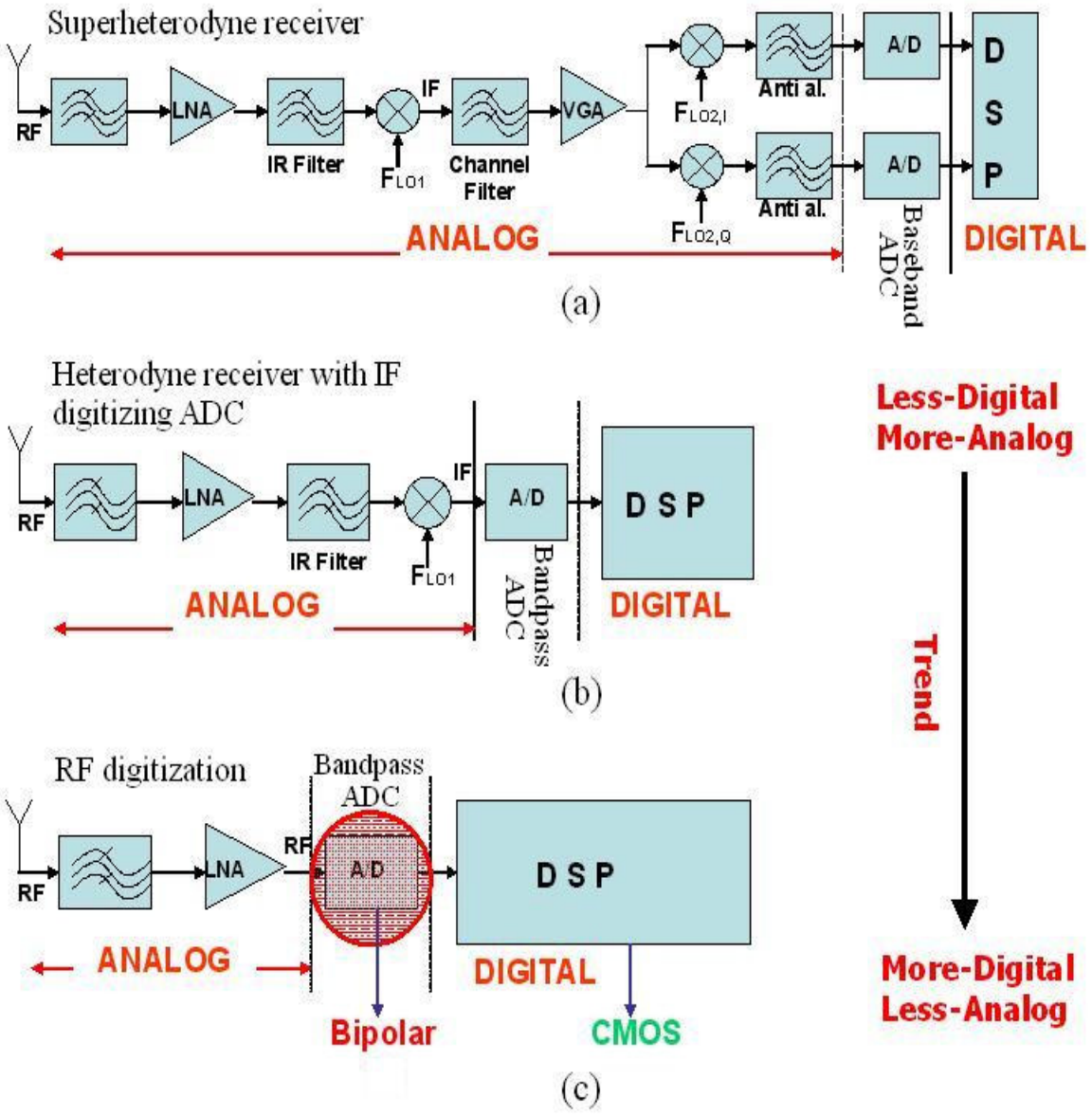


Figure 1.1: Radio receiver architectures

As illustrated in Fig. 1.1, the current research trend is moving from radio receiver architectures which had less digital components but more analog components to

architectures employing more digital components than analog components. This is achieved generally (there might be unexplored other ways) by moving the ADC closer and closer to the antenna.

1.2 Motivation and problem statement

As discussed above, the state of art is to achieve an ADC which is very close to the antenna leading to an 'all-digital radio'. Pushing more functions of the receiver into DSP will tend to a system which is more robust to temperature and process variation with reduced cost, size, weight and power dissipation. Performing all the functions digitally leads to a 'Programmable Software Radio'. Such programmability allows a single set of hardware to be used for multi-standard receiver by just altering the software in it. A few implementations of very high frequency bandpass Sigma Delta modulators in bipolar RF transistors of SiGe HBT [7], AlGaAs/GaAs HBT [20] and InP HBT [21] have been reported. This limits the monolithic integration of the ADC and the digital signal processing modules (which are prevailingly designed in CMOS) on the same chip in a RF receiver as shown in Fig. 1.1(c).

1.2.2 Objective and scope of the research

The Objective of this research is to implement a CMOS continuous–time bandpass $f_s/4$ Sigma Delta modulator for RF front end, which digitizes signals centered at 1GHz with a sampling frequency of 4GHz. This is the first time that such a very high frequency is ever tried in CMOS bandpass Sigma Delta ADC. However, literature search shows that CMOS bandpass Sigma Delta modulators realized in the past were up to a maximum sampling frequency of 400MHz with the signal centered at 100MHz [40].

The targeted performance of the modulator to be designed in this thesis is shown in the Table 1.1.

Table 1.1: Modulator targeted performance

Technology	0.18μm CMOS
Input signal centered at	1GHz
Sampling frequency	4GHz
Input signal bandwidth	500kHz
Dynamic Range	6 bits

The scope of the research would be,

1. To study and identify the suitability of CMOS over bipolar at very high frequencies.
2. The design issues involved when employing CMOS in very high frequencies.
3. System design and simulation of a band pass $f_s/4$ Sigma Delta modulator to meet the above specification.
4. To simulate the non-idealities that may affect the above system when implemented practically for operating at high frequencies.
5. To investigate design solution for very high frequency CMOS applications.
6. To design the system in 0.18μm CMOS technology, taking into account the practical non-idealities and simulation in HSpice.
7. Layout, fabrication and testing of the design.

1.3 Organization of the thesis

Following the above introduction to the role of ADCs in radio receivers and the motivation behind this research, chapter 2 provides the basics of quantization which is the key function of an analog to digital converter. The Sigma-Delta modulator is introduced with the oversampling and noise shaping concepts explained in detail. Among the in numerable choices of ADCs, the continuous-time bandpass $f_s/4$ Sigma-Delta modulator is shown to be the better choice for RF digitization.

In chapter 3, the design of a continuous-time bandpass $f_s/4$ Sigma-Delta modulator is discussed followed by development and simulation of an ideal model in MATLAB Simulink. Chapter 4 explains the different non idealities such as loop delay, quantizer metastability, clock jitter etc. that exist in practical circuit realization of a continuous time modulator. The performance degradation effects of such non idealities on the modulator are also described.

The modulator realization in circuit is elaborated in chapter 5. A circuit topology to realize the ideal modulator and which also circumvents most of the non ideal issues is explained in detail. The individual circuit components comprising the circuit topology are also discussed. Some layout issues in high speed mixed signal design are listed. The post-layout simulation performance of the modulator is also provided along with some analysis for the results obtained.

In an attempt to first test the different parts of the modulator individually, chapter 6 gives the test results of a output buffer and a feedback comparator structure fabricated in 0.18μm CMOS process. In chapter 7 a comparison of this work with the other reported very high frequency CTΣΔMs is tabulated along with suggestions for future work.

Chapter 2

Sigma Delta Modulator – An Overview

In this chapter, the basic concepts involved in analog-to-digital conversion and in a Sigma-Delta modulator has an ADC are looked upon. The different types of ΣΔM are also discussed along with their respective advantages and disadvantages. Among the available design choices a suitable one is chosen for the purpose of analog to digital conversion in Radio Frequency (RF) receiver front ends.

2.1 Quantization noise

The quantization is often considered as the core of analog-to-digital conversion. A general quantization transfer characteristics is shown in Fig. 2.1(a). The quantization error noise (ε) occurs due to the fact that while digitizing, the continuous analog waveform Fig. 2.1(b), is approximated within the quantization levels or the bin width (Δ). Let M be the no. of quantization levels and x be the input signal bonded between [$-M\Delta/2$, $M\Delta/2$] so that the quantizer is not overloaded. The quantization noise rising from such a non-overloaded quantizer is called granular noise and the quantized signal $q(x)$ can be written of the form [5],

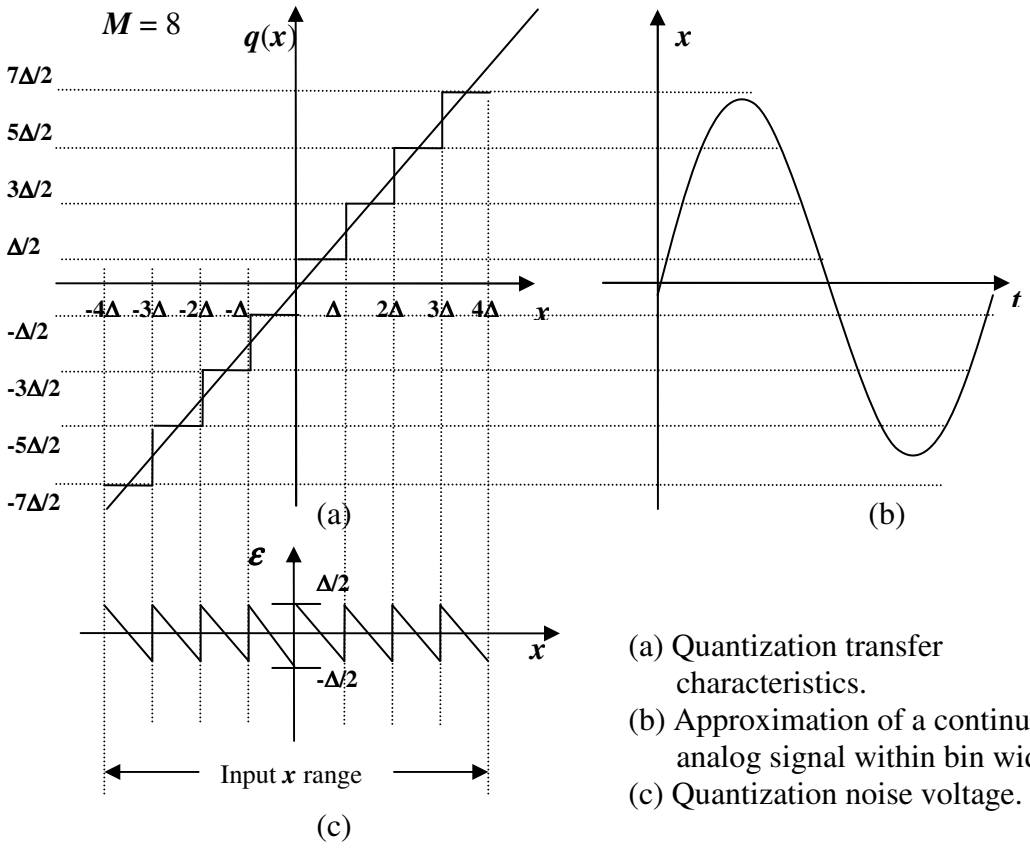
$$q(x) = G\,x + \varepsilon \tag{2.1}$$

G, gain, is the slope of the straight line passing through the center of the quantization characteristics curve. And the granular noise ε is bounded between $\pm\,\Delta/2$ as shown in Fig. 2.1(c). This noise error ε is completely defined by the input, but if the input changes

randomly between samples by amounts comparable with the threshold spacing without overloading, then the error is largely uncorrelated from sample to sample and has equal probability of lying anywhere in the range ± Δ/2 and can be considered as a white noise.

It is reported in [3] that the white noise assumption of the quantization noise provided a good approximation to reality if in particular,

1. The quantizer does not overload,
2. The quantizer has a large number of levels,
3. The bin width is small and
4. The probability distribution of pairs of input samples is given by a smooth probability density function.



(a) Quantization transfer characteristics.
(b) Approximation of a continuous analog signal within bin width.
(c) Quantization noise voltage.

Figure 2.1: Quantization

If the quantization error ε is treated has a white noise then its mean square value can be calculated from,

$$\varepsilon_{\text{rms}}^2 = \int_{-\Delta/2}^{+\Delta/2} \varepsilon^2 d\varepsilon = \frac{\Delta^2}{12} \tag{2.2}$$

When a quantized signal is sampled at a frequency $f_s = 1/T$, all of its quantization noise power folds into the frequency band $0 \le f \le f_s/2$, assuming one-sided representation of frequencies. Then, if the quantization noise is white, the spectral density of the sampled noise is given by [3],

$$\text{E}(f) = \varepsilon_{\text{rms}} \left(\frac{2}{f_s} \right)^{1/2} = \varepsilon_{\text{rms}} \sqrt{2T} \tag{2.3}$$

The quantization noise spectral density is as shown in Fig. 2.2. Examining equation (2.3) it is evident that by increasing the sampling frequency, the amount of quantization noise that an ADC introduces to an analog signal can be reduced, as detailed in Sec. 2.2.2. Increasing the sampling frequency spreads out the quantization noise spectral density over a wider range of frequencies (see Fig. 2.2) with a corresponding reduction in amplitude. However the sampling frequency doesn't affect the total Root Mean Square (RMS) quantization voltage (i.e.) the area under the quantization noise spectrum.

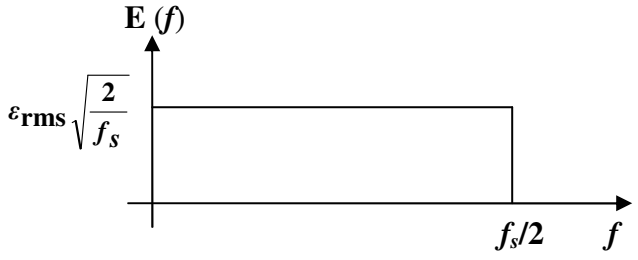


Figure 2.2: Quantization noise spectral density.

2.2 Sigma Delta Modulator – Pulse Density Modulation

The Evolution of Sigma Delta Modulator (ΣΔM) dates back to 1962, when Inose et al. [18], [19] proposed the idea of including an integrator in front of a delta modulator, to eliminate slope overload. Hence the name "Sigma Delta Modulator", "Sigma" to denote the integrator, followed by a "Delta Modulator", was probably given to the system. The idea of reducing the quantization noise by using a feedback [33] also forms a basic operation of this system.

A ΣΔM has three basic components as shown in Fig. 2.3:

1. A loop filter or a loop transfer function $H(z)$.
2. A clocked quantizer.
3. A feedback Digital-to-Analog Converter (DAC).

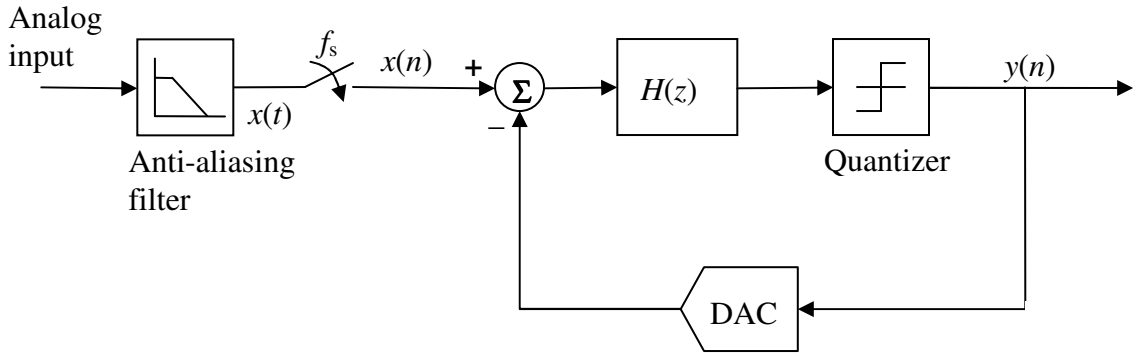


Figure 2.3: The basic components of Sigma Delta modulator

The ΣΔM shown in Fig. 2.3 is a Discrete-Time (DT) modulator. The sampled input $x(n)$ is fed to the quantizer via a loop filter $H(z)$, and the quantizer output $y(n)$ is fed back through a DAC and subtracted from the input. This feedback forces the average value of the quantized signal to track the average input. Any difference between them accumulates

in the integrator and eventually corrects itself. In a single bit ΣΔM, the output of the quantizer oscillates between +1 and -1 and the input signal is represented by the density of ones. This signal is called a Pulse Density Modulated (PDM) signal. Figure 2.4 illustrates this fact, where a sine wave of 122.07Hz and 0.7V amplitude is sampled at 1MHz and the output from the quantizer is averaged over 16 samples. A loop filter of transfer function $H(z) = 1 / (z\text{-}1)$ is used and the DAC is assumed to be unity. It is evident that the averaged value of the quantizer signal tracks the input sine wave. This averaging of the PDM signal output from a ΣΔM is nothing but a lowpass function and it is usually performed by a decimator following the modulator. The modulator plus the following decimator forms the whole ADC. All the discussions in this thesis will be pertaining to the modulator, which forms the important part of the ADC.

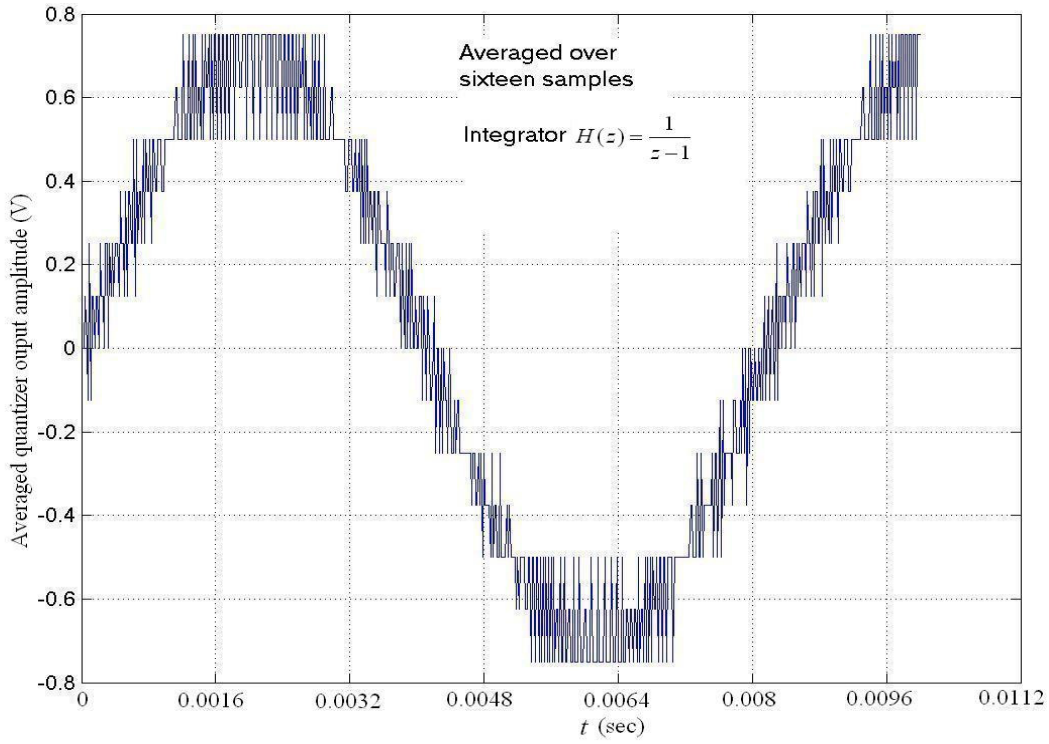


Figure 2.4: The averaged quantizer output signal tracking the modulator sine input

To reduce the quantization noise in the signal band, the ΣΔM uses two main concepts namely (i) Noise shaping and (ii) Oversampling, which are explained below.

2.2.1 Noise Shaping

In Fig. 2.3, the quantizer is the only nonlinear circuit in an otherwise linear system. This makes the behavior of ΣΔM very complicated to investigate analytically [16]. Hence we assume that the quantization noise is independent of the modulator input signal $x(n)$ (as explained in Sec. 2.1) and replace it with an additive white noise $\varepsilon(t)$ as shown in the Fig. 2.5.

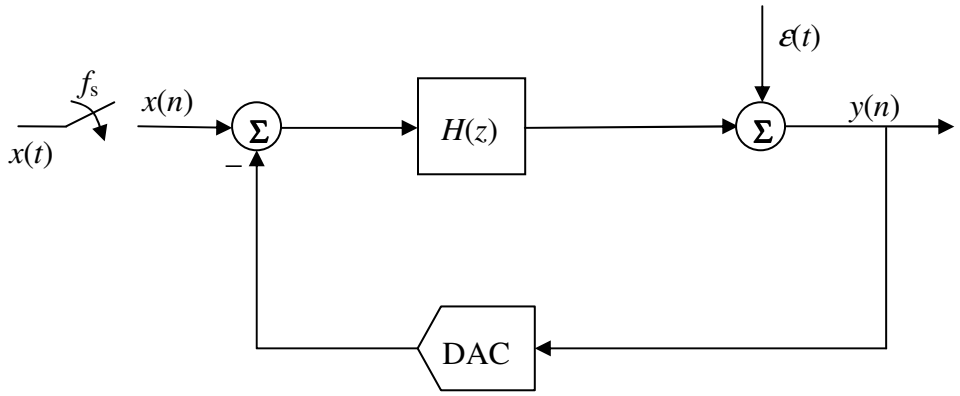


Figure 2.5: Linearizing the quantizer in ΣΔM

The output $y(n)$ can now be written in terms of two inputs $x(n)$ and $\varepsilon(t)$.

$$Y(z) = \frac{H(z)}{1+H(z)} X(z) + \frac{1}{1+H(z)} \varepsilon(z) \tag{2.4}$$

$$Y(z) = STF(z)X(z) + NTF(z)\varepsilon(z) \tag{2.5}$$

where $STF(z)$ and $NTF(z)$ are the Signal Transfer Function and Noise Transfer Function respectively. From equations (2.4) and (2.5), two important conclusions can be deduced (i) the poles of loop filter $H(z)$ becomes the zeros of noise transfer function $NTF(z)$ (i.e.) if

$H(z)$ is lowpass filter then $NTF(z)$ will be of high pass type. (ii) For any frequency where H(z) >> 1, then from equation (2.4) Y(z) ≈ X(z) i.e. the output spectra equals to that of input at frequencies where the gain of H(z) is large.

Loop filter $H(z)$ can be of a lowpass or a bandpass transfer function, which determines the type of modulator under design. Assuming a band pass case where,

$$H(z) = \frac{2z^2 + 1}{\left(z^2 + 1\right)^2} \tag{2.6}$$

then from eq. (2.4),

$$STF(z) = \frac{2z^2 + 1}{z^4 + 4z^2 + 2} \tag{2.7}$$

$$NTF(z) = \frac{(z^2 + 1)^2}{z^4 + 4z^2 + 2} \tag{2.8}$$

the magnitude response of STF(z) and NTF(z) from eq. (2.7) and (2.8) is plotted in the Fig. 2.6(a) and (b) respectively, against normalized frequency. It is evident that the $STF(z)$ has a response similar to a band pass filter, while the response of $NTF(z)$ resembles a band stop filter (this is due to the fact that the poles of $H(z)$ becomes the zeros of $NTF(z)$).

If the input $X(z)$ is centered at $\omega_S/4$ where ω_S is the sampling frequency, the signal transfer function $STF(z)$ in eq. (2.7) passes the input without any attenuation as it is evident from Fig. 2.6(a). However, the quantization noise $\varepsilon(z)$ rising due to the sampling of input $X(z)$ is attenuated at $\omega_S/4$ by the band stop nature of $NTF(z)$ as shown in Fig. 2.6(b). Hence the resultant effect is that while passing the input signal undisturbed, the noise arising due to quantization is totally shaped away from the input signal band. This leads to an increase in Signal-to-Noise Ratio (SNR).

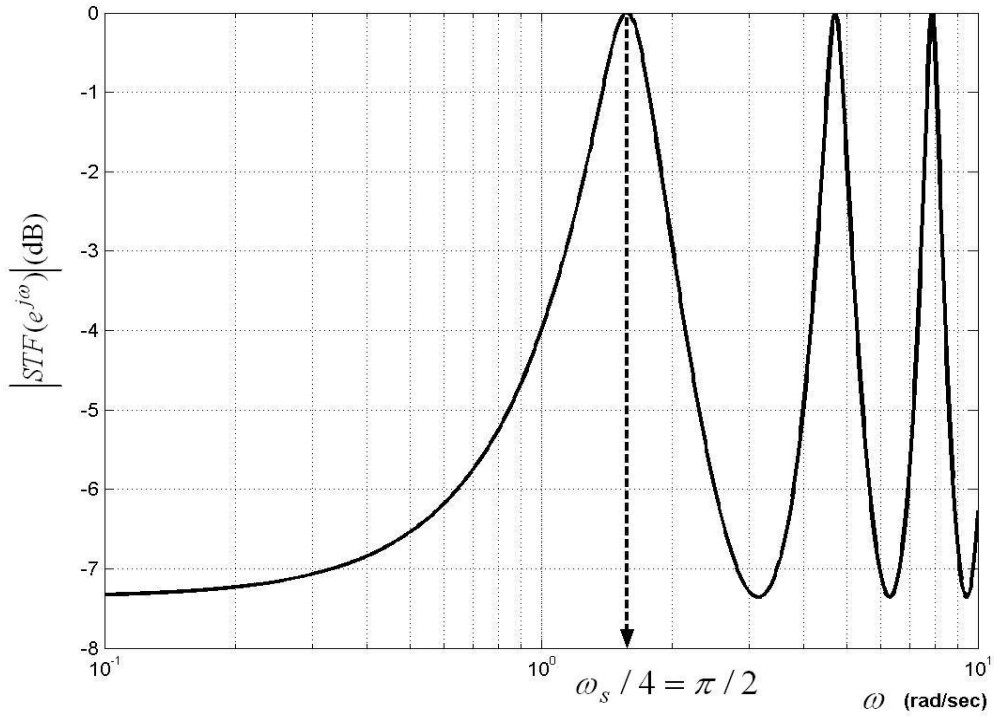


Figure 2.6(a): Magnitude of Signal Transfer Function *STF*(z)

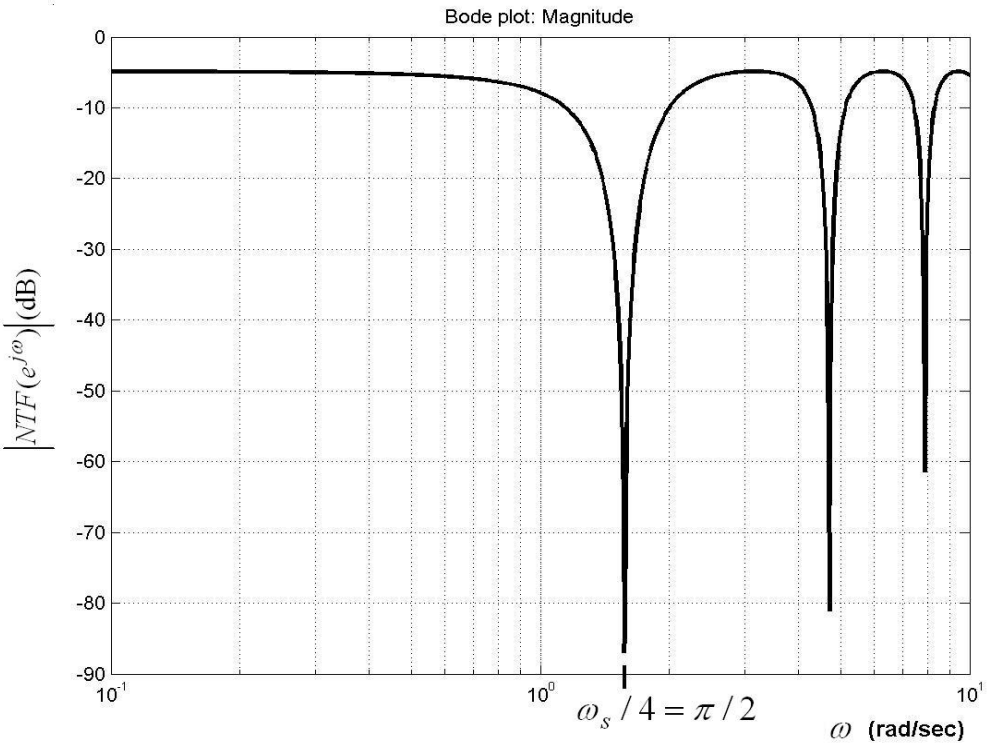


Figure 2.6(b): Magnitude of Noise Transfer Function *NTF*(z)

2.2.2 Oversampling

As observed from Fig. 2.6(b) the quantization noise ε is reduced only in a very small bandwidth when compared to the sampling frequency ω_S. This needs that the sampling frequency to be very high. Say if a signal input x has a bandwidth of B_X, then its Nyquist frequency $\omega_N = 2B_X$ should be such that, $\omega_N << \omega_S$. Hence the modulator samples the signal at a frequency much higher than its Nyquist frequency and such modulators are termed as over sampling modulators. A measure of how much the sampling frequency is higher than the Nyquist frequency is given by the Over Sampling Ratio (OSR),

$$\text{OSR} = \frac{\omega_S}{\omega_N} = \frac{\omega_S}{2B_X} \tag{2.9}$$

From equation (2.3) it is evident that as the sampling frequency ω_S increases (or an increase in OSR), the quantization noise spectrum spreads out and the in band noise amplitude decreases. In general if M is the order of the loop filter $H(z)$ then the rms noise in signal band is given by [5],

$$n_o = \varepsilon_{\text{rms}} \frac{\pi^M}{\sqrt{2M+1}} \left(\frac{1}{\text{OSR}} \right)^{M+1/2} \tag{2.10}$$

which falls by 3(2M+1) dB for every doubling of the sampling rate or the OSR, providing M+0.5 extra bits. In other words increasing OSR, decreases the in band noise and enhances the system performance.

To sum up, the basic idea of a ΣΔM can be stated as [6]: an analog input signal is modulated into a digital word sequence whose spectrum approximates that of the analog input well in a narrow frequency range, but which is otherwise noisy. The noise arising from the quantization of the analog signal is minimized by oversampling and noise shaping by the loop filter in the desired narrow frequency range.

2.3 The choice of an ADC for RF front end

For an ADC to be used in RF front end of receivers, it should operate at very high frequencies, be highly tolerant to component mismatching and consume less power. Among the many types of ADCs reported, Flash and Sigma Delta are the well known very high speed ADCs. In an N bit Flash ADC [37], an input signal is compared with 2^N reference voltages obtained with for instance a resistor string. The digital output word is obtained from the comparator outputs. The sampling rate is determined mainly by the comparator settling time and the accuracy is limited by the resistor matching and by the comparator offset voltages. Flash ADCs of 6-bit resolution, sampling at 1.3GHz have been reported [36]. Even though Flash ADCs can be used in very high speed conversion, their accuracy is ultimately limited by component matching and has a very complex circuitry compared to that of Sigma Delta converters.

In the DT ΣΔM block diagram of Fig. 2.3, the analog input passes through an analog anti-aliasing filter first. This would be case for any ADC where the input signal is first band limited before sampling. In classical ADCs since the anti-aliasing filter has a finite filter roll-off, the signal band is smaller than half of the minimum Nyquist sampling rate (refer Fig. 2.7(a)). However in a Sigma Delta modulator the signal is sampled at a much higher rate than that of the Nyquist rate. From Fig. 2.7(b) it is clear that only signals above f_s-f_N /2 can alias with the signal band. As a result, a smoother pass band slope can be tolerated, which results in simpler filter design. Spurious signals at frequencies between f_N /2 and f_s-f_N /2 are removed afterwards by the decimation filter. By this way comparing to other ADCs, in ΣΔ ADC complex analog filter goes into digital domain, where things are much easier to design. Furthermore, the ability of a ΣΔM to perform

narrowband conversion at a frequency other than dc make them particularly attractive than any other ADCs for radio applications (will be explained in the next section).

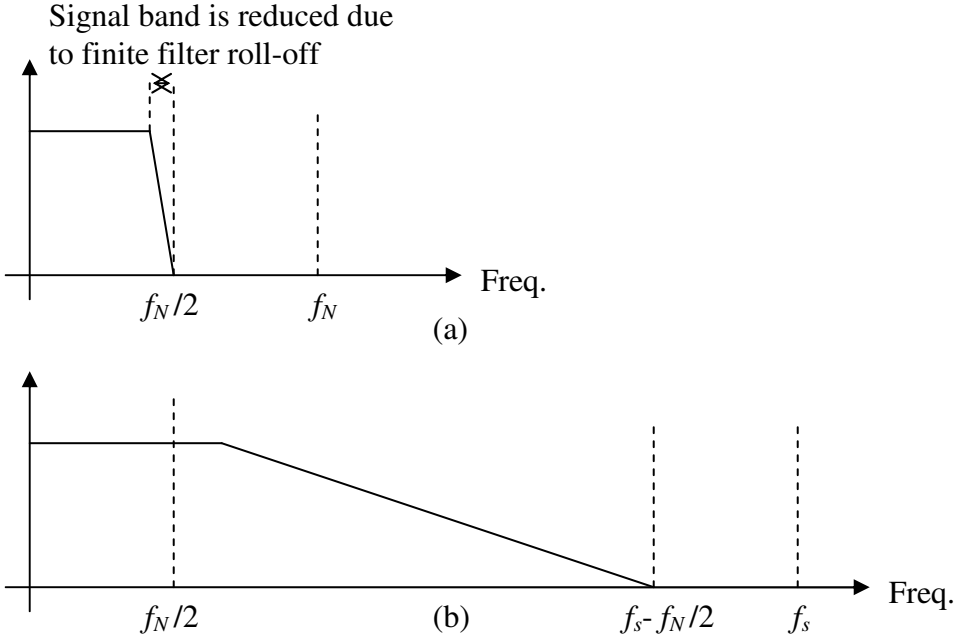


Figure 2.7: The anti-aliasing filter magnitude response
(a) Nyquist rate ADC
(b) Over sampled ΣΔ ADC

2.3.1 Band pass Sigma Delta modulator

The loop filter $H(z)$ shown in Fig. 2.3 can be of a low pass type. In this case the quantization noise is shaped away from dc and the noise transfer function has a high pass shape. This modulator is called a Low Pass (LP) ΣΔM. Alternatively, the $H(z)$ can be of bandpass type, say a resonator. In this case the quantization noise would be shaped away from the resonant frequency and the noise transfer function would be band stop function (as discussed in Sec. 2.2.1). Such a modulator is called a Band Pass (BP) ΣΔM. Given the two options, bandpass Sigma Delta modulators have been the best choice for ADC design, converting a very high frequency narrow band signal with high resolution [7], [13].

Further we choose the resonant frequency of the bandpass filter be at $f_s/4$ for the reason stated below. Usually a bandpass ADC is used in conversion of an RF or IF signal to digital for processing and heterodyning in the digital domain, as shown in Fig. 2.8 [7]. Mixing to baseband digitally for In-phase and Quadrature-phase channel becomes particularly easy when the sampling frequency is chosen to be four times the input signal frequency because sine and cosine are sequences involving only ±1 and 0. This eliminates the complex multiplication in digital domain, because the processing on input digital bits would be easier and it is enough if we only change the sign (for multiplication with -1) or leave it as it is (for multiplication with +1) or make it zero (for multiplication with 0).

With the facts stated above, there are convincing reasons to choose a bandpass $f_s/4$ Sigma Delta Modulator for digital conversion in RF front ends. But still one more design option, whether to choose a discrete time modulator or a continuous time modulator is yet to be decided upon, which will be detailed further.

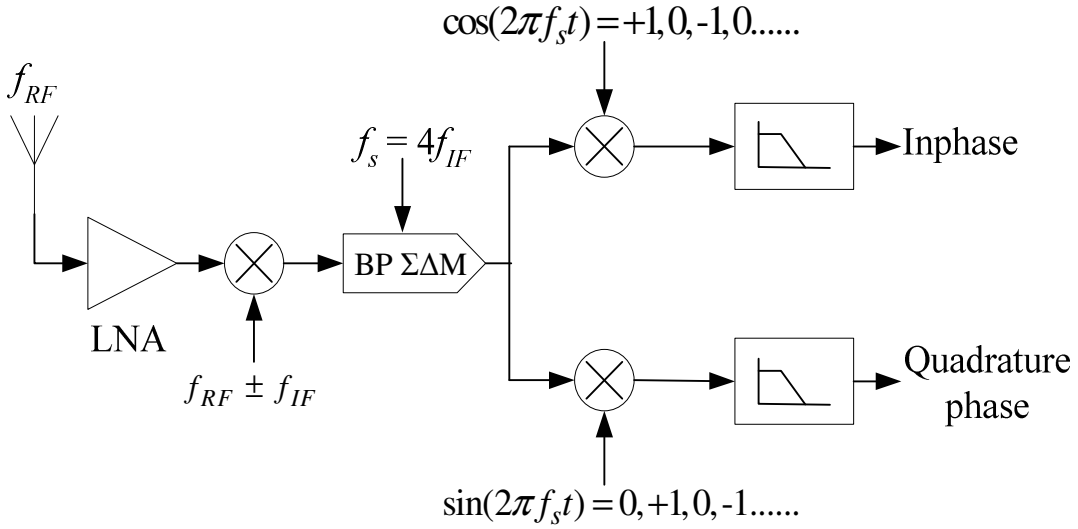


Figure 2.8: An application of BP ΣΔM

2.3.2 DT ΣΔMs Vs CT ΣΔMs

The bandpass loop filter in the ΣΔM can be implemented either as a Discrete-Time (DT) transfer function $H(z)$ using Switched-Capacitor (SC) [24] circuits or as a Continuous-Time (CT) transfer function $H(s)$ with transconductor-C [32] or LC [7] filters. A majority of reported ΣΔM are DT using switched capacitor loop filters. But to digitize signals at very high frequencies of GHz range continuous time modulator would be of a better choice for the reasons stated below.

1. At very high frequencies DT modulator becomes impractical as in that case the clock period is too short to charge the capacitors and to settle outputs of the op-amps of SC filters.
2. The sampling rate (f_s) of DT SC ΣΔM is limited to one-half or less of the unity gain bandwidth (f_u) of its opamps ($f_s < f_u/2$) [4]. However, it has been demonstrated that CT ΣΔM can have sampling rate greater than the unity gain bandwidth of its integrators ($f_s > f_u$) [10].
3. In a DT modulator, large glitches appear on op amp virtual ground nodes due to switching transients. While CT modulators are less prone to pickup digital noise.
4. To avoid aliasing, DT modulators usually require a separate anti-aliasing filter at their inputs as shown in Fig. 2.3. But in the case of CT modulators, the anti-aliasing is a built in inherent property of the modulator [32].
5. In a DT ΣΔM, the sampling occurs at the input and hence the sampling distortions are input referred, so they are not suppressed by the noise shaping behaviour of the feedback loop action. But in a CT modulator, sampling occurs inside the loop (described in the next chapter) and hence the sampling distortions

are shaped out of signal band by the noise shaping feedback loop action.

Considering the above facts, a continuous-time bandpass $f_s/4$ Sigma Delta modulator seems to be a better choice for digitizing at RF frequencies and to achieve the performance shown in Table 1.1 of Chapter 1.

2.3.3 Review of existing research in very high frequency CT ΣΔM

Hitherto research on design of very high frequency CT ΣΔM at gigahertz range has been an area which is very minimally explored. The literature search shows that all of the few reported implementations of such very high frequency Sigma Delta modulators were in bipolar RF transistors and no single implementation was in CMOS. This limits the monolithic integration of the ADC and the digital signal processing modules which are prevailingly designed in CMOS, on the same chip in a RF receiver. The table below shows the existing research work in very high frequency CT Sigma Delta modulator,

Table 2.1: Review of existing research in very high frequency CT ΣΔM

Design	Kaplan [21]	Cherry [7]	Jensen [45]	Raghavan [44]	Jayaraman [20]	Olmos [43]	Gao [42]
Process	InP HBT	0.5µm SiGe HBT	AlInAs / GaInAs SHBT	AlInAs / GaInAs HBT	AlGaAs / GaAs HBT	InGaP / InGaAs HEMT	0.5µm BJT
Type of modulator	4^{th} order Bandpass	4^{th} order Bandpass	4^{th} order Bandpass	4^{th} order Bandpass	4^{th} order Bandpass	2^{nd} order Lowpass	2^{nd} order Bandpass
f_s(GHz)	4.3	4	4	4	3.2	5	3.8
f_c(GHz)	1.3	1	0.21	0.18	0.8	0.04	0.95
f_b(MHz)	200	20	60	1	25	100	0.2
Performance (dB)	39 (SNDR)	37 (SNR)	50 (SNDR)	75.8 (SNDR)	41 (SNDR)	43 (SNR)	49 (SNDR)

2.4 Summary

The Sigma Delta modulator is a pulse density modulator, where the input signal is represented by the density of ones at the outputs. The fact that increasing the sampling frequency decreases in-band quantization noise is made used in the Sigma Delta modulator by oversampling the signal above Nyquist rate by an amount given by OSR. The in-band quantization noise is also further reduced by the noise shaping action of the feedback loop. The superiority of ΣΔMs over other Nyquist rate modulators by having less complex circuitry and more tolerance to component mismatch makes them suitable for very high frequency applications. Based on the reported work, a CT BP ΣΔM with $f_s/4$ as center frequency would be the better choice for sampling a bandpass signal at GHz frequencies in RF front ends.

Chapter 3

Continuous-Time Bandpass Sigma Delta Modulator: System Design and Simulation

This chapter discusses the design of continuous-time bandpass Sigma Delta modulator. The technique of transforming a DT ΣΔM into a CT ΣΔM according to the DAC pulse shape is explained by making use of impulse invariant transformation and state space method.

3.1 Equivalence of continuous-time and discrete-time modulator

A continuous time sigma delta modulator is shown in Fig. 3.1. Unlike a DT ΣΔM where the sampling occurs at the input as shown in Fig. 2.3, in CT ΣΔM the sampling occurs inside the feedback loop before quantization. The open loop transfer function of CT ΣΔM, from the output of the quantizer $y(n)$ to its input $x(n)$ is shown in Fig. 3.2. Due to the presence of a sampler inside the feedback loop, the continuous time open loop transfer function has an exact equivalent discrete time transfer function $H(z)$.

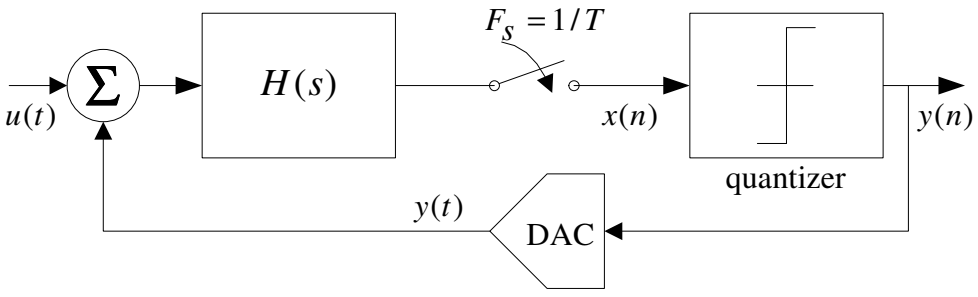


Figure 3.1: Block diagram of a continuous time Sigma Delta modulator

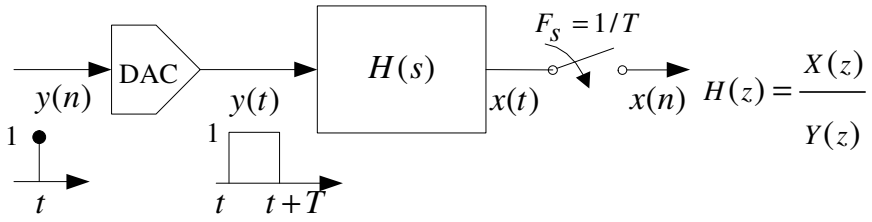


Figure 3.2: Open loop continuous time Sigma Delta modulator.

Hence the samples of the continuous time waveform at sampling instants as seen by the quantizer at its input is the same as the samples from a discrete time system of Fig. 2.3 with the equivalent DT transfer function $H(z)$ as the loop filter. In other words a DT modulator can be transformed into a CT modulator provided that the quantizer sees the same samples for both the modulators. This is called impulse invariant transformation and can be expressed as [14],

$$Z^{-1}\{H(z)\} = L^{-1}\{G_D(s)H(s)\}\Big|_{t=nT} \tag{3.1}$$

or in time domain [31],

$$h(n) = [g_D(t) \otimes h(t)]\,|_{t=nT} \tag{3.2}$$

ensuring that the quantizer sees the same samples for both DT and CT systems. Here, $G_D(s)$ is the impulse response of the DAC in feedback.

Due to the above equivalence of the DT and CT modulators, the noise shaping behavior, stability and other system performance of the continuous time ΣΔM can be designed and analyzed entirely in z domain. The resulting DT transfer function can be converted back to an equivalent CT system using the above impulse invariant transformation. It is worth noting that due to the presence of the impulse response of DAC in eq. (3.1), the transformation of a DT system to a CT system depends specifically on the feedback DAC pulse shape to be used.

3.2 Design of a bandpass continuous-time modulator

To design a continuous time modulator, we start with a discrete time lowpass transfer function which can be converted to a bandpass transfer function through the transformation [28],

$$z^{-1} \rightarrow -z^{-1}\frac{z^{-1}-\alpha}{1-\alpha z^{-1}}\text{ , where } -1 < \alpha < 1 \tag{3.3}$$

To reduce the complexity of the decimation filter which follows the ΣΔM and to simplify the mixing done in a radio receiver in digital domain (explained in Sec. 2.3.1), a sampling frequency of $f_s = 4f_o$, where f_o is the modulator center frequency is chosen. This corresponds to the special case of $\alpha = 0$ in eq. (3.3), leading to a low pass to bandpass transformation of $z^{-1} \rightarrow -z^{-2}$. The order of the bandpass transfer function obtained will be twice as that of the lowpass prototype, with the same SNR and identical stability properties. Applying the above transformation to a double integration low pass prototype,

$$H_{LP}(z) = \frac{-2z^{-1}+z^{-2}}{(1-z^{-1})^2} \rightarrow H_{BP}(z) = \frac{2z^{-2}+z^{-4}}{(1+z^{-2})^2} \tag{3.4}$$

$$H_{BP}(z) = z^{-1}.\hat{H}_{BP}(z)\text{, where } \hat{H}_{BP}(z) = \frac{2z^{-1}+z^{-3}}{(1+z^{-2})^2} \tag{3.5}$$

a bandpass modulator with the same performance and stability as the low pass prototype is obtained.

To implement the above mentioned bandpass modulator in eq. (3.4), in continuous time either a transconductance-C (G_m-C) filter or a LC resonator can be chosen. But the traditional G_m-C filters cannot handle very high frequencies due to its limited bandwidth, hence the later choice of LC resonator structures of the form $H(s) = As/(s^2+(\pi/2T)^2)$, is

chosen to implement the bandpass loop filter. Cascading two such resonators would give a fourth order bandpass transfer function, which could be used to implement the required $H_{BP}(z)$ in eq. (3.4), by applying a impulse invariant transform. Fig. 3.3 shows such a cascade, with a single feedback loop from a Non-return-to-Zero (NZ) DAC.

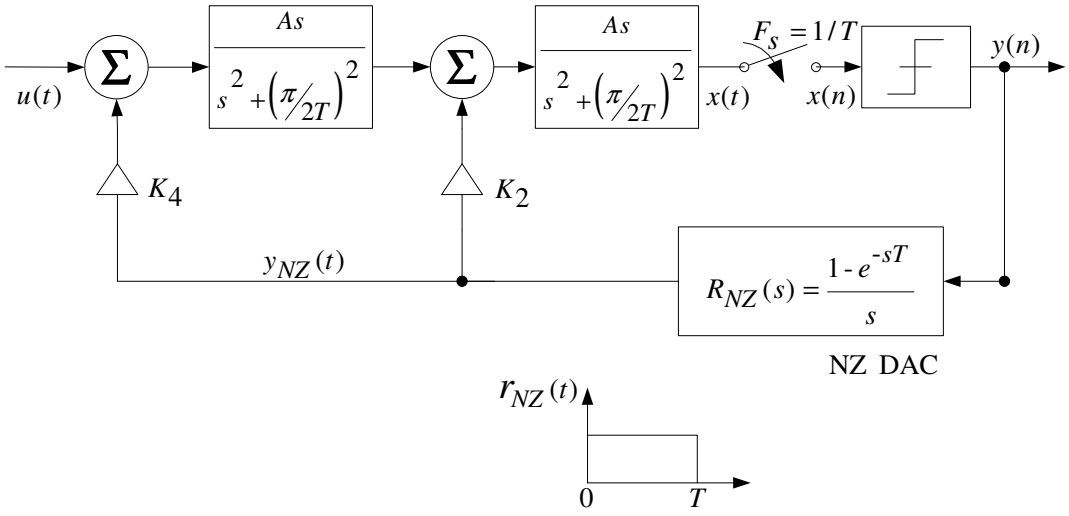


Figure 3.3: The fourth order bandpass CT ΣΔM which is not fully controllable.

This system is not fully controllable to implement the $H_{BP}(z)$ as discussed further. The NZ DAC time domain pulse and its impulse response are also given in Fig. 3.3. Assuming $A = \pi/2$ and normalizing the sampling time to T = 1, the open loop transfer function of the two loops that exist in Fig. 3.3 are,

$$K_2 \cdot Z\left[L^{-1}\left(R_{NZ}(s)H(s)\right)\Big|_{t=nT}\right] = K_2 \frac{z^{-1}\left(1-z^{-1}\right)}{1+z^{-2}} \tag{3.6}$$

second order loop with $R_{NZ}(s)$,

$$K_4 \cdot Z\left[L^{-1}\left(R_{NZ}(s)H(s)H(s)\right)\Big|_{t=nT}\right] = K_4 \frac{0.7854z^{-1}\left(1-z^{-1}-z^{-2}+z^{-3}\right)}{\left(1+z^{-2}\right)^2} \tag{3.7}$$

fourth order loop with $R_{NZ}(s)$,

following the impulse invariant transformation, if we apply superposition to the above two open loops and equate them to $H_{BP}(z)$ as in eq. (3.4), we end up in a situation were there are four numerator coefficients, but only two independent variables K_2 and K_4 to control them. In other words eq. (3.8) below cannot be solved

$$K_2 \frac{z^{-1}\left(1-z^{-1}\right)}{1+z^{-2}} + K_4 \frac{0.7854 z^{-1}\left(1-z^{-1}-z^{-2}+z^{-3}\right)}{\left(1+z^{-2}\right)^2} = \frac{2z^{-2}+z^{-4}}{(1+z^{-2})^2} \qquad (3.8)$$

and so impulse invariance cannot be applied to the above modulator in Fig. 3.3 because the system is not fully controllable.

Hence a multi-feedback continuous time bandpass architecture [30] as shown in Fig. 3.4 is used to implement the fourth order discrete time transfer function $H_{BP}(z)$.

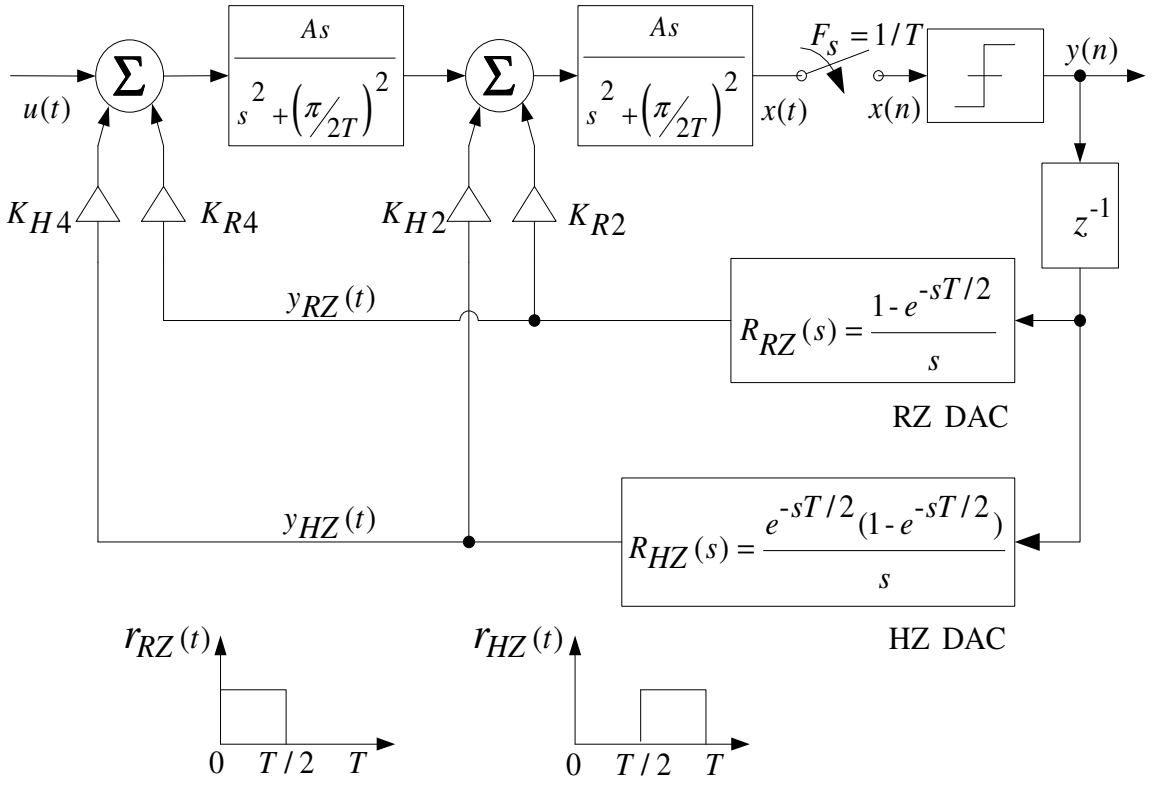


Figure 3.4: A multi feedback CT bandpass ΣΔM architecture.

The DACs in the feedback produce a Return-to-Zero (RZ) and Half-return-to-Zero (HZ) pulse waveforms. The $r_{RZ}(t)$ and $r_{HZ}(t)$ waveforms with their respective impulse responses $R_{RZ}(s)$ and $R_{HZ}(s)$ are also shown in Fig. 3.4. Assuming again $A = \pi/2$ and normalizing the sampling time to $T = 1$, the loop transfer functions of the four loops that exist in the multi feedback architecture are [31],

$$K_{R2} \cdot Z \left[L^{-1}(R_{RZ}(s)H(s)) \Big|_{t=nT} \right] = K_{R2} \frac{z^{-1}\left(\left(1-\frac{1}{\sqrt{2}}\right)-\frac{1}{\sqrt{2}}z^{-1}\right)}{1+z^{-2}} \tag{3.9}$$

second order loop with $R_{RZ}(s)$,

$$K_{H2} \cdot Z \left[L^{-1}(R_{HZ}(s)H(s)) \Big|_{t=nT} \right] = K_{H2} \frac{z^{-1}\left(\frac{1}{\sqrt{2}}-\left(1-\frac{1}{\sqrt{2}}\right)z^{-1}\right)}{1+z^{-2}} \tag{3.10}$$

second order loop with $R_{HZ}(s)$,

$$K_{R4} \cdot Z \left[L^{-1}(R_{RZ}(s)H(s)H(s)) \Big|_{t=nT} \right] = K_{R4} \frac{z^{-1}\left(0.5077 - 0.8330z^{-1} + 0.0476z^{-2} + 0.2777z^{-3}\right)}{\left(1+z^{-2}\right)^2} \tag{3.11}$$

fourth order loop with $R_{RZ}(s)$,

$$K_{H4} \cdot Z \left[L^{-1}(R_{HZ}(s)H(s)H(s)) \Big|_{t=nT} \right] = K_{H4} \frac{z^{-1}\left(0.2777 + 0.0476z^{-1} - 0.8330z^{-2} + 0.5077z^{-3}\right)}{\left(1+z^{-2}\right)^2} \tag{3.12}$$

fourth order loop with $R_{HZ}(s)$.

The feedback coefficients K_{R2}, K_{H2}, K_{R4}, K_{H4} can be obtained by applying superposition to the four feedback paths in eq. (3.9), (3.10), (3.11) and (3.12) then equating them to the DT bandpass transfer function $\hat{H}_{BP}(z)$ as in eq. (3.5). In order to implement $H_{BP}(z)$, the remaining z^{-1} in eq. (3.5) is realized digitally in the feedback loop as shown in Fig. 3.4, with two latches. This reduces quantizer metastability by providing enough regeneration time for the quantizer to resolve small inputs.

3.3 Designing the modulator using state space technique

Alternatively, the coefficients can be calculated using State-Space technique [27].

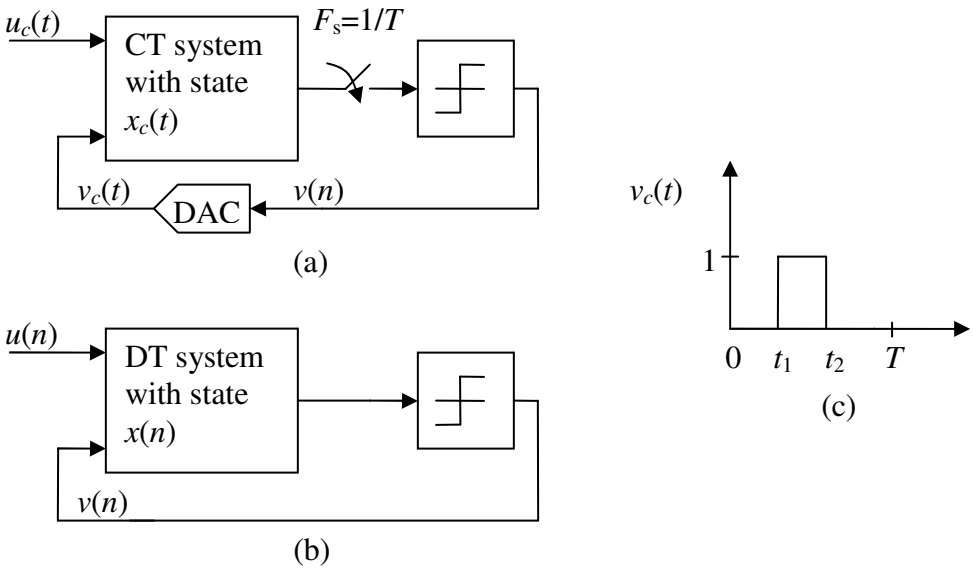


Figure 3.5: State space representation of ΣΔM

(a) Continuous time modulator (b) Discrete time modulator
(c) DAC pulse of the CT modulator

The state equations for the linear parts of the continuous time modulator shown in Fig.3.5 (a) is,

$$x_c'(t) = A_c x_c(t) + B_c \begin{bmatrix} u_c(t) \\ v_c(t) \end{bmatrix} \tag{3.13}$$

where $x_c(t)$ is vector of N states of the modulator and $x_c'(t)$ being its time derivative. A_c is a $N \times N$ matrix, B_c is a $N \times 1$ vector, $u_c(t)$ is the input to the modulator and $v_c(t)$ is the DAC pulse. Correspondingly the state equation for the linear parts of discrete time modulator shown in Fig. 3.5(b) is,

$$x(n+1) = A_d x(n) + B_d \begin{bmatrix} u(n) \\ v(n) \end{bmatrix} \tag{3.14}$$

If the DAC waveform $v_c(t)$ is of the form shown in Fig. 3.5(c), then the continuous and discrete systems are equivalent provided,

$$A_d = e^{A_c} \text{ and } B_d = A_c^{-1}\left(e^{A_c(1-t_1)} - e^{A_c(1-t_2)} \right) B_c \tag{3.15}$$

With the help of MATLAB 'c2d' function one can easily find the zero order hold discrete equivalent of a continuous time system. The B_d matrix of the result can be modified according to eq. (3.15), so as to incorporate the DAC pulse shape. Note that for RZ pulse shape $t_1 = 0$ and $t_2 = 0.5$, while for HZ pulse $t_1 = 0.5$ and $t_2 = 1$ in eq. (3.15) (assuming a normalization of sampling frequency to 1Hz). The MATLAB code to solve the above four equations (3.9), (3.10), (3.11) and (3.12) in state space is given in Appendix A.

3.4 System modeling and simulation

Using MATLAB the above multi feedback architecture was simulated with a Simulink model [34] as shown below in Fig. 3.6. The RZ and HZ DACs were modeled with S-functions (given in Appendix B) as available in Simulink. The power spectral density of the output bit stream is shown in Fig. 3.7 and the Dynamic Range (DR) is also plotted in Fig. 3.8. Using the ideal model, a DR of 90dB with a signal of bandwidth 500 kHz

centered at 1GHz is achieved (at a bandwidth of 20MHz a DR of 62dB is obtained), while sampling at 4GHz frequency.

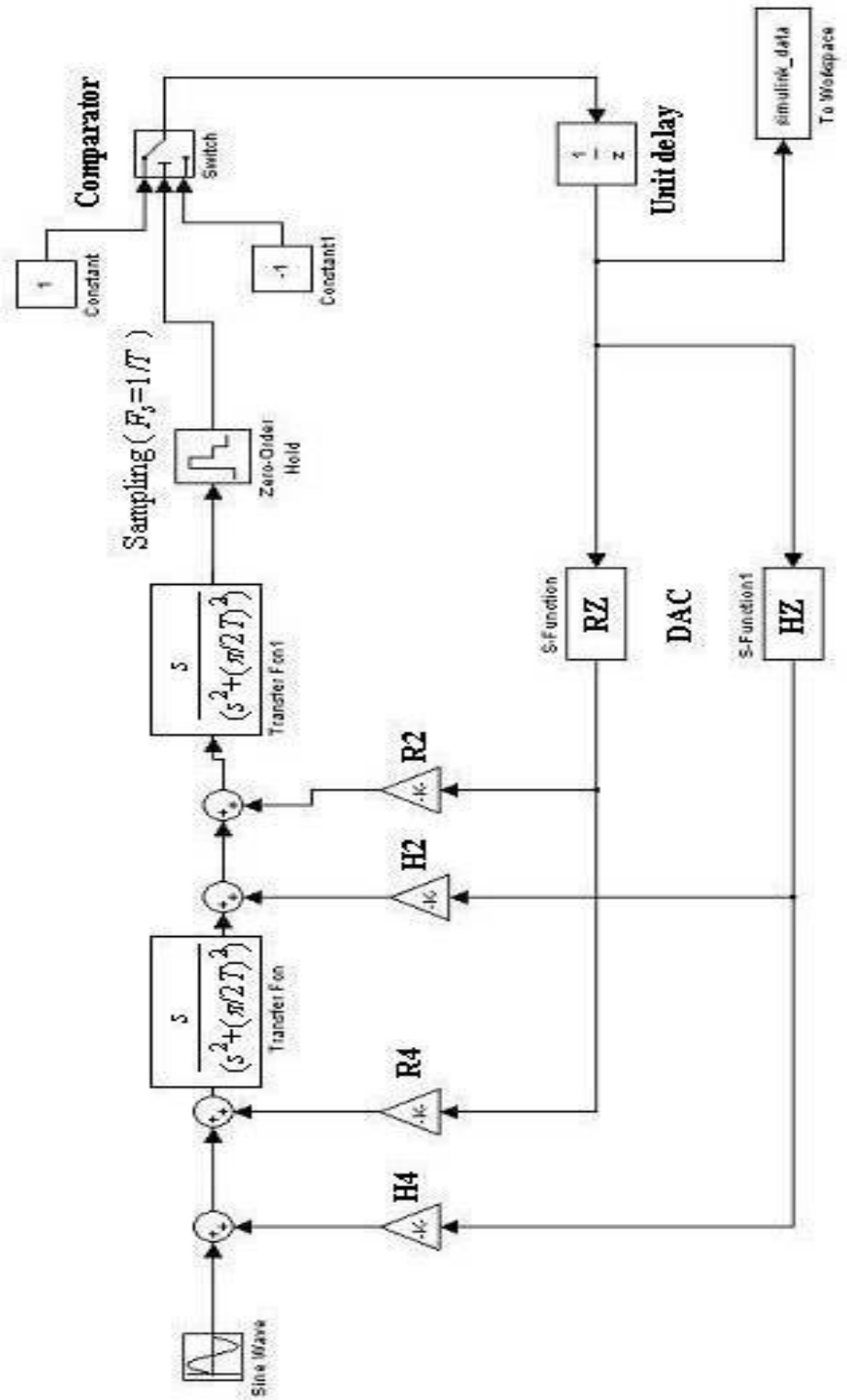


Figure 3.6: Ideal Simulink model of the multi feedback CT ΣΔM.

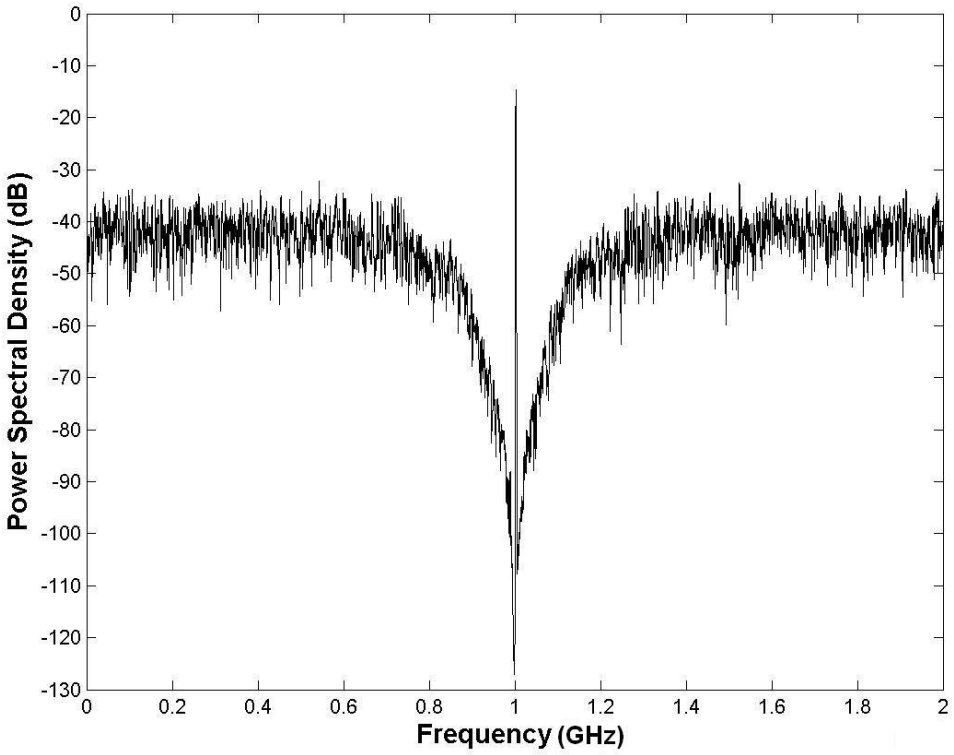


Figure 3.7: Power spectral density of output from Simulink model

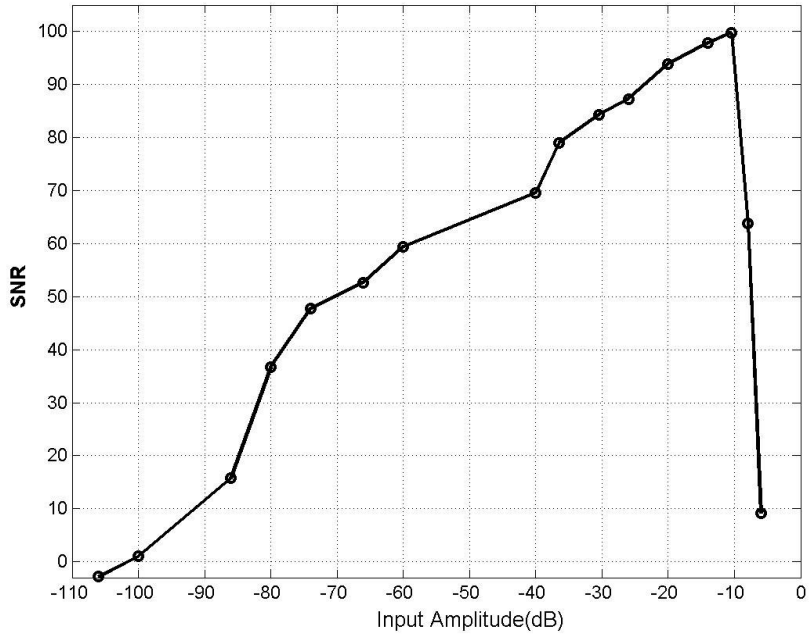


Figure 3.8: Dynamic range plot for the Simulink model of CT ΣΔM.

3.5 Summary

A better and easier way to design a CT ΣΔM is to choose a DT loop filter transfer function which meets the performance specifications, and then transform it to a CT loop filter using the impulse-invariant transformation based on the CT ΣΔM DAC pulse shape. At very high frequencies LC resonators are used to implement bandpass loop filters to obtain a BP CT ΣΔM. When using LC resonators in designing a fourth order bandpass modulator, two feedback paths with different DAC pulse shapes should be employed to have a fully controllable system. Its is easier to use MATLAB built in functions in designing the BP CT ΣΔM using impulse-invariant transformation through state space technique.

Chapter 4

Non-Idealities of Continuous-Time Sigma Delta Modulator and Design Issues at High Frequencies

Ideal conditions are assumed in the design of multi feedback architecture shown in Fig. 3.4 and in the Simulink model shown in Fig. 3.6. However there are many practical non-idealities to be taken care of while realizing the CT ΣΔM in circuit. In this chapter, some of the non-idealities which are very specific to CT ΣΔM are discussed along with design issues of MOSFET in high frequencies.

4.1 Loop delay and modulator stability at very high frequencies

Ideally, the DAC in the feedback of Fig. 3.4 responds immediately to quantizer clock edge. But in practice, transistors in the latch implementing unit delay and that in the DAC cannot switch instantaneously (explained in Sec. 4.5 below). Thus, there always exists a delay between the quantizer clock and DAC pulse. This delay is called the loop delay.

The loop delay changes the CT modulator open loop response at sampling instances which were assumed ideal in Fig. 3.2. However, in a DT modulator, say a switched capacitor modulator, the op amp output voltage is sampled after a safe margin of settling which includes delays caused by switching of transistors in latches and DACs. Therefore, in a DT modulator only the voltage levels at the time of sampling is important. Hence loop delay will not affect a DT modulator.

Consider a loop delay of τ_d in the RZ DAC pulse as shown in Fig. 4.1, where the sampling instance is assumed to be at $t = 0$.

Figure 4.1: Delay in RZ DAC pulse.

This loop delay can be expressed as a fraction of sampling time [8],

$$\tau_d = \delta_d T \tag{4.1}$$

The value of τ_d depends on the switching speed of the transistor f_T, the sampling clock frequency f_s and the number of transistors in feedback loop n_t. With all the transistors in the feedback to switch fully after $1/f_T$ the fraction δ_d can be approximately expressed as,

$$\delta_d \approx \frac{n_t f_s}{f_T} \tag{4.2}$$

Applying the above to a modulator implemented in a 0.18μm MOS process of f_T = 49GHz [25] with a sampling frequency f_s = 4 GHz and having about n_t = 3 transistors in feedback loop, the loop delay would be 24%. Such an amount of loop delay is enough to make the modulator unstable. Hence care must be taken in designing high speed modulators in order to have a stable system.

The extra loop delay in the feedback can be modeled as $e^{-s\Delta T}$ in the open loop response of the modulator where $0 \le \Delta T \le$ T. The loop delayed open loop of CT ΣΔM is shown in Fig. 4.2. Delaying the CT signal $x(t)$ by an amount ΔT requires the information between sampling instants, hence modified z-transform is used to convert the delayed CT signal $x(t-\Delta T)$ to DT. $X(z,m)$ provides the information between the sampling instants of the CT signal $x(t-\Delta T)$. The modified z-transform $X(z,m)$ is given by [22],

$$X(z,m) = z^{-1}\sum_{n=0}^{\infty} x[(n+m)T]z^{-n} \tag{4.3}$$

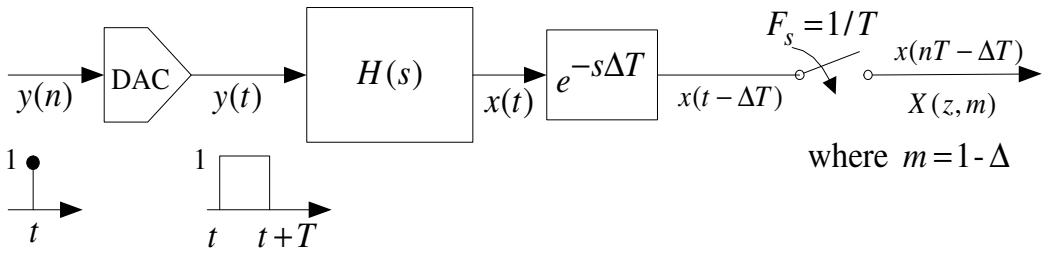


Figure 4.2: Open loop CT ΣΔM with excess loop delay.

In Sec. 3.1 it was explained that the open loop CT ΣΔM has an exact equivalent DT transfer function $H(z)$ and the modulator was implemented by following impulse invariant transformation i.e. the open loop impulse response of CT ΣΔM and the impulse response of the DT transfer function remains the same in time domain (from eq.(3.2)). To examine the effect of loop delay on the CT ΣΔM implemented with the multi feedback architecture of Fig. 3.4, the modified z transform of the time domain impulse response of $H_{BP}(z)$ in eq.(3.4) is obtained,

$$H_{BP}(z,m) = Z_m\left(Z^{-1}\left[\frac{2z^{-2}+z^{-4}}{(1+z^{-2})^2}\right]\right) \tag{4.4}$$

the noise transfer function of the above loop delayed CT ΣΔM is,

$$NTF(z,m) = \frac{1}{(1+H(z,m))} \tag{4.5}$$

$$NTF\left(z,m\right) = \frac{z\left(1+z^2\right)^2}{z^5 + a_3 z^3 + a_2 z^2 + a_1 z + a_0} \tag{4.6}$$

where,
$a_3 = 2 - (0.5(m+3)\sin(m\pi/2))$
$a_2 = -0.5(m+1)\cos(m\pi/2) - 1.5\sin((1-m)\pi/2)$
$a_1 = 1 - (0.5(m+1)\sin(m\pi/2))$
$a_0 = 0.5(1-m)\cos(m\pi/2)) - 1.5\sin((1-m)\pi/2)$

which shows that the fourth order modulator in the presence of loop delay becomes a fifth order system. Plotting the root locus of *NTF*(*z*,*m*) as shown in Fig. 4.3, we can conclude that for a excess loop delay of 22% in the feedback loop, the modulator is no longer stable. Excess loop delay also degrades the modulator performance by increasing the in-band noise and decreasing the maximum stable amplitude there by bringing down the dynamic range [8].

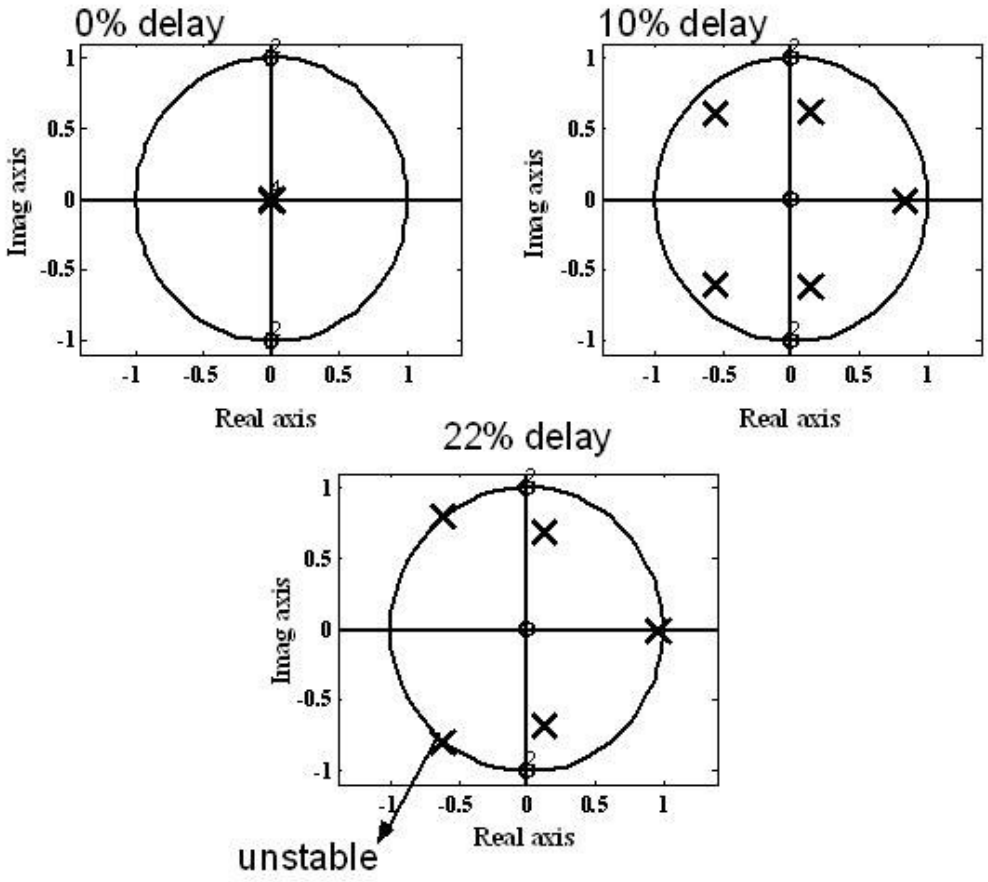


Figure 4.3: Root locus of the noise transfer function *NTF*(z,*m*)

The ideal MATLAB Simulink model shown in Fig. 3.6 was modified to include the loop delay in its feedback. Loop delay was incorporated into the RZ and HZ DAC output waveforms and the modulator was simulated to examine the effects of loop delay on the

output spectrum. Fig 4.4 shows the power spectral density of output bit stream of the loop delayed CT ΣΔM. The peaking in the noise spectrum is due to the fact that the poles of the noise transfer function moves towards the unit circle as explained in Fig. 4.3. It is also worth noting that the in-band noise of the power spectrum increases to about -80dB as compared to -120dB in the ideal modulator shown in Fig. 3.7, hence decreasing the SNR and dynamic range of the modulator.

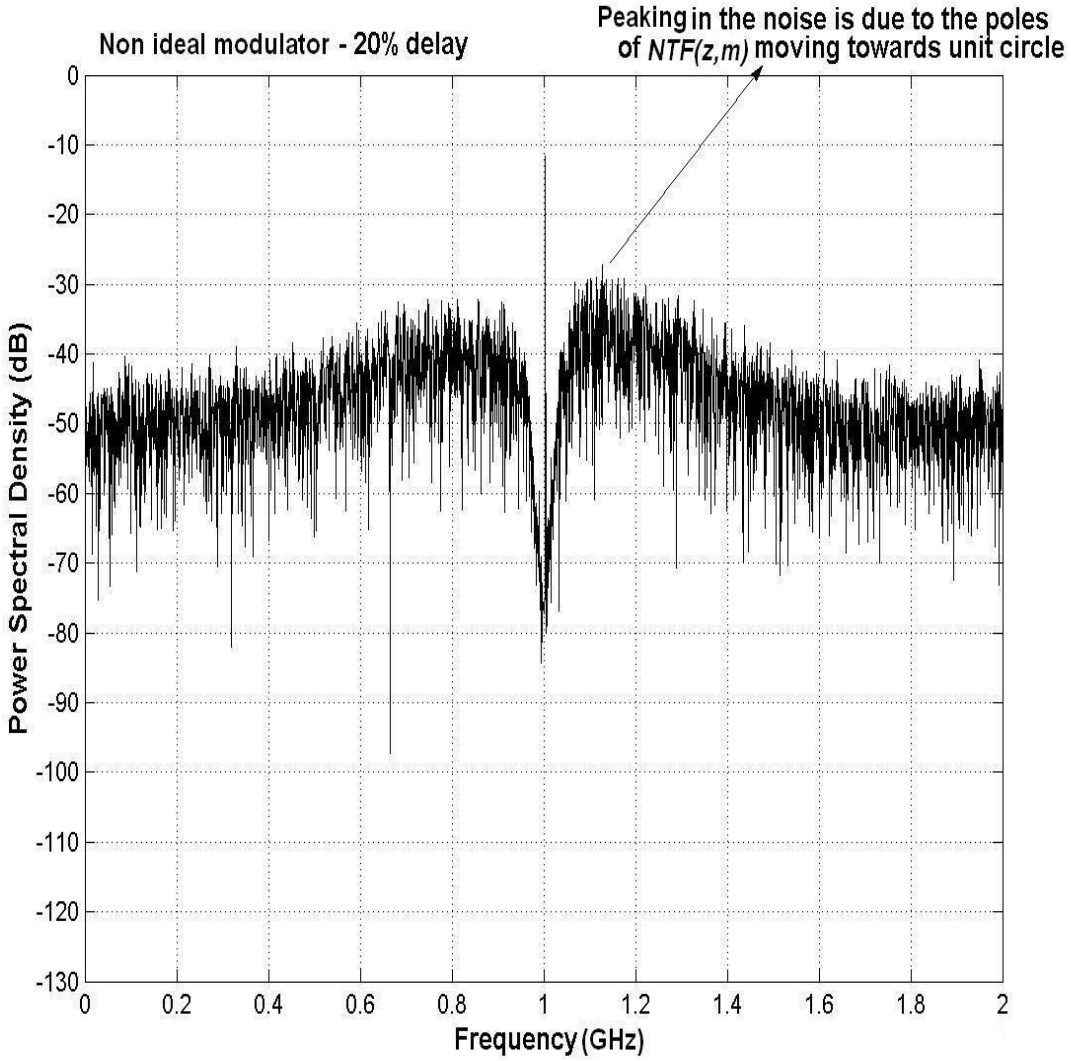


Figure 4.4: Power spectral density of the output from a loop delayed CT ΣΔM.

4.2 Clock jitter effects on SNR

A jitter in the sampling clock is the random variation in clock pulse edges as shown in Fig. 4.5, which are suppose to be at constant intervals for a particular clock frequency f_s.

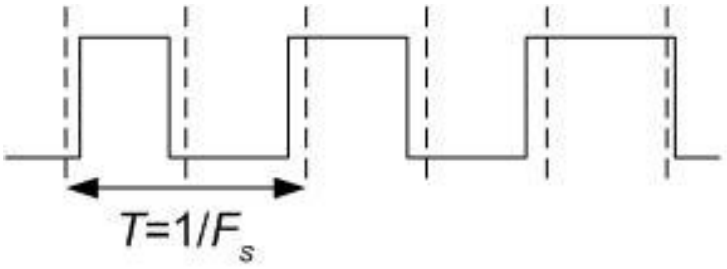


Figure 4.5: A jitter in the sampling clock.

When the signal is sampled with such a jittered clock, the RZ DAC pulse waveform of the feedback loop for the modulator output bit sequence '110' would appear to be as shown in Fig. 4.6(a). Jittered NZ DAC pulse for the same output bit sequence is also shown in Fig. 4.6(b). The edges are shown shaded instead of straight lines since the exact moment of transition is not know due to clock jitter. From the Fig. 4.6 it is clear that for a CT modulator the charge is transferred at a constant rate over a clock period. Hence a larger amount of charge Δq is lost for a sampling period. However in a DT modulator most of the charge of the feedback pulse is transferred at the start of the clock period, so that this loss of Δq is very less when compared to the total charge transferred. Moreover, in a DT design, jitter in the input sample-and-hold clock means only the input waveform is affected. But in a CT design, the sampling occurs at the quantizer rather than the input, which affects the sum of the input plus quantization noise. Hence, CT ΣΔMs are more sensitive to clock jitter compared to DT modulators.

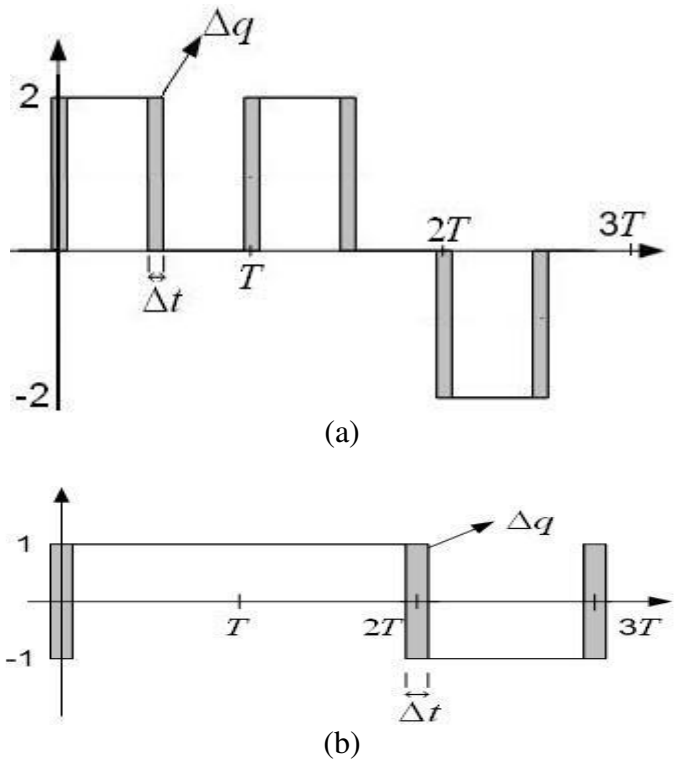


Figure 4.6: DAC pulse due to a jittered sampling clock
(a) RZ DAC (b) NZ DAC

Clock jitter causes a slight random variation in the amount of charge fed back per clock cycle which in turns adds a random phase modulation to the output bit stream. This random phase modulation causes the noise outside the signal band to fold into the signal band, raising the spectrum noise floor and degrading the SNR. Since clock jitter introduces a random phase modulation which has no signal-dependency, no harmonic distortion appears while affecting only the dynamic range.

Assuming the two waveforms of Fig. 4.6 are for two equivalent designs, the output value of the RZ waveform is doubled to supply the same amount of charge compared to the NZ pulse with one symbol. From the comparison of the two waveforms it can be seen that a NZ DAC is affected by this random jitter only when a transition occurs, this introduces a signal-dependency of the jitter power in the DAC output. While in the RZ

DAC for every clock period two transitions with twice the jitter power occurs no matter whatever the modulator output bit sequence may be. Hence it can be concluded that a loss of dynamic range due to clock jitter is signal-dependent for NZ DACs [9] while it is signal-independent, but 6dB larger for RZ DACs.

For the single-bit DACs, if the SNR is completely limited by white jitter noise rather than noise-shaped quantization noise, then for an input amplitude of V_{in}, the SNR can be calculated by [29],

$$\text{SNR} = 10\log_{10}\frac{\text{OSR}\left(V_{in}^2/2\right)}{\sigma_{\delta y}^2\left(\sigma_j/T\right)^2}\text{dB} \tag{4.7}$$

where $\sigma_{\delta y}$ is the density of transitions in the output bit stream, σ_j^2 is the variance of the zero-mean, normally-distributed clock jitter. The value of $\sigma_{\delta y}$ is 2.8 for NZ pulse, 8 for RZ pulse and 24.1 [9] for modulators using both RZ and HZ pulses like the multi feedback architecture of Fig. 3.4.

Generally, clock jitter affects RZ and/or HZ modulators more severely than modulators employing NZ DAC feedback alone.

4.3 Variation of DAC pulse shape due to quantizer metastability

The MATLAB Simulink model of CT ΣΔM of Fig. 3.6 assumes an ideal quantizer, which has no hysteresis and the decision occurs instantly. However practical quantizers suffer from three non idealities shown in Fig. 4.7 are as follows:

1. Propagation delay, which is due the switching delay time of the transistors (will be discussed in Sec. 4.5). The effect of this delay is to increase in-band noise and also affects the modulator stability if not maintained within a certain limit (as

explained in Sec. 4.1).

2. Hysteresis, which is the smallest signal which the quantizer can resolve. Inputs below this value are not enough to create an imbalance in the quantizer positive feedback, so that the output can change to reflect its quantization. As a result, for these inputs the delay is assumed to be infinite as shown in Fig. 4.7. Due to hysteresis the swing of the input signal to quantizer is increased. This is because, as long as the quantizer output bit stream remains the same (due to its inability to resolve very small inputs), the circuitry inside the loop will continue integrating in the same direction leading to larger signal swings. Larger signal swings could lead to signals being clip by the circuit introducing harmonic distortion and degrading stability as well.
3. Metastability, which is the dependence of the regeneration time of quantizer with its input signal. The curve in the practical quantizer characteristics of Fig. 4.7 is due to metastability. The area under the curve indicates the amount of metastability a quantizer has. It is this metastability which changes the shape of the DAC pulses and hence affecting the modulator performance.

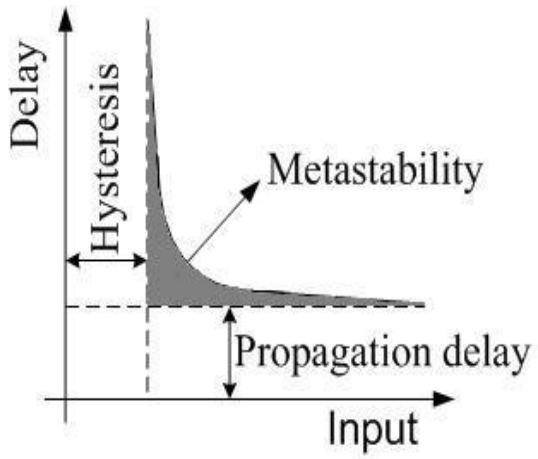


Figure 4.7: Non ideal quantizer characteristics.

The real quantizer contains a regenerative circuit with a finite regeneration gain. Therefore, quantizer inputs with a magnitude near zero will take longer time to resolve than inputs with a large magnitude. This makes the rail-to-rail pulses of quantizer output to have a propagation delay which is dependent on quantizer input signal amplitude. If a dynamic comparator is used as the quantizer, then regeneration occurs only for half the time period of sampling clock. While in the next half period of the clock, the outputs of the quantizer will be reset to either one of the logic levels, by this way a RZ or HZ waveform is generated. The output waveform from such a dynamic quantizer for the bit sequence '110' would appear to be as in Fig. 4.8, where a reset to logic low is assumed. Due to reset, the falling edge of the pulse shown is fixed by the sampling clock (which is assumed be jitter free) exactly at the start of every half time period. But the rising edge of the pulse is determined by the regeneration time of the comparator. Hence the rising edge occurs faster for larger quantizer inputs, while slower for smaller quantizer inputs. This changes the pulse width according to the quantizer input amplitude. When such a pulse drives the DACs (which are usually switched current type), the resultant RZ and HZ pulses also has a width variation accordingly.

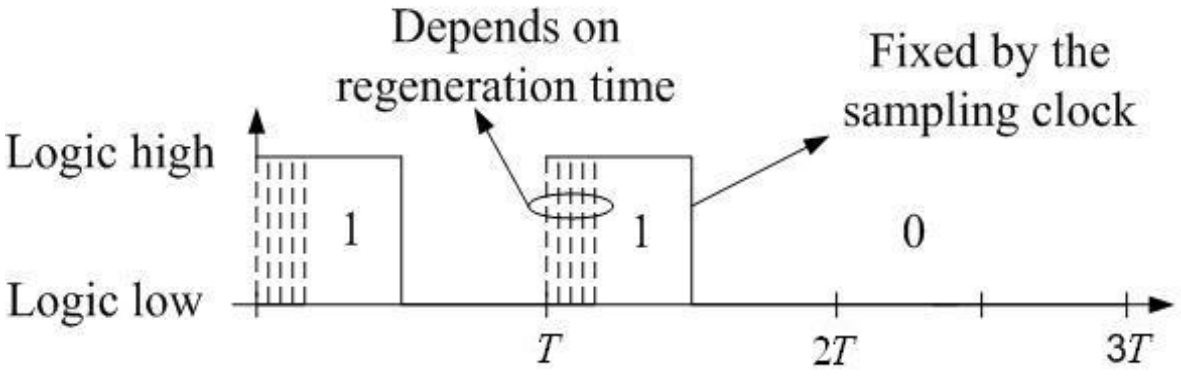


Figure 4.8: DAC pulse width variation due to quantizer metastability.

A real quantizer driving a DAC was simulated in HSpice and the DAC pulse width variation is shown in Fig.4.9. It is evident that as the input amplitude increases the rising edge occurs faster and the pulse width is longer. Another interesting fact is that, when the rising edge occurs faster then the pulses experience a longer regeneration time leading to larger pulse amplitudes. Hence we can also conclude that quantizer metastability not only changes DAC pulse width but also its height.

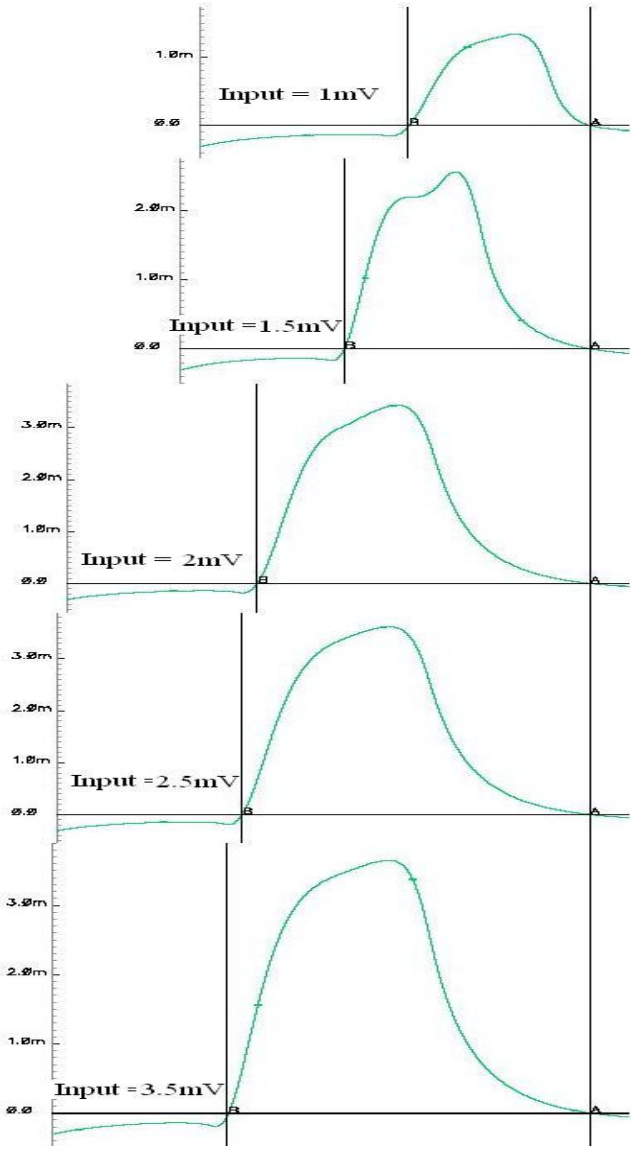


Figure 4.9: Simulation of quantizer metastability

In a ΣΔM, the input to the quantizer is decorrelated from the modulator input to the degree that it appears random. Hence the times when the quantizer input is near zero also appears random. In other words at certain unpredictable random sampling instants, slightly more charge is transferred for the previous clock period and slightly less for the next period due to DAC pulse shape variation. This effect is similar to that of having a jittered clock and hence similar spectral whitening in the signal band results. The SNR can also be calculated as that of a clock jitter as in eq. (4.7).

4.4 Inter-symbol interference with unequal DAC rise/fall time

In general, CT ΣΔMs are sensitive to the exact shape of the DAC pulse, any non uniformity of the pulse shape will lead to performance degradation. An unequal rise and fall time in the DAC switching is one effect difficult to control by circuit techniques. Consider a NZ DAC waveform shown in Fig. 4.10 of a CT ΣΔM, where for illustrative purpose the rise time is assumed to be τ and the fall time is assumed zero.

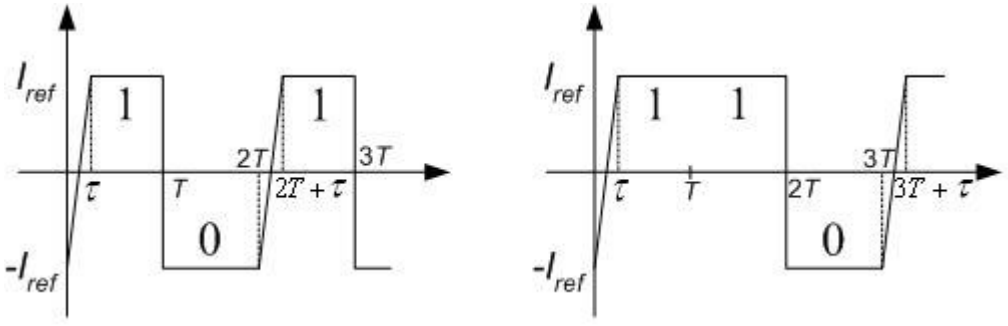


Figure 4.10: NZ DAC waveform asymmetry.

The DAC output for two bit-stream sequences ‘101’ and ‘110’ are analyzed. If the rise and fall times are identical (τ = 0), the charge delivered to the CT loop filter by both sequences would be,

$$Q_{101} = Q_{110} = I_{ref}T \tag{4.8}$$

With switching asymmetry however, the two waveforms change their charge content to,

$$\begin{aligned} Q_{101}^{\tau} &= I_{ref}\left(T - 2\tau\right) \\ Q_{110}^{\tau} &= I_{ref}\left(T - \tau\right) \end{aligned} \tag{4.9}$$

Since the bit-stream driving the DAC output contains both quantization noise and input signal, the charge delivered by the DAC becomes signal-dependent when $\tau \neq 0$. This signal dependency generates harmonics in the output spectrum reducing the peak SNDR. Further, the charge delivered with one symbol is not only dependent on the symbol itself but also on the previous symbol, hence it gives rise to inter-symbol interference. Since the DAC pulse errors are fed back all the way to the modulator input, they become input referred and hence are not noise-shaped by the action of the feedback loop. The maximum asymmetry that a modulator can have to achieve a desired SNR is given by [1],

$$\tau \leq \frac{4T\sqrt{\mathrm{OSR}}}{\mathrm{SNR}_{\mathrm{desired}}} \tag{4.10}$$

where T is the sampling clock period.

The following are the remedies to overcome the above problem,

1. When designing the modulator in circuit choose a differential configuration rather than a single ended one.
2. Use RZ or HZ DAC pulses instead of NZ DAC pulse. Unlike NZ pulse, a RZ pulse resets to zero for every half of the clock. In this way, independent of the quantizer decision, both a rising and a falling edge appear in the DAC pulse. Furthermore, the inter-symbol interference is reduced because no matter the previous quantizer decision, a new DAC output starts from the same reset value.

To reduces the above problem in the multi feedback architecture designed before in Sec. 3.2, we use a RZ and HZ DAC pulse combination, even though the other options of using a RZ and NZ or a HZ and NZ combination exits.

4.5 MOSFET Vs Bipolar in very high frequencies

As mentioned previously in Sec. 1.2, very high frequency ADCs of sampling frequencies in GHz range were implemented largely in BJT. The reason behind is that there are four important differences between a bipolar transistor and a MOSFET device that makes the latter less suitable for high-frequency applications [12]:

1. For the same current, the transconductance of a MOSFET is much smaller than that of a bipolar transistor.
2. The cut-off frequency (f_T) of a MOSFET is much smaller than that of a bipolar transistor.
3. For the same transconductance, the parasitic capacitances of a MOSFET are larger.
4. A MOSFET acts as a delay line.

4.5.1 MOSFET cut-off frequency (f_T)

The cut-off frequency or the transition frequency (f_T) is a first figure of merit for a transistor at high frequency applications. It is the frequency at which the magnitude of the short circuit, common-source current gain, falls to unity. For an n-MOSFET in strong inversion following square law model, the f_T can be defined as [15],

$$f_T = 1.5\frac{\mu_n}{2\pi L^2}\left(V_{GS} - V_t\right) \tag{4.11}$$

and that for a bipolar transistor,

$$f_T = 2\frac{\mu_n}{2\pi {W_B}^2} V_T \tag{4.12}$$

From the above two equations it is evident that for a MOSFET the f_T is inversely proportional to L^2, hence devices of shorter channel lengths are preferred for high frequency applications. To have higher f_T the operating bias point ($V_{GS} - V_t$) of MOSFET can be increased, but at the same time not degrading its g_m/I ratio which is inversely proportional to the overdrive voltage ($V_{GS} - V_t$). Note that the base width W_B in a bipolar transistor is a vertical dimension determined by diffusions or implants and can typically be made much smaller than the channel length L of an MOSFET transistor, which depends on surface geometry and photolithographic processes. Thus bipolar transistors generally have higher f_T than MOSFET transistors made with comparable processing. For an n-MOSFET of L = 0.36μm and over drive voltage of 1V, the f_T is about 23GHz [11].

4.5.2 Delay-line effects in a MOSFET

When the voltage applied to the gate contact (Fig. 4.11) changes, the MOSFET takes some time to modify the channel charge distribution and the drain current. This delay consists of two components:

1. The gate resistor forms a lossy distributed delay line with the gate capacitance. When the voltage at the gate contact changes, the gate signal needs some time to travel along the gate width. The delay time is given by,

$$\tau_g = \frac{1}{3} R_{gate} C_{gate} \approx 0.22 W^2 . \rho . C_{ox} \tag{4.13}$$

where W is the transistor width, ρ is the gate sheet resistance and C_{ox} is the gate oxide capacitance per unit of area. Since the delay is proportional with W^2, it can be concluded that a MOSFET for high frequency applications not only needs to be short but it should also be narrow as well. Wide transistors have to be split up into narrow fingers while layout.

2. After the gate signal has arrived at the transistor, it takes time to modify the channel charge distribution. In other words the transconductance of the MOSFET becomes frequency dependent. This delay time is given by,

$$\tau_c = 0.064 / f_T \tag{4.14}$$

The combined total delay of the MOSFET transistor to respond to a signal applied to the gate adds a phase shift and affects stability of the system.

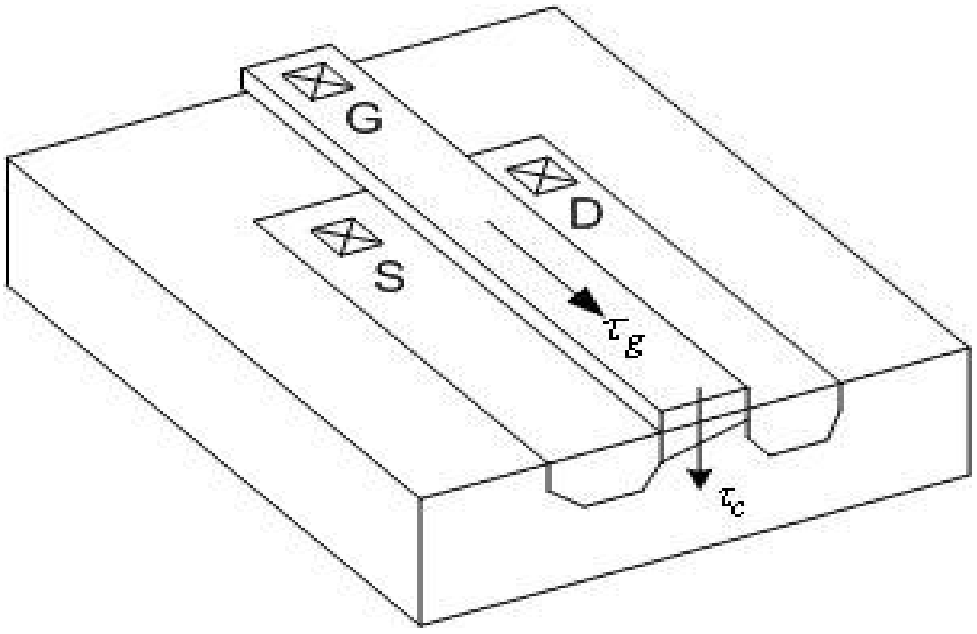


Figure 4.11: The delay in a MOS transistor to respond to a signal applied to its gate.

4.6 Summary

A practical CT ΣΔM experiences non-idealities at high frequencies, which affects its performance. Loop delay, which arises in the feedback loop due to delay line effects of transistors at high frequencies increases the in-band noise and most importantly makes the modulator unstable. Hence the feedback loop delay should be kept below 22% of the sampling clock period in order to get a stable system. A jitter in the sampling clock would introduce random phase modulation to the output bit stream and raise the noise floor, degrading the SNR. Further, the feedback DAC pulse shape is affected by quantizer metastability which in turn whitens the in-band noise spectrum and again degrading the SNR. Finally, it is better use a RZ and HZ DAC pulse than a NZ pulse, since NZ pulses suffer inter-symbol interference due to unequal DAC fall/rise time.

Chapter 5

The Implementation of 4th Order LC Bandpass Modulator in Circuit

With the design of an ideal modulator and its non-idealities given in previous chapters, this chapter deals with the circuit implementation of the fourth order LC bandpass continuous-time Sigma Delta modulator. The multi feedback architecture as shown in Fig. 3.4 is used as the basic architecture and while realizing it in circuit we do some modification to take into account the effects of the non-idealities explained in the previous chapter.

5.1 Modulator circuit topology

The multi feedback architecture as shown in Fig. 3.4 is implemented using circuit with the topology as shown in Fig. 5.1. The input transconductor G_{m1} converts the input voltage v_{in} into current $i_{in} = G_{m1} * v_{in}$, which drives the parallel LC resonator circuit of impedance, $Z_{LC} = 1 / (Cs + (1/Ls))$. The output voltage of the resonator is,

$$V_o = I_{in} Z_{LC} = \frac{G_{m1} V_{in}}{(Cs + (1/Ls))} = \frac{s(G_{m1}/C)}{(s^2 + (1/LC))} V_{in} \tag{5.1}$$

which is a second order band pass transfer function. The transconductance G_{m1}, L and C can be designed in such a way that the above transfer function in eq. (5.1) implements a bandpass transfer function $As / (s^2+\omega^2)$ as in Fig. 3.4. The cascade of two such LC resonators gives a fourth order system. The transconductance G_q implements a negative resistance to increase the quality factor (Q) of the integrated inductor L and the feedback takes place by the current addition of outputs from transconductance and that of the one

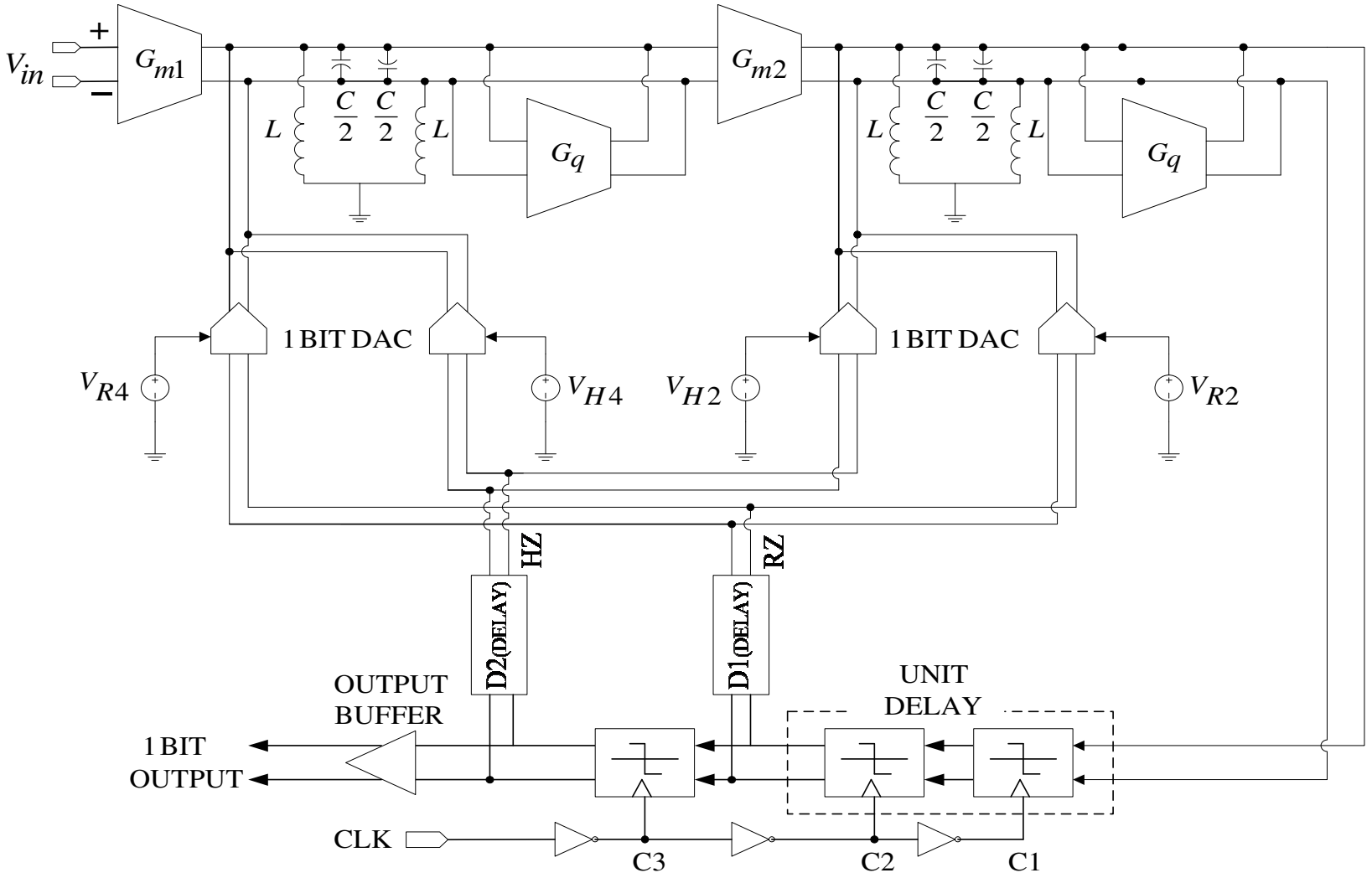


Figure 5.1: Circuit topology of the fourth order band pass continuous time Sigma Delta modulator.

bit switched current Digital to Analog Converter (DAC). Three comparators with two delays (D1 and D2) implement a z^{-1}, quantize the signal and also generate Return to Zero (RZ) and a Half return to Zero (HZ) pulse waveform of the quantized output. The feedback coefficients K_{R2}, K_{H2}, K_{R4}, K_{H4} calculated in Sec. 3.2 is implemented with the control voltages V_{R2}, V_{H2}, V_{R4}, V_{H4} which in turn control the current level of the pulses from the DAC added as feedback.

5.2 Design of bandpass filter

A single ended inductor is laid out and the S-parameter of its equivalent circuit shown in Fig. 5.2 is obtained. From the S-parameter, the value of inductance (L) and its quality factor (Q_L) are plotted against frequency as shown in the Fig. 5.3. From the plot of Fig. 5.3, the values of L and Q_L at 1GHz are obtained.

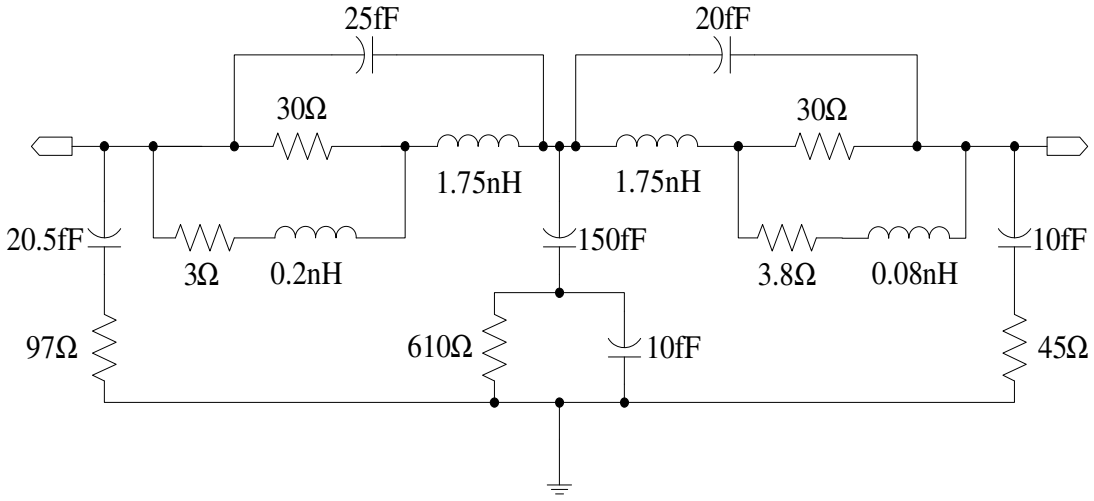


Figure 5.2: Equivalent circuit of an integrated inductor

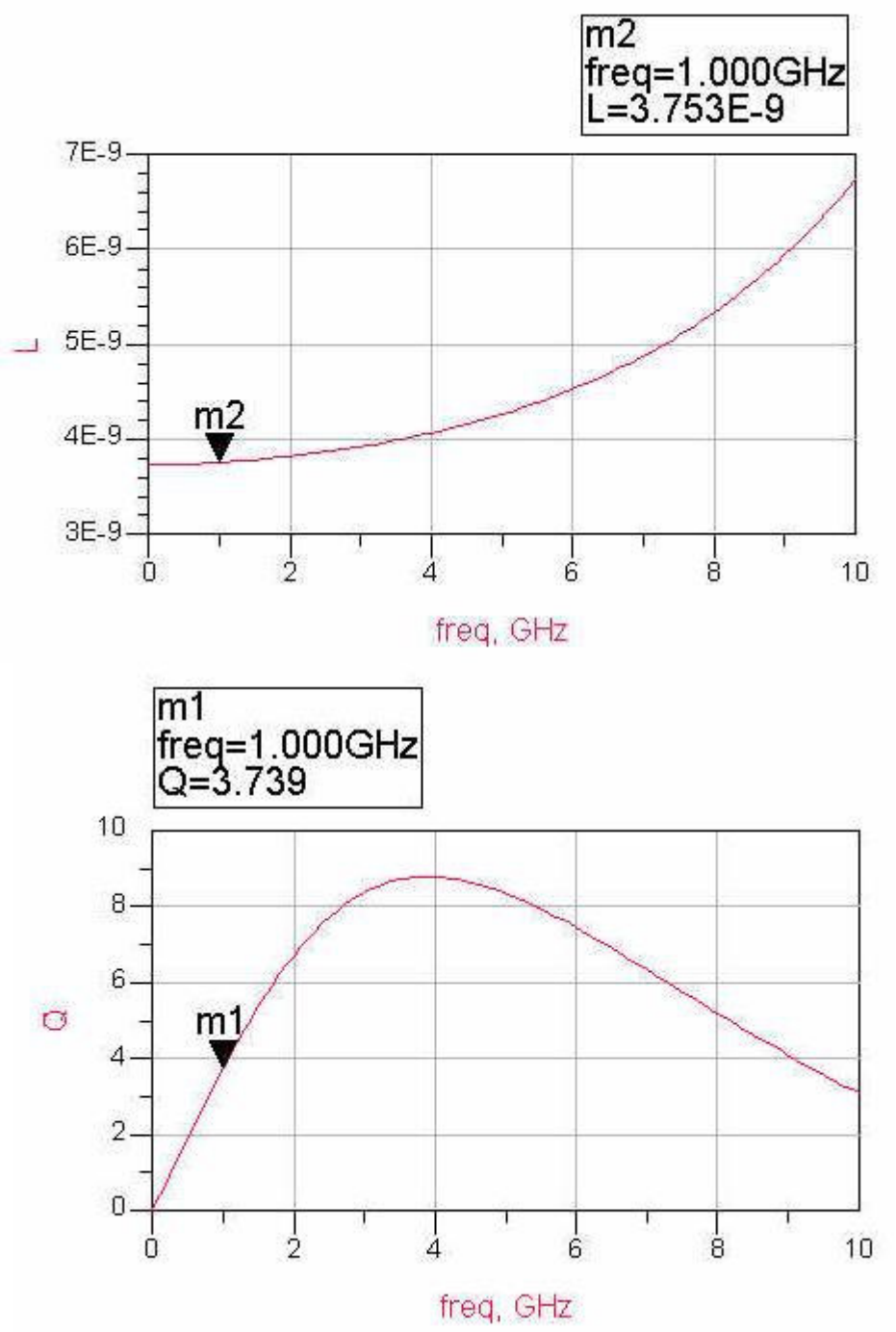


Figure 5.3: The simulated value of L and Q_L of the integrated inductor

Using the above inductor, a bandpass filter with center frequency at 1GHz is implemented with a parallel LC resonator and a transconductor G_m as shown in Fig. 5.4(a). A negative resistance (R) is connected in parallel with the LC resonator to

compensate for the positive series resistance (R_S) of the low Q_L integrated inductor. The equivalent parallel circuit with parallel inductor L_P and resistance R_P is shown in Fig. 5.4(b).

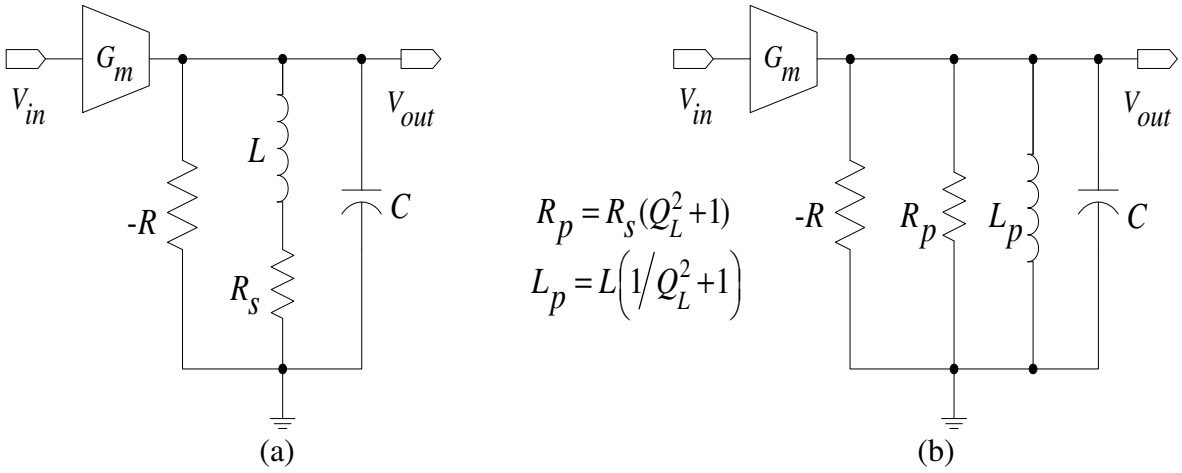


Figure 5.4: Bandpass LC resonator
(a) Parallel LC resonator with a low Q_L inductor
(b) Equivalent circuit of the LC resonator

The transfer function of the equivalent parallel circuit of Fig. 5.4(b) is,

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{s\left(G_m/C\right)}{s^2 + \frac{s}{C}\left(\frac{R - R_p}{R_p R}\right) + \frac{1}{L_p C}} \tag{5.2}$$

By making $R = R_P$, the transfer function $H(s)$ equals to band pass transfer function As / $(s^2+\omega^2)$ whose resonant frequency can be decided with $\omega = 1/\sqrt{L_P C}$.

A Very High Frequency (VHF) transconductor [26] is shown in Fig. 5.5. The inverters Inv1 and Inv2 form the input transconductor G_{m1} (or G_{m2}) as shown in Fig. 5.1 and as G_m of Fig. 5.4. Their transconductance can be tuned with the supply *vdd*1.

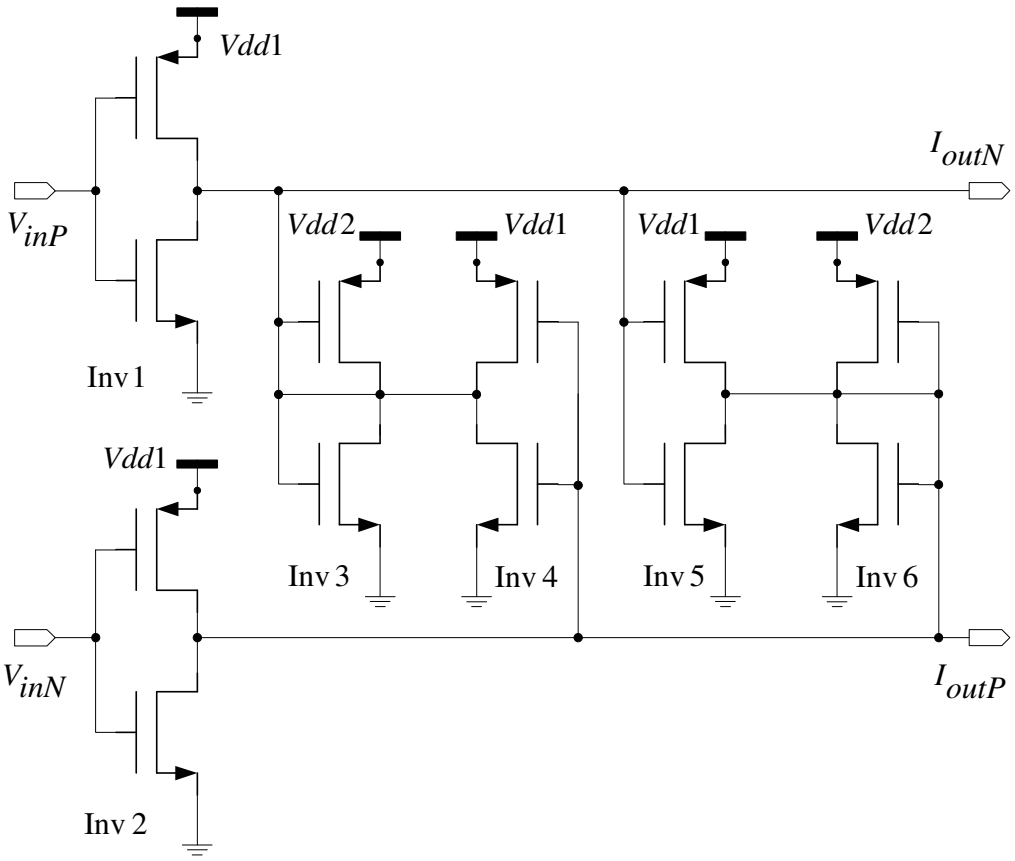


Figure 5.5: A VHF transconductor with negative resistance

The transconductance G_q of Fig. 5.1 which implements the negative resistance R as in Fig. 5.4 is obtained with inverters Inv3-Inv6,

$$R = \frac{1}{g_{m3,6} - g_{m4,5}}, \text{ where } g_{m3,4,6,5} = C_{ox}\sqrt{\frac{\mu_p \mu_n W_p W_n}{L_p L_n}}(vdd1,2 - v_{tn} - v_{tp}) \quad (5.3)$$

by making $g_{m4,5} > g_{m3,6}$, R can be made negative. The fine tuning of Q of the circuit during operation can be done through the supply $vdd2$. The magnitude and phase response of a band pass filter implemented with differential circuit topology and designed using the LC resonator structure of Fig. 5.4 and the VHF transconductor of Fig. 5.5 is shown in Fig. 5.6(a) and Fig 5.6(b).

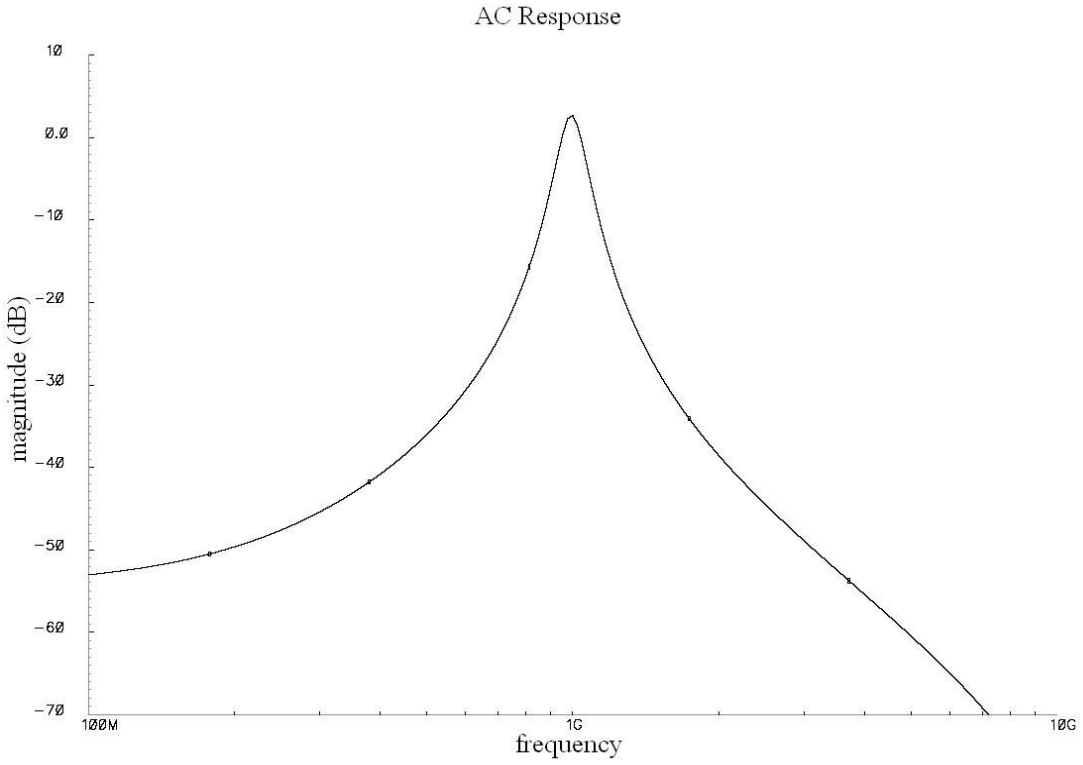


Figure 5.6(a): Magnitude response of bandpass filter

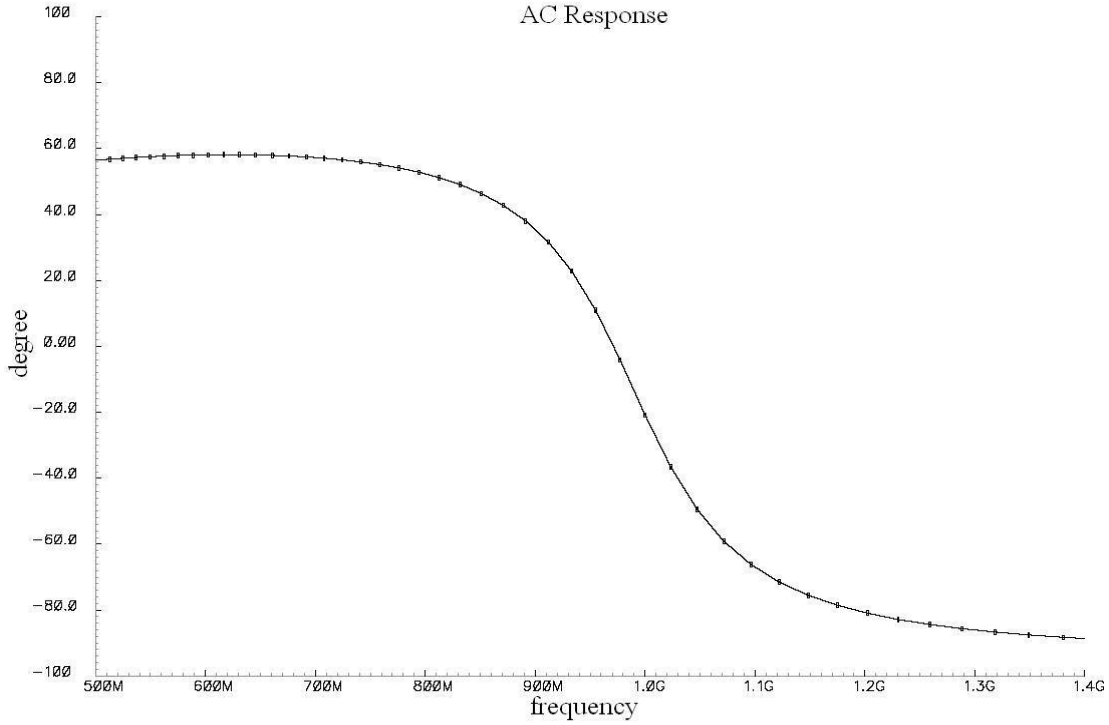
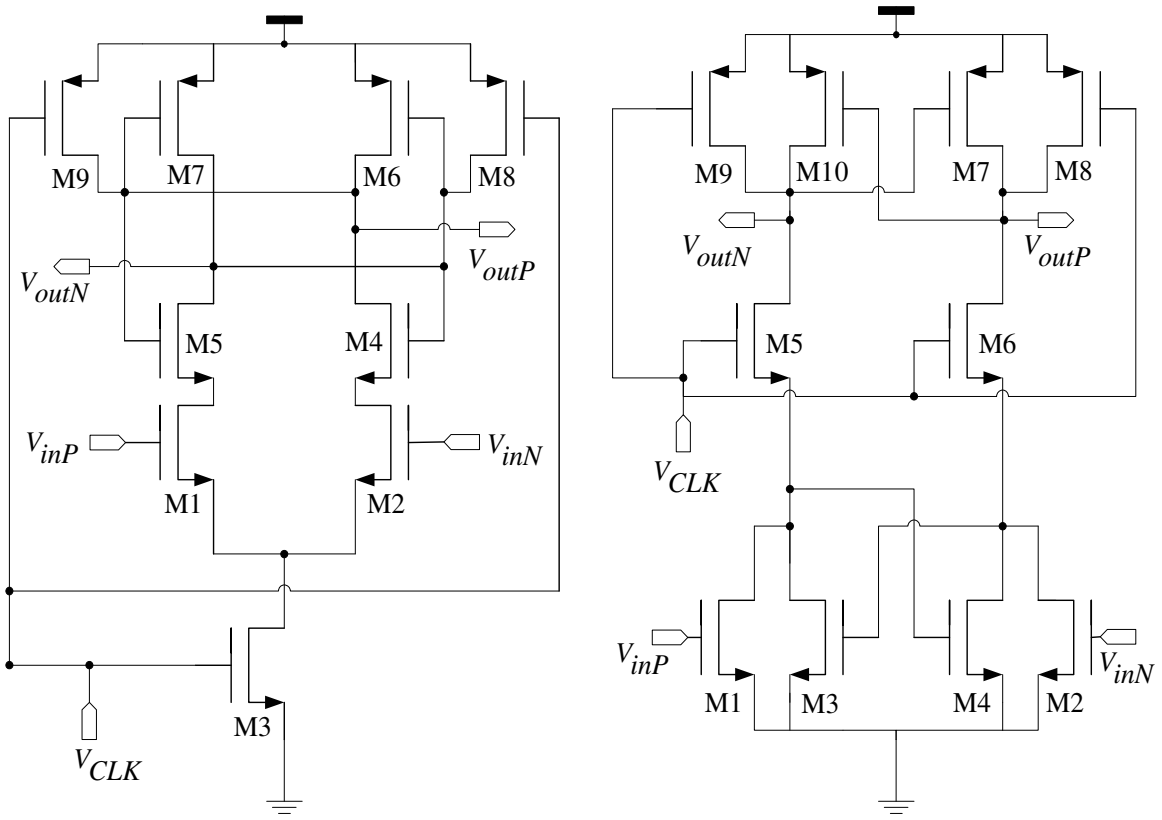


Figure 5.6(b): Phase response of bandpass filter

5.3 Comparator circuit architecture

The 1-bit quantizer and a unit delay shown in Fig. 5.1 are implemented by three clocked comparators where the signal is sampled, compared as well as the output waveform is shaped to RZ or HZ pulses.



(a) (b)

Figure 5.7: The RZ latches used as quantizers in feedback loop.

The comparator C1 of Fig. 5.1 is a differential dynamic comparator [35], with a source coupled differential pair input, a switched current source and a latch as load, shown in Fig. 5.7(a),. The input source coupled differential pair M1, M2 provides a pre amplification before the signal is quantized. When the clock goes high, the switched

current source M3 turns on and the input signals are quantized by the positive feedback of the latch M4-M7. But when the clock goes low the current source is turned off leading to zero DC power consumption, while the pull up transistors M8 and M9 turns on and pulls both the outputs to *vdd*, this gives a return to zero pulse waveform to the outputs of the comparator.

The other two comparators C2, C3 of Fig. 5.1 are as shown in Fig. 5.7(b) [39]. Here the clock strobing is at the drain node of the latch so that the regeneration speed is much faster. This helps in reducing the variation in zero-crossing time [9] of the RZ and HZ waveforms, which would otherwise have the same performance degradation effect as a jitter in quantizer clock would have.

HSpice simulation response of the comparator C1 is shown in Fig 5.8. The comparator C1 quantizes its input when the clock goes high and resets back to logic high with clock goes low. It is also evident from Fig. 5.8 that the quantization provided by a single comparator C1 is not enough, since we don't get a rail-to-rail pulse at the output. This is due to the fact that the sampling clock is so high such that the quantizer doesn't have enough time to pull its outputs to the supply extremes.

Digital implementation of the unit delay z^{-1} as shown in Fig. 5.1 provides enough regeneration time for the quantizer to resolve fully to logic high and low. This reduces quantizer metastability (explained in Sec. 4.3) and is illustrated in Fig. 5.9. At the sampling instant shown by the marker 'A' in Fig. 5.9, comparator C2 of Fig 5.1 sees a large input difference which is the output from C1. C2 again regenerates the output of C1 further to have rail to rail logic levels.

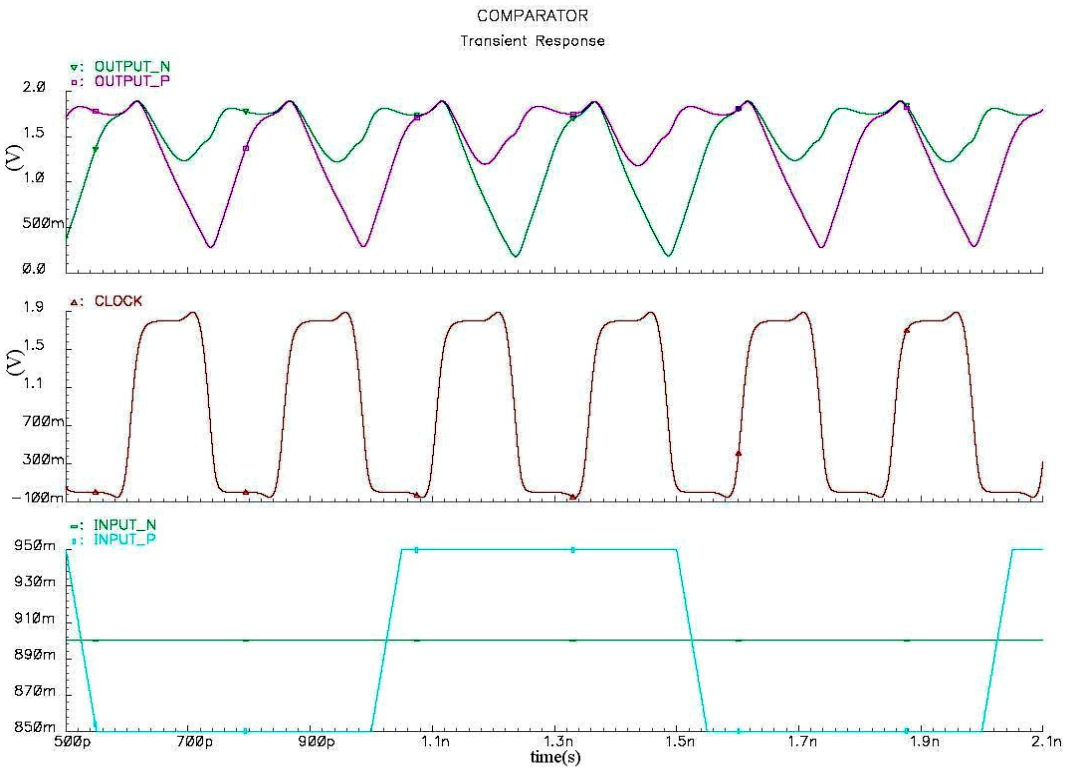


Figure 5.8: Simulation of the comparator.

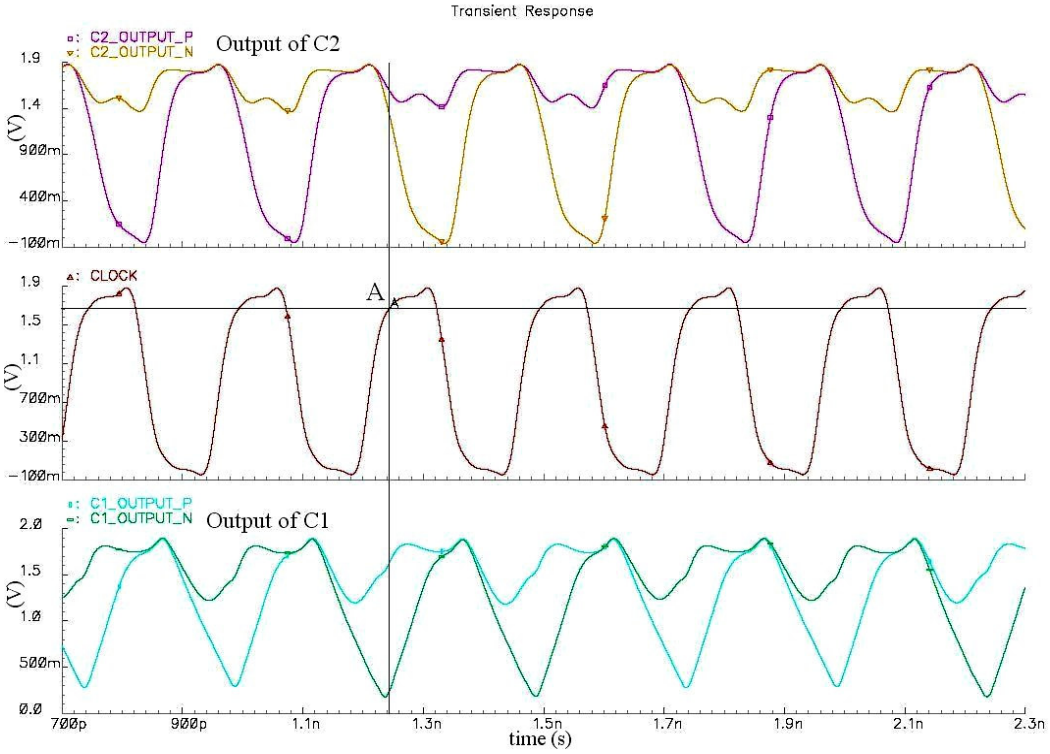


Figure 5.9: Reducing metastability by digital implementation of unit delay.

5.4 High speed current switched DAC

The output of the comparator which is a RZ or HZ voltage waveforms, drives a high speed current switched feedback DAC [23] shown in Fig. 5.10. The DAC converts the voltage waveforms into current. A swing reduction driver of Fig. 5.11 is placed at both the inputs to reduce the transistor switching transition time which enables high speed operation.

Two dummy transistors M3 and M4 of Fig. 5.10 with cross coupled drains reduce the feed-through charges involved in switching off M2 and M1 respectively. The control voltage V_c is used to set the current level of the pulse waveforms according to the feedback coefficient Ks which were calculated in Sec. 3.2. The swing reduction drivers at the input of the DAC reduce the swing of comparator outputs from rail-to-rail to 1.1V-950mV as shown in Fig. 5.12. The current pulse obtained from the current switched DACs at 4GHz is also shown in Fig. 5.12.

In Fig. 5.10 M6, M8 and M9 act as current sources. The current source M6 sinks twice as much as sourced by both M8 and M9. When both the inputs from the comparator go high i.e. in reset state, the input transistors M1 and M2 turns on and there is zero current at output terminals. If one of the inputs, say V_{inP} goes low, M2 turns off and the current from M9 is sourced out to the output terminal I_{outN}, while an equal amount of current is drawn in from I_{outP} through M1. Hence RZ current pulses for both the DAC differential outputs are obtained as shown in Fig. 5.12.

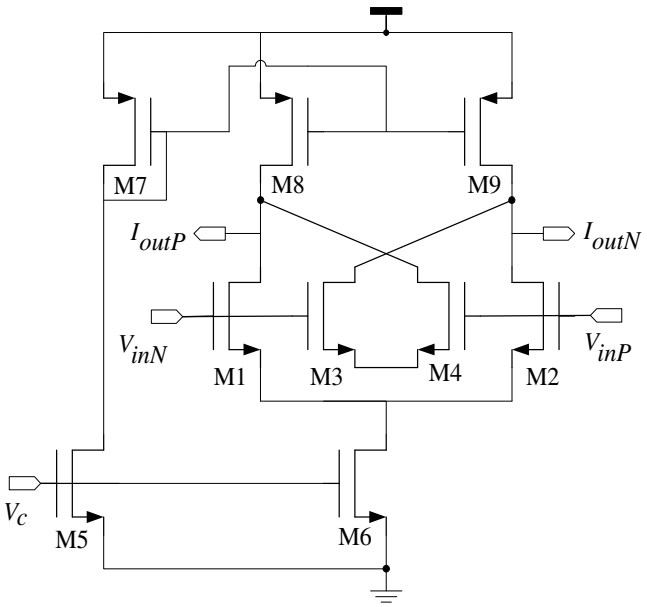


Figure 5.10: High speed current switched DAC.

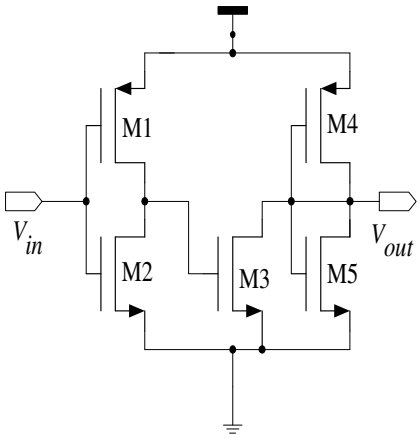


Figure 5.11: Swing reduction driver.

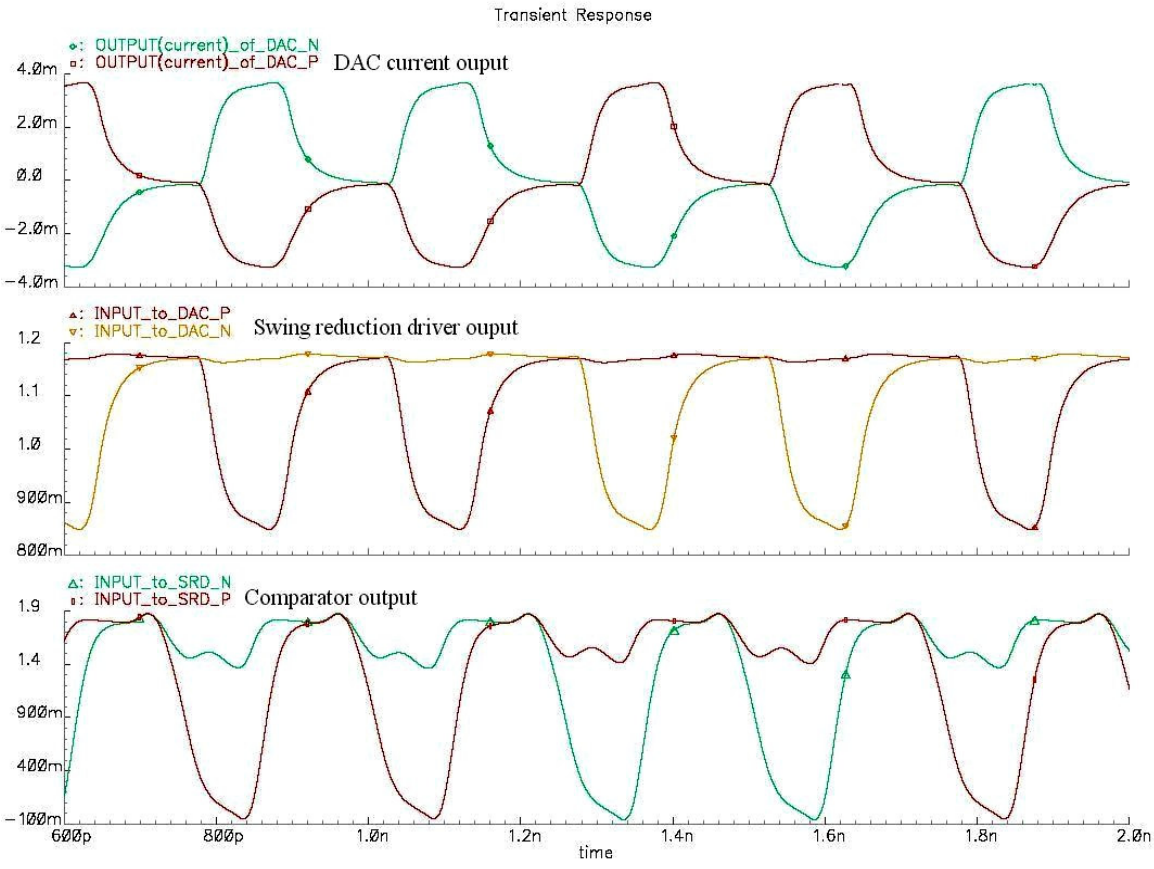


Figure 5.12: Output of swing reduction driver and DAC current pulse.

5.5 Loop delay compensation in feedback

In previous bipolar realization [6], the digital delay z^{-1}, quantization and generation of RZ and HZ pulses were implemented with architecture similar to Fig. 5.13. In the four cascaded comparators, C1 and C2 delay the compared signal by one clock, implementing z^{-1}. The output of C3 is a RZ pulse waveform and that of C4 is a HZ pulse waveform, which is the required ideal case as explained in Fig. 5.13. Thus this four-comparator structure was designed for an ideal case where the propagation delay of comparator in feedback is not taken into account. If the same feedback architecture is realized in CMOS then the practical issues rising due to non-idealities will be discussed further.

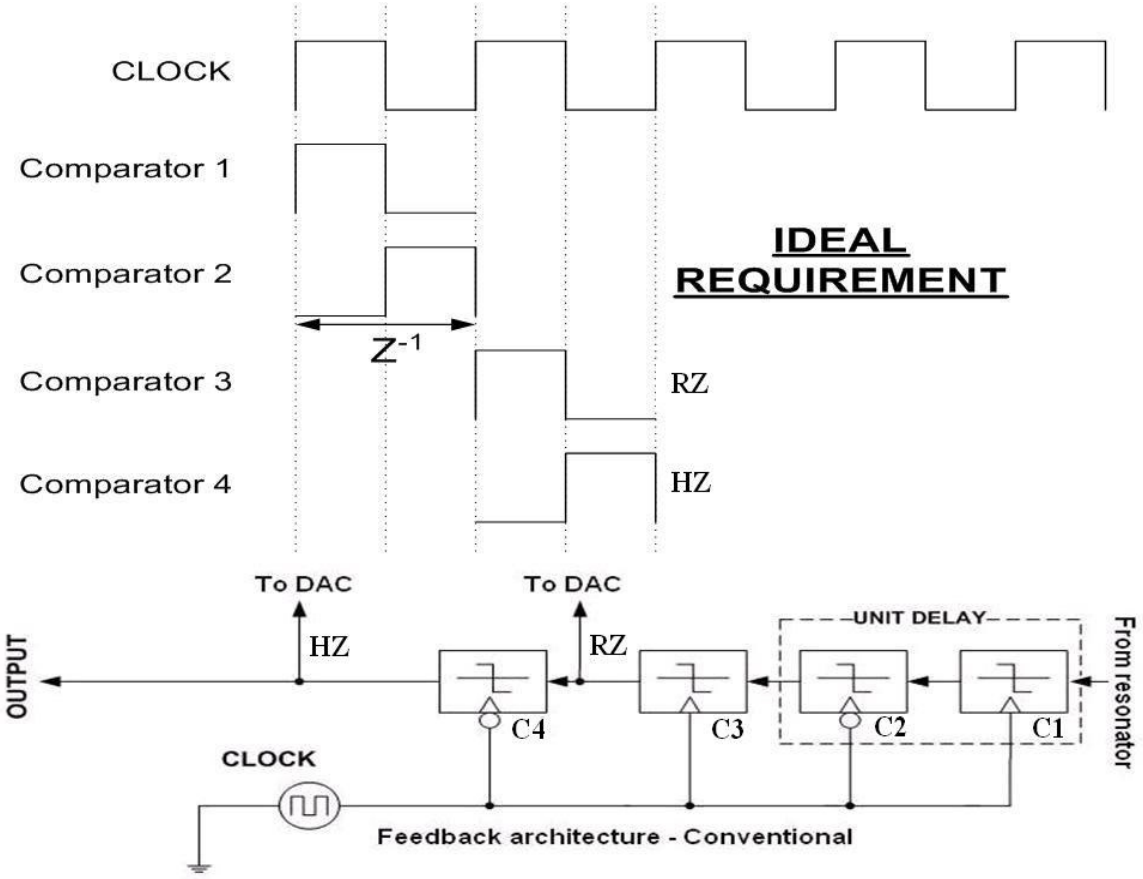


Figure 5.13: Conventional feedback architecture in ideal situation.

Under practical non ideal situations, due to the finite response time of the comparators there always exists a loop delay (as explained in Sec. 4.1) in the pulse with respect to the sample clock as shown in Fig. 5.14. If the clock frequency is in KHz range, the loop delay is negligible when compared to the clock time period. But when the clock frequency is in MHz range, this loop delay will degrade the performance (Sec. 4.1), without affecting the stability of modulator. Fig 5.15 explains the situation under which the clock frequency is in GHz range. In this case the same loop delay of Fig. 5.14 (which doesn't create any stability problem such as) becomes more pronounced since it is a significant part of sample clock period and the modulator goes unstable.

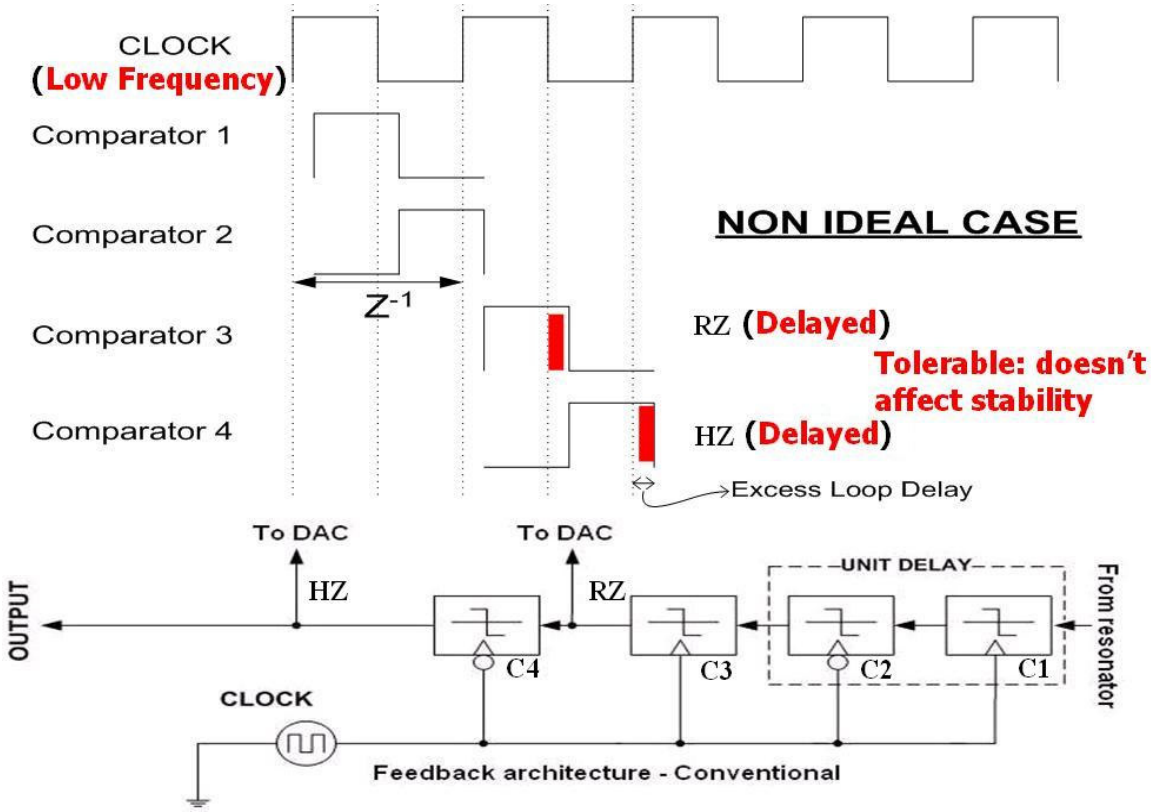


Figure 5.14: Conventional feedback architecture under non ideal situation and when clock frequency is low.

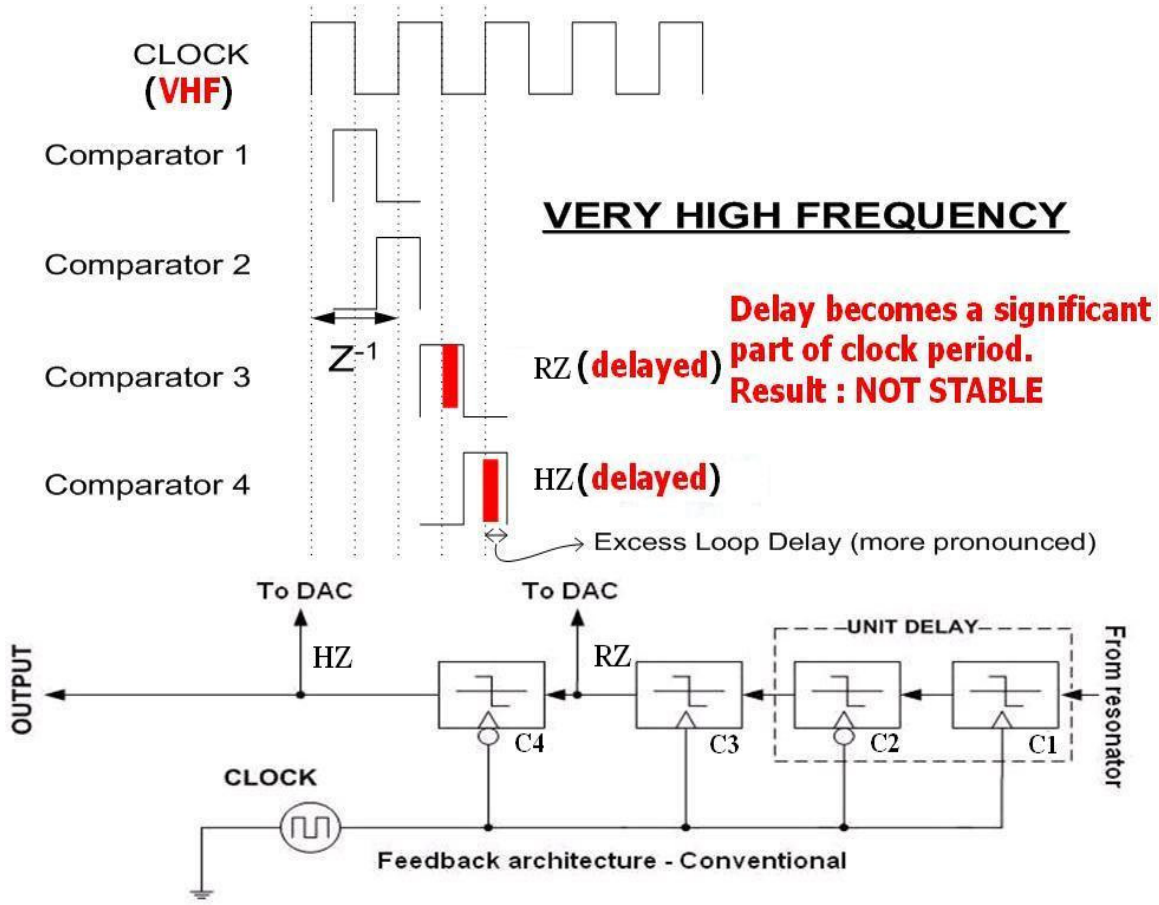


Figure 5.15: The non ideal conventional feedback architecture with very high frequency (VHF) sample clock.

When the CMOS modulator is implemented with this conventional feedback loop structure, the excess loop delay of the DAC current pulse which adds at feedback, is 35.2% (88.15ps from Fig. 5.16) of the clock period (f_s = 4GHz) which renders the modulator unstable as explained in Sec 4.1. Fig. 5.16 shows the simulation of the open loop CMOS realization of conventional feedback architecture along with the DAC output pulses. The input signal from the resonator is sampled at 'M1', after one clock period delay (z^{-1}) a RZ and HZ current pulses which were suppose to appear at marker 'A' appears at marker 'B' due to loop delay. Hence new design solutions are required to mitigate the above stability problem of CMOS modulators at very high frequencies.

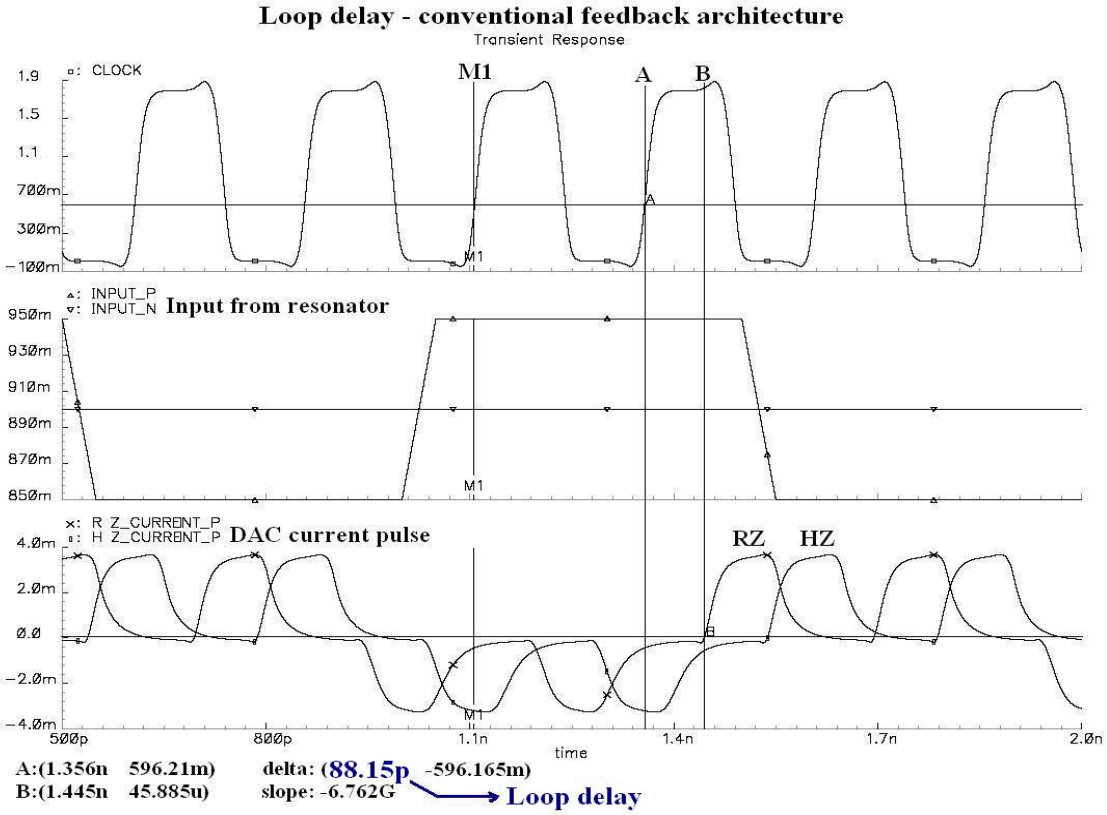


Figure 5.16: Loop delay of a conventional feedback architecture.

A novel feedback structure using only three comparators and two delay elements [41] is proposed as shown in Fig. 5.1. Fig. 5.17 explains the principle being compensating the excess loop delay. Since all the comparators are designed to produce RZ waveform at its output (as explained in Sec. 5.3), the waveform at the output of comparator C2, which already has a large delay is delayed further with D1 so that it becomes a RZ waveform after one clock period (z^{-1}) and the output of the comparator C3 is delayed with D2 in the same way so that it forms a HZ waveform after a one clock period, thus eliminating the fourth comparator. In our implementation, D1 and D2 are just inverter buffers however it is easy to implement D1 and D2 to be programmable delays, which can be tuned with a bias current during operation so that any excess loop delay caused due to process

variation, can be compensated easily. The design of delays D1 and D2 should be such that we obtain a RZ and HZ waveforms. Hence the delay to be introduced is given by,

$$\tau_{D1,D2} = 0.5\left(1/f_s\right) - \tau_{latchcomp} \tag{5.4}$$

where the delay of latched comparator $\tau_{latchcomp}$, is the time taken by the regenerative positive feedback to fully quantize the input signal into a valid logic level [46],

$$\tau_{latchcomp} = K\frac{L^2}{\mu_n V_{eff}}\ln\left(\frac{\Delta V_{out}}{\Delta V_{in}}\right) \tag{5.5}$$

where K is a constant of value between 2 and 4, ΔV_{out} is the valid output logic level and ΔV_{in} is the input signal at the start of latch phase. Hence the design of D1 and D2 should be such that it implements the delay $\tau_{D1,D2}$ given in eq. (5.4). In our case of using inverters as D1 and D2, the design equation for transistor sizing of D1 and D2 is dictated by $\tau_{delayinv}$, the propagation delay of the inverter. Hence D1 and D2 can be designed using eq.(5.4) and [47],

$$\tau_{delayinv} = \tau_{D1,D2} = \frac{2C_L}{V_{dd}}\left(\frac{1}{\mu_n C_{ox} W_n/L_n} + \frac{1}{\mu_p C_{ox} W_p/L_p}\right) \tag{5.6}$$

The simulated DAC current pulse of the proposed feedback architecture is shown in Fig.5.18. From Fig. 5.18 it is evident that the loop delay is keep below 3% (7.73ps) of the clock period (f_s = 4GHz) by using the proposed feedback architecture and hence the stability of the modulator is ensured.

Feedback loop delay of both the feedback structures for different input amplitudes is shown in Fig. 5.19. Fig. 5.19 is obtained by simulating the two feedback structures with a piece wise linear input voltage having a slope of 400mV/250ps. The input voltage goes

negative first such that the output of feedback structure produces a strong negative pulse and then goes positive with a slope of 400mV/250ps such that at the next sampling instant the input to the feedback structure is a specified value V_{inf}, so that the feedback structure produces a positive pulse in the next sampling instant. The delay of this positive pulse from the sampling instant is measured and plotted against varying V_{inf} .

It is evident from Fig. 5.19 that the proposed structure with three comparators has a lesser loop delay compared to the conventional one. But, when the input is larger the loop delay of the conventional architecture attaints a constant value well before than that of the proposed structure. In other words the loop delay of proposed structure is more dependent on input than that of conventional one. As a result, the proposed structure would have higher metastability than the conventional architecture (Sec 4.3).

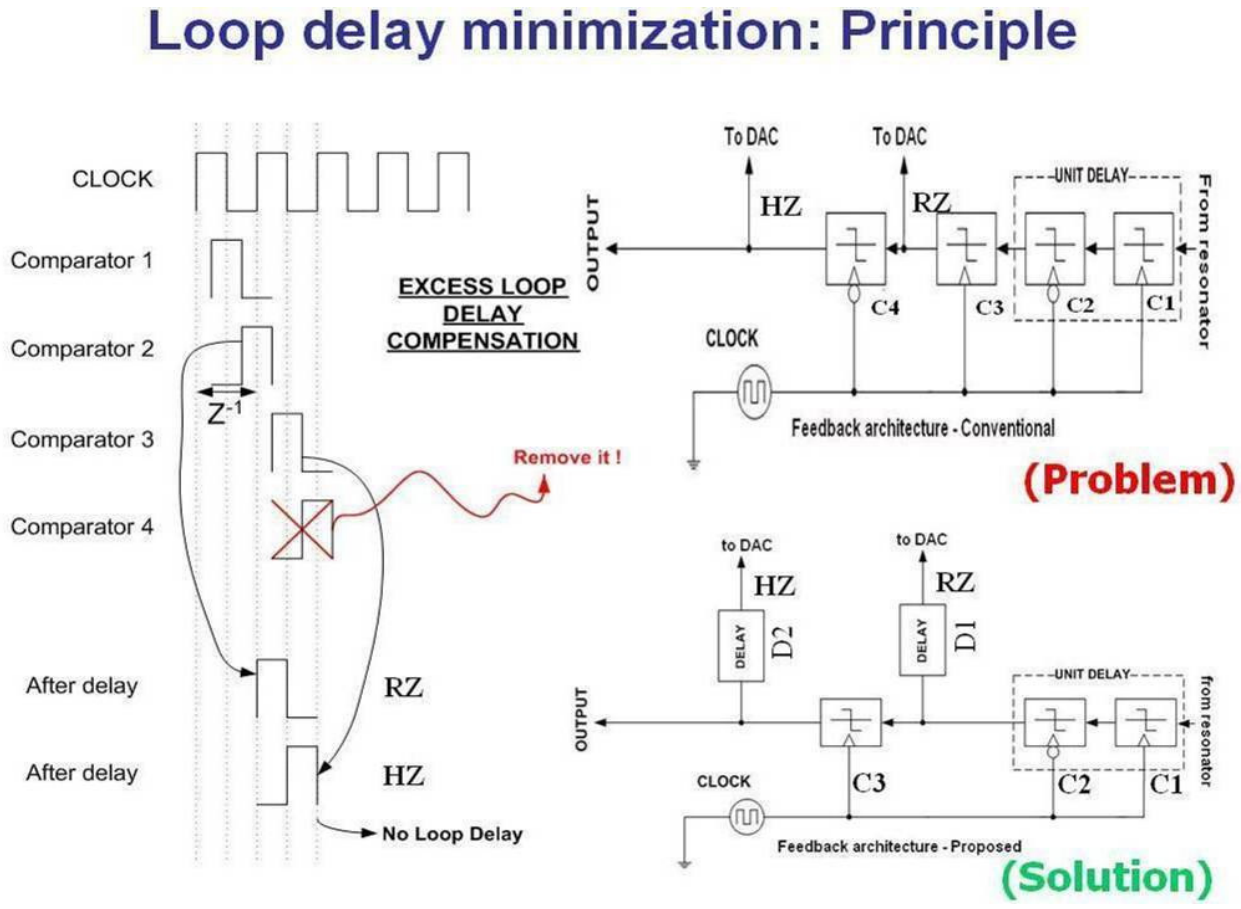


Figure 5.17: The proposed feedback architecture.

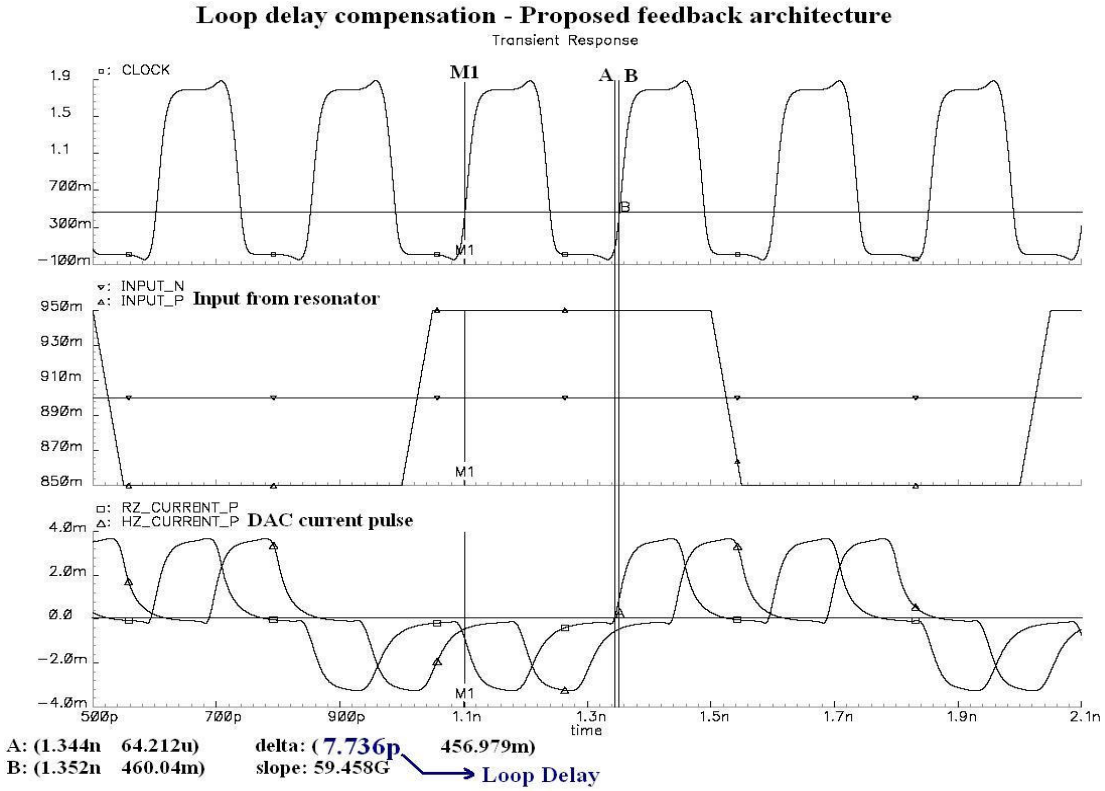


Figure 5.18: Simulation of the proposed feedback architecture.

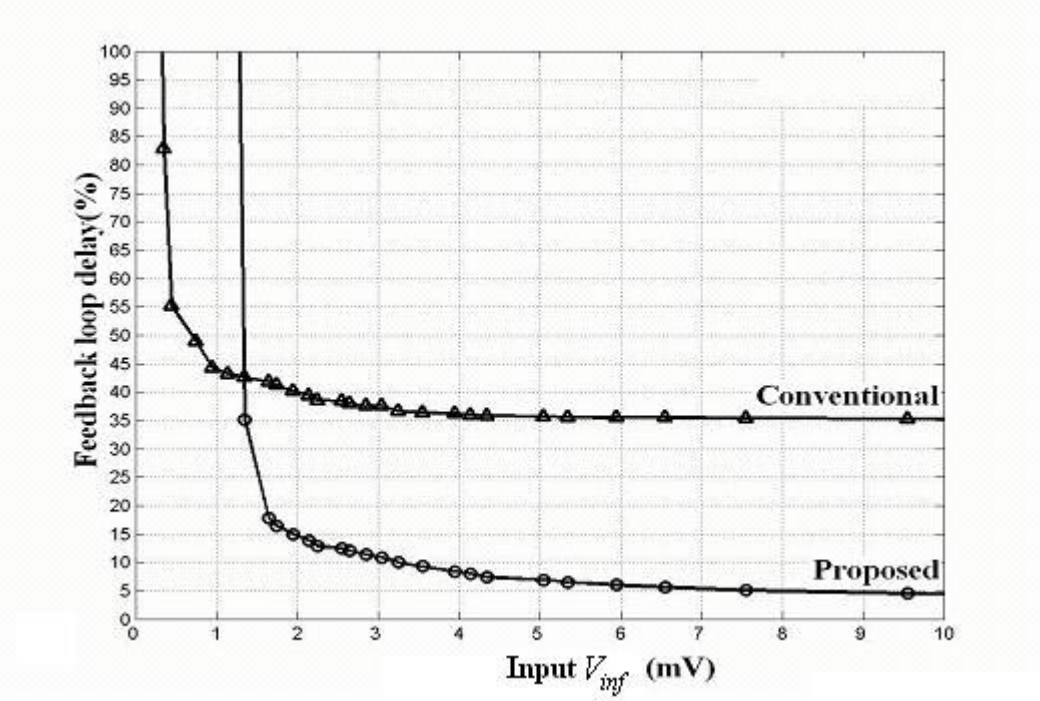


Figure 5.19: Comparison of the loop delays from proposed and conventional feedback structures.

5.6 Modulator layout and post layout simulation

The 4^{th} order continuous time bandpass Sigma Delta modulator was implemented in CMOS 0.18µm/1.8V 1P6M process. The layout of which is shown in Fig. 5.20, occupies an area of $1.8mm^2$ dominated largely by the four single ended inductors. The capacitors were designed using metal-insulator-metal structure to achieve the best quality factor. For each of the capacitance, two capacitors of half the value as shown in Fig. 5.1 were connected back-to-back in parallel to maintain balance in the presence of substrate parasitics. There are also other issues [2] to be taken care while laying out a very high frequency mixed signal design to ensure signal integrity, reduce cross talk and noise. Some of these are listed below:

1. To minimize supply noise reaching other components, use separate *vdd* for more current consuming components.
2. An interconnecting wire of 1µm width can withstand 1mA of current without electro migration, hence width of the current driving interconnects should be estimated with the current requirement of the corresponding component.
3. For other interconnections use a width of 1µm to 3µm of preferably upper metals. When two metals carrying differential signals cross each other, it is better to use alternate metal lines so that the middle metal can be routed between them and connected to ground, which reduces the capacitance formed between the crossing metals.
4. Use star connections in connecting the *vdd* pad to different components.
5. Use metal-1 for *gnd* and metal-2 for *vdd*.

6. Inductors are usually separated from other components by 10 times the thickness of its metal width.
7. Use 45 degree turn in interconnect wires which carry high frequency signals, to avoid signal reflection.
8. While interconnecting capacitors, the vias used could add to the capacitance, so avoid vias as far as possible.
9. In mixed signal designs, separate the analog components from the digital components.
10. Follow a common centroid approach in placing the components.
11. Surround each analog component, in a mixed signal design with guard rings connected to analog ground.
12. In mixed signal design, use separate *vdd* and *gnd* for analog and digital components. This helps in avoiding digital noise entering analog components.
13. In placing pads always follow a ground-signal-ground-signal-ground (GSGSG) approach for very high frequency differential signals.
14. Never place a signal pad close to a *vdd* pad; this avoids noise from *vdd* entering the signal.
15. Fill the unused area of the chip with *gnd*.

The parasitics of the layout is extracted and post layout simulation of the modulator is carried out. The results are tabled in Table 5.1, which shows that the targeted performance of Table 1.1 is achieved. Fig 5.21 shows the dynamic range plot of the modulator. Each of the simulation to find SNR takes many days to complete, hence only a limited no. of data is plotted in Fig.5.21. The spectrum of the output bit stream is shown in Fig. 5.22.

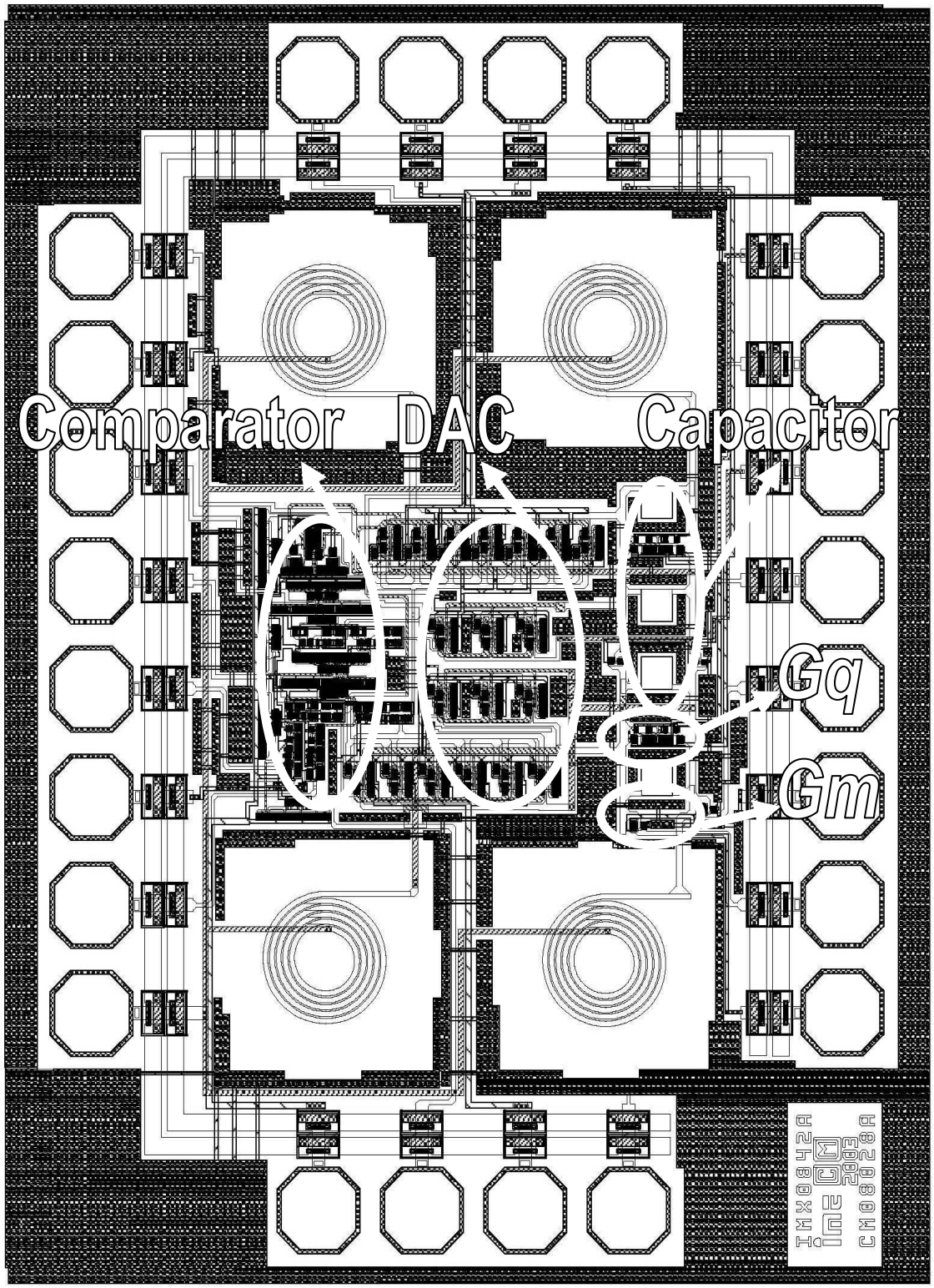


Figure 5.20: The Layout of 4th order continuous time bandpass ΣΔM.

Table 5.1: Simulation results

Technology	0.18μ CMOS
Input Signal (f_c)	1GHz
Bandwidth	500 kHz
Sampling Frequency (f_S)	4GHz
Loop Delay	7.73ps (3% of clock period)
Full scale input range	$700mV_{pp}$
Peak Signal to Noise and Distortion Ratio (SNDR)	40dB
Dynamic Range	6 bits
Power Consumption	290mW
Power Supply	1.8 V

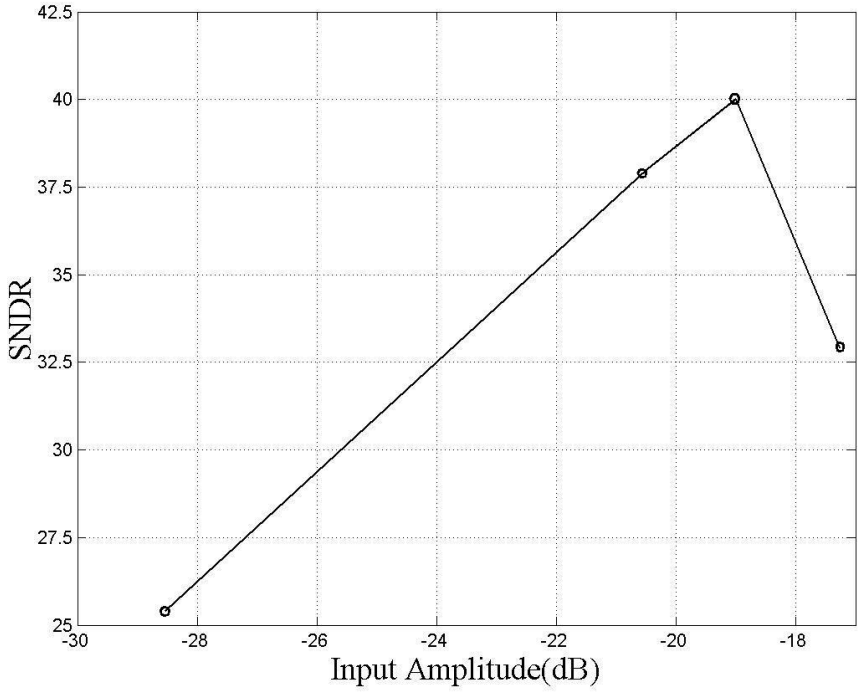


Figure 5.21: Dynamic range plot

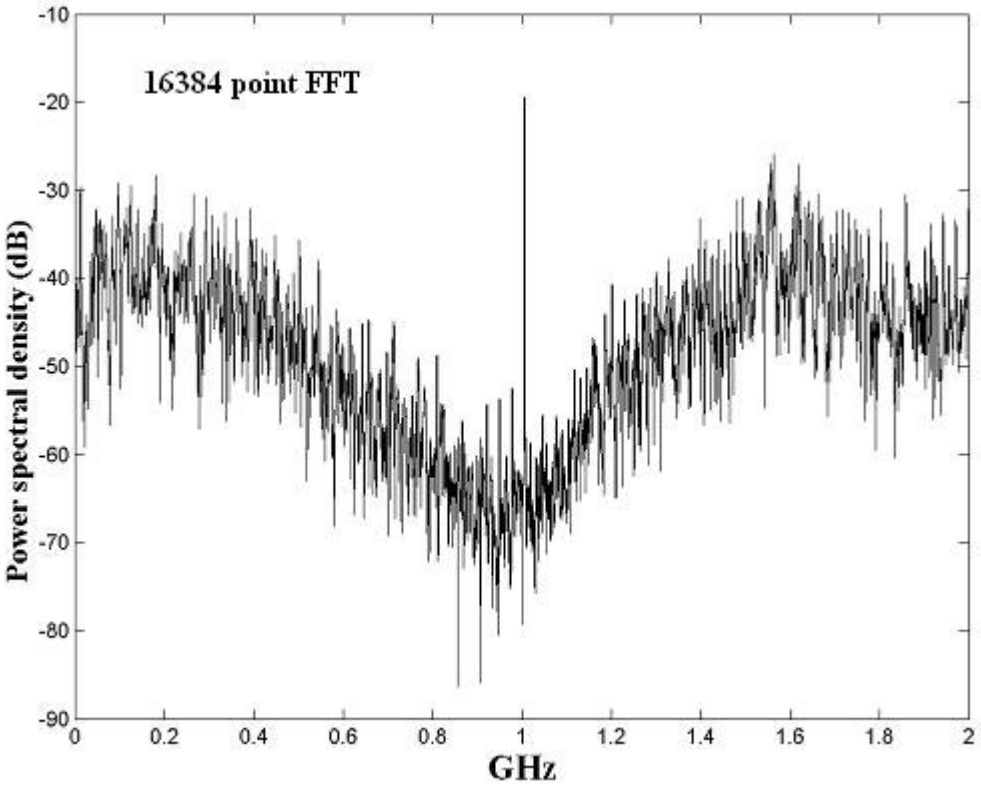


Figure 5.22: Spectrum of the output bit stream from a 4th order CT bandpass ΣΔM.

5.6.1 Analyzing for lower SNR

By capturing the quantizer input waveform, the quantizer input probability density function (pdf) is plotted in Fig.5.23. It is obvious for the pdf to be wider because with higher hysteresis the quantizer output bit remains the same for smaller inputs and the circuitry inside the loop will continue integrating in the same direction, enlarging signal swings (Sec. 4.3). From the quantizer input pdf of Fig 5.23 and the delay profile of the proposed feedback architecture shown again in Fig. 5.24 for larger inputs, the DAC pulse delay for every input of the quantizer can be deduced. From the delay profile of the proposed architecture shown in Fig. 5.24 it was found that only for an input greater than 66.35mV, the delay of the feedback pulse has a constant value of 3% (7.73ps) of clock

period. But for inputs lesser than 66.35mV the delay of the DAC pulse was dependent on the comparator input due to the metastability of the comparator (explained in Fig. 4.8). Hence the DAC pulse width for inputs lesser than 66.35mV tends to vary with the comparator input, which is similar to the result of having a jittered clock as explained in Sec 4.3. The DAC pulse width variation pdf is shown in Fig. 5.25 and its variance was also calculated. The spectrum whitening which rises due to DAC pulse width variation and that due to clock jitter is the same [6], hence from eq. (4.7) the expected SNR with such a DAC pulse width variation pdf for a RZ and HZ pulse would be 44dB, which almost coincides with the result tabulated in Table 5.1. This shows that the degraded SNR is largely due DAC pulse width variation which is a result of comparator metastability.

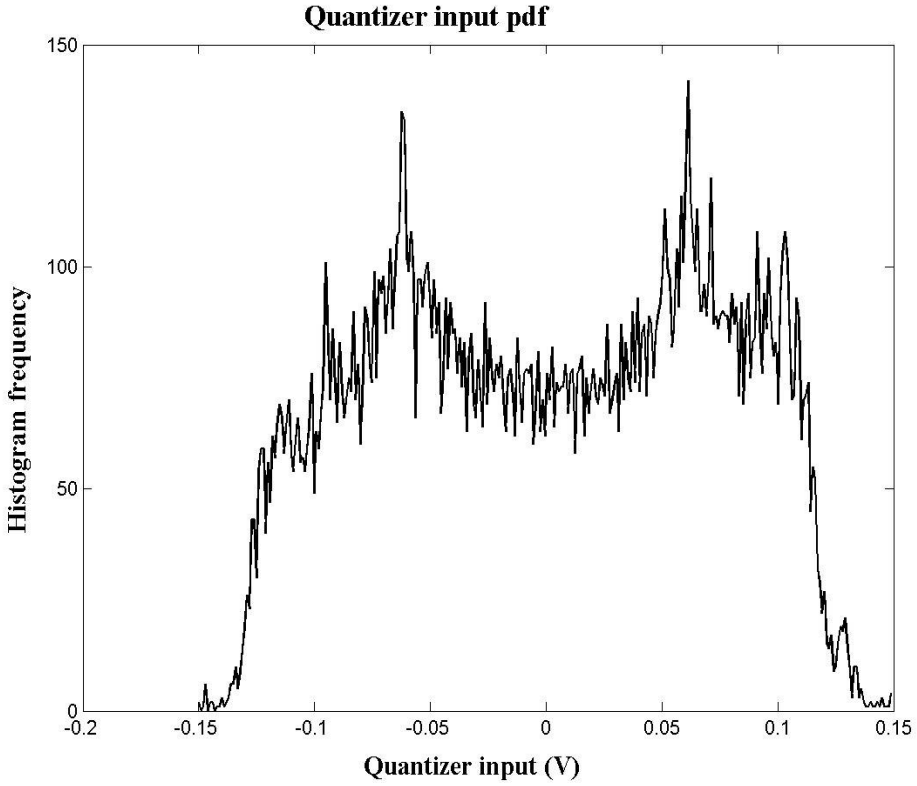


Figure 5.23: Quantizer input pdf.

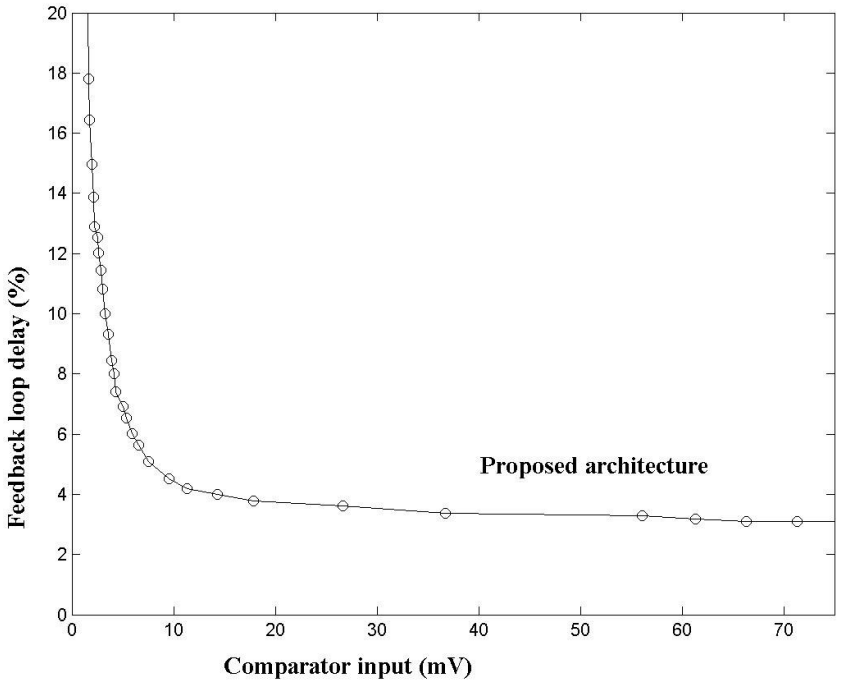


Figure 5.24: Loop delay of the proposed feedback architecture for larger inputs.

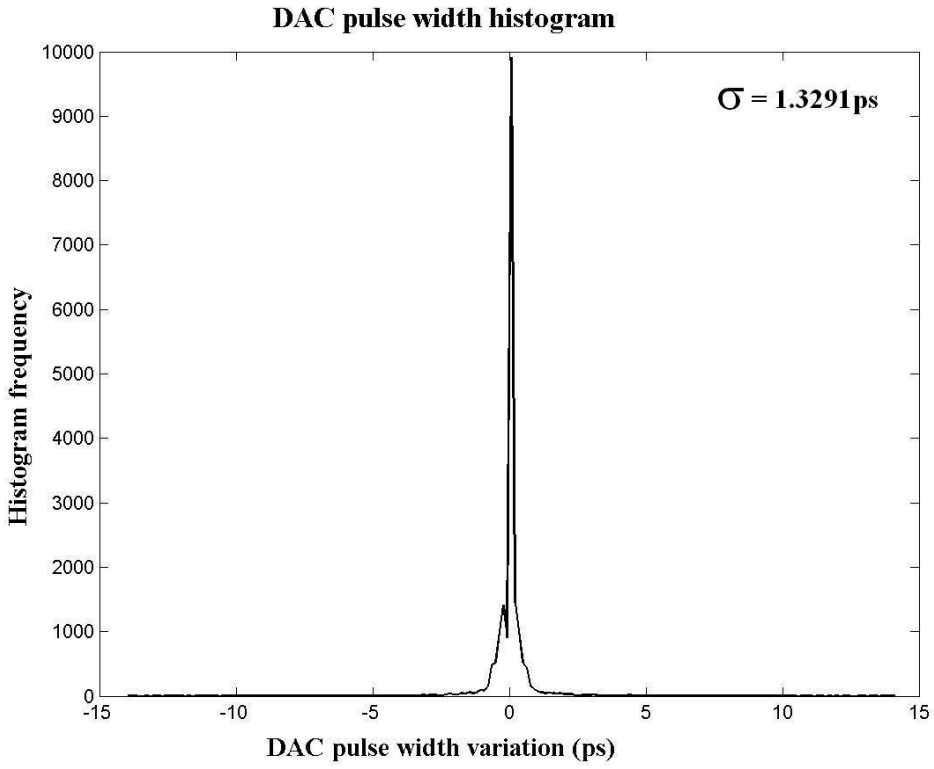


Figure 5.25: DAC pulse width variance pdf.

5.6.2 Testing the modulator for higher sampling frequency of 6GHz

To test the stability of the proposed modulator architecture for higher sampling frequencies, another 4^{th} order CT bandpass ΣΔM was designed to sample a signal at 1.5GHz with a clock frequency of 6GHz. The simulation results of the modulator are tabulated in Table 5.2. The spectrum of modulator output bit stream is in Fig. 5.26. It is evident that the modulator is still stable, but the noise shaping is further degraded at such very high frequencies by metastability of the comparators which whitens the spectrum as explained before.

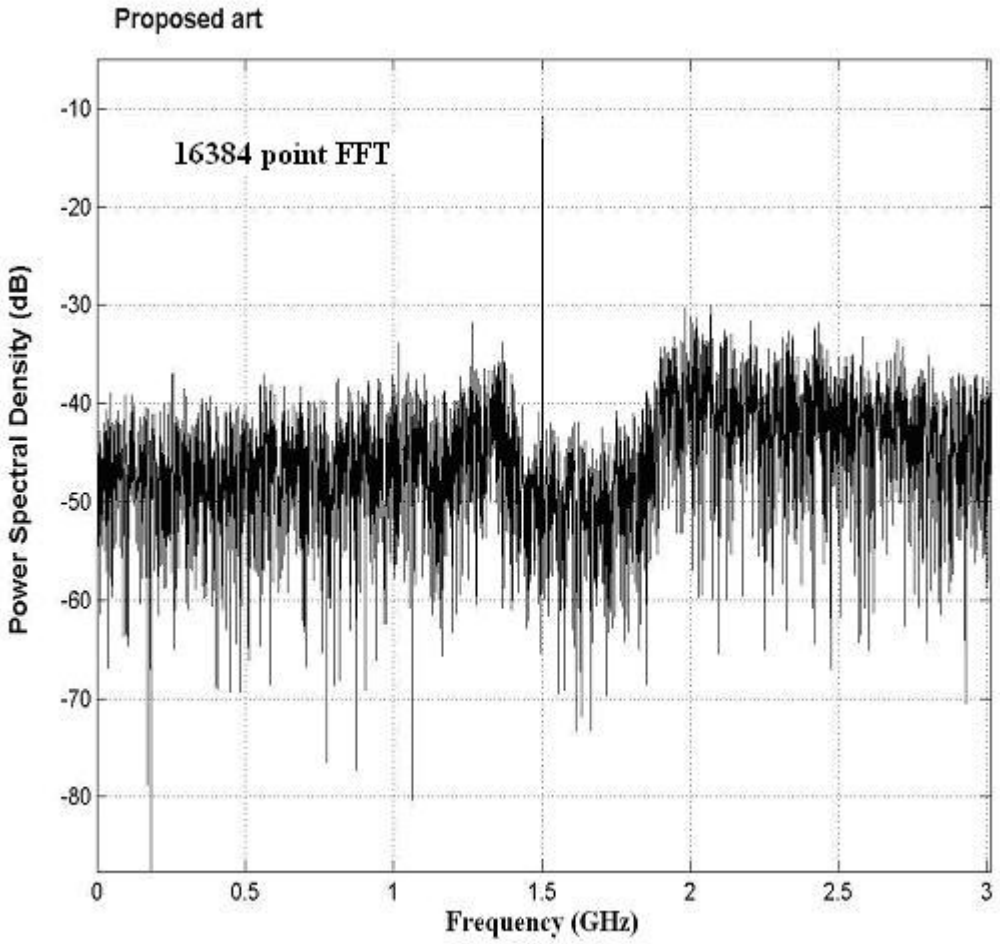


Figure 5.26: Power Spectral Density of output bit stream.

Table 5.2: Simulation results for higher sampling frequency

Technology	0.18μ CMOS
Stability	Stable
Input Signal (f_s)	1.506GHz
Bandwidth	700 kHz
Sampling frequency (f_c)	6.024GHz (4*f_s)
Loop Delay	7.46ps (4.5% of clock period)
Peak Signal to Noise and Distortion Ratio (SNDR)	33dB
Dynamic Range	5 bits
Power Consumption	420mW @ 1.8V

5.7 Summary

The fourth order LC bandpass CT ΣΔM achieves a peak SNDR of 40dB while converting a signal at 1GHz of 500 kHz bandwidth with a sampling frequency of 4GHz. With new proposed feedback architecture, the feedback loop delay of the very high speed modulator is keep below 3%. The modulator is even stable at a higher sampling frequency of 6GHz. Even though loop delay is minimized which otherwise folds out of band noise into signal band, the performance of the modulator is mainly affected by the quantizer metastability at such very high frequencies.

Chapter 6

Test Plan and Measurements

Since the operating frequency of the modulator is very high, it is better to test different parts of the modulator separately before testing the whole CT ΣΔM. The output buffer and the feedback comparator structure along with the digital delay are tested as an initial attempt.

6.1 Output buffer

The modulator needs a 4GHz clock pulse for sampling. Due the absence of a pulse generator to generate such high frequency clocks, we tend to use a high shoot (high amplitude) sine wave as the clock. The idea is to excite an inverter buffer with a high shoot sine wave and the output of which would be used as the clock for the modulator. In order to test this idea and also to test the working of an inverter buffer used at the output of the modulator, the following test setup was built.

6.1.1 Test setup

The test setup to test the output buffer is shown in Fig. 6.1. The buffer consists of an inverter chain to drive 50 ohms load. Since the input is given to an inverter buffer, it is DC shifted to *vdd*/2 and the output pulses are viewed through a digital sampling oscilloscope.

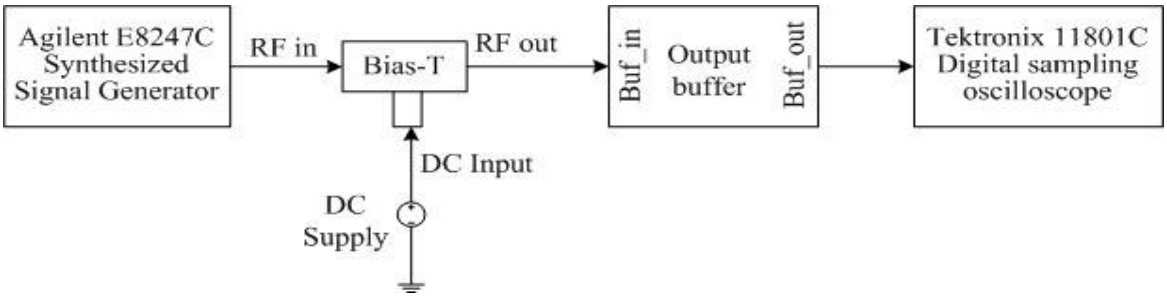


Figure 6.1: Test setup of output buffer.

6.1.2 Test results

The output waveforms at 1GHz and 4GHz are in shown in Fig. 6.2 and Fig. 6.3 respectively. The results for other input frequencies are tabulated in Table 6.1, which shows that the output buffer is functional at such high frequencies.

Table 6.1: Testing output buffer

INPUT (Sinusoid)		OUTPUT					
Freq. (GHz)	Amp. (dBm)	Freq. (GHz)	Peak-Peak (mV)	Rise (ps)	Fall (ps)	Supply (V)	Current (mA)
0.25	8.5	0.25	800	170.6	303.4	1.8	30
0.5	8.5	0.5	744	161.5	243.9	1.8	30
1	8.5	1	700	101.32	292.26	1.8	30
2	8.5	2	560	79.4	73.2	1.8	32
4	10.5	4	472	60.08	57.33	1.8	33

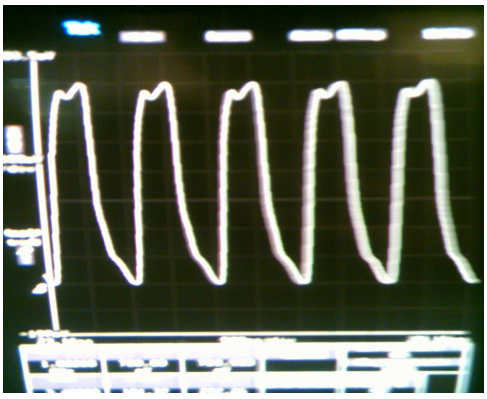


Figure 6.2: Buffer output at 1GHz

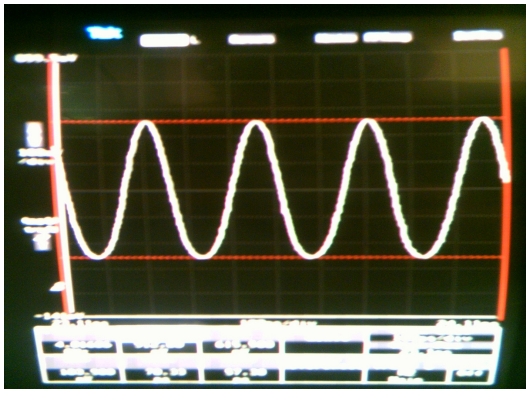


Figure 6.3: Buffer output at 4GHz

6.2 Feedback comparator structure

The feedback comparator structure of the modulator in Fig. 5.1, to be tested is shown separately in Fig. 6.4. Differential inputs *Vin_P* and *Vin_N* are given to C1 and the output of C3 is measured. To have the same loading effects at the output of C2 and C3 as that of the modulator, the delays D1 and D2 are left connected as such, shown in Fig. 6.4. Since the clock goes to an inverter buffer before reaching the comparators, a high shoot sine wave of large amplitude can be used as the clock, which was demonstrated before in Sec. 6.1. The output buffer of Fig. 6.4 is a replica of the same buffer which was tested for its functionality in Sec. 6.1.

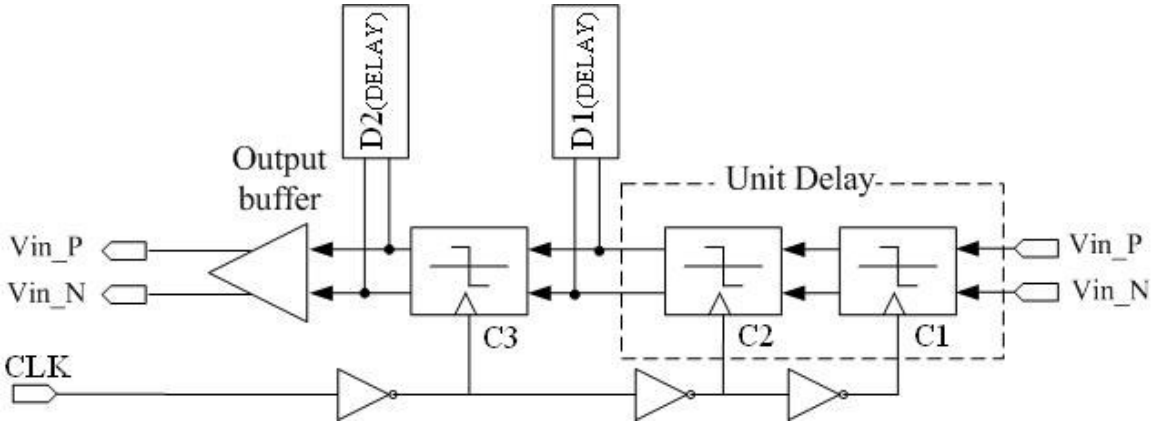


Figure 6.4: Feedback comparator structure to be tested.

The layout of test structures of the output buffer and the feedback comparator is shown in Appendix C. Since the test structures were fabricated along with another design (irrelevant to this work) on the same chip, only the relevant layout parts are shown. Chip photograph of the test structure is shown in Appendix D and the test Printed Circuit Board (PCB) in Appendix E. The RF PCB was laid out using Protel DXP and fabricated with Rodger material dielectric. Transmission lines of 50Ω were also laid out on the PCB for the high frequency input and output signals. Since the frequency is very high, care was

taken such that the power lines are decoupled with capacitors and the transmission lines are properly assisted with ground plane.

6.2.1 Test setup

The test setup is shown in Fig. 6.5. Since the input comparator C1 is a differential dynamic comparator, a DC bias is added to the inputs through the Bias-T in order to keep the input transistors in saturation. A DC bias of *vdd*/2 is also added to the high shoot sine wave before giving it to the buffer. The output RZ pulses are viewed through a digital sampling oscilloscope.

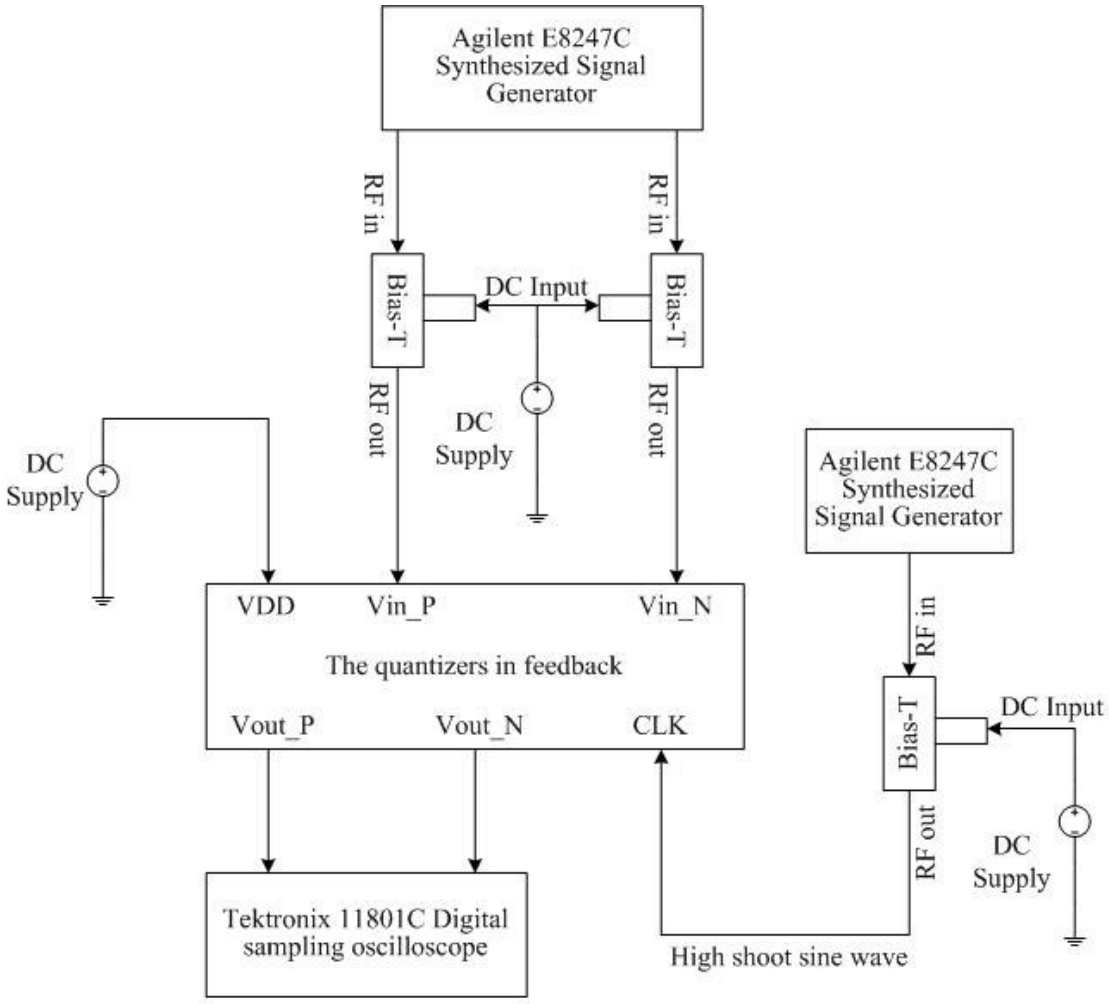


Figure 6.5: Test setup

6.2.2 Test results

Input *Vin_P* of the differential input is held at DC of 900mV and *Vin_N* is excited with a sinusoid with DC shifted to 900mV of different frequencies listed below in Table 6.2 along with the test results. Since the sampling frequency is four times the input, we expect two RZ pulses at both the outputs *Vout_P* and *Vout_N* (as that of Fig. 5.8) for every period of the input sinusoid. The output digital RZ pulses at *Vout_N* and *Vout_P* at 1GHz is shown in Fig.6.6 and that at *Vout_P* at 2.7GHz is shown in Fig. 6.7.

Table 6.2: Test results of the feedback comparator structure

INPUT				OUTPUT						
CLK Freq. (GHz)	Amp. (dBm)	Vin_N (sinusoid)		Freq. (GHz)	Rise (ps)	Fall (ps)	Peak-Peak (mV)	Supply (V)	Current (mA)	Senstivity (mV)
		Freq. (MHz)	Amp. (mV)							
1	8.5	250	200	1	81.22	229.98	558	1.8	41	6
1.3	8.5	325	200	1.3	58	107.03	525.5	1.8	43	11
1.395	8.5	348.7	200	1.395	71.96	235.94	512.63	1.8	44	11
1.6	8.5	398.1	200	1.6	81.3	241.7	443.56	1.8	45	11.9
2	8.5	505	200	2	105.53	229.73	451.17	2	54	30
2.7	8.5	674.9	200	2.7	83.84	54.39	250.94	2.2	67	44.9

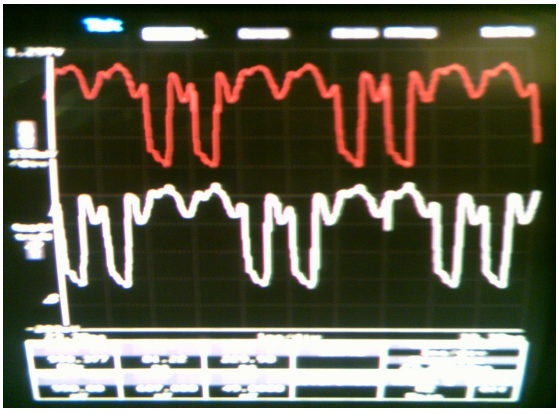


Fig 6.6: Feedback comparator structure at 1GHz

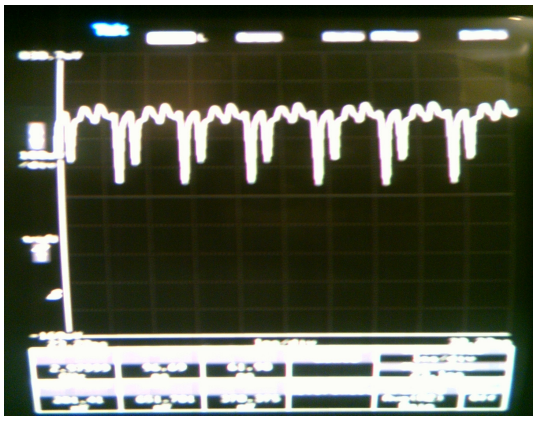


Fig 6.7 Feedback comparator structure at 2.7GHz

6.3 Analyzing the testing results

From the testing results of output buffer in Table 6.1 it is evident that as the sampling frequency increases, the peak-to-peak swing of the digital pulse decreases and also it loses its shape of a square pulse waveform. At 4GHz the swing reduces to 472mV with the maximum amplitude being at 560mV. Apparently the same swing reduction with the increase in sampling frequency happens also with the testing of feedback comparator structure in Table 6.2. Due to the lack of matching network for the above circuits at input and output, this reduction in swing could be the result of reflections in its input and output at higher frequencies. Actually when the sampling frequency is increased beyond 2.7GHz for the feedback comparators structure, both the outputs saturate at positive supply. The reason for the above could be,

1. The inputs suffered reflection before reaching the circuits due to the lack of matching network.
2. The clock swing after the inverters would have been very less to act as sampling clock for the comparators.

The study of actual cause for the above effects is under future scope of investigations. However, the testing of basic structures has strengthened the functionality of the novel architecture.

6.4 The BP CT ΣΔM

The BP CT ΣΔM, whose layout shown in Fig. 5.20, was fabricated and chip photograph is shown in Appendix F. The following test setup in Fig. 6.8 was planned to test the chip. However, further analysis and investigations are needed to improve the

design to work at frequencies beyond 2.7GHz as mentioned above in Sec. 6.3. Hence it is realized that there is a need of second tape out and testing of basic structures before proceeding for the test of BP CT ΣΔM. The second tape out work is considered out of the scope of this thesis due to time constraints and is left for future scope of investigations.

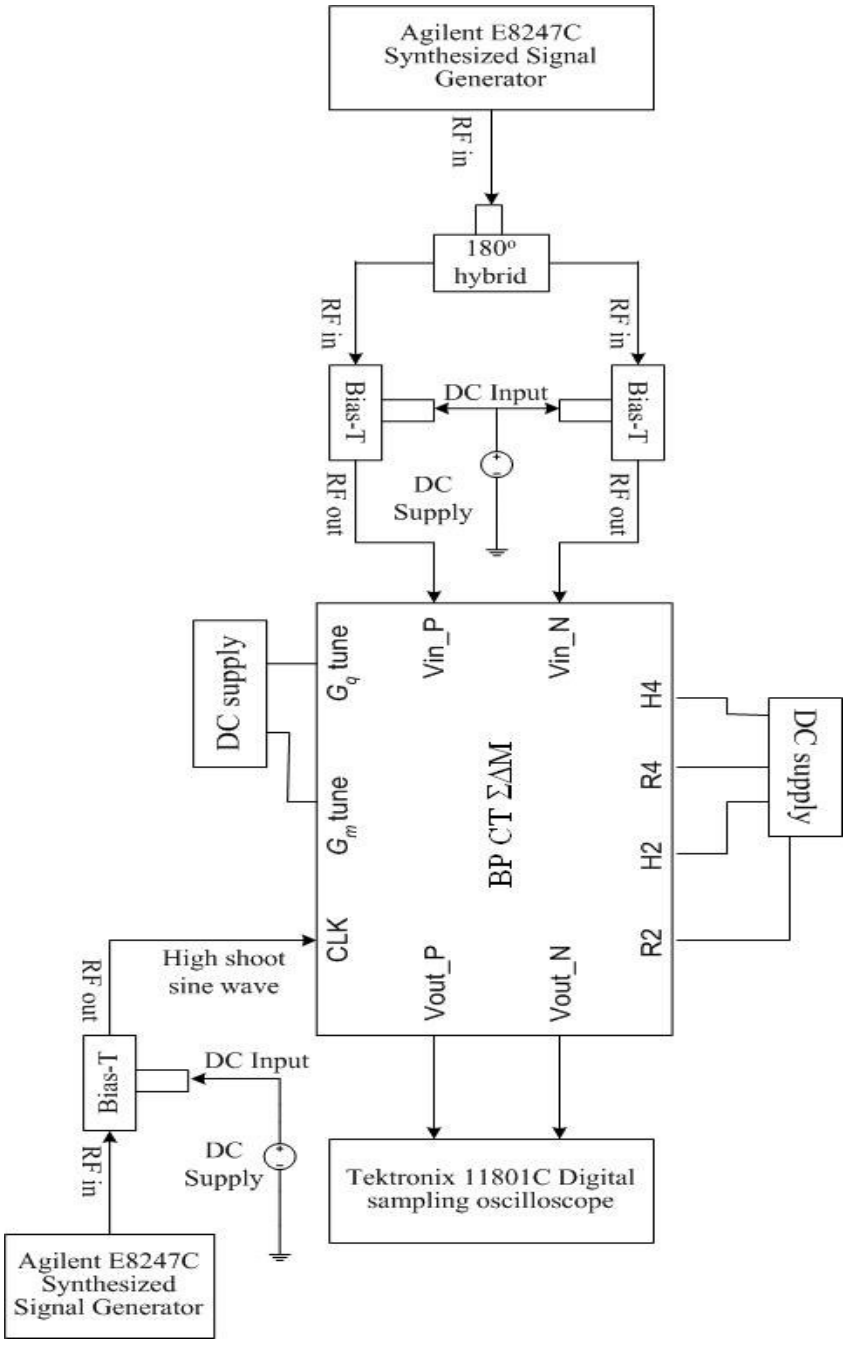


Figure 6.8: Test setup for BP CT ΣΔM.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

A CMOS design of a very high speed 4^{th} order continuous time bandpass Sigma Delta modulator was presented. A novel realization of the feedback architecture was proposed to overcome loop delay in the modulator, thus increasing modulator stability to higher sampling frequencies. Simulation results comparing the conventional architecture and the proposed one were also shown. Analysis on the performance of the modulator shows that it was largely affected by quantizer metastability at such very high sampling frequencies. Test chip was fabricated and testing results along with the test setup suitable for such high frequencies were also discussed.

This work introduces a novel solution to face the design challenge of CMOS realization of very high frequency ADCs.

7.2 Future work

With a stable design of a CMOS ΣΔM sampling at 4GHz, the future work should concentrated on enhancing its performance. The delay D1 and D2 in the modulator of Fig. 5.1 can be replaced with a circuit that can pull the signal at the output of comparator to supply extremes. By this way the delay time can be used in mitigating DAC pulse width variation caused by quantizer metastability (explained in Sec. 4.3).

As mentioned above in Sec 6.3, the cause of swing reduction with increasing sampling frequency and the testing of feedback comparator structure beyond 2.7GHz needs to be investigated further.

Apart from the above, the whole modulator can also be implemented in current domain. This would require current comparators and current mode bandpass filters. Recently reported VHF current mode bandpass filters [38] use fully transistor topology. Hence the area consuming integrated LC resonators can be replaced with transistor only bandpass filters.

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Appendix A: MATLAB Program

```
% To find the DAC feedback coefficients in a Bandpass Continuous time
% Sigma Delta modulator implemented with the multi feedback
% architecture of Fig. 3.4 in Sec. 3.2.
% Here we also  take care of the digital delay in the comparator and implement
% the filter with one coefficient less.
% Program input is the numerator and denominator coefficients of the
% bandpass filter


function  bpdigital_delay_coeff(num2,num1,num0,den2,den1,den0);

% finding the zero-order hold discrete time equivalent for the 2nd order loop

[a2,b2,c2,d2] = tf2ss([num2 num1 num0],[den2 den1 den0]);
continuous_sys_o2 = ss(a2,b2,c2,d2);
discrete_sys_ts_1_o2 = c2d(continuous_sys_o2,1); %equivalence with ts = 1

%adjust for the RZ in 2nd order loop

discrete_sys_RZ_o2 = discrete_sys_ts_1_o2;
discrete_sys_RZ_o2.b = inv(continuous_sys_o2.a)*(expm(continuous_sys_o2.a)-
expm(continuous_sys_o2.a * 0.5))*continuous_sys_o2.b;

%adjust for the HZ in the 2nd order loop

discrete_sys_HZ_o2 = discrete_sys_ts_1_o2;
discrete_sys_HZ_o2.b = inv(continuous_sys_o2.a)*(expm(continuous_sys_o2.a * 0.5)-
eye(size(continuous_sys_o2.a)))*continuous_sys_o2.b;

% finding the zero-order hold discrete time equivalent for the 4th order loop

[a4,b4,c4,d4] = tf2ss([(num2^2) (2*num2*num1) (num1^2 + 2*num2*num0)
(2*num1*num0) (num0^2)],[den2^2 (2*den2*den1) (den1^2 + 2*den2*den0)
(2*den1*den0) den0^2]);
continuous_sys_o4 = ss(a4,b4,c4,d4);
discrete_sys_ts_1_o4 = c2d(continuous_sys_o4,1); %equivalence with ts = 1

% adjust for the RZ in 4th order loop

discrete_sys_RZ_o4 = discrete_sys_ts_1_o4;
discrete_sys_RZ_o4.b = inv(continuous_sys_o4.a)*(expm(continuous_sys_o4.a)-
expm(continuous_sys_o4.a * 0.5))*continuous_sys_o4.b;
```

```
% adjust for the HZ in 4th order loop

discrete_sys_HZ_o4 = discrete_sys_ts_1_o4;
discrete_sys_HZ_o4.b = inv(continuous_sys_o4.a)*(expm(continuous_sys_o4.a * 0.5)-
eye(size(continuous_sys_o4.a )))*continuous_sys_o4.b;

% adjusting to make the 2nd order to 4th order

adjust_o2 = tf([1 0 1],[1 0 1],1);
discrete_trans_RZ_o2 = tf(discrete_sys_RZ_o2) * adjust_o2;
discrete_trans_HZ_o2 = tf(discrete_sys_HZ_o2) * adjust_o2;

% find the transfer function of the systems of order 4

discrete_trans_RZ_o4 = tf(discrete_sys_RZ_o4);
discrete_trans_HZ_o4 = tf(discrete_sys_HZ_o4);

% arrange the coefficients in a matrix

coeff_mat = zeros(4,4);
num_coeff = discrete_trans_RZ_o2.num{:};
coeff_mat(:,1) = num_coeff(2:5)';
num_coeff = discrete_trans_HZ_o2.num{:};
coeff_mat(:,2) = num_coeff(2:5)';
num_coeff = discrete_trans_RZ_o4.num{:};
coeff_mat(:,3) = num_coeff(2:5)';
num_coeff = discrete_trans_HZ_o4.num{:};
coeff_mat(:,4) = num_coeff(2:5)';

% solving for the right hand side of 2*z^3 + z

result = coeff_mat \ [2;0;1;0];
RTZ2 = result(1)
HRTZ2 = result(2)
RTZ4 = result(3)
HRTZ4 = result(4)
```

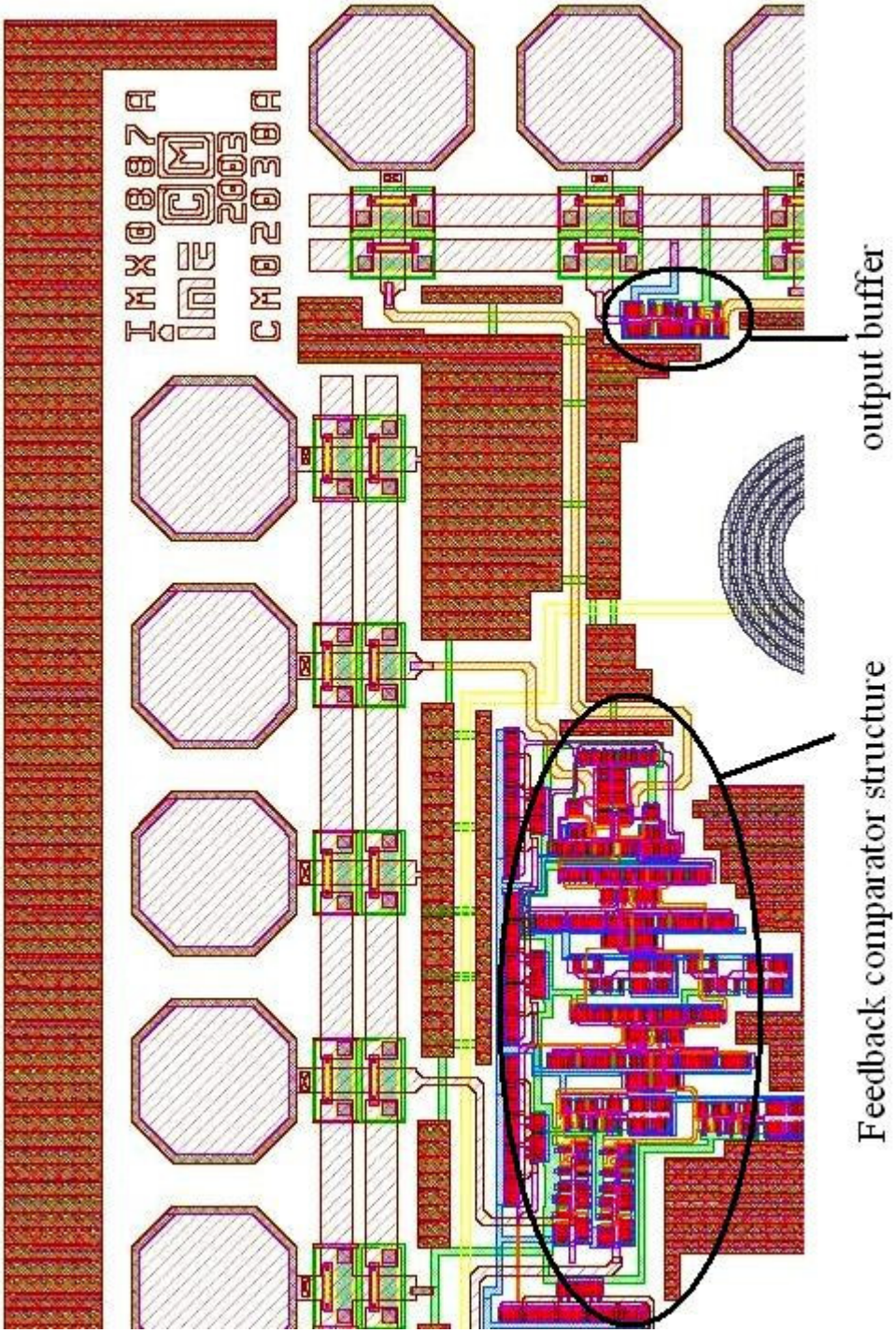
Appendix B: Simulink models

```
% S-function to implement the return to zero DAC

function [sys,x0,str,ts] = RTZ(t,x,u,flag)

% Set the sampling time for the S-function to get executed

sample_period = 0.5;

% set a offset for sampling

sample_offset = 0;

% check for the flag to see which task to perform

switch flag

  case 0         % Initialization
    [sys,x0,str,ts] = mdlInitializeSizes(sample_period,sample_offset);

  case 3
    sys = mdlOutputs(t,x,u,sample_period,sample_offset); % Calculate outputs

  case {1, 2, 4, 9}
    sys = [];       % Unused flags

  otherwise
    error(['unhandled flag = ',num2str(flag)]); % Error handling
end

% Initialization

function [sys,x0,str,ts] = mdlInitializeSizes(sample_period,sample_offset)

% Call simsizes for a sizes structure, fill it in, and convert it
% to a sizes array.

sizes = simsizes;
sizes.NumContStates  = 0;
sizes.NumDiscStates  = 0;
sizes.NumOutputs     = 1;
sizes.NumInputs      = 1;
sizes.DirFeedthrough = 1;
```

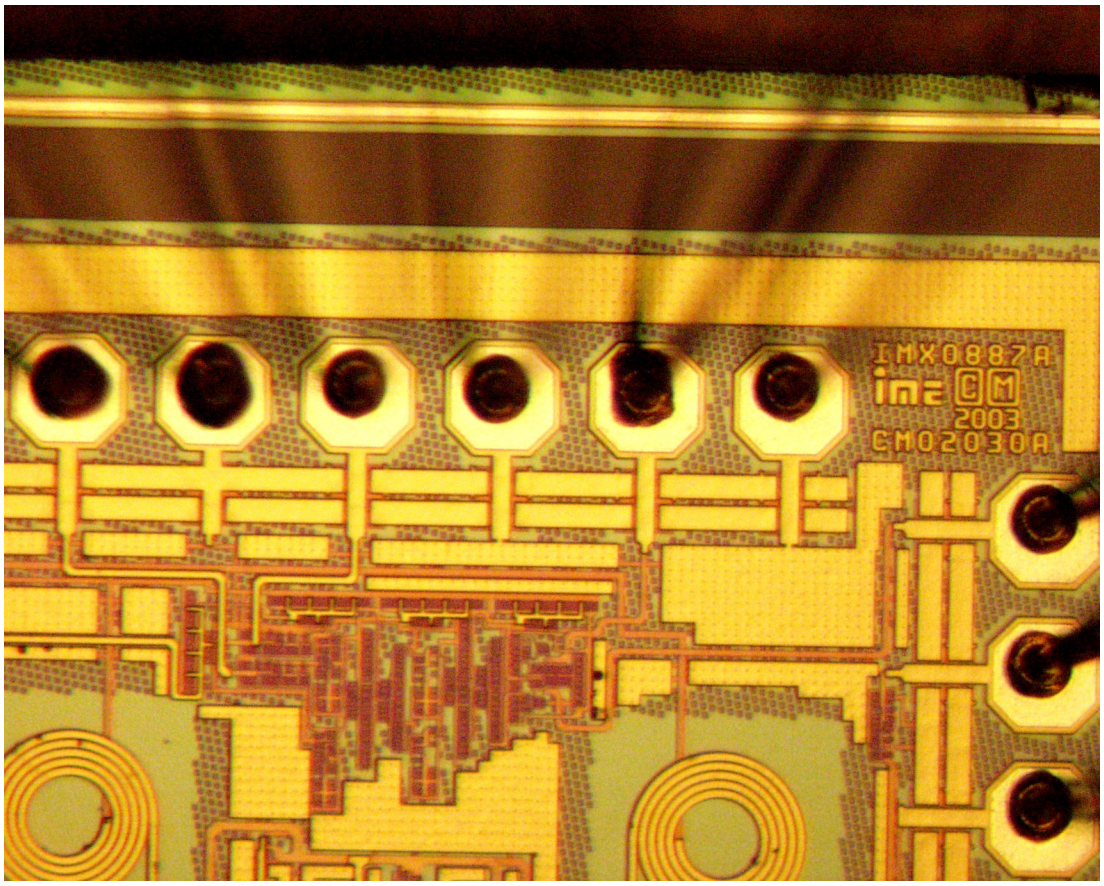
```
sizes.NumSampleTimes = 1;
sys = simsizes(sizes);
x0  = [];
str = [];
ts  = [sample_period sample_offset];       % sample time: [period, offset]

% Calculate outputs

function sys = mdlOutputs(t,x,u,sample_period,sample_offset)

%Genereation of RZ
% check to whether its a even or odd sample time

if rem(((t-sample_offset)/sample_period),2) = = 0
   sys = u ;
else
   sys = 0 ;
end;

% END


==========================================================
% S-function to implement the Half return to zero DAC

function [sys,x0,str,ts] = HRTZ(t,x,u,flag)

% Set the sampling time for the S-function to get executed

sample_period = 0.5 ;

% Set a offset for sampling

sample_offset = 0;

% check for the flag to see which task to perform

switch flag

  case 0        % Initialization
    [sys,x0,str,ts] = mdlInitializeSizes(sample_period,sample_offset);

  case 3
    sys = mdlOutputs(t,x,u,sample_period,sample_offset); % Calculate outputs

case {1, 2, 4, 9}
```

```
   sys = [];       % Unused flags

  otherwise
   error(['unhandled flag = ',num2str(flag)]); % Error handling
end

% Initialization

function [sys,x0,str,ts] = mdlInitializeSizes(sample_period,sample_offset)

% Call simsizes for a sizes structure, fill it in, and convert it
% to a sizes array.

sizes = simsizes;
sizes.NumContStates  = 0;
sizes.NumDiscStates  = 0;
sizes.NumOutputs     = 1;
sizes.NumInputs      = 1;
sizes.DirFeedthrough = 1;
sizes.NumSampleTimes = 1;
sys = simsizes(sizes);
x0  = [];
str = [];
ts  = [sample_period sample_offset];       % sample time: [period, offset]
% End of mdlInitializeSizes.

% Calculate outputs

function sys = mdlOutputs(t,x,u,sample_period,sample_offset)

% Genereation of HZ
% check to whether its a even or odd sample time

if rem(((t-sample_offset)/sample_period),2)== 0
   sys = 0 ;
else
   sys = u ;
end;

% END
```

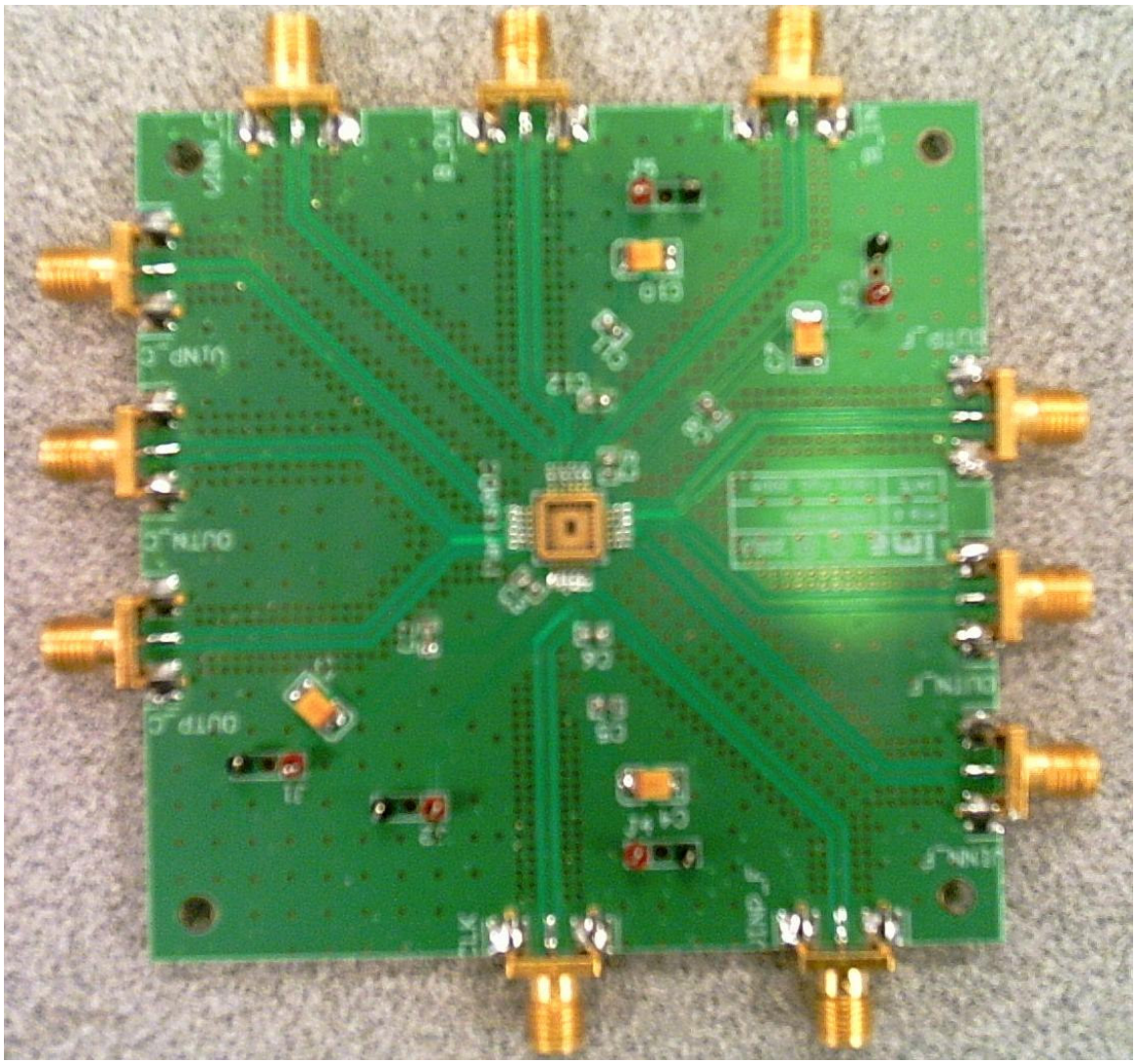
Appendix C: Layout of test structure



Appendix D: Chip photograph of test structure



Appendix E: Test PCB



Appendix F: Chip photograph of CT BP ΣΔM