Semiconductor Nanowires for Future Nanoscale Application: Synthesis, Characterization, and Nanoelectronic Devices

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TABLE OF CONTENTS

Acknowledgements ……………………………………………………………………i

Table of Contents ……………………………………………………………… iii

Summary ……………………………………………………………………………vii

List of Tables ………………………………………………………………….…ix

List of Figures…………………………………………………………………....x

List of Symbols…………………………………...………………………xvi

Chapter 1. Introduction

1.1. Overview………………………………………………………………..1

1.2. Nanotechnology…………………………………………………………...2

1.3. One-Dimensional material ……………………………………………...4

1.3.1. Carbon Nanotube………………………………..………………..4

1.3.2. Semiconductor Nanowire ……………………….…………………7

1.3.2.1. Top Down Method ………………………..………………..7

1.3.2.2. Bottom Up Method ………………………..………………..9

1.4. Semiconductor Nanowire Applications …………………..……………...10

1.5. Schottky Barrier FET …………………..……………………………...12

1.5.1. Basic Conception of Schottky Barrier …………………..………...13

1.5.2. Current transport through the Schottky barrier …..……………..…14

References….……………………………………………………...…………17

Chapter 2. Nanowire Synthesis and Properties

2.1. Introduction ….……………………………………………………….……22

2.2. Vapor liquid Solid mechanism …..……………………….…………..…….23
2.2.1. Phase Diagram ……………..………………………………………..24
2.2.2. VLS mechanism based Nanowire growth …………………………...26
2.3. Experiment Equipment CVD ……………………………………………….29
2.4. Silicon nanowire synthesis …………………………………………………32
2.5. Nanowire Doping Process …………………………………………………..35
2.6. Properties of the fabricated nanowire……………………………………….36
2.6.1. Unintentionally doped SiNW based on Au catalyst …………………36
2.6.2. Doped SiNW based on Au catalyst ……………………………………39
2.6.3. SiNW based on Al catalyst ……………………………………………..43
2.7. Nanowire Surface Treatment ………………………………………………45
2.7.1. Au based SiNW ………………………………………………………...45
2.7.2. Al based SiNW …………………………………………………………46
2.7.3. Summary…………………………………………………………………47
Reference ……………………………………………………………………………48

Chapter 3. Nanowire MOSFET Fabrication and Characteristics

3.1. Introduction ……………….…………………………………………………..51
3.2. Experiment Details ……………………………………………………….....54
3.3. Long Channel Device Characteristics and Analysis ……………………...57
3.3.1. Si Undoped Silicon Nanowire MOSFETs …………………………..57
3.3.1.1. Pd S/D SiNW MOSFET device ……………………………..59
3.3.1.2. Ni S/D SiNW MOSFET device …………………………......59
3.3.2. Doped Nanowire MOSFETs 61
3.3.3. Nanowire MOSFET Device Performance Analysis 65

3.3.3.1. Device Structure 65

3.3.3.2. Unipolar performance 66

3.3.4. Short channel SiNW MOSFET 72

3.3.5. Annealing effect 75

Reference 78

Chapter 4. Temperature Dependence of Carrier Transport of Silicon Nanowire Schottky Barrier Field Effect Transistor

4.1. Introduction 81

4.2. Experiment Details 82

4.3. Device performance in different temperatures 85

4.3.1. I_{ON} and I_{OFF} 85

4.3.2. Schottky Barrier Height Extraction 87

4.3.3. Threshold Voltage (V_{TH}) and Subthreshold Swing (S.S.)...................90

4.3.4. Ti S/D SiNW SB MOSFET 93

4.4. Conclusion 95

References 97

Chapter 5. Electrical Transport of Bottom-Up Grown Single-Crystal $Si_{1-x}Ge_x$ Nanowire

5.1. Introduction 99

5.2. Experiments 100

5.3. $Si_{1-x}Ge_x$ NW MOSFET Performance 103

5.4. Conclusion 111

Reference 112

Chapter 6. Conclusion and Future Work

6.1. Conclusion……………………………………………………………114

6.2. Future Work…………………………………………………………115

6.2.1. Nanowire Synthesis Control………………………………………116

6.2.2. Nanowire Device Integration………………………………………117

6.3. Nanowire Application in Solar Cell………………………………………117

Reference……………………………………………………………………120

Appendix

List of Publications 121

SUMMARY

Semiconductor nanowires have attracted considerable research interest in recent years due to their unique nanoscale size and excellent properties. To meet the aggressive scaling down requirements of the nanoelectronics development, research groups believe that semiconductor nanowires could be one of the most promising building blocks for future device integration. Among many nanowire synthesis methods, Vapor-Liquid-Solid (VLS) mechanism can provide us ideal single crystallized semiconductor nanowires with other advantages such as low cost, fast growing, simple processing steps, and good control of doping process. It will be an interesting project to integrate such nanowires grown by VLS mechanism with back gate dielectric and metal source and drain (S/D) to form novel nanoelectronic devices.

In this thesis, the working Si nanowires (SiNW) Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs) are demonstrated. SiNWs are integrated with High-κ HfO_2 gate dielectric layer and high work function metal S/D (Pd, Ni) to form a back gate device structure. Such nanowire MOSFETs show excellent performance compared with other peer reports. Both the driving current and subthreshold swing (S.S) are improved in our device performance. A very short channel (65nm) SiNW MOSFET is also demonstrated. To make a better metal semiconductor contact, forming gas annealing is carried out to make metal silicidation and the on state current is improved. However, the silicidation consumes Si in the nanowire and nanowire channel become smaller.

Due to the metal-semiconductor contact, Schottky barriers are formed between metal S/D and nanowire channel. We find the Schottky barrier between plays the key role in the nanowire device operation. Due to the back gate device geometrical factor,

gate control of nanowire device is not as strong as conventional planar Silicon MOSFETs. The S/D regions show their effect since it controls the carrier injection at the Schottky barrier. Since high workfuntion metal is utilized to form S/D, holes become the major carriers in nanowire channel. This makes the device working in an accumulation mode and showing p-MOSFET performance. In addition, due to the high and wide barrier for electrons, the electron transport is totally blocked. Therefore, our device shows unipolar device operation which is more applicable for current electronics circuit rather than other reported ambipolar performance.

To further investigate the Schottky barrier, we try to extract the effective and real barrier height for the nanowire device by measuring the device characteristics under different temperatures. Based on the thermoionic theory of Schottky barrier, the Schottky barrier is successfully extracted and explained. The effective Schottky barrier variation with gate bias fully explains the nanowire MOSFET operation. Threshold voltage and subthreshold swing variation with temperature also indicates the Schottky barriers effect on the nanowire MOSFETs operation.

We also integrate $Si_{1-x}Ge_x$ nanowires to form back gate MOSFETs. To improve the device performance, three different $Si_{1-x}Ge_x$ nanowire devices are demonstrated. Based on the device performance of undoped and phosphorus doped $Si_{1-x}Ge_x$ nanowire MOSFETs, we believe the Schottky barrier width is the key issue for tunneling current. For doped nanowire device, it has higher tunneling current part. This barrier width factor can also be equivalent as effective Schottky barrier. Thus, even negative barrier height is observed. Recently, semiconductor nanowires are not only intergrated in nano MOSFET process, but also in fabrication of photovoltaic devices. This new application of nanowire can provide us solar cells with lower cost and higher efficiency.

LIST OF TABLES

Table 1.1	Introduction of roadmap challenges addressed by SB-MOS. Most of the categories have multiple line items in the detailed roadmap tables.	13
Table 2.1	Eutectic temperatures for binary alloy of various elements with Si and Ge	29
Table 2.2	Summary of different nanowires synthesis recipes	34
Table 2.3	List of different nanowire doping process recipes separated by using thermal doping, plasma doping and simultaneous doping.	35
Table 3.1	Summary of device performance of previous reported back gate nanowire MOSFETs by other research groups	53
Table 5.1	Three different SiGe NW MOSFETs with different NWs and thick HfO_2 layer are investigated.	103
Table 5.2	Comparison of performance parameters of different $Si_{1-x}Ge_x$ nanowire MOSFETs, (a) undoped $Si_{1-x}Ge_x$ nanowire MOSFET with 20 nm HfO_2, (b) phosphorus-doped $Si_{1-x}Ge_x$ nanowire MOSFET with 20 nm HfO_2, (c) phosphorus-doped $Si_{1-x}Ge_x$ nanowire MOSFET with 5 nm HfO_2 gate dielectric layer.	108

LIST OF FIGURES

Figure 1.1	CPU transistor counts from 1970s to present, showing the device scaling according to Moore's Law; © Intel corp.	2
Figure 1.2	Nanotechnology is focused on extremely small research objects. The target is to control and investigate smaller and smaller material.	3
Figure 1.3	Schematic pictures of carbon nanotube (CNT) building blocks. CNTs can be either metallic or semiconducting depending on their chirality and enable them to be used for different nanodevices.	5
Figure 1.4	Figure 1.4: (a) Schematic picture of a typical back gate CNT FET [13]. (b) (Top) SEM image of a partially gated CNT FET [14]. (c) Schematic picture of back gate CNT FET structure (cross section view) [14].	6
Figure 1.5	Building block for top-down (conventional technology) and bottom-up approach [26].	8
Figure 1.6	SEM picture of nanowire formed by top down method. (a) the top view of nanowire device, the nanowire channel is suspended between contacts. (b) The cross section view of nanowire core surrounded by other materials [30].	9
Figure 1.7	The Schottky barrier formation between metal and n type semiconductor when the two materials are connected [60].	15
Figure 2.1	(a) binary phase diagram of Au and Si. The eutectic temperature is 363°C. (b) Binary phase diagram of Au and Ge. The eutectic temperature is 356°C. (c) Binary phase diagram of Al and Si. (Source from SGTE - SGTE Alloy Phase Diagrams)	24
Figure 2.2	Ternary phase diagram of Au-Si-Ge. The lowest eutectic temperature is ~350°C	26
Figure 2.3	Schematic process steps for nanowire growth under VLS mechanism	27
Figure 2.4	The birth of a semiconductor nanowire on an Au nanocluster, as observed using in-situ TEM. It is clearly seen that the Au nanocluster started to melt after the formation of GE-Au alloy, and this was followed by an increase in the liquid droplet size during the Ge vapor condensation process.	27

Figure 2.5	The schematic of single wafer loaded type CVD machine for growth of nanowire.	30
Figure 2.6	Schematic picture of gas flow in the main chamber. The gas flow direction has been indicated. Clearly, the gas can fully support the VLS growth at the platform.	30
Figure 2.7	The real temperature at the centre platform in chamber versus the setting temperature. The real temperature in the main chamber is higher than the setting temperature in our recipe.	31
Figure 2.8	The detail process-flow of the sample preparation for nanowire growth. 1. We have p-type Si wafer with 400nm SiO_2 by thermal oxidation. 2. Positive charged poly-l-lysine is dispersed on the substrate. 3. Dispersion of negative charged Au nanocolloids on the substrate. The colloids are attached by poly-l-lysine. 4. The substrate is dried by nitrogen gas. 5. Nanowires are synthesized on this substrate.	32
Figure 2.9	SEM picture of Au catalyst dispersion on the substrate by using Poly-l-lysine.The density of Au nanocolloids	33
Figure 2.10	SEM picture of grown undoped SiNWs on SiO_2 substrate. Numerous nanowires can be obtained after the synthesis process.	37
Figure 2.11	TEM picture of single crystalline SiNW grown on Au catalyst. The diameter is very consistent with the Au catalyst size.	38
Figure 2.12	(a) XPS data of undoped SiNW grown on 20nm Au catalyst with SiH_4: 200sccm, H_2: 200sccm, at 550°C. The Si peak is clearly detected. (b)AES data of composition detection at the stem of undoped SiNW. The nanowires are grown at different temperatures. Si content is high. Oxygen, and carbon element is negligible.	38
Figure 2.13	SEM picture of phosphorus doped SiNW by plasma doping process. The nanowire growth is not interrupted by the introduction of PH_3 or B_2H_6.	39
Figure 2.14	XPS data of boron and phosphorus doped Au SiNW. (a) Boron concentration is detected by XPS. Plasma doping process shows the highest boron peak, and thermal doping process shows lower doping concentration. There is no boron detected in undoped SiNW. (b) XPS data analysis of phosphorus detection in PH_3 plasma doped and undoped SiNW.	41

Figure 2.15 TEM picture and EDS data for doped nanowire. (a) TEM picture of doped nanowire with Au tip. (b)TEM picture of stem of doped Au SiNW. Table: the EDS data of detected area on the nanowire. The boron concentration is high at the surface of nanowire. And again, no Au is detected in the nanowire stem. 42

Figure 2.16 SIMS data to show the (a) Boron and (b) Phosphorus concentration in the plain Si substrate by plasma doping process. 42

Figure 2.17 SEM picture of AlSi nanowires with huge density but with different diameters. Scale bar: 10μm. 43

Figure 2.18 TEM picture and EDS data for undoped AlSi nanowire. (a)TEM picture of singlr AlSi nanowire. 5 positions on the tip, surface, and core of nanowire are detected by EDS. (b) TEM picture of AlSi nanowire. The amorphous layer is clearly indicated. Table: EDS data of atomic concentration of Si and Au in the different positions of AlSi nanowire. 44

Figure 2.19 SEM picture of (a) original SiNW grown by Au catalyst before Aqua Regia etch; (b) SiNW after the 1 hour etch. The Au tip has been removed totally. 46

Figure 3.1 Schematic picture of back gate nanowire MOSFET device structure. The nanowire is connected by two metal terminals. The bottom SiO2 is used as gate dielectric to control the device operation [15]. 52

Figure 3.2 Schematic process flow of Schottky barrier nanowire MOSFET fabrication. (a) Ta/TaN layer is sputtered on 400nm SiO_2 layer. (b) High-κ gate dielectric material (Al_2O_3 or HfO_2) is deposited on the TaN back gate. (c) Grown nanowires are suspended in IPA solution by ultrasonic vibration. (d) The nanowire contained IPA is dipped on the gate dielectric layer. (e) Source and Drain (S/D) patterns are defined by EBL system. (f) Metal S/D is deposited on the substrate followed by lift-off process. After gate opening, the device is measured in the probe station. 54

Figure 3.3 SEM picture of fabricated SB SiNW MOSFET (top view). The Source/Drain size is 50×50 μm for contact. The nanowire channel length is 1 μm. 56

Figure 3.4 SEM picture of fabricated long channel undoped SiNW MOSFET (1um length). The nanowire is fixed on gate dielectric layer HfO2 (20nm). The two terminals of nanowire are covered by the Source/Drain material Pd (80nm). 57

Figure 3.5 Device characteristics of 1um gate length SiNW MOSFET with Pd S/D (a) I_{GS}-V_{GS} Transfer characteristics. Gate voltage sweeps from +3 to -3V. (b) I_{DS}-V_{DS} output characteristics. 58

Figure 3.6 Device characteristics of 1um gate length SiNW MOSFET with Ni S/D (80 nm) and Al2O3 gate dielectric (20 nm). (a) IGS-VGS Transfer characteristics. Gate voltage sweep from +2 to -2V. (b) IDS-VDS output characteristics. 60

Figure 3.7 Device performance of phosphorus doped SiNW MOSFET with Ni S/D and SiO_2 50nm. a) (a) Id-Vg Transfer characteristics. Gate votalge sweeps from +5 to -5V. (b) Id-Vd output characteristics. Vgs starts from -1V, step +1V. 62

Figure 3.8 Device performance of boron doped SiNW MOSFET with Ni S/D and SiO_2 50nm. a) (a) I_{ds}-V_{gs} Transfer characteristics. Gate votalge sweeps from +5 to -5V. (b) I_d-V_d output characteristics. V_{DS} starts from -1V, step +1V. 63

Figure 3.9: Schematic picture of nanowire MOSFET. a) the crossection view of S/D area of the device. The nanowire is covered by metal S/D and gate dielectric has point contact at the bottom. b) the resistance distributed in the nanowire device. The R_{SB} is the Schottky barrier resistance; R_{NW} is the resistance of nanowire; R_{metal} is the resistance of metal 66

Figure 3.10 A typical ambipolar transfer characteristic of an 800 nm CNFET at different processing stages. 67

Figure 3.11 Band diagram along SiNW channel from Source to Drain under different bias voltage (a) At thermal equilibrium status without any gate or drain bias. (b) Negative gate and drain bias (V_g<0, V_{ds}<0) (c) positive gate and negative drain bias (V_g>0, V_{ds}<0) 69

Figure 3.12 Phosphorus doped SiNW device band diagram variation when gate bias is applied. a) at thermal equilibrium status, holes are blocked the Schottky barrier. Electrons can tunnel through the barrier. b) when positive gate bias is applied, more electrons can tunnel through the barrier. Without thermal injection, the tunneling current is smaller compare with undoped or p-type SiNW based devices drive current. 71

Figure 3.13 Top view SEM picture of fabricated device structure, and back gated MOSFET with only 65nm gate length. 73

Figure 3.14 Device performance comparison of long channel (1um) and short channel SiNW MOSFET with same metal S/D and gate dielectric. (a) I_d-V_g Transfer characteristics of short channel 74

SiNW MOSFET. b) Id-Vd output performance of short channel device. (c) -V_g Transfer characteristics of long channel SiNW MOSFET with same gate dielectric and metal S/D as short channel device. (d) Id-Vd output performance of short channel device.

Figure 3.15 Transfer characteristics of the same nanowire device measured before and after forming gas anneal. 75

Figure 3.16 The nanowire is consumed after forming gas anneal. Metal silicide is diffused into the SiNW. 76

Figure 4. 1 TEM image of single crystal SiNWs with diameter in ~20nm synthesized at 440°C by VLS mechanism. Inset: SEM image of SiNWs (length > 10μm). inset: top view of SiNW grown on substrate 83

Figure 4.2 schematic p icture of fabricated SiNW MOSFET with SiO_2 capping layer 83

Figure 4. 3 (a)Top view SEM picture of fabricated SiNW SB MOSFET with Al_2O_3 gate dielectric and SiO_2 capping layer, and (b) magnified SEM picture of SiNW SB MOSFET with 1μm gate length. 84

Figure 4.4 (a)Typical I_{DS}-V_{GS} transfer characteristic of Pd S/D SiNW SB MOSFET at different temperatures (T=192K, 200K, 225K, 250K, 300K, 350K, 400K, and 450K from bottom to top) in both log and linear scale. (b) I_{DS}-V_{DS} output characteristics of the same device at room temperature. 86

Figure 4.5 Effective Schottky barrier height as a function of V_{GS} (at V_{DS}= -0.1V) for Pd S/D SiNW MOSFET extracted at different temperatures (200K/225K, 200K/300K). Inset: i) the schematic band diagram at the interface of source and channel at equilibrium state. ii) the schematic band diagram at the interface of source and channel at device "ON" state. 88

Figure 4. 6 Band diagram of Source-nanowire interface a)at thermal equilibrium status, the barrier width is large due to the undoped nanowire properties. b) when negative gate bias ia applied, the effective barrier height is lowered down and real barrier height can be extracted. At the same time, the barrier width is also reduced. c) Further negative gate bias pull up the band of SiNW and the barrier width is small enough for holes to tunnel through. 89

Figure 4.7 Temperature dependence of threshold voltage (V_{TH}) (open square symbol) and subthreshold swing (S.S.) (solid circle symbol) of Pd S/D SiNW MOSFET. 90

Figure 4.8	Transconductance (G_M) as a function of Temperature variation for Pd S/D SiNW MOSFET at 200 ~ 450K.	92
Figure 4.9	(a) Typical I_{DS}-V_{GS} transfer characteristic of Ti S/D SiNW MOSFET at different temperatures (T=178K, 200K, 250K, 300K, 400K, and 450K from bottom to top). (b) I_{DS}-V_{DS} output characteristics at room temperature.	94
Figure 4.10	Extracted effective Schottky barrier height as a function of V_{GS} (at V_{DS}= -0.1V) for Ti S/D SiNW MOSFET at different temperatures. Inset: schematic picture of thermally assisted tunneling at valence band under negative gate bias.	95
Figure 5.1	Cross sectional schematic picture of a back-gated Si1-xGex nanowire MOSFET with high-κ dielectric and TaN gate.	101
Figure 5.2	SEM image of undoped $Si_{1-x}Ge_x$ NWs grown by VLS mechanism. Inset: TEM picture shows SiGe NW has single crystalline structure.	101
Figure 5.3	XPS graph proves that Ge 2p spectra detected in $Si_{1-x}Ge_x$ nanowire after growing at 430 °C (detecting angle: 10°).	102
Figrue 5.4	TEM picture of single crystallized phosphorus doped $Si_{1-x}Ge_x$ NW. inset picture: the Si, Ge and phosphorus contents are detected by EDS.	103
Figure 5.5	Typical I_{DS}-V_{GS} transfer characteristics of device A and B. V_{GS} sweeps from +3 to -3V.	104
Figure 5.6	Typical I_{DS}-V_{DS} output characteristics for device A and B.	104
Figure 5.7	(a): shows comparison of depletion width (W_D) in the band diagram of metal/$Si_{1-x}Ge_x$ NW at Source region under thermal equilibrium status. (b) Comparison of W_D in the band bending diagram of metal/$Si_{1-x}Ge_x$ NW interface at Source region under negative gate bias condition.	105
Figure 5.8	(a) Typical I_{DS}-V_{GS} transfer characteristics for phosphorus doped $Si_{1-x}Ge_x$ NW MOSFET with thinner HfO_2 dielectric layer (device C). (b) Typical I_{DS}-V_{DS} output performance of device C.	107
Figure 5.9	Effective hole barrier height as a function of V_{GS} for three $Si_{1-x}Ge_x$ MOSFETs	110

LIST OF SYMBOLS

A^*	Effective Robinson constant
C_d/C_{dm}	Depletion layer capacitance
C_{ox}	Gate oxide capacitance
d_{ox}	gate oxide thickness
E_c	Conduction Band
E_f	Fermi Level
E_g	Band gap energy
E_v	Valence band
$\Phi_{\nu B}$	Schottky barrier height for electrons
$\Phi_{\pi B}$	Schottky barrier height for holes
Φ_m	Metal work function
G_M	Transconductance
h	Planck constant
I_{DS}	current transporting in the device channel
I_{off}	current transporting when device is turned off
I_{on}	current transporting when device is turned on
J_n	the current density of the net current flow through the barrier
J_n	current density of the net current flow through the barrier
k	Boltzmann constant
m^*	effective mass of carrier
N_A	the acceptor impurity density
q	Elementary charge

S.S.	Subthreshold Swing
T	absolute temperature
t_{ox}	gate dielectric physical thickness
V_{bi}	the built-in voltage
V_{DS}	drain bias on the device
V_{GS}	gate bias on the device
ξ_{ox}	gate oxide permittivity
ξ_{Si}	Silicon permittivity
χ	electron affinity in semiconductor

Chapter 1

Introduction

1.1 Overview

Since late 1980s, electronics industry is dominated by the planar Si-CMOS devices. It has been possibly mainly due to the monolithic integration of complementary devices with tremendously large density and functionalities. It is also due to the scalable nature of the MOS architecture as it has been sustaining the scaling activities since its invention in early 1960s without major changes in the physical appearance. Semiconductor manufacturing industry is always trying to make faster, smaller and lower power consuming electronic devices to meet people's high demanding. In the last four decades, semiconductor industry developed extremely fast based on the Moore's Law (seen in Figure 1.1), which indicates that the number of transistors that can be placed inexpensively on an integrated circuit has increased exponentially, doubling approximately every two years [1]. To keep this fast pace of development, the industry developed the International Technology Roadmap for Semiconductors (ITRS). The goals of this roadmap are to make a global standard, point out potential technology issues and guide further research direction [2]. In the last few decades, semiconductor devices technology innovation has focused primarily on the new lithography tools, masks, photoresist materials, and critical dimension etch

processes. These technologies have developed to a point that engineering is now on the nanoscale. In order to further improve transistor density, engineering must be performed approaching the atomic level. However, this planar device architecture with conventional materials is now gradually approaching the physical boundary limit. Therefore, the industry is collaborating with academic research groups to identify and develop novel ways to further extend semiconductor technology and innovation. One of these approaches is known as nanotechnology [3], which involves investigating and developing techniques to work at nanoscale range.

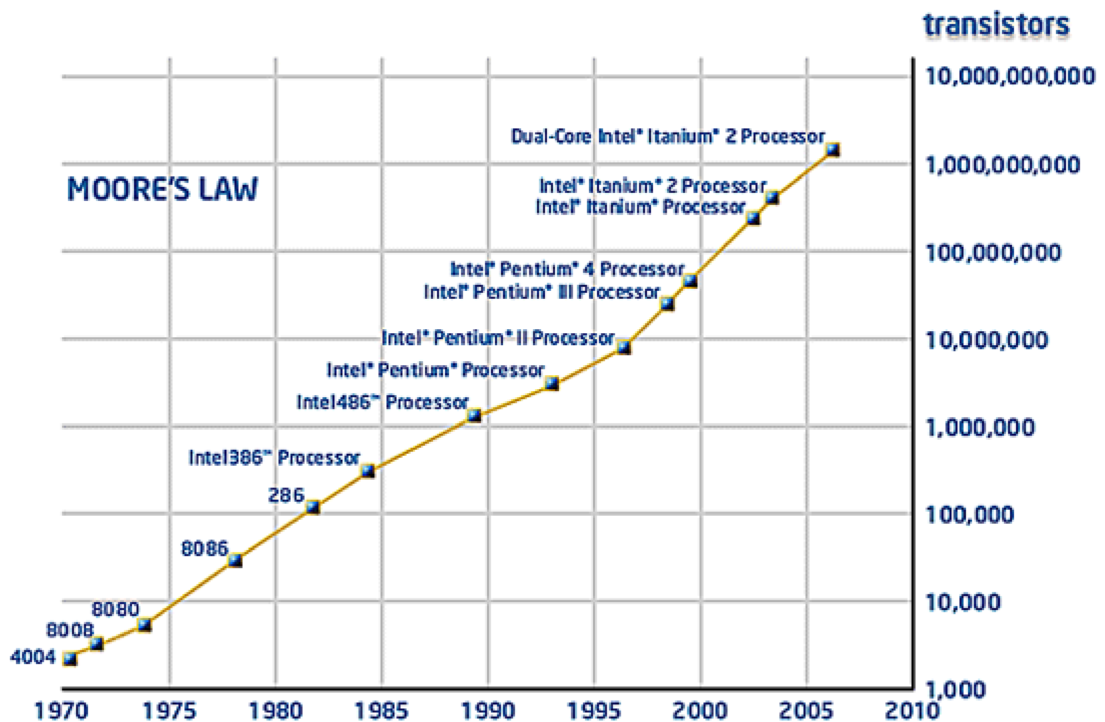

Figure 1.1: Illustration of Moore's law in conventional semiconductor industry: number of transistors integrated in the different generations of Intel's microprocessors vs. the production year of these circuits© Intel corp [4].

1.2 Nanotechnology

Nanotechnology is the study of the control of matter on an atomic and molecular scale. Generally, nanotechnology deals with structures of the size 100

nanometers or smaller, and involves developing materials or devices within that size (shown in Figure 1.2). This approach can be traced back to the famous talk "There's Plenty of Room at the Bottom," given by Richard Feynman at Caltech on December 29, 1959. Feynman described a process by which the ability to manipulate individual atoms and molecules might be developed, using one set of precise tools to build and operate another proportionally smaller set, so on down to the needed scale. In the last several decades, more and more advanced deposition equipment, probe and detection tools, such as chemical vapor deposition (CVD), scanning electron microscope

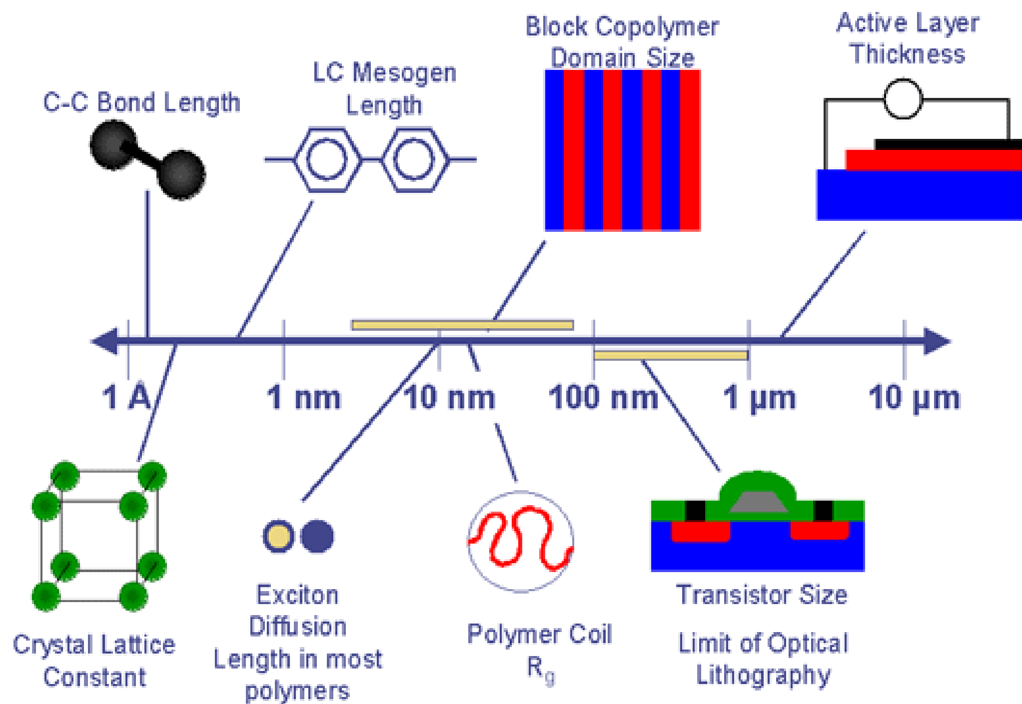

Figure 1.2: Nanotechnology is focused on extremely small research objects. The target is to control and investigate smaller and smaller material [5].

(SEM), atomic force microscope (AFM), X-ray photoelectron spectroscopy (XPS), Transmission electron microscopy (TEM), and electron beam lithography (EBL), were invented. These technology breakthroughs not only help us to investigate

smaller stuffs, but also expand our research area to many disciplines. Nanotechnology is not only limited in physics or electronics, it also includes a large range of science disciplines, including chemistry, biology, and photonics. Hence, nanotechnology also has different sub research areas. Pushed by the development goals of the microelectronic industry, nanotechnology especially nanoelectronics has developed extremely fast over the last two decades. A primary goal of nanoelectronics research is to develop nanoscale semiconductor devices, in an attempt to further reduce the size of semiconductor technology in line with Moore's law.

1.3 One-Dimensional material

One of the key considerations of nano sized MOSFETs is the design of the device channel. Normally, the channel material in industry is Silicon (Si) or Germanium (Ge). With the aggressive scaling down process, both the length and width of the channel must be reduced. One dimensional materials (1-D materials), which have a longer than 1um and a smaller width than 100nm in diameter, are promising candidates for the device channel.

1.3.1 Carbon nanotube

Among the 1-D materials, two approaches have attracted great attention in recent years. One of these is called "carbon nanotube" (CNT) [6]. Carbon nanotube is a fullerene molecule having a cylindrical or toroidal shape. They are molecules composed entirely of carbon atoms. The carbon atoms are usually arranged in a hexagonal pattern, bonded together with extremely strong covalent bonds. A carbon nanotube can be visualized as a finite number of carbon graphite shells arranged around a hollow center axis with a constant spacing of around 0.34 nm (shown in Figure 1.3), a tubular diameter normally ranging from 2-25 nm, and with lengths up to

several microns. Its length can reach to >10um while its diameter is smaller than 10nm. Therefore it can reach a length-to-diameter ratio of up to 28,000,000:1. Techniques have been developed to produce nanotubes in sizeable quantities, including arc discharge [7], laser ablation [8, 9], and chemical vapor deposition (CVD) [10].

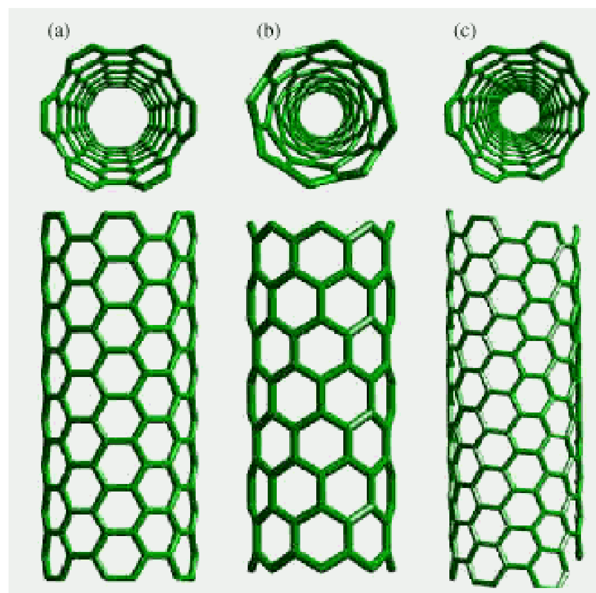

Figure 1.3: Schematic pictures of carbon nanotube (CNT) building blocks. CNTs can be either metallic or semiconducting depending on their chirality and enable them to be used for different nanodevices [11].

Based on the number of graphite shells rolled in one 1-D material, carbon nanotubes can be divided by two types: single walled nanotubes (SWNT) and multi walled nanotubes (MWNT). A SWNT can be viewed conceptually as a grapheme sheet rolled up into a seamless hollow cylinder with a typical diameter on the order of 1.4nm [12]. A multi-walled carbon nanotube consists of concentric cylinders with an interlayer spacing of 3.4Å and a diameter of typically 10-20nm. Detailed theoretical studies have shown that a single walled nanotube behave as a metallic,

semiconducting, or semi-metallic wire depending on its chirality and diameter [11]. There has been tremendous interest in investigating semiconducting single-walled nanotubes due to its ultra-small size and unique physical and chemical properties. Nanotubes can be used individually or as an assembly to build functional device

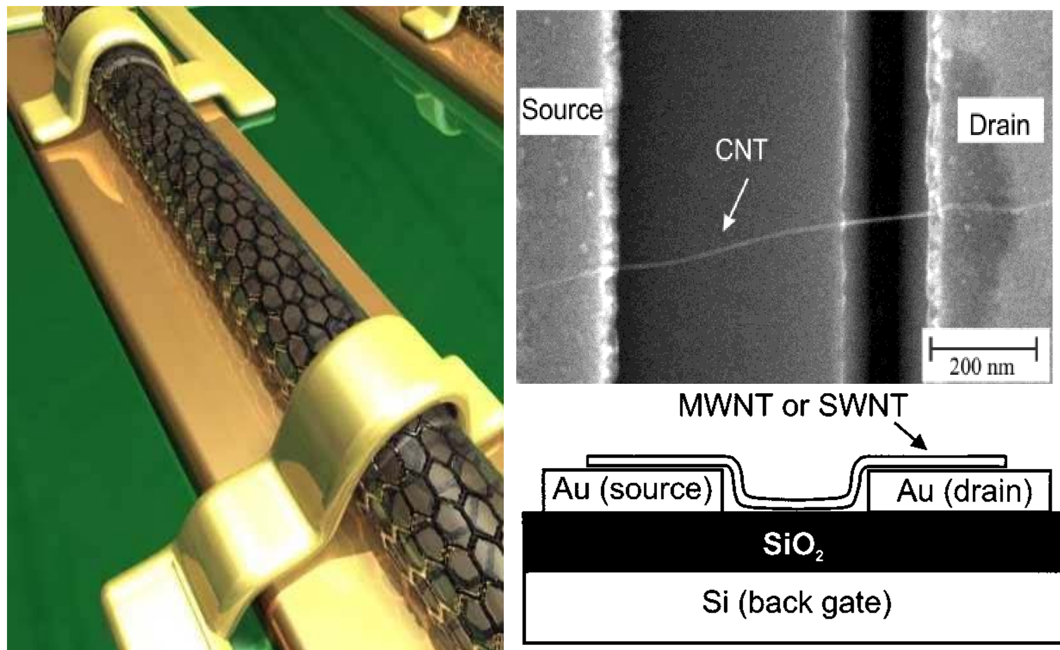

Figure 1.4: (a) Schematic picture of a typical back gate CNT FET [13]. (b) (Top) SEM image of a partially gated CNT FET [14]. (c) Schematic picture of back gate CNT FET structure (cross section view) [14].

prototypes. For example, it is used in integrated circuit interconnect, photonics, nanomechanics, gas detectors, SEM probes, oscillators. The most important point is that its semiconducting properties make it a good candidate as central element of nanoelectronic devices including field-effect-transistors (FETs), as shown in Figure 1.4 (a).

The very first CNT FET was reported by Ph. Avouris group in 1998 [14]. They placed the CNT on the SiO_2 back gate dielectric substrate (shown in Figure 1.4 (b)). By varying the gate voltage, the conductance of a single-wall device could be modulated by more than 5 orders of magnitude. However, multi-wall nanotubes show

typically no gate effect. Further advances have been published with even excellent performance, for example Dai *et.al.* reported ballistic transport in CNT FET [15] and Infinieon showed very short channel CNT FET [16].

However, the nanotube has some disadvantages, particularly when used as the device channel in a FET. First, the inability of controlling selective growth of semiconducting or metallic carbon nanotubes is a serious challenge for scientists. Some creative methods have been invented to solve the problem [17], but significant research is still needed. Secondly, the hollow structure of nanotubes makes it difficult for doping by using other dopant elements. Therefore the advantages of semiconductor materials cannot be fully utilized.

1.3.2 Semiconductor nanowire

Semiconductor nanowires (NWs) [18] are another important type of 1-D wire structure material for nanotechnology research. In contrast to a carbon nanotube, it is solid state which can be predictably synthesized in a single crystal form with all key factors controlled, including chemical composition, diameter and length, and doping properties. Semiconductor nanowires can be formed from many elements and their compounds, such as Silicon (Si) [19, 20], Gemanium (Ge) [21], SiGe [22], GaAs [23], InP [24], ZnO [25]…. These materials can be used in many applications, such as CMOS technology, photonics, quantum computer, nano-robots, thermal electrics, and solar cells. There are two fabrication method to synthesize nanowires. One is so called “top-down” mehod by which nanowire is etched from the thin film materials. The other is “bottom-up” method, by which the nanowire is grown from the substrate. The schematic diagram of the two methods is shown in Figure 1.5.

1.3.2.1 Top down method

For decades, the fabrication of conventional silicon electronics has been dominated by "top-down" manufacturing strategies for decades. The small features are patterned in bulk silicon materials by lithography and wet or dry etched to form device structure as shown in Figure 1.6. Very complicated patterns on the substrate can be defined by controlling the light exposure and using accurate alignment tools. This advantage is very significant for industry manufacturing purposes. In recent years, Si or SiGe nanowires have been fabricated by this method and have been integrated into MOSFET fabrication [27-29]. The diameter of the nanowire can reach 5nm [27]. However, the main disadvantage of this method is the high cost. The exponentially increased cost for building new generation lithography and production lines may not be cost-effective. Furthermore, since the deposition and etch techniques

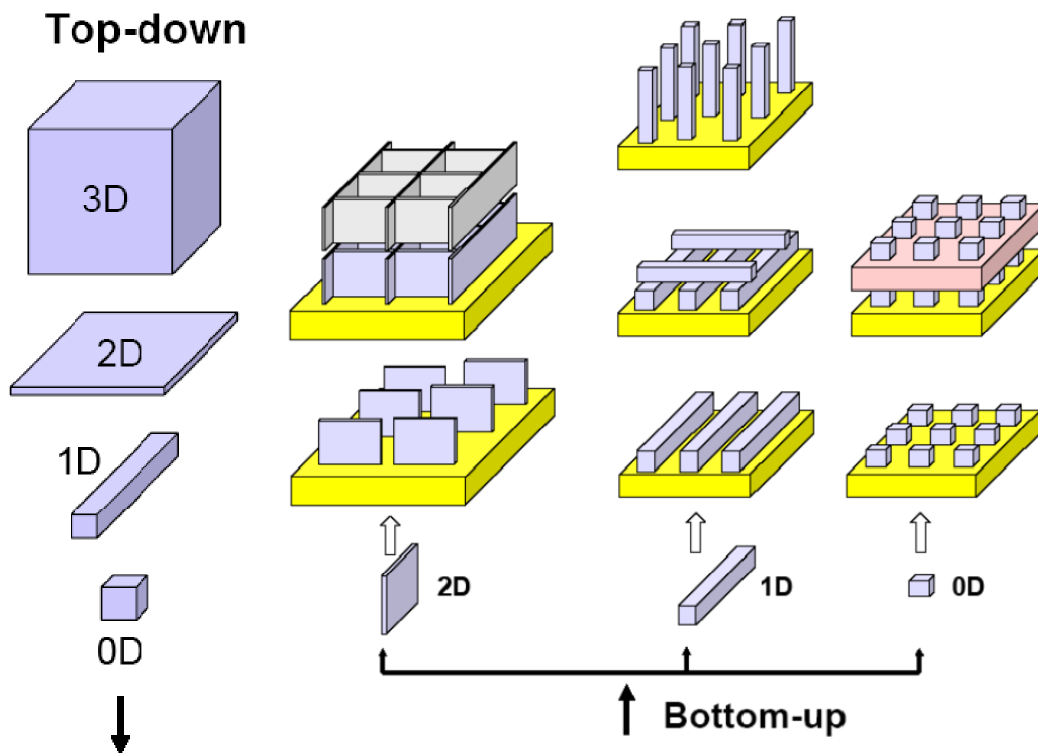

Figure 1.5: Building block for top-down (conventional technology) and bottom-up approach [26].

waste most of the input materials, this method is very expensive relative to the whole system setup. Research in this area is not affordable for most research institutes in the world. Therefore, a cheaper and efficient method to create nanowires needs to be developed. [30]

1.3.2.2 Bottom up method:

The traditional approach for integrated circuit is depositing a thin film on the

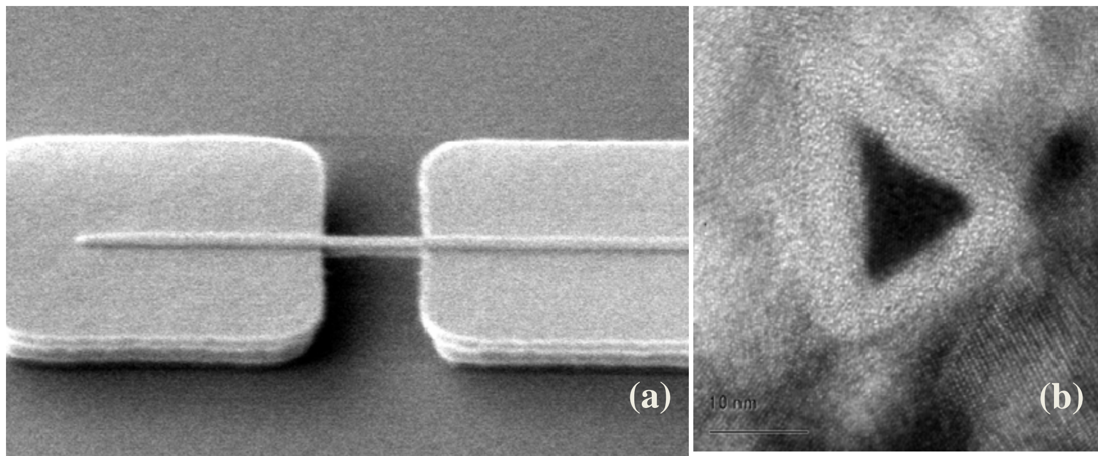

Figure 1.6: SEM picture of nanowire formed by top down method. (a) the top view of nanowire device, the nanowire channel is suspended between contacts. (b) The cross section view of nanowire core surrounded by other materials [30].

top of substrate and patterning design then etching to form device structure following a top down method description. We now consider a bottom up approach. A bottom up approach, which assembles the essential functional targets on the bulk substrate, could be a very promising alternative for future nanoelectronics. It has the potential to go far beyond of the limits of top down technology by defining key nanometer scale functional devices through synthesis and subsequent assembly, rather than lithography.

Many bottom up methods have been developed to grow nanowires, such as vapor-liquid-solid (VLS) mechanism [31], solid-liquid-solid (SLS) mechanism [32], molecular beam epitaxy (MBE) method [33] and so on. The biggest advantage of the bottom-up methods is low cost. We can provide mass production of high quality nanoscaled material in a very short time. Although such methods do not yet compete with current silicon processing technologies, they represent very competitive candidates to replace current top-down processing in the future, if accurate alignment control can be achieved. Here, we are using VLS mechanism to synthesize semiconductor nanowires. The detailed principle of these methods is discussed in chapter 2.

1.4 Semiconductor nanowire applications

Although nanowire technology has emerged only in the 21st century, it has received extraordinary attention because of its huge potential applications in many areas.

Obviously, semiconductor nanowires, especially Si or Ge nanowire is one of the most promising candidates for CMOS technology. Si is still the main stream basic material for CMOS technology, the Si nanowire is much easier to be integrated into the current technology.

The first Si nanowire based MOSFET was successfully demonstrated in 2003 [34]. However, the nanowire has little response to gate control bias. A real working nanowire MOSFET was reported by the same research group in 2004 [35]. They used a back gate device structure and metal contact to form the nanowire device. Thereafter, this method is widely adopted by many research groups. Many other semiconductor nanowires and different device structures have been developed to improve the device

performance. This part will be discussed in chapter 3.

The single crystallized free-standing semiconductor nanowires are attractive building blocks for creating electrically driven lasers because their defect-free structures exhibit the superior electrical transport of high-quality planar inorganic devices and a single nanowire can function as a stand-alone optical cavity and gain medium. ZnO nanowire has been explored to be used as laser emitter [36]. Yang Peidong's group has observed lasing in gallium nitride (GaN) nanowires for the first time [37]. In optics, the feasibility of achieving electrically driven lasing from individual nanowires is investigated. Optical and electrical measurements made on single-crystal cadmium sulphide nanowires show that these structures can function as Fabry–Perot optical cavities with mode spacing inversely related to the nanowire length [38].

Nanowires also have many promising applications in the biological science. They are useful in the development of new devices to enable direct, sensitive, and rapid analysis of species. Devices based on nanowires are emerging as a powerful and general class of ultrasensitive, electrical sensors for the direct detection of biological and chemical species [39-43].

Thermoelectric materials generate electricity by extracting heat from a heat gradient. However, the relatively low efficiency limits thermoelectrics to niche applications in the last 30 years. Recently, many researchers predicted that the efficiency of thermoelectric energy conversion can be enhanced by nanostructure device [44, 45]. By varying the nanowire size and impurity doping levels, Si nanowire shows much better energy conversion efficiency [46, 47]. Other proper nanowire like SiGe [48, 49], Bismuth Telluride (Bi_2Te_3) [50, 51] Nanowires were also investigated as potential candidate for the booming thermoelectric devices.

For solar cell development, the key points are cost and efficiency. How to make a cheap photovoltaic module with high efficiency is always a priority for all solar researchers and engineers. Therefore, the low cost mass production of semiconductor nanowires is potentially a very competitive technique to replace current thin film deposition method. Very recently, many papers have been published about different methods of achieving nanowire based solar cells [52-57]. Si nanowire assembly has much high surface area compared with plane Si film. Therefore, the efficiency of SiNW based solar cell can be higher than Si thin film device. Furthermore, due to the huge aspect ratio of nanowire, the surface of nanowire solar cell is much bigger than normal plain thin film device. Therefore, the absorbance of the sun light for nanowire photovoltaic devices is enhanced.

1.5 Schottky Barrier MOSFET

The first reported SiNW MOSFET has different device structure from a conventional CMOS technology based device. One of the changes is the metal source and drain (S/D) contact replacement of highly doped poly-silicon S/D. This simple change of S/D material is another popular topic in the current CMOS front-end technology.

Based on the ITRS report, many requirements of basic transistors improvement have “no known solution” in some cases within the next two years. This challenge is forcing the industry and R&D department to consider alternative non-conventional CMOS architectures and integration of new and novel performance enhancing materials.

Since the metal S/D provides numerous performances, manufacturability and cost advantages compared to competing silicon CMOS architectures for the physical gate length technology nodes below 45 nm and make the technology scalable to the

sub-10nm regime. SB MOSFET directly solves or indirectly helps solve many of the critical challenges facing the semiconductor manufacturing industry, using a manufacturing process that remarkably requires fewer masks than conventional silicon CMOS. SB MOSFET further enables solutions for sub-threshold leakage control, mobility/transconductance improvement, RF device requirements, and soft error rate. Therefore, SB MOSFETs have attracted much interest as an alternative to conventional MOSFETs. This interest stems from the fact that very abrupt junctions and higher conductivity at S/D region can be formed by the metal semiconductor contact if we control the process properly.

Roadmap	Challenge Roadmap	2005	2007	2010	SBMOS
Technology Node [DRAM 1/2 Pitch (nm)]		80	65	45	
MPU Physical Gate Length (nm) [59]		32	25	18	Help
High K gate dielectric engineering	Front End				Help
Gate engineering (metal gates)	Front End				Help
Source-drain engineering	Front End				Solve
Channel doping	Front End				Help
Sub-threshold leakage current requirements (High performance and Low operating power)	Process Integration (PIDS)				Help
Mobility/Transconductance requirements and technologies (e.g. strained silicon)	PIDS				Help
MOS RF Device requirements	RF&AMS				Help
Soft error rates (FITs)	PIDS, design				Help

Table 1.1: Introduction of roadmap challenges addressed by SBMOS. Most of the categories have multiple line items in the detailed roadmap tables [58].

1.5.1 The Schottky Barrier

We initially provide a basic overview of metal semiconductor contacts. It is known that when metal is making contact with a semiconductor, one potential barrier, which is called “Schottky barrier”, is formed and rectifies the electrical transport

across the heterojunction. When the contacted semiconductor material is heavily doped, the schotkky barrier width is extremely small. This results in the This type of contact is called an "ohmic contact".

The question of how the Schottky barrier height (SBH) is determined can be simply introduced here. We can give a theoretical approach to approximate the SBH derivation in the ideal case. Figure 1.7 shows the electronic energy relations at an ideal contact between a metal and an n-type semiconductor in the absence of surface states. At the far left, the metal and semiconductor are not in contact and the system is not in thermal equilibrium. Metal and semiconductor have their own Fermi level energy (E_f). For metal, the difference between Fermi level and vacuum level is called *workfuntion*. The quantity is denoted by $q\Phi_m$, and equal to $q(\chi + Vn)$ (also represented by Φ_s)in the semiconductor, where $q\chi$ is the electron affinity measured from the bottom of the conduction band E_c to the vacuum level, and qV_n is the energy difference between E_c and the Fermi level. When the two materials contact, the Fermi levels in the two materials must be equal at thermal equilibrium. A negative charge is built up on the metal's surface. An equal and opposite charge (positive) must exist in the semiconductor. Because of the relatively low carrier concentration, this positive charge is distributed over a barrier region near the semiconductor surface. Hence the band of semiconductor is bended at the surface. The barrier height (Φ_{Bn}) is simply the difference between the metal work function and the electron affinity of the semiconductor. It can be given by:

$$q\Phi_{Bn} = q(\Phi_m - \chi) \quad (1\text{-}1)$$

Similarly, for an ideal contact between the metal and a p-type semiconductor, the barrier height $q\Phi_{Bp}$ is given by:

$$q\Phi_{Bp} = E_g - q(\Phi_m - \chi) \quad (1\text{-}2)$$

1.5.2 Current transport through the Schottky barrier

The major current transport in metal-semiconductor contact is due to majority carriers. There are two main types of transport processes. 1) Transport of electrons from the semiconductor over the potential barrier. 2) Quantum-mechanical tunneling of electrons through the barrier. Normally, the first transport process is the main part in the thermal equilibrium status. The classical theory to predict the carrier transport is thermionic emission theory.

Based on the assumptions that 1) the barrier height is much larger than kT, 2) thermal equilibrium is established on the plane that determines emission, and (3) the existence of a net current flow does not affect this equilibrium, so that one can

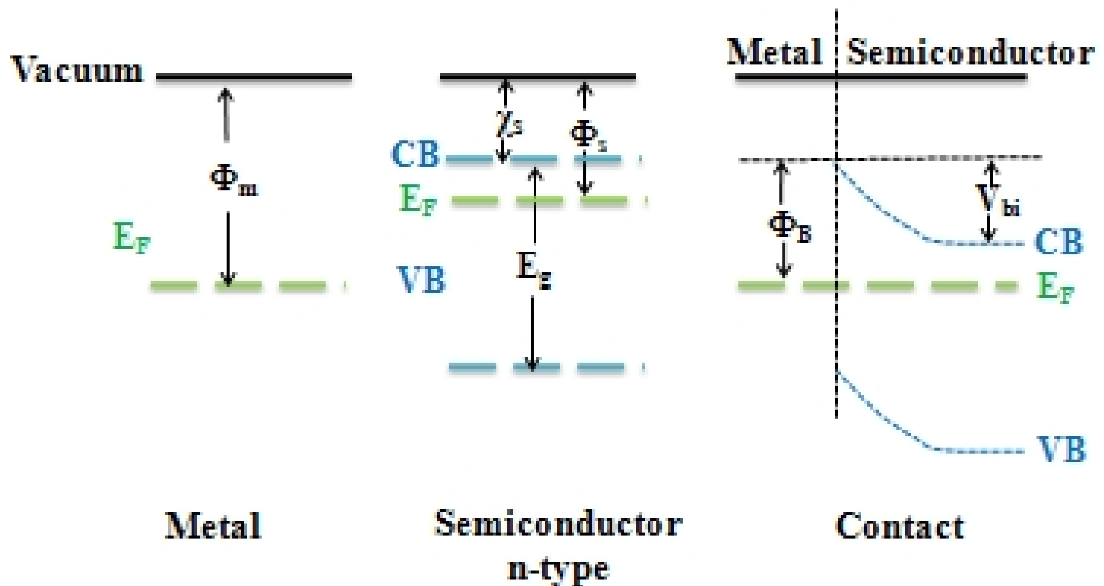

Figure 1.7: The Schottky barrier formation between metal and n type semiconductor when the two materials are connected [60].

superimpose two current fluxes, one from metal to semiconductor, and the other from semiconductor to metal. In this theory, the current flow is purely dependent on the

barrier height. Here, the equation for the current transport through the barrier height is given below:

$$J_n = A^*T^2 \exp\left(-\frac{q\Phi_{Bn}}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad (1\text{-}3)$$

$$and\ A^* = \frac{4\pi q m^* k^2}{h^3} \quad (1\text{-}4)$$

Where J_n is the current density of the net current flow through the barrier, T is the absolute temperature, V is the external bias, k is the Boltzmann constant, h is the Planck constant and m^* is the effective mass of carrier in different material. In section 4.4, more detail about the Schottky barrier of our device is discussed. For a heavily doped semiconductor or for operation at low temperatures, the tunneling current may become the dominant transport process.

The basic theory of Schottky contact is based on the bulk contact between metal and semiconductor. For the nanowire case, the Schottky barrier could be tuned by the 1D contact [61]. The tunneling part of current is not as low as expected even at room temperature. Therefore, therole that the Schottky contact plays at the S/D region in a nanowire MOSFET is a important consideration in this research.

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Chapter 2

Nanowire Synthesis and Properties

2.1. Introduction

As discussed the previous chapter, the bottom up grown semiconductor nanowire can provide an excellent single crystallized nanosized semiconductor building blocks at a very cheap cost. In order for this technology to be used commercially, a repeatable technique must be developed to produce the nanowire. Currently, there are many synthesis methods to achieve nanoscale materials including solid-liquid-solid (SLS) [1], super fluid-liquid-solid method [2], thermal evaporation [3], and nanomaterials growth in porous membranes [4]. However, these methods do not provide a well controlled and high-quality production method for the next generation of nanoelectronics applications. The goal of this research is to develop a general and repeatable method for preparing single crystal nanoscale materials, known as nanowires. One synthetic technique used to produce epitaxial aligned, single crystalline nanowires called the Vapor-Liquid-Solid (VLS) method which was originally developed by Wagner [5] and co-workers to produce micrometer-size whiskers in the 1960s and 70s. The VLS process has now become a widely used method for synthesizing 1D nanostructures from a rich variety of inorganic materials that include elemental semiconductors such as Si [6], Ge [7], and Boron [8], III-V

semiconductors [9-11], II-VI semiconductors [12, 13], and metals [14]. The VLS mechanism introduces a catalytic liquid alloy phase (like AuSi, AuGe, *etc.*) which can rapidly absorb a vapor to supersaturation levels, and from which crystal growth can subsequently occur from nucleated seeds at the liquid-solid interface. The size of the nanostructure is determined by the size of the alloy liquid.

In this chapter, detail of the VLS mechanism is discussed. In this research, we have successfully synthesized SiNW, GeNW, $Si_{1-x}Ge_x$ NW in chemical vapor deposition (CVD) equipment by using Au or Al as catalyst. Further study has been carried out to investigate the properties of grown nanowires. Scanning Electron Microscopic (SEM) pictures show that a huge amount of nanowires are observed after VLS growth. The high resolution Transmission Electron Microscopy (TEM) further indicates the single crystallization of the grown semiconductor nanowires. Surface detection tools such as X-ray photoelectron spectroscopy (XPS), and auger electron spectroscopy (AES), cannot find the Au concentration in the nanowire body. This leads us to predict that the semiconductor nanowire can be used in MOSFET integration. In addition, Al based Si nanowires are also demonstrated. In-situ doping process successfully achieved right after the nanowire growth. The surface detection tools successfully prove the dopants introduced in the nanowire although we cannot get the detail doping concentration in the nanowires.

2.2 Vapor liquid Solid mechanism

Before discussing nanowire synthesis, the basic synthesis principle should be delivered. As mentioned in Chapter1, Vapor-Liquid-Solid method is an interesting and promising methodology for us to get high quality nanowire. The basic idea of this methodology is using metal catalyst to “grow” nanowire from the substrate.

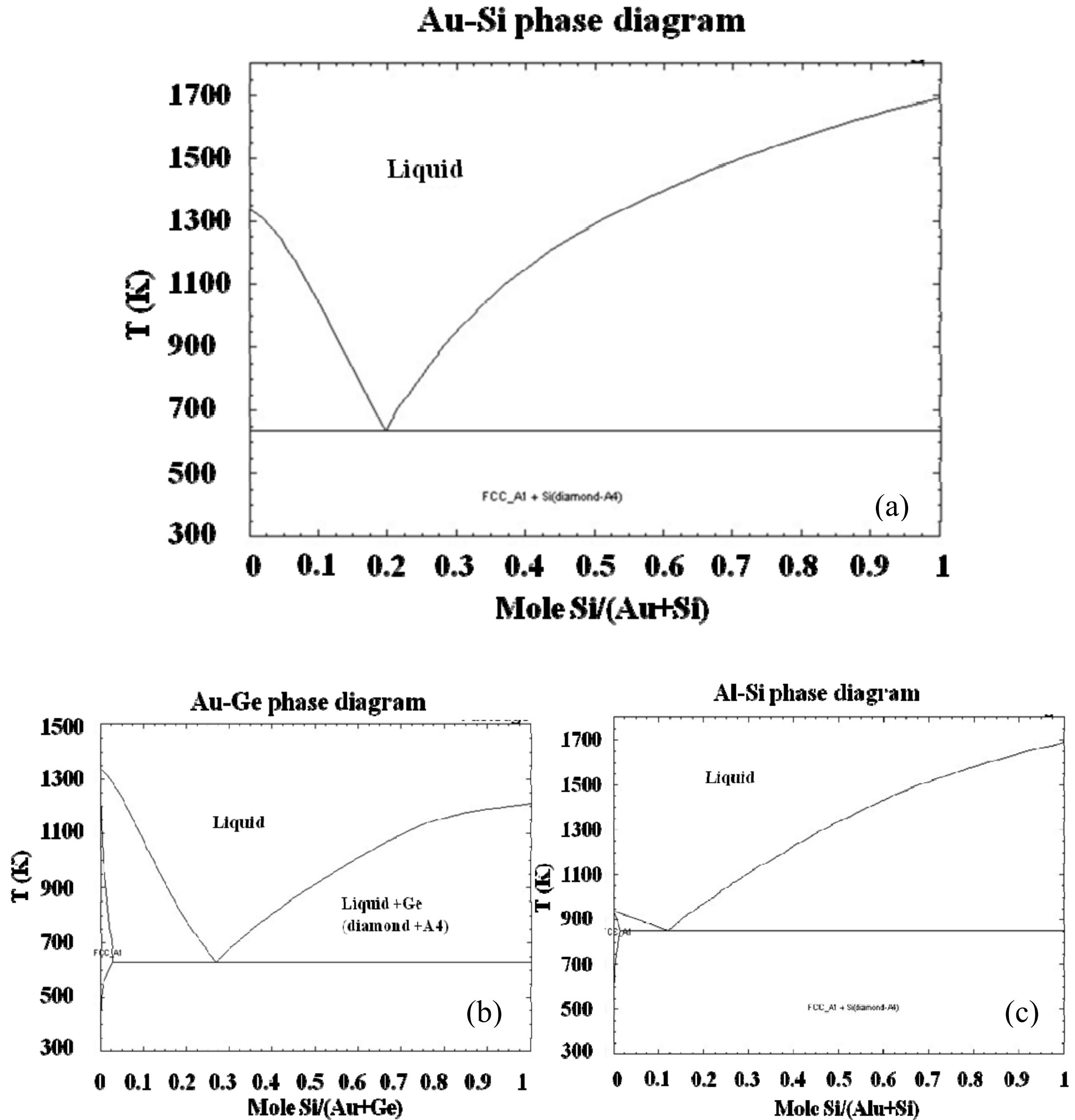
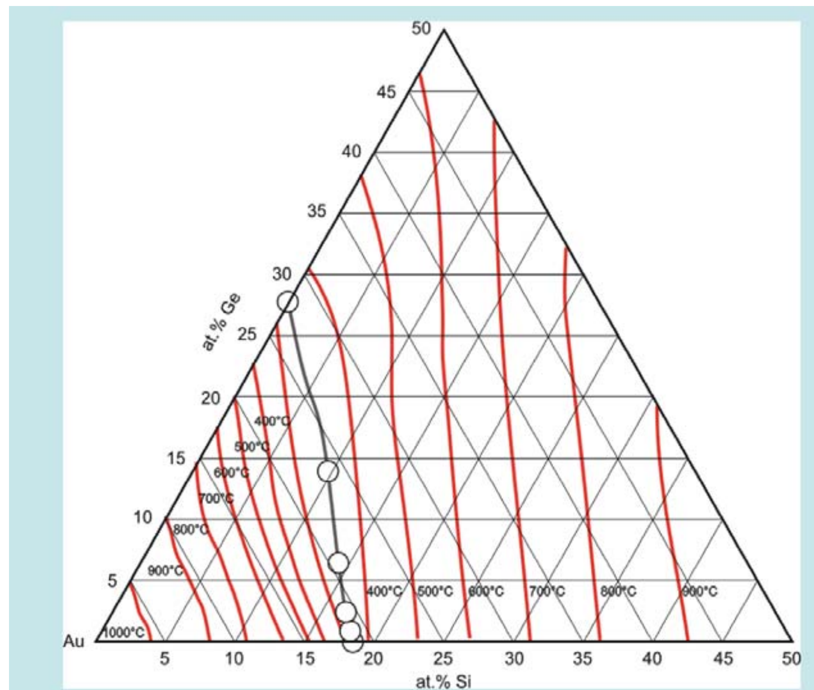


Figure 2. 1 (a) binary phase diagram of Au and Si. The eutectic temperature is 363°C. (b) Binary phase diagram of Au and Ge. The eutectic temperature is 356°C. (c) Binary phase diagram of Al and Si. (Source from **SGTE - SGTE Alloy Phase Diagrams)**

2.2.1 Phase Diagram

Based on the VLS approach, one of the challenges is the selection of an appropriate a catalyst that will work with the solid material to be processed into 1D nanostructure. It has been estimated that the analysis of catalyst and growth conditions can be substantially simplified by considering the binary phase diagram

between the metal as a catalyst and elemental semiconductors (Si, Ge). The phase of the material is determined by temperature and the composition of the material. Therefore, a “phase diagram” (Figure 2.1) can be drawn to show conditions at which thermodynamically-distinct phases can occur at equilibrium. For a binary alloy material, phase diagram plots temperature variation against the relative concentrations of two substances in a binary material. For example, the binary phase diagram of Si with Au, as shown in Figure 2.1 (a) exhibits a large Si-rich region in which liquid Au-Si co-exists with solid Si. In the diagram, the pure Au or Si has a very high melting temperature. However, the alloy of the two elements’ melting temperature varies with the composition of the alloy. When the Au concentration is reduced, the melting point is also reduced to a critical point known as the eutectic temperature. After that, the melting point begins increasing with higher Si concentration in the alloy material. Finally, the melting point of pure silicon is reached. Clearly, this eutectic temperature is lower than both elements’ melting temperature. This information provides us the possibility to obtain single-crystalline pure Silicon based on the Au-Si alloy by adjusting the AuSi composition ratio and growth temperature. Based on Table 2.1, the eutectic temperature of AuSi or AuGe is the lowest in all the Si or Ge based binary alloys. Furthermore, Au is physically and chemically stable at high temperatures. This is the main reason why Au is used as the metal catalyst to grow Si or Ge nanowires although it is not suitable for current conventional silicon based process technology. The second candidate for a catalyst is Aluminum. It has a higher eutectic temperature with Si (577°C) when compared with the corresponding Au-Si alloy. But the obvious advantage of Al catalyst is that Al is compatible in the silicon processing technology and Al will not cause a deep level trap which degrades semiconductor device like Au, especially for MOSFETs.



Figrue 2.2: Ternary phase diagram of Au-Si-Ge. The lowest eutectic temperature is ~350°C [15]

For Au $Si_{1-x}Ge_x$ nanowires, the calculation of the eutectic temperature is much more complex than in the binary alloy case. Based on a ternary phase diagram shown in Figure 2.2, the eutectic point can be predicted at around 350°C, which is higher than the eutectic temperature of the binary phase diagram (Au-Si). To obtain SiGe nanowires with proper Si or Ge composition, the flow rate of Si and Ge gas sources need to be well controlled. Theoretically the growth temperature would be higher than mono Si nanowire.

2.2.2 VLS mechanism based Nanowire growth

Usually, a VLS process begins with the dissolution of gaseous reactants into a liquid of a catalyst metal, followed by nucleation and growth of single-crystalline rods

and then wires. The 1D growth is mainly induced with a metal alloy and the size remains essentially unchanged during the whole nanowire process. There should be a good solvent capable of a forming liquid alloy with the target material, such as Si or Ge. Ideally this solvent should be able to form eutectic compounds, such as aSi-Au or Ge-Au alloy.

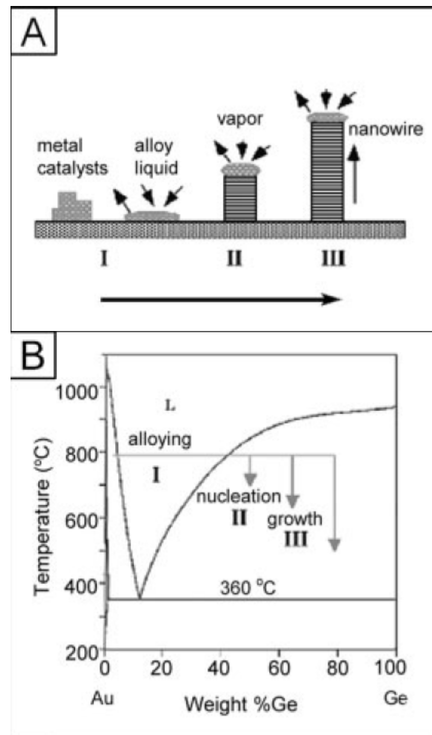


Figure 2.3 Schematics process steps for nanowire growth under VLS mechanism [16]

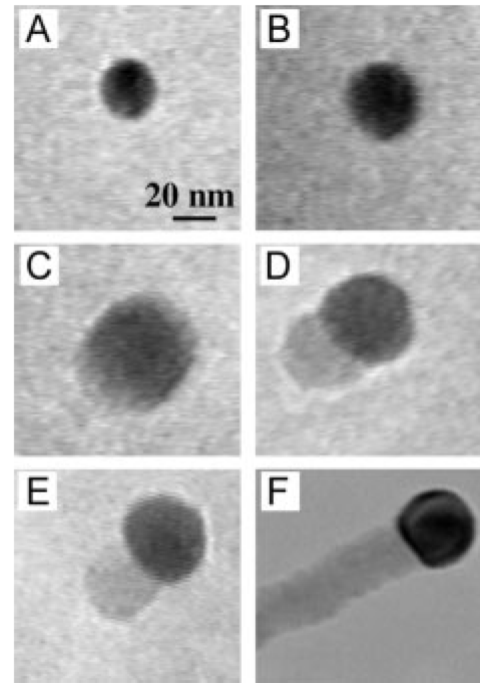


Figure 2.4: The birth of a semiconductor nanowire on a Au nanocluster, as observed using in-situ TEM. It is clearly seen that the Au nanocluster started to melt after the formation of GE-Au alloy, and this was followed by an increase in the liquid droplet size during the Ge vapor condensation process. [16]

To use Au-Si alloy as an example, all NW major growth steps of the VLS mechanism are shown in Figure 2.3 with the growth of Si nanowires. Au nano-catalysts are heated above the eutectic temperatures for the Au-Si system in the presence of a vapor-phase source of the semiconductor, e.g. silane (SiH_4). Adsorption

of the SiH_4 on the Au catalyst leads to the formation of a liquid Au-Si alloy. Continued adsorption of the semiconductor results in super saturation of the liquid alloy, leading to nucleation of solid Si, returning the system to near equilibrium in which the solid Si is formed. Continuous vapor delivery provides the driving force for diffusion of the Si from the liquid-catalyst particles surface to the growth interface. To achieve 1D vertical growth, vapor absorption should occur preferentially at the surface of the catalyst particle rather than on the surface of the Si nanowire. Therefore, the hydrogen-terminated nanowire surface is better to block the SiH_4 decomposition and deposition on the sidewall of nanowire. The important parameter is the partial pressure of the semiconductor elements (Si, Ge) that should be maintained sufficiently. So the hydrogen carrier gas H_2 is also quite important since it can adjust the partial pressure of SiH_4 in the chamber. Another interesting point is that nanowire diameter is dependent on the Au nanocluster size.

Figure 2.4 shows a set of TEM images sequentially recorded during the growth of a semiconductor nanowire. These images clearly show all the steps in the formation of the Au-Si alloy, the nucleation of Si nanocrystal in the droplet of Au-Si alloy, and the growth of a Si nanowire by pushing the liquid-solids interface forward. Based on the VLS mechanism, it is found that the diameter of each nanowire is largely determined by the size of the catalyst, and smaller catalysts can yield thinner nanowires. The semiconducting nanowires produced using the VLS approach are remarkable for the uniformity of their diameter, which is usually of the order of 10nm. Once the growth has been terminated, the presence of a catalyst nano-semiphere at the tip of nanowire is clear evidence supporting the VLS mechanism.

Catalyst	Eutectic Tempearture (°C)		Melting point (癈)	Catalyst	Eutectic Tempearture (°C)		Melting points (癈)	Catalyst	Eutectic Tempearture (°C)		Melting point (癈)
	Si (mol %)	Ge (mol %)			Si (mol %)	Ge (mol %)			Si (mol %)	Ge (mol %)	
Au	363(3.16)	361(12.5)	1064	Dy		860(72)	1412	Sm		820(73)	1072
In	156.6(<0.01)	156.3 (<0.01)	156	Er		877(71)	0	Sr	700(4.0)	714(3.0)	764
Li	180.5 (0.1)	180.5 (0.11)	180	Eu		723(48.9)	0	Tb		830(74)	1360
Ni	964 (29.0)	762 (71.2)	1,453	Fe	1207(58.2)	838(75.2)	1,535	Te	407(4.0)	375(9.1)	449
Pd	892 (23.0)	725 (54.8)	1,552	Gd		860(72)	1,311	Tm		870(70.9)	1545
Pt	979 (22.6)	770 (43.1)	1772	Ho		880(73)	1,470	U	985(1.1)	931(98)	1132
Sn	231.9 (<0.01)	231.1 (0.16)	231	K		63.7(0.1)	63	Y		820(85.7)	1532
Ti	865 (Ti3Si) 1330 (76.0)	900 (92.1)	1,660	La		730(6.7)	920	Yb		735(61)	824
Zn	419.3 (0.02)	394 (5.8)	419	Lu		860(75.3)	1,656	Hf	1330(62.9)		2150
Ag	835 (3.1)	651(17.5)	961	Mg	637 (1.34)	635(3.36)	650	Ru	1370(57.6)		2250
Al	577(12.6)	420(51.6)	660	Mn	1060(11.5)	720(64)	1,245	Ta	1414(94)		2996
As	797(4.0)	745(24.4)	817	Mo	1400(94.4)	935(99)	2,617	Th	1360(79)		1750
B	1270(99.6)		2,300	Na		765(66)	97	V	1400(95)		1890
Ba	630(3.0)	565(2.2)	725	Nb	1400(93.7)	950(99)	2,468	Tl		303.4(0.03)	303
Be	630 (3.0)		1279	P		577(12.0)	44	Zr	1370(73.5)		1852
Bi		271(0.01)	271	Pb		327(0.02)	327	Co	1259(62.1)	817(77)	1495
Ca	792 (4.0)	800(4.6)	839	Pr	1212(49.6)	795(6.6)	935	Nd		825(5.3)	1010
Cd		320(0.15)	320	S		120(2.0)	112				
Ce	650 (2.0)	670(6.0)	795	Sb	629(0.1)	592(9.2)	630				
Cr	1305(71)	895(89)	1857	Sc		892(90)	1,539				
Cs		465(19)	28	Se		212(7.4)	217				
Cu	802 (16)	644(39.6)	1083	Ge	938.3(<0.01)						

Table 2.1 Eutectic temperatures for binary alloy of various elements with Si and Ge [17].

2.3. **Experiment Equipment CVD**

To synthesize nanowires, first we need to customize one multi purpose Chemical-Vapor-Deposition (CVD) machine. The schematic picture of Figure 2.5 shows that the equipment has two chambers: loadlock chamber and main chamber which is separated each other by the gate valve. The two chambers have their own dry pump to vacuum independently. So the main chamber can always maintain at the process condition with high temperature and properly low vacuum level. The sample can be put on the 6-inch dummy wafer in the loadlock chamber first and vacuumed to a relative low pressure (8E-2 torr). Then sample is loaded into the main chamber's center stage with the 6-inch wafer by the robot arm. After the gate valve is closed, the center stage can be raised to the process height in the chamber by the motor. Therefore, different gas can be flowed into the chamber and the VLS nanowire growth can be begun.

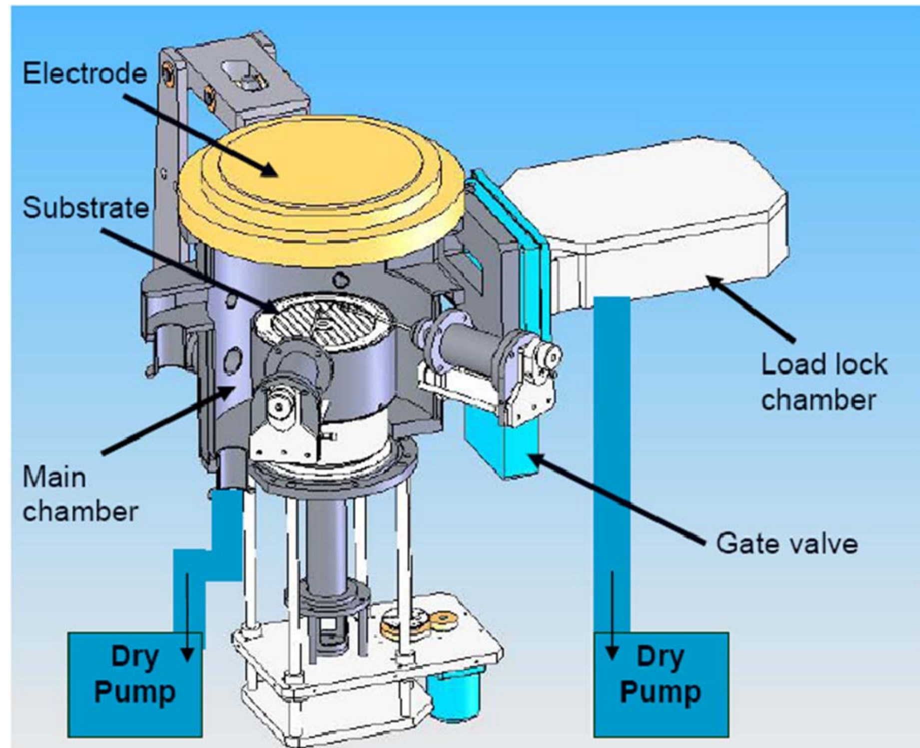


Figure 2.5: The schematic of single wafer loaded type CVD machine for growth of nanowire.

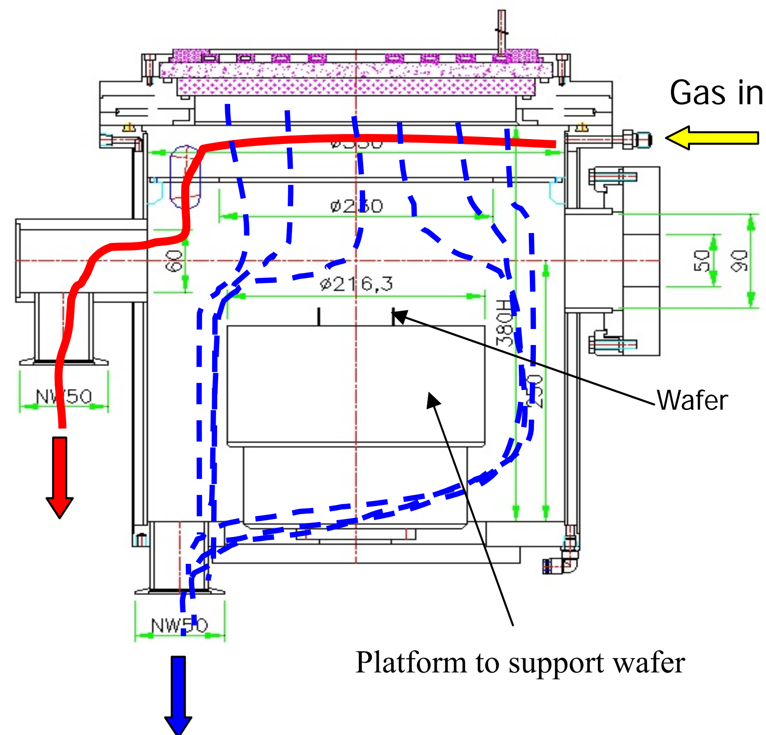


Figure 2.6: Schematic picture of gas flow in the main chamber. The gas flow direction has been indicated. Clearly, the gas can fully support the VLS growth at the platform.

In Figure 2.6, the gas flow direction clearly shows that different gases are combined in the main gas line first and then flowed into the main chamber from the right top side. At the bottom left side, the gas is pumped out of the chamber. In this case, gas can pass the sample surface and react fully with it. Furthermore, the CVD machine also has plasma generator which can provide RF power up to 1000 Watt with matching network. The top electrode is set under the cover of the main chamber, and the substrate is acted as the grounded point. This vertical plasma can help us do the plasma doping (B_2H_6 and PH_3) and cleaning (SF_6) work.

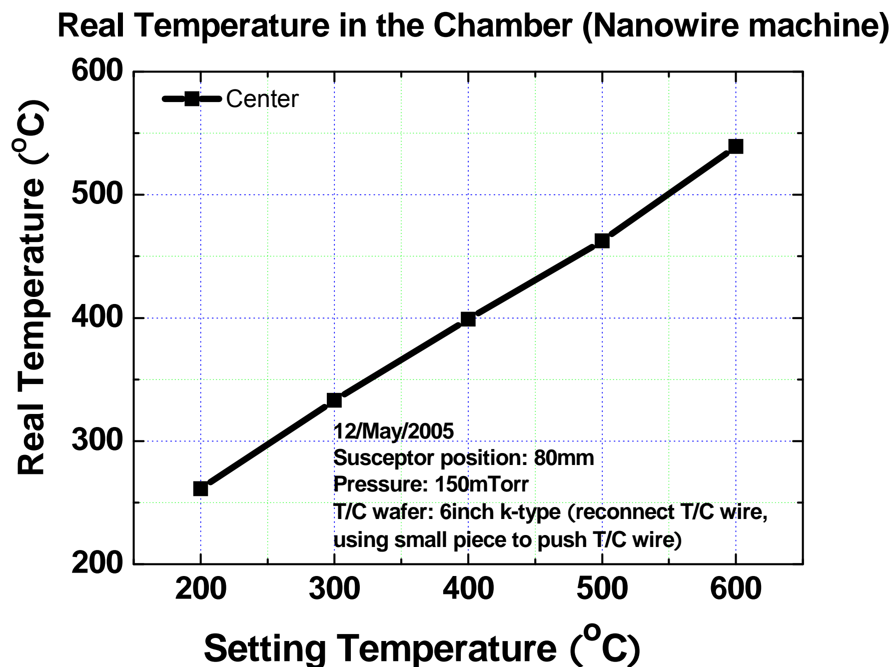


Figure 2.7: The real temperature at the centre platform in chamber versus the setting temperature. The real temperature in the main chamber is higher than the setting temperature in our recipe.

In this system, total eight kinds of gases can be flowed into chamber. SiH_4 (100%) and GeH_4 (10% in N_2) are for Si, $Si_{1-x}Ge_x$ and Ge nanowire growth, respectively. As dopant source, PH_3 (1% in N_2) and B_2H_6 (0.8% in N_2) are installed and SF_6 (100%) gas is used for plasma cleaning. The rest of them (Ar, N_2, and H_2) are

for inert gas that can act as carrier gas for nanowire process. The maximum achievable temperature is around 800°C and pressure is 1,000 torr.

The temperature in the main chamber is controlled by the thermal couple detector which is buried under the center stage. So actually it measures the temperature of the center platform rather than that of sample and we call it as setting temperature. However, the real temperature of the sample is a bit lower than the setting one. After our calibration, the difference between the setting temperature and real temperature has been indicated in Figure 2.7.

2.4 Silicon nanowire synthesis

After discussed VLS mechanism which is the basic principle of nanowire growth, hereby we utilize such method to synthesize silicon nanowire in our CVD machine. The detail process steps and discussion is delivered in this section and shown in Figure 2.8.

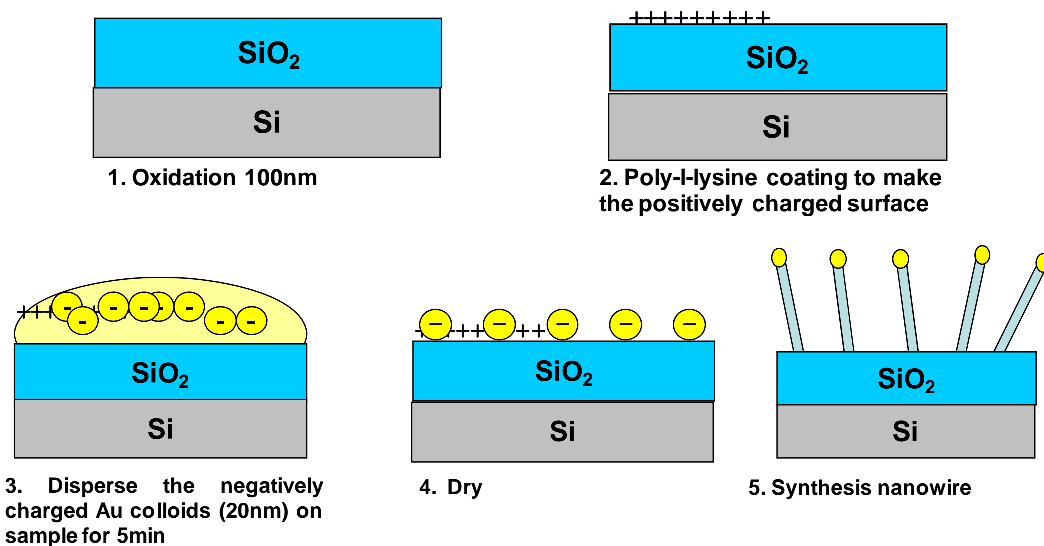


Figure 2.8: The detail process-flow of the sample preparation for nanowire growth. 1. We have p-type Si wafer with 400nm SiO_2 by thermal oxidation. 2. Positive charged poly-l-lysine is dispersed on the substrate. 3. Dispersion of negative charged Au nanocolloids on the substrate. The colloids are attached by poly-l-lysine. 4. The substrate is dried by nitrogen gas. 5. Nanowires are synthesized on this substrate.

Since nanowires can be grown on different substrates, here we use SiO_2 substrate as the basic substrate sample. The sample is cleaned in DHF (1%) for 1 min and rinsed in deionized water (DI water) to clean the surface. One kind of liquid chemical, 0.1% poly-l-lysine is spun coated on the sample to make positively charged surface on oxidized silicon wafers, and then Au colloids (20nm/10nm/5nm) are deposited on the sample. The negatively charged Au colloids stick to positively

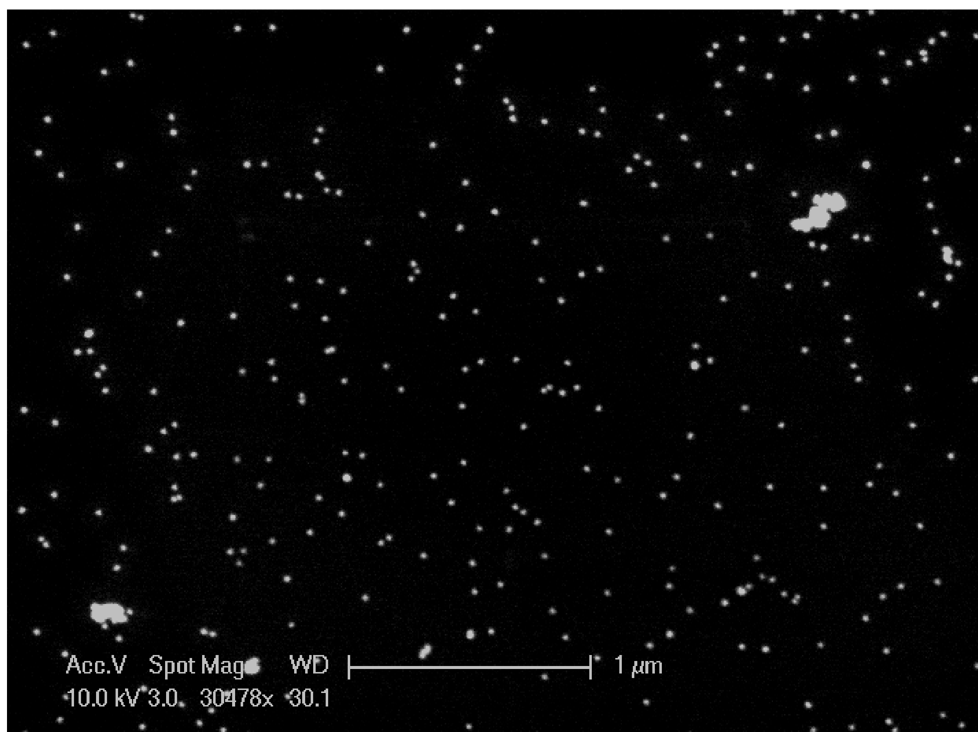


Figure 2.9: SEM picture of Au catalyst dispersion on the substrate by using Poly-l-lysine. The density of Au nanocolloids is large.

charged poly-l-lysine on the sample which is rinsed in Aceton and DI water after the Au coating. Figure 2.9 shows the SEM picture of Au nano-colloids dispersion on the substrate. Then the sample is transferred into the CVD load lock chamber which is pumped down to $5x10^{-2}$ torr, and the sample is loaded into the main chamber to start the nanowire synthesis process. First, chamber is pumped down to $2x10^{-2}$ torr and H_2

gas is flowed into chamber to make the pressure to 25 torr. Therefore, SiH_4 200 sccm is flowed into the main chamber with H_2 carrier gas 200sccm to make sure nanowire successfully grown. After 10 minutes, the nanowires can have more than 10um long. The diameter can be restricted to the size of Au colloids.

Aluminum catalyst based Si nanowire growth is a bit different from Au-SiNW growth. First, the Al catalyst preparation is different from Au catalyst attachment on substrate. We use electron beam evaporator to deposit 10nm Al seeding layer on Si or SiO_2 wafer. To avoid the oxidation of Al, the Al coated sample is transferred into the nanowire machine immediately, the exposure time is less than 1 min. The nanowire synthesis recipe keeps the same except the temperature is changed to 650°C due to the high eutectic temperature of Al and Si (~570°C).

The $Si_{1-x}Ge_x$ nanowire or Ge nanowire synthesis by using Au catalyst is similar as Si counterpart. Based on the trinary phase diagram of Au-Si-Ge, the process temperature of $Si_{1-x}Ge_x$ or Ge nanowire is lower as 440°C and 400°C. Other parameters of the recipe are the same as SiNW synthesis. The summary of the nanowires are summarized in the Table 2.2.

Nanowire types	Catalyst preparation	Gas Flow (sccm)	Processing temperature window (°C)	Diameter (nm)
AuSi	Poly-l-lysine + Au nano particles	SiH_4: 200 H_2: 200	440~550	10~20
AuGe	Poly-l-lysine + Au nano particles	GeH_4: 200 H_2:200	360~420	15
AuSiGe	Poly-l-lysine + Au nano particles	SiH_4:200 GeH_4: 20 H_2: 200	440~475	15~20
AlSi	Al (10nm) deposition by E Beam Evaporator	SiH_4: 200 H_2: 200	550~650	50~100

Table 2.2: Summary of different nanowires synthesis recipes

	Nanowire Type	Doping Type	Gas Flow (sccm)	Plasma Power	Process temperature and pressure	Doping Time	Activation Process
Thermal Doping	SiNW	n type	PH_3: 500 H_2:1000	/	550°C/ 2 torr	1min	650° C 30min
	SiNW	p type	B_2H_6: 500 H_2:1000	/	550°C/ 2 torr	1min	650° C 30min
Plasma Doping	SiNW	n type	PH_3: 500 H_2:1000	300W	550°C/ 2 torr	1min	650° C 30min
	SiNW	p type	B_2H_6: 500 H_2:1000	300W	550°C/ 2 torr	1min	650° C 30min
	$Si_{1-x}Ge_x$ NW	n type	PH_3: 500 H_2:1000	300W	450°C/ 2 torr	1min	650° C 30min
	$Si_{1-x}Ge_x$ NW	p type	B_2H_6: 500 H_2:1000	300W	450°C/ 2 torr	1min	650° C 30min
Simultaneous Doping	SiNW	n type	SiH4: 200 PH_3: 10 H_2:2000	/	440°C/25torr	10min	650° C 30min
	$Si_{1-x}Ge_x$ NW	n type	SiH4: 200 GeH4: 20 PH_3: 10 H_2:2000	/	440°C/25torr	10min	650° C 30min

Table 2.3: Different nanowire doping process recipes by using thermal doping, plasma doping and simultaneous doping.

2.5 Nanowire Doping Process

In addition to synthesis of the nanowire, we can also dope the nanowire by using B_2H_6 (p-type) or PH_3 (n-type) dopant gas. The doping process can be carried out using one of several methods. In the first method, the dopant gas can be flowed immediately after the nanowire growth followed by higher temperature activation of the dopants. This in-situ doping process allows the dopants to terminate the grown nanowires at the surface. Thereafter, the dopants can diffuse into the nanowire core at the high temperature activation (600°C, 30min). We called this method the “thermal doping process”. We have made some modifications to this method. When the dopant is gas flowing, the RF power is switched on. Hence, the plasma is ignited between the top and bottom contact in the chamber. This plasma causes dopant gas to fully

decompose, making for a more efficient doping effect on the nanowire surface. This method is called the “plasma doping process”. The third method to dope nanowires is called the “simultaneous doping process”. During the nanowire growth, we introduce dopant gas together with the combination of SiH_4 (GeH_4) and H_2. This method can provide more uniformly doped nanowires. However, the introduction of the third gas source during the nanowire growth interferes with the VLS mechanism. This phenomenon is made far worse when the B_2H_6 is introduced, as this inhibits nanowire growth. The detail reasons for this are discussed in Whang’s report [18]. PH_3 can be flowed together with SiH4 only when the PH3 flow rate is much smaller than that of SiH4. Even in this case, the nanowire condition is changed. The standard doping process summary is listed in Table 2.3.

2.6 Properties of the fabricated nanowire

Many surface analysis tools are used to investigate the properties of different nanowires before they are integrated in the MOSFET integration. These study results help us to further understand the capability of such semiconductor nanowire application.

2.6.1 Unintentionally doped SiNW based on Au catalyst

Figure 2.10 (a) shows the top view of field-emission scanning electron microscopy (FESEM) image of the SiNWs from 20nm diameter Au nanocolloids. The nanowire density is comparable to the nanocolloids density, indicating that nanowire nucleation is dominated by these colloids. From the picture, the nanowires have relatively uniform diameter (20±5 nm). Usually, when Au catalyst is used, the preferential growth direction of nanowire is along <111> [19]. Even though some

other growth directions are observed, it is not main growth direction for the nanowire. It has been proposed that this specific growth direction occurs since the solid-liquid interface is a single <111> plane, which is the kinetically most stable during growth process. In Figure 2.10 (b), the hemisphere Au tips on the nanowires are clearly observed. In Figure 2.11, Transmission Electron Microscopy (TEM) shows a clear single crystallized structure and a nanowire diameter smaller than 20nm. The length of the Au based SiNWs can reach longer than 15um. Therefore, the average growth rate (1.5um/min) is much slower than other reports [20, 21]. From the Auger Electron Spectroscopy (AES) and X-ray Photoelectron Spectroscopy (XPS) data (Figure 2.12 (a) and (b)), the Au concentration in the nanowire stem is undetectable. The Au catalyst is left on the top of the nanowire, but during the later process, the tip is not used in the nanowire MOSFET channel and removed by Au etchant.

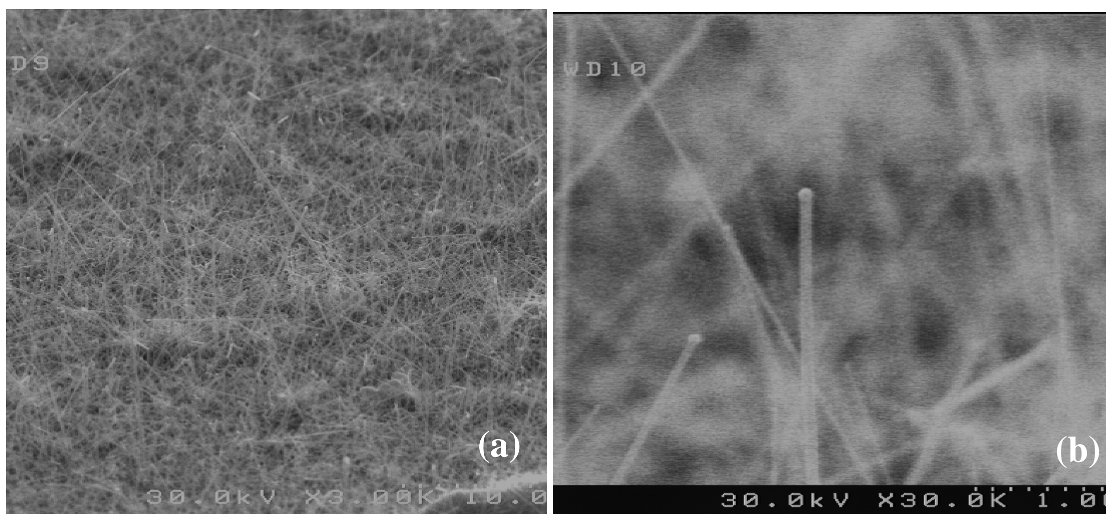


Figure 2.10: (a) SEM picture of grown undoped SiNWs on SiO_2 substrate. Numerous nanowires can be obtained. (b) SEM picture shows all the nanowires have semisphere Au tip on the top. The SiNWs have uniform diameter.

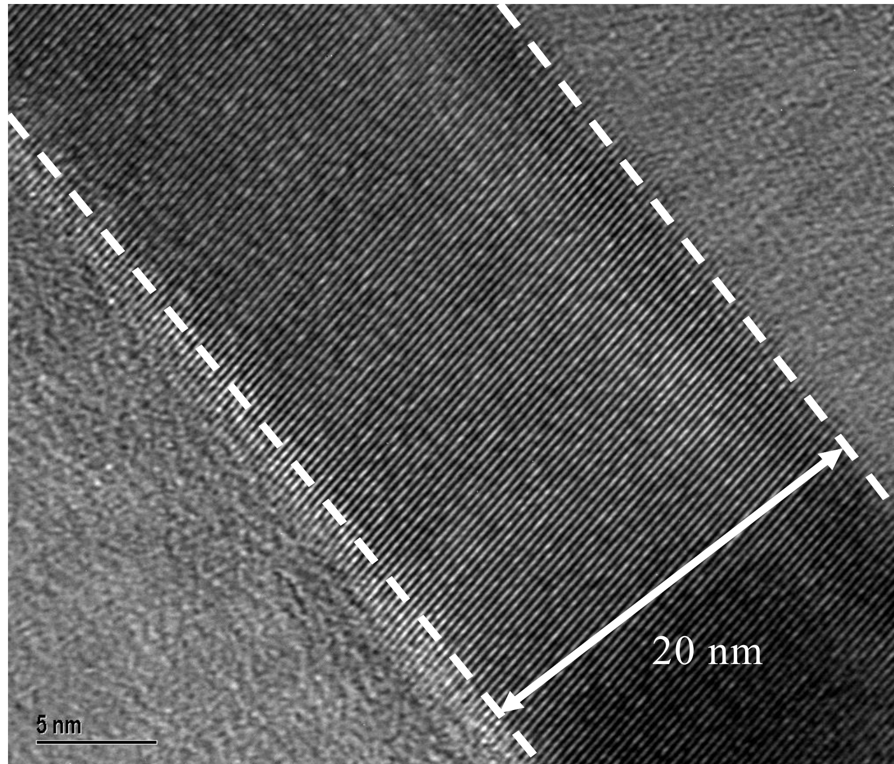


Figure 2.11: TEM picture of single crystalline SiNW grown on Au catalyst. The diameter is very consistent with the Au catalyst size.

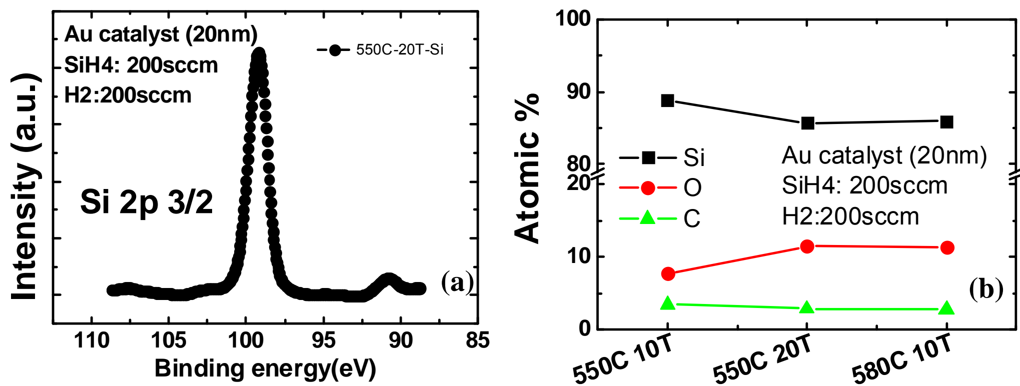


Figure 2.12: (a) XPS data of undoped SiNW grown on 20nm Au catalyst with SiH_4: 200sccm, H_2: 200sccm, at 550°C. The Si peak is clearly detected. (b)AES data of composition detection at the stem of undoped SiNW. The nanowires are grown at different temperatures. Si content is high. Oxygen, and carbon element is negligible.

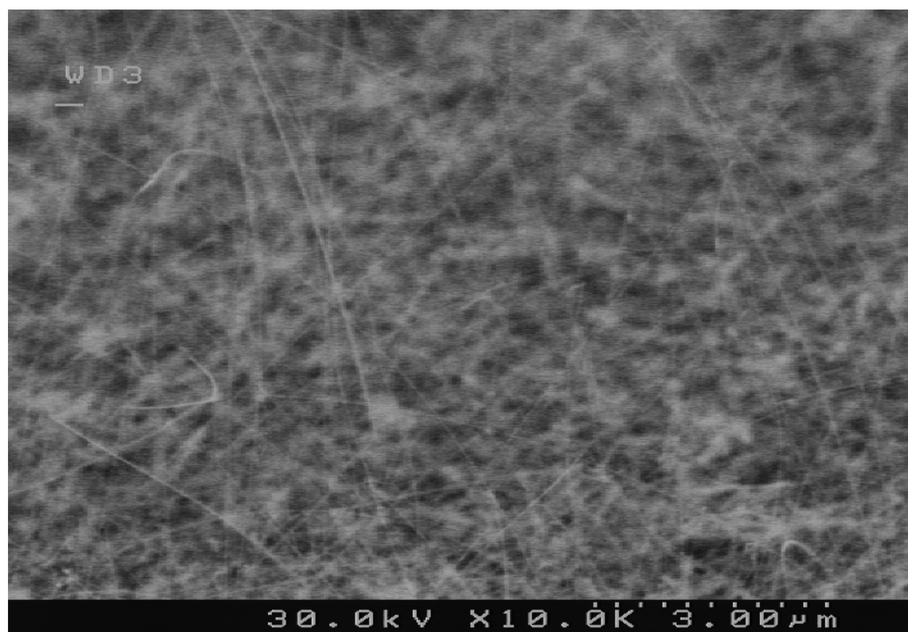


Figure 2.13: SEM picture of phosphorus doped SiNW by plasma doping process. The nanowire growth is not interrupted by the introduction of PH_3 or B_2H_6.

2.6.2 Doped SiNW based on Au catalyst

Since the plasma doping process is more effective, here we only investigate the nanowires grown using this doping process. From the SEM pictures (Figure 2.13), there is no much difference between doped nanowires and undoped ones. No extra shell is around the grown nanowires. XPS data shown in Figure 2.14 (a) and (b) indicate the successful doping is achieved for both Boron and Phos phorus. The dopant elements content is obviously higher than the undoped nanowires. Besides, the plasma doping process can introduce more dopants to nanowires than thermal doping process since the boron peak detected in plasma doped nanowires is more obvious in the XPS data. In Figure 2.15, the TEM picture shows the single crystallized structure of doped SiNW, which indicates that the plasma doping process does not damage the structure of nanowire. Besides, the Au tip has a very clear interface with nanowire stem (shown in Figure 2.15 (a)). This again delivers us a very important message that

Au is confined at the tip of the nanowire. The EDS data (table in the Figure 2.15) is collected at three positions of one nanowire (shown in the Figure 2.15 (b)). Due to the light element, boron concentration can be detected but the concentration value is not accurate in this surface analysis. The data can give us a rough profile of the dopants distribution in the nanowire. The results clearly indicate that the boron is detected in the nanowire. The doping concentration is higher at the surface and lower in the center of the nanowire. Once again, the Au confinement is confirmed.

Unfortunately, it is not possible for us to know the accurate doping concentration in the nanowire, because of its ultra small size. Currently, most surface detection tools are not able to detect the doping level of such small nanowire. Here, we use the planar bulk Si layer as reference sample to detect the doping process effect. We carry out the same doping process on the planar Si wafer, and use Secondary Ion Mass Spectrometry (SIMS) to detect the doping concentration. From Figure 2.16 (a) and (b), we can observe the detail concentration level of plasma doping process on the planar wafer. The doping concentration can reach to $1\times10^{22}/cm^{-2}$ at the surface and reduce quickly with depth of the substrate. Based on figure 2.16 (a), boron concentration can still be detected in the 80nm deep layer. However, phosphorus can only reach the same doping level at very shallow region. Obviously, light element like boron, diffuses much deeper. Therefore, in the nanowire, boron can diffuse much faster and should be more uniform in the nanowire, while phosphorus is easier gathering at the surface of the nanowire. These data can provide us very important information about the nanowire properties and help us to understand the device characteristics after later nanowire MOSFET integration process.

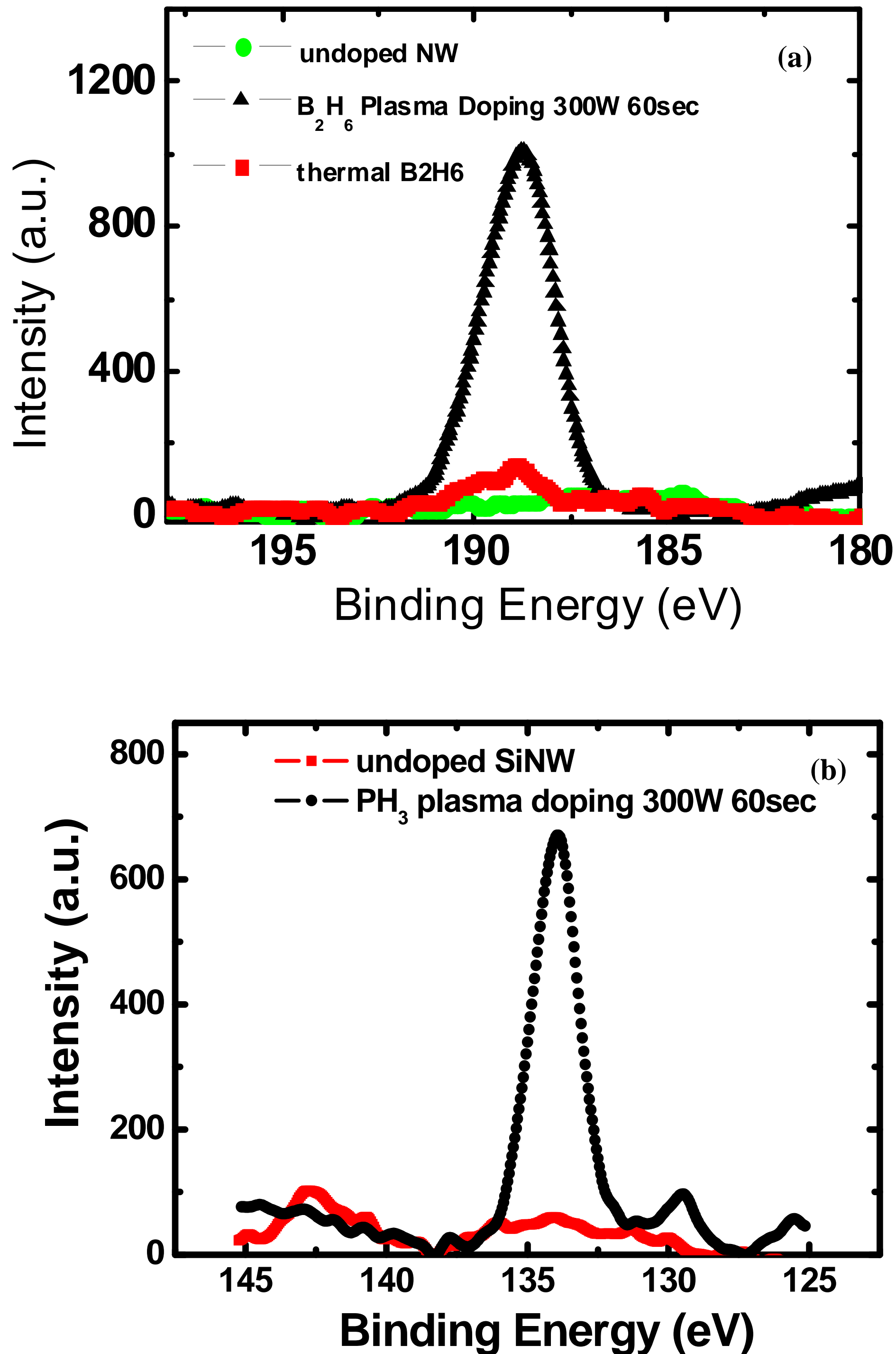
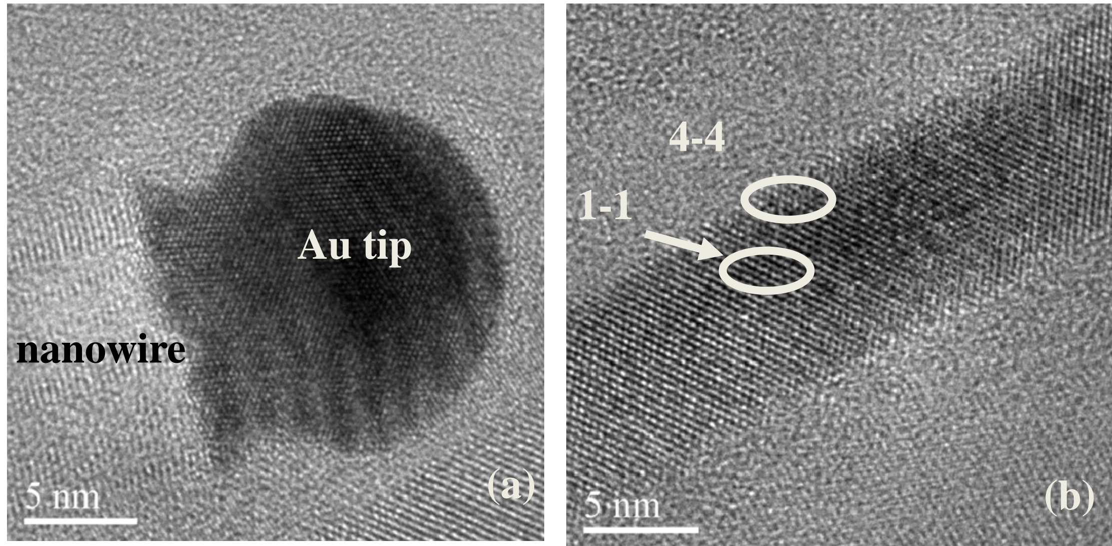


Figure 2.14: XPS data of boron and phosphorus doped Au SiNW. (a) Boron concentration is detected by XPS. Plasma doping process shows the highest boron peak, and thermal doping process also introduces boron into SiNW, but the concentration is much lower than plasma doping does. There is no Boron detected in undoped SiNW. (b) XPS data analysis of phosphorus detection in PH_3 plasma doped SiNW and undoped SiNW.



Si nanowire	tip	4-4	1-1
B (atomic %)	67.45	82.51	63.67
Au (atomic %)	15.19	0	0
Si (atomic %)	17.36	17.49	36.33

Figure 2.15: TEM picture and EDS data for doped nanowire. (a) TEM picture of doped nanowire with Au tip. (b)TEM picture of stem of doped Au SiNW. Area (4-4) is at the surface of nanowire. Area (1-1) is at the center of nanowire. Table: the EDS data of detected area on the nanowire. The boron concentration is high at the surface of nanowire. And again, no Au is detected in the nanowire stem.

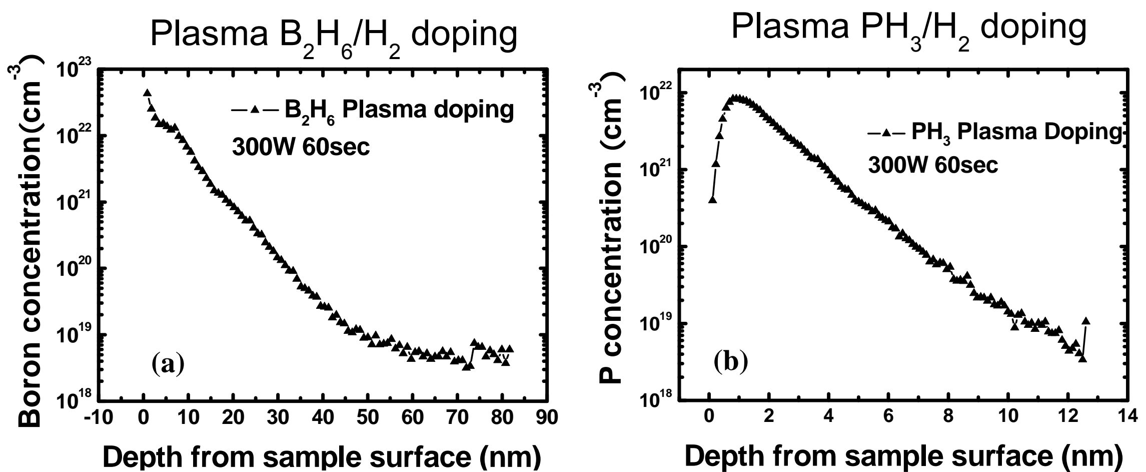


Figure 2.16: SIMS data to show the (a) Boron and b) Phosphorus concentration in the Si substrate by plasma doping process.

2.6.3 SiNW based on Al catalyst

The Al based Si (AlSi) nanowires are also successfully grown. The SEM picture shown in Figure 2.17 indicates the numerous nanowires obtained on the substrate. The Al tips are clearly observed on the top of grown nanowires. Some of the nanowires have kinks which is also reported elsewhere [22, 23]. AlSi nanowires are slightly different from Au based Si nanowires, although VLS mechanism is the same. Due to growth from the seeding layer rather than nano sized particles, the catalysts have different sizes at the very beginning of VLS growth. Therefore, the nanowire diameter is not uniform according to the VLS theory although most nanowires remain at smaller 100nm range.

The detail of single Al SiNW is investigated in TEM (shown in Figure 2.18 (a)). In Figure 2.18 (b), the higher magnified TEM picture shows the core Al SiNW is single crystallized. However, this core nanowire is surrounded by an amorphous layer which is believed as Si amorphous (α-Si) layer. This is due to the flowing gas SiH_4 decomposes rate is faster at high temperature (570°C) since the eutectic temperature

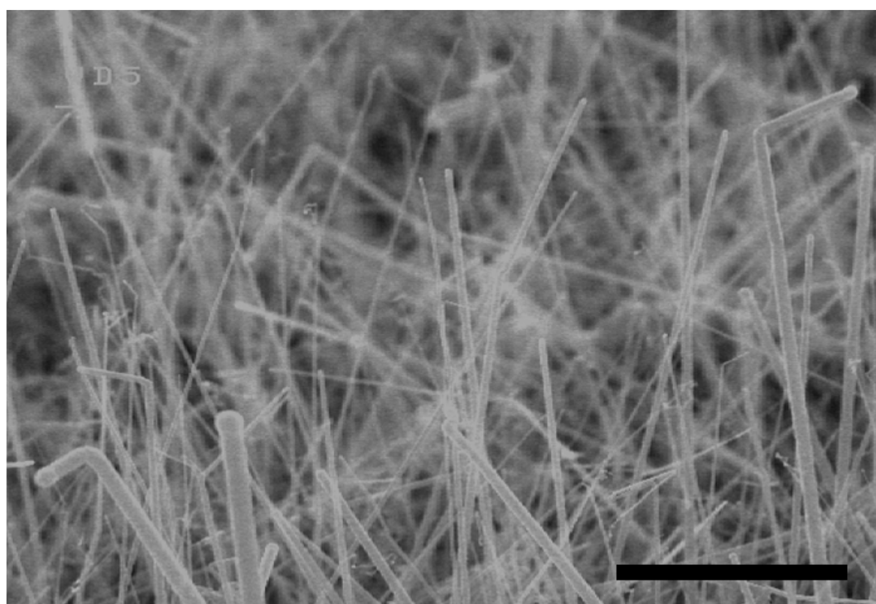
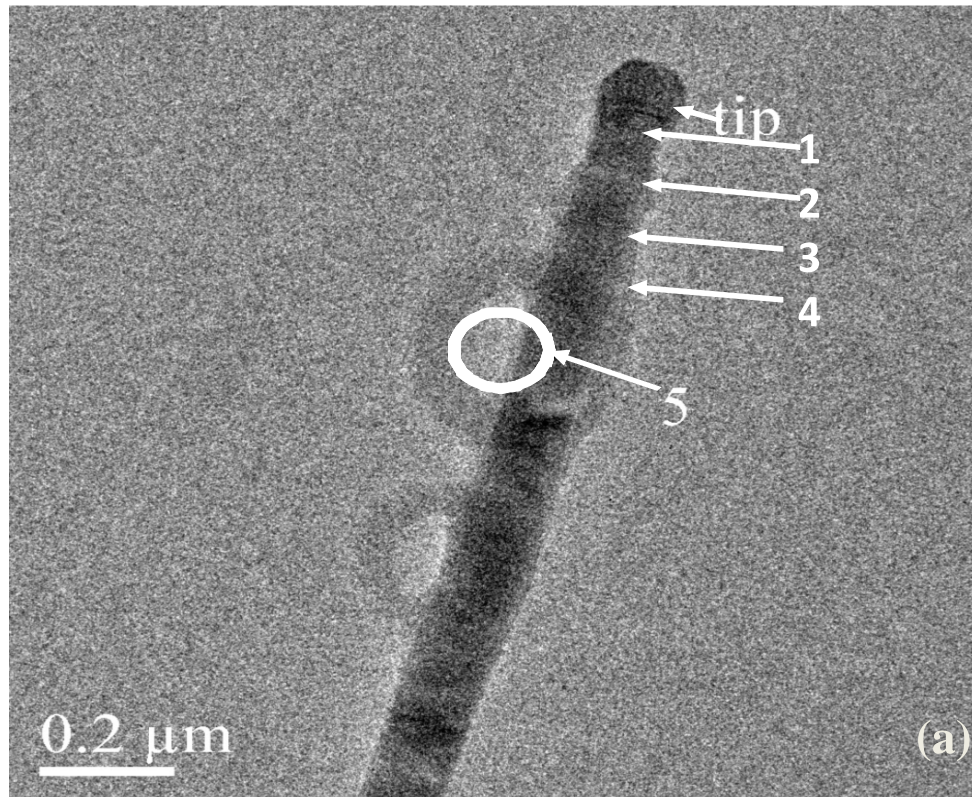
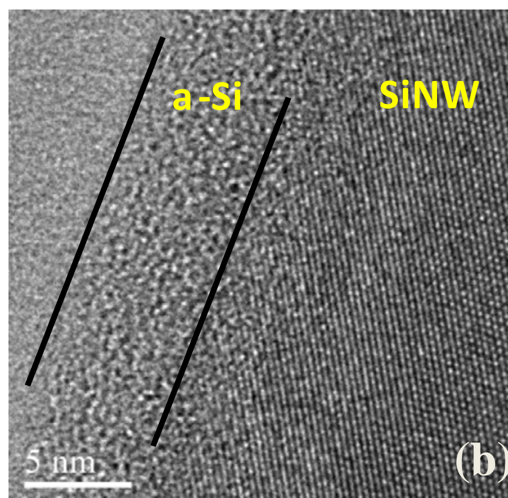


Figure 2.17: SEM picture of AlSi nanowires with huge density but with different diameters. Scale bar: 10µm.





	EDS (atomic %)	
Position	Al	Si
Tip (0nm)	98.93	1.07
1(50nm) interface	3.33	96.67
2(100nm)	2.19	97.81
3(150nm)	1.46	98.54
4(300nm)	1.27	98.73
5(500nm)	0.00	100.00

Figure 2.18: TEM picture and EDS data for undoped AlSi nanowire. (a)TEM picture of singlr AlSi nanowire. 5 positions on the tip, surface, and core of nanowire are detected by EDS. (b) TEM picture of AlSi nanowire. The amorphous layer is clearly indicated. Table: EDS data of atomic concentration of Si and Au in the different positions of AlSi nanowire.

of AlSi alloy is relatively high. This decomposition makes the α-Si layer deposition around the nanowire surface during the nanowire synthesis process. This explanation

can also be applied to other semiconductor nanowire growth. Therefore an Al based SiNWs have a thicker amorphous layer compared with Au based SiNWs. The EDS detection is detected at several positions on the nanowire from tip to the stem. The results (shown in the table of Figure 2.18) show that Al composition is only confined at the top of the nanowire. The farther from the tip, the less Al content is detected, which indicates the nanowire growth is totally based on the VLS mechanism. Furthermore, from the position 5, the surrounding layer is formed only by Si elements, which proves that the α-Si layer deposition is the main reason for the big nanowires. Therefore, the non-uniform diameter of Al based SiNWs could also attributed to the α-Si layer deposition.

2.7 Nanowire Surface Treatment

After the nanowire growth, the nanowires cannot be transferred to the next device integration process immediately. It is necessary to do the surface treatment to remove some parts of both Au SiNWs and Al SiNWs.

2.7.1 Au based Si nanowire

It is known that Au is the deep level recombination center in semiconductor materials [24]. Its existence in semiconductor bulk will cause the minority carrier life time to decrease rapidly, which is not acceptable for conventional MOSFET technology. The argument about whether Au element is in the nanowire is never end from the very beginning of this research. Although current technology cannot detect any Au in the stem of nanowires due to tools detection limit, we still try to remove the Au tips. Therefore, before the integration of Au-semiconductor nanowire MOSFETs, we use Aqua Regia (HNO_3+HCl, 1:3) or KI+I_2+DI Water (4:1:40) solution [25] to

remove the Au tips. After one hour dip in the solution, the Au tip can be removed and semiconductor nanowire is still remained (shown in Figure 2.19).

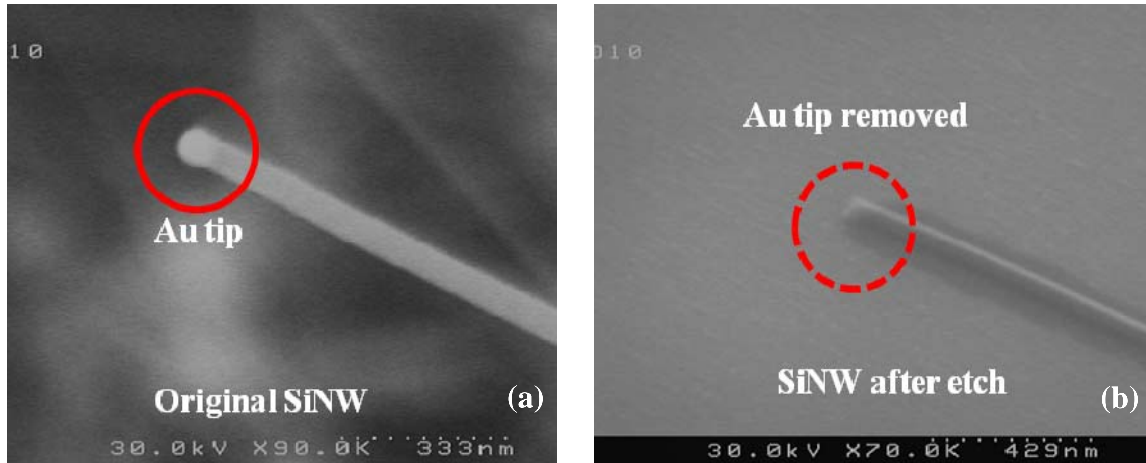


Figure 2.19: SEM picture of (a) original SiNW grown by Au catalyst before Aqua Regia etch; (b) SiNW after the 1 hour etch. The Au tip has been removed totally.

2.7.2 Al Si nanowires

For AlSi nanowires, the amorphous Si layer around the nanowire core is unavoidable during the ~600°C growth since SiH_4 is decomposed and deposited on the nanowire during the process. Higher temperature will cause thicker AlSi nanowires obtained. When the AlSi nanowire is integrated on the gate oxide layer, the vertical gate electrical field is applied on the amorphous layer of the nanowire, which degrades the device performance hugely. Therefore, after the nanowire growth, the first step is to remove the surrounding amorphous Si layer. We choose the solution combined by H_2O + HNO_3+CH_3COOH (70:29:1) which can remove amorphous SiNW pretty fast while single crystallized layer is less affected.

2.8 Summary

Based on Vapor-Liquid-Solid (VLS) mechanism, silicon nanowires (SiNWs) are successfully synthesized based on Au or Al catalyst in LPCVD system. SEM pictures show huge amount of nanowires grown in single time process. The length of nanowire reaches 10μm. The surface analysis equipments (EDX, XPS, and AES) do not detect the Au or Al concentration in nanowires. Successful doping process is also achieved right after nanowire synthesis, but doping concentration in the nanowire is difficult to detect. TEM pictures clearly indicate that both Au and Al based SiNWs have single crystallinze structure. For AuSiNW, the diameter is as thin as 20nm since it is controlled by the Au catalyst size. The Au tips on the SiNWs can be removed by wet etch after nanowire growth. On the other hand, Al catalyst based SiNWs have variable diameters due to amorphous Si layer surrounding nanowire core. This amorphous layer can be removed by the selective wet etch.

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Chapter 3

Nanowire MOSFET Fabrication and Characteristics

3.1 Introduction:

As we discussed in chapter 2, one of the most important applications of the semiconductor nanowire (NW) is MOSFET integration [1-4]. Compared with other candidates [5], semiconductor nanowires have several advantages: nano scale size, low cost production, semiconductor material properties, and compatible doping process.

However, how to integrate nanowires into MOSFETs fabrication is a quite challenging research topic. Yi Cui reported the very first successful undoped SiNW MOSFET in 2001 [6]. The device structure is showed in Figure 3.1. On the degenerate silicon bottom gate layer, very thick SiO_2 layer (600nm) is used as back gate dielectric. Nanowire is positioned on the SiO_2 layer and covered by metal S/D. This simple structure gives stable nanowire FET performance. This first device demonstration led to the development of many different nanowire FETs with greatly improved performance [7-12]. For example, Lieber's group reported Ge/Si core/shell nanowire channel based FET [13], which shows Coulomb blockade and quantum electrical transport properties. Some vertical nanowire transistors have been also

proposed and achieved [14]. The detail performance of nanowire devices referred here are summarized in Table 3.1.

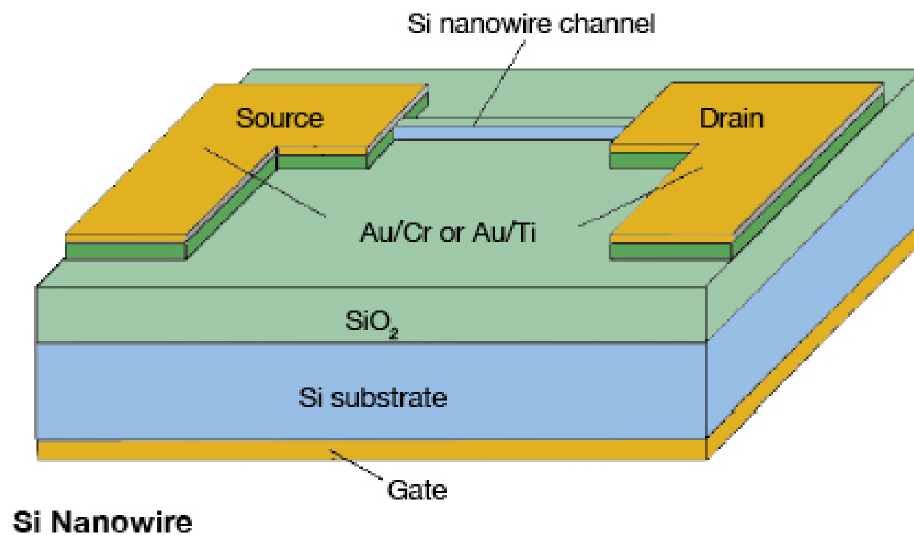

Figure 3.1: Schematic picture of back gate nanowire MOSFET device structure. The nanowire is connected by two metal terminals. The bottom SiO2 is used as gate dielectric to control the device operation [15].

Based on the previous reported device fabrication in section 2.4, we found the performance of nanowire FETs are much related to gate controllability and the metal S/D contact. In recent years, high-κ gate dielectric and metal S/D have become important candidates since they could be promising solutions for deep submicron MOSFET integration in the semiconductor industry. This indicates the needs to investigate the nanoelectronic device with the combination of semiconductor nanowire channel, high-κ gate dielectric and metal S/D. To compare device performance and analyze the device physics, different metal (Nickel, Pladium, Titanium) and high-κ materials (HfO_2, Al_2O_3) are tested with Schottky Barrier (SB) nanowire FET S/D and gate dielectric. Furthermore, to improve the Schottky contact, forming gas anneal effect on device performance was also investigated and metal

diffusion from S/D region to nanowire was observed. In addition, a short channel device can provide us other key information about nanowire practicable use in MOSFET technology. Hence, a high performance 65nm gate length SiNW FET was demonstrated by integrating undoped SiNW.

Reported Device	**[6]**	**[16]**	**[17]**	**[9]**	**[9]**	**Our device performance**
Device structure	**Back gate**	**Back gate**	**Back gate**	**Back gate**	**Top gate**	**Back gate**
Nanowire diameter	**Boron doped Si 5nm**	**Boron doped Ge-Si Shell 10nm**	**Boron Ge 5nm**	**Boron doped Ge 20nm**	**Boron doped Ge 20nm**	**Undoped Si 20nm**
Channel length	**Varied**	**2 µm**	**1 µm**	**5 µm**	**3 µm**	**1µm**
Gate Elect.	**Degenerate back gate**	**Degenerate back gate**	**Plastic sub**	/	**Ti 15nm**	**TaN**
Gate Oxid.	**SiO_2**	**ZrO_2**	**SiO_2**	**SiO_2**	**HfO_2**	**HfO_2**
t_{ox} (nm)	**600nm**	**60nm**	**10nm**	**10 nm**	**12 nm**	**20 nm**
Metal S/D	**Ti**	**Ti**	**Pd 80nm**	**Pd**	**Ti 30nm**	**Pd 80nm**
V_{DS}	**/**	**1 V**	**1V**	**1 V**	**1V**	**0.1/1V**
I_{ON}	**/**	**6 µA**	**600nA**	**3 uA**	**3uA**	**130nA/1.2 µA**
I_{ON} (µA/µm)	**50**	**360**	**120**	**/**	**/**	**/**
I_{ON}/I_{OFF}	**10^4**	**10^5**	**10^5**	**10^3**	**10^3**	**$10^5 \sim 10^6$**
S.S. (mV/dec)	**>174**	**240**	**340**	**300**	**750**	**120**
Gm (µS)	/	**3.3**	**0.34**	**0.21**	**0.19**	**0.11**

Table 3.1 Summary of device performance of previous reported back gate nanowire MOSFETs by other research groups

3.2 Experiment Details:

Based on the previous paper reported [6], we once used degenerate p-Si layer as back gate electrode, however, the dopants in Si layer is very easy to diffuse into upper gate dielectric layer and degrade the quality of gate dielectric. To avoid the problem, the degenerate wafer is replaced by p-Si substrate (~10^{15} cm^{-3}), then Ta (50nm) and TaN(100nm) layers are deposited on the p-Si substrate by magnetic sputter machine (shown in Figure 3.2 (a)). High-κ material (HfO_2 (20nm) or Al_2O_3 (20nm)) was deposited by ALD (Figure 3.2 (b)), and followed by post deposition anneal (PDA 500°C) [18]. The thickness of gate dielectric is varied (5nm ~ 20nm) and measured by ellipsometer. This gate oxide substrate is cleaned by using a procedure known as the TAM method (15 min sonication in trichloroethylene, followed by acetone and methanol) followed by dry blowing with nitrogen gas.

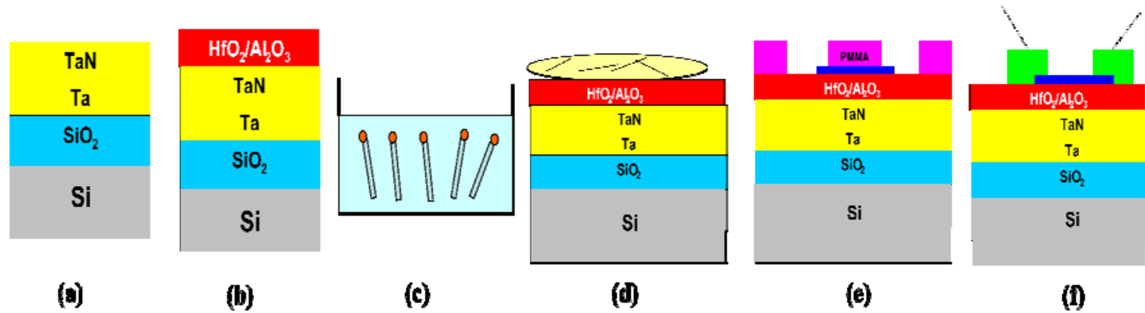

Figure 3.2: schematic process flow of Schottky barrier nanowire MOSFET fabrication. (a) Ta/TaN layer is sputtered on 400nm SiO_2 layer. (b) High-κ gate dielectric material (Al_2O_3 or HfO_2) is deposited on the TaN back gate. (c) Grown nanowires are suspended in IPA solution by ultrasonic vibration. (d) The nanowire contained IPA is dipped on the gate dielectric layer. (e) Source and Drain (S/D) patterns are defined by EBL system. (f) Metal S/D is deposited on the substrate followed by lift-off process. After gate opening, the device is measured in the probe station.

The grown Si nanowires (SiNWs) are first cleaned by DHF and SiGe nanowires are passivated by HCl [19]. To attach the nanowires on the ALD-grown

back gate dielectric layer, we put the nanowire sample in IPA liquid solution and rinse it by ultrasonication (60W, 1min). Therefore, nanowires are "cutted" and contained in the chemical solution (shown in Figure 3.2 (c)). The drawback of this attachment method is that many particles are generated during the sonic vibration and suspended in the liquid solution with nanowires. These small particles are also transferred to the gate dielectric layer with nanowires and they degrade the surface contact between nanowire and gate dielectric. This degradation will cause poor gate control on the nanowire channels which will affect the device performance a lot [20]. Another optional process to attach nanowires is just mechanical pressing the two substrates (gate dielectric sample and nanowire sample) and make nanowires fixed on the gate dielectric layer by van de waal's force. This force is strong enough to attach the 1-D materials on plain substrate. In the next process steps, nanowires do not move their positions on the substrate (Figure 3.2 (d)). In the pattern defining step, the sample is transferred in the Electron Beam Lithography system (Elionix ELS 7700). Nanowires are positioned under SEM browsing based on sample sharp corner. Then the substrate is spun with single layer polymethyl methacrylate liquid (PMMA 950: 300 nm) at 3000 rpm for 40 seconds and post bake on a hot plate at 180°C for 90 seconds. Consequently, the sample is loaded into EBL chamber again followed by litho patterning. After development in 1:3 mixture of methyl-isobutyl-ketone (MIBK): IPA for 40 seconds (Figure 3.2 (e)), metal was deposited on the pattern by electron beam evaporator (Leybold 450B) as metal Source/Drain contact. To fully cover the nanowire height and avoid failure of lift-off process, the thickness of metal Source/Drain should be higher than the nanowire diameter and thinner than the critical thickness of proper lift-off. The distance between Source and Drain electrodes is typically ~1um or even shorter. So different metal like Pd, Ni, Ti, Al *etc.* with 80

nm in thickness are used to investigate the electrical transport properties of such nanowire devices (Figure 3.2 (f)). Sometimes, the forming gas (200 sccm H_2 in 2000 sccm N_2) anneal is performed to improve the contact properties at S/D. Electrical transport measurements were made in room temperature by using a home-built system with < 1pA noise under computer control which is a combination of Micromanipulator probe station, VIBRAPLANE platform and HP 4156A semiconductor parameter analyzer. Figure 3.3 gives a formed structure of our nanowire MOSFET which consists of TaN metal gate electrode, High-κ gate dielectric (HfO_2) and metal S/D.

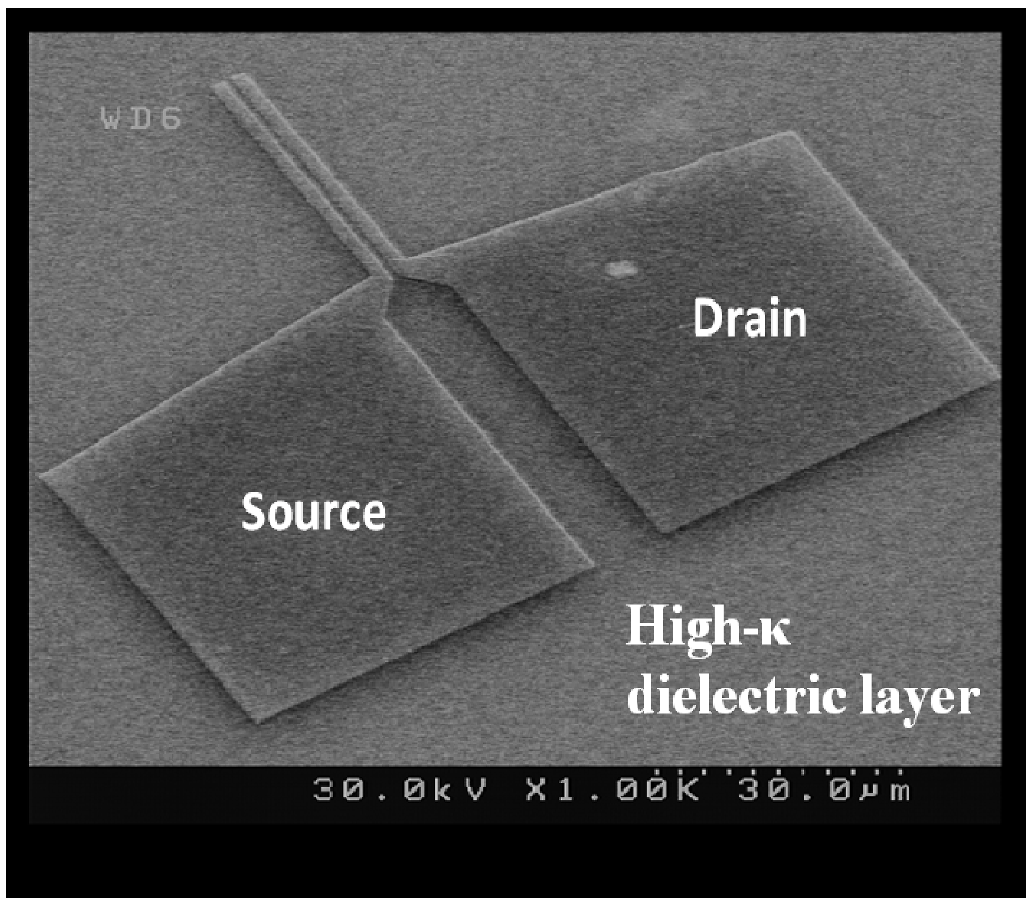

Figure 3.3: SEM picture of fabricated SB SiNW MOSFET (top view). The Source/Drain size is 50×50 µm for contact. The nanowire channel length is 1 µm.

3.3 Long Channel Device Characteristics and Analysis:

Since our undoped Au based SiNW synthesis is very repeatable, such SiNWs become the bench mark material for our device integration. Our first working nanowire MOSFET is also formed by undoped SiNW. At the beginning stage, working long channel device is the very first step for our project to achieve. Here, the device characteristics discussion is started from such long channel Schottky barrier undoped SiNW MOSFET.

3.3.1 Undoped Silicon Nanowire MOSFETs

In this research project, undoped Si nanowire was the first kind of nanowire to be synthesized by the VLS mechanism. After process optimization, nanowire growth is repeatable and the properties of the produced nanowire are stable. As a result, research is first conducted on the application of the developed nanowire.

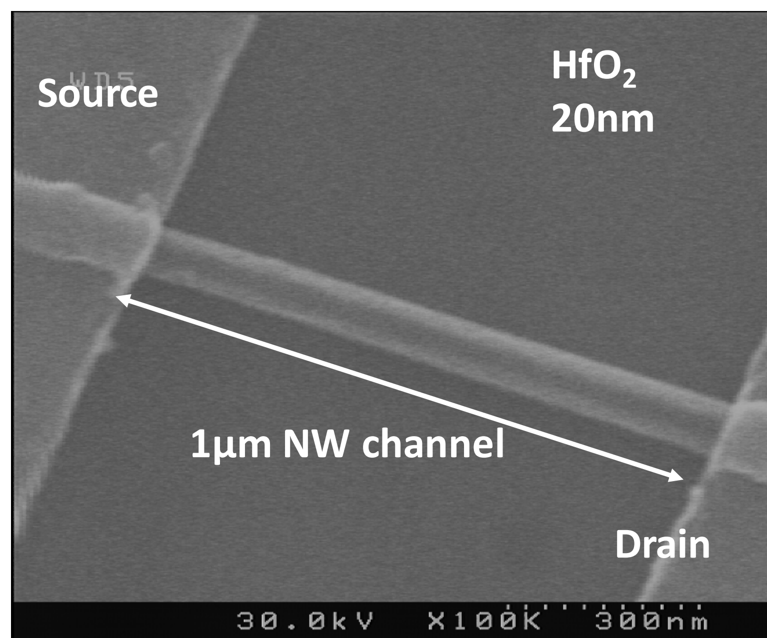

Figure 3.4: SEM picture of fabricated long channel undoped SiNW MOSFET (1um length). The nanowire is fixed on gate dielectric layer HfO2 (20nm). The two terminals of nanowire are covered by the Source/Drain material Pd (80nm).

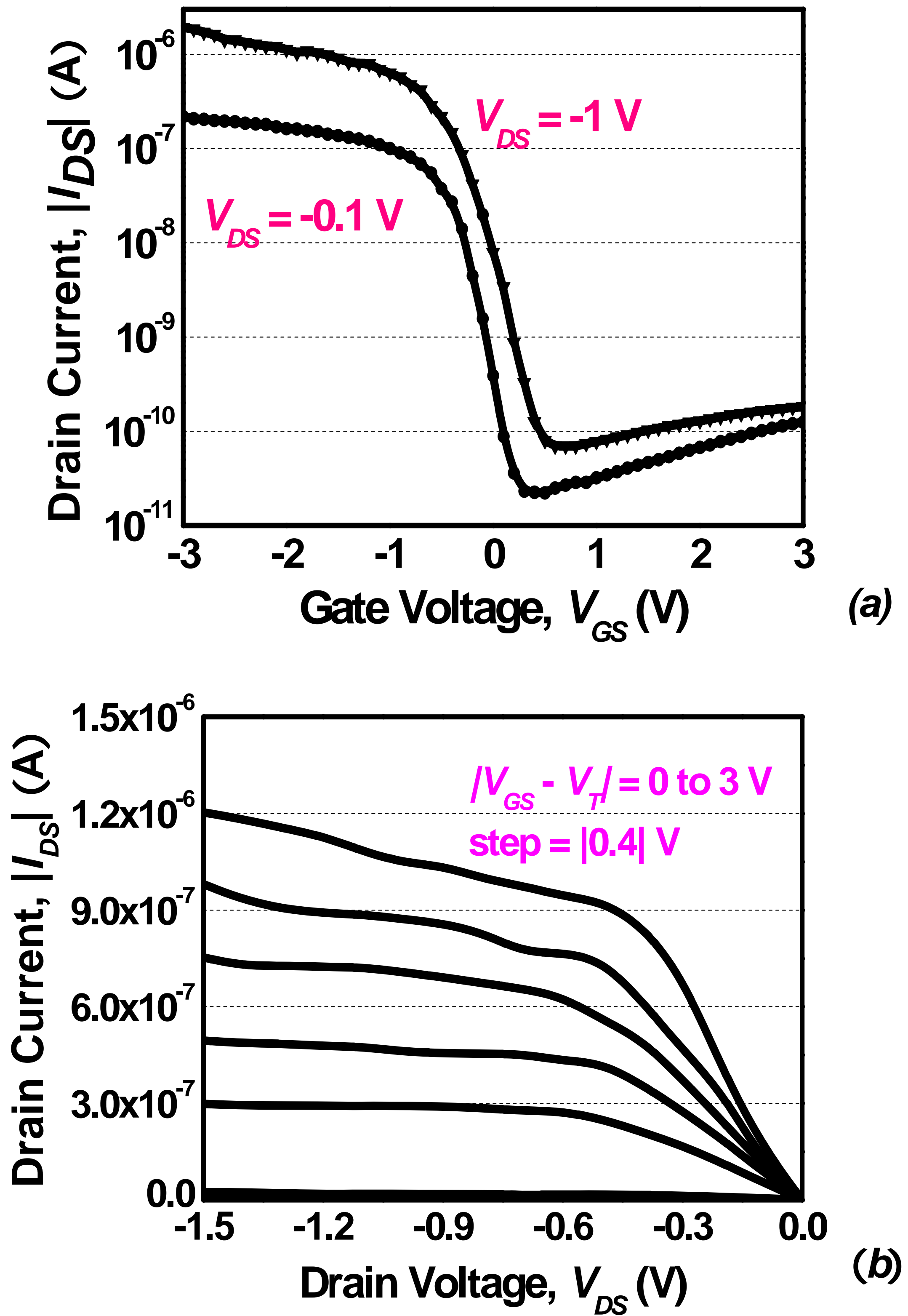

Figure 3.5: Device characteristics of 1um gate length SiNW MOSFET with Pd S/D

3.3.1.1 Pd S/D SiNW MOSFET device

Following the device fabrication process described in section 3.2, the SiNW MOSFET is demonstrated in Figure 3.4. Two terminals of one undoped Si nanowire are covered by Pd S/D (80 nm in thickness) on HfO_2 20nm layer and channel length is 1 μm. The typical transfer characteristic is shown in Figure 3.5 (a). The On state current I_{ON} is ~ 130 nA (~ 5 μA/μm, normalized by the crossection area of nanowire channel) when $|V_{DS}|$ is 0.1 V, while I_{OFF} keeps lower than 10^{-10} A. This translates to an I_{on}/I_{off} ratio of ~10^5. Transconductance (G_M) is 0.11 μS. The subthreshold swing of the device is S.S. ~ 120 mV/decade which is extracted from the range of 10^{-8}~10^{-10} A. Compared with previous data reported by other research groups listed in Table 3.1, this device has an even higher I_{ON}/I_{OFF} ratio and smaller S.S. The device output characteristic of the transistor is shown in Figure 3.5 (b). From the graph, a clear Schottky barrier's effect is observed. Unlike a conventional MOSFET, in the linear region the current increases very slowly due to the carrier blockade by Schottky barrier height.

3.3.1.2 Ni S/D SiNW MOSFET device

Before trying Pd S/D, we tried to integrate undoped SiNW with Ni S/D and Al_2O_3 dielectric layer for different device integration splits. Very small subthreshold swing (S.S.) is observed in this batch. Based on device physics theory [20], S.S is determined by

$$S.S. = \frac{d(Log_{10} I_{DS})}{d(V_{GS})} = \frac{kT}{q} In_{10}(1+\frac{C_d}{C_{ox}})$$

Where k is Boltzmann constant 1.38×10^{-23}, C_d is related to capacitance caused

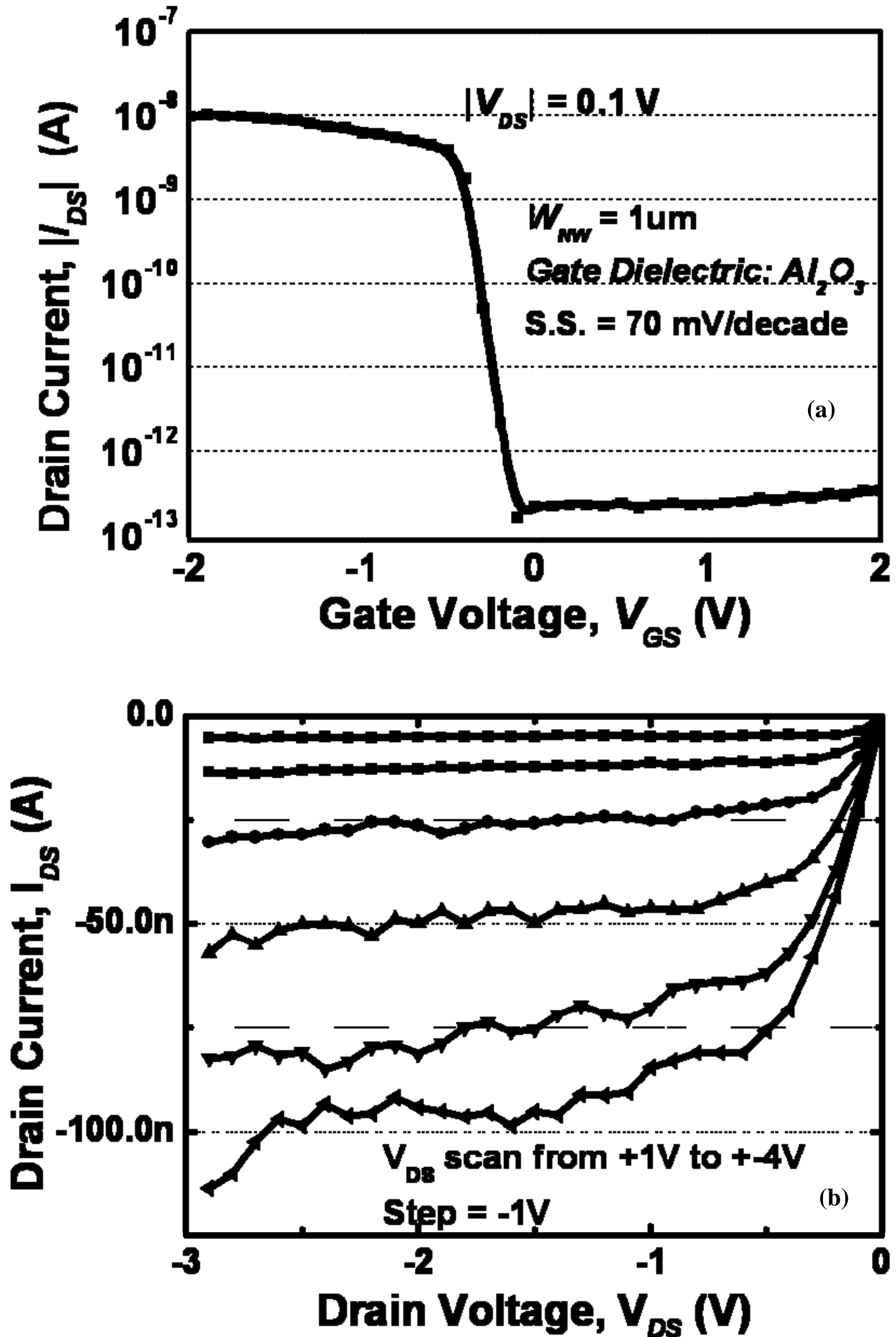

Figure 3.6: Device characteristics of 1um gate length SiNW MOSFET with Ni S/D (80 nm) and Al_2O_3 gate dielectric (20 nm). (a) I_{GS}-V_{GS} Transfer characteristics. Gate voltage sweep from +2 to -2V. (b) I_{DS}-V_{DS} output characteristics.

by depletion layer, C_{ox} is the total gate capacitance. In the ideal case, the best S.S. is ~60 mV/decade in room temperature. To approaching this value, gate oxide thickness (t_{ox}) and channel doping concentration need to be reduced. High-κ dielectric can reach thinner equivalent oxide thickness (EOT) and introduce more efficient electrostatic gating. Therefore, a back gate device formed by undoped SiNW (d = 20 nm) channel, Ni S/D and Al_2O_3 gate oxide (t_{ox} = 20 nm) has a better S.S performance because of the lower doping level and thinner equivalent oxide thickness (EOT). The transfer characteristic curve of the SiNW FET is shown in Figure 3.6, with a very low sub-threshold swing (70 mV/decade) extracted in the range of 10^{-9} ~10^{-12} A. To our knowledge, this value is the lowest S.S. ever reported. This result validates that undoped SiNW FET can yield high performance by selecting a proper metal S/D and gate oxide.

It is noted that I_{ON} was observed to be only 10 nA for this device, which is not a large on state current compared with that reported by other researchers. Considering the metal S/D barrier between Ni and Si and the lack of an annealing process to reduce the contact resistance after the device fabrication, this on state current is not unexpected. If this is the case, the MOSFET could be further improved by forming gas anneal.

3.3.2 Doped Nanowire MOSFETs

After setting up the process base line by using undoped SiNWs, both boron and phosphorus doped SiNWs were also put on dielectric substrate to form MOSFETs. All the devices are integrated with doped nanowires and SiO_2 50nm and 80nm thick Ni S/D. Figure 3. 7 (a) and (b) shows transfer characteristics and output performance of the phosphorus SiNW MOSFETs. Clearly the device shows an n-MOSFET

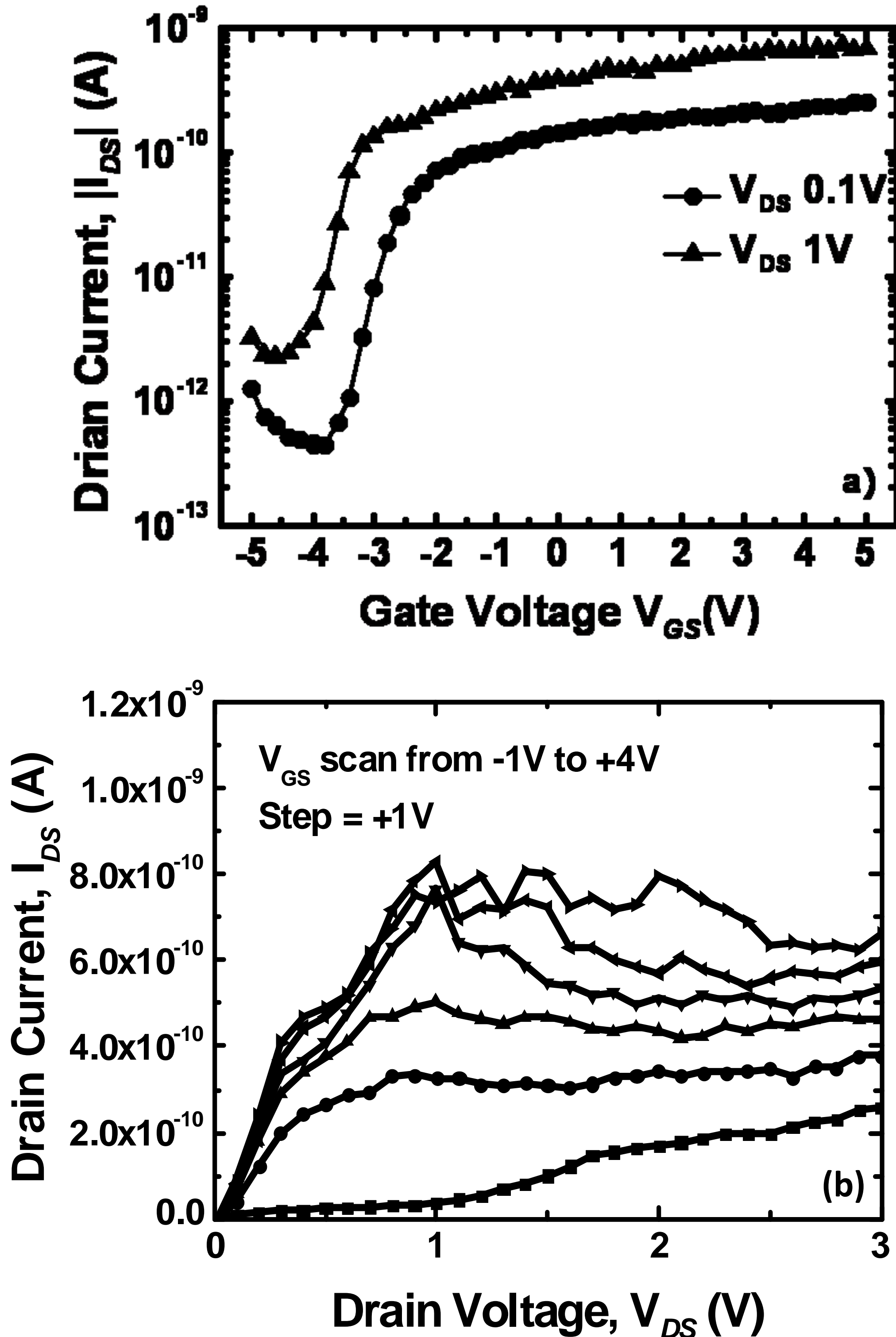

Figure 3.7: Device performance of phosphorus doped SiNW MOSFET with Ni S/D and SiO_2 50nm. (a) Id-Vg Transfer characteristics. Gate votalge sweeps from +5 to -5V. (b) Id-Vd output characteristics. Vgs starts from -1V, step +1V.

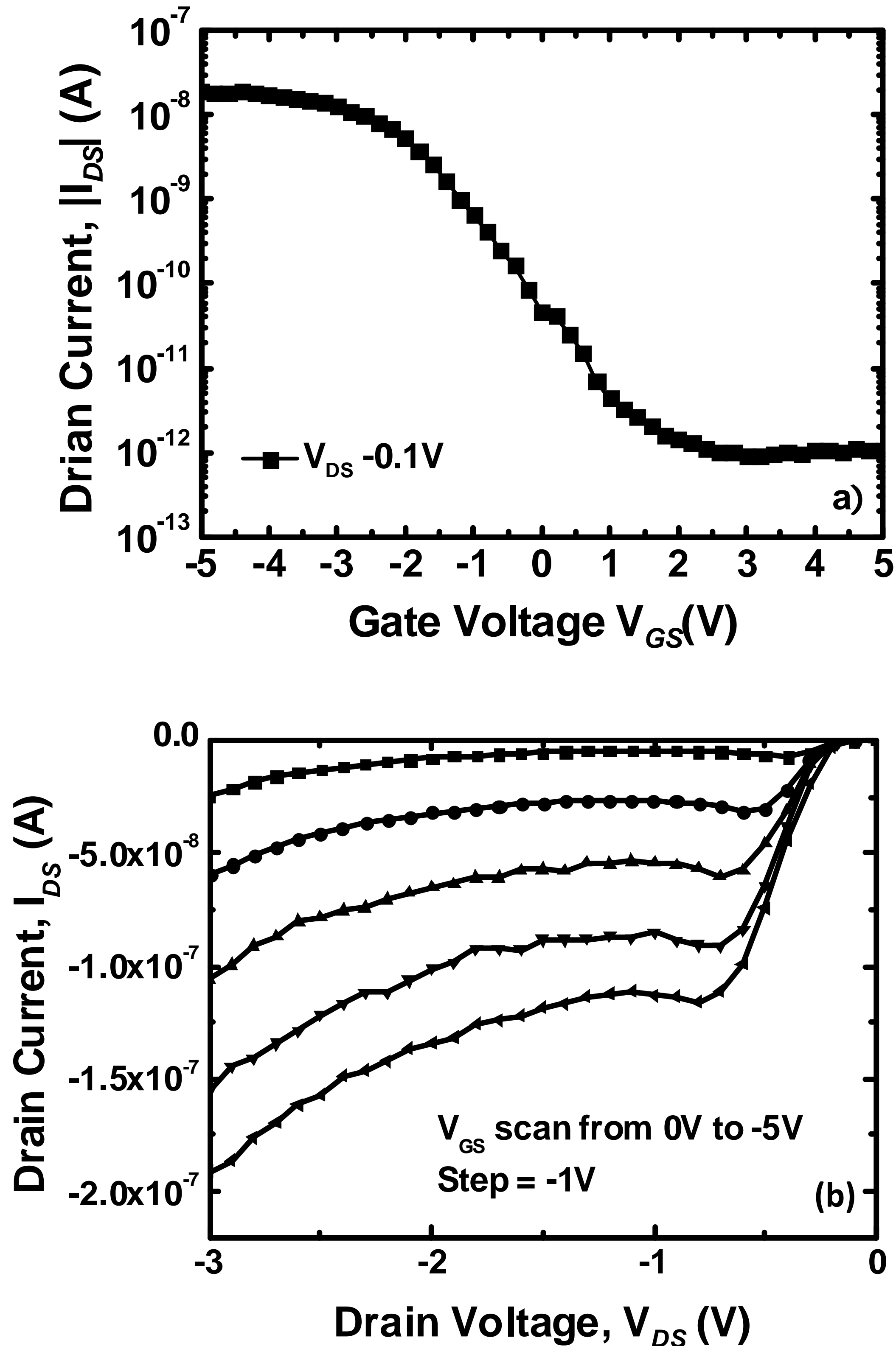

Figure 3.8: Device performance of boron doped SiNW MOSFET with Ni S/D and SiO_2 50nm. a) (a) I_{ds}-V_{gs} Transfer characteristics. Gate votalge sweeps from +5 to -5V. (b) I_d-V_d output characteristics. V_{DS} starts from -1V, step +1V.

performance. The I_{on} of the device is only 1×10^{-10}A (V_{DS}= -0.1V), this current value is extremely low compared with an undoped SiNW device. In figure 3.7 (b), when more positive V_{GS} and V_{DS} are applied, the drive current is still comparable with leakage current. Another interesting phenomenon is that the device is switches to the "On" state when the gate bias is negative. A detailed explanation of these device characteristics is given in the following section. In Figure 3.8 (a) and (b), the p-MOSFET performance is shown for boron doped SiNW MOSFET. The I_{ON} (1×10^{-8}A @ V_{DS}=0.1V) is comparable with undoped SiNW device and much higher than the phosphorus doped SiNW device. I_{off} is suppressed lower than 10^{-12}A, which delivers I_{on}/I_{off} ratio reaches to 10^4. The S.S. is 932mV/dec, this value is quite large compared with undoped SiNW transistor. A possible reason for this large value could be the thick gate dioxide caused by gate control and dopants introduced surface charges at the interface the between gate oxide and nanowire channel. For Schottky barrier transistors, the out performance is always limited at the smaller drain bias region due to the barrier blockade at small bias condition [21]., our device also indicates this phenomenon (shown in Figure 3.8 (b)).

From Figure 3.7 and 3.8, both doped nanowire MOSFETs show enhanced mode device performance rather than inversion mode for conventional plain device. This phenomenon is discussed in the next section.

For doped nanowires, the doping concentration contributes its dopant segregation effect to device operation. As we know, dopants will be redistributed in the device after anneal (>300 °C), and aggregated near the S/D contact. Based on previous reports [22, 23], the Schottky barrier width can be reduced when the many dopants ($>1*10^{26}$ m^{-3}) segregate at the S/D interface. But the dopants in the nanowire channel do increase the scattering and reduce the carrier mobility. So the high doping

of the nanowire could be one of the reasons why doped NW transistors have degraded performance.

3.3.3 Nanowire MOSFET Device Performance Analysis

Although working nanowire MOSFET demonstration is important, the further investigation of such devices is much more critical for us to know the detail device physics behind the performance comparison. Due to the back gate device structure, we find the SiNW MOSFETs perform different from conventional planar devices. Furthermore, Schottky contact at the source and drain region becomes one of the dominant factors in our device operation.

3.3.3.1 Device Structure

Before discussing the principles of the device’s operation, we should first consider the device structure, as shown in Figure 3.9. The back gate device structure is unlike the conventional planar MOSFET. The nanowire channel is located on the gate dielectric layer and sticked by Van Der Waals force. Theoretical speaking, the contact area between nanowire and gate dielectric is only a single line which means the gate dielectric effect on nanowire channel is limited. Furthermore, the channel width is quite small since nanowire diameter is only ~20nm. Also, the interface of gate dielectric and nanowire is another factor which affects the carrier transport. Secondly, as discussed before, metal source and drain sides have Schottky barriers. They not only increase the series resistance in the nanowire MOSFET, but also dominate the carrier injection through the metal-nanowire interface. So in our nanowire MOSFETs, the gate control is limited, while metal S/D Schottky barrier could be another dominant issue.

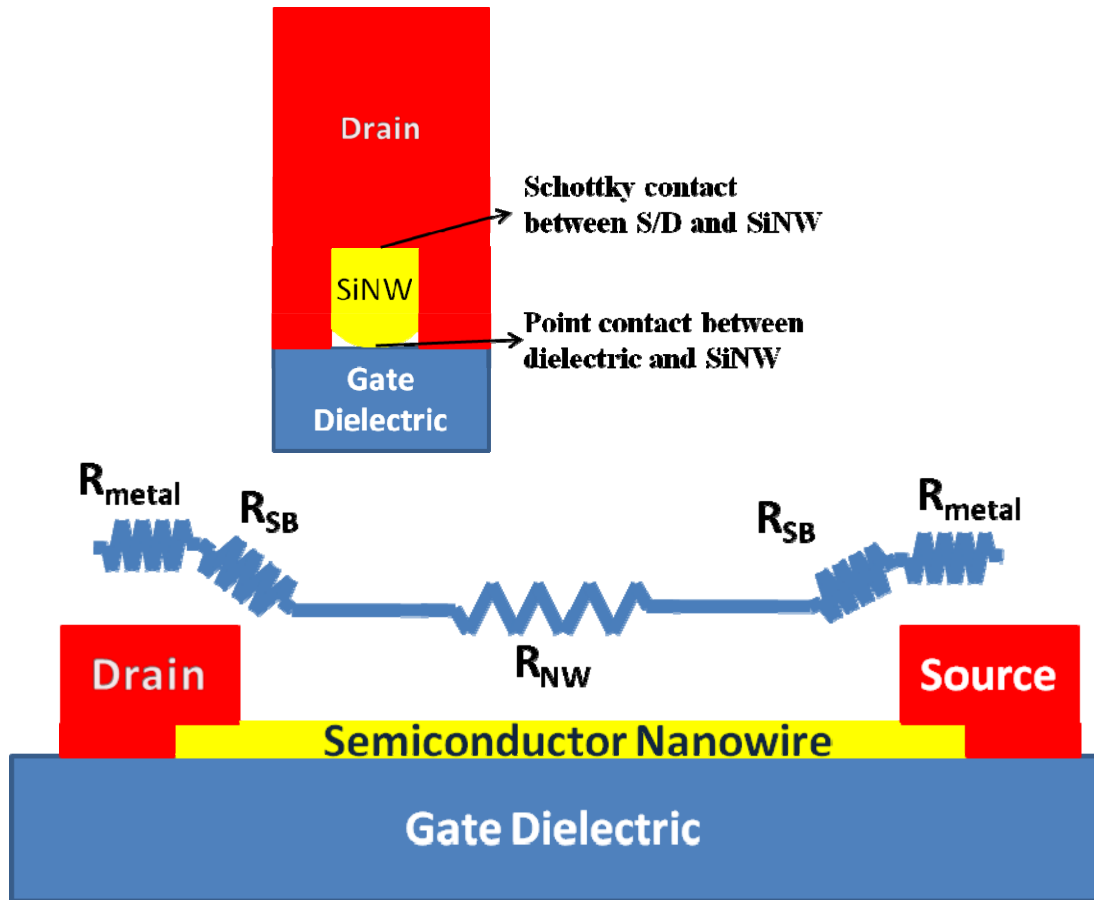

Figure 3.9: Schematic picture of nanowire MOSFET. a) the crossection view of S/D area of the device. The nanowire is covered by metal S/D and gate dielectric has point contact at the bottom. b) the resistance distributed in the nanowire device. The R_{SB} is the Schottky barrier resistance; R_{NW} is the resistance of nanowire; R_{metal} is the resistance of metal

3.3.3.2 Unipolar performance:

Based on previous reports [5, 24, 25], most SiNW or CNT FETs have two "ON" status which is called as "ambipolar performance" and makes them incompatible for practical application. A typical current–voltage curve of an ambipolar transistor is shown in Figure 3.10. Such a device conducts electrons when a positive bias is applied and holes when a negative bias is applied. This phenomenon was first discovered in CNT FET [26].Under certain biasing conditions, electrons and holes can be simultaneously injected from opposite ends of the CNT channel. This

performance is not acceptable in practical MOSFET technology which needs a unipolar switch for device operation.

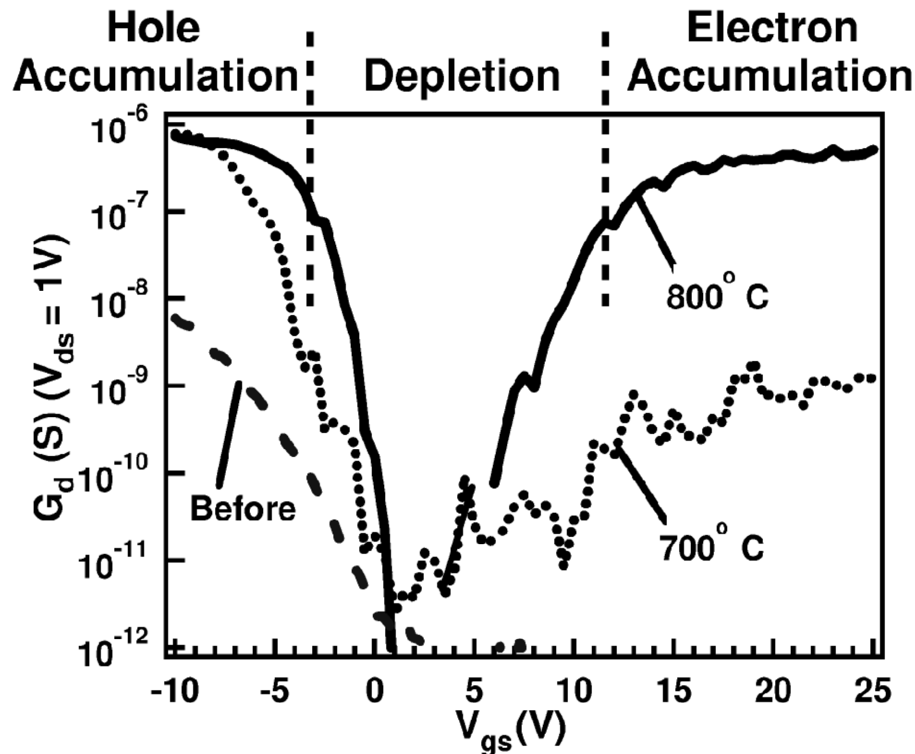

Figure 3.10: A typical ambipolar transfer characteristic of an 800 nm long CNFET at different processing stages. Source from [5]

However, in the undoped SiNW MOSFET there is no ambipolar characteristic. Instead, all the reported devices show enhancement mode unipolar performance, which means only the major carriers are transported in the nanowire channel. We believe this is due to the metal S/D barrier rather than the properties of the nanowire. As discussed in chapter 1, when metal makes contact with a semiconductor, a Schottky barrier is formed [27]. This barrier is caused by the difference of metal workfunction and the electron affinity of the semiconductor. The barrier height for electrons is given by

$$q\Phi_{Bn} = q(\Phi_m - \chi) \tag{3-1}$$

And for holes

$$q\Phi_{Bp} = E_g - q(\Phi_m - \chi) \tag{3-2}$$

Where q is the single electron charge, Φ_m is the workfunction of metal, χ is the electron affinity, E_g is the Fermi level energy. Metal like Pd or Ni has higher workfunction compared with the intrinsic Fermi energy of Si, so such metal is called "p-type" metal. In case of Pd, work-function is Φ_m = 5.12 eV in vacuum. The valence band energy for Si is $E_v = \chi + E_g$ = 5.17 eV (where χ is electron affinity which equals to 4.05 eV, and E_g is the band gap of Si which is 1.12 eV). Hence, the barrier height for holes at valence band can be expressed by $\Phi_{bp}(Pd)=E_v - \Phi_m=0.05$ eV. As for Ni (Φ_m = 5.15 eV), we can get similar result by the same calculation: Φ_{bp} (Ni) = 0.02 eV.

These barrier height values are very small. On the contrary, the barrier height for the electron becomes very large, Φ_{bn} (Pd)= $\Phi_m - \chi$ = 1.16 eV. If gate bias is applied to allow transport of holes in the channel, the Schottky barrier will not block the current. However, if electrons are accumulated in the space charge region, they are blocked by the Schottky barrier height at the interface of metal.

The key reason for the ambipolar performance is the high work-function metal S/D suppresses the carrier transport in the channel. This observation can be explained by a band diagram, which shows bending under gate and drain bias control. For undoped and boron doped nanowire MOSFETs in thermal equilibrium state, the band diagram of the device is shown in Figure 3.11(a). Both electrons and holes are needed to overcome the high barrier to inject into the nanowire channel. Hence, the device is at the "OFF" status. When negative voltage bias is applied, the band of channel bends

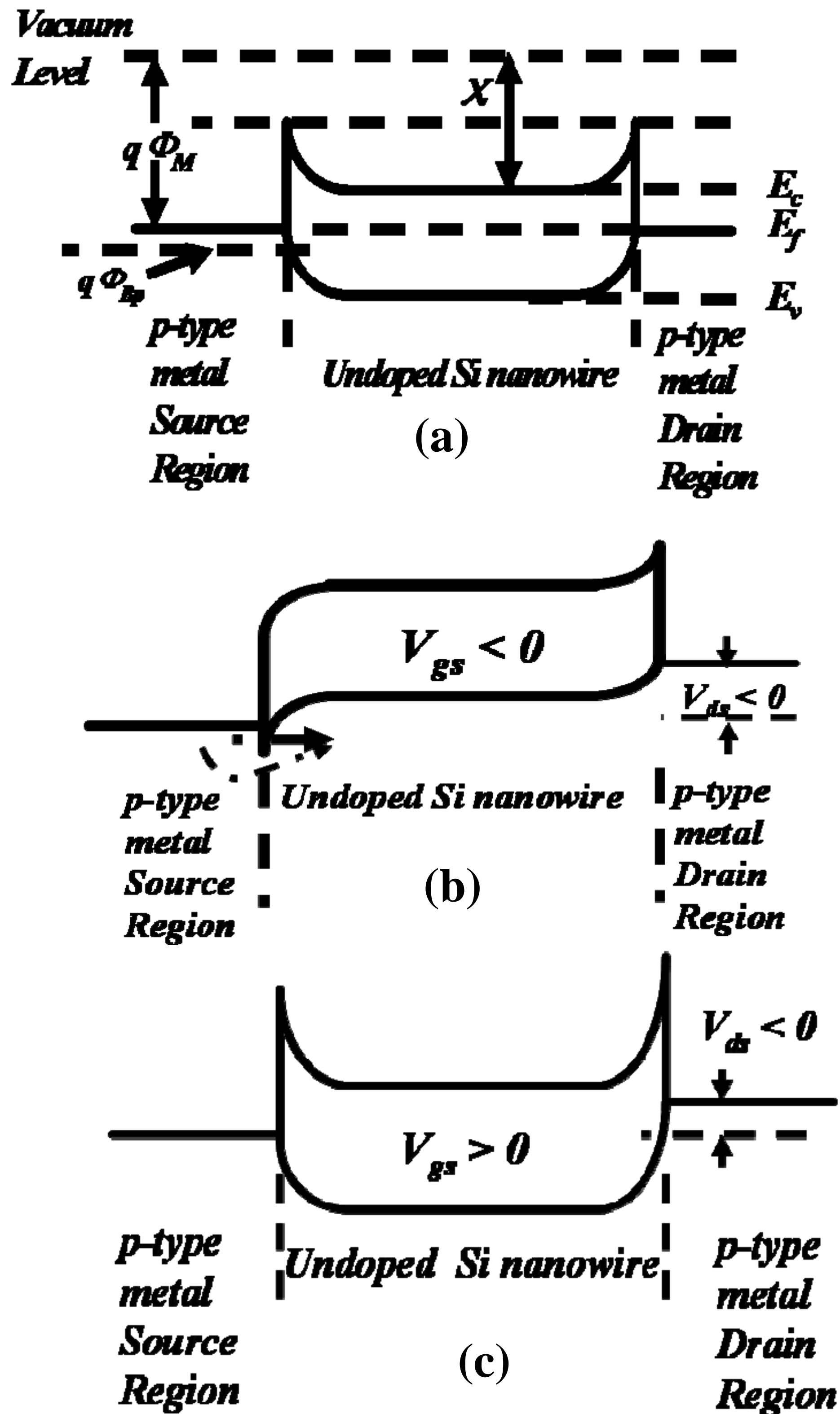

Figure 3.11: Band diagram along SiNW channel from Source to Drain under different bias voltage **(a)** At thermal equilibrium status without any gate or drain bias. **(b)** Negative gate and drain bias ($V_g<0$, $V_{ds}<0$) **(c)** positive gate and negative drain bias ($V_g>0$, $V_{ds}<0$)

up and holes accumulate in the channel. Thus, the effective barrier height for holes at S/D contact decreases while that for electrons increases. Obviously, holes become the major carriers and are thermal emitted into channel if a drain bias voltage is applied (Figure 3.11(b)). If further negative gate voltage is applied, Φ_{bp} remains but the barrier's width will become smaller. Consequently, the efficiency of tunneling through the barrier will increase. As many other reports claimed [20, 28], the "ON" current is composed of hole carriers by both thermal injection and barrier tunneling mechanism. Therefore, I_{ON} still increases although barrier height does not change. At the drain side, the effective Schottky barrier is lower down due to the negative drain bias. Hence this barrier effect can be negligible compared with the source side. When under positive gate bias, holes transportation is blocked (Figure 3.11(c)). However, this doesn't mean that the electron can overcome the huge barrier by thermal emission because the real barrier for electrons is too high. In addition, the barrier's width is too large for electrons to tunnel through. Consequently, I_{OFF} is suppressed at a very small value.

For phosphorus doped SiNW MOSFETs, the majority carrier is electrons. Even at thermal equilibrium, the channel band is already bent down considerably to

align to the Fermi level of Ni and SiN. Hence, even if there is no gate bias, the barrier is easier for electrons to tunnel through under a small drain bias. This is why the device is "on" at zero gate bias. Further positive gate bias makes the barrier width thinner and allows for more electrons transport through the barrier. But importantly, the real barrier height is not changed and current increases slowly.

Based on this theory, we can now explain our nanowire devices performance. The majority carriers in phosphorus doped SiNW electrons need to overcome a very high barrier due to the big difference between the Ni work-function and the SiNW

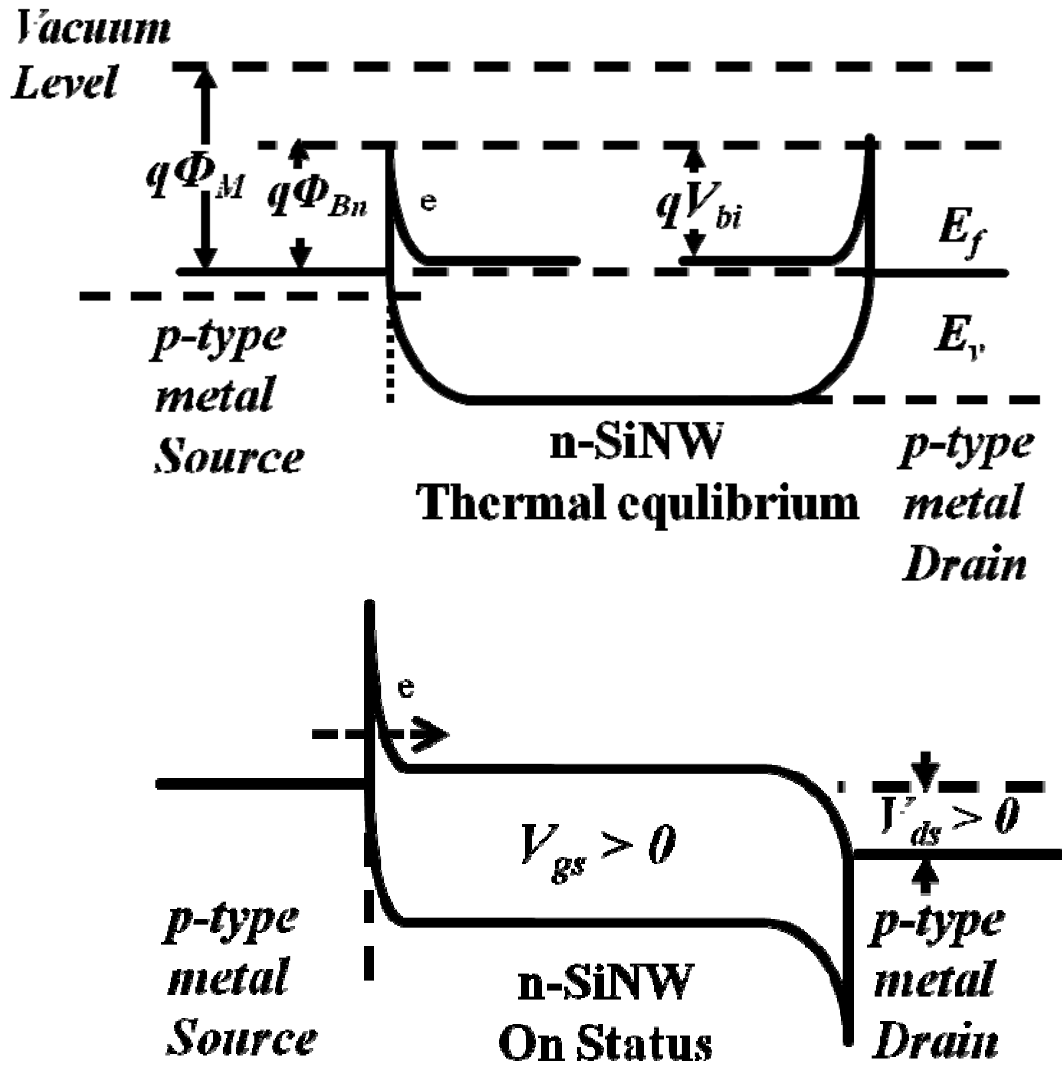

Figure 3.12: Phosphorus doped SiNW device band diagram variation when gate bias is applied. (a) at thermal equilibrium status, holes are blocked the Schottky barrier. Electrons can tunnel through the barrier. (b) when positive gate bias is applied, more electrons can tunnel through the barrier. Without thermal injection, the tunneling current is smaller compare with undoped or p-type SiNW based devices drive current.

valence band. The on status current for phosphorus doped SiNW MOSFET is smaller than the comparable devices formed by undoped or boron doped nanowires.

Second, for undoped SiNW MOSFET, the higher workfunction metal Pd is used to form metal S/D. The Φ_{BP} for undoped SiNW is lower and allows more holes injecting into the nanowire channel. Another reason is that high-k gate dielectric is used for device integration which improves the gate control compared with doped

SiNW devices.

We can also use a low workfunction "n-type" metal to form a low barrier for electrons and a high barrier for holes. As such, this research will pursue a working SiNW n-MOSFET. However, the performance of a n-SiNW MOSFET is not satisfactory. The Ion current is quite low, and the process yield is also far from satisfactory. A possible reason is the unstable chemical properties of a low workfunction metal. Ti, Yb, these metal are very easily oxidized in air. Thus, the contact resistance for the device is extremely high. Even if we use some stable metal as capping layer covering the n-type metal, the work-function of the alloy is changed. Therefore it is difficult to fabricate an operational n-SiNW MOSFETs.

3.3.4 Short channel SiNW MOSFET

With the ambitious requirements for scaling down of the MOSFET device, research into shorter channel MOSFETs grown with nanowires is a priority. Based on the last long channel SiNW FET fabrication, we tried to reduce the channel length and form a short channel SiNW MOSFET. The device structure is exactly the same as the long channel device mentioned before since most processes of the standard long channel and short channel device are the same, except that EBL channel length definition is changed to a 50nm gap between the S/D. After a lift-off process, the gate length of the short channel device is as only 65 nm, as shown in Figure 3.13.

Figure 3.14 (a) & (b) shows the device performance of a 65nm gate length MOSFET. Compared with 1μm SiNW FET, a clear increase in drive current is observed (I_{on}=350nA, V_{DS}=-0.1V). Transconductance in the linear triode region is $G_m=dI_{DS}/dV_{GS}$=0.23μS. The transfer and output characteristics show a typical short channel effect. The saturation part of the I_{DS} in the transfer characteristic curve is not

obvious due to the charge sharing model. Also the decrease in the I_{on}/I_{off} ratio (10^3) and large subthreshold slope (330mV/dec) also suggest that poor gate controllability of the short channel is affected by the dip in the drain field induced band.

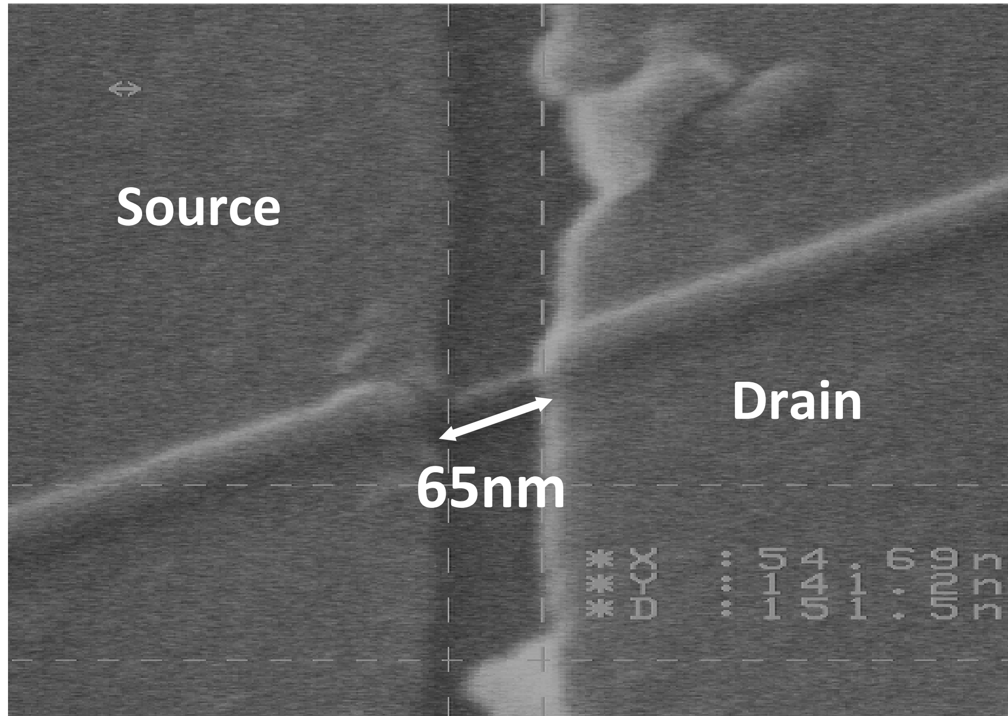

Figure 3.13: Top view SEM picture of fabricated device structure, and back gated MOSFET with only 65nm gate length.

As we know, MOSFET device has two perpendicular electrical fields: vertical gate field and horizontal drain bias field. For our nanowire transistor, the vertical gate field is relative smaller compared with planar Si MOSFET. This is due to the small contact area between the nanowire and gate dielectric layer. Therefore, the drain bias plays more important role in our device performance. This effect is more obvious for our short channel transistor. From the Figure 3.14 (a), when the drain bias is small as 0.1V, the device delivers I_{on} 350nA when V_{DS} is 0.1V, S.S. 330mV/decade, I_{off} ~ $2x10^{-9}$A. Compared with the reference long channel device performance, the short

channel device has higher $I_{on,}$ higher I_{off} and poorer S.S. This can be attributed to short channel effect.

Although a MOSFET device has been successfully fabricated, the short channel NW transistor still has significant potential for improvement. For example, the drive current of the device is still relatively low, which may be due to the S/D Schottcky contact and poor back gate control.

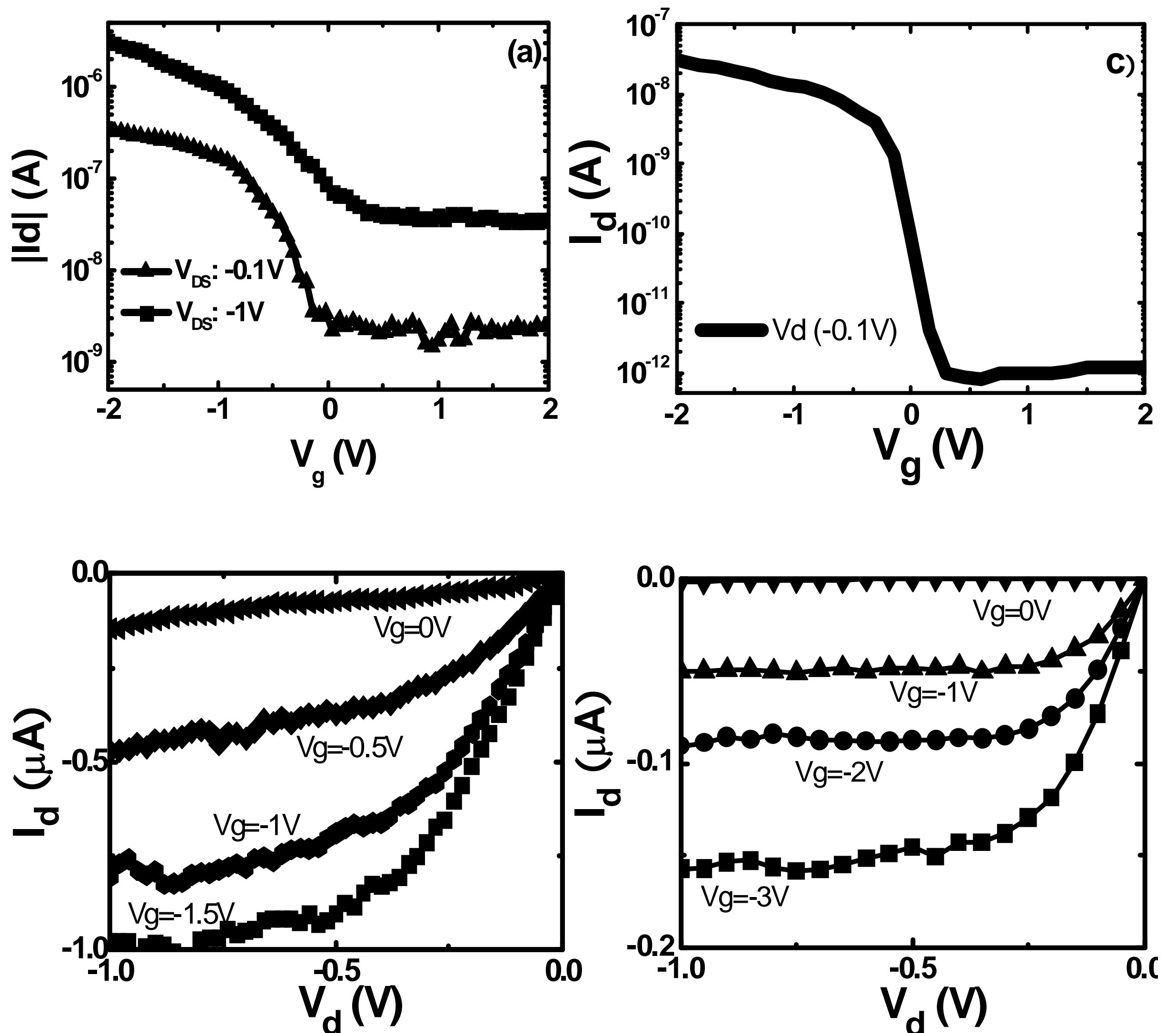

Figure 3.14: Device performance comparison of long channel (1um) and short channel SiNW MOSFET with same metal S/D and gate dielectric. (a) I_d-V_g Transfer characteristics of short channel SiNW MOSFET. (b) Id-Vd output performance of short channel device. (c) -V_g Transfer characteristics of long channel SiNW MOSFET with same gate dielectric and metal S/D as short channel device. (d) Id-Vd output performance of short channel device.

3.3.5 Annealing effect

As discussed in Section 3.3.1, the horizontal drain bias makes a large contribution to the performance of the nanowire MOSFET. This drain bias is applied on the S/D and nanowire, as shown in Figure 3.9. Therefore, to make a more effective bias, we need to reduce the series resistance of the S/D. The metal S/D itself has very low resistance. However, the interface between nanowire and S/D has a Schottky barrier, which works as a valve to block carrier transport. If the Schottky barrier height can be reduced or even eliminated, "Ohmic contact" could be made to allow carrier injection from source side.

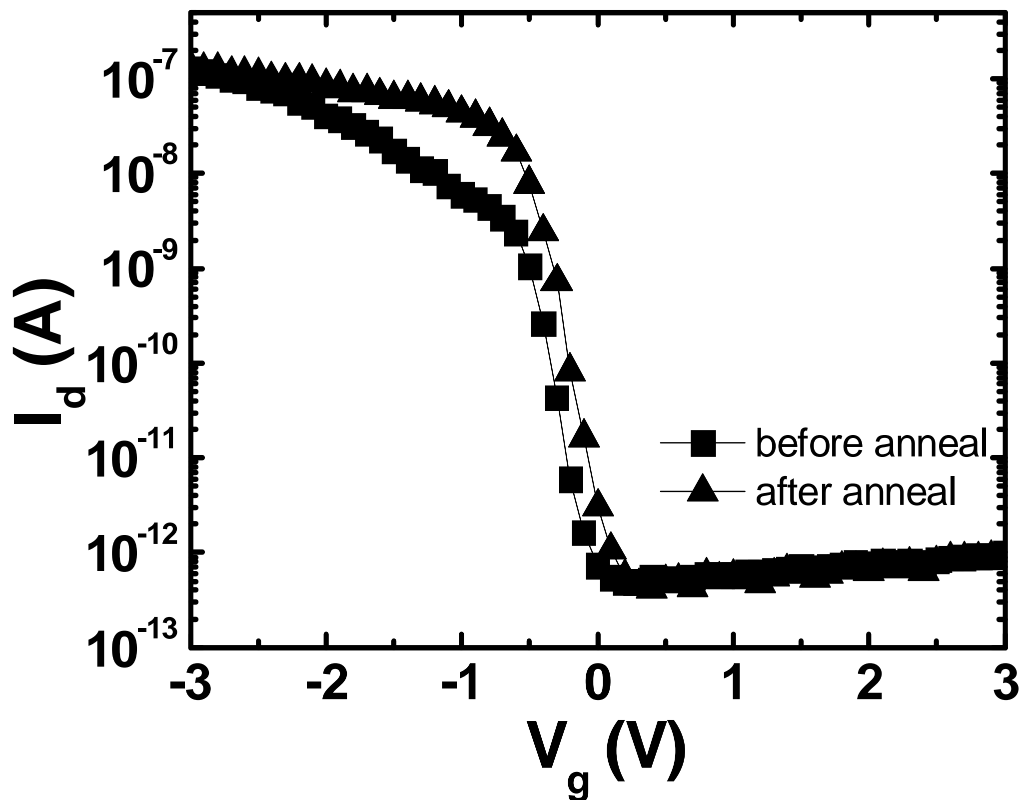

Figure 3.15: Transfer characteristics of the same nanowire device measured before and after forming gas anneal.

One effective method to reduce the barrier is forming gas annealing. Under high temperature, metal reacts with Si to form different phases of "metal silicide".

This process is called silicidation, which is known to lower barrier height (reference). To make use of this process, after our nanowire device formation, a forming gas anneal was applied in an attempt to reduce contact resistivity.

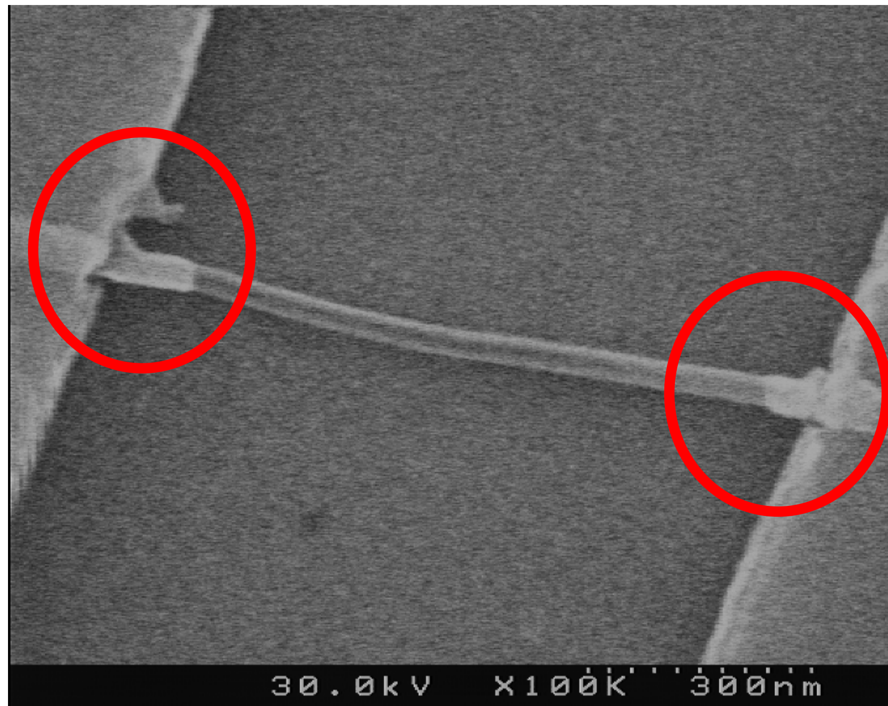

Figure 3.16: The nanowire is consumed after forming gas anneal. Metal silicide is diffused into the SiNW.

We measured the formed device characteristics first and loaded the device back to chamber again to do the forming gas anneal by flowing H_2: 1000 sccm, N_2: 2000 sccm at 300°C for 3 minutes. After the annealing, the device is measured again. The results are shown in Figure 3.15. Clearly, the I_{on} of annealed device increased and I_{off} is still suppressed which means the I_{on}/I_{off} ratio is enhanced. The S.S. is also improved. The improvement indicates the Schottky barrier is effectively lowered.

However, we found the silicidation process need more accurate control. During the annealing process, Pd needs to react with Si which probably causes the

SiNW channel “eaten”. The SEM picture of Figure 3.16 shows that two terminals of SiNW are silicided by the metal S/D. In this case, the channel length is decreased. If we can control the process temperature and time accurately, this effect can provide us very good method to form short channel device [29]. But now, this result is not acceptable for us. Especially for short channel device, after the annealing, the whole channel was consumed and no MOSFET performance was observed. To solve the problem, we add some Si capping layer between the nanowire and metal. So during the annealing process, the capping layer will be consumed and the nanowire channel is protected. Figure 3.15 shows the device performance curve of NW FET with 30nm Pd S/D and 5nm Si capping layer. It also shows the FET performance improved continuously after forming gas anneal.

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Chapter 4

Temperature Dependence of Carrier Transport of Silicon Nanowire Schottky Barrier MOSFET

4.1 Introduction

In the last chapter, the SiNW MOSFETs with different metal S/D are demonstrated. We already find that Schottky barrier (SB) formed at the S/D region is the key point for our device operation. However, limited discussion is reported on the detailed device physics of SB Nanowire MOSFETs [1-3]. Furthermore, the core of this issue, Schottky barrier height (SBH) for nanowire MOSFET is still unknown to us. Some papers discussed the SBH effect on other devices, like carbon nanotube FET and ultra thin body (UTB) SB MOSFET [4-6]. Here, we shed the light from their reports. According to the equation of carrier transport through Schottky barrier, we can extract the SBH if we can get proper data of NW device. Here, SB S/D SiNW MOSFETs have been fabricated with high-κ dielectric (Al_2O_3) and different metal S/D (Palladium, Titanium). The device is loaded into the vacuum chamber and measured at different temperatures (200K~450K). Based on the experimental results, temperature dependence of SB SiNW MOSFETs is investigated and real SBH is extracted. The device characteristics variation with temperature has also been discussed. The results

suggest that in SiNW SB S/D MOSFET, the carrier injection, which is decided by the SB at source-channel interface, is the dominant mechanism which controls the device operation, while acoustic phonon scattering inside the channel has limited effect. Besides, although threshold voltage (V_{TH}) and subthreshold swing (S.S.) has obvious dependence on temperature variation, it cannot be explained only by thermionic emission theory. The Schottky barrier profile, which includes both SBH and SB width, is estimated about its effect on based on the experiment data.

4.2 Experiment Details

First, the SiO_2-coated Si-substrate is dispersed by Au colloids (20 nm) and transferred into CVD reactor. The basic nanowire growth is the same as discussed in the previous two chapters. The detail process of device fabrication is as follows: After DHF cleaning, grown NWs is dispersed on the layer of 10nm thick Al_2O_3 gate dielectric (κ=9) which is grown by ALD system on the sputtered Ta/TaN(50/100nm) which acts as gate electrode. EBL process is employed to define S/D region and channel length is kept at 1μm. Pd and Ti are deposited by E-beam evaporator, followed by lift-off process. To protect nanowire channel affected by water vapor during low temperature measurement, 50 nm SiO_2 capping layer is deposited by E-beam evaporator right after the fabrication of MOSFET. This layer does not change the surface properties of nanowire. Figure 4.3 (a) and (b) shows the SEM images of fabricated metal S/D SiNW SB MOSFET with Pd S/D. For temperature dependent characterization, the nanowire devices are bonded onto a thermally conductive ceramic chip carrier. The carrier is then plugged into a holder lowered into the chamber. The chamber is cooled down by flowing liquid nitrogen under the holder and heated by electric heating system. We measured the same device characteristics

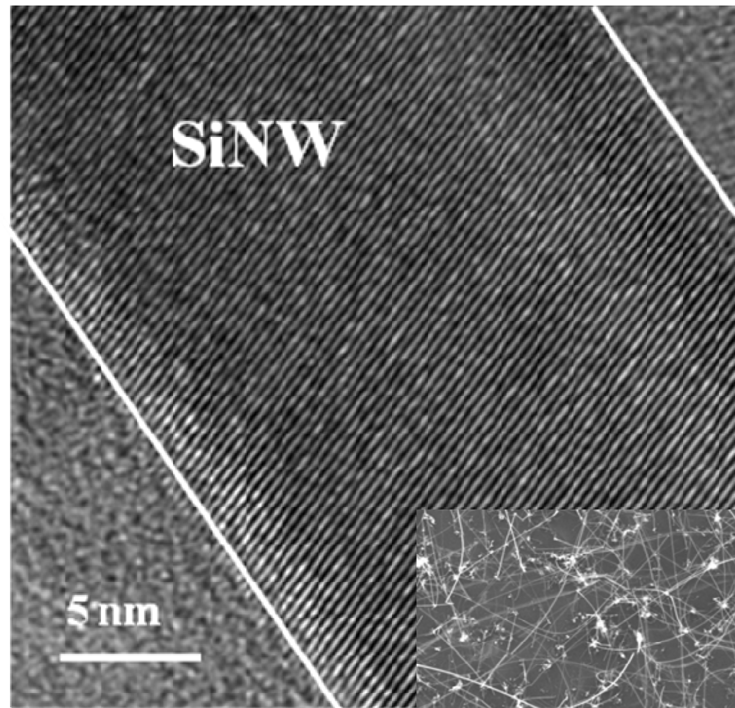

Figure 4. 1: TEM image of single crystal SiNWs with diameter in ~20nm synthesized at 440°C by VLS mechanism. Inset: SEM image of SiNWs (length > 10µm). Inset: top view of SiNW grown on substrate

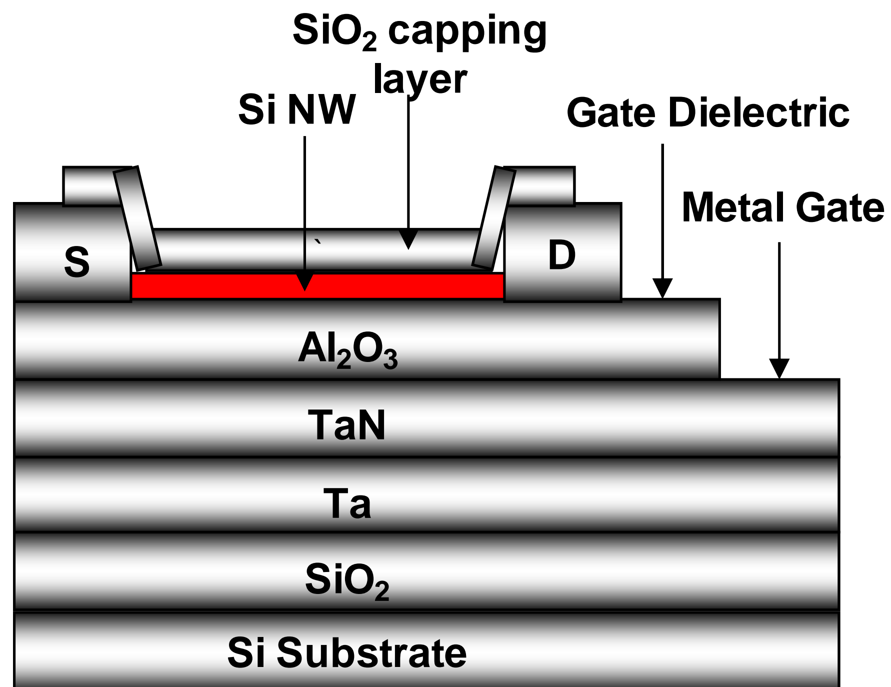

Figure 4.2: schematic picture of fabricated SiNW MOSFET with SiO_2 capping layer.

continuously from low temperature (200K) to high temperature (450K).

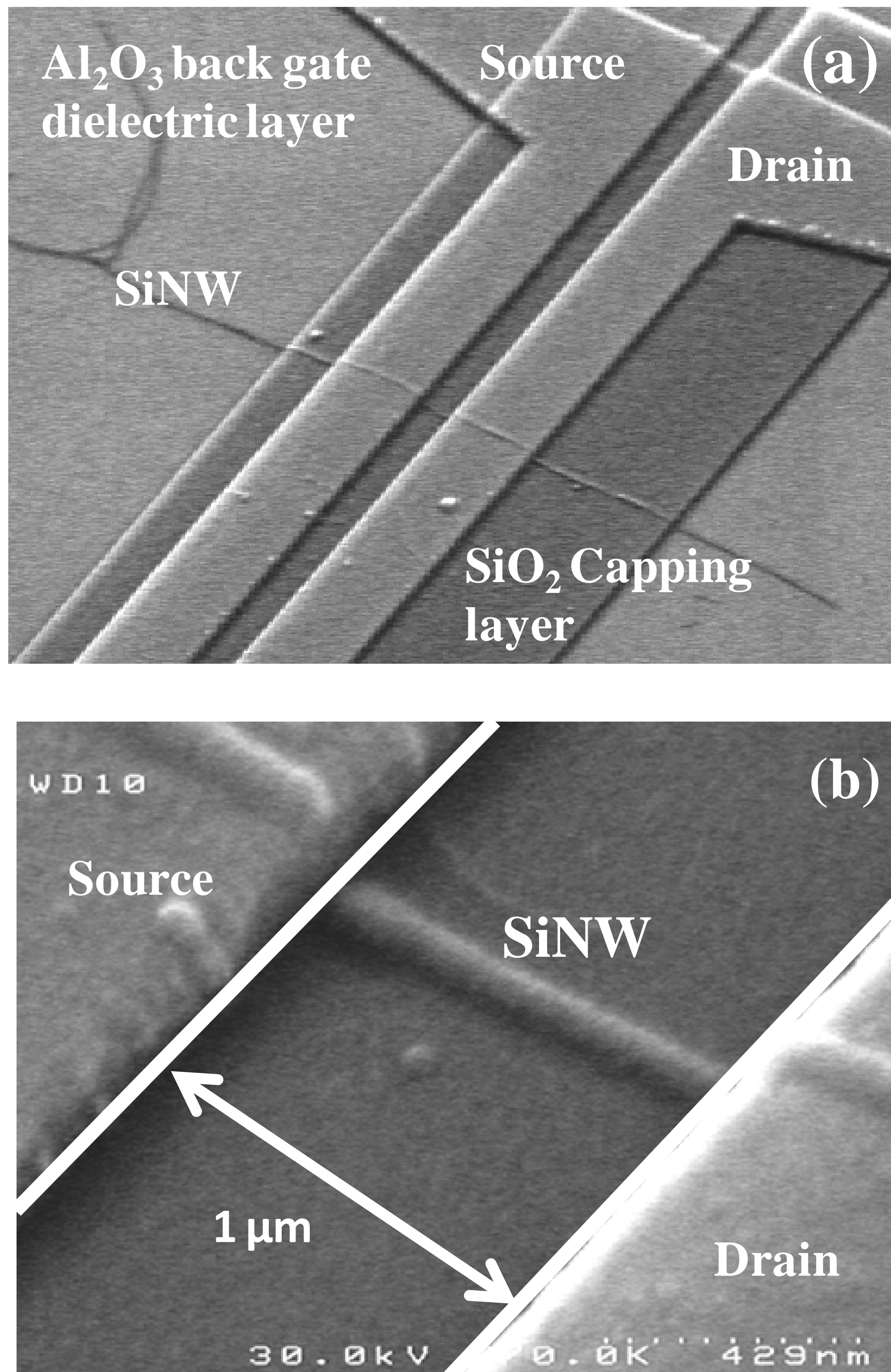

Figure 4.3 (a) Top view SEM picture of fabricated SiNW SB MOSFET with Al_2O_3 gate dielectric and SiO_2 capping layer, and (b) magnified SEM picture of SiNW SB MOSFET with 1μm gate length.

4.3 Device performance in different temperatures

At room temperature, the Pd S/D SiNW SB MOSFET with Al_2O_3 gate dielectric has similar performance as which is reported in chapter 3. The ON-current (I_{ON}) reaches 0.36 μA (I_{DS} at V_{DS} = -0.1V), and V_{TH} ~ -0.1V, peak transconductance G_M ~ 0.2 μS, and subthreshold swing (S.S.) of ~228 mV/dec are observed. Also, the on/off current ratio, $I_{ON}/I_{OF} > 10^5$ and extremely low leakage current (< 1 pA) are obtained.

4.3.1 I_{ON} and I_{OFF}:

Figure 4.4 (a) and (b) show the input transfer characteristics of SiNW SB MOSFET at different temperatures ranging from 200K to 450K and the output characteristics at room temperature. As temperature decreases, I_{ON} decreases by approximately 3.5 times as shown in the Figure 4.4 (a) (linear scale curve). This is contrary to the conventional MOSFET device performance, since at lower temperatures we see a higher drive current due to enhanced mobility which is caused by suppression of acoustic phonon scattering at low temperature [7]. Furthermore, at “OFF” state, the I_{OFF} shows more severe temperature dependence compared with I_{ON}. Similar results have been reported in previous work on planar SB MOSFETs [5]. It is known that in one dimensional FET with Schottky barrier S/D, carrier injection at the interface of source and channel plays more important role than carrier transport in the channel [3], [6]. Therefore, it clearly indicates that carrier transport in the Pd S/D SiNW SB MOSFET is not the limiting factor in the device operation so that acoustic phonon scattering is not the dominant parameter to determine the device performance. There are two mechanisms contribute to the carrier injection to overcome the Schottky barrier, one is tunneling and the other is thermionic emission [8].

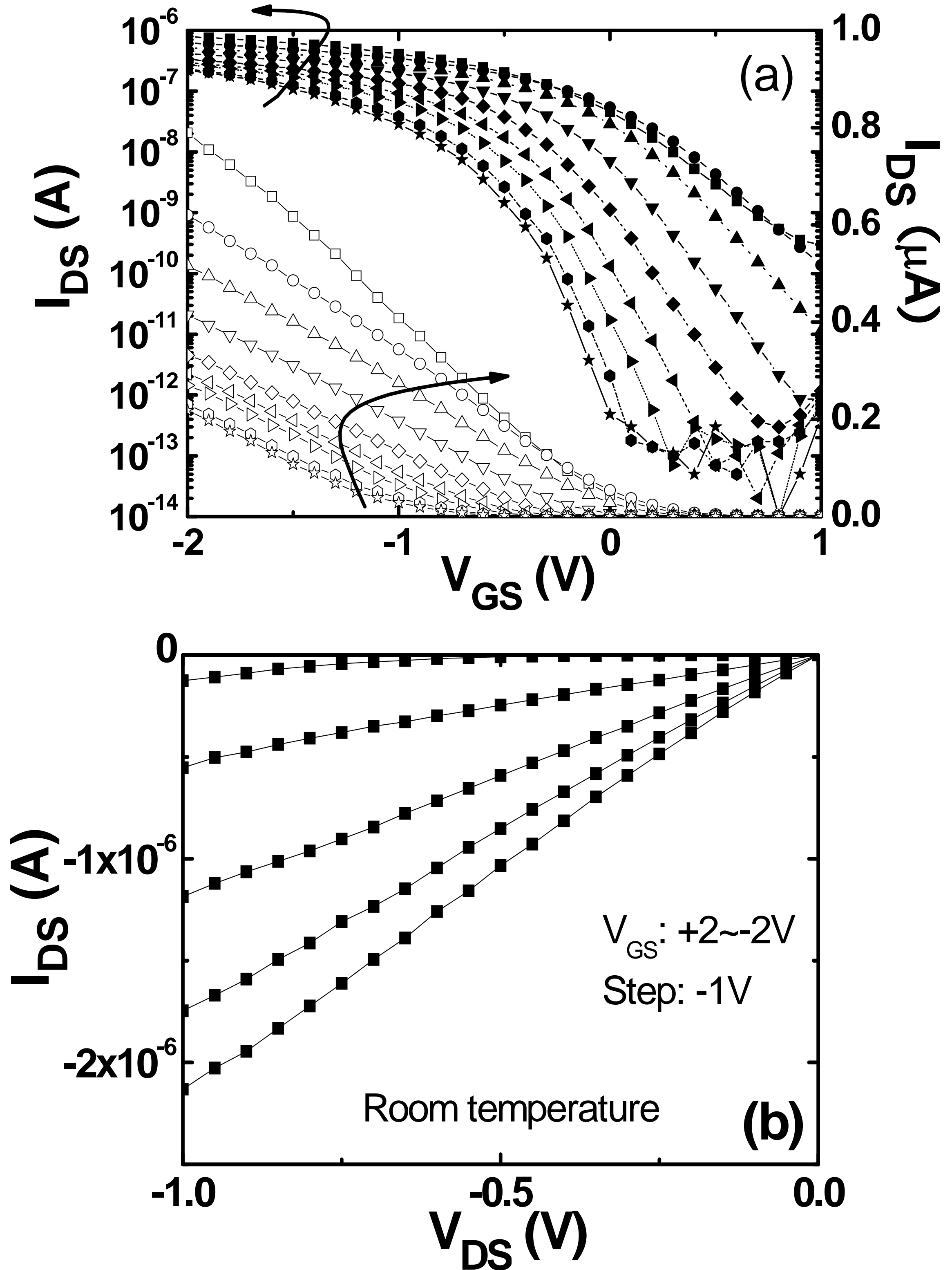

Figure 4.4: (a)Typical I_{DS}-V_{GS} transfer characteristic of Pd S/D SiNW SB MOSFET at different temperatures (T=192K, 200K, 225K, 250K, 300K, 350K, 400K, and 450K from bottom to top) in both log and linear scale. (b) I_{DS}-V_{DS} output characteristics of the same device at room temperature.

Here, at the "OFF" state, this current decrease could be attributed to domination of thermionic emission current component which varies with temperature. And the tunneling current component could be the dominant parameter when the device is at "ON" state.

4.3.2 Schottky Barrier Height Extraction:

Based on the discussion above, the Schottky barrier height (SBH) is a key parameter to investigate the device operation principles of the SiNW SB MOSFET. Here, we use the thermionic emission equation to extract the curve of effective barrier height for holes (Φ_{BH}) as a function of gate voltage (V_{GS}) [9].

$$I_{DS} = -SA^{*}T^{2}\exp\left(-\frac{q\phi_{Bp}}{k_{B}T}\right) \tag{4-1}$$

where S is the cross section area of NW channel, A* is the effective Richardson constant, T is the absolute temperature and Φ_{Bp} is the effective SBH for holes. However, it is difficult to assume the value of the S and A*. Therefore, we use different drive current I_{DS} which are measured at different temperatures to extract the effective barrier height for our device.

$$\frac{I_{DS1}}{I_{DS2}} = \frac{T_1^{2}}{T_2^{2}}\exp\left(-\frac{q\phi_{Bp}}{k_{B}}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)\right) \tag{4-2}$$

Based on equation (4-2), we can get function between drive current and SBH. But please noted, here the SBH is the effective barrier height. On the other hand, this drive current is also related to the gate bias V_{GS}. Therefore we can set up the relationship between the effective barrier height and gate voltage. Figure 4.5 shows the clear trend of effective barrier height variation with V_{GS} at different temperatures. At the equilibrium state, the effective barrier height for holes is high (Figure 4.6 (a)).

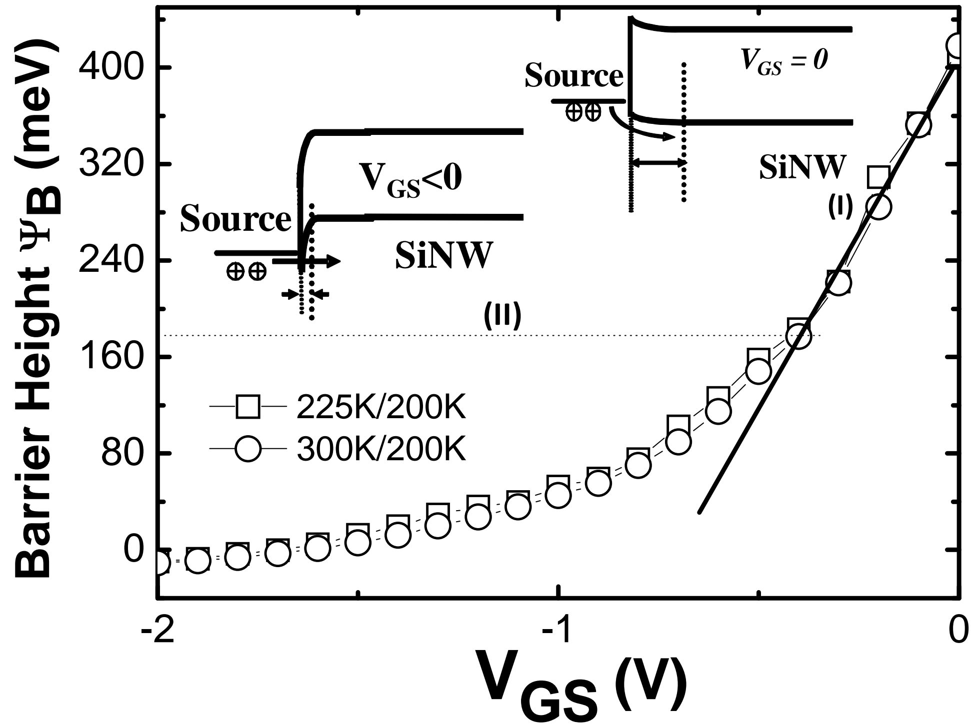

Figure 4.5: Effective Schottky barrier height as a function of V_{GS} (at V_{DS}= -0.1V) for Pd S/D SiNW MOSFET extracted at different temperatures (200K/225K, 200K/300K). Inset: i) the schematic band diagram at the interface of source and channel at equilibrium state. ii) the schematic band diagram at the interface of source and channel at device "ON" state.

When the negative gate voltage is applied, the effective barrier height is continuously decreased to real barrier height (Figure 4.6 (b)). After that, the barrier is not decreasing anymore, but the barrier width is reducing (shown in Figure 4.5). The real barrier height can be extracted from the condition at which the calculated SBH begins to deviate from the linear fitted line of the effective Φ_{BH} versus V_{GS} curve. The calculated real SBH for Pd/SiNW channel contact is ~180 meV, which is smaller than other reference [8]. This may be explained by the one dimensional device geometry which can reduce the barrier height [10]. Although only thermionic emission theory is used here to extract SBH, tunneling mechanism should be considered in this SBH variation trend especially when device is at "ON" state. So the effective barrier height continues reducing at more negative V_{GS} region since the tunneling current

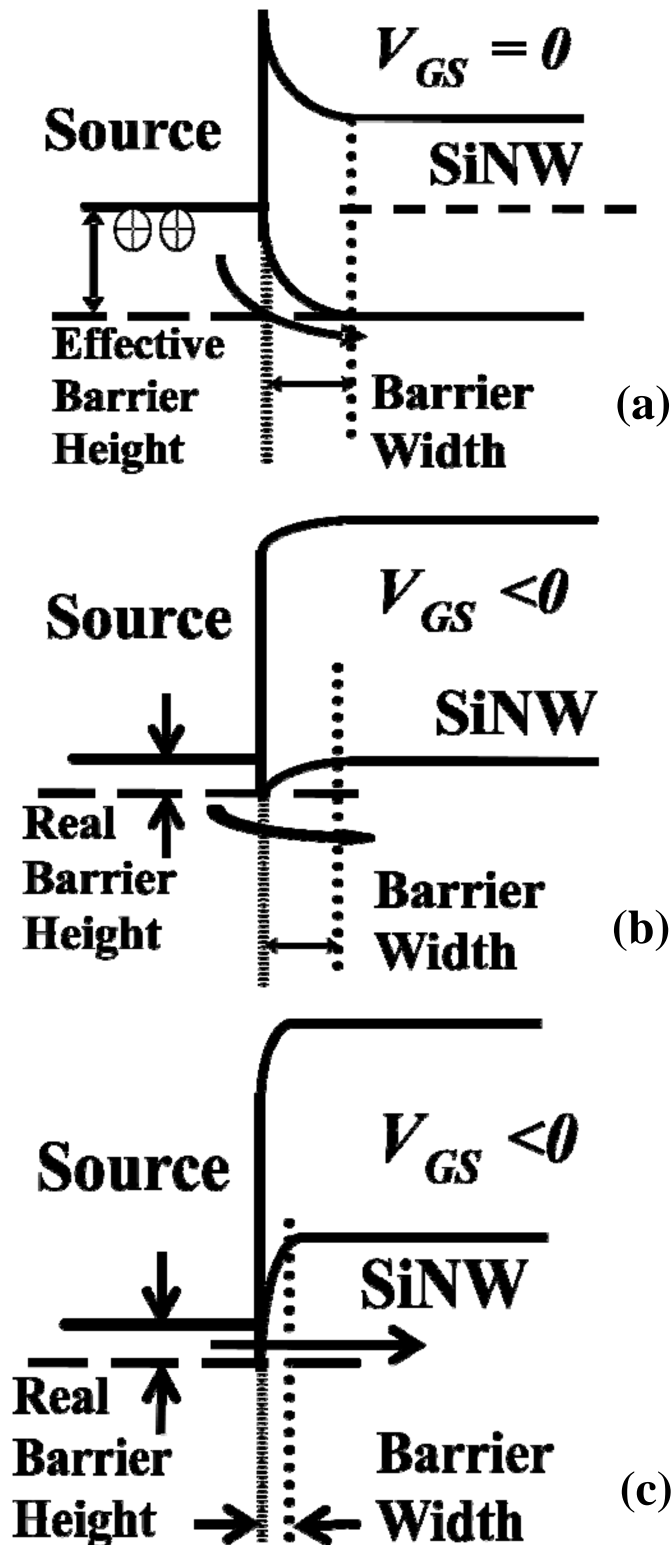

Figure 4.6: Band diagram of Source-nanowire interface (a) at thermal equilibrium status, the barrier width is large due to the undoped nanowire properties. (b) when negative gate bias ia applied, the effective barrier height is lowered down and real barrier height can be extracted. At the same time, the barrier width is also reduced. (c) Further negative gate bias pull up the band of SiNW and the barrier width is small enough for holes to tunnel through.

component increase more and more as shown in Figure 4.5. This is due to high negative gate voltage, which pulls up the band and makes the barrier width thinner. This thinner barrier width can be equivalent to effective barrier reduction which is reflected in Figure 4.6 (c). Even the negative barrier height is observed which further proves tunneling mechanism should be the main carrier transport at the device “ON” state [11].

4.3.4 Threshold Voltage (V_{TH}) and Subthreshold Swing (S.S.)

From the linear transfer characteristics curve, threshold voltage (V_{TH}) at different temperatures has been extracted in Figure 4.7. Threshold voltage shift has been clearly observed. At lower temperature, V_{TH} increases linearly as temperature increases, and the average shift rate reaches 7.4mV/K (200K~300K) which is much larger compared with conventional MOSFET performance (1mV/K) [7]. The possible

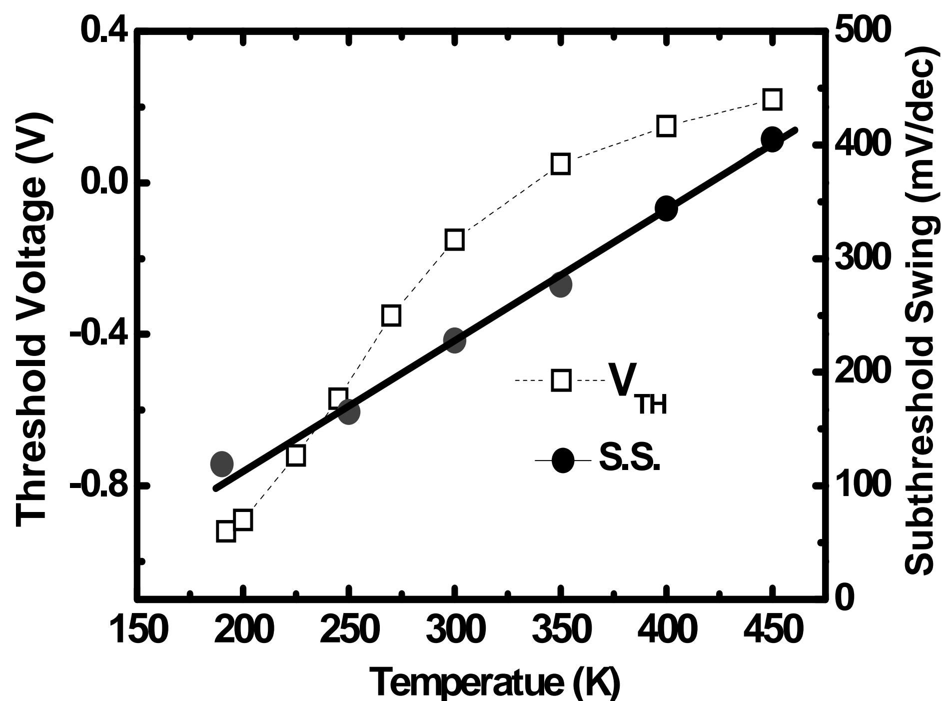

Figure 4.7: Temperature dependence of threshold voltage (V_{TH}) (open square symbol) and subthreshold swing (S.S.) (solid circle symbol) of Pd S/D SiNW MOSFET.

reason for this could be that the V_{TH} shift is controlled not only by thermionic emission and band gap. But also it is controlled by effective Schottky barrier [12]. However, at elevated temperature (>300K), this shift rate decreases and the curve shows saturation trend. Since thermionic emission is enhanced a lot, the Schottky barrier is much easier to be overcome by holes. Therefore, the device performance becomes more dependent on thermionic emission theory and Schottky barrier effect is weakened. Then the shift rate (1.4mV/K from 400K to 450K) becomes more approaching to the conventional value (1mV/K).

Figure 4.7 also shows the curve of S.S. versus temperature which is extracted from the transfer characteristic curve. Unlike the threshold voltage, S.S. has perfect linear dependence over the whole temperature variation range. It is reasonable since the S.S. is extracted at subthreshold region which is mainly controlled by thermionic emission. The S.S. of conventional MOSFETs can be expressed by [7];

$$S.S. = \frac{kT}{q} In(10)(1 + \frac{C_{dm}}{C_{OX}}) \qquad (4\text{-}3)$$

However, the observed slope (1.22×10^{-3} V/dec·K) in S.S. versus temperature curve of Pd S/D SiNW SB MOSFET is much larger than that of normal MOSFETs. It is proposed that S.S. value of one dimensional SB MOSFETs can be expressed as $S.S. = \frac{kT}{q} In(10)(\frac{1}{2} + \frac{\lambda}{d})$ [13, 14], where λ is the relevant length scale on which potential variations are screened, and d is the tunneling length beyond which tunneling current is blocked. Based on this equation, λ=5.64d is obtained for Pd S/D SiNW SB MOSFET, explaining the higher temperature dependence of S.S. considering both thermionic emission and tunneling through low SBH. Considering

our device geometry, the λ can be expressed as $\lambda = \sqrt{\frac{\varepsilon_{Si}}{\eta\varepsilon_{ox}} d_{SiNW} d_{OX}}$, where, Si permittivity ε_{Si} =11.9, Al_2O_3 permittivity ε_{ox} =9, nanowire diameter d_{SiNW} = 20nm, gate oxide thickness d_{OX} =10nm, and η = 1.3 (parameter for the nonuniformity of the lateral field across SiNW [18]). λ is calculated to be 14.3nm.

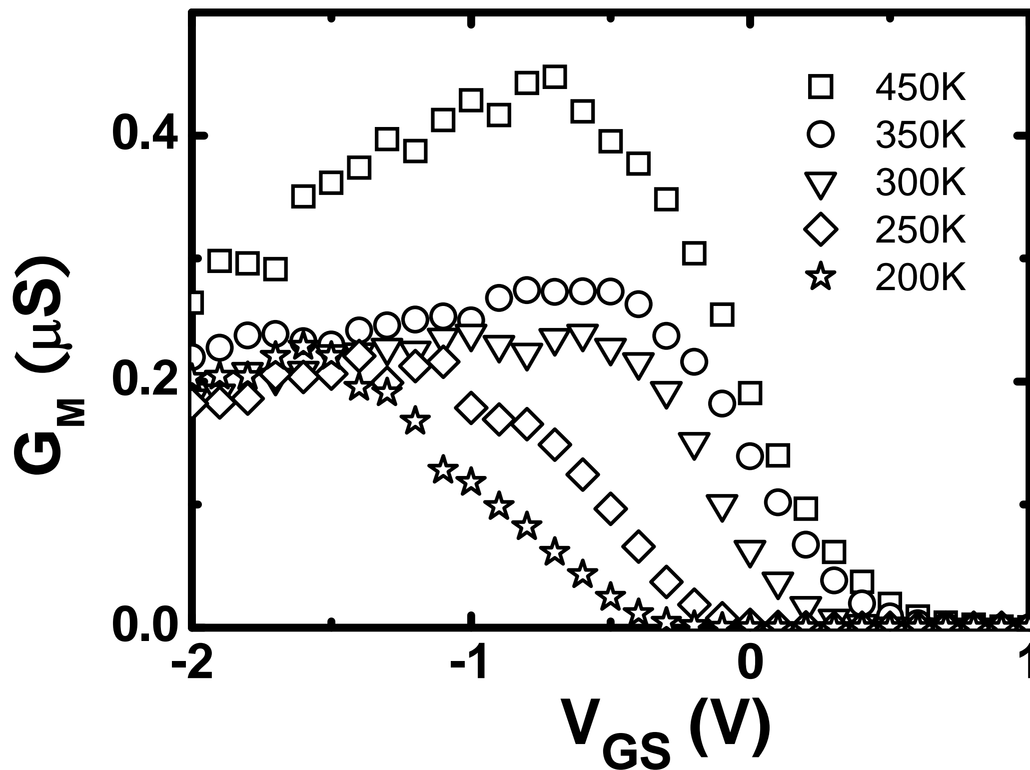

Figure 4.8: Transconductance (G_M) as a function of Temperature variation for Pd S/D SiNW MOSFET at 200 ~ 450K.

Figure 4.8 shows the temperature dependence of transconductance (G_M) for Pd S/D SiNW SB MOSFET. It is known that G_M can be seen as the key parameter to determine the gate controllability. At high temperature, G_M has larger value and increases earlier and more quickly than it varies at low temperature. These results also indicate that the device operation is controlled by carrier injection at Schottky contact

rather than carrier transport in NW channel. At higher temperature, thermionic emission effect has been enlarged and thermal assisted tunneling probability is also increased. Therefore, carriers begin to transport when small gate bias applied. On the other hand, at lower temperature, the device has fewer carriers jump over the barrier at small gate bias. Only when more negative gate bias reduces the band width and tunneling current increases, the gate controllability can be improved largely.

4.3.4 Ti S/D SiNW SB MOSFET

Figure 4.9 (a) and (b) show the temperature dependence of transfer characteristics of Ti S/D SiNW SB MOSFET and its output characteristics at room temperature. The device shows degraded device performance compared with Pd S/D one: low I_{ON} current (~10^{-9} A, V_{DS}=-0.1V) and large I_{OFF} (~10^{-11} A) which translates to smaller I_{ON}/I_{OFF} (~10^{2}). Also, S.S. is degraded a lot. Ti S/D SiNW SB MOSFET has very large temperature dependence when it is measured at different temperatures. From 200K to 450K, the I_{ON} and I_{OFF} have increased by more than two and three orders of magnitude respectively. While Pd S/D device has only around four times increment of I_{ON} within the same temperature range. This indicates that the tunneling current component at device “ON” state is small since it is suppressed by the higher barrier height for both electrons and holes. In addition, the possible reason for large temperature dependence could be due to the thermally assisted tunneling [12], where the carrier jump to the higher level at source region by thermal activation and then tunnel through the barrier at the thinner width (as shown in inset of Figure 4.10). If temperature is lower, this mechanism will be suppressed. This is especially effective for higher barrier case like Ti S/D. Since Pd S/D has lower barrier height for holes and direct tunneling probability is high, the thermally assisted tunneling effect is not

obvious at lower temperature. Therefore, barrier height can determine the carrier injection mechanism in SiNW SB MOSFET.

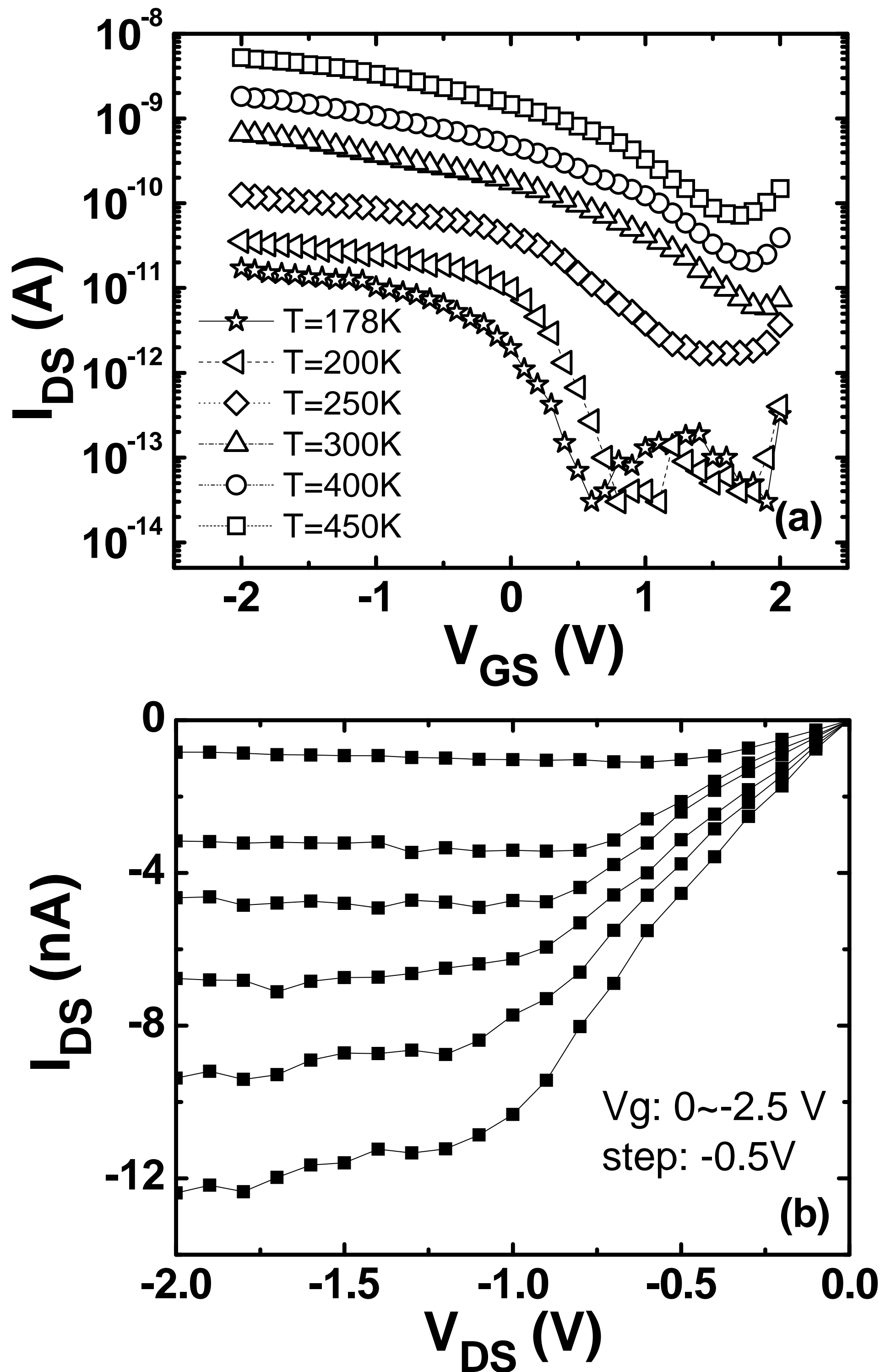

Figure 4.9: (a) Typical I_{DS}-V_{GS} transfer characteristic of Ti S/D SiNW MOSFET at different temperatures (T=178K, 200K, 250K, 300K, 400K, and 450K from bottom to top). (b) I_{DS}-V_{DS} output characteristics at room temperature.

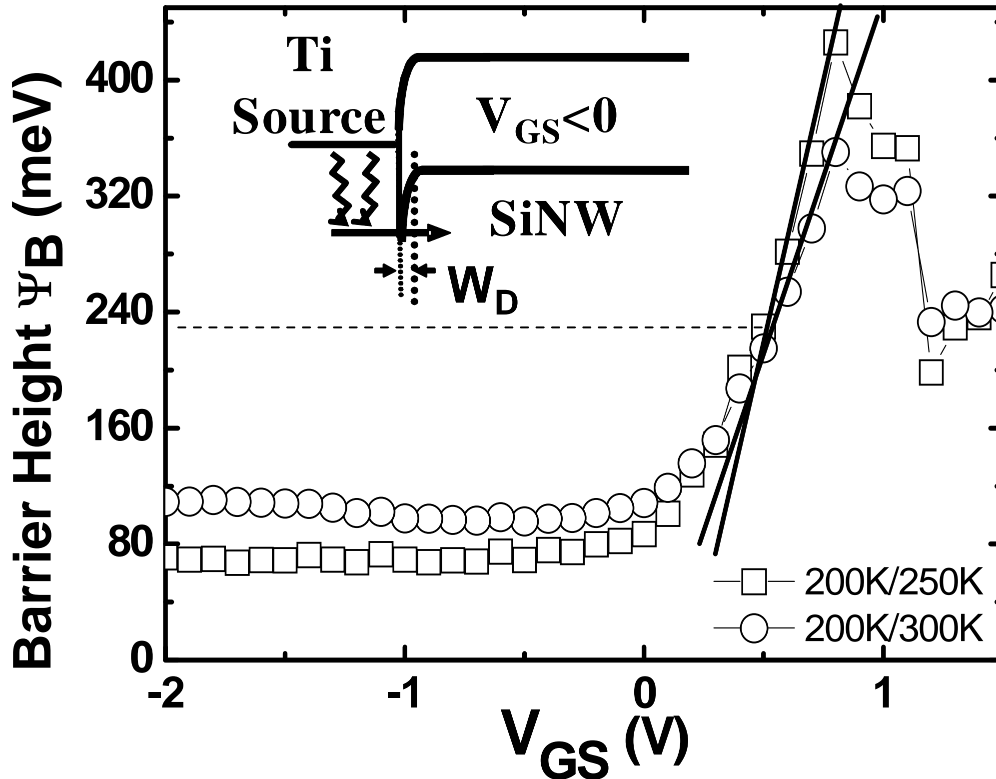

Figure 4.10 Extracted effective Schottky barrier height as a function of V_{GS} (at V_{DS}= -0.1V) for Ti S/D SiNW MOSFET at different temperatures. Inset: schematic picture of thermally assisted tunneling at valence band under negative gate bias.

In Figure 4.10, the effective barrier height has also been extracted by Equation (2) based on the I_{DS}-V_{GS} data which is shown in Figure 4.9 (a). The graph clearly shows that the Ti S/D SiNW SB MOSFET has larger effective barrier height at device "ON" state. The barrier is not lower down at high negative gate bias region, indicating the tunneling component is not increased even though the band pulls up.

4.4 Conclusion:

Different metal S/D SiNW SB MOSFETs have been fabricated and measured at different temperatures. Effective barrier height has been extracted and discussed based on the experimental data. The unexpected device performance of such devices has indicated that the device operation is dominated by the shape of Schottky barriers

between the S/D and nanowire rather than carrier transport in the NW channel [15, 16]. The I_{ON} and G_M increment with higher temperature strongly proves that acoustic phonon scattering has limited effect in device operation, while carrier injection is dominated by the barrier profile at source-channel interface. At subthreshold region, S.S. has linear temperature dependence but SB effect should also be considered. For lower barrier height S/D (Pd), the carrier injection can be dominated by tunneling component. But for higher Schottky barrier height as Ti, the device operation has much more dependence on temperature since the tunneling is blocked and thermionic emission and thermally assisted tunneling effect is more pronounced.

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Chapter 5

Electrical Transport of Bottom-Up Grown Single Crystalline $Si_{1-x}Ge_x$ Nanowire

5.1 Introduction

In the last chapters, we have discussed high performance SB SiNW MOSFET and the device physics which control the carrier transport in the nanowire channel. However, most of our experiments and other research groups' work are only focused on pure Silicon or Germanium nanowires growth, characterization of electrical and optical properties [1-7], and assembly of devices. Then how about using $Si_{1-x}Ge_x$ nanowire as the device channel? It could have higher mobility than pure Si, and it has better interface properties than pure Ge. Obviously, it is a promising active device element for the bottom-up assembly of future electronic and photonic integration, providing potential advantages of high mobility and possible band gap engineering. Recently, we and other group reported on the growth, physical and chemical properties, control of chemical composition, and doping process of $Si_{1-x}Ge_x$ nanowires (NWs) grown via Vapor-Liquid-Solid (VLS) mechanism [8, 9]. But very few works have been reported on the detailed transport properties of $Si_{1-x}Ge_x$ NWs integrated in MOSFET [10], the effects of process parameters and Schottky Barrier Height (SBH) between $Si_{1-x}Ge_x$ NW and metal source/drain (S/D) on transistors performances. In

this chapter, back gated VLS-grown $Si_{1-x}Ge_x$ NW MOSFETs are first time demonstrated in the world by integrating undoped $Si_{1-x}Ge_x$ NW with HfO_2 (20nm in thickness) gate dielectric, TaN/Ta gate electrode, and Pd S/D electrode. To improve the $Si_{1-x}Ge_x$ NW device performance, we utilized phosphorus-doped single crystalline $Si_{1-x}Ge_x$ NWs and thinner HfO_2 gate dielectric layer, the high performance p-MOSFET operations (I_{on} > 100 nA, I_{on}/I_{off} ~ 10^5, and subthreshold slope (S.S.) ~ 142 mV/dec) is achieved. The working devices make it possible for us to investigate the dopant effect in the device performance. In addition, the Schottky barrier of the $Si_{1-x}Ge_x$ NW device is also extracted and compared with that of SiNW MOSFET.

5.2 Experiments

The fabrication process is similar with SiNW MOSFET formation. The Au colloids (20 nm) were dispersed onto the SiO_2-coated Si-substrate. Undoped $Si_{1-x}Ge_x$ NWs (~20 nm) were synthesized at ~430°C via VLS growth mechanism by flowing SiH_4, GeH_4 and H_2 gases simultaneously with the flow rate 200, 20 and 200 sccm respectively in chemical vapor deposition reactor [9]. For doped NWs, the in-situ plasma (300 W) phosphorus-doping process was carried out with flowing PH_3 (500 sccm) and H_2 (1000 sccm) at 440°C, right after the NW growth. Back gated MOSFETs were fabricated on Ta/TaN (50/100 nm) electrode sputtered on SiO_2/Si-sub, followed by atomic layer deposition of HfO_2 using $HfCl_4$ with thickness of 20 and 5 nm, respectively. The grown undoped and doped $Si_{1-x}Ge_x$ NWs were cleaned by DHF and dispersed on HfO_2 dielectric layers. Then, S/D regions were patterned by electron beam lithography and gate length was kept as 1 μm. Pd (80 nm) was deposited by electron-beam evaporator as metal S/D, followed by lift-off process. The

schematic structure of fabricated device is shown in Figure 5.1.

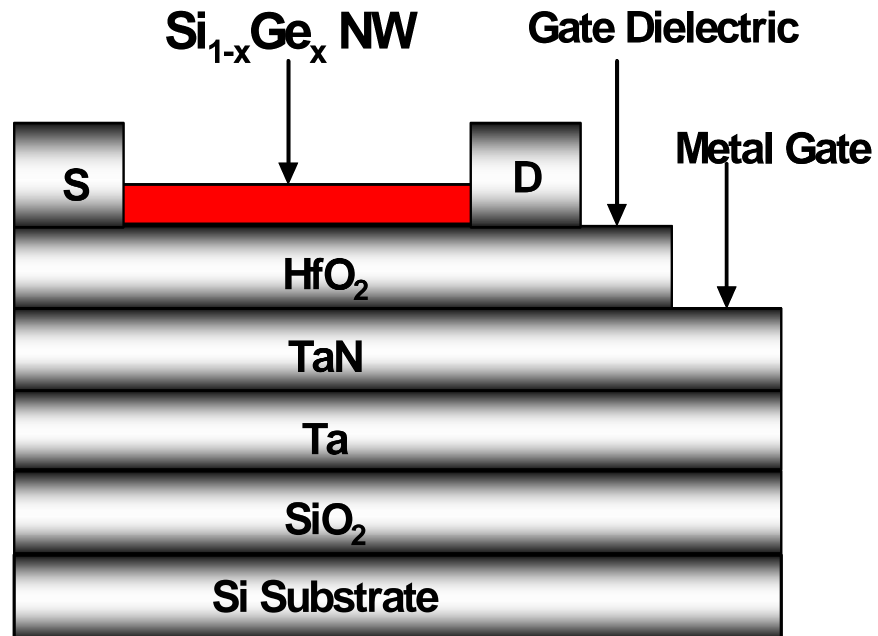


Figure 5.1: Cross sectional schematic picture of a back-gated Si1-xGex nanowire MOSFET with high-κ dielectric and TaN gate.

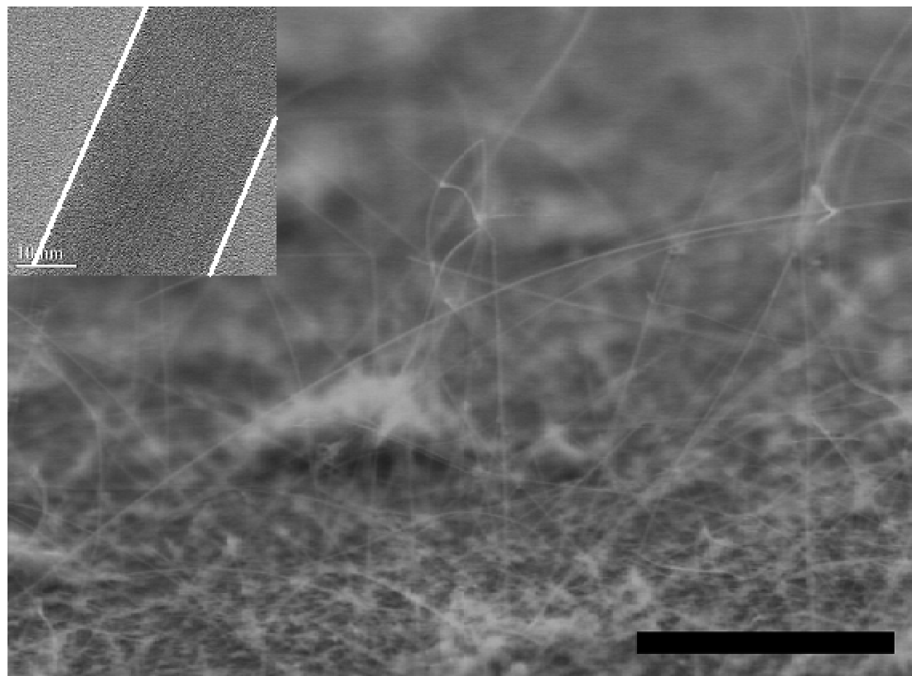


Figure 5.2: SEM image of undoped $Si_{1-x}Ge_x$ NWs grown by VLS mechanism. Inset: TEM picture shows SiGe NW has single crystalline structure.

5.3 $Si_{1-x}Ge_x$ Nanowire Properties:

Figure 5.2 shows the SEM picture of the grown Si_xG_{1-x} nanowires. The density of them is smaller than that of Si nanowires. The average length (~10μm) of Si_xG_{1-x} NWs is long enough for transistor integration. The TEM picture (inset of Figure 5.2) indicates that Si_xG_{1-x} NW is thinner than 20nm in diameter. Excellent single crystalline and negligible amorphous surrounding layer is observed since the growth temperature is relatively lower than SiH_4 decomposition temperature. These excellent properties of Si_xG_{1-x} NW make it perfect candidate for MOSFET integration. The Germanium content can be clearly detected by XPS (shown in Figure 5.3). The plasma phosphorus doped Si_xG_{1-x} nanowire is also successfully fabricated and proved to be single crystallized by the TEM picture (as shown in Figure 5.4). Both Phosphorus and Germanium (13%) contents are detected by EDX (inset of Figure 5.4).

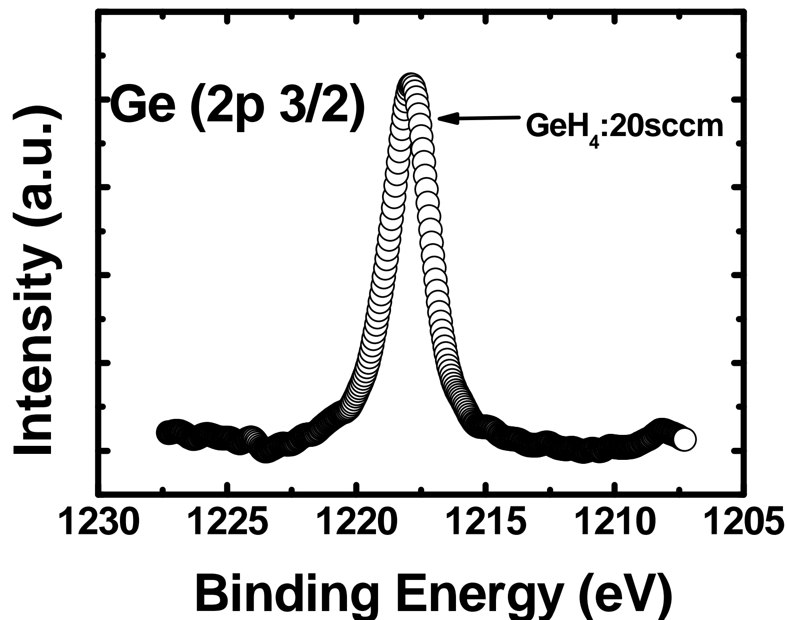
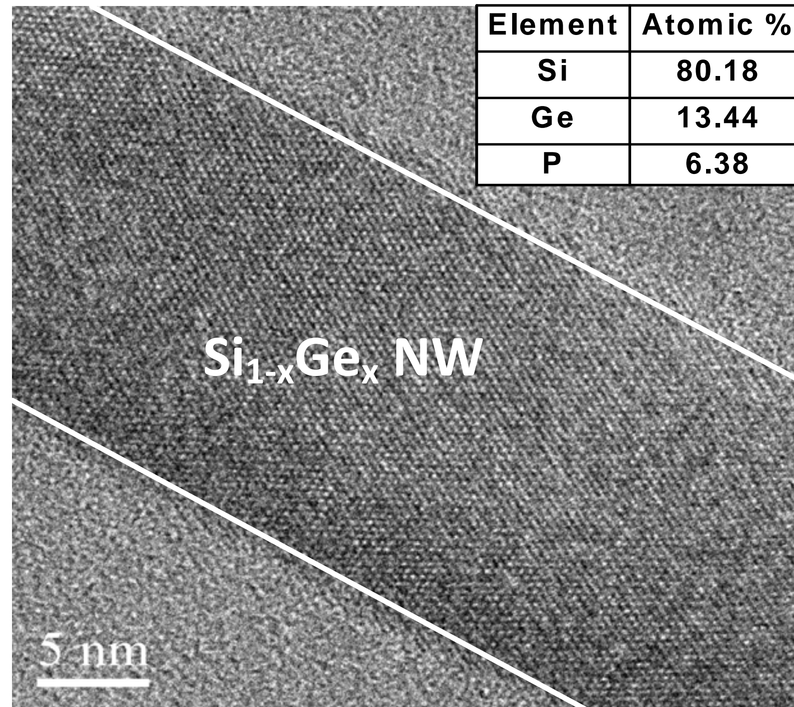


Figure 5.3: XPS graph proves that Ge 2p spectra detected in $Si_{1-x}Ge_x$ nanowire after growing at 430 °C (detecting angle: 10°) [11]



Element	Atomic %
Si	80.18
Ge	13.44
P	6.38

Figrue 5.4: TEM picture of single crystallized phosphorus doped $Si_{1-x}Ge_x$ NW. inset picture: the Si, Ge and phosphorus contents are detected by EDS.

5.3 $Si_{1-x}Ge_x$ NW MOSFET Performance

We investigated three kinds of MOSFETs (device A, B, and C) with different doping or gate oxide thickness. The split Table 5.1 lists the three device conditions. Device A is formed by undoped $Si_{1-x}Ge_x$ NW and HfO_2 gate dielectric (20nm in thickness). Device B is formed by phosphorus doped $Si_{1-x}Ge_x$ NW and 20nm thick HfO_2. To further improve the $Si_{1-x}Ge_x$ NW device performance, device C is integrated

Device	A	B	C
$Si_{1-x}Ge_x$ NW	Undoped	Phosphorus doped	Phosphorus doped
HfO_2 thickness	20 nm	20 nm	5 nm

Table 5.1 Three different SiGe NW MOSFETs with different NWs and thick HfO_2 layer are investigated.

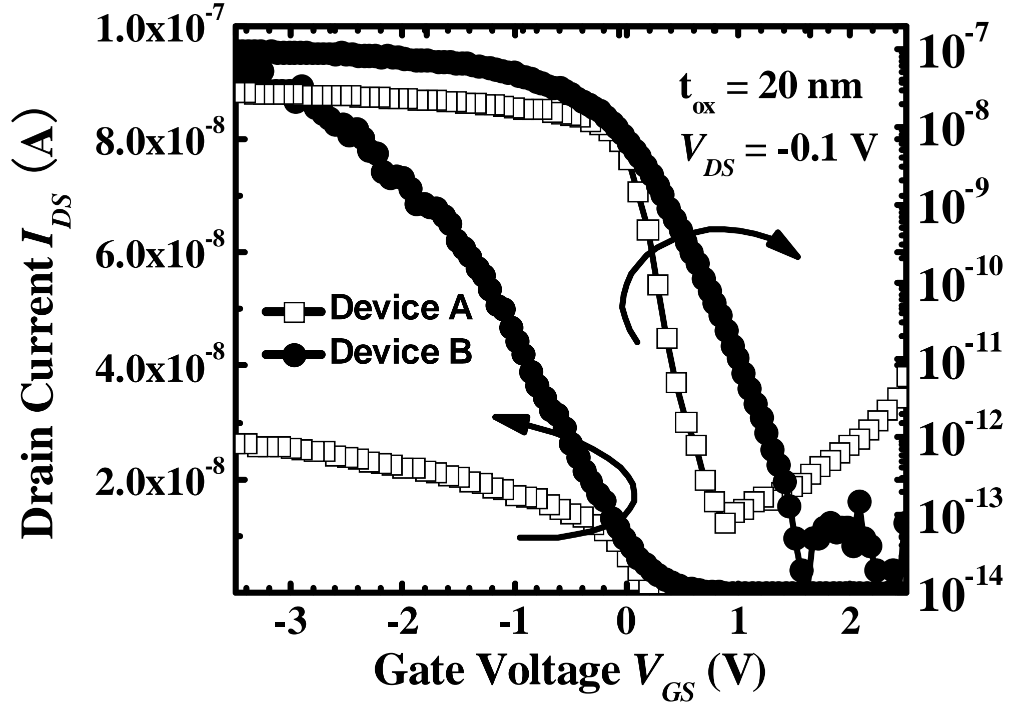


Figure 5.5: Typical I_{DS}-V_{GS} transfer characteristics of device A and B. V_{GS} sweeps from +3 to -3V.

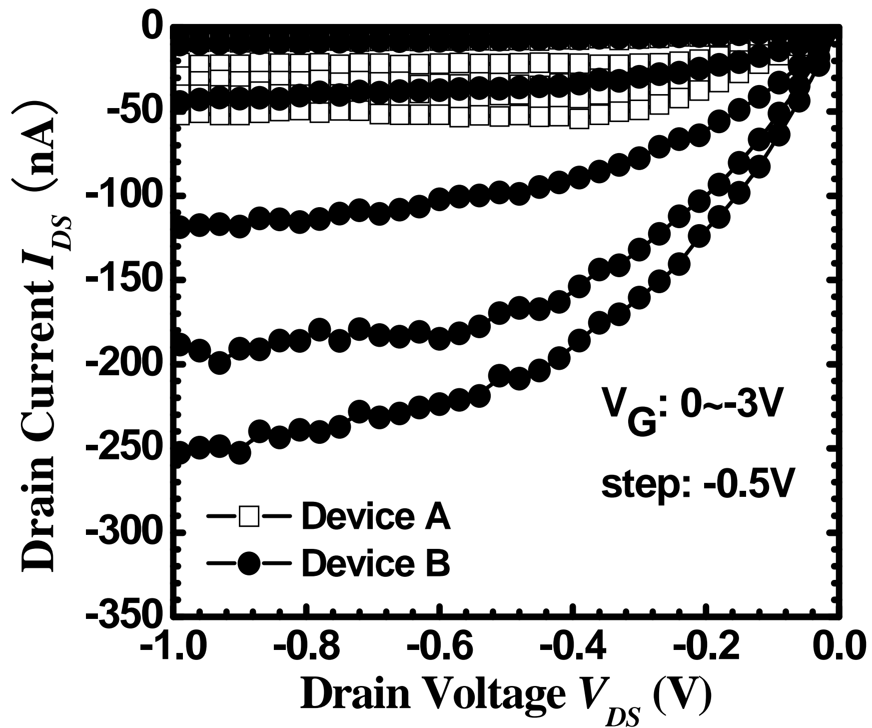


Figure 5.6: Typical I_{DS}-V_{DS} output characteristics for device A and B. VGS sweeps from 0 to -3V, step is -0.5V.

by phosphorus doped $Si_{1-x}Ge_x$ NW on 5nm thick HfO_2 gate dielectric layer. The typical transfer characteristics for both the device A and B are shown in Figure 5.5. The p-MOSFET operations are observed from the two devices. Just like SiNW MOSFET, $Si_{1-x}Ge_x$ NW MOSFETs do not show ambipolar conduction [12]. So it also indicates that high workfuntion noble metal S/D such as Pd has very obvious effect to suppress electron transport in the nanowire channel.

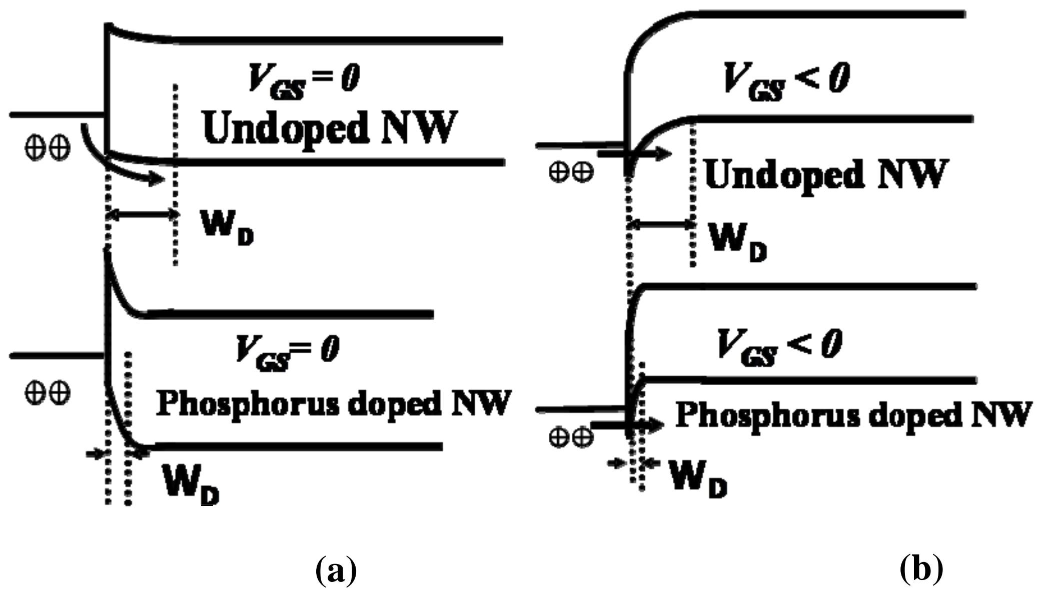


Figure 5.7 (a): Schematic graph to show the comparison of depletion width (W_D) in the band diagram of metal/$Si_{1-x}Ge_x$ NW at Source region under thermal equilibrium status. (b) Comparison of W_D in the band bending diagram of metal/$Si_{1-x}Ge_x$ NW interface at Source region under negative gate bias condition.

From the undoped $Si_{1-x}Ge_x$ NW MOSFET of device A, the on state current, I_{on} ~ 20 nA (at V_{GS} = -3V and V_{DS} =-0.1V) and transconductance, G_m ~ 0.027 μS were obtained. The dramatic increase in I_{on} ~ 100 nA and excellent on-off current ratio of I_{on}/I_{off} ~ 10^6 with suppressed I_{off} < 10^{-13} A were achieved from device B with phosphorus-doped $Si_{1-x}Ge_x$ NW MOSFET. Figure 5.6 indicates that the device B shows a huge enhanced drive current in device output performance. This remarkable

enhancement can be attributed to narrower depletion width (W_D) at the Schottky contact between metal S/D and phosphorus-doped $Si_{1-x}Ge_x$ NW. The depletion width can be expressed in

$$W\ (depletion\ width) = \sqrt{\frac{2\varepsilon_s}{qN_A}\left(V_{bi} - V - \frac{kT}{q}\right)} \quad (5\text{-}1)$$

Where ε_s is semiconductor permittivity, N_A is the acceptor impurity density in the nanowire, V_{bi} is the built-in voltage in the Schottky barrier, and V is the applied bias voltage. Clearly, under thermal equilibrium status, phosphorus-doped $Si_{1-x}Ge_x$ NW has thinner depletion width at S/D region due to the high doping concentration (N_A) [13] (Figure 5.7 (a)). When appropriate negative gate bias is applied, the barrier width of phosphorus doped $Si_{1-x}Ge_x$ NW device is also smaller than that of the undoped $Si_{1-x}Ge_x$ NW device [13]. As we discussed before, when the SB is controlling the carrier injection, the tunneling of carrier becomes critical. When negative gate bias is applied to bend up the channel band, it is easier for hole to tunnel through the thinner barrier (shown in Figure 5.7 (b)). That is the reason why doped device B has higher current than device A. Nevertheless, a degradation in subthreshold swing (S.S.) (348 mV/dec compared with 146 mV/dec for the device A) was observed. We know the S.S. can be expressed in [13]

$$S.S. = 2.3\frac{mkT}{q} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right) = 2.3\frac{kT}{q}(1 + \frac{3t_{ox}}{W_{dm}}) \quad (5\text{-}2)$$

Clearly, the W_{dm} of doped device B is decreased due to the doping concentration of the nanowire. Therefore, the degraded S.S. is due to poor gate control over doped-NW channel with thick gate dielectric. From chapter 2, we already know the dopants are easily gathered at the surface of nanowires. The interface between doped nanowire and gate dielectric has more interface charges than the interface between undoped

nanowire and same dielectric. Therefore, the charges reduce the gate field effect on the nanowire channel.

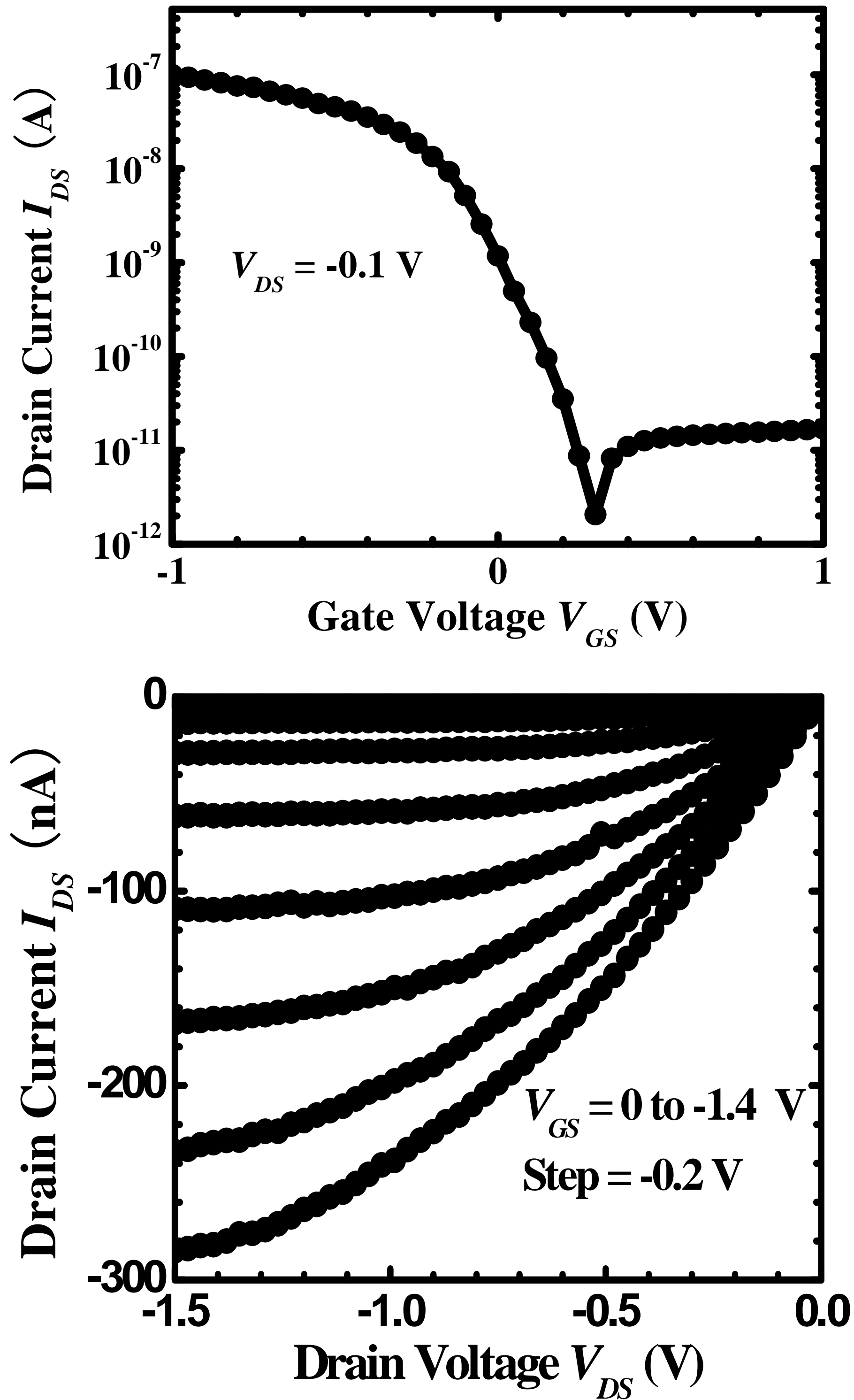


Figure 5.8: (a) Typical I_{DS}-V_{GS} transfer characteristics for phosphorus doped $Si_{1-x}Ge_x$ NW MOSFET with thinner HfO_2 dielectric layer (device C). (b) Typical I_{DS}-V_{DS} output performance of device C.

To improve the doped $Si_{1-x}Ge_x$ NW transistor performance, we try to use thinner high-κ dielectric layer to enhance the gate control. Figure 5.8 (a) and (b) show the input transfer and output characteristics of device C fabricated by using phosphorus-doped $Si_{1-x}Ge_x$ NW and ~5 nm HfO_2 gate dielectric. As expected, thinner dielectric layer gives better gate control over $Si_{1-x}Ge_x$ NW channel, resulting in S.S. ~142 mV/dec and G_m ~ 0.12 μS. In spite of a bit higher I_{off} (~10^{-11} A) due to thin gate dielectric, a good I_{on}/I_{off} ratio of ~10^4 was achieved. The improvements in I_{on} (~100 nA at V_{DS}=-0.1V, V_{GS}=-1V, which is 10% higher than that of device B under the same bias) are also observed.

Material	Undoped SiGe	n-type SiGe	n-type SiGe
Gate Elect.	HfO_2	HfO_2	HfO_2
t_{ox} (nm)	20	20	5
V_{DS}	-0.1	-0.1	-0.1
I_{on} (nA)	27	92	100
I_{on} (μA/μm)	1.38	~ 5	5
I_{on}/I_{off}	10^5	10^6	~ 10^4
S.S. (mV/dec)	164	348	142
G_m (μS)	0.027	0.05	0.12

Table 5.2 Comparison of performance parameters of different $Si_{1-x}Ge_x$ nanowire MOSFETs, (a) undoped SiGe nanowire MOSFET with 20 nm HfO_2, (b) phosphorus-doped $Si_{1-x}Ge_x$ nanowire MOSFET with 20 nm HfO_2, (c) phosphorus-doped $Si_{1-x}Ge_x$ nanowire MOSFET with 5 nm HfO_2 gate dielectric layer.

Just like discussed in chapter 4, the Schottky barrier heights of $Si_{1-x}Ge_x$ NW MOSFETs are extracted as well. Based on thermal emission model, the hole current injected from Source region to channel can be expressed as a function of barrier height [13, 14]:

$$I_{DS} = -SA^{*}T^{2}\exp(-\frac{q\phi_{Bp}}{k_{B}T}) \qquad (5\text{-}3)$$

Where S is the cross section area of NW channel, A* is the effective Richardson constant, T is the absolute temperature and Φ_{Bp} is the effective SBH for holes. Since I_{DS} is related to V_{GS}, Φ_{BH} can be extracted from transfer characteristic (I_{DS}-V_{GS}) data based on this equation. The extracted effective SBH for holes versus gate bias of the three $Si_{1-x}Ge_x$ devices are shown in Figure 5.9. This graph clearly gives us the gate bias effect on effective SBH variation for holes at source region. The real SBH can be extracted from the flatband condition at which the calculated SBH value begins to deviate from the linear fitted line of Φ_{BH} vs. V_{GS} curve (indicated in Figure 5.9). The real SBH of two doped-$Si_{1-x}Ge_x$ NW MOSFETs (device B and C) are almost the same, indicating gate oxide has negligible effect on barrier height. Undoped $Si_{1-x}Ge_x$ NW MOSFET exhibits a bit higher SBH, which is due to that equivalent as thicker barrier width for undoped $Si_{1-x}Ge_x$ NW MOSFET since tunneling mechanism needs to be considered when drain bias is applied. When further negative gate voltage is applied, tunneling current becomes more significant in carrier transport. Therefore, smaller effective SBH was reflected in the graph especially for phosphorus doped $Si_{1-x}Ge_x$ NW MOSFETs. It is observed that the slope of Φ_{BH} vs. V_{GS} curve of the device B is much smaller than those of the other two devices. This less sensitivity of SBH change also indicates the poorer gate control by thick gate oxide on doped NW channel.

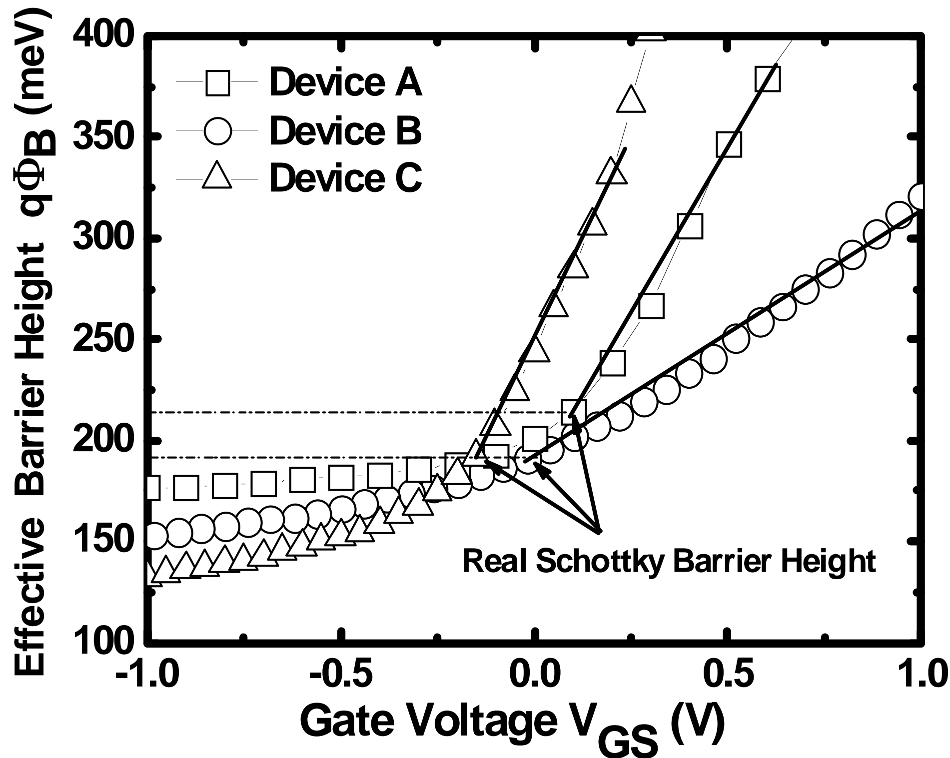


Figure 5.9 Effective Schottky barrier height as a function of V_{GS} for three $Si_{1-x}Ge_x$ MOSFETs

Compared with SiNW MOSFET performance shown in chapter 3, $Si_{1-x}Ge_x$ NW transistors have smaller I_{on} current and worse S.S.. Normally we expect higher I_{on} for $Si_{1-x}Ge_x$ NW device due to the higher mobility of $Si_{1-x}Ge_x$ NW channel. Furthermore, based on the theoretical calculation, the Schottky barrier between $Si_{1-x}Ge_x$ NW and Pd should be smaller than that between SiNW and Pd. So the low device performance is attributed to the Schottky barrier height. The possible reason is the interface between nanowire and gate dielectric. From the S.S. degradation, we already find the gate control is not good enough for $Si_{1-x}Ge_x$ NW transistor. For doped NWs, the dopants gathering at the surface makes the gate control degraded, and the carrier mobility is also degraded much more by the interface defects, traps and scattering [15].

5.4 Conclusion

$Si_{1-x}Ge_x$ NW MOSFETs were fabricated by using VLS grown bottom-up $Si_{1-x}Ge_x$ NWs with HfO_2 dielectric layer and Pd S/D. In all the $Si_{1-x}Ge_x$ NW based transistors, phosphorus-doped $Si_{1-x}Ge_x$ NW device with thinner gate oxide delivers the best performance, such as highest I_{ON} and lowest S.S, due to its thinner depletion layer and better gate control. Schottky barrier height between $Si_{1-x}Ge_x$ NW and Pd S/D is investigated to further understand the nanowire device operation. Results show that thinner depletion width can be equivalent as lower Schottky barrier height for doped NW devices, while gate oxide thickness has large effect on effective SBH since back gate modulates the SBH profile. For doped $Si_{1-x}Ge_x$ NW device, its performance is dominated by the carrier tunneling at S/D since narrower Schottky barrier. However, the $Si_{1-x}Ge_x$ NW transistor has poorer performance than the pure SiNW device due to non-optimized surface passivation and dopant scattering in the nanowire channel. This could be the future optimization plan for $Si_{1-x}Ge_x$ NW MOSFETs.

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Chapter 6

Conclusion and Future Work

6.1 Conclusion

Since late 1980s, electronics industry is dominated by the planar Si-CMOS devices. It has been possibly mainly due to the monolithic integration of complementary devices with tremendously large density and functionalities. It is also due to the scalable nature of the MOS architecture as it has been sustaining the scaling activities since its invention in early 1960s without major changes in the physical appearance. However, this planar device architecture with conventional materials is now gradually approaching the physical boundary limit. To continuously meet the scaling requirement, one has to come either with new materials such as high-κ dielectric, SiGe, or novel device structure. Recently, semiconductor nanowire is becoming a very hot topic since it can be a promising platform material for future nanoelectronic device including novel CMOS architectures. There are many methods to synthesize nanowires. One of stable and efficient way is Vapor Liquid Solid (VLS) mechanism. Mass single crystalline SiNW can be obtained quickly based on this mechanism. Successful doping process for nanowire is also achieved. Such method provides us many high quality single-crystalline nanowires in a short time span.

SiNW and $Si_{1-x}Ge_x$ NW MOSFETs integration is carried out and successful working devices are demonstrated. Our undoped SiNW MOSFET with metal S/D and

hing-κ gate dielectric delivers exciting device performance. All the fabricated devices show enhance mode transistor performance due to the schottky barrier block by the metal S/D. The noble metal provides high and thick barrier for electrons and only let holes transport under proper gate bias. After the long channel device demonstration, our efforts of short channel (65nm) SiNW MOSFET is also achieved. The Ion is improved remarkably. However, the less gate control also shows the long way to improve its device performance. Forming gas anneal is carried out to improve the metal S/D contact and reduce the barrier height. Clear drive current enhancement is observed. However, during the anneal, metal elements is diffusing and reacting with SiNW. So the annealing process control is necessary.

To further investigate the device operation, we measured the SiNW MOSFET in various temperatures. The data help us to prove that the carrier transport in the device is dominated by the schottky barrier since it blocks the carrier injection at the source region. Based on the function of gate bias and drain current, effective and real barrier height is extracted. The variation fully explains the carrier transport in the nanowire transistor.

We also investigated and improved $Si_{1-x}Ge_x$NW MOSFET performance. The doped $Si_{1-x}Ge_x$NW transistor is enhanced by integrating with thin high-k dielectric. The effective barrier height variation with gate bias is also discussed.

6.2 Future Work

Nanowire research is still in its infant development period, there are many potential challenges to overcome before it can be applied in real world.

6.2.1 Nanowire Synthesis Control

One of the key issues is the alignment during the nanowire growth. Based on this thesis and other previous reports, nanowires are grown randomly on the substrate. This is difficult for us to do the further process to make device right on the grown nanowires except for transferring them to other substrate. In this case, the nanowires are inevitably contaminated and damaged. So if we can align the nanowire during its growth or control the nanowire growth at preferred positions, it is a great breakthrough for the nanowire application. The first point is to control the distribution and size of metal catalyst. Second, we need to also control the nanowire growth direction.

There are several methods reported by scientists to align the nanowire during or after their growth. One of them is using external electrical field to guide the nanowire growth direction [1, 2]. The electrical field should be very large in a small distance otherwise it is not effective to affect the nanowire growth direction. Second method is using different precursor like $SiCl_4$ to get vertical nanowire growth. This method can etch away the sidewall of nanowire during the growth by HCl which is generated during the VLS mechanism [3]. Hence, the nanowire growth is preferably following the single crystalline direction. This method can be combined with patterned Au nano-colloids on the substrate. Therefore, the nanowire growth can be perfectly aligned on the substrate.

Another basic and urgent problem to be solved is the doping process and doping concentration measurement. As discussed in previous chapters, doping process has several ways, simultaneous doping, thermal doping and plasma doping. Each doping process has its own advantages and limitations. So the process needs further optimization. Compared with doping process, getting the picture of doping profile in

nanowire is a more challenging question. Until now, we are still lacking of accurate measurement equipment to directly detect the doping concentration of single nanowire.

6.2.2 Nanowire Device Integration

Based on nanowire synthesis improvement, the device fabrication process can also be developed. We are very interested in the carrier mobility in the nanowire channel, but the schottky barrier and extremely small size make us difficult to extract the real mobility of the nanowire channel by using conventional method. So some accurate and smart measurement is needed [4]. The interface between nanowire and gate oxide should also be improved to make sure the good gate control. Schottky barrier at the S/D region needs to be adjusted since it increases the contact resistance and block the carrier injection. The effective solution is the silicidation in the annealing process. To get device performance enhancement, vertical aligned nanowire transistors is an interesting novel device structure for future electronic application [5, 6].

6.3 Nanowire Application in Solar Cell

In chapter 1, we already realize the nanowire is not only applied in MOSFET integration, it has many other applications. Recently nano sized solar cell (or Photovoltaic device) is a very promising research area. The fossil energy is more and more expensive and will be used up in this century. Solar energy is one of the most promising candidates for future energy resources because of its advantages: inexhaustible, clean, carbon dioxide free. All the countries are looking for new energy

resources to replace conventional oil or coal. The key issue for solar cell device is always the cost-efficiency ratio. The target is fabricating devices with high energy transfer efficiency by lower cost manufacturing. Scientists developed the solar cell devices by testing different materials and device structures. So far, silicon based photovoltaic devices are still the main stream in the solar cell industry. The reasons are obvious. First, silicon is a cheap, non-toxic, almost inexhaustible material. Second, the silicon processing is much more mature than other candidates. Although silicon is an indirect band gap material [7], it has attracted much research efforts to improve silicon based photovoltaic device efficiency. Recently, silicon nanowires application in photovoltaic devices is reported by several research groups [8-11]. The main advantages of using silicon nanowire over planar are:

1. Mass production of nanowire can lower the cost
2. Large surface area to absorb incident light [11]
3. High broadband optical absorption and low reflectance are measured [12]
4. Coaxial nanowire structure improve carrier collection and overall efficiency[8]

Currently we are also beginning our process to develop working solar cell based on VLS grown Silicon nanowires. The process is described as follows: On the p-type (1×10^{15} cm^{-3}) silicon substrate, n-type nanowires are synthesized with simultaneous doping process: SiH_4: 200sccm, H_2, 200sccm, PH_3, 20sccm. The processing temperature is 575°C and growth time is 10min. After the synthesis, 1µm thick flowable oxide is covered on the nanowire sample to isolate the bottom and top contact. The pn junction is formed at the substrate-nanowire interface. The flowable oxide can be etched back by DHF to expose the n-SiNW out. The indium tin oxide (ITO) transparent film is evaporated on the sample as top contact. This process is still

under the development. In the future, coaxial nanowire structure can be further developed. Such simple process flow makes nanowire solar cell a competitive candidate for next generation photovoltaic device prototype.

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APPENDIX

List of Publications

[1]. **W.F. Yang,** S.J. Lee, G.C. Liang, R. Eswar, Z.Q. Sun, D.L. Kwong, "Temperature Dependence of Carrier Transport of Silicon Nanowire Schottky Barrier Field Effect Transistor" *IEEE Transaction on Nanotechnology*, vol 7, pp. 728-732, 2008.

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