# Investigation of the Scalability Limitations of Phase Change Random Access Memory

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# Summary

This dissertation addresses the scaling limitations of the Phase Change Random Access Memory (PCRAM) that is considered as one of the best candidates for meeting the scaling requirements for the next wave of memory technologies.

Chapter 1 establishes the background of this thesis, providing a fairly comprehensive description of memory technology and related scaling issues. This chapter proposes a new classification of the scalability limitations of PCRAM, including the lithography technology, the physical limitations of materials in PCRAM, the thermal-cross talk among memory cells and the current limitation of memory cells. Based on this classification, particular emphasis is paid to the physical limitations of the materials and the current limitation of memory cells in subsequent chapters.

The physical limitations of phase change material in PCRAM technology form the focus of Chapter 2. To thoroughly investigate this issue, a new classification of the phase change process is proposed and it includes (1) phase change in the free scale, (2) phase change sandwiched between metals/oxides and (3) reversible phase change sandwiched between metals/oxides. The limitations for phase change in $Ge_2Sb_2Te_5$ material and physical mechanisms are studied according to each category. A thermal electrical methodology is developed to simplify the three-dimension (3D) issue to a thickness-dependent problem. The results show that the limitations for reversible phase change sandwiched between metals/oxides can be considered as a physical limitation of phase change material in PCRAM technology. The possible solutions for extending this physical limitation are proposed.

In the study of physical limitations, the interface effect on crystallization was found to play an important role in ultra-small sized PCRAM technology. A systematical study on this interface-dominant nano-crystallization is presented in Chapter 3. After the

simplification of the 3D issue to the thickness-dependent crystallization issue by the methodology described in Chapter 2, crystallization kinetics including the crystallization mechanism, the corresponding activation barrier and the Avrami coefficient, were next investigated.

The limitation of current supplied to PCRAM cells, which is the subject of the subsequent chapters, refers to the high RESET current required for PCRAM cells. This would affect the scalability of PCRAM chips because a higher programming current requires bigger access transistor to supply sufficient current. In this study, superlattice-like (SLL) structure, which can reduce the current, is applied in a 128-bit PCRAM chip, which demonstrates low current and high-speed. In addition, a universal macro-model of PCRAM cells is developed for this chip's integrated circuit design. Its fabrication, based on 0.35 μm CMOS technology, also demonstrates a high degree of process compatibility. The circuit design and fabrication of this 128-bit SLL_PCRAM is described in further detail in Chapter 5 and Chapter 6, respectively.

This thesis aims at providing a useful understanding of the scalability limitations of PCRAM technology. In addition to presenting the author's findings, it is expected that this document provides useful models and methodologies for other researchers, and serves as a useful reference.

**Keywords**: Semiconductor memory, phase change random access memory, chalcogenide material, physical limitation, nucleation and growth, scaling, integrated circuit design, device fabrication, testing

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# List of Publications

**Publications in Journals:**

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3. T.C. Chong, Shi L.P, **Wei X.Q.,** Zhao R., Lee H. K., "Crystalline amorphous semiconductor superlattices", Phys. Rev. Lett., Vol. 100, pp.136101, 2008.
4. Shi, L.P., Chong, T.C., **Wei, X.Q.**, Zhao, R., Wang, W.J., Yang, H.X., Lee, H.K., Li, J.M., Yeo, N.Y., Lim, K.G., Miao, X.S., Song, W.D., "Investigation of nano-phase change for phase change random access memory", IEEE proceedings, Nonvolatile Memory Technology Symposium 2006, Vol. , 5-8, pp.76 – 80, 2006.
5. Shi, L.P., Chong, T.C., Li, J. M., Koh, S.C., Zhao, R., Yang, H. X., Tan, P.K., **Wei, X.Q.,** and Song, W. D., "Thermal modeling and simulation of nonvolatile and non-rotating phase change memory cell", IEEE proceedings, Nonvolatile Memory Technology Symposium, 2004, Vol.15-17, pp. 83 – 87, 2004.
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7. Zhao, R., Chong, T. C., Shi, L. P., Tan, P. K., Lim, K.G., Yang, H. X., Lee, H. K., Hu, X., Li, J. M., Miao, X. S., **Wei, X. Q.**, Wang, W. J., Song, W. D., "Study of geometric effect on phase change random access memory", IEEE proceedings, Nonvolatile Memory Technology Symposium, pp. 7-10, pp.110 – 114, 2005.

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2. **Wei, X.Q.,** Shi, L. P., Zhao, R., Miao, X.S., Chong, T.C., Rajan, W., Quek, B.S., "Universal HSPICE model for chalcogenide based phase change memory elements", IEEE proceedings, Nonvolatile Memory Technology Symposium 2001, Vol. 15 – 17, pp. 88 – 91, 2004.

# CHAPTER 1
# INTRODUCTION

The recent rapidly growing demand for portable and mobile products has seen an equally rapidly growing demand for nonvolatile memories (NVMs). The most popular NVM, Flash memory, is believed to face the scalability limitations below 32 nm. Therefore, new memories are being widely studied for the next generation NVM technologies. Among all emerging memories, Phase Change Random Access Memory (PCRAM) is believed to be the best candidate for the nonvolatile technology, because of its superior overall performance and good scalability. This chapter will briefly review different existing memory technologies and provide a detailed description of PCRAM technology.

## 1.1 Introduction to Semiconductor Memories

Currently, semiconductor memories constitute the most attractive segment in the global semiconductor market: they occupy one-third of the entire semiconductor market and maintain the fastest growing rate. Generally, there are two categories of semiconductor memories: volatile memories and nonvolatile memories.

Volatile memories are memories that would lose data with the interruption of power supply. The main components are Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM). DRAM is the most cost and space efficient memory because each DRAM cell consists of only one transistor and one capacitor (Lueck, et. al, 1973). DRAMs have been dominating the largest market segment of the semiconductor

memory market for more than 10 years (Databeans, 2007). The second component, SRAM, is the fastest memory with a lower standby current compared to DRAM. However, in SRAM, a single memory cell includes four or six transistors (Lage, et. al, 1996), resulting in a very low chip density and relatively high cost. For a long time, SRAM had been ranked the second in the semiconductor memory market; however, its market already shrank to the third largest due to the fast development of NVM (Databeans, 2007).

The dominant technologies for NVM include EEPROM and Flash memory, which can store the data at least for 10 years, even when the power supply is disturbed. EEPROM is electrically-erasable-and-programmable (Mukherjee, et. al, 1985). The device programmer writes data to the device one bit at a time by applying an electrical charge to the input pins of the chip. Any byte within an EEPROM may be erased and rewritten. From a software viewpoint, Flash and EEPROM technologies are very similar. The major difference is that Flash devices can only be erased one sector at a time, not bit-by-bit.

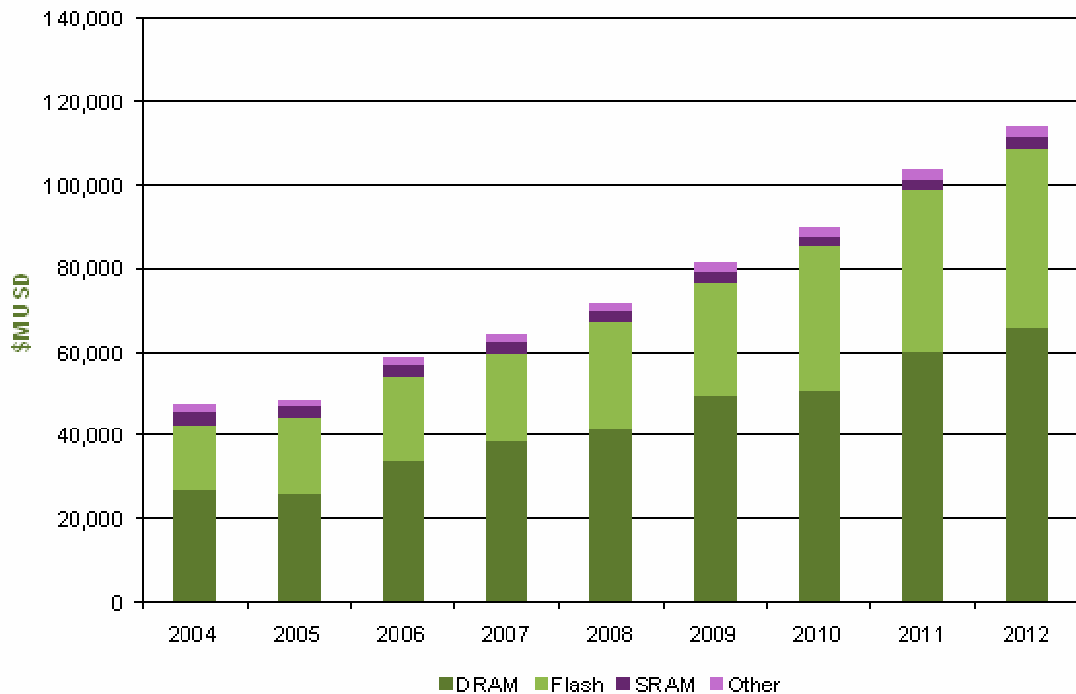



Fig. 1. 1 Forecast of the semiconductor memory market by Databeans Inc.

Flash memory combines the best features of the memory devices described thus far. Since 1999, it has exceeded SRAM, occupying the second largest segment of the market for semiconductor memories. It is projected to be in top position in the 2010s (Databeans, 2007), according to Fig. 1.1. The conventional structure of a Flash memory is shown in Fig. 1.2 (a), in which the cell consists of a Metal-Oxide-Semiconductor (MOS) transistor, which has an additional floating gate between the channel and the control gate. The programming of cells is realized by channel hot electrons within a programming time of 1-10 μs. However, a high programming current is required because of low efficiency of hot electron injection. Erasing is realized by Fowler-Nordheim (FN) tunneling, while recently it has become common for erasing to be carried out by tunneling to the source junction of the transistor. This leads to smaller possible channel lengths and therefore the

better scalability of the cells (Keeney, 2001).

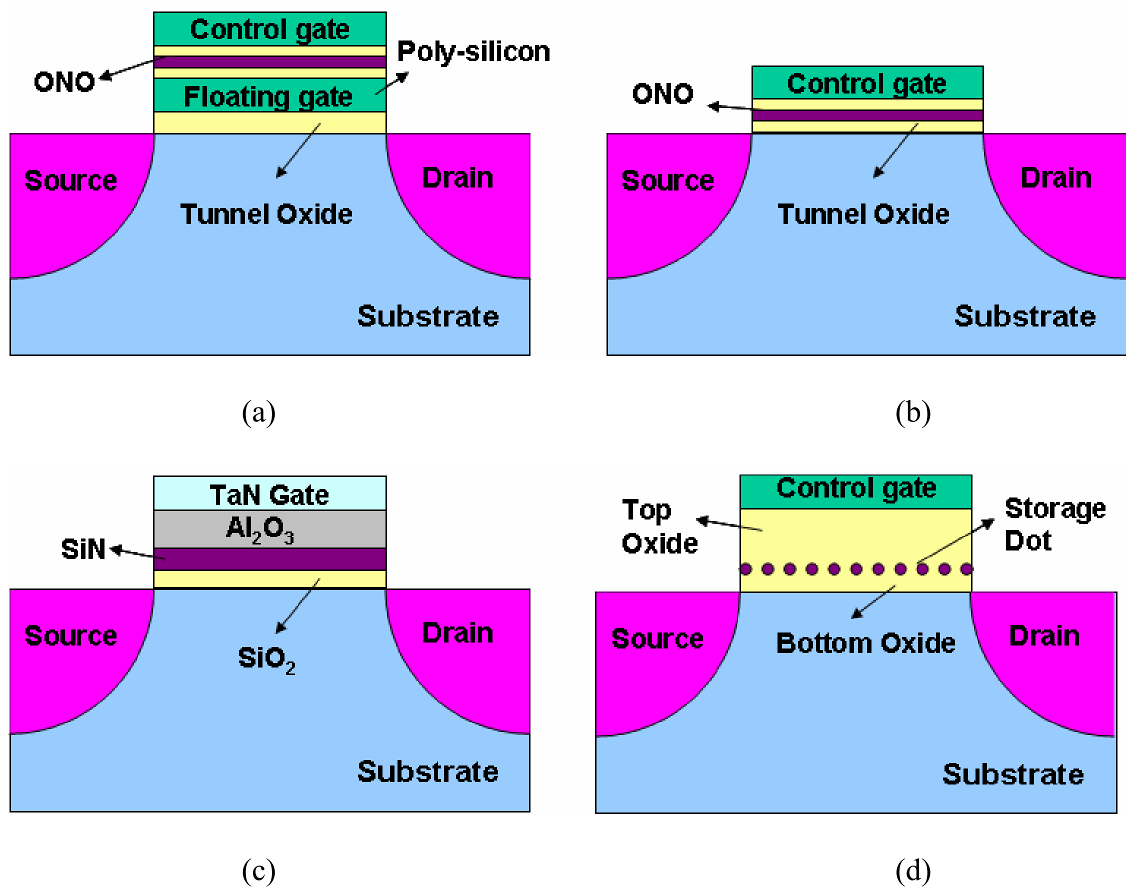



Fig. 1. 2 Schematic structure of (a) conventional Flash cell, (b) SONOS, (c) TANOS and (d) nano-crystal Flash cell.

Although demand for Flash memory is experiencing fast growth, it is not an entirely ideal option because of (1) its relatively long programming time of 1 μs - 1 ms (She, 2003); (2) limited cycle endurance at smaller than $10^6$ (Cappelletti, 1994); and, (3) especially its scaling limitation below 45 nm or 32 nm node (Roberto, 2004). The scaling limitation is due to the tunneling of electron through the floating gate, which would cause the data lost. Although the direct tunneling, preventing the ten-year retention time, occurs at 6-7 nm, stress induced leakage current push the tunnel thickness limit to no less than 8-

9 nm. Moreover, the effective width reduction could be limited by the read current reduction, then impacting the access time (Bez, et.al, 2003). Advanced technologies, such as SONOS (silicon-oxide-nitride-oxide-silicon), TANOS (Si-Oxide-SiN-$Al_2O_3$-TaN), nano-crystal and FinFETs, were proposed to extend the limitation.

Based on the fact that silicon nitride contains intrinsic defects that trap charges, SONOS uses silicon nitrite to replace the silicon used to build a memory cell's floating gate structure as shown in Fig. 1.2 (b). It helps to reduce the thickness of gate from about 1000 angstroms to as small as 100 angstroms - thus allowing it to reduce the size and voltage requirements of Flash cells without taking a hit in performance and reliability (White, et. al, 2000). However with thin tunneling oxide (2-3 nm) the stored charge induces a moderate electric field that is sufficient to cause substrate hole direct tunneling. There is also evidence that electron may tunnel from the nitride trap to the Si/$SiO_2$ interface trap. Thus, data retention is difficult to achieve both from charge loss and from direct hole tunneling (Lu, et. al, 2006).

To solve the problem addressed above in SONOS, high-k blocking oxide ($Al_2O_3$) and TaN gate with high work function are adopted to make a thicker tunneling oxide possible (Shin, et. al, 2005). TANOS (Park, et. al, 2006) is essentially a non-floating gate NAND SONOS. As shown in Fig. 1.2 (c), structure consists of tantalum (metal), aluminum oxide (high k material), nitride, oxide and silicon. However, the data retention is still an issue when the device keeps being scaled. In addition, as MOS devices are scaled, atomic level effects will become increasingly important. Thus, a number of sources of variation become increasingly important.

Another approach, which has been heavily investigated to break the scaling constrains

set by the tunnel oxide thickness, is the nano-crystal device as shown in Fig. 1.2 (d). It breaks up the floating gate into many nano-crystals of polysilicon (or metal) in a floating gate device (Muralidhar, 2003; Salvo, 2003). Electrons are trapped into silicon nano-crystals, which can help to greatly reduce charge leakage through localized oxide defects. Hence the floating gate structures can be built with much thinner tunneling oxide layers, indicating a better scalability. Another major benefit of the nano-floating gate approach is the improved reliability. However, some concerns still remain about the low threshold voltage shift, data retention capabilities, and the intrinsic scalability of nano-crystals.

Recently, FinFET SONOS Flash memory was proposed for embedded application (Xuan, et. al. 2003). FinFET concept is a double-gate device proposed to suppress short-channel effects for sub-100nm CMOS technologies in 1999 (Huang, et. al, 1999). It attracts great interests because of its quasi-parallel structure and relatively simple fabrication process, which helps to reduce the gate length to 10 nm (Yu, et. al, 2002). The combination of FinFET and SONOS is expected to extend the scaling limitation of Flash memory to 22 nm.

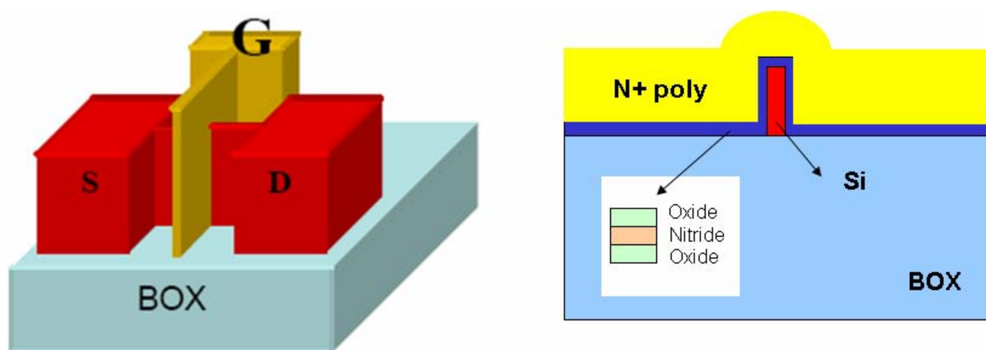



Fig. 1. 3 (a) Three dimension view of a FinFET memory device (b) the cross-sectional view shows that the N+ poly gate surrounds the ONO stack that is deposited on the two sidewalls and the top surface of the surface Fin.

Beyond 22 nm, the intrinsic limitation of electron tunneling, which reduces the data retention, remains to be the problem for Flash memory technology. Going beyond nano-crystals, in order to offer better performance and scalability, new materials and alternative memory concepts than charge-based storage are mandatory to boost the NVM industry. Generally, three technologies have been widely investigated: Magnetoelectric Random Access Memory (MRAM), Ferroelectric Random Access Memory (FeRAM), and PCRAM (Bez, 2004).

FeRAM has a sandwich structure shown in Fig. 1.4 (a), in which ferroelectric material can be polarized spontaneously by an electrical field. The polarization occurs as a lattice deformation of the cubic form, corresponding to a hysteresis loop, shown in Fig. 1.4 (b). In TbOsZnPt, the most popular ferroelectric material, the Ti atom can be moved by an electric field into two stable positions, inducing two different charges across the ferroelectric capacitor. The difference between the two charges is used to store data. Furthermore, the deformation is permanent unless a high writing voltage is applied to change it. This technology has a quick writing speed and low cost, and a much larger read signal (Jung, 1999). However, the read endurance (electric fatigue) is low and the programming voltage is high.

In contrast to FeRAM, MRAM cell comprises a transistor and a resistor 1T/1R (Durlam, 2003), rather than a capacitor. It can be seen in Fig. 1.5, that the adoption of a tunnel junction is coupled to magneto-resistive materials that exhibit changes in the electric resistance when a magnetic field is applied. The main advantages of this technology are its fast writing speed, well-understood material, and low voltage writing. Moreover, the structure is radiation-hard with an unlimited read/write endurance, which

makes an MRAM suitable for write intensive storage applications. However, its main problems include a high writing current, a small read signal and difficult process integration with CMOS.

Despite the previously mentioned issues, another major challenge for MRAM and FeRAM is the scalability, which is critical to maximize the capacity of the memory chip in the limited space. For FeRAM, the potential limitation is due to the superparaelectric limit. Although, theoretically and experimentally, films made from ferroelectric oxides keep their ferroelectric properties to thickness as low as 2 to 3 nm. Lateral scaling is limited to the size above approximately 20 nm (Zschench, et. al, 2005). High current used to write the device is the limiting factor for the scaling of MRAM. This high current is due to the intrinsic requirement of the magneto-resistive materials (Tehrani, et. al, 1999). Compared to FeRAM and MRAM, the phase change material showed the best scalability. It is believed to be the technology that can lead the NVM technology to 20 nm and below.

Besides the good scalability, the PCRAM is also superior in speed, stability and density. Therefore, it is the best candidate for covering different NVM application fields, matching both high density as well as high performance specifications. The comparison among different NVM technologies is shown in Table 1.1. The PCRAM has shown predominant advantages in scaling and multilevel storage capabilities. This technology, which exploits thermally reversible phase transitions of chalcogenide alloys to store data, will be introduced in detail in the following section.

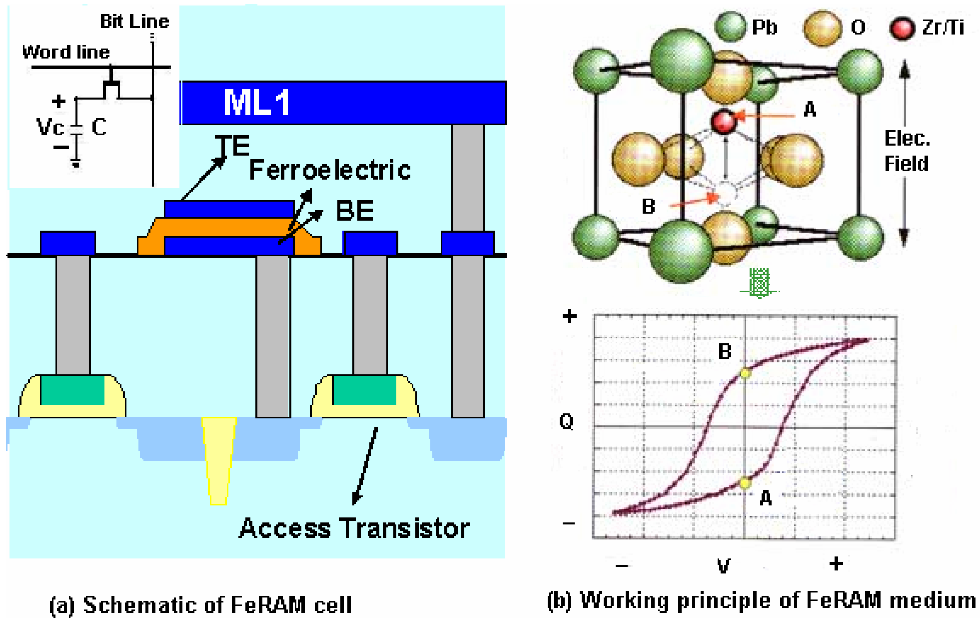



Fig. 1. 4 The schematic structure and working principles of FeRAM cells.

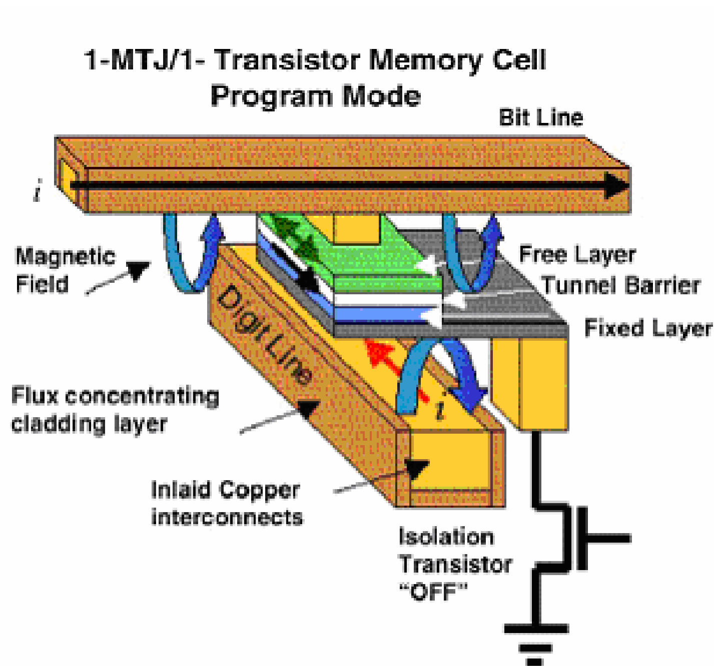



Fig. 1. 5 MRAM cell in the Magnetic Tunnel Junctions 1-MJT /1-transistor option, schematically showing the programming operation mode.

Table 1.1 Performance comparison between volatile memory (DRAM and SRAM) and NVM (Flash, FeRAM, MRAM and PCRAM) devices.

| Memory Type | DRAM | SRAM | Flash-NOR | Flash-NAND | FeRAM | MRAM | PCRAM |
|---|---|---|---|---|---|---|---|
| Cell size factor($F^2$) | 6 – 12 | 90 - 150 | 8- 10 | **4** | 18 | 10-20 | **4-8** |
| Volatility | Volatile | Volatile | **NV** | **NV** | **NV** | **NV** | **NV** |
| Endurance write/read | ∞ /∞ | ∞ / ∞ | $10^6$ / ∞ | $10^6$ / ∞ | $10^{12}$/$10^{12}$ | $10^{14}$ / ∞ | $10^{12}$ / ∞ |
| Read | Destructive | Partially-destructive | **Non-destructive** | **Non-destructive** | Destructive | **Non-destructive** | **Non-destructive** |
| Read/ Program Voltage | ~ 1 | ~ 1 | 2/ 10 | 2/ 18 | 1.5/ 1.5 | 3.3/ 3.3 | **0.4/ 1** |
| Program/ Erase/ Read speed, ns | 50/ 50/ 8 | **8/ 8/ 8** | 1us/ 1-100ms (block)/ 60 ns | 1 ms/ 1-100ms/ 60 ns | 80/ 80/ 80 | 30/ 30/ 30 | 50/ 50/ 50 |
| Direct over-write | **Yes** | **Yes** | No | No | **Yes** | **Yes** | **Yes** |
| Bit/byte Write/ Erase | **Yes** | **Yes** | **Yes** | Block erase | **Yes** | **Yes** | **Yes** |
| Read dynamic range (margin) | 100-200mV | 100- 200mV | Delta current | Delta current | 100-200mV | 10-40%R | **100XR** |
| Programming energy | Medium | Medium | High | **Low** | Medium | Medium | **Low** |
| Transistor | Low performance | **High performance** | High voltage | High voltage | Low performance | **High performance** | **High performance** |
| CMOS logic compatibility | Bad | **Good** | Ok, but High V need | Ok, but High V need | Ok, but High V need | OK | **Good** |
| New material | Yes | No | No | No | Yes | Yes | Yes |
| Scalability limit | Capacitor | 6T/ 4T | Tunnel oxide/ HV | Tunnel oxide/ HV | Polarizable capacitor | Current density | **Lithography?** |
| SER susceptibility | Yes | Yes | **No** | **No** | Yes | **No** | **No** |
| Relative cost per bit | **Low** | High | Medium | Medium | High | Medium | **Low** |

*Cells highlighted in yellow are the superior properties among all memories listed above

## 1.2 Phase Change Random Access Memory

### 1.2.1 Electrical Switching in Chalcogenide Glasses

Studies on the electrical switching in chalcogenide glasses were started in the 1960s (Ovshinsky, 1968). Currently, it is widely used in different technologies, such as sensors

and semiconductor memories. It has been a common practice to separate the switching into two classes according to whether the high resistance amorphous state can be resuscitated after the low resistance state has been maintained for a given length of time. The first type, threshold switching, is a field-assisted transition, which makes an amorphous semiconductor switch from a highly resistive to a conductive state when a threshold voltage is reached. Once the amorphous resistivity drops, the current flowing through the device may heat up the device and lead to a second reversible transformation, called memory switching, corresponding to the phase change transition from the amorphous to the crystalline state.

Threshold switching was firstly discovered by Ovshinsky in 1959 (Ovshinsky, 1959). He succeeded in making a switch based on a tantalum film, which had an amorphous layer of tantalum oxide about 900 Å thick. Switching occurred when the film was sufficiently polarized. It is characterized by a snap-back effect in a IV curve and largely reduced resistance after switching as shown in Fig. 1.6. However, the low resistance conduction state needs to be maintained by a sustaining current. Since this state is reached when a threshold voltage is achieved, it is called threshold switching.

Both the physical mechanism and the nature of threshold switching have been debated for years. However, recently, Redaelli, et al investigated threshold switching in amorphous chalcogenide materials through modeling and experiments (Redaelli, 2004). Their numerical simulation provides a quantitative description of the current-voltage curve of the $Ge_2Sb_2Te_5$ resistor, which is in close agreement with measurements performed on test devices. Their experimental data demonstrated the electronic nature. The physical mechanisms responsible for switching to the highly conductive state are

discussed in their paper. At equilibrium state, the conductivity of $Ge_2Sb_2Te_5$ is p type with the lone-pair band located near the valence band edge and extending for a bout 200meV. At low voltages, electron recombination takes place and quasi-Fermi levels remain close to their equilibrium positions. Structural defects along the Te-Te chains in the amorphous $Ge_2Sb_2Te_5$ giving a high density of donor/acceptor defect pairs. As the voltage across the cell increases, so do the carrier densities, the electron generation rate will be exponentially increased. As the bias rises, it is more and more difficult for the recombination to balance generation. The critical point is reached at $V_{th}$. Increasing the bias above $V_{th}$, the electron recombination rate can not balance the generation anymore, and the only way to reach a new steady state condition is to decrease the voltage drop across the device, thus to reduce the generation rate. In this case, the generated carriers have filled all the traps, the electron quasi-Fermi level moves close to the conduction band, thus increasing the free electron carrier concentration and reducing the material resistivity. The electron generation is therefore mainly sustained by the high free carrier concentration, when the voltage drops, the electronic switching snap-back takes place.

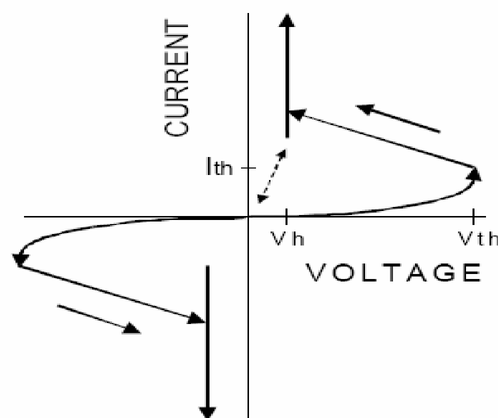



Fig. 1. 6 Electrical threshold switch in phase change material.

Different from threshold switching, the memory switching does not require a sustaining current because the resistance drop during memory switching is caused by a change in the material's atomic structure (Fig. 1.7). These different atomic structures have different physical properties, such as electrical conductivity. Relative to the amorphous state, the crystalline state has a lower resistance. It was initially obtained by the use of a suitable metalized electrode. The result was demonstrated at a lecture given at the Detroit Physiological Society Meeting in the 1959 (Ovshinsky, 1959). A pulse of one polarity set the memory, and a pulse of different amplitude or opposite polarity shut it off. Consequently, the devices can remain indefinitely in either the ON or OFF states without any need for sustaining energy input. The ON state (low resistance) is normally the crystalline state with an ordered atomic structure, while the OFF state (high resistance) is normally the amorphous state with a disordered atomic structure. Generally speaking, the basic difference between two kinds of electrical switching is whether the atomic structure is changed during the switching.

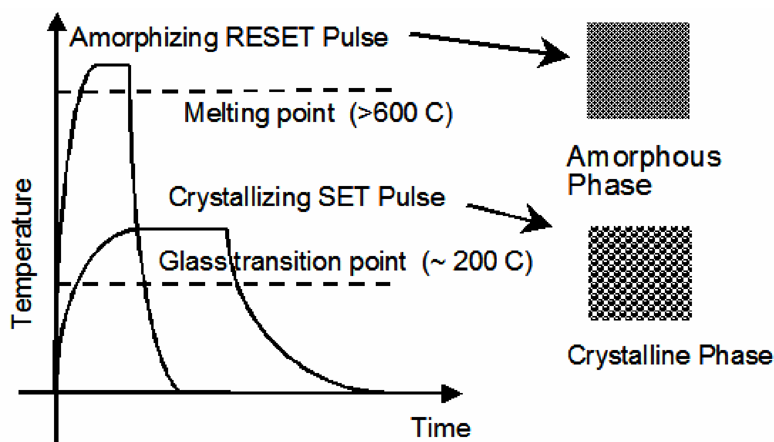



Fig. 1. 7 Phase change process of the chalcogenide material.

### 1.2.2 Principles of PCRAM

The most prominent use of electrical switching is PCRAM technology that is based on a rapid reversible phase change effect in chalcogenide glasses. The most commonly used phase change material is Germanium-Antimony-Tellurium (GeSbTe) alloy, which belongs to the same material family used in optical re-writable discs. During the operation, phase change material changes between its amorphous and crystalline states by electrical pulses. The rapid and reversible structural change results in a change in material resistivity. The transition from the low conductive amorphous state to the high conductive crystalline state is generally referred to as SET, while the transition from the high conductive crystalline state to the low conductive amorphous state is referred as RESET. The small volume of phase change material in the active region acts as a programmable resistor. Its high and low resistances are measured and recorded as data "0" and "1".

To switch to the amorphous state, a short and high RESET current pulse increases the temperature to above melting temperature. After the pulse, the molten state cools rapidly ($10^9$ K/s) and is quenched into the amorphous state. To convert the material back into the crystalline state, a long and low SET current pulse is used to heat the material to above its crystallization temperature (but below its melting temperature). The duration for the SET pulse should be longer than that required by the material-dependent crystallization. A much lower current with little Joule heat is used for reading the cell. The electrical properties of PCRAM are shown in Figure 1.8. In view of the high amorphous resistance, one would expect to need very long SET voltage pulses to dissipate enough energy to induce the crystallization. Therefore, it is critical that the phase-change material is able to conduct 'threshold switching'. This means that when the electric field over the

amorphous volume exceeds the threshold field, highly conductive filaments are formed within the amorphous material. Based on these filaments, Joule heat will be rapidly generated, inducing the desired phase transition at relatively low voltages.

PCRAM cells can be programmed to intermediate resistance values that can be used for multi-state data storage. Since the energy required for phase transformation decreases with cell size, the write current scales with cell size, thus facilitating memory scaling. PCRAM devices have fast access time, long endurance, and good data retention.

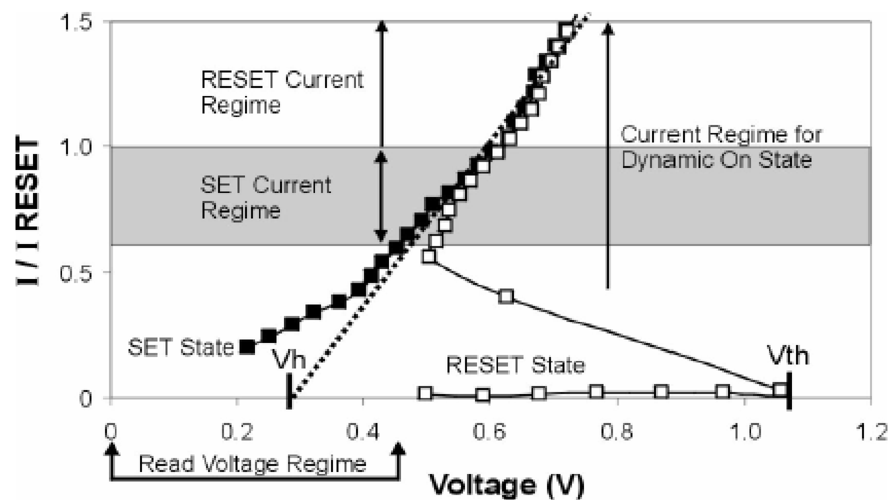



Fig. 1. 8 Electrical properties of PCRAM devices.

The most popular structures of PCRAM memory cells are shown in Fig.1.9. The conventional structure shown in Fig. 1.9 (a) is vertical type. The phase change material is sandwiched between two metal electrodes. Electrical pulses are applied to provide the energy for the crystallization and amorphizing processes. Rather than taking place in the whole phase change film, the phase change only occurs in the active region, which is defined by the area of the bottom electrode. Because of the ultra small contact interface

between the phase change material and bottom electrode, there is a very high current density in the active region, which acts as a programmable resistor.

A recent advanced line-type PCRAM structure as shown in Fig. 1.9 (b) has attracted great interest (Lankhorst et.al, 2005). This line-type PCRAM has an ultra-thin line of phase change material surrounded by a dielectric ($SiO_2$). An electric current is used to heat the material to its phase-change temperature, where it switches reversibly between the crystalline and amorphous phases. This structure has three advantages (Wuttig, 2005). Firstly, it allows the removal of the electrodes from the active region, hence the constraints on the thermal stability of electrode does not exist any more. Secondly, because the active region is surrounded by the dielectric, which has a lower thermal conductivity, this line-type PCRAM dissipates less power and current. Thirdly, the fabrication is with less additional lithography steps compared to vertical structure. However, the ultra-thin films used in line-type PCRAM may bring the problems to the device reliability when the high speed and large overwrite cycle are required by certain application.

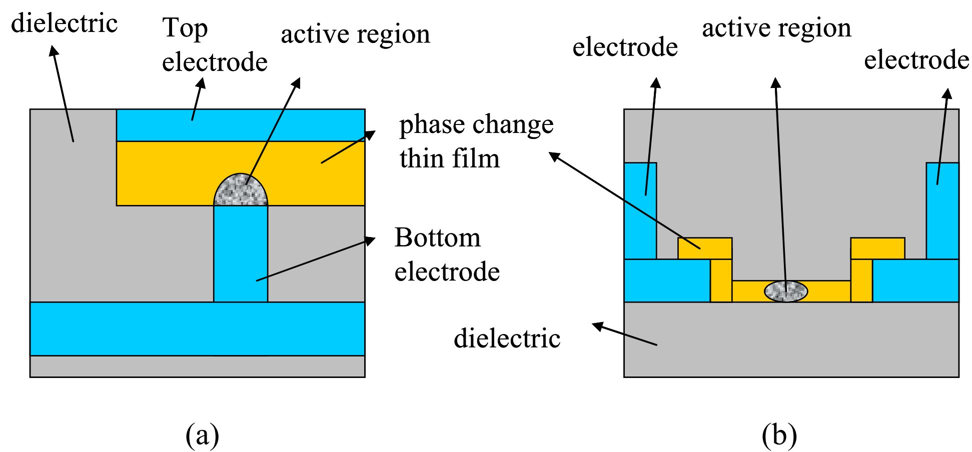



Fig. 1. 9 Vertical (a) and line-type (b) PCRAM memory cells.

### 1.2.3 Studies on PCRAM Technology

The early studies on PCRAM technology between 1960s and 1980s mostly focused on the physical nature of the threshold switch. Many researchers supported the idea that threshold switch was essentially a thermal effect (Popescu, 1975; Owen, et.al, 1979). Later, Adler's model suggested that the generation of the carrier, which was driven by an electrical field, induced the switching (Adler, et.al, 1978, 1980). More recently, a break-through was made through modeling and experiments based on Adler's research (Pirovano, et.al, 2004). It was reported that, during process, carrier concentration competed with a strong Shockley–Hall–Read (SHR) recombination via localized states was proven by the modeling and experiments.

With regards to memory switching, the investigation of physical mechanisms and models mainly began in 1990s. This was followed by the thorough exploration of the crystallization behavior of chalcogenide material and the crystalline structures (Jeong, et.al, 1999; Senkader and Wright, 2003; Alexander, 2004). Two crystalline phases: Face-Center-Cubic (fcc) and Hexagonal-Closed-Packed (hcp), were reported to exist in the GeSbTe material. In fact, it was postulated that fcc is the dominant phase in PCRAM because with an anealing rate around $10^9$ °C/s generated by nano-second electrical pulses, only the amorphous to fcc transformation is allowed (Chiang, 1999).

In 1990s, with the great success of optical discs based on the use of chalcogenide materials and the intense need from portable electronic device markets, PCRAM became a hot topic again. Researchers became eager to change this technology from single memory cell to embedded/stand-alone memory chips (Tyson, et.al, 2000; Lai and Lowery, 2001; Takaura, et.al, 2006; Bedeschi, et. al, 2004; Ahn, et. al, 2004). Based on the

development of memory chips, reliability (Pirovano, et.al, 2004), process compatibility (Hwang, et.al, 2003) and scalability (Pirovano, 2003) became the topics for PCRAM researchers. Most recently, more innovative PCRAM ideas have emerged; one example is the lateral phase change memory cell, which can be programmed by both optical and electrical pulses (Brian, 2007). In addition, it was found that the structural phase of gallium nanoparticles could be switched by optical excitation and read via their cathodoluminescence (CL) when excited by a scanning electron beam (Denisyuk, et. al, 2007). At the same time, reports have been published on conventional material engineering for the PCRAM technology (Feng, et. al, 2007; Byoung, et.al. 2007), device engineering (Rao, et. al, 2007) and multilevel storage application (Rao, et. al, 2007; Dong, et. al, 2007) were also reported.

As the basis for memory technology, the development of innovative phase change memory cells is still the focus for researchers. The material engineering has been the most important approach. Doping of Bismuth (Yeo, et. al, 2006), Nitrogen (Horii, 2003; Seo, 2000), Oxygen (Matsuzaki, et.al, 2005) and Si (Feng, et. al, 2007) into the chalcogenide materials has been found to be helpful in reducing programming current and enhancing reliability. Studies on the better performance of other materials, such as Superlattice-like phase change structure (Chong, et.al., 2002), AgInSbTe (Iwasaki, et.al, 1992), GeTeAsSi (Bunton, 1973), GeTeBi (Bhatia, 1995), GeSbCu/Ag (Ramesh, 1999), GeTeAs (Tsendin, 2001), In-Te (Rajesh, 2003), AsSbTe (Nakayama, 1993), SeSbTe (Nakayama, 2003), PbGeSb (Saheb, 2003), SnGeSbTe (Song, et.al., 2007) have also been undertaken. Recently, after finding the criterion facilitates the search for new phase change materials (Welnic, et. al., 2006), Wuttig took a big step towards the ability to

design novel phase-change materials (Wuttig and Yamada, 2007; Wuttig, et.al., 2006). Phase change magnetic material is also proposed for wider application (Shi, et. al., 2007). Engineering of device structure has been proposed to another important approach. Ring-type contact (Chang, et. al, 2005) helped to improve the reliability. Edge contact (Ha, et.al, 2003) has been reported to reduce the programming current. In addition, trench structure (Pellizzer, et.al, 2004) has been proposed to optimize array density and cell performance. Another proposal was for the inclusion of an additional tungsten heater (Takaura, et.al, 2003) for low-power, high stable and short-read-cycle operations.

## 1.3 New Classification of Scaling Limitation of PCRAM

Lithography technology had been believed to be a scaling limitation for the PCRAM technology for years (Lai, 2001). However, with fast development of advanced lithography technologies, the transistor and device size could reach 20 nm and below. At such a small space, the limitations due to the nano-effect in the materials will become more and more important. First of all, the phase change happens between amorphous state and crystalline state: the former one is short-range ordered, long-range disordered, while the latter one is both short-range and long-range ordered. When the memory cell shrank to the atomic short-range of the phase change material, which is few nanometers, the structural difference between amorphous state and crystalline state becomes unobvious, then further affect the data storage of PCRAM devices. Secondly, various nano-effects, both in the phase change material or at the interface of the devices, would affect the device performance when the memory cell size reaches nano-scale. Therefore, the more broad study of scalability limitations in PCRAM, especially at nano-scale, are

necessary. The scaling limitations for PCRAM include four categories and can be defined as (1) lithography technology, (2) physical limitation of phase change materials in PCRAM, (3) thermal-cross talk among memory cells and (4) current limitation of memory cells.

Although semiconductor lithography was developed in 1960s, the basic equations governing the imaging process have been known for about a century. The resolution of any optical tool is limited by the wavelength of the light source and the numerical aperture of optical lens. It was believed that the lithography technology faced great challenges below 32 nm because of wavelength limitations (Hirose, et al., 2002). Ultra-violet, deep ultra-violet, extreme ultra-violet, electron beam and X-ray are believed to be the alternative technologies for optical lithography (Ito and Okazaki, 2000). Besides the optical approaches, immense lens (Kunz, et.al, 2003), nano-printing (Zhao, et.al, 1997) and near-field optical microscopy (Wang, et.al, 2005) are emerging to reduce the critical size.

Physical limitation of phase change materials in PCRAM refers to the limitation directly caused by certain physical mechanisms that disable the expected phase change in PCRAM devices. A good example is the minimum size requirement on critical nucleus, below which, the crystallization would not happen. However, before scaling to the size of critical nucleus, phase change material would face other limitations caused by the diffusion, stress or phase separation. Till now, to the best of our knowledge few researches were on this topic. Some studies do note that the crystallization would be different in ultra-thin films (Martens, et.al, 2004; Miao, et.al, 1999; Raoux, et.al, 2006). But the minimum size at which phase change material would not function in typical

PCRAM operation is still an open issue. This thesis aims to focus on this topic in chapter 2 and 3.

Thermal cross talk refers to the thermal disturbance among adjacent memory cells. Because memory switching can be induced thermally, thus the heat dissipated from adjacent cells could cause the data to be lost. As shown in Fig. 1.10, when the distance of adjacent cells is big enough, the heat dispersed from neighboring memory cells would not accumulate enough to affect stored data. However, with the increase of memory array density, the heat profile would overlap seriously, and it might change the phase of the phase change material in the center cell and change the data. Simulation studies have shown that below 65 nm, thermal cross talk would not affect the data retention time of PCRAM cells (Pirovano, 2003; Lai, 2003).

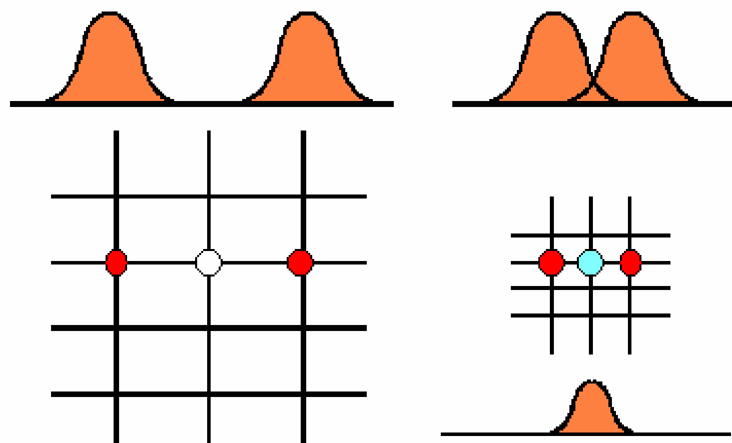


Fig. 1. 10 Thermal cross talk in the PCRAM when the density of memory array increases.

Current limitation refers to the relatively high RESET current in PCRAM memory cells. High programming current can increase the power consumption and reduce the

memory density. Because every single memory cell needs a transistor as the selective element, which can support 1 mA reset current should occupy a very large area (Fig. 1.11). For instance, the maximum current controlled by the smallest transistor at 0.35 μm technology node is only around 140 μA (Tyson, et al., 2000). Material engineering, such as nitrogen doping introduced previously, is a way to reduce the current. Device engineering, edge contact (Ha, et.al, 2003) was also proposed to minimize the programming area (Fig. 1.12), thus reducing the RESET current (Fig. 1.13). However, the contact of the bottom electrode edge was not satisfactory for reliable and long-cycle programming.

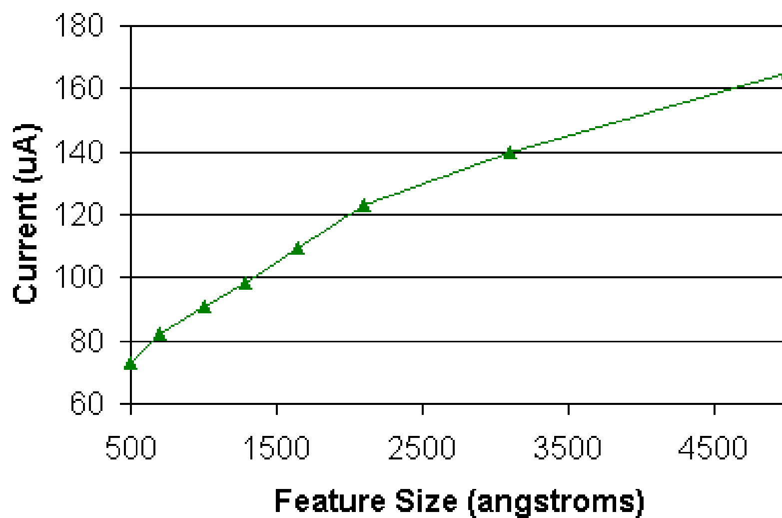



Fig. 1. 11 Maximum current by a minimum size MOS transistor.

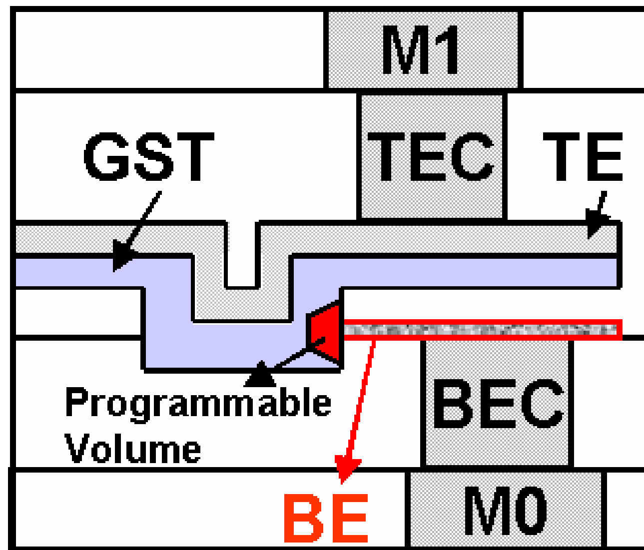



Fig. 1. 12 Edge contact phase change memory cells (Ha, 2003).

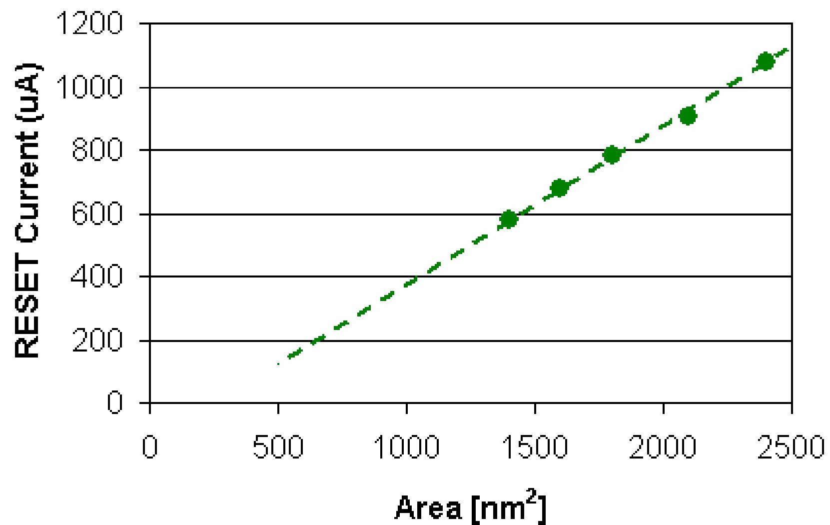



Fig. 1. 13 RESET current scaling with the contact area scaling of a single PCRAM memory cell.

## 1.4 Objectives

This thesis aims to study the scalability limitations of PCRAM. In the previous

sections, four kinds of limitations for PCRAM scaling were proposed: lithography technology, physical limitation of phase change materials, thermal-cross talk among memory cells and current limitation of PCRAM cells. Because lithography and thermal cross talk has been widely studied by researchers from different area and achieved great progress, this work would mainly focus on the other two limitations, physical limitation of phase change material and current limitation of PCRAM cells. Their root causes are to be studied by the research on materials and on device structure engineering. The solutions for extending these limitations will also be provided.

The objectives of this thesis are listed below:

(1) Studying the physical limitation of phase change material in PCRAM based on proposed classification and providing solutions for extending these limitations

(2) Investigating the thickness dependent nano-crystallization of phase change materials limited by interfaces and its effects on the PCRAM performance

(3) Exploring advanced phase change material structures to reduce the current

## 1.5 Organization

To investigate the scaling limitations of PCRAM technology, this thesis elaborates on the physical limitation of the phase change materials and the current limitation of memory cells, based on the previously proposed classification.

Chapter 2 focuses on exploring the physical limitation of phase change material in PCRAM technology. To provide a comprehensive analysis of the limitation, three categories of phase change processes are proposed. Theoretical and experimental researches in different categories are carried out. Additionally, the solutions for extending

physical limitation are explored. In the study of physical limitation in ultra-small size PCRAM cells (2-3 nm), a thermal electrical method is developed to simplify this 3D problem to thickness-dependent issue, which is only considered at thickness direction, to simplify the experiments simple and with efficiency.

The research in Chapter 2 proves that the interfaces have great effects on the crystallization process. Hence Chapter 3 focuses on the interface-affected nano-crystallization. The in-situ thermal electrical measurement developed in the Chapter 2 is used to study the crystallization in ultra-thin films to prove that it is thickness dependent. Kinetics, including the crystallization mechanism, the corresponding activation barrier and the Avrami coefficient are investigated in Chapter 3.

In Chapter 4, an advanced material structure, known as the superlattice-like (SLL) phase change material structure is explored in details. The electrical, crystallization and thermal properties are studies based on different artificial structures.

To demonstrate the performance of SLL structure at chip level, the development of a 128-bit SLL_PCRAM is to be discussed in Chapter 5 and 6. Chapter 5 introduces the integrated circuit design, while Chapter 6 presents the fabrication and testing of this design. Finally, the current reduction capability and the superior performance of 128-bit SLL_PCRAM will be demonstrated.

Chapter 5 also introduces the development of the macromodeling of a PCRAM memory cell into the integrated circuit design. Furthermore, it provides a description of the circuit of the SLL_PCRAM chip, such as the architecture, blocks, simulation and layout.

In Chapter 6, both conventional $Ge_2Sb_2Te_5$ and SLL structure PCRAM are fabricated

for comparison. These chips are tested on a self-developed testing bench to measure the electrical properties, stability, W/R cycles and other memory characteristic parameters. It aims to show that a SLL structure PCRAM has the advantages of low current and good overall performance.

Chapter 7 summarizes the research findings of this dissertation, ranging from the study of basic material to stand-alone chip development. The results in this dissertation should provide a reference on for the study of scalability of PCRAM technology.

# CHAPTER 2
# PHYSICAL LIMITATION OF PHASE CHANGE MATERIALS IN PCRAM

Physical limitation of phase change materials in PCRAM is one category of the scalability limitations of PCRAM technology proposed in this thesis. In this chapter, it aims at three aspects in the study of the physical limitations of phase change materials in PCRAM: (1) categorizing the physical phase change process to explore the limitations; (2) investigating the reasons of the limitations; (3) providing solutions to extend the limitations.

## 2.1 Introduction

Traditionally, it was widely accepted that PCRAM technology is only limited by the lithography process (Lai, 2001). Hence most studies focused on improving the lithography technology. Following the fabrication of 180-nm PCRAM by Intel in 2001 (Lai, 2001), Samsung successfully developed a 90-nm node PCRAM chip (Takaura, 2006). Various advanced lithography technologies, such as the Electron Beam (Vieu, 2000) and Near-field Optical Microscopy (Wang, et.al, 2005), have also been used to fabricate PCRAM cells of a smaller size than 50 nm.

In fact, in Chapter 1, it has been proposed that lithography technology is only one of the four categories of scaling limitations of PCRAM technology. With the emergence of advanced lithography tools, other limitations, such as physical limitation of phase change materials, are likely to become more and more important for the PCRAM

research. In the PCRAM application, the physical limitation of phase change materials in PCRAM is considered as the minimum volume of the phase change material, which could achieve stable and reversible phase change. It can be affected by various factors: the material used, the capping material, the diffusion or environment radiation. However, few studies have so far focused on the physical limitation of phase change materials. Studies based on in-situ X-ray diffraction measurement have reported that a thickness of 3.6 nm is the limitation for the amorphous-fcc transition of $Ge_2Sb_2Te_5$ thin films capped by $Al_2O_3$ (Raoux, et. al, 2006). It is also found that Si and Ge have failed to show crystallization at very high temperatures with thin films of 2 nm thickness (Zacharias et. al, 1999; Williams et.al, 1990). In addition, an effective interfacial energy model was proposed for the physical limitations of Si and Ge. Thus Zacharias' work calls for further research on interface-affected phase change in chalcogenide glasses.

## 2.2 Three Categories of Phase Change for a Study on Physical Limitation

An in-depth investigation of the physical limitation of phase change materials in PCRAM is very important. At nano-scale, the effect of interface may affect phase change materials' properties and then further affect their physical limitations. Some studies have shown that phase change materials would have different crystallization properties when the film thickness was reduced to 20 nm (Martens, 2004; Miao, 1999). This different phase change process occurring at nano-scale is defined as nano-phase change, which is size-dependent, interface-dominated and surrounding materials related (Shi and Chong, 2007). Therefore, the study on physical limitation of phase change materials should

consider the different interface environments. Based on this concept, the phase change process can be divided into three categories for the study of physical limitation: (1) phase change in the free scale, (2) phase change surrounded by oxides/metals, and (3) reversible phase change surrounded by oxides/ metals. Because in PCRAM devices, phase change materials are usually surrounded by oxides or metals, the physical limitation of phase change material in PCRAM should consider the condition in which phase change material is surrounded by oxide/metal. This classification will provide useful guidance for the scaling research in PCRAM technology.

$Ge_2Sb_2Te_5$ is the most commonly used phase change material in PCRAM. An example of the physical limitation of $Ge_2Sb_2Te_5$ material capped by $ZnS\text{-}SiO_2$ is provided in this chapter. The same methodology can be extended to study the physical limitation of $Ge_2Sb_2Te_5$ capped with other materials and of other phase change materials.

### 2.2.1 Limitation for Phase Change in Free Scale

In the free scale, a crystalline cluster nucleates homogeneously within the amorphous regime or heterogeneously on discontinuities, such as precipitates, defects, and so on. The kinetics of the transition from the amorphous to the polycrystalline phase can be described by the classical nucleation theory (Fan and Laughlin, 2003), in which the nucleus formation normally is a gradual process. Initially, a number of atoms, which are accidentally in the right order, may form a nucleus. Once the nucleus reaches a critical radius, the embryo seed needs the energy to grow. Fig. 2.1 schematically describes the crystallization process in the free scale. The left figure shows the initial stage of embryo seed, while the right figure shows the nucleus after gradual growth. Hence, in order to

reduce the free energy, smaller-sized clusters tend to shrink, while those of larger sizes tend to grow. The size above which the clusters tend to grow is determined as the critical nucleus size (Fan and Laughlin, 2003; Zacharias and Streitenberger, 2000):

$$R_{crit} = \frac{2\gamma}{\Delta H * (Tm - T) / Tm} \tag{2.1}$$

where, $\gamma$ (interfacial energy) $=1\times10^{-5}$ J/cm$^2$, $\Delta$H (latent heat) =728 J/cm$^3$, $T_m$ (melting temperature) =900 K.

It is obvious that the critical nucleus size is related to the annealing temperature. When the temperature approaches the crystallization temperature, the critical nucleus in the GeSbTe material can be derived from Equation (2.1) and has been found to be approximate 0.52 nm, which is the size of a cluster of 27 atoms (Zacharias and Streitenberger, 2000):

$$i = 4\pi R_{crit}{}^3 / 3a^3 \approx 27 \tag{2.2}$$

where, the average interatomic distance a =0.28 nm (Kolobov, et. al, 2004).

This critical nucleus, with the size around 0.52 nm, limits the volume of the phase change process of the $Ge_2Sb_2Te_5$ material in the free scale.

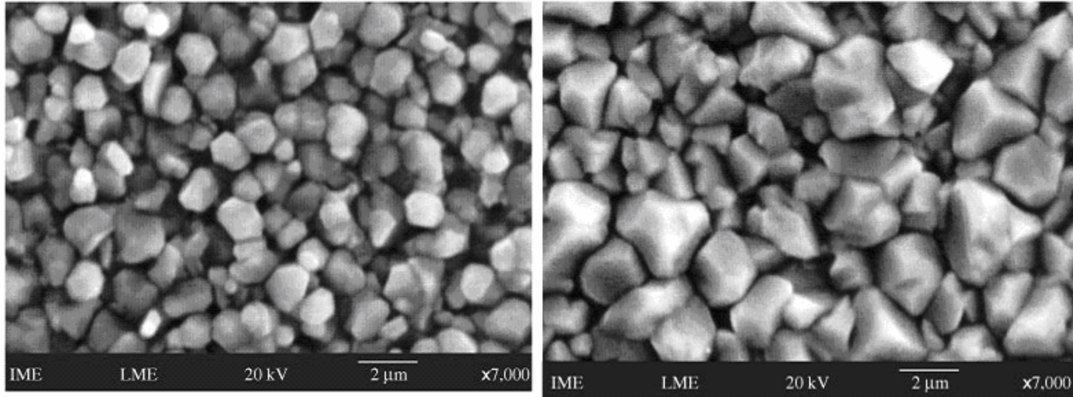



Fig. 2. 1 Schematic nucleation process of phase change material; the left figure shows the initial stage of embryo seed, the right figure shows the nucleus after gradual growth.

### 2.2.2 Limitation for Phase Change in $Ge_2Sb_2Te_5$ Films Surrounded by $ZnS$-$SiO_2$

The phase change process in $Ge_2Sb_2Te_5$ films would be very different when they are sandwiched by dielectrics. Simultaneous optical reflectance study had shown that even ultra-thin dielectric layers have a profound influence on the crystallization process (Leevad Pedersen, et. al., 2001). For a phase change material capped by an oxide, its phase change is a 3D issue, which is difficult to study with current analysis technologies at nano-scale. However, when the size continues scaling, the 3D issue can be simplified because the interfaces then become very close to each other (Fig. 2.2). When the opposite interfaces move closer and closer, the interference between them should be very strong compared to that when they are widely separated. Therefore, the effect of opposite interfaces would be the main concern in Fig. 2.2 (b). This 3D issue can be simplified to a thickness-dependent issue based on above discussion.

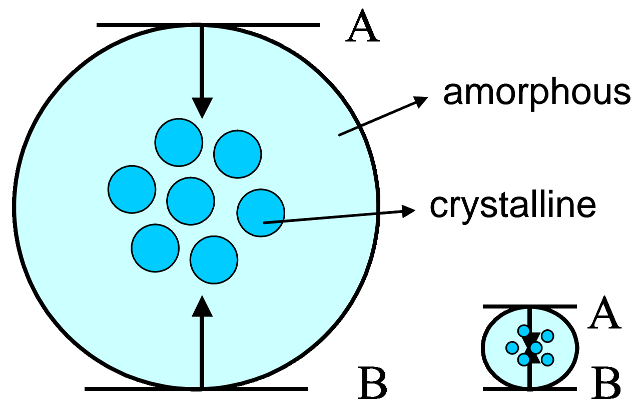


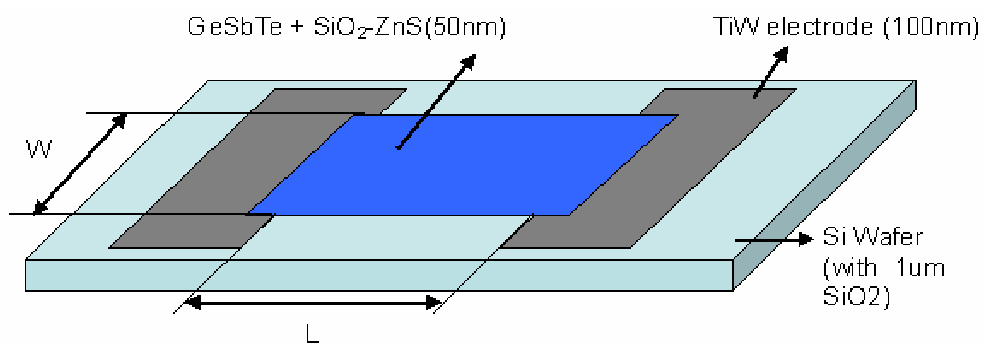

Fig. 2. 2 Interface effects in phase change materials surrounded by oxides/metals.

By considering only the opposite interfaces at thickness direction, the experimental study on the limitation for phase change in $Ge_2Sb_2Te_5$ films is feasible with a very simple set-up. In this thesis, a thermal electrical methodology was used to investigate limitations for the phase change in $Ge_2Sb_2Te_5$ films by simplifying the 3D issue to the thickness related issue. Although the results might vary slightly from those in the 3D condition, the principles and trends should remain applicable. This method is an effective tool for investigating the crystallization process of the $Ge_2Sb_2Te_5$ material because of its large signal margin, the easy-to-prepare samples and simple experimental set-up. The samples and experimental set-up are shown in Fig. 2.3.

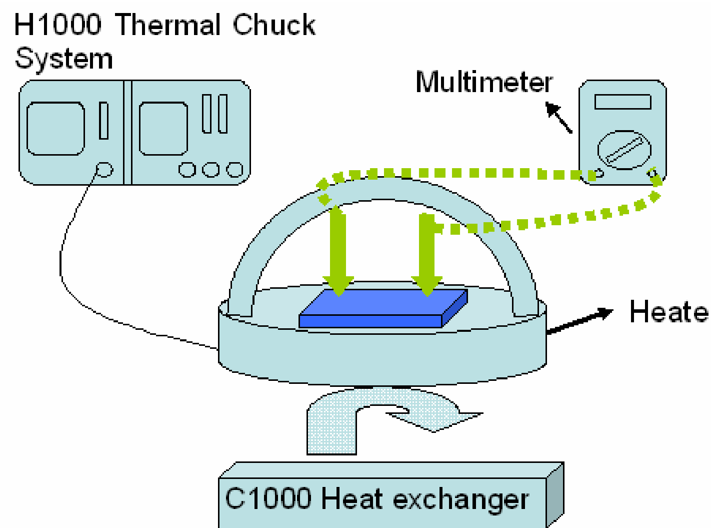
In this study, the $Ge_2Sb_2Te_5$ films were deposited by BLOZER dc magnetron sputtering using a stoichiometric target. The base pressure in the deposition chamber was typically $2 \times 10^{-6}$ Pa. Sputtering was performed using Ar ions at a flow rate of 15 sccm. The sputtering power of $Ge_2Sb_2Te_5$ thin film was 0.08 kW while the sputtering rate was 0.67 nm/s. $Ge_2Sb_2Te_5$ films of different thicknesses sandwiched by 50 nm ZnS-$SiO_2$ films were prepared. Two 100 nm TiW electrodes were embedded in the $Ge_2Sb_2Te_5$ films for

the measurement of resistance by the multimeter. The resistivity was calculated as $R \times \frac{L}{d \cdot W}$. L and W are shown in Fig. 2.3, while d is the thickness of the $Ge_2Sb_2Te_5$ film.

The sample was uniformly heated using the Micromanipulator™ H-1000 thermal Chuck System. The temperature was raised from the ambient temperature to 400 ˚C.




(a)




(b)

Fig. 2. 3 Sample (a) and set-up (b) for in-situ thermal electrical resistance measurement; the resistance of samples would be monitored during the annealing.

In the experiments, only the fcc transition occurring below 200 ˚C was studied. This is because, instead of the hexagonal closed-packed (hcp) phase, fcc is the dominant crystalline phase in PCRAM technology (Chiang et.al, 1999). With nano-second electrical pulses, it is possible for the heating rate to reach approximately $10^9$ ˚C/s in a PCRAM. Only the amorphous to fcc transformation is allowed at a high heating rate.

During the electrical thermal measurement, the samples were heated by means of the thermal chuck system at the rate of 10 ˚C/min. The values of electrical resistance versus temperature were recorded in Fig. 2.4. As the temperature increased, the resistance started to decrease for all the films. The gradual decrease of resistance was due to the temperature-dependent ionization in the semiconductor material rather than to the crystallization process (Pierret, 1988). The crystallization temperature ($T_x$) is the temperature point at which the resistance starts to decrease sharply and it is determined by the maximum in the first derivative of (dR/dT). The abrupt resistance decline was due to the rearrangement of atomic structures. It can be observed in Fig. 2.4, that $T_x$ was thickness (t) dependent. With the films of t >20 nm, the resistance decreased sharply at approximately 150 ˚C. With the films of 3.5nm< t <20 nm, the sharp decrease of resistance became less obvious. $T_x$ increased from >150 ˚C to ~ 170 ˚C as the films became thinner. A more detailed study on the $T_x$ change according to different film thickness will be carried out in the next chapter, when an exponential relationship is studied by plotting $T_x$ versus film thickness (Wei, et al., 2006).

The result discussed above indicated that there is a limitation for phase change at a thickness of t < 3 nm for $Ge_2Sb_2Te_5$ film sandwiched by $ZnS\text{-}SiO_2$. A similar phenomenon has been observed in other studies. For instance, Raoux reported that 3.6 nm

is the size limitation of $Ge_2Sb_2Te_5$ thin films capped by $Al_2O_3$ (Raoux, 2006) based on in-situ X-ray diffraction measurements. The limitation for phase change was also observed in other materials, a crystallization limitation at 2 nm was reported in $Si/SiO_2$ amorphous superlattice based on wide-angle X-ray scattering results (Zacharias, 1999).

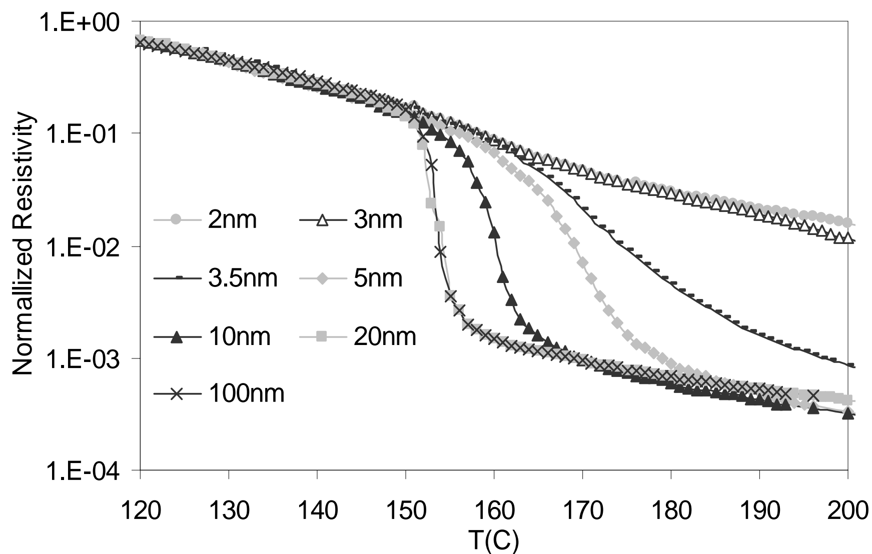



Fig. 2. 4 Exothermal electrical measurement of ultra-thin films; the crystallization process was delayed by a decrease in thin film thickness. When the thin film thickness became thinner than 3 nm, the crystallization did not occur.

### 2.2.3 Limitation for Reversible Phase Change in Thin Films Surrounded by $ZnS-SiO_2$

The third category of phase change process in chalcogenide materials is the reversible phase change sandwiched by oxides/metals. Since PCRAM is a direct over-write technology, the limitations of reversible phase change are critical for a good over-write cycle. Limitation for reversible phase change can be caused by various factors. Residual crystallites or amorphous tails exist when the phase change material was not completely

programmed (Yamazaki, et. al, 2004; Mantegazza, et. al, 2007). Those residuals will affect the following programming behavior of devices. A serious accumulation of residual may even cause the malfunction of PCRAM. Compositional change of $Ge_2Sb_2Te_5$ within the device is another effect that may limit the reversible phase change in phase change materials (Yoon, et. al, 2007). The unexpected formation of a Ge–Te-based alloy may slow down speed of programming to 100 μs. This compositional change can be caused by the reaction of phase change mateiral with adjacent material at high temperature. It can also be caused by the atomic movement under the electrical field. However, besides the limitations mentioned above, what would also affect the scaling of PCRAM technology, especially when the operation temperature is as high as 600 ˚C?

By means of thermal electrical measurement, a limitation for reversible phase change caused by diffusion was identified. It can be seen in Fig. 2.5, that while normal resistance decreased before melting, the resistance of 10 nm $Ge_2Sb_2Te_5$ had an abnormal rising above a certain temperature, after which the thin film become failing to function as phase change material. Thus, this abnormal and non-reversible resistance change of phase change materials caused by long-time and high-temperature annealing was defined as "film breakdown". The temperature, after which film starts to breakdown, was defined as $T_{fdb}$ (film break-down temperature). This resistivity increase was an irreversible process, which indicated that high temperature might have caused a destructive effect on ultra-thin films. $T_{fdb}$ was the temperature at which the destructive damage started to induce an obvious increase in resistance.

Thin films with different thickness were annealed from room temperature to 400 ˚C at a heating rate of 10˚C/ min. The electrical resistance after the thin film breakdown was

recorded according to the temperature in Fig. 2. 6. It is obvious that in thin films of 10 nm and 5 nm thick, the rising of the electrical resistance was gradual. While, when the film thickness was reduced to 3 nm and 2 nm, the breakdown was very obvious and the rising rate of electrical resistance increased dramatically. Therefore, the breakdown is more obvious in thinner films. $T_{fdb}$ as a function of film thickness is also shown in the inset of Fig. 2.6, where it can be found that $T_{fbd}$ is reduced from 295˚C for 10nm thin film to 288˚C for 5 nm thick thin film and finally to 257˚C for 2 nm thick thin film. The physical mechanisms behind this phenomenon will be discussed in section 2.3.

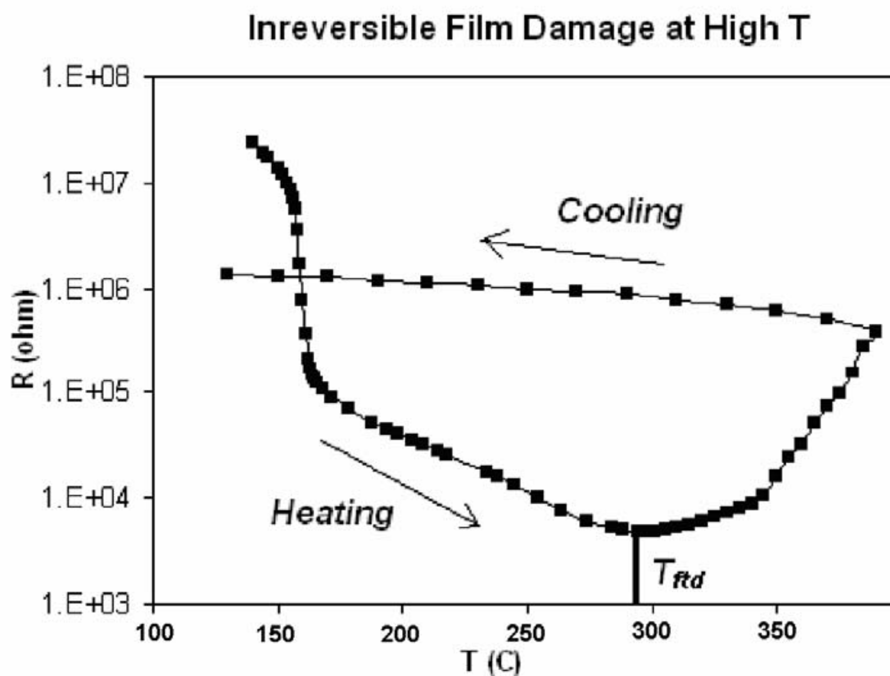



Fig. 2. 5 A thin film breakdown of $Ge_2Sb_2Te_5$/ oxide sandwiched structures at high temperature; the performance of phase change material would not be recovered after the breakdown of the film.

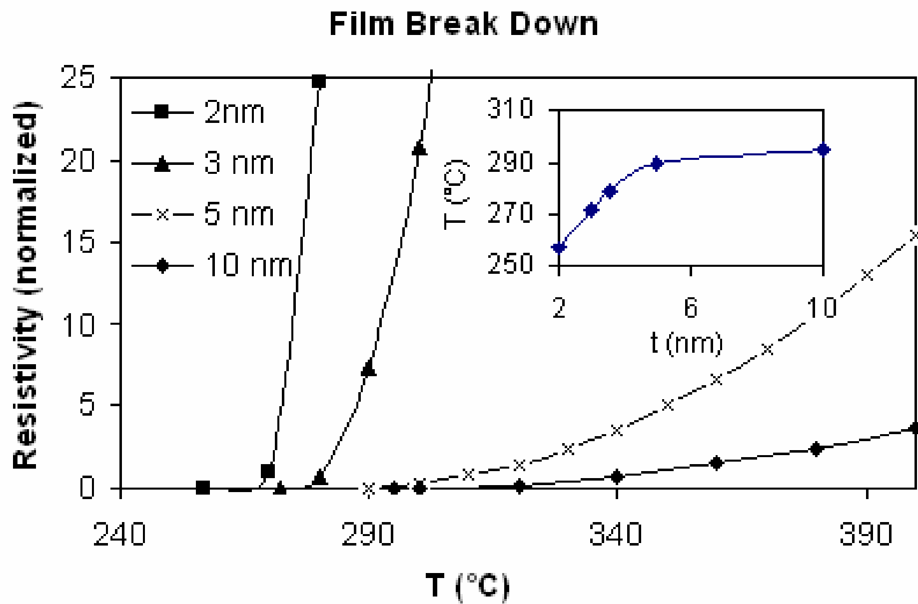



Fig. 2. 6 $T_{fbd}$ in different phase change thin films of different thickness.

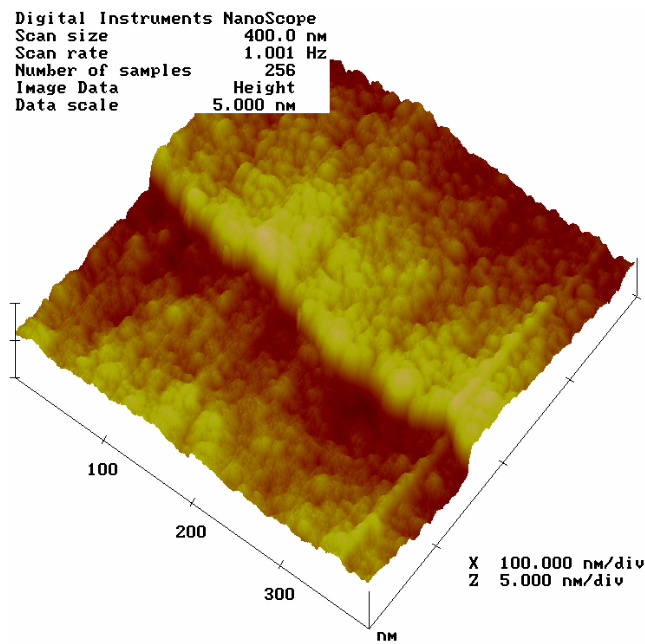
## 2.3 Causes of Physical Limitations of Phase Change Materials

### 2.3.1 Causes of Limitation for phase change in Thin Films Surrounded by ZnS-$SiO_2$

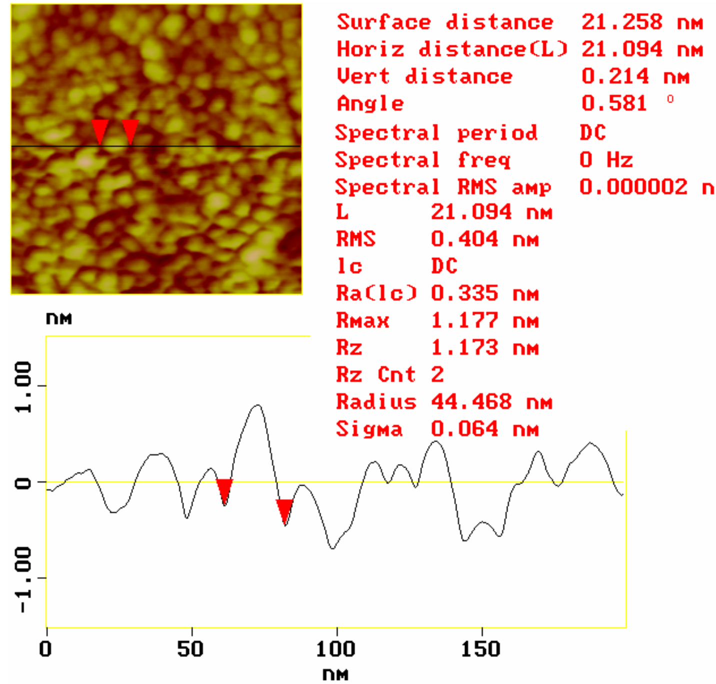
In section 2.2.2, it was reported that crystallization was found to be different in ultra-thin phase change films with different thicknesses. When the thickness of films was less than 3 nm, no sharp decline in resistance was observed. These results indicate that the phase change does not occur below a certain thickness.

One possible explanation for such a phenomenon is the discontinuous model (Levchenko, 2004), in which the film is formed by isolated islands, rather than by the formation of a continuous layer at the initial stage of deposition. When deposition continues, due to the influx of particles to the island and the substrate surface, the

subsequent growth of isolated islands on the surface causes them to come into contact and coalesce, and a continuous film is formed. In order to study whether this model is applicable for the limitation for phase change in thin films, Atomic Force Microscope (AFM) measurement was conducted. From the 3D cross-sectional view as shown in Fig. 2.7 (a), it can be observed that films as thin as 2.8 nm were continuous. The surface roughness of 1.3 nm was formed by the overlapping of ellipsoidal grains, of sizes ranging from 8 nm to 15 nm (Fig. 2.6 (b)). Therefore, the continuity of thin films was not the reason for the limitations for the phase change in thin films.




(a)




(b)

Fig. 2. 7 Topography and cross-section of a 3nm thick $Ge_2Sb_2Te_5$ thin film measured by AFM.

Since the thin film discontinuity model is not applicable for the limitation for phase change in this experiment. Other models are considered. One theory to explain the critical thickness for crystallization is based on the effective interfacial energy model. This model was proposed by Zacharias to explain the thickness dependence of Si/$SiO_2$ amorphous superlattice structure. It was reported that when the thickness of each Si layer was reduced below 2 nm, the Si thin film couldn't be crystallized (Zacharias and Streitenberger, 2000). Similar to Zacharias' experiment, the study on the limitation for phase change in $Ge_2Sb_2Te_5$ films also monitors the thickness dependent crystallization process. Furthermore, $Ge_2Sb_2Te_5$ films are also sandwiched by dielectric. Therefore, Zacharias' model can be used to study the limitation for phase change in $Ge_2Sb_2Te_5$ films.

In Zacharias' model, the crystallization nuclei are assumed to be symmetrically embedded in the amorphous material between the oxide interfaces and is cylindrical in shape. Here, an additional spacing *l* which corresponds to a finite separation of the nucleus from the boundaries represented by the material *o* is introduced (Fig. 2. 8). When the film is very thick, the effect of *l* can be ignored, and the classic nucleation theory is applicable. However, when the thickness keeps being reduced, the effect of *l* will become more and more obvious. The direct influence of this additional spacing results in an increase in the nucleation barrier.

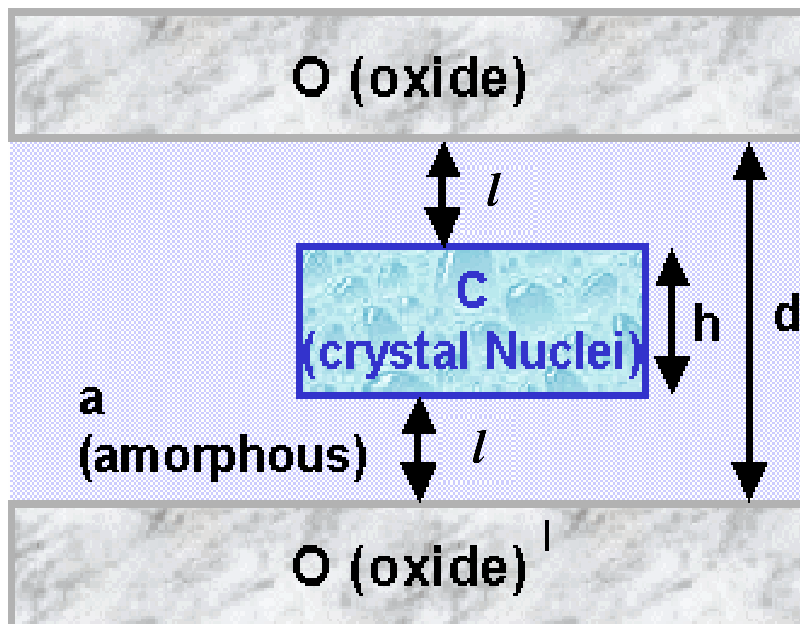



Fig. 2. 8 Model of a cylindrically shaped nano-crystal embedded in an amorphous film with oxide interfaces.

The relationship between *l* and the nucleation barrier is realized by taking into account of the different interface energies and materials. According to the model, a phenomenon, where an exponential increase in the $T_x$ corresponds with decreasing layer

thickness and can be expressed as (Zacharias, et. al, 2000)

$$T_c = T_{ac}(1 + \frac{\gamma_{oc} - \gamma_{ac} - \gamma_{oa}}{\gamma_{ac}})e^{-d/4l_0} \tag{2.3}$$

where, $T_c$ is the actual crystallization temperature. $T_{ac}$ is the crystallization temperature in bulk materials. $\gamma_{ac}$, $\gamma_{oc}$, and $\gamma_{oa}$ are defined as (1) the interfacial free energies per unit area between the amorphous (a) and crystalline (c) semiconductor phases (a/c); (2) between the oxide material (o) and the crystalline (c) semiconductor phase (o/c); and (3) between the oxide material (o) and the amorphous (a) phase (o/a), respectively; $l_o$ is an average screening or bonding length related to the range of interatomic forces typical of materials (o) and (c). Because the nucleation barrier is increased with effective interface energy, the model yielded a lower bound for layer thickness below which no crystallization can occur in the phase change material (Zacharias and Streitenberger, 2000).

Referring to the $Ge_2Sb_2Te_5$ material in this experiment, it can be deduced that the effective interface energy for the film below 3.5 nm is too high for maintaining a stable nucleus for the crystallization to occur. This model can also explain the differences in the critical thickness of crystallization of $Ge_2Sb_2Te_5$, which was reported by Raoux (Raoux, 2006) and in this thesis. The discrepancy was caused by the differences in effective interface energy due to the use of different capping materials.

In addition to the successful explanation on the discrepancy between Raoux's result and the results in this thesis, this effective interfacial energy model is also applicable to the increase in $T_x$ in ultra-thin films. More detailed research is to be introduced in Chapter 3. An exponential relationship can be found by plotting $T_x$ versus film thickness, which corresponds closely to the model (Wei, et al., 2006). Therefore, this model is more plausible to explain the cause of the limitation in thin films surrounded by $ZnS\text{-}SiO_2$.

### 2.3.2 Causes for Limitation for Reversible Phase Change

To investigate the causes for this irreversible change of resistance, X-Ray refractor was used to measure the changes in density and thickness of sample layers during the annealing process (Table 2.1). This high-resolution X-ray specular reflectometry at the grazing incidence angle in the X-ray demonstration and development (XDD) of the beamline carried out with the Huber 4-circle system 90000-0216/0, with a high-precision 0.0001° step size for the omega and two-theta circles. The storage ring, Helios 2, was run at 700 MeV and a typically stored electron beam current of 300 mA. The X-ray beam was conditioned to select $CuK\alpha_1$ radiation (8.048 keV in photon energy) by means of Si (111) channel-cut-monochromator (CCM) and blocked to be 0.90 mm high vertically and 3.0 mm wide horizontally by a slit system. Such set-up yielded an x-ray beam with about 0.01° in vertical divergence. The detector slit was adjusted to be 1.00 mm high to ensure recording of all reflected photons. The typical counting time was 5 seconds for every step and step size of theta 0.005° or 0.0066° for the samples, to ensure that the oscillation in reflectivity was well recorded.

According to the results shown in Table 2.1, the density of the as-deposit amorphous $Ge_2Sb_2Te_5$ was 5.7±0.2 $g/cm^{-3}$. After crystallization, the density increased to 6.3±0.3 $g/cm^{-3}$. Thus the densities are in fairly close agreement with the values in the other studies (Njoroge et. al., 2002). However, when the film breakdown occurred, the density of $Ge_2Sb_2Te_5$ films decreased and reduced to as low as 4.7±0.3 $g/cm^{-3}$ at 390 ºC, which was even lower than the amorphous density of the $Ge_2Sb_2Te_5$ material. This indicated the change in the composition of the phase change thin film. The difference in thickness of sample layers before and after breakdown may provide more information for explaining

this phenomenon. In fact, the thickness of the phase change layer decreased from 3.2±0.1 nm to 2.83±0.09 nm during this process due to the density change. After the thin film had broken down, the thickness in the phase change layer increased while the top ZnS-$SiO_2$ layer shrank. When the temperature reached 390 ºC, the layer had expanded by 2.17 nm, which was roughly the same as the shrinking value of the thickness in the top ZnS-$SiO_2$ layer. Thus the result indicates that the interfaces of the $Ge_2Sb_2Te_5$ layer and the dielectric layer had been enlarged and the diffusion had occurred between the interfaces.

Table 2. 1 Layer parameters of ZnS-$SiO_2$ /$Ge_2Sb_2Te_5$/ZnS-$SiO_2$ sandwich structures obtained by X-Ray refractor measurement.

| **Sample** | | **As deposited** | **250 °C** | **390 °C** |
|---|---|---|---|---|
| Top ZnS-$SiO_2$ layer | Thickness, nm | 63.7±0.2 | 63.2±0.2 | 60.2±0.2 |
| | Surface Roughness, nm | 0.5±0.1 | 0.73±0.06 | 0.7±0.2 |
| | Density, $g/cm^{-3}$ | 3.5±0.1 | 3.5±0.1 | 3.5±0.1 |
| $Ge_2Sb_2Te_5$ layer | Thickness, nm | 3.2±0.1 | 2.83±0.09 | 5.0±0.2 |
| | Interface Roughness, nm | 0.6±0.1 | 0.9±0.3 | 1.2±0.5 |
| | Density, $g/cm^{-3}$ | 5.7±0.2 | 6.3±0.3 | 4.7±0.3 |

## 2.4 Possible Solution for Extending Physical Limitations in Phase Change Materials

Based on the above discussion, diffusion may cause the physical limitation for phase change materials at a thickness of 10 nm for the reversible phase change when $Ge_2Sb_2Te_5$ thin films were capped with ZnS-$SiO_2$. To extend the physical limitation, one efficient way was to add the diffusion protective layers. For example, $Al_2O_3$ was added to prohibit the diffusion of Aluminum (Shunichi, et.al., 1984). Therefore, in this thesis, additional diffusion protective layer was proposed to extend the physical limitation for the reversible phase change in $Ge_2Sb_2Te_5$ thin films. To prevent the diffusion between oxide

dielectric layer and other material, nitrides, such as Ta-Si-N, AlNx and GeNx, are commonly used because of the good diffusion protective effect of N to O atoms (Adedeji, et. al., 2006; Nakamura, et.al., 1998).

In this experiment, 20 nm GeNx thin film was added between the ZnS-$SiO_2$ layer and $Ge_2Sb_2Te_5$ material. This sample was compared with the one, in which GeNx was absent. The total thickness of the dielectric layers (including GeNx layer) of both samples maintained at 50 nm. The first experiment was carried out on the samples with the same $Ge_2Sb_2Te_5$ thin film (10 nm thick) and the results were shown in Fig. 2.9. It is obvious that at the temperature around 350°C, the resistance of the sample without GeNx increased fast while the resistance of the sample with GeNx was stably reduced. In other words, the thin film breakdown didn't happen in the sample with diffusion protective layer. It indicates that the GeNx diffusion protective layer can effectively extend the physical limitation caused by diffusion in reversible phase change of phase change material.

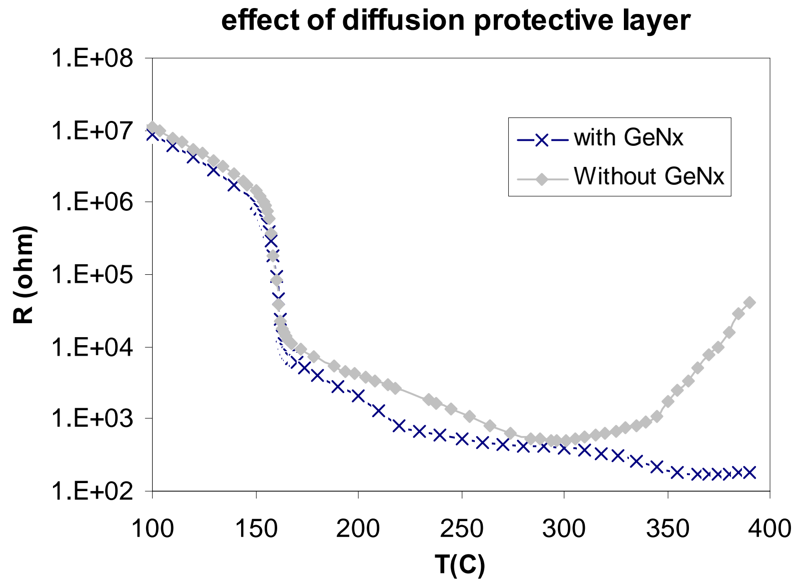



Fig. 2. 9. The electrical resistance of samples with and without 20 nm thick GeNx layer during annealing; the $Ge_2Sb_2Te_5$ thin film was kept the same thickness 10 nm in both samples.

## 2.5 Summary

To study the physical limitation of PCRAM technology, three categories of the phase change processes were proposed: (1) phase change in the free scale, (2) phase change surrounded by oxides/metals, and (3) reversible phase change surrounded by oxides/metals. An electrical thermal methodology was developed to simplify the 3D limitation issue to that of a thickness dependent issue. For the physical limitation in free scale, the critical radius of the stable $Ge_2Sb_2Te_5$ nucleus was calculated to be approximately 0.52 nm. Below this value, the crystallization would not occur. In the case of limitation of phase change material sandwiched by dielectrics, it was found that $Ge_2Sb_2Te_5$ films thinner than 3 nm could not crystallize because the thickness dependent interfacial energy would increase the crystallization barrier in the phase change materials.

Regarding the reversible phase change in memory cells, the diffusion induced physical limitation was discussed. It was noted that the diffusion of dielectrics would destroy the ultra-thin $Ge_2Sb_2Te_5$ films (10 nm) at high temperatures. A diffusion protection layer was proven to effectively extend the limitation for reversible phase change. This work has provided an important reference for the systematic study of the scaling limitations of PCRAM technology.

It is important to emphasize that the diffusion is one of the major reasons for the physical limitation in reversible phase change categories. The annealing time in this experiment is approximately ten minutes, while the heating pulses in PCRAM devices would be shorter than 100 nano-seconds. Therefore, the diffusion would not be as obvious during the PCRAM operation as during the experiment in this chapter. However, it still can be predicted that when PCRAM devices have been written for about $10^8$ cycles or less, the effect of diffusion would become significant and affected the functionality of device.

# CHAPTER 3
# THICKNESS DEPENDENT NANO-CRYSTALLIZATION

The study of the physical limitation of PCRAM has shown that crystallization of phase change materials could be affected by the interfaces at the nano-scale. More systematical study on interface effects is carried out in this chapter while a thickness-dependent nano-crystallization in ultra-thin films is comprehensively investigated. Furthermore, crystallization kinetics, including the crystallization mechanism, the corresponding activation barrier and the Avrami coefficient are also studied. In addition, the effects of thickness-dependent nano-crystallization on PCRAM performance are discussed in this chapter.

## 3.1 Background

After Yamada (Yamada, et.al., 1991) initially proposed the GeTe-$Sb_2Te_3$ pseudobinary amorphous thin films as a rapid-phase transition material for optical disk memory in 1991, GST materials quickly became the most used phase change materials for phase change storage technologies. Its crystallization process has also been widely investigated, especially for the most popular $Ge_2Sb_2Te_5$ material.

In the previous studies, $Ge_2Sb_2Te_5$ materials were found to have two crystalline states: fcc structure and hexagonal structure (Yamada, et. al, 1987; Friedrich, et. al, 2000). In these studies, X-ray diffraction (XRD) was the most common tool for studying the atomic

structure. In XRD scanning, it was found that the transition to fcc structure occurs around 150 ˚C and its lattice constant is approximately 6 Å. The transition to the hexagonal structure happens at approximately 270 ˚C and its lattice constant was determined to be a ~ 4.2 Å and c ~17 Å (Friedrich, et. al, 2000).

The crystallization process of $Ge_2Sb_2Te_5$ materials can be divided into two stages: the nucleation and growth stages. The crystallization kinetics, which include the crystallization mechanism, the corresponding activation barrier and the Avrami coefficient, have been mostly investigated employing the optical reflectivity/transmission measurement and the electrical resistance measurement (Yamada et. al, 1991; Friedrich et. al, 2000). The activation barrier is normally determined by the Kissinger plots which can be obtained from the exothermal measurement. For the fcc and hexagonal transitions in $Ge_2Sb_2Te_5$ materials, the activation barriers were measured to be 2.24 eV and 3.64 eV, respectively (Friedrich, 2000). The Avrami coefficient was normally determined by Johnson–Mehl–Avrami (JMA) plot, which can be obtained by means of isothermal measurement. The Avrami value for $Ge_2Sb_2Te_5$ was found to be approximate 2.5 (Weidenhof, 2001), however, these parameters were dependent on the capping dielectric material (Norikazu, 1996). The $E_a$ values reported in different literatures were listed in Table 3.1.

Table 3. 1 Activation energy ($E_a$) and avrami coefficient (n) in publications.

| $E_a$ | Journal | Notes |
|---|---|---|
| 2.7 ± 0.1 eV | Privitera, et. al, 2003 | $Ge_2Sb_2Te_5$ capped by ZnS-$SiO_2$ |
| 2.24 ± 0.11eV (fcc)<br>3.64 ± 0.19 eV (hex) | Friedrich et. al, 2000 | $Ge_2Sb_2Te_5$ |
| 2.5-3.0eV | Ohshima, et.al, 1996 | $Ge_2Sb_2Te_5$ capped by different dielectric materials |
| 2.23 eV ($Ge_2Sb_2Te_5$)<br>1.82 eV ($GeSb_2Te_4$)<br>1.52 eV ($GeSb_4Te_7$) | Yamada, et. al, 1991 | by Kissinger's plot |
| 2.0 eV | Trappe, et. al, 1998 | $Ge_2Sb_2Te_5$ capped by ZnS-$SiO_2$ |
| 1.98eV<br>2.31eV | Jeong, et. al, 1999 | $Ge_2Sb_2Te_5$ on Si<br>Two stage model: $1^{st}$) n >4, En =2.26eV, surface nucleation domain, $2^{nd}$), n =1.1, Eg =1.98, growth domain |
| **N** | **Journal** | **Notes** |
| 2.5 ± 1 | Weidenhof, et. al 2001 | $Ge_2Sb_2Te_5$ on glass |
| 1.5($Ge_2Sb_2Te_5$)<br>1 (capped with $SiO_2$)<br>1.8 (with $Si_3N_4$)<br>1.5(with $Ta_2O_5$)<br>3.0(with ZnS)<br>3.2(with ZnS-$SiO_2$) | Ohshima, et. al, 1996 | $Ge_2Sb_2Te_5$ capped by different dielectric materials<br><br>Laser as the thermal source |
| 1 | Trappe, et. al, 1998 | |
| 2 | Tominaga, et. al, 1998 | |
| 1.15- 1.25 | Jeong, et. al, 1999 | Proposed two-stage model<br>Surface nucleation |

However, the crystallization in the nano-scale was reported to register significant differences (Shi and Chong, 2006). Furthermore, the interfaces were found to affect the crystallization at nano-scale. In this chapter, two-probe resistance measurements are used to investigate the thickness-dependent nano-crystallization in ultra-thin films. Only the fcc transition is to be studied in this dissertation because of its dominant role in memory cell operations.

## 3.2 Experiments

### 3.2.1 Set-up and Samples

The in-situ thermal electrical measurement is an effective method of investigating the crystallization process of phase change materials. This method was used to study the physical limitation in Chapter 2. Although the resistivity may be slightly affected by parameters of electrodes, such as material, film thickness or contact area, this error does not affect the characterization of crystallization process. Electrodes with different resistances would cause differences in the calculated electrical resistivity of phase change materials. However the crystallization point and the shape of curves should be the same. As shown in Fig. 3.1, two samples are prepared with the same GeSbTe films but different electrodes. The GeSbTe was kept 30 nm thick while the electrodes were 20 nm and 80 nm respectively. Because $T_x$, which was defined by the first derivative of resistance, was the focus in this study, if two samples can deliver the same $T_x$ value, this experiment is accurate enough for this study. The result showed that the crystallization process was almost the same in both samples and the $T_x$, which is determined by the minimum in the first derivative obtained by (dR/dT) was identical. In this thesis, this two-probe measurement set-up has proven to be significantly efficient and accurate to analyze the $T_x$ of the materials.

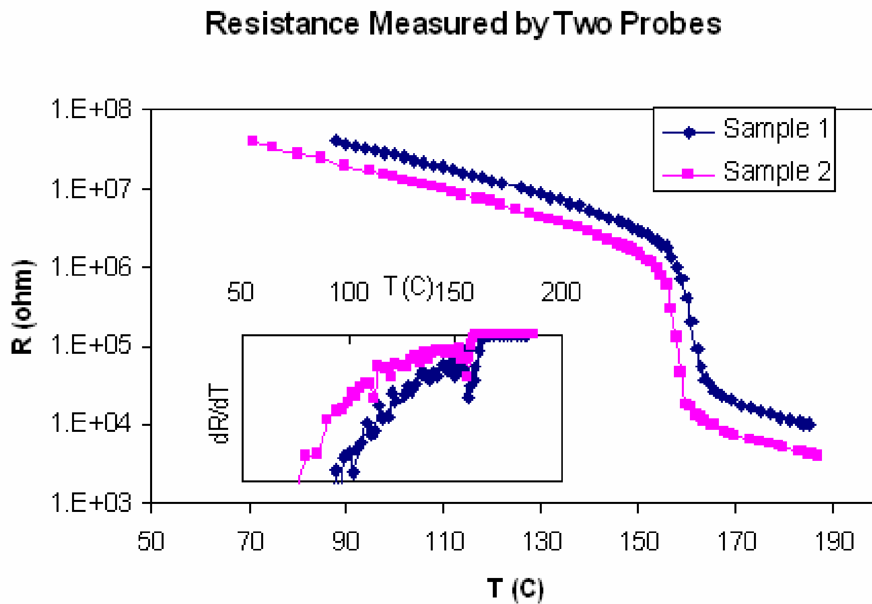



Fig. 3. 1 Resistance measurement by two-probe set-up.

### 3.2.2 Exothermal Measurements

The exothermal measurement (ETTM) is used to measure the properties' change (electrical, optical, and so on) of the materials during increase/decrease of temperatures. It is a very important method for studying the activation energy and properties of thermally induced changes in a material. In this thesis, the experiment was carried out at a heating rate of 0.5 ˚C/min, 1 ˚C/min, 3 ˚C/min, 10 ˚C/min and 20 ˚C/min, respectively, ranging from 21 ˚C to 220 ˚C. The dependence of electrical resistivity on temperature was recorded for 30 nm and 5 nm thin films, respectively (Fig. 3.2). The steep drop of resistivity identified the crystallization process. It was obvious that the crystallization was delayed when the heating rate increased from 0.5 ˚C/min to 20 ˚C/min. In 30 nm thin films, the $T_x$ was increased from around 145 ˚C to nearly 160 ˚C . Similar in 5 nm thin

films, the $T_x$ was increased from around 160 ˚C to higher than 170 ˚C. Furthermore, the decline of the electrical resistance during crystallization in 30 nm sample was also much steeper than that of the 5 nm sample. In 30 thin films, the crystallization happened within 1 min, while in 5 nm thin films, the crystallization process took more than 5 minutes.

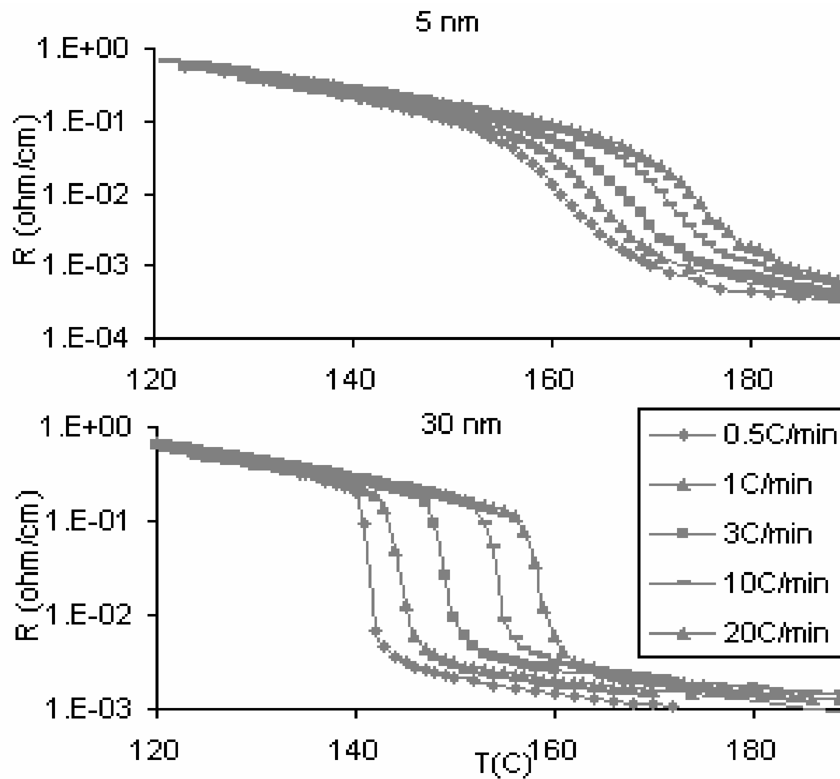



Fig. 3. 2 ETTM of 5 nm and 30 nm $Ge_2Sb_2Te_5$ thin films at different heating rate.

Besides different heating rates, samples with different thicknesses but maintaining with the same heating rate were also fully investigated. $Ge_2Sb_2Te_5$ films of 3.5 nm, 5 nm, 10 nm, 15 nm, 20 nm, 30 nm, 100 nm were prepared for ETTM measurement at a heating rate of 10 ˚C /min. Fig. 3.3 shows that it was obvious that the crystallization process was strongly related to film thickness. For films thicker than 20 nm, the curves are almost overlapped; while for those below a thickness of 20 nm, the decline of resistance shifted

towards higher temperatures and the curvature of decline was less sharp.

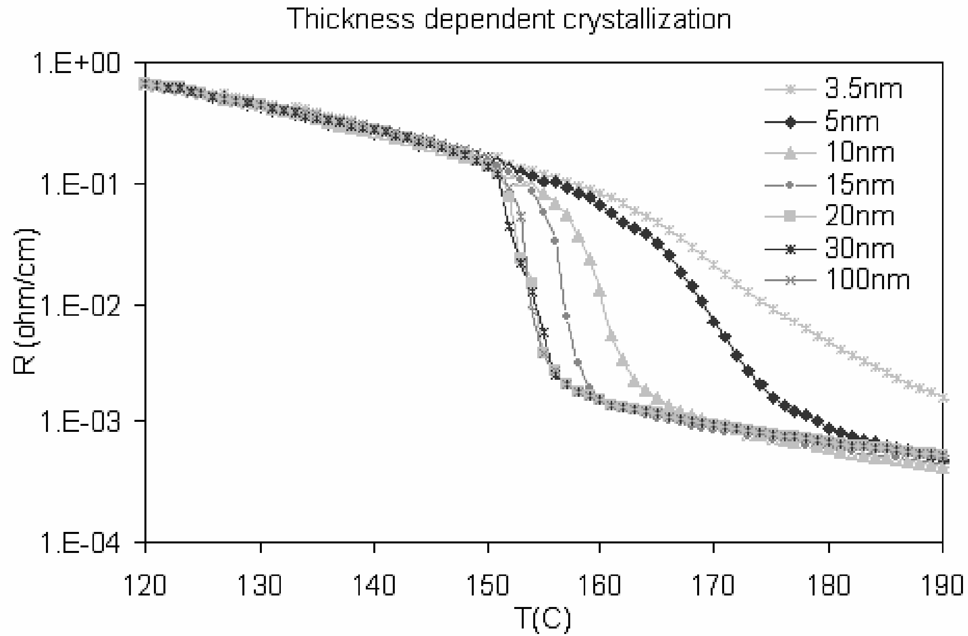



Fig. 3. 3 ETTM of different thick $Ge_2Sb_2Te_5$ thin films at 10 ˚C/min.

### 3.2.3 Isothermal Measurements

Isothermal measurement (ITTM) is another important method for studying the *in situ*-material properties during the annealing process. During an ITTM, the same temperature would be maintained and the relevant parameters were recorded according to the annealing duration. In the experiment, samples of GeSbTe films of 100 nm, 30 nm, 20 nm, 10 nm, 15 nm, 5 nm and 3.5 nm thicknesses were isothermally annealed at 143.5 ˚C. The resistivity as a function of time was recorded (Fig. 3.4). A featured parameter in isothermal measurement is the incubation time ( $\tau$ ), which is determined by the time

before a sharp transition. It was obvious that $\tau$ was much larger for the samples with GeSbTe films thinner than 20 nm, which was in close agreement with the values measured by ETTM. Correspondingly, the transition time from the highest to the lowest resistivity was increased as the thickness decreased, from $10^2$ s for 100 nm to $10^5$ s for 3.5 nm. It indicated that the crystallization speed decreased as the film thickness scaled.

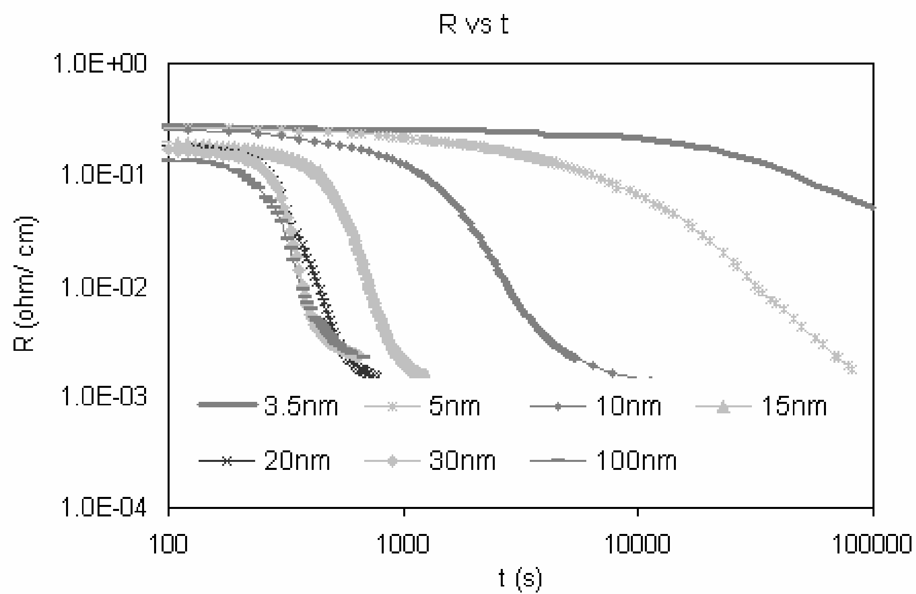



Fig. 3. 4 Resistivity as function of time when $Ge_2Sb_2Te_5$ thin films under 143.5 ˚C.

# 3.3 Thickness Dependent Nano-crystallization

## 3.3.1 Crystallization Temperature

The $T_x$, can be determined by the ETTM results as the minimum temperature in the first derivative obtained by (dR/dT). The $T_x$ at a heating rate of 10 ˚C/min for different film thickness is shown in Fig. 3.5. It was obvious that the $T_x$ increased with a decrease in

the thickness of GeSbTe. The $T_x$ at different thicknesses and at different heating rates are listed in Table 3.2. It is shown that the $T_x$ increased from 138˚C to 157˚C when the thickness was reduced from 30 nm to 5 nm at a heating rate of 0.5˚C/min. At the same time, $T_x$ was also related to the heating rate. It increased from 157˚C to 170˚C when the heating rate was increased from 0.5˚C/ min to 20˚C /min at a same thin film thickness.

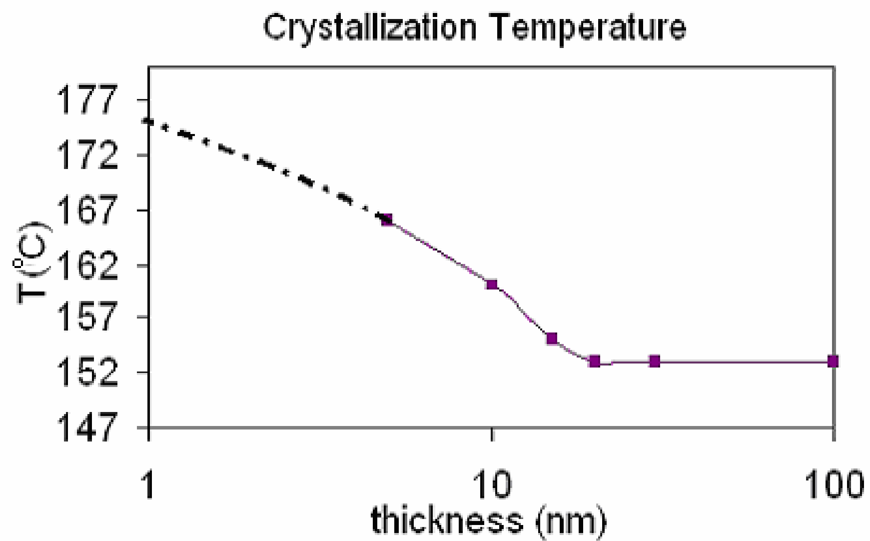



Fig. 3. 5 The dependence of the crystallization temperature dependence on thickness at a heating rate of 10 ˚C/min.

Table 3. 2 Crystallization temperature (˚C) measured by ETTM.

| R (˚C/min) | 5nm | 10nm | 15nm | 20nm | 30nm |
|---|---|---|---|---|---|
| 0.5 | 157 | 149 | 141 | 138 | 138 |
| 1 | 159 | 153 | 147 | 142 | 142 |
| 3 | 164 | 157 | 152 | 148 | 148 |
| 10 | 166 | 160 | 155 | 154 | 154 |
| 20 | 170 | 164 | 160 | 157 | 157 |

### 3.3.2 Crystallization Activation Energy

The activation energy for crystallization could be derived by the Kissinger plot (Shelby 2005) as:

$$\ln\left(R / Tx^2\right) = E_{ec} / K_B Tx + X \quad (3.1)$$

where, R is the heating rate; $T_x$ is the crystallization temperature at heating rate R; $K_B$ is the Boltzmann's constant.

Based on the previously determined $T_x$, the Kissinger curve for each sample was plotted in Fig. 3.6, which shows that the slope of each line corresponded to the activation energy (Ea). It is obvious that a linear relationship was obtained between $\ln\left(R/Tx^2\right)$ and $\left(R/Tx\right)$. The Ea, which can be estimated from the slope of the Kissinger plot, is listed in Table 3.3. It is obvious that the activation energy was increased from approximately 2.86 ev for the films thicker than 20 nm, to 4.66 eV for the films of 5 nm thick.

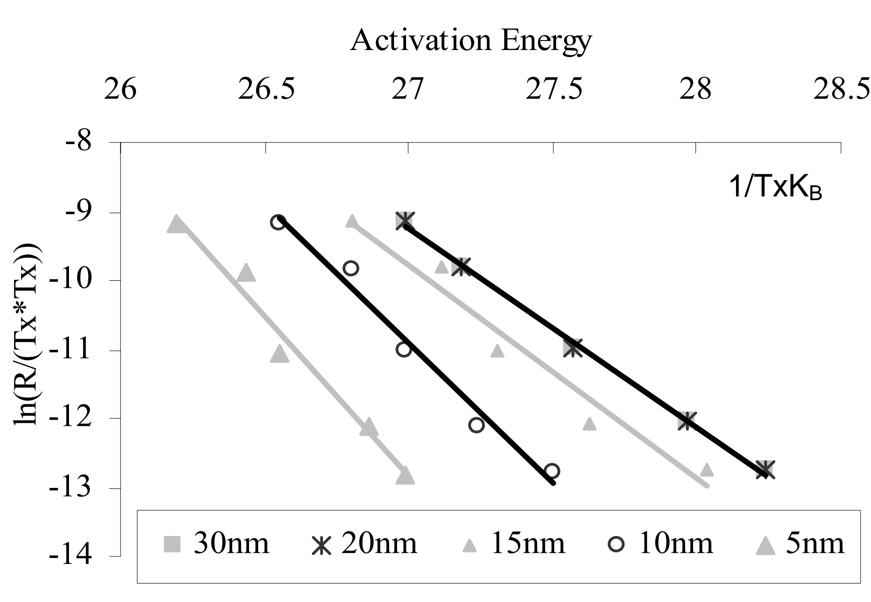



Fig. 3. 6 ETTM kissinger plot of ultra-thin GeSbTe films measured by ETTM.

Table 3. 3 $E_a$ in ultra-thin $Ge_2Sb_2Te_5$ films.

| | 5nm | 10nm | 15nm | 20nm | 30nm |
|---|---|---|---|---|---|
| $E_a$ (eV) | 4.66 | 4.06 | 3.11 | 2.86 | 2.86 |

Furthermore, based on the $E_a$ estimated from the slopes of the Kissinger plots, a linear relationship was found between Ln ($T_x$) and thickness *d* as shown in Fig. 3.7. Because the $E_a$ is directly related to the $T_x$, it can be used to explain the increasing $T_x$ in ultra-thin films. This linear relationship is in good agreement with the results obtained by by Zacharias, which was introduced in detail in Chapter 2.

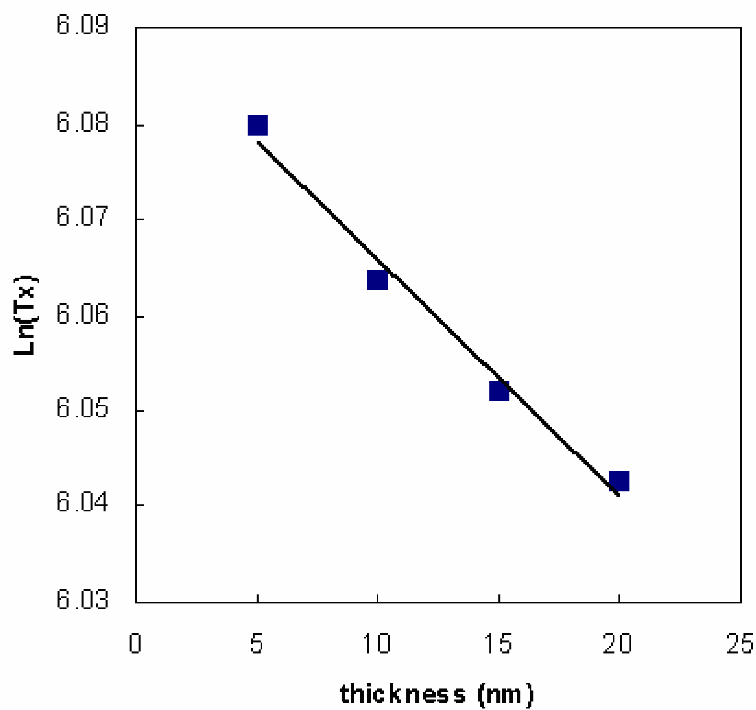



Fig. 3. 7 The linear relationship between Ln ($T_x$) and thin film thickness.

### 3.3.4 Avrami Coefficient

In JMA model, a 3D nucleation and growth process was proposed (Senkader, 2004;

Weidenhof et. al, 2001). The volume fraction of the transformed materials X(t) can be described by the well-known JMA equation:

$$\ln[-\ln(1-x(t)) = \ln k + n\ln(t) \tag{3.3}$$

$$k = v\exp\left(\frac{E_A}{k_B T}\right) \tag{3.4}$$

where t is time; n is the Avrami coefficient; and k is an effective rate constant; v is the frequency factor; $E_a$ is the activation energy; T is the absolute temperature; and $K_B$ is the Boltzmann constant ($K_B$ = 1.380658e-23 J/K = 8.617e-5 eV/K).

The detailed conditions for the calculation of the Avrami coefficient of crystallization dominated by diffusion-controlled growth are listed in Table 3.4.

Table 3. 4 Avrami coefficients in diffusion controlled growth.

| Conditions | n |
| --- | --- |
| All shapes growing from small dimensions, increasing nucleation rate | >2.5 |
| All shapes growing from small dimensions, constant nucleation rate | 2.5 |
| All shapes growing from small dimensions, decreasing nucleation rate | 1.5 – 2.5 |
| All shapes growing from small dimensions, zero nucleation rate | 1.5 |
| Growth of particles of appreciable initial volume | 1 – 1.5 |
| Needles and plates of finite long dimensions, small in comparison with their separation | 1 |
| Thickening of long cylinders /needles, (e.g after completion and impingement) | 1 |
| Thickening of very large plates (e.g after complete edge impingement) | 0.5 |
| Precipitation on dislocations (in the very early stages) | ~ 0.666 |

Figure 3.8 shows the $\ln(-\ln(1-\chi))$ and $\ln t$ curves for each sample. A good linear relationship was obtained in each case. The slopes of these plots correspond to the Avrami coefficients as the function of thickness are listed in Table 3.5.

According to Table 3.5, it is obvious that GeSbTe films thicker than 20 nm

experienced a crystallization process in which grain growth occurred with nucleation. Its nucleation rate decreased with the grain growth. When the film thickness was reduced to 10 nm, the grain only grew in a parallel dimension and the thickening of long cylinders (needles) occurred. When the thickness was reduced to 5 nm, the thickening of very large plates (e.g. after complete edge impingement) occurred.

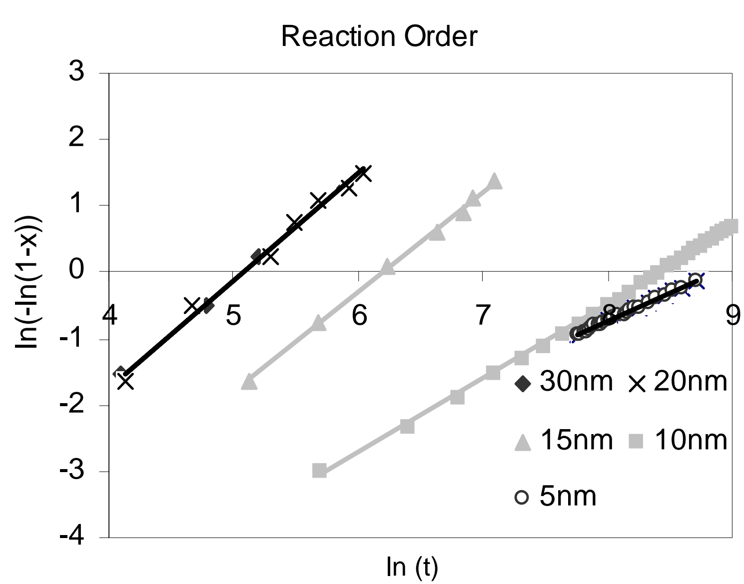



Fig. 3. 8 Avrami plot of ultra-thin $Ge_2Sb_2Te_5$ films derived by ITTM measurements and the slopes of these plots found to correspond with the Avrami coefficients.

Table 3. 5 Avrami coefficients (n) for ultra-thin $Ge_2Sb_2Te_5$ films.

| thickenss | 5nm | 10nm | 15nm | 20nm | 30nm |
|---|---|---|---|---|---|
| n | 0.85 | 1.118 | 1.501 | 1.616 | 1.621 |

## 3.4 Summary

In this chapter, the interface effect on phase change process mentioned in Chapter 2 was studied in more details. A thickness dependent nano-crystallization phenomenon in

ultra-thin films was systematically investigated. An increased crystallization point and decreased crystallization speed were observed with the down scaling of film thickness. In films thicker than 20 nm, the crystallization points are kept around 154 ˚C at the heating rate of 10 ˚C/min. However, when the thickness of films keeps scaling, the crystallization point can reach 166 ˚C at the same heating rate.

Based on ETTM and ITTM results, the thickness dependent crystallization mechanism is discussed. Using the Kissinger plot, the crystallization activation energy was found to increase in ultra-thin films with decreased film thickness. A model based on thickness dependent interfacial energy is used to explain this phenomenon. In this model, the interfacial energy was found to be correlated with the film thickness in ultra-thin films: the thinner the phase change thin films, the higher the interfacial energy. Therefore, the increasing interfacial energy causes the nucleation barrier to increase thus causing crystallization temperature to increase. Furthermore, an exponential relationship between crystallization temperature and thickness was found in films thinner than 20 nm. According to the JMA equation, it was found that crystallization kinetics changed in ultra-thin films, i.e. when the film was reduced to approximately 10 nm, the grain only grew in parallel dimension and the thickening of long cylinders (needles) occurred. When the thickness was reduced to 5 nm, the thickening of very large plates (e.g., after complete edge impingement) occurred.

Above results of thickness dependent crystallization can be used to analyze the performance of PCRAM devices when the phase change area is reduced to nano-scale.

# CHAPTER 4
# SUPERLATTICE-LIKE PHASE CHANGE STRUCTURE

Recently, to improve the scalability of PCRAM, material engineering has attracted great interests from the industry. Dopping phase change material is the mostly used method to engineer materials' properties. However it is challenging for single compound to meet the requirements of a particular application. One approach for material engineering is superlattice-like (SLL) phase change structure, which forms the artificial structure by alternatively depositing two phase-change materials with different electrical, thermal or crystallization properties. Rather than doping, the interface effect and nano-effect are utilized in this structure to customize the material properties. In this chapter, the electrical, crystallization and thermal properties of SLL phase change structure are investigated. Furthermore, developed from the SLL structure, a new category of superlattice, crystalline-amorphous superlattice (CASL), is proposed.

## 4.1 Introduction

As a fundamental PCRAM topic, material engineering on phase change materials constantly attracts intense interest. The most popular phase change material is the GeTe-$Sb_2Te_3$ pseudobinary system, which possesses a good combination of high speed, good stability and a proper crystallization temperature (Yamada, 1991).

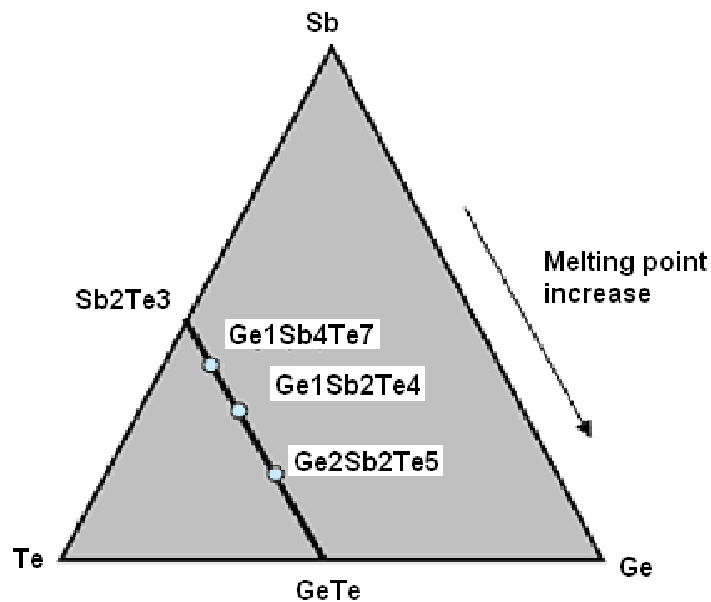



Fig. 4. 1 The GeTe-$Sb_2Te_3$ pseudobinary system, the compounds on the line between $Sb_2Te_3$ and GeTe are the most popular materials used in phase change technologies.

$Sb_2Te_3$ has a rhombohedral lattice of the tetradymite ($Bi_2Te_2S$) type (space group R3m) in the hexagonal configuration, of which the hexagonal unit cell contains three five-layer packets (Anderson, 1974; Sehr, 1962). Because these five-layer packets are bonded to each other by a weak Van der Waals force, $Sb_2Te_3$ has a relatively low crystallization temperature between 80 $^{o}$C and 100 $^{o}$C. It has a small band gap of 0.21 eV at the temperature of 300 K. Thus, it has a high crystallization speed but poor stability.

On the other hand, the crystalline state of GeTe has a slightly rhombohedrally deformed NaCl type structure at room temperature. It is made up of six stacked cyclic layers; -Te-Ge-Te-Ge-Te-Ge- (Karpinsky, 1998; Bahl, 1969). However, it has a large band gap of 0.73 ~ 0.95 eV at the temperature of 300 K which results in a high crystallization temperature of 189 $^{o}$C and a high melting point of about 700 $^{o}$C. GeTe has very stable crystalline state but a slow crystallization speed.

Because $Sb_2Te_3$ and GeTe have constrains on high stability and crystallization speed respectively, other popular compounds $GeSb_4Te_7$, $GeSb_2Te_4$ and $Ge_2Sb_2Te_5$ in this pseudo-binary system are proposed for data storage. As shown in Fig. 4. 2, $GeSb_4Te_7$ has 12 stacked cyclic layers -Te-Sb-Te-Te-Sb-Te-Ge-Te-Sb-Te-Te-Sb-; $GeSb_2Te_4$ has 21 cyclic layers -Te-Te-Sb-Sb-Te-Te-Ge-Te-Te-Sb-Sb-Te-Te-Ge-Te-Te-Sb-Sb-te-Te-Ge-; and $Ge_2Sb_2Te_5$ has 9 cyclic layers -Te-Sb-Te-Ge-Te-Te-Ge-Te-Sb- in their thermal equilibrium (Yamada, et.al, 1991). Based on the similar atomic arrangement with GeTe, the values of band gap for these three compounds are much larger than $Sb_2Te_3$, therefore, these compounds have very good stability.

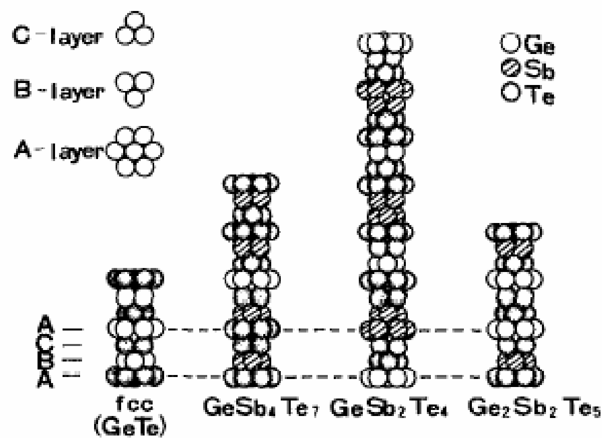



Fig. 4. 2 Stacking models of three ternary compounds in GeTe-$Sb_2Te_3$ pseudobinary system and GeTe (Yamada, et. al., 1991).

At the same time, a high crystallization speed is maintained in these compounds. Firstly, the fcc structure of crystalline state has a high grade symmetry which is most similar to the amorphous structure having an isotropic atom distribution. Therefore, phase change can be completed without appreciable atomic movement. Secondly, the films of

the pseudo-binary system can be crystallized without any phase separation with the compositions that varies along the line. Thus the composite atoms in the amorphous state do not need to travel long distance to be fixed into the crystal lattice. Thirdly, the DSC measurement results indicated that the difference between the free energy of the amorphous state and that of fcc crystal state in these compounds is large; this large free energy difference becomes the motive force for the fast crystallization (Yamada, et. al, 1991).

Although ongoing researches and development have proven the great potential of GeTe-$Sb_2Te_3$ pseudo-binary system, there are still several issues. One issue is that the programming current and crystallization speed of the PCRAM devices, currently using the materials in GeTe-$Sb_2Te_3$ pseudo-binary system, have not been improved to an ideal level. Especially the programming speed is still far behind the SRAM and processor. Another more general issue is natural constrains in single compound by the contradictory phase change properties requested by applications, such as speed and stability (Chong, et. al, 2006). Hence, it is very important to explore new phase change materials.

One possible approach is to make phase change materials with artificial structures. A SLL structure for phase change materials has recently been proposed and is in active development (Chong, et. al., 2002; Chong, et. al., 2006; Chong, et. al., 2007).

## 4.2 SLL Phase Change Structure

As shown in Fig. 4.3, the basic concept of SLL is to alternatively deposit two phase change materials, each with different electrical, thermal, and crystallization characteristics. This structure was firstly proposed by Chong in 2002 for optical

recording in order to increase the crystallization speed and data transfer rate (DTR). In their experiments, GeTe and $Sb_2Te_3$ thin films were alternatively deposited to form the recording layer. The phase change optical disk with the SLL structure and red light demonstrated an excellent recording property with the DTR as high as 140 Mbit/s, comparable with when the blue light is used (Chong, et. al., 2002). Another research also reported that the SLL phase change optical disc demonstrated a better recording performance than the $Ge_1Sb_2Te_4$ and $Ge_1Sb_4Te_7$ discs in terms of CNR, erasability, and overwrite jitter (Qiang, et. al., 2004).

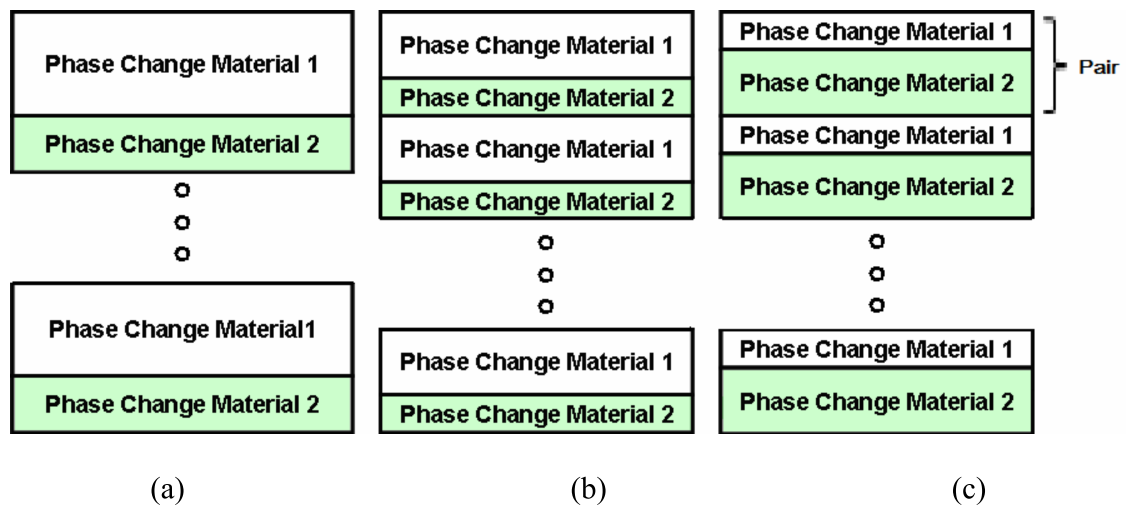



Fig. 4. 3 SLL phase change material structure and the structural engineering of SLL medium (a) 2-pair SLL structure (b) 3-pair SLL structure (c) 3-pair SLL structure with compositionally different artificial structure.

SLL structure provides a new approach for the material engineering to improve the performance of semiconductor memories when it is used in PCRAM technology. By the artificial structure, rather than doping, it utilizes the interface effect and nano-effect to customize the material properties. However, the detailed results about the relationship between different artificial SLL structures and material properties have not been reported yet. This chapter would focus on the structure engineering of SLL structure, by using

different number of pairs of $Sb_2Te_3$/GeTe as shown in Fig. 4.3 (a) and (b), or by changing the proportion of two different materials as shown in Fig. 4.3 (b) and (c). The crystallization and electrical properties of different SLL structures will be explored. Furthermore, the thermal properties of SLL structure will be discussed.

### 4.2.1 Electrical Properties

ETTM measurement is proven to be an effective way to investigate the electrical properties of phase change material (Trappe, et. al, 1998; Ohshima, et. al, 1996; Wei, et. al., 2006). The samples with different SLL structures were fabricated and tested by ETTM experiment setup as shown in Fig. 3.2. In this experiment, SLL structures with different pairs of $Sb_2Te_3$/GeTe and with different artificial structural composition were fabricated and compared. The $(Sb_2Te_3)_n(GeTe)_1$ artificial structural composition was formed by alternatively depositing GeTe and $Sb_2Te_3$ according to a certain proportion. The compositional artificial structure is called SLL_$Ge_1Sb_{2n}Te_{3n+1}$ correspondingly, eg. SLL_$Ge_2Sb_2Te_5$, SLL_$Ge_1Sb_2Te_4$ and SLL_$Ge_1Sb_4Te_7$. The thickness of $Sb_2Te_3$ and GeTe thin films can be calculated by density and molecular weight based on the equation:

$$t(Sb_2Te_3)/t(GeTe) = n \times M(GeTe) \times d(Sb_2Te_3)/d(GeTe) \times M(Sb_2Te_3) \qquad (4.1)$$

Where, n is the compositional proportion between $Sb_2Te_3$ and GeTe; $t(Sb_2Te_3)$ and $t(GeTe)$ are thickness of $Sb_2Te_3$ and GeTe respectively. $M(GeTe)$ and $M(Sb_2Te_3)$ are the molecular weight of $Sb_2Te_3$ and GeTe, which are 200.21 g/mol and 626.3 g/mol, respectively; $d(Sb_2Te_3)$ and $d(GeTe)$ are the densities of $Sb_2Te_3$ and GeTe, which are 5.785 g/cm$^3$ and 6.426 g/cm$^3$, respectively.

The schematic cross-section of the SLL samples is shown in Fig. 4.4. The thickness

of all the samples is kept as 50 nm. Because the pairs (Fig. 4.4) of the samples are changed from 4 to 12 and because the limitation on the minimum thickness by sputtering capability, SLL_$Ge_6Sb_2Te_9$ and SLL_$Ge_2Sb_2Te_5$ structures are chosen in this experiment to guarantee the film uniform. TiW electrodes fabricated under SLL structure for the electrical measurement are 100 nm thick. $Sb_2Te_3$ and GeTe thin film was deposited by BALZERS sputtering machine with power of 0.08 KW and Ar flow rate of 15 sccm. The deposition rate was as low as 0.98 nm/s and 1.01 nm/s for $Sb_2Te_3$ and GeTe, respectively. 50 nm ZnS-$SiO_2$ was grown on top of the sample to prevent SLL structure from oxidation. After fabrication, the sample was annealed at 120 $^{o}$C for 2 min on hot plate, the process that is included in the PCRAM device fabrication. Because the crystallization temperature of $Sb_2Te_3$ is lower than 100 $^{o}$C, $Sb_2Te_3$ layer is expected to be in poly-crystalline state after the annealing (Wei, et. al., 2004).

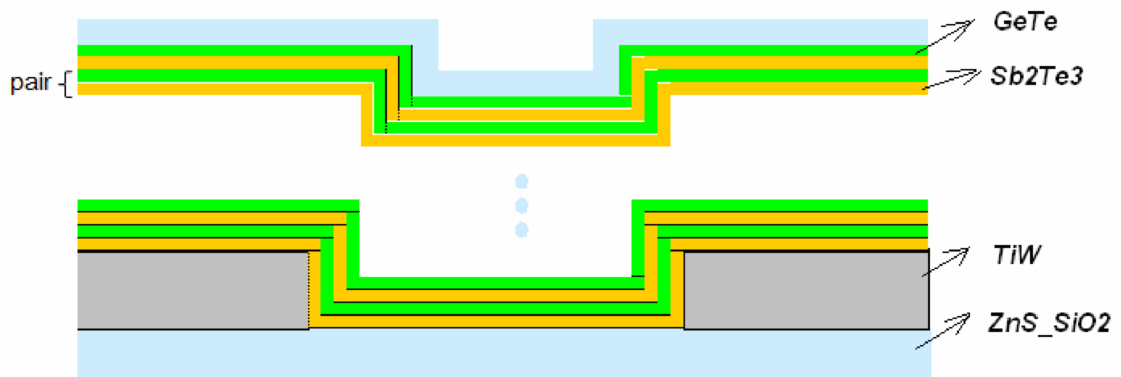



Fig. 4. 4 Schematic cross-sectional view of SLL sample in ETTM measurement.

#### 4.2.1.1 Layer Dependent Effect

In this experiment, SLL_$Ge_6Sb_2Te_9$ structures with different pairs of GeTe/$Sb_2Te_3$

thin films were firstly studied. $Ge_6Sb_2Te_9$ is on GeTe-$Sb_2Te_3$ pseudo-binary line with the composition of $(Sb_2Te_3)_1$ and $(GeTe)_6$. The total thickness of SLL structure is 50 nm for all the samples with $Sb_2Te_3$ deposited firstly. The number of pairs is changed from 4 to 12 in the samples. When the sample has 12 pairs, the thicknesses of $Sb_2Te_3$ and GeTe films in each pair are 1.599 nm and 3.401 nm, respectively. Based on Equ. 4.1, the pairs and thickness of the GeTe/$Sb_2Te_3$ thin film are calculated and listed in Table 4.1.

Table 4. 1 The parameters of phase change thin films in artificial compound SLL_ $Ge_6Sb_2Te_9$ structure.

| SLL-$Ge_2Sb_2Te_5$ | No. of pairs | $Sb_2Te_3$ | GeTe |
|---|---|---|---|
| Sample 1 | 4 | 3.997 nm | 8.503 nm |
| Sample 2 | 6 | 2.664 nm | 5.669 nm |
| Sample 3 | 8 | 2.000 nm | 4.252 nm |
| Sample 4 | 10 | 1.599 nm | 3.401 nm |
| Sample 5 | 12 | 1.332 nm | 2.834 nm |

The electrical resistance measured by ETTM is shown in Fig. 4.5. During the experiment, the temperature was raised from room temperature to above 200 $^oC$ at a heating rate of 10 $^oC$/min. All the samples showed standard thermal crystallization process as observed in other chalcogenide materials. The electrical resistance was larger than $10^5$ ohm until the temperature was raised above 150 $^oC$. Then the electrical resistance dropped quickly to 1 Kohm in less than 15 seconds. This decrease was due to the crystallization process. A layer dependent effect was observed in this process. It is obvious that for structure with more pairs and thinner films, the crystallization happened at higher temperature. Furthermore, the values of electrical resistance (inset of Fig.4.5) before the crystallization process are dependent on the number of layers. At the

temperature of 70 °C, the electrical resistances of 4-pair, 6-pair, 8-pair, 10-pair and 12-pair structures were 18 Mohm, 34 Mohm, 39 Mohm, 48 Mohm and 52 Mohm, respectively. Therefore, it can be deduced that the electrical resistance of SLL_$Ge_6Sb_2Te_9$ structures would increase with an increase of pairs of thin films. However, it is also worthy to note that the increase of electrical resistance would saturate when the structure has more than 10 pairs. The resistance increased 88% when the structure changed from 4-pair to 6-pair, while it increased only 8.3% when the structure changed from 10-pair to 12-pair.

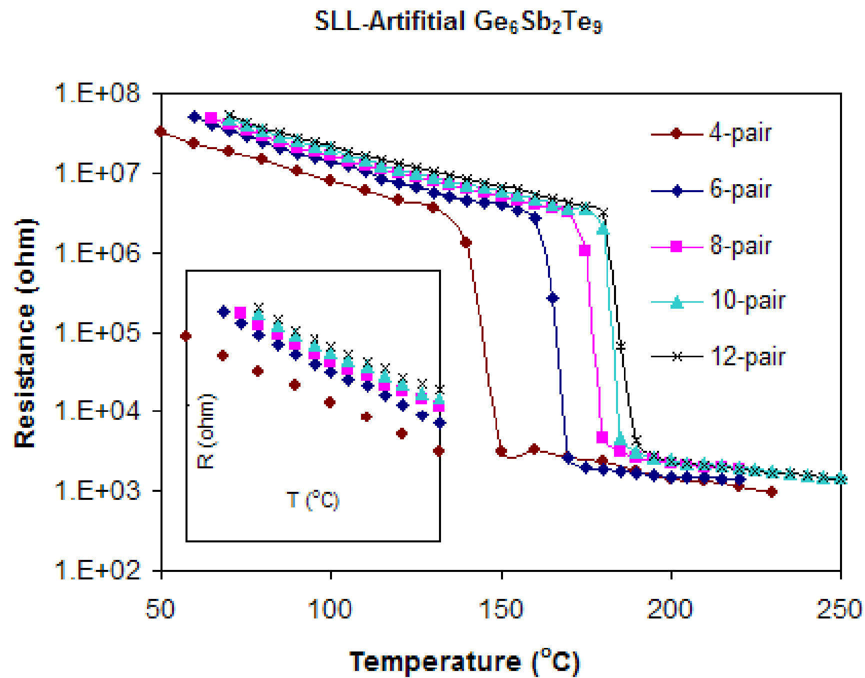



Fig. 4. 5 ETTM measured electrical resistance of the SLL-$Ge_6Sb_2Ge_9$ structures during annealing.

It is believed that the layer dependent electrical resistance is caused by the interface effects in those structures. In multi-layer structure, it has been reported that the roughness of the interfaces between layers would cause additional scattering resistivity to the

material (Levy, et. al. 1990). Therefore, the material with more interfaces would have higher electrical resistivity because of the additional interfaces. It was also reported that, in superlattice structure, electrical properties were found to be dependent on the pairs of thin film and thickness of the incorporated materials: the more pairs and the thinner of the incorporated material, the higher the resistivity (Esaki, 1986).

Since SLL has the layer dependent electrical resistance similar to SL and other multi-layer structure, the electrical properties of SLL structure can be designed by changing the thickness and pairs of layers of SLL structure.

### 4.2.1.2 Compositional Dependent Effect

To study the influence of artificial composition on the electrical properties and crystallization properties, samples with the artificial composition of SLL_$Ge_2Sb_2Te_5$ are also fabricated. It can be viewed as combination of $(Sb_2Te_3)_1$ and $(GeTe)_2$ components. ETTM results of SLL_$Ge_2Sb_2Te_5$ are compared with those of SLL_$Ge_6Sb_2Te_9$, which can be viewed as combination of $(Sb_2Te_3)_1$ and $(GeTe)_6$. The total thickness phase change material in SLL_$Ge_2Sb_2Te_5$ is still 50 nm for all the samples with $Sb_2Te_3$ deposited firstly. The number of pairs is changed from 4 to 12 in the samples. Based on Equ. 4.1, when the sample has 12 pairs, the thicknesses of $Sb_2Te_3$ and GeTe films in each pair are 2.436 nm and 1.730 nm, respectively. The detailed thickness and number of pairs of SLL_$Ge_2Sb_2Te_5$ samples are listed in Table 4.2. The ETTM plots in Fig. 4.6 show the layer dependent effect as well that (1) SLL with less pairs crystallized at lower temperature; (2) the more the pairs of thin films, the higher the resistance of amorphous states.

Table 4. 2 The parameters of phase change thin films in SLL-$Ge_2Sb_2Ge_5$ structure.

| SLL-$Ge_2Sb_2Te_5$ | No. of pairs | $Sb_2Te_3$ | GeTe |
|---|---|---|---|
| Sample 1 | 4 | 7.309 nm | 5.183 nm |
| Sample 2 | 6 | 4.873 nm | 3.461 nm |
| Sample 3 | 8 | 3.655 nm | 2.595 nm |
| Sample 4 | 10 | 2.924 nm | 2.076 nm |
| Sample 5 | 12 | 2.436 nm | 1.730 nm |

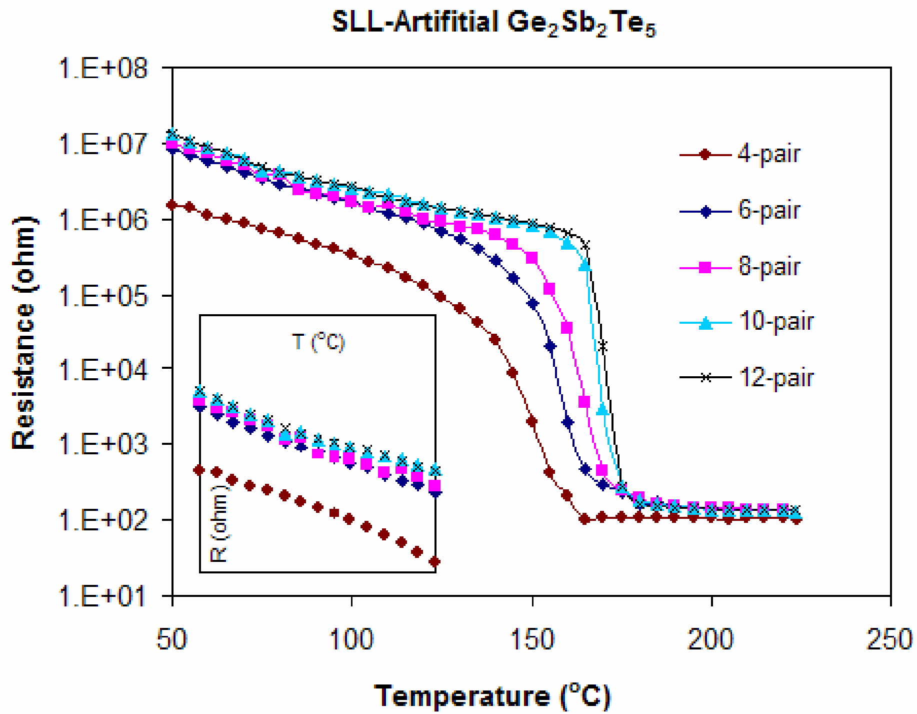



Fig. 4. 6 ETTM measured electrical resistance of the SLL-$Ge_2Sb_2Ge_5$ structures during annealing.

Furthermore, when the electrical resistances of SLL_$Ge_6Sb_2Te_9$ and SLL_$Ge_2Sb_2Te_5$ are compared, a compositional dependent effect is observed. Firstly, the electrical resistance dropped during crystallization of SLL_$Ge_2Sb_2Te_5$ at the temperatures ranged from 140 °C to 160 °C, much lower than those for SLL_$Ge_6Sb_2Te_9$. Secondly, the slope of the resistance decrease during crystallization was more gradual in SLL_$Ge_2Sb_2Te_5$, which

took longer than 40 seconds. Thirdly, the electrical resistance of SLL_$Ge_2Sb_2Te_5$ was lower than SLL_$Ge_6Sb_2Te_9$ as a whole as shown in Fig. 4.7. At 70 °C, the electrical resistance of 12-pair SLL_$Ge_2Sb_6Te_9$ was 52 Mohm while the 12-pair SLL_$Ge_2Sb_2Te_5$ was 6 Mohm.

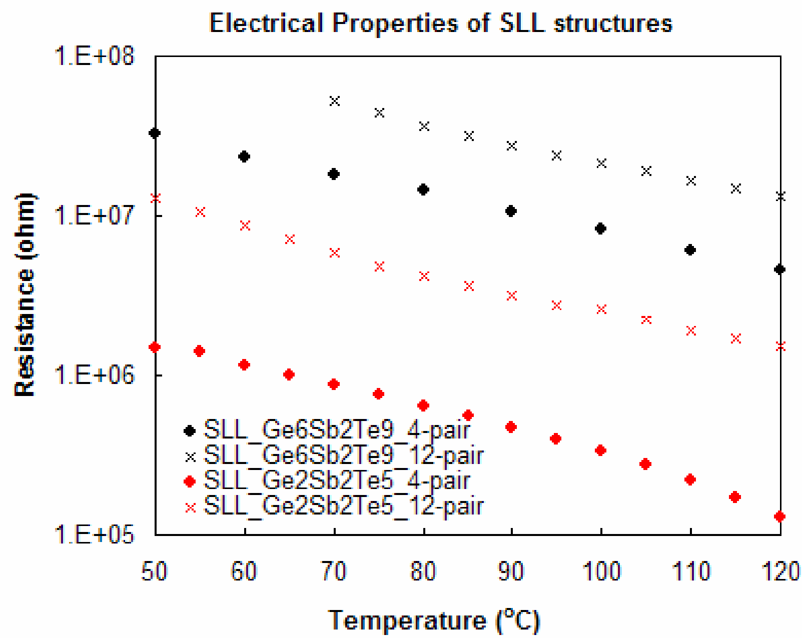



Fig. 4. 7 Compositional dependent effect in ETTM measured electrical resistance of the SLL_$Ge_6Sb_2Ge_9$ and SLL_$Ge_2Sb_2Te_5$ structures.

## 4.2.2 Crystallization Properties

Crystallization temperature $T_x$, determined as the minimum temperature in the first derivative obtained by (dR/dT), is shown in Fig. 4.8. The layer dependent and compositional dependent effects were both observed in crystallization properties. For the same compositional SLL structure, it is obvious that $T_x$ increased with an increased number of pairs. For SLL_$Ge_6Sb_2Te_9$, $T_x$ grew from 140˚C to 180˚C when the number of

pairs was increased from 4-pair to 12-pair. Additionally, all SLL_$Ge_6Sb_2Te_9$ samples showed a fast crystallization process according to its steep decrease of electrical resistance as shown in Fig. 4.8 (a). However, when the pair number kept increasing, the increase of $T_x$ became saturated. Similar layer dependent effect was also observed in SLL_$Ge_2Sb_2Te_5$ as shown in Fig. 4.8 (b).

When $T_x$ of SLL_$Ge_6Sb_2Te_9$ was compared with that of SLL_$Ge_2Sb_2Te_5$, compositional dependent effect was observed. $T_x$ of SLL_$Ge_2Sb_2Te_5$ was ranged from 140˚C to 160˚C when the number of pairs was increased from 4 to 12, which is much lower than those in SLL_$Ge_6Sb_2Te_9$ structure. Furthermore, the $T_x$ difference between two artificial structures is larger in samples with more pairs. For 4-pair structure, $T_x$ difference between SLL_$Ge_6Sb_2Te_9$ and SLL_$Ge_2Sb_2Te_5$ was within 5 ˚C. While for 10-pair structure, the $T_x$ difference between SLL_$Ge_6Sb_2Te_9$ and SLL_$Ge_2Sb_2Te_5$ was around 20 ˚C.

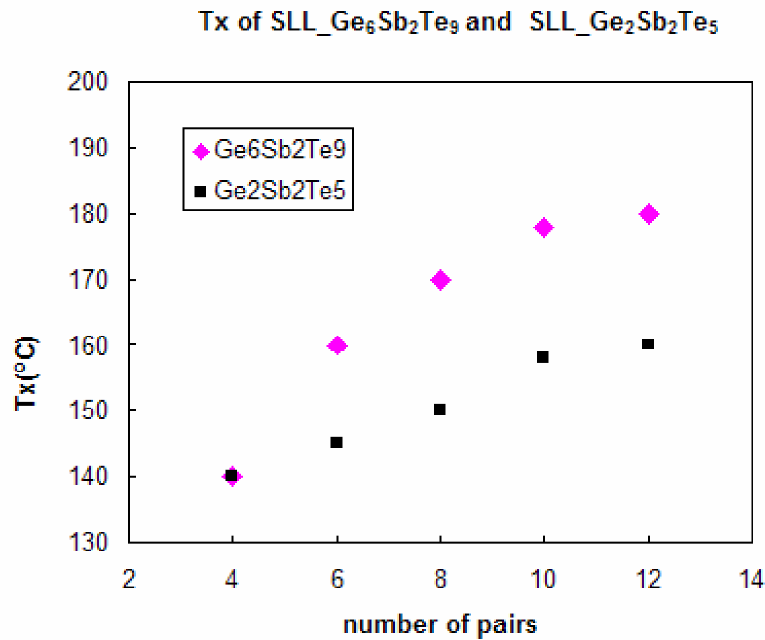



Fig. 4. 8 $T_x$ vs the number of pairs in the SLL_$Ge_6Sb_2Ge_9$ structures and SLL_$Ge_2Sb_2Te_5$ structures.

The nano-crystallization in ultra-thin film discussed in Chapter 3 can be used to explain the layer dependent effect on the SLL crystallization temperature. In bulk material, the crystallization is a nucleation followed by a subsequent growth (Senkader, 2004; Weidenhof et. al, 2001). However, the interface started to affect the crystallization when the film became very thin. Thickness dependent nano-crystallization in ultra-thin chalcogenide films was observed: the thinner films would have higher crystallization temperature (Wei, et. al., 2006; Shi and Chong, 2006). Therefore, samples with more pairs of SLL materials and thinner thin film would have higher crystallization temperature.

Furthermore, the SLL structure can enhance the crystallization speed of the phase change material. The material with high crystallization speed would crystallize firstly and

then act as an induced layer for the material with lower crystallization speed to enhance nucleation and crystal growth (Chong, et. al., 2007). The crystallization seed effect of $Sb_2Te_3$ film was also found in optical disc, in which $Sb_2Te_3$ film was used to make the initialization-free DVD discs (Wei, et. al., 2004). This seed effect can also be used to explain the compositional dependence of crystallization temperature, because SLL_$Ge_2Sb_2Te_5$ had a lower crystallization point than SLL_$Ge_6Sb_2Te_9$ for the same pairs of thin films.

### 4.2.3 Thermal Properties

The thermal properties of SLL structure are affected by the density, specific heat and thermal conductivity. The density and specific heat are quite similar for crystalline state and amorphous state in chalcogenide material (Chong, et. al., 2007). However, theoretical studies have revealed that the thermal conductivities along both in-plane and cross-plane directions deviate significantly from its constituent bulk materials (Chong, et. al., 2007). In conventional superlattice structure, the interface phonon scattering and phonon confinement effects in multilayer structure cause the lower thermal conductivity (Chen, 1996; Hyldaard, 1997; Tamura, 1999). Because similar multilayer structure existed in both SLL structure and conventional superlattice, the thermal conductivity in SLL structure compared to bulk material is believed to be mainly dependent on the interfaces and phonon scattering within the superlattice.

The thermal properties of superlattice structures have attracted great attention due to the importance of thermal control and management properties in microelectronics and semiconductor devices in both in-plane and cross-plane studies since 1980. Significant reductions in the in-plane and cross-plane thermal conductivities of superlattice have

been observed in studies (Yao, 1987; Yu, 1995; Venkatasubramanian, 2000).

In a direction parallel to the thin film plane of superlattice, Ren and Dow first studied on the thermal conductivity of superlattice (Ren, 1982), using a phenomenological model for bulk thermal conductivity and assumed that the phonon scattering processes can be represented by frequency-dependent relaxation to predict the additional temperature dependence on the thermal resistance of superlattice. Chen (Chen, 1996) established models based on thermal boundary resistance (TBR) to calculate the thermal conductivity of superlattice structures in parallel direction. Hyldgaard (Hyldaard, 1997) and Tamura (Tamura, 1999) studied phonon transport in supperlattices and found that total internal reflection confines the superlattice modes and significantly reduces the average group velocity at non-zero in-plane momenta. These consequences of the acoustic mismatch at high temperatures cause an order-of-magnitude reduction in the ratio of superlattice thermal conductivity by phonon relaxation.

In a direction perpendicular to the thin film plane of superlattice, Chen established the models of thermal conductivity and phonon transport, based on the phonon Boltzmann transport equation (BTE) (Chen, 1997). The results show that the effective thermal conductivity of superlattice in the perpendicular direction is generally controlled by phonon transport atom within each layer and the TBR between different layers. TBR is no longer an intrinsic property of the interface, but depends on layer thickness as well as the phonon mean free path. The thermal conductivity of superlattice is almost independent of the scattering mechanisms in bulk materials and is determined by the mismatch of specific heat, group velocity, and density of adjacent layers.

Besides the theoretical models discussed above to explain the thermal conductivity

reduction in superlattice and SLL structure, the experimental results on thermal conductivity of SLL phase change material also demonstrated 30% reduction compared to that of bulk material (Chong, et. al., 2006). Furthermore, the reduction of thermal conductivity and its effect on PCRAM device has been investigated by simulation. When the thermal conductivity was treated as both isotropic and anisotropic, the higher maximum temperature could be obtained using SLL structure (Chong, et. al., 2006, Chong, et. al., 2007). However, due to different interfaces and phonon scattering, SLL structure has higher possibility to display anisotropic thermal conductivity. In this case, when the thermal conductivity was reduced from 100% to 50% of the bulk, the temperature of the structure for the in-plane adjustment is increased from 610 $^{o}$C to 735 $^{o}$C. The temperature for the cross plane adjustment is increase from 506 $^{o}$C to 936 $^{o}$C. While the temperature for both-plane is increased from 481 $^{o}$C to and 1125 $^{o}$C (Chong, et. al., 2007). Therefore, by designing the SLL structure with different in-plane and cross-plane thermal conductivity, the thermal performance of the PCRAM cells based on SLL structure can be controlled and modified.

### 4.2.4 Discussion

SLL structure was proven to be a flexile medium, which can be designed to meet different requirements on electrical properties, crystallization properties and thermal properties. The interface effect and nano-effect in SLL provide good opportunities for material engineering.

In the following chapters, SLL phase change material will be applied to PCRAM technology. Based on the results above, the SLL_$Ge_2Sb_2Te_5$ structure with 6-pair $Sb_2Te_3$ and GeTe films was chosen because it has a good combination between fast

crystallization speed and low crystallization temperature. It is expected that a lower crystallization point may help to reduce programming power of PCRAM.

## 4.3 Crystalline-Amorphous-Superlattice (CASL)

In this section, a new category of superlattice structure, crystalline-amorphous-superlattcie (CASL), will be developed based on the SLL structure.

Semiconductor superlattice (SL) exhibits many attractive electric, optical and thermal properties that are associated with the periodic nature of the SLs of the repeat distance in the structure, such as quantum size effects (Esaki, 1970; Dingle, 1974; Smith, 1990). To date, there are mainly two types of superlattice (SL), crystalline SL and amorphous SL. Crystalline SL was the first to be produced. The matching of the lattice constants of the individual layers is the crucial requirement in fabrication of crystalline SL, which restricts the number of materials to form SLs. However, such strict requirement can be relaxed in amorphous SL due to amorphous structure by its very own nature. Amorphous SLs do not need the matching of the lattices (Abeles, 1983; Davis, 1995; Zeng, 2001). It has been demonstrated that uniformed multilayer of amorphous semiconductor can be fabricated with very thin component layer of sharp interfaces. Compared to crystalline SL, amorphous SL has much more freedom in choosing components of the SL structures, as there is no limitation by the lattice matching condition.

The combination of SL concept with phase change mechanism is expected to provide a new category of SL structure: CASL, which consists of two kinds of phase change materials, which are alternatively deposited. The component materials could be either at polycrystalline or amorphous phase. Depending on the phase of the component materials,

CASL displayed three different states: both in amorphous phases demonstrating an amorphous SL (a CASL); both in polycrystalline phases demonstrating a crystalline SL (c CASL); one in polycrystalline phase while the other one in amorphous phase, thus demonstrating a mix of amorphous and crystalline SL (m CASL). The key to fabricate CASL is to form defect free interface, which is highly dependent on the properties of the component materials, such as lattice constant, bonding, adhesion force, etc. In order to realize m-CASL state, it is desirable for the component materials to have a large difference in their crystallization temperatures $T_x$ (c). If the component materials are chosen appropriately, for example chalcogenide materials, which can realize reversible transition between amorphous and crystalline phases, CASL is capable of reversibly transition among the three states by using different means, e.g. electrical or laser pulse. The reversible phase transition in chalcogenide materials is due to that the top of the valence band consists of lone-pair orbits with lone-pair electron and hole, and the localized states in the gap which is caused by the interactions between lone-pair electrons on different atoms and interactions with their local environment (Ovshinsky, 1976; Bahl and Chopra, 1969).

**Sample Preparation**

In this study, CASL was fabricated on Si substrate using binary compounds of GeTe and $Sb_2Te_3$ as the two component materials, prepared by ion beam deposition system, Roth & Rau IonSys 1000. The base pressure was initially $3\times10^{8}$ mbar. During deposition, a microwave power of 243 W at 2.45 GHz, a beam voltage of 800 V and an accelerator voltage of -600 V were applied. Using Ar at a flow rate of 4 sccm, the pressure was increased to $9.2\times10^{-5}$ mbar. $Sb_2Te_3$ and GeTe were then deposited at rates of 7.3 nm/min

and 2.5 nm/min respectively. Each component layer was deposited alternatively with the same thickness varying from 1 to 20 nm. The thickness of a pair of GeTe/Sb2Te3 layers is called a period in this paper. For the CASL sample, 40 periods were grown.

**Superlattice structure and three states of CASL**

GeTe/$Sb_2Te_3$ CASL crystalline structure was characterized by X-ray diffractometry using CuK$\alpha_1$ radiation. For the as-deposited sample, no peak was observed, indicating that both GeTe and $Sb_2Te_3$ were at amorphous phase. When the sample was heated to 100 °C in vacuum for 5 minutes, a peak at 36.7° was observed, indicating that $Sb_2Te_3$ layer had crystallized. No peak for polycrystalline GeTe was observed, indicating that GeTe remained in amorphous phase. The state was a m-CASL. When the sample was further heated to 200 °C, an additional peak at 25.90° appeared which showed the existence of polycrystalline GeTe and $Sb_2Te_3$. The CASL was then a c-CASL.

The three states were confirmed by X-ray reflectometry (XRR) as shown in Fig. 4.9. The CASL period was designed to be 7 nm, and the 40 periods grown were capped with 4.3 nm thick ZnS-$SiO_2$ layer. From Fig. 4.9, it can be seen that the three states all exhibit sharp satellite diffraction peaks. The full width at half-maximum (FWHM) of the diffraction peak on the diffraction angle θ bears the information on the interfacial abruptness. For a-CASL, FWHM is 0.07 ° for the peak at θ = 0.645 °, which corresponds to a period of 7.73 nm. It shows that a well-defined amorphous SL was obtained at a-CASL state; for m-CASL, FWHM is 0.07 ° for the peak at θ = 0.652 °. The increase of the peak angle is due to the decrease in period to 7.62 nm and increase in $Sb_2Te_3$ density from 6.05 g/cm$^3$ to 6.26 g/cm$^3$ during the crystallization; For c-CASL FWHM is 0.05 ° for the peak at θ = 0.688 ° which corresponds to a period of 7.13 nm. It reveals that the

period of c-CASL is the smallest. After fitting the XRR data, the density was found to increase from 6.05 g/cm$^3$ to 6.44 g/cm$^3$ for $Sb_2Te_3$ and from 5.10 g/cm$^3$ to 5.33 g/cm$^3$ for GeTe. These results show that the density of crystalline phase is larger than that of amorphous phase. The small FWHM for the three peaks showed that well-defined SL has been obtained in all three states of CASL.

Furthermore, by properly choosing the component materials and the method to induce their phase transitions, reversible changes among the three states of CASL could be achieved by electrical pulses (Chong, et. al, 2008).

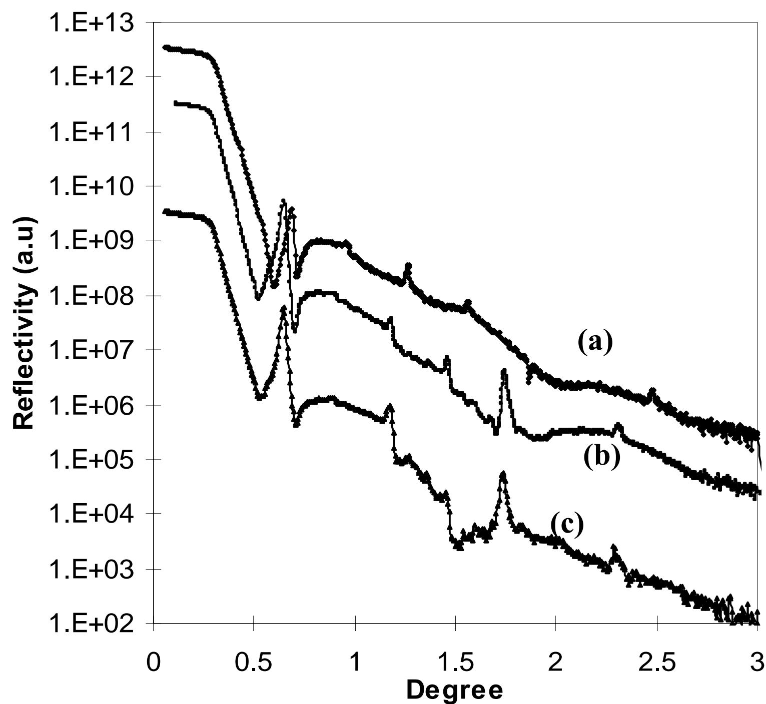



Fig. 4. 9 Small angle X-ray diffraction results: (a) as deposited samples (b) the sample was heated to 100°C in an vacuum furnace for 5 minutes, (c) the sample was heated to 150°C in an vacuum furnace for 5 minutes.

**Quantum effect in CASL**

To study the quantum effect in CASL, the optical properties of CASL at different

states were also studied by measuring normal incident reflection and transmission that are determined by the ordinary refractive index no in the range of 0.4 to 1.2 eV. The values of the band gap as a function of the component thickness were measured for the CASL at different state. Fig. 4.10 shows the absorption edge values that were influenced by quantum well confinement for layer thickness less than 10 nm obtained for m-CASL. The blue shift of absorption edge was obviously observed. Similar blue-shifts were also observed for c CASL and a-CASL. The absence of any concrete information about the modulation profiles of the valence and conduction band edges, or about electron and hole effective masses, prevents an exact comparison of the measured blue shift with calculation. Nevertheless, the magnitude of the shift and the layer thickness values at which it sets in can be modeled with a square-wave modulation of band edge (Bittar, et.al. 1989). This model demonstrates that the variation in blue shift with layer thickness is indeed a quantum size effect.

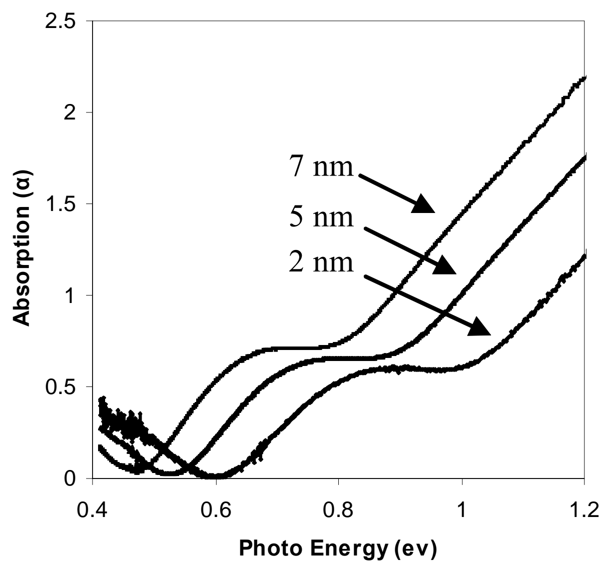



Fig. 4. 10 Blue shift of absorption edges in m-CASL structures.

## 4.4 Summary

The crystallization, electrical and thermal properties of SLL phase change structure were studied in this chapter. Experimental and theoretical evidences show that the crystallization and electrical properties are layer dependent: the more pairs and thinner of the films, the higher crystallization temperature and higher electrical resistance the SLL structure would have. The 4-pair structure showed an obvious different thermal electrical properties and phase change process compared to 6-pair structures and above. When the number of pairs is larger than 10, the change of crystallization process and electrical resistance became saturate. Furthermore, compositional dependent was observed on different artificial structures. SLL_$Ge_2Sb_2Te_5$ has lower crystallization temperature, slower crystallization speed, and lower electrical resistance compared to SLL_$Ge_6Sb_2Te_9$. Physical mechanisms behind these electrical, crystallization and thermal properties of SLL structure were discussed. This SLL structure was proven to be a flexible structure which can be designed to meet various requirements on the different considerations.

In addition, a new class of semiconductor SL, crystalline-amorphous CASL, has been synthesized by alternatively depositing two semiconductor materials such as GeTe and $Sb_2Te_3$. The CASL displays three different states depending on the phase of each component materials: both in polycrystalline phase and both in amorphous phase, and one in polycrystalline phase while another in amorphous phase. Small angle X-ray was used to prove their existence. A blue shift on the optical absorption edge were observed and interpreted as quantum or nano-effects.

# CHAPTER 5
# Integrated Circuit Design of 128 Bit PCRAM Chip

To verify the current reduction capability of SLL structure memory devices, a 128 bit PCRAM chip is designed in this chapter. The Integrated Circuit (IC) design of the memory chip is very critical because it is closely related to the performance, cost, and stability of devices. However, for emerging technologies, IC design faces the challenge to integrate the innovative element model to conventional IC simulators. The other challenge is to determine the special IC design requirement from the new technology. This chapter will present the studies on the IC modeling of PCRAM memory cells and propose a full circuit design for a 128-bit PCRAM chip.

## 5.1 Introduction of Memory IC Design

The development of the microelectronics chip includes the IC design, prototype manufacturing and testing (Fig. 5.1). The IC design is the first step and it consists of defining circuit inputs and outputs, building schematics, circuit simulations, and the layout of the circuit (Baker, et.al, 1998). The design of the semiconductor memory should go through the same procedure. Fortunately, the architecture of binary RAM chip is well established. RAM requires that every single bit should have its individual memory locations/ address randomly accessed either for reading or writing (Martin, 1999). A control line, often designated as $R/\overline{W}$, determines whether a storage cell in the RAM is

being read from or written into the storage cell. Although the design for high-capacity or high-speed are much more complicated, the basic architecture and principle of each block are similar. Because the main purpose of SLL_PCRAM chip in this experiment is to demonstrate the functionality of SLL structure, only basic functions are included in the design.

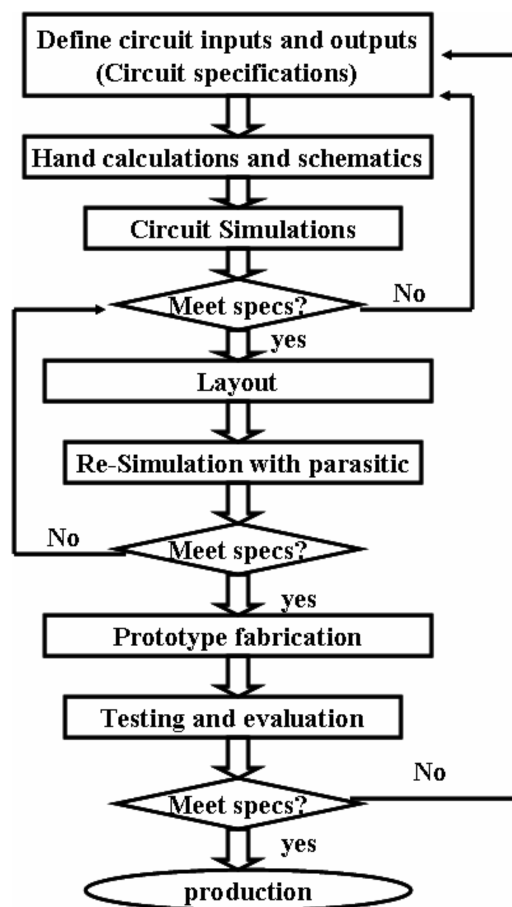



Fig. 5. 1 Integrated circuit design flow chart.

Besides the contents listed in the design flow shown in Fig. 5.1, non-silicon or innovative technology may request an additional work: device modeling. Circuit

simulation is based on the models of included elements: resistors, capacitor and MOSFET. These models affect the accuracy, time and costs of the simulation (R. J. Baker, et.al, 1997). Generally, there are two kinds of models: the physical model and macromodel. The physical model is based on the mathematical equation of physical mechanisims, such as the internal electrical field, the thermal field, and the magnetic field. It could be accurate but sometimes complicated. For CMOS technology, the Berkeley short-channel model has become industry standard (Sheu, et.al, 1987). For some innovative devices, when the physical mechanisms are not clearly defined, it is not easy to develop an accurate physical model. Macromodels are utilized for this situation. The macromodel treats the object as a black box, using simple equations to simulate the performance of whole block. It saves the simulation time but has trade-off on the accuracy and flexibility.

For the design of PCRAM chips, there is no available model of phase change memory cells in the simulator's standard category. Although there has been substantial progress in the modeling of threshold switches and phase distribution (Pirovano, et. al, 2004 and Ielmini, et. al, 2004), there are still many unclear mechanisms in the PCRAM operation. Therefore, it is not easy to make an exact physical model, thus a macromodel is needed. Although a SPICE macromodel was developed by researchers to simulate the I-V curve of the PCRAM element (Cobley et. al, 2003), it was inflexible for the various device structures because its internal mapping functions were generated from the experimental data, rather than the structure parameters. The macromodel developed in this thesis treats the PCRAM memory cells as simple resistors. Meanwhile, it includes physical mechanisms in the operation, such as the threshold switch and the crystallization process. Therefore, this macromodel combines the flexible advantage of a physical model and the

simple advantage of the macromodel.

The vertical structure (Fig. 5. 2) is utilized in the proposed macromodel. The phase change material ($Ge_2Te_2Sb_5$) is sandwiched between two TiW electrodes, and the temperature of the active region can be raised to a high value by Joule heat generated by electrical pulse (Maimon, 2001). The PCRAM element is treated as a resistance-changeable resistor. Temperature and crystallization fractions were the two parameters determining the resistance of the elements. This model aims to provide the SET, RESET and READ functions.

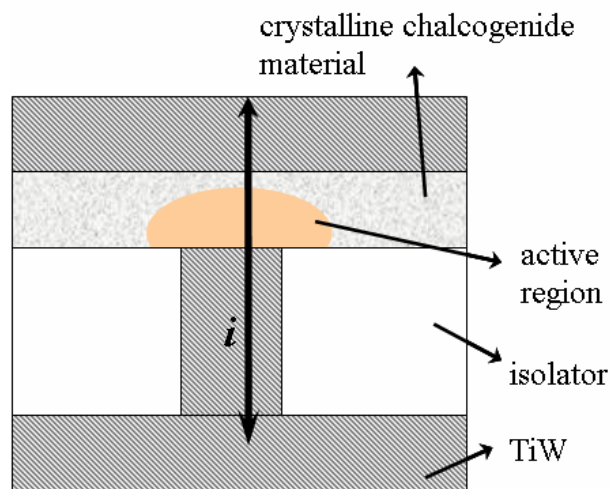



Fig. 5. 2 Schematic structure of the PCRAM element, the active region is the red area above the bottom electrode.

During the RESET operation, the current pulse should be relatively high to raise the temperature above the melting point of the chalcogenide material. At melting point, all crystalline structures are expected to disappear in this model. After that, the material changes to the amorphous state.

The SET operation is more complicated, because it includes two mechanisms: the threshold switch and the memory switch (Tyson et. al, 2000). During the threshold switch,

the resistance will be reduced to a very low transient value by the breakdown effect when the electrical field across the amorphous phase change material is higher than a certain value. This low transient resistance allows a noticeable current to pass through the material, so that the temperature can be raised above the crystallization temperature (≥ 200ºC). Then the material begins to crystallize after the threshold switch. The crystallization percentage is calculated to determine the resistance the memory cell would have.

When a current pulse is used to read PCRAM elements, there is a large difference in voltage between the readings of the crystalline state and the amorphous state. It should be noted that this reading pulse must be low enough to avoid erasing existing data.

The macromodel described below is to simulate the physical mechanisms described above. This model was based on a Simulation Program with Integrated Circuit Emphasis (SPICE) simulator. This powerful and general-purpose program is the most popular circuit analysis program for simulating analog circuits. It was developed by the Integrated Circuit Group of Electronics Research Laboratory and the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley, in the late 1960s. Over the years, SPICE has experienced many updates and there are more than 35 SPICE derivative programs, including the HSPICE (from Meta-software) used in this work.

## 5.2 HSPICE Modeling of PCRAM Cells

### 5.2.1 Binary Macromodel of PCRAM

The macromodel, acting as the black box, is realized as a two-terminal sub-circuit in

the HSpice simulator. The current is forced into this model, then the generated joule heat is calculated and temperature is determined. In addition, the crystalline percentage in the phase change active region is monitored. Based on the temperature and crystalline percentage, the resistance of the model is decided and the corresponding resistor is connected to the external circuit. In binary storage, two resistors with different resistances are included to represent the complete amorphous and the complete crystalline state. It can be observed from the simulation flow chart in Fig. 5.3, that when the temperature is higher than the melting point (Tm), the switch connected to high resistance resistor is turned on, while when the crystal fraction in the active region reaches the threshold value (set as 100% in this model for a complete crystalline condition), the switch to the low resistance resistor is turned on. The proposed macromodel, as shown in figure 5.4, consists of three circuits: (1) bi-stable circuit, (2) phase change circuit, (3) logical control circuit.

#### 5.2.1.1 Bi-stable circuit

In this circuit, two resistors $R_m$ and $R_x$ are used to represent the amorphous state and crystalline states; the control signals from logical control circuit determine which resistor should be connected into the circuit. In this macromodel, Voltage Controlled Resistors (VCR), whose resistance can change from 0.001ohm to 100M ohm with the control voltage, have the function as switches (e.g. $S_m$, $S_x$).

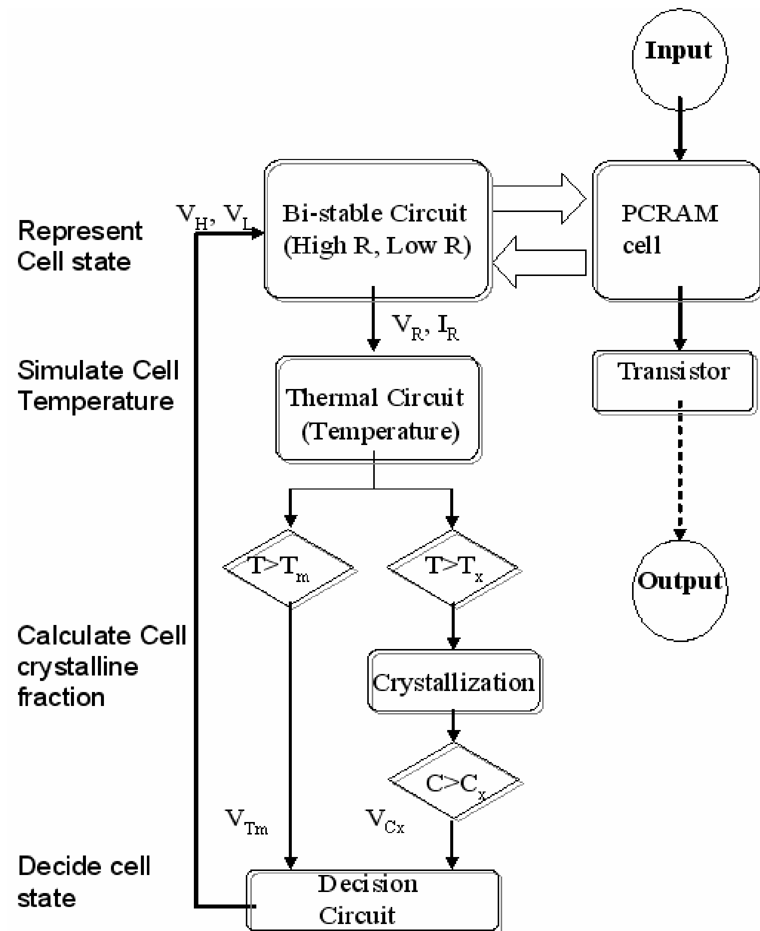



Fig. 5. 3 Flowchart of macromodel binary phase change memory cells.

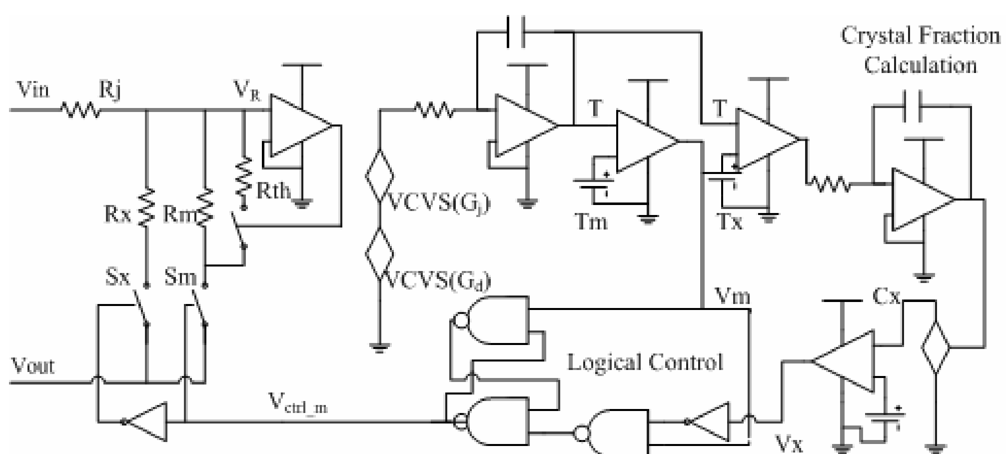



Fig. 5. 4 Schematic of binary macromodel of phase change memory cells

Threshold switch is considered in the bi-stable circuit. When the voltage across the $R_m$ is higher than threshold voltage $V_T$, a resistor $R_t$ parallel to $R_m$ is switched on to reduce the resistance of the amorphous state to a transient low value. A comparison between $V_R$ and $V_T$ is realized by an Op-Amp formed by Voltage Controlled Voltage Source (VCVS) and resistors (Connelly et. al, 1991).

### 5.2.2.2 Phase Change Circuit

The phase change circuit comprises three parts: the thermal part, the crystallizing part and the amorphizing part. Thermal dispersion and the joule heat model are used in the thermal part to calculate the temperature in the active region. The circuit outputs this temperature as $T_R$, which is compared with the melting point $T_m$ and the crystallization temperature $T_x$.

When the $T_R$ is higher than $T_x$, the crystallizing part would begin to work and calculate the crystalline fraction ($C_x$). When the crystalline fraction of the active region is equal to 1, the element would be viewed as in the crystalline state.

When the temperature is higher than $T_m$, amorphizing (melting) process would start. It changed the parameter of the crystalline fraction ($C_x$) to zero and gave a signal ($V_m$= 3.5 V) to show that the element has been changed to the amorphous state.

The physical models in this circuit are described as follows:

(1) Joule heating model

The power of joule heating is given by

$$W_j = I_R \times V_R \tag{5.1}$$

where, $I_R$ and $V_R$ represent the current and voltage across the resistor.

It is not difficult to simulate this model using a VCVS ($G_j$). A 1Ω resistor $R_j$ is used in

the circuit to monitor the current passing through the element $I_R$.

(2) Thermal dispersion model

The heat would disperse from the active region through the surrounding material, for example, from the top/bottom electrode, and from the crystalline chalcogenide material outside the active region:

$$W_d = \frac{\partial Q}{\partial t} = -\sum k \nabla T \tag{5.2}$$

where, $W_d$ is the heat dispersion power; k is the thermal conductivity. The power dispersed from different materials are added together to obtain the total thermal dispersion power. Another VCVS ($G_d$) is used to realize this model.

(3) Temperature calculation

The temperature $T_R$ is given by the following equation

$$T = \int_{t0}^{t1} \frac{W_j - W_d}{C \times V} dt \tag{5.3}$$

where, C and V are the thermal capacity and volume of the active region, respectively. The above equation is realized by an integration circuit.

(4) Crystallization model

In order to obtain the crystalline fraction, Johnson-Mehl-Avrami equations are used to simulate the crystallization kinetics (Wicker, 1996).

$$C_x = 1 - \exp(-Kt^n) \tag{5.4}$$

$$K = K_0 \exp(\frac{-E_a}{K_B T}) \tag{5.5}$$

where, $C_x$ is the crystalline fraction, n, $K_0$ and $E_a$ are constants specific to the material, $K_B$ is the Boltzmann's constant, t is time and T is temperature.

To apply the JMA equations in the circuit, K is set as a constant with a temperature

maintained at 900 K and equation 5.4 was expended by the expansive of the Taylor series. Because the programming pulses are very short (<<1us), the second and higher order parts are ignored:

$$V_c = 1-(1+(-Kt^n)+\frac{(-Kt^n)^2}{2!}+....) \tag{5.6}$$

Hence, the crystal fraction could be calculated by

$$V_c = Kt^n \tag{5.7}$$

In the macromodel, an integration circuit is initially used to obtain the duration of crystallization, then a VCVS calculates the quadratic or cubed to obtain the $V_c$. Subsequently, the output $V_c$ ($C_x$) would be compared with the threshold crystal fraction $C_T$.

#### 5.2.2.3 Logical control circuit

The logical control circuit is formed using logical gates. The input signals are $V_m$ and $V_x$, while $V_m$= 3.5V represents that temperatures exceed the melting temperature and $V_x$=3.5V represents that the crystalline fraction reaches 100%. The output $V_{m_ctrl}$ is the control signal for $R_m$ in a bi-stable circuit. The control signal $V_{x_ctrl}$ for $R_x$ is kept reversing to $V_{m_ctrl}$, hence the element will have a single state at any time. The relationship between the inputs and outputs is listed in Table 5.1.

Table 5. 1 Logical Relationship of Switches in PCRAM Macromodel.

| $V_x$ | $V_m$ | $V_{x_ctrl}$ | $V_{m_ctrl}$ |
|---|---|---|---|
| 0 | 0 | Unchange | Unchange |
| 3.5V | 0 | 3.5V | 0 |
| 0 | 3.5V | 0 | 3.5V |
| 3.5V | 3.5V | 0 | 3.5V |

#### 5.2.2.4 Simulation Results

The macromodel was simulated by means of HSPICE®, and was integrated with the voltage source, the current pulse generator and sense amplifier to verify its efficiency and compatibility with the peripheral circuitry of semiconductor memory technology. In the simulation, both dc analysis and transient analysis were carried out on the macromodel. It was also used to investigate the programming characteristics of the PCRAM cell.

The PCRAM element and device parameters used in the simulation are listed in Table 5.2. The feature size of the PCRAM element was 0.45 μm, while the thicknesses of the phase change material and electrodes were both 100 nm. The resistances of crystalline and amorphous states were set at 10 K ohm and 100 K ohm.

Table 5. 2 Parameters in PCRAM cell macromodel.

| Symbol | Quantity | Value |
|---|---|---|
| $R_x$ | crystalline state resistance | 10 K ohm |
| $T_x$ | crystallization temperature | 155 °C |
| $R_m$ | amorphous state resistance | 100K ohm |
| $R_T$ | transient resistance for amorphous state | 1K |
| $T_m$ | melting point | 620 °C |
| $\kappa_{TiW}$ | thermal conductivity of TiW | 1.76 J/cm-k-s |
| $\kappa_c$ | thermal conductivity of crystalline chalcogenide material | 0.02 J/cm-k-s |
| F | feature size of PCRAM element | 0.45 μ m |
| $t_c$ | thickness of phase change material | 100nm |
| $t_e$ | thickness of electrode | 100nm |
| Vth | Threshold switch voltage | 0.8 V |

(1) I-V characteristics of PCRAM macromodel

In the circuit shown in Fig.5.5, the PCRAM element was connected in serial with a voltage source. A voltage pulse with the rising slope from 0 to 1.5 V in 5 ns was produced and the I-V curves of the PCRAM element were simulated. Although there was no negative resistance part in the I-V curve, it can simulate the electrical characteristics in the programming and reading region (Fig. 5. 6).

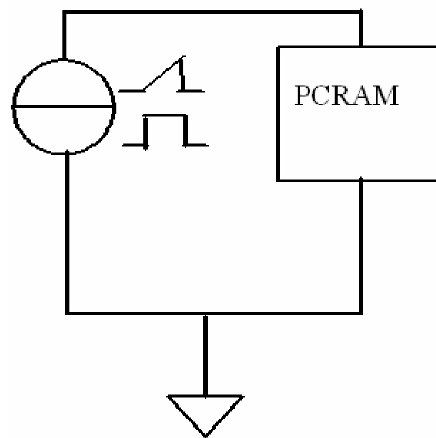



Fig. 5. 5 Voltage programming circuit for PCRAM element.

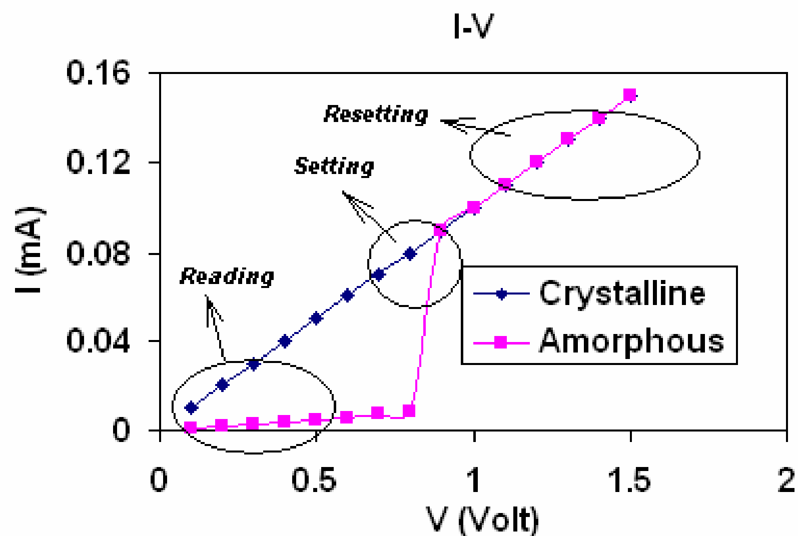



Fig. 5. 6 Simulation results of I-V characteristics of PCRAM elements.

(2) Programming of PCRAM macromodel

Based on the circuit in Fig. 5.7, the programming of the PCRAM element by current pulses was simulated based on the macromodel integrated with standard read/ write integrated circuit of memory technology (Rabaey et. al, 2003; Haraszti, 2000). The whole circuit was able to function efficiently with this macromodel. Designed current pulse generator can provide a pulse of 0.862 and 0.31 mA/ 300 ns for SET and RESET the element, respectively. The element programming/ reading characteristics are shown in Fig. 5.8. The current generator provided a 0.31 mA pulse and increased the temperature of active region to above 223 ˚C. The crystal fraction was increased to 100%, which was then maintained at this level in the model. After the programming pulse, sense amplifier successfully registered a reading of "1." During the reset process, the current generator generated a 0.862 mA pulse, increased the temperature of active region to 629 ºC and changed the crystal fraction to 0 %. Meanwhile, the sense amplifier was registered a "0". The temperature was quenched to room temperature in 30 ns.

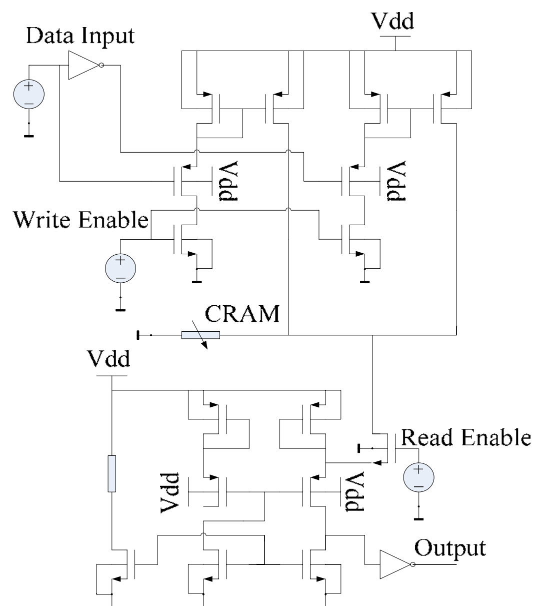



Fig. 5. 7 Circuit of standard read/ write operation of PCRAM.

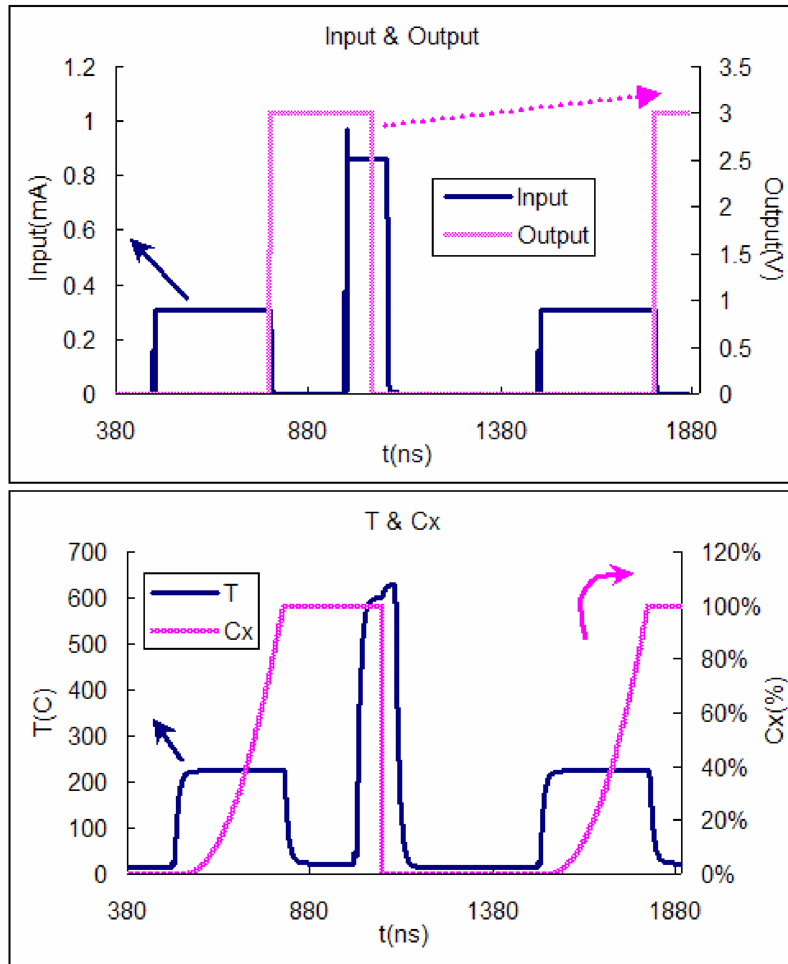



Fig. 5. 8 PCRAM operation with standard read/write circuit; (Upper) Input and Output Data with programming pulses; (Lower) simulated temperature and crystal fraction of the active region.

(3) Characteristics of PCRAM Macromodel

The simulated and experimental curves are shown in Fig. 5. 9. After changing the current amplitude from 0 mA to 1 mA at a pulse width of 300 ns, the dc resistance of PCRAM after the pulse was recorded. The upper diagram shows the simulated binary macromodel results. When the current amplitude was raised to 0.309 mA, the resistance changed to 10 K ohm, and this corresponded to the crystalline state of the PCRAM element. When the current amplitude was raised to 0.756 mA, the resistance reverted to 1

M ohm of the amorphous state. Compared to experimental results, there were no intermediate states between 10 K ohm and 1 M ohm because only two resistors were included.

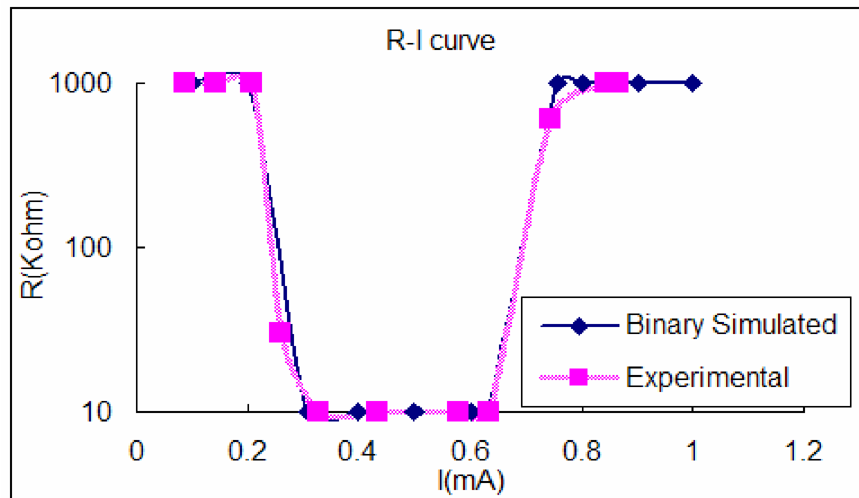



Fig. 5. 9 R–I curve of PCRAM elements based on binary macromodel.

(4) Relationship between the amplitude and width of programming pulses

Based on the circuit illustrated in Fig. 5. 7, the relationship between the amplitude and the width of programming pulses was also investigated. During the simulation, the pulse width changed from 250 ns to 400 ns and the minimum required amplitude of SET pulses was recorded for each pulse width. The results are shown in Fig. 5. 10. Obviously, the amplitude decreased with an increase in the pulse width. It is also obvious that with a further increase in pulse width, the amplitude became slower and saturated at around 0.3 mA. That is because when the amplitude of current pulses was too low to raise the temperature of active region to the crystallization temperature and the crystallization thus would not happen. The experimental results match the simulation results better in low amplitude pulses, while the required current is obviously larger than experimental results

with short pulses. It is because the temperature dependence of effective constant in Equation 5.5 is not considered in this model. At high amplitude, a higher temperature would speed up the crystallization process, but the crystallization speed is treated as a constant in this macromodel. Therefore, a higher required program current than in experiments was obtained in this simulation.

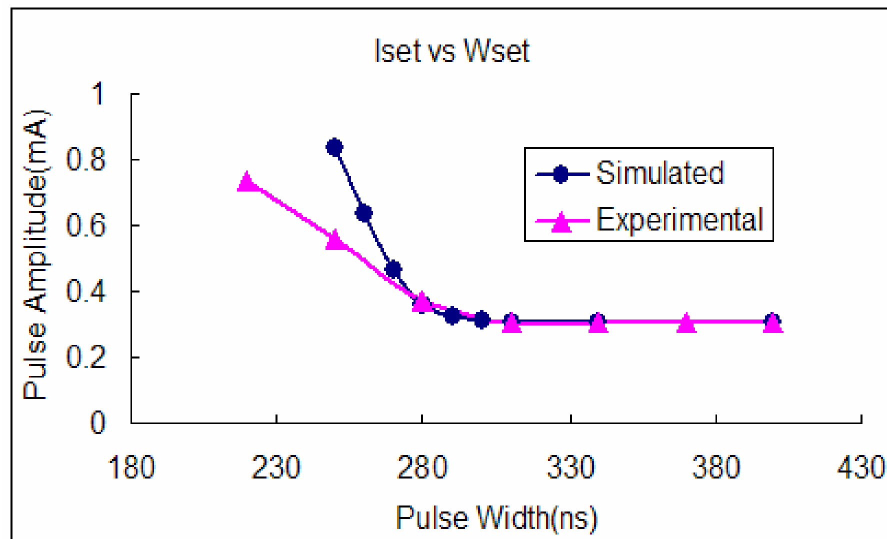



Fig. 5. 10 Relationship between amplitude and width of programming pulses of the SET operation.

### 5.2.3 Multi-level Macromodel of PCRAM

#### 5.2.3.1 Four-level Macromodel

Multi-level storage is an effective way to increase density, reduce costs and enhance the data transfer rate of semiconductor memory. By storing two or more bits in a single memory cell, the array size can be largely reduced. PCRAM technology is very promising in the application of multi-level storage because of its large difference between the resistance of crystalline state and the resistance of amorphous state. However,

although there have been some experimental research of multi-level PCRAM element, to my best knowledge, no IC model has been proposed for multi-level PCRAM element.

The chart flow and circuit of a proposed four-level PCRAM macromodel are shown in Fig.5.11 and Fig.5.12. It was developed by a simple modification of a binary macromodel, i.e. adding two more resistors to represent the intermediate states and by including two more threshold crystal fractions. The macromodel for 8-level or 16-level storage can also be developed using similar modifications.

The entire circuit is also divided into three parts, i.e. the four-level circuit, phase change circuit, and logical control circuit.

Four resistors are included in the four-level circuit to represent four states of PCRAM elements. These resistances can change according to device structure and different phase change materials. The switch, current monitoring and threshold switch modeling are the same as that of the binary macromodel.

The phase change circuit has the same thermal part and crystallization part as the binary model and is used to calculate the temperature and crystal fraction. The difference with binary model is that there are three threshold crystal fractions in the crystallization part of four-level model. Their values were set as 60%, 80% and 100% respectively in this thesis. When the crystal fraction Cx is higher than any threshold, a corresponding signal would be sent to the logical control circuit.

The logical control circuit is more complex than that of binary macromodel, because there are four signal inputs to control four switches. At any time instant, the logical control circuit should select one and only one resistor in this four-level circuit. The logic table of the logical control circuit is shown in Table 5.3.

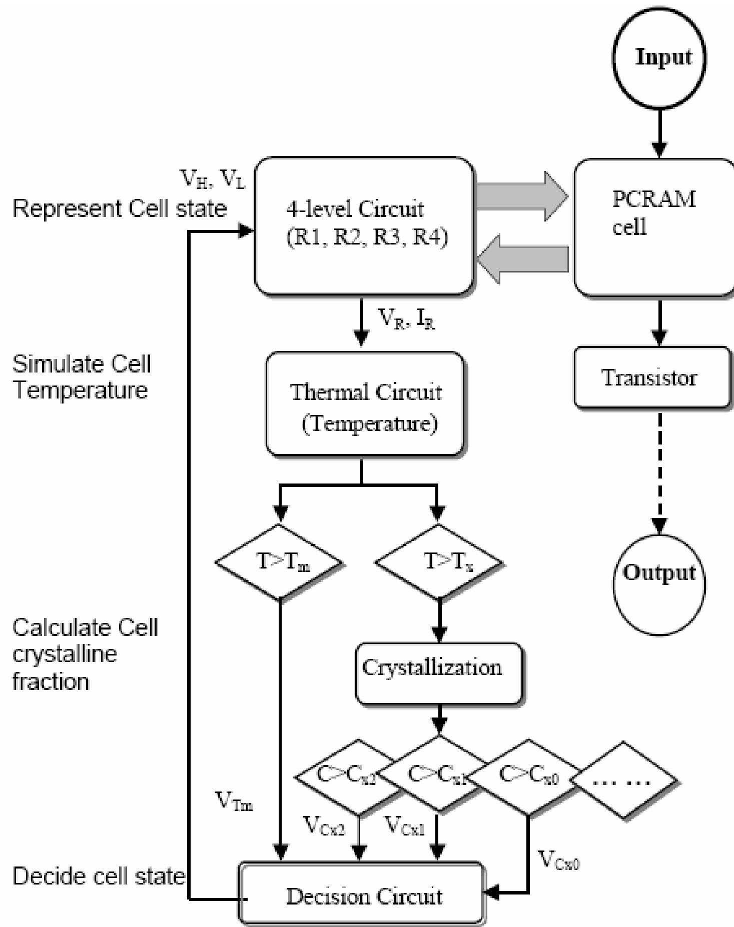



Fig. 5. 11 Flow chart of the macromodel of four level PCRAM cells.

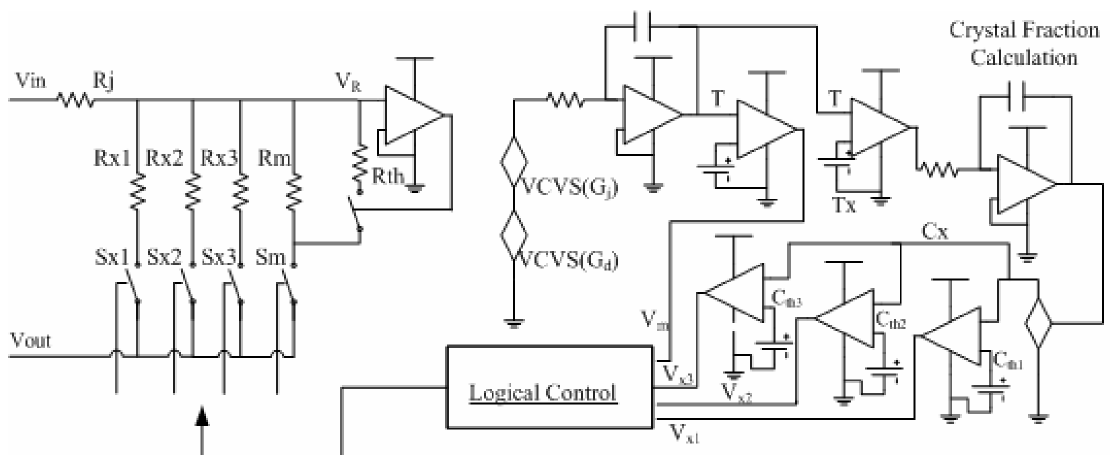



Fig. 5. 12 Schematics of the macromodel of four-level phase change memory cells.

Table 5. 3 Logical relationship in the logical control circuit of four level PCRAM macromodel.

| Tm(T>600°C) | 0 | 0 | 0 | 1 | 0 |
|---|---|---|---|---|---|
| Tx01 (CF>0.6) | 1 | 1 | 1 | 0/1 | 0 |
| Tx10 (CF>0.8) | 0 | 1 | 1 | 0/1 | 0 |
| Tx11 (CF>1) | 0 | 0 | 1 | 0/1 | 0 |
| C00 | 0 | 0 | 0 | 1 | UC |
| C01 | 1 | 0 | 0 | 0 | UC |
| C10 | 0 | 1 | 0 | 0 | UC |
| C11 | 0 | 0 | 1 | 0 | UC |

UC represents "unchanged"

### 5.2.3.2 Simulation Results

The multilevel programming can be realized by changing the width of programming pulses. The programming pulses used in the simulation are shown in the upper section of the Fig. 5.13. The set pulses were 0.31 mA/ 300 ns, 0.31 mA/ 250 ns and 0.31 mA/ 200 ns, respectively. Reset pulses were maintained at 0.864 mA/ 100 ns. The bottom section of the figure shows the temperatures and crystal fractions produced by these programming pulses. Because the sense amplifier for multilevel storage is much more complex than that of binary system, it is not included here. However, based on the calculated crystal fraction, the corresponding resistor is to be selected by the macromodel. It is also possible to program the PCRAM to multilevel states by means of pulses with different amplitudes of the same width.

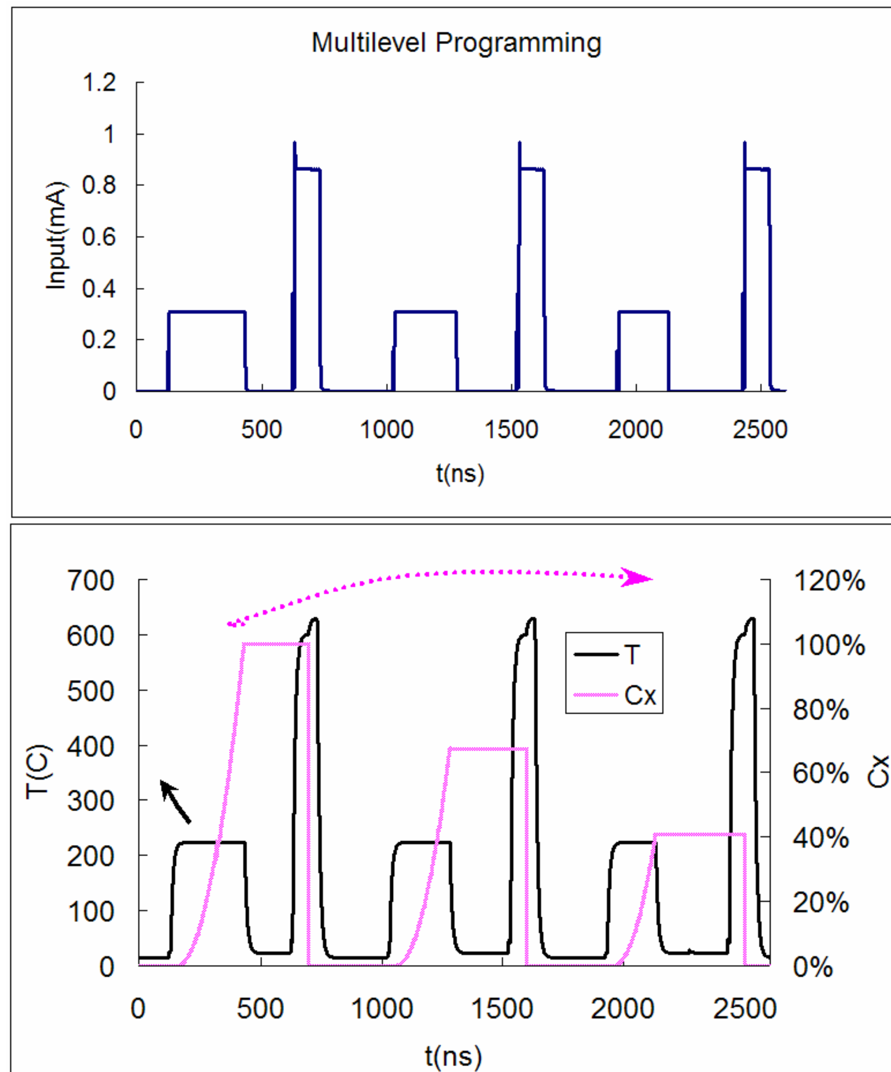



Fig. 5. 13 Multilevel storage of the PCRAM element (top-input current pulses, bottom- temperature and crystal fraction of active region); the fraction of crystalline states in the active region would increase with a longer SET pulse width.

## 5.3 IC Design of 128-bit PCRAM Chip

In this section, the circuit of the proposed 128-bit PCRAM memory chip based on 0.35 μm CMOS technology is introduced. The entire simulation and the layout are based on CADENCE™ under the UNIX operation system. The memory array is able to realize

the random access, programming and sensing functions. The read access time of this design is 30 ns according to the simulation results.

### 5.3.1 Architecture and Main Blocks

The architecture and main blocks for 128-bit SLL_PCRAM are illustrated in Fig. 5. 14. The blocks are divided according to their functions, for example, the sense amplifier for reading the data, the current mirror for programming and the decoders for accessing the targeted memory cells. Other blocks include the memory array, input/output buffers, input receivers and clock/control circuits.

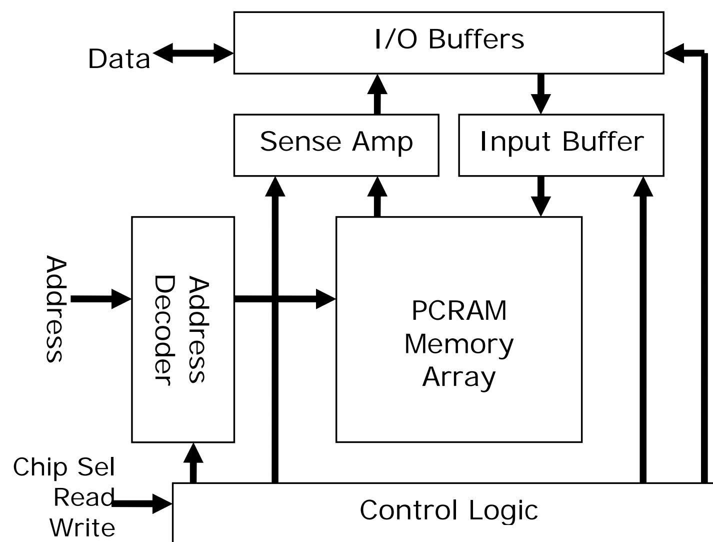



Fig. 5. 14 Architecture of 128-bit SLL_PCRAM chip.

#### 5.3.1.1 Memory Array

Memory elements cannot be directly connected as an array due to the leakage path in the memory array as shown in Fig. 5.15 (a). Each memory element should be integrated with a selective element, which can meet the requirement on current, leakage and voltage

of memory cells. There are two available selecting elements: NMOS transistor and diode. Transistors are more popular in modern integrated circuit design. Diode/BJT has the advantage to provide high current. In this work, NMOS transistor was chosen as in Fig. 5.15 (b) because of its wider application.

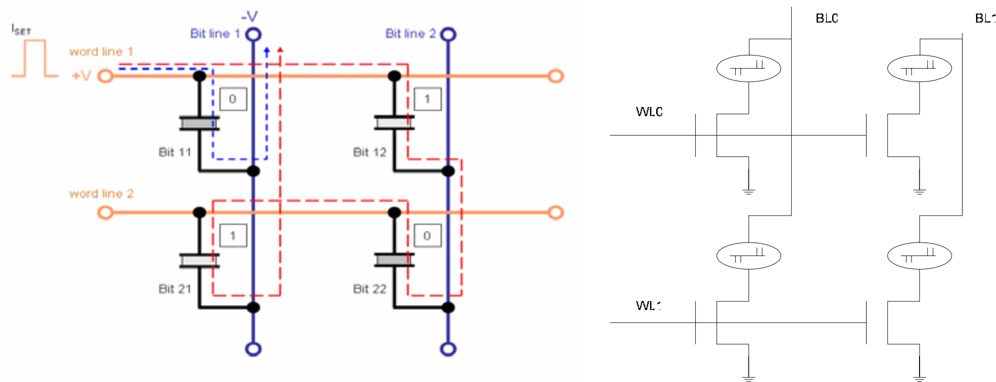



Fig. 5. 15 (a) Leakage current in PCRAM memory array without the selecting elements, (b) Schematic of PCRAM array with transistors. The leakage among memory cells in array was eliminated by the NMOS selective elements.

### 5.3.1.2 Decoder

The row/column decoder is an essential element in all random-access memories. It requires an $n$-bit address and produces $2^n$ outputs, one of which is activated each time.

In this design, the decoder controlled 16 word lines of the memory array, thus there are 4-bit address signals. The decoder is implemented by a 2-level 'NOR' structure as shown in Fig. 5.16.

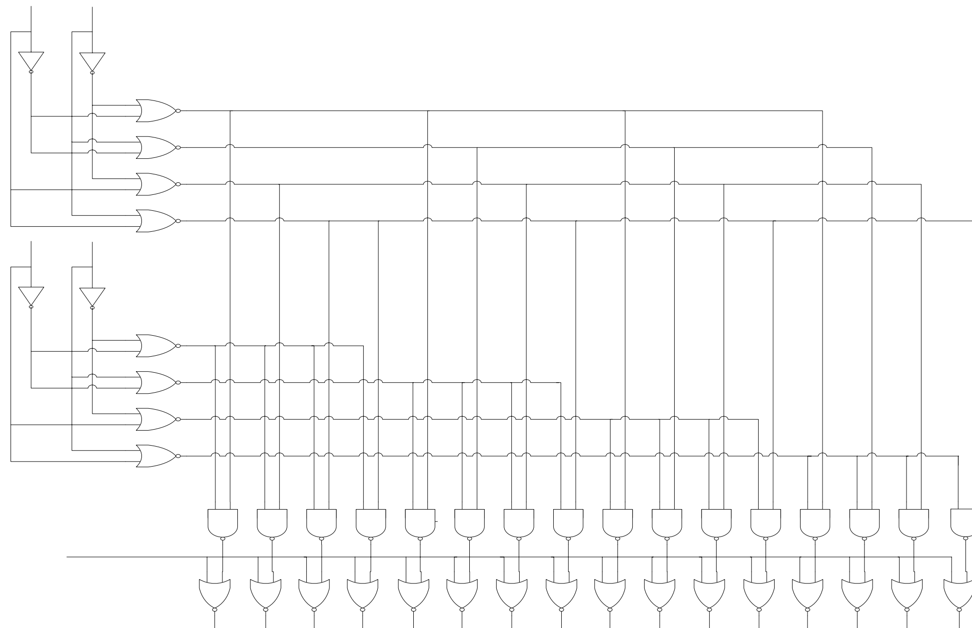


Fig. 5. 16 Schematics of a row decoder; it requires an $n$-bit address and produces $2^n$ outputs, one of which is activated.

### 5.3.1.3 Sense Amplifier

The sense amplifier in this design is shown in Fig. 5. 17. The requirement is to continuously provide the dc sense current, which must be lower than 2 μA to avoid data lose. It also includes an external bias resistor, which controls the sense current amplitude. Therefore, it is possible to adjust the sense current and optimize the reading conditions.

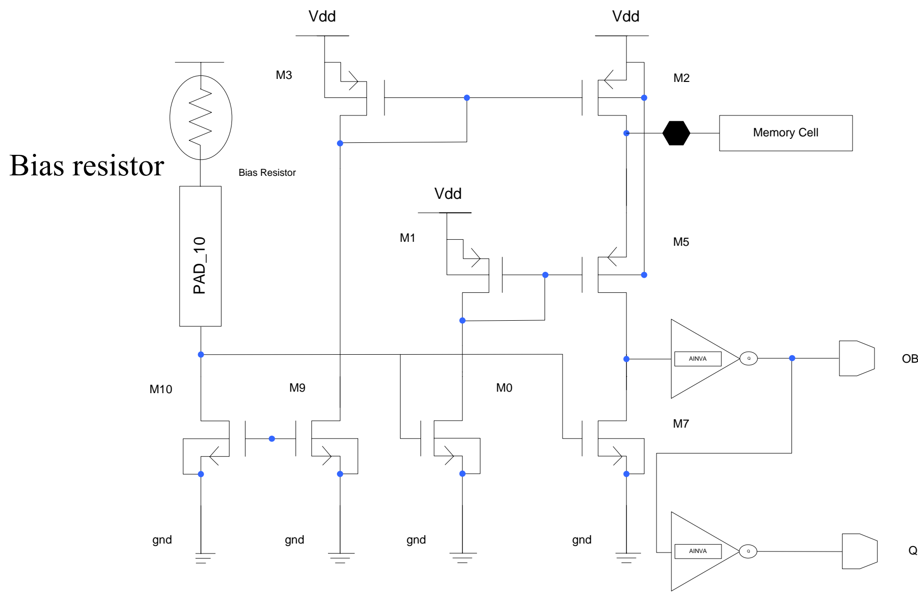



Fig. 5. 17 The schematics of a single ended sense amplifier with external bias resistor.

### 5.3.1.4 Programming circuit

The current generator is designed to provide the current pulse of two different amplitudes to reset or set the PCRAM element (Fig. 5. 18). An external bias is also included to adjust the programming current.

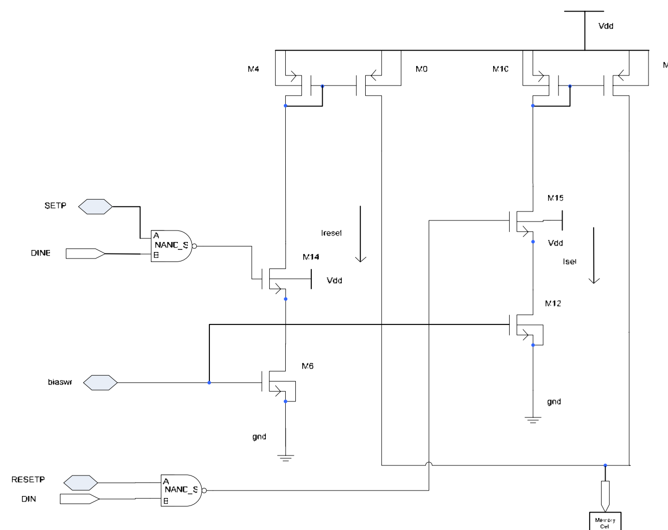
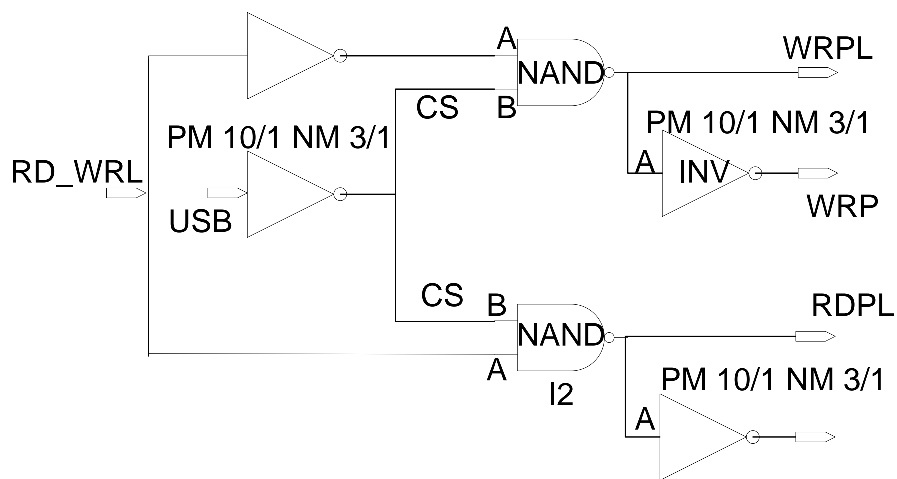


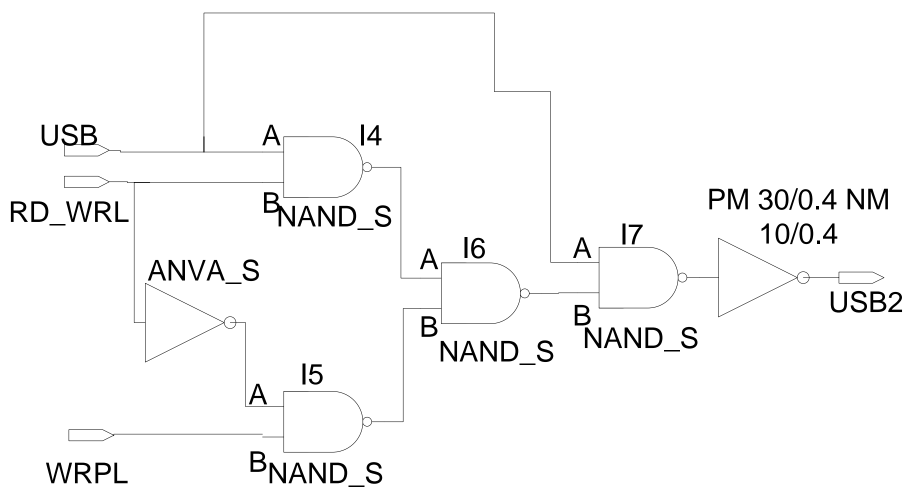

Fig. 5. 18 The schematics of the current generator; the external bias was also included to adjust the programming current.

### 5.3.1.5 Control Logic Circuit

The logic control circuit (Fig. 5.19) is included to synchronize different blocks by controlling the “enable” signal of every block. Based on the time set in the logic control circuit according to the clock, the different blocks would work in order and realize different functions.




(a)




(b)

Fig. 5. 19 Logic control circuit schematic.

### 5.3.1.6 Design for test circuits

The design for testing (DFT) structure is included for the failure analysis of the chip. It can monitor the functionality of PCRAM memory cells and blocks separately. It is also designed to debug the process issues. The basic DFT circuits in this design are shown in Fig. 5. 20.

(1) A 2×2 transistor array without a PCRAM cell is used to verify the selected element design/ fabrication and the array design/fabrication.

(2) A single PCRAM memory cell is used to verify the performance of the memory cell alone.

(3) A single memory unit (with memory cell and selective NMOS) is used to verify the integration of the PCRAM cell and selective elements.

(4) A small memory array is used to doubly guarantee the working of the array design.

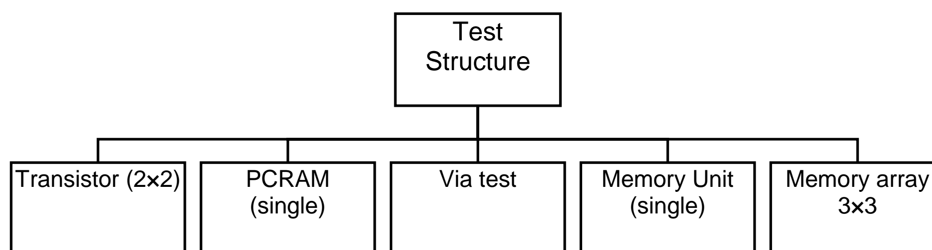



Fig. 5. 20 Testing structure of memory array.

Embedded testing structures are also included in the memory to monitor the working characteristics of the sense amplifier and programming circuit. Additionally, the bias resistor of sense amplifier, the current generator and clock signals are provided externally.

Therefore, it is possible to adjust the sense amplifier current and programming current during the testing. It provides more flexible specifications for testing.

### 5.3.3 Full Schematics, Simulations and Layouts

In this section, the schematics, simulation and layout of the entire 128-bit SLL_PCRAM will be briefly introduced. The access time of this design is 30 ns based on the simulation results. However, since the circuit simulation is not the focus of this thesis, the detailed account on the simulation process will not be included here.

#### 5.3.3.1 Full Schematics

The memory IC design schematics as shown in Fig. 5.21 include several key blocks, such as the memory array, decoder, the sense amplifier, programming circuit, control logic and low-ESD and I/O pads. In order to accurately simulate the electrical characteristics of this full function memory design, the parasitic conductance and resistance of the bonding wire and external resistor was considered for more realistic simulation results.

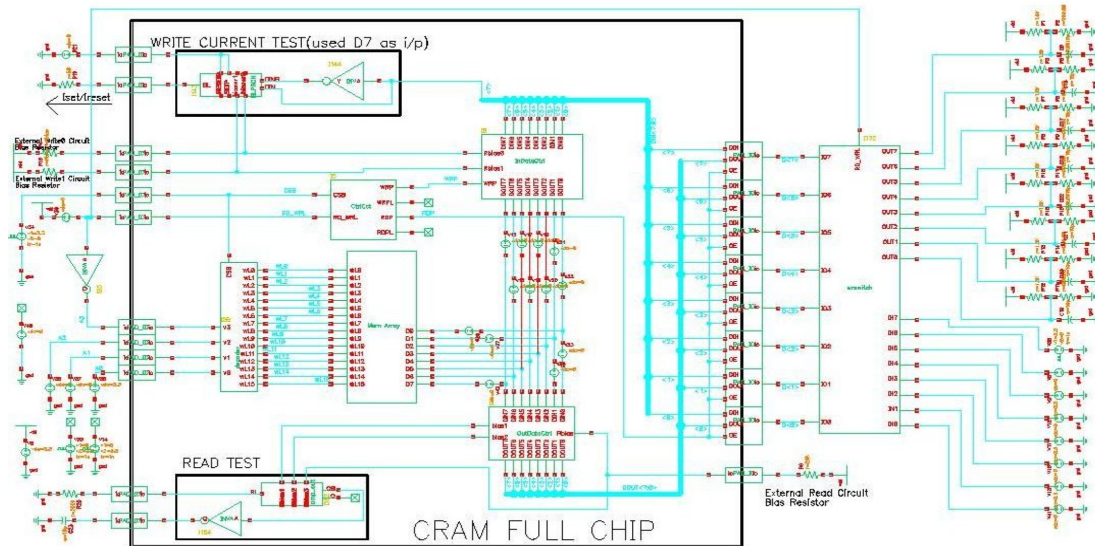



Fig. 5. 21 Full schematics of 128-bit memory chip, including key blocks, such as the memory array, decoder, sense amplifier, programming circuit, control logic and I/O pad.

### 5.3.3.2 Access time simulations

The simulations were carried out while focusing on the access time of the memory chip, which is the most important parameter for evaluating the performance of memory devices. The access time is defined as the time interval between the instant, at which storage/ sense of data is requested and the instant, at which storage/sense is started. It includes the chip select, addressing and programming access time.

The chip select access time is the time interval between the instant at which the chip select signal comes "on" and the instant at which the data is sensed on the output pad. During the simulation, it was seen that the access time from when the chip was enabled to the data output at the I/O pad was less than 30 ns. The addressing access time is the time interval between the instant at which the address is input at the input pad and the instant at which the data is sensed at the output pad. The delay at the positive going edge was less than 25 ns and the delay at the negative edge was less than 20 ns. Programming

access time is defined as the time interval between the instant at which storage of data is requested and the instant at which current is generated. A quick response within 10 ns was observed in the simulation.

### 5.3.3.3 Layout

Chip layout defines various layers associated with the masks used in fabrication as shown in Fig. 5.22. The handoff of the final layout from the designer to the fabrication facility is known as "tapeout". The goal of the layout process is to implement the design in a compact area while satisfying the design rules set by the foundry. Layout design is as much an art as it is a science, but there are some fundamental guidelines that must be adhered to if the chip is to be fabricated successfully. These guidelines, when violated, are flagged by modern CAD tools, called Design Rule Checkers (DRCs), that can handle the billions of geometries needed to represent complex layouts. The design rules are a set of tolerances based on the minimum feature size imposed by a given technology. These tolerances are due to registration errors in processes, such as mask alignment transferring from one pattern to another, process control due to variation in exposure and etching and overlap requirements to ensure low ohmic contact where necessary.

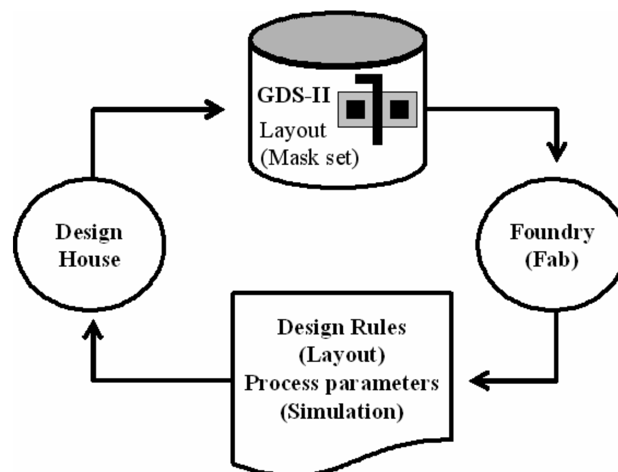



Fig. 5. 22 The flow of data between the design house and the foundry.

In this design, the layout of the full chip occupied the area of 1887 × 1108 $\mu m^2$ as shown in Fig. 5.23. It is important to note that the layout of R/W circuits should match the pitch of the memory array, given that pitch is defined as the length of the memory unit along the bit-line. This is because every column has its own current generator and sense amplifier. In this simulation, the pitch of the 16 × 8 transistor memory array is 20 μm; therefore, one sense amplifier occupied the area of 66 × 20 $\mu m^2$.

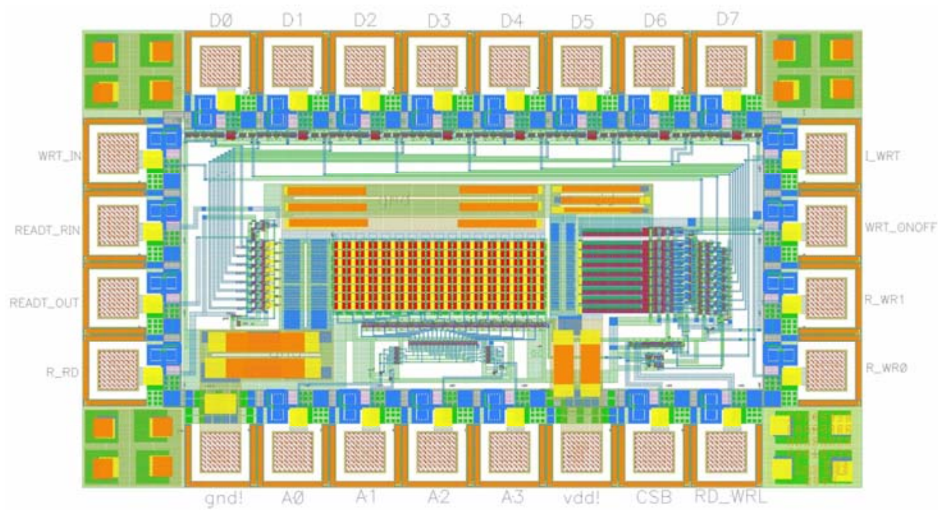



Fig. 5. 23 The full layout of transistor version.

## 5.4 Summary

In this chapter, the IC design of the 128-bit SLL_PCRAM chip was presented and a macromodel of PCRAM memory cells was proposed for HSPICE simulator.

This two-terminal HSPICE macromodel was based on simplified physical models of PCRAM elements. All parameters in this macromodel are the physical parameters of the PCRAM memory cells, making it very flexible and universal. Additionally, based on the crystal fraction calculated in the macromodel, the multi-level storage application was developed based on the binary macromodel. In this work, the macromodel was integrated

with standard write/read circuitry in memory technology and successfully simulated the programming of the PCRAM element in both binary and multilevel storage.

The design of the 128-bit stand-alone PCRAM chip was based on the 0.35 μm CMOS technology. The simulation and layout were completed based on the CADENCE in UNIX operation system. This design included the functions of programming, sensing, decoding, and test structures. The layout occupied the area of 1887 × 1108 $\mu m^2$. This design was later used in the prototyping of SLL_PCRAM and $Ge_2Sb_2Te_5$_PCRAM memory chips.

# CHAPTER 6
# FABRICATION AND TESTING OF 128-BIT SLL_PCRAM CHIP

This chapter describes the fabrication and testing of 128-bit SLL_PCRAM chip, which is used to verify the superior performance of SLL structure in PCRAM technology. The SLL_$Ge_2Sb_2Te_5$ structure with 6-pair $Sb_2Te_3$ and GeTe films was used in this chip. The R-I curve, life cycle and reliability were measured and compared with those of conventional $Ge_2Sb_2Te_5$ material. This work is also to prove the process compatibility between the SLL structure and the standard CMOS technology.

## 6.1 Introduction

The single SLL phase change memory cell has been reported to yield lower RESET current compared to conventional $Ge_2Sb_2Te_5$ cells (Chong, et.al., 2005; Chong, et.al., 2006). However, when memory cells are integrated into a CMOS chip, the process compatibility and the periphery circuits would also affect the device performance. Furthermore, chalcogenide materials would require additional processes. Hence stability and reliability may be other issues (Skotnicki, 2005). To verify the compatibility of SLL structure and CMOS process, 128-bit SLL_PCRAM chip was fabricated and tested. Its performance was compared with the conventional $Ge_2Sb_2Te_5$ material in the same device structure and chip design.

SLL_PCRAM chip can be physically divided to front-end CMOS, back-end metal connection and memory cells. A schematic cross-section of PCRAM memory bit is

shown in Fig. 6.1. One PCRAM unit includes a selective element and one memory cell. Phase change memory cells are built on top of backend metal connection and the CMOS transistors. The drain of selective element NMOS is connected to the bottom electrode of the memory cell by metal connections in the memory array.

The CMOS wafer was fabricated by Chartered Semiconductor Manufacturing Ltd. (CSM). After the front-end CMOS was fabricated, two layers of metal: metal 1 and metal 2 were deposited for electrical inter-connection. The process stopped at "via 2", which connects metal 2 and metal 3. The wafer fabricated in CSM is 8-inch. Laser technology (Fig. 6.3) was used to cut the wafers into 4-inch to match the stepper in Data Storage Institute (DSI). PCRAM memory cells and the interconnections were fabricated on top of "via 2".

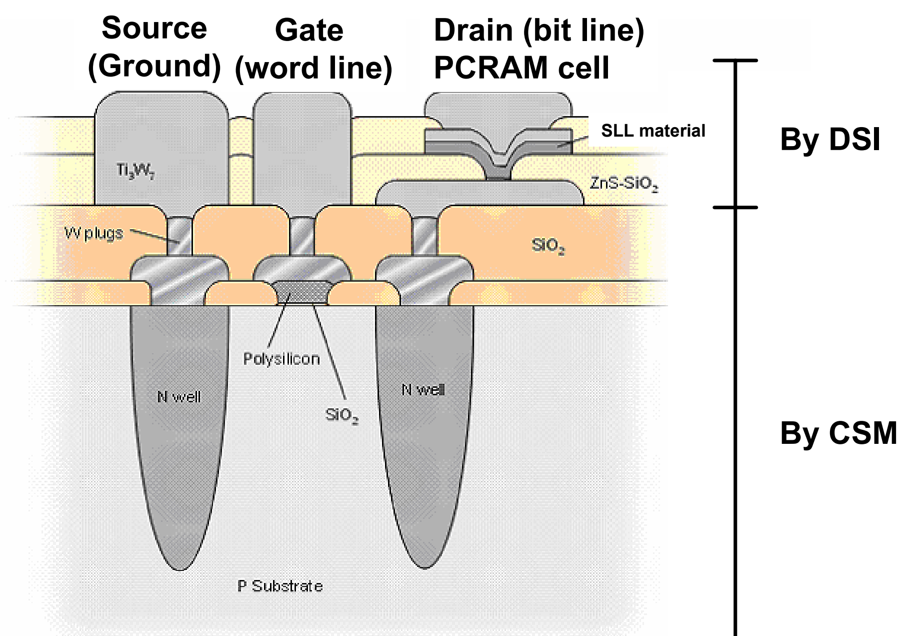



Fig. 6. 1 Schematic cross-section of SLL_PCRAM memory bits.

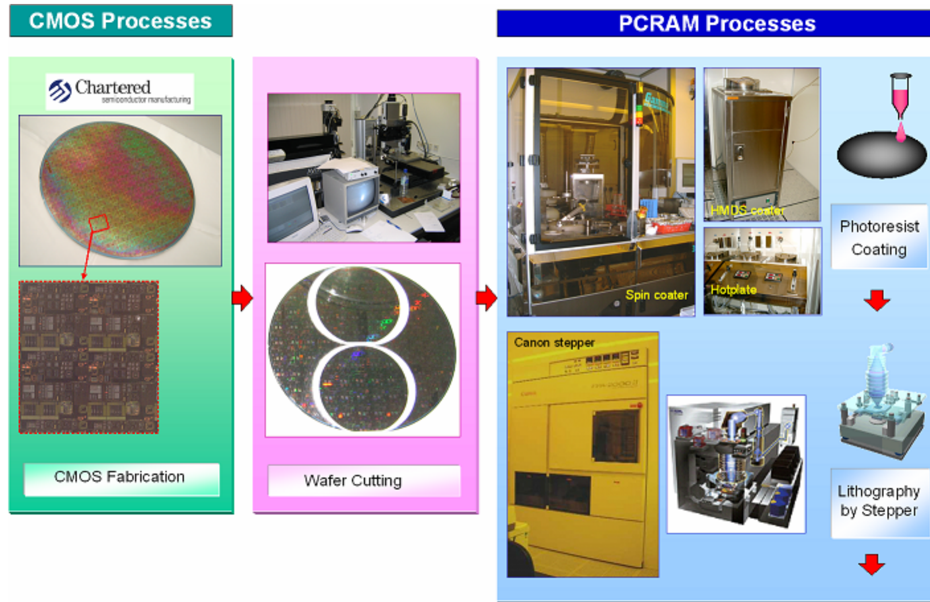



Fig. 6. 2 Schematic of PCRAM fabrication flow.

## 6.2 Fabrication of SLL_PCRAM

### 6.2.1 SLL Memory Cell Structure

The schematic cross-section of SLL_PCRAM memory cells is shown in Fig. 6.3. It has five layers. The bottom layer is 200 nm thick TiW electrode. The second layer is 100 nm thick $ZnS-SiO_2$ thin film, which defines the 1 μm critical size for memory cells. The third layer is 50 nm thick phase change material with 10 nm TiW on top. TiW is used to enhance the electrical contact and protect phase change material from oxidization. The SLL structure used in this experiment has been introduced in section 4.2.5. It is made by alternatively depositing 4.87 nm thick $Sb_2Te_3$ thin films and 3.46 nm thick GeTe thin films. The fourth layer is 100 nm thick $ZnS-SiO_2$ thin film, which is used to isolate the top electrode from side wall of the SLL structure. It is also critical to confine the heat and to define the thermal properties of the memory cells. The fifth layer is 200 nm thick TiW top

electrode.

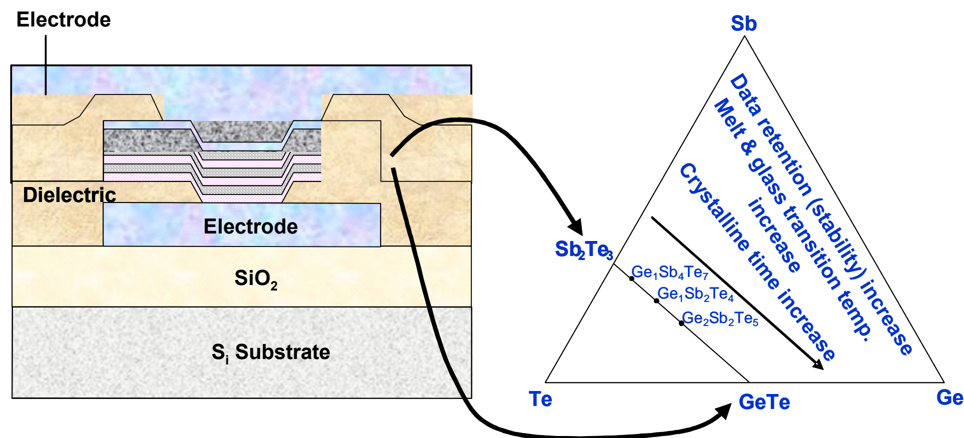



Fig. 6. 3 Schematic cross section of SLL_PCRAM memory cells.

### 6.2.2 General Processes and Equipments

The process for each layer of PCRAM memory cells includes similar steps: lithography, thin film deposition and lift-off. The details would be introduced in the following section. The process flow of lithography, thin film deposition and lift-off is shown in Fig. 6.4. Firstly, photo-resist film is deposit on the wafer using a spin coater. Next, ultraviolet (UV) light is injected through the mask onto the wafer. This is usually done using a stepper machine. The masks are glass or quartz outlines of the design, which is to be developed on the wafer. Then the photo-resist is removed leaving the desired pattern. Following this, the material to be used is sputtered onto the substrates according to requirements. Lastly, the photo-resist is lifted off leaving only the pattern formed by the sputtered material.

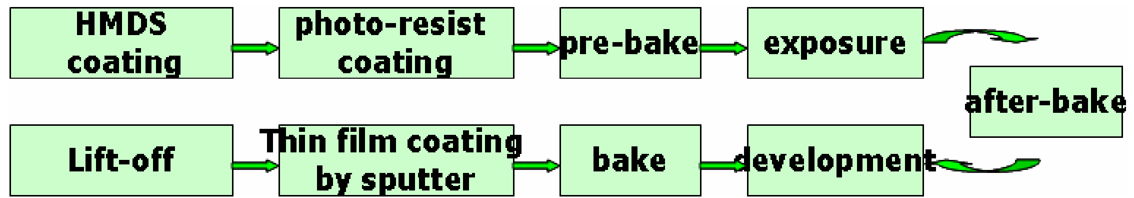
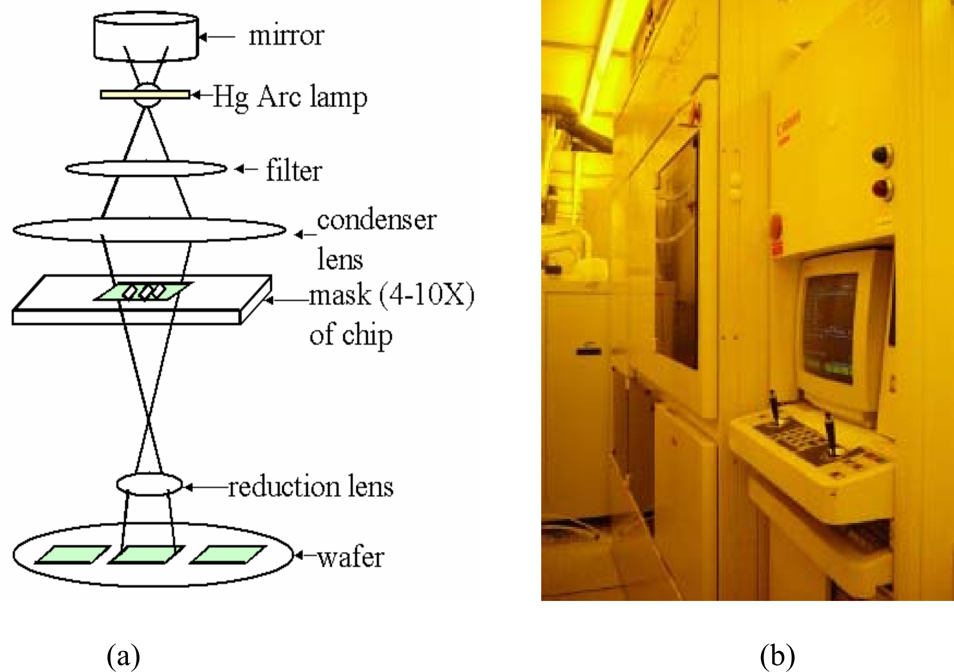



Fig. 6. 4 Schematic process flow for SLL_PCRAM memory cells.

Lithography is the process of transferring a pattern from a mask to the substrate. The detailed procedures for lithography include HMDS coating, photoresist coating, pre-baking, exposure, post baking and photoresist developing. Canon i-line Aligner was used in lithography process. The laser source wavelength is 365 nm, thus the critical size that can be obtained is around 0.200 μm. The general principle of projection lithography is shown in Figure 6.5. The pattern on the reticle (mask) can either be the same size as that of the wafer, or five or ten times greater. A quasi-monochromatic, spatially incoherent light source is used to illuminate the mask. The source is then homogenized to ensure a highly uniform intensity distribution on the plane of the mask. Next, the condenser lens can be controlled to adjust the degree of coherence of the illuminating beam. The reduction lens would collect the light transmitted through the mask, usually at a magnification of 0.2. Therefore, a typical wafer can contain many copies of the mask pattern as the stepper calculates the wafer size and exposes it multiple times.




(a) (b)

Fig. 6. 5 (a) The principle and (b) the picture of Canon i-line Aligner used for SLL_PCRAM fabrication.

The Balzers sputtering machine was used to deposit the thin films of the SLL_PCRAM chip. It has three chambers where the targets can be placed (Fig. 6.6). A high negative voltage is applied to the material to be sputtered. An electrical gas discharge leads to the formation of positive argon ions, which would be accelerated in the direction of the coating material. The colliding positive ions would knock off atoms from the coating material's surface, which would be deposited on the surface of the target. Chamber 1 and 3 are DC sputtering chambers for metal or semiconductor material while the Chamber 2 is the RF sputtering chamber for dielectric materials. The highest power for the sputtering is 5 KW.

Fig. 6. 6 Balzers sputtering machine used to deposit phase change, dielectric and metal thin films.

### 6.2.3 Memory Cell and Memory Chip

After the wafer level fabrication was completed, the wafer was sent for dicing, bonding and packaging. The top view of the bonded chip is shown in Fig. 6.7. It totally had 24 pads with 2 VDD/ GND, 4 addresses, 8 data I/O, 4 control signals and 6 test structure outputs.

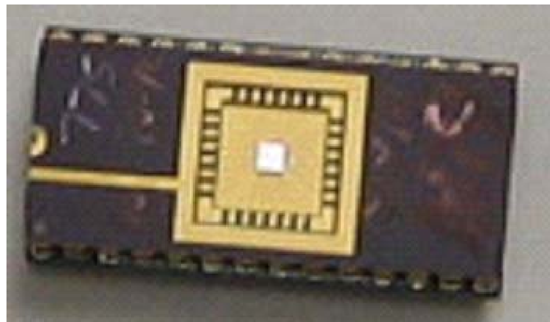


Fig. 6. 7 The top view of 128-bit SLL_PCRAM memory chip after wire bonding.

## 6.3 Testing of PCRAM Chips

### 6.3.1 Memory Chip Testing Bench

The testing bench was developed by DSI to test the 128-bit memory array. The hardware chart-flow is shown in Fig. 6. 8. The main circuits include pulse generator, current driver and test board. Current driver generates current pulses. While the pulse width and the pulse amplitude are controlled by pulse generator through the interface with NI DIO card. Test board includes pulse source for current driver, measurement probe from oscilloscope and digital multi-meter. This test bench has strong testing capability with the tunable pulse width ranged from 3 ns to 900 ns and tunable pulse amplitude ranged from 0V to 14V for device programming.

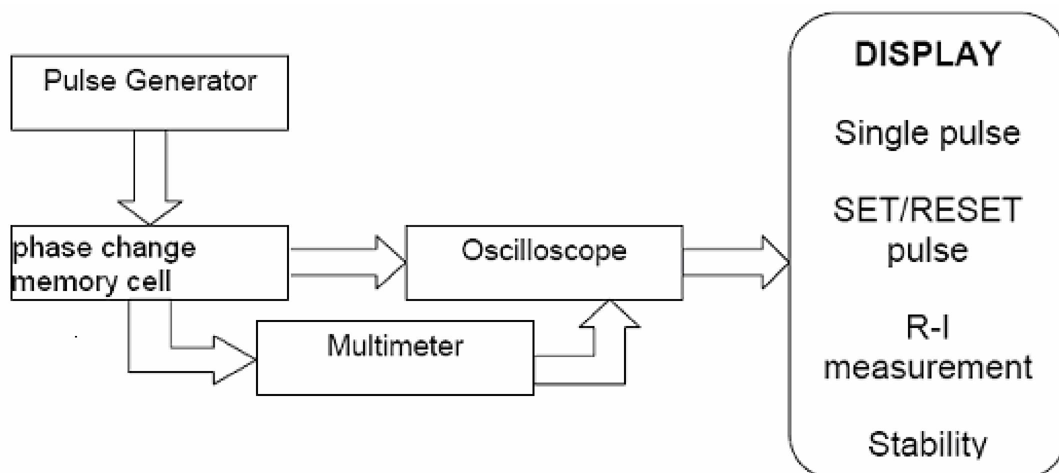



Fig. 6. 8 Schematic diagram of the testing system.

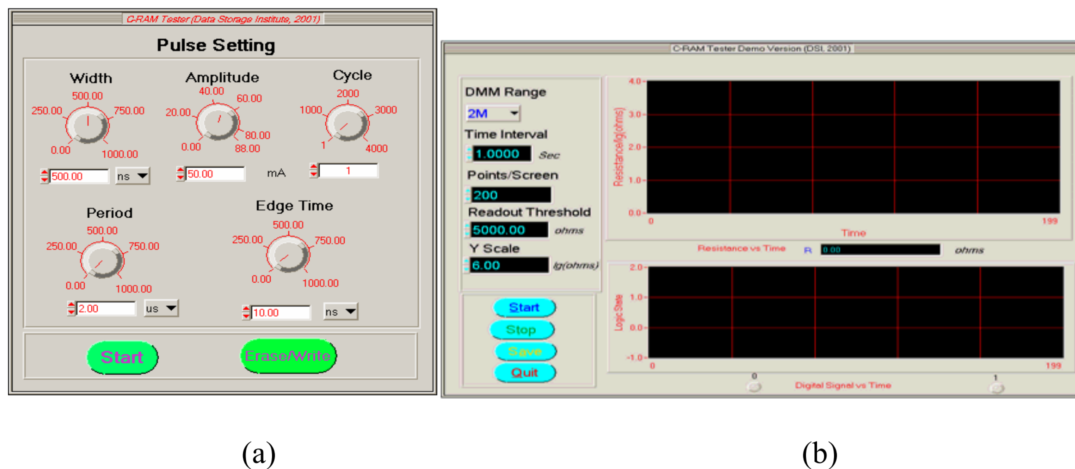
### 6.3.2 Testing of SLL_PCRAM Chip

The performance of 128-bit SLL_$Ge_2Sb_2Te_5$ memory chip was measured using the

testing bench introduced above. The R-I curve, life cycle and reliability of this structure were compared with the memory chip with conventional $Ge_2Sb_2Te_5$ devices.

**Low current**

In the R-I (Resistance vs Current) curve measurement, control signals were firstly input to select the memory bit. The electrical pulses with the amplitude changed from 0 V to 6 V were used to program the SLL_PCRAM device. The corresponding programming current was monitored by oscilloscope. At the same time, a constant voltage of 0.2 V was applied to the memory cell to read the resistance. The software control interface is shown in Fig. 6.9.




(a) (b)

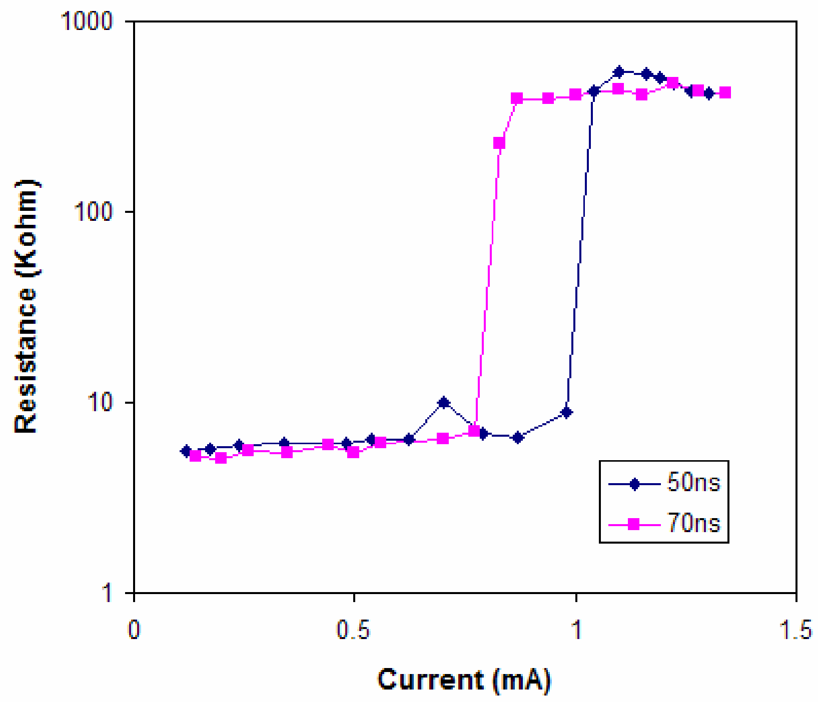
Fig. 6. 9 Single pulse operation and resistance monitor of testing bench (a) single pulse interface (b) resistance monitor.

In this experiment, the electrical pulse of 50 ns and 70 ns was applied. Fig. 6.10 (a) shows the resistance changes from crystalline state induced by electrical pulses. It was found that a RESET pulse of 50 ns and 1.04 mA was able to change the SLL_PCRAM memory cell from starting state of crystalline state to amorphous state, by observing the sharp increase of electrical resistance. Fig. 6.10 (b) shows the U curve, recording, starting from amorphous state, the resistance change induced by electrical pulses. The electrical

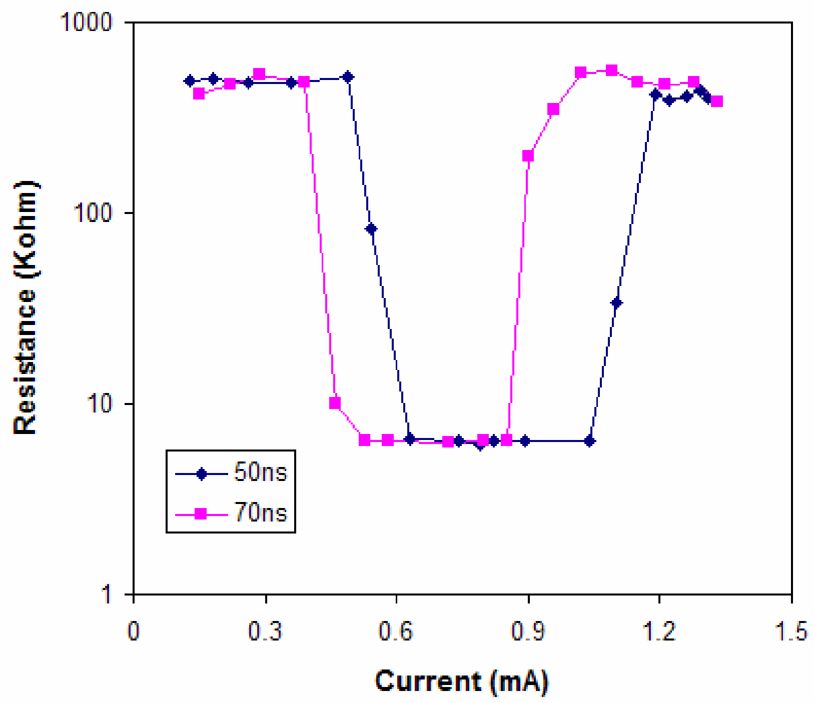
pulses of 50 ns and 0.63 mA could SET the device from amorphous state to crystalline state. If an electrical pulse of 50 ns and 1.19 mA was applied subsequently, the device changed back to amorphous state.

Electrical pulses of 70 ns were also used to program the memory cells. When the initial state of memory cells were at crystalline state, electrical pulses of 70 ns and 0.83 mA can RESET the memory cell with around 100 times difference of electrical resistances between the amorphous and crystalline states as shown in Fig. 6.10 (a). When the initial state of memory cells were at amorphous sate, the minimum amplitude of current pulses for SET was 0.46 mA and the minimum amplitude for RESET was 0.96 mA as shown in Fig. 6.10 (b).

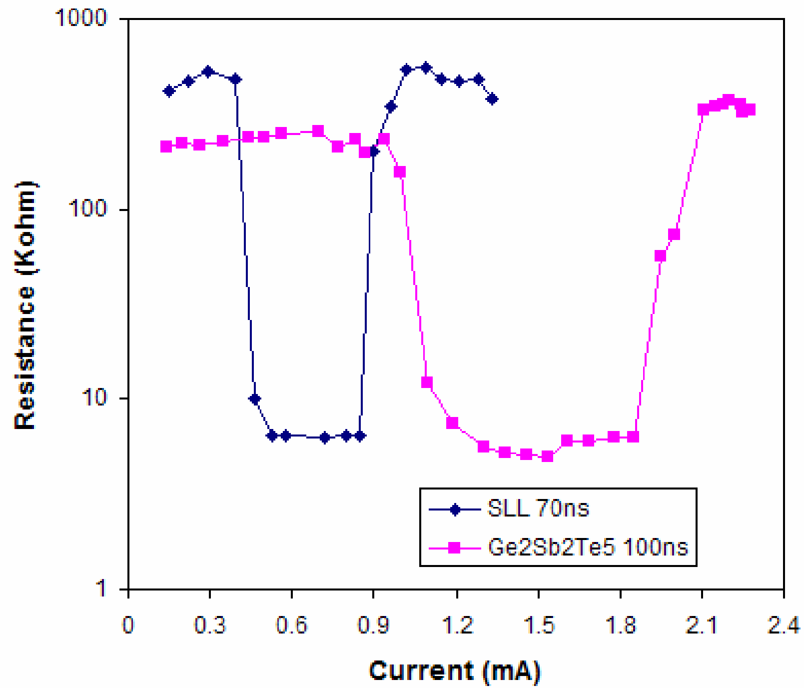
In Fig. 6.10 (c), the SLL_PCRAM is compared to the conventional $Ge_2Sb_2Te_5$ PCRAM. Because 70 ns electrical pulse could not SET the $Ge_2Sb_2Te_5$ PCRAM memory in this experiment, 100 ns program pulse was used. It was found that even with longer electrical pulse, the minimum SET and RESET current for $Ge_2Sb_2Te_5$ PCRAM programming were 1.1 mA and 2.11 mA respectively, much higher than SLL_PCRAM. Therefore, the SLL_PCRAM structure showed the ability to reduce the program current almost by half compared to conventional $Ge_2Sb_2Te_5$ PCRAM.




(a)



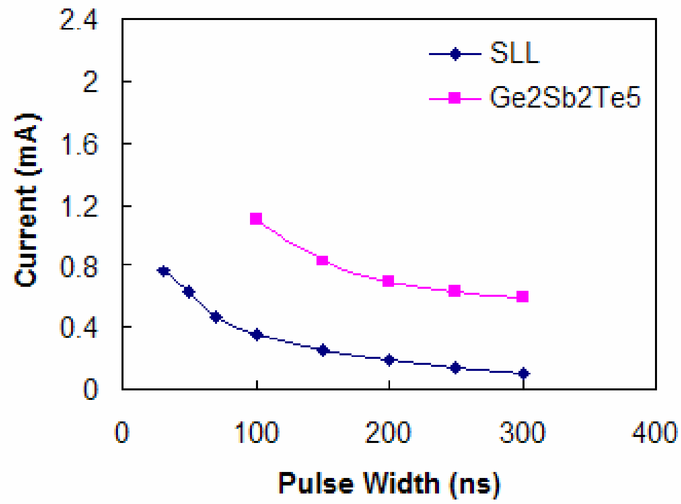
(b)



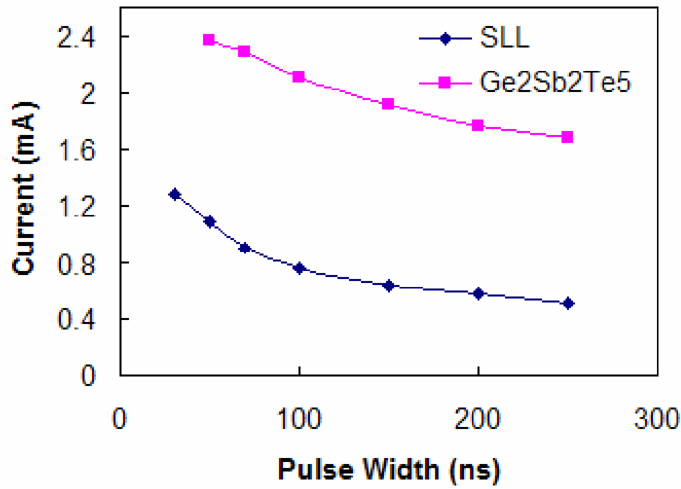

(c)

Fig. 6. 10 The low current operation of the SLL_PCRAM (a) programming from the crystalline state (b) U curve (c) the R-I curve compared with $Ge_2Sb_2Te_5$ PCRAM.

Figures 6. 11 (a) and 6.11 (b) show the SET and RESET programming current as a function of pulse width for SLL_PCRAM and conventional $Ge_2Sb_2Te_5$ PCRAM, respectively. In these figures, the SET and RESET programming currents are the minimum currents required to induce resistance change. It can be seen that, both SET and RESET currents are smaller for cell with SLL structure than those with conventional $Ge_2Sb_2Te_5$ with the same pulse width. It can also be observed that the device with SLL structure could work with much shorter pulse widths for both SET and RESET when compared to the device with a single $Ge_2Sb_2Te_5$.




(a)




(b)

Fig. 6. 11 (a) SET programming current as a function of pulse width (b) RESET programming current as a function of pulse width.

**Long Life Cycles**

Life cycle is the number at which the memory cells that can be reliably programmed. In life cycle testing, the memory devices were written to crystalline state and amorphous state alternatively. It is an important parameter for the memory devices. The software interface for the life cycle test is shown in Fig. 6.12.

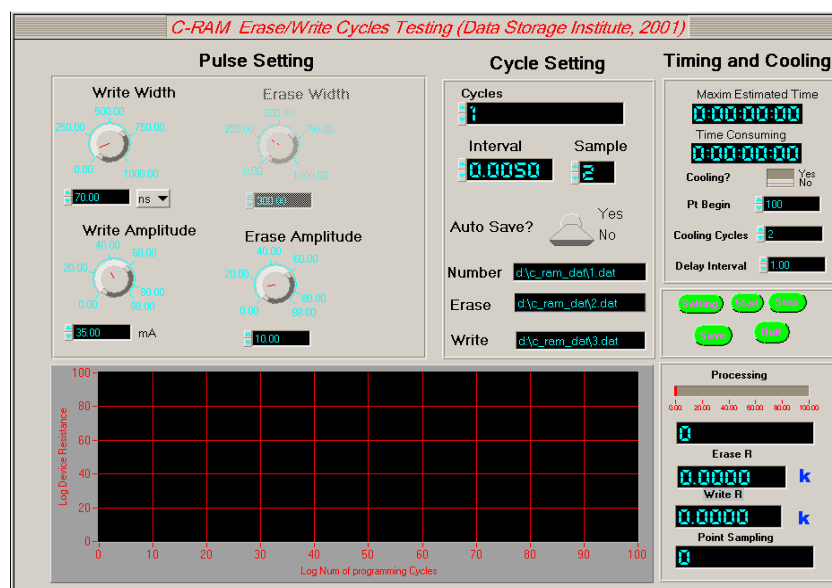



Fig. 6. 12 The life-cycle measurement of memory testing bench.

In the experiment, 0.2 V voltage was constantly applied to the device to read the memory bits. After every 10000 times SET and RESET, the resistance was recorded. The test result of life cycle in SLL_PCRAM is shown in Fig. 6. 13. It can be noted that larger than 100 times difference of resistances between amorphous state and crystalline state after $10^6$ times programming.

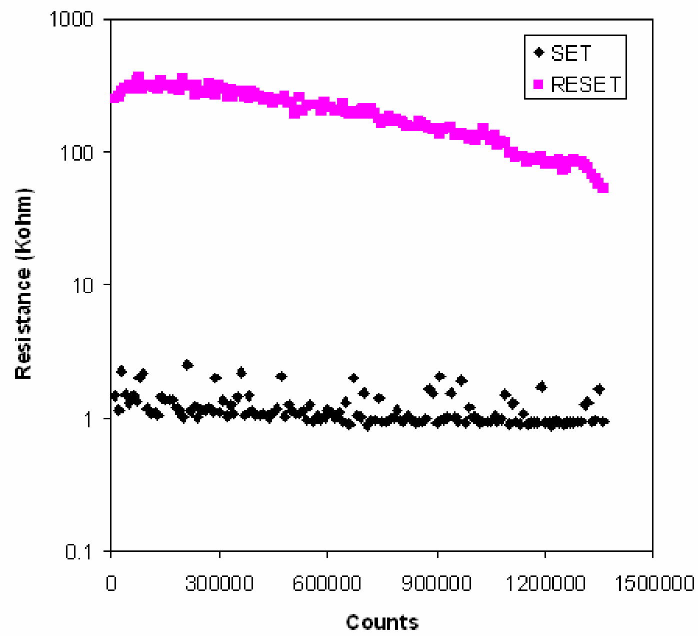



Fig. 6. 13 Overwriting cycles of SLL_PCRAM chips.

### High Reliability

The reliability refers to the maximum number for which the data can be correctly read out. Because the reading is realized by applying a small constant current or voltage across the memory cells, it still generates heat in the phase change material. Therefore, the reading may change the data after certain read cycles. The software interface for reliability measurement is shown in Fig. 6.14.

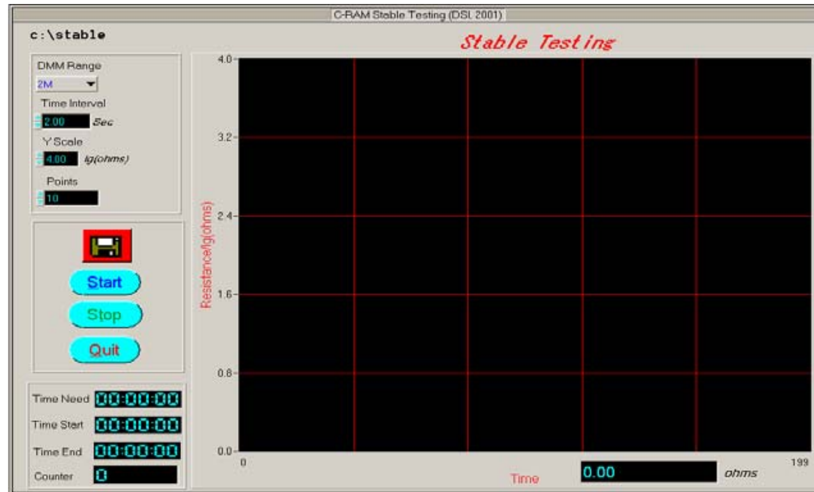



Fig. 6. 14 The reliability measurement of memory testing bench.

In this experiment, the reliability test was carried out by constantly reading the resistance of a memory cell, at both amorphous and crystalline states. 0.2 V voltage was used for reading. Different from the life cycle measurement, memory cell would not be programmed during the reliability testing. The reading process showed negligible effect on the data even after $10^6$ times readings between two read pulses as shown in Fig. 6.15.

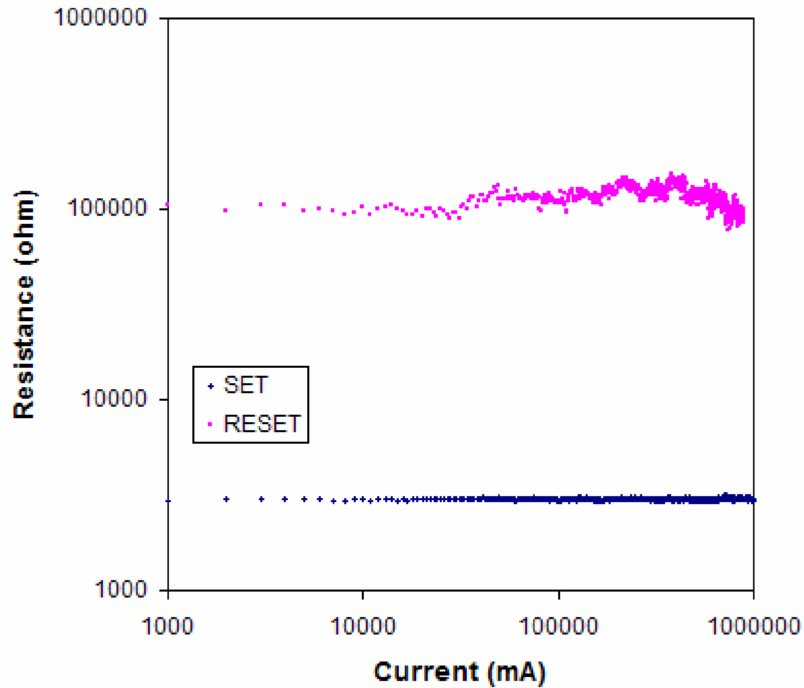



Fig. 6. 15 Reliability cycles of SLL_PCRAM chips.

### 6.3.3 Discussion

SLL_PCRAM chip has shown lower programming current compared to conventional $Ge_2Sb_2Te_5$ chip. It can be explained by the thermal, electrical and crystallization properties of SLL structure discussed in Chapter 4.

Theoretically and experimentally, the SLL structure has lower thermal conductivity compared to single compound. The better confinement of heat can significantly reduce the programming current and increase the crystallization speed (Chong, et. al., 2006).

In addition, as discussed in Chapter 4, the multilayer structure, which generates the higher electrical resistivity is beneficial for the current reduction. Simply speaking, the programming current is directly related to the electrical resistance of phase change

devices as shown in Equation 6.1 and 6.2:

$$W = R \times I^2 \tag{6.1}$$

$$T = \int_{t0}^{t1} \frac{W_j - W_d}{C \times V} dt \tag{6.2}$$

Where, W is the power, R is the resistance of phase change devices, I is the programming current, T is the temperature, $W_j$ is the power of joule heat, $W_d$ is the power dispersed through electrodes and dielectrics, C is the thermal capacitance of the phase change material, V is the volume of phase change active region, and t is the pulse length.

Therefore, the higher the resistance of memory devices, the lower the required programming current for PCRAM devices to reach the crystallization or melting temperature. To increase the overall resistance, researchers added different heat layer, such as tungsten, tungsten nitride, silicon germanium and carbon to increase the resistance (Takaura, et.al, 2003, Moore, 2001; Xu, 2003; Lee, et. al, 2006). Similarly, the higher resistance brought by the multilayer structure can help to reduce the programming current.

## 6.4 Summary

In this chapter, the 128-bit SLL_PCRAM chip with 6-pair SLL_$Ge_2Sb_2Te_5$ structure was fabricated and tested. It demonstrated low current, long life cycle and good reliability. Especially for the programming current, there is 50% reduction compared to that of the conventional $Ge_2Sb_2Te_5$ structure with the electrical pulse less than 100 ns. This low RESET current can largely reduce the size of memory array and enhance the scalability of PCRAM technology. Furthermore, the speed, life cycle and reliability were also found

to be satisfactory in SLL_PCRAM. The physical mechanisms to explain the advantages of the application of SLL structure in the PCRAM technology were discussed.

In addition, this study verified the good compatibility between SLL structure and the CMOS technology.

# CHAPTER 7
# CONCLUSIONS

It is widely believed that the PCRAM is the best candidates for the next generation nonvolatile memories. Its superior scaling capability is attracting great interest from the semiconductor memory industry. In this thesis, the scaling limitations were investigated and the main results include:

- Proposed four categories of scaling limitations for PCRAM: the lithography technology, the physical limitation of phase change materials in PCRAM, the thermal-cross talk among memory cells and the current limitation in memory cells; this thesis focuses on the second and the fourth categories of the scaling limitations of PCRAM;
- Studied the physical limitation of phase change materials in PCRAM based on a newly proposed classification of the phase change processes: a phase change in the free scale, the phase change between metals/oxides and the reversible phase change between metals/ oxides. The limitation for reversible phase change with metal/ oxides was found to be the physical limitation for PCRAM technology.
- Developed a thickness-dependent thermal electrical method to study 3D phase change in nano-scale; found that the root causes of limitations for phase change in above three categories are the critical size of nuclei, the interface effect and the diffusion effect, respectively;
- Provided solutions to extend the physical limitation;
- Introduced the physical kinetics of thickness dependent nano-crystallization,

including the crystallization of active energy and the Avrami coefficient;

- Explored the electrical, crystallization and thermal properties of advanced SLL phase change structure and reported its layer dependent and compositional dependent effects;
- Developed 128 bit chip to demonstrate the low current performance of SLL_PCRAM at chip level, and at the same time highlighted the compatibility of phase change materials and the standard CMOS process;
- Generated an innovative HSPICE macromodel of PCRAM memory cells, which is meaningful in integrating PCRAM technology into IC simulators.

## 7.1 Summary

The booming market in electronic devices has been a strong driving force for NVM technologies. Small size, high speed, low power consumption, long data retention time and low costs are the common requirements of various memory technologies. PCRAM, as the best candidate for the new generation of NVM, possesses an attractive performance radiation-hard nature and scalability. Besides its radiation-hard and high-performance natures, the most important advantage of PCRAM over other NVM is the high scaling potential. The purpose of this thesis is to study the scaling limitations of the PCRAM technology.

Although PCRAM is the best scalable NVM technology, it still has limitations for smaller-sized devices. Four categories of scaling limitation for PCRAM were proposed in the areas of lithography technology, physical limitations of phase change materials in PCRAM, thermal-cross talk among memory cells and the current limitations of the

memory chips. Previously, lithography technology was believed to be the major limitation for this technique. However, it became less critical with the emerging of advanced lithography technologies for nano-scale applications. Of four categories of physical limitations, this thesis focused on the physical limitation of the phase change materials in PCRAM and current limitation of the memory chips.

To study the physical limitation of phase change materials in PCRAM, a classification of phase change process was proposed by considering the surrounding interfaces: (1) phase change in free scale, (2) phase change sandwiched between metals/oxides and (3) reversible phase change sandwiched by metals/oxides. The limitation for phase change process in each category was studied. A thermal electrical method was developed to simplify the physical limitation study from 3D issue to thickness-dependent issue. The experimental results on $Ge_2Sb_2Te_5$ showed that different factors affected the limitations in different categories. In free-scale, the limitation for crystallization was 0.52 nm. In the second category, the crystallization was limited by interfacial energy and the limitation was around 3 nm. For the reversible phase change, high temperature diffusion was critical and it changed the limitation to above 10 nm. Solutions were proposed and successfully demonstrated to extend the limitation.

During investigation of the limitation in phase change material sandwiched by dielectrics, the interface effect was found to significantly affect the phase change process. Therefore, a systematical study on interface-dominated nano-crystallization in phase change materials was carried out. It was found that when the film thickness was below 20 nm, an exponential increase of the crystallization temperature happened with decreasing film thickness. Furthermore, the crystallization speed was decreased with a reduction of

film thickness. Based on the Kissinger plot and the JMA model, the crystallization kinetics including the crystallization mechanism, the corresponding activation barrier and the Avrami coefficient were investigated. The crystallization activation energy increased from 2.86 eV in 30 nm thick films, to 4.66 eV in 5 nm thick films. The increase in activation energy could be explained by the thickness dependent interfacial energy model and was believed to be the main reason for the increase of crystallization temperature. In the films thinner than 10 nm, the 2D nucleus growth, corresponding to an Armani coefficient $n < 1$, was proposed to account for the decrease of crystallization speed.

Besides the physical limitation of the phase change materials in PCRAM, the current limitation in memory chip is another topic for the study of PCRAM scaling. It refers to the relatively high RESET current required for PCRAM cells, which would limit the scalability of PCRAM chips because the higher current would need the larger-size access transistor to supply enough current as well as the greater distance among memory cells to avoid thermal cross-talk.

To overcome the current limitation on PCRAM chips, the SLL structure phase change material was studied. The basic concept of SLL structure is to alternatively deposit two phase-change materials with different electrical, thermal or crystallization properties. In this thesis, $Sb_2Te_3$, with a high crystallization speed, and GeTe, with a relatively low crystallization speed but a high stability, were chosen. The electrical, crystallization and thermal properties were found to be related to layers and composition. On one hand, experiments indicated that for the same artificial composition, the structure with more layers would have higher $T_x$ and higher electrical resistance. On the other hand, SLL_$Ge_2Sb_2Te_5$ was found to have lower $T_x$, electrical resistance and crystallization

speed compared to SLL_$Ge_6Sb_2Te_9$. The results demonstrated the flexibility for design of this SLL structure by interface and nano effect.

Lastly, a 128-bit SLL_PCRAM chip was developed to demonstrate its performance, current consumption and stability. The chip development included three steps: an integrated circuit design, memory chip fabrication and characterization testing. For the IC design of the memory chip, an innovative macro-model of phase change memory cell was proposed. All parameters in this macro-model were the physical parameters of the device, which made this model flexible and universal. Furthermore, a four-level macromodel was developed for the multi-level storage application. Based on this macro-model, a 128-bit PCRAM chip was designed and simulated. The design was used to fabricate the 6-pair SLL_$Ge_2Sb_2Te_5$ PCRAM and $Ge_2Sb_2Te_5$ PCRAM for studying the superior performance of SLL structure. SLL structure PCRAM showed a 50% reduction of RESET current with satisfactory speed, reliability and life cycle.

Above results may provide a useful understanding of the scalability limitations of PCRAM, ranging from the basic materials to the integrated memory chip. Furthermore, the model and methodology used in this thesis are universal and applicable in future developments of PCRAM technology.

## 7.2 Future Research

The study on scaling limitation in this thesis mainly focused on the thickness in vertical dimension. The investigation of 3D limitations may become feasible with the development of lithography technology. Currently, advanced lithography technologies such as NSOM and E-beam are used to fabricate memory cells with critical size of less

than 20 nm. Therefore, the physical limitation in 3D can be a topic for future research.

Furthermore, because different phase change materials have different interfacial energies when they are sandwiched by different dielectrics, investigating the thickness dependent effect of other phase change materials, such as AgInSbTe and BiSbTe, would be meaningful. The physical limitations of these materials can also be a topic for future study.

The integrated circuit design for PCRAM, especially the design for high capacity memory chips, is the other topic. Compared to the 128-bit PCRAM developed in this thesis, the integrated design of high capacity memory chips is much more complex. The long bit-line usually causes severe drop of voltage during the reading process. It will bring new challenges to the design work of the sense amplifier. Furthermore, new challenges will also appear concerning the timing, the delay and the power consumption when the memory capacity is increased.

The SLL structure is a new approach for material engineering in PCRAM technology. Although its application has been successfully demonstrated in PCRAM based on GeTe and $Sb_2Te_3$ materials, other combinations of materials, such as the growth dominant AgInSbTe, may have different properties which are plausible for certain applications. Material engineering of the SLL structure would be a very important and meaningful topic for the future research. More studies should be carried out to explore the principles of the superior current/ power and the speed performance of this technology.

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