DUAL-BAND FSK RECEIVER AND BUILDING BLOCK DESIGN FOR UWB IMPULSE RADIO

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I. ABSTRACT

A CMOS non-coherent impulse radio receiver implementing a dual-band frequency shift keying (FSK) modulation scheme for ultra-wideband communication is presented. The quadrature direct-conversion architecture of the receiver retains low-complexity operation while the added diversity gain of the FSK modulation enables reliable demodulation at signal to interference ratio (SIR) as low as –60dB. Several innovative circuit structures including an area and power efficient UWB low-noise amplifier utilizing active inductors and a hybrid topology mixer to extend operational bandwidth without compromising conversion gain have been explored. In addition, a 4-bit R-2R DAC capable of less than 0.5 LSB INL and DNL, a four-quadrant squarer with squaring gain of 65 and a dual threshold comparator with more than 700mV hysterisis and have also been designed.

The fabricated receiver achieves a sensitivity of -88 dBm at a BER of 10^{-5} at 25 MHz data rate with an energy efficiency of 2.7 to 4.95 nJ/bit.

Keywords: ultra-wideband (UWB), receiver, low-noise amplifier, frequency shift keying (FSK), digital to analog converter (DAC), active inductor

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SUMMARY

Ultra-wideband technology is fast gaining popularity in high speed, short range wireless communication and localization applications due to its extremely low transmission levels and ability to share the congested 3-10 GHz communication band with other existing narrow-band devices. However, due to its unique pulse based implementation, the design of conventional I-UWB receivers differs significantly from traditional radio systems and generally suffers from added system complexity due to the additional circuit blocks needed for synchronization and channel estimation requirements. In this thesis, an alternate I-UWB receiver structure based on a novel system approach which incorporates the unique benefits of UWB while at the same time reducing design complexity and achieving better interference rejection is proposed and discussed.

A new dual-band FSK modulation scheme using conventional short monocycle Gaussian pulses and the corresponding receiver system architecture capable of implementing this scheme are described in detail. Based on these system characteristics, required RF components are designed in Chartered Semiconductor's 0.18μm process and analyzed. Several building blocks required for system implementation including an LNA, mixer, DAC, squarer and comparator are designed and their functionality is analyzed in detail both theoretically and through extensive simulation and measurements.

Active inductors are utilized in the LNA design in order to achieve a

drastically reduced chip size of 0.05mm^2 while maintaining wideband (3-5GHz) operation with a gain of 15.1dB and noise figure (NF) between 4.95dB to 6.1dB while consuming 7.1 mW. A hybrid UWB mixer structure which combines the gate-source injection and Gilbert cell topologies in order to extend the operational bandwidth without compromising conversion gain has been implemented. It can achieve greater than 5.5dB conversion gain with 11dB NF and excellent isolation over the entire 3.1-4.8 GHz bandwidth. A 4-bit R-2R resistor ladder structure is used to implement the DAC which is capable of less than 0.5 LSB INL and DNL performance with less than 25ns settling time for maximum output voltage step (0-1.8V). A four quadrant baseband squarer with a squaring gain of 65 and input bandwidth of 210MHz is also utilized. The comparator has a dual threshold operation with more than 700mV hysterisis and is also capable of excellent signal integrity and load driving capabilities.

As the final objective of this work, the various component blocks are laid out and are used to realize the proposed receiver system in 0.18μm CMOS technology. The feasibility of implementation of the proposed I-UWB system and its functionality are confirmed and its unique ability to reject in-band interference is also demonstrated. The receiver can achieve a voltage sensitivity of up to 90μV and IIP3 of -32 dBm at a data-rate in excess of 25 MHz while consuming between 48 to 84 mA current from a 1.8V source.

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LIST OF SYMBOLS AND ABBREVATIONS

C_L	Load Capacitance
I_{ds}	Drain to source current of a MOSFET
I_{out}	Output current
M	Symbol for MOS transistor
g_{mA}	Transconductance of MOSFET M_A
r_o	Drain source resistance of mos transistor
$Z_{in/out}$	Input/ Output resistance
V_{ctrl}	Control voltage for QVCO
V_{DD}	Positive supply voltage
V_{out}	Output voltage
V_T	Threshold Voltage
ω_p	Pole
A_v	Voltage Gain
V_{ds}	Drain-source voltage of MOSFET
K	Transconductance parameter of MOSFET
μ_0	Mobility of MOSFET
C_{ox}	Unit gate capacitance of MOSFET
W/L	Aspect ratio of MOSFET

ADS	Advanced Design System
CMOS	Complementary MOS
DLL	Delay Lock Loop
FCC	Federal Communication Commission
IC	Integrated Circuit
ICS	Integrated Circuit and Systems
IME	Institute of Microelectronics
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NMOS	N-channel Metal Oxide Semiconductor
NUS	National University of Singapore
RF	Radio Frequency
SNR	Signal to Noise Ratio
UWB	Ultra Wide band

Chapter 1

Introduction

1.1 Overview of UWB Communications

Over the past decade, the notion of traditional wired telecommunication which has prevailed for over half a century has become obsolete and is rapidly being replaced by wireless communication systems. From global applications like cellular telephones, wireless internet networks and Global Positioning System (GPS) to personal applications like personal digital assistants (PDA) and Bluetooth, wireless technology is gaining a presence in every facet of our lives. However, to sustain this presence, new wireless technologies are required that can achieve higher speeds and higher data-rates so as to meet the ever changing demands of today's devices.

Ultra wide-band (UWB) is an emerging wireless technology which shows great potential for short range, high data-rate communication and localization applications. The biggest advantages of the UWB technology are derived from the fact that it utilizes a much wider bandwidth and operates at much lower power levels than traditional narrowband systems. This statement is supported by the Shannon-Hartley Theorem (Eq. (1.1)) for channel capacity which states that in an additive white Gaussian noise (AWGN) environment, the maximum channel capacity (C) is directly proportional to the bandwidth (B) of the channel and to the logarithm of signal to noise ratio (SNR).

$$C = B\log_2(1 + SNR) \tag{1.1}$$

This means that the wide operational bandwidth of UWB communication allows it to achieve higher data-rates more cost-effectively (i.e. without an exponential rise in signal

power) than narrowband systems while at the same time the very low transmission levels allow co-existence between UWB and existing standards. The unique features of UWB technology are especially beneficial in short range applications where it can achieve much higher channel capacities than existing standards as shown in Fig. 1.1 [3]. Moreover, the narrow pulse based nature of UWB makes it much less immune to multipath distortion due to destructive fading than narrowband systems.

UWB technology is at present defined by the Federal Communications Commission (FCC) as any wireless transmission scheme that occupies a fractional bandwidth of more than 20% with respect to its center frequency or more than 500 MHz of absolute bandwidth. More specifically, the FCC has approved the unlicensed deployment of UWB in the 3.1-10.6 GHz range subject to strict regulations that limit the emitted power spectral density (PSD) measured over a 1 MHz bandwidth to below -41.3 dBm as shown in Fig. 1.2 [1].

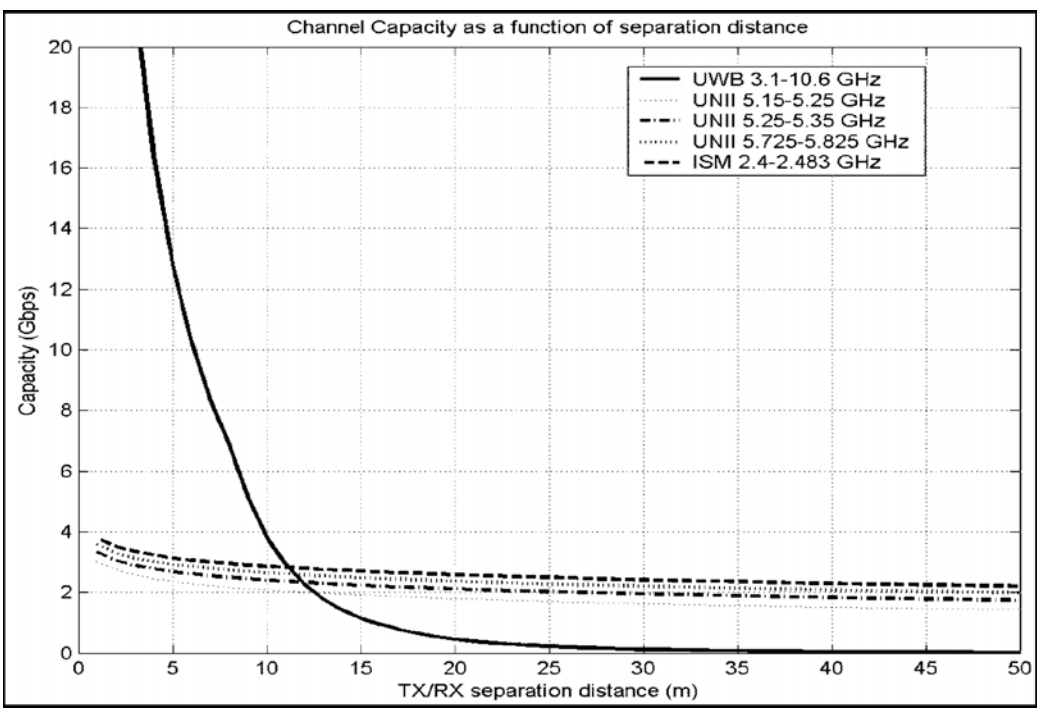


Fig. 1.1 UWB capacity versus other WLAN technologies

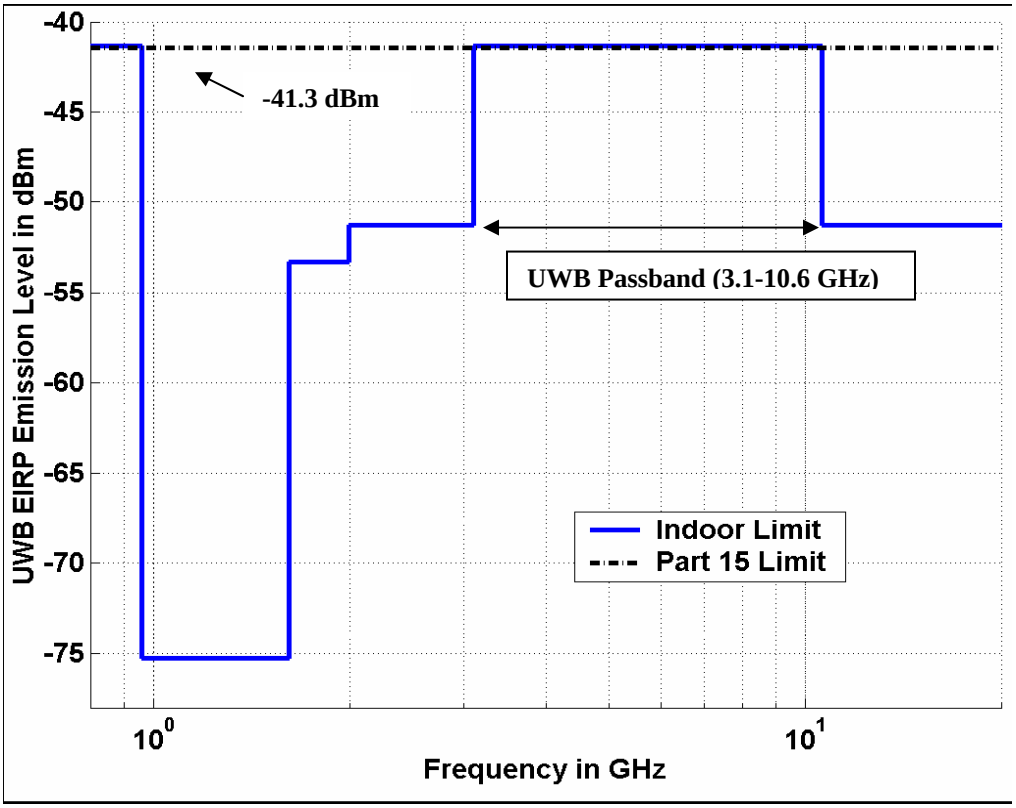


Fig. 1.2 FCC Spectral Mask for UWB Communication Systems

1.2 Motivation

Due to its unique features, in recent years UWB has found applications in high speed short range wireless data connectivity between several remote hosts as well as in sensor networks and precision localization and ranging. With the significant interest being shown by the research community and a concerted effort on the part of the regulatory bodies to finalize the standards, the future is looking very bright for UWB technology and it is tipped as having potential for realizing an exciting new set of applications that are presently not being fulfilled by other wireless short range technologies currently available (e.g., 802.11 LANs (Local Area Networks) and Bluetooth PANs (Personal area networks)).

The key to successful implementation of any telecommunications platform in mainstream applications is the cost feasibility, robustness and reliable performance of the end product. These demands are especially difficult to meet at the high operating frequencies of UWB devices and pose unique challenges to circuit designers.

In this thesis, a UWB receiver architecture which utilizes a novel dual-band FSK modulation scheme for a UWB impulse Radio (IR) system is proposed. The design of the building blocks has been done in the 0.18μm CMOS technology provided by Chartered Semiconductors foundry. All the constituent components have been built in silicon CMOS technology instead of using specialized III-V technologies like GaAs or SiGe which provide better RF performance in terms of output power, linearity and phase noise. This choice is made because silicon CMOS in the most mature and cost effective technology and at the same time guarantees better yields and a larger scope for future integration with baseband and digital processes.

1.3 Organization of the Thesis

Chapter 2 is dedicated to briefly introducing some fundamental RF design concepts to facilitate the understanding of the rest of the thesis.

In chapter 3, popular receiver architectures for conventional narrowband well as DS-UWB systems are briefly reviewed. The related Binary Phase Shift Keying (BPSK) and Frequency Shift Keying (FSK) modulation schemes are also discussed.

In Chapter 4, a new modulation scheme for I-UWB applications, ‘dual-band UWB FSK’ is proposed and the quadrature receiver designed to implement this scheme is discussed

Chapter 5 concentrates on design of the various UWB receiver building blocks for the required application and their performance. Blocks including an LNA, mixer, DAC, squarer and comparator are discussed in detail. Blocks designed by group members are briefly introduced.

In chapter 6, detailed simulation results of the aforementioned receiver system are shown. Measurement results from tests carried out on the fabricated front-end alone are also given

Conclusions drawn from this work are given in Chapter 7 along with suggestions for future work.

Chapter 2

RF system design fundamentals

Even though the receiver structures used in UWB telecommunication have several parallels with more conventional low frequency narrowband systems, the design of the various required components is radically different due to the unique demands of RF wide bandwidth operation. In order to understand these challenges better, this chapter is dedicated to briefly explaining some of the key RF design parameters and the ways in which these specifications are met.

2.1 Impedance matching

In order to achieve the best possible system performance in any electrical system, it is essential to ensure that there is a maximum transfer of power between the output of each block and the input of the subsequent block. In the case of passive devices with fixed input and output resistances, this condition can be achieved by making the load and source resistances the same. However in the case of active devices with reactive input and output impedances, the condition for maximum power is met when the source and load impedances are complex conjugates of each. In all practical electrical structures, including the circuit blocks that will be discussed in this thesis, the latter situation applies and hence special attention needs to be paid to ensure that proper impedance matching is obtained.

However, since the inherent reactive properties of successive blocks almost never match each other, it is often necessary to add an impedance matching network to achieve maximum power transfer. As shown in Fig 2.1, in most cases an impedance matching network is a specific configuration of suitably chosen reactive components (capacitors or inductors) that buffer successive stages in a circuit chain so that the effective load and source impedances seen by each block satisfy the maximum power transfer requirement.

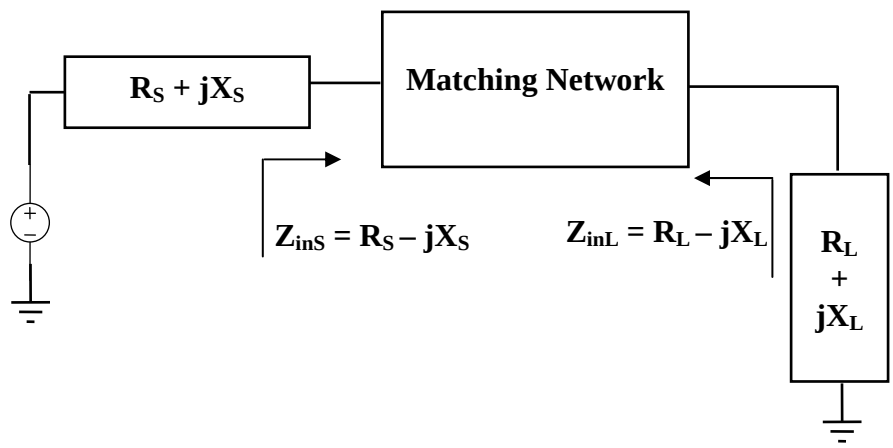


Fig. 2.1 Conjugate matching of reactive impedances using a matching network

2.2 Scattering Parameters

One of the biggest challenges in RF circuit design is posed by the fact that at high frequencies, the impedance of even small reactive components becomes significant and hence cannot be neglected. This means that all parasitic elements of the transistors, transmission lines, bonding wires etc. need to be included in the design process to achieve accurate results. But in doing so, the process of circuit design from basic design equations becomes overly complex and intractable. Scattering parameters are an essential circuit design tool that allows the accurate and efficient characterization of even the most complex component in a way that simplifies the design steps considerably.

The S parameter representation of any *N*-port electrical network is an *N* by *N* matrix as shown in Fig 2.2 which characterizes the network in its entirety as an *N*-port 'black box' based on its response to various steady state small signal stimuli. Various circuit performance parameters can be easily derived directly from this simple and handy representation. The S-parameter based metrics used extensively in the design and analysis of the 2-port circuit blocks described in this thesis are as follows:

Scalar logarithmic gain, $A = 20\log_{10} |S_{21}|\, dB$

Input Return Loss, $RL_{in} = |20\log_{10} |S_{11}|| \, dB$

Output Return Loss, $RL_{out} = |20\log_{10} |S_{22}|| \, dB$

Reverse Isolation, $A_{rev} = 20\log_{10} |S_{21}|\, dB$

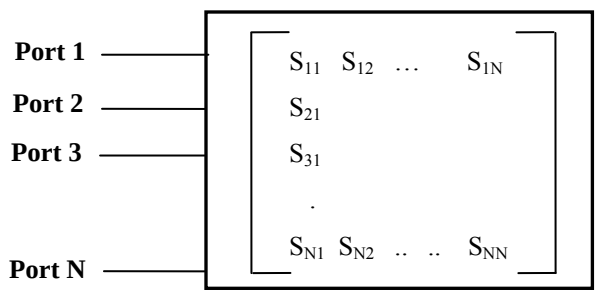


Fig. 2.2 S-parameter representation of an *N*-port network

In all the following S-parameter usage, a characteristic impedance of 50Ω is assumed.

2.3 Noise Figure

Noise can be seen as any undesired interference signal present in a system within the pass band of the desired signal. Noise adversely affects the signal detection capability of the system. Several forms of noise have been identified in electrical devices including

thermal noise and flicker noise. Noise can be characterized as a random variable with Gaussian distribution and zero mean and is generally quantified as a root mean square (RMS) value over a specified time interval as

$$V_{nRMS} = \sqrt{\int_{T_0}^{T_0+T_M} [v_n(t)]^2 \, dt} \tag{2.1}$$

where $v_n(t)$ is the instantaneous noise voltage variable and T_0 to T_0+T_M is the time interval of interest.

The source of noise in conductors is the inherent random motion of charge carriers. In particular, the two major sources of noise in any RF circuit are the thermal noise of resistors and transistors. These can be quantified as follows [11]

$$V_{nRES}^{\ 2} = 4kTRB \tag{2.2}$$

$$V_{nMOS}^{\ 2} = 4kT\gamma g_m B \tag{2.3}$$

where k is Boltzmann's constant (1.38 x10^{-12} J/ ^{o}K), T is the absolute temperature in ^{o}K, B is the noise bandwidth (Hertz) of the system and V_{nRES} and V_{nMOS} represent the RMS thermal noise voltages of a resistor R and a MOSFET in saturation with transconductance g_m and γ represents a technology dependant coefficient (γ = 2/3 and > 4/3 for long and short channel devices respectively).

In circuit design, noise figure (NF) is a measure of the degradation of the signal to noise ratio (SNR), caused by components in the RF signal chain. In other words, the noise figure is the ratio of the total output noise power of a device to the portion thereof attributable to the noise at the input from the source.

$$NF = 10\log_{10}\frac{SNR_{in}}{SNR_{out}} \tag{2.4}$$

NF is an important metric for almost all radio components and low NF is essential for high system sensitivity.

2.4 Linearity and IIP3

All devices are non-linear to some extent and it is unrealistic to expect even the most carefully designed circuit to behave perfectly linearly over all input power levels. Therefore the transfer function of a device can be modeled by Taylor series expansion as

$$V_{out} = k_1 V_{in} + k_2 V_{in}^{\ 2} + k_3 V_{in}^{\ 3} + \ldots \qquad (2.5)$$

where $k_{1..n}$ are known constants. Now assume that the device is excited by an input signal consisting of two adjacent frequency tones so that $V_{in} = A\cos\omega_1 t + A\cos\omega_2 t$. Then by expanding the output term and applying some basic trigonometric identities, we find

$$V_{out} = \alpha_1 A(\cos\omega_1 t + \cos\omega_2 t) + \alpha_2 A^2(\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t)$$

$$- \alpha_3 A^3(\cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 t - \omega_1 t) + ..) + .. \qquad (2.6)$$

where generally $\alpha_1 > \alpha_2 > \alpha_3 > \ldots$

As seen in Eq. (2.6), for higher power levels, the output of the device gets more and more distorted by higher order harmonics. Since the 3rd order product components, $2\omega_2$-ω_1 and $2\omega_1$-ω_2 lie in close proximity to the desired frequency components, they merit special attention. Fig. 2.2 [12] illustrates the behavior of the third-order intermodulation products as input power level increases. With the input and output powers plotted on a log scale, the intermodulation product amplitudes follow straight line trajectories with gradients proportional the order of the products. By extrapolating these lines, a theoretical threshold called Input referred 3rd order intermodulation point (IIP3) can be derived

which signifies the maximum input power level below which the fundamental tones are stronger than the 3rd order harmonics. IIP3 serves as a measure for the device's linearity.

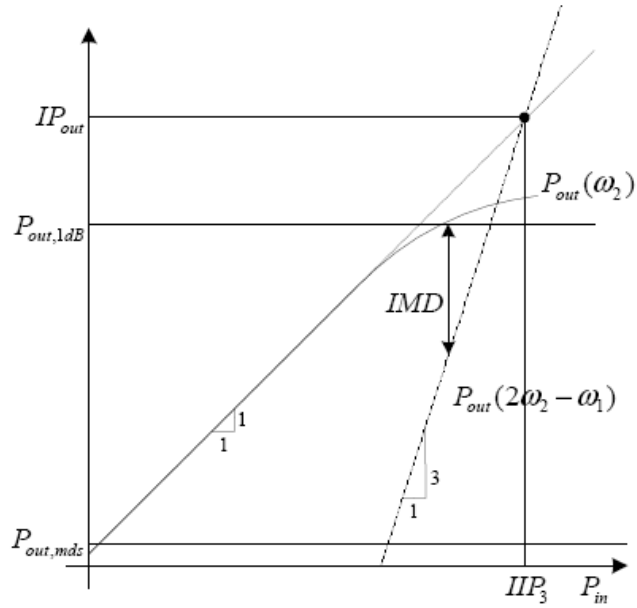


Fig. 2.3 3rd order intermodulation behavior and IIP3 definition

For N cascaded stages, the IIP3 of the system ($IIP3_{total}$) can be expressed as:

$$\frac{1}{IIP3_{total}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \ldots\ldots + \frac{G_1 G_2 \ldots\ldots G_{n-1}}{IIP3_n} \tag{2.7}$$

Where $IIP3_n$ is the IIP3 of the nth stage, G_n is the power gain of the nth stage.

2.5 Signal to Noise ratio

SNR is a measure of the clarity of a signal. It is defined as the ratio of a signal power to the background noise power corrupting the signal and can be written as

$$SNR = \frac{P_{signal}}{P_{noise}} \tag{2.8}$$

2.6 Minimum detectable Signal (MDS)

MDS is another key performance metric for any receiver system and quantifies its sensitivity to weak input signals. It signifies the smallest possible input signal that can be successfully detected and demodulated by the receiver chain. In practical terms, the MDS is determined by the Noise Floor, which represents the sum of all present noisy sources within the system and the minimum possible SNR of the device. It can be written as [13]

$$MDS = P_n + NF + 10\log BW + SNR_{\min} \tag{2.9}$$

where BW is the bandwidth of the system and P_n represents the average noise power per unit frequency bandwidth (approximately -174 dBm/Hz) at the input to the device. Note that the sum of the first three terms represents the noise floor of the system.

2.7 Dynamic Range

In the same way that the noise floor determines the MDS of a system, the dynamic range determines the maximum possible input signal that the system can handle. We have seen in an earlier subsection how the IIP3 quantifies the non-linear nature of a system. But this input level is a purely theoretical value since in almost all real devices the output signal starts to saturate well before the IIP3 level is reached.

An alternative representation of the signal distortion is the 1 dB compression point. As the input approaches the system's saturation region, the output signal begins to fall. The point where the gain of the system deviates from its linear approximation by 1 dB is called the 1 dB compression point. The difference between the power levels of the 1 dB compression point and the MDS is defined as the Dynamic Range of a system as shown in Fig. 2.4 [12]. This represents the effective linear region of the system within which

input signals can be demodulated accurately without being distorted by noise or intermodulation products.

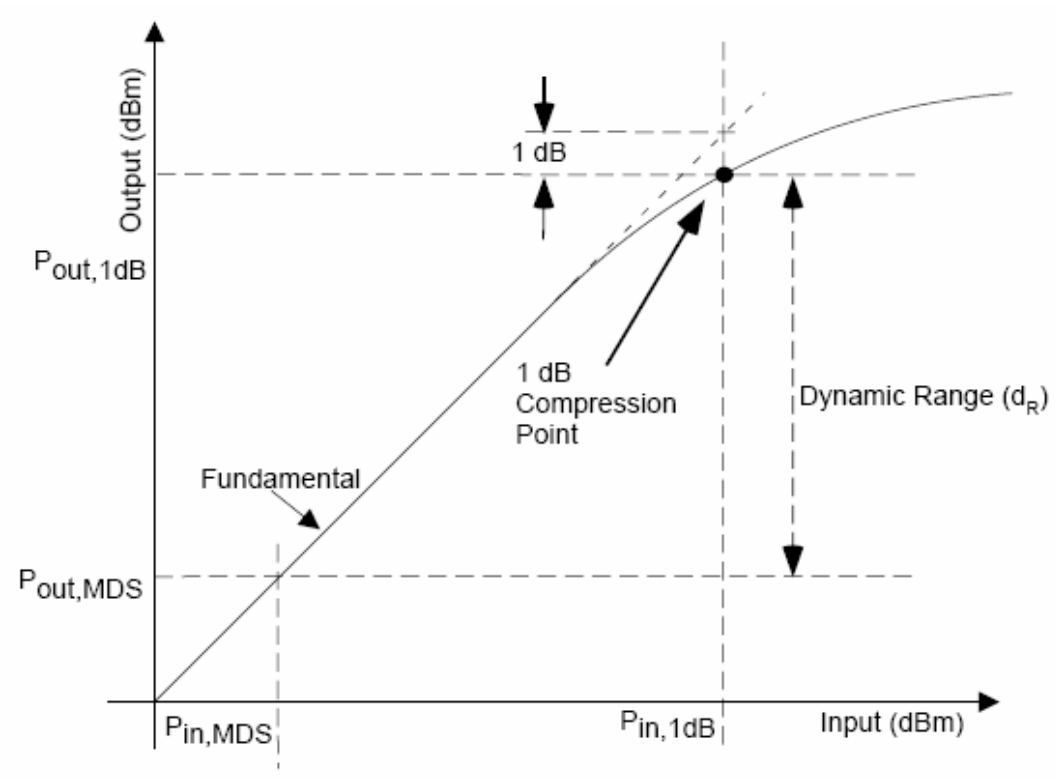


Fig. 2.4 Graphical definition of the dynamic range

Chapter 3

Conventional UWB receiver architectures

This chapter discusses various popular RF receiver architectures. The first section briefly reviews direct conversion and super heterodyne receiver architectures used for conventional narrowband wireless communication systems. The second section focuses on two of the most popular receiver architectures used to implement the DS-UWB scheme.

3.1 Narrowband receiver overview

3.1.1 Common modulation schemes

Most narrowband signals are characterized by a stream of digital data being modulated by a high frequency carrier signal to enable wireless transmission over long ranges. Several modulation schemes can be utilized in order to achieve this and they can be classed broadly into three categories, the somewhat archaic amplitude modulation (AM) and the more popular phase modulation (PM) and frequency modulation (FM). A brief understanding of the latter two modulation techniques can be garnered by analyzing two specific modulation schemes, namely binary phase-shift keying (BPSK) and frequency shift keying (FSK).

3.1.1.1 Binary Phase-Shift Keying (BPSK)

BPSK is an example of Phase modulation. In this scheme, the phase of a constant amplitude carrier signal is switched between two values (0° and 180°) according to the two possible signals corresponding to binary 1 and 0 respectively as shown in Fig. 3.1.

This scheme is also sometimes referred to as antipodal modulation since the two binary bits are negatives of each other. The sharp phase transitions involved have the effect of producing a very wideband transmitted spectrum. In order to combat this, M-ary PSK modulation schemes are utilized so that more than 1 bit of data can be transmitted per signaling interval and hence increase the bandwidth utilization.

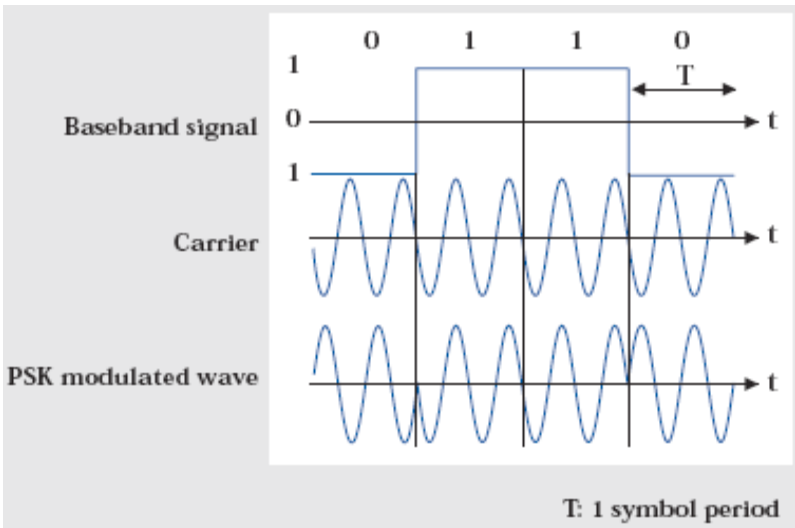


Fig. 3.1 BPSK Modulation

3.1.1.2 Frequency Shift Keying (FSK)

FSK is an example of Frequency modulation. In this scheme, the digital information is transmitted through discrete frequency changes of the carrier wave. So, a set of *M* different carrier frequencies are needed for *M*-FSK. Fig. 3.2 illustrates the modulation scheme in the 2-FSK mode. The main advantage of FSK over PSK is that the transmitted FSK signal has continuous phase characteristics and therefore occupies a smaller bandwidth for the same symbol rate. Moreover, the constant envelope nature of FSK modulated signals makes it impervious to the effects of filtering and spectral re-growth when passing through the devices in the receiver chain.

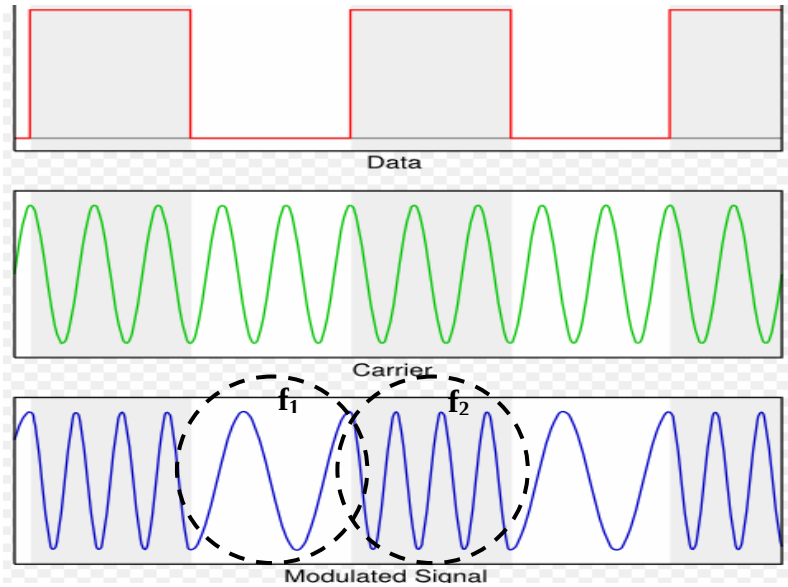


Fig. 3.2 FSK Modulation

3.1.2 Common receiver architectures

Before delving into the design of UWB receivers, it is instructive to first look at some conventional narrowband receiver designs. These receivers employ techniques that have been incorporated in the proposed UWB receiver design.

3.1.2.1 Direct Conversion (DC) receiver

The simplest RF receiver structure is of the DC variety which uses a single down conversion stage to convert the received RF signal directly to a demodulated baseband signal. In order to do this, the incoming signals are amplified and mixed with a local oscillator signal synchronized in frequency to the carrier of the wanted signal. The basic architecture of a DC receiver in shown in Fig. 3.3

The biggest advantages of the DC architecture are its simplicity and high selectivity. But it also suffers from several drawbacks that make it a less attractive candidate for robust radio design. These factors are:

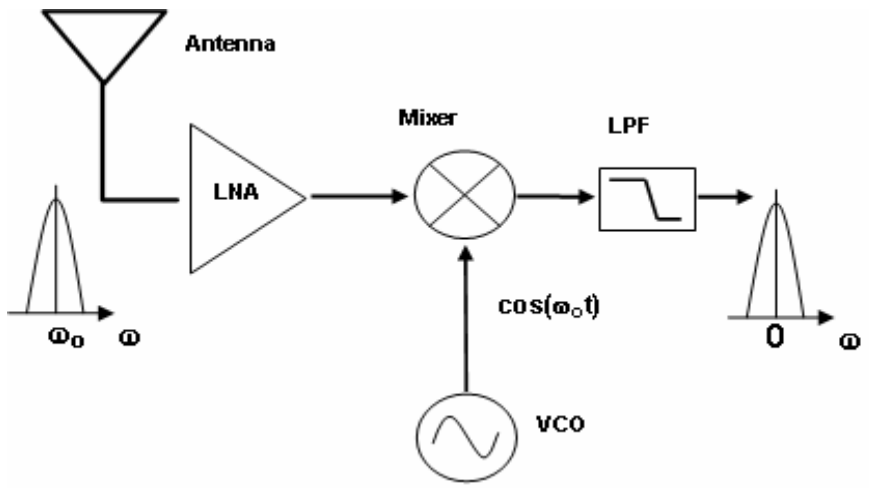


Fig. 3.3 Direct Conversion receiver architecture

DC Offsets

Since in a direct conversion topology the down-converted band extends to zero frequency, extraneous offset voltages can corrupt the signal and more importantly, saturate the following stages. In this respect, the phenomenon of self mixing of the LO signal due to inadequate isolation or the mixing product of a strong in band interferer can be detrimental to the receiver performance.

Flicker Noise

Since the down-converted spectrum extends to zero frequency, the flicker noise of devices, which can usually be disregarded due to its limited bandwidth, substantially corrupts the signals. This is a severe problem especially in MOS implementations.

Even order harmonics

Due to the single down-conversion stage employed, adjacent interference signals can produce even order inter-modulation products that occur near the desired down converted

baseband signal, thereby causing significant distortion that may not be removable by post filtering.

3.1.2.2 Super-heterodyne receiver

Heterodyne receivers are the most popular narrowband receiver architectures. In order to alleviate the problems caused by the zero intermediate frequency (IF) nature of direct conversion receivers, super-heterodyne receivers employ more than one demodulation stage with non zero IF. Fig. 3.4 shows a dual IF super-heterodyne receiver where the received signal in down-converted twice by two distinct LO frequencies ω_1 and ω_2 to IFs ω_{IF1} and ω_{IF2}.

In order to ensure proper demodulation while operating with non-zero IFs, an image rejection filter is required preceding every down-conversion stage in the super-heterodyne receiver chain. These filters require a band-pass response with sharp roll-offs often with very narrow pass bands which makes them extremely difficult to design. This combined with the requirement for additional VCO and mixer blocks for proper demodulation make the super-heterodyne architecture much more complex and inefficient with regard to power and area.

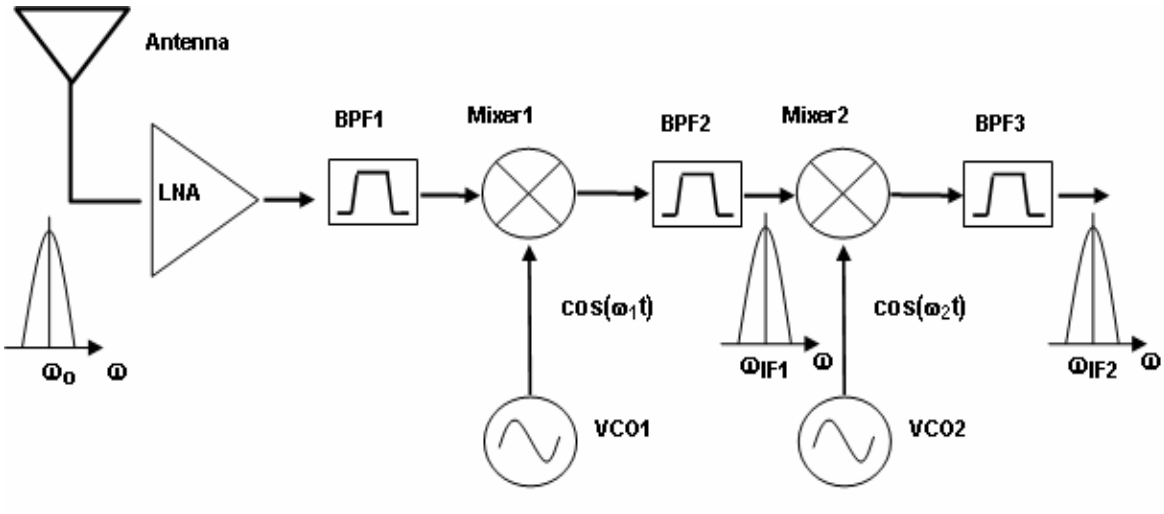


Fig. 3.4 Super-heterodyne receiver architecture

3.2 UWB receiver overview

There are two competing physical layer specifications available; one that is based on direct sequence spread spectrum (DS-UWB), and the other that is based on multiband orthogonal frequency division multiplexing (MB-OFDM) [4]. In MB-OFDM, entire UWB band is divided into several smaller sub-bands and orthogonal UWB pulse trains are generated using several equally spaced carriers. These pulse trains are then transmitted simultaneously in order to achieve high bit-rates and optimize the spectral efficiency. However, the need to generate and demodulate multiple carriers adds to the complexity of MB-OFDB transceivers. In addition, due to the loss of orthogonality of the various channel in a multipath fading channel, MB-OFDM systems often suffer from inter symbol interference (ISI) necessitating a high degree of synchronization [5], [9].

DS-UWB is an example of an Impulse-UWB (I-UWB) system. It utilizes narrow impulse signals to widen the bandwidth of the transmitted spectrum. Very narrow pulse width impulses can be chosen to occupy the whole UWB frequency band (3.1 – 10.6

GHz), or alternatively several types of impulse signals with different widths can be used, each occupying a sub-band of the whole UWB spectrum. The carrier-less nature of DS-UWB systems make the transceiver architecture much simpler and are also more robust in multipath fading environments while maintaining low transmit powers.

In this thesis, I-UWB based radios will be the focus and in order to better understand this system, two of the most common receiver structures in use today implementing DS-UWB are discussed in the following section.

3.2.1 DS-UWB receiver architectures

3.2.1.1 Coherent receivers

Coherent receivers rely on demodulation of the incoming pulse train by using a locally generated template to down-convert the received signal to baseband. The basic coherent UWB receiver architecture is shown in Fig. 3.5. The LNA amplifies the weak incoming pulses and subsequently the pulses are correlated with the local pulse templates in the multiplier and integrator. The integrator outputs a constant correlation level in each period for baseband processing which generally consists of gain stages followed by an Analog to Digital Converter (ADC).

The reason for the popularity of coherent receivers is the relatively simple architecture and large achievable data rates. However, the performance of this class of receivers is directly dependant on how well the locally generated template matches the incoming waveform in time and shape. Since narrow UWB pulses undergo significant distortion in multipath fading channels, it is extremely difficult to accurately model the local template pulse to fit the received pulse for operation over varying channel qualities

and transmission ranges. Moreover, the template pulses need to be synchronized with the incoming pulse train with sub-nanosecond precision and even small phase shifts can cause drastic deterioration in the correlation output.

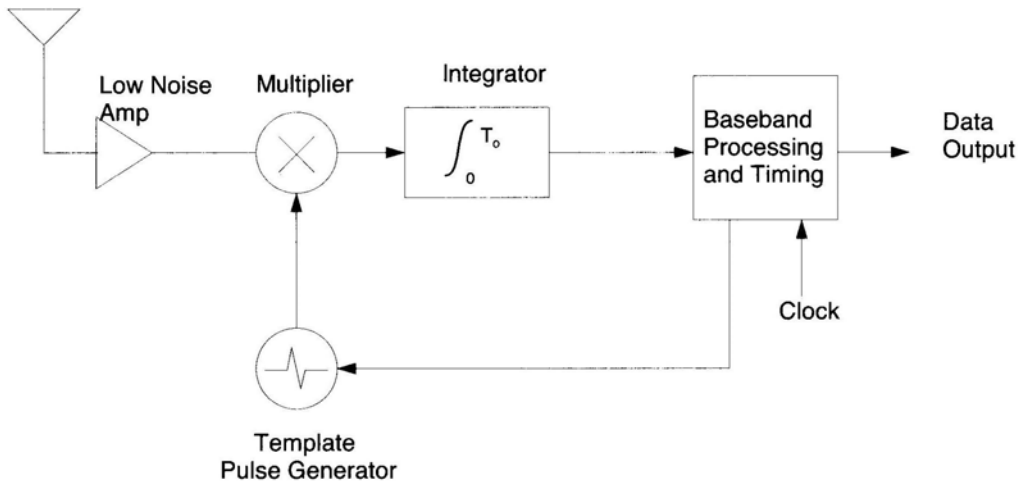


Fig. 3.5 Basic coherent UWB receiver architecture

Another major problem of this architecture is that of DC offsets similar to those encountered in Direct Conversion receivers (DCR) discussed earlier. Since the correlation output is the result of multiplying two nearly identical signals, it consists mainly of DC and low frequency components. Therefore any DC offset caused through leakage or self mixing can significantly distort the desired baseband signal and impair the receiver performance. This phenomenon is exacerbated by the fact that most of the blocks in the receiver chain are directly coupled (DC) and hence device mismatches through differential signal paths can also cause offset errors that are liable to saturate the subsequent gain stages.

In order to mitigate these inherent problems of the coherent architecture, several additional synchronization, channel estimation and offset cancellation blocks need to be added to ensure robust performance and in doing so, the receiver complexity and power consumption are greatly increased.

3.2.1.2 Non-Coherent receivers

Non-coherent DS-UWB receivers perform demodulation of the incoming pulse train without the requirement of generating a template pulse in the receiver [6], [8]. This can be achieved in many ways. In a common technique employed by Transmitted Reference (TR) receivers (Fig. 3.6), every modulated data pulse that is transmitted is accompanied by an unmodulated reference pulse separated by a fixed period, τ. Since the reference pulse is generated similarly to the data pulse and passes through the same channel, it encounters similar temporal and spectral distortion. The receiver utilizes delay cells to delay the reference pulse by τ again to resynchronize the two transmitted pulses and uses the reference to demodulate the data pulse accurately.

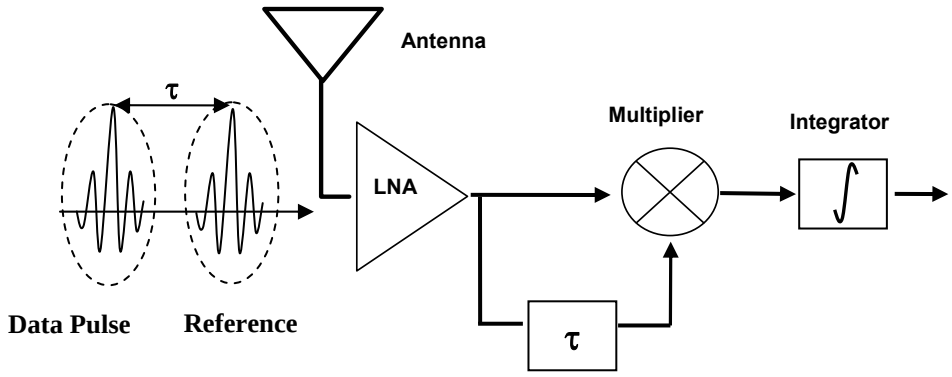


Fig. 3.6 Non-coherent Transmitted Reference UWB receiver architecture

A more straightforward method of achieving non-coherent detection is that used in the Auto-correlation receiver as shown in Fig 3.6. In this architecture the received impulse train itself is utilized as the reference template for down-conversion. The received weak pulse sequence is amplified by the LNA and subsequently fed to the two input ports of a multiplier concurrently, resulting in a self-modulated squared operation (Fig. 2.14d). This squaring operation de-spreads the pulse and thus has a high processing gain. The squared output is then amplified the desired baseband envelope is extracted through low-pass filtering. The extracted envelope is then passed through a threshold comparator to recover the desired baseband data.

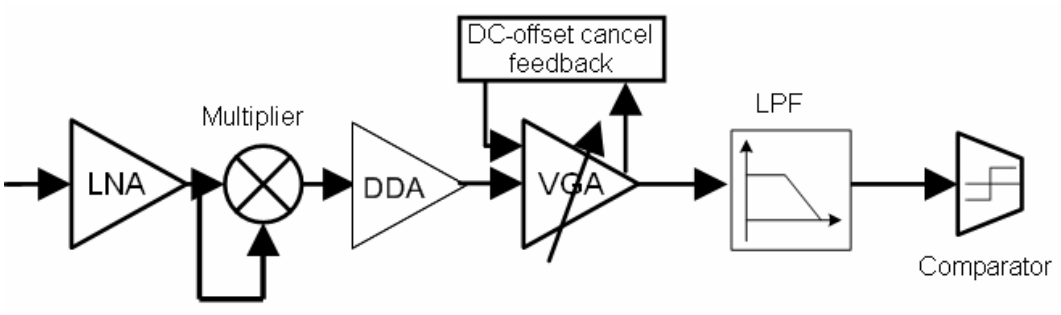


Fig. 3.7 Non-coherent Auto-correlation UWB receiver architecture

Even though non-coherent receivers are much simpler to build than their coherent counterparts since template pulse generation and complex synchronization circuits are not required, they do have other drawbacks that affect the receiver performance.

Firstly, since the received pulses are very weak and the LNA can provide only a limited amount of gain (less than 40 dB in practice) with an acceptable noise figure, the self-correlation output is significantly smaller as compared to the case when a strong locally generated template is used. Moreover, the output of the squaring operation ($y = kx^2$) in

the multiplier decays rapidly if the magnitude of the impulse train falls below a certain threshold. As a result, the sensitivity of the non-coherent receiver is significantly worse than that of a coherent UWB receiver described in the previous section.

Another major concern is phase mismatch between the inputs of the multiplier. Since the output of the LNA is split into two separate signal paths, it is crucial to ensure that both these paths generate the same phase delay because even small errors in synchronization will cause a significant deterioration in SNR of the demodulated signal. In addition, non-coherent receivers are very susceptible to produce erroneous detections in the presence of in-band interference signals because the self-correlation operation folds any received signal down to baseband.

Chapter 4

Proposed system architecture

From the discussion in the previous chapter on popular UWB receiver architectures that have been employed to date, it is clear that there is still room for improvement. As we have seen, the coherent structures are excessively complex due to the stringent synchronization and channel estimation requirements whereas non-coherent structures, although much simpler, lose out in terms of the overall receiver sensitivity. Moreover, both structures have relatively poor in-band interference rejection capabilities and hence negate one of the key advantages of UWB technology: the ability to co-exist with other narrowband communication standards. In order to avoid these problems, direct conversion receiver architectures for UWB receivers have also been looked into [6], [10].

In [12] and [14], the use of a simple sine wave template instead of the exact UWB pulse replica for demodulation is discussed. Even though the resultant architectures are simpler because a voltage controlled oscillator (VCO) is used to generate the template, they still require a high degree of synchronization for proper operation and hence additional blocks like a phase-locked loop (PLL) and clock recovery circuits are needed.

In this thesis, a novel UWB receiver system is proposed that circumvents the tradeoff between complexity and sensitivity that afflicts traditional architectures and at the same time also displays significantly better interference rejection capabilities. This chapter starts with a description of the modulation scheme utilized. This will be followed by a brief description of the proposed receiver architecture and the various building blocks.

Finally, the overall system level operation is modeled mathematically in order to describe the working principle of the entire system more fully.

4.1 UWB Impulse based Dual-band FSK modulation

The traditional application of FSK modulation in narrowband systems was described in Chapter 3. In this project, a new form of modulation for I-UWB transmission based on wide-band impulse transmission is utilized.

In the traditional 2-FSK case, discrete data bits are assigned to fixed single tone carriers, but in the proposed modulation scheme the '1's and '0's are assigned fixed sub-bands of the lower UWB communications bandwidth (3.1-4.8 GHz). These sub-bands are 3.2-3.8 GHz for data bit '0' and 4.0-4.6 GHz for data bit '1' and are denoted as Band1 and Band2 in the subsequent analysis. In order to meet FCC mask requirements with conventional modulation schemes like OOK [15], PPM [16] etc., very narrow and high-swing Gaussian pulses requiring power hungry hardware for detection and synchronization are required [17] in order to cover the 3.1-4.8 GHz UWB bandwidth. Each FSK modulated pulse however only occupies a much smaller 600 MHz sub-band which greatly relaxes the constraints on pulse width and allows longer, low-swing pulses to be employed while still retaining good overall mask occupancy. Moreover, this modulation scheme retains the advantages of the robustness to multipath fading and low transmission power levels which are characteristic of UWB impulse radios.

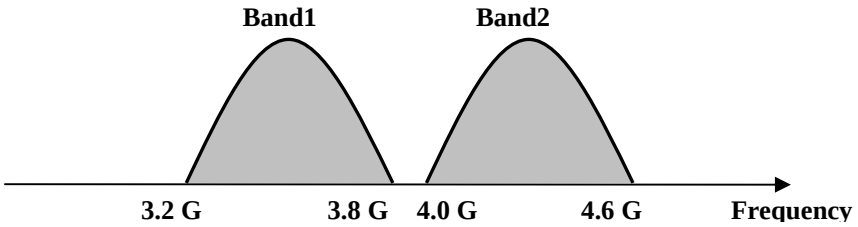


Fig. 4.1 Wideband FSK Modulation sub-band allocation

4.2 Proposed Receiver Architecture

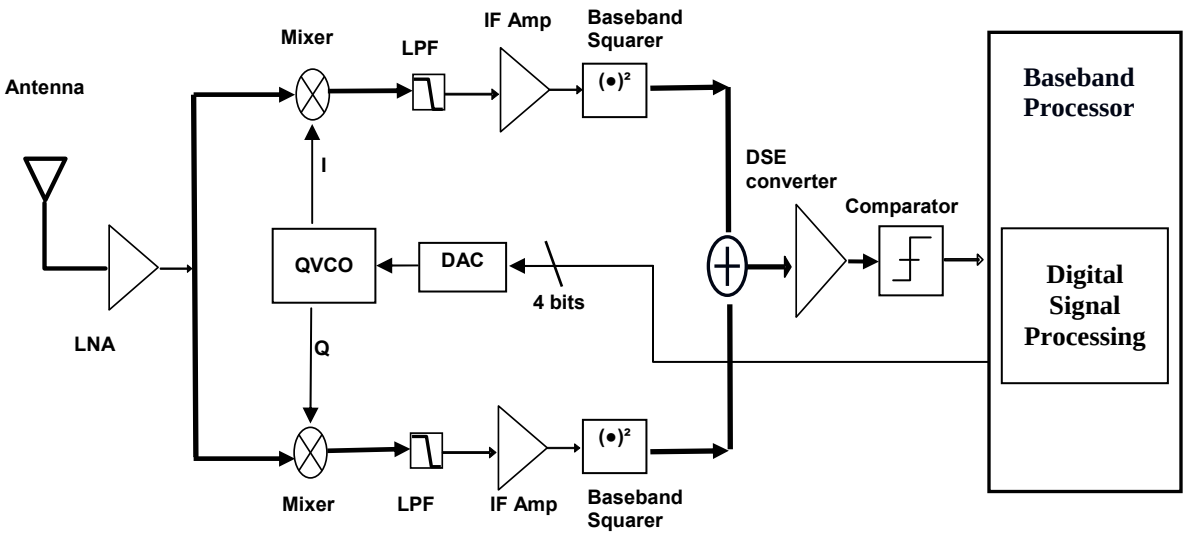


Fig. 4.2 Proposed receiver architecture for UWB dual-band FSK

Fig. 4.2 shows the overall schematic of the proposed receiver architecture to effectively recover the data sent using the dual-band UWB FSK modulation scheme described in the previous section. The receiver front-end consists of a low noise amplifier (LNA), a quadrature voltage controlled oscillator (QVCO), a 4-bit digital to analog converter (DAC), 2 mixers and 2 variable bandwidth low-pass filters (LPF). The back-end consists of 2 intermediate frequency amplifiers (IFA), 2 squarers, a differential to single ended (DSE) converter and a comparator.

The received pulse train is a random sequence of UWB impulses, each of which occupies either Band1 or Band2 depending on the digital data being transmitted. The weak received impulse train is amplified by the LNA and then down-converted by the mixers using the quadrature phased I and Q sinusoidal tones (0° and 90°) produced by the

QVCO. The 4 bit DAC is used to generate the control voltage for the QVCO which in turn controls the frequency of the generated sinusoidal template signal (LO). Depending on which sub-band the LO frequency lies in, either Band1 or Band2 data will be down-converted to baseband. In order to ensure proper operation, the QVCO must have a large enough tuning range to span the total operational bandwidth (3.2-4.6 GHz) and concurrently the DAC must be designed to be able to produce the control voltages required so that the QVCO frequency can be toggled over its entire tuning range. The LPF is used to filter out the out-of-band components and any narrowband interferers leaving only the baseband information of the desired sub-band. The bandwidth of the LPF is designed to be variable (between 50-300 MHz) and can be dynamically changed to maximize the amount of signal capture while maintaining the required external and inter-symbol interference rejection performance. The filtered I and Q signals are amplified by the IFAs and then squared causing further dispreading of the signal. The I and Q branch signals are subsequently added and this combined signal is then converted to a single ended signal by the DSE converter and subsequently a comparator is used to generate an NRZ data train representing the demodulation output. Since the output of the comparator still has a very low duty cycle, some basic baseband processing needs to be applied to it to match it to the data bit rate.

The FSK modulation scheme allows the system to benefit from added frequency diversity. Since ‘1’ and ‘0’ bits are modulated to separate wideband frequency channels, the system in effect transmits complimentary data the 2 channels, either of which could be used to demodulate the transmitted data. The frequent impairments suffered by the UWB channel, especially in indoor environments due to in-band interference from a

neighboring communication device can be assumed to be narrowband in nature and hence confined to one of the 2 sub-bands. In such cases, the data in the affected sub-band is corrupted by the interfering signal and causes demodulation errors. The signal processing unit in the off-chip baseband processor responds to the erroneous detections by altering the DAC control signals so as to shift the LO frequency to demodulate the data in the unaffected sub-band. This enables robust demodulation to be maintained even in the presence of strong interference.

The worst case interference scenario for this implementation is when the interference falls in the region at the mean of the center frequencies of the 2 sub-bands, i.e. around 3.9 GHz. In this case, both channels are equally affected and sufficient interference signal may fall within the receiver passband to compromise demodulation. Here, we have two options: a) to reduce the LPF bandwidth until the interference is sufficiently suppressed. and b) to shift the LO frequencies away from the respective sub-band center frequencies until the interference has been pushed out of the receiver passband. The wideband spectral occupation of UWB pulses results in the transmitted energy being spread quite evenly across the transmission band. Hence, shifting the LO frequency away from the center frequency does not significantly reduce the received pulse energy. However, since the LPF has been designed to have a sharp 5th order roll-off, the interference is greatly attenuated. For optimal compromise between signal energy collection (and hence sensitivity) and interference rejection, the LO frequency must be shifted in small steps. Hence, a DAC with a resolution of 4 bits is used to supply the control voltage to the QVCO to achieve an equivalent least significant bit (LSB) LO step size of around 60 MHz.

4.3 Mathematical model for proposed receiver system

In order to fully understand the theoretical aspects of the functionality of the proposed modulation scheme and receiver architecture, we need to derive a mathematical model for the entire system. In order to do so, we first need to define the characteristics of the UWB pulse that will be used for modulation. In this thesis, we utilize a traditional monocycle Gaussian pulse, which is the second order derivative of Gaussian function as shown in Fig.4.3.

The Gaussian monocycle pulse (GMP) signal can be expressed mathematically as [3]:

$$p(t) = A\left[1 - 4\pi(\frac{t}{T_d})^2\right]e^{-2\pi(\frac{t}{T_d})^2} \tag{4.1}$$

where T_d is half of the pulse width and A is the amplitude scaling factor.

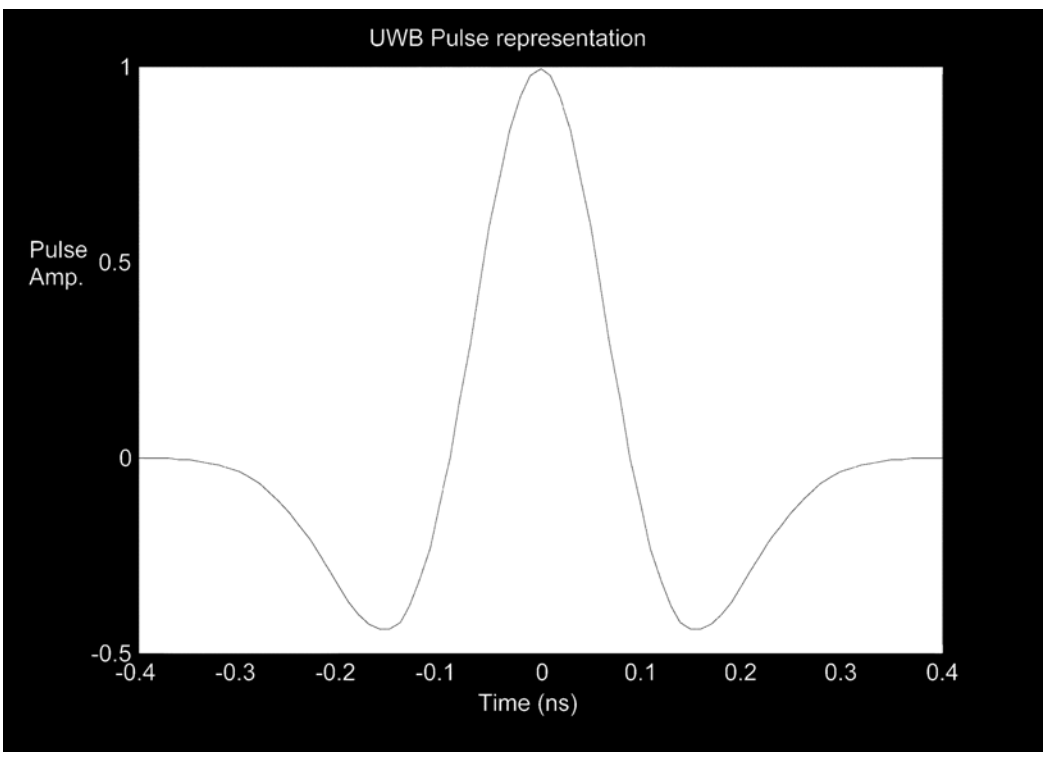
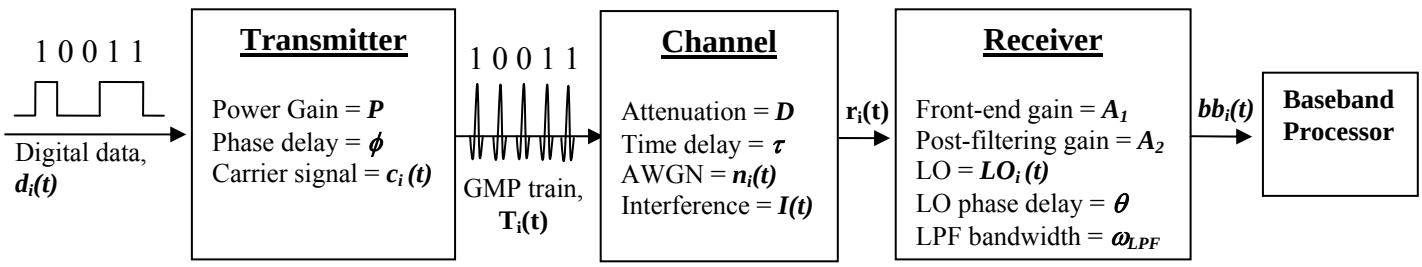


Fig. 4.3 Gaussian monocycle pulse in time domain



` **Fig. 4.4 Analytical UWB dual FSK system model**

The entire I-UWB system is modeled as shown in Fig. 4.4

We define the carrier signal as

$$c_i(t) = C\cos\omega_i t\ ,\ i=1, 2 \tag{4.2}$$

where C is the carrier amplitude and i=1 when $d_i(t)$ = 0 and i=2 when $d_i(t)$ = 1 representing Band1 and Band2 modulation respectively. Therefore the transmitted modulated data is,

$$T_i(t) = Pp(t)\ c_i(t+\phi) \tag{4.3}$$

$$= PCp(t)\cos(\omega_i t + \phi) \tag{4.4}$$

where $p(t)$ is the GMP train of Eq. (4.1). The received pulse at the receiver input can be written as,

$$r_i(t) = D\ T_i(t-\tau) + n_i(t) + I(t) \tag{4.5}$$

$$= D\ PC\ p(t-\tau)\cos(\omega_i t + \phi - \varepsilon) + n_i(t) + I\cos\omega_{int}t \tag{4.6}$$

$$= Kp(t-\tau)\cos(\omega_i t + \phi') + n_i(t) + I\cos\omega_{int}t \tag{4.7}$$

where $\varepsilon = \dfrac{\tau}{\omega_i}$, $\phi' = \phi - \varepsilon$ and $K = D\ PC$

Let the 2 discrete QVCO output tones corresponding to each band be

$$LO_i(t) = L\cos(\omega_n t + \theta), \tag{4.8}$$

where n=1,2 and $\omega_1 \in Band1$ and $\omega_2 \in Band2$

After mixing, the down-converted pulse train can be represented as,

$$v_I(t) = r_i(t) LO_i(t) \tag{4.9}$$

$$= L\ r_i(t)\cos(\omega_n t + \theta) \tag{4.10}$$

$$\begin{aligned} &= \frac{LK}{2} p(t-\tau)(\cos[(\omega_i + \omega_n)t + \theta + \phi'] + (\cos[(\omega_i - \omega_n)t + \theta - \phi']) \\ &\quad + IL[\cos(\omega_{\text{int}} + \omega_n)t + \cos(\omega_{\text{int}} - \omega_n)t] \end{aligned} \tag{4.11}$$

And similarly,

$$v_Q(t) = L\ r_i(t)\cos(\omega_n t + \theta + 90^0) \tag{4.12}$$

$$= L\ r_i(t)\sin(\omega_n t + \theta) \tag{4.13}$$

$$\begin{aligned} &= \frac{LK}{2} p(t-\tau)(\sin[(\omega_i + \omega_n)t + \theta + \phi'] - (\sin[(\omega_i - \omega_n)t + \theta - \phi']) \\ &\quad + IL[\sin(\omega_{\text{int}} + \omega_n)t - \sin(\omega_{\text{int}} - \omega_n)t] \end{aligned} \tag{4.14}$$

The filter bandwidth, ω_{LPF} is tuned such that,

$$\omega_{i+}\omega_n \pm 0.3\text{GHz} > \omega_{LPF} \quad \& \quad \omega_i - \omega_n \pm 0.3\text{GHz} < \omega_{LPF} \tag{4.15}$$

$$|\omega_{int} - \omega_n| > \omega_{LPF} \tag{4.16}$$

where the bandwidth of $p(t)$ is assumed to be 0.6 GHZ for Eq. (4.15). Assuming for simplicity that the LO frequency is matched to the carrier exactly so that $\omega_i = \omega_n$ for $[i,n]$=[1,1] or [2,2], then after low pass filtering, the I and Q signals become,

When $[i,n]$=[1,1] or [2,2],

$$f_I(t) = \frac{LK}{2} p(t-\tau)\cos(\theta - \phi') \tag{4.17}$$

$$f_Q(t) = -\frac{LK}{2} p(t-\tau)\sin(\theta - \phi') \tag{4.18}$$

And when [*i,n*]=[1,2] or [2,1],

$$f_I(t) = f_Q(t) = 0 \tag{4.19}$$

After Squaring and adding the I and Q branch signals, we have,

When *n*=1 and *i*=1 OR *n*=2 and *i*=2,

$$s_i(t) = [A_2 f_I(t)^2 + A_2 f_Q(t)^2] \tag{4.20}$$

$$= \left[\frac{A_2 LK}{2}\right]^2 [p(t-\tau)]^2 \tag{4.21}$$

After the demodulated signal undergoes a comparison operation with a pre-determined threshold voltage level VT_{comp}, the following output to the baseband processor is as follows

$$bb_i(t) = \begin{cases} 1.8V, & if\, b_i(t) > VT_{comp} \\ 0V, & otherwise \end{cases} \tag{4.22}$$

We can see from the preceding analysis that the phase mismatch between the LO template and the received pulse train does not affect the overall demodulation performance of the receiver and hence no synchronization is required between transmitter and receiver. We further see that by tuning ω_{LPF} to meet the conditions stated in Eq. (4.15), (4.16), robust demodulation can be achieved even in the presence of strong in-band interferers.

Chapter 5

Receiver Building Blocks design

No matter how theoretically sound a receiver structure is, its overall performance is still largely dependant on the merits of the design of its constituent circuit blocks. In this chapter, the designs of all the required blocks needed for overall integration are discussed. Particular attention is given to the design of the LNA, mixer, DAC, squarer, comparator and other baseband blocks. The remaining building blocks necessary for the receiver, the conventional 3-stage LNA, QVCO and LPF were designed by other group members and are briefly reviewed for better understanding of the entire system.

In this thesis, all circuit and integration level simulations are performed in the Agilent Advanced Design System (ADS) environment and are based on the 0.18μm CMOS technology device models provided by the Chartered Semiconductor Manufacturing (CSM). All packaging and bonding models and are included in simulation and are based on the in-house facilities provided at the Institute of Microelectronics, Singapore (IME).

5.1 Low Noise Amplifier

The low noise amplifier (LNA) is the first RF block in any wireless receiver. It serves to increase the signal to noise ratio (SNR) and to suppress noise. This can be understood better by studying the famous Friis formula which is used to calculate the total Noise Factor, F_{total} of a cascaded system as

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots \qquad (5.1)$$

where $F_{1,2,..}$ and $G_{1,2..}$ represent the noise factor and gain of stage *1,2..* respectively.From Eq. (5.1), we can see that as the first stage, the noise figure of the LNA is the most dominant term in the overall receiver NF. Moreover, high LNA gain is essential to mitigate the effect of other noisy stages of the system. Hence, the LNA performance plays a major role in determining the overall system's minimum detectable signal level.

Other considerations in LNA design are good linearity so as to achieve large signal accommodation without distortion, and impedance matching to the input source (usually an antenna) over the desired frequency range. This chapter starts with a review of conventional wideband LNA designs. In the second section, a novel low power UWB LNA structure utilizing area efficient active inductors is proposed and its merits are compared to other recent works. Finally, the structure of a more conventional 3 stage current reuse LNA that is utilized for implementation in the receiver architecture discussed in the previous sections is shown.

5.1.1 Commonly used wideband LNA topologies

The starting point for any LNA design is the choosing of the correct architecture for the specific application. In wide band designs, one of the most important considerations is to obtain wideband impedance matching without degrading the Noise Figure (NF). Several LNA topologies have been discussed in the past to achieve this and Fig 5.1 shows some of the most common ones.

Fig. 5.1(a) shows a simple 50Ω resistive termination approach for input matching. However, despite its simplicity, this approach is seldom used because of the unacceptably high NF caused by the fact that the resistor thermal noise is added straight to the input terminal and also because the resistive termination causes signal attenuation.

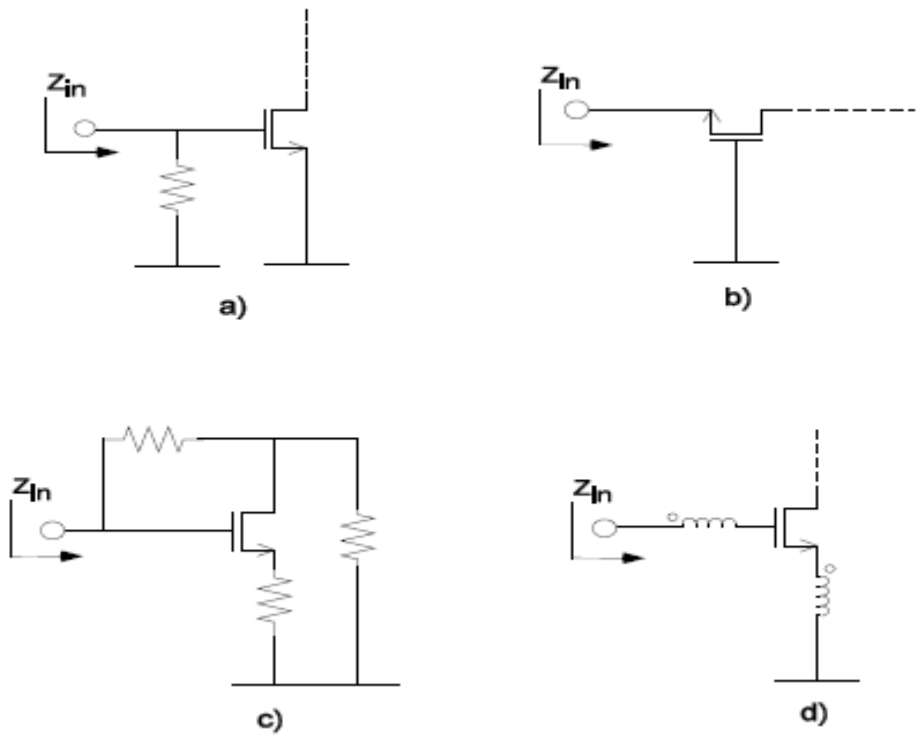


Fig. 5.1 Common LNA topologies (a) Resistive termination (b) Common gate (c) Shunt-series Feedback. (d) Common source with inductive degeneration

Fig. 5.1(b) shows a Common Gate (CG) LNA topology. The input impedance is

$$Z_{in,CG} = \frac{r_o}{1+(g_m+g_{mb})r_o} \approx \frac{1}{(g_m+g_{mb})} \tag{5.2}$$

where r_o is the output resistance of transistor. The noise factor can be written as

$$F \geq 1+\frac{\gamma}{\alpha}\frac{1}{g_m R_s} \tag{5.3}$$

where R_s is the input source resistance, γ is a constant determined by technology and has value of 2/3 for long channel devices in saturation (γ is larger and takes a value between 2 and 3 in short channel devices), and $\alpha = g_m / g_{d0}$ [19].

This topology does not suffer from the Miller effect and from Eq. (5.1) it is obvious that Z_{in} is independent of the effect of parasitics associated with the MOSFET. The

desired source impedance can be easily matched over a wide bandwidth by changing the g_m of the transistor alone and hence complex input matching networks are not required. Moreover, the input matching circuit has a quite low Q factor which results in stability against variation of passive components. However, in order to achieve 50Ω input matching in this topology, g_m must have a value of about 20mS which is rather high and requires a large biasing current to drive the transistor which inevitably results in an increase in the total power consumption. Assuming perfect input matching, the minimum noise factor of common gate LNA is obtained as $F \geq 1 + \frac{\gamma}{\alpha} \approx 3dB$ (for $\alpha = 0.85$).

For the shunt feedback amplifier shown in Fig. 5.1(c), the input resistance is

$$Z_{in,SFB} = \frac{R_F + R_L \parallel r_o}{1 + g_m (R_L \parallel r_o)} \tag{5.4}$$

and the associated 3-dB bandwidth of the stage is

$$\omega_{-3dB} = \frac{(1 + A_v)}{R_F (C_{gs} + (1 + A_v) C_{gd})} \tag{5.5}$$

From Eq. (5.4), we can see that this topology can achieve similar broadband matching performance to the CG topology but without having to resort to prohibitively large bias currents by using smaller values of R_F which leads to an increase in overall bandwidth (Eq. (5.5)). But this comes at the cost of increased NF [20]. Moreover, the shunt-resistor in this topology causes the input common mode voltage to be fixed with the output voltage and hence the input transistor cannot be optimally biased for gain performance.

In the common source topology with source degeneration shown in Fig. 5.1(d), the 50Ω input resistance is obtained by adding a series inductor L_s to the source terminal of the input transistor to resonate out the gate capacitance of the transistor leaving only a

resistive component. In Figure 5.2, the small signal model of CS amplifier with degeneration inductor is shown. The input resistance of common source LNA is expressed as

$$Z_{in,CS} = s(L_s + L_g) + \frac{1}{sC_{gs}} + (\frac{g_m}{C_{gs}})L_s \approx s(L_s + L_g) + \frac{1}{sC_{gs}} + \omega_T L_s \tag{5.6}$$

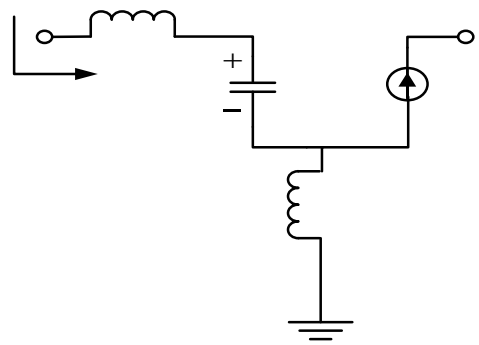


Fig. 5.2 Small signal model of a source degeneration amplifier

At resonant frequency,

$$s(L_s + L_g) + \frac{1}{sC_{gs}} = 0 \tag{5.7}$$

$$Z_{in,CS} = (\frac{g_m}{C_{gs}})L_s = \omega_T L_s = 50\Omega \tag{5.8}$$

The effective transconductance of this topology is:

$$G_m = g_m Q = \frac{g_m}{\omega_0 C_{gs}(R_s + \omega_T L_s)} = \frac{\omega_T}{\omega_0 R_s (1 + \frac{\omega_T L_s}{R_s})} \tag{5.9}$$

where ω_0 is the operation frequency, C_{gs}, ω_T and g_m are the gate source capacitor, the transition frequency and the transconductance of input transistor, respectively.

The most attractive feature of this topology is that by adding L_s, good input matching is obtained without NF deterioration because an inductor is inherently a noiseless passive device. Equation 5.9 also indicates that the effective transconductance is enhanced Q

times by the pure RLC input matching network at the resonant frequency. Thus, to achieve a desired gain, this topology requires a smaller biasing current.

5.1.2 UWB LNA utilizing Active Inductor

One of the major drawbacks of wideband LNA designs is their heavy reliance on large passive inductors to achieve performance requirements like impedance matching, stability and bandwidth extension. These requirements are even harder to satisfy at the higher frequencies of operation that are required in UWB communication, which in turn causes a further increase in the number of inductors required and adversely affects chip sizes. Active inductors (AI) have been advocated for a long time as area efficient replacements for passive inductors. Several AI topologies have been presented [21], [22], [23], most of which utilize a capacitor-gyrator (C-G) structure to duplicate the required inductive properties. These designs are not only much smaller but also provide much larger quality factors (almost 8000 [21]) than passive inductors. However, most presented active inductors have very narrow-band operation ranges. Moreover, they typically require prohibitively large currents to achieve high center frequencies and moderate inductance values

In this thesis, a novel LNA utilizing AI is presented which is capable of low voltage (1V) low-power UWB applications while achieving large chip area reduction. The following section deals with the design methodology for the AI as well as the overall LNA.

5.1.2.1 Active Inductor design

The active inductor structure utilized for this work, shown in Fig. 5.3(a) has a C-G based grounded cascode topology and incorporates a modified implementation of the

feedback loss-regulation technique presented in [21]. The loss compensation is achieved through transistor M3 which creates a series negative resistance that compensates for the losses due to the other active devices in the AI. We denote the gate-source capacitance, transconductance and drain-source conductance of transistor M_X as C_{gsx}, gm_x and g_{dsx} respectively. S(ω) represents the frequency dependent admittance of C_{gs3} incorporated with the loss compensation R-C network at the gate of transistor M3. Using first order small signal analysis, the relevant AI parameters shown in Fig. 5.3(b) can be extracted:

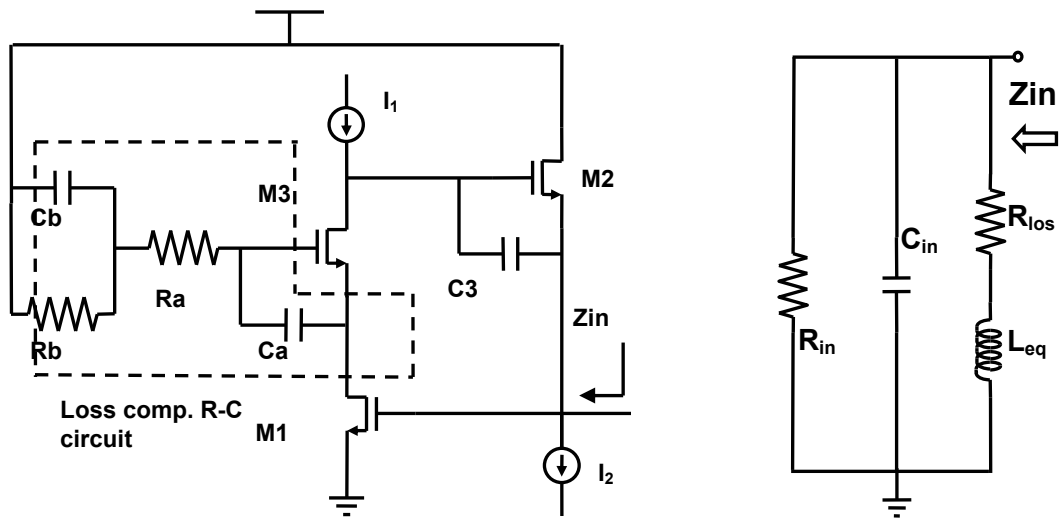


Fig. 5.3 (a) Active inductor structure; (b) Small signal equivalent

$$L_{eq} = \frac{g_{m2}g_{m3}(C_3 + C_{gs2}) + \omega^2 C_{gs2}{}^2 S(\omega)}{g_{m1}g_{m2}{}^2 g_{m3} + \omega^2 g_{m1}g_{m3}C_{gs2}{}^2} \cong \frac{(C_3 + C_{gs2})}{g_{m1}g_{m2}} \tag{5.10}$$

$$R_{loss} = \frac{g_{m2}g_{ds1}g_{ds3} + \omega^2[g_{m3}C_{gs2}{}^2 - g_{m2}C_{gs2}S(\omega)]}{g_{m1}g_{m2}{}^2 g_{m3} + \omega^2 g_{m1}g_{m3}C_{gs2}{}^2} \tag{5.11}$$

$$R_{in} = \frac{1}{g_{ds3}} \text{ and } C_{in} = C_{gs1}$$

Self-resonant frequency, $\omega_0 = \sqrt{\dfrac{g_{m1}g_{m2}}{C_{gs1}(C_3 + C_{gs2})}}$ (5.12)

At self-resonant frequency ω_0, the quality factor can be written as

$$QF = \frac{\omega_0 L_{eq}}{R_{loss}} \cong \sqrt{\frac{g_{m1} g_{m2} g_{m3}^{\ 2} (C_3 + C_{gs2})}{C_{gs1} g_{ds1}^{\ 2} g_{ds3}^{\ 2}}} \tag{5.13}$$

Fig. 2 shows the typical performance of the presented AI at UWB frequencies. From (5.11) we see that the RC network makes the series negative resistance created due to M3, and hence the R_{loss}, frequency dependent. By tuning the RC network, we can shape the total resistive loss of the AI and consequently control the value and peaking frequency of its QF independently of the ω_0 and L_{eq} as shown in Fig. 2.

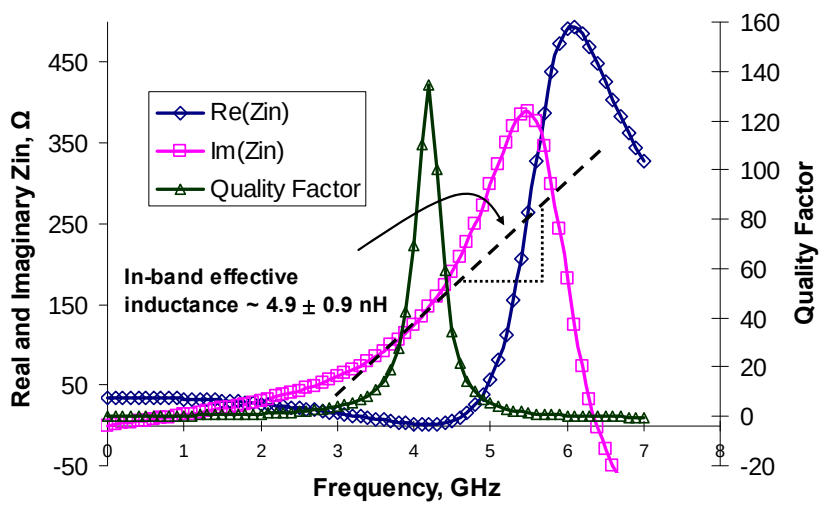


Fig. 5.4 High frequency performance of the active inductor

From Eq. (5.10), (5.12) and (5.13), we see that there also exists a strong inter-dependence between the L_{eq}, ω_0 and QF based primarily on the values of the transconductances and gate capacitances of M1 and M2. For high frequency gain peaking in the LNA, the active inductor needs to be designed for a moderately high inductance (4nH-6nH) with a moderately low QF (15-20) for gain flatness. This is achieved by first increasing the bias current I_1 to raise g_{m1}, and as a result raise the ω_0 to the desired value.

The corresponding undesired rise in the QF can then be lowered by tuning the R-C loss compensation circuit to reduce the negative series resistance. Finally, by selecting a suitable *C3* to increase the total gate to source capacitance of M2, the relatively large L_{eq} that is desired can be achieved without increasing M2 sizing or the current drawn from I_2.

5.1.2.2 LNA design

Fig. 3 shows the overall LNA schematic. It consists of two inductively peaked common source stages followed by a common-drain source-follower output stage. Both peaking inductors are implemented as active inductors. One big advantage of this structure is that it allows the reuse of the large drain currents of the amplification transistors, M4 and M5 through one branch of each active inductor. This equivalently removes the need for current source I_2 in Fig. 1(a) and hence results in substantial power savings.

a) Input and Output matching

Due to overall noise performance considerations, a passive inductor, L_{g1} was used in the input matching network for the source degenerated first stage. From Eq. (5.6), we see that by choosing appropriate values of L_{g1} and L_{s1}, low NF and reasonable input matching can be concurrently achieved. According to these considerations, the calculated values of the source degeneration inductances for both stages, Ls_1 and Ls_2 are very small (0.25nH and 0.4nH) and hence are implemented using transmission lines. The source follower output stage is necessary to provide a 50Ω output match for testing purposes. The calculated output impedance is:

$$Zout = \frac{1}{(g_{m8} + \frac{1}{r_{o7}} + \frac{1}{r_{o8}})} \tag{5.14}$$

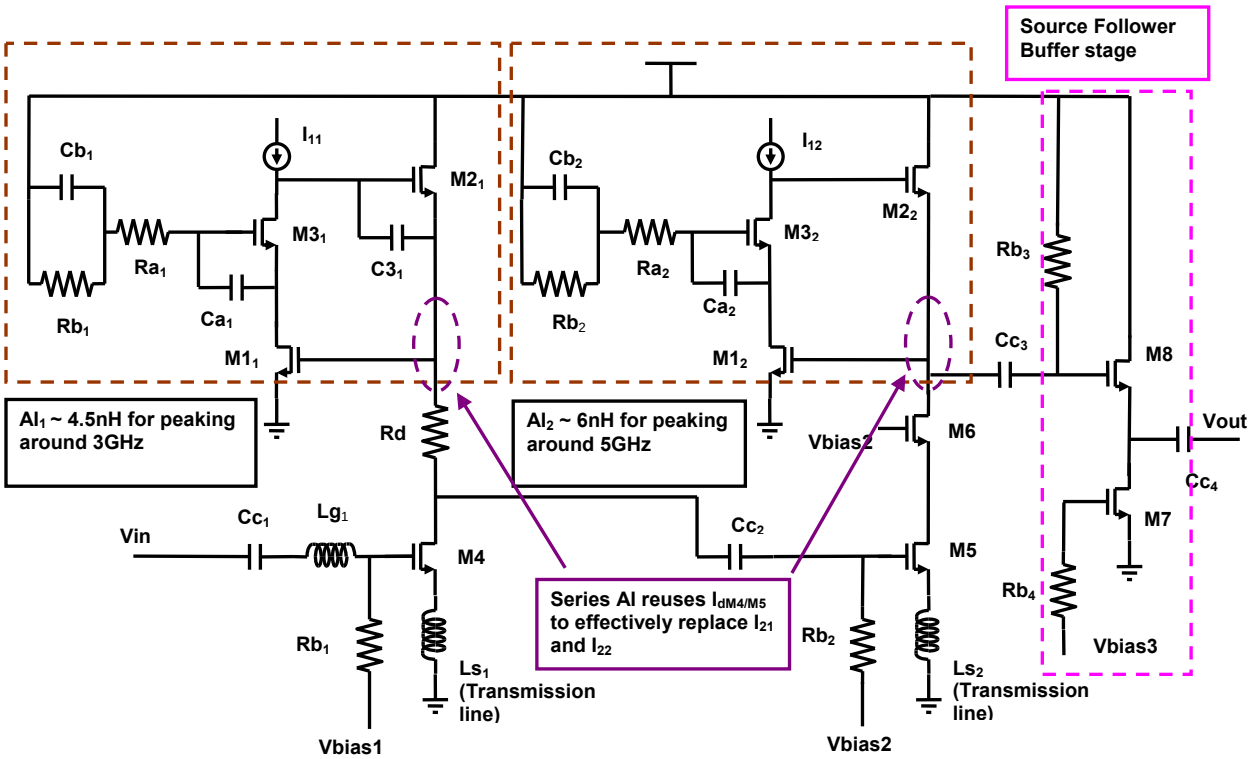


Fig. 5.5 Overall three stage LNA schematic

b) Gain

In order to utilize the higher QF that can be achieved by the active inductor without compromising the overall gain flatness of the LNA, a cascaded LNA topology is chosen where the two stages are optimized with a peaked gain around the lower and upper corner frequencies of our target bandwidth. Due to the NF and linearity considerations which are discussed in more detail in the related reference [24], the ω_0 for the first and second stage, $\omega_{0,1}$ and $\omega_{0,2}$ are chosen to cause the stages to peak near the lower (3GHz) and upper (5GHz) corner frequencies respectively so that when cascaded, an overall wideband gain is achievable. The gain of the first stage can be calculated approximately as:

$$G_{CS} = \frac{g_{m4} R_{eff} \left(1 + s \frac{L_{d1}}{R_{eff}}\right)}{(s^2 L_{d1} C_{eff} + s R_{eff} C_{eff} + 1)(1 + g_{m4} s L_{s1})} \tag{5.15}$$

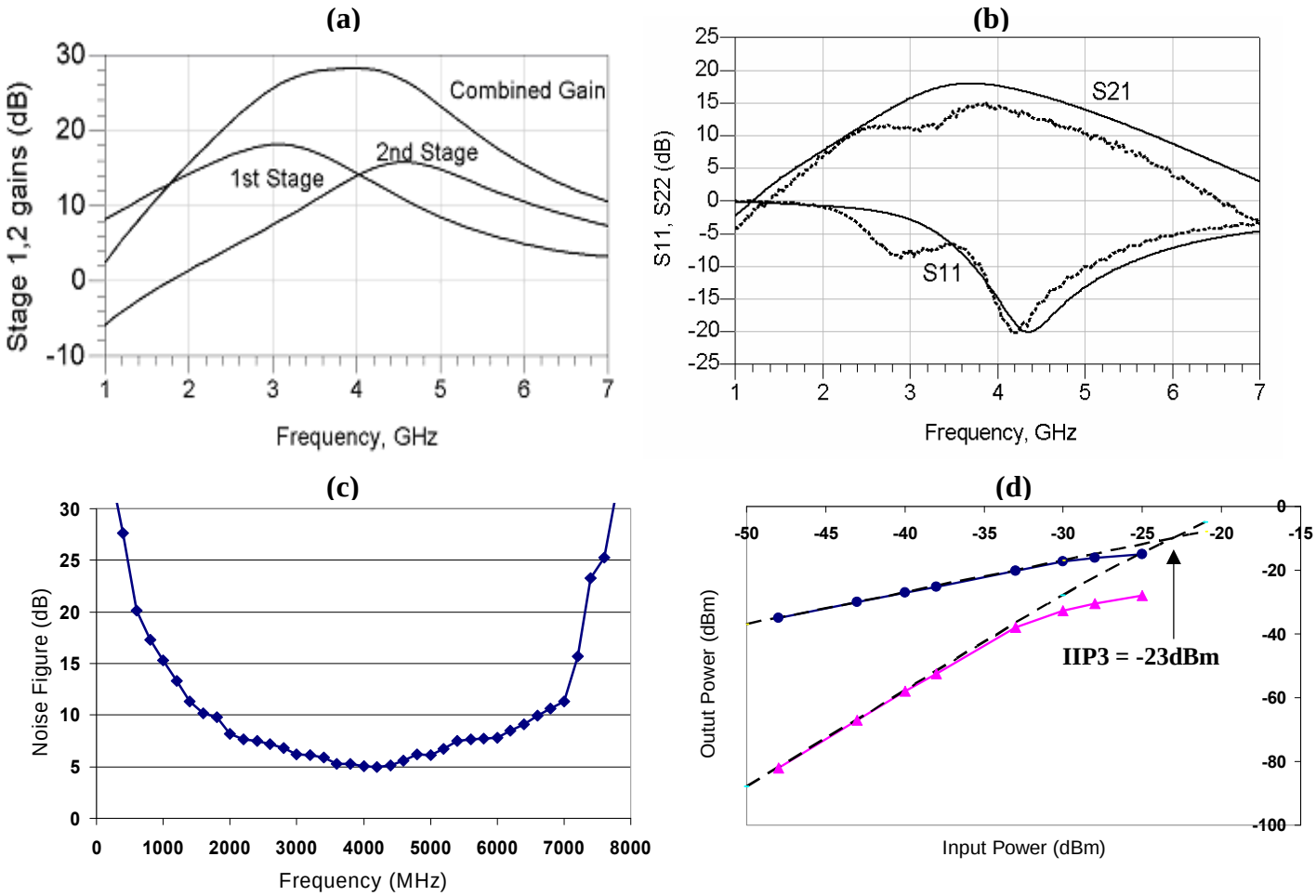


Fig. 5.5 (a) Individual and staggered stage gains (b) Measured (---) and simulated (—) S21 and S11 (c) Measured Noise Figure (d) Measured Linearity

where L_{d1} is the active inductance, $R_{eff} = R_D + R_{inAI}$ is the total drain resistance of M4 and C_{eff} is the total load capacitance being driven by the stage. The second stage has similar gain characteristics but it also utilizes a cascode transistor M6 to increase isolation and boost high frequency gain by reducing the Miller feedback capacitance. Fig. 5.5(a) shows the gain peaking of the two stages individually and their overall wide-band response in the cascaded topology. The gain of the source follower causes significant (7-8dB) signal attenuation but has been included to facilitate the testing of the device using low impedance measurement devices.

c) Measurement Results

The measured S-parameters are shown overlaid with the simulated results in Fig. 5(b). The measured power gain (S21) has a peak value of 15.1dB and -3dB passband from 3.25GHz to 4.8GHz while the measured input return loss (S11) is less than -7.2dB across the bandwidth. The bond wires to the LNA supply appear in series with the AI and hence add to the load inductances $L_{d1/2}$. In order to minimize this added loading, multiple pads are provided for the supply voltage so that several bond wires can be utilized in parallel in order to minimize the unwanted loading inductance. However, the additional pads add parasitic capacitive loading and together with the finite bond wire inductances cause the effective resonant frequencies of the two stages to be slightly lower than simulated which causes the high frequency gain to roll-off in measurement as seen in Fig. 5(b). The measured noise figure, shown in Fig. 5(c), is between 4.95dB and 6.1dB throughout the passband. A two tone test was used to measure the linearity of the LNA at 3.5, 4 and 4.5GHz and Fig. 5(d) shows the average linearity trend with a measured IIP3 of -23dB. The degradation in LNA linearity can be partially explained by the inevitable shrinking of headroom due to the reduced supply voltage of 1V. The die photo of the LNA with biasing circuits is shown in Appendix A. The LNA core occupies only 0.05mm^2 die area while drawing 7.1mA current from a 1V supply. Due to the current reuse technique used, the additional currents required for AI implementation, $I1_1$ & $I1_2$ are only 125μA & 200μA respectively which constitutes a very small increase in power consumption. A summary of the LNA performance in comparison with other published LNA structures using AI is shown in Table I.

Table I: Comparison of presented work with other published LNA designs with Active Inductors

Author(s)	Technology	Centre freq.	3-dB Bandwidth	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Area (mm^2)
Zhuo *et al.* [25] *	0.5µm CMOS	1 GHz	N/A***	20.5	3.65	-17	14	0.08 **
Sharaf [26] *	0.5µm CMOS	900 MHz	500 MHz	12.2	3.1	-21	17	N/A***
Pascht *et al.* [27] *	0.3µm CMOS	2.4 GHz	250 MHz	19.2	2.5	N/A***	40.8	0.6
Yang *et al.* [28]*	0.35µm CMOS	1.75 GHz	30 MHz	24	N/A***	N/A***	9.3	0.03
This work [24]	0.18µm CMOS	4 GHz	1.55 GHz	15.1	4.95 to 6.1	-23	7.1	0.05

* Simulation only, ** Estimated area, *** Not reported

5.1.3 3-stage current reuse UWB LNA

Even though the proposed active inductor based LNA is far superior to traditional LNA architectures in terms of chip area, it does suffer from poorer NF and linearity performance. The fact that the presented structure has been optimized for low voltage application (1V) is a further hindrance to eventual integration with a system with a 1.8V supply voltage. Since the Dual FSK quadrature receiver of this thesis is such a system and places a premium on high LNA gain without significant loss in NF and linearity performance, after careful consideration a more traditional LNA architecture using passive inductors was used for integration in the receiver chain at the cost of significantly larger chip area. It must be noted that although the active inductor based LNA is not optimally suited to perform as the first amplification stage in a sensitive receiver chain, it still has great potential as an area efficient second wideband gain stage in cascade with a more conventional first stage. In this way, its poor NF can be suppressed by the first stage gain while a higher supply voltage (1.8V) will inevitably improve linearity. This approach will be used in future versions of this receiver once the overall functionality has been confirmed.

Fig. 5.6 shows the schematic of the utilized LNA architecture. It implements a 3-stage

current reuse architecture with inductive peaking for bandwidth expansion. It employs a common gate input stage and hence does not require an input matching network. The output impedance is optimized to match the input impedance of the mixer loads rather than 50Ω. The last stage performs a single to differential operation on the amplified UWB pulse train. This LNA has a simulated voltage gain of 38 dB, NF of 4.2dB, OIP3 of 9dBm with better than -10dB input and output matching.

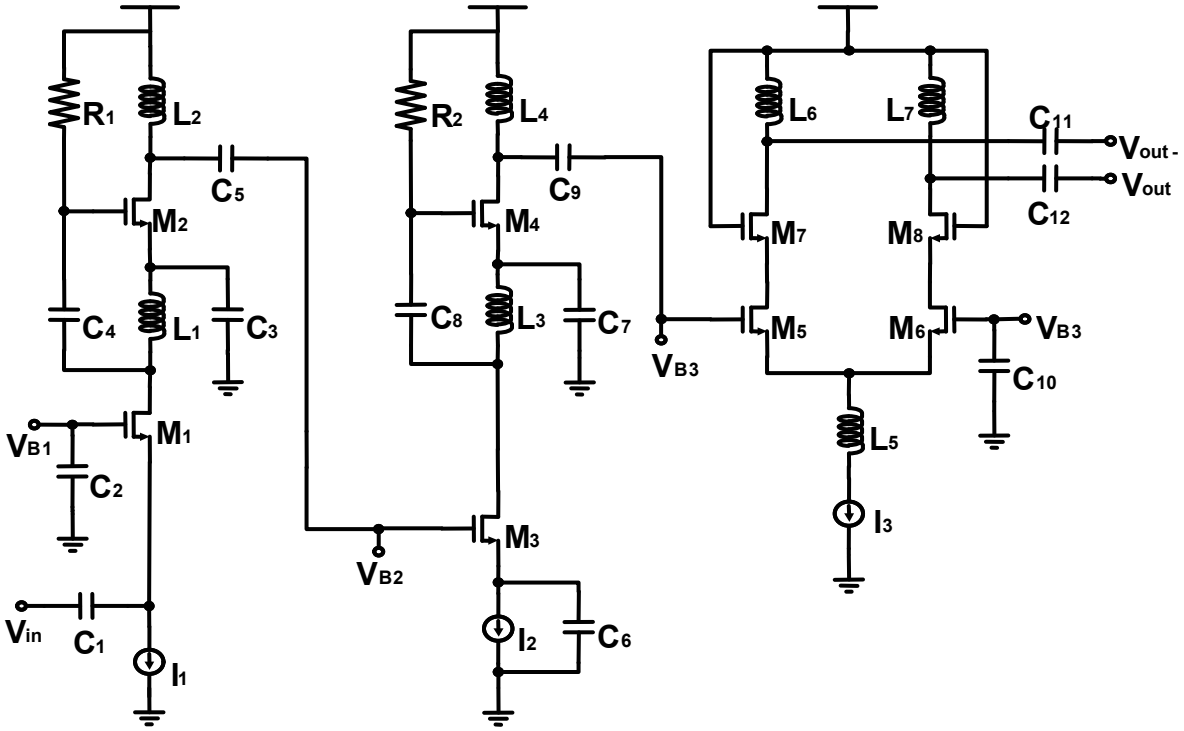


Fig. 5.6 3-stage current reuse UWB LNA

5.2 UWB Mixer

Mixers are some of the most commonly used RF components. They are non-linear devices used in systems to trans-late (multiply) one frequency to another. All mixer types work on the principle that a large Local Oscillator (LO) drive will cause switching so that the incoming RF signal is modulated to the Intermediate Frequency (IF). In this thesis, we will only be discussing the down-conversion mixer where a high frequency wide-band UWB pulse (RF) is down-converted by a large QVCO output signal (LO) to a pulse with the same bandwidth but centered on or near DC (IF). Some mixer parameters are briefly defined below for clearer understanding of the following discussions.

Conversion Gain - This is the ratio (in dB) between the IF signal and the RF signal.

Double sideband (DSB) mixing - This assumes that both signal and noise are present in the upper and lower sidebands of the carrier. Importantly, $NF_{DSB} = NF_{SSB} - 3$ dB

Linearity – Defined by the 1dB compression point of the IF with respect to RF power

Double balanced (DB) mixer – This refers to mixer architectures where the DC components of the RF and LO signals are totally cancelled.

There are various mixer topographies from simple single ended, single balanced mixers to more complicated double & triple balanced mixers that provide better isolation from the Local Oscillator (LO) and spurious. This chapter will start by examining two of the most popular mixer structures in use today, the Gate-source injection mixer and the Gilbert cell mixer. Next, a hybrid mixer structure is studied that combines the benefits of these two traditional architectures, which makes it ideally suited for application in the overall UWB receiver system.

5.2.1 Gate-source injection mixer

The gate-source injection (GSI) mixer is one of the simplest 4 quadrant mixer structures and is shown in Fig. 5.7(a). Fig. 5.7(b) shows the 4 quadrant cancellation scheme that is employed by this mixer.

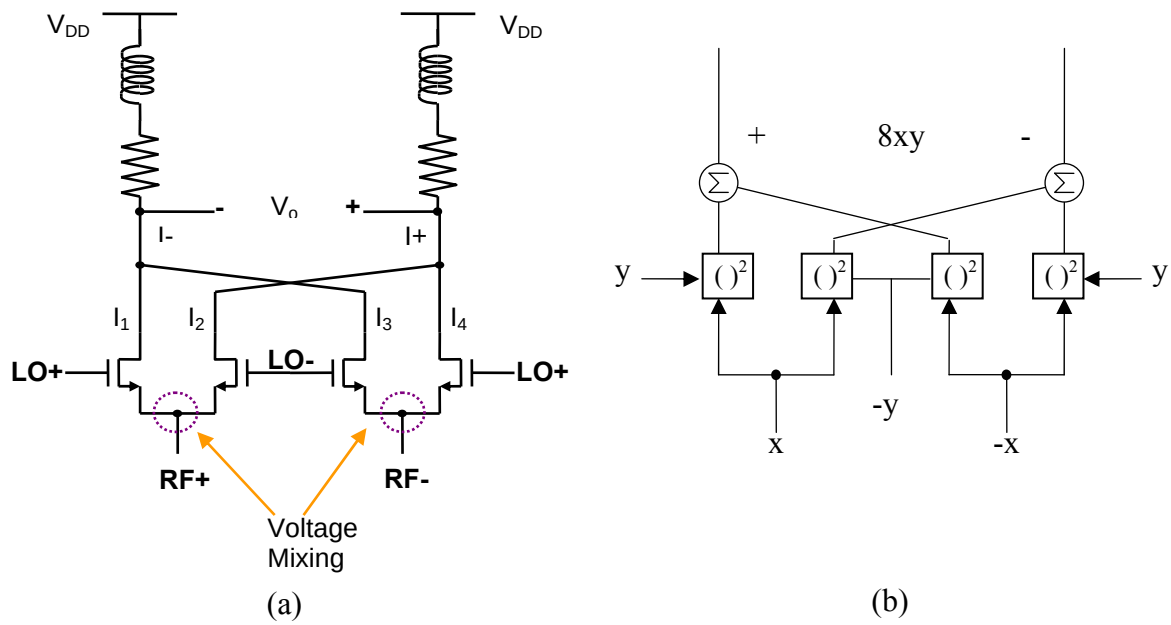


Fig. 5.7 (a) Gate source mixer architecture (b) Associated 4 quadrant cancellation scheme

Representing the RF and LO signals for convenience as $X \pm x$ and $Y \pm y$. and assuming that the square law device represented in the scheme of Fig. 5.7(b) is a MOSFET in saturation, then the following analysis holds

$$I_1 = \frac{1}{2} k_n \frac{W}{L} [C + (x - y)]^2 \tag{5.16}$$

$$I_2 = \frac{1}{2} k_n \frac{W}{L} [C + (-x - y)]^2 \tag{5.17}$$

$$I_1 = \frac{1}{2} k_n \frac{W}{L} [C + (-x + y)]^2 \tag{5.18}$$

$$I_1 = \frac{1}{2} k_n \frac{W}{L} [C + (x + y)]^2 \tag{5.19}$$

where $k_n = \mu_n C_{ox}$ and $C = X - Y - V_t$ and $\frac{W}{L}$ is the aspect ratio of $M_{1,2,3,4}$

$$I_{out} = (I_2 + I_4) - (I_1 + I_3) \tag{5.20}$$

$$I_{out} = 4k_n \frac{W}{L} xy \tag{5.21}$$

$$V_{out} = 4k_n \frac{W}{L} xy(R + j\omega L) \tag{5.22}$$

We see that by properly biasing the transistors to be in saturation, the square law properties of the MOSFET can be utilized to implement the cancellation scheme described above leaving only the desired mixed product (Eq. (5.22)).

5.2.2 Gilbert Cell mixer

The Gilbert cell mixer is by far the most common mixer architecture in use today. It was introduced in 1968 [29] and its popularity and longevity to this day is a testament to its superior design. Fig. 5.8 shows the basic DB Gilbert cell architecture. The structure is very similar to the GSI mixer described above and can be broken down into 3 main parts, RF transconductance stage (M1, M2), LO switch pairs (M3-M6) and the shunt peaking load (R-L series combination).

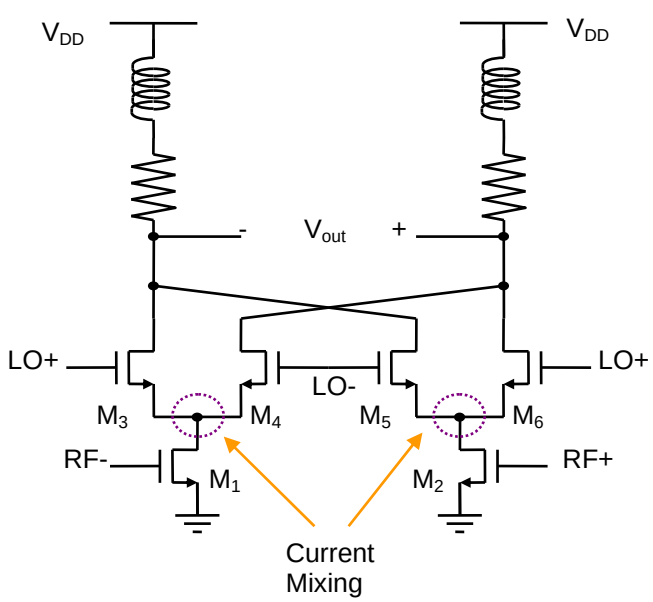


Fig. 5.8 Gilbert cell mixer architecture

The RF signal is applied to the gate of transistors M1 & M2 which perform a voltage to current conversion. For correct operation these devices should be biased and sized to remain in the linear region and so RF signals considerably less than the 1dB compression point should be used. Performance can be improved by adding degeneration resistors to the source terminals of M1 & M2 but these cause a loss in the conversion gain and are omitted in this design. FETs M3 to M6 provide the switching function controlled by the LO signal. By doing this they channel the RF current through the two loads at the LO frequency and hence implement the multiplication function. For proper operation, the LO signal swing must be large enough to completely switch M3-M6 on and off.

5.2.3 Hybrid Mixer

In the previous section, we have seen two similar mixing techniques, one implementing voltage mixing and the other current mixing. But in both these structures, in order to achieve high conversion gain while maintaining the large operating bandwidth required in UWB systems, the transconductances of the M1 and M2 need to be increased resulting in unacceptably large power consumption. The benefits of hybrid structures for increasing conversion gain and bandwidth have been previously shown for multiplier applications in [30]. In this thesis, a hybrid mixer structure, shown in Fig.5.9 which incorporates both the Gilbert cell and GSI mixers together without raising the power consumption is shown.

It uses a flipped voltage follower (FVF) to feed the RF signal to the drain of M11 and M12 in order to implement the voltage mixing operation of the GSI mixer. The FVF is used instead of the more conventional source follower because its sourcing ability is relatively independent on the biasing current source [31]. Moreover, the current flowing

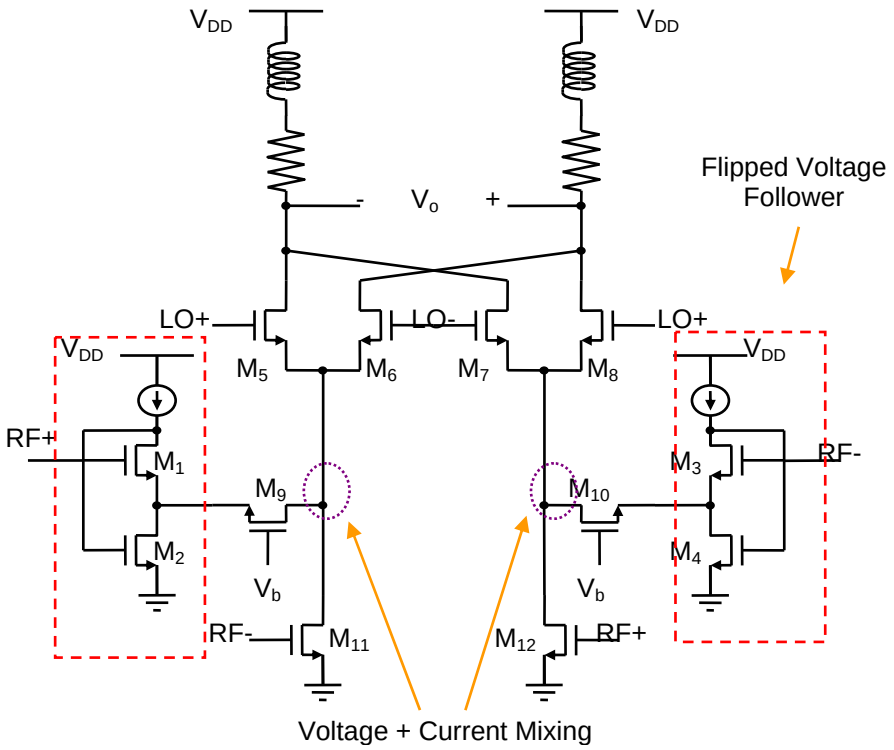


Fig. 5.9 Hybrid mixer architecture

through transistor M1 and M3 is not dependent on the output current as is the case in the source follower. This means that FVF causes smaller attenuation (-2dB) than the source follower (-5dB) at high frequencies even when driving small loads. To increase the mixer bandwidth, shunt peaking inductor loads (250Ω and 2.65nH) are used to cancel the dominant pole of the system and hence boost the conversion gain at high frequencies. To further extend the bandwidth, the second dominant pole location, which occurs due to the capacitance at the output node of the FVF, needs to be pushed to higher frequencies. FETs M9 and M10 are biased in the linear region and act like resistors in the signal path, and are used to reposition the non-dominant pole of the system [30].

The optimum LO signal level for maximum conversion gain was found through simulation to be between -2dBm to 5dBm and in this case, Fig. 5.10 shows the overall conversion gain of the mixer to be greater than 5.5 dB over the entire 3.1-4.8 GHz

bandwidth. Fig. 5.11(a)–(c) show the isolation performance of the mixer to be adequate to avoid adverse LO or RF leakage. With a high gain LNA preceding it, the 11dB NF shown in Fig. 5.11(d) will be suppressed significantly and hence is acceptable.

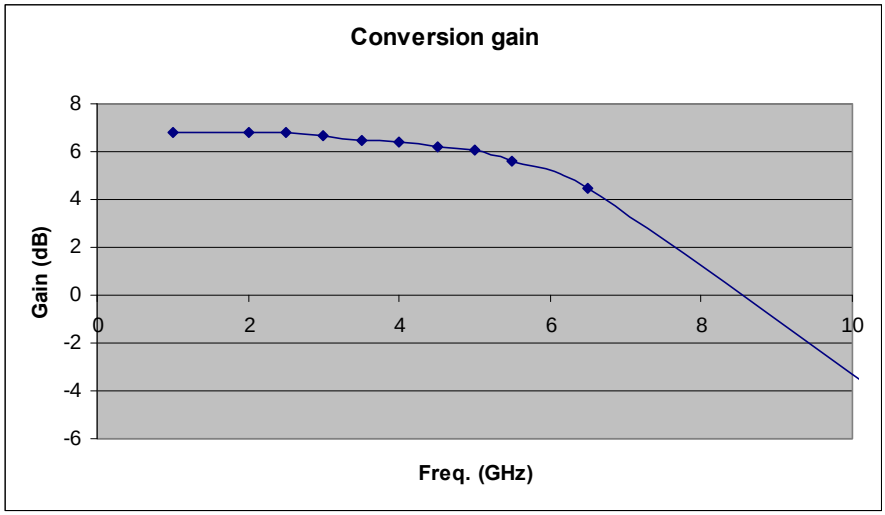


Fig. 5.10 Hybrid mixer conversion gain

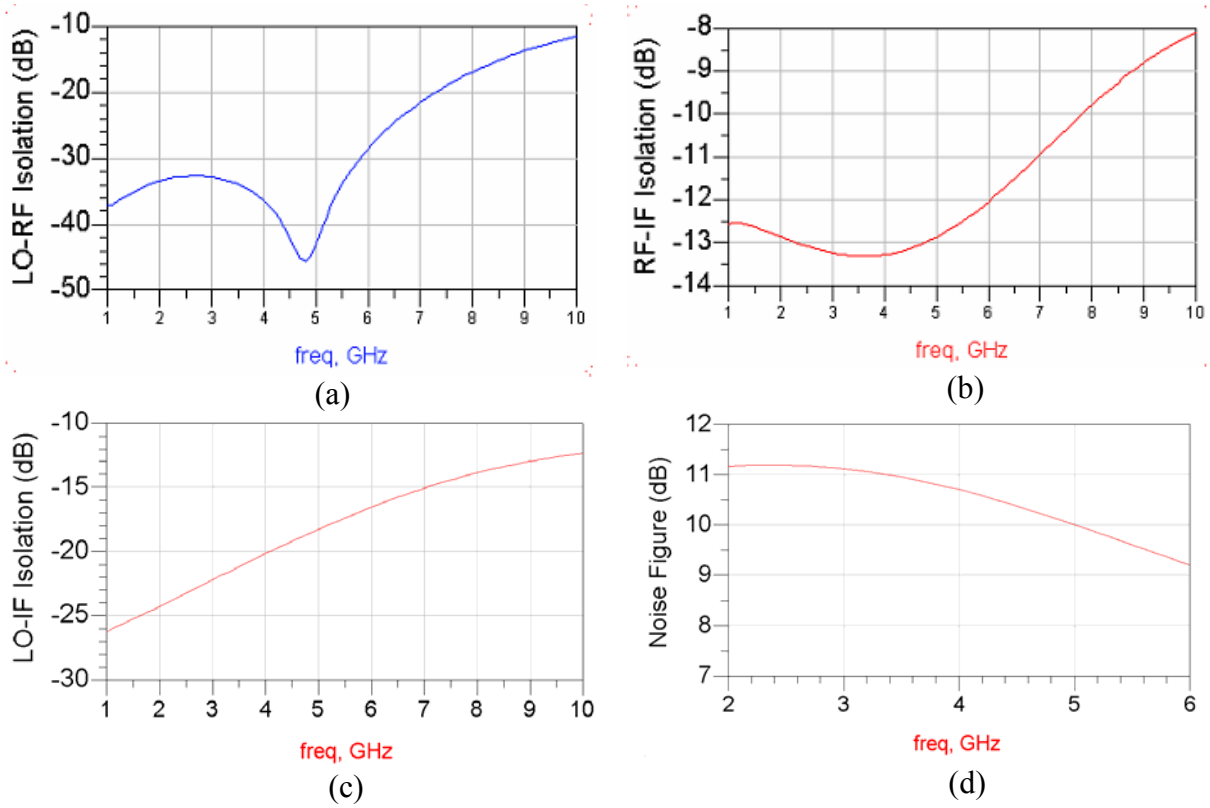


Fig. 5.11 (a) LO-RF Isolation (b) RF-IF Isolation (c) LO-IF Isolation (d) Noise Figure

5.3 Quadrature VCO

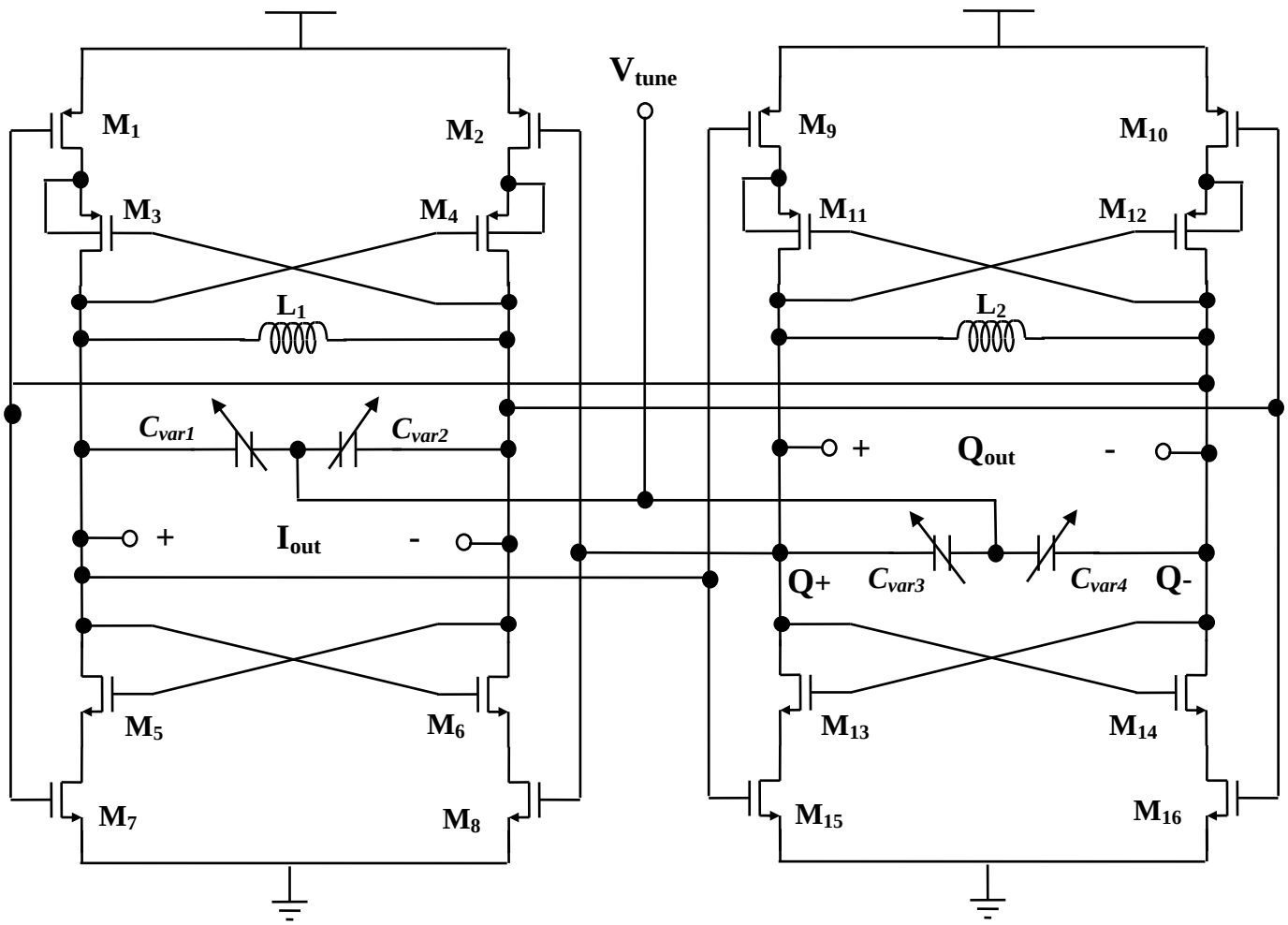


Fig. 5.12 QVCO structure

The QVCO used to generate the LO tones for this project is a cross-coupled L-C tank VCO as shown in Fig. 5.12. The structure consists of 2 oscillator cores for the differential I and Q tone generation. In each core the complimentary switching pairs are connected in a cascode structure with the cross-coupled transistor pairs (M_3/M_4, M_5/M_6, M_{11}/M_{12}, and M_{13}/M_{14}) in order to enhance the phase noise performance [32].

The oscillation frequency, f_{osc} of this L-C resonant QVCO is determined by the tank inductors (L_1, L_2) and varactor capacitances (C_{var1}/ C_{var2} and C_{var3}/ C_{var4}) as,

$$f_{osc} = \frac{1}{2\pi\sqrt{LC_{eff}}} \tag{5.23}$$

where C_{eq} is the overall capacitance present in the tank. Hence by using an external tuning voltage to change the varactor capacitance, the f_{osc} can be tuned dynamically. The QVCO is capable of providing more than 900MHz tuning range (3.5 – 4.4 GHz) in the required UWB bandwidth for tuning voltage ranging from 0V - 1.8V with LO signal strength greater than 800 mV peak-peak. The I-Q signal phase mismatch is less than 3° and the VCO jitter is less than 20ps.

5.4 R-2R Digital to Analog Converter

The DAC is a device used to convert a fixed point *N*-bit binary number into a physical quantity, usually an electrical voltage. Normally the output voltage is a linear function of the input number. In the receiver application discussed in this thesis, the DAC is used to produce a control voltage that is used to tune the QVCO over its entire tuning range. It has a 4-bit input which drives the output voltage between 0V and 1.8V, which is the desired tuning voltage range for the QVCO. Some key DAC performance parameters are briefly defined below for clearer understanding of the following discussions.

Gain Error - Distance between the theoretical and real values measured on the last transition of the converter and expressed in LSB assuming offset error has been adjusted.

Offset Error - Distance between the theoretical and real output values measured on the first transition of the converter and expressed in LSB

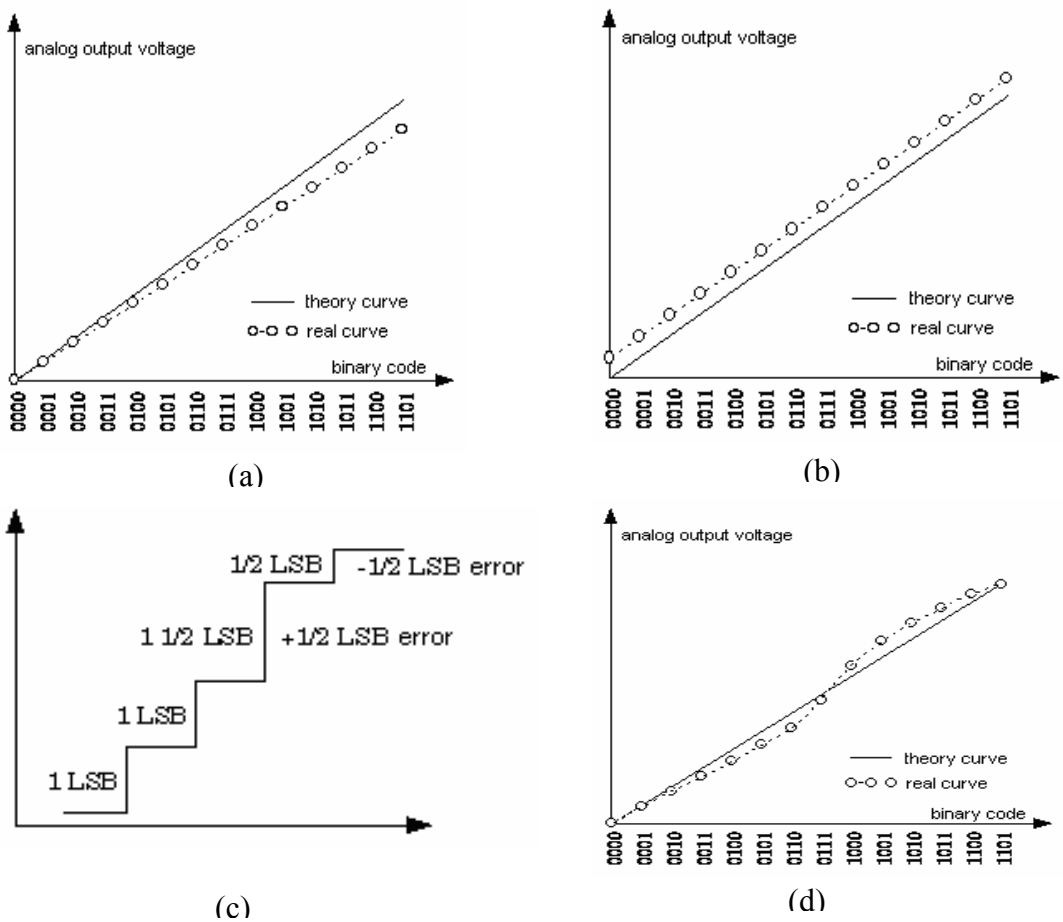


Fig. 5.13 (a) Gain error (b) Offset error (c) DNL representation (d) INL representation [33]

Differential Non-linearity (DNL) – DNL is computed as the difference between the analog output values corresponding to two successive input codes referred to one LSB.

Integral Non-linearity (INL) – INL is the maximum difference noticed over the entire range of conversion between the theoretical values and real values

Several DAC architectures have been discussed in literature and were considered for this work like weighted resistor network DAC and segmented DAC. Weighted resistor networks are simple to design but require several different and often large resistance values which make them very susceptible to process variations [34]. A segmented DAC links 2 or more internal DACs to form one DAC of higher resolution and hence are only

optimal for more than 8-bit operation. An R-2R resistor ladder DAC is chosen because it provides the best INL and DNL performance (less than 0.5 LSB) for a medium resolution DAC (less than 5 bits). Moreover, the fact that only 2 distinct and relatively small resistor values are required minimizes its total resistance [35] and this greatly reduces the errors due to mismatch and increases its process tolerance.

5.4.1 R-2R Ladder

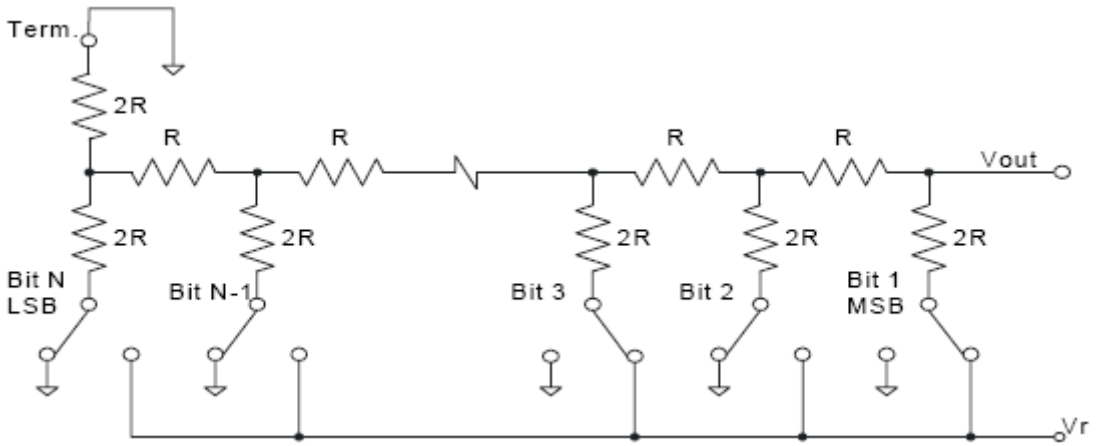


Fig. 5.14 N-bit R-2R ladder in voltage mode

The R-2R network is one of the simplest and most effective ways of achieving accurate voltage division which is essential to the performance of a DAC. Fig. 5.14

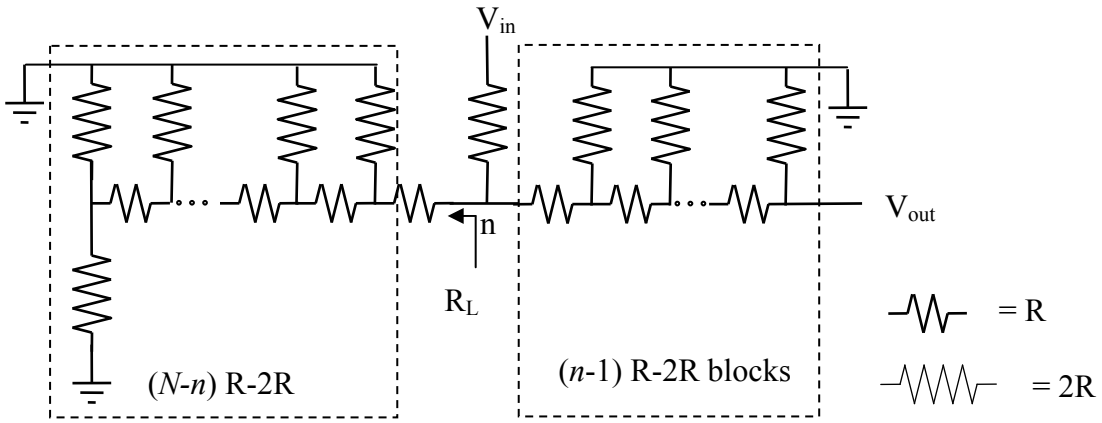


Fig. 5.15 R-2R ladder with [0,0,..,bn = 1, 0,0… 0] input

shows an ideal *N*-bit R-2R ladder network where R is a discrete resistance value.

The network is controlled by an *N*-bit word [$b_1, b_2 \ldots b_N$] which controls the switches that connect the 2R resistors to either V_{in} (bit value '1') or ground (bit value '0'). For the sake of simplicity, let us consider the case where only a single bit, b_n is '1' and the rest are zero. The switching caused by this input will cause the R-2R ladder to look like Fig. 5.15. We notice that the equivalent resistance seen to the left of node 'n' in Fig. 5.15, R_L is 2R for any value of *n*. Therefore, the equivalent circuit shown in Fig. 5.16 can be derived.

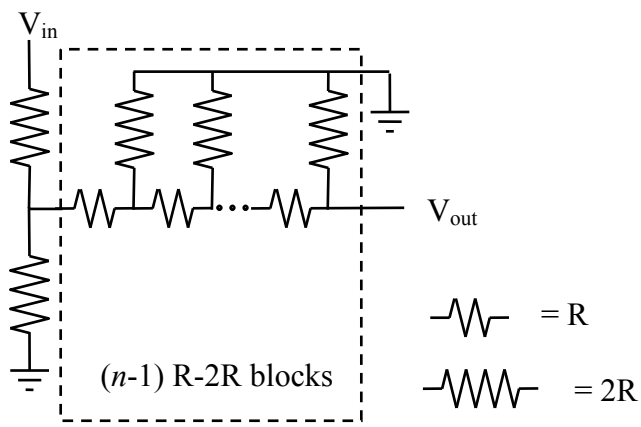


Fig. 5.16 R-2R ladder equivalent circuit

By repeatedly applying the Thevenin theorem on this circuit, we can easily calculate the output voltage in this case (when b_n is '1' and the rest are zero) as $V_{out} = \frac{V_{in}}{2^n}$.

Therefore the general output voltage due to bit *n* independent of the other bit values is

$$V_{out,n} = b_n \frac{V_{in}}{2^n} \quad , b_n = \text{'1' or '0'} \tag{5.24}$$

Since the R-2R DAC is a linear device, the voltage superposition law applies, and hence the total output voltage in response to a random data input [$b_1, b_2 \ldots b_N$] can be calculated as the sum of the independent output voltage contributions of each bit individually as,

$$V_{out} = \sum_{n=1}^{n=N} b_n \frac{V_{in}}{2^n} = V_{in} \sum_{n=1}^{n=N} b_n \frac{1}{2^n} \tag{5.25}$$

From Eqn. 5.19, we can see that the R-2R ladder can produce 2*n* discrete output voltages between 0V and V_{in} with a LSB step size of $\frac{V_{in}}{2^n}$.

5.4.2 Voltage mode R-2R DAC

The R-2R ladder is typically used in one of two ways to construct a DAC. Current mode exploits current division along the ladder while voltage mode is based on voltage division. However a current mode DAC would require a dual supply (negative and positive) op-amp in order to achieve functionality [36] and hence is unsuitable for our application.

Very careful attention needs to be paid to the drivability of the DAC because capacitive loads can severely deteriorate the settling time of the DAC output and low impedances can load the R-2R chain and hence affect its accuracy. In order to be able to drive the varactor load of the QVCO as required in its application in the receiver chain, the DAC is implemented as shown in Fig. 5.17 in this work. Here a high gain, low bandwidth op-amp [37] is used to drive the output load so that the R-2R output node, V_o is buffered with the large op-amp input impedance while the drivability of the op-amp output stage can charge even large capacitive loads to the correct value quickly. For proper operation, the op-amp needs to be in its correct operating region for input DC levels from 0V up to V_{in}. If V_{in} is 1.8V, then the op-amp design becomes overly difficult. In order to solve this problem, a non-inverting voltage divider op-amp configuration is used so that.

$$V_{out} = (1 + \frac{2R_b}{R_b})V_o = 3V_o \tag{5.26}$$

In this way, to achieve the required output range of 1.8V, V_{in} needs to be set to only 0.6V. This technique also has the added advantage of lowering the total power consumption of the DAC. Fig. 5.18(a) shows the monotonic output step response while Fig. 5.18(b) shows the maximum step (0V-1.8V) settling time of the DAC when loaded with the QVCO to be 25ns. Fig. 5.19 shows the op-amp gain and phase response.

Another critical design consideration is to choose the right 'R' value. Two factors influence this choice, the switch resistance and the settling time. Even though the switches used in this DAC were designed with large transistor sizes, they still have a small finite resistance, and hence the R value must be large to minimize the effect of the switch resistance on the R-2R ladder. But, in order to achieve fast charging of node V_o and hence minimize the settling time, R must be small. After extensive simulations, the best compromise was achieved for R = 2.1 kΩ

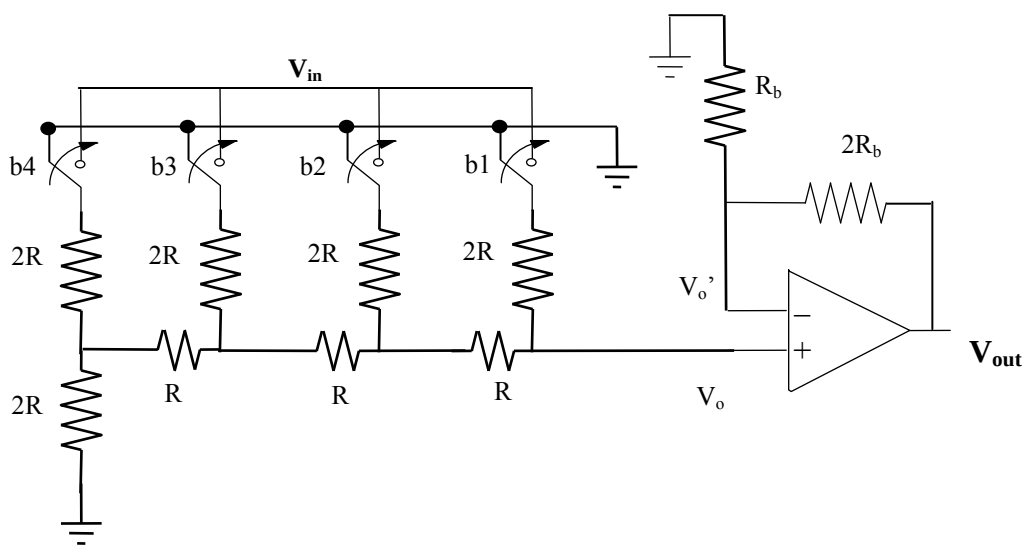


Fig. 5.17 Proposed R-2R ladder DAC circuit

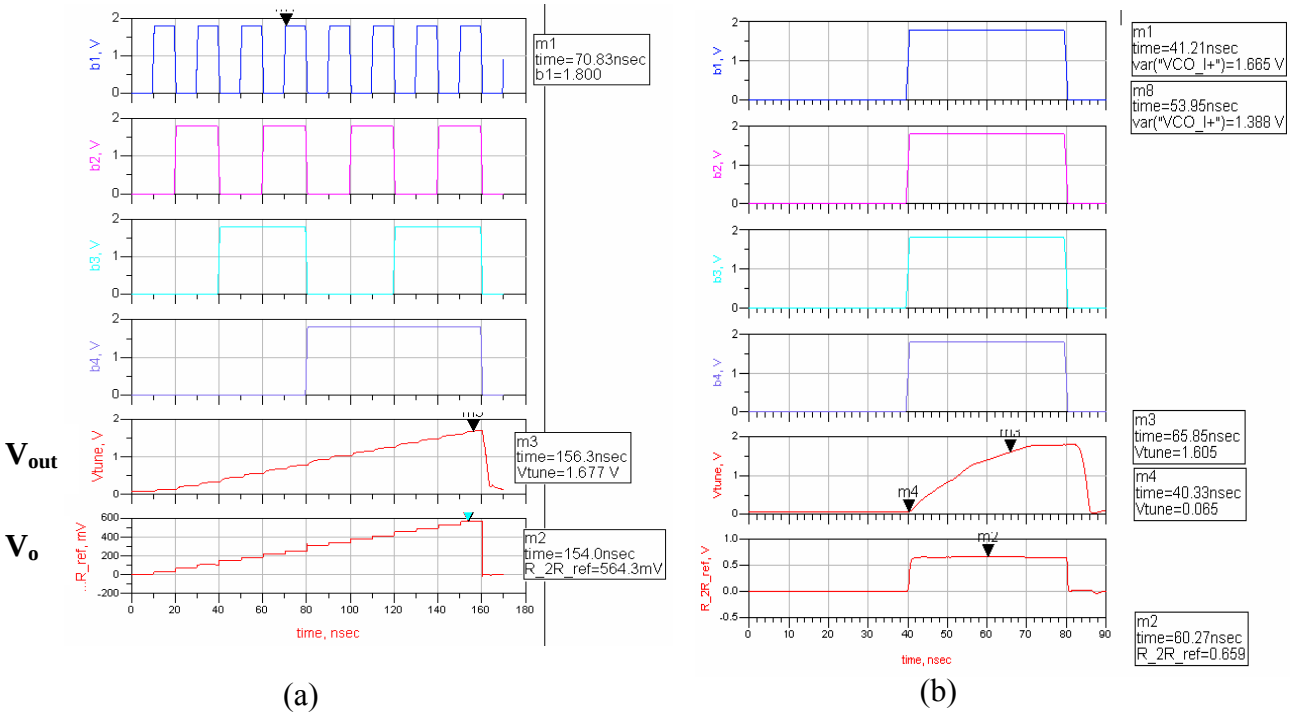


Fig. 5.18 Loaded DAC output for (a) Monotonic step input (b) Maximum step input

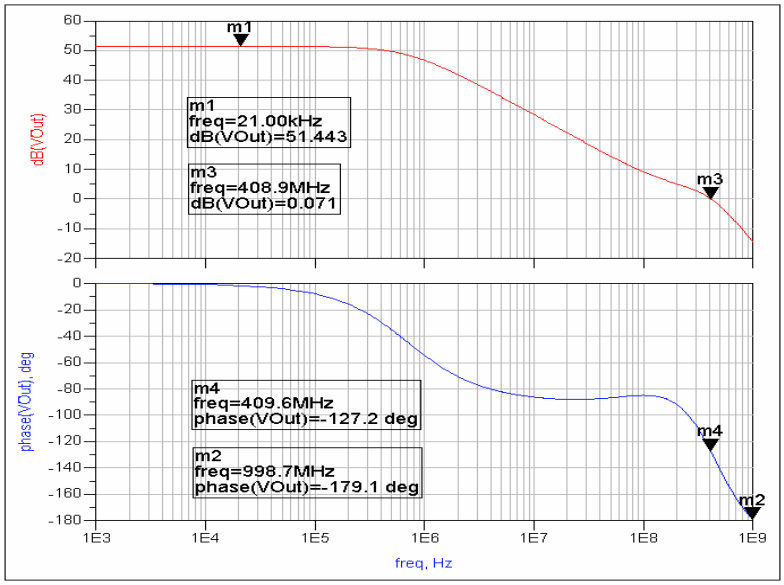


Fig. 5.19 Op-amp Gain and phase response

5.5 Low-pass Filter and IF Amplifier

The low-pass filter in this application is used to extract the desired down-converted sub-band signal while rejecting the other sub-band as well as any in-band narrowband interferers to prevent ISI and improve the interference rejection capability of the receiver. In order to achieve this, the filter needs to have a large variable bandwidth for maximum signal capture as well as a sharp roll-off for maximum stop-band attenuation.

The LPF structure is implemented as a 5th order Elliptic filter with one differential first order G_m-C filter stage (Fig. 5.20) and 2 differential bi-quadratic G_m-C filter stages cascaded in series.

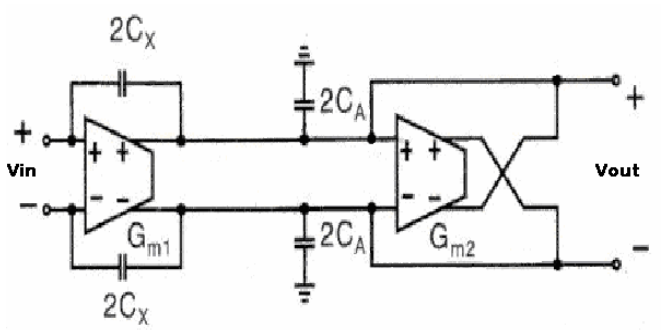


Fig. 5.20 First order G_m-C filter

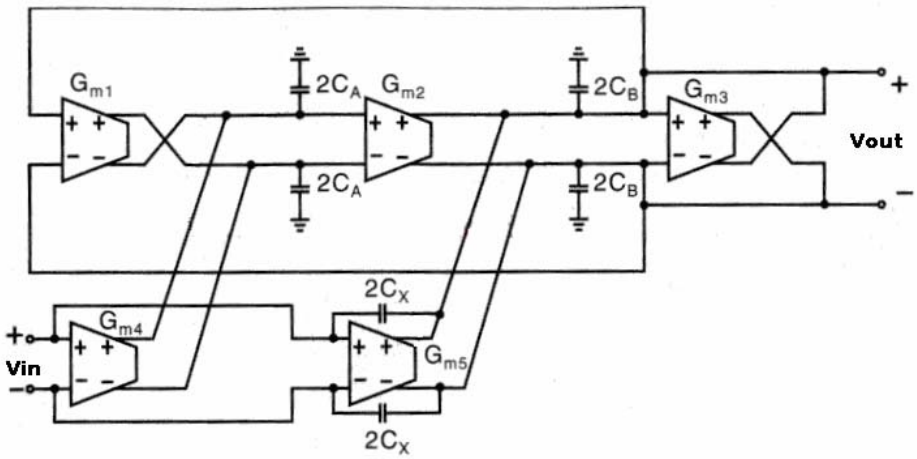


Fig. 5.21 Bi-quadratic G_m-C filter

The role of the IF amp in the receiver chain is to boost the desired filtered signal to beyond the squarer input threshold (defined in next section). In order to do so, it not only needs to provide high gain, but also achieve an overall bandwidth that is greater than the maximum filter bandwidth (300 MHz) so that no signal distortion occurs.

Fig. 5.22 shows the IF amplifier implementation used which consists of two cascaded NMOS differential gain stages. The first stage utilizes an active PMOS load (M7, M8) with common mode feedback and provides the bulk of the overall gain. The second stage is a simple differential pair with a resistive load that provides low gain and acts as a buffer to drive the next stage (squarer) without compromising the bandwidth. To achieve this, the 1st stage differential pair transistors M6, M5 as well as the active loads M7/M8 are optimized for high gain while 2nd stage input transistors M9, M10 are made very small (1μ width) to reduce the loading capacitance seen by the 1st stage. The 2nd stage

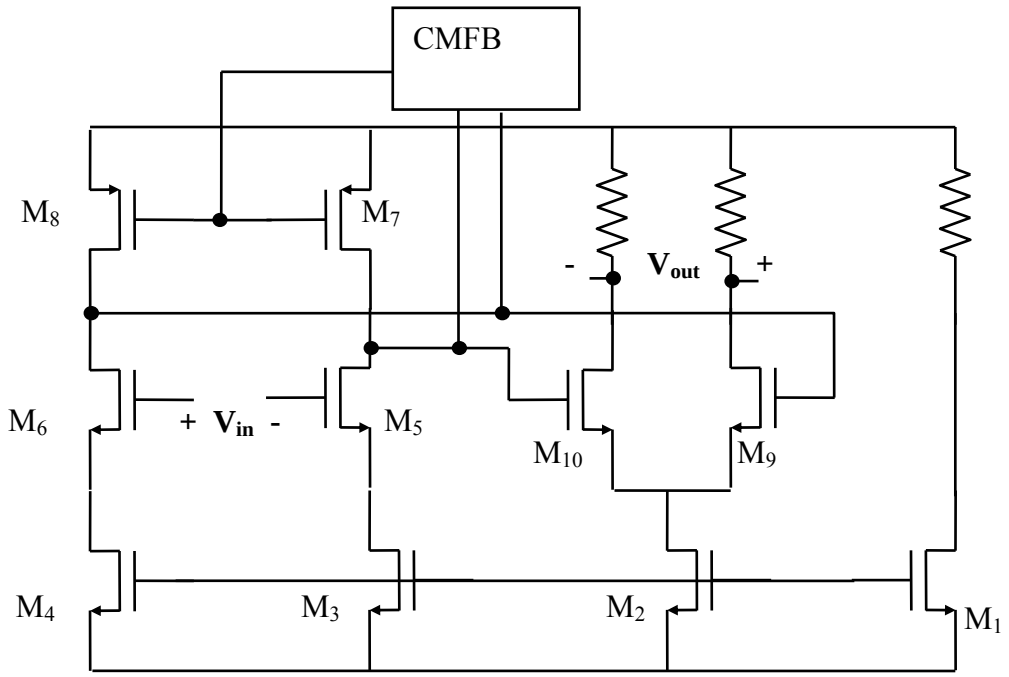


Fig. 5.22 Intermediate Frequency (IF) Amplifier

bias current is chosen to be relatively large by sizing up the mirror transistor M2 so that it can maintain the required overall bandwidth while driving the required load at the expense of lower gain. The CMFB circuit ensures that device mismatches do not cause the output common mode to shift and saturate the subsequent stages. Fig. 5.23(a) shows that the 5th order filter has an effective tuning range of 40-300MHz with -6dB gain. The IF amplifier provides 27dB gain over 330MHz bandwidth. Fig. 5.23(b) shows the frequency response of the Filter + IF Amplifier combination with 21dB overall gain.

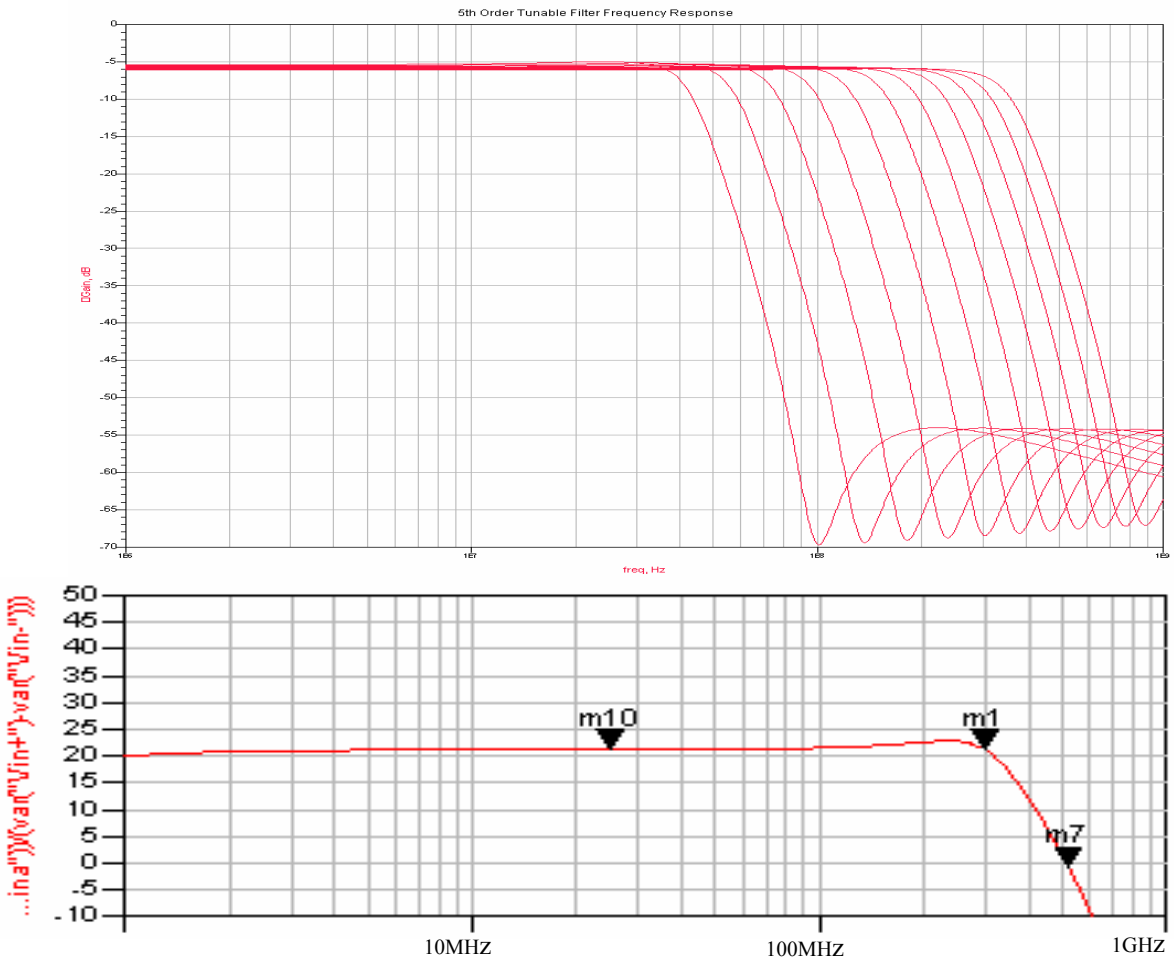


Fig. 5.23 Frequency response of (a) 5th order Elliptic LPF
(b) Filter + IF Amplifier

5.6 Squarer

The squarer is essentially a multiplier in which both inputs are fed the same signal. In I-UWB applications, the squarer is most commonly used in the non-coherent auto-correlation receiver to perform the correlation function. But, in this application, the role of the squarer is to enable the removal of the phase mismatch between the transmitted carrier and the locally generated LO template as discussed in section 4.3. Another key difference in this application is that the squarer input bandwidth does not need to be extended to accommodate UWB pulses. In this application, the squarer input is the filtered output of the LPF and hence an input bandwidth greater than the maximum LPF passband (300MHz) is sufficient.

In order to implement the multiplication function, the same four quadrant cancellation schemes that are mentioned in section 5.2 apply and hence the Gilbert cell architecture mentioned in section 5.2.2 is used in this block as well because of its proven robustness. The schematic of the squarer architecture is shown in Fig 5.24.

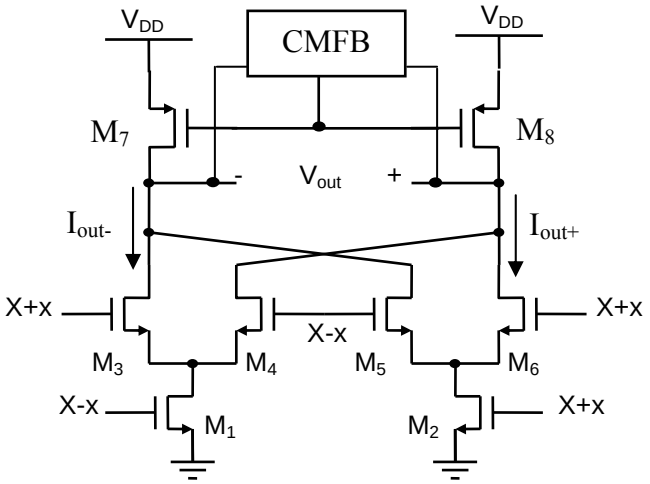


Fig. 5.24 Squarer architecture

Following a similar analysis and nomenclature as that of section 5.2, we can calculate the total multiplied output current of the squarer as [38]

$$I_{total} = I_{out+} - I_{out-} = (I_4 - I_3) + (I_6 - I_5) \tag{5.27}$$

Assuming $\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_{3,4,5,6} = k_A$ and $\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_{1,2} = k_B$,

$$I_{total} = 2k_B x\left[\sqrt{\frac{k_A}{k_B}\left(\sqrt{\frac{2I_{bias}}{k_A} - 2x^2} - \sqrt{2}x\right)^2 + 2x^2} - \sqrt{\left(\frac{k_B}{k_A}\sqrt{\frac{2I_{bias}}{k_B} - 2x^2} - \sqrt{2}x\right)^2 - 2x^2}\right] \tag{5.28}$$

where I_{bias} is the DC bias current of M1 and M2. Assuming x and y are small,

$$I_{total} = 4\sqrt{2}k_A x^2 \tag{5.29}$$

Now let $V_{out} = I_{total} \times R_{load} = A_{sq} x^2$ (5.30)

where R_{load} is the load impedance and A_{sq} is defined as the squarer gain. Since we know that a wide bandwidth gain function is not needed for this application, the R_{load} is implemented as a PMOS active load pair (M7, M8) with common mode feedback to increase the achievable gain. The gain is maximized by making M3-M6 large to raise k_A and M1, M2 small to lower I_{bias} and hence increase the active load impedance. However, the gain cannot be increased indiscriminately because as gain increases the output bandwidth decreases causing significant signal spreading which will badly distort the pulse shape. In this design, an A_{sq} of 65 and output bandwidth of approximately 210 MHz was achieved with a total current consumption of 2.3 mA. Fig. 5.25 shows the transient response of the squarer output with a filtered pulse train input.

From Eq. (5.30) we can see that for small input values the squaring function causes a significant reduction in the signal swing. Hence, we can define the squarer input

threshold. V_{Tsq} as the minimum signal level at which the squarer can operate without attenuating the input signal.

$$V_{out} = A_{sq} V_{Tsq}{}^{2} \geq V_{Tsq} \text{. Therefore } V_{Tsq} \geq \frac{1}{A_{sq}} = \frac{1}{65} = 15.4mV \qquad (5.31)$$

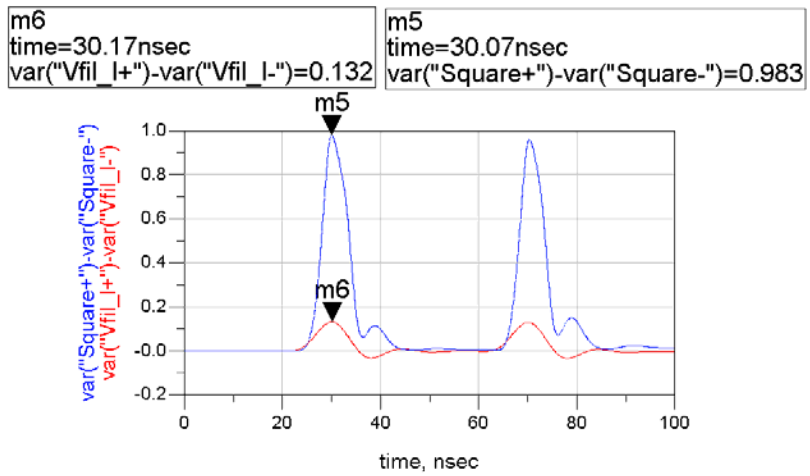


Fig. 5.25 Squarer transient response with a filtered pulse train input

5.7 Differential to Single-ended (D-S) converter

Up till now all receiver components have been differential in nature. But the comparator used in this work is a single input device and hence a D-S converter is required. The role of this block is not only to convert the signal but also to amplify it beyond the switching threshold of the comparator so that the right demodulated data can be generated. Since the inputs pulse train to this block has already been squared, it only has an upswing and hence it is essential to make sure that the output common mode level of this stage of the D-S converter is as low as possible to allow maximum output signal swing.

Fig. 5.26 shows the schematic of the D-S converter which is implemented as a PMOS differential pair with active NMOS loads. The differential gain of this stage, A_v can be written as:

$$A_v = g_{m\,PMOS} \frac{r_{oNMOS}}{2} \tag{5.32}$$

In order to get a low output common mode voltage, relatively large NMOS load transistors are used and the resulting loss in gain is made up by optimizing the PMOS differential pair sizes and the biasing current. This block consumes 0.8mA current and provides 16dB gain while maintaining an output common mode voltage of 480 mV.

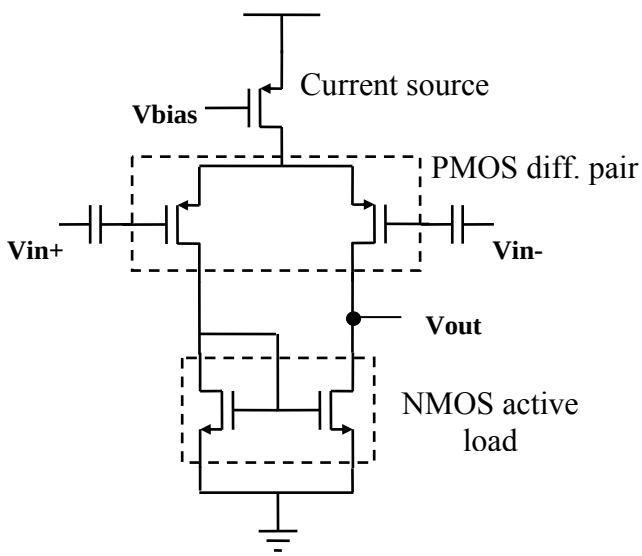


Fig. 5.26 Differential to Single-ended converter

5.8 Comparator

The comparator is the last stage in the receiver chain and is responsible for converting the demodulated analog signal to a non return to zero (NRZ) pulse train. Although in traditional circuits, an Analog to Digital converter (ADC) is used for this purpose, it is unsuitable in I-UWB receiver applications because even after down-conversion and pulse spreading effects of low-pass filtering, the width of the input pulse to the comparator is still too narrow and would require an unreasonably fast ADC for Nyquist rate sampling.

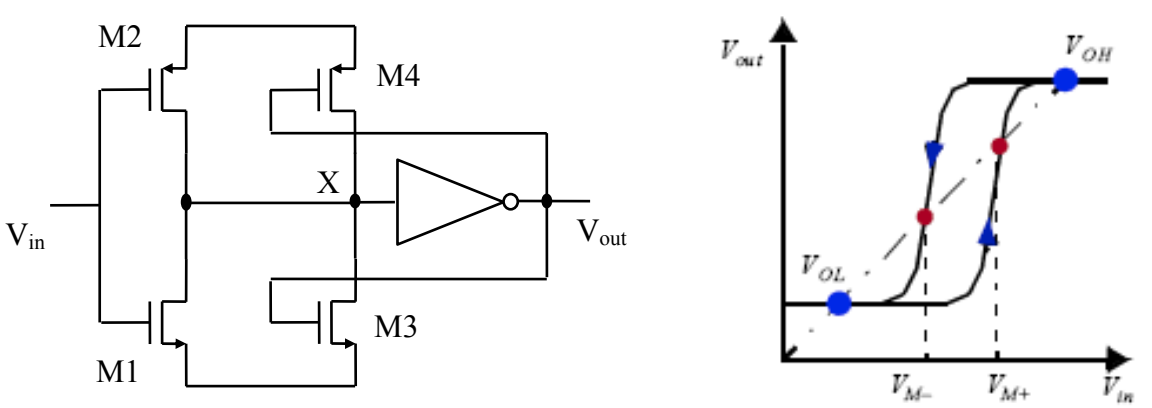
The comparator used in this thesis is based on the classic Schmitt trigger circuit shown in Fig 5.27(a). The Schmitt trigger is a dual threshold comparator circuit that incorporates positive feedback to achieve its hysterisis properties. The main benefit of a Schmitt trigger over a fixed threshold comparator is greater stability (noise immunity). With only one input threshold, a noisy input signal near that threshold could cause the output to switch rapidly back and forth due to noise alone. The Schmitt trigger on the other hand has memory and holds its state until a significant deviation, which is designed to be greater than the noise level, is reached. By doing so, it helps to clean up the noisy signal before it is fed to the baseband processor.

The Schmitt trigger design is governed by the device sizes of M1-M4 where M3 and M4 effectively move the switching voltage of the inverter formed my M1 and M2 while the last stage inverter provides positive feedback that gives this circuit its 'memory'. In the case where V_{in} is '0', at steady state, V_X = '1' and V_{out} ='0' and hence only transistors M2 and M4 are on. As V_{in} starts to rise, transistors M1 and M2 start to turn on and off respectively but M4 remains in strong saturation. Therefore the switching voltage of node X, V_{M+} and consequently the output is determined by the ratio

$\frac{\mu_p C_{ox}\left(\frac{W}{L}\right)_{M4}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1}}$. Similarly, V_{M-} is determined by the ratio $\frac{\mu_n C_{ox}\left(\frac{W}{L}\right)_{M3}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{M2}}$. Therefore, by sizing M3 and M4 appropriately, the hysterisis shown in Fig. 5.27 (a) can be achieved.

Fig. 5.28 shows the overall schematic of the comparator used in this work. It consists of the Schmitt trigger of Fig. 5.27(a) with a 4-stage inverter chain to drive the large capacitive load (10pF) presented by the measuring equipment. The chain is designed to present a small input capacitance to the Schmitt trigger (500fF) and drive a load of 10pF and optimized to achieve the smallest propagation delay. This leads to a calculated fan-out factor of 2.11 (approximated as 2) for a 4 stage design [39].

Fig. 5.29(a) shows the overall hysterisis characteristics of the designed comparator with V_{M+} of 1.077 V and V_{M-} of 365mV while Fig. 5.29(b) shows a rise time of 730 ps, fall time of 630 ps and propagation delay of approximately 550 ps.



(a) **(b)**

Fig. 5.27 (a) CMOS Schmitt trigger and (b) associated hysterisis characteristics

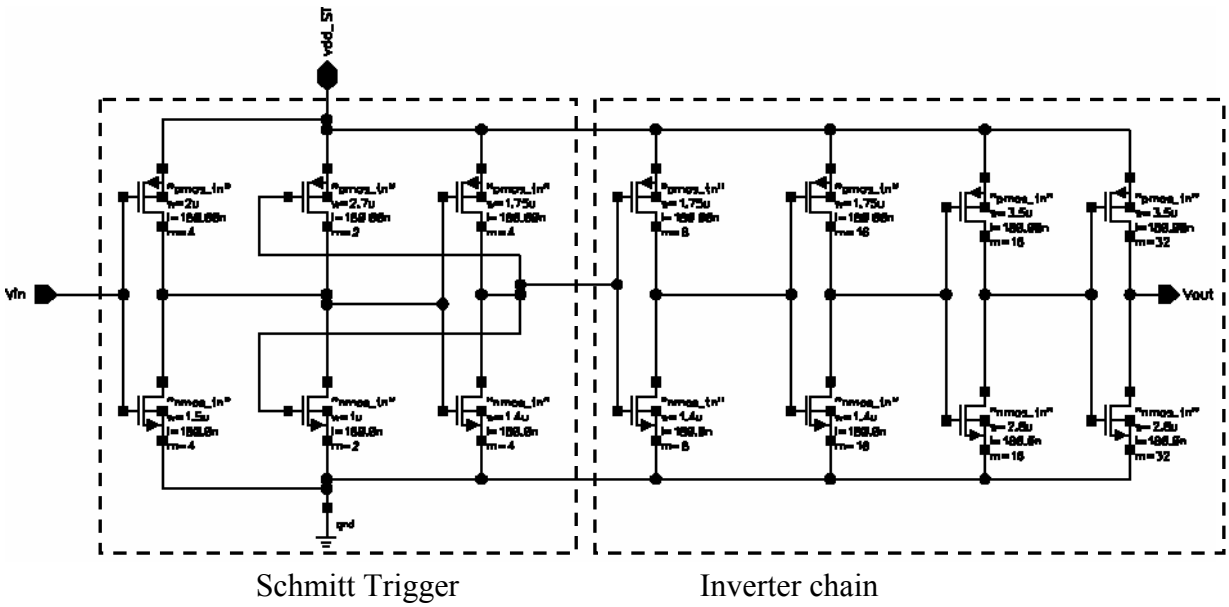


Fig. 5.28 Schmitt trigger with 4-stage inverter chain

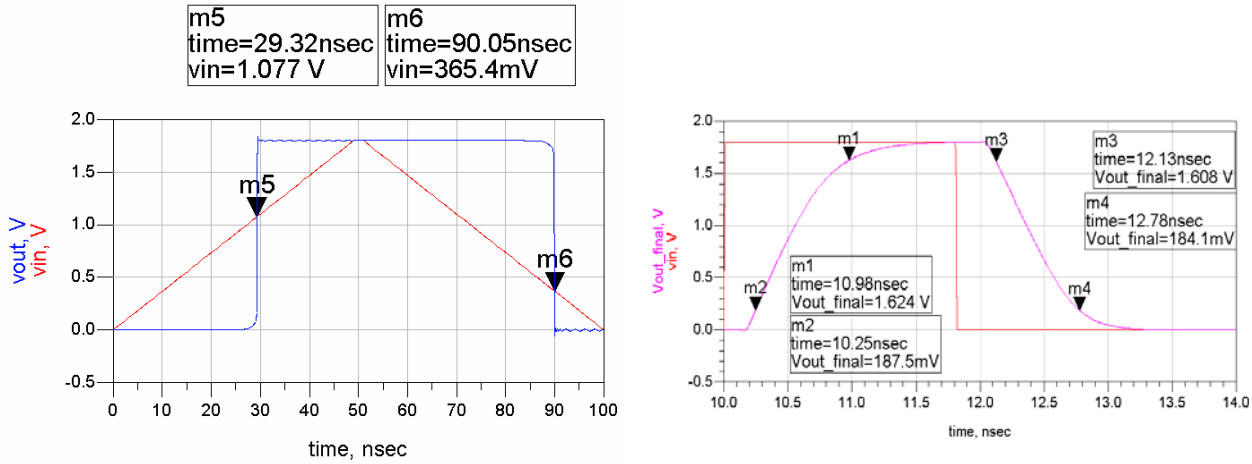


Fig. 5.29 (a) Comparator hysterisis and (b) propagation delays

Chapter 6

System Integration and Simulation results

The Dual-band UWB FSK quadrature receiver architecture was discussed in Chapter 4 and the design of all its components was discussed in Chapter 5. In order to integrate the components so as to achieve the expected performance, careful attention needs to be paid to factors such as inter-stage matching, loading and parasitics introduced by packaging and transmission lines. These and other integration issues will be discussed in the following sections. The first section explains the detailed system simulation setup used and the in the next section, some key layout considerations that were observed for on-chip integration are discussed. In the final detailed simulation results for the entire receiver are presented together with measured results for key sub-blocks, the RF front end as well as the integrated receiver.

6.1 System Simulation setup

Fig. 6.1 and Fig. 6.2 show the system simulation setup used for the front-end and back-end respectively. For simulation, an external UWB monocycle pulse generator block and a -80dB attenuator are used to model the transmitter and channel respectively as shown in Fig. 6.1. The LNA amplifies and performs single-ended to differential conversion on the input pulse train. As mentioned in Chapter 4, the LNA is optimized to drive the 2 mixer loads and the LNA output is connected to the mixers using AC coupling (series capacitors). The 4-bit DAC output voltage is connected directly to the varactor tuning node and the required LO quadrature tones are produced and used for the mixing.

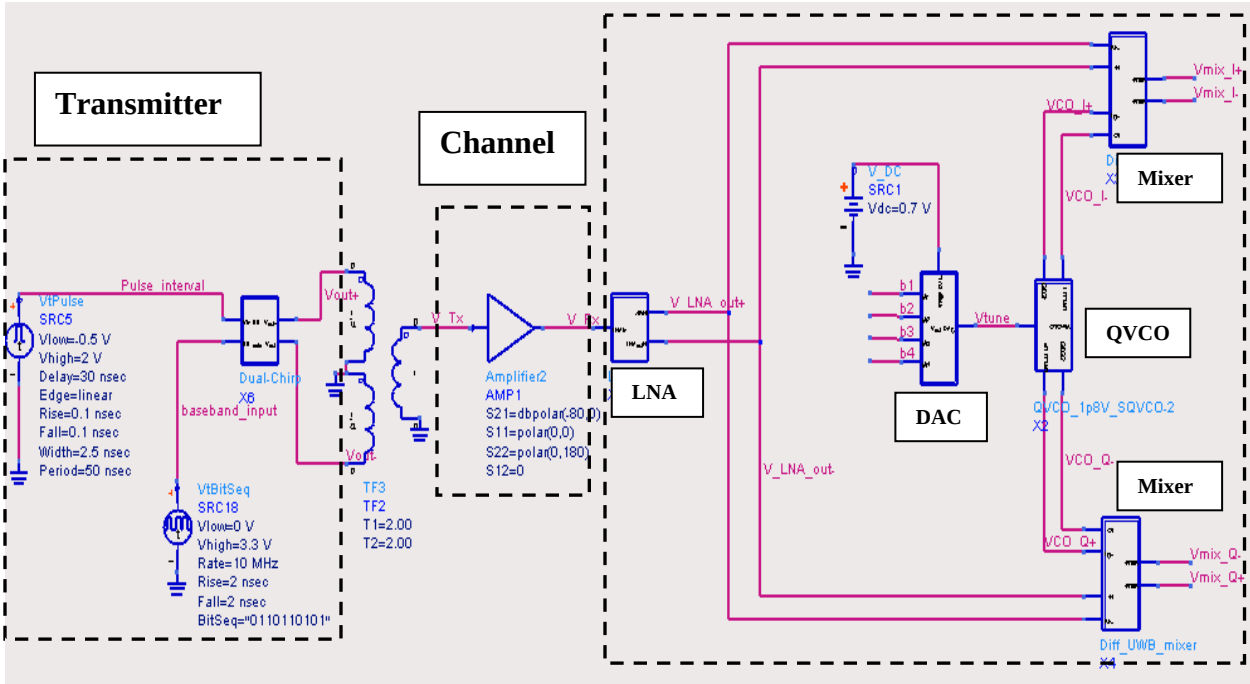


Fig. 6.1 System front-end simulation setup

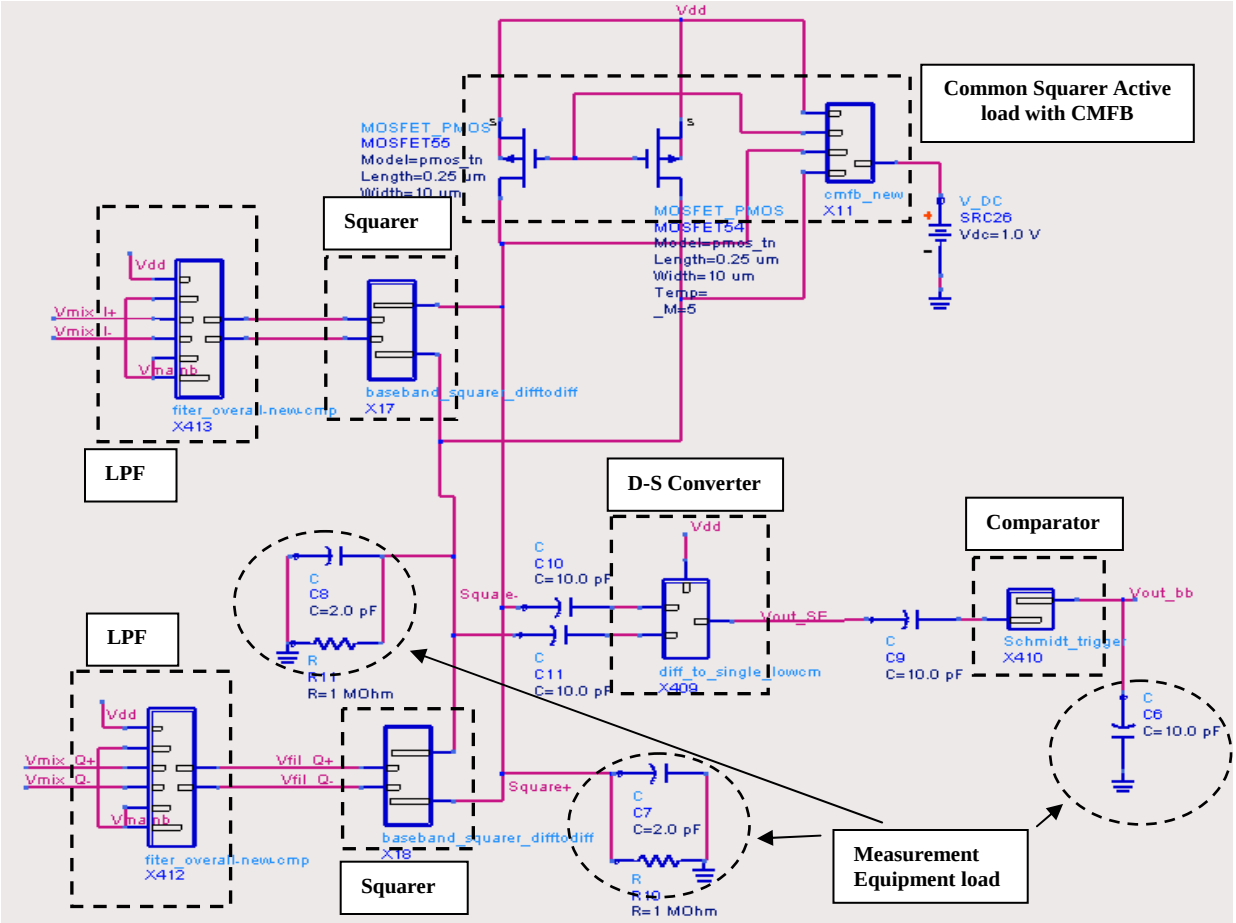


Fig. 6.2 System back-end simulation setup

An important feature of this circuit is that due to the wideband nature of the down-converted signal, AC coupling is utilized at the mixer output and hence any self mixing DC offsets are removed after down-conversion with only minor signal loss. This is a significant advantage over traditional direct conversion receivers discussed in Chapter 3.

In Fig. 6.2, we see that after the down-converted signal has been filtered, the squared differential outputs of the I and Q branch squarers are added by summing the respective currents and dropping them across a common active load. Therefore, the combined differential squarer outputs correspond to $I_{square+}+Q_{square+}$ and $I_{square-}+Q_{square-}$. The signal is subsequently D-S converted and the comparator finally produces the NRZ pulse train corresponding to the desired sub-band data, thereby completing the FSK demodulation. As shown in Fig. 6.2, all external loads expected during measurement have also been included in the simulations. AC coupling has been incorporated in every inter-stage connection. However, larger coupling capacitor sizes were used in the latter stages to preserve the signal integrity.

6.2 Layout considerations

In order to minimize the non-ideal effects of process variation, substrate noise coupling and high frequency signal coupling, careful attention was paid to the layout of the receiver chip. The die photo for the integrated front end is shown in Appendix B while the layout of the fully integrated receiver system is shown in Appendix C. The following is a list of major considerations and techniques used in the layout of the receiver.

- Common-centroid technique and geometrically symmetric layout is used for all the differential pairs and four-transistor cross-coupled pairs.
- All ground planes of the front-end components were separated in order to avoid signal coupling and possible instabilities arising from positive feed-back loops.
- Large numbers of down-bonding pads are provided for the ground planes.
- A dedicated digital ground which is completely isolated from the RF grounds is provided prevent leaked RF signals from corrupting the clean baseband data.
- Guard rings with taps are used for all the front-end circuits to block substrate coupled noise and to avoid latch-up.
- Lengths of high-frequency wires are minimized by careful floor planning and optimal choice of pad order.
- Lengths of wires connecting all the differential signal lines were kept the same in order to minimize the phase and gain mismatch.
- Large de-coupling capacitors to ground are used for every VDD plane.
- Electrostatic Discharge (ESD) protection circuits are used with all the pads.
- Multi-layer metals wires with vias are placed to enclose each high frequency block to avoid interference between blocks.
- Dummy poly is used at both ends of transistor and resistor arrays.
- Metal wires with large width are used for paths with DC current larger than 1mA to ensure reliability.
- Large numbers of vias and contacts are used for all electrical connections.

6.3 Simulation and Measurement results

6.3.1 Integrated receiver simulation results

Fig. 6.3 shows the time domain receiver performance in the case where Band2 data is demodulated while Fig. 6.4 shows the corresponding frequency domain representation of this scenario. As mentioned in the modulation scheme description of Chapter 4, Band2 refers to the 4.2-4.8 GHz sub-band that modulates data bit '1'. The received signal is the modulated pulse sequence corresponding to data "0101010101". The LO signal, shown in Fig. 6.4 is set by the 4-bit DAC to lie in the desired sub-band (4.5 GHz). The LNA amplifies the weak input pulse train (350μV p-p) by 42dB and the mixer down-converts the signal using the LO signal. Fig. 6.4 clearly shows the down-conversion function of the mixer and we can see that in the mixer output, the desired sub-band (Band2) shifts to baseband while the Band1 components and higher order mixing products occupy higher frequencies. The mixer output is then filtered and the LPF output only obtains the desired sub-band data. This signal is then squared, added and converted to a single-ended signal by the squarer and the D-S converter respectively. The D-S comparator also amplifies the signal so that it is over the comparator threshold. The comparator then performs the threshold comparison and outputs the desired NRZ data corresponding to Band2.

Fig. 6.5 shows the receiver performance in the presence of a noisy in-band interferer located in Band2 (at 4.8 GHz). The transmitted data is the same in the first case. However, as described in Chapter 4, Band1 demodulation is preferred in this case so as to achieve the best interference immunity. From Fig.6.5 it can be seen that the desired UWB pulse train has been completely swamped by the much stronger interference signal. The 4-bit DAC inputs and the LPF tuning voltage have been tuned so that the LO frequency and LPF bandwidth meet the conditions specified in Eq. (4.15) and (4.16). As shown in

Fig. 6.5, once these values have been optimally set, the filtered output is free of any interference and the demodulation proceeds as expected through the rest of the receiver chain and the comparator output is the NRZ data corresponding to Band1 as expected.

The simulation results confirm the feasibility of the novel dual-band UWB FSK modulation/ demodulation scheme proposed in this thesis. Moreover, the receiver designed is shown to be capable of implementing this scheme and achieving the interference rejection capabilities that were targeted. Table II summarizes the simulated receiver performance. The receiver gain is calculated from the LNA input to the D-S converter output. The sensitivity is calculated by operating the receiver in its highest gain mode and then lowering the input pulse train signal strength until the demodulated data falls below the comparator threshold and hence cannot be detected.

Further details regarding the system design and performance can be found in the related paper for publication [40]. Measured performance of the fabricated chip is presented in the following sections and compared to the state of the art in recent publication.

Table II: Overall simulated receiver performance

Parameter	Simulated Value	Specification	Units
Operating Frequency Bandwidth	3.1 - 4.8	3.1 - 4.8	GHz
Supply Voltage	1.8	1.8	V
Current Consumption	48 to 84 *	60	mA
Receiver processing Gain	Up to 90	80	dB
Input Pulse width	2 to 6	2 to 6	ns
IIP3	-32	-20	dBm
Max. data rate	40	10	MHz
Sensitivity (Pulse amplitude)	90	100	μV

* For min. and max. LPF pass bandwidth (because power consumption of the LPF increases as bandwidth increases)

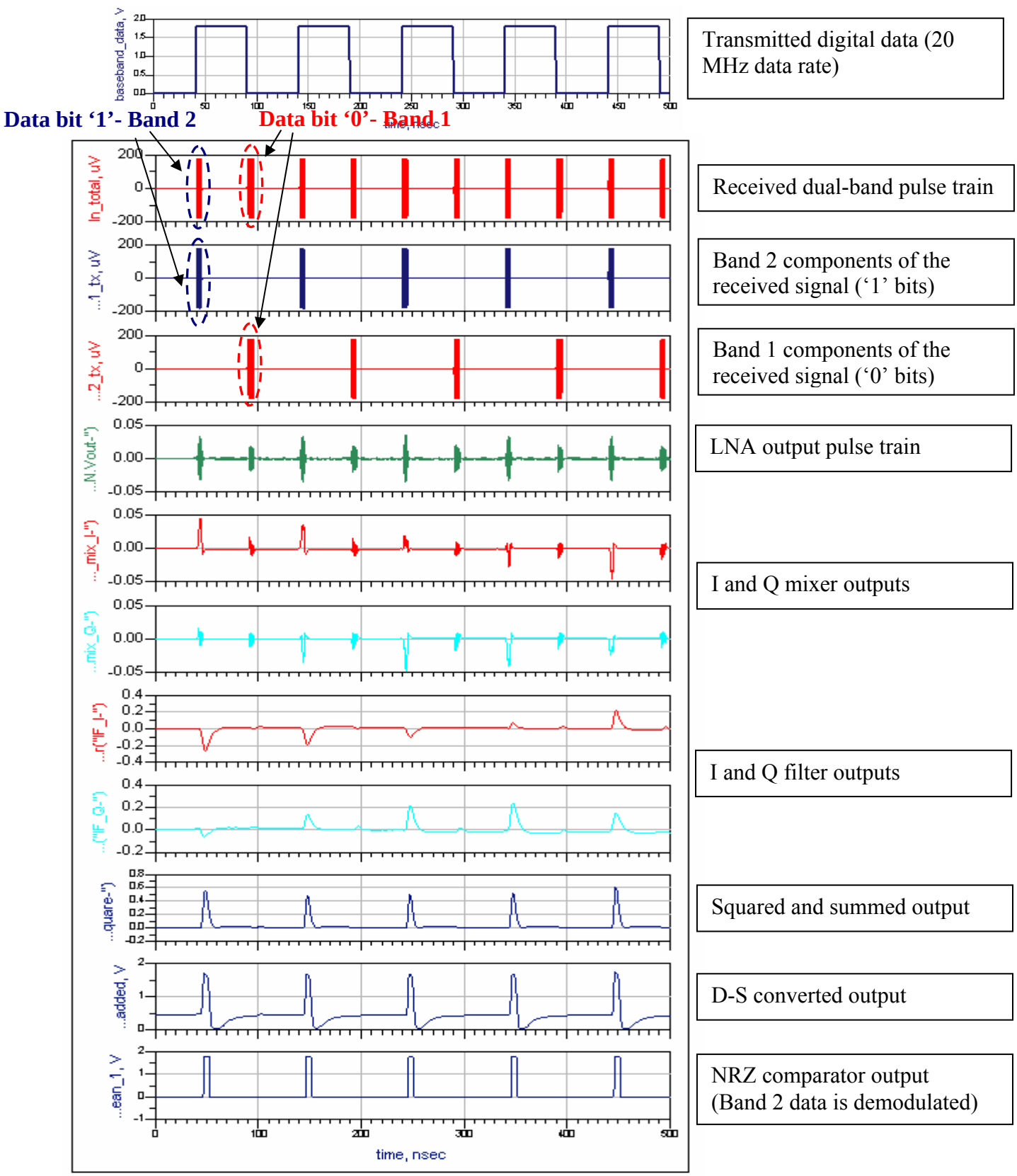


Fig. 6.3 Simulated receiver performance (Band 2 demodulation)

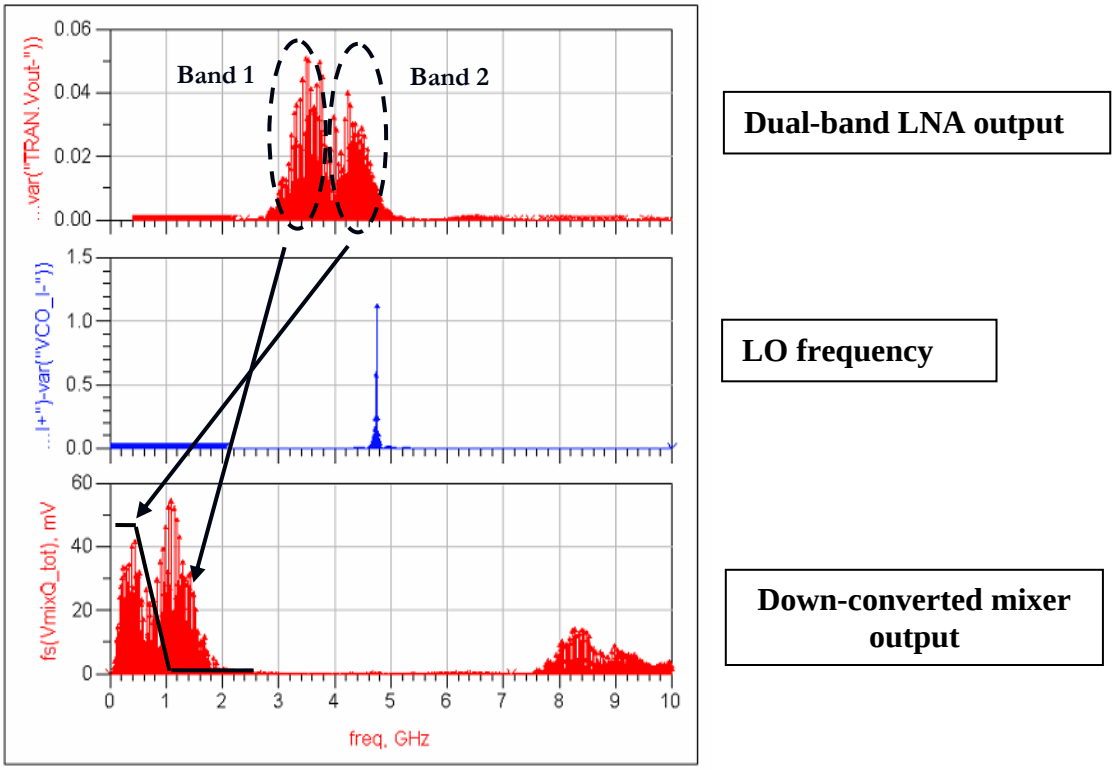


Fig. 6.4 Simulated receiver performance in clean channel (Band 2 demodulation)

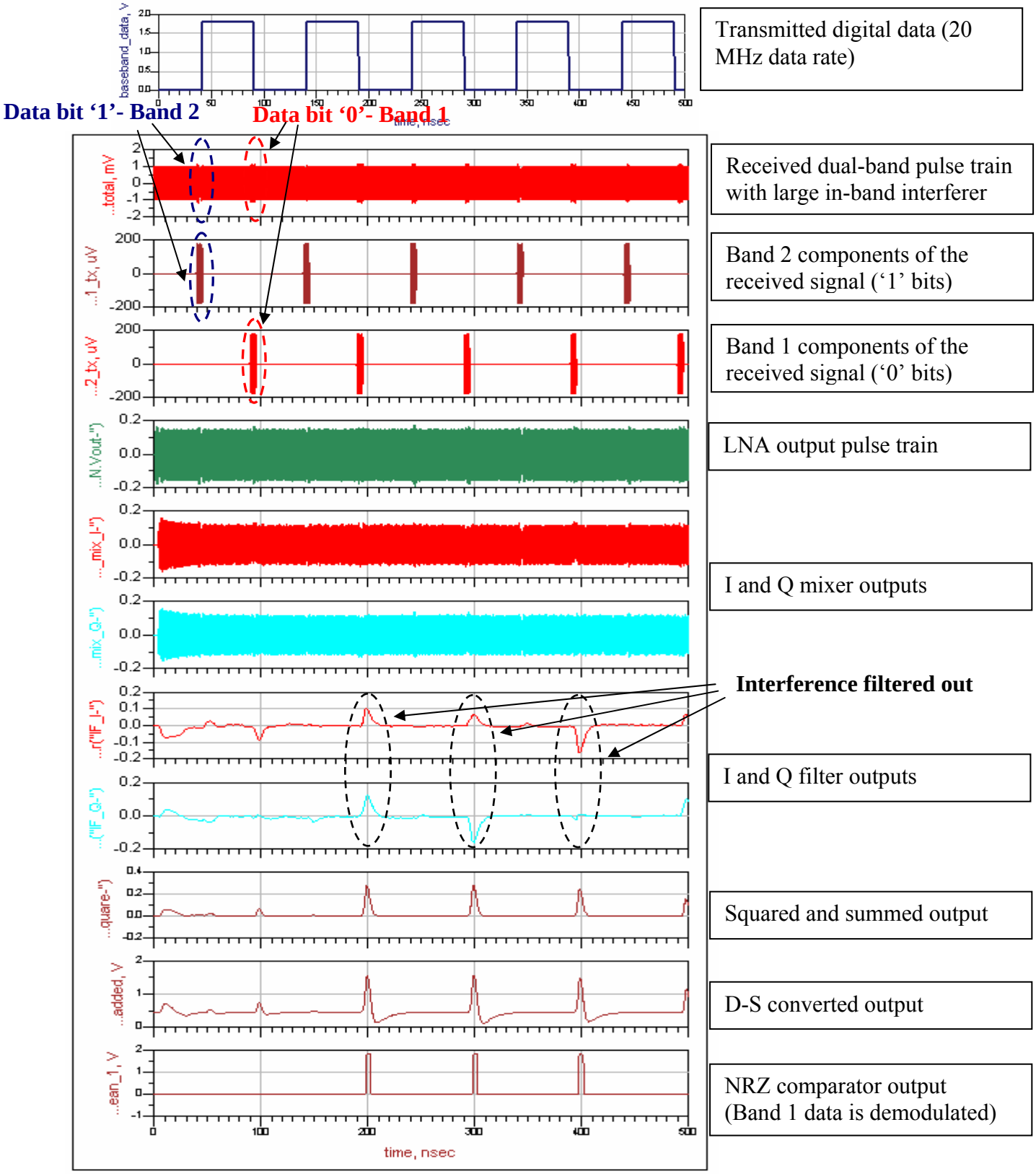


Fig. 6.5 Simulated receiver demodulation and interference rejection performance (Band 1 demodulation)

6.3.2 Receiver front-end measurement results

In order to characterize the receiver functionality as completely as possible, the RF front-end of the receiver as defined in Fig. 6.1 was fabricated separately and measurements were carried out by packaging the chip in a Quad Flat pack No lead 48 pin (QFN48) package and mounting it on a Rogers RO4350B RF PCB test bed.

An external Gaussian monocycle pulse generator was used to generate the transmitted UWB pulse train which was subsequently attenuated and fed to the front-end input. The LO frequency was set to the centre frequency of the received wide-band pulse for maximum base-band signal capture. The mixer output is connected to a high impedance external buffer. This not only ensures that testing apparatus can be driven but also acts like a low pass filter due to its finite bandwidth.

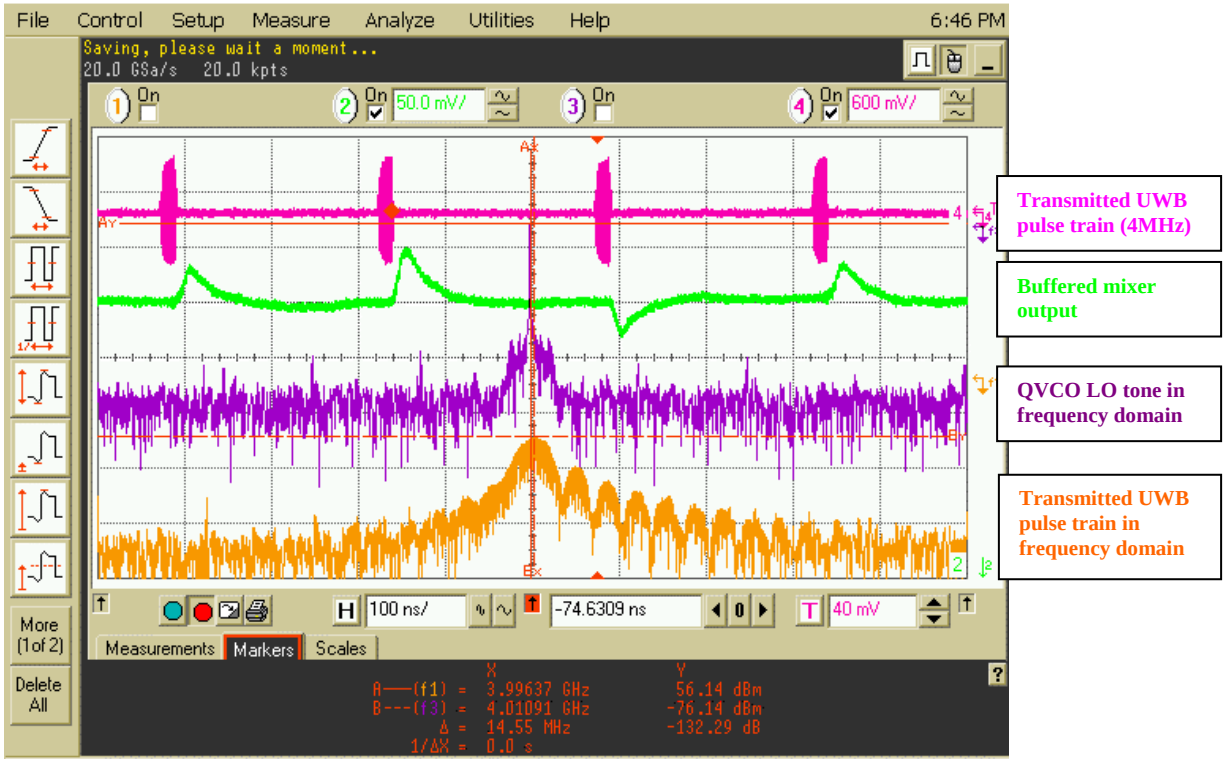


Fig. 6.6 Measured receiver front-end performance

The measured results are shown in Fig. 6.6 and the buffered mixer output clearly shows the demodulated low frequency pulse train and confirms the front-end demodulation functionality.

From the theoretical analysis presented in Chapter 4, we know that in order to ensure robust demodulation using a sinusoidal template, the phase difference between the I and Q LO tones must be kept as close to 90° as possible. The generated LO output was tapped out for measurement and the results in Fig. 6.7 show the LO power to be +2.73dBm with I/Q phase mismatch less than $\pm 3.5^o$. The front-end measurements also showed the LNA gain and NF to be 30dB and less than 6.1 dB respectively while the mixer conversion gain for the desired UWB bandwidth is +5dB.

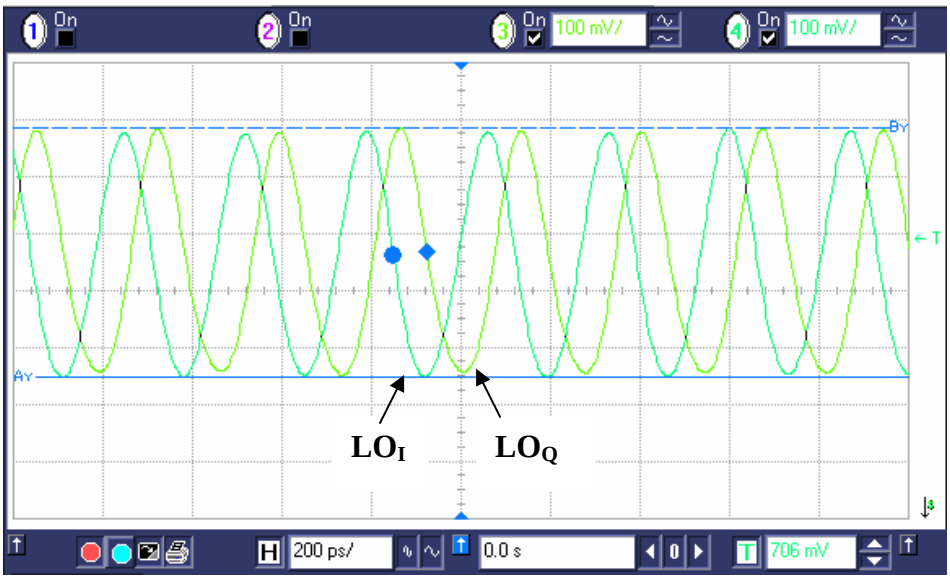


Fig. 6.7 QVCO I and Q single-ended outputs at 3.6 GHz

6.3.3 Integrated receiver measurement results

The integrated receiver chain contains all the elements of the RF front end and the analog back end. The receiver chip was packaged in a QFN56 package and again tested

on a Rogers PCB test bed. Since the baseband section is not included in the test IC, the digital control for the DAC was provided on the PCB level through switches. An FSK modulated pseudo-random bit sequence was generated through an external UWB transmitter and supplied to the receiver after attenuation. The demodulation performance of the receiver was then tested by proper calibration of the various sub-blocks as described in the previous sections in order to recover the data in the 2 sub-bands independently. Fig. 6.8 and Fig. 6.9 show the results of demodulation process in both Band1 and Band2 and they correspond well with the simulated response of Fig. 6.4 and Fig. 6.5.

A summary of the key metrics of the proposed system is reported in Table III together with a brief comparison against other recent publications addressing interference robust UWB communication using conventional approaches.

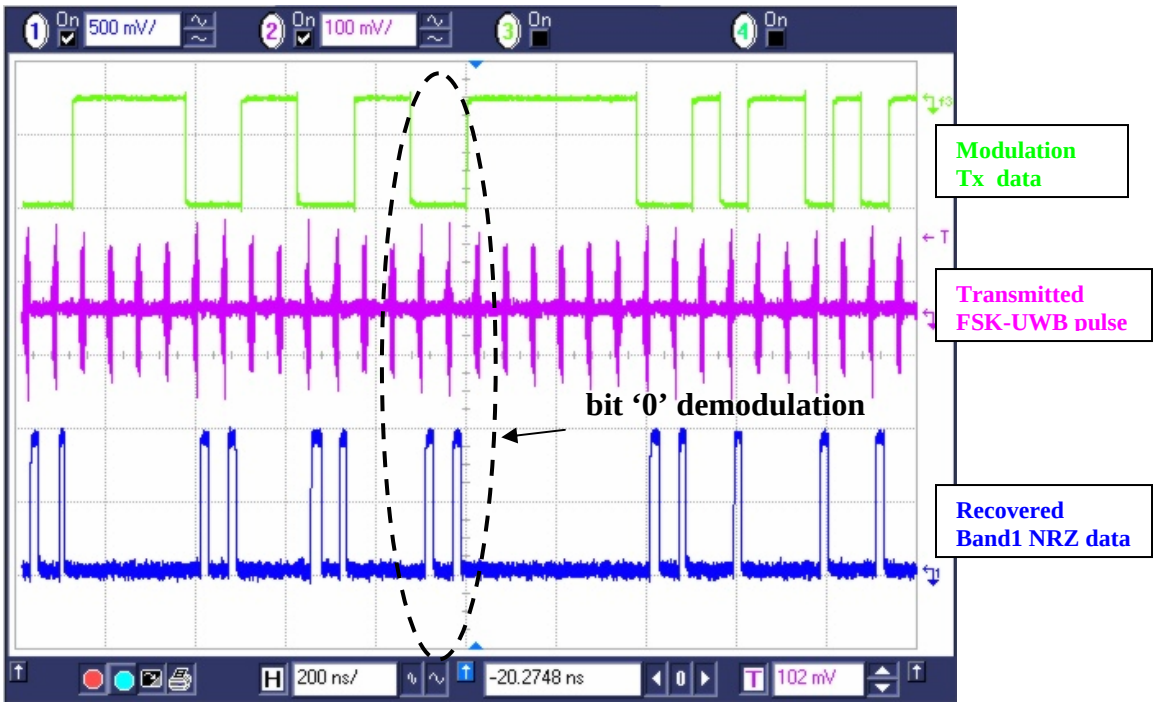


Fig. 6.8 Receiver demodulated output of UWB FSK signal in Band '1'

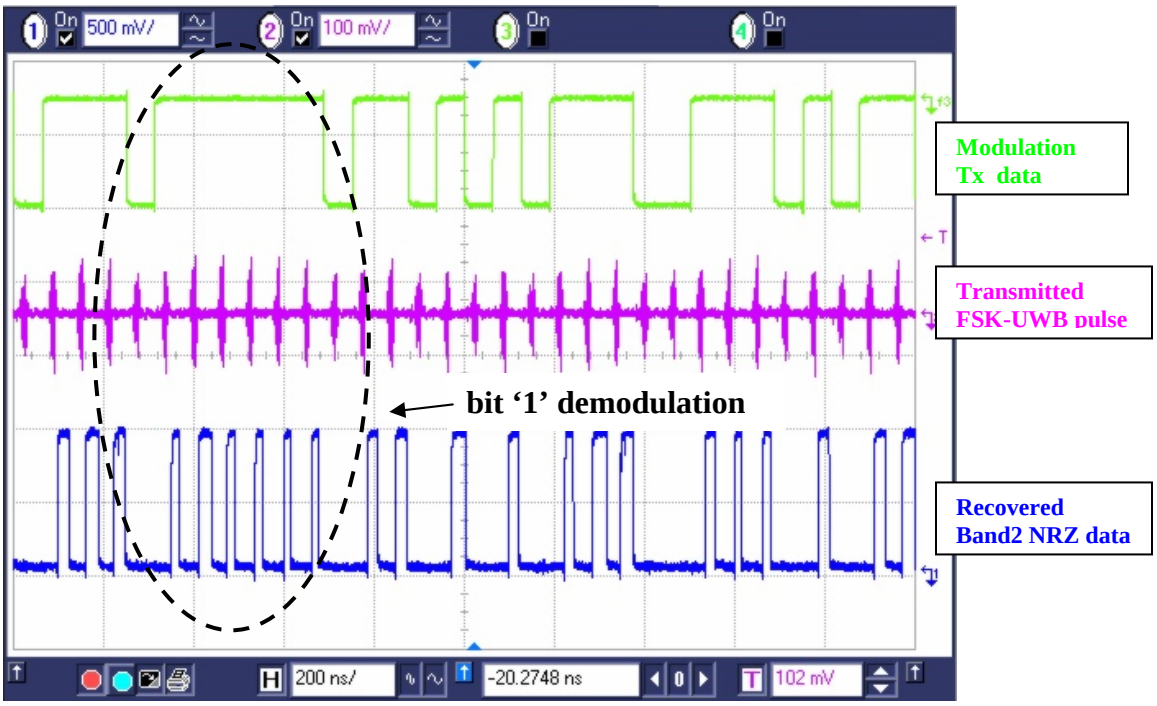


Fig. 6.9 Receiver demodulated output of UWB FSK signal in Band '2'

Table III: Summary of measured receiver performance and benchmarking against state of the art in publication

Author / Institution	This work	Lee et al. / MIT [16]	Ryckaert et al. / IMEC [18]	Medi et al. / UCLA [15]
Product / Publication	-	ISSCC 2007	JSSC 2007	JSSC 2008
Approach	FSK Quad. energy detection Rx	Sub-banded PPM Rx	Quad. Analog Corr. PPM Rx	Channelized BPSK TxRx
Technology / Supply	0.18µm CMOS 1.8 V	90nm CMOS 0.65 V	0.18µm CMOS 1.8 V	0.18µm CMOS 1.8 V
Sensitivity (BER)	-88 dBm (10^{-5})	-99 dBm (10^{-3})	-75 dBm	-
Out-of-band SIR (10^{-3} BER)	-60 dB	-51 dB	-33 dB	0 dBm (int. power level)
In-band SIR (10^{-3} BER)	-19 dB	-15 dB	-23 dB †	-20 dBm (int. power level)
Data rate	25 MHz	0 - 16.7 MHz	< 1 MHz	1 Gbps
Power	2.7-4.95nJ/b	2.5nJ/b	1.44nJ/b	98pJ/b

† Only measured for in-band interference signals > 250MHz away from the transmitted signal center frequency

Chapter 7

Conclusion and Future Directions

7.1 Conclusions

A new dual-band FSK modulation scheme is proposed for I-UWB applications and a receiver that can successfully implement this scheme have been presented. The utilization of FSK serves as a mean to increase the diversity gain of the system, hence making it ideally suited for robust demodulation in noisy and interference-ridden channels. In addition, this scheme significantly relaxes the requirements of narrow and high swing pulses which limit the scalability of traditional UWB systems to advanced low supply voltage technologies. The feasibility of system and the performance of the receiver were confirmed through extensive simulations and measurement results.

Many of the circuit blocks needed for the receiver were designed from scratch and some innovative circuit structures were explored and used. A UWB LNA utilizing active inductors in order to obtain drastic chip area savings was presented. A hybrid UWB mixer structure which combines the gate-source injection and Gilbert cell topologies in order to extend the operational bandwidth without compromising conversion gain has been implemented. A 4-bit R-2R resistor ladder DAC capable of less than 0.5 LSB INL and DNL performance with less than 25ns settling time for maximum output voltage swing has been designed. A four quadrant baseband squarer with a squaring gain of 65

and a dual threshold comparator with more than 700mV hysterisis, excellent signal integrity and good load driving capabilities have also been designed. All blocks were designed using CSM 0.18μm technology models. Integration and layout challenges have been discussed in detail and system level design considerations as well as meticulous layout techniques that were used to ensure proper functionality have been reported.

The fabricated receiver achieves a sensitivity of -88 dBm for a very robust BER of 10^{-5}. The maximum achievable data rate for the receiver is 25 MHz with an energy efficiency of 2.7 to 4.95 nJ/b. The benefits of the proposed UWB FSK communication scheme for interference mitigation have also been confirmed and the receiver can achieve 10^{-3} BER demodulation while tolerating as low as -19 dB/ -60 dB in/out of band signal to interference ratio (SIR).

7.2 Future Directions

1) The fabricated receiver needs further rigorous testing for robustness in real-life indoor noisy environment.
2) Ways to minimize the total number of components required for this system need to be found in order to lower the chip area and power consumption.
3) The active inductor based LNA will be modified and utilized as a second amplification stage to achieve drastic overall area reduction.
4) The baseband section needed for full implementation of the proposed system will be integrated on to the same IC.
5) The suitability of the proposed wide-band FSK modulation scheme to incorporate

added functionalities such as localization needs further exploration.

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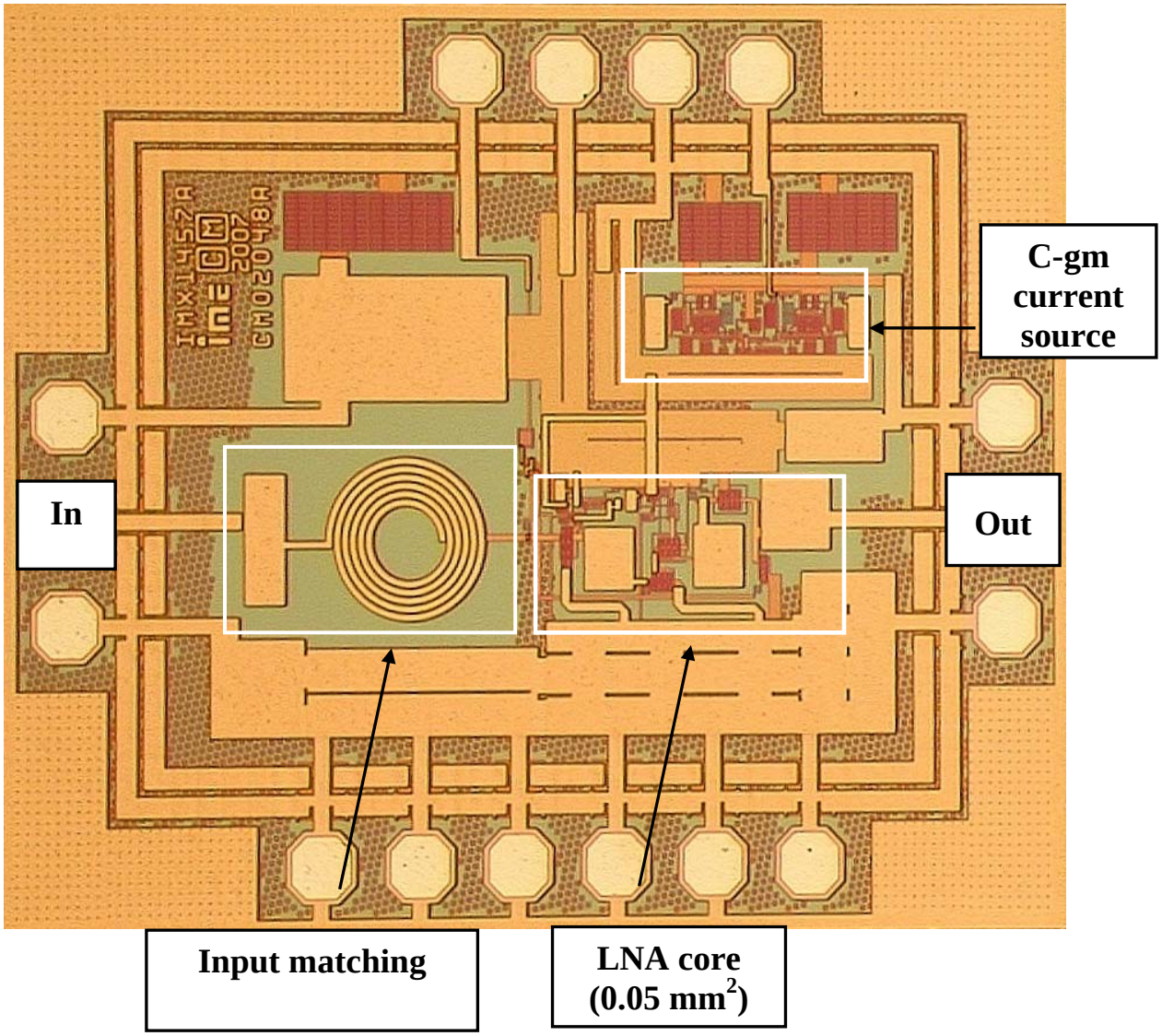
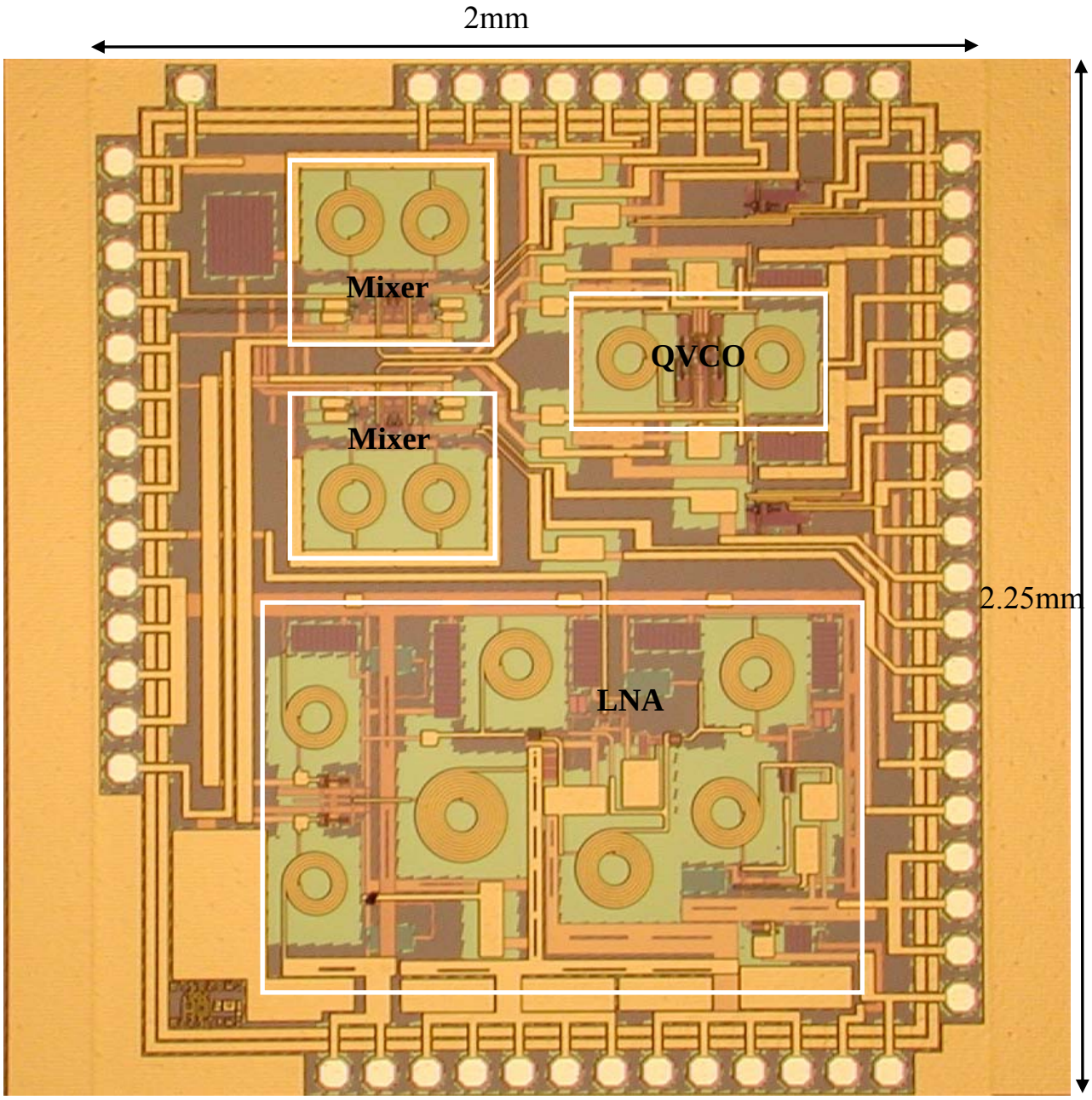
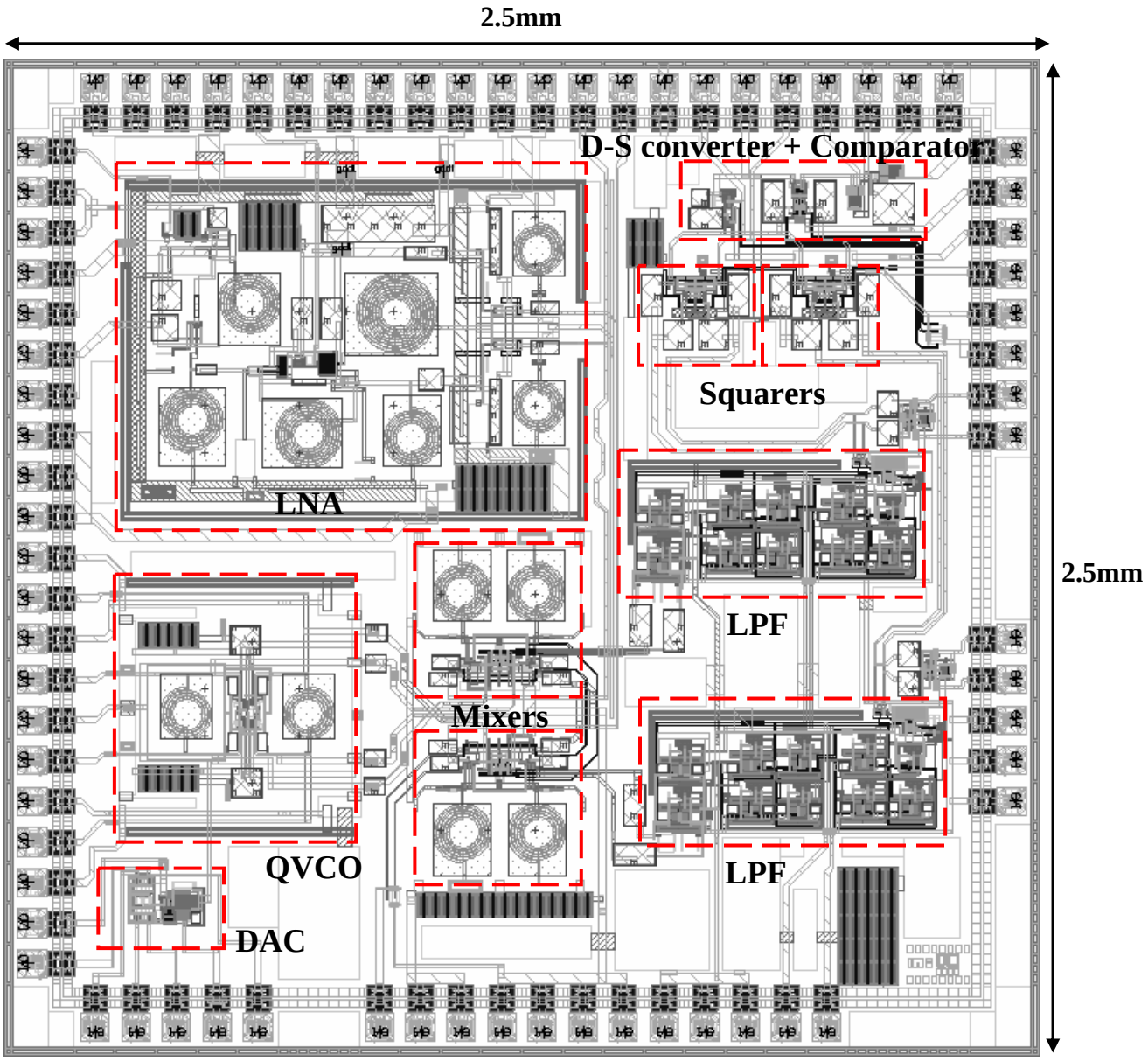
Appendix A – Active Inductor based UWB LNA die photo



Appendix B –
Dual-band UWB FSK receiver integrated front-end die photo



Appendix C –
Dual-band UWB FSK fully integrated receiver layout



Appendix D – Publication List

P1: M. Nair, Y. Zheng, and Y. Lian, "An Active Inductor based Low-Power UWB LNA" *IEEE International. Conference on Ultra Wideband,* pp. 813 – 816, Sep. 2007.

P2: M. Nair, Y. Zheng, and Y. Lian, "A 1V, 0.18µm area and power efficient UWB LNA utilizing active inductors" *IEE Electronics Letters,* vol. 44, No. 19, pp. 1127 – 1129, Sep. 2008.

P3: M. Nair, Y. Zheng, and Y. Lian, "A dual-band FSK receiver for interference robust UWB-IR applications" *IEEE Transactions on Circuits and Systems I,* "To be submitted"

(Patent disclosed in Oct. 2007)